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MICROCOMPUTER PRODUCTS

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DATA BOOK

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1983/1984 MICROCOMPUTER CATALOG

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GENERAL INFORMATION 2

MICROCOMPUTER SELECTION GUIDE

SINGLE CHIP 4-BIT MICROCOMPUTERS

DEVICE	FAMILY	ROM	RAM	I/O	PROCESS	OUTPUT	FEATURES	SUPPLY VOLTAGE	PINS
μPD553	μCOM-43H	2000 × 8	96 × 4	35	PMOS	O.D.	A	−10	42
μPD557L	μCOM-43SL	2000 × 8	96 × 4	21	PMOS	O.D.	A	−8	28
μPD552	μCOM-44H	1000 × 8	64 × 4	35	PMOS	O.D.	A	−10	42
μPD550	μCOM-45	640 × 8	32 × 4	21	PMOS	O.D.	A	−10	28
μPD550L	μCOM-45L	640 × 8	32 × 4	21	PMOS	O.D.	A	−8	28
μPD554	μCOM-45	1000 × 8	32 × 4	21	PMOS	O.D.	A	−10	28
μPD554L	μCOM-45L	1000 × 8	32 × 4	21	PMOS	O.D.	A	−8	28
μPD556B	μCOM-43	External	96 × 4	35	PMOS	O.D.	B	−10	64
MC-430P	μCOM-43	2000 × 8 UV EPROM	96 × 4	35	PMOS	O.D.	G	−10	42
μPD7500	μPD7500 Series	External	256 × 4	46	CMOS	O.D.	C	+2.7 to 5.5	64
μPD7501	μPD7500 Series	1024 × 8	96 × 4	24	CMOS	O.D.	D	+2.7 to 5.5	64
μPD7502	μPD7500 Series	2048 × 8	128 × 4	23	CMOS	O.D.	D	+2.7 to 5.5	64
μPD7503	μPD7500 Series	4096 × 8	224 × 4	23	CMOS	O.D.	D	+2.7 to 5.5	64
μPD7506	μPD7500 Series	1024 × 8	64 × 4	22	CMOS	O.D.		+2.7 to 5.5	28
μPD7507	μPD7500 Series	2048 × 8	128 × 4	32	CMOS	O.D.		+2.7 to 5.5	40/52
μPD7507S	μPD7500 Series	2048 × 8	128 × 4	20	CMOS	O.D.		+2.7 to 5.5	28
μPD7508	μPD7500 Series	4096 × 8	224 × 4	32	CMOS	O.D.		+2.7 to 5.5	40/52
μPD7508H	μPD7500 Series	4096 × 8	224 × 4	32	CMOS	O.D.		+2.7 to 5.5	40/52
μPD7508A	μPD7500 Series	4096 × 8	208 × 4	32	CMOS	O.D.	A	+2.7 to 5.5	40
μPD7519	μPD7500 Series	4096 × 8	256 × 4	28	CMOS	O.D.	F	+2.7 to 5.5	64
μPD7520	μPD7500 Series	768 × 8	48 × 4	24	PMOS	O.D.	E	−6 to −10	28
μPD7514	μPD7500 Series	4096 × 8	256 × 4	31	CMOS	O.D.	D	+2.7 to 5.5	80
μPD7528/38	μPD7500 Series	4096 × 8	160 × 4	35	CMOS	O.D.	A	+2.7 to 5.5	42
μPD7527/37	μPD7500 Series	2048 × 8	160 × 4	35	CMOS	O.D.	A	+2.7 to 5.5	42

Notes. A = −35V VF Display Drive
B = μCOM-4 Evaluation Chip
C = μPD750X Evaluation Chip
D = LCD Controller/Driver
E = LED Display Controller/Driver
F = VF Display Controller/Driver
G = Pin-Compatible with μPD546
O.D. = Open Drain

MICROCOMPUTER SELECTION GUIDE

SINGLE CHIP 8-BIT MICROCOMPUTERS

DEVICE	SPECIAL FEATURES	ROM	RAM	I/O	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGE	PINS
μPD8021	Zero-Cross Detector	1024 × 8	64 × 8	21	NMOS	BD	3.6 MHz	+5	28
μPD8035HL	μPD8048 w/External Memory	External	64 × 8	27	HMOS	TS, BD	6 MHz	+5	40
μPD8039HL	μPD8049 w/External Memory	External	128 × 8	27	HMOS	TS, BD	11 MHz	+5	40
μPD8041	Peripheral Interface w/Slave Bus	1024 × 8	64 × 8	18	NMOS	TS, BD	6 MHz	+5	40
μPD8041A	Enhanced μPD8041	1024 × 8	64 × 8	18	NMOS	TS, BD	6 MHz	+5	40
μPD8048H	Expansion Bus	1024 × 8	64 × 8	27	HMOS	TS, BD	6 MHz	+5	40
μPD8049H	High Speed μPD8048	2048 × 8	128 × 8	27	HMOS	TS, BD	11 MHz	+5	40
μPD8741A	UV-EPROM μPD8041A	1024 × 8	64 × 8	18	NMOS	TS, BD	6 MHz	+5	40
μPD8748	UV-EPROM μPD8048	1024 × 8	64 × 8	27	NMOS	TS, BD	6 MHz	+5	40
μPD8749H	UV-EPROM μPD8049	2048 × 8	128 × 8	27	HMOS	TS, BD	11 MHz	+5	40
μPD80C35	CMOS 8035	External	64 × 8	27	CMOS	TS, BD	6 MHz	+2.7 to 5.5	40
μPD80C48	CMOS 8048	1024 × 8	64 × 8	27	CMOS	TS, BD	6 MHz	+2.7 to 5.5	40
μPD80C39	CMOS 8039	External	128 × 8	27	CMOS	TS, BD	8 MHz	+2.7 to 5.5	40
μPD80C39H	CMOS 8039H	External	128 × 8	27	CMOS	TS, BD	12 MHz	+2.7 to 5.5	40
μPD80C49	CMOS 8049	2048 × 8	128 × 8	27	CMOS	TS, BD	8 MHz	+2.7 to 5.5	40
μPD80C49H	CMOS 8049H	2048 × 8	128 × 8	27	CMOS	TS, BD	12 MHz	+2.7 to 5.5	40
μPD7800	Development Chip	External	128 × 8	48	NMOS	TS, BD	4 MHz	+5	64
μPD7801	8080 Expansion Bus 64K Memory Address Space	4096 × 8	128 × 8	48	NMOS	TS, BD	4 MHz	+5	64
μPD7802	Expanded μPD7801	6144 × 8	64 × 8	48	NMOS	TS, BD	4 MHz	+5	64
μPD78C05	CMOS Microprocessor	External	128 × 8	46	CMOS	TS, BD	4 MHz	+5	64
μPD78C06	CMOS Microcomputer	4096 × 8	128 × 8	46	HCMOS	TS, BD	4 MHz	+5	64
μPD7807	7809 w/Ext. Memory	External	256 × 8	40	HMOS	TS, BD	12 MHz	+5	64
μPD7809	8/16 Bit Microcomputer	8192 × 8	256 × 8	40	HMOS	TS, BD	12 MHz	+5	64
μPD7810	Romless μPD7811	External	256 × 8	44	NMOS	TS, BD	12 MHz	+5	64
μPD7811	8 Channel A/D/8-16 Bit Micro	4096 × 8	128 × 8	44	NMOS	TS, BD	12 MHz	+5	64

MICROPROCESSORS

DEVICE	PRODUCT	SIZE	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD780	Microprocessor	8-bit	NMOS	3-State	2.5 MHz	+5	40
μPD780-1	Microprocessor	8-bit	NMOS	3-State	4.0 MHz	+5	40
μPD780-2	Microprocessor	8-bit	NMOS	3-State	6.0 MHz	+5	40
μPD8085A	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+5	40
μPD8085A-2	Microprocessor	8-bit	NMOS	3-State	5.0 MHz	+5	40
μPD8085AH	Microprocessor	8-bit	NMOS	3-State	3.0 MHz	+5	40
μPD8086	Microprocessor	16-bit	NMOS	3-State	5.0 MHz	+5	40
μPD8086-2	Microprocessor	16-bit	NMOS	3-State	8.0 MHz	+5	40
μPD8088	Microprocessor	8-bit	NMOS	3-State	5.0 MHz	+5	40

MICROCOMPUTER SELECTION GUIDE

SYSTEM SUPPORT

DEVICE	PRODUCT	SIZE	PROCESS	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
μPD765A	Double Sided/Double Density Floppy Disk Controller	8-bit	NMOS	3-State	8 MHz	+5	40
μPD7201A	Multi-Protocol Serial Controller	8-bit	NMOS	3-State	4 MHz	+5	40
μPD7210	IEEE Controller (Talker, Listener, Controller)	8-bit	NMOS	3-State	8 MHz	+5	40
μPD7220	Color Graphic Display Controller	8-bit	NMOS	3-State	5 MHz	+5	40
μPD7225	Alpha Numeric LCD Controller/Driver	8-bit	CMOS	–	–	2.7 to 5.5	52
μPD7227	Dot Matrix LCD Controller/Driver	8-bit	CMOS	–	–	2.7 to 5.5	64
μPD7228	Dot Matrix LCD Controller/Driver	8-bit	CMOS	–	–	2.7 to 5.5	80
μPD7720	Signal Processor	16-bit	NMOS	3-State	8 MHz	+5	28
μPD77P20	EPROM Version of μPD7720	16-bit	NMOS	3-State	8 MHz	+5	28
μPD8155H	256 x 8 RAM with I/O Ports and Timer	8-bit	HMOS	3-State	–	+5	40
μPD8155-2	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPD8156H	256 x 8 RAM with I/O Ports and Timer	8-bit	HMOS	3-State	–	+5	40
μPD8156-2	256 x 8 RAM with I/O Ports and Timer	8-bit	NMOS	3-State	–	+5	40
μPB8212	I/O Port	8-bit	Bipolar	3-State	–	+5	24
μPB8216	Bus Driver Non-Inverting	4-bit	Bipolar	3-State	–	+5	16
μPB8226	Bus Driver Inverting	4-bit	Bipolar	3-State	–	+5	16
μPD8243	I/O Expander	4 x 4 bits	NMOS	3-State	–	+5	24
μPD82C43	I/O Expander	4 x 4 bits	CMOS	3-State	–	+5	24
μPD8251A/AF	Programmable Communications Interface (Async/Sync)	8-bit	NMOS	3-State	A-9.6K baud S-64K baud	+5	28
μPD8253-2/-5	Programmable Timer	8-bit	NMOS	3-State	4.0 MHz	+5	24
μPD8255A-2/-5	Peripheral Interface	8-bit	NMOS	3-State	–	+5	40
μPD8257-2/-5	Programmable DMA Controller	8-bit	NMOS	3-State	4 MHz	+5	40
μPD8259-2/-5	Programmable Keyboard/Display Interface	8-bit	NMOS	3-State	–	+5	40
μPB8282/8283	8-Bit Latches		Bipolar	3-State	5 MHz	+5	20
μPB8284A	Clock Driver		Bipolar	3-State	5 MHz	+5	18
μPB8286/8287	8-Bit Bus Transceivers		Bipolar	3-State	5 MHz	+5	20
μPB8288	Bus Controller		Bipolar	3-State	5 MHz	+5	20
μPB8289	Bus Arbiter		Bipolar	3-State	5 MHz	+5	20
μPD8355/-2/A	2048 x 8 ROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40
μPD8755A	2048 x 8 EPROM with I/O Ports	8-bit	NMOS	3-State	–	+5	40
μPD8759A/A-2	Programmable Interrupt Controller	8-bit	HMOS	3-State	5/8 MHz	+5	28
SPEECH PRODUCTS							
μPD7751	ADPCM Speech Synthesizer	8-bit	NMOS	3-State	6 MHz	+5	40
μPD7752	Formant Speech Synthesizer	8-bit	CMOS	3-State	3 6 MHz	+5	28
μPD7761 μPD7762 μMC-4760	K 3 Chip-SR Speech Recognition Chip Set	16-bit 8-bit –	NMOS NMOS Hybrid	3-State 3-State 3-State	8 MHz 4 MHz 2 MHz	+5 +5 +5, ±12	28 64 24

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	AM8085A	Microprocessor (3.0 MHz)	μPD8085A
	AM8155	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155
	AM8156	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156
	AM8212	I/O Port (8-Bit)	μPB8212
	AM8214	Priority Interrupt Controller	μPB8214
	AM8216	Bus Driver, Inverting	μPB8216
	AM8226	Bus Driver, Non-Inverting	μPB8226
	AM8251	Programmable Communications Interface	μPD8251
	AM8255	Programmable Peripheral Interface	μPD8255
	AM8257	Programmable DMA Controller	μPD8257
	AM8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	AM8048	Single Chip Microcomputer	μPD8048
AMI	7500 Family	4-Bit CMOS Microcomputer	μPD750X
	78C06/78C05	8-Bit CMOS Microcomputer	μPD78C06/78C05
	7810/7811	16-Bit High-Performance Microcomputer	μPD7810/7811
	7807/7809	16-Bit High-Performance Microcomputer	μPD7807/7809
	7720	Signal Processor	μPD7720
INTEL	8021	Microcomputer with ROM	μPD8021
	8035HL	Microprocessor	μPD8035HL
	8039HL	Microprocessor	μPD8039HL
	8041A	Programmable Peripheral Controller with ROM	μPD8041A
	8048H	Microcomputer with ROM	μPD8048H
	8049H	Microcomputer with ROM	μPD8049H
	8085A	Microprocessor (3.0 MHz)	μPD8085A
	8085A-2	Microprocessor (5.0 MHz)	μPD8085A-2
	8086	Microprocessor (16-Bit)	μPD8086
	8155/8155-2	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155/8155-2
	8156/8156-2	Programmable Peripheral Interface with 256 x 8 RAM	μPD8156/8156-2
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8226	Bus Driver, Inverting	μPB8226
	8243	I/O Expander	μPD8243

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
INTEL (CONT.)	8251A	Programmable Communications Interface (Async/Sync)	μPD8251A
	8253-5	Programmable Timer	μPD8253-5
	8255A-5	Programmable Peripheral Interface	μPD8255A-5
	8257-5	Programmable DMA Controller	μPD8257-5
	8259A	Programmable Interrupt Controller	μPD8259A
	8272	Double Sided/Double Density Floppy Disk Controller	μPD765
	8279-5	Programmable Keyboard/Display Interface	μPD8279-5
	8282/8283	8-Bit Latches	μPB8282/8283
	8284	Clock Driver	μPB8284
	8286/8287	8-Bit Transceivers	μPB8286/8287
	8288	Bus Controller	μPB8288
	8355	Programmable Peripheral Interface with 2048 x 8 ROM	μPD8355
	8741A	Programmable Peripheral Controller with EPROM	μPD8741A
	8748	Microcomputer with EPROM	μPD8748
	8749H	Microcomputer with EPROM	μPD8749H
	8755A	Programmable Peripheral Interface with 2K x 8 EPROM	μPD8755A
	8274	Multiprotocol Serial Controller	μPD7201
NATIONAL	INS8048	Microcomputer with ROM	μPD8048
	INS8049	Microcomputer with ROM	μPD8049
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8226	Bus Driver, Inverting	μPB8226
	INS8251	Programmable Communications Interface	μPD8251A
	INS8253	Programmable Timer	μPD8253-5
	INS8255	Programmable Peripheral Interface	μPD8255A-5
	INS8257	Programmable DMA Controller	μPD8257-5
	INS8259	Programmable Interrupt Controller	μPD8259A
T.I.	SN74S412	I/O Port (8-Bit)	μPB8212

ROM-BASED PRODUCTS ORDERING PROCEDURE

The following NEC products fall under the guidelines set by the ROM-based Products Ordering Procedure:

μPD7801	μPD80C48	μPD554L	μPD7508A	μPD2308A
μPD7802	μPD8049H	μPD557L	μPD7508H	μPD2316E
μPD78C06	μPD80C49	μPD7501	μPD7514	μPD2332
μPD7807	μPD8355	μPD7502	μPD7519	μPD2364
μPD7808	μPD550	μPD7503	μPD7520	μPD2380
μPD7811	μPD550L	μPD7506	μPD7527	μPD23128
μPD8021	μPD552	μPD7507	μPD7528	μPD23256
μPD8041AH	μPD553	μPD7507S	μPD7537	μPD231000
μPD8048H	μPD554	μPD7508	μPD7538	μPD23C128
			μPD7720	μPD73128G
				μPD23C256
				μPD731000

NEC Electronics Inc. is able to accept mask patterns in a variety of formats to facilitate the transferral of ROM mask information. These are intended to suit various customer needs and minimize turnaround time. Always enclose a listing of the code and a complete "ROM Code Submission" form. The following is a list of acceptable media for code transferral.

- PROM/EPROM equivalents to ROM devices
- Sample ROMs or ROM-based microcomputers
- ISIS-II compatible 8" floppy disks
- CP/M (® Digital Research Corp.) compatible 8" single-density floppy disk

Thoroughly tested verification procedures protect against unnecessary delays or costly mistakes. NEC Electronics Inc. will return the ROM code patterns to the customer in the most convenient format. Unprogrammed EPROMs, if sent with the ROM code, can be programmed and returned for verification. Earth satellites and the world-wide GE Mark III timesharing systems provide reliable and instant communication of ROM patterns to the factory.

The following is an example of a ROM code transferral procedure. The μPD8048H is used here; however, the process is the same for all other ROM-based products.

1. The customer contacts his local NEC Electronics Inc. Sales Representative, concerning a ROM pattern for the μPD8048H that he would like to send.

2. Since an EPROM version of that part is available, the μPD8748 is proposed as a code transferral medium. Alternatively, a μPD2716 or a floppy disk may be used.

3. Two programmed μPD8748s are sent to NEC Electronics Inc., along with a listing and the "ROM Code Submission" form. A floppy disk may also be sent as back-up.

4. NEC Electronics Inc. compares the media provided and enters the code into GE-TSS. The GE-TSS file is accessed at the NEC factory and a copy of the code is returned to NEC Electronics Inc. for verification. One of the μPD8748s is erased and reprogrammed with the customer's code as the NEC factory has it. The μPD8748s, a listing, and a "ROM Code Verification" form are returned to the customer for final verification.

5. Once the customer has notified NEC Electronics Inc. *in writing* that the code is verified, and has provided both the mask charge payment and a hard-copy purchase order, work begins immediately on production of his μPD8048Hs.

Please contact your local Sales Representative for assistance with all ROM-based product orders.

NEC

ROM Code Submission

To: **NEC Electronics Inc.**
252 Humboldt Court
Sunnyvale, CA 94086

Date: _____

Attn ROM-Based Product Administrator

We are ready to place our purchase order for our _____ (Customer Part Number), your _____ (NEC Part Number), and are submitting **Two** copies of the ROM Code on the following medium/media (Please check all applicable boxes):

- ☐ μPD2716
- ☐ μPD2732
- ☐ μPD2764
- ☐ μPD27128
- ☐ μPD8741A
- ☐ μPD8748
- ☐ μPD8749H
- ☐ μPD8755A
- ☐ CP/M® compatible 8" single-density floppy disk
- ☐ Intel ISIS-II compatible 8" single-density floppy disk
- ☐ Intel ISIS-II compatible 8" double-density floppy disk

Please manufacture this device with the special marking._____, and with the I/O Port Loading Options (available only on the μPD7519, μPD7527, μPD7528, μPD7537, μPD7538, μPD8021, μPD80C48, and μPD80C49, and not available on all other NEC ROM-Based Products) selected on the back of this page

The mask charge payment and the ROM code listing are also enclosed

Please return the processed ROM code to the following individual for our verification

_____
Name

_____
Company

_____
Division

_____
Shipping Address (not a P O Box please)

_____
City State Zip

_____
Telephone Number

Send this form along with the ROM code, a listing, and the mask charge payment, in a package clearly marked with "ROM CODE ENCLOSED" to the attention of the ROM-Based Product Administrator at the address above

CP/M is a registered trademark of Digital Research Corp

Device	Port	I/O Port Loading Option	
μPD7519	S0	☐ open drain	☐ pull-down resistor to V_{LOAD}
	S1	☐ open drain	☐ pull-down resistor to V_{LOAD}
	S2	☐ open drain	☐ pull-down resistor to V_{LOAD}
	S3	☐ open drain	☐ pull-down resistor to V_{LOAD}
	S4	☐ open drain	☐ pull-down resistor to V_{LOAD}
	S5	☐ open drain	☐ pull-down resistor to V_{LOAD}
	S6	☐ open drain	☐ pull-down resistor to V_{LOAD}
	S7	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T8/S8	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T9/S9	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T10/S10	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T11/S11	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T12/S12	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T13/S13	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T14/S14	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T15/S15	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T0	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T1	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T2	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T3	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T4	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T5	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T6	☐ open drain	☐ pull-down resistor to V_{LOAD}
	T7	☐ open drain	☐ pull-down resistor to V_{LOAD}
μPD7527 μPD7528 μPD7537 μPD7538	$P0_0/INT_0$	☐ direct connection (no zero-crossing detector)	☐ zero-crossing detector
	$P2_3$-$P2_1$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P3_3$-$P3_0$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P4_3$-$P4_0$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P5_3$-$P5_0$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P8_0$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P8_1$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P8_2$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P8_3$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P9_0$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P9_1$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P9_2$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P9_3$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P10_0$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P10_1$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P10_2$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P10_3$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P11_0$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P11_1$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P11_2$	☐ open drain	☐ pull-down resistor to V_{LOAD}
	$P11_3$	☐ open drain	☐ pull-down resistor to V_{LOAD}
μPD8021	T1	☐ zero-crossing detector	☐ TTL-compatible
	P00-P07	☐ open drain	☐ TTL-compatible
μPD80C48 μPD80C49	P10-P17	☐ CMOS (-5μA)	☐ TTL-compatible (-50μA)
	P20-P23	☐ CMOS (-5μA)	☐ TTL-compatible (-50μA)
	P24-P27	☐ CMOS (-5μA)	☐ TTL-compatible (-50μA)

NEC

SINGLE CHIP 4-BIT MICROCOMPUTERS

3

4-BIT SINGLE CHIP MICROCOMPUTER FAMILY

DESCRIPTION

The μCOM-4 4-bit Microcomputer Family is a broad product line of 14 individual devices designed to fulfill a wide variety of design criteria. The product line shares a compatible architecture and instruction set. The architecture includes all functional blocks necessary for a single chip controller, including an ALU, Accumulator, Byte-wide ROM, RAM, and Stack. The instruction set maximizes the efficient utilization of the fixed ROM space, and includes a variety of Single Bit Manipulation, Table Look-Up, BCD arithemetic, and Skip instructions.

The μCOM-4 Microcomputer Family includes seven different products capable of directly driving 35V Vacuum Fluorescent Displays. Four products are manufactured with a CMOS process technology. μCOM-4 Microcomputers are ideal for low-cost general purpose controller applications such as industrial controls, instruments, appliance controls, intelligent VF display drivers, and games.

FEATURES

- Choice of ROM size: 2000 x 8, 1000 x 8, or 640 x 8
- Choice of RAM size: 96 x 4, 64 x 4, or 32 x 4
  - Six 4-Bit Working Registers Available
  - One 4-Bit Flag Register Available
- Powerful Instruction Set
  - Choice of 80 or 58 Instructions
  - Table Look-Up Capability with CZP and JPA Instructions
  - Single Bit Manipulation of RAM or I/O Ports
  - BCD Arithmetic Capability
- Choice of 3-Level, 2-Level, or 1-Level Subroutine Stack
- Extensive I/O Capability
  - Choice of 35 or 21 I/O Lines

	42/52-Pin Packages	28-Pin Package
– 4-Bit Input Ports	2	1
– 4-Bit I/O Ports	2	2
– 4-Bit Output Ports	4	2
– 3-Bit Output Ports	1	–
– 1-Bit Output Port	–	1

- Programmable 6-Bit Timer Available
- Choice of Hardware or Testable Interrupt
- Built-In Clock Signal Generation Circuitry
- Built-In Reset Circuitry
- Single Power Supply
- Low Power Consumption
- PMOS or CMOS Technologies
- Choice of 42-pin DIP, 28-pin DIP, or 52-pin Flat Plastic Package

Internal Registers

The ALU, the Accumulator, and the Carry Flag together comprise the central portion of the μCOM-4 Microcomputer Family architecture. The ALU performs the arithmetic and logical operations and checks for various results. The Accumulator stores the results generated by the ALU and acts as the major interface point between the RAM, the I/O ports, and the Data Pointer registers. The Carry F/F can be addressed directly, and can also be set during an addition. The μPD546, μPD553, μPD557L, and μPD650 also have a Carry Save F/F for storage the value of the Carry F/F.

Data Pointer Registers

The DP_H register and 4-bit DP_L register reside outside the RAM. They function as the Data Pointer, addressing the rows and columns of the RAM, respectively. They are individually accessible and the L register can be automatically incremented or decremented.

RAM

All μCOM-4 microcomputers have a static RAM organized into a multiple-row by 16-column configuration, as follows:

MICROCOMPUTER	RAM	ORGANIZATION	DP_H	DP_L
μPD546, μPD553, μPD557L, and μPD650	96 x 4	6 rows x 16 columns	3	4
μPD547, μPD547L μPD552, and μPD651	64 x 4	4 rows x 16 columns	2	4
μPD550, μPD550L, μPD554, μPD554L, and μPD652	32 x 4	2 rows x 16 columns	1	4

The μPD546, μPD553, μPD557L, and μPD650 also have a 4-bit Flag register and six 4-bit working registers resident in the last row of the RAM. Their extended instruction set provides 10 additional instructions with which you can access or manipulate these seven registers.

ROM

The ROM is the mask-programmable portion of the μCOM-4 Microcomputer which stores the application program. It is organized as follows:

MICROCOMPUTER	ROM	ORGANIZATION	
		FIELDS	PAGES
μPD546, μPD553, μPD557L, and μPD650	2000 x 8	8	16
μPD547, μPD547L, μPD552, μPD651	1000 x 8	8	8
μPD554, μPD554L, and μPD652	1000 x 8	8	8
μPD550 and μPD550L	640 x 8	8	8

FUNCTIONAL DESCRIPTION (CONT.)

Program Counter and Stack Register

The Program Counter contains the address of a particular instruction being executed. It is incremented during normal operation, but can be modified by various JUMP and CALL instructions. The Stack Register is a LIFO push-down stack register used to save the value of the Program Counter when a subroutine is called. It is organized as follows:

MICROCOMPUTER	STACK ORGANIZATION	ALLOWABLE SUBROUTINE CALLS
μPD546, μPD553, μPD557L, and μPD650	3 words x 11 bits	3 Levels
μPD651	2 words x 10 bits	2 Levels
μPD547, μPD547L, and μPD552	1 word x 10 bits	1 Level
μPD550, μPD550L, μPD554, μPD554L, and μPD652	1 word x 10 bits	1 Level

Interrupts

All μCOM-4 microcomputers are equipped with a software-testable interrupt which skips an instruction if the Interrupt F/F has been set. The TIT instruction resets the Interrupt F/F.

In addition, the μPD546, μPD553, μPD557L, and μPD650 have a level-triggered hardware interrupt, which causes an automatic stack level shift and interrupt service routine call when an interrupt occurs.

Interval Timer

The μPD546, μPD553, μPD557L, and μPD650 are equipped with a programmable 6-bit interval timer which consists of a 6-bit polynomial counter and a 6-bit binary down counter. The STM instruction sets the initial value of the binary down counter and starts the timing. The polynomial counter decrements the binary down counter when 63 instruction cycles have been completed. When the binary down counter reaches zero, the timer F/F is set. The TTM instruction tests the timer F/F, and skips the next instruction if it is set.

Clock and Reset Circuitry

The Clock Circuitry for any μCOM-4 microcomputer can be implemented by connecting either an Intermediate Frequency Transformer (IFT) and a capacitor, or a Ceramic Resonator and two capacitors, to the CL_0 and CL_1 Inputs. The Power-On-Reset Circuitry for any μCOM-4 microcomputer can be implemented by connecting a Resistor, a Capacitor, and a Diode to the RESET input.

I/O Capability

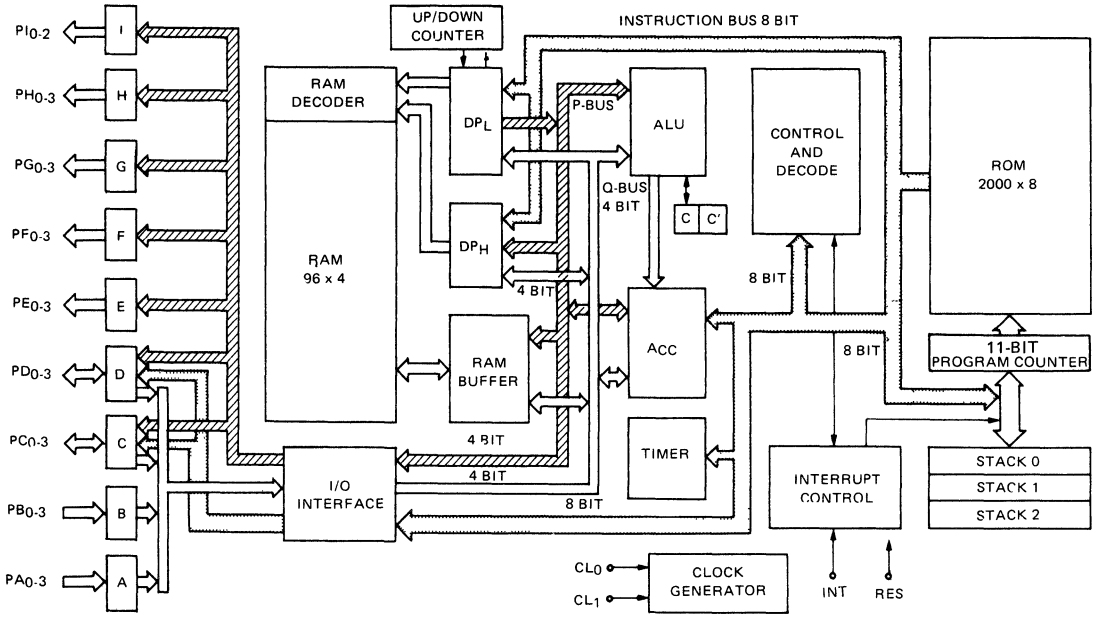
The μCOM-4 microcomputer family devices have either 35 or 21 I/O lines, depending upon the individual device, for communication with and control of external circuitry. They are organized as follows:

PORT	SYMBOL	FUNCTION	μPD546, μPD547, μPD547L, μPD552, μPD553, μPD650, and μPD651	μPD550, μPD550L, μPD554, μPD554L, μPD557L, and μPD652
Port A	PA_{0-3}	4-Bit Input	•	•
Port B	PB_{0-3}	4-Bit Input	•	
Port C	PC_{0-3}	4-Bit Input/Output (VF Drive Possible)	•	•
Port D	PD_{0-3}	4-Bit Input/Output (VF Drive Possible)	•	•
Port E	PE_{0-3}	4-Bit Output (VF Drive Possible)	•	•
Port F	PF_{0-3}	4-Bit Output (VF Drive Possible)	•	•
Port G	PG_{0-3}	4- Bit Output (VF Drive Possible)	•	
	PG_{0-1}	1-Bit Output (VF Drive Possible)		•
Port H	PH_{0-3}	4-Bit Output (VF Drive Possible)	•	
Port I	PI_{0-2}	3-Bit Output (VF Drive Possible)	•	

Development Tools

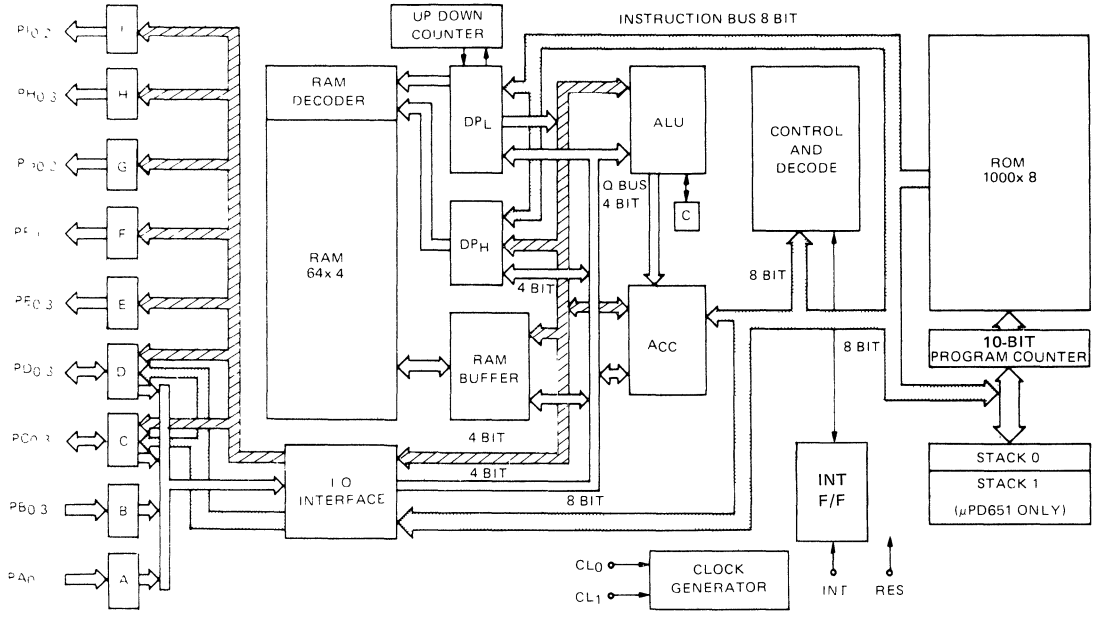
The NEC Development System (NDS) is available for developing software service code, editing, and assembling source code into object code. In addition, the ASM-43 Cross Assembler is available for systems which support either the Intel ISIS-II Operating System or the CP/M (® Digital Research Corp.) Operating System.

The EVAKIT-43P Evaluation Board is available for production device emulation and prototype system debugging. The SE-43P Emulation Board is available for demonstrating the final system design. The μPD556B ROM-less Evaluation Chip is available for small pilot production.

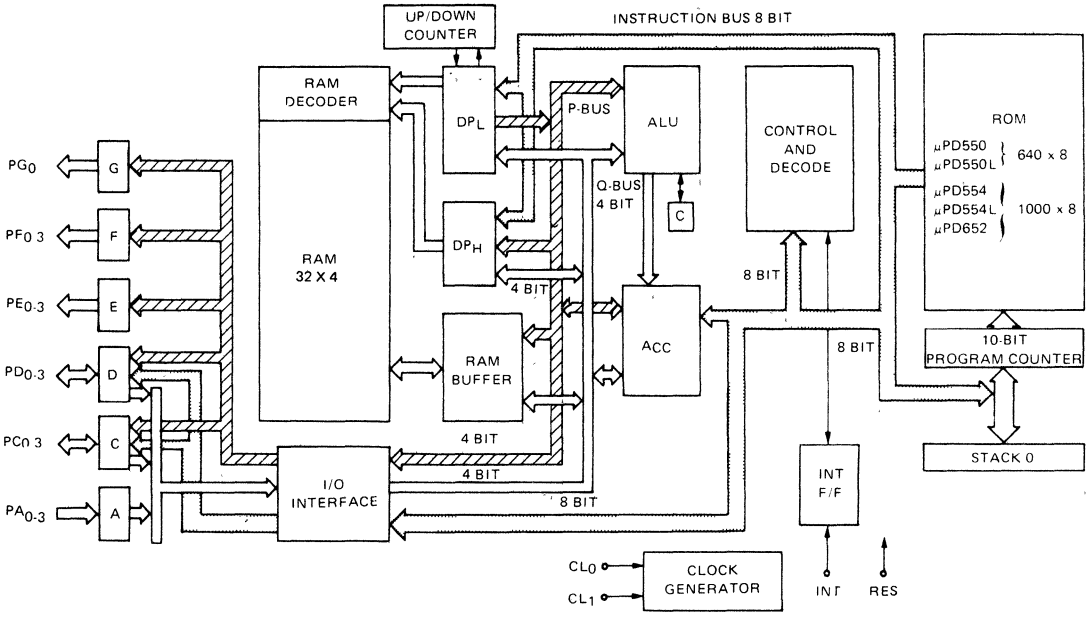


Note Block diagram above applies to μPD546, μPD553, and μPD650 4-bit microcomputers The μPD557L block diagram is similar to the above, except that PB_{0-3}, PG_{1-3}, PH_{0-3}, and PI_{0-2} have been eliminated to accommodate the μPD557L's 28-pin package

μPD547, μPD547L,
μPD552, μPD651
BLOCK DIAGRAM



BLOCK DIAGRAM



INSTRUCTION SET

The μPD546, μPD553, μPD557L, and μPD650 execute all 80 instructions of the extended μCOM-4 instruction set. The 22 additional instructions are indicated by shading.

The μPD547, μPD547L, μPD550, μPD550L, μPD552, μPD554, μPD554L, μPD651, and μPD652 execute a 58 instruction subset of the μCOM-4 instruction set.

INSTRUCTION SET SYMBOL DEFINITIONS

The following abbreviations are used in the description of the μCOM-4 instruction set:

SYMBOL	EXPLANATION AND USE
A_{CC}	Accumulator
A_{CC_n}	Bit "n" of Accumulator
address	Immediate address
C	Carry F/F
C'	Carry Save F/F
data	Immediate data
D_n	Bit "n" of immediate data or immediate address
DP	Data Pointer
DP_H	Upper Bits of Data Pointer
DP_L	Lower 4 Bits of Data Pointer
FLAG	FLAG Register
INTE F/F	Interrupt Enable F/F
INT F/F	Interrupt F/F
P( )	Parallel Input/Output Port addressed by the value within the brackets
P_n	Bit "n" of Program Counter
PA	Input Port A
PC	Input/Output Port C
PD	Input/Output Port D
PE	Output Port E
R	R Register
S	S Register
SKIP	Number of Bytes in next instruction when skip condition occurs
STACK	Stack Register
TC	6-Bit Binary Down Timer Counter
TIMER F/F	Timer F/F
W	W Register
X	X Register
Y	Y Register
Z	Z Register
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
-	Complement
⊻	LOGICAL EXCLUSIVE OR
	Applies to μPD546, μPD553, μPD556B, μPD557L, and μPD650 only

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								BYTES	CYCLES	SKIP CONDITION
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
LOAD													
LI data	$A_{CC} \leftarrow D_{3-0}$	Load A_{CC} with 4 bits of immediate data; execute succeeding LI instructions as NOP instructions	1	0	0	1	D_3	D_2	D_1	D_0	1	1	String
L	$A_{CC} \leftarrow (DP)$	Load A_{CC} with the RAM contents addressed by DP	0	0	1	1	1	0	0	0	1	1	
LM data	$A_{CC} \leftarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$	Load A_{CC} with the RAM contents addressed by DP; Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of Immediate Data, Store the result in DP_H	0	0	1	1	1	0	D_1	D_0	1	1	
LDI data	$DP \leftarrow D_{6-0}$	Load DP with 7 bits of immediate data	0 0	0 D_6	0 D_5	1 D_4	0 D_3	1 D_2	0 D_1	1 D_0	2	2	
LDZ data	$DP_H \leftarrow 0$ $DP_L \leftarrow D_{3-0}$	Load DP_H with 0, Load DP_L with 4 bits of immediate data	1	0	0	0	D_3	D_2	D_1	D_0	1	1	
STORE													
S	$(DP) \leftarrow A_{CC}$	Store A_{CC} into the RAM location addressed by DP	0	0	0	0	0	1	0	0	1	1	
TRANSFER													
TAL	$DP_L \leftarrow A_{CC}$	Transfer A_{CC} to DP_L	0	0	0	0	0	1	1	1	1	1	
TLA	$A_{CC} \leftarrow DP_L$	Transfer DP_L to A_{CC}	0	0	0	1	0	0	1	0	1	1	
TAW	$W \leftarrow A_{CC}$	Transfer A_{CC} to W	0	1	0	0	0	0	1	1	1	2	
TAZ	$Z \leftarrow A_{CC}$	Transfer A_{CC} to Z	0	1	0	0	0	0	1	0	1	2	
THX	$X \leftarrow DP_H$	Transfer DP_H to X	0	1	0	0	0	1	1	1	1	2	
TLY	$Y \leftarrow DP_L$	Transfer DP_L to Y	0	1	0	0	0	1	1	0	1	2	
EXCHANGE													
X	$A_{CC} \leftrightarrow (DP)$	Exchange A with the RAM contents addressed by DP	0	0	1	0	1	0	0	0	1	1	
XI	$A_{CC} \leftrightarrow (DP)$ $DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Exchange A_{CC} with RAM contents addressed by DP, increment DP_L, Skip if $DP_L = 0H$	0	0	1	1	1	1	0	0	1	1 + S	$DP_L = 0H$
XD	$A_{CC} \leftrightarrow (DP)$ $DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Exchange A_{CC} with the RAM contents addressed by DP, decrement DP_L, Skip if $DP_L = FH$	0	0	1	0	1	1	0	0	1	1 + S	$DP_L = FH$
XM data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$	Exchange A_{CC} with the RAM contents addressed by DP, Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data, store the results in DP_H	0	0	1	0	1	0	D_1	D_0	1	1	
XMI data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$ $DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Exchange A_{CC} with the RAM contents addressed by DP, Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data, store the results in DP_H increment DP_L, Skip if $DP_L = 0H$	0	0	1	1	1	1	D_1	D_0	1	1 + S	$DP_L = 0H$
XMD data	$A_{CC} \leftrightarrow (DP)$ $DP_H \leftarrow DP_H \forall D_{1-0}$ $DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Exchange A_{CC} with the RAM contents addressed by DP, Perform a LOGICAL EXCLUSIVE-OR Between DP_H and 2 bits of immediate data, store the results in DP_H decrement DP_L, Skip if $DP_L = FH$	0	0	1	0	1	1	D_1	D_0	1	1 + S	$DP_L = FH$
XAW	$A_{CC} \leftrightarrow W$	Exchange A_{CC} with W	0	1	0	0	1	0	1	1	1	2	
XAZ	$A_{CC} \leftrightarrow Z$	Exchange A_{CC} with Z	0	1	0	0	1	0	1	0	1	2	
XHR	$DP_H \leftrightarrow R$	Exchange DP_H with R	0	1	0	0	1	1	0	1	1	2	
XHX	$DP_H \leftrightarrow X$	Exchange DP_H with X	0	1	0	0	1	1	1	1	1	2	
XLS	$DP_L \leftrightarrow S$ Register	Exchange DP_L with S Register	0	1	0	0	1	1	0	0	1	2	
XLY	$DP_L \leftrightarrow Y$	Exchange DP_L with Y	0	1	0	0	1	1	1	0	1	2	
XC	$C \leftrightarrow C'$	Exchange Carry F/F with Carry Save F/F	0	0	0	1	1	0	1	0	1	1	

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
ARITHMETIC													
AD	$A_{CC} \leftarrow A_{CC} + (DP)$ Skip if overflow	Add the RAM contents addressed by DP to A_{CC}; skip if overflow is generated	0	0	0	0	1	0	0	0	1	1 + S	Overflow
ADC	$A_{CC} \leftarrow A_{CC} + (DP) + C$ if overflow occurs, $C \leftarrow 1$	Add the RAM contents addressed by DP, and the Carry F/F to A_{CC}; if overflow occurs, set carry F/F	0	0	0	1	1	0	0	1	1	1	
ADS	$A_{CC} \leftarrow A_{CC} + (DP) + C$ if overflow occurs, $C \leftarrow 1$ and skip	Add the RAM contents addressed by DP and the carry F/F to A_{CC}, if overflow occurs, set Carry F/F and skip	0	0	0	0	1	0	0	1	1	1 + S	Overflow
DAA	$A_{CC} \leftarrow A_{CC} + 6$	Add 6 to A_{CC} to Adjust Decimal for BCD Addition	0	0	0	0	0	1	1	0	1	1	
DAS	$A_{CC} \leftarrow A_{CC} + 10$	Add 10 to A_{CC} to Adjust Decimal for BCD Subtraction	0	0	0	0	1	0	1	0	1	1	
LOGICAL													
EXL	$A_{CC} \leftarrow A_{CC} \veebar (DP)$	Perform a LOGICAL EXCLUSIVE-OR between the RAM contents addressed by DP and A_{CC}, store the result in A_{CC}	0	0	0	1	1	0	0	0	1	1	
ACCUMULATOR													
CLA	$A_{CC} \leftarrow 0$	Clear A_{CC} to zero	1	0	0	1	0	0	0	0	1	1	String
CMA	$A_{CC} \leftarrow \overline{A_{CC}}$	Complement A_{CC}	0	0	0	1	0	0	0	0	1	1	
CIA	$A_{CC} \leftarrow \overline{A_{CC}} + 1$	Complement A, Increment A	0	0	0	1	0	0	0	1	1	1	
RAR	$A_{CC_{n-1}} \leftarrow A_{CC_n}$ $C \leftarrow A_{CC_0}$ $(n = 1 \rightarrow 3)$ $A_{CC_3} \leftarrow C$	Rotate A_{CC} right through Carry F/F	0	0	1	1	0	0	0	0	1	1	
CARRY FLAG													
CLC	$C \leftarrow 0$	Reset Carry F/F to zero	0	0	0	0	1	0	1	1	1	1	
STC	$C \leftarrow 1$	Set Carry F/F to one	0	0	0	1	1	0	1	1	1	1	
TC	Skip if C = 1	Skip if Carry F/F is true	0	0	0	0	0	1	0	0	1	1 + S	C = 1
FLAG													
SFB	$FLAG_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of FLAG Register to one	0	1	1	1	1	1	D_1	D_0	1	2	
RFB	$FLAG_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of FLAG Register to zero	0	1	1	0	1	1	D_1	D_0	1	2	
FBT	Skip if $FLAG_{bit} = 1$	Skip if a single bit (denoted by D_1D_0) of the FLAG Register is true	0	1	0	1	1	1	D_1	D_0	1	2 + S	$FLAG_{bit} = 1$
FBF	Skip if $FLAG_{bit} = 0$	Skip if a single bit (denoted by D_1D_0) of the FLAG Register is false	0	0	1	0	0	0	D_1	D_0	1	2 + S	$FLAG_{bit} = 0$
INCREMENT AND DECREMENT													
INC	$A_{CC} \leftarrow A_{CC} + 1$ Skip if overflow	Increment A; Skip if overflow is generated	0	0	0	0	1	1	0	1	1	1 + S	Overflow
DEC	$A_{CC} \leftarrow A_{CC} - 1$ Skip if underflow	Decrement A, Skip if underflow occurs	0	0	0	0	1	1	1	1	1	1 + S	Underflow
IND	$DP_L \leftarrow DP_L + 1$ Skip if $DP_L = 0H$	Increment DP_L, Skip if $DP_L = 0H$	0	0	1	1	0	0	1	1	1	1 + S	$DP_L = 0H$
DED	$DP_L \leftarrow DP_L - 1$ Skip if $DP_L = FH$	Decrement DP_L, Skip if $DP_L = FH$	0	0	0	1	0	0	1	1	1	1 + S	$DP_L = FH$
INM	$(DP) \leftarrow (DP) + 1$ Skip if (DP) = 0H	Increment the RAM contents addressed by DP; Skip if the contents = 0H	0	0	0	1	1	1	0	1	1	1 + S	(DP) = 0H
DEM	$(DP) \leftarrow (DP) - 1$ Skip if (DP) = FH	Decrement the RAM contents addressed by DP; skip if the contents = FH	0	0	0	1	1	1	1	1	1	1 + S	(DP) = FH

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
BIT MANIPULATION													
RMB data	$(DP)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1-D_0) of RAM at the location addressed by DP to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB data	$(DP)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of RAM at the location addressed by DP to one	0	1	1	1	1	0	D_1	D_0	1	1	
REB data	$PE_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of output Port E to zero	0	1	1	0	0	1	D_1	D_0	1	2	
SEB data	$PE_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of output Port E to one	0	1	1	1	0	1	D_1	D_0	1	2	
RPB data	$P(DP_L)_{bit} \leftarrow 0$	Reset a single bit (denoted by D_1D_0) of the output port addressed by DP_L to zero	0	1	1	0	0	0	D_1	D_0	1	1	
SPB data	$P(DP_L)_{bit} \leftarrow 1$	Set a single bit (denoted by D_1D_0) of the output port addressed by DP_L	0	1	1	1	0	0	D_1	D_0	1	1	
JUMP, CALL AND RETURN													
JMP address	$P_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Jump to the address specified by 11 bits of immediate data	1 D_7	0 D_6	1 D_5	0 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	2	2	
JCP address	$P_{5\text{-}0} \leftarrow D_{5\text{-}0}$	Jump to the address within the current ROM page specified by 6 bits of immediate data	1	1	D_5	D_4	D_3	D_2	D_1	D_0	1	1	
JPA	$P_{5\text{-}2} \leftarrow A_{CC}$ $P_{1\text{-}0} \leftarrow 00$	Jump to the address within the current ROM page modified by A_{CC}	0	1	0	0	0	0	0	1	1	2	
CAL address	Stack $\leftarrow$ P + 2 $P_{10\text{-}0} \leftarrow D_{10\text{-}0}$	Store a return address (P + 2) in the stack, call the subroutine program at the location specified by 11 bits of immediate data	1 D_7	0 D_6	1 D_5	0 D_4	1 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	2	2	
CZP address	Stack $\leftarrow$ P + 1 $P_{10\text{-}6} \leftarrow 00000$ $P_{5\text{-}2} \leftarrow D_{3\text{-}0}$ $P_{1\text{-}0} \leftarrow 00$	Store a return address (P + 1) in the stack, call the subroutine program at one of sixteen locations in Page 0 of Field 0, specified by 4 bits of immediate data	1	0	1	1	D_3	D_2	D_1	D_0	1	1	
RT	P $\leftarrow$ Stack	Return from Subroutine	0	1	0	0	1	0	0	0	1	2	
RTS	P $\leftarrow$ Stack Skip unconditionally	Return from Subroutine, skip unconditionally	0	1	0	0	1	0	0	1	1	2 + S	Unconditional
SKIP													
CI data	Skip if $A_{CC} = D_{3\text{-}0}$	Skip if A_{CC} equals 4 bits of immediate data	0 1	0 1	0 0	1 0	0 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	$A_{CC} = D_{3\text{-}0}$
CM	Skip if A_{CC} = (DP)	Skip if A_{CC} equals the RAM contents addressed by DP	0	0	0	0	1	1	0	0	1	1 + S	A_{CC} = (DP)
CMB data	Skip if $A_{CC_{bit}} = (DP)_{bit}$	Skip if the single bit (denoted by D_1D_0) of A_{CC}, is equal to the single bit (also denoted by D_1D_0) of RAM addressed by DP	0	0	1	1	0	1	D_1	D_0	1	1 + S	$A_{CC_{bit}} = (DP)_{bit}$
TAB data	Skip if $A_{CC_{bit}} = 1$	Skip if the single bit (denoted by D_1D_0) of A_{CC} is true	0	0	1	0	0	1	D_1	D_0	1	1 + S	$A_{CC_{bit}} = 1$
CLI data	Skip if $DP_L = D_{3\text{-}0}$	Skip if DP_L equals 4 bits of immediate data	0 1	0 1	0 1	1 0	0 D_3	1 D_2	1 D_1	0 D_0	2	2 + S	$DP_L = D_{3\text{-}0}$
TMB data	Skip if $(DP)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by DP is true	0	1	0	1	1	0	D_1	D_0	1	1 + S	$(DP)_{bit} = 1$
TPA data	Skip if $PA_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of Port A is true	0	1	0	1	0	1	D_1	D_0	1	2 + S	$PA_{bit} = 1$
TPB data	Skip if $P(DP_L)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the input Port addressed by DP_L is true	0	1	0	1	0	0	D_1	D_0	1	1 + S	$P(DP_L)_{bit} = 1$
STM	TIMER F/F $\leftarrow$ 0 TC $\leftarrow D_{5\text{-}0}$	Reset Timer F/F to zero; Load Timer Counter with 6 bits of immediate data; Start timer	0 1	0 0	0 D_5	1 D_4	0 D_3	1 D_2	0 D_1	0 D_0	2	2	
TTM	Skip if TIMER F/F = 1	Skip if Timer F/F is true	0	0	0	0	0	1	0	1	1	1 + S	TIMER F/F = 1

INSTRUCTION SET
(CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE								BYTES	CYCLES	SKIP CONDITION
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			
INTERRUPT													
TIT	Skip if INT F/F = 1	Skip if Interrupt F/F is true, Reset Interrupt F/F	0	0	0	0	0	0	1	1	1	1 + S	INT F/F = 1
EI	INTE F/F ← 1	Set Interrupt Enable F/F to one; Enable Interrupt	0	0	1	1	0	0	0	1	1	1	
DI	INTE F/F ← 0	Reset Interrupt Enable F/F to zero; Disable Interrupt	0	0	0	0	0	0	0	1	1	1	
PARALLEL I/O													
IA	$A_{CC} \leftarrow PA$	Input Port A to A_{CC}	0	1	0	0	0	0	0	0	1	2	
IP	$A_{CC} \leftarrow P(DP_L)$	Input the Port addressed by DP_L to A_{CC}	0	0	1	1	0	0	1	0	1	1	
OE	$PE \leftarrow A_{CC}$	Output A_{CC} to Port E	0	1	0	0	0	1	0	0	1	2	
OP	$P(DP_L) \leftarrow A_{CC}$	Output A_{CC} to the port addressed by DP_L	0	0	0	0	1	1	1	0	1	1	
OCD	$PD_{3-0} \leftarrow D_{7-4}$ $PC_{3-0} \leftarrow D_{3-0}$	Output 8 bits of immediate data to Ports C and D	0 D_7	0 D_6	0 D_5	1 D_4	1 D_3	1 D_2	1 D_1	0 D_0	2	2	
CPU CONTROL													
NOP		Perform no operation, consume one machine cycle	0	0	0	0	0	0	0	0	1	1	

3

Package Outlines

For information, see Package Outline Section 7.

Plastic, μCOM-4C
Plastic Miniflat, μCOM-4G

4-BIT SINGLE CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

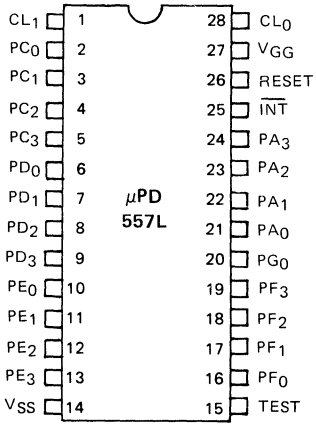
DESCRIPTION

The μPD557L is a 4-bit single chip microcomputer which has the same architecture as the μPD553, but is pin-compatible with the μPD550L and the μPD554L. The μPD557L contains a 2000 x 8-bit ROM and a 96 x 4-bit RAM, which includes six working registers and the FLAG register. It has a lever-triggered hardware interrupt input $\overline{INT}$, a three-level stack and a 6-bit programmable timer. The μPD557L provides 21 I/O lines, organized into the 4-bit input port A, the 4-bit I/O ports C and D, and the 4-bit output ports E and F, and the 1-bit output port G. The 17 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. The μPD557L typically executes all 80 instructions of the extended μCOM-4 family instruction set with a 25 μs instruction cycle time. It is manufactured with a modified PMOS process, allowing use of a single −8V power supply and is available in a 28-pin dual-in-line plastic package.

The μPD550L and the μPD554L are upward-compatible with the μPD557L.

3

PIN CONFIGURATION



PIN NAMES

PA_0–PA_3	Input Port A
PC_0–PC_3	Input/Output Port C
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
PG_0	Output Port G
$\overline{INT}$	Interrupt Input
CL_0–CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature		−10°C to +70°C
Storage Temperature		−40°C to +125°C
Supply Voltage, V_{GG}		−15 to +0.3V
Input Voltages	(Port A, $\overline{INT}$, RESET)	−15 to +0.3V
	(Ports C, D)	−40 to +0.3V
Output Voltages		−40 to +0.3V
Output Current	(Ports C, D, each bit)	−4 mA
	(Ports E, F, G, each bit)	−25 mA
	(Total, all ports)	−100 mA

$T_a = 25°C$

*COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.5	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−6.5		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−6.5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET $V_I = -9V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -9V$
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through G, $I_{OH} = -2$ mA
	V_{OH_2}			−4.0	V	Ports E, F, G, $I_{OH} = -20$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, $V_O = -9V$
	I_{LOL_2}			−30	μA	Ports C through G, $V_O = -35V$
Supply Current	I_{GG}		−20	−36	mA	

CAPACITANCE

$T_a = 25°C$

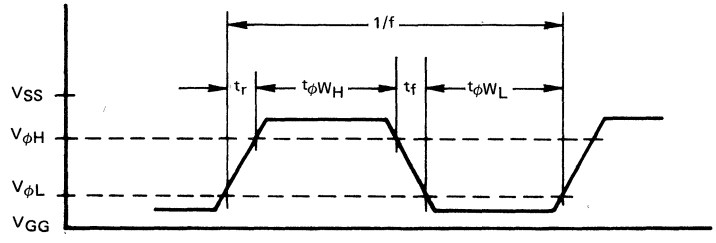
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -8.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	kHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD557LC
Plastic Shrinkdip, μPD557LCT

4-BIT SINGLE CHIP MICROCOMPUTERS WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

DESCRIPTION

The μPD552 and the μPD553 are pin-compatible 4-bit single chip microcomputers which have similar architectures.

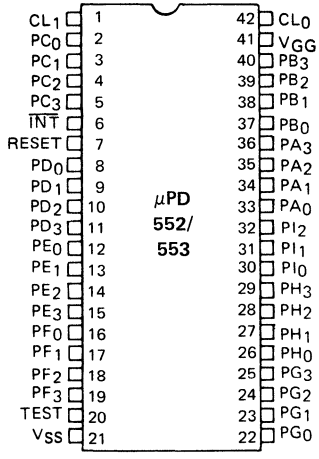
The μPD552 contains a 1000 x 8-bit ROM and a 64 x 4-bit RAM. It has a testable interrupt input $\overline{INT}$, a single-level stack, and executes all 58 instructions of the μCOM-4 family instruction set. The μPD552 is upward compatible with the μPD553.

The μPD553 contains a 2000 x 8-bit ROM, and a 96 x 4-bit RAM which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit Timer. The μPD553 executes all 80 instructions of the extended μCOM-4 family instruction set.

Both the μPD552 and the μPD553 provide 35 I/O lines organized into the 4-bit input Ports A and B, the 4-bit I/O Ports C and D, the 4-bit output Ports E, F, G, and H, and the 3-bit output Port I. The 27 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. Both devices typically execute their instructions with a 10 μs instruction cycle time. The μPD552 and the μPD553 are manufactured with a standard PMOS process, allowing use of a single −10V power supply, and are available in a 42-pin dual-in-line plastic package.

3

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Supply Voltage, V_{GG} . . . . . −15 to +0.3V
Input Voltages (Port A, B, $\overline{INT}$, RESET) . . . . . −15 to +0.3V
(Ports C, D) . . . . . −40 to +0.3V
Output Voltages . . . . . −40 to +0.3V
Output Current (Ports C through I, each bit) . . . . . −12 mA
(Total, all ports) . . . . . −60 mA

$T_a = 25°C$

*COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−3 5	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−7 5		V_{GG}	V	Ports A, B, $\overline{INT}$, RESET
	V_{IL_2}	−7 5		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0 8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6 0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -1V$
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A through D, $\overline{INT}$, RESET, $V_I = -11V$
	I_{LIL_2}			−30	μA	Ports C, D, $V_I = -35V$
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H} = 0V$
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L} = -11V$
Output Voltage High	V_{OH}			-2 0	V	Ports C through I, $I_{OH} = -8$ mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through I, $V_O = -11V$
	I_{LOL_2}			−30	μA	Ports C through I, $V_O = -35V$
Supply Current	I_{GG}		−30	−50	mA	

CAPACITANCE

$T_a = 25°C$

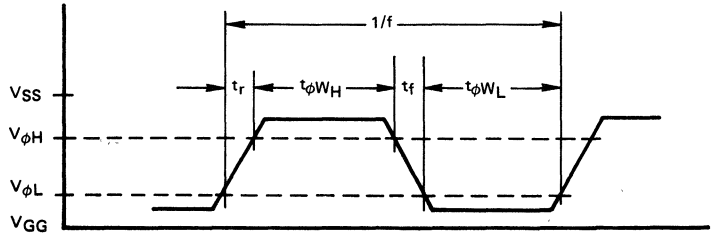
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0 3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0 5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5 6	μs	

CLOCK WAVEFORM



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD552C/553C

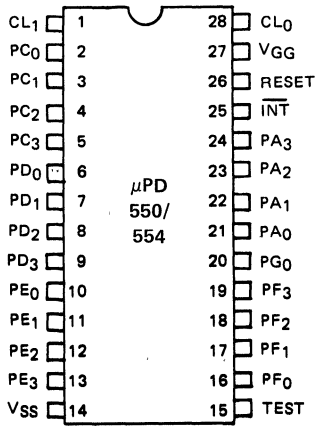
4-BIT SINGLE CHIP MICROCOMPUTERS WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

DESCRIPTION

The μPD550 and the μPD554 are pin-compatible 4-bit single chip microcomputers which have the same architecture. The only difference between them is that the μPD550 contains a 640 x 8-bit ROM, whereas the μPD554 contains a 1000 x 8-bit ROM. Both devices have a 32 x 4-bit RAM, a testable interrupt input $\overline{INT}$, and a single-level stack. The μPD550 and the μPD554 provide 21 I/O lines organized into the 4-bit input port A, the 4-bit I/O ports C and D, the 4-bit output ports E and F, and the 1-bit output port G. The 17 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. The μPD550 and the μPD554 typically execute all 58 instructions of the μCOM-4 family instruction set with a 10 μs instruction cycle time. Both devices are manufactured with a standard PMOS process, allowing use of a single −10V power supply, and are available in a 28 pin dual-in-line plastic package.

3

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
CL_0-CL_1	External Clock Signals
$\overline{INT}$	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Supply Voltage, V_{GG} . . . . . −15 to +0.3V
Input Voltages (Port A, $\overline{INT}$, RESET) . . . . . −15 to +0.3V
(Ports C, D) . . . . . −40 to +0.3V
Output Voltages . . . . . −40 to +0.3V
Output Current (Ports C, D, each bit) . . . . . −4 mA
(Ports E, F, G, each bit) . . . . . −15 mA
(Total, all ports) . . . . . −60 mA

$T_a = 25°C$

*COMMENT. Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.3		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.3		−35	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −1V
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −11V
	I_{LIL_2}			−30	μA	Ports C, D, V_I = −35V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −11V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, I_{OH} = −2 mA
	V_{OH_2}			−2.5	V	Ports E, F, G, I_{OH} = −10 mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, V_O = −11V
	I_{LOL_2}			−30	μA	Ports C through G, V_O = −35V
Supply Current	I_{GG}		−20	−40	mA	

CAPACITANCE

T_a = 25°C

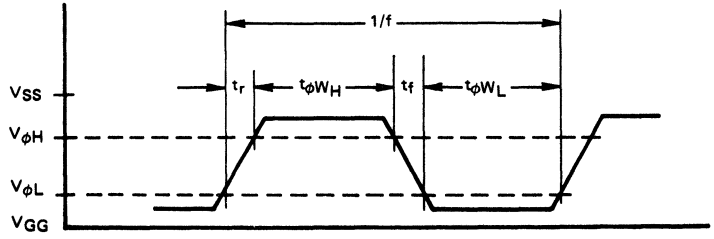
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{GG} = −10V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CLOCK WAVEFORM



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD550C/554C
Plastic Shrinkdip, μPD550CT
Plastic Shrinkdip, μPD554CT

4-BIT SINGLE CHIP MICROCOMPUTERS WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

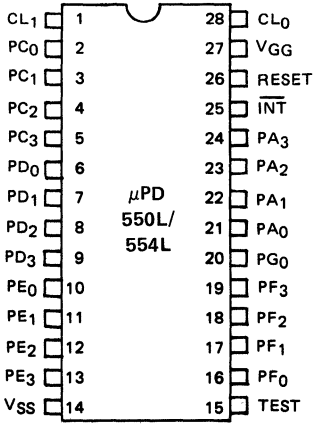
DESCRIPTION

The μPD550L and the μPD554L are pin-compatible 4-bit single chip microcomputers which have the same architecture. The only difference between them is that the μPD550L contains a 640 x 8-bit ROM, whereas the μPD554L contains a 1000 x 8-bit ROM. Both devices have a 32 x 4-bit RAM, a testable interrupt input $\overline{INT}$, and a single-level stack. The μPD550L and the μPD554L provide 21 I/O lines organized into the 4-bit input port A, the 4-bit I/O ports C and D, the 4-bit output ports E and F, and the 1-bit output port G. The 17 I/O ports and output ports are capable of being pulled to −35V in order to drive Vacuum Fluorescent Displays directly. The μPD550L and the μPD554L typically execute all 58 instructions of the μCOM-4 family instruction set with a 25 μs instruction cycle time. Both devices are manufactured with a modified PMOS process, allowing use of a single −8V power supply, and are available in a 28-pin dual-in-line plastic package.

The μPD550L and the μPD554L are upward compatible with the μPD557L.

3

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0	Output Port G
CL_0-CL_1	External Clock Signals
$\overline{INT}$	Interrupt Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage, V_{GG}	−15 to +0.3V
Input Voltages (Port A, $\overline{INT}$, RESET)	−15 to +0.3V
(Ports C, D)	−40 to +0.3V
Output Voltages	−40 to +0.3V
Output Current (Ports C, D, each bit)	−4 mA
(Ports E, F, G, each bit)	−15 mA
(Total, all ports)	−60 mA

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −8.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−1.6	V	Ports A, C, D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL_1}	−4.5		V_{GG}	V	Ports A, $\overline{INT}$, RESET
	V_{IL_2}	−4.5		−3.5	V	Ports C, D
Clock Voltage High	$V_{\phi H}$	0		−0.6	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −1V
Input Leakage Current Low	I_{LIL_1}			−10	μA	Ports A, C, D, $\overline{INT}$, RESET V_I = −9V
	I_{LIL_2}			−30	μA	Ports C, D, V_I = −35V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −9V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C, D, I_{OH} = −2 mA
	V_{OH_2}			−2.5	V	Ports E, F, G, I_{OH} = −10 mA
Output Leakage Current Low	I_{LOL_1}			−10	μA	Ports C through G, V_O = −9V
	I_{LOL_2}			−30	μA	Ports C through G, V_O = −35V
Supply Current	I_{GG}		−12	−24	mA	

CAPACITANCE

T_a = 25°C

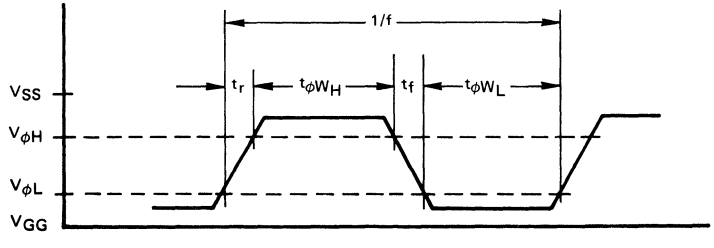
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	
Input/Output Capacitance	C_{IO}			15	pF	

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −8.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	100		180	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	External Clock
Clock Pulse Width High	$t_{\phi W_H}$	2.0		8.0	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	2.0		8.0	μs	

CLOCK WAVEFORM



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD550LC/554LC

μCOM-4 4-BIT SINGLE CHIP ROM-LESS EVALUATION CHIP

DESCRIPTION

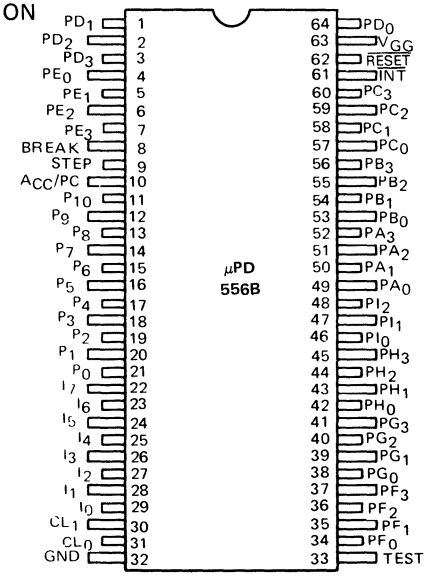
The μPD556B is the ROM-less evaluation chip for the μCOM-4 4-bit single chip microcomputer family. The μPD556B is used in conjunction with an external 2048 x 8-bit program memory, such as the μPD2716 UV EPROM, to emulate each of the 14 different μCOM-4 single chip microcomputers.

The μPD556B contains a 96 x 4-bit RAM, which includes six working registers and the Flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit timer. The μPD556B executes all 80 instructions of the extended μCOM-4 family instruction set.

The μPD556B provides 35 I/O lines organized into the 4-bit input Ports A and B, the 4-bit I/O Ports C and D, the 4-bit output Ports E, F, G, and H, and the 3-bit output Port I. It typically executes its instructions with a 10μs instruction cycle time. The μPD556B is manufactured with a standard PMOS process, allowing use of a single -10V power supply, and is available in a 64-pin quad-in-line ceramic package.

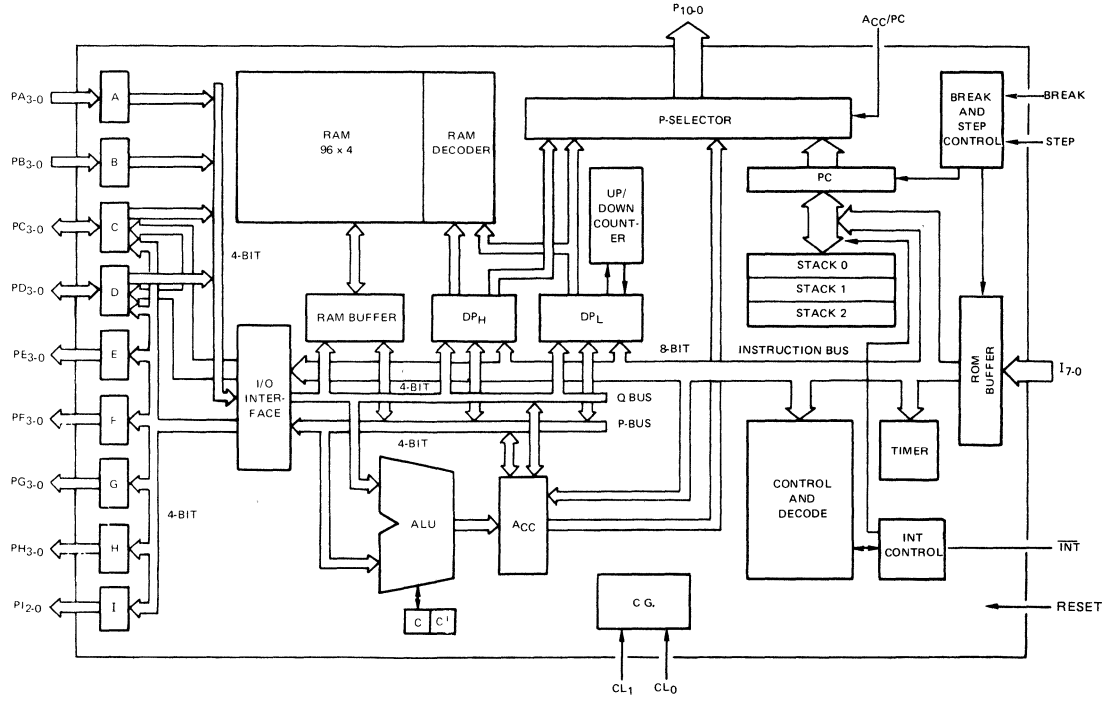
3

PIN CONFIGURATION



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
I_{0-7}	Instruction Input
PC_{0-10}	Program Counter Output
A_{CC}/PC	Accumulator/Program Counter Select
BREAK	Break Input
STEP	Single Step Input
CL_0-CL_1	External Clock Source
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage, V_{GG}	−15V to +0.3V
All Input Voltages	−15V to +0.3V
All Output Voltages	−15V to +0.3V
Output Current (total, all ports)	−4 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		−2.0	V	Ports A to D, I_{7-0} BREAK, STEP, $\overline{INT}$, RESET, and A_{CC}/PC
Input Low Voltage	V_{IL}	−4.3		V_{GG}	V	Ports A to D, I_{7-0} BREAK, STEP, $\overline{INT}$, RESET, and A_{CC}/PC
Clock High Voltage	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Low Voltage	$V_{\phi L}$	−6 0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			±10	μA	Ports A and B, I_{7-0} $\overline{INT}$, RESET, BREAK, STEP, A_{CC}/PC, V_I = −1V
				±10	μA	Ports C and D, V_I = −1V
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A and B, I_{7-0} $\overline{INT}$, RESET, BREAK, STEP, A_{CC}/PC, V_I = −11V
				−10	μA	Ports C and D, V_I = −11V
Clock Input Leakage High	$I_{L\phi H}$			±200	μA	CL_0 Input, External Clock, $V_{\phi H}$ = 0V
Clock Input Leakage Low	$I_{L\phi L}$			−200	μA	CL_0 Input, External Clock, $V_{\phi L}$ = −11V
Output High Voltage	V_{OH1}			−1 0	V	Ports C to I, P_{10-0} I_{OH} = −1.0 mA
	V_{OH2}			−2.3	V	Ports C to I, P_{10-0} I_{OH} = −3.3 mA
Output Leakage Current Low	I_{LOL}			−30	μA	Ports C to I, P_{10-0} V_O = −11V
Supply Current	I_{GG}		−30	−50	mA	

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%

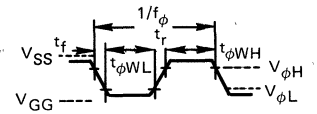
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Frequency	f_ϕ	150		440	KHz	
Clock Rise and Fall Times	t_r, t_f	0		0 3	μs	
Clock Pulse Width High	$t_{\phi WH}$	0 5		5 6	μs	
Clock Pulse Width Low	$t_{\phi WL}$	0 5		5 6	μs	
Input Setup Time	t_{IS}			5	μs	
Input Hold Time	t_{IH}	0			μs	
BREAK to STEP Interval	t_{BS}	200			μs	f = 400 KHz, "1" Written
STEP to RUN Interval	t_{SB}	200			μs	f = 400 KHz, "1" Written
STEP Pulse Width	t_{WS}	30			μs	f = 400 KHz, "1" Written
BREAK to A_{CC} Interval	t_{BA}	200			μs	f = 400 KHz, "1" Written
A_{CC}/PC Pulse Width	t_{WA}	30			μs	f = 400 KHz, "1" Written
STEP to A_{CC} Interval	t_{SA1}	200			μs	f = 400 KHz, "1" Written
PC to STEP Overlap	t_{SA2}			5	μs	f = 400 KHz, "1" Written
PC to RUN Interval	t_{AB}	0			μs	f = 400 KHz, "1" Written
A_{CC}/PC → P_{10-0} Delay	t_{DAP1}			15	μs	f = 400 KHz, "1" Written
	t_{DAP2}			15	μs	f = 400 KHz, "1" Written

CAPACITANCE

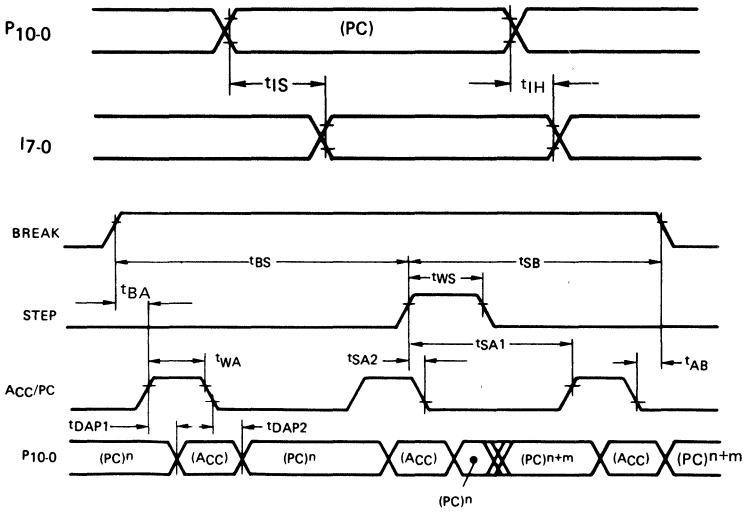
T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

CLOCK WAVEFORM



TIMING WAVEFORMS



Package Outlines

For information, see Package Outline Section 7.

Ceramic Quil, μPD556B

Description

The μPD7500 Series CMOS 4-Bit Single Chip Microcomputer Family is a broad product line of 16 individual devices designed to fulfill a wide variety of applications. The advanced 4th generation architecture includes all of the functional blocks necessary for a single chip controller, including an ALU, Accumulator, Program Memory (ROM), Data Memory (RAM), four General Purpose Registers, Stack Pointer, Program Status Word (PSW), 8-Bit Timer/Event Counter, Interrupt Controller, Display Controller/Driver, and 8-Bit Serial Interface. The instruction set maximizes the efficient utilization of fixed Program Memory space, and includes a variety of addressing, Table-Look-up, Logical, Single Bit Manipulation, vectored jump, and Condition Skip Instructions.

The μPD7500 Series includes four different devices, the μPD7501, μPD7502, μPD7503, and μPD7514, capable of directly driving Liquid Crystal Displays with up to 16 7-segment digits. The μPD7508A, μPD7528, μPD7517, μPD7538, μPD7537, and μPD7519 can directly drive up to 35V Vacuum Fluorescent Displays with up to 8 7-segment digits, and the μPD7519 can directly drive up to 35V Vacuum Fluorescent Displays with up to 16 7-segment digits.

All 16 devices are manufactured with a Silicon gate CMOS process, consuming only 900μA max at 5V, and only 400μA max at 3V. The HALT and STOP power-down instructions can significantly reduce power consumption even further.

The flexibility and the wide variety of μPD7500 Series devices available make the μPD7500 series ideally suited for a wide range of battery-powered, solar-powered, and portable products, such as telecommunication devices, hand-held instruments and meters, automotive products, industrial controls, energy management systems, medical instruments, portable terminals, portable measuring devices, appliances, and consumer products.

Features

- ☐ Advanced 4th Generation Architecture
- ☐ Choice of 8-Bit Program Memory (ROM) size:
  - 1K, 2K, 4K internal, or 8K external bytes
- ☐ Choice of 4-Bit Data Memory (RAM) size:
  - 64, 96, 128, 208, 224, or 256 internal nibbles
- ☐ RAM Stack
- ☐ Four General Purpose Registers: D, E, H, and L
  - Can address Data Memory and I/O ports
  - Can be stored to or retrieved from Stack
- ☐ Powerful Instruction Set
  - From 58 to 110 instructions, including:
    - Direct/indirect addressing
    - Table Look-up
    - RAM Stack Push/Pop
    - Single byte subroutine calls
    - RAM and I/O port single bit manipulation
    - Accumulator and I/O port Logical operations
    - 10 μs Instruction Cycle Time, typically
- ☐ Extensive General Purpose I/O Capability
  - One 4-Bit Input Port
  - Two 4-Bit latched tri-state Output Ports
  - Five 4-Bit input/latched tri-state Output Ports
  - Easily expandable with μPD82C43 CMOS I/O Expander
  - 8-Bit Parallel I/O capability
- ☐ Hardware Logic Blocks — Reduce Software Requirements
  - Operation completely transparent to instruction execution
  - 8-Bit Timer/Event Counter
    - Binary-up counter generates INT_T at coincidence
    - Accurate Crystal Clock or External Event operation possible
  - Vectored, Prioritized Interrupt Controller
    - Three external interrupts (INT_0, INT_1, INT_2)
    - Two internal interrupts (INT_T, INT_S)
  - Display Controller/Driver
    - Complete Direct Drive and Control of Multiplexed LCD or Vacuum Fluorescent Display
    - Display Data automatically multiplexed from RAM to dedicated segment/backplane/digit driver lines
  - 8-Bit Serial Interface
    - 3-line I/O configuration generates INT_S upon transmission of eighth bit
    - Ideal for distributed intelligence systems or communication with peripheral devices
  - Complete operation possible in HALT and STOP power-down modes
- ☐ Built-in System Clock Generator
- ☐ Built-in Schmidt-Trigger RESET Circuitry
- ☐ Single Power Supply, Variable from 2.7V to 5.5V
- ☐ Low Power Consumption Silicon Gate CMOS Technology
  - 900 μA max at 5V, 400 μA max at 3V
  - HALT, STOP Power-down instructions reduce power consumption to 20 μA max at 5V, 10μA at 3V (Stop mode)
- ☐ Extended −40°C to +85°C Temperature Range Available
- ☐ Choice of 28-pin, 40-pin, 42-pin dual-in-line packages, or 52-pin, 64-pin, or 80-pin flat plastic packages.

Features	7500	7501	7502	7503	7514	7506	7507	7507S	7508	7508A	7519	7527	7528	7537	7538
Internal ROM (8-bit words)		1K	2K	4K	4K	1K	2K	2K	4K	4K	4K	2K	4K	2K	4K
Expandable to	8K														
RAM	256 x 4	96 x 4	128 x 4	224 x 4	256 x 4	64 x 4	128 x 4	128 x 4	224 x 4	208 x 4	256 x 4	160 x 4	160 x 4	160 x 4	160 x 4
I/O Lines	32	24	23	23	67	22	32	20	32	32	28	35	35	35	35
8-Bit Timer/Event Counter	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
8-Bit Serial Interface	•	•	•	•	•		•	•	•	•	•	•	•	•	•
Registers Outside RAM	4 x 4	2 x 4	4 x 4	4 x 4		2 x 4	4 x 4	4 x 4	4 x 4	4 x 4	4 x 4	2 x 4	2 x 4	2 x 4	2 x 4
Instructions	110	63	92	92	92	58	92	91	92	92	92	66	66	67	67
Min Cycle Time (μs)	6.67	6.67	6.67	6.67	5	6.67	6.67	6.67	6.67	6.67	6.67	4	4	4	4
Interrupts	5	4	4	4	4	2	4	4	4	4	4	3	3	3	3
Stack Levels	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM	RAM
Display Controller/ Driver		LCD	LCD	LCD	LCD					VFD drive only	VFD	VFD DRIVE ONLY	VFD DRIVE ONLY	VFD DRIVE ONLY	VFD DRIVE ONLY
Analog I/O										14-bit D/A					
Current Consumption (max)															
Normal Operation			←			900 μA at 5V ± 10%; 400μA at 3V ± 10%									→
Stop Mode			←			20 μA at 5V ± 10%; 10μA at 3V ± 10%									→
Operating Temperature Range	−10°C to +70°C	←				−40°C to +85°C					→				
Packages															
28-pin DIP						•			•						
40-pin DIP							•		•	•					
52-pin Flat						•	•		•						
64-pin Flat		•	•	•											
64-pin QUIL	•										•				
42-pin DIP												•	•	•	•
80-pin Flat					•										

Instruction Set

The μPD7500 Series Instruction Set consists of 110 powerful instructions designed to take full advantage of the advanced μPD7500 architecture in your application. It is divided into two subsets, according to the complexity of the device.

Instruction Set "A" is available for the higher-performance μPD7500 Series devices having either a 2K × 8-bit or a 4K × 8-bit Program Memory. It can be used with the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, μPD7519, μPD7514, μPD7527, μPD7528, μPD7537, and μPD7538 products.

Instruction Set "B" is available for the lower-cost μPD7500 Series devices having a 1K × 8-bit Program Memory. Its instructions are a compatible subset of Instruction Set "A," and can be used with the μPD7500, μPD7501, and μPD7506 products.

Instruction Set Symbol Definitions

The following abbreviations are used in the description of the μPD7500 Series Instruction sets:

Symbol	Explanation and Use
A	Accumulator
A_n	Bit "n" of Accumulator
addr	Address
bit	Operand specifying one bit of a nibble
B_n	Bit "n" of two-bit operand B_1 B_0 Bit Specified 0 0 Bit 0 (LSB) 0 1 Bit 1 1 0 Bit 2 1 1 Bit 3 (MSB)
Bank	Bank Flag of PSW (μPD7500 only)
borrow	Resulting value is less than 0H
C	Carry Flag
data	Immediate data operand
D	D Register
D_n	Bit "n" of immediate data operand
DE	DE Register Pair
DL	DL Register Pair
E	E Register
H	H Register
HL	HL Register Pair
IER	Interrupt Enable Register IER bit: 0 1 2 3 Interrupt: INT_T $INT_{0/S}$ INT_1 INT_2
IME	Interrupt Master Enable F/F
INT_n	Interrupt "n"
IRF_n	Interrupt Request Flag "n"
L	L Register
overflow	Resulting value is greater than FH
P( )	Parallel Input/Output Port addressed by the value within the parentheses
PC	Program Counter
PC_n	Bit "n" of Program Counter
PSW	Program Status Word PSW bit: 0 1 2 3 Flag: Carry Bank SK_0 SK_1
rp	Register Pair, specified by the 3-bit immediate data operand D_{2-0}, as follows: D_2 D_1 D_0 rp Additional Action 0 0 0 DL none (instruction set "A" only) 0 0 1 DE none (instruction set "A" only) 1 0 0 HL– decrement L; skip if L = FH 1 0 1 HL+ increment L; skip if L = 0H 1 1 0 HL none
S	Skip Cycles: 0 when skip condition does not occur 1 when skip condition does occur
SIO	Serial I/O Shift Register
SIOCR	Serial I/O Count Register
SP	Stack Pointer
String	String Effect; in a string of similar instructions, only the first encountered is executed; the remainder of the instructions in the string are executed as NOP instructions
taddr	Operand specifying ROM Table Data
T_n	Bit "n" of ROM Table Data
TCR	Timer Counter Register
TMR	Timer Modulo Register
( )	The contents of the RAM location addressed by the value within the parentheses
[ ]	The contents of the ROM location addressed by the value within the brackets
←	Load, Store, or Transfer right operand into left operand
↔	Exchange the left and right operands
NOT	Logical NOT (One's complement)
AND	LOGICAL AND
OR	LOGICAL OR
XOR	LOGICAL Exclusive OR
.....	Instruction pertains to μPD7500 only

Instruction Set "A"

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
		Load												
LADR addr	A←(D_{7-0})	Load Accumulator from directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	38 00-FF	2	2	
LAI data	A←D_{3-0}	Load Accumulator with immediate data	0	0	0	1	D_3	D_2	D_1	D_0	10-1F	1	1	String
LAM rp	A←(rp) rp = DL, DE, HL−, HL+, HL if rp = HL−, skip if borrow if rp = HL+, skip if overflow	Load Accumulator from Memory, possible skip	0	1	0	D_2	0	0	D_1	D_0	40, 41 50-52	1	1+S	See explanation of "rp" in symbol definitions
LAMT (μPD7500, μPD7502 only)	ROM addr = PC_{10-6}, 0, C, A_{3-0} A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table	0	1	0	1	1	1	1	0	5E	1	2	
LAMTL (μPD7500, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, μPD7519, only)	ROM addr = PC_{11-8}, A_{3-0}, $(HL)_{3-0}$ A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table Long	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 0	3F 34	2	2	
LDEI data	D←D_{7-4} E←D_{3-0}	Load DE register pair with immediate data	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	1 D_1	1 D_0	4F 00-FF	2	2	
LDI data	D←D_{3-0}	Load D register with immediate data	0 0	0 0	1 1	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 20-2F	2	2	
LEI data	E←D_{3-0}	Load E register with immediate data	0 0	0 0	1 0	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 00-0F	2	2	
LHI data	H←D_{3-0}	Load H register with immediate data	0 0	0 0	1 1	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 30-3F	2	2	
LHLI data	H←D_{7-4} L←D_{3-0}	Load HL register pair with immediate data	0 D_7	1 D_6	0 D_5	0 D_4	1 D_3	1 D_2	1 D_1	0 D_0	4E 00-FF	2	2	String
LHLT taddr	ROM addr = 0C0H + D_{3-0} H←[ROM addr]$_{7-4}$ L←[ROM addr]$_{3-0}$	Load HL register pair from ROM Table	1	1	0	0	D_3	D_2	D_1	D_0	C0-CF	1	2	String
LLI data	L←D_{3-0}	Load L register with immediate data	0 0	0 0	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 10-1F	2	2	
		Store												
ST	(HL)←A	Store A to Memory	0	1	0	1	0	1	1	1	57	1	1	
		Transfer												
TAD	D←A	Transfer A to D	0 1	0 0	1 1	1 0	1 1	1 0	1 1	0 0	3E AA	2	2	
TAE	E←A	Transfer A to E	0 1	0 0	1 0	1 0	1 1	1 0	1 1	0 0	3E 8A	2	2	
TAH	H←A	Transfer A to H	0 1	0 0	1 1	1 1	1 1	1 0	1 1	0 0	3E BA	2	2	
TAL	L←A	Transfer A to L	0 1	0 0	1 0	1 1	1 1	1 0	1 1	0 0	3E 9A	2	2	
TDA	A←D	Transfer D to A	0 1	0 0	1 1	1 0	1 1	1 0	1 1	0 1	3E AB	2	2	
TEA	A←E	Transfer E to A	0 1	0 0	1 0	1 0	1 1	1 0	1 1	0 1	3E 8B	2	2	
THA	A←H	Transfer H to A	0 1	0 0	1 1	1 1	1 1	1 0	1 1	0 1	3E BB	2	2	
TLA	A←L	Transfer L to A	0 1	0 0	1 0	1 1	1 1	1 0	1 1	0 1	3E 9B	2	2	
		Exchange												
XAD	A↔D	Exchange A with D	0	1	0	0	1	0	1	0	4A	1	1	
XADR addr	A↔(D_{7-0})	Exchange A with directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	39 00-FF	2	2	
XAE	A↔E	Exchange A with E	0	1	0	0	1	0	1	1	4B	1	1	
XAH	A↔H	Exchange A with H	0	1	1	1	1	0	1	0	7A	1	1	
XAL	A↔L	Exchange A with L	0	1	1	1	1	0	1	1	7B	1	1	
XAM rp	A↔(rp) rp = DL, DE, HL−, HL+, HL if rp = HL−, skip if borrow if rp = HL+, skip if overflow	Exchange A with Memory, Possible Skip	0	1	0	D_2	0	1	D_1	D_0	44, 45 54-56	1	1+S	See explanation or "rp" in symbol definitions
XHDR addr	H↔(D_{7-0})	Exchange H with directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	0 D_0	3A 00-FF	2	2	
XLDR addr	L↔(D_{7-0})	Exchange L with directly addressed RAM	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	1 D_0	3B 00-FF	2	2	

Instruction Set "A" (Cont.)

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code								Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0 HEX			
Arithmetic													
ACSC	A, C←A+(HL)+C skip if carry	Add with carry, skip if carry	0	1	1	1	1	1	0	0 7C	1	1+S	Carry = 1
ADSC	A←A + D skip if overflow	Add D to A, skip if overflow	0 1	0 0	1 1	1 0	1 1	1 0	1 0	0 3E 1 A9	2	2+S	Overflow
AESC	A←A + E skip if overflow	Add E to A, skip if overflow	0 1	0 0	1 0	1 0	1 1	1 0	1 0	0 3E 1 89	2	2+S	Overflow
AHSC	A←A + H skip if overflow	Add H to A, skip if overflow	0 1	0 0	1 1	1 1	1 1	1 0	1 0	0 3E 1 B9	2	2+S	Overflow
AISC data	A←A + D_{3-0} skip if overflow	Add immediate skip if overflow	0	0	0	0	D_3	D_2	D_1	D_0 00-0F	1	1+S	Overflow
ALSC	A←A + L skip if overflow	Add H to A, skip if overflow	0 1	0 0	1 0	1 1	1 1	1 0	1 0	0 3E 1 99	2	2+S	Overflow
ASC	A←A + (HL) skip if overflow	Add memory; skip if overflow	0	1	1	1	1	1	0	1 7C	1	1+S	Carry = 1
SDSB	A←A − D skip if borrow	Subtract D from A, skip if borrow	0 1	0 0	1 1	1 0	1 1	1 0	1 0	0 3E 0 A8	2	2+S	Borrow
SESB	A←A − E skip if borrow	Subtract E from A, skip if borrow	0 1	0 0	1 0	1 0	1 1	1 0	1 0	0 3E 0 88	2	2+S	Borrow
SHSB	A←A − H skip if borrow	Subtract H from A, skip if borrow	0 1	0 0	1 1	1 1	1 1	1 0	1 0	0 3E 0 B8	2	2+S	Borrow
SLSB	A←A − L skip if borrow	Subtract L from A, skip if borrow	0 1	0 0	1 0	1 1	1 1	1 0	1 0	0 3E 0 98	2	2+S	Borrow
Logical													
ANL	A←A AND (HL)	AND Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 3F 0 B2	2	2	
EXL	A←A XOR (HL)	Exclusive-Or Accumulator and Memory	0	1	1	1	1	1	1	0 7E	1	1	
ORL	A←A OR (HL)	OR Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 3F 0 B6	2	2	
Accumulator													
CMA	A←NOT A	Complement Accumulator	0	1	1	1	1	1	1	1 7F	1	1	
RAL	C←A_3 A_3←A_2 A_2←A_1 A_1←A_0 A_0←C (old)	Rotate Accumulator left through Carry	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 3F 1 B7	2	2	
RAR	C←A_0 A_0←A_1 A_1←A_2 A_2←A_3 A_3←C (old)	Rotate Accumulator right through Carry	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 3F 1 B3	2	2	
Program Status Word													
RC	C←0	Reset Carry	0	1	1	1	1	0	0	0 78	1	1	
SC	C←1	Set Carry	0	1	1	1	1	0	0	1 79	1	1	
Increment and Decrement													
DDE	DE←DE − 1	Decrement DE	0 1	0 0	1 0	1 0	1 1	1 1	1 0	0 3E 0 8C	2	2	
DDRS addr	(D_{7-0})←(D_{7-0}) − 1 skip if (D_{7-0}) = FH	Decrement directly addressed RAM; skip if borrow	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 3C D_0 00-FF	2	2+S	(D_{7-0}) = FH
DES	E←E − 1 skip if E = FH	Decrement E; skip if borrow	0	1	0	0	1	0	0	0 48	1	1+S	E = FH
DHL	HL←HL − 1	Decrement HL	0 1	0 0	1 0	1 1	1 1	1 1	1 0	0 3E 0 9C	2	2	
DLS	L←L − 1 skip if L = FH	Decrement L, skip if borrow	0	1	0	1	1	0	0	0 58	1	1+S	L = FH
IDE	DE←DE + 1	Increment DE	0 1	0 0	1 0	1 0	1 1	1 1	1 0	0 3E 1 8D	2	2	
IDRS addr	(D_{7-0})←(D_{7-0}) − 1 skip if (D_{7-0}) = 0H	Increment directly addressed; skip if overflow	0 D_7	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0 3D 00-FF	2	2+S	(D_{7-0}) = 0H
IES	E←E + 1 skip if E = 0H	Increment E; skip if overflow	0	1	0	0	1	0	0	1 49	1	1+S	E = 0H
IHL	HL←HL + 1	Increment HL	0 1	0 0	1 0	1 1	1 1	1 1	1 0	0 3E 1 9D	2	2	
ILS	L←L + 1 skip if L = 0H	Increment L; skip if overflow	0	1	0	1	1	0	0	1 59	1	1+S	L = 0H 1
Bit Manipulation													
RMB bit	(HL)bit←0 bit = B_{1-0} (0-3)	Reset Memory bit	0	1	1	0	1	0	B_1	B_0 68-6B	1	1	
SMB bit	(HL)bit←1 bit = B_{1-0} (0-3)	Set Memory bit	0	1	1	0	1	1	B_1	B_0 6C-6F	1	1	

3

Instruction Set "A" (Cont.)

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
			Branch											
CALL addr	(SP – 1)←PC_{7-4} (SP – 2)←PC_{3-0} (SP – 3)←PSW (SP – 4)←PC_{11-18} SP←SP – 4 BANK←0 PC_{11}←0 PC_{10-0}←D_{10-0}	Call subroutine	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	30-37 00-FF	2	2	
CALT addr	(SP – 1)←PC_{7-4} (SP – 2)←PC_{3-0} (SP – 3)←PSW (SP – 4)←PC_{11-8} ROM addr = 0C0H + D_{5-0} BANK←0 PC_{11-10}←00 PC_{9-7}←[ROM addr]7-5 PC_{6-5}←00 PC_{4-0}←[ROM addr]4-0	Call subroutine through ROM Table (single byte)	1	1	D_5	D_4	D_3	D_2	D_1	D_0	D0-FF	1	2	
JAM data	PC_{11-8}←D_{3-0} PC_{7-4}←A PC_{3-0}←(HL)	Vectored Jump on Accumulator and Memory	0 0	0 0	1 0	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 10-1F	2	2	
JCP addr	PC_{5-0}←D_{5-0}	Jump within current page	1	0	D_5	D_4	D_3	D_2	D_1	D_0	80-BF	1	1	
JMP addr	PC_{11-0}←D_{11-0}	Jump to specified address	0 D_7	0 D_6	1 D_5	0 D_4	D_{11} D_3	D_{10} D_2	D_9 D_1	D_8 D_0	20-2F 00-FF	2	2	
JUMPL addr	BANK←D_{12} PC_{11-0}←D_{11-0}	Jump Long to specified address	0 0 D_7	0 0 D_6	1 D_{12} D_5	1 0 D_4	1 D_{11} D_3	1 D_{10} D_2	1 D_9 D_1	1 D_8 D_0	3F 00-0F 20-2F 00-FF	3	3	
RT	PC_{11-8}←(SP) BANK←(SP + 1) PC_{3-0}←(SP + 2) PC_{7-4}←(SP + 3) SP←SP + 4	Return from Subroutine	0	1	0	1	0	0	1	1	53	1	1	
RTPSW	PC_{11-8}←(SP) PSW←(SP + 1) PC_{3-0}←(SP + 2) PC_{7-4}←(SP + 3) SP←SP + 4	Return from Subroutine and restore PSW	0	1	0	0	0	0	1	1	43	1	2	
RTS	PC_{11-8}←(SP) BANK←(SP + 1) PC_{3-0}←(SP + 2) PC_{7-4}←(SP + 3) SP←(SP + 4) Skip unconditionally	Return from Subroutine; then skip next instruction	0	1	0	1	1	0	1	1	5B	1	1+S	Unconditional
			Stack											
POPDE	E←(SP) D←(SP + 1) SP←SP + 2	Pop DE register pair off Stack	0 1	0 0	1 0	1 0	1 1	1 1	1 1	0 1	3E 8F	2	2	
POPHL	L←(SP) H←(SP + 1) SP←SP + 2	Pop HL register pair off Stack	0 1	0 0	1 0	1 1	1 1	1 1	1 1	0 1	3E 9F	2	2	
PSHDE	(SP – 1)←D (SP – 2)←E SP←SP – 2	Push DE register pair on Stack	0 1	0 0	1 0	1 0	1 1	1 1	1 1	0 0	3E 8E	2	2	
PSHHL	(SP – 1)←H (SP – 2)←L SP←SP – 2	Push HL register pair on Stack	0 1	0 0	1 0	1 1	1 1	1 1	1 1	0 0	3E 9E	2	2	
TAMSP	SP_{7-4}←A SP_{3-1}←$(HL)_{3-1}$ SP_0←0	Transfer Accumulator and Memory to Stack Pointer	0 0	0 0	1 1	1 1	1 0	1 0	1 0	1 1	3F 31	2	2	
TSPAM	A←SP_{7-4} $(HL)_{3-1}$←SP_{3-1} $(HL)_0$←0	Transfer Stack Pointer to Accumulator and Memory	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 1	3F 35	2	2	
			Conditional Skip											
SKABT bit	Skip if A_{bit} = 1 bit = $B_{1-0(0-3)}$	Skip if Accumulator bit true	0	1	1	1	0	1	B_1	B_0	74-77	1	1+S	A_{bit} = 1
SKAEI data	Skip if A = D_{3-0}	Skip if Accumulator equals immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 60-6F	2	2+S	A = D_{3-0}
SKAEM	Skip if A = (HL)	Skip if Accumulator equals Memory	0	1	0	1	1	1	1	1	5F	1	1+S	A = (HL)
SKC	Skip if C = 1	Skip if Carry	0	1	0	1	1	0	1	0	5A	1	1+S	C = 1
SKDEI data	Skip if D = D_{3-0}	Skip if D equals immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 60-6F	2	2+S	D = D_{3-0}
SKEEI data	Skip if E = D_{3-0}	Skip if E equals immediate data	0 0	0 1	1 0	1 0	1 D_3	1 D_2	1 D_1	0 D_0	3E 40-4F	2	2+S	E = D_{3-0}
SKHEI data	Skip if H = D_{3-0}	Skip if H equals immediate data	0 0	0 1	1 1	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 70-7F	2	2+S	H = D_{3-0}

Instruction Set "A" (Cont.)

For the μPD7500, μPD7502, μPD7503, μPD7507, μPD7507S, μPD7508, μPD7508A, and μPD7519 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
Conditional Skip (Cont.)														
SKLEI data	Skip if L = D_{3-0}	Skip if L equals immediate data	0 0	0 1	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 50-5F	2	2+S	L = D_{3-0}
SKMBF bit	Skip if $(HL)_{bit}$ = 0 bit = B_{1-0}(0-3)	Skip if Memory bit false	0	1	1	0	0	0	B_1	B_0	60-63	1	1+S	$(HL)_{bit}$ = 0
SKMBT bit	Skip if $(HL)_{bit}$ = 1 bit = B_{1-0}(0-3)	Skip if Memory bit true	0	1	1	0	0	1	B_1	B_0	64-67	1	1+S	$(HL)_{bit}$ = 1
SKMEI	Skip if (HL) = D_{3-0}	Skip if Memory equals immediate data	0 0	0 1	1 1	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 70-7F	2	2+S	(HL) = D_{3-0}
Timer/Event Counter														
TAMMOD	TMR_{7-4}←A TMR_{3-0}←(HL)	Transfer Accumulator and Memory to Timer Modulo Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 1	3F 3F	2	2	
TCNTAM	A←TCR_{7-4} (HL)←TCR_{3-0}	Transfer Timer Count Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 1	3F 3B	2	2	
TIMER	TCR_{7-0}←0 IRF_T←0	Start Timer	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 0	3F 32	2	2	
Interrupt Control														
DI data	IME F/F←0 if data = 0 IER_{3-0}←IER_{3-0} AND NOT D_{3-0} if data < > 0	Disable Interrupt, Interrupt Master Enable F/F or specified	0 1	0 0	1 0	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 80-8F	2	2	
EI data	IME F/F←1 if data = 0 IER_{3-0}←IER_{3-0} OR D_{3-0} if data < > 0	Enable Interrupt, Interrupt Master Enable F/F or specified	0 1	0 0	1 0	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 90-8F	2	2	
SKI data	Skip if IRF_n AND D_{3-0} < > 0 IRF_n←IRF_n AND NOT D_{3-0}	Skip if Interrupt Request Flag is true	0 0	0 1	1 0	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 40-4F	2	2+S	IRF_n = 1
Serial Interface														
SIO	SIOCR←0 $IRF_{0/S}$←0	Start Serial I/O Operation	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 1	3F 33	2	2	
TAMSIO	SIO_{7-4}←A SIO_{3-0}←(HL)	Transfer Accumulator and Memory to SI Shift Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 0	3F 3E	2	2	
TSIOAM	A←SIO_{7-4} (HL)←SIO_{3-0}	Transfer SI Shift Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 0	3F 3A	2	2	
Parallel I/O														
ANP data	$P(P_{3-0})$←$P(P_{3-0})$ AND D_{3-0}	AND output port latch with immediate data	0 D_3	1 D_2	0 D_1	0 D_0	1 P_3	1 P_2	0 P_1	0 P_0	4C 00-FF	2	2	
IP port	A←$P(P_{3-0})$	Input from port, immediate address	0 1	0 1	1 0	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F C0-CF	2	2	
IP1 (except μPD7507S)	A←P(1)	Input from Port 1	0	1	1	1	0	0	0	1	71	1	1	
IP54	A←P(5) (HL)←P(4)	Input Byte from Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 0	1 0	1 0	3F 38	2	2	
IPL	A←P(L)	Input from Port specified by L	0	1	1	1	0	0	0	0	70	1	1	
OP port	$P(P_{3-0})$←A	Output to port, immediate address	0 1	0 1	1 1	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F E0-EF	2	2	
OP3	P(3)←A	Output to Port 3	0	1	1	1	0	0	1	1	73	1	1	
OP54	P(5)←A P(4)←(HL)	Output Byte to Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 1	1 0	1 0	3F 3C	2	2	
OPL	P(L)←A	Output to port specified by L	0	1	1	1	0	0	1	0	72	1	1	
ORP data	$P(P_{3-0})$←(P_{3-0}) OR D_{3-0}	OR output port latch with immediate data	0 D_3	1 D_2	0 D_1	0 D_0	1 P_3	1 P_2	0 P_1	1 P_0	4D 00-FF	2	2	
RPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit (L_{1-0})←0	Reset Port Bit specified by L	0	1	0	1	1	1	0	0	5C	1	1	
SPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit (L_{1-0})←1	Set Port Bit specified by L	0	1	0	1	1	1	0	1	5D	1	1	
CPU Control														
HALT		Enter HALT Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 0	3F 36	2	2	
NOP		No operation	0	0	0	0	0	0	0	0	00	1	1	
STOP		Enter STOP Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 1	3F 37	2	2	

Instruction Set "B"

For the μPD7500, μPD7501, and μPD7506 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
		Load												
LADR addr	A←(D_{6-0})	Load Accumulator from directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	38 00-5F	2	2	
LAI data	A←D_{3-0}	Load Accumulator with immediate data	0	0	0	1	D_3	D_2	D_1	D_0	10-1F	1	1	String
LAM rp	A←(rp) rp = HL−, HL+, HL if rp = HL−, skip if borrow if rp = HL+, skip if overflow	Load Accumulator from Memory, possible skip	0	1	0	1	0	0	D_1	D_0	50-52	1	1+S	See explanation of "rp" in symbol definitions
LAMT	ROM addr = PC_{10-8}, 0, C, A_{3-0} A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table	0	1	0	1	1	1	1	0	5E	1	2	
LAMTL	ROM addr = PC_{10-8}, A_{3-0}, (HL)$_{3-0}$ A←[ROM addr]$_{7-4}$ (HL)←[ROM addr]$_{3-0}$	Load Accumulator and Memory from Table Long	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 0	3F 34	2	2	
LHI data	H_3←0 H_{2-0}←D_{2-0}	Load H register with immediate data	0	0	1	0	1	D_2	D_1	D_0	28-2F	1	1	
LHLI data	H_{3-1}←0 H_0←D_4 L←D_{3-0}	Load HL register pair with immediate data	1	1	0	D_4	D_3	D_2	D_1	D_0	C0-DF	1	1	String
		Store												
ST	(HL)←A	Store A to Memory	0	1	0	1	0	1	1	1	57	1	1	
STII data	(HL)←D_{3-0} L←L + 1	Store immediate data and increment L	0	1	0	0	D_3	D_2	D_1	D_0	40-4F	1	1	
		Exchange												
XADR addr	A↔(D_{6-0})	Exchange A with directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	39 00-5F	2	2	
XAH	A↔H	Exchange A with H	0	1	1	1	1	0	1	0	7A	1	1	
XAL	A↔L	Exchange A with L	0	1	1	1	1	0	1	1	7B	1	1	
XAM rp	A↔(rp) rp = HL−, HL+, HL if rp = HL−, skip if borrow if rp = HL+, skip if overflow	Exchange A with Memory, Possible Skip	0	1	0	1	0	1	D_1	D_0	54-56	1	1+S	See explanation or "rp" in symbol definitions
XHDR addr	H↔(D_{6-0})	Exchange H with directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	0 D_0	3A 00-5F	2	2	
XLDR addr	L↔(D_{6-0})	Exchange L with directly addressed RAM	0 0	0 D_6	1 D_5	1 D_4	1 D_3	0 D_2	1 D_1	1 D_0	3B 00-5F	2	2	
		Arithmetic												
ACSC	A, C←A ± (HL) + C skip if carry	Add with carry; skip if carry	0	1	1	1	1	1	0	0	7C	1	1+S	Carry = 1
AISC data	A←A + D_{3-0} skip if overflow	Add immediate; skip if overflow	0	0	0	0	D_3	D_2	D_1	D_0	00-0F	1	1+S	Overflow
ASC	A←A + (HL) skip if overflow	Add memory; skip if overflow	0	1	1	1	1	1	0	1	7C	1	1+S	Carry = 1
		Logical												
ANL	A←A AND (HL)	AND Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 0	3F B2	2	2	
EXL	A←A XOR (HL)	Exclusive-Or Accumulator and Memory	0	1	1	1	1	1	1	0	7E	1	1	
ORL	A←A OR (HL)	OR Accumulator and Memory	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 0	3F B6	2	2	
		Accumulator												
CMA	A←NOT A	Complement Accumulator	0	1	1	1	1	1	1	1	7F	1	1	
RAL	C←A_3 A_3←A_2 A_2←A_1 A_1←A_0 A_0←C (old)	Rotate Accumulator left through Carry	0 1	0 0	1 1	1 1	1 0	1 1	1 1	1 1	3F B7	2	2	
RAR	C←A_0 A_0←A_1 A_1←A_2 A_2←A_3 A_3←C (old)	Rotate Accumulator right through Carry	0 1	0 0	1 1	1 1	1 0	1 0	1 1	1 1	3F B3	2	2	
		Program Status Word												
RC	C←0	Reset Carry	0	1	1	1	1	0	0	0	78	1	1	
SC	C←1	Set Carry	0	1	1	1	1	0	0	1	79	1	1	

Instruction Set "B" (Cont.)

For the μPD7500, μPD7501, and μPD7506 devices only

Mnemonic	Function	Description	Instruction Code D7	D6	D5	D4	D3	D2	D1	D0	HEX	Bytes	Cycles	Skip Condition
Increment and Decrement														
DDRS addr	$(D_{6-0}) \leftarrow (D_{6-0}) - 1$ skip if (D_{6-0}) = FH	Decrement directly addressed RAM; skip if borrow	0 0	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	3C 00-5F	2	2+S	(D_{6-0}) = FH
DLS	$L \leftarrow L - 1$ skip if L = FH	Decrement L; skip if borrow	0	1	0	1	1	0	0	0	58	1	1+S	L = FH
IDRS addr	$(D_{6-0}) \leftarrow (D_{6-0}) + 1$ skip if (D_{6-0}) = 0H	Increment directly addressed; skip if overflow	0 0	0 D_6	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	3D 00-5F	2	2+S	(D_{6-0}) = 0H
ILS	$L \leftarrow L + 1$ skip if L = 0H	Increment L; skip if overflow	0	1	0	1	1	0	0	1	59	1	1+S	L = 0H
Bit Manipulation														
RMB bit	$(HL)_{bit} \leftarrow 0$ bit = B_{1-0} (0-3)	Reset Memory bit	0	1	1	0	1	0	B_1	B_0	68-6B	1	1	
SMB bit	$(HL)_{bit} \leftarrow 1$ bit = B_{1-0} (0-3)	Set Memory bit	0	1	1	0	1	1	B_1	B_0	6C-6F	1	1	
Branch														
CALL addr	$(SP-1) \leftarrow PC_{7-4}$ $(SP-2) \leftarrow PC_{3-0}$ $(SP-3) \leftarrow PSW$ $(SP-4) \leftarrow PC_{10-8}$ $SP \leftarrow SP-4$ $BANK \leftarrow 0$ $PC_{10-0} \leftarrow D_{10-0}$	Call subroutine	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	30-37 00-FF	2	2	
CAL addr	$(SP-1) \leftarrow PC_{7-4}$ $(SP-2) \leftarrow PC_{3-0}$ $(SP-3) \leftarrow PSW$ $(SP-4) \leftarrow PC_{10-8}$ $BANK \leftarrow 0$ $PC_{10-0} \leftarrow 001D_4D_3000D_2D_1D_0$	Call short to CAL address subroutine	1	1	1	D_4	D_3	D_2	D_1	D_0	E0-FF	1	2	
JAM data	$PC_{10-8} \leftarrow D_{2-0}$ $PC_{7-4} \leftarrow A$ $PC_{3-0} \leftarrow (HL)$	Vectored Jump on Accumulator and Memory	0 0	0 0	1 0	1 1	1 0	1 D_2	1 D_1	1 D_0	3F 10-17	2	2	
JCP addr	$PC_{5-0} \leftarrow D_{5-0}$	Jump within current page	1	0	D_5	D_4	D_3	D_2	D_1	D_0	80-BF	1	1	
JMP addr	$PC_{10-0} \leftarrow D_{10-0}$	Jump to specified address	0 D_7	0 D_6	1 D_5	0 D_4	0 D_3	D_{10} D_2	D_9 D_1	D_8 D_0	20-27 00-FF	2	2	
JMPL addr	$BANK \leftarrow D_{12}$ $PC_{11-0} \leftarrow D_{11-0}$	Jump Long to specified address	0 0 D_7	0 0 D_6	1 D_{12} D_5	1 0 D_4	1 D_{11} D_3	1 D_{10} D_2	1 D_9 D_1	1 D_8 D_0	3F 00-0F 20-2F 00-FF	3	3	
RT	$PC_{10-8} \leftarrow (SP)$ $BANK \leftarrow (SP+1)$ $PC_{3-0} \leftarrow (SP+2)$ $PC_{7-4} \leftarrow (SP+3)$ $SP \leftarrow SP+4$	Return from Subroutine	0	1	0	1	0	0	1	1	53	1	1	
RTS	$PC_{10-8} \leftarrow (SP)$ $BANK \leftarrow (SP+1)$ $PC_{3-0} \leftarrow (SP+2)$ $PC_{7-4} \leftarrow (SP+3)$ $SP \leftarrow SP+4$ Skip unconditionally	Return from Subroutine; then skip next instruction	0	1	0	1	1	0	1	1	5B	1	1+S	Unconditional
Stack														
TAMSP	$SP_{7-4} \leftarrow A$ $SP_{3-1} \leftarrow (HL)_{3-1}$ $SP_0 \leftarrow 0$	Transfer Accumulator and Memory to Stack Pointer	0 0	0 0	1 1	1 1	1 0	1 0	1 0	1 1	3F 31	2	2	
TSPAM	$A \leftarrow SP_{7-4}$ $(HL)_{3-1} \leftarrow SP_{3-1}$ $(HL)_0 \leftarrow 0$	Transfer Stack Pointer to Accumulator and Memory	0 0	0 0	1 1	1 1	1 0	1 1	1 0	1 1	3F 35	2	2	
Conditional Skip														
SKABT bit	Skip if A_{bit} = 1 bit = B_{1-0}(0-3)	Skip if Accumulator bit true	0	1	1	1	0	1	B_1	B_0	74-77	1	1+S	A_{bit} = 1
SKAEI data	Skip if A = D_{3-0}	Skip if Accumulator equals immediate data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	3F 60-6F	2	2+S	A = D_{3-0}
SKAEM	Skip if A = (HL)	Skip if Accumulator equals Memory	0	1	0	1	1	1	1	1	5F	1	1+S	A = (HL)
SKC	Skip if C = 1	Skip if Carry	0	1	0	1	1	0	1	0	5A	1	1+S	C = 1
SKLEI data	Skip if L = D_{3-0}	Skip if L equals immediate data	0 0	0 1	1 0	1 1	1 D_3	1 D_2	1 D_1	0 D_0	3E 50-5F	2	2+S	L = D_{3-0}
SKMBF bit	Skip if $(HL)_{bit}$ = 0 bit = B_{1-0}(0-3)	Skip if Memory bit false	0	1	1	0	0	0	B_1	B_0	60-63	1	1+S	$(HL)_{bit}$ = 0
SKMBT bit	Skip if $(HL)_{bit}$ = 1 bit = B_{1-0}(0-3)	Skip if Memory bit true	0	1	1	0	0	1	B_1	B_0	64-67	1	1+S	$(HL)_{bit}$ = 1
SKMEI	Skip if (HL) = D_{3-0}	Skip if Memory equals immediate data	0 0	0 1	1 1	1 1	1 D_3	1 D_2	1 D_1	1 D_0	3F 70-7F	2	2+S	(HL) = D_{3-0}

Instruction Set "B" (Cont.)

For the μPD7500, μPD7501, and μPD7506 devices only

Mnemonic	Function	Description	Instruction Code									Bytes	Cycles	Skip Condition
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX			
Timer/Event Counter														
TAMMOD	$TMR_{7-4} \leftarrow A$ $TMR_{3-0} \leftarrow (HL)$	Transfer Accumulator and Memory to Timer Modulo Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 1	3F 3F	2	2	
TCNTAM (except μPD7506)	$A \leftarrow TCR_{7-4}$ $(HL) \leftarrow TCR_{3-0}$	Transfer Timer Count Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 1	3F 3B	2	2	
TIMER	$TCR_{7-0} \leftarrow 0$ $IRF_T \leftarrow 0$	Clear Timer Counter Register	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 0	3F 32	2	2	
Interrupts														
SKI data	Skip if IRF_n AND $D_{3-0} <> 0$ $IRF_n \leftarrow IRF_n$ AND NOT D_{3-0}	Skip if Interrupt Request Flag is true	0 0	0 1	1 0	1 0	1 0	1 D_2	1 D_1	1 D_0	3F 40-47	2	2+S	$IRF_n = 1$
Serial Interface														
SIO (except μPD7506)	$SIOCR \leftarrow 0$ $IRF_{0/S} \leftarrow 0$	Start Serial I/O Operation	0 0	0 0	1 1	1 1	1 0	1 0	1 1	1 1	3F 33	2	2	
TAMSIO (except μPD7506)	$SIO_{7-4} \leftarrow A$ $SIO_{3-0} \leftarrow (HL)$	Transfer Accumulator and Memory to SIO Shift Register	0 0	0 0	1 1	1 1	1 1	1 1	1 1	1 0	3F 3E	2	2	
TSIOAM (except μPD7506)	$A \leftarrow SIO_{7-4}$ $HL \leftarrow SIO_{3-0}$	Transfer SIO Shift Register to Accumulator and Memory	0 0	0 0	1 1	1 1	1 1	1 0	1 1	1 0	3F 3A	2	2	
Parallel I/O														
IP port	$A \leftarrow P(P_{3-0})$	Input from port, immediate address	0 1	0 1	1 0	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F C0-CF	2	2	
IP1	$A \leftarrow (1)$	Input from Port 1	0	1	1	1	0	0	0	1	71	1	1	
IP54	$A \leftarrow P(5)$ $(HL) \leftarrow P(4)$	Input Byte from Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 0	1 0	1 0	3F 38	2	2	
IPL	$A \leftarrow P(L)$	Input from Port specified by L	0	1	1	1	0	0	0	0	70	1	1	
OP port	$P(P_{3-0}) \leftarrow A$	Output to port, immediate address	0 1	0 1	1 1	1 0	1 P_3	1 P_2	1 P_1	1 P_0	3F E0-EF	2	2	
OP3 (except μPD7506)	$P(3) \leftarrow A$	Output to Port 3	0	1	1	1	0	0	1	1	73	1	1	
OP54	$P(5) \leftarrow A$ $P(4) \leftarrow (HL)$	Output Byte to Ports 5 and 4	0 0	0 0	1 1	1 1	1 1	1 1	1 0	1 0	3F 3C	2	2	
OPL	$P(L) \leftarrow A$	Output to port specified by L	0	1	1	1	0	0	1	0	72	1	1	
RPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit $(L_{1-0}) \leftarrow 0$	Reset Port Bit Specified by L	0	1	0	1	1	1	0	0	5C	1	1	
SPBL	μPD82C43 I/O Expander Port (L_{3-2}) bit $(L_{1-0}) \leftarrow 1$	Set Port Bit Specified by L	0	1	0	1	1	1	0	1	5D	1	1	
CPU Control														
HALT		Enter HALT Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 0	3F 36	2	2	
NOP		No operation	0	0	0	0	0	0	0	0	00	1	1	
STOP		Enter STOP Mode	0 0	0 0	1 1	1 1	1 0	1 1	1 1	1 1	3F 37	2	2	

Development Tools

For software development, editing, debugging, and assembly into object code, the NDS Development System, designed and manufactured by NEC Electronics U.S.A., Inc., is available. Additionally, for systems supporting either the ISIS-II (®Intel Corp.), CP/M (®Digital Research Corp.) operating systems, or Fortran IV ANSI 1966 V3.9, the ASM75 Cross-Assembler is available.

Once software development is complete, the code can be completely evaluated and debugged with hardware by the Evakit-7500 Evaluation Board. Available options include the Evakit-7500-LCD LCD driver board (for the μPD7501, μPD7502, and μPD7503), Evakit-7500-VFD Vacuum Fluorescent Display driver board (for the μPD7508A and μPD7519), and the Evakit-7500-RTT Real Time Tracer. The SE-7502 System Emulation Board will emulate complete functionality of the μPD7501, μPD7502, or μPD7503 for demonstrating your final system design. The SE-7508 System Emulation Board will emulate complete functionality of the μPD7506, μPD7507, μPD7507S, μPD7508, or μPD7508A for demonstrating your final system design. All of these boards take advantage of the capabilities of the μPD7500 Rom-less evaluation chip to perform their tasks.

Complete operation details on any μPD7500 Series CMOS 4-Bit Microcomputer can be found in the μPD7500 Series CMOS 4-Bit Microcomputer Technical Manual.

NEC

PRELIMINARY

μPD7501
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

Description

The μPD7501 is a CMOS 4-bit single chip microcomputer which has the μPD750x architecture.

The μPD7501 contains a 1024 x 8-bit ROM, and a 96 x 4-bit RAM.

The μPD7501 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7501 typically executes 63 instructions of the μPD7500 series "B" instruction set with a 10μs instruction cycle time.

The μPD7501 has two external and two internal edge-triggered testable interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. The on-board LCD controller/driver supervises all of the timing required by the 24 Port S segment drivers and the 4 Port COM backplane drivers, for either a 12-digit 7-segment quadriplexed LCD, or an 8-digit 7-segment triplexed LCD.

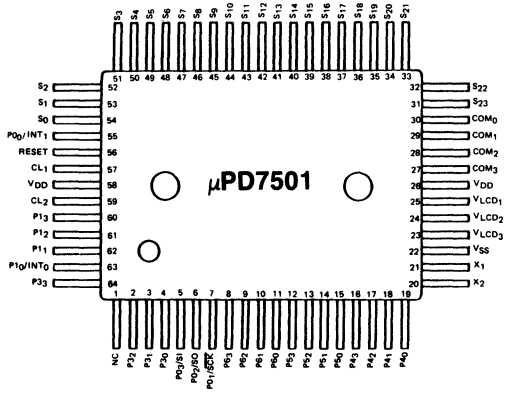
The μPD7501 provides 24 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit input Port 1, the 4-bit output Port 3, and the 4-bit I/O Ports 4, 5, and 6. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7501 is available in a space-saving 64-pin flat plastic package.

The μPD7501 is upward compatible with the μPD7502 and the μPD7503.

Pin Identification

Pin No.	Pin Symbol	Function
1	NC	No connection.
2-4, 64	$P3_3$-$P3_0$	4-bit latched tri-state output Port 3 (active high).
5	$P0_3$/SI	4-bit input Port 0/serial I/O interface (active high).
6 7 55	$P0_2$/SO $P0_1$/$\overline{SCK}$ $P0_0$/INT_1	This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer, comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_1.
8-11	$P6_3$-$P6_0$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
12-15	$P5_3$-$P5_0$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
16-19	$P4_3$-$P4_0$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
20, 21	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
22	V_{SS}	Ground.
23-25	V_{LCD_3}, V_{LCD_2}, V_{LCD_1}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.
26, 58	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
27-30	COM_3-COM_0	LCD backplane driver outputs.
31-54	S_{23}-S_0	LCD segment driver outputs.
56	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7501 after power-up.
57, 59	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
60-63	$P1_3$-$P1_0$ (PI_0/INT_0)	4-bit input Port 1 (active high). Line $P1_0$ is also shared with external interrupt INT_0.

Pin Configuration

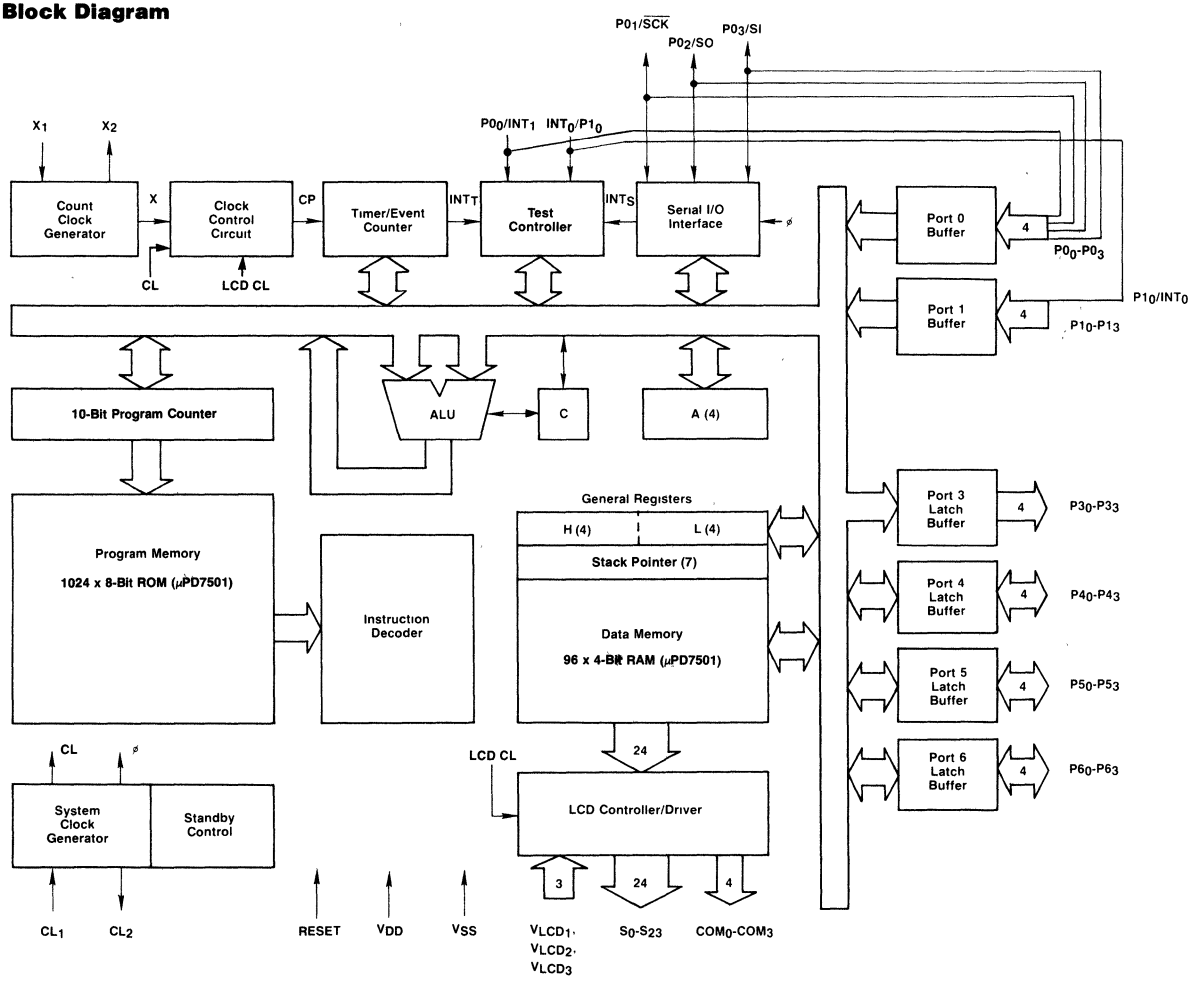


Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
Input Voltage High	V_{IH_1}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IH_2}	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL_1}	0		0 3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IL_2}	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LIH_1}			3	μA	All Inputs Other than CL_1, X_1	$V_I = V_{DD}$
	I_{LIH_2}			10		CL_1, X_1	
Input Leakage Current Low	I_{LIL_1}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	I_{LIL_2}			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	$V_O = V_{DD}$	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Output Impedance	R_{COM}			5	kΩ	COM_0 to COM_3, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			5				V_{DD} = 2.7V to 5.5V
	R_S			20		S_0 to S_{23}, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			20				V_{DD} = 2.7V to 5.5V
Supply Voltage	V_{DDDR}	2.0			V	Data Retention Mode	
Supply Current	I_{DD_1}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_2}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	I_{DDDR}		0.4	10		Data Retention Mode	V_{DDDR} = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
System Clock Oscillation Frequency	t_{CC}	120	200	280	KHz	CL_1, CL_2 R/C Clock R = 82 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		R = 160 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	t_C	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	t_{CR}, t_{CF}			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	t_{CH}, t_{CL}	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_{XX}	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
	f_X	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{XR}, t_{XF}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{X_H}, t_{X_L}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{KCY}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{K_H}, t_{K_L}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7v to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to $\overline{SCK}$↑	t_{SIK}	300			ns		
SI Hold Time after $\overline{SCK}$↑	t_{KSI}	450			ns		
SO Delay Time after $\overline{SCK}$↓	t_{KSO}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	t_{I0H}, t_{I0L}	10			μs		
INT_1 Pulse Width	t_{I1H}, t_{I1L}	$2/t_\phi$			μs		
RESET Pulse Width	t_{RS_H}, t_{RS_L}	10			μs		
RESET Setup Time	t_{SRS}	0			ns		
RESET Hold Time	t_{HRS}	0			ns		

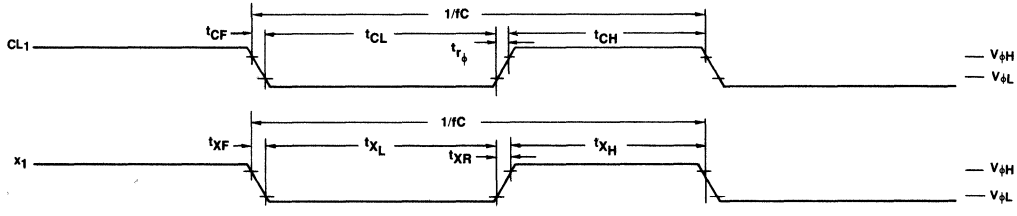
Capacitance

T_a = 25°C, V_{DD} = 0V

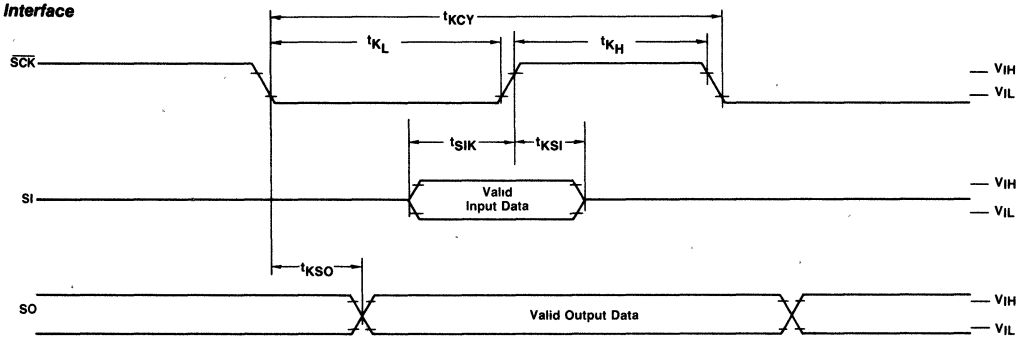
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15	pF	

Timing Waveforms

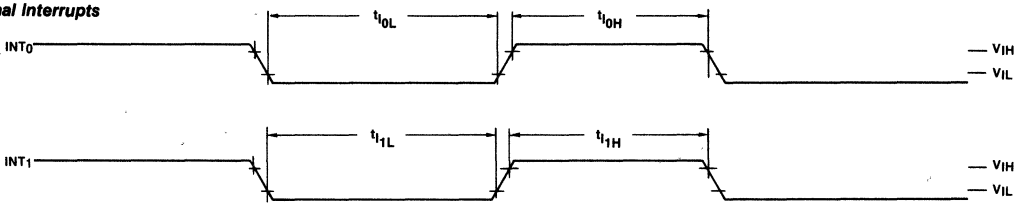
Clocks



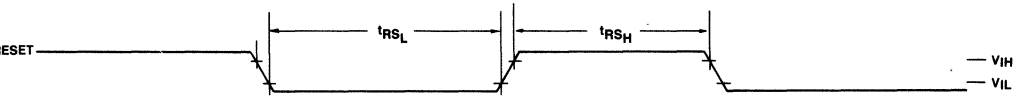
Serial Interface



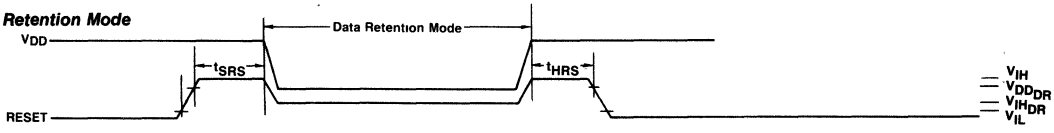
External Interrupts



Reset

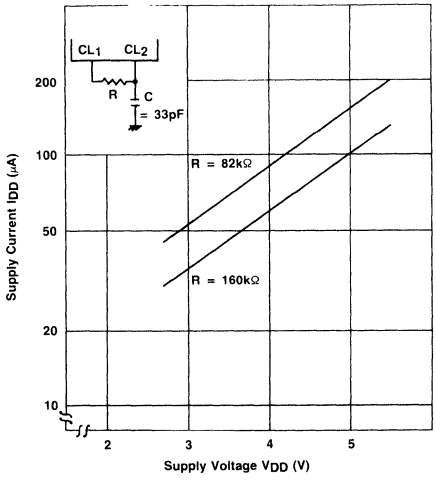


Data Retention Mode

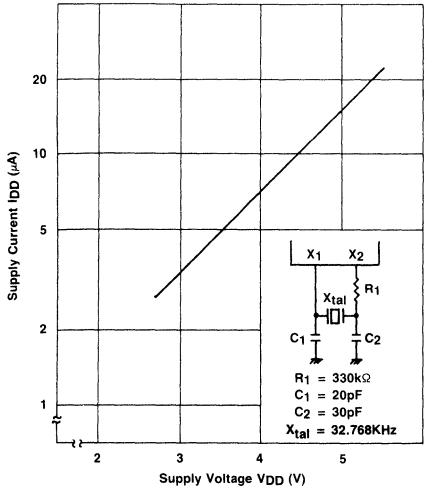


Operating Characteristics
Typical, T_a = 25°C

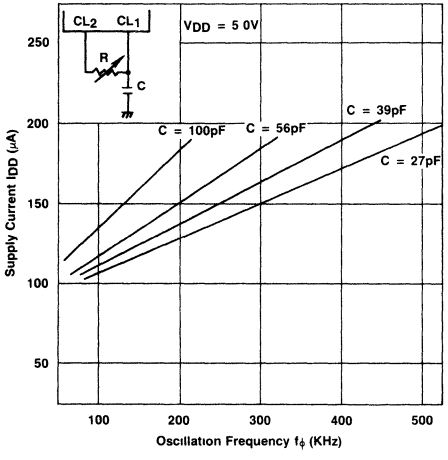
Supply Current
vs
Supply Voltage (Note ①)



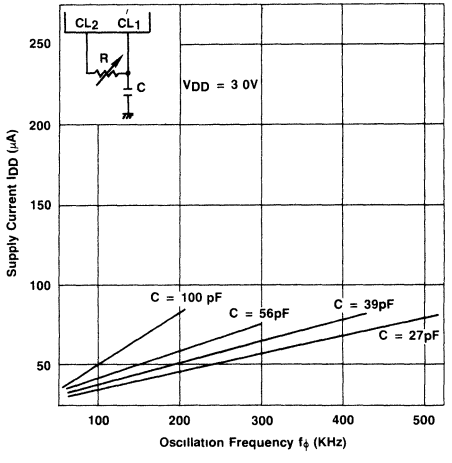
Supply Current
vs
Supply Voltage (Note ②)



Supply Current
vs
System Clock Oscillation Frequency
(Note ①)



Supply Current
vs
System Clock Oscillation Frequency
(Note ①)

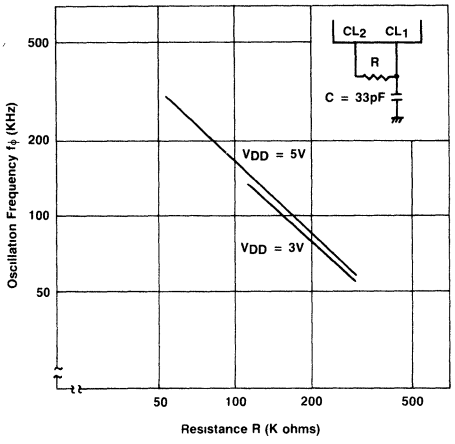


Notes:
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.
② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

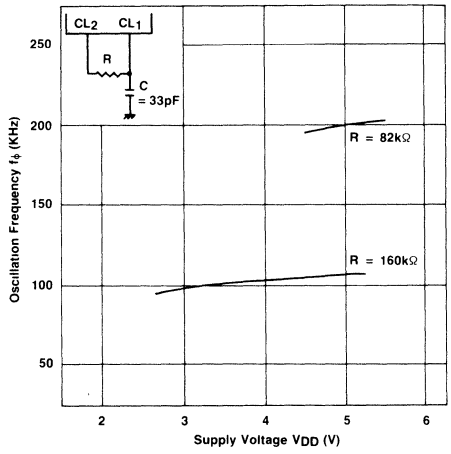
Operating Characteristics (Cont.)

Typical, T_a = 25°C

System Clock Oscillation Frequency vs Resistance



System Clock Oscillation Frequency vs Supply Voltage



Recommended R and C Values for the System Clock Oscillator Circuit

T_a = −10~ +70°C

Supply Voltage Range			Recommended Values		Frequency Range (kHz)		
Min	*Typ*	*Max*	R	C	*Min*	*Typ*	*Max*
4.5V < V_{DD} < 6V			82kΩ ± 2%	33pF ± 5% (|dC/°C| < 60 ppm)	150		250
2.7V < V_{DD} < 6V			160kΩ ± 2%	33pF ± 5% (|dC/°C| < 60 ppm)	75		135
V_{DD} = 3V ± 10%			160kΩ ± 2%	33pF ± 5% (|dC/°C| < 60 ppm)	75		120
2.5V < V_{DD} < 6V			240kΩ ± 2%	33pF ± 5% (|dC/°C| < 60 ppm)	50		85
2.5V < V_{DD} < 3.3V			240kΩ ± 2%	33pF ± 5% (|dC/°C| < 60 ppm)	50		80

Package Outlines

For information, see Package Outline Section 7.

Plastic Miniflat, μPD7501G

μPD7502
μPD7503
CMOS 4-BIT SINGLE CHIP MICROCOMPUTERS WITH LCD CONTROLLER/DRIVER

Description

The μPD7502 and the μPD7503 are pin-compatible CMOS 4-bit single chip microcomputers which have the same μPD750x architecture.

The μPD7502 contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM. The μPD7503 contains a 4096 x 8-bit ROM, and a 224 x 4-bit RAM.

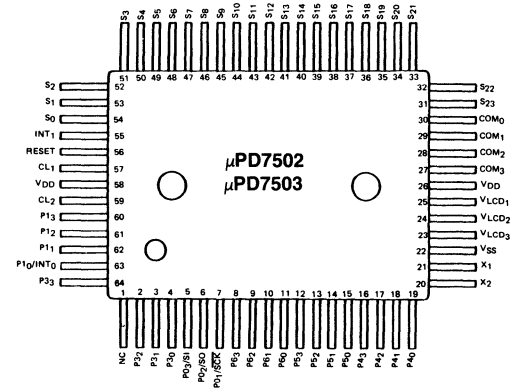
Both the μPD7502 and the μPD7503 contain four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7502 and the μPD7503 typically execute 92 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

The μPD7502 and the μPD7503 have two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. The on-board LCD controller/driver supervises all of the timing required by the 24 Port S segment drivers and the 4 Port COM backplane drivers, for either a 12-digit 7-segment quadriplexed LCD, or an 8-digit 7-segment triplexed LCD.

Both the μPD7502 and the μPD7503 provide 23 I/O lines, organized into the 3-bit input/serial interface Port 0, the 4-bit input Port 1, the 4-bit output Port 3, and the 4-bit I/O Ports 4, 5, and 6. They are manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7502 and the μPD7503 are available in a space-saving 64-pin flat plastic package.

The μPD7502 is downward compatible with the μPD7501.

Pin Configuration



Pin Names

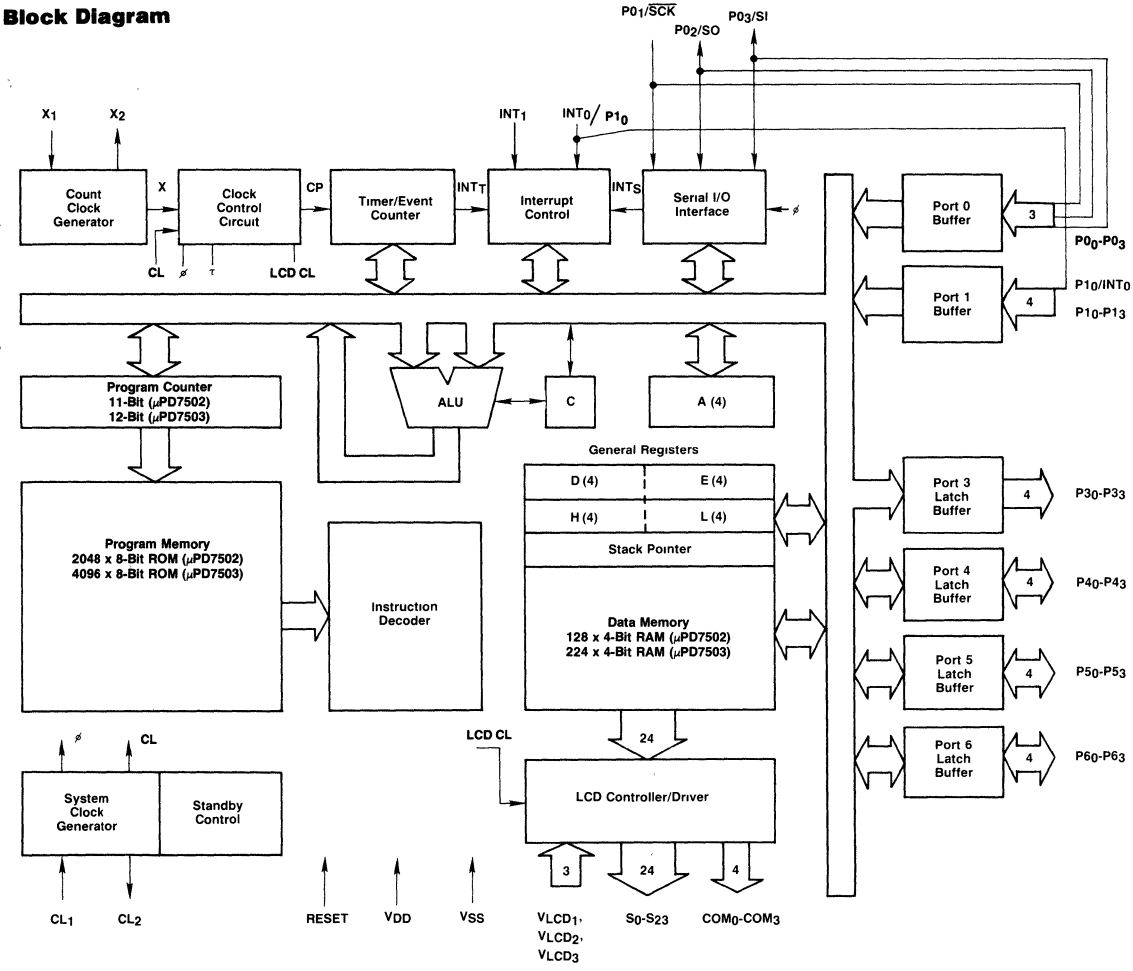
Pin No.	Symbol	Function
1	NC	No connection.
2-4, 64	$P3_3$-$P3_0$	4-bit latched tristate output Port 3 (active high).
5	$P0_3$/SI	3-bit input Port 0/serial I/O interface (active high)
6	$P0_2$/SO	This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active high), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer, comprise the 8-bit serial I/O interface
7	$P0_1/\overline{SCK}$	
8-11	$P6_3$-$P6_0$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register
12-15	$P5_3$-$P5_0$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
16-19	$P4_3$-$P4_0$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5
20, 21	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
22	V_{SS}	Ground
23-25	V_{LCD_3}, V_{LCD_2}, V_{LCD_1}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.
26, 58	V_{DD}	Power supply positive Apply single voltage ranging from 2.7V to 5 5V for proper operation.
27-30	COM_3-COM_0	LCD backplane driver outputs.
31-54	S_{23}-S_0	LCD segment driver outputs.
55	INT_1	External Interrupt INT_1 (active high). This is a rising edge-triggered interrupt
56	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7502 or μPD7503 after power-up.
57, 59	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
60-63	$P1_3$-$P1_0$ (PI_0/INT_0)	4-bit input Port 1 (active high). Line $P1_0$ is also shared with external interrupt INT_0, which is a rising edge-triggered interrupt.

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz,
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15	pF	

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
Input Voltage High	V_{IH_1}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IH_2}	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL_1}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IL_2}	0		0.5		CL_1, X_1	
Input Leakage Current High	$I_{LI_{H1}}$			3	μA	All Inputs Other than CL_1, X_1	V_I = V_{DD}
	I_{LIH_2}			10		CL_1, X_1	
Input Leakage Current Low	$I_{LI_{L1}}$			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	I_{LIL_2}			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	V_O = V_{DD}	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Output Impedance	R_{COM}			5	kΩ	COM_0 to COM_3, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			5				V_{DD} = 2.7V to 5.5V
	R_S			20		S_0 to S_{23}, 2.7V ≤ V_{LCD} ≤ V_{DD}	V_{DD} = 5V ± 10%
			20				V_{DD} = 2.7V to 5.5V
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_1}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_2}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

AC Characteristics

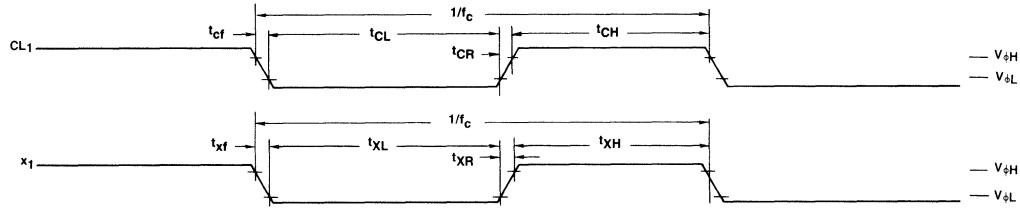
T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
System Clock Oscillation Frequency	f_{cc}	120	200	280	kHz	R = 82 kΩ ± 2%, C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		CL_1, CL_2 R/C Clock: R = 160 kΩ ± 2%, C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	f_c	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	t_{CR},t_{CF}			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	t_{CH},t_{CL},	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_{xx}	25	32	50	kHz	X_1, X_2 Crystal Oscillator	
	f_x	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{Xr},t_{Xf}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{XH},t_{XL}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{KCY}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{KH},t_{KL}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7v to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to SCK↑	t_{SIK}	300			ns		
SI Hold Time after SCK↑	t_{KSI}	450			ns		
SO Delay Time after SCK↓	t_{KSO}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	t_{I0H},t_{I0L}	10			μs		
INT_1 Pulse Width	t_{I1H},t_{I1L}	$2/f_\phi$			μs		
RESET Pulse Width	t_{RSH},t_{RSL}	10			μs		

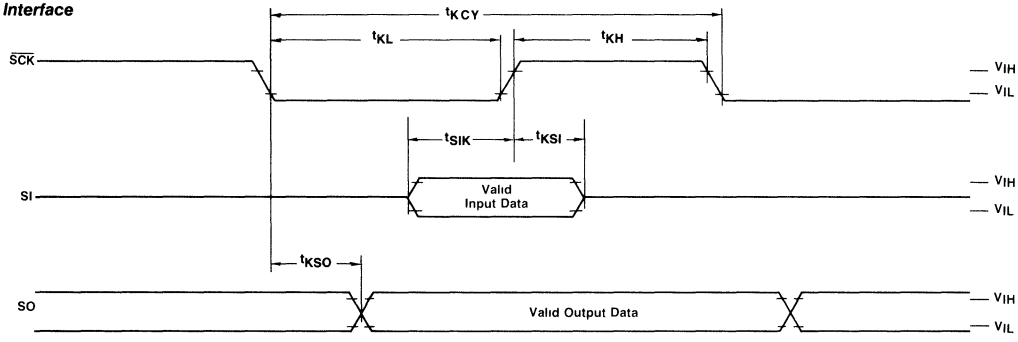
3

Timing Waveforms

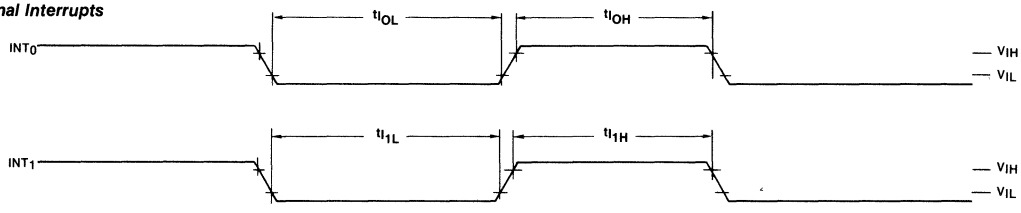
Clocks



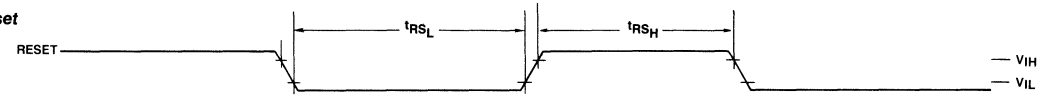
Serial Interface



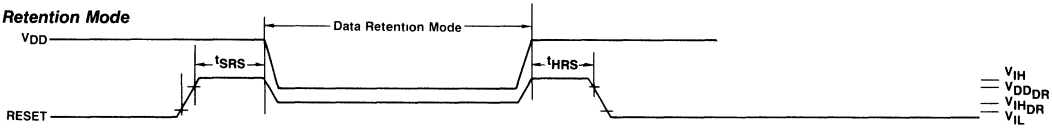
External Interrupts



Reset



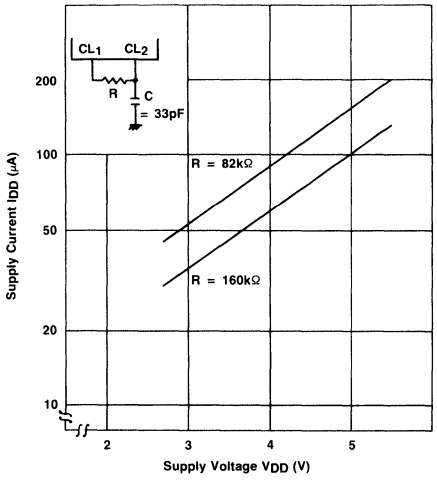
Data Retention Mode



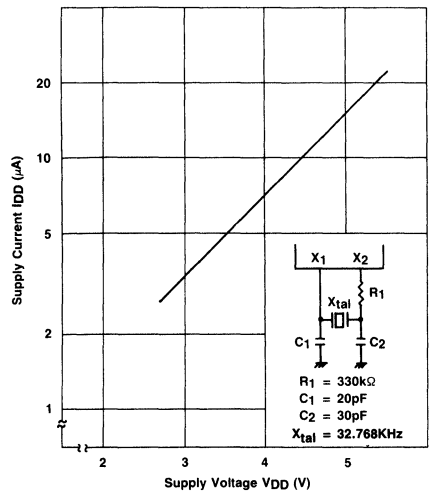
Operating Characteristics

Typical, T_a = 25°C

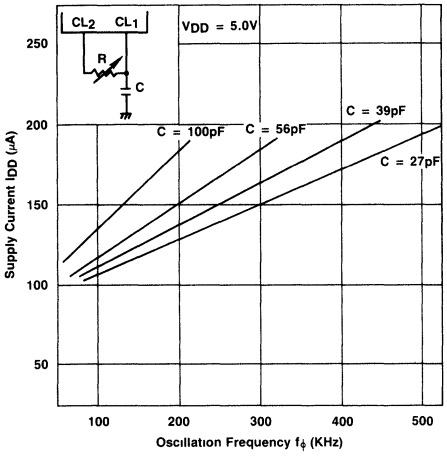
Supply Current vs Supply Voltage (Note ①)



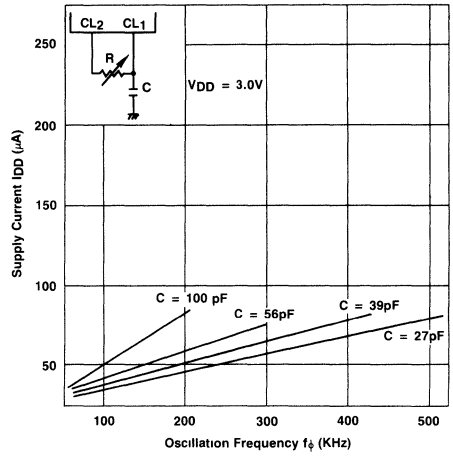
Supply Current vs Supply Voltage (Note ②)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Notes:

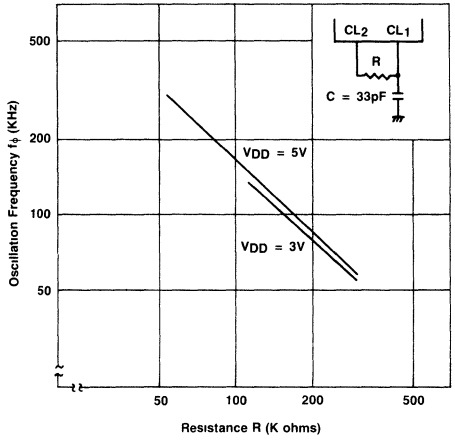
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

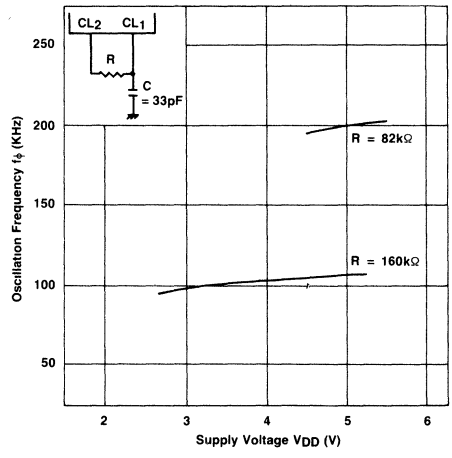
Operating Characteristics (Cont.)

Typical, T_a = 25°C

System Clock Oscillation Frequency vs Resistance



System Clock Oscillation Frequency vs Supply Voltage



Package Outlines

For information, see Package Outline Section 7.

Plastic Miniflat, μPD7502G/03G

Description

The μPD7506 is a CMOS 4-bit single chip microcomputer which has the μPD750x architecture.

The μPD7506 contains a 1024 x 8-bit ROM, and a 64 x 4-bit RAM.

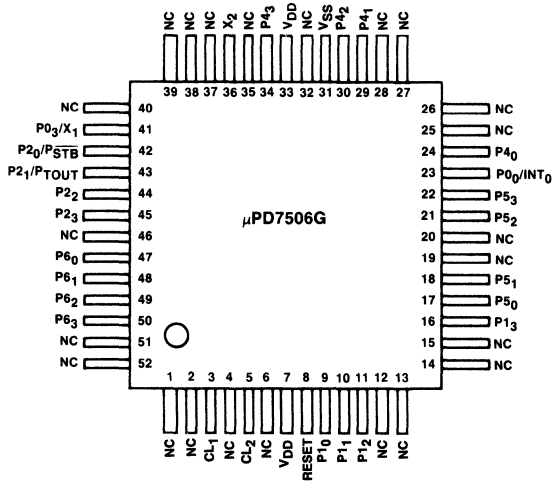
The μPD7506 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7506 typically executes 58 instructions of the μPD7500 series "B" instruction set with a 10μs instruction cycle time.

The μPD7506 has one external and one internal edge-triggered testable interrupts. It also contains an 8-bit timer/event counter to help reduce software requirements.

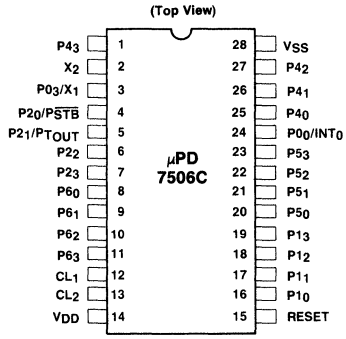
The μPD7506 provides 22 I/O lines, organized into the 2-bit input Port 0, the 4-bit output Port 2, and the 4-bit I/O Ports 1, 4, 5, and 6. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 600μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7506 is available either in a 28-pin dual-in-line plastic package, or in a space-saving 52-pin flat plastic package.

The μPD7506 is upward compatible with the μPD7507 and the μPD7507S.

Pin Configuration



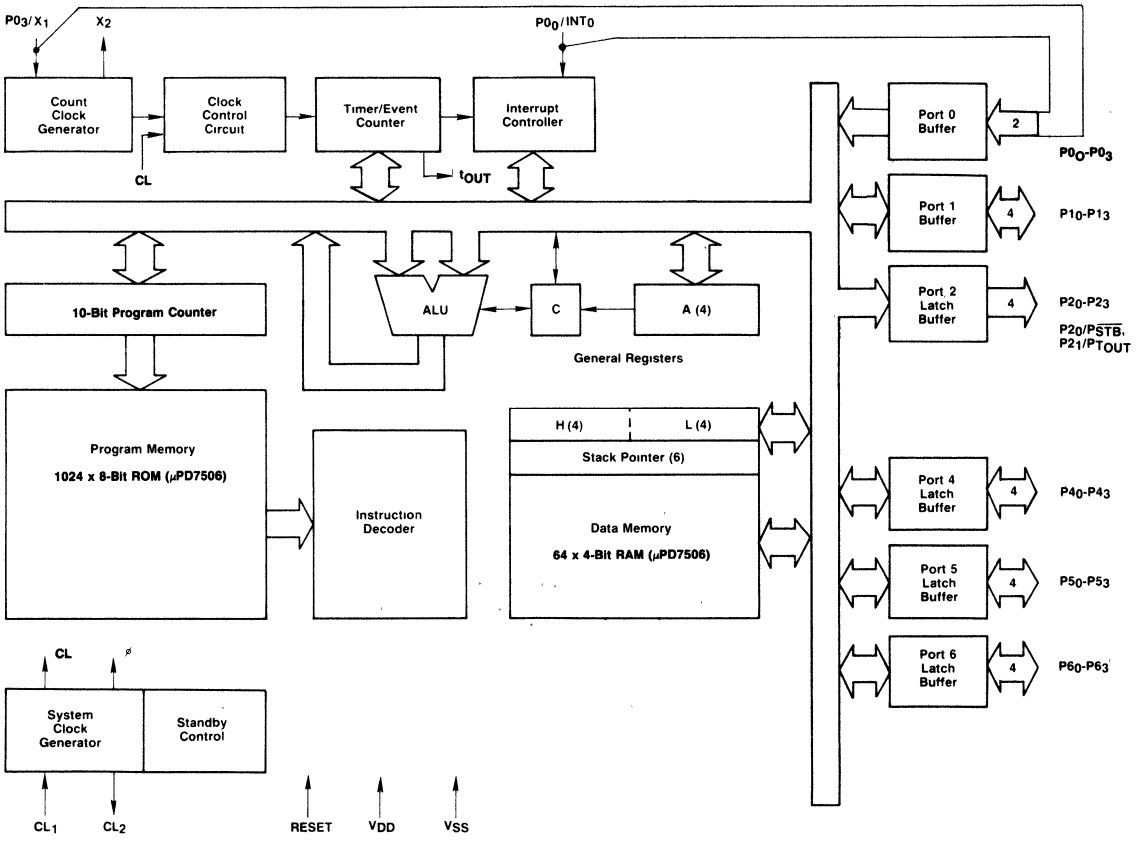
Pin Configuration (Cont.)



Pin Names

28-Pin DIP	52-Pin Flat	Symbol	Function
1, 25-27	24, 29, 30, 34	$P4_0$-$P4_3$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
2, 3	36, 41	X_2,$P0_3$/ X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting. Line X_1 is always shared with Port 0 input $P0_3$.
4-7	42-45	$P2_0$-$P2_3$ $P2_0$/$P\overline{STB}$ $P2_1$/P_{TOUT}	4-bit latched tristate output Port 2 (active high). Line $P2_0$ is also shared with $P\overline{STB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with P_{TOUT}, the timer-out F/F signal (active high).
8-11	47-50	$P6_0$-$P6_3$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
12, 13	3, 5	CL_1, CL_2	System clock input (active high). Connect 120kΩ resistor across CL_1 and CL_2. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
14	7, 33	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
15	8	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
16-19	9-11, 16	$P1_0$-$P1_3$	4-bit input/tristate output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0$/$P\overline{STB}$ pulse.
20-23	16-18, 21	$P5_0$-$P5_3$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
24, 3	23, 41	$P0_0$/INT_0 $P0_3$/X_1	2-bit input Port 0 (active high). Line $P0_0$ is always shared with external interrupt INT_0 (active high). Line $P0_3$ is always shared with crystal clock/external event input X_1 (active high).
28	31	V_{SS}	Ground.
—	1, 2, 4, 6 12-15, 19, 20, 25-28, 32, 35, 37-40, 46, 51, 52	NC	No connection.

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 32mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1MHz, Unmeasured pins returned to V_{SS}
Output Capacitance	C_O			15		
Input/Output Capacitance	$C_{I/O}$			15		

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IH_2}	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IL_2}	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	V_I = V_{DD}
	I_{LIH_2}			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	I_{LIL_2}			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400μA	
Output Leakage Current High	I_{LO_H}			3	μA	V_O = V_{DD}	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_1}		200	600	μA	Normal Operation	V_{DD} = 5V ± 10%
			100	300			V_{DD} = 3V ± 10%
	I_{DD_2}		1	10		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.3	5			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.3	5		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

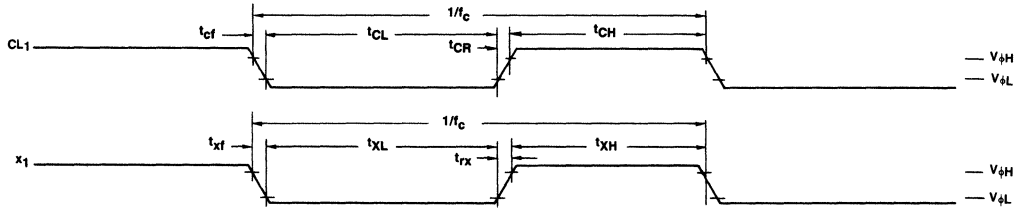
AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

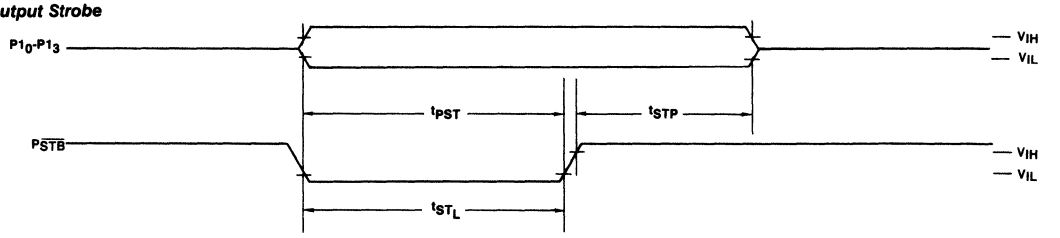
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
System Clock Oscillation Frequency	t_{cc}	120	200	260	kHz	R = 82 kΩ ± 2%	V_{DD} = 5V ± 10%
		60	100	130		CL_1, CL_2 R = 160 kΩ ± 2%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	t_c	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	t_{CR},t_{CF}			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	t_{CH},t_{CL}	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_{XX}	25	32	50	kHz	X_1, X_2 Crystal Oscillator	
	f_X	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{XR},t_{XF}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{XH},t_{XL}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
Port 1 Output Setup Time to $P_{\overline{STB}}$↑	t_{PST}	1/($2f_\phi$-800)			ns	V_{DD} = 5V ± 10%	
		1/($2f_\phi$-2000)				V_{DD} = 2.7V to 5.5V	
Port 1 Output Hold Time after $P_{\overline{STB}}$↑	t_{STP}	300	350	500	ns	V_{DD} = 5V ± 10%	
		300		1500		V_{DD} = 2.7V to 5.5V	
$P_{\overline{STB}}$ Pulse Width	t_{SW_L}	1/($2f_\phi$-800)			ns	V_{DD} = 5V ± 10%	
		1/($2f_\phi$-2000)				V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	t_{I0H}, t_{I0L}	10			μs		
$\overline{RESET}$ Pulse Width	t_{RS_H},t_{RS_L}	10			μs		

Timing Waveforms

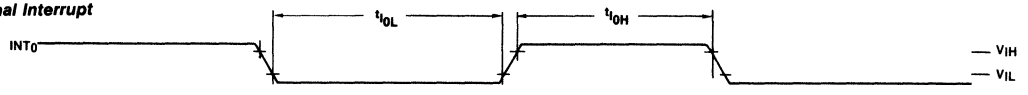
Clocks



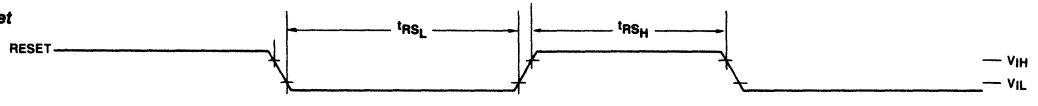
Output Strobe



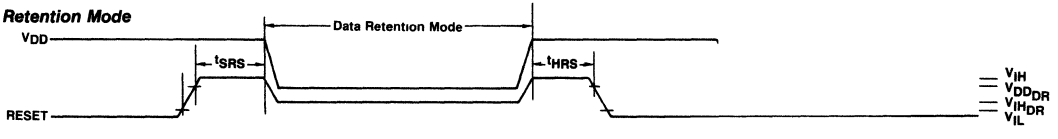
External Interrupt



Reset



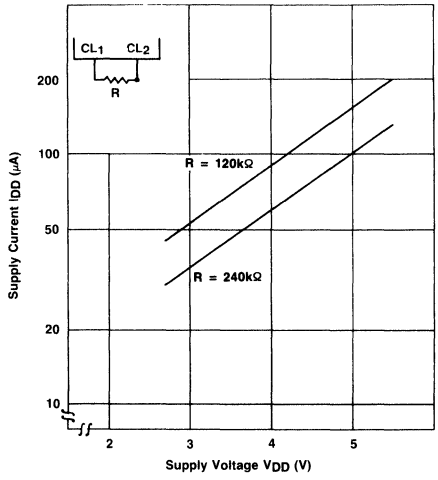
Data Retention Mode



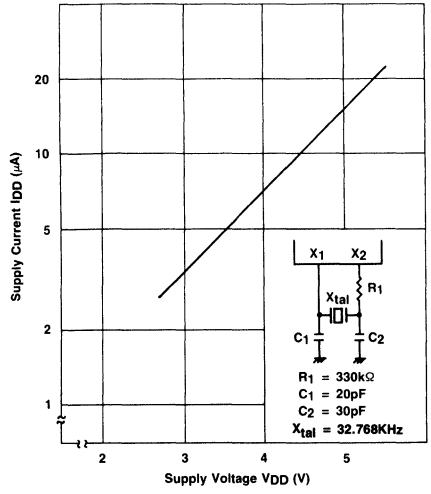
Operating Characteristics

Typical, T_a = 25°C

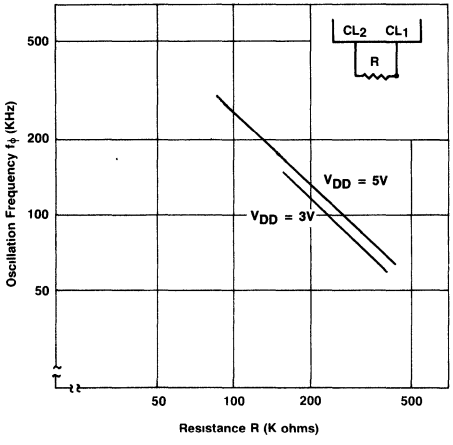
Supply Current vs Supply Voltage (Note ①)



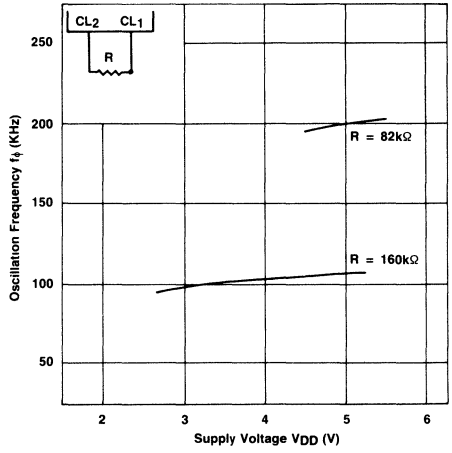
Supply Current vs Supply Voltage (Note ②)



System Clock Oscillation Frequency vs Resistance



System Clock Oscillation Frequency vs Supply Voltage



Notes:

① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7506C

Plastic Miniflat, μPD7506G

Plastic Shrinkdip, μPD7506CT

3

Notes

μPD7507
μPD7508
CMOS 4-BIT SINGLE CHIP MICROCOMPUTERS

Description

The μPD7507 and the μPD7508 are pin-compatible CMOS 4-bit single chip microcomputers which have the same μPD750x architecture.

The μPD7507 contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM. The μPD7508 contains a 4096 x 8-bit ROM, and a 224 x 4-bit RAM.

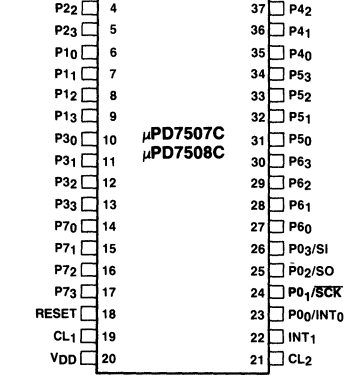
Both the μPD7507 and the μPD7508 contain four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7507 and the μPD5708 typically execute 92 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

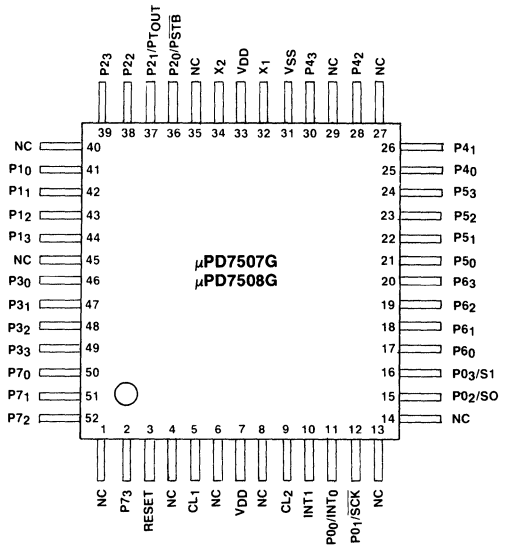
The μPD7507 and the μPD7508 have two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

Both the μPD7507 and the μPD7508 provide 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit input Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. They are manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7507 and the μPD7508 are available in either a 40-pin dual-in-line plastic package or in a space-saving 52-pin flat plastic package.

The μPD7507 is downward compatible with the μPD7506 and the μPD7507S.

Pin Configuration





Pin Identification

40-Pin DIP	52-Pin Flat	Symbol	Function
1, 40	32, 34	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
2-5	36-39	$P2_0$-$P2_3$ $P2_0/P\overline{STB}$ $P2_1/PT_{OUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_0$ is also shared with $P\overline{STB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with PT_{OUT}, the timer-out F/F signal (active high).
6-9	41-44	$P1_0$-$P1_3$	4-bit input/tri-state output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0/P\overline{STB}$ pulse.
10-13	46-49	$P3_0$-$P3_3$	4-bit latched tri-state output Port 3 (active high).
14-17	50-52, 2	$P7_0$-$P7_3$	4-bit input/latched tri-state output Port 7 (active high).
18	3	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
19, 21	5, 9	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
20	7, 33	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
22	10	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
23-26	11, 12 15, 16	$P0_0/INT_0$ $P0_1/\overline{SCK}$ $P0_2/SO$ $P0_3/SI$	4-bit input Port 0/Serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.

Pin Identification (Cont.)

40-Pin DIP	52-Pin Flat	Symbol	Function
27-30	17-20	$P6_0$-$P6_3$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
31-34	21-24	$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
35-38	25, 26, 28, 30	$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
39	31	V_{SS}	Ground.
—	1, 4, 6, 8, 13, 14, 27, 29, 35, 40, 45	NC	No connection.

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IH_2}	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ +0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IL_2}	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	V_I = V_{DD}
	I_{LIH_2}			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	I_{LIL_2}			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	V_{OUT} = V_{DD}	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_{OUT} = 0V	
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_1}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_2}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
System Clock Oscillation Frequency	f_{CC}	120	200	280	KHz	CL_1, CL_2 R = 82 kΩ ± 2%, C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	100	130		R = 160 kΩ ± 2%, C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		180			V_{DD} = 2.7V to 5.5V
	f_C	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	t_{CR},t_{CF}			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	t_{CH},t_{CL}	1.5		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_{XX}	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
	f_X	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{XR},t_{XF}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{XH},t_{XL}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V

AC Characteristics (Cont.)

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
$\overline{SCK}$ Cycle Time	t_{KCY}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{KH}, t_{KL}	1.8			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7v to 5.5V
		3.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to $\overline{SCK}$↑	t_{SIK}	300			ns		
SI Hold Time after $\overline{SCK}$↑	t_{KSI}	450			ns		
SO Delay Time after $\overline{SCK}$↓	t_{KSO}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
Port 1 Output Setup Time to $P_{\overline{STB}}$↑	t_{PST}	$1/(2f_\phi$-800)			ns	V_{DD} = 5V ± 10%	
		$1/(2f_\phi$-2000)				V_{DD} = 2.7V to 5.5V	
Port 1 Output Hold Time after $P_{\overline{STB}}$↑	t_{STP}	300	350	500	ns	V_{DD} = 5V ± 10%	
		300		1500		V_{DD} = 2.7V to 5.5V	
$P_{\overline{STB}}$ Pulse Width	t_{SW_L}	$f/(2f_\phi$-800)			ns	V_{DD} = 5V ± 10%	
		$f/(2f_\phi$-2000)				V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	t_{I0H}, t_{IOL}	10			μs		
INT_1 Pulse Width	$t_{I_1W_H}$, $t_{I_1W_L}$	$2/t_\phi$			μs		
RESET Pulse Width	t_{RS_H}, t_{RS_L}	10			μs		
RESET Setup Time	t_{SRS}	0			ns		
RESET Hold Time	t_{HRS}	0			ns		

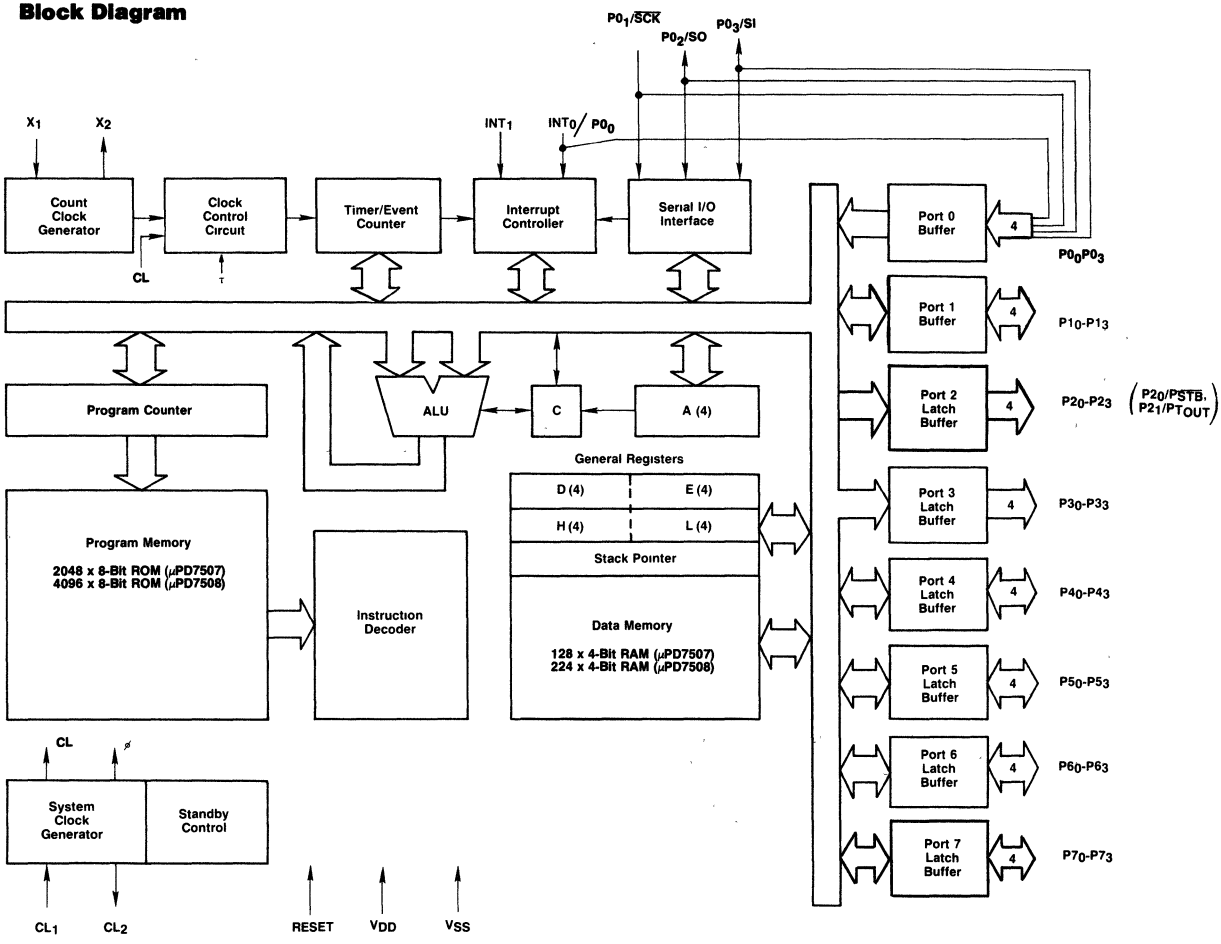
Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15		

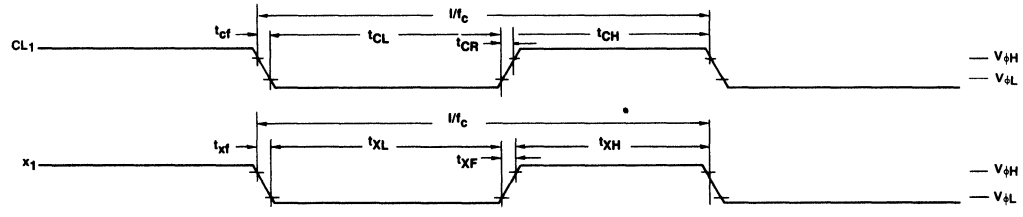
3

Block Diagram

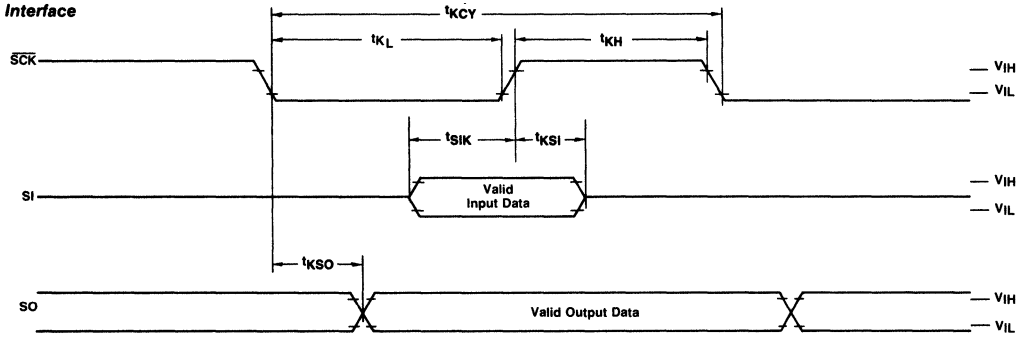


Timing Waveforms

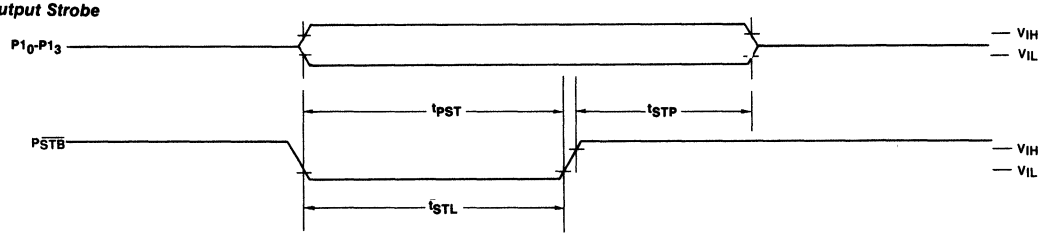
Clocks



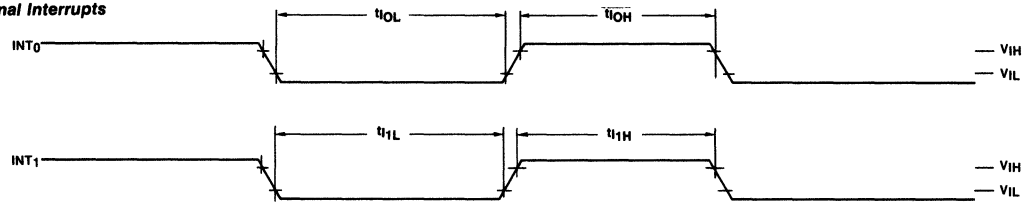
Serial Interface



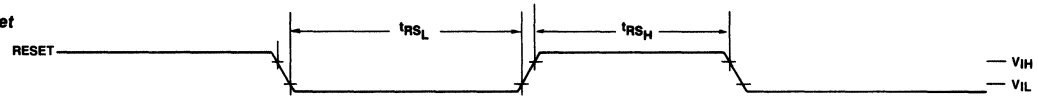
Output Strobe



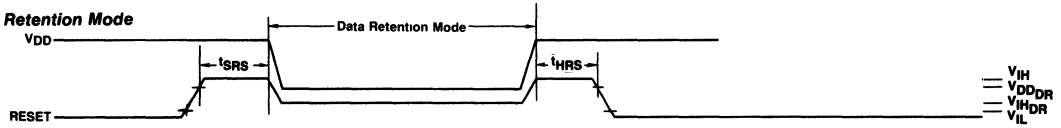
External Interrupts



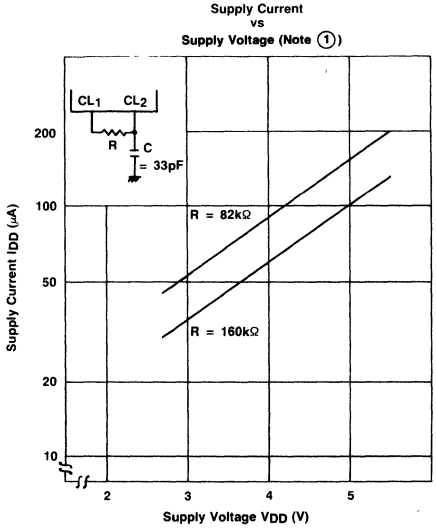
Reset

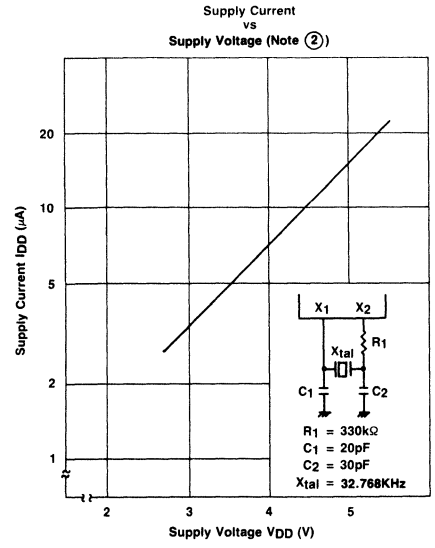


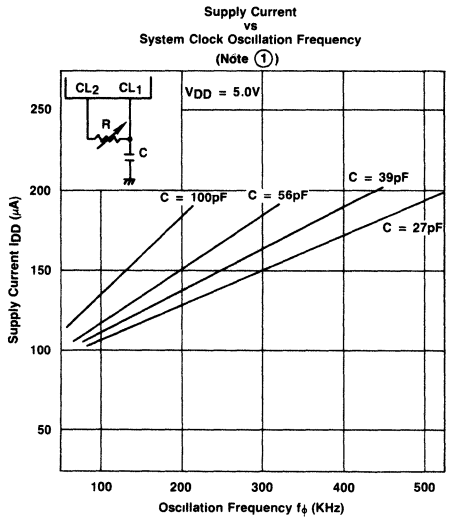
Data Retention Mode

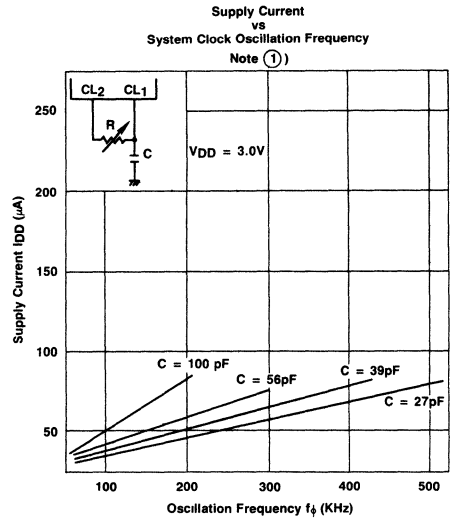


Operating Characteristics (Typical, T_a = 25°C)



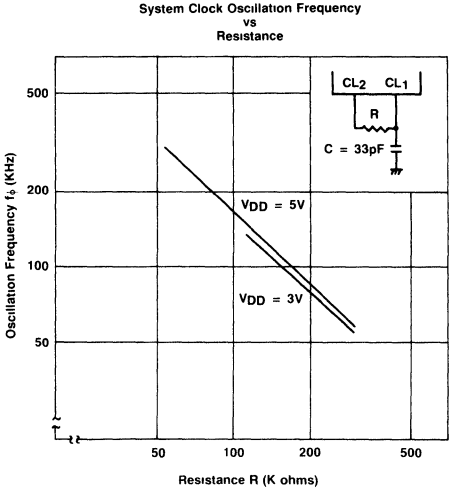


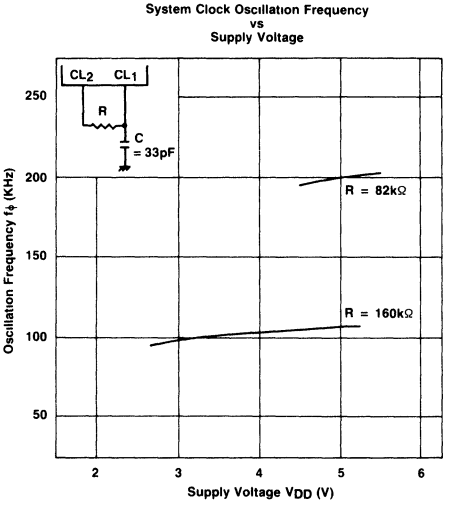




Notes:
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.
② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

Operating Characteristics (Cont.) (Typical, T_a = 25°C)





3

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7507C/08C
Plastic Miniflat, μPD7507G/08G
Plastic Shrinkdip, μPD7507CU μPD7508CU

PRELIMINARY

μPD7507S
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

Description

The μPD7507S is a CMOS 4-bit single chip microcomputer which has the same μPD750x architecture.

The μPD7507S contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM.

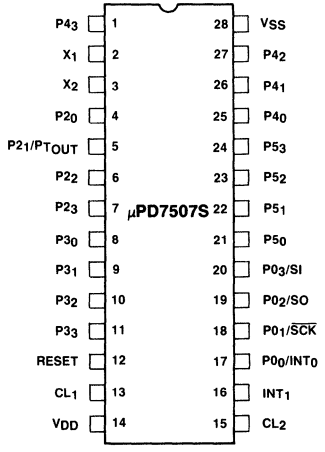
The μPD7507S contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7507S typically executes 91 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

The μPD7507S has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

The μPD7507S provides 20 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 4 and 5. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7507S is available in a 28-pin dual-in-line plastic package.

The μPD7507S is upward compatible with the μPD7507, and downward compatible with the μPD7506.

Pin Configuration



Pin Identification

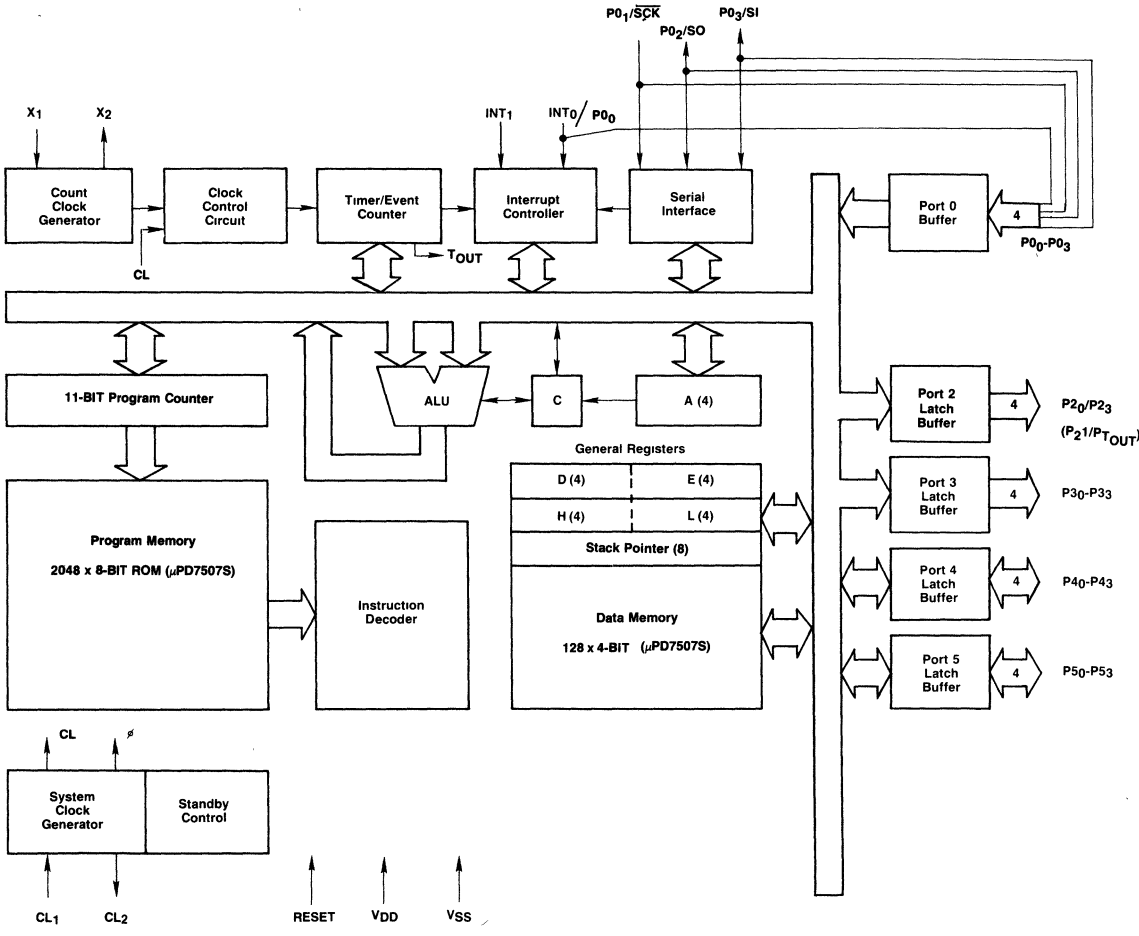
Pin No.	Pin Symbol	Function
1, 25-27	$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
2, 3	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
4-7	$P2_0$-$P2_3$ $P2_1/PT_{OUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_1$ is shared with PT_{OUT}, the timer-out F/F signal (active high).
8-11	$P3_0$-$P3_3$	4-bit latched tri-state output Port 3 (active high).
12	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
13, 15	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and $\overline{CL}_2$, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
14	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
16	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
17-20	$P0_0/INT_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.
21-24	$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
28	V_{SS}	Ground.

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = -17mA
	I_{OL} = -34mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IH_2}	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IL_2}	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than CL_1, X_1	$V_I = V_{DD}$
	V_{LIH_2}			10		CL_1, X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	V_{LIL_2}			−10		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	$V_O = V_{DD}$	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_1}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			70	300			V_{DD} = 3V ± 10%
	I_{DD_2}		1	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.3	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
System Clock Oscillation Frequency	t_{cc}	150	200	240	KHz	CL_1, CL_2 R/C Clock R = 82 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		75	100	120		R = 160 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		75		135			V_{DD} = 2.7V to 5.5V
	t_c	10	200	300		CL_1, External Clock	V_{DD} = 5V ± 10%
		10		135			V_{DD} = 2.7V to 5.5V
System Clock Rise and Fall Times	t_{CR}, t_{CF}			0.2	μs	CL_1, External Clock	
System Clock Pulse Width	t_{CH}, t_{CL}	1.1		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%
		3.5		50			V_{DD} = 2.7V to 5.5V
Counter Clock Oscillation Frequency	f_{xx}	20	32	50	KHz	X_1, X_2 Crystal Oscillator	
	f_x	0		300		X_1, External Pulse Input	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{xR}, t_{xF}			0.2	μs	X_1, External Pulse Input	
Counter Clock Pulse Width	t_{xH}, t_{xL}	1.5			μs	X_1, External Pulse Input	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{KCY}	4.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Pulse Width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7V to 5.5V
		2.2				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to $\overline{SCK}$↑	t_{SIK}	300			ns		
SI Hold Time after $\overline{SCK}$↑	t_{KSI}	450			ns		
SO Delay Time after $\overline{SCK}$↓	t_{KSO}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	$t_{I_{OH}}$, $t_{I_{OL}}$	10			μs		
INT_1 Pulse Width	$t_{I_{1H}}$, $t_{I_{1L}}$	$2/f_c$			μs		
RESET Pulse Width	t_{RS_H}, t_{RS_L}	10			μs		
RESET Setup Time	t_{SRS}	0			ns		
RESET Hold Time	t_{HRS}	0			ns		

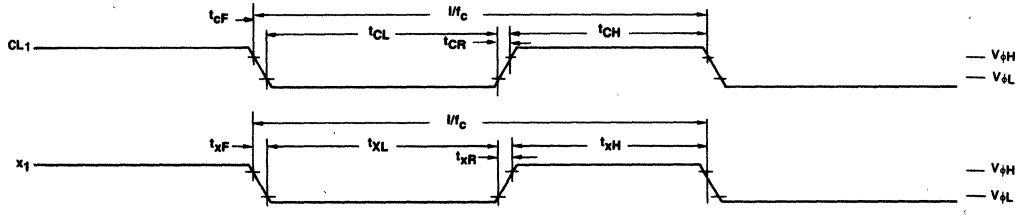
Capacitance

T_a = 25°C, V_{DD} = 0V

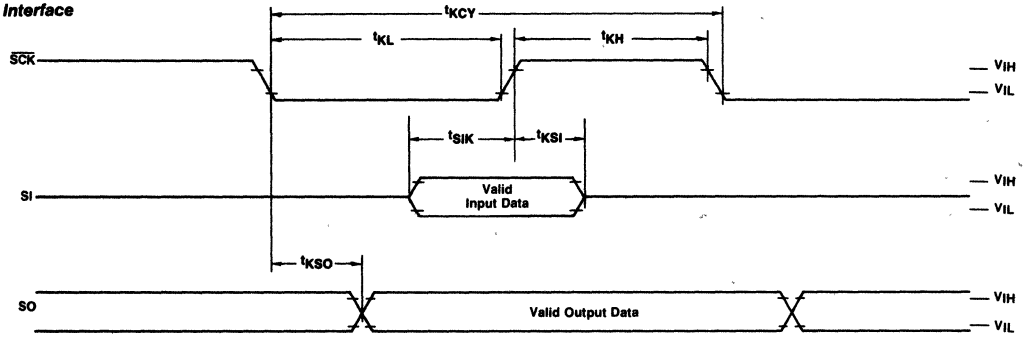
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15	pF	

Timing Waveforms

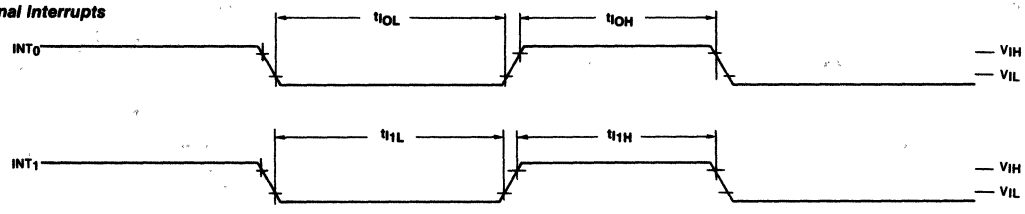
Clocks



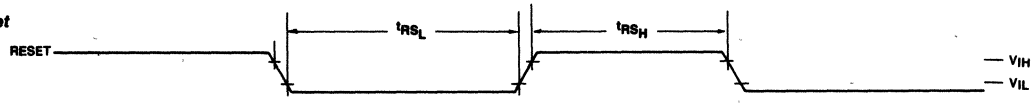
Serial Interface



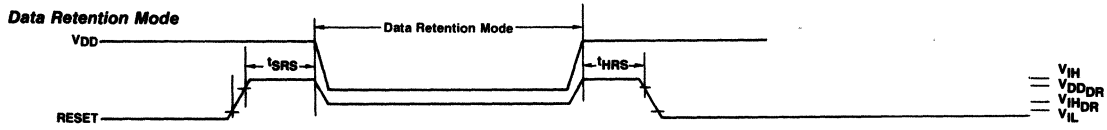
External Interrupts



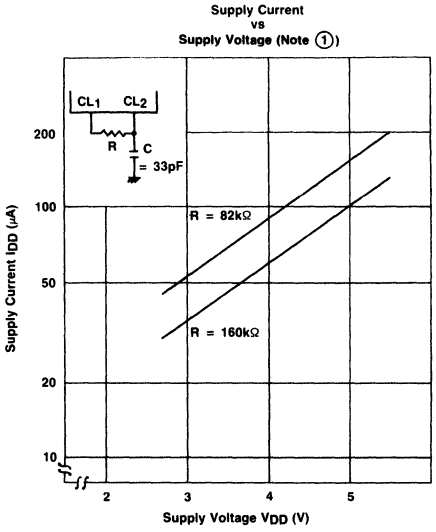
Reset

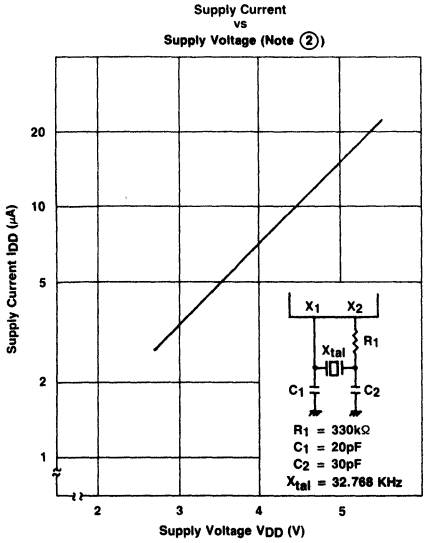


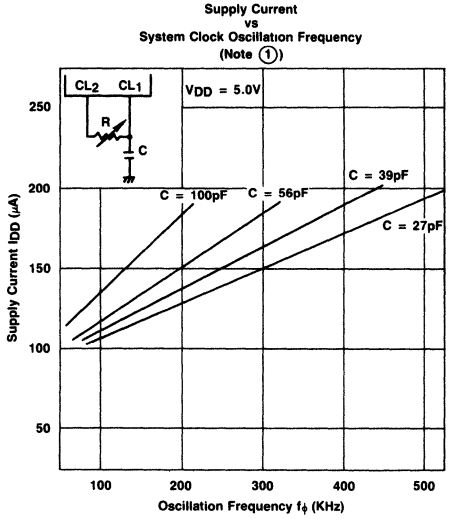
Data Retention Mode

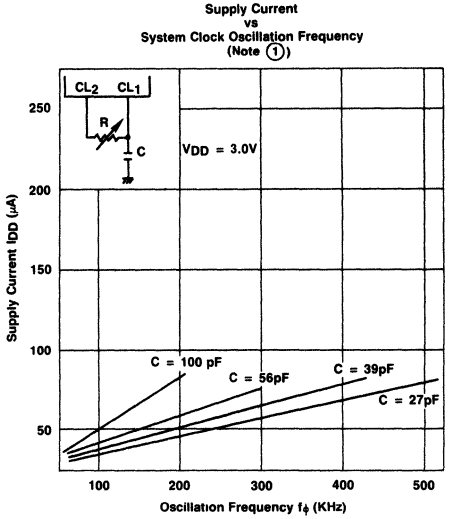


Operating Characteristics (Typical, T_a = 25°C)



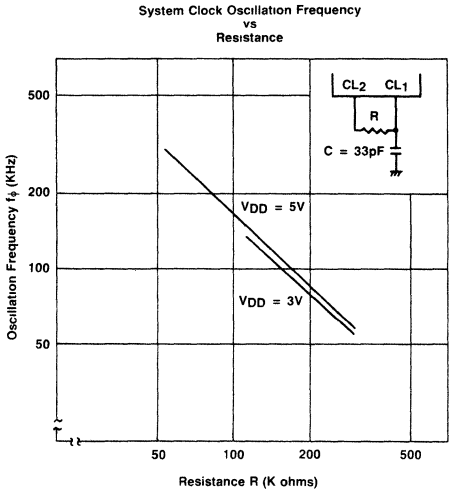


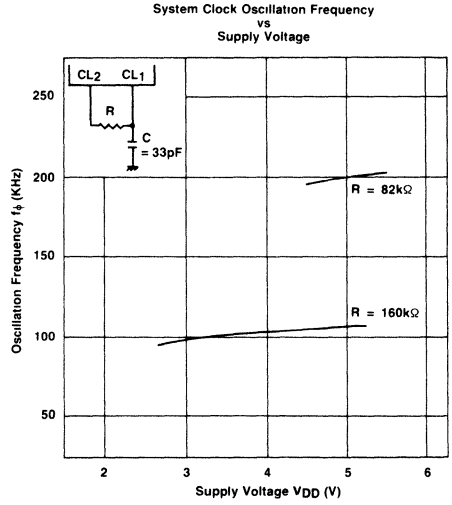




Notes:
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.
② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

Operating Characteristics (Cont.) (Typical, T_a = 25°C)





Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7507SC
Plastic Shrinkdip, μPD7507SCT

μPD7508A CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

Description

The μPD7508A is a CMOS 4-bit single chip microcomputer which has the μPD750x architecture. It is identical to the μPD7508, except for a slightly smaller RAM, and 16 lines of vacuum fluorescent display drive capability.

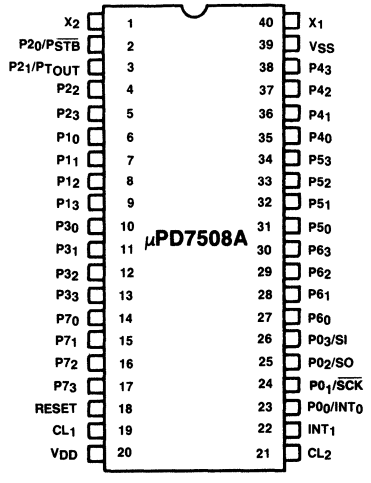
The μPD7508A contains a 4096 x 8-bit ROM, and a 208 x 4-bit RAM.

The μPD7508A contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7508A typically executes 92 instructions of the μPD7500 series "A" instruction set with a 10μs instruction cycle time.

The μPD7508A has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

The μPD7508A provides 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. Ports 3, 4, 5, and 6 are capable of being pulled to −35V in order to drive vacuum fluorescent displays directly. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7508A is available in a 40-pin dual-in-line plastic package.

Pin Configuration



Pin Names

40-Pin DIP	Symbol	Function
1, 40	X_2, X_1	Crystal clock external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
2-5	$P2_0$-$P2_3$ $P2_0$/$\overline{STB}$ $P2_1$/PT_{OUT}	4-bit latched tristate output Port 2 (active high). Line $P2_0$ is also shared with $P\overline{STB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with PT_{OUT}, the timer out F/F signal (active high).
6-9	$P1_0$-$P1_3$	4-bit input/tristate output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0$/$\overline{STB}$ pulse.
10-13	$P3_0$-$P3_3$	4-bit latched tristate output Port 3 (active high).
14-17	$P7_0$-$P7_3$	4-bit input/latched tristate output Port 7 (active high).
18	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
19, 21	CL_1, CL_2	System clock input (active high). Connect 82kΩ resistor across CL_1 and CL_2, and connect 33 pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
20	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
22	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
23-26	$P0_0$/INT_0 $P0_1$/$\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.
27-30	$P6_0$-$P6_3$	4-bit input/latched tristate output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
31-34	$P5_0$-$P5_3$	4-bit input/latched tristate output Port 5 (active high). Can also perform 8-bit parallel I/O conjunction with Port 4.
35-38	$P4_0$-$P4_3$	4-bit input/latched tristate output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
39	V_{SS}	Ground.

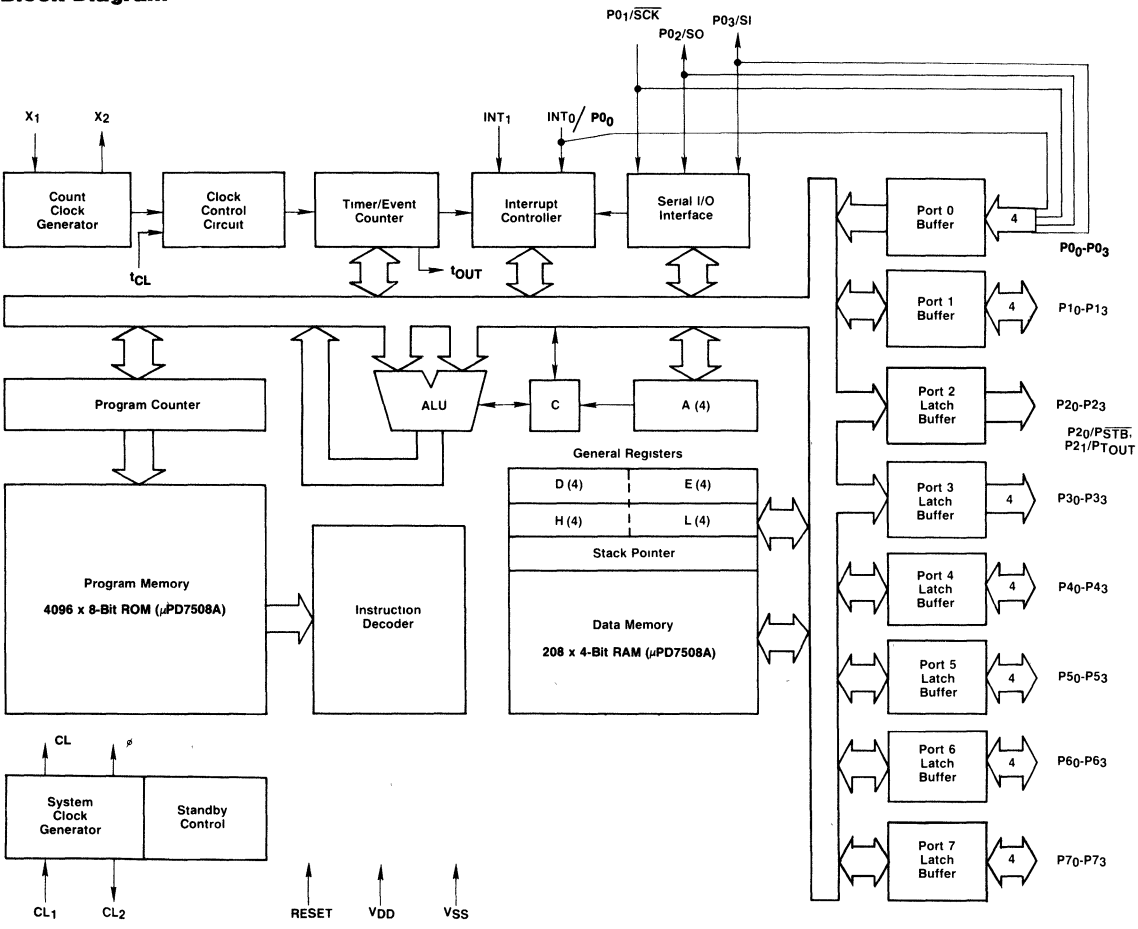
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
Input Voltages, Ports 4, 5, and 6	(V_{DD} − 40.0)V to (V_{DD} + 0.3)V
All Other Input Ports	−0.3V to V_{DD} +0.3V
Output Voltages, Ports 3, 4, 5, and 6	(V_{DD} − 40.0)V to (V_{DD} + 0.3)V
All Other Output Ports	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −150mA
	I_{OL} = 50mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

μPD7508A

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1	
	V_{IH_2}	V_{DD} − 0.5		V_{DD}		CL_1, X_1	
	$V_{IH_{DR}}$	0.9$V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL_1}	0		0.3V_{DD}	V	All Inputs Other than CL_1, X_1, Ports 4, 5, and 6	
	V_{IL_3}	V_{DD} − 35.0		0.3V_{DD}		Ports 4, 5, and 6	
	V_{IL_2}	0		0.5		CL_1, X_1	
Input Leakage Current High	I_{LIH_1}			3	μA	All Inputs Other than CL_1, X_1, Ports 4, 5, and 6	V_I = V_{DD}
	I_{LIH_2}			10		Ports 4, 5, and 6,	V_I = V_{DD}
	I_{LIH_3}			60		CL_1, X_1	
Input Leakage Current Low	I_{LIL_1}			-3	μA	All Inputs Other than CL_1, X_1	V_I = 0V
	I_{LIL_2}			-10		Ports 4, 5, and 6,	V_I = -30.0V
	I_{LIL_3}			-30		CL_1, X_1	
Output Voltage High	V_{OH}	V_{DD} − 2.0			V	V_{DD} = 5V ± 10%, I_{OH} = -1.0mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400μA	
Output Leakage Current High	I_{LOH_1}			3	μA	V_O = V_{DD}	
	I_{LOH_2}			30	μA	Ports 3, 4, 5, and 6,	V_O = -30V
Output Leakage Current Low	I_{LOL_2}			-3	μA	V_O = 0V	
	I_{LOL_2}			-30	μA	Ports 3, 4, 5, and 6,	V_O = -30V
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_1}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			70	300			V_{DD} = 3V ± 10%
	I_{DD_2}		1	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.3	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode, $V_{DD_{DR}}$ = 2.0V	

Capacitance

T_a = 25°C, V_{DD} = 0V

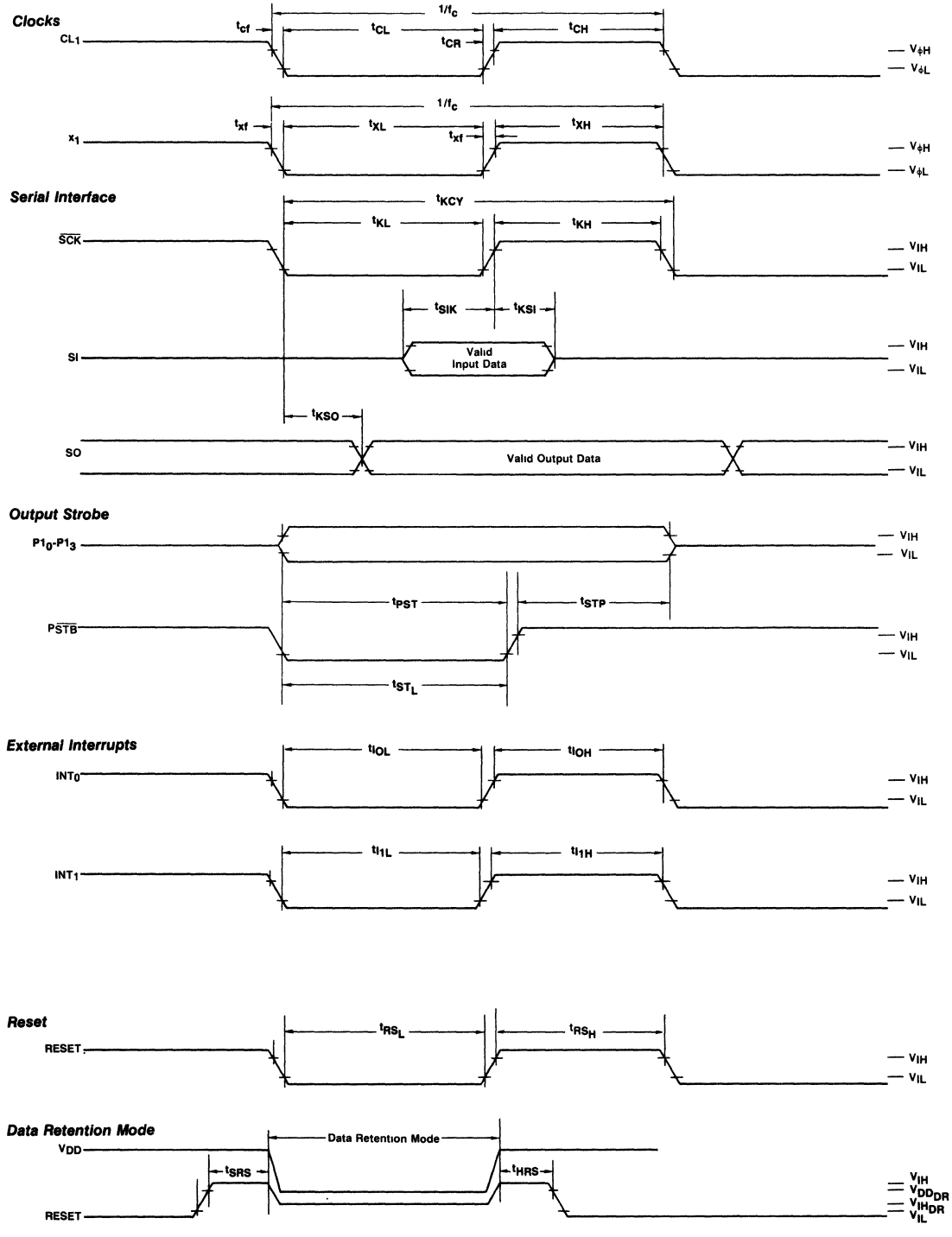
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			20	pF	f = 1MHz,
Output Capacitance	C_O			20	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			20		

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions		
System Clock Oscillation Frequency	f_{CC}	150	200	240	KHz	CL_1, CL_2 R/C Clock	R = 82kΩ ± 2% C = 33pF ± 5%	V_{DD} = 5V ± 10%
		75	100	120			R = 160kΩ ±2% C = 33pF ± 5%	V_{DD} = 3V ± 10%
		75		135				V_{DD} = 2.7V to 5.5V
	f_C	10		410		CL_1, External Clock	V_{DD} = 5V ± 10%	
		10		125			V_{DD} = 2.7V to 5.5V	
System Clock Rise and Fall Times	t_{CR}, t_{CF}			0.2	μs	CL_1, External Clock		
System Clock Pulse Width	t_{CH}, t_{CL}	1.1		50	μs	CL_1, External Clock	V_{DD} = 5V ± 10%	
		3.5		50			V_{DD} = 2.7V to 5.5V	
Counter Clock Oscillation Frequency	f_{XX}	25	32	50	KHz	X_1, X_2 Crystal Oscillator		
	f_X	0		410		X_1, External Pulse Input		V_{DD} = 5V ± 10%
		0		135				V_{DD} = 2.7V to 5.5V
Counter Clock Rise and Fall Times	t_{XR}, t_{XF}			0.2	μs	X_1, External Pulse Input		
Counter Clock Pulse Width	t_{XH}, t_{XL}	1.1			μs	X_1, External Pulse Input		V_{DD} = 5V ± 10%
		3.5						V_{DD} = 2.7V to 5.5V
$\overline{SCK}$ Cycle Time	t_{KCY}	3.0			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%	
		7.0					V_{DD} = 2.7V to 5.5V	
		5.0				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%	
		14.0					V_{DD} = 2.7V to 5.5V	
$\overline{SCK}$ Pulse Width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ is an input	V_{DD} = 5V ± 10%	
		3.3					V_{DD} = 2.7V to 5.5V	
		2.2				$\overline{SCK}$ is an output	V_{DD} = 5V ± 10%	
		6.5					V_{DD} = 2.7V to 5.5V	
SI Setup Time to $\overline{SCK}$↑	t_{SIK}	.3			μs			
SI Hold Time after $\overline{SCK}$↑	t_{KSI}	.45			μs			
SO Delay Time after $\overline{SCK}$↓	t_{KSO}			850	ns	V_{DD} = 5V ±		
				1200		V_{DD} = 2.7V to 5.5V		
Port 1 Output Setup Time to P_{STB}↑	t_{PST}	$1/(2f_c$-800)			ns	V_{DD} = 5V ± 10%		
		$1/(2f_c$-2000)				V_{DD} = 2.7V to 5.5V		
Port 1 Output Hold Time after P_{STB}↑	t_{STP}	100			ns	V_{DD} = 5V ± 10%		
		100				V_{DD} = 2.7V to 5.5V		
P_{STB} Pulse Width	t_{SL}	$1(2f_c$-800)			ns	V_{DD} = 5V ± 10%		
		$1/(2f_c$-2000)				V_{DD} = 2.7V to 5.5V		
INT_0 Pulse Width	t_{I0H}, t_{I0L}	10			μs			
INT_1 Pulse Width	t_{I1H}, t_{I1L}	$2/f_c$			μs			
RESET Pulse Width	t_{RSH}, t_{RSL}	10			μs			

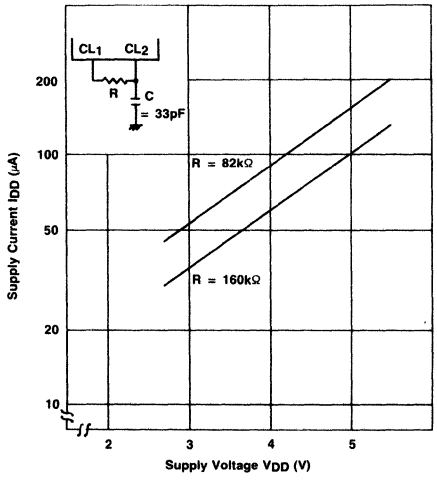
Timing Waveforms



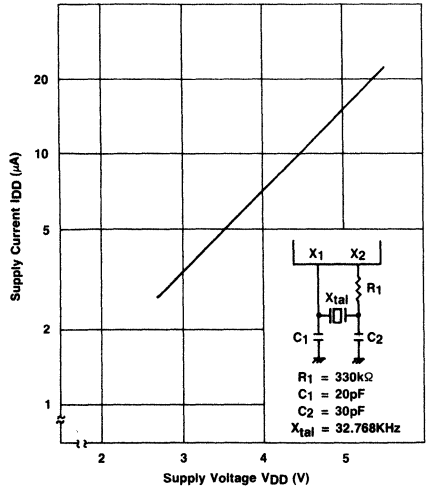
Operating Characteristics

Typical, T_a = 25°C

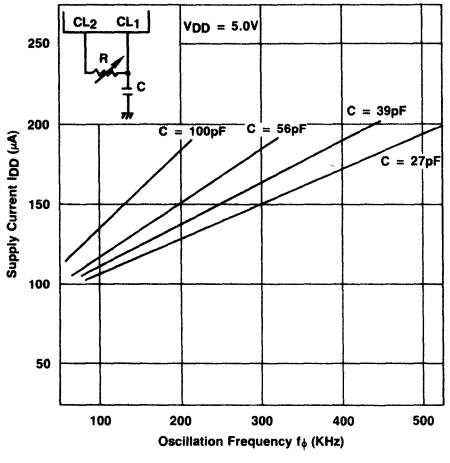
Supply Current vs Supply Voltage (Note ①)



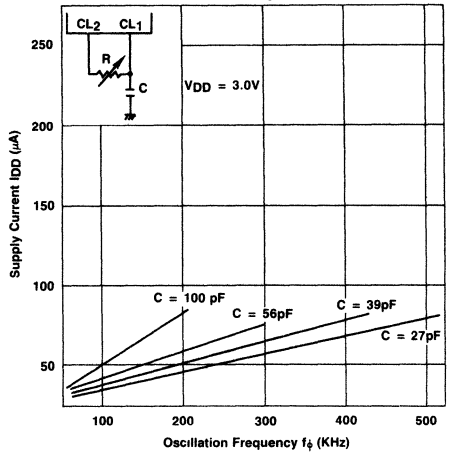
Supply Current vs Supply Voltage (Note ②)



Supply Current vs System Clock Oscillation Frequency (Note ①)



Supply Current vs System Clock Oscillation Frequency (Note ①)



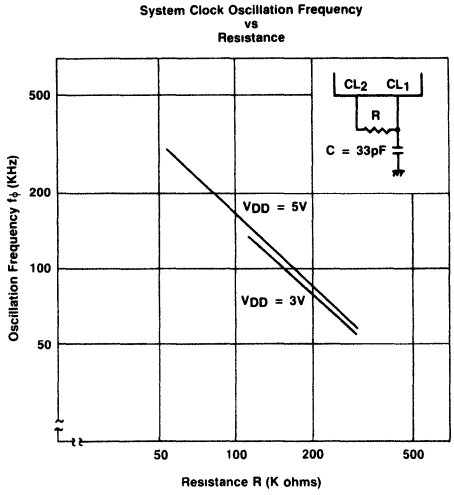
Notes:

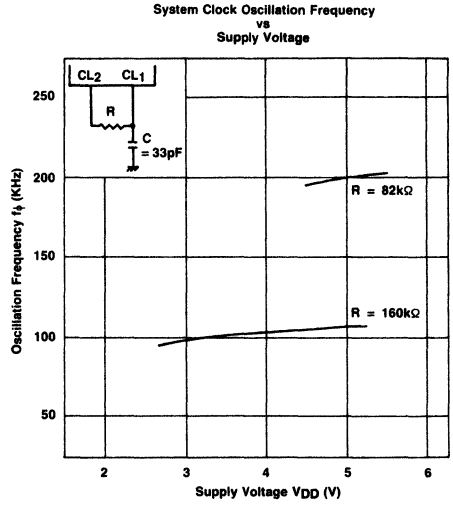
① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active.

② Only crystal oscillator clock is operating and consuming power. All other internal logic blocks are not active.

Operating Characteristics (Cont.)

Typical, T_a = 25°C





3

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7508AC
Plastic Shrinkdip, μPD7508ACU
Ceramic Piggyback, μPD75CG08E

NEC

PRELIMINARY

μPD7508H HIGH SPEED CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

Description

The μPD7508H is a high-speed CMOS 4-bit single chip microcomputer which is based upon the μPD7500 series architecture.

The μPD7508H contains a 4096 x 8-bit ROM, and a 224 x 4-bit RAM. It contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7508H typically executes 92 instructions of the μPD7500 series "A" instruction set with 4μs instruction cycle time.

The μPD7508H has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

The μPD7508H provides 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit input Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. It is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7508H is available in a 40-pin dual-in-line plastic package. The μPD7508H is downward compatible with the μPD7508 and the μPD7507. The μPD7508H is ideally suited as a controller in the following applications:

- ☐ telephone/telecommunication equipment
- ☐ portable instruments
- ☐ automotive dashboard controls
- ☐ medical instruments
- ☐ portable and hand-held computer terminals
- ☐ office equipment

Development Tools

For software development, editing, debugging, and assembly into object code, you can use the NEC Development System (NDS). Additionally, for systems supporting either the ISIS-II (®Intel Corp.), CP/M (®Digital Research Corp.) operating systems, or Fortran IV ANSI 1966 V3.9, the ASM75 Cross-Assembler is available.

During software development, the code can be completely evaluated and debugged with hardware by the Evakit-7500 Evaluation Board. The Evakit-7500-RTT Real-Time Tracer Board is an optional device used to examine operation of your code in the actual prototype circuit. The SE-7508 System Emulation Board will emulate complete functionality of the μPD7508H for demonstrating your final system design. All of these boards take advantage of the capabilities of the μPD7500 ROM-less evaluation chip to perform their tasks.

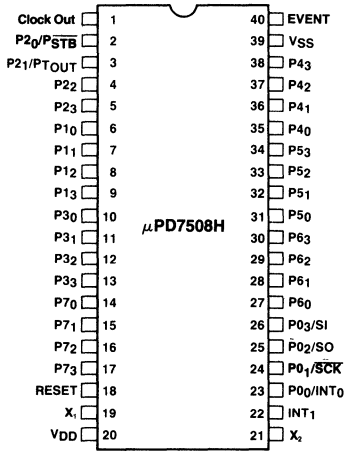
Complete operation details on the μPD7508H CMOS 4-bit Microcomputer can be found in the μPD7506, μPD7507, and μPD7508 CMOS 4-bit Microcomputers Technical Manual.

Features

- ☐ Advanced 4th Generation Architecture
- ☐ Program Memory (ROM) size: 4K x 8-bit bytes
- ☐ Data Memory (RAM) size: 224 x 4-bit nibbles
- ☐ RAM Stack
- ☐ Four General Purpose Registers: D, E, H, and L
  - – Can address Data Memory and I/O ports
  - – Can be stored to or retrieved from Stack
- ☐ 92 Powerful Instructions, including
  - – Direct/indirect addressing
  - – Table look-up
  - – RAM stack push/pop
  - – Single byte subroutine calls
  - – RAM and I/O port single bit manipulation
  - – Accumulator and I/O port logical operations
  - – 4μs instruction cycle time, typically
- ☐ Extensive General Purpose I/O Capability
  - – One 4-bit input port
  - – Two 4-bit latched tri-state output ports
  - – Five 4-bit input/latched tri-state output ports
  - – Easily expandable with μPD82C43 CMOS I/O expander
  - – 8-bit parallel I/O capacity
- ☐ Hardware Logic Blocks – Reduce Software Requirements
  - – Operation completely transparent to instruction execution
  - – 8-bit Timer/Event counter
    - Binary-up counter generates INT_T at coincidence
    - Accurate Crystal Clock or External Event operation possible
  - – Vectored, Prioritized Interrupt Controller
    - Three external interrupts (INT_0, INT_1, INT_2)
    - Two internal interrupts (INT_T, INT_S)
  - – 8-bit Serial Interface
    - 3-line I/O configuration generates INT_S upon transmission of eighth bit
    - Ideal for distributed intelligence systems or communication with peripheral devices
  - – Complete operation possible in HALT and STOP power-down modes
- ☐ Built-in System Clock Generator
- ☐ Built-in Schmidt-Trigger RESET Circuitry
- ☐ Single Power Supply, Variable from 2.7V to 5.5V
- ☐ Low Power Consumption Silicon Gate CMOS Technology
  - – 900μA max at 5V, 400μA max at 3V
  - – HALT, STOP power-down instructions reduce power consumption to 20μA max at 5V, 10μA at 3V (Stop Mode)
- ☐ Extended −40°C to +85°C Temperature Range Available
- ☐ 40-pin Dual-in-line Plastic Package

3

Pin Configuration



Absolute Maximum Ratings*

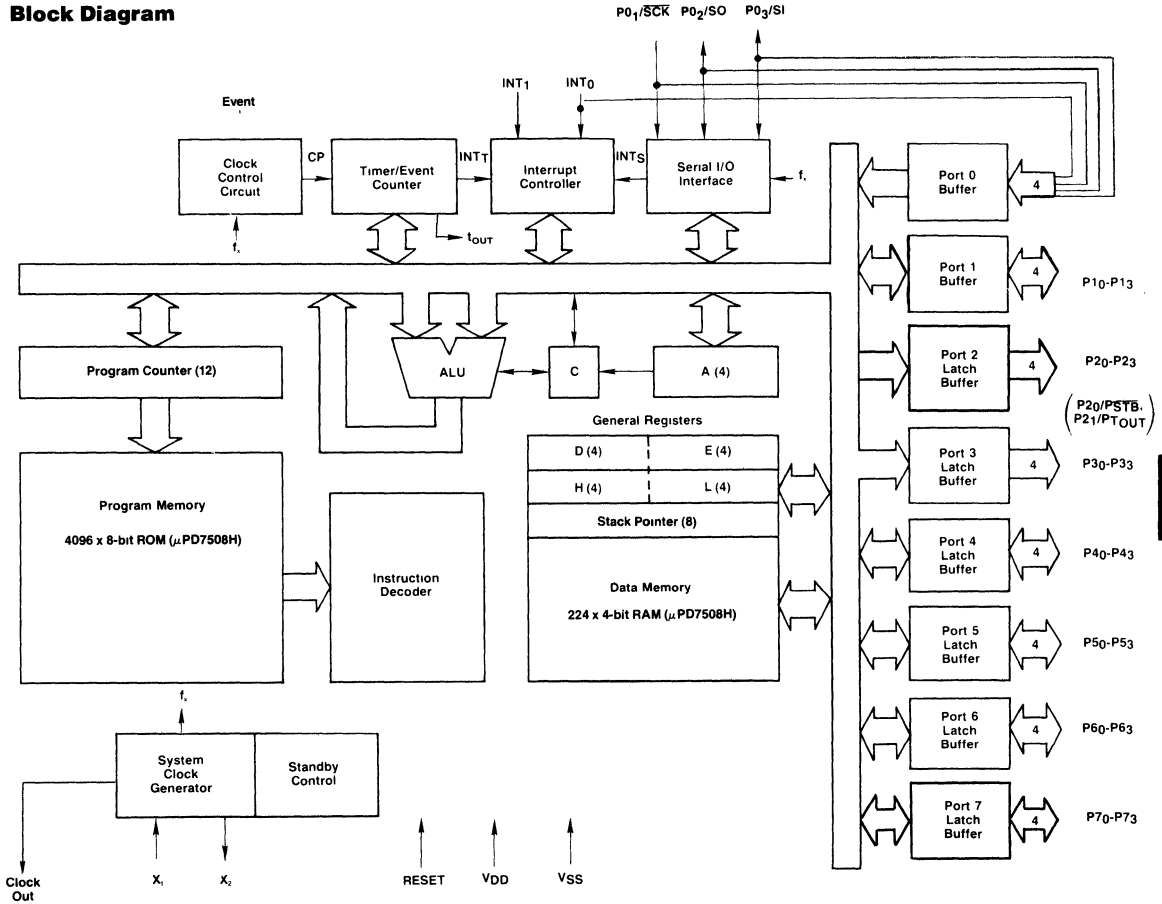
T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} + 0.3V
Output Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 30mA

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Identification

Pin No.	Symbol	Function
1	Clock Out	Crystal Clock Output (active high) The Crystal Oscillator frequency is divided by 12, and then output through a buffer
2-5	$P2_0$-$P2_3$ $P2_0/P_{STB}$ $P2_1/P_{TOUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_0$ is also shared with P_{STB}, the Port 1 output strobe pulse (active low). Line P2, is also shared with P_{TOUT}, the timer-out F/F signal (active high).
6-9	$P1_0$-$P1_3$	4-bit input/tri-state output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0/P_{STB}$ pulse.
10-13	$P3_0$-$P3_3$	4-bit input/latched tri-state output Port 3 (active high).
14-17	$P7_0$-$P7_3$	4-bit input/latched tri-state output Port 7 (active high).
18	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7507 or μPD7508 after power-up.
19,21	X_1, X_2	Crystal Clock Oscillator input (active high). Connect a 4.19MHz crystal across X_1, and X_2.
20	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
22	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
23-26	$P0_0/INT_0$ $P0_1/\overline{SCK}$ $P0_2/SO$ $P0_3/SI$	4-bit input Port 0/Serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock SCK (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface Line $P0_0$ is always shared with external interrupt INT_0 (active high) which is a rising edge-triggered interrupt.
27-30	$P6_0$-$P6_3$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
31-34	$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
35-38	$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
39	V_{SS}	Ground.
40	EVENT	EVENT counter pulse input (active high)

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than X_1	
	V_{IH_2}	V_{DD} − 0.5		V_{DD}		X_1	
	V_{IH_3}	0.9 $V_{DD_{DR}}$		$V_{DD_{DR}}$ + 0.2		RESET, Data Retention Mode	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	All Inputs Other than X_1	
	V_{IL_2}	0		0.5		X_1	
Input Leakage Current High	I_{LI_H}			3	μA	All Inputs Other than X_1	$V_I = V_{DD}$
	I_{IH_2}			10		X_1	
Input Leakage Current Low	I_{LI_L}			−3	μA	All Inputs Other than X_1	V_I = 0V
	I_{IL_2}			−10		X_1	
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 10%, I_{OH} = −1.0 mA	
		V_{DD} − 0.5				V_{DD} = 2.7V to 5.5V, I_{OH} = −100 μA	
Output Voltage Low	V_{OL}			0.4	V	V_{DD} = 5V ± 10%, I_{OL} = 1.6 mA	
				0.5		V_{DD} = 2.7V to 5.5V, I_{OL} = 400 μA	
Output Leakage Current High	I_{LO_H}			3	μA	$V_O = V_{DD}$	
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V	
Supply Voltage	$V_{DD_{DR}}$	2.0			V	Data Retention Mode	
Supply Current	I_{DD_1}		300	900	μA	Normal Operation	V_{DD} = 5V ± 10%
			150	400			V_{DD} = 3V ± 10%
	I_{DD_2}		2	20		Stop Mode, X_1 = 0V	V_{DD} = 5V ± 10%
			0.5	10			V_{DD} = 3V ± 10%
	$I_{DD_{DR}}$		0.4	10		Data Retention Mode	$V_{DD_{DR}}$ = 2.0V

AC Characteristics

T_a = −10°C to +70°C, V_{DD} = 2.7V to 5.5V

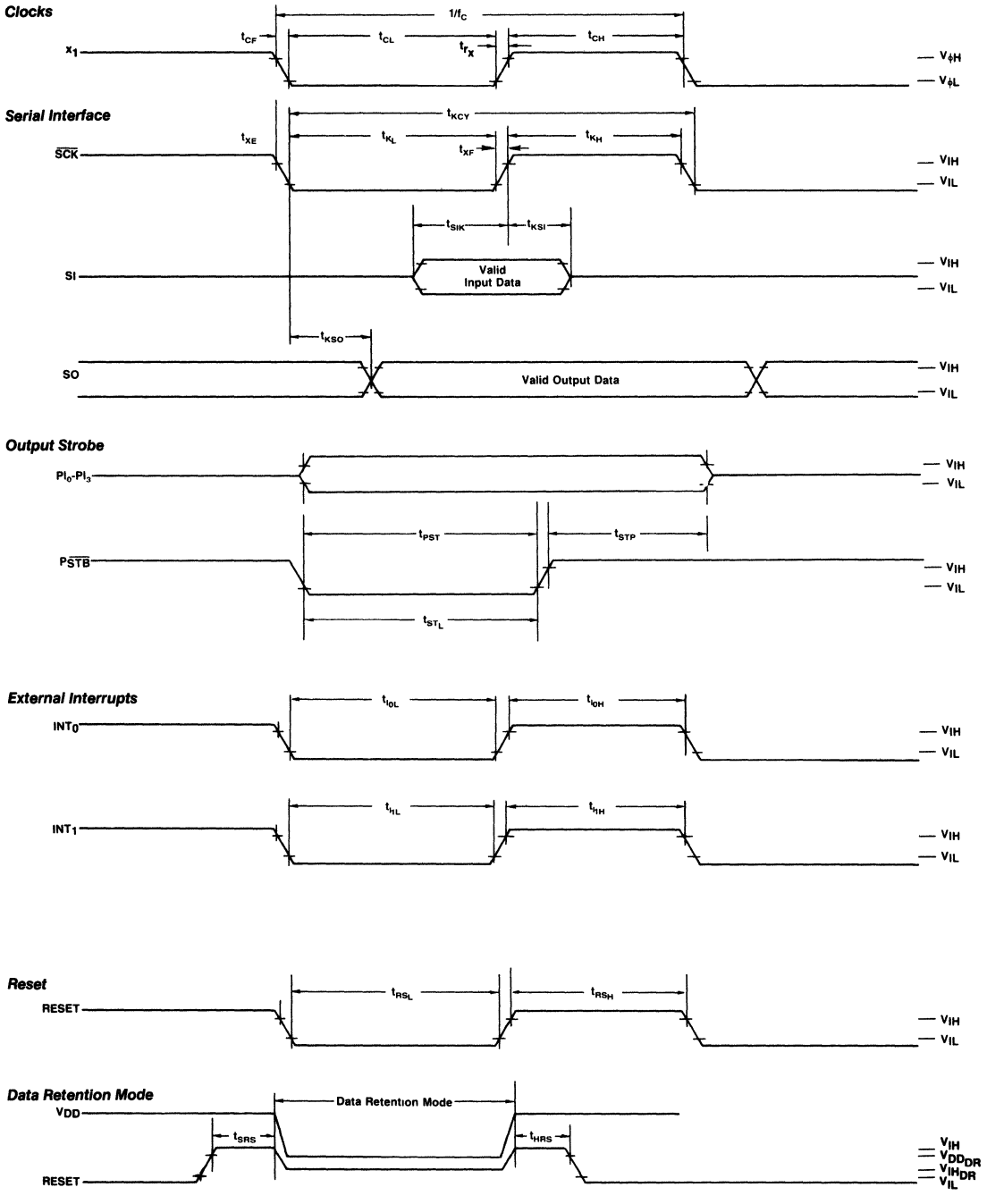
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
System Clock Oscillation Frequency	f_{CC}	120	TBD	TBD	KHz	X_1, X_2 R = 120 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 5V ± 10%
		60	TBD	TBD		R = 250 kΩ ± 2% C = 33 pF ± 5%	V_{DD} = 3V ± 10%
		60		TBD			V_{DD} = 2.7V to 5.5V
	f_C	10	TBD	TBD		X_1, External Clock	V_{DD} = 5V ± 10%
		10		TBD			V_{DD} = 2.7V to 5.5V
EVENT Frequency	f_x	25	32	50	KHz	X_1, X_2 Crystal Oscillator	
	f_{EVENT}	0		300		EVENT	V_{DD} = 5V ± 10%
		0		135			V_{DD} = 2.7V to 5.5V
EVENT Rise and Fall Times	t_{CR}, t_{CF}			0.2	μs	EVENT	
EVENT Pulse Width	t_{XH}, t_{XL}	1.5			μs	EVENT	V_{DD} = 5V ± 10%
		3.5					V_{DD} = 2.7V to 5.5V
SCK Cycle Time	t_{KCY}	4.0			μs	SCK is an input	V_{DD} = 5V ± 10%
		7.0					V_{DD} = 2.7V to 5.5V
		6.7				SCK is an output	V_{DD} = 5V ± 10%
		14.0					V_{DD} = 2.7V to 5.5V
SCK Pulse Width	t_{KH}, t_{KL}	1.8			μs	SCK is an input	V_{DD} = 5V ± 10%
		3.3					V_{DD} = 2.7V to 5.5V
		3.0				SCK is an output	V_{DD} = 5V ± 10%
		6.5					V_{DD} = 2.7V to 5.5V
SI Setup Time to SCK ↑	t_{SIK}	300			ns		
SI Hold Time after SCK ↑	t_{KSI}	450			ns		
SO Delay Time after SCK ↓	t_{KSO}			850	ns	V_{DD} = 5V ± 10%	
				1200		V_{DD} = 2.7V to 5.5V	
Port 1 Output Setup Time to P_{STB} ↑	t_{PST}	$1/(2f_\phi$-800)			ns	V_{DD} = 5V ± 10%	
		$1/(2f_\phi$-2000)				V_{DD} = 2.7V to 5.5V	
Port 1 Output Hold Time after P_{STB} ↑	t_{STP}	300	350	500	ns	V_{DD} = 5V ± 10%	
		300		1500		V_{DD} = 2.7V to 5.5V	
P_{STB} Pulse Width	t_{SW_L}	$f/(2f_\phi$-800)			ns	V_{DD} = 5V ± 10%	
		$f/(2f_\phi$-2000)				V_{DD} = 2.7V to 5.5V	
INT_0 Pulse Width	t_{I0H}, t_{I0L}	10			μs		
INT_1 Pulse Width	t_{I1W_H}, t_{I1W_L}	$2/f_\phi$			μs		
RESET Pulse Width	t_{RS_H}, t_{RS_L}	10			μs		

Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to V_{SS}
Input/Output Capacitance	$C_{I/O}$			15	pF	

Timing Waveforms



3

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7508HC

Plastic Shrinkdip, μPD7508HCU

μPD7514
CMOS 4-BIT SINGLE CHIP MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

Description

The μPD7514 CMOS 4-bit single chip microcomputer has the standard μPD750X architecture. It contains 4K x 8-bits of program memory ROM, 256 x 4-bits of data memory RAM, an 8-bit timer/event counter, and an 8-bit serial interface.

The on-chip LCD controller/driver is capable of driving a variety of LCD displays configured from biplexed to quad-riplexed (2–4 backplane). It can utilize up to 32 segment and 4 common drive lines that are output from a 128-bit (32 x 4) display data memory.

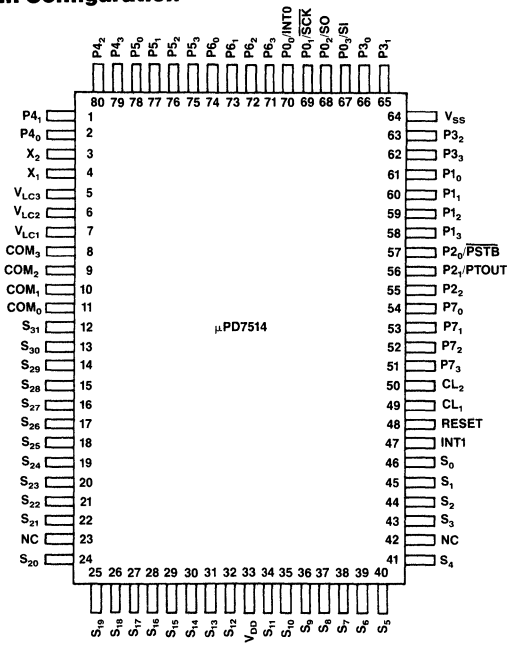
The μPD7514 also features 4 vectored interrupts (2 internal and 2 external) and 2 standby modes. It is available in the 80-pin plastic flat package to conserve space and is manufactured with a low power consumption CMOS process allowing the use of a single 5V power supply. A powerful 92 instruction set (subset of μPD750X Instruction Set A) allows greater software flexibility.

The μPD7514 is capable of forming a system with a minimum amount of additional circuitry. It is designed to operate with low power and can be used for a wide variety of applications because the chip can generate a reference clock for timer operations.

Features

- ☐ 4-bit single chip microcomputer
- ☐ 92 instructions (subset of μPD7500 set A)
- ☐ Instruction cycle: 5μs/400kHz at 5V
- ☐ Program memory (ROM): 4096 x 8 bits
- ☐ Data memory (RAM): 256 x 4 bits
- ☐ Vectored interrupts: 2 externals, 2 internals
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ On-chip LCD controller/driver
  - 1/2 bias: biplexed, triplexed
  - 1/3 bias: triplexed, quadriplexed
  - Segment outputs: 32 lines
  - Common outputs: 4 lines
- ☐ Standby modes (stop/halt)
- ☐ Low-power data retention capability
- ☐ 31 I/O lines
- ☐ On-chip RC oscillator for system clock
- ☐ On-chip crystal oscillator for count clock
- ☐ CMOS technology
- ☐ Single power supply
- ☐ 80-pin plastic flat package

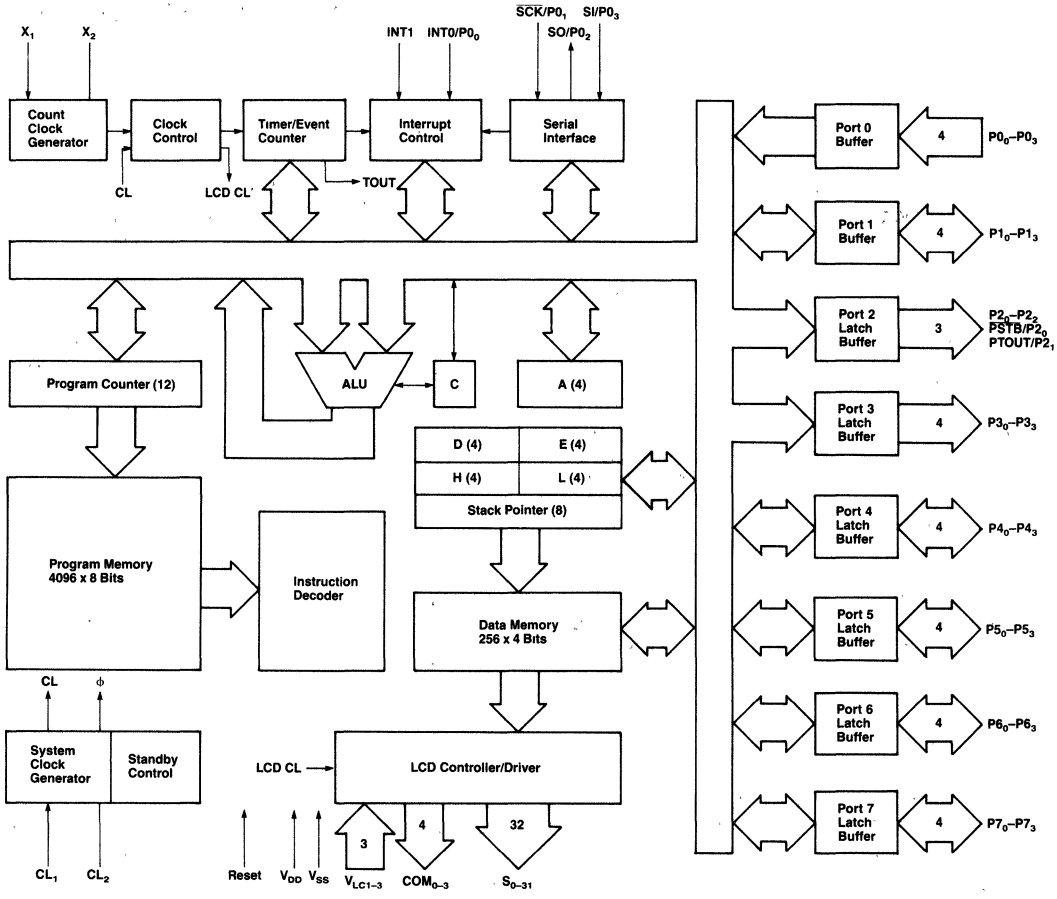
Pin Configuration



Pin Identification

Pin No.	Symbol		Function
1, 2, 79, 80	$P4_0$–$P4_3$	I/O	I/O pins (4 bits) of Port 4 (4-bit I/O port).
3, 4	X_1, X_2		Count Clock Oscillation pins to be connected to crystal. X_1 is for External Clock input.
5–7	V_{LC1}–V_{LC3}		LCD bias voltage supply input pins.
8–11	COM_0–COM_3		LCD common signal output pins.
12–22, 24–32, 34–41, 43–46	S_0–S_{31}		LCD segment signal output pins.
33	V_{DD}		Power supply positive.
47	INT1		External interrupt input pin.
48	RESET		Reset input pin.
49, 50	CL_1, CL_2		System Clock Oscillation pins to be connected to RC. CL_1 is for External Clock input.
51–54	$P7_0$–$P7_3$	I/O	I/O pins (4 bits) of Port 7 (4-bit I/O port).
55 56 57	$P2_2$ $P2_1$/PTOUT $P2_0$/PSTB		Output pins (3 bits) of Port 2 (3-bit output port). Commonly used as Strobe output (PSTB) for Port 1 output, TOUT output (PTOUT).
58–61	$P1_0$–$P1_3$	I/O	I/O pins (4 bits) of Port 1 (4-bit I/O port), not including latches.
62, 63, 65, 66	$P3_0$–$P3_3$		Output pins (4 bits) of Port 3 (4-bit output port).
64	V_{SS}		Ground.
67 68 69 70	$P0_3$/SI $P0_2$/SO $P0_1$/SCK $P0_0$/INT0	 I/O I/O 	Input pins (4 bits) of Port 0 (4-bit input port). Commonly used as interrupt Request input (INT0), Serial Clock I/O (SCK), Serial Data input (SI), Serial Data output (SO).
71–74	$P6_0$–$P6_3$	I/O	I/O pins (4 bits) of Port 6 (programmable 4-bit I/O port).
75–78	$P5_0$–$P5_3$	I/O	I/O pins (4 bits) of Port 5 (4-bit I/O port).

Block Diagram

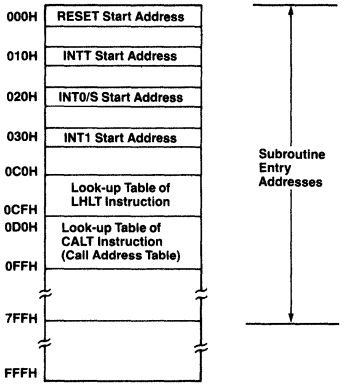


Program Memory (ROM)

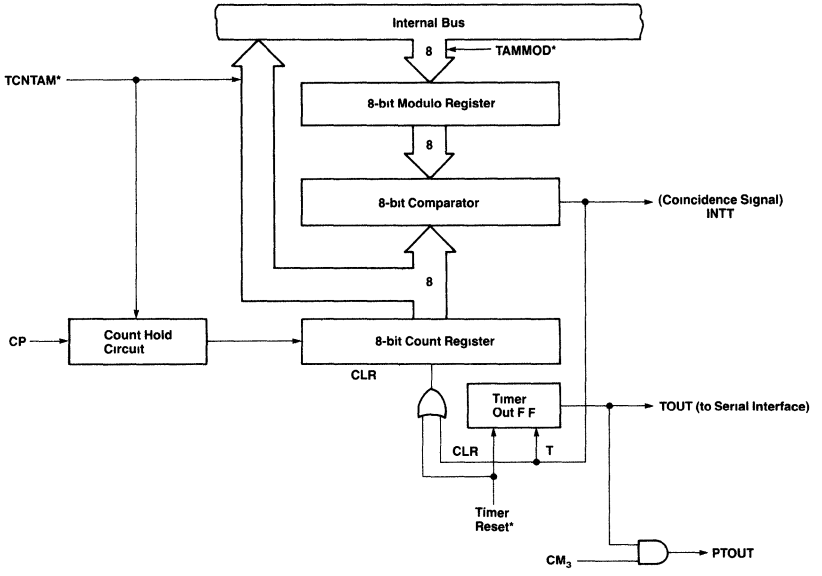
Program Memory is a mask-programmable ROM of 4096-word x 8-bit configuration, and is addressed by the program counter. Program Memory stores programs and table data.

The address locations of the program memory are from 000H to FFFH. RESET, Interrupt, start address, and the table areas of LHLT and CALT instructions have been allocated specific memory locations. When a program is generated, the aforementioned memory locations must be taken into consideration.

Program Memory Map



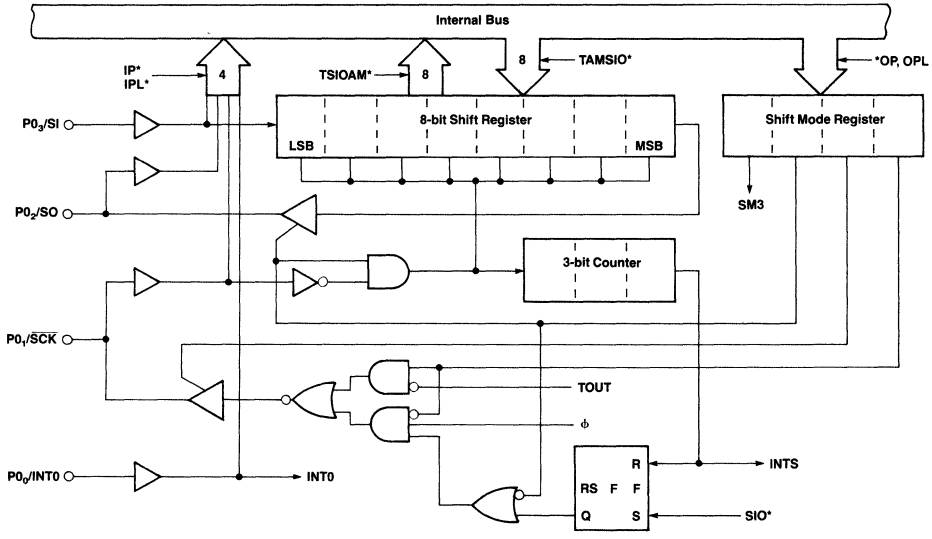
Timer/Event Counter Configuration



Notes: ① CP is a count pulse selected by the clock mode register
② CM_3 is used for output designation of the time-out F/F
③ * indicates execution of instruction

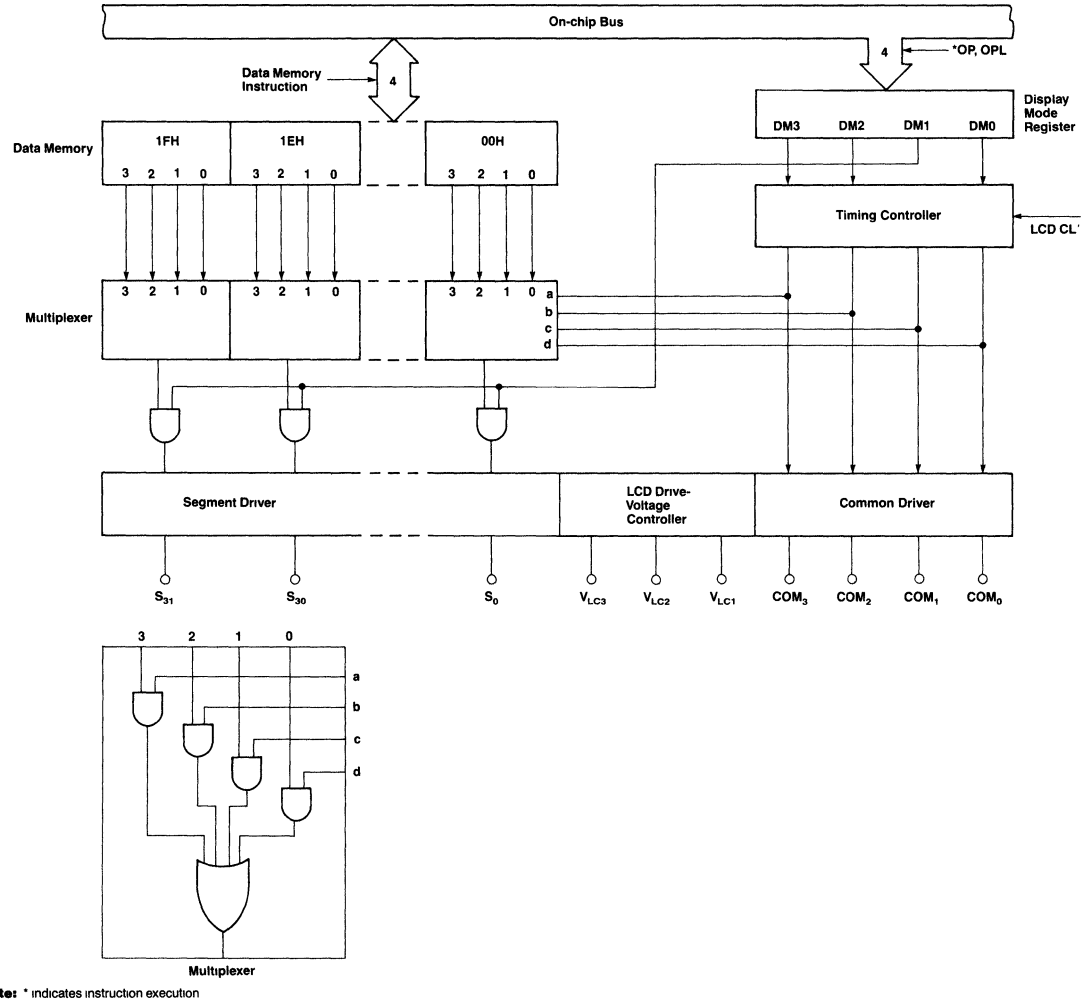
Serial interface is used to input/output serial data and is basically composed of an 8-bit shift register, a 4-bit shift mode register and a 3-bit counter.

Serial Interface Block Diagram



Notes: ① ϕ indicates the internal clock signal (system clock)
② TOUT is the timer-out F/F signal
③ * indicates the execution of instruction
④ SM3 is to the interrupt controller

LCD Controller/Driver Block Diagram



Note: * indicates instruction execution

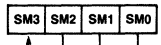
The LCD controller/driver consists of a 4-bit display mode register (DM0 – DM3), 128-bit (32 x 4) display data memory (i.e., addresses from 00H to 1FH in data memory), a timing controller, multiplexers, an LCD drive-voltage controller, segment drivers, and common drivers.

The LCD controller/driver provides an LCD direct drive function with 1/2 bias voltage (biplexed, triplexed) and 1/3 bias voltage (triplexed, quadriplexed) configurations. For LCD driver outputs, 32 segment lines ($S_0 - S_{31}$) and 4 common lines ($COM_0 - COM_3$) are provided.

Maximum Segment Number

Bias	Multiplexing	COM Lines	Maximum Segment Number
1/2	Biplexed	COM_0, COM_1	64 (32 Segments x 2 Commons)
	Triplexed	COM_0, COM_1, COM_2	96 (32 Segments x 3 Commons)
1/3	Triplexed		
	Quadriplexed	COM_0, COM_1, COM_2, COM_3,	128 (32 Segments x 4 Commons)

Format of Shift Mode Register



Serial Interface Operation and Mode Setting of Port 0

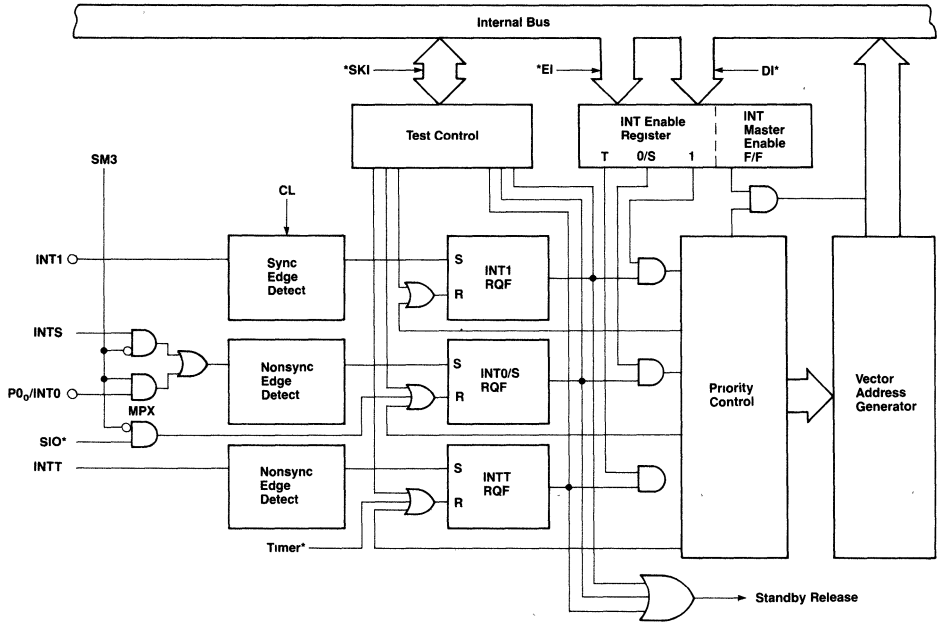
SM2	SM1	SM0	$P0_3$/SI	$P0_2$/SO	$P0_1$/$\overline{SCK}$	Serial Operation
0	0	0	Port Input	Port Input	Port Input	Stop
0	1	0			To output ϕ continuously	
0	1	1			To output TOUT continuously	
1	0	0	SI Input	SO Output	$\overline{SCK}$ Input	To operate with external clock
1	1	0			$\overline{SCK}$ Output (ϕ x 8)	To operate with ϕ
1	1	1			$\overline{SCK}$ Output (TOUT)	To operate with TOUT

Selection of INT0 or INTS

SM3	Interrupt Source
0	INTS
1	INT0

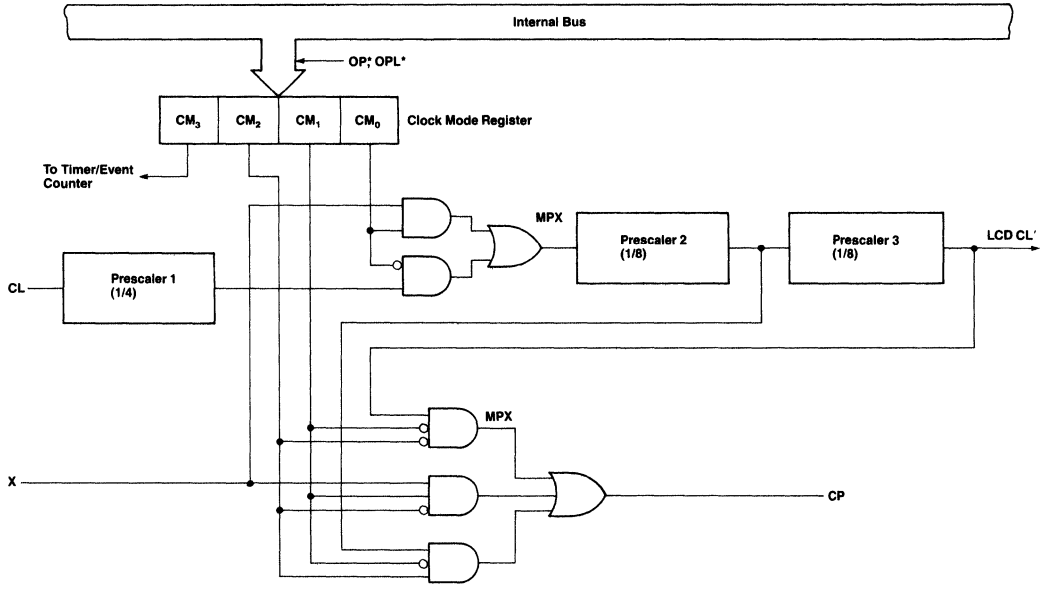
Note: ϕ = System Clock

Interrupt Controller Block Diagram



Notes: ① * indicates execution of instruction
② SM3 is bit 3 of the shift mode register (Selection of INT0 or INTS)

Clock Control Circuit



Package Outlines

For information, see Package Outline Section 7.

Plastic Miniflat, μPD7514G

Notes

μPD7519
CMOS 4-BIT SINGLE-CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY CONTROLLER/DRIVER

Description

The μPD7519 is a CMOS 4-bit single-chip microcomputer which has the μPD750x architecture.

The μPD7519 contains a 4096 x 8-bit ROM, and a 256 x 4-bit RAM.

The μPD7519 contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7519 typically executes 106 instructions of the μPD7500 series A instruction set with a 7.637μs instruction cycle time.

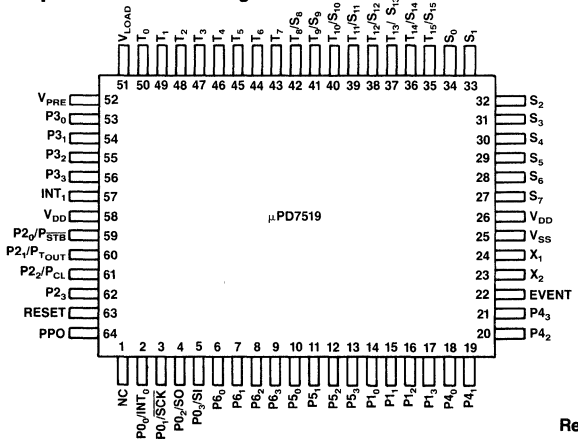
The μPD7519 has two external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter, an 8-bit serial interface, and a 9-bit D/A programmable pulse generator, to help reduce software requirements. The on-board vacuum fluorescent display controller/driver supervises all of the timing required by the 24 Port S segment drivers either for a 16-digit 7-segment vacuum fluorescent display, or for an 8-character 14-segment vacuum fluorescent display.

The μPD7519 provides 28 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, and 6. Additionally, Port 1 can be automatically expanded to 16 I/O lines through connection to a μPD82C43. The μPD7519 is manufactured with a low power consumption CMOS process, allowing the use of a single power supply between 2.5V and 5.5V. Current consumption is less than 2mA maximum, and can be lowered much further in the Halt and Stop power-down modes. The μPD7519 is available in a space-saving 64-pin flat plastic package, or a 64-pin QUIL package.

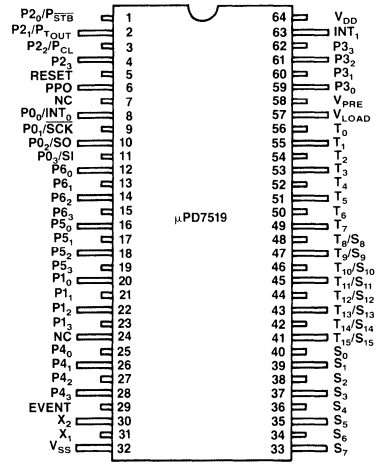
There is also a piggyback EPROM version available, the 75CG19E, which is pin-compatible and functionally equivalent to the masked version. It is excellent for prototyping and program development.

Pin Configuration

64-pin Plastic Flat Package



64-pin Plastic QUIL Package



Pin Identification

Pin Nos. Flat	Pin Nos. QUIL	Symbol	Description
1	7, 24	NC	No connection
2 3 4 5	8 9 10 11	$P0_0/\overline{INT_0}$ $P0_1/\overline{SCK}$ $P0_2/SO$ $P0_3/SI$	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active high), and the Serial Clock SCK (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt $\overline{INT_0}$, which is a rising edge-triggered interrupt.
6–9	12–15	$P6_0$–$P6_3$	4-bit input/latched three-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
10–13	16–19	$P5_0$–$P5_3$	4-bit input/latched three-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
14–17	20–23	$P1_0$–$P1_3$	4-bit input/latched three-state output Port 1 (active high).
18–21	25–28	$P4_0$–$P4_3$	4-bit input/latched three-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
22	29	EVENT	1-bit external event input for timer/event counter (active high).
23–24	30–31	X_2, X_1	Crystal clock input (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for system clock operation. Alternatively, an external clock source may be connected to input X_1 while output X_2 is left open.
25	32	V_{SS}	Ground.
26, 58	64	V_{DD}	Power supply positive. Apply single voltage ranging from 2.5V to 5.5V for proper operation.
27–34 35–42 43–50	33–40 41–48 49–56	S_0–S_7 T_8/S_8–T_{15}/S_{15} T_0–T_7	Vacuum fluorescent display outputs (active high). S_0–S_7 are always segment driver outputs, and T_0–T_7 are always digit driver outputs. T_8/S_8–T_{15}/S_{15} can be configured as either segment driver outputs or as digit driver outputs under control of the display mode select register.

Pin Identification (Cont.)

Pin Nos. Flat	Pin Nos. QUIL	Symbol	Description
51	57	V_{LOAD}	Vacuum fluorescent display power supply negative. Apply single voltage between $V_{DD}-35.0$ and V_{DD} for proper display operation.
52	58	V_{PRE}	Power supply for VFD driver.
53–56	59–62	$P3_0$–$P3_3$	4-bit latched three-state output Port 3 (active high).
57	63	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
59	1	$P2_0/P_{\overline{STB}}$	4-bit latched output Port 2 (active high). Line $P2_0$ is also shared with $P_{\overline{STB}}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with $P_{T_{OUT}}$, the timer-out F/F signal (active high).
60	2	$P2_1/P_{T_{OUT}}$	
61	3	$P2_2/P_{CL}$	Internal system clock output.
62	4	$P2_3$	General purpose output.
63	5	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7502 or μPD7503.
64	6	PPO	1-bit programmable pulse generator output (active high).

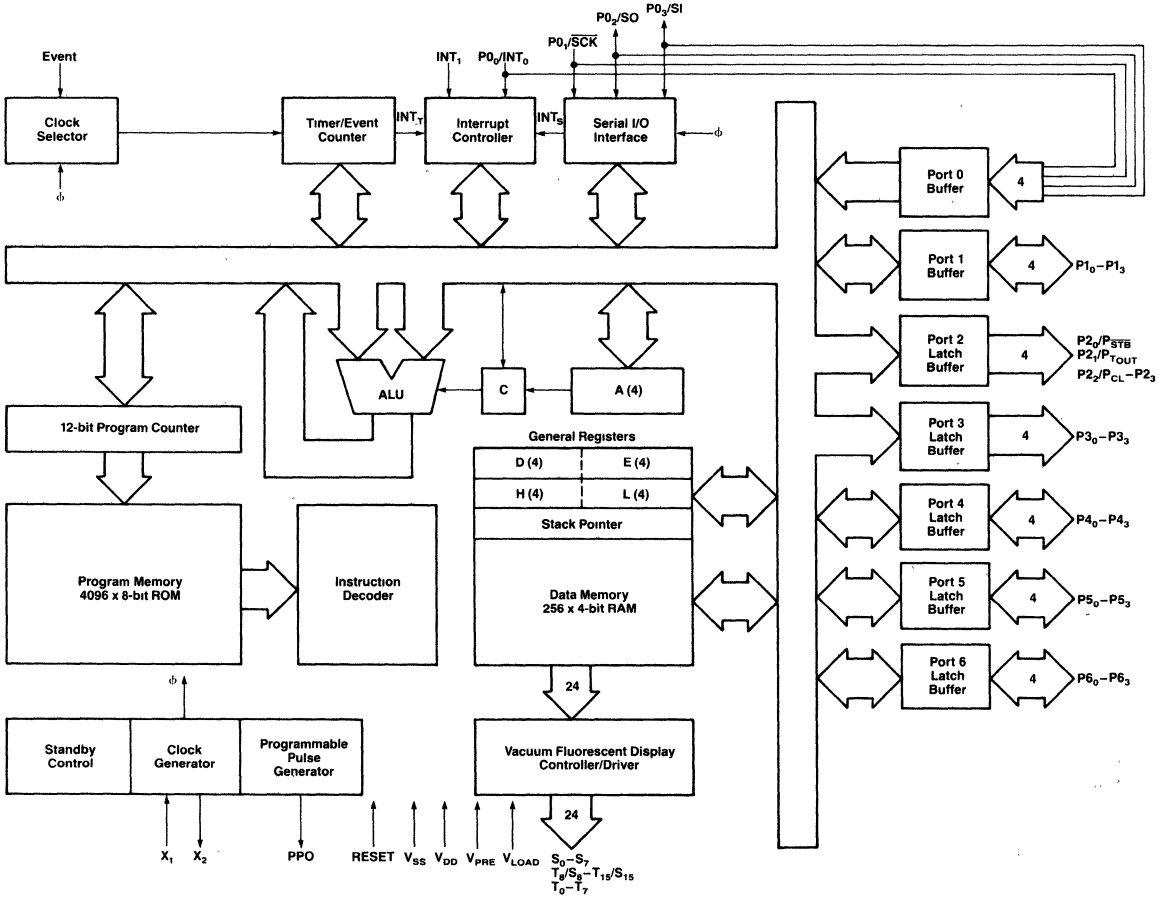
Operating Supply Voltage

T_a = −10°C to +70°C

Parameter	Limits Min	Typ	Max	Unit	Test Conditions
CPU ②	4.0		6.0	V	High-speed Mode (EM2 = 1)
	2.5		6.0	V	Low-speed Mode (EM2 = 0)
Crystal Oscillation Circuit	2.7		6.0	V	Crystal Oscillation ③ C_1 = 10pF, $C_2 \leq$ 10pF
	2.85		6.0	V	Crystal Oscillation ③ C_1 = 10pF, $C_2 \leq$ 22pF
	2.5		6.0	V	External Clock ③
Display Controller	4.0		6.0	V	
Programmable Pulse Generator	4.0		6.0	V	
Port 1	2.5		6.0	V	Port Output Mode
	4.0		6.0	V	I/O Expander Mode

Notes: See notes ② and ③ after AC Characteristics tables

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C

Supply Voltage	V_{DD} = −0.3V to +7.0V
	V_{LOAD} = V_{DD} − 40V to V_{DD} + 0.3V
	V_{PRE} = V_{DD} − 12V to V_{DD} + 0.3V
Input Voltage, V_I	−0.3V to V_{DD} + 0.3V
Output Voltage	
Outputs other than display outputs	V_O = −0.3V to V_{DD} + 0.3V
Display outputs	V_{OD} = V_{DD} − 40V to V_{DD} + 0.3V
Output Current High, I_{OH}	
Per pin other than display outputs	−15mA
Per pin, S_0–S_7	−15mA
Per pin, T_0–T_7, T_8/S_8–T_{15}/S_{15}	−30mA
Total, all outputs other than display outputs	−20mA
Total, all display outputs	−120mA
Output Current Low, I_{OL}	
Per pin	17mA
Total, all outputs	60mA
Total Power Consumption, P_T ①	
Plastic flat package	400mw
Plastic QUIL package	600mw
Operating Temperature, T_{OPT}	−10°C to +70°C
Storage Temperature, T_{STG}	−40°C to 125°C

Note: ① See note ① after AC Characteristics tables

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			15	pF	
Output Capacitance				15	pF	f = 1MHz
Other than display outputs Display outputs	C_{OUT}			35	pF	Unmeasured pins returned to 0V.
I/O Capacitance	C_{IO}			15	pF	

DC Characteristics

T_a = −10°C to +70°C; V_{DD} = 2.5V to 6.0V

Parameter		Symbol	Limits Min	Typ	Max	Unit	Test Conditions	
Input Voltage High	Other than X_1, X_2	V_{IH1}	0.7V_{DD}		V_{DD}	V		
	X_1, X_2	V_{IH2}	V_{DD} − 0.4		V_{DD}	V	③	
Input Voltage Low	Other than X_1, X_2	V_{IL1}	0		0.3V_{DD}	V		
	X_1, X_2	V_{IL2}	0		0.4	V	③	
Output Voltage High		V_{OH}	V_{DD} − 1.0			V	V_{DD} = 5V ± 0.5V; I_{OH} = −1mA	
			V_{DD} − 0.5			V	I_{OH} = −100μA	
Output Voltage Low		V_{OL}			0.4	V	V_{DD} = 5V ± 0.5V; I_{OL} = 1.6mA	
					0.5	V	I_{OL} = 400μA	
Input Leakage Current High	Other than X_1, X_2	I_{LIH1}			3	μA	V_{IN} = V_{DD}	
	X_1, X_2	I_{LIH2}			20	μA		
Input Leakage Current Low	Other than X_1, X_2	I_{LIL1}			−3	μA	V_{IN} = 0V	
	X_1, X_2	I_{LIL2}			−20	μA		
Output Leakage Current High		I_{LOH}			3	μA	V_{OUT} = V_{DD}	
Output Leakage Current Low								
Other than display outputs		I_{LOL1}			−3	μA	V_{OUT} = 0V	
Display outputs		I_{LOL2}			−10	μA	V_{OUT} = V_{LOAD} = V_{DD} − 35V	
Display Output Current		I_{OD}	−7			mA	V_{DD} = 4V to 6V; V_{PRE} = V_{DD} − 9 ± 1V③	S_0–S_7
			−15			mA		T_0–T_{15}
			−3			mA		S_0–S_7
			−7			mA	V_{OD} = V_{DD} − 2V; V_{PRE} − 0V	T_0–T_{15}
Resistance (On-chip, pull-down resistor)		R_L	100	150	200	kΩ		
Supply Current ⑤		I_{DD1}		600	2000	μA	f_X = 4.19MHz	V_{DD} = 5V ± 0.5V, High speed
				200	700	μA		V_{DD} = 3V ± 0.5V, Low speed
		I_{DD2}		260	800	μA	Halt Mode (Low speed) C_1 = C_2 = 10pF	V_{DD} = 5V ± 0.5V
				120	400	μA		V_{DD} = 3V ± 0.5V
		I_{DD3}			10	μA	Stop Mode	

Notes: See notes ③, ④, and ⑤ after AC Characteristics tables

AC Characteristics

T_a = 10°C to +70°C

Clock Operation (V_{DD} = 2.5V to 6.0V)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System Clock Oscillation Frequency	f_{XX}	3.5	4.19	5.0	MHz	Crystal Oscillation ③, ⑥
System Clock Input Frequency	f_X	0.1		5.0	MHz	
X_1, X_2 Input Pulse Width, High and Low	t_{XH}, t_{XL}	100			ns	External Clock ③
EVENT Input Frequency	f_E			410	kHz	V_{DD} = 4V to 6V
				80	kHz	
EVENT Input Pulse Width, High and Low	t_{EH}, t_{EL}	1.2			μs	V_{DD} = 4V to 6V
		6.25			μs	

Note: See notes ③ and ⑤ after AC Characteristics tables

AC Characteristics (Cont.)

Port 1 I/O Operation (V_{DD} = 2.5V to 6.0V)

Parameter	Symbol	Limits Min	Typ	Max	Units	Test Conditions
Port 1 Output Set-up Time (to $P_{\overline{STB}}$ ↑)	t_{PST}	400			ns	Port Output Mode
Port 1 Output Hold Time (after $P_{\overline{STB}}$ ↑)	t_{STP}	100			ns	
$P_{\overline{STB}}$ Pulse Width Low	t_{STL1}	600			ns	
Output Data Set-up Time (to $P_{\overline{STB}}$ ↑)	t_{DST}	400			ns	I/O Expander Mode V_{DD} = 4V to 6V
Output Data Hold Time (after $P_{\overline{STB}}$ ↑)	t_{STD}	100			ns	
Input Data Valid Time (after $P_{\overline{STB}}$ ↓)	t_{STDV}			850	ns	
Input Data Floating Time (after $P_{\overline{STB}}$ ↑)	t_{STDF}	0			ns	
Control Set-up Time (to $P_{\overline{STB}}$ ↓)	t_{CST}	400			ns	
Control Hold Time Output Command	t_{STC}	100			ns	
Control Hold Time Input Command	t_{STC}	0		80	ns	
$P_{\overline{STB}}$ Pulse Width Low	t_{STL2}	1200			ns	

Serial Interface Operation (V_{DD} = 2.5V to 6.0V)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
SCK Cycle Time	t_{KCY}	3.0			μs	Input V_{DD} = 4V to 6V
		12.5			μs	
		4.9			μs	Output V_{DD} = 4V to 6V
		25			μs	
SCK Pulse Width High, Low	t_{KH}, t_{KL}	1.3			μs	Input V_{DD} = 4V to 6V
		6.5			μs	
		2.2			μs	Output V_{DD} = 4V to 6V
		11.5			μs	
SI Set-up Time (to SCK ↑)	t_{SIK}	300			ns	V_{DD} = 4V to 6V
		1000			ns	
SI Hold Time (after SCK ↑)	t_{KSI}	450			ns	V_{DD} = 4V to 6V
		1000			ns	
SO Output Delay Time (after SCK ↓)	t_{KSO}			850	ns	V_{DD} = 4V to 6V
				2000	ns	

Other Operation (V_{DD} = 2.5V to 6.0V)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
INT_0 Pulse Width High, Low	t_{I0H}, t_{I0L}	10			μs	
INT_1 Pulse Width High, Low	t_{I1H}, t_{I1L}	⑦			μs	
RESET Pulse Width High, Low	t_{RSH}, t_{RSL}	10			μs	

Notes: ① Calculation of Total Power Consumption

The μPD7519 has three kinds of power consumption, the total for which should be less than the total power consumption (P_T) given in the specifications. (Use under the condition that less than *80%* of the specification is recommended.)

1. Power consumption of CPU: V_{DD} (max) × I_{DD1} (max)
2. The power consumption of output pins can be classified as normal output and display output. The total power consumption of each output pin to which the maximum current flows should be calculated.
3. The power consumption of on-chip pull-down resistors (mask option) on display output lines. See following example:

Example:

Configuration 9 segments × 11 digits, 4 LED outputs
V_{DD} = 5V ± 10%
Segment pin = 5mA (max)
Timing pin = 15mA (max)
LED output pin = 10mA (max)
Vacuum Fluorescent Display (V_{LOAD}) = −30V

CPU. 5.5V × 2.0mA = 11mW . . . (1)

Output Pins
Segment pins: (5/7 × 2V) × 5mA × 9 = 64mw
Timing pins 2V × 15mA = 30mw
LED output pins (10/15 × 2V) × 10mA × 4 = 53mw . (2)

Pull-down Resistors

$$\frac{(30 + 5.5V)^2}{100\Omega} \times 10 = 126mw \quad . \quad (3)$$

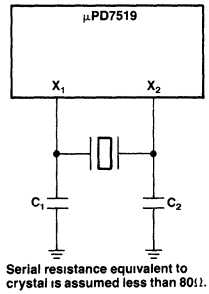
Therefore

P_T = (1) + (2) + (3) = 284mw

② Except Crystal Oscillation Circuit, Display Controller, Programmable Pulse Generator, and Port 1.

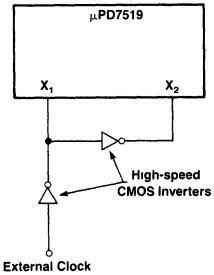
③ The following circuits are recommended:

Crystal

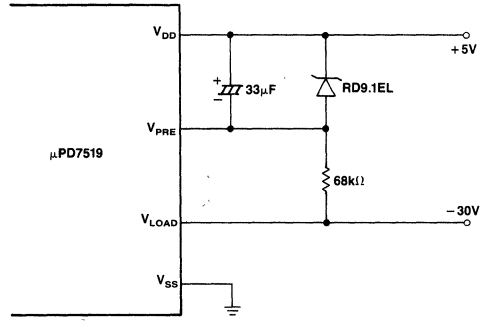


Serial resistance equivalent to crystal is assumed less than 80Ω.

External Clock



④ The following external circuit is recommended:



Note: RD9 1EL Zener diode (NEC)
Zener voltage = 8.29V to 9 30V

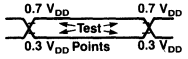
⑤ Display Controller and Programmable Pulse Generator are not operated.

⑥ Refer to Operating Supply Voltage.

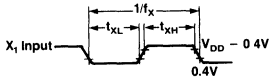
⑦ $2^8/f_X$ or $2^8/f_{XX}$.

Timing Waveforms

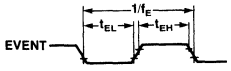
AC Test Points (Except X_1)



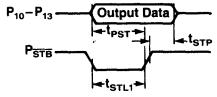
Clock Timing



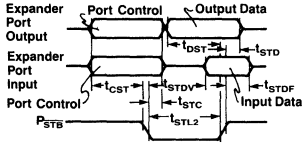
EVENT Timing



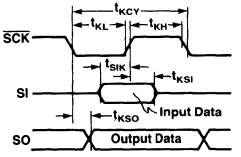
Strobe Output Timing



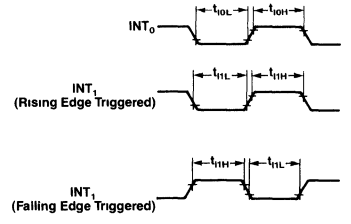
Port 1 I/O Expander Timing



Serial Interface Timing



Interrupt Input Timing



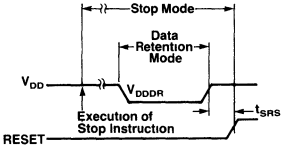
RESET Input Timing

Stop Mode Low Voltage Data Retention Characteristics

T_a = −10°C to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data Retention Supply Voltage	V_{DDDR}	2.0		6.0	V	
Data Retention Supply Current	I_{DDDR}			10	μA	V_{DDDR} = 2.0V
Reset Set-up Time	t_{SRS}	0			μs	

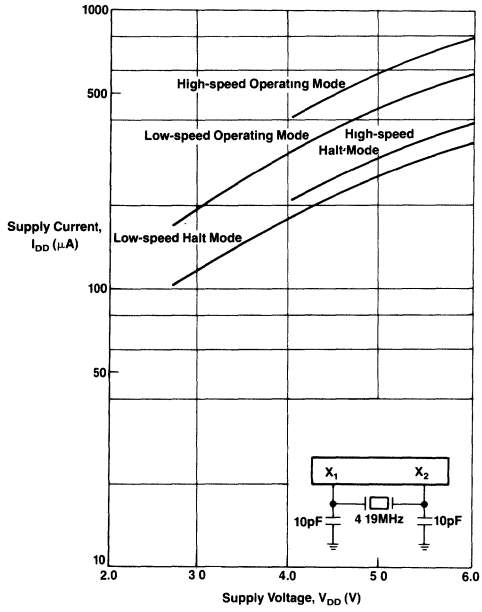
Data Retention Timing



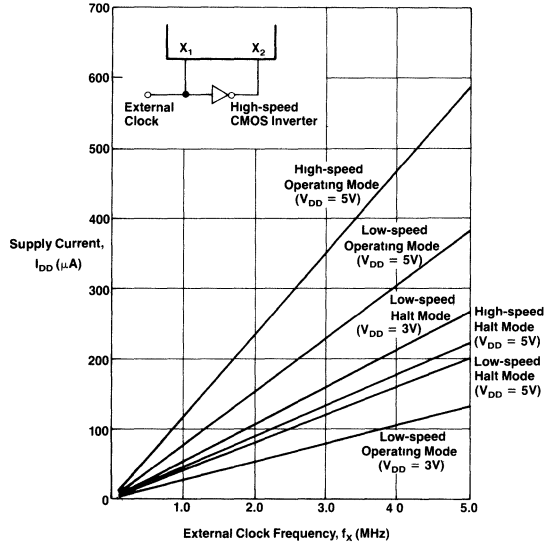
Operating Characteristics

T_a = 25°C, Typical

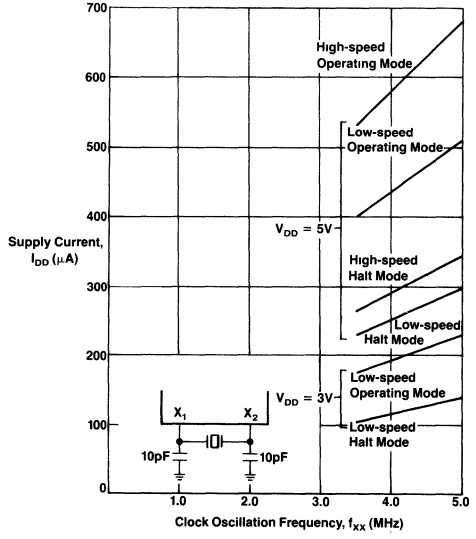
Supply Current versus Supply Voltage
I_{DD} vs V_{DD} (f_{XX} = 4.19MHz)



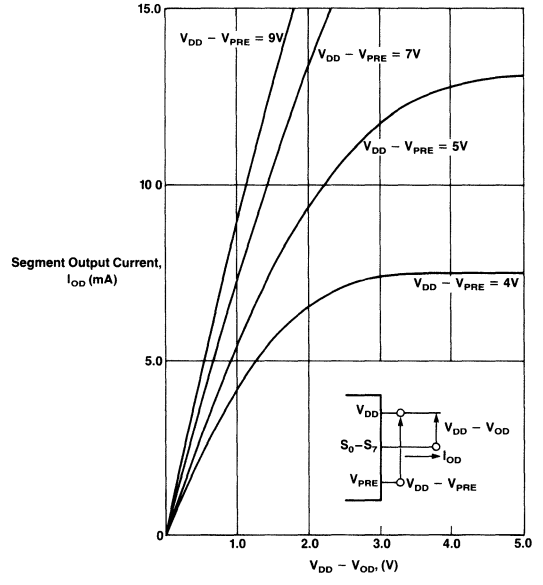
Supply Current versus External Clock Frequency
I_{DD} vs f_X



Supply Current versus Clock Oscillation Frequency
I_{DD} vs f_{XX}



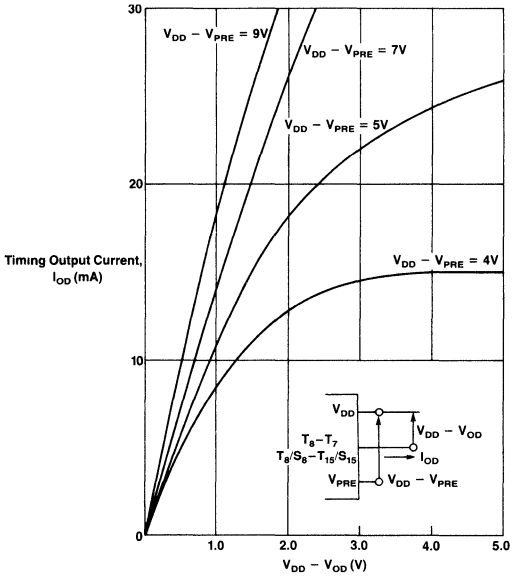
Segment Output Current versus Output Voltage
I_{OD} vs (V_{DD} − V_{OD}); (V_{DD} = 4V to 6V)



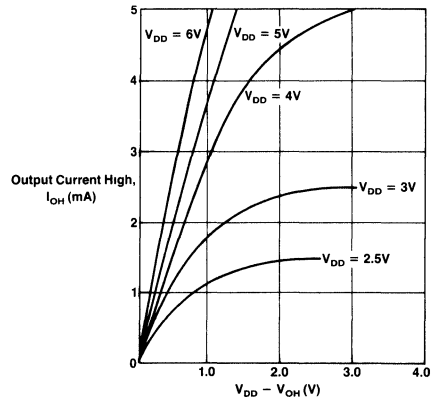
Operating Characteristics (Cont.)

T_a = 25°C, Typical

Timing Output Current versus Output Voltage
I_{OD} vs ($V_{DD} - V_{OD}$); (V_{DD} = 4V to 6V)



Output Current Low versus Output Voltage Low
I_{OL} vs V_{OL}



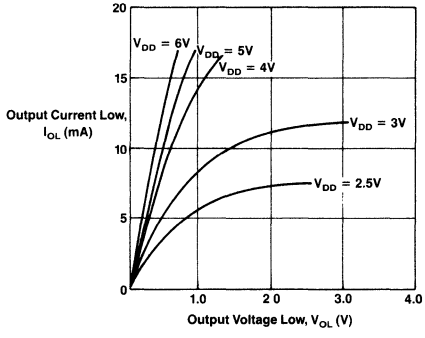
3

Package Outlines

For information, see Package Outline Section 7.

Plastic Quil, μPD7519G
Plastic Shrinkdip, μPD7519CW
QUIL Ceramic Piggyback, μPD75CG19E

Output Current High versus Output Voltage High
I_{OH} vs ($V_{DD} - V_{OH}$)

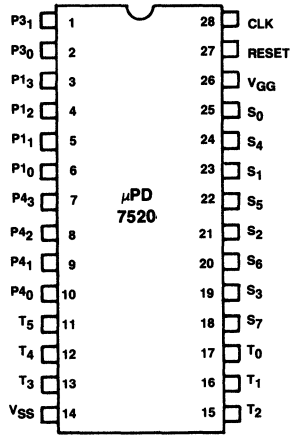


μPD7520
4-BIT SINGLE CHIP MICROCOMPUTER WITH LED DISPLAY CONTROLLER/DRIVER

Description

The μPD7520 is a low-cost 4-bit single chip microcomputer which shares the 4th generation architecture of the μPD7500 series of CMOS 4-bit microcomputers. It contains a 768 x 8-bit ROM and a 48 x 4-bit RAM. It has a 2-level subroutine stack, and executes a 47-instruction subset of the μPD7500 series instruction set. The μPD7520 provides 24 I/O lines, organized into the 4-bit input Port 1, the 4-bit I/O Port 4, the 2-bit output Port 3, the 8-bit output Port S, and the 6-bit output Port T. Ports S and T are controlled by the on-board programmable LED display controller/driver hardware logic block, which automatically directly drives either static or multiplexed common-anode 7-segment LED displays totally transparent to program execution. The μPD7520 is manufactured with a low-power consumption PMOS process, allowing use of a single power supply between −6V and −10V, and is available in a 28-pin dual-in-line plastic package.

Pin Configuration



Pin Names

S_0–S_7	Segment Drive Output Port S
T_0–T_5	Digit Drive Output Port T
$P1_0$–$P1_3$	Input Port 1
$P3_0$–$P3_1$	Output Port 3
$P4_0$–$P4_3$	Input/Output Port 4
CLK	Clock Input
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Ground

Further details on device operation can be found in the μPD7520 4-Bit Single Chip Microcomputer Technical Manual.

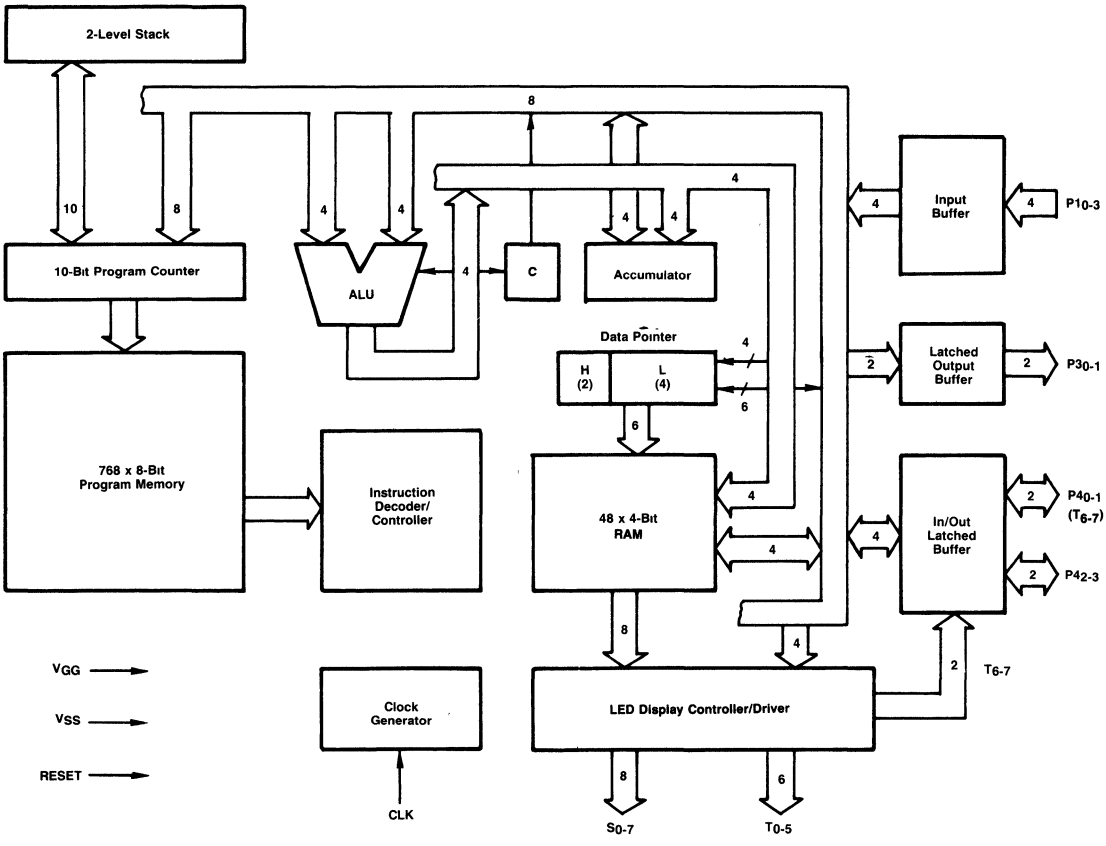
3

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{GG}	−15V to +0.3V
Input Voltages	−15V to +0.3V
Output Voltages	−15V to +0.3V
Output Current (I_{OH} Total)	−100mA
(I_{OL} Total)	90mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



DC Characteristics

T_a = −10°C to +70°C, V_{GG} = −6V to −10V, V_{SS} = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Voltage High	V_{IH}			−2.0	V	Ports 1, 4, RESET; V_{GG} = −9V ± 1V
				−1.8		V_{GG} = −6V to −10V
Input Voltage Low	V_{IL}	V_{GG} + 1.5			V	Ports 1, 4, RESET; V_{GG} = −9V ± 1V
		V_{GG} + 0.8				V_{GG} = −6V to −10V
Clock Voltage High	$V_{\phi H}$			−0.8	V	CLK, External Clock
Clock Voltage Low	$V_{\phi L}$	−5.0			V	CLK, External Clock
Input Current High	I_{IH}	45		200	μA	Port 1, RESET; V_I = 0V, V_{GG} = −9V ± 1V
		40		200		V_I = 0V, V_{GG} = −6V to −10V
Input Leakage Current High	I_{LIH}			+5	μA	Port 4, V_I = 0V
Input Leakage Current Low	I_{LIL_1}			−5	μA	Port 1, RESET, V_I = −10V, V_{GG} = −10V
	I_{LIL_2}			−5	μA	Port 4, V_I = −10V
Clock Current High	$I_{\phi H}$			0.5	mA	CLK, External Clock, $V_{\phi H}$ = 0V, V_{GG} = −9V ± 1V
Clock Current Low	$I_{\phi L}$			−2.1	mA	CLK, External Clock, $V_{\phi L}$ = −5V, V_{GG} = −9V ± 1V
Output Voltage Low	V_{OL}	0 6 V_{GG}			V	Port 3, No Load
Output Current High	I_{OH_1}	−1.0			mA	Port 3, V_O = −1.0V, V_{GG} = −9V ± 1V
		−0.6				V_O = −1.0V, V_{GG} = −6V
	I_{OH_2}	−2.0			mA	Port 4, V_O = −1.0V, V_{GG} = −9V ± 1V
		−1.2				V_O = −1.0V, V_{GG} = −6V
	I_{OH_3}	−5	−10		mA	Port S, V_O = −2.0V, V_{GG} = −9V ± 1V
		−3	−6			V_O = −2.0V, V_{GG} = −6V
		−1	−3			V_O = −1.0V, V_{GG} = −6V to −10V
	I_{OH_4}	−24	−48		mA	Port T, V_O = −2.0V, V_{GG} = −9V ± 1V
		−13	−27			V_O = −1.0V, V_{GG} = −9V ± 1V
		−9	−18			V_O = −1.0V, V_{GG} = −6V
Output Current Low	I_{OL_1}	1.0	2.0		mA	Port 3, V_O = V_{GG} + 1.5V, V_{GG} = −9V ± 1V ①
		0.3	0.6			V_O = −4.5V, V_{GG} = −6V ①
	I_{OL_2}	4.5	9		mA	Port S, V_O = V_{GG} + 5.0V, V_{GG} = −9V ±1V
		1.0	2.0			V_O = V_{GG} + 3.5V, V_{GG} = −6V to −10V
Output Leakage Current High	I_{LOH}			+5	μA	Ports 4, T, V_O = 0V
Output Leakage Current Low	I_{LOL_1}			−5.0	μA	Port T, V_O = −10V
	I_{LOL_2}			−5.0		Port 3, V_O = V_{GG}
Supply Current	I_{GG}		−5②	−9.8	mA	No Load

Notes:

① Current within 2.5 ms after turning to the low level (T_a = 25°C).

② T_a = 25°C, V_{GG} = −9V.

AC Characteristics

T_a = −10°C to +70°C, V_{GG} = −6V to −10V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Clock Frequency	f_{osc}	225	300	375	KHz	R_f = 1MΩ, V_{GG} = −9V ± 1V, T_a = 25°C
		180	300	450	KHz	R_f = 1MΩ, V_{GG} = −9V ± 1V
	f_ϕ	100		330	KHz	
Clock Rise and Fall Times	t_r, t_f			2	μs	CLK, External Clock
Clock Pulse Width High	$t_{\phi W_H}$	1.5		3	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	1.5		3	μs	

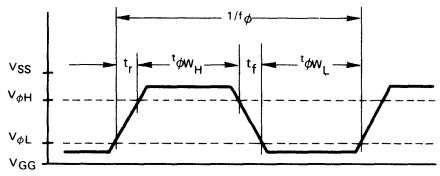
Capacitance

T_a = 25°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	Port 1, RESET
Output Capacitance	C_O			20	pF	Ports 3, S,T
Input/Output Capacitance	C_{IO}			20	pF	Port 4
Clock Capacitance	C_ϕ			30	pF	CLK

f = 1MHz

Clock Waveform



Development Tools

The NEC Electronics U.S.A.'s NDS Development System is available for the development of software source code, editing, and assembly into object code. In addition, the ASM75 Cross Assembler is available for systems supporting the ISIS-II or the CP/M (® Digital Research Corp.) Operating Systems.

The EVAKIT-7520 Evaluation Board is available for production device evaluation and prototype system debugging.

The ASM75-F9T Cross Assembler is available for systems supporting fortran IV ANSI Standard 1966-V3.9.

Instruction Set Symbol Definitions

The following abbreviations are used in the description of the μPD7520 instruction set:

SYMBOL	EXPLANATION AND USE
A	Accumulator
address	Immediate address
C	Carry Flag
data	Immediate data
D_n	Bit "n" of immediate data or immediate address
H	Register H
HL	Register pair HL
L	Register L
P( )	Parallel Input/Output Port addressed by the value within the brackets
PC_n	Bit "n" of Program Counter
S	Zero when Skip Condition does not occur; the number of bytes in next instruction when Skip Condition occurs
Stack	Stack Register
String	String Effect Skip Condition, whereby succeeding instructions of the same type are executed as NOP instructions
( )	The contents of RAM addressed by the value within the brackets
[ ]	The contents of ROM addressed by the value within the brackets
←	Load, Store, or Transfer
↔	Exchange
—	Complement
∀	LOGICAL Exclusive-OR

Instruction Set

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
			LOAD										
LAI data	A ← P_{3-0}	Load A with 4 bits of immediate data, execute succeeding LAI instructions as NOP instructions	0	0	0	1	D_3	D_2	D_1	D_0	1	1	String
LHI data	H ← D_{1-0}	Load H with 2 bits of immediate data	0	0	1	0	1	0	D_1	D_0	1	1	
LHLI data	HL ← D_{4-0}	Load HL with 5 bits of immediate data, execute succeeding LHLI instructions as NOP instructions	1	1	0	D_4	D_3	D_2	D_1	D_0	1	1	String
LAMT	A ← $[PC_{9-6}, 0, C, A]_H$	Load the upper 4 bits of ROM Table Data at address PC_{9-6}, 0, C, A to A	0	1	0	1	1	1	1	0	1	2	
	(HL) ← $[PC_{9-6}, 0, C, A]_L$	Load the lower 4 bits of ROM Table Data at address PC_{9-6}, 0, C, A to the RAM location addressed by HL											
L	A ← (HL)	Load A with the contents of RAM addressed by HL	0	1	0	1	0	0	1	0	1	1	
LIS	A ← (HL) L = L + 1 Skip if L = 0H	Load A with the contents of RAM addressed by HL, increment L, skip if L = 0H	0	1	0	1	0	0	0	1	1	1 + S	L = 0H
LDS	A ← (HL) L = L − 1 Skip if L = FH	Load A with the contents of RAM addressed by HL, decrement L, skip if L = FH	0	1	0	1	0	0	0	0	1	1 + S	L = FH
LADR address	A ← (D_{5-0})	Load A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	0 D_0	2	2	

Instruction Set (Cont.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
		STORE											
ST	(HL) ← A	Store A into the RAM location addressed by HL	0	1	0	1	0	1	1	1	1	1	
STII data	(HL) ← D_{3-0} L ← L + 1	Store 4 bits of immediate data into the RAM location addressed by HL; increment L	0	1	0	0	D_3	D_2	D_1	D_0	1	1	
		EXCHANGE											
XAH	A_{1-0} ↔ H_{1-0} A_{3-2} ← 00H	Exchange A with H	0	1	1	1	1	0	1	0	1	1	
XAL	A ↔ L	Exchange A with L	0	1	1	1	1	0	1	1	1	1	
X	A ↔ (HL)	Exchange A with the contents of RAM addressed by HL	0	1	0	1	0	1	1	0	1	1	
XIS	A ↔ (HL) L ← L + 1 Skip if L = 0H	Exchange A with the contents of RAM addressed by HL; increment L, skip if L = 0H	0	1	0	1	0	1	0	1	1	1 + S	L = 0H
XDS	A ↔ (HL) L ← L − 1 Skip if L = FH	Exchange A with the contents of RAM addressed by HL; decrement L; skip if L = FH	0	1	0	1	0	1	0	0	1	1 + S	L = FH
XADR address	A ↔ (D_{5-0})	Exchange A with the contents of RAM addressed by 6 bits of immediate data	0 0	0 0	1 D_5	1 D_4	1 D_3	0 D_2	0 D_1	1 D_0	2	2	
		ARITHMETIC AND LOGICAL											
AISC data	A ← A + D_{3-0} Skip if overflow	Add 4 bits of immediate data to A, Skip if overflow is generated	0	0	0	0	D_3	D_2	D_1	D_0	1	1 + S	Overflow
ASC	A ← A + (HL) Skip if overflow	Add the contents of RAM addressed by HL to A; skip if overflow is generated	0	1	1	1	1	1	0	1	1	1 + S	Overflow
ACSC	A, C ← A + (HL) + C Skip if C = 1	Add the contents of RAM addressed by HL and the carry flag to A, skip if carry is generated	0	1	1	1	1	1	0	0	1	1 + S	C = 1
EXL	A ← A ∨ (HL)	Perform a LOGICAL Exclusive—OR operation between the contents of RAM addressed by HL and A, store the result in A	0	1	1	1	1	1	1	0	1	1	
		ACCUMULATOR AND CARRY FLAG											
CMA	A ← $\overline{A}$	Complement A	0	1	1	1	1	1	1	1	1	1	
RC	C ← 0	Reset Carry Flag	0	1	1	1	1	0	0	0	1	1	
SC	C ← 1	Set Carry Flag	0	1	1	1	1	0	0	1	1	1	
		INCREMENT AND DECREMENT											
ILS	L ← L + 1 Skip if L = 0H	Increment L, Skip if L = 0H	0	1	0	1	1	0	0	1	1	1 + S	L = 0H
IDRS address	(D_{5-0}) ← (D_{5-0}) + 1 Skip if (D_{5-0}) = 0H	Increment the contents of RAM addressed by 6 bits of immediate data; Skip if the contents = 0H	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	1 D_0	2	2 + S	(D_{5-0}) = 0H
DLS	L ← L − 1 Skip if L = FH	Decrement L; Skip if L = FH	0	1	0	1	1	0	0	0	1	1 + S	L = FH
DDRS address	(D_{5-0}) ← (D_{5-0}) − 1 Skip if (D_{5-0}) = FH	Decrement the contents of RAM addressed by 6 bits of immediate data, skip if the contents = FH	0 0	0 0	1 D_5	1 D_4	1 D_3	1 D_2	0 D_1	0 D_0	2	2 + S	(D_{5-0}) = FH
		BIT MANIPULATION											
RMB data	$(HL)_{bit}$ ← 0	Reset a single bit (denoted by D_1D_0) of the RAM location addressed by HL to zero	0	1	1	0	1	0	D_1	D_0	1	1	
SMB data	$(HL)_{bit}$ ← 1	Set a single bit (denoted by D_1D_0) of the RAM location addressed by HL to one	0	1	1	0	1	1	D_1	D_0	1	1	
		JUMP, CALL, AND RETURN											
JMP address	PC_{9-0} ← D_{9-0}	Jump to the address specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	0 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
JAM data	PC_{9-8} ← D_{1-0} PC_{7-4} ← A PC_{3-0} ← (HL)	Jump to the address specified by 2 bits of immediate data, A, and the RAM contents addressed by HL	0 0	0 0	1 0	1 1	1 0	1 0	1 D_1	1 D_0	2	2	

Instruction Set (Cont.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	BYTES	CYCLES	SKIP CONDITION
			JUMP, CALL, AND RETURN										
JCP address	$PC_{5-0} \leftarrow D_{5-0}$	Jump to the address specified by the higher-order bits PC_{9-6} of the PC, and 6 bits of immediate data	1	0	D_5	D_4	D_3	D_2	D_1	D_0	1	1	
CALL address	STACK ← PC + 2 $PC_{9-0} \leftarrow D_{9-0}$	Store a return address (PC + 2) in the stack; call the subroutine program at the location specified by 10 bits of immediate data	0 D_7	0 D_6	1 D_5	1 D_4	0 D_3	0 D_2	D_9 D_1	D_8 D_0	2	2	
CAL address	STACK ← PC + 1 $PC_{9-0} \leftarrow 01D_4D_3$ $000D_2D_1D_0$	Store a return address (PC + 1) in the stack; call the subroutine program at one of the 32 special locations specified by 5 bits of immediate data	1	1	1	D_4	D_3	D_2	D_1	D_0	1	1	
RT	PC ← STACK	Return from Subroutine	0	1	0	1	0	0	1	1	1	1	
RTS	PC ← STACK Skip unconditionally	Return from Subroutine; skip unconditionally	0	1	0	1	1	0	1	1	1	1 + S	Unconditional
			SKIP										
SKC	Skip if C = 1	Skip if carry flag is true	0	1	0	1	1	0	1	0	1	1 + S	C = 1
SKMBT data	Skip if $(HL)_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is true	0	1	1	0	0	1	D_1	D_0	1	1 + S	$(HL)_{bit} = 1$
SKMBF data	Skip if $(HL)_{bit} = 0$	Skip if the single bit (denoted by D_1D_0) of the RAM location addressed by HL is false	0	1	1	0	0	0	D_1	D_0	1	1 + S	$(HL)_{bit} = 0$
SKABT data	Skip if $A_{bit} = 1$	Skip if the single bit (denoted by D_1D_0) of A is true	0	1	1	1	0	1	D_1	D_0	1	1 + S	$A_{bit} = 1$
SKAEI data	Skip if A = data	Skip if A equals 4 bits of immediata data	0 0	0 1	1 1	1 0	1 D_3	1 D_2	1 D_1	1 D_0	2	2 + S	A = data
SKAEM	Skip if A = (HL)	Skip if A equals the RAM contents addressed by HL	0	1	0	1	1	1	1	1	1	1 + S	A = (HL)
			PARALLEL I/O										
IPL	A ← P(L)	Input the Port addressed by L to A	0	1	1	1	0	0	0	0	1	1	
IP1	A ← P1	Input Port 1 to A	0	1	1	1	0	0	0	1	1	1	
OPL	P(L) ← A	Output A to the port addressed by L	0	1	1	1	0	0	1	0	1	1	
OP3	$P3 \leftarrow A_{1-0}$	Output the lower 2 bits of A to Port 3	0	1	1	1	0	0	1	1	1	1	
			CPU CONTROL										
NOP		Perform no operation; consume one machine cycle	0	0	0	0	0	0	0	0	1	1	

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7520C

Plastic Shrinkdip, μPD7520CT

μPD7527/7528/7537/7538 CMOS 4-BIT SINGLE-CHIP MICROCOMPUTER WITH VACUUM FLUORESCENT DISPLAY DRIVE CAPABILITY

Description

The μPD7527/28 and the μPD7537/38 are pin-compatible CMOS 4-bit single-chip microcomputers which have the same μPD750X architecture.

The μPD7527/37 contains a 2048 x 8-bit ROM, and a 128 x 4-bit RAM. The μPD7528/38 contains a 4096 x 8-bit ROM, and a 160 x 4-bit RAM.

Both the μPD7527/28 and the μPD7537/38 contain two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater depth and flexibility. The μPD7527/28 and μPD7537/38 typically execute 67 instructions of the μPD7500 series A instruction set with a 5μs instruction cycle time.

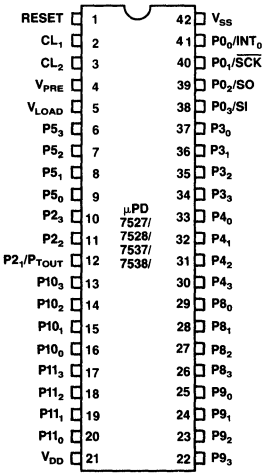
The μPD7527/28 and the μPD7537/38 have one external and two internal edge-triggered hardware vectored interrupts. They also contain an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

Both the μPD7527/28 and the μPD7537/38 provide 31 I/O lines organized into the 4-bit input/serial interface Port 0, the 3-bit Port 2, the 4-bit Port 3, and the 4-bit I/O Ports 1, 4, 5, 8, 9, 10 and 11. They are manufactured with a low power consumption CMOS process, allowing the use of a power supply between 2.7V and 5.5V. Current consumption is less than 900μA maximum, and can be lowered much further in the Halt and Stop power-down modes. The μPD7527/28 and μPD7537/38 are available in a 42-pin dual-in-line plastic package.

The μPD7527/28 and μPD7537/38 are upward compatible with other members of the μPD75xx product family.

For prototyping work, and as an aid to program development, there are piggyback EPROM versions for both devices: the 75CG28E and 75CG38E. These are pin-compatible and functionally compatible with the final, masked versions of the devices.

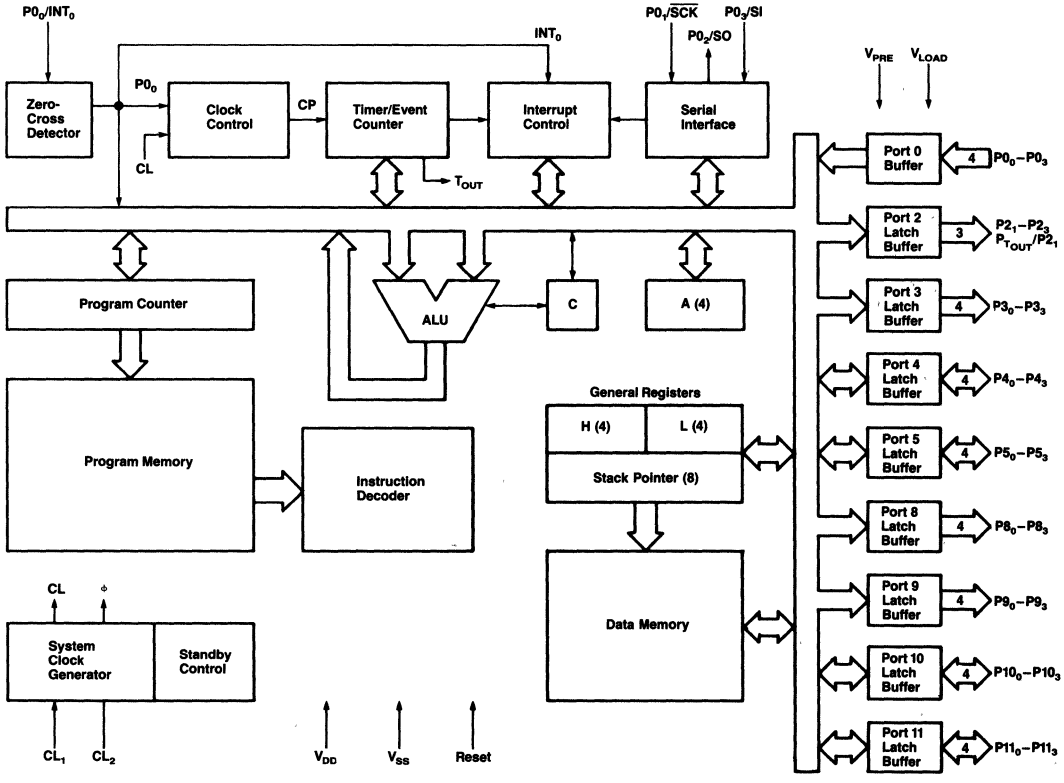
Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	RESET	Reset input (active high). R/C circuit or pulse initializes the microcomputer after power up.
2, 3	CL_1, CL_2	System clock oscillator. CL_1 is the input and CL_2 the output.
4	V_{PRE}	Power supply input for the high voltage output predrivers.
5	V_{LOAD}	Power supply common input for output load resistors.
6, 7, 8, 9	$P5_0$–$P5_3$	Input/output Port 5
10, 11, 12	$P2_1/PT_{OUT}$ $P2_2$–$P2_3$	Port 2, bit 3 output, and timer output. Output Port 2, bits 2 and 3.
13, 14, 15, 16	$P10_0$–$P10_3$	Input/output Port 10.
17, 18, 19, 20	$P11_0$–$P11_3$	Input/output Port 11.
21	V_{DD}	Positive power supply.
22, 23, 24, 25	$P9_0$–$P9_3$	Output Port 9.
26, 27, 28, 29	$P8_0$–$P8_3$	Output Port 8.
30, 31, 32, 33	$P4_0$–$P4_3$	Output Port 4.
34, 35, 36, 37	$P3_0$–$P3_3$	Output Port 3.
38, 39, 40, 41	$P0_0/INT_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/serial I/O interface. This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode register. The serial input SI, serial output SO, and the serial clock SCK (NOT) used for synchronizing data transfer comprise the 8-bit serial I/O interface.
42	V_{SS}	Ground.

Block Diagram



Distinguishing Features

	μPD7527	μPD7528	μPD7537	μPD7538
Type of Oscillator (CL_1, CL_2)	R/C	R/C	Crystal	Crystal
Program Counter	11 bits	12 bits	11 bits	12 bits
Program Memory	2048 x 8	4096 x 8	2048 x 8	4096 x 8
Data Memory	128 x 4	160 x 4	128 x 4	160 x 4
Number of Instructions	67	67	66	66

Mask Options

$P0_0/INT_0$	This input, as a mask option, can be altered from a standard digital CMOS input to a zero-crossing detector.
Ports 2_1-2_3, 3_0-3_3, 4_0-4_3, 5_0-5_3, 8_0-8_3, 9_0-9_3, 10_0-10_3, 11_0-11_3	These I/O ports can selectively be provided with optional pull-down load resistors at the bit level.

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7527C/28C/37C/38C
Plastic Shrinkdip, μPD7527C 28C 37C 38C
Ceramic Piggyback, μPD75CG28E/CG38E

μPD7500
CMOS 4-BIT MICROPROCESSOR
μPD7500 SERIES ROM-LESS EVALUATION CHIP

Description

The μPD7500 is a CMOS 4-bit microprocessor which has the μPD750x architecture, and also functions as the μPD7500 series ROM-less evaluation chip.

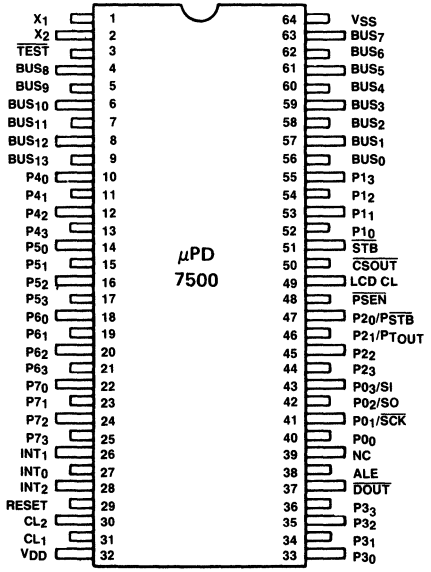
The μPD7500 contains a 256 x 4-bit RAM, and is capable of addressing up to 8192 x 8-bits of external program memory.

The μPD7500 contains four 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values. The μPD7500 typically executes either all 110 instructions of the μPD7500 series "A" instruction set, or all 70 instructions of the μPD7500 series "B" instruction set with a 10μs instruction cycle time.

The μPD7500 has three external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements. A display timing pulse is also provided when emulating the μPD7501, μPD7502, the μPD7503, or the μPD7519.

The μPD7500 provides 32 I/O lines organized into the 4-bit input/serial interface Port 0, the 4-bit output Port 2, the 4-bit output Port 3, and the 4-bit I/O Ports 1, 4, 5, 6, and 7. It is manufactured with a low power consumption CMOS process, allowing the use of a single +5V power supply. Current consumption is less than 900μA maximum, and can be lowered much further in the HALT and STOP power-down modes. The μPD7500 is available in a 64-pin quad-in-line plastic package.

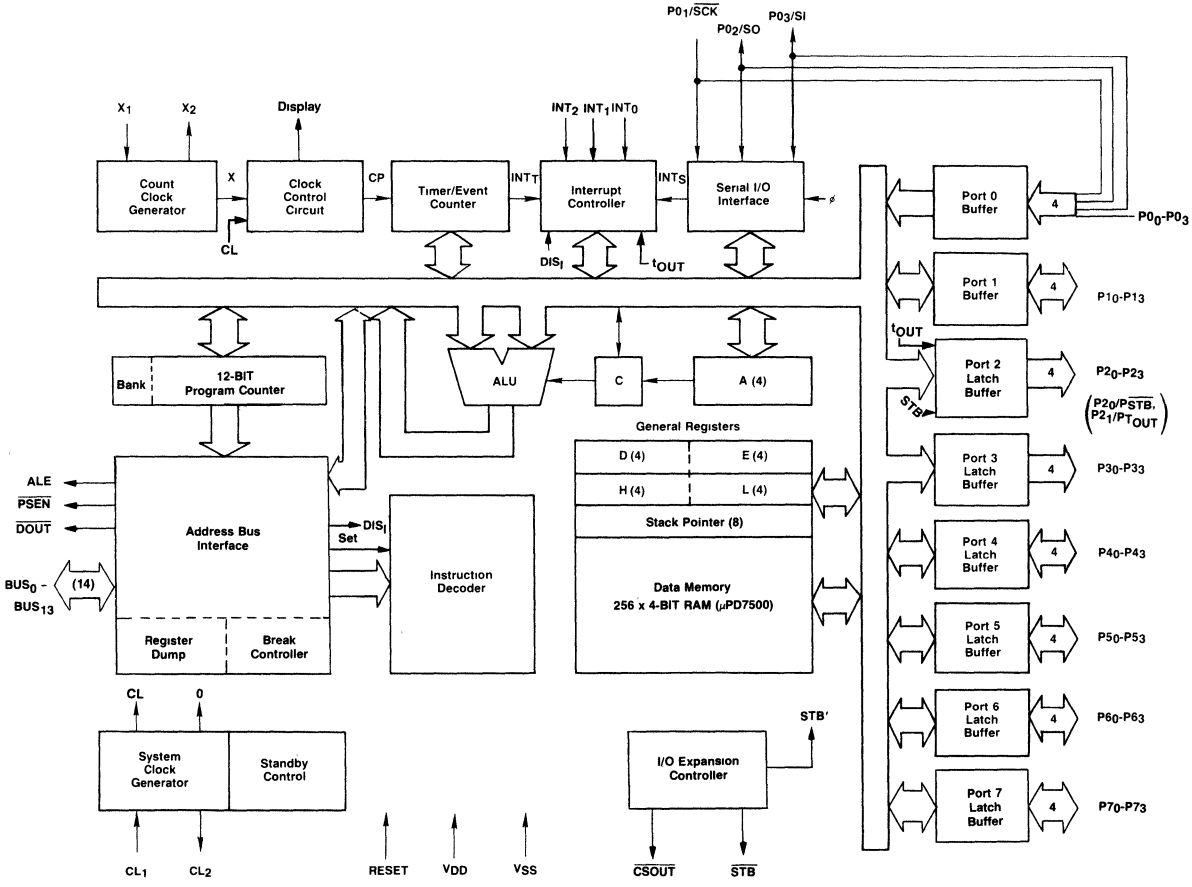
Pin Configuration



Pin Names

Pin No.	Pin Symbol	Function
1, 2	X_2, X_1	Crystal clock/external event input Port X (active high). A crystal oscillator circuit is connected to input X_1 and output X_2 for crystal clock operation. Alternatively, external event pulses are connected to input X_1 while output X_2 is left open for external event counting.
3	$\overline{TEST}$	Factory test pin (connect to V_{SS}).
4-9, and 56-63	BUS_0-BUS_{13}	External data bus (active high). Connected to external program memory.
10-13	$P4_0$-$P4_3$	4-bit input/latched tri-state output Port 4 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 5.
14-17	$P5_0$-$P5_3$	4-bit input/latched tri-state output Port 5 (active high). Can also perform 8-bit parallel I/O in conjunction with Port 4.
18-21	$P6_0$-$P6_3$	4-bit input/latched tri-state output Port 6 (active high). Individual lines can be configured either as inputs or as outputs under control of the Port 6 mode select register.
22-25	$P7_0$-$P7_3$	4-bit input/latched tri-state output Port 7 (active high).
26	INT_1	External interrupt INT_1 (active high). This is a rising edge-triggered interrupt.
27	INT_0	External interrupt INT_0 (active high). This is a rising edge-triggered interrupt.
28	INT_2	External interrupt INT_2 (active high). This is a rising edge-triggered interrupt.
29	RESET	RESET input (active high). R/C circuit or pulse initializes μPD7500 after power-up.
30, 31	CL_1, CL_2	System clock input (active high). Connect 82KΩ resistor across CL_1 and CL_2, and connect 33pF capacitor from CL_1 to V_{SS}. Alternatively, an external clock source may be connected to CL_1, whereas CL_2 is left open.
32	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
33-36	$P3_0$-$P3_3$	4-bit input/latched tri-state output Port 3 (active high).
37	$\overline{DOUT}$	Data output (active low).
38	ALE	Address latch enable (active high).
39	NC	No connection.
40-43	$P0_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input Port 0/serial I/O interface (active high). This port can be configured either as a 4-bit parallel input port, or as the 8-bit serial I/O interface, under control of the serial mode select register. The Serial Input SI (active high), Serial Output SO (active low), and the Serial Clock $\overline{SCK}$ (active low) used for synchronizing data transfer comprise the 8-bit serial I/O interface.
44-47	$P2_0$-$P2_3$ $P2_0/P\overline{STB}$ $P2_1/PT_{OUT}$	4-bit latched tri-state output Port 2 (active high). Line $P2_0$ is also shared with $P\overline{STB}$, the Port 1 output strobe pulse (active low). Line $P2_1$ is also shared with PT_{OUT}, the timer-out F/F signal (active high).
48	$\overline{PSEN}$	Program store enable (active low).
49	DISPLAY	DISPLAY timing pulse (active high).
50	$\overline{CSOUT}$	Chip select output (active low). Connected to μPD82C43.
51	$\overline{STB}$	STROBE output (active low). Connected to μPD82C43.
52-55	$P1_0$-$P1_3$	4-bit input/tri-state output Port 1 (active high). Data output to Port 1 is strobed in synchronization with a $P2_0/P\overline{STB}$ pulse.
64	V_{SS}	Ground.

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage, V_{DD}	−0.3V to +7.0V
All Input and Output Voltages	−0.3V to V_{DD} +0.3V
Output-Current (Total, All Output Ports)	I_{OH} = −20mA
	I_{OL} = 50mA

*Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C, V_{DD} = 5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Voltage High	V_{IH_1}	0.7 V_{DD}		V_{DD}	V	All Inputs Other than CL_1, X_1
	V_{IH_2}	V_{DD} −0.5		V_{DD}		CL_1, X_1
Input Voltage Low	V_{IL_1}	0		0.3 V_{DD}	V	All Inputs Other than CL_1, X_1
	V_{IL_2}	0		0.5		CL_1, X_1
Input Leakage Current High	$I_{LI_{H1}}$			3	μA	All Inputs Other V_I = V_{DD} than CL_1, X_1
	$I_{LI_{H2}}$			10		CL_1, X_1
Input Leakage Current Low	$I_{LI_{L1}}$			−3	μA	All Inputs Other V_I = 0V than CL_1, X_1
	$I_{LI_{L2}}$			−10		CL_1, X_1
Output Voltage High	V_{OH}	V_{DD} − 1.0			V	
Output Voltage Low	V_{OL}			0.4	V	
Output Leakage Current High	I_{LO_H}			3	μA	V_O = V_{DD}
Output Leakage Current Low	I_{LO_L}			−3	μA	V_O = 0V
Supply Current	I_{DD_1}			2	mA	Normal Operation All Output Pins Open No BUS Conflicts
	I_{DD_2}	2	20		μA	Stop Mode, X_1 = 0V
	$I_{DD_{DR}}$	0.4	10			Data Retention Mode $V_{DD_{DR}}$ = 2.0V

Capacitance

T_a = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			15	pF	f = 1MHz
Output Capacitance	C_{OUT}			15	pF	Unmeasured pins returned to V_{SS}
I/O Capacitance	C_{IO}			15	pF	

AC Characteristics

T_a = −10° ∼ +70°C, V_{DD} = 5V ± 10%

Clock Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System Clock Oscillation Frequency	f_ϕ	120	200	280	KHz	R = 82kΩ ± 2% C = 33pF ± 5%
	f_ϕ	10		300	KHz	CL_1, External Clock
CL_1 Input Rise Time	t_{CR}			0.2	μs	
CL_1 Input Fall Time	t_{CF}			0.2	μs	
CL_1 Input Clock Width (High)	t_{CH}	1.5			μs	
CL_1 Input Clock Width (Low)	t_{CL}	1.5			μs	
Count Clock Oscillation Frequency (X_1, X_2)	f_{XX}		32		KHz	Xtal Oscillation
Count Clock Input Frequency (X_1)	f_X	0		300	KHz	
X_1 Input Rise Time	t_{XR}			0.2	μs	
X_1 Input Fall Time	t_{XF}			0.2	μs	
X_1 Input Clock Width (High)	t_{XH}	1.5			μs	
X_1 Input Clock Width (Low)	t_{XL}	1.5			μs	

Bus I/O Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
ALE Pulse Width (High)	t_{LH}	600			ns	
Address Setup Time to ALE↓	t_{AL}	200			ns	
Address Hold Time after ALE↓	t_{LA}	100			ns	
Output Data Setup Time to $\overline{DOUT}$↑	t_{DDO}	200			ns	
Output Data Hold Time after $\overline{DOUT}$↑	t_{DOD}	100			ns	
$\overline{DOUT}$ Pulse Width (Low)	t_{DOL}	600			ns	
ALE → Data Input Valid Time	t_{LDV}			700	ns	
Address → Data Input Valid Time	t_{ADV}			900	ns	
$\overline{PSEN}$ Pulse Width (Low)	t_{PSL}	1200			ns	
$\overline{PSEN}$ → Data Input Valid Time	t_{PSDV}			600	ns	
$\overline{PSEN}$ → Data Float	t_{PSDF}	0			ns	

3

Port 1 I/O Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port 1 Output Setup Time to $\overline{STB}$↑	t_{PST}	200			ns	
Port 1 Output Hold Time after $\overline{STB}$↑	t_{STP}	100			ns	Port Output Mode
$\overline{STB}$ Pulse Width (Low)	t_{STL_1}	600			ns	
Output Data Setup Time to $\overline{STB}$↑	t_{DST}	300			ns	
Output Data Hold Time after $\overline{STB}$↑	t_{STD}	100			ns	
$\overline{STB}$↓ → Input Data Valid Time	t_{STDV}			850	ns	
$\overline{STB}$↓ → Input Data Float Time	t_{STDF}	0			ns	
Control Setup Time to $\overline{STB}$↓	t_{CST}	200			ns	I/O Expander Mode
Control Hold Time after $\overline{STB}$↓	t_{STC}	100			ns	
$\overline{STB}$ Pulse Width (Low)	t_{STL_2}	1200			ns	
$\overline{CSOUT}$ Setup Time to $\overline{STB}$↓	t_{CSST}	200			ns	
$\overline{CSOUT}$ Hold Time after $\overline{STB}$↓	t_{STCS}	100			ns	

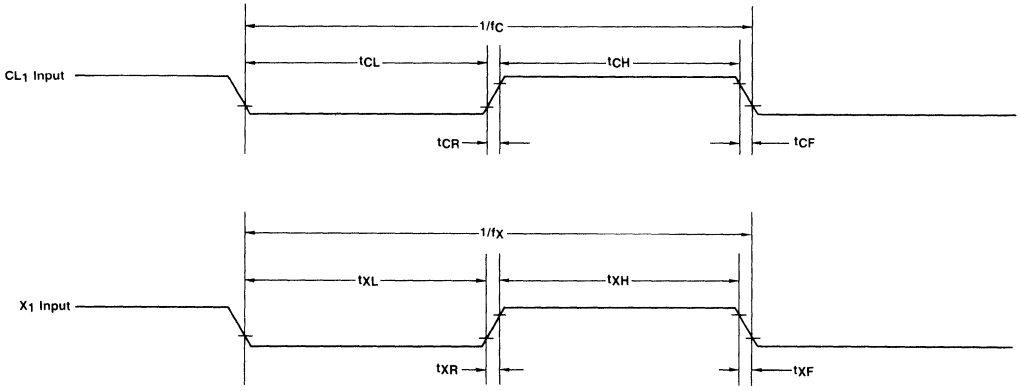
Serial Interface Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ Cycle Time	t_{KCY}	4.0			μs	Input
		6.7			μs	Output
$\overline{SCK}$ Pulse Width High	t_{KH}	1.8			μs	Input
		3.0			μs	Output
$\overline{SCK}$ Pulse Width Low	t_{KL}	1.8			μs	Input
		3.0			μs	Output
SI Setup Time to $\overline{SCK}$↑	t_{SIK}	300			ns	
SI Hold Time after $\overline{SCK}$↑	t_{KSI}	450			ns	
SO Output Delay after $\overline{SCK}$↑	t_{KSO}			850	ns	

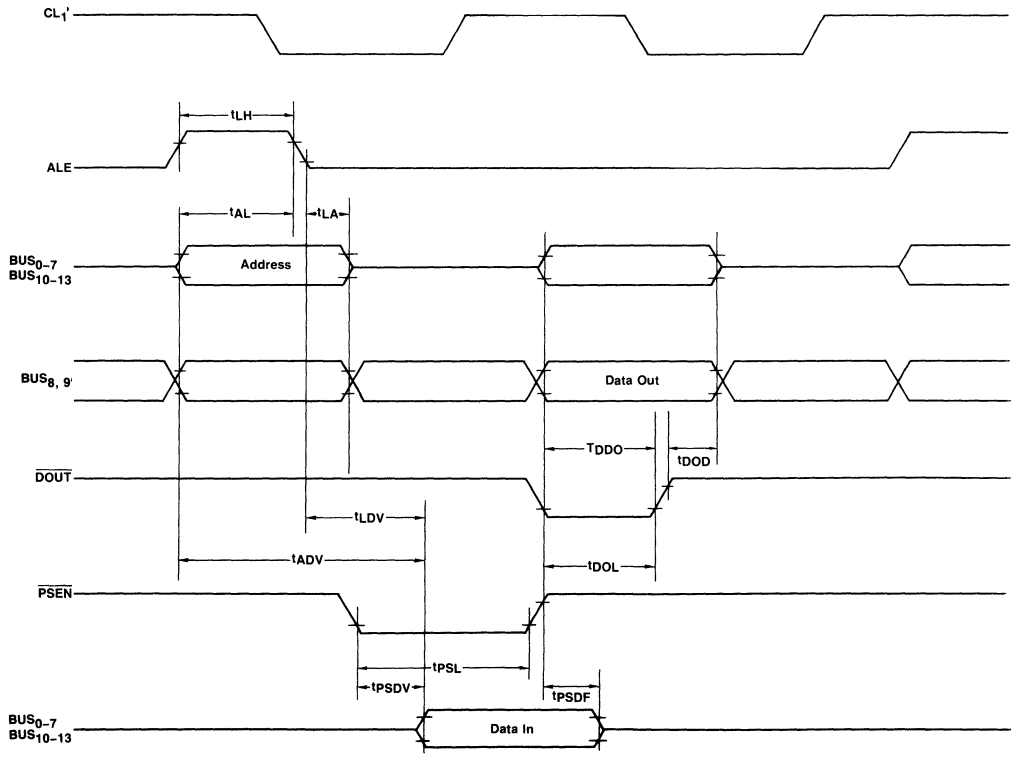
Other Operations

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
INT_0 Pulse Width High	t_{I_0H}	10			μs	
INT_0 Pulse Width Low	t_{I_0L}	10			μs	
INT_1 Pulse Width High	t_{I_1H}	$2/f_\phi$			μs	
INT_1 Pulse Width Low	t_{I_1L}	$2/f_\phi$			μs	
INT_2 Pulse Width High	t_{I_2H}	$2/f_\phi$			μs	
INT_2 Pulse Width Low	t_{I_2L}	$2/f_\phi$			μs	
RESET Pulse Width High	t_{RSH}	10			μs	
RESET Pulse Width Low	t_{RSL}	10			μs	

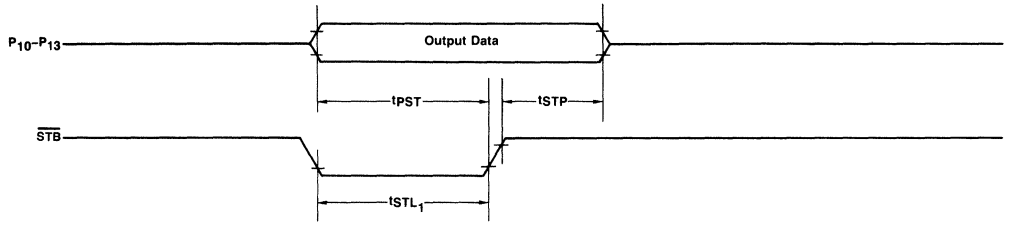
Clock Timing Waveforms



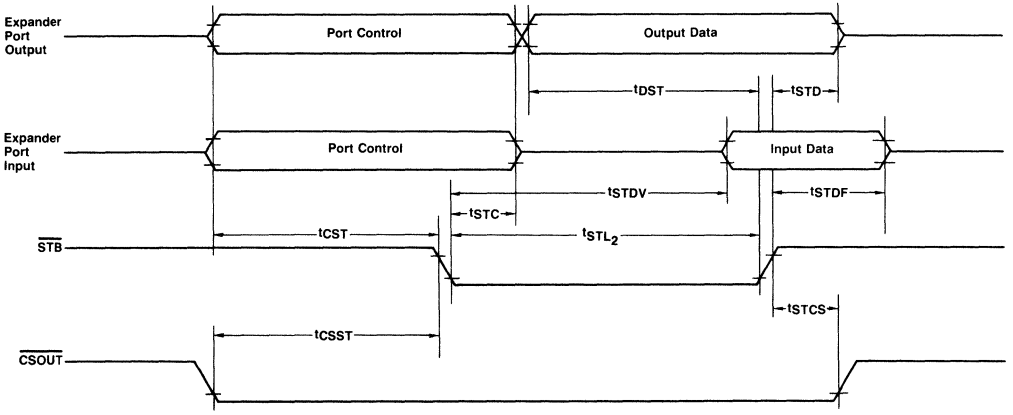
Bus I/O Timing Waveforms



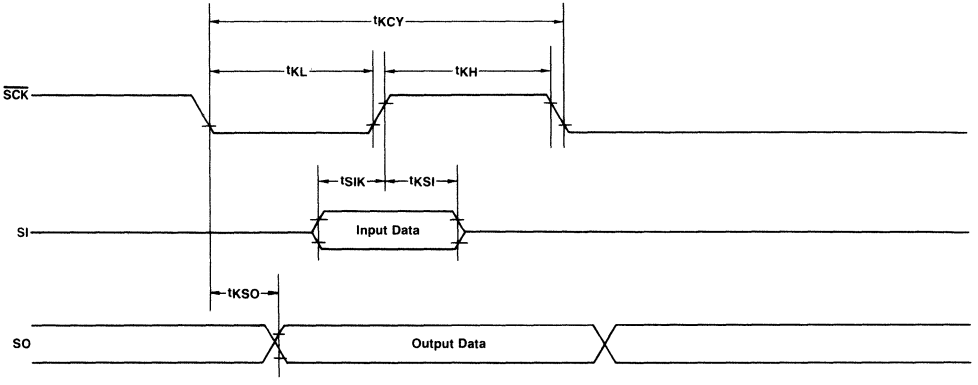
Strobe Output Timing Waveforms



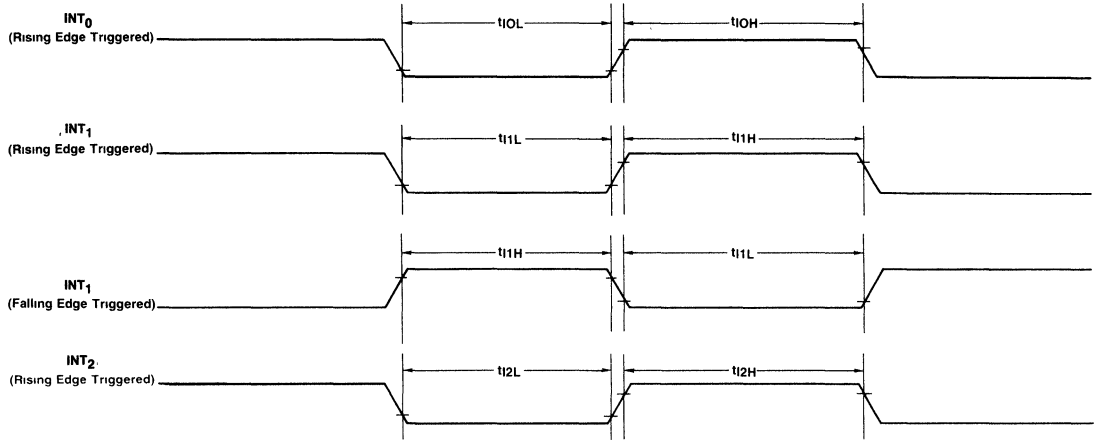
Port 1 I/O Expander Port Timing Waveforms



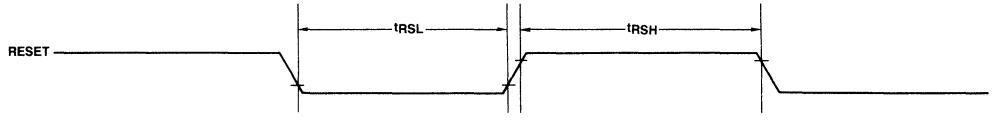
Serial Interface Timing Waveforms



Interrupt Input Timing Waveforms



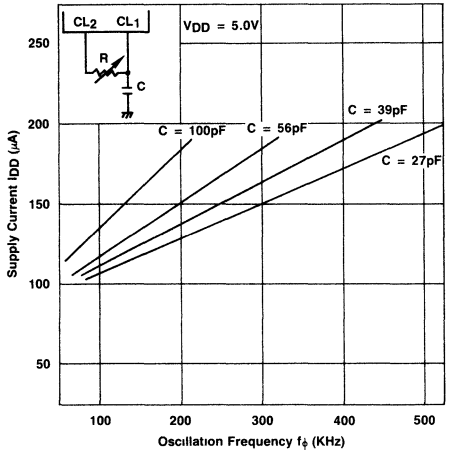
RESET Input Timing



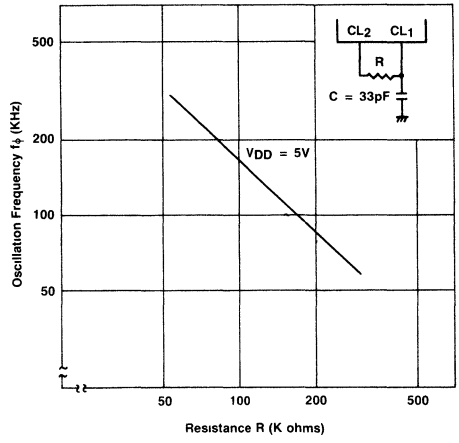
Operating Characteristics

Typical, T_a = 25°C

Supply Current vs System Clock Oscillation Frequency (Note ①)



System Clock Oscillation Frequency vs Resistance



Note:

① Only R/C system clock is operating and consuming power. All other internal logic blocks are not active

Package Outlines

For information, see Package Outline Section 7.

Plastic Quil, μPD7500G Evaluation Chip

HYBRID UV EPROM
4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The MC-430P is a hybrid chip containing a μPD556B ROM-less Evaluation chip, a μPD2716 2K x 8-bit UV EPROM, a μPC7905 3-terminal voltage regulator, and pull-up resistors on the same ceramic substrate. The MC-430P is pin-compatible with the μPD546C/μPD547C, and can emulate the high-voltage drive or CMOS μCOM-4 microcomputers with the corresponding I/O line buffers.

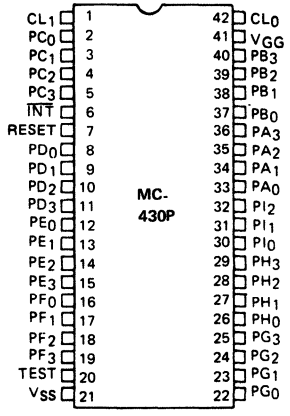
The MC-430P contains a 2048 x 8-bit UV EPROM and a 96 x 4-bit RAM which includes six working registers and the flag register. It has a level-triggered hardware interrupt, a three-level stack, and a programmable 6-bit timer. The MC-430P executes all 80 instructions of the extended μCOM-4 family instruction set.

The MC-430P provides 35 I/O lines organized into the 4-bit input ports A and B, the 4-bit I/O ports C and D, the 4-bit output ports E, F, G, and H, and the 3-bit output port I. It typically executes its instructions with a 10 μs instruction cycle time. The MC-430P is manufactured with a standard PMOS process, allowing use of a single −10V power supply, and is available in a 42-pin dual-in-line ceramic hybrid package.

3

PIN CONFIGURATION

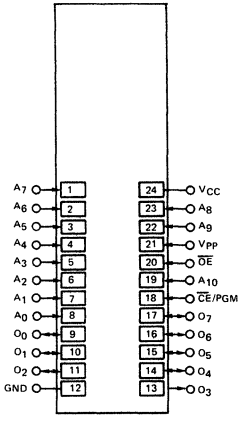
MC-430P (PIN COMPATIBLE WITH μPD546/μPD547)



PIN NAMES

PA_0-PA_3	Input Port A
PB_0-PB_3	Input Port B
PC_0-PC_3	Input/Output Port C
PD_0-PD_3	Input/Output Port D
PE_0-PE_3	Output Port E
PF_0-PF_3	Output Port F
PG_0-PG_3	Output Port G
PH_0-PH_3	Output Port H
PI_0-PI_2	Output Port I
$\overline{INT}$	Interrupt Input
CL_0-CL_1	External Clock Signals
RESET	Reset
V_{GG}	Power Supply Negative
V_{SS}	Power Supply Positive
TEST	Factory Test Pin (Connect to V_{SS})

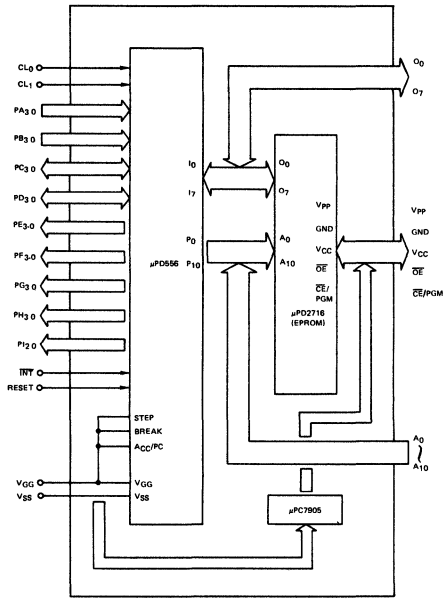
EPROM WRITE PADS (μPD2716)

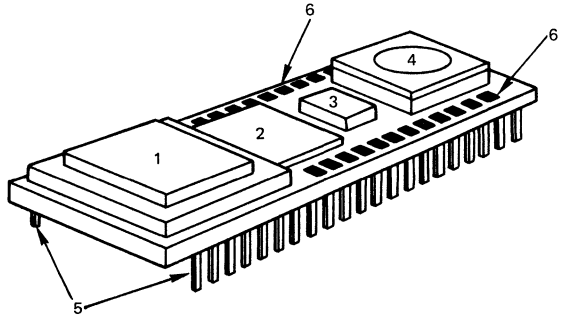


PIN NAMES

A_0-A_{10}	Addresses
$\overline{OE}$	Output Enable
O_0-O_7	Data Outputs
$\overline{CE}$/PGM	Chip Enable/Program

BLOCK DIAGRAM





1 : μPD556
2 : Pull-Up Resistors
3 : μPC7905 (3-Terminal 5 Volt Voltage Regulator)
4 : μPD2716 (EPROM)
5 : μPD546C/μPD547C Compatible Pins (42 Pins)
6 : EPROM Write Pads (24 Pads)

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−25°C to +85°C
Supply Voltage, V_{GG}	−15 to +0.3V
Input Voltages	−15 to +0.3V
Output Voltages	−15 to +0.3V
Output Current (Total, all ports)	−4 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MC-430P 42-PIN OPERATING SPECIFICATIONS

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Voltage High	V_{IH}	0		−2.0	V	Ports A through D, $\overline{INT}$, RESET
Input Voltage Low	V_{IL}	−4.3		V_{GG}	V	Ports A through D, $\overline{INT}$, RESET
Clock Voltage High	$V_{\phi H}$	0		−0.8	V	CL_0 Input, External Clock
Clock Voltage Low	$V_{\phi L}$	−6.0		V_{GG}	V	CL_0 Input, External Clock
Input Leakage Current High	I_{LIH}			+10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = −1V
Input Leakage Current Low	I_{LIL}			−10	μA	Ports A through D, $\overline{INT}$, RESET, V_I = −11V
Clock Input Leakage Current High	$I_{L\phi H}$			+200	μA	CL_0 Input, $V_{\phi H}$ = 0V
Clock Input Leakage Current Low	$I_{L\phi L}$			−200	μA	CL_0 Input, $V_{\phi L}$ = −11V
Output Voltage High	V_{OH_1}			−1.0	V	Ports C through I, I_{OH} = −1.0 mA
	V_{OH_2}			−2.3	V	Ports C through I, I_{OH} = −3.3 mA
Output Leakage Current Low	I_{LOL}			−10	μA	Ports C through I, V_O = −11V
Supply Current	I_{GG}		−110	−165	mA	

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%

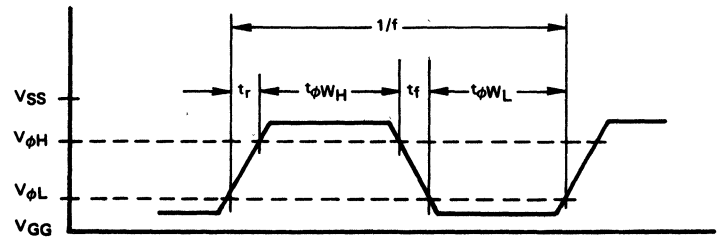
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Oscillator Frequency	f	150		440	KHz	
Rise and Fall Times	t_r, t_f	0		0.3	μs	EXTERNAL CLOCK
Clock Pulse Width High	$t_{\phi W_H}$	0.5		5.6	μs	
Clock Pulse Width Low	$t_{\phi W_L}$	0.5		5.6	μs	

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pF	f = 1 MHz
Output Capacitance	C_O			40	pF	
Input/Output Capacitance	C_{IO}			30	pF	

CLOCK WAVEFORM



MC-430P 24-PAD
μPD2716 UV-EPROM
PROGRAMMING SPECIFICATIONS

DC CHARACTERISTICS

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C, V_{CC} ① = +5V ± 5%, V_{PP} ①② = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2 0		V_{cc} +1	V	
Input Low Voltage	V_{IL}	-0 1		+0 8	V	
Input Leakage Current	I_{IL}			±10	μA	V_{IN} = 5 25V/0.45V
V_{PP} Current	I_{PP1}			+5	mA	$\overline{CE}/PGM = V_{IL}$ Program Verify / Program Inhibit
	I_{PP2}			+30	mA	$\overline{CE}/PGM = V_{IH}$ Program Mode
V_{CC} Current'	I_{CC}			+100	mA	

AC CHARACTERISTICS

PROGRAM, PROGRAM VERIFY AND PROGRAM INHIBIT MODE

T_a = 25°C ± 5°C, V_{CC} ① = +5V ± 5%, V_{PP} ①② = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	$\overline{CE}/PGM = V_{IL}$
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}/PGM = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

Test Conditions

Input Pulse Levels . 0 8V to 2 2V Output Timing Reference Level 0.8V and 2V
Input Timing Reference Level. . 1V and 2V

Notes ① V_{CC} must be applied simultaneously or before Vpp and removed after Vpp

② During programming, program inhibit, and program verify, a maximum of +26V should be applied to the Vpp pin Overshoot voltages to be generated by the Vpp power supply should be limited to less than +26V

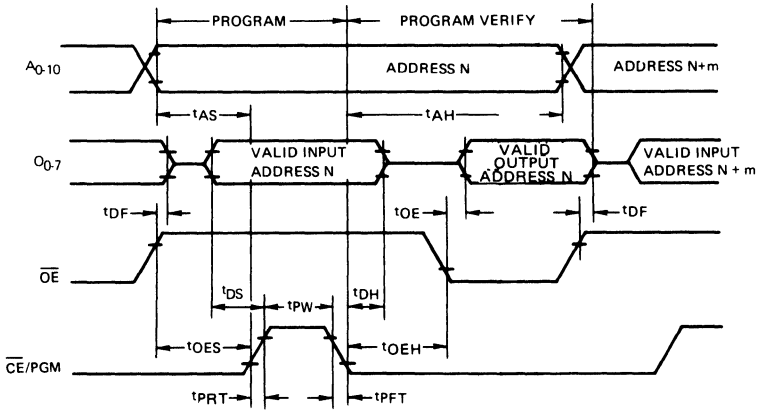
CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			60	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}			45	pF	V_{OUT} = 0V

TIMING WAVEFORM

PROGRAM MODE



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Package Outlines

For information, see Package Outline Section 7.

Cerdip, MC-430PD

NEC

SINGLE CHIP 8-BIT MICROCOMPUTERS

4

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER ROM-LESS DEVELOPMENT DEVICE

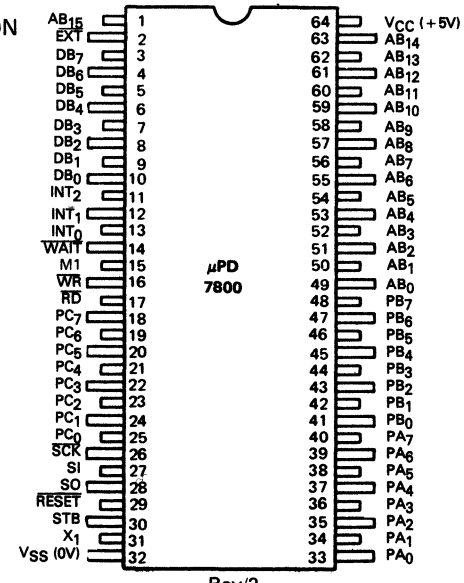
DESCRIPTION

The NEC μPD7800 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-channel Silicon Gate MOS Technology. Intended as a ROM-less development device for NEC μPD7801/7802 designs, the μPD7800 can also be used as a powerful microprocessor in volume production enabling program memory flexibility. Basic on-chip functional blocks include 128 bytes of RAM data memory, 8-bit ALU, 32 I/O lines, Serial I/O port, and 12-bit timer. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of 8080A/8085A peripheral and memory products. Total memory address space is 64K bytes.

FEATURES

- NMOS Silicon Gate Technology Requiring Single +5V Supply.
- Single-Chip Microcomputer with On-Chip ALU, RAM and I/O
  - 128 Bytes RAM
  - 32 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five-Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 64K Byte Memory Address Range
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes; Including Auto-Increment/Decrement
- Multi-Level Stack-Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog, Inc.

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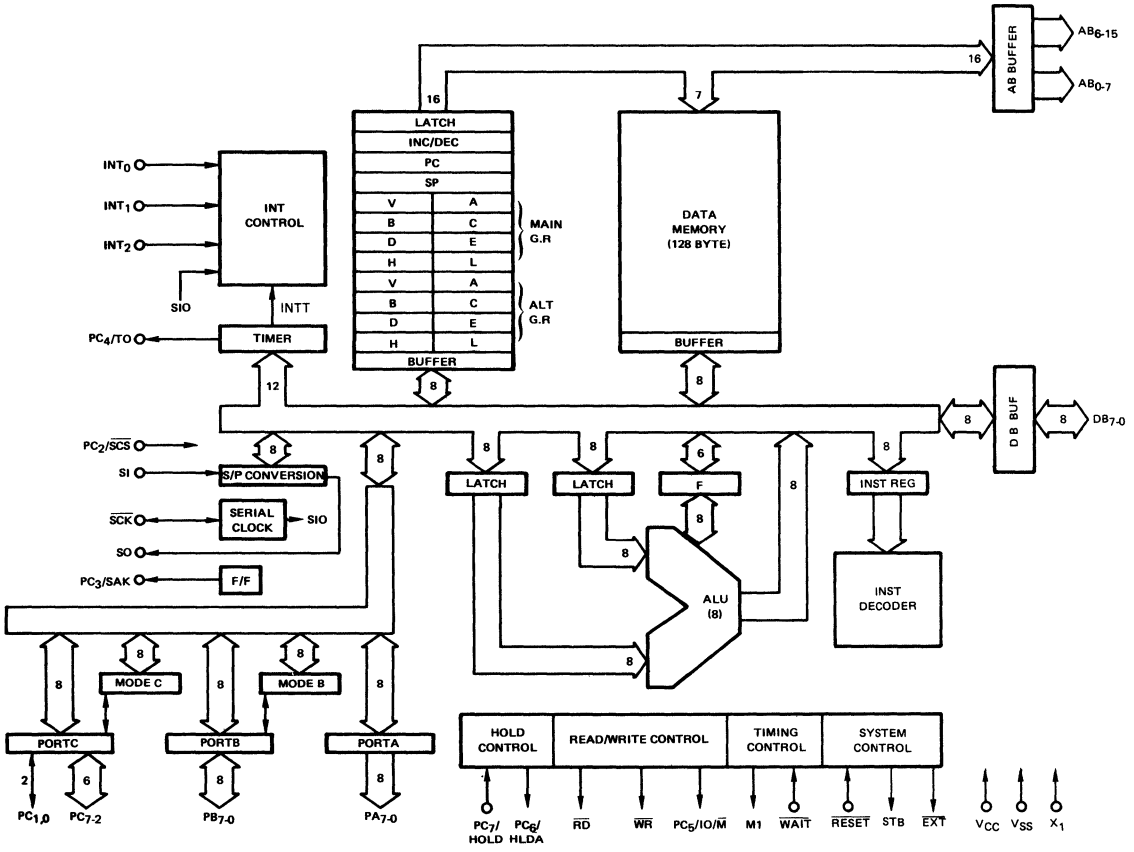
PIN DESCRIPTION

PIN NO	DESIGNATION	FUNCTION
1, 49-63	AB_0-AB_{15}	(Tri-State, Output) 16-bit address bus.
2	$\overline{EXT}$	(Output) $\overline{EXT}$ is used to simulate μPD7801/7802 external memory reference operation. $\overline{EXT}$ distinguishes between internal and external memory references, and goes low when locations 4096 through 65407 are accessed.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices on the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of $\overline{SCK}$.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of $\overline{SCK}$, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7800.
30	STB	(Output) Used to simulate μPD7801/7802 Port E operation, indicating that a Port E operation is being performed when active.
31	X_1	(Input) Clock Input
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

BLOCK DIAGRAM



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Architecturally consistent with μPD7801/7802 devices, the μPD7800 uses a slightly different pin-out to accommodate for the address bus and lack of on-chip clock generator. For complete μPD7800 functional operation, please refer to μPD7801 product information. Listed below are functional differences that exist between μPD7800 and μPD7801 devices.

μPD7800/7801 Functional Differences

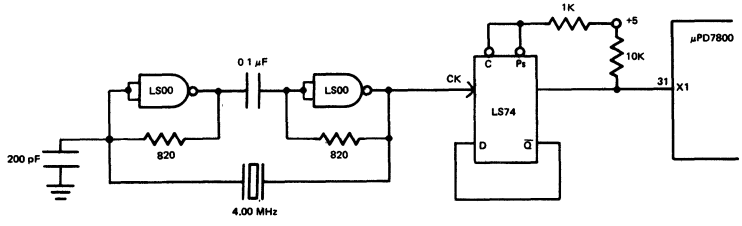
1. The functionality of μPD7801 Port E is somewhat different on the μPD7800. Because the μPD7800 contains no program memory, the address bus is made accessible to address external program memory. Thus, lines normally used for Port E operation with the μPD7801 are used as the address bus on the μPD7800. AB_0-AB_{15} is active during memory access 0 through 4095.
2. Consequently Port E instructions (PEX, PEN, and PER) have different functionality.

   PEX Instruction – The contents of B and C register are output to the address bus. The value 01H is output to the data bus. STB becomes active.

   PEN Instruction – B and C register contents are output to the address bus. The value 02H is output to the data bus. STB becomes active.

   PER Instruction – The address bus goes to the high impedance state. The value 04H is output to the data bus. STB becomes active.
3. ON-CHIP CLOCK GENERATOR. The μPD7800 contains no internal clock generator. An external clock source is input to the X_1 input.
4. PIN 30. This pin functions as the X_2 crystal connection on the μPD7801. On the μPD7800, pin 30 functions as a strobe output (STB) and becomes active when a Port E instruction is executed. This control signal is useful in simulating μPD7801 Port E operation – indicating that a port E operation is being performed.
5. PIN 2. Functions as the Φ out clock output used for synchronizing system external memory and I/O devices, on the μPD7801. On the μPD7800, this pin is used to simulate external memory reference operation of the μPD7801. $\overline{EXT}$ is used to distinguish between internal and external memory references and goes low when location 4096 through 65407 are accessed.

RECOMMENDED CLOCK DRIVE CIRCUIT



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... −10°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin ..... −0.3V to +7.0V

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C ~ +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0 45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

AC CHARACTERISTICS

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X_{OUT} Cycle Time	t_{CYX}	454	2000	ns	t_{CYX}
X_{OUT} Low Level Width	t_{XXL}	212		ns	t_{XXL}
X_{OUT} High Level Width	t_{XXH}	212		ns	t_{XXH}

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → X_{OUT} L.E.	t_{RX}	20		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	$200_{(T3)}$; $700_{(T4)}$		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → WAIT L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from X_{OUT} L.E.)	t_{WTS}	180		ns	
$\overline{WAIT}$ Hold Time (Referenced from X_{OUT} L.E.)	t_{WTH}	0	120	ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	t_{CYX} = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
X_{OUT} L.E. → WR L.E.	t_{XW}		270	ns	
Address (PE_{0-15}) → X_{OUT} T.E.	t_{AX}		300	ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS (CONT.)

SERIAL I/O OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	80		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

PEN, PEX, PER OPERATION

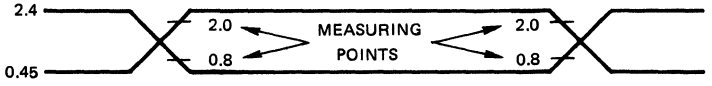
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
X_1 L.E. → $\overline{EXT}$	t_{XE}		250	ns	
Address (AB_{0-15}) → STB L.E.	t_{AST}	200			
Data (DB_{0-7}) → STB L.E.	t_{DST}	200			t_{CYX} = 500 ns
STB Hold Time	t_{STST}	300			
STB → Data	t_{STD}	400			

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from X_{OUT} L.E.)	t_{HDS_1}	100		ns	
	t_{HDS_2}	100		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	100		ns	
X_{OUT} L.E. → HLDA	t_{XHA}		100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

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AC CHARACTERISTICS (CONT.)

t_{CYX} DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
t_{RX}	(1/25) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MIN	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
t_{XW}	(27/50) T	MAX	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns
t_{AST}	(2/5) T	MIN	ns
t_{DST}	(2/5) T	MIN	ns
t_{STST}	(3/5) T	MIN	ns
t_{STD}	(4/5) T	MIN	ns

Notes: ① N = Number of Wait States

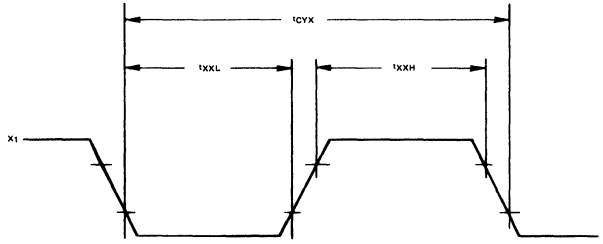
② T = t_{CYX}

③ Only above parameters are t_{CYX} dependent

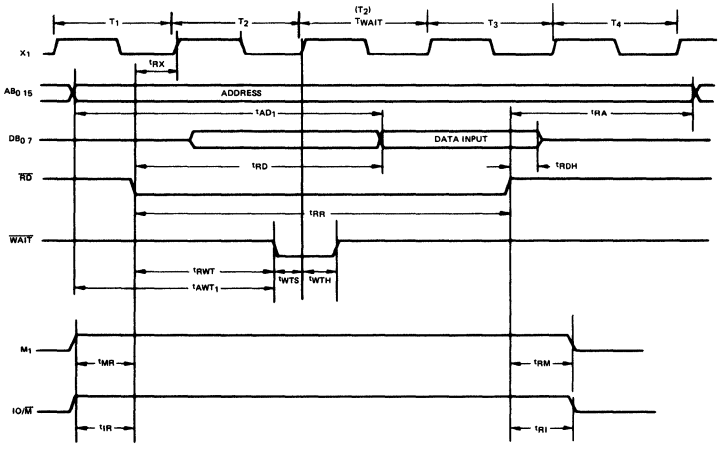
④ When a crystal frequency other than 4 MHz is used (t_{CYX} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

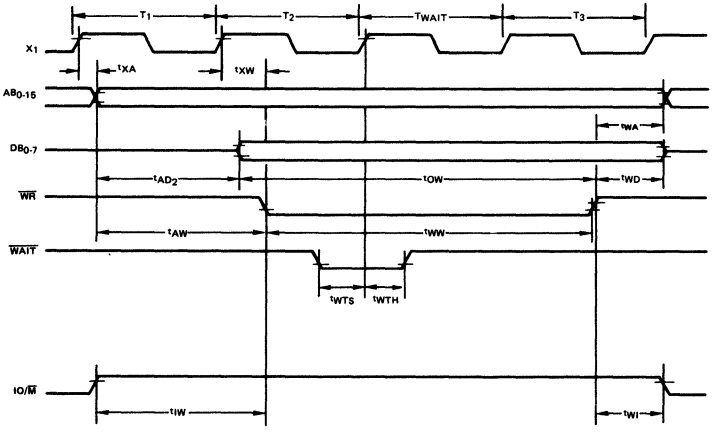
CLOCK TIMING



READ OPERATION



WRITE OPERATION



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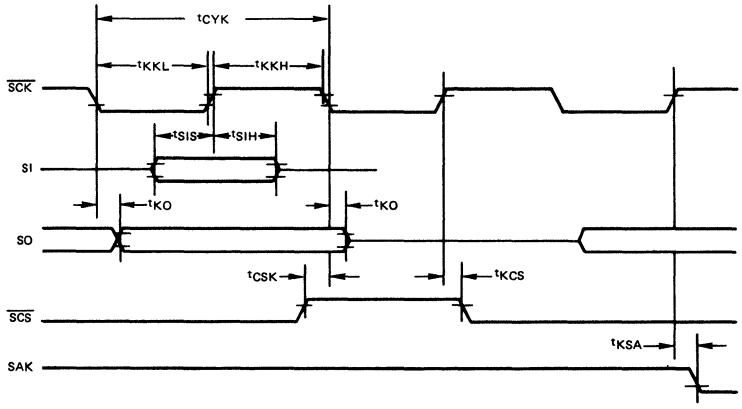
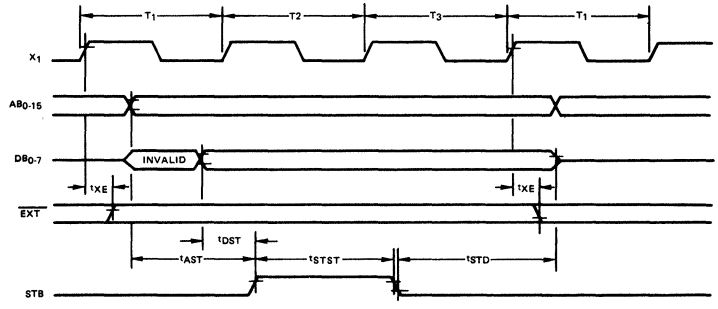
TIMING WAVEFORMS (CONT.)

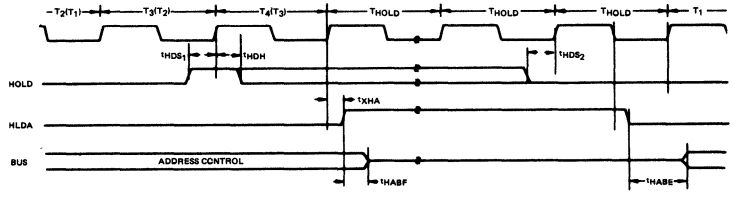
SERIAL I/O OPERATION



PEN, PEX, PER OPERATION



HOLD OPERATION



Package Outlines

For information, see Package Outline Section 7.

Plastic Quil, μPD7800G

HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH 4K ROM

PRODUCT DESCRIPTION

The NEC μPD7801/7802 is an advanced 8-bit general purpose single-chip microcomputer fabricated with N-Channel Silicon Gate MOS technology

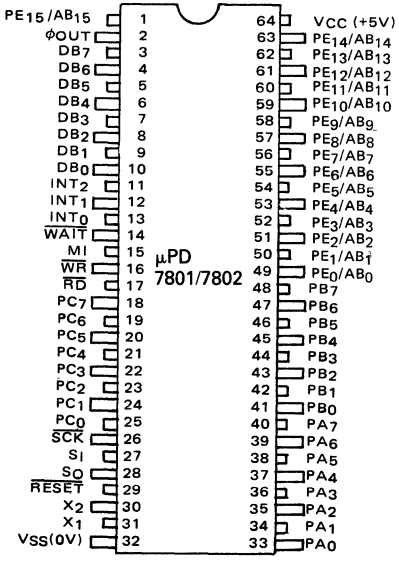
The NEC μPD7801/7802 is intended to serve a broad spectrum of 8-bit designs ranging from enhanced single chip applications extending into the multi-chip microprocessor range. All the basic functional blocks – 8-bit ALU, 48 I/O lines, Serial I/O port, 12-bit timer, and clock generator are provided on-chip to enhance stand-alone applications. Fully compatible with the industry standard 8080A bus structure, expanded system operation can be easily implemented using any of the 8080A/8085A peripherals and memory products. Total memory space can be increased to 64K bytes.

The powerful 140 instruction set coupled with 4K bytes of ROM program memory and 128 bytes of RAM data memory greatly extends the range of single chip microcomputer applications. Five level vectored interrupt capability combined with a 2 microsecond cycle time enable the μPD7801 to compete with multi-chip microprocessor systems with the advantage that most of the support functions are on-chip.

FEATURES

- NMOS Silicon Gate Technology Requiring +5V Supply
- Complete Single-Chip Microcomputer with On-Chip ROM, RAM and I/O
  - 4K Bytes ROM-7801
  - 128 Bytes RAM
  - 6K Bytes-7802
  - 64 Bytes-7802
  - 48 I/O Lines
- Internal 12-Bit Programmable Timer
- On-Chip 1 MHz Serial Port
- Five Level Vectored, Prioritized Interrupt Structure
  - Serial Port
  - Timer
  - 3 External Interrupts
- Bus Expansion Capabilities
  - Fully 8080A Bus Compatible
  - 60K Bytes External Memory Address Range-7801
  - 58K Bytes-7802
- On-Chip Clock Generator
- Wait State Capability
- Alternate Z80™ Type Register Set
- Powerful 140 Instruction Set
- 8 Address Modes, Including Auto-Increment/Decrement
- Multi-Level Stack Capabilities
- Fast 2 μs Cycle Time
- Bus Sharing Capabilities

PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog, Inc.

Rev/2

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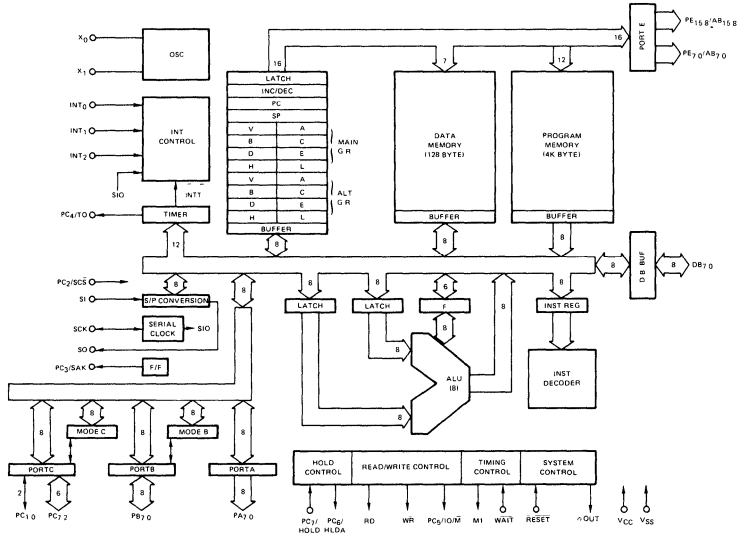
PIN DESCRIPTION

PIN NO.	DESIGNATION	FUNCTION
49-63	PE_0/AB_0-	(Tri-State, Output) 16-bit address bus.
1	PE_{15}/AB_{15}	
2	ϕOUT	(Output) ϕOUT provides a prescaled output clock for use with external I/O devices or memories. ϕOUT frequency is $f_{XTAL}/2$.
3-10	DB_0-DB_7	(Tri-State Input/Output, active high) 8-bit true bi-directional data bus used for external data exchanges with I/O and memory.
11	INT_0	(Input, active high) Level-sensitive interrupt input.
12	INT_1	(Input, active high) Rising-edge sensitive interrupt input. Interrupts are initiated on low-to-high transitions, providing interrupts are enabled.
13	INT_2	(Input) INT_2 is an edge sensitive interrupt input where the desired activation transition is programmable. By setting the ES bit in the Mask Register to a 1, INT_2 is rising edge sensitive. When ES is set to 0, INT_2 is falling edge sensitive.
14	$\overline{WAIT}$	(Input, active low) $\overline{WAIT}$, when active, extends read or write timing to interface with slower external memory or I/O. $\overline{WAIT}$ is sampled at the end of T_2, if active processor enters a wait state TW and remains in that state as long as $\overline{WAIT}$ is active.
15	M1	(Output, active high) when active, M1 indicates that the current machine cycle is an OP CODE FETCH.
16	$\overline{WR}$	(Tri-State Output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes to the high impedance state during HALT, HOLD, or RESET.
17	$\overline{RD}$	(Tri-State Output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes to the high impedance state during HALT, HOLD, and RESET.
18-25	PC_0-PC_7	(Input/Output) 8-bit I/O configured as a nibble I/O port or as control lines.
26	$\overline{SCK}$	(Input/Output) $\overline{SCK}$ provides control clocks for Serial Port Input/Output operations. Data on the SI line is clocked into the Serial Register on the rising edge. Contents of the Serial Register is clocked onto SO line on falling edges.
27	SI	(Input) Serial data is input to the processor through the SI line. Data is clocked into the Serial Register MSB to LSB with the rising edge of SCK.
28	SO	(Output) SO is the Serial Output Port. Serial data is output on this line on the falling edge of SCK, MSB to LSB.
29	$\overline{RESET}$	(Input, active low) $\overline{RESET}$ initializes the μPD7801.
30	X_2	(Output) Oscillator output.
31	X_1	(Input) Clock Input.
33-40	PA_0-PA_7	(Output) 8-bit output port with latch capability.
41-48	PB_0-PB_7	(Tri-State Input/Output) 8-bit programmable I/O port. Each line configurable independently as an input or output.

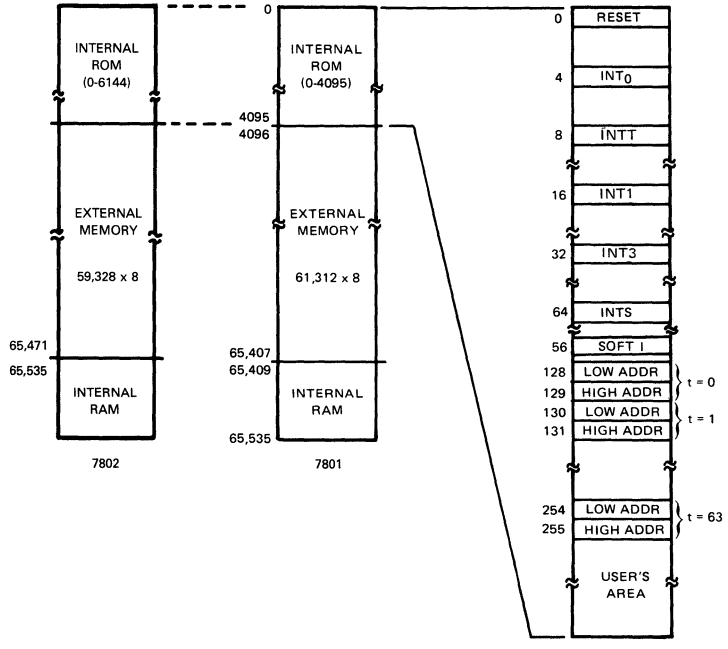
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Memory Map

The μPD7801/7802 can directly address up to 64K bytes of memory. Except for the on-chip ROM and RAM, any memory location can be used as either ROM or RAM. The following memory map defines the 0-64K byte memory space for the μPD7801/7802 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the internal ROM area.



I/O Ports

PORT	FUNCTIONS
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port w/latch
Port C	8-bit nibble I/O or Control port
Port E	16-bit Address/Output Port

Port A

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using Arithmetic and logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B

Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output modes. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_{n=1}$) or an Output (Mode $B_{n=0}$).

Port C

Port C is an 8-bit I/O port. The Mode C register is used to program the upper 6 bits of Port C to provide control functions or to set the I/O structure per the following table.

	MODE $C_n = 0$	MODE $C_n = 1$
PC_0	Output	Input
PC_1	Output	Input
PC_2	$\overline{SCS}$ Input	Input
PC_3	SAK Output	Output
PC_4	To Output	Output
PC_5	IO/$\overline{M}$ Output	Output
PC_6	HLDA Output	Output
PC_7	HOLD Input	Input

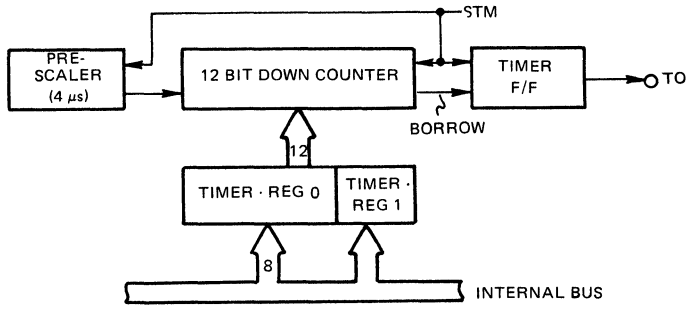
Port E

Port E is a 16-bit address bus/output port. It can be set to one of three operating modes using the PER, PEN, or PEX instructions.

- 16-Bit Address Bus – the Per instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 4-Bit Output Port/12 Bit Address Bus – the PEN instruction sets this mode which allows for memory expansion of up to 4K bytes, externally, plus the transfer of 4-bit nibbles.
- 16-Bit Output Port – the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_{8-15} and PE_{0-7}, respectively.

FUNCTIONAL DESCRIPTION (CONT.)

Timer Operation



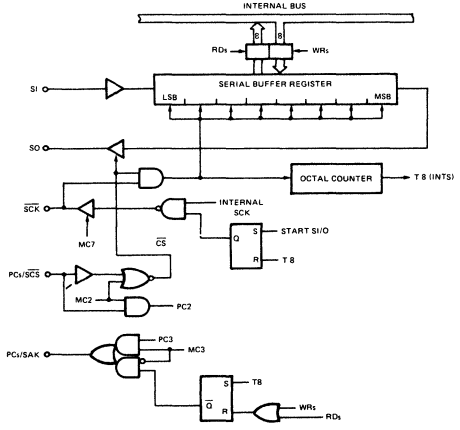
TIMER BLOCK DIAGRAM

A programmable 12-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 4 μs to 16 μs in duration. The timer consists of a prescaler which decrements a 12-bit counter at a fixed 4 μs rate. Count pulses are loaded into the 12-bit down counter through timer register (TM0 and TM1). Count-down operation is initiated upon extension of the STM instruction when the contents of the down counter are fully decremented and a borrow operation occurs, an interval interrupt (INTT) is generated. At the same time, the contents of TM0 and TM1 are reloaded into the down-counter and countdown operation is resumed. Count operation may be restarted or initialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the down counter.

The timer flip flop is set by the STM instruction and reset on a countdown operation. Its output (TO) is available externally and may be used in a single pulse mode or general external synchronization.

Timer interrupt (INTT) may be disabled through the interrupt.

Serial Port Operation



SERIAL PORT BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION (CONT.)

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD7801/7802 to serially interface with external devices.

Serial Transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 1 Mbit/second if the internal clock is used or is variable between DC and 1 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select Signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Serial Acknowledge (SAK) goes high when data transfers between the accumulator and Serial Register is completed. SAK goes low when the buffer becomes full after the completion of serial data receive or transmit operations. While SAK is low, no further data can be received.

Interrupt Structure

The μPD7801/7802 provides a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources; three external interrupts, two internal interrupts, and non-maskable software interrupt. Each interrupt when activated branches to a designated memory vector location for that interrupt.

INT	VECTORED MEMORY LOCATION	PRIORITY	TYPE
INTT	8	3	Internal, Timer Overflow
INTS	64	6	Internal, Serial Buffer Full/Empty
INT0	4	2	Ext., level sensitive
INT1	16	4	Ext., Rising edge sensitive
INT2	32	5	Ext., Rising/Falling edge sensitive
SOFTI	96	1	Software Interrupt

FUNCTIONAL DESCRIPTION (CONT.)

$\overline{\text{RESET}}$ (Reset)

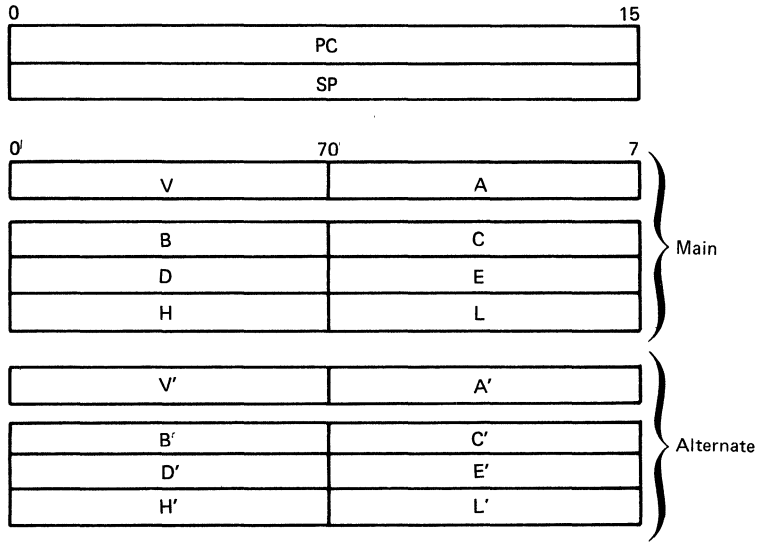
An active low-signal on this input for more than 4 μs forces the μPD7801 into a Reset condition. $\overline{\text{RESET}}$ affects the following internal functions:

- The Interrupt Enable Flags are reset, and Interrupts are inhibited.
- The Interrupt Request Flag is reset.
- The HALT flip flop is reset, and the Halt-state is released.
- The contents of the MODE B register are set to FF_H, and Port B becomes an input port.
- The contents of the MODE C register are set to FF_H. Port C becomes an I/O port and output lines go low.
- All Flags are reset to 0.
- The internal COUNT register for timer operation is set to FFF_H and the timer F/F is reset.
- The ACK F/F is set.
- The HLDA F/F is reset.
- The contents of the Program Counter are set to 0000_H.
- The Address Bus (PE_{0-15}), Data Bus (DB_{0-7}), $\overline{\text{RD}}$, and $\overline{\text{WR}}$ go to a high impedance state.

Once the $\overline{\text{RESET}}$ input goes high, the program is started at location 0000_H.

REGISTERS

The μPD7801 contains sixteen 8-bit registers and two 16-bit registers.



General Purpose Registers (B, C, D, E, H, L)

There are two sets of general purpose registers (Main: B, C, D, E, H, L: Alternate: B', C', D', H', L'). They can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL, B'C', D'E', H'L'). Auto Increment and Decrement addressing mode capabilities extend the uses for the DE, HL, D'E', and H'L' register-pairs. The contents of the BC, DE, and HL register-pairs can be exchanged with their Alternate Register counterparts using the EXX instruction.

FUNCTIONAL DESCRIPTION (CONT.)

Vector Register (V)

When defining a scratch pad area in the memory space, the upper 8-bit memory address is defined in the V-register and the lower 8-bits is defined by the immediate data of an instruction. Also the scratch pad indicated by the V-register can be used as 256 x 8-bit working registers for storing software flags, parameters and counters.

Accumulator (A)

All data transfers between the μPD7801/7802 and external memory or I/O are done through the accumulator. The contents of the Accumulator and Vector Registers can be exchanged with their Alternate Registers using the EX instruction.

Program Counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

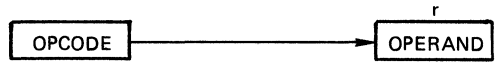
Stack Pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in-first-out). The contents of the SP are decremented during a CALL or PUSH instruction or if an interrupt occurs. The SP is incremented during a RETURN or POP instruction.

ADDRESS MODES

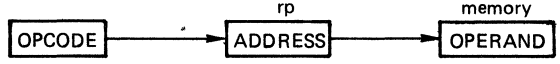
Register Addressing	Working Register Addressing
Register Indirect Addressing	Direct Addressing
Auto-Increment Addressing	Immediate Addressing
Auto-Decrement Addressing	Immediate Extended Addressing

Register Addressing



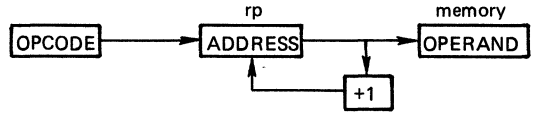
The instruction opcode specifies a register r which contains the operand.

Register Indirect Addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

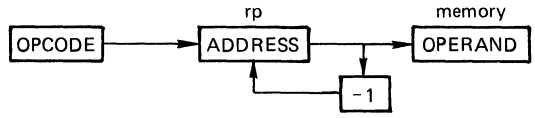
Auto-Increment Addressing



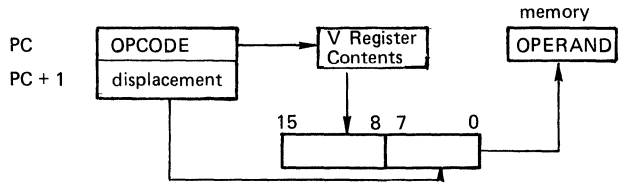
The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair is automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

ADDRESS MODES (CONT.)

Auto-Decrement Addressing

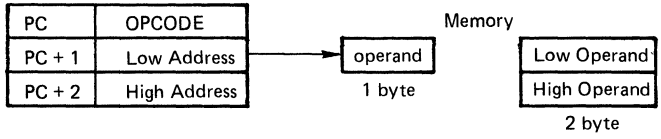


Working Register Addressing



The contents of the register is linked with the byte following the opcode to form a memory address whose contents is the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only 1 additional byte is required for the address. Mnemonics with a W suffix ending this address mode.

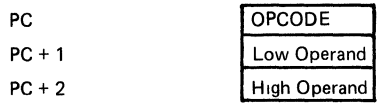
Direct Addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate Addressing

Immediate Extended Addressing



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Operand Description

OPERAND	DESCRIPTION
r	V, A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA PB PC MK MB MC TM0 TM1 S
sr1	PA PB PC MK S
sr2	PA PB PC MK
rp	SP, B, D, H
rp1	V, B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
wa	8 bit immediate data
word	16 bit immediate data
byte	8 bit immediate data
bit	3 bit immediate data
f	F0, F1, F2, FT, FS,

Notes:
1. When special register operands sr, sr1, sr2 are used; PA=Port A, PB=Port B, PC=Port C, MK=Mask Register, MB=Mode B Register, MC=Mode C Register, TM0=Timer Register 0, TM1=Timer Register 1, S=Serial Register.
2. When register pair operands rp, rp1 are used; SP=Stack Pointer, B=BC, D=DE, H=HL, V=VA.
3. Operands rPa, rPa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B=(BC), D=(DE), H=(HL)
   $D+=(DE)^+$, $H+=(HL)^+$, $D-=(DE)^-$, $H-=(HL)^-$.
4. When the interrupt operand f is used; F0=INTF0, F1=INTF1, F2=INTF2, FT=INTFT, FS=INTFS.

INSTRUCTION GROUPS

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
8-BIT DATA TRANSFER							
MOV	r1, A	1	4	r1 ← A			
MOV	A, r1	1	4	A ← r1			
MOV	sr, A	2	10	sr ← A			
MOV	A, sr1	2	10	A ← sr1			
MOV	r, word	4	17	r ← (word)			
MOV	word, r	4	17	(word) ← r			
MVI	r, byte	2	7	r ← byte			
MVIW	wa, byte	3	13	(V, wa) ← byte			
MVIX	rpa1, byte	2	10	(rpa1) ← byte			
STAW	wa	2	10	(V, wa) ← A			
LDAW	wa	2	10	A ← (V, wa)			
STAX	rpa	1	7	(rpa) ← A			
LDAX	rpa	1	7	A ← (rpa)			
EXX		1	4	Exchange register sets			
EX		1	4	V, A ↔ V, A			
BLOCK		1	13 (C+1)	$(DE)^+ \leftarrow (HL)^+$, C ← C − 1			
16-BIT DATA TRANSFER							
SBCD	word	4	20	(word) ← C, (word + 1) ← B			
SDED	word	4	20	(word) ← E, (word + 1) ← D			
SHLD	word	4	20	(word) ← L, (word + 1) ← H			
SSPD	word	4	20	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	20	C ← (word), B ← (word + 1)			
LDED	word	4	20	E ← (word), D ← (word + 1)			
LHLD	word	4	20	L ← (word), H ← (word + 1)			
LSPD	word	4	20	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	17	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	15	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	10	rp ← word			
TABLE		1	19	C ← (PC + 2 + A) B ← (PC + 2 + A + 1)			

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
ARITHMETIC							
ADD	A, r	2	8	A ← A + r		‡	‡
ADD	r, A	2	8	r ← r + A		‡	‡
ADDX	rpa	2	11	A ← A + (rpa)		‡	‡
ADC	A, r	2	8	A ← A + r + CY		‡	‡
ADC	r, A	2	8	r ← r + A + CY		‡	‡
ADCX	rpa	2	11	A ← A + (rpa) + CY		‡	‡
SUB	A, r	2	8	A ← A − r		‡	‡
SUB	r, A	2	8	r ← r − A		‡	‡
SUBX	rpa	2	11	A ← A − (rpa)		‡	‡
SBB	A, r	2	8	A ← A − r − CY		‡	‡
SBB	r, A	2	8	r ← r − A − CY		‡	‡
SBBX	rpa	2	11	A ← A − (rpa) − CY		‡	‡
ADDNC	A, r	2	8	A ← A + r	No Carry	‡	‡
ADDNC	r, A	2	8	r ← r + A	No Carry	‡	‡
ADDNCX	rpa	2	11	A ← A + (rpa)	No Carry	‡	‡
SUBNB	A, r	2	8	A ← A − r	No Borrow	‡	‡
SUBNB	r, A	2	8	r ← r − A	No Borrow	‡	‡
SUBNBX	rpa	2	11	A ← A − (rpa)	No Borrow	‡	‡
LOGICAL							
ANA	A, r	2	8	A ← A ∧ r			‡
ANA	r, A	2	8	r ← r ∧ A			‡
ANAX	rpa	2	11	A ← A ∧ (rpa)			‡
ORA	A, r	2	8	A ← A ∨ r			‡
ORA	r, A	2	8	r ← r ∨ A			‡
ORAX	rpa	2	11	A ← A ∨ (rpa)			‡
XRA	A, r	2	8	A ← A ∨̲ r			‡
XRA	r, A	2	8	A ← r ∨̲ A			‡
XRAX	rpa	2	11	A ← A ∨̲ (rpa)			‡
GTA	A, r	2	8	A − r − 1	No Borrow	‡	‡

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
LOGICAL (CONT.)							
GTAX	rpa	2	11	A – (rpa) – 1	No Borrow	‡	‡
LTA	A, r	2	8	A – r	Borrow	‡	‡
LTA	r, A	2	8	r – A	Borrow	‡	‡
LTAX	rpa	2	11	A – (rpa)	Borrow	‡	‡
ONA	A, r	2	8	A∧r	No Zero		‡
ONAX	rpa	2	11	A∧(rpa)	No Zero		‡
OFFA	A, r	2	8	A∧r	Zero		‡
OFFAX	rpa	2	11	A∧(rpa)	Zero		‡
NEA	A, r	2	8	A – r	No Zero	‡	‡
NEA	r, A	2	8	r – A	No Zero	‡	‡
NEAX	rpa	2	11	A – (rpa)	No Zero	‡	‡
EQA	A, r	2	8	A – r	Zero	‡	‡
EQA	r, A	2	8	r – A	Zero	‡	‡
EQAX	rpa	2	11	A – (rpa)	Zero	‡	‡
IMMEDIATE DATA TRANSFER (ACCUMULATOR)							
XRI	A, byte	2	7	A ← A ⊻ byte			‡
ADINC	A, byte	2	7	A ← A + byte	No Carry	‡	‡
SUINB	A, byte	2	7	A ← A – byte	No Borrow	‡	‡
ADI	A, byte	2	7	A ← A + byte		‡	‡
ACI	A, byte	2	7	A ← A + byte + CY		‡	‡
SUI	A, byte	2	7	A ← A – byte		‡	‡
SBI	A, byte	2	7	A ← A – byte – CY		‡	‡
ANI	A, byte	2	7	A ← A∧byte			‡
ORI	A, byte	2	7	A ← A∨byte			‡
GTI	A, byte	2	7	A – byte – 1	No Borrow	‡	‡
LTI	A, byte	2	7	A – byte	Borrow	‡	‡
ONI	A, byte	2	7	A∧byte	No Zero		‡
OFFI	A, byte	2	7	A∧byte	Zero		‡
NEI	A, byte	2	7	A – byte	No Zero	‡	‡
EQI	A, byte	2	7	A – byte	Zero	‡	‡

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER							
XRI	r, byte	3	11	r ← r ∀ byte			↕
ADINC	r, byte	3	11	r ← r + byte	No Carry	↕	↕
SUINB	r, byte	3	11	r ← r − byte	No Borrow	↕	↕
ADI	r, byte	3	11	r ← r + byte		↕	↕
ACI	r, byte	3	11	r ← r + byte + CY		↕	↕
SUI	r, byte	3	11	r ← r − byte		↕	↕
SBI	r, byte	3	11	r ← r − byte − CY		↕	↕
ANI	r, byte	3	11	r ← r ∧ byte		↕	↕
ORJ	r, byte	3	11	r ← r ∨ byte			↕
GTI	r, byte	3	11	r − byte − 1	No Borrow	↕	↕
LTI	r, byte	3	11	r − byte	Borrow	↕	↕
ONI	r, byte	3	11	r ∧ byte	No Zero		↕
OFFI	r, byte	3	11	r ∧ byte	Zero		↕
NEI	r, byte	3	11	r − byte	No Zero	↕	↕
EQI	r, byte	3	11	r − byte	Zero	↕	↕
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER)							
XRI	sr2, byte	3	17	sr2 ← sr2 ∀ byte			↕
ADINC	sr2, byte	3	17	sr2 ← sr2 + byte	No Carry	↕	↕
SUINB	sr2, byte	3	17	sr2 ← sr2 − byte	No Borrow	↕	↕
ADI	sr2, byte	3	17	sr2 ← sr2 + byte		↕	↕
ACI	sr2, byte	3	17	sr2 ← sr2 + byte + CY		↕	↕
SUI	sr2, byte	3	17	sr2 ← sr2 − byte		↕	↕
SBI	sr2, byte	3	17	sr2 ← sr2 − byte − CY		↕	↕
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
GTI	sr2, byte	3	14	sr2 − byte − 1	No Borrow	↕	↕
LTI	sr2, byte	3	14	sr2 − byte	Borrow	↕	↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
IMMEDIATE DATA TRANSFER (SPECIAL REGISTER) (CONT.)							
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
NEI	sr2, byte	3	14	sr2 – byte	No Zero	↕	↕
EQI	sr2, byte	3	14	sr2 – byte	Zero	↕	↕
WORKING REGISTER							
XRAW	wa	3	14	A ← A ∀ (V, wa)			↕
ADDNCW	wa	3	14	A ← A + (V, wa)	No Carry	↕	↕
SUBNBW	wa	3	14	A ← A – (V, wa)	No Borrow	↕	↕
ADDW	wa	3	14	A ← A + (V, wa)		↕	↕
ADCW	wa	3	14	A ← A + (V, wa) + CY		↕	↕
SUBW	wa	3	14	A ← A – (V, wa)		↕	↕
SBBW	wa	3	14	A ← A – (V, wa) – CW		↕	↕
ANAW	wa	3	14	A ← A ∧ (V, wa)			↕
ORAW	wa	3	14	A ← A ∨ (V, wa)			↕
GTAW	wa	3	14	A ← (V, wa) – 1	No Borrow	↕	↕
LTAW	wa	3	14	A – (V, wa)	Borrow	↕	↕
ONAW	wa	3	14	A ∧ (V, wa)	No Zero		↕
OFFAW	wa	3	14	A ∧ (V, wa)	Zero		↕
NEAW	wa	3	14	A – (V, wa)	No Zero	↕	↕
EQAW	wa	3	14	A – (V, wa)	Zero	↕	↕
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) – byte – 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) – byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) – byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) – byte	Zero	↕	↕
INCREMENT/DECREMENT							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕

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INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
INCREMENT/DECREMENT (CONT.)							
DCR	r2	1	4	r2 ← r2 − 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) − 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp − 1			
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
ROTATE AND SHIFT							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RCL		2	8	Cm + 1 ← Cm, C_0 ← CY, CY ← C_7		↕	
RAR		2	8	Am − 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RCR		2	8	Cm − 1 ← Cm, C_7 ← CY, CY ← C_0		↕	
SHAL		2	8	Am + 1 ← Am, A_0 ← 0, CY ← A_7		↕	
SHCL		2	8	Cm + 1 ← CM, C_0 ← 0, CY ← C_7		↕	
SHAR		2	8	Am − 1 ← Am, A_7 ← 0, CY ← A_0		↕	
SHCR		2	8	Cm − 1 ← Cm, C_7 ← 0, CY ← C_0		↕	
JUMP							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
CALL							
CALL	word	3	16	(SP − 1) ← $(PC - 3)_H$, (SP − 2) ← $(PC - 3)_L$, PC ← word			
CALB		1	13	(SP − 1) ← $(PC - 1)_H$, (SP − 2) ← $(PC - 1)_L$, PC_H ← B, PC_L ← C			
CALF	word	2	16	$(SP-1)\leftarrow(PC-2)_H$, $(SP-2)\leftarrow(PC-2)_L$ PC15 ~ 11 ← 00001, PC10 ~ 0 ← fa			
CALT	word	1	19	$(SP-1)\leftarrow(PC-1)_H$, $(SP-2)\leftarrow(PC-1)_L$ $PC_L\leftarrow(128-2ta)$, $PC_H\leftarrow(129+2ta)$			
SOFTI		1	19	(SP − 1) ← PSW, SP − 2, (SP − 3) ← PC PC ← 0060_H, SIRQ ← 1			

INSTRUCTION GROUPS (CONT.)

MNEMONIC	OPERANDS	NO. BYTES	CLOCK CYCLES	OPERATION	SKIP CONDITION	FLAGS CY	FLAGS Z
RETURN							
RET		1	11	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $SP \leftarrow SP - 2$			
RETS		1	11+a	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1),$ $SP \leftarrow SP + 2, PC \leftarrow PC + n$			
RETI		1	15	$PC_L \leftarrow (SP), PC_H \leftarrow (SP + 1)$ $PSW \leftarrow (SP+2), SP \leftarrow SP+3, SIRQ \leftarrow 0$			
SKIP							
BIT	bit, wa	2	10	Bit test	$(V, wa)_{bit} = 1)$		
SKC		2	8	Skip if Carry	CY = 1		
SKNC		2	8	Skip if No Carry	CY = 0		
SKZ		2	8	Skip if Zero	Z = 1		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKIT	f	2	8	Skip if INT X = 1, then reset INT X	f = 1		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU CONTROL							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
HLT		1	6	Halt			
SERIAL PORT CONTROL							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
INPUT/OUTPUT							
IN	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow byte$ $A \leftarrow DB_{7-0}$			
OUT	byte	2	10	$AB_{15-8} \leftarrow B, AB_{7-0} \leftarrow byte$ $DB_{7-0} \leftarrow A$			
PEX		2	11	$PE_{15-8} \leftarrow B, PE_{7-0} \leftarrow C$			
PEN		2	11	$PE_{15-12} \leftarrow B_{7-4}$			
PER		2	11	Port E AB Mode			

4

Program Status Word (PSW) Operation

OPERATION						D6	D5	D4	D3	D2	D0
REG, MEMORY			IMMEDIATE		SKIP	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDW ADCW SUBW SBBW	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAW ORAW XRAW	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCW SUBNBW GTAW LTAW	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
ONA OFFA	ONAW OFFAW	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAW EQAW	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW					↕	↕	↕	0	0	•
DAA						↕	0	↕	0	0	↕
RAL, RAR, RCL, RCR SHAL, SHAR, SHCL, SHCR						•	0	•	0	0	↕
RLD, RRD						•	0	•	0	0	•
STC						•	0	•	0	0	1
CLC						•	0	•	0	0	0
			MVI A, byte			•	0	•	1	0	•
			MVI L, byte LXI H, word			•	0	•	0	1	•
					BIT SKC SKNC SKZ SKNZ SKIT SKNIT	•	↕	•	0	0	•
					RETS	•	1	•	0	0	•
All other instructions						•	0	•	0	0	•

↕ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage On Any Pin . . . . . −0.3V to +7.0V

T_a = 25°C

*COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

−10°C to +70°C, V_{CC} = +5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	Except $\overline{SCK}$, X1
	V_{IH2}	3.8		V_{CC}	V	$\overline{SCK}$, X1
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100 μA
	V_{OH2}	2.0			V	I_{OH} = −500 μA
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0V
High Level Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.45V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Power Supply Current	I_{CC}		110	200	mA	

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Input Capacitance	C_I			10	pF	fc = 1 MHz All pins not under test at 0V
Output Capacitance	C_O			20	pF	
Input/Output Capacitance	C_{IO}			20	pF	

AC CHARACTERISTICS

$-10°C$ to $+70°C$, $V_{CC} = +5.0V \pm 10\%$

CLOCK TIMING

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
X1 Input Cycle Time	t_{CYX}	227	1000	ns	
X1 Input Low Level Width	t_{XXL}	106		ns	
X1 Input High Level Width	t_{XXH}	106		ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	454	2000	ns	
ϕ_{OUT} Low Level Width	$t_{\phi\phi L}$	150		ns	
ϕ_{OUT} High Level Width	$t_{\phi\phi H}$	150		ns	
ϕ_{OUT} Rise/Fall Time	t_r, t_f		40	ns	

READ/WRITE OPERATION

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
$\overline{RD}$ L.E. → ϕ_{OUT} L.E.	$t_{R\phi}$	100		ns	
Address (PE_{0-15}) → Data Input	t_{AD1}		550 + 500 x N	ns	
$\overline{RD}$ T.E. → Address	t_{RA}	200(T3); 700(T4)		ns	
$\overline{RD}$ L.E. → Data Input	t_{RD}		350 + 500 x N	ns	
$\overline{RD}$ T.E. → Data Hold Time	t_{RDH}	0		ns	
$\overline{RD}$ Low Level Width	t_{RR}	850 + 500 x N		ns	
$\overline{RD}$ L.E. → $\overline{WAIT}$ L.E.	t_{RWT}		450	ns	
Address (PE_{0-15}) → $\overline{WAIT}$ L.E.	t_{AWT1}		650	ns	
$\overline{WAIT}$ Set Up Time (Referenced from ϕ_{OUT} L.E.)	t_{WTS}	290		ns	
$\overline{WAIT}$ Hold Time (Referenced from ϕ_{OUT} L.E.)	t_{WTH}	0	120	ns	
M1 → $\overline{RD}$ L.E.	t_{MR}	200		ns	$t_{CY\phi}$ = 500 ns
$\overline{RD}$ T.E. → M1	t_{RM}	200		ns	
IO/$\overline{M}$ → $\overline{RD}$ L.E.	t_{IR}	200		ns	
$\overline{RD}$ T.E. → IO/$\overline{M}$	t_{RI}	200		ns	
ϕ_{OUT} L.E. → $\overline{WR}$ L.E.	$t_{\phi W}$	40	125	ns	
Address (PE_{0-15}) → ϕ_{OUT} T.E.	$t_{A\phi}$	100		ns	
Address (PE_{0-15}) → Data Output	t_{AD2}	450		ns	
Data Output → $\overline{WR}$ T.E.	t_{DW}	600 + 500 x N		ns	
$\overline{WR}$ T.E. → Data Stabilization Time	t_{WD}	150		ns	
Address (PE_{0-15}) → $\overline{WR}$ L.E.	t_{AW}	400		ns	
$\overline{WR}$ T.E. → Address Stabilization Time	t_{WA}	200		ns	
$\overline{WR}$ Low Level Width	t_{WW}	600 + 500 x N		ns	
IO/$\overline{M}$ → $\overline{WR}$ L.E.	t_{IW}	500		ns	
$\overline{WR}$ T.E. → IO/$\overline{M}$	t_{WI}	250		ns	

AC CHARACTERISTICS
(CONT.)

SERIAL I/O OPERATION

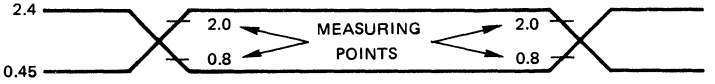
PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
$\overline{SCK}$ Cycle Time	t_{CYK}	800		ns	$\overline{SCK}$ Input
		900	4000	ns	$\overline{SCK}$ Output
$\overline{SCK}$ Low Level Width	t_{KKL}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
$\overline{SCK}$ High Level Width	t_{KKH}	350		ns	$\overline{SCK}$ Input
		400		ns	$\overline{SCK}$ Output
SI Set-Up Time (referenced from $\overline{SCK}$ T.E.)	t_{SIS}	80		ns	
SI Hold Time (referenced from $\overline{SCK}$ T.E.)	t_{SIH}	260		ns	
$\overline{SCK}$ L.E. → SO Delay Time	t_{KO}		180	ns	
$\overline{SCS}$ High → $\overline{SCK}$ L.E.	t_{CSK}	100		ns	
$\overline{SCK}$ T.E. → $\overline{SCS}$ Low	t_{KCS}	100		ns	
$\overline{SCK}$ T.E. → SAK Low	t_{KSA}		260	ns	

HOLD OPERATION

PARAMETER	SYMBOL	MIN	MAX	UNIT	CONDITION
HOLD Set-Up Time (referenced from ϕ_{OUT} L.E.)	t_{HDS_1}	200		ns	$t_{CY\phi}$ = 500 ns
	t_{HDS_2}	200		ns	
HOLD Hold Time (referenced from ϕ_{OUT} L.E.)	t_{HDH}	0		ns	
ϕ_{OUT} L.E. → HLDA	t_{DHA}	110	100	ns	
HLDA High → Bus Floating (High Z State)	t_{HABF}	−150	150	ns	
HLDA Low → Bus Enable	t_{HABE}		350	ns	

Notes:

① AC Signal waveform (unless otherwise specified)



② Output Timing is measured with 1 TTL + 200 pF measuring points are V_{OH} = 2.0V
V_{OL} = 0.8V

③ L.E. = Leading Edge, T.E. = Trailing Edge

AC CHARACTERISTICS (CONT.)

$t_{CY\phi}$ DEPENDENT AC PARAMETERS

PARAMETER	EQUATION	MIN/MAX	UNIT
$t_{R\phi}$	(1/5) T	MIN	ns
t_{AD_1}	(3/2 + N) T - 200	MAX	ns
t_{RA} (T_3)	(1/2) T - 50	MIN	ns
t_{RA} (T_4)	(3/2) T - 50	MIN	ns
t_{RD}	(1 + N) T - 150	MAX	ns
t_{RR}	(2 + N) T - 150	MIN	ns
t_{RWT}	(3/2) T - 300	MAX	ns
t_{AWT_1}	(2) T - 350	MAX	ns
t_{MR}	(1/2) T - 50	MIN	ns
t_{RM}	(1/2) T - 50	MIN	ns
t_{IR}	(1/2) T - 50	MIN	ns
t_{RI}	(1/2) T - 50	MIN	ns
$t_{\phi W}$	(1/4) T	MAX	ns
$t_{A\phi}$	(1/5) T	MIN	ns
t_{AD_2}	T - 50	MIN	ns
t_{DW}	(3/2 + N) T - 150	MIN	ns
t_{WD}	(1/2) T - 100	MIN	ns
t_{AW}	T - 100	MIN	ns
t_{WA}	(1/2) T - 50	MIN	ns
t_{WW}	(3/2 + N) T - 150	MIN	ns
t_{IW}	T	MIN	ns
t_{WI}	(1/2) T	MIN	ns
t_{HABE}	(1/2) T - 150	MAX	ns

Notes: ① N = Number of Wait States

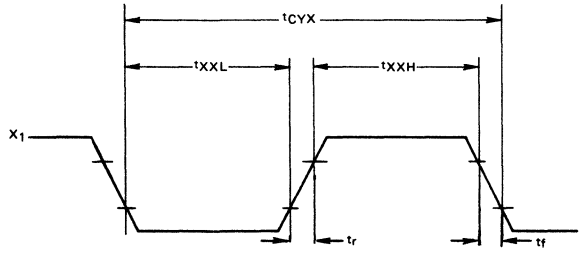
② $T = t_{CY\phi}$

③ Only above parameters are t_{CY_ϕ} dependent

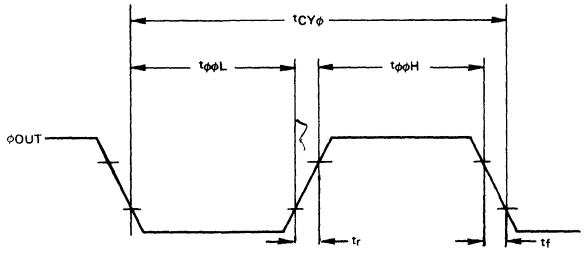
④ When a crystal frequency other than 4 MHz is used (t_{CY_ϕ} = 500 ns) the above equations can be used to calculate AC parameter values.

TIMING WAVEFORMS

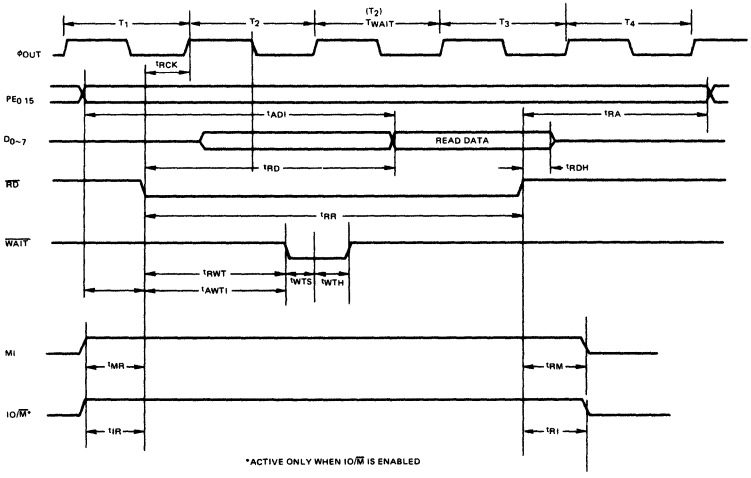
CLOCK TIMING



TIMING WAVEFORMS (CONT.)

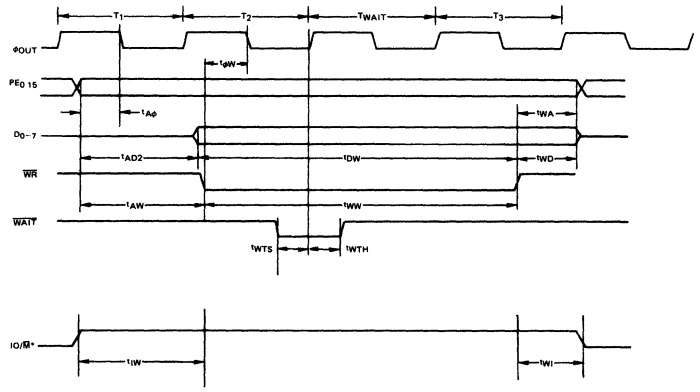


READ OPERATION



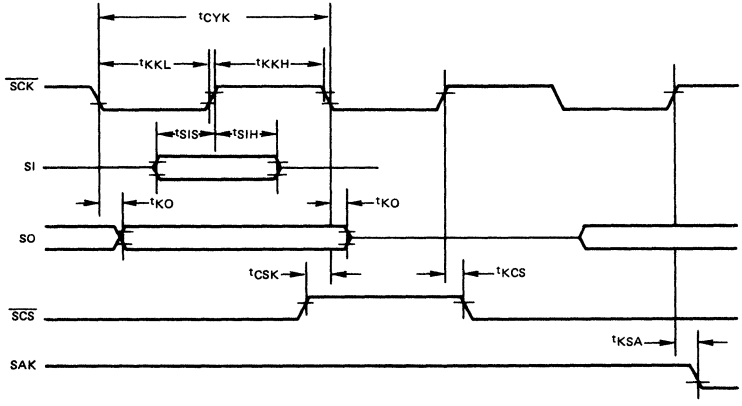
*ACTIVE ONLY WHEN IO/M IS ENABLED

WRITE OPERATION

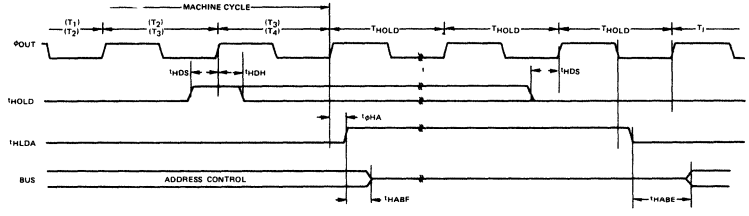


*ACTIVE ONLY WHEN IO/M IS ENABLED

SERIAL I/O OPERATION



HOLD OPERATION



Package Outlines

For information, see Package Outline Section 7.

Plastic Quil, μPD7801G/02G
Plastic Shrinkdip, μPD7801CW μPD7802CW

Description

The NEC μPD78C06/μPD78C05 are advanced CMOS 8-bit general purpose single-chip microcomputers intended for applications requiring 8-bit microprocessor control and extremely low power consumption, and ideally suited for portable, battery-powered/backedup products. Subsets of the μPD7801, the μPD78C06/05 integrate an 8-bit ALU, 4K-ROM, 128-byte RAM, 46 I/O lines, an 8-bit timer, and a serial I/O port on a single die. Fully compatible with the 8080A bus structure, expanded system operation can easily be implemented using industry standard peripheral and memory components. Total memory space can be increased to 64K-bytes.

The μPD78C06/05 lend themselves well to low power, portable applications by featuring two power down modes to further conserve power when the processor is not active. The μPD78C06 is packaged in a 64-pin flat pack. The μPD78C05 is a ROM-less version packaged in a 64-pin QUIL, designed for prototype development and small volume production.

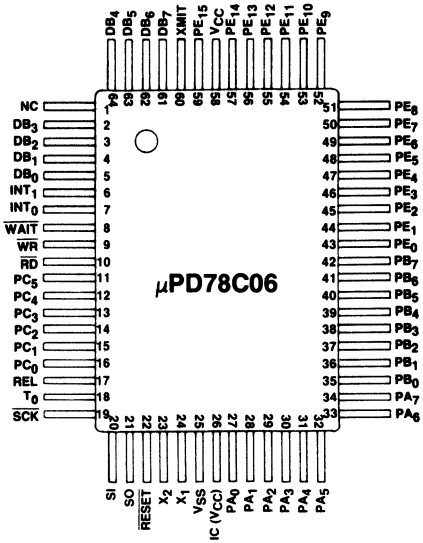
Features

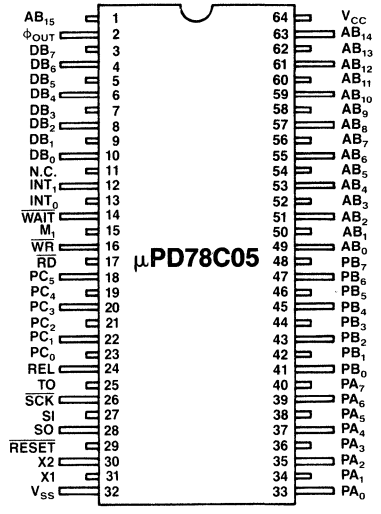
- ☐ CMOS silicon gate technology +5V supply
- ☐ Complete single-chip microcomputer
  - 8-bit ALU
  - 4K-ROM
  - 128-Byte RAM
- ☐ Low power consumption
- ☐ 46 I/O lines
- ☐ Expansion capabilities
  - 8080A bus-compatible
  - 60K-byte external memory address range
- ☐ Serial I/O port
- ☐ 101 instruction set
  - Multiple address modes
- ☐ Power-down modes
  - Halt mode
  - Stop mode
- ☐ 8-bit timer
- ☐ Prioritized interrupt structure
  - 2 external
  - 1 internal
- ☐ On-chip clock generator
- ☐ 64-pin flat pack
- ☐ ROM-less version available (78C05)

Pin Identification

Symbol	Name
PA_7–PA_0, PB_7–PB_0, PC_5–PC_0, PE_{15}–PE_0	I/O Ports
DB_7–DB_0	Data Bus
$\overline{WAIT}$	Wait Request
INT_0, INT_1	Interrupt Request
X_2, X_1	Crystal
$\overline{SCK}$	Serial Clock Input/Output
SI	Serial Input
SO	Serial Output
$\overline{RESET}$	Reset
$\overline{RD}$	Read Strobe
$\overline{WR}$	Write Strobe
ϕ_{OUT}	Clock Output

Pin Configuration





4

Block Diagram

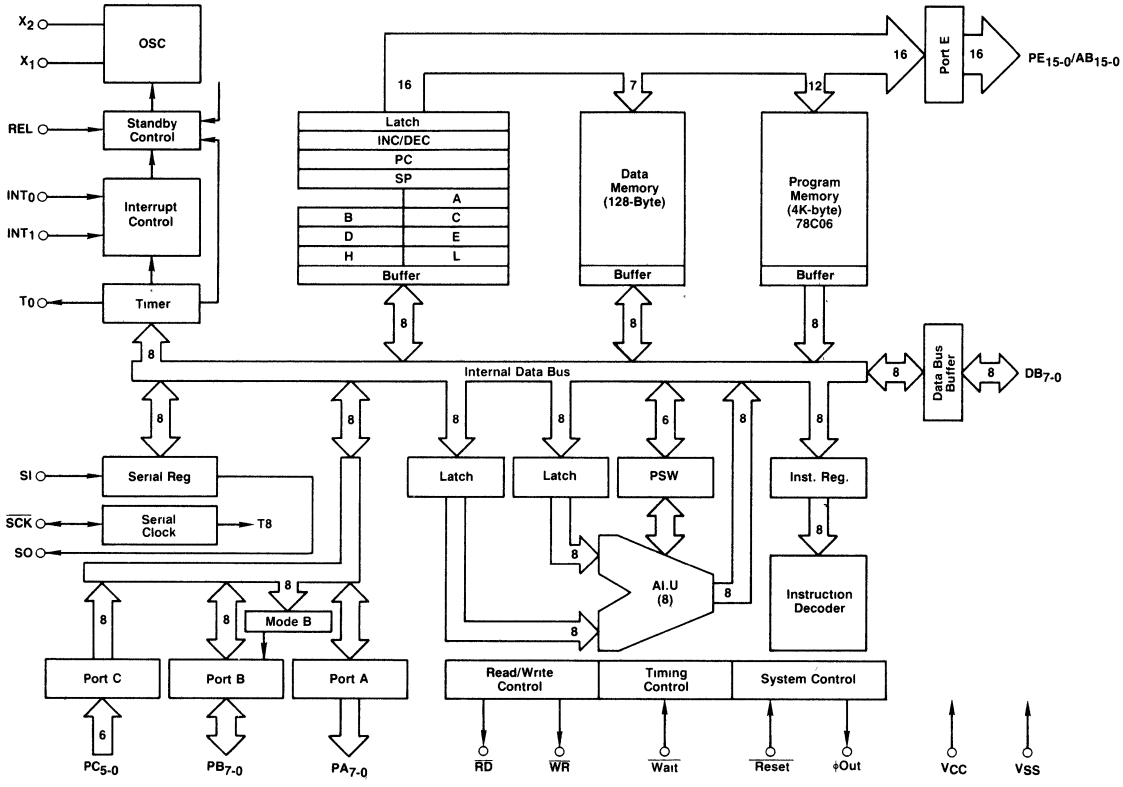


Table 1. Halt and Stop Modes

Function	Halt Mode	Stop Mode
Oscillator	Run	Stop
Internal System Clock	Stop	
Timer	Run	
Timer Register	Hold	Set
Upcounter, Prescaler 0, 1	Run	Cleared
Serial Interface		Run ①
Serial Clock	Hold	Hold
Interrupt Control Circuit	Run	Stop
Interrupt Enable Flag	Hold	Reset
$\overline{INT_0}$, $\overline{INT_1}$ Input	Active	Inactive
INT_T		—
T_8 (INTFS)		—
Mask Register	Hold	Set
Pending Interrupts (INTFX)		Reset
REL Input	Inactive	Active
$\overline{RESET}$ Input	Active	

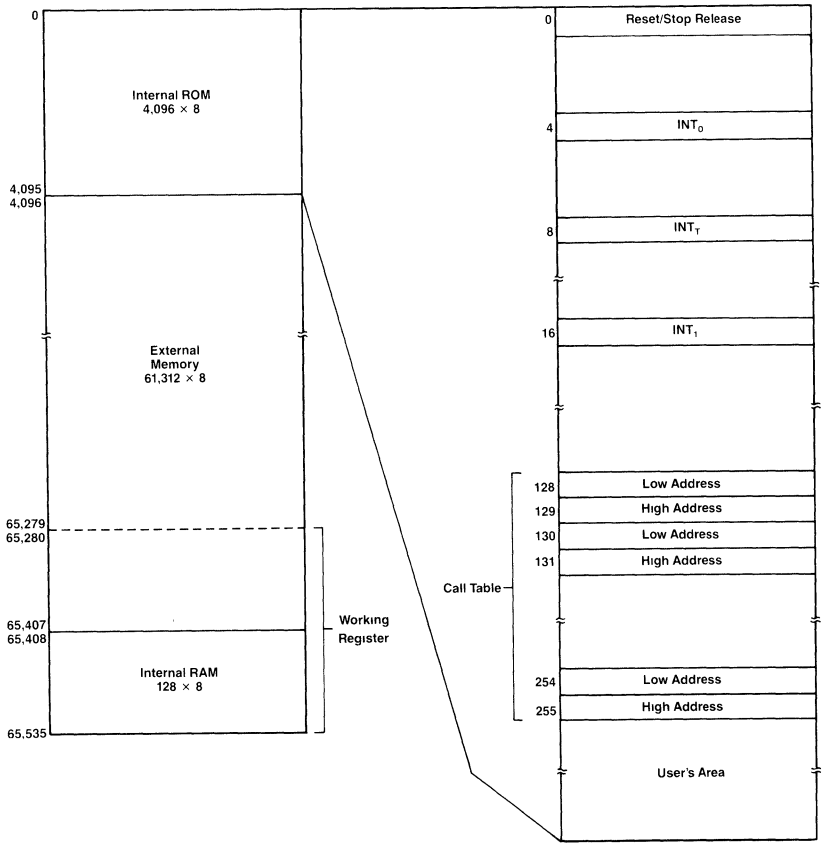
Function	Halt Mode	Stop Mode
On-chip RAM	Hold	Hold
Output Latch in Ports A, B, E		
Program Counter (PC)		Cleared
Stack Pointer (SP)		
General Registers (A, B, C, D, E, F, L)		Unknown
Program Status Word (PSW)		Reset
Mode B Register		Hold
Standby Control Register (SC_0–SC_3)		
Standby Control Register (SC_4)		Set
Timer Mode Register (TMM_0–TMM_1)		Hold
Timer Mode Register (TMM_1)		Set
Serial Mode Register (SM)		Hold
Data Bus (DB_0–DB_7)	High-Z	High-Z
$\overline{RD}$, $\overline{WR}$ Output	High	High

Note: ① Serial clock counter is running and T_8 is generated, however, there are no effects from it

Functional Description

Memory map

The μPD78C06 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0–4,095) and RAM 65,408–65,535), any memory location can be used as either ROM or RAM. The following memory map defines the 0–64K-byte memory space for the μPD78C06 showing that the Reset Start Address, Interrupt Start Address, Call Tables, etc., are located in the internal ROM area.



I/O Ports

Port	Functions
Port A	8-bit output port with latch
Port B	8-bit programmable Input/Output port with latch
Port C	6-bit nibble I/O or Control port
Port E	16-bit Address/Output port

Port A. Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using arithmetic and logic instructions. Data remains latched at Port A unless acted on by another Port A instruction or a RESET is issued.

Port B. Port B is an 8-bit I/O port. Data is latched at Port B in both the Input or Output mode. Each bit of Port B can be independently set to either Input or Output modes. The Mode B register programs the individual lines of Port B to be either an Input (Mode $B_n = 1$) or an Output (Mode $B_{n=0}$)

Port C. Port C is a 6-bit I/O port with internal pull-up resistors.

Port E (78C06). Port E is a 16-bit address bus/output port. It can be set to one of two operating modes using the PER or PEX instruction.

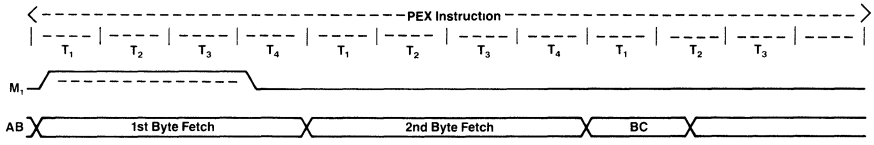
- ☐ 16-bit address bus — the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- ☐ 16-bit output port — the PEX instruction sets Port E to a 16-bit output port. The contents of B and C registers appear on PE_8–PE_{15} and PE_0–PE_1, respectively.

Address bus AB_{15}–AB_0 (78C05)

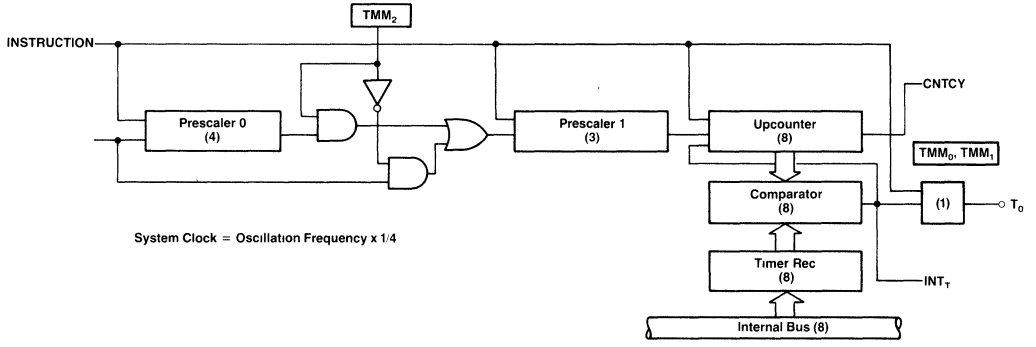
These lines are the 16 bit-to-bit address bus to the main memory. The 78C05, having no internal ROM, must address the area from 0 to 4096 as external ROM.

The 78C05 AB lines are unlike the 78C06 PE lines in that they have no internal latches. When the Port E output instruction PEX is executed in a 78C05, the register pair BC is output to the AB lines for only one clock cycle during the third machine cycle. This is provided to allow external hardware to emulate the Port E operation of the 78C06.

Functional Description (Cont.)



Timer Block Diagram



Timer operation

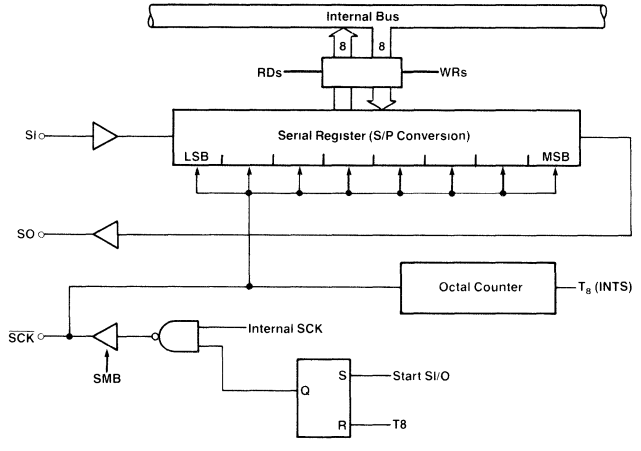
A programmable 8-bit timer is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 8μs to 32ms in duration. The timer consists of a prescaler which decrements an 8-bit counter at a fixed 8μs or 128μs rate. Count pulses are loaded into the 8-bit upcounter through the timer register.

Countup operation is initiated upon execution of the STM instruction when the contents of the upcounter are fully incremented and a coincidence occurs, an interval interrupt (INT_T) is generated. Count operation may be reinitialized with the STM instruction. The duration of the timeout may be altered by loading new contents into the timer register.

The timer flip-flop is set by the STM instruction and reset on a countup operation. Its output (T_0) is available externally and may be used for general external synchronization.

Timer interrupt (INT_T) may be disabled through the interrupt.

Serial Port Block Diagram



Functional Description (Cont.)

Serial port operation

The on-chip serial port provides basic synchronous serial communication functions allowing the NEC μPD78C06/05 to serially interface with external devices.

Serial transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at 0.5 Mbit/second if the internal clock is used or is variable between DC and 0.5 Mbit/second when an external clock is used. The Clock Source Select is determined by the Mode C register. The serial clock (internal or external $\overline{SCK}$) is enabled when the Serial Chip Select signal ($\overline{SCS}$) goes low. At this time receive and transmit operations through the Serial Input port (SI)/Serial Output port (SO) are enabled. Receive and transmit operations are performed MSB first.

Interrupt structure

The μPD78C06/05 provide a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from six different sources: two external interrupts, two internal interrupts, and nonmaskable software interrupt. When activated, each interrupt branches to a designated memory vch interrupt branches to a designated memory vector location for that interrupt.

Interrupt Structure

INT	Vectored Memory Location	Priority	Type
INT_T	8	3	Internal, Timer Overflow
INT_0	4	2	External, level sensitive
INT_1	16	4	External, Rising edge sensitive

$\overline{RESET}$ (Reset)

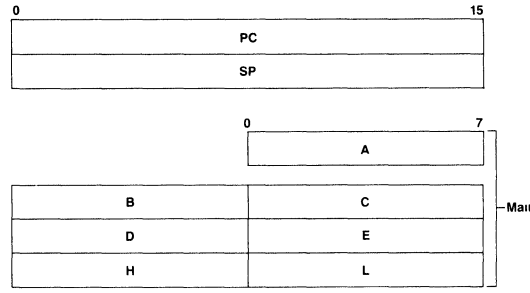
An active-low signal on this input for more than 4μs forces the μPD780C06/05 into a Reset condition. $\overline{RESET}$ affects the following internal functions:

- ☐ The Interrupt Enable flags are reset, and interrupts are inhibited.
- ☐ The Interrupt Request flag is reset.
- ☐ The Halt flip-flop is reset, and the Halt state is released.
- ☐ The contents of the Mode B register are set to FF_H, and Port B becomes an input port.
- ☐ All flags are reset to 0.
- ☐ The internal Count register for timer operation is set to FF_H and the timer F/F is reset.
- ☐ The contents of the program counter are set to 0000_H.
- ☐ Data bus (DB_0–DB_7), $\overline{RD}$, and $\overline{WR}$ go to a high impedance state.

Once the $\overline{RESET}$ input goes high, the program is started at location 0000_H.

Registers

The μPD78C06/05 contain seven 8-bit registers and two 16-bit registers.



General purpose registers. The general purpose registers A, B, C, D, E, H, L, can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL). Automatic increment and decrement addressing mode capabilities extend the uses for the DE and HL register pairs.

Accumulator (A)

All data transfers between the μPD78C06/05 and external memory or I/O are done through the accumulator.

Program counter (PC)

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000_H.

Stack pointer (SP)

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in/first-out). The contents of the SP are decremented during a Call or Push instruction or if an interrupt occurs. The SP is incremented during a Return or POP instruction.

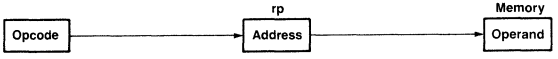
Address Modes

- Register addressing
- Register indirect addressing
- Automatic increment addressing
- Automatic decrement addressing
- Working-register addressing
- Direct addressing
- Immediate addressing
- Immediate extended addressing

Register addressing

The instruction opcode specifies a register r which contains the operand.

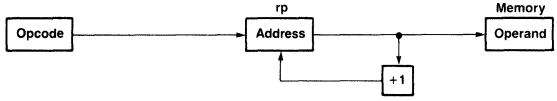
Register indirect addressing



The instruction opcode specifies a register pair which contains the memory address of the operand. Mnemonics with an X suffix are ending this address mode.

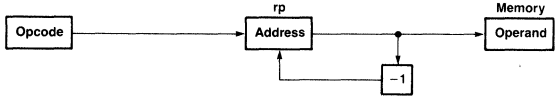
Address Modes (Cont.)

Automatic increment addressing

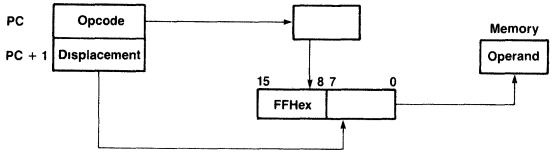


The opcode specifies a register pair which contains the memory address of the operand. The contents of the register pair are automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

Automatic decrement addressing

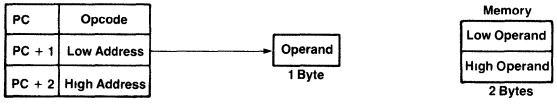


Working-register addressing



The contents of the register are linked with the byte following the opcode to form a memory address which contains the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only one additional byte is required for the address. Mnemonics with a W suffix indicate this address mode. In the 78C06/05 the V register is always FFH.

Direct addressing



The two bytes following the opcode specify an address of a location containing the operand.

Immediate addressing

PC

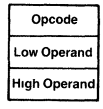
PC + 1

Immediate extended addressing

PC

PC + 1

PC + 2



Instruction Set Definitions

Operand	Description
r	A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, MK, MB, TM_0, TM_1, S, SM, SC
sr1	PA, PB, PC, MK, S, TM_0, TM_1, SC
sr2	PA, PB, PC, MK
rp	SP, B, D, H
rp1	B, D, H
rpa	B, D, H, D+, H+, D−, H−
wa	8-bit immediate data
word	16-bit immediate data
byte	8-bit immediate data
bit	3-bit immediate data
if	F0, 1, FT, FS
F	CY, Z

Notes:
1. When special register operands sr, sr1, sr2 are used, PA = Port A, PB = Port B, PC = Port C, MK = Mask register, MB = Mode B register, MC = Mode C Register, TM_0 = Timer register 0, TM_1 = Timer register 1, S = Serial register.
2. When register pair operands rp, rp1 are used, SP = Stack Pointer, B = BC, D = DE, H = HL.
3. Operands rPa, rPa1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes.
   B = (BC), D = (DE), H = (HL)
   D+ = $(DE)^+$, H+ = $(HL)^+$, D− = $(DE)^-$, H− = $(HL)^-$.
4. When the interrupt operand if is used, F0 = INTF0, F1 = INTF1, FT = INTFT, FS = INTFS.
5. When the operand F is used, CY = Carry and Z = Zero.
6. The V register is always FFHex.

Instruction Set

Mnemonic	Operand	No. Bytes	Clock Cycles	Operation	Skip Condition	Flags CY	Flags Z
8-bit Data Transfer							
MOV	r1, A	1	6	r1 ← A			
MOV	A, r1	1	6	A ← r1			
MOV	sr, A	2	14	sr ← A			
MOV	A, sr1	2	14	A ← sr1			
MOV	r, word	4	25	r ← (word)			
MOV	word, r	4	25	(word) ← r			
MVI	r, byte	2	11	r ← byte			
STAW	wa	2	14	(V, wa) ← A			
LDAW	wa	2	14	A ← (V, wa)			
STAX	rpa	1	39	(rpa) ← A			
LDAX	rpa	1	9	A ← (rpa)			
16-bit Data Transfer							
SBCD	word	4	28	(word) ← C, (word + 1) ← B			
SDED	word	4	28	(word) ← E, (word + 1) ← D			
SHLD	word	4	28	(word) ← L, (word + 1) ← H			
SSPD	word	4	28	(word) ← SP_L, (word + 1) ← SP_H			
LBCD	word	4	28	C ← (word), B ← (word + 1)			
LDED	word	4	28	E ← (word), D ← (word + 1)			
LHLD	word	4	28	L ← (word), H ← (word + 1)			
LSPD	word	4	28	SP_L ← (word), SP_H ← (word + 1)			
PUSH	rp1	2	21	(SP − 1) ← $rp1_H$, (SP − 2) ← $rp1_L$			
POP	rp1	2	18	$rp1_L$ ← (SP) $rp1_H$ ← (SP + 1), SP ← SP + 2			
LXI	rp, word	3	16	rp ← word			

Instruction Set (Cont.)

Mnemonic	Operand	No. Bytes	Clock Cycles	Operation	Skip Condition	Flags CY	Flags Z
Arithmetic							
ADD	A, r	2	12	A ← A + r		↕	↕
ADDX	rpa	2	15	A ← A + (rpa)		↕	↕
ADC	A, r	2	12	A ← A + r + CY		↕	↕
ADCX	rpa	2	15	A ← A + (rpa) + CY		↕	↕
SUB	A, r	2	12	A ← A − r		↕	↕
SUBX	rpa	2	15	A ← A − (rpa)		↕	↕
SBB	A, r	2	12	A ← A − r − CY		↕	↕
SBBX	rpa	2	15	A ← A − (rpa) − CY		↕	↕
ADDNC	A, r	2	12	A ← A + r	No Carry	↕	↕
ADDNCX	rpa	2	15	A ← A + (rpa)	No Carry	↕	↕
SUBNB	A, r	2	12	A ← A − r	No Borrow	↕	↕
SUBNBX	rpa	2	15	A ← A + (rpa)	No Borrow	↕	↕
Logical							
ANA	A, r	2	8/12	A ← A ∧ r			↕
ANAX	rpa	2	11/15	A ← A ∧ (rpa)			↕
ORA	A, r	2	12	A ← A ∨ r			↕
ORAX	rpa	2	15	A ← A ∨ (rpa)			↕
XRA	A, r	2	12	A ← A ∨̄ r			↕
XRAX	rpa	2	15	A ← A ∨̄ (rpa)			↕
GTA	A, r	2	12	A − r − 1	No Borrow	↕	↕
GTAX	rpa	2	15	A − (rpa) − 1	No Borrow	↕	↕
LTA	A, r	2	12	A − r	Borrow	↕	↕
LTAX	rpa	2	15	A − (rpa)	Borrow	↕	↕
ONA	A, r	2	12	A ∧ r	No Zero		↕
ONAX	rpa	2	15	A ∧ (rpa)	No Zero		↕
OFFA	A, r	2	12	A ∧ r	Zero		↕
OFFAX	rpa	2	15	A ∧ (rpa)	Zero		↕
NEA	A, r	2	12	A − r	No Zero	↕	↕
NEAX	rpa	2	15	A − (rpa)	No Zero	↕	↕
EQA	A, r	2	12	A − r	Zero	↕	↕
EQAX	rpa	2	15	A − (rpa)	Zero	↕	↕
Immediate Data Transfer (Accumulator)							
XRI	A, byte	2	7/11	A ← A ∨̄ byte			↕
ADINC	A, byte	2	7/11	A ← A + byte	No Carry	↕	↕
SUINB	A, byte	2	7/11	A ← A − byte	No Borrow	↕	↕
ADI	A, byte	2	7/11	A ← A + byte		↕	↕
ACI	A, byte	2	7/11	A ← A + byte + CY		↕	↕
SUI	A, byte	2	7/11	A ← A − byte		↕	↕
SBI	A, byte	2	7/11	A ← A − byte − CY		↕	↕
ANI	A, byte	2	7/11	A ← A ∧ byte			↕
ORI	A, byte	2	7/11	A ← A ∨ byte			↕
GTI	A, byte	2	7/11	A − byte − 1	No Borrow	↕	↕
LTI	A, byte	2	7/11	A − byte	Borrow	↕	↕
ONI	A, byte	2	7/11	A ∧ byte	No Zero		↕
OFFI	A, byte	2	7/11	A ∧ byte	Zero		↕
NEI	A, byte	2	7/11	A − byte	No Zero	↕	↕
EQI	A, byte	2	7/11	A − byte	Zero	↕	↕
Immediate Data Transfer (Special Register)							
ANI	sr2, byte	3	17	sr2 ← sr2 ∧ byte			↕
ORI	sr2, byte	3	17	sr2 ← sr2 ∨ byte			↕
OFFI	sr2, byte	3	14	sr2 ∧ byte	Zero		↕
ONI	sr2, byte	3	14	sr2 ∧ byte	No Zero		↕
Working Register							
ANIW	wa, byte	3	16	(V, wa) ← (V, wa) ∧ byte			↕
ORIW	wa, byte	3	16	(V, wa) ← (V, wa) ∨ byte			↕
GTIW	wa, byte	3	13	(V, wa) − byte − 1	No Borrow	↕	↕
LTIW	wa, byte	3	13	(V, wa) − byte	Borrow	↕	↕
ONIW	wa, byte	3	13	(V, wa) ∧ byte	No Zero		↕
OFFIW	wa, byte	3	13	(V, wa) ∧ byte	Zero		↕
NEIW	wa, byte	3	13	(V, wa) − byte	No Zero	↕	↕
EQIW	wa, byte	3	13	(V, wa) − byte	Zero	↕	↕

Instruction Set (Cont.)

Mnemonic	Operand	No. Bytes	Clock Cycles	Operation	Skip Condition	Flags CY	Flags Z
Increment/Decrement							
INR	r2	1	4	r2 ← r2 + 1	Carry		↕
INRW	wa	2	13	(V, wa) ← (V, wa) + 1	Carry		↕
DCR	r2	1	4	r2 ← r2 − 1	Borrow		↕
DCRW	wa	2	13	(V, wa) ← (V, wa) − 1	Borrow		↕
INX	rp	1	7	rp ← rp + 1			
DCX	rp	1	7	rp ← rp − 1			
Miscellaneous							
DAA		1	4	Decimal Adjust Accumulator		↕	↕
STC		2	8	CY ← 1		1	
CLC		2	8	CY ← 0		0	
Rotate and Shift							
RLD		2	17	Rotate Left Digit			
RRD		2	17	Rotate Right Digit			
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
RAR		2	8	Am − 1 ← Am, A_7 ← CY, CY ← A_0		↕	
RAL		2	8	Am + 1 ← Am, A_0 ← CY, CY ← A_7		↕	
Jump							
JMP	word	3	10	PC ← word			
JB		1	4	PC_H ← B, PC_L ← C			
JR	word	1	13	PC ← PC + 1 + jdisp1			
JRE	word	2	13	PC ← PC + 2 + jdisp			
Call							
CALL	word	3	16	(SP − 1) ← $(PC - 3)_H$, (SP − 2) ← $(PC - 3)_L$, PC ← word			
CALF	word	2	16	(SP − 1) ← $(PC - 2)_H$, (SP − 2) ← $(PC - 2)_L$, PC_{15}–PC_{11} ← 00001, PC_{10}–PC_0 ← fa			
CALT	word	1	19	(SP − 1) ← $(PC - 1)_H$, (SP − 2) ← $(PC - 1)_L$, PC_L ← (128 − 2ta), PC_H ← (129 + 2ta)			
Return							
RET		1	11	PC_L ← (SP), PC_H ← (SP + 1) SP ← SP − 2			
RETS		1	11 + a	PC_L ← (SP), PC_H ← (SP + 1), SP ← SP + 2, PC ← PC + n			
RETI		1	15	PC_L ← (SP), PC_H ← (SP + 1) PSW ← (SP + 2), SP ← SP + 3, SIRQ ← 0			
Skip							
SKNC		2	8	Skip if No Carry	CY = 0		
SKNZ		2	8	Skip if No Zero	Z = 0		
SKNIT	f	2	8	Skip if No INT X otherwise reset INT X	f = 0		
CPU Control							
NOP		1	4	No Operation			
EI		2	8	Enable Interrupt			
DI		2	8	Disable Interrupt			
Serial Port Control							
SIO		1	4	Start (Trigger) Serial I/O			
STM		1	4	Start Timer			
Port E Control							
PEX		2	11	PE_{15-8} ← B, PE_{7-0} ← C			
PER		2	11	Port E AB Mode			

4

Program Status Word (PSW) Operation

Operation					D6	D5	D4	D3	D2	D0
Reg. Memory	Immediate			Skip	Z	SK	HC	L1	L0	CY
ADD ADC SUB SBB	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	GTIW LTIW		↕	↕	↕	0	0	↕
	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR INRW DCR DCRW					↕	↕	↕	0	0	•
DAA					↕	0	↕	0	0	↕
RLL, RLR					•	0	•	0	0	↕
RLD – RRD					•	0	•	0	0	•
STC					•	0	•	0	0	1
CLC					•	0	•	0	0	0
		MVI A, byte			•	0	•	1	0	•
		MVI L, byte LXI H, word			•	0	•	0	1	•
				SKNC SKNZ SKNIT	•	↕	•	0	0	•
				RETS	•	1	•	0	0	•
All other instructions					•	0	•	0	0	•

Notes: ↕ Flag affected according to result of operation
1 Flag set
0 Flag reset
• Flag not affected

Absolute Maximum Ratings*

(T_a = 25°C)

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_I	−0.3V to V_{CC} +0.3V
Output Voltage, V_O	−0.3V to V_{CC} +0.3V
Output High Current, I_{OH} (Device Total)	−5mA
Output Low Current, I_{OL} (Device Total)	43.5mA
Operating Temperature, T_{OPT}	−10°C to +70°C
Storage Temperature, T_{STG}	−40°C to +125°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C; V_{CC} = 5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH1}	0.7V_{CC}		V_{CC}	V	Except DB_0–DB_7, X_1
	V_{IH2}	V_{CC} − 2.0		V_{CC}	V	DB_0–DB_7
	V_{IH3}	V_{CC} − 0.5		V_{CC}	V	X_1
Input Low Voltage	V_{IL1}	0		0.3V_{CC}	V	Except DB_0–DB_7, X_1
	V_{IL2}	0		0.8	V	DB_0–DB_7
	V_{IL3}	0		0.5	V	X_1
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −100μA
	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −50μA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.8mA
Input High Current	I_{IH1}	8		90	μA	V_{IN} = V_{CC} (REL)
	I_{IH2}			40	μA	V_{IN} = V_{CC} (X_1)

DC Characteristics

T_a = −10°C to +70°C; V_{CC} = 5V ± 10%

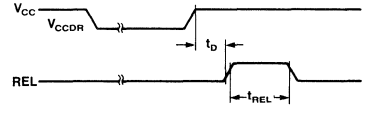
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Current	I_{IL1}	−8		−90	μA	V_{IN} = 0V (WAIT, PC_0–PC_5)
	I_{IL2}			−40	μA	V_{IN} = 0V (X_1)
Input High Leakage Current	I_{LIH}			3	μA	V_{IN} = V_{CC} (Except REL, X_1)
Input Low Leakage Current	I_{LIL1}			−3	μA	V_{IN} = 0V Except WAIT, PC_0–PC_5, X_1
	I_{LIL2}			−3	μA	V_{IN} = 0V (Stop Mode, X_1)
Output High Leakage Current	I_{LOH}			3	μA	V_{OUT} = V_{CC}
Output Low Leakage Current	I_{LOL}			−3	μA	V_{OUT} = 0V
V_{CC} Supply Current	I_{CC1}		3.5	6.0	mA	Operation Mode
	I_{CC2}		0.8	1.8	mA	Halt Mode
	I_{CC3}		1	15	μA	Stop Mode (X_1 = 0V, X_2 = Open)

Low Power Data Memory Retention Characteristics for Stop Mode Operation

T_a = −10°C to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data Retention Voltage	V_{CCDR}	2.0			V	
Data Retention Supply Current	I_{CCDR}		0.8	15	μA	V_{CCDR} = 2.0V, (X_1 = 0V, X_2 = Open)
Data Retention Input Low RES Voltage	V_{ILDR}	0		0.2V_{CCDR}	V	
Data Retention Input High RESET Voltage	V_{IHDR}	0.8V_{CCDR}		V_{CCDR}	V	
REL Input Delay Time	t_D	500			μs	
REL Input High Time	t_{REL}	10			μs	

Notes: In data retention mode, Input voltages to WAIT and PC_0–PC_5 pins (with pull-up resistors) should be maintained same as V_{CCDR} level, other input voltages should be kept less than V_{CCDR} level



DC Characteristics

Read/Write Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
RD LE to ϕ_{OUT} LE	$t_{R\phi}$	300			ns	
Address (PE_0–PE_{15}) to Data Input	t_{AD1}			1200 + 1000 × N	ns	
RD TE to Address	t_{RA}	300 (T_3) 1300 (T_4)			ns	
RD LE to Data Input	t_{RD}			700 + 1000 × N	ns	
RD TE to Data Hold Time	t_{RDH}	0			ns	
RD Low Time	t_{RR}	1700 + 1000 × N			ns	
RD LE to WAIT LE	t_{RWT}			700	ns	
Address (PE_0–PE_{15}) to WAIT LE	t_{AWT1}			1200	ns	
WAIT Set-up Time to ϕ_{OUT} LE	t_{WTS}	600			ns	
WAIT Hold Time after ϕ_{OUT} LE	t_{WTH}	0			ns	$t_{CY\phi}$ = 1000ns
M_1 to RD LE ①	t_{MR}	200			ns	
RD TE to M_1 ①	t_{RM}	300			ns	
ϕ_{OUT} LE to WR LE	$t_{\phi W}$			250	ns	
Address (PE_0–PE_{15}) to ϕ_{OUT} TE	$t_{A\phi}$	150			ns	

DC Characteristics (Cont.)

Read/Write Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address (PE_0–PE_{15}) to Data Output	t_{AD2}	850			ns	
Data Output to WR TE	t_{DW}	1200 +1000 × N			ns	
WR TE to Data Stable Time	t_{WD}	300			ns	
Address (PE_0–PE_{15}) to WR LE	t_{AW}	800			ns	
WR TE to Address Stable Time	t_{WA}	300			ns	
WR Low Time	t_{WW}	1200 +1000 × N			ns	
WR LE to WAIT LE	t_{WWT}			250	ns	

Notes: ① Applies only to μPD78C05
N is number of T_{WAIT}
LE is leading edge, and TE is trailing edge

Serial Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
SCK Cycle Time	t_{CYK}	1800			ns	SCK Input
		1818		80000	ns	SCK Output
SCK Low Time	t_{KKL}	700			ns	SCK Input
		759			ns	SCK Output
SCK High Time	t_{KKH}	700			ns	SCK Input
		759			ns	SCK Output
SI Set-up Time to SCK TE	t_{SIS}	200			ns	
SI Hold Time after SCK TE	t_{SIH}	500			ns	
SCK LE to SO Delay Time	t_{KO}			550	ns	

Notes: Input timings are measured at V_{IH} min and V_{IL} max
Output timings are measured at V_{OH} = 2.4V and V_{OL} = 0.45V with 1-TTL + 200pF = load
LE is leading edge, TE is trailing edge

Capacitance

T_a = 25°C; V_{CC} = GND = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			15	pF	f_C = 1MHz
Output Capacitance	C_O			15	pF	Unmeasured pins returned to 0V
I/O Capacitance	$C_{I/O}$			15	pF	

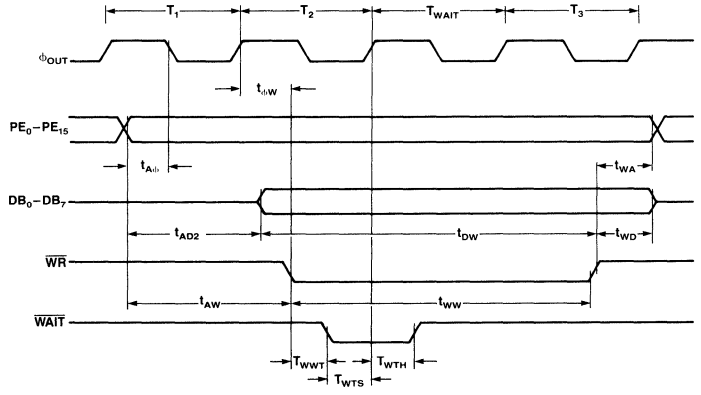
AC Characteristics

T_a = −10°C to +70°C; V_{CC} = +5V ± 10%

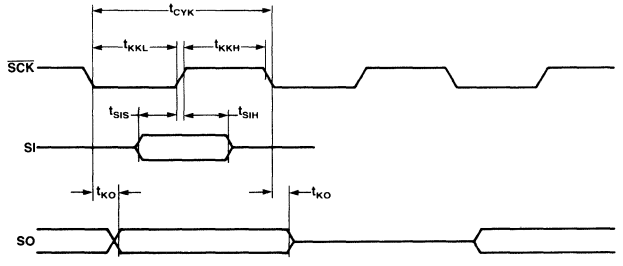
Clock Timing

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
X_1 Input Cycle Time	t_{CYX}	227		10000	ns	
X_1 Input Low Time	t_{XXL}	106			ns	
X_1 Input High Time	t_{XXH}	106			ns	
ϕ_{OUT} Cycle Time	$t_{CY\phi}$	908		40000	ns	
ϕ_{OUT} Low Time	$t_{\phi\phi L}$	300			ns	
ϕ_{OUT} High Time	$t_{\phi\phi H}$	300			ns	
ϕ_{OUT} Rise/Fall Time	t_R, t_F			150	ns	

Write Operation

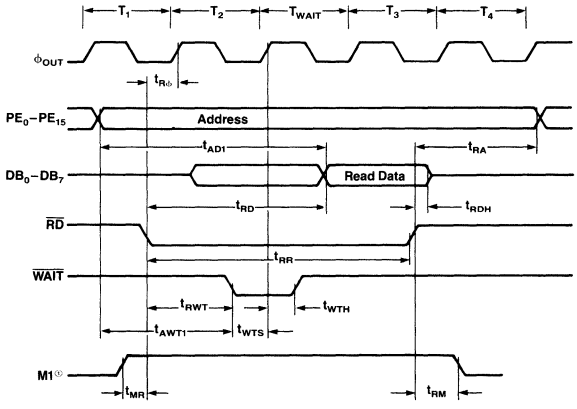


Serial Operation



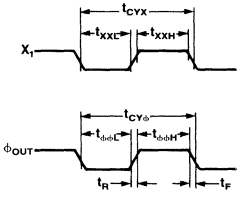
Timing Waveforms (Cont.)

Read Operation



Note: ① Applies only to μPD78C05

Clock Timing



Package Outlines

For information, see Package Outline Section 7.

Plastic Miniflat, μPD78C06G

Plastic Quil, μPD78C05G

NEC

PRELIMINARY

μPD7809/μPD7807/μPD78P09 HIGH END SINGLE CHIP 8-BIT MICROCOMPUTER WITH COMPARATOR, 8K ROM

Description

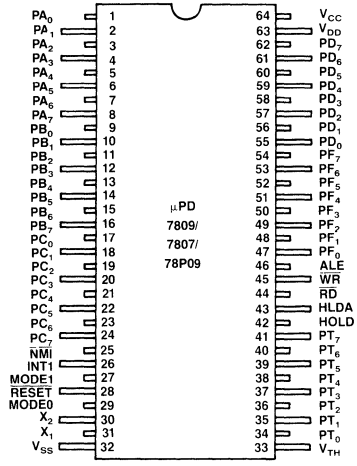
The μPD7809/7807/78P09 single chip microcomputer augments the high-end in NEC's family of 8-bit microcomputers with sophisticated on-chip peripheral functionality. Like its nearest relative in the family, the μPD7811, this device has a fast internal 16-bit ALU and data paths, 256 bytes of RAM, multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs. Features that distinguish this device in the NEC 8-bit family are: 8K ROM, programmable threshold comparator (8 inputs), programmable WAIT function, watchdog timer, hold and hold acknowledge for DMA interface, and bit test/write instructions for both RAM and I/O.

The μPD7809 is the mask-ROM version with the customer's program on chip. The μPD7807 is the ROM-less version for prototyping and small volume applications. The μPD78P09 is an EPROM version of the 8K ROM μPD7809.

Features

- ☐ NMOS silicon gate technology requiring +5v supply
- ☐ Complete single chip microcomputer
  - — 16-bit ALU
  - — 8K ROM
  - 256 bytes RAM
- ☐ Large I/O capability
  - — 40 I/O port lines (μPD7809)
  - — 28 I/O port lines (μPD7807)
  - — 8 input lines
- ☐ Two zero-cross detect inputs
- ☐ Expansion capability (total of 64K memory access)
  - — 8085A bus compatible
  - — 56K bytes external memory address range
- ☐ Programmable threshold comparator
  - — 8 inputs, 1 of 16 software selectable levels
- ☐ Full duplex USART
  - — Synchronous and asynchronous
- ☐ 165 powerful instructions
  - — 16-bit arithmetic, multiply and divide
- ☐ 1μs instruction cycle time
- ☐ Prioritized interrupt structure
  - — 3 external
  - — 8 internal
- ☐ Hold, hold acknowledge for DMA interface
- ☐ Programmable WAIT function
- ☐ Watchdog timer
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-pin QUIL package

Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output Reset places all lines of Port B in input mode
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port Each line independently programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer Reset puts Port C in Port mode and all lines in input mode. — Transmit Data (TxD): Serial data output terminal
18	PC_1	Receive Data (RxD): Serial data input terminal.
19	PC_2	Serial Clock (SCK): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3	Timer Input (TI)/interrupt request input (INT_2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4	Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5	Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7	Counter Outputs 0, 1 (CO_0–CO_1). Programmable rectangular wave output terminal based on timer/event counter

4

Pin Identification (Cont.)

Pin No.	Pin Symbol	Function	
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt (NMI) input.	
26	INT_1	This signal is a rising-edge, maskable interrupt input This input is also used to make the zero-cross detection AC input.	
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch	
28	RESET	(Input, active low), RESET initializes the μPD7811.	
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to ouput IO/M.	
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.	
32	V_{SS}	Power supply ground potential.	
33	V_{TH}	V_{TH} threshold voltage input. Reference voltage for variable threshold input, Port T. Threshold voltage to each Port T input is software programmable to 16 different levels.	
34–41	PT_1–PT_7	Eight variable threshold input ports. Ports T_0–T_7 inputs are each connected internally to comparators where the other input is the threshold voltage.	
42	HOLD	HOLD request input. When high, CPU is in a HOLD state until HOLD goes low.	
43	HLDA	HOLD Acknowledge output by CPU when HOLD state is accepted; goes low when HOLD is released.	
44	$\overline{RD}$	(Three-state output, active low) RD is used as a strobe to gate data from external devices onto the data bus. RD goes high during Reset.	
45	$\overline{WR}$	(Three-state output, active low) WR, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. WR goes high during Reset.	
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.	
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output.	Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output.	Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This is a backup power terminal for on-chip RAM.	
64	V_{CC}	+5V power supply.	

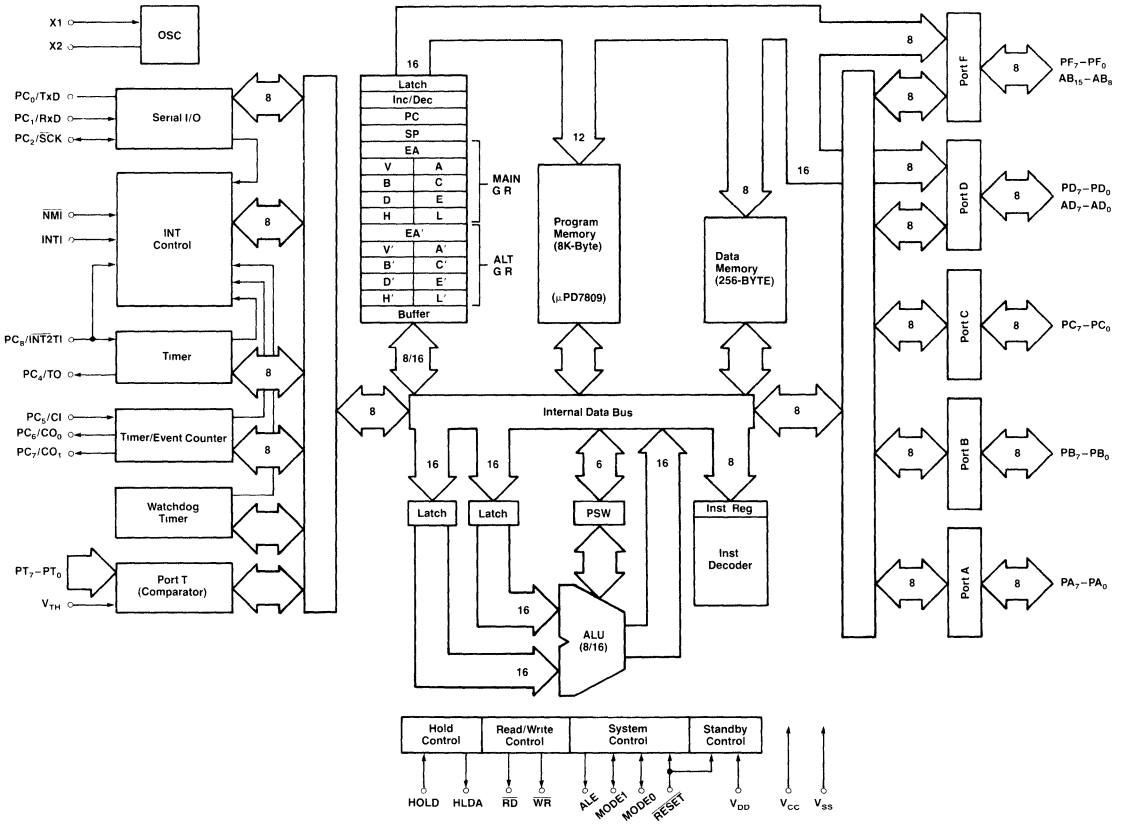
Notes: 1 clock cycle = 1 CL = 3/f
1 machine cycle = 3 or 4 clock cycles
1 instruction cycle = 1 to 19 machine cycles
f System clock frequency (MHz)

Instruction Set

In addition to the basic 7800 family instruction set, the following instructions are incorporated in the μPD7809/7807/78P09:

- ☐ 16-bit data transfers between memory, registers, and extended accumulator
- ☐ 16-bit addition and subtraction
- ☐ 16-bit comparison and skip
- ☐ 16-bit and, or, ex-or operation
- ☐ 16-bit data shift and rotation
- ☐ Multiply
  8-bit by 8-bit, 16-bit product
  Less than 8μs execution
- ☐ Divide
  16-bit by 8-bit, 16-bit quotient, 8-bit remainder
  Less than 14μs execution
- ☐ Working register instructions for efficient RAM addressing, testing and manipulating
- ☐ Direct bit addressing for code-efficient addressing, testing and manipulating bits in RAM, port lines and mode registers

Block Diagram



Note: The μPD7807 has no on chip ROM (8K bytes)

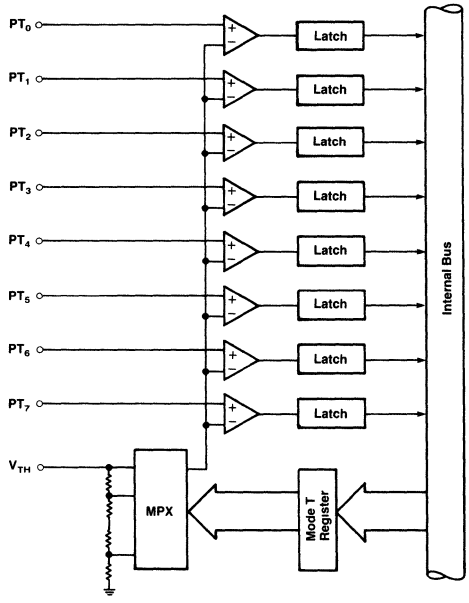
Please refer to the section on μPD7811 for description of the following functions which are the same as on this device:

1. Memory expansion (except 56K bytes maximum for μPD7809)
2. Timer/event counter
3. USART
4. Interrupt structure
5. Standby function
6. Reset
7. External memory access and timing
8. Package information

Variable Threshold Input Port (Port T)

- ☐ 8 input lines
- ☐ 16 levels — from 1/16 of reference voltage (V_{TH}) to 16/16 V_{TH}
- ☐ Level selected by software write to Mode T register
- ☐ Input at Port bit reads 0 until voltage at pin exceeds selected level
- ☐ Comparison execution time: 12μs.

Block Diagram of Threshold Variable Input Port



Input/Output

- ☐ 40 digital I/O lines — Five 8-bit ports (Port A, Port B, Port C, Port D, Port F)
- ☐ Port operation for Ports A, B, C, and F:
  Each line of these ports can be individually programmed as an input or as an output.
- ☐ Port D can be programmed as a byte input or a byte output.
- ☐ Control lines:
  Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter.

Block Diagram of Threshold Variable Port

Format of MODE T Register

7	6	5	4	3	2	1	0
–	–	–	–	MT_3	MT_2	MT_1	MT_0

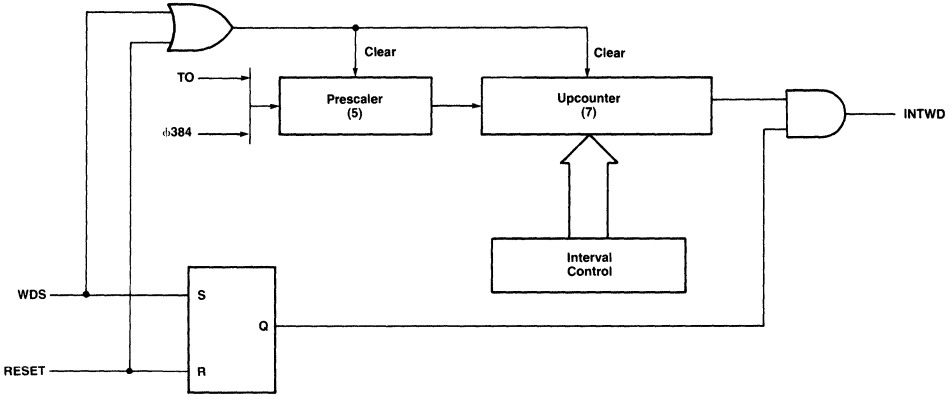
Specification of 16 Threshold Levels

0	0	0	0	$V_{TH} \times 16/16$
0	0	0	1	$V_{TH} \times 1/16$
0	0	1	0	$V_{TH} \times 2/16$
0	0	1	1	$V_{TH} \times 3/16$
0	1	0	0	$V_{TH} \times 4/16$
0	1	0	1	$V_{TH} \times 5/16$
0	1	1	0	$V_{TH} \times 6/16$
0	1	1	1	$V_{TH} \times 7/16$
1	0	0	0	$V_{TH} \times 8/16$
1	0	0	1	$V_{TH} \times 9/16$
1	0	1	0	$V_{TH} \times 10/16$
1	0	1	1	$V_{TH} \times 11/16$
1	1	0	0	$V_{TH} \times 12/16$
1	1	0	1	$V_{TH} \times 13/16$
1	1	1	0	$V_{TH} \times 14/16$
1	1	1	1	$V_{TH} \times 15/16$

Watchdog Timer

☐ Used for software safety check or overall performance safety check. Watchdog, if enabled, must be cleared at regular intervals in program execution to avoid watchdog interrupt. Intervals are software selectable.

Block Diagram for Watchdog Timer



Note: $\phi 384 = f_{XTAL} \times 1/384$

Bit Address Instructions

The following bits may be addressed directly with certain instructions:

☐ Any bit in a 16-byte group in RAM
☐ Any bit in the five 8-bit I/O ports (A, B, C, D, F)
☐ Any bit in the variable threshold port
☐ Any bit in the following special registers:
9-bit interrupt mask register, serial mode register, timer mode register, timer/event counter output register

An addressed bit may be tested, set, cleared, or complemented.
An addressed bit may be moved to or from the carry flag.
An addressed bit may be ANDed, ORed, X-ORed with the carry flag.

Difference between the μPD7801, μPD7811, μPD7807, and μPD7809

		μPD7801	μPD7811	μPD7807	μPD7809
Number of Instructions		134	158	165	165
16-bit Operation Instruction		No	Yes	Yes	Yes
Multiply/Divide Instruction		No	Yes	Yes	Yes
Instruction Cycle		2μs/4MHz	1μs/12MHz	1μs/12MHz	1μs/12MHz
Number of General-purpose Registers		16	18	18	18
On-chip ROM Capacity		4K Bytes	4K Bytes	No	8K Bytes
On-chip RAM Capacity		128 Bytes	256 Bytes	256 Bytes	256 Bytes
Direct-Addressable External Memory Capacity		60K Bytes	60K Bytes	64K Bytes	56K Bytes
Interrupt Source	Internal	2	8	8	8
	External	3	3	3	3
I/O Lines		48	40+4	28*	40
Threshold Variable Port		No	No	8 Bits	8 Bits
Timer/Counter	Timer	12 Bits	8 Bits x 2	8 Bits x 2	8 Bits x 2
	Counter	No	16 Bits	16 Bits	16 Bits
Watchdog Timer		No	No	Yes	Yes
Serial Interface	Asynchronous	No	Yes	Yes	Yes
	Synchronous	No	Yes	Yes	Yes
	I/O Interface	Yes	Yes	Yes	Yes
A/D Converter		No	Yes	No	No
Standby Function		No	Yes	Yes	Yes
Hold Function		Yes	No	Yes	Yes
Technology		NMOS	NMOS	NMOS	NMOS
Package		64-Pin Flat	64-Pin QUIP	64-Pin QUIP	64-Pin QUIP

* at 4K-byte Access

Package Outlines

For information, see Package Outline Section 7.

Plastic Quil, μPD7807G/09G
Plastic Shrinkdip, μPD7809CW/07CW

Notes

μPD7810/μPD7811 HIGH-END SINGLE-CHIP 8-BIT MICROCOMPUTER WITH A/D CONVERTER

Description

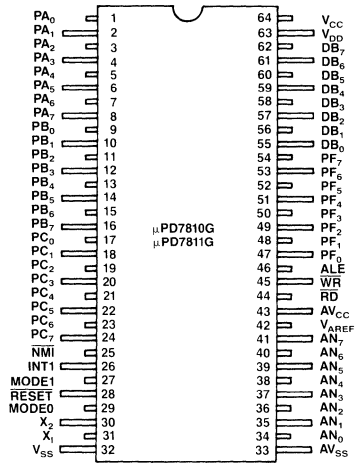
The NEC μPD7810/μPD7811 is a high-performance single-chip microcomputer integrating sophisticated on-chip peripheral functionality normally provided by external components. The device's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the μPD7810/7811 appropriate in data processing as well as control applications. The device integrates a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART and two zero-cross detect inputs on a single die, to direct the device into fast, high-end processing applications involving analog signal interface and processing.

The μPD7811 is the mask-ROM high volume production device embedded with custom customer program. The μPD7810 is a ROM-less version for prototyping and small volume production. The μPD78PG11E is a piggy-back EPROM version for design development.

Features

- ☐ NMOS silicon gate technology requiring +5V supply
- ☐ Complete single-chip microcomputer
  - 16-bit ALU
  - 4K-ROM
  - 256-byte RAM
- ☐ 44 I/O lines
- ☐ Two zero-cross detect inputs
- ☐ Two 8-bit timers
- ☐ Multifunction 16-bit timer/event counter
- ☐ Expansion capabilities
  - 8085A bus compatible
  - 60K-byte external memory address range
- ☐ 8-channel, 8-bit A/D converter
  - Auto scan
  - Channel select
- ☐ Full duplex USART
  - Synchronous and asynchronous
- ☐ 153 instruction set
  - 16-bit arithmetic, multiply and divide
- ☐ 1μs instruction cycle time (12MHz operation)
- ☐ Prioritized interrupt structure
  - 2 external
  - 4 internal
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-quil package

Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1–8	PA_0–PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode
9–16	PB_0–PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.
17	PC_0	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer. Reset puts Port C in Port mode and all lines in input mode. — Transmit Data (TxD): Serial data output terminal.
18	PC_1	Receive Data (RxD): Serial data input terminal.
19	PC_2	Serial Clock (SCK): Serial clock input/output terminal. When internal clock is used, the output can be selected; when an external clock is used, the input can be selected.
20	PC_3	Timer Input (TI)/interrupt request input (INT_2): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4	Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5	Counter Input (CI): External pulse input terminal to the timer/event counter.
23–24	PC_6, PC_7	Counter Outputs 0, 1 (CO_0–CO_1): Programmable rectangular wave output terminal based on timer/event counter.

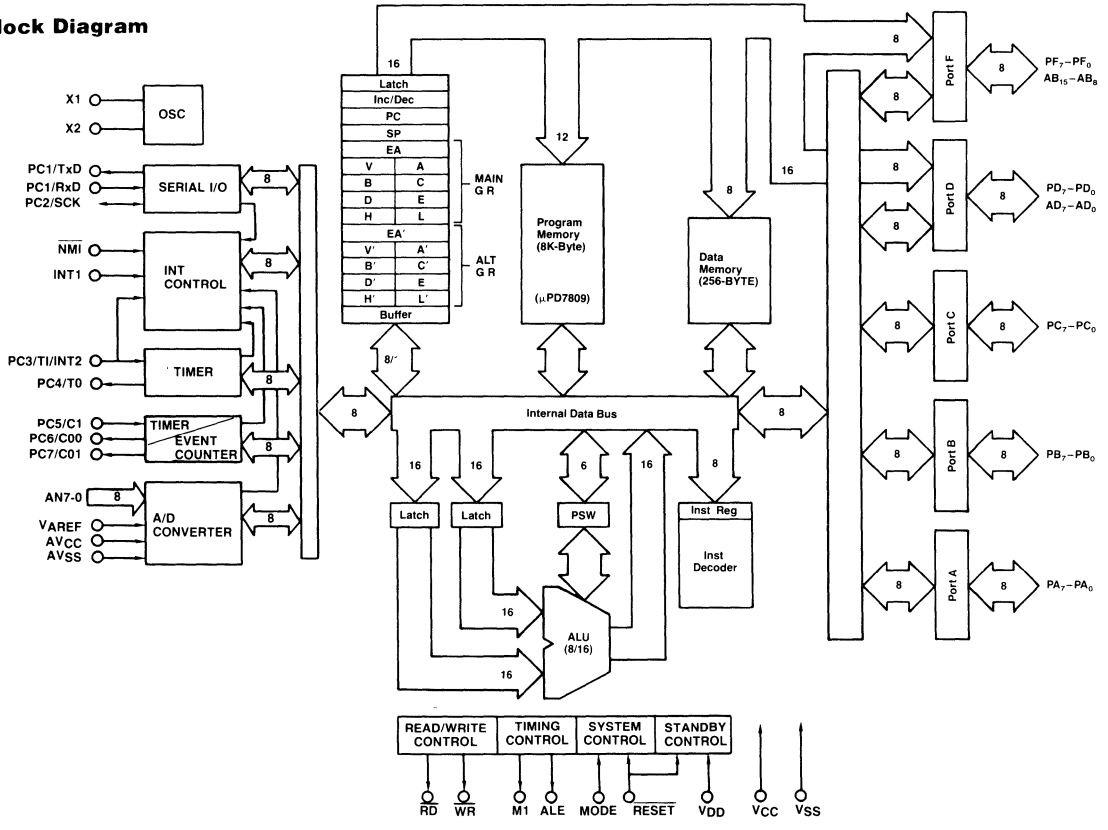
Pin Identification (Cont.)

Pin No.	Pin Symbol	Function
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.
26	INT_1	This signal is a rising-edge, maskable interrupt input This input is also used to make the zero-cross detection AC input.
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 Signal during each opcode fetch.
28	$\overline{RESET}$	(Input, active low), $\overline{RESET}$ initializes the μPD7811.
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to ouput IO/M.
30–31	X_2, X_1 (crystal)	This is a crystal connection terminal for system clock oscillation. When an external clock is supplied X_1 is the input.
32	V_{SS}	Power supply ground potential.
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion range lower limit.
34–41	AN_0–AN_7	Eight analog inputs to the A/D converter. AN_7–AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.

Pin No.	Pin Symbol	Function	
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.	
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.	
46	ALE	The strobe signal is for latching the address signal to the output from PD_7–PD_0 when accessing external expansion memory.	
47–54	PF_0–PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output	Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55–62	DB_0–DB_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output.	Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	This is a backup power terminal for on-chip RAM.	
64	V_{CC}	+5V power supply.	

Notes: 1 clock cycle = 1 CL = 3/f
1 machine cycle = 3 or 4 clock cycles
1 instruction cycle = 1 to 19 machine cycles
f System clock frequency (MHz)

Block Diagram

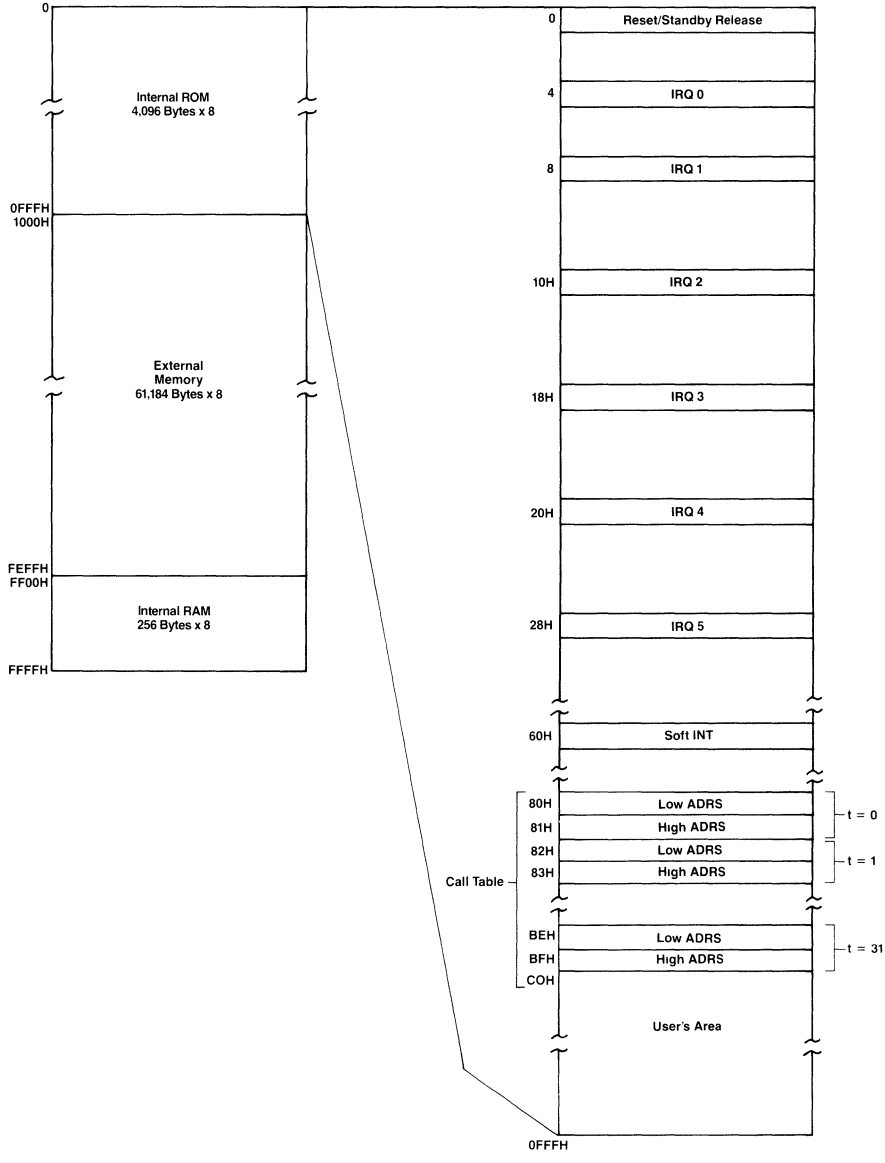


Functional Index

Memory map

The μPD7811 can directly address up to 64K-bytes of memory. Except for the on-chip ROM(0-4095) and RAM(65280-65535), any memory location can be used as ROM or RAM. The following memory map defines the 0–64K-byte memory space for the μPD7811.

Memory Map



Input/Output

8 Analog Input Lines

44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4–AN_7)

1. Analog Input Lines
   AN_0–AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   – Port A, Port B, Port C, Port F
   Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latched outputs, high-impedance inputs.
   – Port D
   Port D can be programmed as a byte input or a byte output.
   – AN_4–AN_7
   The high-order analog input lines, AN_4–AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer and timer/counter.
4. Memory Expansion
   In addition to the single-chip operation mode μPD7811 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

Memory Expansion	Port Configuration	
None	Port D	I/O Port
	Port F	I/O Port
256 Bytes	Port D	Multiplexed Address/Data Bus
	Port F	I/O Port
4K Bytes	Port D	Multiplexed Address/Data Bus
	Port F_0–F_3	Address Bus
	Port F_4–F_7	I/O Port
16K Bytes	Port D	Multiplexed Address/Data Bus
	Port F_0–F_5	Address Bus
	Port F_6–F_7	I/O Port
60K Bytes	Port D	Multiplexed Address/Data Bus
	Port F	Address Bus

Timers

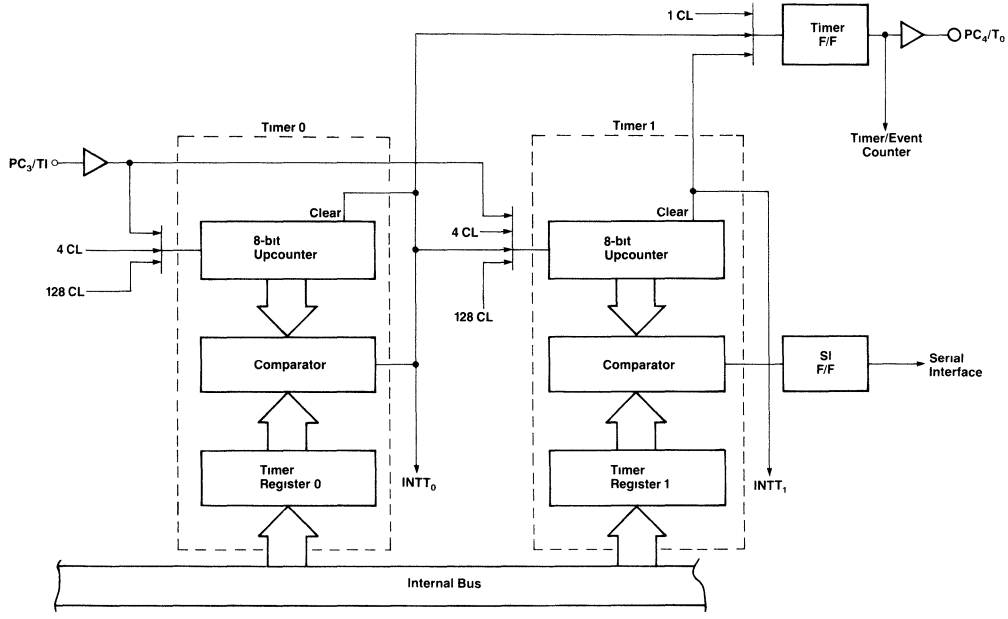
The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set in software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at T_1.

Timer/Event Counter

The 16-bit multifunctional timer/event counter can be used for the following operations:

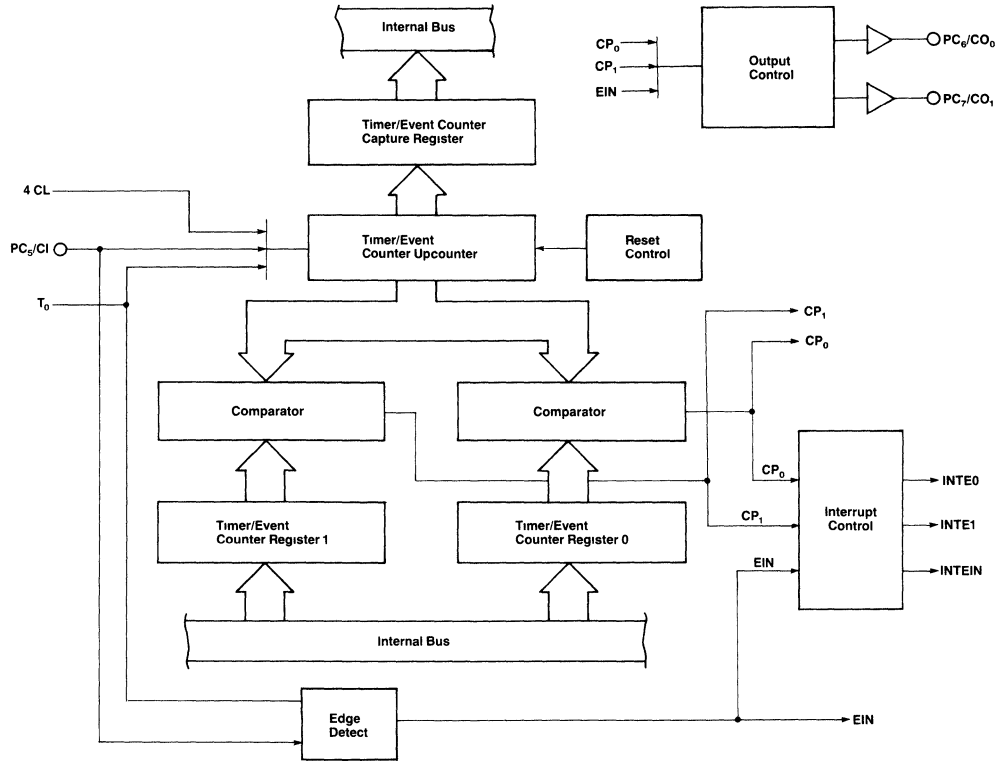
Interval timer
External event timer
Frequency measurement
Pulse width measurement
Programmable square-wave output

Timer Block Diagram



Notes: 1 CL = 3/f (250ns 12MHz operation)
f System clock frequency (MHz)

Block Diagram for Timer/Event Counter



Notes: CL = 3/f (250ns 12 MHz operation)
f System clock frequency (MHz)

8-Bit A/D Converter

8 Input Channels
4 Conversion Result Registers
2 Powerful Operation Modes
  Auto Scan Mode
  Channel Select Mode
Successive Approximation Technique

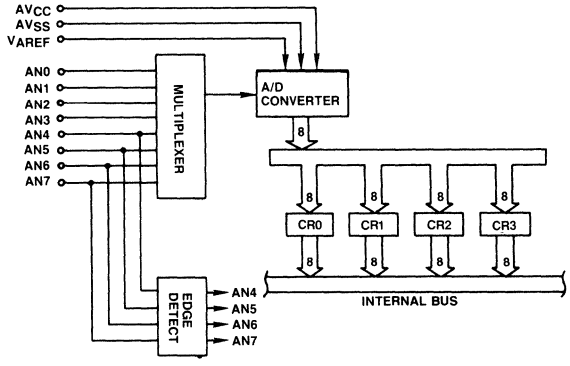
Absolute Accuracy	± 1.5 LSB (± 0.6%)
Conversion Range	0 ~ 5V
Conversion Time	50 μs

Interrupt Generation

Analog/Digital Converter

The μPD7810/7811 features an 8-bit, high-speed, high accuracy A/D converter. The A/D converter comprises a 256-Resistor Ladder and Successive Approximation Register (SAR). There are four conversion result registers (CR_0–CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0–CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

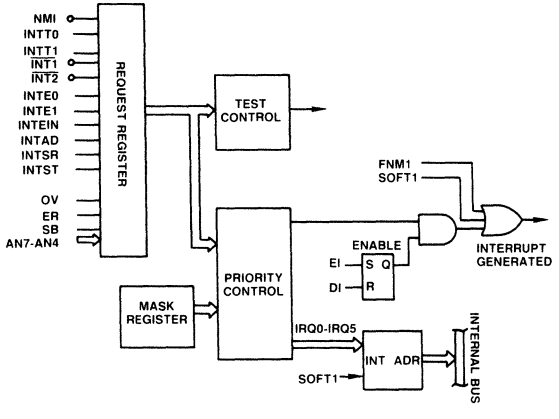
A/D Converter Block Diagram



Interrupt Structure

There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

Interrupt Request	Interrupt	Type of Interrupt	In/Ext
IRQ0	4	NMI (Non-maskable interrupt)	External
IRQ1	8	INTT0 (Coincidence signal from timer 0) INTT1 (Coincidence signal from timer 1)	Internal
IRQ2	16	INT1 (Maskable interrupt) INT2 (Maskable interrupt)	External
IRQ3	24	INTE0 (Coincidence signal from timer/event counter) INTE1 (Coincidence signal from timer/event counter)	Internal
IRQ4	32	INTEIN (Falling signal of C1 and T0 counter) INTAD (A/D converter interrupt)	In/External
IRQ5	40	INTSR (Serial receive interrupt) INST (Serial send interrupt)	Internal



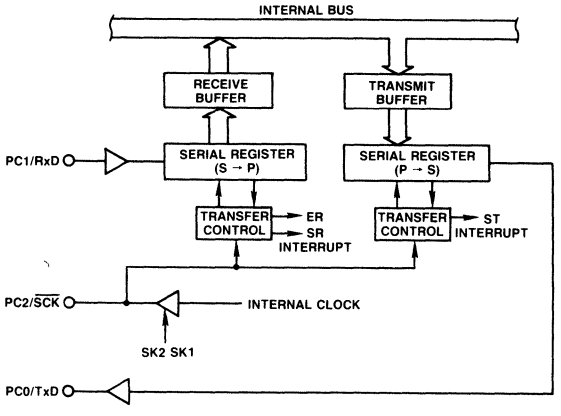
Standby Function

The μPD7810/7811 offers a standby function that allows the user to save up to 32 bytes of RAM with back-up power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD7811 checks whether recovery was made from standby mode or from cold start.

Universal Serial Interface

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data is transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

Universal Serial Interface Block Diagram



Zero-crossing Detector

The INT_1 and INT_2 terminals (used common to TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

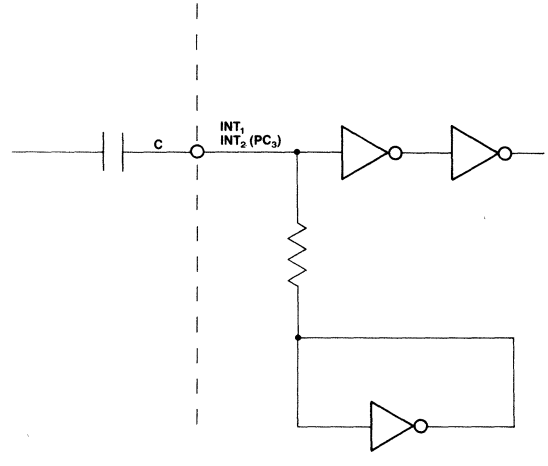
To utilize the zero-cross detection mode, an AC signal of approximately 1–3V AC peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT_1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT_1 interrupt is generated.

For the INT_2 pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and INT_2 interrupt is generated.

The zero-cross detection capability allows the user to make the 50–60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

Zero-crossing Detection Circuit



Operand Format/Description

Format	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD,PF, MKH MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM,MCC, MA, MB, MC MF, TXB, TM0, TM1
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM
sr3	ETM0, ETM1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D−, H−, D+byte, H+A, H+B, H+EA, H+byte
rpa3	D, H, D+, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8-bit immediate data
word	16-bit immediate data
byte	8-bit immediate data
bit	3-bit immediate data
f	CY, HC, Z
irf	FNMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FAD, FSR, FST, ER, OV, AN4, AN5, AN6, AN7, SB

Remarks

1. sr–sr4 (special register)

PA	= Port A	ECNT	= Timer/Event Counter Upcounter
PB	= Port B	ECPT	= Timer/Event Counter Capture
PC	= Port C	ETMM	= Timer/Event Counter Mode
PD	= Port D	EOM	= Timer/Event Counter Output Mode
PF	= Port F	ANM	= A/D Channel Mode
MA	= Mode A	CR0 to CR3	= A/D Conversion Result 0–3
MB	= Mode B	TXB	= Tx Buffer
MC	= Mode C	RXB	= Rx Buffer
MCC	= Mode Control C	SMH	= Serial Mode High
MF	= Mode F	SML	= Serial Mode Low
MM	= Memory Mapping	MKH	= Mask High
TM0	= Timer Register 0	MKL	= Mask Low
TM1	= Timer Register 1		
TMM	= Timer Mode		
ETM0	= Timer/Event Counter Register 0		
ETM1	= Timer/Event Counter Register 1		

2. rp–rp3 (register pair)

SP	= Stack Pointer	H	= HL
B	= BC	V	= VA
D	= DE	EA	= Extended Accumulator

3. rpa–rpa3 (rp addressing)

B	= (BC)	D++	= $(DE)^{++}$
D	= (DE)	H++	= $(HL)^{++}$
H	= (HL)	D + byte	= (DE + byte)
D+	= $(DE)^{+}$	H + A	= (HL + A)
H+	= $(HL)^{+}$	H + B	= (HL + B)
D−	= $(DE)^{-}$	H + EA	= (HL + EA)
H−	= $(HL)^{-}$	H + byte	= (HL + byte)

4. f (flag)

CY = Carry HC = Half Carry Z = Zero

5. irf (interrupt flag)

FNMI	= INTFNMI	FSR	= INTFSR
FT0	= INTFT0	FST	= INTFST
FT1	= INTFT1	ER	= Error
F1	= INTF1	OV	= Overflow
F2	= INTF2	AN4 to AN7	= Analog Input 4–7
FE0	= INTFE0		
FE1	= INTFE1		
FEIN	= INTFEIN	SB	= Standby
FAD	= INTFAD		

4

Instruction Groups

8-bit Data Transfer

Mnemonic		Operand	OP Code B1	B2	B3	B4	State	Operation	Skip Condition
MOV		r1, A	00011$T_2T_1T_0$				4	r1 ← A	
		A, r1	00001$T_2T_1T_0$				4	A ← r1	
	*	sr, A	01001101	110$S_4S_3S_2S_1S_0$			10	sr ← A	
	*	A, sr1	01001100	11$S_5S_4S_3S_2S_1S_0$			10	A ← sr1	
		r, (word)	01110000	01101$R_2R_1R_0$	Low Adrs	High Adrs	17	r ← (word)	
		(word), r	01110000	01111$R_2R_1R_0$	Low Adrs	High Adrs	17	(word) ← r	
MVI	*	r, byte	01101$R_2R_1R_0$	Data			7	r ← byte String skip, other r = A or L	
		sr2, byte	01100100	$S_3$0000$S_2S_1S_0$	Data		14	sr2 ← byte	
MVIW	*	wa, byte	01110001	Offset	Data		13	(V, wa) ← byte	
MVIX	*	rpa1, byte	01001$0A_1A_0$	Data			10	(rpa1) ← byte	
STAW	*	wa	01100011	Offset			10	(V, wa) ← A	
LDAW	*	wa	00000001	Offset			10	A ← (V, wa)	
STAX	*	rpa2	$A_3$0111$A_2A_1A_0$	Data *①			7/13	(rpa2) ← A	
LDAX	*	rpa2	$A_3$0101$A_2A_1A_0$	Data *①			7/13	A ← (rpa2)	
EXX			01001000	10101111			8	B ↔ B′, C ↔ C′, D ↔ D′ E ↔ E′, H ↔ H′, L ↔ L′	
EXA			01001000	10101100			8	V, A ↔ V′, A′, EA ↔ EA′	
EXH			01001000	10101110			8	H, L ↔ H′, L′	

16-bit Data Transfer

BLOCK		D+	00010000				13 (C + 1)	(DE) + ← (HL) +, C ← C − 1 End if borrow	
		D−	00010001				13 (C + 1)	(DE) − ← (HL) −, C ← C − 1 End if borrow	
DMOV		rp3, EA	101101P_1P_0				4	$rp3_L$ ← EAL, $rp3_H$ ← EAH	
		EA, rp3	101001P_1P_0				4	EAL ← $rp3_L$, EAH ← $rp3_H$	
		sr3, EA	01001000	1101001U_0			14	sr3 ← EA	
		EA, sr4	↓	110000V_1V_0			14	EA ← sr4	
SBCD		(word)	01110000	00011110	Low Adrs	High Adrs	20	(word) ← C, (word + 1) ← B	
SDED		(word)	↓	00101110	↓	↓	20	(word) ← E, (word + 1) ← D	
SHLD		(word)	↓	00111110	↓	↓	20	(word) ← L, (word + 1) ← H	
SSPD		(word)	↓	00001110	↓	↓	20	(word) ← SP_L, (word + 1) ← SP_H	
STEAX		rpa3	01001000	1001$C_3C_2C_1C_0$	Data *②	↓	14/20	(rpa3) ← EAL, (rpa3 + 1) ← EAH	
LBCD		word	01110000	00011111	Low Adrs	High Adrs	20	C ← (word), B ← (word + 1)	
LDED		word	↓	00101111	↓	↓	20	E ← (word), D ← (word + 1)	
LHLD		word	↓	00111111	↓	↓	20	L ← (word), H ← (word + 1)	
LSPD		word	↓	00001111	↓	↓	20	SP_L ← (word), SP_H ← (word + 1)	
LDEAX		rpa3	01001000	1000$C_3C_2C_1C_0$	Data *②	↓	14/20	EAL ← (rpa3), EAH ← (rpa3 + 1)	
PUSH		rp1	10110$Q_2Q_1Q_0$				13	(SP − 1) ← $rp1_H$ ← (SP − 2) ← $rp1_L$ SP ← SP − 2	
POP		rp1	10100$Q_2Q_1Q_0$				10	$rp1_L$ ← (SP), $rp1_H$ ← (SP + 1) SP ← SP + 2	
LXI		rp2, word	0$P_2P_1P_0$0100		Low Byte	High Byte	10	rp2 ← (word) String skip when rp2 = H	

8-bit Arithmetic (Register)

TABLE			01001000	10101000			17	C ← (PC + 3 + A) B ← (PC + 3 + A + 1)	
ADD		A, r	01100000	11000$R_2R_1R_0$			8	A ← A + r	
		r, A	↓	01000$R_2R_1R_0$			8	r ← r + A	
ADC		A, r	↓	11010$R_2R_1R_0$			8	A ← A + r + CY	
		r, A	↓	01010$R_2R_1R_0$			8	r ← r + A + CY	
ADDNC		A, r	↓	10100$R_2R_1R_0$			8	A ← A + r	No Carry
		r, A	↓	00100$R_2R_1R_0$			8	r ← r + A	No Carry
SUB		A, r	↓	11100$R_2R_1R_0$			8	A ← A − r	
		r, A	↓	01100$R_2R_1R_0$			8	r ← r − A	
SBB		A, r	↓	11110$R_2R_1R_0$			8	A ← A − r − CY	
		r, A	↓	01110$R_2R_1R_0$			8	r ← r − A − CY	
SUBNB		A, r	↓	10110$R_2R_1R_0$			8	A ← A − r	No Borrow
		r, A	↓	00110$R_2R_1R_0$			8	r ← r − A	No Borrow
ANA		A, r	↓	10001$R_2R_1R_0$			8	A ← A ∧ r	
		r, A	↓	00001$R_2R_1R_0$			8	r ← r ∧ A	
ORA		A, r	↓	10011$R_2R_1R_0$			8	A ← A ∨ r	
		r, A	↓	00011$R_2R_1R_0$			8	r ← r ∨ A	
XRA		A, r	↓	10010$R_2R_1R_0$			8	A ← A ∨̄ r	
		r, A	↓	00010$R_2R_1R_0$			8	r ← r ∨̄ A	
GTA		A, r	↓	10101$R_2R_1R_0$			8	A − r − 1	No Borrow
		r, A	↓	00101$R_2R_1R_0$			8	r − A − 1	No Borrow

Instruction Groups (Cont.)

			OP Code					
Mnemonic	Operand	B1	B2	B3	B4	State	Operation	Skip Condition
8-bit Arithmetic (Register) (Cont.)								
LTA	A, r	01100000	10111$R_2R_1R_0$			8	A − r	Borrow
	r, A		00111$R_2R_1R_0$			8	r − A	Borrow
NEA	A, r		11101$R_2R_1R_0$			8	A − r	No Zero
	r, A		01101$R_2R_1R_0$			8	r − A	No Zero
EQA	A, r		11111$R_2R_1R_0$			8	A − r	Zero
	r, A		01111$R_2R_1R_0$			8	r − A	Zero
ONA	A, r		11001$R_2R_1R_0$			8	A ∧ R	No Zero
OFFA	A, r		11011$R_2R_1R_0$			8	A ∧ R	Zero
8-bit Arithmetic (Memory)								
ADDX	rpa	01110000	11000$A_2A_1A_0$			11	A ← A + (rpa)	
ADCX	rpa		11010$A_2A_1A_0$			11	A ← A + (rpa) + CY	
ADDNCX	rpa		10100$A_2A_1A_0$			11	A ← A + (rpa)	No Carry
SUBX	rpa		11100$A_2A_1A_0$			11	A ← A − (rpa)	
SBBX	rpa		11110$A_2A_1A_0$			11	A ← A − (rpa) − CY	
SUBNBX	rpa		10110$A_2A_1A_0$			11	A ← A − (rpa)	No Borrow
ANAX	rpa		10001$A_2A_1A_0$			11	A ← A − (rpa)	
ORAX	rpa		10011$A_2A_1A_0$			11	A ← A V (rpa)	
XRAX	rpa		10010$A_2A_1A_0$			11	A ← A ¥ (rpa)	
GTAX	rpa		10101$A_2A_1A_0$			11	A − (rpa) − 1	No Borrow
LTAX	rpa		10111$A_2A_1A_0$			11	A − (rpa)	Borrow
Immediate Data								
NEAX	rpa		11101$A_2A_1A_0$			11	A − (rpa)	No Zero
EQAX	rpa		11111$A_2A_1A_0$			11	A − (rpa)	Zero
ONAX	rpa		11001$A_2A_1A_0$			11	A ← (rpa)	No Zero
OFFAX	rpa		11011$A_2A_1A_0$			11	A ← (rpa)	Zero
ADI *	A, byte	01000110	← Data →			7	A ← A + byte	
	r, byte	01110100	01000$R_2R_1R_0$	Data		11	r ← r + byte	
	sr2, byte	0110	$S_3$1000$S_2S_1S_0$	↓		20	sr2 ← sr2 + byte	
ACI *	A, byte	01010110	← Data →			7	A ← A + byte + CY	
	r, byte	01110100	01010$R_2R_1R_0$	Data		11	r ← r + byte + CY	
	sr2, byte	0110	$S_3$1010$S_2S_1S_0$	↓		20	sr2 ← sr2 + byte + CY	
ADINC *	A, byte	00100110	← Data →			7	A ← A + byte	No Carry
	r, byte	01110100	00100$R_2R_1R_0$	Data		11	r ← r + byte	No Carry
	sr2, byte	0110	$S_3$0100$S_2S_1S_0$	↓		20	sr2 ← sr2 + byte	No Carry
SUI *	A, byte	01100110	← Data →			7	A ← A − byte	
	r, byte	01110100	01100$R_2R_1R_0$	Data		11	r ← r − byte	
	sr2, byte	0110	$S_3$1100$S_2S_1S_0$	↓		20	sr2 ← sr2 − byte	
SBI *	A, byte	01110110	← Data →			7	A ← A − byte − CY	
	r, byte	01110100	01110$R_2R_1R_0$	Data		11	r ← r − byte − CY	
	sr2, byte	0110	$S_3$1110$S_2S_1S_0$	↓		20	sr2 ← sr2 − byte − CY	
SUINB *	A, byte	00110110	Data			7	A ← A − byte	No Borrow
	r, byte	01110100	00110$R_2R_1R_0$			11	r ← r − byte	No Borrow
	sr2, byte	0110 ↓	$S_3$0110$S_2S_1S_0$			20	sr2 ← sr2 ← byte	No Borrow
ANI *	A, byte	00000111	Data			7	A ← A \ byte	
	r, byte	01110100	00001$R_2R_1R_0$	Data		11	r ← r \ byte	
	sr2, byte	01100100	$S_3$0001$S_2S_1S_0$	↓		20	sr2 ← sr2 \ byte	
ORI *	A, byte	00010111	Data			7	A ← A V byte	
	r, byte	01110100	00011$R_2R_1R_0$	Data		11	r ← r V byte	
	sr2, byte	0110 ↓	$S_3$0011$S_2S_1S_0$	↓		20	sr2 ← sr2 V byte	
XRI *	A, byte	00010110	Data			7	A ← A ¥ byte	
	r, byte	01110100	00010$R_2R_1R_0$	Data		11	r ← r ¥ byte	
	sr2, byte	0110 ↓	$S_3$0010$S_2S_1S_0$	↓		20	sr2 ← sr2 ¥ byte	
GTI *	A, byte	00100111	Data			7	A − byte − 1	No Borrow
	r, byte	01110100	00101$R_2R_1R_0$	Data		11	r − byte − 1	No Borrow
	sr5, byte	0110 ↓	$S_3$0101$S_2S_1S_0$	↓		14	sr5 − byte − 1	No Borrow
LTI *	A, byte	00110111	Data			7	A − byte	Borrow
	r, byte	01110100	00111$R_2R_1R_0$	Data		11	r − byte	Borrow
	sr5, byte	0110 ↓	$S_3$0111$S_2S_1S_0$	↓		14	sr5 − byte	Borrow
NEI *	A, byte	01100111	← Data →			7	A − byte	No Zero
	r, byte	01110100	01101$R_2R_1R_0$	Data		11	r − byte	No Zero
	sr5, byte	0110 ↓	$S_3$1101$S_2S_1S_0$	↓		14	sr5 − byte	No Zero
EQI *	A, byte	01110111	← Data →			7	A − byte	Zero
	r, byte	01110100	01111$R_2R_1R_0$	Data		11	r − byte	Zero
	sr5, byte	0110 ↓	$S_3$1111$S_2S_1S_0$	↓		14	sr5 − byte	Zero

Instruction Groups (Cont.)

Immediate Data (Cont.)

Mnemonic		Operand	OP Code B1	OP Code B2	OP Code B3	OP Code B4	State	Operation	Skip Condition
ONI	*	A, byte	01000111	← Data →			7	A \ byte	No Zero
		r, byte	01110100	01001 $R_2R_1R_0$	Data		11	r \ byte	No Zero
		sr5, byte	0110 ↓	$S_3$1001 $S_2S_1S_0$	↓		14	sr5 \ byte	No Zero
OFFI	*	A, byte	01010111	← Data →			7	A \ byte	Zero
		r, byte	01110100	01011 $R_2R_1R_0$	Data		11	r \ byte	Zero
		sr5, byte	0110 ↓	$S_3$1011 $S_2S_1S_0$	↓		14	sr5 \ byte	Zero

Working Register

ADDW		wa	01110100	11000000	Offset		14	A ← A + (V, wa)	
ADCW		wa		1101			14	A ← A + (V, wa) + CY	
ADDNCW		wa		1010			14	A ← A + (V, wa)	No Carry
SUBW		wa		1110			14	A ← A − (V, wa)	
SBBW		wa		1111			14	A ← A − (V, wa) − CY	
SUBNBW		wa		1011			14	A ← A − (V, wa)	No Borrow
ANAW		wa		10001000			14	A ← A \ (V, wa)	
ORAW		wa		1001			14	A ← A V (V, wa)	
XRAW		wa	01110100	10010000	Offset		14	A ← A ¥ (V, wa)	
GTAW		wa		10101000			14	A − (V, wa) − 1	No Borrow
LTAW		wa		1011			14	A − (V, wa)	Borrow
NEAW		wa		1110			14	A − (V, wa)	No Zero
EQAW		wa		1111			14	A − (V, wa)	Zero
ONAW		wa		1100			14	A \ (V, wa)	No Zero
OFFAW		wa		1101			14	A \ (V, wa)	Zero
ANIW	*	wa, byte	00000101	← Offset →	Data		19	(V, wa) ← (V, wa) [byte]	
ORIW	*	wa, byte	0001				19	(V, wa) ← (V, wa) V byte	
GTIW	*	wa, byte	0010				13	(V, wa) − byte − 1	No Borrow
LTIW	*	wa, byte	0011				13	(V, wa) − byte	Borrow
NEIW	*	wa, byte	0110				13	(V, wa) − byte	No Zero
EQIW	*	wa, byte	0111				13	(V, wa) − byte	Zero
ONIW	*	wa, byte	0100				13	(V, wa) \ byte	No Zero
OFFIW	*	wa, byte	0101				13	(V, wa) \ byte	Zero

16-bit Arithmetic

EADD		EA, r2	01110000	010000 R_1R_0			11	EA ← EA + r2	
DADD		EA, rp3	0100	110001 P_1P_0			11	EA ← EA + rp3	
DADC		EA, rp3		1101			11	EA ← EA + rp3 + CY	
DADDNC		EA, rp3		1010			11	EA ← EA + rp3	No Carry
ESUB		EA, r2	0000	011000 R_1R_0			11	EA ← EA − r2	
DSUB		EA, rp3	01110100	111001 P_1P_0			11	EA ← EA − rp3	
DSBB		EA, rp3		1111			11	EA ← EA − rp3 − CY	
DSUBNB		EA, rp3		1011			11	EA ← EA − rp3	No Borrow
DAN		EA, rp3		100011 P_1P_0			11	EA ← EA − rp3	
DOR		EA, rp3		1001			11	EA ← EA V rp3	
DXR		EA, rp3		100101 P_1P_0			11	EA ← EA ¥ rp3	
DGT		EA, rp3		101011 P_1P_0			11	EA − rp3 − 1	No Borrow
DLT		EA, rp3		1011			11	EA − rp3	Borrow
DNE		EA, rp3		1110			11	EA − rp3	No Zero
DEQ		EA, rp3		1111			11	EA − rp3	Zero
DON		EA, rp3		1100			11	EA Λ rp3	No Zero
DOFF		EA, rp3		1101			11	EA Λ rp3	Zero

Multiply/Divide

MUL		r2	01001000	001011 R_1R_0			32	EA ← A × r2	
DIV		r2	↓	0011 ↓			59	EA ← EA − r2, r2 ← Surplus	

Increment/Decrement

INR		r2	010000 R_1R_0				4	r2 − r2 + 1	Carry
INRW	*	wa	00100000	← Offset →			16	(V, wa) ← (V, wa) + 1	Carry
INX		rp	00 $P_1P_0$0010				7	rp ← rp + 1	
		EA	10101000				7	EA ← EA + 1	
DCR		r2	010100 R_1R_0				4	r2 ← r2 − 1	Borrow
DCRW	*	wa	00110000	← Offset →			16	(V, wa) ← (V, wa) − 1	Borrow
DCX		rp	00 $P_1P_0$0011				7	rp ← rp − 1	
		EA	10101001				7	EA ← EA − 1	

Instruction Groups (Cont.)

Others

Mnemonic		Operand	OP Code B1	OP Code B2	OP Code B3	OP Code B4	State	Operation	Skip Condition
DAA			01100001				4	Decimal Adjust Accumulator	
STC			01001000	00101011			8	$CY \leftarrow 1$	
CLC			↓	00101010			8	$CY \leftarrow 0$	
CMC			01001000	10101010			8	$CY \leftarrow \overline{CY}$	
NEGA			↓	00111010			8	$A \leftarrow \overline{A} + 1$	

Rotate and Shift

RLD			01001000	00111000			17	Rotate Left Digit	
RRD			↓	1001			17	Rotate Right Digit	
RLL		r2	01001000	$001101R_1R_0$			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow CY$, $CY \leftarrow r2_7$	
RLR		r2	↓	$00R_1R_0$			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow CY$, $CY \leftarrow r2_0$	
SLL		r2	↓	$001001R_1R_0$			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	
SLR		r2	↓	$00R_1R_0$			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	
SLLC		r2	↓	$000001R_1R_0$			8	$r2_{m+1} \leftarrow r2_m$, $r2_0 \leftarrow 0$, $CY \leftarrow r2_7$	Carry
SLRC		r2	↓	$00R_1R_0$			8	$r2_{m-1} \leftarrow r2_m$, $r2_7 \leftarrow 0$, $CY \leftarrow r2_0$	Carry
DRLL		EA	↓	10110100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow CY$, $CY \leftarrow EA_{15}$	
DRLR		EA	↓	0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow CY$, $CY \leftarrow EA_0$	
DSLL		EA	↓	10100100			8	$EA_{n+1} \leftarrow EA_n$, $EA_0 \leftarrow 0$, $CY \leftarrow EA_{15}$	
DSLR		EA	↓	0000			8	$EA_{n-1} \leftarrow EA_n$, $EA_{15} \leftarrow 0$,	

Jump

JMP	*	word	01010100	← Low Adrs →	High Adrs		10	PC ← (word)	
JB			00100001				4	$PC_H \leftarrow B$, $PC_L \leftarrow C$	
JR		word	11 ← jdisp 1 →				10	PC ← PC + 1 + jdisp 1	
JRE	*	word	0100111	← jdisp →			10	PC ← PC + 2 + jdisp	
JEA			01001000	00101000			8	PC ← EA	

Call

CALL	*	word	01000000	← Low Adrs →	High Adrs		16	$(SP-1) \leftarrow (PC+3)_H$, $(SP-2) \leftarrow (PC+3)_L$, PC ← (word), SP ← SP − 2	
CALB			01001000	00101001			17	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, $PC_H \leftarrow B$, SP ← SP − 2	
CALF	*	word	01111 ←	fa →			13	$(SP-1) \leftarrow (PC+2)_H$, $(SP-2) \leftarrow (PC+2)_L$, $PC_{15-11} \leftarrow 00001$, $PC_{10-0} \leftarrow$ fa, SP ← SP − 2	
CALT		word	100 ← ta →				16	$(SP-1) \leftarrow (PC+1)_H$, $(SP-2) \leftarrow (PC+1)_L$, $PC_L \leftarrow (128 + 2ta)$, $PC_H \leftarrow (129 + 2ta)$, SP ← SP − 2	
SOFTI			01110010				16	$(SP-1) \leftarrow PSW$, $(SP-2) \leftarrow (PC+1)_H$, $(SP-3) \leftarrow (PC+1)_L$, PC ← 0060H, SP ← SP − 3	

Return

RET			10111000				10	$PC \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP + 2	
RETS			↓ 1001				10	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, SP ← SP + 2, PC ← PC + n	
RETI			01100010				13	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$, $PSW \leftarrow (SP+2)$, SP ← SP + 3	Unconditional Skip

Skip

BIT		bit, wa	$01011B_2B_1B_0$	← Offset →			10	Bit Test	(V, wa) bit = 1

4

Instruction Groups (Cont.)

CPU Control

Mnemonic	Operand	OP Code B1	OP Code B2	OP Code B3	OP Code B4	State	Operation	Skip Condition
SK	f	01001000	00001$F_2F_1F_0$			8	Skip if f = 1	f = 1
SKN	f		0001 ↓			8	Skip if f = 0	f = 0
SKIT	irf		010$I_4I_3I_2I_1I_0$			8	Skip if irf = 1, then reset irf	irf = 1
SKNIT	irf		011$I_4I_3I_2I_1I_0$			8	Skip if irf = 0 Reset irf, if irf = 1	irf = 0
NOP		00000000				4	No Operation	
EI		10101010				4	Enable Interrupt	
DI		10111010				4	Disable Interrupt	
HLT		01001000	00111011			11	Halt	

Notes: *① B2 (Data) rpa2 = D + byte, H + byte
*② B3 (Data) rpa3 = D + byte, H + byte
*③ Right side of slash (/) in states indicates case rpa2, rpa3 = D + byte, H + A, H + B, H + EA, H + byte
*④ In the case of skip condition, the idle states are as follows
1-byte instruction 4 states 2-byte instruction (with *) 7 states
2-byte instruction 8 states 3-byte instruction (with *) 10 states
3-byte instruction 11 states 4-byte instruction 14 states

Absolute Maximum Ratings*

T_a = 25°C

Power Supply Voltages, V_{CC}	−0.5V to +7.0V
V_{DD}	−0.5V to +7.0V
AV_{CC}	−0.5V to +7.0V
Input Voltage, V_I	−0.5V to +7.0V
Output Voltage, V_O	−0.5V to +7.0V
Reference Input Voltage, V_{AREF}	−0.5V to +7.0V
Operating Temperature, T_{OPT}	
10MHz < f_{XTAL} ≤ 12MHz	−10°C to +70°C
f_{XTAL} ≤ 10MHz	−40°C to 85°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

Parameter: Osc. Freq.	T_a	V_{CC}, AV_{CC}
10MHz < f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0V ± 5%
f_{XTAL} ≤ 10MHz	−40°C to 85°C	+5.0V ± 10%

Capacitance

T_a = 25°C; V_{CC} = V_{DD} = V_{SS} = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Capacitance	C_I			10	pF	Af_c = 1MHz Unmeasured pin returned to 0V.
Output Capacitance	C_O			20	pF	
I/O Capacitance	C_{IO}			20	pF	

DC Characteristics

T_a = −10°C to +70°C; V_{CC} = −5.0V ± 5%; V_{SS} = 0V; V_{CC} −0.8V ≤ V_{DD} ≤ V_{CC}

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	All except $\overline{SCK}$, $\overline{RESET}$ and X1
	V_{IH2}	0.8V_{CC}		V_{CC}	V	$\overline{SCK}$, X1
	V_{IH3}	0.8V_{DD}		V_{CC}	V	$\overline{RESET}$
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −200μA
Input Current	I_I			±200	μA	INT_1, TI (PC_3); +0.45V ≤ V_{IN} < V_{CC}
Input Leakage Current	I_{LI}			±10	μA	All except INT_1, TI (PC_3) 0V ≤ V_{IN} ≤ V_{CC}
Output Leakage Current	I_{LO}			±10	μA	+0.45V ≤ V_O ≤ V_{CC}
V_{DD} Supply Current	I_{DD}		1.5①	3.5	mA	T_a = −40°C to +85°C
V_{CC} Supply Current	I_{CC}		110①	220	mA	T_a = −40°C to +85°C

Note: ① T_a = 25°C, V_{CC} = V_{DD} = +5.0V

AC Characteristics

T_a = −10°C to 70°C; V_{CC} = +5.0V ± 5%; V_{SS} = 0V; V_{CC} − 0.8V ≤ V_{DD} ≤ V_{CC}

Read/Write Operation

Parameter	Symbol	Limits f_{XTAL} = 10MHz Min	Limits f_{XTAL} = 10MHz Max	Limits f_{XTAL} = 12 MHz Min	Limits f_{XTAL} = 12 MHz Max	Unit	Test Conditions
X_1 Input Cycle Time	t_{CYC}	100		83		ns	
Address Setup to ALE ↓	t_{AL}	100		65		ns	
Address Hold after ALE ↓	t_{LA}	70		50		ns	
Address to $\overline{RD}$ ↓ Delay Time	t_{AR}	200		150		ns	
$\overline{RD}$ ↓ to Address Floating	t_{AFR}		20		20	ns	
Address to Data Input	t_{AD}		480		360	ns	
ALE ↓ to Data Input	t_{LDR}		300		215	ns	
$\overline{RD}$ ↓ to Data Input	t_{RD}		250		180	ns	
ALE ↓ to $\overline{RD}$ ↓ Delay Time	t_{LR}	50		35		ns	
Data Hold Time to $\overline{RD}$ ↑	t_{RDH}	0		0		ns	
$\overline{RD}$ ↑ to ALE ↑ Delay Time	t_{RL}	150		115		ns	
$\overline{RD}$ Width Low	t_{RR}	350		280		ns	Data Read
		650		530		ns	OP Code Fetch
ALE Width High	t_{LL}	160		125		ns	
Address to $\overline{WR}$ ↓ Delay	t_{AW}	200		150		ns	
ALE ↓ to Data Output	t_{LDW}		210		195	ns	
$\overline{WR}$ ↓ to Data Output	t_{WD}	130		100		ns	
ALE ↓ to $\overline{WR}$ ↓ Delay	t_{LW}	50		35		ns	
Data Setup Time to $\overline{WR}$ ↑	t_{DW}	300		230		ns	
Data Hold Time to $\overline{WR}$ ↑	t_{WDH}	130		95		ns	
$\overline{WR}$ ↑ to ALE ↑ Delay Time	t_{WL}	150		115		ns	
$\overline{WR}$ Width Low	t_{WW}	350		280		ns	

Note: ① Load capacitance C_L = 150pF

Serial Operation

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
$\overline{SCK}$ Cycle Time	t_{CYK}	1			μs	$\overline{SCK}$ Input	②
		500			ns		③
		2			μs	$\overline{SCK}$ Output	
$\overline{SCK}$ Width Low	t_{KKL}	400			ns	$\overline{SCK}$ Input	②
		200			ns		③
		900			ns	$\overline{SCK}$ Output	
$\overline{SCK}$ Width High	t_{KKH}	400			ns	$\overline{SCK}$ Input	②
		200			ns		③
		900			ns	$\overline{SCK}$ Output	
RxD Setup Time to $\overline{SCK}$ ↑	t_{RXK}	80			ns		②
RxD Hold Time After $\overline{SCK}$ ↑	t_{KRX}	80			ns		②
$\overline{SCK}$ ↓ TxD Delay Time	t_{KTX}			210	ns		②

Notes: ② 1x Baud rate in Asynchronous, Synchronous, or I/O Interface mode
③ 16x Baud rate or 64x Baud rate in Asynchronous mode

AC Characteristics (Cont.)

T_a = −10°C to +70°C; V_{CC} = +5.0V ± 5%; V_{SS} = 0V; V_{CC} − 0.8V ≤ V_{DD} ≤ V_{CC}

Zero-cross Characteristics

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Zero-cross Detection Input	V_{ZX}	1		3	VAC_{P-P}	AC Coupled
Zero-cross Accuracy	A_{ZX}			±135	mV	60Hz Sine Wave
Zero-cross Detection Input Frequency	f_{ZX}	0.05		1	kHz	

T_a = −10°C to +70°C; V_{CC} = AV_{CC} = +5.0V ± 5%; V_{SS} = AV_{SS} = 0V; AV_{CC} − 0.5V ≤ V_{AREF} ≤ AV_{CC}

A/D Converter Characteristics

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Resolution		8			Bits	
Absolute Accuracy				0.4% ± ½	LSB	T_a = −10°C to +50°C
				0.6% ± ½	LSB	T_a = −10°C to +70°C④
Conversion Time	t_{CONV}	576			t_{CYC}	83ns ≤ t_{CYC} ≤ 110ns
		432			t_{CYC}	110ns ≤ t_{CYC} ≤ 170ns
Sampling Time	t_{SAMP}	96			t_{CYC}	83ns ≤ t_{CYC} ≤ 110ns
		72			t_{CYC}	110ns ≤ t_{CYC} ≤ 170ns
Analog Input Voltage	V_{IA}	0		V_{AREF}	V	

Note: ④ In case of f_{XTAL} ≤ 10MHz, T_a = −40°C to +85°C.

Bus Timing Depending on t_{CYC}

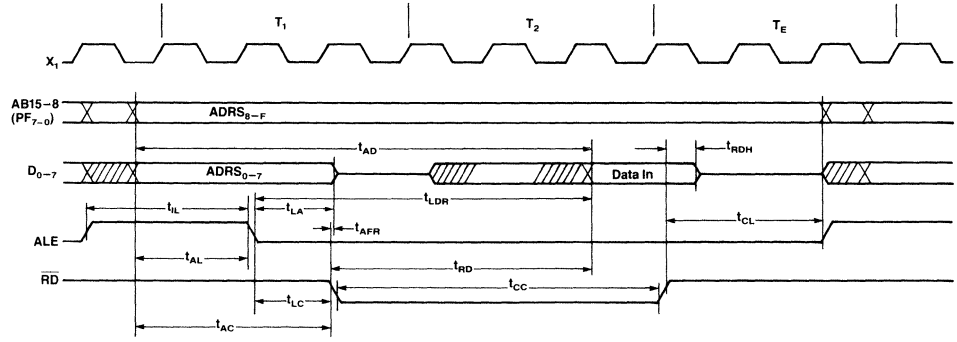
Symbol	Calculating Expression	Min/Max	Unit
t_{AL}	2T − 100	Min	ns
t_{LA}	T − 30	Min	ns
t_{AR}	3T − 100	Min	ns
t_{AD}	7T − 220	Max	ns
t_{LDR}	5T − 200	Max	ns
t_{RD}	4T − 150	Max	ns
t_{LR}	T − 50	Min	ns
t_{RL}	2T − 50	Min	ns
t_{RR}	4T − 50 (Data Read)	Min	ns
	7T − 50 (OP Code Fetch)		
t_{LL}	2T − 40	Min	ns
t_{AW}	3T − 100	Min	ns
t_{LDW}	T + 110	Max	ns
t_{LW}	T − 50	Min	ns
t_{DW}	4T − 100	Min	ns
t_{WDH}	2T − 70	Min	ns
t_{WL}	2T − 50	Min	ns
t_{WW}	4T − 50	Min	ns
t_{CYK}	12T ($\overline{SCK}$ Input) ①	Min	ns
	24T ($\overline{SCK}$ Output)		
t_{KKL}	6T − 100 ($\overline{SCK}$ Input) ①	Min	ns
	12T − 100 ($\overline{SCK}$ Output)		
t_{KKH}	6T − 100 ($\overline{SCK}$ Input) ①	Min	ns
	12T − 100 ($\overline{SCK}$ Output)		

Notes: ① 1x Baud rate in Asynchronous, Synchronous, or I/O Interface mode
T = t_{CYC} = $1/f_{XTAL}$
The items out of this list are not dependent on oscillating frequency (f_{XTAL})

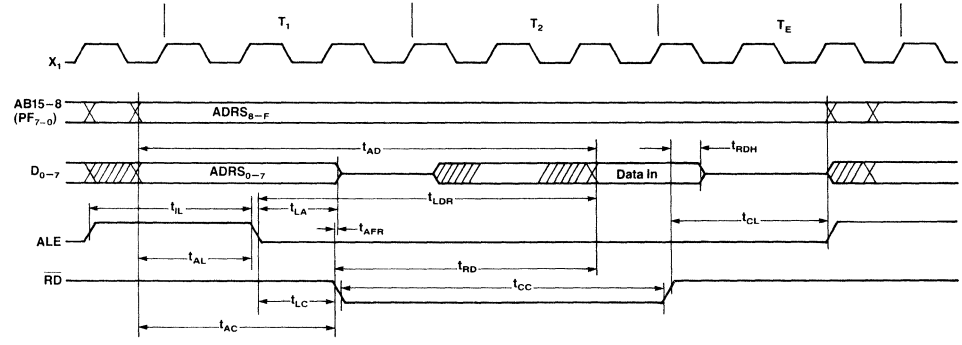
4

Timing Waveforms

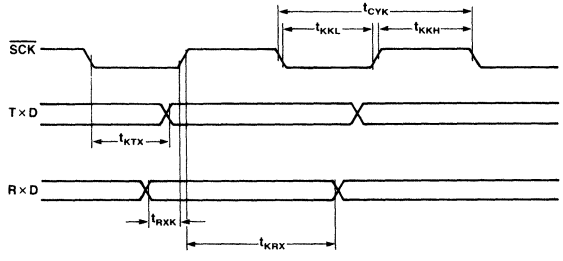
Read Operation



Write Operation



Transmit/Receive Timing



Package Outlines

For information, see Package Outline Section 7.

Plastic Quil, μPD7810G/11G
Plastic Shrinkdip, μPD7810CW/11CW
QUIL Ceramic Piggyback, μPD78PG11E

SINGLE CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

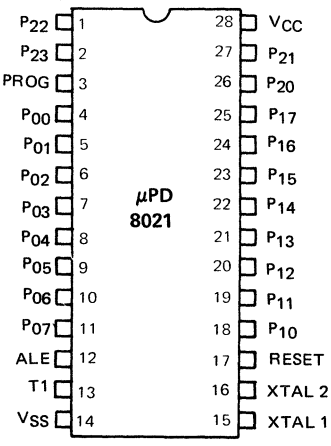
The NEC μPD8021 is a stand alone 8-bit parallel microcomputer incorporating the following features usually found in external peripherals. The μPD8021 contains: 1K x 8 bits of mask ROM program memory, 64 x 8 bits of RAM data memory, 21 I/O lines, an 8-bit interval timer/event counter, and internal clock circuitry.

FEATURES

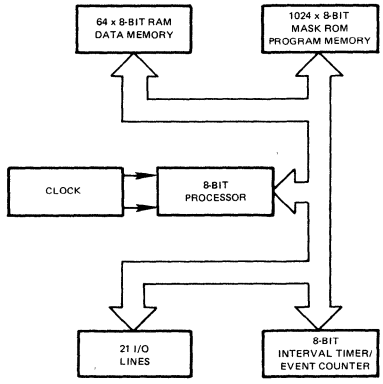
- 8-Bit Processor, ROM, RAM, I/O, Timer/Counter
- Single +5V Supply (+4.5V to +6.5V)
- NMOS Silicon Gate Technology
- 8.38 μs Instruction Cycle Time
- All Instructions 1 or 2 Cycles
- Instructions are Subset of μPD8048/8748/8035
- High Current Drive Capability – 2 I/O Pins
- Clock Generation Using Crystal or Single Inductor
- Zero-Cross Detection Capability
- Expandable I/O Using μ8243's
- Available in 28-Pin Plastic Package

4

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . -65°C to +150°C
(Plastic Package) . . . . . -65°C to +150°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①
Power Dissipation . . . . . 1 Watt

Note: ① With Respect to Ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5.5V \pm 1V$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		+ 0.8	V	
Input High Voltage, RESET, T1 (All Except XTAL 1, XTAL 2)	V_{IH}	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	$V_{CC} = 5.5V \pm 1V$
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 1.7$ mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			2.5	V	$I_{OL} = 7$ mA
Output High Voltage (All Unless Open Drain)	V_{OH}	2.4			V	$I_{OH} = 40\ \mu A$
Output Leakage Current (Open Drain Option – Port 0)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
V_{CC} Supply Current	I_{CC}		40	75	mA	

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Cycle Time	T_{CY}	8.38		50.0	μs	3.58 MHz XTAL for T_{CY} Min.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1-2, 26-27	P_{20}-P_{23} (Port 2)	P_{20}-P_{23} comprise the 4-bit bi-directional I/O port which is also used as the expander bus for the μPD8243.
3	PROG	PROG is the output strobe pin for the μPD8243.
4-11	P_{00}-P_{07} (Port 0)	One of the two 8-bit quasi bi-directional I/O ports.
12	ALE	Address Latch Enable output (active-high). Occurring once every 30 input clock periods, ALE can be used as an output clock.
13	T1	Testable input using transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction. T1 also provides zero-cross sensing for low-frequency AC input signals.
14	V_{SS}	Processor's ground potential.
15	XTAL 1	One side of frequency source input using resistor, inductor, crystal or external source.(non-TTL compatible V_{IH}).
16	XTAL 2	The other side of frequency source input.
17	RESET	Active high input that initializes the processor and starts the program at location zero.
18-25	P_{10}-P_{17} (Port 1)	The second of two 8-bit quasi bi-directional I/O ports.
28	V_{CC}	+5V power supply input.

4

FUNCTIONAL DESCRIPTION

The NEC μPD8021 is a single component, 8-bit, parallel microprocessor using N-channel silicon gate MOS technology. The self-contained 1K x 8-bit ROM, 64 x 8-bit RAM, 8-bit timer/counter, and clock circuitry allow the μPD8021 to operate as a single-chip microcomputer in applications ranging from controllers to arithmetic processors.

The instruction set, a subset of the μPD8048/8748/8035, is optimum for high-volume, low cost applications where I/O flexibility and instruction set power are required. The μPD8021 instruction set is comprised mostly of single-byte instructions with no instructions over two bytes.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
DATA MOVES													
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
MOV A, Rr	(A) ← (Rr), r = 0 - 7	Move the contents of the designated registers into the Accumulator	1	1	1	1	1	r	r	r	1	1	
MOV A, @ Rr	(A) ← ((Rr)), r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1	
MOV Rr, = data	(Rr) ← data, r = 0 - 7	Move Immediate the specified data into the designated register	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2	
MOV Rr, A	(Rr) ← (A), r = 0 - 7	Move Accumulator Contents into the designated register	1	0	1	0	1	r	r	r	1	1	
MOV @ Rr, A	((Rr)) ← (A), r = 0 - 1	Move Indirect Accumulator Contents into data memory location	1	0	1	0	0	0	0	r	1	1	
MOV @ Rr, = data	((Rr)) ← data, r = 0 - 1	Move Immediate the specified data into data memory	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2	
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator	1	0	1	0	0	0	1	1	2	1	
XCH A, Rr	(A) ⇄ (Rr), r = 0 - 7	Exchange the Accumulator and designated register's contents	0	0	1	0	1	r	r	r	1	1	
XCH A, @ Rr	(A) ⇄ ((Rr)), r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory	0	0	1	0	0	0	0	r	1	1	
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)), r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory	0	0	1	1	0	0	0	r	1	1	
FLAGS													
CPL C	(C) ← NOT (C)	Complement Content of carry bit	1	0	1	0	0	1	1	1	1	1	•
CLR C	(C) ← 0	Clear content of carry bit to 0	1	0	0	1	0	1	1	1	1	1	•
INPUT/OUTPUT													
ANLD Pp, A	(P_p) ← (P_p) AND (A 0 - 3) p = 4 - 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1	
IN A, P_p	(A) ← (P_p), p = 1 - 2	Input data from designated port (1 - 2) into Accumulator	0	0	0	0	1	0	p	p	2	1	
MOVD A, P_p	(A 0 - 3) ← (P_p), p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator	0	0	0	0	1	1	p	p	2	1	
MOVD P_p, A	(P_p) ← A 0 - 3, p = 4 - 7	Move contents of Accumulator to designated port (4 - 7)	0	0	1	1	1	1	p	p	1	1	
ORLD P_p, A	(P_p) ← (P_p) OR (A 0 - 3) p = 4 - 7	Logical or contents of Accumulator with designated port (4 - 7)	1	0	0	0	1	1	p	p	1	1	
OUTL P_p, A	(P_p) ← (A), p = 1 - 2	Output contents of Accumulator to designated port (1 - 2)	0	0	1	1	1	0	p	p	1	1	
REGISTERS													
INC Rr	(Rr) ← (Rr) + 1, r = 0 - 7	Increment by 1 contents of designated register	0	0	0	1	1	r	r	r	1	1	
INC @ Rr	((Rr)) ← ((Rr)) + 1, r = 0 - 1	Increment Indirect by 1 the contents of data memory location	0	0	0	1	0	0	0	r	1	1	
SUBROUTINE													
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word	1	0	0	0	0	0	1	1	2	1	
TIMER/COUNTER													
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator	0	1	0	0	0	0	1	0	1	1	
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter	0	1	1	0	0	0	1	0	1	1	
STOP TCNT		Stop Count for Event Counter	0	1	1	0	0	1	0	1	1	1	
STRT CNT		Start Count for Event Counter	0	1	0	0	0	1	0	1	1	1	
STRT T		Start Count for Timer	0	1	0	1	0	1	0	1	1	1	
MISCELLANEOUS													
NOP		No Operation performed	0	0	0	0	0	0	0	0	1	1	

Notes ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions

SYMBOL	DESCRIPTION
A	The Accumulator
addr	Program Memory Address (12 bits)
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 - 7)
Rr	Register Designator (r = 0, 1 or 0 - 7)

SYMBOL	DESCRIPTION
T	Timer
T_1	Testable Flag 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
ACCUMULATOR													
ADD A, = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator	0	1	1	0	1	r	r	r	1	1	•
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents the data memory location to the Accumulator	0	1	1	0	0	0	0	r	1	1	•
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator	0	1	1	1	1	r	r	r	1	1	•
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator	0	1	1	1	0	0	0	r	1	1	•
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical and contents of designated register with Accumulator	0	1	0	1	1	r	r	r	1	1	
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical and Indirect the contents of data memory with Accumulator	0	1	0	1	0	0	0	r	1	1	
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator	0	0	1	1	0	1	1	1	1	1	
CLR A	(A) ← 0	CLEAR the contents of the Accumulator	0	0	1	0	0	1	1	1	1	1	
DA A		DECIMAL ADJUST the contents of the Accumulator	0	1	0	1	0	1	1	1	1	1	•
DEC A	(A) ← (A) - 1	DECREMENT by 1 the Accumulator's contents	0	0	0	0	0	1	1	1	1	1	
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents	0	0	0	1	0	1	1	1	1	1	
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator	0	1	0	0	1	r	r	r	1	1	
ORL A @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR Indirect the contents of data memory location with Accumulator	0	1	0	0	0	0	0	r	1	1	
RL A	(AN + 1)← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1-bit without carry	1	1	1	0	0	1	1	1	1	1	
RLC A	(AN + 1) ← (AN), N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry	1	1	1	1	0	1	1	1	1	1	•
RR A	(AN) ← (AN + 1), N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry	0	1	1	1	0	1	1	1	1	1	
RRC A	(AN) ← (AN + 1), N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•
SWAP A	(A_{4-7}) ⇄ (A_0 - 3)	Swap the 24-bit nibbles in the Accumulator	0	1	0	0	0	1	1	1	1	1	
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator	1	1	0	1	1	r	r	r	1	1	
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR Indirect the contents of data memory location with Accumulator	1	1	0	1	0	0	0	r	1	1	
BRANCH													
DJNZ Rr, addr	(Rr) ← (Rr) - 1, r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2	
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JMP addr	(PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
JMPP @ A	(PC 0 - 7) ← ((A))	Jump indirect to specified address with address page	1	0	1	1	0	0	1	1	2	1	
JNC addr	(PC 0 - 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JNZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2	

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8021C
Cerdip, μPD8021D

UNIVERSAL PROGRAMMABLE PERIPHERAL INTERFACE — 8-BIT MICROCOMPUTER

DESCRIPTION

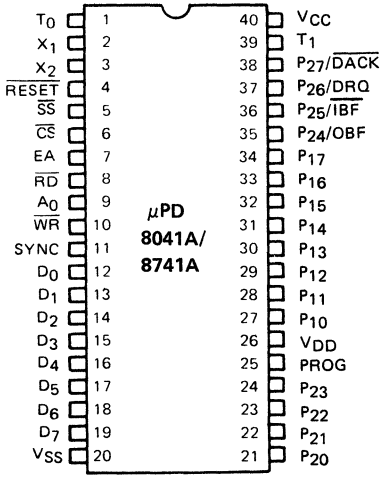
The μPD8041A/8741A is a programmable peripheral interface intended for use in a wide range of microprocessor systems. Functioning as a totally self-sufficient controller, the μPD8041A/8741A contains an 8-bit CPU, 1K x 8 program memory, 64 x 8 data memory, I/O lines, counter/timer, and clock generator in a 40-pin DIP. The bus structure, data registers, and status register enable easy interface to 8048, 8080A or 8085A based systems. The μPD8041A's program memory is factory mask programmed, while the μPD8741A's program memory is UV EPROM to enable user flexibility.

FEATURES

- Fully Compatible with 8048, 8080A, 8085A and 8086 Bus Structure
- 8-Bit CPU with 1K x 8 ROM, 64 x 8 RAM, 8-Bit Timer/Counter, 18 I/O Lines
- 8-Bit Status and Two Data Registers for Asynchronous Slave-to-Master Interface
- Interchangeable EPROM and ROM Versions
- Interrupt, DMA or Polled Operation
- Expandable I/O
- 40-Pin Plastic or Cerdip DIP Package
- Single +5V Supply

4

PIN CONFIGURATION



PIN IDENTIFICATION

PIN NO	PIN SYMBOL	FUNCTION
1,39	T_0 T_1	Testable input pins using conditional transfer instructions JT0, JNT0, JT1, JNT1. T_1 can be made the counter/timer input using the STRT CNT instruction. The PROM programming and verification on the μPD8741A uses T_0.
2	X_1	One side of the crystal input for external oscillator or frequency source.
3	X_2	The other side of the crystal input.
4	$\overline{RESET}$	Active-low input for processor initialization. $\overline{RESET}$ is also used for PROM programming, verification, and power down.
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with SYNC output allows the μPD8741A to "single-step" through each instruction in program memory.
6	$\overline{CS}$	Chip Select input (active-low). $\overline{CS}$ is used to select the appropriate μPD8041A/8741A on a common data bus.
7	EA	External Access input (active-high). A logic "1" at this input commands the μPD8041A/8741A to perform all program memory fetches from external memory.
8	$\overline{RD}$	Read strobe input (active-low). $\overline{RD}$ will pulse low when the master processor reads data and status words from the DATA BUS BUFFER or Status Register.
9	A_0	Address input which the master processor uses to indicate if a byte transfer is a command or data.
10	$\overline{WR}$	Write strobe input (active-low). $\overline{WR}$ will pulse low when the master processor writes data or status words to the DATA BUS BUFFER or Status Register.
11	SYNC	The SYNC output pulses once for each μPD8041A/8741A instruction cycle. It can function as a strobe for external circuitry. SYNC can also be used together with $\overline{SS}$ to "single-step" through each instruction in program memory.
12-19	D_0-D_7 BUS	The 8-bit, bi-directional, tri-state DATA BUS BUFFER lines by which the μPD8041A/8741A interfaces to the 8-bit master system data bus.
20	V_{SS}	Processor's ground potential.
21-24, 35-38	P_{20}-P_{27}	PORT 2 is the second of two 8-bit, quasi-bi-directional I/O ports. P_{20}-P_{23} contain the four most significant bits of the program counter during external memory fetches. P_{20}-P_{23} also serve as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER. P_{24}-P_{27} can be used as port lines or can provide Interrupt Request (IBF and OBF) and DMA handshake lines (DRQ and $\overline{DACK}$).
25	PROG	Program Pulse. PROG is used in programming the μPD8741A. It is also used as an output strobe for the μPD8243.
26	V_{DD}	V_{DD} is the programming supply voltage for programming the μPD8741A. It is +5V for normal operation of the μPD8041A/8741A. V_{DD} is also the Low Power Standby input for the ROM version.
27-34	P_{10}-P_{17}	PORT 1 is the first of two 8-bit quasi-bi-directional I/O ports.
40	V_{CC}	Primary power supply. V_{CC} must be +5V for programming and operation of the μPD8741A and for the operation of the μPD8041A.

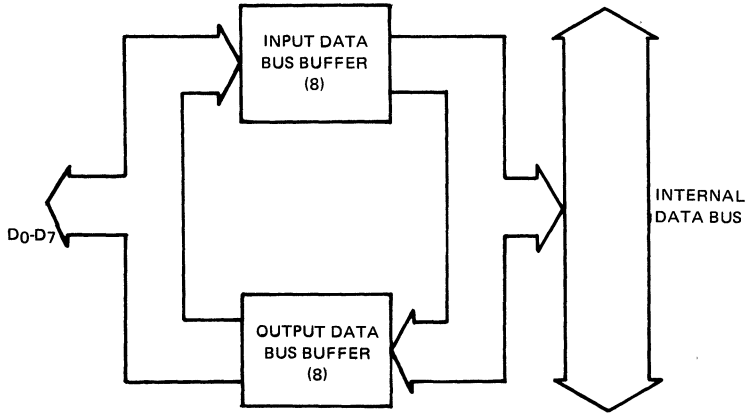
FUNCTIONAL DESCRIPTION

The μPD8041A/8741A is a programmable peripheral controller intended for use in master/slave configurations with 8048, 8080A, 8085A, 8086 – as well as most other 8-bit and 16-bit microprocessors. The μPD8041A/8741A functions as a totally self-sufficient controller with its own program and data memory to effectively unburden the master CPU from I/O handling and peripheral control functions. The μPD8041A/8741A is an intelligent peripheral device which connects directly to the master processor bus to perform control tasks which off load main system processing and more efficiently distribute processing functions.

μPD8041A/8741A FUNCTIONAL ENHANCEMENTS

The μPD8041A/8741A features several functional enhancements to the earlier μPD8041 part. These enhancements enable easier master/slave interface and increased functionality.

1. Two Data Bus Buffers. Separate Input and Output data bus buffers have been provided to enable smoother data flow to and from master processors.

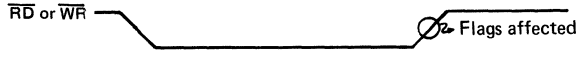


2. 8-Bit Status Register. Four user-definable status bits, ST_4-ST_7, have been added to the status register. ST_4-ST_7 bits are defined with the MOV STS, A instruction which moves accumulator bits 4-7 to bits 4-7 of the status register. ST_0-ST_3 bits are not affected.

ST_7	ST_6	ST_5	ST_4	F_1	F_0	IBF	OBF
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MOV STS, A Instruction OP Code 90H

3. $\overline{RD}$ and $\overline{WR}$ inputs are edge-sensitive. Status bits IBF, OBF, F1 and F0 are affected on the trailing edge at $\overline{RD}$ or $\overline{WR}$.



μPD8041A/8741A
FUNCTIONAL
ENHANCEMENTS (CONT.)

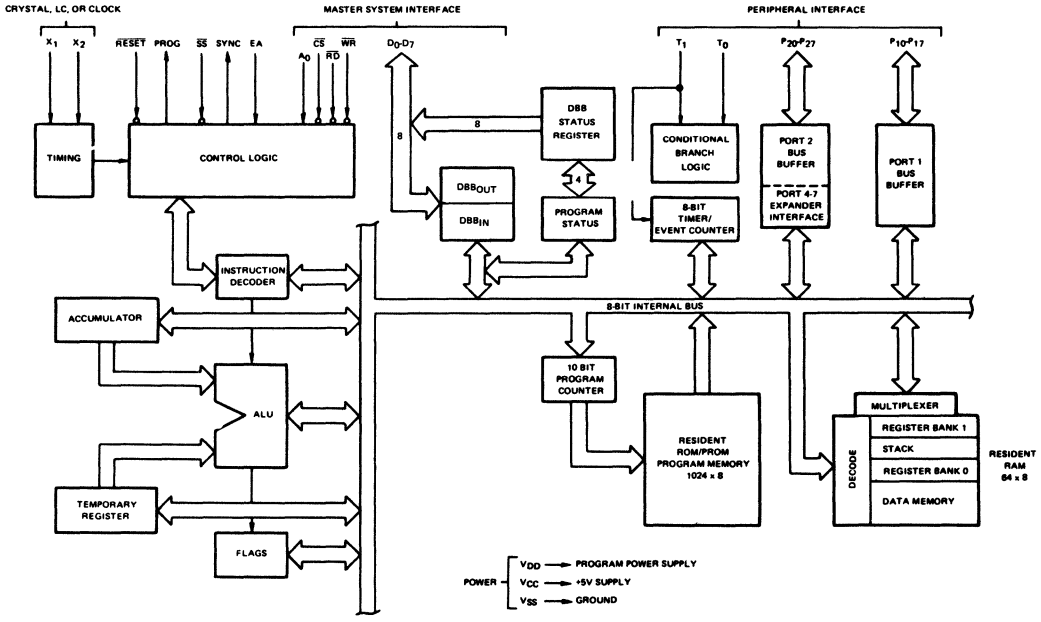
4. P_{24} and P_{25} can be used as either port lines or Buffer Status Flag pins. This feature allows the user to make OBF and IBF status available externally to interrupt the master processor. Upon execution of the EN Flags instruction, P_{24} becomes the OBF pin. When a "1" is written to P_{24}, the OBF pin is enabled and the status of OBF is output. A "0" written to P_{24} disables the OBF pin and the pin remains low. This pin indicates valid data is available from the μPD8041A/8741A. EN Flags instruction execution also enables P_{25} indicate that the μPD8041A/8741A is ready to accept data. A "1" written to P_{25} enables the IBF pin and the status of IBF is available on P25. A "0" written to P_{25} disables the IBF pin. If OBF is not true, the data at the databus is invalid.

   EN Flags Instruction Op code – F5H.

5. P_{26} and P_{27} can be used as either port lines or DMA handshake lines to allow DMA interface. The EN DMA instruction enables P_{26} and P_{27} to be used as DRQ (DMA Request) and $\overline{DACK}$ (DMA acknowledge) respectively. When a "1" is written to P_{26}, DRQ is activated and a DMA request is issued. Deactivation of DRQ is accomplished by the execution of the EN DMA instruction, $\overline{DACK}$ anded with $\overline{RD}$, or $\overline{DACK}$ anded with $\overline{WR}$. When EN DMA has been executed, P_{27} ($\overline{DACK}$) functions as a chip select input for the Data Bus Buffer registers during DMA transfers.

   EN DMA Instruction Op Code – E5H.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . −65°C to +150°C
Storage Temperature (Plastic Package) . . . . . −65°C to +150°C
Voltage on Any Pin . . . . . −0.5 to +7 Volts ①
Power Dissipation . . . . . 1.5 Watt

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note ① With respect to ground

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All except X_1 and X_2)	V_{IL}	−0.5		+0.8	V	
Input Low Voltage (X_1 and X_2, $\overline{RESET}$)	V_{IL1}	−0.5		0.6	V	
Input High Voltage (All except X_1, X_2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (X_1, X_2, $\overline{RESET}$)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (D_0-D_7, SYNC)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All other outputs except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.0 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 1.0 mA
Output High Voltage (D_0-D_7)	V_{OH}	2.4			V	I_{OH} = −400 μA
Output High Voltage (All other outputs)	V_{OH1}	2.4			V	I_{OH} = −50 μA
Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (D_0-D_7; High Z State)	I_{OL}			±10	μA	V_{SS} + 0.45 ≤ $V_{IN} \leq V_{CC}$
V_{DD} Supply Current	I_{DD}			15	mA	
Total Supply Current	$I_{CC} + I_{DD}$			125	mA	
Low Input Source Current (P_{10}-P_{17}; P_{20}-P_{27})	I_{LI}			0.5	mA	V_{IL} = 0.8V
Low Input Source Current (SS; $\overline{RESET}$)	I_{LI1}			0.2	mA	V_{IL} = 0.8V

4

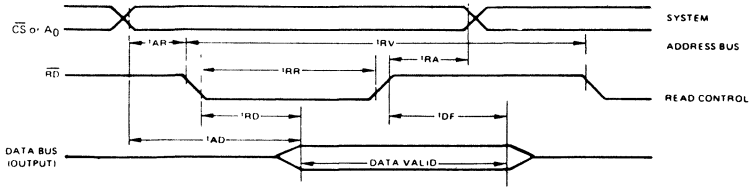
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{DD} = V_{CC} = +5V ± 10%; V_{SS} = 0V

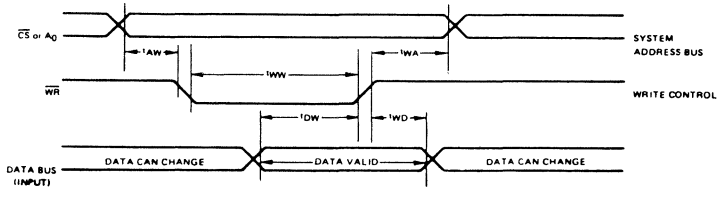
PARAMETER	SYMBOL	LIMITS μPD8041A MIN	LIMITS μPD8041A MAX	LIMITS μPD8741A MIN	LIMITS μPD8741A MAX	UNITS	TEST CONDITIONS
DBB READ							
$\overline{CS}$, A_0 Setup to $\overline{RD}$ ↓	t_{AR}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{RD}$ ↑	t_{RA}	0		30		ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		225		370	ns	C_L = 150 pF
$\overline{RD}$ ↓ to Data Out Delay	t_{RD}		225		200	ns	C_L = 150 pF
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}		100		140	ns	
Cycle Time	t_{CY}	2.5	15	2.5	15	μs	6 MHz Crystal
DBB WRITE							
$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	t_{AW}	10		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{WR}$ ↑	t_{WA}	10		30		ns	
$\overline{WR}$ Pulse Width	t_{WW}	260		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
Data Setup to $\overline{WR}$ ↑	t_{DW}	150		250		ns	
Data Hold after $\overline{WR}$ ↑	t_{WD}	10		30		ns	
PORT 2							
Port Control Setup before falling edge of $\overline{PROG}$	t_{CP}	110		110		ns	
Port Control Hold after Falling Edge of $\overline{PROG}$	t_{PC}	100		100		ns	
$\overline{PROG}$ to P_2 Input Valid	t_{PR}		810		810	ns	
Input Data Hold Time	t_{PF}	0	150	0	150	ns	
Output Data Setup Time	t_{DP}	250		250		ns	
Output Data Hold Time	t_{PD}	65		65		ns	
$\overline{PROG}$ Pulse Width		1200		1200		ns	
DMA							
$\overline{DACK}$ ↓ to $\overline{RD}$ ↓ or $\overline{WR}$ ↓	t_{ACC}	0		0		ns	
$\overline{RD}$ ↑ or $\overline{WR}$ to $\overline{DACK}$ ↑	t_{CAC}	0		0		ns	
$\overline{DACK}$ to Data Valid	t_{ACD}		225		225	ns	C_L 150pF
$\overline{RD}$ or $\overline{WR}$ to DRQ ↓	t_{CRQ}		225		225	ns	

TIMING WAVEFORMS

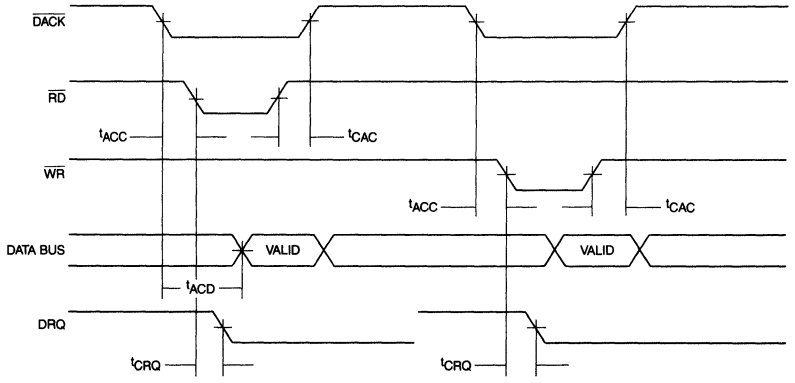
READ OPERATION – DATA BUS BUFFER REGISTER



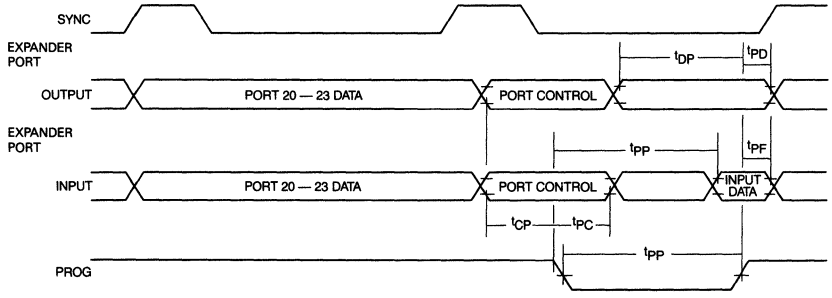
WRITE OPERATION – DATA BUS BUFFER REGISTER



DMA TIMING DIAGRAM



PORT 2 TIMING DIAGRAM



MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST_{4-7}
ACCUMULATOR																			
ADD A, #data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator	0	0	0	0	0	0	1	1	2	2	•						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator	0	1	1	0	1	r	r	r	1	1	•						
ADD A, @Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add Indirect the contents the data memory location to the Accumulator	0	1	1	0	0	0	0	r	1	1	•						
ADDC A, #data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator	0	0	0	1	0	0	1	1	2	2	•						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator	0	1	1	1	1	r	r	r	1	1	•						
ADDC A, @Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add Indirect with carry the contents of data memory location to the Accumulator	0	1	1	1	0	0	0	r	1	1	•						
ANL A, #data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator	0	1	0	1	0	0	1	1	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical and contents of designated register with Accumulator	0	1	0	1	1	r	r	r	1	1							
ANL A, @Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical and Indirect the contents of data memory with Accumulator	0	1	0	1	0	0	0	r	1	1							
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator	0	0	1	1	0	1	1	1	1	1							
CLR A	(A) ← 0	CLEAR the contents of the Accumulator	0	0	1	0	0	1	1	1	1	1							
DA A		DECIMAL ADJUST the contents of the Accumulator	0	1	0	1	0	1	1	1	1	1	•						
DEC A	(A) ← (A) - 1	DECREMENT by 1 the accumulator's contents	0	0	0	0	0	1	1	1	1	1							
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents	0	0	0	1	0	1	1	1	1	1							
ORL A, #data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0	1	0	0	0	0	1	1	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator	0	1	0	0	1	r	r	r	1	1							
ORL A, @Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR Indirect the contents of data memory location with Accumulator	0	1	0	0	0	0	0	r	1	1							
RL A	$(A_{N+1}) \leftarrow (A_N)$ $(A_0) \leftarrow (A_7)$ for N = 0 - 6	Rotate Accumulator left by 1 bit without carry	1	1	1	0	0	1	1	1	1	1							
RLC A	$(A_{N+1}) \leftarrow (A_N)$, N = 0 - 6 $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$	Rotate Accumulator left by 1 bit through carry	1	1	1	1	0	1	1	1	1	1	•						
RR A	$(A_N) \leftarrow (A_{N+1})$, N = 0 - 6 $(A_7) \leftarrow (A_0)$	Rotate Accumulator right by 1 bit without carry	0	1	1	1	0	1	1	1	1	1							
RRC A	$(A_N) \leftarrow (A_{N+1})$, N = 0 - 6 $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$	Rotate Accumulator right by 1 bit through carry	0	1	1	0	0	1	1	1	1	1	•						
SWAP A	$(A_{4-7}) \leftarrow (A_{0-3})$	Swap the 2 4 bit nibbles in the Accumulator	0	1	0	0	0	1	1	1	1	1							
XRL A, #data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator	1	1	0	1	0	0	1	1	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator	1	1	0	1	1	r	r	r	1	1							
XRL A, @Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR Indirect the contents of data memory location with Accumulator	1	1	0	1	0	0	0	r	1	1							
BRANCH																			
DJNZ Rr, addr	(Rr) ← (Rr) - 1, r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents	1	1	1	0	1	r	r	r	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JBb addr	(PC 0 - 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set	b_2	b_1	b_0	1	0	0	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set	1	1	1	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JF0 addr	(PC 0 - 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set	1	0	1	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JF1 addr	(PC 0 - 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set	0	1	1	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JMP addr	(PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block	a_{10}	a_9	a_8	0	0	1	0	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JMPP @A	(PC 0 - 7) ← ((A))	Jump indirect to specified address with with address page	1	0	1	1	0	0	1	1	2	1							
JNC addr	(PC 0 - 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low	1	1	1	0	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JNIBF addr	(PC 0 - 7) ← addr if IBF = 0 (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if input buffer full flag is low	1	1	0	1	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
JOBF	(PC 0 - 7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	Jump to specified address if output buffer full flag is set	1	0	0	0	0	1	1	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									

INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION		INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST_{4-7}
BRANCH (CONT.)																			
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T 1 = 1	Jump to specified address if Test 1 is low	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non zero	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
CONTROL																			
EN I		Enable the External Interrupt input	0	0	0	0	0	1	0	1	1	1							
DIS I		Disable the External Interrupt input	0	0	0	1	0	1	0	1	1	1							
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory	1	1	0	0	0	1	0	1	1	1							
SEL RB1	(BS) ← 1	Select Bank 0 (locations 24 – 31) of Data Memory	1	1	0	1	0	1	0	1	1	1							
EN DMA		Enable DMA Handshake	1	1	1	1	0	1	0	1	1	1							
EN FLAGS		Enable Interrupt to Master Device	1	1	1	0	0	1	0	1	1	1							
DATA MOVES																			
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
MOV A, Rr	(A) ← (Rr), r = 0 7	Move the contents of the designated registers into the Accumulator	1	1	1	1	1	r	r	r	1	1							
MOV A, @ Rr	(A) ← ((Rr)) r = 0 1	Move Indirect the contents of data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1							
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator	1	1	0	0	0	1	1	1	1	1							
MOV Rr, # data	(Rr) ← data, r = 0 7	Move Immediate the specified data into the designated register	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2							
MOV Rr A	(Rr) ← (A), r = 0 7	Move Accumulator Contents into the designated register	1	0	1	0	1	r	r	r	1	1							
MOV @ Rr, A	((Rr)) ← (A), r = 0 1	Move Indirect Accumulator Contents into data memory location	1	0	1	0	0	0	0	r	1	1							
MOV @ Rr, # data	((Rr)) ← data r = 0 1	Move Immediate the specified data into data memory	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2							
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word	1	1	0	1	0	1	1	1	1	1							
MOVP A, @ A	(PC 0 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator	1	0	1	0	0	0	1	1	2	1							
MOVP3 A @ A	(PC 0 7) ← (A) (PC 8 - 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator	1	1	1	0	0	0	1	1	2	1							
XCH A, Rr	(A) ⇄ (Rr), r = 0 – 7	Exchange the Accumulator and designated register's contents	0	0	1	0	1	r	r	r	1	1							
XCH A, @ Rr	(A) ⇄ ((Rr)), r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory	0	0	1	0	0	0	0	r	1	1							
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)), r = 0 – 1	Exchange Indirect 4 bit contents of Accumulator and data memory	0	0	1	1	0	0	0	r	1	1							
FLAGS																			
CPL C	(C) ← NOT (C)	Complement Content of carry bit	1	0	1	0	0	1	1	1	1	1	•						
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0	1	0	0	1	0	1	0	1	1	1			•				
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•			
CLR C	(C) ← 0	Clear content of carry bit to 0	1	0	0	1	0	1	1	1	1	1	•						
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•				
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0	1	0	1	0	0	1	0	1	1	1				•			
MOV STS, A	ST_4-ST_7 ← A4-A7	Move high order 4 bits of Accumulator into status register bits 4-7	1	0	0	1	0	0	0	0	1	1							•

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INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF	ST4-7
INPUT/OUTPUT																			
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 3) p = 4 7	**Logical and contents of Accumulator with designated port (4 – 7).**	1	0	0	1	1	1	p	p	2	1							
IN A, Pp	(A) ← (Pp), p = 1 2	Input data from designated port (1 or 2) into Accumulator	0	0	0	0	1	0	p	p	2	1							
IN A, DBB	(A) ← (DBB)	Input strobed DBB data into Accumulator and clear IBF	0	0	1	0	0	0	1	0	1	1							
MOVD A, Pp	(A 0 – 3) ← (Pp) p = 4 – 7 (A 4 7) ← 0	Move contents of designated port (4 – 7) into Accumulator	0	0	0	0	1	1	p	p	2	1							
MOVD Pp, A	(Pp) ← A 0 3 p = 4 7	Move contents of Accumulator to designated port (4 – 7)	0	0	1	1	1	1	p	p	1	1							
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 3) p = 4 7	Logical or contents of Accumulator with designated port (4 – 7)	1	0	0	0	1	1	p	p	1	1							
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 2	Logical or Immediate specified data with designated port (1 or 2)	1	0	0	0	1	0	p	p	2	2							
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0									
OUT DBB, A	(DBB) (A)	**Output contents of Accumulator onto DBB and set OBF.**	0	0	0	0	0	0	1	0	1	1							
OUTL Pp, A	(Pp) ← (A), p = 1 2	Output contents of Accumulator to designated port (1 or 2)	0	0	1	1	1	0	p	p	1	1							
REGISTERS																			
DEC Rr (Rr)	(Rr) ← (Rr) 1 r = 0 7	Decrement by 1 contents of designated register	1	1	0	0	1	r	r	r	1	1							
INC Rr	(Rr) ← (Rr) +1 r = 0 7	Increment by 1 contents of designated register	0	0	0	1	1	r	r	r	1	1							
INC @ Rr	((Rr)) ← ((Rr)) + 1 r = 0 1	Increment Indirect by 1 the contents of data memory location	0	0	0	1	0	0	0	r	1	1							
SUBROUTINE																			
CALL addr	((SP)) ← (PC), (PSW 4 7) (SP) ← (SP) + 1 (PC 8 10) ← addr 8 10 (PC 0 7) ← addr 0 7 (PC 11) ← DBF	Call designated Subroutine	a_{10}	a_9	a_8	1	0	1	0	0	2	2							
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0									
RET	(SP) ← (SP) 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word	1	0	0	0	0	0	1	1	2	1							
RETR	(SP) ← (SP) 1 (PC) ← ((SP)) (PSW 4 7) ← ((SP))	Return from Subroutine restoring Program Status Word	1	0	0	1	0	0	1	1	2	1							
TIMER/COUNTER																			
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output	0	0	1	0	0	1	0	1	1	1							
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output	0	0	1	1	0	1	0	1	1	1							
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator	0	1	0	0	0	0	1	0	1	1							
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter	0	1	1	0	0	0	1	0	1	1							
STOP TCNT		Stop Count for Event Counter	0	1	1	0	0	1	0	1	1	1							
STRT CNT		Start Count for Event Counter	0	1	0	0	0	1	0	1	1	1							
STRT T		Start Count for Timer	0	1	0	1	0	1	0	1	1	1							
MISCELLANEOUS																			
NOP		No Operation performed	0	0	0	0	0	0	0	0	1	1							

Notes
① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
IBF	Input Buffer Full Flag

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Inputs 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By
OBF	Output Buffer Full
DBB	Data Bus Buffer

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8041AC
Ceramic, μPD8041AD
Cerdip, μPD8741AD, has quartz window

Notes

Description

The μPD8048H family of single chip 8-bit microcomputers is comprised of the μPD8048H and the μPD8035HL. The processors in this family differ only in their internal program memory options: The μPD8048H with 1K x 8 bytes of mask ROM and the μPD8035HL with external memory.

Features

- ☐ Fully Compatible with Industry Standard 8048/8748/8035
- ☐ HMOS Silicon Gate Technology Requiring a Single +5V Supply
- ☐ 2.5 μs Cycle Time. All Instructions 1 or 2 Bytes
- ☐ Interval Timer/Event Counter
- ☐ 64 x 8 Byte RAM Data Memory
- ☐ External and Timer Interrupts
- ☐ 96 Instructions: 70% Single Byte
- ☐ 27 I/O Lines
- ☐ Internal Clock Generator
- ☐ 8 Level Stack
- ☐ Compatible with 8080A/8085A Peripherals
- ☐ Available in Both Ceramic and Plastic 40 Pin Packages

Functional Description

The NEC μPD8048H and μPD8035HL are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048H family of components functions efficiently in control as well as in arithmetic applications. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048H/8035HL instruction set is comprised of 1 and 2 byte instructions with over 70% of them single-byte and requiring only 1 or 2 cycles per instruction with over 50% single-cycle.

The μPD8048H series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

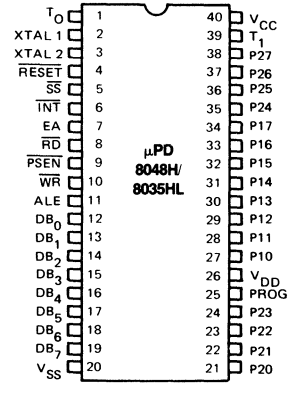
The μPD8048H contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8035HL is intended for applications using external program memory only. It contains all the features of the μPD8048H except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

Pin Identification

Pin No.	Pin Symbol	Function
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non-TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using RD and WR strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{RD}$, and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is used as an output strobe for the μPD8243.
26	V_{DD}	V_{DD} must be set to +5V for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048H.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for operation of the μPD8035H and μPD8048H.

Pin Configuration



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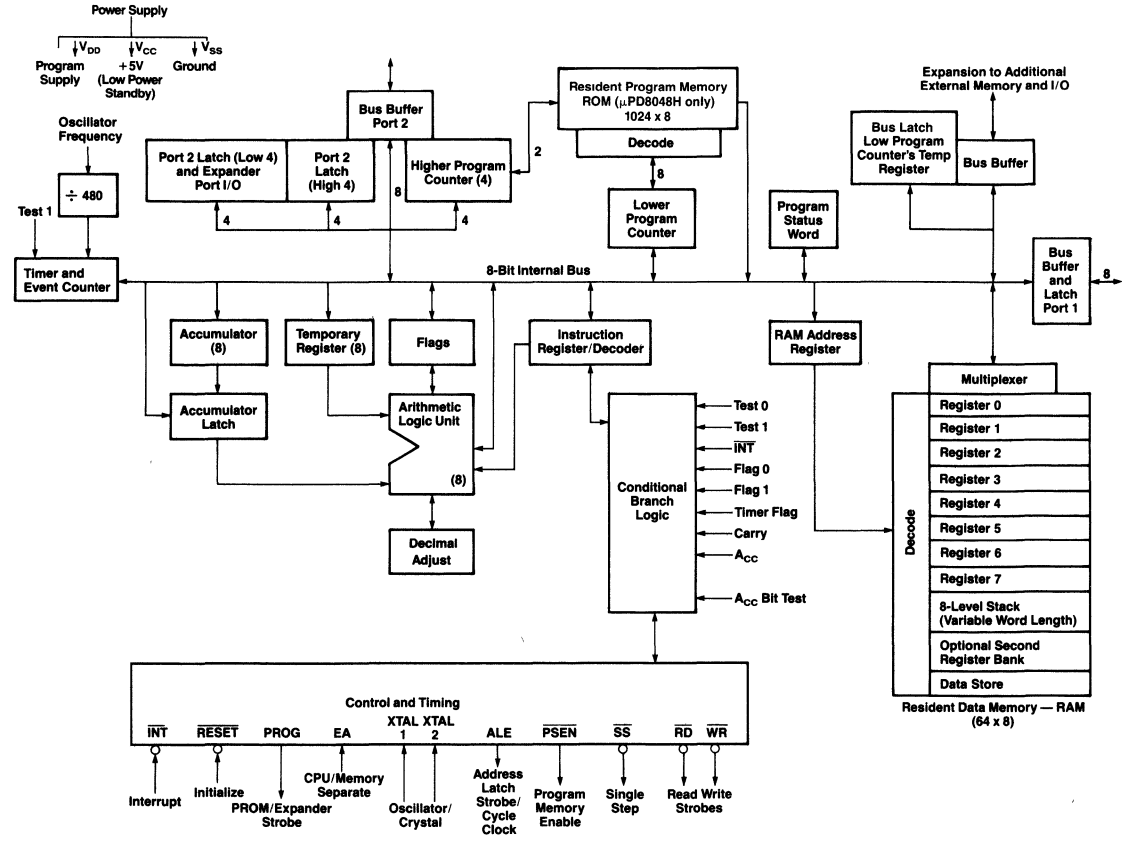
Block Diagram



Note: μPD8035H does not include ROM.

DC Characteristics

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	−0.5		0.8	V	
Input Low Voltage ($\overline{RESET}$, X1, X2)	V_{IL1}	−0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage ($\overline{RESET}$, XTAL 1, XTAL 2)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (BUS)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs)	V_{OL3}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage (BUS)	V_{OH}	2.4			V	I_{OH} = −400 μA
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	I_{OH} = −400 μA
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	I_{OH} = −40 μA
Input Leakage Current (T_1, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Leakage Current (P_{10}–P_{17}, P_{20}–P_{27}, EA, $\overline{SS}$)	I_{IL1}			−500	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Output Leakage Current (BUS, T_0–High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Power Down Supply Current	I_{DD}		4	8	mA	T_a = 25°C
Total Supply Current	$I_{DD} + I_{CC}$		50	80	mA	T_a = 25°C
RAM Standby Voltage	V_{DD}	2.2		5.5	V	Standby Mode. Reset ≤ 0.6V

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V ①
Power Dissipation	1.5 W

Note: ① With respect to ground

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

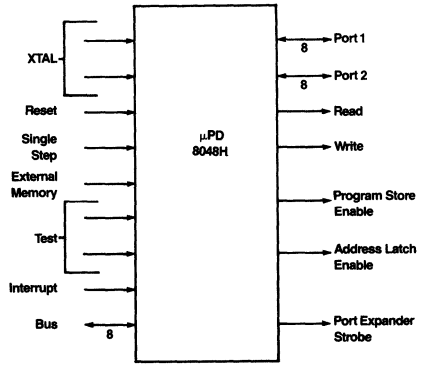
AC Characteristics

T_a = 0°C to 70°C; V_{CC} = V_{DD} = 5V ± 10%; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	f(t_{CY}) and Test Conditions ①
ALE Pulse Width	t_{LL}	410			ns	7/30 t_{CY} − 170
Addr Setup to ALE	t_{AL}	220			ns	2/15 t_{CY} − 110
Addr Hold from ALE	t_{LA}	120			ns	1/15 t_{CY} − 40
Control Pulse Width (RD, WR)	t_{CC1}	1050			ns	1/2 t_{CY} − 200
Control Pulse Width ($\overline{PSEN}$)	t_{CC2}	800			ns	2/5 t_{CY} − 200
Data Setup $\overline{WR}$	t_{DW}	880			ns	13/30 t_{CY} − 200
Data Hold after $\overline{WR}$	t_{WD}	110			ns	1/15 t_{CY} − 50 ②
Data Hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	0		220	ns	1/10 t_{CY} − 30
$\overline{RD}$ to Data in	t_{RD1}			800	ns	2/5 t_{CY} − 200
$\overline{PSEN}$ to Data in	t_{RD2}			550	ns	3/10 t_{CY} − 200
Addr Setup to $\overline{WR}$	t_{AW}	680			ns	1/3 t_{CY} − 150
Addr Setup to Data ($\overline{RD}$)	t_{AD1}			1570	ns	11/15 t_{CY} − 250
Addr Setup to Data ($\overline{PSEN}$)	t_{AD2}			1090	ns	8/15 t_{CY} − 250
Addr Float to $\overline{RD}$, $\overline{WD}$	t_{AFC1}	290			ns	2/15 t_{CY} − 40
Addr Float to $\overline{PSEN}$	t_{AFC2}	40			ns	1/30 t_{CY} − 40
ALE to Control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	420			ns	1/5 t_{CY} − 75
ALE to Control ($\overline{PSEN}$)	t_{LAFC2}	170			ns	1/10 t_{CY} − 75
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	120			ns	1/15 t_{CY} − 40
Control to ALE ($\overline{PSEN}$)	t_{CA2}	620			ns	4/15 t_{CY} − 40
Port Control Setup to $\overline{PROG}$	t_{CP}	210			ns	1/10 t_{CY} − 40
Port Control Hold to $\overline{PROG}$	t_{PC}	460			ns	4/15 t_{CY} − 200
PROG to P2 Input Valid	t_{PR}			1300	ns	17/30 t_{CY} − 120
Input Data Hold from $\overline{PROG}$	t_{PF}			250	ns	1/10 t_{CY}
Output Data Setup	t_{DP}	850			ns	2/5 t_{CY} − 150
Output Data Hold	t_{PD}	200			ns	1/10 t_{CY} − 50
$\overline{PROG}$ Pulse Width	t_{PP}	1500			ns	7/10 t_{CY} − 250
Port 2 I/O Setup to ALE	t_{PL}	460			ns	4/15 t_{CY} − 200
Port 2 I/O Hold to ALE	t_{LP}	150			ns	1/10 t_{CY} − 100
Port Output from ALE	t_{PV}			850	ns	3/10 t_{CY} + 100
Cycle Time	t_{CY}	2.5			μs	6MHz
TO Rep Rate	t_{OPRR}	500			ns	3/15 t_{CY}

Notes: ① Control Outputs CL = 80pF
BUS Outputs CL = 150pF
② BUS High Impedance Load 20pF

Logic Symbol



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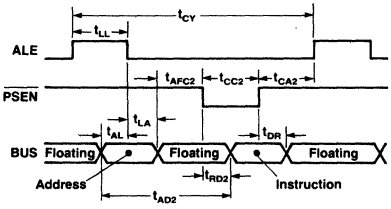
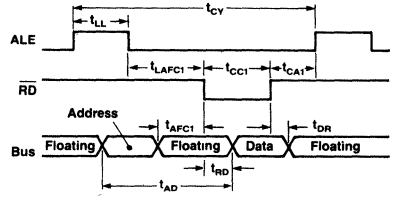
Timing Waveforms

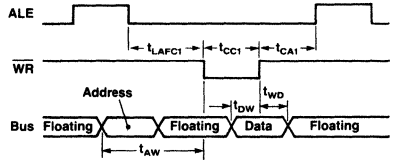
Instruction Fetch from External Memory



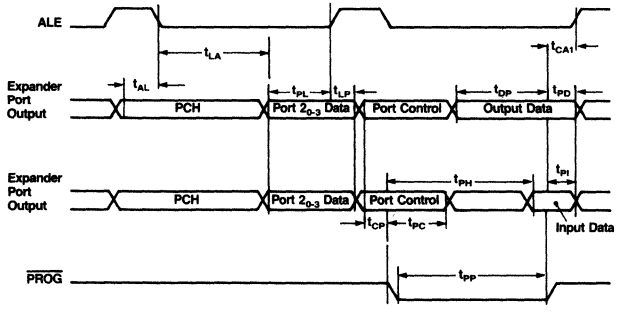
Read from External Data Memory



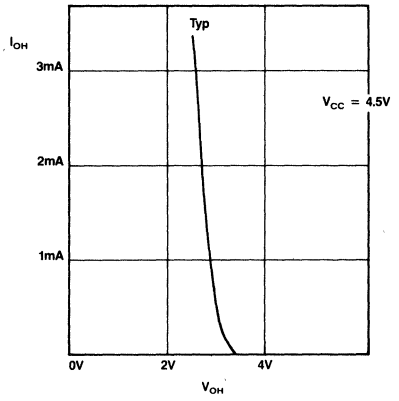
Write to External Memory



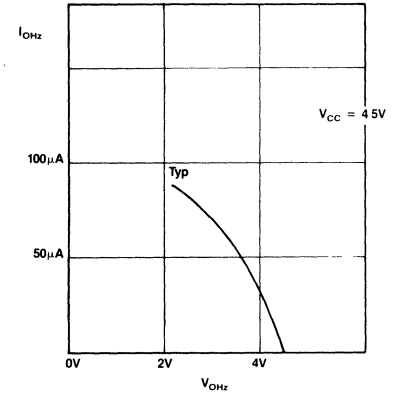
Port 2 Timing



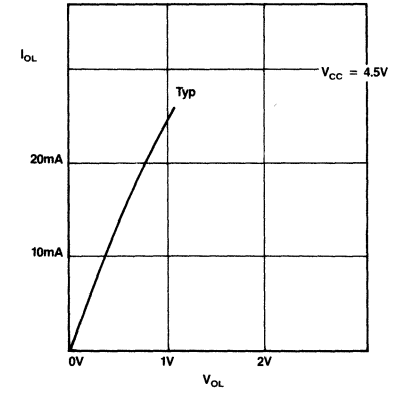
BUS Output High Voltage vs. Source Current



Port P1 and P2 Output High Voltage vs. Source Current



BUS Output Low Voltage vs. Sink Current



Instruction Set (for Symbol Definitions, see page 8.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0
Accumulator															
ADD A, # data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•		
ADD A, Rr	(A) ← (A) + (Rr) for r = 0–7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•		
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0–1	Add Indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•		
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•		
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•		
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0–1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•		
ANL A, # data	(A) ← (A) AND data	Logical AND specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2			
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0–7	Logical AND contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1			
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0–1	Logical AND Indirect the contents of data memory with Accumulator	0	1	0	1	0	0	0	r	1	1			
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1			
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1			
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•		
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1			
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1			
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2			
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0–7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1			
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0–1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1			
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0–6	Rotate Accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1			
RLC A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•		
RR A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (A_0)	Rotate Accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1			
RRC A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•		
SWAP A	(A_{4-7}) ← (A_{0-3})	Swap the two 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1			
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2			
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1			
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0–1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1			
Branch															
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 if (Rr) = 0 (PC 0–7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2			
JBb addr	(PC 0–7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2			
JC addr	(PC 0–7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2			
JF0 addr	(PC 0–7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2			
JF1 addr	(PC 0–7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2			
JMP addr	(PC 8–10) ← addr 8–10 (PC 0–7) ← addr 0–7 (PC11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2			
JMPP @ A	(PC 0–7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1			
JNC addr	(PC 0–7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2			
JNI addr	(PC 0–7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2			

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (Cont.)																
JNT0 addr	(PC 0–7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0–7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0–7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0–7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0–7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0–7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0–7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the Contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the Contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0–7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0–7) ← (A) (PC 8–10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ ((Rr)); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇆ ((Rr)(0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Input/Output																
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical AND immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 – 2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical AND contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 = 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	2	1				
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical OR immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical OR contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	2	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 – 2	Logical OR immediate specified data with designated port (1 – 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A ⑤	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	2	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1– 2).	0	0	1	1	1	0	p	p	2	1				
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) + 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) = 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) = 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable internal interrupt Flag for Timer/ Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable internal interrupt Flag for Timer/ Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/ Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected
⑤ When the Bus is written to, with an OUTL instruction, the Bus remains an Output Port until either device is reset or a MOVX instruction is executed

Symbol Definitions

Symbol	Description
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number of Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8048HC/35HLC
Ceramic, μPD8048HD/35HLD

μPD8048 FAMILY OF SINGLE CHIP 8-BIT MICROCOMPUTERS

DESCRIPTION

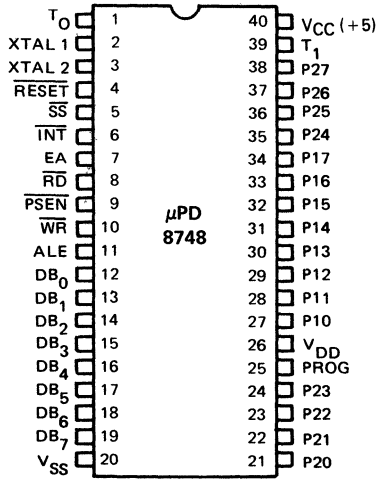
The μPD8748 is a member of the μPD8048 family of single-bit 8-chip microcomputers. It differs from the μPD8048H/8035HL in that it contains 2K of on-board EPROM rather than math programmable ROM. The μPD8748 uses N-channel MOS technology. Refer to the μPD8048H/8035HL data sheet for additional information.

FEATURES

- Fully Compatible With Industry Standard 8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 Byte RAM Data Memory
- Single Level Interrupt
- 96 Instructions: 70% Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages

4

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The NEC μPD8748 is a single component, 8-bit, parallel microprocessor using N-channel silicon gate MOS technology. The 8748 efficiently functions in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

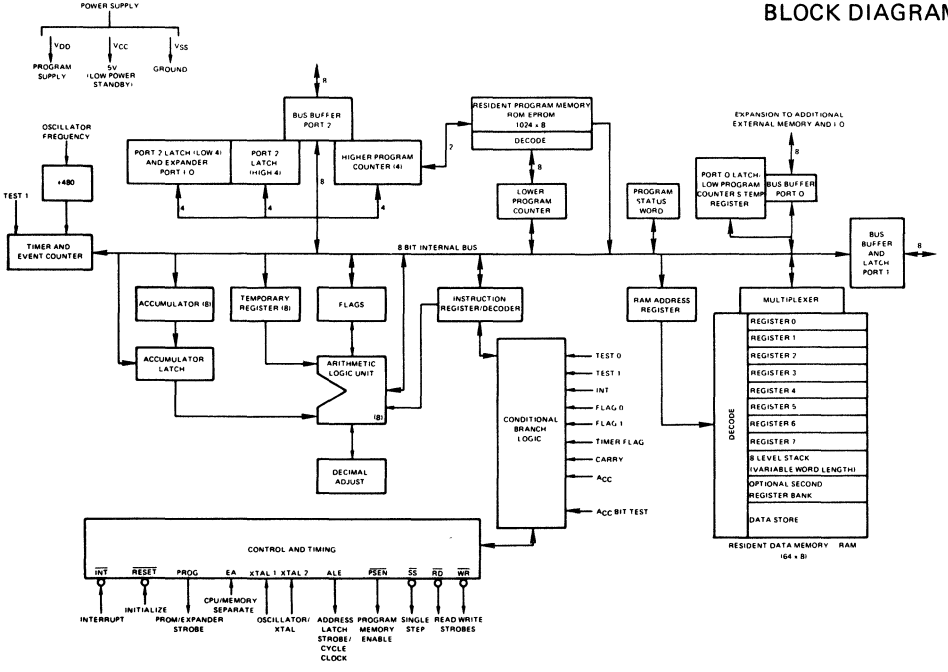
The μPD8748 instruction set is comprised of 1 and 2 byte instructions with over 70% single-byte and requiring only 1 or 2 cycles per instruction with over 50% single-cycle.

The μPD8748 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8748 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0 The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction T_0 can also be used during programming as a testable flag
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low) $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory
6	$\overline{INT}$	Interrupt input (active-low) $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high) A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential
21 – 24, 35 – 38	$P_{20} - P_{27}$ PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27 – 34	$P_{10} - P_{17}$ PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for programming and operation of the μPD8748, and for operation of the μPD8035L and μPD8048.

4

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	-65°C to +150°C
Storage Temperature (Plastic Package)	-65°C to +150°C
Voltage on Any Pin	- 0.5 to +7 Volts ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = -0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	3 8		V_{CC}	V	
Output Low Voltage (BUS)	V_{OL}			0 45	V	$I_{OL} = 2.0$ mA
Output Low Voltage ($\overline{RD}$, $\overline{WR}$, PSEN, ALE)	V_{OL1}			0 45	V	$I_{OL} = 1.8$ mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	$I_{OL} = 1.0$ mA
Output Low Voltage (All Other Outputs)	V_{OL3}			0 45	V	$I_{OL} = 1.6$ mA
Output High Voltage (BUS)	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	$I_{OH} = -100\ \mu A$
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	$I_{OH} = -40\ \mu A$
Input Leakage Current (T_1, INT)	I_{LI}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Leakage Current (P_{10}-P_{17}, P_{20}-P_{27}, EA, $\overline{SS}$)	I_{LI1}			-500	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
Power Down Supply Current	I_{DD}		7	15	mA	$T_a = 25°C$
Total Supply Current	$I_{DD} + I_{CC}$		60	135	mA	$T_a = 25°C$

DC CHARACTERISTICS PROGRAMMING THE μPD8748

$T_a = 25°C \pm 5°C$, $V_{CC} = +5V \pm 10\%$, $V_{DD} = +25V \pm 1V$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{DD} Program Voltage High-Level	V_{DOH}	24.0		26 0	V	
V_{DD} Voltage Low-Level	V_{DDL}	4.75		5.25	V	
PROG Voltage High-Level	V_{PH}	21 5		24.5	V	
PROG Voltage Low-Level	V_{PL}			0 2	V	
EA Program or Verify Voltage High-Level	V_{EAH}	21.5		24 5	V	
EA Voltage Low-Level	V_{EAL}			5.25	V	
V_{DD} High Voltage Supply Current	I_{DD}			30.0	mA	
PROG High Voltage Supply Current	I_{PROG}			16.0	mA	
EA High Voltage Supply Current	I_{EA}			1 0	mA	

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

AC CHARACTERISTICS T_a = 0°C to +70°C, V_{CC} - V_{DD} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST ① CONDITIONS
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	120			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	700			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2 5		15 0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			ns	
Control Pulse to ALE	**t_{CA}**	**10**			**ns**	

Notes ① For Control Outputs C_L = 80 pF
For Bus Outputs C_L = 150 pF
t_{CY} = 2 5 μs

PORT 2 TIMING

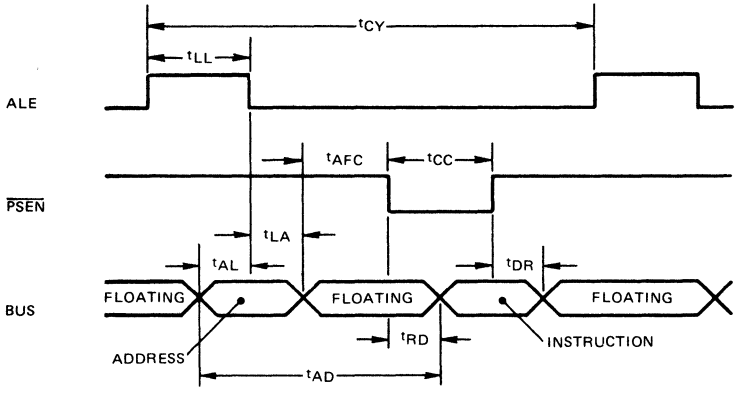
T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of $\overline{PROG}$	t_{CP}	110			ns	
Port Control Hold after Falling Edge of $\overline{PROG}$	t_{PC}	100			ns	
$\overline{PROG}$ to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	250			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
$\overline{PROG}$ Pulse Width	t_{PP}	1200			ns	
Port 2 I/O Data Setup	t_{PL}	350			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

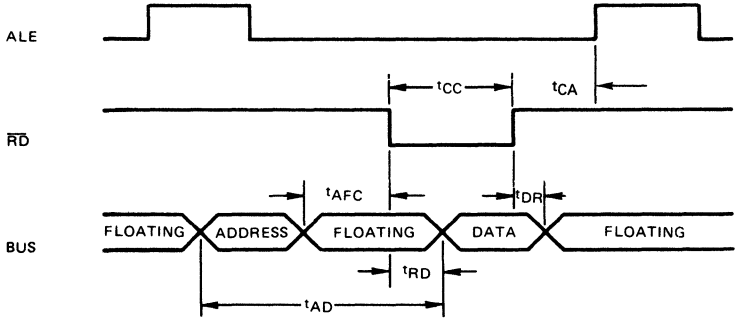
PROGRAMMING SPECIFICATIONS – μPD8748

T_a = 25°C ± 5°C; V_{CC} = +5V ± 10%; V_{DD} = +25V ± 1V

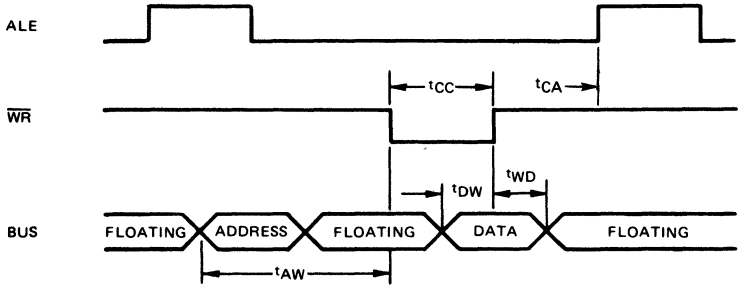
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Address Setup Time before $\overline{RESET}$ ↑	t_{AW}	4 t_{CY}				
Address Hold Time after $\overline{RESET}$ ↑	t_{WA}	4 t_{CY}				
Data In Setup Time before $\overline{PROG}$ ↑	t_{DW}	4 t_{CY}				
Data In Hold Time after $\overline{PROG}$ ↓	t_{WD}	4 t_{CY}				
RESET Hold Time to VERIFY	t_{PH}	4 t_{CY}				
V_{DD}	t_{VDDW}	4 t_{CY}				
V_{DD} Hold Time after $\overline{PROG}$ ↓	t_{VDDH}	0				
Program Pulse Width	t_{PW}	50		60	ms	
Test 0 Setup Time before Program Mode	t_{TW}	4 t_{CY}				
Test 0 Hold Time after Program Mode	t_{WT}	4 t_{CY}				
Test 0 to Data Out Delay	t_{DO}			4 t_{CY}		
$\overline{RESET}$ Pulse Width to Latch Address	t_{WW}	4 t_{CY}				
V_{DD} and $\overline{PROG}$ Rise and Fall Times	t_r,t_f	0.5		2.0	μs	
Processor Operation Cycle Time	t_{CY}	5.0			μs	
$\overline{RESET}$ Setup Time before EA ↑	t_{RE}	4 t_{CY}				



INSTRUCTION FETCH FROM EXTERNAL MEMORY

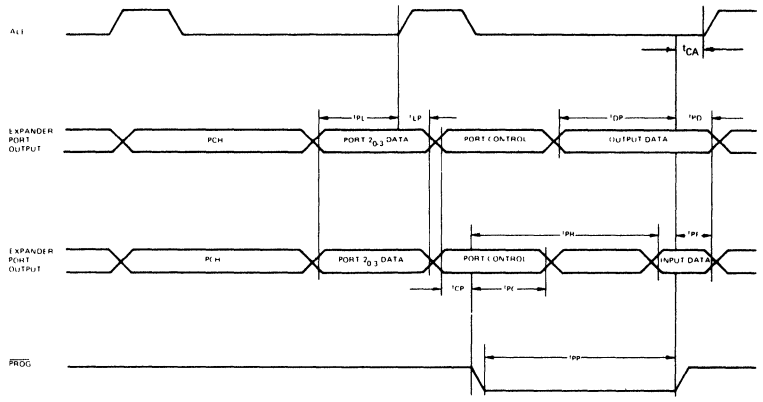


READ FROM EXTERNAL DATA MEMORY

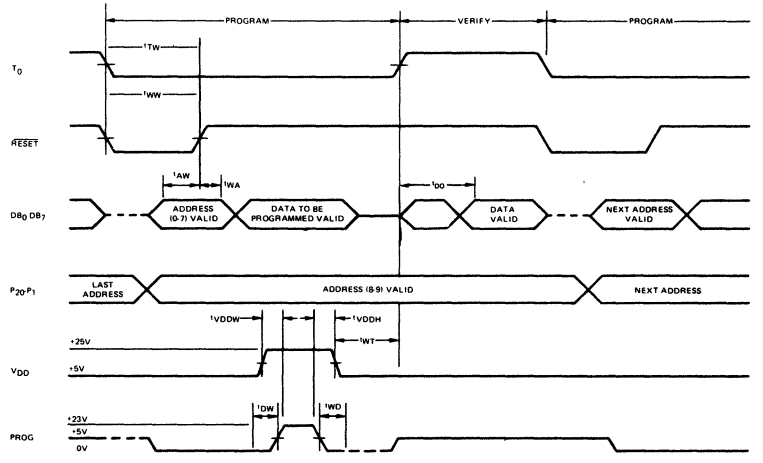


WRITE TO EXTERNAL MEMORY

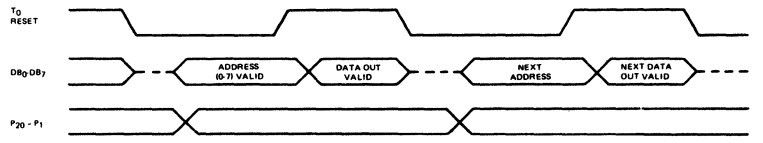
TIMING WAVEFORMS (CONT.)



PORT 2 TIMING



PROGRAM/VERIFY TIMING
(μPD8748 ONLY)



VERIFY MODE TIMING
(μPD8048/8748 ONLY)

Notes:
① Conditions: $\overline{CS}$ TTL Logic "1"; Ao TTL Logic "0" must be met. (Use 10K resistor to V_{CC} for $\overline{CS}$, and 10K resistor to V_{SS} for Ao)
② t_{CY} 5μs can be achieved using a 3 MHz frequency source (LC, XTAL or external) at the XTAL 1 and XTAL 2 inputs.

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, # data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 1	Logical and Indirect the contents of data memory with Accumulator	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) · (A) 1	DECREMENT by 1 the accumulator's contents	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical ORcontents of designated register with Accumulator	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1 bit without carry	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN), N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1), N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ⇄ (A_0 – 3)	Swap the 2 4-bit nibbles in the Accumulator	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) – 1, r = 0 – 7 If (Rr) ≠ 0 (PC 0 – 7) ← addr	Decrement the specified register and test contents	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if FO = 1 (PC) ←)(PC) + 2 if FO = 0	Jump to specified address if Flag F0 is set	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page	1	0	1	1	0	0	1	1	2•	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non zero	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 2047) of Program Memory	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 4095) of Program Memory	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 31) of Data Memory	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, data	(A) ← data	Move Immediate the specified data into the Accumulator	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr), r = 0 – 7	Move the contents of the designated registers into the Accumulator	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)), r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator	1	1	0	0	0	1	1	1	1	1				
MOV Rr, data	(Rr) ← data, r = 0 – 7	Move Immediate the specified data into the designated register	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A), r = 0 – 7	Move Accumulator Contents into the designated register	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A), r = 0 – 1	Move Indirect Accumulator Contents into data memory location	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, data	((Rr)) ← data, r = 0 – 1	Move Immediate the specified data into data memory	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)), r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A), r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr), r = 0 – 7	Exchange the Accumulator and designated register's contents	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)), r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)) 0 – 3)), r = 0 – 1	Exchange Indirect 4 bit contents of Accumulator and data memory	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) NOT (C)	Complement Content of carry bit	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) · NOT (F0)	Complement Content of Flag F0	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) 0	Clear content of carry bit to 0	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) · 0	Clear content of Flag 0 to 0	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) 0	Clear content of Flag 1 to 0	1	0	1	0	0	1	0	1	1	1				•

4

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, #data	(BUS) ← (BUS) AND data	Logical and Immediate specified data with contents of BUS	1	0	0	1	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL Pp, #data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7)	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp), p = 1 – 2	Input data from designated port (1 – 2) into Accumulator	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp), p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3, p = 4 – 7	Move contents of Accumulator to designated port (4 – 7)	0	0	1	1	1	1	p	p	2	1				
ORL BUS, #data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS	1	0	0	0	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7)	1	0	0	0	1	1	p	p	2	1				
ORL Pp, #data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2)	1	0	0	0	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS	0	0	0	0	0	0	1	0	2	1				
OUTL Pp, A	(Pp) ← (A), p = 1 – 2	Output contents of Accumulator to designated port (1 – 2)	0	0	1	1	1	0	p	p	2	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) + 1, r = 0 – 7	Decrement by 1 contents of designated register	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1, r = 0 – 7	Increment by 1 contents of designated register	0	0	0	1	1	r	r	r	1	1				
INC @ Ri	((Ri)) ← ((Ri)) + 1, r = 0 – 1	Increment Indirect by 1 the contents of data memory location	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal Interrupt Flag for Timer/Counter output	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal Interrupt Flag for Timer/Counter output	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed	0	0	0	0	0	0	0	0	1	1				

Notes ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in

③ References to the address and data are specified in bytes 2 and/or 1 of the instruction

④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

Package Outlines

For information, see Package Outline Section 7.

Cerdip, μPD8748D, has quartz window

Description

The NEC μPD80C48 is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 1K-byte ROM, a 64-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C48 can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C48 without ROM is offered by the μPD80C35.

Providing compatibility with industry-standard 8048, 8748, and 8035 processors, the μPD80C48 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C48 is distinct in offering two standby modes (Halt mode and Stop mode) to further minimize power drain.

Features

- ☐ 8-bit CPU with ROM, RAM, and I/O on a single chip
- ☐ Hardware/software-compatible with industry-standard 8048, 8748, and 8035 processors
- ☐ 1K x 8 ROM
- ☐ 64 x 8 RAM
- ☐ 27 I/O lines
- ☐ 2.5μs cycle time (6MHz crystal)
- ☐ All instructions executable in 1 or 2 cycles
- ☐ 97 instructions: 70 percent are single-byte instructions
- ☐ Internal timer/event counter
- ☐ 2 interrupts (an external interrupt and a timer interrupt)
- ☐ Easily expandable memory and I/O
- ☐ Bus compatible with 8080A/8085A peripherals
- ☐ Power-efficient CMOS technology requiring a single +2.5V to +5.5V power supply
- ☐ Available in 40-pin DIP, 44-pin flat pack, and 52-pin flat pack
- ☐ Halt mode
  - 1mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- ☐ Stop mode
  - 1μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware (V_{DD})
  - Mode release via reset

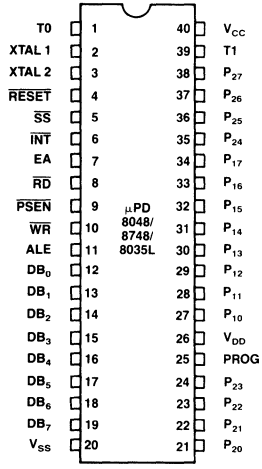
Pin Identification

Pin No.	Symbol	Name	Function
1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENTO CLK instruction.
2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals (Non-TTL-compatible V_{IH})
3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. (Non-TTL-compatible V_{IH})
4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes ①
5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time
6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode
7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging
8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory
9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory
10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory
11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus
12–19	DB_0–DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals
20	V_{SS}	Ground	Ground potential
21–24, 35–38	P_{20}–P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches, P_{20}–P_{23} output the most-significant 4 bits of the external program memory address. Lines P_{20}–P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander
25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
26	V_{DD}	Oscillator Control Voltage Line	This input line is used to control oscillator stopping and restarting in Stop mode. Stop mode is enabled by forcing V_{DD} LOW during a reset.
27–34	P_{10}–P_{17}	Port 1	These lines constitute Port 1, an 8-bit, general-purpose quasi-bidirectional port.
39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction
40	V_{CC}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +5.5V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: ① The pulse width of $\overline{RESET}$ must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset

Rev/1

Pin Configuration



Standby Function

HALT mode

In Halt mode, the oscillator continues to operate, but the internal clock is disabled. The status of all internal logic just prior to execution of the HALT instruction is maintained by the CPU. In Halt mode, power consumption is less than 10 percent of normal μPD80C48 operation and less than 1 percent of normal 8048 operation.

The Halt mode is initiated by execution of the HALT instruction, and is released by either INT or RESET input.

INT input: When the INT pin receives a low-level input, if interrupts are enabled, the internal clock is restarted and the interrupt is executed after the first or second instruction following the HALT instruction. However, if interrupts are disabled, program operation is resumed from the next address following the HALT instruction. The first instruction following a HALT instruction should be a NOP instruction to ensure proper program execution.

If the Halt mode is released when interrupts are enabled, the interrupt service routine is usually executed after the first or second instruction following the release of Halt mode. However, if either a timer or external interrupt is accepted within one machine cycle prior to a HALT instruction, the corresponding timer or external interrupt service routine is executed immediately following the release of Halt mode. It is important to note this sequence of execution when considering interrupt service routine execution following a HALT instruction.

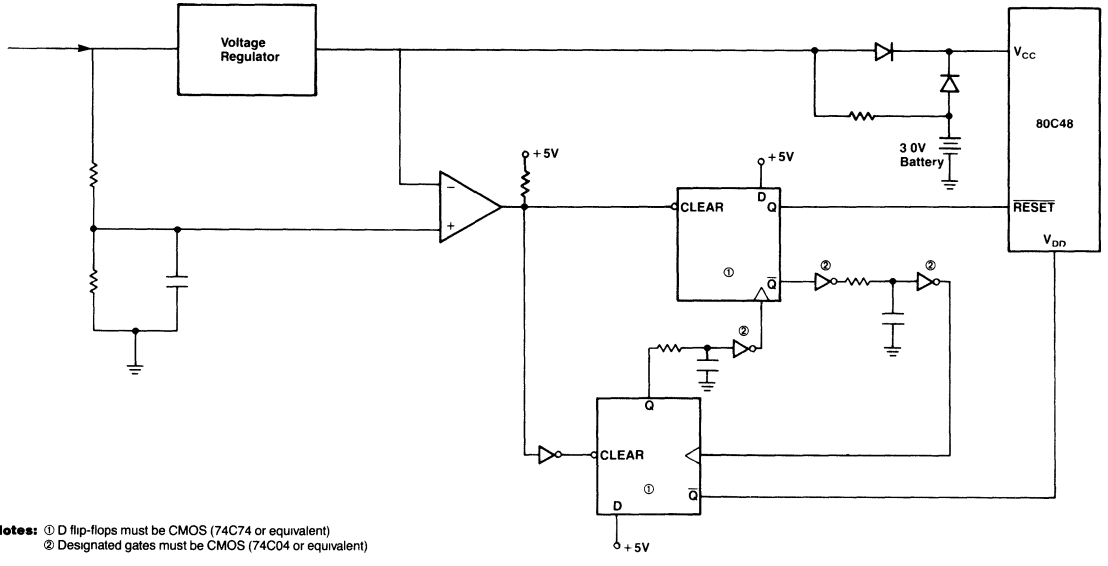
RESET input: When a low-level input is received by the RESET pin, Halt mode is released and the normal reset operation is activated, restarting program operation from address 0.

Stop mode

In Stop mode, the oscillator is deactivated and only the contents of RAM are maintained. The operation status of the μPD80C48 resembles that of a reset condition. Because only the contents of RAM are maintained, Stop mode provides even lower power consumption than Halt mode, only requiring a minimum V_{CC} as low as +2V.

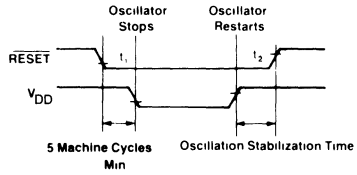
Stop mode is initiated by setting V_{DD} to LOW when RESET is LOW, to protect the contents of RAM. Stop mode is released by first raising the supply voltage at the V_{CC} pin from standby level to correct operating level and setting V_{DD} to HIGH when RESET is LOW. After the oscillator has been restarted and the oscillation has stabilized, RESET must be set to HIGH, whereby program operation is started from address 0.

Stop Mode Circuit



Notes: ① D flip-flops must be CMOS (74C74 or equivalent)
② Designated gates must be CMOS (74C04 or equivalent)

Stop Mode Timing

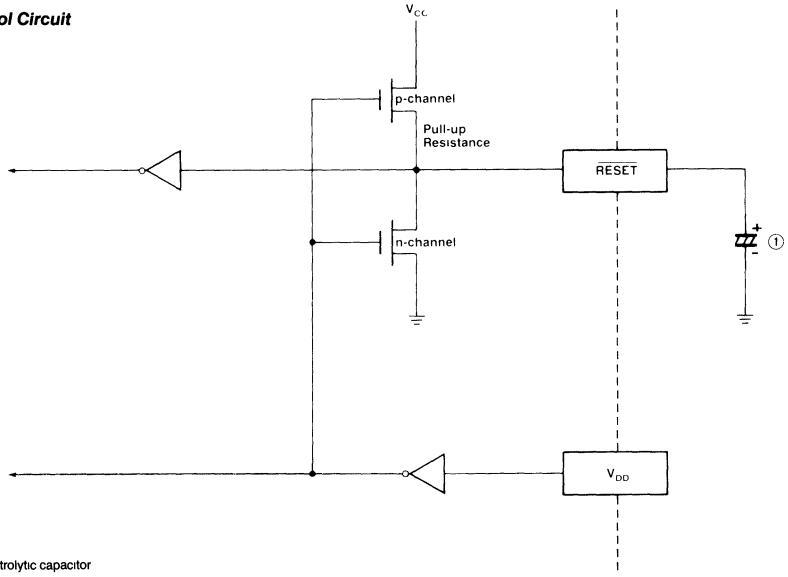


Stop Mode Circuit: Since V_{DD} controls the restarting of the oscillator, it is important that V_{DD} be protected from noise interference. The time required to reset the CPU is represented by t_1 (see Stop Mode Timing diagram), which is a minimum of 5 machine cycles. The reset operation will not be completed in less than 5 machine cycles. In Stop mode, it is important to note that if V_{DD} goes LOW before 5 machine cycles have elapsed, the CPU will be deactivated and the output of ALE, RD, WR, PSEN, and PROG will not have been stabilized.

Oscillation stabilization time is represented by t_2 (see Stop Mode Timing diagram). When V_{DD} goes HIGH, oscillator operation is reactivated, but it takes time before oscillation can be stabilized. In particular, such high Q resonators as crystals require longer periods to stabilize. Because there is a delay between restarting of the oscillator and oscillator stabilization, t_2 should be long enough to ensure that the oscillator has been fully stabilized.

To facilitate Stop mode control, an external capacitor can be connected to the RESET pin (see Stop Mode Control Circuit), affecting only t_2, allowing control of the oscillator stabilization time. When V_{DD} is asserted in Stop mode, the capacitor begins charging, pulling up RESET. When RESET reaches a threshold level equivalent to a logic 1, Stop mode is released. The time it takes RESET to reach the threshold level of logic 1 determines the oscillator stabilization time, which is a function of the capacitance and pull-up resistance values.

Stop Mode Control Circuit



Note: ① Polarized electrolytic capacitor

Port Operation

A port-loading option is offered at the time of ordering the mask. Individual source current requirements for Port 1 and the upper and lower halves of Port 2 may be factory set at either $-5\mu A$ or $-50\mu A$ (see Port-Loading Options table). The $-50\mu A$ option is required for interfacing with TTL/NMOS devices. The $-5\mu A$ option is recommended for interfacing to other CMOS devices. The CMOS option results in lower power consumption and greater noise immunity.

Port lines P_{10} to P_{17} and P_{24} to P_{27} include a protective circuit "E" to prevent a signal conflict at the port. The circuit prevents a logic 1 from being written to a line that is being pulled down externally (see Port Protection Circuit "E" diagram). When a logic 0 is detected at the port line and a logic 1 is written from the bus, the NOR gate sends a logic 1 to the D input of the flip-flop. The output is inverted, forcing the NAND gate to send a high-level output. This turns off transistor A, preventing the output of a logic 1 from the port.

Port-Loading Options

I_{OH} (min) V_{CC} = V_{DD} = 5V ± 10%; V_{OH} = 2.4V (min)

Option Selected	P_{10}–P_{17}	P_{20}–P_{23}	P_{24}–P_{27}	Unit
A	−5	−5	−5	μA
B	−50	−5	−5	μA
C	−5	−50	−5	μA
D	−50	−50	−5	μA
E	−5	−5	−50	μA
F	−50	−5	−50	μA
G	−5	−50	−50	μA
H	−50	−50	−50	μA

Notes: ① The selection of $I_{OH} = -5\mu A$ will result in a port source current of $I_{ILP} = -40\mu A$ max when used as input port
② The selection of $I_{OH} = -50\mu A$ will result in a port source current of $I_{ILP} = -500\mu A$ max when used as input port

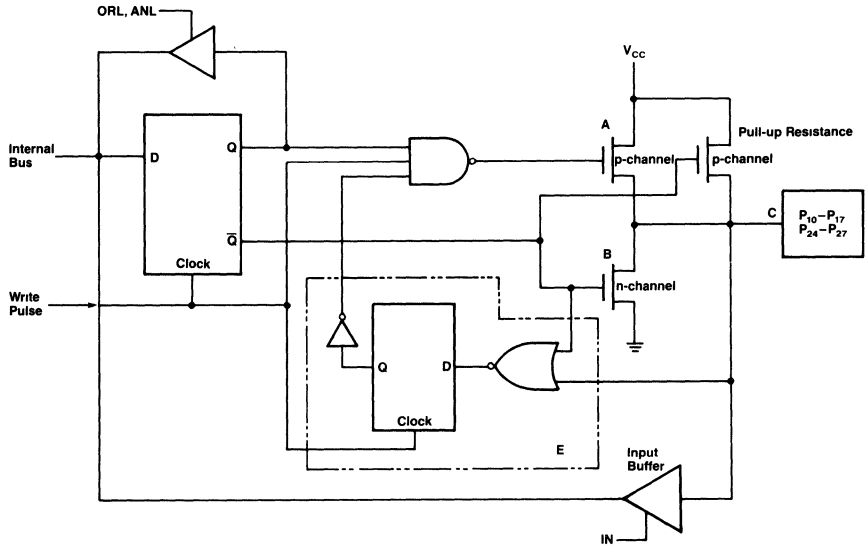
Oscillator Operation

The oscillator maintains an internal frequency for clock generation and controls all system timing cycles. The oscillation is initiated by either a self-generating external resonator or external clock input. The oscillator acts as a high-gain amplifier which produces square-wave pulses at the frequency determined by the resonator or clock source to which it is connected.

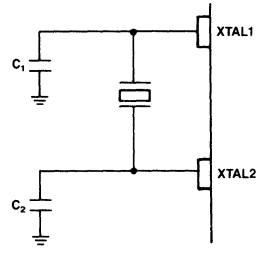
To obtain the oscillation frequency, an external LC network may be connected to the oscillator, or, a ceramic or crystal external resonator may be connected.

As the crystal frequency is lowered, there is an equivalent reduction in series resistance (R). As the temperature of the crystal is lowered, R is increased. Due to this relationship, it becomes difficult to stabilize oscillation when there is low power supply voltage. When V_{CC} is less than 2.7V and the oscillator frequency is 3MHz or less, T_a (ambient temperature) should not be less than −10°C.

Port Protection Circuit "E"



Crystal Frequency Reference Circuit

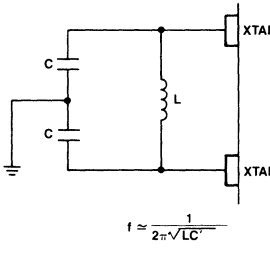


Notes: ① Crystal oscillator constants of f_{osc} = 6MHz
R_{max} = 50Ω
C_L = 16 ± 0 2pF
P = 1 ± 0 2mW

② Operating frequency less than 4MHz
$0 < C_1 \leq 20pF$
$0 < C_2 \leq 20pF$
$| C_2 - C_1 | \leq 10pF$

③ Operating frequency more than 4MHz
$0 < C_1 \leq 10pF$
$0 < C_2 \leq 10pF$
$| C_2 - C_1 | \leq 5pF$

LC Frequency Reference Circuit

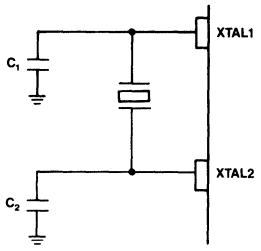


L	C	Nominal f
45μH	20pF	5 2MHz
120μH	20pF	3 2MHz

$$f \simeq \frac{1}{2\pi\sqrt{LC'}} \qquad C' = \frac{C + 3C_{pp}}{2}$$

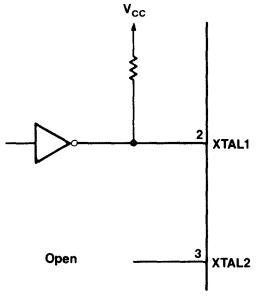
Note: C_{pp} = 5–10pF Pin to pin capacitance should be approximately 20pF, including stray capacitance

Ceramic Resonator Frequency Reference Circuit



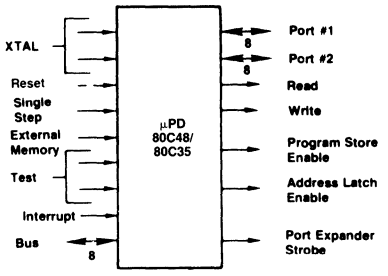
Note: $C_1 > C_2$
$|C_1 - C_2| \approx 20pF$
For example, $C_1 = 30pF$, and $C_2 = 10pF$
Values of C_1 and C_2 do not include stray capacitance

External Clock Frequency Reference Circuit



Note: A minimum voltage of V_{CC}-1 is required for XTAL1 to go HIGH

Major Input and Output Signals



Instruction Set Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program or data memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank Switch
BUS	Bus
C	Carry Flag
CLK	Clock
CNT	Counter
data	8-bit binary data (d_0–d_7)
DBF	Memory Bank Flip-Flop
F0, F1	Flag 0, Flag 1
INT	Interrupt pin
n	Indicates the hex number of the specified register or port
PC	Program Counter
P_p	Port 1, Port 2, or Port 4–7 ($_p$ = 1, 2, or 4–7)
PSW	Program Status Word
R_r	Register R_0–R_7 ($_r$ = 0–7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Test 0, Test 1 pin
#	Immediate data indication
@	Indirect address indication
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the operand
(x)	Contents of RAM
((x))	Contents of memory addressed by (x)
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
⊻	Exclusive OR
—	Complement

4

Instruction Set

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Accumulator													
ADD A, # data	(A) ← (A) + data	Adds immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags.②	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, R_r	(A) ← (A) + (R_r) $_r$ = 0–7	Adds the contents of register R_r to the accumulator. Sets or clears both carry flags ②	6n④	0	1	1	0	1	r	r	r	1	1
ADD A, @ R_r	(A) ← (A) + ((R_r)) $_r$ = 0–1	Adds the contents of the internal data memory location specified by bits 0–5 of register R_r to the accumulator. Sets or clears both carry flags.②	6n④	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + data + (C)	Adds, with carry, immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags.②	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, R_r	(A) ← (A) + (R_r) + (C) $_r$ = 0–7	Adds, with carry, the contents of register R_r to the accumulator. Sets or clears both carry flags.②	7n④	0	1	1	1	1	r	r	r	1	1
ADDC A, @ R_r	(A) ← (A) + ((R_r)) + (C) $_r$ = 0–1	Adds, with carry, the contents of the internal data memory location specified by bits 0–5 of register R_r, to the accumulator. Sets or clears both carry flags.②	7n④	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A)∧data	Takes the logical product (logical AND) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, R_r	(A) ← (A)∧(R_r) $_r$ = 0–7	Takes the logical product (logical AND) of the contents of register R_r and the accumulator, and stores the result in the accumulator	5n④	0	1	0	1	1	r	r	r	1	1
ANL A, @ R_r	(A) ← (A)∧((R_r)) $_r$ = 0–1	Takes the logical product (logical AND) of the contents of the internal data memory location specified by bits 0–5 of register R_r, and the accumulator, and stores the result in the accumulator.	5n④	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← $\overline{(A)}$	Takes the complement of the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clears the contents of the accumulator	27	0	0	1	0	0	1	1	1	1	1
DA A		Converts the contents of the accumulator to BCD. Sets or clears the carry flags. When the lower 4 bits (A_{0-3}) are greater than 9, or if the Auxiliary Carry Flag has been set, adds 6 to A_{0-3}. When the upper 4 bits (A_{4-7}) are greater than 9 or if the Carry Flag (C) has been set, adds 6 to A_{4-7}. If an overflow occurs at this point, C is set.②	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrements the contents of the accumulator by 1.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increments the contents of the accumulator by 1.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A)∨data	Takes the logical sum (logical OR) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, R_r	(A) ← (A)∨(R_r) $_r$ = 0–7	Takes the logical sum (logical OR) of register R_r and the contents of the accumulator, and stores the result in the accumulator	4n④	0	1	0	0	1	r	r	r	1	1
ORL A, @ R_r	(A) ← (A)∨((R_r)) $_r$ = 0–1	Takes the logical sum (logical OR) of the contents of the internal data memory location specified by bits 0–5 in register R_r, and the contents of the accumulator, and stores the result in the accumulator.	4n④	0	1	0	0	0	0	0	r	1	1
RL A	(Ab + 1) ← (Ab) (A_0) ← (A_7) b = 0–6	Rotates the contents of the accumulator one bit to the left. The MSB is rotated into the LSB.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	(Ab + 1) ← (Ab) (A_0) ← (C) (C) ← (A_7) b = 0–6	Rotates the contents of the accumulator one bit to the left through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	(Ab) ← (Ab + 1) (A_7) ← (A_0) b = 0–6	Rotates the contents of the accumulator one bit to the right. The LSB is rotated into the MSB	77	0	1	1	1	0	1	1	1	1	1
RRC A	(Ab) ← (Ab + 1) (A_7) ← (C) (C) ← (A_0) b = 0–6	Rotates the contents of the accumulator one bit to the right through carry	67	0	1	1	0	0	1	1	1	1	1
SWAP A	(A_{4-7}) ↔ (A_{0-3})	Exchanges the contents of the lower 4 bits of the accumulator with the upper 4 bits of the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A)∀data	Takes the exclusive OR of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, R_r	(A) ← (A)∀(R_r) $_r$ = 0–7	Takes the exclusive OR of the contents of register R_r and the accumulator, and stores the result in the accumulator.	Dn④	1	1	0	1	1	r	r	r	1	1
XRL A, @ R_r	(A) ← (A)∀((R_r)) $_r$ = 0–1	Takes the exclusive OR of the contents of the location in data memory specified by bits 0–5 in register R_r, and the accumulator, and stores the result in the accumulator.	Dn④	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ R_r, addr	(R_r) ← (R_r) – 1 If (R_r) ≠ 0, then (PC_{0-7}) ← addr $_r$ = 0–7	Decrements the contents of register R_r by 1, and if the result is not equal to 0, jumps to the address indicated by a_0–a_7.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	(PC_{0-7}) ← addr if b = 1 (PC) = (PC) + 2 if b = 0	Jumps to the address specified by a_0–a_7 if the bit in the accumulator specified by b_0–b_2 is set.	x2⑥	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2

Instruction Set (Cont.)

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Branch (Cont.)													
JC addr	$(PC_{0-7}) \leftarrow$ addr if C = 1 $(PC) \leftarrow (PC) + 2$ if C = 0	Jumps to the address specified by a_0-a_7 if the Carry Flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_{0-7}) \leftarrow$ addr if F0 = 1 $(PC) \leftarrow (PC) + 2$ if F0 = 0	Jumps to the address specified by a_0-a_7 if F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_{0-7}) \leftarrow$ addr if F1 = 1 $(PC) \leftarrow (PC) + 2$ if F1 = 0	Jumps to the address specified by a_0-a_7 if F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_{8-10}) \leftarrow addr_{8-10}$ $(PC_{0-7}) \leftarrow addr_{0-7}$ $(PC_{11}) \leftarrow$ DBF	Jumps directly to the address specified by a_0-a_{10} and the DBF.	x4⑥	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_{0-7}) \leftarrow ((A))$	Replaces the lower 8 bits of the Program Counter with the contents of program memory specified by the contents of the accumulator, producing a jump to the specified address within the current page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_{0-7}) \leftarrow$ addr if C = 0 $(PC) \leftarrow (PC) + 2$ if C = 1	Jumps to the address specified by a_0-a_7 if the Carry Flag is not set	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_{0-7}) \leftarrow$ addr if I = 0 $(PC) \leftarrow (PC) + 2$ if I = 1	Jumps to the address specified by a_0-a_7 if the Interrupt Flag is not set.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jumps to the address specified by a_0-a_7 if Test 0 is LOW.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 0 $(PC) \leftarrow (PC) + 2$ if T1 = 1	Jumps to the address specified by a_0-a_7 if Test 1 is LOW.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_{0-7}) \leftarrow$ addr if A ≠ 0 $(PC) \leftarrow (PC) + 2$ if A = 0	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are not equal to 0.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_{0-7}) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jumps to the address specified by a_0-a_7 if the Timer Flag is set. The Timer Flag is cleared after the instruction is executed.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jumps to the address specified by a_0-a_7 if Test 0 is HIGH.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jumps to the address specified by a_0-a_7 if Test 1 is HIGH.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ	$(PC_{0-7}) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are equal to 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
Control													
EN I		Enables external interrupts. When external interrupts are enabled, a low-level input to the INT pin causes the processor to vector to the interrupt service routine.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disables external interrupts. When external interrupts are disabled, low-level inputs to the INT pin have no effect on program execution.	15	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enables clock output to pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) ← 0	Clears the Memory Bank Flip-Flop, selecting Program Memory Bank 0 [program memory addresses $0-2047_{(10)}$]. Clears PC_{11} after the next JMP or CALL instruction.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) ← 1	Sets the Memory Bank Flip-Flop, selecting Program Memory Bank 1 [program memory addresses $2048-4095_{(10)}$]. Sets PC_{11} after the next JMP or CALL instruction.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Selects Data Memory Bank 0 by clearing bit 4 (Bank Switch) of the PSW. Specifies data memory addresses $0-7_{(10)}$ as registers 0–7 of Data Memory Bank 0.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Selects Data Memory Bank 1 by setting bit 4 (Bank Switch) of the PSW. Specifies data memory $24-31_{(10)}$ as registers 0–7 of Data Memory Bank 1.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates Halt mode.	01	0	0	0	0	0	0	0	1	1	1
Data Moves													
MOV A, # data	(A) ← data	Moves immediate data d_0-d_7 into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, R_r	(A) ← (R_r) $_r$ = 0–7	Moves the contents of register R_r into the accumulator.	Fn④	1	1	1	1	1	r	r	r	1	1
MOV A, @ R_r	(A) ← ((R_r)) $_r$ = 0–1	Moves the contents of internal data memory specified by bits 0–5 in register R_r, into the accumulator.	Fn④	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Moves the contents of the Program Status Word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV R_r, # data	(R_r) ← data $_r$ = 0–7	Moves immediate data d_0-d_7 into register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV R_r, A	(R_r) ← (A) $_r$ = 0–7	Moves the contents of the accumulator into register R_r	An④	1	0	1	0	1	r	r	r	1	1
MOV @ R_r, A	((R_r)) ← (A) $_r$ = 0–1	Moves the contents of the accumulator into the data memory location specified by bits 0–5 in register R_r.	An④	1	0	1	0	0	0	0	r	1	1
MOV @ R_r, # data	((R_r)) ← data $_r$ = 0–1	Moves immediate data d_0-d_7 into the data memory location specified by bits 0–5 in register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2
MOV PSW, A	(PSW) ← (A)	Moves the contents of the accumulator into the Program Status Word.	D7	1	1	0	1	0	1	1	1	1	1

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Instruction Set (Cont.)

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
		Data Moves (Cont.)											
MOVP A, @ A	$(PC_{0-7}) \leftarrow (A)$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by PC_{8-11} concatenated with the contents of the accumulator, into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	$(PC_{0-7}) \leftarrow (A)$ $(PC_{8-11}) \leftarrow 001$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by 0011 (PC_{8-11}, page 3 of Program Memory Bank 0) and the contents of the accumulator, into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	$(A) \leftarrow ((R_r))$ $r = 0–1$	Moves the contents of the external data memory location specified by register R_r, into the accumulator.	8n④	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	$((R_r)) \leftarrow (A)$ $r = 0–1$	Moves the contents of the accumulator into the external data memory location specified by register R_r.	9n④	1	0	0	1	0	0	0	r	2	1
XCH A, R_r	$(A) \leftrightarrow (R_r)$ $r = 0–7$	Exchanges the contents of the accumulator and register R_r.	2n④	0	0	1	0	1	r	r	r	1	1
XCH A, @ R_r	$(A) \leftrightarrow ((R_r))$ $r = 0–1$	Exchanges the contents of the accumulator and the contents of the data memory location specified by bits 0–5 in register R_r.	2n④	0	0	1	0	0	0	0	r	1	1
XCHD A, @ R_r	$(A_{0-3}) \leftrightarrow ((R_{r0-3}))$ $r = 0–1$	Exchanges the contents of the lower 4 bits of the accumulator with the contents of the lower 4 bits of the internal data memory location specified by bits 0–5 in register R_r.	3n④	0	0	1	1	0	0	0	r	1	1
		Flags											
CPL C	$(C) \leftarrow \overline{(C)}$	Takes the complement of the Carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	$(F0) \leftarrow \overline{(F0)}$	Takes the complement of Flag 0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	$(F1) \leftarrow \overline{(F1)}$	Takes the complement of Flag 1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	$(C) \leftarrow 0$	Clears the Carry bit.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	$(F0) \leftarrow 0$	Clears Flag 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	$(F1) \leftarrow 0$	Clears Flag 1.	A5	1	0	1	0	0	1	0	1	1	1
		Input/Output											
ANL BUS, # data	$(BUS) \leftarrow (BUS) \wedge data$	Takes the logical AND of the contents of the bus and immediate data $d_0–d_7$, and sends the result to the bus.	98	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ANL P_p, # data	$(P_p) \leftarrow (P_p) \wedge data$ $p = 1–2$	Takes the logical AND of the contents of designated port P_p and immediate data $d_0–d_7$, and sends the result to port P_p for output.	9n⑤	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
ANLD P_p, A	$(P_p) \leftarrow (P_p) \wedge (A_{0-3})$ $p = 4–7$	Takes the logical AND of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	9n⑤	1	0	0	1	1	1	p	p	2	1
IN A, P_p	$(A) \leftarrow (P_p)$ $p = 1–2$	Loads the accumulator with the contents of designated port P_p.	0n⑤	0	0	0	0	1	0	p	p	2	1
INS A, BUS	$(A) \leftarrow (BUS)$	Loads the contents of the bus into the accumulator on the rising edge of RD.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, P_p	$(A_{0-3}) \leftarrow (P_p)$ $(A_{4-7}) \leftarrow 0$ $p = 4–7$	Moves the contents of designated port P_p to the lower 4 bits of the accumulator, and clears the upper 4 bits.	0n⑤	0	0	0	0	1	1	p	p	2	1
MOVD P_p, A	$(P_p) \leftarrow (A_{0-3})$ $p = 4–7$	Moves the lower 4 bits of the accumulator to designated port P_p. The upper 4 bits of the accumulator are not changed.	3n⑤	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	$(BUS) \leftarrow (BUS) \vee data$	Takes the logical OR of the contents of the bus and immediate data $d_0–d_7$, and sends the result to the bus.	88	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ORLD P_p, A	$(P_p) \leftarrow (P_p) \vee (A_{0-3})$ $p = 4–7$	Takes the logical OR of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	8n⑤	1	0	0	0	1	1	p	p	2	1
ORL P_p, # data	$(P_p) \leftarrow (P_p) \vee data$ $p = 1–2$	Takes the logical OR of the contents of designated port P_p and immediate data $d_0–d_7$, and sends the result to port P_p for output.	9n⑤	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
OUTL BUS, A	$(BUS) \leftarrow (A)$	Latches the contents of the accumulator onto the bus on the rising edge of $\overline{WR}$. **Note:** Never use the OUTL BUS instruction when using external program memory, as this will permanently latch the bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL P_p, A	$(P_p) \leftarrow (A)$ $p = 1–2$	Latches the contents of the accumulator into designated port P_p for output.	3n⑤	0	0	1	1	1	0	p	p	2	1
		Registers											
DEC R_r	$(R_r) \leftarrow (R_r) - 1$ $r = 0–7$	Decrements the contents of register R_r by 1.	Cn④	1	1	0	0	1	r	r	r	1	1
INC R_r	$(R_r) \leftarrow (R_r) + 1$ $r = 0–7$	Increments the contents of register R_r by 1	1n④	0	0	0	1	1	r	r	r	1	1
INC @ R_r	$((R_r)) \leftarrow ((R_r)) + 1$ $r = 0–1$	Increments by 1 the contents of the data memory location specified by bits 0–5 in register R_r.	1n④	0	0	0	1	0	0	0	r	1	1

Instruction Set (Cont.)

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
		Subroutine											
CALL addr	((SP)) ← (PC), (PSW_{4-7}) (SP) ← (SP) + 1 (PC_{8-10}) ← $addr_{8-10}$ (PC_{0-7}) ← $addr_{0-7}$ (PC_{11}) ← DBF	Stores the contents of the Program Counter and the upper 4 bits of the PSW in the address indicated by the Stack Pointer, and increments the contents of the Stack Pointer, calling the subroutine specified by address a_0–a_{10} and the DBF.	x4⑥	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the location specified by the Stack Pointer, executing a return from subroutine without restoring the PSW.	83	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) − 1 (PC) ← ((SP)) (PSW_{4-7}) ← ((SP))	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the upper 4 bits of the PSW and the contents of the location specified by the Stack Pointer, executing a return from subroutine with restoration of the PSW.	93	1	0	0	1	0	0	1	1	2	1
		Timer/Counter											
EN TCNTI		Enables internal interrupt of timer/event counter. If an overflow condition occurs, then an interrupt will be generated.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disables internal interrupt of timer/event counter.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Moves the contents of the timer/counter into the accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Moves the contents of the accumulator into the timer/counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stops the operation of the timer/event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Starts the event counter operation of the timer/counter when T1 changes from a low-level input to a high-level input.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Starts the timer operation of the timer/counter. The timer is incremented every 32 machine cycles.	55	0	1	0	1	0	1	0	1	1	1
		Miscellaneous											
NOP		Uses one machine cycle without performing any operation.	00	0	0	0	0	0	0	0	0	1	1

Notes: ① Binary instruction code designations $_1$ and $_2$ represent encoded values or the lowest-order bit value of specified registers and ports, respectively

② Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the Auxiliary Carry Flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions

③ References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction

④ The hex value of n for specific registers is as follows

a) Direct addressing
R_0 n = 8 R_2 n = A R_4 n = C R_6 n = E
R_1 n = 9 R_3 n = B R_5 n = D R_7 n = F

b) Indirect addressing
@R_0 n = 0 @R_1 n = 1

⑤ The hex value of n for specific ports is as follows
P_1 n = 9 P_4 n = C P_6 n = E
P_2 n = A P_5 n = D P_7 n = F

⑥ The hex value of x for specific accumulator or address bits is as follows

a) JBb instruction
B_0 x = 1 B_2 x = 5 B_4 x = 9 B_6 x = D
B_1 x = 3 B_3 x = 7 B_5 x = B B_7 x = F

b) JMP instruction
Page 0 x = 0 Page 2 x = 4 Page 4 x = 8 Page 6 x = C
Page 1 x = 2 Page 3 x = 6 Page 5 x = A Page 7 x = E

c) CALL instruction
Page 0 x = 1 Page 2 x = 5 Page 4 x = 9 Page 6 x = D
Page 1 x = 3 Page 3 x = 7 Page 5 x = B Page 7 x = F

DC Characteristics: Standard Voltage Range

$T_a = -40°C$ to $+85°C$; $V_{CC} = +5V \pm 10\%$; $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input High Voltage	V_{IH}	$V_{CC}-2$		V_{CC}	V	All except XTAL1, XTAL2, $\overline{RESET}$
	V_{IH1}	$V_{CC}-1$		V_{CC}	V	$\overline{RESET}$, XTAL1, XTAL2
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.0mA$
Output High Voltage	V_{OH}	2.4			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100\mu A$
	V_{OH1}①	2.4			V	Port 1, Port 2; $I_{OH} = -5\mu A$ (Type 0)
						Port 1, Port 2; $I_{OH} = -50\mu A$ (Type 1)
	V_{OH2}	$V_{CC}-0.5$			V	All outputs; $I_{OH} = -0.2\mu A$
Input Current	I_{ILP}①		−15	−40	μA	Port 1, Port 2; $V_{IN} \le V_{IL}$ (Type 0)
				−500	μA	Port 1 Port 2; $V_{IN} \le V_{IL}$ (Type 1)
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \le V_{IL}$
Input Leakage Current	I_{LI1}			±1	μA	T1, $\overline{INT}$, V_{DD}; $V_{SS} \le V_{IN} \le V_{CC}$
	I_{LI2}			±3	μA	EA; $V_{SS} \le V_{IN} \le V_{CC}$
Output Leakage Current	I_{LO}			±1	μA	Bus, T0, High-Impedance State; $V_{SS} \le V_O \le V_{CC}$
Standby Current	I_{CC1}		0.4	0.8	mA	Halt mode; $t_{CY} = 2.5\mu s$
	I_{CC2}		1	20	μA	Stop mode②
Supply Current	I_{CC}		4	8	mA	$t_{CY} = 2.5\mu s$
Data Retention Voltage	V_{CCDR}	2.0			V	Stop mode (V_{DD}, $\overline{RESET} \le 0.4V$)

DC Characteristics: Extended Voltage Range

$T_a = -40°C$ to $+85°C$; $V_{CC} = +2.5V$ to $+5.5V$; $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.3		$0.18V_{CC}$	V	
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH}	$0.7V_{CC}$		V_{CC}	V	
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}	$0.8V_{CC}$		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 1.0mA$
Output High Voltage (Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0	V_{OH}	$0.75V_{CC}$			V	$I_{OH} = -100\mu A$
Output High Voltage (All Other Outputs	V_{OH1}	$0.7V_{CC}$			V	Port 1, Port 2; $I_{OH} = -1\mu A$ (Type 0)
						Port 1, Port 2; $I_{OH} = -10\mu A$ (Type 1)
Output High Voltage (All Outputs)	V_{OH2}	$V_{CC} - 0.5$			V	$I_{OH} = -0.2\mu A$
Input Leakage Current (Port 1, Port 2)	I_{ILP}		−15	−40	μA	$V_{IN} \le V_{IL}$ (Type 0)
				−500	μA	$V_{IN} \le V_{IL}$ (Type 1)
Input Leakage Current ($\overline{SS}$, $\overline{RESET}$)	I_{ILC}			−40	μA	$V_{IN} \le V_{IL}$
Input Leakage Current (T1, $\overline{INT}$)	I_{IL1}			±1	μA	$V_{SS} < V_{IN} < V_{CC}$
Input Leakage Current (EA)	I_{IL2}			±3	μA	$V_{SS} < V_{IN} < V_{CC}$
Output Leakage Current (Bus, T0 — High Impedance State)	I_{OL}			±1	μA	$V_{SS} < V_O < V_{CC}$
Supply Current	I_{CC}		0.8	1.6	mA	$V_{CC} = 3V$, $t_{CY} = 10\mu s$
Halt Mode Standby Current	I_{CC1}		100	200	μA	$V_{CC} = 3V$, $t_{CY} = 10\mu s$
Stop Mode Standby Current	I_{CC2}		1	20	μA	

Notes: ① Type 0 and type 1 options apply only to the μPD80C48, the μPD80C35 is type 1 only
② Input Pin Voltage is V_{IN}, V_{IL}, or V_{IN}, V_{IH}

AC Characteristics

Read, Write and Instruction Fetch: External Data and Program Memory

$T_a = -40°C$ to $+85°C$; $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

Parameter	Symbol	$V_{CC} = +5V \pm 10\%$ Min	Typ	Max	$V_{CC} = +2.5V$ to $+5.5V$ Min	Typ	Max	Unit	Test Conditions
ALE Pulse Width	t_{LL}	400			2160			ns	
Address Setup before ALE	t_{AL}	120			1620			ns	
Address Hold from ALE	t_{LA}	80			330			ns	①
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	700			3700			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			3500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			370			ns	②
Cycle Time	t_{CY}	2.5		150	10		150	μs	6MHz XTAL
Data Hold	t_{DR}	0		200	0		950	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500			2750	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			3230			ns	①
Address Setup before Data In	t_{AD}			950			5450	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			500			ns	
Control Pulse to ALE	t_{CA}	10			10			ns	

Port 2 Timing
$T_a = -40°C$ to $+85°C$; $V_{CC} = +5V \pm 10\%$

Parameter	Symbol	$V_{CC} = +5V \pm 10\%$ Min	Typ	Max	$V_{CC} = +2.5V$ to $+5.5V$ Min	Typ	Max	Unit	Test Conditions
Port Control Setup before Falling Edge of PROG	t_{CP}	110			860			ns	
Port Control Hold after Falling Edge of PROG	t_{PC}	0		80	0		200	ns	④
PROG to Time P2 Input must be Valid	t_{PR}			810			5310	ns	
Output Data Setup Time	t_{DP}	250			3250			ns	③
Output Data Hold Time	t_{PD}	65			820			ns	
Input Data Hold Time	t_{PF}	0		150	0		900	ns	
PROG Pulse Width	t_{PP}	1200			6450			ns	
Port 2 I/O Data Setup	t_{PL}	350			2100			ns	
Port 2 I/O Data Hold	t_{LP}	150			1400			ns	

Notes: ① For Control Outputs C_L = 80pF, for Bus Outputs C_L = 150pF
② C_L = 20pF
③ For Control Outputs C_L = 80pF
④ Refer to the operating characteristic curves for Supply Voltage and Port Control Hold

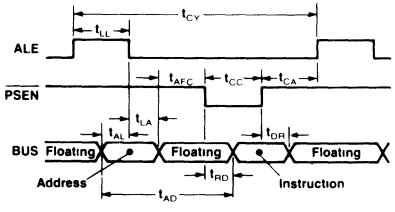
BUS Timing Requirements

Symbol	Timing Formula	Min	Max	Unit
t_{LL}	(7/30) T − 170	•		ns
t_{AL}	(1/5) T − 380	•		ns
t_{LA}	(1/30) T	•		ns
t_{CC}	(2/5) T − 300	•		ns
t_{DW}	(2/5) T − 500	•		ns
t_{WD}	(1/30) T + 40	•		ns
t_{DR}	(1/10) T − 50		•	ns
t_{RD}	(3/10) T − 250		•	ns
t_{AW}	(2/5) T − 770	•		ns
t_{AD}	(3/5) T − 550		•	ns
t_{AFC}	(1/15) T − 165	•		ns
t_{CP}	(1/10) T − 140	•		ns
t_{PR}	(3/5) T − 690		•	ns
t_{PF}	(1/10) T − 100		•	ns
t_{DP}	(2/5) T − 750	•		ns
t_{PD}	(1/10) T − 180	•		ns
t_{PP}	(7/10) T − 550	•		ns
t_{PL}	(7/30) T − 230	•		ns
t_{LP}	(1/6) T − 265	•		ns

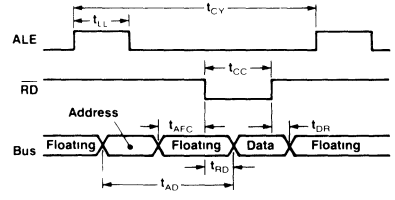
Notes: T = t_{CY}
Unlisted parameters are not affected by cycle time

Timing Waveforms

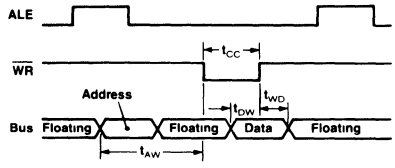
Instruction Fetch From External Memory



Read From External Data Memory

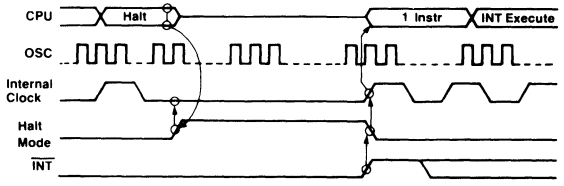


Write to External Memory

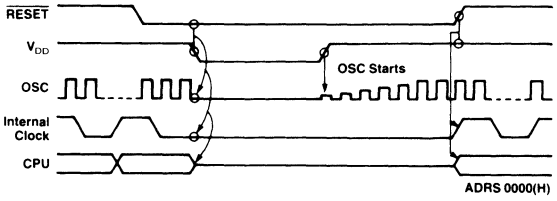


Low Power Standby Operation

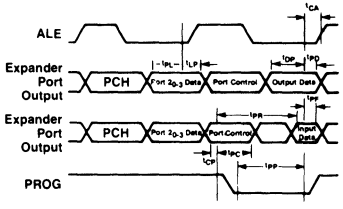
1) Halt Mode (When EI)



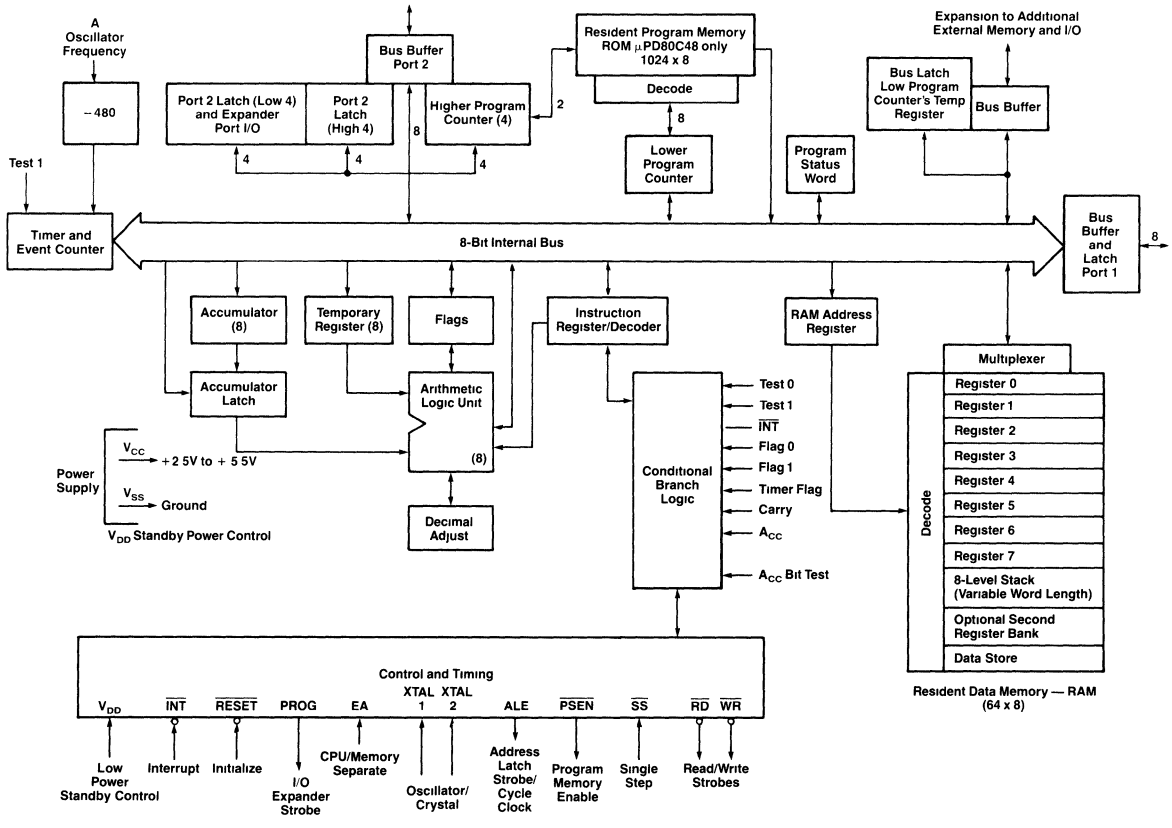
2) Stop Mode



Port 2 Timing



Block Diagram



Note: μPD80C35 does not include ROM

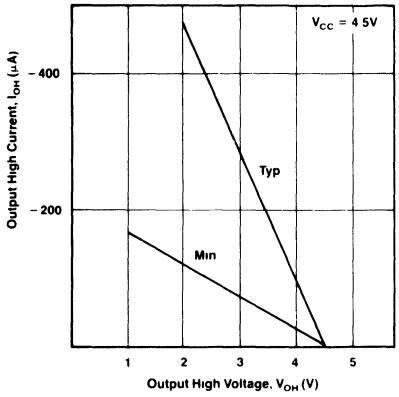
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Cerdip Package), T_{stg}	−65°C to +150°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +125°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage, V_{CC}	V_{SS} −0.3 to +10V
Power Dissipation, P_D	0.35w

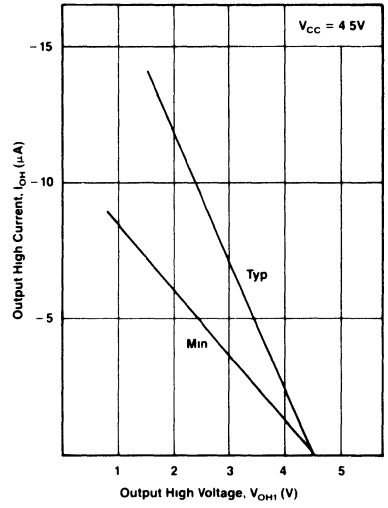
*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Characteristic Curves

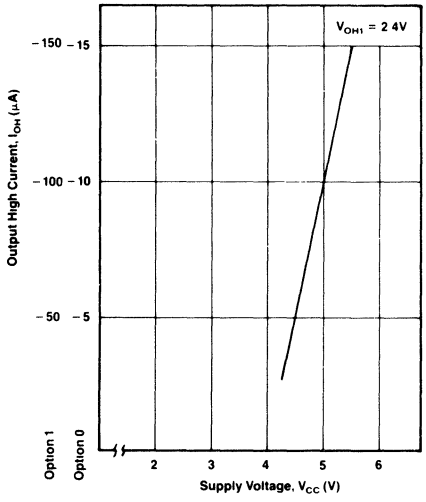
Output High Current vs. Output High Voltage



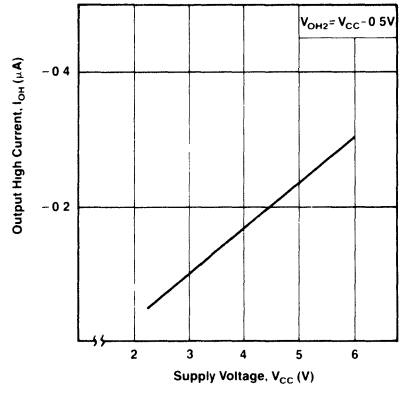
Output High Current vs. Output High Voltage



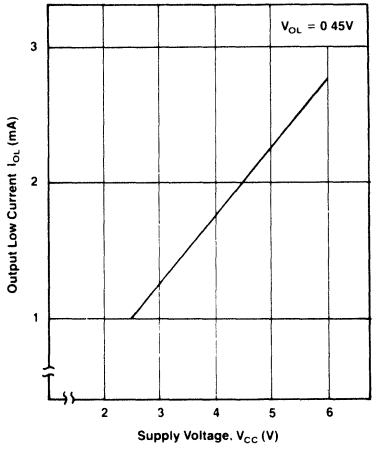
Output High Current vs. Supply Voltage



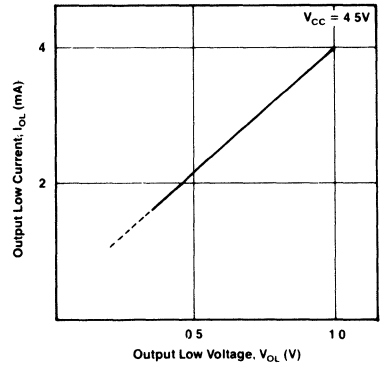
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage



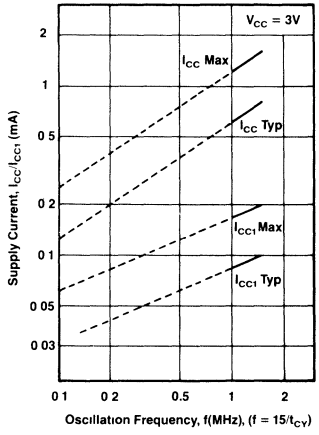
Output Low Current vs. Output Low Voltage



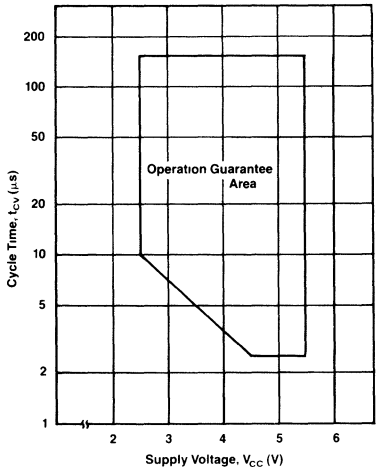
4

Operating Characteristic Curves (Cont.)

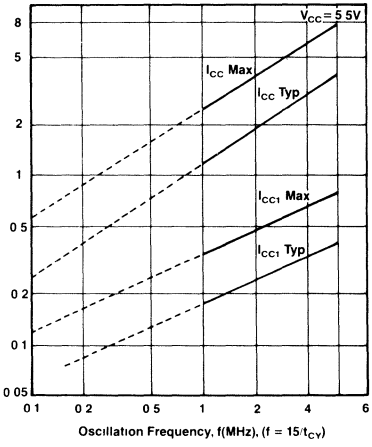
Supply Current vs. Oscillation Frequency



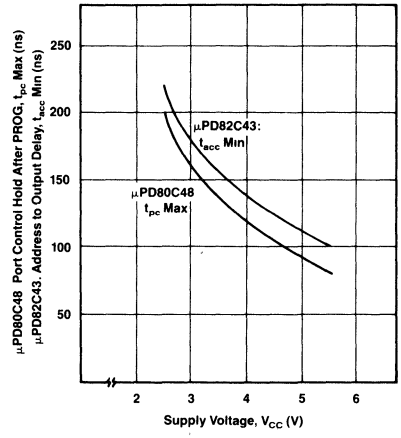
Cycle Time vs. Supply Voltage



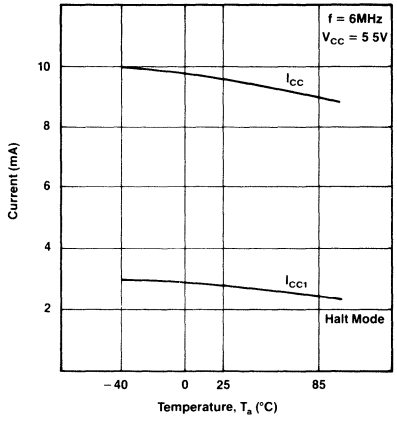
Supply Current vs. Oscillation Frequency ①



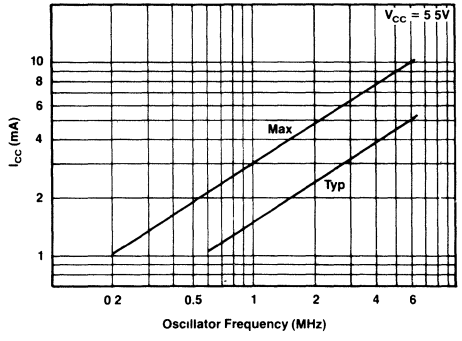
Port Control Hold After PROG, t_{pc} Max (μPD80C48), and Address to Output Delay, t_{acc} Min (μPD82C43), vs. Supply Voltage



Current Consumption as a Function of Temperature — Normal Operating Mode



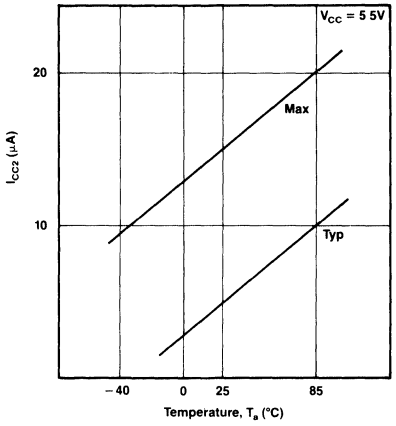
Current Consumption as a Function of Operating Frequency — Normal Operating Mode



Note: ① External oscillation is assumed for frequency less than 1MHz
Internal oscillation requires more power

Operating Characteristic Curves (Cont.)

Current Consumption as a Function of Temperature — Stop Mode



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8048HC/35HLC
Ceramic, μPD8048HD/35HLD
Plastic Shrinkdip, μPD80C48C
Plastic Miniflat, μPD80C48G/C35G

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μPD8049H/μPD8749H/μPD8039HL
HIGH PERFORMANCE SINGLE CHIP 8-BIT MICROCOMPUTERS

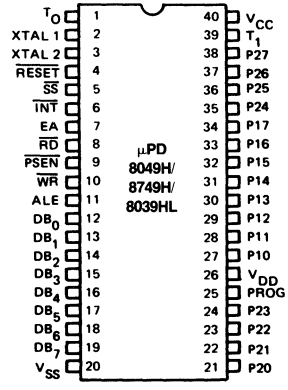
Description

The NEC μPD8049H, μPD8749H and μPD8039HL are single chip 8-bit microcomputers. The processors differ only in their internal program memory options: the μPD8049 has 2K x 8 bytes of mask ROM, the μPD8749 has 2K x 8 of UV erasable EPROM and the μPD8039HL has external program memory.

Features

- ☐ High performance 11 MHz operation
- ☐ Fully compatible with industry standard 8049/8749/8039
- ☐ Pin compatible with the μPD8048/8748/8035
- ☐ HMOS silicon gate technology requiring a single +5V ±10% supply
- ☐ 1.36 μs cycle time. All instructions 1 or 2 bytes
- ☐ Programmable interval timer/event counter
- ☐ 2K x 8 bytes of ROM, 128 x 8 bytes of RAM
- ☐ External and internal interrupts
- ☐ 96 instructions: 70 percent single byte
- ☐ 27 I/O lines
- ☐ Internal clock generator
- ☐ Expandable with 8080A/8085A peripherals
- ☐ Available in both ceramic and plastic 40-pin packages

Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Function
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal, LC, or external frequency source. (Non-TTL compatible V_{IH})
3	XTAL 2	The other side of the crystal or LC frequency source. For external sources, XTAL 2 must be driven with the logical complement of the XTAL 1 input.
4	RESET	Active low input from processor initialization. $\overline{\text{RESET}}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).
5	SS	Single Step input (active-low). $\overline{\text{SS}}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	INT	Interrupt input (active-low). $\overline{\text{INT}}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{\text{INT}}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	RD	READ strobe outputs (active-low). $\overline{\text{RD}}$ will pulse low when the processor performs a BUS READ. $\overline{\text{RD}}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	PSEN	Program Store Enable output (active-low). $\overline{\text{PSEN}}$ becomes active only during an external memory fetch.
10	WR	WRITE strobe output (active-low). $\overline{\text{WR}}$ will pulse low when the processor performs a BUS WRITE. $\overline{\text{WR}}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12-19	D_0–D_7 BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. The contents of the D_0–D_7 BUS can be latched in a static mode. During an external memory fetch, the D_0–D_7 BUS holds the least significant bits of the program counter. $\overline{\text{PSEN}}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the D_0–D_7 BUS, controlled by ALE, $\overline{\text{RD}}$ and $\overline{\text{WR}}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21-24, 35-38	P_{20}–P_{27}: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in P_{20}–P_{23}. Bits P_{20}–P_{23} are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is used as an output strobe for μPD8243s during I/O expansion. When the μPD8049H is used in a stand-alone mode the PROG pan can be allowed to float.
26	V_{DD}	V_{DD} is used to provide +5V to the 128 x 8-bit RAM section During normal operation V_{CC} must also be +5V to provide power to the other functions in the device. During stand-by operation V_{DD} must remain at +5V while V_{CC} is at ground potential.
27-34	P_{10}–P_{17}: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V during normal operation

4

Functional Description

The NEC μPD8049H, μPD8749H and the μPD8039HL are high performance, single component, 8-bit parallel microcomputers using H-channel silicon gate MOS technology. The μPD8049H family functions efficiently in control as well as arithmetic applications. The powerful instruction set eases bit handling applications and provides facilities for binary and BCD arithmetic. Standard logic functions implementation is facilitated by the large variety of branch and table look-up instructions.

The instruction set is comprised of 1 and 2 byte instructions, most of which are single-byte. The instruction set requires only 1 or 2 cycles per instruction with over 50 percent of the instructions single-cycle.

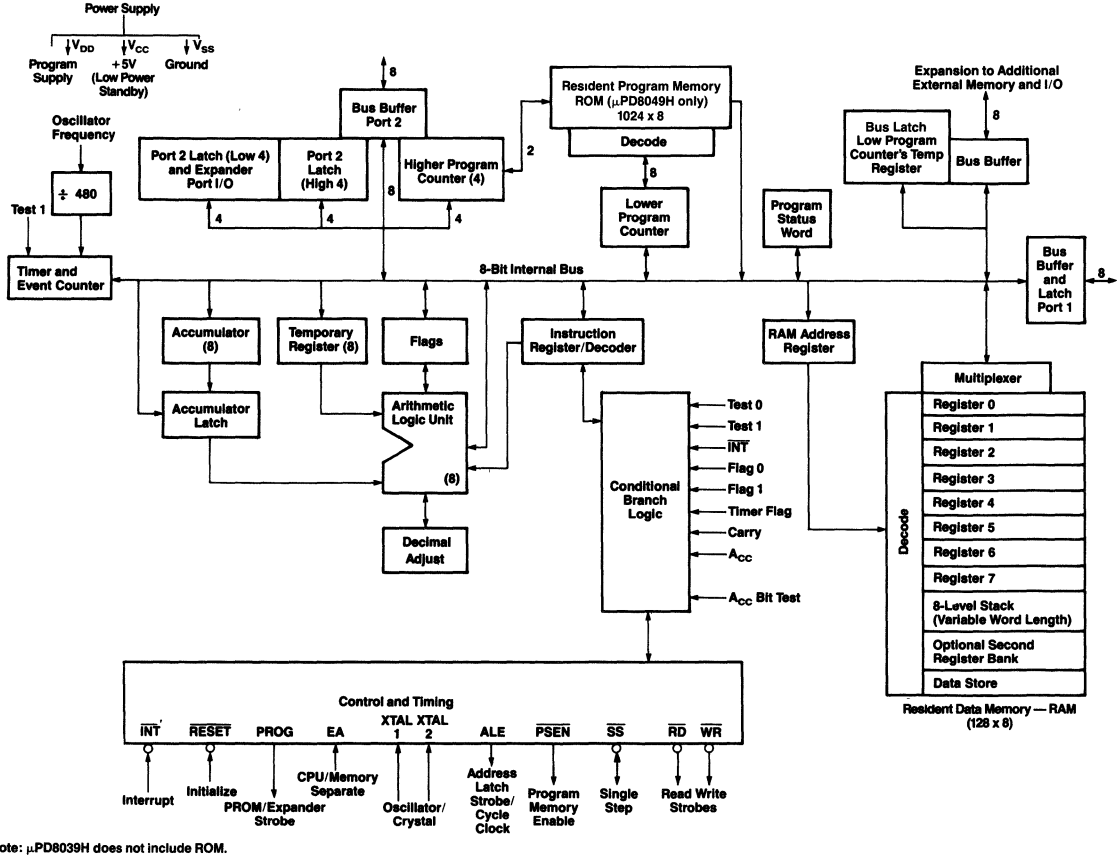
The μPD8049H family of microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8049H contains the following functions usually found in external peripheral devices: 2048 x 8 bits of mask ROM program memory; 128 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry.

The μPD8749H differs from the μPD8049H in its 2048 x 8-bit UV erasable EPROM program memory instead of the mask ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8039HL is intended for applications using external program memory only. It contains all the features of the μPD8049H except for the internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

Block Diagram



Note: μPD8039H does not include ROM.

Absolute Maximum Ratings*

T_a = 25°C

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V①
Power Dissipation	1.5 W

Note: ① With respect to ground.

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	−0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, RESET)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	3.8		V_{CC}	V	
Output Low Voltage (BUS, RD, WR, PSEN, ALE)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage (BUS)	V_{OH}	2.4			V	I_{OH} = −400μA
Output High Voltage (RD, WR, PSEN, ALE)	V_{OH1}	2.4			V	I_{OH} = −400μA
Output High Voltage (All Other Outputs)	V_{OH2}	2.4			V	I_{OH} = −40μA
Input Leakage Current (T_1, EA, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Leakage Current P10-17, P20-27, EA, SS	I_{IL1}			−500	μA	V_{SS} + .45 ≤ $V_{IN} \leq V_{CC}$
Output Leakage Current (BUS, T_0 — High Impedance State)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Power Down Supply Current	I_{DD}		5	10	mA	T_a = 25°C
Total Supply Current	I_{DD} + I_{CC}		80	110	mA	T_a = 25°C

DC Characteristics for Programming

T_a = 25° C ± 5°C; V_{CC} = +5V ± 5%; V_{DD} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
V_{DD} Program Voltage High Level	V_{DDH}	20.5		21.5	V	
V_{DD} Voltage Low Level	V_{DDL}	4.75		5.25	V	
PROG Program Voltage High Level	V_{PH}	17.5		18.5	V	
PROG Voltage Low Level	V_{PL}			4.0	V	
EA Program or Verify Voltage High Level	V_{EAH}	17.5		18.5	V	
V_{DD} High Voltage Supply Current	I_{DD}			20.0	mA	
PROG High Voltage Supply Current	I_{PROG}			1.0	mA	
EA High Voltage Supply Current	I_{EA}			1.0	mA	

AC Characteristics

T_a = 0°C to +70°C, V_{CC} = V_{DD} = 5V ± 10%, V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	f(t_{CY}) and Test Conditions
ALE Pulse Width	t_{LL}	150			ns	7/30 t_{CY} − 170
Addr Setup to ALE	t_{AL}	70			ns	2/15 t_{CY} − 110
Addr Hold from ALE	t_{LA}	50			ns	1/15 t_{CY} − 40
Control Pulse Width (RD, WR)	t_{CC1}	480			ns	1/2 t_{CY} − 200
Control Pulse Width (PSEN)	t_{CC2}	350			ns	2/5 t_{CY} − 200
Data Setup before WR	t_{DW}	390			ns	13/30 t_{CY} − 200
Data Hold after WR	t_{WD}	40			ns	1/15 t_{CY} − 50 ②
Data Hold (RD, PSEN)	t_{DR}	0		110	ns	1/10 t_{CY} − 30
RD to Data In	t_{RD1}			350	ns	2/5 t_{CY} − 200
PSEN to Data In	t_{RD2}			210	ns	3/10 t_{CY} − 200
Addr Setup to WR	t_{AW}	300			ns	1/3 t_{CY} − 150
Addr Setup to Data (RD)	t_{AD1}			750	ns	11/15 t_{CY} − 250
Addr Setup to Data (PSEN)	t_{AD2}			480	ns	8/15 t_{CY} − 250
Addr Float to RD, WR	t_{AFC1}	140			ns	2/15 t_{CY} − 40
Addr Float to PSEN	t_{AFC2}	10			ns	1/30 t_{CY} − 40
ALE to Control (RD, WR)	t_{LAFC1}	200			ns	1/5 t_{CY} − 75
ALE to Control (PSEN)	t_{LAFC2}	50			ns	1/10 t_{CY} − 75
Control to ALE (RD, WR, PROG)	t_{CA1}	50			ns	1/15 t_{CY} − 40
Control to ALE (PSEN)	t_{CA2}	320			ns	4/15 t_{CY} − 40
Port Control Setup to PROG	t_{CP}	100			ns	1/10 t_{CY} − 40
Port Control Hold to PROG	t_{PC}	160			ns	4/15 t_{CY} − 200
PROG to P2 Input Valid	t_{PR}			550	ns	17/30 t_{CY} − 120
Input Data Hold from PROG	t_{PF}	0		140	ns	1/10 t_{CY}
Output Data Setup	t_{DP}	400			ns	2/5 t_{CY} − 150
Output Data Hold	t_{PD}	90			ns	1/10 t_{CY} − 50
PROG Pulse Width	t_{PP}	700			ns	7/10 t_{CY} − 250
Port 2 I/O Setup to ALE	t_{PL}	180			ns	4/15 t_{CY} − 200
Port 2 I/O Hold to ALE	t_{LP}	40			ns	1/10 t_{CY} − 100
Port Output from ALE	t_{PV}			510	ns	3/10 t_{CY} − 100
Cycle Time	t_{CY}	1.36			μs	11 MHz
I/O Rep Rate	t_{OPRR}	270			ns	3/15 t_{CY}

Notes: ① Control Outputs CL = 60pF
BUS Outputs CL = 150pF
② BUS High Impedance Load 20pF
③ Calculated values will be equal to or better than published 8049 values.

AC Characteristics for Programming

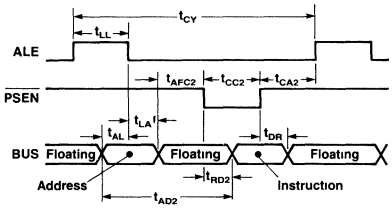
T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{DD} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time to RESET ↑	t_{AW}	4t_{CY}				
Address Hold Time After RESET ↑	t_{WA}	4t_{CY}				
Data in Setup Time to PROG ↑	t_{DW}	4t_{CY}				
Data in Hold Time After PROG ↓	t_{WD}	4t_{CY}				
RESET Hold Time to Verify	t_{PH}	4t_{CY}				
V_{DD}	t_{VDDW}	0		1.0	ms	
V_{DD} Hold Time After PROG ↓	t_{VDDH}	0		1.0	ms	
Program Pulse Width	t_{PW}	50		60	ms	
Test 0 Setup Time for Program Mode	t_{TW}	4t_{CY}				
Test 0 Hold Time After Program Mode	t_{WT}	4t_{CY}				
Test 0 to Data Out Delay	t_{DO}			4t_{CY}		
RESET Pulse Width to Latch Address	t_{WW}	4t_{CY}				
V_{DD} and PROG Rise and Fall Times	t_r, t_f	0.5		100	μs	
CPU Operation Cycle Time	t_{CY}	4.0		15	μs	
RESET Setup Time before EA ↑	t_{RE}	4t_{CY}				

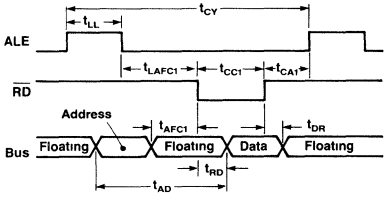
Notes: ① Control Outputs CL = 60pF
BUS Outputs CL = 150pF
② BUS High Impedance Load 20pF
③ Calculated values will be equal to or better than published 8049 values.

Timing Waveforms

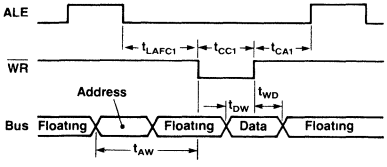
Instruction Fetch from External Memory



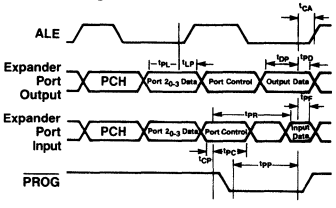
Read from External Data Memory



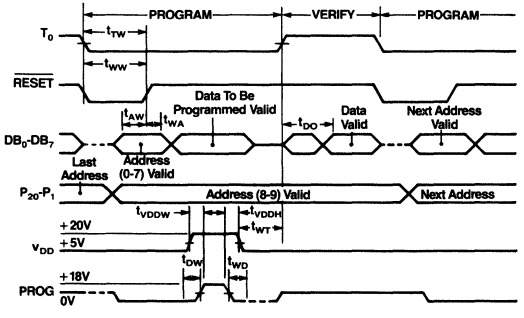
Write to External Memory



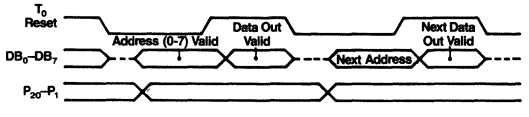
Port 2 Timing



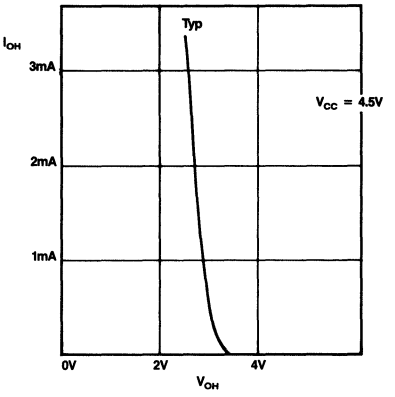
Waveforms for Programming the μPD8749H



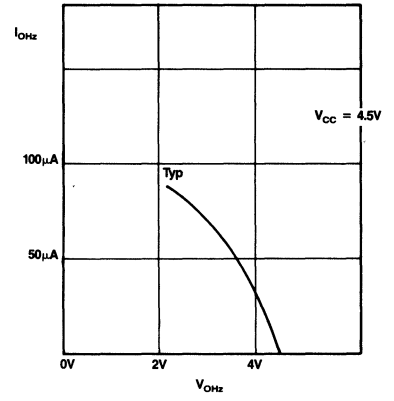
Program/Verify Timing (ROM/EPROM)



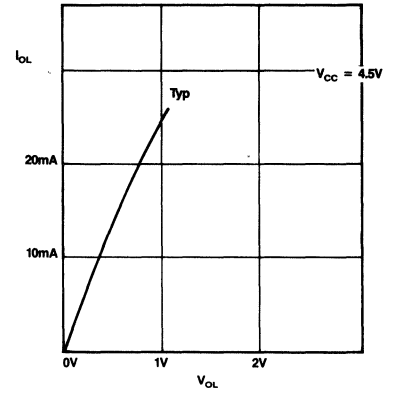
BUS Output Low Voltage vs. Sink Current



Port P1 & P2 Output High Voltage vs. Source Current



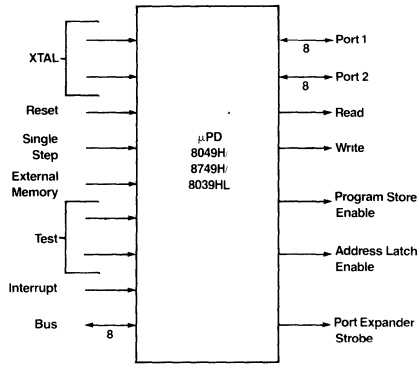
BUS Output High Voltage vs. Source Current



Symbol Definitions

Symbol	Description
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number of Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

Logic Symbol



4

Instruction Set

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator																
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
Add A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents of the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	DECREMENT by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ← (A_0 – 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 if (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (Cont.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 - 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 - 4095) of Program Memory	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 - 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 - 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, = data	(A) ← data	Move immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 – 7	Move immediate the specified data into the designated register	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 – 1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)(0 – 3)); r = 0 – 1	Exchange indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement content of Flag F0	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement content of Flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

Instruction Set (Cont.)

Mnemonic	Function	Description	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Input/Output																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, = data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, = data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A ⑤	(BUS) ← (A)	Output contents of Accumulator onto BUS	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
Registers																
DEC Rr, (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0 – 7	Increment by 1 contents of designated register	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
Timer/Counter																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected
⑤ When the Bus is written to, with an OUTL instruction, the Bus remains an Output Port until either device is reset or a MOVX instruction is executed

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8049HC/39HLC
Ceramic, μPD8049HD/39HLD
Cerdip, μPD8749HD, has quartz window

Description

The NEC μPD80C49 is a true stand-alone 8-bit microcomputer fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 2K-byte ROM, a 128-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C49 can be expanded using peripherals and memory compatible with industry-standard 8080A/8085A processors. A version of the μPD80C48 without ROM is offered by the μPD80C39.

Providing compatibility with industry-standard 8049, 8749, and 8039 processors, the μPD80C49 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C49 is distinct in offering two standby modes (Halt mode and Stop mode) to further minimize power drain.

Features

- ☐ 8-bit CPU with ROM, RAM, and I/O on a single chip
- ☐ Hardware/software-compatible with industry-standard 8049, 8749, and 8039 processors
- ☐ 2K x 8 ROM
- ☐ 128 x 8 RAM
- ☐ 27 I/O lines
- ☐ 1.875μs cycle time (8MHz crystal)
- ☐ All instructions executable in 1 or 2 cycles
- ☐ 97 instructions: 70 percent are single-byte instructions
- ☐ Internal timer/event counter
- ☐ 2 interrupts (an external interrupt and a timer interrupt)
- ☐ Easily expandable memory and I/O
- ☐ Bus compatible with 8080A/8085A peripherals
- ☐ Power-efficient CMOS technology requiring a single +2.5V to +6V power supply
- ☐ Available in 40-pin DIP, 44-pin flat pack (80C49 only), and 52-pin flat pack
- ☐ Halt mode
  - 1mA typical supply current
  - Maintenance of internal logic values and control states
  - Mode initialization via HALT instruction
  - Mode release via external interrupt or reset
- ☐ Stop mode
  - 1μA typical supply current
  - Disabling of internal clock generation and internal logic
  - Maintenance of RAM contents
  - Mode initialization via hardware (V_{DD})
  - Mode release via reset

Pin Identification

Pin No.	Symbol	Name	Function
1	T0	Test 0	Testable input using conditional jump instructions JT0 and JNT0. Also enables clock output via the ENTO CLK instruction.
2	XTAL1	Crystal 1	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals. May also be used as an input for external clock signals (Non-TTL-compatible V_{IH}.)
3	XTAL2	Crystal 2	One of two inputs for external crystal oscillator or LC circuit to generate internal clock signals (Non-TTL-compatible V_{IH})
4	$\overline{RESET}$	Reset	Active-low input line that initializes the processor. Also used to release both the Halt and Stop modes.①
5	$\overline{SS}$	Single Step	Active-low input line, that, in conjunction with ALE, causes the processor to single-step through a program one instruction at a time
6	$\overline{INT}$	Interrupt	Active-low input line that causes an interrupt if an enable instruction has been executed. A reset disables the interrupt. May be used as a testable input with a conditional jump instruction. Can also be used to release the Halt mode
7	EA	External Access	Input line that inhibits internal program memory fetches and initiates access of external program memory. Essential for system testing and may also be used for program debugging.
8	$\overline{RD}$	Read	Active-low output strobe line that is used to read data from external data memory
9	$\overline{PSEN}$	Program Store Enable	Active-low output line that is used to fetch instructions from external program memory
10	$\overline{WR}$	Write	Active-low output strobe line that is used to write data into external data memory.
11	ALE	Address Latch Enable	Output line for address latch enable. At the falling edge of ALE, the address of either external data memory or external program memory is available on the bus.
12–19	DB_0–DB_7	Bus	These I/O lines constitute an 8-bit bidirectional data/address bus. Synchronous read and write operations can be performed on this bus using $\overline{RD}$ and $\overline{WR}$ signals. Data driven out on the bus by an OUTL BUS instruction is statically latched. The address of external memory is available on the bus at the falling edge of ALE when reading from external program memory or writing to and reading from external data memory. During external program memory fetches, the least-significant 8 bits of the external program memory address are driven out on the bus and the addressed instruction is fetched using $\overline{PSEN}$. When no external memory is used, the bus can serve as a true bidirectional 8-bit port. Information is strobed in or out by the $\overline{RD}$ and $\overline{WR}$ signals.
20	V_{SS}	Ground	Ground potential.
21–24, 35–38	P_{20}–P_{27}	Port 2	These lines constitute Port 2, an 8-bit quasi-bidirectional port. During external program memory fetches, P_{20}–P_{23} output the most-signficant 4 bits of the external program memory address. Lines P_{20}–P_{23} can also be used as a 4-bit I/O expander bus to interface with the optional μPD82C43 I/O expander
25	PROG	Program Pulse	This line is used as an output strobe when interfacing with the optional μPD82C43 I/O expander.
26	V_{DD}	Oscillator Control Voltage Line	This input line is used to control oscillator stopping and restarting in Stop mode. Stop mode is enabled by forcing V_{DD} LOW during a reset.
27–34	P_{10}–P_{17}	Port 1	These lines constitute Port 1, an 8-bit, general-purpose quasi-bidirectional port.
39	T1	Test 1	Testable input using conditional jump instructions JT1 and JNT1. Can also be used as the timer/counter input line via the STRT CNT instruction.
40	V_{CC}	Primary Power Supply	Power supply. V_{CC} must be between +2.5V to +6V for normal operation. In Stop mode, V_{CC} must be at least +2V to ensure data retention.

Note: ① The pulse width of $\overline{RESET}$ must be a minimum of 5 machine cycles in length following oscillator stabilization to reinitialize the processor and stabilize CPU operation. At power-up, the states of the output lines are undefined until completion of reset

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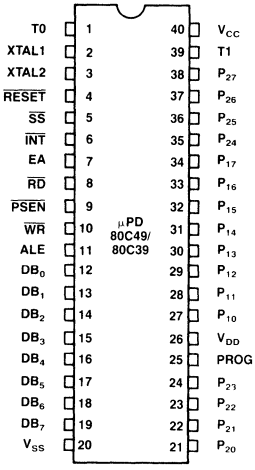
Pin Configuration



Standby Function

HALT mode

In Halt mode, the oscillator continues to operate, but the internal clock is disabled. The status of all internal logic just prior to execution of the HALT instruction is maintained by the CPU. In Halt mode, power consumption is less than 10 percent of normal μPD80C49 operation and less than 1 percent of normal 8049 operation.

The Halt mode is initiated by execution of the HALT instruction, and is released by either INT or RESET input.

INT input: When the INT pin receives a low-level input, if interrupts are enabled, the internal clock is restarted and the interrupt is executed after the first or second instruction following the HALT instruction. However, if interrupts are disabled, program operation is resumed from the next address following the HALT instruction. The first instruction following a HALT instruction should be a NOP instruction to ensure proper program execution.

If the Halt mode is released when interrupts are enabled, the interrupt service routine is usually executed after the first or second instruction following the release of Halt mode. However, if either a timer or external interrupt is accepted within one machine cycle prior to a HALT instruction, the corresponding timer or external interrupt service routine is executed immediately following the release of Halt mode. It is important to note this sequence of execution when considering interrupt service routine execution following a HALT instruction.

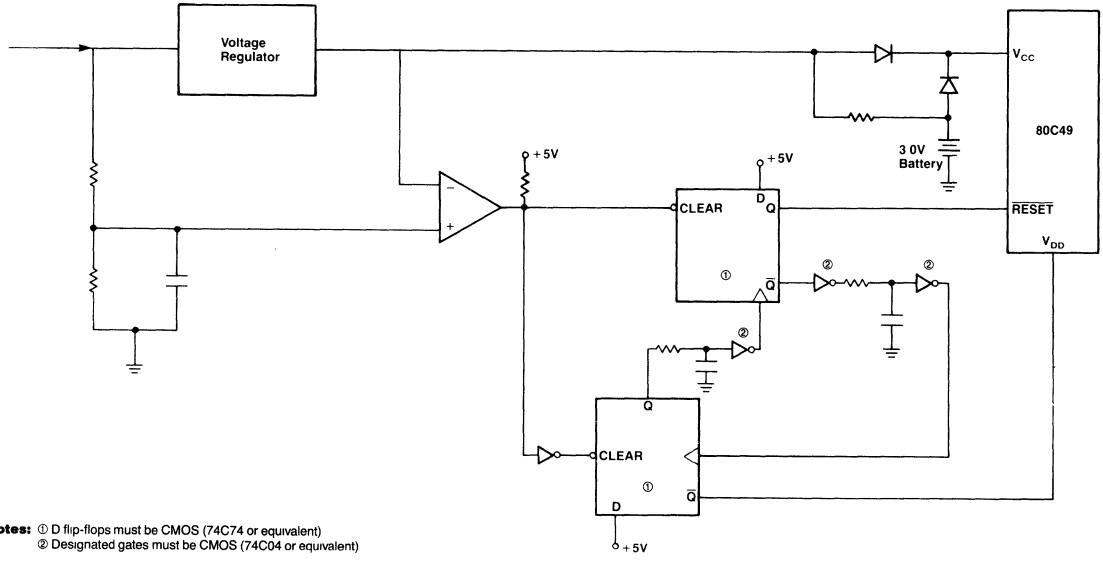
RESET input: When a low-level input is received by the RESET pin, Halt mode is released and the normal reset operation is activated, restarting program operation from address 0.

Stop mode

In Stop mode, the oscillator is deactivated and only the contents of RAM are maintained. The operation status of the μPD80C49 resembles that of a reset condition. Because only the contents of RAM are maintained, Stop mode provides even lower power consumption than Halt mode, only requiring a minimum V_{CC} as low as +2V.

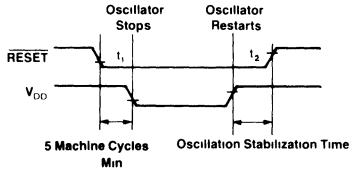
Stop mode is initiated by setting V_{DD} to LOW when RESET is LOW, to protect the contents of RAM. Stop mode is released by first raising the supply voltage at the V_{CC} pin from standby level to correct operating level and setting V_{DD} to HIGH when RESET is LOW. After the oscillator has been restarted and the oscillation has stabilized, RESET must be set to HIGH, whereby program operation is started from address 0.

Stop Mode Circuit



Notes: ① D flip-flops must be CMOS (74C74 or equivalent)
② Designated gates must be CMOS (74C04 or equivalent)

Stop Mode Timing

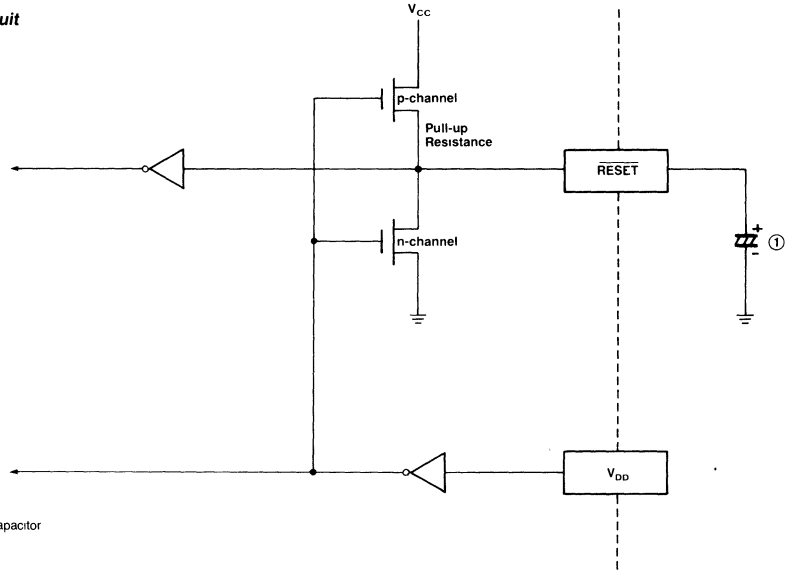


Stop Mode Circuit: Since V_{DD} controls the restarting of the oscillator, it is important that V_{DD} be protected from noise interference. The time required to reset the CPU is represented by t_1 (see Stop Mode Timing diagram), which is a minimum of 5 machine cycles. The reset operation will not be completed in less than 5 machine cycles. In Stop mode, it is important to note that if V_{DD} goes LOW before 5 machine cycles have elapsed, the CPU will be deactivated and the output of ALE, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, and PROG will not have been stabilized.

Oscillation stabilization time is represented by t_2 (see Stop Mode Timing diagram). When V_{DD} goes HIGH, oscillator operation is reactivated, but it takes time before oscillation can be stabilized. In particular, such high Q resonators as crystals require longer periods to stabilize. Because there is a delay between restarting of the oscillator and oscillator stabilization, t_2 should be long enough to ensure that the oscillator has been fully stabilized.

To facilitate Stop mode control, an external capacitor can be connected to the $\overline{RESET}$ pin (see Stop Mode Control Circuit), affecting only t_2, allowing control of the oscillator stabilization time. When V_{DD} is asserted in Stop mode, the capacitor begins charging, pulling up $\overline{RESET}$. When $\overline{RESET}$ reaches a threshold level equivalent to a logic 1, Stop mode is released. The time it takes $\overline{RESET}$ to reach the threshold level of logic 1 determines the oscillator stabilization time, which is a function of the capacitance and pull-up resistance values.

Stop Mode Control Circuit



Note: ① Polarized electrolytic capacitor

Port Operation

A port-loading option is offered at the time of ordering the mask. Individual source current requirements for Port 1 and the upper and lower halves of Port 2 may be factory set at either $-5\mu A$ or $-50\mu A$ (see Port-Loading Options table). The $-50\mu A$ option is required for interfacing with TTL/NMOS devices. The $-5\mu A$ option is recommended for interfacing to other CMOS devices. The CMOS option results in lower power consumption and greater noise immunity.

Port lines P_{10} to P_{17} and P_{24} to P_{27} include a protective circuit "E" to prevent a signal conflict at the port. The circuit prevents a logic 1 from being written to a line that is being pulled down externally (see Port Protection Circuit "E" diagram). When a logic 0 is detected at the port line and a logic 1 is written from the bus, the NOR gate sends a logic 1 to the D input of the flip-flop. The output is inverted, forcing the NAND gate to send a high-level output. This turns off transistor A, preventing the output of a logic 1 from the port.

Port-Loading Options

I_{OH} (min) V_{CC} = V_{DD} = 5V ± 10%; V_{OH} = 2.4V (min)

Option Selected	P_{10}–P_{17}	P_{20}–P_{23}	P_{24}–P_{27}	Unit
A	−5	−5	−5	μA
B	−50	−5	−5	μA
C	−5	−50	−5	μA
D	−50	−50	−5	μA
E	−5	−5	−50	μA
F	−50	−5	−50	μA
G	−5	−50	−50	μA
H	−50	−50	−50	μA

Notes: ① The selection of I_{OH} = −5μA will result in a port source current of I_{ILP} = −40μA max when used as input port
② The selection of I_{OH} = −50μA will result in a port source current of I_{ILP} = −500μA max when used as input port

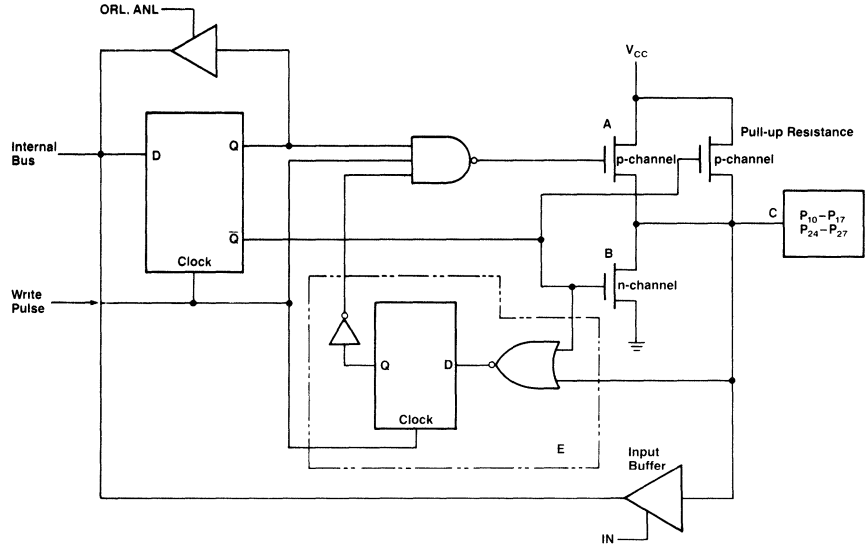
Oscillator Operation

The oscillator maintains an internal frequency for clock generation and controls all system timing cycles. The oscillation is initiated by either a self-generating external resonator or external clock input. The oscillator acts as a high-gain amplifier which produces square-wave pulses at the frequency determined by the resonator or clock source to which it is connected.

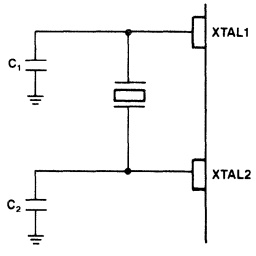
To obtain the oscillation frequency, an external LC network may be connected to the oscillator, or, a ceramic or crystal external resonator may be connected.

As the crystal frequency is lowered, there is an equivalent reduction in series resistance (R). As the temperature of the crystal is lowered, R is increased. Due to this relationship, it becomes difficult to stabilize oscillation when there is low power supply voltage. When V_{CC} is less than 2.7V and the oscillator frequency is 3MHz or less, T_a (ambient temperature) should not be less than −10°C.

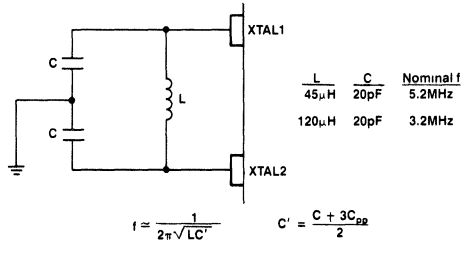
Port Protection Circuit "E"



Crystal Frequency Reference Circuit



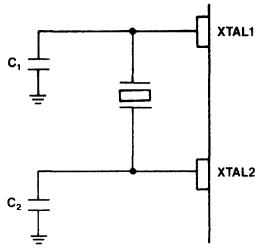
LC Frequency Reference Circuit



Notes: ① Crystal oscillator constants of f_{osc} = 6MHz
R_{max} = 50Ω
C_L = 16 ± 0 2pF
P = 1 ± 0 2mW
② Operating frequency less than 4MHz
$0 < C_1 \leq 20pF$
$0 < C_2 \leq 20pF$
$|C_2 - C_1| \leq 10pF$
③ Operating frequency more than 4MHz
$0 < C_1 \leq 10pF$
$0 < C_2 \leq 10pF$
$|C_2 - C_1| \leq 5pF$

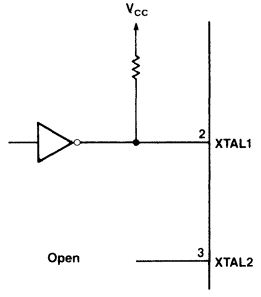
Note: C_{pp} = 5–10pF Pin to pin capacitance should be approximately 20pF, including stray capacitance

Ceramic Resonator Frequency Reference Circuit



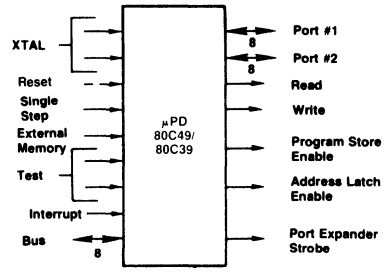
Note: $C_1 > C_2$
$(C_1 - C_2) = 20pF$
For example, C_1 = 30pF, and C_2 = 10pF
Values of C_1 and C_2 do not include stray capacitance

External Clock Frequency Reference Circuit



Note: A minimum voltage of V_{CC}-1 is required for XTAL1 to go HIGH

Major Input and Output Signals



Instruction Set Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary Carry Flag
addr	Program or data memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank Switch
BUS	Bus
C	Carry Flag
CLK	Clock
CNT	Counter
data	8-bit binary data (d_0–d_7)
DBF	Memory Bank Flip-Flop
F0, F1	Flag 0, Flag 1
INT	Interrupt pin
n	Indicates the hex number of the specified register or port
PC	Program Counter
P_p	Port 1, Port 2, or Port 4–7 ($_p$ = 1, 2, or 4–7)
PSW	Program Status Word
R_r	Register R_0–R_7 ($_r$ = 0–7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T0, T1	Test 0, Test 1 pin
#	Immediate data indication
@	Indirect address indication
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the operand
(x)	Contents of RAM
((x))	Contents of memory addressed by (x)
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
⊻	Exclusive OR
‾‾	Complement

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Instruction Set

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Accumulator													
ADD A, # data	(A) ← (A) + data	Adds immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags.②	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, R_r	(A) ← (A) + (R_r) $_r$ = 0–7	Adds the contents of register R_r to the accumulator Sets or clears both carry flags.②	6n④	0	1	1	0	1	r	r	r	1	1
ADD A, @ R_r	(A) ← (A) + ((R_r)) $_r$ = 0–1	Adds the contents of the internal data memory location specified by bits 0–5 of register R_r to the accumulator. Sets or clears both carry flags.②	6n④	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + data + (C)	Adds, with carry, immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags.②	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, R_r	(A) ← (A) + (R_r) + (C) $_r$ = 0–7	Adds, with carry, the contents of register R_r to the accumulator. Sets or clears both carry flags.②	7n④	0	1	1	1	1	r	r	r	1	1
ADDC A, @ R_r	(A) ← (A) + ((R_r)) + (C) $_r$ = 0–1	Adds, with carry, the contents of the internal data memory location specified by bits 0–5 of register R_r, to the accumulator. Sets or clears both carry flags.②	7n④	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A)∧data	Takes the logical product (logical AND) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, R_r	(A) ← (A)∧(R_r) $_r$ = 0–7	Takes the logical product (logical AND) of the contents of register R_r and the accumulator, and stores the result in the accumulator.	5n④	0	1	0	1	1	r	r	r	1	1
ANL A, @ R_r	(A) ← (A)∧((R_r)) $_r$ = 0–1	Takes the logical product (logical AND) of the contents of the internal data memory location specified by bits 0–5 of register R_r, and the accumulator, and stores the result in the accumulator.	5n④	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← $\overline{(A)}$	Takes the complement of the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clears the contents of the accumulator.	27	0	0	1	0	0	1	1	1	1	1
DA A		Converts the contents of the accumulator to BCD Sets or clears the carry flags. When the lower 4 bits (A_{0-3}) are greater than 9, or if the Auxiliary Carry Flag has been set, adds 6 to A_{0-3}. When the upper 4 bits (A_{4-7}) are greater than 9 or if the Carry Flag (C) has been set, adds 6 to A_{4-7}. If an overflow occurs at this point, C is set.②	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrements the contents of the accumulator by 1.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increments the contents of the accumulator by 1.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A)∨data	Takes the logical sum (logical OR) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, R_r	(A) ← (A)∨(R_r) $_r$ = 0–7	Takes the logical sum (logical OR) of register R_r and the contents of the accumulator, and stores the result in the accumulator	4n④	0	1	0	0	1	r	r	r	1	1
ORL A, @ R_r	(A) ← (A)∨((R_r)) $_r$ = 0–1	Takes the logical sum (logical OR) of the contents of the internal data memory location specified by bits 0–5 in register R_r, and the contents of the accumulator, and stores the result in the accumulator.	4n④	0	1	0	0	0	0	0	r	1	1
RL A	(Ab + 1) ← (Ab) (A_0) ← (A_7) b = 0–6	Rotates the contents of the accumulator one bit to the left. The MSB is rotated into the LSB.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	(Ab + 1) ← (Ab) (A_0) ← (C) (C) ← (A_7) b = 0–6	Rotates the contents of the accumulator one bit to the left through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	(Ab) ← (Ab + 1) (A_7) ← (A_0) b = 0–6	Rotates the contents of the accumulator one bit to the right. The LSB is rotated into the MSB.	77	0	1	1	1	0	1	1	1	1	1
RRC A	(Ab) ← (Ab + 1) (A_7) ← (C) (C) ← (A_0) b = 0–6	Rotates the contents of the accumulator one bit to the right through carry.	67	0	1	1	0	0	1	1	1	1	1
SWAP A	(A_{4-7}) ↔ (A_{0-3})	Exchanges the contents of the lower 4 bits of the accumulator with the upper 4 bits of the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A)∀data	Takes the exclusive OR of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, R_r	(A) ← (A)∀(R_r) $_r$ = 0–7	Takes the exclusive OR of the contents of register R_r and the accumulator, and stores the result in the accumulator.	Dn④	1	1	0	1	1	r	r	r	1	1
XRL A, @ R_r	(A) ← (A)∀((R_r)) $_r$ = 0–1	Takes the exclusive OR of the contents of the location in data memory specified by bits 0–5 in register R_r, and the accumulator, and stores the result in the accumulator.	Dn④	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ R_r, addr	(R_r) ← (R_r) – 1 If (R_r) ≠ 0, then (PC_{0-7}) ← addr $_r$ = 0–7	Decrements the contents of register R_r by 1, and if the result is not equal to 0, jumps to the address indicated by a_0–a_7.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	(PC_{0-7}) ← addr if b = 1 (PC) = (PC) + 2 if b = 0	Jumps to the address specified by a_0–a_7 if the bit in the accumulator specified by b_0–b_2 is set.	x2⑥	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2

Instruction Set (Cont.)

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
		Branch (Cont.)											
JC addr	$(PC_{0-7}) \leftarrow$ addr if C = 1 $(PC) \leftarrow (PC) + 2$ if C = 0	Jumps to the address specified by a_0-a_7 if the Carry Flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_{0-7}) \leftarrow$ addr if F0 = 1 $(PC) \leftarrow (PC) + 2$ if F0 = 0	Jumps to the address specified by a_0-a_7 if F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_{0-7}) \leftarrow$ addr if F1 = 1 $(PC) \leftarrow (PC) + 2$ if F1 = 0	Jumps to the address specified by a_0-a_7 if F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_{8-10}) \leftarrow addr_{8-10}$ $(PC_{0-7}) \leftarrow addr_{0-7}$ $(PC_{11}) \leftarrow$ DBF	Jumps directly to the address specified by a_0-a_{10} and the DBF.	x4⑥	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_{0-7}) \leftarrow ((A))$	Replaces the lower 8 bits of the Program Counter with the contents of program memory specified by the contents of the accumulator, producing a jump to the specified address within the current page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_{0-7}) \leftarrow$ addr if C = 0 $(PC) \leftarrow (PC) + 2$ if C = 1	Jumps to the address specified by a_0-a_7 if the Carry Flag is not set.	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_{0-7}) \leftarrow$ addr if I = 0 $(PC) \leftarrow (PC) + 2$ if I = 1	Jumps to the address specified by a_0-a_7 if the Interrupt Flag is not set.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jumps to the address specified by a_0-a_7 if Test 0 is LOW.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 0 $(PC) \leftarrow (PC) + 2$ if T1 = 1	Jumps to the address specified by a_0-a_7 if Test 1 is LOW.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_{0-7}) \leftarrow$ addr if A ≠ 0 $(PC) \leftarrow (PC) + 2$ if A = 0	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are not equal to 0.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_{0-7}) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jumps to the address specified by a_0-a_7 if the Timer Flag is set. The Timer Flag is cleared after the instruction is executed.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_{0-7}) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jumps to the address specified by a_0-a_7 if Test 0 is HIGH.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_{0-7}) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jumps to the address specified by a_0-a_7 if Test 1 is HIGH.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ	$(PC_{0-7}) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jumps to the address specified by a_0-a_7 if the contents of the accumulator are equal to 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
		Control											
EN I		Enables external interrupts. When external interrupts are enabled, a low-level input to the INT pin causes the processor to vector to the interrupt service routine.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disables external interrupts. When external interrupts are disabled, low-level inputs to the INT pin have no effect on program execution.	15	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enables clock output to pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) ← 0	Clears the Memory Bank Flip-Flop, selecting Program Memory Bank 0 [program memory addresses $0\text{-}2047_{(10)}$]. Clears PC_{11} after the next JMP or CALL instruction.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) ← 1	Sets the Memory Bank Flip-Flop, selecting Program Memory Bank 1 [program memory addresses $2048\text{-}4095_{(10)}$]. Sets PC_{11} after the next JMP or CALL instruction.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Selects Data Memory Bank 0 by clearing bit 4 (Bank Switch) of the PSW. Specifies data memory addresses $0-7_{(10)}$ as registers 0–7 of Data Memory Bank 0.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Selects Data Memory Bank 1 by setting bit 4 (Bank Switch) of the PSW. Specifies data memory $24-31_{(10)}$ as registers 0–7 of Data Memory Bank 1.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates Halt mode.	01	0	0	0	0	0	0	0	1	1	1
		Data Moves											
MOV A, # data	(A) ← data	Moves immediate data d_0-d_7 into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, R_r	(A) ← (R_r) $_r$ = 0–7	Moves the contents of register R_r into the accumulator.	Fn④	1	1	1	1	1	r	r	r	1	1
MOV A, @ R_r	(A) ← ((R_r)) $_r$ = 0–1	Moves the contents of internal data memory specified by bits 0–5 in register R_r, into the accumulator.	Fn④	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Moves the contents of the Program Status Word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV R_r, # data	(R_r) ← data $_r$ = 0–7	Moves immediate data d_0-d_7 into register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV R_r, A	(R_r) ← (A) $_r$ = 0–7	Moves the contents of the accumulator into register R_r.	An④	1	0	1	0	1	r	r	r	1	1
MOV @ R_r, A	((R_r)) ← (A) $_r$ = 0–1	Moves the contents of the accumulator into the data memory location specified by bits 0–5 in register R_r.	An④	1	0	1	0	0	0	0	r	1	1
MOV @ R_r, # data	((R_r)) ← data $_r$ = 0–1	Moves immediate data d_0-d_7 into the data memory location specified by bits 0–5 in register R_r.	Bn④	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2
MOV PSW, A	(PSW) ← (A)	Moves the contents of the accumulator into the Program Status Word.	D7	1	1	0	1	0	1	1	1	1	1

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Instruction Set (Cont.)

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
		Data Moves (Cont.)											
MOVP A, @ A	$(PC_{0-7}) \leftarrow (A)$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by PC_{8-11} concatenated with the contents of the accumulator, into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	$(PC_{0-7}) \leftarrow (A)$ $(PC_{8-11}) \leftarrow 001$ $(A) \leftarrow ((PC))$	Moves the contents of the program memory location specified by 0011 (PC_{8-11}, page 3 of Program Memory Bank 0) and the contents of the accumulator, into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	$(A) \leftarrow ((R_r))$ $r = 0-1$	Moves the contents of the external data memory location specified by register R_r, into the accumulator.	8n④	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	$((R_r)) \leftarrow (A)$ $r = 0-1$	Moves the contents of the accumulator into the external data memory location specified by register R_r.	9n④	1	0	0	1	0	0	0	r	2	1
XCH A, R_r	$(A) \leftrightarrow (R_r)$ $r = 0-7$	Exchanges the contents of the accumulator and register R_r.	2n④	0	0	1	0	1	r	r	r	1	1
XCH A, @ R_r	$(A) \leftrightarrow ((R_r))$ $r = 0-1$	Exchanges the contents of the accumulator and the contents of the data memory location specified by bits 0–5 in register R_r.	2n④	0	0	1	0	0	0	0	r	1	1
XCHD A, @ R_r	$(A_{0-3}) \leftrightarrow ((R_{r0-3}))$ $r = 0-1$	Exchanges the contents of the lower 4 bits of the accumulator with the contents of the lower 4 bits of the internal data memory location specified by bits 0–5 in register R_r.	3n④	0	0	1	1	0	0	0	r	1	1
		Flags											
CPL C	$(C) \leftarrow \overline{(C)}$	Takes the complement of the Carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	$(F0) \leftarrow \overline{(F0)}$	Takes the complement of Flag 0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	$(F1) \leftarrow \overline{(F1)}$	Takes the complement of Flag 1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	$(C) \leftarrow 0$	Clears the Carry bit.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	$(F0) \leftarrow 0$	Clears Flag 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	$(F1) \leftarrow 0$	Clears Flag 1.	A5	1	0	1	0	0	1	0	1	1	1
		Input/Output											
ANL BUS, # data	$(BUS) \leftarrow (BUS) \wedge data$	Takes the logical AND of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus.	98	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ANL P_p, # data	$(P_p) \leftarrow (P_p) \wedge data$ $p = 1-2$	Takes the logical AND of the contents of designated port P_p and immediate data d_0–d_7, and sends the result to port P_p for output.	9n⑤	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
ANLD P_p, A	$(P_p) \leftarrow (P_p) \wedge (A_{0-3})$ $p = 4-7$	Takes the logical AND of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	9n⑤	1	0	0	1	1	1	p	p	2	1
IN A, P_p	$(A) \leftarrow (P_p)$ $p = 1-2$	Loads the accumulator with the contents of designated port P_p.	0n⑤	0	0	0	0	1	0	p	p	2	1
INS A, BUS	$(A) \leftarrow (BUS)$	Loads the contents of the bus into the accumulator on the rising edge of RD.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, P_p	$(A_{0-3}) \leftarrow (P_p)$ $(A_{4-7}) \leftarrow 0$ $p = 4-7$	Moves the contents of designated port P_p to the lower 4 bits of the accumulator, and clears the upper 4 bits.	0n⑤	0	0	0	0	1	1	p	p	2	1
MOVD P_p, A	$(P_p) \leftarrow (A_{0-3})$ $p = 4-7$	Moves the lower 4 bits of the accumulator to designated port P_p. The upper 4 bits of the accumulator are not changed.	3n⑤	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	$(BUS) \leftarrow (BUS) \vee data$	Takes the logical OR of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus	88	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ORLD P_p, A	$(P_p) \leftarrow (P_p) \vee (A_{0-3})$ $p = 4-7$	Takes the logical OR of the contents of designated port P_p and the lower 4 bits of the accumulator, and sends the result to port P_p for output.	8n⑤	1	0	0	0	1	1	p	p	2	1
ORL P_p, # data	$(P_p) \leftarrow (P_p) \vee data$ $p = 1-2$	Takes the logical OR of the contents of designated port P_p and immediate data d_0–d_7, and sends the result to port P_p for output.	9n⑤	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
OUTL BUS, A	$(BUS) \leftarrow (A)$	Latches the contents of the accumulator onto the bus on the rising edge of $\overline{WR}$. **Note:** Never use the OUTL BUS instruction when using external program memory, as this will permanently latch the bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL P_p, A	$(P_p) \leftarrow (A)$ $p = 1-2$	Latches the contents of the accumulator into designated port P_p for output.	3n⑤	0	0	1	1	1	0	p	p	2	1
		Registers											
DEC R_r	$(R_r) \leftarrow (R_r) - 1$ $r = 0-7$	Decrements the contents of register R_r by 1.	Cn④	1	1	0	0	1	r	r	r	1	1
INC R_r	$(R_r) \leftarrow (R_r) + 1$ $r = 0-7$	Increments the contents of register R_r by 1.	1n④	0	0	0	1	1	r	r	r	1	1
INC @ R_r	$((R_r)) \leftarrow ((R_r)) + 1$ $r = 0-1$	Increments by 1 the contents of the data memory location specified by bits 0–5 in register R_r.	1n④	0	0	0	1	0	0	0	r	1	1

Instruction Set (Cont.)

Mnemonic	Function	Description	Hex Code	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
		Subroutine											
CALL addr	$((SP)) \leftarrow (PC), (PSW_{4-7})$ $(SP) \leftarrow (SP) + 1$ $(PC_{8-10}) \leftarrow addr_{9-10}$ $(PC_{0-7}) \leftarrow addr_{0-7}$ $(PC_{11}) \leftarrow DBF$	Stores the contents of the Program Counter and the upper 4 bits of the PSW in the address indicated by the Stack Pointer, and increments the contents of the Stack Pointer, calling the subroutine specified by address a_0–a_{10} and the DBF.	x4④	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	$(SP) \leftarrow (SP) - 1$ $(PC) \leftarrow ((SP))$	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the location specified by the Stack Pointer, executing a return from subroutine without restoring the PSW.	83	1	0	0	0	0	0	1	1	2	1
RETR	$(SP) \leftarrow (SP) - 1$ $(PC) \leftarrow ((SP))$ $(PSW_{4-7}) \leftarrow ((SP))$	Decrements the contents of the Stack Pointer by 1 and stores, in the Program Counter, the contents of the upper 4 bits of the PSW and the contents of the location specified by the Stack Pointer, executing a return from subroutine with restoration of the PSW.	93	1	0	0	1	0	0	1	1	2	1
		Timer/Counter											
EN TCNTI		Enables internal interrupt of timer/event counter. If an overflow condition occurs, then an interrupt will be generated.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disables internal interrupt of timer/event counter.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	$(A) \leftarrow (T)$	Moves the contents of the timer/counter into the accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	$(T) \leftarrow (A)$	Moves the contents of the accumulator into the timer/counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stops the operation of the timer/event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Starts the event counter operation of the timer/counter when T1 changes from a low-level input to a high-level input.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Starts the timer operation of the timer/counter. The timer is incremented every 32 machine cycles.	55	0	1	0	1	0	1	0	1	1	1
		Miscellaneous											
NOP		Uses one machine cycle without performing any operation.	00	0	0	0	0	0	0	0	0	1	1

Notes: ① Binary instruction code designations $_r$ and $_p$ represent encoded values or the lowest-order bit value of specified registers and ports, respectively

② Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the Auxiliary Carry Flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions

③ References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction

④ The hex value of n for specific registers is as follows

a) Direct addressing

R_0 n = 8 R_2 n = A R_4 n = C R_6 n = E
R_1 n = 9 R_3 n = B R_5 n = D R_7 n = F

b) Indirect addressing

@R_0 n = 0 @R_1 n = 1

⑤ The hex value of n for specific ports is as follows

P_1 n = 9 P_4 n = C P_6 n = E
P_2 n = A P_5 n = D P_7 n = F

⑥ The hex value of x for specific accumulator or address bits is as follows

a) JBb instruction

B_0 x = 1 B_2 x = 5 B_4 x = 9 B_6 x = D
B_1 x = 3 B_3 x = 7 B_5 x = B B_7 x = F

b) JMP instruction

Page 0 x = 0 Page 2 x = 4 Page 4 x = 8 Page 6 x = C
Page 1 x = 2 Page 3 x = 6 Page 5 x = A Page 7 x = E

c) CALL instruction

Page 0 x = 1 Page 2 x = 5 Page 4 x = 9 Page 6 x = D
Page 1 x = 3 Page 3 x = 7 Page 5 x = B Page 7 x = F

DC Characteristics: Standard Voltage Range

T_a = −40°C to +85°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input High Voltage	V_{IH}	V_{CC}−2		V_{CC}	V	All except XTAL1, XTAL2, $\overline{RESET}$
	V_{IH1}	V_{CC}−1		V_{CC}	V	$\overline{RESET}$, XTAL1, XTAL2
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0mA
Output High Voltage	V_{OH}	2.4			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; I_{OH} = −100μA
	V_{OH1}①	2.4			V	Port 1, Port 2; I_{OH} = −5μA (Type 0)
						Port 1, Port 2; I_{OH} = −50μA (Type 1)
	V_{OH2}	V_{CC}−0.5			V	All outputs; I_{OH} = −0.2μA
Input Current	I_{ILP}①		−15	−40	μA	Port 1, Port 2; $V_{IN} \le V_{IL}$ (Type 0)
				−500	μA	Port 1 Port 2; $V_{IN} \le V_{IL}$ (Type 1)
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \le V_{IL}$
Input Leakage Current	I_{LI1}			±1	μA	T1, $\overline{INT}$, V_{DD}; $V_{SS} \le V_{IN} \le V_{CC}$
	I_{LI2}			±3	μA	EA; $V_{SS} \le V_{IN} \le V_{CC}$
Output Leakage Current	I_{LO}			±1	μA	Bus, T0, High-Impedance State; $V_{SS} \le V_O \le V_{CC}$
Standby Current	I_{CC1}		0.4	0.8	mA	Halt mode; t_{CY} = 2.5μs
	I_{CC2}		1	20	μA	Stop mode ②
Supply Current	I_{CC}		4	8	mA	t_{CY} = 2.5μs
Data Retention Voltage	V_{CCDR}	2.0			V	Stop mode (V_{DD}, $\overline{RESET}$ ≤ 0.4V)

DC Characteristics: Extended Voltage Range

T_a = −40°C to +85°C; V_{CC} = +2.5V to +5.5V; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.3		0.18 V_{CC}	V	
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH}	0.7V_{CC}		V_{CC}	V	
Input High Voltage (XTAL 1, XTAL 2)	V_{IH1}	0.8V_{CC}		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.0mA
Output High Voltage (Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0	V_{OH}	0.75V_{CC}			V	I_{OH} = −100μA
Output High Voltage (All Other Outputs	V_{OH1}	0.7V_{CC}			V	Port 1, Port 2; I_{OH} = −1μA (Type 0)
						Port 1, Port 2; I_{OH} = −10μA (Type 1)
Output High Voltage (All Outputs)	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −0.2μA
Input Leakage Current (Port 1, Port 2)	I_{ILP}		−15	−40	μA	$V_{IN} \le V_{IL}$ (Type 0)
				−500	μA	$V_{IN} \le V_{IL}$ (Type 1)
Input Leakage Current ($\overline{SS}$, $\overline{RESET}$)	I_{ILC}			−40	μA	$V_{IN} \le V_{IL}$
Input Leakage Current (T1, $\overline{INT}$)	I_{IL1}			±1	μA	$V_{SS} < V_{IN} < V_{CC}$
Input Leakage Current (EA)	I_{IL2}			±3	μA	$V_{SS} < V_{IN} < V_{CC}$
Output Leakage Current (Bus, T0 — High Impedance State)	I_{OL}			±1	μA	$V_{SS} < V_O < V_{CC}$
Supply Current	I_{CC}		0.8	1.6	mA	V_{CC} = 3V, t_{CY} = 10μs
Halt Mode Standby Current	I_{CC1}		100	200	μA	V_{CC} = 3V, t_{CY} = 10μs
Stop Mode Standby Current	I_{CC2}		1	20	μA	

Notes: ① Type 0 and type 1 options apply only to the μPD80C48, the μPD80C35 is type 1 only
② Input Pin Voltage is V_{IN}, V_{IL}, or V_{IN}, V_{IH}

AC Characteristics

Read, Write and Instruction Fetch: External Data and Program Memory

T_a = −40°C to +85°C; V_{CC} = V_{DD} = +5V ± 10%; V_{SS} = 0V

Parameter	Symbol	V_{CC} = +5V ± 10% Min	Typ	Max	V_{CC} = +2.5V to +5.5V Min	Typ	Max	Unit	Test Conditions
ALE Pulse Width	t_{LL}	400			2160			ns	
Address Setup before ALE	t_{AL}	120			1620			ns	
Address Hold from ALE	t_{LA}	80			330			ns	①
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	700			3700			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			3500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			370			ns	②
Cycle Time	t_{CY}	2.5		150	10		150	μs	6MHz XTAL
Data Hold	t_{DR}	0		200	0		950	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500			2750	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			3230			ns	①
Address Setup before Data In	t_{AD}			950			5450	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			500			ns	
Control Pulse to ALE	t_{CA}	10			10			ns	

Port 2 Timing
T_a = −40°C to +85°C; V_{CC} = +5V ± 10%

Parameter	Symbol	V_{CC} = +5V ± 10% Min	Typ	Max	V_{CC} = +2.5V to +5.5V Min	Typ	Max	Unit	Test Conditions
Port Control Setup before Falling Edge of PROG	t_{CP}	110			860			ns	
Port Control Hold after Falling Edge of PROG	t_{PC}	0		80	0		200	ns	④
PROG to Time P2 input must be Valid	t_{PR}			810			5310	ns	
Output Data Setup Time	t_{DP}	250			3250			ns	③
Output Data Hold Time	t_{PD}	65			820			ns	
Input Data Hold Time	t_{PF}	0		150	0		900	ns	
PROG Pulse Width	t_{PP}	1200			6450			ns	
Port 2 I/O Data Setup	t_{PL}	350			2100			ns	
Port 2 I/O Data Hold	t_{LP}	150			1400			ns	

Notes: ① For Control Outputs C_L = 80pF, for Bus Outputs· C_L = 150pF
② C_L = 20pF
③ For Control Outputs C_L = 80pF
④ Refer to the operating characteristic curves for Supply Voltage and Port Control Hold

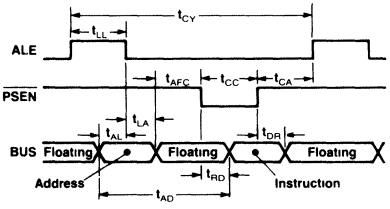
BUS Timing Requirements

Symbol	Timing Formula	Min	Max	Unit
t_{LL}	(7/30) T−167	•		ns
t_{AL}	(1/5) T−285	•		ns
t_{LA}	(1/30) T	•		ns
t_{CC}	(2/5) T−300	•		ns
t_{DW}	(2/5) T−500	•		ns
t_{WD}	(1/30) T+40	•		ns
t_{DR}	(1/10) T−50		•	ns
t_{RD}	(3/10) T−250		•	ns
t_{AW}	(2/5) T−600	•		ns
t_{AD}	(3/5) T−550		•	ns
t_{AFC}	(1/15) T−125	•		ns
t_{CP}	(1/10) T−87	•		ns
t_{PR}	(3/5) T−475		•	ns
t_{PF}	(1/10) T−100		•	ns
t_{DP}	(2/5) T−550	•		ns
t_{PD}	(1/10) T−167	•		ns
t_{PP}	(7/10) T−550	•		ns
t_{PL}	(7/30) T−230	•		ns
t_{LP}	(1/6) T−265	•		ns

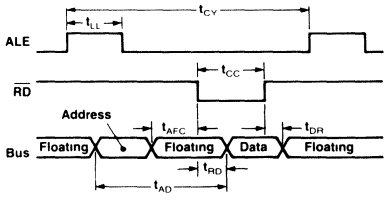
Notes: T = t_{CY}
Unlisted parameters are not affected by cycle time

Timing Waveforms

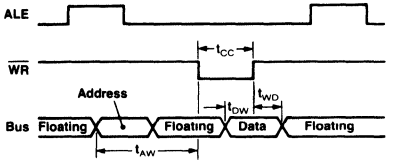
Instruction Fetch From External Memory



Read From External Data Memory

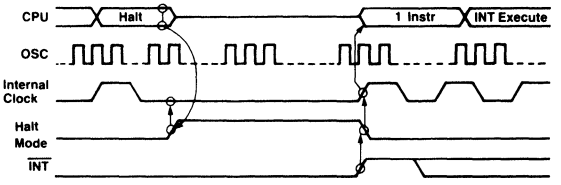


Write to External Memory

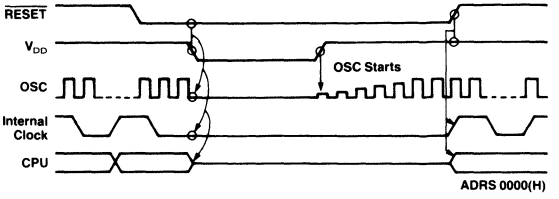


Low Power Standby Operation

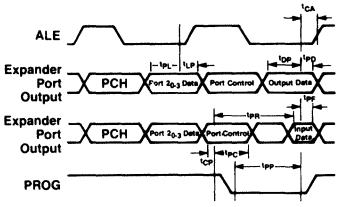
1) Halt Mode (When EI)



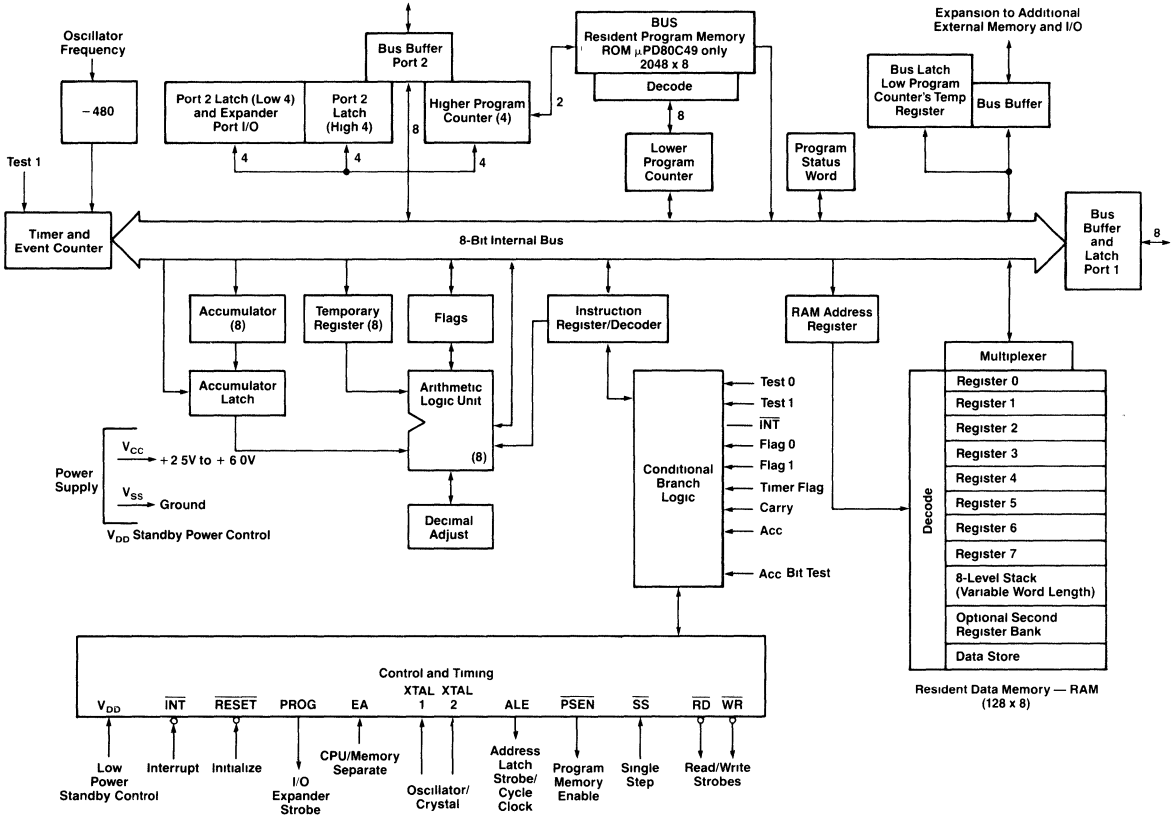
2) Stop Mode



Port 2 Timing



Block Diagram



Note: μPD80C39 does not include ROM

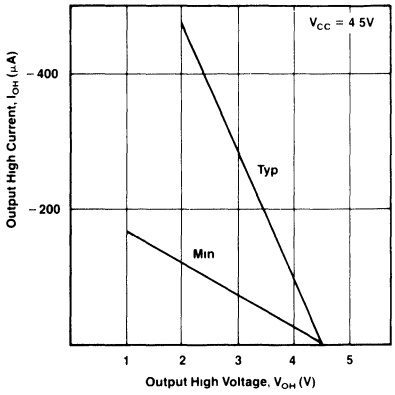
Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature, T_{opt}	−40°C to +85°C
Storage Temperature (Cerdip Package), T_{stg}	−65°C to +150°C
Storage Temperature (Plastic Package), T_{stg}	−65°C to +125°C
Voltage on Any Pin, $V_{I/O}$	V_{SS} −0.3V to V_{CC} +0.3V
Supply Voltage, V_{CC}	V_{SS} −0.3 to +10V
Power Dissipation, P_D	0.35w

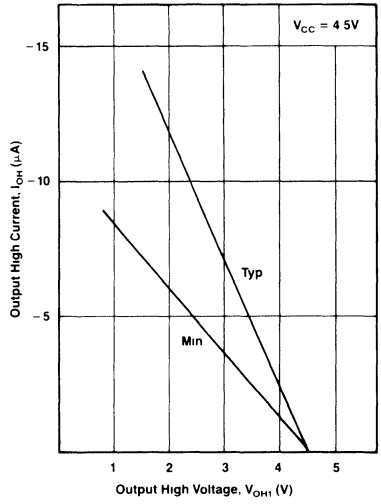
*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Characteristic Curves

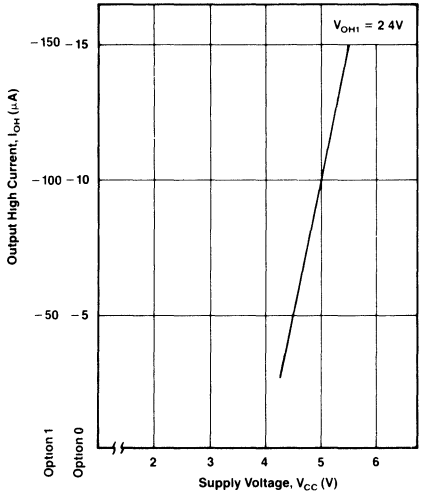
Output High Current vs. Output High Voltage



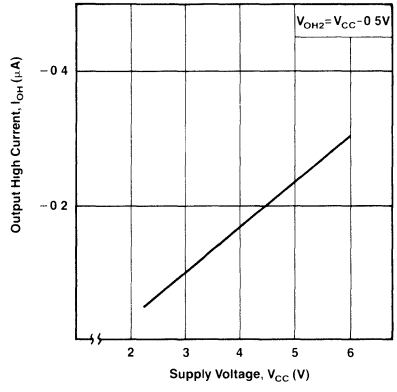
Output High Current vs. Output High Voltage



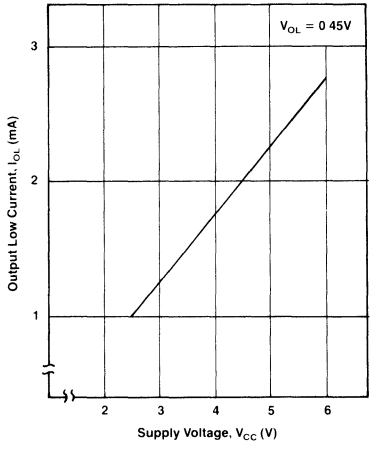
Output High Current vs. Supply Voltage



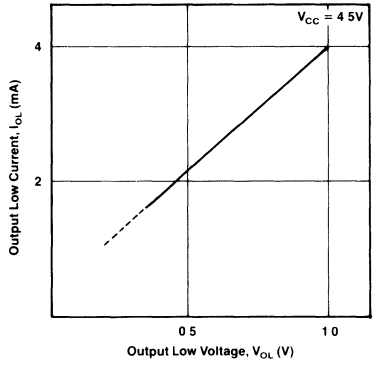
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage



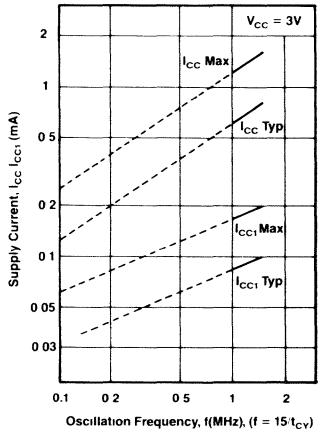
Output Low Current vs. Output Low Voltage



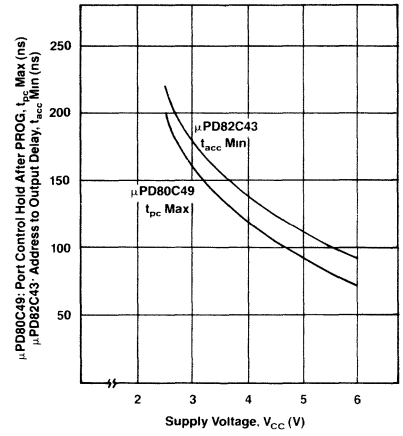
4

Operating Characteristic Curves (Cont.)

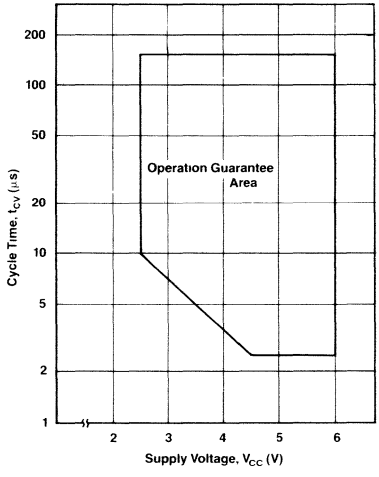
Supply Current vs. Oscillation Frequency



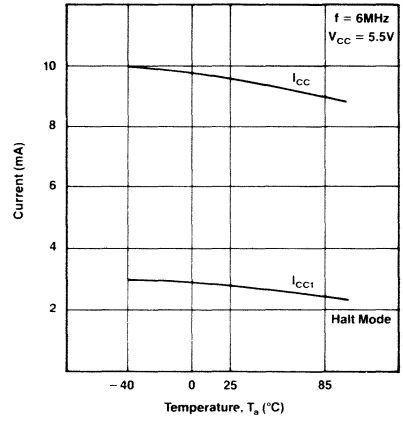
Port Control Hold After PROG, t_{pc} Max (μPD80C49), and Address to Output Delay, t_{acc} Min (μPD82C43), vs. Supply Voltage



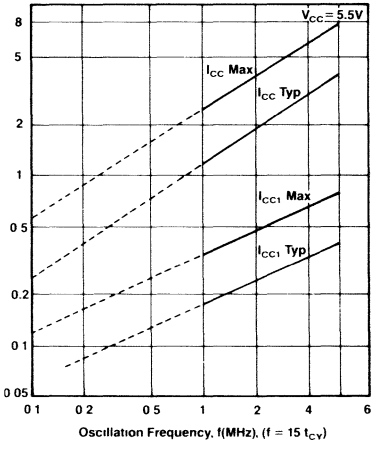
Cycle Time vs. Supply Voltage



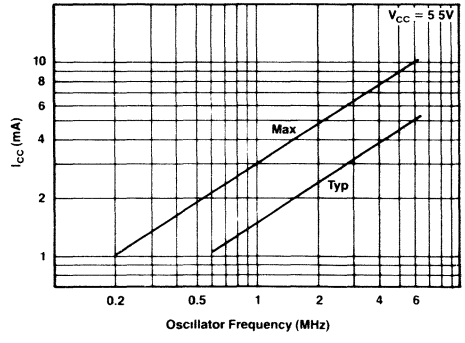
Current Consumption as a Function of Temperature — Normal Operating Mode



*Supply Current vs. Oscillation Frequency*①



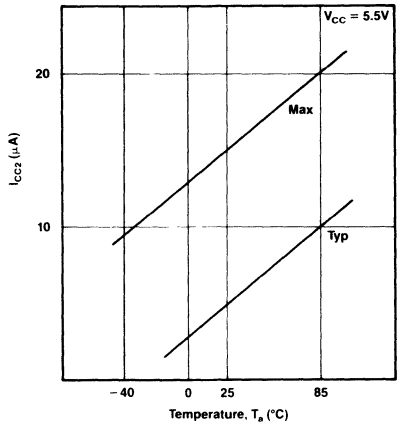
Current Consumption as a Function of Operating Frequency — Normal Operating Mode



Note: ① External oscillation is assumed for frequency less than 1 MHz. Internal oscillation requires more power.

Operating Characteristic Curves (Cont.)

Current Consumption as a Function of Temperature — Stop Mode



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD80C49C/C39C
Plastic Shrinkdip, μPD80C49HC
Plastic Miniflat, μPD80C49G/C39G

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NEC

MICROPROCESSORS 5

NEC

μPD780/μPD780-1/μPD780-2 HIGH-PERFORMANCE CP/M®-COMPATIBLE NMOS 8-BIT MICROPROCESSOR

Description

The μPD780 microprocessor utilizes a highly consistent architectural organization, a comprehensive instruction set that is a superset of the industry-standard 8080A instruction set, and third-generation technology, to provide a flexible, high-performance, efficient CPU easily adaptable to a very broad range of industrial and commercial applications.

All software developed on 8080A-based systems may be run on 780-based systems as a subset of the full 780 instruction set. In addition, the NEC μPD780 is fully pin-compatible and software-compatible with the Z80® microprocessor and is therefore perfectly suited for CP/M® designs. The NEC μPD780 provides system designers with powerful, wide-range logic capability that requires minimal additional circuitry to complete a microcomputer system.

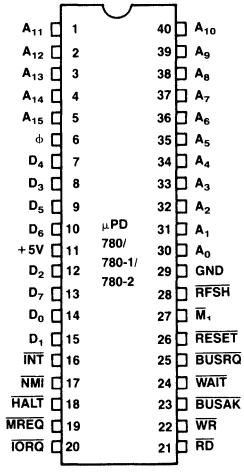
The output signals of the μPD780 are fully decoded and signal timing is fully compatible with industry-standard memory and peripheral devices. Two faster versions of the basic μPD780 (2.5MHz master clock rate) are offered by the μPD780-1 (4MHz master clock rate) and the μPD780-2 (6MHz master clock rate). Other than clock rates, all three versions are identical.

Features

- ☐ Powerful, wide-range logic capability requiring minimal support circuitry
- ☐ Fully Z80®-compatible
- ☐ Industry-standard 8080A software compatibility
- ☐ CP/M®-compatible
- ☐ Comprehensive, powerful instruction set featuring 158 instruction types
- ☐ Vectored, multilevel interrupt structure
- ☐ Highly consistent architectural structure featuring dual register set
- ☐ Foreground/background programming
- ☐ Automatic refreshing of external dynamic memory
- ☐ Signal timing compatible with industry-standard memory and peripheral devices
- ☐ TTL-compatible signals
- ☐ Single-phase +5V clock and +5VDC power supply
- ☐ Available in plastic package

®Z80 is a registered trademark of Zilog, Inc
®CP/M is a registered trademark of Digital Research Corporation

Pin Configuration



Pin Identification

Pin No.	Pin Symbol	Name	Function
1–5 30–40	A_0–A_{15}	Address Bus	These three-state output lines constitute a 16-bit address bus. Lines A_0–A_6 output the external memory address during refresh operations
6	φ	Clock	This line is used as an input for external clock sources.
7–10 12–15	D_0–D_7	Data Bus	These three-state I/O lines constitute an 8-bit bidirectional data bus
11	+5V	Power Supply	Single +5V power supply.
16	$\overline{INT}$	Interrupt Request	This active-low input line is used for interrupt requests by external I/O devices. Interrupts are serviced upon completion of the current instruction if the Interrupt Enable Flip-Flop (IFF) has been turned on by the software. There are three interrupt response modes: the mode-0 response is equivalent to an 8080 interrupt response, mode 1 uses location $0038_{(H)}$ as a restart address, and mode 2 is a simple vectoring to an interrupt-service routine that can be located anywhere in memory.
17	$\overline{NMI}$	Nonmaskable Interrupt	This active-low input line is used for nonmaskable interrupts. A nonmaskable interrupt is always acknowledged at the end of the current instruction, regardless of whether or not the Interrupt Enable Flip-Flop has been turned on, except when the $\overline{BUSRQ}$ signal is asserted. Because of the higher priority of the $\overline{BUSRQ}$ signal, it is acknowledged before the $\overline{NMI}$ signal. When $\overline{NMI}$ is acknowledged, program execution automatically restarts from location $0066_{(H)}$.
18	$\overline{HALT}$	Halt State	This active-low input line is used with the HALT instruction to initiate a halt state. When $\overline{HALT}$ is asserted, program execution stops and does not resume until an interrupt is generated. During the halt state, NOPs are executed in order to continue memory refresh operations.
19	$\overline{MREQ}$	Memory Request	This three-state active-low output line is used to indicate that the address specified for the memory read or write operation is valid.

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Pin Identification (Cont.)

Pin No.	Pin Symbol	Name	Function
20	$\overline{IORQ}$	I/O Request	This three-state active-low output line is used to indicate that the lower half of the address bus holds a valid address for an I/O read or write operation. During interrupt acknowledge cycles, $\overline{IORQ}$ and $\overline{M_1}$ are asserted together to indicate that a vector address can be sent to the data bus.
21	$\overline{RD}$	Read	This three-state active-low output line is used to strobe data from external memory or I/O devices onto the data bus. $\overline{RD}$ is asserted to indicate that the CPU is requesting data from external memory or I/O devices. This line is three-stated during halt or reset conditions.
22	$\overline{WR}$	Write	This three-state active-low output line is used to strobe data from the data bus to external memory or I/O devices. $\overline{WR}$ is asserted to indicate that the data bus holds valid data. This line is three-stated during halt or reset conditions.
23	$\overline{BUSAK}$	Bus Acknowledge	This active-low output line is used to inform the device requesting bus control that the data bus, address bus, and all three-state bus control signals ($\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, and $\overline{MREQ}$) are in a high-impedance state and the requesting device can now assume control.
24	$\overline{WAIT}$	Wait State	This active-low input line is used to indicate that external memory or I/O devices addressed by the CPU are not ready to transfer data. When $\overline{WAIT}$ is asserted, the CPU is placed in a wait condition
25	$\overline{BUSRQ}$	Bus Request	This active-low input signal is used to place the data bus, address bus, and all three-state bus control signals ($\overline{WR}$, $\overline{RD}$, $\overline{IORQ}$, and $\overline{MREQ}$) in a high-impedance state to allow a requesting device to assume bus control. The $\overline{BUSRQ}$ signal has a higher priority than the $\overline{NMI}$ signal and is always honored at the end of the current machine cycle ①
26	$\overline{RESET}$	Reset	This active-low input signal is used to initialize the CPU. When $\overline{RESET}$ is asserted, the Interrupt Enable Flip-Flop is reset, the program counter and the I and R registers are cleared, and interrupt response mode 0 is enabled. In a reset condition, the address and data buses are three-stated and all output control signals are inactive, after which program execution begins from address 0000 ②
27	$\overline{M_1}$	Machine Cycle 1	This active-low output line is used to indicate that the current machine cycle is the opcode fetch phase of an instruction execution.
28	$\overline{RFSH}$	Refresh	This active-low output line is used in conjunction with the $\overline{MREQ}$ signal to initiate a refresh read of all external dynamic memory. $\overline{RFSH}$ and $\overline{MREQ}$ are both asserted when the least-significant 7 bits of the address on the address bus hold a valid external dynamic memory address.
29	GND	Ground	Ground potential

Notes: ① Excessive DMA operations resulting in long periods in which $\overline{BUSRQ}$ is asserted can impair the CPU's ability to adequately refresh the dynamic RAMs

$\overline{BUSRQ}$ does not have an internal pull-up resistor. For input signals to this pin in a wire-OR'ed configuration, an external pull-up resistor should be used

② The pulse width of $\overline{RESET}$ must be a minimum of 3 clock cycles in length to reinitialize the CPU and stabilize operation

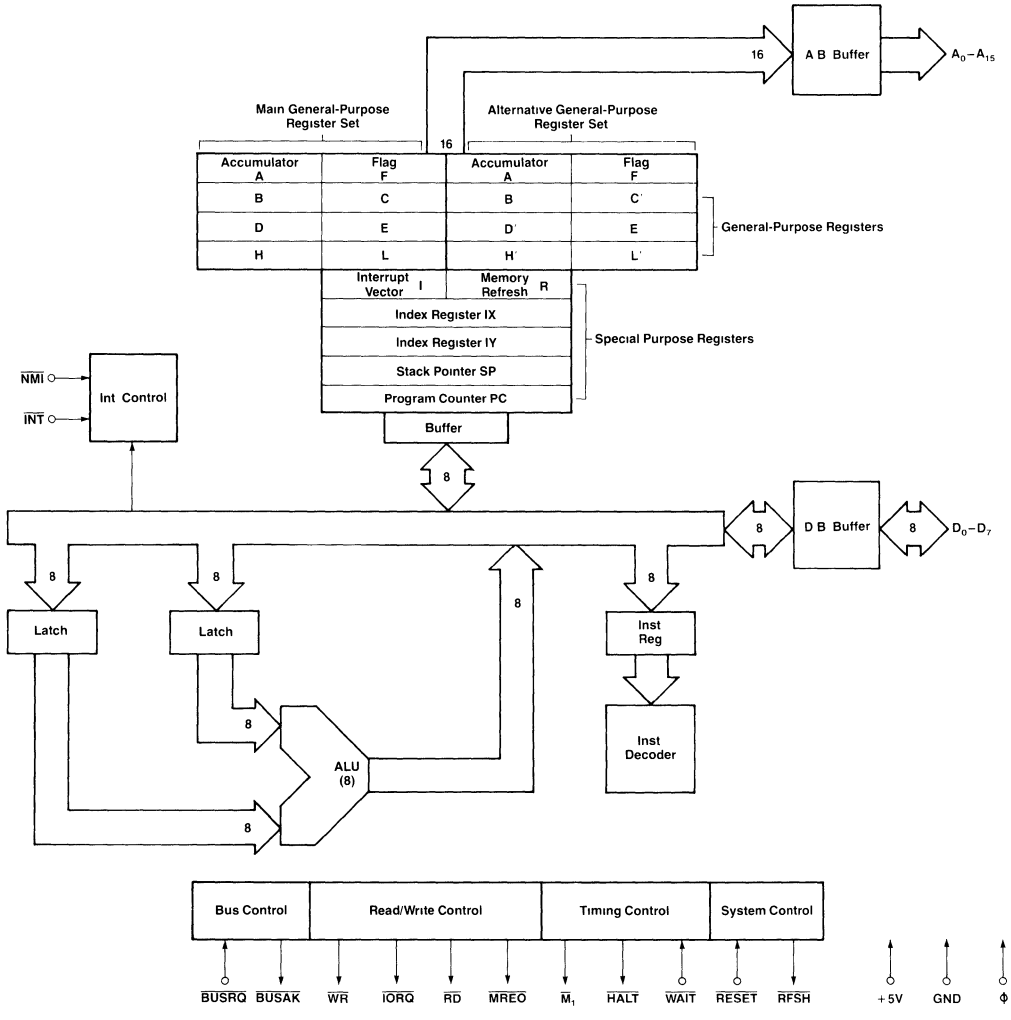
Architecture

The architecture includes a dual set of six 8-bit general-purpose registers and two 8-bit accumulators and flag registers. A flexible vectored interrupt structure is supported by an 8-bit interrupt vector register that provides the most-significant 8 bits of a pointer to a table of vector addresses, while the requesting device generates the least-significant 8 bits of the pointer. Two 16-bit index registers enable the manipulation of tabular data as well as facilitating code relocation.

Multilevel interrupts as well as virtually unlimited subroutine nesting are supported by a 16-bit stack pointer and complimentary 16-bit program counter, enhancing the speed and efficiency of a wide variety of data-handling operations. Processing efficiency is additionally supported by a special memory refresh register that enables automatic refreshing of all external dynamic memory with minimal processor overhead.

The dual set of general-purpose registers may be used as individual 8-bit registers or paired as 16-bit registers. The dual register set (including a dual accumulator and flag register) not only allows more powerful addressing and data transfer operations, but also permits programming in foreground/background mode for vastly improved throughput.

Block Diagram



Instruction Set

The instruction set of the μPD780 consists of 158 types of instructions divided into 16 categories as follows:

- 8-bit load operations
- register exchanges
- memory block searches
- 16-bit arithmetic operations
- rotate and shift operations
- jump operations
- restart operations
- miscellaneous operations
- 16-bit load operations
- memory block transfers
- 8-bit arithmetic and logic operations
- bit set, reset, and test operations
- I/O operations
- call operations
- return operations
- general-purpose accumulator and flag operations

This comprehensive instruction set is made more powerful by the array of addressing modes implemented by the architecture, as follows:

- bit addressing
- register-indirect addressing
- immediate addressing
- extended addressing
- implied addressing
- register addressing
- relative addressing
- immediate-extended addressing
- indexed addressing
- modified page zero addressing

Instruction Set (Cont.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OPCODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg pair ss to HL	1	15	↕	↕	V	↕	0	X	11 101 101 Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrr Ⓑ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrr Ⓑ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss1 001 Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 Ⓓ 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 rrr Ⓑ
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ← A∧(IX + d)	Logical 'AND' of loc (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ← A∧(IY + d)	Logical 'AND' of loc (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	Z ← $(\overline{HL})_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 Ⓔ 01 bbb 110
BIT b, (IX + d)	Z ← $(\overline{IX + d})_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	Z ← $(\overline{IY + d})_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	Z ← $\overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 ⒷⒺ 01 bbb rrr
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	↕	•	•	•	11 ←cc→ 100 Ⓗ nn nnn nnn nn nnn nnn
CALL nn	(SP − 1) ← PC_H (SP − 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← $\overline{CY}$	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A − r	Compare Reg r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrr Ⓑ
CP n	A − n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A − (HL)	Compare loc (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A − (IX + d)	Compare loc (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A − (HL) HL ← HL − 1 BC ← BC − 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A − (HL) HL ← HL − 1 BC ← BC − 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

Instruction Set (Cont.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OPCODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	↕	↕	P	↕	•	↕	00 100 111
DEC r	r ← r – 1	Decrement Reg r		4	•	↕	V	↕	1	↕	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc (HL)		11	•	↕	V	↕	1	↕	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc (IX + d)		23	•	↕	V	↕	1	↕	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc (IY + d)		23	•	↕	V	↕	1	↕	11 111 101 00 110 101 dd ddd ddd
DEC IX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄— e-2 —►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF, AF	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg r with input from device (C)	2	12	•	↕	P	↕	0	↕	11 101 101① 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	↕	V	↕	0	↕	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	↕	V	↕	0	↕	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	↕	V	↕	0	↕	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg r	1	4	•	↕	V	↕	0	↕	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	↕③	X	X	1	X	11 101 101 10 101 010

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Instruction Set (Cont.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO BYTES	NO T STATES	FLAGS C	Z	P/V	S	N	H	OPCODE 76 543 210
INDR	(HL) ← (C) B ← B – 1 HL ← HL – 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B – 1 HL ← HL + 1	Load location (HL) with input from port (C), and increment HL and decrement B	2	16	•	↕③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B – 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met 12, if not	•	•	•	•	•	•	00 111 000 ←e-2→
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ←e-2→
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ←e-2→
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z ≠ 0)	2	7	•	•	•	•	•	•	00 100 000 ←e-2→
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ←e-2→
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg r	1	7	•	•	•	•	•	•	01 110 rrrⒷ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg r	3	19	•	•	•	•	•	•	11 011 101Ⓑ 01 110 rrr dd ddd ddd

Instruction Set (Cont.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO BYTES	NO T STATES	FLAGS C	Z	P/V	S	N	H	OPCODE 76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	r ← r'	Load Reg r with Reg r	1	4	•	•	•	•	•	•	01 rrr r'r' Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL - 1 BC ← BC - 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL - 1 BC ← BC 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	Load location (DE) with location (HL), increment DE, HL, decrement BC	2	16	•	•	↕ ①	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL, decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 − A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

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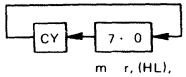
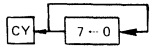
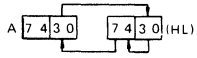
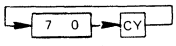
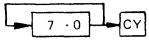
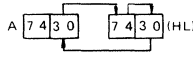
Instruction Set (Cont.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO BYTES	NO T STATES	FLAGS C	Z	P/V	S	N	H	OPCODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← AV r	Logical 'OR' of Reg r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr (B)
OR n	A ← AV n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← AV (HL)	Logical 'OR' of loc (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d)	Logical 'OR' of loc (IX + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← AV (IY + d)	Logical 'OR' of loc (IY + d) ∧ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	•	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = 0	•	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg r	2	12	•	•	•	•	•	•	11 101 101 (B) 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	? (3)	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	? (3)	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 (G)
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 (G)
RES b, r	S_b ← 0	Reset Bit b of Reg r		8	•	•	•	•	•	•	11 001 011 (B) 10 bbb rrr (E)
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc (HL)		15	•	•	•	•	•	•	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 cc 000 (H)
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 010 rrr
RL (HL)		Rotate left through carry loc (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)		Rotate left through carry loc (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)	m r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

Instruction Set (Cont.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO BYTES	NO T STATES	FLAGS C	Z	P/V	S	N	H	OPCODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m – r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg r left circular	2	8	↕	↕	P	↕	0	0	11 001 011 (B) 00 000 rrr
RLCA		Rotate left circular ACC	1	4	↕	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 011 rrr
RR (HL)		Rotate right through carry loc (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m – r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	•	•	•	0	0	00 011 111
RRC r		Rotate Reg r right circular		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 001 rrr
RRC (HL)		Rotate loc (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	 m – r, (HL), (IX + d), (IY + d), A	Rotate loc (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 100 111
RST_t	(SP 1) ← PC_H (SP 2) ← PC_L PC_H ← 0, PC_L ← T	Restart to location T	1	11	•	•	•	•	•	•	11 ttt 111
SBC A, r	A ← A – r – CY	Subtract Reg r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 rrr (B)
SBC A, n	A ← A – n – CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 nn nnn nnn
SBC A, (HL)	A ← A – (HL) – CY	Sub loc (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A – (IX + d) – CY	Subtract loc (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A – (IY + d) – CY	Subtract loc (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL – ss – CY	Subtract Reg pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101 (A) 01 ss0 010
SCF	CY ← 1	Set carry flag (C ← 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	$(HL)_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 bbb 110
SET b, (IX + d)	$(IX + d)_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 bbb 110

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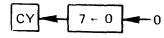
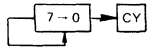
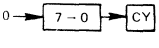
Instruction Set (Cont.)

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO BYTES	NO T STATES	FLAGS C	Z	P/V	S	N	H	OPCODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)		Shift loc (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SLA (IY + d)		Shift loc (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)		Shift loc (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
	m ≡ r, (HL), (IX + d), (IY + d)										
SRA (IY + d)		Shift loc (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)		Shift loc (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
	m – r, (HL), (IX + d), (IY + d)										
SRL (IY + d)		Shift loc (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A – r	Subtract Reg r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A – n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A – (HL)	Subtract loc (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A – (IX + d)	Subtract loc (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A – (IY + d)	Subtract loc (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	A ← A∀r	Exclusive 'OR' Reg r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	A ← A∀n	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	A ← A∀ (HL)	Exclusive 'OR' loc (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	A ← A∀ (IX + d)	Exclusive 'OR' loc (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	A ← A∀ (IY + d)	Exclusive 'OR' loc (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES.

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS

• = Flag not affected

0 = Flag reset

1 = Flag set

X = Flag unknown

↕ = Flag affected according to result of operation

V = Overflow set

P = Parity set

IFF = Interrupt flip-flop set

Ⓐ

Reg	s s
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	r r
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION

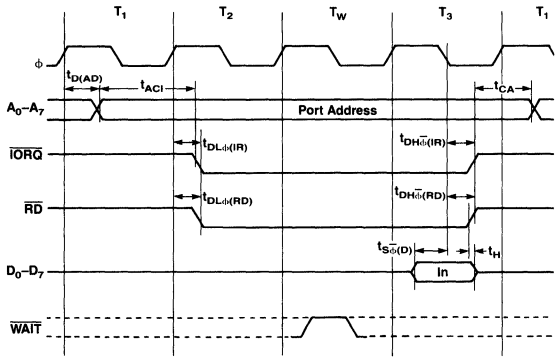
C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

Timing Waveforms

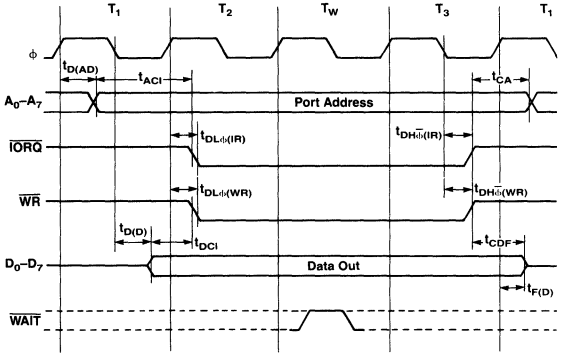
Input and output cycles

In I/O operations, a single wait state (T_W) is automatically included to provide adequate time for an I/O port to decode the address from the port address lines and initiate a wait condition if needed.

Input Cycle



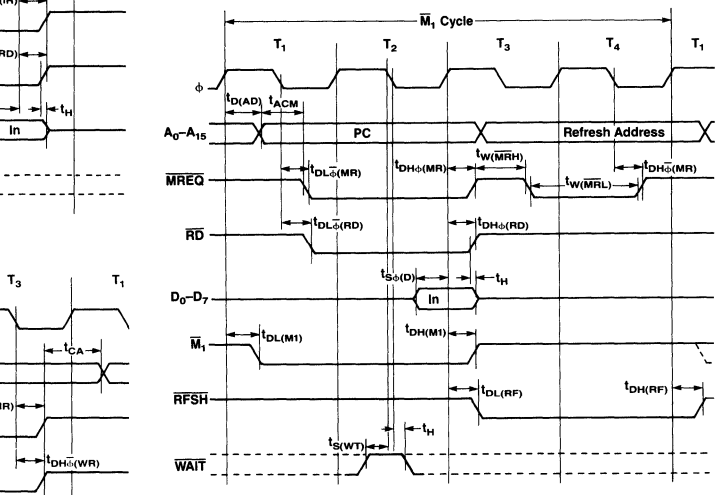
Output Cycle



Opcode fetch instruction cycle

At the beginning of the cycle, the contents of the program counter are placed on the address bus. After approximately one-half cycle, $\overline{MREQ}$ is asserted and its falling edge can be used directly by the external memory as a chip enable signal. The data from the external memory can be gated onto the data bus when $\overline{RD}$ is asserted. The CPU reads the data at the rising edge of T_3. During T_3 and T_4, external dynamic memory is refreshed while the instruction is decoded and executed. The assertion of $\overline{RFSH}$ indicates that the external dynamic memory requires a refresh read.

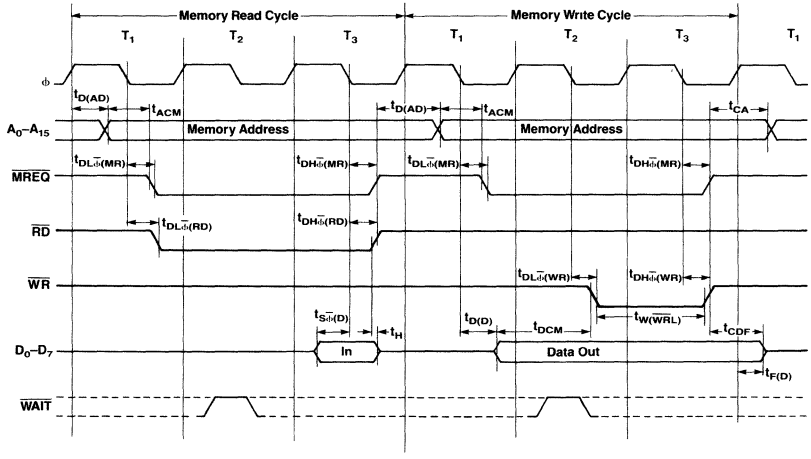
$\overline{M_1}$ Cycle



Timing Waveforms (Cont.)

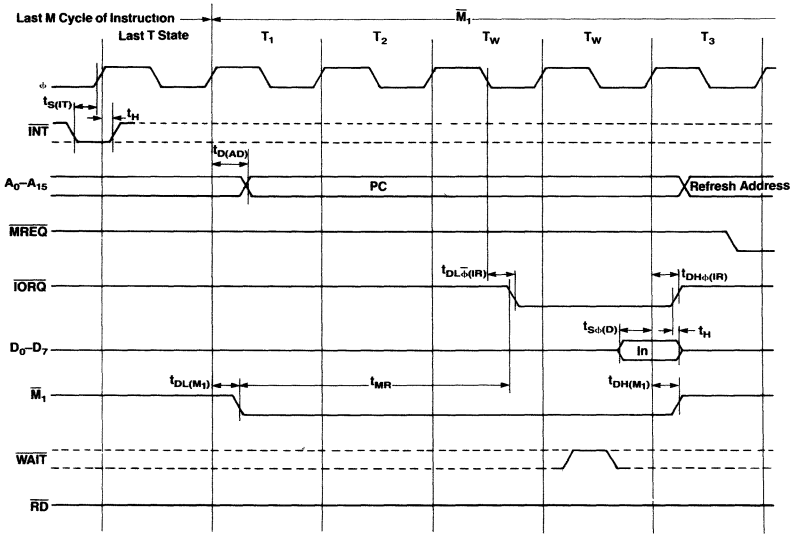
Memory read or write cycles

In read and write operations, the $\overline{MREQ}$ and $\overline{RD}$ signals function the same as they do in opcode fetch operations. In a write operation $\overline{MREQ}$ is asserted and can be used directly by external memory as a chip enable signal when information on the address bus is stable. The $\overline{WR}$ signal is used as a write strobe to almost any type of semiconductor memory, and is asserted when data on the data bus is stable.



Interrupt request/acknowledge cycle

The interrupt signal is sampled at the rising edge of the final clock pulse at the end of an instruction. When an interrupt is accepted, an $\overline{M_1}$ cycle is begun. Instead of $\overline{MREQ}$, $\overline{IORQ}$ is asserted during this cycle to indicate that an 8-bit vector address can be placed on the data bus by the interrupting device. This cycle includes the automatic addition of two wait states to facilitate the implementation of a daisy-chain priority interrupt protocol.



Standard Test Conditions

The standard test conditions reference all voltages to ground (0V) and follow the convention that positive current flows into the referenced pin. The listing of AC parameters is based on a load capacitance of 50pF unless explicitly stated otherwise. For every 50pF increase in load capacitance there is a 10ns delay, up to a maximum increase of 200pF for the data bus and 100pF for the address bus and the bus control lines.

The operating temperature range is: 0°C to +70°C; $+4.75V \leq V_{CC} \leq +5.25V$.

Absolute Maximum Ratings*

T_a = 25°C

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin	−0.3V to +7V①
Power Dissipation	1.5w

Note: ① With respect to ground

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = 0°C to +70°C; V_{CC} = +5V ±5% unless otherwise specified.

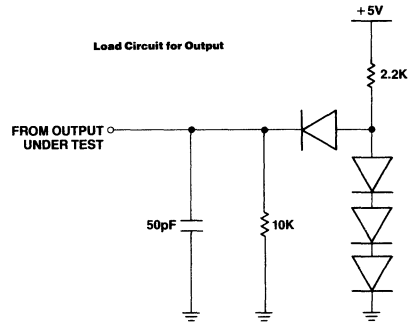
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Input Low Voltage	V_{ILC}	−0.3		0.45	V	
Clock Input High Voltage	V_{IHC}	V_{CC} −0.6		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.3		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.8mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −250μA
Power Supply Current μPD780	I_{CC}			150	mA	t_C = 400ns
Power Supply Current μPD780-1	I_{CC}		90	200	mA	t_C = 250ns
Input Leakage Current	I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
Three-state Output Leakage Current in Float	I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{CC}
Three-state Output Leakage Current in Float	I_{LOL}			−10	μA	V_{OUT} = 0.4V
Data Bus Leakage Current in Input Mode	I_{LD}			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

T_a = 25°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Capacitance	C_{ϕ}			35	pF	f_c = 1MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured pins
Output Capacitance	C_{OUT}			10	pF	returned to ground.

Load Circuit for Output



5

AC Characteristics

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

Parameter	Symbol	Limits μPD780 Min	Limits μPD780 Max	Limits μPD780-1 Min	Limits μPD780-1 Max	Limits μPD780-2 Min	Limits μPD780-2 Max	Unit	Test Conditions
Clock Period	t_C	0.4	①	0.25	①	0.165	①	μs	
Clock Pulse Width, Clock High	$t_W(\phi H)$	180	②	110	②	65	②	ns	
Clock Pulse Width, Clock Low	$t_W(\phi L)$	180	2000	110	2000	65	2000	ns	
Clock Rise and Fall Time	t_{Rf}		30		30		20	ns	
Address Output Delay	$t_{D(AD)}$		145		110		90	ns	
Delay to Float	$t_{F(AD)}$		110		90		80	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{ACM}	③		③		③		ns	
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{ACI}	④		④		④		ns	C_L = 50pF
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{CA}	⑤		⑤		⑤		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ during Float	t_{CAF}	⑥		⑥		⑥		ns	
Data Output Delay	$t_{D(D)}$		230		150		130	ns	
Delay to Float during Write Cycle	$t_{F(D)}$		90		90		80	ns	
Data Setup Time to Rising Edge of Clock during M_1 Cycle	$t_{S\phi(D)}$	50		35		30		ns	
Data Setup Time to Falling Edge of Clock during M_2 to M_5 Cycles	$t_{S\bar{\phi}(D)}$	60		50			40	ns	C_L = 200pF
Data Stable prior to $\overline{WR}$ (Memory Cycle)	t_{DCM}	⑦		⑦		⑦		ns	
Data Stable prior to $\overline{WR}$ (I/O Cycle)	t_{DCI}	⑧		⑧		⑧		ns	
Data Stable from $\overline{WR}$	t_{CDF}	⑨		⑨		⑨		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{S(BQ)}$	80		50		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100		90	ns	C_L = 50pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100		90	ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80		70	ns	
$\overline{M_1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{MR}	⑩		⑩		⑩		ns	
Any Hold Time for Setup Time	t_H	0			0		0	ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300		260	ns	C_L = 50pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{S(IT)}$	80		80		70		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\phi(IR)}$		90		75		65	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\bar{\phi}(IR)}$		110		85		70	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\phi(IR)}$		100		85		70	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\bar{\phi}(IR)}$		110		85		70	ns	C_L = 50pF
$\overline{M_1}$ Delay from Rising Edge of Clock to $\overline{M_1}$ Low	$t_{DL(M_1)}$		130		100		80	ns	
$\overline{M_1}$ Delay from Rising Edge of Clock to $\overline{M_1}$ High	$t_{DH(M_1)}$		130		100		80	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\bar{\phi}(MR)}$		100		85		70	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\phi(MR)}$		100		85		70	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\bar{\phi}(MR)}$		100		85		70	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(MRL)}$	⑪		⑪		⑪		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(MRH)}$	⑫		⑫		⑫		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{W(NMI)}$	80		80		70		ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{S(RS)}$	90		60		60		ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\phi(RD)}$		100		85		70	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\bar{\phi}(RD)}$		130		95		80	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\phi(RD)}$		100		85		70	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\bar{\phi}(RD)}$		110		85		70	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130		110	ns	C_L = 30pF
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120		100	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{S(WT)}$	70		70		60		ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\phi(WR)}$		80		65		60	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\bar{\phi}(WR)}$		90		80		70	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\bar{\phi}(WR)}$		100		80		70	ns	
Pulse Width to $\overline{WR}$ Low	$t_{W(WRL)}$	⑬		⑬		⑬		ns	

Notes:
① $t_C = t_W(\phi H) + t_W(\phi L) + t_R + t_F$
② Though the structure of the 780 is static, 200μs is a guaranteed maximum
③ $t_{ACM} = t_W(\phi H) + t_F - 65$ (75)* (50)**
④ $t_{ACI} = t_C - 70$ (80)* (55)**
⑤ $t_{CA} = t_W(\phi L) + t_R - 50$ (40)* (50)**
⑥ $t_{CAF} = t_W(\phi L) + t_R - 45$ (60)* (40)**
⑦ $t_{DCM} = t_C - 170$ (210)* (140)**
⑧ $t_{DCI} = t_W(\phi L) + t_R - 170$ (210)* (140)**
⑨ $t_{CDF} = t_W(\phi L) + t_R - 70$ (80)* (55)**
⑩ $t_{MR} = 2t_C + t_W(\phi H) + t_F - 65$ (80)* (50)**
⑪ $t_W(MRL) = t_C - 30$ (40)* (30)**
⑫ $t_W(MRH) = t_W(\phi H) + t_F - 20$ (30)* (20)**
⑬ $t_W(WR) = t_C - 30$ (40)* (30)**

* These values apply to the μPD780
** These values apply to the μPD780-2

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD780C
Ceramic, μPD780D

μPD8085A SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

DESCRIPTION

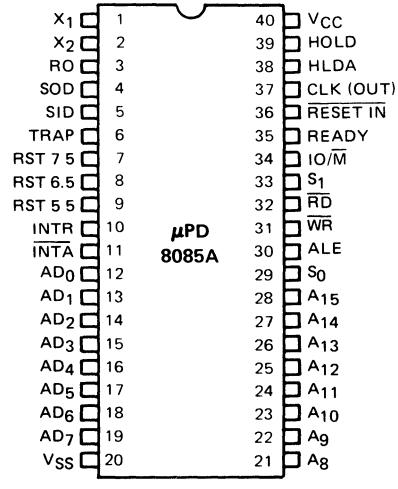
The μPD8085A is a single chip 8-bit microprocessor which is 100 percent software compatible with the industry standard 8080A. It has the ability of increasing system performance of the industry standard 8080A by operating at a higher speed Using the μPD8085A in conjunction with its family of ICs allows the designer complete flexibility with minimum chip count.

FEATURES

- Single Power Supply: +5 Volt, ±10%
- Internal Clock Generation and System Control
- Internal Serial In/Out Port.
- Fully TTL Compatible
- Internal 4-Level Interrupt Structure
- Multiplexed Address/Data Bus for Increased System Performance
- Complete Family of Components for Design Flexibility
- Software Compatible with Industry Standard 8080A
- Higher Throughput. μPD8085AH – 3 MHz
  μPD8085A-2 – 5 MHz
- Available in Either Plastic or Ceramic Package

5

PIN CONFIGURATION



Rev/5

FUNCTIONAL DESCRIPTION

The μPD8085A contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8085A also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8085A has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8085A also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

The μPD8085A was designed with speed and simplicity of the overall system in mind. The multiplexed address/data bus increases available pins for advanced functions in the processor and peripheral chips while providing increased system speed and less critical timing functions. All signals to and from the μPD8085A are fully TTL compatible.

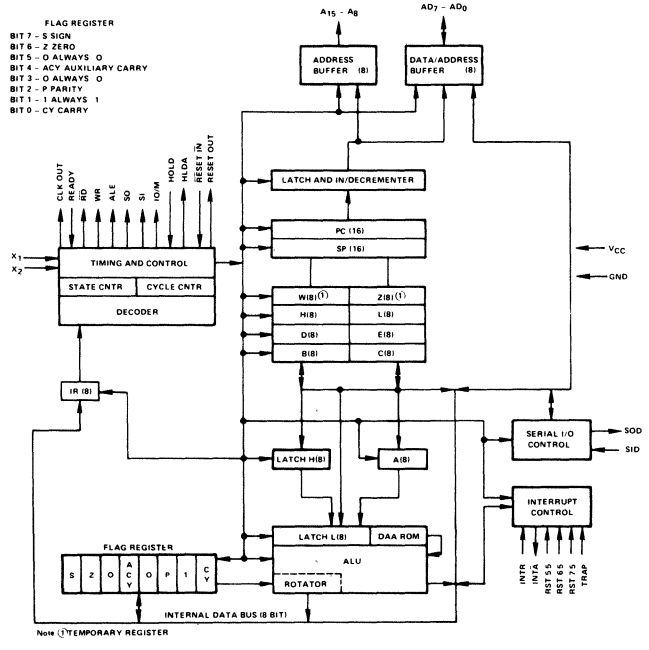
The internal interrupt structure of the μPD8085A features 4 levels of prioritized interrupt with three levels internally maskable.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address, data and control lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8085A features internal clock generation with status outputs available for advanced read/write timing and memory/IO instruction indications. The clock may be crystal controlled, RC controlled, or driven by an external signal.

On chip serial in/out port is available and controlled by the newly added RIM and SIM instructions.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO	SYMBOL	NAME	FUNCTION
1, 2	X_1, X_2	Crystal In	Crystal, RC, or external clock input
3	RO	Reset Out	Acknowledge that the processor is being reset to be used as a system reset
4	SOD	Serial Out Data	1 bit data out by the SIM instruction
5	SID	Serial In Data	1 bit data into ACC bit 7 by the RIM instruction
6	Trap	Trap Interrupt Input	Highest priority nonmaskable restart interrupt
7 8 9	RST 7 5 RST 6 5 RST 5 5	Restart Interrupts	Priority restart interrupt inputs, of which 7 5 is the highest and 5 5 the lowest priority
10	INTR	Interrupt Request In	A general interrupt input which stops the PC from incrementing, generates $\overline{INTA}$, and samples the data bus for a restart or call instruction
11	$\overline{INTA}$	Interrupt Acknowledge	An output which indicates that the processor has responded to INTR
12-19	$AD_0 - AD_7$	Low Address/Data Bus	Multiplexed low address and data bus
20	V_{SS}	Ground	Ground Reference
21-28	$A_8 - A_{15}$	High Address Bus	Nonmultiplexed high 8-bits of the address bus
29, 33	S_0, S_1	Status Outputs	Outputs which indicate data bus status Halt, Write, Read, Fetch
30	ALE	Address Latch Enable Out	A signal which indicates that the lower 8-bits of address are valid on the AD lines
31, 32	$\overline{WR}$, $\overline{RD}$	Write/Read Strobes Out	Signals out which are used as write and read strobes for memory and I/O devices
34	IO/$\overline{M}$	I/O or Memory Indicator	A signal out which indicates whether $\overline{RD}$ or $\overline{WR}$ strobes are for I/O or memory devices
35	Ready	Ready Input	An input which is used to increase the data and address bus access times (can be used for slow memory)
36	$\overline{Reset\ In}$	Reset Input	An input which is used to start the processor activity at address 0, resetting IE and HLDA flip flops
37	CLK	Clock Out	System Clock Output
38, 39	HLDA, HOLD	Hold Acknowledge Out and Hold Input Request	Used to request and indicate that the processor should relinquish the bus for DMA activity When hold is acknowledged, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, Address and Data busses are all 3 stated
40	V_{CC}	5V Supply	Power Supply Input

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts
Power Dissipation	1.5W

T_a = 25°C; V_{CC} = ±5V ± 5%, 8085A-2

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = GND, unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS} - 0 5	V_{SS} + 0 8	V	
Input High Voltage	V_{IH}	2 0	V_{CC} + 0 5	V	
Output Low Voltage	V_{OL}		0 45	V	I_{OL} = 2 mA on all outputs
Output High Voltage	V_{OH}	2 4		V	I_{OH} = -400 μs ①
Power Supply Current (V_{CC})	I_{CC} (AV)		170	mA	t_{CY} min (8085A-2)
Maximum Unit Test			135	mA	t_{CY} min (8085AH)
Input Leakage	I_{IL}		±10 ①	μA	$0 \leq V_{IN} \leq V_{CC}$
Output Leakage	I_{LO}		±10 ①	μA	$0\ 45V \leq V_{OUT} \leq V_{CC}$
Input Low Level, Reset	V_{ILR}	-0 5	+0 8	V	
Input High Level, Reset	V_{IHR}	2 4	V_{CC} + 0 5	V	
Hysteresis, Reset	V_{HY}	0 25		V	
X_1, X_2 Input Voltage High	V_{IHX}	4.0	V_{CC} + 0 5	V	

Note ① Minus (−) designates current flow out of the device

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%, 8085A-2

PARAMETER	SYMBOL	LIMITS				UNITS
		D8085AH		μPD8085A-2		
		MIN	MAX	MIN	MAX	
CLK Cycle Period	t_{CYC}	320	2000	200	2000	ns
CLK Time Low	t_1	80		40		ns
CLK Time High	t_2	120		70		ns
CLK Rise and Fall Time	$t_{r,tf}$		30		30	ns
X_1 Rising to CLK Rising	t_{XKR}	30	120	50		ns
X_1 Rising to CLK Falling	t_{XKF}	30	150	80		ns
A_{8-15} Valid to Leading Edge of CONTROL ①	t_{AC}	270		50		ns
A_{7-0} Valid to Leading Edge of CONTROL	t_{ACL}	240		60		ns
A_{0-15} Valid to Data in	t_{AD}		575		0	ns
Address Float after Leading Edge of $\overline{RD}$($\overline{INTA}$)	t_{AFR}		0		350	ns
A_{8-15} Valid before Trailing Edge of ALE ①	t_{AL}	115			150	ns
A_{0-7} Valid before Trailing Edge of ALE	t_{ALL}	90		0		ns
READY Valid from Address Valid	t_{ARY}		220	90		ns
A_{8-15} Valid after CONTROL	t_{CA}	120		60		ns
Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}	400		230		ns
Trailing Edge of CONTROL to Leading Edge of ALE	t_{CL}	50		25		ns
Data Valid to Trailing Edge of $\overline{WR}$	t_{DW}	420			100	ns
HLDA to Bus Enable	t_{HABE}		210		150	ns
Bus Float After HLDA	t_{HABF}		210		150	ns
HLDA Valid to Trailing Edge of CLK	t_{HACK}	110		40		ns
HOLD Hold Time	t_{HDH}	0				ns
HOLD Setup Time to Trailing Edge of CLK	t_{HDS}	170				ns
INTR Hold Time	t_{INH}	0				ns
INTR,RST,TRAP Setup Time to Failing Edge of CLK	t_{INS}	160		220		ns
Address Hold Time After ALE	t_{LA}	100		115		ns
Trailing Edge of ALE to Leading Edge of CONTROL	t_{LC}	130		120		ns
ALE Low Time during CLK High	t_{LCK}	100		0		ns
ALE to Valid Data in during Read	t_{LDR}		460		270	ns
ALE to Valid Data during Write	t_{LDW}		200	0		ns
ALE Pulse Width	t_{LL}	140		30	100	ns
ALE to READY stable	t_{LRY}		110	30	110	ns
Trailing Edge of $\overline{RD}$ to Re-enabling of Address	t_{RAE}	150			20	ns
$\overline{RD}$ (or $\overline{INTA}$) to Valid Data	t_{RD}		300	50		ns
Trailing Edge of CONTROL to Leading Edge of next CONTROL	t_{RV}	400		50		ns
Data Hold Time after $\overline{RD}$ ($\overline{INTA}$)(7)	t_{RDH}	0			120	ns
READY Hold Time	t_{RYH}	0			30	ns
READY Set up Time to Leading Edge of CLK	t_{RYS}	110		115		ns
Leading Edge Data Valid After Trailing Edge of $\overline{WR}$	t_{WD}	100		40		ns
Leading Edge of $\overline{WR}$ to Data Valid	t_{WDL}		40			ns

Notes: ① A8-A15 address specs apply to IO/M S0 and S1 except A8-A15 are undefined during T4-T6 of OF cycle whereas IO/M, S0 and S1 are stable

② Test Conditions t_{CYC} = 320 ns (8085AH)/200 ns (8085A-2)
C_L = 150 pF

③ For all output timing where except C_L = 150 pF use the following correction factors
25 pF C_L 150 pF −0 10 ns/pF
150 pF C_L 300 pF +0 3 ns/pF

④ Output Timings are measured with purely capacitive load

⑤ All timings are measured as the following,
Output Voltage V_L = 0 8V, V_H = 2 0V
Input Voltage 1 5V, t_r, t_f = 20 ns

⑥ To calculate timing specifications at other values of t_{CYC} use Table 1

⑦ Data hold time is guaranteed under all loading conditions

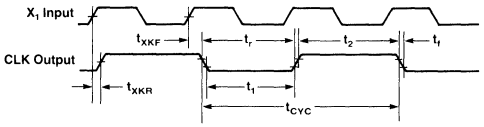
BUS TIMING SPECIFICATIONS

Tcyc as a dependent

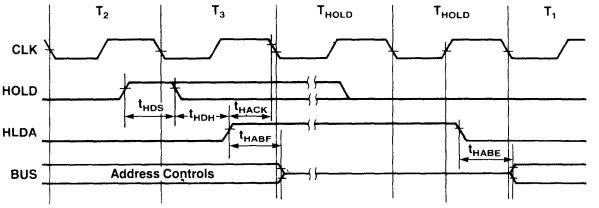
	μPD8085AH	μPD808A-2	
t_{AL}	(1/2)T − 45	(1/2)T − 50	min
t_{LA}	(1/2)T − 60	(1/2)T − 50	min
t_{LL}	(1/2)T − 20	(1/2)T − 20	min
t_{LCK}	(1/2)T − 60	(1/2)T − 50	min
T_{LC}	(1/2)T − 30	(1/2)T − 40	min
t_{AD}	(5/2 + N)T − 225	(5/2 + N)T − 150	max
t_{RD}	(3/2 + N)T − 180	(3/2+ N)T − 150	max
t_{RAE}	(1/2)T − 10	(1/2)T − 10	min
t_{CA}	(1/2)T − 40	(1/2)T − 40	min
t_{DW}	(3/2 + N)T − 60	(3/2 + N)T − 70	min
t_{WD}	(1/2)T − 60	(1/2)T − 40	min
t_{CC}	(3/2 + N)T − 80	(3/2 + N)T − 70	min
t_{CL}	(1/2)T − 110	(1/2)T − 75	min
t_{ARY}	(3/2)T − 260	(3/2)T − 200	max
t_{HACK}	(1/2)T − 50	(1/2)T − 60	min
t_{HABF}	(1/2)T + 50	(1/2)T − 50	max
t_{HABE}	(1/2)T + 50	(1/2)T − 50	max
t_{AC}	(2/2)T − 50	(2/2)T − 85	min
t_1	(1/2)T − 80	(1 /2)T − 60	min
t_2	(1/2)T − 40	(1/2)T − 30	min
t_{RV}	(3/2)T − 80	(3/2)T − 80	min
t_{LDR}	(4/2 + N)T − 180	(4/2 + N)T − 130	max

Note N = Number of WAIT State
T = t_{CYC}

Clock Timing Waveform

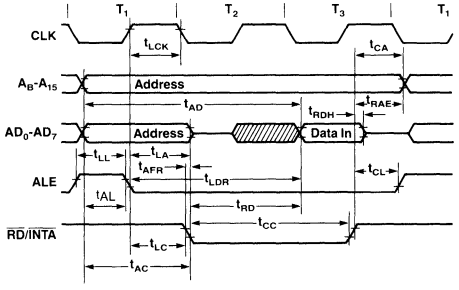


Hold Timing

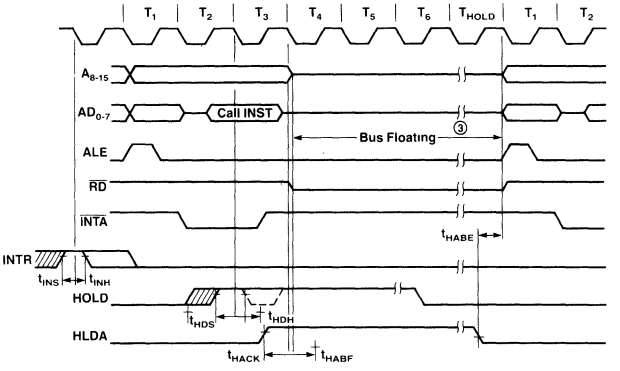


8085AH Bus Timing

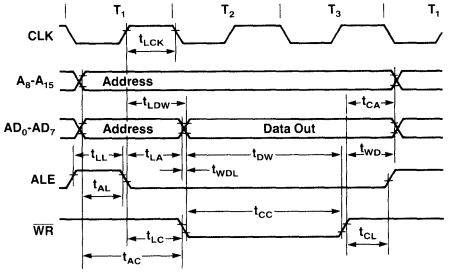
Read Operation



Interrupt and Hold Timing

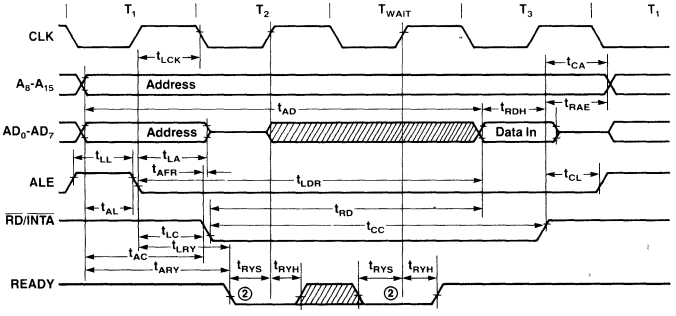


Write Operation



Read Operation with Wait Cycle

Same Ready Timing Applies To Write Operation

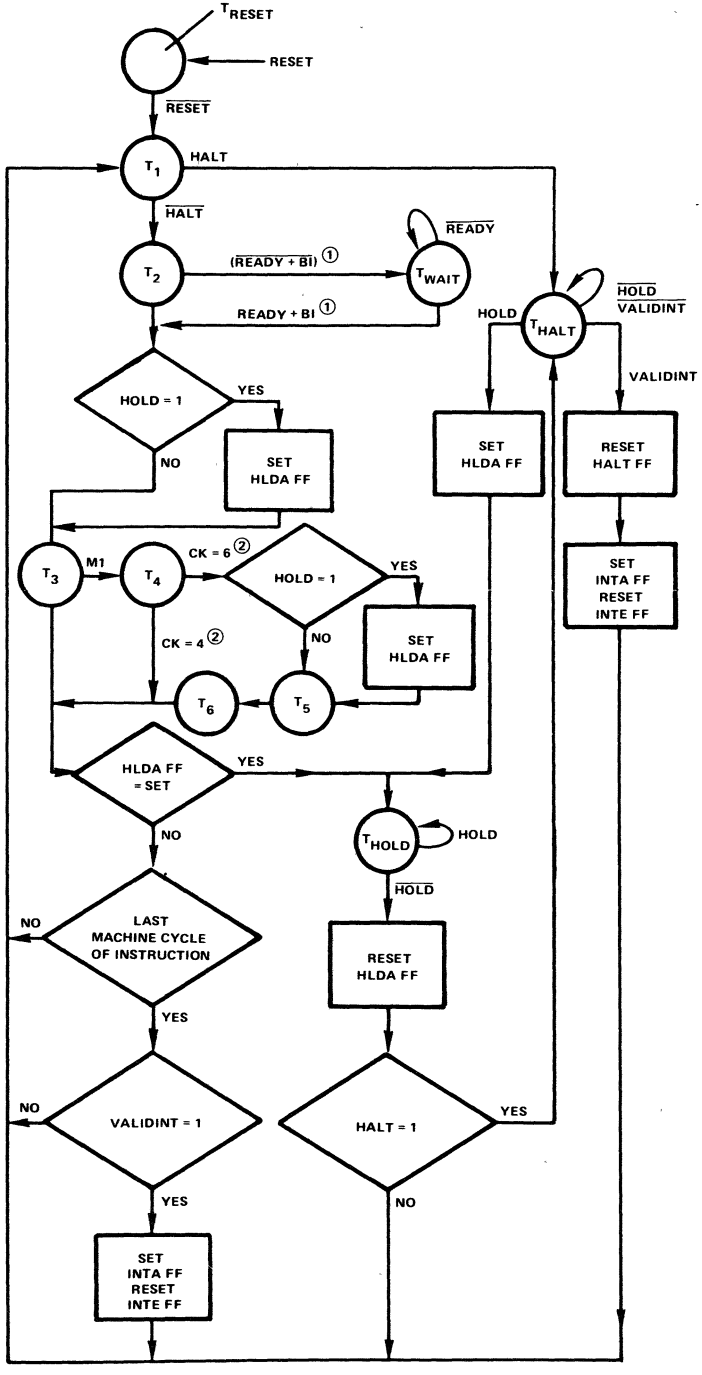


Note: ②READY must remain stable during t_{RYS} and t_{RYH}

③IO/M is also floating during this time

5

PROCESSOR STATE
TRANSITION DIAGRAM

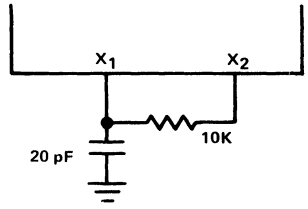


Notes: ① BI indicates that the bus is idle during this machine cycle.
② CK indicates the number of clock cycles in this machine cycle.

CLOCK INPUTS ①

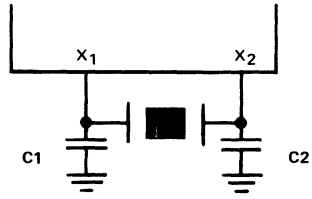
As stated, the timing for the μPD8085A may be generated in one of three ways; crystal, RC, or external clock. Recommendations for these methods are shown below.

RC



≈3 MHz Input Frequency
RC Resonance

CRYSTAL

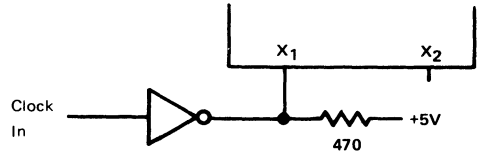


1-6 MHz Input Frequency
Parallel Resonant Crystal

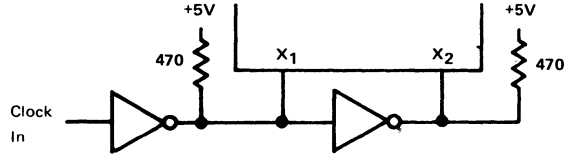
For 1-6 MHz Input Frequency,
C1 = C2 = 10 pF max.

For 6-10 MHz Input Frequency,
C1 = C2 = 5 pF max.

EXTERNAL



1-6 MHz 25-50% DC
X_2 not used



1-6 MHz > 50% DC

Note ① Input frequency must be twice the internal operating frequency

STATUS OUTPUTS

The Status Outputs are valid during ALE time and have the following meaning:

	S1	S0
Halt	0	0
Write	0	1
Read	1	0
Fetch	1	1

These pins may be decoded to portray the processor's data bus status.

INTERRUPTS

The μPD8085A has five interrupt pins available to the user. INTR is operationally the same as the 8080 interrupt request, three (3) internally maskable restart interrupts: RESTART 5.5, 6.5 and 7.5, and TRAP, a non-maskable restart.

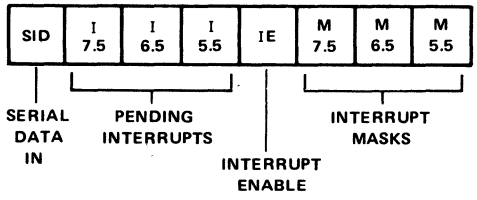
PRIORITY	INTERRUPT	RESTART ADDRESS
Highest	TRAP	24_{16}
|	RST 7.5	$3C_{16}$
|	RST 6.5	34_{16}
|	RST 5.5	$2C_{16}$
Lowest	INTR	

INTR, RST 5.5 and RST 6.5 are all level sensing inputs while RST 7.5 is set on a rising edge. TRAP, the highest priority interrupt, is non-maskable and is set on the rising edge or positive level. It must make a low to high transition and remain high to be seen, but it will not be generated again until it makes another low to high transition.

SERIAL I/O

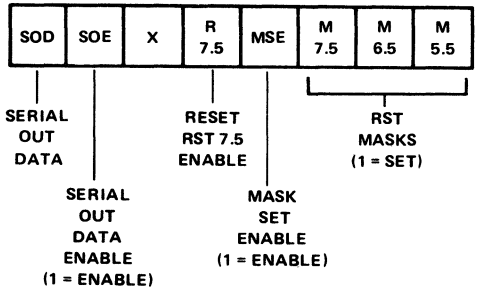
Serial input and output is accomplished with two new instructions not included in the 8080: RIM and SIM. These instructions serve several purposes: serial I/O, and reading or setting the interrupt mask.

The RIM (Read Interrupt Mask) instruction is used for reading the interrupt mask and for reading serial data. After execution of the RIM instruction the ACC content is as follows:



Note: After the TRAP interrupt, the RIM instruction must be executed to preserve the status of IE.

The SIM (Set Interrupt Mask) instruction is used to program the interrupt mask and to output serial data. Presetting the ACC for the SIM instruction has the following meaning:



INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also, the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8085A has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8085A. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8085A instruction set.

Two instructions, RIM and SIM, are used for reading and setting the internal interrupt mask as well as input and output to the serial I/O port.

The special instruction group completes the μPD8085A instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

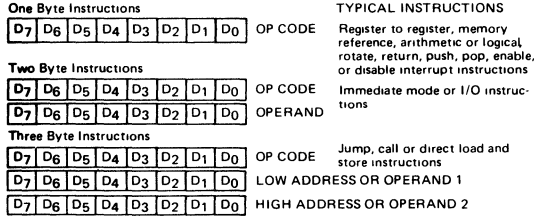
DATA AND INSTRUCTION FORMATS

Data in the μPD8085A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.



INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d s	Move register to register	0	1	d	d	d	s	s	s	4				
MOV M s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	4	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	4	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR Memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU ROTATE														
RLC	Rotate A left MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	7/10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	7/10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	7/10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	7/10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	7/10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	7/10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	7/10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	7/10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	18				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	9/18				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	9/18				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	9/18				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	9/18				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	9/18				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	9/18				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	9/18				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	9/18				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	6/12				
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12				
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12				
RC	Return on carry	1	1	0	1	1	0	0	0	6/12				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12				
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12				
RP	Return on positive	1	1	1	1	0	0	0	0	6/12				
RM	Return on minus	1	1	1	1	1	0	0	0	6/12				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	12				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	12				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	12				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	6				
INX D	Increment DE	0	0	0	1	0	0	1	1	6				
INX H	Increment HL	0	0	1	0	0	0	1	1	6				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	6				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	6				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	6				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	6				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	6				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	16				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	6				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	6				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4				
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4				
RST A	Restart	1	1	A	A	A	1	1	1	12				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				CY
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	5				

Notes

[1] Operand Symbols used
- A : 8 bit address or expression
- s : source register
- d : destination register
- PSW : Processor Status Word
- SP : Stack Pointer
- D8 : 8 bit data quantity expression, or constant, always B_2 of instruction
- D16 : 16 bit data quantity, expression or constant, always B_3B_2 of instruction
- ADDR : 16 bit Memory address expression

[2] ddd or sss : 000 B 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A

[3] Two possible cycle times (7/10) indicate instruction cycles dependent on condition flags

[4]
- • flag affected
- flag not affected
- 0 = flag reset
- 1 flag set

INSTRUCTION CYCLE TIMES

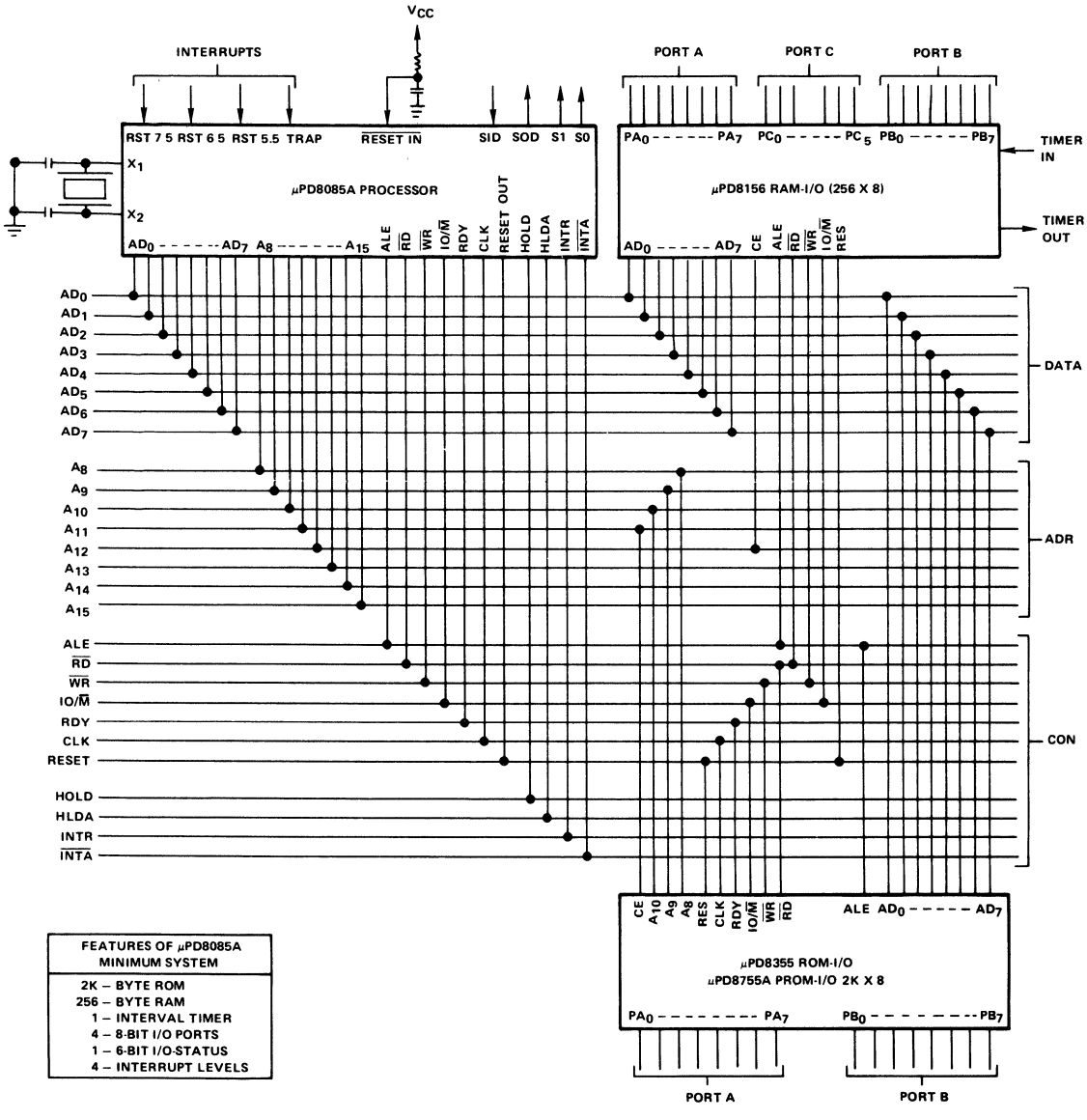
One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$).

Machine cycles and clock states used for each type of instruction are shown below.

INSTRUCTION TYPE	MACHINE CYCLES EXECUTED MIN/MAX	CLOCK STATUS MIN/MAX
ALU R	1	4
CMC	1	4
CMA	1	4
DAA	1	4
DCR R	1	4
DI	1	4
EI	1	4
INR R	1	4
MOV R, R	1	4
NOP	1	4
ROTATE	1	4
RIM	1	4
SIM	1	4
STC	1	4
XCHG	1	4
HLT	1	5
DCX	1	6
INX	1	6
PCHL	1	6
RET COND.	1/3	6/12
SPHL	1	6
ALU I	2	7
ALU M	2	7
JNC	2/3	7/10
LDAX	2	7
MVI	2	7
MOV M, R	2	7
MOV R, M	2	7
STAX	2	7
CALL COND.	2/5	9/18
DAD	3	10
DCR M	3	10
IN	3	10
INR M	3	10
JMP	3	10
LOAD PAIR	3	10
MVI M	3	10
OUT	3	10
POP	3	10
RET	3	10
PUSH	3	12
RST	3	12
LDA	4	13
STA	4	13
LHLD	5	16
SHLD	5	16
XTHL	5	16
CALL	5	18

A minimum computer system consisting of a processor, ROM, RAM, and I/O can be built with only 3-40 pin packs. This system is shown below with its address, data, control busses and I/O ports.

μPD8085A FAMILY MINIMUM SYSTEM CONFIGURATION



FEATURES OF μPD8085A MINIMUM SYSTEM
2K – BYTE ROM
256 – BYTE RAM
1 – INTERVAL TIMER
4 – 8-BIT I/O PORTS
1 – 6-BIT I/O-STATUS
4 – INTERRUPT LEVELS

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8085AC/AHC
Ceramic, μPD8085AD
Cerdip, μPD8085AD AHD

16-BIT MICROPROCESSOR

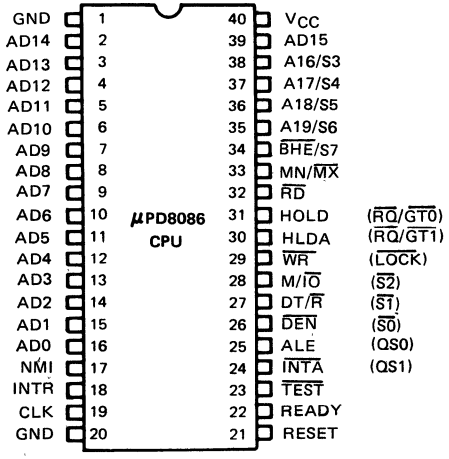
DESCRIPTION

The μPD8086 is a 16-bit microprocessor that has both 8-bit and 16-bit attributes. It has a 16-bit wide physical path to memory for high performance. Its architecture allows higher throughput than the 5 MHz μPD8085A-2.

FEATURES

- Can Directly Address 1 Megabyte of Memory
- Fourteen 16-Bit Registers with Symmetrical Operations
- Bit, Byte, Word, and Block Operations
- 8- and 16-Bit Signed and Unsigned Arithmetic Operations in Binary or Decimal
- Multiply and Divide Instructions
- 24 Operand Addressing Modes
- Assembly Language Compatible with the μPD8080/8085
- Complete Family of Components for Design Flexibility

PIN CONFIGURATION



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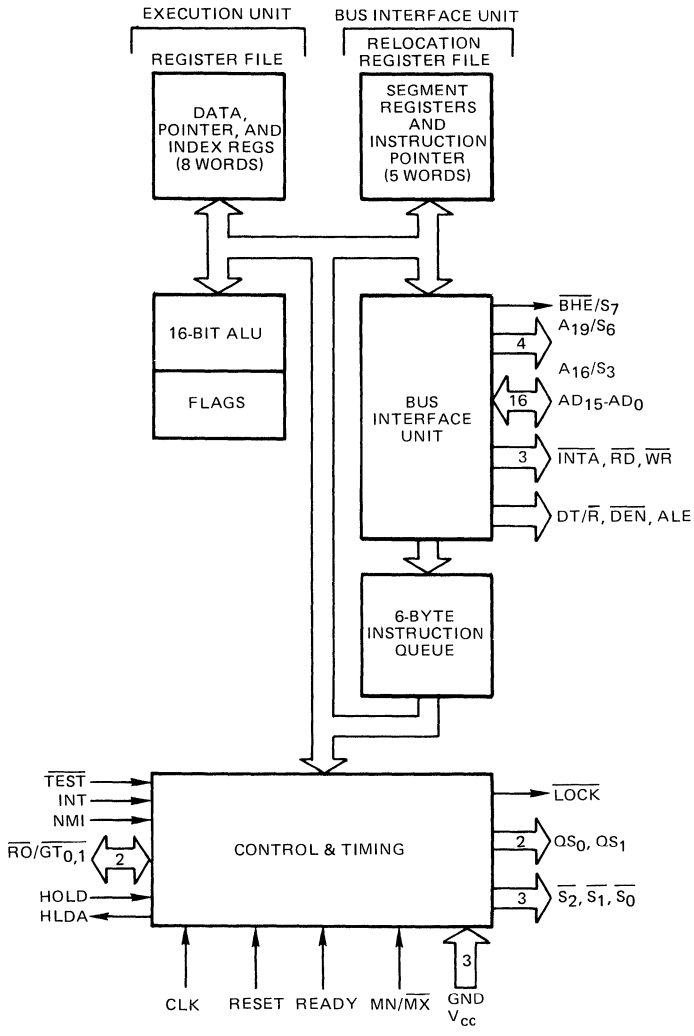
*Preliminary

PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
2-16, 39	AD0-AD15	Address/Data Bus	Multiplexed address (T_1) and data (T_2, T_3, T_W, T_4) bus. 8-bit peripherals tied to the lower 8 bits, use A0 to condition chip select functions. These lines are tri-state during interrupt acknowledge and hold states.
17	NMI	Non-Maskable Interrupt	This is an edge triggered input causing a type 2 interrupt. A look-up table is used by the processor for vectoring information.
18	INTR	Interrupt Request	A level triggered input sampled on the last clock cycle of each instruction. Vectoring is via an interrupt look-up table. INTR can mask in software by resetting the interrupt enable bit.
19	CLK	Clock	The clock input is a 1/3 duty cycle input basic timing for the processor and bus controller.
21	RESET	Reset	This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.
22	READY	Ready	An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.
23	$\overline{TEST}$	Test	This input is examined by the "WAIT" instruction, and if low, execution continues. Otherwise the processor waits in an "Idle" state. Synchronized by the processor on the leading edge of CLK.
24	$\overline{INTA}$	Interrupt Acknowledge	This is a read strobe for reading vectoring information. During T_2, T_3, and T_W of each interrupt acknowledge cycle it is low.
25	ALE	Address Latch Enable	This is used in conjunction with the μPD8282/8283 latches to latch the address, during T_1 of any bus cycle.
26	$\overline{DEN}$	Data Enable	This is the output enable for the μPD8282/8287 transceivers. It is active low during each memory and I/O access and INTA cycles.
27	DT/$\overline{R}$	Data Transmit/Receive	Used to control the direction of data flow through the transceivers.
28	M/$\overline{IO}$	Memory/IO Status	This is used to separate memory access from I/O access.
29	$\overline{WR}$	Write	Depending on the state of the M/$\overline{IO}$ line, the processor is either writing to I/O or memory.
30	HLDA	Hold Acknowledge	A response to the HOLD input, causing the processor to tri-state the local bus. The bus return active one cycle after HOLD goes back low.
31	HOLD	Hold	When another device requests the local bus, driving HOLD high, will cause the μPD8086 to issue a HLDA.
32	$\overline{RD}$	Read	Depending on the state of the M/$\overline{IO}$ line, the processor is reading from either memory or I/O.
33	MN/$\overline{MX}$	Minimum/Maximum	This input is to tell the processor which mode it is to be used in. This effects some of the pin descriptions.
34	$\overline{BHE}$/S_7	Bus/High Enable	This is used in conjunction with the most significant half of the data bus. Peripheral devices on this half of the bus use BHE to condition chip select functions.
35-38	A16-A19	Most Significant Address Bits	The four most significant address bits for memory operations. Low during I/O operations.
26, 27, 28 34-38	S_0-S_7	Status Outputs	These are the status outputs from the processor. They are used by the μPD8288 to generate bus control signals.
24, 25	QS_1, QS_0	Que Status	Used to track the internal μPD8086 instruction que.
29	$\overline{LOCK}$	Lock	This output is set by the "LOCK" instruction to prevent other system bus masters from gaining control.
30, 31	$\overline{RQ}/\overline{GT_0}$ $\overline{RQ}/\overline{GT_1}$	Request/Grant	Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . -1.0 to +7V
Power Dissipation 2.5W

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	+0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2.5 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = -400 μA
Power Supply Current μPD8086/ μPD8086-2	I_{CC}		 340 350	 mA mA	$T_a = 25°C$
Input Leakage Current	I_{LI}		±10	μA	$0V < V_{IN} < V_{CC}$
Output Leakage Current	I_{LO}		±10	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
Clock Input Low Voltage	V_{CL}	-0.5	+0.6	V	
Clock Input High Voltage	V_{CH}	3.9	V_{CC} + 1.0	V	
Capacitance of Input Buffer (All input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IN}		15	pF	fc = 1 MHz
Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	C_{IO}		15	pF	fc = 1 MHz

AC CHARACTERISTICS

μPD8086: $T_a = 0°C$ to $70°C$; $V_{CC} = 5V \pm 10\%$

MINIMUM COMPLEXITY SYSTEM

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1.0V to 3.5V
CLK Fall Time	TCL2CL1		10		10	ns	From 3.5V to 1.0V
Data In Setup Time	TDVCL	30		20		ns	
Data In Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ① ②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ① ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) –15		(2/3 TCLCL) –15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY Inactive to CLK ③	TRYLCL	–8		–8		ns	
HOLD Setup Time	THVCH	35		20		ns	
INTR, NMI, $\overline{TEST}$ Setup Time ②	TINVCH	30		15		ns	
Input Rise Time	TILIH		20			ns	From 0.8V to 2.0V
Input Fall Time	TIHIL		12			ns	From 2.0V to 0.8V

TIMING RESPONSES

TIMING RESPONSES

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Address Valid Delay	TCLAV	10	110	10	60		
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
ALE Width	TLHLL	TCLCH–20		TCLCH–10		ns	
ALE Active Delay	TCLLH		80		50	ns	
ALE Inactive Delay	TCHLL		85		55	ns	
Address Hold Time to ALE Inactive	TLLAX	TCHCL–10		TCHCL–10		ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
Data Hold Time	TCHDX	10		10		ns	
Data Hold Time After WR	TWHDX	TCLCH–30		TCLCH–30		ns	
Control Active Delay 1	TCVCTV	10	110	10	70	ns	
Control Active Delay 2	TCHCTV	10	110	10	60	ns	
Control Active Delay	TCVCTX	10	110	10	70	ns	
Address Float to READ Active	TAZRL	0		0		ns	
$\overline{RD}$ Active Delay	TCLRL	10	165	10	100	ns	
$\overline{RD}$ Inactive Delay	TCLRH	10	150	10	80	ns	
$\overline{RD}$ Inactive to Next Address Active	TRHAV	TCLCL–45		TCLCL–40		ns	
HLDA Valid Delay	TCLHAV	10	160	10	100	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL–75		2TCLCL–50		ns	
$\overline{WR}$ Width	TWLWH	2TCLCL–60		2TCLCL–40		ns	
Address Valid to ALE Low	TAVAL	TCLCH–60		TCLCH–40		ns	
Output Rise Time	TOLOH		20			ns	From 0.8V to 2.0V
Output Fall Time	TOHOL		12			ns	From 2.0V to 0.8V

NOTES: ① Signal at μPD8284 shown for reference only
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
③ Applies only to T2 state (8 ns into T3)

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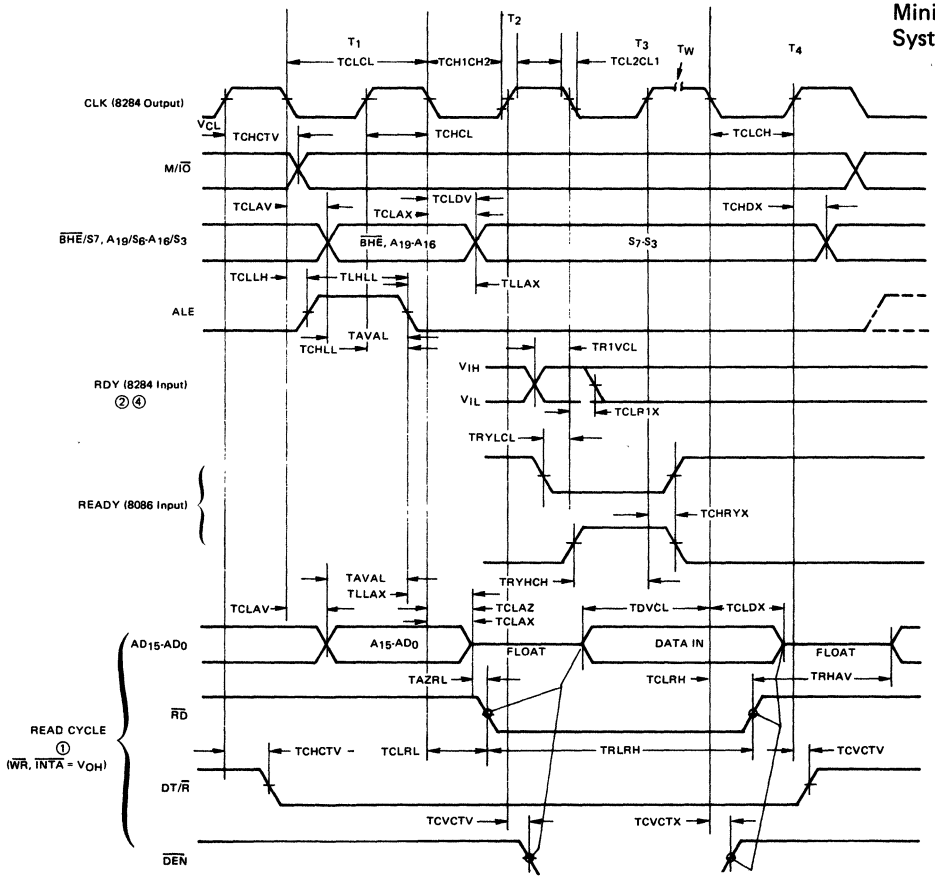
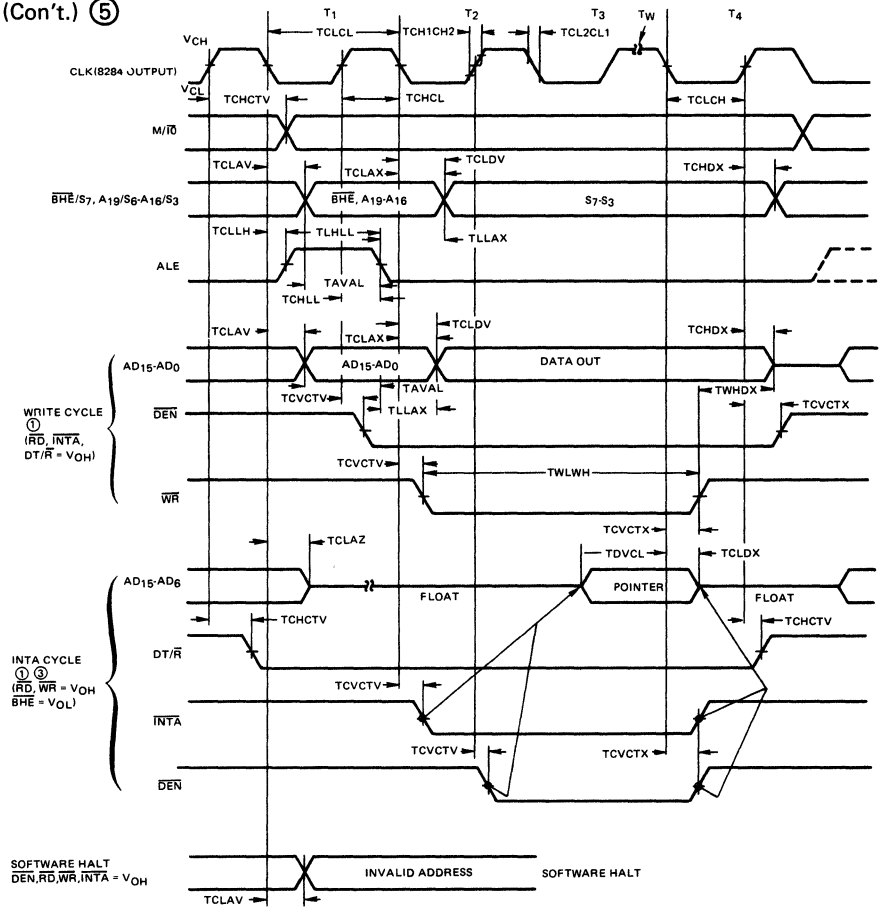
TIMING WAVEFORMS

Minimum Complexity Systems ⑤



TIMING WAVEFORMS

Minimum Complexity Systems (Con't.) ⑤



NOTES: ① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.

③ Two INTA cycles run back-to-back. The μPD8086 local ADDR/Data Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.

④ Signals at μPD8284 are shown for reference only.

⑤ All timing measurements are made at 1.5V unless otherwise noted.

MAXIMUM MODE SYSTEM
With μPB8288
Bus Controller

TIMING WITH μPB8288 BUS CONTROLLER

TIMING REQUIREMENTS

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
CLK Cycle Period – μPD8086	TCLCL	200	500	125	500	ns	
CLK Low Time	TCLCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2		(1/3 TCLCL) +2		ns	
CLK Rise Time	TCH1CH2		10		10	ns	From 1 0V to 3 5V
CLN Fall Time	TCL2CL1		10		10	ns	From 3 5V to 1 0V
Data in Setup Time	TDVCL	30		20		ns	
Data in Hold Time	TCLDX	10		10		ns	
RDY Setup Time into μPD8284 ①②	TR1VCL	35		35		ns	
RDY Hold Time into μPD8284 ①, ②	TCLR1X	0		0		ns	
READY Setup Time into μPD8086	TRYHCH	(2/3 TCLCL) -15		(2/3 TCLCL) -15		ns	
READY Hold Time into μPD8086	TCHRYX	30		20		ns	
READY inactive to CLK ④	TRYLCL	-8		-8		ns	
Setup Time for Recognition (INTR, NMI, TEST) ②	TINVCH	30		15		ns	
$\overline{RQ}/\overline{GT}$ Setup Time	TGVCH	30		15		ns	
$\overline{RQ}$ Hold Time into μPD8086	TCHGX	40		30		ns	
Input Rise Time	TILIH		20			ns	From 0 8V to 2 0V
Input Fall Time	TIHIL		12			ns	From 2 0V to 0 8V

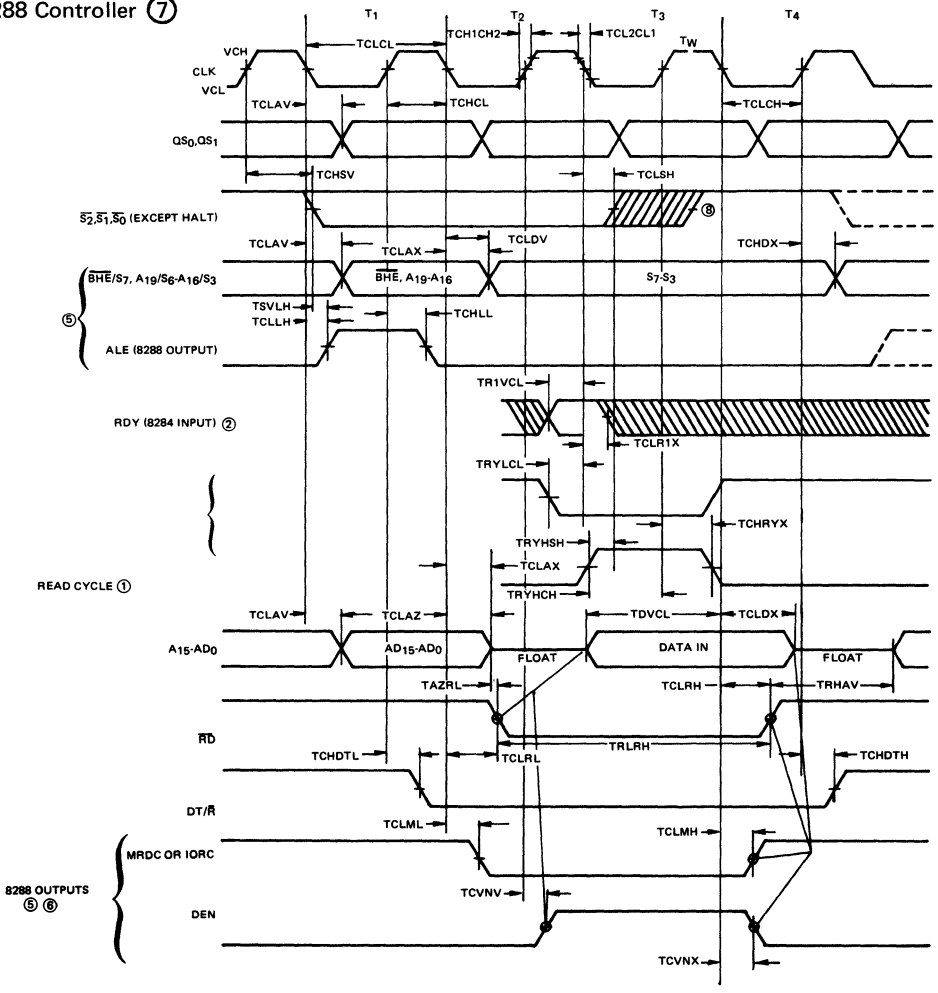
TIMING RESPONSES

PARAMETER	SYMBOL	μPD8086		μPD8086-2 (Preliminary)		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Command Active Delay (See Note 1)	TCLML	10	35	10	35	ns	
Command Inactive Delay (See Note 1)	TCLMH	10	35	10	35	ns	
READY Active to Status Passive (See Note 3)	TRYHSH		110		65	ns	
Status Active Delay	TCHSV	10	110	10	60	ns	
Status Inactive Delay	TCLSH	10	130	10	70	ns	
Address Valid Delay	TCLAV	10	110	10	60	ns	
Address Hold Time	TCLAX	10		10		ns	
Address Float Delay	TCLAZ	TCLAX	80	TCLAX	50	ns	
Status Valid to ALE High (See Note 1)	TSVLH		15		15	ns	
Status Valid to MCE High (See Note 1)	TSVMCH		15		15	ns	
CLK Low to ALE Valid (See Note 1)	TCLLH		15		15	ns	
CLK Low to MCE High (See Note 1)	TCLMCH		15		15	ns	
ALE Inactive Delay (See Note 1)	TCHLL		15		15	ns	C_L = 20-100 pF for all μPD8086 Outputs (In addition to μPD8086 self-load)
MCE Inactive Delay (See Note 1)	TCLMCL		15		15	ns	
Data Valid Delay	TCLDV	10	110	10	60	ns	
Data Hold Time	TCHDX	10		10		ns	
Control Active Delay (See Note 1)	TCVNV	5	45	5	45	ns	
Control Inactive Delay (See Note 1)	TCVNX	10	45	10	45	ns	
Address Float to Read Active	TAZRL	0		0		ns	
RD Active Delay	TCLRL	10	165	10	100	ns	
RD Inactive Delay	TCLRH	10	150	10	80	ns	
RD Inactive to Next Address Active	TRHAV	TCLCL-45		TCLCL-40		ns	
Direction Control Active Delay (See Note 1)	TCHDTL		50		50	ns	
Direction Control Inactive Delay (See Note 1)	TCHDTH		30		30	ns	
$\overline{GT}$ Active Delay	TCLGL	0	85	0	50	ns	
$\overline{GT}$ Inactive Delay	TCLGH	0	85	0	50	ns	
$\overline{RD}$ Width	TRLRH	2TCLCL-50		2TCLCL-50		ns	
Output Rise Time	TOLOH		20			ns	From 0 8V to 2 0V
Output Fall Time	TOHOL		12			ns	From 2 0V to 0 8V

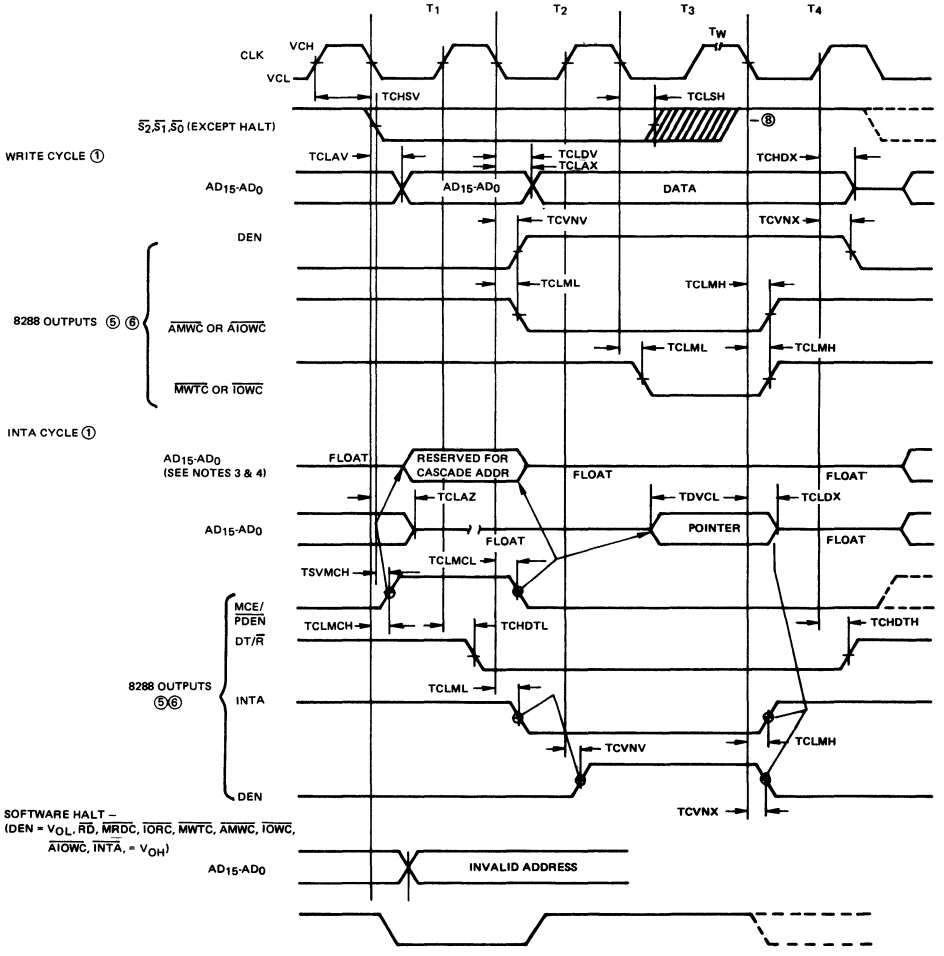
NOTES ① Signal at μPB8284 or μPB8288 shown for reference only.
② Setup requirement for asynchronous signal only to guarantee recognition at next CLK
③ Applies only to T3 and wait states
④ Applies only to T2 state (8 ns into T3)

TIMING WAVEFORMS

Maximum Mode
System Using
μPB8288 Controller (7)

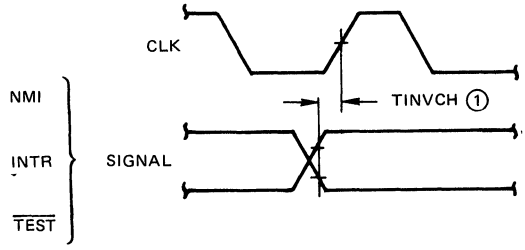


TIMING WAVEFORMS
Maximum Mode
System Using
μPB8288 Controller
(Con't.) ⑦



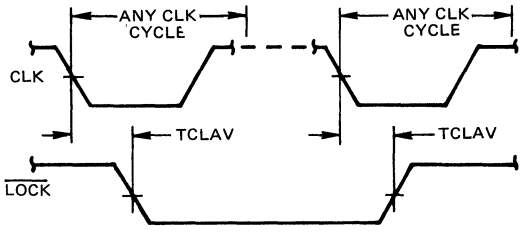
NOTES
① All signals switch between V_{OH} and V_{OL} unless otherwise specified.
② RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
③ Cascade address is valid between first and second INTA cycle.
④ Two INTA cycles run back-to-back. The 8086 local ADDR/Data Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
⑤ Signals at 8284 or 8288 are shown for reference only.
⑥ The issuance of the 8288 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 8288 CEN
⑦ All timing measurements are made at 1.5V unless otherwise noted.
⑧ Status inactive in state just prior to T_4.

ASYNCHRONOUS SIGNAL RECOGNITION

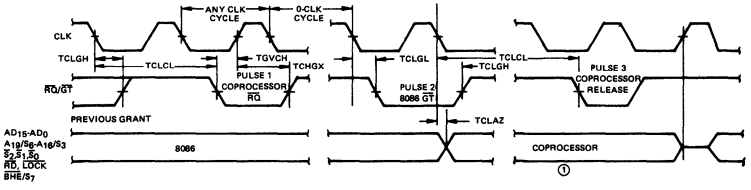


NOTE: (1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK.

BUS LOCK SIGNAL TIMING



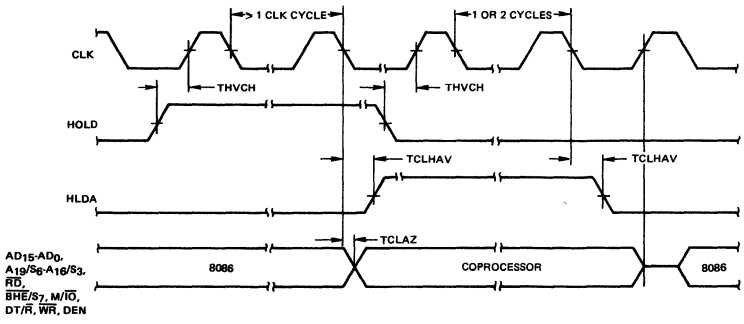
REQUEST/GRANT SEQUENCE TIMING*



NOTE: (1) The coprocessor may not drive the buses outside the region shown without risking contention.

*for Maximum Mode only

HOLD/HOLD ACKNOWLEDGE TIMING*



*for Minimum Mode only

Package Outlines

For information, see Package Outline Section 7.

Cerdip, μPD8086D

μPD8088
HIGH-PERFORMANCE 8-BIT MICROPROCESSOR

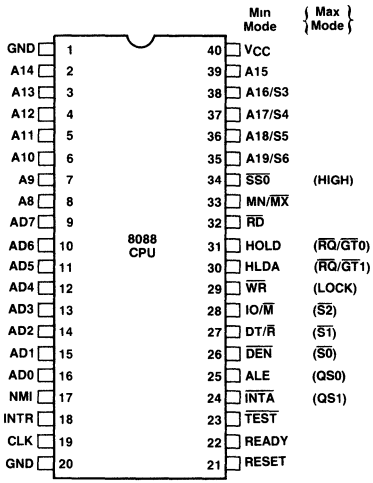
Description

The μPD8088 is a powerful 8-bit microprocessor that is software-compatible with the μPD8086. The μPD8088 has the same bus interface signals as the μPD8085A, allowing it to interface directly with multiplexed bus peripherals. The μPD8088 has a 20-bit address space which can be divided into four segments of up to 64K bytes each.

Features

- ☐ 8-bit data bus interface
- ☐ 16-bit internal architecture
- ☐ Addresses 1 M-byte of memory
- ☐ Software-compatible with the 8086
- ☐ Provides byte, word, and block operations
- ☐ Performs 8- and 16-bit signed and unsigned arithmetic in binary and decimal
- ☐ Multiply and divide instruction
- ☐ Directly interfaces to 8155, 8355, and 8755A multiplexed peripherals
- ☐ 40-pin DIP

Pin Configuration

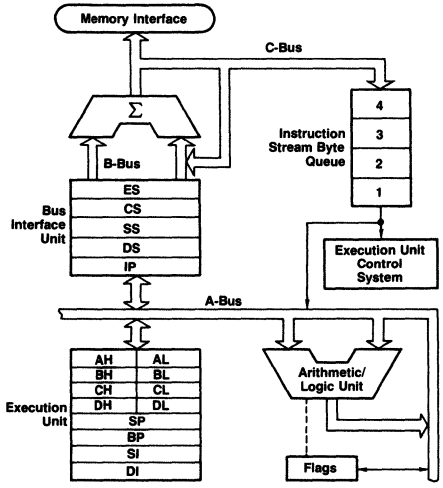


Pin Identification

No.	Symbol	Name	Function
1, 20	GND	Ground	
2–8, 35–39	A_{19}–A_8	Most significant address bits	Most significant bits for memory operations.
9–16	AD_7–AD_0	Address/Data bus	Multiplexed address and data bus. 8-bit peripherals tied to these bits use A_0 to condition chip select functions. These lines are tri-state during hold and interrupt acknowledge states.
17	NMI	Non-maskable interrupt	This edge-triggered input causes a type 2 interrupt. The processor uses a lookup table for vectoring information.
18	INTR	Interrupt request	This is a level-triggered interrupt sampled on the last clock cycle of each instruction. A lookup table is used for vectoring. INTR can be masked by software by resetting the interrupt enable bit.
19	CLK	Clock	The clock is a 1/3 duty cycle input providing basic timing for the processor and bus controller.
21	RESET	Reset	This active high signal must be high for 4 clock cycles. When it returns low, the processor restarts execution.
22	READY	Ready	An acknowledgement from memory or I/O that data will be transferred. Synchronization is done by the μPD8284 clock generator.
23	$\overline{TEST}$	Test	This input is examined by the "WAIT" instruction and if low, execution continues. Otherwise the processor waits in an "idle" state. Synchronized by the processor on the leading edge of CLK.
24	$\overline{INTA}$	Interrupt Acknowledge	This is a read strobe for reading vectoring information. During T_2, T_3, and T_W of each interrupt acknowledge cycle it is low.
25	$\overline{ALE}$	Address Latch Enable	Used with the μPD8282/8283 latches to latch the address during T_1 of any bus cycle.
24, 25	QS_1, QS_0	Queue Status	(Max Mode) Tracks the internal μPD8088 instruction queue.
26	$\overline{DEN}$	Data Enable	This is the output enable for the μPD8286/8287 transceivers. It is active low during memory and I/O access and INTA cycles.
27	DT/$\overline{R}$	Data Transmit/ Receive	Controls the direction of data flow through the transceivers.
28	IO/M	I/O/Memory Status	Separates memory access from I/O access.
29	$\overline{WR}$	Write	The processor is writing to memory or I/O, depending on the state of the IO/M line.
29	LOCK	Lock	(Max Mode) This output is set by the lock instruction to prevent other system bus masters from gaining control.
30	HLDA	Hold Acknowledge	A response to the HOLD input, causing the processor to tri-state the local bus. The bus becomes active one cycle after HOLD returns low.
31	HOLD	Hold	When another device requests the local bus, HOLD is driven high, causing the μPD8088 to issue a HLDA.
30, 31	$\overline{RQ}/GT_0$ $\overline{RQ}/GT_1$	Request/Grant	(Max Mode) Other local bus masters can force the processor to rebase the local bus at the end of the current bus cycle.
32	$\overline{RD}$	Read	Depending on the state of the $\overline{IO}$/M line, the processor is reading from memory or I/O.
33	MN/$\overline{MX}$	Minimum/ Maximum	This input tells the processor in which mode it is to be used. This affects some of the pin descriptions.
34	$\overline{SS0}$	Status Line	Equivalent to $\overline{S_0}$ in Max Mode.
26–28	$\overline{S_0}$–$\overline{S_2}$	Status Outputs	(Max Mode)
35–38	S_3–S_6	Status Outputs	These outputs from the processor are used by the μPD8288 to generate bus control signals.
40	V_{CC}	Power Supply	5V power input.

5

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C

Tentative	
Ambient Temperature under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin with respect to Ground	−0.5V to +7V
Power Dissipation	2.5 Watt

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = 0°C to +70°C, V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Input Low Voltage	V_{CL}	−0.5		+0.6	V	
Clock Input High Voltage	V_{CH}	3.9		V_{CC} + 1.0	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Input High Voltage	V_{IH}	2.0		VCC + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 400 μA
Power Supply Current	I_{CC}			340	mA	
Input Leakage	I_{LI}			±10	μA	0V < V_{IN} < V_{CC}
Output Leakage	I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Capacitance of Input Buffer (All input except AD_0–AD_7 RQ/GT)	C_{IN}			15	pF	fc = 1 MHz
Capacitance of I/O Buffer (AD_0–AD_7 RQ/GT)	C_{IO}			15	pF	fc = 1 MHz

AC Characteristics

Minimum Mode Timing Requirements

T_a = 0°C to +70°C, V_{CC} = +5V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
CLK Period	t_{CLCL}	200		500	ns	
CLK Low Time	t_{CLCH}	$(2/3t_{CLCL})-15$			ns	
CLK High Time	t_{CHCL}	$(1/3t_{CLCL})+2$			ns	
CLK Rise Time	t_{CH1CH2}			10	ns	1.0V to 3.5V
CLK Fall Time	t_{CL2CL1}			10	ns	3.5V to 1.0V
Data In Setup Time	t_{DVCL}	30			ns	
Data In Hold Time	t_{CLDX}	10			ns	
RDY Setup Time μPD8284 ① ②	t_{R1VCL}	35			ns	
RDY Hold Time into μPD8284 ① ②	t_{CLR1X}	0			ns	
READY Setup Time into μPD8088	t_{RYHCH}	$(2/3t_{CLCL})-15$			ns	
READY Hold Time into μPD8088	t_{CHRYX}	30			ns	
READY Inactive to CLK ③	t_{RYLCL}	−8			ns	
HOLD Setup Time	t_{HVCH}	35			ns	
INTR, NMI, $\overline{TEST}$ Setup Time ②	t_{INVCH}	30			ns	
Input Rise Time (Except CLK)	t_{ILIH}			20	ns	0.8V to 2.0V
Input Fall Time (Except CLK)	t_{IHIL}			12	ns	2.0V to 0.8V

Notes:

① Signal at μPD8284 shown for reference only.

② Setup requirement for asynchronous signal guarantees recognition at next CLK.

③ Applies to T_2 state (8 ns into T_3 state).

Timing Responses

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Address Valid Delay	t_{CLAV}	15		110	ns	
Address Hold Time	t_{CLAX}	10			ns	
Address Float Delay	t_{CLAZ}	t_{CLAX}		80	ns	
ALE Width	t_{LHLL}	$t_{CLCH}-20$			ns	
ALE Active Delay	t_{CLLH}			80	ns	
ALE Inactive Delay	t_{CHLL}			85	ns	
Address Hold Time to ALE Inactive	t_{LLAX}	$t_{CHCL}-10$			ns	
Data Valid Delay	t_{CLDV}	10		110	ns	C_L = 20-100 pF for all 8088 outputs and internal loads
Data Hold Time	t_{CHDX}	10			ns	
Data Hold Time After $\overline{WR}$	t_{WHDX}	$t_{CLCH}-30$			ns	
Control Active Delay 1	t_{CVCTV}	10		110	ns	
Control Active Delay 2	t_{CHCTV}	10		110	ns	
Control Inactive Delay	t_{CVCTX}	10		110	ns	
Address Float to READ Active	t_{AZRL}	0			ns	
$\overline{RD}$ Active Delay	t_{CLRL}	10		165	ns	
$\overline{RD}$ Inactive Delay	t_{CLRH}	10		150	ns	
$\overline{RD}$ Inactive to Next Address Active	t_{RHAV}	$t_{CLCL}-45$			ns	
HLDA Valid Delay	t_{CLHAV}	10		160	ns	
$\overline{RD}$ Width	t_{RLRH}	$2t_{CLCL}-75$			ns	
$\overline{WR}$ Width	t_{WLWH}	$2t_{CLCL}-60$			ns	
Address Valid to ALE Low	t_{AVAL}	$t_{CLCH}-60$			ns	
Output Rise Time	t_{OLOH}			20	ns	0.8V to 2.0V
Output Fall Time	t_{OHOL}			12	ns	2.0V to 0.8V

AC Characteristics (Cont.)

Max Mode System Timing Requirements (Using 8288 Bus Controller)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
CLK Period	t_{CLCL}	200		500	ns	
CLK Low Time	t_{CLCH}	$(2/3t_{CLCL})-15$			ns	
CLK High Time	t_{CHCL}	$(1/3t_{CLCL})+2$			ns	
CLK Rise Time	t_{CH1CH2}			10	ns	1.0V to 3.5V
CLK Fall Time	t_{CL2CL1}			10	ns	3.5V to 1.0V
Data In Setup Time	t_{DVCL}	30			ns	
Data In Hold Time	t_{CLDX}	10			ns	
RDY Setup Time into μPD8284 ① ②	t_{R1VCL}	35			ns	
RDY Hold Time into μPD8284 ① ②	t_{CLR1X}	0			ns	
READY Setup Time into μPD8088	t_{RYHCH}	$(2/3t_{CLCL})-15$			ns	
READY Hold Time into μPD8088	t_{CHRYX}	30			ns	
READY Inactive to CLK ④	t_{RYLCL}	-8			ns	
Setup Time for Recognition (INTR, NMI, TEST) ②	t_{INVCH}	30			ns	
RQ/GT Setup Time	t_{GVCH}	30			ns	
RQ Hold Time into μPD8088	t_{CHGX}	40			ns	
Input Rise Time (Except CLK)	t_{ILIH}			20	ns	0.8V to 2.0V
Input Fall Time (Except CLK)	t_{IHIL}			12	ns	2.0V to 0.8V

Timing Responses

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Command Active Delay ①	t_{CLML}	10		35	ns	
Command Inactive Delay ①	t_{CLMH}	10		35	ns	
READY Active to Status Passive ③	t_{RYHSH}			110	ns	
Status Active Delay	t_{CHSV}	10		110	ns	
Status Inactive Delay	t_{CLSH}	10		130	ns	
Address Valid Delay	t_{CLAV}	15		110	ns	
Address Hold Time	t_{CLAX}	10			ns	
Address Float Delay	t_{CLAZ}	t_{CLAX}		80	ns	
Status Valid to ALE High ①	t_{SVLH}			15	ns	
Status Valid to MCE High ①	t_{SVMCH}			15	ns	
CLK Low to ALE Valid ①	t_{CLLH}			15	ns	
CLK Low to MCE High ①	t_{CLMCH}			15	ns	
ALE Inactive Delay ①	t_{CHLL}			15	ns	C_L = 20-100 pF for all 8088 outputs and internal loads
MCE Inactive Delay ①	t_{CLMCL}			15	ns	
Data Valid Delay	t_{CLDV}	15		110	ns	
Data Hold Time	t_{CHDX}	10			ns	
Control Active Delay ①	t_{CVNV}	5		45	ns	
Control Inactive Delay ①	t_{CVNX}	10		45	ns	
Address Float to READ Active	t_{AZRL}	0			ns	
RD Active Delay	t_{CLRL}	10		165	ns	
RD Inactive Delay	t_{CLRH}	10		150	ns	
RD Inactive to Next Address Active	t_{RHAV}	$t_{CLCL}-45$			ns	
Direction Control Active Delay ①	t_{CHDTL}			50	ns	
Direction Control Inactive Delay ①	t_{CHDTH}			30	ns	
$\overline{GT}$ Active Delay	t_{CLGL}			85	ns	
$\overline{GT}$ Inactive Delay	t_{CLGH}			85	ns	
$\overline{RD}$ Width	t_{RLRH}	$2t_{CLCL}-75$			ns	
Output Rise Time	t_{OLOH}			20	ns	0.8V to 2.0V
Output Fall Time	t_{OHOL}			12	ns	2.0V to 0.8V

Notes:

① Signal at μPD8284 or μPD8288 shown for reference only.

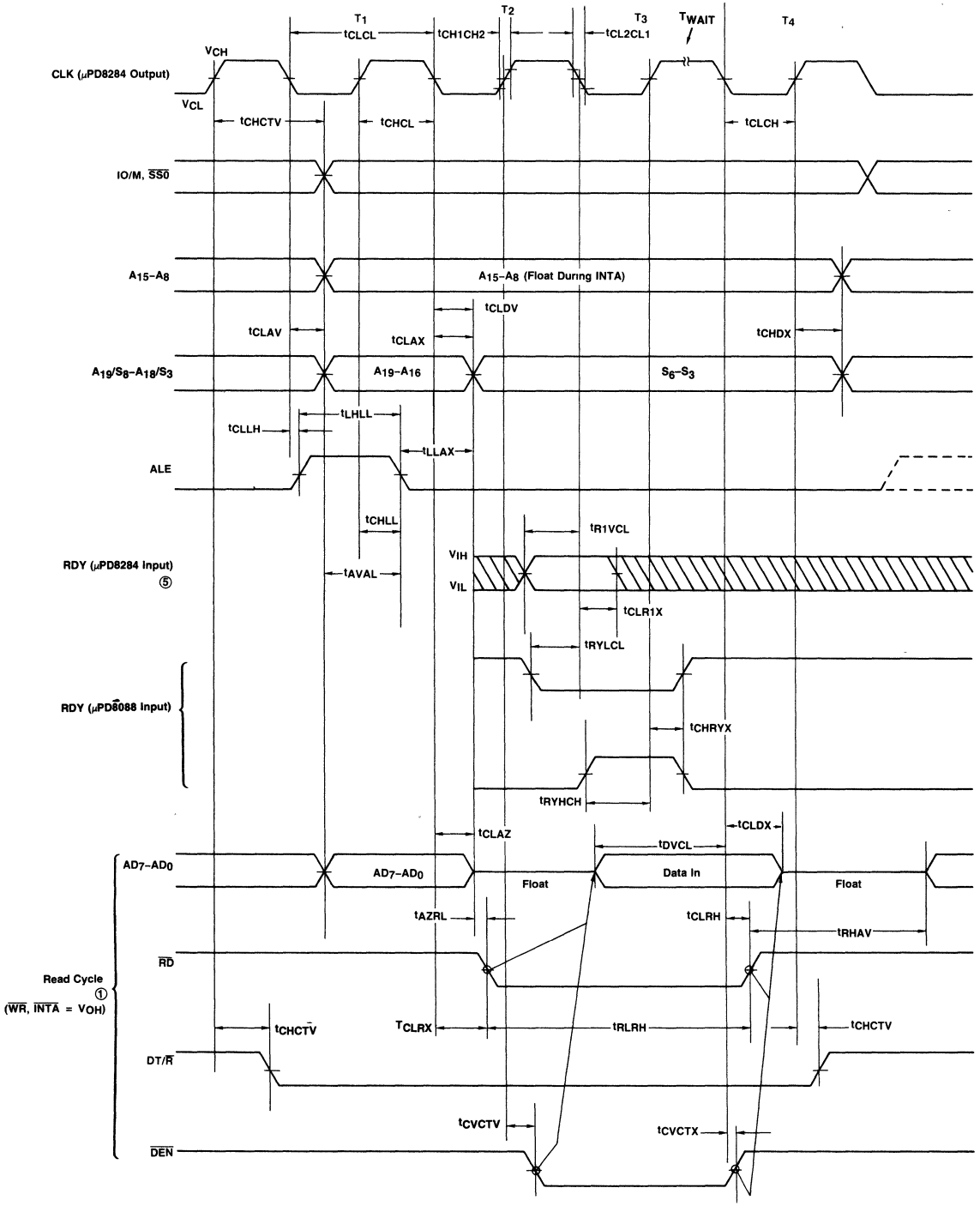
② Setup requirement for asynchronous signal guarantees recognition at next CLK.

③ Applies to T_3 and wait states.

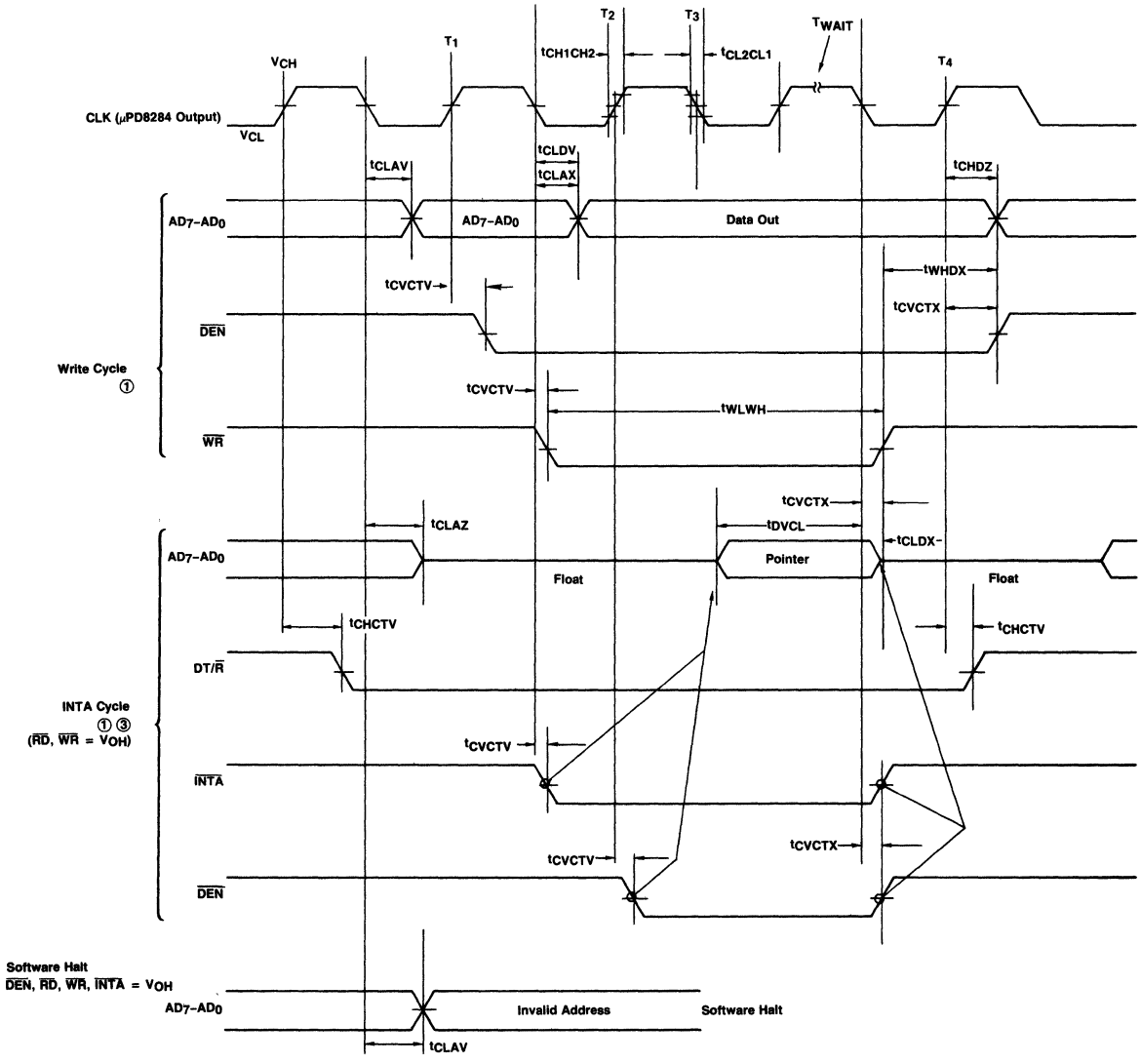
④ Applies to T_2 state (8 ns into T_3 state).

5

Timing Waveforms



Timing Waveforms (Cont.)



Notes:

① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

② RDY is sampled near the end of T_2, T_3, T_{WAIT} to determine if T_{WAIT} machine states are inserted.

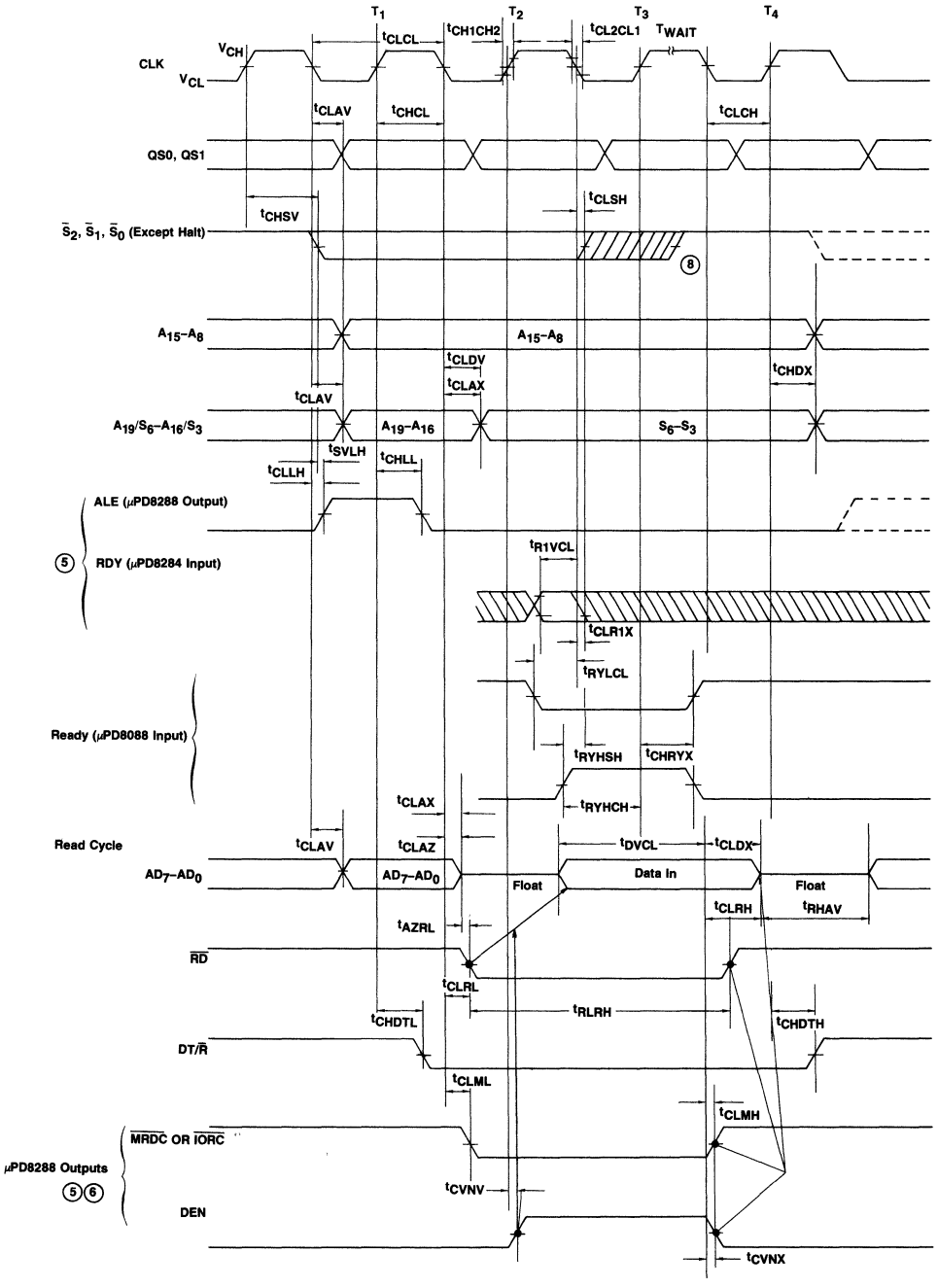
③ Two INTA cycles run back-to-back. The μPD8088 local Address/ Data bus floats during both INTA cycles. The control signals shown are for the second INTA cycle.

④ Signals at the μPD8284 are shown for reference.

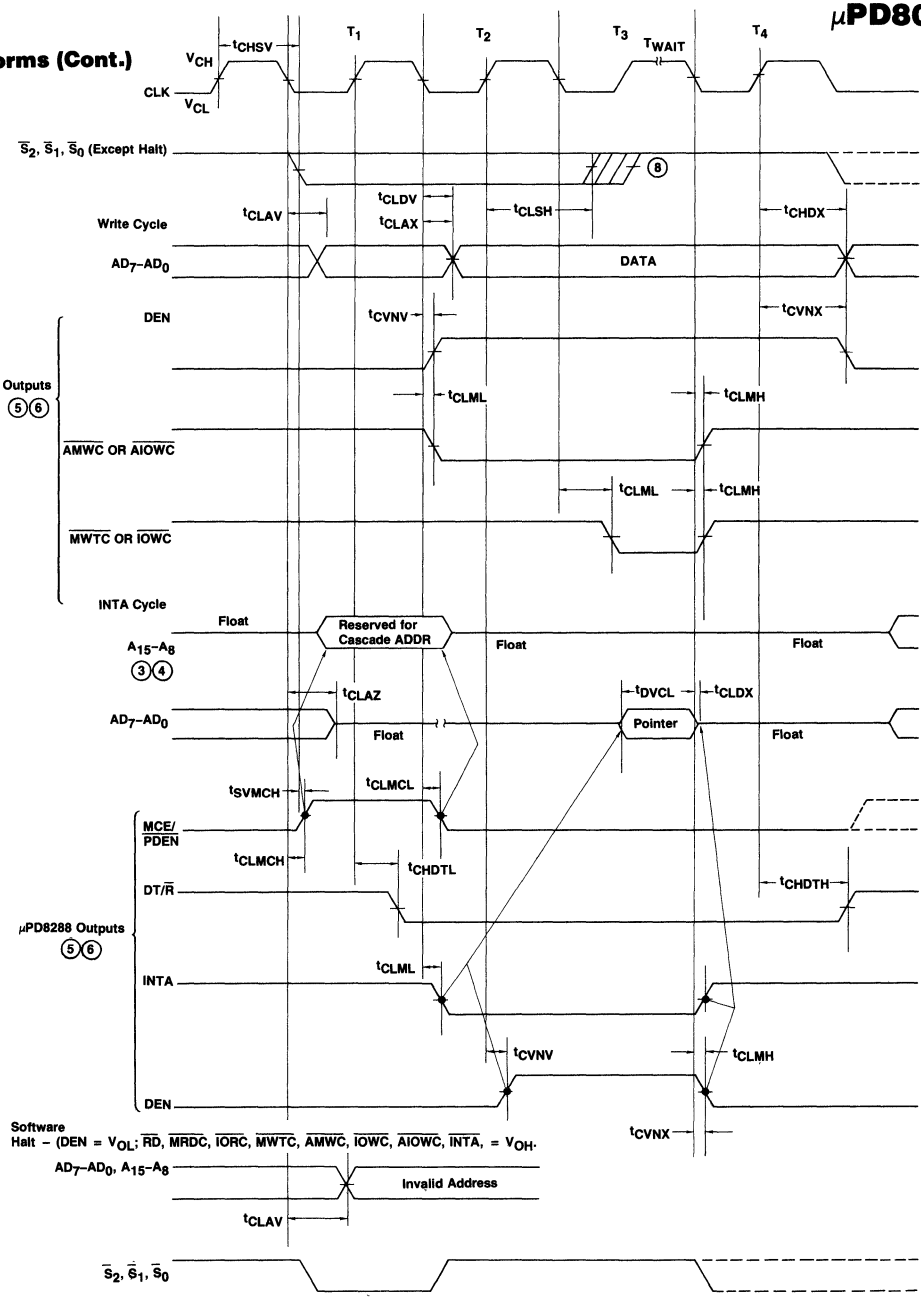
⑤ All timing measurements are taken at 1.5V unless otherwise specified.

Timing Waveforms (Cont.)

Maximum Mode System Bus Timing (using 8288 Bus Controller)



Timing Waveforms (Cont.)

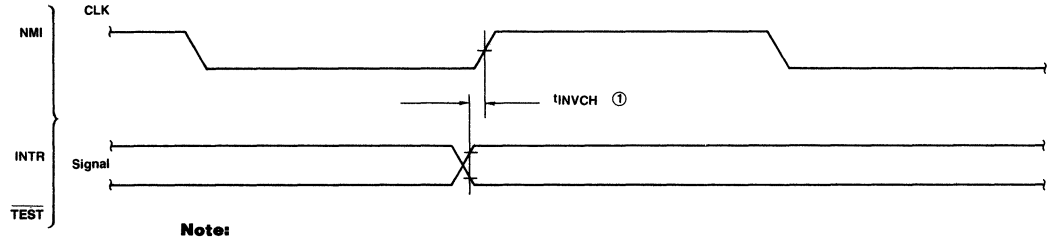


Notes:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_{WAIT} to determine if T_{WAIT} machine states are inserted.
3. The cascade address is valid between the first and second INTA cycles.
4. Two INTA cycles run back-to-back. The μPD8088 local Address/Data bus floats during both INTA cycles. The control signals shown are for the second INTA cycle.
5. Signals at the μPD8284 and μPD8288 are shown for reference.
6. The μPD8288 active-high CEN lags when the μPD8288 issues command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$, and $\overline{DEN}$).
7. All timing measurements are taken at 1.5V unless otherwise specified.
8. Status is inactive prior to T_4.

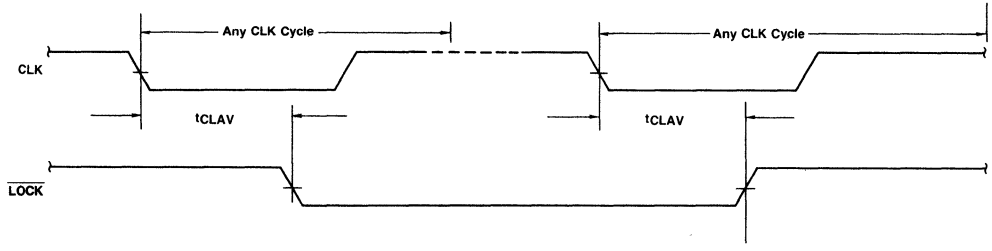
Timing Waveforms (Cont.)

Asynchronous Input Recognition

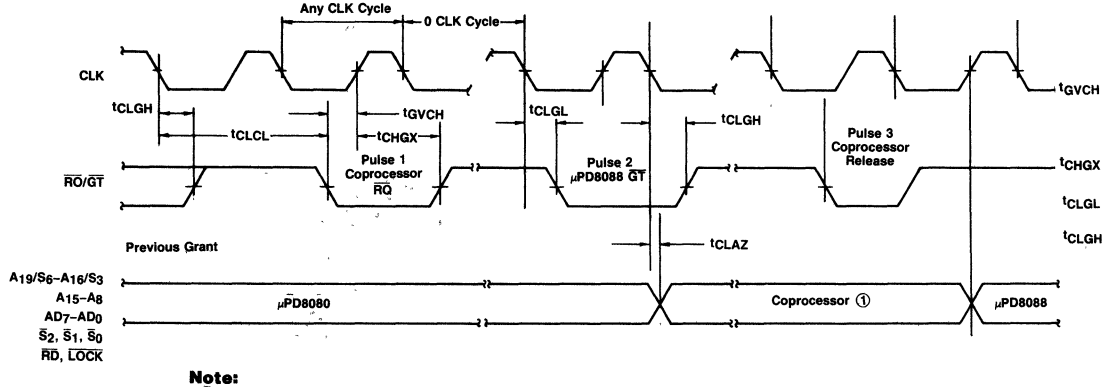


Note:
① Setup requirements for asynchronous signals guarantee recognition at next CLK.

Maximum Mode Bus Lock Signal Timing



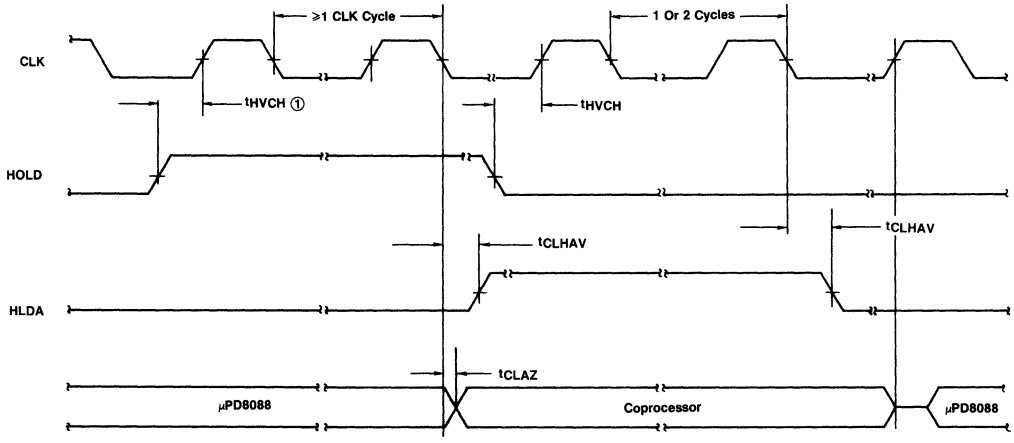
Maximum Mode Request/Grant Sequence Timing



Note:
① The coprocessor risks bus contention if it drives the buses outside the areas shown.

Timing Waveforms (Cont.)

Mimimum Mode Hold Acknowledge Timing



Note:
① All signals switch between V_{OH} and V_{OL} unless otherwise specified.

5

Package Outlines

For information, see Package Outline Section 7.

Cerdip, μPD8088D

PERIPHERALS 6

μPD765A/μPD7265
SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

Description

The μPD765A is an LSI Floppy Disk Controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to 4 floppy-disk drives. It is capable of supporting either IBM 3740 Single Density format (FM), or IBM System 34 Double Density format (MFM) including double-sided recording. The μPD765A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy-disk interface.

The μPD7265 is an addition to the FDC family that has been designed specifically for the Sony Micro Floppydisk® drive. The μPD7265 is pin-compatible and electrically equivalent to the 765A but utilizes the Sony recording format. The μPD7265 can read a diskette that has been formatted by the μPD765A.

Hand-shaking signals are provided in the μPD765A/μPD7265 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

There are 15 commands which the μPD765A/μPD7265 will execute. Each of these commands requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

READ DATA	SCAN HIGH OR EQUAL	WRITE DELETED DATA
READ ID	SCAN LOW OR EQUAL	SEEK
SPECIFY	READ DELETED DATA	RECALIBRATE
READ TRACK	WRITE DATA	SENSE INTERRUPT STATUS
SCAN EQUAL	FORMAT TRACK	SENSE DRIVE STATUS

Features

Address Mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable. The μPD765A/μPD7265 offers additional features such as multitrack and multiside read and write commands and single and double density capabilities.

- ☐ Sony (EMCA) Compatible Recording Format (μPD7265)
- ☐ IBM-compatible Format (Single and Double Density) (μPD765A)
- ☐ Multisector and Multitrack Transfer Capability
- ☐ Drive Up to 4 Floppy or Micro Floppydisk® Drives
- ☐ Data Scan Capability—Will scan a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- ☐ Data Transfers in DMA or Non-DMA Mode
- ☐ Parallel Seek Operations on Up to Four Drives
- ☐ Compatible with μPD8080/85, μPD8086/88 and μPD780 (Z80™) Microprocessors
- ☐ Single Phase Clock (8 MHz)
- ☐ +5V Only
- ☐ 40-Pin Plastic Package

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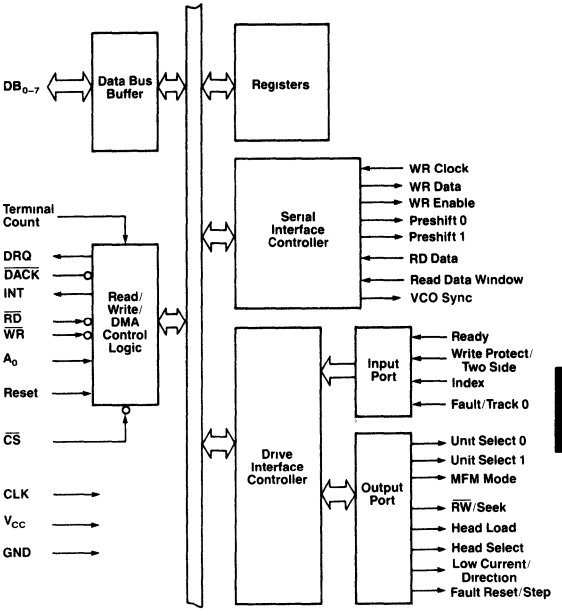
Micro Floppydisk® is a registered trademark of Sony Corporation

Block Diagram



Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.5 to +7V
All Input Voltages	−0.5 to +7V
Supply Voltage V_{CC}	−0.5 to +7V
Power Dissipation	1W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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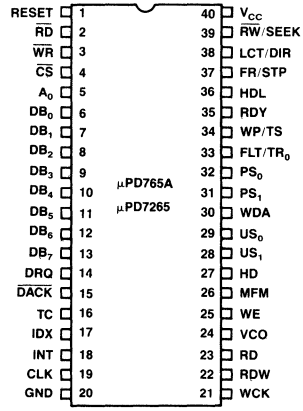
μPD765A/7265

Pin Configuration



DC Characteristics

T_a = −10°C to +70°C;
V_{CC} = +5V ± 5% unless otherwise specified

Parameter	Symbol	Limits Min	Limits Typ ①	Limits Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −200 μA
Input Low Voltage (CLK + WR Clock)	$V_{IL}(\phi)$	−0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH}(\phi)$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			150	mA	
Input Load Current	I_{LI}			10	μA	V_{IN} = V_{CC}
(All Input Pins)				−10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = +0.45V

Note: ① Typical values for T_a = 25°C and nominal supply voltage

Capacitance

T_a = 25°C; f_c = 1MHz; V_{CC} = 0V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Clock Input Capacitance	$C_{IN(\phi)}$			20	pF	All pins except pin under test tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Pin Identification

Pin No.	Symbol	Name	I/O	Connects To	Function
1	RST	Reset	I	Processor	Places FDC in idle state Resets output lines to FDD to 0 (low) Does not affect SRT, HUT or HLT in Specify command If RDY pin is held high during Reset, FDC will generate an interrupt within 1 024 msec To clear this interrupt use Sense Interrupt Status command
2	$\overline{RD}$	Read	I ①	Processor	Control signal for transfer of data from FDC to Data Bus, when 0 (low)
3	$\overline{WR}$	Write	I ①	Processor	Control signal for transfer of data to FDC via Data Bus, when 0 (low)
4	$\overline{CS}$	Chip Select	I	Processor	IC selected when 0 (low), allowing RD and WR to be enabled
5	A_0	Data/Status Reg Select	I ①	Processor	Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents of the FDC to be sent to Data Bus
6–13	DB_0–DB_7	Data Bus	I/O ①	Processor	Bidirectional 8-bit Data Bus
14	DRQ	Data DMA Request	O	DMA	DMA Request is being made by FDC when DRQ = 1
15	$\overline{DACK}$	DMA Acknowledge	I	DMA	DMA cycle is active when 0 (low) and controller is performing DMA transfer.
16	TC	Terminal Count	I	DMA	Indicates the termination of a DMA transfer when 1 (high) It terminates data transfer during Read/Write/Scan command in DMA or Interrupt mode
17	IDX	Index	I	FDD	Indicates the beginning of a disk track
18	INT	Interrupt	O	Processor	Interrupt Request generated by FDC
19	CLK	Clock	I		Single phase 8 MHz square-wave clock
20	GND	Ground			DC power return
21	WCK	Write Clock	I		Write data rate to FDD FM = 500 KHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM
22	RDW	Read Data Window	I	Phase Lock Loop	Generated by PLL, and used to sample data from FDD
23	RDD	Read Data	I	FDD	Read data from FDD, containing clock and data bits
24	VCO/ Sync	VCO/Sync	O	Phase Locked Loop	Inhibits VCO in PLL when 0 (low), enables VCO when 1
25	WE	Write Enable	O	FDD	Enables write data into FDD
26	MFM	MFM Mode	O	Phase Lock Loop	MFM mode when 1, FM mode when 0
27	HD	Head Select	O	FDD	Head 1 selected when 1 (high), Head 0 selected when 0 (low)
28, 29	US_1, US_0	Unit Select	O	FDD	FDD Unit selected
30	WDA	Write Data	O	FDD	Serial clock and data bits to FDD
31, 32	PS_1, PS_0	Precompensation (preshift)	O	FDD	Write precompensation status during MFM mode Determines early, late, and normal times
33	FLT/TR_0	Fault/Track 0	I	FDD	Senses FDD fault condition in Read/Write mode, and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two Side	I	FDD	Senses Write Protect status in Read/Write mode, and Two-Side Media in Seek mode
35	RDY	Ready	I	FDD	Indicates FDD is ready to send or receive data
36	HDL	Head Load	O	FDD	Command which causes read write head in FDD to contact diskette
37	FR/STP	Flt Reset/Step	O	FDD	Resets fault FF in FDD in Read Write mode, contains step pulses to move head to another cylinder in Seek mode
38	LCT/DIR	Low Current/ Direction	O	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal
39	$\overline{RW}$/ SEEK	Read Write/ Seek	O	FDD	When 1 (high) Seek mode selected and when 0 (low) Read/Write mode selected
40	V_{CC}	+5V			DC power.

Note: ① Disabled when $\overline{CS}$ = 1

AC Characteristics

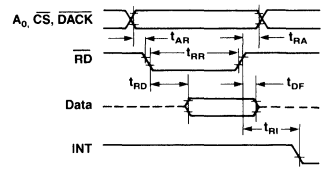
T_a = −10°C to +70°C;
V_{CC} = +5V ±5% unless otherwise specified

Parameter	Symbol	Limits Min	Typ ①	Max	Unit	Test Conditions
Clock Period	φCY	120	125	500	ns	8" FDD
			250			5¼" FDD
			125			3½" Sony
Clock Active (High)	φ0	40			ns	
Clock Rise Time	φr			20	ns	
Clock Fall Time	φf			20	ns	
A_0, CS, DACK Setup Time to RD ↓	t_{AR}	0			ns	
A_0, CS, DACK Hold Time from RD ↑	t_{RA}	0			ns	
RD Width	t_{RR}	250			ns	
Data Access Time from RD ↓	t_{RD}			200	ns	C_L = 100 pf
DB to Float Delay Time from RD ↑	t_{DF}	20		100	ns	C_L = 100 pF
A_0, CS, DACK Setup Time to WR ↓	t_{AW}	0			ns	
A_0, CS, DACK Hold Time to WR ↑	t_{WA}	0			ns	
WR Width	t_{WW}	250			ns	
Data Setup Time to WR ↑	t_{DW}	150			ns	
Data Hold Time from WR ↑	t_{WD}	5			ns	
INT Delay Time from RD ↑	t_{RI}			500	ns	
INT Delay Time from WR ↑	t_{WI}			500	ns	
DRQ Cycle Time	t_{MCY}	13			μs	
DACK ↓ → DRQ ↓ Delay	t_{AM}			200	ns	
DRQ ↑ → DACK ↓ Delay	t_{MA}	200			ns	ϕ_{CY} = 125 ns
DACK Width	t_{AA}	2			ϕ_{cy}	
TC Width	t_{TC}	1			φCY	
Reset Width	t_{RST}	14			φCY	
WCK Cycle Time	t_{CY}		4		μs	MFM = 0 5¼"
			2			MFM = 1 5¼"
			2			MFM = 0 8"
			1			MFM = 1 8"
			2			MFM = 0 3½" ③
			1			MFM = 1 3½" ③
WCK Active Time (High)	t_0	80	250	350	ns	
WCK Rise Time	t_r			20	ns	
WCK Fall Time	t_f			20	ns	
Preshift Delay Time from WCK ↑	t_{CP}	20		100	ns	
WCK ↑ → WE ↑ Delay	t_{CWE}	20		100	ns	
WDA Delay Time from WCK ↑	t_{CD}	20		100	ns	
RDD Active Time (High)	t_{RDD}	40			ns	
Window Cycle Time	t_{WCY}		4		μs	MFM = 0 5¼"
			2			MFM = 1 5¼"
			2			MFM = 0 8"
			1			MFM = 1 8"
			2			MFM = 0 3½"
			1			MFM = 1 3½"
Window Hold Time to/from RDD	t_{RDW} t_{WRD}	15			ns	
$US_{0,1}$ Hold Time to RW/SEEK ↑	t_{US}	12			μs	
RW/SEEK Hold Time to LOW CURRENT/DIRECTION ↑	t_{SD}	7			μs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/ STEP ↑	t_{DST}	1.0			μs	
$US_{0,1}$ Hold Time from FAULT RESET/STEP 1	t_{STU}	5.0			μs	8 MHz Clock Period ④
STEP Active Time (High)	t_{STP}	6	7	8	μs	④
STEP Cycle Time	t_{SC}	33	②	②	μs	④
FAULT RESET Active Time (High)	t_{FR}	8.0		10	μs	④
Write Data Width	t_{WDD}	T_0−50			ns	
$US_{0,1}$ Hold Time After SEEK	t_{SU}	15			μs	
Seek Hold Time from DIR	t_{DS}	30			μs	8 MHz Clock Period
DIR Hold Time after STEP	t_{STD}	24			μs	
Index Pulse Width	t_{IDX}	10			φCY	
RD ↓ Delay from DRQ	t_{MR}	800			μs	
WR ↓ Delay from DRQ	t_{MW}	250			μs	8 MHz Clock Period
WE or RD Response Time from DRQ ↑	t_{MRW}			12	μs	

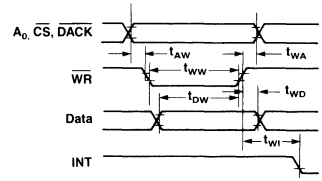
Notes: ① Typical values for T_a = 25°C and nominal supply voltage
② Under Software Control The range is from 1 ms to 16 ms at 8 MHz clock period, and 2 to 32 ms at 4 MHz clock period
③ Sony Micro Floppydisk® 3½" drive
④ Double these values for a 4 MHz clock period

Timing Waveforms

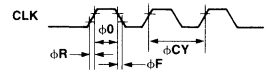
Processor Read Operation



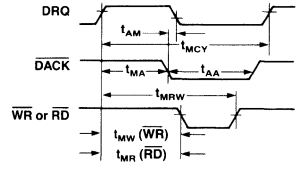
Processor Write Operation



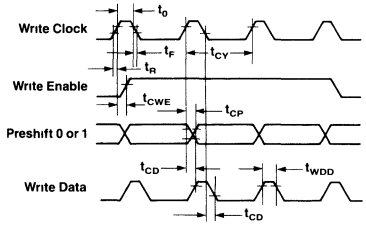
Clock



DMA Operation



FDD Write Operation



	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0
Invalid	1	1

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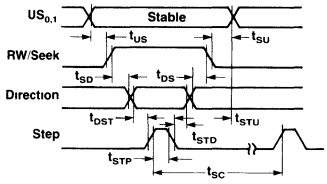
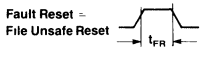
Timing Waveforms (Cont.)

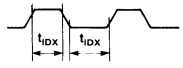
Seek Operation



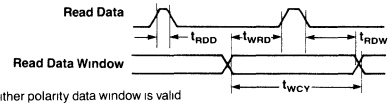
FLT Reset



Index

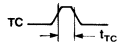


FDD Read Operation

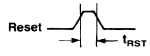


Note: Either polarity data window is valid

Terminal Count



Reset



Internal Registers

The μPD765A/μPD7265 contains two registers which may be accessed by the main system processor: a Status Register and a Data Register The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (which actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. Only the Status Register may be read and used to facilitate the transfer of data between the processor and μPD765/μPD7265.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

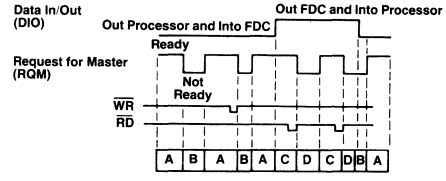
A_0	RD	WR	Function
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

Internal Registers (Cont.)

The bits in the Main Status Register are defined as follows:

Bit No.	Name	Symbol	Description
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
DB_6	Data Input/ Output	DIO	Indicates direction of data transfer between FDC and Data Register If DIO = 1, then transfer is from Data Register to the processor If DIO = 0, then transfer is from the processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time the Main Status Register is read the CPU should wait 12 μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC busy) goes low is 12 μs.



Notes: A — Data register ready to be written into by processor
B — Data register not ready to be written into by processor
C — Data register ready for next data byte to be read by processor
D — Data register not ready to be read by processor

Status Register Identification

No.	Bit Name	Symbol	Description
			Status Register 0
D_7 D_6	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of command, (NT). Command was completed and properly executed. D_7 = 0 and D_6 = 1 Abnormal Termination of command, (AT). Execution of command was started but was not successfully completed. D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started. D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault signal is received from the FDD, or if the Track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single-sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US_1	These flags are used to indicate a Drive Unit Number at Interrupt.
D_0	Unit Select 0	US_0	
			Status Register 1
D_7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC① error in either the ID field or the data field, this flag is set.
D_4	Overrun	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN command, if the FDC cannot find the sector specified in the IDR② Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A cylinder command, if the starting sector cannot be found, then this flag is set.
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in data field) of Status Register 2 is set.
			Status Register 2
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During execution of the READ DATA or SCAN command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of C③ on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is $FF_{(16)}$, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

Status Register Identification (Cont.)

No.	Bit Name	Symbol	Description
			Status Register 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the FDD
D_1	Unit Select 1	US_1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US_0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

Notes: ① CRC = Cyclic Redundancy Check
② IDR = Internal Data Register
③ Cylinder (C) is described more fully in the Command Symbol Description on page 7

Command Sequence

The μPD765A/μPD7265 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the μPD765A/μPD7265 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase.	The FDC performs the operation it was instructed to do.
Result Phase.	After completion of the operation, status and other housekeeping information are made available to the processor

Following are shown the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase The "W" to the left of each byte indicates a command phase byte to be written, and an "R" indicates a result byte

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Instruction Set ① ②

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	③
	W	←			C				→	Sector ID information prior
	W	←			H				→	to command execution. The
	W	←			R				→	4 bytes are commanded
	W	←			N				→	against header on Floppy
	W	←			EOT				→	Disk.
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior
	W	←			H				→	to command execution. The
	W	←			R				→	4 bytes are commanded
	W	←			N				→	against header on Floppy
	W	←			EOT				→	Disk.
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior
	W	←			H				→	to command execution. The
	W	←			R				→	4 bytes are commanded
	W	←			N				→	against header on Floppy
	W	←			EOT				→	Disk.
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the main system and FDD
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	

Notes: ① Symbols used in this table are described at the end of this section
② A_0 should equal binary 1 for all operations
③ X = Don't care, usually made to equal binary 0

Instruction Set

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior
	W	←			H				→	to command execution. The
	W	←			R				→	4 bytes are commanded
	W	←			N				→	against header on Floppy
	W	←			EOT				→	Disk.
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	
Read A Track										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior
	W	←			H				→	to command execution
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system FDC reads all data fields from index hole to EOT.
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in Data Register.
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information read
	R	←			H				→	during Execution phase from
	R	←			R				→	Floppy Disk.
	R	←			N				→	
Format A Track										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			N				→	Bytes/Sector
	W	←			SC				→	Sectors/Track
	W	←			GPL				→	Gap 3
	W	←			D				→	Filler byte
Execution										FDC formats an entire track.
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	In this case, the ID
	R	←			H				→	information has no meaning.
	R	←			R				→	
	R	←			N				→	
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior
	W	←			H				→	to command execution
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	

Instruction Set (Cont.)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to
	W	←			H				→	command execution
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to
	W	←			H				→	command execution
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST 0				→	Status information after
	R	←			ST 1				→	command execution
	R	←			ST 2				→	
	R	←			C				→	Sector ID information after
	R	←			H				→	command execution
	R	←			R				→	
	R	←			N				→	
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to Track 0
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	←			STO				→	Status information about
	R	←			PCN				→	the FDC at the end of seek operation
Specify										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	← SRT			→	←		HUT →		
	W	←	HLT			→	ND			
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	←			ST 3				→	Status information about FDD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			NCN				→	
Execution										Head is positioned over proper cylinder on diskette.
Invalid										
Command	W	←			Invalid Codes				→	Invalid Command Codes (NoOp — FDC goes into Standby state.)
Result	R	←			ST 0				→	ST 0 = $80_{(16)}$

Command Symbol Description

Symbol	Name	Description
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7–D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multitrack	If MT is high, a Multitrack operation is performed. If MT = 1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the Number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a New Cylinder Number which is going to be reached as a result of the Seek operation. Desired position of head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA mode.
PCN	Present Cylinder Number	PCN stands for the cylinder number at the completion of Sense Interrupt Status command. Position of Head at present time.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives (F = 1 ms, E = 2 ms, etc.).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST 0–3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0–3 may be read only after a command has been executed and contains information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

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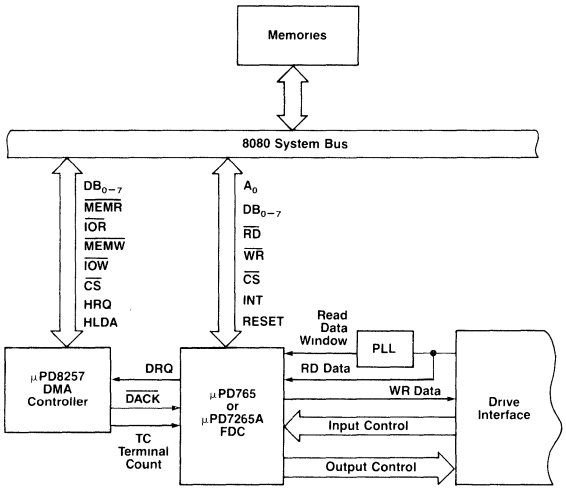
System Configuration



Processor Interface

During Command or Result phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to the Data Register, CPU should wait for 12μs before reading Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765A/μPD7265. Many of the commands require multiple bytes and, as a result, the Main Status Register must be read prior to each byte transfer to the μPD765A/μPD7265. On the other hand, during the Result phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the μPD765A/μPD7265 is required only in the Command and Result phases, and *not* during the Execution phase.

During the Execution phase, the Main Status Register need not be read. If the μPD765A/μPD7265 is in the non-DMA mode, then the receipt of each data byte (if μPD765A/μPD7265 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will clear the Interrupt as well as output the data onto the data bus. If the processor cannot handle Interrupts fast enough (every 13 μs for the MFM mode and 27 μs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write command is in process then the $\overline{WR}$ signal negates the reset to the Interrupt signal.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal.

If the μPD765A/μPD7265 is in the DMA mode, no Interrupts are generated during the Execution phase. The μPD765A/μPD7265 generates DRQs (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and an $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0), then the DMA Request is cleared (DRQ = 0). If a Write command has been issued then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the Interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

It is important to note that during the Result phase all bytes shown in the Command Table must be read. The Read Data command, for example, has seven bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The μPD765A/μPD7265 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase.

The μPD765A/μPD7265 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only after completing a command. The particular command that has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765A/μPD7265 to form the Command phase and are read out of the μPD765A/μPD7265 in the Result phase must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the μPD765A/μPD7265, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the μPD765A/μPD7265 is ready for a new command.

Polling Feature of the μPD765A/μPD7265

After Reset has been sent to the μPD765A/μPD7265, the Unit Select lines US_0 and US_1 will automatically go into a polling mode. In between commands (and between step pulses in the Seek command) the μPD765A/μPD7265 polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing), then the μPD765A/μPD7265 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the μPD765A/μPD7265 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms.

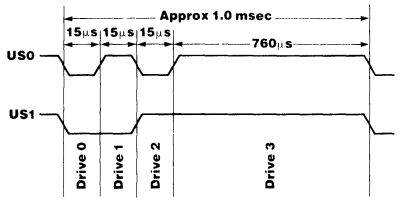


figure 1. (polling feature)

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the $\overline{DACK}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

Functional Description of Commands

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	C+1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	LSB	R = 01	NC

Notes: NC (No Change) The same value as the one at the beginning of command execution
LSB (Least Significant Bit) The least significant bit of H is complemented

Write Data

A set of nine (9) bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match

the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multisector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the data bus, must occur every 27 μs in the FM mode and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

Read A Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hole for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format A Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) format are recorded. The particular format which will be written is controlled by the values programmed into N (Number of bytes/sector), SC (Sectors/Cylinder), GPL (Gap Length), and D (Data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder number), H (Head number), R (Sector number) and N (Number of bytes/sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765A/μPD7265 for each sector on the track If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If a Fault signal is received from the FDD at the end of a Write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high) and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a Ready signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 1 shows the relationship between N, SC, and GPL for various sector sizes.

Functional Description of Commands (Cont.)

Format	Sector Size	N	SC	GPL①	GPL②③
	8" Standard Floppy				
FM Mode	128 bytes/sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode ④	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
	5¼" Minifloppy				
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode ④	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
	3½" Sony Microfloppy				
FM Mode	128 bytes/sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode ④	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

Table 1

Notes: ① Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections
② Suggested values of GPL in format command
③ All values except sector size are hexidecimal
④ In MFM mode FDC cannot perform a Read/Write/format operation with 128 bytes/sector (N = 00)

Scan Commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 2 shows the status of bits SH and SN under various conditions of Scan.

Command	Status Register 2 Bit 2 = SN	Status Register 2 Bit 3 = SH	Comments
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

Table 2

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (Multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM mode) or 13 μs (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out)

The rate at which Step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each Step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B-D_3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state, but during the execution phase it is in the Nonbusy state. While the FDC is in the Nonbusy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a Not Ready state at the beginning of the command execution phase or during the Seek operation, then the NR (Not Ready) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write three bytes of Seek command exceeds 150μs, the timing between the first two step pulses may be shorter than set in the Specify command by as much as 1ms.

Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 step pulses have been issued, the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s (highs) and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command. If the Diskette has more than 77 tracks, then Recalibrate command should be issued twice, in order to position the Read/Write head to the Track 0.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

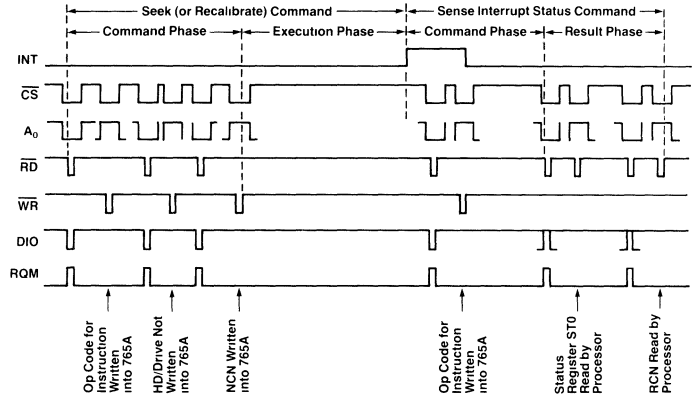
Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command when issued resets the Interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

Table 3

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk drive has reached the desired head position the μPD765A/μPD7265 will set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. A graphic example is shown:

Seek, Recalibrate, and Sense Interrupt Status



Specify

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 = 32ms . . . $0F_{16}$ = 240ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1ms, E = 2ms, D = 3ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2ms, 02 = 4ms, 03 = 6ms . . . 7F = 254ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8MHz clock; if the clock was reduced to 4MHz (minifloppy application) then all time intervals are increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1) the Non-DMA mode is selected, and when ND = 0 the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

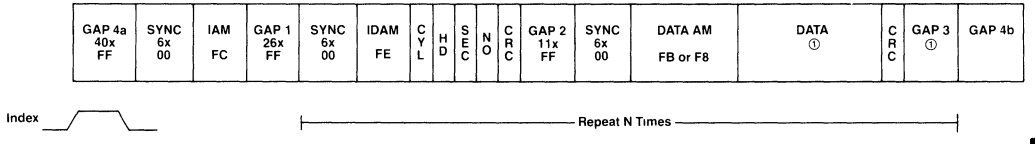
Invalid

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the μPD765A/μPD7265 during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the μPD765A/μPD7265 is in the Result phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80 hex, indicating an Invalid command was received.

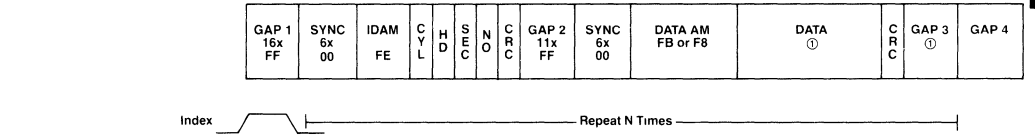
A Sense Interrupt Status command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid command.

In some applications the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

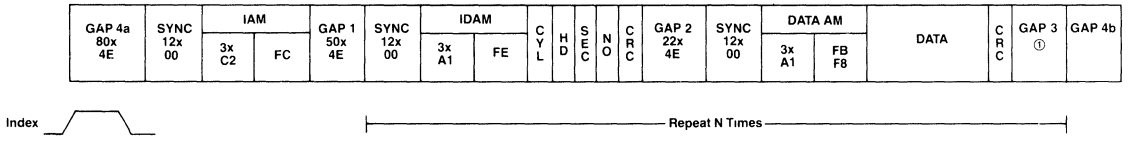
μPD765A (FM Mode)



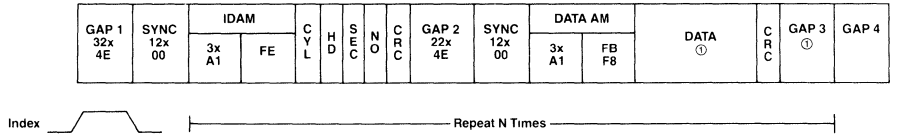
μPD7265 (FM Mode)



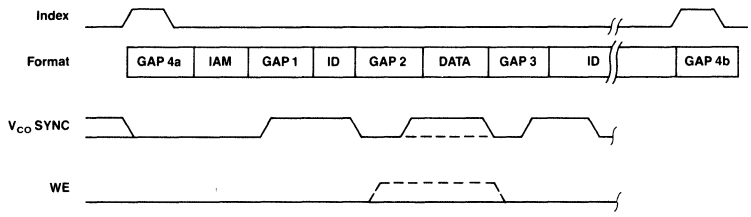
μPD765A (MFM Mode)



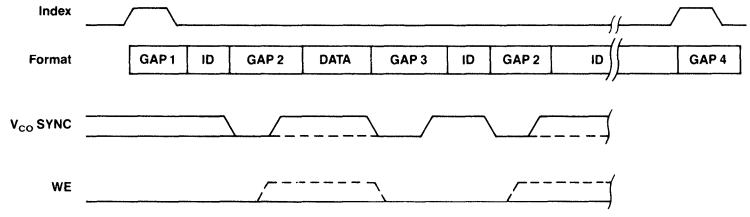
μPD7265 (MFM Mode)



μPD765A



μPD7265



Note: _____ Read
_ _ _ _ Write

Notes: It is suggested that the user refer to the following application notes
① #8 — for an example of an actual interface as well as a theoretical data separator
② #10 — for a well documented example of a working phase – locked loop

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD765AC/7265C
Ceramic, μPD765AD/7265D

NEC

PRELIMINARY

μPD7201A
MULTIPROTOCOL SERIAL COMMUNICATION CONTROLLER

Description

The μPD7201A is a dual-channel multifunction peripheral communication controller designed to satisfy a wide variety of serial data communication requirements in computer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller and within that role it is configurable by systems software so its "personality" can be optimized for a given serial data communications application.

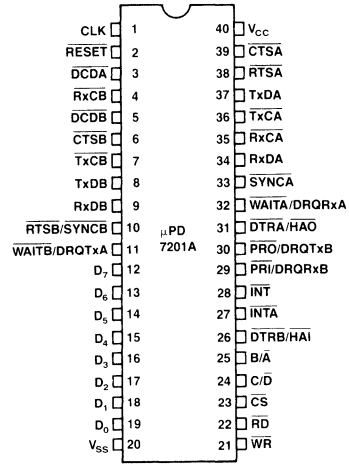
The μPD7201A is capable of handling asynchronous and synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device can also be used to support virtually any other serial protocol for applications other than data communications.

The μPD7201A can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. In applications where these controls are not needed the modem controls can be used for general-purpose I/O.

Features

- ☐ Two fully independent duplex serial channels
- ☐ Four independent DMA channels for send/received data for both serial inputs/outputs
- ☐ Programmable interrupt vectors and interrupt priorities
- ☐ Modem controls signals
- ☐ Variable software programmable data rate, up to 1.25M baud at 5MHz clock
- ☐ Double buffered transmitter data and quadruply buffered received data
- ☐ Programmable CRC algorithm
- ☐ Selection of Interrupt, DMA or Polling mode of operation
- ☐ Asynchronous operation
  - Character length: 5, 6, 7, or 8 bits
  - Stop bits: 1, 1½, 2
  - Transmission speed: x1, x16, x32, or x64 clock frequency
  - Parity: odd, even, or disable
  - Break generation and detection
  - Interrupt on parity, overrun, or framing errors
- ☐ Monosync, bisync, and external sync operations
  - Software selectable sync characters
  - Automatic sync insertion
  - CRC generation and checking
- ☐ HDLC and SDLC operations
  - Abort sequence generation and detection
  - Automatic zero insertion and detection
  - Address field recognition
  - CRC generation and checking
  - I-field residue handling
- ☐ N-channel MOS technology
- ☐ Single +5V power supply; interface to most microprocessors including 8080, 8085, 8086, and others.
- ☐ Single-phase TTL clock
- ☐ Available in plastic and ceramic dual-in-line packages

Pin Configuration



Pin Identification

Pin No.	Symbol	Name	I/O	Description
1	CLK	System Clock	I	A TTL-level system clock signal is applied to this input. The system clock frequency must be at least 4.5 times the data clock frequency applied to any of the data clock inputs (TxCA, TxCB, RxCA, or LRxCB).
2	RESET	Reset	I	A low on this input (one complete CLK cycle minimum) initializes the MPSC² to the following conditions: disables the receivers and transmitters; sets TxDA and TxDB to marking (high); and sets the modem control outputs (DTRA, DTRB, RTSA, RTSB) high. Additionally, all interrupts are disabled and all interrupt and DMA requests are cleared. All control registers must be rewritten after a reset and before a restart. (Active low)
3, 5	DCDA, DCDB	Data Carrier Detect	I	Data carrier detect generally indicates the presence of valid serial data at RxD. The MPSC² may be programmed so that the receiver is enabled only when DCD is low, and also so that any change in state that lasts longer than the minimum specified pulse width causes an interrupt and latches the DCD status bit to the new state. (Active low)
4, 35	RxCA, RxCB	Receiver Clocks	I	The receiver clock controls the sampling and shifting of serial data at RxD. The MPSC² may be programmed so that the clock rate is 1x, 16x, 32x, or 64x the data rate. RxD is sampled on the rising edge of RxC. RxC features a Schmitt-trigger input for relaxed rise and fall time requirements. (Active low)
6, 39	CTSA, CTSB	Clear to Send	I	Clear to send generally indicates that the receiving modem or peripheral is ready to receive data from the MPSC². The MPSC² may be programmed so that the transmitter is enabled only when CTS is low. As with DCD, the MPSC² may be programmed to cause an interrupt and latch the new state when CTS changes state for longer than the minimum specified pulse width. (Active low)

6

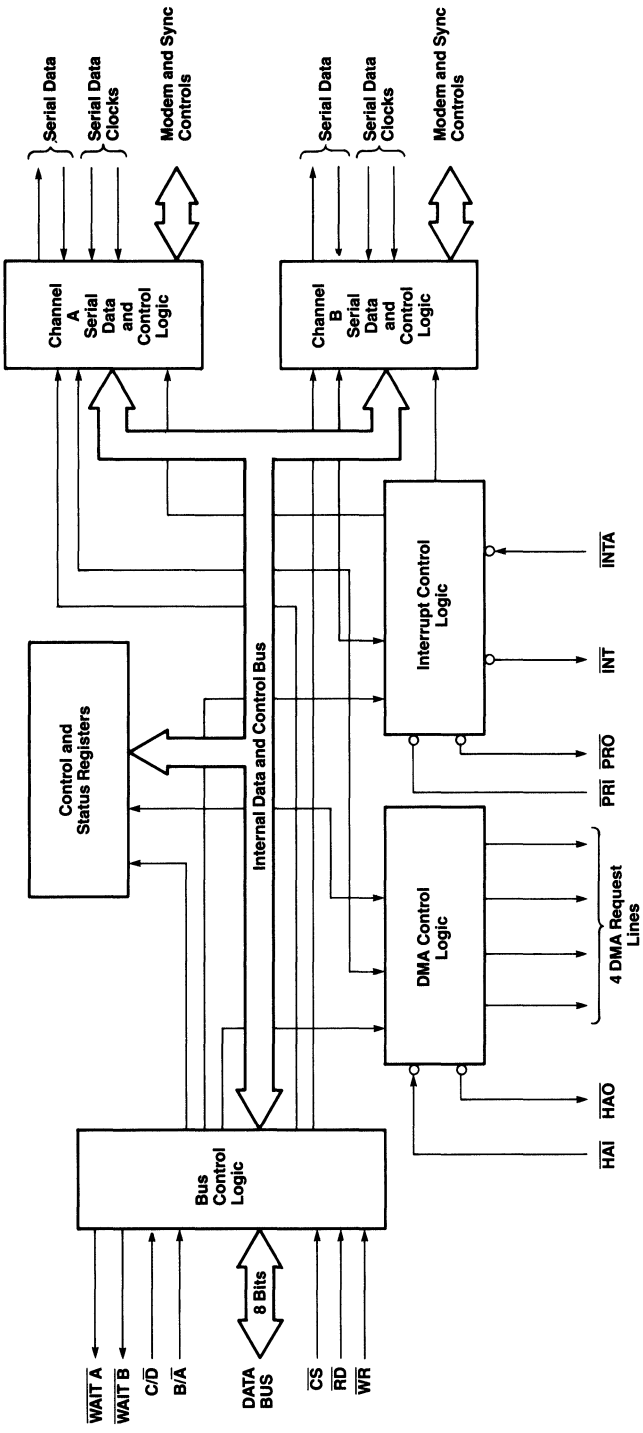
Pin Identification

Pin No.	Symbol	Name	I/O	Description
7, 36	TxCA, TxCB	Transmitter Clocks	I	The transmitter clock controls the rate at which data is shifted out at TxD. The MPSC² may be programmed so that the clock rate is 1x, 16x, 32x, or 64x the data rate. Data changes on the falling edge of TxC. TxC features a Schmitt-trigger input for relaxed rise and fall time requirements. (Active low)
8, 37	TxDA, TxDB	Transmit Data	O	Serial data from the MPSC² is output on these pins. (Marking high)
9, 34	RxDA, RxDB	Receive Data	I	Serial data to the MPSC² is input on these pins. (Marking high)
10, 33	SYNCA, SYNCB	Synchronization (Sync)	I/O	The function of the Sync pin depends on the MPSC² operating mode. In asynchronous mode, Sync is an input that the processor can read. It can be programmed to generate an interrupt in the same manner as DCD or CTS. In external sync mode, SYNC is also an input that notifies the MPSC² that synchronization has been achieved. (See the timing waveforms for details). Once synchronization is achieved, SYNC should be held low until synchronization is lost or a new message is about to start. In internal synchronization modes (monosync, bisync, SDLC), SYNC is an output which is active wherever a Sync character match is made. There is no qualifying logic associated with this function. Regardless of character boundaries, SYNC is active on any match. (Active low)
10, 38	RTSA, RTSB	Request to Send	O	When the MPSC² is operated in one of the synchronous modes, RTSA and RTSB are general-purpose outputs that may be set or reset with commands to the MPSC². In asynchronous mode, RTS is active immediately as soon as it is programmed on. However, when programmed off, RTS remains active until the transmitter is completely empty. This feature simplifies the programming required to perform modem control. (Active low)
11, 29, 30, 32,	DRQTxA, DRQTxB, DRQRxA, DRQRxB	DMA Request	O	When these lines are active, they indicate to a DMA controller that a transmitter or receiver is requesting a DMA data transfer. (Active high)
11, 32	WAITA WAITB	Wait	O	These outputs synchronize the processor with the MPSC² when block transfer mode is used. It may be programmed to operate with either the receiver or transmitter, but not both simultaneously. WAIT is normally inactive. For example, if the processor tries to perform an inappropriate data transfer such as write to the transmitter when the transmitter buffer is full, the WAIT output for the channel is active until the MPSC² is ready to accept the data. The CS, C/D, B/A, RD and WR inputs must remain stable while WAIT is active. (Open drain)
12–19	D_0–D_7	Data Bus	I/O	The data bus lines are connected to the system data bus. Data or status from the MPSC² is output on these lines when CS and RD are active; data or commands are latched into the MPSC² on the rising edge of WR when CS is active. (Three-state)
20	V_{SS}	Ground		Ground.
21	WR	Write	I	This input (with either CS during a read cycle or HAI during a DMA cycle) notifies the MPSC² to write data or control information to the device. (Active low)
22	RD	Read	I	This input (with either CS during a read cycle or HAI during a DMA cycle) notifies the MPSC² to read data or status from the device. (Active low)
23	CS	Chip Select	I	Chip select allows the MPSC² to transfer data or commands during a read or write cycle. (Active low)

Pin Identification

Pin No.	Symbol	Name	I/O	Description
24	C/D	Control/Data Select	I	This input, with RD, WR, and B/A selects the data register (C/D = 0) or the control and status registers (C/D = 1) for access over the data bus.
25	B/A	Channel Select	I	A low selects channel A and a high selects channel B for access during a read or write cycle.
26	HAI	Hold Acknowledge In	I	This input notifies the MPSC² that the host processor has acknowledged the DMA request and has placed itself in the hold state. The MPSC² then performs a DMA cycle for the highest priority outstanding DMA request, if any. (Active low)
26 , 31	DTRA, DTRB	Data Terminal Ready	O	The DTR pins are general-purpose outputs which may be set or reset with commands to the MPSC² (Active low)
27*	INTA	Interrupt Acknowledge	I	The processor generates two or three INTA pulses (depending on the processor type) to signal all peripheral devices that an interrupt acknowledge sequence is taking place. During the interrupt acknowledge sequence, the MPSC², if so programmed, places information on the data bus to vector the processor to the appropriate interrupt service location. (Active low)
28	INT	Interrupt Request	O	INT is pulled low when an internal interrupt request is accepted. (Active low, open drain)
29	PRI	Interrupt Priority In	I	This input informs the MPSC² that the highest priority device is requesting interrupt and is used with PRO to implement a priority resolution daisy chain when there is more than one interrupting device. The state of PRI and the programmed interrupt mode determine the MPSC²'s response to an interrupt acknowledge sequence. (Active low)
30	PRO	Interrupt Priority Out	O	This output is active when HAI is active and the MPSC² is not requesting interrupt (INT is inactive). The active state informs the next lower priority device that there are no higher priority interrupt requests pending during an interrupt acknowledge sequence. (Active low)
31	HAO	Hold Acknowledge Out	O	This output, with HAI implements a priority daisychain for multiple DMA devices. HAO is active when HAI is active and there are no DMA requests pending in the MPSC². (Active low)

Block Diagram



Programming the MPSC²

The software operation of the MPSC² is very straightforward. Its consistent register organization and high-level command structure help minimize the number of operations required to implement complex protocol designs. Programming is further simplified by the MPSC²'s extensive interrupt and status reporting capabilities. This section is divided into two parts.

The MPSC² Registers

The MPSC² interfaces to the system software with a number of control and status registers associated with each channel. Commonly used commands and status bits are accessed directly through control and status registers 0. Other functions are accessed indirectly with a register pointer to minimize the address space that must be dedicated to the MPSC².

Control Register

Control Register	Function
0	Frequently used commands and register pointer control
1	Interrupt control
2	Processor/bus interface control
3	Receiver control
4	Mode control
5	Transmitter control
6	Sync/address character
7	Sync character

Status Register

Status Register	Function
0	Buffer and "external/status" status
1	Received character error and special condition status
2 (Channel B only)	Interrupt vector
3	Tx byte count register, low byte
4	Tx byte count register, high byte

All control and status registers except CR2 are separately maintained for each channel. Control and status registers 2 are linked with the overall operation of the MPSC² and have different meanings when addressed through different channels.

When initializing the MPSC² control register 2A (and 2B if desired) should be programmed first to establish the MPSC² processor/bus interface mode. Each channel may then be programmed to be used separately, beginning with control register 4 to set the protocol mode for that channel. The remaining registers may then be programmed in any order.

Control Register 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CRC Control Command		Command			Register Pointer		

Register pointer ($D_0 - D_2$)

The register pointer specifies which register number is accessed at the next control register write or status register read. After a hardware or software reset the register pointer is set to zero. Therefore, the first control byte goes to control register 0. When the register pointer is set to a value other than zero the next control or status ($C/\overline{D} = 1$) access is to the specified register, after which the pointer is reset to zero. Other commands can be freely combined in control register 0 by setting the register pointer.

Commands ($D_3 - D_5$)

Commands commonly used during the operation of the MPSC² are grouped in control register 0. They include the following:

Null (000): This command has no effect and is used only to set the register pointer or issue a CRC command.

Send abort (001): When operating in the SDLC mode this command causes the MPSC² to transmit the SDLC abort code, issuing 8 to 13 consecutive ones. Any data currently in the transmitter or the transmitter buffer is destroyed. After sending the abort the transmitter reverts to the idle phase (flags). When using the Tx byte count mode enable (D_6 of CR1), and an underrun condition occurs, the μPD7201A will automatically issue the send abort command.

Reset external status interrupts (010): When the external/status change flag is set, the condition of bits $D_3 - D_7$ of status register 0 are latched to allow the capture of the short pulses that may occur. The reset external/status interrupts command reenables the latches so that new interrupts may be sensed.

Channel reset (011): This command has the same effect on a single channel as an external reset at pin 2. A channel reset command to channel A resets the internal interrupt prioritization logic. This does not occur when a channel reset command is issued to channel B. All control registers associated with the channel to be reset must be reinitialized. After a channel reset, wait at least four system clock cycles before writing new commands or controls to that channel.

Enable interrupt on next character (100): When operating the MPSC² in an interrupt on first received character mode this command may be issued at any time. This command must be issued at the end of a message to reenable the interrupt logic for the next received character (the first character of the next message).

Reset pending transmitter interrupt/DMA request (101): A pending transmitter buffer becoming empty interrupt or DMA request can be reset without sending another character by issuing this command (typically at the end of a message). A new transmitter buffer becoming empty interrupt or DMA request is not made until another character has been loaded and transferred to the transmitter shift register or when, if operating in the synchronous or SDLC modes, the first CRC character has been sent.

Error Reset (110): This command resets a special receive condition interrupt. It also reenables the parity and overrun error latches that allow errors at the end of a message to be checked.

End of interrupt (111) (channel A only): Once an interrupt request has been issued by the MPSC² all lower priority internal and external interrupts in the daisychain are held off to permit the current interrupt to be serviced while allowing higher priority interrupts to occur. At some point in the interrupt service routine (generally at the end), the end of interrupt command must be issued to channel A to reenable the daisychain and allow any pending lower priority internal interrupt requests to occur. The EOI command must be sent to channel A for interrupts that occurred on either channel.

CRC Control Commands ($D_6 - D_7$)
The following commands control the operation of the CRC generator/checker logic.

Null (00): This command has no effect and is used when issuing other commands or setting the register pointer.

Reset receiver CRC checker (01): This command resets the CRC checker to zero when the channel is in a synchronous mode and resets to all ones when in an SDLC mode.

Reset transmitter CRC generator (10): This command resets the CRC generator to zero when the channel is in a synchronous mode and resets to all ones when in an SDLC mode.

Reset idle/CRC latch (11): This command resets the idle/CRC latch so that when a transmitter underrun condition occurs (that is, the transmitter has no more characters to send), the transmitter enters the CRC phase of operation and begins to send the 16-bit CRC character calculated up to that point. The latch is then set so that if the underrun condition persists, idle characters are sent following the CRC. After a hardware or software reset the latch is in the set state. This latch is automatically reset after the first character has been loaded into the Tx buffer in the SDLC mode.

Control Register 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Wait Function Enable	Tx Byte Count Mode Enable	Wait on Receiver Transmitter	Receiver Interrupt Mode		Condition Affects Vector	Transmitter Interrupt Enable	Ext/Status INT Enable

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Low Byte							

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
High Byte							

External/status interrupt enable (D_0)
When this bit is set to one the MPSC² issues an interrupt whenever any of the following conditions occur:

- Transition of the $\overline{DCD}$ input pin
- Transition of the $\overline{CTS}$ input pin
- Transition of the $\overline{SYNC}$ input pin
- Entering or leaving synchronous hunt phase, break detection or termination
- SDLC abort detection or termination
- Idle/CRC latch becoming set (CRC being sent)
- After ending flag is sent in the SDLC mode

Transmitter interrupt enable (D_1)
When this bit is set to one the MPSC² issues an interrupt when:

1) The character currently in the transmitter buffer is transferred to the shift register (transmitter buffer becoming empty) or,
2) The transmitter enters the idle phase and begins transmitting sync or flag characters.
3) The Tx byte mode enable bit is set (CR1 – D6 = 1). The 7201A will automatically issue a Tx interrupt or DMA request when the transmitter becomes enabled (CR5 – D3 = 1).

Condition affects vector (D_2) (programmed in channel B for both channels)
When this bit is set to zero the fixed vector programmed in CR2B during MPSC² initialization is returned in an interrupt acknowledge sequence. When this bit is set to one the vector is modified to reflect the condition that caused the interrupt.

Receiver interrupt mode ($D_3 - D_4$)
This field controls how the MPSC²'s interrupt/DMA logic handles the character received condition.

Receiver interrupts/DMA request disabled (00)
The MPSC² does not issue an interrupt or a DMA request when a character has been received.

Interrupt/DMA on first received character only (01)
In this mode the MPSC² issues an interrupt only for the first character received after an enable interrupt/DMA on first character command (CR0) has been given. If the channel is in a DMA mode, a DMA request is issued for each character received including the first. This mode generally is used whenever the MPSC² is in a DMA or block transfer mode. This will signal the processor that the beginning of an incoming message has been received.

Interrupt (and issue a DMA request) on all received characters (10)
In this mode an interrupt (and DMA request if the DMA mode is selected) is issued whenever there is a character present in the receiver buffer. A parity error is considered a special receive condition.

Interrupt (and issue a DMA request) on all received characters (11)
This mode is the same as the one above except that a parity error is not considered a special receive condition. The following are considered special receive conditions:

- Receiver overrun factor
- Asynchronous framing error
- Parity error (if specified)
- SDLC end of message (final flag received)

Wait on receiver/transmitter (D_5)
If the wait function is enabled for block mode transfers, setting this bit to zero causes the MPSC² to issue a wait ($\overline{WAIT}$ output goes low) when the processor attempts to write a character to the transmitter while the transmitter buffer is full. Setting this bit to one causes the MPSC² to issue a wait when the processor attempts to read a character from the receiver while the receiver buffer is empty.

Tx byte count mode enable (D_6)

Each channel has a 16-bit Tx byte count register used for automatic transmit termination. When this bit is set to one the next two consecutive command cycle writes will be to the byte count register. The first byte is loaded into the lower 8 bits and the second to the upper 8 bits of the byte count register. The byte count register holds the number of transfers to be performed by the transmitter. A byte counter is incremented each time a transfer is performed until the value of the byte counter is equal to the value in the byte count register. When equal, interrupts or DMA requests will be stopped until the byte count enable bit is issued and a new byte count is loaded into the byte count register. If a transmit underrun occurs in the SDLC mode, and the byte count is not equal to the byte count register, the abort sequence will be sent automatically.

Also, when using the Tx byte count mode, a transmit interrupt or DMA request will automatically become active after issuing the Tx enable command to CR5.

The Tx byte count mode can be cleared by either a channel reset command or a hardware reset.

Wait function enable (D_7)

Setting this bit to one enables the wait function which is described in CR1.

Control Register 2 (Channel A)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Pin 10 SYNCB/RTSB	Rx INT Mask	Interrupt Vector Mode			Priority	DMA Mode Select	

DMA mode select ($D_0 - D_1$)

Setting this field determines whether channel A or B is used in a DMA mode (i.e., data transfers are performed by a DMA controller) or in a non-DMA mode where transfers are performed by the processor in either a polled, interrupt, or block transfer mode. The functions of some MPSC² pins are also controlled by this field.

DMA Mode Selection

		Channel		Pin Function					
D_1	D_0	A	B	11	26	29	30	31	32
0	0	Non-DMA	Non-DMA	WAITB	DTRB	PRI	PRO	DTRA	WAITA
0	1	DMA	Non-DMA	DRQTxA	HAI	PRI	PRO	HAO	DRQRxA
1	0	DMA	DMA	DRQTxA	HAI	DRQRxB	DRQTxB	HAO	DRQRxA
1	1	DMA	DMA	DRQTxA	DTRB	DRQRxB	DRQTxB	DTRA	DRQRxA

Priority (D_2)

This bit selects the relative priorities of the various interrupt and DMA conditions according to the application requirements.

DMA/Interrupt Priorities

D_2	Mode: Channel A	Mode: Channel B	DMA Priority Relation	Interrupt Priority Relation
0	INT	INT	—	SRxA, RxA > TxA > SRxB, RxB > TxB > ExTA > ExTB
1			—	SRxA, RxA > SRxB, RxB > TxA > TxB > ExTA > ExTB
0	DMA	INT	RxA > TxA	SRxA, RxA > SRxB, RxB > TxB > ExTA > ExTB
1			RxA > TxA	SRxA, RxA > SRxB, RxB > TxB > ExTA > ExTB
0	DMA	DMA	RxA > TxA > RxB > TxB	SRxA, RxA > SRxB, RxB > ExTA > ExTB
1			RxA > RxB > TxA > TxB	SRxA, RxA > SRxB, RxB > ExTA > ExTB

Interrupt vector mode ($D_3 - D_5$)

This field determines how the MPSC² responds to an interrupt acknowledge sequence from the processor.

Interrupt Acknowledge Sequence Response

D_5	D_4	D_3	Mode	Status Register 2B and Interrupt Vector Bits Affected When Condition Affects Vector Is Enabled
0	0	0	Nonvectored	$D_4\ D_3\ D_2$
0	0	1	Nonvectored	$D_4\ D_3\ D_2$
0	1	0	Nonvectored	$D_2\ D_1\ D_0$
0	1	1	Illegal	—
1	0	0	8085 Master	$D_4\ D_3\ D_2$
1	0	1	8085 Slave	$D_4\ D_3\ D_2$
1	1	0	8086	$D_2\ D_1\ D_0$
1	1	1	8085/8259A Slave	$D_4\ D_3\ D_2$

Rx INT mask (D_6)

This option is generally used in the DMA modes. Enabling this bit inhibits the interrupt from occurring when the interrupt/DMA Request On First Received Character mode is selected. In other words, only a DMA request will be generated when the first character is received.

Pin 10 $\overline{\text{SYNCB}}/\overline{\text{RTSB}}$ select (D_7)

Programming a zero into this bit selects $\overline{\text{RTSB}}$ as the function of pin 10. A one selects $\overline{\text{SYNCB}}$ as the function.

Control Register 2 (Channel B)

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector							

Interrupt vector ($D_0 - D_7$)

When the MPSC² is used in the vectored interrupt mode the contents of this register is placed on the bus during the appropriate portion of the interrupt acknowledge sequence. Its value is modified if status affects vector is enabled. The value of SR2B can be read at any time. This feature is particularly useful in determining the cause of an interrupt when using the MPSC² in a nonvectored interrupt mode.

Control Register 3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Number of Received Bits per Character		Auto Enables	Enter Hunt Phase	Receiver CRC Enable	Address Search Mode	Sync Character Load Inhibit	Receiver Enable

Receiver enable (D_0)

After the channel has been completely initialized, setting this bit to one allows the receiver to begin operation. This bit may be set to zero at any time to disable the receiver.

Sync character load inhibit (D_1)

In the character synchronous modes, this bit inhibits the transfer of sync characters to the receiver buffer thus performing a "sync-stripping" operation. When using the MPSC²'s CRC checking ability this feature should be used only to strip leading sync characters preceding a message since the load inhibit does not exclude sync characters embedded in the message from the CRC calculation. Synchronous protocols using other types of block checking such as checksum or LRC are free to strip embedded sync characters with this bit.

Address search mode (D_2)

In the SDLC mode, setting this bit places the MPSC² in an address search mode. Character assembly does not begin until the 8-bit character (secondary address field) following the starting flag of a message matches either the address programmed into CR6 or the global address 11111111.

Receiver CRC enable (D_3)

This bit enables and disables (1 = enable) the CRC checker in the COP mode allowing characters from the CRC calculation to be selectively included or excluded. The MPSC² features a one-character delay between the receiver shift register and the CRC checker so that the enabling or disabling takes effect with the last character transferred from the shift register to the receiver buffer. Therefore, there is one full character time in which to read the character and decide whether or not it should be included in the CRC calculation. In the SDLC mode, there is no 8-bit delay.

Enter hunt phase (D_4)

Although the MPSC² receiver automatically enters the sync hunt phase after a reset, there are times when reentry may be desired, such as when it has been determined that synchronization has been lost or, in an SDLC mode, to ignore the current incoming message. Writing a one into this bit at any time after initialization causes the MPSC² to reenter the hunt phase.

Auto enables (D_5)

Setting this bit to one causes the $\overline{DCD}$ and $\overline{CTS}$ inputs to act as enable inputs to the receiver and transmitter, respectively.

Number of received bits per character ($D_6 - D_7$)

This field specifies the number of data bits assembled to make each character. The value may be changed on the fly while a character is being assembled and, if the change is made before the new number of bits has been reached it affects that character. Otherwise the new specifications take effect on the next character received.

Received Bits per Character

D_7	D_6	Bits per Character
0	0	5
0	1	7
1	0	6
1	1	8

Control Register 4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Clock Rate		Sync Mode		Number of Stop Bits per Sync Mode		Parity Even/Odd	Parity Enable

Parity enable (D_0)

Setting this bit to one adds an extra data bit containing parity information to each transmitted character. Each received character is expected to contain this extra bit and the receiver parity checker is enabled.

Parity even/odd (D_1)

Programming a zero into this bit when parity is enabled causes the transmitted parity bit to take on the value required for odd parity. The received character is checked for odd parity. Conversely, a one in this bit signifies even parity generation and checking.

Number of stop bits per sync mode ($D_2 - D_3$)

This field specifies whether the channel is used in a synchronous (SDLC) or an asynchronous mode. In an asynchronous mode this field also specifies the number of bit times used as the stop bit length by the transmitter. The receiver always checks for one stop bit.

Stop Bits

D_3	D_2	Mode
0	0	Synchronous modes
0	1	Asynchronous 1-bit time (1 stop bit)
1	0	Asynchronous 1½ bit times (1½ stop bits)
1	1	Asynchronous 2-bit times (2 stop bits)

Sync mode ($D_4 - D_5$)

When the stop bits/sync mode field is programmed for synchronous modes (D_2, D_3 = 00), this field specifies the particular synchronous format to be used. This field is ignored in an asynchronous mode.

Synchronous Formats

Sync Mode 1	Sync Mode 2	
D_5	D_4	Mode
0	0	8-bit internal synchronization character (monosync)
0	1	16-bit internal synchronization character (bisync)
1	0	SDLC
1	1	External synchronization (SYNC pin becomes an input)

Clock rate ($D_6 - D_7$)

This field specifies the relationship between the transmitter and receiver clock inputs ($\overline{TxC}$, $\overline{RxC}$) and the actual data rates at TxD and RxD. When operating in a synchronous mode a 1x clock rate must be specified. In asynchronous modes any of the rates may be specified, however, with a 1x clock rate the receiver cannot determine the center of the start bit. In this mode, the sampling (rising) edge of $\overline{RxC}$ must be externally synchronized with the data.

Clock Rates

Clock Rate 1	Clock Rate 2	
D_7	D_6	Clock Rate
0	0	Clock Rate = 1x Data Rate
0	1	Clock Rate = 16x Data Rate
1	0	Clock Rate = 32x Data Rate
1	1	Clock Rate = 64x Data Rate

Control Register 5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
DTR	Number of Transmitted Bits per Character		Send Break	Transmitter Enable	CRC Polynomial Select	$\overline{RTS}$	Transmitter CRC Enable

Transmitter CRC enable (D_0)

A one or a zero enables or disables respectively, the CRC generator calculation. The enable or disable does not take effect until the next character is transferred from the transmitter buffer to the shift register, thus allowing specific characters to be included or excluded from the CRC calculation. By setting or resetting this bit just before loading

the next character, it and subsequent characters are included or excluded from the calculation. If this bit is zero when the transmitter becomes empty the MPSC² goes to the idle phase regardless of the state of the idle/CRC latch.

$\overline{RTS}$ (D_1)

In synchronous and SDLC modes setting this bit to one causes the $\overline{RTS}$ pin to go low while a zero causes it to go high. In an asynchronous mode setting this bit to zero does not cause $\overline{RTS}$ to go high until the transmitter is completely empty. This feature facilitates programming the MPSC² for use with asynchronous modems.

CRC polynomial select (D_2)

This bit selects the polynomial used by the transmitter and receiver for CRC generation and checking. A one selects the CRC-16 polynomial ($x^{16} + x^{15} + x^2 + 1$). A zero selects the CRC-CCITT polynomial ($x^{16} + x^{12} + x^5 + 1$). In an SDLC mode CRC-CCITT must be selected. Either polynomial may be used in other synchronous modes.

Transmitter enable (D_3)

After a reset the transmitted data output (TxD) is held high (marking) and the transmitter is disabled until this bit is set.

In an asynchronous mode TxD remains high until data is loaded for transmission.

In synchronous and SDLC modes the MPSC² automatically enters the idle phase and sends the programmed sync or flag characters.

When the transmitter is disabled in an asynchronous mode any character currently being sent is completed before TxD returns to the marking state.

If the transmitter is disabled during the data phase in a synchronous mode the current character is sent. TxD then goes high (marking). In an SDLC mode the current character is sent, but the marking line following is zero-inserted. That is, the line goes low for one bit time out of every five.

The transmitter should never be disabled during the SDLC data phase unless a reset is to follow immediately. In either case, any character in the buffer register is held.

Disabling the transmitter during the CRC phase causes the remainder of the CRC character to be bit-substituted with the sync (or flag). The total number of bits transmitted is correct and TxD goes high after they are sent.

If the transmitter is disabled during the idle phase the remainder of the sync (flag) character is sent. TxD then goes high.

Send break (D_4)

Setting this bit to one immediately forces the transmitter output (TxD) low (spacing). This function overrides the normal transmitter output and destroys any data being transmitted although the transmitter is still in operation. Resetting this bit releases the transmitter output.

Transmitted bits per character ($D_5 - D_6$)

This field controls the number of data bits transmitted in each character. The number of bits per character may be changed by rewriting this field just before the first character is loaded to use the new specification.

Transmitted Bits per Character

Transmitted Bits per Character 1 (D_6)	Transmitted Bits per Character (D_5)	Bits per Character
0	0	5 or less (see below)
0	1	7
1	0	6
1	1	8

Normally each character is sent to the MPSC² right-justified and the unused bits are ignored. However, when sending five bits or less the data should be formatted as shown below to inform the MPSC² of the precise number of bits to be sent.

Transmitted Bits per Character for 5 Characters or Less

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Number of Bits per Character
1	1	1	1	0	0	0	D_0	1
1	1	1	0	0	0	D_1	D_0	2
1	1	0	0	0	D_2	D_1	D_0	3
1	0	0	0	D_3	D_2	D_1	D_0	4
0	0	0	D_4	D_3	D_2	D_1	D_0	5

$\overline{DTR}$ (data terminal ready) (D_7)

When this bit is one the $\overline{DTR}$ output is low (active). Conversely, when this bit is zero $\overline{DTR}$ is high.

Control Register 6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Sync Byte 1							

Sync byte 1 ($D_0 - D_7$)

Sync byte 1 is used in the following modes:

Monosync	8-bit sync character transmitted during the idle phase
Bisync	Least significant (first) 8 bits of the 16-bit transmit and receive sync character
External Sync	Sync character transmitted during the idle phase
SDLC	Secondary address value matched to secondary address field of the SDLC frame when the MPSC² is in the address search mode

Control Register 7

D_7	D_6	D_5	D_4		D_2	D_1	D_0
Sync Byte 2							

Sync byte 2 ($D_0 - D_7$)

Sync byte 2 is used in the following modes:

Monosync	8-bit sync character matched by the receiver
Bisync	Most significant (second) 8 bits of the 16-bit transmit and receive sync characters
SDLC	The flag character, 01111110, must be programmed into control register 7 for flag matching by the MPSC² receiver

Status Register 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Break/ Abort	Idle/CRC	CTS	Sync Status	DCD	Transmitter Buffer Empty	Interrupt Pending	Received Character Available

Received character available (D_0)

When this bit is set it indicates that one or more characters in the receiver buffer is available for the processor to read. Once all the available characters have been read the MPSC² resets this bit until a new character is received.

Interrupt pending (D_1 — channel A only)

The interrupt pending bit is used with the interrupt vector register (status register 2) to make it easier to determine the MPSC²'s interrupt status, particularly in a nonvectored interrupt mode where the processor must poll each device to determine the interrupt source. In this mode interrupt pending is set when status register 2B is read, the $\overline{PRI}$ input is active (low), and the MPSC² is requesting interrupt service.

The status registers of both channels need not be analyzed to determine if an interrupt is pending. If the status affects vector is enabled and the interrupt pending is set the vector read from SR2 contains valid condition information.

In a vectored interrupt mode interrupt pending is set during the interrupt acknowledge cycle (on the leading edge of the second $\overline{INTA}$ pulse) when the MPSC² is the highest priority device requesting interrupt service ($\overline{PRI}$ is active). In either mode if there are no other pending interrupt requests interrupt pending is reset when the end of the interrupt command is issued.

Transmitter buffer empty (D_2)

This bit is set whenever the transmitter buffer is empty except during the transmission of CRC. (The MPSC² uses the buffer to facilitate this function.) After a reset the buffer is considered empty and transmit buffer empty is set.

External/status flags (D_3–D_7)

The following status bits reflect the state of the various conditions that cause an external/status interrupt. The MPSC² latches all external/status bits whenever a change occurs that would cause an external/status interrupt (regardless of whether this interrupt is enabled). This allows transient status changes on these lines to be captured with relaxed software timing requirements.

When the MPSC² is operated in an interrupt-driven mode for external/status interrupts, status register 0 should be read when this interrupt occurs and a reset external/status interrupt command issued to reenable the interrupt and the latches. To poll these bits without interrupts, the reset external/status interrupt command can be issued to first update the status to reflect the current values.

$\overline{DCD}$ (D_3): This bit reflects the inverted state of the $\overline{DCD}$ input. When $\overline{DCD}$ is low the $\overline{DCD}$ status bit is high. Any transition on this bit causes an external/status interrupt request.

Sync status (D_4): The meaning of this bit depends on the operating mode of the MPSC².

Asynchronous mode: Sync status reflects the inverted state of the $\overline{SYNC}$ input. When $\overline{SYNC}$ is low, sync status is high. Any transition on this bit causes an external/status interrupt request.

External synchronization mode: Sync status operates in the same manner as an asynchronous mode. The MPSC²'s receiver synchronization logic is also tied to the sync status bit in an external synchronization mode and a low-to-high transition ($\overline{SYNC}$ input going low) informs the receiver that synchronization has been achieved and character assembly begins.

A low-to-high transition on the $\overline{SYNC}$ input indicates that synchronization has been lost and is reflected both in the sync status becoming zero and the generation of an external/status interrupt. The receiver remains in the receive data phase until the enter hunt phase bit in control register 3 is set.

Monosync, bisync, SDLC modes: In these modes, sync status indicates whether the MPSC² receiver is in the sync hunt or receive data phase of operation. A zero indicates that the MPSC² is in the receive data phase and a one indicates that the MPSC² is in the sync hunt phase (as after a reset or a setting of the enter sync hunt phase bit). As in the other modes a transition on this bit causes an external/status interrupt to be issued. It should be noted that entering a sync hunt phase after either a reset or when programmed causes an external/status interrupt request which may be cleared immediately with a reset external/status interrupt command.

$\overline{CTS}$ (D_5): This bit reflects the inverted state of the $\overline{CTS}$ input. When $\overline{CTS}$ is low, the $\overline{CTS}$ status bit is high. Any transition on this bit causes an external/status interrupt request.

Idle/CRC (D_6) (Tx underrun/EOM): This bit indicates the state of the idle/CRC latch used in the synchronous and SDLC modes. After a hardware reset this bit is set to one, indicating that the transmitter is completely empty. When the MPSC² enters idle phase it automatically transmits sync or flag characters.

In the SDLC mode the MPSC² automatically resets this latch after the first byte of a frame is written to the Tx buffer.

When the transmitter is completely empty, the MPSC² sends the 16-bit CRC character and sets the latch again. An external/status interrupt is issued when the latch is set, indicating that CRC is being sent. No interrupt is issued when the latch is reset.

Break/abort (D_7): In the asynchronous mode this bit indicates the detection of a break sequence (a null character plus framing error that occurs when the RxD input is held low, spacing, for more than one character time). Break/abort is reset when RxD returns high (marking).

In the SDLC mode, Break/abort indicates the detection of an abort sequence when seven or more ones are received in sequence. It is reset when a zero is received.

Any transition of the break/abort bit causes an external/status interrupt.

Status Register 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
End of SDLC Frame	CRC Framing Error	Overrun Error	Parity Error	SDLC Residue Code			All Sent

All sent (D_0)

This bit is set when the transmitter is empty and reset when a character is present in the transmitter buffer or shift register. This feature simplifies the modem control software routines. In the bit synchronous mode, this bit will be set when the ending flag pattern is sent.

SDLC residue code ($D_1 - D_3$)

Since the data portion of an SDLC message can consist of any number of bits and not necessarily an integral number of characters, the MPSC² features special logic to determine and report when the end of frame flag has been received, the boundary between the data field and the CRC character in the last few data characters that were just read.

When the end of frame condition is indicated, that is, status register 1 $D_7 = 1$ and special receive condition interrupt (if enabled), the last bits of the CRC character are in the receiver buffer. The residue code for the frame is valid in the status register 1 byte associated with that data character. (SR1 tracks the received data in its own buffer.)

The meaning of the residue code depends upon the number of bits per character specified for the receiver. The previous character refers to the last character read before the end of frame, and so forth.

Residue Codes

D_3	D_2	D_1	Previous Character	2nd Previous Character	
8 Bits per Character					
1	0	0	CCCCCCCC	CCCCCDDD	
0	1	0	CCCCCCCC	CCCCDDDD	
1	1	0	CCCCCCCC	CCCDDDDD	
0	0	1	CCCCCCCC	CCDDDDDD	
1	0	1	CCCCCCCC	CDDDDDDD	
0	1	1	CCCCCCCC	DDDDDDDD	(no residue)
1	1	1	CCCCCCCD	DDDDDDDD	
0	0	0	CCCCCCDD	DDDDDDDD	
7 Bits per Character					
1	0	0	CCCCCCC	CCCCCDD	
0	1	0	CCCCCCC	CCCCDDD	
1	1	0	CCCCCCC	CCCDDDD	
0	0	1	CCCCCCC	CCDDDDD	
1	0	1	CCCCCCC	CDDDDDD	
0	1	1	CCCCCCC	DDDDDDD	(no residue)
0	0	0	CCCCCCD	DDDDDDD	
6 Bits per Character					
1	0	0	CCCCCC	CCCCCD	
0	1	0	CCCCCC	CCCCDD	
1	1	0	CCCCCC	CCCDDD	
0	0	1	CCCCCC	CCDDDD	
1	0	1	CCCCCC	CDDDDD	
0	0	0	CCCCCC	DDDDDD	(no residue)
5 Bits per Character					
D_3	D_2	D_1	2nd Previous Character	3rd Previous Character	
1	0	0	CCCCC	DDDDD	(no residue)
0	1	0	CCCCD	DDDDD	
1	1	0	CCCDD	DDDDD	
0	0	1	CCDDD	DDDDD	
0	0	0	CDDDD	DDDDD	

Special receive condition flags

The status bits described below — parity error (if parity as a special receive condition is enabled), receiver overrun error, CRC/framing error, and end of SDLC frame — all represent special receive conditions.

When any of these conditions occur and interrupts are enabled, the MPSC² issues an interrupt request. In addition, if a condition affects vector mode is enabled, the vector generated (and the contents of SR2B for nonvectored interrupts) is different from that of a received character available condition. Thus, it is not necessary to analyze SR1 with each character to determine if an error has occurred.

As a further convenience, the parity error and receiver overrun error flags are latched. That is, once one of these errors occurs, the flag remains set for all subsequent characters until reset by the error reset command. With this facility SR1 need only be read at the end of a message to determine if either of these errors occurred anywhere in the message. The other flags are not latched and follow each character available in the receiver buffer.

Parity error (D_4): This bit is set and latched when parity is enabled and the received parity bit does not match the sense (odd or even) calculated from the data bits.

Receiver overrun error (D_5): This error occurs and is latched when the receiver buffer already contains three characters and a fourth character is completely received, overwriting the last character in the buffer.

CRC/framing error (D_6): In the asynchronous mode a framing error is flagged (but not latched) when no stop bit is detected at the end of a character (i.e., RxD is low one bit time after the center of the last data or parity bit). When this condition occurs, the MPSC² waits an additional one-half bit time before sampling again so that the framing error is not interpreted as a new start bit.

In the synchronous and SDLC modes this bit indicates the result of the comparison between the current CRC result and the appropriate check value and is usually set to one since a message rarely indicates a correct CRC result until correctly completed with the CRC check character. Note that a CRC error does not result in a special receive condition interrupt.

End of SDLC frame (EOF) (D_7): This status bit is used only in the bit synchronous mode to indicate that the end of frame flag has been received and that the CRC error flag and residue code are valid. This flag can be reset at any time by issuing an error reset command. The MPSC² also automatically resets this bit when the first character of the next message frame is sent.

Status Register 2B

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Interrupt Vector							

Interrupt vector ($D_0 - D_7$ — channel B only)

Reading status register 2B returns the interrupt vector that is programmed into control register 2B. If a condition affects vector mode is enabled the value of the vector is modified as shown in the following table.

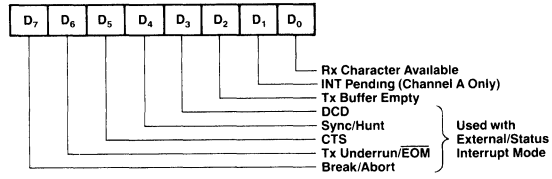
Condition Affects Vector Modifications

Interrupt Pending (SR0, D_1 Channel A)	8085 Modes / 8086 Modes	D_4 D_2	D_3 D_1	D_2 D_0	Condition
0		1	1	1	No interrupt pending
1		0	0	0	Channel B transmitter buffer empty
1		0	0	1	Channel B external/status change
1		0	1	0	Channel B received character available
1		0	1	1	Channel B special receive condition
1		1	0	0	Channel A transmitter buffer empty
1		1	0	1	Channel A external/status change
1		1	1	0	Channel A received character available
1		1	1	1	Channel A special receive condition

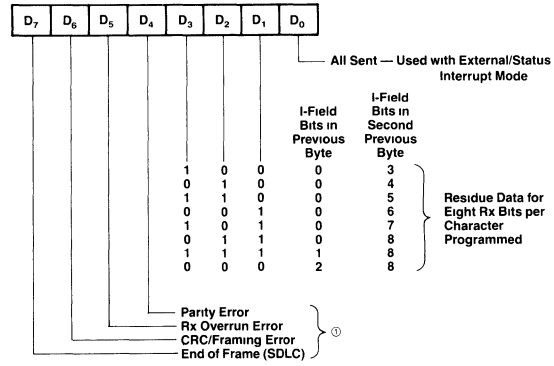
As can be seen code 111 can mean either channel A special receive condition or no interrupt pending. They can be easily distinguished by examining the interrupt pending bit (D_1) of status register 0, channel A. In a nonvectored interrupt mode the vector register must be read first for the interrupt pending to be valid.

Read Register Bit Functions

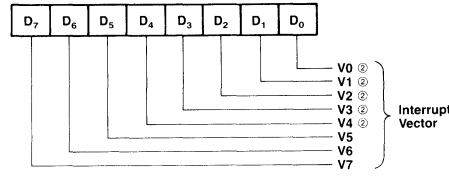
Read Register 0



*Read Register 1*①



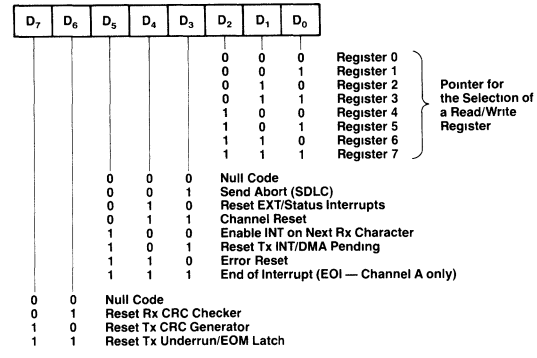
Read Register 2



Notes: ① Used with special receive condition mode
② Variable if Status Affects Vector is programmed

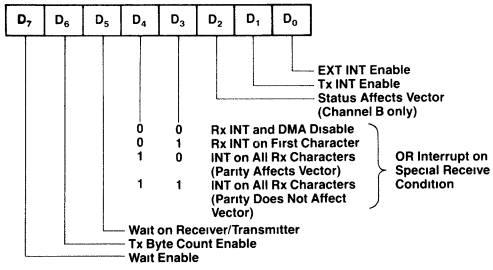
Write Register Bit Functions

Write Register 0

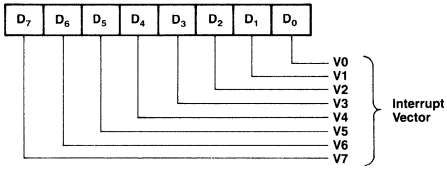


Write Register Bit Functions (Cont.)

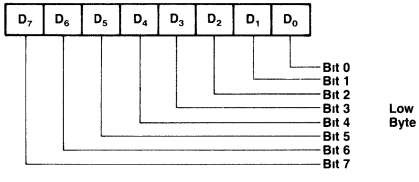
Write Register 1



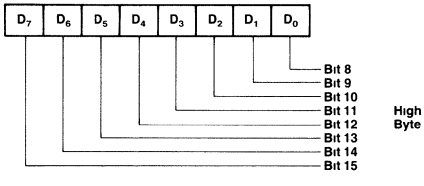
Write Register 2 (Channel B)



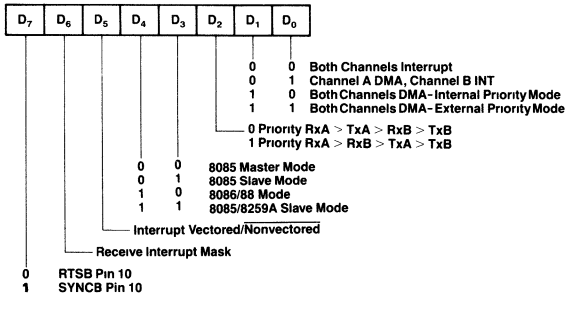
Tx Byte Count Register



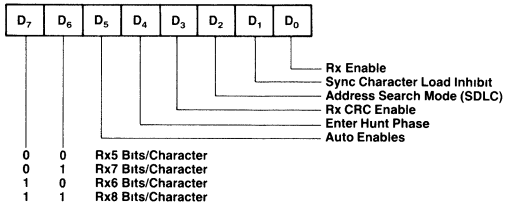
Tx Byte Count Register



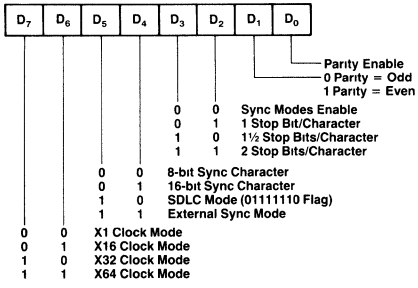
Write Register 2 (Channel A)



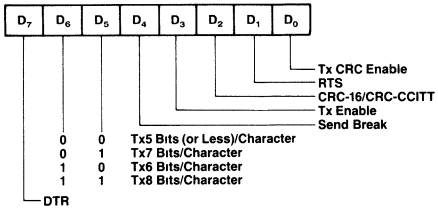
Write Register 3



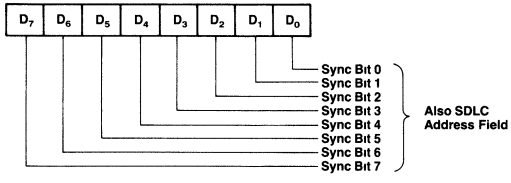
Write Register 4



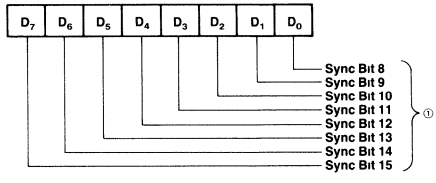
Write Register 5



Write Register 6



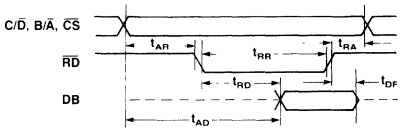
Write Register 7



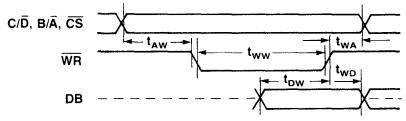
Note: ① For SDLC it must be programmed to 01111110 for flag recognition

Timing Waveforms

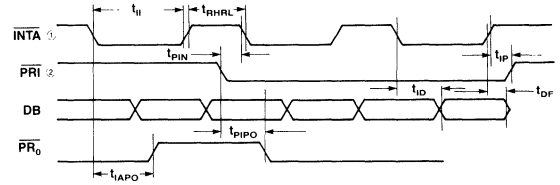
Read Cycle



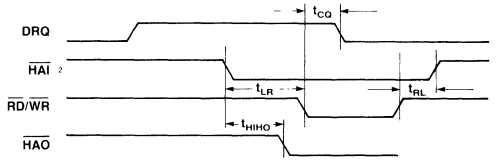
Write Cycle



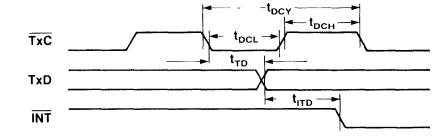
INTA Cycle



DMA Cycle

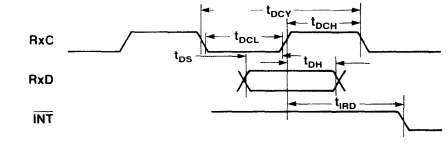


Transmit Data Cycle

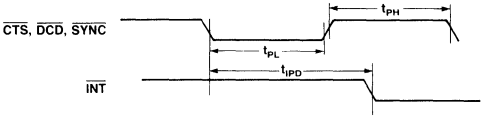


Notes: ① $\overline{\text{INTA}}$ signal acts as $\overline{\text{RD}}$ signal
② $\overline{\text{PRI}}$ and $\overline{\text{HAI}}$ signals act as $\overline{\text{CS}}$ signal

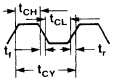
Receive Data Cycle



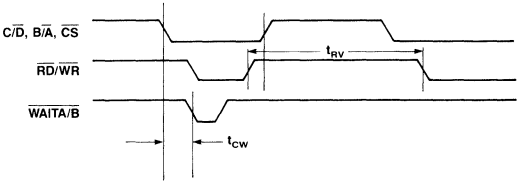
Other Timing



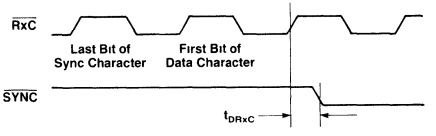
Clock



Read/Write Cycle (Software Block Transfer Mode)



Sync Pulse Generation (External Sync Mode)



6

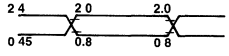
AC Characteristics

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Cycle	t_{CY}	200		4000	ns	
Clock High Width	t_{CH}	70		2000	ns	
Clock Low Width	t_{CL}	70		2000	ns	
Clock Rise Time	t_r	0		30	ns	
Clock Fall Time	t_f	0		30	ns	
Address Setup to RD	t_{AR}	0			ns	
Address Hold from RD	t_{RA}	0			ns	
RD Pulse Width	t_{RR}	200			ns	
Data Output Delay from Address	t_{AD}			140	ns	
Data Output Delay from RD	t_{RD}			140	ns	
Data Float Delay from RD	t_{DF}	0		70	ns	
Address Setup to WR	t_{AW}	0			ns	
Address Hold from WR	t_{WA}	0			ns	
WR Pulse Width	t_{WW}	200			ns	
Data Setup to WR	t_{DW}	130			ns	
Data Hold from WR	t_{WD}	0			ns	
PRO Delay from PRI	t_{PIPO}			100	ns	
PRO Delay from INTA	t_{IAPO}			200	ns	
PRI Setup to INTA	t_{PIN}	0			ns	
PRI Hold from INTA	t_{IP}	20			ns	
INTA Pulse Width	t_{II}	200			ns	
End of INTA to Next INTA	t_{IHRL}	300			ns	
Data Output Delay from INTA	t_{ID}			140	ns	
Data Float Delay from INTA	t_{DF}	0		70	ns	
Request Hold from RD/WR	t_{CQ}			60	ns	
HAI Setup to RD/WR	t_{LR}	300			ns	
HAI Hold from RD/WR	t_{RL}	0			ns	
HAO Delay from HAI	t_{HIHO}			100	ns	
Data Clock Cycle	t_{DCY}	400			ns	RxC, TxC
Data Clock High Width	t_{DCH}	180			ns	RxC, TxC
Data Clock Low Width	t_{DCL}	180			ns	RxC, TxC
Tx Data Delay from TxC	t_{TD}			300	ns	x1 Mode
				1000		x16, 32, 64
Rx Data Setup to RxC	t_{DS}	0			ns	
Rx Data Hold from RxC	t_{DH}	140			ns	
INT Delay Time from Tx Data	t_{ITD}			4–6	t_{CY}	
INT Delay Time from RxC	t_{IRD}			7–11	t_{CY}	
CTS, DCD, SYNC High Pulse Width	t_{PH}	200			ns	
CTS, DCD, SYNC Low Pulse Width	t_{PL}	200			ns	
External INT from CTS, DCD, SYNC	t_{IPD}			500	ns	
Recovery Time Between Controls	t_{RV}	300			ns	
WAIT Delay Time from Address	t_{CW}			80	ns	
SYNC Setup to RxC	t_{DRxC}			100	ns	

Notes: 1 $\overline{\text{RESET}}$ must be active for a minimum of one complete CLK cycle
2 In all modes system clock rate must be 4 5 times data rate

AC Waveform Measurement Points



μPD7201A Target Specifications

Absolute Maximum Ratings

T_a = 25°C	
Power Supply, V_{CC}	−0.5V to +7.0V
Input Voltages, V_I	−0.5V to +7.0V
Output Voltages, V_O	−0.5V to +7.0V
Operating Temperature, T_{OPT}	0°C to +70°C
Storage Temperature, T_{STG}	−65°C to +125°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Input High Voltage	V_{IH}	+2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			+0.45	V	I_{OL} = +2 0mA
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = 200μA
Input Leakage Current	I_{IL}			±10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{OL}			±10	μA	V_{OUT} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}			180	mA	

Capacitance

T_a = 25°C; V_{CC} = GND = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			10	pF	fc = 1MHz Unmeasured pins returned to GND.
Output Capacitance	C_{OUT}			15	pF	
I/O Capacitance	$C_{I/O}$			20	pF	

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7201AC
Ceramic, μPD7201AD

Notes

μPD7210
INTELLIGENT GPIB
INTERFACE CONTROLLER

DESCRIPTION

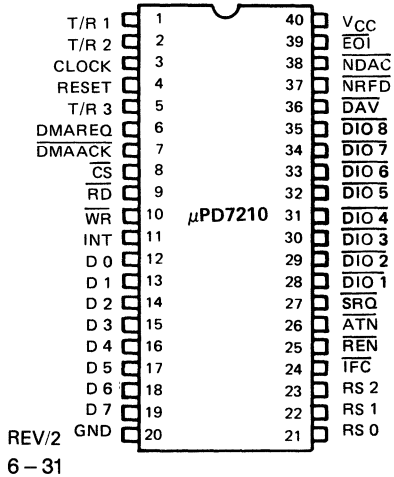
The μPD7210 TLC is an intelligent GPIB Interface Controller designed to meet all of the functional requirements for Talkers, Listeners, and Controllers as specified by the IEEE Standard 488-1978. Connected between a processor bus and the GPIB, the TLC provides high level management of the GPIB to unburden the processor and to simplify both hardware and software design. Fully compatible with most processor architectures, Bus Driver/Receivers are the only additional components required to implement any type of GPIB interface.

FEATURES

- All Functional Interface Capability Meeting IEEE Standard 488-1978
  - SH1 (Source Handshake)
  - AH1 (Acceptor Handshake)
  - T5 or TE5 (Talker or Extended Talker)
  - L3 or LE3 (Listener or Extended Listener)
  - SR1 (Service Request)
  - RL1 (Remote Local)
  - PP1 or PP2 ((Parallel Poll) (Remote or Local Configuration))
  - DC1 (Device Clear)
  - DT1 (Device Trigger)
  - C1-5 ((Controller) (All Functions))
- Programmable Data Transfer Rate
- 16 MPU Accessible Registers – 8 Read/8 Write
- 2 Address Registers
  - Detection of MTA, MLA, MSA (My Talk/Listen/Secondary Address)
  - 2 Device Addresses
- EOS Message Automatic Detection
- Command (IEEE Standard 488-78) Automatic Processing and Undefined Command Read Capability
- DMA Capability
- Programmable Bus Transceiver I/O Specification (Works with T.I./Motorola/Intel)
- 1 to 8 MHz Clock Range
- TTL Compatible
- N Channel MOS
- +5V Single Power Supply
- 40-Pin Plastic DIP
- 8080/85/86 Compatible

6

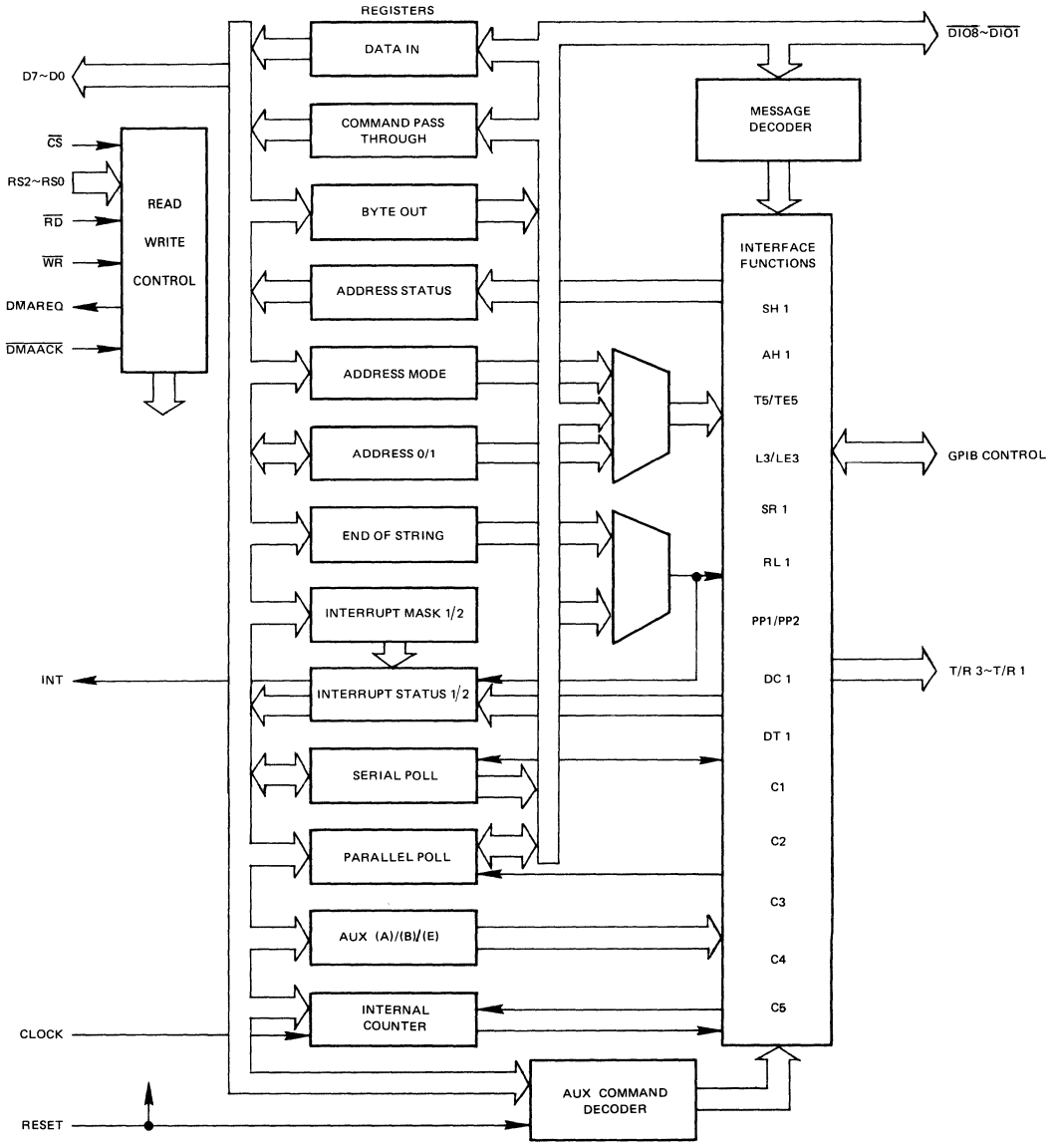
PIN CONFIGURATION



PIN IDENTIFICATION

PIN	NAME	I/O	DESCRIPTION
1	T/R1	O	Transmit/Receive Control – Input/Output Control Signal for the GPIB Bus Transceivers.
2	T/R2	O	Transmit/Receive Control – The functions of T/R2, T/R3 are determined by the values of TRM1, TRM0 of the address mode register.
3	CLK	I	Clock – (1-8 MHz) Reference Clock for generating the state change prohibit times T1, T6, T7, T9 specified in IEEE Standard 488-1978.
4	RST	I	Reset – Resets 7210 to an idle state when high (active high).
5	T/R3	O	Transmit/Receive Control – Function determined by TRM1 and TRM0 of address mode register (See T/R2).
6	DRQ	O	DMA Request – 7210 requests data transfer to the computer system, becomes low on input of DMA acknowledge signal $\overline{\text{DACK}}$.
7	$\overline{\text{DACK}}$	I	DMA Acknowledge – (Active Low) Signal connects the computer system data bus to the data register of the 7210.
8	$\overline{\text{CS}}$	I	Chip Select – (Active Low) Enables access to the register selected by RS0-2 (read or write operation).
9	$\overline{\text{RD}}$	I	Read – (Active Low) Places contents of read register specified by RS0-2 – on D0-7 (Computer Bus).
10	$\overline{\text{WR}}$	I	Write – (Active Low) writes data on D0-7 into the write register specified by RS0-2.
11	INT / $\overline{\text{INT}}$	O	Interrupt Request – (Active High/Low) Becomes active due to any 1 of 13 internal interrupt factors (unmasked) active state software configurable, active high on chip reset.
12-19	D0-7	I/O	Data Bus – 8-bit bidirectional data bus, for interface to computer system.
20	GND		Ground.
21-23	RS0-2	I	Register Select – These lines select one of eight read (write) registers during a read (write) operation.
24	$\overline{\text{IFC}}$	I/O	Interface Clear – Control line used for clearing the interface functions.
25	$\overline{\text{REN}}$	I/O	Remote Enable – Control line used to select remote or local control of the devices.
26	$\overline{\text{ATN}}$	I/O	Attention – Control line which indicates whether data on DIO lines is an interface message or device dependent message.
27	$\overline{\text{SRQ}}$	I/O	Service Request – Control line used to request the controller for service.
28-35	$\overline{\text{DIO1-8}}$	I/O	Data Input/Output – 8-bit bidirectional bus for transfer of message on the GPIB.
36	$\overline{\text{DAV}}$	I/O	Data Valid – Handshake line indicating that data on DIO lines is valid.
37	$\overline{\text{NRFD}}$	I/O	Ready for Data – Handshake line indicating that device is ready for data.
38	$\overline{\text{NDAC}}$	I/O	Data Accepted – Handshake line indicating completion of message reception.
39	$\overline{\text{EOI}}$	I/O	End or Identify – Control line used to indicate the end of multiple byte transfer sequence or to execute a parallel polling in conjunction with ATN.
40	V_{CC}		+5V DC – Technical Specifications: +5V; NMOS; 500 MW; 40 Pins; TTL Compatible; 1-8 MHz.

BLOCK DIAGRAM



INTRODUCTION

The IEEE Standard 488 describes a "Standard Digital Interface for Programmable Instrumentation" which, since its introduction in 1975, has become the most popular means of interconnecting instruments and controllers in laboratory, automatic test and even industrial applications. Refined over several years, the 488-1978 Standard, also known as the General Purpose Interface Bus (GPIB), is a highly sophisticated standard providing a high degree of flexibility to meet virtually most all instrumentation requirements. The μPD7210 TLC implements all of the functions that are required to interface to the GPIB. While it is beyond the scope of this document to provide a complete explanation of the IEEE 488 Standard, a basic description follows:

The GPIB interconnects up to 15 devices over a common set of data control lines. Three types of devices are defined by the standard: Talkers, Listeners, and Controllers, although some devices may combine functions such as Talker/Listener or Talker/Controller.

Data on the GPIB is transferred in a bit parallel, byte serial fashion over 8 Data I/O lines (D101 – D108). A 3 wire handshake is used to ensure synchronization of transmission and reception. In order to permit more than one device to receive data at the same time, these control lines are "Open Collector" so that the slowest device controls the data rate. A number of other control lines perform a variety of functions such as device addressing, interrupt generation, etc.

The μPD7210 TLC implements all functional aspects of Talker, Listener and Controller functions as defined by the 488-1978 Standard, and on a single chip.

GENERAL

The μPD7210 TLC is an intelligent controller designed to provide high level protocol management of the GPIB, freeing the host processor for other tasks. Control of the TLC is accomplished via 16 internal registers. Data may be transferred either under program control or via DMA using the TLC's DMA control facilities to further reduce processor overhead. The processor interface of the TLC is general in nature and may be readily interfaced to most processor lines.

In addition to providing all control and data lines necessary for a complete GPIB implementation, the TLC also provides a unique set of bus transceiver controls permitting the use of a variety of different transceiver configurations for maximum flexibility.

INTERNAL REGISTERS

The TLC has 16 registers, 8 of which are read and 8 write.

REGISTER NAME	ADDRESSING						SPECIFICATION							
	RS2	RS1	RS0	W/R	D/R	C/S								
Data In [0R]	0	0	0	1	0	0	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
Interrupt Status 1 [1R]	0	0	1	1	0	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Status 2 [2R]	0	1	0	1	0	0	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC
Serial Poll Status [3R]	0	1	1	1	0	0	S8	PEND	S6	S5	S4	S3	S2	S1
Address Status [4R]	1	0	0	1	0	0	CIC	ATN	SPMS	LPAS	TPAS	LA	TA	MJMN
Command Pass Through [5R]	1	0	1	1	0	0	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0
Address 0 [6R]	1	1	0	1	0	0	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
Address 1 [7R]	1	1	1	1	0	0	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
Byte Out [0W]	0	0	0	0	1	0	BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
Interrupt Mask 1 [1W]	0	0	1	0	1	0	CPT	APT	DET	END	DEC	ERR	DO	DI
Interrupt Mask 2 [2W]	0	1	0	0	1	0	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC
Serial Poll Mode [3W]	0	1	1	0	1	0	S8	rsv	S6	S5	S4	S3	S2	S1
Address Mode [4W]	1	0	0	0	1	0	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0
Auxiliary Mode [5W]	1	0	1	0	1	0	CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0
Address 0/1 [6W]	1	1	0	0	1	0	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1
End of String [7W]	1	1	1	0	1	0	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

DATA REGISTERS

The data registers are used for data and command transfers between the GPIB and the microcomputer system.

DATA IN (0R)

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

Holds data sent from the GPIB to the computer

BYTE OUT (0W)

BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0

Holds information written into it for transfer to the GPIB

INTERRUPT REGISTERS

The interrupt registers are composed of interrupt status bits, interrupt mask bits, and some other noninterrupt related bits.

READ

INTERRUPT STATUS 1 [1R]	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT STATUS 2 [2R]	INT	SRQI	LOK	REM	CO	LOKC	REMC	ADSC

WRITE

INTERRUPT MASK 1 [1W]	CPT	APT	DET	END	DEC	ERR	DO	DI
INTERRUPT MASK 2 [2W]	0	SRQI	DMAO	DMAI	CO	LOKC	REMC	ADSC

There are thirteen factors which can generate an interrupt from the μPD7210, each with their own status bit and mask bit.

The interrupt status bits are always set to one if the interrupt condition is met. The interrupt mask bits decide whether the INT bit and the interrupt pin will be active for that condition.

Interrupt Status Bits

INT	OR of All Unmasked Interrupt Status Bits
CPT	Command Pass Through
APT	Address Pass Through
DET	Device Trigger
END	End (END or EOS Message Received)
DEC	Device Clear
ERR	Error
DO	Data Out
DI	Data In
SRQI	Service Request Input
LOKC	Lockout Change
REMC	Remote Change
ADSC	Address Status Change
CO	Command Output

Noninterrupt Related Bits

LOK	Lockout
REM	Remote/Local
DMAO	Enable/Disable DMA Out
DMAI	Enable/Disable DMA In

SERIAL POLL REGISTERS

READ

SERIAL POLL STATUS [3R]	S8	PEND	S6	S5	S4	S3	S2	S1

WRITE

SERIAL POLL MODE [3W]	S8	rsv	S6	S5	S4	S3	S2	S1

The Serial Poll Mode register holds the STB (status byte: S8, S6-S1) sent over the GPIB and the local message rsv (request service). The Serial Poll Mode register may be read through the Serial Poll Status register. The PEND is set by rsv = 1, and cleared by NPRS • $\overline{rsv}$ = 1 (NPRS = Negative Poll Response State).

ADDRESS MODE/STATUS REGISTERS

ADDRESS STATUS [4R]	CIC	$\overline{ATN}$	SPMS	LPAS	TPAS	LA	TA	MJMN
ADDRESS MODE [4W]	ton	lon	TRM1	TRM0	0	0	ADM1	ADM0

The Address Mode register selects the address mode of the device and also sets the mode for T/R3 and T/R2 the transceiver control lines.

The functions of T/R2, T/R3 terminals (2 and 5) are determined as below by the TRM1, TRM0 values of the address mode register.

T/R2	T/R3	TRM1	TRM0
EOIOE	TRIG	0	0
CIC	TRIG	0	1
CIC	EOIOE	1	0
CIC	PE	1	1

EOIOE = TACS + SPAS + CIC · $\overline{CSBS}$

This denotes the input/output of $\overline{EOI}$ terminal.

When "1": Output
When "0": Input

CIC = $\overline{CIDS + CADS}$

This denotes if the controller inteface function is active or not.

When "1": $\overline{ATN}$ = output, $\overline{SRQ}$ = input
When "0": $\overline{ATN}$ = input, $\overline{SRQ}$ = output

PE = CIC + $\overline{PPAS}$

This indicates the type of bus driver connected to DI08 to DI01 and DAV lines.

When "1": 3 state type
When "0": Open collector type

TRIG: When DTAS state is initiated or when a trigger auxiliary command is issued, a high pulse is generated.

Upon RESET, TRM0 and TRM1 become "0" (TRM0 = TRM1 = 0) and local message port is provided, so that T/R2 and T/R3 both become "LOW."

ADDRESS MODES

ton	lon	ADM1	ADM0	ADDRESS MODE	CONTENTS OF ADDRESS (0) REGISTER	CONTENTS OF ADDRESS (1) REGISTER
1	0	0	0	Talk only mode	Address Identification Not Necessary (No controller on the GPIB)	
0	1	0	0	Listen only mode	Not Used	
0	0	0	1	Address mode 1 (A1)	Major talk address or Major listen address	Minor talk address or Minor listen address
0	0	1	0	Address mode 2 (A2)	Primary address (talk or listen)	Secondary address (talk or listen)
0	0	1	1	Address mode 3 (A3)	Primary address (major talk or major listen)	Primary address (minor talk or minor listen)
Combinations other than above indicated Prohibited.						

Notes: (A1)– Either MTA or MLA reception is indicated by coincidence of either address with the received address. Interface function T or L.

(A2)– Address register 0 = primary, Address register 1 = secondary, interface function TE or LE.

(A3)– CPU must read secondary address via Command Pass Through Register interface function (TE or LE).

ADDRESS STATUS BITS

$\overline{ATN}$	Data Transfer Cycle (device in CSBS)
LPAS	Listener Primary Addressed State
TPAS	Talker Primary Addressed State
CIC	Controller Active
LA	Listener Addressed
TA	Talker Addressed
MJMN	Sets minor T/L address Reset = Major T/L address
SPMS	Serial Poll Mode State

ADDRESS REGISTERS

ADDRESS 0 [6R]	X	DT0	DL0	AD5-0	AD4-0	AD3-0	AD2-0	AD1-0
ADDRESS 1 [7R]	EOI	DT1	DL1	AD5-1	AD4-1	AD3-1	AD2-1	AD1-1
ADDRESS 0/1 [6W]	ARS	DT	DL	AD5	AD4	AD3	AD2	AD1

The TLC is able to automatically detect two types of addresses which are held in address registers 0 and 1. The addressing modes are outlined below.

Address settings are made by writing into the address 0/1 register. The function of each bit is described below.

ADDRESS 0/1 REGISTER BIT SELECTIONS

ARS – Selects which address register 0 or 1
DT – Permits or Prohibits address to be detected as Talk
DL – Permits or Prohibits address to be detected as Listen
AD5 – AD1 – Device address value
EOI – Holds the value of EOI line when data is received

COMMAND PASS THROUGH REGISTER

COMMAND PASS THROUGH [5R]	CPT7	CPT6	CPT5	CPT4	CPT3	CPT2	CPT1	CPT0

The CPT register is used such that the CPU may read the DIO lines in the cases of undefined command, secondary address, or parallel poll response.

END OF STRING REGISTER

END OF STRING [7W]

EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

This register holds either a 7- or 8-bit EOS message byte used in the GPIB system to detect the end of a data block. Aux Mode Register A controls the specific use of this register.

AUXILIARY MODE REGISTER

AUXILIARY MODE [5W]

CNT2	CNT1	CNT0	COM4	COM3	COM2	COM1	COM0

This is a multipurpose register. A write to this register generates one of the following operations according to the values of the CNT bits.

CNT 2	1	0	COM 4	3	2	1	0	OPERATION
0	0	0	C_4	C_3	C_2	C_1	C_0	Issues an auxiliary command specified by C_4 to C_0.
0	0	1	0	F_3	F_2	F_1	F_0	The reference clock frequency is specified and T_1, T_6, T_7, T_9 are determined as a result.
0	1	1	U	S	P_3	P_2	P_1	Makes write operation to the parallel poll register.
1	0	0	A_4	A_3	A_2	A_1	A_0	Makes write operation to the aux. (A) register.
1	0	1	B_4	B_3	B_2	B_1	B_0	Makes write operation to the aux. (B) register.
1	1	0	0	0	0	E_1	E_0	Makes write operation to the aux. (E) register.

AUXILIARY COMMANDS 0 0 0 C_4 C_3 C_2 C_1 C_0

COM 43210			
00000	iepon	–	Immediate Execute pon – Generate local pon Message
00010	crst	–	Chip Reset – Same as External Reset
00011	rrfd	–	Release RFD
00100	trig	–	Trigger
00101	rtl	–	Return to Local Message Generation
00110	seoi	–	Send EOI Message
00111	nvld	–	Non Valid (OSA reception) – Release DAC Holdoff
01111	vld	–	Valid (MSA reception, CPT, DEC, DET) – Release DAC Holdoff
0X001	sppf	–	Set/Reset Parallel Poll Flag
10000	gts	–	Go To Standby
10001	tca	–	Take Control Asynchronously
10010	tcs	–	Take Control Synchronously
11010	tcse	–	Take Control Synchronously on End
10011	ltn	–	Listen
11011	ltnc	–	Listen with Continuous Mode
11100	lun	–	Local Unlisten
11101	epp	–	Execute Parallel Poll
1X110	sifc	–	Set/Reset IFC
1X111	sren	–	Set/Reset REN
10100	dsc	–	Disable System Control

INTERNAL COUNTER 0 0 1 0 F_3 F_2 F_1 F_0

The internal counter generates the state change prohibit times (T_1, T_6, T_7, T_9) specified in the IEEE std 488-1978 with reference to the clock frequency.

AUXILIARY A REGISTER 1 0 0 A_4 A_3 A_2 A_1 A_0

Of the 5 bits that may be specified as part of its access word, 2 bits control the GPIB data receiving modes of the 7210 and 3 bits control how the EOS message is used.

A_1	A_0	DATA RECEIVING MODE
0	0	Normal Handshake Mode
0	1	RFD Holdoff on all Data Modes
1	0	RFD Holdoff on End Mode
1	1	Continuous Mode

BIT NAME	FUNCTION		
A_2	0	Prohibit	Permits (prohibits) the setting of the END bit by reception of the EOS message.
	1	Permit	
A_3	0	Prohibit	Permits (prohibits) automatic transmission of END message simultaneously with the transmission of EOS message TACS.
	1	Permit	
A_4	0	7 bit EOS	Makes the 8 bits/7 bits of EOS register the valid EOS message.
	1	8 bit EOS	

AUXILIARY B REGISTER 1 0 1 B_4 B_3 B_2 B_1 B_0

The Auxiliary B Register is much like the A Register in that it controls the special operating features of the device.

BIT NAME	FUNCTION		
B_0	1	Permit	Permits (prohibits) the detection of undefined command. In other words, it permits (prohibits) the setting of the CPT bit on reception of an undefined command.
	0	Prohibit	
B_1	1	Permit	Permits (prohibits) the transmission of the END message when in serial poll active state (SPAS).
	0	Prohibit	
B_2	1	T_1 (high-speed)	T_1 (high speed) as T_1 of handshake after transmission of 2nd byte following data transmission.
	0	T_1 (low-speed)	
B_3	1	$\overline{INT}$	Specifies the active level of $\overline{INT}$ pin.
	0	INT	
B_4	1	ist = SRQS	SRQS indicates the value of ist level local message (the value of the parallel poll flag is ignored). SRQS = 1 . . . ist = 1. SRQS = 0 . . . ist = 0.
	0	ist = Parallel Poll Flag	The value of the parallel poll flag is taken as the ist local message.

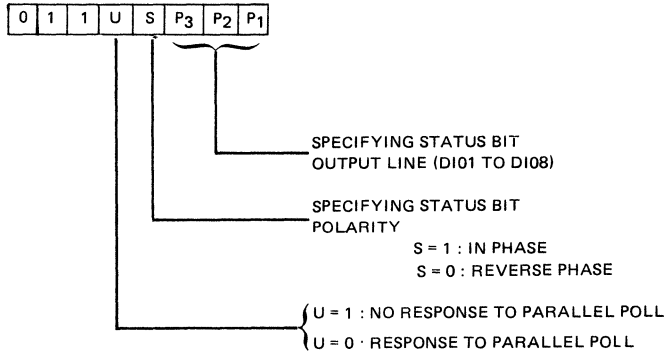
AUXILIARY E REGISTER 1 1 0 0 0 0 E_1 E_0

This register controls the Data Acceptance Modes of the TLC.

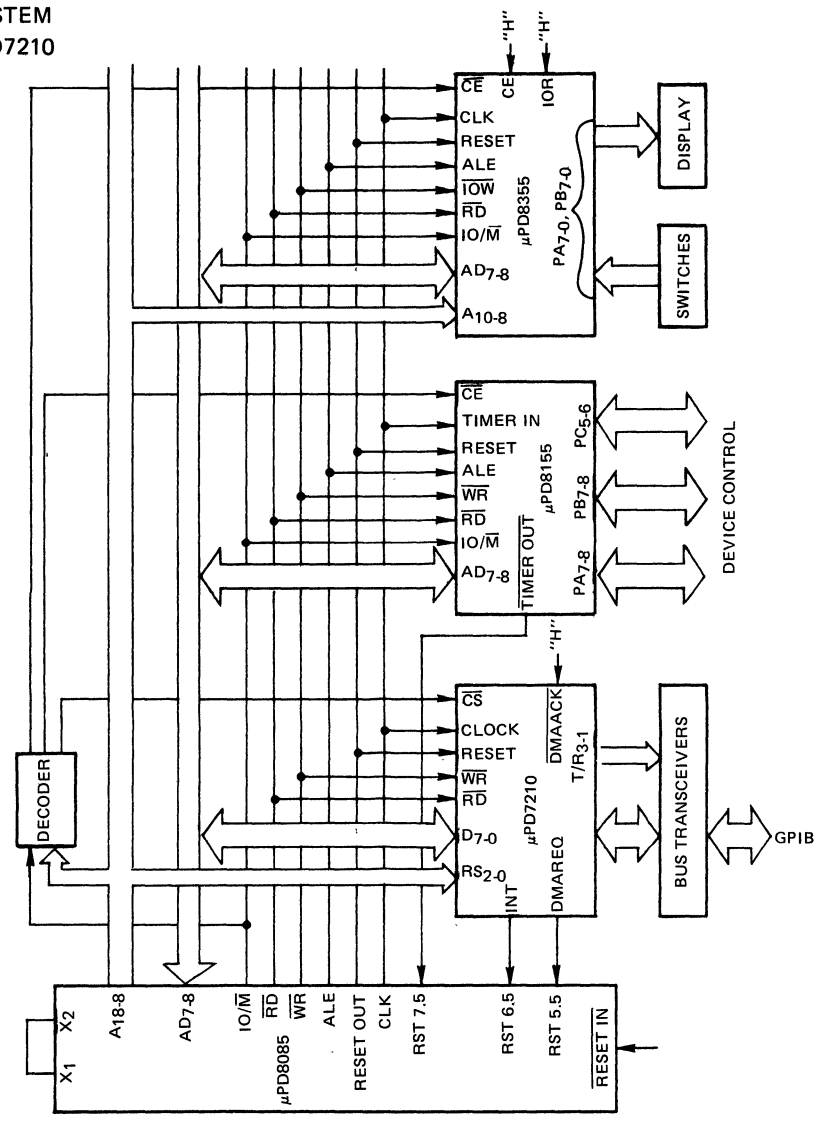
BIT	FUNCTION		
E_0	1	Enable	DAC Holdoff by initiation of DCAS
	0	Disable	
E_1	1	Enable	DAC Holdoff by initiation of DTAS
	0	Disable	

Parallel Poll Register 0 1 1 U S P_3 P_2 P_1

The Parallel Poll Register defines the parallel poll response of the μPD7210.



MINIMUM 8085 SYSTEM
WITH μPD7210



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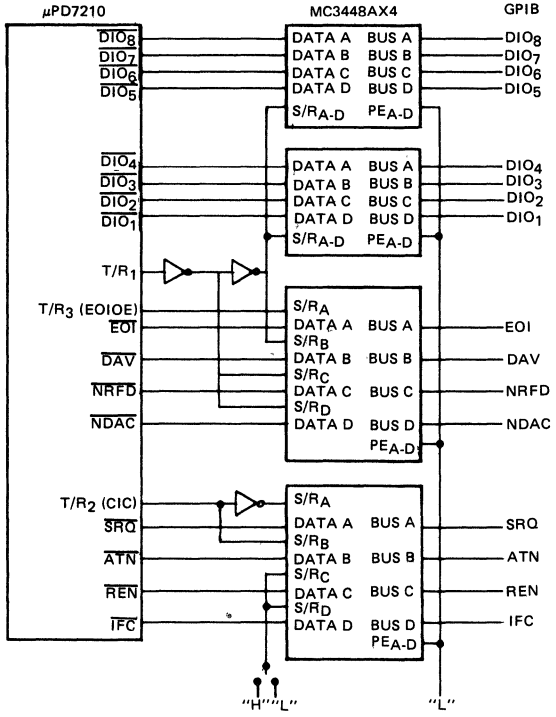
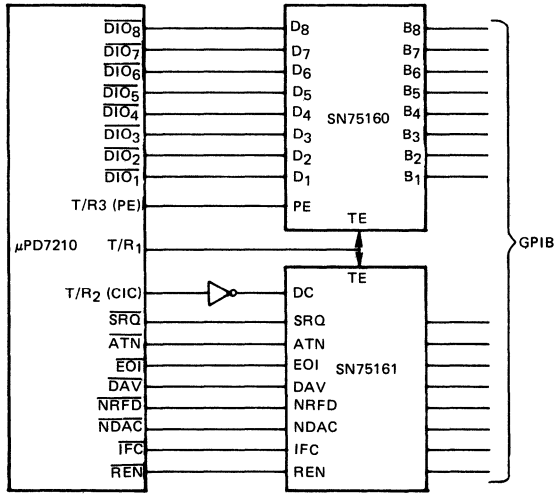
MINIMUM 8085 SYSTEM WITH μPD7210 (CONT.)



Note: In this example, high-speed data transfer cannot be made since the bus transceiver is of the open collector type (Set $B_2 = 0$).



Note: In the case of low-speed data transfer ($B_2 = 0$), the T/R_3 pin can be used as a TRIG output. The PE input of SN75160 should be cleared to "0."

ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

Parameter	Symbol	Test Conditions	Ratings	Unit
Supply Voltage	V_{CC}		-0.5 ~ + 7.0	V
Input Voltage	V_I		-0.5 ~ +7.0	V
Output Voltage	V_O		-0.5 ~ +7.0	V
Operating Temperature	T_{opt}		0 ~ +70	°C
Storage Temperature	T_{stg}		-65 ~ +125	°C

DC CHARACTERISTICS

(T_a = 0 ~ +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Input Low Voltage	V_{IL}		-0.5		+0.8	V
Input High Voltage	V_{IH}		+2.0		V_{CC} + 0.5	V
Low Level Output Voltage	V_{OL}	I_{OL} = 2 mA (4 mA : T/R1 Pin)			+0.45	V
High Level Output Voltage	V_{OH1}	I_{OH} = -400 μA (Except INT)	+2.4			V
High Level Output Voltage (INT Pin)	V_{OH2}	I_{OH} = -400 μA I_{OH} = -50 μA	+2.4 +3.5			V
Input Leakage Current	I_{IL}	V_{IN} = 0V ~ V_{CC}	-10		+10	μA
Output Leakage Current	I_{OL}	V_{OUT} = 0.45V ~ V_{CC}	-10		+10	μA
Supply Current	I_{CC}				+180	mA

CAPACITANCE

(T_a = 25°C, V_{CC} = GND = 0V)

Parameter	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max	
Input Capacitance	C_{IN}	f = 1 MHz			10	pF
Output Capacitance	C_{OUT}	All Pins Except Pin Under Test Tied to AC Ground			15	pF
I/O Capacitance	$C_{I/O}$				20	pF

6

AC CHARACTERISTICS

(T_a = 0 ~ 70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Conditions	Limits		Unit
			Min	Max	
$\overline{EOI}\downarrow \rightarrow \overline{DIO}$	t_{EODI}	PPSS → PPAS, ATN = True		250	ns
$\overline{EOI}\downarrow \rightarrow$ T/R1↑	t_{EOT11}	PPSS → PPAS, ATN = True		155	ns
$\overline{EOI}\uparrow \rightarrow$ T/R1↓	t_{EOT12}	PPAS → PPSS, ATN = False		200	ns
$\overline{ATN}\downarrow \rightarrow \overline{NDAC}\downarrow$	t_{ATND}	AIDS → ANRS, LIDS		155	ns
$\overline{ATN}\downarrow \rightarrow$ T/R1↓	t_{ATT1}	TACS + SPAS → TADS, CIDS		155	ns
$\overline{ATN}\downarrow \rightarrow$ T/R2↓	t_{ATT2}	TACS + SPAS → TADS, CIDS		200	ns
$\overline{DAV}\downarrow \rightarrow$ DMAREQ	t_{DVRQ}	ACRS → ACDS, LACS		600	ns
$\overline{DAV}\downarrow \rightarrow \overline{NRFD}\downarrow$	t_{DVNR1}	ACRS → ACDS		350	ns
$\overline{DAV}\downarrow \rightarrow \overline{NDAC}\uparrow$	t_{DVND1}	ACRS → ACDS → AWNS		650	ns
$\overline{DAV}\uparrow \rightarrow \overline{NDAC}\downarrow$	t_{DVND2}	AWNS → ANRS		350	ns
$\overline{DAV}\uparrow \rightarrow \overline{NRFD}\uparrow$	t_{DVNR2}	AWNS → ANRS → ACRS		350	ns
$\overline{RD}\downarrow \rightarrow \overline{NRFD}\uparrow$	t_{RNR}	ANRS → ACRS LACS, DI reg. selected		500	ns
$\overline{NDAC}\uparrow \rightarrow$ DMAREQ↑	t_{NDRQ}	STRS → SWNS → SGNS, TACS		400	ns
$\overline{NDAC}\uparrow \rightarrow \overline{DAV}\uparrow$	t_{NDDV}	STRS → SWNS → SGNS		350	ns
$\overline{WR}\uparrow \rightarrow \overline{DIO}$	t_{WDI}	SGNS → SDYS, BO reg. selected		250	ns
$\overline{NRFD}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{NRDV}	SDYS → STRS, T_1 = True		350	ns
$\overline{WR}\uparrow \rightarrow \overline{DAV}\downarrow$	t_{WDV}	SGNS → SDYS → STRS BO reg. selected, RFD = True N_F = fc = 8 MHz, T_1 (High Speed)		830 +t_{SYNC}	ns
TRIG Pulse Width	t_{TRIG}		50		ns

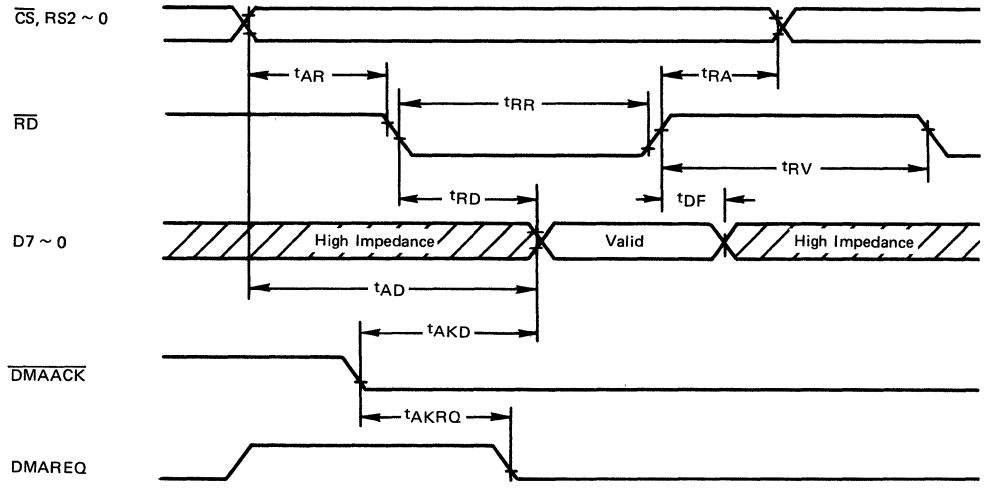
AC CHARACTERISTICS (CONT.)

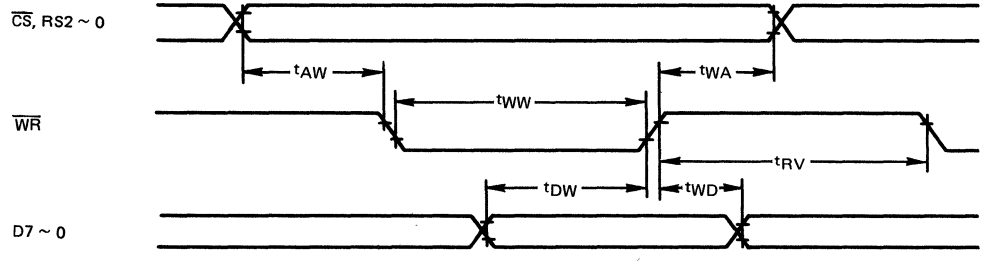
(T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Limits Min	Limits Max	Unit
Address Setup to $\overline{RD}$	t_{AR}	RS0 ~ RS2	85		ns
		$\overline{CS}$	0		ns
Address Hold from $\overline{RD}$	t_{RA}		0		ns
$\overline{RD}$ Pulse Width	t_{RR}		170		ns
Data Delay from Address	t_{AD}			250	ns
Data Delay from $\overline{RD}$↓	t_{RD}			150	ns
Output Float Delay from $\overline{RD}$↑	t_{DF}		0	80	ns
$\overline{RD}$ Recovery Time	t_{RV}		250		ns
Address Setup to $\overline{WR}$	t_{AW}		0		ns
Address Hold from $\overline{WR}$	t_{WA}		0		ns
$\overline{WR}$ Pulse Width	t_{WW}		170		ns
Data Setup to $\overline{WR}$	t_{DW}		150		ns
Data Hold from $\overline{WR}$	t_{WD}		0		ns
$\overline{WR}$ Recovery Time	t_{RV}		250		ns
DMAREQ↓ Delay from $\overline{DMAACK}$	t_{AKRQ}			130	ns
Data Delay from $\overline{DMAACK}$	t_{AKD}			200	ns

6

TIMING WAVEFORMS





Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7210C
Ceramic, μPD7210D

Description

The μPD7220 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the GDC is ideal for advanced computer graphics applications.

For a more detailed description of the GDC's operation, please refer to the GDC Design Manual.

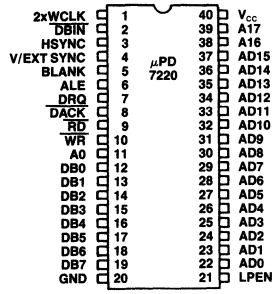
System Considerations

The GDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the GDC's design, each of the system components is used to the maximum extent through six-level hierarchy of simultaneous tasks. At the lowest level, the GDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the GDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the GDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the GDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

Features

- ☐ Microprocessor Interface
  - DMA transfers with 8257- or 8237-type controllers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles in under 800ns
  - Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light Pen Input
- ☐ External video synchronization mode
- ☐ Graphics Mode
  - Four megabit, bit-mapped display memory
- ☐ Character Mode
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Character Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities
  - Figure drawing of lines, arc/circles, rectangles, and graphics characters in 800ns per pixel
  - Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - Two independently scrollable areas
- ☐ Character Capabilities
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
  - Single +5 volt, NMOS, 40-pin DIP
- ☐ DMA Capability
  - Bytes or word transfers
  - 4 clock periods per byte transferred

Pin Configuration



Pin Identification

Pin No.	Symbol	Direction	Function
1	2xWCLK	IN	Clock Input
2	$\overline{DBIN}$	OUT	Display Memory Read Input Flag
3	HSYNC	OUT	Horizontal Video Sync Output
4	V/EXT SYNC	IN/OUT	Vertical Video Sync Output or External VSYNC Input
5	BLANK	OUT	CRT Blanking Output
6	ALE ($\overline{RAS}$)	OUT	Address Latch Enable Output
7	DRQ	OUT	DMA Request Output
8	$\overline{DACK}$	IN	DMA Acknowledge Input
9	$\overline{RD}$	IN	Read Strobe Input for Microprocessor Interface
10	WR	IN	Write Strobe Input for Microprocessor Interface
11	A0	IN	Address Select Input for Microprocessor Interface
12-19	DB0 to 7	IN/OUT	Bidirectional Data Bus to Host Microprocessor
20	GND	—	Ground
21	LPEN	IN	Light Pen Detect Input
22-34	AD0 to 12	IN/OUT	Address and Data Lines to Display Memory
35-37	AD13 to 15	IN/OUT	Utilization Varies with Mode of Operation
38	A16	OUT	Utilization Varies with Mode of Operation
39	A17	OUT	Utilization Varies with Mode of Operation
40	V_{CC}	—	+ 5V ± 10%

Character Mode Pin Utilization

Pin No.	Name	Direction	Function
35-37	AD13 to 15	OUT	Line Counter Bits 0 to 2 Outputs
38	A16	OUT	Line Counter Bit 3 Output
39	A17	OUT	Cursor Output and Line Counter Bit 4*

Mixed Mode Pin Utilization

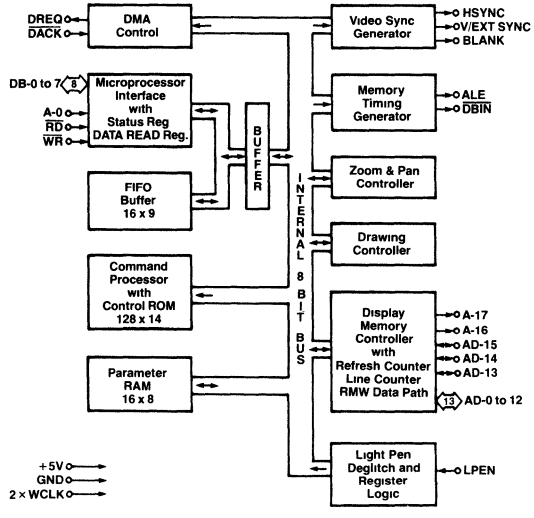
Pin No.	Name	Direction	Function
35-37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Attribute Blink and Clear Line Counter* Output
39	A17	OUT	Cursor and Bit-Map Area* Flag Output

*Output 10 clock cycles after trailing edge of HSYNC. See figure for timing example.

Graphics Mode Pin Utilization

Pin No.	Name	Direction	Function
35-37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Address Bit 16 Output
39	A17	OUT	Address Bit 17 Output

Block Diagram



GDC Components

Microprocessor Bus Interface

Control of the GDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal GDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destinations within the GDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control

The DMA control circuitry in the GDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a μPD8257 or μPD8237 DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM

The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator

Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple GDCs.

Memory Timing Generator

The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the GDC's ALE and DBIN outputs.

Zoom & Pan Controller

Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independently of the other display areas.

Drawing Controller

The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing controller needs no further assistance to complete the figure drawing.

Display Memory Controller

The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher

Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address.

Programmer's View of GDC

The GDC occupies two addresses on the system microprocessor bus through which the GDC's status register and FIFO are accessed. Commands and parameters are written into the GDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	Status Register	Parameter Into FIFO
1	FIFO Read	Command Into FIFO

GDC Microprocessor Bus Interface Registers

Commands to the GDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacks the parameters, loads them into the appropriate registers within the GDC, and initiates the required operations.

The commands available in the GDC can be organized into five categories as described in the following section.

GDC Command Summary

Video Control Commands

1. RESET — Resets the GDC to its idle state.
2. SYNC — Specifies the video display format.
3. VSYNC — Selects master or slave video synchronization mode.
4. CCHAR — Specifies the cursor and character row heights.

Display Control Commands

1. START — Ends Idle mode and unblanks the display.
2. BCTRL — Controls the blanking and unblanking of the display.
3. ZOOM — Specifies zoom factors for the display and graphics characters writing.
4. CURS — Sets the position of the cursor in display memory.
5. PRAM — Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
6. PITCH — Specifies the width of the X dimension of display memory.

Drawing Control Commands

1. WDAT — Writes data words or bytes into display memory.
2. MASK — Sets the mask register contents.
3. FIGS — Specifies the parameters for the drawing controller.
4. FIGD — Draws the figure as specified above.
5. GCHRD — Draws the graphics character into display memory.

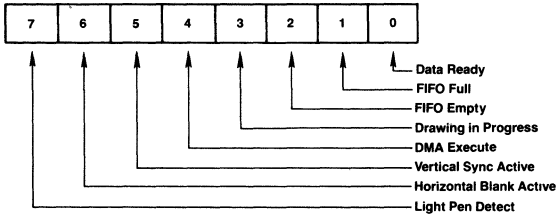
Data Read Commands

1. RDAT: — Reads data words or bytes from display memory.
2. CURD: — Reads the cursor position.
3. LPRD: — Reads the light pen address.

DMA Control Commands

1. DMAR — Requests a DMA read transfer.
2. DMAW — Requests a DMA write transfer.

Status Register Flags



Status Register (SR)

SR-7: Light Pen Detect

When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blanking Active

A 1 value for this flag signifies that horizontal retrace blanking is currently underway.

SR-5: Vertical Sync

Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute

This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress

While the GDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty

This bit and the FIFO Full flag coordinate system microprocessor accesses with the GDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the GDC have been interpreted.

SR-1: FIFO Full

A 1 at this flag indicates a full FIFO in the GDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the GDC.

SR-0: Data Ready

When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation & Command Protocol

The first-in, first-out buffer (FIFO) in the GDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the GDC's command set. The host microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the GDC requires differentiation of the first byte of a command sequence from the succeeding bytes. The first byte contains the operation code and the remaining bytes carry parameters. Writing into the GDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the GDC tests this bit as it interprets the

entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the GDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the GDC always put the FIFO into write mode if it wasn't in it already. If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a GDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the GDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the GDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the GDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT parameters or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

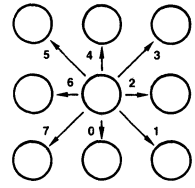
The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the Pattern Register data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The GDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 5MHz, this is equal to 800ns. During the RMW cycle the GDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the GDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the GDC's internal RMW logic.

During the drawing process, the GDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The GDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.



Drawing Directions

Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left.

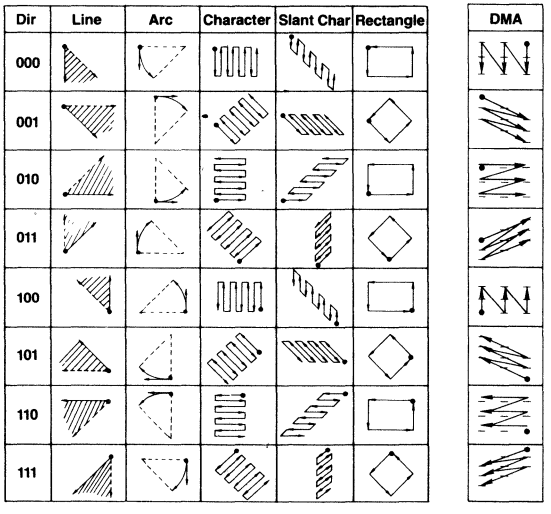
The table below summarizes these operations for each direction.

Dir	Operations to Address the Next Pixel
000	EAD + P → EAD
001	EAD + P → EAD dAD (MSB) = 1:EAD + 1 → EAD dAD → LR
010	dAD (MSB) = 1:EAD + 1 → EAD dAD → LR
011	EAD − P → EAD dAD (MSB) = 1:EAD + 1 → EAD dAD → LR
100	EAD − P → EAD
101	EAD − P → EAD dAD (LSB) = 1:EAD − 1 → EAD dAD → RR
110	dAD (LSB) = 1:EAD − 1 → EAD dAD → RR
111	EAD + P → EAD dAD (LSB) = 1:EAD − 1 → EAD dAD → RR

Where P = Pitch, LR = Left Rotate, RR = Right Rotate,
EAD = Execute Word Address, and
dAD = Dot Address stored in the Mask Register

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45 degrees in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the GDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45 degree diagonal path by pixels.

Drawing Parameters

In preparation for graphics figure drawing, the GDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the GDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The GDC Drawing Controller coordinates the RMW circuitry and address registers to draw the specifed figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the GDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

Drawing Type	DC	D	D2	D1	DM
Initial Value*	0	8	8	−1	−1
Line	|Δl|	2|ΔD| − |Δl|	2(|ΔD| − |Δl|)	2|ΔD|	−
Arc**	rsin ϕ	r−1	2(r−1)	−1	rsin θ ↓
Rectangle	3	A−1	B−1	−1	A−1
Area Fill	B−1	A	A	−	−
Graphic Character***	B−1	A	A	−	−
Write Data	W−1	−	−	−	−
DMAW	D−1	C−1	−	−	−
DMAR	D−1	C−2	(C−2)/2†	−	−
Read Data	W	−	−	−	−

*Initial values for the various parameters remain as each drawing process ends

**Circles are drawn with 8 arcs, each of which span 45°, so that sin $\phi = 1/\sqrt{2}$ and sin $\theta = 0$

***Graphic characters are a special case of bit-map area filling in which B and A ≤ 8 If A = 8 there is no need to load D and D2

Where
−1 = all ONES value

All numbers are shown in base 10 for convenience The GDC accepts base 2 numbers (2s complement notation where appropriate)

− = No parameter bytes sent to GDC for this parameter
Δl = The larger at Δx or Δy
ΔD = The smaller at Δx or Δy
r = Radius of curvature, in pixels
ϕ = Angle from major axis to end of the arc $\phi \leq 45°$
θ = Angle from major axis to start of the arc $\theta \leq 45°$
↑ = Round up to the next higher integer
↓ = Round down to the next lower integer
A = Number of pixels in the initially specified direction
B = Number of pixels in the direction at right angles to the initially specified direction
W = Number of words to be accessed
C = Number of bytes to be transferred in the initially specified direction (Two bytes per word if word transfer mode is selected)
D = Number of words to be accessed in the direction at right angles to the initially specified direction
DC = Drawing count parameter which is one less than the number of RMW cycles to be executed
DM = Dots masked from drawing during arc drawing
† = Needed only for word reads

Graphics Character Drawing

Graphics characters can be drawn into display memory pixel-by-pixel. The up to 8-by-8 character display is loaded into the GDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command. Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The GDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is less than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the GDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mozaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8.)

Parameter RAM Contents: RAM Address RA 0 to 15

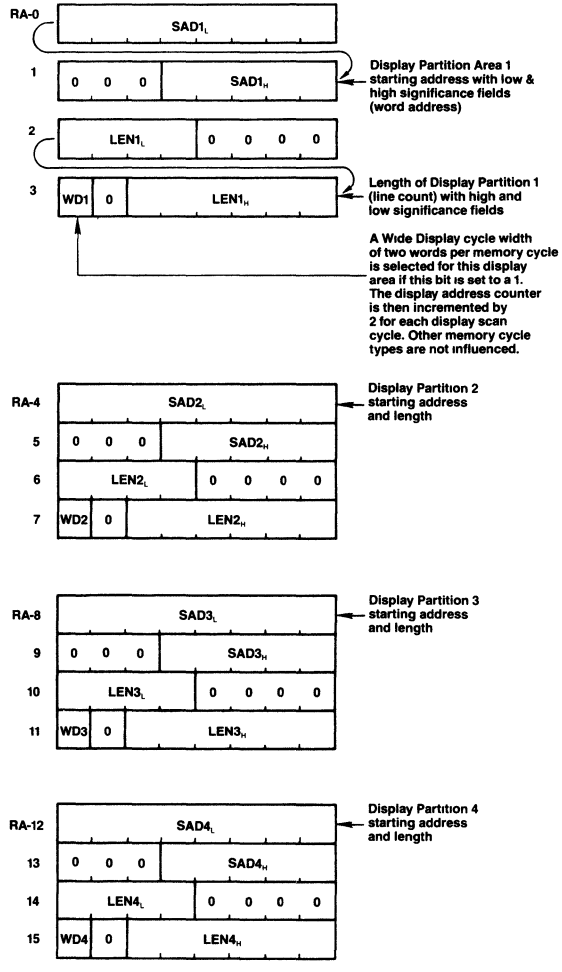
The parameters stored in the parameter RAM, PRAM, are available for the GDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the GDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

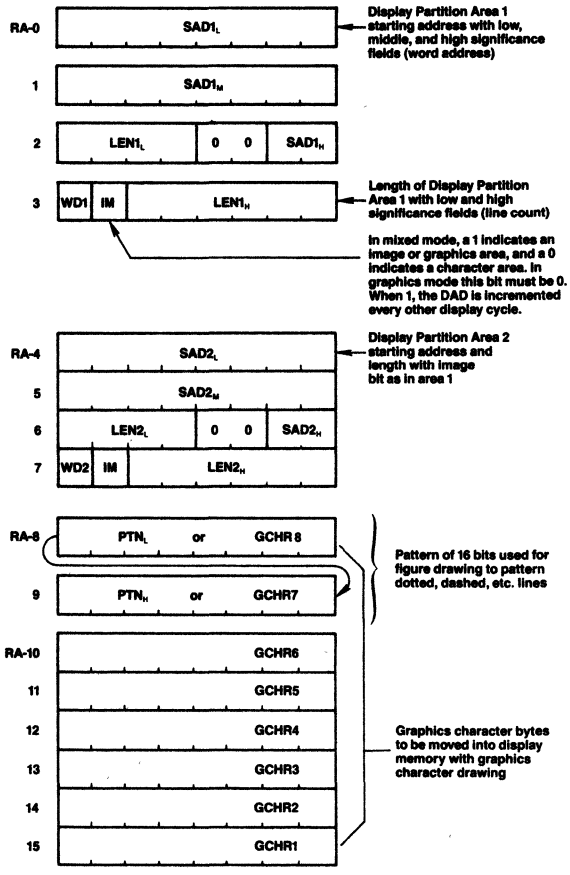
The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern Register to allow the GDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing locations 8 through 15 are referenced for the pattern or character to be drawn.

Details of the bit assignments are shown for the various modes of operation.

Character Mode



Graphics and Mixed Graphics and Character Modes

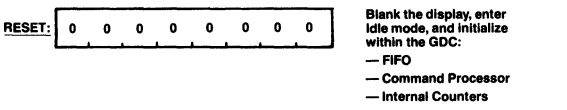


Command Bytes Summary

RESET	0	0	0	0	0	0	0	0
SYNC	0	0	0	0	1	1	1	DE
VSYNC	0	1	1	0	1	1	1	M
CCHAR	0	1	0	0	1	0	1	1
START	0	1	1	0	1	0	1	1
BCTRL	0	0	0	0	1	1	0	DE
ZOOM	0	1	0	0	0	1	1	0
CURS	0	1	0	0	1	0	0	1
PRAM	0	1	1	1	SA			
PITCH	0	1	0	0	0	1	1	1
WDAT	0	0	1	TYPE		0	MOD	
MASK	0	1	0	0	1	0	1	0
FIGS	0	1	0	0	1	1	0	0
FIGD	0	1	1	0	1	1	0	0
GCHRD	0	1	1	0	1	0	0	0
RDAT	1	0	1	TYPE		0	MOD	
CURD	1	1	1	0	0	0	0	0
LPRD	1	1	0	0	0	0	0	0
DMAR	1	0	1	TYPE		1	MOD	
DMAW	0	0	1	TYPE		1	MOD	

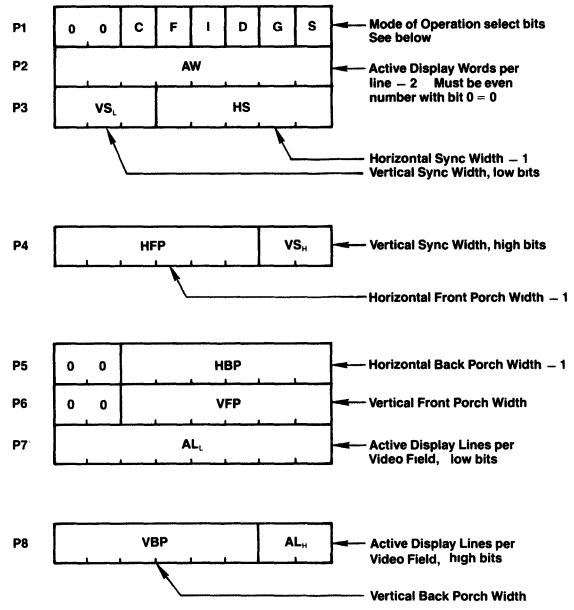
Video Control Commands

Reset



This command can be executed at any time and does not modify any of the parameters already loaded into the GDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below. Idle mode is exited with the START command.



In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any. The number of active words per line must be an even number from 2 to 256. An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field for vertical parameters. All horizontal widths are counted in display words. All vertical intervals are counted in lines.

Horizontal Back Porch Constraints

1. In general:
   HBP ≥ 3 Display Word Cycles (6 clock cycles).
2. If the IMAGE or WD modes change within one video field:
   HBP ≥ 5 Display Word Cycles (10 clock cycles).
3. If interlace or mixed mode is used:
   HBP ≥ 5 Display Word Cycles (10 clock cycles).

Horizontal Front Porch Constraints

1. If the display ZOOM function is used at other than 1X:
   HFP ≥ 2 Display Word Cycles (4 clock cycles).
2. If the GDC is used in the video sync Slave mode:
   HFP ≥ 4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP ≥ 6 Display Word Cycles (12 clock cycles).
4. If interlace mode is used:
   HFP ≥ 3 Display Word Cycles (6 clock cycles).

Horizontal SYNC Constraints

1. If Interlaced display mode is used:
   HS ≥ 5 Display Word Cycles (10 clock cycles).

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed Graphics & Character
0	1	Graphics Mode
1	0	Character Mode
1	1	Invalid

I	S	Video Framing
0	0	Noninterlaced
0	1	Invalid
1	0	Interlaced Repeat Field for Character Displays
1	1	Interlaced

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.

Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.

Noninterlaced Framing: 1 field brings all of the information to the screen.

Total scanned lines in interlace mode is odd. The sum of VFP + VS + VBP + AL should equal one less than the desired odd number of lines.

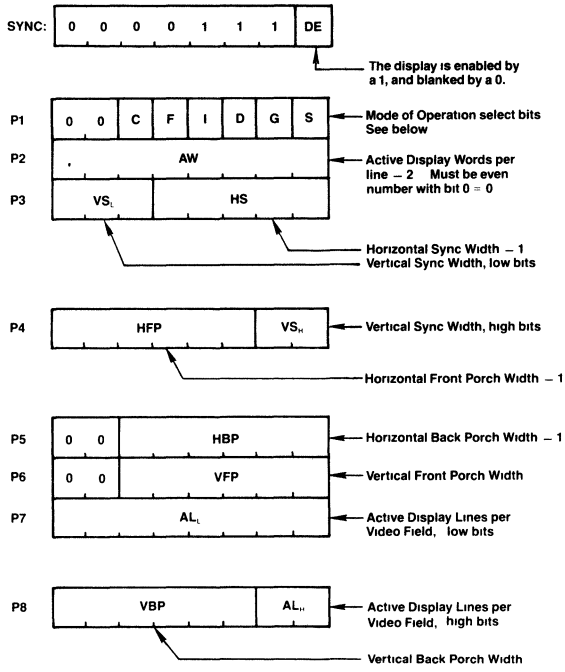
D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — STATIC RAM
1	Refresh — Dynamic RAM

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

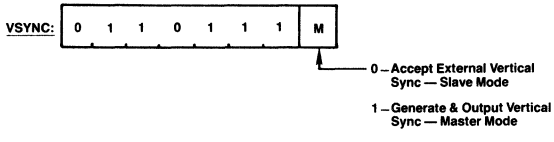
Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.

SYNC Format Specify



This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The GDC is not reset nor does it enter idle mode.

Vertical Sync Mode

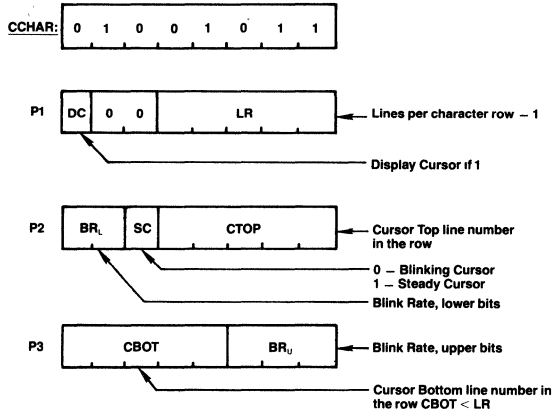


When using two or more GDCs to contribute to one image, one GDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all GDCs are connected together.

A few considerations should be observed when synchronizing two or more GDCs to generate overlayed video via the VSYNC INPUT/OUTPUT pin. As mentioned above, the Horizontal Front Porch (HFP) must be 4 or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave GDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave GDC to complete the operation before the start of the HSYNC interval.

Once the GDCs are initialized and set up as Master and Slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the Master GDC and wait until after one or more VSYNC pulses have been generated before the display process is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated for the Slaves to synchronize to.

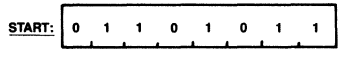
Cursor & Character Characteristics



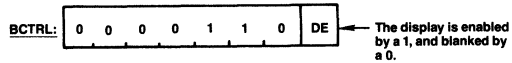
In graphics mode, LR should be set to 0. The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on-¼ off duty cycle. All three parameter bytes must be output for interlace displays, regardless of mode. For interlace displays in graphics mode, the parameter $BR_L = 3$.

Display Control Commands

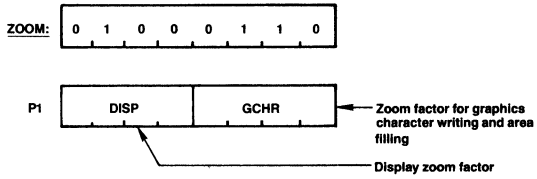
Start Display & End Idle Mode



Display Blanking Control

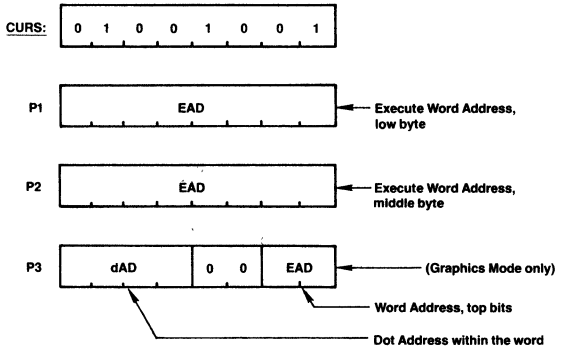


Zoom Factors Specify



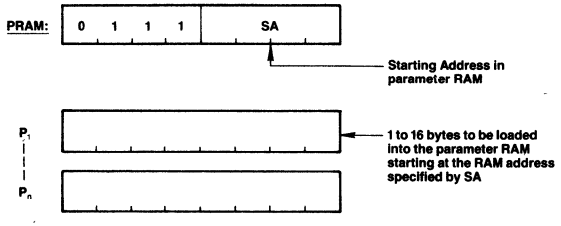
Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

Cursor Position Specify



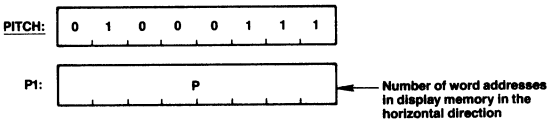
In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address. In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

Parameter RAM Load



From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

Pitch Specification

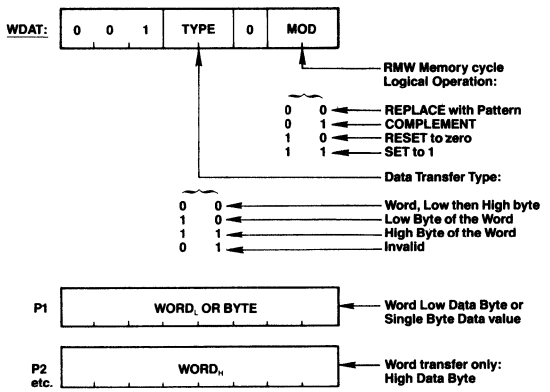


This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active words per line" parameter, which specifies the width of the raster-scan display, also sets the Pitch of the display memory. Note that the AW value is two less than the display window width. The PITCH command must be used to set the proper memory width larger than the window width.

Drawing Control Commands

Write Data into Display Memory



Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

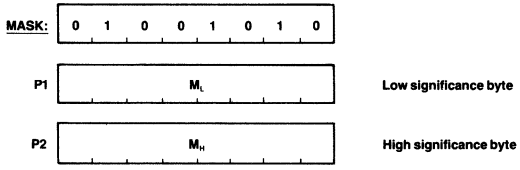
For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires

parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceded by a FIGS command and its parameters. Only the first three parameters need be given following the FIGS opcode, to set up the type of drawing, the DIR direction, and the DC value. The DC parameter +1 will be the number of RMW cycles done by the GDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed per set of parameters.

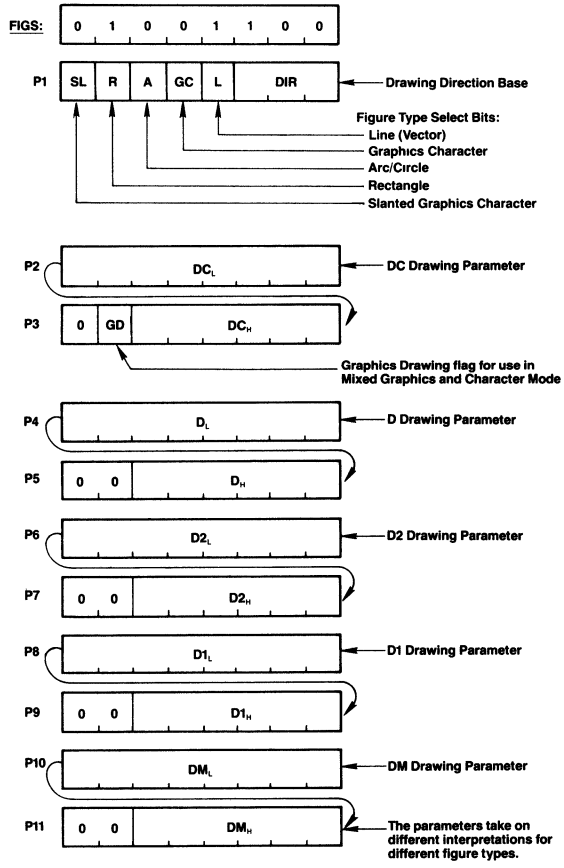
Mask Register Load



This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

The Mask register is loaded both by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16 bits can be individually one or zero, under program control. The CURS command on the other hand, puts a "1 of 16" pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing operations using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output. The Mask register should be set to all "ONES" for any "word-at-a-time" operation.

Figure Drawing Parameters Specify

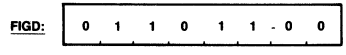


Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing, Individual Dot Drawing, DMA, WDAT, and RDAT
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area filling with graphics character pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted Graphics Character Drawing and Slanted Area Filling

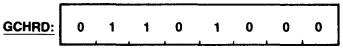
Only these bit combinations assure correct drawing operation.

Figure Draw Start



On execution of this instruction, the GDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

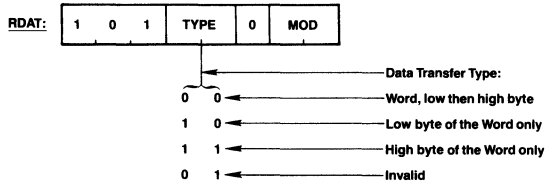
Graphics Character Draw and Area Filling Start



Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

Data Read Commands

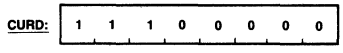
Read Data from Display Memory



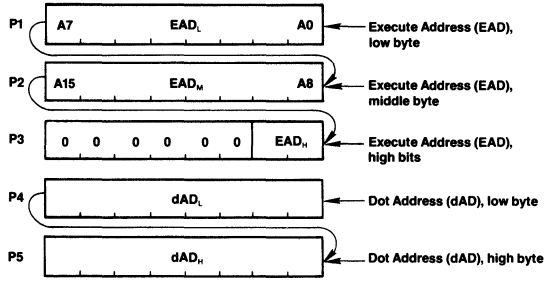
Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the GDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.

Cursor Address Read



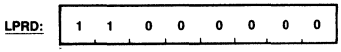
The following bytes are returned by the GDC through the FIFO:



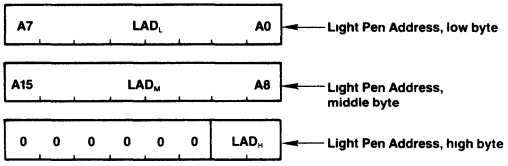
The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.

The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read



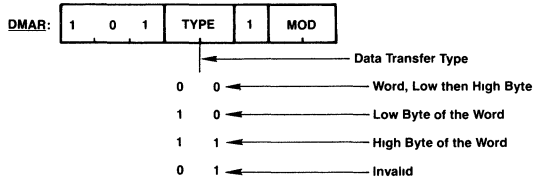
The following bytes are returned by the GDC through the FIFO:



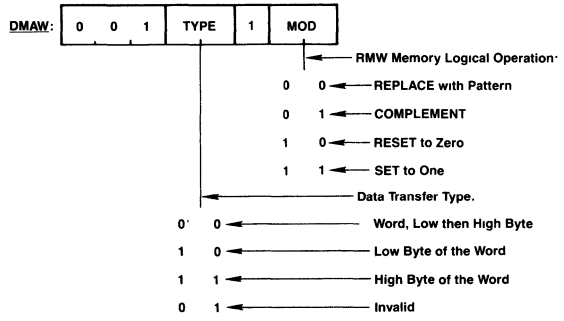
The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Read Request



DMA Write Request



6

AC Characteristics, μPD7220D

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Read Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Address Setup to RD ↓	t_{AR}	0		0		0		ns	
Address Hold from RD ↑	t_{RA}	0		0		0		ns	
RD Pulse Width	t_{RR1}	t_{RD1} + 20	t_{RCY} − ½ t_{CLK}	t_{RD1} + 20	t_{RCY} − ½ t_{CLK}	t_{RD1} + 20	t_{RCY} − ½ t_{CLK}	ns	
Data Delay from RD ↓	t_{RD1}		120		80		70	ns	C_L = 50 pF
Data Floating from RD ↑	t_{DF}	0	120	0	100	0	90	ns	
RD Pulse Cycle	t_{RCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	

Write Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Address Setup to WR ↓	t_{AW}	0		0		0		ns	
Address Hold from WR ↑	t_{WA}	0		0		10		ns	
WR Pulse Width	t_{WW}	120		100		90		ns	
Data Setup to WR ↑	t_{DW}	100		80		70		ns	
Data Hold from WR ↑	t_{WD}	10		10		10		ns	
WR Pulse Cycle	t_{WCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	

DMA Read Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
DACK Setup to RD ↓	t_{KR}	0		0		0		ns	
DACK Hold from RD ↑	t_{RK}	0		0		0		ns	
RD Pulse Width	t_{RR2}	t_{RD2} + 20		t_{RD2} + 20		t_{RD2} + 20		ns	
Data Delay from RD ↓	t_{RD2}		1.5 t_{CLK} + 120		1.5 t_{CLK} + 80		1.5 t_{CLK} + 70	ns	C_L = 50 pF
DREQ Delay from 2XWCLK ↑	t_{REQ}		150		120		110	ns	C_L = 50 pF
DREQ Setup to DACK ↓	t_{QK}	0		0		0		ns	
DACK High Level Width	t_{DK}	t_{CLK}		t_{CLK}		t_{CLK}		ns	
DACK Pulse Cycle	t_E	4 t_{CLK}*		4 t_{CLK}*		4 t_{CLK}*		ns	
DREQ ↓ Delay from DACK ↓	$t_{KQ(R)}$		t_{CLK} + 150		t_{CLK} + 120		t_{CLK} + 110	ns	C_L = 50 pF

* for high byte and low byte transfers: t_E = 5 t_{CLK}

DMA Write Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
DACK Setup to WR ↓	t_{KW}	0		0		0		ns	
DACK Hold from WR ↑	t_{WK}	0		0		0		ns	
DREQ ↓ Delay from DACK ↓	$t_{KQ(W)}$		t_{CLK} + 150		t_{CLK} + 120		t_{CLK} + 100	ns	C_L = 50 pF
WR Pulse Width	t_{WW}	120	3 t_{CLK}	100	3 t_{CLK}	90	3 t_{CLK}	ns	

R/M/W Cycle (GDC ↔ Display Memory)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Address/ Data Delay from 2XWCLK ↑	t_{AD}	30	160	30	130	30	115	ns	C_L = 50 pF
Address/Data Floating from 2XWCLK ↑	t_{OFF}	30	160	30	130	30	115	ns	C_L = 50 pF
Input Data Setup to 2XWCLK ↓	t_{DIS}	0		0		0		ns	
Input Data Hold from 2XWCLK ↓	t_{DIH}	t_{DE} − 20		t_{DE} − 20		t_{DE} − 20		ns	
DBIN Delay from 2XWCLK ↓	t_{DE}	30	120	30	90	30	80	ns	C_L = 50 pF
ALE ↑ Delay from 2XWCLK ↑	t_{RR}	30	125	30	100	30	90	ns	C_L = 50 pF

ALE ↓ Delay from 2XWCLK ↓	t_{RF}	30	100	30	80	30	70	ns	C_L = 50 pF
ALE Width	t_{RW}	⅓ t_{CLK}		⅓ t_{CLK}		⅓ t_{CLK}		ns	C_L = 50 pF
ALE Low Width	t_{RL}	t_{CLK} + 30		t_{CLK} + 30		t_{CLK} + 30		ns	

Display Cycle **(GDC ↔ Display Memory)**

		7220D Limits		7220D-1 Limits		7220D-2 Limits			Test
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Video Signal Delay from 2XWCLK ↑	t_{VD}		150		120		100	ns	C_L = 50 pF

Input Cycle **(GDC ↔ Display Memory)**

		7220D Limits		7220D-1 Limits		7220D-2 Limits			Test
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Input Signal Setup to 2XWCLK ↑	t_{PS}	30		20		15		ns	
Input Signal Width	t_{PW}	t_{CLK}		t_{CLK}		t_{CLK}		ns	

Clock **(2XWCLK)**

		7220D Limits		7220D-1 Limits		7220D-2 Limits			Test
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Clock Rise Time	t_{CR}		20		20		20	ns	
Clock Fall Time	t_{CF}		20		20		20	ns	
Clock High Pulse Width	t_{CH}	105		80		70		ns	
Clock Low Pulse Width	t_{CL}	105		80		70		ns	
Clock Cycle	t_{CLK}	250	2000	200	2000	180	2000	ns	

DC Characteristics

T_a = 0°C to 70°C; V_{CC} = 5V ± 10%; GND = 0V

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	①
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	②
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Low Leak Current	I_{IL}			−10	μA	V_I = 0V
Input High Leak Current	I_{IH}			+10	μA	V_I = V_{CC}
Output Low Leak Current	I_{OL}			−10	μA	V_O = 0V
Output High Leak Current	I_{OH}			+10	μA	V_O = V_{CC}
Clock Input Low Voltage	V_{CL}	−0.5		0.6	V	
Clock Input High Voltage	V_{CH}	3.5		V_{CC} + 1.0	V	
V_{CC} Supply Current	I_{CC}			270	mA	

Capacitance

T_a = 25°C; V_{CC} = GND = 0V

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	V_I (unmeasured) = 0V
Output Capacitance	C_{OUT}			20	pF	
Clock Input Capacitance	$C\phi$			20	pF	

Notes:
① For 2XWCLK, V_{IL} = −0.5V to +0.6V.
② For 2XWCLK, V_{IH} = +3.9V to V_{CC} +1.0V.

Absolute Maximum Ratings* (Tentative)

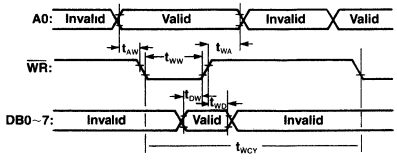
Ambient Temperature under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Power Dissipation	1.5 W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

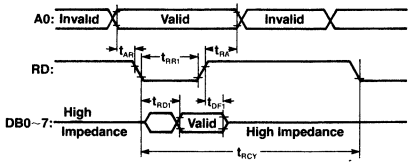
6

Timing Waveforms

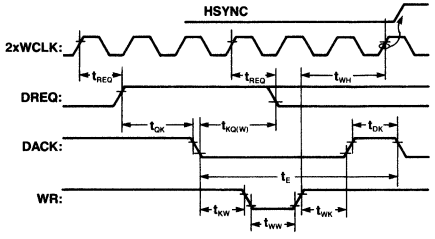
Microprocessor Interface Write Timing



Microprocessor Interface Read Timing



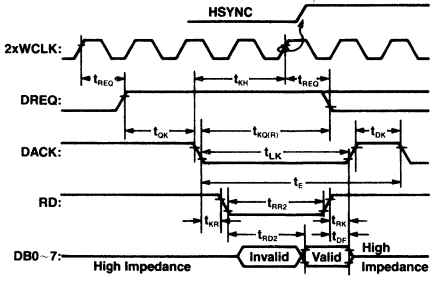
Microprocessor Interface DMA Write Timing



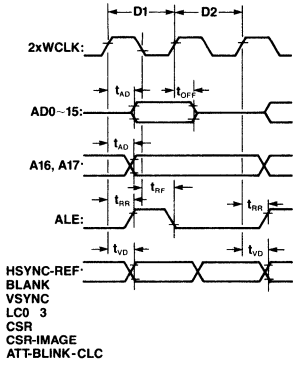
t_{WH} (WR ↑ to HSYNC ↑) ≥ t_{CLK}

t_{KH} (DACK ↓ to HSYNC ↑) ≥ t_{CLK}

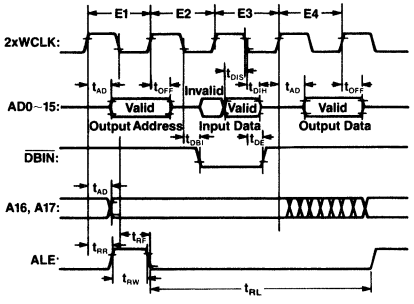
Microprocessor Interface DMA Read Timing



Display Memory Display Cycle Timing

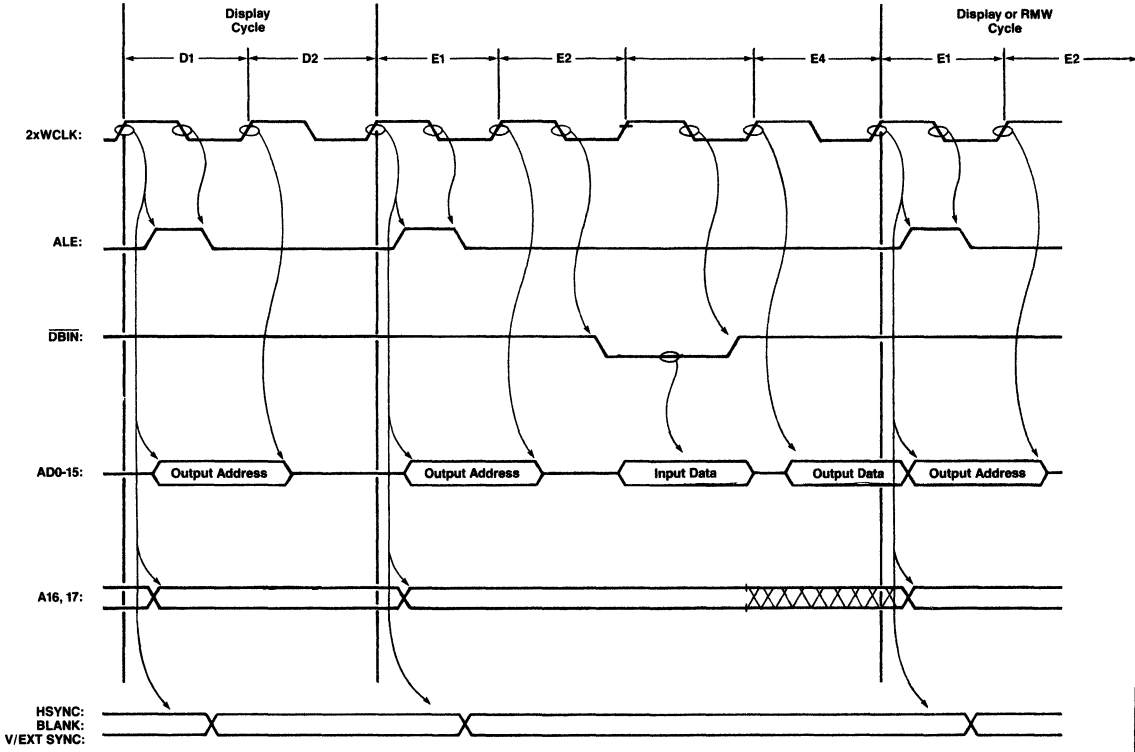


Display Memory RMW Timing

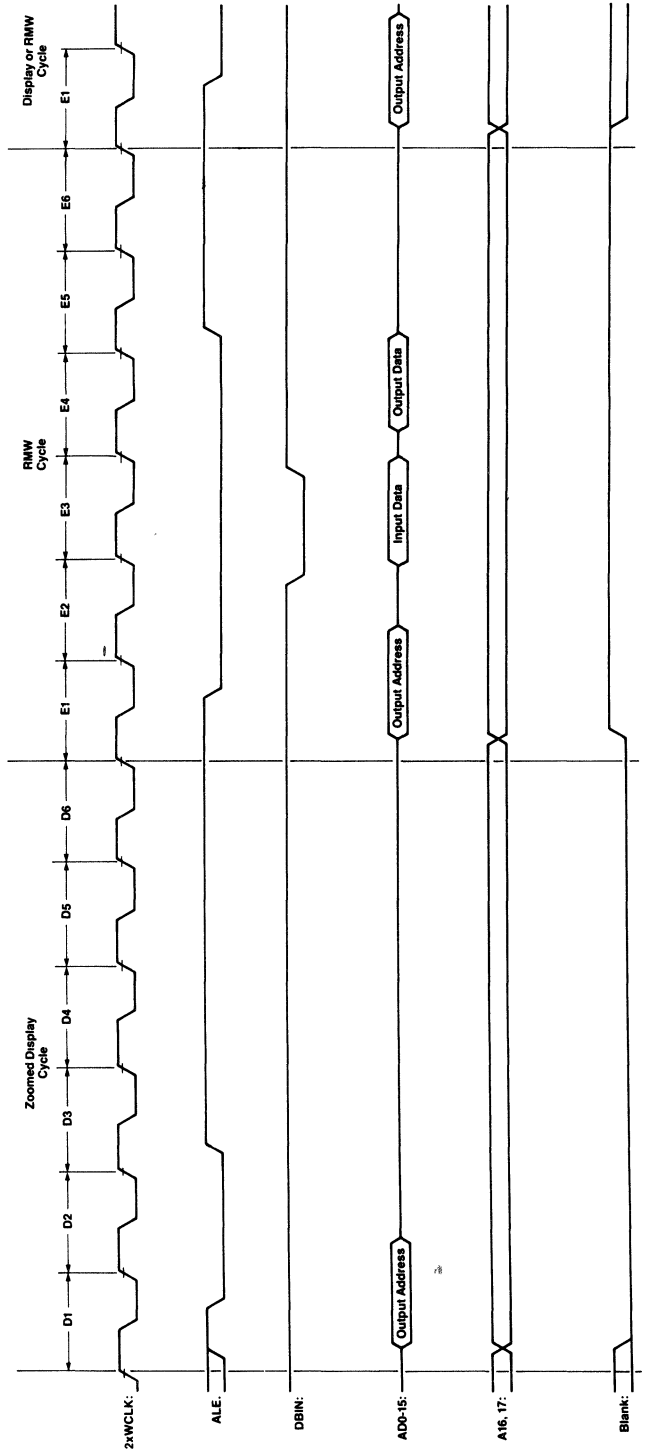


Timing Waveforms (Cont.)

Display and RMW Cycles (1x Zoom)



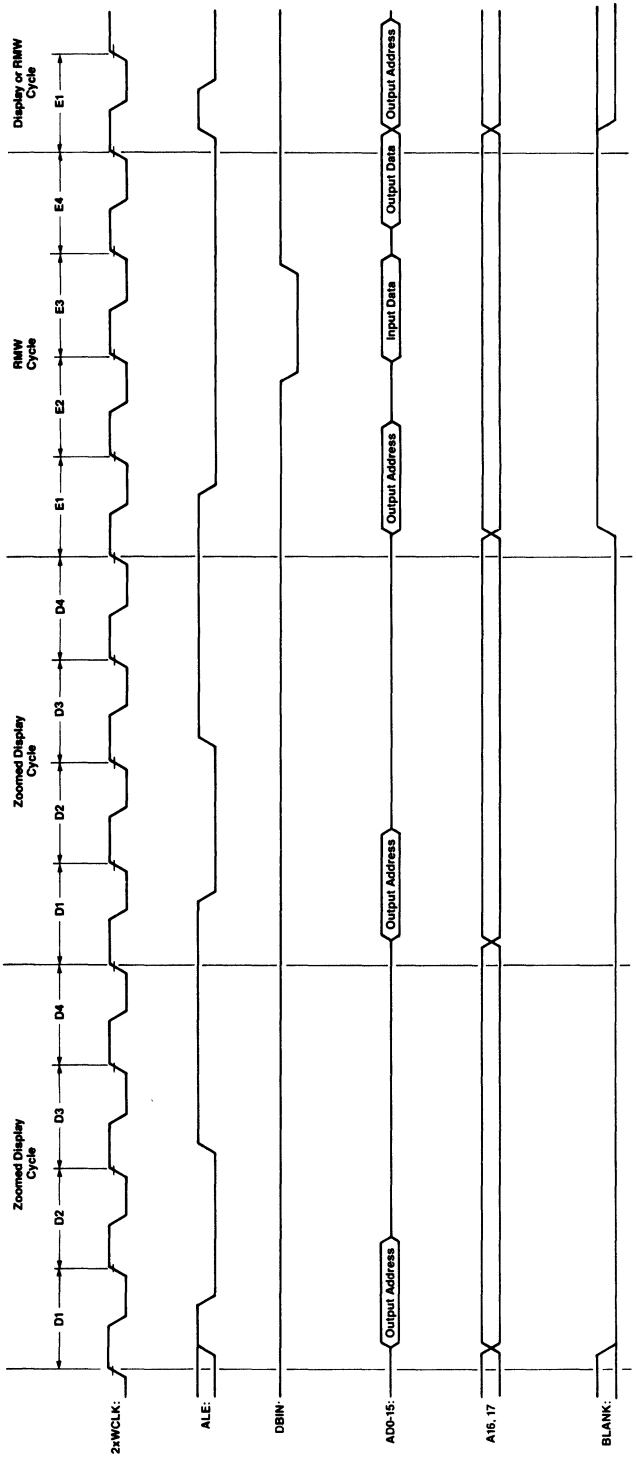
Timing Waveforms (Cont.)



Display and RMW Cycles (2x Zoom)

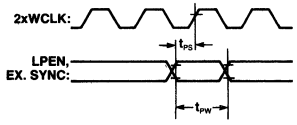
Timing Waveforms (Cont.)

Zoomed Display Operation with RMW Cycle (3x Zoom)

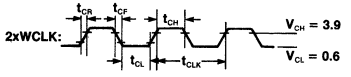


Timing Waveforms (Cont.)

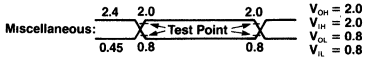
Light Pen and External Sync Input Timing



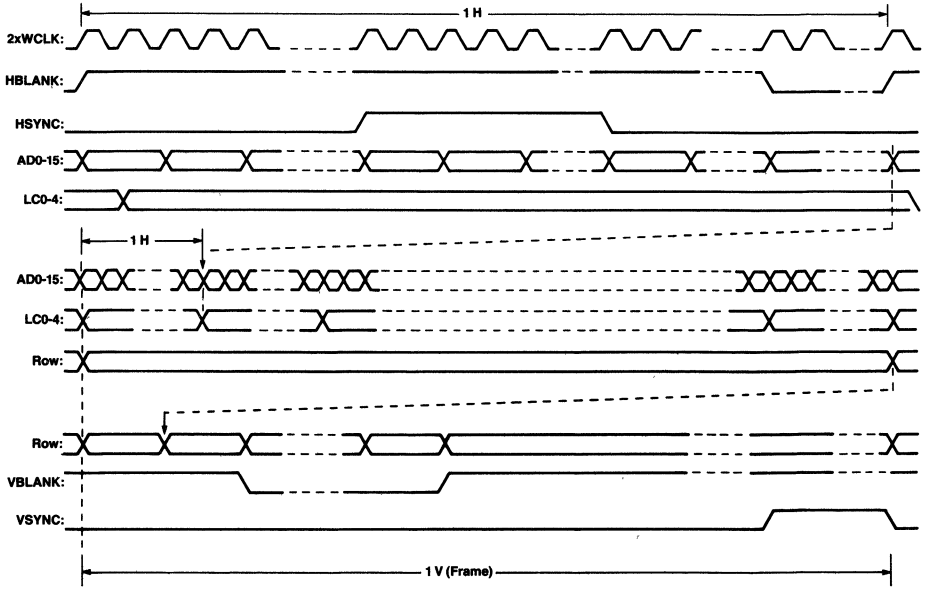
Clock Timing (2XWCLK)



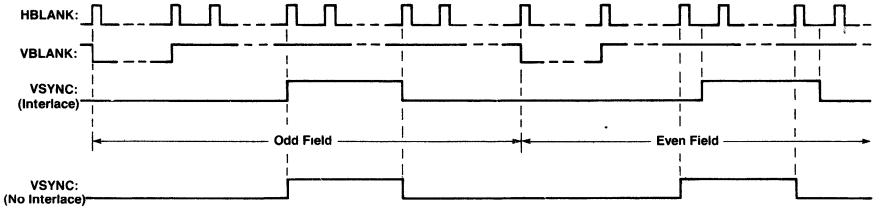
Test Level (for AC Tests, except 2XWCLK)



Video Sync Signals Timing

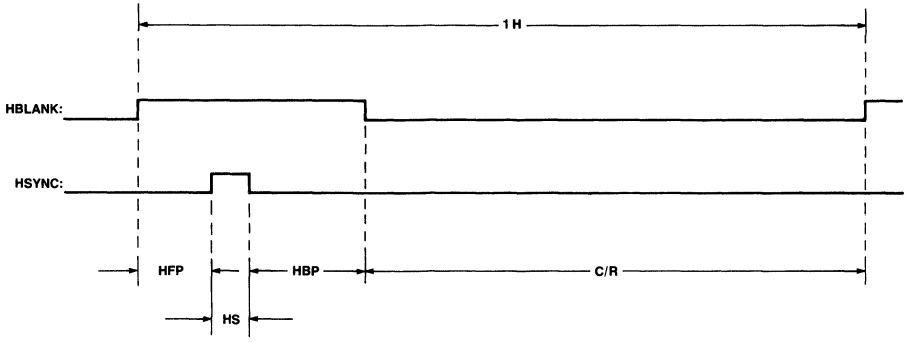


Interlaced Video Timing

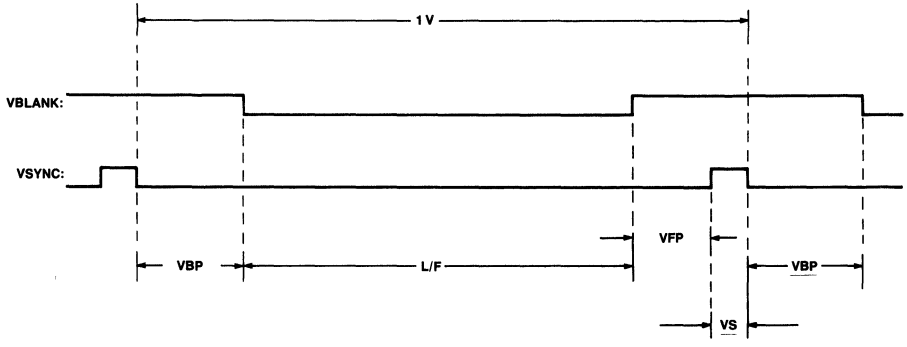


Timing Waveforms (Cont.)

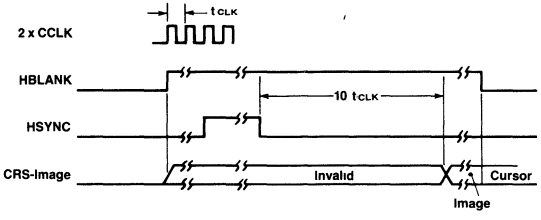
Video Horizontal Sync Generator Parameters



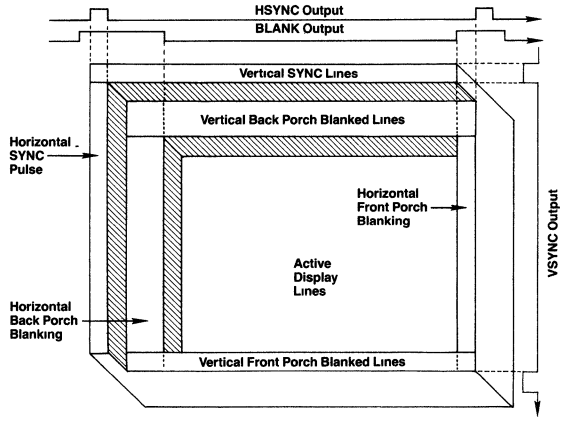
Video Vertical Sync Generator Parameters



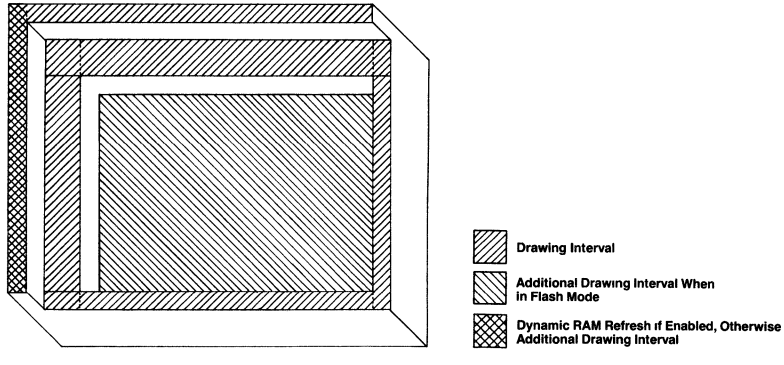
Cursor — Image Bit Flag



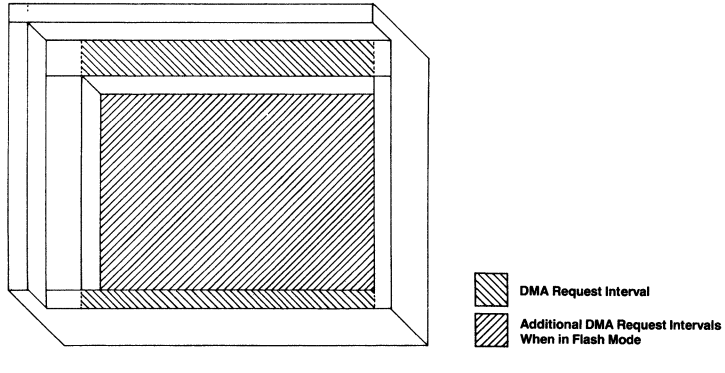
Video Field Timing



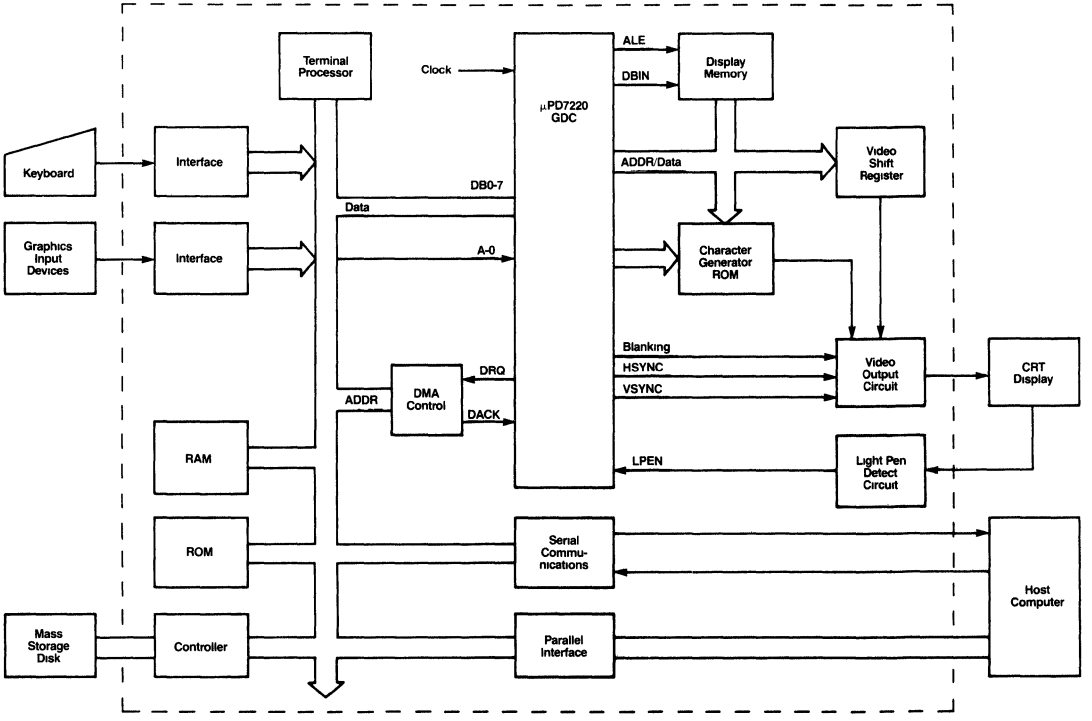
Drawing Intervals



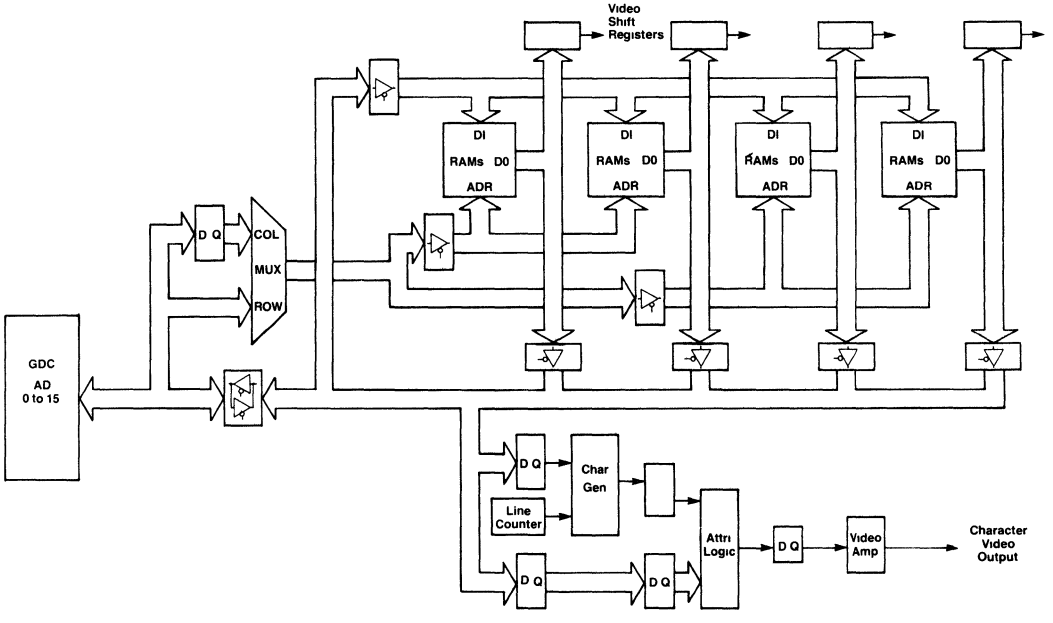
DMA Request Intervals



Block Diagram of a Graphics Terminal



Multiplane Display Memory Diagram



6

Package Outlines

For information, see Package Outline Section 7.

Ceramic, μPD7220D

μPD7225
INTELLIGENT ALPHANUMERIC LCD CONTROLLER/DRIVER

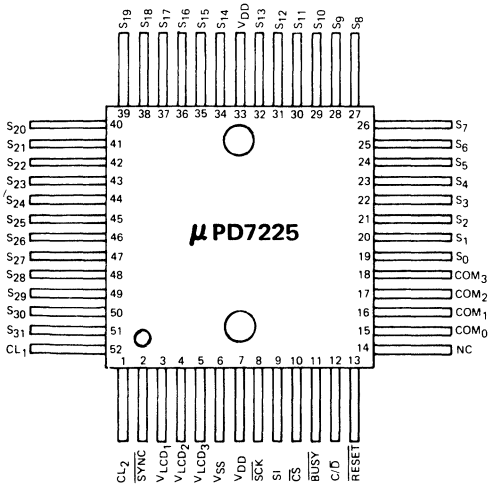
Description

The μPD7225 is an intelligent peripheral device designed to interface most microprocessors with a wide variety of alphanumeric LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 32 segments and is easily cascaded for larger LCD applications. The μPD7225 communicates with a host microprocessor through an 8-bit serial interface. It includes a 7-segment numeric and a 14-segment alphanumeric segment decoder to reduce system software requirements. The μPD7225 is manufactured with low power consumption CMOS process allowing use of a single power supply between 2.7V and 5.5V and is available in a space-saving 52-pin flat plastic package.

Features

- ☐ Single-chip LCD Controller with Direct LCD Drive
- ☐ Low-cost Serial Interface to most Microprocessors
- ☐ Compatible with:
  - 7-Segment Numeric LCD Configurations—up to 16 Digits
  - 14-Segment Alphanumeric LCD Configurations—up to 8 Characters
- ☐ Selectable LCD Drive Configuration: Static, Biplexed, Triplexed, or Quadriplexed
- ☐ 32-Segment Drivers
- ☐ Cascadable for Larger LCD Applications
- ☐ Selectable LCD Bias Voltage Configuration: Static, 1/2, or 1/3
- ☐ Hardware Logic Blocks Reduce System Software Requirements
  - — 8-Bit Serial Interface
  - — Two 32 x 4-Bit Static RAMs for Display Data and Blinking Data Storage
  - — Programmable Segment Decoding Capability
    - 16-Character, 7-Segment Numeric Decoder
    - 64-Character, 14-Segment USASCII Alphanumeric Decoder
  - — Programmable Segment Blinking Capability
  - — Automatic Synchronization of Segment Drivers with Sequentially Multiplexed Backplane Drivers
- ☐ Single Power Supply, Variable from 2.7V to 5.5V
- ☐ Low Power Consumption CMOS Technology
- ☐ Extended −40°C to +85°C Temperature Range Available
- ☐ Space-saving 52-Pin Flat Plastic Package

Pin Configuration

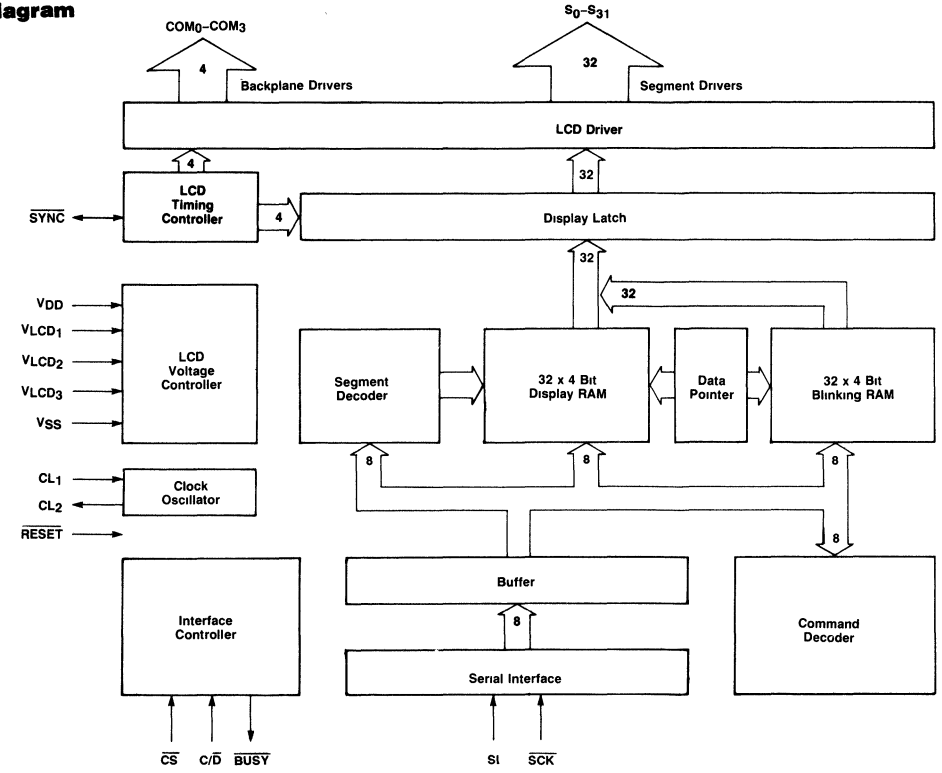


Pin Description

Pin No.	Pin Symbol	Function
1	CL_2	System clock output (active high). Connect to CL_1 with 180kΩ resistor, or leave open.
2	$\overline{SYNC}$	Synchronization port (active low). For multichip operation tie all $\overline{SYNC}$ lines together.
3–5	V_{LCD_1}, V_{LCD_2}, V_{LCD_3}	LCD bias voltage supply inputs to LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.
6	V_{SS}	Ground.
7, 33	V_{DD}	Power supply positive. Apply single voltage ranging from 2.7V to 5.5V for proper operation.
8	$\overline{SCK}$	Serial clock input (active low). Synchronizes 8-bit serial data transfer from microprocessor to μPD7225.
9	SI	Serial input (active high). Data input from microprocessor.
10	$\overline{CS}$	Chip select input (active low). Enables μPD7225 for data input from microprocessor. Display can also be updated when μPD7225 is deselected.
11	$\overline{BUSY}$	Busy output (active low). Handshake line indicates that μPD7225 is ready to receive next data byte.
12	$C/\overline{D}$	Command/data select input (active both high and low). Distinguishes serially input data byte as a command or as display data.
13	$\overline{RESET}$	Reset input (active low). R/C circuit or pulse initializes μPD7225 after power-up.
14	NC	No connection.
15–18	COM_0–COM_3	LCD Backplane Driver Outputs.
19–32, 34–51	S_0–S_{31}	LCD Segment Driver Outputs.
52	CL_1	System clock input (active high). Connect to CL_2 with 180kΩ resistor, or to external clock source.

6

Block Diagram



Command Summary

Command	Description	Instruction Code Binary D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
1. MODE SET	Initialize the μPD7225, including selection of: 1) LCD Drive Configuration 2) LCD Bias Voltage Configuration 3) LCD Frame Frequency	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
2. UNSYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with $\overline{CS}$	0	0	1	1	0	0	0	0	30
3. SYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with LCD Drive Cycle	0	0	1	1	0	0	0	1	31
4. INTERRUPT DATA TRANSFER	Interrupt Display RAM data transfer to Display Latch	0	0	1	1	1	0	0	0	38
5. LOAD DATA POINTER	Load Data Pointer with 5 bits of Immediate Data	1	1	1	D_4	D_3	D_2	D_1	D_0	E0-FF
6. CLEAR DISPLAY RAM	Clear the Display RAM and reset the Data Pointer	0	0	1	0	0	0	0	0	20
7. WRITE DISPLAY RAM	Write 4 bits of Immediate Data to the Display RAM location addressed by the Data Pointer; Increment Data Pointer	1	1	0	1	D_3	D_2	D_1	D_0	D0-DF
8. AND DISPLAY RAM	Perform a Logical AND between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data; Write result to same Display RAM location Increment Data Pointer	1	0	0	1	D_3	D_2	D_1	D_0	90-9F

Command	Description	Instruction Code (Binary) D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
9. OR DISPLAY RAM	Perform a Logical OR between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data, Write result to same Display RAM location, Increment Data Pointer	1	0	1	1	D_3	D_2	D_1	D_0	B0-BF
10. ENABLE SEGMENT DECODER	Start use of the Segment Decoder	0	0	0	1	0	1	0	1	15
11. DISABLE SEGMENT DECODER	Stop use of the Segment Decoder	0	0	0	1	0	1	0	0	14
12. ENABLE DISPLAY	Turn on the LCD	0	0	0	1	0	0	0	1	11
13. DISABLE DISPLAY	Turn off the LCD	0	0	0	1	0	0	0	0	10
14. CLEAR BLINKING RAM	Clear the Blinking RAM and reset the Data Pointer	0	0	0	0	0	0	0	0	00
15. WRITE BLINKING RAM	Write 4 bits of Immediate Data to the Blinking RAM location addressed by the Data Pointer; Increment Data Pointer	1	1	0	0	D_3	D_2	D_1	D_0	C0-CF
16. AND BLINKING RAM	Perform a Logical AND between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data; Write result to same Blinking RAM Location; Increment Data Pointer	1	0	0	0	D_3	D_2	D_1	D_0	80-8F
17. OR BLINKING RAM	Perform a Logical OR between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data, Write result to same Blinking Location; Increment Data Pointer	1	0	1	0	D_3	D_2	D_1	D_0	A0-AF
18. ENABLE BLINKING	Start Segment Blinking at the Frequency Specified by 1 bit of Immediate Data	0	0	0	1	1	0	1	D_0	1A-1B
19. DISABLE BLINKING	Stop Segment Blinking	0	0	0	1	1	0	0	0	18

Details of operation and application examples can be found in the "μPD7225 Intelligent Alphanumeric LCD Controller/Driver Technical Manual."

Absolute Maximum Ratings*

T_a = 25°C	
Supply Voltage, V_{DD}	−0.3V to +7.0V
All Inputs and Outputs with Respect to V_{SS}	−0.3V to V_{DD} +0.3V
Storage Temperature	−65°C to +150°C
Operating Temperature	−10°C to +70°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C; V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	
Input Leakage Current High	I_{LIH}			2	μA	V_{IH} = V_{DD}
Input Leakage Current Low	I_{LIL}			−2	μA	V_{IL} = 0V
Output Voltage High	V_{OH}	V_{DD} −0.5			V	$\overline{BUSY}$, $\overline{SYNC}$, I_{OH} = −10 μA
Output Voltage Low	V_{OL_1}			0.5	V	$\overline{BUSY}$, I_{OL} = 100 μA
	V_{OL_2}			1.0	V	$\overline{SYNC}$, I_{OL} = 900 μA
Output Leakage Current Low	I_{LOH}			2	μA	V_{OH} = V_{DD}
	I_{LOL}			−2	μA	V_{OL} = 0V
Output Short Circuit Current	I_{OS}			−300	μA	$\overline{SYNC}$, V_{OS} = 1.0V
Backplane Driver Output Impedance	R_{COM}		5	7	kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Segment Driver Output Impedance	R_{SEG}		7	14	kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Supply Current	I_{DD}		100	250	μA	CL_1 external clock, f_ϕ = 200 KHz

DC Characteristics (Cont.)

T_a = 0°C to +70°C; V_{DD} = 2.7 to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Voltage High	V_{IH_1}	0.7 V_{DD}		V_{DD}	V	Except $\overline{SCK}$
	V_{IH_2}	0.8 V_{DD}		V_{DD}	V	$\overline{SCK}$
Input Voltage Low	V_{IL_1}	0		0.3 V_{DD}	V	Except $\overline{SCK}$
	V_{IL_2}	0		0.2 V_{DD}	V	$\overline{SCK}$
Input Leakage Current High	I_{LIH}			2	μA	$V_{IH} = V_{DD}$
Input Leakage Current Low	I_{LIL}			−2	μA	V_{IL} = 0V
Output Voltage High	V_{OH}	V_{DD} − 0 75			V	$\overline{BUSY}$, $\overline{SYNC}$, I_{OH} = −7 μA
Output Voltage Low	V_{OL_1}			0.5	V	$\overline{BUSY}$, I_{OL} = 100 μA
	V_{OL_2}			0.5	V	$\overline{SYNC}$, I_{OL} = 400 μA
Output Leakage Current Low	I_{LOH}			2	μA	$V_{OH} = V_{DD}$
	I_{LOL}			−2	μA	V_{OL} = 0V
Output Short Circuit Current	I_{OS}			−200	μA	$\overline{SYNC}$, V_{OS} = 0.5V
Backplane Driver Output Impedance	R_{COM}		6		kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Segment Driver Output Impedance	R_{SEG}		12		kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$. Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes
Supply Current	I_{DD}		30	100	μA	CL_1 external clock, V_{DD} = 3.0V ± 10%, f_ϕ = 140 KHz

AC Characteristics

T_a = −10°C to +70°C; V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Frequency	f_ϕ	50		200	KHz	
	f_{OSC}	85	130	175	KHz	R = 180 kΩ + 5%
Clock Pulse Width High	$t_\phi W_H$	2		16	μs	CL_1, external clock
Clock Pulse Width Low	$t_\phi W_L$	2		16	μs	CL_1, external clock
$\overline{SCK}$ Cycle	t_{CY_K}	900			ns	
$\overline{SCK}$ Pulse Width High	t_{KW_H}	400			ns	
$\overline{SCK}$ Pulse Width Low	t_{KW_L}	400			ns	
$\overline{BUSY}$↑ to $\overline{SCK}$↓ Hold Time	t_{BH_K}	0			ns	
SI Setup Time to $\overline{SCK}$↑	t_{IS_K}	100			ns	
SI Hold Time After $\overline{SCK}$↑	t_{IH_K}	200			ns	
8th $\overline{SCK}$↑ to $\overline{BUSY}$↓ Delay Time	t_{KD_B}			3	μs	C_{LOAD} = 50 pF
$\overline{CS}$↓ to $\overline{BUSY}$↓ Delay Time	t_{CD_B}			1 5	μs	C_{LOAD} = 50 pF
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$↑	t_{DS_K}	9			μs	
C/$\overline{D}$ Hold Time After 8th $\overline{SCK}$↑	t_{DH_K}	1			μs	
$\overline{CS}$ Hold Time After 8th $\overline{SCK}$↑	t_{CH_K}	1			μs	
$\overline{CS}$ Pulse Width High	t_{CW_H}	8/f_ϕ			μs	
$\overline{CS}$ Pulse Width Low	t_{CW_L}	8/f_ϕ			μs	

AC Characteristics (Cont.)

T_a = 0°C to +70°C; V_{DD} = 2.7V to 5.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Frequency	f_ϕ	50		140	KHz	
	f_{OSC}	50	100	140	KHz	R = 180 kΩ + 5%, V_{DD} = 3 0V ± 10%
Clock Pulse Width High	$t_\phi W_H$	3		16	μs	CL_1, external clock
Clock Pulse Width Low	$t_\phi W_L$	3		16	μs	CL_1, external clock
$\overline{SCK}$ Cycle	t_{CY_K}	4			μs	
$\overline{SCK}$ Pulse Width High	t_{KW_H}	1 8			μs	
$\overline{SCK}$ Pulse Width Low	t_{KW_L}	1 8			μs	
$\overline{BUSY}$↑ to $\overline{SCK}$↓ Hold Time	t_{BH_K}	0			ns	
SI Setup Time to $\overline{SCK}$↑	t_{IS_K}	1			μs	
SI Hold Time After $\overline{SCK}$↑	t_{IH_K}	1			μs	
8th $\overline{SCK}$↑ to $\overline{BUSY}$↓ Delay Time	t_{KD_B}			5	μs	C_{LOAD} = 50 pF
$\overline{CS}$↓ to $\overline{BUSY}$↓ Delay Time	t_{CD_B}			5	μs	C_{LOAD} = 50 pF
C/$\overline{D}$ Setup Time to 8th $\overline{SCK}$↑	t_{DS_K}	18			μs	
C/$\overline{D}$ Hold Time After 8th $\overline{SCK}$↑	t_{DH_K}	1			μs	
$\overline{CS}$ Hold Time After 8th $\overline{SCK}$↑	t_{CH_K}	1			μs	
$\overline{CS}$ Pulse Width High	t_{CW_H}	8/f_ϕ			μs	
$\overline{CS}$ Pulse Width Low	t_{CW_L}	8/f_ϕ			μs	
$\overline{SYNC}$ Load Capacitance	C_{LOAD}			50	pF	f_ϕ = 200 KHz

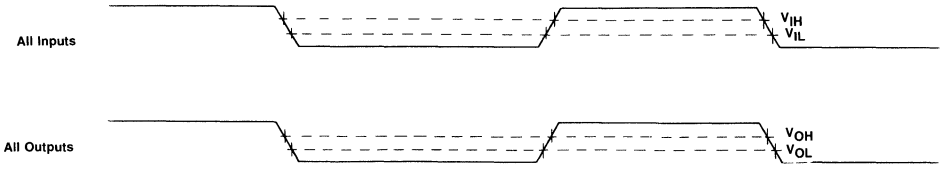
Capacitance

T_a = 25°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10	pF	
Output Capacitance	C_{O_1}			20	pF	Except $\overline{BUSY}$
	C_{O_2}			15	pF	$\overline{BUSY}$
Input/Output Capacitance	C_{IO}			15	pF	$\overline{SYNC}$
Clock Capacitance	C_ϕ			30	pF	CL_1 Input

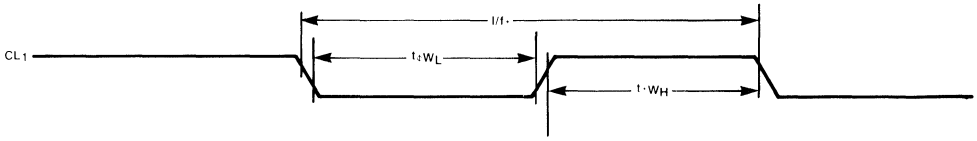
f_ϕ = 1 MHz. Unmeasured pins return to 0V.

AC Timing Characteristics

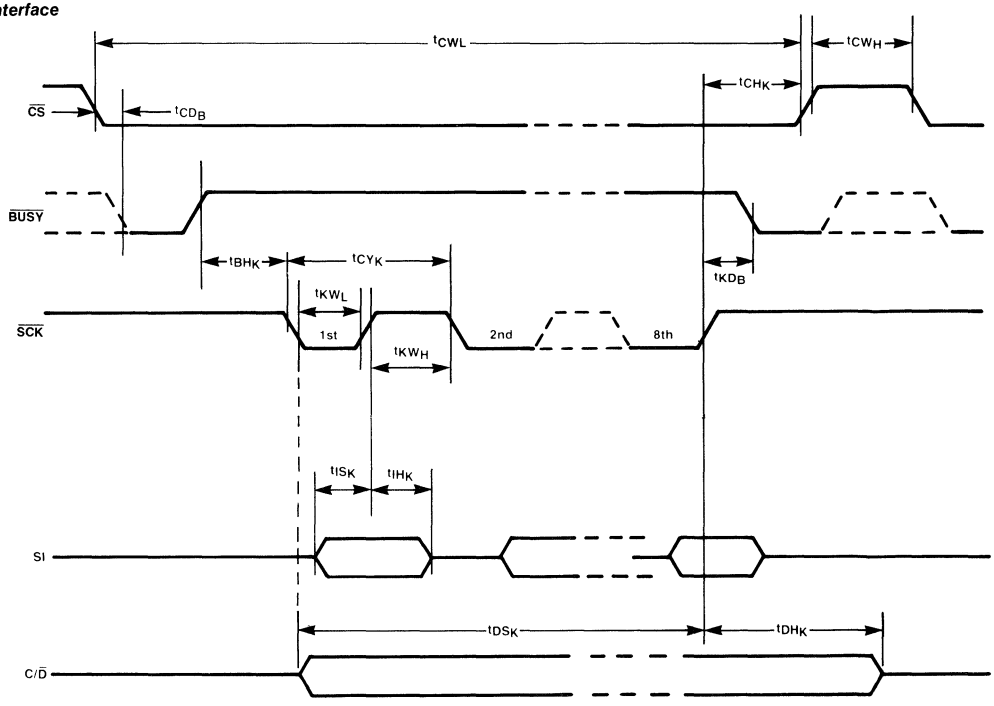


Timing Waveforms

Clock



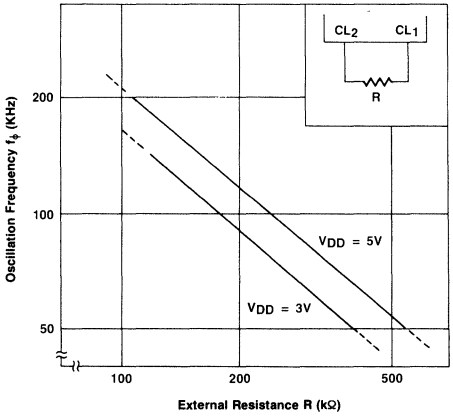
Serial Interface



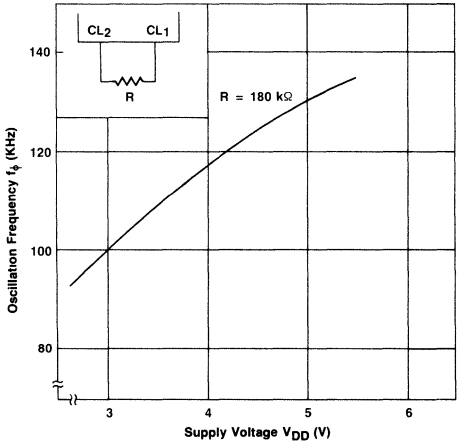
Characteristics Curves

T_a = 25°C

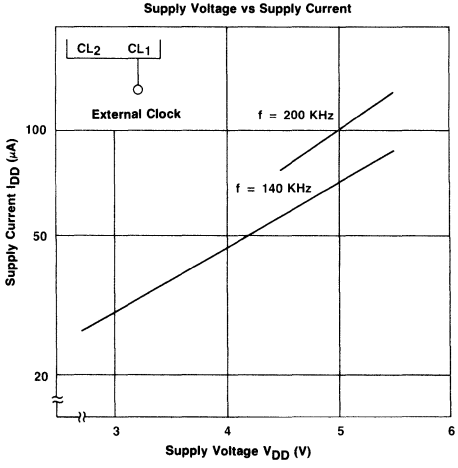
External Resistance vs Oscillation Frequency



Supply Voltage vs Oscillation Frequency



Supply Voltage vs Supply Current



7-Segment Numeric Data Decoder Character Set

Display Byte (HEX)	Character	Decoded Display RAM Data				
		Triplexed			Quadruplexed	
		Display RAM Address			Display RAM Address	
		n+2	n+1	n	n+1	n
00		3	5	3	D	7
01		0	0	3	0	6
02		2	7	1	E	3
03		0	7	3	A	7
04		1	2	3	3	6
05		1	7	2	B	5
06		3	7	2	F	5
07		0	1	3	0	7
08		3	7	3	F	7
09		1	7	3	B	7
0A		3	2	0	2	0
0B		3	7	0	F	1
0C		3	5	0	D	1
0D		0	6	0	A	0
0E		2	6	2	E	4
0F		0	0	0	0	0

Display Byte (HEX)	Char	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char	Display RAM Address n+3	n+2	n+1	n
A0		0	0	0	0	B0		4	7	E	2	C0		A	7	C	0	D0		2	3	6	4
A1			Invalid			B1		0	6	0	0	C1		2	7	6	4	D1		0	7	E	8
A2			Invalid			B2		2	3	C	4	C2		8	7	8	5	D2		2	3	6	C
A3			Invalid			B3		2	7	8	4	C3		0	1	E	0	D3		1	5	8	4
A4			Invalid			B4		2	6	2	4	C4		8	7	8	1	D4		8	1	0	1
A5			Invalid			B5		2	5	A	4	C5		2	1	E	4	D5		0	6	E	0
A6			Invalid			B6		2	5	E	4	C6		2	1	6	4	D6		4	0	6	2
A7		0	0	0	2	B7		0	7	0	0	C7		0	5	E	4	D7		4	6	6	8
A8		0	0	0	A	B8		2	7	E	4	C8		2	6	6	4	D8		5	0	0	A
A9		5	0	0	0	B9		2	7	A	4	C9		8	1	8	1	D9		9	0	0	2
AA		F	0	0	F	BA			Invalid			CA		0	6	C	0	DA		4	1	8	2
AB		A	0	0	5	BB			Invalid			CB		2	0	6	A	DB			Invalid		
AC			Invalid			BC		4	0	8	2	CC		0	0	E	0	DC		1	0	0	8
AD		2	0	0	4	BD		2	0	8	4	CD		1	6	6	2	DD			Invalid		
AE			Invalid			BE		1	0	8	8	CE		1	6	6	8	DE			Invalid		
AF		4	0	0	2	BF			Invalid			CF		0	7	E	0	DF			Invalid		

Package Outlines

For information, see Package Outline Section 7.

Plastic Miniflat, μPD7225G

μPD7227 INTELLIGENT DOT-MATRIX LCD CONTROLLER/DRIVER

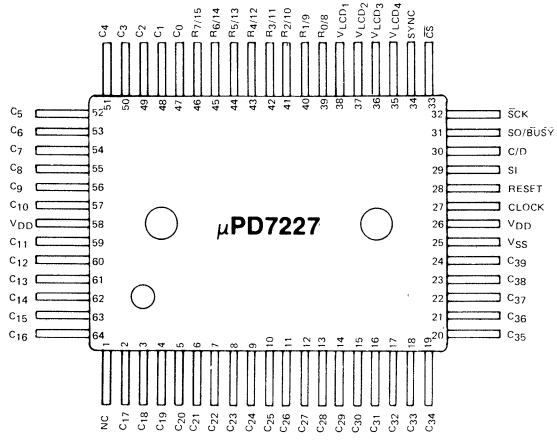
DESCRIPTION

The μPD7227 Intelligent Dot-matrix LCD Controller/Driver is a peripheral device designed to interface most microprocessors with a wide variety of dot matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 40 columns, and is easily cascaded up to 16 rows and 280 columns. The μPD7227 is equipped with several hardware logic blocks, such as an 8-bit serial interface, ASCII character generator, 40 x 16 static RAM with full read/write capability, and an LCD timing controller; all of which reduce microprocessor system software requirements. The μPD7227 is manufactured with a single 5V CMOS process, and is available in a space-saving 64-pin flat plastic package.

FEATURES

- Single-chip LCD controller with direct LCD drive
- Compatible with most microprocessors
- Eight row drives
  - Designed for dot-matrix LCD configurations up to 280 dots
  - Designed for 5 x 7 dot-matrix character LCD configuration; up to 8 characters
  - Cascadable to 16 row drives
- 40 column drives
  - Cascadable to 280 column drives
- Hardware logic blocks reduce system software requirements
  - 8-bit serial interface for communication
  - ASCII 5 x 7 dot-matrix character generator with 64-character vocabulary
  - 40 x 16 bit static RAM for data storage, retrieval, and complete back-up memory capability
  - Voltage controller generates LCD bias voltages
  - Timing controller synchronizes column drives with sequentially-multiplexed row drives
- Single +5V power supply
- CMOS technology

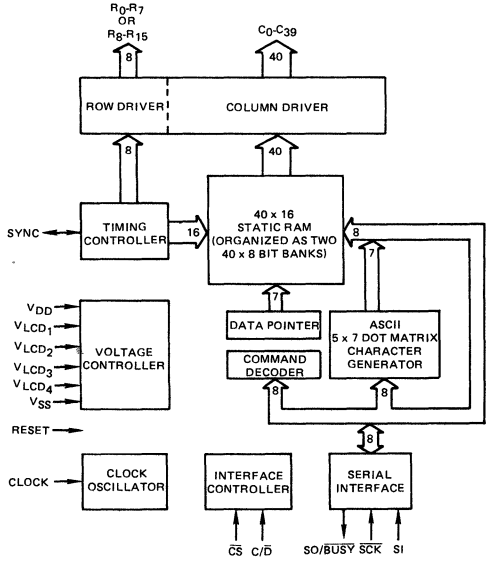
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	NC	No connection
2-24, 47-57, 59-64	C_0-C_{39}	LCD Column Driver Outputs
25	V_{SS}	Ground
26, 58	V_{DD}	Power supply positive Apply single voltage ranging from 2.7V to 5.5V for proper operation
27	CLOCK	System Clock input (active high) connect to external clock source.
28	RESET	Reset input (active high) R/C circuit or pulse initializes μPD7227 after power-up
29	SI	Serial input (active high) Data input from microprocessor
30	C/$\overline{D}$	Command/Data Select input (active both high and low) Distinguishes serially input data byte as a command or as display data.
31	SO/$\overline{BUSY}$	Serial Output (active high)/Busy output (active low) Data output from μPD7227 to microprocessor when in READ MODE and C/$\overline{D}$ is low Handshake output indicates that μPD7227 is ready to receive/send next data byte
32	$\overline{SCK}$	Serial Clock input (active low) Synchronizes 8-bit serial data transfer between microprocessor and μPD7227
33	$\overline{CS}$	Chip Select Input (active low) enables μPD7227 for communication with microprocessor
34	SYNC	Synchronization port (active high) For multichip operation tie all SYNC lines together, and configure with MODE SET command
35-38	V_{LCD_1}, V_{LCD_2}, V_{LCD_3}, V_{LCD_4}	LCD Bias Voltage supply inputs to LCD Voltage Controller Apply appropriate voltages from a voltage ladder connected across V_{DD}.
39-46	$R_{0/8}$-$R_{7/15}$	LCD Row Driver Outputs.

BLOCK DIAGRAM



COMMAND SUMMARY

Command	Description	Instruction Code								
		Binary								HEX
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1. MODE SET	Initialize the μPD7227, including selection of 1. LCD Drive Configuration 2. Row Driver Port Function 3. RAM Bank 4. SYNC Port Function	0	0	0	1	1	D_2	D_1	D_0	18-1F
2. FRAME FREQUENCY SET	Set LCD Frame Frequency	0	0	0	1	0	D_2	D_1	D_0	10-17
3. LOAD DATA POINTER	Load Data Pointer with 7 bits of Immediate Data	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80-E7
4. WRITE MODE	Write Display Byte in Serial Register to RAM location addressed by Data Pointer, modify Data Pointer	0	1	1	0	0	1	D_1	D_0	64-67
5. READ MODE	Load RAM contents addressed by Data Pointer into Serial Register for output; modify Data Pointer	0	1	1	0	0	0	D_1	D_0	60-63
6. AND MODE	Perform a Logical AND between the display byte in the Serial Register and the RAM contents addressed by Data Pointer; write result to same RAM location; modify Data Pointer	0	1	1	0	1	1	D_1	D_0	6C-6F
7. OR MODE	Perform a Logical OR between the display byte in the Serial Register and the RAM contents addressed by Data Pointer; write Result to same RAM location; modify Data Pointer	0	1	1	0	1	0	D_1	D_0	68-6B
8. CHARACTER MODE	Decode display byte in Serial Register into 5 x 7 character with Character Generator; write character to RAM location addressed by Data Pointer; increment Data Pointer by 5	0	1	1	1	0	0	1	0	72
9. SET BIT	Set single bit of RAM location addressed by Data Pointer; modify Data Pointer	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
10. RESET BIT	Reset single bit of RAM location addressed by Data Pointer; modify Data Pointer	0	0	1	D_4	D_3	D_2	D_1	D_0	20-3F
11. ENABLE DISPLAY	Turn on the LCD	0	0	0	0	1	0	0	1	09
12. DISABLE DISPLAY	Turn off the LCD	0	0	0	0	1	0	0	0	08

Further details of operation can be found in the "μPD7227 Intelligent Dot-Matrix LCD Controller/Driver Technical Manual."

ABSOLUTE MAXIMUM RATINGS*

Power Supply, V_{DD} . . . . . −0.3V to +7.0V
All inputs and outputs with respect to V_{SS} . . . . . −0.3V to V_{DD} +0.3
Storage Temperature . . . . . −65° C to +150° C
Operating Temperature. . . . . −10°C to +70°C

T_a = 25°C

*COMMENT. Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{DD} = + 5.0V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITIONS
Input Voltage High	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input Voltage Low	V_{IL}	0		0.3 V_{DD}	V	
Input Leakage Current High	I_{LIH}			+10	μA	V_{IH} = V_{DD}
Input Leakage Current Low	I_{LIL}			−10	μA	V_{IH} = 0V
Output Voltage High	V_{OH_1}	V_{DD}-0.5			V	SO/$\overline{BUSY}$, I_{OH} = −400 μA
	V_{OH_2}					SYNC, I_{OH} = −100 μA
Output Voltage Low	V_{OL_1}			0.45	V	SO/$\overline{BUSY}$, I_{OL} = +1.7mA
	V_{OL_2}					SYNC, I_{OL} = +100 μA
Output Leakage Current High	I_{LOH}			+10	μA	V_{OH} = V_{DD}
Output Leakage Current Low	I_{LOL}			−10	μA	V_{OL} = 0V
LCD Operating Voltage	V_{LCD}	3.0		V_{DD}	V	8-Row Multiplexed LCD Drive Configuration
			V_{DD}			16-Row Multiplexed LCD Drive Configuration
Row Drive Output Impedance	R_{ROW}		4	8	kΩ	
Column Drive Output Impedance	R_{COLUMN}		10	15	kΩ	
Supply Current	I_{DD}		200	400	μA	fϕ = 400 KHz

CAPACITANCE

T_a = −25°C, V_{DD} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	CONDITIONS
Input Capacitance	C_I			10	pF	fϕ = 1 MHz
Output Capacitance	C_O			25	pF	Unmeasured pins returned to Ground.
Input/Output Capacitance	C_{IO}			15	pF SYNC	

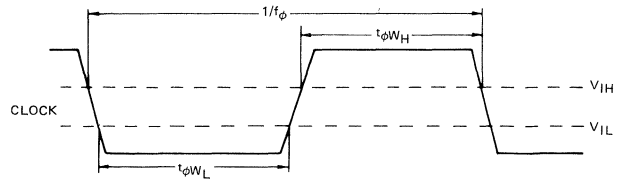
AC CHARACTERISTICS $T_a = -10°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	CONDITIONS
Clock Frequency	$f\phi$	100		1000	KHz	
Clock Pulse Width High	$t\phi W_H$	400			ns	
Clock Pulse Width Low	$t\phi W_L$	400			ns	
$\overline{SCK}$ Cycle	t_{CY_K}	0.9			μs	
$\overline{SCK}$ Pulse Width High	t_{kW_H}	400			ns	
$\overline{SCK}$ Pulse Width Low	t_{KW_L}	400			ns	
$\overline{SCK}$ Hold Time After $\overline{BUSY}\uparrow$	t_{KH_B}	0			ns	
SI Setup Time To $\overline{SCK}\uparrow$	t_{IS_K}	100			ns	
SI Hold Time After $\overline{SCK}\uparrow$	t_{IH_K}	250			ns	
SO Delay Time After $\overline{SCK}\downarrow$	t_{OD_K}			320	ns	
SO Delay Time After $C/\overline{D}\downarrow$	t_{OD_D}			2	μs	
$\overline{SCK}$ Hold Time After $C/\overline{D}\downarrow$	t_{KH_D}	2			μs	
$\overline{BUSY}$ Delay Time After 8th $\overline{SCK}\uparrow$	t_{BD_K}			3	μs	$C_{LOAD} = 50$ pF
$\overline{BUSY}$ Delay Time After $C/\overline{D}\uparrow$	t_{BD_D}			2	μs	
$\overline{BUSY}$ Delay Time After $\overline{CS}\downarrow$	t_{BD_C}			2	μs	
$C/\overline{D}$ Setup Time to 8th $\overline{SCK}\uparrow$	t_{DS_K}	2			μs	
$C/\overline{D}$ Hold Time After 8th $\overline{SCK}\uparrow$	t_{DH_K}	2			μs	
$\overline{CS}$ Hold Time After 8th $\overline{SCK}\uparrow$	t_{CH_K}	2			μs	
$\overline{CS}$ Pulse Width High	t_{CW_H}	$2/f\phi$			μs	
$\overline{CS}\uparrow$ Delay Time to $\overline{BUSY}$ Floating	t_{CD_B}	2			μs	$C_{LOAD} = 50$ pF
SYNC Load Capacitance	C_{LOAD_S}			100	pF	

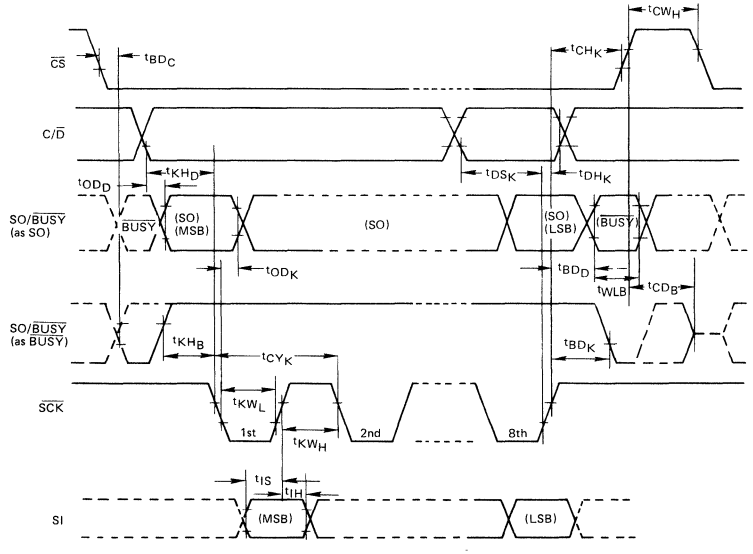
AC CHARACTERISTICS T_a −10 to +70° C, V_{DD} = 2.7 to 5 5V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	CONDITIONS
Clock Frequency	$f\phi$	100		250	KHz	
Clock Pulse Width High	$t\phi W_H$	1800			ns	
Clock Pulse Width Low	$t\phi W_L$	1800			ns	
$\overline{SCK}$ Cycle	t_{CY_K}	4			μs	
$\overline{SCK}$ Pulse Width High	t_{kW_H}	1800			ns	
$\overline{SCK}$ Pulse Width Low	t_{KW_L}	1800			ns	
$\overline{SCK}$ Hold Time After $\overline{BUSY}\uparrow$	t_{KH_B}	0			ns	
SI Setup Time To $\overline{SCK}\uparrow$	t_{IS_K}	500			ns	
SI Hold Time After $\overline{SCK}\uparrow$	t_{IH_K}	1			ns	
SO Delay Time After $\overline{SCK}\downarrow$	t_{OD_K}			1200	ns	
SO Delay Time After $C/\overline{D}\downarrow$	t_{OD_D}			3	μs	
$\overline{SCK}$ Hold Time After $C/\overline{D}\downarrow$	t_{KH_D}	3			μs	
$\overline{BUSY}$ Delay Time After 8th $\overline{SCK}\uparrow$	t_{BD_K}			4	μs	$C_{LOAD} = 50$ pF
$\overline{BUSY}$ Delay Time After $C/\overline{D}\uparrow$	t_{BD_D}			3	μs	
$\overline{BUSY}$ Delay Time After $\overline{CS}\downarrow$	t_{BD_C}			3	μs	
$C/\overline{D}$ Setup Time to 8th $\overline{SCK}\uparrow$	t_{DS_K}	3			μs	
$C/\overline{D}$ Hold Time After 8th $\overline{SCK}\uparrow$	t_{DH_K}	3			μs	
$\overline{CS}$ Hold Time After 8th $\overline{SCK}\uparrow$	t_{CH_K}	3			μs	
$\overline{CS}$ Pulse Width High	t_{CW_H}	$2/f\phi$			μs	
$\overline{CS}\uparrow$ Delay Time to $\overline{BUSY}$ Floating	t_{CD_B}	3			μs	$C_{LOAD} = 50$ pF
SYNC Load Capacitance	C_{LOAD_S}			100	pF	

CLOCK WAVEFORM



SERIAL INTERFACE
TIMING WAVEFORMS



5 X 7 CHARACTER SET
AS GENERATED IN μPD7227

Display Byte

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								1	1	0	0
								0	1	0	1
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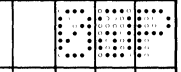
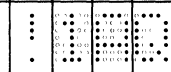
				0	0	0	0				
				0	0	0	1				
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				0	0	1	1				
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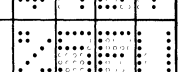
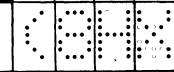
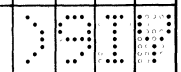
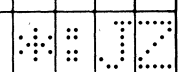
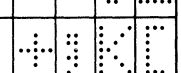
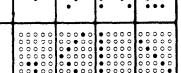
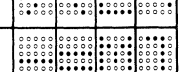
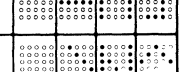
				0	1	0	1				
				0	1	1	0				
				0	1	1	1				

Display Byte

								0	0	1	1
								1	1	0	0
								0	1	0	1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0				
				1	0	0	0				
				1	0	0	1				
				1	0	1	0				
				1	0	1	1				
				1	1	0	0				
				1	1	0	1				
				1	1	1	0				
				1	1	1	1				

6

Package Outlines

For information, see Package Outline Section 7.

Plastic Miniflat, μPD7227G

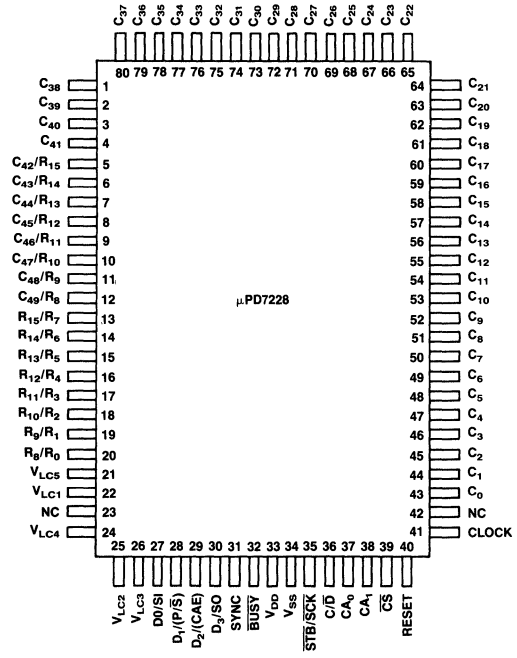
Description

The μPD7228 Intelligent Dot-Matrix LCD Controller/Driver is a peripheral device designed to interface most microprocessors with a wide variety of dot-matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows x 50 columns or 16 rows by 42 columns. The μPD7228 has a standby function to conserve power. It is equipped with several logic blocks, such as an 8-bit serial interface, a 4-bit parallel interface, an ASCII upper/lower case, a Kana character generator, a 50 x 16 static RAM with full read/write capability, and an LCD timing controller, all of which reduce microprocessor system software requirements. The μPD7228 is manufactured with a single 5V CMOS process, and is available in an 80-pin space saving flat plastic package.

Features

- ☐ LCD direct drive
- ☐ 8-line or 16-line multiplexing drive possible with single chip
  - 8-line multiplexing: 400 (50 x 8) dots
  - 16-line multiplexing: 672 (42 x 16) dots
- ☐ 8-line or 16-line multiplexing drive with *n* chip configuration
  - 8-line multiplexing: *n* x 400 (*n* x 50 x 8) dots
  - 16-line multiplexing: *n* x 800 (*n* x 50 x 16) dots
- ☐ RAM: 2 x 50 x 8 bits for display data storage
- ☐ Programmer designated dot (graphics) display
- ☐ 5 x 7 dot-matrix display by on-chip character generator ASCII characters (alphanumerics, others): 64 characters; JIS characters (Kana and others): 96 characters
- ☐ Cursor operating command
- ☐ 8-bit serial interface compatible with μPD7500, μCOM-43N, μCOM-87/87LC
- ☐ 4-bit parallel interface compatible with μPD7500, μCOM-84/84C
- ☐ Standby function
- ☐ CMOS
- ☐ Single power supply
- ☐ 80-pin plastic flat package
- ☐ Extended −40°C to +85°C temperature range available

Pin Configuration

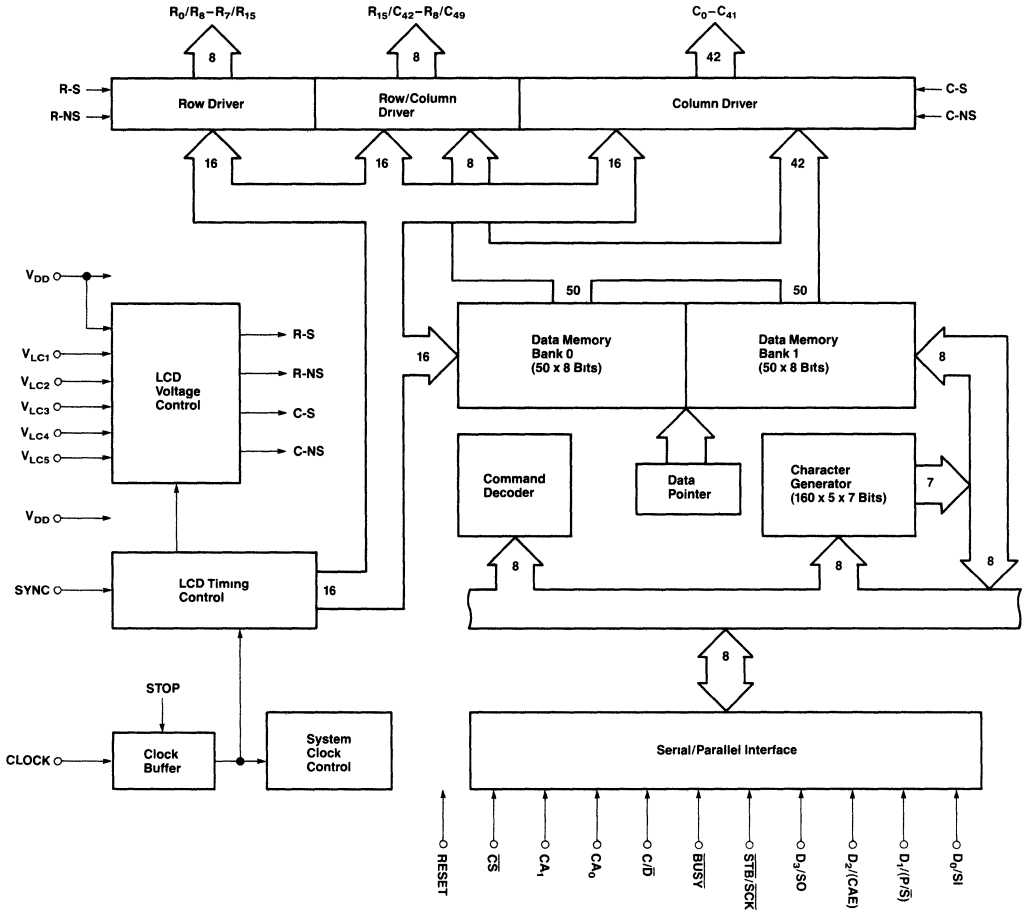


Pin Identification

Pin No.	Symbol	Description
1–18 42–80	C_0–C_{41}	LCD Column Drive Outputs
5–12	C_{42}/R_{15}–C_{49}/R_8	LCD Row/Column Drive Outputs
13–20	R_0/R_8–R_7/R_{15}	LCD Row Drive Outputs
21, 22 24–26	V_{LC1}–V_{LC5}	LCD Power Supply
23, 42	NC	No Connection
27	D_0/SI	Data Bus 0/Serial Input
28	D_1(P/$\overline{S}$)	Data Bus 1 (Parallel/Serial Select)
29	D_2(CAE)	Data Bus 2 (Chip Address Enable)
30	D_3/SO	Data Bus 3/Serial Output
31	SYNC	Synchronization Signal Input/Output
32	$\overline{BUSY}$	Busy Signal Output
33	V_{DD}	Power Supply
34	V_{SS}	Ground
35	$\overline{STB}$/$\overline{SCK}$	Strobe/Serial Clock Input
36	C/$\overline{D}$	Command/Data Select Input
37, 38	CA_0, CA_1	Chip Address Select Inputs
39	$\overline{CS}$	Chip Select Input
40	RESET	Reset Signal Input
41	CLOCK	System Clock Input

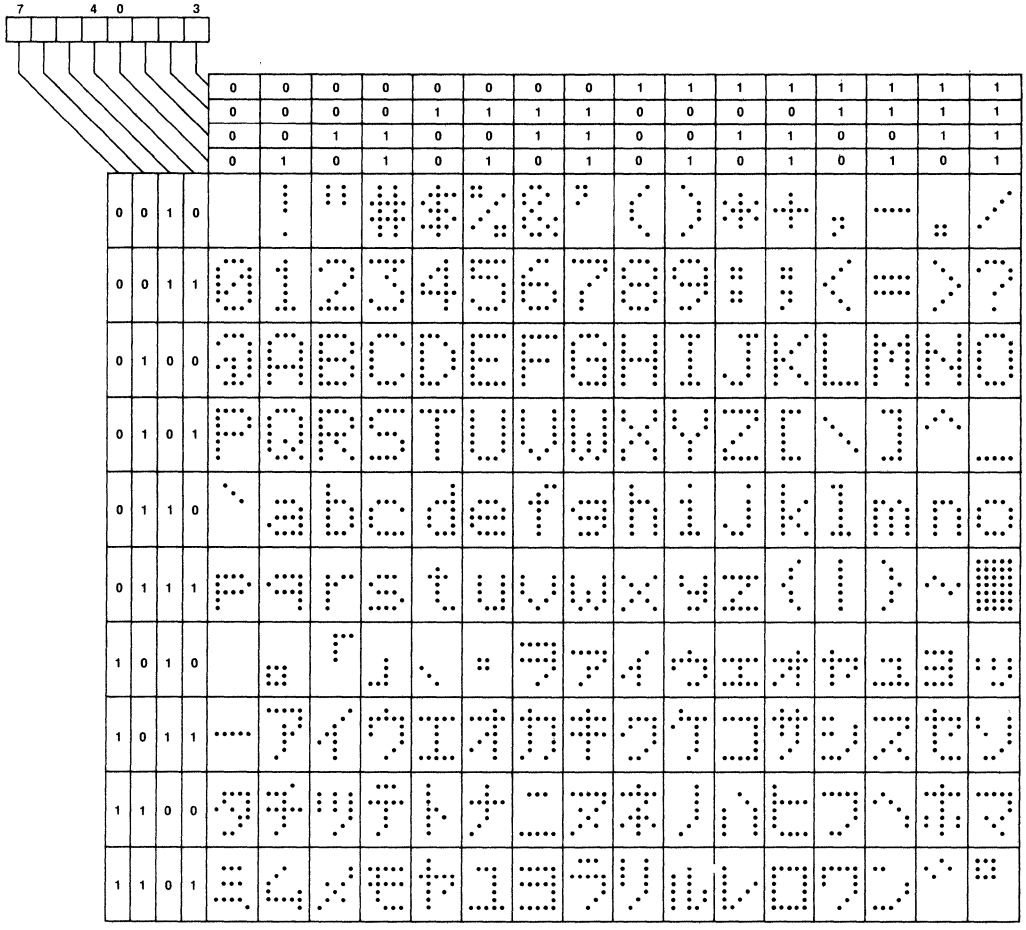
6

Block Diagram



Character Code

Character Codes and Display Patterns



Commands for μPD7228

The μPD7228 is provided with sixteen types of commands, each command consisting of one byte (8 bits).

Command Summary

1. Set Frame Frequency	0	0	0	1	0	F2	F1	F0
2. Set Multiplexing Mode	0	0	0	1	1	M2	M1	M0
3. Display Off	0	0	0	0	1	0	0	0
4. Display On	0	0	0	0	1	0	0	1
5. Set Read Mode	0	1	1	0	0	0	I1	I0
6. Set Write Mode	0	1	1	0	0	1	I1	I0
7. Set AND Mode	0	1	1	0	1	1	I1	I0
8. Set OR Mode	0	1	1	0	1	0	I1	I0
9. Set Character Mode with Right Entry	0	1	1	1	0	0	1	1
10. *Set Character Mode with Left Entry*	0	1	1	1	0	0	0	0
11. Bit Set	0	1	0	B2	B1	B0	J1	J0
12. Bit Reset	0	0	1	B2	B1	B0	J1	J0
13. *Write Cursor*	0	1	1	1	1	1	0	1
14. *Clear Cursor*	0	1	1	1	1	1	0	0
15. Load Immediate to Data Pointer	1	D6	D5	D4	D3	D2	D1	D0
16. *Set Stop Mode*	0	0	0	0	0	0	0	1

Note: *Newly added (compared to μPD7227)

Command Summary

Mnemonic	Operation	Instruction Code Binary D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
SFF	Set Frame Frequency	0	0	0	1	0	D_2	D_1	D_0	10-14
SMM	Set Multiplexing Mode	0	0	0	1	1	D_2	D_1	D_0	18-1F
DISP OFF	Display Off	0	0	0	0	0	0	0	0	08
DISP ON	Display On	0	0	0	0	1	0	0	1	09
LDPI	Load Data Pointer with Immediate	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80-B1 C0-F1
SRM	Set Read Mode	0	1	1	0	0	0	D_1	D_0	60-63
SWM	Set Write Mode	0	1	1	0	0	1	D_1	D_0	64-67
SORM	Set OR Mode	0	1	1	0	1	0	D_1	D_0	68-6B
SANDM	Set AND Mode	0	1	1	0	1	1	D_1	D_0	6C-6F
SCML	Set Character Mode with Left Entry	0	1	1	1	0	0	0	1	71
SCMR	Set Character Mode with Right Entry	0	1	1	1	0	0	1	0	72
BSET	Bit Set	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
BRESET	Bit Reset	0	0	1	D_4	D_3	D_2	D_1	D_0	20-3F
WRCURS	Write Cursor	0	1	1	1	1	1	0	1	7D
CLCURS	Clear Cursor	0	1	1	1	1	1	0	0	7C
STOP	Set Stop Mode	0	0	0	0	0	0	0	1	01

Electrical Specifications

Absolute Maximum Ratings*

T_a = 25°C	
Supply Voltage, V_{DD}	−0.3V to +7.0V
Input Voltage, V_I	−0.3V to V_{DD} + 0.3V
Output Voltage, V_O	−0.3V to V_{DD} + 0.3V
Operating Temperature, T_{OPT}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_a = 25°C; V_{DD} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			10	pF	f = 1MHz
Output Capacitance	C_{OUT}			25	pF	Unmeasured pins returned to 0V
I/O Capacitance	C_{IO}			15	pF	

DC Characteristics

T_a = −10°C to +70°C; V_{DD} = +5V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Voltage High	V_{IH1}	0.7V_{DD}		V_{DD}	V	Except $\overline{SCK}$
	V_{IH2}	0.8V_{DD}		V_{DD}	V	$\overline{SCK}$
Input Voltage Low	V_{IL}	0		0.3V_{DD}	V	
Input Leakage Current High	I_{LIH}			10	μA	V_I = V_{DD}
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Voltage High	V_{OH1}	V_{DD} − 0.5			V	$\overline{BUSY}$, D_0–D_3, I_{OH} = −400μA
	V_{OH2}	V_{DD} − 0.5			V	SYNC, I_{OH} = −100μA
Output Voltage Low	V_{OL1}			0.45	V	$\overline{BUSY}$, D_0–D_3, I_{OL} = 1.7mA
	V_{OL2}			0.45	V	SYNC, I_{OL} = 100μA
Output Leakage Current High	I_{LOH}			10	μA	V_O = V_{DD}
Output Leakage Current Low	I_{LOL}			−10	μA	V_I = 0V
LCD Operating Voltage	V_{LCD}	3.0		V_{DD}	V	
Row Output Impedance	R_{ROW}		4	8	kΩ	
Row/Column Output Impedance	$R_{ROW/COL}$		5	10	kΩ	
Column Output Impedance	R_{COL}		10	15	kΩ	
Supply Current	I_{DD1}		200	400	μA	Operating Mode, f_C = 400kHz
	I_{DD2}			20	μA	Stop Mode, CLK = 0V

AC Characteristics

T_a = −10°C to +70°C; V_{DD} = +5V ± 10%

Common Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock Frequency	f_C	100		1100	kHz	
Clock Pulse Width High	t_{WHC}	350			ns	
Clock Pulse Width Low	t_{WLC}	350			ns	
$\overline{BUSY}$ Delay Time from $\overline{CS}$ ↓	t_{DCSB}			2	μs	C_L = 50pF
$\overline{CS}$ ↑ Delay Time to $\overline{BUSY}$ Floating	t_{DCSBF}			4	μs	C_L = 50pF
$\overline{CS}$ High Level Time	t_{WHCS}	4			μs	
SYNC Load Capacitance	C_{LSY}			100	pF	
Data Set-up Time to RESET ↓	t_{SDR}	0			μs	
Data Hold Time from RESET ↓	t_{HRD}	4			μs	

AC Characteristics (Cont.)

T_a = −10°C to +70°C; V_{DD} = +5V ± 10%
Serial Interface Operation

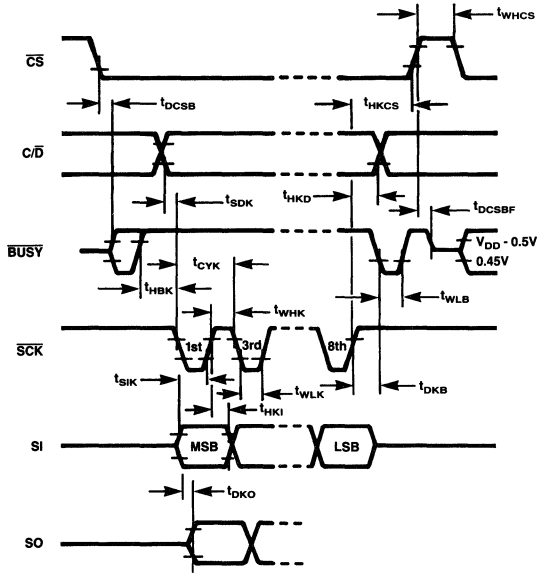
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ Cycle	t_{CYK}	0.9			μs	
$\overline{SCK}$ Pulse Width High	t_{WHK}	400			ns	
$\overline{SCK}$ Pulse Width Low	t_{WLK}	400			ns	
$\overline{SCK}$ Hold Time from $\overline{BUSY}$ ↑	t_{HBK}	0			ns	
SI Set-up Time to $\overline{SCK}$ ↑	t_{SIK}	100			ns	
SI Hold Time from $\overline{SCK}$ ↑	t_{HKI}	250			ns	
SO Delay Time from $\overline{SCK}$ ↓	t_{DKO}			320	ns	C_L = 50pF
$\overline{BUSY}$ Delay Time from Eighth $\overline{SCK}$ ↑	t_{DKB}			3	μs	C_L = 50pF
$\overline{BUSY}$ Low-level Time	t_{WLB}	18		64	$1/f_C$	C_L = 50pF
C/$\overline{D}$ Set-up Time to First $\overline{SCK}$ ↓	t_{SDK}	0			μs	
C/$\overline{D}$ Hold Time from Eighth $\overline{SCK}$ ↑	t_{HKD}	2			μs	
$\overline{CS}$ Hold Time from Eighth $\overline{SCK}$ ↑	t_{HKCS}	2			μs	

AC Characteristics (Cont.)

T_a = −10°C to +70°C; V_{DD} = +5V ± 10%
Parallel Interface Operation

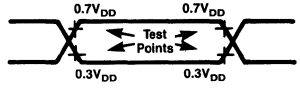
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Command Set-up Time to $\overline{STB}$ ↓	t_A	100			ns	C_L = 80pF
Input Command Hold Time from $\overline{STB}$ ↓	t_B	90			ns	C_L = 20pF
Input Data Set-up Time to $\overline{STB}$ ↑	t_C	230			ns	C_L = 80pF
Input Data Hold Time from $\overline{STB}$ ↑	t_D	50			ns	C_L = 20pF
Output Data Delay Time	t_{ACC}	90		650	ns	C_L = 80pF
Output Data Hold Time	t_H	0		150	ns	C_L = 20pF
$\overline{STB}$ Pulse Width Low	t_{SL}	700			ns	
$\overline{STB}$ High Level Time	t_{SH}	1			μs	
$\overline{STB}$ Hold Time from $\overline{BUSY}$ ↑	t_{HBS}	0			μs	
$\overline{BUSY}$ Delay Time from Second $\overline{STB}$ ↑	t_{DSB}			3	μs	
C/$\overline{D}$ Set-up Time to First $\overline{STB}$ ↓	t_{SDS}	0			μs	
C/$\overline{D}$ Hold Time from Second $\overline{STB}$ ↑	t_{HSD}	2			μs	
$\overline{CS}$ Hold Time from Second $\overline{STB}$ ↑	t_{HSCS}	2			μs	

Serial Interface Timing Waveforms

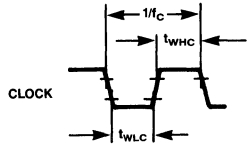


Serial Interface Timing Waveforms (Cont.)

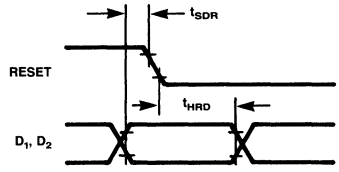
AC Test Points



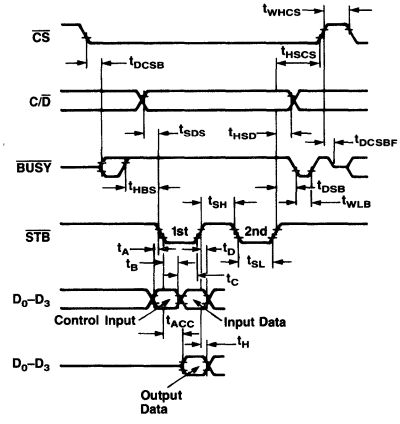
Clock Waveform



Interface Timing Waveforms



Parallel Interface Timing Waveforms



Package Outlines

For information, see Package Outline Section 7.

Plastic Miniflat, μPD7228G

Notes

PRELIMINARY

μPD7261
HARD-DISK CONTROLLER

Description

The μPD7261 hard-disk controller is an intelligent microprocessor peripheral designed to control a number of different types of disk drives. It is capable of supporting either hard-sector or soft-sector disks and provides all control signals that interface the controller with either SMD disk interfaces or Seagate floppy-like drives. Its sophisticated instruction set minimizes the software overhead for the host microprocessor. By using the DMA controller, the microprocessor needs only to load a few command bytes into the μPD7261 and all the data transfers associated with read, write, or format operations are done by the μPD7261 and the DMA controller. Extensive error reporting, verify commands, ECC, and CRC data error checking assure reliable controller operation. The μPD7261 provides internal address mark detection, ID verification, and CRC or ECC checking and verification. An eight-byte FIFO is used for loading command parameters and obtaining command results. This makes the structuring of software drivers a simple task. The FIFO is also used for buffering data during DMA read/write operations.

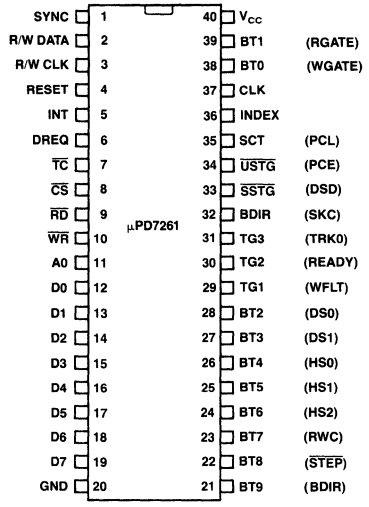
Features

- ☐ Flexible interface to various types of hard-disk drives
- ☐ Programmable track format
- ☐ Controls up to 8 drives
- ☐ Parallel seek operation capability
- ☐ Multisector and multitrack transfer capability
- ☐ Data scan and data verify capability
- ☐ High-level commands, including:

READ DATA	SEEK (normal or buffered)
READ ID	RECALIBRATE (normal or buffered)
WRITE DATA	READ DIAGNOSTIC (SMD only)
FORMAT	SPECIFY
SCAN DATA	SENSE INTERRUPT STATUS
VERIFY DATA	SENSE UNIT STATUS
VERIFY ID	DETECT ERROR
CHECK	

- ☐ NRZ or MFM data format
- ☐ Maximum data transfer rate: 12MHz (SMD mode)
- ☐ Error detection and correction capability
- ☐ Simple I/O structure: compatible with most microprocessors
- ☐ All inputs and outputs except clock pins are TTL-compatible (clock pins require pullup)
- ☐ Single +5V power supply
- ☐ 40-pin dual-in-line package

Pin Configuration



Note: Signals shown in parentheses are used when the μPD7261 is in the floppy-like mode.

Pin Identification — Host Interface Pins

Pin No.	Pin Name	I/O	Function
4	RESET	I	Reset input. When high, it forces the device into an idle state. The device remains idle until a command is issued by the system.
5	INT	O	Interrupt request to the system, set high for request.
6	DREQ	O	DMA request. Normally low, set high to request a transfer of data between the disk controller and memory.
7	$\overline{TC}$	I	This is used as a terminal count input during DMA.
8	$\overline{CS}$	I	Chip select. When low, it enables reading from or writing into the register selected by A0.
9	$\overline{RD}$	I	Read strobe. When low, selected register contents are read.
10	$\overline{WR}$	I	Write strobe. When low, data is written into the selected register.
11	A0	I	Register select input, to be connected to a non-multiplexed address bus line. When high, the command/status register is selected; when low, the data buffer is selected.
12-19	D0–D7	I/O	Data bus port, to be connected to data bus.
20	GND	P.S.	Ground.
36	INDEX	I	This signal indicates the beginning of sector zero.
37	CLOCK	I	External clock input, used as timing clock for the on-chip processor.
40	V_{CC}	P.S.	+5V power supply.

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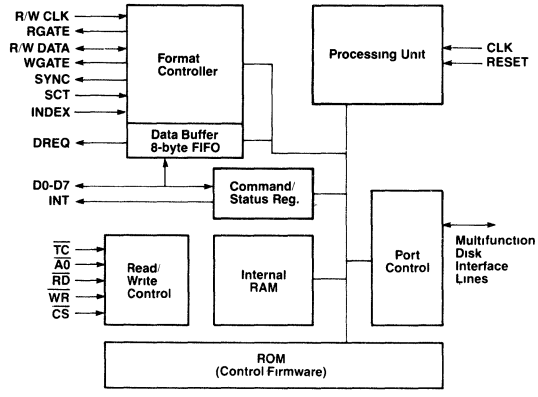
Disk Interface Pins (Defined by mode)

Pin No.	Pin Name	SMD	Floppy-like
1	SYNC	Read Clock Enable	PLO Lock/Read Clock Enable
2	R/W DATA	Read/Write Data	Read/Write Data
3	R/W CLK	Read Clock | Servo Clock	Read Clock | Write Clock
21	BT9, DIR	Bit 9 | Unit Selected	Direction In
22	BT8, −STEP	Bit 8 | Seek End	Step Pulse
23	BT7, RWC	Bit 7 | WR Protected | (SR7)	Reduced Write Current
24	BT6, HS2	Bit 6 | (AM Found) | (SR6)	Head Select 2^2
25	BT5, HS1	Bit 5 | Unit Ready | (SR5)	Head Select 2^1
26	BT4, HS0	Bit 4 | On Cylinder | (SR4)	Head Select 2^0
27	BT3, DS1	Bit 3 | Seek Error | (SR3)	Drive Select 2^1
28	BT2, DS0	Bit 2 | Fault | (SR2)	Drive Select 2^0
29	$\overline{TG1}$, WFLT	$\overline{Tag\ 1}$	Write Fault
30	$\overline{TG2}$, READY	$\overline{Tag\ 2}$	Ready
31	$\overline{TG3}$, TRK0	$\overline{Tag\ 3}$	Track 000
32	BDIR, SKC	Direction	Seek Complete
33	$\overline{SSTG}$, DSD	($\overline{SR\ Select\ Tag}$)	Drive Selected
34	$\overline{USTG}$, PCL	$\overline{Unit\ Select\ Tag}$	Precomp Late
35	SCT, PCE	Sector | (SR1)	Precomp Early
36	INDEX	Index | (SR0)	Index
38	BT0, WGATE	Bit 0	Write Gate
39	BT1, RGATE	Bit 1	Read Gate

Note: The multifunction signals above are defined by the use of the Specify command. By setting the SSEC bit in the mode byte of the Specify command to a one the floppy-like mode is selected. To better understand the functions of these pins, refer to the individual instructions and to the SMD and floppy-like interface definitions.

Block Diagram



DC Characteristics

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5	+0.8	V	All except CLK
Input Low Voltage	V_{IL1}	−0.5	+0.6	V	CLK
Input High Voltage	V_{IH}	+2.0	V_{CC}	V	All except CLK, RESET
Input High Voltage	V_{IH1}	+3.3	V_{CC}	V	CLK, RESET
Output Low Voltage	V_{OL}		+0.45	V	I_{OL} = +2.0mA DREQ, INT, D0–D7
Output Low Voltage	V_{OL1}		+0.45	V	I_{OL} = +1.6mA all except DREQ, INT, D0–D7
Output High Voltage	V_{OH}	+2.4		V	I_{OH} = −100μA DREQ, INT, D0–D7
Output High Voltage	V_{OH1}	+2.4		V	I_{OH} = −50μA all except DREQ, INT, D0–D7
Input Leakage Current	I_{IL}		±10	μA	V_{IN} = V_{CC} to 0.45, all except Pins 21–34
Input Leakage Current	I_{IL1}		±500	μA	V_{IN} = V_{CC} to 0.45 Pins 21–34
Output Leakage Current	I_{OL}		±10	μA	V_{OUT} = V_{CC} to 0.45
Input Capacitance	C_{IN}		15	pf	f = 1 MHz
Output Capacitance	C_{OUT}		15	pf	f = 1 MHz
I/O Capacitance	C_{IO}		20	pf	f = 1 MHz
Supply Current	I_{CC}		360	mA	V_{CC} = 5V ± 10% Ta = 0 to 70°C
Supply Voltage	V_{CC}	+4.5	5.5	V	Ta = 0 to 70°C

Absolute Maximum Ratings*

Operating Temperature	0°C	to	+70°C
Storage Temperature	−65°C	to	+150°C
Voltage on any Pin with Respect to Ground	−0.5V	to	+7.0V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics (Processor Interface)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
CLOCK Cycle	ϕ_{CY}	90		ns	
CLOCK Low Time	ϕ_{CH}	32		ns	
CLOCK High Time	ϕ_{CL}	32		ns	
CLOCK Rise Time	ϕ_R		10	ns	
CLOCK Fall Time	ϕ_F		10	ns	
A0, $\overline{CS}$ Setup to $\overline{RD}$	t_{AR}	0		ns	
A0, $\overline{CS}$ Hold from $\overline{RD}$	t_{RA}	0		ns	
$\overline{RD}$ Pulse Width	t_{RR}	200		ns	
Data Delay from $\overline{RD}$	t_{RD}		150	ns	
Output Float Delay	t_{DF}	0	100	ns	
Data Delay from A0, $\overline{CS}$	t_{AD}		150	ns	
A0, $\overline{CS}$ Setup to $\overline{WR}$	t_{AW}	0		ns	
A0, $\overline{CS}$ Hold from $\overline{WR}$	t_{WA}	0		ns	
$\overline{WR}$ Pulse Width	t_{WW}	200		ns	
Data Setup to $\overline{WR}$	t_{DW}	100		ns	
Data Hold from $\overline{WR}$	t_{WD}	0		ns	
Recovery Time from $\overline{RD}$, $\overline{WR}$	t_{RV}	200		ns	
RESET Pulse Width	t_{RST}	100		ϕCY	
$\overline{TC}$ Pulse Width	t_{TC}	100		ns	
INT Delay from $\overline{WR}$	t_{WI}		200	ns	
DREQ Delay from $\overline{WR}$	t_{WAI}		250	ns	
DREQ Delay from RD1	t_{RAI1}		250	ns	
DREQ Delay from RD2	t_{RAI2}		150	ns	

AC Characteristics (Floppy-like Interface)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
R/WCLK Cycle Period	t_{CY}	83		ns	
R/WCLK Low Time	t_{CL}	30		ns	
R/WCLK High Time	t_{CH}	30		ns	
R/WCLK Rise Time	t_R		10	ns	
R/WCLK Fall Time	t_F		10	ns	
R/WDATA Set up to R/WCLK	t_{DCS}	40		ns	
R/WDATA Hold from R/WCLK	t_{CDH}	0		ns	
R/WDATA Delay from R/WCLK	t_{DCD}		70	ns	
RGATE Delay from R/WCLK	t_{CRG}		300	ns	
WGATE Delay from R/WCLK	t_{CWG}		150	ns	
PCE/PCL Delay from R/WCLK	t_{CPC}		70	ns	
SYNC Delay from R/WCLK	t_{CSY}		150	ns	
DS0, DS1 Set up to $\overline{STEP}$	t_{DSST}	250		ϕ_{CY}	Normal Seek Mode
DIR Set up to $\overline{STEP}$	t_{DIST}	200		ϕ_{CY}	
$\overline{STEP}$ Pulse Width	t_{STP}	69	85	ϕ_{CY}	
DS0, DS1 Hold from $\overline{STEP}$	t_{STDS}	750		ϕ_{CY}①	
DIR Hold from $\overline{STEP}$	t_{STDI}	750		ϕ_{CY}①	
DS0, DS1 Hold from SKC	t_{SKDS}	100		ϕ_{CY}②	
DIR Hold from SKC	t_{SKDI}	100		ϕ_{CY}②	
DS0, DS1 Set up to $\overline{STEP}$	t_{DSSTB}	250		ϕ_{CY}	Buffered Seek Mode
DIR Set up to $\overline{STEP}$	t_{DIST3}	200		ϕ_{CY}	
$\overline{STEP}$ Pulse Width	t_{STPB}	69	85	ϕ_{CY}	
$\overline{STEP}$ Cycle Period	t_{STCB}	570	795	ϕ_{CY}	
DS0, DS1 Hold from $\overline{STEP}$	t_{STDSB}	200		ϕ_{CY}①	
DIR Hold from $\overline{STEP}$	t_{STDIB}	200		ϕ_{CY}①	
DS0, DS1 Hold from SKC	t_{SKDSB}	100		ϕ_{CY}②	
DIR Hold from SKC	t_{SKDIB}	100		ϕ_{CY}②	

Note: ① Polling mode ② Nonpolling

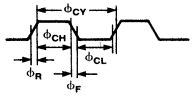
AC Characteristics (SMD Interface)

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

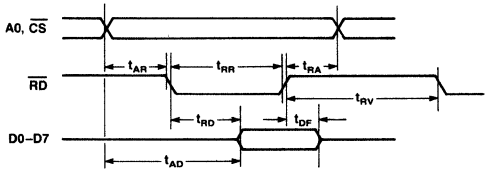
Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
R/WCLK Cycle Period	t_{CY}	83		ns	
R/WCLK Low Time	t_{CL}	30		ns	
R/WCLK High Time	t_{CH}	30		ns	
R/WCLK Rise Time	t_R		10	ns	
R/WCLK Fall Time	t_F		10	ns	
R/WDATA Set up to R/WCLK	t_{DCS}	40		ns	
R/WDATA Hold from R/WCLK	t_{CDH}	0		ns	
R/WDATA Delay from R/WCLK	t_{DCD}		70	ns	
RGATE Delay from R/WCLK	t_{CRG}		300	ns	
WGATE Delay from R/WCLK	t_{CWG}		150	ns	
SYNC Delay from R/WCLK	t_{CSY}		150	ns	
BDIR Set up to USTG	t_{BDUT}	60		ϕ_{CY}	
BDIR Hold from USTG	t_{UTBD}	15		ϕ_{CY}	Unit Select Operation
UNIT ADR Set up to USTG	t_{UAUT}	20	40	ϕ_{CY}	
UNIT ADR Hold from USTG	t_{UTUA}	15		ϕ_{CY}	
BDIR Set up to TAG1	t_{BDT1}	27	48	ϕ_{CY}	
BDIR Hold from TAG1	t_{T1BD}	60		ϕ_{CY}	
CYL. ADR Set up to TAG1	t_{CAT1}	27	48	ϕ_{CY}	Cylinder Select Operation
CYL. ADR Hold from TAG1	t_{T1CA}	60		ϕ_{CY}	
TAG1 Pulse Width	t_{TAG1}	24	36	ϕ_{CY}	
BDIR Set up to TAG2	t_{BDT2}	15		ϕ_{CY}	
BDIR Hold from TAG2	t_{T2BD}	70		ϕ_{CY}	
HEAD ADR Set up TAG2	t_{HAT2}	15	70	ϕ_{CY}	Head Select Operation
HEAD ADR Hold from TAG2	t_{T2HA}	70		ϕ_{CY}	
TAG2, Pulse Width	t_{TAG2}	24	36	ϕ_{CY}	
BDIR Set up to TAG3	t_{BDT3}	24		ϕ_{CY}	RTZ,
BDIR Hold from TAG3	t_{T3BD}	24	36	ϕ_{CY}	FAULT CLR.,
BT DATA Set up to TAG3	t_{BTT3}		56	ϕ_{CY}	SERVO,
RTZ/FLIRST Hold from TAG3	t_{T3RBT}	24		ϕ_{CY}	DATA STB.
TAG3 Pulse Width	t_{TAG3}	56	66	ϕ_{CY}	Control
DATA STB./SERVO OFF. Hold from TAG3	t_{T3RBT}	75		ϕ_{CY}	Timing
BDIR Delay from SSTG	t_{STBD}	24		ϕ_{CY}	
BDIR High Time	t_{BDIR}	54	66	ϕ_{CY}	Sense
BT9 Set up to BDIR	t_{B9BD}	24	36	ϕ_{CY}	Unit
BT9 Hold from BDIR	t_{BDB9}	24	33	ϕ_{CY}	Status
SSTG Pulse Width	t_{SSTG}		200	ϕ_{CY}	Timing

Timing Waveforms Host System Interface

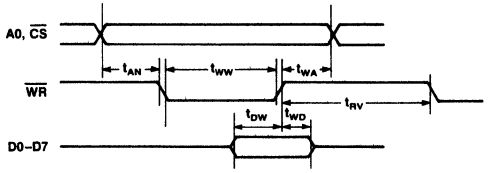
Clock



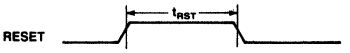
Read Operation



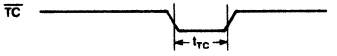
Write Operation



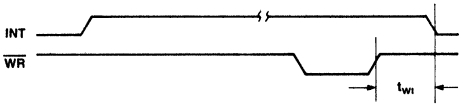
Reset



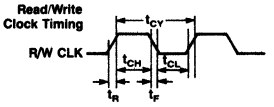
Terminal Count



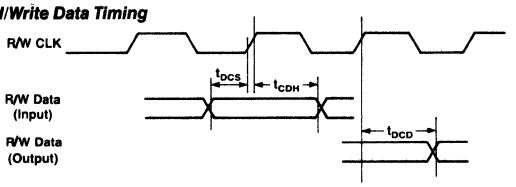
Interrupt



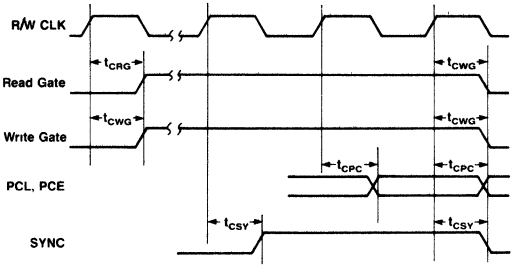
Drive Interface



Read/Write Data Timing



Read/Write Operation

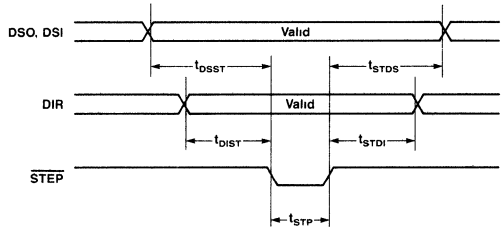


6

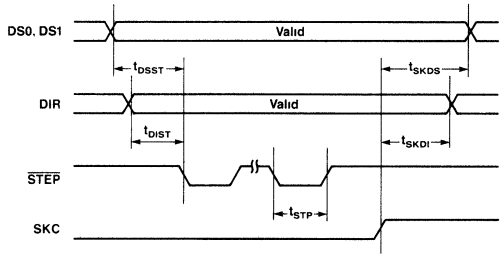
Timing Waveforms (Cont.)

Normal Seek (Floppy-like) Operation

Polling Mode

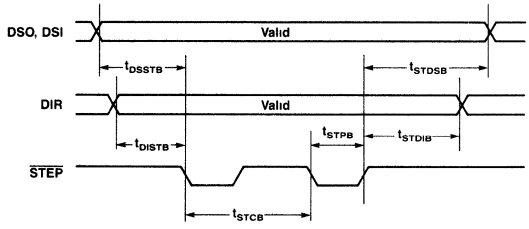


Nonpolling Mode

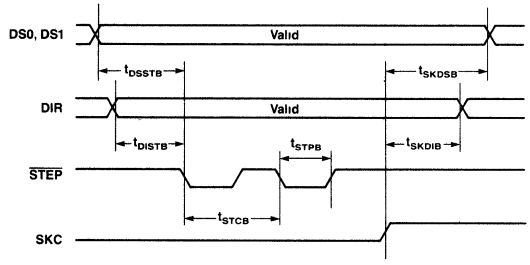


Buffered Seek (Floppy-like) Operation

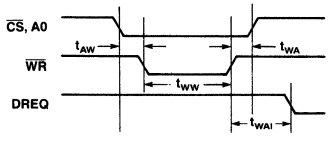
Polling Mode



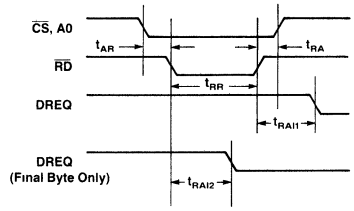
Nonpolling Mode



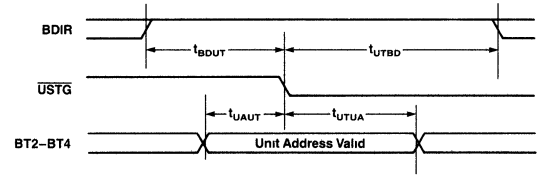
DMA Timing: Write Operation



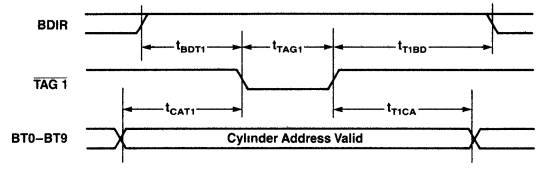
DMA Timing: Read Operation



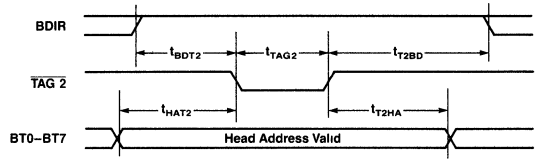
Unit Select Operations (SMD Interface)



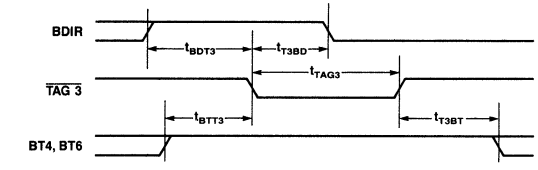
Cylinder Select (SEEK) Operation (SMD Interface)



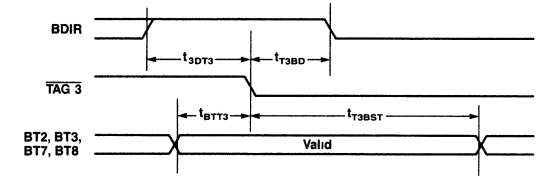
Head Select Operation (SMD Interface)



RTZ/Fault Clear Operation (SMD Interface)

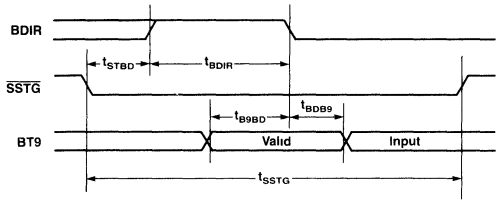


Data Strobe/Servo Offset Control Timing (SMD Interface)



Timing Waveforms (Cont.)

Sense Unit Status Operation (SMD Interface)



High-level Commands

SPECIFY

Allows user to select SMD or floppy-like mode data block length, ending track number, end sector number, gap length, track at which write current is reduced, ECC or CRC function, choice of polynomial, and polling mode enable.

SENSE INTERRUPT STATUS

When a change of disk status occurs, the HDC will interrupt the host CPU. This command will reveal the cause of interrupt, such as seek end, disk ready change, seek error, or equipment check. The disk unit address is also supplied.

SENSE UNIT STATUS

The host CPU specifies the drive numbers and the HDC will return information such as write fault, ready, track 000, seek complete and drive selected, or for SMD units fault, seek error, on cylinder, unit ready, AM found, write protected, seek end and unit selected.

DETECT ERROR

Used after a read operation where ECC has been employed. The detect error command supplies the information needed to allow the host CPU to execute an error correction routine. (Only allowed when an actual correctable error is detected by the HDC.)

RECALIBRATE

Returns the disk drive heads to the home position or track 000 position. Has four modes of operation: SMD, normal, buffered, or nonpolling.

SEEK

Moves the disk drive heads to the specified cylinder. As in recalibrate, seek has four modes of operation.

FORMAT

This command is used to initialize the medium with the desired format which includes various gap lengths, data patterns, and CRC codes. This command is used in conjunction with the specify command.

VERIFY ID

Used to verify the ID bytes with data from memory. Performs the operation over a specified number of sectors.

READ ID

Used to verify the position of the read/write heads.

READ DIAGNOSTIC

Used in SMD mode only, the command allows the programmer to read a sector of data even if the ID portion of the sector is defective. Only one sector at a time can be read.

READ DATA

Reads and transfers to the system memory the number of sectors specified. The HDC can read multiple sectors and multiple tracks with one instruction.

SCAN

Compares a specified block of memory with specified sectors on the disk. The 7261 continues until a sector with matching data is found, until the sector count reaches zero, or the end of the cylinder is reached.

VERIFY DATA

Makes a sector-by-sector comparison of data in the system memory by DMA transfer. As in read operation, multiple sectors and tracks may be verified with this command.

WRITE DATA

Data from the system memory, transferred by DMA, is written onto the specified disk unit. As in the read command, data may be written onto successive sectors and tracks.

AUXILIARY COMMAND

Allows four additional functions to be executed: software reset, clear data buffer, mask interrupt request bit (masks interrupts caused by change of status of drives), and reset interrupt caused by command termination (used when no further disk commands will be issued, which would normally reset the interrupt).

Command Operation

There are three phases for most of the instructions that the μPD7261 can execute: Command Phase, Execution Phase, and Result Phase. During the command phase the host CPU loads preset parameters into the μPD7261 FIFO via the data bus and by successive write pulses to the part with A0 and $\overline{CS}$ true low. Once the required parameter bytes are loaded the appropriate command is initiated by issuing a write pulse with A0 high and $\overline{CS}$ low and the command code on the data bus.

The μPD7261 is now in the execution phase. This can be verified by examining the status register bit 7 (the controller busy bit). The execution phase is ended when a normal termination or an abnormal termination occurs. An abnormal termination can occur due to a read or write error, or a change of status in the addressed disk drive. A normal termination occurs when the command given is correctly completed. (This is indicated by bits in the status register.) The result phase is then entered. The host CPU may read various result parameters from the FIFO. These result parameters may be useful in determining the cause of an interrupt, or the location of a sector causing a read error, for example.

The chart shown on this page illustrates the preset parameters and result parameters that are associated with each command. The abbreviations are defined below.

Preset Parameters and Result Status Bytes

Disk Command	Command Code	Preset Parameters/Result Status							
		1st	2nd	3rd	4th	5th	6th	7th	8th
DETECT ERROR	0100X	EADH	EADL	EPT1	EPT2	EPT3			
RECALIBRATE	0101[B]	IST*							
SEEK	0110[B]	PCNH	PCNL						
		IST*							
FORMAT WRITE	0111(S)	PHN	(PSN)	SCNT	DPAT	GPL1	[GPL3]		
		EST	SCNT						

Preset Parameters and Result Status Bytes (Cont.)

Disk Command	Command Code	Preset Parameters/Result Status							
		1st	2nd	3rd	4th	5th	6th	7th	8th
VERIFY ID	1000(S)	PHN	(PSN)	SCNT					
		EST	SCNT						
READ ID	1001(S)	PHN	(PSN)	SCNT					
		EST	SCNT						
(READ DIAG-NOSTIC)	1010X	PHN	PSN						
		EST							
READ DATA	1011X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
CHECK	1100X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
SCAN	1101X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
VERIFY DATA	1110X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
WRITE DATA	1111X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
		EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
SENSE INTERRUPT STATUS	0001X								
		IST							
SPECIFY	0010X	MODE	DTLH	DTLL	ETN	ESN	GPL2	(MGPL1) [RWCL] [RWCH]	
SENSE UNIT STATUS	0011X								
		UST							

Note: ( ) These are omitted for soft-sector disks
[ ] These are omitted for hard-sector disks
* IST available as a result byte only when in nonpolling mode
B Indicates buffered mode when set
S Indicates skewed mode (SMD only) when set
X Indicates don't care

Mnemonic Definitions

EADH	Error Address, High Byte
EADL	Error Address, Low Byte
EPT1	Error Pattern, Byte One
EPT2	Error Pattern, Byte Two
EPT3	Error Pattern, Byte Three
PCNH	Physical Cylinder Number, High Byte
PCNL	Physical Cylinder Number, Low Byte
PHN	Physical Head Number
PSN	Physical Sector Number
SCNT	Sector Count
DPAT	Data Pattern
GPL1	Gap Length One
GPL3	Gap Length Three
EST	Error Status Byte
FLAG	Flag Byte
LCNH	Logical Cylinder Number, High Byte
LCNL	Logical Cylinder Number, Low Byte
LHN	Logical Head Number
LSN	Logical Sector Number
IST	Interrupt Status Byte
MODE	Mode
DTLH	Data Length, High Byte
DTLL	Data Length, Low Byte
ETN	Ending Track Number
ESN	Ending Sector Number
GPL2	Gap Length Two
RWCL	Write Current Cylinder, Low Byte
RWCH	Write Current Cylinder, High Byte
UST	Unit Status Byte
MGPL1	Modified Gap Length 1

Status Register

This register is a read only register and may be read by asserting $\overline{RD}$ and $\overline{CS}$ with A0 high. The status register may be read at any time. It is used to determine controller status and partial result status.

Bit No.	Bit Name	Bit Symbol	Description
D7	Controller Busy	CB	Set by a disk command issue. Cleared when the command is completed. (This bit is also set by an external reset signal or an RST command, but will be cleared at the completion of the reset function.) When this bit is set, a new disk command will not be accepted.
D6 D5	Command End	CEH CEL	CEH = 0 and CEL = 0 A disk command is in process, or no disk command is issued after the last reset signal or the last CLCE auxiliary command. Both the CEH and CEL bits are cleared by a disk command, a CLCE auxiliary command, or a reset signal.
			CEH = 0 and CEL = 1 Abnormal termination of a disk command. Execution of a disk command was started, but was not successfully completed.
			CEH = 1 and CEL = 0 Normal termination of a disk command. The execution of a disk command was completed and properly executed.
			CEH = 1 and CEL = 1 Invalid command issue.
D4	Sense Interrupt Status Request	SRQ	When a seek end, an equipment check condition, or a ready signal state change is detected, this bit is set requesting a sense interrupt status command be issued to take the detailed information. This bit is cleared by an issue of that command or by a reset signal.
D3	Reset Request	RRQ	Set when controller has lost control of the format controller (missing address mark, for example). An auxiliary RST command or another disk command will clear this bit.
D2	ID Error	IER	Set when a CRC error is detected in the ID field. An auxiliary RST or another disk command will reset this bit.
D1	Not Coincident	NCI	Set if the controller cannot find a sector on the cylinder which meets the comparison condition during the execution of a scan command. This bit is also set if data from the disk does not coincide with the data from the system during a verify ID or a verify data command. This bit is cleared by a disk command or a reset signal.
D0	Data Request	DRQ	During execution of write ID, verify ID, scan, verify data, or a write data command, this bit is set to request that data be written into the data buffer. During execution of read ID, read diagnostic, or read data command, this bit is set to request that data be read from the data buffer.

Error Status Byte

This byte is available to the host at the termination of a read, write, or data verification command and provides additional error information to the host CPU. If the status register indicates a normal command termination, it can be assumed that the command was executed without error and it is not necessary to read this byte. When it is necessary to determine the cause of an error this byte may be read by issuing an $\overline{RD}$ pulse with $\overline{CS}$ and A0 low. The remaining result bytes associated with a particular command may be read by issuing additional $\overline{RD}$ pulses. Data transfer from or to the FIFO is asynchronous and may occur at rates up to 2.5M bytes per second.

Bit No.	Bit Name	Bit Symbol	Description
D7	End of Cylinder	ENC	Set when the controller tries to access a sector beyond the final sector of a cylinder. Cleared by a disk command or an auxiliary RST command.
D6	Overrun	OVR	When set, indicates that the FIFO became full during a read operation, or empty during a write operation.
D5	Data Error	DER	A CRC or an ECC error was detected in the data field.
D4	Equipment Check	EQC	A fault signal from the drive has been detected or a track 0 signal has not been returned within a certain time interval after the recalibrate command was issued.
D3	Not Ready	NR	The drive is not in ready state.
D2	No Data	ND	The sector specified by ID parameters was not found on the track.
D1	Not Writable	NWR	Set if write protect signal is detected when the controller tries to write on the disk. It is cleared by a disk command or by an auxiliary RST command.
D0	Missing Data Mark	MDM	During execution of read data, check, scan, or verify data commands, no address mark was found in the data field.

Interrupt Status Byte

This byte is made available to the host CPU by executing the Sense Interrupt Status command. This command should be issued only when the μPD7261 requests it, as indicated by bit D4 of the status register. This byte reveals changes in disk drive status that have occurred.

Bit No.	Bit Name	Bit Symbol	Description
D7	Seek End	SEN	A seek end or seek complete signal has been returned after a seek or a recalibrate command was issued.
D6	Ready Change	RC	The state of the ready signal from the drives has changed. The state itself is indicated by the NR bit.
D5	Seek Error	SER	Seek error has been detected on seek end.
D4	Equipment Check	EQC	Identical to bit 4 of the error status byte.
D3	Not Ready	NR	Identical to bit 3 of the error status byte.
D2	Unit Address	UA2	The unit address of the drive which caused an interrupt request on any of the above conditions.
$\overline{D1}$		$\overline{UA1}$	
D0		UA0	

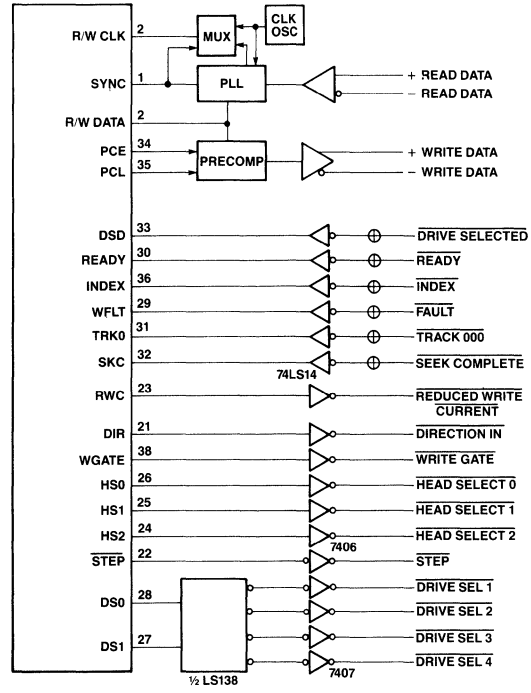
Drive Interface

The μPD7261 has been designed to implement two of the more popular types of interfaces: the SMD (Storage Module Drive) and the floppy-like Winchester drive which has come to be known as the ST-506 (Seagate Technology) interface. The desired interface mode is selected by the specify command.

Floppy-like Interface

In the floppy-like mode the μPD7261 performs MFM encoding and decoding at data rates to 6 MHz and provides all necessary drive interface signals. Included internally is circuitry for address mark detection, sync area recognition, serial-to-parallel-to-serial conversion, an 8-byte FIFO for data buffering, and circuitry for logical addressing of the drives. External circuitry required consists of control signal buffering, a delay network for precompensation, a phase lock loop, a write clock oscillator and a differential transceiver for drive data. The floppy-like interface can be implemented with as few as 12 to 14 additional SSI ICs.

μPD7261 Floppy-like Interface

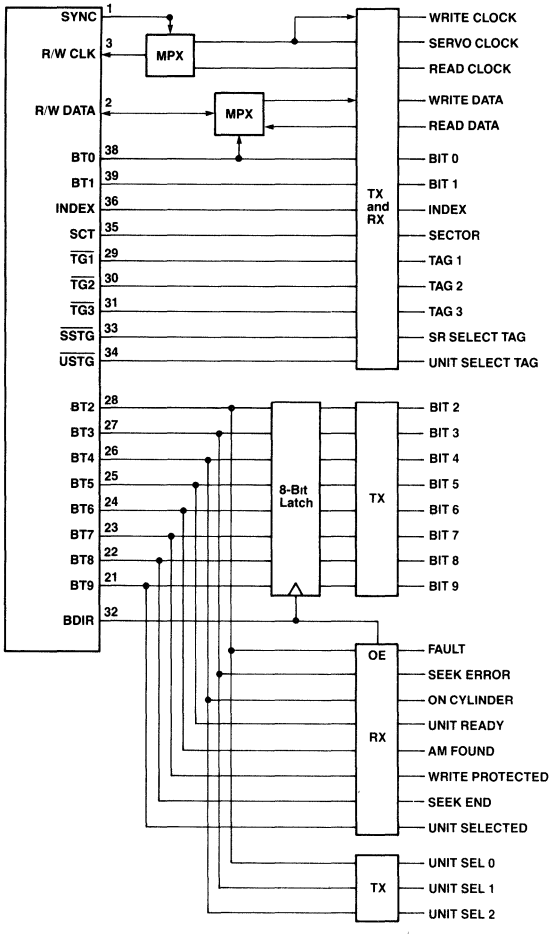


Note: ⊕ = 220Ω Pull-up/330Ω Pull-down terminator

SMD Interface

In the SMD mode the μPD7261 will support data rates to 12 MHz in the NRZ format. All control functions necessary for an SMD interface are implemented on-chip with de-multiplexing of 8 data lines performed externally by a single 8-bit latch. A small amount of logic is required to multiplex the data and clock lines, and differential drivers and receivers are required to implement the actual interface. Depending on individual logic design and the number of drives used, the SMD interface may be implemented with as few as 12 ICs.

μPD7261D SMD Interface



Note: TX and RX are differential drivers and receivers

Internal Architecture

The μPD7261 can be divided into three major internal logic blocks: command processor; format controller; microprocessor interface.

Command Processor

The command processor is an 8-bit microprocessor with its own instruction set, program ROM, scratchpad RAM, ALU, and I/O interface. Its major functions are:

- ☐ To decode the commands from the host microcomputer that are received through the 8-bit data bus;
- ☐ To execute seek and recalibrate commands;
- ☐ To interface to the drives and read the drive status lines;
- ☐ To load the format controller with the appropriate microcode, enabling it to execute the various read/write data commands.

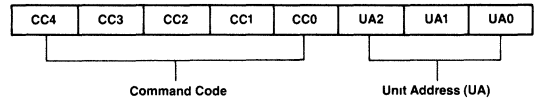
The command processor microprocessor is idle until it receives the command from the host microcomputer. It then reads the parameter bytes from the FIFO, and loads them into its RAM. The command byte is decoded and, depending on its opcode, the appropriate subroutine from the 2.5K-internal ROM is selected and executed. Some of these commands are executed by the command processor without involvement of the format controller. When data transfers to and from the disk are made, the command processor loads the appropriate microcode into the format controller, then relinquishes control. When the data transfer is complete, the command processor again takes control. One other important function that the command processor performs is managing the interface to the disk drives. The command processor contains an I/O port structure similar to many single chip microcomputers in that the ports may be configured as input or output pins. Depending on the mode of operation selected by the Specify command, the command processor will use the bidirectional I/O lines for different functions.

Command Register

This register is a write only register. It is selected when the A0 input is high and the $\overline{CS}$ input is low. There are two kinds of commands: disk commands and auxiliary commands. Each command format is shown below.

An auxiliary command is accepted at any time and is immediately executed, while a disk command is ignored if the on-chip processor is busy processing another disk command. A valid disk command causes the processor to begin execution using the parameters previously loaded into the data buffer. Disk commands and the parameters needed are described in the next section.

Disk Command Byte



CC4	CC3	CC2	CC1	CC0	
0	0	0	0	X	(Auxiliary Command)
0	0	0	1	X	SENSE INT. STATUS ①
0	0	1	0	X	SPECIFY ①
0	0	1	1	X	SENSE UNIT STATUS
0	1	0	0	X	DETECT ERROR ①
0	1	0	1	[B]	RECALIBRATE
0	1	1	0	[B]	SEEK
0	1	1	1	[S]	FORMAT
1	0	0	0	[S]	VERIFY ID
1	0	0	1	[S]	READ ID
1	0	1	0	X	READ DIAGNOSTIC
1	0	1	1	X	READ DATA
1	1	0	0	X	CHECK
1	1	0	1	X	SCAN
1	1	1	0	X	VERIFY DATA
1	1	1	1	X	WRITE DATA

Note: ① means the UA field is 000
[B] indicates buffered mode when set
[S] indicates skewed mode when set

Format Controller

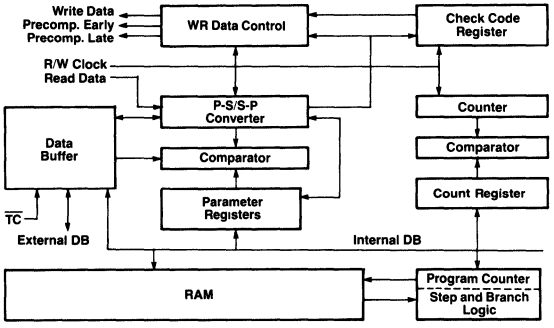
The format controller is built with logic that enables it to execute instructions at very high speed: one instruction per single clock cycle. The major functions it performs are:

- ☐ Serial-to-parallel and parallel-to-serial data conversion;
- ☐ CRC and ECC generation and checking;
- ☐ MFM data decoding and encoding;
- ☐ Write precompensation;

- ☐ Address mark detection and generation;
- ☐ ID field search in soft-sector format;
- ☐ DMA data transfer control during read/write operations.

The major blocks in the format controller are the sequencer and the serial/parallel data handler. The sequencer consists of a writable control store (32 words by 16 bits), a program counter, branch logic, and the parameter register. The serial/parallel logic consists of a parallel-to-serial converter for disk write operations, a serial-to-parallel converter for disk read operations, precompensation logic for writing MFM data, comparator logic that locates sync fields, address marks, and ID fields. There is also comparator logic that is used during Verify Data commands.

Block Diagram of the Format Controller



Microprocessor Interface

Read/Write Control

The internal registers are selected via the truth table shown.

Register Selection Table

$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	Selection
0	0	0	1	Data Buffer Register ①
0	0	1	0	
0	1	0	1	Status Register
0	1	1	0	Command Register
0	X	1	1	Don't Care
1	X	X	X	
0	X	0	0	Inhibited

Note: ① Preset parameters and result status information are written and read from the result status register in the HDC through this data buffer register

Interrupt

The interrupt request line is activated or inactivated according to the following equation:

$$INT = CEH + CEL + SRQ \cdot \overline{SRQM}$$

This means that if either of the command end bits is set or if the Sense Interrupt Status Request bit is set (and the SRQM mask is not set), then an interrupt will be generated. The command end bits, CEH and CEL, are set by command termination.

The SRQ bit is set when an equipment check condition or a state change of the ready signal from the disk drives is detected. It is also set when a seek operation is completed. Under these conditions the INT line is activated unless the SRQM mask is set.

Both of the CEH and CEL bits are cleared by a disk command, but both bits may be cleared before the next disk command by issuing a CLCE auxiliary command.

The interrupt caused by the SRQ bit indicates that a Sense Interrupt Status command should be issued by the host microprocessor so that it can determine the exact cause of the interrupt. However, the μPD7261 may be processing a disk command when the interrupt occurs. Since it is not possible to issue a disk command while the μPD7261 is busy, an HSRQ auxiliary command can be issued to set the SRQM (Sense Interrupt Request Mask) and mask the interrupt. The SRQM is reset upon completion of the disk command in progress.

DMA Control

When true, the DREQ pin and the DRQ (data request) bit of the status register indicate a request for data transfer between the disk controller and external memory. These are activated during execution of the following disk commands:

HDC ← memory: FORMAT, Verify ID, Scan, Verify Data, Write Data
HDC → memory: Read ID, Read Diagnostic, Read Data

Data being read from a disk or external memory is temporarily stored in the data buffer (8-bytes maximum), and is transferred to external memory or a disk respectively.

Data transfers are terminated externally by a reset signal or by a read or a write data operation coinciding with an active terminal count (TC) signal. They are also terminated internally when an abnormal condition is detected or all the data specified by the sector count parameter (SCNT) has been transferred.

Data transfers are accomplished by $\overline{RD}$ or $\overline{WR}$ signals to the μPD7261 when DREQ is active. During Read operations, DREQ goes active when the FIFO contains three or more bytes. If the FIFO contains three bytes and an $\overline{RD}$ pulse is issued, DREQ goes low within t_{RAI1}. DREQ will stay active on the final sector until the final byte is extracted. In this case, DREQ goes low within t_{RAI2}. During Write operations DREQ is asserted as soon as a WRITE DATA command is accepted. DREQ remains high until the FIFO contains six bytes, at which time it goes low within t_{WAI}. DREQ corresponds to FIFO almost-full and FIFO almost-empty as implemented in the μPD7261. This has been done so that a fast DMA controller may actually overrun the FIFO by one or two bytes without harm.

Recalibrate

0101B	
	IST*

The read/write heads of the specified drive are retracted to the cylinder 0 position. IST* is available as a result byte only if polling mode is disabled. See SPECIFY.

a. Hard Sector

An RTZ (Return to zero) signal is asserted on the bit-6 line with the TAG-3 bit being set. Then the CEH bit of the status register is set indicating a normal termination of the command.

After this command is given, the HDC checks the Seek End, Unit Ready, and Fault lines of the drive continually

until an active signal is detected on these lines. Then the SRQ bit of the status register is set indicating that a Sense Interrupt Status command should be performed. Each bit of the IST (Interrupt Status) byte is set according to the result, in anticipation of the Sense Interrupt Status command.

b. Soft Sector

There are four different ways to implement the Recalibrate command when the ST506 interface mode has been specified. Both polling and nonpolling modes of operation are provided, with both normal or buffered Recalibrate commands available in either mode.

b-1. Normal Mode with Polling

The CEH bit of EST is set to "1" immediately after the Recalibrate command is issued (a Recalibrate command may now be issued to another drive). The HDC now begins generating step pulses at the specified rate. The PCN for the drive is cleared and the TRK0 signal is checked while stepping pulses are sent to one or more drives. When TRK0 is asserted, the SEN (Seek End) bit of the IST (Interrupt Status) byte is set and the SRQ bit of the status register is set. This causes an interrupt and requests that a Sense Interrupt Status command be issued. If 1023 pulses have been sent and TRK0 is not asserted, then the SRQ bit is again set, but with the SER (Seek Error) bit of the IST byte set. The Ready signal of each drive is checked before each step pulse is sent, and the Recalibrate command is terminated if the drive enters a not-ready state, whereby the NR bit of the IST byte is set to "1."

b-2. Normal Mode with Polling Disabled

Operation is similar to that in section "b-1," but the CEH and CEL bits of the status register are not set until either the SEN (Seek End) or the SER (Seek Error) condition occurs. The SRQ bit is not set when polling is disabled, and the IST byte is now available as a result byte when the Recalibrate command is terminated (see "Preset Parameters and Result Status Bytes"). It is not possible to overlap Recalibrate operations in this mode.

b-3. Buffered Mode with Polling

This mode operates in a manner similar to that described in section "b-1," but with the following differences:

1. 1023 step pulses are sent at a high rate of speed (approximately 50μs between pulses)
2. After the required number of pulses are sent, the CEH bit is set, and then additional Recalibrate or Seek commands will be accepted for other drives
3. The SRQ bit is set when the drive asserts SKC, which causes the SEN bit of the IST byte to be set
4. If SEN is not set within the time it takes to send 1023 "normal" pulses (i.e., when in normal stepping mode), then SER of the IST byte is set.

b-4. Buffered Mode with Polling Disabled

1023 stepping pulses are immediately sent after the Recalibrate command is issued. CEH and/or CEL is set when SEN or SER occurs. SEN is set when TRKO from the addressed drive is asserted. SER is set if TRKO is not asserted within the time required to send 1023 "normal" pulses. The Recalibrate command will be terminated abnormally if a not-ready condition occurs prior to SEN being set. The SRQ bit of the status register is not set. The IST byte (Interrupt Status) is available as a result byte when either CEH or CEL is set.

Seek

0110B	PCNH	PCNL
	IST*	

PCNH = Physical Cylinder Number, High Byte
PCNL = Physical Cylinder Number, Low Byte

The read/write heads of the specified drive are moved to the cylinder specified by PCNH and PCNL. IST* is available as a result byte only if polling mode is disabled.See SPECIFY.

a. Hard sector

The contents of PCNH and PCNL are asserted on the bit-0 through bit-9 output lines of the SMD interface with the TAG-1 control line being set. (The most significant six bits of PCNH are not used.) The CEH bit of the status register is then set, and the command is terminated normally.

The HDC then checks the Seek End, Unit Ready and Fault lines of the drive continually until an active signal is detected on these lines. The SRQ bit of the status register is then set requesting that a Sense Interrupt Status command be performed. Each bit of the IST (Interrupt Status) byte is set appropriately in anticipation of the Sense Interrupt Status command.

b. Soft Sector (Normal Stepping, Polling Enabled)

In this mode, the CEH bit of the status register is set to "1" as soon as the Seek command is issued. This allows a Seek or Recalibrate command to be issued to another drive. The HDC now sends stepping pulses at the specified rate and monitors the Ready signal. Should the drive enter a not-ready state, the SER bit of the IST byte is set and the SRQ bit of the status register is set, causing an interrupt and requesting a Sense Interrupt Status command. When the drive asserts the Seek Complete (SKC) signal, the SEN bit of the IST byte is set and the SRQ bit of the status register is set, again requesting service.

c. Soft Sector (Normal Stepping, Polling Disabled)

Stepping pulses to the drive begin as soon as the Seek command is accepted. The Ready signal is checked prior to each step pulse. If the drive enters a not-ready state the Seek command is terminated abnormally (CEL = 1), and SER of the IST byte is set. If the Seek operation is successful, the Seek command will be terminated normally (CEH = 1) when the drive asserts SKC (Seek Complete). The SEN (Seek End) bit of the IST byte is set and the IST (Interrupt Status) byte is available as a result byte. The Sense Interrupt Status command is not allowed (SRQ is not set), nor can Seek operations be overlapped in this mode.

d. Soft Sector (Buffered Stepping, Polling Enabled)

As soon as the Seek command is accepted by the HDC, high-speed stepping pulses are generated. As soon as the required number of pulses are sent, CEH is set to "1," indicating a normal termination. Another Seek command in the same mode may now be issued. (The drive is now controlling its own head positioner and asserts SKC when the target cylinder is reached.) If the drive has not asserted SKC (Seek Complete) within the time it takes to send the required number of pulses in normal stepping mode, or if the drive enters a not-ready state, then the SER bit of the IST byte and the SRQ bit of the status register are set. Otherwise, the SEN bit of the IST byte is set, along with SRQ of the status register.

e. Soft Sector (Buffered Stepping, Polling Disabled)

In this mode, the appropriate number of high-speed stepping pulses are sent as soon as the Seek command is issued. If the drive enters a not-ready state, or if SKC (Seek Complete) is not asserted within the time it takes to send the required number of pulses in normal stepping mode, then the Seek command is terminated abnormally (CEL = 1). The IST byte is available as a result byte and the appropriate bit is set; i.e., SER or NR (Not Ready). If the Seek operation is successful, the Seek command is terminated normally (CEH = 1) and the SEN bit of the IST byte is set. The IST byte is available as a result byte. The Sense Interrupt Status command is not allowed (SRQ is not set), nor can Seek operations be overlapped in this mode.

Format

0111S	PHN	(PSN)	SCNT	DPAT	GPL1	[GPL3]
	EST	SCNT				

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
DPAT = Data Pattern
GPL1 = Gap Length 1
GPL3 = Gap Length 3
EST = Error Status

This command is used to write the desired ID and Data format on the disk.

a. When using hard-sector drives, this command will begin format-writing at the sector specified by PHN and PSN, which are loaded during command phase.

When soft-sector drives are specified, this command will begin format-writing at the sector immediately following the index pulse on the track specified by PHN.

In either case, data transmitted from the local memory by DMA operation is written into the ID field, and the Data field is filled with the data constant specified by DPAT until DTL (Data Length) is zero. DTL is established during the Specify command with DTLH and DTLL. The Sector Count, SCNT, is decremented by one at the end of the Format-Write operation on each sector. The following bytes are required by the HDC for each sector: (FLAG), LCNH, LCNL, LHN, and LSN. FLAG is omitted on soft-sector drives. These bytes are transferred by DMA.

b. The above operation is repeated until SCNT is equal to zero. The execution of the command is terminated normally, when the content of SCNT is equal to zero and the second index pulse has occurred.

c. When using a hard-sector drive, it is possible to write the ID field displaced from the normal position by 64 bytes by setting the Skew bit of the command byte ((S) = 1). This is useful when defective media prevent writing in the normal area of the sector.

d. Items d, e, and h of the Read Data and item d of the Write Data command are identical for this command. Refer to these items (which appear later in this section) for the remaining Format Write detail.

Verify ID

1000S	PHN	(PSN)	SCNT
	EST	SCNT	

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
EST = Error Status

ID bytes of specified sectors are read and compared with the data that are accessed from local memory via DMA control. The first sector that is verified is specified by PHN and PSN when a hard-sector disk is used. For soft-sector disks, only PHN is given and the Verify ID command begins comparisons with the first physical sector on the track.

Byte comparisons continue as long as successful or until the sector count is zero or a CRC error is found.

When using a hard-sector drive, it is possible to have the HDC verify a Skewed ID field by setting the Skew bit of the command byte. Refer to the Format Write section, given earlier, for details.

Read ID

1001S	PHN	(PSN)	SCNT
	EST	SCNT	

PHN = Physical Head Number
PSN = Physical Sector Number
SCNT = Sector Count
EST = Error Status

ID bytes of specified sectors are read and transferred to local memory by DMA.

Hard-sector disks: Beginning with the sector specified by PHN and PSN, the ID bytes of each sector are read until an error is found or the SCNT has reached zero.

It is also possible to perform the above operation with skewed ID fields by setting the Skew bit of the command byte. This will allow reading ID fields that have been shifted by 64 bytes by the Write Skewed ID command.

Soft-sector disks: This command will begin checking ID fields immediately following the index pulse and will continue until one valid ID field is read, or until the second index pulse is detected.

Read Diagnostic

1010X	PHN	PSN
	EST	

PHN = Physical Head Number
PSN = Physical Sector Number
EST = Error Status

This command is implemented only for hard-sector disks. The desired physical sector is specified, and the data field will be read even if the ID bytes of that sector contain a CRC error. Only one sector at a time may be read by this command.

Read Data

1011X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to read and transfer data via DMA from the disk to the local memory.

a. The HDC reads data from the specified sector which is determined by the following preset parameters: FLAG (for hard sector only), LCNH, LCNL, LHN, and LSN. The drive is selected by UA (Unit Address) in the command byte. The

HDC then transfers the read data to the local memory via DMA operation.

b. After reading each sector, the HDC updates the SCNT and LSN to point to the next sector, and repeats the above described operation until SCNT is equal to zero. During the above read operations, if LSN is equal to ESN, the HDC updates LSN, and continues the read operations after relocating the head (track) specified by LHN.

c. The HDC abnormally terminates the execution of this command, if SCNT is not equal to zero when the HDC reads out the data from the last sector (LSN = ESN and LHN = ETN). The ENC (End of Cylinder) bit of EST (Error Status) is set to one in this situation.

d. The HDC will terminate this command if a Fault signal is detected while reading data. The HDC will set the EQC (Equipment Check) of the EST (Error Status) byte when this occurs.

e. The HDC will terminate this command abnormally if the Ready signal from the drive is not active or becomes not-active while a Read Data command is being performed. The NR (Not Ready) bit of the EST (Error Status) register will be set to one in this case.

f. The HDC will end this command abnormally if it cannot find an AM (Address Mark) (soft-sector mode) or a SYNC byte (hard-sector mode) of the ID field before three index pulses occur. Under these conditions, the RRQ (Reset Request) bit of the STR (Status Register) will be set. In order to perform further disk commands the HDC will have to be reset because the Format Controller is hung up looking for an AM or SYNC byte.

g. ECC mode: If the HDC detects an ECC error during a read operation, it will execute the following operations: First, the HDC decides whether or not the error is correctable by checking the syndrome of the error pattern. If the error is correctable, the HDC terminates the command in the normal mode after setting the DER (Data Error) bit of EST register to one. The host system can input the error-address and the error-pattern information by issuing the Detect Error command. If it is not a correctable error, the HDC will terminate the command in the abnormal mode after setting the DER bit of the EST register to one.

CRC mode: If the HDC detects a CRC error on a sector during the read operation, the HDC will terminate the command in the abnormal mode after setting the DER bit of the EST register to one.

h. If the HDC detects an overrun condition during a Read Data operation, the OVR (Over Run) bit of the EST register is set. (An overrun condition occurs when the internal data FIFO is full, another data byte has been received from the disk drive, and a DMA service does not occur.) The command is then terminated in the abnormal mode.

i. If the HDC cannot find the desired sector within the occurrence of two index pulses, the ND (No Data) bit of the EST register is set to one and the command is terminated in the abnormal mode.

j. If TC (Terminal Count) occurs during a Read Data command the DMA transfers to the local memory will stop. However, the HDC does continue the read operation until SCNT has reached zero or any other errors have been detected.

k. If the Read Data command has been successfully completed, the result status will be set indicating such, and the result status bytes will be updated according to the number of sectors that have been read. The logical disk parameters — LSN, LHN, and LCNL — are incremented as follows:

LSN is incremented at the end of each sector until the value of ESN is reached. LSN is then set to 0 and LHN is incremented. If LHN reaches the value of ETN, then LHN is cleared and LCNL is incremented.

In other words; if a Read or Write operation is terminated normally, the various parameters will point to the next logical sector.

If the command is terminated in the abnormal mode, the result status bytes will indicate on which sector, cylinder, and head the error occurred.

l. If the HDC cannot detect the Address Mark (soft sector) or SYNC bytes (hard sector) immediately following the VFO Sync in the data field, the HDC will set the MDM (Missing Data Mark) bit of the EST register to one, and will terminate the command in the abnormal mode.

Check

1100X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to confirm that the data previously written to the medium by the Write Data command contains the correct CRC or ECC.

a. The HDC reads the data in the sector specified by FLAG (hard sector only), LCNH, LCNL, LHN, and LSN. The Check command differs from the Read Data command in that no DMA transfers occur.

With the exception of the ECC mode, the Check command is the same as the Read Data command. Please refer to items b, c, d, e, f, g, h, k, and l of Read Data command for details.

b. If in the ECC mode, the HDC detects only ECC errors and does not execute any error-correction operation even if the ECC errors are correctable. No data transfers have been made, and there is no data to correct.

Scan

1101X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT	
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

a. In executing the Scan command, the HDC reads the data from the sector specified by the preset parameters of the command phase. The HDC then compares this data

with the data transmitted from the local memory. (The purpose of this command is to locate a sector that contains the same data as the local memory.)

This command will terminate successfully if the data from the disk and the data from the local memory are the same. If they are not, the HDC updates SCNT and LSN, and executes the above-mentioned operation again.

If the HDC cannot locate a sector that satisfies the Scan conditions, the NCI bit of the STR will be set. The HDC tries to compare data until the end of the cylinder has been reached, or until SCNT is zero.

b. If the value of the LSN (Logical Sector Number) is equal to that of ESN (Ending Sector Number) after updating LSN, the HDC updates the contents of LHN (increasing by 1) and that of LSN (LSN = 0), and repeats the operation described in item a after selecting the next head.

c. After comparing the data transferred from the host CPU with the data in the specified sectors, the result bytes (FLAG, which is only for hard-sector disks, LCNH, LCNL, LHN, and LSN) will be set equal to the sector location that satisfies the Scan command.

d. The descriptions in d, e, f, h, and i of Read Data command, and items c and d of Verify Data command are identical for this command. Refer to these descriptions for additional details.

Verify Data

1110X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

This command is used to verify data on the disk.

a. The HDC reads the data from the specified sector, and compares the data transmitted from the local memory via DMA with the data from the disk.

The sector is specified by FLAG (hard sector only), LCNH, LCNL, LHN, and LSN, and the drive is selected by UA. If the data transmitted from the local memory is the same as that read from the sector, the HDC updates the contents of LSN and SCNT, and continues the above-mentioned operation. After updating SCNT, if the value of SCNT is equal to zero, the HDC ends the execution of the command in the normal mode. If the value of LSN is equal to that of ESN after updating LSN, the HDC updates the contents of LHN and LSN, and the HDC continues Verify Data operation after selecting the head (track) specified by LHN.

If the data transmitted from the local memory is not the same as that read from the sector, the HDC ends the execution of the command in the abnormal mode after setting the NCI (Not Coincident) bit of STR to one.

b. If, after verifying the data on the last sector, the contents of SCNT are not equal to zero, the HDC terminates execution of the command abnormally after setting the ENC (End of Cylinder) bit of the EST register to one.

c. After verifying the data read from a sector, the HDC checks the CRC bytes (CRC mode) or the ECC bytes (ECC mode).

If the HDC detects a CRC or an ECC error on a sector, the HDC terminates execution of the command abnormally after setting the DER bit of the EST register to a one.

d. After detecting an active TC signal (TC = 1), the HDC executes the above operation by comparing the read data from the disk drive with the data 00 instead of the data from the main system.

e. After verification of the data on all the sectors, FLAG (hard sector only), LCNH, LCNL, LHN, and LSN are set to the values of FLAG, LCNH, LCNL, LHN, and LSN of the last verified sector.

f. The descriptions in items d, e, f, h, i, and l of the Read Data command are valid in this command. Please refer to these items for additional detail.

Write Data

1111X	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT
	EST	PHN	(FLAG)	LCNH	LCNL	LHN	LSN	SCNT

PHN = Physical Head Number
FLAG = Flag Byte, Hard-sector ID Field Only
LCNH = Logical Cylinder Number, High Byte
LCNL = Logical Cylinder Number, Low Byte
LHN = Logical Head Number
LSN = Logical Sector Number
SCNT = Sector Number
EST = Error Status

a. This command is used to write data into the data field of the sectors specified by FLAG (hard disks only), LCNH, LCNL, LHN, and LSN, and to write CRC bytes or ECC bytes according to each internally specified mode (CRC or ECC). The data is written to the disk via DMA transfer from the local memory.

b. After writing data on a sector, the HDC updates the contents of SCNT and LSN, and repeats the above described Write-Data operation until SCNT is equal to zero.

During the above Write-Data operations, if LSN is equal to ESN, the HDC updates LHN and LSN, and continues the Write-Data operations after selecting the new head (track) specified by LHN.

As described above, the HDC has the capability of multi-sector and multitrack write operations.

c. The HDC abnormally terminates the execution of this command, if the SCNT is not equal to zero when the HDC writes the data to the last sector (LSN = ESN and LHN = ETN). The ENC (End of Cylinder) bit of the EST (Error Status) register is set to one in this situation.

d. If the Write Protected signal is active (high) at the beginning of the execution of this command, the HDC ends the execution of this command in the abnormal mode after setting the NWR (Not Writable) bit of the EST register to one.

e. After detecting an active TC signal (TC = 1), the HDC writes the data 00 to the sector, instead of the data from the host system, until the SCNT is equal to zero, or until the HDC detects any abnormal state.

f. In the floppy-like mode, the HDC will set the Reduced Write Current output bit of port 1 to a one when the cylinder number becomes greater than that specified by RWCH and

RWCL. These parameters are loaded during execution of the Specify command.

The descriptions in items d, e, f, h, i, and k of the Read Data command are applicable here also. Refer to these items for further detail.

Sense Interrupt Status

0001X	
	IST

IST = Interrupt Status

a. The HDC transfers the new disk status to the host CPU at the end of a Seek or Recalibrate operation or the new disk status resulting from a change of state of the Ready signal, which may occur at any time.

b. If the Seek or Recalibrate command in progress is completed when this command is issued or if there has been no change of state of the Ready signal from the drive, this command will be terminated abnormally.

Specify

0010X	MODE	DTLH	DTLL	ETN	ESN	GPL2	(MGPL1) [RWCH]	[RWCL]

MODE = Mode Byte; Selects Operation Mode

MDU	ECC	CRCS	SSEC	DSL/ STP3	DSE/ STP2	SOM/ STP1	SOP/ STP0

Bit Name		Specified Mode
MDU	1	Inhibited
	0	MFM data when SSEC = 1, NRZ when SSEC = 0
ECC	1	ECC is appended in data field $(x^{21} + 1)(x^{11} + x^2 + 1)$
	0	CRC is appended in data field
CRCS	1	Generator polynomial: $(x^{16} + 1)$
	0	Generator polynomial: $(x^{16} + x^{12} + x^5 + 1)$
SSEC	1	Soft-sector disk (floppy-like interface)
	0	Hard-sector disk (SMD interface)

	SSEC = 0		SSEC = 1
DSL	Data Strobe Late	STP3	Stepping rate for ST506 Mode:
DSE	Data Strobe Early	STP2	f_H = 2.11ms
SOM	Servo Offset Minus	STP1	⋮
SOP	Servo Offset Plus	STP0	0_H = 33.76ms assuming a 10MHz-processor clock.
Stepping Rate = (16 − STP) x 21100 x t_{CY}			

DTLH = Data Length, High Byte

1	CRC•	PAD	POL	DTL11	DTL10	DTL9	DTL8

CRC• = Initial Value of Polynomial Counter, Either All Zeros or All Ones
PAD = Selects ID/Data pad of 00H if 0
= Selects ID/Data pad of 4EH if 1.
POL = Polling Mode if 0
= Nonpolling Mode if 1.
DTLL = Data Length, Low Byte
ETN = Ending Track Number
ESN = Ending Sector Number
GPL2 = Gap Length 2
MGPL1 = Gap Length 1 (used in SMD mode only), Controls Read Gate Timing
RWCH = Reduced Write Current (Cylinder No.), High Byte
RWCL = Reduced Write Current (Cylinder No.), Low Byte

The Specify command is used to set the operational mode of the HDC by presetting various parameters. Parameters such as MODE, DTLH, DTLL, ETN, ESN, GPL2, GPL1/ RCNH, and RCNL may be programmed into the HDC. This allows for a high degree of versatility.

Sense Unit Status

Soft-Sector Mode

0011X	
	UST

SMD Mode

0011X	1	2	5
	UST	DS	DT

The Sense Unit Status (SUS) command is used to transfer the Unit Status (UST) to the host. In the case of SMD mode the SUS command may also be used to transfer the Detail Status (DS) and Device Type (DT) by using the appropriate preset parameter value as shown above. No preset parameters are used in the soft-sector mode, although one is required in the SMD mode. Values other than 1, 2, or 5 do not produce valid results.

The DS and DT bytes are defined by the type of drives used. The UST is shown below:

Unit Status Byte

Bit No.	Interface Type	
	SMD	Floppy-like
D7	Unit Selected	0
D6	Seek End	0
D5	Write Protected	0
D4	(AM Found)	Drive Selected
D3	Unit Ready	Seek Complete
D2	On Cylinder	Track 000
D1	Seek Error	Ready
D0	Fault	Write Fault

Detect Error

0100X						
	EADH	EADL	EPT1	EPT2	EPT3	

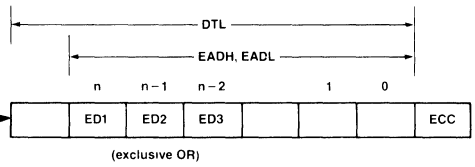
EADH = Error Address, High Byte
EADL = Error Address, Low Byte
EPT1 = Error Pattern, Byte 1
EPT2 = Error Pattern, Byte 2
EPT3 = Error Pattern, Byte 3

This command is used to transfer the error pattern and the error address to the host CPU, when correctable errors have occurred during the execution of a Read Data command with the ECC mode enabled.

The error address (EADH and EADL) is calculated from the last data byte of the sector that contained a correctable error which was indicated by the status bits of the previous Read Data command with the ECC mode enabled. The error pattern is used for correcting the error data at the location where the error occurred. After receiving the error address and the error pattern, the host CPU can correct the error data by performing an exclusive-OR of the error pattern and the error data.

The result bytes are available to the host CPU within 100 μs.

The sector included correctable error



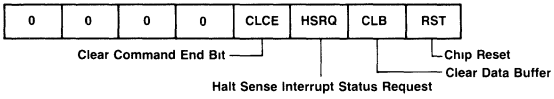
Note: EDn equals error byte

Auxiliary command

0000AAAA	

There are no preset parameters or result bytes associated with this command. The definitions of the 4 LSBs (AAAA) are given below. The auxiliary command is accepted at any time and is immediately executed. The auxiliary command may be used to recover from certain types of error conditions, or to mask and clear interrupts.

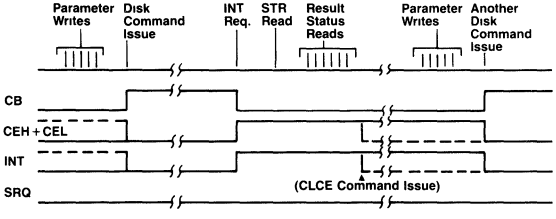
Bit Name	Operation
CLCE	Clears the CE bits of the status register, inactivating the interrupt request output caused by Command End condition. This is used when no disk commands are going to be issued and it is desired to clear the interrupt.
HSRQ	Deactivates the interrupt request output caused by Sense Interrupt Status Request condition until a Command End occurs. However, this command has no effect on the SRQ bit of the status register.
CLB	Clears the data buffer.
RST	This has the same effect as a reset signal on the Reset input. This function is used whenever the RRQ bit in the status register is set (indicating the format controller is hung up), or when a software reset is needed.



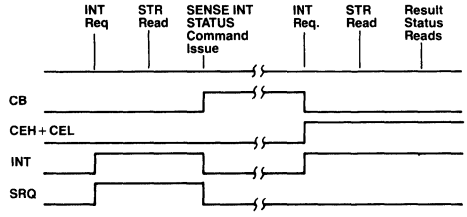
Timing Waveforms

Read/Write Sequence

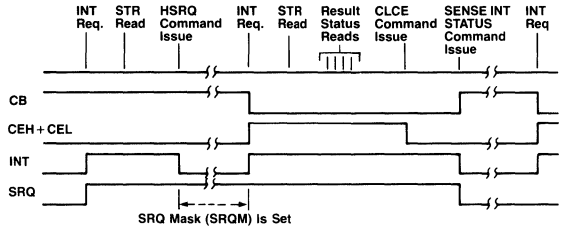
Disk command issue



Sense Interrupt Status Request When Controller Not Busy

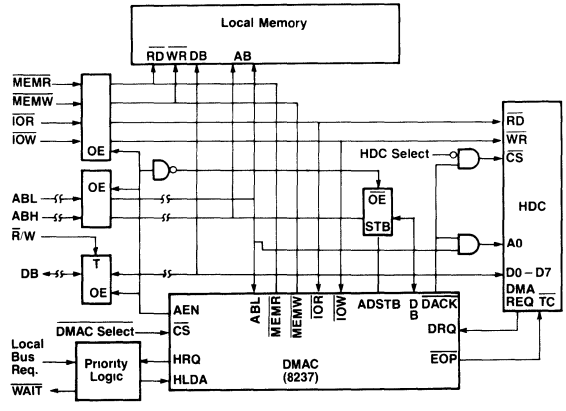


Sense Interrupt Status Request When Controller Busy



System Example

Local Bus System



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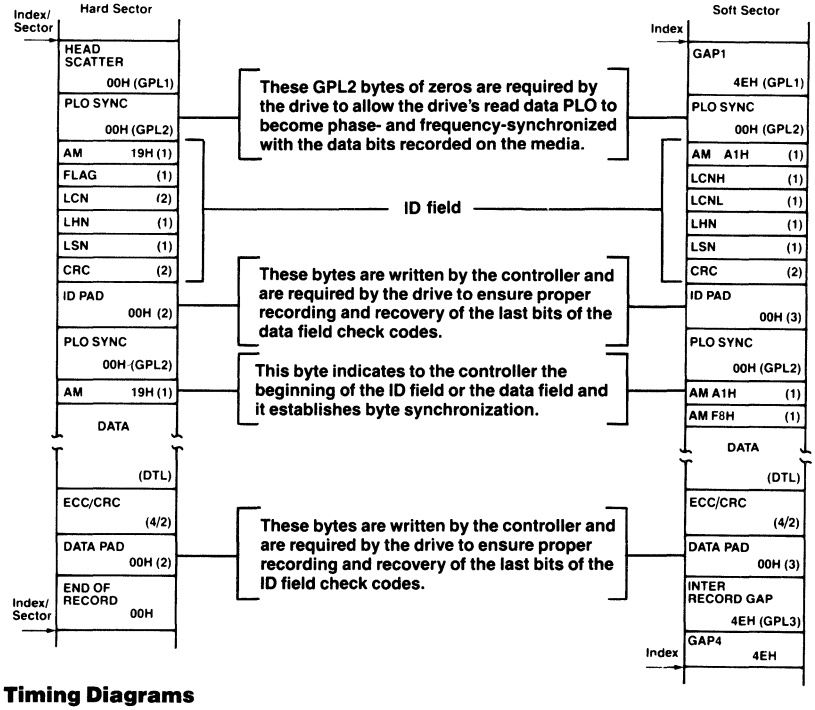
Track Format



System Example Timing Diagrams

Figures 1 through 12 show the interface timing (soft sector and hard sector) required to interface the hard-disk drive.

Figure 1. "Unit Selection" and "State Sense" Timing (Hard Sector)

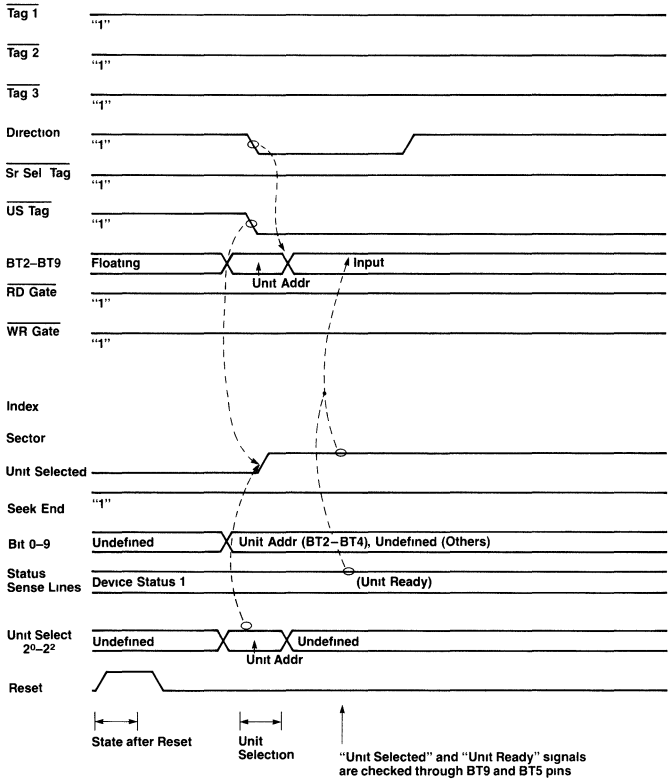


Figure 2. Return to Zero Timing (Hard Sector)

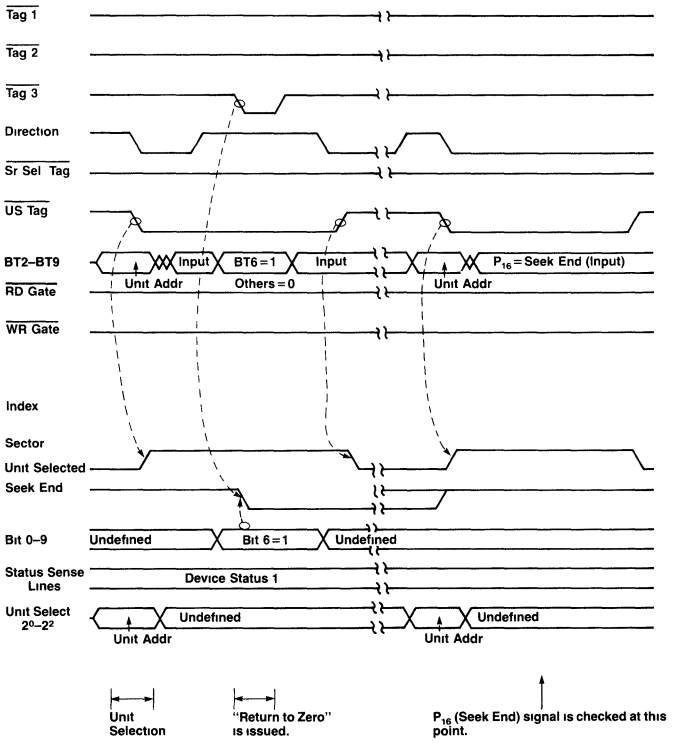


Figure 3. "Seek" Timing (Hard Sector)

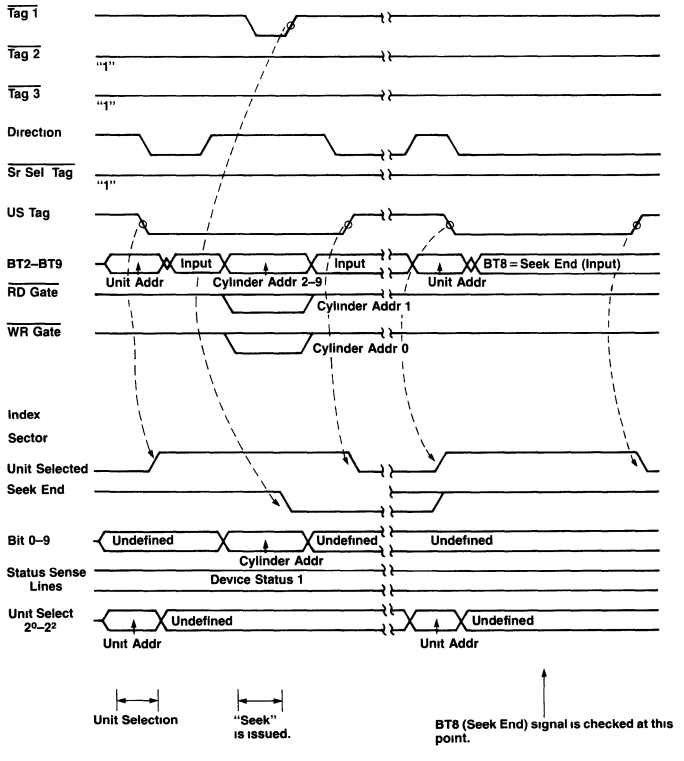


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Figure 4. "Head Select" Timing (Hard Sector)

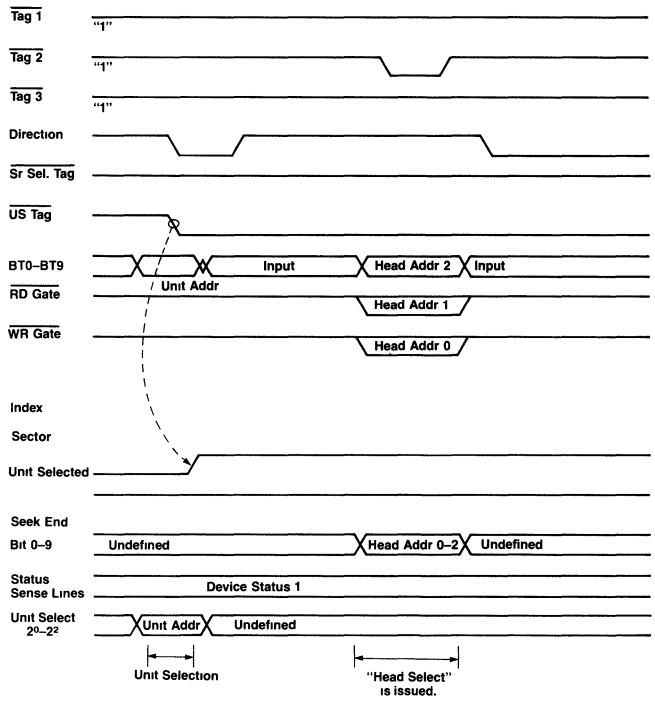

Figure 5. "Device Status Sense" Timing (Hard Sector)

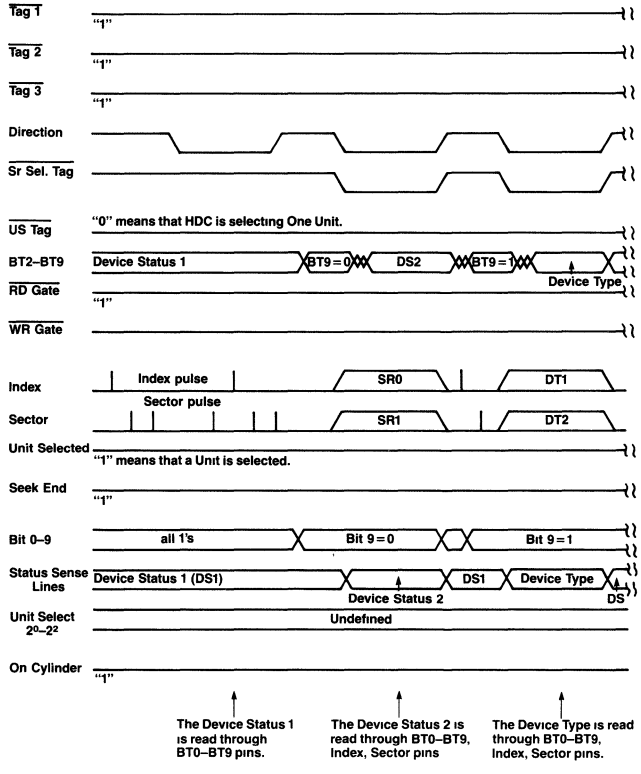

Figure 6. "Data Read" Timing (Hard Sector)

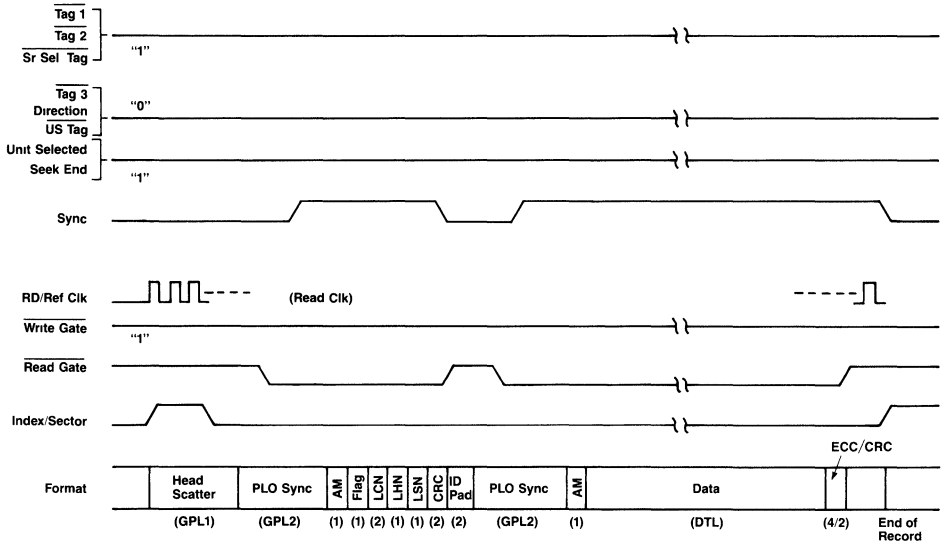

Figure 7. "Data Write" Timing (Hard Sector)

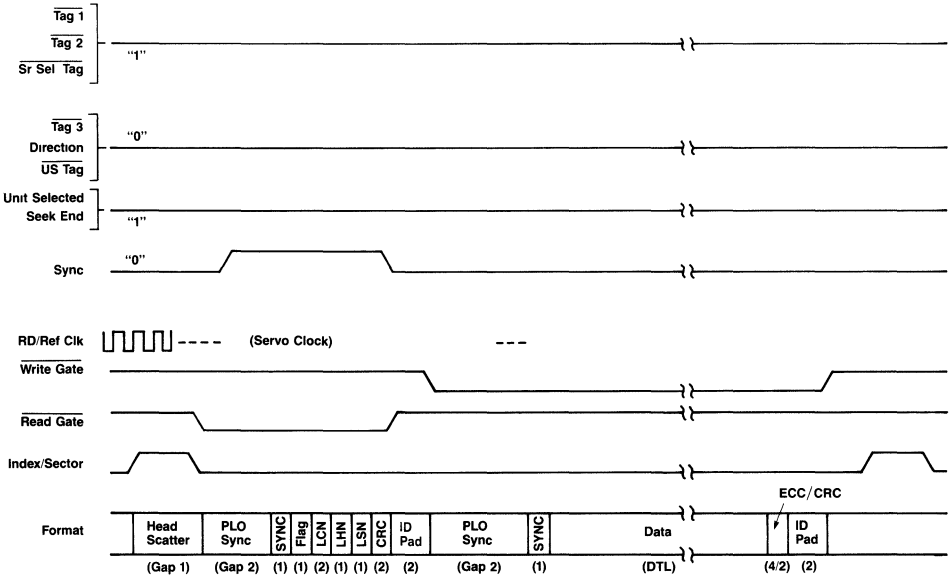

Figure 8. "Drive Select" and "Unit Status Sense" Timing (Soft Sector)

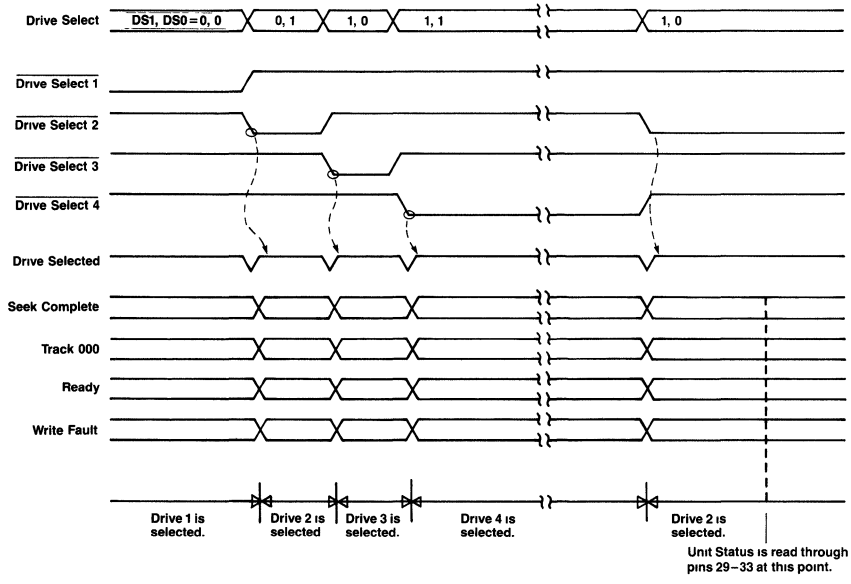

Figure 9. "Normal Seek" Timing (Soft Sector)

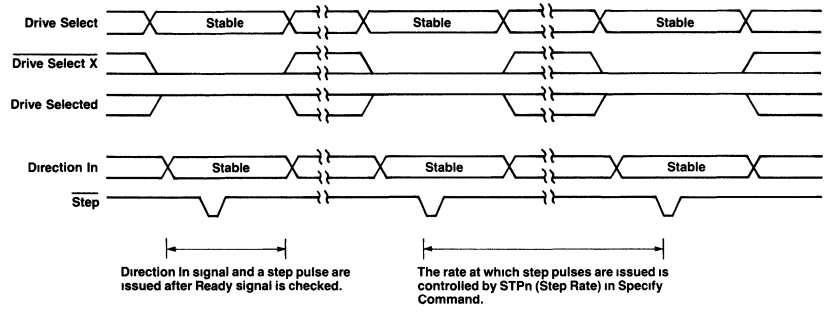

Figure 10. "Buffered Seek" Timing (Soft Sector)

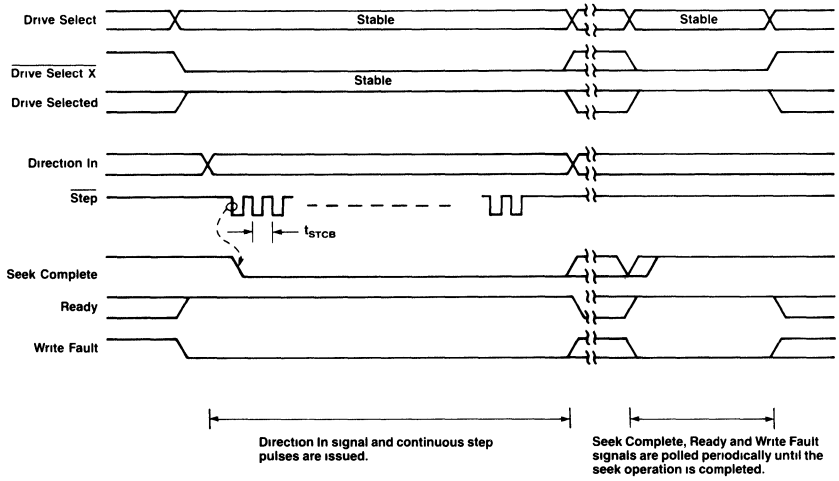

Figure 11. "Data Read" Timing (Soft Sector)

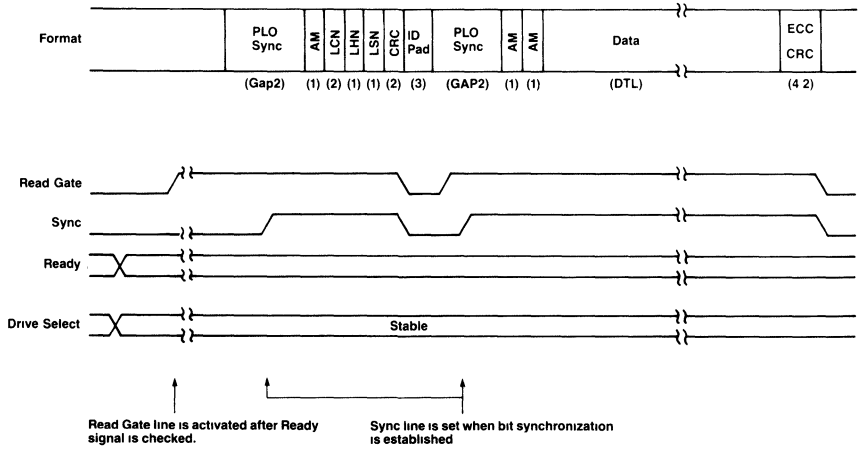

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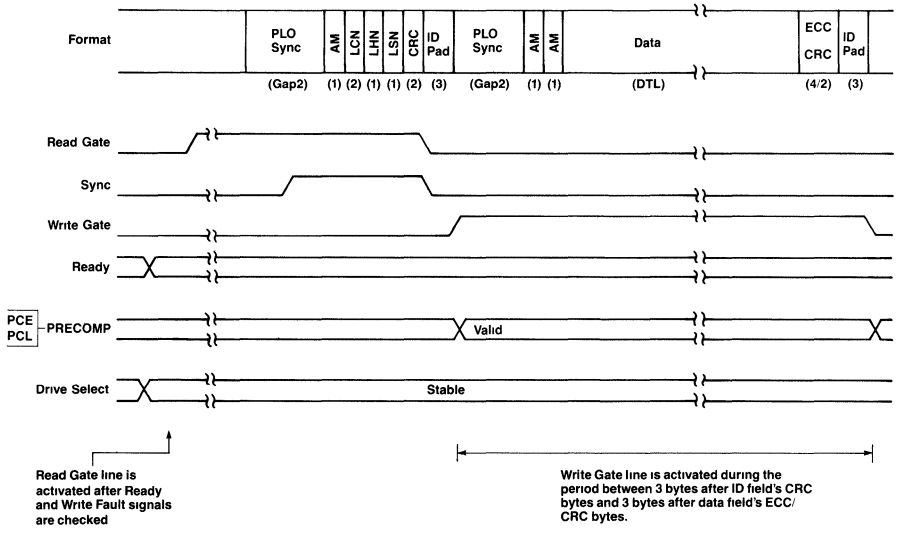
Figure 12. "Data Write" Timing (Soft Sector)



Package Outlines

For information, see Package Outline Section 7.

Ceramic, μPD7261D

Description

The NEC μPD7720 Signal Processing Interface (SPI) is an advanced architecture microcomputer optimized for signal processing algorithms. Its speed and flexibility allow the SPI to efficiently implement signal processing functions in a wide range of environments and applications.

The NEC SPI is the state of the art in signal processing today, and for the future.

Applications

- ☐ Speech Synthesis and Analysis
- ☐ Digital Filtering
- ☐ Fast Fourier Transforms (FFT)
- ☐ Dual-Tone Multi-Frequency (DTMF) Transmitters/Receivers
- ☐ High Speed Data Modems
- ☐ Equalizers
- ☐ Adaptive Control
- ☐ Sonar/Radar Image Processing
- ☐ Numerical Processing

Performance Benchmarks

☐ Second Order Digital Filter (Biquad)	2.25 μs
☐ Sine/Cos of Angles	5.25 μs
☐ μ/A Law to Linear Conversion	0.50 μs
☐ FFT: 32-point Complex	0.7 ms
64-point Complex	1.6 ms

Features

- ☐ Fast Instruction Execution — 250 ns
- ☐ 16-Bit Data Word
- ☐ Multi-Operation Instructions for Optimizing Program Execution
- ☐ Large Memory Capacities

Program ROM	512 x 23 Bits
Data ROM	510 x 13 Bits
Data RAM	128 x 16 Bits

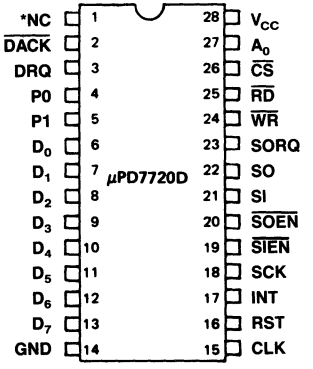
- ☐ Fast (250 ns) 16 x 16 31-Bit Multiplier
- ☐ Dual Accumulators
- ☐ Four Level Subroutine Stack for Program Efficiency
- ☐ Multiple I/O Capabilities
  - Serial
  - Parallel
  - DMA
- ☐ Compatible with Most Microprocessors, Including:
  - μPD8080
  - μPD8085
  - μPD8086
  - μPD780 (Z80)™*
- ☐ Power Supply +5V
- ☐ Technology NMOS
- ☐ Package — 28 Pin Dip

*Z80 is a registered trademark of Zilog Corporation

Pin Identification

Pin No.	Pin Symbol	I/O	Function
1	NC	I	No Connection for masked ROM μPD7720 Consult μPD77P20 specifications for connection for pin-compatible EPROM version
2	$\overline{DACK}$	I	DMA Request Acknowledge. Indicates to the μPD7720 that the Data Bus is ready for a DMA transfer. ($\overline{DACK} = \overline{CS} \bullet A_0 = 0$)
3	DRQ	O	DMA Request. Signals that the μPD7720 is requesting a data transfer on the Data Bus.
4, 5	P_0, P_1	O	General purpose output control lines.
6-13	D_0-D_7	I/O Three-state	Port for data transfer between the Data Register or Status Register and external Data Bus.
14	GND		Ground.
15	CLK	I	Single phase Master Clock input.
16	RST	I	Reset. Initializes the μPD7720 internal logic and sets the PC to 0.
17	INT	I	Interrupt. A low to high transition on this pin executes a call instruction to location 100H, if interrupts were previously enabled.
18	SCK	I	Serial Data Input/Output Clock. A serial data bit is transferred when this pin is high.
19	$\overline{SIEN}$	I	Serial Input Enable. Enables the shift clock to the Serial Input Register.
20	$\overline{SOEN}$	I	Serial Output Enable. Enables the shift clock to the Serial Output Register.
21	SI	I	Serial Data Input. Inputs 8- or 16-bit serial data words from an external device such as an A/D converter.
22	SO	O Three-state	Serial Data Output. Outputs 8- or 16-bit data words to an external device such as a D/A converter.
23	SORQ	O	Serial Data Output Request. Specifies to an external device that the Serial Data Register has been loaded and is ready for output. SORQ is reset when the entire 8- or 16-bit word has been transferred.
24	$\overline{WR}$	I	Write Control Signal. Writes an input from the data port into the Data Register.
25	$\overline{RD}$	I	Read Control Signal. Reads an output to the data port from the Data or Status Register.
26	$\overline{CS}$	I	Chip Select. Enables data transfer through data port with $\overline{RD}$ or $\overline{WR}$.
27	A_0	I	Selects Data Register for Read/Write (low) or Status Register for read (high).
28	V_{CC}		+5V Power

Pin Configuration



*No connection, μPD7720
Must be connected for EPROM version, consult μPD77P20 specifications

Rev/3

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Functional Description

Fabricated in high speed NMOS, the μPD7720 SPI is a complete 16-bit microcomputer on a single chip. ROM space is provided for program and coefficient storage, while the on-chip RAM may be used for temporary data, coefficients, and results. Computational power is provided by a 16-bit Arithmetic/Logic Unit (ALU) and a separate 16 x 16-bit fully parallel multiplier. This combination allows the implementation of a "sum of products" operation in a single 250 ns instruction cycle. In addition, each arithmetic instruction provides for a number of data movement operations to further increase throughput. Two serial I/O ports are provided for interfacing to codecs and other serially-oriented devices while a parallel port provides both data and status information to conventional microprocessors. Handshaking signals, including DMA controls, allow the SPI to act as a sophisticated programmable peripheral as well as a stand-alone microcomputer.

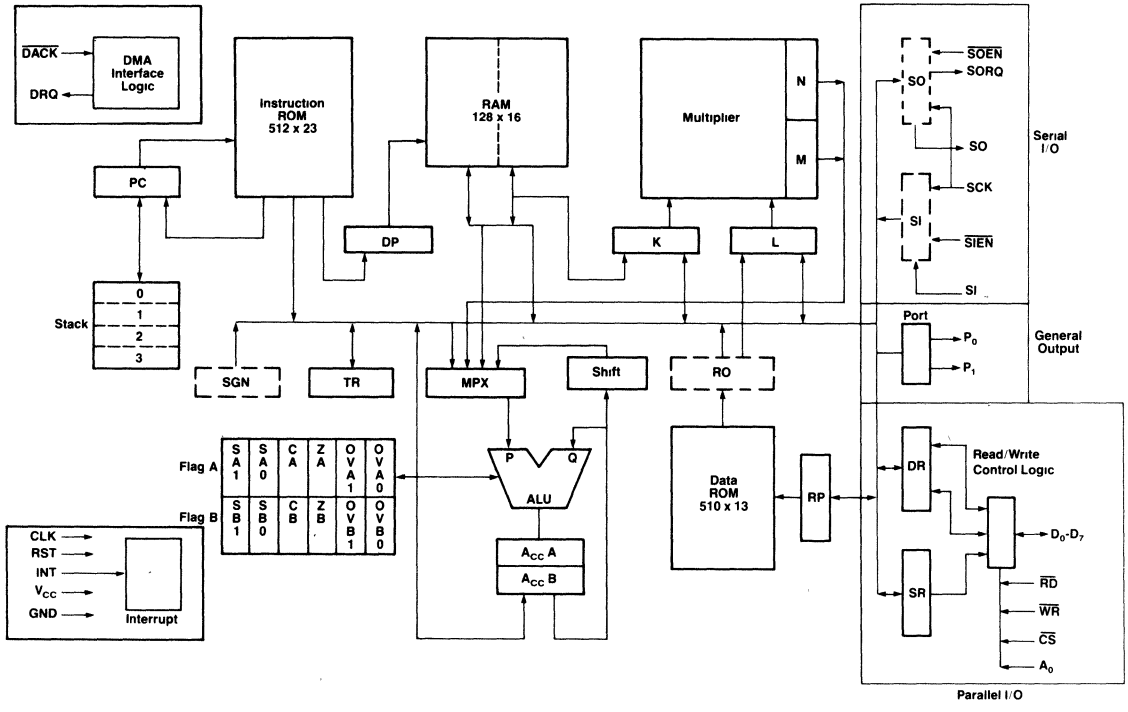
Memory

Memory is divided into three types: Program ROM, Data ROM, and Data RAM. The 512 x 23-bit words of Program ROM are addressed by a 9-bit Program Counter which can be modified by an external reset, interrupt, call, jump, or return instruction.

The Data ROM is organized in 510 x 13-bit words which are addressed through a 9-bit ROM pointer (RP register). The RP may be modified simultaneously with arithmetic instructions so that the next value is available for the next instruction. The Data ROM is ideal for storing the necessary coefficients, conversion tables, and other constants for your processing needs.

The Data RAM is 128 x 16-bit words and is addressed through a 7-bit data pointer (DP register). The DP has extensive addressing features that operate simultaneously with arithmetic instructions so that no added time is taken for addressing or address modification.

Block Diagram



Arithmetic Capabilities

General

One of the unique features of the SPI's architecture is its arithmetic facilities. With a separate multiplier, ALU, and multiple internal data paths, the SPI is capable of carrying out a multiply, an add, or other arithmetic operation, and a data move between internal registers in a single instruction cycle.

ALU

The ALU is a 16-bit 2's complement unit capable of executing 16 distinct operations on virtually any of the SPI's internal registers, thus giving the SPI both speed and versatility for efficient data management.

Accumulators (ACCA/ACCB)

Associated with the ALU are a pair of 16-bit accumulators, each with its own set of flags, which are updated at the end of each arithmetic instruction (except NOP). In addition to Zero Result, Sign Carry, and Overflow Flags, the SPI incorporates auxiliary Overflow and Sign Flags (SA1, SB1, OVA1, OVB1). These flags enable the detection of an overflow condition and maintain the correct sign after as many as three successive additions or subtractions.

ACC A/B Flag Registers

Flag A	SA1	SA0	CA	ZA	OVA1	OVA0
Flag B	SB1	SB0	CB	ZB	OVB1	OVB0

Sign Register (SGN)

When OVA1 is set, the SA1 bit will hold the corrected sign of the overflow. The SGN Register will use SA1 to automatically generate saturation constants 7FFFH(+) or 8000H(−) to permit efficient limiting of a calculated value.

Multiplier

Thirty-one bit results are developed by a 16 x 16-bit 2's complement multiplier in 250 ns. The result is automatically latched to two 16-bit registers M&N (sign and 15 higher bits in M, 15 lower bits in N; LSB in N is zero) at the end of each instruction cycle. A new product is available for use after every instruction cycle, providing significant advantages in maximizing processing speed for real time signal processing.

Stack

The SPI contains a 4-level program stack for efficient program usage and interrupt handling.

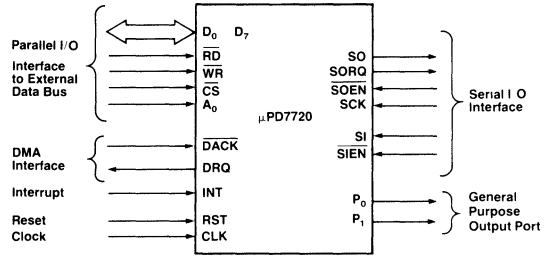
Interrupt

A single level interrupt is supported by the SPI. Upon sensing a high level on the INT terminal, a subroutine call to location 100H is executed. The EI bit of the status register is automatically reset to 0, thus disabling the interrupt facilities until reenabled under program control.

Input/Output

General

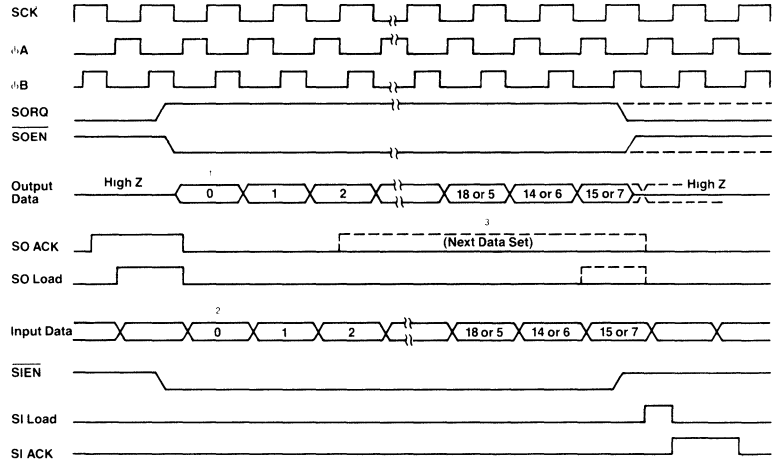
The NEC SPI has three communication ports; two serial and one 8-bit parallel, each with its own control lines for interface handshaking. The parallel port also includes DMA control lines (DRQ and $\overline{DACK}$) for high speed data transfer and reduced processor overhead. A general purpose 2-line output port rounds out a full complement of interface capability.



Serial I/O

The two shift registers (SI, SO) are software-configurable to single or double byte transfers. The shift registers are externally clocked (SCK) to provide a simple interface between the SPI and serial peripherals such as A/D and D/A converters, codecs, or other SPIs.

Serial I/O Timing



Notes: ① Data clocked out on falling edge of SCK
② Data clocked in on rising edge of SCK
③ Broken line denotes consecutive sending of next data

Parallel I/O

The 8-bit parallel I/O port may be used for transferring data or reading the SPI's status. Data transfer is handled through a 16-bit Data Register (DR) that is software-configurable for double or single byte data transfers. The port is ideally suited for operating with 8080, 8085, and 8086 processor buses and may be used with other processors and computer systems.

Parallel R/W Operation

$\overline{CS}$	A_0	$\overline{WR}$	$\overline{RD}$	Operation
1	X	X	X	No effect on internal operation. D_0-D_7 are at high impedance levels
X	X	1	1	
0	0	0	1	Data from D_0-D_7 are latched to DR ①
0	0	1	0	Contents of DR are output to D_0-D_7 ①
0	1	0	1	Illegal (SR is read only)
0	1	1	0	Eight MSBs of SR are output to D_0-D_7
0	X	0	0	Illegal (May not read and write simultaneously)

Note: ① Eight MSBs or 8 LSBs of data register (DR) are used depending on DR status bit (DRS) The condition of $\overline{DACK}$ = 0 is equivalent to A_0 = $\overline{CS}$ = 0

Status Register (SR)

MSB LSB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RQM	USF1	USF0	DRS	DMA	DRC	SOC	SIC	EI	0	0	0	0	0	P1	P0

The status register is a 16-bit register in which the 8 most significant bits may be read by the system's MPU for the latest I/O and processing status.

Status Register Flags

Flag	Description
RQM (Request for Master)	A read or write from DR to IDB sets RQM = 1. An external read (write) resets RQM = 0.
USF1 and USF0 (User Flags 1 and 0)	General purpose flags which may be read by an external processor for user defined signaling.
DRS (DR Status)	For 16-bit DR transfers (DRC = 0). DRS = 1 after first 8 bits have been transferred DRS = 0 after all 16 bits transferred.
DMA (DMA Enable)	DMA = 0 (Non-DMA transfer mode) DMA = 1 (DMA transfer mode).
DRC (DR Control)	DRC = 0 (16-bit mode) DRC = 1 (8-bit mode).
SOC (SO Control)	SOC = 0 (16-bit mode) SOC = 1 (8-bit mode).
SIC (SI Control)	SIC = 0 (16-bit mode) SIC = 1 (8-bit mode).
EI (Enable Interrupt)	EI = 0 (interrupts disabled) EI = 1 (interrupts enabled).
P1, P0 (Ports 0 and 1)	P0 and P1 directly control the state of output pins P0 and P1.

Instructions

The SPI has 3 types of instructions, all of which are one 23-bit word and execute in 250 ns.

Arithmetic/Move-Return (OP = 00/RT = 01)

	22 21	20 19	18 17 16 15	14	13 12	11 10 9	8	7 6 5 4	3 2 1 0
OP	0 0	P-Select	ALU	ASL	DP_L	DP_H-M	BDCR	SRC	DST
RT	0 1	Same as OP instruction							

OP/RT Instruction Field Specification

There are two instructions of this type, both of which are capable of executing all ALU functions listed in Table 2. The ALU functions operate on the value specified by the P-select field. (See Table 1.)

Besides the arithmetic functions these instructions can also modify (1) the RAM Data Pointer DP, (2) the Data ROM Pointer RP, and (3) move data along the on-chip data bus from a source register to a destination register (the possible source and destination registers are listed in Tables 7 and 8 respectively). The difference in the two instructions of this type is that RT executes a subroutine or interrupt return at the end of the instruction cycle while the OP does not.

Table 1. P-Select Field

Mnemonic	D_{20}	D_{19}	ALU Input
RAM	0	0	RAM
IDB	0	1	Internal Data Bus ①
M	1	0	M Register
N	1	1	N Register

Note: ① Any value on the on-chip data bus Value may be selected from any of the registers listed in Table 7 source register selections

Table 2. ALU Field

						Flags	SA1	SA0	CA	ZA	OVA1	OVA0
Mnemonic	D_{18}	D_{17}	D_{16}	D_{15}	ALU Function		SB1	SB0	CB	ZB	OVB1	OVB0
NOP	0	0	0	0	No Operation		–	–	–	–	–	–
OR	0	0	0	1	OR		X	↕	0	↕	0	0
AND	0	0	1	0	AND		X	↕	0	↕	0	0
XOR	0	0	1	1	Exclusive OR		X	↕	0	↕	0	0
SUB	0	1	0	0	Subtract		↕	↕	↕	↕	↕	↕
ADD	0	1	0	1	ADD		↕	↕	↕	↕	↕	↕
SBB	0	1	1	0	Subtract with Borrow		↕	↕	↕	↕	↕	↕
ADC	0	1	1	1	Add with Carry		↕	↕	↕	↕	↕	↕
DEC	1	0	0	0	Decrement A_{CC}		↕	↕	↕	↕	↕	↕
INC	1	0	0	1	Increment A_{CC}		↕	↕	↕	↕	↕	↕
CMP	1	0	1	0	Complement A_{CC} (1's Complement)		X	↕	0	↕	0	0
SHR1	1	0	1	1	1-bit R-Shift		X	↕	↕	↕	0	0
SHL1	1	1	0	0	1-bit L-Shift		X	↕	↕	↕	0	0
SHL2	1	1	0	1	2-bit L-Shift		X	↕	0	↕	0	0
SHL4	1	1	1	0	4-bit L-Shift		X	↕	0	↕	0	0
XCHG	1	1	1	1	8-bit Exchange		X	↕	0	↕	0	0

Notes: ↕ May be affected, depending on the results
– Previous status can be held
0 Reset
X Indefinite

Table 3. ASL Field

Mnemonic	D_{14}	A_{CC} Selection
ACCA	0	A_{CC} A
ACCB	1	A_{CC} B

Table 4. DP_L Field

Mnemonic	D_{13}	D_{12}	Low DP Modify (DP_3-DP_0)
DPNOP	0	0	No Operation
DPINC	0	1	Increment DP_L
DPDEC	1	0	Decrement DP_L
DPCLR	1	1	Clear DP_L

Table 5. DP_H-M Field

Mnemonic	D_{11}	D_{10}	D_9	High DP Modify
M0	0	0	0	Exclusive OR of DP_H (DP_6-DP_4) with the Mask defined by the three bits (D_{11}-D_9) of the DP_H-M field
M1	0	0	1	
M2	0	1	0	
M3	0	1	1	
M4	1	0	0	
M5	1	0	1	
M6	1	1	0	
M7	1	1	1	

Table 6. RPDCR Field

Mnemonic	D_8	RP Operation
RPNOP	0	No Operation
RPDEC	1	Decrement RP

Table 7. SRC Field

Mnemonic	D_7	D_6	D_5	D_4	Source Register
NON	0	0	0	0	No Register
A	0	0	0	1	A_{CC} A (Accumulator A)
B	0	0	1	0	A_{CC} B (Accumulator B)
TR	0	0	1	1	TR Temporary Register
DP	0	1	0	0	DP Data Pointer
RP	0	1	0	1	RP ROM Pointer
RO	0	1	1	0	RO ROM Output Data
SGN	0	1	1	1	SGN Sign Register
DR	1	0	0	0	DR Data Register
DRNF	1	0	0	1	DR No Flag ①
SR	1	0	1	0	SR Status Register
SIM	1	0	1	1	SI Serial in MSB ②
SIL	1	1	0	0	SI Serial in LSB ③
K	1	1	0	1	K Register
L	1	1	1	0	L Register
MEM	1	1	1	1	RAM

Notes: ① DR to IDB, RQM not set In DMA, DRQ not set
② First bit in goes to MSB, last bit to LSB
③ First bit in goes to LSB, last bit to MSB (bit reversed)

Table 8. DST Field

Mnemonic	D_3	D_2	D_1	D_0	Destination Register
@NON	0	0	0	0	No Register
@A	0	0	0	1	A_{CC} A (Accumulator A)
@B	0	0	1	0	A_{CC} B (Accumulator B)
@TR	0	0	1	1	TR Temporary Register
@DP	0	1	0	0	DP Data Pointer
@RP	0	1	0	1	RP ROM Pointer
@DR	0	1	1	0	DR Data Register
@SR	0	1	1	1	SR Status Register
@SOL	1	0	0	0	SO Serial Out LSB ①
@SOM	1	0	0	1	SO Serial Out MSB ②
@K	1	0	1	0	K (Mult)
@KLR	1	0	1	1	IDB → K, ROM → L ③
@KLM	1	1	0	0	Hi RAM → K, IDB → L ④
@L	1	1	0	1	L (Mult)
@NON	1	1	1	0	No Register
@MEM	1	1	1	1	RAM

Notes: ① LSB is first bit out
② MSB is first bit out
③ Internal data bus to K and ROM to L register
④ Contents of RAM address specified by DP_6 = 1, (i e , 1, DP_5, DP_4-DP_0) is placed in K register IDB is placed in L

Jump/Call/Branch

JP Instruction Field Specification

	22 21	20 19 18	17 16 15 14 13	12 11 10 9 8 7 6 5 4	3 2 1 0
JP	10	BRCH	CND	NA	

Three types of program counter modifications are accommodated by the processor and are listed in Table 9. All the instructions, if unconditional or if the specified condition is true, take their next program execution address from the Next Address field (NA); otherwise PC = PC + 1.

Table 9. BRCH Field

D_{20}	D_{19}	D_{18}	Branch Instruction
1	0	0	Unconditional jump
1	0	1	Subroutine call
0	1	0	Conditional jump

For the conditional jump instruction, the condition field specifies the jump condition. Table 10 lists all the instruction mnemonics of the Jump/Call/Branch codes.

Load Data (LDI)

LD Instruction Field Specification

22 21	20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
LD	11	ID DST

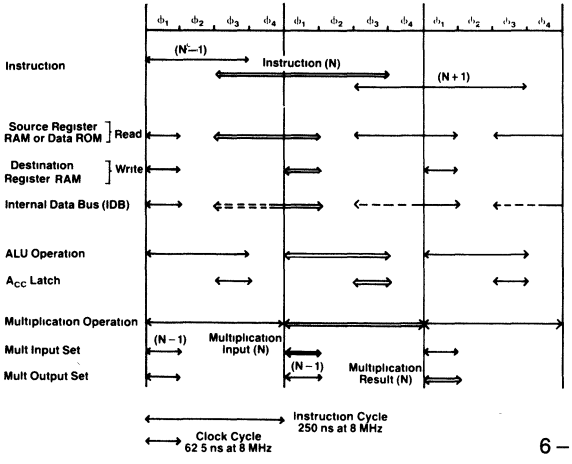
The Load Data instruction will take the 16-bit value contained in the Immediate Data field (ID) and place it in the location specified by the Destination field (DST) (see Table 8).

Table 10. BRCH/CND Fields

Mnemonic	D_{20}	D_{19}	D_{18}	D_{17}	D_{16}	D_{15}	D_{14}	D_{13}	Conditions①
JMP	1	0	0	0	0	0	0	0	No Condition
CALL	1	0	1	0	0	0	0	0	No Condition
JNCA	0	1	0	0	0	0	0	0	CA = 0
JCA	0	1	0	0	0	0	0	1	CA = 1
JNCB	0	1	0	0	0	0	1	0	CB = 0
JCB	0	1	0	0	0	0	1	1	CB = 1
JNZA	0	1	0	0	0	1	0	0	ZA = 0
JZA	0	1	0	0	0	1	0	1	ZA = 1
JNZB	0	1	0	0	0	1	1	0	ZB = 0
JZB	0	1	0	0	0	1	1	1	ZB = 1
JNOVA0	0	1	0	0	1	0	0	0	OVA0 = 0
JOVA0	0	1	0	0	1	0	0	1	OVA0 = 1
JNOVB0	0	1	0	0	1	0	1	0	OVB0 = 0
JOVB0	0	1	0	0	1	0	1	1	OVB0 = 1
JNOVA1	0	1	0	0	1	1	0	0	OVA1 = 0
JOVA1	0	1	0	0	1	1	0	1	OVA1 = 1
JNOVB1	0	1	0	0	1	1	1	0	OVB1 = 0
JOVB1	0	1	0	0	1	1	1	1	OVB1 = 1
JNSA0	0	1	0	1	0	0	0	0	SA0 = 0
JSA0	0	1	0	1	0	0	0	1	SA0 = 1
JNSB0	0	1	0	1	0	0	1	0	SB0 = 0
JSB0	0	1	0	1	0	0	1	1	SB0 = 1
JNSA1	0	1	0	1	0	1	0	0	SA1 = 0
JSA1	0	1	0	1	0	1	0	1	SA1 = 1
JNSB1	0	1	0	1	0	1	1	0	SB1 = 0
JSB1	0	1	0	1	0	1	1	1	SB1 = 1
JDPL0	0	1	0	1	1	0	0	0	DP_L = 0
JDPLF	0	1	0	1	1	0	0	1	DP_L = F (HEX)
JNSIAK	0	1	0	1	1	0	1	0	SI ACK = 0
JSIAK	0	1	0	1	1	0	1	1	SI ACK = 1
JNSOAK	0	1	0	1	1	1	0	0	SO ACK = 0
JSOAK	0	1	0	1	1	1	0	1	SO ACK = 1
JNRQM	0	1	0	1	1	1	1	0	RQM = 0
JRQM	0	1	0	1	1	1	1	1	RQM = 1

Note: ① BRCH or CND values not in this table are prohibited

Instruction Timing (Four Phase-Internal Clock)



Instruction Timing

To control the execution of instructions, the external 8-MHz clock is divided into a four-phase, nonoverlapping clock. Execution begins at the rising edge of $\phi 3$ and ends at the falling edge of $\phi 2$. The ALU commences operation at the rise of $\phi 1$, and completes all operations at the fall of $\phi 3$.

Once an instruction-ROM address is available at the rise of $\phi 3$, the instruction is latched, and the source register and RAM address are determined so that data may be put on the internal bus by the fall of $\phi 4$. The ALU input is latched at the rise of $\phi 1$, and the output is available for accumulator latch at the rise of $\phi 3$. The cycle then repeats.

The multiplier takes its input at the rise of $\phi 1$, and its results are available in 250 ns, at the rise of the next $\phi 1$.

Absolute Maximum Ratings*

T_a = 25°C	
Voltage (V_{CC} Pin)	−0.5 to +7.0V ①
Voltage, Any Input	−0.5 to +7.0V ①
Voltage, Any Output	−0.5 to +7.0V ①
Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C

Note: ① With respect to GND

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} +0.5	V	
CLK Low Voltage	$V\phi_L$	−0.5		0.45	V	
CLK High Voltage	$V\phi_H$	3.5		V_{CC} +0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{LIL}			−10	μA	V_{IN} = 0V
Input Load Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Output Float Leakage	I_{LOL}			−10	μA	V_{OUT} = 0.47V
Output Float Leakage	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		180	280	mA	

Capacitance

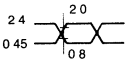
		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
CLK, SCK Input Capacitance	$C\phi$			20	pF	
Input Pin Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Output Pin Capacitance	C_{OUT}			20	pF	

AC Characteristics

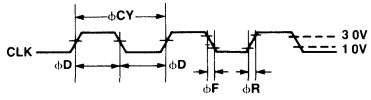
T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

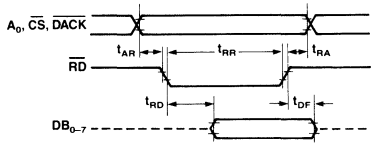
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK Cycle Time	ϕCY	122		2000	ns	①
CLK Pulse Width	ϕD	60			ns	
CLK Rise Time	ϕR			10	ns	①
CLK Fall Time	ϕF			10	ns	①
Address Setup Time for $\overline{RD}$	t_{AR}	0			ns	
Address Hold Time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{RD}$	t_{RD}			150	ns	C_L = 100 pF
Read to Data Floating	t_{DF}	10		100	ns	C_L = 100 pF
Address Setup Time for $\overline{WR}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	250			ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$, Recovery Time	t_{RV}	250			ns	②
DRQ Delay	t_{AM}			150	ns	
$\overline{DACK}$ Delay Time	t_{DACK}	1			ϕD	②
SCK Cycle Time	t_{SCY}	480		DC	ns	
SCK Pulse Width	t_{SCK}	230			ns	
SCK Rise/Fall Time	t_{RSC}			20	ns	①
SORQ Delay	t_{DRQ}	30		150	ns	C_L = 100 pF
$\overline{SOEN}$ Setup Time	t_{SOC}	50			ns	
$\overline{SOEN}$ Hold Time	t_{CSO}	30			ns	
SO Delay from SCK = LOW	t_{DCK}			150	ns	
SO Delay from SCK with SORQ ↑	t_{DZRQ}	20		300	ns	②
SO Delay from SCK	t_{DZSC}	20		300	ns	②
SO Delay from $\overline{SOEN}$	t_{DZE}	20		180	ns	②
$\overline{SOEN}$ to SO Floating	t_{HZE}	20		200	ns	②
SCK to SO Floating	t_{HZSC}	20		300	ns	②
SO Delay from SCK with SORQ ↓	t_{HZRQ}	70		300	ns	②
$\overline{SIEN}$, SI Setup Time	t_{DC}	55			ns	②
$\overline{SIEN}$, SI Hold Time	t_{CD}	30			ns	
P_0, P_1 Delay	t_{DP}			ϕCY +150	ns	
RST Pulse Width	t_{RST}	4			ϕCY	
INT Pulse Width	t_{INT}	8			ϕCY	

Notes: ① Voltage at measuring point of timing 1 0V and 3 0V
② Voltage at measuring point of AC Timing
V_{IL} = V_{OL} = 0 8V
V_{IH} = V_{OH} = 2 0V
Input Waveform of AC Test (except CLK, SCK)



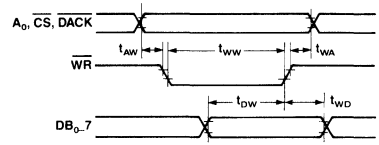
Timing Waveforms



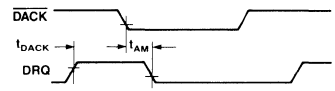


Timing Waveforms (Cont.)

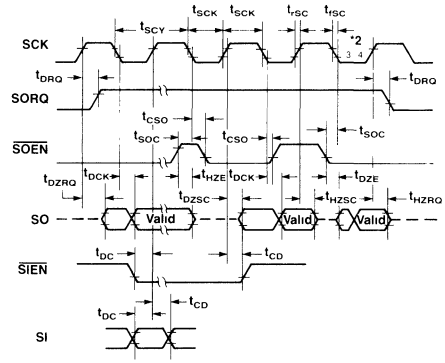
WRITE Operation



DMA Operation



Serial Timing



Notes. ① For SO timing, the data at rising edge of SCK is valid and the other data is invalid In set-up hold time of data for SCK, the most strict specifications are the following
setup = t_{SCK} − t_{DCK}
hold = t_{HZRQ}
② Voltage at measuring point of t_{rsc} and t_{fsc} for SCK timing
③ 3 0V ④ 1 0V

Development Tools

For software development, editing, debugging, and assembly into object code, the NDS Development System, designed and manufactured by NEC Electronics U.S.A. Inc., is available. The ASM77 Cross-Assembler and SIM77 Simulator for analyzing development code and I/O timing characteristics are available for both the NDS and for other systems supporting CP/M (®Digital Research Corp.) or ISIS-II (®Intel Corp.) operating systems. Additionally, the ASM77 Cross-Assembler is offered in Fortran for VAX systems under VMS (®Digital Equipment Corp.).

Once software development is complete, the code can be completely evaluated and debugged in hardware with the Evakit-7720 Evaluation System. The Evakit provides true in-circuit real time emulation of the SPI for debugging and demonstrating your final system design. Code may be down-loaded to the Evakit from a development system via an RS232 port. The Evakit also serves to program the μPD77P20, a full-speed EPROM version of the SPI. A demonstration mask ROM chip, containing some common digital filtering routines, including N-stage IIR (biquadratic) and FIR (transversal) filters, is available to test hardware interfaces to the SPI.

Further operational details of the SPI can be found in the μPD7720 Signal Processing Interface Technical Manual.

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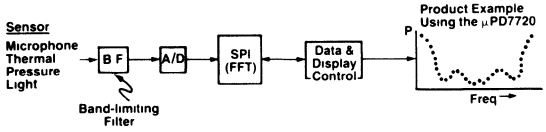
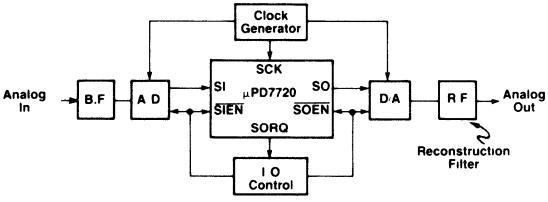
Operation of the SPI development tools is described in the Cross-Assembler User Manual, the Simulator Operating Manual, the Evakit-7720 Operation Manual, and the NEC Development Systems Users' Manual.

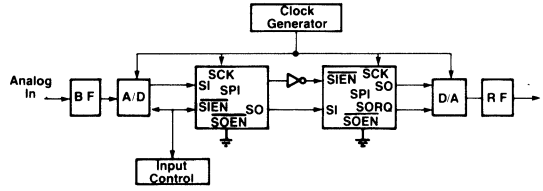
Spectrum Analysis System



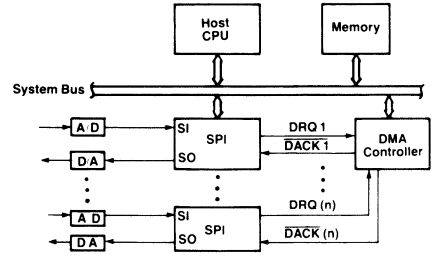
An Analog-to-Analog Digital Processing System Using a Single SPI



A Signal Processing System Using Cascaded SPIs & Serial Communication



A Signal Processing System Using SPI(s) as a Complex Computer Peripheral



Package Outlines

For information, see Package Outline Section 7.

Ceramic, μPD7720D

μPD77P20
UV ERASABLE SIGNAL PROCESSING INTERFACE (SPI)

Description

The μPD77P20 is an ultraviolet erasable and electrically programmable (EPROM) version of the μPD7720 signal processing interface (SPI). Functionally, the two parts are identical. Program and data ROM, masked for the μPD7720, are implemented in EPROM for the μPD77P20. The μPD77P20 is useful in prototye applications or in systems where quantities are insufficient for masked ROM development. For a complete functional description consult the μPD7720 Technical Manual.

Applications

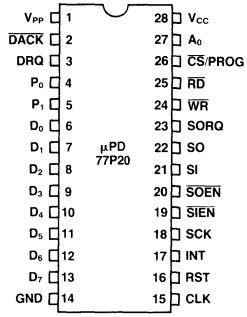
- ☐ Speech synthesis and analysis
- ☐ Digital filtering
- ☐ Fast Fourier transforms (FFT)
- ☐ Dual-tone Multifrequency (DTMF) transmitters/receivers
- ☐ High-speed data modems
- ☐ Equalizers
- ☐ Adaptive control
- ☐ Sonar/radar image processing
- ☐ Numerical processing

Features

- ☐ Internal ultraviolet EPROM (instruction and data)
- ☐ Programmable with single pulse
- ☐ Compatible with μPD7720
- ☐ 8MHz clock/250ns instruction execution
- ☐ 16-bit data word
- ☐ Multioperation instructions for optimizing program execution
- ☐ Large memory capacities
  - – Programmable program ROM 512 × 23 bits
  - – Programmable data ROM 512 × 13 bits
  - – Data RAM 128 × 16 bits
- ☐ Fast (250ns) 16 × 16-bit parallel multiplier with 31-bit result
- ☐ Dual accumulators
- ☐ Four-level subroutine stack for program efficiency
- ☐ Multiple I/O capabilities
  - – Serial
  - – Parallel
  - – DMA
- ☐ Fully bus compatible with most microprocessors, including:
  - – μPD8080
  - – μPD8085
  - – μPD8086
  - – μPD780 (Z80)™
- ☐ +5V power supply
- ☐ NMOS technology
- ☐ 28-pin dip package

TM Z80 is a registered trademark of Zilog Inc

Pin Configuration

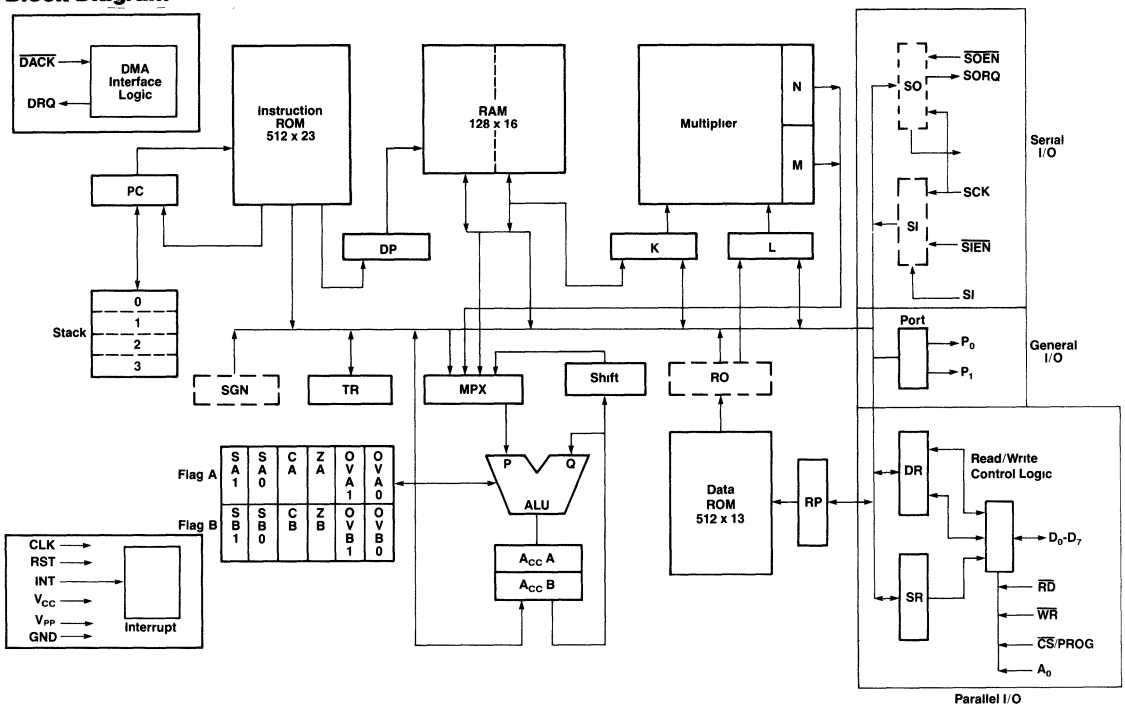


Pin Identification

Pin No.	Symbol	I/O	Function
1	V_{PP}	I	Programming voltage
2	$\overline{DACK}$	I	DMA Request Acknowledge. Indicates to the μPD7720 that the data bus is ready for a DMA transfer. ($\overline{DACK} = \overline{CS} \bullet A_0 = 0$)
3	DRQ	O	DMA Request signals that the μPD7720 is requesting a data transfer on the data bus.
4, 5	P_0, P_1	O	P_0, P_1 are general purpose output control lines
6–13	D_0–D_7	I/O Three-state	Port for data transfer between the data or status register and the data bus.
14	GND		
15	CLK	I	Single phase Master Clock input.
16	RST	I	Reset initializes the μPD7720 internal logic and sets the PC to 0.
17	INT	I	Interrupt. A low to high transition on this pin will (if interrupts are enabled by the program) execute a call instruction to location 100H.
18	SCK	I	Serial Data Input/Output Clock. A serial data bit is transferred when this pin is high.
19	$\overline{SIEN}$	I	Serial Input Enable. This line enables the shift clock to the serial input register.
20	$\overline{SOEN}$	I	Serial Output Enable. This pin enables the shift clock to the serial output register
21	SI	I	Serial Data Input. This pin inputs 8- or 16-bit serial data words from an external device such as an A/D converter.
22	SO	O	Serial Data Output. This pin outputs 8- or 16-bit data words to an external device such as a D/A converter.
23	SORQ	O Three-state	Serial Data Output Request. Specifies to an external device that the serial data register has been loaded and is ready for output. SORQ is reset when the entire 8- or 16-bit word has been transferred.
24	$\overline{WR}$	I	Write control signal writes the contents of the data bus into the data register.
25	$\overline{RD}$	I	Read control signal. Enables an output to the data port from the data or status register.
26	$\overline{CS}$/PROG	I	Chip Select. Enables data transfer with data or status port with $\overline{RD}$ or $\overline{WR}$.
27	A_0	I	Selects data register for read/write (low) or status register for read (high).
28	V_{CC}		+5V power

6

Block Diagram



Mode Selection

Mode \ Pins	$\overline{CS}$/PROG	V_{PP}	V_{CC}	Outputs
Instruction ROM program	V_{IH}	V_{PP}	+5V	D_{IN}
Data ROM program	V_{IH}	V_{PP}	+5V	D_{IN}
Instruction ROM read	V_{IL}	V_{CC}	+5V	D_{OUT}
Data ROM read	V_{IL}	V_{CC}	+5V	D_{OUT}
Operation	V_{IL}	V_{CC}	+5V	D_{IN}, D_{OUT}
	V_{IH}			High Z

Absolute Maximum Ratings*

T_a = 25°C	
Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_I	−0.3V to +7.0V
Output Voltage, V_O	−0.3V to +7.0V
Operating Temperature, T_{OPT}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C
Supply Voltage, V_{PP}	−0.3V to +22V

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = −10°C +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Input CLK Voltage Low	$V_{\phi L}$	−0.5		0.45	V	
Input CLK Voltage High	$V_{\phi H}$	3.5		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL}= 2.0mA
Output High Voltage	V_{OH}	2.4			V	I_{OH}= −400μA
Input Load Current	I_{LIL}			−10	μA	V_{IN}= 0V
Input Load Current	I_{LIH}			10	μA	V_{IN}= V_{CC}
Output Float Leakage	I_{LOL}			−10	μA	V_{OUT} = 0.47V
Output Float Leakage	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Power Supply Current	I_{CC}		270	350	mA	
V_{PP} Current	I_{PP}			70	mA	Program Mode Max Pulse Current①
		0.5		3.0		Program Verify, Inhibit②

Notes: ① V_{PP} = (21 ± 0.5) V
② for K-level parts, $V_{PP}MAX = V_{CC}MAX + 0.25V$, $V_{PP}MIN = V_{CC}MIN - 0.85V$
for E-level and P-level parts, $V_{PP} = V_{CC}$

AC Operating Characteristics

T_a = −10°C to +70°C; V_{CC} = +5V ± 5%; K-level parts, $V_{PP}MAX = V_{CC}MAX + 0.25V$; $V_{PP}MIN = V_{CC}MIN - 0.85V$; E-level and P-level parts, $V_{PP} = V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK Cycle Time	ϕCY	122		2000	ns	
CLK Pulse Width	ϕD	60			ns	
CLK Rise Time	ϕr			10	ns	Voltage at measuring point of timing 1.0V and 3.0V
CLK Fall Time	ϕf			10	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Setup Time for $\overline{RD}$	t_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time for $\overline{RD}$	t_{RA}	0			ns	
$\overline{RD}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{RD}$	t_{RD}			150	ns	C_L = 100pF
Read to Data Floating	t_{DF}	10		100	ns	C_L = 100pF
A_0, $\overline{CS}$, $\overline{DACK}$ Setup Time for $\overline{WR}$	t_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time for $\overline{WR}$	t_{WA}	0			ns	
$\overline{WR}$ Pulse Width	t_{WW}	250			ns	
Data Setup Time for $\overline{WR}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WR}$	t_{WD}	0			ns	
$\overline{RD}$, $\overline{WR}$ Recovery Time	t_{RV}	250			ns	
DRQ Delay Time	t_{AM}			150	ns	
$\overline{DACK}$ Delay Time	t_{DACK}	1			ϕD	
SCK Cycle Time	t_{SCY}	480		DC	ns	
SCK Pulse Width	t_{SCK}	230			ns	
SCK Rise Time	t_{rSC}			20	ns	Voltage at measuring point of timing 1.0V and 3.0V
SCK Fall Time	t_{fSC}			20	ns	
SORQ Delay	t_{DRQ}	30		150	ns	C_L = 100pF
$\overline{SOEN}$ Setup Time for SCK	t_{SOC}	50			ns	
$\overline{SOEN}$ Hold Time for SCK	t_{CSO}	30			ns	
SO Delay	t_{DCK}			150	ns	
SO Delay from SCK with SORQ	t_{DZRQ}	20		300	ns	
SO Delay from SCK	t_{DZSC}	20		300	ns	
SO Delay from $\overline{SOEN}$	t_{DZE}	20		180	ns	
$\overline{SOEN}$ to SO Floating	t_{HZE}	20		200	ns	
SCK to SO Floating	t_{HZSC}	20		300	ns	
SO Delay from SCK with SORQ	t_{HZRQ}	70		300	ns	
$\overline{SEIN}$, SI Setup Time	t_{DC}	55			ns	
$\overline{SEIN}$, SI Hold Time	t_{CD}	30			ns	
P_0, P_1 Delay	t_{DP}			$\phi CY + 150$	ns	
RST Pulse Width	t_{RST}	4			ϕCY	
INT Pulse Width	t_{INT}	8			ϕCY	

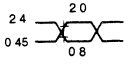
Note: Voltage at measuring point of AC timing
$V_{IL} = V_{OL} = 0.8V$
$V_{IH} = V_{OH} = 2.0V$

Capacitance

T_a = 25°C; V_{CC} = 0V

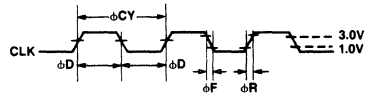
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK, SCK Capacitance	C_ϕ			20	pF	f_C = 1MHz
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Input Waveform of AC Test (except CLK, SCK)

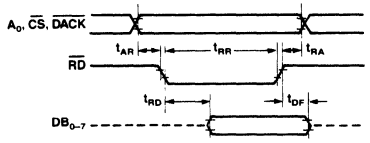


Timing Waveforms

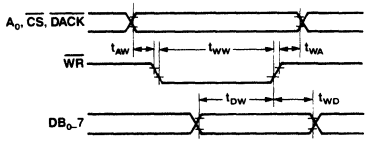
Clock



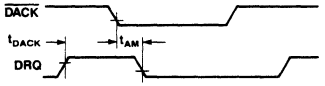
Read Operation



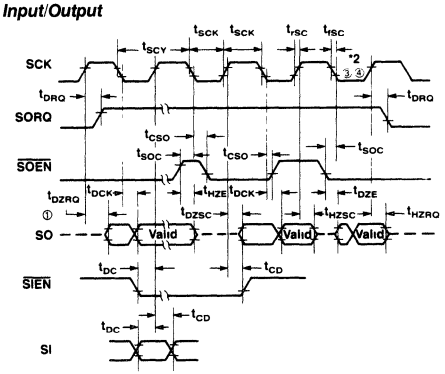
Write Operation



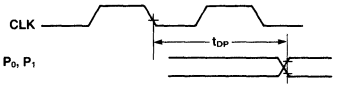
DMA Operation



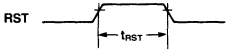
Serial Input/Output



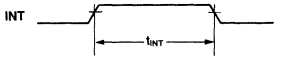
Port Output



Reset



Interrupt



Notes: ① For SO timing, the data at rising edge of SCK is valid and the other data is invalid In set-up hold time of data for SCK, the most strict specifications are the following
setup = $t_{SCK} - t_{DCK}$
hold = t_{HZRQ}
② Voltage at measuring point of t_{rSC} and t_{fSC} for SCK timing
③ 3.0V ④ 1.0V

μPD77P20

Function

The μPD77P20 operates from a single +5V power supply and accordingly, can be used in any μPD7720 masked ROM application.

Programming of the μPD77P20 is achieved with a single 50ms TTL pulse. Total programming time for the 11,776 bits of instruction EPROM and also for the 6,630 bits data EPROM is 26 seconds.

Erasure of the μPD77P20 programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 angstroms (Å). It should also be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the μPD77P20. Consequently, if the μPD77P20 is to be exposed to these types of lighting conditions for long periods of time its window should be masked to prevent unintentional erasure.

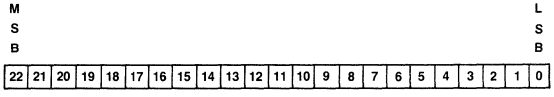
The recommended erasure procedure for the μPD77P20 is exposure to ultraviolet light with wavelengths of 2,537 angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should not be less than 15W-sec/cm^2. The erasure time is approximately 20 minutes using an ultraviolet lamp with a power rating of 12,000μW/cm^2.

During erasure the μPD77P20 should be placed within 1 inch of the lamp tubes. If the lamp tubes have filters the filters should be removed before erasure.

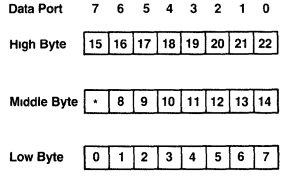
Configuration

Data transfer for programming and reading the internal ROM is partitioned into three bytes for each 23-bit wide instruction location and into two bytes for each 13-bit wide data location. Partitioning of data transfer into and out of the data port is as follows:

Instruction ROM

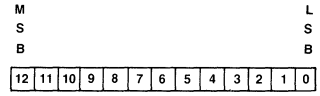


The instruction ROM data is transferred through the data port as a high byte, middle byte, and low byte. Bit 7 of the middle byte should be assigned a value of zero. Data is presented to the data port in a bit-reversed format. The LSB through the MSB of an instruction ROM byte is applied to the MSB through the LSB of the data port, respectively.

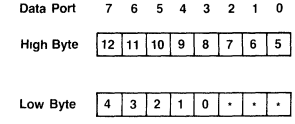


Note: * = Set to zero as dummy data

Data ROM



The data ROM data is transferred through the data port as a low byte and a high byte. Bits 0, 1, and 2 of the low byte should be assigned a value of zero. Data is presented to the data port in corresponding order. The MSB through the LSB of a data ROM byte is applied to the MSB through the LSB of the data port, respectively.



Note: * = Set to zero as dummy data

Initially and after each erasure, all bits of the μPD77P20 are in the zero state.

Operation

In order to read or write the instruction or data ROMs the mode of operation of the μPD77P20 must be initially set. At the RST trailing edge, the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ should be logical zero and the $\overline{DACK}$, A_0, and SI signals should be set to determine the mode of operation accordingly.

$\overline{DACK}$	A_0	SI	
0	0	0	Write mode instruction and data ROMs
0	0	1	Read the instruction ROM
0	1	0	Read the data ROM

Once set in any of these modes the μPD77P20 will remain in the selected mode. To transfer to another mode a reset is required.

Write Mode

The individual instruction ROM and data ROM bytes are specified by control signals $\overline{RD}$, A_0, SI, and INT. Before writing the EPROM location, the bytes should be loaded accordingly.

$\overline{RD}$	A_0	SI	INT	
1	0	0	1	Write instruction byte, high
1	0	1	0	Write instruction byte, middle
1	0	1	1	Write instruction byte, low
1	1	0	0	Write data byte, low
1	1	0	1	Write data byte, high

Read Mode

The instruction ROM and data ROM bytes are specified by the control signals $\overline{RD}$, A_0, SI, and INT. Reading is accomplished by setting the control signals accordingly.

$\overline{RD}$	A_0	SI	INT	
0	0	0	1	Read instruction byte, high
0	0	1	0	Read instruction byte, middle
0	0	1	1	Read instruction byte, low
1	0	0	0	Read data byte, high and low

Addressing

The instruction ROM and data ROM are addressed by the 9-bit program counter and the 9-bit ROM pointer respectively. The PC is reset to 000H and is automatically incremented to the end address 1FFH. The RP is reset to 1FFH and is automatically decremented to 000H.

Programming

Programming begins by erasing all data and consequently having all bits in the low (0) level state. Data is then entered by programming a high (1) level into the chosen bit locations. Both instruction ROM and data ROM should be programmed since they cannot be erased independently. Both instruction ROM and data ROM programming modes are entered in the same manner. The device must be initially reset before it can be placed into the programming mode. After being reset the $\overline{WR}$ signal and all other inputs ($\overline{RD}$, $\overline{CS}$/PROG, $\overline{DACK}$, A_0, SI, and INT) should be a TTL low (0) signal T_{RS} prior to the falling edge of RST. $\overline{WR}$ is then held for T_{RH} before being set to a TTL high (1) level signal. The device is now in a programming mode and will stay in this mode allowing ROM locations to be sequentially programmed.

Programming Mode—Instruction ROM

Instruction ROM locations are sequentially programmed from address 000H to address 1FFH. The location address is incremented by the application of CLK for a duration of T_{CY}. Data bytes for each location as specified by control signals $\overline{RD}$, A_0, SI, and INT are clocked into the device by the falling edge of $\overline{RD}$. After the three bytes have been loaded into the device, V_{PP} is raised to 21V ± 0.5V T_{VS} prior to $\overline{CS}$/PROG transitioning to a TTL high (1) level signal. V_{PP} is held for the duration of T_{PW} plus T_{VH} before returning to the V_{CC} level. After T_{AH} the instruction ROM address can be incremented to program the next location.

Programming Mode—Data ROM

Data ROM locations are sequentially programmed from address 1FFH to address 000H. The location address is decremented by the application of CLK for T_{CY}. The data bytes for each location as specified by control signals $\overline{RD}$, A_0, SI, and INT are clocked into the device by the falling edge of $\overline{RD}$. After the two bytes have been loaded into the device, V_{PP} is raised to 21V ± 0.5V T_{VS} prior to $\overline{CS}$/PROG transitioning to a TTL high (1) level signal. V_{PP} is held for the duration of T_{PW} plus T_{VH} before returning to the V_{CC} level. After T_{AH} the data ROM address can be decremented to program the next location.

Read Mode

A read should be performed to verify that the data was programmed correctly. Prior to entering read mode the device must be reset.

Read Mode—Instruction ROM

This mode is entered by holding the $\overline{WR}$ signal at a TTL low (0) level with the SI signal at a TTL high (1) level and all other specified inputs ($\overline{RD}$, $\overline{CS}$/PROG, $\overline{DACK}$, A_0, INT) at TTL low (0) levels for T_{RS} prior to the falling edge of RST. $\overline{WR}$ is then held for T_{RH} before being set to a TTL high (1) level. The device is now in the instruction ROM read mode and will stay in this mode until reset. Instruction ROM locations are sequentially read from address 000H through 1FFH. Application of CLK for T_{CY} will increment the location address. The three data bytes will be read as specified by the control signals $\overline{RD}$, A_0, SI, and INT.

Read Mode—Data ROM

This mode is entered by holding the $\overline{WR}$ signal at a TTL low (0) level with the A_0 signal at a TTL high (1) level and all other specified inputs ($\overline{RD}$, $\overline{CS}$/PROG, $\overline{DACK}$, SI, INT) at TTL low (0) levels for T_{RS} prior to the falling edge of RST. $\overline{WR}$ and A_0 are then held for T_{RH} prior to the falling edge of RST. $\overline{WR}$ and A_0 are then held for T_{RH} before being set to a TTL high (1) level and TTL low (0) level respectively. The device is now in the data ROM read mode and will stay in this mode until it is reset. Data ROM locations are sequentially read from address 1FFH through 000H. Application of CLK for T_{CY} will decrement the location address. After decrementing the location address, the low byte of the current location will be available at the data port subsequent to a T_{CKD} delay. Application of $\overline{RD}$ will present the high byte T_{RD} from the falling edge of the $\overline{RD}$ pulse. $\overline{RD}$ is then applied for T_{VR} to complete reading of the current location.

Programming Operation, AC Characteristics

T_a = 25° ± 5 °C, V_{CC} = 5V ± 5%, V_{PP} = 21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK Cycle Time	T_{CY}	240			ns	
RST Pulse Width	T_{RST}	4			T_{CY}	
RST Setup Time	T_{RS}	1			μs	
RST Hold Time	T_{RH}	6			μs	
CLK Setup Time	T_{CLKS}	2			μs	
Data Setup Time	T_{DS}	1			μs	
Data Hold Time	T_{DH}	100			ns	
Control Signal Setup Time	T_{CSS}	100			ns	
Control Signal Hold Time	T_{CSH}	100			ns	
Read Pulse Width	T_{RW}	1			μs	
Write Data Setup Time	T_{WDS}	100			ns	
Write Data Hold Time	T_{WDH}	2			μs	
V_{PP} Setup Time	T_{VS}	2			μs	
V_{PP} Hold Time	T_{VH}	2			μs	
Address Hold Time	T_{AH}	200			ns	
Program Pulse Width during Programming	T_{PW}	45	50	55	ms	

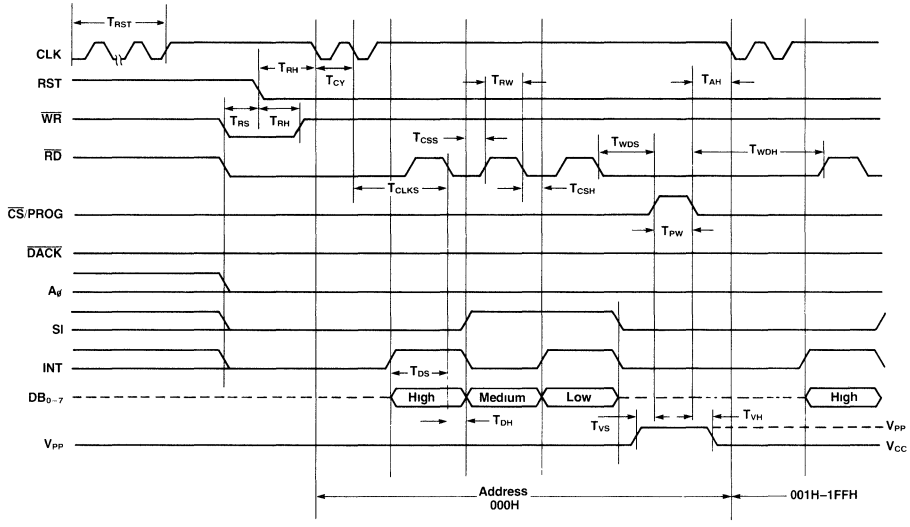
Read Operation, AC Characteristics

T_a = 25°C ± 5°C; V_{CC} = 5V ± 5%; V_{PP} = V_{CC} ± 5%; K-level parts, $V_{PP}MAX$ = $V_{CC}MAX$ + 0.25V; $V_{PP}MIN$ = $V_{CC}MIN$ − 0.85V; E-level and P-level parts, V_{PP} = V_{CC}

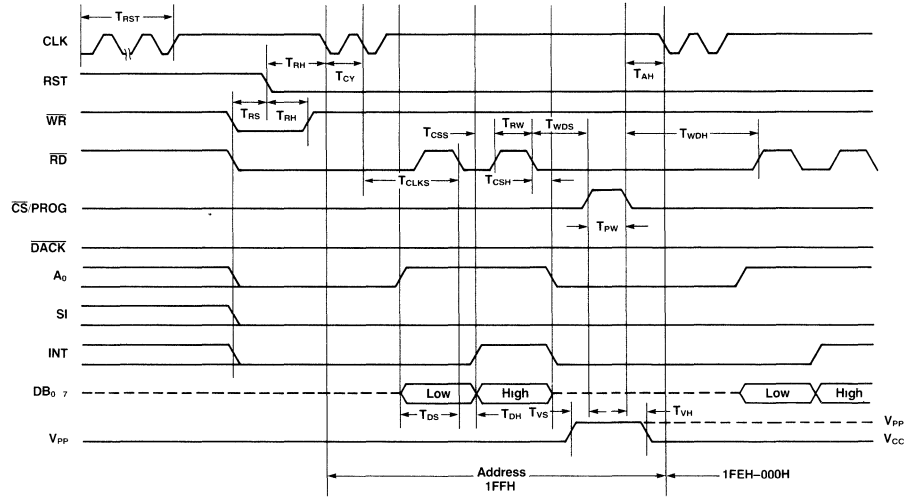
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output Delay from CLK	T_{CKD}			1	μs	
Output Delay from Control Signal	T_{CSD}			1	μs	
Output Hold Time from Control Signal	T_{CSH}	0			ns	
Control Signal Pulse Width	T_{CSW}	1			μs	
Recovery Time Between Control Signal	T_{RV}	500			ns	
$\overline{RD}$ to Output Delay	T_{RD}			150	ns	
$\overline{RD}$ to Output Float	T_{DF}	10			ns	

6

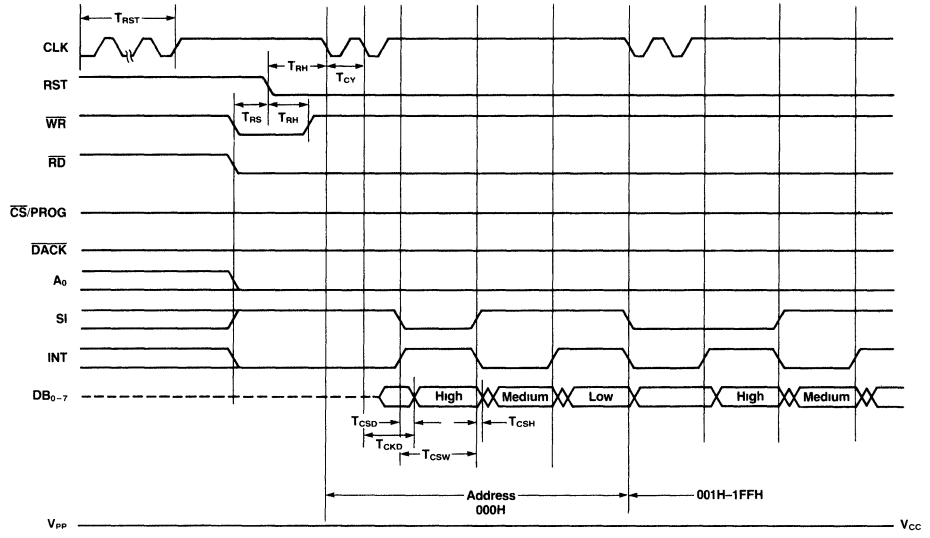
Write Mode of Instruction ROM



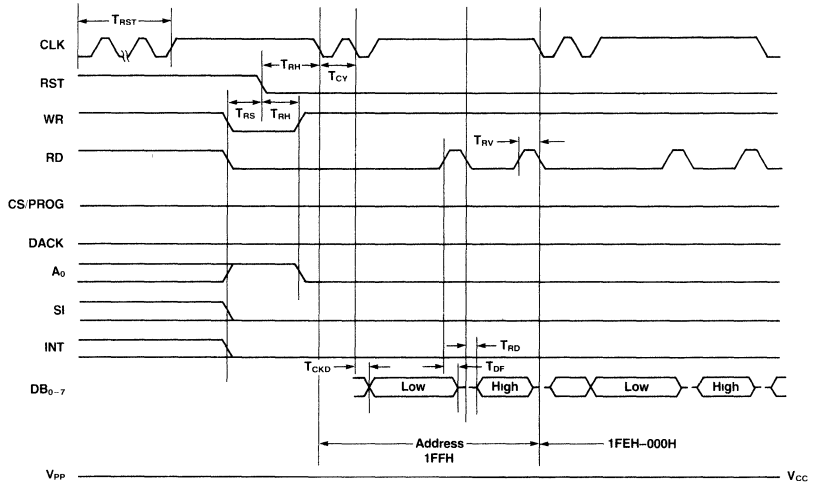
Write Mode of Data ROM



Read Mode of Instruction ROM



Read Mode of Data ROM



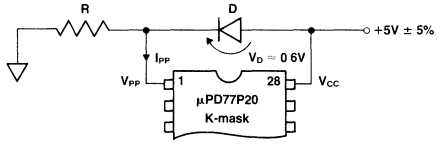
6

Operation Mode

The μPD77P20 may be utilized in an operation mode after the instruction ROM and data ROM have been programmed. Operation modes are invoked in slightly different manners depending on the mask level and the specific mask lot within the series.

K-mask

The μPD77P20 K-mask requires that V_{PP} be supplied in a different manner than for the E-mask for an operation mode only. V_{PP} voltage should be supplied in the following fashion:



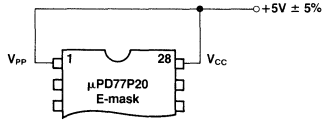
$$V_{PP} = V_{CC} - (0.6 \pm 0.25)V$$
$$I_{PP} \quad \text{Min} = 0.5mA$$
$$\text{Max} = 3.5mA$$

A silicon junction diode of 0.6V forward voltage (V_F) should be used. R should be 800Ω to 1.8KΩ to satisfy the V_{PP} and I_{PP} requirements.

Parts before lot K21031 (excluding K21031) require a NOP (No Operation) to be programmed into instruction ROM location 000H in order to properly operate at 8MHz. For parts with lot numbers equal to or greater than K21031 location 000H of the instruction ROM does not require a NOP for 8MHz operation.

E-mask and P-mask

The μPD77P20 E-mask and P-mask requires that V_{PP} be connected directly to V_{CC} for an operation mode as shown. The P-mask version is packaged as a cerdip. Note that these versions are also compatible with the K-mask V_{PP} specifications.



No additional constraints apply to these versions. For both versions adequate power supply decoupling should be provided.

Package Outlines

For information, see Package Outline Section 7.

Ceramic, μPD77P20D, has quartz window

PRELIMINARY

μPD7751
ADPCM VOICE SYNTHESIS LSI

Description

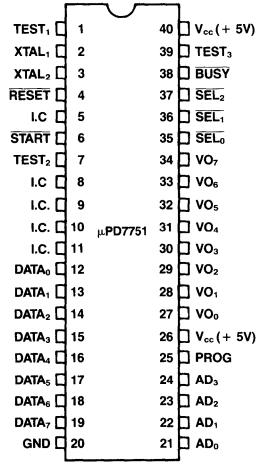
The μPD7751 is an LSI device for high quality voice synthesis applications. Based on an ADPCM algorithm (adaptive differential PCM), the device decodes voice data stored in external ROM and outputs a synthesized voice signal. This output may be sent to a conventional audio speaker through an 8-bit D/A converter, filter and power amplifier.

Eight messages can be stored per 128K-bit memory bank, at compressed bit rates of 14 to 20K-bits/second. Efficient encoding of silences within a message allows further compression of digitized voice signals. Voices may also be mixed with background music or other sounds.

Features

- ☐ ADPCM decoding capability
- ☐ Eight messages selectable per memory bank
- ☐ Compatible with 2716/32 external ROM
- ☐ Unlimited number of messages storable in multiple memory banks
- ☐ Variable bit rate 14 to 20Kbps
- ☐ Sampling clock 4, 5, or 6KHz
- ☐ Compressed encoding for pauses
- ☐ Easy voice processing
  - – High quality voice reproduction
  - – Minimum dependence on voice characteristics of speaker
  - – Easy analysis and data generation
  - – Stable voice quality
  - – Combined voice and background music capability
- ☐ N channel MOS
- ☐ +5V single power supply
- ☐ 40-pin plastic DIP

Pin Configuration



Pin Identification

Pin No.	Symbol	Name	I/O	Function
2,3	$XTAL_1$ $XTAL_2$	Crystal	–	Form a clock oscillator circuit when externally connected to 6MHz crystal
4	$\overline{RESET}$	Reset	I	Initializes the μPD7751 internal logic
6	$\overline{START}$	Start	I	Starts output of message that has been selected by SEL_0- SEL_2. Active low trigger input
12-19	$DATA_0$ to $DATA_7$	Data Signal	I	Transfers the compressed voice data from an external memory for decoding.
21-24	AD_0 to AD_3	Address Signal	O	Specifies to I/O expander ports (eg, μPD8243) the address of the external memory containing the stored voice data.
25	PROG	Program Signal	O	Strobe signal for decoding address signals Low to high transition indicates address information is present on lines AD_0-AD_3
27-34	VO_0 to VO_7	Voice Signal	O	Outputs to D/A converter the 8-bit voice signal that has been decoded via ADPCM
35-37	$\overline{SEL_0}$ to $\overline{SEL_2}$	Message Select	I	Specifies which of eight types of stored messages to be output from external memory
38	$\overline{Busy}$	Busy Signal	O	Chip status; goes low during decode and output operations
26,40	V_{CC}	Power Supply	I	+5volt power supply.
20	GND	Ground		
5,8-11	IC	Internal Connection	O	Must be left open during normal operation.
1,7,39	$TEST_1$ to $TEST_3$	Test Input	I	Inputs for LSI testing. Must be connected to GND during normal operation.

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7751

7751DS-7-83-CAT-W

Notes

μPD7752
FORMANT VOICE SYNTHESIS

PRELIMINARY

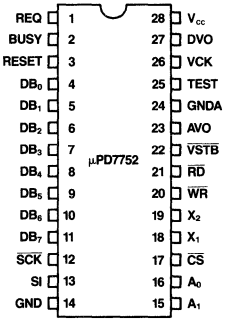
Description

The μPD7752 is an LSI for voice synthesis which employs formant data as accumulated parameters. With five filters corresponding to the first through the fifth formants, vocal characteristics are reproduced to synthesize voice at bit rates as low as 2400bps. The μPD7752 can be connected easily to any bus system of the 8080A family. Through serial interfaces, the LSI can also be connected to various other microcomputers. The μPD7752 operates with attractive low power consumption because of its CMOS structure.

Features

- ☐ Voice synthesizing system using formant parameters
- ☐ 5 formants — first through fifth
- ☐ Bit rate variable between 5600bps and 2400bps
- ☐ Internal 32K-bit ROM for voice data storage (voice duration: approx. 13 seconds at 2400bps, max 63 messages)
- ☐ External formant parameter ROM (option)
- ☐ On-board 9-bit D/A converter — option provided to interface an external D/A converter
- ☐ 3 different voice synthesizing speeds (slow, normal, and fast)
- ☐ Frame length: 10ms or 20ms
- ☐ Bus-compatible with the μPD8080A, μPD8085A and μPD8048
- ☐ Serial interface for mode/command input
- ☐ Clock oscillator circuit
- ☐ CMOS structure
- ☐ +5V single power supply
- ☐ 28-pin plastic DIP

Pin Configuration



Pin Identification

Pin No.	Symbol	Name	I/O	Function
1	REQ	Request	O	Requests a formant parameter from external ROM. Returns to low level after the parameter has been written, or if an error occurs during the parameter transfer, or if a stop command is received during voice generation.
2	BUSY	Busy	O	Indicates message select command accepted and synthesis operation is in progress.
3	RESET	Reset	I	Resets device.
4–11	DB_0–DB_7	Data Bus	Three-state	Bidirectional data bus for input of mode, command, and formant parameter data to μPD7752, and output of status information.
12	$\overline{SCK}$	Serial Clock	I	Clock for serial input. Should be held high for parallel input mode
13	SI	Serial Input	I	Serial input for mode or command data, as specified by A_0.
14	GND	Ground		
15, 16	A_0, A_1	Input Data Identification	I	Specification of parallel bus input as mode, command, or formant data (see I/O Control Signals Table). For serial input: A_0 = 0 for mode; A_0 = 1 for command.
17	$\overline{CS}$	Chip Select	I	Low-level signal enables read/write transfers on parallel data bus.
18, 19	X_1, X_2	Crystal Oscillator		Connection for 3.6MHz (3.579545MHz) crystal or ceramic oscillator, or for input of external clock into X_1.
20	$\overline{WR}$	Write	I	Low-level signal writes bus input to the μPD7752 (mode, command, or formant data as specified by A_0, A_1, see I/O Control Signals Table).
21	$\overline{RD}$	Read	I	Low-level signal reads status information from the μPD7752, independent of the value of A_0 and A_1.
22	$\overline{VSTB}$	Voice Output Strobe	O	Strobe indicates that all 16 bits of serial data have been output from DVO (digital voice output).
23	AVO	Analog Voice Output	O	Synthesized analog voice output from 9-bit D/A converter. Requires external load resistor
24	GNDA	Analog Ground		Ground potential for AVO (analog voice output)
25	TEST	Test	I	Input for LSI testing. Must be connected to GND during normal operation.
26	VCK	Voice Clock	O	Output of 16 clock pulses synchronized to DVO signal.
27	DVO	Digital Voice Output	O	Synthesized digital voice output as the 14 MSB of a 16-bit serial data stream. Output is LSB first, and the first two (LSB) bits are zero.
28	V_{CC}	Power		+5V power supply.

I/O Control Signals

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_0	A_1	Operation
1	X	X	X	X	No operation
0	0	1	X	X	Status read
0	1	0	0	0	Formant parameter write
0	1	0	0	1	Mode write
0	1	0	1	0	Prohibited
0	1	0	1	1	Command write

Note: 0 = Low
1 = High
X = Don't Care

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD7752

7752DS-7-83-CAT-W

6

PRELIMINARY

μPD7761/μPD7762/MC-4760 SPEECH RECOGNITION 3-CHIP SET

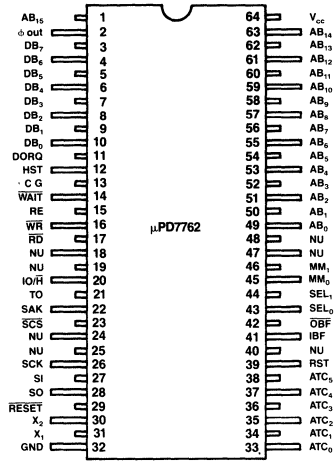
Description

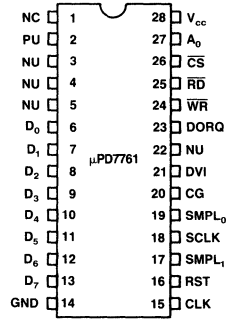
The μPD7761, μPD7762, and MC-4760 constitute a 3-chip LSI set containing the main functions of an isolated word, speaker-dependent recognition system. These functions include an analog interface, processing for voice analysis, compressed dynamic programming (DP) matching, and system control. The 3-chip set employs a DP time warping algorithm to compensate for variations in the rate of speech, which greatly facilitates the matching of a given spoken phrase to a stored vocabulary of digitized words. Three kinds of system I/O interface are supported for ease of control by external microcomputers. With this LSI chip set, speech recognition systems can be developed for low cost and with low total chip count.

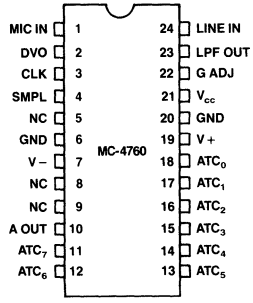
Features

- ☐ Recognition of 128 isolated words
- ☐ Compressed DP matching algorithm
- ☐ Word registration capacity: 128 to 512 words (with 16K-to 64K-byte memory)
- ☐ Word duration up to 2 seconds
- ☐ Average 0.5 seconds response time for recognition
- ☐ Recognition rate above 98 percent
- ☐ Directly connectable to microphone for voice input
- ☐ Supports parallel, serial, and RS-232C system I/O interfaces
- ☐ Convenient commands for recognition, training, data transfer, and other functions
- ☐ Includes analog interface (MC-4760), analysis and calculation processor (μPD7761), and control processor (μPD7762)
- ☐ Requires +5V, +12V, −12V power supply
- ☐ A/D converter sampling at 10kHz

Pin Configurations







6

Notes

μPD8155
μPD8155-2
μPD8156
μPD8156-2

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

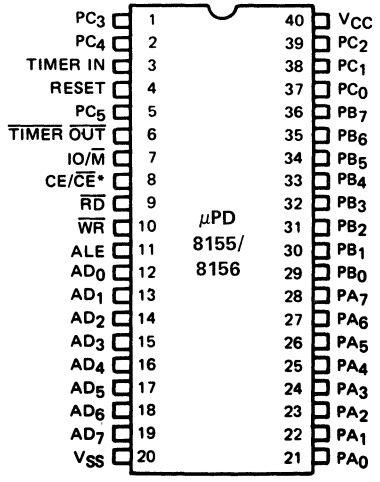
DESCRIPTION

The μPD8155 and μPD8156 are μPD8085A family components having 256 X 8 Static RAM, 3 programmable I/O ports and a programmable timer. They directly interface to the multiplexed μPD8085A bus with no external logic. The μPD8155 has an active low chip enable while the μPD8156 is active high.

FEATURES

- 256 X 8-Bit Static RAM
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Single Power Supplies: +5 Volt, ±10%
- Directly interfaces to the μPD8085A and μPD8085A-2
- Available in 40 Pin Plastic Packages

PIN CONFIGURATION



*μPD8155: $\overline{CE}$
μPD8156: CE

6

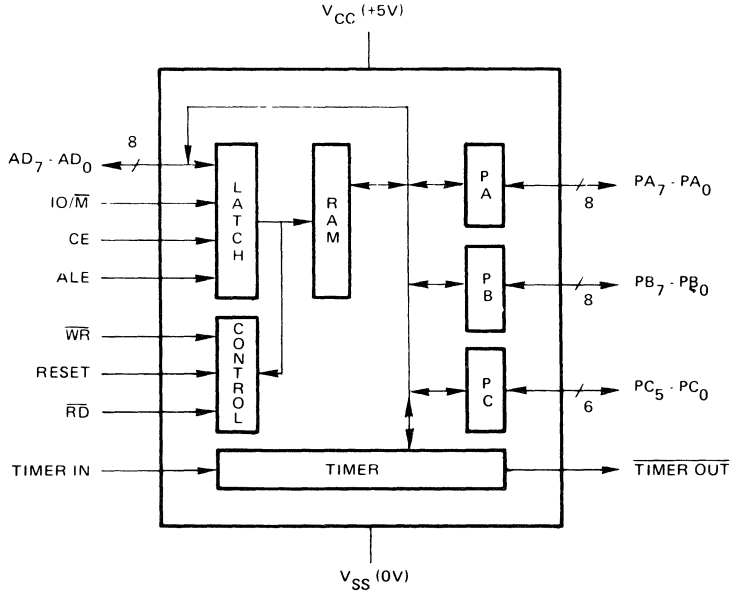
FUNCTIONAL DESCRIPTION

The μPD8155 and μPD8156 contain 2048 bits of Static RAM organized as 256 X 8. The 256 word memory location may be selected anywhere within the 64K memory space by using combinations of the upper 8 bits of address from the μPD8085A as a chip select.

The two general purpose 8-bit ports (PA and PB) may be programmed for input or output either in interrupt or status mode. The single 6-bit port (PC) may be used as control for PA and PB or general purpose input or output port. The μPD8155 and μPD8156 are programmed for their system personalities by writing into their Command/Status Registers (C/S) upon system initialization.

The timer is a single 14-bit down counter which is programmable for 4 modes of operation; see Timer Section.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1.5 W

Note: ① With Respect to Ground.

$T_a = 25°C$

*COMMENT. Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 5 39, 38, 37	PC_3, PC_4, PC_5 PC_2, PC_1, PC_0	Port C	Used as control for PA and PB or as a 6-bit general purpose port
3	TIMER IN	Timer Clock In	Clock input to the 14-bit binary down counter
4	RESET	Reset In	From μPD8085A system reset to set PA, PB, PC to the input mode
6	$\overline{\text{TIMER OUT}}$	Timer Counter Output	The output of the timer function
7	IO/$\overline{M}$	I/O or Memory Indicator	Selects whether operation to and from the chip is directed to the internal RAM or to I/O ports
8	CE/$\overline{CE}$	Chip Enable	Chip Enable Input. Active low for μPD8155 and active high for μPD8156
9	$\overline{RD}$	Read Strobe	Causes Data Read
10	$\overline{WR}$	Write Strobe	Causes Data Write
11	ALE	Address Low Enable	Latches low order address in when valid
12-19	$AD_0 - AD_7$	Low Address/Data	3-State address/data bus to interface directly to μPD8085A
20	V_{SS}	Ground	Ground Reference
21-28	$PA_0 - PA_7$	Port A	General Purpose I/O Port
29-36	$PB_0 - PB_7$	Port B	General Purpose I/O Port
40	V_{CC}	5 Volt Input	Power Supply

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage		V_{IL}	-0.5		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = 400 μA
Input Leakage		I_{IL}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current		I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current		I_{CC}			180	mA	
Chip Enable Leakage	μPD8155	I_{IL} (CE)			+100	μA	$V_{IN} = V_{CC}$ to 0V
	μPD8156	I_{IL}(CE)			-100	μA	

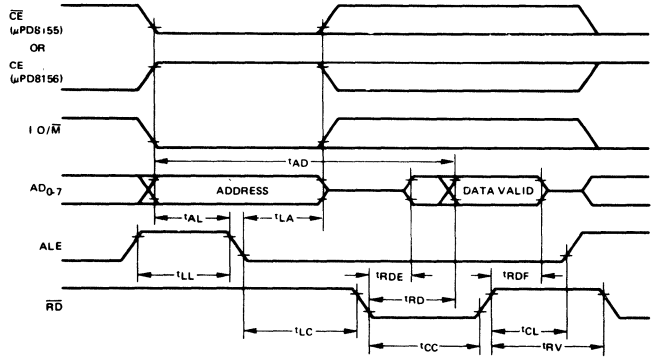
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

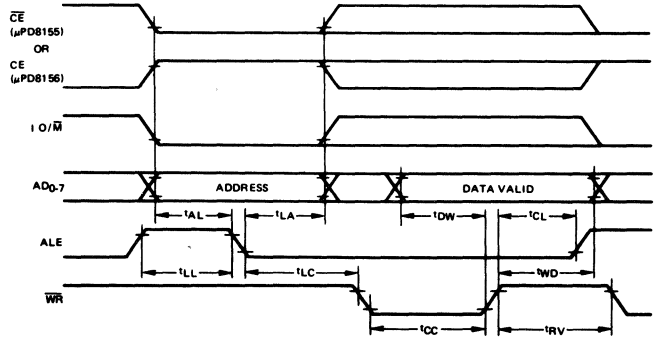
PARAMETER	SYMBOL	LIMITS 8155/8156 MIN	LIMITS 8155/8156 MAX	LIMITS 8155-2/8156-2 MIN	LIMITS 8155-2/8156-2 MAX	UNIT	TEST CONDITIONS
Address to Latch Set Up Time	t_{AL}	50		30		ns	150 pF Load
Address Hold Time after Latch	t_{LA}	80		30		ns	
Latch to READ/WRITE Control	t_{LC}	100		40		ns	
Valid Data Out Delay from READ Control	t_{RD}		170		140	ns	
Address Stable to Data Out Valid	t_{AD}		400		330	ns	
Latch Enable Width	t_{LL}	100		70		ns	
Data Bus Float After READ	t_{RDF}	0	100	0	80	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20		10		ns	
READ/WRITE Control Width	t_{CC}	250		200		ns	
Data In to WRITE Set Up Time	t_{DW}	150		100		ns	
Data In Hold Time After WRITE	t_{WD}	0		0		ns	
Recovery Time Between Controls	t_{RV}	300		200		ns	
WRITE to Port Output	t_{WP}		400		300	ns	
Port Input Setup Time	t_{PR}	70		50		ns	
Port Input Hold Time	t_{RP}	50		10		ns	
Strobe to Buffer Full	t_{SBF}		400		300	ns	
Strobe Width	t_{SS}	200		150		ns	
READ to Buffer Empty	t_{RBE}		400		300	ns	
Strobe to INTR On	t_{SI}		400		300	ns	
READ to INTR Off	t_{RDI}		400		300	ns	
Port Setup Time to Strobe	t_{PSS}	50		0		ns	
Port Hold Time After Strobe	t_{PHS}	120		100		ns	
Strobe to Buffer Empty	t_{SBE}		400		300	ns	
WRITE to Buffer Full	t_{WBE}		400		300	ns	
WRITE to INTR Off	t_{WI}		400		300	ns	
TIMER-IN to TIMER-OUT Low	t_{TL}		400		300	ns	
TIMER-IN to TIMER-OUT High	t_{TH}		400		300	ns	
Data Bus Enable from READ Control	t_{RDE}	10		10		ns	

TIMING WAVEFORMS

READ CYCLE

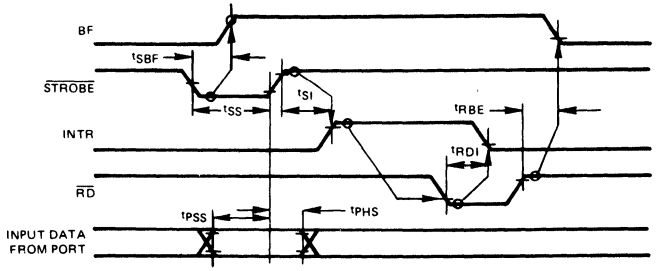


WRITE CYCLE

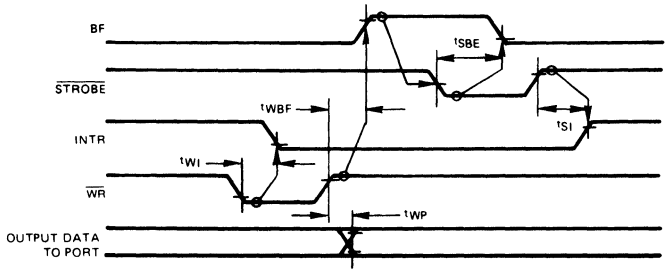


TIMING WAVEFORMS
(CONT.)

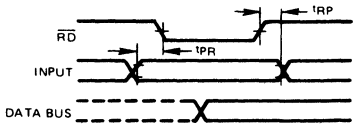
STROBED INPUT MODE



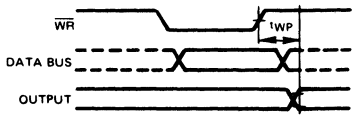
STROBED OUTPUT MODE



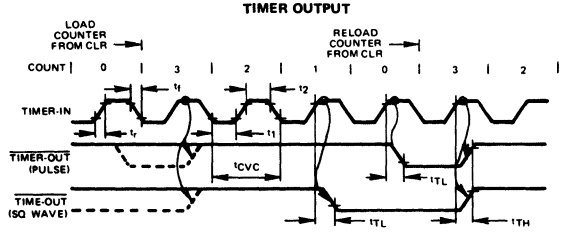
BASIC INPUT MODE



BASIC OUTPUT MODE



TIMER OUTPUT



COUNTDOWN FROM 3 TO 0

	μPD8155/8156	μPD8155-2/8156-2
t_{CYC}	320 ns MIN	200 ns MIN
t_{RISE} & t_{FALL}	30 ns MAX.	30 ns MAX
t_1	80 ns MIN	40 ns MIN
t_2	120 ns MIN	70 ns MIN
t_{TL}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ LOW (TO BE DEFINED)	
t_{TH}	TIMER-IN to $\overline{\text{TIMER-OUT}}$ HIGH (TO BE DEFINED)	

6

COMMAND STATUS REGISTER

The Command Status Register is an 8-bit register which must be programmed before the μPD8155/8156 may perform any useful functions. Its purpose is to define the mode of operation for the three ports and the timer. Programming of the device may be accomplished by writing to I/O address XXXXX000 (X denotes don't care) with a specific bit pattern. Reading of the Command Status Register can be accomplished by performing an I/O read operation at address XXXXX000. The pattern returned will be a 7-bit status report of PA, PB and the Timer. The bit patterns for the Command Status Register are defined as follows:

COMMAND STATUS WRITE

TM2	TM1	IEB	IEA	PC_2	PC_1	PB	PA

where:

TM2-TM1	Define Timer Mode
IEB	Enable Port B Interrupt
IEA	Enable Port A Interrupt
PC_2-PC_1	Define Port C Mode
PB/PA	Define Port B/A as In or Out ①

The Timer mode of operation is programmed as follows during command status write:

TM2	TM1	TIMER MODE
0	0	Don't Affect Timer Operation
0	1	Stop Timer Counting
1	0	Stop Counting after TC
1	1	Start Timer Operation

Interrupt enable status is programmed as follows:

IEB/IEA	INTERRUPT ENABLE PORT B/A
0	No
1	Yes

Port C may be placed in four possible modes of operation as outlined below. The modes are selected during command status write as follows:

PC_2	PC_1	PORT C MODE
0	0	ALT 1
0	1	ALT 3
1	0	ALT 4
1	1	ALT 2

The function of each pin of port C in the four possible modes is outlined as follows:

PIN	ALT 1	ALT 2	ALT 3 ②	ALT 4 ②
PC0	IN	OUT	A INTR	A INTR
PC1	IN	OUT	A BF	A BF
PC2	IN	OUT	A $\overline{STB}$	A $\overline{STB}$
PC3	IN	OUT	OUT	B INTR
PC4	IN	OUT	OUT	B BF
PC5	IN	OUT	OUT	B $\overline{STB}$

Notes: ① PB/PA Sets Port B/A Mode: 0 = Input; 1 = Output

② In ALT 3 and ALT 4 mode the control signals are initialized as follows:

CONTROL	INPUT	OUTPUT
$\overline{STB}$ (Input Strobe)	Input Control	Input Control
INTR (Interrupt Request)	Low	High
BF (Buffer Full)	Low	Low

COMMAND STATUS REGISTER (CONT.)

COMMAND STATUS READ

	TI	INTE B	B BF	INTR B	INTE A	A BF	INTR A

Where the function of each bit is as follows:

TI	Defines a Timer Interrupt. Latched high at TC and reset after reading the CS register or starting a new count, or reset.
INTE B/A	Defines If Port B/A Interrupt is Enabled. High = enabled.
B/A BF	Defines If Port B/A Buffer is Full-Input Mode or Empty-Output Mode. High = active.
INTR B/A	Port B/A Interrupt Request. High = active.

The programming address summary for the status, ports, and timer are as follows:

I/O Address	Number of Bits	Function
XXXXX000	8	Command Status
XXXXX001	8	PA
XXXXX010	8	PB
XXXXX011	6	PC
XXXXX100	8	Timer-Low
XXXXX101	8	Timer-High

TIMER

The Internal Timer is a 14-bit binary down counter capable of operating in 4 modes. Its desired mode of operation is programmable at any time during operation. Any TTL clock meeting timer in requirements (See AC Characteristics) may be used as a time base and fed to the timer input. The timer output may be looped around and cause an interrupt or used as I/O control. The operational modes are defined as follows and programmed along with the 6 high bits of timer data.

M2	M1	Operation
0	0	High at Start, Low During Second Half of Count
0	1	Square Wave (Period = Count Length, Auto Reload at TC)
1	0	Single Pulse at TC
1	1	Single Pulse at TC with Auto Reload

6

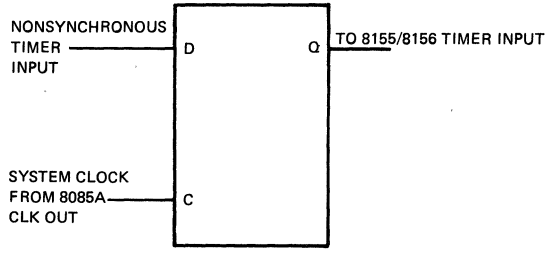
TIMER (CONT.)

Programming the timer requires two words to be written to the μPD8155/8156 at I/O address XXXXX100 and XXXXX101 for the low and high order bytes respectively. Valid count length must be between 2_H and $3FFF_H$. The bit assignments for the high and low programming words are as follows:

Word	Bit Pattern								I/O Address
High Byte	M_2	M_1	T13	T12	T11	T10	T9	T8	XXXXX101
Low Byte	T7	T6	T5	T4	T3	T2	T1	T0	XXXXX100

The control of the timer is performed by TM2 and TM1 of the Command Status Word.

Note that counting will be stopped by a hardware reset and a START command must be issued via the Command Status Register to begin counting. A new mode and/or count length can be loaded while counter is counting, but will not be used until a START command is issued.



When using the timer of the 8155/8156 care must be taken if the timer input is an external, nonsynchronous event. To sync this signal to the system clock the flip-flop shown should be used.

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8155C/56C
Ceramic, μPD8155D/56D

μPD8155H
μPD8155-2
μPD8156H
μPD8156-2

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

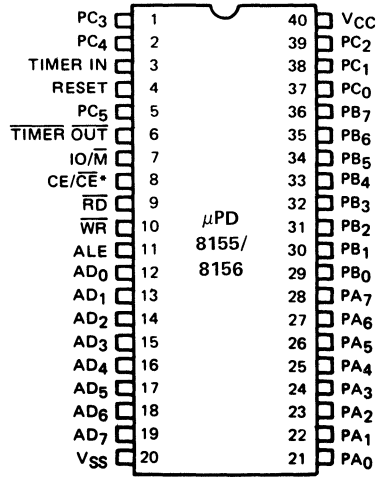
DESCRIPTION

The μPD8155 and μPD8156 are μPD8085A family components having 256 X 8 Static RAM, 3 programmable I/O ports and a programmable timer. They directly interface to the multiplexed μPD8085A bus with no external logic. The μPD8155 has an active low chip enable while the μPD8156 is active high.

FEATURES

- 256 X 8-Bit Static RAM
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Single Power Supplies: +5 Volt, ±10%
- Directly interfaces to the μPD8085A and μPD8085A-2
- Available in 40 Pin Plastic Packages

PIN CONFIGURATION



*μPD8155: $\overline{CE}$
μPD8156: CE

6

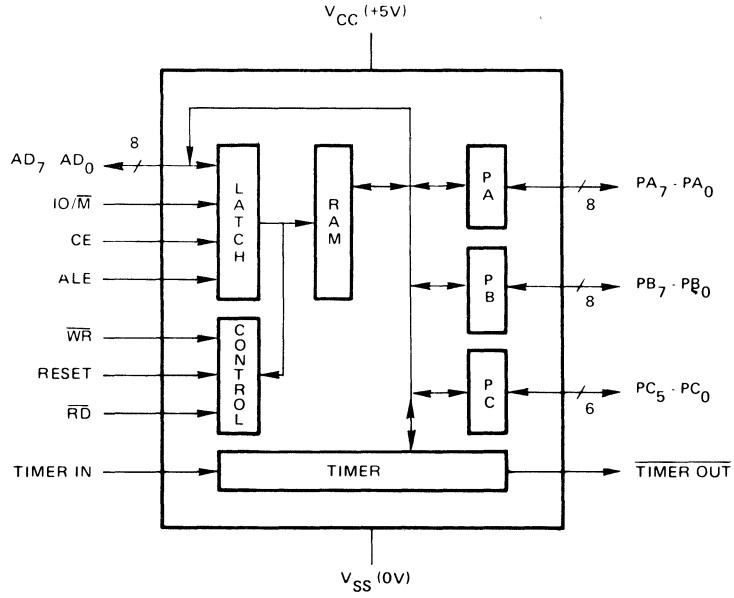
FUNCTIONAL DESCRIPTION

The μPD8155 and μPD8156 contain 2048 bits of Static RAM organized as 256 X 8. The 256 word memory location may be selected anywhere within the 64K memory space by using combinations of the upper 8 bits of address from the μPD8085A as a chip select.

The two general purpose 8-bit ports (PA and PB) may be programmed for input or output either in interrupt or status mode. The single 6-bit port (PC) may be used as control for PA and PB or general purpose input or output port. The μPD8155 and μPD8156 are programmed for their system personalities by writing into their Command/Status Registers (C/S) upon system initialization.

The timer is a single 14-bit down counter which is programmable for 4 modes of operation; see Timer Section.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1.5 W

Note: ① **With Respect to Ground.**

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 5 39, 38, 37	PC_3, PC_4, PC_5 PC_2, PC_1, PC_0	Port C	Used as control for PA and PB or as a 6-bit general purpose port
3	TIMER IN	Timer Clock In	Clock input to the 14-bit binary down counter
4	RESET	Reset In	From μPD8085A system reset to set PA, PB, PC to the input mode
6	$\overline{TIMER\ OUT}$	Timer Counter Output	The output of the timer function
7	IO/$\overline{M}$	I/O or Memory Indicator	Selects whether operation to and from the chip is directed to the internal RAM or to I/O ports
8	CE/$\overline{CE}$	Chip Enable	Chip Enable Input. Active low for μPD8155 and active high for μPD8156
9	$\overline{RD}$	Read Strobe	Causes Data Read
10	$\overline{WR}$	Write Strobe	Causes Data Write
11	ALE	Address Low Enable	Latches low order address in when valid
12-19	$AD_0 - AD_7$	Low Address/Data	3-State address/data bus to interface directly to μPD8085A
20	V_{SS}	Ground	Ground Reference
21-28	$PA_0 - PA_7$	Port A	General Purpose I/O Port
29-36	$PB_0 - PB_7$	Port B	General Purpose I/O Port
40	V_{CC}	5 Volt Input	Power Supply

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 10\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage		V_{IL}	-0.5	0.8	V	
Input High Voltage		V_{IH}	2.0	V_{CC}+0.5	V	
Output Low Voltage		V_{OL}		0.45	V	$I_{OL} = 2$ mA
Output High Voltage		V_{OH}	2.4		V	$I_{OH} = 400\ \mu A$
Input Leakage		I_{IL}		±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current		I_{LO}		±10	μA	$0.45V \leqslant V_{OUT} \leqslant V_{CC}$
V_{CC} Supply Current		I_{CC}		125	mA	8155H/8156H
				180	mA	8155-2/8156-2
Chip Enable Leakage	μPD8155	I_{IL} (CE)		+100	μA	$V_{IN} = V_{CC}$ to 0V
	μPD8156	I_{IL} (CE)		-100	μA	

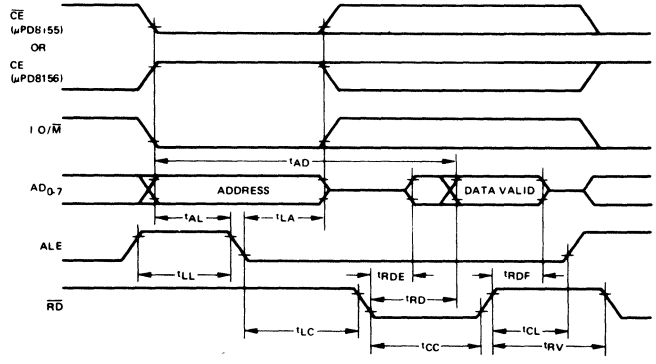
AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = 5V ± 10%

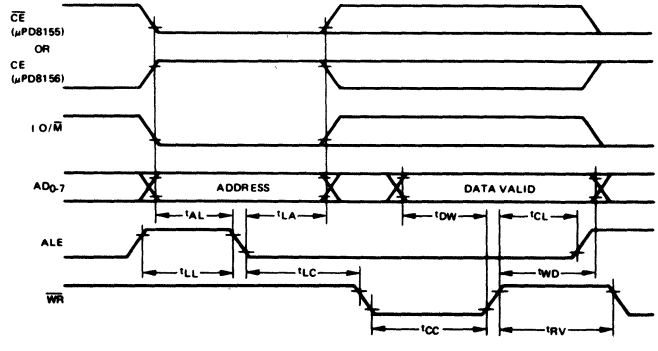
PARAMETER	SYMBOL	LIMITS 8155H/8156H MIN	LIMITS 8155H/8156H MAX	LIMITS 8155-2/8156-2 MIN	LIMITS 8155-2/8156-2 MAX	UNIT	TEST CONDITIONS
Address to Latch Set Up Time	t_{AL}	50		30		ns	150 pF Load
Address Hold Time after Latch	t_{LA}	80		30		ns	
Latch to READ/WRITE Control	t_{LC}	100		40		ns	
Valid Data Out Delay from READ Control	t_{RD}		170		140	ns	
Address Stable to Data Out Valid	t_{AD}		400		330	ns	
Latch Enable Width	t_{LL}	100		70		ns	
Data Bus Float After READ	t_{RDF}	0	100	0	80	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20		10		ns	
READ/WRITE Control Width	t_{CC}	250		200		ns	
Data In to WRITE Set Up Time	t_{DW}	150		100		ns	
Data In Hold Time After WRITE	t_{WD}	0		0		ns	
Recovery Time Between Controls	t_{RV}	300		200		ns	
WRITE to Port Output	t_{WP}		400		300	ns	
Port Input Setup Time	t_{PR}	70		50		ns	
Port Input Hold Time	t_{RP}	50		10		ns	
Strobe to Buffer Full	t_{SBF}		400		300	ns	
Strobe Width	t_{SS}	200		150		ns	
READ to Buffer Empty	t_{RBE}		400		300	ns	
Strobe to INTR On	t_{SI}		400		300	ns	
READ to INTR Off	t_{RDI}		400		300	ns	
Port Setup Time to Strobe	t_{PSS}	50		0		ns	
Port Hold Time After Strobe	t_{PHS}	120		100		ns	
Strobe to Buffer Empty	t_{SBE}		400		300	ns	
WRITE to Buffer Full	t_{WBE}		400		300	ns	
WRITE to INTR Off	t_{WI}		400		300	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low	t_{TL}		400		300	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ High	t_{TH}		400		300	ns	
Data Bus Enable from READ Control	t_{RDE}	10		10		ns	

TIMING WAVEFORMS

READ CYCLE

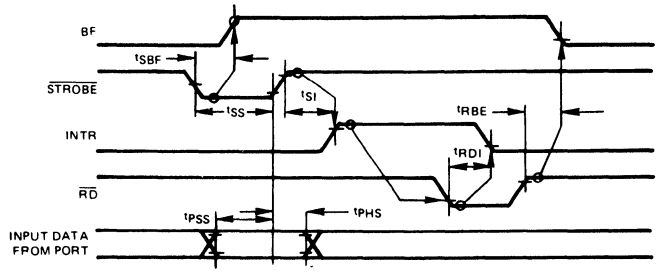


WRITE CYCLE

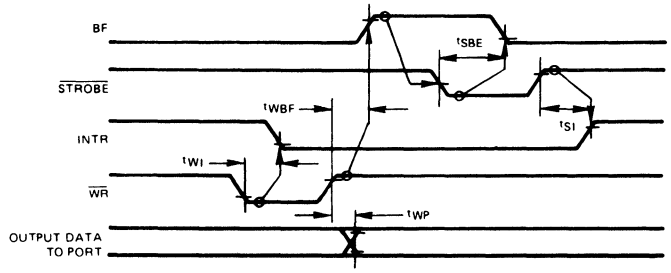


TIMING WAVEFORMS
(CONT.)

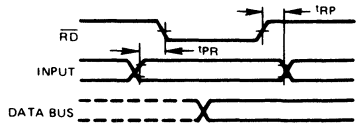
STROBED INPUT MODE



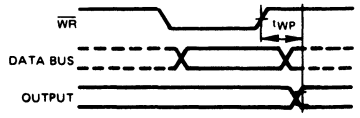
STROBED OUTPUT MODE



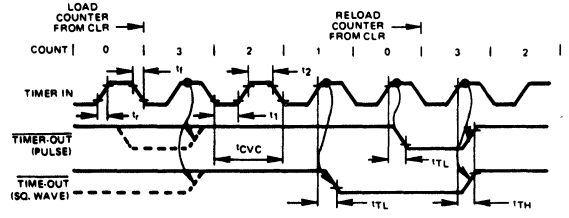
BASIC INPUT MODE



BASIC OUTPUT MODE



TIMER OUTPUT



COUNTDOWN FROM 3 TO 0

	μPD8155/8156	μPD8155-2/8156-2
t_{CYC}	320 ns MIN	200 ns MIN
t_{RISE} & t_{FALL}	30 ns MAX	30 ns MAX
t_1	80 ns MIN	40 ns MIN
t_2	120 ns MIN	70 ns MIN
t_{TL}	TIMER-IN to TIMER-OUT LOW (TO BE DEFINED)	
t_{TH}	TIMER-IN to TIMER-OUT HIGH (TO BE DEFINED)	

6

COMMAND STATUS REGISTER

The Command Status Register is an 8-bit register which must be programmed before the μPD8155/8156 may perform any useful functions. Its purpose is to define the mode of operation for the three ports and the timer. Programming of the device may be accomplished by writing to I/O address XXXXX000 (X denotes don't care) with a specific bit pattern. Reading of the Command Status Register can be accomplished by performing an I/O read operation at address XXXXX000. The pattern returned will be a 7-bit status report of PA, PB and the Timer. The bit patterns for the Command Status Register are defined as follows:

COMMAND STATUS WRITE

TM2	TM1	IEB	IEA	PC_2	PC_1	PB	PA

where:

TM2-TM1	Define Timer Mode
IEB	Enable Port B Interrupt
IEA	Enable Port A Interrupt
PC_2-PC_1	Define Port C Mode
PB/PA	Define Port B/A as In or Out ①

The Timer mode of operation is programmed as follows during command status write:

TM2	TM1	TIMER MODE
0	0	Don't Affect Timer Operation
0	1	Stop Timer Counting
1	0	Stop Counting after TC
1	1	Start Timer Operation

Interrupt enable status is programmed as follows:

IEB/IEA	INTERRUPT ENABLE PORT B/A
0	No
1	Yes

Port C may be placed in four possible modes of operation as outlined below. The modes are selected during command status write as follows:

PC_2	PC_1	PORT C MODE
0	0	ALT 1
0	1	ALT 3
1	0	ALT 4
1	1	ALT 2

The function of each pin of port C in the four possible modes is outlined as follows:

PIN	ALT 1	ALT 2	ALT 3 ②	ALT 4 ②
PC0	IN	OUT	A INTR	A INTR
PC1	IN	OUT	A BF	A BF
PC2	IN	OUT	A $\overline{STB}$	A $\overline{STB}$
PC3	IN	OUT	OUT	B INTR
PC4	IN	OUT	OUT	B BF
PC5	IN	OUT	OUT	B $\overline{STB}$

Notes: ① PB/PA Sets Port B/A Mode: 0 = Input; 1 = Output

② In ALT 3 and ALT 4 mode the control signals are initialized as follows:

CONTROL	INPUT	OUTPUT
$\overline{STB}$ (Input Strobe)	Input Control	Input Control
INTR (Interrupt Request)	Low	High
BF (Buffer Full)	Low	Low

COMMAND STATUS REGISTER (CONT.)

COMMAND STATUS READ

	TI	INTE B	B BF	INTR B	INTE A	A BF	INTR A

Where the function of each bit is as follows:

TI	Defines a Timer Interrupt. Latched high at TC and reset after reading the CS register or starting a new count, or reset.
INTE B/A	Defines If Port B/A Interrupt is Enabled. High = enabled.
B/A BF	Defines If Port B/A Buffer is Full-Input Mode or Empty-Output Mode. High = active.
INTR B/A	Port B/A Interrupt Request. High = active.

The programming address summary for the status, ports, and timer are as follows:

I/O Address	Number of Bits	Function
XXXXX000	8	Command Status
XXXXX001	8	PA
XXXXX010	8	PB
XXXXX011	6	PC
XXXXX100	8	Timer-Low
XXXXX101	8	Timer-High

6

TIMER

The Internal Timer is a 14-bit binary down counter capable of operating in 4 modes. Its desired mode of operation is programmable at any time during operation. Any TTL clock meeting timer in requirements (See AC Characteristics) may be used as a time base and fed to the timer input. The timer output may be looped around and cause an interrupt or used as I/O control. The operational modes are defined as follows and programmed along with the 6 high bits of timer data.

M2	M1	Operation
0	0	High at Start, Low During Second Half of Count
0	1	Square Wave (Period = Count Length, Auto Reload at TC)
1	0	Single Pulse at TC
1	1	Single Pulse at TC with Auto Reload

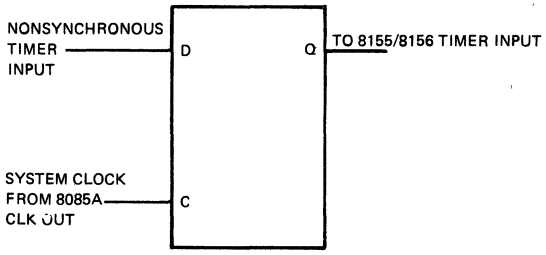
TIMER (CONT.)

Programming the timer requires two words to be written to the μPD8155/8156 at I/O address XXXXX100 and XXXXX101 for the low and high order bytes respectively. Valid count length must be between 2_H and $3FFF_H$. The bit assignments for the high and low programming words are as follows:

Word	Bit Pattern								I/O Address
High Byte	M_2	M_1	T13	T12	T11	T10	T9	T8	XXXXX101
Low Byte	T7	T6	T5	T4	T3	T2	T1	T0	XXXXX100

The control of the timer is performed by TM2 and TM1 of the Command Status Word.

Note that counting will be stopped by a hardware reset and a START command must be issued via the Command Status Register to begin counting. A new mode and/or count length can be loaded while counter is counting, but will not be used until a START command is issued.



When using the timer of the 8155/8156 care must be taken if the timer input is an external, nonsynchronous event. To sync this signal to the system clock the flip-flop shown should be used.

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8155C/56C
Ceramic, μPD8155D/56D

EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

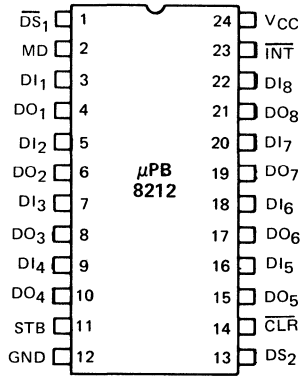
The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

6

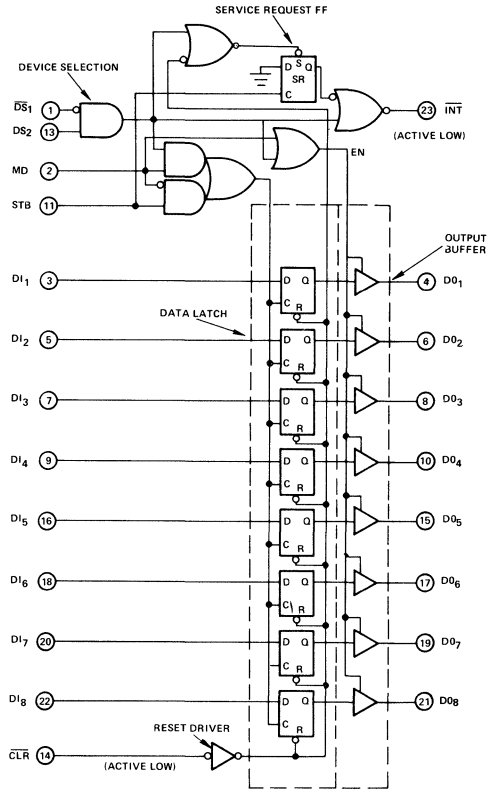
PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_8$	Data In
$DO_1 - DO_8$	Data Out
$\overline{DS}_1, DS_2$	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

BLOCK DIAGRAM



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{CLR}$	$(\overline{DS_1} \cdot DS_2)$	STB	SR ②	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↓	0	1	1
1	0	↓	0	0
1	1	0	1	0
1	1	↓	0	0

Notes ① $\overline{CLR}$ resets data latch sets SR flip-flop (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	125 mA

$T_a = 25°C$

*COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current STB, DS_2, $\overline{CLR}$, $DI_1 - DI_8$ Inputs	IIL1		−0 25	mA	V_F = 0 45V
Input Load Current MD Input	IIL2		−0 75	mA	V_F = 0 45V
Input Load Current $\overline{DS}_1$ Input	IIL3		−1 0	mA	V_F = 0 45V
Input Leakage Current STB DS, $\overline{CLR}$, $DI_1 - DI_8$ Inputs	IIH1		10	μA	V_R = 5 25V
Input Leakage Current MD Input	IIH2		30	μA	V_R = 5 25V
Input Leakage Current $\overline{DS}_1$ Input	IIH3		40	μA	V_R = 5 25V
Input Forward Voltage Clamp	V_C		−1 0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}		0 85	V	
Input "High" Voltage	V_{IH}	2 0		V	
Output "Low" Voltage	V_{OL}		0 48	V	I_{OL} = 15 mA
Output "High" Voltage	V_{OH}	3 65		V	I_{OH} = −1 mA
Short Circuit Output Current	I_O[5]	−15	−75	mA	V_O = 0V V_{CC} = 5V
Output Leakage Current High Impedance State $DO_0 - DO_8$	I_O		20	μA	V_O = 0 45V/5 25V
Power Supply Current	I_{CC}		130	mA	

CAPACITANCE ①

T_a = 25°C; V_{CC} = +5V; V_{BIAS} = 2.5V; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		12	pF	$\overline{DS}_1$, MD
Input Capacitance	C_{IN}		9	pF	DS_2, $\overline{CLR}$, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		12	pF	$DO_1 - DO_8$

Note: ① This parameter is periodically sampled and not 100% tested

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30		ns	Input Pulse Amplitude = 2.5V
Data To Output Delay	t_{pd}		30	ns	
Write Enable To Output Delay	t_{we}		40	ns	Input Rise and Fall Times = 5 ns
Data Setup Time	t_{set}	15		ns	
Data Hold Time	t_h	20		ns	Between 1V and 2V
Reset to Output Delay	t_r		40	ns	Measurement made
Set To Output Delay	t_s		30	ns	at 1.5V with 15 mA
Output Enable/Disable Time	t_e/t_d		45	ns	① and 30 pF Test Load
Clear To Output Delay	t_c		55	ns	

Notes: ① R_1 = 300Ω/10KΩ, R_2 = 600Ω/1KΩ

6

Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note. Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

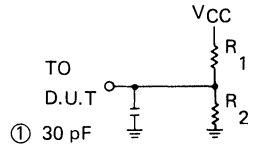
When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

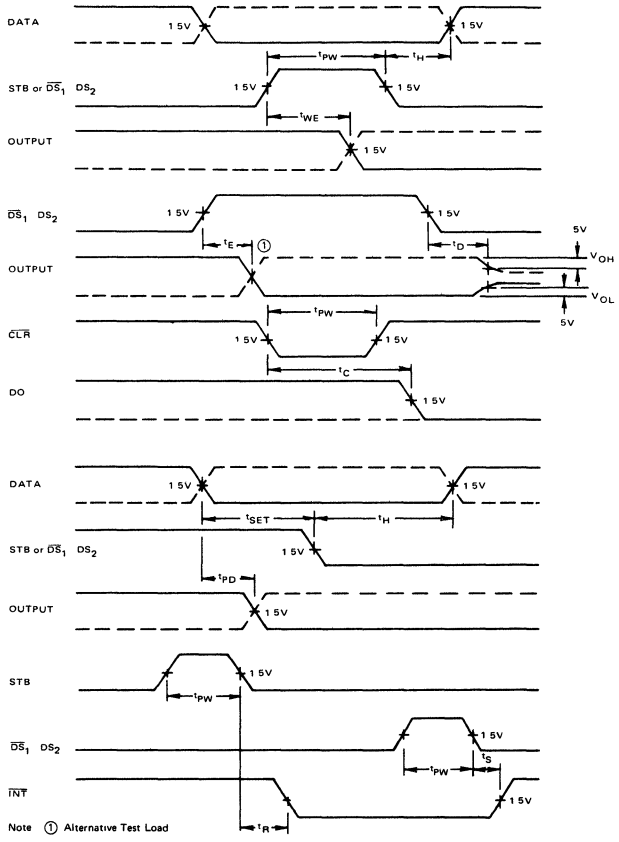
Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

TIMING WAVEFORMS



Note: ① Including Jig and Probe Capacitance

TEST CIRCUIT



6

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPB8212C
Cerdip, μPB8212D

4-BIT PARALLEL BIDIRECTIONAL BUS DRIVER

DESCRIPTION

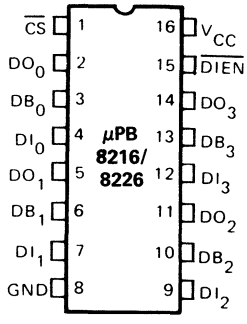
All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V (V_{OH}), and for high capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability.

FEATURES

- Data Bus Buffer Driver for μCOM-8 Microprocessor Family
- Low Input Load Current – 0.25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to μCOM-8 Microprocessor Family
- Three State Outputs
- Reduces System Package Count
- Available in 16-pin packages: Cerdip and Plastic

6

PIN CONFIGURATION



PIN NAMES

DB_0 – DB_3	Data Bus Bi Directional
DI_0 – DI_3	Data Input
DO_0 – DO_3	Data Output
$\overline{DIEN}$	Data in Enable Direction Control
$\overline{CS}$	Chip Select

FUNCTIONAL DESCRIPTION

Microprocessors like the μPD8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The μPD8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers. They are three state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL compatible and it has high drive (55 mA). For maximum flexibility on the other side of the driver the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080A Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080A processor is achieved with an adequate amount of noise immunity (650 mV worst case).

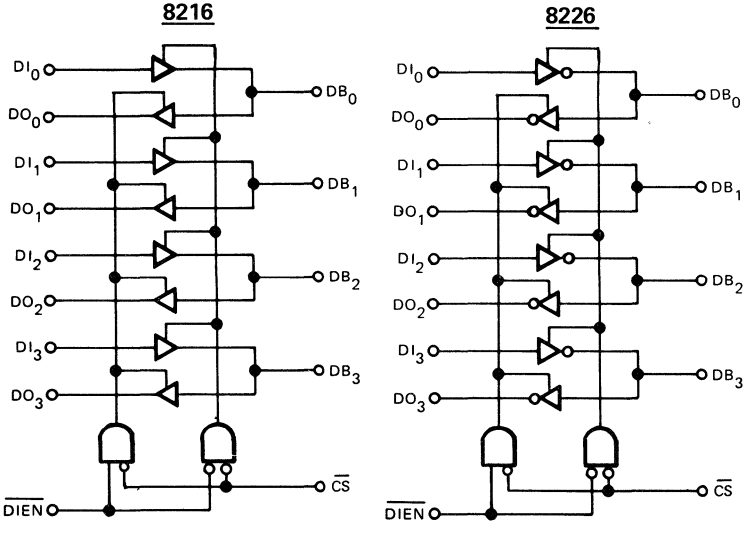
Control Gating $\overline{CS}$, $\overline{DIEN}$

The $\overline{CS}$ input is used for device selection. When $\overline{CS}$ is "high" the output drivers are all forced to their high-impedance state. When it is "low" the device is selected (enabled) and the data flow direction is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the data flow direction (see Block Diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two gate circuit.

The μPB8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

BLOCK DIAGRAMS



$\overline{DIEN}$	$\overline{CS}$	RESULT
0	0	DI → DB
1	0	DB → DO
0	1	High Impedance
1	1	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
All Output and Supply Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −1.0 to +5.5 Volts
Output Currents ..... 125 mA

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current $\overline{DIEN}$, $\overline{CS}$		I_{F1}			−0.5	mA	$V_F = 0.45$
Input Load Current All Other Inputs		I_{F2}			−0.25*	mA	$V_F = 0.45$
Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		I_{R1}			20	μA	$V_R = 5.25V$
Input Leakage Current DI Inputs		I_{R2}			10	μA	$V_R = 5.25V$
Input Forward Voltage Clamp		V_C			−1.0	V	$I_C = -5$ mA
Input "Low" Voltage		V_{IL}			0.95	V	
Input "High" Voltage		V_{IH}	2.0			V	
Output Leakage Current (3 State)	DO	I_O			20	μA	$V_O = 0.45/5.25V$
	DB	I_O			100		
Power Supply Current	8216	I_{CC}			130	mA	
	8226	I_{CC}			120	mA	
Output "Low" Voltage		V_{OL1}			0.48	V	DO Outputs $I_{OL} = 15$ mA DB Outputs $I_{OL} = 25$ mA
Output "Low" Voltage	8216	V_{OL2}			0.7	V	DB Outputs $I_{OL} = 55$ mA
	8226	V_{OL2}			0.7	V	DB Outputs $I_{OH} = 50$ mA
Output "High" Voltage		V_{OH1}	3.65			V	DO Outputs $I_{OH} = -1$ mA
Output "High" Voltage		V_{OH2}	2.4			V	DB Outputs $I_{OH} = -10$ mA
Output Short Circuit Current		I_{OS}	−15		−65	mA	DO Outputs $V_O = 0V$
		I_{OS}	−30		−120	mA	DB Outputs $V_{CC} = 5.0V$

Note ① Typical values are for $T_a = 25°C$, $V_{CC} = 5.0V$

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	$V_{BIAS} = 2.5V$ $V_{CC} = 5V$ $T_a = 25°C$ f = 1 MHz
Output Capacitance	C_{OUT1}			10 ②	pF	
Output Capacitance	C_{OUT2}			18 ③	pF	

Notes: ① This parameter is not 100% tested.
② DO Output.
③ DB Output.

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

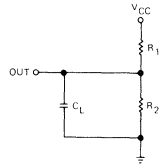
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input to Output Delay DO Outputs		t_{PD1}			25	ns	$C_L = 30$ pF, $R_1 = 300\Omega$, $R_2 = 600\Omega$ ④
Input to Output Delay	8216	t_{PD2}			30	ns	$C_L = 300$ pF, $R_1 = 90\Omega$,
DB Outputs	8226	t_{PD2}			25	ns	$R_2 = 180\Omega$ 4
Output Enable Time	8216	t_E			65	ns	② ④
	8226	t_E			54	ns	
Output Disable Time		t_D			35	ns	③ ④

Notes ① Typical values are for $T_a = 25°C$, $V_{CC} = 5.0V$

② DO Outputs, $C_L = 30$ pF, $R_1 = 300/10$ KΩ, $R_2 = 600/1$ KΩ,
DB Outputs, $C_L = 300$ pF, $R_1 = 90/10$ KΩ, $R_2 = 180/1$ KΩ

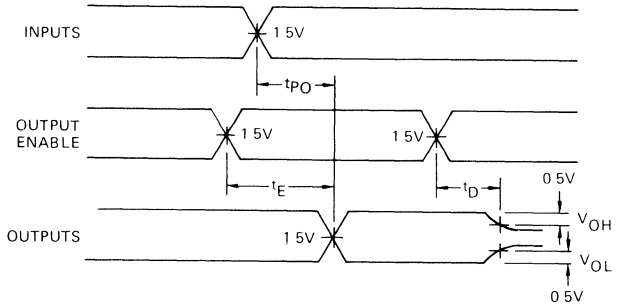
③ DO Outputs, $C_L = 5$ pF, $R_1 = 300/10$ KΩ, $R_2 = 600/1$ KΩ,
DB Outputs, $C_L = 5$ pF, $R_1 = 90/10$ KΩ, $R_2 = 180/1$ KΩ

④ Input pulse amplitude 2.5V
Input rise and fall times of 5 ns between 1 and 2 volts
Output loading is 5 mA and 10 pF
Speed measurements are made at 1.5 volt levels



TEST CIRCUIT

TIMING WAVEFORMS



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPB8216C/26C
Cerdip, μPB8216D/26D

μPD8237A-5
HIGH PERFORMANCE PROGRAMMABLE DMA CONTROLLER

Description

The μPD8237A-5 High Performance DMA Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The μPD8237A-5 offers a wide variety of programmable control features to enhance data throughput and allow dynamic reconfiguration under program control.

The μPD8237A-5 is designed to be used with an external 8-bit address register such as the 8282. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

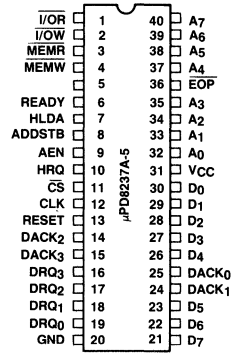
The three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process (EOP).

Each channel has a full 64K byte address and word count capability.

Features

- ☐ Memory-to-memory transfers
- ☐ Memory block initialization
- ☐ Address increment or decrement
- ☐ Four independent DMA channels
- ☐ Multiple transfer modes: block, demand, single word, cascade
- ☐ Independent Autoinitialization of all channels
- ☐ Enable/Disable control of individual DMA requests
- ☐ Independent polarity control for DREQ and DACK signals
- ☐ End of Process input for terminating transfers
- ☐ Software DMA requests
- ☐ High performance: transfers up to 1.6 M-bytes/second
- ☐ Directly expandable to any number of channels
- ☐ 40-pin plastic or ceramic DIP

Pin Configuration



Pin Identification

No.	Symbol	Direction	Function
1	$\overline{I/OR}$	IN/OUT	In Idle state, $\overline{I/OR}$ is an input control line used by the CPU to read control registers. In Active state, the μPD8237A-5 uses $\overline{I/OR}$ as an output control signal to access data from a peripheral during a DMA Write
2	$\overline{I/OW}$	IN/OUT	In Idle state, the CPU uses $\overline{I/OW}$ as an input control signal to load information to the μPD8237A-5. In Active state, the μPD8237A-5 uses I/$\overline{OW}$ as an output control signal to load data to a peripheral during a DMA Read. The rising edge of $\overline{WR}$ must follow each data byte transfer in order for the CPU to write to the μPD8237A-5. Holding $\overline{I/OW}$ low while toggling $\overline{CS}$ does not produce the same effect.
3	$\overline{MEMR}$	OUT	$\overline{MEMR}$ accesses data from a specified memory location during memory-to-peripheral or memory-to-memory transfers
4	$\overline{MEMW}$	OUT	$\overline{MEMW}$ writes data to a specified memory location during peripheral-to-memory or memory-to-memory transfers.
5		IN	Pin 5 is always tied high.
6	READY	IN	The READY signal can extend memory read and write pulses for slow memories or I/O peripherals.
7	HLDA	IN	HLDA indicates that the CPU has relinquished control of the system buses
8	ADDSTB	OUT	This signal strobes the upper address byte from D_0-D_7 into an external latch
9	AEN	OUT	This signal allows the external latch to output the upper address byte by disabling the system bus during DMA cycles. You should use HLDA and AEN to deselect I/O peripherals that may be erroneously accessed during DMA transfers The μPD8237A-5 deselects itself during DMA transfers.
10	HRQ	OUT	This signal requests control of the system bus. The μPD8237A-5 issues this signal in response to software requests or DRQ inputs from peripherals.
11	$\overline{CS}$	IN	The CPU uses $\overline{CS}$ to select the μPD8237A-5 as an I/O device during an I/O Read or Write by the CPU. This provides CPU communication on the data bus. $\overline{CS}$ may be held low during multiple transfers to or from the μPD8237A-5 as long as $\overline{I/OR}$ or $\overline{I/OW}$ is toggled following each transfer.
12	CLK	IN	Controls internal operations and data transfer rate.
13	RESET	IN	Clears the Command, Status, Request, and Temporary registers, the first/last flip/flop, and sets the Mask register. The μPD8237A-5 is in Idle state after a Reset.
14, 15 24, 25	$DACK_0$- $DACK_3$	OUT	These lines indicate an active channel. They are sometimes used to select a peripheral. Only one DACK may be active at any time. All DACK lines are inactive unless DMA has control of the bus. You may program the polarity of these lines, however, Reset initializes them to active low.
16-19	DRQ_0-DRQ_3	IN	These are asynchronous channel request inputs used by peripherals to request DMA service. In a Fixed Priority scheme, DRQ_0 has the highest priority and DRQ_3 has the lowest. You may program the polarity of these lines; however, Reset initializes them to active high.
20	GND		Ground.
21-23, 26-30	D_0-D_7	IN/OUT	During an I/O Read, the CPU enables these lines as outputs, allowing it to read an Address register, a Word Count register, or the Status or Temporary register. During an I/O Write, these lines are enabled as inputs, allowing the CPU to program the μPD8237A-5 control registers. During DMA cycles, the eight MSBs of the address are output to the data bus to be strobed to an external latch via ADDSTB.
31	V_{CC}		Power Supply.

Rev/1

No.	Symbol	Direction	Function
32-35	A_0-A_3	IN/OUT	During DMA Idle states, these lines are inputs; allowing the CPU to load or examine control registers. During DMA Active states, these lines are outputs that provide the 4 LSB of the output address.
36	$\overline{EOP}$	IN/OUT	$\overline{EOP}$ signals that DMA service has been completed. When the word count of a channel becomes zero, the μPD8237A-5 pulses $\overline{EOP}$ low to notify the peripheral that DMA service is complete. The peripheral may pull $\overline{EOP}$ low to prematurely end DMA service. Internal or external receipt of $\overline{EOP}$ causes the currently active channel to end service, set its TC bit in the Status register, and reset its request bit. If the channel is programmed for Autoinitialization, the current registers are updated from the base registers. Otherwise, the channel's mask bit is set and the contents of the register are unaltered. $\overline{EOP}$ is output when TC for channel 1 occurs during memory-to-memory transfers. $\overline{EOP}$ applies to the channel with an active DACK. When $DACK_0$-$DACK_3$ are inactive, external $\overline{EOP}$s are ignored. It is recommended that you use an external pullup resistor of 3.3kΩ or 4.7kΩ. This pin cannot sink the current passed by a 1kΩ pullup.
37-40	A_4-A_7		These lines are outputs that provide the four LSB of the address. These lines are active only during DMA service.

Functional Description

The μPD8237A-5 has three basic control logic blocks, as shown in the block diagram. The Command Control block decodes commands issued by the CPU to the μPD8237A-5 before DMA requests are serviced. It also decodes the Mode Control word of each channel. The Timing Control block generates the external control signals and the internal timing. The Priority Encoder block settles priority contentions among channels simultaneously requesting service.

DMA Operation

The μPD8237A-5 operates in two states: Idle and Active. Each of these is made up of several smaller states equal to one clock cycle. The inactive state, S1, is entered when there are no pending DMA requests. The controller is inactive in S1, but the CPU may program it. S0 is the initial state for DMA service; the μPD8237A-5 requests a hold, but the CPU has not acknowledged. Transfers may begin upon acknowledgement from the CPU. The normal working states of DMA service are S1, S2, S3, and S4. If more time is needed for a transfer, a wait state, SW, can be inserted using the READY line.

A memory-to-memory transfer requires read-from-memory and write-to-memory operations. The states S11, S12, S13, and S14 provide the read-from operation. S21, S22, S23, and S24 provide the write-to part of the transfer. The byte is stored in the Temporary register between operations.

Idle State

When there are no pending service requests, the μPD8237A-5 is in the Idle state; more specifically, in S1. DRQ lines and $\overline{CS}$ are sampled to determine requests for DMA service and CPU attempts to inspect or modify the registers of the μPD8237A-5, respectively. The CPU can read or write to the registers when $\overline{CS}$ and HLDA are low. A_0–A_3 are used as inputs to the μPD8237A and select the registers affected. The $\overline{I/OR}$ and $\overline{I/OW}$ lines select and time the reads and writes. An internal flip-flop generates an additional address bit which determines the upper or lower byte of the Address and Word Count registers. This flip-flop can be reset by master Clear, Reset, or a software command.

When $\overline{CS}$ and HLDA are low (Program Phase), the μPD8237A-5 can execute special software commands. When $\overline{CS}$ and $\overline{I/OW}$ are active, the commands are decoded as addresses and do not use the data bus.

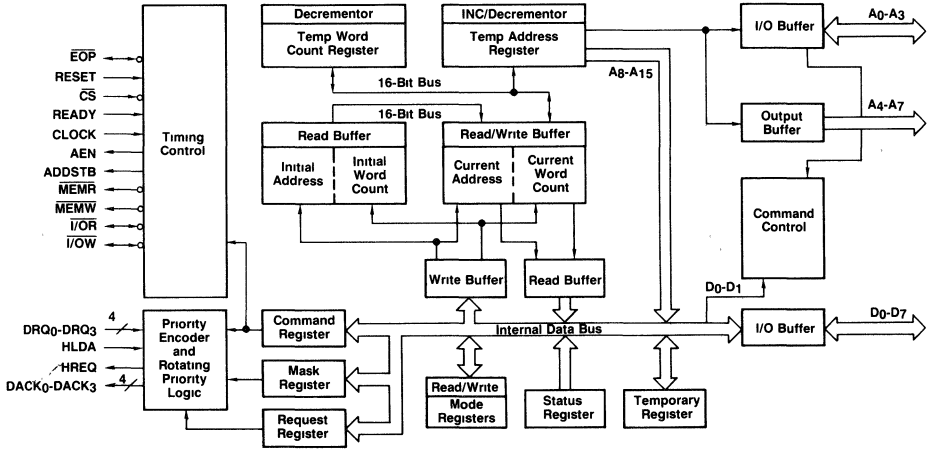
Active State

When a channel requests service while the μPD8237A-5 is in Idle state, the μPD8237A-5 outputs an HRQ to the CPU and enters the Active state. DMA service takes place in the Active state, in one of the four modes described below.

Byte Transfer Mode

In this mode, a one-byte transfer is made during each HRQ/HLDA handshake. HRQ goes active when DRQ goes active. The CPU responds by making HLDA active, and the one-byte transfer takes place. After the transfer, HRQ goes inactive, the word count is decremented, and the address is incremented or decremented. If the word count goes to zero, a Terminal Count (TC) causes

Block Diagram



an Autoinitialize if the channel has been programmed for it.

DRQ is held active only until the corresponding DACK goes active when a single transfer is performed. If DRQ is held active for a longer period, HRQ will become inactive after each transfer, become active again, and a one-byte transfer will be made after each rising edge of HLDA. This assures a full machine cycle between DMA transfers in 8080A/8085A systems. Timing between the μPD8237A-5 and other bus control protocols depends on the CPU being used.

Block Transfer Mode

In this mode, the μPD8237A-5 makes transfers until it encounters a TC or an external $\overline{EOP}$. Hold DRQ active only until DACK goes active. The channel will Autoinitialize at the end of the DMA service if it has been programmed to do so.

Demand Transfer Mode

In this mode, the μPD8237A-5 makes transfers until it encounters a TC or an external EOP, or until DRQ becomes inactive. This allows the device requesting service to stop the transfers by sending DRQ inactive. The device can resume service by making DRQ active. The Current Address and Current Word Count registers may be examined during the time between services when the CPU is allowed to operate. Autoinitialization can occur only after a TC or $\overline{EOP}$ at the end of the DMA service. After an Autoinitialization, there must be an active-going DRQ edge to begin new DMA service.

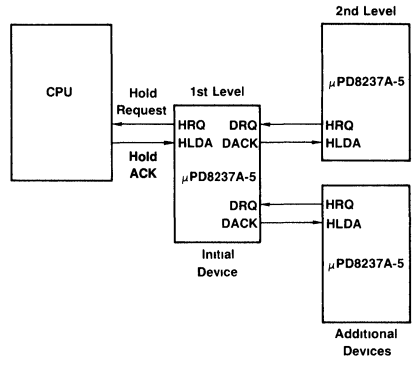
Cascade Mode

In this mode, you can expand your system by cascading several μPD8237A-5s together. Connect the HLDA and HRQ signals from the additional μPD8237A-5s to the DRQ and DACK signals of a channel of the initial μPD8237A-5. This scheme allows the additional devices to send the DMA requests through the priority resolution circuitry of the preceding device, preserving the priority chain and forcing the device to wait its turn to acknowledge requests. The cascade channel in the initial device does not output any address or control signals because its only function is that of assigning priorities. The μPD8237A-5 responds to DRQ with DACK, but all outputs except HRQ are disabled.

The following figure shows two μPD8237A-5s cascaded into two channels of another one, forming a two-level DMA system. You could add more devices at the second level by using the leftover channels of the first level; likewise, you could add more devices to form a third level by cascading into the channels of the second level.

Transfers

There are three types of transfers that can be performed by the three active transfer modes: Read, Write, and Verify. Read transfers activate $\overline{MEMR}$ and $\overline{I/OW}$ to move memory data to an I/O device. Write transfers activate $\overline{I/OR}$ and $\overline{MEMW}$ to move data from an I/O device to memory. Verify transfers are not really transfers; the μPD8237A-5 goes through the motions of a transfer but the memory and I/O lines are not active.



Memory-to-Memory Transfers

Use Block Transfer mode for memory-to-memory transfers. Mask out channels 0 and 1, and initialize the channel 0 word count to the same value as channel 1. Setting bit C0 of the command register to 1 makes channels 0 and 1 operate as memory-to-memory transfer channels. Channel 0 is the source address, channel 1 is the destination address, and the channel 1 word count is used. Initiate the memory-to-memory transfer by setting a DMA request for channel 0. You can write a single source word to a block of memory when channel 0 is programmed for a fixed source address. The μPD8237A-5 responds to external $\overline{EOP}$ signals during these transfers, but no DACK outputs are active. The $\overline{EOP}$ input may be used by data comparators doing block searches to end service when a match is found.

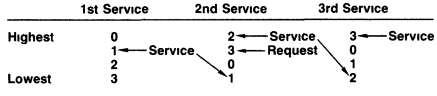
Autoinitialization

A channel may be set for Autoinitialize by programming a bit in the Mode register. Autoinitialize restores the original values of the Current Address and Current Word Count registers from the Initial Address and Initial Word Count registers of that channel. The CPU loads the Current and Initial registers simultaneously and they are unchanged through DMA service. $\overline{EOP}$ does not set the mask bit when the channel is in Autoinitialize. The channel can repeat its service following Autoinitialize without CPU intervention.

Priority Resolution

Two software-selectable priority resolution schemes are available on the μPD8237A-5: Fixed Priority and Rotating Priority. In the Fixed Priority scheme, priority is assigned by the value of the channel number. Channel 3 is the lowest priority and channel 0 is the highest priority.

In the Rotating Priority scheme, the channel that was just serviced assumes the lowest priority and the other channels move up accordingly. This guarantees that a device requesting service can be acknowledged after no more than three other devices have been serviced, preventing any channel from monopolizing the system.



The highest priority channel is selected on each active-going HLDA edge. Once service to a channel begins, it cannot be interrupted by a request from a higher priority channel. A higher priority channel gets control only when the lower priority channel releases HRQ. The CPU gets bus control when control passes from channel to channel, ensuring that a rising HLDA edge can be generated to select the new highest priority request.

Transfer Timing

You can cut transfer timing, if the system allows, by compressing the transfer time to two clock periods. Since state 3 (S_3) extends the access time for the read pulse, you can eliminate S_3, making the width of the read pulse equal to the write pulse. A transfer is then made up of S_2 to change the address and S_4 to perform the read or write. When the address lines A_8–A_{15} need to be updated, S_1 states occur.

Generating Addresses

The eight MSBs of the address are multiplexed on the data lines. These bits are output to an external latch during S_1, after which they can be placed on the address bus. The falling edge of ADDSTB loads the bits from the data lines to the latch. AEN places the bits on the address bus. The eight LSBs of the address are directly output on lines A_0–A_7. Connect A_0–A_7 to the address bus.

Sequential addresses are generated during Block and Demand Transfer mode operations because they include several transfers. Often, data in the external address latch does not change; it changes only when a carry or borrow from A_7 to A_8 occurs in the sequence of addresses. S1 states are executed only when A_8–A_{15} need to be updated. In the course of lengthy transfers, S1 states may be executed only once every 256 transfers.

Registers

The following chart summarizes the registers of the μPD8237A-5.

Register	Bits
Current Address registers (4)	16
Current Word Count registers (4)	16
Initial Address registers (4)	16
Initial Word Count registers (4)	16
Command register	8
Mode registers (4)	6
Request register	4
Mask register	4
Status register	8
Temporary register	8
Temporary Address register	16
Temporary Word Count register	16

Current Address Register

There is a Current Address register for each channel. This register holds the address used for DMA transfers; the address is incremented or decremented after each transfer and the intermediate values are stored here during the transfer. The CPU writes or reads this register in 8-bit bytes. An Autoinitialize restores this register to its initial value.

Current Word Count Register

There is a Current Word Count register for each channel. Program this register with the value of the number of words to be transferred, minus one. The word count is decremented after each transfer and intermediate values are stored in this register during the transfer. A TC is generated when the word count is zero. The CPU writes or reads this register in 8-bit bytes during Program Phase. An Autoinitialize restores this register to its initial value. After an internally generated $\overline{EOP}$, the contents of this register will be FFFFH.

Initial Address and Initial Word Count Registers

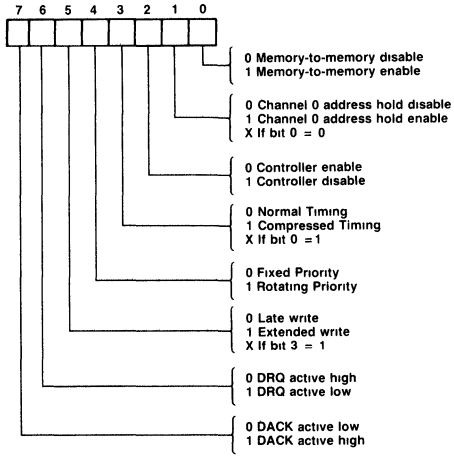
There is an Initial Address register and an Initial Word Count register for each channel. The initial values of the associated Current registers are stored in these registers. The values in these registers are used to restore the Current registers at Autoinitialize. During DMA programming, the CPU writes the Initial registers and the corresponding Current registers at the same time, in 8-bit bytes. Intermediate values in the Current registers are overwritten if you write to the Initial registers while the Current registers contain intermediate values. The CPU cannot read the Initial registers.

		Signals							Internal Flip-Flop	
Channel	Operation	$\overline{CS}$	$\overline{I/OR}$	$\overline{I/OW}$	A_3	A_2	A_1	A_0		D_0-D_7
0	Initial & Current Address Write	0	1	0	0	0	0	0	0	A_0-A_7
		0	1	0	0	0	0	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	0	0	0	0	A_0-A_7
		0	0	1	0	0	0	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	0	0	1	0	W_0-W_7
		0	1	0	0	0	0	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	0	0	1	0	W_0-W_7
		0	0	1	0	0	0	1	1	W_8-W_{15}
1	Initial & Current Address Write	0	1	0	0	0	1	0	0	A_0-A_7
		0	1	0	0	0	1	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	0	1	0	0	A_0-A_7
		0	0	1	0	0	1	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	0	1	1	0	W_0-W_7
		0	1	0	0	0	1	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	0	1	1	0	W_0-W_7
		0	0	1	0	0	1	1	1	W_8-W_{15}
2	Initial & Current Address Write	0	1	0	0	1	0	0	0	A_0-A_7
		0	1	0	0	1	0	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	1	0	0	0	A_0-A_7
		0	0	1	0	1	0	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	1	0	1	0	W_0-W_7
		0	1	0	0	1	0	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	1	0	1	0	W_0-W_7
		0	0	1	0	1	0	1	1	W_8-W_{15}
3	Initial & Current Address Write	0	1	0	0	1	1	0	0	A_0-A_7
		0	1	0	0	1	1	0	1	A_8-A_{15}
	Current Address Read	0	0	1	0	1	1	0	0	A_0-A_7
		0	0	1	0	1	1	0	1	A_8-A_{15}
	Initial & Current Word Count Write	0	1	0	0	1	1	1	0	W_0-W_7
		0	1	0	0	1	1	1	1	W_8-W_{15}
	Current Word Count Read	0	0	1	0	1	1	1	0	W_0-W_7
		0	0	1	0	1	1	1	1	W_8-W_{15}

Word Count and Address Register Command Codes

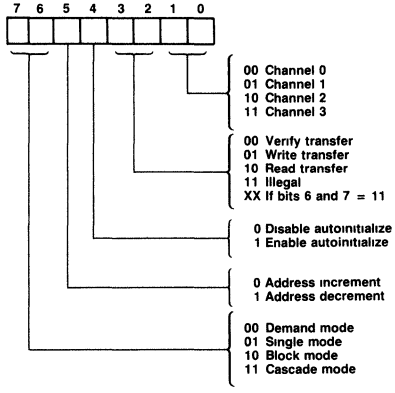
Command Register

The CPU programs this register during Program Phase. The register can be cleared with Reset.



Mode Register

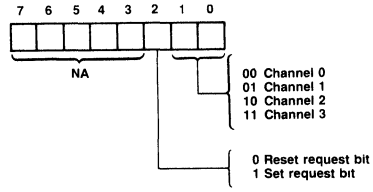
There is a Mode register associated with each channel. When the CPU writes to this register during the Program Phase, bits 0 and 1 determine on which channel Mode register the operation is performed.



Request Register

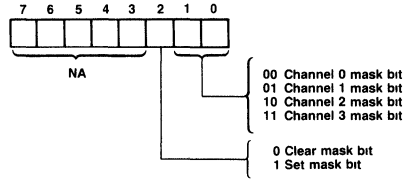
This register allows the μPD8237A-5 to respond to DMA requests from software as well as hardware. There is a bit pattern for each channel in the Request register. These bits can be prioritized by the Priority Resolving circuitry and are not maskable. Each bit is set or reset under software control or cleared when TC or an external $\overline{EOP}$ is generated. A Reset clears the entire register. The correct data word is loaded by software to set or reset a bit.

Software requests receive service only when the channel is in Block mode. The software request for channel 0 should be set at the beginning of a memory-to-memory transfer.

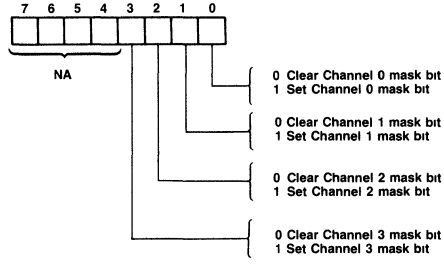


Mask Register

There is a mask bit for each channel which can disable an incoming DRQ. If the channel is not set for Autoinitialize, each mask bit is set when its channel produces an $\overline{EOP}$. Each bit can be set or cleared under software control. Reset clears the register. This disallows DMA requests until they are permitted by a Clear Mask Register instruction.

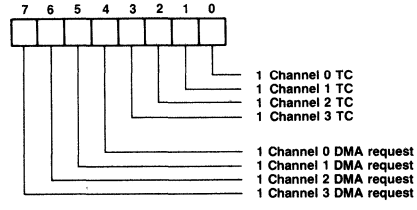


You may also write all four bits of the Mask register with a single command.



Status Register

The Status register indicates which channels have made DMA requests and which channels have reached TC. Each time a channel reaches TC, including after Autoinitialization, bits 0–3 are set. Status Read and Reset clear these bits. Bits 4–7 are set when a channel is requesting service. The CPU can read the Status register.



Temporary Register

The Temporary register holds data during memory-to-memory transfers. The CPU can read the last word moved when the transfer is complete. This register always contains the last byte transferred in a memory-to-memory transfer unless cleared by a Reset.

Software Commands

There are two software commands that can be executed in the Program Phase. These commands are independent of data on the data bus.

Clear First/Last Flip-Flop

You may issue this command before reading or writing any word count or address information. It allows the CPU to access registers, addressing upper and lower bytes correctly, by initializing the flip-flop to an identifiable state.

Master Clear

This command produces the same effect as Reset. It clears the Command, Status, Request, Temporary, and Internal First/Last Flip-Flop registers, sets the Mask register, and causes the μPD8237A-5 to enter Idle state.

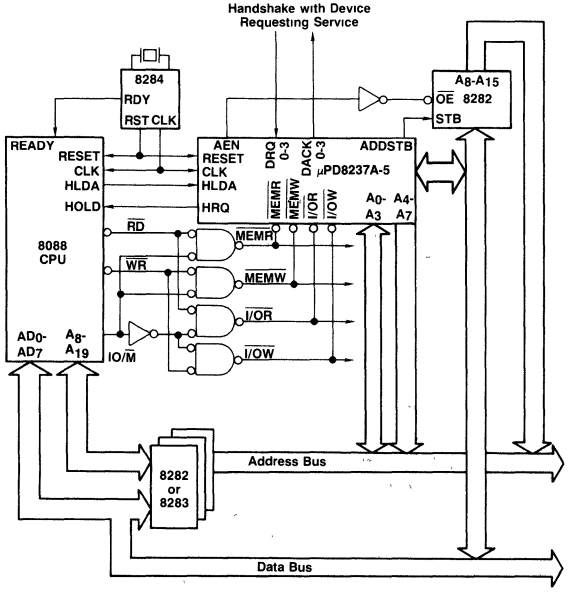
The following chart illustrates address codes for the software commands.

A_3	A_2	A_1	A_0	$\overline{I/OR}$	$\overline{I/OW}$	Operation
1	0	0	0	0	1	Read Status register
1	0	0	0	1	0	Write to Command register
1	0	0	1	1	0	Write to Request register
1	0	1	0	1	0	Write a Mask register bit
1	0	1	1	1	0	Write to Mode register
1	1	0	0	1	0	Clear byte pointer flip-flop
1	1	0	1	0	1	Read Temporary register
1	1	0	1	1	0	Master Clear
1	1	1	1	1	0	Write all Mask register bits
1	1	1	0	0	1	Clear Mask register

All other bit combinations are illegal.

Application Example

The following diagram shows an application using the μPD8237A-5 with an 8088. The μPD8237A-5 sends a hold request to the CPU whenever there is a valid DMA request from a peripheral device. The μPD8237A-5 takes control of the Address, Data, and Control buses when the CPU replies with an HLDA signal. The address for the first transfer appears in two bytes: the eight LSBs are output on A_0–A_7 and the eight MSBs are output on the data bus pins. The contents of the data bus pins are latched to the 8282 to make up the 16 bits of the address bus. Once the address is latched, the data bus transfers data to or from a memory location or I/O device, using the control bus signals generated by the μPD8237A-5.



AC Characteristics Supplementary Information

All AC timing measurement points are 2.0V for high and 0.8V for low, for both inputs and outputs. The loading on the outputs is one TTL gate plus 100 pF of capacitance for the data bus pins, and one TTL gate plus 50 pF for all other outputs.

Recovery time between successive read and write inputs must be at least 400 ns. I/O or memory write pulse widths will be T_{CY} – 100 ns for normal DMA transfers and 2 T_{CY} – 100 ns for extended cycles. I/O or memory reads will be 2 T_{CY} – 50 ns for normal reads and T_{CY} – 50 ns for compressed cycles. T_{DQ1} and T_{DQ2} are measured on two different levels. T_{DQ1} at 2.0V, T_{DQ2} at 3.3V with a 3.3 kΩ pull-up resistor. DREQ and DACK are both active high and low. DREQ must be held in the active state (user defined) until DACK is returned from the μPD8237A-5. The AC waveforms assume these are programmed to the active high state.

Absolute Maximum Ratings*

Tentative	
Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	−65°C to 150°C
Voltage on any Pin with respect to Ground	−0.5V to +7V
Power Dissipation	1.5 Watt

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

		Limits				
Parameter	Symbol	Min	Typ ①	Max	Unit	Test Conditions
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
		3 3			V	I_{OH} = −100 μA (HRQ Only)
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA (Data Bus)
						I_{OL} = 3.2 mA (Other Outputs)
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input Load Current	I_{LI}			±10	μA	$0V \leq V_{IN} \leq V_{CC}$
Output Leakage Current	I_{LO}			±10	μA	$0.45 \leq V_{OUT} \leq V_{CC}$
V_{CC} Supply Current	I_{CC}		65	130	mA	T_a = +25°C
			75	150	mA	T_a = 0°C

Note:

① Typical values measured at T_a = 25°C, nominal processing parameters, and nominal V_{CC}.

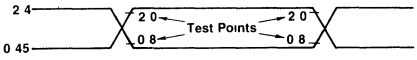
Capacitance

Parameter	Symbol	Limits Min	Typ ①	Max	Unit	Test Conditions
Output Capacitance	C_O		4	8	pF	fc = 1.0 MHz, Inputs = 0V
Input Capacitance	C_I		8	15	pF	
I/O Capacitance	C_{IO}		10	18	pF	

Note:

① Typical values measured at T_a = 25°C, nominal processing parameters, and nominal V_{CC}.

AC Testing Input/Output Waveform



Inputs are driven at 2.4V for logic 1 and 0.45V for logic 0. These timing measurements are made at 2.0V for logic 1 and 0.8V for logic 0. A transition time of 20 ns or less is assumed for input timing parameters. Unless noted, output loading is 1 TTL gate plus 50 pF capacitance.

AC Characteristics
DMA (Master) Mode
T_a = 0°C to +70°C; V_{CC} = 5V ± 5%; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit
AEN High from CLK Low (S1) Delay Time	t_{AEL}			200	ns
AEN Low from CLK High (S1) Delay Time	t_{AET}			130	ns
ADR Active to Float Delay from CLK High	t_{AFAB}			90	ns
$\overline{READ}$ or $\overline{WRITE}$ Float from CLK High	t_{AFC}			120	
DB Active to Float Delay from CLK High	t_{AFDB}			170	ns
ADR from $\overline{READ}$ High Hold Time	t_{AHR}	t_{CY} – 100			ns
DB from ADDSTB Low Hold Time	t_{AHS}	30			ns
ADR from $\overline{WRITE}$ High Hold Time	t_{AHW}	t_{CY} – 50			ns
DACK Valid from CLK Low Delay Time				170	ns
$\overline{EOP}$ High from CLK High Delay Time	t_{AK}			170	ns
$\overline{EOP}$ Low to CLK High Delay Time				100	ns
ADR Stable from CLK High	t_{ASM}			170	ns
Data Bus to ADDSTB Low Setup Time	t_{ASS}	100			ns
Clock High Time (Transitions ≤ 10 ns)	t_{CH}	80			ns
Clock Low Time (Transitions ≤ 10 ns)	t_{CL}	68			
CLK Cycle Time	t_{CY}	200			ns
CLK High to $\overline{READ}$ or $\overline{WRITE}$ Low Delay ①	t_{DCL}			190	ns
$\overline{READ}$ High from CLK High (S4) Delay Time ①	t_{DCTR}			190	ns
$\overline{WRITE}$ High from CLK High (S4) Delay Time ①	t_{DCTW}			130	ns
HRQ Valid from CLK High Delay Time ②	t_{DQ1}			120	ns
	t_{DQ2}			120	ns
$\overline{EOP}$ Low from CLK Low Setup Time	t_{EPS}	40			
$\overline{EOP}$ Pulse Width	t_{EPW}	220			ns
ADR Float to Active Delay from CLK High	t_{FAAB}			170	ns
$\overline{READ}$ or $\overline{WRITE}$ Active from CLK High	t_{FAC}			150	ns
Data Bus Float to Active Delay from CLK High	t_{FADB}			200	ns
HLDA Valid to CLK High Setup Time	t_{HS}	75			ns
Input Data from $\overline{MEMR}$ High Hold Time	t_{IDH}	0			ns
Input Data to $\overline{MEMR}$ High Setup Time	t_{IDS}	170			ns
Output Data from $\overline{MEMW}$ High Hold Time	t_{ODH}	10			ns
Output Data Valid to $\overline{MEMW}$ High	t_{ODV}	125			ns
DRQ to CLK Low (S_1, S_4) Setup Time	t_{QS}	0			ns
CLK to READY Low Hold Time	t_{RH}	20			ns
READY to CLK Low Setup Time	t_{RS}	60			ns
ADDSTB High from CLK High Delay Time	t_{STL}			130	ns
ADDSTB Low from CLK High Delay Time	t_{STT}			90	ns

Notes:

① Net $\overline{I/OW}$ or $\overline{MEMW}$ pulse width for normal write is t_{CY} – 100 ns and $2t_{CY}$ – 100 ns for extended write. Net $\overline{I/OR}$ or $\overline{MEMR}$ pulse width for normal read is $2t_{CY}$ – 50 ns and t_{CY} – 50 ns for compressed read.

② T_{DQ1} is measured at 2.0V. t_{DQ2} is measured at 3.3V. An external pullup resistor of 3.3kΩ connected from HRQ to V_{CC} is assumed for t_{DQ2}.

AC Characteristics Peripheral Mode
T_a = 0°C to +70°C; V_{CC} = 5V ± 5%; V_{SS} = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit
ADR Valid or $\overline{CS}$ Low to $\overline{READ}$ Low	t_{AR}	50			ns
ADR Valid to $\overline{WRITE}$ High Setup Time	t_{AW}	150			ns
$\overline{CS}$ Low to $\overline{WRITE}$ High Setup Time	t_{CW}	150			ns
Data Valid to $\overline{WRITE}$ High Setup Time	t_{DW}	150			ns
ADR or $\overline{CS}$ Hold from $\overline{READ}$ High	t_{RA}	0			ns
Data Access from $\overline{READ}$ Low ①	t_{RDE}			140	ns
Data Bus Float Delay from $\overline{READ}$ High	t_{RDF}	0		70	ns
Power Supply High to RESET Low Setup Time	t_{RSTD}	500			ns
RESET to First $\overline{I/OR}$ or $\overline{I/OW}$	t_{RSTS}	$2t_{CY}$			ns
RESET Pulse Width	t_{RSTW}	300			ns
$\overline{READ}$ Width	t_{RW}	200			ns
ADR from $\overline{WRITE}$ High Hold Time	t_{WA}	20			ns
$\overline{CS}$ High from $\overline{WRITE}$ High Hold Time	t_{WC}	20			ns
Data from $\overline{WRITE}$ High Hold Time	t_{WD}	30			ns
Write Width	t_{WWS}	160			ns

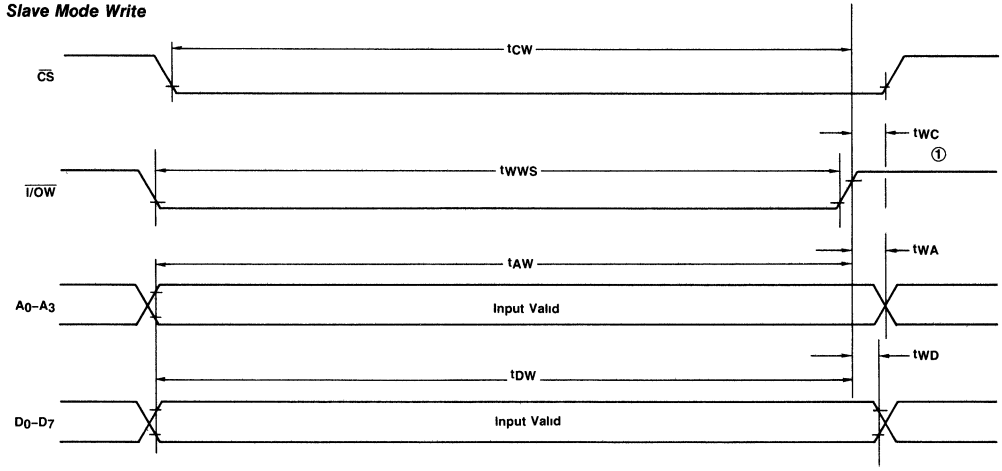
Note:

① Data bus output loading is 1 TTL gate plus 100 pF capacitance.

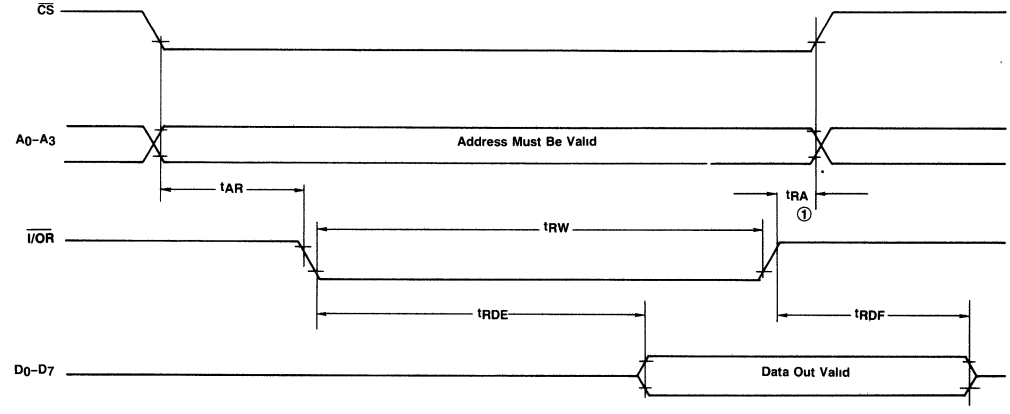
6

Timing Waveforms

Slave Mode Write



Slave Mode Read

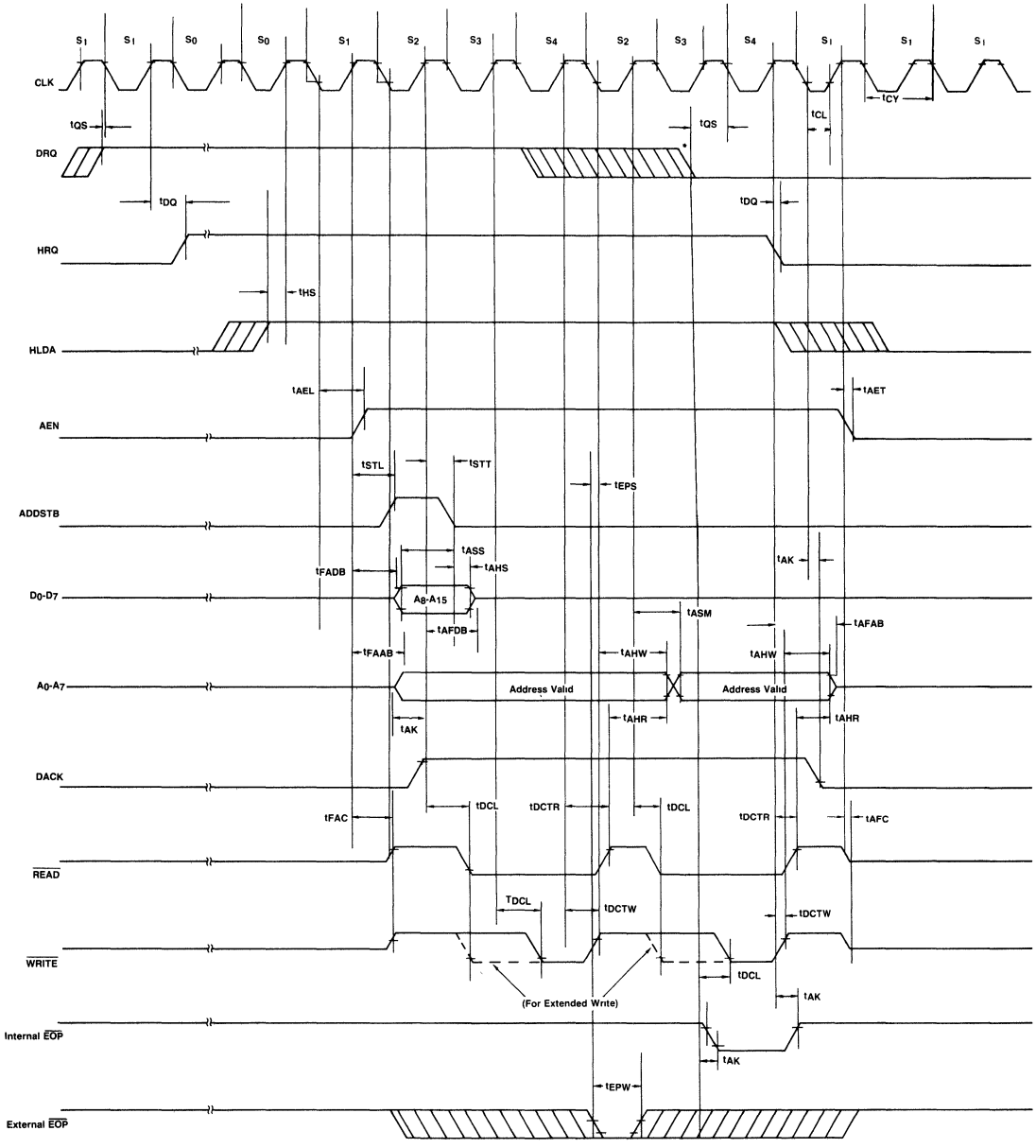


Note:

① You must time successive read or write operations by the CPU to allow at least 400 ns recovery time for the μPD8237A-5 between read and write pulses.

Timing Waveforms (Cont.)

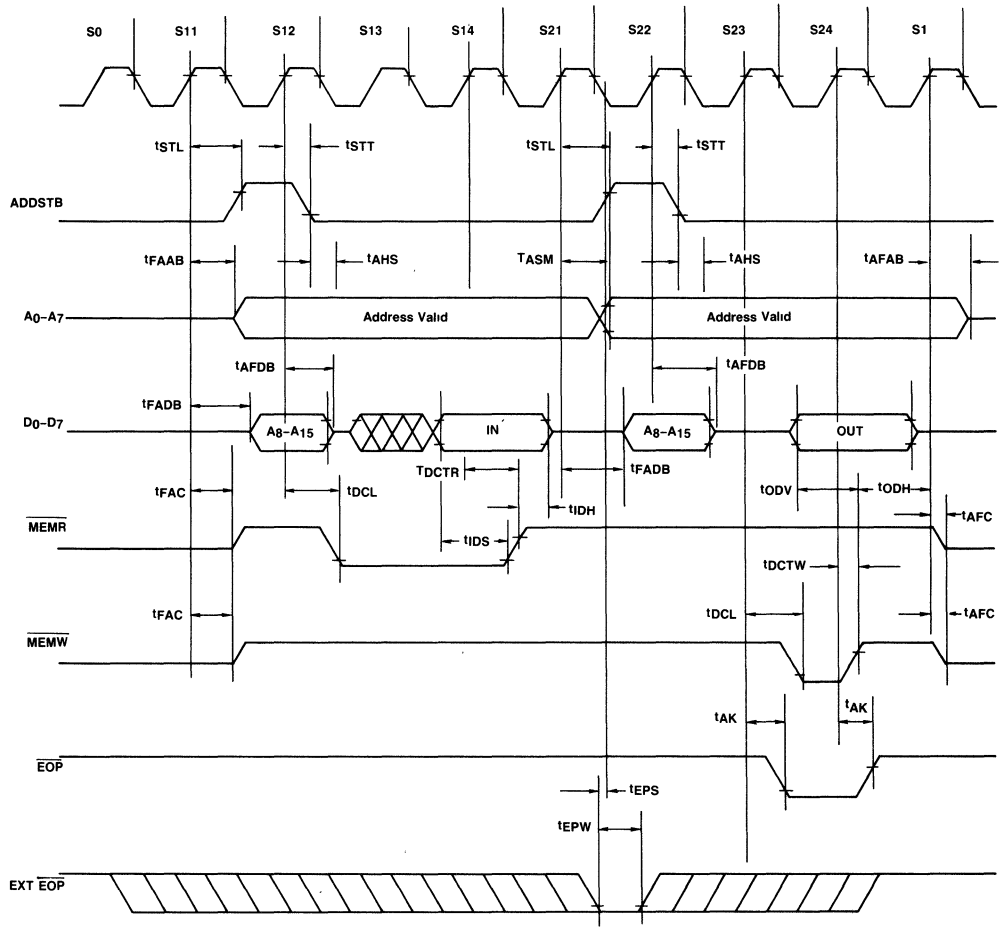
DMA Transfer



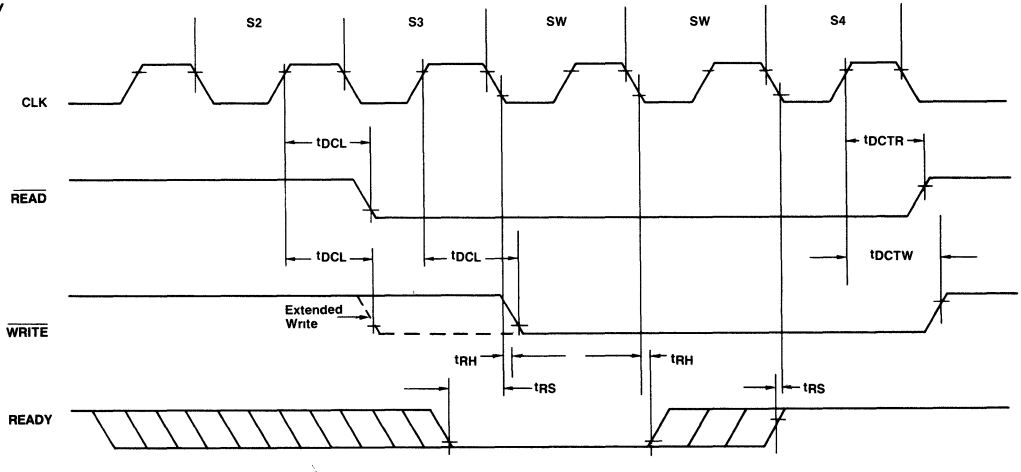
*See Note 2, AC Characteristics, DMA Mode

Timing Waveforms (Cont.)

Memory-to-Memory Transfer

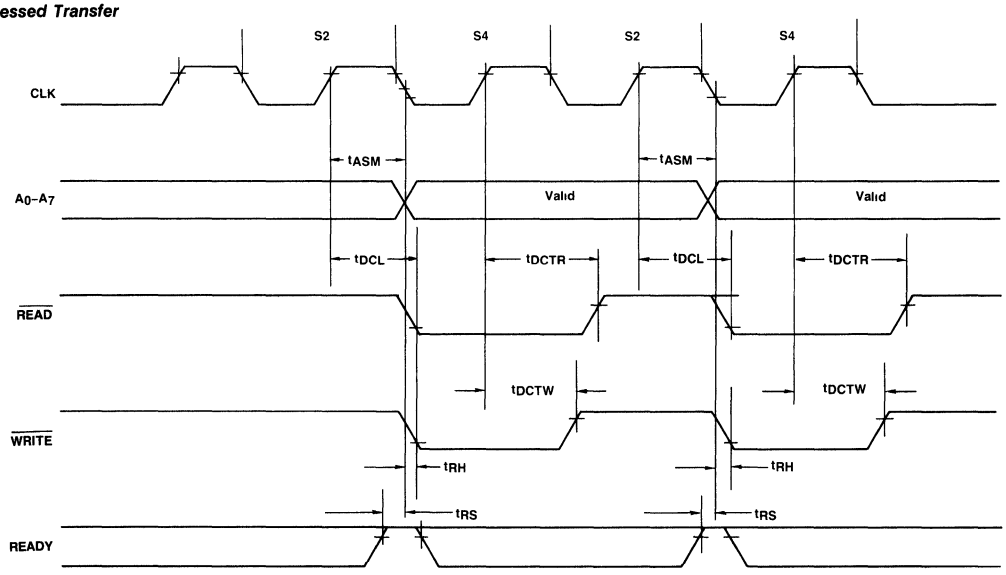


Ready

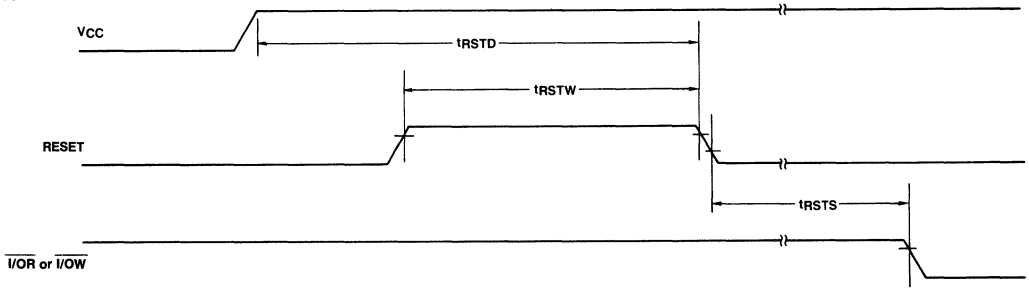


Timing Waveforms (Cont.)

Compressed Transfer



Reset



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8237C-5
Ceramic, μPD8237D-5
Cerdip, μPD8237AD-5

INPUT/OUTPUT EXPANDER FOR μPD8048 FAMILY

DESCRIPTION

The μPD8243 input/output expander is directly compatible with the μPD8048 family of single-chip microcomputers. Using NMOS technology the μPD8243 provides high drive capabilities while requiring only a single +5V supply voltage.

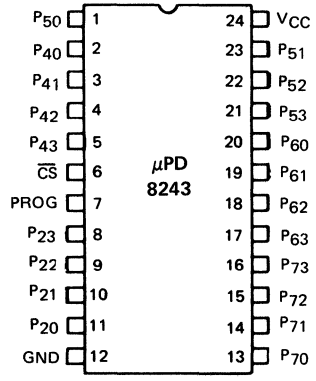
The μPD8243 interfaces to the μPD8048 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple μPD8243's to be added using the bus port.

The bi-directional I/O ports of the μPD8243 act as an extension of the I/O capabilities of the μPD8048 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with μPD8048 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident μPD8048 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in a 24-Pin Plastic Package

6



FUNCTIONAL DESCRIPTION

General Operation

The I/O capabilities of the μPD8048 family can be enhanced in four 4-bit I/O port increments using one or more μPD8243's. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 (P_{20}-P_{23}) forms the 4-bit bus through which the μPD8243 communicates with the host processor. The PROG output from the μPD8048 family provides the necessary timing to the μPD8243. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD8243's can be used for additional I/O. The output lines from the μPD8048 family can be used to form the chip selects for the additional μPD8243's.

Power On Initialization

Applying power to the μPD8243 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time V_{CC} drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD8243 operations.

Port Address			Op-Code		
P_{21}	P_{20}	Address Code	P_{23}	P_{22}	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

For example an 0010 appearing on P_{20}-P_{23}, respectively, would result in a Write to Port 4.

Read Mode

There is one Read mode in the μPD8243. A falling edge on the PROG pin latches the op-code and port address from input Port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The Port (4,5,6, or 7) that was selected by the Port address (P_{21}-P_{20}) is returned to the tri-state mode, and Port 2 is switched to the input mode.

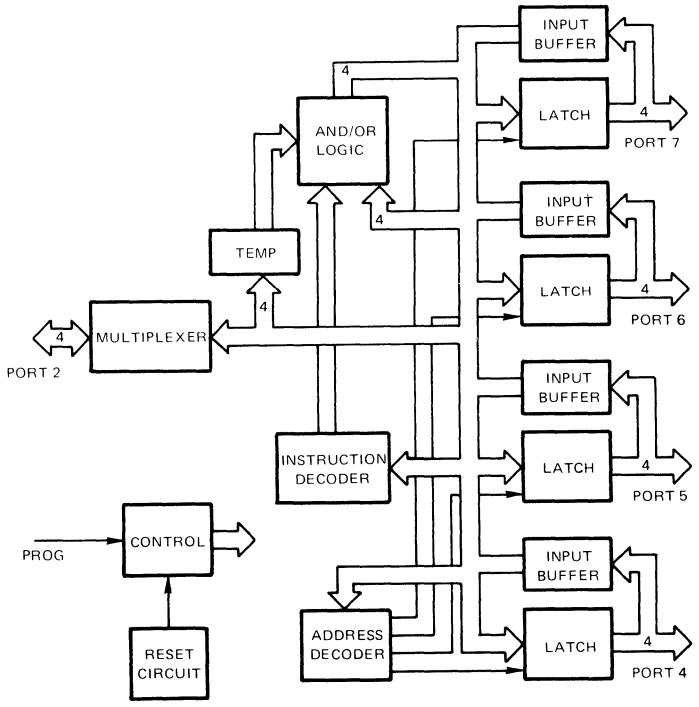
Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD8243's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

Write Modes

There are three write modes in the μPD8243. The MOVD $P_{p,A}$ instruction from the μPD8048 family writes the new data directly to the specified port (4,5,6, or 7). The old data previously latched at that port is lost. The ORLD $P_{p,A}$ instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD $P_{p,A}$ instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
2-5 1, 21-23 17-20 13-16	P_{40}-P_{43} P_{50}-P_{53} P_{60}-P_{63} P_{70}-P_{73}	The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines P_{20}-P_{23} can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines.
6	$\overline{CS}$	Chip Select input (active-low). When the μPD8343 is deselected ($\overline{CS}$ = 1), output or internal status changes are inhibited.
7	PROG	Clock input pin. The control and address information are present on port lines P_{20}-P_{23} when PROG makes a high-to-low transition. Data is present on port lines P_{20}-P_{23} when PROG makes a low-to-high transition.
8-11	P_{20}-P_{23}	P_{20}-P_{23} form a 4-bit bi-directional port. Refer to PROG function for contents of P_{20}-P_{23} at the rising and falling edges of PROG. Data from a selected port is present on P_{20}-P_{23} prior to the rising edge of PROG if during a Read operation.
12	GND	The μPD8041/8741 ground potential.
24	V_{CC}	+5 volt supply.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts①
Power Dissipation	1 W

Note: ① With respect to ground.

T_a = 25°C

*COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	0.8	V	
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.5	V	
Output Low Voltage (Ports 4-7)	V_{OL1}		0.45	V	I_{OL} = 4.5 mA①
Output Low Voltage (Port 7)	V_{OL2}		1	V	I_{OL} = 20 mA
Output Low Voltage (Port 2)	V_{OL3}		0.45	V	I_{OL} = 0.6 mA
Output High Voltage (Ports 4-7)	V_{OH1}	2.4		V	I_{OH} = 240 μA
Output High Voltage (Port 2)	V_{OH2}	2.4		V	I_{OH} = 100 μA
Sum of All I_{OL} From 16 Outputs	I_{OL}		100 (8243) 80 (8243H)	mA	5 mA Each Pin
Input Leakage Current (Ports 4-7)	I_{IL1}	-10	20	μA	V_{IN} = V_{CC} to 0V
Input Leakage Current (Port 2, $\overline{CS}$, PROG)	I_{IL2}	-10	10	μA	V_{IN} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}		20	mA	

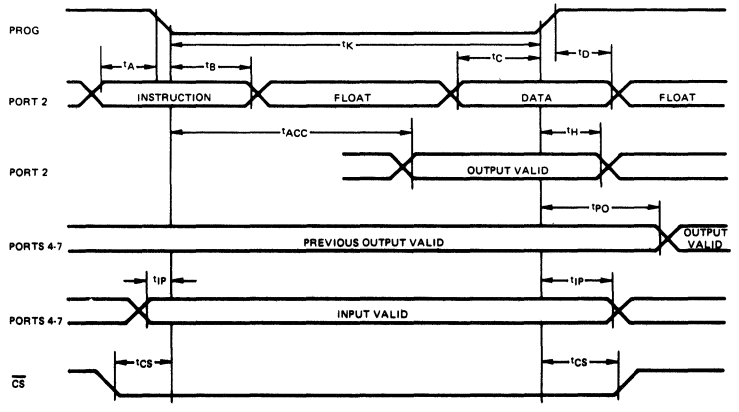
Note ① Refer to graph of additional sink current drive

AC CHARACTERISTICS

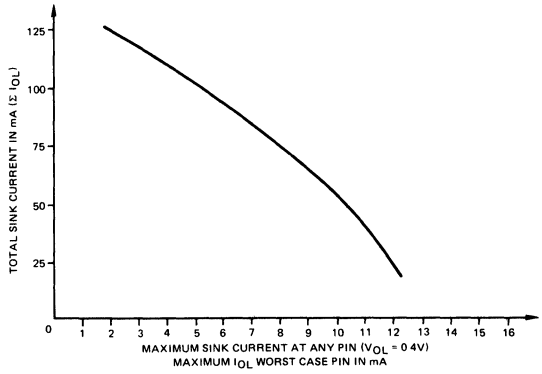
T_a = 0°C to +70°C; V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
Code Valid Before PROG	t_A	100		ns	80 pF Load
Code Valid After PROG	t_B	60		ns	20 pF Load
Data Valid Before PROG	t_C	200		ns	80 pF Load
Data Valid After PROG	t_D	20		ns	20 pF Load
Port 2 Floating After PROG	t_H	0	150	ns	20 pF Load
PROG Negative Pulse Width	t_K	700		ns	
Ports 4-7 Valid After PROG	t_{PO}		700	ns	100 pF Load
Ports 4-7 Valid Before/After PROG	t_{LP1}	100		ns	
Port 2 Valid After PROG	t_{ACC}		650	ns	80 pF Load
$\overline{CS}$ Valid Before/After PROG	$t_{\overline{CS}}$	50		ns	

TIMING WAVEFORMS



CURRENT SINKING CAPABILITY ①



Note ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins

The μPD8243 is capable of sinking 5 mA (for V_{OL} = 0.4V) through each of the 16 I/O lines simultaneously The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8243C
Ceramic, μPD8243D
Cerdip, μPD8243D

6

Notes

CMOS INPUT/OUTPUT EXPANDER FOR μPD8048/80C48 FAMILY

DESCRIPTION

The μPD82C43 input/output expander is directly compatible with the μPD8048/80C48 family of single-chip microcomputers. Using NMOS technology the μPD82C43 provides high drive capabilities while requiring only a single +5V supply voltage.

The μPD82C43 interfaces to the μPD8048/80C48 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple μPD8243s to be added using the bus port.

The bi-directional I/O ports of the μPD82C43 act as an extension of the I/O capabilities of the μPD8048/80C48 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with μPD8048/80C48 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident μPD8048/80C48 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in a 24-Pin Plastic Package

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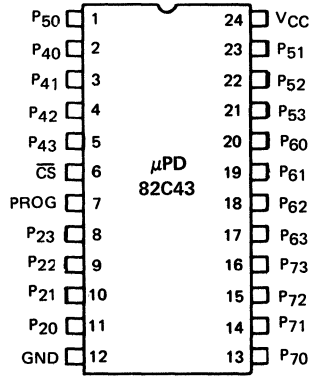


FUNCTIONAL DESCRIPTION

General Operation

The I/O capabilities of the μPD8048/80C48 family can be enhanced in four 4-bit I/O port increments using one or more μPD82C43s. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 (P_{20}-P_{23}) forms the 4-bit bus through which the μPD82C43 communicates with the host processor. The PROG output from the μPD8048/80C48 family provides the necessary timing to the μPD82C43. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD82C43s can be used for additional I/O. The output lines from the μPD8048/80C48 family can be used to form the chip selects for the additional μPD82C43s.

Power On Initialization

Applying power to the μPD82C43 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time V_{CC} drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD82C43 operations.

Port Address			Op-Code		
P_{21}	P_{20}	Address Code	P_{23}	P_{22}	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

For example an 0010 appearing on P_{20}-P_{23}, respectively, would result in a Write to Port 4.

Read Mode

There is one Read mode in the μPD82C43. A falling edge on the PROG pin latches the op-code and port address from input port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The port (4, 5, 6, or 7) that was selected by the port address (P_{21}-P_{20}) is returned to the tri-state mode, and port 2 is switched to the input mode.

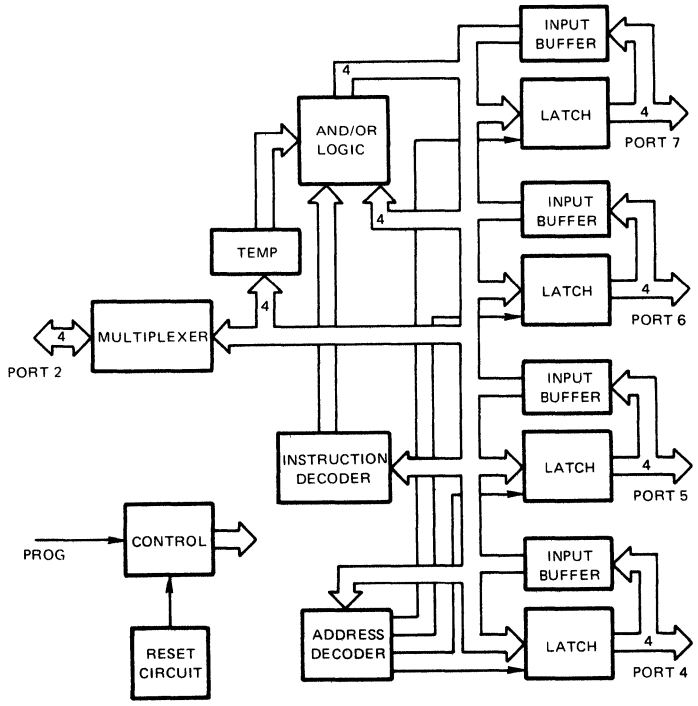
Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD82C43's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

Write Modes

There are three write modes in the μPD82C43. The MOVD P_p,A instruction from the μPD8048/80C48 family writes the new data directly to the specified port (4, 5, 6, or 7). The old data previously latched at that port is lost. The ORLD Pp,A instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD Pp,A instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
2-5 1, 21-23 17-20 13-16	P_{40}-P_{43} P_{50}-P_{53} P_{60}-P_{63} P_{70}-P_{73}	The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines P_{20}-P_{23} can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines.
6	$\overline{CS}$	Chip Select input (active-low). When the μPD82C43 is deselected (CS = 1), output or internal status changes are inhibited.
7	PROG	Clock input pin. The control and address information are present on port lines P_{20}-P_{23} when PROG makes a high-to-low transition. Data is present on port lines P_{20}-P_{23} when PROG makes a low-to-high transition.
8-11	P_{20}-P_{23}	P_{20}-P_{23} form a 4-bit bi-directional port. Refer to PROG function for contents of P_{20}-P_{23} at the rising and falling edges of PROG. Data from a selected port is present on P_{20}-P_{23} prior to the rising edge of PROG if during a Read operation.
12	GND	The μPD8041/8741 ground potential.
24	V_{CC}	+5 volt supply.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts①
Power Dissipation	1 W
Supply Voltage	−0.3 to +10V
Input, Output Voltage	−0.3 to V_{CC} +0 3V

Note: ① With respect to ground.

*T_a = 25°C

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = −40°C to +85°C V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	0 3		0 8	V	
Input High Voltage	V_{IH}	V_{CC} - 2 0		V_{CC}	V	
Output Low Voltage (Ports 4 7)	V_{OL1}			0 45	V	I_{OL} 5 mA ①
Output Low Voltage (Port 7)	V_{OL2}			1	V	I_{OL} + 20mA
Output Low Voltage (Port 2)	V_{OL3}			0 45	V	I_{OL} = 0 6 mA
Output High Voltage (Ports 4 7)	V_{OH1}	V_{CC} - 0 5			V	I_{OH} = −240μA
Output High Voltage (Port 2)	V_{OH2}	V_{CC} - 0 5			V	I_{OH} = −100μA
Sum of All I_{OL} From 16 Outputs	I_{OL}			80	mA	5 mA Each Pin
Input Leakage Current (Ports 4 7)	I_{IL1}			±1	μA	V_{IN} = V_{CC} to 0V
Input Leakage Current (Port 2, $\overline{CS}$, PROG)	I_{IL2}			±1	μA	V_{IN} - V_{CC} to 0V
V_{CC} Supply Current	I_{CC_1}		100	300	μA	
Power Down Supply Current	I_{CC2}		1	10	μA	

Note ① Refer to graph of additional sink current drive

T_a = −40°C ~ +85°C, V_{CC} = +2.5V ~ +6V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0 3		0 18V_{CC}	V	
Input High Voltage	V_{IH}	0 7V_{CC}		V_{CC}	V	
Output Low Voltage	V_{OL1}			+ 0 45	V	Port 4-7, I_{OL} = 2 5mA
	V_{OL2}			+ 1	V	Port 7, I_{OL} = 7mA
	V_{OL3}			+ 0 45	V	Port 2, I_{OL} = 0 3mA
Output High Voltage	V_{OH1}	0 75V_{CC}			V	Port 4-7, I_{OH} = −120μA
	V_{OH2}	0 75V_{CC}			V	Port 2, I_{OH} = −50μA
Input Leakage Current	I_{IL1}			± 1	μA	Port 4-7, V_{IN} OV V_{CC}
	I_{IL2}			± 1	μA	Port 2, $\overline{CS}$, PROG, V_{IN} = V_{CC} DV
Supply Current	I_{CC1}		1	IO	μA	STANDBY MODE
	I_{CC2}		100	300	μA	OPERATION MODE (I_{OH} = OμA, PROG Pulse Cycle = 5μs (MIN)
Output Current (Low)	I_{OL}			40	mA	Port 4-7, 2 5mA Each Pin

AC CHARACTERISTICS

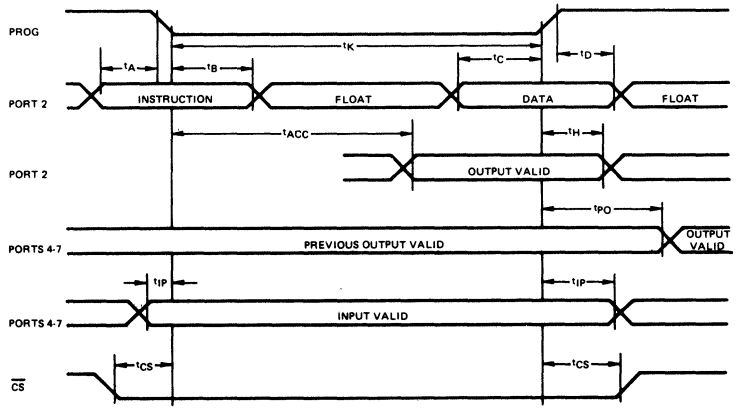
T_a = 40°C to +85°C, V_{CC} = +5V ±10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Code Valid Before PROG	t_A	100			ns	80 pF Load
Code Valid After PROG	t_B	0			ns	20 pF Load
Data Valid Before PROG	t_C	200			ns	80 pF Load
Data Valid After PROG	t_D	20			ns	20 pF Load
Port 2 Floating After PROG	t_H	0		150	ns	20 pF Load
PROG Negative Pulse Width	t_K	700			ns	
Ports 4-7 Valid After PROG	t_{PO}			700	ns	100 pF Load
Ports 4-7 Valid Before/After PROG	t_{IP}	100			ns	
Port 2 Valid After PROG	t_{ACC}	90		650	ns	80 pF Load
$\overline{CS}$ Valid Before/After PROG	$t_{\overline{CS}}$	50			ns	

T_a = −40°C ~ +85°C, V_{CC} = +2.5V ~ + 6V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Command Input Setup Time to PROG ↓	t_A	300			ns	Port 2 (Control, Port, Address), 80pF Load
Command Input Hold Time after PROG ↓	t_B	0			ns	Port 2, (Control, Port, Address), 20pF Load
Data Input Setup Time to PROG ↑	t_C	600			ns	Port 2, (Write Mode), 80pF Load
Data Input Hold Time after PROG ↑	t_D	80			ns	Port 2, (Write Mode), 20pF Load
Data Float Delay Time from PROG ↑	t_H	0		400	ns	Port 2, (Read Mode), 20pF Load
PROG Pulse Width	t_K	2			μs	
$\overline{CS}$ Input Setup Time to PROG ↓ $\overline{CS}$ Input Hold Time after PROG ↑	t_{CS}	200			ns	
Data Output Delay Time from PROG ↑	t_{PO}			2	μs	Port 4 7 100pF Load
Data Input Setup Time to PROG ↓ Data Input Hold Time after PROG ↑	t_{IP}	100			ns	Port 4 7
Data Output Delay Time from PROG ↓	t_{ACC}	*		3 5	μs	Port 2, 80pF Load

TIMING WAVEFORMS



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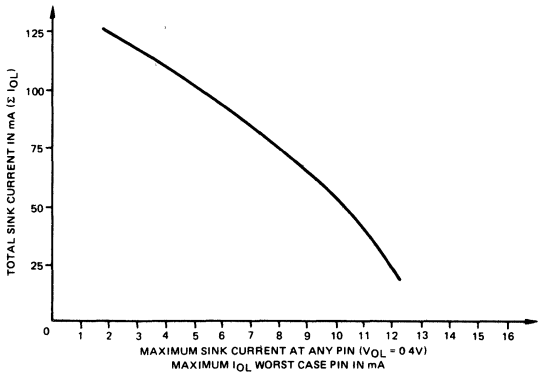
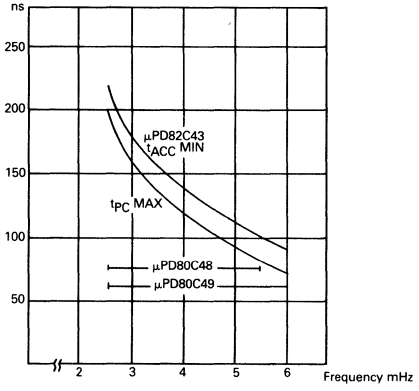
CURRENT SINKING CAPABILITY ①



Note. ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins

The μPD82C43 is capable of sinking 5 mA (for V_{OL} 0 4V) through each of the 16 I/O lines simultaneously The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded

t_{ACC}(MIN)/μPD82C43 vs t_{PC}(MAX)/μPD80C48, 49



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD82C43C
Cerdip, μPD82C43D
Plastic Skinnydip, μPD82C43CX

PROGRAMMABLE COMMUNICATION INTERFACES

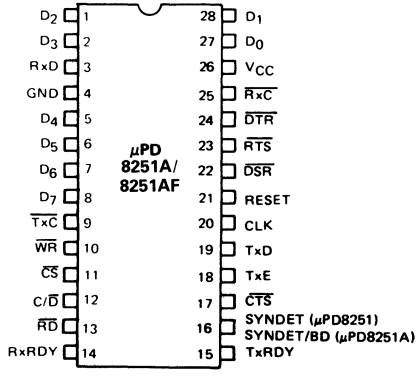
DESCRIPTION

The μPD8251A/AF Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the 8080A or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - Five 8-Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
    - Automatic Break Detect and Handling (μPD8251A)
  - Synchronous:
    - Five 8-Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate (1X Mode) – DC to 64K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080A/8085/μPD780 (Z80™)
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply, ± 10%
- Separate Device Receive and Transmit TTL Clocks
- 28 Pin Plastic,Cerdip,and Ceramic DIP Packages
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

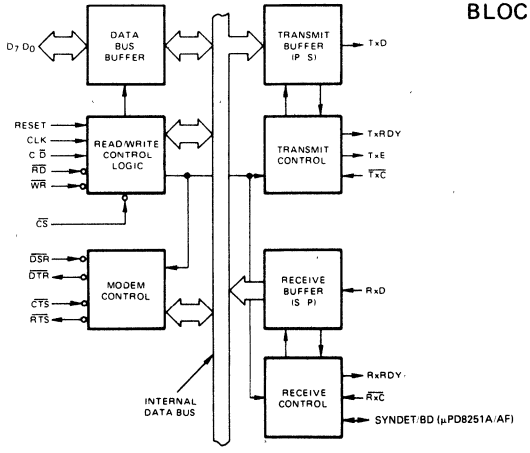
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
SYNDET/BD	Sync Detect/Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

6

TM: Z80 is a registered trademark of Zilog, Inc.

*Preliminary

BLOCK DIAGRAM



μPD8251AF ENHANCEMENTS

	PRESENT μPD8251A	NEW μPD8251AF
1.	A previously loaded data character will be retransmitted if Tx was disabled before TxEMPTY by TxEnable ↓ or $\overline{CTS}$ ↑, and is re-enabled by TxEnable ↑ or $\overline{CTS}$ ↓ before a new data character is sent to μPD8251A by CPU. CPU.	A previously loaded character will be flushed out and not transmitted on $\overline{CTS}$ ↓ or TxEnable ↑.
2.	Break Detect does not always reset upon RxData returning to a '1' during the last bit of the character following the break. Break detect will latch up, and the device must be cleared by device Reset.	Break Detect will reset on RxData going to '1'.
3.	On TxEnable ↓ or $\overline{CTS}$ ↑ during the first character of a double-character sync output, the second sync character will not be output.	Will output both sync characters on TxEnable ↓ or $\overline{CTS}$ ↑.
4.	If the Status Register is read during a status update, an erroneous status read may result.	Some valid status (either new or old) will always be available.
5.	In Rx mode, a hardware or software reset does not force asynchronous mode, clear hunt condition or require a proper line initialization (1 to 0 transition) before receiving. This may cause reception of garbage characters.	Reset will clear Rx hunt condition, force asynchronous operation (64X clock), and require a proper line initialization before receiving anything.
6.	Break Detect will occur on the first complete (start bit to stop bit) break. This situation could be confused with a null frame (all zeroes) that also has a framing error.	Will give a framing error at the end of the first complete or partial break and will give a Break Detect at the stop bit position of the second contiguous break character.
7.	Sync Detect does not reset on status read.	Sync Detect will reset on status read.
8.	RxRDY clears within 2 tCY's of $\overline{RD}$ leading edge.	RxRDY will clear on $\overline{RD}$ leading edge.
9.	TxEMPTY oscillates with internal clock when TxEnable ↓ or $\overline{CTS}$ ↑.	TxEMPTY will not oscillate this way.
10.	TxRDY and TxEMPTY clear on $\overline{WR}$ trailing edge (data).	TxRDY, TxEMPTY will clear on $\overline{WR}$ leading edge.
11.	Enter hunt command affects asynchronous Rx by loss of data characters.	Enter hunt will not affect asynchronous operation.
12.	Writing a command will sometimes clear TxRDY or TxEMPTY if C/$\overline{D}$ set up or hold is marginal. Reading status will sometimes clear RxRDY if C/$\overline{D}$ set up or hold is marginal.	C/$\overline{D}$ set up and hold margin will be improved.
13.	Rx data overrun error will not occur and garbage data may result if $\overline{RD}$ and $\overline{CS}$ are active during an internal data update.	Will indicate an overrun error properly.
14.	In asynchronous mode, after a reset, the first TxD bit may be shifted out on either the first or second $\overline{TxC}$ ↓ edge.	The first TxD bit will be shifted out on the first $\overline{TxC}$ ↓ edge.
15.	RxRDY can glitch when CLK does not have a fixed phase relationship to $\overline{RxC}$.	RxRDY will not glitch.
16.	The receiver occasionally gives an extra character following the end of Break condition.	No extra characters will occur.

FUNCTIONAL DESCRIPTION

The μPD8251A/AF Universal Synchronous/Asynchronous Receiver/Transmitters are designed specifically for 8080 microcomputer systems but work with most 8-bit processors. Operations of the μPD8251A/AF, like other I/O devices in the 8080 family, are programmed by system software for maximum flexibility.

In the receive mode, the μPD8251A/AF converts incoming serial format data into parallel data and makes certain format checks. In the transmit mode, it formats parallel data into serial form. The device also supplies or removes characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BASIC OPERATION

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	μPD8251A/AF → Data Bus
0	1	0	0	Data Bus → μPD8251A/AF
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the USART to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/Write Control Logic

PIN			FUNCTION
NO	SYMBOL	NAME	
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is 6 t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be at least 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the USART to accept the data or control word which the processor is writing out on the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the USART to place the data or status information onto the Data Bus for the processor to read
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the USART to accept or provide either a data character, control word or status information via the Data Bus 0 = Data, 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART to read from or write to the processor.
Modem Control			**The μPD8251A/AF have a set of control inputs and outputs which may be used to simplify the interface to a Modem.**
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one)

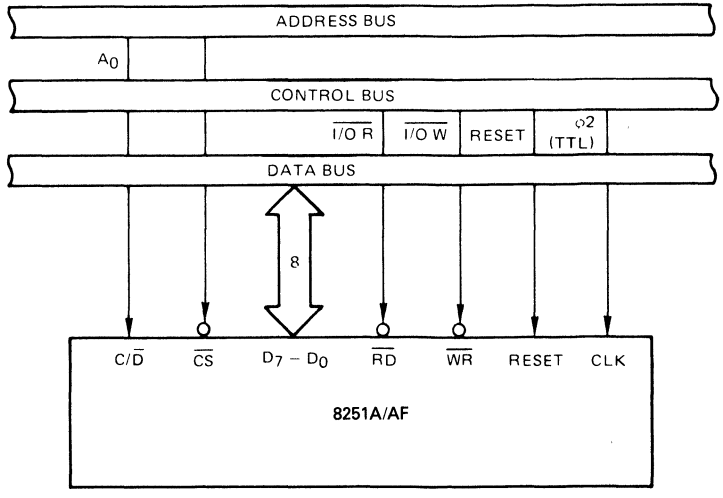
TRANSMIT BUFFER

The Transmit Buffer receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD pin.

PIN IDENTIFICATION (CONT.)

PIN			FUNCTION
NO.	SYMBOL	NAME	
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for polled operation. Loading a character from the processor automatically resets TxRDY, on the leading edge.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

μPD8251A/AF INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVE BUFFER

The Receive Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251A/AF set the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure Note that reading the character to the processor automatically resets RxRDY
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock determines the rate at which the incoming character is received In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1.16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate Unlike $\overline{TxC}$, data is sampled by the μPD8251A/AF on the rising edge of $\overline{RxC}$. ①
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin
16	SYNDET (μPD8251)	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251A/AF may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251A/AF has located the SYNC character in the Receive mode If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251A/AF to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251A/AF is in SYNC.
16	SYNDET/BD (μPD8251A/AF)	Sync Detect/ Break Detect	The SYNDET/BD pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the Break Detect output will go high which all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx data returns to a logic one state or upon chip reset. The state of Break Detect can be read as a status bit.

Note: ① Since the μPD8251A/AF will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be the same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples

If the Baud Rate equals 110 (Async)	If the Baud Rate equals 300.
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)	$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)	$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)	$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251A/AF to define the desired mode and communications format. The control words will specify the BAUD rate factor (1x, 16x, 64x), character length (5 to 8), number of STOP bits (1, 1-1/2, 2) Asynchronous or Synchronous mode, SYNDET (IN or OUT), parity, etc.

After receiving the control words, the μPD8251A/AF are ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251A/AF may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251A/AF may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251A/AF cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new control words.

USART PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A RESET (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the μPD8251A/AF.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

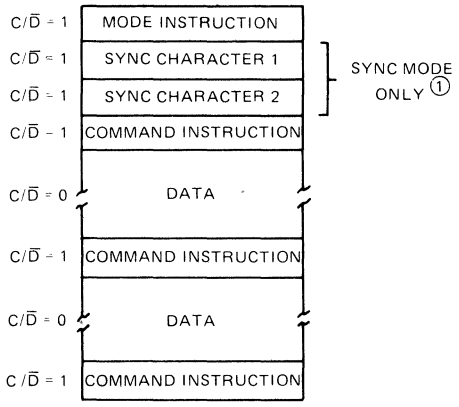
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the Synchronous or Asynchronous mode, BAUD rate factor, character length, parity, and number of stop bits. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the μPD8251A/AF to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the μPD8251A/AF to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251A/AF can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components (one asynchronous and the other synchronous) which share the same support circuits and package. Although the format definition can be changed at will or "on the fly," the two modes will be explained separately for clarity.

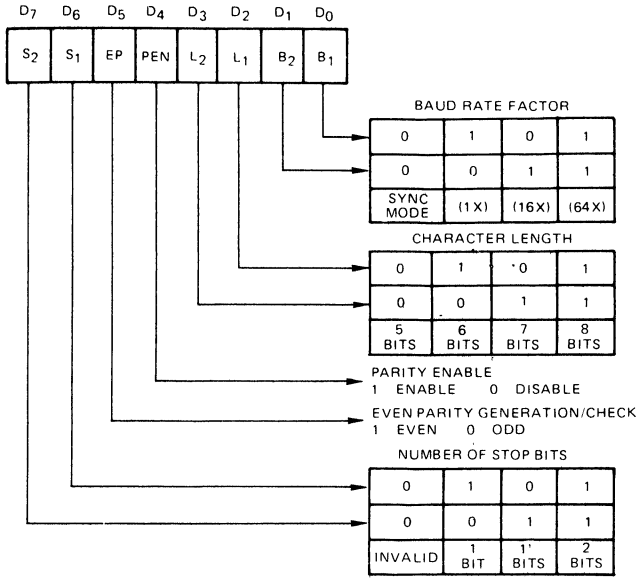
ASYNCHRONOUS TRANSMISSION

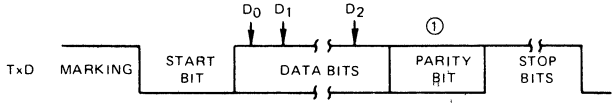
When a data character is written into the μPD8251A/AF, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251A/AF, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

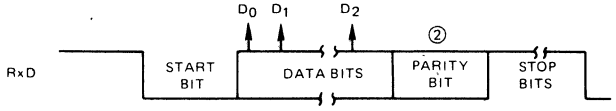
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input **character is loaded into the parallel Data Bus Buffer of the μPD8251A/AF and the RxRDY signal is raised to indicate to the processor that a character is ready to** be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

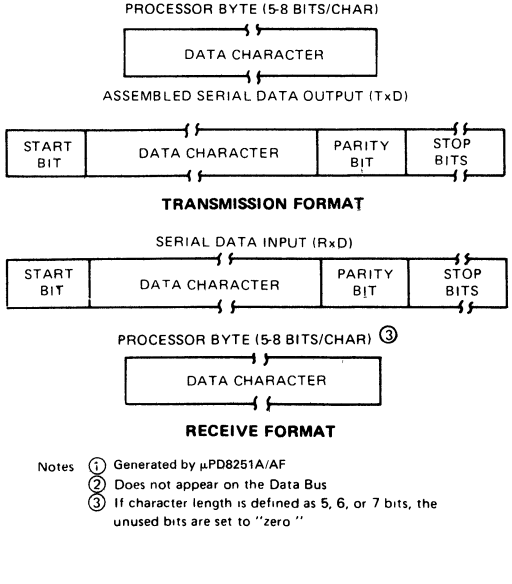




TRANSMITTER OUTPUT



RECEIVER INPUT



TRANSMISSION FORMAT

RECEIVE FORMAT

Notes
① Generated by μPD8251A/AF
② Does not appear on the Data Bus
③ If character length is defined as 5, 6, or 7 bits, the unused bits are set to "zero"

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SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251A/AF receive the first character (usually a SYNC character) from the processor. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251A/AF Transmit Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251A/AF become empty, and must send the SYNC characters(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

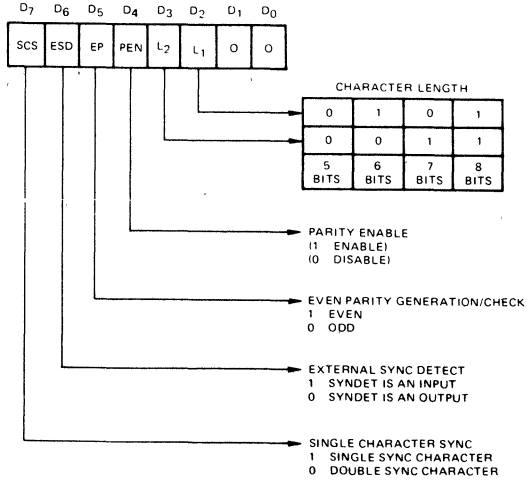
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receive Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251A/AF leave the HUNT mode and are in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

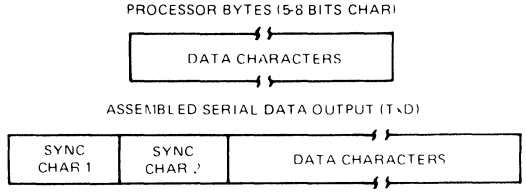
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. If not in HUNT, parity will continue to be checked even if the receiver is not enabled. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

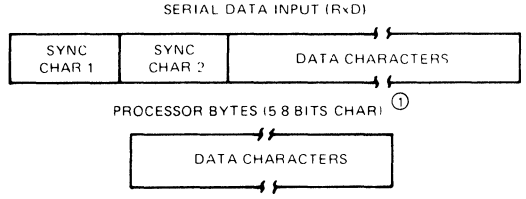
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

Note ① If character length is defined as 5, 6 or 7 bits, the unused bits are set to "zero."

COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251A/AF has been specified by the Mode Instruction and the SYNC character(s) have been entered (if in SYNC mode), the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s) (as needed) are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251A/AF to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the status of an active interface device to determine if errors have occurred or if there are other conditions which require a response from the processor. The μPD8251A/AF have features which allow the processor to read the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251A/AF to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of 28 clock periods in the μPD8251A/AF.

PARITY ERROR

When a parity error is detected, the PE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

If the processor fails to read a data character before the one following is available, the OE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

If a valid STOP bit is not detected at the end of a character, the FE flag is set. It is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note. ① ASYNC mode only.

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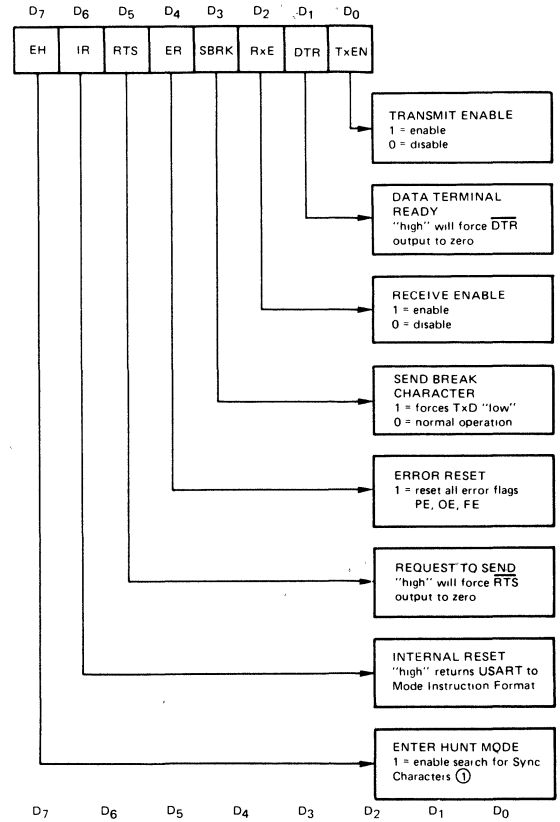
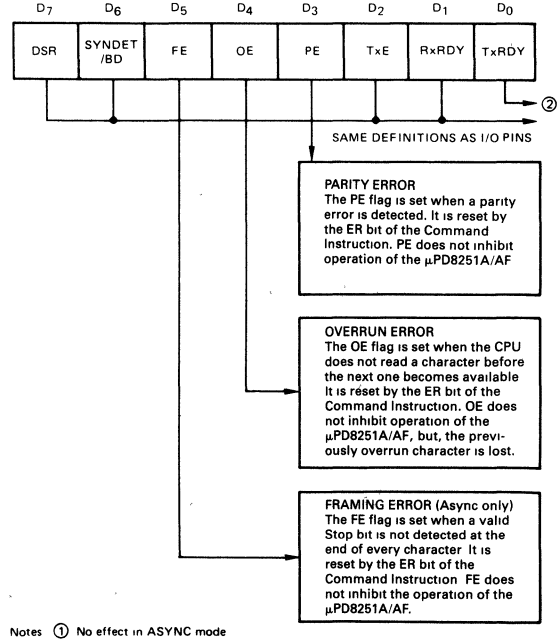
COMMAND INSTRUCTION FORMAT



STATUS READ FORMAT



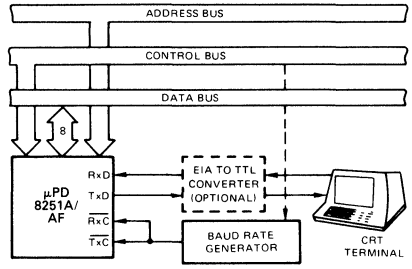
Notes ① No effect in ASYNC mode

② TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows

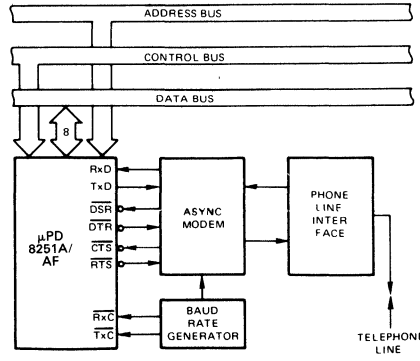
TxRDY status bit = DB Buffer Empty

TxRDY (pin 15) = DB Buffer Empty • $\overline{CTS}$ • TxEn

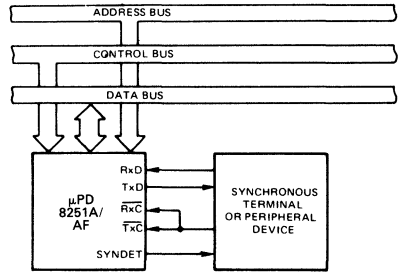
APPLICATION OF THE μPD8251A/AF



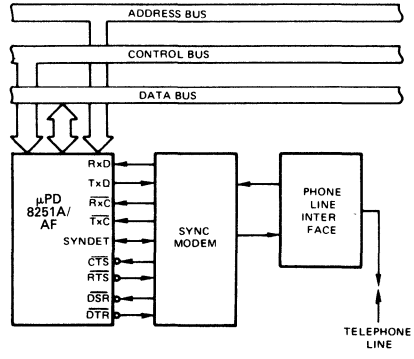
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
All Output Voltages . . . . . -0.5 to +7 Volts
All Input Voltages . . . . . -0.5 to +7 Volts
Supply Voltages . . . . . -0.5 to +7 Volts

T_a = 25°C

*COMMENT. Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10% for 8251A/AF; GND = 0V.

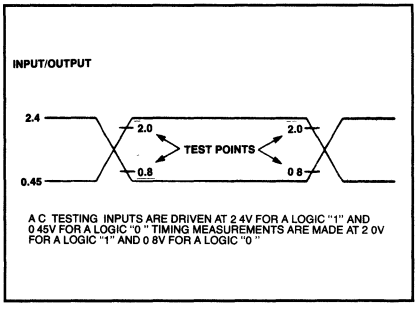
PARAMETER	SYMBOL	LIMITS μPD8251A/AF MIN	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	0 8	V	
Input High Voltage	V_{IH}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}		0.45	V	μPD8251 I_{OL} = 1.7 mA μPD8251A I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4		V	μPD8251. I_{OH} = -100 μA μPD8251A I_{OH} = -400 μA
Output Float Leakage	I_{OFL}		±10	μA	V_{OUT} = 0.45V
			10		.45V ≤ V_{OUT} ≤ V_{CC}
Input Load Current	I_{IL}		10	μA	.45V ≤ V_{IN} ≤ V_{CC}
Power Supply Current	I_{CC}		100	mA	All Outputs = Logic 1

CAPACITANCE

T_a = 25°C, V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

TESTING INPUT, OUTPUT WAVEFORM



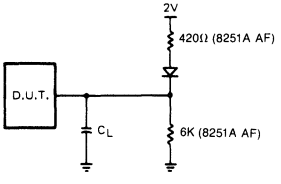
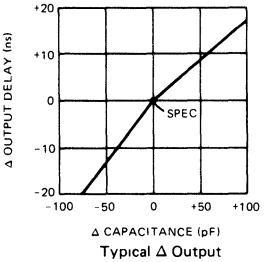


Figure 1.

TEST LOAD CIRCUIT



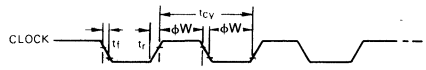
Typical Δ Output Delay Versus Δ Capacitance (pF)

AC CHARACTERISTICS

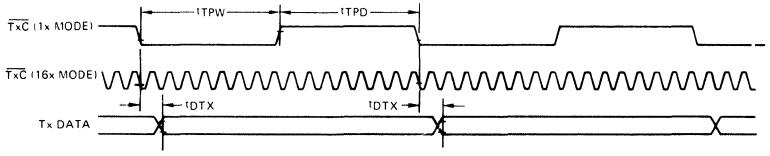
T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10% for 8251A/AF; GND = 0V.

PARAMETER	SYMBOL	LIMITS μPD8215A MIN	LIMITS μPD8215A MAX	LIMITS μPD8251AF MIN	LIMITS μPD8251AF MAX	UNIT	TEST CONDITIONS
READ							
Address Stable before READ (CS C D) ⑦	t_{AR}	50		0		ns	
Address Hold Time for READ (CS CD) ⑦	t_{RA}	50		0		ns	
READ Pulse Width	t_{RR}	250		200		ns	
Data Delay from READ ⑧	t_{RD}		250		140	ns	μPD8251A C_L 150pF
READ to Data Floating	t_{DF}	10	100	10	80	ns	
WRITE							
Address Stable before WRITE	t_{AW}	50		0		ns	
Address Hold Time for WRITE	t_{WA}	50		0		ns	
WRITE Pulse Width	t_{WW}	250		200		ns	
Data Set-Up Time for WRITE	t_{DW}	150		100		ns	
Data Hold Time for WRITE	t_{WD}	30		0		ns	
Recovery Time Between WRITES ②	t_{RV}	6		6		t_{CY}	
OTHER TIMING							
Clock Period ③	t_{CY}	0 32	1 35	20	1 35	μs	
Clock Pulse Width High	$t_{\phi W}$	140	t_{CY}-90	70	t_{CY}-40	ns	
Clock Pulse Width Low	$t_{\phi W}$	90		40		ns	
Clock Rise and Fall Time	t_R t_F	5	20	5	20	ns	
TxD Delay from Falling Edge of TxC	t_{DTx}		1		1	μs	
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2				μs	
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2				μs	
Transmitter Input Clock Frequency 1X Baud Rate	f_{Tx}		64	DC	64	kHz	
16X Baud Rate			310	DC	310	kHz	
64X Baud Rate			615	DC	615	kHz	
Transmitter Input Clock Pulse Width 1X Baud Rate	t_{TPW}	12		12		t_{CY}	
16X and 64X Baud Rate		1		1		t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate	t_{TPD}	15		15		t_{CY}	
16X and 64X Baud Rate		3		3		t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate	f_{Rx}		64	DC	64	kHz	
16X Baud Rate			310	DC	310	Khz	
64X Baud Rate			615	DC	615	kHz	
Receiver Input Clock Pulse Width 1X Baud Rate	t_{RPW}	12		12		t_{CY}	
16X and 64X Baud Rate		1		1		t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate	t_{RPD}	15		15		t_{CY}	
16X and 64X Baud Rate		3		3		t_{CY}	
TxRDY Delay from Center of Data Bit ⑫	t_{Tx}		8		8	t_{CY}	
TxRDY ↓ from Leading Edge of WR ⑨	t_{Tx} RDY CLEAR				300	ns	
RxRDY Delay from Center of Data Bit	t_{RX}		24		20	t_{CY}	
Internal SYNDET Delay from Center of Data Bit ⑬	t_{IS}		24			t_{CY}	
RxRDY ↓ from Leading Edge of RD ⑨	t_{Rx} RDY CLEAR				300	ns	
External SYNDET Set-Up Time before Falling Edge of RxC ⑨	t_{ES}	16		18		t_{CY}	
TxEMPTY Delay from Center of Data Bit ⑬	t_{TxE}		20		20	t_{CY}	
Control Delay from Rising Edge of WRITE (TxE, DTR RTS) ⑨	t_{WC}		8		8	t_{CY}	
Control to READ Set-Up Time (DSR, CTS) ⑨	t_{CR}	20		20		t_{CY}	

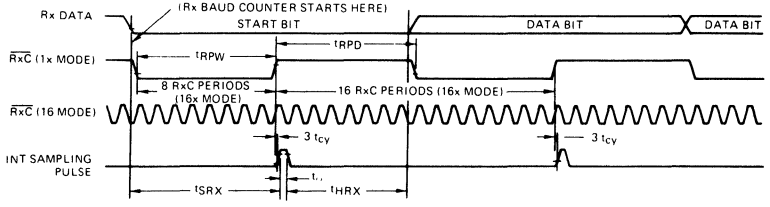
Notes
① AC timings measured at V_{OH} = 2 0 V_{CL} = 0 8 and with load circuit of Figure 1
② This recovery time is for initialization only when MODE SYNC1 SYNC2 COMMAND and first DATA BYTES are written into the USART Subsequent writing of both COMMAND and DATA are only allowed when TxRDY 1
③ The TxC and RxC frequencies have the following limitations with respect to CLK
For 1X Baud Rate f_{Tx} or f_{Rx} < 1 (30 t_{CY})
For 16X and 64X Baud Rate f_{Tx} or f_{Rx} 1 (4 5 t_{CY})
④ Reset Pulse Width = 6 t_{CY} minimum
⑤ $T_{TXRDYCCR}$-$2T_{CY}$ · T_{ϕ} · T_R · 200ns
⑥ $T_{RXRDYCLR}$-$2T_{CY}$ · T_{ϕ} · T_R · 170ns
⑦ Chip Select (CS) and Command Data (C D) are considered as Addresses
⑧ Assumes that address is valid before R_D ↓
⑨ Status update can have a maximum delay of 28 clock periods from the event affecting the status



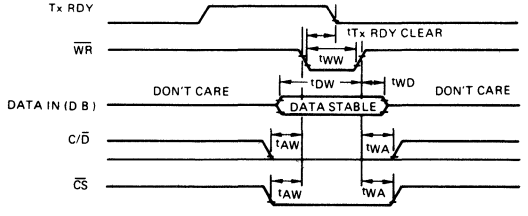
SYSTEM CLOCK INPUT



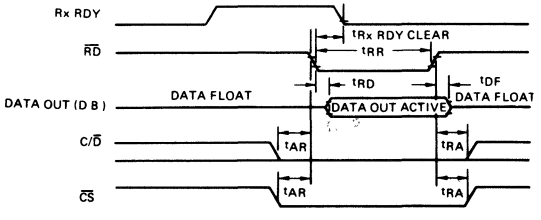
TRANSMITTER CLOCK AND DATA



RECEIVER CLOCK AND DATA

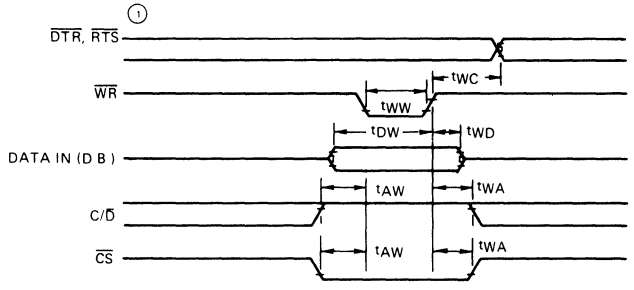


WRITE DATA CYCLE (PROCESSOR → USART)

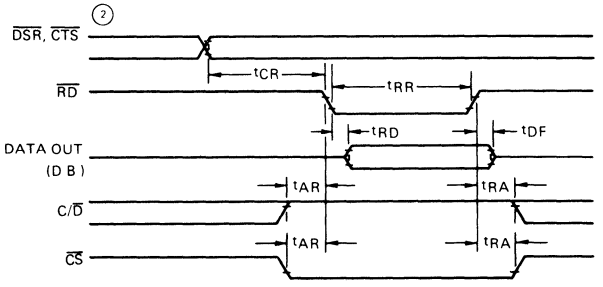


READ DATA CYCLE (PROCESSOR ← USART)

TIMING WAVEFORMS
(CONT.)



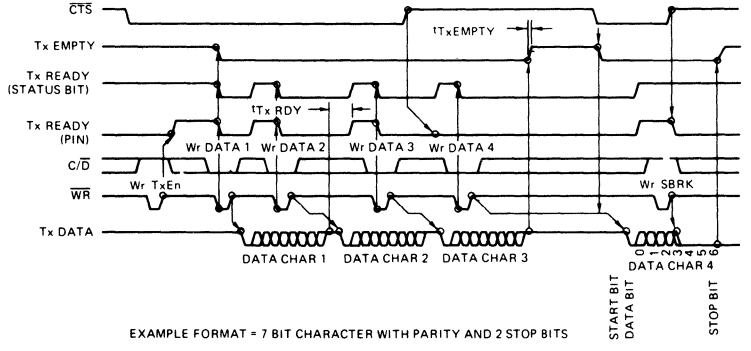
WRITE CONTROL OR OUTPUT PORT CYCLE
(PROCESSOR → USART)



READ CONTROL OR INPUT PORT CYCLE
(PROCESSOR ← USART)

NOTES ① T_{WC} includes the response timing of a control byte

② T_{CR} includes the effect of CTS on the TxENBL circuitry

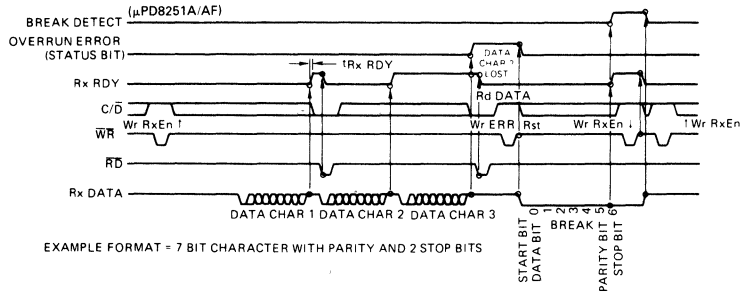


EXAMPLE FORMAT = 7 BIT CHARACTER WITH PARITY AND 2 STOP BITS

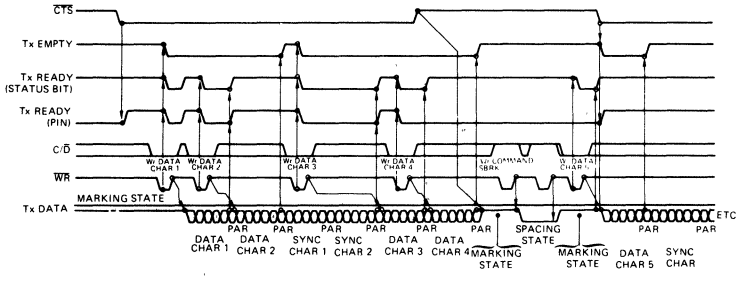
TRANSMITTER CONTROL AND FLAG TIMING
(ASYNC MODE)

6

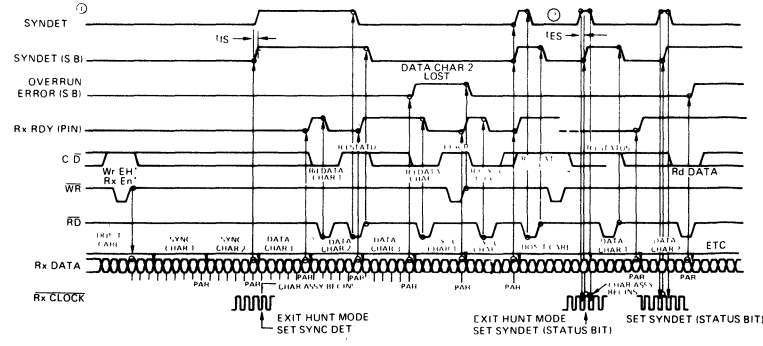
TIMING WAVEFORMS (CONT.)



RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)

Notes ① Internal sync, 2 sync characters, 5 bits, with parity
② External sync, 5 bits, with parity

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8251AC/AFC
Cerdip, μPD8251AD/AFD
Ceramic, μPD8251AD/AFD

PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The NEC μPD8253 contains three independent, programmable, multi-modal 16-bit counter/timers. It is designed as a general purpose device, fully compatible with the 8080 family. The μPD8253 interfaces directly to the busses of the processor as an array of I/O ports.

The μPD8253 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be clocked at rates from DC to 4 MHz. The system software controls the loading and starting of the counters to provide accurate multiple time delays. The counter output flags the processor at the completion of the time-out cycles.

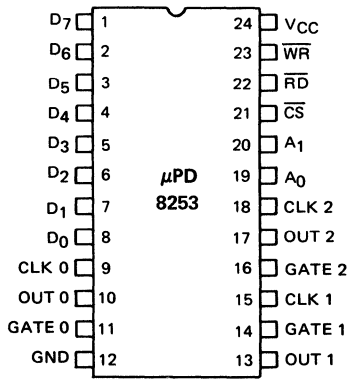
System overhead is greatly improved by relieving the software from the maintenance of timing loops. Some other common uses for the μPD8253 in microprocessor based systems are:

- Programmable Baud Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

FEATURES

- Three Independent 16-Bit Counters
- Clock Rate: DC to 4 MHz
- Count Binary or BCD
- Single +5 Volt Supply, ±10%
- 24 Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8-Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0, A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

Data Bus Buffer

The 3-state, 8-bit, bi-directional Data Bus Buffer interfaces the μPD8253 to the 8080AF/8085A microprocessor system. It will transmit or receive data in accordance with the INput or OUTput instructions executed by the processor. There are three basic functions of the Data Bus Buffer.

1. Program the modes of the μPD8253.
2. Load the count registers.
3. Read the count values.

Read/Write Logic

The Read/Write Logic controls the overall operation of the μPD8253 and is governed by inputs received from the processor system bus.

Control Word Register

Two bits from the address bus of the processor, A_0 and A_1, select the Control Word Register when both are at a logic "1" (active-high logic). When selected, the Control Word Register stores data from the Data Bus Buffer in a register. This data is then used to control:

1. The operational MODE of the counters.
2. The selection of BCD or Binary counting.
3. The loading of the count registers.

$\overline{RD}$ (Read)

This active-low signal instructs the μPD8253 to transmit the selected counter value to the processor.

$\overline{WR}$ (Write)

This active-low signal instructs the μPD8253 to receive MODE information or counter input data from the processor.

A_1, A_0

The A_1 and A_0 inputs are normally connected to the address bus of the processor. They control the one-of-three counter selection and address the control word register to select one of the six operational MODES.

$\overline{CS}$ (Chip Select)

The μPD8253 is enabled when an active-low signal is applied to this input. Reading or writing from this device is inhibited when the chip is disabled. The counter operation, however, is not affected.

Counters #0, #1, #2

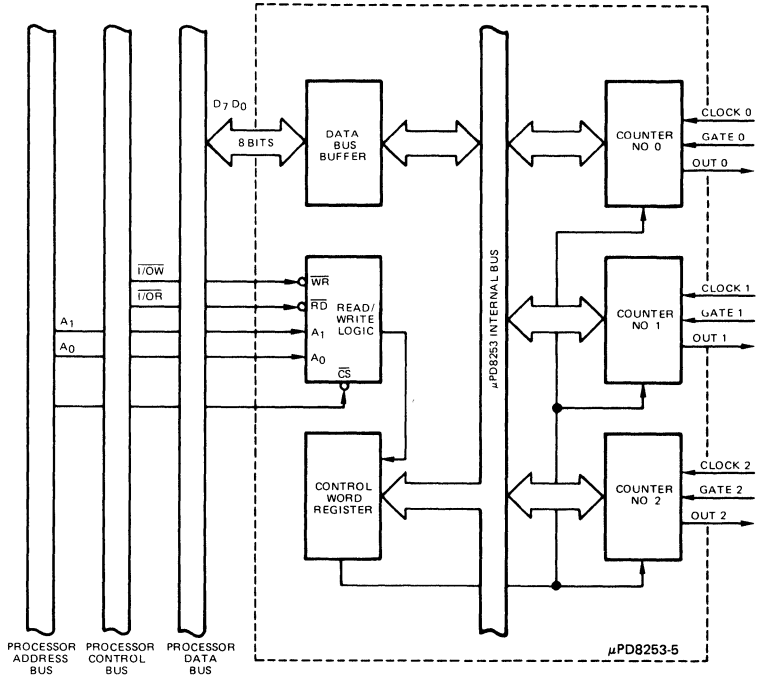
The three identical, 16-bit down counters are functionally independent allowing for separate MODE configuration and counting operation. They function as Binary or BCD counters with their gate, input and output line configuration determined by the operational MODE data stored in the Control Word Register. The system software overhead time can be reduced by allowing the control word to govern the loading of the count data.

The programmer, with READ operations, has access to each counter's contents. The μPD8253 contains the commands and logic to read each counter's contents while still counting without disturbing its operation.

The following is a table showing how the counters are manipulated by the input signals to the Read/Write Logic.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	FUNCTION
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation, 3-State
1	X	X	X	X	Disable, 3-State
0	1	1	X	X	No-Operation, 3-State

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts (1)

Note (1) With respect to ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}①	2.0		V_{CC}+0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{IL}			±10	μA	$0 \leq V_{IN} \leq V_{CC}$
Output Float Leakage Current	I_{OFL}			±10	μA	$0.45 \leq V_{OUT} \leq V_{CC}$
V_{CC} Supply Current	I_{CC}			140	mA	

Note: ① V_{IH} 2.2 min for 8253-2.

CAPACITANCE

$T_a = 25°C$, $V_{CC} = GND = 0V$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Input/Output Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}.

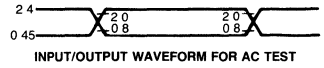
T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; GND = 0V

AC CHARACTERISTICS ①

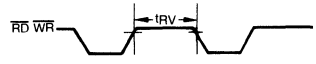
PARAMETER	SYMBOL	LIMITS μPD8253-2		LIMITS μPD8253-5		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
READ							
Address Stable Before $\overline{READ}$	t_{AR}	0		0		ns	
Address Hold Time for $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	200		250		ns	
Data Delay from $\overline{READ}$	t_{RD}		140		170	ns	CL = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	10	100	25	100	ns	CL = 150 pF
Recovery Time Between $\overline{READ}$	t_{RV}	200		1000		ns	
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	0		0		ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20		0		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	200		250		ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	150		150		ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	20		0		ns	
Recovery Time Between $\overline{WRITES}$	t_{RV}	200		1000		ns	
CLOCK AND GATE TIMING							
Clock Period	t_{CLK}	200		250	DC	ns	
High Pulse Width	t_{PWH}	100		160		ns	
Low Pulse Width	t_{PWL}	100		90		ns	
Gate Pulse Width High	t_{GW}	150		150		ns	
Gate Set Up Time to Clock ↑	t_{GS}	100		100		ns	
Gate Hold Time After Clock ↑	t_{GH}	100		50		ns	
Low Gate Width	t_{GL}	50		100		ns	
Output Delay from Clock ↓	t_{OD}		300		300	ns	CL = 150 pF
Output Delay from Gate	t_{ODG}		300		300	ns	CL = 150 pF

Note: ① AC Timing Measured at V_{OH} = 2.0V, V_{OL} = 0.8V

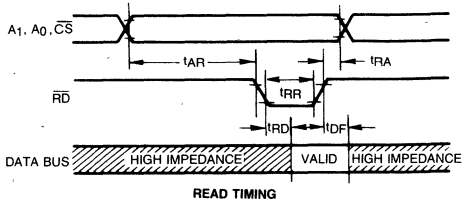
TIMING WAVEFORMS



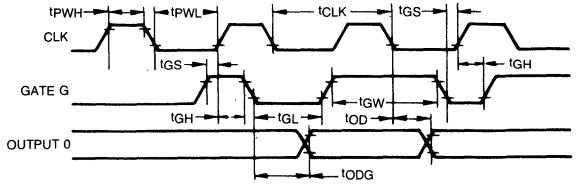
INPUT/OUTPUT WAVEFORM FOR AC TEST



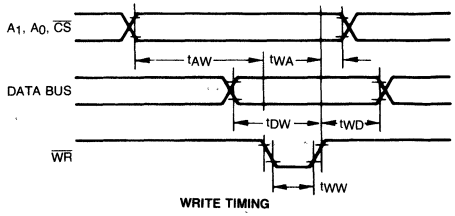
READ AND WRITE TIMING



READ TIMING



CLOCK AND GATE TIMING



WRITE TIMING

PROGRAMMING THE μPD8253

The programmer can select any of the six operational MODES for the counters using system software. Individual counter programming is accomplished by loading the CONTROL WORD REGISTER with the appropriate control word data (A_0, A_1 = 11).

CONTROL WORD FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC – Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Invalid

RL – Read/Load

RL1	RL0	
0	0	Counter Latching Operation
1	0	Read/Load Most Significant Byte Only
0	1	Read/Load Least Significant Byte Only
1	1	Read/Load Least Significant Byte First, Then Most Significant Byte

BCD

0	Binary Counter, 16-Bits
1	BCD Counter, 4-Decades

M-Mode

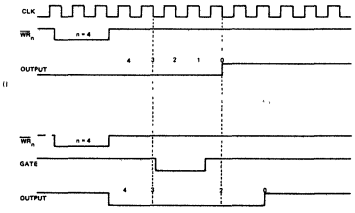
M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

OPERATIONAL MODES ①

Each of the three counters can be individually programmed with different operating MODES by appropriately formatted Control Words. The following is a summary of the MODE operations.

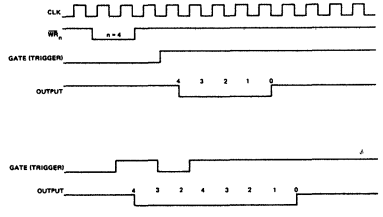
Mode 0: Interrupt on Terminal Count

The initial MODE set operation forces the OUTPUT low. When the specified counter is loaded with the count value, it will begin counting. The OUTPUT will remain low until the terminal count sets it high. It will remain in the high state until the trailing edge of the second $\overline{WR}$ pulse loads in COUNT data. If data is loaded during the counting process, the first $\overline{WR}$ stops the count. Counting starts with the new count data triggered by the falling clock edge after the second $\overline{WR}$. If a GATE pulse is asserted while counting, the count is terminated for the duration of GATE. The falling edge of CLK following the removal of GATE restarts counting from the terminated point.



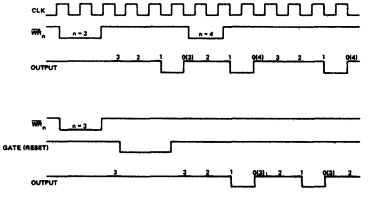
Mode 1: Programmable One-Shot

The OUTPUT is set low by the falling edge of CLOCK following the trailing edge of GATE. The OUTPUT is set high again at the terminal count. The output pulse is not affected if new count data is loaded while the OUTPUT is low. The new data will be loaded on the rising edge of the next trigger pulse. The assertion of a trigger pulse while OUTPUT is low, resets and retriggers the One-Shot. The OUTPUT will remain low for the full count value after the rising edge of TRIGGER.



Mode 2: Rate Generator

The RATE GENERATOR is a variable modulus counter. The OUTPUT goes low for one full CLOCK period as shown in following timing diagram. The count data sets the time between OUTPUT pulses. If the count register is reloaded between output pulses the present period will not be affected. The subsequent period will reflect the new value. The OUTPUT will remain high for the duration of the asserted GATE input. Normal operation resumes on the falling CLOCK edge following the rising edge of GATE.



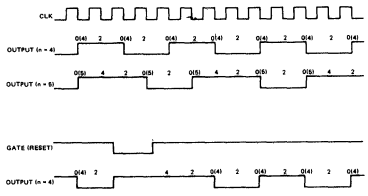
Note: ① All internal counter events occur at the falling edge of the associated clock in all modes of operation.

OPERATIONAL MODES (Cont.)

Mode 3: Square Wave Generator

MODE 3 resembles MODE 2 except the OUTPUT will be high for half of the count and low for the other half (for even values of data). For odd values of count data the OUTPUT will be high one clock cycle longer than when it is low (High Period → $\frac{N+1}{2}$ clock cycles; Low Period → $\frac{N-1}{2}$ clock periods, where N is the decimal value of count data). If the count register is reloaded with a new value during counting, the new value will be reflected immediately after the output transition of the current count.

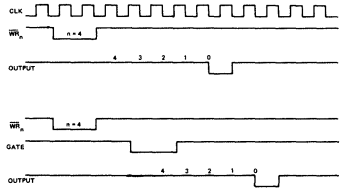
The OUTPUT will be held in the high state while GATE is asserted. Counting will start from the full count data after the GATE has been removed.



Mode 4: Software Triggered Strobe

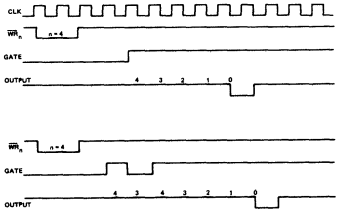
The OUTPUT goes high when MODE 4 is set, and counting begins after the second byte of data has been loaded. When the terminal count is reached, the OUTPUT will pulse low for one clock period. Changes in count data are reflected in the OUTPUT as soon as the new data has been loaded into the count registers. During the loading of new data, the OUTPUT is held high and counting is inhibited.

The OUTPUT is held high for the duration of GATE. The counters are reset and counting begins from the full data value after GATE is removed.



Mode 5: Hardware Triggered Strobe

Loading MODE 5 sets OUTPUT high. Counting begins when count data is loaded and GATE goes high. After terminal count is reached, the OUTPUT will pulse low for one clock period. Subsequent trigger pulses will restart the counting sequence with the OUTPUT pulsing low on terminal count following the last rising edge of the trigger input (Reference bottom half of timing diagram).



Package Outlines

For information, see Section 7.

Plastic, μPD8253C-5
Ceramic, μPD8253D-5
Cerdip, μPD8253D-5

PROGRAMMABLE PERIPHERAL INTERFACES

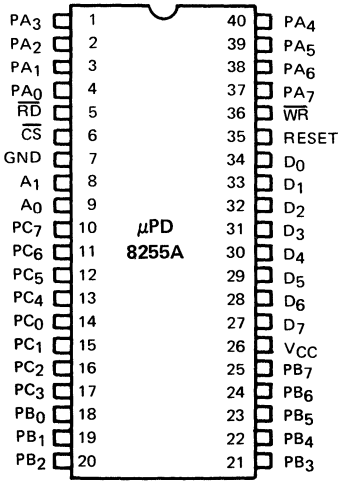
DESCRIPTION

The μPD8255A is a general purpose programmable INPUT/OUTPUT device designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or ıtput. Three of the remaining four pins in each group are used for handshakıng strobes and ınterrupt control signals. The Bi-directional Bus mode, (MODE 2), uses the 8 lines of Port A for a bi-directional bus, and five lines from Port C for bus control signals. The μPD8255A is packaged in 40-pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays
- LSI Drastically Reduces System Package Count
- Standard 40-Pin Dual-In-Line Plastic.

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

6

General

The μPD8255A Programmable Peripheral Interface (PPI) is designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255A. The μPD8255A is functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, 8-bit Data Bus Buffer (D_0-D_7) of the μPD8255A can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255A for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255A to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9

Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255A. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)
Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

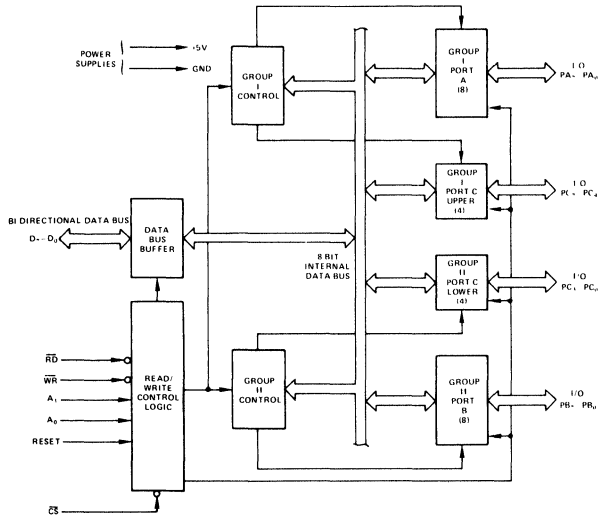
Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255A can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255A are further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin With Respect to V_{SS} . . . . . -0.5 to +7 Volts

Note: ① With respect to V_{SS}

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS μPD8255A MIN	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	0.8	V	
Input High Voltage	V_{IH}	2	V_{CC}	V	
Output Low Voltage	V_{OL}		0.45	V	②
Output High Voltage	V_{OH}	2.4		V	③
Darlington Drive Current	I_{OH} ①	-1	-4	mA	$V_{EXT} = 1.5V$, $R_{EXT} = 750\Omega$
Power Supply Current	I_{CC}		120	mA	$V_{CC} = +5V$, Output Open
Input Leakage Current	I_{LIH}		10	μA	$V_{IN} = V_{CC}$
Input Leakage Current	I_{LIL}		-10	μA	$V_{IN} = 0.4V$
Output Leakage Current	I_{LOH}		±10	μA	$V_{OUT} = V_{CC}$, $\overline{CS} = 2.0V$
Output Leakage Current	I_{LOL}		-10	μA	$V_{OUT} = 0.4V$, $\overline{CS} = 2.0V$

Notes ① Any set of eight (8) outputs from either Port A, B, or C can source 4 mA into 1.5V.

② I_{OL} = 2.5 mA for DB Port, 1.7 mA for Peripheral Ports

③ I_{OH} = -400 μA for dB Port, -200 μA for Peripheral Ports

CAPACITANCE

$T_a = 25°C$, $V_{CC} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	$f_c = 1$ MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

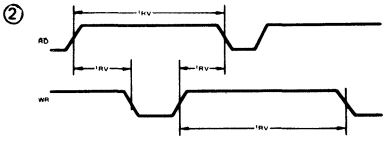
T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{SS} = 0V

AC CHARACTERISTICS

PARAMETER	SYMBOL	8255A-2 LIMITS MIN	8255A-2 LIMITS MAX	8255A-5 LIMITS MIN	8255A-5 LIMITS MAX	UNIT	TEST CONDITIONS
Address Stable Before $\overline{READ}$	t_{AR}	0		0		ns	
Address Stable After $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	200		250		ns	
Data Valid From $\overline{READ}$	t_{RD}		140		170	ns	C_L = 150 pF
Data Float After $\overline{READ}$	t_{DF}		100		100	ns	C_L = 100 pF
		10		10		ns	C_L = 15 pF
Time Between $\overline{READS}$ and/$\overline{WRITES}$	t_{RV}	200		850		ns	②
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	0		0		ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20		20		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	200		250		ns	
Data Valid to $\overline{WRITE}$ (T.E.)	t_{DW}	100		100		ns	
Data Valid After $\overline{WRITE}$	t_{WD}	0		0		ns	
OTHER TIMING							
$\overline{WR}$ = 0 To Output	t_{WB}		350		350	ns	C_L = 150 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0		0		ns	
Peripheral Data After $\overline{RD}$	t_{HR}	0		0		ns	
$\overline{ACK}$ Pulse Width	t_{AK}	300		300		ns	
$\overline{STB}$ Pulse Width	t_{ST}	350		350		ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	0		0		ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150		150		ns	
$\overline{ACK}$ = 0 To Output	t_{AD}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}		250		250	ns	C_L = 50 pF
		20		20			C_L = 15 pF
$\overline{WR}$ = 1 To OBF = 0	t_{WOB}		300		650	ns	
$\overline{ACK}$ = 0 To OBF = 1	t_{AOB}		350		350	ns	
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}		300		300	ns	
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}		300		300	ns	
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}		400		400	ns	
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}		300		300	ns	C_L = 150 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}		350		350	ns	
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}		450		850	ns	C_L = 150 pF ③

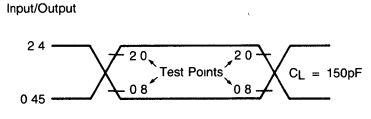
Note: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

②



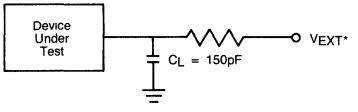
③ INTR↑ may occur as early as $\overline{WR}$↓.

AC Testing Input, Output Waveform



AC Testing inputs are driven at 2 4V for a logic 1 and 0 45V for a logic 0 Timing measurements are made at 2 0V for a logic 1 and 0 8V for a logic 0

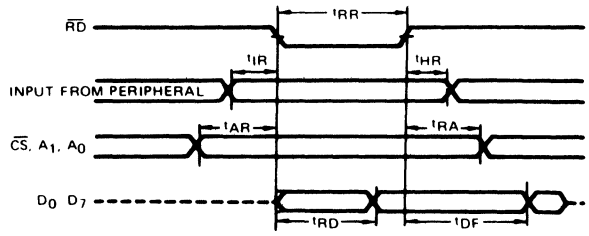
AC Testing Load Circuit



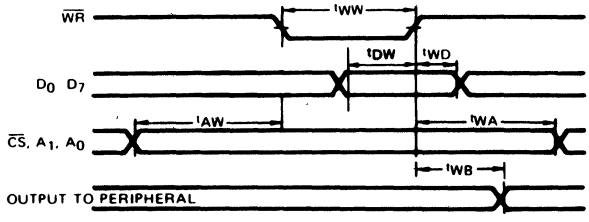
*V_{EXT} is set at various voltages during testing to guarantee the specification

TIMING WAVEFORMS

MODE 0

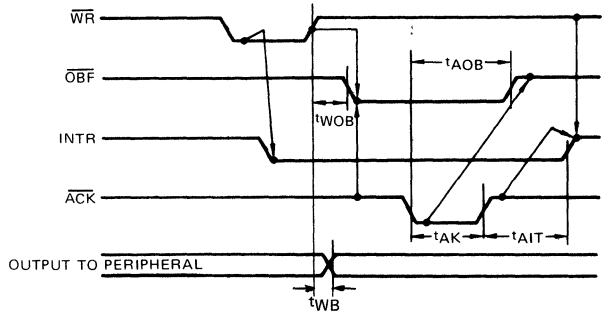


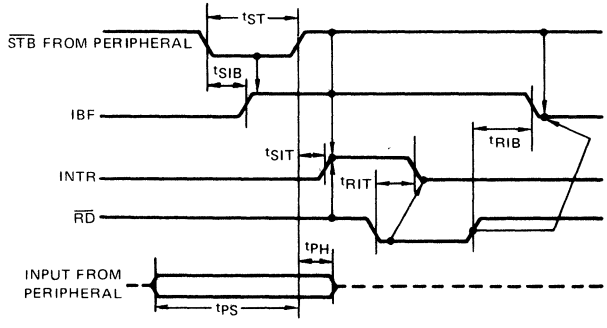
BASIC INPUT (READ)



BASIC OUTPUT (WRITE)

MODE 1





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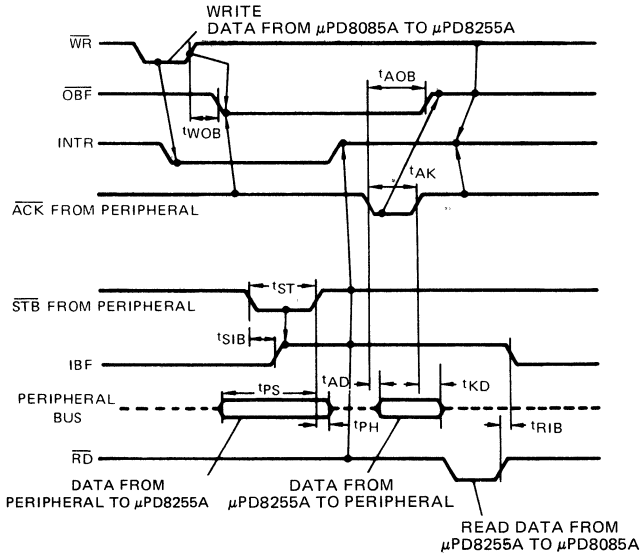
TIMING WAVEFORMS (CONT.)

MODE 2



Note ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

② When the μPD8255A is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

MODES

The μPD8255A can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed
  - 16 different configurations in MODE 0
  - Two 8-bit ports and two 4-bit ports
  - Inputs are not latched
  - Outputs are latched

MODE 1

- MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C
  - Two I/O Groups (I and II)
  - Both groups contain an 8-bit data port and a 4-bit control/data port
  - Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

- MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2
  - An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})
  - Both inputs and outputs are latched
  - An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

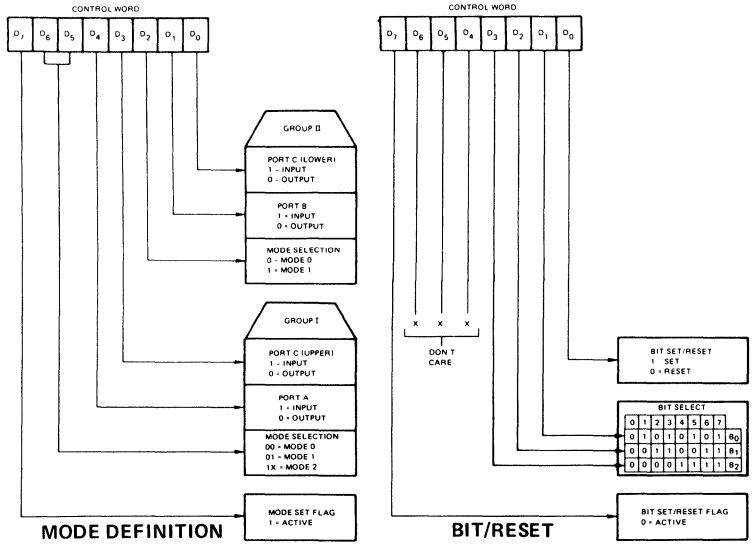
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

NOTES ① X means "DO NOT CARE"
② All conditions not listed are illegal and should be avoided

FORMATS



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8255AC-5
Ceramic, μPD8255AD-5

Notes

PROGRAMMABLE DMA CONTROLLER

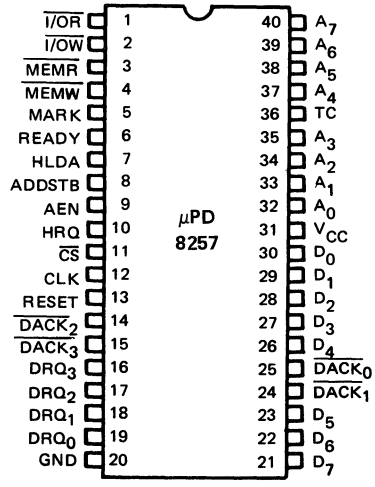
DESCRIPTION

The μPD8257 is a programmable four-channel Direct Memory Access (DMA) controller. It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the μPD8257 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the μPD8257 so that the system bus may be acquired by the generation of a single HOLD command to the 8080A. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other μPD8257 devices for systems requiring more than four DMA channels.

FEATURES

- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply ±10%
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION

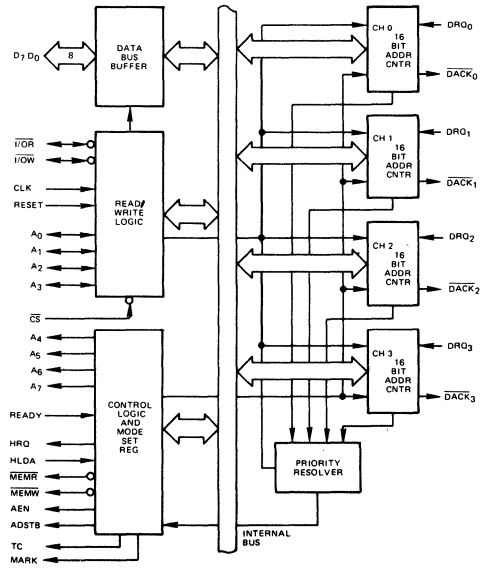


PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{CS}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

6

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①
Power Dissipation . . . . . 1 Watt

Note: ① With Respect to Ground

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$ GND = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	0.8	Volts	
Input High Voltage	V_{IH}	2 0	V_{CC} + 0.5	Volts	
Output Low Voltage	V_{OL}		0.45	Volts	I_{OL} = 1 6 mA
Output High Voltage	V_{OH}	2.4	V_{CC}	Volts	I_{OH} = -150 μA for AB, DB and AEN I_{OH} = -80 μA for others
HRQ Output High Voltage	V_{HH}	3 3	V_{CC}	Volts	I_{OH} = -80 μA
Power Supply Current	I_{CC}		100	mA	8257-2
			120	mA	8257-5
Input Leakage	I_{IL}	-10	10	μA	$0 \le V_{IN} \le V_{CC}$
Output Leakage During Float	I_{OFL}	-10	10	μA	$0\,45 \le V_{OUT} \le V_{CC}$

CAPACITANCE

$T_a = 25°C$; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE 8080 BUS PARAMETERS

BUS PARAMETERS

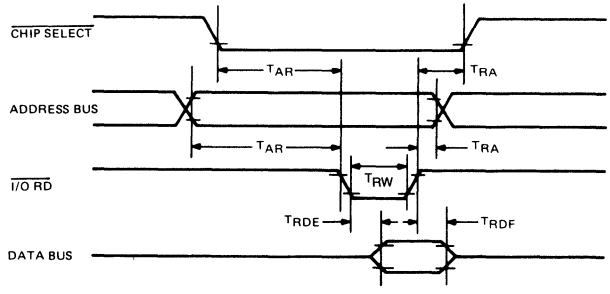
T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, GND = 0V ①

PARAMETER	SYMBOL	LIMITS μPD8257-2		LIMITS μPD8257-5		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
READ							
Adr or $\overline{CS}$↓ Setup to $\overline{Rd}$↓	T_{AR}	20		0		ns	
Adr or $\overline{CS}$→ Hold from $\overline{Rd}$↑	T_{RA}	20		0		ns	
Data Access from $\overline{Rd}$↓	T_{RDE}	0	140	0	170	ns	C_L = 100 pF
DB→ Float Delay from $\overline{Rd}$↑	T_{RDF}		100		100	ns	C_L = 100 pF
		10		20		ns	C_L = 15 pF
$\overline{Rd}$ Width	T_{RW}	200		250		ns	
WRITE							
Adr Setup to $\overline{Wr}$↓	T_{AW}	20		20		ns	
Adr Hold from $\overline{Wr}$↑	T_{WA}	20		0		ns	
Data Setup to $\overline{Wr}$↓	T_{DW}	100		200		ns	
Data Hold from $\overline{Wr}$↑	T_{WD}	20		0		ns	
$\overline{Wr}$ Width	T_{WWS}	100		200		ns	
OTHER TIMING							
Reset Pulse Width	T_{RSTW}	300		300		ns	
Power Supply ↑(V_{CC}) Setup to Reset↓	TRSTD	500		500		μs	
Signal Rise & Fall Times	T_r, T_f		20		20		
Reset to First $\overline{IOWR}$	T_{RSTS}	2		2		t_{CY}	

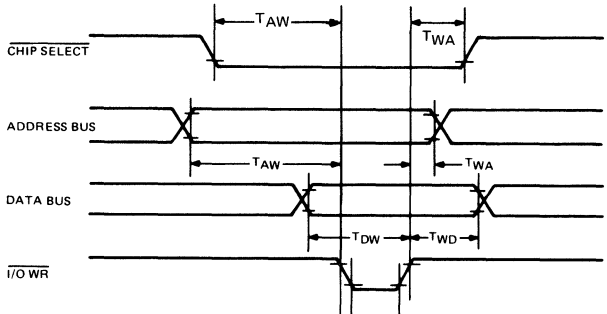
Note ① All timing measurements are made at the following reference voltages unless specified otherwise Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

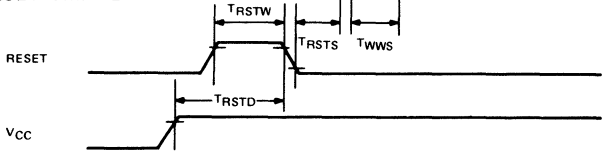
READ TIMING



WRITE TIMING



RESET TIMING



T_a = 0°C to 70°C, V_{CC} = +5V ± 10%, GND = 0V

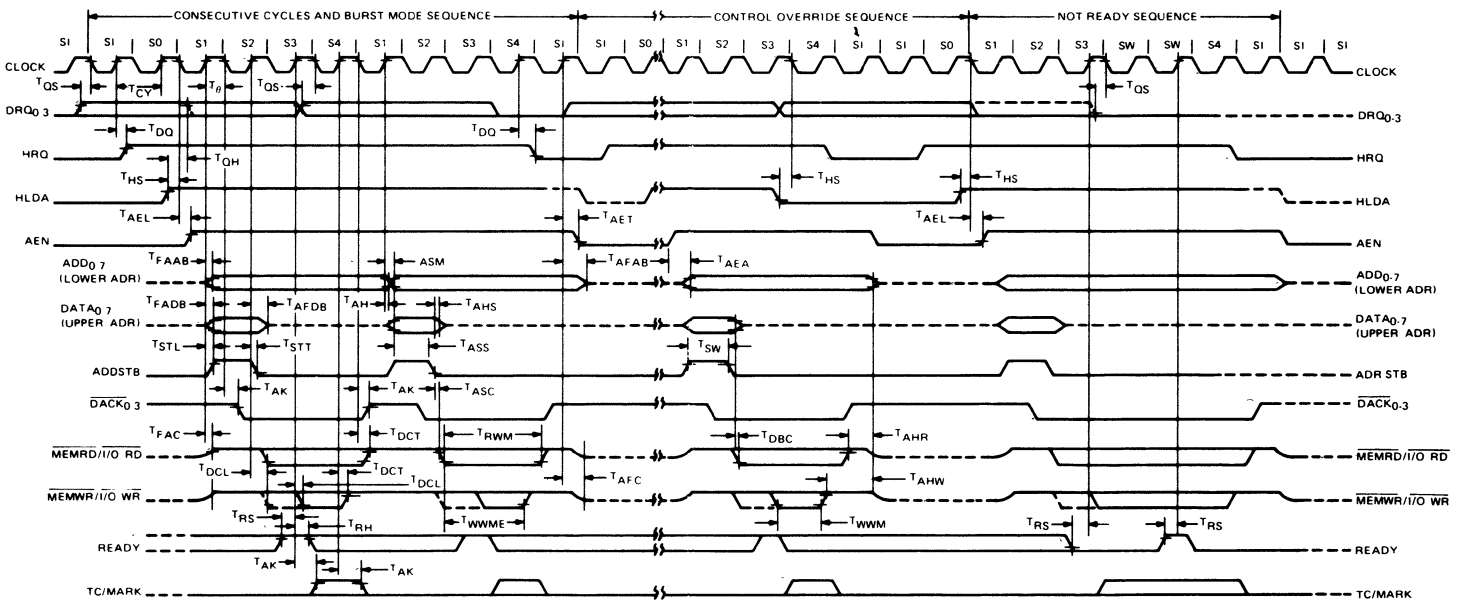
AC CHARACTERISTICS DMA (MASTER) MODE

Timing Requirements

PARAMETER	SYMBOL	LIMITS μPD8257-2		LIMITS μPD8257-5		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Cycle Time (Period)	T_{CY}	0 200	4	0 320	4	μs	
Clock Active (High)	$T\theta$	80		80	$8T_{CY}$	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	50		120			
DRQ↓ Hold from HLDA↑	T_{QH}	0		0			④
HRQ↑ or ↓ Delay from θ↑ (SI, S4) (measured at 2 0V)	T_{DQ}		160		160	ns	
HRQ↑ or ↓ Delay from θ↑ (SI, S4) (measured at 3 3V)	T_{DQ1}		200		250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	50		100		ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}		150		300	ns	
AEN↓ Delay from θ↑ (SI)	T_{AET}		150		200	ns	
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20		20		ns	④
Adr (AB) (Active Delay from θ↑ (S1)	T_{FAAB}		200		250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}		150		150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}		200		250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	$T_{ASM}-50$		$T_{ASM}-50$			②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S2, SI)	T_{AHR}	60		60		ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	100		300		ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}		150		300	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	T_{STT}	140	$T_{STT}+20$	170	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100		100		ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	20		50		ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}		150		200	ns	
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}		140		140	ns	
Adr Stb Width (S1-S2)	T_{SW}	$T_{CY}-100$		$T_{CY}-100$		ns	④
$\overline{RD}$↑ or $\overline{Wr}$ (Ext)↑ Delay from Adr Stb↓ (S2)	T_{ASC}	20		70		ns	④
RD↓ or Wr (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	0		20		ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark ↑ Delay from θ↑ (S3) and TC/Mark ↓ Delay from θ↑ (S4)	T_{AK}		200		250	ns	⑤
$\overline{Rd}$↑ or $\overline{Wr}$ (Ext) ↓ Delay from θ↑ (S2) and $\overline{Wr}$↑ Delay from θ↑ (S3)	T_{DCL}		150		200	ns	②⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}		150		200	ns	②⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}		200		300	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}		150		150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	$2T_{CY}+T_\theta-50$		$2T_{CY}+T_\theta-50$		ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	$T_{CY}-50$		$T_{CY}-50$		ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	$2T_{CY}-50$		$2T_{CY}-50$		ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30		30		ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	30		30		ns	

Notes: 1 Load = 1 TTL
2 Load = 50 pF
3 Load = V_{OH} = 3 3V
4 Tracking Specification
5 ΔT_{AK} <50 ns
6 ΔT_{DCL} <50 ns
7 ΔT_{DCT} <50 ns

TIMING WAVEFORMS
DMA (MASTER) MODE



FUNCTIONAL DESCRIPTION

The μPD8257 is a programmable, Direct Memory Address (DMA) device. When used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080A/808085A based systems. Once initialized by an 8080A/8085A CPU, the μPD8257 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occurs within the μPD8257.

- It acquires control of the system bus (placing 8080A/8085A in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16-bit memory address word is generated with the aid of an 8212 in the following manner:

  The μPD8257 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.
  The μPD8257 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The μPD8257 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read, which causes data to be transferred from memory to a peripheral;
- DMA write, which causes data to be transferred from a peripheral to memory; and
- DMA verify, which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the μPD8257. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cyclic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

DMA OPERATION

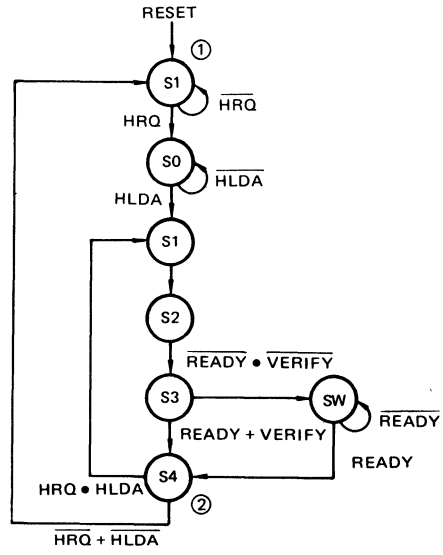
Internally the μPD8257 contains six different states (S0, S1, S2, S3, S4 and SW). The duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the μPD8257 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080A/8085A and the μPD8257 waits in S0 until the 8080A/8085A issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK}_n$) with the highest priority is driven low, selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK}_n$) or both $\overline{DACK}_n$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst model).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the μPD8257 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the μPD8257 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the μPD8257 should lose control of the system bus (i.e., HLDA goes low)then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the μPD8257 and the 8080A/8085A.

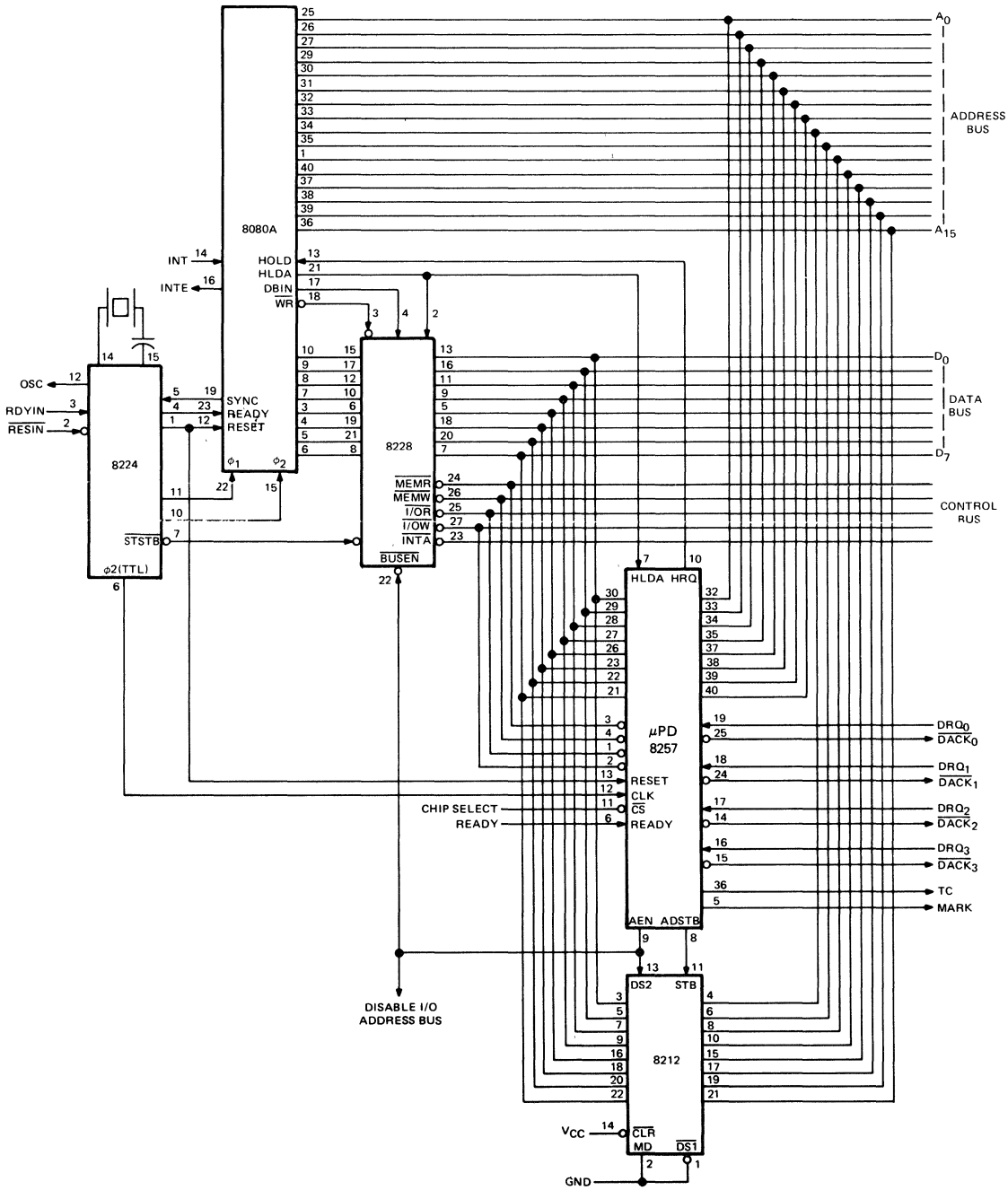
During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

DMA OPERATION STATE DIAGRAM



Notes ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

TYPICAL μPD8257
SYSTEM INTERFACE SCHEMATIC



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8257C-5
Ceramic, μPD8257D-5

Notes

PROGRAMMABLE INTERRUPT CONTROLLER

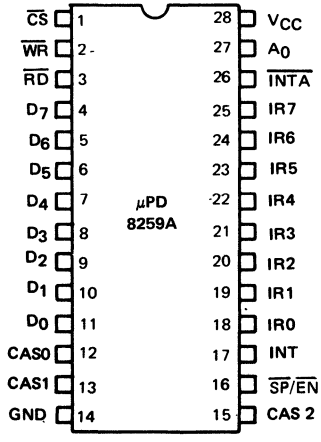
DESCRIPTION

The NEC μPD8259A is a programmable interrupt controller directly compatible with the 8080A/8085A/8086/8088 microprocessors. It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to 64 levels with the addition of other μPD8259As. The user is offered a selection of priority algorithms to tailor the priority processing to meet his system requirements. These can be dynamically modified during operation, expanding the versatility of the system.
The μPD8259A is completely upward compatible with the μPD8259-5, so software written for the μPD8259-5 will run on the μPD8259A and μPD8259A-2.

FEATURES

- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Full Compatibility with 8080A/8085A/8086/8088

PIN CONFIGURATION



PIN NAMES

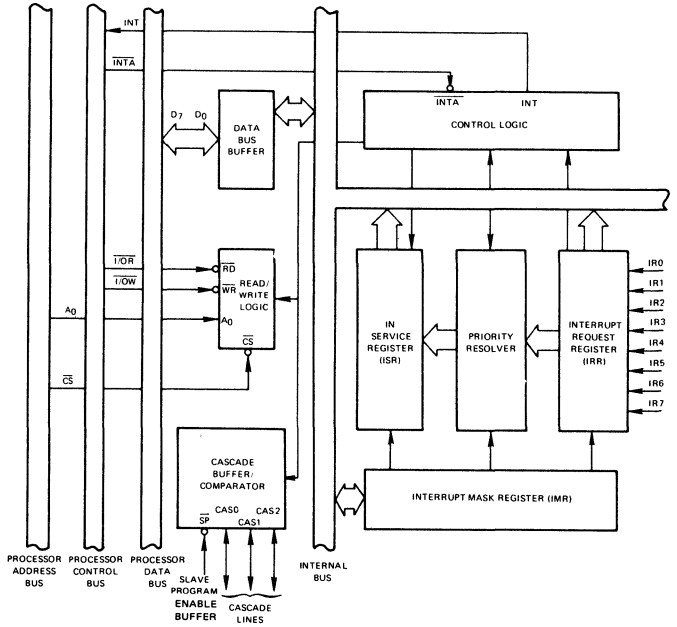
$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program Input/ Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – IR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select

6

PIN IDENTIFICATION

Pin No.	Pin Symbol	I/O	Function
1	$\overline{CS}$	I	**Chip Select.** When CS is low, the CPU can read from the write to the 8259A INTA operates independently of CS
2	$\overline{WR}$	O	**Write.** The 8259A can receive command words from the CPU when both WR and CS are low
3	$\overline{RD}$	I	**Read.** When both RD and CS are low, the 8259A sends status onto the dta bus for the CPU to read
4–11	D_7–D_0	I/O	**Bidirectional data bus.** This bus carries control, status, and interrupt-vector data
12, 13, 15	CAS_0–CAS_2	I/O	**Cascade lines.** These lines are used as a bus which controls multiple 8259A in a master/slave configuration When an 8259A is a master, these lines are outputs When an 8259A is used as a slave, the lines are inputs
14	GND	I	**Ground.**
16	$\overline{SP}/\overline{EN}$	I/O	This is a dual-function pin **Slave Program.** When SP = 1, the 8259A operates as a master When SP = 0, the 8259A operates as a slave **Enable Buffer.** This is an output to enable buffer transceivers
17	INT	O	**Interrupt.** When the 8259A receives a valid interrupt request, INT goes high to interrupt the CPU This pin should be connected directly to the interrupt pin on the CPU
18–25	IR_0–IR_7	I	**Interrupt Requests.** These are asynchronous inputs that operate in two modes In Edge Triggered mode, the input must be raised from low to high and held high until acknowledged The Level Triggered mode requires only a high
26	$\overline{INTA}$	I	**Interrupt Acknowledge.** When the CPU sends a series of pulses to this input, the 8259A releases interrupt-vector data onto the data bus
27	A_0	I	**A_0 Address Line.** The 8259A uses this input, with $\overline{CS}$ and $\overline{WR}$, to decode command words written by the CPU A_0 is used with $\overline{CS}$ and $\overline{RD}$ to decode status for the CPU to read A_0 is normally connected to the A_0 address line on the CPU (A_1 for an iAPX 86, 88)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1W

Note: ① With respect to ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259 is set high. The IR input line must remain high until the first $\overline{\text{INTA}}$ input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080A/8085A/8086/8088.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

$\overline{INTA}$ pulses cause the μPD8259A to put vectoring information on the bus. The number of pulses depends upon whether the μPD8259A is in μPD8085A mode or 8086/8088 mode.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{WR}$ and $\overline{RD}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs.

μPD8259A BASIC OPERATION						
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259A aligns these commands in the proper order.

CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259 Array.)

The IDs of all μPD8259As are buffered and compared in the cascade buffer/comparator. The master μPD8259A sends the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{INTA}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

SLAVE PROGRAM ($\overline{SP}$). (For Use in Multiple μPD8259A Array.)

The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259As in a master-plus-slaves array. The master controls the slaves through the CAS0, 1, 2 lines. The $\overline{SP}$ input to the device selects the CAS0-2 lines as either outputs ($\overline{SP}$=1) for the master or as inputs ($\overline{SP}$=0) for the slaves. For one device only the $\overline{SP}$ must be set to a logic "1" since it is functioning as a master..

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5	0 8	V	
Input High Voltage	V_{IH}	2 0	V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}		0 45	V	I_{OL} = 2 2 mA
Output High Voltage	V_{OH}	2 4		V	I_{OH} = −400 μA
Interrupt Output-High Voltage	V_{OH-INT}	2.4 3.5		V V	I_{OH} = −400 μA I_{OH} = −100 μA
Input Leakage Current for other inputs	I_{LI}	−10	10	μA	$0 \le V_{IN} \le V_{CC}$
Output Leakage Current	I_{LOL}	−10	+10	μA	$0.45 \le V_{OUT} \le V_{CC}$
V_{CC} Supply Current	I_{CC}		85	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$		20	pF	Unmeasured Pins Returned to V_{SS}

AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

Timing Requirements

PARAMETER	SYMBOL	μPD8259A MIN	μPD8259A MAX	μPD8259A-2 MIN	μPD8259A-2 MAX	UNIT	TEST CONDITIONS
A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$↓	t_{AHRL}	0		0		ns	
A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$↑	t_{RHAX}	0		0		ns	
$\overline{RD}$ Pulse Width	t_{RLRH}	235		160		ns	
A0/$\overline{CS}$ Setup to $\overline{WR}$↓	t_{AHWL}	0		0		ns	
A0/$\overline{CS}$ Hold after $\overline{WR}$↑	t_{WHAX}	0		0		ns	
$\overline{WR}$ Pulse Width	t_{WLWH}	290		190		ns	
Data Setup to $\overline{WR}$↑	t_{DVWH}	240		160		ns	
Data Hold after $\overline{WR}$↑	t_{WHDX}	0		0		ns	
Interrupt Request Width (Low)	t_{JLJH}	100		100		ns	①
Cascade Setup to Second or Third $\overline{INTA}$↓ (Slave Only)	t_{CVIAL}	55		40		ns	
End of $\overline{RD}$ to Next Command	t_{RHRL}	160		160		ns	
End of $\overline{WR}$ to Next Command	t_{WHRL}	190		190		ns	
End of Command to next Command (Not same command type)	TCHCL	500		500		ns	②
End of INTA sequence to next INTA sequence							

Note: ① This is the low time required to clear the input latch in the edge triggered mode

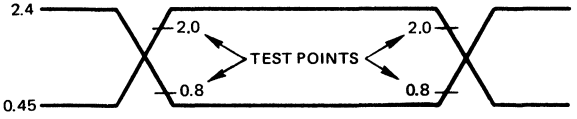
② Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i e 8085A = 1 6 μs, 8085A-2 = 1 μs, 8086 = 1μs, 8086-2 = 625 ns)

Timing Responses

AC CHARACTERISTICS (CONT.)

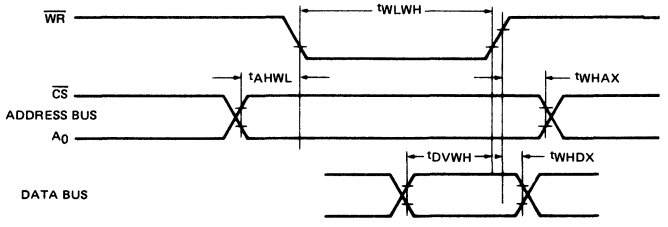
PARAMETER	SYMBOL	μPD8259A		μPD8259A-2		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
Data Valid from $\overline{RD}$/$\overline{INTA}$↓	t_{RLDV}		200		120	ns	C of Data Bus = 100pF
Data Float after $\overline{RD}$/$\overline{INTA}$↑	t_{RHDZ}	10	100	10	85	ns	C of Data Bus
							Max Test C = 100 pF
							Min Test C = 15 pF
Interrupt Output Delay	t_{JHIH}		250		300	ns	
Cascade Valid from First $\overline{INTA}$↓ (Master Only)	t_{IALCV}		565		360	ns	C_{INT} = 100 pF
Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↑	t_{RLEL}		125		100	ns	
Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑	t_{RHEH}		150		150	ns	$C_{CASCADE}$ = 100 pF
Data Valid from Stable Address	t_{AHDV}		200		200	ns	
Cascade Valid to Valid Data	t_{CVDV}		300		200	ns	

INPUT WAVEFORMS FOR AC TESTS

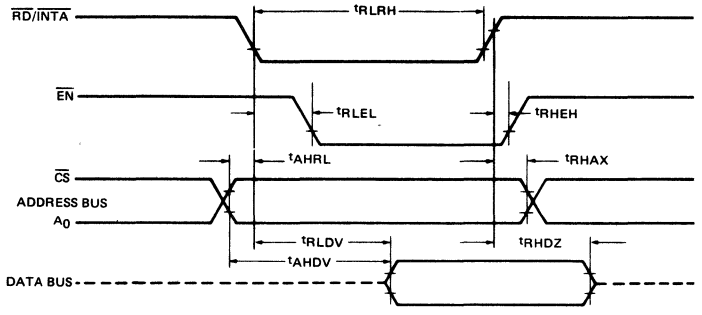


TIMING WAVEFORMS

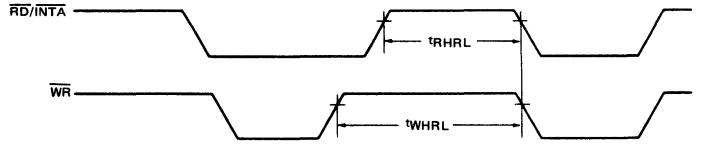
WRITE MODE



READ/$\overline{INTA}$ MODE

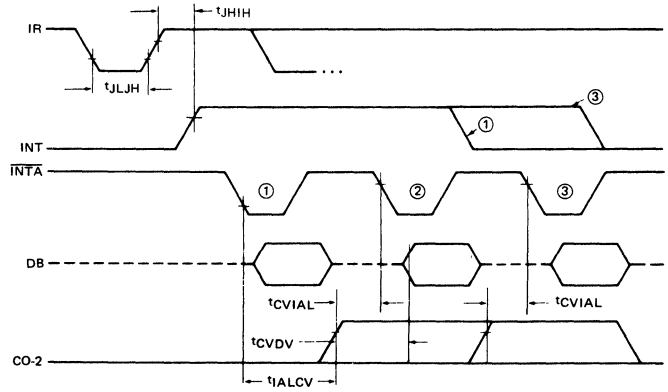


OTHER TIMING

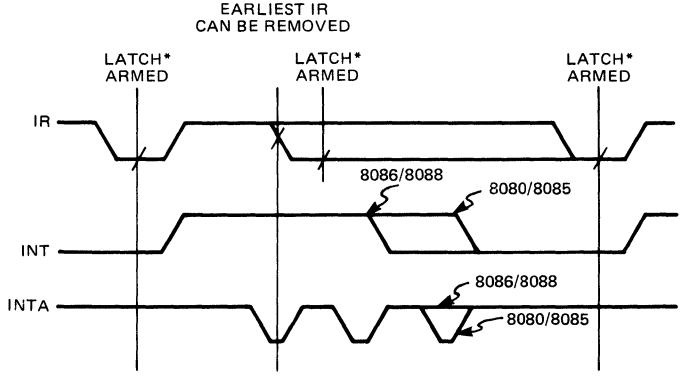


TIMING WAVEFORMS (CONT.)

INTA SEQUENCE



IR TRIGGERING TIMING REQUIREMENTS



*EDGE TRIGGERED MODE ONLY

DETAILED OPERATIONAL DESCRIPTION

The sequence used by the μPD8259A to handle an interrupt depends upon whether an 8080A/8085A or 8086/8088 CPU is being used.

The following sequence applies to 8080A/8085A systems:

The μPD8259A derives its versatility from programmable interrupt modes and the ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259A interacts with the processor.

1. An interrupt or interrupts appearing on IR_{0-7} sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259A will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{INTA}$ to the μPD8259A when it receives the INT.
4. The $\overline{INTA}$ input to the μPD8259A from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The $\overline{INTA}$ also signals the μPD8259A to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more $\overline{INTA}$ pulses to the μPD8259A.

DETAILED OPERATIONAL DESCRIPTION (CONT.)

6. The two $\overline{INTA}$ pulses signal the μPD8259A to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{INTA}$ releases the low-order 8-bits of the address and the second $\overline{INTA}$ releases the high-order 8-bits.
7. The μPD8259A's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259A at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259A to service the next interrupt.

For 8086/8088 systems the first three steps are the same as described above, then the following sequence occurs:

4. During the first $\overline{INTA}$ from the processor, the μPD8259A does not drive the data bus. The highest priority ISR bit is set and the corresponding IRR bit is reset.
5. The μPD8259A puts vector onto the data bus on the second $\overline{INTA}$ pulse from the 8086/8088.
6. There is no third $\overline{INTA}$ pulse in this mode. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse, or it remains set until an EOI command is issued.

INTERRUPT SEQUENCE

8080A/8085A MODE

For these processors, the μPD8259A is controlled by three $\overline{INTA}$ pulses. The first $\overline{INTA}$ pulse will cause the μPD8259A to put the CALL op-code onto the data bus. The second and third $\overline{INTA}$ pulses will cause the upper and lower address of the interrupt vector to be released on the bus.

FIRST $\overline{INTA}$

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

SECOND $\overline{INTA}$

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

INTERRUPT SEQUENCE (CONT.)

THIRD $\overline{INTA}$

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

In this mode only two $\overline{INTA}$ pulses are sent to the μPD8259A. After the first $\overline{INTA}$ pulse, the μPD8259A does not output a CALL but internally sets priority resolution. If it is a master, it sets the cascade lines. The interrupt vector is output to the data bus on the second $\overline{INTA}$ pulse.

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

INITIALIZATION COMMAND WORDS

ICW1 AND ICW2

A_5-A_{15}. *Page starting address of service routines.* In an 8085A system, the 8 request levels generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the μPD8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the μPD8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval maintains compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an MCS-86 system, T7-T3 are inserted in the five most significant bits of the vectoring byte and the μPD8259A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address Interval) has no effect.

LTIM: If LTIM = 1, then the μPD8259A operates in the level interrupt mode. Edge detect logic on the interrupt inputs is disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only μPD8259A in the system. If SNGL = 1 no ICW3 is issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

ICW3

This word is read only when there is more than one μPD8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then releases byte 1 of the call sequence (for 8085A system) and enables the corresponding slave to release bytes 2 and 3 (for 8086/8088 only byte 2) through the cascade lines.

INITIALIZATION COMMAND WORDS (CONT.)

b. In the slave mode (either when SP = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the CALL sequence (or just byte 2 for 8086/8088) are released by it on the Data Bus.

ICW4

SFNM: If SFNM = 1 the special fully nested mode is programmed.

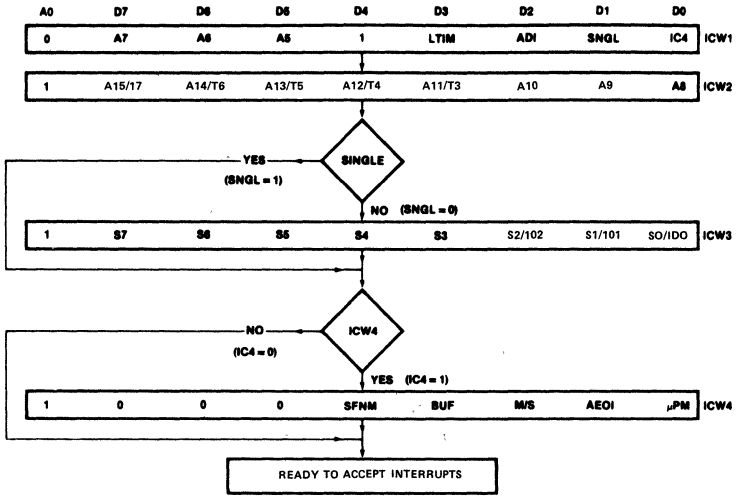
BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the μPD8259A is programmed to be a master, M/S = 0 means the μPD8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the μPD8259A for 8085A system operation, μPM = 1 sets the μPD8259A for 8086 system operation.

INITIALIZATION SEQUENCE



OPPERATIONAL COMMAND WORDS (OCW's) ②

Once the μPD8259A has been programmed with Initialization Command Words, it can be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259A can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCW's.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259A has acknowledged an interrupt, i.e., the μPD8259A has sent an INT signal to the processor and the system controller has sent it an $\overline{\text{INTA}}$ signal, the interrupt input, although it is masked, inhibits lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259A's basic operating mode. It will operate in this mode after the initialization sequence, without requiring Operation Command Words for formatting. Priorities are set IR_0 through IR_7, with IR_0 the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an INTA, the priority resolver determines the priority of the interrupt, sets the corresponding IR bit, and outputs the vector address to the Data bus. The EOI command resets the corresponding ISR bits at the end of its service routines.

Notes: ① Reference Figure 2
② Reference Figure 3

6

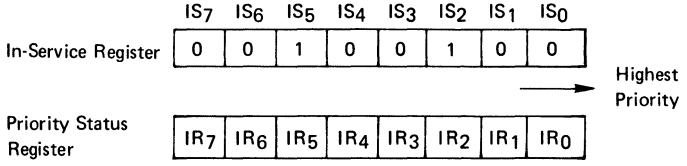
ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

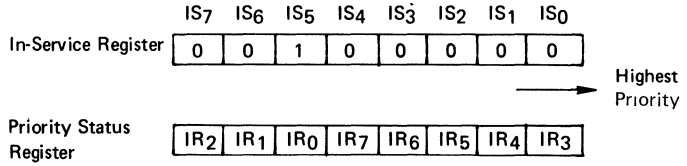
   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:



   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:



   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259A is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259A then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

OPERATIONAL COMMAND WORDS (CONT.)

END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259A is ready to service the next interrupt.

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259A's operating mode.

1. Non-Specific End-of-Interrupt (EOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command automatically resets the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.

2. Specific End-of-Interrupt (SEOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" inhibits lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259A remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

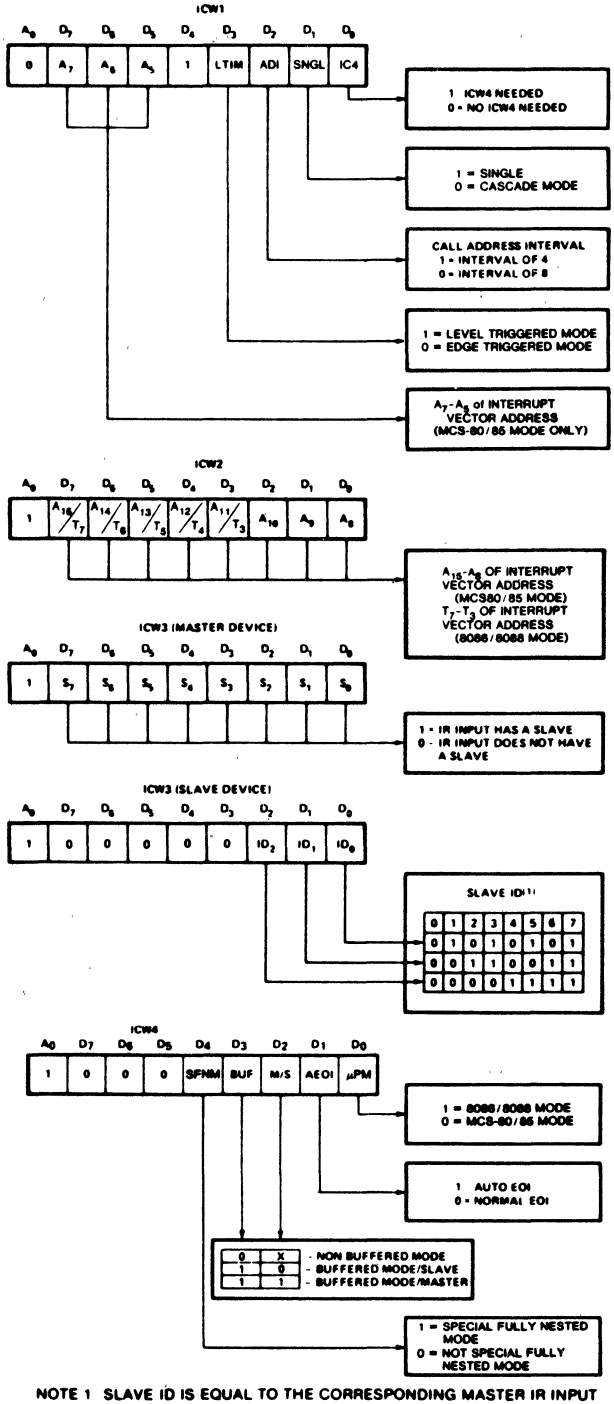
where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

$W_{2\text{-}0}$ forms the binary code of the highest priority level of the interrupts requesting service

Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required, thus saving in ROM space. Poll Mode can also be used to expand the number of interrupts beyond 64.

6

INITIALIZATION COMMAND WORD FORMAT



NOTE 1 SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT

READING μPD8259 STATUS

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. The highest priority in-service bit is reset once it has been acknowledged. (Note that the Interrupt Mask Register has no effect on the IRR.) A WR command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

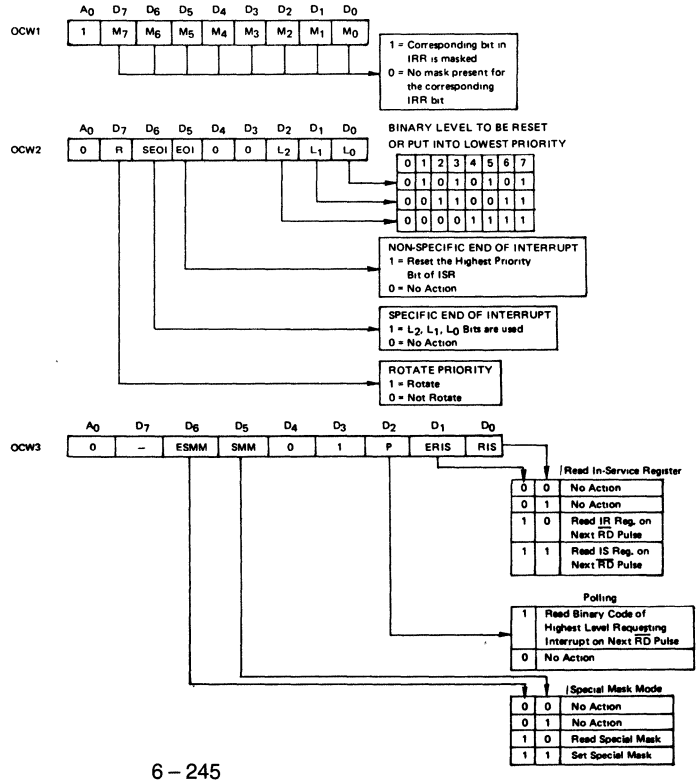
The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode when bits P and ERIS of OCW3 are set to a logic "1."

OPERATION COMMAND WORD FORMAT



SUMMARY OF 8259A INSTRUCTION SET

Inst. #	Mnemonic	A0	D7	D6	D5	D4	D3	D2	D1	D0	Operation Description
1	ICW1 A	0	A7	A6	A5	1	0	1	1	0	Format = 4, single, edge triggered
2	ICW1 B	0	A7	A6	A5	1	1	1	1	0	Format = 4, single, level triggered
3	ICW1 C	0	A7	A6	A5	1	0	1	0	0	Byte 1 Initialization Format = 4, not single, edge triggered
4	ICW1 D	0	A7	A6	A5	1	1	1	0	0	Format = 4, not single, level triggered
5	ICW1 E	0	A7	A6	0	1	0	0	1	0	No ICW4 Required Format = 8, single, edge triggered
6	ICW1 F	0	A7	A6	0	1	1	0	1	0	Format = 8, single, level triggered
7	ICW1 G	0	A7	A6	0	1	0	0	0	0	Format = 8, not single, edge triggered
8	ICW1 H	0	A7	A6	0	1	1	0	0	0	Format = 8, not single, level triggered
9	ICW1 I	0	A7	A6	A5	1	0	1	1	1	Format = 4, single, edge triggered
10	ICW1 J	0	A7	A6	A5	1	1	1	1	1	Format = 4, single, level triggered
11	ICW1 K	0	A7	A6	A5	1	0	1	0	1	Byte 1 Initialization Format = 4, not single, edge triggered
12	ICW1 L	0	A7	A6	A5	1	1	1	0	1	Format = 4, not single, level triggered
13	ICW1 M	0	A7	A6	0	1	0	0	1	1	ICW4 Required Format = 8, single, edge triggered
14	ICW1 N	0	A7	A6	0	1	1	0	1	1	Format = 8, single, level triggered
15	ICW1 O	0	A7	A6	0	1	0	0	0	1	Format = 8, not single, edge triggered
16	ICW1 P	0	A7	A6	0	1	1	0	0	1	Format = 8, not single, level triggered
17	ICW2	1	A15	A14	A13	A12	A11	A10	A9	A8	Byte 2 initialization
18	ICW3 M	1	S7	S6	S5	S4	S3	S2	S1	S0	Byte 3 initialization — master
19	ICW3 S	1	0	0	0	0	0	S2	S1	S0	Byte 3 initialization — slave
20	ICW4 A	1	0	0	0	0	0	0	0	0	No action, redundant
21	ICW4 B	1	0	0	0	0	0	0	0	1	Non-buffered mode, no AEOI, 8086/8088
22	ICW4 C	1	0	0	0	0	0	0	1	0	Non-buffered mode, AEOI, 80/85
23	ICW4 D	1	0	0	0	0	0	0	1	1	Non-buffered mode, AEOI, 8086/8088
24	ICW4 E	1	0	0	0	0	0	1	0	0	No action, redundant
25	ICW4 F	1	0	0	0	0	0	1	0	1	Non-buffered mode, no AEOI, 8086/8088
26	ICW4 G	1	0	0	0	0	0	1	1	0	Non-buffered mode, AEOI, 80/85
27	ICW4 H	1	0	0	0	0	0	1	1	1	Non-buffered mode, AEOI, 8086/8088
28	ICW4 I	1	0	0	0	0	1	0	0	0	Buffered mode, slave, no AEOI, 80/85
29	ICW4 J	1	0	0	0	0	1	0	0	1	Buffered mode, slave, no AEOI, 8086/8088
30	ICW4 K	1	0	0	0	0	1	0	1	0	Buffered mode, slave, AEOI, 80/85
31	ICW4 L	1	0	0	0	0	1	0	1	1	Buffered mode, slave, AEOI, 8086/8088
32	ICW4 M	1	0	0	0	0	1	1	0	0	Buffered mode, master, no AEOI, 80/85
33	ICW4 N	1	0	0	0	0	1	1	0	1	Buffered mode, master, no AEOI, 8086/8088
34	ICW4 O	1	0	0	0	0	1	1	1	0	Buffered mode, master, AEOI, 80/85
35	ICW4 P	1	0	0	0	0	1	1	1	1	Buffered mode, master AEOI, 8086, 8088
36	ICW4 NA	1	0	0	0	1	0	0	0	0	Fully nested mode, 8085A, non-buffered, no AEOI
37	ICW4 NB	1	0	0	0	1	0	0	0	1	ICW4 NB through ICW4 ND are identical to ICW4 B through ICW4 D with the addition of Fully Nested Mode
38	ICW4 NC	1	0	0	0	1	0	0	1	0	
39	ICW4 ND	1	0	0	0	1	0	0	1	1	
40	ICW4 NE	1	0	0	0	1	0	1	0	0	Fully Nested Mode, 80/85, non-buffered, no AEOI
41	ICW4 NF	1	0	0	0	1	0	1	0	1	ICW4 NF through ICW4 NP are identical to ICW4 F through ICW4 P with the addition of Fully Nested Mode
42	ICW4 NG	1	0	0	0	1	0	1	1	0	
43	ICW4 NH	1	0	0	0	1	0	1	1	1	
44	ICW4 NI	1	0	0	0	1	1	0	0	0	
45	ICW4 NJ	1	0	0	0	1	1	0	0	1	
46	ICW4 NK	1	0	0	0	1	1	0	1	0	
47	ICW4 NL	1	0	0	0	1	1	0	1	1	
48	ICW4 NM	1	0	0	0	1	1	1	0	0	
49	ICW4 NN	1	0	0	0	1	1	1	0	1	
50	ICW4 NO	1	0	0	0	1	1	1	1	0	
51	ICW4 NP	1	0	0	0	1	1	1	1	1	
52	OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0	Load mask register, read mark register
53	OCW2 E	0	0	0	1	0	0	0	0	0	Non-specific EOI
54	OCW2 SE	0	0	1	1	0	0	L2	L1	L0	Specific EOI, L0-L2 code of IS FF to be reset
55	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate on Non-Specific EOI
56	OCW2 RSE	0	1	1	1	0	0	L2	L1	L0	Rotate on Specific EOI L0-L2 code of line
57	OCW2 R	0	1	0	0	0	0	0	0	0	Rotate in Auto EOI (set)
58	OCW2 CR	0	0	0	0	0	0	0	0	0	Rotate in Auto EOI (clear)
59	OCW2 RS	0	1	1	0	0	0	L2	L1	L0	Set Priority Command
60	OCW3 P	0	0	0	0	0	1	1	0	0	Poll mode
61	OCW3 RIS	0	0	0	0	0	1	0	1	1	Read IS register

SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

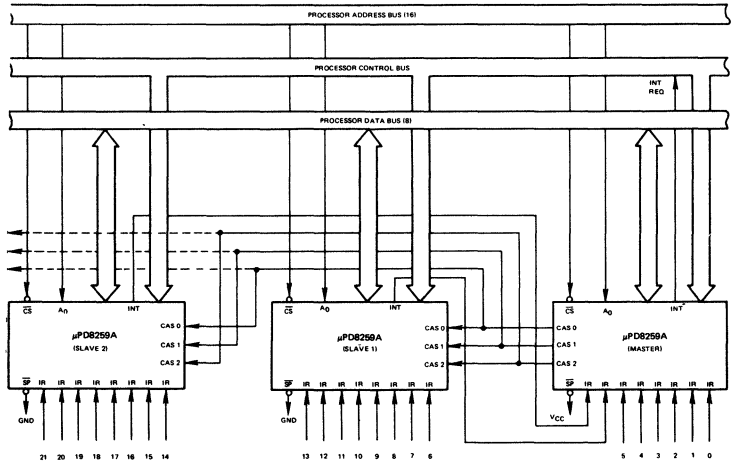
	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

LOWER MEMORY INTERRUPT VECTOR ADDRESS

	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259A's.



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8259AC
Cerdip, μPD8259AD

PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

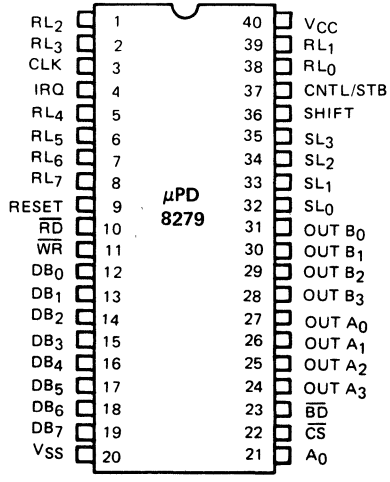
The μPD8279-2 and μPD8279-5 are programmable keyboard and display Input/Output devices. They provide the user with the ability to display data on alphanumeric segment displays or simple indicators. The display RAM can be programmed as 16 x 8 or a dual 16 x 4 and loaded or read by the host processor. The display can be loaded with right or left entry with an auto-increment of the display RAM address.

The keyboard interface provides a scanned signal to a 64 contact key matrix expandable to 128. General sensors or strobed keys may also be used. Keystrokes are stored in an 8 character FIFO and can be either 2 key lockout or N key rollover. Keyboard entries generate an interrupt to the processor.

FEATURES

- Programmable by Processor
- 32 HEX or 16 Alphanumeric Displays
- 64 Expandable to 128 Keyboard
- Simultaneous Keyboard and Display
- 8 Character Keyboard – FIFO
- 2 Key Lockout or N Key Rollover
- Contact Debounce
- Programmable Scan Timer
- Interrupt on Key Entry
- Single +5 Volt Supply, ±10%
- Fully Compatible with 8080A, 8085A, μPD780 (Z80™)
- Available in 40 Pin Plastic Package

PIN CONFIGURATION



PIN NAMES

DB_{0-7}	Data Bus (Bi-directional)
CLK	Clock Input
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Buffer Address
IRQ	Interrupt Request Output
SL_{0-3}	Scan Lines
RL_{0-7}	Return Lines
SHIFT	Shift Input
CNTL/STB	Control/Strobe Input
$OUT\ A_{0-3}$	Display (A) Outputs
$OUT\ B_{0-3}$	Display (B) Outputs
$\overline{BD}$	Bland Display Output

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μPD8279

FUNCTIONAL DESCRIPTION

The μPD8279 has two basic functions: 1) to control displays to output and 2) to control a keyboard for input. Its specific purpose is to unburden the host processor from monitoring keys and refreshing displays. The μPD8279 is designed to directly interface the microprocessor bus. The microprocessor must program the operating mode to the μPD8279. These modes are as follows:

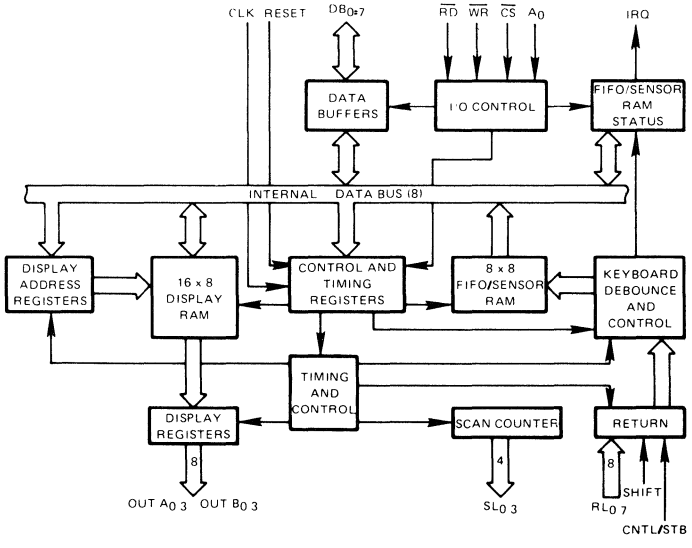
Output Modes

- 8 or 16 Character Display
- Right or Left Entry

Input Modes

- Scanned Keyboard with Encoded 8 x 8 x 4 Key Format or Decoded 4 x 8 x 8 Scan Lines.
- Scanned Sensor Matrix with Encoded 8 x 8 or Decoded 4 x 8 Scan Lines
- Strobed Input.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0 5 to +7 Volts①
All Input Voltages	-0 5 to +7 Volts①
Supply Voltages	-0 5 to +7 Volts①
Power Dissipation	1W

Note ① With respect to V_{SS}

$T_a = 25°C$

*COMMENT. Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN IDENTIFICATION

PIN			DESCRIPTION
NO.	SYMBOL	NAME	
1, 2, 5, 6, 7, 8, 38, 39	RL_{0-7}	Return Lines	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode
3	CLK	Clock	Clock from system used to generate internal timing
4	IRQ	Interrupt Request	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/ Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
9	Reset	Reset Input	A high signal on this pin resets the μPD8279.
10	$\overline{RD}$	Read Input	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
11	$\overline{WR}$	Write Input	
12 19	DB_{0-7}	Data Bus	Bi-Directional data bus All data and commands between the processor and the μPD8279 are transmitted on these lines.
20	V_{SS}	Ground Reference	Power Supply Ground
21	A_0	Buffer Address	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status A low indicates that they are data
22	$\overline{CS}$	Chip Select	Chip Select. A low on this pin enables the interface functions to receive or transmit.
23	$\overline{BD}$	Blank Display Output	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.
24-27	$OUT\ A_{0-3}$	Display A Outputs	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4-bit ports may be blanked independently. These two ports may also be considered as one 8-bit port
28-31	$OUT\ B_{0-3}$	Display B Outputs	
32-35	SL_{0-3}	Scan Lines	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
36	Shift	Shift Input	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low
37	CNTL/STB	Control/ Strobe Input	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in Strobed input mode (Rising Edge) It has an active internal pullup to keep it high until a switch closure pulls it low
40	V_{CC}	+5V Input	Power Supply Input

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage for Return Lines	V_{IL1}	-0.5		1.4	V	
Input Low Voltage (Others)	V_{IL2}	-0.5		0.8	V	
Input High Voltage for Return Lines	V_{IH1}	2.2			V	
Input High Voltage (Others)	V_{IH2}	2.0			V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage on Interrupt Line	IRQ Pin	+3.5			V	I_{OH} = -50μA
		+2.4			V	I_{OH} = -400μA
	OTHERS	+2.4			V	I_{OH} = -400μA
Input Current on Shift, Control and Return Lines	I_{IL1}			+10	μA	V_{IN} = V_{CC}
				-100	μA	V_{IN} = 0V
Input Leakage Current (Others)	I_{IL2}			±10	μA	V_{IN} = V_{CC} to 0V
Output Float Leakage	I_{OFL}			±10	μA	V_{OUT} = V_{CC} to 0V
Power Supply Current	I_{CC}			120	mA	

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}	5		10	pF	V_{IN} = V_{CC}
Output Capacitance	C_{OUT}	10		20	pF	V_{OUT} = V_{CC}

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
READ		μPD8279-5		μPD8279-2			
Address Stable Before $\overline{READ}$	t_{AR}	0		0		ns	
Address Hold Time for $\overline{READ}$	t_{RA}	0		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	250		200		ns	
Data Delay from $\overline{READ}$	t_{RD}		150		140	ns	C_L = 150 pF
Address to Data Valid	t_{AD}		250		250	ns	C_L = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	10	100	10	100	ns	
Read Cycle Time	t_{RCY}	1000		200		ns	
WRITE							
Address Stable Before $\overline{WRITE}$	t_{AW}	0		0		ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	0		0		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	250		200		ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	150		150		ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	0		0		ns	
Write Cycle Time	t_{WCY}	1000		200		ns	
OTHER							
Clock Pulse Width	$t_{\phi W}$	120		70		ns	
Clock Period	t_{CY}	320		200		ns	

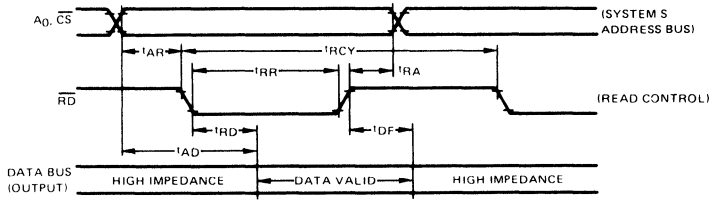
GENERAL TIMING

Keyboard Scan Time:	5.1 ms	Digit-on Time:	480 μs
Keyboard Debounce Time:	10.3 ms	Blanking Time:	160 μs
Key Scan Time:	80 μs	Internal Clock Cycle:	10 μs
Display Scan Time:	10.3 ms		

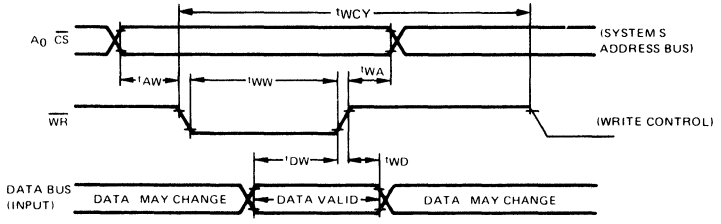
TIMING WAVEFORMS

INPUT FOR AC TESTS

READ



WRITE



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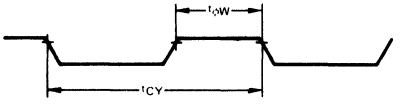
CLOCK INPUT



OPERATIONAL DESCRIPTION

The following is a description of each section of the μPD8279. See the block diagram for functional reference.

I/O Control and Data Buffers

Communication to and from the μPD8279 is performed by selecting $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$. The type of information written or read by the processor is selected by A_0. A logic 0 states that information is data while a 1 selects command or status. $\overline{RD}$ and $\overline{WR}$ select the direction by which the transfer occurs through the Data Buffers. When the chip is deselected ($\overline{CS}$ = 1) the bi-directional Data Buffers are in a high impedance state thus enabling the μPD8279 to be tied directly to the processor data bus.

Timing Registers and Timing Control

The Timing Registers store the display and keyboard modes and other conditions programmed by the processor. The timing control contains the timing counter chain. One counter is a divide by N scaler which may be programmed to match the processor cycle time. The scaler must take a value between 2 and 31 in binary. A value which scales the internal frequency to 100 KHz gives a 5.1 ms scan time and 10.3 ms switch debounce. The other counters divide down to make key, row matrix and display scans.

Scan Counter

The scan counter can operate in either the encoded or decoded mode. In the encoded mode, the counter provides a count which must be decoded to provide the scan lines. In the decoded mode, the counter provides a 1 out of 4 decoded scan. In the encoded mode the scan lines are active high and in the decoded mode they are active low.

Return Buffers, Keyboard Debounce and Control

The eight return lines are buffered and latched by the return buffers. In the keyboard mode these lines are scanned sampling for key closures in each row. If the debounce circuit senses a closure, about 10 ms are timed out and a check is performed again. If the switch is still pressed, the address of the switch matrix plus the status of shift and control are written into the FIFO. In the scanned sensor mode, the contents of return lines are sent directly to the sensor RAM (FIFO) each key scan. In the strobed mode, the transfer takes place on the rising edge of CNTL/STB.

FIFO/Sensor RAM and Status

This section is a dual purpose 8 x 8 RAM. In strobe or keyboard mode it is a FIFO. Each entry is pushed into the FIFO and read in order. Status keeps track of the number of entries in the FIFO. Too many reads or writes to the FIFO will be treated as an error condition. The status logic generates an IRQ whenever the FIFO has an entry. In the sensor mode the memory is a sensor RAM which detects changes in the status of a sensor. If a change occurs, the IRQ is generated until the change is acknowledged.

Display Address Registers and Display RAM

The Display Address Register contains the address of the word being read or written by the processor, as well as the word being displayed. This address may be programmed to auto-increment after each read or write. The display RAM may be read by the processor any time after the mode and address is set. Data entry to the display RAM may be set to either right or left entry.

COMMAND OPERATION

The commands programmable to the μPD8279 via the data bus with $\overline{CS}$ active (0) and A_0 high are as follows

Keyboard/Display Mode Set

0	0	0	D	D	K	K	K

MSB LSB

Display Mode

DD

0	0	8-8-bit character display – Left entry
0	1 ①	16-8 bit character display – Left entry
1	0	8-8 bit character display – Right entry
1	1	16-8 bit character display – Right entry

Note ① Power on default condition

Keyboard Mode

KKK

0	0	0	Encoded Scan – 2 Key Lockout
0	0	1	Decoded Scan – 2 Key Lockout
0	1	0	Encoded Scan – N Key Rollover
0	1	1	Decoded Scan – N Key Rollover
1	0	0	Encoded Scan-Sensor Matrix
1	0	1	Decoded Scan-Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value between 2 and 31 this prescaler divides the external clock by PPPPP to develop its internal frequency After reset, a default value of 31 is generated

Read FIFO/Sensor RAM

0	1	0	A1	X	A	A	A

$A_0 = 0$

A_1 is the auto-increment flag. AAA is the row to be read by the processor The read command is accomplished with ($\overline{CS} \cdot RD \cdot \overline{A0}$) by the processor If A_1 is 1, the row select counter will be incremented after each read. Note that auto-incrementing has no effect on the display.

Read Display RAM

0	1	1	A1	A	A	A	A

$A_0 = 0$

Where A_1 is the auto-increment flag and AAAA is the character which the processor is about to read.

Write Display RAM

1	0	0	A1	A	A	A	A

where AAAA is the character the processor is about to write

Display Write Inhibit Blanking

1	0	1	X	IW A	IW B	BL A	BL B

Where IWA and IWB are Inhibit Writing nibble A and B respectively, and BLA, BLB are blanking. When using the display as a dual 4-bit, it is necessary to mask one of the 4-bit halves to eliminate interaction between the two halves. This is accomplished with the IW flags. The BL flags allow the programmer to blank either half of the display independently. To blank a display formatted as a single 8-bit, it is necessary to set both BLA and BLB. Default after a reset is all zeros. All signals are active high (1).

Clear

1	1	0	C_D	C_D	C_D	C_F	C_A

C_D	C_D	C_D	
1	0	X	All zeros
1	1	0	AB = 20_{16}
1	1	1	All ones
0	X	X	Disable clear display

This command is used to clear the display RAM, the FIFO, or both. The C_D options allow the user the ability to clear the display RAM to either all zeros or all ones.

C_F clears the FIFO.
C_A clears all.

Clearing the display takes one complete display scan. During this time the processor can't write to the display RAM.

C_F will set the FIFO empty flag and reset IRQ. The sensor matrix mode RAM pointer will then be set to row 0.

C_A is equivalent to C_F and C_D. The display is cleared using the display clear code specified and resets the internal timing logic to synchronize it.

End Interrupt/Error Mode Set

1	1	1	E	X	X	X	X

In the sensor matrix mode, this instruction clears IRQ and allows writing into RAM.

In N key rollover, setting the E bit to 1 allows for operating in the special Error mode. See Description of FIFO status.

FIFO Status

D_U	S/E	O	U	F	N	N	N

Where: D_U = Display Unavailable because a clear display or clear all command is in progress.
S/E = Sensor Error flag due to multiple closure of switch matrix.
O = FIFO Overrun since an attempt was made to push too many characters into the FIFO.
U = FIFO Underrun. An indication that the processor tried to read an empty FIFO.
F = FIFO Full Flag.
NNN = The Number of characters presently in the FIFO.

The FIFO Status is Read with A_0 high and $\overline{CS}$, $\overline{RD}$ active low.

The Display not available is an indication that the C_D or C_A command has not completed its clearing. The S/E flags are used to show an error in multiple closures has occurred. The O or U, overrun or underrun, flags occur when too many characters are written into the FIFO or the processor tries to read an empty FIFO. F is an indication that the FIFO is full and NNN is the number of characters in the FIFO.

Data Read

Data can be read during A_0 = 0 and when $\overline{CS}$, $\overline{RD}$ are active low. The source of the data is determined by the Read Display or Read FIFO commands.

Data Write

Data is written to the chip when A_0, $\overline{CS}$, and $\overline{WR}$ are active low. Data will be written into the display RAM with its address selected by the latest Read or Write Display command.

COMMAND OPERATION (CONT.)

Data Format

CNTL	SH	SCAN	RET

In the Scanned Key mode, the characters in the FIFO correspond to the above format where CNTL and SH are the most significant bits and the SCAN and return lines are the scan and column counters.

RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

In the Sensor Matrix mode, the data corresponds directly to the row of the sensor RAM being scanned. Shift and control (SH, CNTL) are not used in this mode.

Control Address Summary

A_0	DATA MSB							LSB	
1	0	0	0	D	D	K	K	K	Keyboard Display Mode Set
1	0	0	1	P	P	P	P	P	Load Program Clock
0	0	1	0	A_1	X	A	A	A	Read FIFO/Sensor RAM
0	0	1	1	A_1	A	A	A	A	Read Display RAM
1	1	0	0	A_1	A	A	A	A	Write Display RAM
1	1	0	1	X	IW A	IW B	BL A	BL B	Display Write Inhibit/Blanking
1	1	1	0	C_D	C_D	C_D	C_F	C_A	Clear
1	1	1	1	E	X	X	X	X	End Interrupt/Error Mode Set
1	D_U	S/E	0	U	F	N	N	N	FIFO Status

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Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8279C-5
Ceramic, μPD8279D-5

Notes

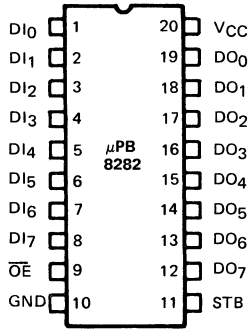
OCTAL LATCH

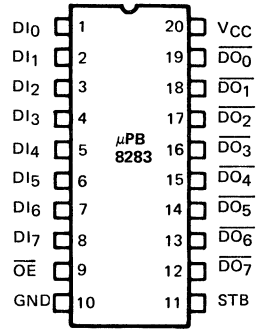
DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. The 8282 is non-inverting and the 8283 inverts the input data. These devices are ideal for demultiplexing the address/data buses on the 8085A/8086 microprocessors.
The 8282/8283 are fabricated using NEC's Schottky bipolar process.

FEATURES

- Supports 8080, 8085A, 8048, 8086 Family Systems
- Transparent During Active Strobe
- Fully Parallel 8-Bit Data Register and Buffer
- High Output Drive Capability (32 mA) for Driving the System Data Bus
- Tri-State Outputs
- 20-Pin Package





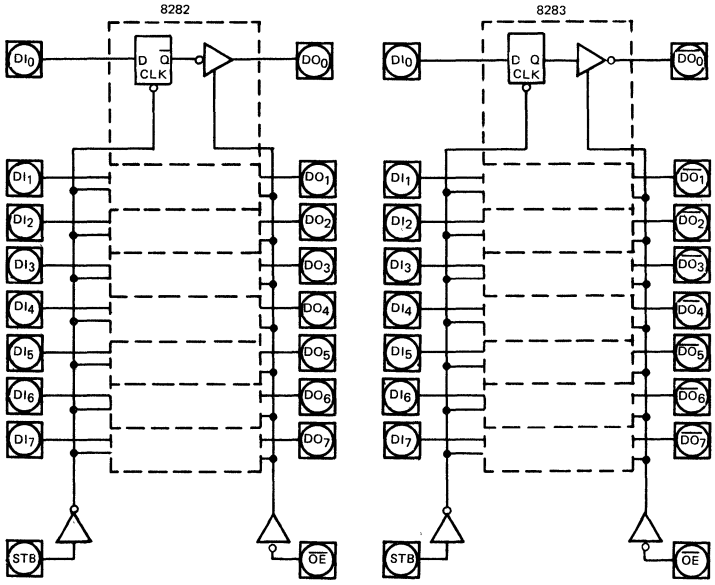
PIN NAMES

DI_0-DI_7	DATA IN
DO_0DO_7	DATA OUT
$\overline{OE}$	OUTPUT ENABLE
STB	STROBE

FUNCTIONAL DESCRIPTION

The μPB8282/8283 are 8-bit latches with tri-state output buffers. Data on the inputs is latched into the data latches on a high to low transition of the STB line. When STB is high, the latches appear transparent. The $\overline{OE}$ input enables the latched data to be transferred to the output pins. When $\overline{OE}$ is high, the outputs are put in the tri-state condition. $\overline{OE}$ will not cause transients to appear on the data outputs.

BLOCK DIAGRAMS



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 5.5V

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Conditions: V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		160	mA	
Forward Input Current	I_F		−0.2	mA	V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Output Low Voltage	V_{OL}		0 45	V	I_{OL} = 32 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −5 mA
Output Off Current	I_{OFF}		±50	μA	V_{OFF} = 0.45 to 5.25V
Input Low Voltage	V_{IL}		0.8	V	V_{CC}=5.0V①
Input High Voltage	V_{IH}	2.0		V	V_{CC}=5.0V①
Input Capacitance	C_{IN}		12	pF	V_{BIAS}=2.5V, V_{CC}=5V, T_a=25°C, F=1 MHz

Note: ① Output Loading I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF

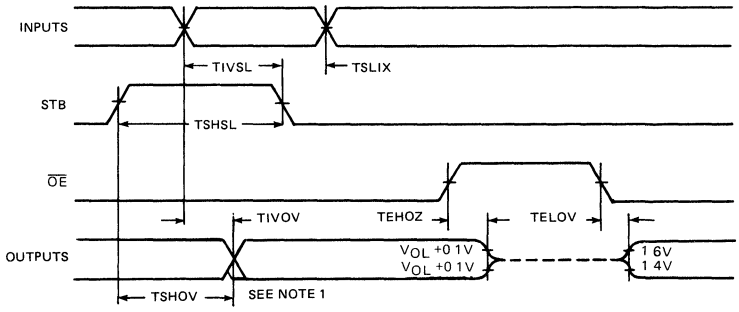
AC CHARACTERISTICS

Conditions: V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

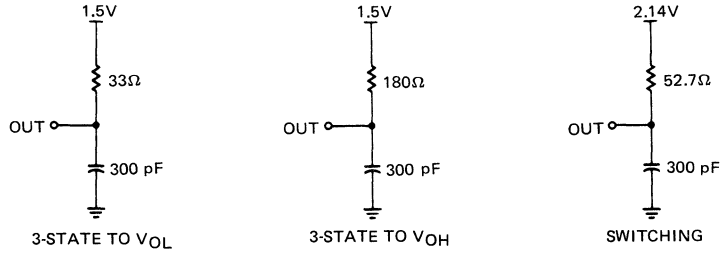
Loading: Outputs – I_{OL} = 32 mA, I_{OH} = –5 mA, C_L = 300 pF

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input to Output Delay	TIVOV	5		
—Inverting			22	ns
—Non-Inverting		5	30	ns
STB to Output Delay	TSHOV			
—Inverting		10	40	ns
—Non-Inverting		10	45	ns
Output Disable Time	TEHOZ	5	22	ns
Output Enable Time	TELOV	10	30	ns
Input to STB Setup Time	TIVSL	0		ns
Input to STB Hold Time	TSLIX	25		ns
STB High Time	TSHSL	15		ns
Input, Output Rise Time	T_{ILIH}, T_{OLOH}		20	ns
Input, Output Fall Time	T_{IHIL}, T_{OHOL}		12	nw

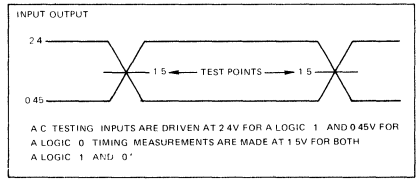
TIMING WAVEFORMS



Note: Output may be momentarily invalid following the high going into STB transition.



AC TESTING INPUT, OUTPUT WAVEFORM



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPB8282C/83C
Cerdip, μPB8282D/83D

CLOCK GENERATOR AND DRIVER FOR 8086/8088 MICROPROCESSORS

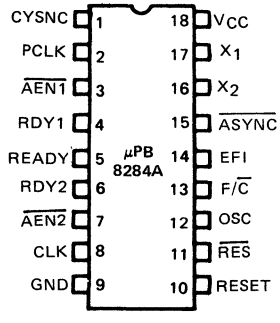
DESCRIPTION

The μPB8284A is a clock generator and driver for the 8066 and 8088 microprocessors. This bipolar driver provides the microprocessor with a reset signal and also provides properly synchronized READY timing. A TTL clock is also provided for peripheral devices.

FEATURES

- Generate System Clock for the 8086 and 8088
- Frequency Source can be a Crystal or a TTL Signal
- MOS Level Output for the Processor
- TTL Level Output for Peripheral Devices
- Power-Up Reset for the Processor
- READY Synchronization
- +5V Supply
- 18 Pin Package

PIN CONFIGURATION



PIN NAMES

X_1, X_2	Crystal Connections
TANK	For Overtone Crystal
F/C	Clock Source Select
EFI	External Clock Input
CSYNC	Clock Synchronization Input
RDY1, RDY2	Ready Signal from Multibus™* Systems
AEN1, AEN2	Address Enable Qualifiers for the two RDY Signals
RES	Reset Input
RESET	Synchronized Reset Output
OSC	Oscillator Output
CLK	MOS Clock for the Processor
PCLK	TTL Clock for Peripherals
READY	Synchronized Ready Output

*TM - Multibus is a trademark of Intel Corporation.

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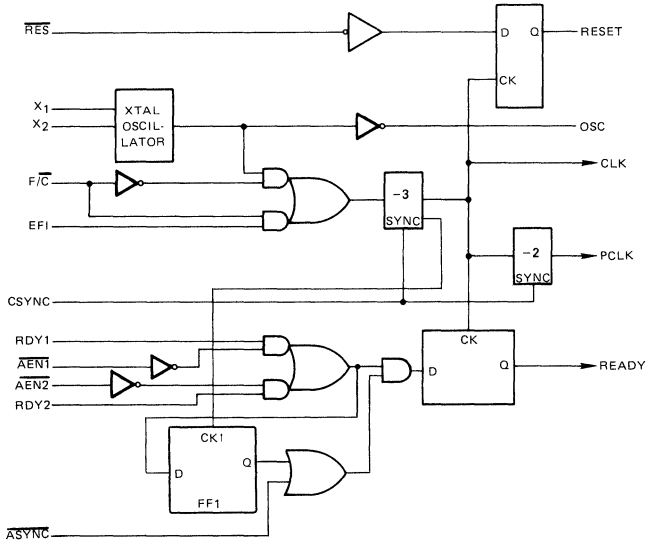
PIN IDENTIFICATION

NO.	SYMBOL	NAME	FUNCTION
1	CSYNC	Clock Synchronization	An active high signal which allows multiple 8284s to be synchronized. When CYSNC is low, the internal counters count and when high the counters are reset. CYSNC should be grounded when the internal oscillator is used.
2	PCLK	Peripheral Clock	A TTL level clock for use with peripheral devices. This clock is one-half the frequency of CLK.
3, 7	$\overline{AEN1}$, $\overline{AEN2}$	Address Enable	This active low signal is used to qualify its respective RDY inputs. If there is only one bus to interface to, $\overline{AEN}$ inputs are to be grounded.
4, 6	RDY1, RDY2	Bus Ready	This signal is sent to the 8284 from a peripheral device on the bus to indicate that data has been received or data is available to be read.
5	READY	Ready	The READY signal to the microprocessor is synchronized by the RDY inputs to the processor CLK. READY is cleared after the guaranteed hold time to the processor has been met.
8	CLK	Processor Clock	This is the MOS level clock output of 33% duty cycle to drive the microprocessor and bipolar support devices (8288) connected to the processor. The frequency of CLK is one third of the crystal or EFI frequency.
10	RESET	Reset	This is used to initialize the processor. Its input is derived from an RC connection to a Schmitt trigger input for power up operation.
11	$\overline{RES}$	Reset In	This Schmitt trigger input is used to determine the timing of RESET out via an RC circuit.
12	OSC	Oscillator Output	This TTL level clock is the output of the oscillator circuit running at the crystal frequency.
13	F/$\overline{C}$	Frequency Crystal Select	F/$\overline{C}$ is a strapping option used to determine where CLK is generated. A high is for the EFI input, and a low is for the crystal.
14	EFI	External Frequency In	A square wave in at three times the CLK output. A TTL level clock to generate CLK.
16, 17	X_1, X_2	Crystal In	A crystal is connected to these inputs to generate the processor clock. The crystal chosen is three times the desired CLK output.
15	$\overline{ASYNC}$	Asynchronous Input	Ready Synchronization Select. $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, 2 stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH, a single stage of READY synchronization is provided.
18	VCC	VCC	+5V

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The clock generator can provide the system clock from either a crystal or an external TTL source. There is an internal divide by three counter which receives its input from either the crystal or TTL source (EFI Pin) depending on the state of the F/$\overline{C}$ input strapping. There is also a clear input (C SYNC) which is used for either inhibiting the clock, or synchronizing it with an external event (or perhaps another clock generator chip). Note that if the TTL input is used, the crystal oscillator section can still be used for an independent clock source, using the OSC output.

For driving the MOS output level, there is a 33% duty cycle MOS output (CLK) for the microprocessor, and a TTL output (PCLK) with a 50% duty cycle for use as a peripheral clock signal. This clock is at one half of the processor clock speed.

Reset timing is provided by a Schmitt Trigger input ($\overline{RES}$) and a flip-flop to synchronize the reset timing to the falling edge of CLK. Power-on reset is provided by a simple RC circuit on the $\overline{RES}$ input.

There are two READY inputs, each with its own qualifier ($\overline{AEN1}$, $\overline{AEN2}$). The unused $\overline{AEN}$ signal should be tied low.

The READY logic in the 8284A synchronizes the RDY1 and RDY2 asynchronous inputs to the processor clock to insure proper set up time, and to guarantee proper hold time before clearing the ready signal.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V

T_a = 25°C

*COMMENT Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Conditions: T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Forward Input Current ($\overline{ASYNC}$) (Other Inputs)	I_F		-1.3 -0.5	mA	V_F = 0.45V V_F = 0.45V
Reverse Input Current	I_R		50	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C		-1.0	V	I_C = -5 mA
Power Supply Current	I_{CC}		140	mA	
Input Low Voltage	V_{IL}		0.8	V	V_{CC} = 5.0V
Input High Voltage	V_{IH}	2.0		V	V_{CC} = 5.0V
Reset Input High Voltage	V_{IHR}	2.6		V	V_{CC} = 5.0V
Output Low Voltage	V_{OL}		0.45	V	5 mA = I_{OL}
Output High Voltage (CLK) (Other Outputs)	V_{OH}	4 2.4		V V	-1 mA } I_{OH} -1 mA }
$\overline{RES}$ Input Hysteresis	V_{IHR}-V_{ILR}	0.25		V	V_{CC} = 5.0V

AC CHARACTERISTICS

Conditions: T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
External Frequency High Time	TEHEL	13		ns	90%-90% V_{IN}
External Frequency Low Time	TELEH	13		ns	10%-10% V_{IN}
EFI Period	TELEL	TEHEL + TELEH + δ		ns	(1)
XTAL Frequency		12	25	MHz	
RDY1, RDY2 Set-Up to CLK	TR1VCL	35		ns	
RDY1, RDY2 Hold to CLK	TCLR1X	0		ns	
AEN1, AEN2 Set-Up to RDY1, RDY2	TA1VR1V	15		ns	
AEN1, AEN2 Hold to CLK	TCLA1X	0		ns	
CSYNC Set-Up to EFI	TYHEH	20		ns	
CSYNC Hold to EFI	TEHYL	10		ns	
CSYNC Width	TYHYL	2 TELEL		ns	
RES Set-Up to CLK	TI1HCL	65		ns	(2)
RES Hold to CLK	TCLI1H	20		ns	(2)
RDY1, RDY2 Active Set-Up to CLK	t_{R1VCH}	35		ns	$\overline{ASYNC}$ = LOW
RDY1, RDY2 Inactive Set-Up to CLK	t_{R1VCL}	35		ns	
$\overline{ASYNC}$ Set-Up to CLK	t_{AYVCL}	50		ns	
$\overline{ASYNC}$ Hold to CLK	t_{CLAYX}	0		ns	
Input Rise Time	t_{ILIH}		20	ns	From 0.8V to 2.0V
Input Fall Time	t_{ILIL}		12	ns	From 2.0V to 0.8V

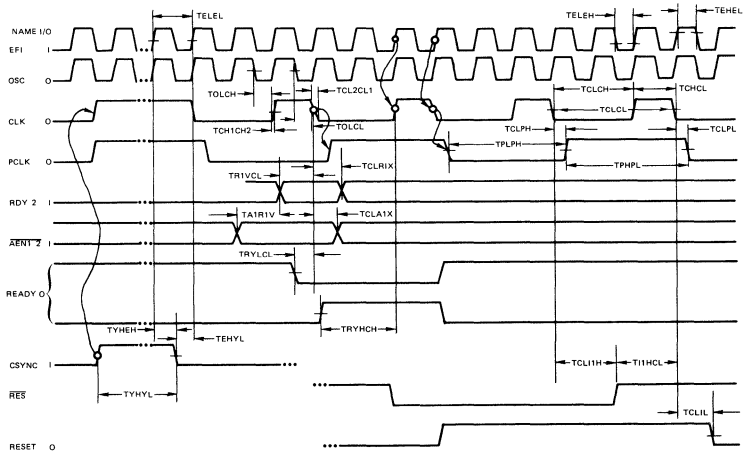
AC CHARACTERISTICS (CONT.)

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
CLK Cycle Period	TCLCL	125		ns	
CLK High Time	TCHCL	(1/3 TCLCL) +2 0		ns	Figure 3 and Figure 4
CLK Low Time	TCLCH	(2/3 TCLCL) -15 0		ns	Figure 3 and Figure 4
CLK Rise and Fall Time	TCH1CH2 TCL2CL1		10	ns	1 0V to 3 5V
PCLK High Time	TPHPL	TCLCL -20		ns	
PCLK Low Time	TPLPH	TCLCL -20		ns	
Ready Inactive to CLK (4)	TRYLCL	-8		ns	Figure 5 and Figure 6
Ready Active to CLK (3)	TRYHCH	(2/3 TCLCL) -15 0		ns	Figure 5 and Figure 6
CLK To Reset Delay	TCLIL		40	ns	
CLK to PCLK High Delay	TCLPH		22	ns	
CLK to PCLK Low Delay	TCLPL		22	ns	
OSC to CLK High Delay	TOLCH	-5	12	ns	
OSC to CLK Low Delay	TOLCL	2	22	ns	
Output Rise Time (except CLK)	t_{OLOH}		20	ns	From 0 8V to 2 0V
Output Fall Time (except CLK)	t_{OHOL}		12	ns	From 2 0V to 0.8V

Notes: (1) δ = EFI rise (5 ns max) + EFI fall (5 ns max)
(2) Set up and hold only necessary to guarantee recognition at next clock.
(3) Applies only to T3 and TW states
(4) Applies only to T2 states

TIMING WAVEFORM*



*ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED

AC TEST CIRCUITS

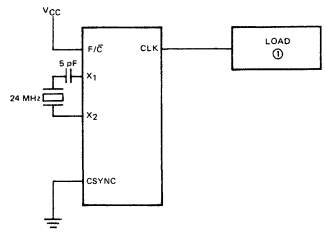


FIGURE 1
CLOCK HIGH AND LOW TIME

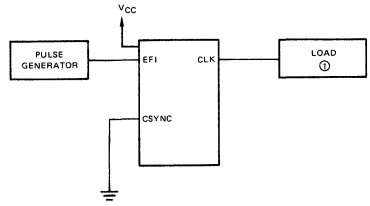


FIGURE 2
CLOCK HIGH AND LOW TIME

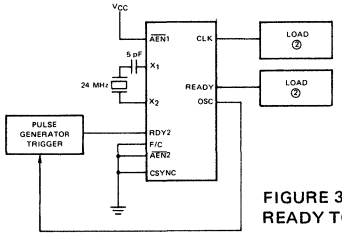


FIGURE 3
READY TO CLK

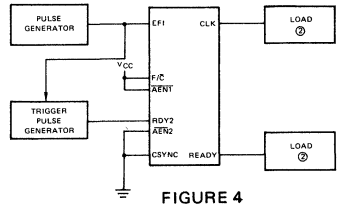
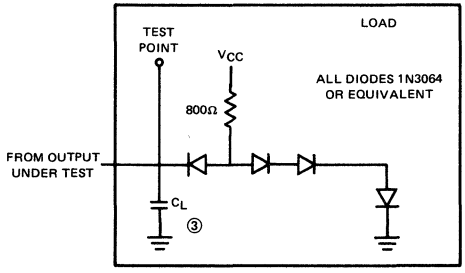
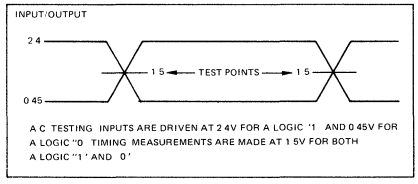


FIGURE 4
READY TO CLK



NOTES ① C_L = 100 pF
② C_L = 30 pF
③ C_L INCLUDES PROBE AND JIG CAPACITANCE

AC TESTING INPUT, OUTPUT WAVEFORM



Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8284AC
Cerdip, μPB8284AD

8-BIT BUS TRANSCEIVER

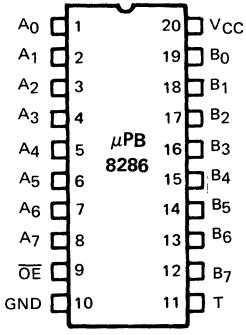
DESCRIPTION

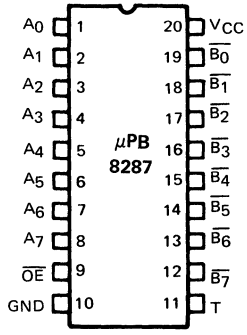
The 8286 and 8287 are octal bus transceivers used for buffering microprocessor bus lines. Being bi-directional, they are ideal for buffering the data bus lines on 8- or 16-bit microprocessors. Each B output is capable of driving 32 mA low or 5 mA high.

FEATURES

- Data Bus Buffer Driver for μCOM-8 (8080, 8085A, 780) and μCOM-16 (8086) families
- Low Input Load Current — 0.2 mA max
- High Output Drive Capability for Driving System Data Bus
- Tri-State Outputs
- 20 Pin Package with Fully Parallel 8-Bit Transceivers

PIN CONFIGURATIONS



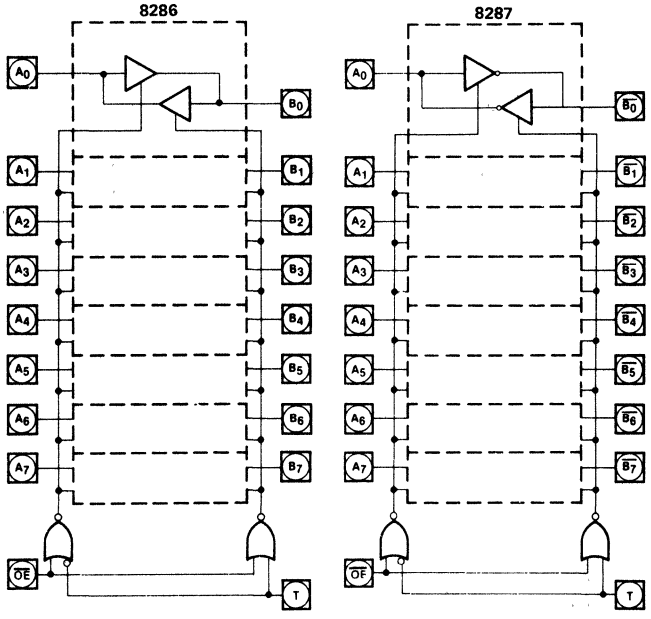


PIN NAMES

A_0-A_7	Local Bus Data
B_0-B_7	System Bus Data
$\overline{OE}$	Output Enable
T	Transmit

6

BLOCK DIAGRAMS



$\overline{OE}$	T	RESULT
0	0	B → A
0	1	A → B
1	0	A and B HIGH IMPEDANCE
1	1	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

PARAMETER		SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Input Clamp Voltage		V_C		−1	V	I_C = −5 mA
Power Supply Current	− 8287	I_{CC}		130	mA	
	− 8286	I_{CC}		160	mA	
Forward Input Current		I_F		−0 2	mA	V_F = 0 45V
Reverse Input Current		I_R		50	μA	V_R = 5.25V
Output Low Voltage	− B Outputs	V_{OL}		0.45	V	I_{OL} = 32 mA
	− A Outputs			0.45	V	I_{OL} = 16 mA
Output High Voltage	− B Outputs	V_{OH}	2 4		V	I_{OH} = −5 mA
	− A Outputs		2.4		V	I_{OH} = −1 mA
Output Off Current		I_{OFF}		I_F		V_{OFF} = 0 45V
Output Off Current		I_{OFF}		I_R		V_{OFF} = 5 25V
Input Low Voltage	− A Side	V_{IL}		0.8	V	V_{CC} = 5 0V ①
	− B Side	V_{IL}		0 9	V	V_{CC} = 5 0V ①
Input High Voltage		V_{IH}	2.0		V	V_{CC} = 5 0V ① F = 1 MHz
Input Capacitance	− A Side	C_{IN}		16	pF	V_{BIAS} = 2.5V, V_{CC} = 5V T_a = 25°C F = 1 MHz

Note ① B Outputs − I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
A Outputs − I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 100 pF

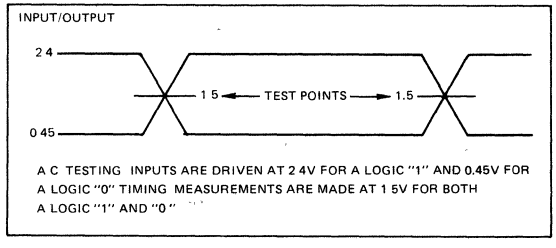
AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 10%

SYMBOL	PARAMETER	MIN	MAX	UNITS
TIVOV	Input to Output Delay			
	Inverting	5	22	ns
	Non-Inverting	5	30	ns
TEHTV	Transmit/Receive Hold Time	TEHOZ		ns
TTVEL	Transmit/Receive Setup	10		ns
TEHOZ	Output Disable Time	5	22	ns
TELOV	Output Enable Time	10	30	ns
TILIH, TOLOH	Input Output Rise Time		20	ns
TIHIL, TOHOL	Input Output Fall Time		12	ns

Notes: See waveforms and test load circuit.
B Outputs − I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
A Outputs − I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 100 pF

AC TESTING INPUT, OUTPUT WAVEFORM



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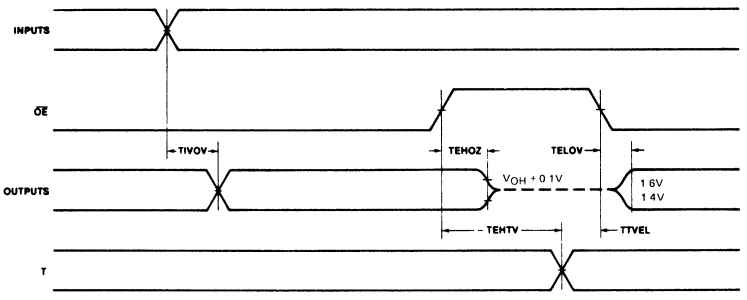
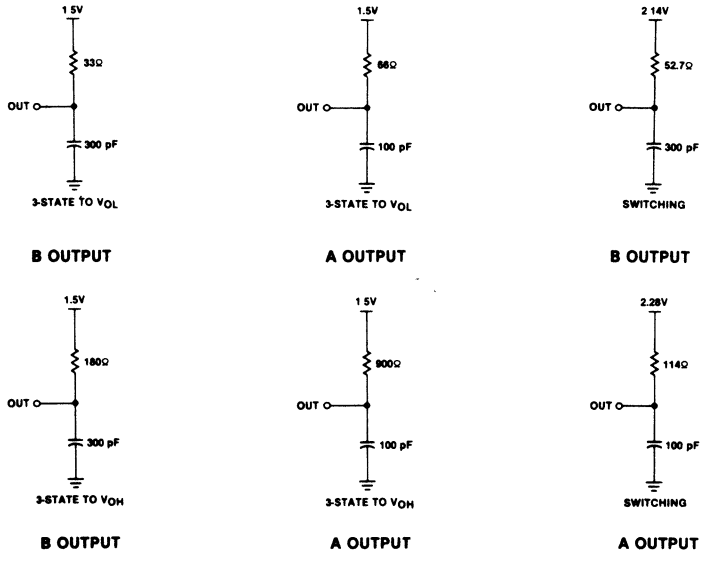
WAVEFORMS



TEST LOAD CIRCUITS



FUNCTIONAL DESCRIPTION

MOS microprocessors like the 8080/8085A/8086 are generally capable of driving a single TTL load. This also applies to MOS memory devices. While sufficient for minimum type small systems on a single PC board, it is usually necessary to buffer the microprocessor and memory signals when a system is expanded or signals go to other PC boards.
These octal bus transceivers are designed to do the necessary buffering.

Bi-Directional Driver

Each buffered line of the octal driver consists of two separate tri-state buffers. The B side of the driver is designed to drive 32 mA and interface the system side of the bus to I/O, memory, etc. The A side is connected to the microprocessor.

Control Gating, $\overline{OE}$, T

The $\overline{OE}$ (output enable) input is an active low signal used to enable the drivers selected by T on to the respective bus.

T is an input control signal used to select the direction of data through the transceivers. When T is high, data is transferred from the A_0-A_7 inputs to the B_0-B_7 outputs, and when low, data is transferred from B_0-B_7 to the A_0-A_7 outputs.

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPB8286C/87C
Cerdip, μPB8286D/87D

Notes

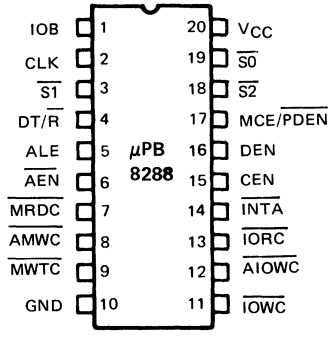
DESCRIPTION

The μPB8288 bus controller is for use in medium to large μPD8086/8088 systems. This 20-pin bipolar component provides command and control timing generation, plus bipolar drive capability and optimal system performance. It provides both Multibus™ command signals and control outputs for the microprocessor system. There is an option to use the controller with a multi-master system bus and separate I/O bus.

FEATURES

- System Controller for μPD8086/8088 Systems
- Bipolar Drive Capability
- Provides Advanced Commands
- Tri-State Output Drivers
- Can be used with an I/O Bus
- Enables Interface to One or Two Multi-Master Buses
- 20-Pin Package

PIN CONFIGURATION



PIN NAMES

S0-S2	Status Input Pins
CLK	Clock
ALE	Address Latch Enable
DEN	Data Enable
DT/R	Data Transmit/Receive
AEN	Address Enable
CEN	Command Enable
IOB	I/O Bus Mode
AIOWC	Advanced I/O Write
IOWC	I/O Write Command
IORC	I/O Read Command
AMWC	Advanced Memory Write
MWTC	Memory Write Command
MRDC	Memory Read Command
INTA	Interrupt Acknowledge
MCE/PDEN	Master Cascade/Peripheral Data Enable

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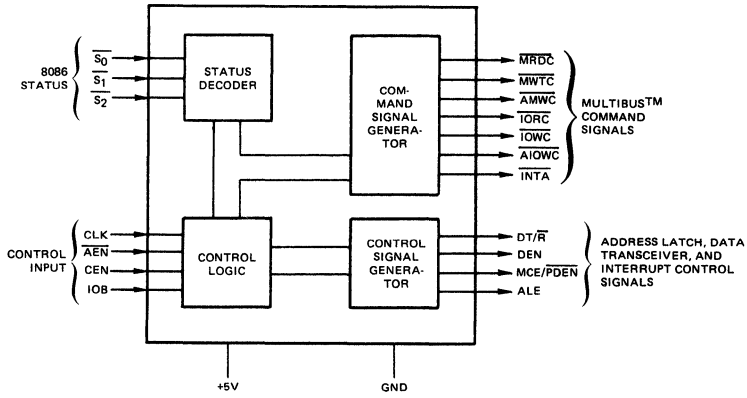
™ — Multibus is a trademark of Intel Corp.

REV/1

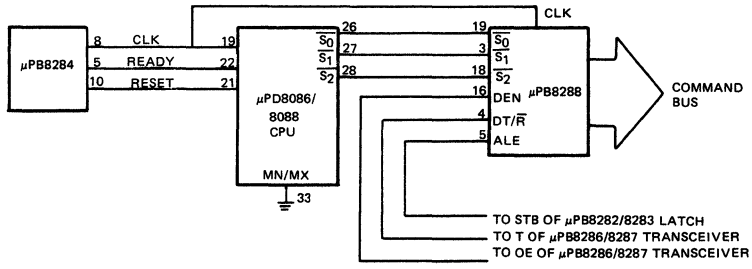
PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1	IOB	I/O Bus Mode	Sets mode of μPB8288, high for the I/O bus mode and low for the system bus mode.
2	CLK	Clock	The clock signal from the μPB8284 clock generator synchronizes the generation of command and control signals.
3, 19, 18	$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	Status Input Pins	The μPB8288 decodes these status lines from the μPB8086 to generate command and control signals. When not in use, these pins are high.
4	DT/$\overline{R}$	Data Transmit/Receive	This signal is used to control the bus transceivers in a system. A high for writing to I/O or memory and a low for reading data.
5	ALE	Address Latch Enable	This signal is used for controlling transparent D type latches (μPB8282/8283). It will strobe in the address on a high to low transition.
6	$\overline{AEN}$	Address Enable	In the I/O system bus mode, AEN enables the command outputs of the μPB8288 105 ns after it becomes active. If AEN is inactive, the command outputs are tri-stated.
7	$\overline{MRDC}$	Memory Read Command	This active low signal is for switching the data from memory to the data bus.
8	$\overline{AMWC}$	Advanced Memory Write Command	This is an advanced write command which occurs early in the machine cycle, with timing the same as the read command.
9	$\overline{MWTC}$	Memory Write Command	This is the memory write command to transfer data bus to memory, but not as early as $\overline{AMWC}$. (See timing waveforms.)
11	$\overline{IOWC}$	I/O Write Command	This command is for transferring information to I/O devices.
12	$\overline{AIOWC}$	Advanced I/O Write Command	This write command occurs earlier in the machine cycle than $\overline{IOWC}$.
13	$\overline{IORC}$	I/O Read Command	This signal enables the CPU to read data from an I/O device.
14	$\overline{INTA}$	Interrupt Acknowledge	This is to signal an interupting device to put the vector information on the data bus
15	CEN	Command Enable	This signal enables all command and control outputs. If CEN is low, these outputs are inactive.
16	DEN	Data Enable	This signal enables the data transceivers onto the bus.
17	MCE/$\overline{PDEN}$	Master Cascade Enable Peripheral Data Enable	Dual function pin system. MC/E – In the bus mode, this signal is active during an interrupt sequence to read the cascade address from the master interrupt controller onto the data bus. $\overline{PDEN}$ – In the I/O bus mode, it enables the transceivers for the I/O bus just as DEN enables bus transceivers in the system bus mode.

BLOCK DIAGRAM



CONNECTING THE BUS CONTROLLER TO THE CPU



ABSOLUTE MAXIMUM RATINGS*

OPERATING TEMPERATURE	0°C to 70°C
Storage Temperature	−65°C to +150°C
All Output and Supply Voltages ①	−0.5V to +7V
All Input Voltages ①	−1.0V to +5.5V

Note: ① With Respect to Ground.

$T_a = 25°C$

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device, This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

The three status lines ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) from the μPD8086 CPU are decoded by the command logic to determine which command is to be issued. The following chart shows the decoding:

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	μPD8086 State	μPB8288 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

There are two ways the command is issued depending on the mode of the μPB8288.

The I/O bus mode is enabled if the IOB pin is pulled high. In this mode, all I/O command lines are always enabled and not dependent upon $\overline{AEN}$. When the processor sends out an I/O command, the μPB8288 activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control any bus transceivers.

This mode is advantageous if I/O or peripherals dedicated to one microprocessor are in a multiprocessor system, allowing the μPB8288 to control two external buses. No waiting is required when the CPU needs access to the I/O bus, as an $\overline{AEN}$ low signal is needed to gain normal memory access.

If the IOB pin is tied to ground, the μPB8288 is in the system bus mode. In this mode, command signals are dependent upon the $\overline{AEN}$ line. Thus the command lines are activated 105 ns after the $\overline{AEN}$ line goes low. In this mode, there must be some bus arbitration logic to toggle the $\overline{AEN}$ line when the bus is free for use. Here, both memory and I/O are shared by more than one processor, over one bus, with both memory and I/O commands waiting for bus arbitration.

Among the command outputs are some advanced write commands which are initiated early in the machine cycle and can be used to prevent the CPU from entering unnecessary wait states.

The $\overline{INTA}$ signal acts as an I/O read during an interrupt cycle. This is to signal the interrupting device that its interrupt is being acknowledged, and to place the interrupt vector on the data bus.

The control outputs of the μPB8288 are used to control the bus transceivers in a system DT/$\overline{R}$ determines the direction of the data transfer, and $\overline{DEN}$ is used to enable the outputs of the transceiver. In the IOB mode the MCE/$\overline{PDEN}$ pin acts as a dedicated data enable signal for the I/O bus.

The MCE signal is used in conjunction with an interrupt acknowledge cycle to control the cascade address when more than one interrupt controller (such as a μPD8259A) is used. If there is only one interrupt controller in a system, MCE is not used as the $\overline{INTA}$ signal gates the interrupt vector onto the processor bus. In multiple interrupt controller systems, MCE is used to gate the μPD8259A's cascade address onto the processors local bus, where ALE strobes it into the address latches. This occurs during the first $\overline{INTA}$ cycle. During the second $\overline{INTA}$ cycle the addressed slave μPD8259A gates its interrupt vector onto the processor bus.

The ALE signal occurs during each machine cycle and is used to strobe data into the address latches and to strobe the status ($\overline{S0}$, $\overline{S1}$, $\overline{S2}$) into the μPB8288. ALE also occurs during a halt state to accomplish this.

The CEN (Command Enable) is used to control the command lines. If pulled high the μPB8288 functions normally and if grounded all command lines are inactive.

DC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

PARAMETER	SYMBOL	MIN	MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage	V_C		−1	V	I_C = −5 mA
Power Supply Current	I_{CC}		230	mA	
Forward Input Current	I_F		−0.7	mA	V_F = 0 45V
Reverse Input Current	I_R		50	μA	$V_R = V_{CC}$
Output Low Voltage — Command Outputs Control Outputs	V_{OL}		0.5 0.5	V V	I_{OL} = 32 mA I_{OL} = 16 mA
Output High Voltage — Command Outputs Control Outputs	V_{OH}	2 4 2.4		V V	I_{OH} = −5 mA I_{OH} = −1 mA
Input Low Voltage	V_{IL}		0.8	V	
Input High Voltage	V_{IH}	2.0		V	
Output Off Current	I_{OFF}		100	μA	V_{OFF} = 0.4 to 5.25V

AC CHARACTERISTICS

V_{CC} = 5V ± 10%, T_a = 0°C to 70°C

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
CLK Cycle Period	TCLCL	100		ns	
CLK Low Time	TCLCH	50		ns	
CLK High Time	TCHCL	30		ns	
Status Active Setup Time	TSVCH	35		ns	
Status Active Hold Time	TCHSV	10		ns	
Status Inactive Setup Time	TSHCL	35		ns	
Status Inactive Hold Time	TCLSH	10		ns	
Input Rise Time	T_{ILIH}		20	ns	
Input Fall Time	T_{IHIL}		12	ns	

TIMING RESPONSES

PARAMETER	SYMBOL	MIN	MAX	UNIT	LOADING
Control Active Delay	TCVNV	5	45	ns	
Control Inactive Delay	TCVNX	10	45	ns	
ALE MCE Active Delay (from CLK)	TCLLH, TCLMCH		20	ns	
ALE MCE Active Delay (from Status)	TSVLH, TSVMCH		20	ns	$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
ALE Inactive Delay	TCHLL	4	15	ns	
Command Active Delay	TCLML	10	35	ns	
Command Inactive Delay	TCLMH	10	35	ns	
Direction Control Active Delay	TCHDTL		50	ns	
Direction Control Inactive Delay	TCHDTH		30	ns	
Command Enable Time	TAELCH		40	ns	
Command Disable Time	TAEHCZ		40	ns	
Enable Delay Time	TAELCV	105	275	ns	Other: I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 80 pF
AEN to DEN	TAEVNV		20	ns	
CEN to DEN, PDEN	TCEVNV		25	ns	
CEN to Command	TCELRH		TCLML	ns	
Output Rise Time	T_{OLOH}		20	ns	
Output Fall Time	T_{OHOL}		12	ns	

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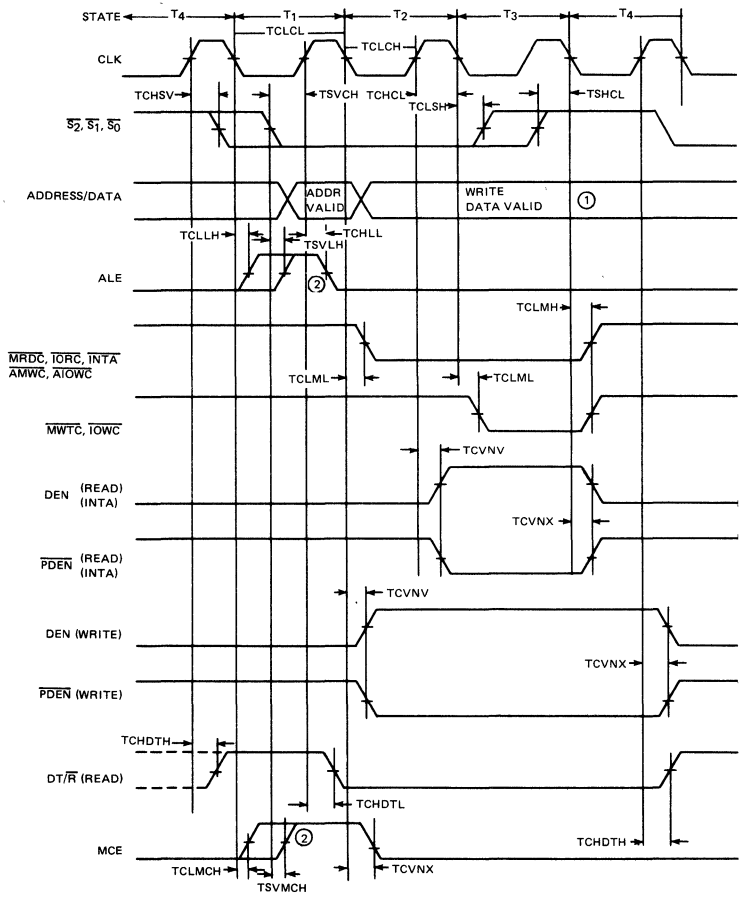
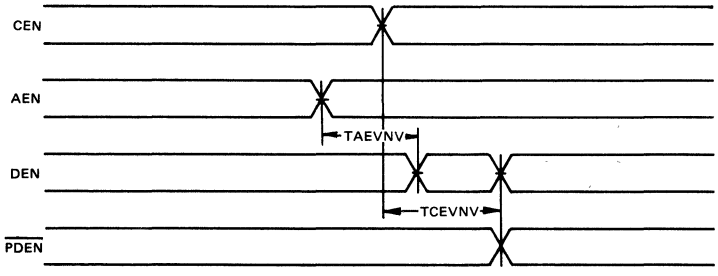
TIMING WAVEFORMS



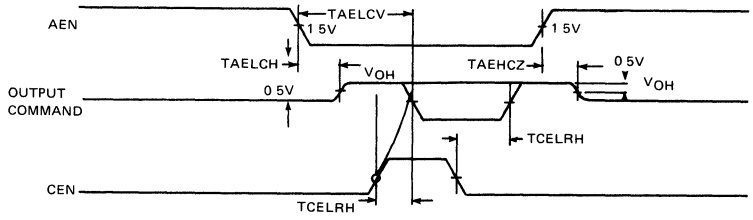
NOTES:

1. ADDRESS/DATA BUS IS SHOWN ONLY FOR REFERENCE PURPOSES
2. LEADING EDGE OF ALE AND MCE IS DETERMINED BY THE FALLING EDGE OF CLK OR STATUS GOING ACTIVE, WHICHEVER OCCURS LAST
3. ALL TIMING MEASUREMENTS ARE MADE AT 1 5V UNLESS SPECIFIED OTHERWISE

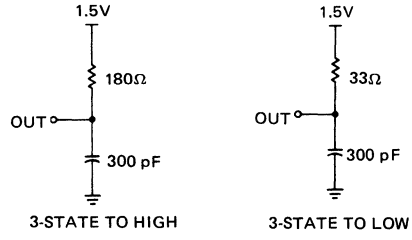
DEN, PDEN QUALIFICATION TIMING



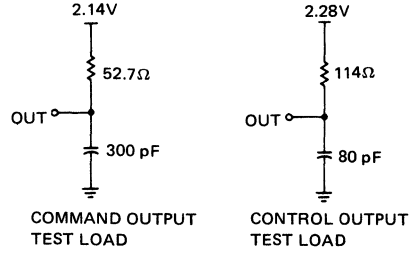
μPB8288 ADDRESS ENABLE ($\overline{AEN}$) TIMING (3-STATE ENABLE/DISABLE)



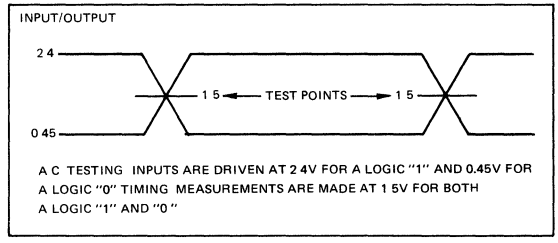
TEST LOAD CIRCUITS



3-STATE COMMAND OUTPUT TEST LOAD



AC TESTING INPUT, OUTPUT WAVEFORM



Package Outlines

For information, see Package Outline Section 7.

Cerdip, μPB8288D

Description

The μPB8289 Bus Arbiter is used with the μPD8288 Bus Controller to interface 8086 and 8088 microprocessors to a multimaster system bus. The μPD8289 controls the μPD8288 bus controller and the bus transceivers and address latches, preventing them from accessing the system bus if the processor does not have use of the bus.

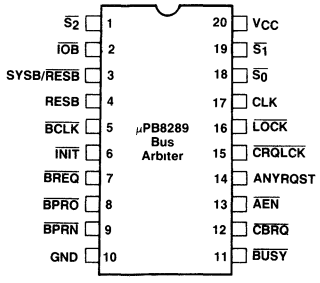
An external command sequence will cause the associated microprocessor to enter a wait state until the bus is ready. The processor remains in the wait state until the bus arbiter acquires use of the multimaster system bus. Then, the arbiter allows the bus controller, data transceivers, and address latches to access the system.

Once use of the bus has been acquired and data has been transferred, transfer acknowledge (XACK) is returned to the processor to indicate that the accessed slave device is ready. The processor may then complete its transfer cycle.

Features

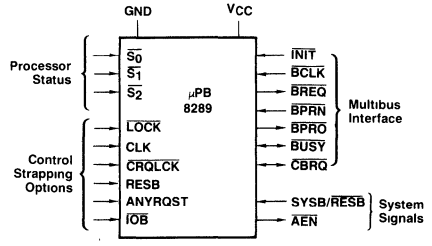
- ☐ Multimaster system bus protocol
- ☐ 8086 and 8088 processor synchronization with multimaster bus
- ☐ Simple interface with the 8288 bus controller and 8283/8282 address latches to a system bus
- ☐ Four operating modes for flexible system configuration
- ☐ Simplified interface to Multibus™ systems
- ☐ Parallel, Serial, and Rotating priority resolution
- ☐ Bipolar buffering and drive capability

Pin Configuration



TM: Multibus is a registered trademark of Intel Corporation.

Functional Configuration

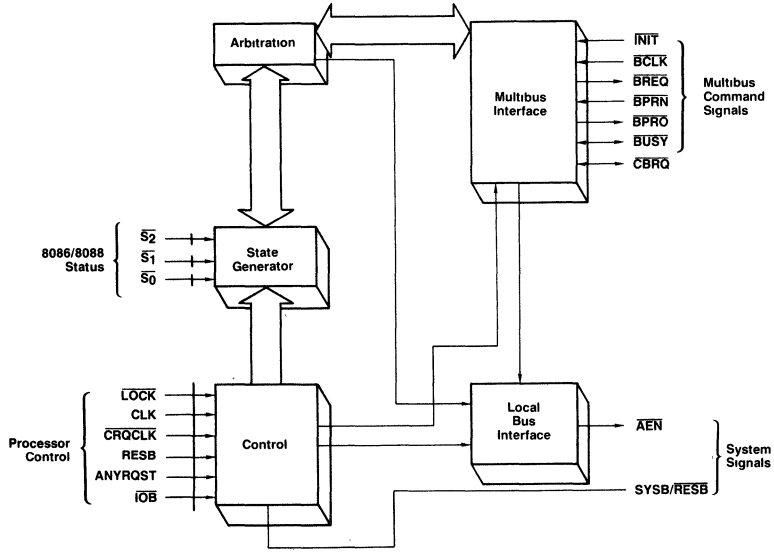


Pin Identification

Pin Number	Pin Name	Direction	Pin Functions
18, 19, 1	S0, S1, S2	IN	Status inputs from the 8086 or 8088 processor. The μPB8289 decodes them to begin bus requests and surrenders.
17	CLK	IN	Clock signal from the 8284 clock generator.
16	LOCK	IN	
15	CRQLCK	IN	Common Request Lock. Prevents the μPB8289 from surrendering the bus in response to request on the CBRQ input.
4	RESB	IN	Resident Bus Input. This signal tells the μPB8289 that there is a multimaster and resident bus. When this signal is high, the SYSB/RESB pin handles bus arbitration.
14	ANYRQST	IN	This signal allows the multimaster bus to be surrendered to a lower priority arbiter
2	IOB	IN	I/O Bus. This signal tells the μPB8289 that there is an I/O peripheral bus and a multimaster system bus.
13	AEN	OUT	Address Enable. This output tells the 8288 bus controller, 8284 clock driver, and the processor's address latches when to tri-state their output drivers.
3	SYSB/RESB	IN	System Bus/Resident Bus. This signal determines when bus requests and surrenders are permitted in SR mode.
12	CBRQ	IN/OUT	Common Bus Request. This is an input from a lower priority arbiter requesting the bus. It is an output from arbiters that surrender the multimaster bus upon request.
6	INIT	IN	Initialize. This is an active low input that resets all bus arbiters on the multimaster bus. No arbiters have use of the bus following INIT.
5	BCLK	IN	System Bus Clock. This clock synchronizes all system bus interface signals.
7	BREQ	OUT	Bus Request. This output is used by an arbiter to request use of the multimaster system bus.
9	BPRN	IN	Bus Priority In. This signal tells the arbiter it may acquire the bus on the next falling edge of BCLK.

6

Block Diagram



Pin Functions (Cont.)

Pin Number	Pin Name	Direction	Pin Functions
8	$\overline{BPRO}$	OUT	Bus Priority Out. In serial priority resolving schemes, this output daisy-chains to $\overline{BPRN}$ of the next lower priority arbiter.
11	$\overline{BUSY}$	IN/OUT	Busy notifies all arbiters on the bus when the bus is available. The highest requesting arbiter seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off the bus.
20	V_{CC}	IN	+5V
10	GND	IN	Ground

Bus Master Arbitration

Higher priority masters generally acquire use of the bus when a lower priority master completes its present transfer cycle. Lower priority masters acquire the bus when no higher priority master is accessing the system bus. The ANYRQST strapping option allows the arbiter to surrender the bus to a lower priority master as if it were a higher priority master. The arbiter maintains the bus as long as no other bus masters are requesting the bus and its processor has not entered the Halt state. The arbiter does not voluntarily surrender the bus and must be forced off by a request from another bus master, unless the arbiter's processor has entered the Halt state. Additional strapping options allow for other sets of conditions.

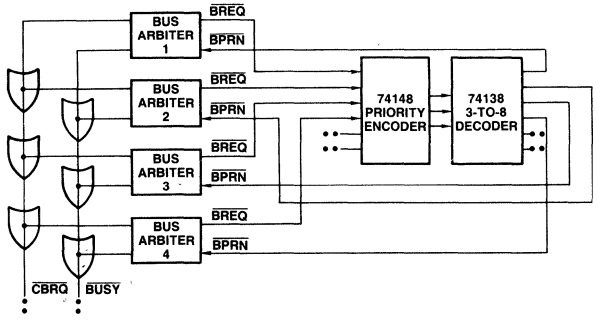
Priority Resolving Techniques

The μPB8289 provides several techniques for resolving priority between the many possible bus masters of a multimaster system bus. All of these techniques assume that one bus master will have priority over all others at any given time. You may use Parallel, Serial, or Rotating Priority Resolving.

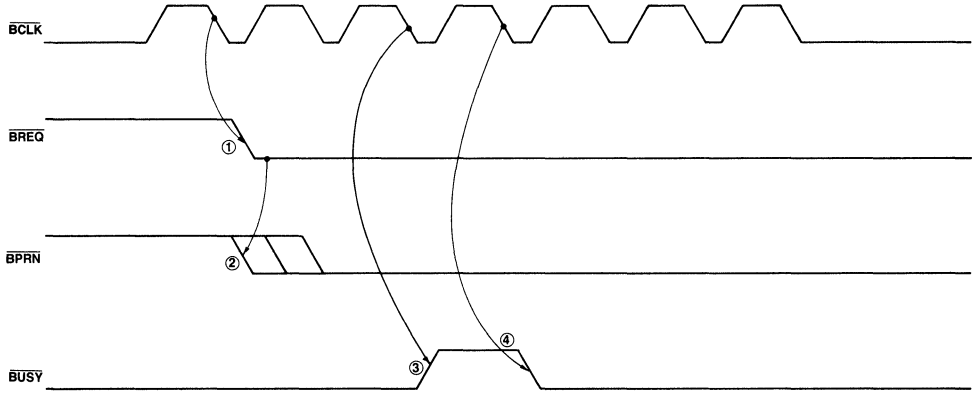
Parallel Priority Resolving

This technique uses a Bus Request line ($\overline{BREQ}$) for each arbiter on the multimaster system bus. Each $\overline{BREQ}$ line goes to a priority encoder that generates the address of the highest priority active $\overline{BREQ}$ line. This binary address is decoded to select the Bus Priority In line ($\overline{BPRN}$) that is returned to the highest priority active arbiter. The arbiter that receives priority ($\overline{BPRN}$ true) allows its bus master onto the multimaster system bus as soon as the bus becomes available. An arbiter that gets priority over another arbiter cannot immediately seize the bus, but must wait until the current bus transaction is complete. When the transaction is complete, the current occupant of the bus surrenders the bus by releasing $\overline{BUSY}$. $\overline{BUSY}$ is an active low OR tied line which goes to every arbiter on the system bus. When $\overline{BUSY}$ goes high (inactive), the priority arbiter seizes the bus and brings $\overline{BUSY}$ low to keep other arbiters off the bus. Note that all multimaster system bus transactions are synchronized to the bus clock ($\overline{BCLK}$).

Parallel Priority Resolving



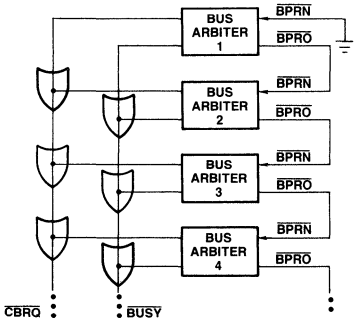
Higher Priority Arbiter Obtaining the Bus from a Lower Priority Arbiter



Notes:
① Higher priority arbiter requests the system bus.
② Attains priority.
③ Lower priority arbiter releases BUSY.
④ Higher priority arbiter then acquires the bus and pulls BUSY low.

Serial Priority Resolving

The serial priority resolving technique daisy-chains the bus arbiters together by connecting the higher priority arbiter's BPRO output to the BPRN of the next lowest priority arbiter. This eliminates the need for the priority encoder-decoder arrangement. The number of arbiters that may be daisy-chained together is a function of BCLK and the propagation delay from arbiter to arbiter. At 10 MHz, only 3 arbiters may be daisy-chained.



Rotating Priority Resolving

This technique resembles the parallel priority resolving technique except that priority is dynamically reassigned. The priority encoder is replaced by a circuit that rotates priority between arbiters to allow each arbiter an equal chance to use the system bus.

Modes of Operation

The μPB8289 has two basic operating modes: I/O Peripheral Bus mode (IOB mode), and Resident Bus mode (RESB mode). The IOB strapping option configures the μPB8289 into IOB mode and the RESB strapping option configures it to RESB mode. If both options are strapped false, the arbiter interfaces the processor to a multimaster system bus only. If both options are strapped true, the arbiter interfaces the processor to a multimaster system bus, a resident bus, and an I/O bus.

IOB Mode

IOB mode allows the processor to access both an I/O peripheral bus and a multimaster system bus. On an I/O peripheral bus, all devices on the bus, including memory, are treated as I/O devices and addressed by I/O commands. All memory commands are directed to the multimaster system bus. In IOB mode, the processor communicates with and controls peripherals over the peripheral bus and communicates with system memory over the system memory bus.

RESB Mode

RESB mode allows the processor to communicate over both a resident bus and a multimaster system bus. A resident bus can issue memory and I/O commands, but it is separate from the multimaster system bus. The resident bus has one master and is dedicated to only that master. The 8086 and 8088 can communicate with a resident bus and a multimaster system bus. The processor can access the memory and peripherals of both buses. Memory mapping selects which bus is accessed. The SYSB/RESB input on the arbiter instructs the arbiter on which bus to access. The signal connected to SYSB/RESB also enables and disables commands from one of the bus controllers.

Mode Summary

	Status Lines From 8086 or 8088 or 8089			IOB Mode Only	RESB (Mode) Only IOB = High RESB = High		IOB Mode RESB Mode IOB = Low RESB = High		Single Bus Mode IOB = High RESB = Low
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	$\overline{IOB}$ = Low	SYSB/$\overline{RESB}$ = High	SYSB/$\overline{RESB}$ = Low	SYSB/$\overline{RESB}$ = High	SYSB/$\overline{RESB}$ = Low	
	0	0	0	x	✓	x	x	x	✓
I/O Commands	0	0	1	x	✓	x	x	x	✓
	0	1	0	x	✓	x	x	x	✓
Halt	0	1	1	x	x	x	x	x	x
	1	0	0	✓	✓	x	✓	x	✓
Memory Commands	1	0	1	✓	✓	x	✓	x	✓
	1	1	0	✓	✓	x	✓	x	✓
Idle	1	1	1	x	x	x	x	x	x

Notes:

① x = Multimaster System Bus is allowed to be surrendered.

② ✓ = Multimaster System Bus is requested.

Multimaster System Bus

Mode	Pin Strapping	Requested ①	Surrendered ②
Single Bus Multimaster Mode	$\overline{IOB}$ = High RESB = Low	When the processor's status lines go active	HLT + TI • HPBRQ†
RESB Mode Only	$\overline{IOB}$ = High RESB = High	SYSB/$\overline{RESB}$ = High 2 Active	(SYSB/$\overline{RESB}$ = Low + TI) CBRQ + HLT + HPBRQ
IOB Mode Only	$\overline{IOB}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) • CBRQ + HLT + HPBRQ
IOB Mode • RESB Mode	$\overline{IOB}$ = Low RESB = High	(Memory Command) • (SYSB/$\overline{RESB}$ = High)	((I/O Status Commands) + (TI) (SYSB/$\overline{RESB}$ = Low) • CBRQ + HPBRQ† + HLT)

Notes:

① Except for HALT and Idle status.

② $\overline{LOCK}$ prevents surrender of bus to any other arbiter. $\overline{CRQLCK}$ prevents surrender of bus to a lower priority arbiter.

③ HLT = processor halt; $\overline{S}_2$–$\overline{S}_0$ = 011.

④ TI = processor idle; $\overline{S}_2$–$\overline{S}_0$ = 111.

⑤ + means OR.

⑥ • means AND.

† HPBRQ = higher priority bus request or $\overline{BPRN}$ = 1.

Absolute Maximum Ratings*

T_a = 25°C	
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin	−0.5V to +7V
All Input Voltages	−1.0V to +5.5V
Power Dissipation	1.5W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

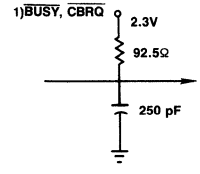
DC Characteristics

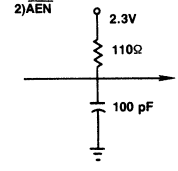
T_a = 0°C to +70°C; V_{CC} = 5V ±10%

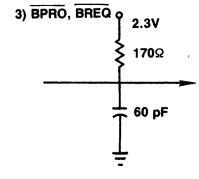
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input Clamp Voltage	V_C			−1.0	V	V_{CC} = 4.50V, I_C = −5 mA
Input Forward Current	I_F			−0.5	mA	V_{CC} = 5.50V, V_F = 0.45V
Reverse Input Leakage Current	I_R			60	μA	V_{CC} = 5.50V V_R = 5.50V
Output Low Voltage	V_{OL}					
$\overline{BUSY}$, $\overline{CBRQ}$				0.45	V	I_{OL} = 20 mA
$\overline{AEN}$				0.45	V	I_{OL} = 16 mA
$\overline{BPRO}$, $\overline{BREQ}$				0.45	V	I_{OL} = 10 mA
Output High Voltage	V_{OH}					
$\overline{BUSY}$, $\overline{CBRQ}$			Open Collector			
All Other Outputs		2.4			V	I_{OH} = 400 μA
Power Supply Current	I_{CC}			165	mA	

Capacitance

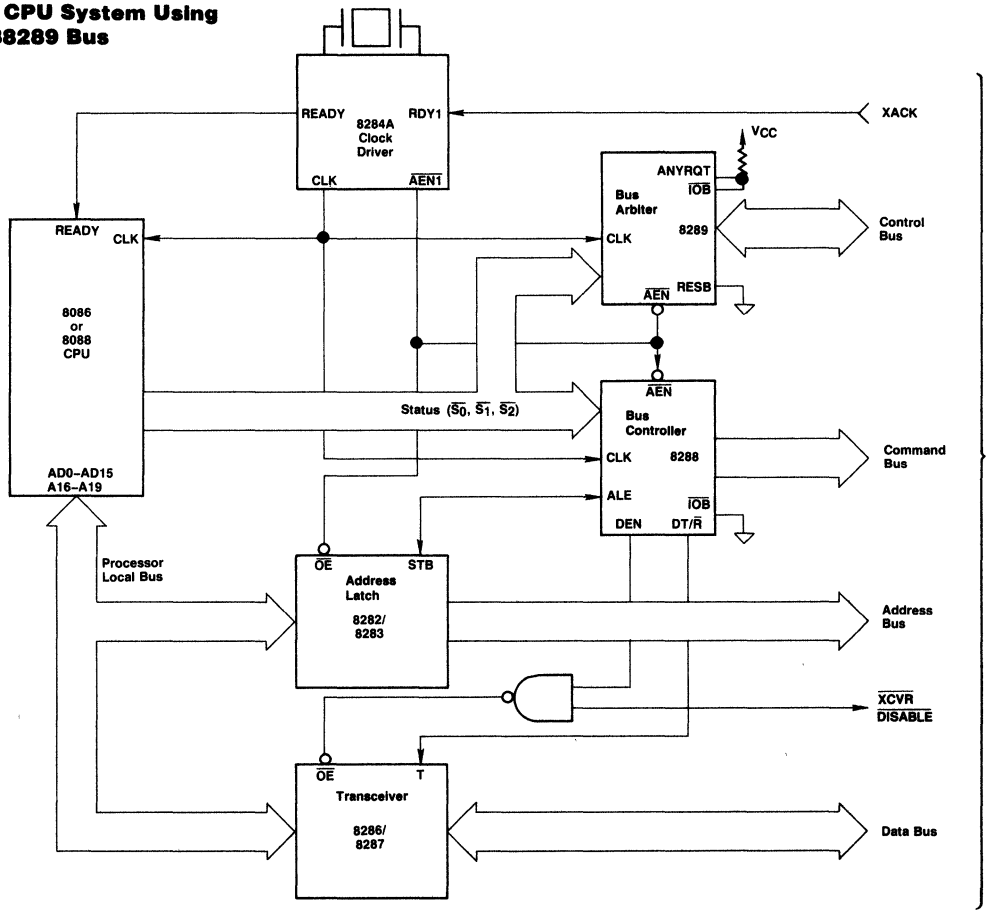
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin Status			25	pF	
Input Capacitance	Cin (Others)			12	pF	

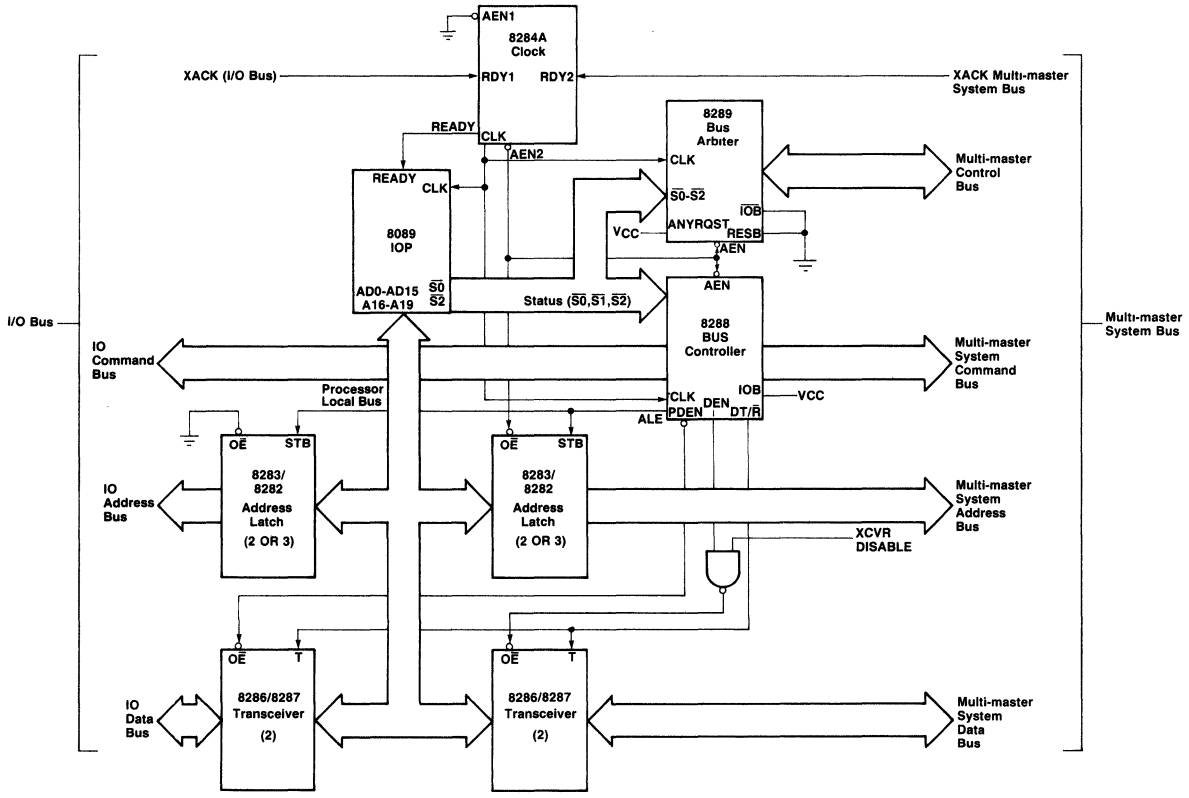




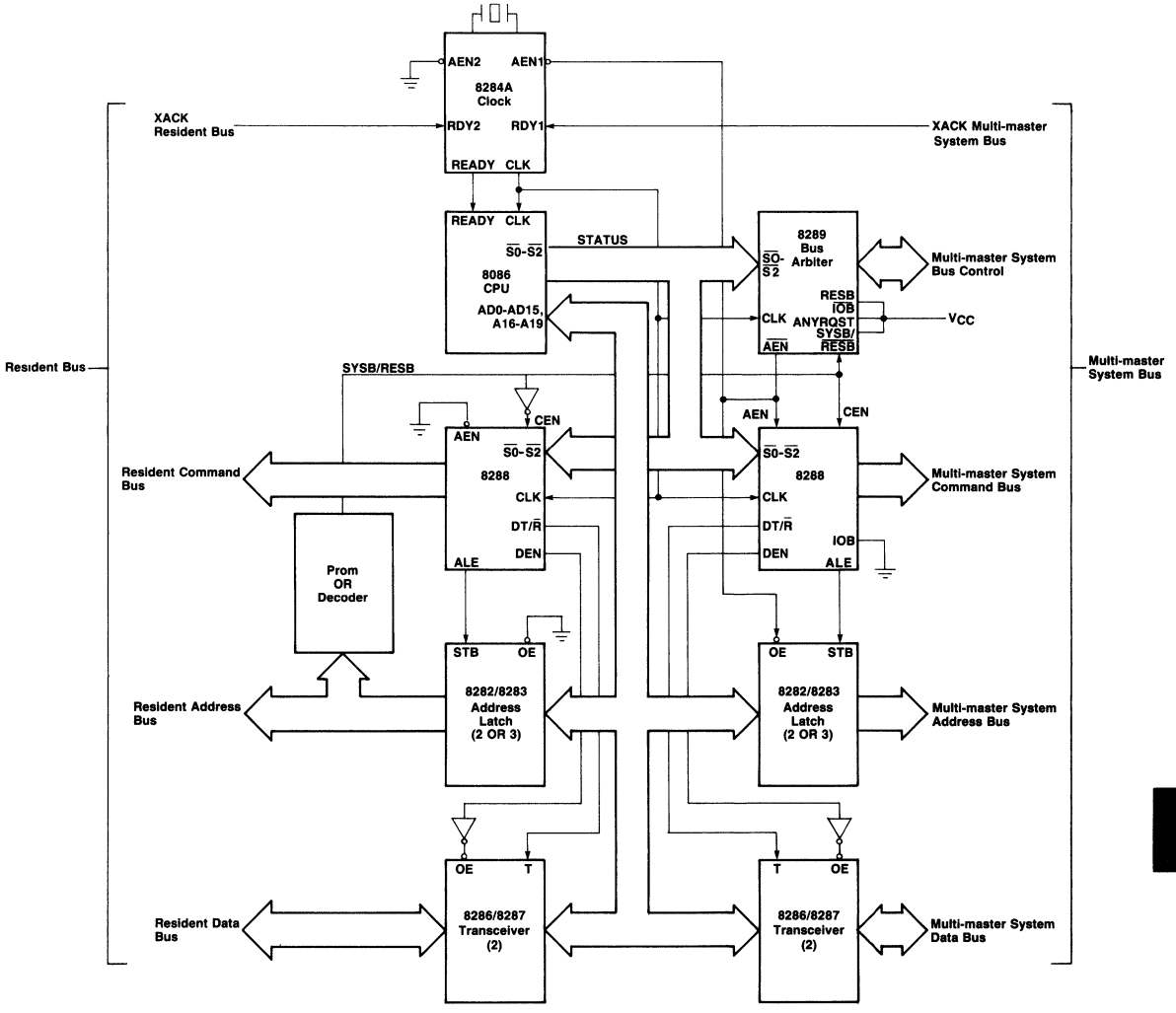


Typical CPU System Using the μPB8289 Bus Arbiter





TYPICAL 10B System



*By adding another 8289 arbiter and connecting its AEN to the 8288 whose AEN is presenty grounded, the processor could have access to two multi-master buses.

6

AC Characteristics
Timing Requirements

T_a = 0°C to +70°C; V_{CC} = 5V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CLK Cycle Period	t_{CLCL}	125			ns	
CLK Low Time	t_{CLCH}	65			ns	
CLK High Time	t_{CHCL}	35			ns	
Status Active Setup	t_{SVCH}	65		t_{CLCL}-10	ns	
Status Inactive Setup	t_{SHCL}	50		t_{CLCL}-10	ns	
Status Active Hold	t_{HVCH}	10			ns	
Status Inactive Hold	t_{HVCL}	10			ns	
$\overline{BUSY}$↑↓ Setup to $\overline{BCLK}$↓	t_{BYSBL}	20			ns	
$\overline{CBRQ}$↑↓ Setup to $\overline{BCLK}$↓	t_{CBSBL}	20			ns	
$\overline{BCLK}$ Cycle Time	t_{BLBL}	100			ns	
$\overline{BCLK}$ High Time	t_{BHCL}	30		0 65 (t_{BLBL})	ns	
$\overline{LOCK}$ Inactive Hold	t_{CLLL1}	10			ns	
$\overline{LOCK}$ Active Setup	t_{CLLL2}	40			ns	
$\overline{BPRN}$↓↑ to $\overline{BCLK}$ Setup Time	t_{PNBL}	15			ns	
SYSB/$\overline{RESB}$ Setup	t_{CLSR1}	0			ns	
SYSB/$\overline{RESB}$ Hold	t_{CLSR2}	20			ns	
Initialization Pulse Width	t_{IVIH}	3 t_{BLBL} + 3 t_{CLCL}			ns	
Input Rise Time	t_{ILIH}			20	ns	From 0.8V to 2.0V
Input Fall Time	t_{IHIL}			12	ns	From 2 0V to 0.8V

Timing Responses

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{BCLK}$ to $\overline{BREQ}$ Delay ①	t_{BLBRL}			35	ns	
$\overline{BCLK}$ to $\overline{BPRO}$ ①②	t_{BLPOH}			40	ns	
$\overline{BPRN}$↓↑ to $\overline{BPRO}$↓↑ Delay ①②	t_{PNPO}			25	ns	
$\overline{BCLK}$ to $\overline{BUSY}$ Low	t_{BLBYL}			60	ns	
$\overline{BCLK}$ to $\overline{BUSY}$ Float ③	t_{BLBYH}			35	ns	
CLK to $\overline{AEN}$ High	t_{CLAEH}			65	ns	
$\overline{BCLK}$ to $\overline{AEN}$ Low	t_{BLAEL}			40	ns	
$\overline{BCLK}$ to $\overline{CBRQ}$ Low	t_{BLCBL}			60	ns	
$\overline{BCLK}$ to $\overline{CBRQ}$ Float ③	t_{RLCRH}			35	ns	
Output Rise Time	t_{OLOH}			20	ns	From 0.8V to 2.0V
Output Fall Time	t_{OHOL}			12	ns	From 2.0V to 0.8V

Notes:

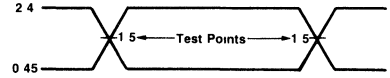
① Denotes that the spec applies to both transitions of the signal.

② $\overline{BCLK}$ generates the first $\overline{BPRO}$. Subsequent changes of $\overline{BPRO}$ are generated through BPRON

③ Measured at 0.5V above GND

AC Test Condition Waveform

Input/Output

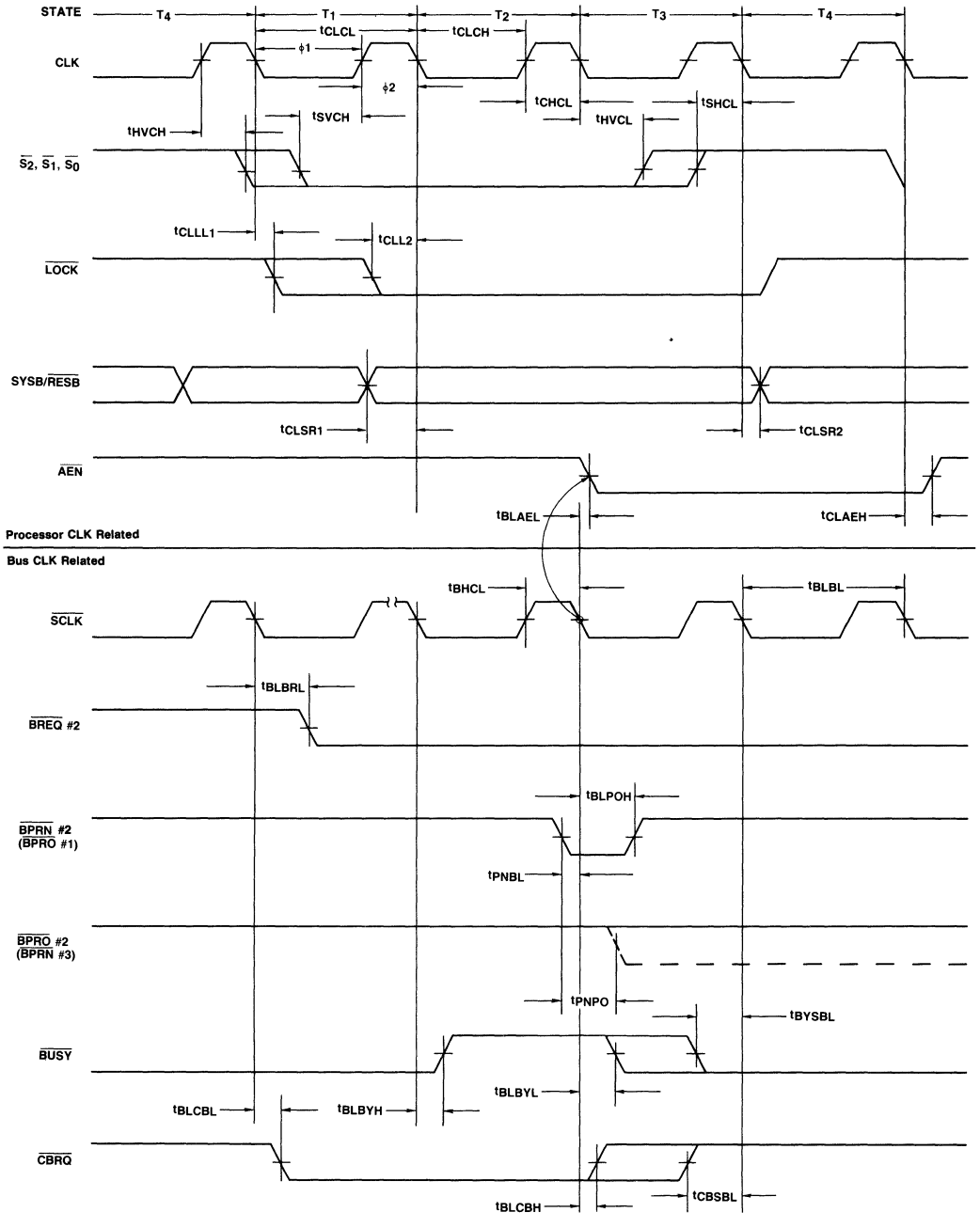


AC Testing inputs are driven at 2.4V for LOGIC 1 and 0.45V for LOGIC 0. The clock is driven at 4.3V and 0.25 Timing measurements are made at 1.5V for LOGIC 1 and 0.

Timing Waveforms

The signals related to CLK are typical processor signals and do not relate to the depicted sequence of events of the signals referenced to $\overline{BCLK}$. The signals shown related to the $\overline{BCLK}$ represent a hypothetical sequence of events for illustration. Assume three bus arbiters of priorities 1, 2, and 3 configured in the serial priority resolving scheme. Assume arbiter 1 has the bus and is holding $\overline{BUSY}$ low. Arbiter 2 detects its processor wants the bus and pulls $\overline{BREQ}$ #2 low. If $\overline{BPRN}$ #2 is high (as shown), arbiter 2 pulls $\overline{CBRQ}$ low. $\overline{CBRQ}$ signals to higher priority arbiter 1 that a lower priority arbiter wants the bus. A higher priority arbiter would be given $\overline{BPRN}$ when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{CBRQ}$. Arbiter 1 relinquishes the multimaster system bus when it enters a state of not requiring it, by lowering its $\overline{BPRO}$ #1 (tied to $\overline{BPRN}$ #2) and releasing $\overline{BUSY}$. Arbiter 2 now sees that it has priority from $\overline{BPRN}$ #2 being low and releases $\overline{CBRQ}$. As soon as $\overline{BUSY}$ signifies the bus is available (high), arbiter 2 pulls $\overline{BUSY}$ low on the next falling edge of $\overline{BCLK}$. Note that if arbiter 2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority by lowering its $\overline{BPRO}$ #2 (TPNPO). Note also that even a higher priority aribiter which is acquiring the bus through $\overline{BPRN}$ will momentarily drop $\overline{CBRQ}$ until it has acquired the bus.

Timing Waveforms



6

Package Outlines

For information, see Package Outline Section 7.

Cerdip, μPB8289D

16,384-BIT ROM WITH I/O PORTS
*16,384-BIT EPROM WITH I/O PORTS

DESCRIPTION

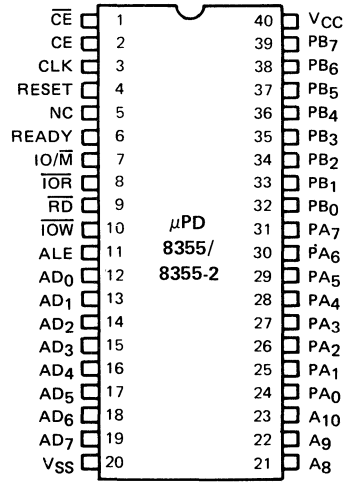
The μPD8355 and the μPD8755A are μPD8085A Family components. The μPD8355 contains 2048 x 8 bits of mask ROM and the μPD8755A contains 2048 x 8 bits of mask EPROM for program development. Both components also contain two general purpose 8-bit I/O ports. They are housed in 40 pin packages, are designed to directly interface to the μPD8085A, and are pin-for-pin compatible with each other.

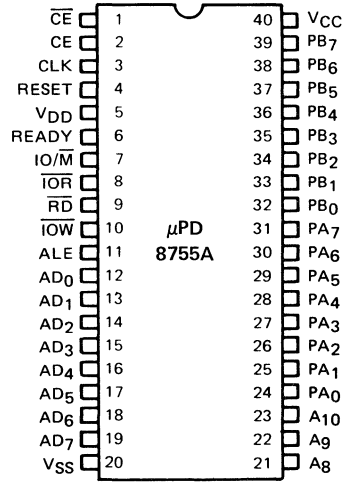
FEATURES

- 2048 X 8 Bits Mask ROM (μPD8355 and μPD8355-2)
- 2048 X 8 Bits Mask EPROM (μPD8755A)
- 2 Programmable I/O Ports
- Single Power Supplies: +5V
- Directly Interfaces to the μPD8085A
- Pin for Pin Compatible
- μPD8755A: UV Erasable and Electrically Programmable
- μPD8335 and μPD8355-2 Available in Plastic Package
- μPD8755A Available in Ceramic Package

6

PIN CONFIGURATIONS





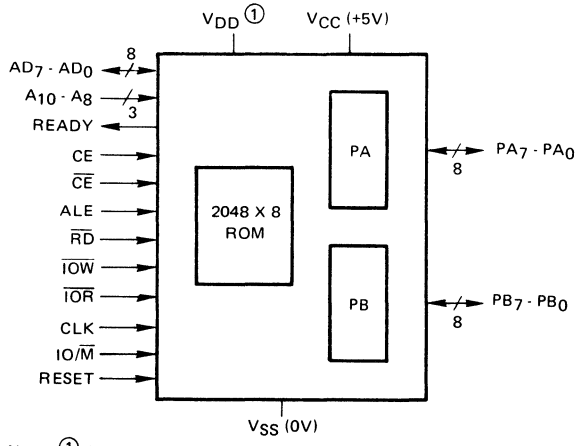
NC: Not Connected

FUNCTIONAL DESCRIPTION

The μPD8355 and μPD8755A contain 16,384 bits of mask ROM and EPROM respectively, organized as 2048 X 8. The 2048 word memory location may be selected anywhere within the 64K memory space by using the upper 5 bits of address from the μPD8085A as a chip select.

The two general purpose I/O ports may be programmed input or output at any time. Upon power up, they will be reset to the input mode.

BLOCK DIAGRAM



Note ① V_{DD} applies to μPD8755A only.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature (μPD8355) . . . . . 0°C to +70°C
(μPD8755A) . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin (μPD8355) . . . . . −0.5 to +7V ①
(μPD8755A) . . . . . −0.5 to +7V ①
Power Dissipation 1.5W

Note: ① With Respect to Ground

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5	0.8	V	V_{CC} = 5.0V ①
Input High Voltage	V_{IH}	2.0	V_{CC}+0.5	V	V_{CC} = 5.0V ①
Output Low Voltage	V_{OL}		0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −400 μA
Input Leakage	I_{IL}		10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LO}		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current	I_{CC}		180/125	mA	μPD8355/8355-2

Note: ① These conditions apply to μPD8355/μPD8355-2 only.

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1,2	$\overline{CE}$, CE	Chip Enables	Enable Chip activity for memory or I/O
3	CLK	Clock Input	Used to Synchronize Ready
4	Reset	Reset Input	Resets PA and PB to all inputs
5 ①	NC	Not Connected	
5 ②	V_{DD}	Programming Voltage	Used as a programming voltage, tied to +5V normally
6	Ready	Ready Output	A tri-state output which is active during data direction register loading
7	IO/$\overline{M}$	I/O or Memory Indicator	An input signal which is used to indicate I/O or memory activity
8	IOR	I/O Read	I/O Read Strobe In
9	$\overline{RD}$	Memory Read	Memory Read Strobe In
10	$\overline{IOW}$	I/O Write	I/O Write Strobe In
11	ALE	Address Low Enable	Indicates information on Address/Data lines is valid
12-19	AD_0-AD_7	Low Address/Data Bus	Multiplexed Low Address and Data Bus
20	V_{SS}	Ground	Ground Reference
21-23	A_8-A_{10}	High Address	High Address inputs for ROM reading
24-31	PA_0-PA_7	Port A	General Purpose I/O Port
32-39	PB_0-PB_7	Port B	General Purpose I/O Port
40	V_{CC}	5V Input	Power Supply

Notes: ① μPD8355
② μPD8755A

I/O PORTS

I/O port activity is controlled by performing I/O reads and writes to selected I/O port numbers. Any activity to and from the μPD8355 requires the chip enables to be active. This can be accomplished with no external decoding for multiple devices by utilizing the upper address lines for chip selects. ① Port activity is controlled by the following I/O addresses:

AD_1	AD_0	PORT SELECTED	FUNCTION
0	0	A	Read or Write PA
0	1	B	Read or Write PB
1	0	A	Write PA Data Direction
1	1	B	Write PB Data Direction

Since the data direction registers for PA and PB are each 8-bits, any pin on PA or PB may be programmed as input or output (0 = in, 1 = out).

Note: ① During ALE time the data/address lines are duplicated on A_{15}-A_8.

AC CHARACTERISTICS

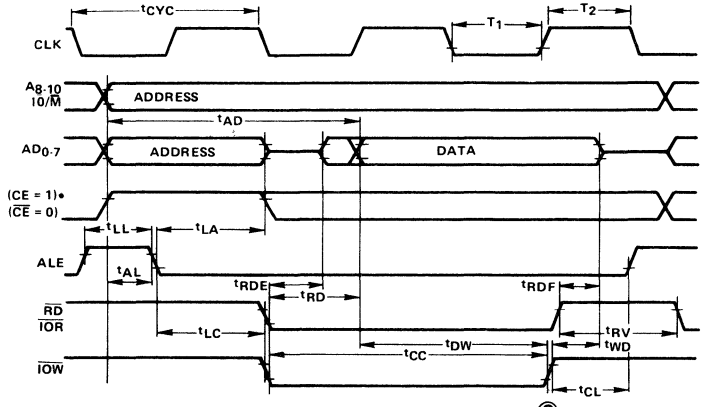
T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

Symbol	Parameter	8355 Min	8355 Max.	8355-2 Min.	8355-2 Max	Unit	Test Conditions
t_{CYC}	Clock Cycle Time	320		200		ns	C_{LOAD} = 150 pF
T_1	CLK Pulse Width	80		40		ns	
T_2	CLK Pulse Width	120		70		ns	
t_f, t_r	CLK Rise and Fall Time		30		30	ns	
t_{AL}	Address to Latch Set Up Time	50		30		ns	150 pF Load
t_{LA}	Address Hold Time after Latch	80		30		ns	
t_{LC}	Latch to READ/WRITE Control	100		40		ns	
t_{RD}	Valid Data Out Dealy from READ Control		170		140	ns	
t_{AD}	Address Stable to Data Out Valid		400		330	ns	
t_{LL}	Latch Enable Width	100		70		ns	
t_{RDF}	Data Bus Float after READ	0	100	0	85	ns	
t_{CL}	READ/WRITE Control to Latch Enable	20		10		ns	
t_{CC}	READ/WRITE Control Width	250		200		ns	
t_{DW}	Data in to Write Set Up Time	150		150		ns	
t_{WD}	Data in Hold Time After WRITE	10		10		ns	
t_{WP}	WRITE to Port Output		400		400	ns	
t_{PR}	Port Input Set Up Time	50		50		ns	
t_{RP}	Port Input Hold Time	50		50		ns	
t_{RYH}	READY HOLD Time	0	160	0	160	ns	
t_{ARY}	ADDRESS (CE) to READY		160		160	ns	
t_{RV}	Recovery Time Between Controls	300		200		ns	
t_{RDE}	READ Control to Data Bus Enable	10		10		ns	

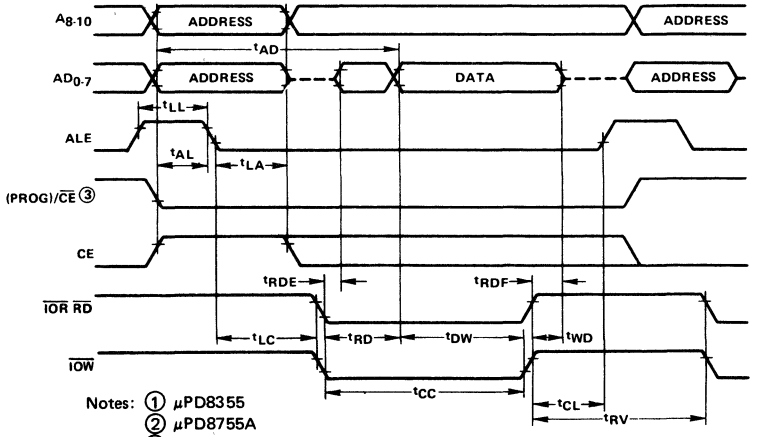
Notes 30 ns for μPD8755A
C_{LOAD} = 150 pF

TIMING WAVEFORMS

ROM READ, I/O READ AND WRITE ①



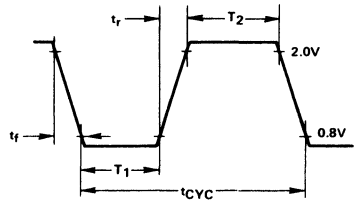
PROM READ, I/O READ AND WRITE ②



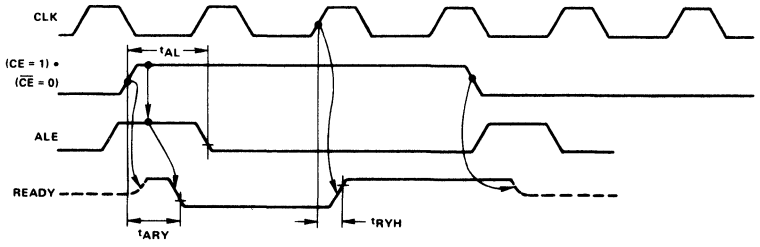
Notes: ① μPD8355
② μPD8755A
③ CE must remain low for the entire cycle

TIMING WAVEFORMS (CONT.)

CLOCK

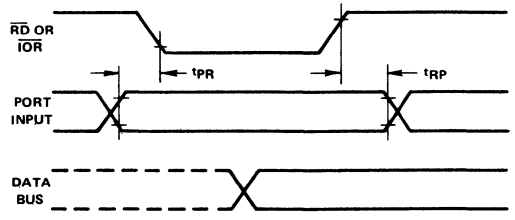


WAIT STATE TIMING (READY = 0)

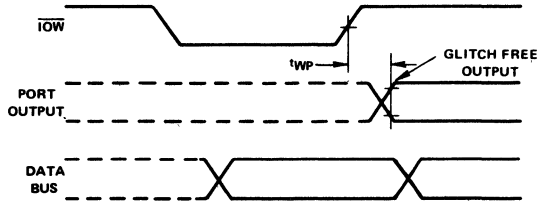


I/O PORT

INPUT MODE



OUTPUT MODE



EPROM PROGRAMMING μPD8755A

Erasure of the μPD8755A occurs when exposed to ultraviolet light sources of wavelengths less than 4000 Å. It is recommended, if the device is exposed to room fluorescent lighting or direct sunlight, that opaque labels be placed over the window to prevent exposure. To erase, expose the device to ultraviolet light at 2537 Å at a minimum of 15 W-sec/cm^2 (intensity X expose time). After erasure, all bits are in the logic 1 state. Logic 0's must be selectively programmed into the desired locations. It is recommended that NEC's PROM programmer be used for this application.

6

Package Outlines

For information, see Package Outline Section 7.

Plastic, μPD8355HC/8755AC
Ceramic, μPD8355D
Ceramic, μPD8355HD
Ceramic, μPD8755AD
Cerdip, μPD8755AD, has quartz window

NEC

PACKAGE OUTLINES 7

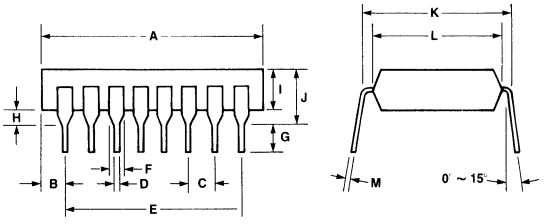
All packaging information is contained in this Package Outlines section. Specifications and dimensions for every package are shown together with a list of the products available in each. Additions, changes, and updates will be incorporated in succeeding editions of the catalog.

16 PIN

Plastic

μPB8216C/26C

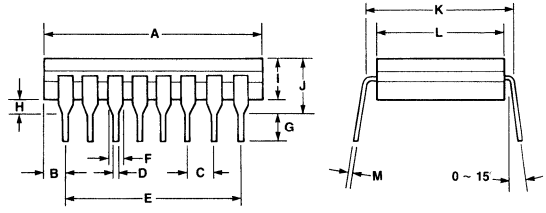
Item	Millimeters	Inches
A	19.4 max	0.76 max
B	0.81	0.03
C	2.54	0.10
D	0.5	0 02
E	17.78	0.70
F	1.3	0.051
G	2.54 min	0.10 min
H	0.5 min	0 02 min
I	4.05 max	0.16 max
J	4.55 max	0 18 max
K	7.62	0.30
L	6.4	0 25
M	$0.25^{+0\ 10}_{-0.05}$	0.01



Cerdip

μPB8216D/26D

Item	Millimeters	Inches
A	19.9 max	0.784 max
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 min	0.10 min
H	0.5 min	0.019 min
I	4.58 max	0.181 max
J	5.08 max	0.20 max
K	7.62	0.30
L	6.4	0.25
M	$0\ 25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

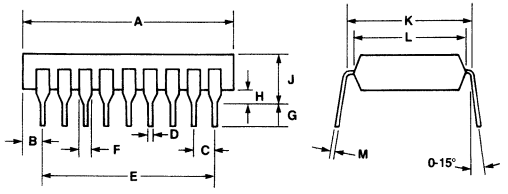


18 PIN

Plastic

μPD8284AC

Item	Millimeters	Inches
A	23.2 max	0.91 max
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.5	0.059
G	2.5 min	0.1 min
H	0 5 min	0.02 min
I	4.6 max	0.18 max
J	5.1 max	0.2 max
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01



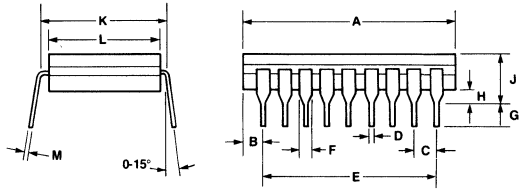
7

PACKAGE OUTLINES

18 PIN (Cont.)

Cerdip

μPB8284AD

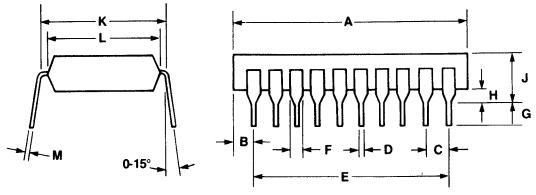


Item	Millimeters	Inches
A	23.2 max	0.91 max
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 min	0.1 min
H	0.5 min	0.02 min
I	4.6 max	0.18 max
J	5.1 max	0.2 max
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

20 PIN

Plastic

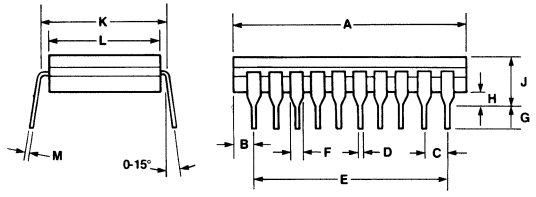
μPB8282C/83C
μPB8286C/87C



Item	Millimeters	Inches
A	26.7 max	1.05 max
B	1.05	0.041
C	2.54	0.1
D	0.5 - 0.1	0.02 - 0.004
E	22.86	0.9
F	1.4	0.055
G	2.54 min	0.1 min
H	0.5 min	0.02 min
I	3.55	0.14
J	5.08 max	0 2 max
K	7.62	0.3
L	6.4	0.25
M	0.25 - 0.10 - 0.05	0.01 - 0.004 - 0.002

Cerdip

μPB8282D/83D
μPB8286D/87D
μPB8288D
μPB8289D

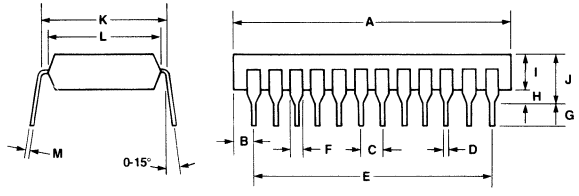


Item	Millimeters	Inches
A	26.7 max	1.05 max
B	0.7	0.028
C	2.54	0.1
D	0.46 ± 0.1	0.018 ± 0.004
E	22.86	0.9
F	1.4	0.055
G	2.54 min	0.1 min
H	0.5 min	0.02 min
I	4.32 max	0.17 max
J	5.08 max	0.2 max
K	7.62	0.3
L	6.8	0.27
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

24 PIN

Plastic

μPB8212C
μPD8243C
μPD82C43C
μPD8253C-5



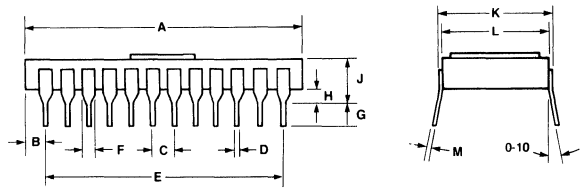
Item	Millimeters	Inches
A	33 max	1.3 max
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 min	0.1 min
H	0.5 min	0.02 min
I	5.22 max	0.205 max
J	5.72 max	0.225 max
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

24 PIN (Cont.)

Ceramic

μPD8243D
μPD8253D-5

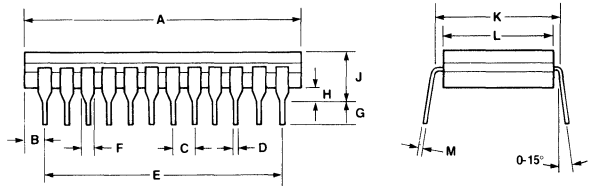
Item	Millimeters	Inches
A	30.78 max	1.21 max
B	1.53 max	0.06 max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94 ± 0.1	1.10 ± 0.004
F	1.02 min	0.04 min
G	3.2 min	0.13 min
H	1.02 min	0.04 min
I	3.23 max	0.13 max
J	4.25 max	0.17 max
K	15.24 typ	0.60 typ
L	14.93 typ	0.59 typ
M	0.25 ± 0.05	0.010 ± 0.002



Cerdip

μPB8212D
μPD8243D
μPD82C43D
μPD8253D-5

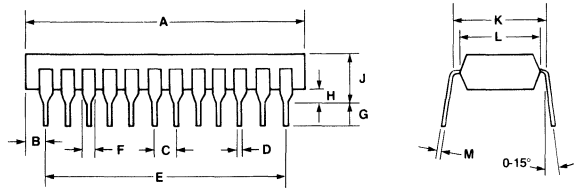
Item	Millimeters	Inches
A	33.5 max	1.32 max
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 min	0.1 min
H	0.5 min	0.019 min
I	4.58 max	0.181 max
J	5.08 max	0.2 max
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



Plastic Skinnydip

μPD82C43CX

Item	Millimeters	Inches
A	33 max	1.3 max
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 min	0.1 min
H	0.5 min	0.02 min
I	5.22 max	0.205 max
J	5.72 max	0.225 max
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

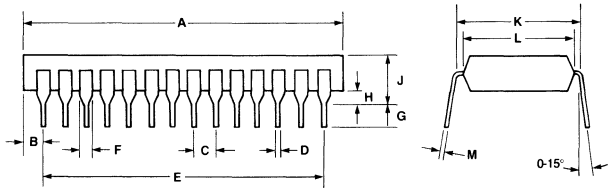


28 PIN

Plastic

μCOM-4C
μPD557LC
μPD550C/554C
μPD550LC/554LC
μPD7506C
μPD7507SC
μPD7520C
μPD8021C
μPD8251AC/AFC
μPD8259AC

Item	Millimeters	Inches
A	38.0 max	1.496 max
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 min	0.10 min
H	0.5 min	0.02 min
I	5.22 max	0.205 max
J	5.72 max	0.225 max
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



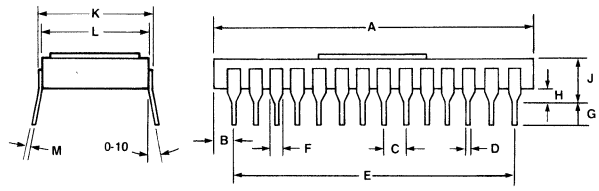
7

PACKAGE OUTLINES

28 PIN (Cont.)

Ceramic

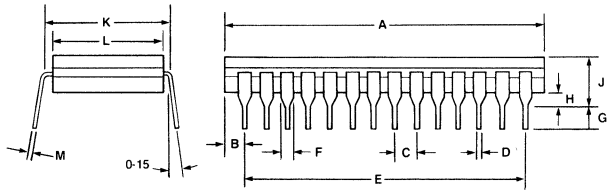
μPD7720D
μPD77P20D*
μPD8251AD/AFD
*has quartz window



Item	Millimeters	Inches
A	36.2 max	1.43 max
B	1.59 max	0.06 max
C	2.54 ± 0.1	0.1 ± 0.004
D	0.46 ± 0.01	0.02 ± 0.004
E	33.02 ± 0.1	1.3 ± 0.004
F	1.02 min	0.04 min
G	3.2 min	0.13 min
H	1.0 min	0.04 min
I	3.5 max	0.14 max
J	4.5 max	0.18 max
K	15.24 typ	0.6 typ
L	14.93 typ	0.59 typ
M	0.25 ± 0.05	0.01 ± 0.002

Cerdip

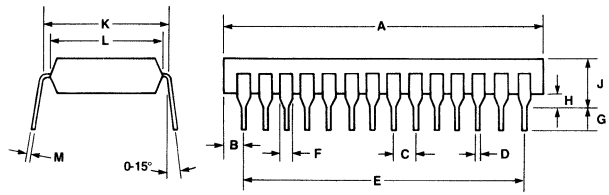
μPD8021D
μPD8251AD/AFD
μPD8259AD



Item	Millimeters	Inches
A	37.7 max	1.48 max
B	2.78	1.1
C	2.54	0.1
D	0.46 ± 0.10	0.018 ± 0.004
E	27.94	1.10
F	1.3	0.05
G	2.54 min	0.1 min
H	0.5 min	0.020
I	5.0 max	0.20
J	5.5 max	0.216
K	15.24	0.60
L	14.66	0.58
M	0.25 ± 0.05	0.010 ± 0.002

Plastic Shrinkdip

μPD7506CT
μPD7520CT
μPD7507SCT
μPD554CT
μPD550CT
μPD557LCT

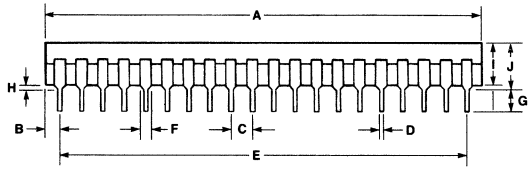


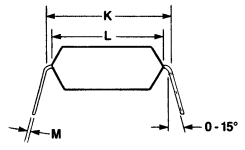
Item	Millimeters	Inches
A	15.95 max	.628 max
C	1.778	.07
D	0.5	.02
E	24.89	.98
F	1.1	.043
G	2.54	.1
H	.51 min	.02 min
J	5.08 max	.2 max
K	15.24	.600
L	13.2	.52
M	$0.25^{+0.10}_{-0.05}$	$.01^{+.004}_{-.002}$

40 PIN

Plastic

μPD7507C/08C
μPD7508AC
μPD7508HC
μPD8041AC
μPD8048HC/35HLC
μPD80C35C/C48C
μPD8049HC/39HLC
μPD80C49C/C39C
μPD780C
μPD8085AC/AHC
μPD765AC/7265C
μPD7201AC
μPD7210C
μPD7751C
μPD8155C/56C
μPD8237C-5
μPD8255AC-5
μPD8257C-5
μPD8279C-5
μPD8355HC/8755AC

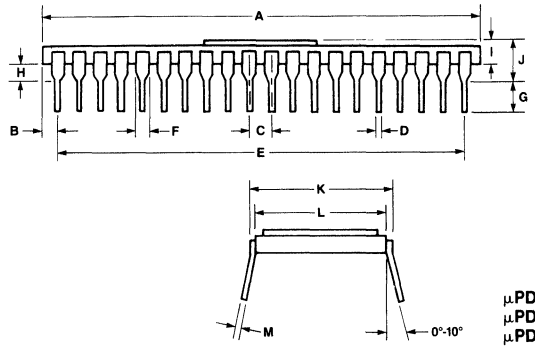




Item	Millimeters	Inches
A	51.5 max	2.028 max
B	1.62 max	0.064 max
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.2 min	0.047 min
G	2.54 min	0.10 min
H	0.5 min	0.019 min
I	5.22 max	0.206 max
J	5.72 max	0.225 max
K	15.24 typ	0.600 typ
L	13.2 typ	0.520 typ
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

40 PIN (Cont.)

Item	Millimeters	Inches
A	51.5 max	2.03 max
B	1.62 max	0.06 max
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 min	0.04 min
G	3.2 min	0.13 min
H	1.0 min	0.04 min
I	3.5 max	0.14 max
J	4.5 max	0.18 max
K	15.24 typ	0.6 typ
L	14.93 typ	0.59 typ
M	0.25 ± 0.05	0.01 ± 0.0019

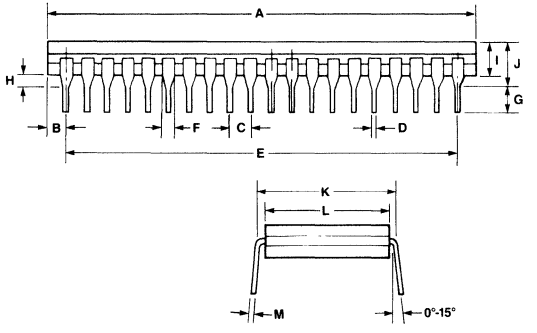


μPD8279D-5
μPD8355D
μPD8355HD

Ceramic

μPD8041AD
μPD8048HD/35HLD
μPD80C35D/C48D
μPD8049HD/39HLD
μPD780D
μPD8085AD
μPD765AD/7265D
μPD7201AD
μPD7210D
μPD7220D
μPD7261D
μPD8237D-5
μPD8255AD-5
μPD8755AD
μPD8155D/56D
μPD8257D-5

Item	Millimeters	Inches
A	53.34 max	2.1 max
B	13.2	.52
C	2.54 ± 0.25	.1 ± .01
D	0.5 ± 0.1	.002 ± .004
E	48.56	1.91
F	1.3	.051
G	0.51 min	.02 min
H	7.62	.3
J	5.08 max	.2 max
K	15.24	.6
M	0.25 ± 0.05	.01 ± .002

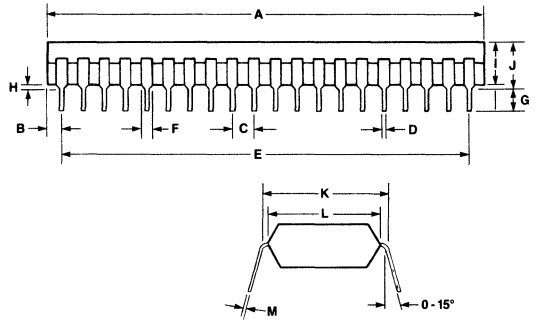


Cerdip

μPD8086D
μPD8088D
μPD8085AD
μPD8237D-5
μPD8085AHD
μPD8741AD*
μPD8748D*
μPD8749HD*
μPD8755AD*

*has quartz window

Item	Millimeters	Inches
A	39 max	1.54 max
C	1.778	.07
D	0.5	.02
E	35.56	1.4
F	1.1	.043
G	2.54	.1
H	.51 min	.02 min
J	5.08 max	.2 max
K	15.24	.600
L	13.2	.52
M	0.25 $^{+0.10}_{-0.05}$	.01 $^{+.004}_{-.002}$



Plastic Shrinkdip

μPD7507CU
μPD7508CU
μPD7508ACU
μPD7507HCU
μPD7508HCU
μPD80C48CU
μPD80C49HCU

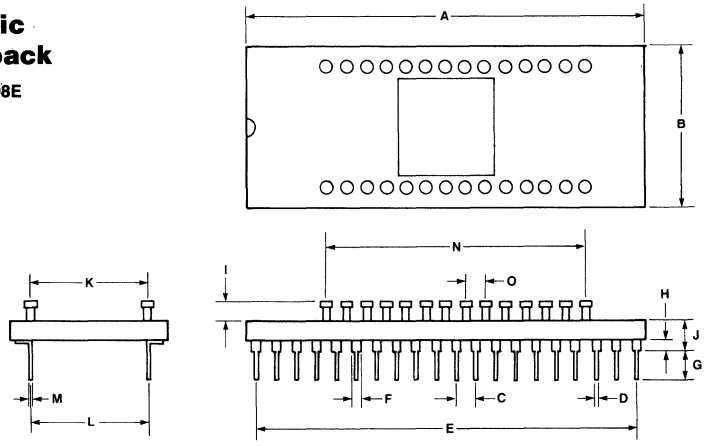
7

PACKAGE OUTLINES

40 PIN (Cont.)

Ceramic Piggyback

μPD75CG08E

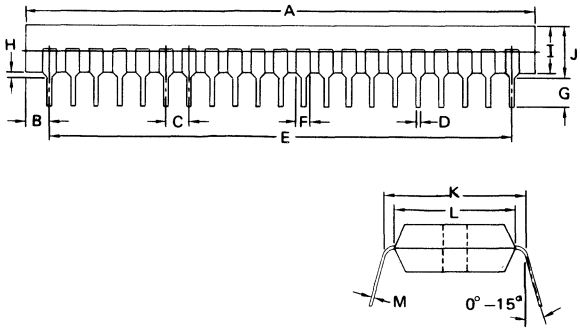


Item	Millimeters	Inches
A	53.34 max	2.1 max
B	20.32	.8
C	2.54 ± 0.25	.1 ± .01
D	0.46 ± 0.05	.018 ± .002
E	48.26	1.9
F	1.02	.04
G	3.2 min	.126 min
H	1.02 min	.04 min
I	3.0 max	.118 max
J	4.32 max	.170 max
K	15.24	.6
L	15.24	.6
M	0.25 ± 0.05	.01 ± .002
N	33.02	1.3
O	2.54 ± 0.25	.1 ± .01

42 PIN

Plastic

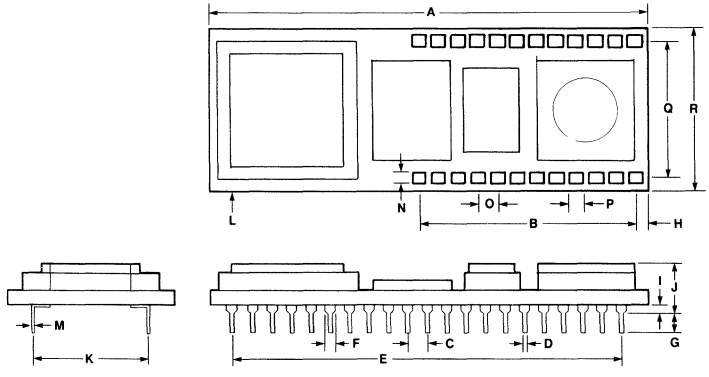
μCOM-4C
μPD552C/553C
μPD7527C/28C/37C/38C



Item	Millimeters	Inches
A	56.0 max	2.2 max
B	2.6 max	0.1 max
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 min	0.126 min
H	0.5 min	0.02 min
I	5.22 max	0.20 max
J	5.72 max	0.22 max
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

Cerdip

MC-430PD



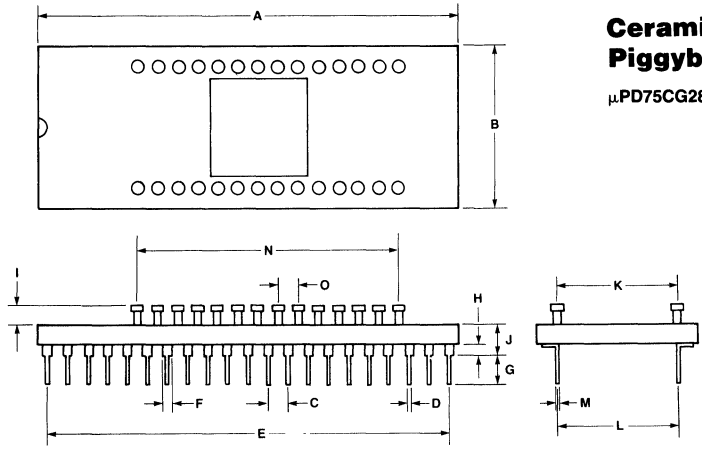
Item	Millimeters	Inches
A	56.5 max	2.24 max
B	27.94 ± 0.5	1.1 ± .02
C	2.54	0.1
D	$0.5^{+0.25}_{-0.1}$	$.02^{+.01}_{-.004}$
E	50.8	2.0
F	1.27	.05
G	2.54 min	0.1 min
H	1.5 ± 0.3	.059 ± .012
I	1.0 min	.039 min
J	6.5 max	.256 max
K	15.24	0.6
L	1	.039
M	$0.35^{+0.25}_{-0.1}$	$.014^{+.01}_{-.004}$
N	1.6	.063
O	2.54 ± 0.3	0.1 ± .012
P	2.0	.079
Q	1.74 ± 0.25	.685 ± .01
R	21.0 max	.827 max

42 PIN (Cont.)

Ceramic Piggyback

μPD75CG28E/CG38E

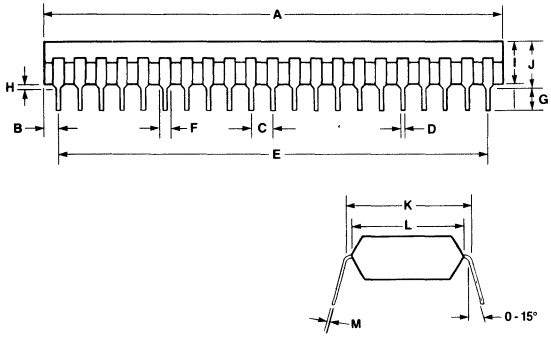
Item	Millimeters	Inches
A	55.88 max	2.2 max
B	20.32	.80
C	2.5 ± 0.25	.1 ± .01
D	0.46 ± 0.05	.018 ± .002
E	50.80	2.0
F	1.02	.04
G	3.2 min	.126 min
H	1.02 min	.04 min
I	3.0 max	.118 max
J	4.32 max	.17 max
K	15.24	.6
L	15.24	.6
M	0.25 ± 0.05	.001 ± .01
N	33.02	1.3
O	2.54 ± 0.25	.1 ± .01



Plastic Shrinkdip

μPD7527CU/28CU/ 37CU/38CU

Item	Millimeters	Inches
A	40.95 max	1.612 max
C	1.778	.07
D	0.5	.02
E	37.34	1.47
F	1.1	.043
G	2.54	.1
H	.51 min	.02 min
J	5.08 max	.2 max
K	15.24	.600
L	13.2	.52
M	$0.25^{+0.10}_{-0.50}$	$.01^{+.004}_{-.002}$

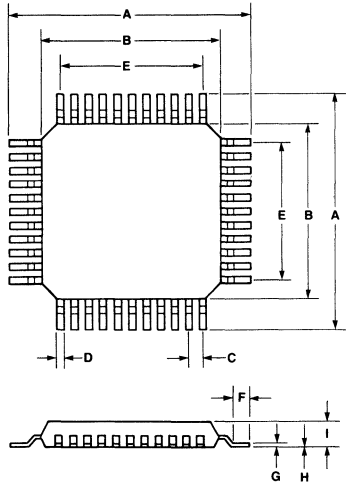


44 PIN

Plastic Miniflat

μPD80C49G
μPD80C48G

Item	Millimeters	Inches
A	1.36 ± 0.4	.054 ± .016
B	$10^{+.3}_{-.2}$	$.394^{+.012}_{-.008}$
C	0.8 ± 0.2	.03 ± .008
D	$.35^{+0.3}_{-0.1}$	$.014^{+.01}_{-.004}$
E	8.0 ± 0.3	.315 ± .012
F	1.0 ± 0.2	.39 ± .008
G	$0.15^{+0.10}_{-0.005}$	$.006^{+.004}_{-.0002}$
H	0.0 ± 0.1	0.0 ± .004
I	1.5 max	.059 max

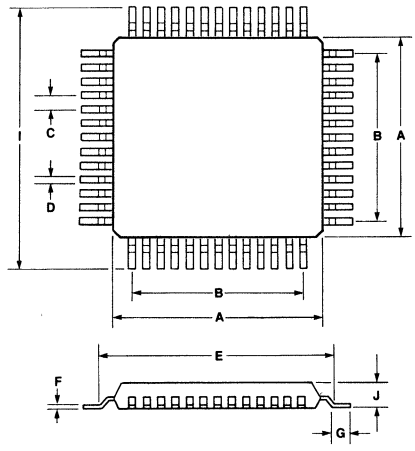


PACKAGE OUTLINES

52 PIN

Plastic Miniflat

μCOM-4G
μPD7506G
μPD7507G/08G
μPD80C49G/C39G
μPD80C48G/C35G
μPD7225G

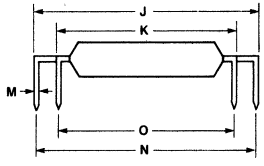


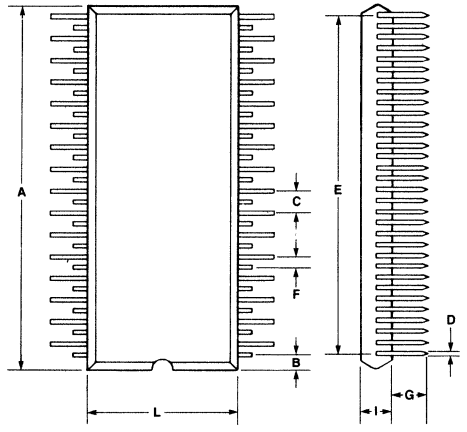
Item	Millimeters	Inches
A	14	.55
B	12.0 ± 0.3	.472 ± .012
C	1.0 ± 0.15	.039 ± .006
D	$0.4^{+0.2}_{-0.1}$	$.016^{+.008}_{-.004}$
E	17.0 max	.669 max
F	$0.15^{+0.10}_{-0.05}$	$.006^{+.004}_{-.002}$
G	2.2 ± 0.2	.087 ± .008
H	0.1 max	.004 max
I	20.6 ± 0.4	.811 ± .016
J	2.8 max	.110 max

64 PIN

Plastic QUIL

μPD7500G Evaluation Chip
μPD7800G
μPD7801G/02G
μPD7810G/11G
μPD7519G
μPD78C05G
μPD7807G/09G

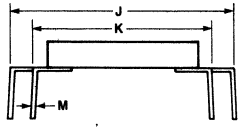


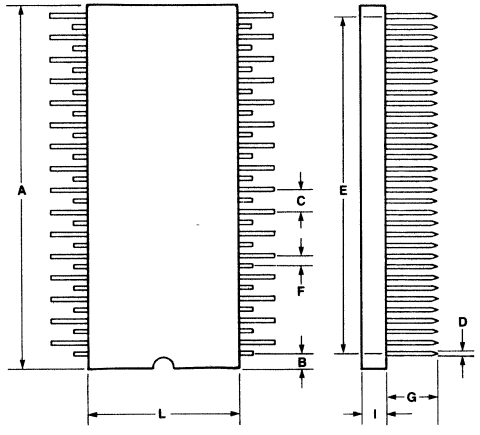


Item	Millimeters	Inches
A	41.5	1.63
B	1.05 ± 0.2	.041 ± .008
C	2.54	0.1
D	0.5 ± 0.1	.02 ± .004
E	39.4 ± 0.3	1.55 ± .012
F	1.27 ± 0.25	.05 ± .01
I	3.6	.142
J	24.13	.95
K	19.05	.75
L	16.5	.65
M	$.25^{+0.10}_{-0.05}$	$.01^{+.004}_{-.002}$
N	23.1 ~ 25.2	.909 ~ .99
O	18.0 ~ 20.1	.709 ~ .791

Ceramic QUIL

μPD556B





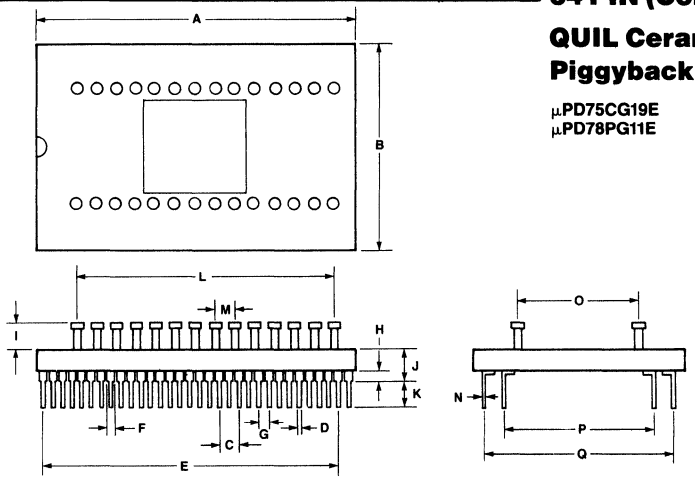
Item	Millimeters	Inches
A	41.5	1.634 max
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 min	0.21 min
I	2.35 max	0.13 max
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

64 PIN (Cont.)

QUIL Ceramic Piggyback

μPD75CG19E
μPD78PG11E

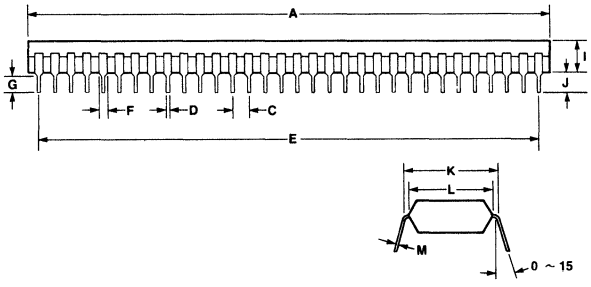
Item	Millimeters	Inches
A	42.0 max	1.65 max
B	26.67	1.05
C	2.54 ± 0.25	0.1 ± .01
D	0.46 ± 0.05	0.018 ± .002
E	38.10	1.5
F	1.02	.04
G	1.27 ± 0.25	.05 ± .01
H	1.02 min	.04 min
I	3.9 max	.154 max
J	4.45 max	.175 max
K	3.2 min	.126 min
L	33.02	1.3
M	2.54 ± 0.25	0.1 ± .01
N	0.25 ± 0.05	.01 ± .002
O	15.24	.6
P	19.05	.75
Q	24.13	.95



Plastic Shrinkdip

μPD7519CW
μPD7519HCW
μPD7801CW
μPD7802CW
μPD7810CW/11CW
μPD7809CW/07CW

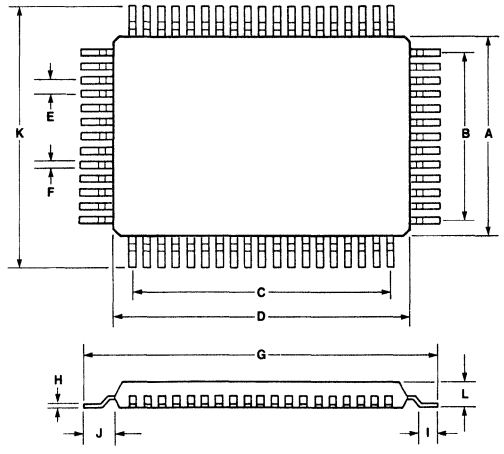
Item	Millimeters	Inches
A	58 typ	2.284 typ
C	1.778 typ	0.07 typ
D	0.5 typ	.0197 typ
E	55.12 typ	2.17 typ
F	1.1 typ	0.043 typ
G	3.2	.126
H	22.3 typ	.878 typ
I	4.05 typ	.159 typ
J	3.95 typ	0.156 typ
K	19.05 typ	0.75 typ
L	17 typ	0.669 typ
M	2.75 typ	0.108 typ



Plastic Miniflat

μPD7501G
μPD7502G/03G
μPD7227G
μPD78C06G

Item	Millimeters	Inches
A	14	.551
B	12 ± 0.3	.472 ± .012
C	18.0 ± 0.3	.709 ± .012
D	20	.787
E	1.0 ± 0.15	.039 ± .006
F	$0.4^{+0.2}_{-0.1}$	$.016^{+.008}_{-.004}$
G	24.7 ± 0.4	.972 ± .016
H	$0.15^{+0.10}_{-0.05}$	$.006^{+.004}_{-.002}$
I	1.2 ± 0.2	.047 ± .008
J	2.35 ± 0.2	.0925 ± .008
K	18.7 ± 0.4	.736 ± .016
L	2.3 max	.091 max



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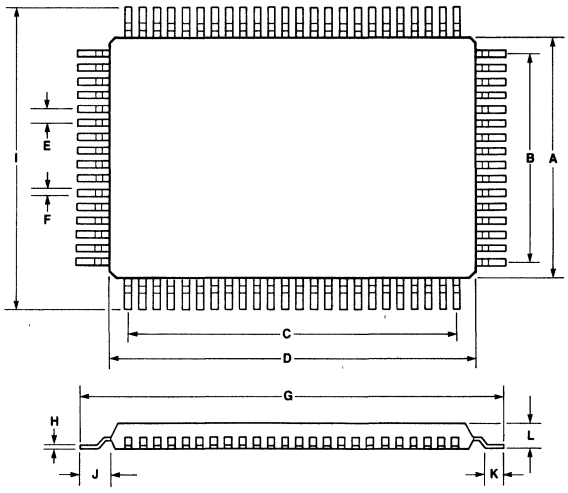
PACKAGE OUTLINES

80 PIN

Plastic Miniflat

μPD7514G
μPD7228G



Item	Millimeters	Inches
A	$14^{+.3}_{-.2}$	$.55^{+.012}_{-.008}$
B	12.0 ± 0.3	.472 ± .012
C	18.4 ± 0.3	.724 ± .012
D	$20^{+.3}_{-.2}$	$.787^{+.012}_{-.008}$
E	0.8 ± 0.15	.0315 ± .006
F	$0.35^{+0.2}_{-0.1}$	$.0925^{+.008}_{-.004}$
G	24.7 ± 0.4	.972 ± .016
H	$0.15^{+0.10}_{-0.05}$	$.006^{+.004}_{-.002}$
I	18.7 ± 0.4	.736 ± .016
J	2.35 ± 0.2	.0925 ± .008
K	1.2 ± 0.2	.048 ± .008
L	$2.05^{+0.25}_{-0.10}$	$.081^{+.01}_{-.004}$

NEC

QUALITY & RELIABILITY OF NEC MICROPROCESSORS

8

Introduction

As large-scale integration reaches a higher level of density, reliability of devices imposes a profound impact on system reliability. And as device reliability becomes a major factor, test methods to assure acceptable reliability become more complicated. Simply performing a reliability test according to a conventional method cannot satisfy the demanding requirements for higher reliability: at these new, higher levels of LSI density, it is increasingly difficult to activate all the elements in the internal circuits. A different philosophy and methodology is needed for reliability assurance in microprocessors and family products. Moreover, as integration density increases, the degradation of internal elements in an LSI device is seldom detected by measuring characteristics across external terminals.

In order to improve and guarantee a certain level of reliability for large-scale integrated circuits, it is essential to build quality and reliability into the product. Then the conventional reliability tests are followed to ensure that the product demonstrates an acceptable level of reliability.

NEC has introduced the concept of Total Quality Control (TQC) across its entire semiconductor production line. By adopting TQC, NEC can build quality into the product and thus assure higher reliability. The concept and methodology of Total Quality Control are companywide activities—involving workers, engineers, quality control staffs, and all levels of management.

NEC has also introduced a prescreening method into the production line that helps eliminate most of the potentially defective units. The combination of building quality in and screening projected early failures out has resulted in superior quality and excellent reliability.

This Reliability Report describes the philosophy and methodology used by NEC to attain a higher level of reliability for microprocessors and family products.

Technology Description

Most microprocessors and family products are produced utilizing high performance, high density, N-channel MOS technology. State-of-the-art high performance has been achieved by introducing fine line generation techniques. The data presented in this report shows that this advanced technology yields products as reliable as those from previous technologies.

By reducing physical parameters, circuit density and performance were increased while active circuit power dissipation decreased. Current state-of-the-art N-channel MOS technology utilizes 2–4μm channel length and a gate oxide thickness of 300–500Å. This advanced process yields integration densities of 400–800 gates/mm^2 with a speed-power product of 1pJ or less.

Technology evolution

Technology evolved from early P-channel MOS to current state-of-the-art high performance, high density, N-channel MOS during the past decade. This evolution is expected to continue in the future. As a result, even more high level functions will be included in a small area, as past history demonstrates.

Reliability Testing

Reliability is defined as the characteristics of an item expressed by the probability that it will perform a required function under stated conditions for a stated period of time. This involves the concept of probability, definition of a required function(s), and the critical time used in defining the reliability.

Definition of a required function, by implication, treats the definition of a failure. Failure is defined as the termination of the ability of a device to perform its required function(s). Futhermore, a device is said to have failed if it shows inability to perform within guaranteed parameters as given in an electrical specification.

Discussion of reliability and failure can be approached in two ways: with respect to systems or to individual devices. The accumulation of normal device failure rates constitutes the expected failure rate of the system hardware. Important considerations here are the constant failure period, the early failure (infant mortality) period, and overall reliability level. With regard to individual devices, areas of prime interest include specific failure mechanisms, failures in accelerated tests, and screening tests.

Some of these failure considerations pertain to both systems and devices. The probability of no failures in a system is the product of the probability of no failure in each of its components. The failure rate of system hardware is then the sum of the failure rates of the components used to construct the system.

Life distribution

The fundamental principles of Reliability Engineering predict that the failure rate of a group of devices will follow the well-known Bathtub curve in Figure 1. The curve is divided into three regions: Infant Mortality, Random Failures, and Wearout Failures.

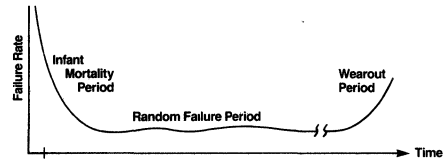


Figure 1. Reliability Life (Bathtub) Curve

Infant mortality, as the name implies, represents the early life failures of devices. These failures are usually associated with one or more manufacturing defects.

After some period of time, the failure rate reaches a low value. This is the random failure portion of the curve, representing the useful portion of the life of a device. During this random failure period there is a decline in the failure rate due to the depletion of potential random failures from the general population.

The wearout failures occur at the end of the device's useful life. They are characterized by a rapidly rising failure rate over time as devices wear out both physically and electrically.

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Thus, for devices which have very long life expectancies compared to those of systems, the areas of concern will be the infant mortality and the random failure portions of the population.

The system failure rates are related to the collective device failure rates. In a given system, after elimination of the early failures, the system will be left to the failure rate of its components. In order to make proper projections of the failure rate in the operating environment, time-to-failure must be accelerated in tests in a predictable way.

Failure distribution at NEC

MOS and Bipolar integrated circuits returned to NEC from the field underwent extensive failure analysis at NEC's Integrated Circuit Division.

First, approximately 50 percent of the field returns were found to be damaged either from improper handling or misuse of the devices. These units were eliminated from the analysis. The remaining failed units were classified by their failure mechanisms, as depicted in Figure 2. These failures were then related to the major integrated circuit failure mechanisms and to their origins in a particular manufacturing step.

As shown in Figure 2, the first four failure mechanisms accounted for more than 90 percent of total failures. As a result, NEC improved processes and material to reduce these failures. Additionally, NEC introduced screening procedures to detect and eliminate defective devices.

Temperature, humidity, and bias tests are used for testing the moisture resistance of plastic encapsulated integrated circuits. NEC developed a special process to improve the plastic encapsulation material. As a result, moisture-related—thus packaging-related—failures have been drastically reduced.

As a preventive measure, NEC has introduced a special screening procedure embedded in the production line. A burn-in at an elevated temperature is performed for 100 percent of the lots. This burn-in effectively removes the potentially defective units. In addition, improvement of the plastic encapsulation material has lowered the failures in a high temperature and high humidity environment.

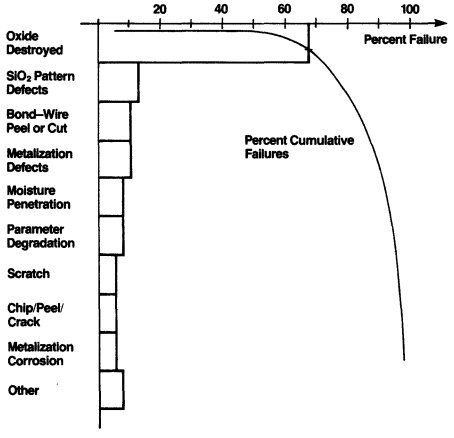

Figure 2. Failure Distribution of MOS Integrated Circuits

Accelerated reliability testing

As an example, assume that an electronic system contains 1000 integrated circuits and can tolerate 1 percent system failures per month. The failure rate per component is:

$$\frac{0.01 \text{ Failures}}{720\text{K Device Hours}} = 13.888 \times 10^{-9} \text{ Failures/Hour or } 13.8888 \text{ FITs}$$

Where: FIT = Failure unit per 10^9 device hours

To demonstrate this failure rate, note that 13.8888 FITs correspond to one failure in about 7,000 devices in an operating test of 10,000 hours. It is quickly apparent that a test condition is required to accelerate the time-to-failure in a predictable and understandable way. The implicit requirement for the accelerated stress test is that the relationship between the accelerated stress testing condition and the condition of actual use be known.

A most common time-to-failure relationship involves the effect of temperature, which accelerates many physiochemical reactions leading to device failure. Other environmental conditions are voltage, current, humidity, vibration, or some combination of these. Table 2 lists the Reliability Assurance Tests performed at NEC for the N-channel MOS devices.

Table 1. Monthly NEC Reliability Tests

Test	Method	Test Conditions
Life Test	***MIL-STD-883B***	
High Temperature, Operating	1005A, D	T_a = 100°C to 125°C for 1000 hrs
High Temperature, Storage	1008C	T_a = 150°C for 1000 hrs
High Temperature, High Humidity Test	—	T_a = 85°C @85% RH for 1000 hrs
Pressure Cooker Test	—	T_a = 125°C @2.3 Atm for 168 hrs
Environmental Test		
Soldering Heat Test	2031*	T = 260°C for 10s without flux
Temperature Cycle	1010C	T = −65°C to +150°C for 10 cycles
Thermal Shock	1011A	T = 0°C to 100°C for 15 cycles
Lead Fatigue	2004B2	@250gm: 3 leads, 3 bends
Solderability	2003	T = 230°C for 5s with flux

Note: * MIL-STD-750A

Temperature Effect: The effect of temperature that concerns us is that which responds to the Arrhenius relationship. This relates the reaction rate to temperature.

$$R = Ro\ Exp[-Ea/kT]$$

Where: Ro = Constant
Ea = Activation energy in eV
k = Boltzmann's constant
= 8.617*10**(−5) eV/degrees K
T = Absolute temperature in degrees K

The significance of this relationship is that the failure mechanisms of semiconductor devices are directly applicable to it. A linear relationship between failure mechanism and time is assumed.

Activation Energy: Associated with each failure mechanism is an activation energy value. Table 3 lists some of the more common failure mechanisms and the associated activation energy of each.

Table 2. Activation Energy and Detection of Failure Mechanisms

Failure Mechanism	Activation Energy	Detection
Oxide Defect	0.3eV	High Temperature Operating Life Test
Silicon Defect	0.3eV	
Ionic Contamination	1.0–1.35eV	
Electromigration	0.4–0.8eV	
Charge Injection	1.3eV	
Gold–Aluminum Interface	0.8eV	
Metal Corrosion	0.7eV	High Humidity Operating Life Test

High Temperature Operating Life Test: This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. For N-channel MOS microprocessors and their family products, the operating temperature is 125°C. The data obtained is translated to a lower temperature by using the Arrhenius relationship.

High Temperature and High Humidity Test: Semiconductor integrated circuits are highly sensitive to the general accelerating effect of humidity in causing electrolytic corrosion between biased lines. The high temperature and high humidity test is performed to detect failure mechanisms which are accelerated by these conditions. This test is effective in accelerating leakage-related failures and drifts in device parameters due to process instability.

High Temperature Storage Test: Another common test is the high temperature storage test in which devices are subjected to elevated temperatures with no applied bias. This test is used to detect mechanical problems and process instability.

Environmental Test: Other environmental tests are performed to detect problems related to the package, material, susceptibility to extremes in environment, and problems related to usage of the devices.

Failure Rate Calculation and Prediction

Analysis of integrated circuit failure rates can serve many useful purposes. For example, the early life failure rate helps establish a warranty period, while the mature life failure rate aids in estimating repair costs, spare parts stock requirements, or product downtime. Accurate prediction of failure rates can also be used for process control.

The following sections describe the failure rate calculation and prediction methods used by NEC's Integrated Circuit Division.

The Arrhenius model

Most integrated circuit failure mechanisms depend, to some degree, on temperature. This relationship can be represented by the Arrhenius model, which includes the effects of temperature and activation energy of the failure mechanisms.

As applied to accelerated life testing of integrated circuits, the Arrhenius model assumes that degradation of a performance parameter is linear with time. Temperature dependence is taken to be the exponential function that defines the probability of occurrence. The relationship of failure rate to temperature is expressed as:

$$F_1 = F_2 * \mathrm{Exp}[(Ea/k) * (1/T_1 - 1/T_2)]$$

Where: F_2 = Failure rate at T_2
F_1 = Failure rate at T_1
Ea = Activation energy
k = Boltzmann's constant
T = Operating junction temperature in degrees K

This equation explains the thermal dependence of integrated circuit failure rates and is used for derating the resulting failure rate to a more realistic temperature.

Acceleration factor

The acceleration factor is the factor by which the failure rate can be accelerated by increased temperature. This factor is derived from the Arrhenius failure rate expression, resulting in the following form:

$$A = F_1/F_2 = \mathrm{Exp}[(Ea/k) * (1/T_1 - 1/T_2)]$$

Where: A = Acceleration factor
F_2 = Failure rate at T_2
F_1 = Failure rate at T_1

In calculating the field reliability of an integrated circuit, it is necessary to calculate the junction temperature. In general, the junction temperature will depend on the ambient temperature, cooling, package type, operating cycle time, and power dissipation of the circuit itself. In these terms, the junction temperature (T_j) is expressed as:

$$T_j = T_a + Pd * Af * \theta jA$$

Where: T_j = Junction temperature
T_a = Ambient temperature
Pd = Power dissipation
Af = Air flow factor
θjA = Package thermal resistance

Table 4 lists derating factors of various failure mechanisms. This table is generated assuming that an accelerated test is performed at a junction temperature of 125°C. The result is then derated to 55°C junction temperature. The acceleration factor may then be obtained by taking the inverse of the derating factor.

Table 3. Derating Factors of Failure Mechanisms

Failure Mechanism	Activation Energy	Derating Factor
Oxide Defect	0.3eV	0.1546
Silicon Defect	0.3eV	0.1546
Ionic Contamination	1.0eV	0.001984
Electromigration	0.4eV	0.08307
Charge Injection	1.3eV	0.0003067
Metal Corrosion	0.7eV	0.01315
Gold–Aluminum Interface	0.8eV	0.006886

The acceleration of failure mechanisms in a high humidity and high temperature environment must be expressed as a function not only of temperature but also of humidity.

According to the reliability test statistics, the acceleration factor in such an environment can best be approximated with Peck's model as follows:

$$A = \mathrm{Exp}[(Ea/k) * (1/T_1 - 1/T_2)] * [H_2/H_1] ** 4.5$$

Where: Ea = Activation energy
k = Boltzmann's constant
T = Junction temperature
H = Relative humidity

For example, the acceleration factor for high humidity and high temperature or pressure cooker tests ranges from 100 to 1000 times that of the normal operating environment.

Failure rate calculation

As an example, suppose that NEC's microprocessors and family product samples are submitted to a 1000-hour life test at 125°C junction temperature and encounter two failures: one oxide and one metalization defect. The sample size is 885 units.

Thus, the oxide failure rate is 0.11 percent per 1000 hours and the metalization failure rate is 0.11 percent per 1000 hours. Therefore, the total failure rate at 125°C sums to 0.22 percent per 1000 hours at 1K hours.

Failure rate prediction

To derate these failure rates to a normal operating environment, use the derating factors listed in Table 4.

Oxide Failures = 0.11 * 0.1546 = 0.01701% per 1K hrs
Metal Failures = 0.11 * 0.01315 = 0.00145% per 1K hrs
Total Failures = 0.01846% per 1K hours

Note that the example above is a snapshot of the high temperature life test performed on a particular lot. It is not accumulated data that can be used to represent overall reliability. This conservative illustration, however, shows that the failure rate in a normal operating environment is approximately 12 times lower than that of a higher temperature environment.

The failure rate prediction takes different activation energies into account whenever the causes of failures are known through performing failure analysis. In some cases, however, an average activation energy is assumed in order to accomplish a quick first-order approximation: NEC assumes an average activation energy of 0.7eV whenever the exact failure mechanism is not known, to yield a conservative estimate of failure rates.

Reliability Test Results

Before introducing new technologies or products, NEC's internal reliability goals must be attained. Several categories of testing are used in the internal qualification program to assure that product reliability meets NEC's reliability goals. Once the product is qualified, its reliability level is regularly monitored in a monthly reliability test.

NEC's Goals on Failure Rates

NEC's approach to achieving high reliability is to build quality into the product, as opposed to merely screening out defective units. The use of distributed control methods embedded in the production line, in conjunction with conventional screening methods, results in the highest reliability at the lowest cost.

NEC currently maintains failure rates for infant mortality and long-term device operation as listed in Table 4.

Table 4. Infant Mortality and Long-term Failure Rates

	Percent Failure Rate Goals
Infant Mortality Failure Rate	0.10/1K hrs
Long-term Life Failure Rate	
1.2M Device Hour Average	0.02/1K hrs
3.0M Device Hour Average	0.01/1K hrs

Infant mortality process average goals

The infant mortality goal for each product group is set at 0.10 percent. When a failure rate exceeds this level, there is prompt remedial action to reduce this rate.

Long-term failure rate goals

The long-term failure rate goal is based on the following conditions:

- ☐ A minimum of 1.2 million device hours at 125°C is accumulated to resolve 0.02 percent per 1000 hours at 55°C with a 60 percent confidence level.
- ☐ A minimum of 3 million device hours at 125°C is accumulated to resolve 0.01 percent per 1000 hours at 55°C with a 60 percent confidence level.

Infant Mortality Failure Screening

It is logical to assume that the integrated circuit that fails at one temperature would also fail at another temperature, except that it would fail sooner at a higher temperature. As can be expected, the failure rate is a function of its associated activation energy. Establishing infant mortality screening, therefore, requires knowledge of the likely failure mechanisms and their associated activation energy.

The most likely mechanisms associated with infant mortality failures are generally manufacturing defects and process anomalies. These generally consist of contamination, cracked chips, wire bond shorts, or bad wire bonds. Since these describe a number of possible mechanisms, any one of which might predominate at a given time, the activation energy for infant mortality might be expected to vary considerably.

The effectiveness of a screening condition, preferably at some stress level in order to shorten the time, varies greatly with the failure mechanism being screened for. Another factor is the economics of the screening process introduced into the production line. Optimal conditions and duration of a screening process will be a compromise of these two factors.

For example, failures due to ionic contamination have an activation energy of approximately 1.0eV. Therefore, a 15-hour stress at 125°C junction temperature would be the equivalent of approximately 90 days of operation at a junction temperature of 55°C. On the other hand, failures due to oxide defects have an activation energy of approximately 0.3eV, and a 15-hour stress at 125°C junction temperature would be the equivalent of approximately one week's operation at 55°C junction temperature. As indicated by this, the condition and duration of infant mortality screening would be a strong function of the allowable component failures, hence the system failure, in the field.

Empirical data, gathered over more than a year at NEC, indicates that early failure does occur after less than 4 hours of stress at 125°C ambient temperature. This fact is supported by the life test of the same lot, where the failure rate shows random distribution, as opposed to a decreasing failure rate which then runs into the random failure region.

NEC has adopted the initial infant mortality burn-in at 125°C as a standard production screening procedure. As a result, the field reliability of NEC devices is an order of magnitude higher than the goals set for NEC's integrated circuit products.

Life Tests

The most significant difference between NEC's products and those of other integrated circuit manufacturers is the fact that NEC's have been prescreened for their infant mortality defects. The products delivered to customers are operating at the beginning of the random failure region of the life curve. The life test data also reflect this fact, as will be shown in the following sections.

The failure mechanism distribution from field failures, as previously shown in Figure 2, also contains a very low percentage due to infant mortality. The majority of failures are long-term life failures, and these can be eliminated by stringent process control. Usually, these failure mechanisms have low activation energy associated with them.

Another significant improvement devised by NEC is plastic encapsulation and passivation. As a result, NEC products show excellent reliability in both high humidity and high temperature environments. Following is life test data accumulated over more than a year for N-channel microprocessors and family products.

High temperature operating life test

This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. For microprocessors and family products, the failure rate is 0.242 percent per 1000 hours at 125°C. This is equivalent to 0.0071 percent per 1000 hours in an operating environment of 55°C (Table 5).

Table 5. High Temperature Operating Life Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
3317	0	0	1	4	3

Total Number of Failures at 1K hrs = 8
Failure Rate at 1K hrs at 125°C = 0.242% per 1K hrs
Projected Failure Rate at 55°C = 0.007% per 1K hrs

High temperature and high humidity life test

This test is used to accelerate failure mechanisms by operating the devices at high temperature and high humidity. Leakage-related failures and device parameter drift are accelerated by this test. For microprocessors and family products, the failure rate is 0.091 percent per 1000 hours. This is equivalent to 0.0027 percent per 1000 hours in an operating environment of 55°C. The test conditions are T_a = 85°C and relative humidity (RH) = 80% (Table 6).

Table 6. High Temperature and High Humidity Life Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2190	0	0	0	0	2

Total Number of Failures at 1K hrs = 2
Failure Rate at 1K hrs at 85°C/85% RH = 0.091% per 1K hrs
Projected Failure Rate at 55°C/60% RH = 0.003% per 1K hrs

High temperature storage life test

This test is effective in accelerating the failure mechanisms related to mechanical reliability problems and process instability. For microprocessors and family products, the failure rate is 0.207 percent per 1000 hours at 125°C. This is equivalent to 0.0061 percent per 1000 hours in an operating environment of 55°C (Table 7).

Table 7. High Temperature Storage Life Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2410	0	0	0	1	4

Total Number of Failures at 1K hrs = 5
Failure Rate at 1K hrs at 125°C = 0.207% per 1K hrs
Projected Failure Rate at 55°C = 0.006% per 1K hrs

Pressure cooker test

This test is effective in accelerating failure mechanisms related to metalization corrosion due to moisture. The failure rate is 0.52 percent per 1000 hours at T_a = 125°C and 2.3 Atm at 100 percent humidity. This is equivalent to 0.0013 percent per 1000 hours at 55°C and an environment of 60 percent humidity (Table 8).

Table 8. Pressure Cooker Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
1718	0	4	5	No Test Performed	

Total Number of Failures at 168 hrs = 9
Failure Rate at 125°C = 0.54% per 1K hrs
Projected Failure Rate at 55°C = 0.001% per 1K hrs

Life test data summary

Table 9 summarizes the life test results and projected failure rates in the normal operating environment. The failure rate shows random distribution as opposed to a decreasing failure rate. This is a result of infant mortality screening.

Table 9. Life Test Data

Test Item	Number of Samples	Number of Failures at 96 hrs	168 hrs	500 hrs	1K hrs	Total Number of Failures
High Temperature Life Test	3317	0	1	4	3	8
High Humidity Life Test	2190	0	0	0	2	2
High Temperature Storage Life Test	2410	0	0	1	4	5
Pressure Cooker Test	1718	4	5	*	*	9
Total	9635	4	6	5	9	24

Note: * = No test performed

The projected failure rate in the normal operating environment is calculated assuming that the average activation energy is 0.7eV.

Figure 3 shows the life distribution of NEC integrated circuits as a form of the Bathtub curve.

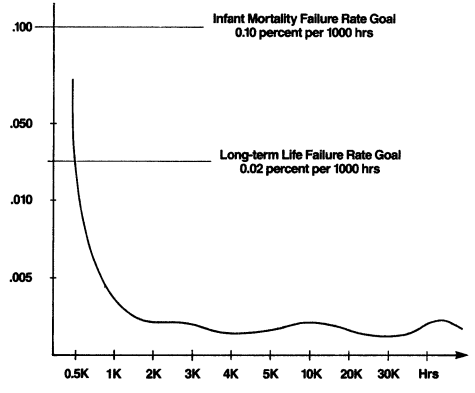

Figure 3. Plot of Life Test Results

This life test data shows improvements of approximately an order of magnitude better than NEC's goal. The hours of operation are equivalent to the normal operating environment. Wear-out failures, which had been the main target for reliability improvement, have also been significantly reduced. This result comes mainly from process improvements and stringent manufacturing process control.

NEC's main goal has been to improve reliability with respect to infant mortality and long-term life failures. This can be achieved by introducing an effective screening method for infant mortality and building quality into the product.

Thermal stress tests

Temperature cycling and thermal shock test the thermal compatibility of material and metal used to make integrated circuits. Table 10 lists the reliability test results of thermal stress tests.

Table 10. Thermal Stress Results

Test Item	Number of Samples	Number of Failures
Soldering Heat Test T_a = 260°C for 10 seconds	1891	0
Temperature Cycle T_a = −65°C to +150°C, 10 cycles	1891	0
Thermal Shock Test T_a = 0°C to +100°C, 15 cycles	1891	0

Mechanical stress tests

In addition to the device life test, NEC performs mechanical stress tests to detect reliability problems related to the package, material, and device susceptibility to an extreme environment. Table 11 lists mechanical stress test results.

Table 11. Mechanical Stress Results

Test Item	Number of Samples	Number of Failures
Mechanical Shock Test @15kg, 3 axis	315	0
Vibration Test @100Hz to 2kHz, 20g	315	0
Constant Acceleration @20kg, 3 axis	315	0
Lead Fatigue Test @250 gms	638	0
Solderability Test @230°C for 5 seconds	638	0

Built-in Quality and Reliability

As large-scale integration reaches even higher levels of density, simple quality inspections cannot assure adequate levels of product quality and reliability. In order to ensure the reliability of state-of-the-art, very large-scale integrated circuits, NEC has adopted another approach. Highest reliability and superior quality of a device can only be achieved by building these characteristics into the product at each process step. NEC, therefore, has introduced the notion of Total Quality Control (TQC) into its entire semiconductor production line. Quality control is distributed into each process step and then all are summed to form a consolidated system.

Approaches to Total Quality Control

First, the quality control function is embedded into each process. This method enables early detection of possible causes of failure and immediate feedback.

Second, the reliability and quality assurance policy is an integral part of the entire organization. This enables a companywide quality control activity. At NEC, everyone in the company is involved with the concept and methodology of Total Quality Control.

Third, there is an on-going research and development effort to set even higher standards of device quality and reliability.

Fourth, extensive failure analysis is performed periodically and corrective actions are taken as preventive measures. Process control is based on statistical data gathered from this analysis.

The goal is to maintain the superior product quality and reliability that has become synonymous with the NEC name. The new standard is continuously upgraded and the iterative process continues.

Implementation of distributed quality control

Building quality into a product requires early detection of possible cause of failure at each process step. Then, immediate feedback to remove the cause of failure is a must. A fixed station quality inspection is often lacking in immediate feedback. It is, therefore, necessary to distribute quality control functions to each process step, including the conceptual stage. NEC has implemented a distributed quality control function at each step of the process. Following is a breakdown of the significant steps:

- ☐ Product development phase
- ☐ Wafer processing
- ☐ Chip mounting and packaging
- ☐ Electrical testing and thermal aging
- ☐ Incoming material inspection

Product Development Phase: The product development phase includes conception of a product, review of the device proposal, organization and physical element design, engineering evaluation, and finally, transfer of the product to manufacturing. Quality and reliability are considered at every step. More significantly, at the design review stage and prior to product transfer, the quality and reliability requirements have to be examined and determined to be satisfactory. This often adds two to three months to the product development cycle. Building in high reliability, however, cannot be sacrificed.

Wafer Processing Stage Inspection: The in-process quality inspections that occur at the wafer fabrication stage are listed in Table 12.

Table 12. Wafer Fabrication Inspection

Process	Inspection Item
Wafer	Resistivity, Dimension, and Appearance, Lot Sampling Inspection
Mask	
Photo-Lithography	Alignment and Etching, 100 Percent Inspection
Cleaning	
Diffusion and Oxidation	Oxide Thickness, Sheet Resistivity, Lot Sampling Inspection
Metalization and Passivation	Thickness, V_{th}, C-V Characteristics, and Lot Sampling
Wafer Sort and Scribe	DC Parameters, 100 Percent Inspection
Die Sort	100 Percent Visual Inspection

Chip Mounting and Packaging: The in-process quality inspections that are done at the chip mounting and packaging stage are listed in Table 13.

Table 13. Chip Mounting and Packaging Inspection

Process	Inspection Item
Die	Incoming Material Inspection
Die Attach	Appearance, Lot Sampling Inspection
Wire Bonding	Bond Strength, Appearance, Lot Sampling
Packaging	100 Percent Appearance Inspection
Fine Leak*	Lot Sampling
Gross Leak*	100 Percent Inspection

Note: * For ceramic package devices only

Electrical Testing and Screening: Electrical testing and infant mortality screening are performed at this stage. A flowchart of the process is depicted in Figure 4.

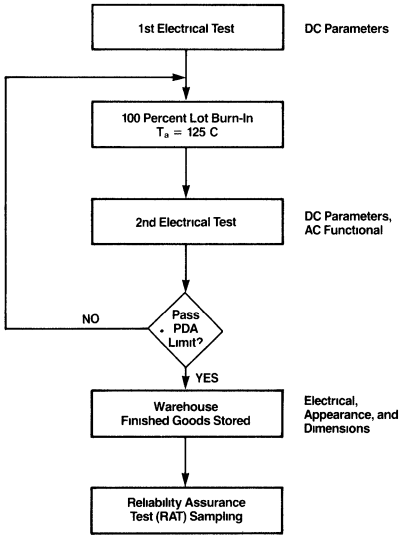

Figure 4. Electrical Testing and Screening

At the first electrical test, DC parameters are tested, according to the electrical specifications, on 100 percent of each lot. This is a prescreening prior to the infant mortality test. At the second electrical test, AC functional as well as DC parameter tests are performed on 100 percent of the subjected lot. If the percentage of defective units exceeds the limit, the lot is subjected to an additional burn-in. As this defective lot is being subjected to an additional burn-in, the defective units are undergoing a failure analysis, the results of which are then fed back into the process for corrective action.

Incoming Material Inspection: Prior to warehouse storage, lots are subjected to an incoming inspection according to the following sampling plan:

☐ Electrical test: DC parameters LTPD 3%
Functional test LTPD 3%
☐ Appearance LTPD 3%

Reliability assurance test

Samples are continually taken from the warehouse and subjected to monthly reliability tests as discussed in the previous section. They are taken from similar process groups so that it can be assumed that any device is representative of the reliability of that group.

In-process screening

Perhaps the most significant preventive measure that NEC has implemented is the introduction of 100 percent burn-in as an integral part of the standard production process. Most of the potential infant failures are effectively screened from every lot, thereby improving reliability. Assuming average activation energy of 0.7eV, burn-in at T_a = 125°C for four hours is equivalent to a week's operation in a normal operating environment. This appears to be ample time for accelerating the time-to-failure mechanisms for early failures.

Process automation, as previously mentioned, has also contributed a great deal in improving reliability. Since its introduction, assembly related failure mechanisms have been substantially reduced. And, in combination with in-process screening and materials improvement, it has helped establish quality and reliability above NEC's initial goals.

Summary and Conclusion

As has been discussed, building quality and reliability into products is the most efficient way to ensure product reliability. NEC's approach of distributing quality control functions to process steps, then forming a consolidated quality control system, has produced superior quality and excellent reliability.

Prescreening, introduced as an integral part of large-scale integrated circuit production, has been a major factor in improving reliability. The most recent year's production clearly demonstrates continuation of NEC's high reliability and the effectiveness of this method.

Reliability Assurance Tests (RATs), performed monthly, have ensured high outgoing quality levels. The combination of building quality into products, effective prescreening of potential failures, and the reliability assurance test has established a singularly high standard of quality and reliability for NEC's large-scale integrated circuits.

With a companywide quality control program, NEC is committed to building superior quality and highest reliability into all its products. Through continuous research and development activities, extensive failure analysis, and process improvements, a higher standard of quality and reliability will continuously be set and maintained.

Notes

NEC

NEC

U.S. REPRESENTATIVES

Alabama

20th Century Marketing, Inc
Huntsville, AL 35801
205-533-9281

Arizona

Fred Board Associates, Inc
Scottsdale, AZ 85251
602-994-9388

Tucson, AZ 85704
602-299-1508

California

CERCO
San Diego, CA 92117
619-274-1901

Quorum Technical Sales
Santa Clara, CA 95054
408-980-0812

Colorado

Candal, Inc
Golden, CO 80401
303-233-0155

Connecticut

HLM Associates
Waterbury, CT 06708
203-753-9894

Florida

Semtronics, Inc
Altamonte Springs, FL 32701
305-831-8233

Clearwater, FL 33515
813-461-4675

Georgia

Montgomery Marketing, Inc
Norcross, GA 30092
404-447-6124

Illinois

A M E Sales
Collinsville, IL 62234
618-345-7404

Seiger Associates
Rolling Meadows, IL 60008
312-991-6161

Indiana

M/S Sales & Associates, Inc
Fort Wayne, IN 46808
219-484-1904

Indianapolis, IN 46260
317-257-8915

Iowa

George Russell & Associates
Cedar Rapids, IA 52402
319-369-9134

Kansas

A M E Sales
Overland Park, KS 66202
913-262-3971

Maryland

Professional Representatives
Baltimore, MD 21208
301-653-3600

Massachusetts

Compass Technology
Woburn, MA 01801
617-933-3336

Michigan

Miltmore Sales, Inc
Grand Rapids, MI 49506
616-942-9721

Novi, MI 48050
313-349-0260

Minnesota

George Russell & Associates
Bloomington, MN 55420
612-854-1166

New Jersey

B G R Associates
Marlton, NJ 08053
609-428-2440

HLM Associates, Inc
Parsippany, NJ 07054
201-263-1535

New Mexico

Rontek, Inc
Albuquerque, NM 87191
505-299-4124

New York

ELCOM Sales
Penfield, NY 14526
716-385-1400

Skaneateles, NY 13152
315-685-8245

HLM Associates, Inc
Northport, NY 11768
516-757-1606

North Carolina

Montgomery Marketing, Inc
Cary, NC 27511
919-467-6319

Pennsylvania

Imtech, Inc
Pittsburgh, PA 15243
412-344-0844

Ohio

Imtech, Inc
Akron, OH 44321
216-666-1185

Dayton, OH 45414
513-278-6507

Oregon

Electronic Technical Sales Associates
Hillsboro, OR 97123
503-640-8086

Tennessee

20th Century Marketing, Inc
Knoxville, TN 37923
615-966-3608

Texas

Technical Marketing, Inc
Austin, TX 78758
512-835-0064

Carrollton, TX 75006
214-387-3601

Houston, TX 77081
713-777-9228

Utah

Aspen Sales
Salt Lake City, UT 84115
801-467-2401

Washington

Electronic Technical Sales Associates
Kirkland, WA 98033
206-827-8086

CANADIAN REPRESENTATIVES

British Columbia

Kaytronics Western
Surrey, BC V3R 4G8
604-581-7611

Ontario

Kaytronics, Inc
Concord, Ontario L4K 1B1
416-669-2262

Kanata, Ontario K2K 2A3
613-592-6606

Quebec

Kaytronics, Inc
Ville St Pierre, QU H8R 3Y8
514-367-0101

NEC NEC Electronics

401 Ellis Street
Mountain View, CA 94043
TEL. 415-960-6000, TWX: 910-379-6985

84 MICROCAT–1-84–USA 50 K