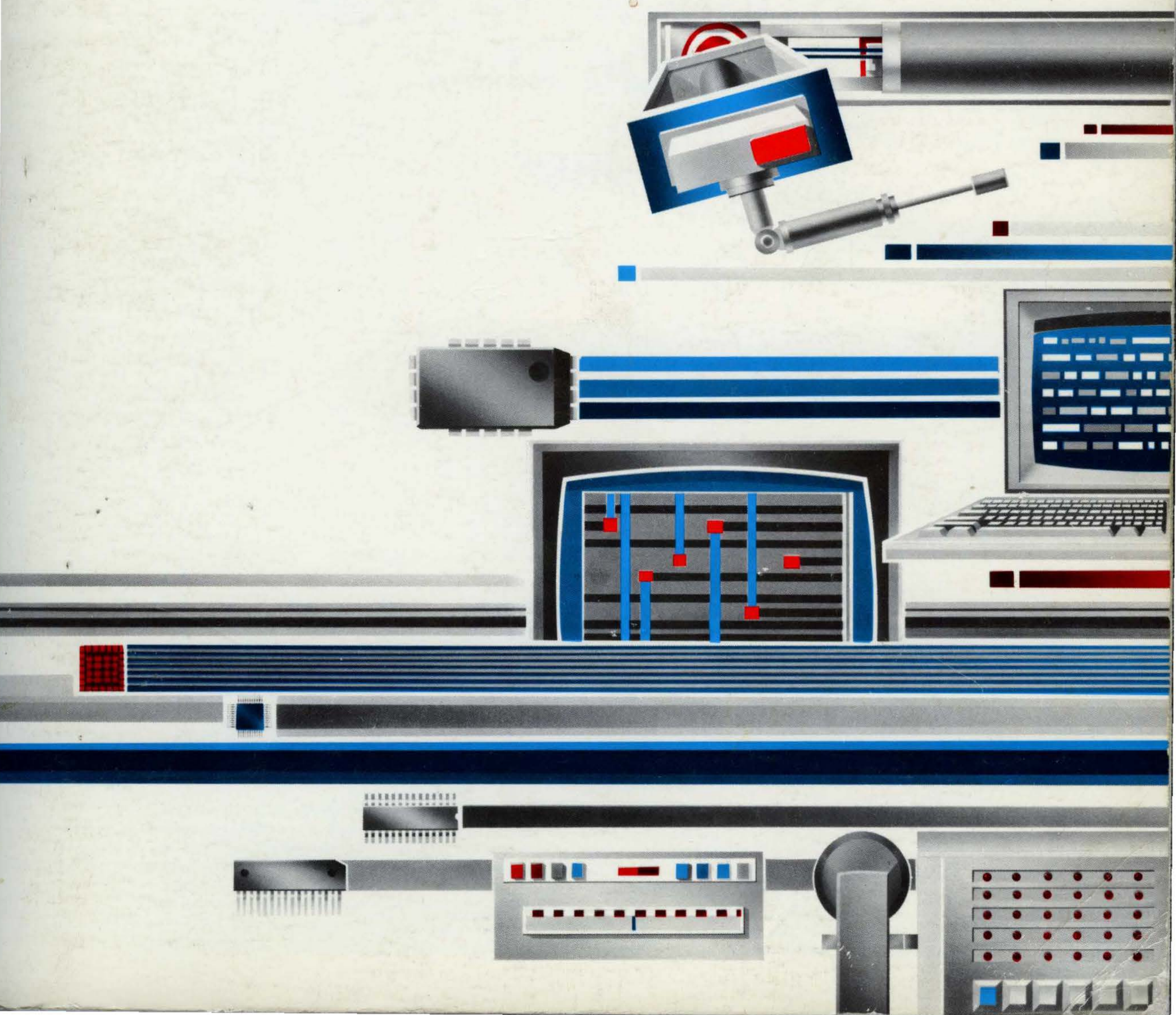
NEC

NEC Electronics Inc.

Memory Products Data Book

1989



MEMORY PRODUCTS DATA BOOK

1989

NECEL-000154
Stock No. 600100
Document No. UIS-UP60000

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GENERAL INFORMATION

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Section 1
General Information

1

Introduction

This 1989 edition of the *MEMORY PRODUCTS DATA BOOK* contains the most current information available at the time of printing. Please contact your local representative of NEC Electronics Inc. to stay informed of upcoming releases. Additional products in development but not yet announced are referred to below. The addition of these products to our total memory line, already the broadest in the industry (and briefly described in this section), means an even greater selection of device types, configurations, and packaging options in each of the major memory groups.

Among our new application-specific products are high-performance devices for graphics, video/TV, communications, image processing, data processing, and other specialized applications. The μPD42274, for example, is able to store 1M bits of data and continues our leadership in the design of dual-port graphics buffers. The μPD43501 is the world's first VLSI device to integrate 1024 channels for time division switching in digital PBX applications. The μPD43608 is the world's first cache subsystem on a chip. Designed with a general-purpose interface to many microprocessors and fabricated with 1.3-μm CMOS technology, it combines all cache functions, peripheral circuitry, and 8K bytes of data storage on a single 132-pin chip—providing a high cache hit ratio in compact packaging. Other new products in this category include a triple-port graphics buffer, a line buffer for communications systems, a 910 x 263 x 4 field buffer for NTSC TV systems, and a 1M-bit silicon file for semiconductor disk storage.

In building on our position as an industry leader in the production of latest-generation DRAMs, we have focused our attention on developing products with higher density, lower power consumption, and faster access times. Five recently released 1M-bit CMOS DRAMs—the μPD421000, μPD421001, μPD421002, μPD424256, and μPD424258—reflect this trend toward higher integration and represent substantial improvements in both access speed and power consumption over our popular 256K-bit NMOS DRAMs. Furthermore, a family of modules based on these 1M-bit DRAMs is being offered with 8- or 9-bit organization and either leaded or socketable mounting options. Packaged in Single Inline Memory Modules (SIMMs™) to enhance reliability and reduce the size, weight and cost of a system, they provide the same high performance at the module level as at the device level. This product family will be extended in 1989 to include five versions of the 4M-bit DRAM—the μPD424100, μPD424101, μPD424102, μPD424400, and μPD424402.

An increasing demand for enlarged program and data memory in applications ranging from point-of-sale systems and numerically controlled machining systems to hand-held computers and portable terminals/word processors has led to our development of low-power CMOS SRAMs, all of which feature advanced circuitry, a short-channel, silicon-gate fabrication process, fast access times, and fully static operation (with no clock or refreshing required). Density will increase to 1M-bit and beyond in our byte-wide SRAMs. Other products with increasing density and improved access times are also planned in this family.

NEC has continued to develop more efficient, super high-speed products for use as cache memory and control storage memory in mainframe computers and IC testers, as evidenced by our announcement of four new bipolar ECL RAMs. These devices have 10K or 100K interfaces and are organized by 1 or 4 bits for compatibility with the memory size and word width of the application system. Additional products, through 256K bits, are in development.

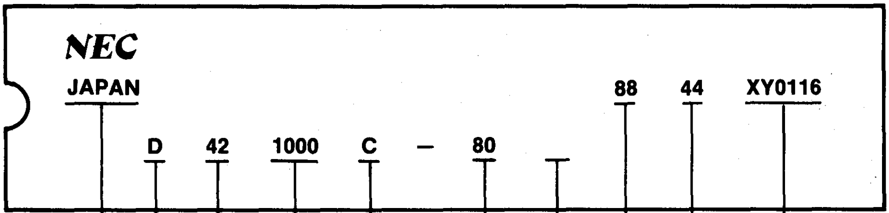
Our family of EPROMs has also been expanded to include EEPROMs and higher-density products offering greater integrity, improved programming features, and a considerable savings in both operating and standby power. Our fast 1M- and 2M-bit EPROMs are in production now, while samples of the 4M-bit EPROM will be available soon after this book is in print.

Five new mask-programmable ROMs featuring very large capacity (as high as 4M bits) and either 8- or 16-bit organization have been developed in response to the growing demand for storing greater quantities of data on one chip, e.g., dictionary and thesaurus data, embedded application routines in portable systems, and large-size character sets/fonts. Future efforts in this area will concentrate on producing denser and faster speed versions for these applications.

This *1989 MEMORY PRODUCTS DATA BOOK* is for your reference. If you need further assistance, please contact one of the sales offices listed elsewhere in this book. Our field applications engineers or personnel in the technology centers will be glad to assist you.

SIMM is a trademark of Wang Laboratories.

Monolithic Part Number Guide



Country of Origin

NEC Control Code

Date Code
Week

Device Type
B = Digital bipolar
D = Digital MOS

Year

Product Class
10 = 10K ECL RAM
100 = 100K ECL RAM
21 = NMOS static RAM
23 = NMOS ROM
23C = CMOS ROM
27 = NMOS EPROM
27C = CMOS EPROM
28C = CMOS EEPROM
4 = Bipolar PROM
40 = NMOS static RAM
41 = NMOS dynamic RAM
42 = CMOS dynamic RAM
43 = CMOS static RAM
44 = CMOS static RAM (6-T cell)

Low Power Indicator [optional]
L = Low power
LL = Very low power

Speed Selection
-10 = 100 ns
-12 = 120 ns
-15 = 150 ns
-70 = 70 ns
-80 = 80 ns
-85 = 85 ns
-XX = Etc.

Device Identifier

Package
B = Ceramic flatpack
C = Plastic DIP
CU = Plastic DIP
CX = Plastic DIP
D = Cerdip or ceramic DIP
DH = Cerdip or ceramic DIP
G = Plastic miniflat
GU = Plastic miniflat
GF = Quad flatpack
K = Ceramic LCC
L = PLCC
LA = Plastic SOJ
LE = Plastic SOJ
R = Ceramic PGA
V = Plastic ZIP

Notes:
(1) The marking format may vary among package types.
(2) Regardless of the format, the device number does not change.
(3) The "μP" in NEC part numbers does not appear on the package.
(4) DIP = dual-inline package
(5) LCC = leadless chip carrier
(6) PLCC = plastic leaded chip carrier
(7) PGA = pin grid array
(8) SOJ = small-outline J-lead package
(9) ZIP = zig-zag inline package

Module Part Number Guide

MC - 42 1000 B 9 A - 80

NEC Memory Module — MC

Product Class — 42
- 41 = NMOS dynamic RAM
- 42 = CMOS dynamic RAM

Word Depth — 1000
- 256 = 256K words
- 1000 = 1024K words

Features — B
- A = Page or fast page
- B = Nibble
- C = Static column

Number of Output Bits — 9

Package Type — A
- A = Leaded SIMM
- B = Socket-mountable SIMM

Speed Selection — 80
- -80 = 80 ns
- -10 = 100 ns
- -12 = 120 ns
- -15 = 150 ns

Product Line Overview

Density	Application Specific	RAM Module	RAM Dynamic	RAM MOS Static	RAM ECL	EPROM	EEPROM	ROM
1K					μPB10422 μPB100422			
4K					μPB10470 μPB10474 μPB10474A μPB100470 μPB100474 μPB100474A		μPD28C04	
8K	μPD41101 μPD41102 μPD42101 μPD42102							
16K	μPD43501			μPD4311 μPD4314	μPB10480 μPB10484 μPB100480 μPB100484			
40K	μPD42505							
64K	μPD43608			μPD4361 μPD4362 μPD4363 μPD4364 μPD4464			μPD28C64	
256K	μPD41264 μPD42232 μPD42532		μPD41256 μPD41257 μPD41464	μPD43254 μPD43256A		μPD27C256A		
512K						μPD27C512		
1M	μPD42270 μPD42601 μPD42273 μPD42274		μPD421000 μPD421001 μPD421002 μPD424256 μPD424258			μPD27C1000A μPD27C1001A μPD27C1024		μPD23C1000A μPD23C1000EA μPD23C1001E μPD23C1010A
2M		MC-41256A8 MC-41256A9				μPD27C2001		μPD23C2000 μPD23C2001
4M								μPD23C4000 μPD23C4001E
8M		MC-421000A8 MC-421000B8 MC-421000C8 MC-421000A9 MC-421000B9 MC-421000C9						

Application-Specific Devices

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW) Standby	Active	Package (Note 1)	Pins
μPD41101-3	910 x 8	NMOS	27	34	+5	—	495	C/G	24
μPD41101-2			27	34(R)/69(W)					
μPD41101-1			49	69					
μPD41102-3	1135 x 8	NMOS	21	28	+5	—	495	C/G	24
μPD41102-2			21	28(R)/56(W)					
μPD41102-1S			27	34					
μPD41102-1			40	56					
μPD41264-12	64K x 4 with	NMOS	120 Port A 40 Port B	220 Port A 40 Port B	+5	66	853	C/V	24
μPD41264-15	dual ports		150 Port A 60 Port B	270 Port A 60 Port B			715		
μPD42101-3	910 x 8	CMOS	27	34	+5	—	385	C/G	24
μPD42101-2			27	34(R)/69(W)			330		
μPD42101-1			49	69			193		
μPD42102-3	1135 x 8	CMOS	21	28	+5	—	440	C/G	24
μPD42102-2			21	28(R)/56(W)			385		
μPD42102-1			40	56			220		
μPD42232-12	32K x 8 with	CMOS	120 Port A 40 Port B	220 Port A 40 Port B	+5	82.5	468	CU	40
μPD42232-15	triple ports		150 Port A 60 Port B	260 Port A 60 Port B			385		
μPD42270	910 x 263 x 4	CMOS	40	60	+5	—	440	C	28
μPD42273-10	256K x 4	CMOS	100 Port A 30 Port B	190 Port A 30 Port B	+5	17.5	550	LE/V	28
μPD42273-12			120 Port A 40 Port B	220 Port A 40 Port B		17.5	495		
μPD42274-10	256K x 4	CMOS	100 Port A 30 Port B	190 Port A 30 Port B	+5	17.5	550	LE/V	28
μPD42274-12			120 Port A 40 Port B	220 Port A 40 Port B		17.5	495		
μPD42505-50	5048 x 8	CMOS	40	50	+5	—	330	C	24
μPD42505-75			55	75					
μPD42532	32K x 8	CMOS	50	100	+5	110	440	C	40
μPD42601-60	1M x 1	CMOS	600 (Single) 100 (Page)	1000 (Single) 200 (Page)	+5	0.660	66	C/LA/V	C = 18 LA = 26/20
μPD42601-60L						0.165	66		V = 20
μPD43501	2 x 1K x 8	CMOS	60	61	+5	—	1485	R	132
μPD43608-3	512 x 32 x 4 or 1K x 16 x 4	CMOS	64	100	+5	—	1485	R	132
μPD43608-2			85	125					

Note:

(1) C = plastic DIP; CU = plastic shrink DIP; G = plastic miniflat; LA or LE = plastic SOJ; R = ceramic PGA; V = plastic ZIP.

Dynamic RAM Modules

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW) Standby	Maximum Power Dissipation (mW) Active	Package (Note 1)	Pins
MC-41256A8-10	256K x 8	NMOS	100	200	+5	220	3652	A/B	30
MC-41256A8-12	(page)		120	220			3080		
MC-41256A8-15			150	260			2640		
MC-41256A9-10	256K x 9	NMOS	100	200	+5	248	4109	A/B	30
MC-41256A9-12	(page)		120	220			3465		
MC-41256A9-15			150	260			2970		
MC-421000A8-80	1M x 8	CMOS	80	160	+5	44	3080	A/B	30
MC-421000A8-10	(fast page)		100	190			2640		
MC-421000A8-12			120	220			2200		
MC-421000B8-80	1M x 8	CMOS	80	160	+5	44	3080	A/B	30
MC-421000B8-10	(nibble)		100	190			2640		
MC-421000B8-12			120	220			2200		
MC-421000C8-80	1M x 8	CMOS	80	160	+5	44	3080	A/B	30
MC-421000C8-10	(static column)		100	190			2640		
MC-421000C8-12			120	220			2200		
MC-421000A9-80	1M x 9	CMOS	80	160	+5	49.5	3465	A/B	30
MC-421000A9-10	(fast page)		100	190			2970		
MC-421000A9-12			120	220			2475		
MC-421000B9-80	1M x 9	CMOS	80	160	+5	49.5	3465	A/B	30
MC-421000B9-10	(nibble)		100	190			2970		
MC-421000B9-12			120	220			2475		
MC-421000C9-80	1M x 9	CMOS	80	160	+5	49.5	3465	A/B	30
MC-421000C9-10	(static column)		100	190			2970		
MC-421000C9-12			120	220			2475		

Note:

(1) A = leaded SIMM; B = socket-mountable SIMM.

Dynamic RAMs

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW) Standby	Maximum Power Dissipation (mW) Active	Package (Note 1)	Pins
µPD41256-10	256K x 1	NMOS	100	200	+5	28	440	C/L	C = 16
µPD41256-12	(page)		120	220			385		L = 18
µPD41256-15			150	260			330		
µPD41257-12	256K x 1	NMOS	120	220	+5	28	413	C/L	C = 16
µPD41257-15	(nibble)		150	260			385		L = 18
µPD41257-20			200	330			330		
µPD41464-10	64K x 4	NMOS	100	200	+5	28	440	C/L/V	C = 18
µPD41464-12			120	220			413		L = 18
µPD41464-15			150	260			385		V = 20
µPD421000-80	1M x 1	CMOS	80	160	+5	5.5	385	C/LA/V	C = 18
µPD421000-10	(fast page)		100	190			330		LA = 26/20
µPD421000-12			120	220			275		V = 20
µPD421001-80	1M x 1	CMOS	80	160	+5	5.5	385	C/LA/V	C = 18
µPD421001-10	(nibble)		100	190			330		LA = 26/20
µPD421001-12			120	220			275		V = 20
µPD421002-80	1M x 1	CMOS	80	160	+5	5.5	385	C/LA/V	C = 18
µPD421002-10	(static column)		100	190			330		LA = 26/20
µPD421002-12			120	220			275		V = 20
µPD424256-80	256K x 4	CMOS	80	160	+5	5.5	385	C/LA/V	C = 20
µPD424256-10	(fast page)		100	190			330		LA = 26/20
µPD425256-12			120	220			275		V = 20
µPD424258-80	256K x 4	CMOS	80	160	+5	5.5	385	C/LA/V	C = 20
µPD424258-10	(static column)		100	190			330		LA = 26/20
µPD425258-12			120	220			275		V = 20

Notes:

(1) C = plastic DIP; L = PLCC; LA = plastic SOJ; V = plastic ZIP.

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Static RAMs

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW) Standby	Maximum Power Dissipation (mW) Active	Package (Note 1)	Pins
μPD4311-35	16K x 1	CMOS	35	35	+5	11	440	C	20
μPD4311-45			45	45					
μPD4311-55			55	55					
μPD4314-35	4K x 4	CMOS	35	35	+5	11	440	C	20
μPD4314-45			45	45					
μPD4314-55			55	55					
μPD4361-40	64K x 1	CMOS	40	40	+5	11	660	K	22
μPD4361-45			45	45				C/K	
μPD4361-55			55	55				C/K	
μPD4361-70			70	70				C	
μPD4362-45	16K x 4	CMOS	45	45	+5	11	495	C	22
μPD4362-55	($\overline{CS}$ only)		55	55					
μPD4362-70			70	70					
μPD4363-45	16K x 4	CMOS	45	45	+5	11	495	C	24
μPD4363-55	($\overline{CS}$, $\overline{OE}$)		55	55					
μPD4363-70			70	70					
μPD4364-10	8K x 8	CMOS	100	100	+5	11/0.55/0.28	248	C/CX/G	28
μPD4364-12			120	120			220	C/CX/G	
μPD4364-15			150	150			220	C/CX/G	
μPD4364-20			200	200			193	C/G	
μPD4464-12	8K x 8	CMOS	120	120	+5	0.055	220	C/G	28
μPD4464-15		(6 - T cell)	150	150		(Note 2)	220		
μPD4464-20			200	200			193		
μPD43254-35	64K x 4	CMOS	35	35	+5	11	660	C	24
μPD43254-45			45	45					
μPD43254-55			55	55					
μPD43256A-85	32K x 8	CMOS	85	85	+5	0.55	248	C/GU	28
μPD43256A-10			100	100			220		
μPD43256A-12			120	120			220		
μPD43256A-15			150	150			193		

Notes:

(1) C = plastic DIP; CX = plastic slim DIP; G or GU = plastic miniflat; K = ceramic LCC.

(2) Lower power version available; refer to the data sheet for more detail.

ECL RAMs

Device	Organization	Process	Address Access Time (ns)	Chip Select Access Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)	Package (Note 1)	Pins
μPB10422-7	256 x 4	10K	7	5 (Note 2)	–5.2	1144	D	24
μPB10422-10			10	5 (Note 2)				
μPB10470-10	4K x 1	10K	10	6	–5.2	1144	D	18
μPB10470-15			15	8				
μPB10474-8	1K x 4	10K	8	5	–5.2	1144	D	24
μPB10474-10			10	6				
μPB10474-15			15	8				
μPB10474A-5	1K x 4	10K	5	3	–5.2	1300	D	24
μPB10474A-7			7	5				
μPB10480-10	16K x 1	10K	10	5	–5.2	1352	B/D	20
μPB10480-15			15	8		1248		
μPB10484-10	4K x 4	10K	10	5	–5.2	1352	B/D	28
μPB10484-15			15	8		1248		
μPB100422-7	256 x 4	100K	7	5 (Note 2)	–4.5	990	B/D	24
μPB100422-10			10	5 (Note 2)				
μPB100470-10	4K x 1	100K	10	6	–4.5	990	D	18
μPB100470-15			15	8				
μPB100474-4.5	1K x 4	100K	4.5	4	–4.5	2025	K	24
μPB100474-6			6	4		2025	B/K	
μPB100474-8			8	5		990	B/D	
μPB100474-10			10	6		990	B/D	
μPB100474-15			15	8		990	B/D	
μPB100474A-5	1K x 4	100K	5	3	–4.5	1125	B/D	24
μPB100474A-7			7	5				
μPB100480-10	16K x 1	100K	10	5	–4.5	1170	B/D	20
μPB100480-15			15	8		1080		
μPB100484-10	4K x 4	100K	10	5	–4.5	1170	B/D	28
μPB100484-15			15	8		1080		

Notes:

(1) B = ceramic flatpack; D = ceramic DIP and cerdip; K = ceramic LCC.

(2) Block select access time (ns).

NEC

EPROMs

Device	Organization	Process	Access Time (ns)	Programming Option	Supply Voltage	Maximum Power Dissipation (mW)		Package (Note 1)	Pins
						Standby	Active		
μPD27C256A-15 μPD27C256A-20	32K x 8	CMOS	150 200	UV	+5 (Note 2)	0.55	165	D	28
μPD27C512-15 μPD27C512-20 μPD27C512-25	64K x 8	CMOS	150 200 250	UV	+5 (Note 2)	0.55	165	D	28
μPD27C1000A-12 μPD27C1000A-15 μPD27C1000A-20	128K x 8 (ROM Comp.)	CMOS	120 150 200	UV	+5 (Note 2)	0.55	220 165 138	D	32
μPD27C1001A-12 μPD27C1001A-15 μPD27C1001A-20	128K x 8 (JEDEC)	CMOS	120 150 200	UV	+5 (Note 2)	0.55	220 165 138	D	32
μPD27C1024-15 μPD27C1024-20 μPD27C1024-25	64K x 16	CMOS	150 200 250	UV	+5 (Note 2)	0.55	275	D	40
μPD27C2001-15 μPD27C2001-17 μPD27C2001-20	256K x 8	CMOS	150 170 200	UV	+5 (Note 2)	0.55	165	D	32

Notes:

(1) D = ceramic DIP with quartz window.

(2) Programming voltage = 12.5 V ±0.3.

EEPROMs

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW)		Package (Note 1)	Pins
						Standby	Active		
μPD28C04-20 μPD28C04-25	512 x 8	CMOS	200 250	200 250	+5	0.55	94	C/G	24
μPD28C64-20 μPD28C64-25	8K x 8	CMOS	200 250	200 250	+5	0.55	275	C	28

Notes:

(1) C = plastic DIP; G = plastic miniflat.

Mask-Programmable ROMs

Device	Organization	Process	Access Time (ns)	Cycle Time (ns)	Supply Voltage	Maximum Power Dissipation (mW) Standby	Active	Package (Note 1)	Pins
μPD23C1000A	128K x 8 ($\overline{CE}$)	CMOS	200	200	+5	0.55	220	C/G	28
μPD23C1000EA	128K x 8 ($\overline{CE}$/$\overline{OE}$)	CMOS	200	200	+5	0.55	220	C	32
μPD23C1001E	128K x 8	CMOS	200	200	+5	0.55	220	C	32
μPD23C1010A	128K x 8 ($\overline{OE}$)	CMOS	200	200	+5	N/A	220	C	28
μPD23C2000	128K x 16 or 256K x 8	CMOS	250	250	+5	0.55	220	C/G	40/52
μPD23C2001	256K x 8	CMOS	250	250	+5	0.55	220	C	32
μPD23C4000	256K x 16 or 512K x 8	CMOS	250	250	+5	0.55	220	C/GF	40/64
μPD23C4001E	512K x 8	CMOS	250	250	+5	0.55	220	C	32

Notes:

(1) C = plastic DIP; G or GF = plastic miniflat.

NEC

Alternate Source Index

AMD	NEC
Am2167	μPD4311
Am2168	μPD4314
Am99C88	μPD4364
Am99C164	μPD4362
Am99C328	μPD43256A
Am99C641	μPD4361
Am27C1024	μPD27C1024
Am2864A	μPD28C64

CYPRESS	NEC
CY7C164	μPD4362
CY7C167	μPD4311
CY7C187	μPD4361
CY7C185	μPD4364
CY7C186	μPD4364
CY7C194	μPD43254
CY7C198	μPD43256A

EXEL	NEC
XLS2864A	μPD28C64

FAIRCHILD	NEC
F10422	μPB10422
F10470	μPB10470
F10474	μPB10474
F100422	μPB100422
F100470	μPB100470
F100474	μPB100474
F100480	μPB100480

FUJITSU	NEC
MB81256	μPD41256
MB81257	μPD41257
MB81464	μPD41464

FUJITSU	NEC
MB81C1000	μPD421000
MB81C1001	μPD421001
MB81C1002	μPD421002
MB81C4256	μPD424256
MB81C67	μPD4311
MB81C68	μPD4314
MB81C71	μPD4361
MB81C74	μPD4362
MB8184	μPD43254
MB8464	μPD4464
MB84256	μPD43256A
MB85225	MC-41256A8
MB85227	MC-41256A9
MBM10422	μPB10422
MBM10470	μPB10470
MBM10474	μPB10474
MBM100422	μPB100422
MBM100470	μPB100470
MBM100474	μPB100474
MBM100480	μPB100480
MBM100484	μPB100484
MBM27C256	μPD27C256A
MBM27C512	μPD27C512
MBM27C1000	μPD27C1000A
MBM27C1024	μPD27C1024
MB61461	μPD41264
MBM28C64	μPD28C64
MB831000	μPD23C1000A
MB831124	μPD23C1000A

HITACHI	NEC
HM50256	μPD41256
HM50257	μPD41257
HM50464	μPD41464
HM511000	μPD421000
HM511001	μPD421001
HM511002	μPD421002
HM514256	μPD424256

HITACHI	NEC
HM6168	μPD4314
HM6264	μPD4364
HM6267	μPD4311
HM6287	μPD4361
HM6208	μPD43254
HM62256	μPD43256A
HB561003	MC-41256A9
HB56A18	MC-421000A8
HB58A19	MC-421000A9
HM10422	μPB10422
HM10470	μPB10470
HM10474	μPB10474
HM100422	μPB100422
HM100470	μPB100470
HM100474	μPB100474
HN27C256	μPD27C256A
HN27301	μPD27C1000A
HN27C1024	μPD27C1024
HM53461	μPD41264
HM534253	μPD42274
HN58C65	μPD28C64
HN62301	μPD23C1000A

HYUNDAI	NEC
HY62C64	μPD28C64

IDT	NEC
IDT6167	μPD4311
IDT7164	μPD4364
IDT7187	μPD4361
IDT7188	μPD4362
IDT71C65	μPD4464
IDT71258	μPD43254
IDT71256	μPD43256A
IDT78C64A	μPD28C64

Alternate Source Index (cont)

INMOS	NEC
IMS1420	μPD4314
IMS1600	μPD4361
IMS1620	μPD4362
IMS1630	μPD4364
IMS1820	μPD43254
IMS1830	μPD43256A

INTEL	NEC
51C67	μPD4311
51C68	μPD4314
27010	μPD27C1001A
27210	μPD27C1024
27C256	μPD27C256A
2864A	μPD28C64

LATTICE	NEC
SR64K1	μPD4361
SR64K4	μPD4362
SR64K8	μPD4364
SR256K4	μPD43254
SR256K8	μPD43256A

MITSUBISHI	NEC
M5M4256	μPD41256
M5M4257	μPD41257
M5M4464	μPD41464
M5M4C1000	μPD421000
M5M4C1001	μPD421001
M5M4C1002	μPD421002
M5M4C256	μPD424256
M5M21C67	μPD4311
M5M21C68	μPD4314
M5M5164	μPD4464
M5M5165	μPD4364
M5M5256	μPD43256A
M5M5258	μPD43254
M5M27C256	μPD27C256A
M5M27512	μPD27C512

MITSUBISHI	NEC
M5M4C264	μPD41264
M5M442256	μPD42274

MOTOROLA	NEC
MCM6168	μPD4314
MCM6187	μPD4361
MCM6188	μPD4362
MCM10422	μPB10422
MCM10470	μPB10470
MCM10474	μPB10474
MCM100422	μPB100422
MCM100470	μPB100470
MCM100474	μPB100474

NATIONAL	NEC
DM10422	μPB10422
DM10470	μPB10470
DM10474	μPB10474
DM100422	μPB100422
DM100470	μPB100470
DM100474	μPB100474

OKI	NEC
MSM27C256	μPD41256
MSM41257	μPD41257
MSM514252	μPD42274

PERFORMANCE	NEC
P4C164	μPD4364
P4C187	μPD4361
P4C188	μPD4362

SEEQ	NEC
27C256	μPD27C256A
28C64	μPD28C64
2804A	μPD28C04

TI	NEC
TMS4256	μPD41256
TMS4257	μPD41257
TMS4464	μPD41464
TMS4C1024	μPD421000
TMS4C1025	μPD421001
TMS4C1027	μPD421002
TMS44C256	μPD424256
TMS27C256	μPD27C256A
TMS4461	μPD41264
TMS44C251	μPD42274

TOSHIBA	NEC
TMM41256	μPD41256
TMM41257	μPD41257
TMM41464	μPD41464
TC511000	μPD421000
TC511001	μPD421001
TC511002	μPD421002
TC514256	μPD424256
TC5561	μPD4361
TC5564	μPD4464
TC5565	μPD4364
TC55257	μPD43256A
THM81000	MC-421000A8
THM91000	MC-421000A9
TC57256	μPD27C256A
TC571000	μPD27C1000A
TC571024	μPD27C1024
TC524256	μPD42274
TC531000	μPD23C1000A

XICOR	NEC
X24C04	μPD28C04
X28C64	μPD28C64

NEC

QUALITY AND RELIABILITY

2

NEC

Section 2
Quality and Reliability

QUALITY AND RELIABILITY

Introduction

As large-scale integration reaches a higher level of density, reliability of devices imposes a profound impact on system reliability. And as device reliability becomes a major factor, test methods to assure acceptable reliability become more complicated. Simply performing a reliability test according to a conventional method cannot satisfy the demanding requirements for higher reliability. At these new, higher levels of LSI density, it is increasingly difficult to activate all the elements in the internal circuits. A different philosophy and methodology is needed for reliability assurance. Moreover, as integration density increases, the degradation of internal elements in an LSI device is seldom detected by measuring characteristics across external terminals.

In order to improve and guarantee a certain level of reliability for large-scale integrated circuits, it is essential to build quality and reliability into the product. Then, the conventional reliability tests are followed to ensure that the product demonstrates an acceptable level of reliability.

NEC has introduced the concept of total quality control (TQC) across its entire semiconductor product line. By adopting TQC, NEC can build quality into the product and thus assure higher reliability. The concept and methodology of total quality control are company-wide activities involving workers, engineers, quality control staffs, and all levels of management.

NEC has also introduced a prescreening method into the production line that helps eliminate potentially defective units. The combination of building quality in and screening projected early failures out has resulted in superior quality and excellent reliability.

Most large-scale integrated circuits utilize high-density, MOS technology. State-of-the-art high performance has been achieved by introducing fine-line generation techniques. By reducing physical parameters, circuit density and performance increase while active circuit power dissipation decreases. The data presented here shows that this advanced technology yields products as reliable as those from previous technologies.

Reliability Testing

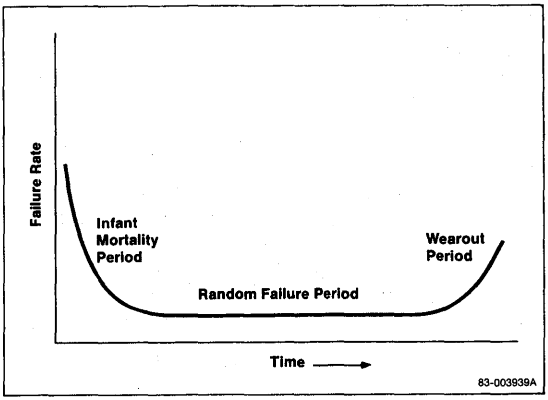
Reliability is defined as the characteristics of an item expressed by the probability that it will perform a required function under stated conditions for a stated period of time. This involves the concept of probability, definition of required function(s), and the critical time used in defining the reliability.

Definition of a required function, by implication, treats the definition of a failure. Failure is defined as the termination of the ability of a device to perform its required function. Furthermore, a device is said to have failed if it shows inability to perform within guaranteed parameters as given in an electrical specification.

Discussion of reliability and failure can be approached in two ways: with respect to systems or to individual devices. The accumulation of normal device failure rates constitutes the expected failure rate of the system hardware. Important considerations here are the constant failure period, the early failure (infant mortality) period, and overall reliability level. With regard to individual devices, areas of prime interest include specific failure mechanisms, failures in accelerated tests, and screening tests.

Some of these failure considerations pertain to both systems and devices. The probability of no failures in a system is the product of the probability of no failure in each of its components. The failure rate of system hardware is then the sum of the failure rates of the components used to construct the system.

Figure 1. Reliability Life (Bathtub) Curve



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Life Distribution

The fundamental principles of reliability engineering predict that the failure rate of a group of devices will follow the well-known bathtub curve in figure 1. The curve is divided into three regions: infant mortality, random failures, and wearout failures.

Infant mortality, as the name implies, represents the early-life failures of devices. These failures are usually associated with one or more manufacturing defects.

After some period of time, the failure rate reaches a low value. This is the random failure portion of the curve, representing the useful portion of the life of a device. During this random failure period, there is a decline in the failure rate due to the depletion of potential random failures from the general population.

The wearout failures occur at the end of the device's useful life. They are characterized by a rapidly rising failure rate over time as devices wear out both physically and electrically.

Thus, for devices that have very-long life expectancies compared to those of systems, the areas of concern will be the infant mortality and the random failure portions of the population.

The system failure rates are related to the collective device failure rates. In a given system, after elimination of the early failures, the system will be left to the failure rate of its components. In order to make proper projections of the failure rate in the operating environment, time-to-failure must be accelerated in tests in a predictable way.

Failure Distribution at NEC

Integrated circuits returned to NEC from the field underwent extensive failure analysis at NEC's Integrated Circuit Division.

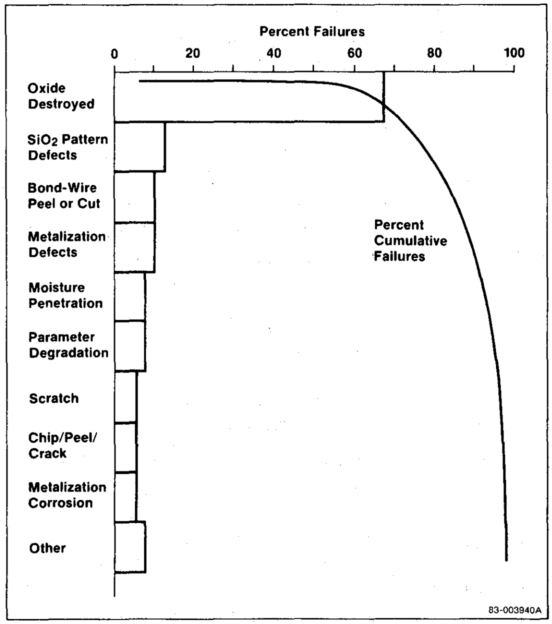
First, approximately 50 percent of the field returns were found to be damaged either from improper handling or misuse of the devices. These units were eliminated from the analysis. The remaining failed units were classified by their failure mechanisms as depicted in figure 2. These failures were then related to the major integrated circuit failure mechanisms and to their origins in a particular manufacturing step.

As shown in figure 2, the first four failure mechanisms accounted for more than 90 percent of total failures. As a result, NEC improved processes and material to reduce these failures. Additionally, NEC introduced screening procedures to detect and eliminate defective devices.

Temperature, humidity, and bias tests are used for testing the moisture resistance of plastic encapsulated integrated circuits. NEC developed a special process to improve the plastic encapsulation material. As a result, moisture-related—thus packaging-related—failures have been drastically reduced.

As a preventive measure, NEC has introduced a special screening procedure embedded in the production line. A burn-in at an elevated temperature is performed for 100 percent of the lots. This burn-in effectively removes the potentially defective units. In addition, improvement of the plastic encapsulation material has lowered the failures in a high-temperature and high-humidity environment.

Figure 2. Failure Distribution of MOS Integrated Circuits



Accelerated Reliability Testing

As an example, assume that an electronic system contains 1000 integrated circuits and can tolerate 1 percent system failures per month. The failure rate per component is:

$$\frac{0.01 \text{ Failures}}{720\text{K Device Hours}} = 13.888 \times 10^{-9} \text{ Failures/Hour or } 13.8888 \text{ FITs}$$

where FIT = Failure units per 10^9 device hours

To demonstrate this failure rate, note that 13.8888 FITs corresponds to one failure in about 7000 devices during an operating test of 10,000 hours. It is quickly apparent that a test condition is required to accelerate the time-to-failure in a predictable and understandable way. The implicit requirement for the accelerated stress test is that the relationship between the accelerated stress testing condition and the condition of actual use be known.

A most common time-to-failure relationship involves the effect of temperature, which accelerates many physiochemical reactions leading to device failure. Other environmental conditions are voltage, current, humidity, vibration, or some combination of these. Table 1 lists the reliability assurance tests performed at NEC for integrated circuits.

Table 1. Monthly NEC Reliability Tests

Test	MIL-STD-883 Method	Test Conditions
Life Test		
High-temperature, operating	1005	T_A = 100 to 125 °C for 1000 hours
High-temperature, storage	1008	T_A = 150 °C for 1000 hours
High-temperature, high-humidity test	—	T_A = 85 °C at 85% RH for 1000 hours
Pressure cooker test	—	T_A = 125 °C at 2.3 atm for 168 hours
Environmental Test		
Soldering heat test	2031 (MIL-STD-750)	T = 260 °C for 10 s without flux
Temperature cycle	1010	T = −65 to +150 °C for 10 cycles
Thermal shock	1011	T = 0 to 100 °C for 15 cycles
Lead fatigue	2004	at 250 gm: 3 leads, 3 bends
Solderability	2003	T = 230 °C for 5 s with flux

Temperature Effect. The effect of temperature that concerns us is that which responds to the Arrhenius relationship. This relates the reaction rate to temperature.

$$R = R_o \exp(-E_a/kT)$$

where R_o = Constant
E_a = Activation energy in eV
k = Boltzmann's constant
= 8.617×10^{-5} eV/K
T = Absolute temperature in kelvin (K)

The significance of this relationship is that the failure mechanisms of semiconductor devices are directly applicable to it. A linear relationship between failure mechanism and time is assumed.

Activation Energy. Associated with each failure mechanism is an activation energy value. Table 2 lists some of the more common failure mechanisms and the associated activation energy of each.

Table 2. Activation Energy and Detection of Failure Mechanisms

Failure Mechanism	Activation Energy	Detection
Oxide defect	0.3 eV	High-temperature operating life test
Silicon defect	0.3 eV	
Ionic contamination	1.0-1.35 eV	
Electromigration	0.4-0.8 eV	
Charge injection	1.3 eV	
Gold-aluminum interface	0.8 eV	
Metal corrosion	0.7 eV	High-humidity operating life test

High-Temperature Operating Life Test. This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125 °C. The data obtained is translated to a lower temperature by using the Arrhenius relationship.

High-Temperature and High-Humidity Test. Semiconductor integrated circuits are highly sensitive to the general accelerating effect of humidity in causing electrolytic corrosion between biased lines. The high-temperature and high-humidity test is performed to detect failure mechanisms that are accelerated by these conditions. This test is effective in accelerating leakage-related failures and drifts in device parameters due to process instability.

High-Temperature Storage Test. Another common test is the high-temperature storage test in which devices are subjected to elevated temperatures with no applied bias. This test is used to detect mechanical problems and process instability.

Environmental Test. Other environmental tests are performed to detect problems related to the package, material, susceptibility to extremes in environment, and problems related to usage of the devices.

Failure Rate Calculation and Prediction

Analysis of integrated circuit failure rates can serve many useful purposes. For example, the early-life failure rate helps establish a warranty period, while the mature-life failure rate aids in estimating repair costs, spare parts stock requirements, or product downtime. Accurate prediction of failure rates can also be used for process control.

The following sections describe the failure rate calculation and prediction methods used by NEC's Integrated Circuit Division.

The Arrhenius Model

Most integrated circuit failure mechanisms depend to some degree on temperature. This relationship can be represented by the Arrhenius model, which includes the effects of temperature and activation energy of the failure mechanisms.

As applied to accelerated life testing of integrated circuits, the Arrhenius model assumes that degradation of a performance parameter is linear with time. Temperature dependence is taken to be the exponential function that defines the probability of occurrence. The relationship of failure rate to temperature is expressed as:

$$F_1 = F_2 \exp[(E_a/k) \times (1/T_1 - 1/T_2)]$$

Where:
F_2 = Failure rate at T_2
F_1 = Failure rate at T_1
E_a = Activation energy in eV
k = Boltzmann's constant
T = Operating junction temperature in kelvin (K)

The equation explains the thermal dependence of integrated circuit failure rates and is used for derating the resulting failure rate to a more realistic temperature.

Acceleration Factor

The acceleration factor is the factor by which the failure rate can be accelerated by increased temperature. This factor is derived from the Arrhenius failure rate expression, resulting in the following form.

$$A = F_1/F_2 = \exp[(E_a/k) \times (1/T_1 - 1/T_2)]$$

where
A = Acceleration factor
F_2 = Failure rate at T_2
F_1 = Failure rate at T_1

In calculating the field reliability of an integrated circuit, it is necessary to calculate the junction temperature. In general, the junction temperature will depend on the ambient temperature, cooling, package type, operating cycle time, and power dissipation of the circuit itself. In these terms, the junction temperature (T_J) is expressed as:

$$T_J = T_A + P_d A_f \theta_{JA}$$

where
T_J = Junction temperature
T_A = Ambient temperature
P_d = Power dissipation
A_f = Air flow factor
θ_{JA} = Package thermal resistance

Table 3 lists derating factors of various failure mechanisms. This table is generated assuming that an accelerated test is performed at a junction temperature of 125°C. The result is then derated to 55°C junction temperature. The acceleration factor may then be obtained by taking the inverse of the derating factor.

Table 3. Derating Factors of Failure Mechanisms

Failure Mechanisms	Activation Energy, eV	Derating Factor
Oxide defect	0.3	0.1546
Silicon defect	0.3	0.1546
Ionic contamination	1.0	0.001984
Electromigration	0.4	0.08307
Charge injection	1.3	0.0003067
Metal corrosion	0.7	0.01315
Gold-aluminum interface	0.8	0.006886

The acceleration of failure mechanisms in a high-humidity and high-temperature environment must be expressed as a function not only of temperature but also of humidity.

According to the reliability test statistics, the acceleration factor in such an environment can best be approximated with Peck's model as follows.

$$A = \exp[(E_a/k) \times (1/T_1 - 1/T_2)] \times (H_2/H_1)^{4.5}$$

where E_a = Activation energy
k = Boltzmann's constant
T = Junction temperature
H = Relative humidity

For example, the acceleration factor for high-humidity and high-temperature or pressure cooker tests ranges from 100 to 1000 times that of the normal operating environment.

Failure Rate Calculation

As an example, suppose that product samples are submitted to a 1000-hour life test at 125°C junction temperature and two failures are encountered: one oxide and one metalization defect. The sample size is 885 units.

Thus, the oxide failure rate is 0.11 percent per 1000 hours and the metalization failure rate is 0.11 percent per 1000 hours. Therefore, the total failure rate at 125°C sums to 0.22 percent per 1000 hours at 1K hours.

Failure Rate Prediction

To derate these failure rates to a normal operating environment, use the derating factors listed in table 3.

Oxide failures = 0.11 x 0.1546 = 0.01701% per 1K hrs
Metal failures = 0.11 x 0.01315 = 0.00145% per 1K hrs
Total failures = 0.01846% per 1K hrs

Note that the example above is a snapshot of the high-temperature life test performed on a particular lot. It is not accumulated data that can be used to represent overall reliability. This conservative illustration, however, shows that the failure rate in a normal operating environment is approximately one-twelfth the failure rate in a higher-temperature environment.

The failure rate prediction takes different activation energies into account whenever the causes of failures are known through performing failure analysis. In some cases, however, an activation energy is assumed in order to accomplish a quick first-order approximation. To yield a conservative estimate of failure rates, NEC assumes an average activation energy of 0.7 eV whenever the exact failure mechanism is not known.

Reliability Test Results

Before introducing new technologies or products, NEC's internal reliability goals must be attained. Several categories of testing are used in the internal qualification program to assure that product reliability meets NEC's reliability goals. Once the product is qualified, its reliability level is regularly monitored in a monthly reliability test.

NEC's Goals on Failure Rates

NEC's approach to achieving high reliability is to build quality into the product, as opposed to merely screening out defective units. The use of distributed control methods embedded in the production line, in conjunction with conventional screening methods, results in the highest reliability at the lowest cost.

NEC's maximum failure rate goals for infant mortality and long-term device operation are listed in table 4.

Table 4. Infant Mortality and Long-Term Failure Rates

Type	Failure Rate Percent/1000 Hours
Infant mortality	0.10 max
Long-term	
1.2M device hours average	0.02 max
3.0M device hours average	0.01 max

Infant Mortality Failure Rate

The infant mortality goal for each product group is set at 0.10 percent maximum. When a failure rate exceeds this level, there is prompt remedial action.

Long-Term Failure Rate

The long-term failure rate goal is based on the following conditions:

- A minimum of 1.2 million device hours at 125°C is accumulated to resolve 0.02 percent per 1000 hours at 55°C with a 60-percent confidence level.
- A minimum of 3 million device hours at 125°C is accumulated to resolve 0.01 percent per 1000 hours at 55°C with a 60-percent confidence level.

Infant Mortality Failure Screening

It is logical to assume the integrated circuit that fails at one temperature would also fail at another temperature, except it would fail sooner at a higher temperature. As can be expected, the failure rate is a function of activation energy. Establishing infant mortality screening, therefore, requires knowledge of the likely failure mechanisms and their associated activation energy.

The most likely mechanisms associated with infant mortality failures are generally manufacturing defects and process anomalies. These generally consist of contamination, cracked chips, wire bond shorts, or bad wire bonds. Since these describe a number of possible mechanisms, any one of which might predominate at a given time, the activation energy for infant mortality might be expected to vary considerably.

The effectiveness of a screening condition, preferably at some stress level in order to shorten the time, varies greatly with the failure mechanism being screened for. Another factor is the economics of the screening process introduced into the production line. Optimal conditions and duration of a screening process will be a compromise of these two factors.

For example, failures due to ionic contamination have an activation energy of approximately 1.0 eV. Therefore, a 15-hour stress at 125°C junction temperature would be the equivalent of approximately 90 days of operation at a junction temperature of 55°C. On the other hand, failures due to oxide defects have an activation energy of approximately 0.3 eV, and a 15-hour stress at 125°C junction temperature would be the equivalent of approximately one week's operation at 55°C junction temperature. As indicated by this, the condition and duration of infant mortality screening would be a strong function of the allowable component failures, hence the system failure, in the field.

Empirical data, gathered over more than a year at NEC, indicates that early failure does occur after less than 4 hours of stress at 125°C ambient temperature. This fact is supported by the life test of the same lot, where the failure rate shows random distribution, as opposed to a decreasing failure rate that then runs into the random failure region.

NEC has adopted the initial infant mortality burn-in at 125°C as a standard production screening procedure. As a result, the field reliability of NEC devices is an order of magnitude higher than the goals set for NEC's integrated circuit products.

Life Tests

The most significant difference between NEC's products and those of other integrated circuit manufacturers is that NEC's have been prescreened for their infant mortality defects. The products delivered to customers are operating at the beginning of the random failure region of the life curve. The life test data also reflects this fact, as will be shown.

The failure mechanism distribution from field failures, as previously shown in figure 2, also contains a very low percentage due to infant mortality. The majority of failures are long-term life failures, and these can be eliminated by stringent process control. Usually, these failure mechanisms have low activation energy associated with them.

Another significant improvement devised by NEC is plastic encapsulation and passivation. As a result, NEC products show excellent reliability in both high-humidity and high-temperature environments. Following is life test data accumulated over more than a year for large-scale integrated circuits.

High-Temperature Operating Life Test

This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. For large-scale integrated circuits, the failure rate is 0.242 percent per 1000 hours at 125°C. This is equivalent to 0.0071 percent per 1000 hours in an operating environment of 55°C (table 5).

Table 5. High-Temperature Operating Life Test

Number of Samples	Number of Failures at				
	48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
3317	0	0	1	4	3

Total number of failures at 1K hrs = 8
Failure rate at 1K hrs at 125°C = 0.242% per 1K hrs
Projected failure rate at 1K hrs at 55°C = 0.007% per 1K hrs

High-Temperature and High-Humidity Life Test

This test is used to accelerate failure mechanisms by operating the devices at high temperature and high humidity. Leakage-related failures and device parameter drift are accelerated by this test. For these large-scale integrated circuits, the failure rate is 0.091 percent per 1000 hours. This is equivalent to 0.0027 percent per 1000 hours in an operating environment of 55°C. The test conditions are T_A = 85°C and relative humidity (RH) = 80% (table 6).

Table 6. High-Temperature and High-Humidity Life Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2190	0	0	0	0	2

Total number of failures at 1K hrs	= 2
Failure rate at 1K hrs at 85°C/80% RH	= 0.091% per 1K hrs
Projected failure rate at 1K hrs at 55°C/60% RH	= 0.003% per 1K hrs

High-Temperature Storage Life Test

This test is effective in accelerating the failure mechanisms related to mechanical reliability problems and process instability. For these LSI devices, the failure rate is 0.207 percent per 1000 hours at 125°C. This is equivalent to 0.0061 percent per 1000 hours in an operating environment of 55°C (table 7).

Table 7. High-Temperature Storage Life Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2410	0	0	0	1	4

Total number of failures at 1K hrs	= 5
Failure rate at 1K hrs at 125°C	= 0.207% per 1K hrs
Projected failure rate at 1K hrs at 55°C	= 0.006% per 1K hrs

Pressure Cooker Test

This test is effective in accelerating failure mechanisms related to metalization corrosion due to moisture. The failure rate is 0.52 percent per 1000 hours at T_A = 125°C and 2.3 atm at 100 percent humidity. This is equivalent to 0.0013 percent per 1000 hours at 55°C and an environment of 60 percent humidity (table 8).

Table 8. Pressure Cooker Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
1718	0	4	5	No test performed	

Total number of failures at 168 hrs	= 9
Failure rate at 125°C	= 0.54% per 1K hrs
Projected failure rate at 55°C	= 0.001% per 1K hrs

Life Test Data Summary

Table 9 summarizes the life test results and projected failure rates in the normal operating environment. The failure rate shows random distribution as opposed to a decreasing failure rate. This is a result of infant mortality screening.

Table 9. Life Test Data

Test Time	Number of Samples	Number of Failures at 96 hrs	168 hrs	500 hrs	1K hrs	Total Number of Failures
High-temperature life test	3317	0	1	4	3	8
High-humidity life test	2190	0	0	0	2	2
High-temperature storage life test	2410	0	0	1	4	5
Pressure cooker test	1718	4	5	No test performed		9
Total	9635	4	6	5	9	24

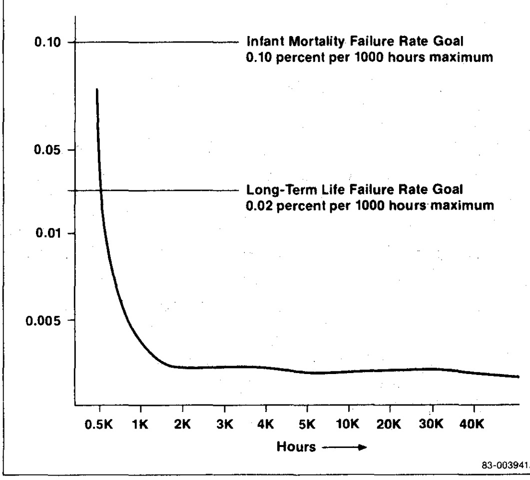
The projected failure rate in the normal operating environment is calculated assuming that the average activation energy is 0.7 eV.

Figure 3 shows the life distribution of NEC integrated circuits as a form of the bathtub curve.

This life test data shows improvements of approximately an order of magnitude better than NEC's goal. The hours of operation are equivalent to the normal operating environment. Wear-out failures, which had been the main target for reliability improvement, have also been significantly reduced. This result comes mainly from process improvements and stringent manufacturing process control.

NEC's main goal has been to improve reliability with respect to infant mortality and long-term life failures. This can be achieved by introducing an effective screening method for infant mortality and building quality into the product.

Figure 3. Plot of Life Test Results



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Thermal Stress Tests

Temperature cycling and thermal shock test the thermal compatibility of material and metal used to make integrated circuits. Table 10 lists the reliability test results of thermal stress tests.

Table 10. Thermal Stress Tests

Test Item	Number of Samples	Number of Failures
Soldering heat test $T_A = 260°C$ for 10 seconds	1891	0
Temperature cycle $T_A = -65$ to $+150°C$, 10 cycles	1891	0
Thermal shock test $T_A = 0$ to $+100°C$, 15 cycles	1891	0

Mechanical Stress Tests

In addition to the device life test, NEC performs mechanical stress tests to detect reliability problems related to the package, material, and device susceptibility to an extreme environment. Table 11 lists mechanical stress test results.

Table 11. Mechanical Stress Tests

Test Item	Number of Samples	Number of Failures
Mechanical shock test at 15 kg, 3 axis	315	0
Vibration test at 100 Hz to 2 kHz, 20 g	315	0
Constant acceleration at 20 kg, 3 axis	315	0
Lead fatigue test at 240 grams	538	0
Solderability test at 230°C for 5 seconds	638	0

Built-In Quality and Reliability

As large-scale integration reaches even higher levels of density, simple quality inspections cannot assure adequate levels of product quality and reliability. In order to ensure the reliability of state-of-the-art VLSI, NEC has adopted another approach. Highest reliability and superior quality of a device can only be achieved by building these characteristics into the product at each process step. NEC, therefore, has introduced the notion of total quality control (TQC) into its entire semiconductor production line. Quality control is distributed into each process step and then summed to form a consolidated system.

Approaches to Total Quality Control

First, the quality control function is embedded into each process. This method enables early detection of possible causes of failure and immediate feedback.

Second, the reliability and quality assurance policy is an integral part of the entire organization. This enables a companywide quality control activity. At NEC, everyone in the company is involved with the concept and methodology of total quality control.

Third, there is an ongoing research and development effort to set even higher standards of device quality and reliability.

Fourth, extensive failure analysis is performed periodically and corrective actions are taken as preventive measures. Process control is based on statistical data gathered from this analysis.

The goal is to maintain the superior product quality and reliability that has become synonymous with the NEC name. The new standard is continuously upgraded and the iterative process continues.

Implementation of Distributed Quality Control

Building quality into a product requires early detection of possible causes of failure at each process step. Then, immediate feedback to remove the causes is a must. A fixed station quality inspection is often lacking in immediate feedback. It is, therefore, necessary to distribute quality control functions to each process step, including the conceptual stage. NEC has implemented a distributed quality control function at each step of the process. Following is a breakdown of the significant steps:

- Product development phase
- Wafer processing
- Chip mounting and packaging
- Electrical testing and thermal aging
- Incoming material inspection

Product Development Phase. The product development phase includes conception of a product, review of the device proposal, organization and physical element design, engineering evaluation, and finally, transfer of the product to manufacturing. Quality and reliability are considered at every step. More significantly, at the design review stage and prior to product transfer, the quality and reliability requirements have to be examined and determined to be satisfactory. This often adds 2 to 3 months to the product development cycle. Building in high reliability, however, cannot be sacrificed.

Wafer Processing Stage Inspection. The in-process quality inspections that occur at the wafer fabrication stage are listed in table 12.

Table 12. Wafer Processing Inspection

Process	Inspection Item
Wafer	Resistivity, dimension, and appearance, (lot sampling inspection)
Mask	
Photolithography	Alignment and etching (100% inspection)
Cleaning	
Diffusion and oxidation	Oxide thickness, sheet resistivity (lot sampling inspection)
Metalization and passivation	Thickness, V_{th}, C-V characteristics (lot sampling)
Wafer sort and scribe	Dc parameters (100% inspection)
Die sort	100% visual inspection

Chip Mounting and Packaging. The in-process quality inspections done at the chip mounting and packaging stage are listed in table 13.

Table 13. Chip Mounting and Packaging Inspection

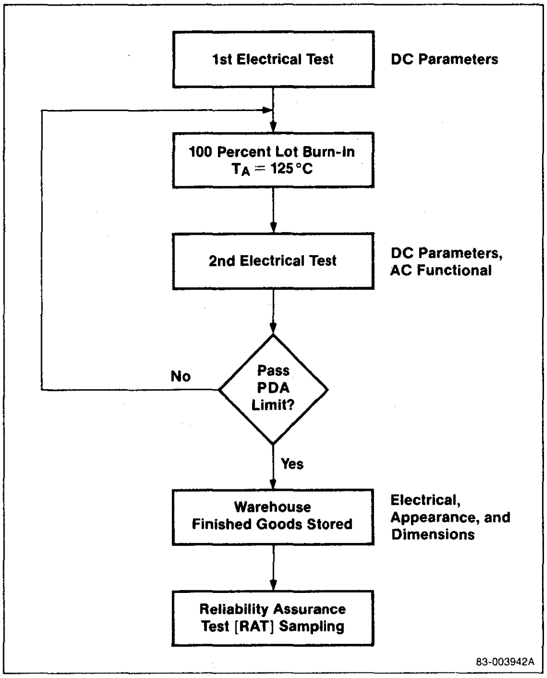
Process	Inspection Item
Die	Incoming material Inspection
Die attach	Appearance (lot sampling inspection)
Wire bonding	Bond strength, appearance (lot sampling)
Packaging	100% appearance inspection
Fine leak*	Lot sampling
Gross leak*	100% inspection

*For ceramic package devices only.

Electrical Testing and Screening. Electrical testing and infant mortality screening are performed at this stage. A flowchart of the process is depicted in figure 4.

At the first electrical test, dc parameters are tested according to the electrical specifications on 100% of each lot. This is a prescreening prior to the infant mortality test. At the second electrical test, ac functional tests as well as dc parameter tests are performed on 100% of the subjected lot. If the percentage of defective units exceeds the limit, the lot is subjected to an additional burn-in. During this time, the defective units are undergoing a failure analysis, the results of which are then fed back into the process for corrective action.

Figure 4. Electrical Testing and Screening



Incoming Material Inspection. Prior to warehouse storage, lots are subjected to an incoming inspection according to the following sampling plan.

• Electrical test:	Dc parameters	LTPD	3%
	Functional test	LTPD	3%
• Appearance		LTPD	3%

Reliability Assurance Test

Samples are continually taken from the warehouse and subjected to monthly reliability tests as discussed previously. They are taken from similar process groups so that it can be assumed that any device is representative of the reliability of the group.

In-Process Screening

Perhaps the most significant preventive measure that NEC has implemented is the introduction of 100% burn-in as an integral part of the standard production process. Most of the potential infant failures are effectively screened from every lot, thereby improving reliability. Assuming average activation energy of 0.7 eV, burn-in at $T_A = 125\,°C$ for 4 hours is equivalent to a week's operation in a normal operating environment. This appears to be ample time for accelerating the time-to-failure mechanisms for early failures.

Process automation, as previously mentioned, has also contributed a great deal toward improving reliability. Since its introduction, assembly related failure mechanisms have been substantially reduced. And, in combination with in-process screening and materials improvement, it has helped establish quality and reliability above NEC's initial goals.

Summary and Conclusion

As has been discussed, building quality and reliability into products is the most efficient way to ensure product reliability. NEC's approach of distributing quality control functions to process steps, then forming a consolidated quality control system, has produced superior quality and excellent reliability.

Prescreening, introduced as an integral part of large-scale integrated circuit protection, has been a major factor in improving reliability. The most recent year's production clearly demonstrates continuation of NEC's high reliability and the effectiveness of this method.

Reliability assurance tests (RATs), performed monthly, have ensured high outgoing quality levels. The combination of building quality into products, effective prescreening of potential failures, and the reliability assurance test has established a singularly high standard of quality and reliability for NEC's large-scale integrated circuits.

With a companywide quality control program, NEC is committed to building superior quality and highest reliability into all its products. Through continuous research and development activities, extensive failure analysis, and process improvements, a higher standard of quality and reliability will continuously be set and maintained.

APPLICATION-SPECIFIC DEVICES

Section 3
Application-Specific Devices

NEC Electronics Inc.

μPD41101
910 x 8-BIT
LINE BUFFER FOR NTSC TV

Description

The μPD41101 is a 910-word by 8-bit line buffer fabricated with the N-channel silicon-gate process. The device helps to create an NTSC flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD41101 can also be used as a digital delay line. The delay length is variable from 10 bits (at maximum clock speed) to 910 bits.

Features

- ☐ 910-word x 8-bit organization
- ☐ Line buffer for NTSC, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operation
- ☐ 1H (910-bit) delay line capability
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single 5-volt ±10% power supply
- ☐ 300-mil, 24-pin plastic DIP and 450-mil, 24-pin plastic miniflat packaging

Ordering Information

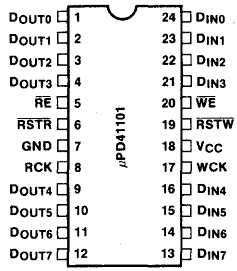
Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD41101C-3	34 ns	34 ns	24-pin plastic DIP
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD41101G-3	34 ns	34 ns	24-pin plastic miniflat
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Identification

Symbol	Function
D_{IN0}-D_{IN7}	Write data inputs
D_{OUT0}-D_{OUT7}	Read data outputs
$\overline{\text{RSTW}}$	Write address reset input
$\overline{\text{RSTR}}$	Read address reset input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{RE}}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

Pin Configuration

24-Pin Plastic DIP or Miniflat



83-003653A

Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{\text{RSTW}}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0 if $\overline{\text{WE}}$ is also at a low level. If $\overline{\text{WE}}$ is at a high level when the $\overline{\text{RSTW}}$ input is brought low, the internal write address is set to 909. The state of this input is strobed by the rising edge of WCK.

$\overline{\text{RSTR}}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0 if $\overline{\text{RE}}$ is also at a low level. If $\overline{\text{RE}}$ is at a high level when the $\overline{\text{RSTR}}$ input is brought low, the internal read address is set to 909.

$\overline{\text{WE}}$ [Write Enable Input]

This input controls write operation. If $\overline{\text{WE}}$ is at a low level, all write cycles proceed. If $\overline{\text{WE}}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{\text{WE}}$ is strobed by the rising edge of WCK.

$\overline{RE}$ [Read Enable Input]

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK [Read Clock Input]

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram

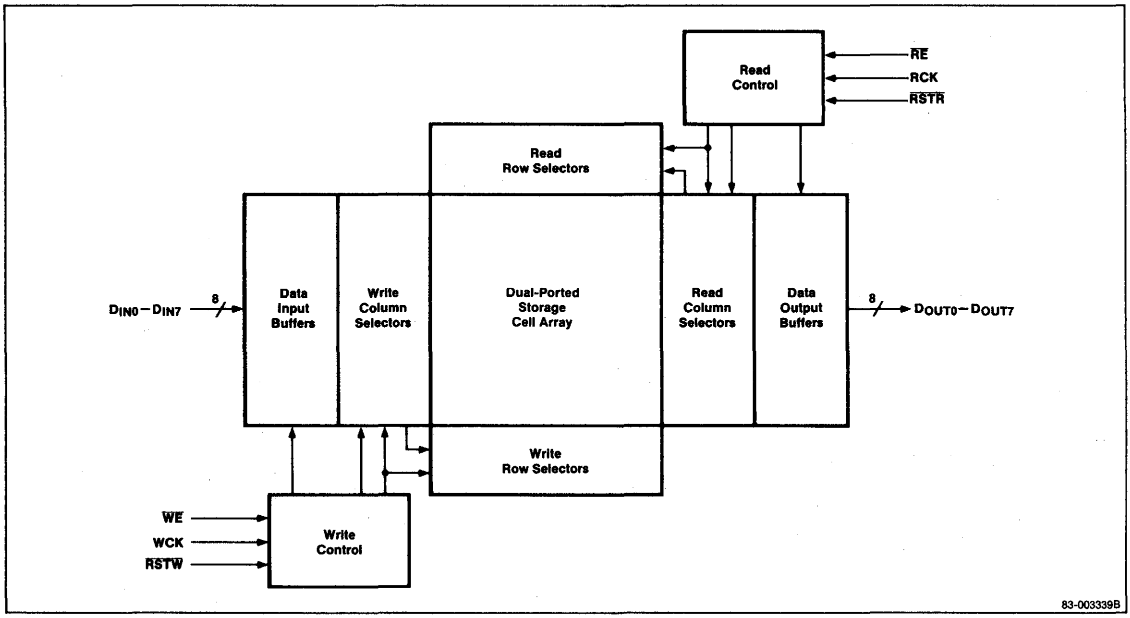
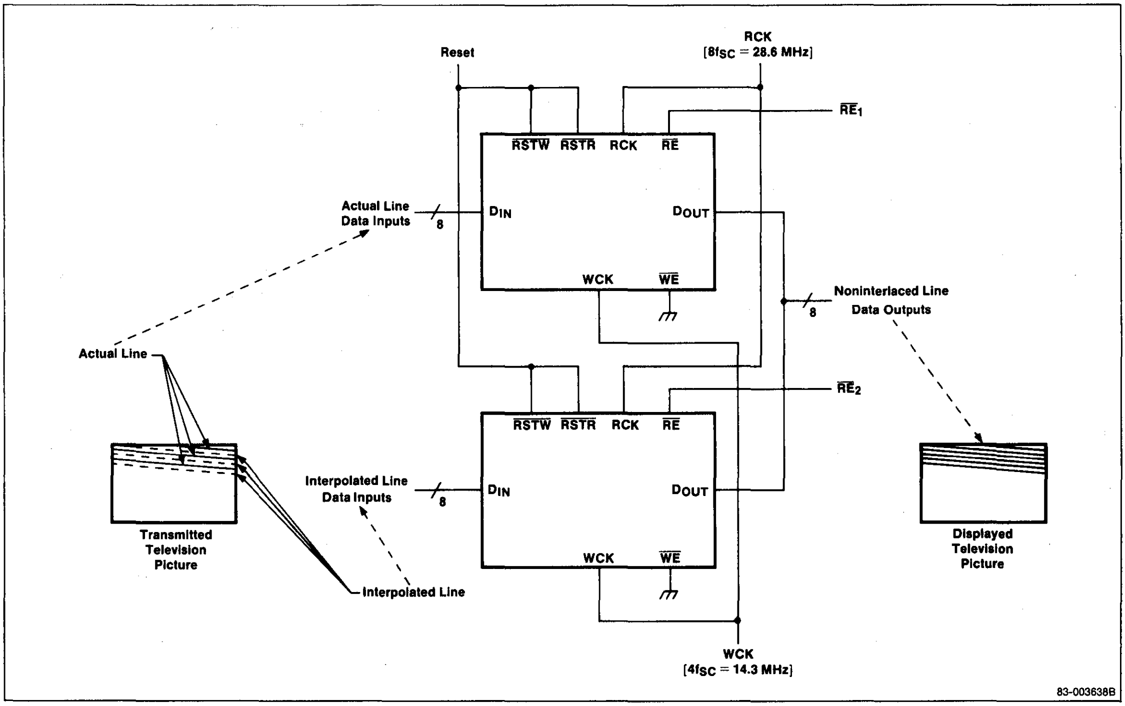


Figure 1. Connection for Noninterlaced Scan Conversion



Recommended DC Operating Conditions

T_A = −20 to +70°C; GND = 0 V

		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V

Capacitance

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%; f = 1 MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			90	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

Notes:

(1) All voltages are referenced to ground.

AC Characteristics

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD41101-3		μPD41101-2		μPD41101-1			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write clock cycle time	t_{WCK}	34	1090	69	1090	69	1090	ns	
WCK pulse width	t_{WCW}	14		25		25		ns	
WCK precharge time	t_{WCP}	14		25		25		ns	
Read clock cycle time	t_{RCK}	34	1090	34	1090	69	1090	ns	
RCK pulse width	t_{RCW}	14		14		25		ns	
RCK precharge time	t_{RCP}	14		14		25		ns	
Access time	t_{AC}		27		27		49	ns	Figure 5
Access time after a reset cycle	t_{ACR}		27		27		49	ns	
Output hold time	t_{OH}	5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		ns	Figure 5 (Note 7)
Output active time	t_{LZ}	5	27	5	27	5	49	ns	(Note 4)
Output disable time	t_{HZ}	5	27	5	27	5	49	ns	
Data-in setup time	t_{DS}	14		18		18		ns	
Data-in hold time	t_{DH}	5		5		5		ns	
Reset active setup time	t_{RS}	14		14		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		ns	
Reset inactive hold time	t_{RN1}	5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	14		14		20		ns	
Write enable setup time	t_{WES}	14		20		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		ns	
Write enable high delay from WCK	t_{WEN1}	5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	14		20		20		ns	
Read enable setup time	t_{RES}	14		14		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		ns	
Read enable high delay from RCK	t_{REN1}	5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	14		14		20		ns	
Write disable pulse width	t_{WEW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read disable pulse width	t_{REW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Write reset time	t_{RSTW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read reset time	t_{RSTR}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Transition time	t_T	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 3.

(3) Output timing reference levels are 0.8 and 2.0 volts. See figure 4.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 6. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristics (cont)

Notes [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (910-Bit) Delay Line

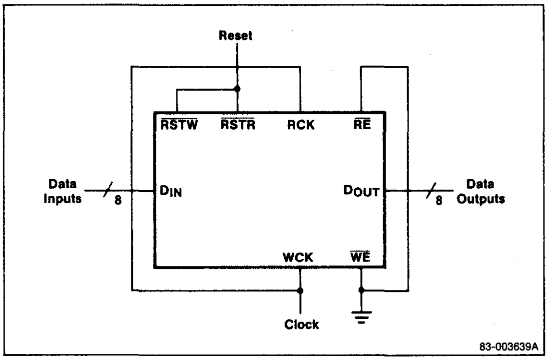


Figure 3. AC Input Timing Reference Waveform

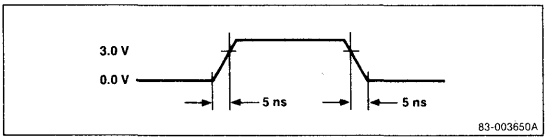


Figure 4. AC Output Timing Reference Waveform

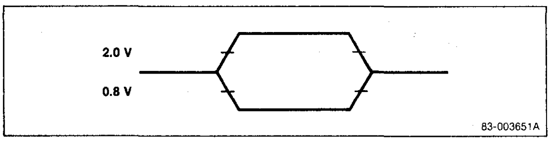


Figure 5. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

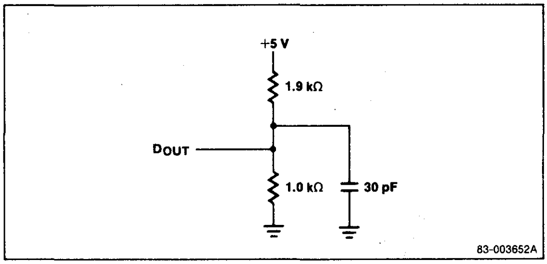
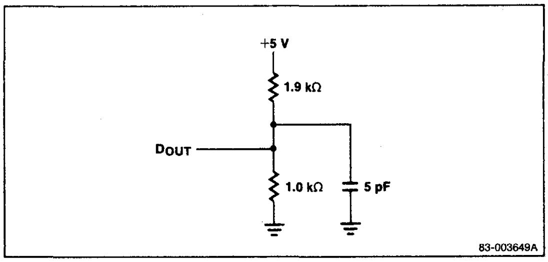
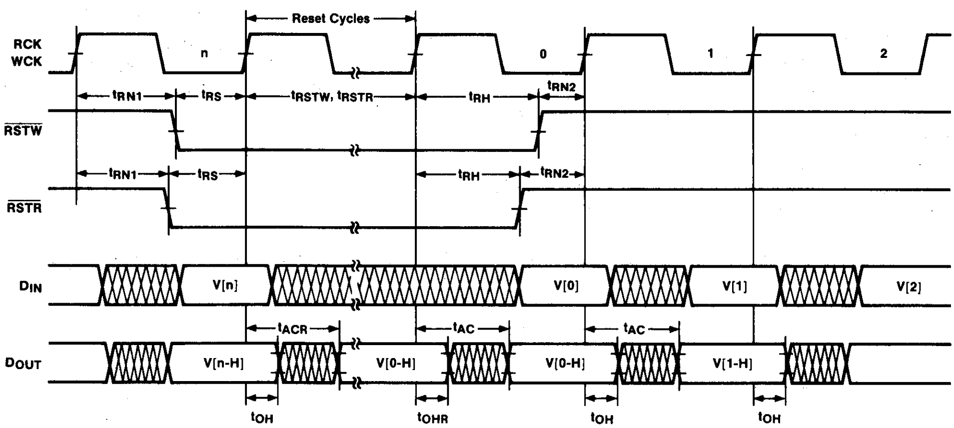


Figure 6. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

Read or Write Reset



Note:

[1] $\overline{WE} = \overline{RE} = V_{IL}$.

[2] V = Valid Data.

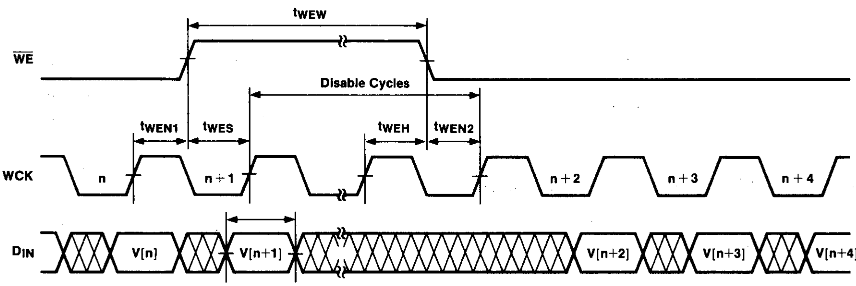
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 910 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-003645B

Write Disable



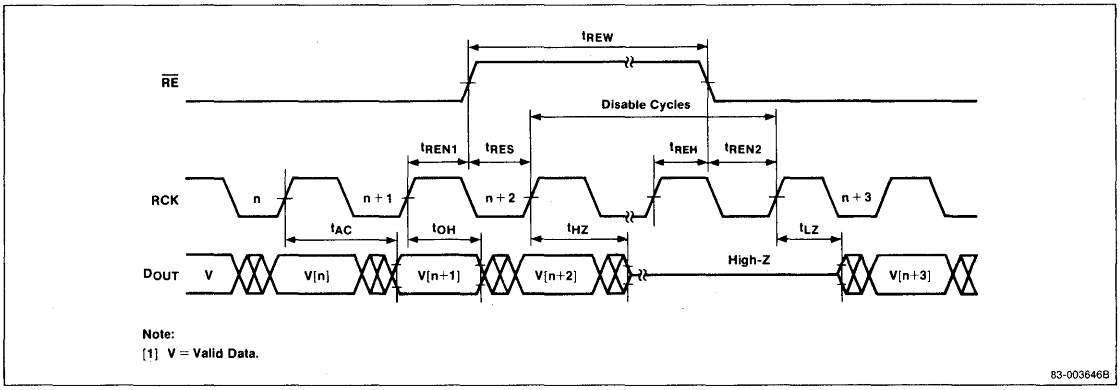
Note:

[1] V = Valid Data.

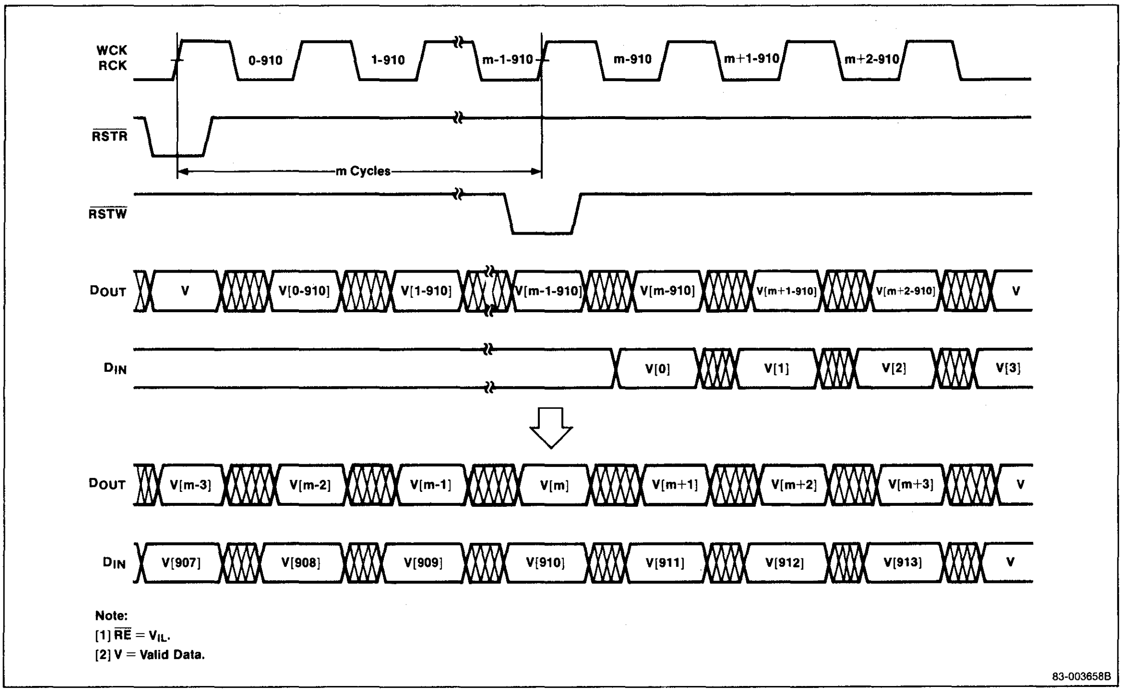
83-003723B

Timing Waveforms (cont)

Read Disable



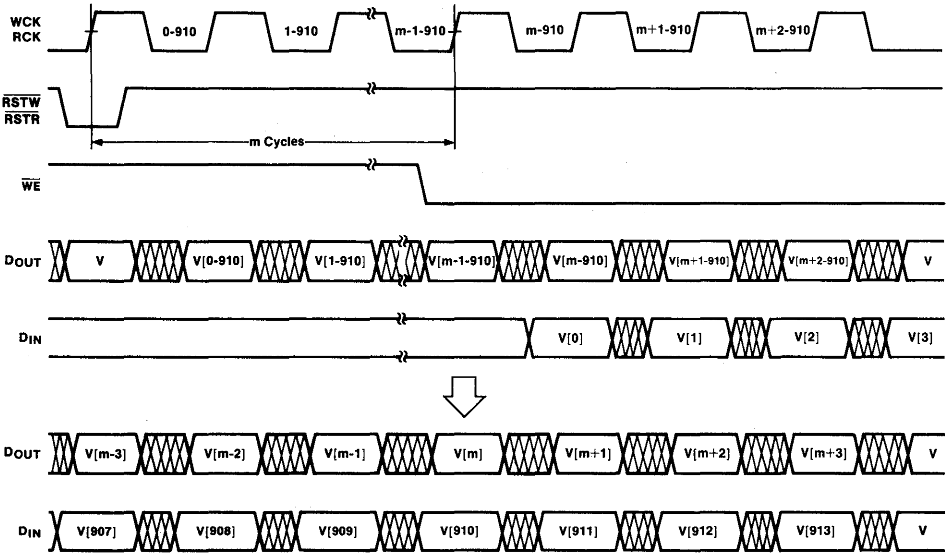
(910-m)-Bit Delay Line, No. 1



3

Timing Waveforms (cont)

(910-m)-Bit Delay Line, No. 2

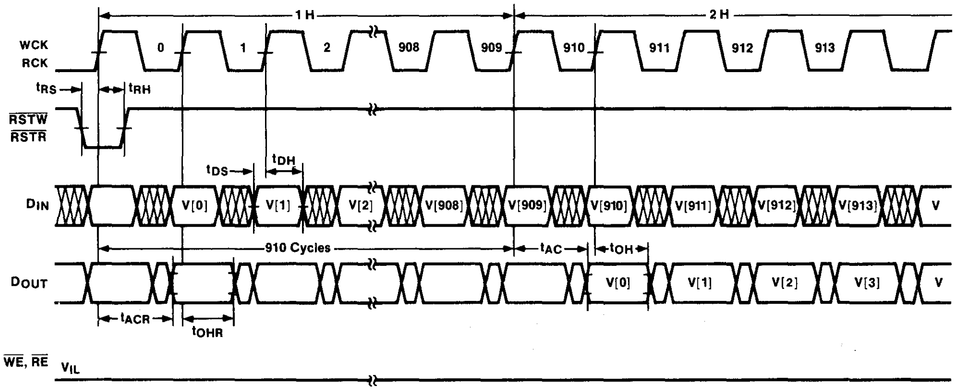


Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003659B

Timing Waveforms (cont)

910-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits. See figure 2.

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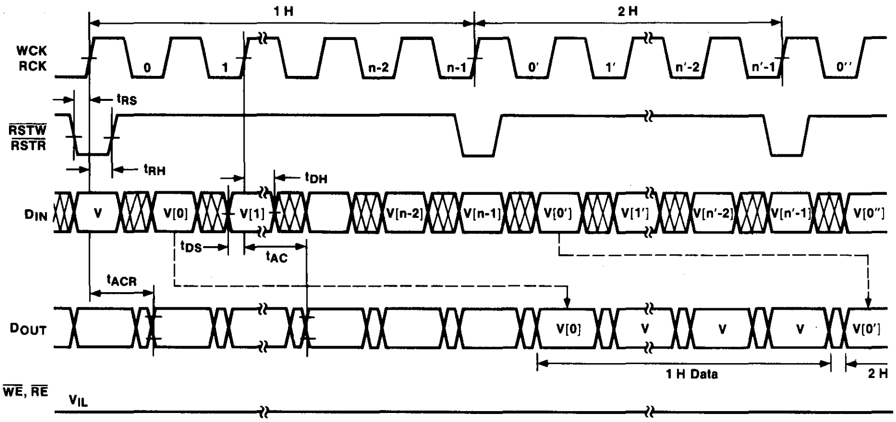
3

Timing Waveforms (cont)

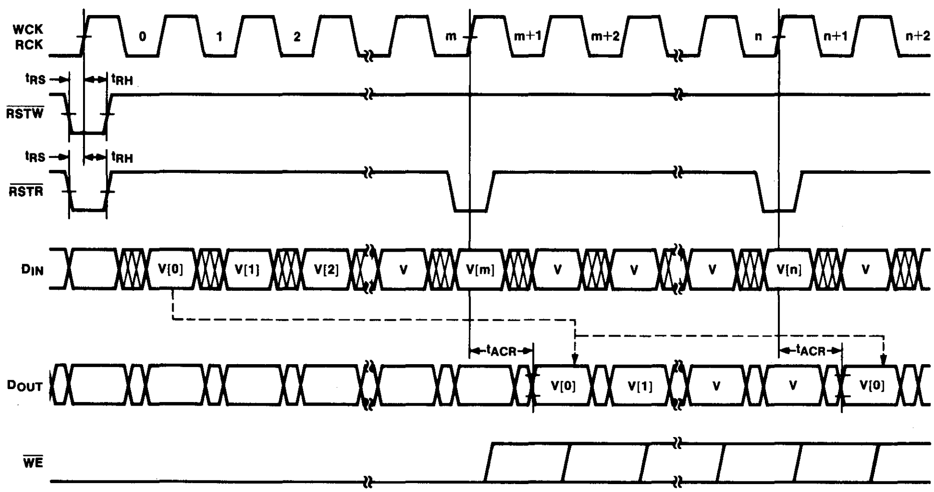
n-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

83-003643B

Re-Read Operation

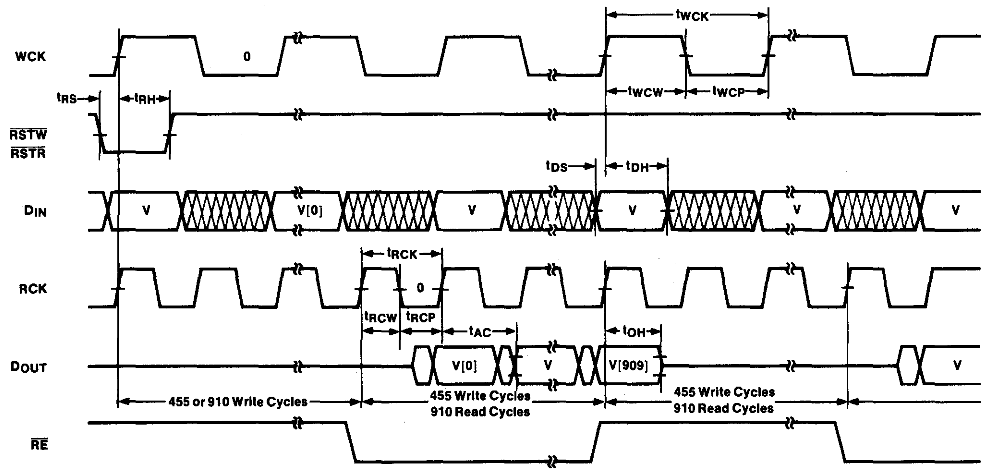


Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

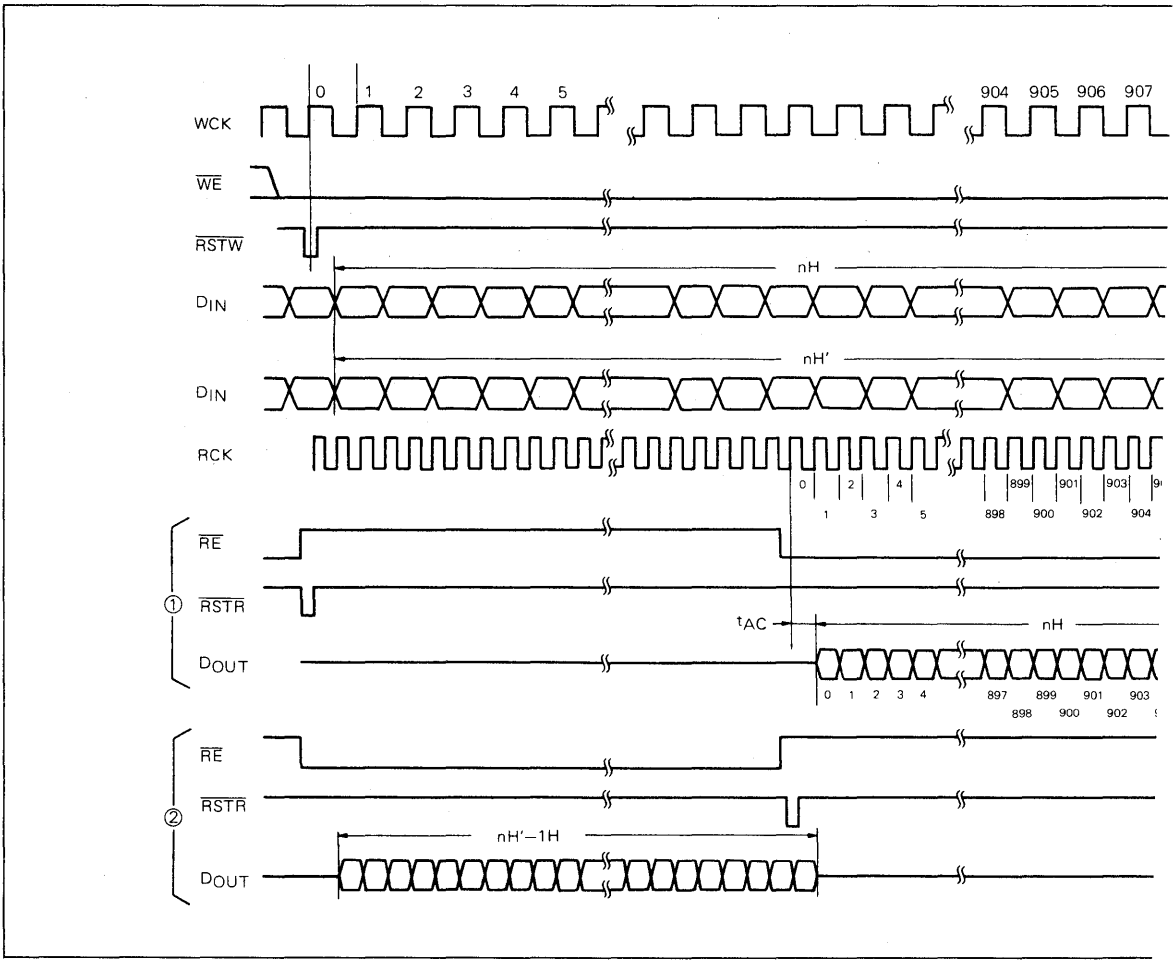
[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

83-003655B

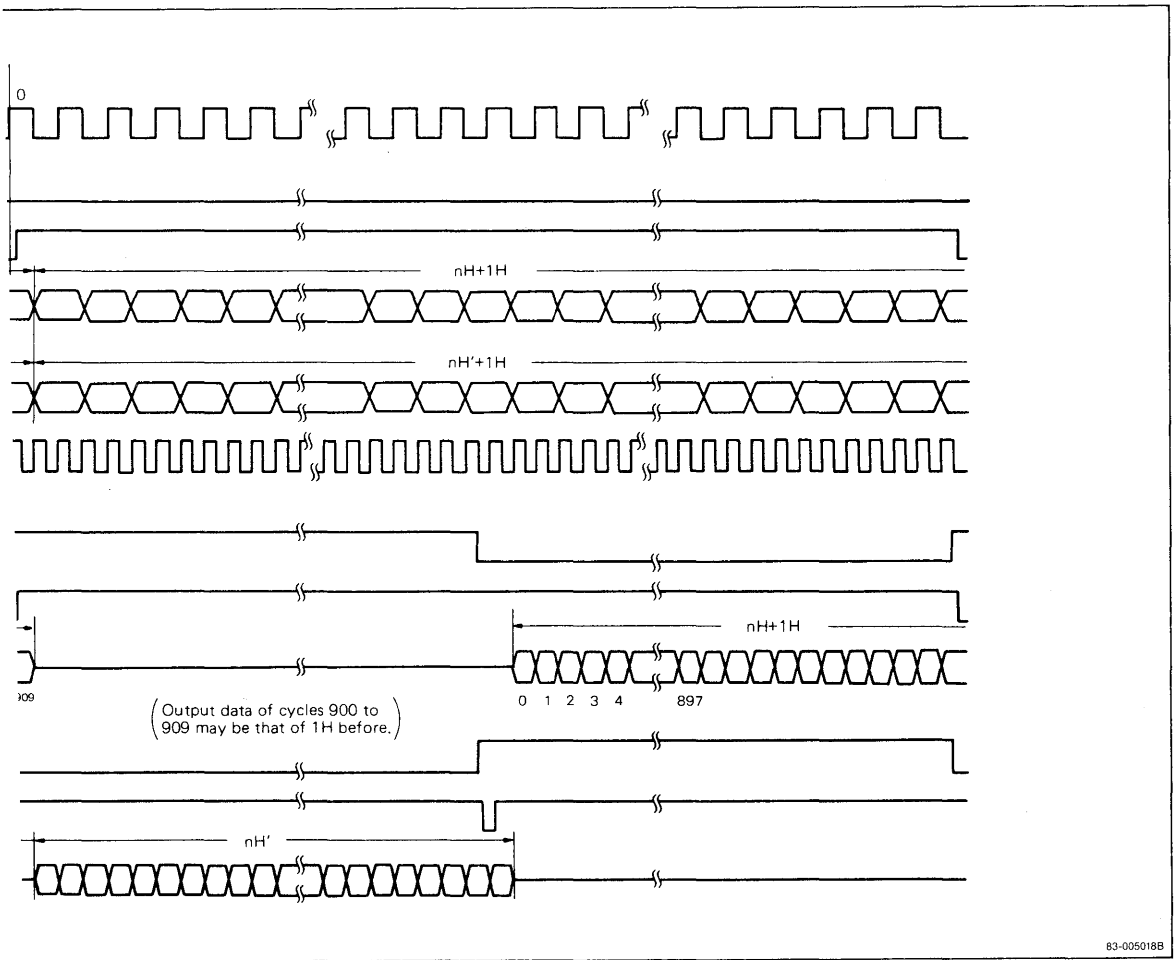
3

Timing Waveforms (cont)

Application Timing for Noninterlaced Scan Conversion



3


0
nH+1H
nH'+1H
nH+1H
909
0 1 2 3 4 897
Output data of cycles 900 to 909 may be that of 1H before.
nH'
83-005018B

μPD41102 1135 x 8-BIT LINE BUFFER FOR PAL TV

Description

The μPD41102 is a 1135-word by 8-bit line buffer fabricated with the N-channel silicon-gate process. The device helps to create a PAL flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD41102 can also be used as a digital delay line. The delay length is variable from 12 bits (at maximum clock speed) to 1135 bits.

Features

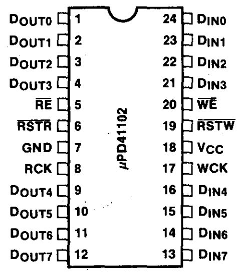
- ☐ 1135-word x 8-bit organization
- ☐ Line buffer for PAL, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operation
- ☐ 1H (1135-bit) delay line
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt ±10% power supply
- ☐ 300-mil, 24-pin plastic DIP and 450-mil, 24-pin plastic miniflat packaging

Ordering Information

Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD41102C-3	28 ns	28 ns	24-pin plastic DIP
C-2	28 ns	56 ns	
C-1S	34 ns	34 ns	
C-1	56 ns	56 ns	
μPD41102G-3	28 ns	28 ns	24-pin plastic miniflat
G-2	28 ns	56 ns	
G-1S	34 ns	34 ns	
G-1	56 ns	56 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0}-D_{IN7}	Write data inputs
D_{OUT0}-D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{\text{RSTW}}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0 if $\overline{\text{WE}}$ is also at a low level. If $\overline{\text{WE}}$ is at a high level when the $\overline{\text{RSTW}}$ input is brought low, the internal write address is set to 1134. The state of this input is strobed by the rising edge of WCK.

$\overline{\text{RSTR}}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0 if $\overline{\text{RE}}$ is also at a low level. If $\overline{\text{RE}}$ is at a high level when the $\overline{\text{RSTR}}$ input is brought low, the internal read address is set to 1134.

$\overline{\text{WE}}$ [Write Enable Input]

This input controls write operation. If $\overline{\text{WE}}$ is at a low level, all write cycles proceed. If $\overline{\text{WE}}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{\text{WE}}$ is strobed by the rising edge of WCK.

$\overline{\text{RE}}$ [Read Enable Input]

This signal is similar to $\overline{\text{WE}}$ but controls read operation. If $\overline{\text{RE}}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{\text{RE}}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]

All write cycles are executed synchronously with WCK. The states of both $\overline{\text{RSTW}}$ and $\overline{\text{WE}}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{\text{WE}}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{\text{WE}}$, the internal write address will automatically wrap around from 1134 to 0 and begin increasing again.

RCK [Read Clock Input]

All read cycles are executed synchronously with RCK. The states of both $\overline{\text{RSTR}}$ and $\overline{\text{RE}}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{\text{RE}}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{\text{RE}}$, the internal read address will automatically wrap around from 1134 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram

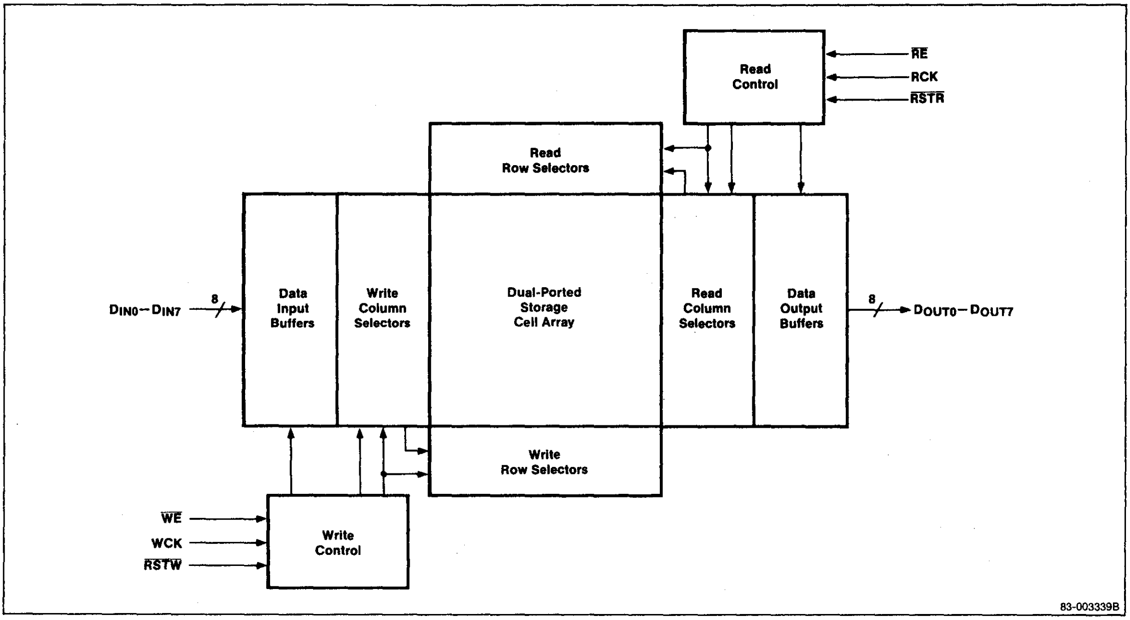


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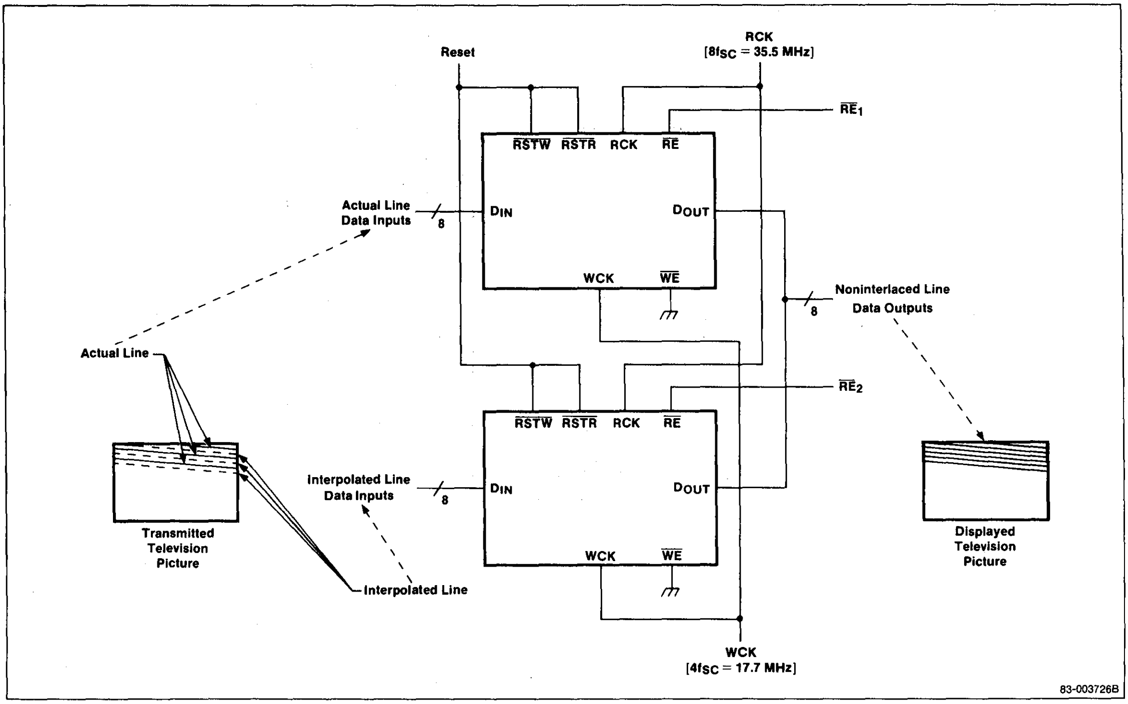
Figure 1. Connection for Noninterlaced Scan Conversion



Recommended DC Operating Conditions

$T_A = -20$ to $+70°C$; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V

Capacitance

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			90	mA	
Input leakage current	I_I	−10		10	μA	$V_I = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; $V_O = 0$ to 5.5 V
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1$ mA
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 2$ mA

Notes:

(1) All voltages are referenced to ground.

AC Characteristics

T_A = −20 to +70 °C; V_{CC} = 5.0 V ±10%

		Limits									
		μPD41102-3		μPD41102-2		μPD41102-1S		μPD41102-1			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write clock cycle time	t_{WCK}	28	880	56	880	34	880	56	880	ns	
WCK pulse width	t_{WCW}	12		20		14		20		ns	
WCK precharge time	t_{WCP}	12		20		14		20		ns	
Read clock cycle time	t_{RCK}	28	880	28	880	34	880	56	880	ns	
RCK pulse width	t_{RCW}	12		12		14		20		ns	
RCK precharge time	t_{RCP}	12		12		14		20		ns	
Access time	t_{AC}		21		21		27		40	ns	Figure 5
Access time after a reset cycle	t_{ACR}		21		21		27		40	ns	
Output hold time	t_{OH}	5		5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		5		ns	Figure 5 (Note 7)
Output active time	t_{LZ}	5	21	5	21	5	27	5	40	ns	(Note 4)
Output disable time	t_{HZ}	5	21	5	21	5	27	5	40	ns	
Data-in setup time	t_{DS}	12		15		14		15		ns	
Data-in hold time	t_{DH}	5		5		5		5		ns	
Reset active setup time	t_{RS}	12		12		14		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		5		ns	
Reset inactive hold time	t_{RN1}	5		5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	12		12		14		20		ns	
Write enable setup time	t_{WES}	12		20		14		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		5		ns	
Write enable high delay from WCK	t_{WEN1}	5		5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	12		20		14		20		ns	
Read enable setup time	t_{RES}	12		12		14		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		5		ns	
Read enable high delay from RCK	t_{REN1}	5		5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	12		12		14		20		ns	
Write disable pulse width	t_{WEW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read disable pulse width	t_{REW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Write reset time	t_{RSTW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read reset time	t_{RSTR}	0	(Note 6)	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Transition time	t_T	3	35	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 3.

(3) Output timing reference levels are 0.8 and 2.0 volts. See figure 4.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 6. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

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AC Characteristics (cont)

Notes [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (1135-Bit) Delay Line

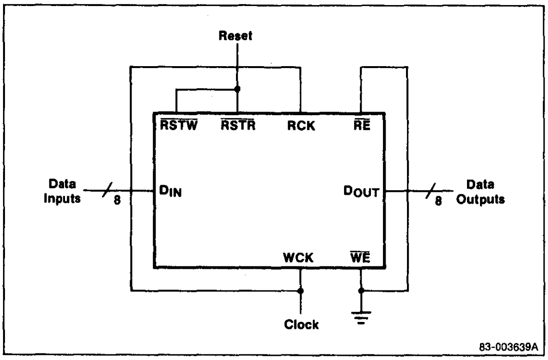


Figure 3. AC Input Timing Reference Waveform

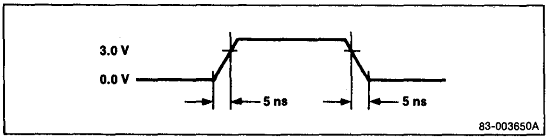


Figure 4. AC Output Timing Reference Waveform

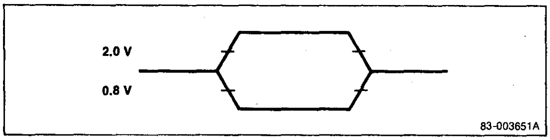


Figure 5. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

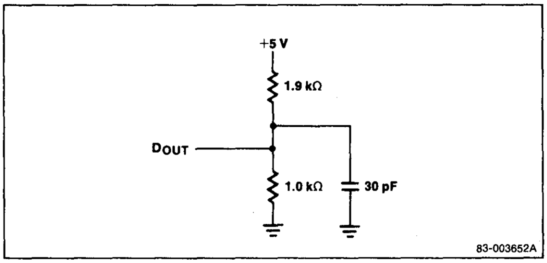
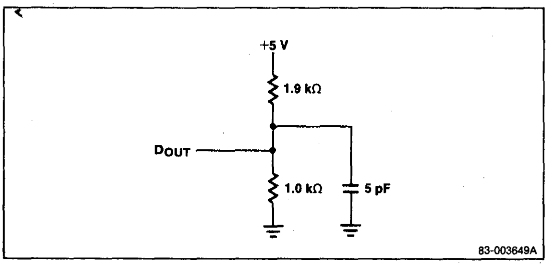
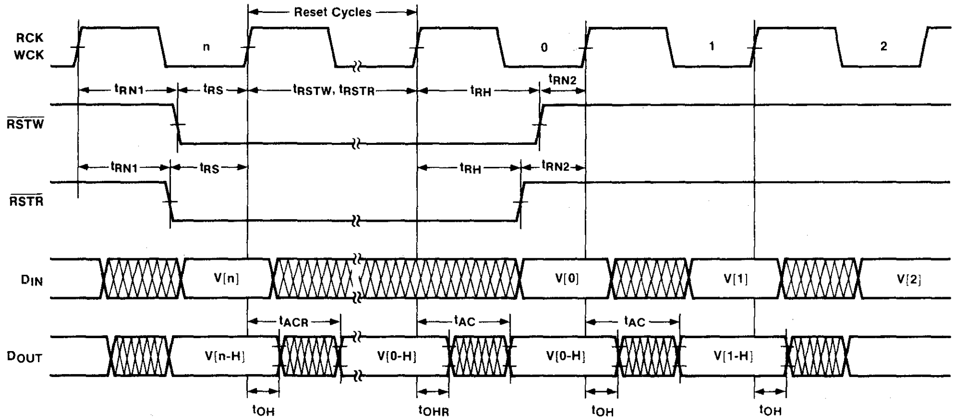


Figure 6. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

Read or Write Reset



Note:

[1] $\overline{WE} = \overline{RE} = V_{IL}$

[2] V = Valid Data.

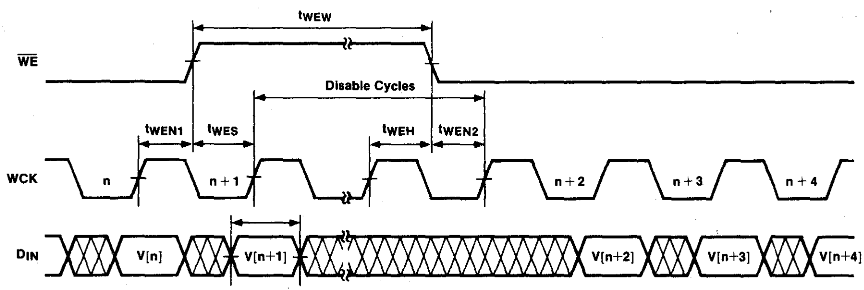
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 1135 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-003727B

Write Disable



Note:

[1] V = Valid Data.

83-003723B

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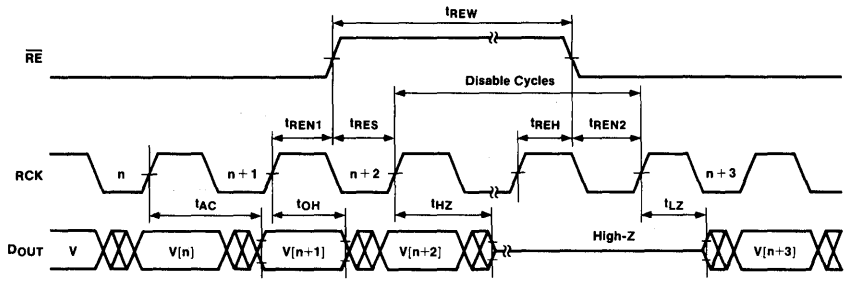
Timing Waveforms (cont)

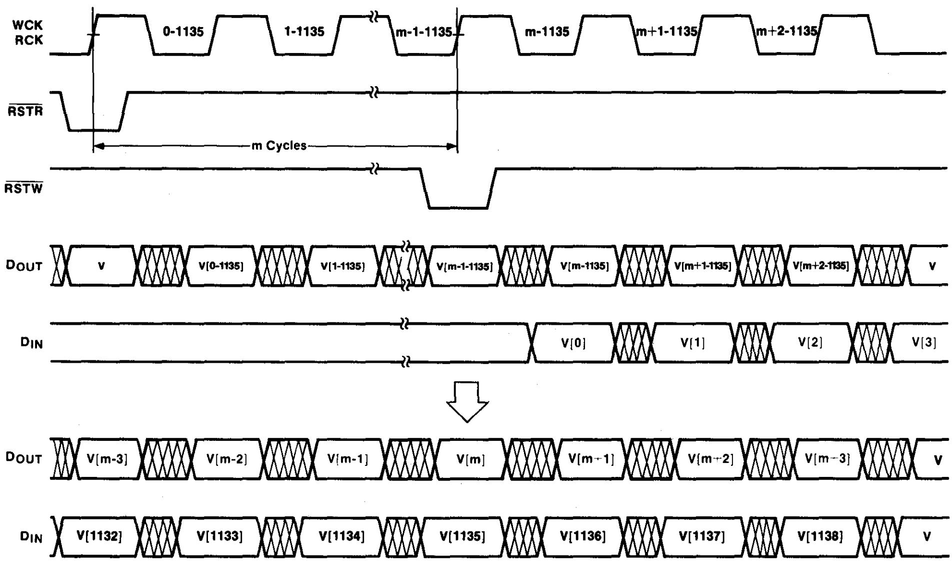
Read Disable



Note:
[1] V = Valid Data.

83-003646B

(1135-m)-Bit Delay Line, No. 1

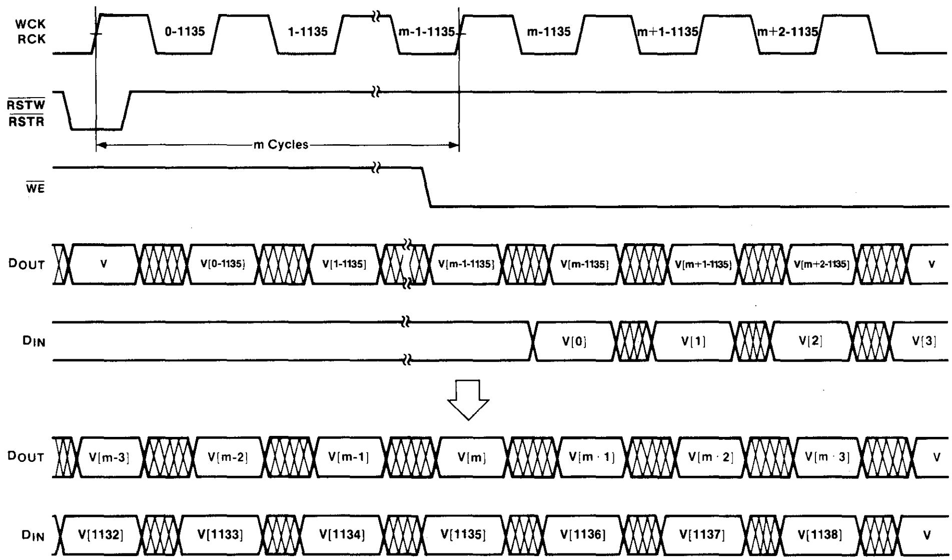


Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003647B

Timing Waveforms (cont)

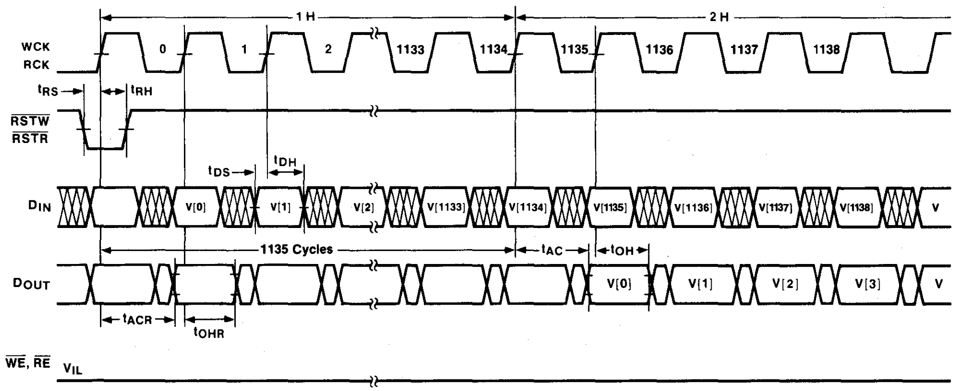
(1135-m)-Bit Delay Line, No. 2



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003648B

1135-Bit Delay Line

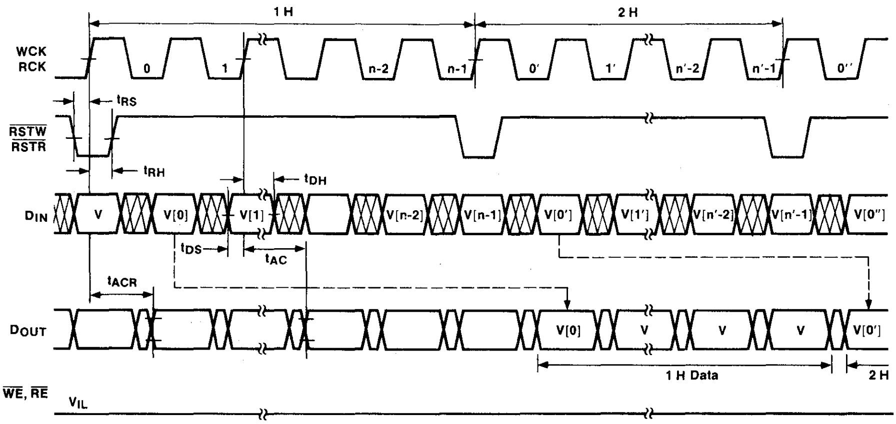


Note:
[1] V = Valid Data.
[2] 1H = the first group of 1135 bits. 2H = the second group of 1135 bits. See figure 2.

83-003642B

Timing Waveforms (cont)

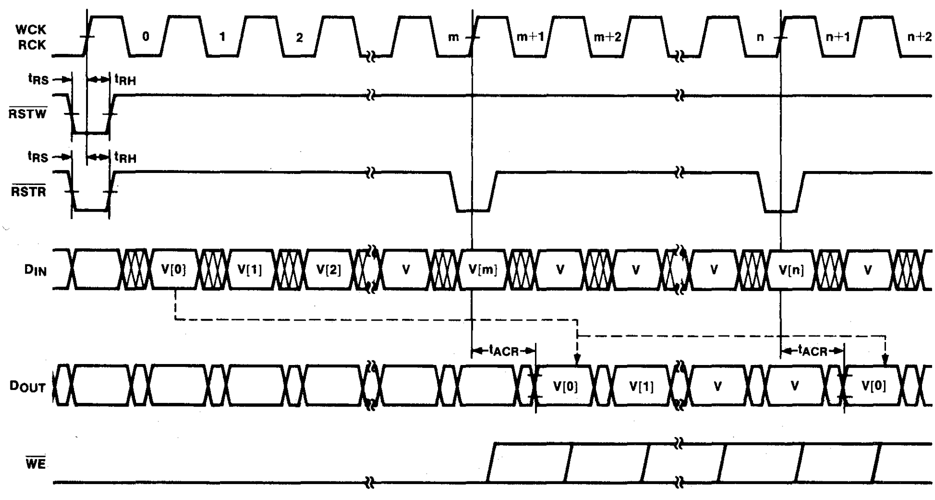
n-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n bits.

83-003643B

Re-Read Operation

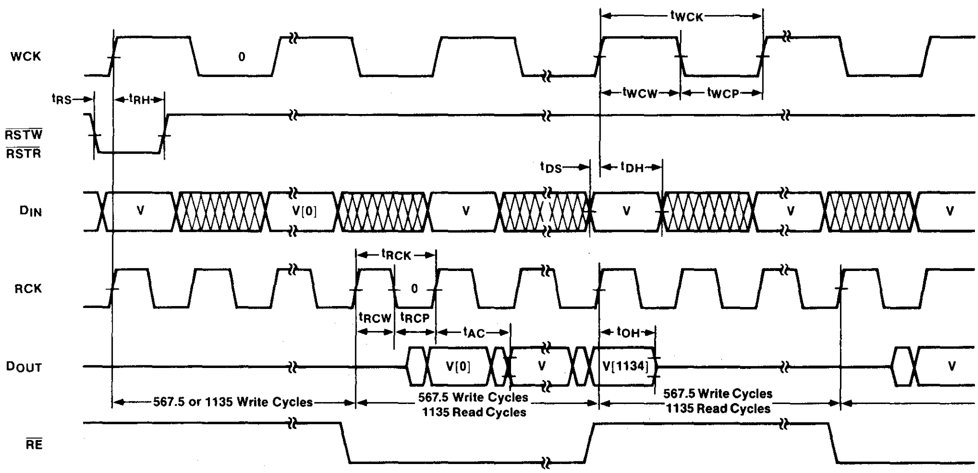


Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:
[1] $\overline{WE}$ = V_{IL}.
[2] V = Valid Data.
[3] For compatibility with PAL standards the WCK frequency is approximately 17.7 MHz. RCK cycles at twice this frequency, 35.5 MHz.

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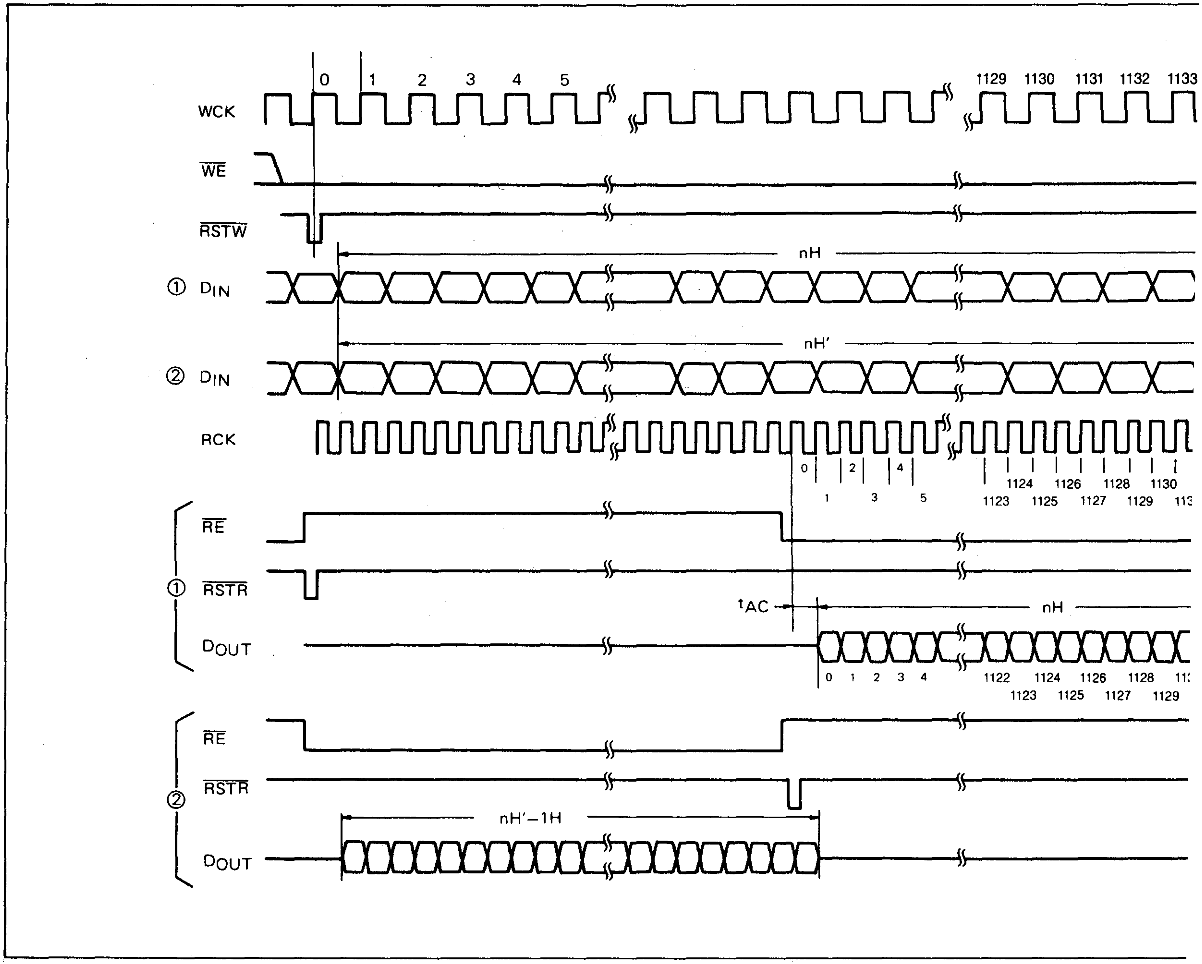
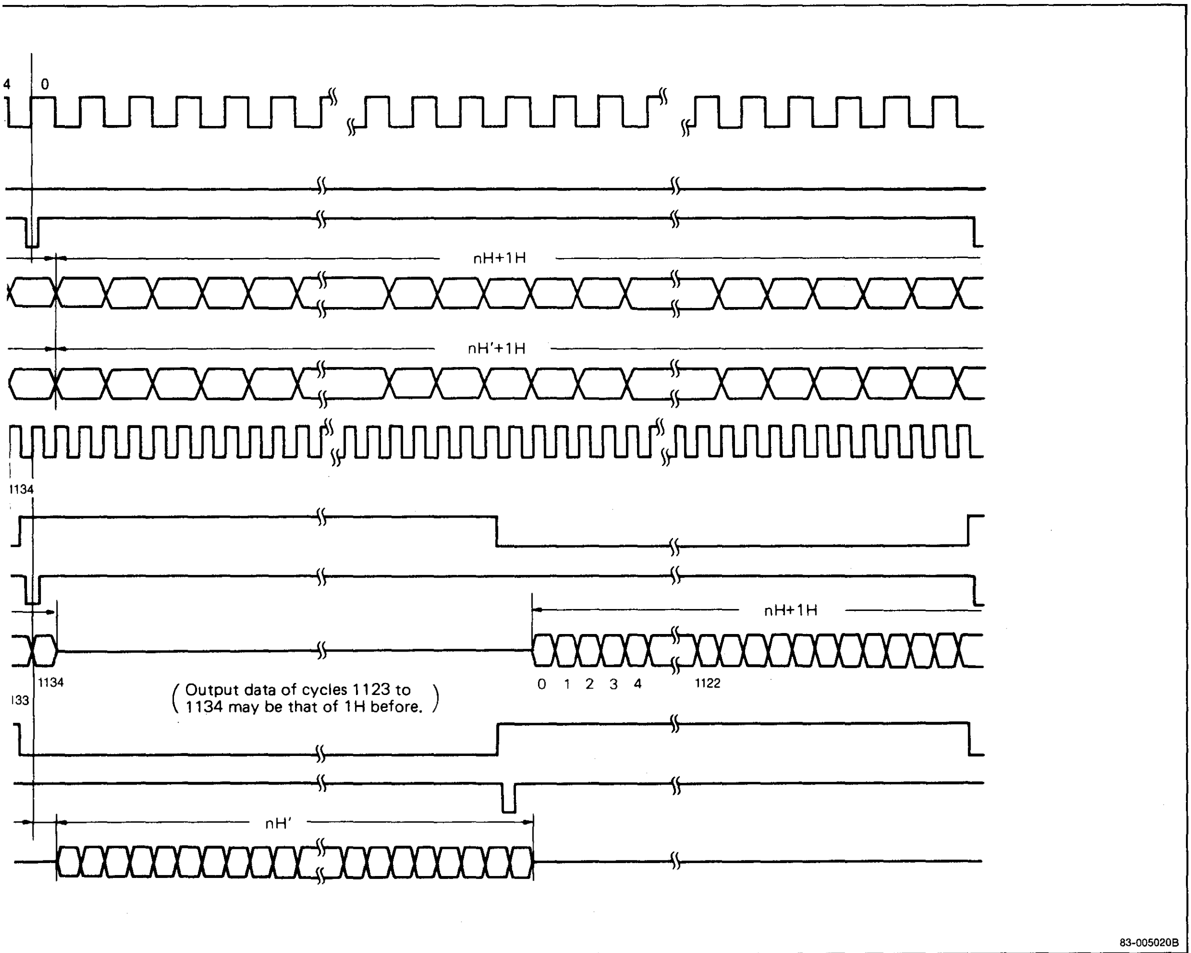
Timing Waveforms (cont)

Application Timing For Noninterlaced Scan Conversion




4
0
nH+1H
nH'+1H
1134
nH+1H
1134
133
(Output data of cycles 1123 to
1134 may be that of 1H before.)
0 1 2 3 4
1122
nH'
83-005020B

3

μPD41264 DUAL-PORT GRAPHICS BUFFER

Description

The μPD41264 is a dual-port graphics buffer equipped with a 64K x 4-bit random access port and a 256 x 4-bit serial read port. The random access port is used by the host CPU to read or write data addressed in any desired order. The serial read port is connected to an internal 1024-bit data register through a 256 x 4-bit serial read output circuit. In addition to its conventional features, the random access port also has a write-per-bit capability that allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD41264 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port, however, continues to operate normally. Following the clock transition of a data transfer, the serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD41264 is fabricated with a double polylayer, N-channel, silicon-gate process that provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD41264 is available in a 24-pin plastic ZIP or a 400-mil, 24-pin plastic DIP and is guaranteed for operation at 0 to +70 °C.

Features

- ☐ Three functional blocks
  - — 64K x 4-bit random access storage array
  - — 1024-bit data register
  - — 256 x 4-bit serial read output circuit
- ☐ Two data ports: random access and serial read
- ☐ Dual-port accessibility except during data transfer
- ☐ Addressable start of serial read operation
- ☐ Real-time data transfer
- ☐ Single +5-volt ± 10% power supply
- ☐ On-chip substrate bias generator
- ☐ Random access port
  - — Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - — Multiplexed address inputs
  - — Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - — Refresh interval: 256 cycles/4 ms
  - — Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and page mode capabilities
  - — Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - — Hidden refreshing by means of $\overline{CAS}$-controlled output
  - — Write-per-bit capability regarding four I/O bits
  - — Write bit selection multiplexed on IO_0-IO_3
- ☐ $\overline{RAS}$-activated data transfer
  - — Same cycle time as for random access
  - — Row data transferred to data register as specified by row address inputs
  - — Starting location of following serial read operation specified by column address inputs
  - — Transfer of 1024 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - — Data transfer during real-time or standby operation of serial port
- ☐ Fast serial read operation by means of serial control pins
  - — Serial data presented on SO_0-SO_3
  - — Direct connection of multiple serial outputs for extension of data length
- ☐ Fully TTL-compatible inputs, outputs, and clocks
- ☐ Three-state outputs for random and serial access
- ☐ Double polylayer, N-channel, silicon-gate process
- ☐ 400-mil, 24-pin plastic DIP or 24-pin plastic ZIP packaging

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NEC

Ordering Information

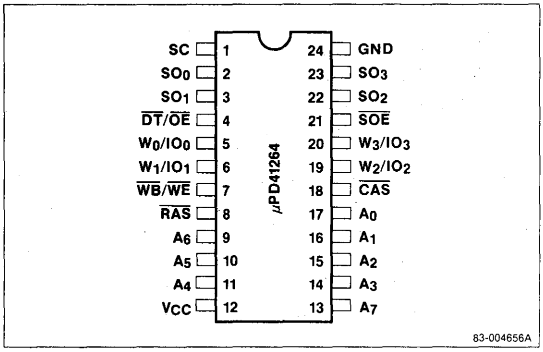
Part Number	Row Access Time (max)	Serial Access Time (max)	Package
µPD41264C-12	120 ns	40 ns	24-pin plastic DIP
C-15	150 ns	60 ns	
µPD41264V-12	120 ns	40 ns	24-pin plastic ZIP
V-15	150 ns	60 ns	

Pin Identification

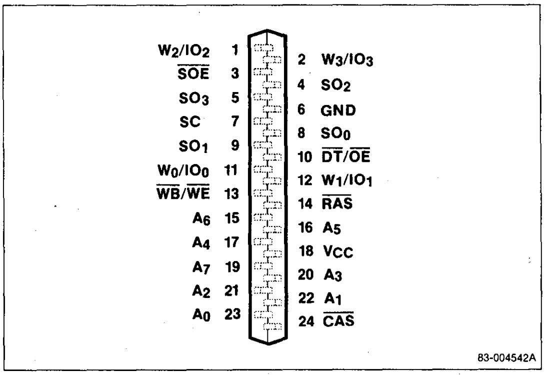
Symbol	Function
A_0-A_7	Address inputs
W_0/IO_0-W_3/IO_3	Write selects in write-per-bit/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB}/\overline{WE}$	Write-per-bit/write enable
$\overline{DT}/\overline{OE}$	Data transfer/output enable
SO_0-SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply

Pin Configurations

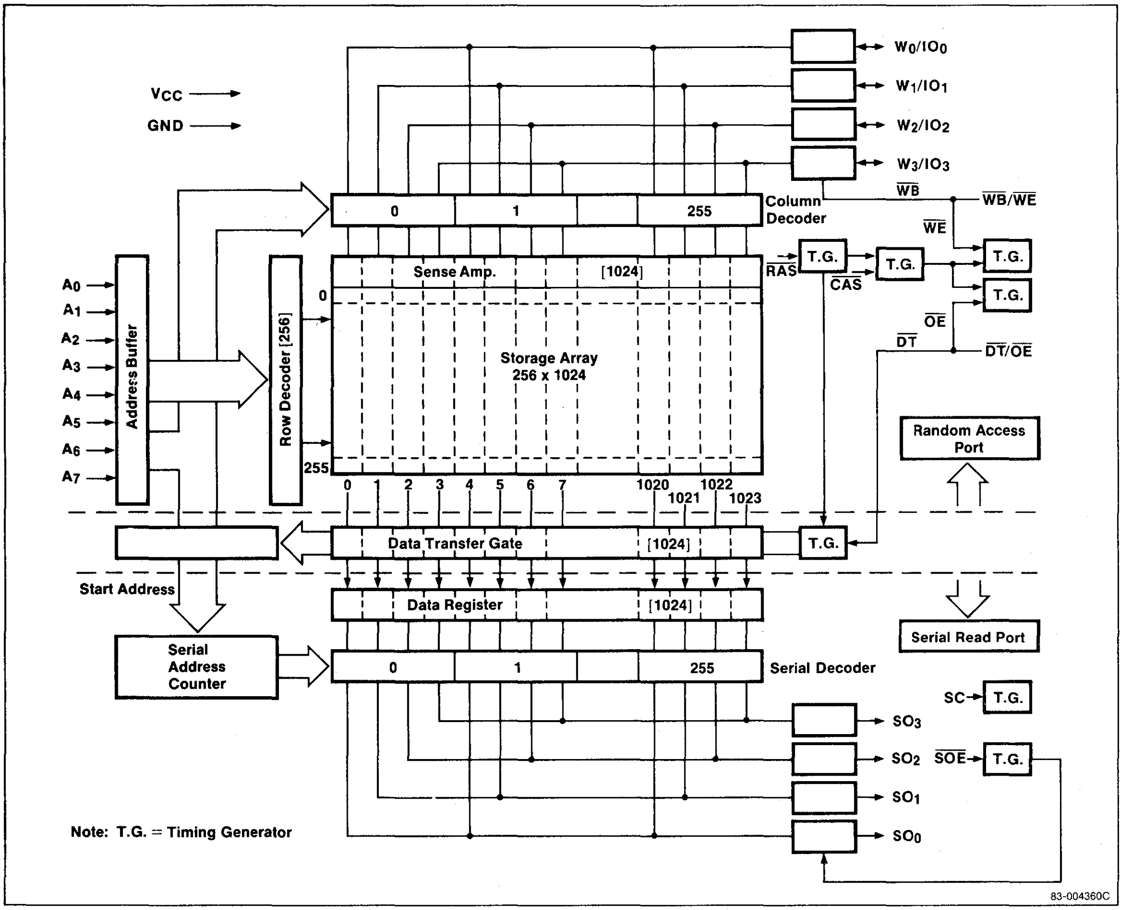
24-Pin Plastic DIP



24-Pin Plastic ZIP



Block Diagram



Device Operation

Overall Description

The μPD41264 consists of a random access port and a serial read port. The random access port performs standard read and write operation as well as the data transfer operation, all of which are based on the conventional $\overline{RAS}/\overline{CAS}$ timing cycle. In a data transfer cycle, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. The serial read port shows the contents of the data register in serial order. The random access port and the serial read port can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The graphics storage array is arranged in a 256-row by 1024-column matrix. Each of 4 data bits in the random access port corresponds to 65,536 storage cells. Therefore, 16 address bits are required to decode one cell location. Eight row address bits are set up on pins A_0 through A_7 and latched onto the chip by $\overline{RAS}$. Eight column address bits then are set up on pins A_0 through A_7 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 1024 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 256 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In the data transfer cycle, 8 row address bits are used to select 1 of the 256 possible rows involved in the transfer of data to the data register. Eight column address bits are then used to select the 1 of 256 possible serial decoders that corresponds to the starting location of the next serial read cycle.

In the serial read port, when SC is activated, 4 data bits in the 1024-bit data register are transferred to 4 serial data buses and read out. By activating SC repeatedly, the serial read operation (starting from the location specified in the data transfer cycle) is executed within the 1024 bits in the data register.

Random Access Port Operation

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multiplexed in the random access port.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations. The $\overline{DT}$, $\overline{WB}$, and W_i functions are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$. The $\overline{DT}$ level determines whether a cycle is a random access operation or a data transfer operation. WB affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD41264 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 1024-bit data register from the corresponding 1024-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 1024 data transfer gates and transfer data from one of the rows to the data register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining a high $(\overline{WB}/)\overline{WE}$ during an active $\overline{CAS}$. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in a state of high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following three calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$ to $\overline{CAS}$ and $\overline{RAS}$ to $\overline{OE}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. A high $\overline{CAS}$ or $\overline{OE}$ returns the output to a high impedance condition.

Write Cycle. A write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or $(\overline{WB}/)\overline{WE}$ strobes the data on $(W_i/)IO_i$ into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}(/\overline{WE})$ must be low as $\overline{RAS}$ falls. In this case, data bits to which the write operation is applied can be specified by keeping $W_i(/IO_i)$ high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of $W_i(/IO_i)$ that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}(/\overline{WE})$ is high as $\overline{RAS}$ falls, the write-per-bit capability is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low before $\overline{CAS}$. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in a state of high impedance for the entire cycle. As $\overline{RAS}$ falls, $(\overline{DT}/)\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$; but otherwise $(\overline{DT}/)\overline{OE}$ does not affect any circuit operation during an active $\overline{CAS}$.

Read-Write/Read-Modify-Write [RW/RMW] Cycle. An RW/RMW cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. $(W_i/)IO_i$ shows read data at access time. Afterward, in preparation for the upcoming write cycle, $(W_i/)IO_i$ is returned to a high-impedance condition by a high $(\overline{DT}/)\overline{OE}$. The data to be written is strobed by $(\overline{WB}/)\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of $(\overline{DT}/)\overline{OE}$, which can be activated just after $(\overline{WB}/)\overline{WE}$ falls, even when $(\overline{WB}/)\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 256 row addresses (A_0 through A_7) will refresh all storage cells. Any operation performed in the random access port (i.e., read, write, refresh, or data transfer) refreshes the 1024 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-only Refresh. A cycle having only $\overline{RAS}$ active refreshes one row of the storage array. A high $\overline{CAS}$ is maintained during an active $\overline{RAS}$ to keep $(W_i/)IO_i$ in a state of high impedance. This mode is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ before $\overline{RAS}$ Refresh. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically performs refreshing for row addresses specified by the internal refresh address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Page Cycle. This feature allows effectively faster data access by keeping the same row address and strobing successive column addresses onto the chip. By maintaining a low $\overline{RAS}$ while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because $\overline{RAS}$ addresses are maintained internally and do not have to be reapplied. During this operation, read, write and RW/RMW cycles are possible. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following page write cycle.

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}(/\overline{OE})$ low as $\overline{RAS}$ falls. As described previously, the specified 1 of the possible 256 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}(/\overline{OE})$ must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. At least one SC cycle is required to hold the data in the register. Otherwise, the beginning of the next transfer cycle destroys the newly transferred data. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the transferred data in the random access port.

Serial Read Port Operation

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows the data transfer cycle. Data stored in the serial register remains valid for a minimum of 4 ms after the transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from a high SC, only when a low $\overline{SOE}$ is maintained. The SC cycle that includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD41264 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended DC Operating Conditions

T_A = 0 to +70°C; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4		V_{CC}	V	$I_{OH(R)}$ = −2 mA
Random access port output voltage, low	$V_{OL(R)}$	0		0.4	V	$I_{OL(R)}$ = 4.2 mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4		V_{CC}	V	$I_{OH(S)}$ = −2 mA
Serial read port output voltage, low	$V_{OL(S)}$	0		0.4	V	$I_{OL(S)}$ = 4.2 mA

Power Supply Current Definitions

Port	Operation	Symbol	Operating Conditions
Random Access	Read/write	RW	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min)
	Standby	STB	$\overline{RAS} = V_{IH}$; D_{OUT} = high impedance
	$\overline{RAS}$-only refresh	ROR	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ (min)
	Page mode	PAGE	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min)
	$\overline{CAS}$ before $\overline{RAS}$ refresh	CBR	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
	Data transfer	DTR	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
Serial Read	Standby	STB	$SC = \overline{SOE} = V_{IH}$
	Serial read	ACT	$\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ (min)

Power Supply Current

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Port Random Access	Serial Read	Symbol	Limits μPD41264 -12 Max	-15 Max	Unit	Test Conditions
RW	STB	I_{CC1}	95	85	mA	(Note 1)
STB	STB	I_{CC2}	12	12	mA	
ROR	STB	I_{CC3}	75	65	mA	
PAGE	STB	I_{CC4}	65	55	mA	(Note 1)
CBR	STB	I_{CC5}	75	65	mA	(Note 1)
DTR	STB	I_{CC6}	120	100	mA	
RW	ACT	I_{CC7}	155	130	mA	(Note 1)
STB	ACT	I_{CC8}	60	45	mA	(Note 1)
ROR	ACT	I_{CC9}	135	110	mA	(Note 1)
PAGE	ACT	I_{CC10}	125	100	mA	(Note 1)
CBR	ACT	I_{CC11}	135	110	mA	(Note 1)
DTR	ACT	I_{CC12}	180	145	mA	(Note 1)

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, and I_{CC6}, real values depend on output loading and cycle rates.

Capacitance

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 to A_7
Input capacitance	$C_{I(\overline{DT}/\overline{OE})}$	6	pF	$\overline{DT}/\overline{OE}$
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 to W_3/IO_3
Input capacitance	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	6	pF	$\overline{SOE}$
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 to SO_3
Input capacitance	$C_{I(SC)}$	8	pF	SC

AC Input/Output Timing Waveforms

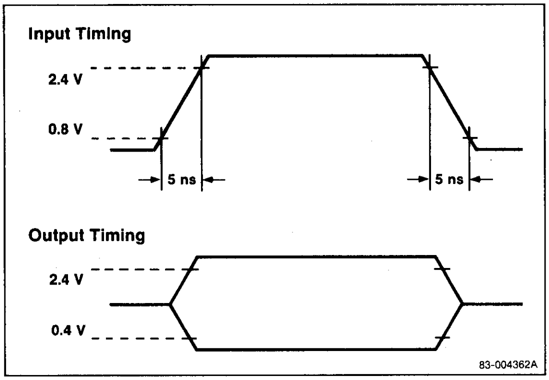


Figure 1. Random Access Port: Output Loading

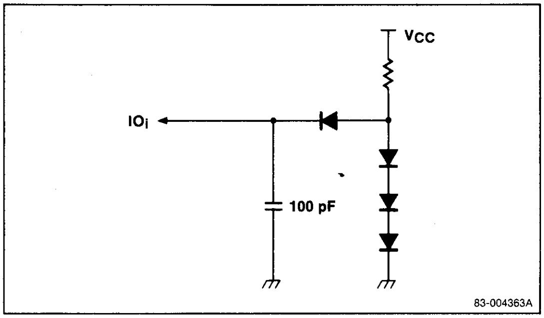
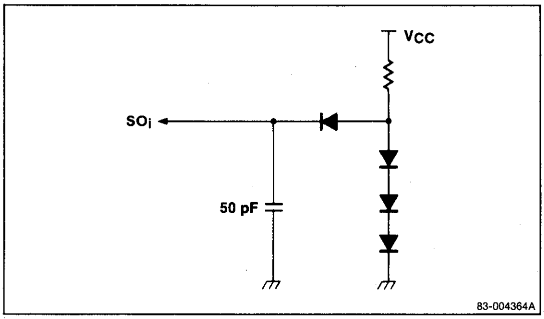


Figure 2. Serial Read Port: Output Loading



AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V $\pm 10\%$

		Limits					
		μPD41264-12		μPD41264-15			Test
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Switching Characteristics							
Access time from $\overline{\text{RAS}}$	t_{RAC}		120		150	ns	(Notes 2, 4)
Access time from $\overline{\text{CAS}}$	t_{CAC}		60		75	ns	(Notes 2, 5)
Access time from $\overline{\text{OE}}$	t_{OEA}		30		40	ns	(Note 2)
Serial output access time from SC	t_{SCA}		40		60	ns	(Notes 2, 7)
Serial output access time from $\overline{\text{SOE}}$	t_{SOA}		35		50	ns	(Notes 2, 7)
Output disable time from $\overline{\text{CAS}}$ high	t_{OFF}	0	30	0	40	ns	(Note 6)
Output disable time from $\overline{\text{OE}}$ high	t_{OEZ}	0	30	0	40	ns	(Note 6)
Serial output disable time from $\overline{\text{SOE}}$ high	t_{SOZ}	0	30	0	40	ns	(Note 6)
Timing Requirements							
Random read or write cycle time	t_{RC}	220		270		ns	
Read-write/read-modify-write cycle	t_{RWC}	300		355		ns	
Page mode cycle time	t_{PC}	120		145		ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	90		100		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	60		75		ns	
$\overline{\text{CAS}}$ precharge time (nonpage mode)	t_{CPN}	25		30		ns	
$\overline{\text{CAS}}$ precharge time (page mode only)	t_{CP}	50		60		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	120		150		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	25	60	30	75	ns	(Note 4)
$\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low precharge time	t_{CRP}	10		10		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		20		ns	
Column address setup time	t_{ASC}	0		0		ns	

AC Characteristics (cont)

		Limits					
		µPD41264-12		µPD41264-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Timing Requirements (cont)							
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time after $\overline{RAS}$ low	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	20		20		ns	(Note 9)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 9)
Write command setup time	t_{WCS}	0		0		ns	(Note 10)
Write command hold time	t_{WCH}	35		45		ns	
Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	35		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 11)
Data-in hold time	t_{DH}	35		45		ns	(Note 11)
Data-in hold time after $\overline{RAS}$ low	t_{DHR}	95		120		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	100		120		ns	(Note 10)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	160		195		ns	(Note 10)
$\overline{OE}$ high to data-in setup delay	t_{OED}	35		40		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	30		40		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	10		10		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	25		30		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Refresh time interval	t_{REF}		4		4	ms	
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	100		130		ns	
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	40		55		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		20		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		20		ns	
$\overline{OE}$ pulse width	t_{OE}	35		40		ns	
Serial clock cycle time	t_{SCC}	40	50000	60	50000	ns	
SC pulse width	t_{SCH}	10		20		ns	
SC precharge time	t_{SCL}	10		20		ns	
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	10		10		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	20		25		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	10		10		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write-per-bit hold time	t_{WBH}	20		25		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	20		25		ns	
$\overline{SOE}$ pulse width	t_{SOE}	15		20		ns	
$\overline{SOE}$ precharge time	t_{SOP}	15		20		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	20		25		ns	

Notes:

(1) See input/output timing waveforms for timing reference voltages.

(2) See figures 1 and 2 for output loads.

(3) An initial pause of 100 µs is required after power-up, followed by any eight $\overline{RAS}$ cycles (except $\overline{CAS}$-before-$\overline{RAS}$ cycles), before proper device operation is achieved. Also, $\overline{SOE}$ must be held high or SC must be held low until completion of the first data transfer cycle.

Notes [cont]:

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(6) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(7) Data in the serial output register remains valid for 4 ms (min) after a data transfer cycle.

(8) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

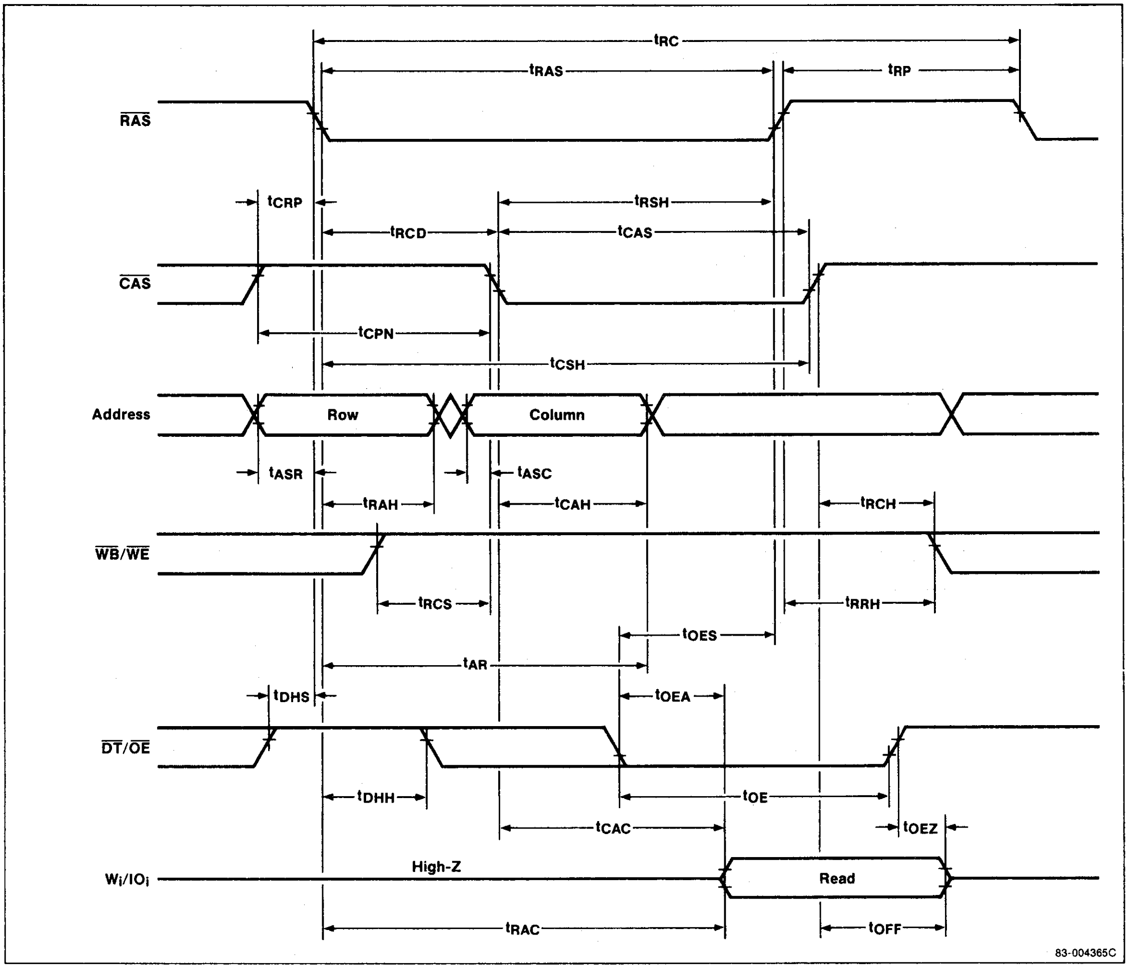
(9) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(10) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(11) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of ($\overline{WB}$/) $\overline{WE}$ in delayed write or read-modify-write cycles.

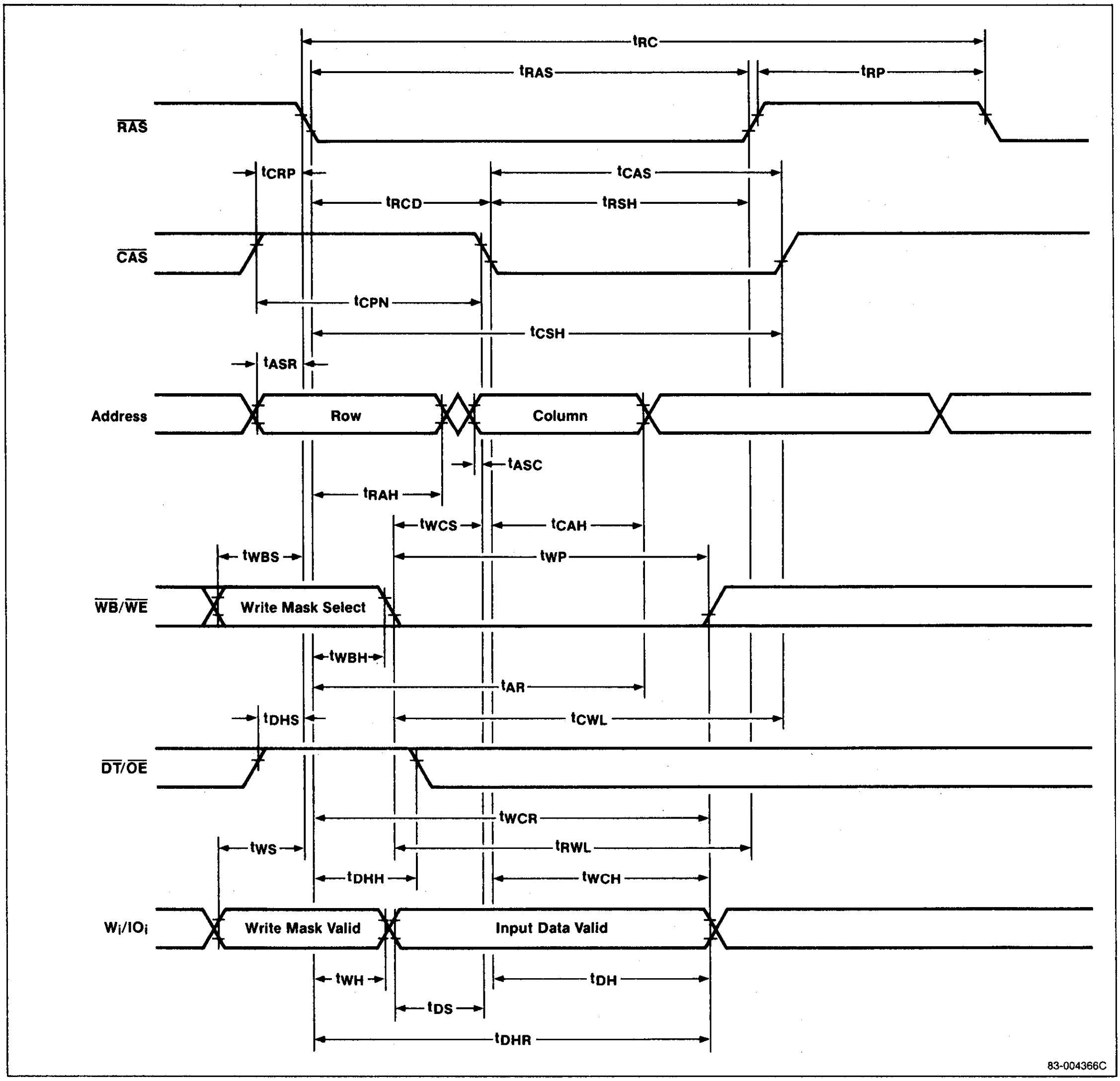
Timing Waveforms

Read Cycle



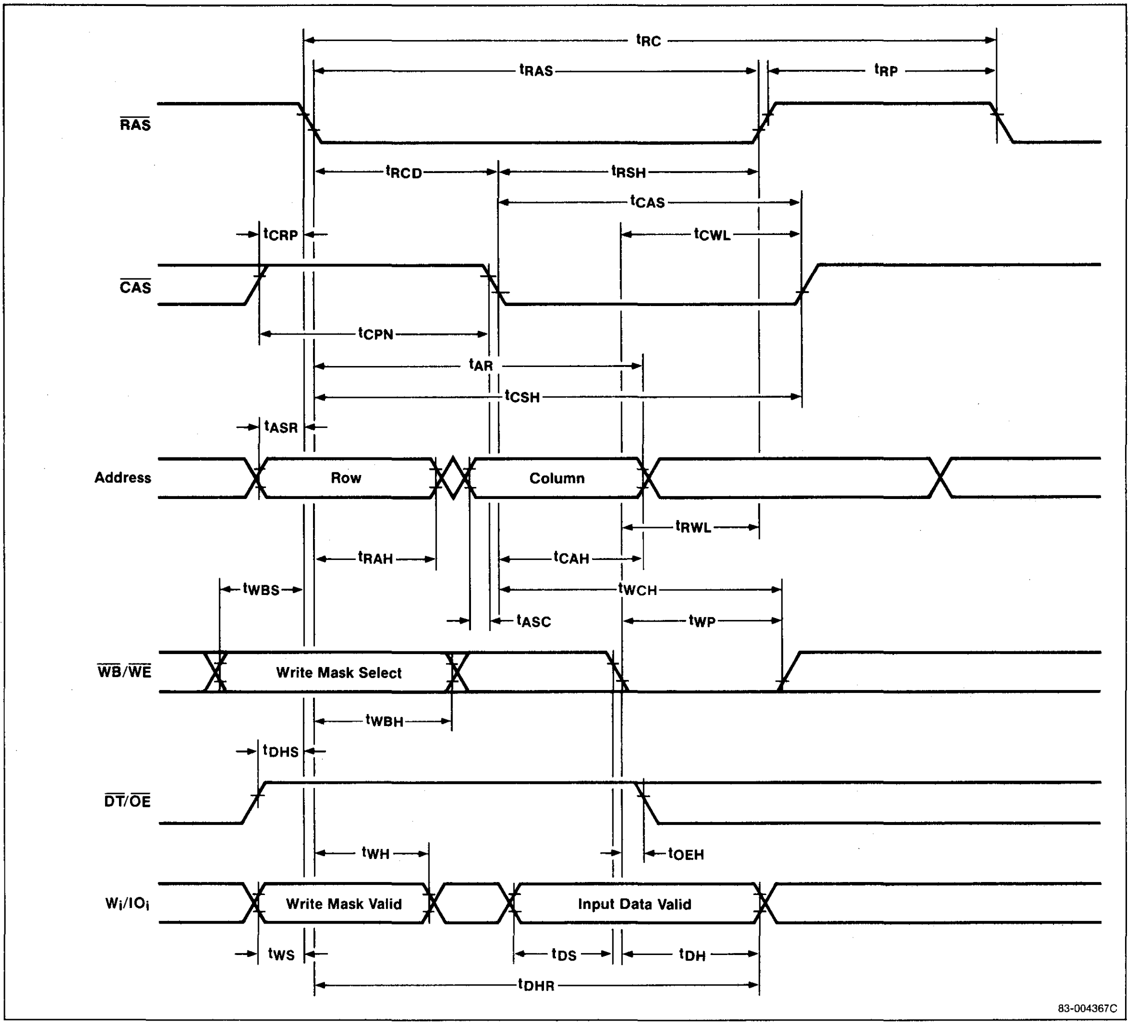
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Late Write Cycle



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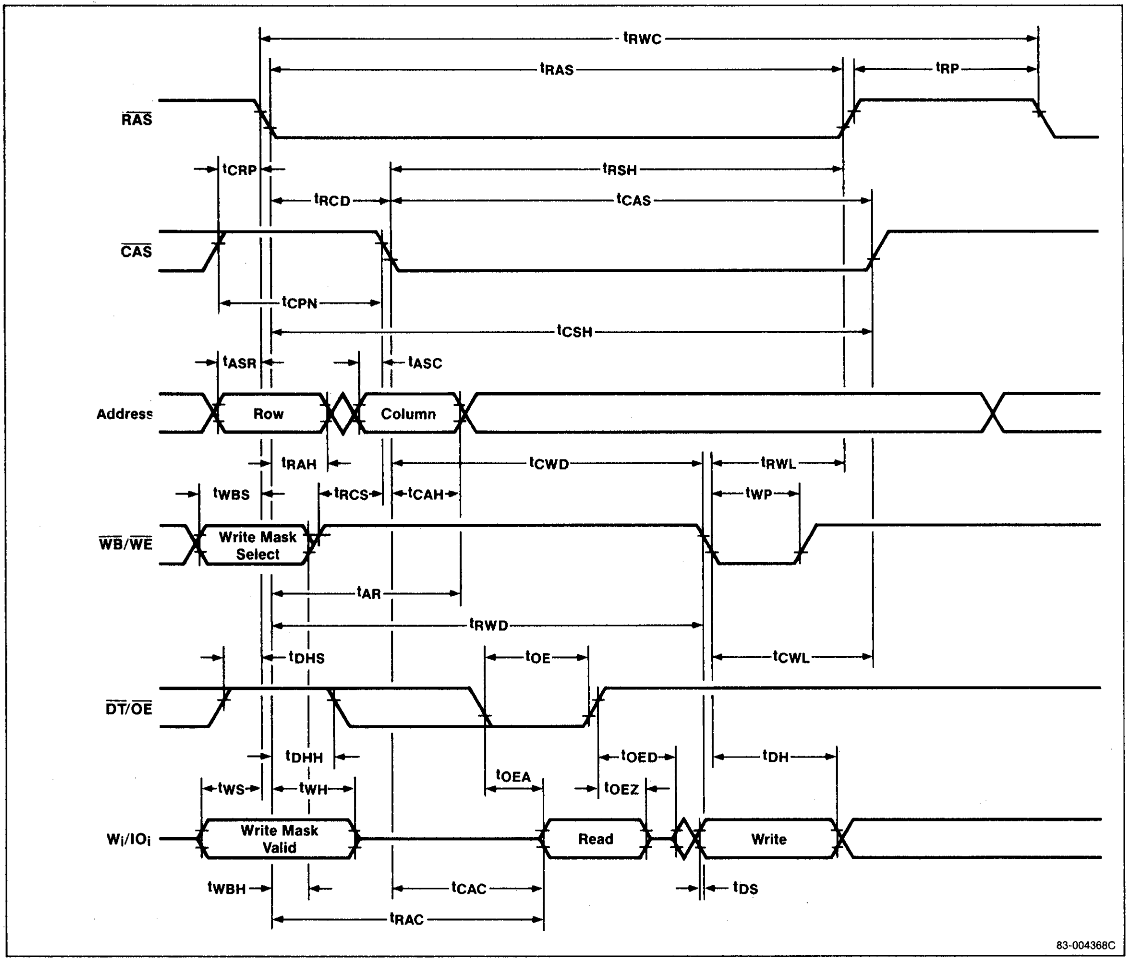
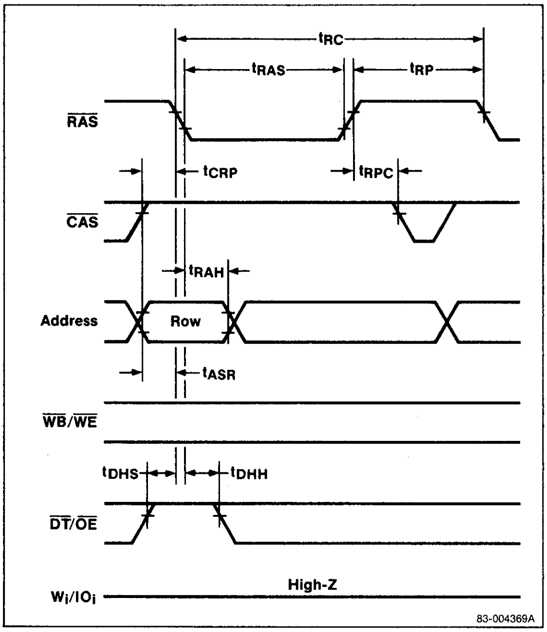
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycles

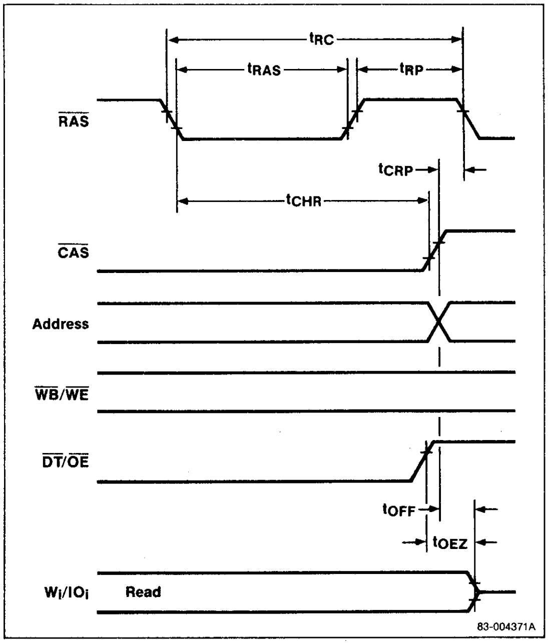


Timing Waveforms (cont)

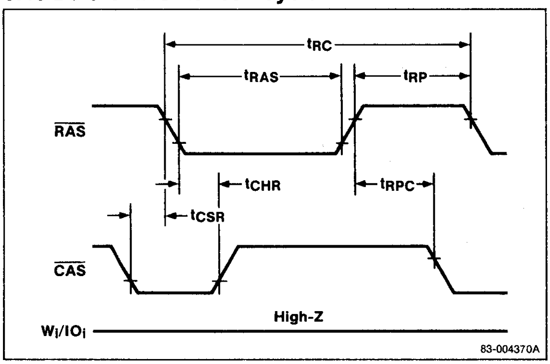
$\overline{RAS}$-Only Refresh



Hidden Refresh



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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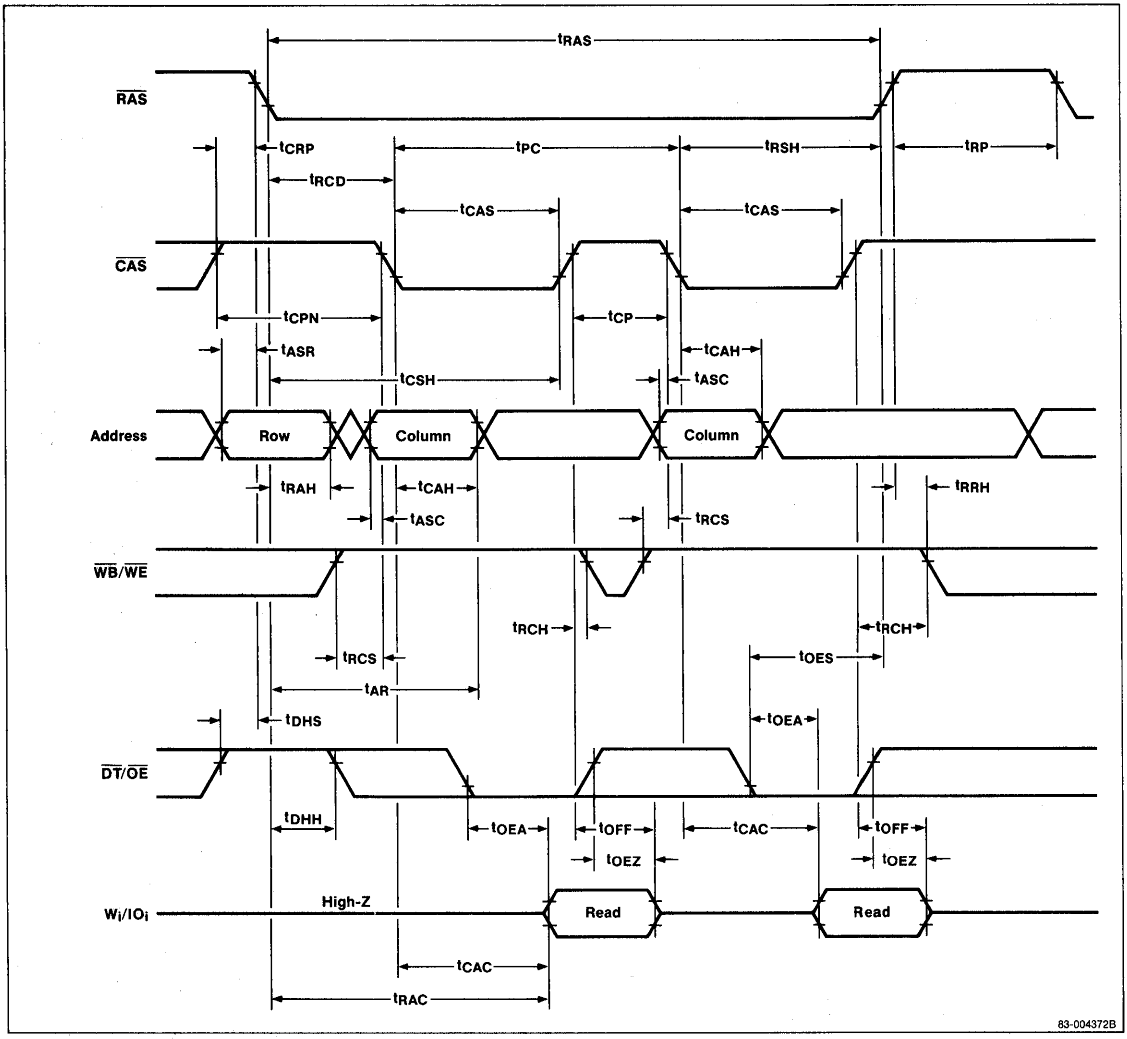
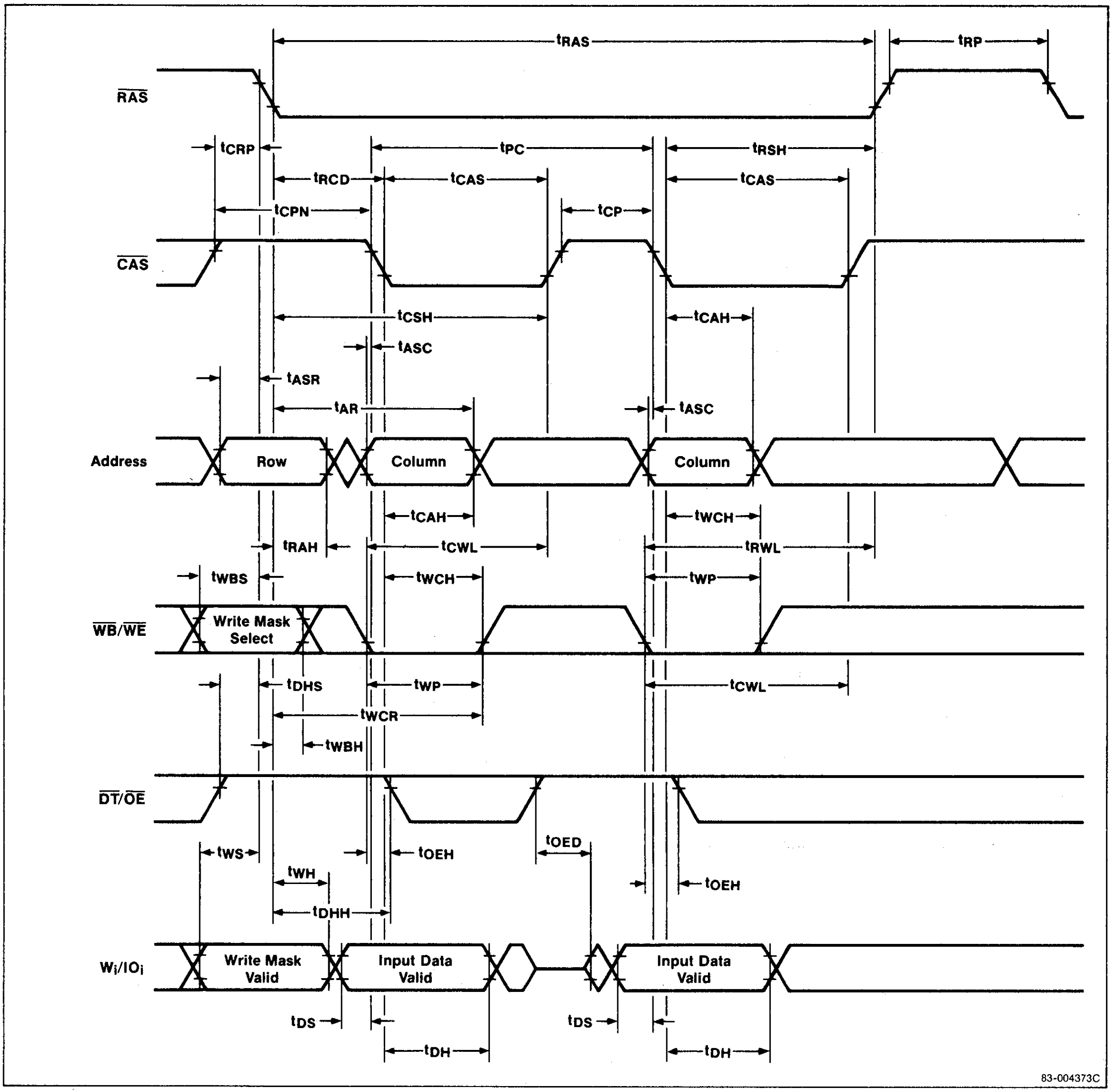
Timing Waveforms (cont)

Page Mode Read Cycle



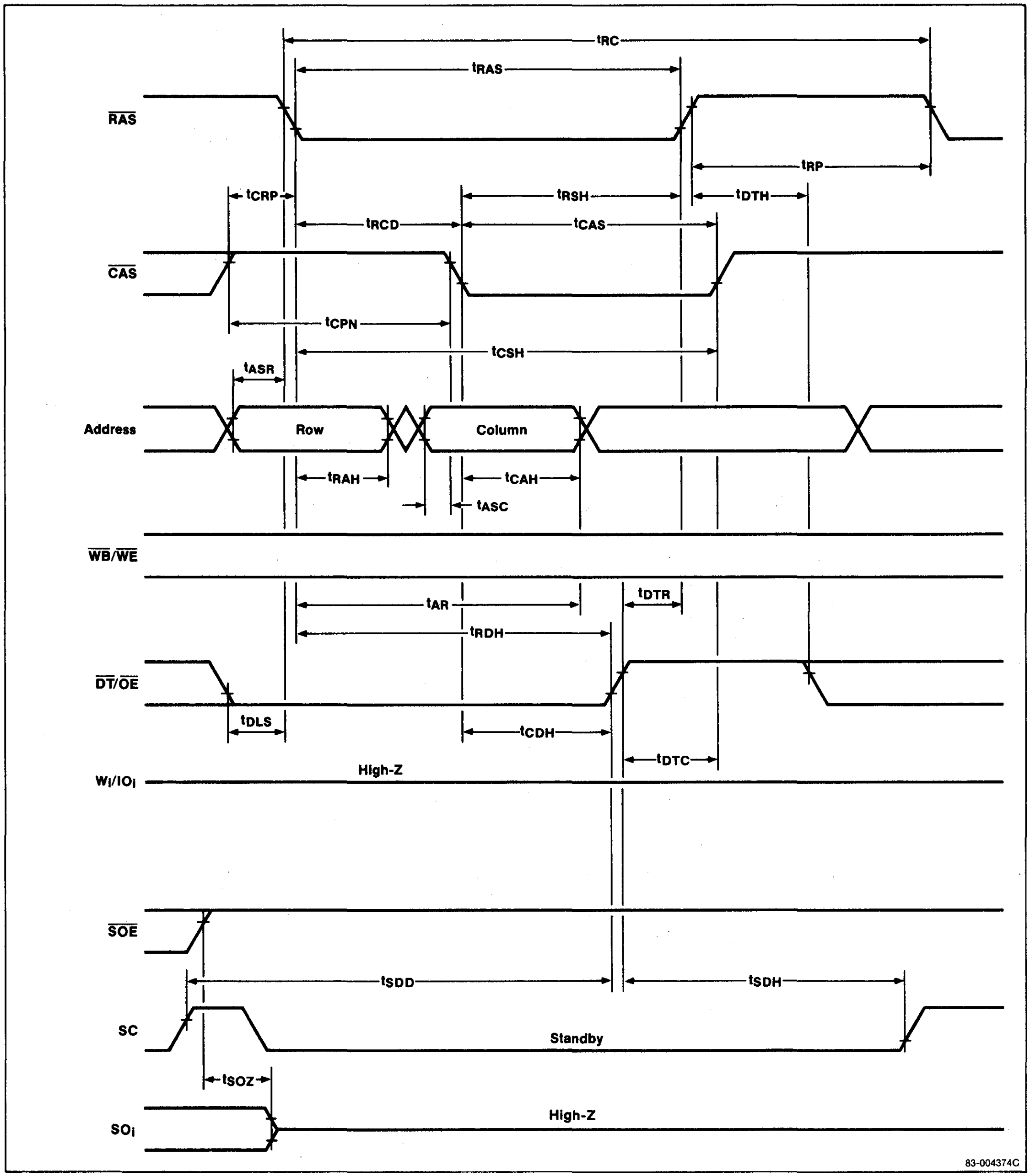
Timing Waveforms (cont)

Page Mode Write Cycle



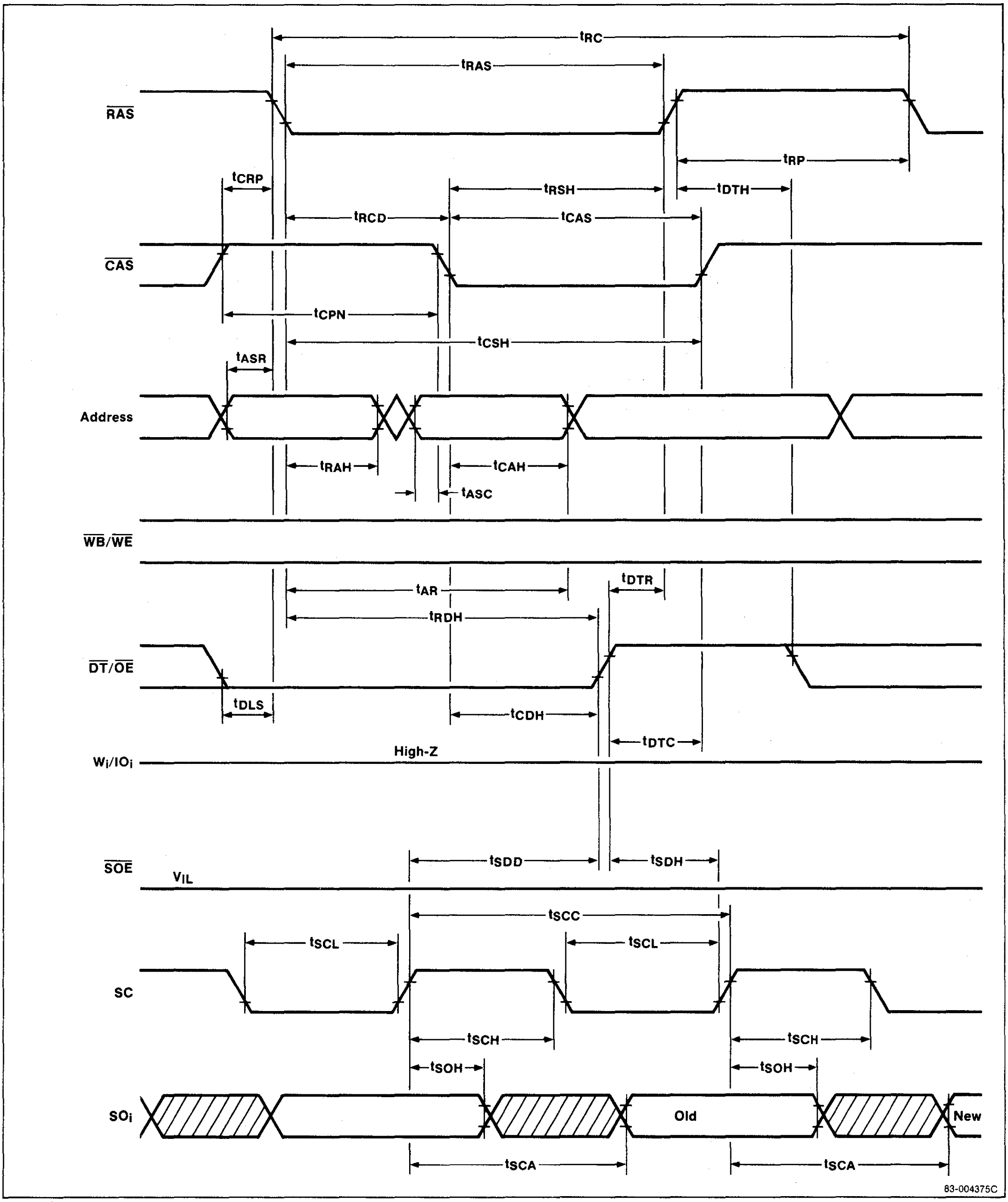
Timing Waveforms (cont)

Data Transfer Cycle (Port B Standby)



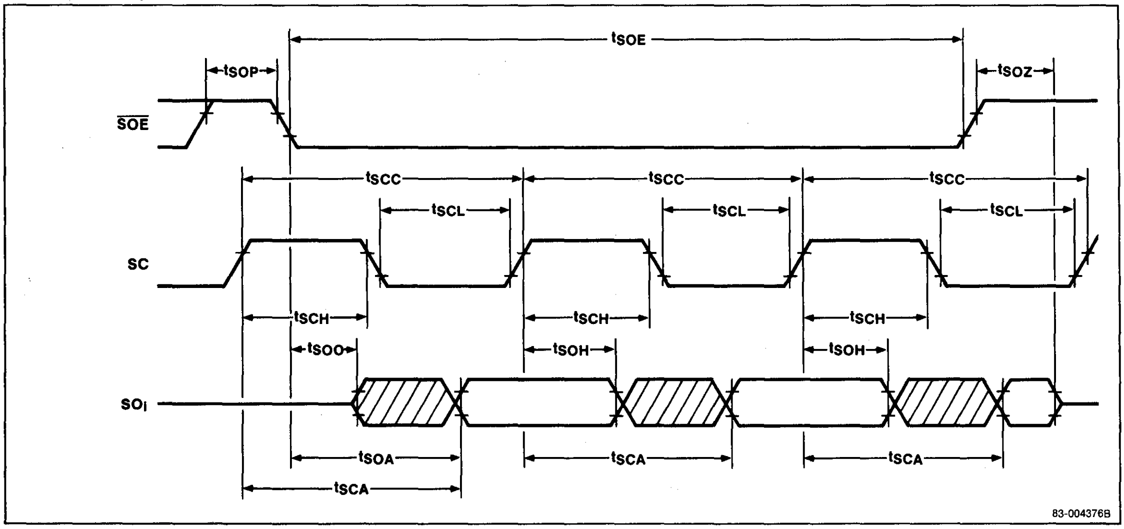
Timing Waveforms (cont)

Data Transfer Cycle (Port B Active)



Timing Waveforms (cont)

Serial Read Cycle



NEC
NEC Electronics Inc.

μPD42101
910 x 8-BIT
LINE BUFFER FOR NTSC TV

PRELIMINARY INFORMATION

Description

The μPD42101 is a 910-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create an NTSC flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42101 can also be used as a digital delay line. The delay length is variable from 10 bits (at maximum clock speed) to 910 bits.

Features

- □ 910-word x 8-bit organization
- □ Line buffer for NTSC, $4f_{SC}$ digital television systems
- □ Asynchronous and simultaneous read/write operation
- □ 1H (910-bit) delay line capability
- □ TTL-compatible inputs and outputs
- □ Three-state outputs
- □ Single 5-volt ±10% power supply
- □ 300-mil, 24-pin plastic DIP and 450-mil, 24-pin plastic miniflat packaging

Ordering Information

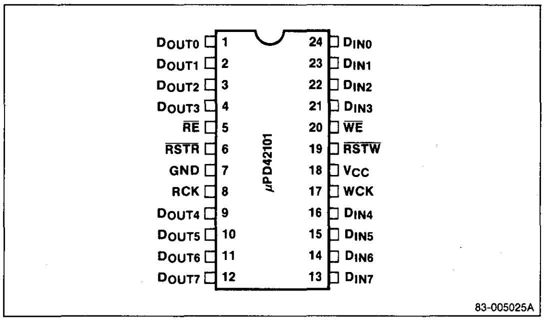
Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42101C-3	34 ns	34 ns	24-pin plastic DIP
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD42101G-3	34 ns	34 ns	24-pin plastic miniflat
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Identification

Symbol	Function
D_{IN0}-D_{IN7}	Write data inputs
D_{OUT0}-D_{OUT7}	Read data outputs
$\overline{\text{RSTW}}$	Write address reset input
$\overline{\text{RSTR}}$	Read address reset input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{RE}}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{\text{RSTW}}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0 if $\overline{\text{WE}}$ is also at a low level. If $\overline{\text{WE}}$ is at a high level when the $\overline{\text{RSTW}}$ input is brought low, the internal write address is set to 909. The state of this input is strobed by the rising edge of WCK.

$\overline{\text{RSTR}}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0 if $\overline{\text{RE}}$ is also at a low level. If $\overline{\text{RE}}$ is at a high level when the $\overline{\text{RSTR}}$ input is brought low, the internal read address is set to 909.

$\overline{\text{WE}}$ [Write Enable Input]

This input controls write operation. If $\overline{\text{WE}}$ is at a low level, all write cycles proceed. If $\overline{\text{WE}}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{\text{WE}}$ is strobed by the rising edge of WCK.

$\overline{\text{RE}}$ [Read Enable Input]

This signal is similar to $\overline{\text{WE}}$ but controls read operation. If $\overline{\text{RE}}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{\text{RE}}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]

All write cycles are executed synchronously with WCK. The states of both $\overline{\text{RSTW}}$ and $\overline{\text{WE}}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{\text{WE}}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{\text{WE}}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK [Read Clock Input]

All read cycles are executed synchronously with RCK. The states of both $\overline{\text{RSTR}}$ and $\overline{\text{RE}}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{\text{RE}}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{\text{RE}}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram

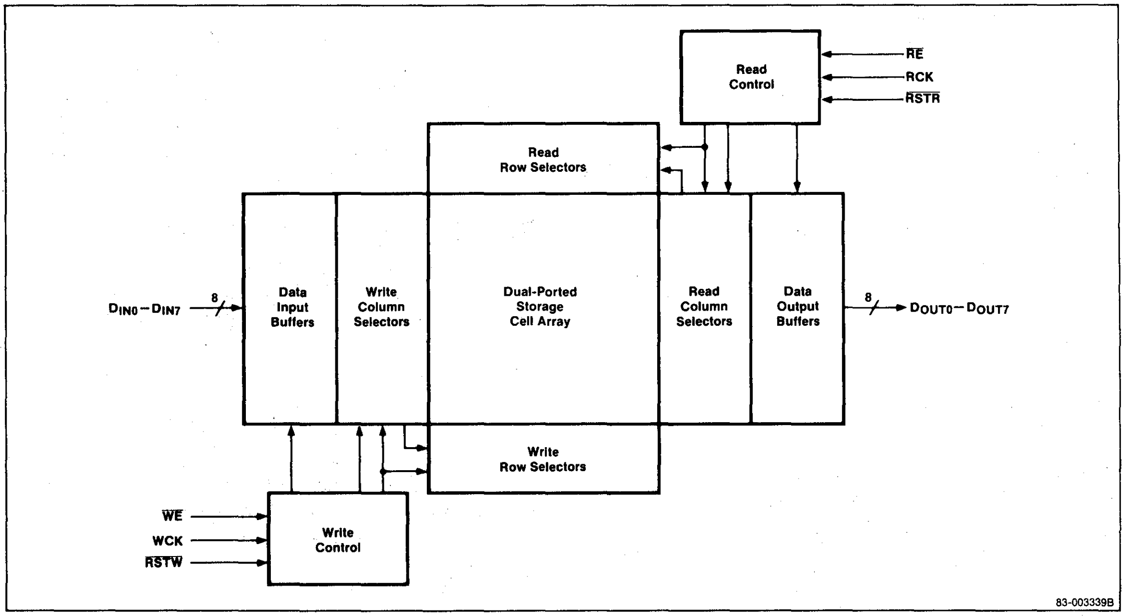
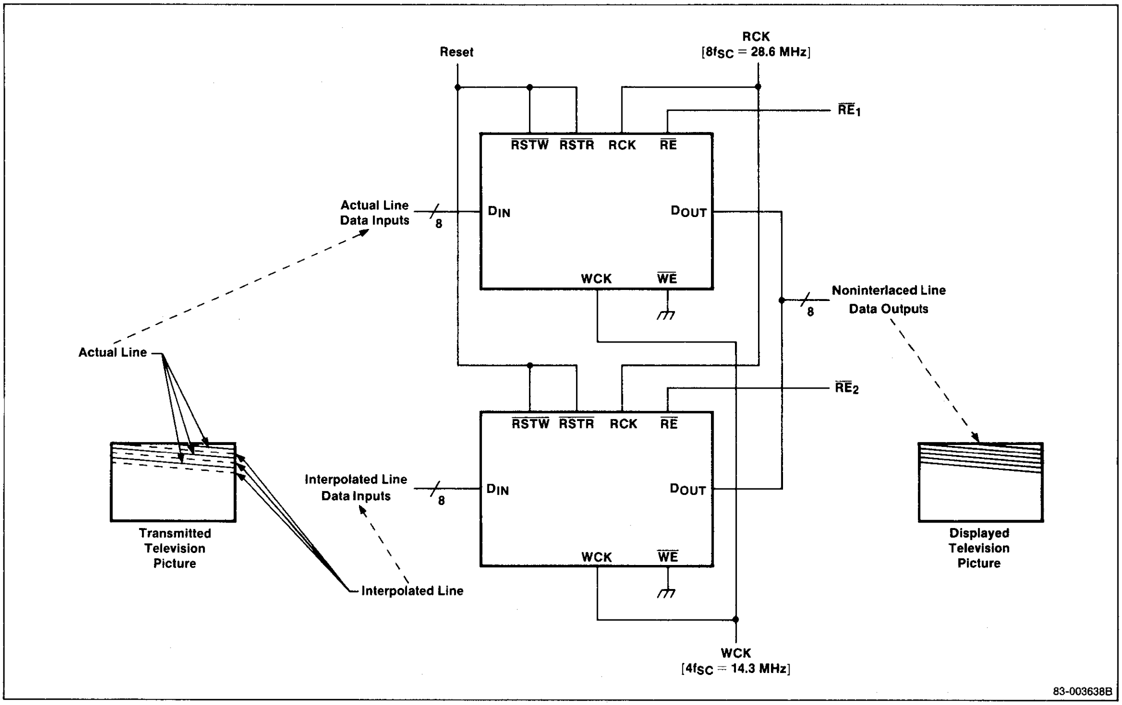


Figure 1. Connection for Noninterlaced Scan Conversion



Recommended DC Operating Conditions

T_A = −20 to +70°C; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

Notes:

(1) All voltages are referenced to ground.

3

AC Characteristics

T_A = −20 to +70 °C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD42101-3 Min	μPD42101-3 Max	μPD42101-2 Min	μPD42101-2 Max	μPD42101-1 Min	μPD42101-1 Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		70		60		35	mA	
Write clock cycle time	t_{WCK}	34	1090	69	1090	69	1090	ns	
WCK pulse width	t_{WCW}	14		25		25		ns	
WCK precharge time	t_{WCP}	14		25		25		ns	
Read clock cycle time	t_{RCK}	34	1090	34	1090	69	1090	ns	
RCK pulse width	t_{RCW}	14		14		25		ns	
RCK precharge time	t_{RCP}	14		14		25		ns	
Access time	t_{AC}		27		27		49	ns	Figure 5
Access time after a reset cycle	t_{ACR}		27		27		49	ns	
Output hold time	t_{OH}	5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		ns	Figure 5 (Note 7)
Output active time	t_{LZ}	5	27	5	27	5	49	ns	(Note 4)
Output disable time	t_{HZ}	5	27	5	27	5	49	ns	
Data-in setup time	t_{DS}	14		18		18		ns	
Data-in hold time	t_{DH}	5		5		5		ns	
Reset active setup time	t_{RS}	14		14		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		ns	
Reset inactive hold time	t_{RN1}	5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	14		14		20		ns	
Write enable setup time	t_{WES}	14		20		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		ns	
Write enable high delay from WCK	t_{WEN1}	5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	14		20		20		ns	
Read enable setup time	t_{RES}	14		14		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		ns	
Read enable high delay from RCK	t_{REN1}	5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	14		14		20		ns	
Write disable pulse width	t_{WEW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read disable pulse width	t_{REW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Write reset time	t_{RSTW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read reset time	t_{RSTR}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Transition time	t_T	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 3.

(3) Output timing reference levels are 0.8 and 2.0 volts. See figure 4.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 6. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristics (cont)

Notes [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (910-Bit) Delay Line

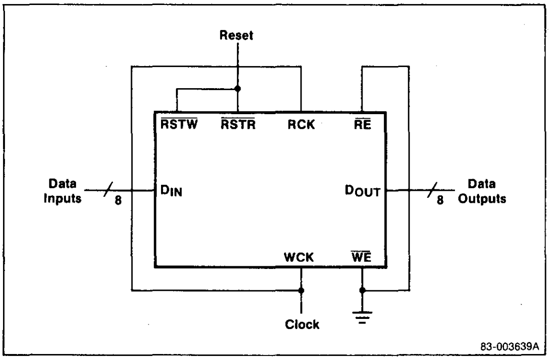


Figure 3. AC Input Timing Reference

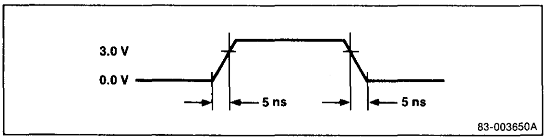


Figure 4. AC Output Timing Reference

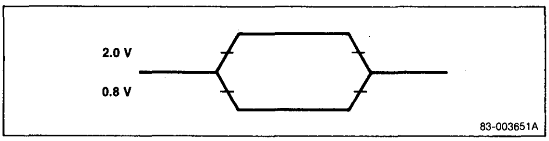


Figure 5. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

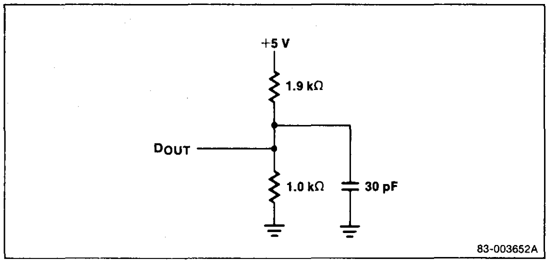
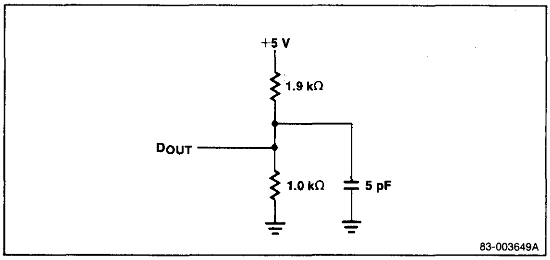


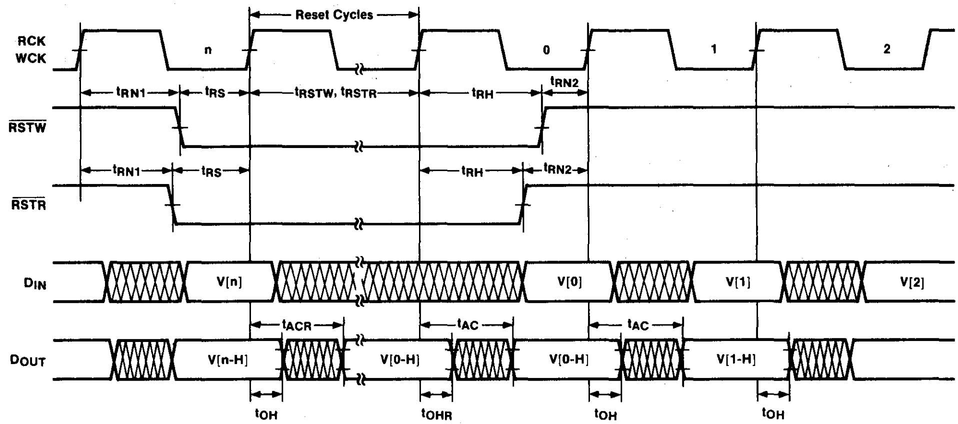
Figure 6. Output Load for t_{LZ} and t_{HZ}



3

Timing Waveforms

Read or Write Reset



Note:

[1] $\overline{WE} = \overline{RE} = V_{IL}$.

[2] V = Valid Data.

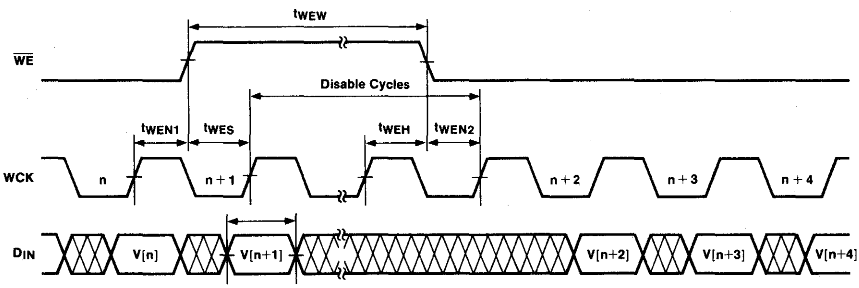
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 910 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-003645B

Write Disable



Note:

[1] V = Valid Data.

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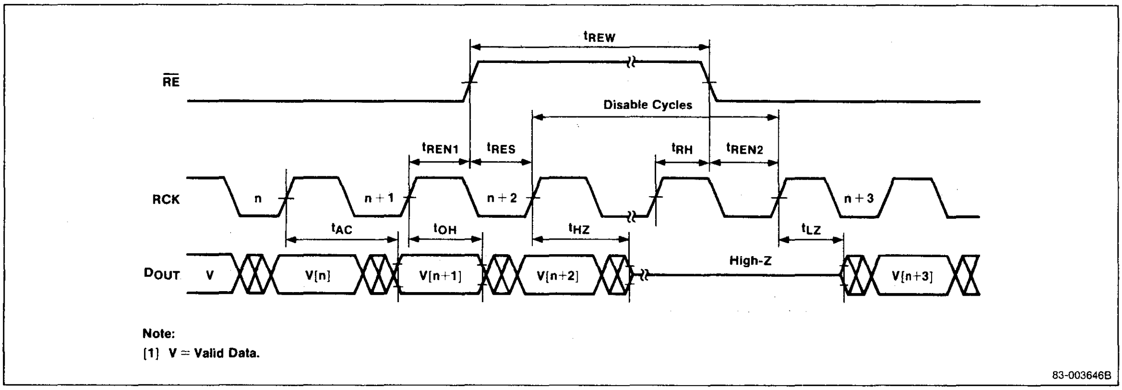
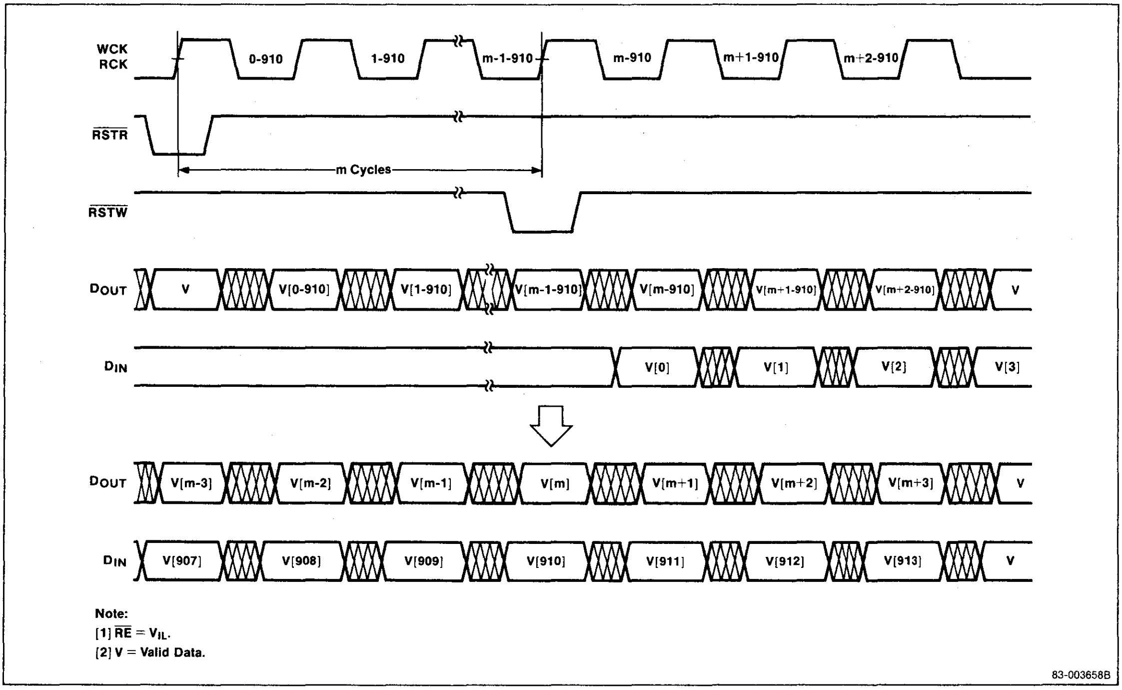
Timing Waveforms (cont)

Read Disable



(910-m)-Bit Delay Line, No. 1



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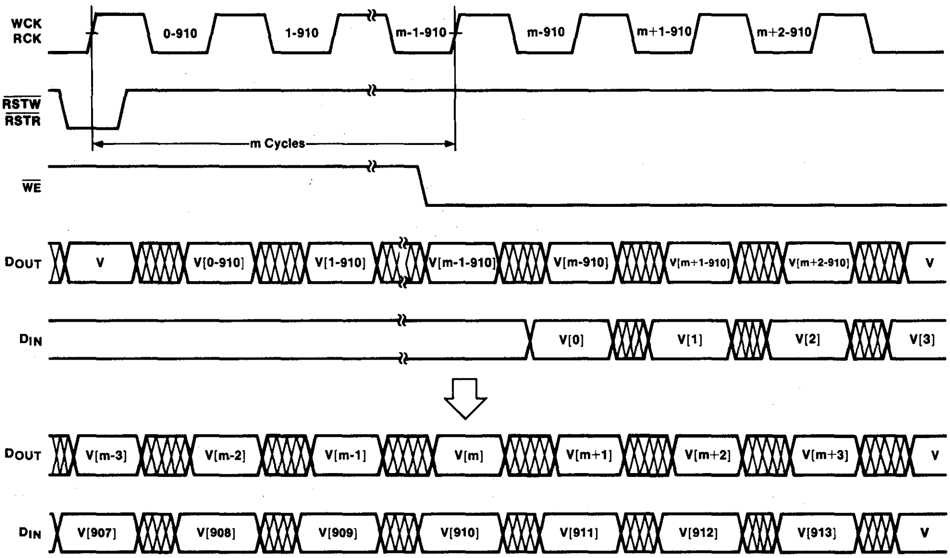
Timing Waveforms (cont)

(910-m)-Bit Delay Line, No. 2



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

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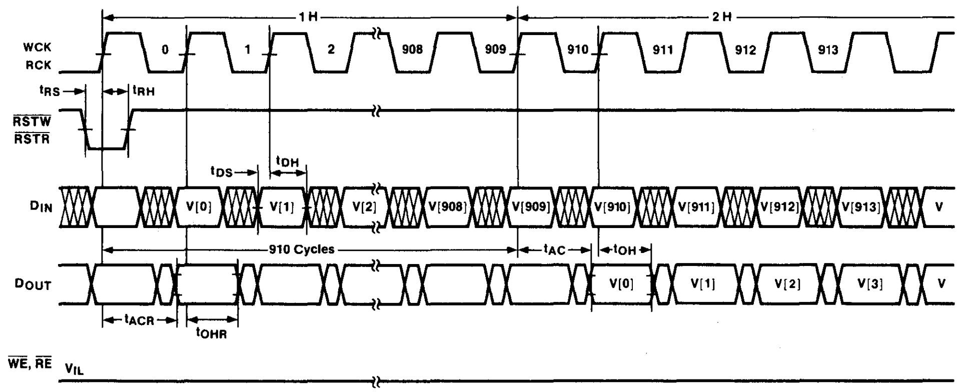
Timing Waveforms (cont)

910-Bit Delay Line



Note:

[1] V = Valid Data.

[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits.

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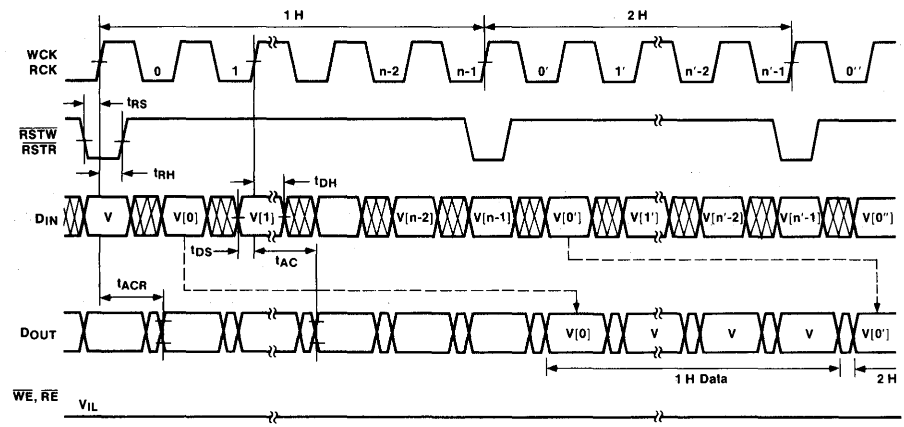
Timing Waveforms (cont)

n-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

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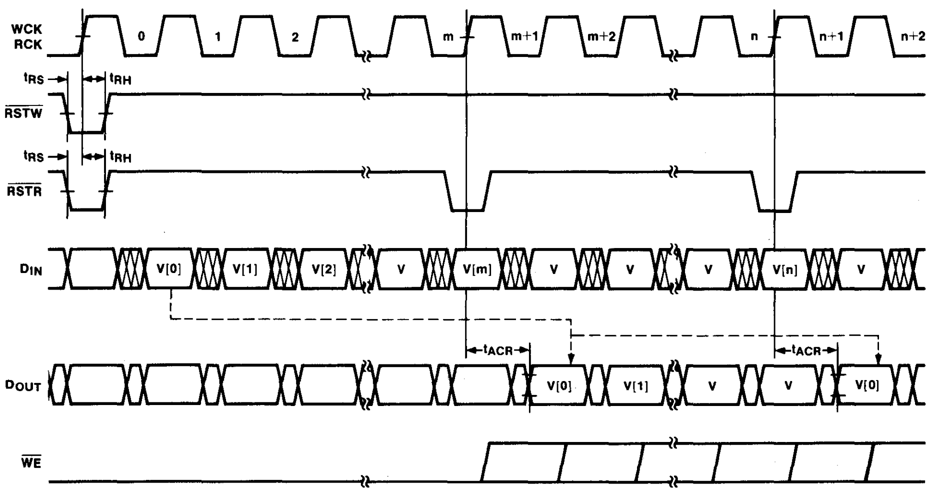
Re-Read Operation



Note:
[1] RE = V_{IL}.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

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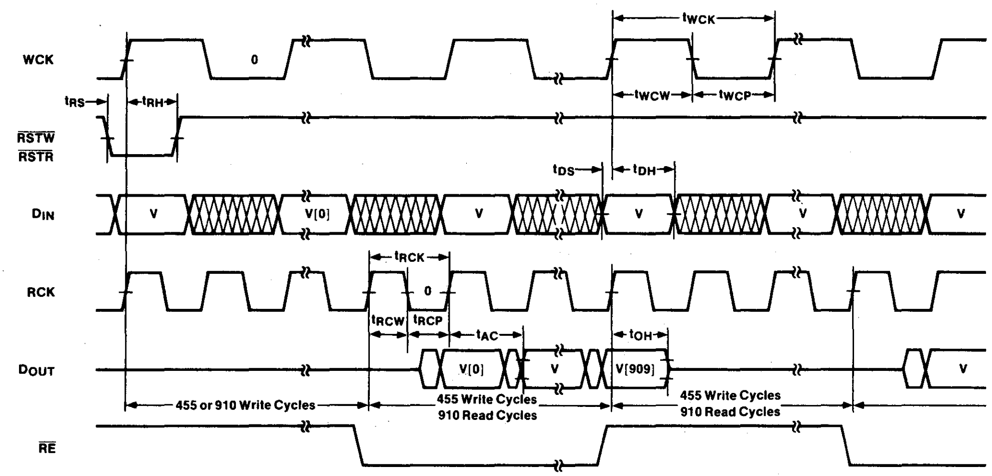
Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = Valid Data.
[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

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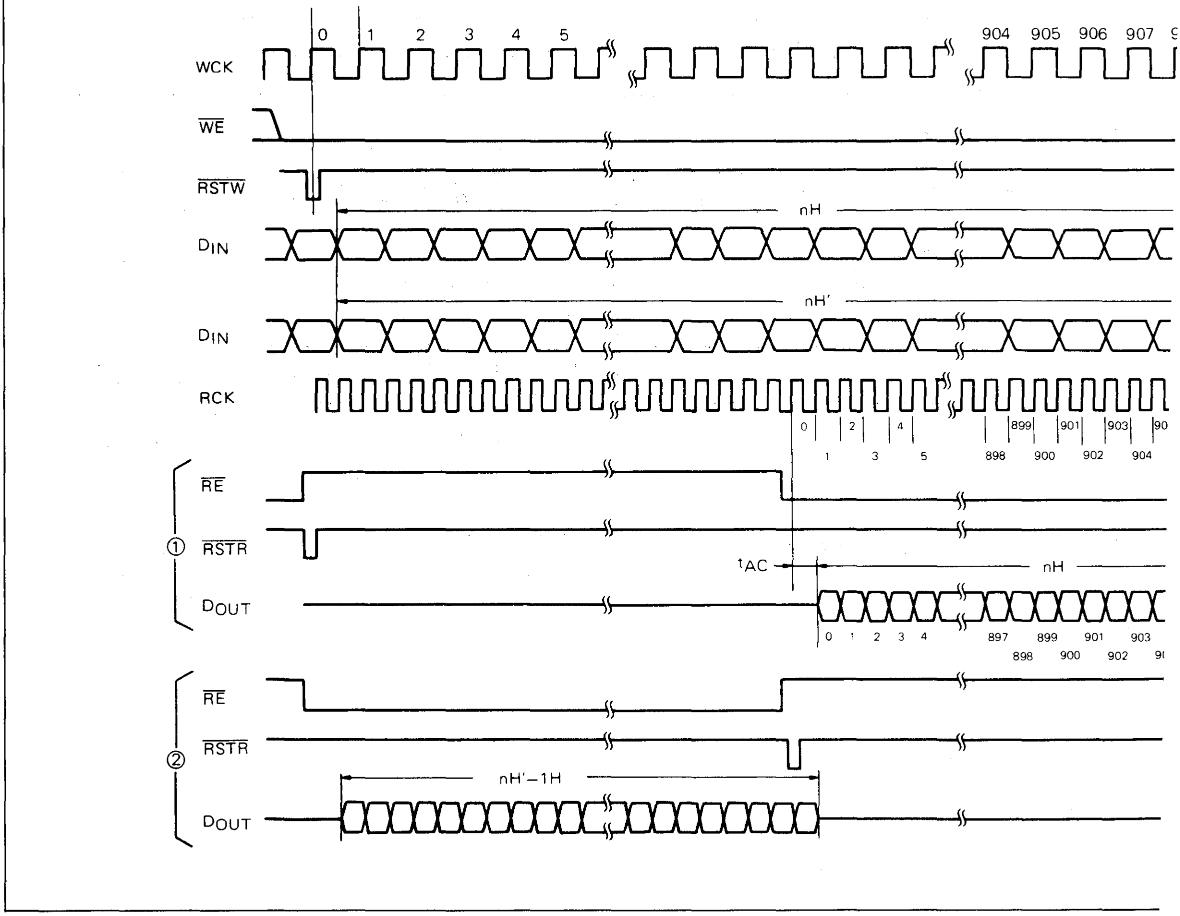
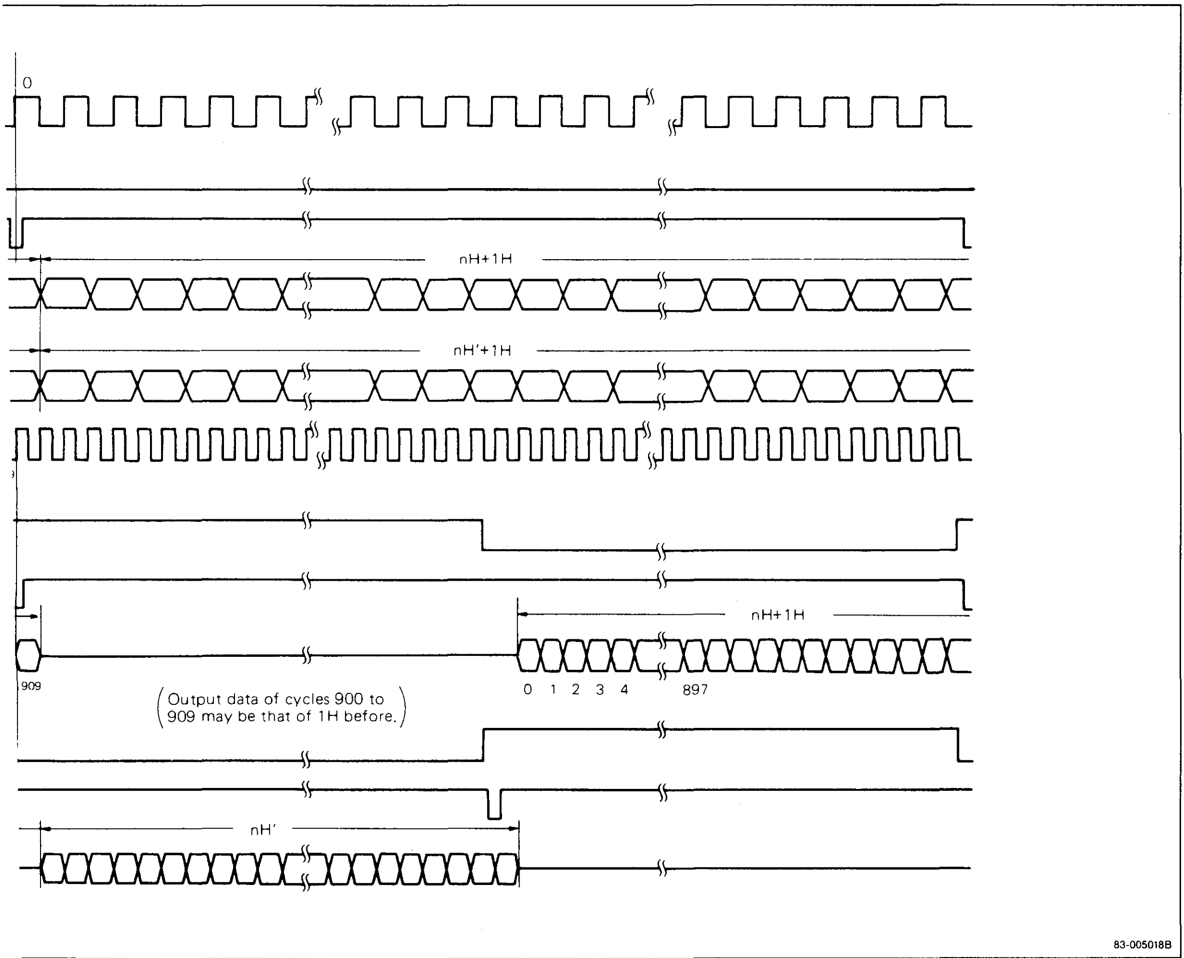
NEC

Timing Waveforms (cont)

Application Timing for Noninterlaced Scan Conversion




0
nH+1H
nH'+1H
nH+1H
909
0 1 2 3 4 897
Output data of cycles 900 to 909 may be that of 1H before.
nH'
83-005018B

3

NEC

NEC Electronics Inc.

μPD42102 1135 x 8-BIT LINE BUFFER FOR PAL TV

PRELIMINARY INFORMATION

Description

The μPD42102 is a 1135-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create a PAL flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42102 can also be used as a digital delay line. The delay length is variable from 12 bits (at maximum clock speed) to 1135 bits.

Features

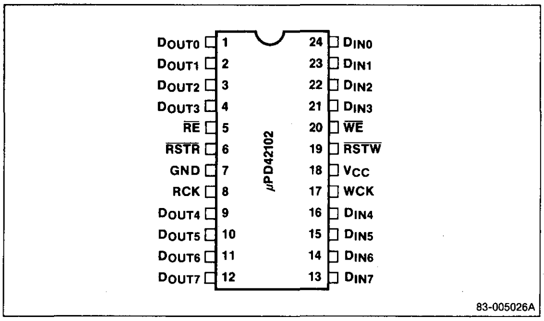
- ☐ 1135-word x 8-bit organization
- ☐ Line buffer for PAL, $4f_{SC}$ digital television systems
- ☐ Asynchronous and simultaneous read/write operation
- ☐ 1H (1135-bit) delay line
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt ±10% power supply
- ☐ 300-mil, 24-pin plastic DIP and 450-mil, 24-pin plastic miniflat packaging

Ordering Information

Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42102C-3	28 ns	28 ns	24-pin plastic DIP
C-2	28 ns	56 ns	
C-1	56 ns	56 ns	
μPD42102G-3	28 ns	28 ns	24-pin plastic miniflat
G-2	28 ns	56 ns	
G-1	56 ns	56 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0}-D_{IN7}	Write data inputs
D_{OUT0}-D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

3

Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

In a digital television application, the digital composite signal, luminance, chrominance, etc., information is written into these inputs.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{\text{RSTW}}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0 if $\overline{\text{WE}}$ is also at a low level. If $\overline{\text{WE}}$ is at a high level when the $\overline{\text{RSTW}}$ input is brought low, the internal write address is set to 1134. The state of this input is strobed by the rising edge of WCK.

$\overline{\text{RSTR}}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0 if $\overline{\text{RE}}$ is also at a low level. If $\overline{\text{RE}}$ is at a high level when the $\overline{\text{RSTR}}$ input is brought low, the internal read address is set to 1134.

$\overline{\text{WE}}$ [Write Enable Input]

This input controls write operation. If $\overline{\text{WE}}$ is at a low level, all write cycles proceed. If $\overline{\text{WE}}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{\text{WE}}$ is strobed by the rising edge of WCK.

$\overline{\text{RE}}$ [Read Enable Input]

This signal is similar to $\overline{\text{WE}}$ but controls read operation. If $\overline{\text{RE}}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{\text{RE}}$ is strobed by the rising edge of RCK.

WCK [Write Clock Input]

All write cycles are executed synchronously with WCK. The states of both RSTW and $\overline{\text{WE}}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{\text{WE}}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{\text{WE}}$, the internal write address will automatically wrap around from 1134 to 0 and begin increasing again.

RCK [Read Clock Input]

All read cycles are executed synchronously with RCK. The states of both $\overline{\text{RSTR}}$ and $\overline{\text{RE}}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{\text{RE}}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{\text{RE}}$, the internal read address will automatically wrap around from 1134 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram

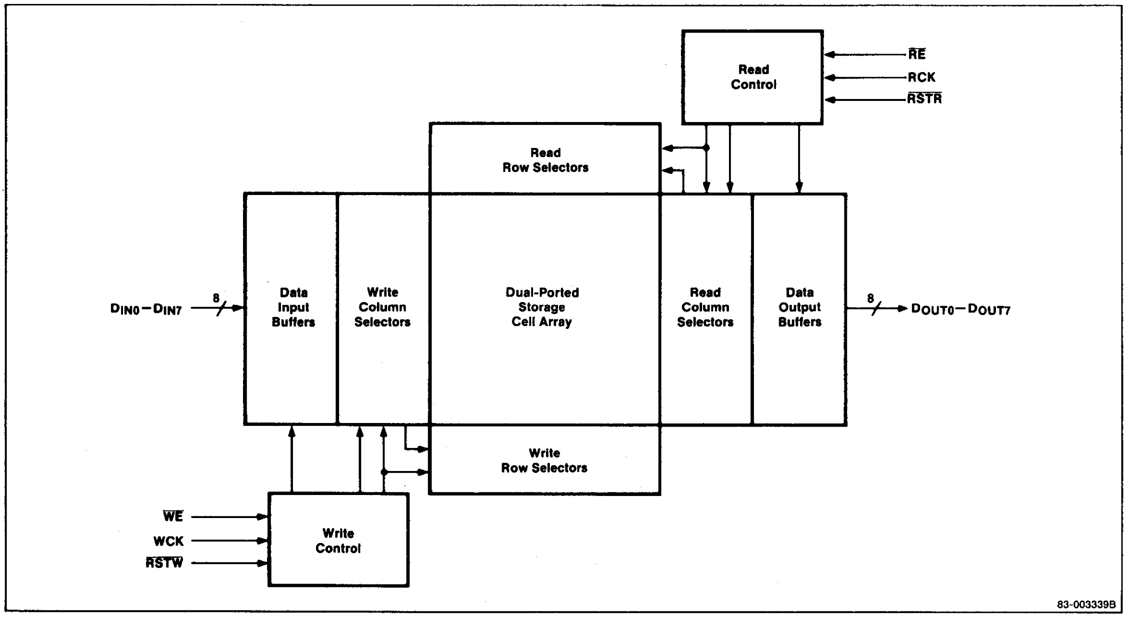


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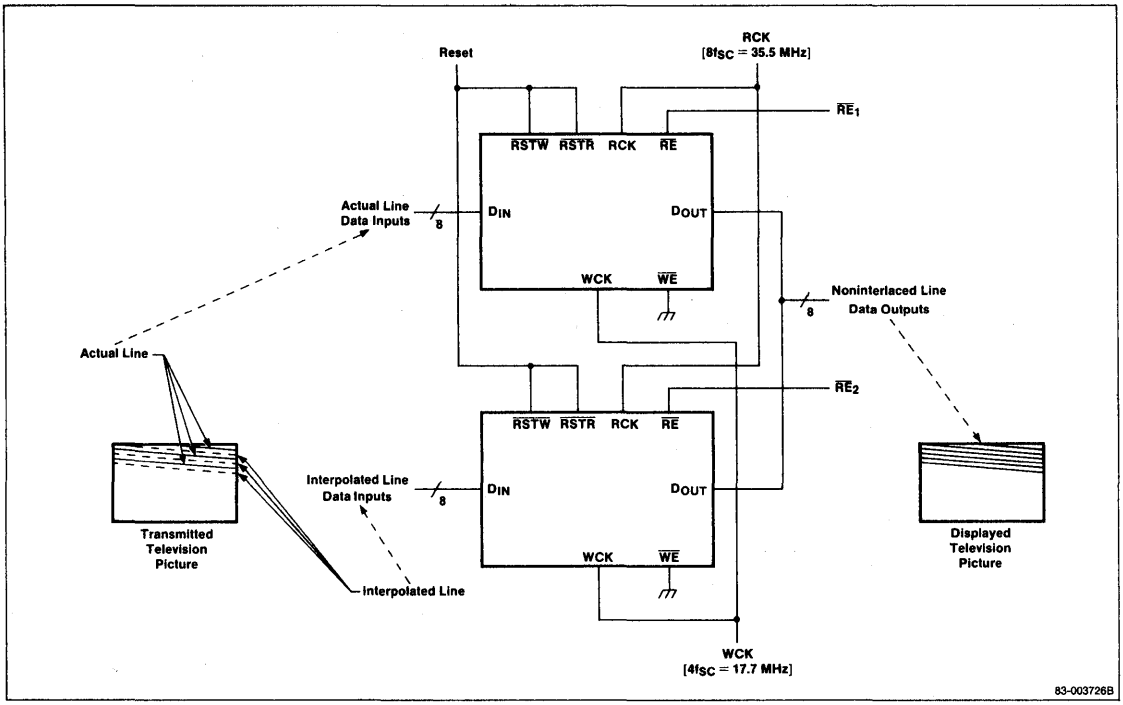
Figure 1. Connection for Noninterlaced Scan Conversion



Recommended DC Operating Conditions

T_A = −20 to +70°C; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

Notes:

(1) All voltages are referenced to ground.

AC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

		Limits							
		μPD42102-3		μPD42102-2		μPD42102-1			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		80		70		40	mA	
Write clock cycle time	t_{WCK}	28	880	56	880	56	880	ns	
WCK pulse width	t_{WCW}	12		20		20		ns	
WCK precharge time	t_{WCP}	12		20		20		ns	
Read clock cycle time	t_{RCK}	28	880	28	880	56	880	ns	
RCK pulse width	t_{RCW}	12		12		20		ns	
RCK precharge time	t_{RCP}	12		12		20		ns	
Access time	t_{AC}		21		21		40	ns	Figure 5
Access time after a reset cycle	t_{ACR}		21		21		40	ns	
Output hold time	t_{OH}	5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		ns	Figure 5 (Note 7)
Output active time	t_{LZ}	5	21	5	21	5	40	ns	(Note 4)
Output disable time	t_{HZ}	5	21	5	21	5	40	ns	
Data-in setup time	t_{DS}	12		15		15		ns	
Data-in hold time	t_{DH}	5		5		5		ns	
Reset active setup time	t_{RS}	12		12		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		ns	
Reset inactive hold time	t_{RN1}	5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	12		12		20		ns	
Write enable setup time	t_{WES}	12		20		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		ns	
Write enable high delay from WCK	t_{WEN1}	5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	12		20		20		ns	
Read enable setup time	t_{RES}	12		12		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		ns	
Read enable high delay from RCK	t_{REN1}	5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	12		12		20		ns	
Write disable pulse width	t_{WEW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read disable pulse width	t_{REW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Write reset time	t_{RSTW}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Read reset time	t_{RSTR}	0	(Note 6)	0	(Note 6)	0	(Note 6)	ms	
Transition time	t_T	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 3.

(3) Output timing reference levels are 0.8 and 2.0 volts. See figure 4.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 6. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

AC Characteristics (cont)

Notes [cont]:

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1 line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) This parameter has meaning when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 2. Connection for a 1H (1135-Bit) Delay Line

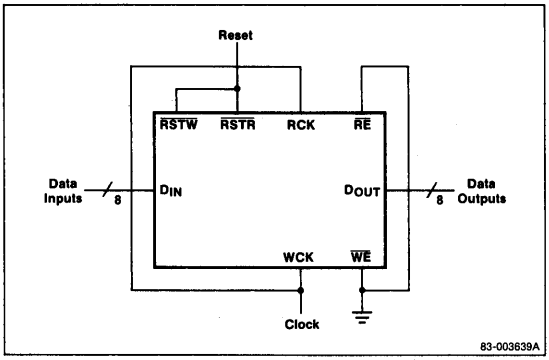


Figure 3. AC Input Timing Reference

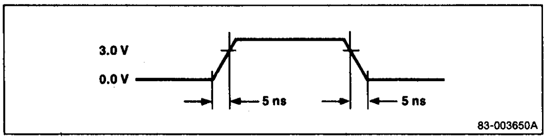


Figure 4. AC Output Timing Reference

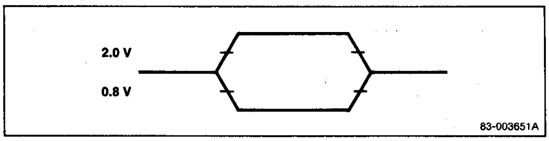


Figure 5. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

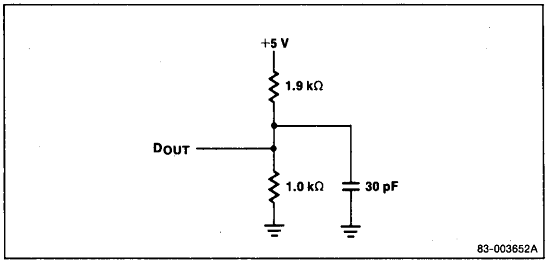
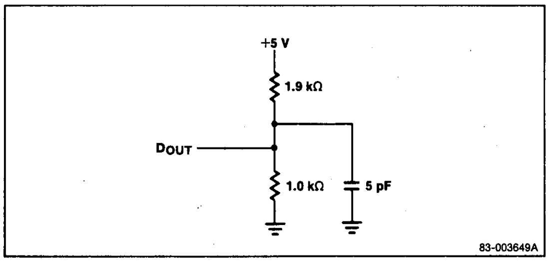
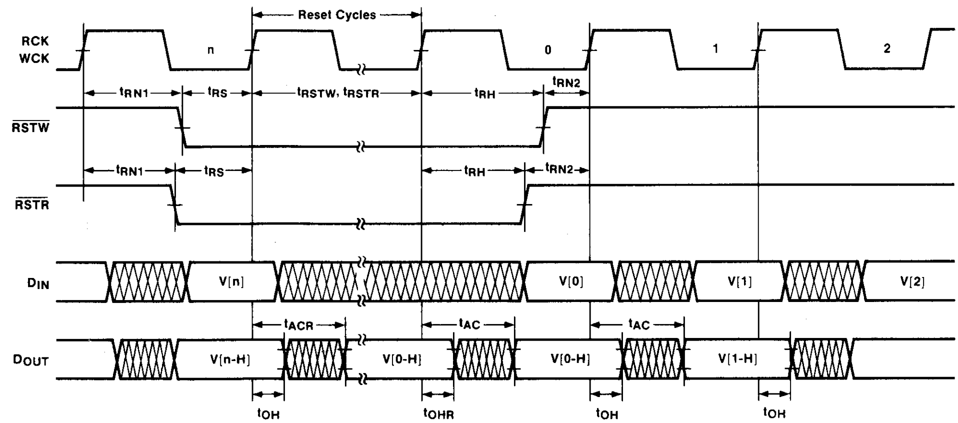


Figure 6. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

Read or Write Reset



Note:

[1] $\overline{WE} = \overline{RE} = V_{IL}$

[2] V = Valid Data.

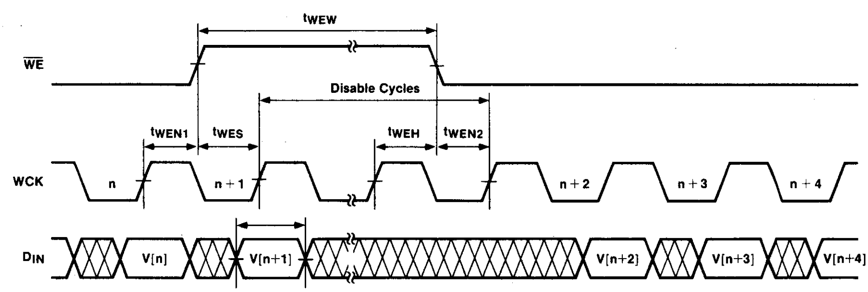
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 1135 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-003727B

Write Disable



Note:

[1] V = Valid Data.

83-003723B

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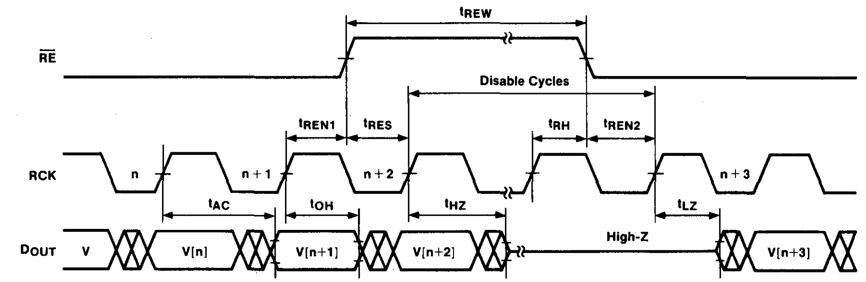
Timing Waveforms (cont)

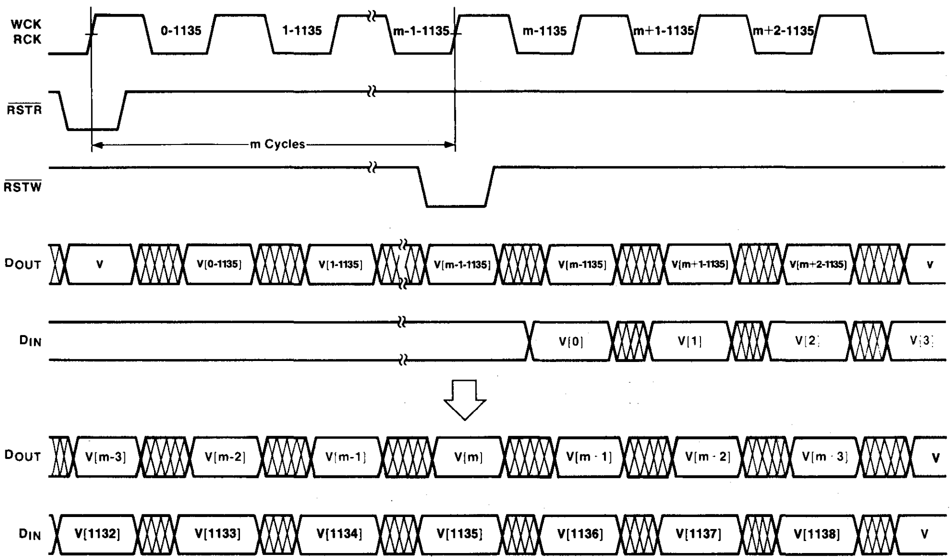
Read Disable



Note:
[1] V = Valid Data.

83-003646B

(1135-m)-Bit Delay Line, No. 1

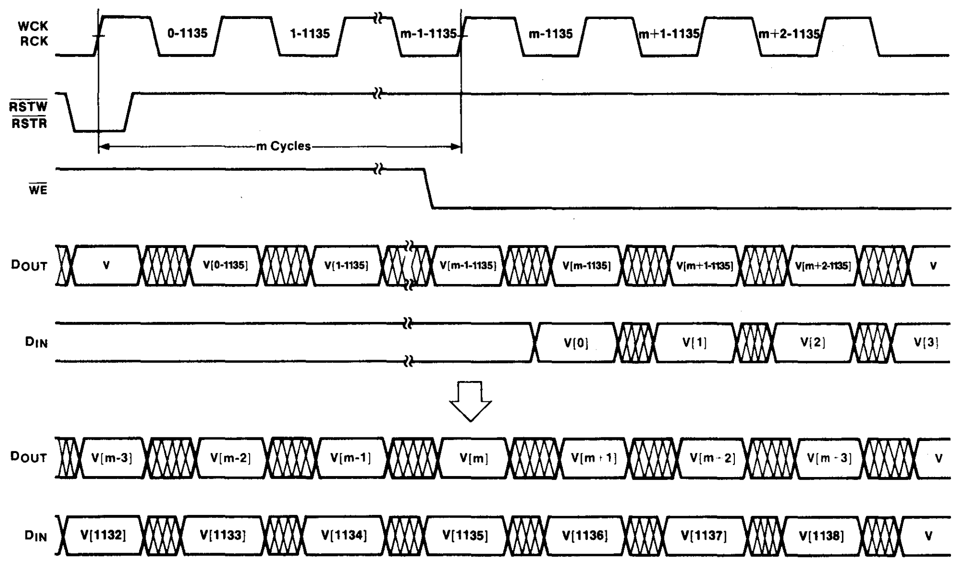


Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003647B

Timing Waveforms (cont)

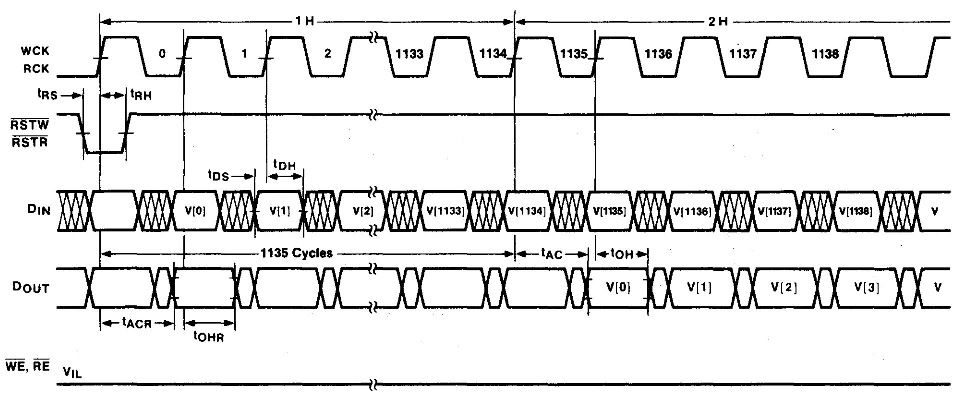
(1135-m)-Bit Delay Line, No. 2



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = Valid Data.

83-003648B

1135-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of 1135 bits. 2H = the second group of 1135 bits.

83-003642B

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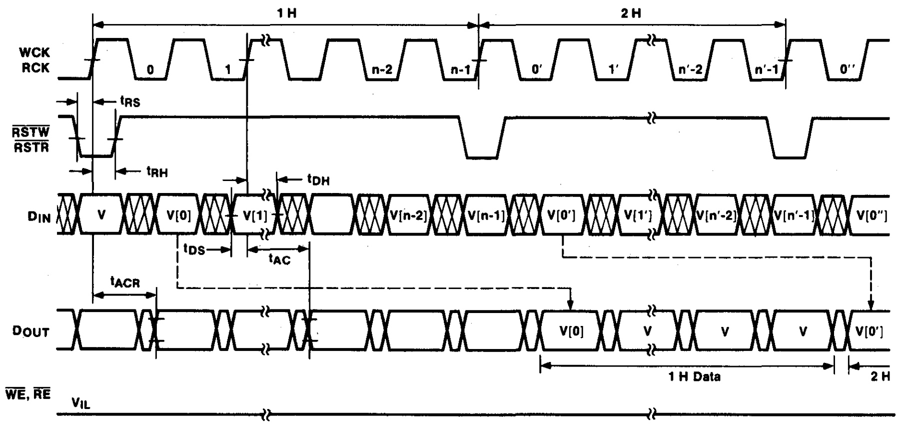
Timing Waveforms (cont)

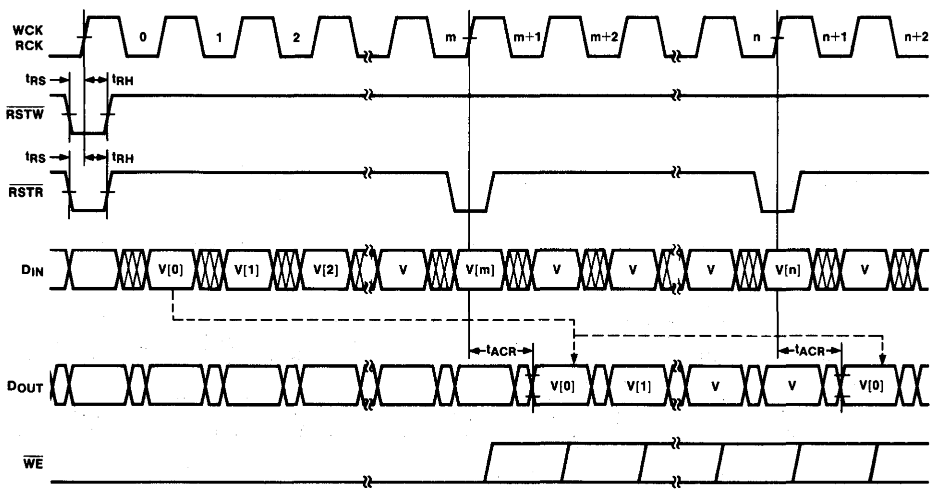
n-Bit Delay Line



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

83-003643B

Re-Read Operation

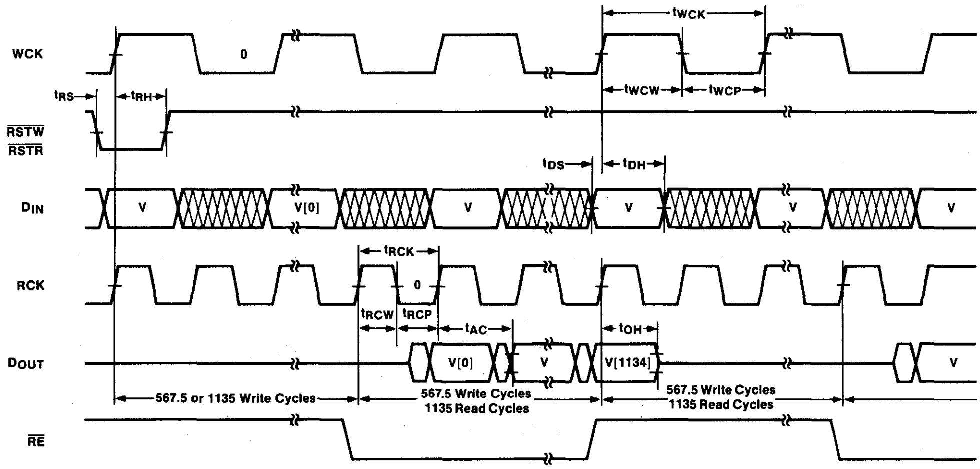


Note:
[1] $\overline{RE}$ = V_{IL}.
[2] V = Valid Data.
[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

[3] For compatibility with PAL standards the WCK frequency is approximately 17.7 MHz. RCK cycles at twice this frequency, 35.5 MHz.

83-003640B

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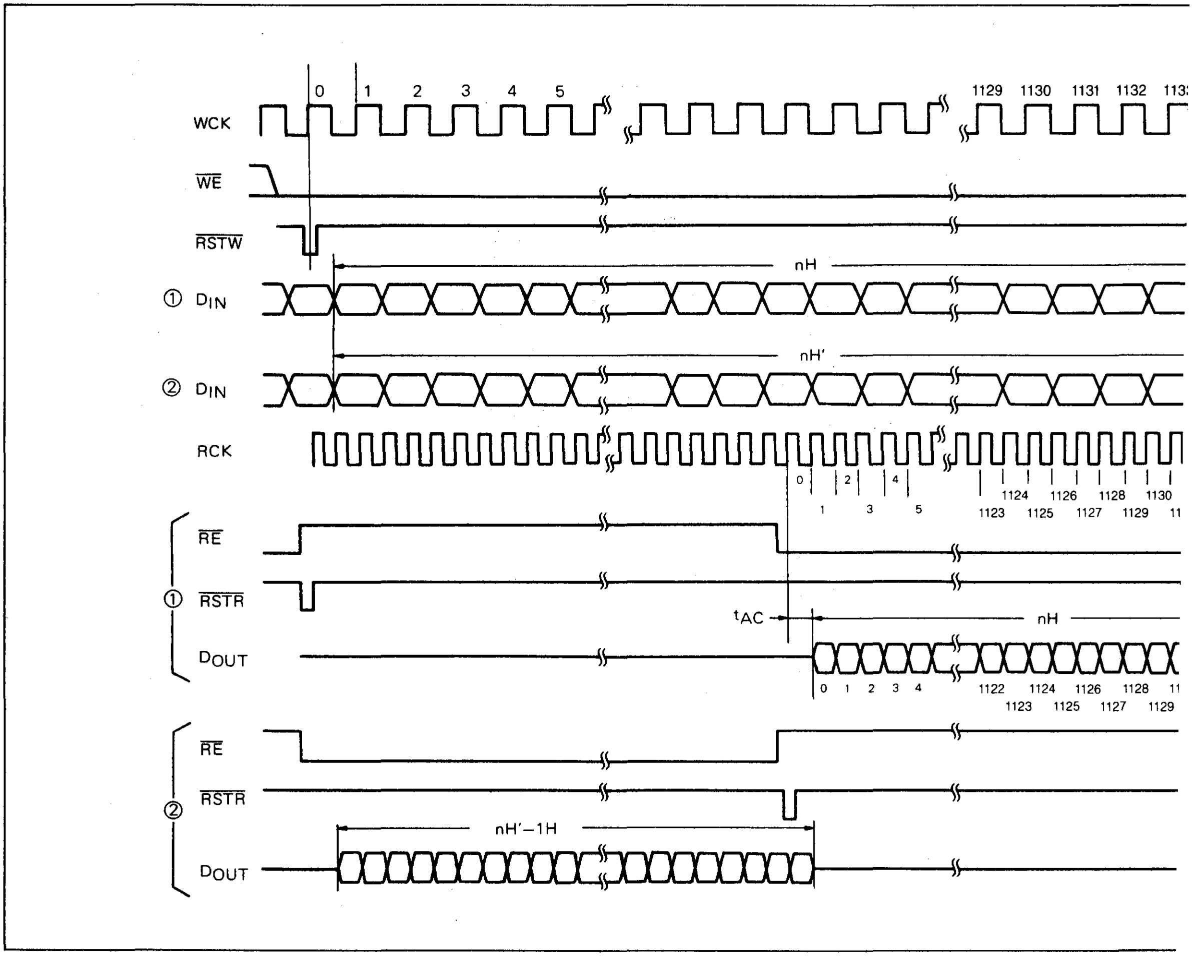
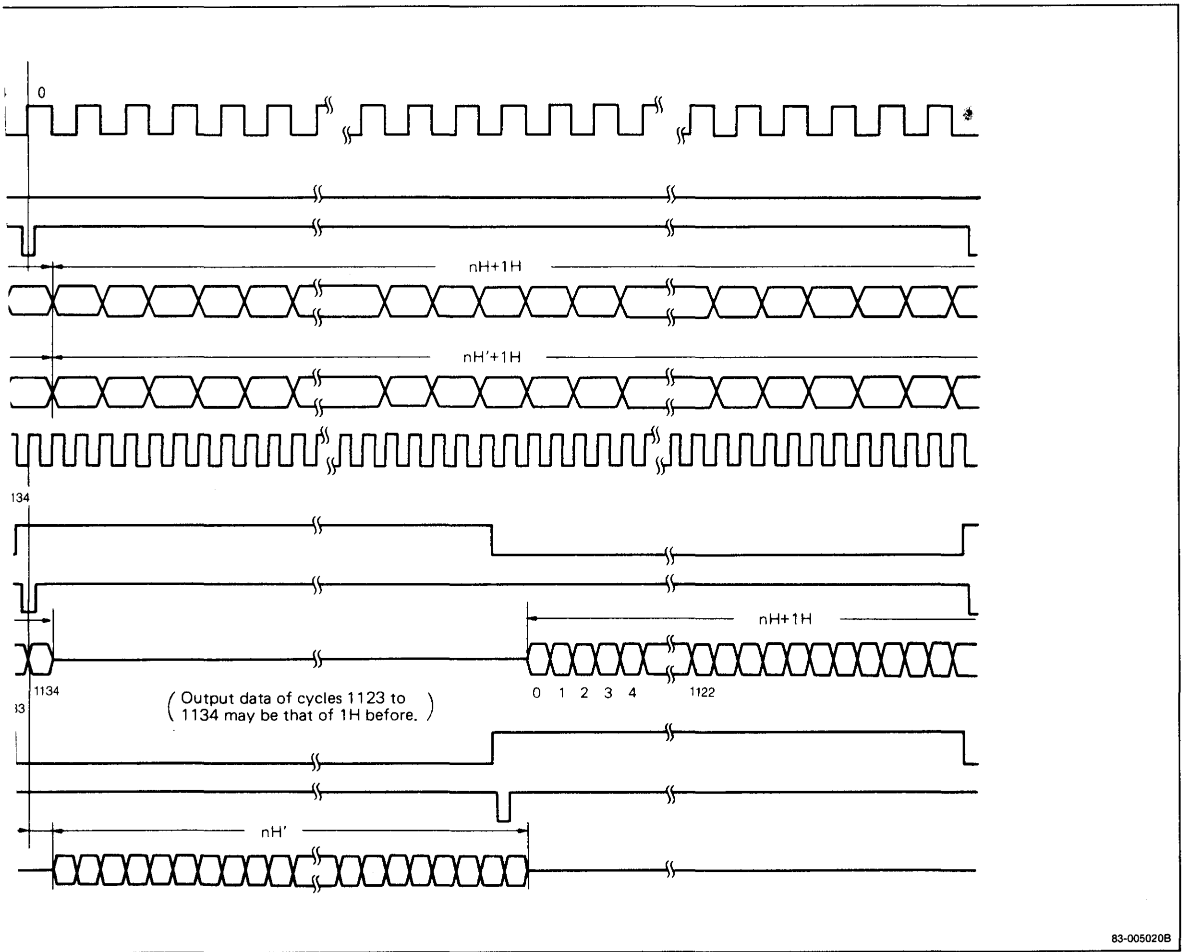
Timing Waveforms (cont)

Application Timing for Noninterlaced Scan Conversion




0
nH+1H
nH'+1H
134
nH+1H
1134
0 1 2 3 4
1122
(Output data of cycles 1123 to 1134 may be that of 1H before.)
nH'
83-005020B

3

NEC

NEC Electronics Inc.

μPD42232 TRIPLE-PORT GRAPHICS BUFFER

PRELIMINARY INFORMATION

Description

The μPD42232 is a highly integrated triple-port graphics buffer specifically designed for graphics and image processing applications. The device is configured as 32K words by 8 bits with a serial input/output port and a dual port for random access. Asynchronous operation of the serial port allows the random access port to draw graphics while data is output serially. Serial input and output ports may be configured by 8, 4, 2, or 1 bit(s).

The random access port can be used to form a matrix frame buffer with coexistent 8-bit plane and 1-bit pixel operation. In plane operation, data across the screen in one plane (x and y dimension) is accessed. In pixel operation, data in multiple planes (z dimension) is accessed. In the matrix frame buffer architecture, selection of plane or pixel access is made in a special command cycle. Furthermore, a selectable open-drain connection allows the outputs to be wire-ORed.

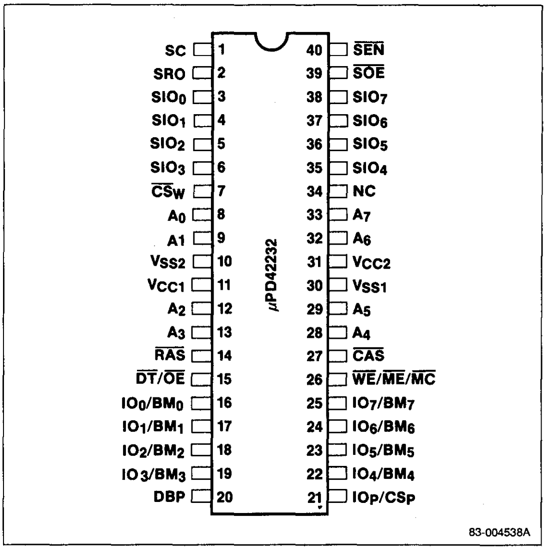
The μPD42232 supports 256 trinomial raster operations, as well as bit, chip or plane writing and reading. Refreshing is accomplished by means of $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and hidden refresh cycles. The device is packaged in a 600-mil, 40-pin plastic shrink DIP and a 400-mil, 40-pin plastic SOJ.

Features

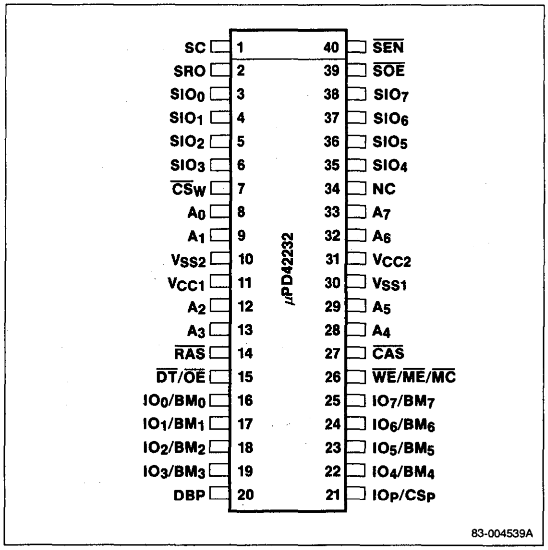
- Triple-port organization
  - — 32K x 8-bit random access port
    - 8-bit input/output port for plane access
    - 1-bit input/output port for pixel access
  - — 128 x 8-bit serial input/output port
- Ten built-in registers
  - — 256 types of raster operations
  - — Random access of bit, chip, or plane data
  - — Compare function
- Each of 8 serial data registers configured as a split buffer, allowing for relaxed data transfer timing
- Bidirectional data transfer between random access storage array and serial data registers
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and hidden refreshing
- Serial port configuration by 8, 4, 2, or 1 bit(s)
- Selectable open-drain or three-state random access outputs
- Fully TTL-compatible inputs and outputs
- Standard 40-pin plastic shrink DIP and 40-pin plastic SOJ packaging

Pin Configurations

40-Pin Plastic DIP



40-Pin Plastic SOJ



Contact your NEC sales representative for a copy of the complete data sheet.

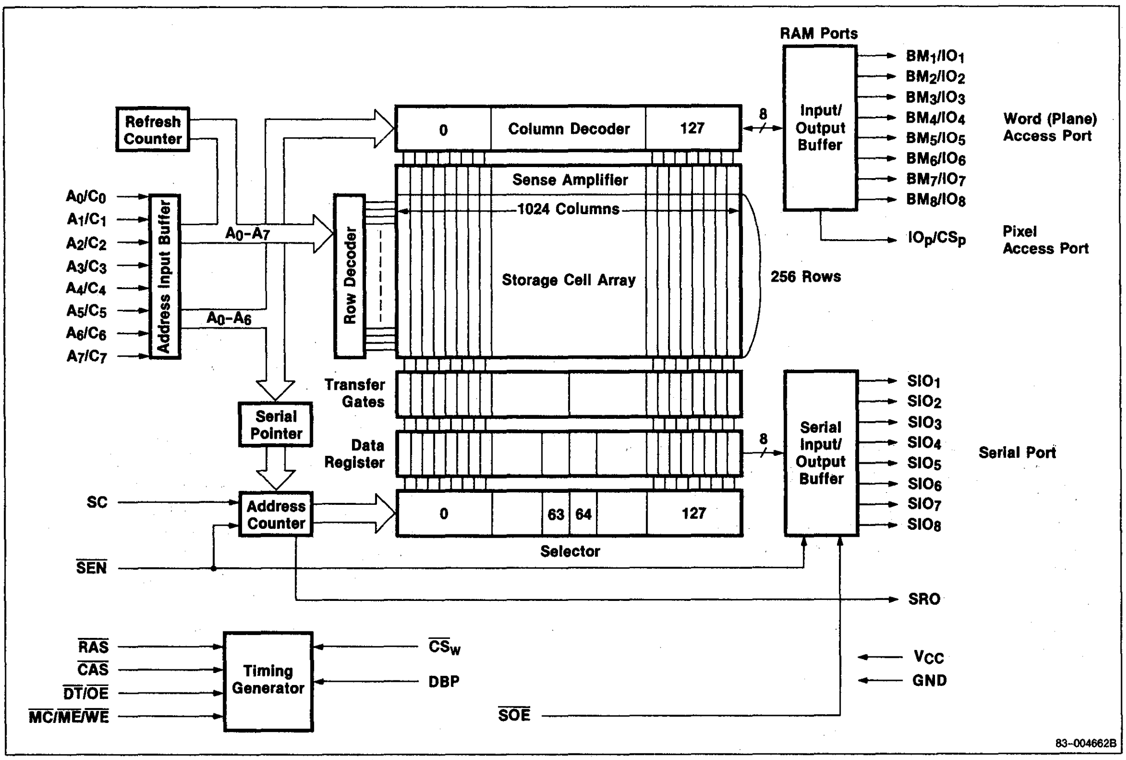
Ordering Information

Part Number	Random Write/Read Cycle Time (min)	Serial Write/Read Cycle Time (max)	$\overline{RAS}$ Access Time (max)	Package
μPD42232CU-12	220 ns	40 ns	120 ns	40-pin plastic shrink DIP
CU-15	260 ns	60 ns	150 ns	
μPD42232LA-12	220 ns	40 ns	120 ns	40-pin plastic SOJ
LA-15	260 ns	60 ns	150 ns	

Pin Identification

Symbol	Function
A_0/C_0-A_7/C_7	Address inputs/command code inputs
BM_0/IO_0-BM_7/IO_7	Bit mask inputs/plane data inputs and outputs
$\overline{CAS}$	Column address strobe
CS_P/IO_P	Chip select mask inputs/pixel data inputs and outputs
$\overline{CS_W}$	Chip select for random access port
DBP	Data bus precharge (selects open-drain output)
$\overline{DT}/\overline{OE}$	Data transfer control/output enable
$\overline{RAS}$	Row address strobe
SC	Serial clock
$\overline{SEN}$	Serial port enable
SIO_0-SIO_7	Serial data inputs and outputs
$\overline{SOE}$	Serial output enable
SRO	Serial runout output
$\overline{WE}/\overline{ME}/\overline{MC}$	Write enable/mask enable/memory command
V_{SS1}/V_{SS2}	Ground
V_{CC1}/V_{CC2}	+5-volt power supply
NC	No connection

Block Diagram



Example of Matrix Frame Buffer Architecture

The following describes the configuration for an 8-plane, 512 x 512 dot matrix frame buffer using one μPD42232 per plane and an 8-bit CPU interface bus. As can be seen in figure 1, the IO_0 through IO_7 plane access ports on each μPD42232 are connected to DB_0 through DB_7 of the CPU interface bus. Pixel access port IO_P on the first μPD42232 is connected to DB_0. IO_P on the second μPD42232 is connected to DB_1 and so on.

This configuration supports two types of operation, either of which can be selected in a special command cycle:

- Plane—where 8 bits in the same plane are accessed
- Pixel—where 8 bits of the same pixel, 8 planes deep, are accessed

In plane operation, one plane is selected by means of the chip select or plane-mask function, causing the 8 bits of data specified by IO_0 through IO_7 to be accessed. In pixel operation, one pixel (8 bits) of data from the IO_P pin of each chip is accessed using the bit-mask function to select only one of the 8 bits at the specified address.

The example shown in figure 1, where one bit from each chip (plane) in a diagonal line is accessed (IO_0 through IO_7), was chosen for the ease of explaining the pixel access function, which was developed to quickly change the color or shade of each pixel. In most applications, a single pixel at the same IO_X bit is updated. Since all eight chips are accessed simultaneously, a pixel update can be accomplished in one write cycle.

Split Buffer Configuration

A split buffer configuration is useful because it greatly relaxes the synchronization of timing between the random access and serial ports during data transfers, making it possible to design a video system where the serial port can be loaded at any time during the display or horizontal retrace period. Furthermore, the ability to perform serial register updates from the random access port during any part of the display time allows the size of the frame buffer to match CRT resolution, reducing the number of data transfers required and making more efficient use of video storage.

Item 1 of figure 2 shows the initial loading of both the lower (L) and upper (U) halves of the split buffer, which is required as part of the initialization sequence. Item 2 indicates that serial read cycles begin executing at location k and continue through location 63. The SRO serial runout pin goes high after locations 63 and 127. Items 3 and 4 show the beginning of serial reading in the right buffer (U), while the left (L) is being reloaded. Full asynchronous operation is provided by the simultaneous reading of one serial buffer while the opposite side is reloaded.

Logic Operation

The μPD42232 is equipped with a function that performs trinomial logic operation for each bit using the internal pattern and destination registers and write data input from the random access port as source data. To select this function, the raster operation code must be set by means of a special command cycle. Once set, it is retained until changed by another special command cycle. In a mask write cycle, this logic operation can be performed in 256 ways using the 8-bit raster operation code register.

The setup and execution of this logic operation takes five cycles (figure 3):

- Loading of pattern or destination register (1 cycle)
- Setting of raster operation code during memory command cycle
  - — Lower 4 bits (1 cycle)
  - — Upper 4 bits (1 cycle)
- Setting of raster operation enable function (1 cycle)
- Execution of raster operation by writing in the mask write cycle (1 cycle)

Figure 1. Pixel Access Using the Matrix Frame Buffer Architecture

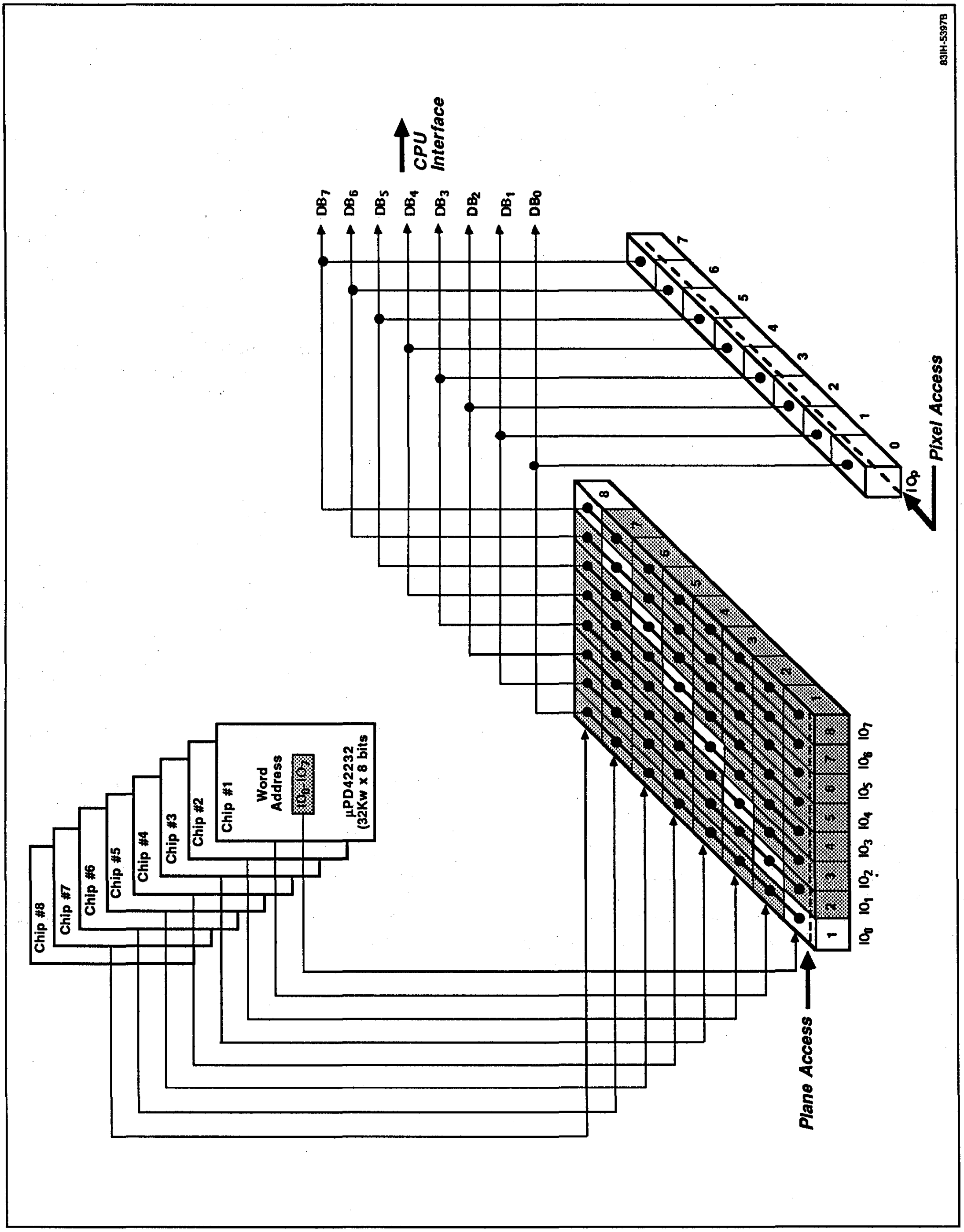


Figure 2. Serial Port Operation in Split Buffer Configuration

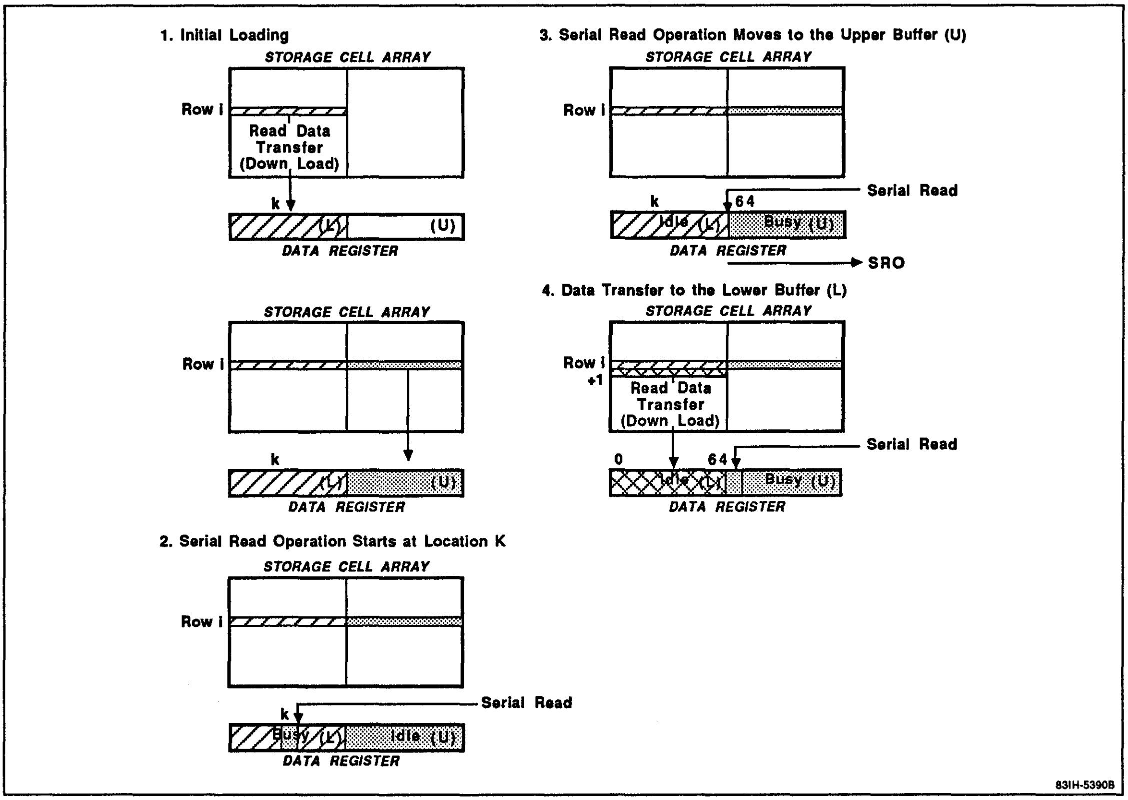
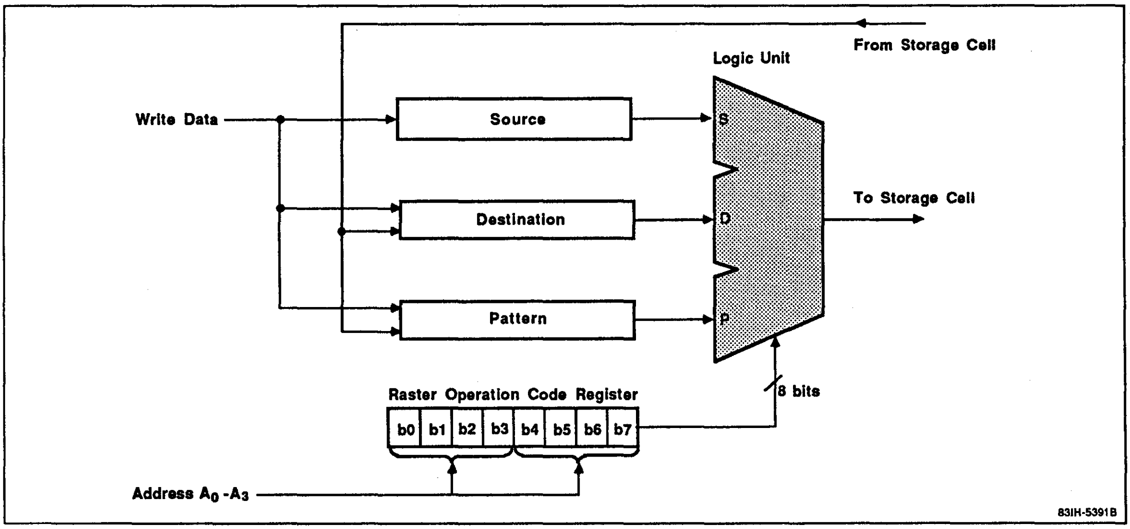


Figure 3. Logic Operation



3

NEC
NEC Electronics Inc.

μPD42270
NTSC FIELD BUFFER

PRELIMINARY INFORMATION

Description

The μPD42270 is a field buffer designed for NTSC TV applications and for other applications where serial data is needed. Equipped with four planes of 263-line by 910-bit storage, the μPD42270 can execute serial write and read cycles on any of the 263 lines. Within a line, four planes of 910 bits each may be written or read at the NTSC sampling rate of $4f_{SC}$.

Each of the four planes in the μPD42270 is equipped with two ports, one each for the write and read data registers. Each of the registers is split into two 455-bit segments, but functions as if it were organized as one scan line of 910 bits. Independent control of write and read operation makes it possible for the device to operate synchronously or asynchronously at a clock frequency of 14.3 MHz or higher.

The synchronous option simplifies interframe luminance (Y) and chrominance (C) separation and interfield noise reduction and makes it easy to obtain a one-field delay line for digital TV and VCR applications requiring NTSC $4f_{SC}$ sampling. To obtain a very long delay, field length can be configured from 260 to 263 lines and line length of the last line from 896 to 910 bits.

The asynchronous option is useful in applications such as frame synchronization and time base correction, where line jump, line hold, line reset and pointer clear functions are required to support special effects in TV field processing.

Regular refreshing of the device's dynamic storage cells is performed automatically by an internal arbitration circuit. All inputs and outputs, including clocks, are TTL-compatible. The μPD42270 is packaged in a 400-mil, 28-pin plastic DIP and is guaranteed for operation at −20 to +70°C.

Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42270C-60	40 ns	60 ns	28-pin plastic DIP

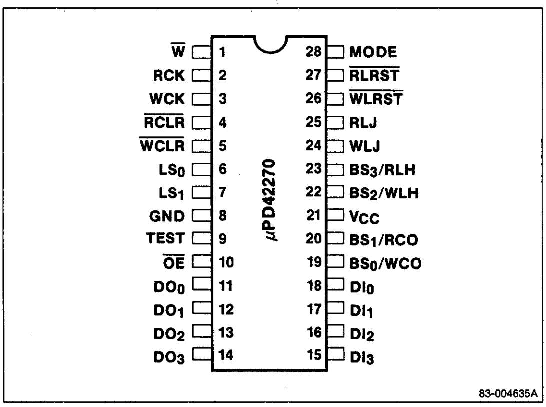
Features

- ☐ Three functional blocks
  - — Four 263-line x 910-bit storage planes
  - — 910-bit write register for each plane
  - — 910-bit read register for each plane
- ☐ Two data ports: serial write and serial read
- ☐ Asynchronous operation
  - — Dual-port accessibility
  - — Carry-out capability to indicate position of scan line
  - — Line jump, line hold, line reset, and pointer clear functions
- ☐ Synchronous operation
  - — Variable field length: 260 to 263 lines
  - — Variable last line length: 896 to 910 bits
- ☐ Automatic refreshing
- ☐ CMOS technology
- ☐ Fully TTL-compatible inputs, outputs, and clocks
- ☐ Three-state outputs
- ☐ Single +5-volt ±10% power supply
- ☐ On-chip substrate bias generator
- ☐ Standard 400-mil, 28-pin plastic DIP packaging

3

Pin Configuration

28-Pin Plastic DIP



Pin Identification

Symbol	Function
D_{IN0}-D_{IN3}	Write data inputs
D_{OUT0}-D_{OUT3}	Read data outputs
$\overline{W}$	Write enable
$\overline{OE}$	Output enable
WCK	Write clock input
RCK	Read clock input
$\overline{WCLR}$	Write pointer clear
$\overline{RCLR}$	Read pointer clear
$\overline{WLRST}$	Write line reset
$\overline{RLRST}$	Read line reset
WLJ	Write line jump
RLJ	Read line jump
WLH	Write line hold
RLH	Read line hold
WCO	Write data register carry output
RCO	Read data register carry output
LS_0-LS_1	Line select inputs
BS_0-BS_3	Bit select inputs
MODE	Mode control
GND	Ground
V_{CC}	+5-volt power supply
TEST	Test pin (connect to GND in system)

Pin Functions

D_{IN0}-D_{IN3}. These pins function as write data inputs, e.g., for $4f_{SC}$ composite color or brightness signals.

D_{OUT0}-D_{OUT3}. These pins are three-state read data outputs.

$\overline{W}$. A low level on $\overline{W}$ enables write operation. $\overline{W}$ must be kept low throughout the entire scan line to ensure that data is stored serially; if $\overline{W}$ goes high any time during the WCK clock sequencing for a line, write operation will be disabled for the half of the line (455 bits) being written. The write address pointer increments in synchronization with WCK, regardless of $\overline{W}$.

$\overline{OE}$. This signal controls read data output. When $\overline{OE}$ is low, read data is output on D_{OUT0}-D_{OUT3}. When $\overline{OE}$ is high, D_{OUT0}-D_{OUT3} are in a state of high impedance. The read address pointer is incremented by RCK, regardless of the signal level of $\overline{OE}$.

WCK. The rising edge of WCK latches write data from D_{IN0}-D_{IN3}. Each time this signal is activated, the write bit pointer increments sequentially and 4 bits of data are sampled and loaded into the write register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial write cycles are being executed in one-half of the register, the 455 addresses previously written to the other half are simultaneously transferred to storage. Writing continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the internal arbitration circuit after each block of 455 addresses has been written.

RCK. The rising edge of RCK initiates read operation. Each time this signal is activated, the bit pointer increments by 1 and serial read cycles are executed in the read register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial read cycles are being executed in one-half of the register, the 455 addresses previously read out of the other half are replaced by data from the storage array. Reading continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the arbitration circuit after each block of 455 addresses has been read. In synchronous operation, WCK controls read cycles and RCK is not used.

$\overline{\text{WCLR}}$. When $\overline{\text{WLRST}}$ is high, $\overline{\text{WCLR}}$ can be brought low to clear the write pointers to address 0 of the data register and scan line 0 of the storage array. At least one rising edge of WCK must occur while $\overline{\text{WCLR}}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{\text{WCLR}}$ goes high. If $\overline{\text{WLRST}}$ is still high, the next rising edge of WCK writes the data on D_{IN0}-D_{IN3} into address 0 of the write register.

$\overline{\text{RCLR}}$. When $\overline{\text{RLRST}}$ is high, $\overline{\text{RCLR}}$ can be brought low to clear the read pointers to address 0 of the data register and scan line 0 of the storage array (asynchronous operation only). At least one rising edge of RCK must occur while $\overline{\text{RCLR}}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{\text{RCLR}}$ goes high. If $\overline{\text{RLRST}}$ is still high, the data from address 0 is read out on D_{OUT0}-D_{OUT3} and the next rising edge of RCK initiates data access from address 1.

$\overline{\text{WLRST}}$. This pin is used in synchronous or asynchronous operation to reset the bit pointer to address 0 of the line following the one to which the signal is applied. In standard write operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{\text{WCLR}}$ is high, $\overline{\text{WLRST}}$ can be brought low for a minimum of 3 μs to force an end-of-line condition, whereby write cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with WLH, $\overline{\text{WLRST}}$ resets the current scan line; when combined with WLJ, $\overline{\text{WLRST}}$ begins writing from address 0 of the line to which the scan line pointer is jumped.

$\overline{\text{RLRST}}$. This pin is valid in asynchronous operation and can be used to reset the bit pointer to address 0 of the read line following the one to which the signal is applied. In standard read operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{\text{RCLR}}$ is high, $\overline{\text{RLRST}}$ can be brought low for a minimum of 3 μs to force an end-of-line condition, whereby read cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with RLH, $\overline{\text{RLRST}}$ resets the current scan line; when combined with RLJ, $\overline{\text{RLRST}}$ begins reading from address 0 of the line to which the scan line pointer is jumped.

WLJ. Each positive pulse of this signal increments the write scan line pointer by one line (asynchronous operation only). WLJ is sampled at the rising edge of WCK. If WLJ is high, a single jump is executed. If WLJ remains high, no further jumps occur. To jump again, WLJ must go low for at least one rising edge of WCK before going high again. It takes a minimum of two WCK cycles to complete a line jump. The first cycle senses the high level of WLJ and increments the scan line pointer. An additional WCK cycle with WLJ low is required to complete the function. If more than one line jump is needed, then the sequence must be repeated.

A line jump occurs either when the current line has been completely filled or after $\overline{\text{WLRST}}$ has reset the write address. The new scan line can be calculated by n+1+x (where "n" is the current line and "x" equals the number of positive WLJ pulses).

Changes in the level of WLJ must be made when the bit pointer is between locations 229 and 909 of the current line and when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLH is low.

RLJ. Each positive pulse of this signal increments the read scan line pointer by one line (asynchronous operation only). RLJ is sampled at the rising edge of RCK. If RLJ remains high, a single line jump is executed. To jump again, RLJ must go low for at least one rising edge of RCK before going high again. It takes a minimum of two RCK cycles to complete a line jump. The first cycle senses the high level of RLJ and increments the scan line pointer. An additional RCK cycle with RLJ low is required to complete the function. If more than one line jump is needed, then this sequence must be repeated.

A line jump occurs either when the current line has been completely read or after $\overline{\text{RLRST}}$ has reset the read address. The new scan line can be calculated by n+1+x (where "n" is the current line and "x" equals the number of positive RLJ pulses).

Changes in the level of RLJ must be made when the bit pointer is between locations 682 and 909 of the previous line, or between 0 and 452 of the current line, and when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLH is low.

WLH. Once this input is applied, the write scan line pointer will hold its position even if successive write clocks are applied. The level of WLH is sampled at the rising edge of WCK and must be applied between locations 229 and 909 of the line to be held. The held line is released after 910 addresses have been rewritten or after $\overline{\text{WLRST}}$ resets the write line address. WLH is multiplexed with BS_2 and is valid in asynchronous operation only. WLH (high) must be input only when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLJ is low.

RLH. Once this input is applied, the read scan line pointer will hold its position even if successive read clocks are applied. The level of RLH is sampled at the rising edge of RCK and must be clocked between locations 682 and 909 of the line preceding the line to hold, or between locations 0 and 452 of the line to hold. The held line is released after 910 addresses have been read or after $\overline{\text{RLRST}}$ resets the read line address. RLH (high) must be input only when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLJ is low. RLH is multiplexed with BS_3 and is valid in asynchronous operation only.

WCO. When the bit pointer reaches address 909 of the write data register, this signal goes high for one WCK cycle. WCO is multiplexed with BS_0 and is valid in asynchronous operation only.

RCO. When the bit pointer reaches address 909 of the read data register, this signal goes high for one RCK cycle. RCO is multiplexed with BS_1 and is valid in asynchronous operation only.

BS_0-BS_3. These pins input control signals to change the number of bits in the last line of the field. The combined signals of BS_0-BS_3 set the line length from 896 to 910 bits in one-bit steps (table 1). The length of the last line can change for each field, but all four pins should not be set low. BS_0, BS_1, BS_2 and BS_3 are multiplexed with WCO, RCO, WLH and RLH, respectively, and are valid in synchronous operation only. In asynchronous operation, the line length is fixed at 910 bits.

LS_0-LS_1. These pins input control signals to change the number of lines for one field in either synchronous or asynchronous operation. The combined signals of LS_0 and LS_1 set the number of lines to 260, 261, 262, or 263 (table 2). The number of lines can be changed for each field.

MODE. This pin selects the operating mode. A low signal selects synchronous operation and a high signal selects asynchronous operation. If MODE is changed after power has been applied to the μPD42270, it is necessary to clear the address pointers by bringing $\overline{\text{WCLR}}$ and $\overline{\text{RCLR}}$ low. MODE can be changed at any time; however, data input in one mode may be unreliable in the other (see table 3 for valid pin functions).

Table 1. Line Length Adjustment

BS_3	BS_2	BS_1	BS_0	Number of Bits in the Last Line
L	L	L	L	Prohibited
L	L	L	H	896
L	L	H	L	897
L	L	H	H	898
L	H	L	L	899
L	H	L	H	900
L	H	H	L	901
L	H	H	H	902
H	L	L	L	903
H	L	L	H	904
H	L	H	L	905
H	L	H	H	906
H	H	L	L	907
H	H	L	H	908
H	H	H	L	909
H	H	H	H	910

Notes:

(1) LS_0-LS_1 and BS_0-BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates the position between lines 258 and 262.

Table 2. Line Number Adjustment

LS_1	LS_0	Number of Lines
L	L	260
L	H	261
H	L	262
H	H	263

Notes:

(1) LS_0-LS_1 and BS_0-BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates a position between lines 258 and 262.

Table 3. Valid Pin Functions According to Mode

Pin Name	Synchronous Mode (Note 1)	Asynchronous Mode (Note 2)
MODE	0	1
BS_0/WCO	BS_0	WCO
BS_1/RCO	BS_1	RCO
BS_2/WLH	BS_2	WLH
BS_3/RLH	BS_3	RLH
$\overline{RCLR}$	invalid	valid
RCK	invalid	valid
$\overline{RLRST}$	invalid	valid
$\overline{WCLR}$	valid	valid
WCK	valid	valid
$\overline{WLRST}$	valid	valid
WLJ	invalid	valid
RLJ	invalid	valid

Notes:

(1) Write and read cycles are controlled by $\overline{WCLR}$, WCK, and $\overline{WLRST}$ in synchronous operation.

(2) In asynchronous operation, write and read cycles are controlled independently.

Capacitance

$T_A = -20$ to $+70$°C; $V_{CC} = 5.0$ V ±10%; GND = 0 V; f = 1 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	D_{IN0}-D_{IN3}, $\overline{W}$, $\overline{OE}$, WCK, RCK, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$, WLJ, RLJ, LS_0-LS_1, BS_2/WLH, BS_3/RLH, MODE
I/O capacitance	$C_{I/O}$			8	pF	BS_0/WCO, BS_1/RCO
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT3}

Device Operation

The μPD42270 supports two operating modes to accommodate various NTSC TV applications. Depending on the logic level of the MODE pin, the device will execute either synchronous or asynchronous write and read cycles on the addresses specified by the internal address pointers. When selecting the mode after power-on, it is necessary to reset these pointers to starting address 0 using $\overline{\text{WCLR}}$ and $\overline{\text{RCLR}}$. The level of MODE may be changed at any time.

Synchronous Mode

In synchronous mode, write and read cycles are executed simultaneously by $\overline{\text{WCLR}}$, $\overline{\text{WLRST}}$, WCK, $\overline{\text{W}}$ and $\overline{\text{OE}}$ to create a delay line, which means that write and read addresses always coincide. After all lines within a field have been written, they then are read out as the device begins overwriting new data to the same addresses again. Field length may be configured from 260 to 263 lines and last line length from 896 to 910 bits by means of the LS and BS pins, respectively. Synchronous operation is useful in applications where a very long delay line is required and may be selected by setting MODE low.

Asynchronous Mode

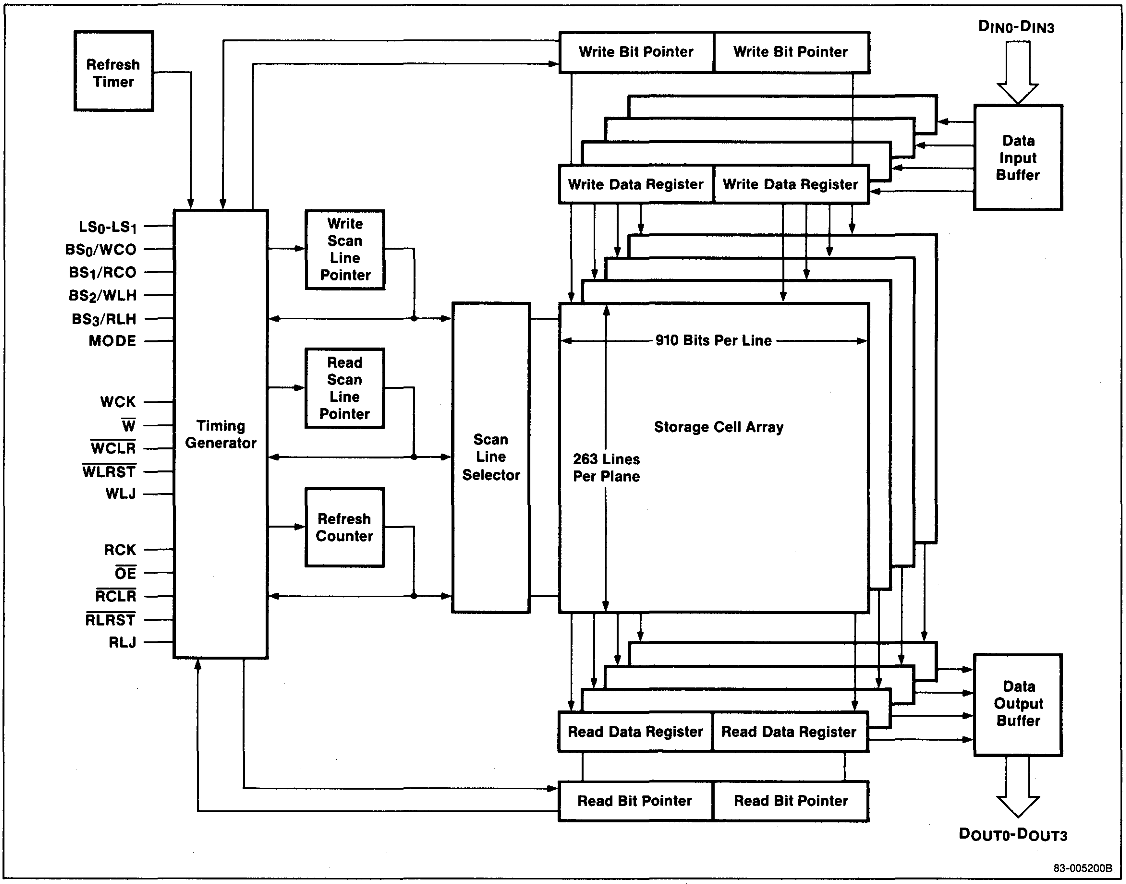
In asynchronous mode, $\overline{\text{WCLR}}$, $\overline{\text{WLRST}}$, WCK and $\overline{\text{W}}$ control write cycles, while read cycles are controlled independently by $\overline{\text{RCLR}}$, $\overline{\text{RLRST}}$, RCK and $\overline{\text{OE}}$. Field length may be configured from 260 to 263 lines using LS_0-LS_1. Line length remains fixed at 910 bits and BS_0-BS_3 are disabled to provide for the register carry out, line hold, and line jump functions. Asynchronous operation is useful for frame synchronization or time-base correction and may be selected by setting MODE high.

Address Clear. Setting $\overline{\text{WCLR}}$ and $\overline{\text{RCLR}}$ low for a minimum of 3 μs during successive WCK and RCK cycles initializes the internal pointers to starting address 0 of the first scan line ($\overline{\text{RCLR}}$ is disabled in synchronous mode). Although address clear signals must meet the specifications for setup and hold times as measured from the rising edges of WCK and RCK, they are not dependent on the status of $\overline{\text{W}}$ or $\overline{\text{OE}}$. An address clear cycle cannot occur in conjunction with $\overline{\text{WLRST}}$ or $\overline{\text{RLRST}}$ line reset cycles.

Write Operation. Write cycles are executed in synchronization with WCK as $\overline{\text{W}}$ is held low. Bits are input sequentially into one of the two halves of the data register before being transferred to the storage array. Since data is transferred into the array in blocks of 455 x 4 bits, no data transfer occurs if $\overline{\text{W}}$ goes high to disable write operation before all 455 bits are written. Despite write operation being disabled, the internal bit pointer continues to increment with each successive write clock.

Read Operation. Read cycles are executed in synchronization with RCK (asynchronous operation only) or WCK (synchronous operation only) as $\overline{\text{OE}}$ is held low. If $\overline{\text{OE}}$ goes high any time during a cycle, the outputs are in a state of high impedance until $\overline{\text{OE}}$ returns low. Since the internal bit pointer increments by 1 in spite of read operation being disabled, it is always important to reset the write and read pointers using $\overline{\text{WCLR}}$ and $\overline{\text{RCLR}}$ prior to beginning or resuming operation at the first address location in the array.

Block Diagram



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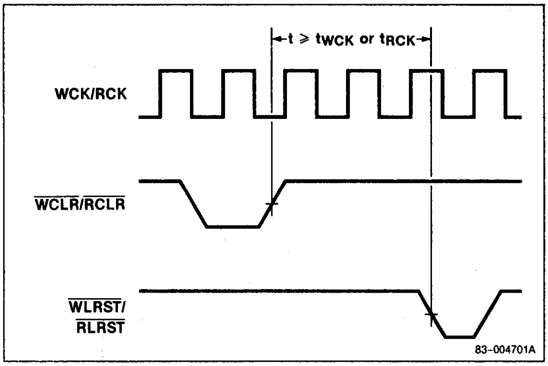
Special Functions

Line Reset. A line reset is similar to an address clear cycle, except that it only affects the bit pointers within a current line. While $\overline{\text{WCLR}}$ and $\overline{\text{RCLR}}$ are held high, $\overline{\text{WLRST}}$ or $\overline{\text{RLRST}}$ can be brought low for a minimum of 3 μs during successive WCK or RCK cycles to reset the bit pointer to address 0 of the current scan line. $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ (or $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$) must be separated by at least one serial WCK (or RCK) cycle (figure 1). After data in the first address of the current line is rewritten or reread at the rising edge of WCK or RCK, the bit pointer increments by 1 and the cycle repeats for the next address (see timing waveform for line reset cycles). In asynchronous operation, $\overline{\text{WLRST}}$ and $\overline{\text{RLRST}}$ independently reset the write and read bit pointers. During synchronous operation, $\overline{\text{WLRST}}$ resets both pointers.

Line Jump. With the line jump function, it is possible to advance the current write or read line position according to the number of positive WLJ or RLJ pulses applied (see descriptions for the WLJ and RLJ pins). In this cycle, which is valid in asynchronous mode only, the scan line pointer resets to address 0 if the number of positive pulses causes the resulting line number (n+1+x, where "n" is the current line number and "x" is the number of positive WLJ or RLJ pulses) to exceed the maximum line number (number of lines minus 1) specified by the LS_0 and LS_1 pins (table 2).

Line Hold. The line hold feature is available in asynchronous mode only and can be used to prevent the internal scan line pointers from incrementing to the next sequential address. The read and write line pointers may be held independently; however, restrictions pertaining to when this function can be initiated, detailed in the descriptions for the WLH and RLH pins, should be carefully followed.

Figure 1. Separation of Clear and Reset Signals



Absolute Maximum Ratings

Supply voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.5 to +7.0 V
Supply voltage on V_{CC} relative to GND, V_{R2}	−1.5 to +7.0 V
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

		Limits			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Ambient temperature	T_A	−20		70	°C

DC Characteristics

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA
Standby current	I_{CC1}		6	20	mA	WCK, RCK = V_{IL}
Operating current	I_{CC2}		40	80	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Access time from RCK	t_{AC}		40	ns	
Write clock cycle time	t_{WCK}	60		ns	(Note 5)
Write clock active pulse width	t_{WCW}	20		ns	
Write clock precharge time	t_{WCP}	20		ns	
Read clock cycle time	t_{RCK}	60		ns	(Note 5)
Read clock active pulse width	t_{RCW}	20		ns	
Read clock precharge time	t_{RCP}	20		ns	
Output hold time	t_{OH}	5		ns	
Output low impedance delay	t_{LZ}	5	40	ns	(Note 6)
Data output buffer high impedance delay	t_{HZ}	5	40	ns	(Note 7)
Input data setup time	t_{DS}	18		ns	
Input data hold time	t_{DH}	3		ns	
$\overline{WCLR}$ ($\overline{RCLR}$) setup time before the rising edge of WCK (RCK)	t_{CS}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) hold time after the rising edge of WCK (RCK)	t_{CH}	3		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid hold time after the rising edge of WCK (RCK)	t_{CN1}	5		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid setup time before the rising edge of WCK (RCK)	t_{CN2}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) low level valid time	t_{CLR}	3		μs	

Figure 2. Input Timing

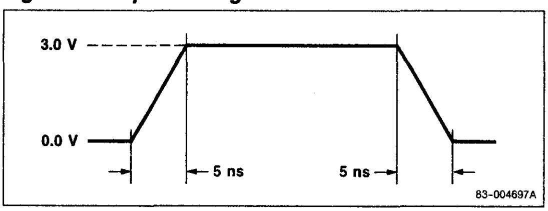
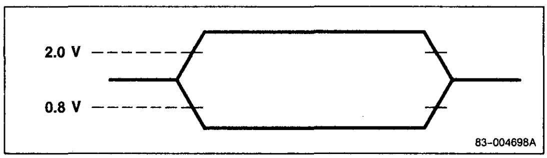


Figure 3. Output Timing



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AC Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{WLRST}$ ($\overline{RLRST}$) setup time before the rising edge of WCK (RCK)	t_{LRS}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) hold time after the rising edge of WCK (RCK)	t_{LRH}	3		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid hold time after the rising edge of WCK (RCK)	t_{LRN1}	5		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid setup time before the rising edge of WCK (RCK)	t_{LRN2}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) low level valid time	t_{LRST}	3		μs	
$\overline{W}$ setup time before the rising edge of WCK	t_{WS}	20		ns	(Note 9)
$\overline{W}$ hold time after the rising edge of WCK	t_{WH}	3		ns	(Note 9)
$\overline{W}$ valid hold time after subline (1/2) switch	t_{WN1}	5		ns	(Note 9)
$\overline{W}$ valid setup time before subline (1/2) switch	t_{WN2}	20		ns	(Note 9)
WLH (RLH) setup time before the rising edge of WCK (RCK)	t_{LHS}	20		ns	
WLH (RLH) hold time after the rising edge of WCK (RCK)	t_{LHH}	3		ns	
WLH invalid hold time measured from the end of write cycle 227	t_{WHN1}	5		ns	
WLH invalid setup time measured before write cycle 0	t_{WHN2}	20		ns	
RLH invalid hold time measured from the end of read cycle 681	t_{RHN1}	5		ns	
RLH invalid setup time measured before read cycle 453	t_{RHN2}	20		ns	
WLJ (RLJ) setup time before the rising edge of WCK (RCK)	t_{LJS}	20		ns	
WLJ (RLJ) hold time after the rising edge of WCK (RCK)	t_{LJH}	3		ns	
WLJ hold time measured from the end of write cycle 227	t_{WJN1}	5		ns	
WLJ setup time measured before write cycle 0	t_{WJN2}	20		ns	
RLJ hold time measured from the end of read cycle 681	t_{RJN1}	5		ns	
RLJ setup time measured before read cycle 453	t_{RJN2}	20		ns	

AC Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{OE}$ setup time before the rising edge of RCK (WCK)	t_{OES}	20		ns	(Note 9)
$\overline{OE}$ hold time after the rising edge of RCK (WCK)	t_{OEH}	3		ns	(Note 9)
$\overline{OE}$ valid hold time after the rising edge of RCK (WCK)	t_{OEN1}	5		ns	(Note 9)
$\overline{OE}$ valid setup time before the rising edge of RCK (WCK)	t_{OEN2}	20		ns	(Note 9)
LS, BS setup time before WCK (RCK), line 258	t_{FSS}	0		ns	
LS, BS hold time after WCK (RCK), line 0	t_{FSH}	3		μs	
Write carry output high level delay	t_{WCLH}		40	ns	
Write carry output low level delay	t_{WCHL}		40	ns	
Read carry output high level delay	t_{RCLH}		40	ns	
Read carry output low level delay	t_{RCHL}		40	ns	
Transition time	t_T	3	35	ns	(Note 4)

Notes:

(1) All voltages are referenced to GND.

(2) Ac measurements assume $t_T = 5$ ns.

(3) Input timing reference levels = 1.5 V; input levels are measured between GND and 3.0 V; output levels are measured between 0.8 and 2.0 V. See figures 2 and 3.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = -20$ to 70°C) is assured.

(6) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 5.

(7) This delay is measured at the maximum steady-state output high voltage −200 mV or the minimum steady-state output low voltage +200 mV with the load specified in figure 5.

(8) For proper execution of the pointer clear and line reset functions, specifications for t_{CS}, t_{CH}, t_{CN1}, t_{CN2}, t_{LRS}, t_{LRH}, t_{LRN1} and t_{LRN2} must be met; otherwise, these functions may not affect the desired cycles or may affect adjacent cycles erroneously.

(9) If a $\overline{W}$ (or $\overline{OE}$) pulse does not satisfy the specifications for t_{WS}, t_{WH}, t_{WN1} and t_{WN2} (or t_{OES}, t_{OEH}, t_{OEN1} and t_{OEN2}), the write disable function (output high impedance) being executed may not affect the desired cycles or may affect adjacent cycles erroneously.

(10) For the μPD42270 to read new data, read operation must be delayed from write operation by at least 920 cycles. In those cases where the delay is less than 920 cycles, read data will vary as shown below:

Source of Read Data	Delay Between Write and Read Operation
Old data	0 to 450 cycles
Indeterminate (either old or new data)	451 to 919 cycles
New data	920 or more cycles

Figure 4. Output Loading for t_{AC}, t_{OH}, t_{WCLH}, t_{WCHL}, t_{RCLH}, t_{RCHL}

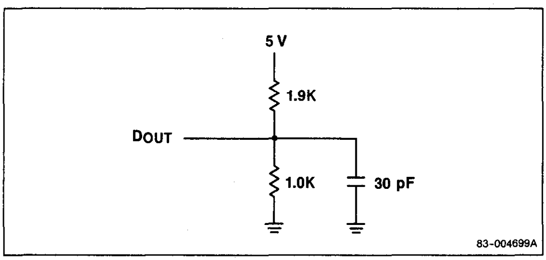
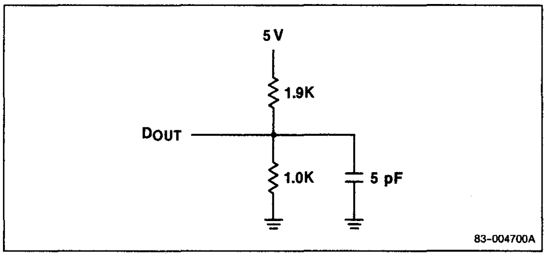
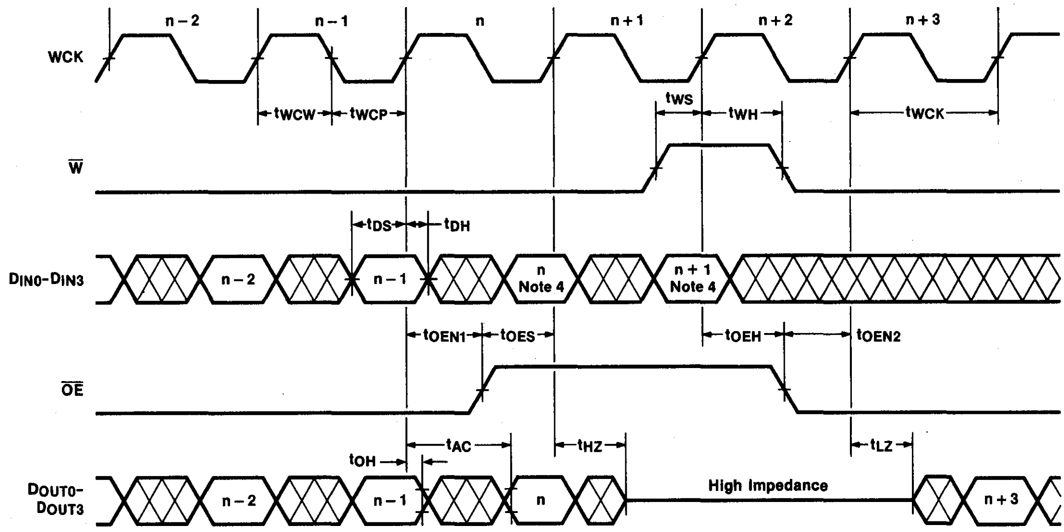


Figure 5. Output Loading for t_{LZ}, t_{HZ}



Timing Waveforms

Synchronous Write/Read Cycle



Notes:

[1] In synchronous mode, output data is delayed by one field from the input data.

[2] $\overline{WLRST} = \overline{WCLR} = V_{IH}$. MODE = V_{IL}. LS_0 and $LS_1 = V_{IH}$ or V_{IL}. $\overline{RLRST}$, $\overline{RCLR}$, and RCK are "don't care" inputs.

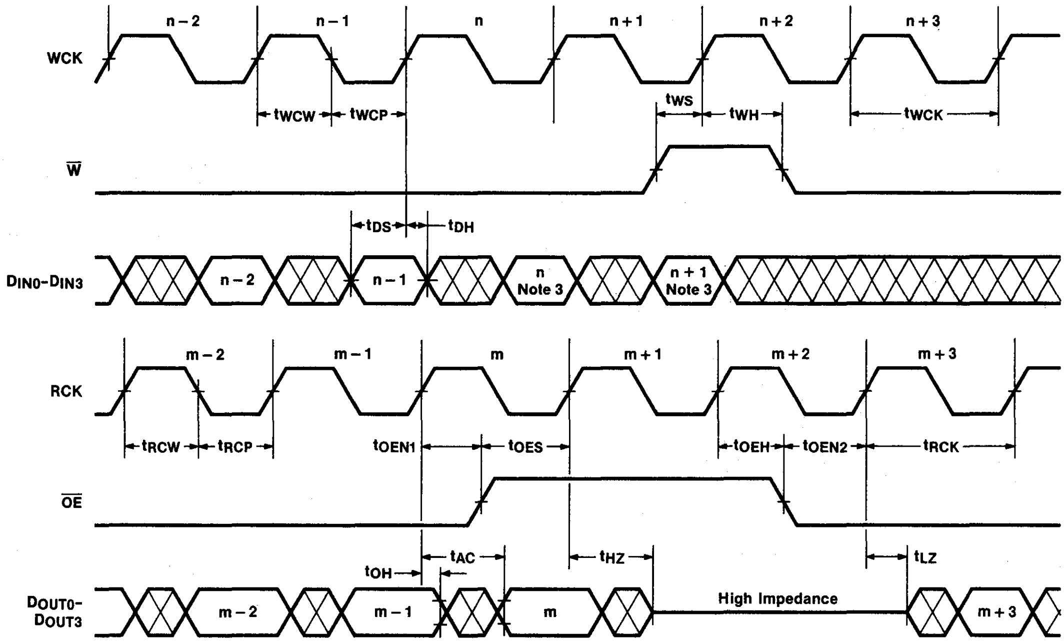
[3] BS_0-$BS_3 = V_{IH}$ or V_{IL}.

[4] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

83-004705B

Timing Waveforms (cont)

Asynchronous Write and Read Cycles



Notes:

[1] $\overline{WCLR} = \overline{RCLR} = V_{IH}$. $\overline{WLRST} = \overline{RLRST} = V_{IH}$. MODE $= V_{IH}$.

[2] RLJ, WLJ, WLH, and RLH $= V_{IH}$ or V_{IL}. LS_0 and $LS_1 = V_{IH}$ or V_{IL}.

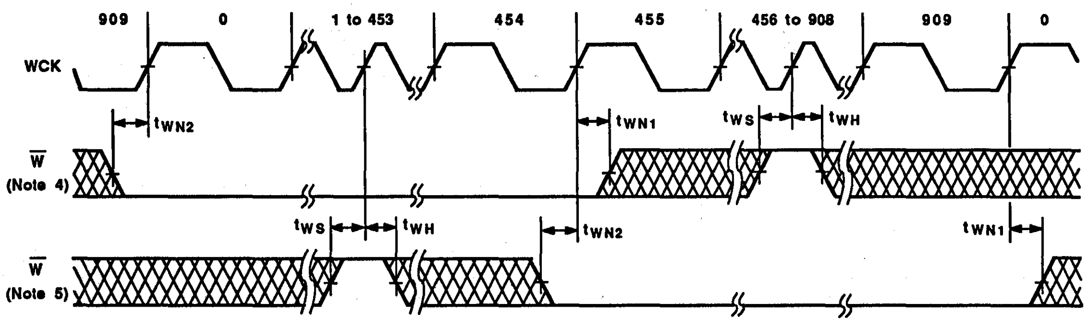
[3] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

83-004704B

3

Timing Waveforms (cont)

Write Control Timing

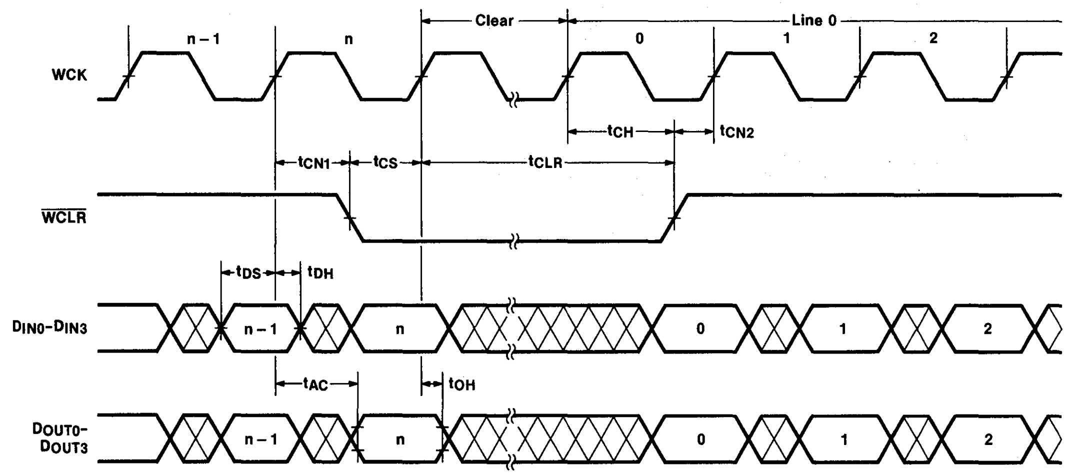


Notes:

[1] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH} .
[2] LS_0 and LS_1 = V_{IH} or V_{IL} .
[3] WLJ, RLJ, WLH, RLH, RCK, $\overline{OE}$, $\overline{RCLR}$, and MODE = "don't care".
[4] $\overline{W}$ timing for writing only to locations 0 through 454 of a scan line.
[5] $\overline{W}$ timing for writing only to locations 455 through 909 of a scan line.
[6] If $\overline{W}$ goes high, then write operation is inhibited for that half-line.

83YL-5408B

Synchronous Pointer Clear Cycle



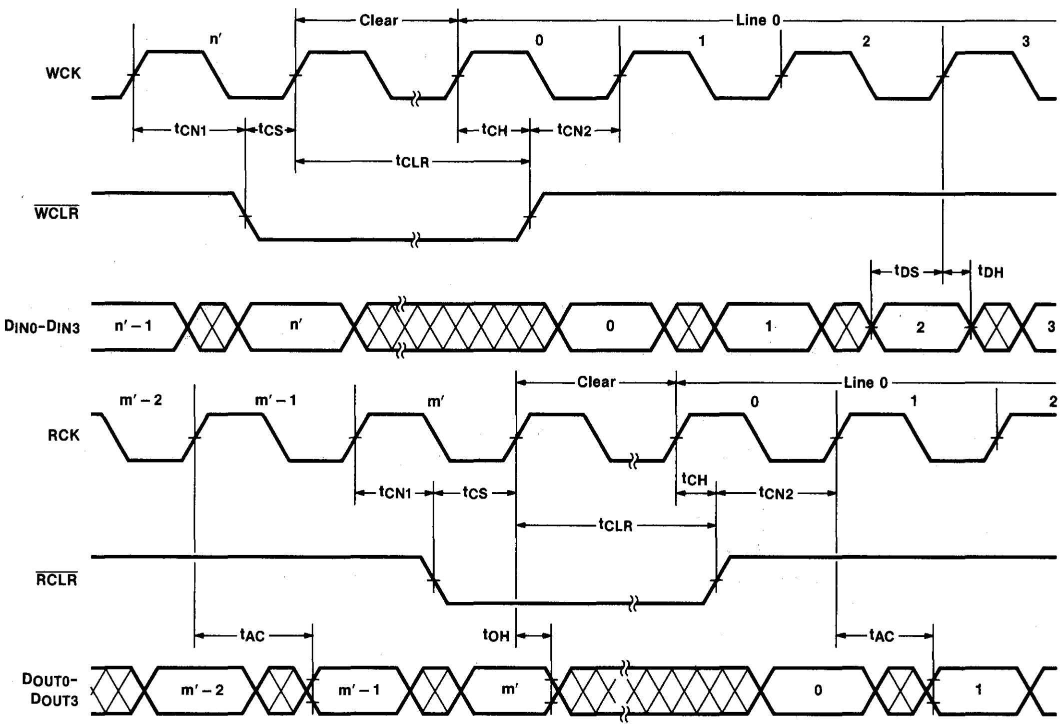
Notes:

[1] $\overline{W}$ = $\overline{OE}$ = V_{IL}. MODE = V_{IL}.
[2] LS_0 and LS_1 = V_{IH} or V_{IL}. BS_0, BS_1, BS_2, and BS_3 = V_{IH} or V_{IL}.
[3] $\overline{RLRST}$, $\overline{RCLR}$, and RCK = don't care.
[4] $\overline{WLRST}$ = V_{IH} during the clear cycle.

83-004703B

Timing Waveforms (cont)

Asynchronous Pointer Clear Cycle



Notes:

[1] $\overline{W}$ = $\overline{OE}$ = V_{IL}. MODE = V_{IH}. $\overline{WLRST}$ and $\overline{RLRST}$ = V_{IH} during clear pulse.

[2] LS_0 and LS_1 = V_{IH} or V_{IL}.

[3] WLH, RLH, WLJ, and RLJ = V_{IL} during clear pulse.

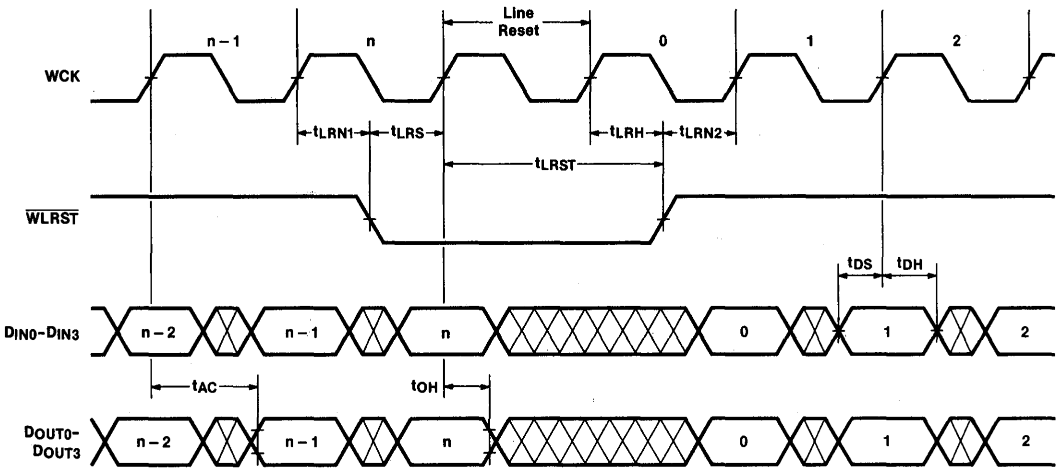
83-005021B

3

NEC

Timing Waveforms (cont)

Synchronous Line Reset Cycle

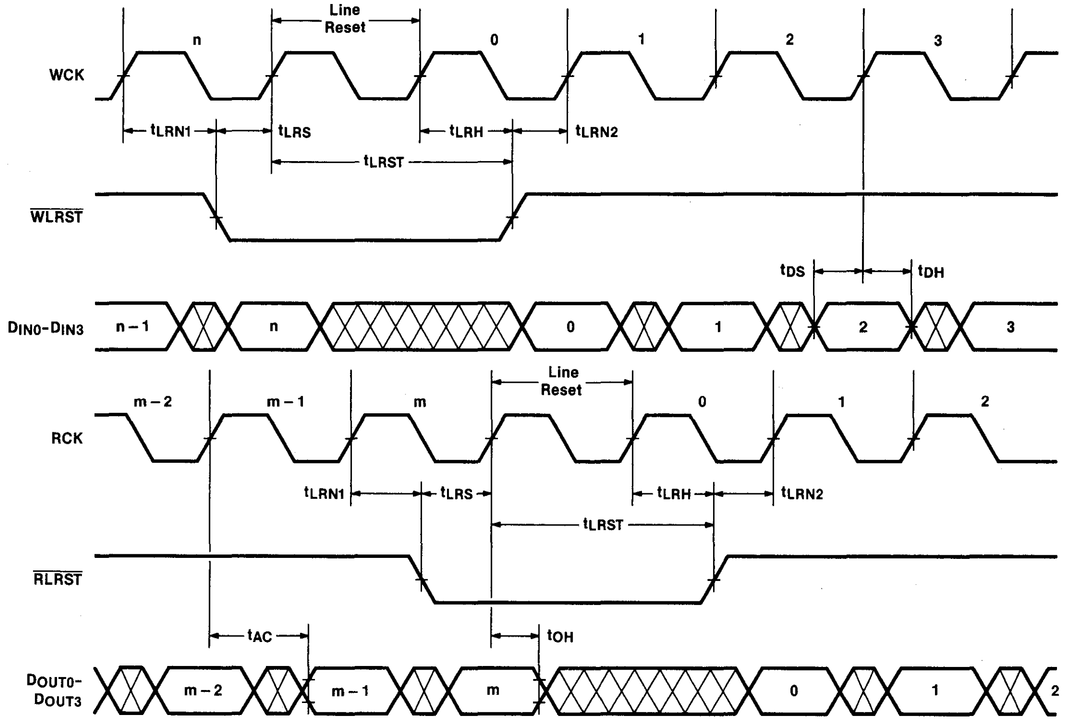


[1] $\overline{WCLR}$ = V_{IH}. $\overline{W}$, $\overline{OE}$, and MODE = V_{IL}.
[2] LS_0 and LS_1 = V_{IH} or V_{IL}. BS_0-BS_3 = V_{IH} or V_{IL}.
[3] $\overline{RCLR}$, $\overline{RLRST}$, RCK, WLJ, and RLJ = don't care.

83-004714B

Timing Waveforms (cont)

Asynchronous Line Reset Cycle



Notes:

[1] $\overline{WCLR}$, $\overline{RCLR}$ and MODE = V_{IH}. WLH, RLH, WLJ, and RLJ = V_{IL} during a reset cycle.

[2] LS_0 and LS_1 = V_{IL}.

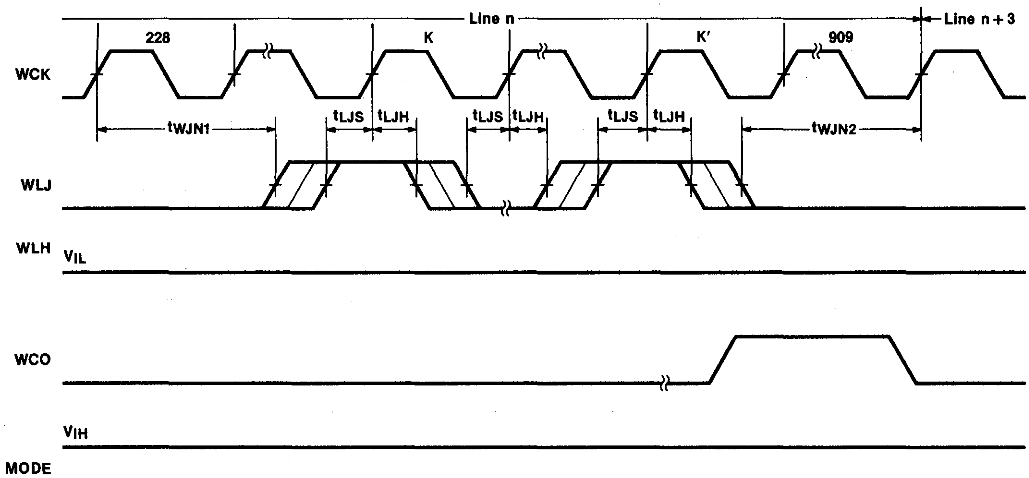
[3] $\overline{W}$ = $\overline{OE}$ = V_{IL}.

83-004713B

3

Timing Waveforms (cont)

Write Line Jump Cycle

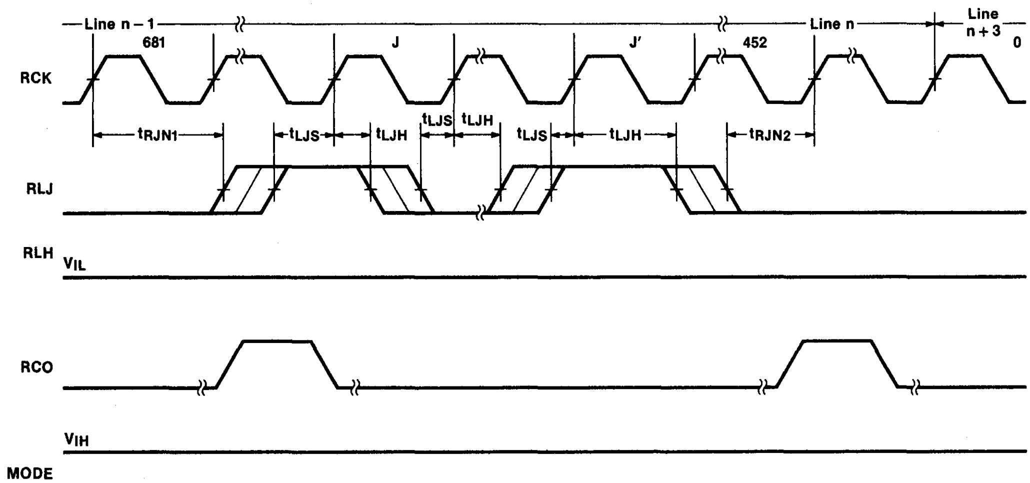


Notes:

[1] $\overline{RCLR}$, $\overline{RLRST}$, RCK, RLH, RLJ, $\overline{W}$, and $\overline{OE}$ = don't care.
[2] K and K' = 229 to 909 of line n.
[3] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.
[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

83-004711B

Read Line Jump Cycle



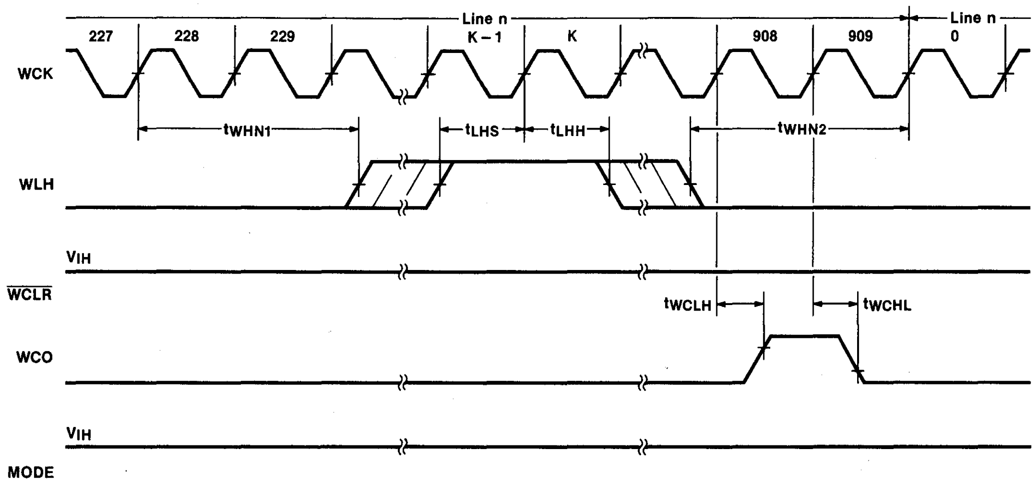
Notes:

[1] $\overline{WCLR}$, $\overline{WLRST}$, WCK, WLH, WLJ, $\overline{W}$, and $\overline{OE}$ = don't care.
[2] J and J' = 0 to 452 of line n or 682 to 909 of line n–1.
[3] $\overline{RLRST}$ and $\overline{RCLR}$ = V_{IH}.
[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

83-004712B

Timing Waveforms (cont)

Write Line Hold Cycle



Notes:

[1] $\overline{RLRST}$, RLJ, $\overline{W}$, RLH, $\overline{OE}$, $\overline{RCLR}$, and RCK = don't care.

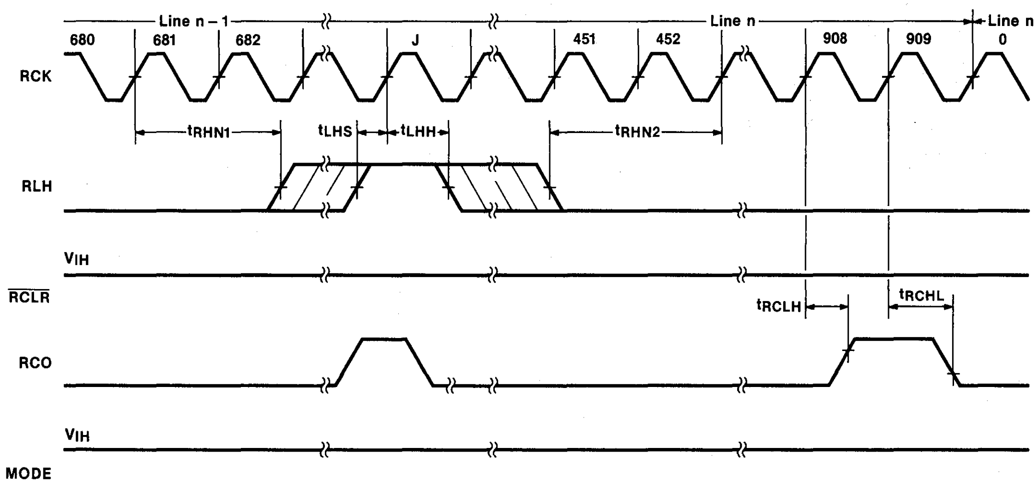
[2] K = 229 to 909.

[3] $\overline{WLRST}$ = V_{IH}. WLJ = V_{IL}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

83-004709B

Read Line Hold Cycle



Notes:

[1] $\overline{WLRST}$, WLJ, $\overline{W}$, WLH, $\overline{OE}$, $\overline{WCLR}$, and WCK = don't care.

[2] J = 682 to 909 in (n−1)th or 0 to 452 in nth line.

[3] $\overline{RLRST}$ = V_{IH}. RLJ = V_{IL}.

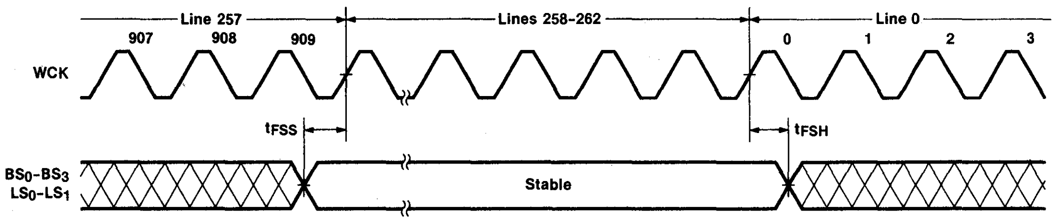
[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

83-004710B

3

Timing Waveforms (cont)

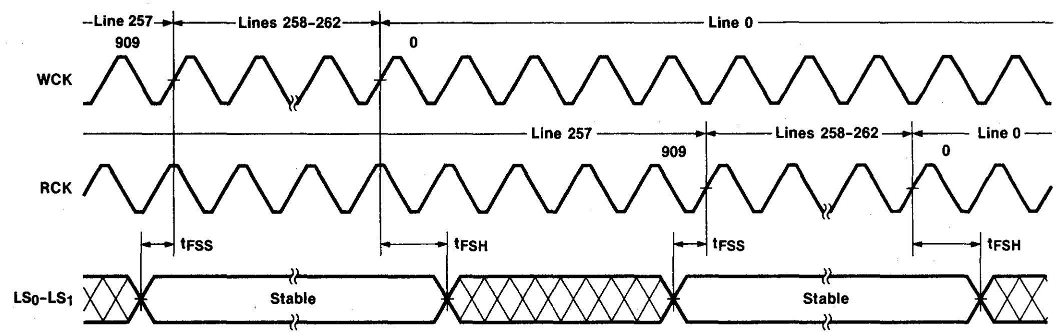
Synchronous Field Buffer Size Adjustment



Notes:
[1] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.
[2] MODE = V_{IL}.
[3] $\overline{RLRST}$, $\overline{W}$, RCK, $\overline{RCLR}$, and $\overline{OE}$ = don't care.

83-005022B

Asynchronous Field Buffer Size Adjustment

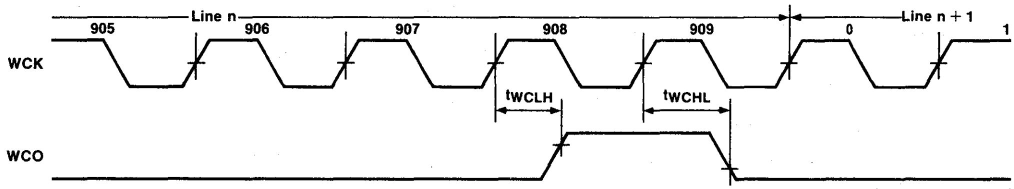


Notes:
[1] $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] MODE = V_{IH}. WLJ and RLJ = V_{IL}.
[3] $\overline{W}$, $\overline{OE}$, WLH, and RLH = don't care.

83-004707B

Timing Waveforms (cont)

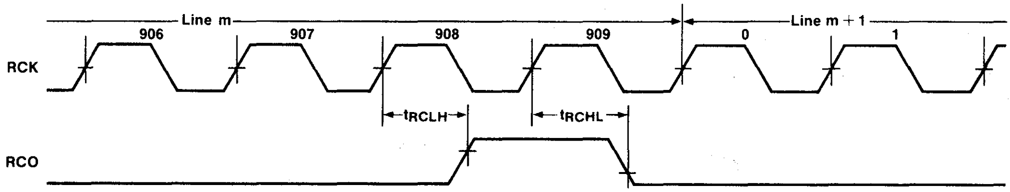
Write Register Carry Out



Notes:
[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}.
[2] LS_0 and LS_1 = V_{IH} or V_{IL}.
[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

83-005195B

Read Register Carry Out



Notes:
[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}.
[2] LS_0 and LS_1 = V_{IH} or V_{IL}.
[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

83-004708B

3

Application Examples

Delay Line

The synchronous mode may be used to create a full-field delay line with a fixed length (figures 6 and 7). Useful video applications include field interpolation, interframe noise reduction, and separation of luminance (Y) and chrominance (C) signals. In these applications, field buffer size is determined by the logic levels applied to pins LS_0-LS_1 and BS_0-BS_3. The former allows variation of the number of lines from 260 to 263, while the latter controls the actual line length at 896 to 910 bits for the last line. The actual delay between data being written into D_{IN} and read on D_{OUT} is controlled by the WCK clock period and the configured size of the buffer.

Frame Synchronization or Time Base Correction

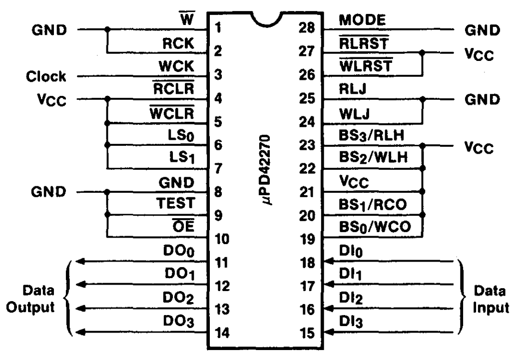
The μPD42270 has the capability of executing asynchronous write and read cycles by independently clocking WCK and RCK, respectively. The feature is useful in applications requiring frame synchronization, time base correction or buffering, where WCK, RCK, $\overline{WCLR}$ and $\overline{RCLR}$ may all have variable time periods. In addition, the write carry out (WCO) and read carry out (RCO) options give a positive indication when the bit pointer reaches the end of the line.

Vertical or Horizontal Image Compression and Expansion

Vertical compression and expansion of the video image may be accomplished by means of the line jump or line hold functions. Compression occurs when WLJ or RLJ are used to jump over lines that are not to be displayed. Expansion occurs when the WLH or RLH line hold signals are used to display a line multiple times.

Horizontal compression and expansion can be achieved by modifying the cycle time of the WCK and RCK clocks, and by using the $\overline{WLRST}$ and $\overline{RLRST}$ line reset signals.

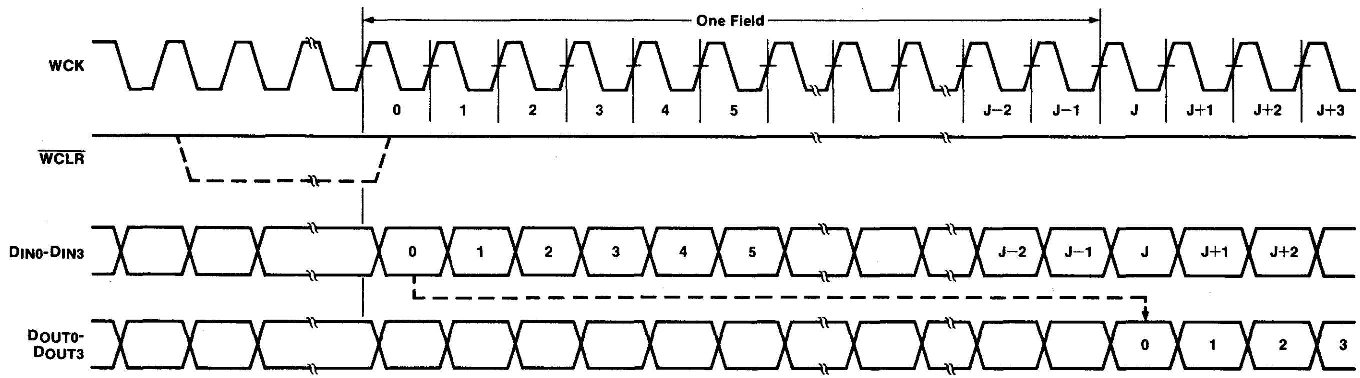
Figure 6. Example of Delay Line



Notes:
[1] $\overline{W}$, $\overline{OE}$, MODE, WLJ, and RLJ = V_{IL}.
[2] BS_0-BS_3, LS_0-LS_1, $\overline{WCLR}$, and $\overline{WLRST}$ = V_{IH}.
[3] RCK, $\overline{RCLR}$, and $\overline{RLRST}$ = don't care.

83-005301B

Figure 7. Delay Line Timing



Notes:

[1] J = 910 n+m.

[2] n = 259, 260, 261, or 262.

[3] m = 896 to 910.

[4] MODE, $\overline{W}$, and $\overline{OE}$ = V_{IL}.

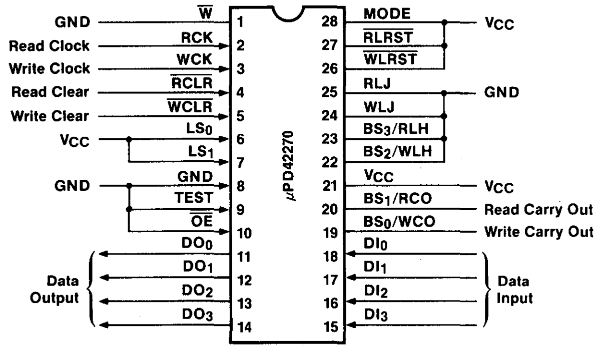
[5] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.

[6] BS_0-BS_3 and LS_0-LS_1 = V_{IH} or V_{IL}.

[7] $\overline{RLRST}$, RCK, and $\overline{RCLR}$ = don't care.

83-005302B

Figure 8. Example of Frame Synchronization/Time Base Correction



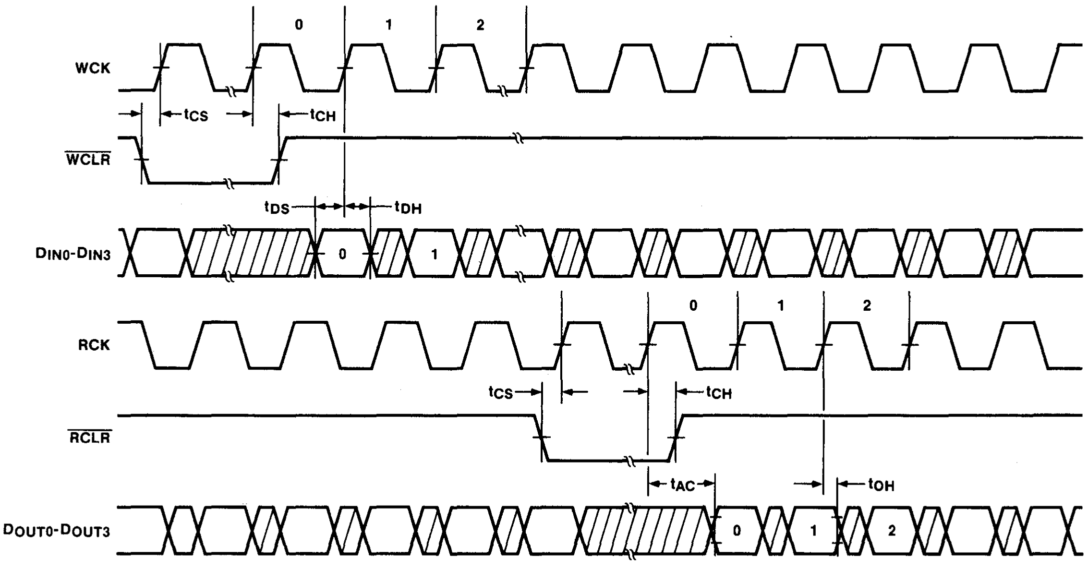
Notes:

[1] $\overline{W}$, $\overline{OE}$, WLJ, RLJ, WLH, and RLH = V_{IL}.

[2] LS_0-LS_1, MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.

83-005303B

Figure 9. Asynchronous Read/Write Timing for Frame Synchronization or Time Base Correction



Notes:
[1] MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] $\overline{W}$ and $\overline{OE}$ = V_{IL}.
[3] LS_0 and LS_1 = V_{IH} or V_{IL}.
[4] WLH, RLH, RLJ, and WLJ = V_{IL}.

83-5323B

3

NEC
NEC Electronics Inc.

μPD42273
DUAL-PORT GRAPHICS BUFFER

PRELIMINARY INFORMATION

Description

The μPD42273 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The random access port is used by the host CPU to read or write data addressed in any desired order. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit. In addition to its conventional features, the random access port also has a write-per-bit capability that allows each of the four data bits to be individually selected or masked for a write cycle.

The μPD42273 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port, however, continues to operate normally. Following the clock transition of a data transfer, the serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD42273 is fabricated with an advanced CMOS silicon-gate process using polycide technology and trench capacitors. The process provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD42273 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to +70°C.

Features

- ☐ Three functional blocks
  - — 256K x 4-bit random access storage array
  - — 2048-bit data register
  - — 512 x 4-bit serial read output circuit
- ☐ Two data ports: random access and serial read
- ☐ Dual-port accessibility except during data transfer
- ☐ Addressable start of serial read operation
- ☐ Real-time data transfer
- ☐ Single +5-volt ± 10% power supply
- ☐ On-chip substrate bias generator
- ☐ Random access port
  - — Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - — Multiplexed address inputs
  - — Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - — Refresh interval: 512 cycles/8 ms
  - — Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast page capabilities
  - — Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - — Hidden refreshing by means of $\overline{CAS}$-controlled output
  - — Write-per-bit capability regarding four I/O bits
  - — Write bit selection multiplexed on IO_0-IO_3
- ☐ $\overline{RAS}$-activated data transfer
  - — Same cycle time as for random access
  - — Row data transferred to data register as specified by row address inputs
  - — Starting location of following serial read operation specified by column address inputs
  - — Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - — Data transfer during real-time or standby operation of serial port
- ☐ Fast serial read operation by means of serial control pins
  - — Serial data presented on SO_0-SO_3
  - — Direct connection of multiple serial outputs for extension of data length
- ☐ Fully TTL-compatible inputs, outputs, and clocks
- ☐ Three-state outputs for random and serial access
- ☐ CMOS silicon-gate process with trench capacitors
- ☐ 400-mil, 28-pin plastic SOJ and 28-pin plastic ZIP packaging

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42273LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42273V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Pin Identification

Symbol	Function
A_0-A_8	Address inputs
W_0/IO_0-W_3/IO_3	Write selects in write-per-bit/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB}/\overline{WE}$	Write-per-bit/write enable
$\overline{DT}/\overline{OE}$	Data transfer/output enable
SO_0-SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

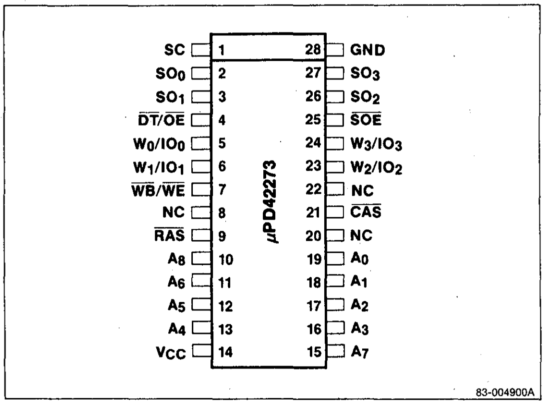
Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

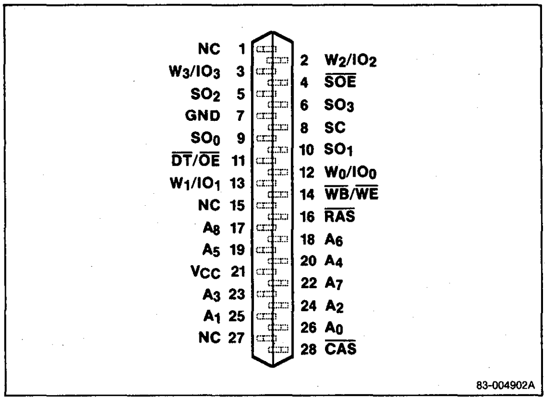
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic ZIP



Pin Functions

A_0-A_8 [Address Inputs]. These pins are multiplexed as row address inputs and column address inputs. Since each of four data bits in the random access port corresponds to 262,144 storage cells, nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are used to select one of the 512 possible rows for a read, write, data transfer, or refresh operation. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{\text{RAS}}$-only refresh cycles.)

W_0/IO_0-W_3/IO_3 [Write-Per-Bit Inputs/Common Data Inputs and Outputs]. Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{\text{RAS}}$ in a write cycle, and then updated at the next falling edge of $\overline{\text{RAS}}$.

In a read cycle, these pins function as outputs for the selected storage cells. In a write cycle, input data on these pins is latched by the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.

$\overline{\text{RAS}}$ [Row Address Strobe]. This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, and $\overline{\text{WB}}/\overline{\text{WE}}$ are simultaneously latched to determine device operation.

$\overline{\text{CAS}}$ [Column Address Strobe]. This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{\text{CAS}}$.

$\overline{\text{WB}}/\overline{\text{WE}}$ [Write-Per-Bit Control/Write Enable]. At the falling edge of $\overline{\text{RAS}}$, the input $\overline{\text{WB}}/\overline{\text{WE}}$ must be low and $\overline{\text{CAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ high to enable the write-per-bit capability. A high $\overline{\text{WB}}/\overline{\text{WE}}$ can be used at the beginning of a standard write or read cycle.

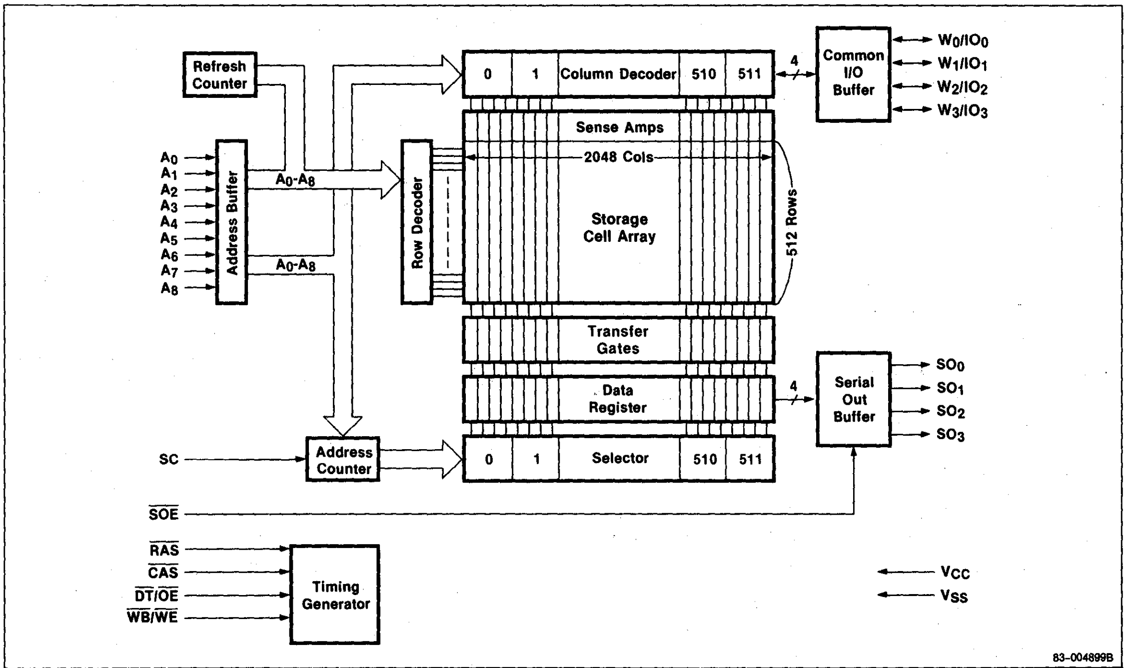
$\overline{\text{DT}}/\overline{\text{OE}}$ [Data Transfer/Output Enable]. At the falling edge of $\overline{\text{RAS}}$, a high-level $\overline{\text{CAS}}$ and a low $\overline{\text{DT}}/\overline{\text{OE}}$ initiate a data transfer, regardless of the level of $\overline{\text{WB}}/\overline{\text{WE}}$. A high $\overline{\text{DT}}/\overline{\text{OE}}$ initiates conventional read or write cycles and controls the output buffer in the random access port.

SO_0-SO_3 [Serial Data Output]. Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

SC [Serial Control]. By activating this signal repeatedly the serial read operation (starting from the location specified in the data transfer cycle) is performed within the 2,048 bits in the data register. The rising edge of SC activates the serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{\text{SOE}}$ [Serial Output Enable]. This signal controls the serial data output buffer.

Block Diagram



Device Operation

Overall Description

The μPD42273 consists of a random access port and a serial read port. The random access port performs standard read and write operation as well as the data transfer operation, all of which are based on the conventional $\overline{RAS}/\overline{CAS}$ timing cycle. In a data transfer cycle, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. The serial read port shows the contents of the data register in serial order. The random access port and the serial read port can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The graphics storage array is arranged in a 512-row by 2048-column matrix. Each of 4 data bits in the random access port corresponds to 262,144 storage cells. Therefore, 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In the data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle.

In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. By activating SC repeatedly, the serial read operation (starting from the location specified in the data transfer cycle) is executed within the 2048 bits in the data register.

Random Access Port Operation

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multiplexed in the random access port.

- $\overline{DT}/\overline{OE}$
- $\overline{WB}/\overline{WE}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{OE}$, $\overline{WE}$ and IO_i functions represent standard operations. The $\overline{DT}$, $\overline{WB}$, and W_i functions are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{RAS}$. The $\overline{DT}$ level determines whether a cycle is a random access operation or a data transfer operation. $\overline{WB}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{DT}(/\overline{OE})$, for example, depending on the function being described.

To use the μPD42273 for random access, $\overline{DT}(/\overline{OE})$ must be high as $\overline{RAS}$ falls. Holding $\overline{DT}(/\overline{OE})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{DT}(/\overline{OE})$ must be low as $\overline{RAS}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and maintaining a high $(\overline{WB}/)\overline{WE}$ during an active $\overline{CAS}$. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in a state of high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$ to $\overline{CAS}$, $\overline{RAS}$ to column address, and $\overline{RAS}$ to $\overline{OE}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. A high $\overline{CAS}$ or $\overline{OE}$ returns the output to high impedance.

Truth Table (Random Access Port)

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Function
↓	H	H	H	Read/write
↓	H	H	L	Write-per-bit
↓	H	L	X	Data transfer
↓	L	X	X	$\overline{CAS}$ before $\overline{RAS}$ refresh

Notes:

(1) X = "don't care"

Write Cycle. A write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or $(\overline{WB}/)\overline{WE}$ strobes the data on $(W_i/)IO_i$ into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}(/\overline{WE})$ must be low as $\overline{RAS}$ falls. In this case, data bits to which the write operation is applied can be specified by keeping $W_i(/IO_i)$ high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of $W_i(/IO_i)$ that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}(/\overline{WE})$ is high as $\overline{RAS}$ falls, the write-per-bit capability is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing $(\overline{WB}/)\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in a state of high impedance for the entire cycle. As $\overline{RAS}$ falls, $(\overline{DT}/)\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$; but otherwise $(\overline{DT}/)\overline{OE}$ does not affect any circuit operation during an active $\overline{CAS}$.

Read-Write/Read-Modify-Write [RW/RMW] Cycle. An RW/RMW cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i is returned to a high-impedance condition by a high ($\overline{DT}$/)$\overline{OE}$. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any operation performed in the random access port (i.e., read, write, refresh, or data transfer) refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

$\overline{RAS}$-only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all of the storage cells in one row of the graphics storage array. A high $\overline{CAS}$ is maintained during an active $\overline{RAS}$ to keep (W_i/)IO_i in a state of high impedance. This mode is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically performs refreshing for row addresses specified by the internal refresh address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows effectively faster data access by keeping the same row address and strobing successive column addresses onto the chip. By maintaining a low $\overline{RAS}$ while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. During this operation, read, write and RW/RMW cycles are possible. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following fast-page write cycle.

During a fast-page read cycle, the (W_i/)IO_i data pin (i = 0, 1, 2, or 3) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

- t_{ACP}, when $t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
- t_{AA}, when $t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max) or when $t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
- t_{CAC}, when $t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}$(/$\overline{OE}$) low as $\overline{RAS}$ falls. As described previously, the specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}$(/$\overline{OE}$) must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates: column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Serial Read Port Operation

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows the data transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}$(/$\overline{OE}$) must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from a high SC, only when a low $\overline{SOE}$ is maintained. The SC cycle which includes the positive transition of $\overline{DT}$(/$\overline{OE}$) shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42273 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

Recommended DC Operating Conditions

$T_A = 0$ to $+70°C$; GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	$V_{IN} = 0$ to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; $V_{OUT} = 0$ to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)} = -2$ mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)} = 4.2$ mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)} = -1$ mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)} = 2.1$ mA

Power Supply Current Definitions

Port	Operation	Symbol	Operating Conditions
Random Access	Read/write	RW	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min)
	Standby	STB	$\overline{CAS} = \overline{RAS} = V_{IH}$
	$\overline{RAS}$-only refresh	ROR	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ (min)
	Fast page	PAGE	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min)
	$\overline{CAS}$ before $\overline{RAS}$ refresh	CBR	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
	Data transfer	DTR	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
Serial Read	Standby	STB	$\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
	Serial read	ACT	$\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ (min)

Power Supply Current

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; GND = 0 V

Port Random Access	Port Serial Read	Symbol	Limits μPD42273 -10 Max	Limits μPD42273 -12 Max	Unit	Test Conditions (Note 1)
RW	STB	I_{CC1}	70	60	mA	
STB	STB	I_{CC2}	3	3	mA	
ROR	STB	I_{CC3}	70	60	mA	(Note 2)
PAGE	STB	I_{CC4}	60	50	mA	(Note 3)
CBR	STB	I_{CC5}	70	60	mA	
DTR	STB	I_{CC6}	70	60	mA	
RW	ACT	I_{CC7}	100	90	mA	
STB	ACT	I_{CC8}	35	30	mA	
ROR	ACT	I_{CC9}	100	90	mA	(Note 2)
PAGE	ACT	I_{CC10}	85	75	mA	(Note 3)
CBR	ACT	I_{CC11}	100	90	mA	
DTR	ACT	I_{CC12}	100	90	mA	

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, and I_{CC6}, real values depend on output loading and cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high or low level. The column addresses are also assumed to be kept at a stable high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

Capacitance

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 to A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 to W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 to SO_3

3

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Switching Characteristics							
Access time from $\overline{RAS}$	t_{RAC}		100		120	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{CAS}$	t_{CAC}		25		30	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		55		65	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{CAS}$	t_{ACP}		55		65	ns	(Notes 3 and 15)
Access time from $\overline{OE}$	t_{OEA}		25		30	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		30		40	ns	(Note 3)
Serial output access time from $\overline{SOE}$	t_{SOA}		25		30	ns	(Note 3)
Output disable time from $\overline{CAS}$ high	t_{OFF}	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{OE}$ high	t_{OEZ}	0	25	0	30	ns	(Note 5)
Serial output disable time from $\overline{SOE}$ high	t_{SOZ}	0	15	0	20	ns	(Note 5)
$\overline{SOE}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	5		10		ns	
Timing Requirements							
Random read or write cycle time	t_{RC}	190		220		ns	(Note 11)
Read-write/ read-modify-write cycle	t_{RWC}	255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	60		70		ns	(Note 11)
Fast-page read-write/ read-modify write cycle time	t_{PRWC}	125		145		ns	(Note 11)

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Notes 3, 10 and 18)
$\overline{RAS}$ precharge time	t_{RP}	80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25		30		ns	
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	25	15	30	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}	25	75	25	90	ns	(Note 4)
$\overline{CAS}$ high to $\overline{RAS}$ low precharge time	t_{CRP}	10		10		ns	(Note 16)
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	12		15		ns	
Column address setup time	t_{ASC}	0	25	0	30	ns	(Note 15)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	ns	(Notes 9 and 14)
Column address to $\overline{RAS}$ lead time	t_{RAL}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns	(Note 6)
Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns	(Note 6)

AC Characteristics (cont)

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Write command hold time	t_{WCH}	20		30		ns	
Write command pulse width	t_{WP}	20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 8)
Data-in hold time	t_{DH}	20		25		ns	(Note 8)
Column address to $\overline{WE}$ delay	t_{AWD}	85		100		ns	(Note 7)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55		65		ns	(Note 7)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		ns	(Note 7)
$\overline{OE}$ high to data-in setup delay	t_{OED}	30		35		ns	
$\overline{OE}$ high hold time after $\overline{WE}$ low	t_{OEH}	25		30		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh setup time	t_{CSR}	0		0		ns	
$\overline{CAS}$ before $\overline{RAS}$ refresh hold time	t_{CHR}	15		20		ns	
$\overline{RAS}$ high to $\overline{CAS}$ low precharge time	t_{RPC}	0		0		ns	
Refresh time interval	t_{REF}		8		8	ms	Addresses A_0-A_8
$\overline{DT}$ low setup time	t_{DLS}	0		0		ns	
$\overline{DT}$ low hold time after $\overline{RAS}$ low	t_{RDH}	90		120		ns	

Parameter	Symbol	μPD42273-10 Min	μPD42273-10 Max	μPD42273-12 Min	μPD42273-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
$\overline{DT}$ low hold time after $\overline{CAS}$ low	t_{CDH}	30		35		ns	
SC high to $\overline{DT}$ high delay	t_{SDD}	10		15		ns	
SC low hold time after $\overline{DT}$ high	t_{SDH}	10		15		ns	
Serial clock cycle time	t_{SCC}	30		40		ns	(Note 11)
SC pulse width	t_{SCH}	10		15		ns	
SC precharge time	t_{SCL}	10		15		ns	
$\overline{DT}$ high setup time	t_{DHS}	0		0		ns	
$\overline{DT}$ high hold time	t_{DHH}	15		20		ns	
$\overline{DT}$ high to $\overline{RAS}$ high delay	t_{DTR}	10		10		ns	
$\overline{DT}$ high to $\overline{CAS}$ high delay	t_{DTC}	5		5		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write-per-bit hold time	t_{WBH}	15		20		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	15		20		ns	
$\overline{SOE}$ pulse width	t_{SOE}	10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	10		15		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15		20		ns	

Notes:

(1) All voltages are referenced to GND.

Notes [cont]:

(2) An initial pause of 100 μs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved. Also, $\overline{SOE}$ must be held high or SC must be held low until completion of the first data transfer cycle.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of ($\overline{WB}$/) $\overline{WE}$ in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Ac measurements assume t_T = 5 ns.

Figure 1. Input Timing

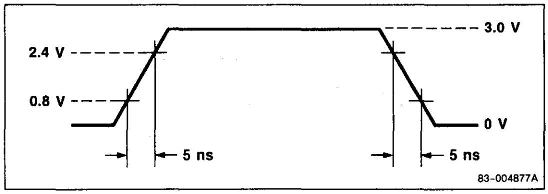


Figure 2. Output Timing

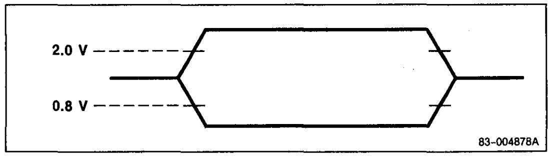


Figure 3. Random Access Port: Output Loading

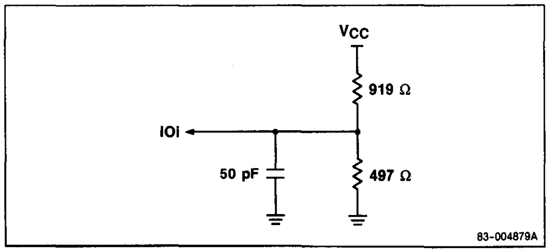
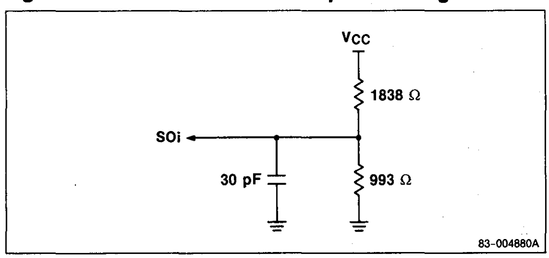
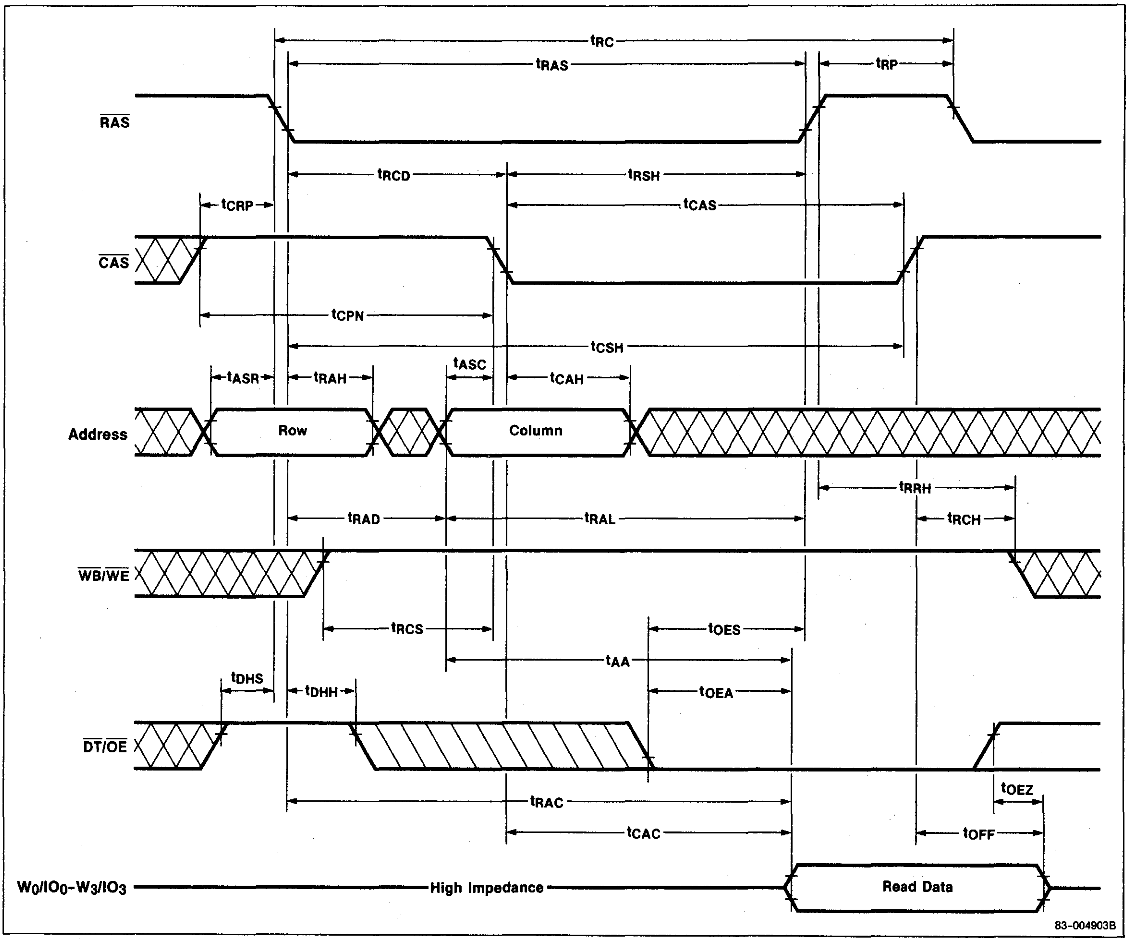


Figure 4. Serial Read Port: Output Loading



Timing Waveforms

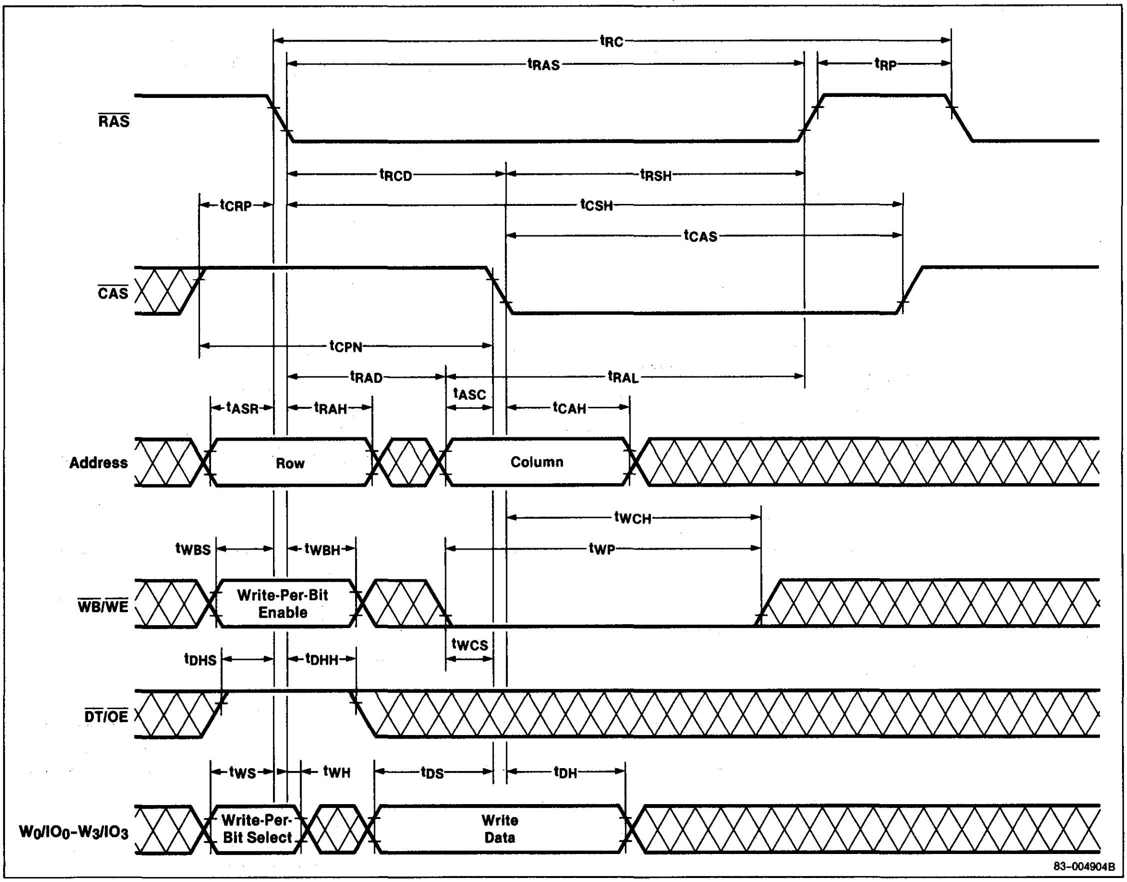
Read Cycle



3

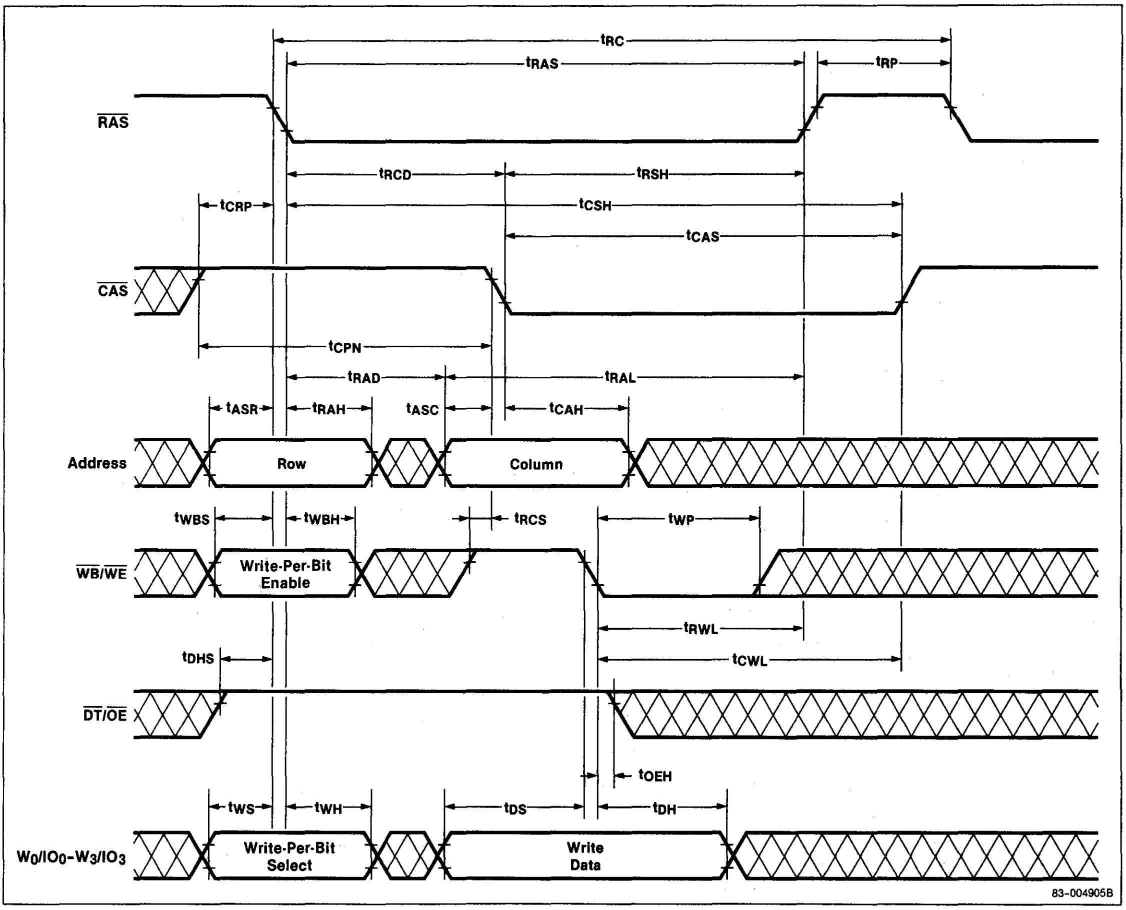
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

Late Write Cycle



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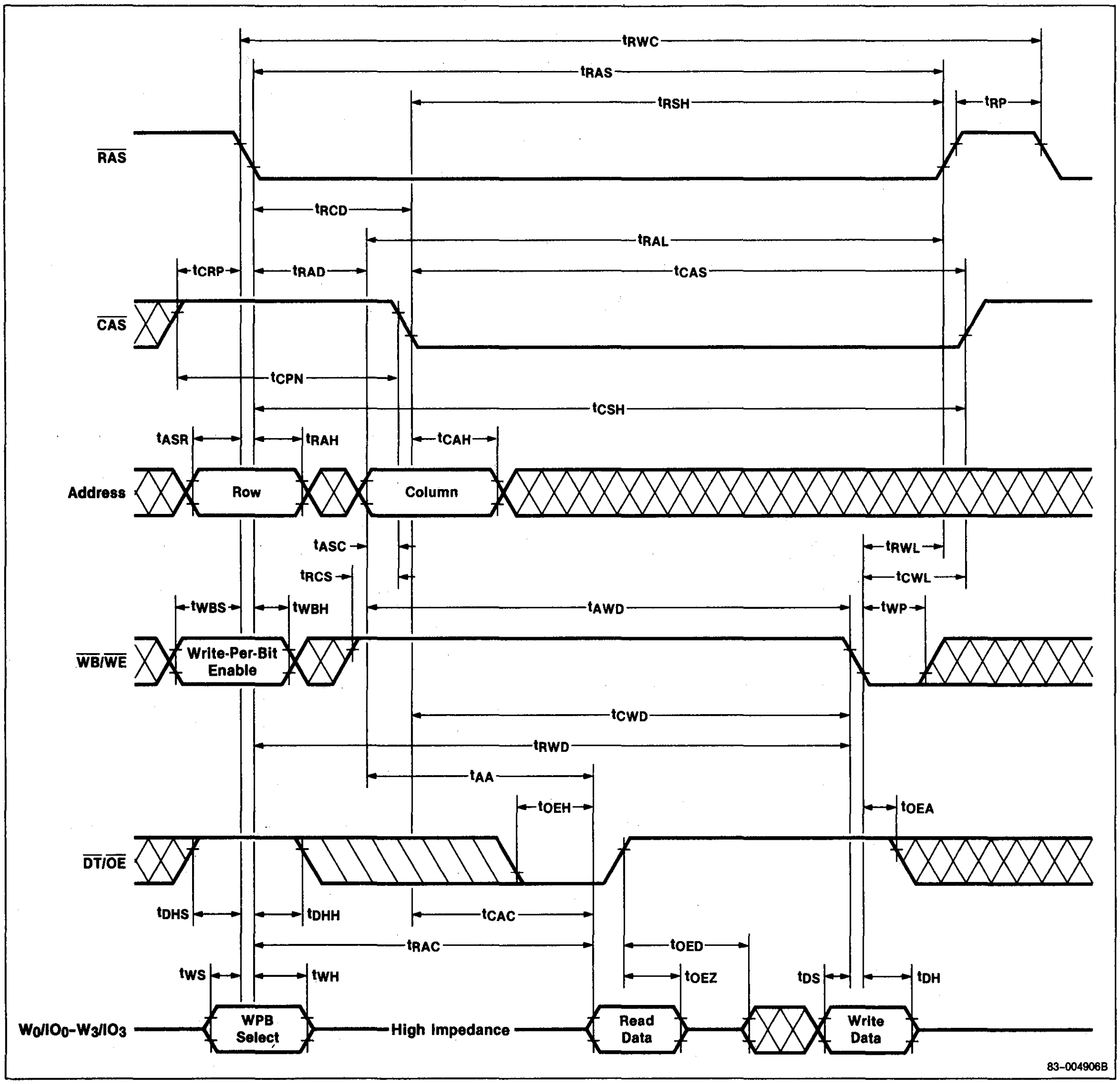
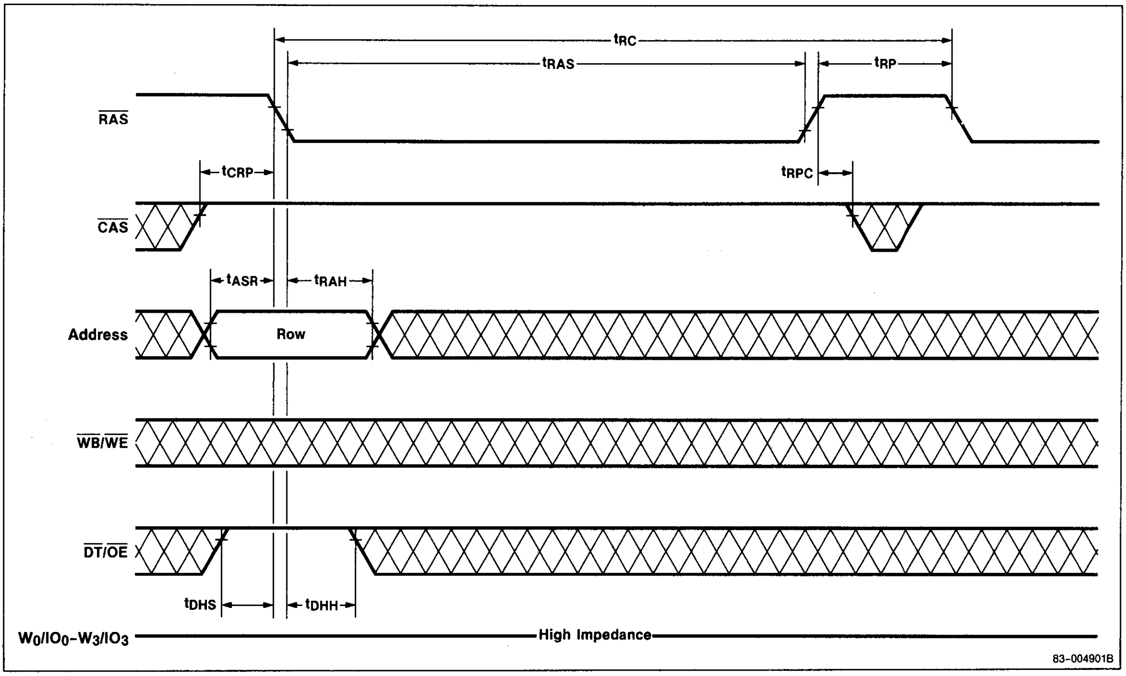
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycles



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh



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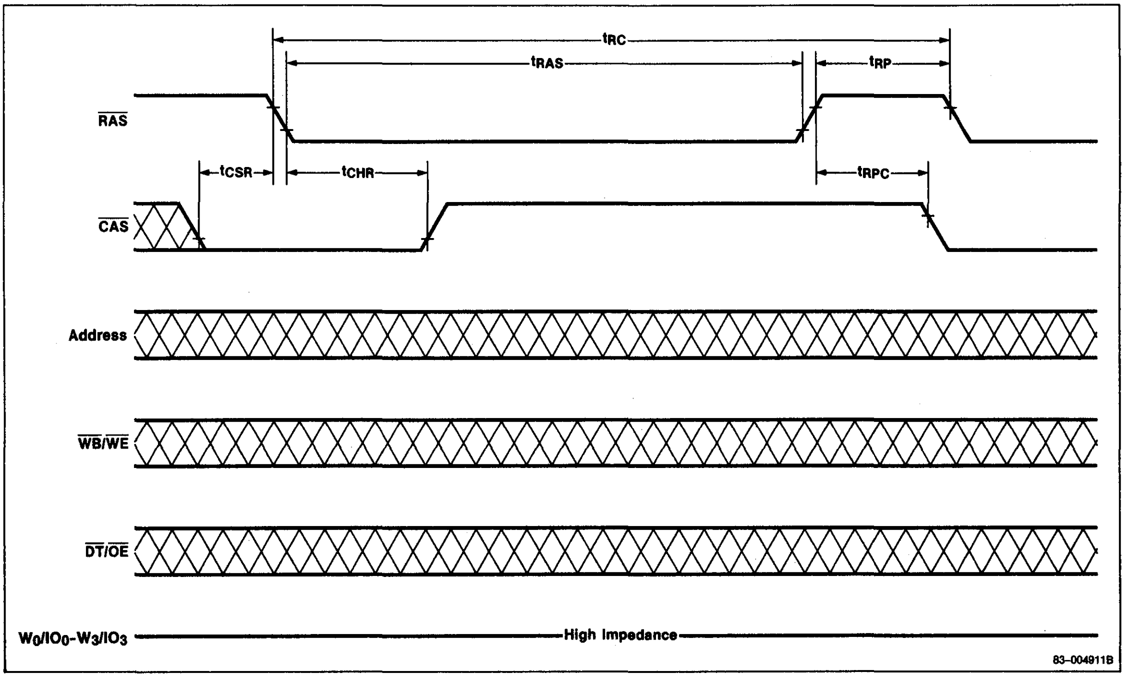
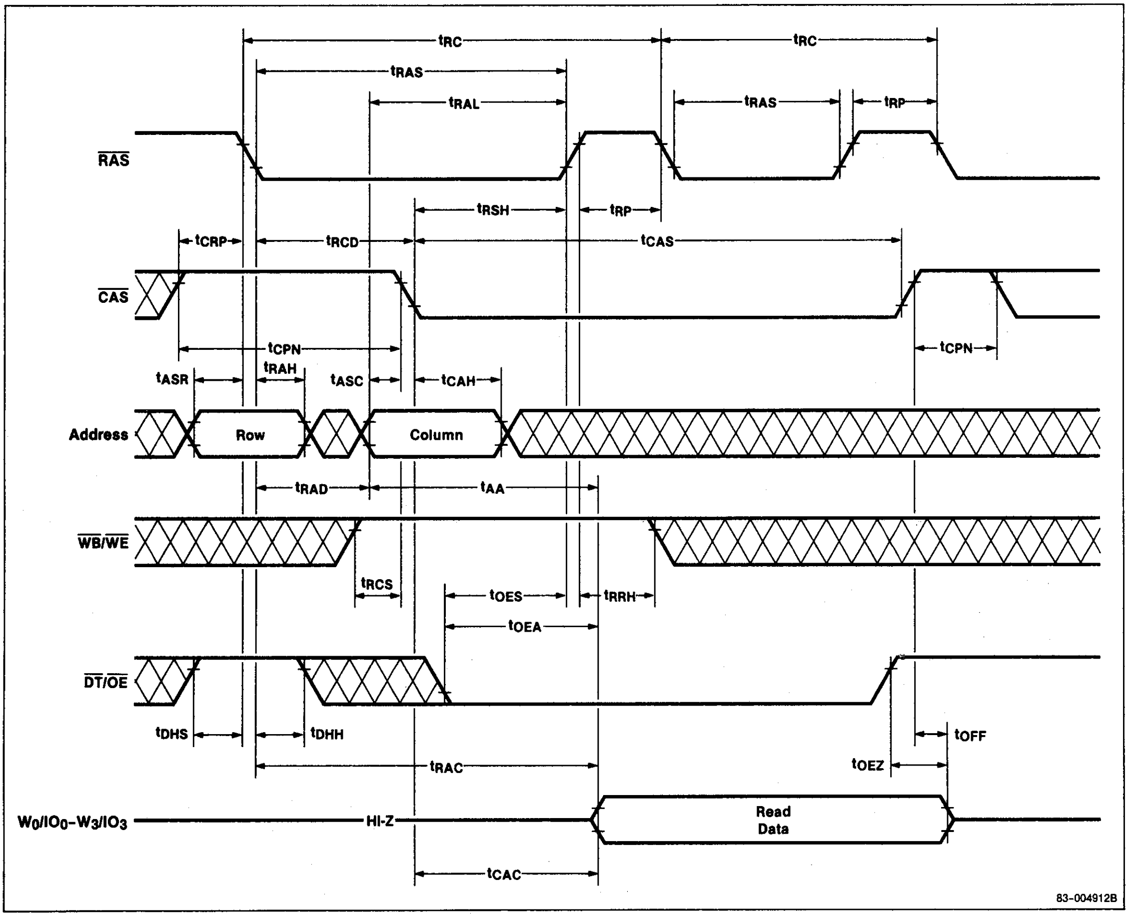
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh



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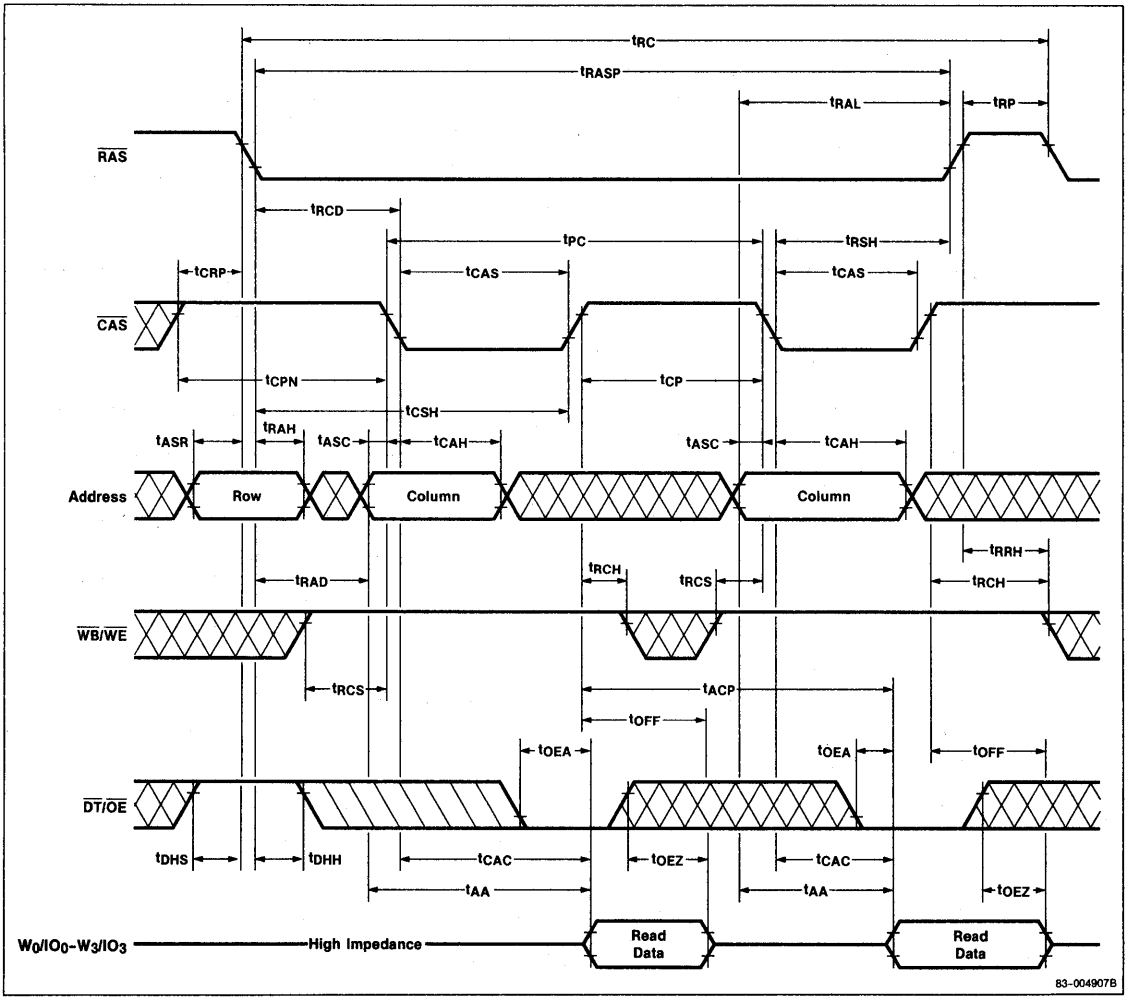
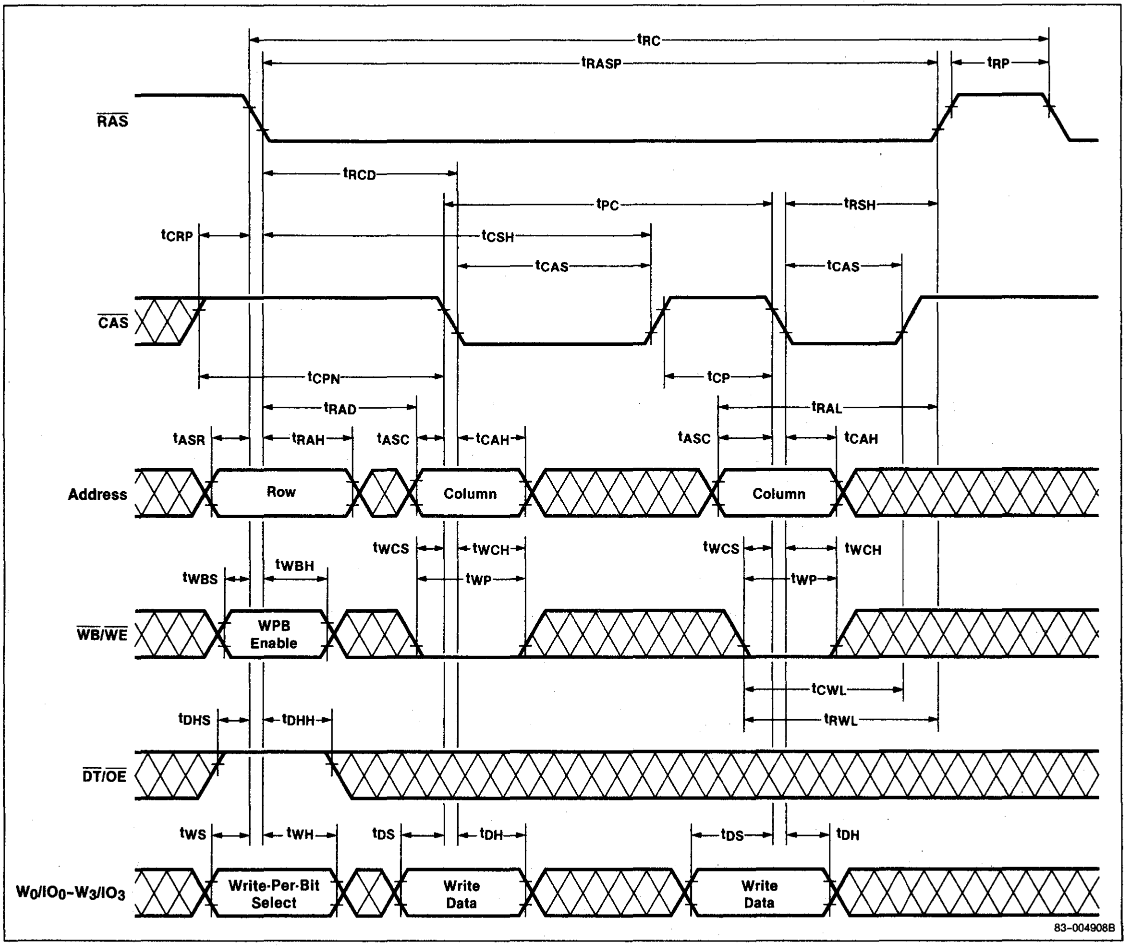
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Write Cycle



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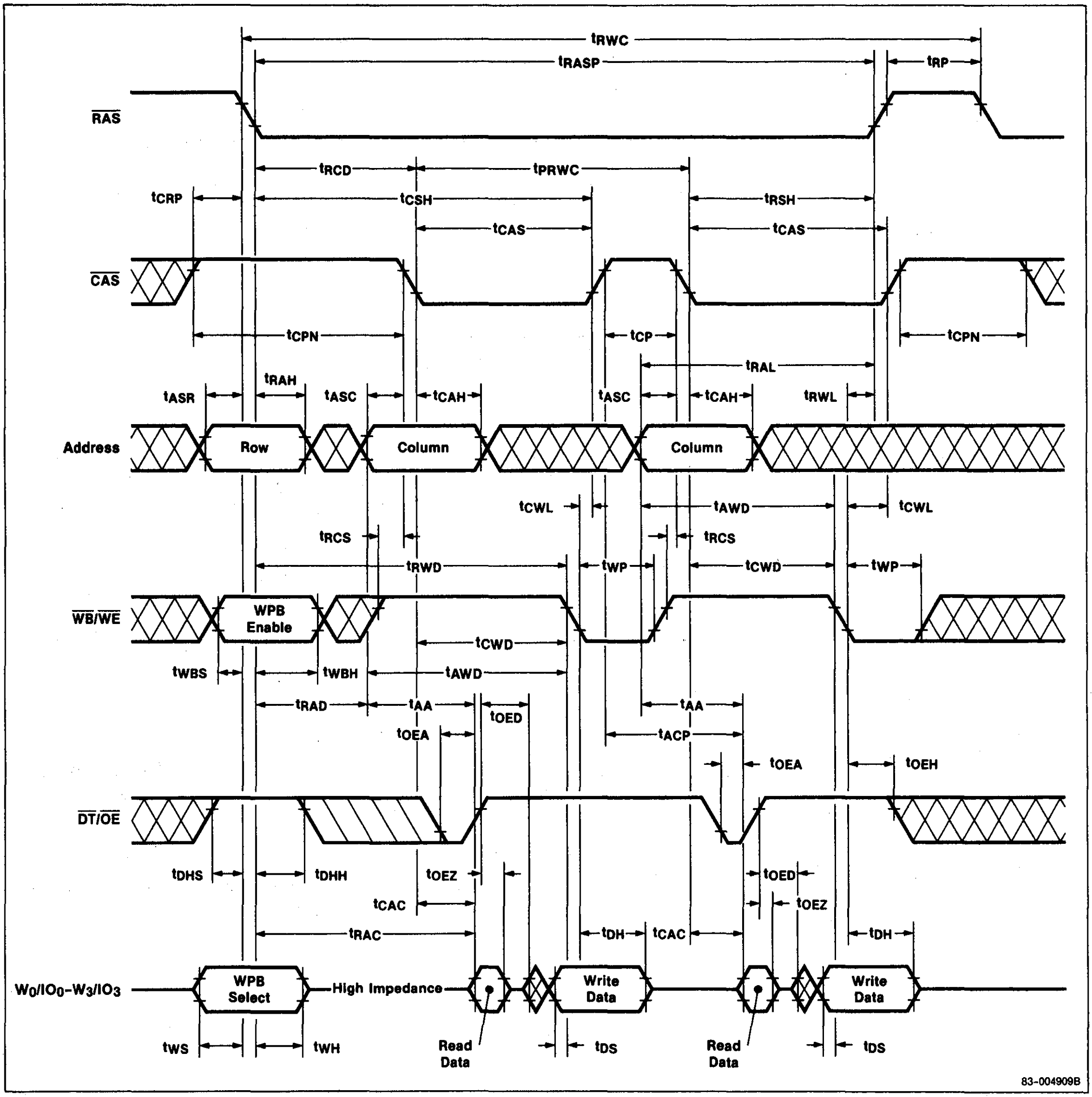
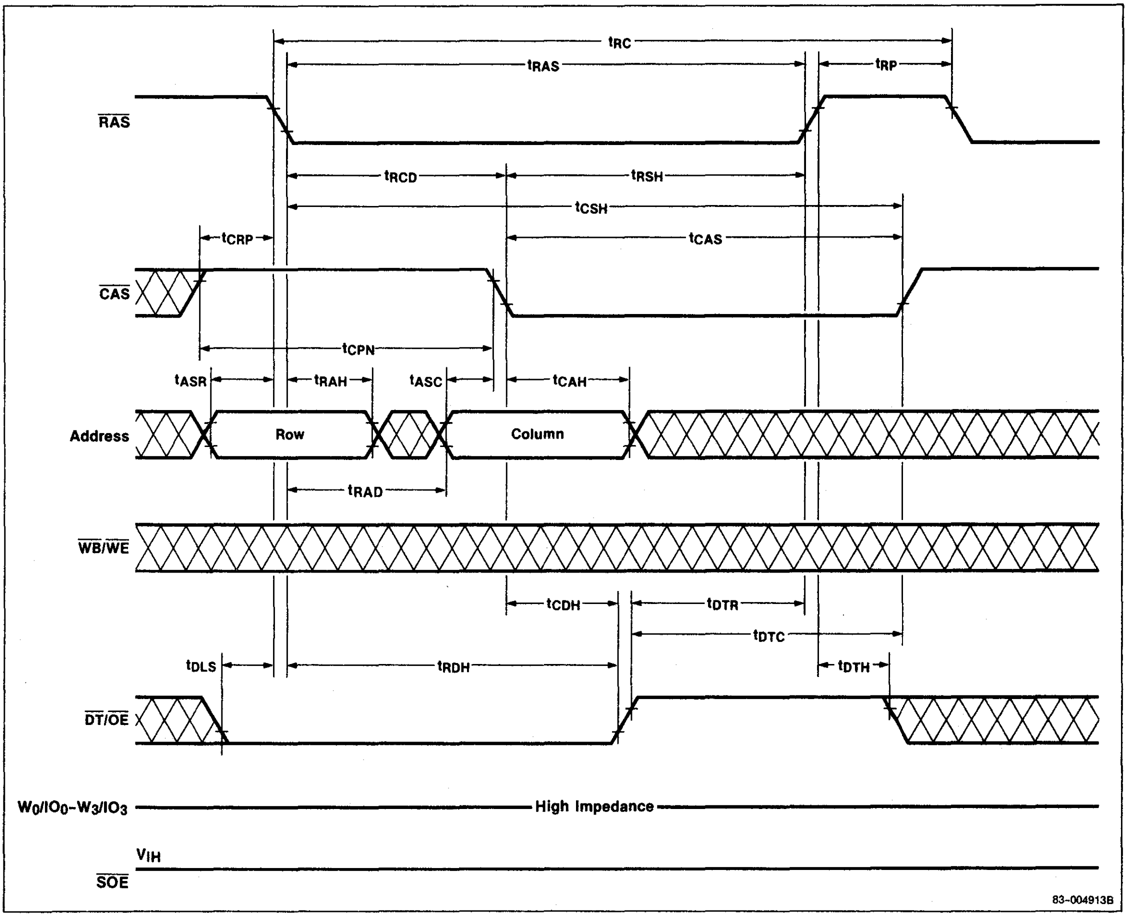
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



Timing Waveforms (cont)

Data Transfer Cycle (Serial Port Standby)



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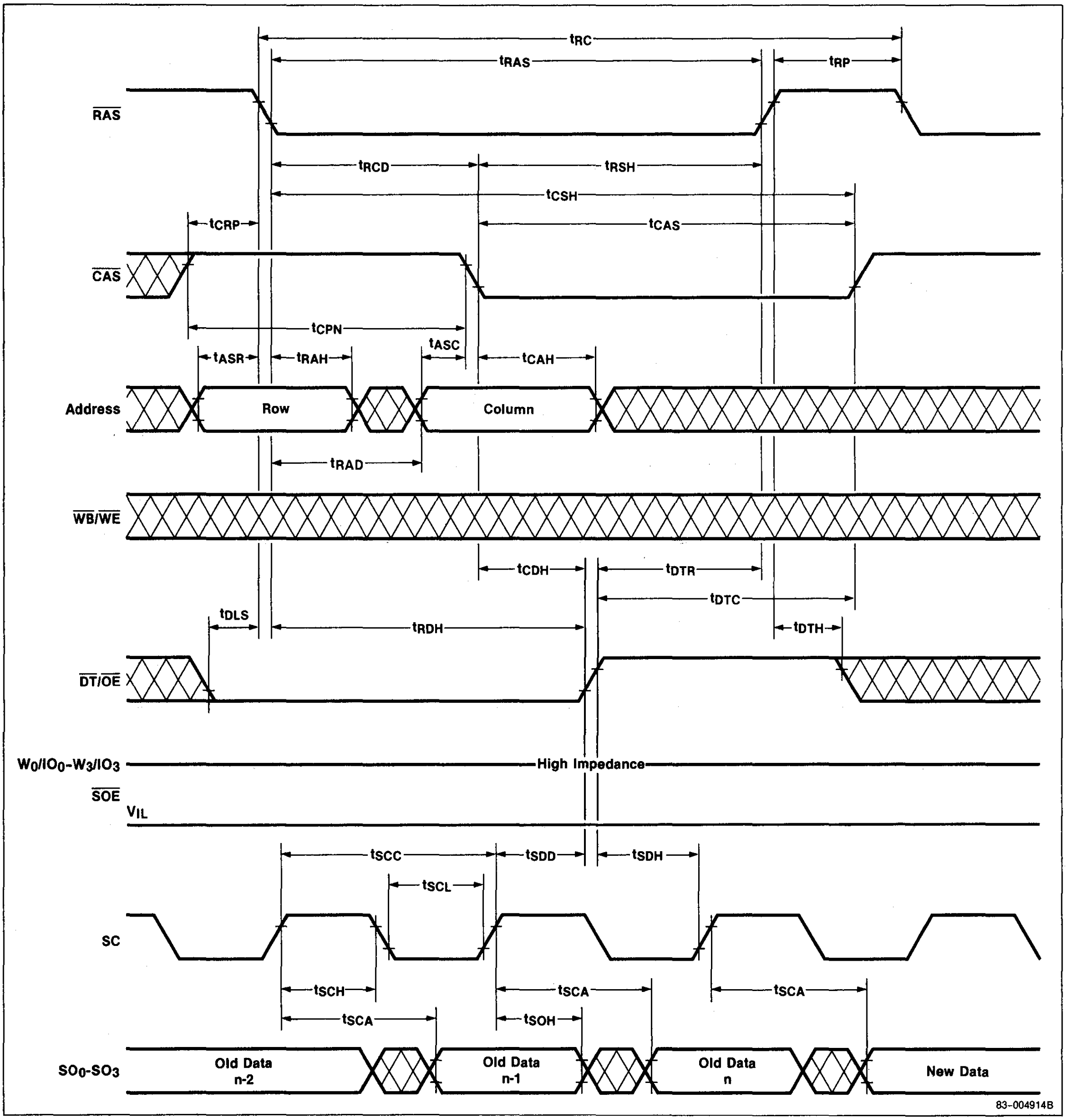
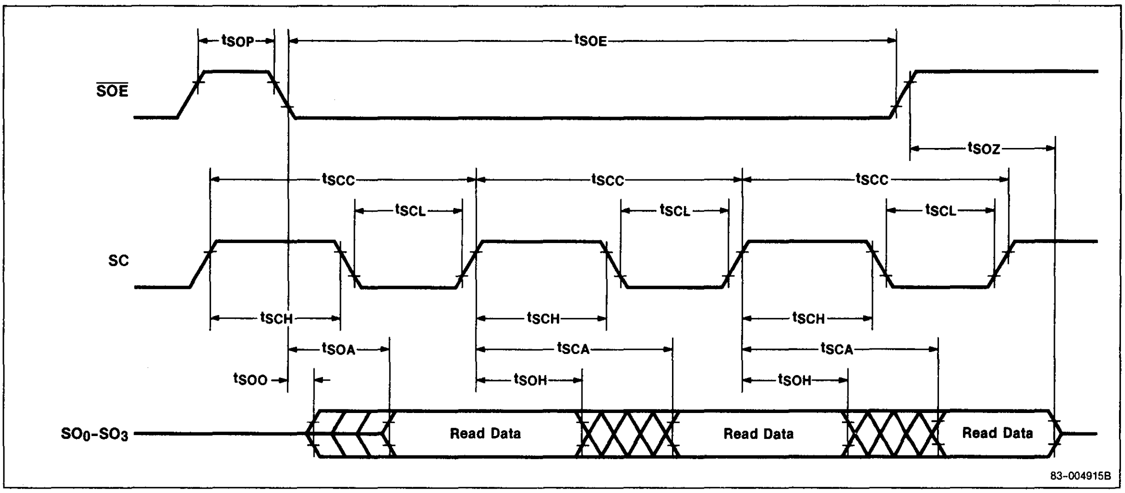
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port Active)



Timing Waveforms (cont)

Serial Read Cycle



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μPD42274 DUAL-PORT GRAPHICS BUFFER

PRELIMINARY INFORMATION

Description

The μPD42274 is a dual-port graphics buffer equipped with a 256K x 4-bit random access port and a 512 x 4-bit serial read port. The random access port is used by the host CPU to read or write data addressed in any desired order. The serial read port is connected to an internal 2048-bit data register through a 512 x 4-bit serial read output circuit.

In addition to its conventional features, the random access port also has a write-per-bit capability that allows each of the four data bits to be individually selected or masked for a write cycle. Furthermore, a flash write option with write-per-bit control is provided by the FWE pin and enables data in the color register to be written to a selected row in the random access port.

The μPD42274 features fully asynchronous dual access, except when transferring stored graphics data from a selected row of the storage array to the data register. During a data transfer, the random access port requires a special timing cycle using a transfer clock; the serial read port, however, continues to operate normally. Following the clock transition of a data transfer, the serial read output data changes from an old line to a new line and the starting location on the new line is addressable in the data transfer cycle.

The μPD42274 is fabricated with an advanced CMOS silicon-gate process using polycide technology and trench capacitors. The process provides high storage cell density, high performance, and high reliability.

Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during an 8-ms period. Automatic internal refreshing, by means of either hidden refreshing or the $\overline{CAS}$ before $\overline{RAS}$ timing and on-chip internal refresh circuitry, is also available. The transfer of a row of data from the storage array to the data register also refreshes that row automatically.

All inputs and outputs, including clocks, are TTL-compatible. All address and data-in signals are latched on-chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The μPD42274 is available in a 28-pin plastic ZIP or 28-pin plastic SOJ and is guaranteed for operation at 0 to +70°C.

Features

- ☐ Three functional blocks
  - — 256K x 4-bit random access storage array
  - — 2048-bit data register
  - — 512 x 4-bit serial read output circuit
- ☐ Two data ports: random access and serial read
- ☐ Dual-port accessibility except during data transfer
- ☐ Addressable start of serial read operation
- ☐ Real-time data transfer
- ☐ Single +5-volt ± 10% power supply
- ☐ On-chip substrate bias generator
- ☐ Random access port
  - — Two main clocks: $\overline{RAS}$ and $\overline{CAS}$
  - — Multiplexed address inputs
  - — Direct connection of I/O and address lines allowed by $\overline{OE}$ to simplify system design
  - — Refresh interval: 512 cycles/8 ms
  - — Read, early write, late write, read-write/read-modify-write, $\overline{RAS}$-only refresh, and fast-page capabilities
  - — Automatic internal refreshing by means of the $\overline{CAS}$ before $\overline{RAS}$ on-chip address counter
  - — Hidden refreshing by means of $\overline{CAS}$-controlled output
  - — Write-per-bit capability regarding four I/O bits
  - — Write bit selection multiplexed on IO_0-IO_3
- ☐ Flash write option with write-per-bit control
- ☐ $\overline{RAS}$-activated data transfer
  - — Same cycle time as for random access
  - — Row data transferred to data register as specified by row address inputs
  - — Starting location of following serial read operation specified by column address inputs
  - — Transfer of 2048 bits of data on one row to the data register, and the starting location of the serial read circuit, activated by a low-to-high transition of $\overline{DT}$
  - — Data transfer during real-time or standby operation of serial port
- ☐ Fast serial read operation by means of serial control pins
  - — Serial data presented on SO_0-SO_3
  - — Direct connection of multiple serial outputs for extension of data length
- ☐ Fully TTL-compatible inputs, outputs, and clocks
- ☐ Three-state outputs for random and serial access
- ☐ CMOS silicon-gate process with trench capacitors
- ☐ 400-mil, 28-pin plastic SOJ and 28-pin plastic ZIP packaging

Ordering Information

Part Number	Row Access Time (max)	Serial Access Time (max)	Package
μPD42274LE-10	100 ns	30 ns	28-pin plastic SOJ
LE-12	120 ns	40 ns	
μPD42274V-10	100 ns	30 ns	28-pin plastic ZIP
V-12	120 ns	40 ns	

Pin Identification

Symbol	Function
A_0-A_8	Address inputs
W_0/IO_0-W_3/IO_3	Write selects in write-per-bit/data inputs and outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB}/\overline{WE}$	Write-per-bit/write enable
$\overline{DT}/\overline{OE}$	Data transfer/output enable
FWE	Flash write enable
SO_0-SO_3	Serial read outputs
SC	Serial control
$\overline{SOE}$	Serial output enable
GND	Ground
V_{CC}	+5-volt ±10% power supply
NC	No connection

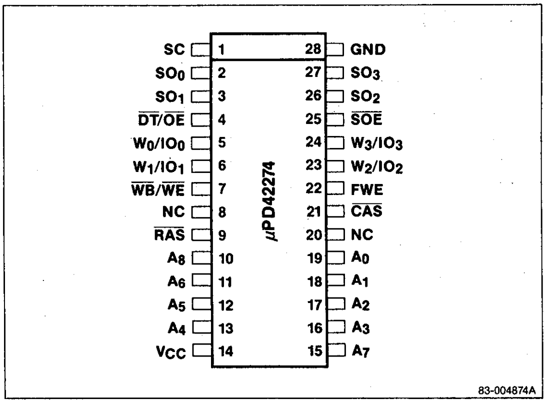
Absolute Maximum Ratings

Voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.0 to +7.0 V
Voltage on V_{CC} relative to GND, V_{R2}	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

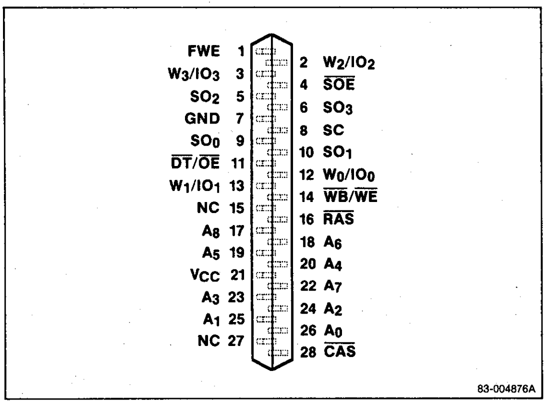
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configurations

28-Pin Plastic SOJ



28-Pin Plastic Zip



Pin Functions

A_0-A_8 [Address Inputs]. These pins are multiplexed as row address inputs and column address inputs. Since each of four data bits in the random access port corresponds to 262,144 storage cells, nine row addresses and nine column addresses are required to decode one cell location. Nine row addresses are used to select one of the 512 possible rows for a read, write, data transfer, or refresh operation. Nine column addresses are then used to select the one of 512 possible column decoders for a read or write cycle or the one of 512 possible starting locations for the next serial read cycle. (Column addresses are not required in $\overline{\text{RAS}}$-only refresh or flash write cycles.)

W_0/IO_0-W_3/IO_3 [Write-Per-Bit Inputs/Common Data Inputs and Outputs]. Each of the four data bits can be individually latched by these inputs at the falling edge of $\overline{\text{RAS}}$ in a write or flash write cycle, and then updated at the next falling edge of $\overline{\text{RAS}}$.

In a read cycle, these pins function as outputs for the selected storage cells. In a write cycle, input data on these pins is latched by the falling edge of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.

$\overline{\text{RAS}}$ [Row Address Strobe]. This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 2,048 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The nine row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$, $\overline{\text{WB}}/\overline{\text{WE}}$, and FWE are simultaneously latched to determine device operation.

$\overline{\text{CAS}}$ [Column Address Strobe]. This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The nine column address bits are latched at the falling edge of $\overline{\text{CAS}}$.

$\overline{\text{WB}}/\overline{\text{WE}}$ [Write-Per-Bit Control/Write Enable]. At the falling edge of $\overline{\text{RAS}}$, the inputs $\overline{\text{WB}}/\overline{\text{WE}}$ and FWE must be low and $\overline{\text{CAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ high to enable the write-per-bit capability. When $\overline{\text{CAS}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ and FWE are high at the falling edge of $\overline{\text{RAS}}$, the level of this signal indicates either a color register set cycle or flash write cycle. A high $\overline{\text{WB}}/\overline{\text{WE}}$ can be used at the beginning of a standard write or read cycle.

$\overline{\text{DT}}/\overline{\text{OE}}$ [Data Transfer/Output Enable]. At the falling edge of $\overline{\text{RAS}}$, a high-level $\overline{\text{CAS}}$, a low FWE and a low $\overline{\text{DT}}/\overline{\text{OE}}$ initiate a data transfer, regardless of the level of $\overline{\text{WB}}/\overline{\text{WE}}$. A high $\overline{\text{DT}}/\overline{\text{OE}}$ initiates conventional read or write cycles and controls the output buffer in the random access port.

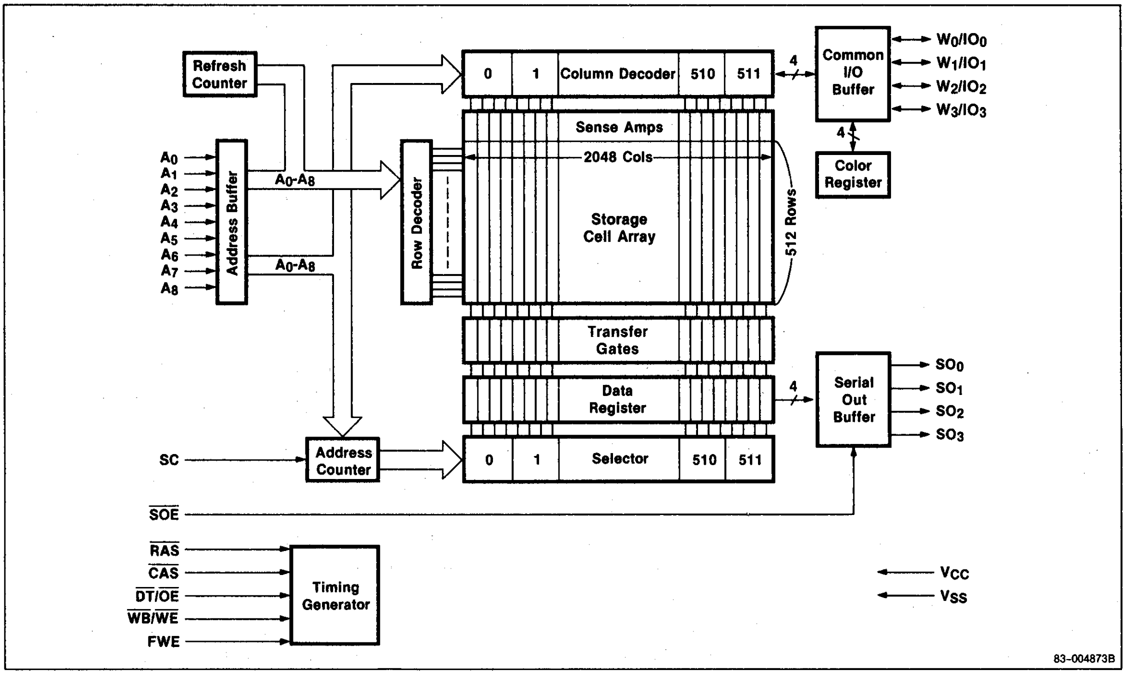
FWE [Flash Write Enable]. If this signal is low and $\overline{\text{CAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ are high at the falling edge of $\overline{\text{RAS}}$, a read or write cycle is initiated. If FWE, $\overline{\text{CAS}}$ and $\overline{\text{DT}}/\overline{\text{OE}}$ are high at the falling edge of $\overline{\text{RAS}}$, either a color register set cycle or flash write cycle is initiated depending on the level of $\overline{\text{WB}}/\overline{\text{WE}}$.

SO_0-SO_3 [Serial Data Output]. Four-bit data is read from these pins. Data remains valid until the next SC signal is activated.

SC [Serial Control]. By activating this signal repeatedly, the serial read operation (starting from the location specified in the data transfer cycle) is performed within the 2,048 bits in the data register. The rising edge of SC activates the serial read operation, in which four of the 2,048 data bits are transferred to four serial data buses, respectively, and read out. Whenever SC is low, the serial port is in standby.

$\overline{\text{SOE}}$ [Serial Output Enable]. This signal controls the serial data output buffer.

Block Diagram



Device Operation

Overall Description

The μPD42274 consists of a random access port and a serial read port. The random access port performs standard read and write operation as well as the data transfer and flash write operations, all of which are based on a conventional $\overline{RAS}/\overline{CAS}$ timing cycle. In a data transfer, data in each storage cell on the selected row is transferred simultaneously through a transfer gate to the corresponding register location. Flash write is used to write an entire row of data to predetermined values. The serial read port shows the contents of the data register in serial order. The random access port and the serial read port can operate asynchronously, except when the transfer gate is turned on during the data transfer period.

Addressing

The graphics storage array is arranged in a 512-row by 2048-column matrix. Each of 4 data bits in the random access port corresponds to 262,144 storage cells. Therefore, 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 through A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 through A_8 and latched onto the chip by $\overline{CAS}$. All addresses must be stable, on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable signal; whenever it is activated, 2048 cells on the selected row are sensed simultaneously and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Through 1 of 512 column decoders, 4 storage cells on the row are connected to 4 data buses, respectively. In the data transfer cycle, 9 row address bits are used to select 1 of the 512 possible rows involved in the transfer of data to the data register. Nine column address bits are then used to select the 1 of 512 possible serial decoders that corresponds to the starting location of the next serial read cycle.

In the serial read port, when SC is activated, 4 data bits in the 2048-bit data register are transferred to 4 serial data buses and read out. By activating SC repeatedly, the serial read operation (starting from the location specified in the data transfer cycle) is executed within the 2048 bits in the data register.

Random Access Port Operation

An operation in the random access port begins with a negative transition of $\overline{\text{RAS}}$. Both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following functions are multiplexed in the random access port.

- $\overline{\text{DT}}/\overline{\text{OE}}$
- $\overline{\text{WB}}/\overline{\text{WE}}$
- W_i/IO_i (i = 0, 1, 2, 3)

The $\overline{\text{OE}}$, $\overline{\text{WE}}$ and IO_i functions represent standard operations. The $\overline{\text{DT}}$, $\overline{\text{WB}}$, and W_i functions are special inputs to be applied in the same way as row address inputs, with setup and hold times referenced to the negative transition of $\overline{\text{RAS}}$. The $\overline{\text{DT}}$ level determines whether a cycle is a random access operation or a data transfer operation. $\overline{\text{WB}}$ affects only write cycles and determines whether or not the write-per-bit capability is used. W_i defines data bits to be written with the write-per-bit capability. In the following discussions, these multiplexed pins are designated as $\overline{\text{DT}}(/\overline{\text{OE}})$, for example, depending on the function being described.

To use the μPD42274 for random access, $\overline{\text{DT}}(/\overline{\text{OE}})$ must be high as $\overline{\text{RAS}}$ falls. Holding $\overline{\text{DT}}(/\overline{\text{OE}})$ high disconnects the 2048-bit register from the corresponding 2048-digit lines of the storage array. Conversely, to execute a data transfer, $\overline{\text{DT}}(/\overline{\text{OE}})$ must be low as $\overline{\text{RAS}}$ falls to open the 2048 transfer gates and transfer data from one of the rows to the register.

Truth Table (Random Access Port)

$\overline{\text{CAS}}$	$\overline{\text{DT}}/\overline{\text{OE}}$	$\overline{\text{WB}}/\overline{\text{WE}}$	FWE	Function
H	H	H	L	Read or write cycle (Note 1)
H	H	L	L	Mask write cycle (Note 2)
H	L	X	L	Read data transfer cycle (Note 3)
H	L	H	H	
L	X	X	X	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle (Note 4)
H	H	H	H	Color register set cycle (Note 5)
H	H	L	H	Flash write cycle (write-per-bit) (Note 6)

Notes:

(1) Initiates a normal read or write cycle and disables the write-per-bit capability.

(2) Enables the write-per-bit capability. Individual bits can be selected or masked for a write cycle. Four-bit masked data is latched at the falling edge of $\overline{\text{RAS}}$ and reset at the rising edge of $\overline{\text{RAS}}$.

(3) Initiates a read data transfer cycle.

(4) Initiates a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. As $\overline{\text{RAS}}$ falls, $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ and FWE = don't care.

(5) Defines a color register set cycle, where data in the register can be accessed in a read or write cycle.

(6) Initiates a flash write cycle, where the storage cells on an entire selected row can be set to the same data stored in the color register with write-per-bit control. As $\overline{\text{RAS}}$ falls, the input level of $\overline{\text{DT}}/\overline{\text{OE}}$ = don't care.

(7) X = don't care.

Read Cycle. A read cycle is executed by activating $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{OE}}$ and maintaining a high $(\overline{\text{WB}}/)\overline{\text{WE}}$ during an active $\overline{\text{CAS}}$. The $(W_i/)IO_i$ data pin (i = 0, 1, 2, 3) remains in a state of high impedance until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay (t_{RCD}) + t_{CAC}
- $\overline{\text{RAS}}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{\text{RAS}}$ to $\overline{\text{OE}}$ delay + t_{OEA}

Access times from $\overline{\text{RAS}}$ (t_{RAC}), from $\overline{\text{CAS}}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{\text{OE}}$ (t_{OEA}) are device parameters. The $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$, $\overline{\text{RAS}}$ to column address, and $\overline{\text{RAS}}$ to $\overline{\text{OE}}$ delays are system-dependent timing parameters.

Output becomes valid after the access time has elapsed and it remains valid while both $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ are low. A high $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ returns the output pins to high impedance.

Write Cycle. A write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes the data on (W_i/)IO_i into the on-chip data latch. To make use of the write-per-bit capability, $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case, data bits to which the write operation is applied can be specified by keeping W_i(/IO_i) high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

For those data bits of W_i(/IO_i) that are kept low as $\overline{RAS}$ falls, write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability is not used and a write cycle is executed for all four data bits.

Early Write Cycle. An early write cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in a state of high impedance for the entire cycle. As $\overline{RAS}$ falls, ($\overline{DT}$/)$\overline{OE}$ must meet the setup and hold times of a high $\overline{DT}$; but otherwise ($\overline{DT}$/)$\overline{OE}$ does not affect any circuit operation during an active $\overline{CAS}$.

Read-Write/Read-Modify-Write [RW/RMW] Cycle. An RW/RMW cycle is executed by bringing ($\overline{WB}$/)$\overline{WE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. (W_i/)IO_i shows read data at access time. Afterward, in preparation for the upcoming write cycle, (W_i/)IO_i is returned to a high-impedance condition by a high ($\overline{DT}$/)$\overline{OE}$. The data to be written is strobed by ($\overline{WB}$/)$\overline{WE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of ($\overline{DT}$/)$\overline{OE}$, which can be activated just after ($\overline{WB}$/)$\overline{WE}$ falls, even when ($\overline{WB}$/)$\overline{WE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 through A_8) will refresh all storage cells. Any operation performed in the random access port (i.e., read, write, refresh, data transfer, color register set, or flash write) refreshes the 2048 bits selected by the $\overline{RAS}$ addresses or by the on-chip refresh address counter.

RAS-only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all of the storage cells in one row of the graphics storage array. A high $\overline{CAS}$ is maintained during an active $\overline{RAS}$ to keep (W_i/)IO_i in a state of high impedance. This mode is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle. This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically performs refreshing for row addresses specified by the internal refresh address counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle.

Hidden Refresh Cycle. This function performs hidden refreshing after a read cycle, without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Fast-Page Cycle. This feature allows effectively faster data access by keeping the same row address and strobing successive column addresses onto the chip. By maintaining a low $\overline{RAS}$ while successive $\overline{CAS}$ cycles are executed, data is transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. During this operation, read, write and RW/RMW cycles are possible. Additionally, the write-per-bit control specified in the entry write cycle is maintained through the following fast-page write cycle.

During a fast-page read cycle, the (W_i/)IO_i data pin ($i = 0, 1, 2,$ or 3) remains in a state of high impedance until valid data appears at the output pin at access time. Device access time in this cycle will be one of the following calculated intervals:

- t_{ACP}, when $t_{ASC} \geq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
- t_{AA}, when $t_{ASC} \leq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max) or when $t_{ASC} \leq t_{CP}$ and $t_{CP} \leq t_{CP}$ (max)
- t_{CAC}, when $t_{ASC} \geq t_{ASC}$ (max) and $t_{CP} \geq t_{CP}$ (max)

Data Transfer Cycle. A data transfer cycle is executed by bringing $\overline{DT}$(/$\overline{OE}$) and FWE low as $\overline{RAS}$ falls. As described previously, the specified 1 of the possible 512 rows involved in the data transfer, as well as the starting location of the following serial read cycle in the serial read port, are defined by address inputs. $\overline{DT}$(/$\overline{OE}$) must be low for a specified time, measured from $\overline{RAS}$ and $\overline{CAS}$, so that the data transfer condition may be satisfied. The low-to-high transition of $\overline{DT}$ causes two transfer operations through the data transfer gates:

column address buffer outputs are transferred to the serial address counters, and storage cell data amplified on digit lines is transferred to the data register. $\overline{RAS}$ and $\overline{CAS}$ must be low during these operations to keep the data in the random access port.

Color Register Set Cycle. A color register set cycle is executed in the same fashion as a conventional read or write cycle, with the level of FWE high as $\overline{RAS}$ falls. In this cycle, read or write operation is available to the color register under the control of $\overline{WE}$. In read operation, color register data is read out on the common IO_i pins. In write operation, common IO_i data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 through A_8 in this cycle.

Flash Write Cycle. A flash write cycle can clear or set each of the four 512-bit data sets on the selected one of 512 possible rows according to data stored in the color register. Bit mask inputs are latched as $\overline{RAS}$ falls. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Serial Read Port Operation

The serial read port is used only to read serially the contents of the data register starting from a specified location. The entire operation, therefore, follows the data transfer cycle. The only condition under which the serial read port must synchronize with the random access port is when the positive transition of $\overline{DT}(/\overline{OE})$ must occur within a specified period in an SC cycle. Except for this SC cycle, the serial read port can operate asynchronously with the random access port. The output data appears at SO_i after an access time of t_{SCA}, measured from a high SC, only when a low $\overline{SOE}$ is maintained. The SC cycle which includes the positive transition of $\overline{DT}(/\overline{OE})$ shows old data in the data register; subsequent SC cycles show new data transferred to the data register serially and in a looped manner. The serial output is maintained until the next SC signal is activated. $\overline{SOE}$ controls the impedance of the serial output to allow multiplexing of more than one bank of μPD42274 graphics buffers into the same external circuitry. When $\overline{SOE}$ is at a low logic level, SO_i is enabled and the proper data is read. When $\overline{SOE}$ is at a high logic level, SO_i is disabled and in a state of high impedance.

Recommended DC Operating Conditions

$T_A = 0$ to $+70°C$; GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V

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DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	$V_{IN} = 0$ to 5.5 V; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} (IO_i, SO_i) disabled; V_{OUT} = 0 to 5.5 V
Random access port output voltage, high	$V_{OH(R)}$	2.4			V	$I_{OH(R)} = -2$ mA
Random access port output voltage, low	$V_{OL(R)}$			0.4	V	$I_{OL(R)} = 4.2$ mA
Serial read port output voltage, high	$V_{OH(S)}$	2.4			V	$I_{OH(S)} = -1$ mA
Serial read port output voltage, low	$V_{OL(S)}$			0.4	V	$I_{OL(S)} = 2.1$ mA

Power Supply Current Definitions

Port	Operation	Symbol	Operating Conditions
Random Access	Read/write	RW	$\overline{RAS}$, $\overline{CAS}$ cycling; FWE low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
	Standby	STB	$\overline{CAS} = \overline{RAS} = V_{IH}$
	$\overline{RAS}$-only refresh	ROR	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; FWE low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
	Fast page	PAGE	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min)
	$\overline{CAS}$ before $\overline{RAS}$ refresh	CBR	$\overline{CAS}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
	Data transfer	DTR	$\overline{DT}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
	Color register set cycle	CRS	FWE and $\overline{WB}/\overline{WE}$ high as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
	Flash write	FW	FWE high and $\overline{WB}/\overline{WE}$ low as $\overline{RAS}$ falls; $t_{RC} = t_{RC}$ (min)
Serial Read	Standby	STB	$\overline{SOE} = V_{IH}$; SC = V_{IH} or V_{IL}
	Serial read	ACT	$\overline{SOE} = V_{IL}$; SC cycling; $t_{SCC} = t_{SCC}$ (min)

Capacitance

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; f = 1 MHz; GND = 0 V

Parameter	Symbol	Limit (max)	Unit	Pins Under Test
Input capacitance	$C_{I(A)}$	5	pF	A_0 to A_8
	$C_{I(\overline{DT}/\overline{OE})}$	8	pF	$\overline{DT}/\overline{OE}$
	$C_{I(\overline{WB}/\overline{WE})}$	8	pF	$\overline{WB}/\overline{WE}$
	$C_{I(FWE)}$	8	pF	FWE
	$C_{I(\overline{RAS})}$	8	pF	$\overline{RAS}$
	$C_{I(\overline{CAS})}$	8	pF	$\overline{CAS}$
	$C_{I(\overline{SOE})}$	8	pF	$\overline{SOE}$
	$C_{I(SC)}$	8	pF	SC
Input/output capacitance	$C_{IO(W/IO)}$	7	pF	W_0/IO_0 to W_3/IO_3
Output capacitance	$C_{O(SO)}$	7	pF	SO_0 to SO_3

Power Supply Current

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

Port			Limits			
			μPD42274			
			-10	-12		
Random Access	Serial Read	Symbol	Max	Max	Unit	Test Conditions (Note 1)
RW	STB	I_{CC1}	70	60	mA	
STB	STB	I_{CC2}	3	3	mA	
ROR	STB	I_{CC3}	70	60	mA	(Note 2)
PAGE	STB	I_{CC4}	60	50	mA	(Note 3)
CBR	STB	I_{CC5}	70	60	mA	
DTR	STB	I_{CC6}	70	60	mA	
RW	ACT	I_{CC7}	100	90	mA	
STB	ACT	I_{CC8}	35	30	mA	
ROR	ACT	I_{CC9}	100	90	mA	(Note 2)
PAGE	ACT	I_{CC10}	85	75	mA	(Note 3)
CBR	ACT	I_{CC11}	100	90	mA	
DTR	ACT	I_{CC12}	100	90	mA	
CRS	STB	I_{CC13}	65	55	mA	
FW	STB	I_{CC14}	65	55	mA	
CRS	ACT	I_{CC15}	100	90	mA	
FW	ACT	I_{CC16}	100	90	mA	

Notes:

(1) No load on IO_i or SO_i. Except for I_{CC2}, I_{CC3}, I_{CC6}, and I_{CC14}, real values depend on output loading in addition to cycle rates.

(2) $\overline{CAS}$ is not clocked, but is kept at a stable high level. The column addresses are also assumed to be kept stable, at a high or low level.

(3) A change in column addresses must not occur more than once in a fast-page cycle.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

Parameter	Symbol	Limits μPD42274-10 Min	Limits μPD42274-10 Max	Limits μPD42274-12 Min	Limits μPD42274-12 Max	Unit	Test Conditions
Switching Characteristics							
Access time from $\overline{\text{RAS}}$	t_{RAC}		100		120	ns	(Notes 3, 4 and 12)
Access time from falling edge of $\overline{\text{CAS}}$	t_{CAC}		25		30	ns	(Notes 3, 4, 13, 14 and 15)
Access time from column address	t_{AA}		55		65	ns	(Notes 3, 4, 14 and 15)
Access time from rising edge of $\overline{\text{CAS}}$	t_{ACP}		55		65	ns	(Notes 3 and 15)
Access time from $\overline{\text{OE}}$	t_{OEA}		25		30	ns	(Notes 3 and 4)
Serial output access time from SC	t_{SCA}		30		40	ns	(Note 3)
Serial output access time from $\overline{\text{SOE}}$	t_{SOA}		25		30	ns	(Note 3)
Output disable time from $\overline{\text{CAS}}$ high	t_{OFF}	0	25	0	30	ns	(Note 5)
Output disable time from $\overline{\text{OE}}$ high	t_{OEZ}	0	25	0	30	ns	(Note 5)
Serial output disable time from $\overline{\text{SOE}}$ high	t_{SOZ}	0	15	0	20	ns	(Note 5)
$\overline{\text{SOE}}$ low to serial output setup delay	t_{SOO}	5		5		ns	
Serial output hold time after SC high	t_{SOH}	5		10		ns	
Timing Requirements							
Random read or write cycle time	t_{RC}	190		220		ns	(Note 11)
RW/RMW cycle time	t_{RWC}	255		295		ns	(Note 11)
Fast-page cycle time	t_{PC}	60		70		ns	(Note 11)
Fast-page RW/RMW cycle time	t_{PRWC}	125		145		ns	(Note 11)

Parameter	Symbol	Limits μPD42274-10 Min	Limits μPD42274-10 Max	Limits μPD42274-12 Min	Limits μPD42274-12 Max	Unit	Test Conditions
Timing Requirements (cont)							
Transition time (rise and fall)	t_T	3	50	3	50	ns	(Notes 3, 10 and 18)
$\overline{\text{RAS}}$ precharge time	t_{RP}	80		90		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	100	10000	120	10000	ns	
Fast-page $\overline{\text{RAS}}$ pulse width	t_{RASP}	100	100000	120	100000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	25		30		ns	
$\overline{\text{CAS}}$ precharge time (non-page mode)	t_{CPN}	10		15		ns	
Fast-page $\overline{\text{CAS}}$ precharge time	t_{CP}	10	25	15	30	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	25	10000	30	10000	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	100		120		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	t_{RCD}	25	75	25	90	ns	(Note 4)
$\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low precharge time	t_{CRP}	10		10		ns	(Note 16)
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	12		15		ns	
Column address setup time	t_{ASC}	0	25	0	30	ns	(Note 15)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	17	45	20	55	ns	(Notes 9 and 14)
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	55		65		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time after $\overline{\text{RAS}}$ high	t_{RRH}	10		10		ns	(Note 6)
Read command hold time after $\overline{\text{CAS}}$ high	t_{RCH}	0		0		ns	(Note 6)

AC Characteristics (cont)

		Limits					
		μPD42274-10		μPD42274-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Timing Requirements (cont)							
Write command setup time	t_{WCS}	0		0		ns	(Note 7)
Write command hold time	t_{WCH}	20		30		ns	
Write command pulse width	t_{WP}	20		25		ns	(Note 17)
Write command to $\overline{\mathrm{RAS}}$ lead time	t_{RWL}	30		35		ns	
Write command to $\overline{\mathrm{CAS}}$ lead time	t_{CWL}	30		35		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 8)
Data-in hold time	t_{DH}	20		25		ns	(Note 8)
Column address to $\overline{\mathrm{WE}}$ delay	t_{AWD}	85		100		ns	(Note 7)
$\overline{\mathrm{CAS}}$ to $\overline{\mathrm{WE}}$ delay	t_{CWD}	55		65		ns	(Note 7)
$\overline{\mathrm{RAS}}$ to $\overline{\mathrm{WE}}$ delay	t_{RWD}	130		155		ns	(Note 7)
$\overline{\mathrm{OE}}$ high to data-in setup delay	t_{OED}	30		35		ns	
$\overline{\mathrm{OE}}$ high hold time after $\overline{\mathrm{WE}}$ low	t_{OEH}	25		30		ns	
$\overline{\mathrm{CAS}}$ before $\overline{\mathrm{RAS}}$ refresh setup time	t_{CSR}	0		0		ns	
$\overline{\mathrm{CAS}}$ before $\overline{\mathrm{RAS}}$ refresh hold time	t_{CHR}	15		20		ns	
$\overline{\mathrm{RAS}}$ high to CAS low precharge time	t_{RPC}	0		0		ns	
Refresh time interval	t_{REF}		8		8	ms	Addresses A_0-A_8
$\overline{\mathrm{DT}}$ low setup time	t_{DLS}	0		0		ns	
$\overline{\mathrm{DT}}$ low hold time after $\overline{\mathrm{RAS}}$ low	t_{RDH}	90		120		ns	

		Limits					
		μPD42274-10		μPD42274-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Timing Requirements (cont)							
$\overline{\mathrm{DT}}$ low hold time after $\overline{\mathrm{CAS}}$ low	t_{CDH}	30		35		ns	
SC high to $\overline{\mathrm{DT}}$ high delay	t_{SDD}	10		15		ns	
SC low hold time after $\overline{\mathrm{DT}}$ high	t_{SDH}	10		15		ns	
Serial clock cycle time	t_{SCC}	30		40		ns	(Note 11)
SC pulse width	t_{SCH}	10		15		ns	
SC precharge time	t_{SCL}	10		15		ns	
$\overline{\mathrm{DT}}$ high setup time	t_{DHS}	0		0		ns	
$\overline{\mathrm{DT}}$ high hold time	t_{DHH}	15		20		ns	
$\overline{\mathrm{DT}}$ high to $\overline{\mathrm{RAS}}$ high delay	t_{DTR}	10		10		ns	
$\overline{\mathrm{DT}}$ high to $\overline{\mathrm{CAS}}$ high delay	t_{DTC}	5		5		ns	
$\overline{\mathrm{OE}}$ to $\overline{\mathrm{RAS}}$ inactive setup time	t_{OES}	10		10		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write-per-bit hold time	t_{WBH}	15		20		ns	
Flash write enable setup time	t_{FWS}	0		0		ns	
Flash write enable hold time	t_{FWH}	15		20		ns	
Write bit selection setup time	t_{WS}	0		0		ns	
Write bit selection hold time	t_{WH}	15		20		ns	

AC Characteristics (cont)

		Limits					
		μPD42274-10		μPD42274-12			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Timing Requirements (cont)							
$\overline{SOE}$ pulse width	t_{SOE}	10		15		ns	
$\overline{SOE}$ precharge time	t_{SOP}	10		15		ns	
$\overline{DT}$ high hold time after $\overline{RAS}$ high	t_{DTH}	15		20		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved. Also, $\overline{SOE}$ must be held high or SC must be held low until completion of the first data transfer cycle.

(3) See input/output timing waveforms for timing reference voltages. See figures 3 and 4 for output loads.

(4) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. The t_{RCD} (max) limit is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}, t_{OEA}, or t_{AA}.

(5) An output disable time defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

(6) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(7) t_{WCS}, t_{AWD}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{AWD} \geq t_{AWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(8) These parameters are referenced to the falling edge of $\overline{CAS}$ in early write cycles and to the falling edge of ($\overline{WB}$/) $\overline{WE}$ in delayed write or read-modify-write cycles.

(9) Assumes that t_{RAD} (min) = t_{RAH} (min) + typical t_T of 5 ns.

(10) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Additionally, transition times are measured between V_{IH} and V_{IL}.

(11) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(12) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(13) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(14) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(15) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(16) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(17) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) Ac measurements assume t_T = 5 ns.

Figure 1. Input Timing

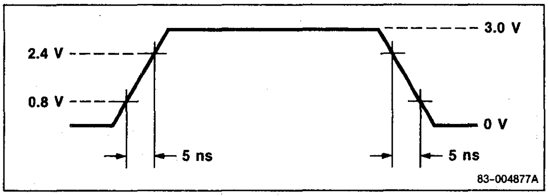

Figure 2. Output Timing

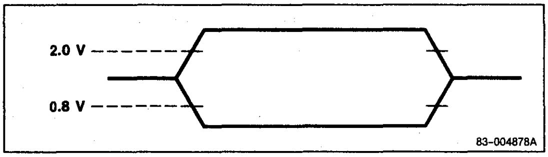

Figure 3. Random Access Port: Output Loading

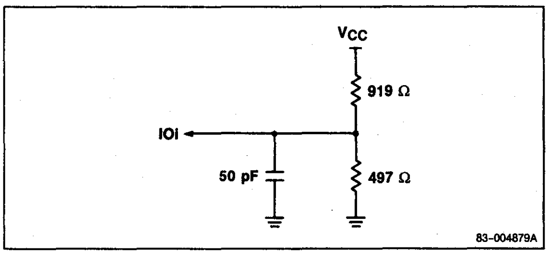

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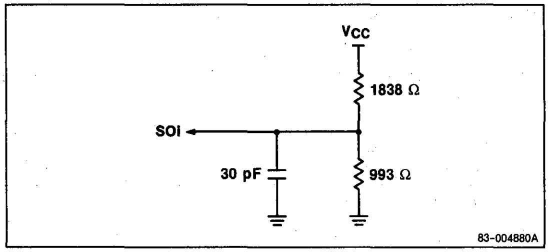
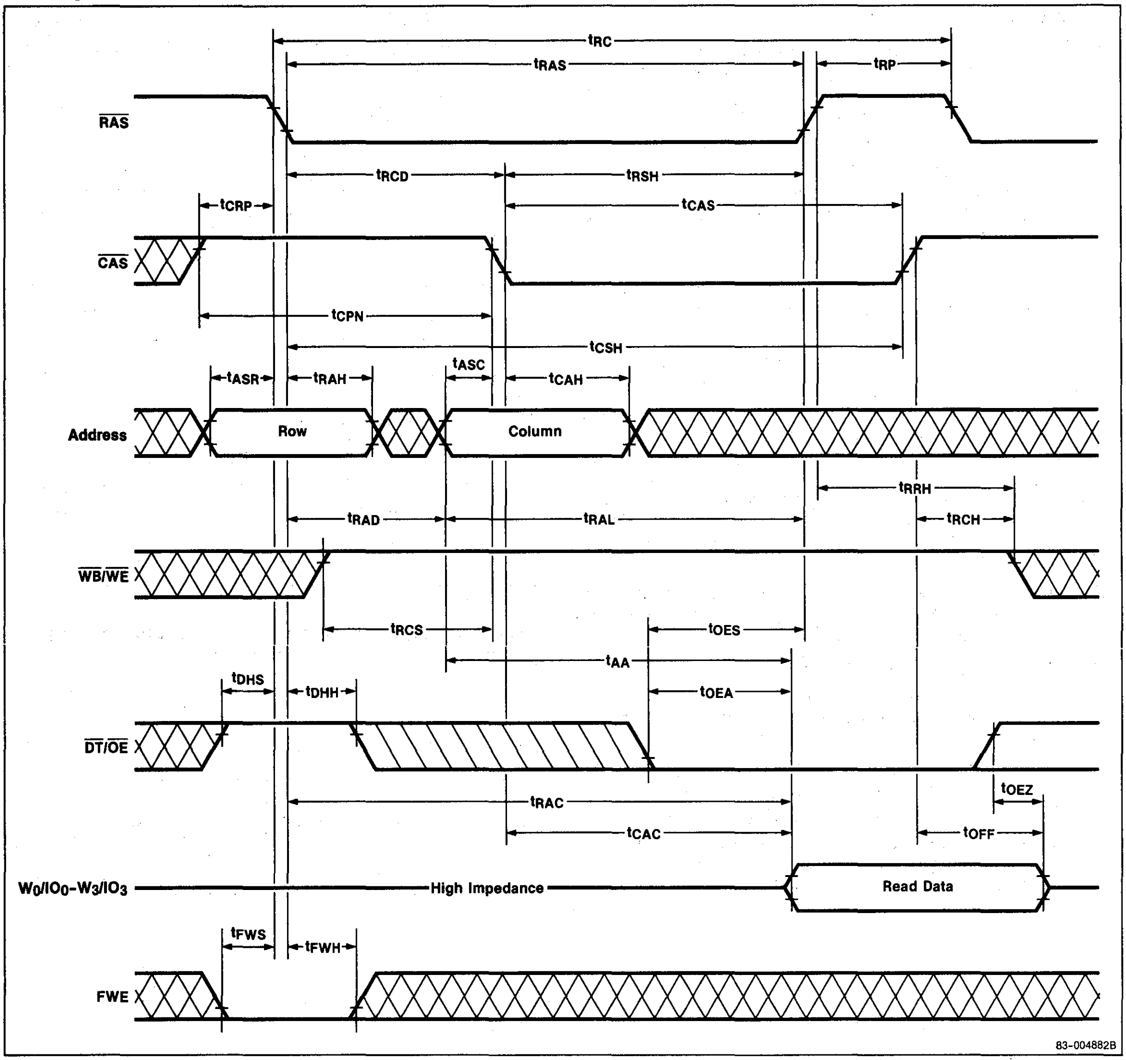
Figure 4. Serial Read Port: Output Loading



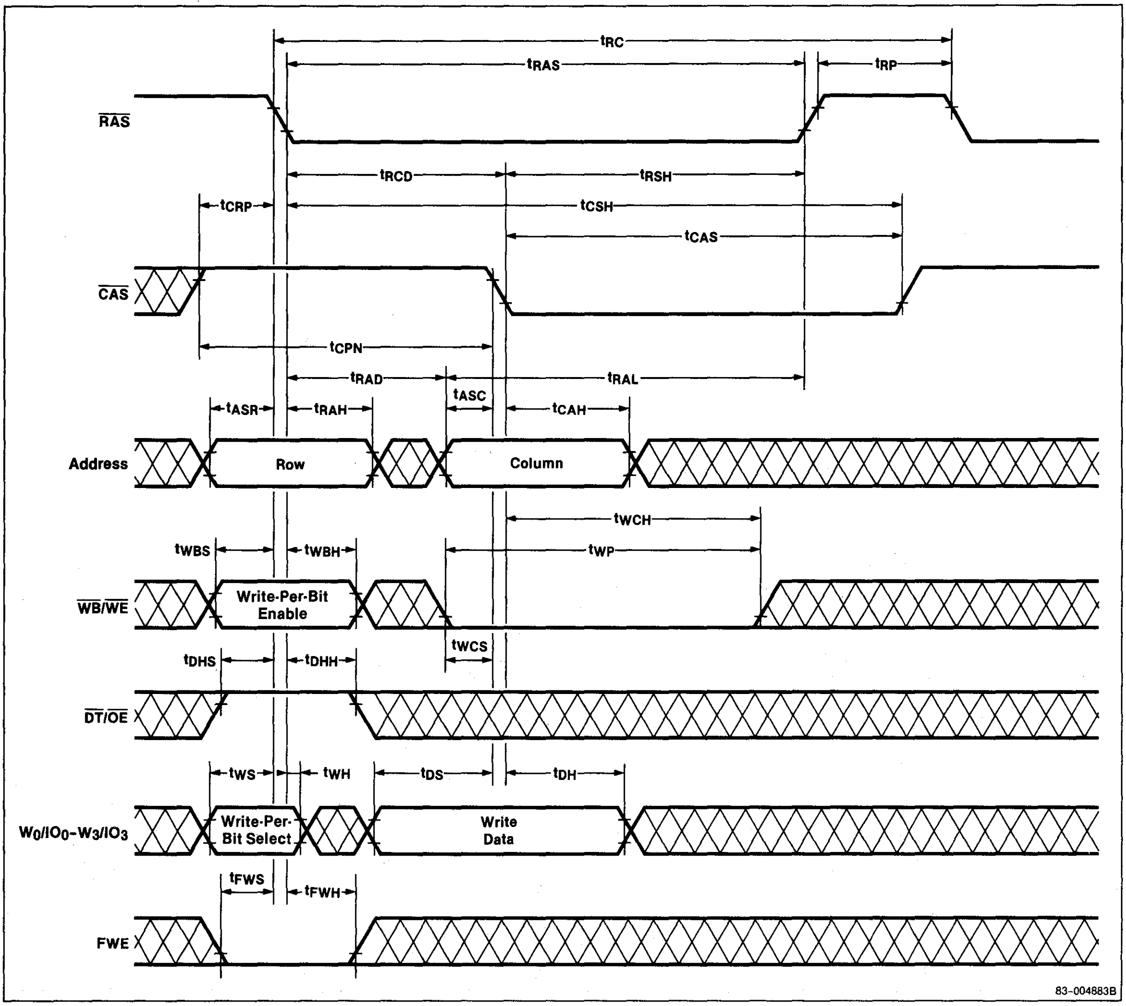
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Early Write Cycle



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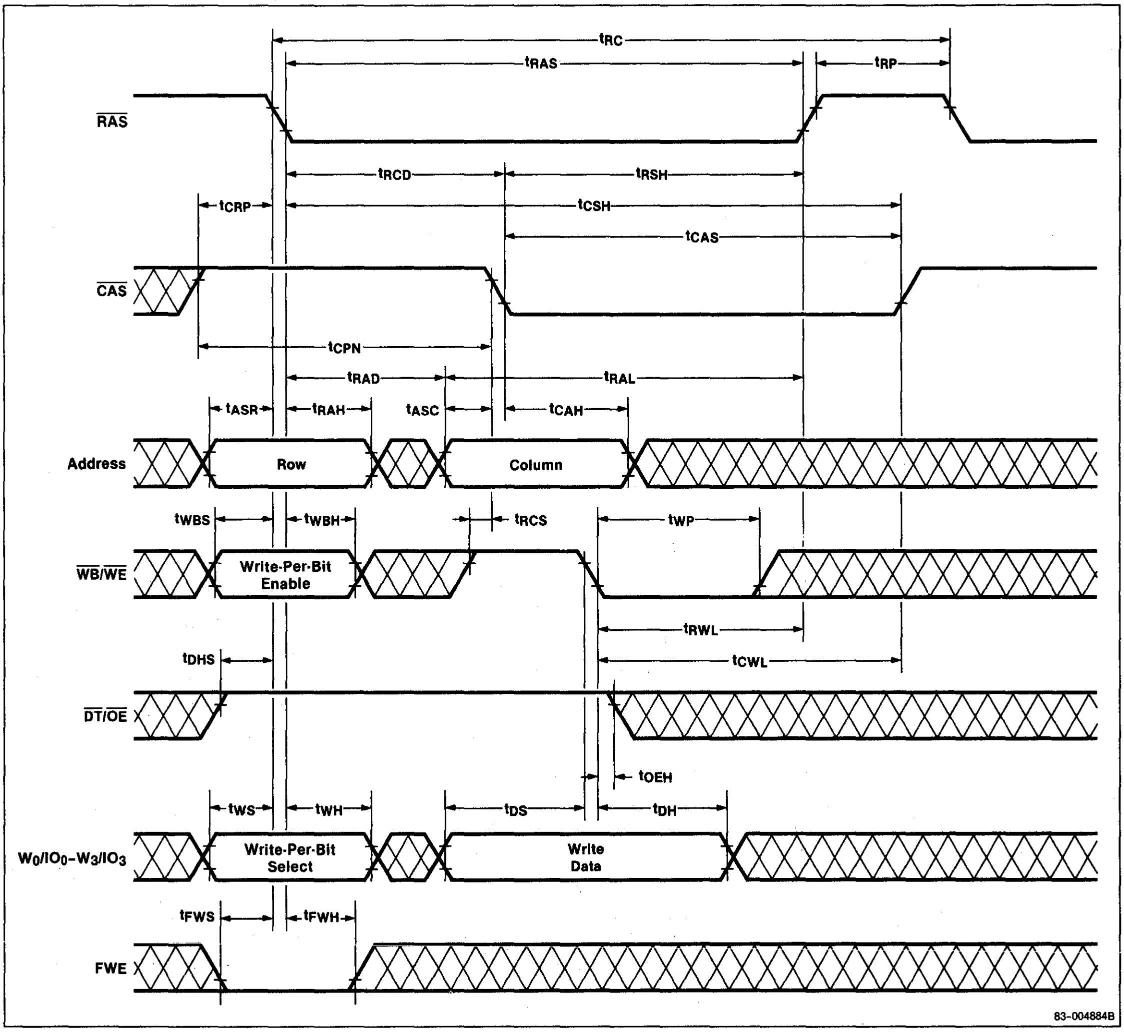
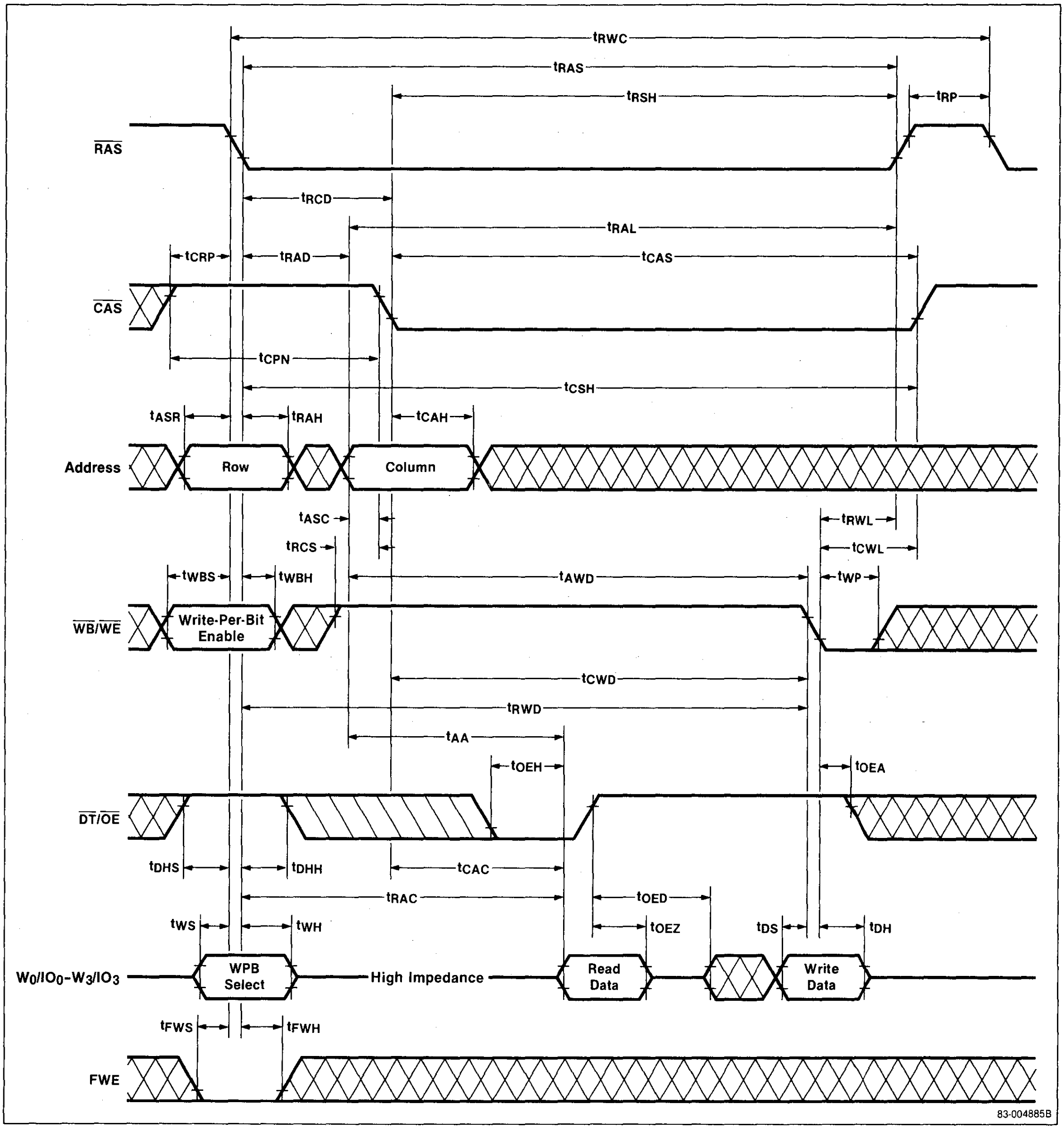
Timing Waveforms (cont)

Late Write Cycle



Timing Waveforms (cont)

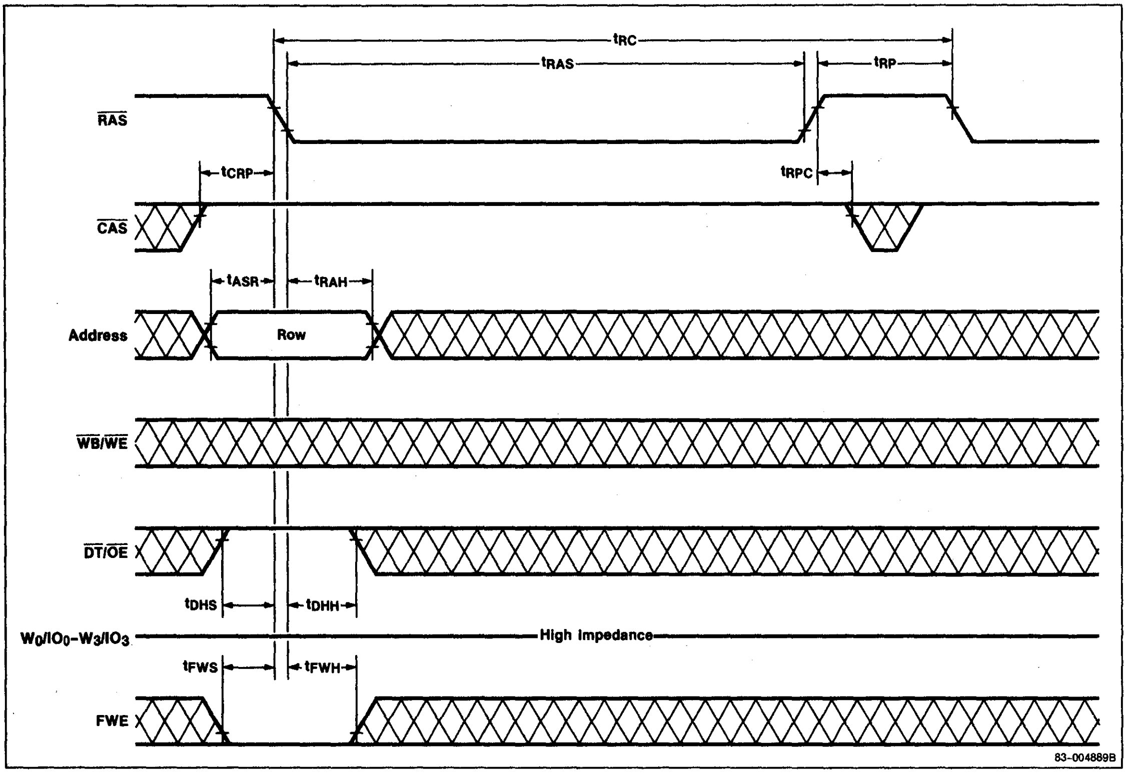
Read-Write/Read-Modify-Write Cycles



3

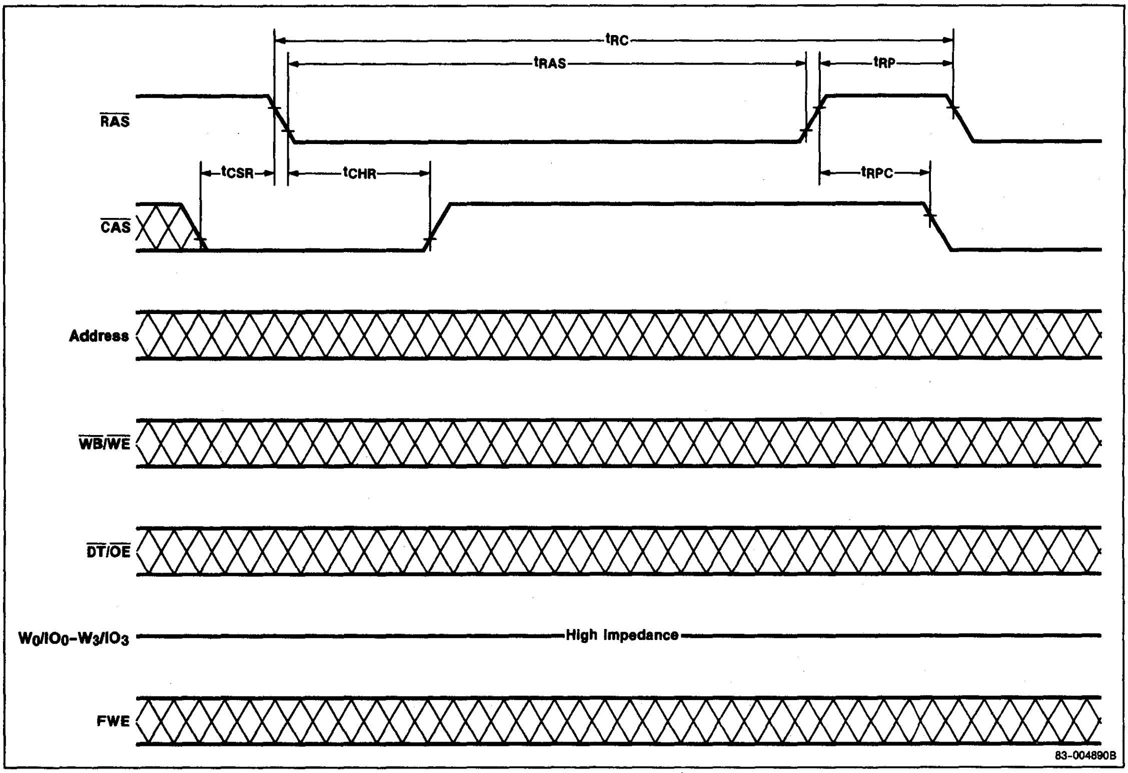
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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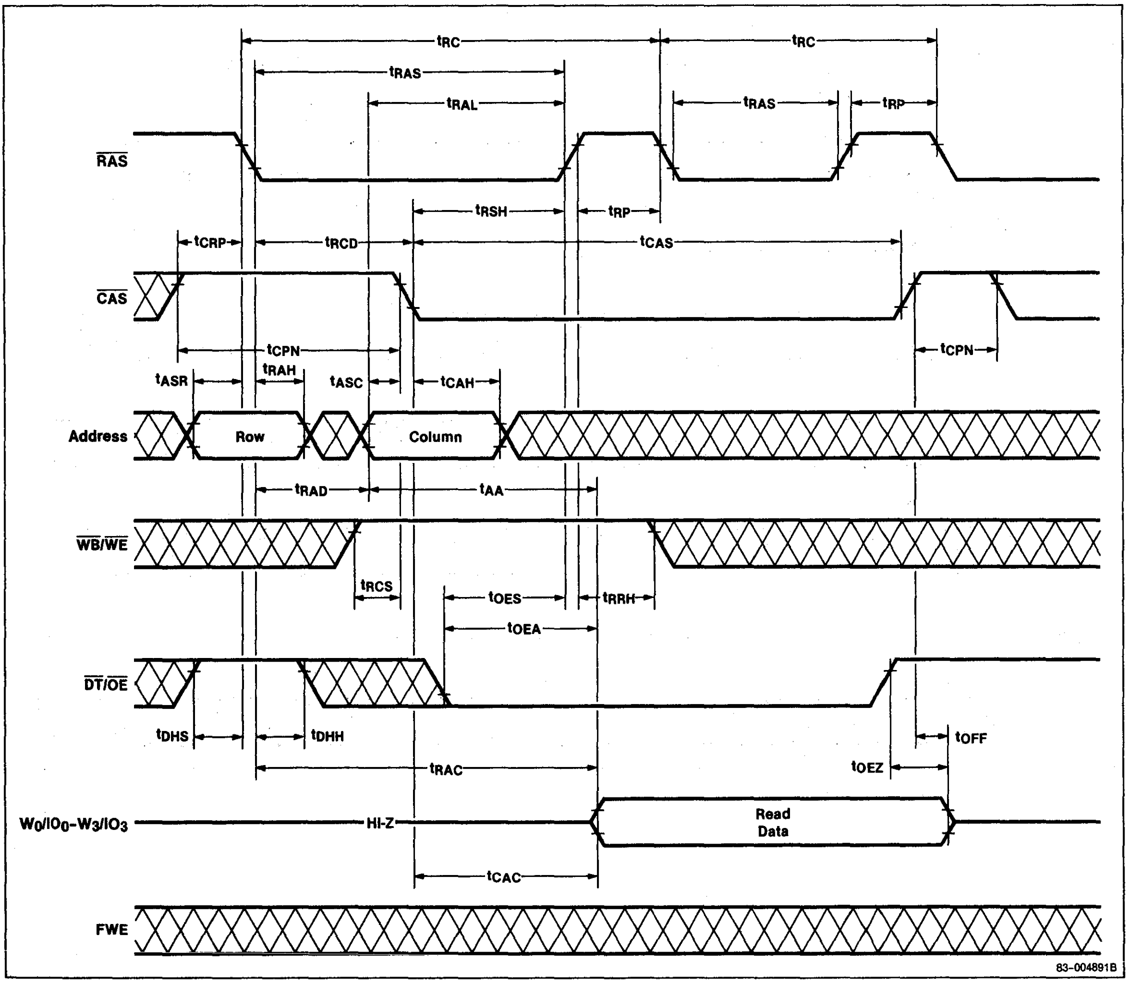
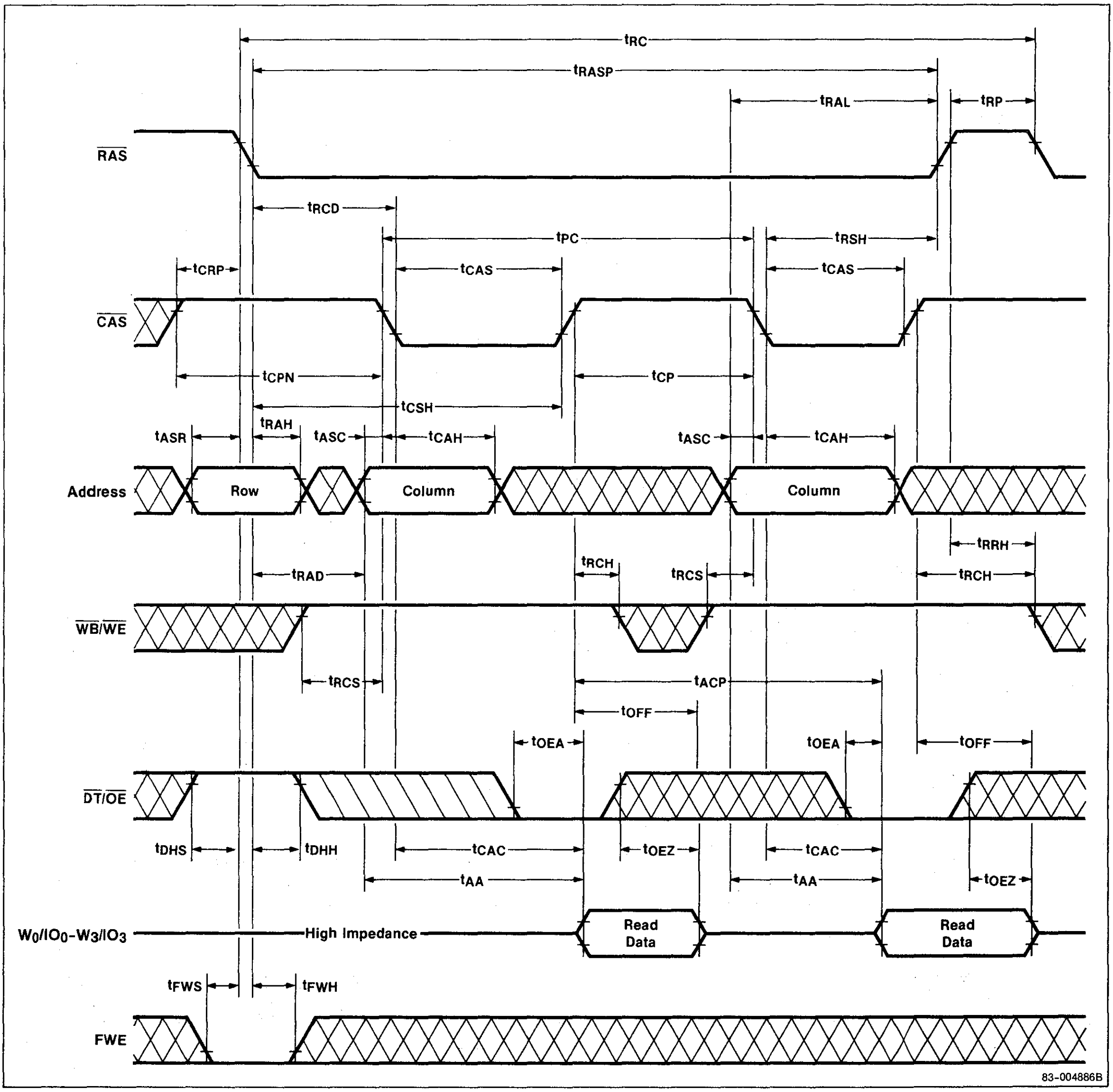
Timing Waveforms (cont)

Hidden Refresh



Timing Waveforms (cont)

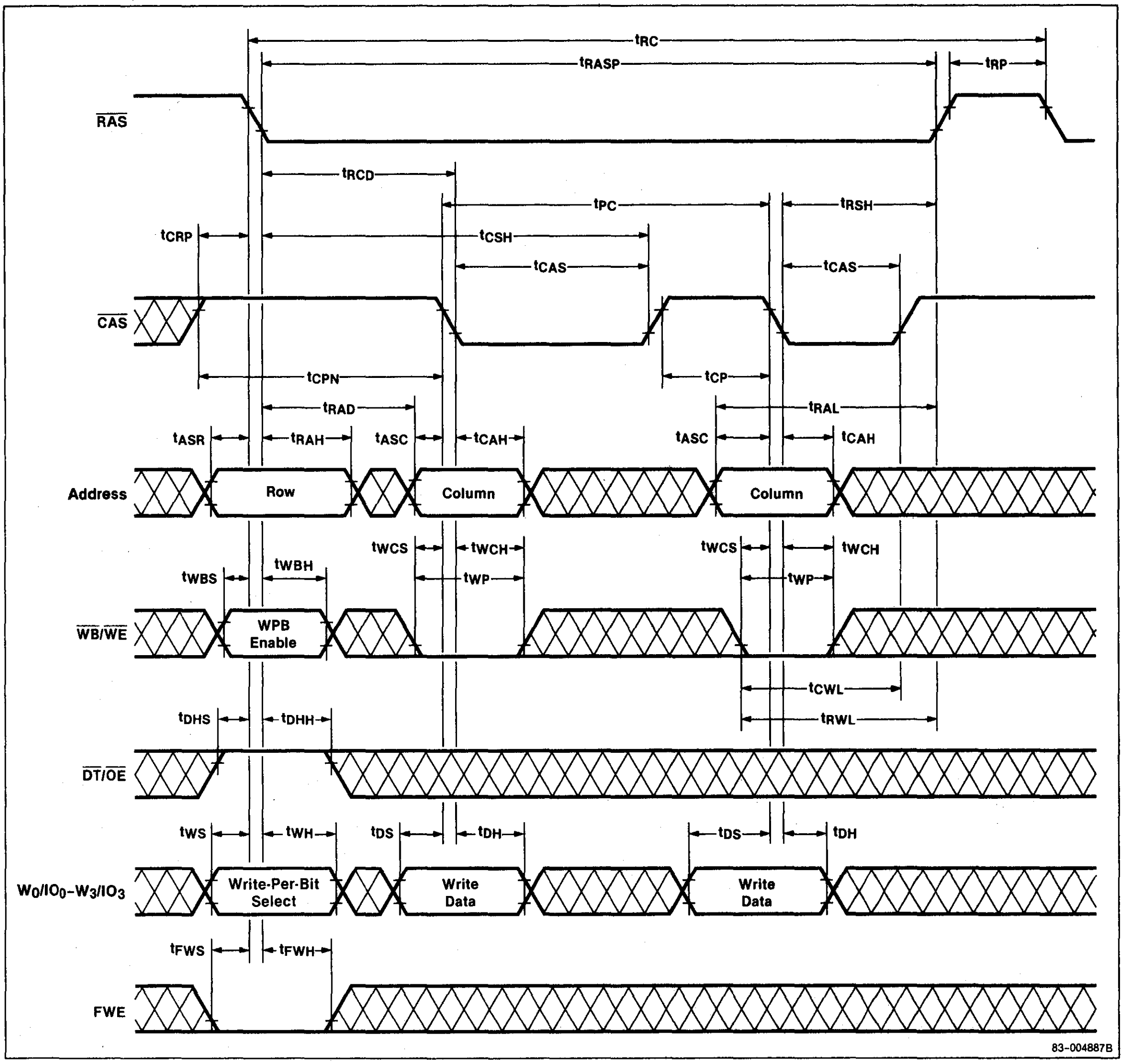
Fast-Page Read Cycle



3

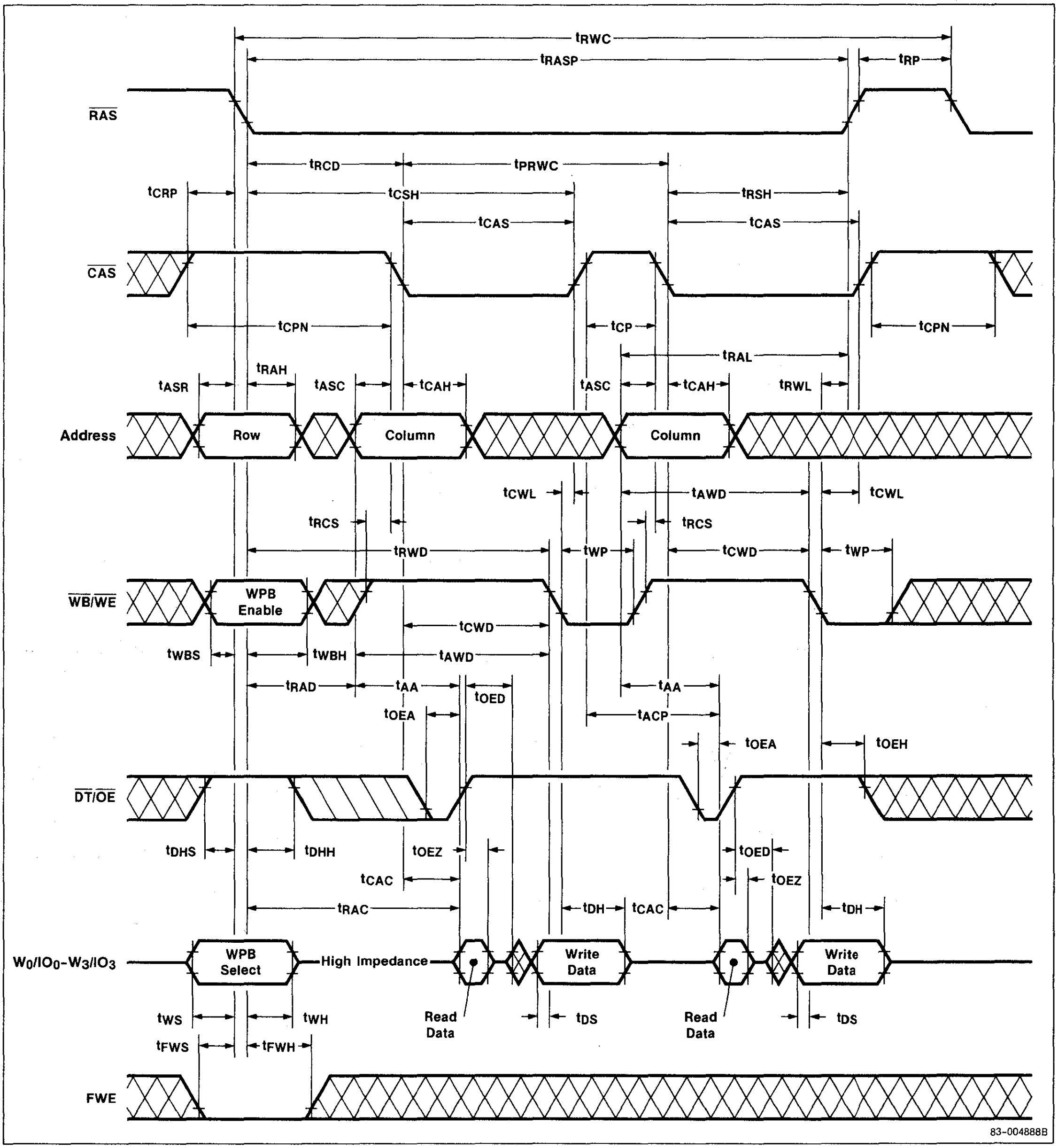
Timing Waveforms (cont)

Fast-Page Write Cycle



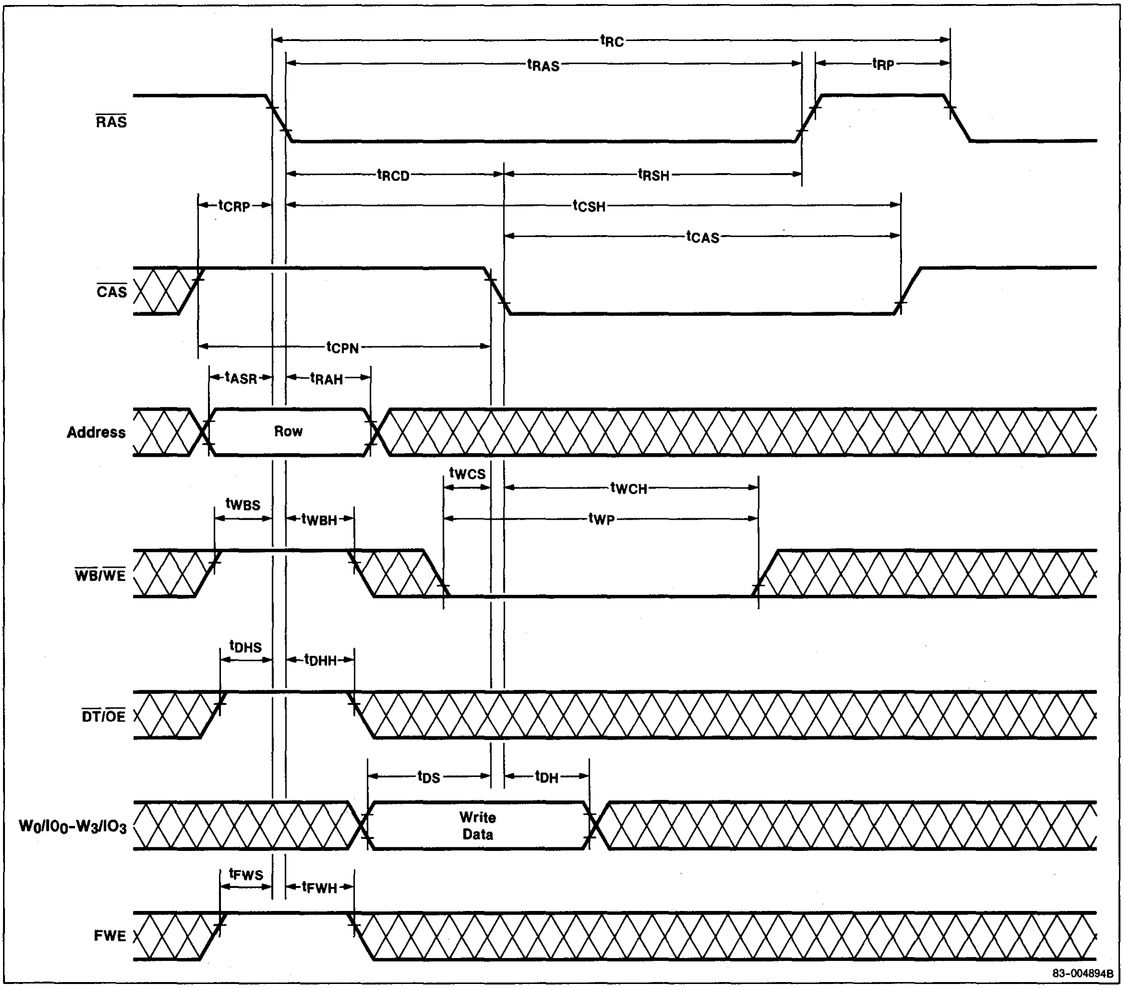
Timing Waveforms (cont)

Fast-Page Read-Modify-Write Cycle



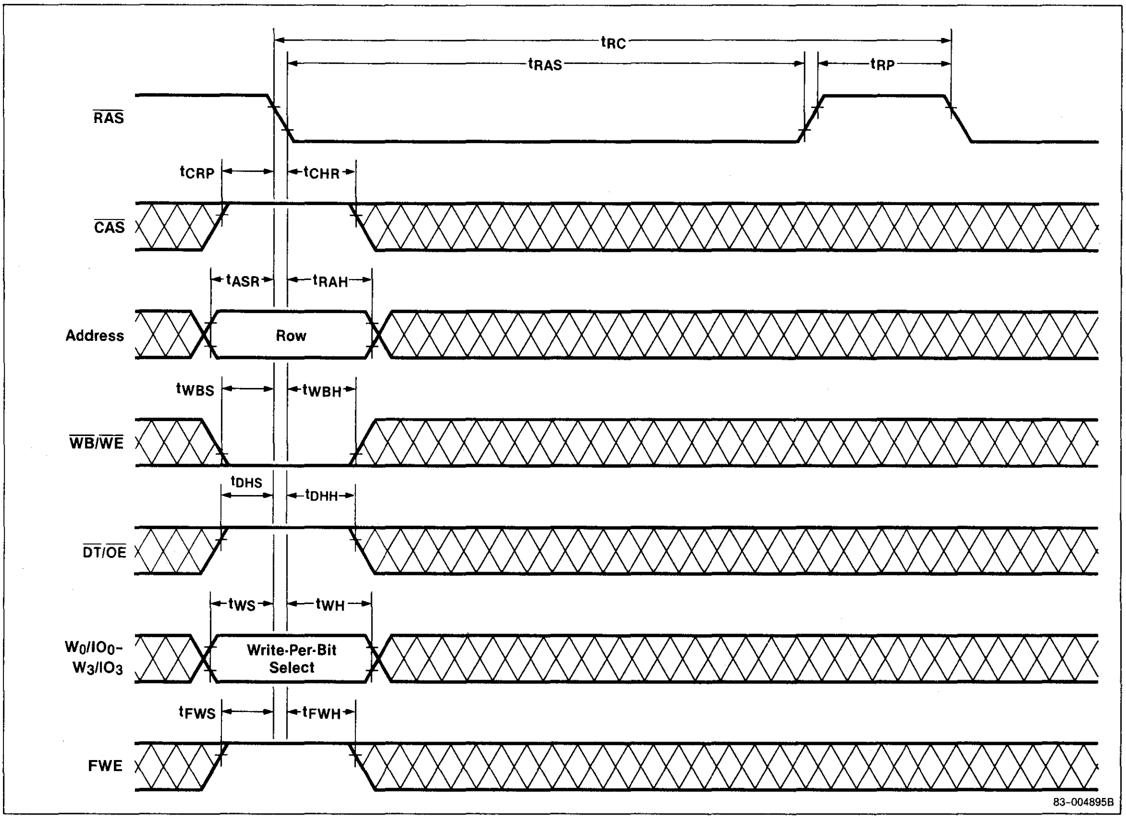
Timing Waveforms (cont)

Color Register Set Cycle



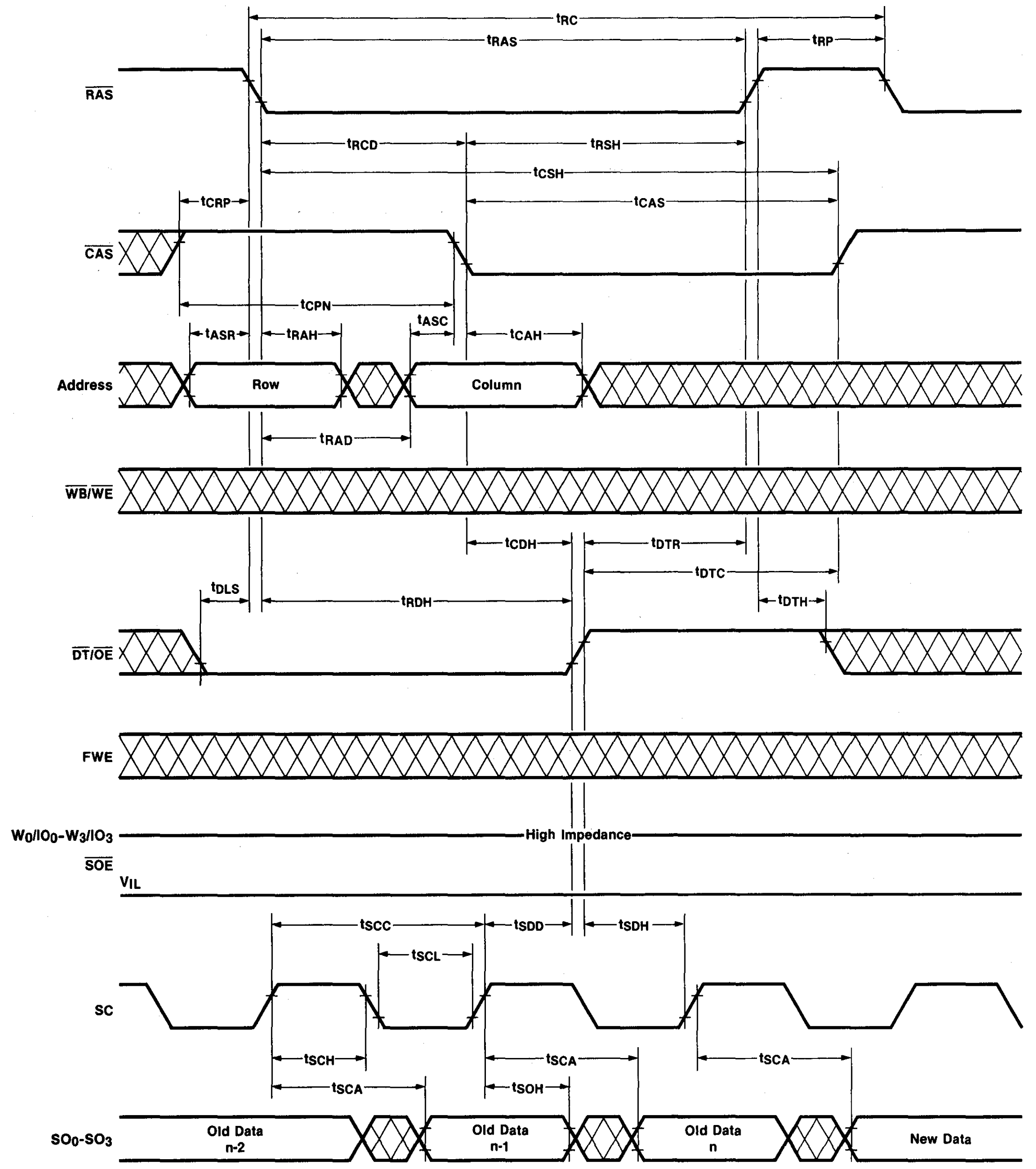
Timing Waveforms (cont)

Flash Write Cycle



Timing Waveforms (cont)

Data Transfer Cycle (Serial Port Active)



Notes:

[1] Refer to the Truth Table [Random Access Port] for details on the required input levels for WB/WE and FWE.

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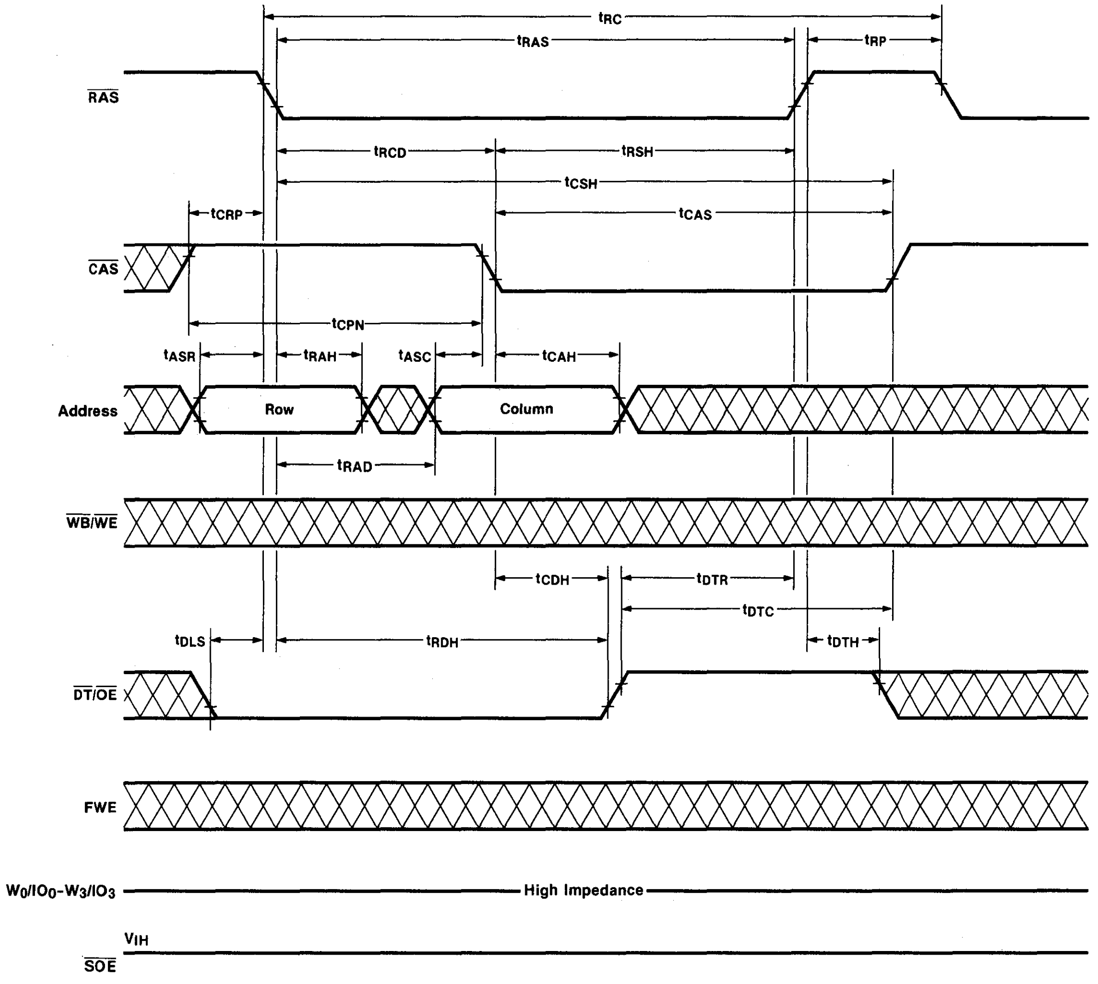
Timing Waveforms (cont)

Data Transfer Cycle (Serial Port Standby)



Notes:
[1] Refer to the Truth Table [Random Access Port] for details on the required input levels for WB/WE and FWE.

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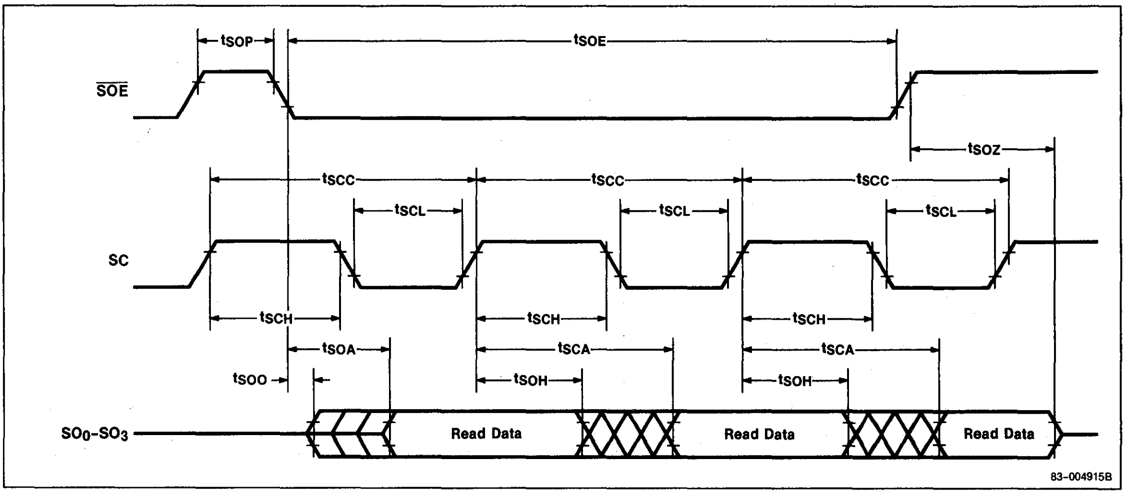
Timing Waveforms (cont)

Serial Read Cycle



NEC

NEC Electronics Inc.

µPD42505 5048 x 8-BIT CMOS LINE BUFFER FOR COMMUNICATIONS SYSTEMS

Description

The µPD42505 is a 5048-word by 8-bit dual-port line buffer fabricated with a silicon-gate CMOS process. The device is capable of asynchronous read and write operation at high speed, and can be used as a time axis converter or a digital delay line of up to 5048 bits (at maximum frequency, the minimum delay line length is 10 bits).

Applications include image processing in facsimile machines, plain paper copiers, video systems, and other optical scanners; time base correction in video playback systems; and data communication buffering in multiprocessor systems and local area networks.

Features

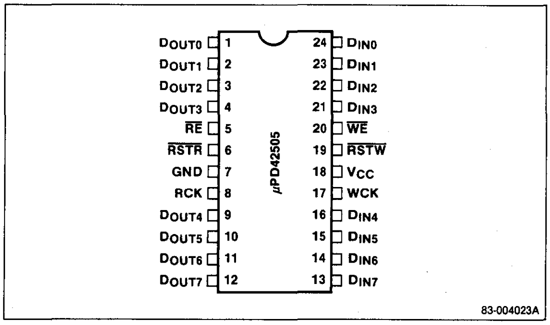
- ☐ 5048-word x 8-bit organization
- ☐ Dual-port operation
- ☐ Image processing and data communications systems applications
- ☐ Asynchronous and simultaneous read/write operation
- ☐ 1H (5048-bit) delay line capability
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt ± 10% power supply
- ☐ 300-mil, 24-pin plastic DIP and 400-mil, 28-pin plastic ZIP packaging

Ordering Information

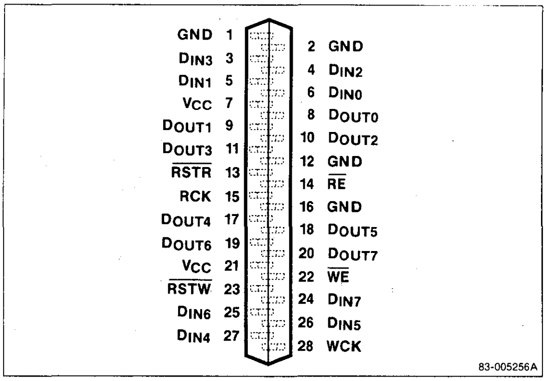
Device	Cycle Time (min)	Read Access Time (max)	Hold Time (min)	Package
µPD42505C-50	50 ns	40 ns	5 ms	24-pin plastic DIP
C-75	75 ns	55 ns	5 ms	
C-50H	50 ns	40 ns	20 ms	
C-75H	75 ns	55 ns	20 ms	
µPD42505V-50	50 ns	40 ns	5 ms	28-pin plastic ZIP
V-75	75 ns	55 ns	5 ms	
V-50H	50 ns	40 ns	20 ms	
V-75H	75 ns	55 ns	20 ms	

Pin Configurations

24-Pin Plastic DIP



28-Pin Plastic ZIP



Pin Identification

Symbol	Function
D_{IN0}-D_{IN7}	Write data inputs
D_{OUT0}-D_{OUT7}	Read data outputs
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RSTR}$	Read address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
$\overline{RSTW}$	Write address reset input
GND	Ground
V_{CC}	+5-volt power supply

3

Pin Functions

D_{IN0}-D_{IN7} [Data Inputs]

New data is entered on these pins.

D_{OUT0}-D_{OUT7} [Data Outputs]

These tri-state outputs are used to access the stored information. In a simple digital delay line application, a minimum delay of 10 clock cycles is required to move data from the data inputs to the data outputs.

RCK [Read Clock Input]

All read operations are performed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts the internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle, unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 5047 to 0 and begin increasing again.

$\overline{RE}$ [Read Enable Input]

This signal controls read operation. If $\overline{RE}$ is at a low level, all read cycles proceed. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{RSTR}$ [Read Address Reset Input]

Strobed by the rising edge of RCK, this signal resets the internal read address to 0.

$\overline{RSTW}$ [Write Address Reset Input]

Bringing this signal to a low level resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

WCK [Write Clock Input]

All write operations are performed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle, unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 5047 to 0 and begin increasing again.

$\overline{WE}$ [Write Enable Input]

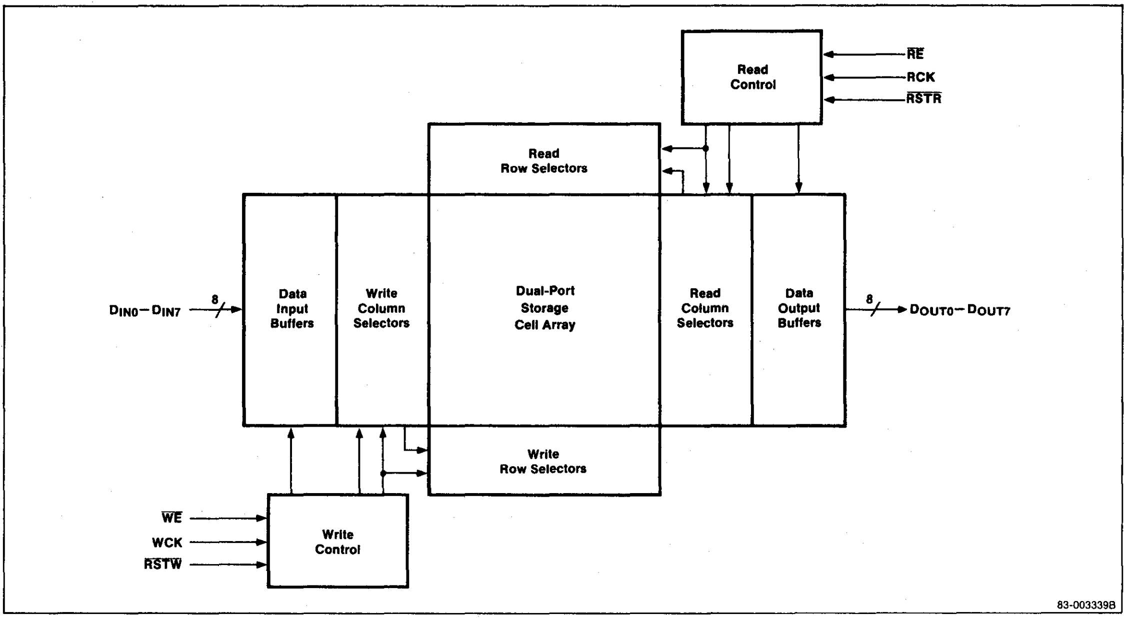
This input is similar to $\overline{RE}$ but controls write operation. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Operation

Reset Cycle

The μPD42505 requires the initialization of internal circuits using the $\overline{RSTW}/\overline{RSTR}$ reset signals before starting operation as a time axis converter or a digital delay line.

A reset cycle can be executed at any time and does not depend on the state of $\overline{RE}$ or $\overline{WE}$. However, $\overline{RSTW}$ and $\overline{RSTR}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

Write/Read Cycles

Write and read cycles are synchronized to their respective WCK/RCK inputs and executed individually when WCK or RCK is high and $\overline{WE}$ or $\overline{RE}$ is low. Write data must satisfy the setup and hold times as specified from the rising edge of WCK. New data written to a particular address is available for reading after 1/2 write cycle + 500 ns (maximum).

The access time of the read operation is measured from the rising edge of RCK, either by t_{ACR} for an access during the first cycle directly after a reset begins, or by t_{AC} for an access under other conditions. Stored data is read nondestructively; data can be repeatedly read within a prescribed time of 5 ms maximum (20 ms maximum for H versions).

Time Axis Conversion

In order to use the μPD42505 as a time axis converter, write and read cycles must be controlled independently. First, write/read ports are initialized separately using the reset signals. Then, write cycles are executed in synchronization with WCK and write data is stored sequentially from address 0 of this device. Afterward, when a read cycle is executed in synchronization with RCK, stored data can be read sequentially from address 0.

Since write and read cycles can be executed independently, data loaded at one arbitrary drive frequency can be read at another arbitrary drive frequency. In this sense, the μPD42505 functions as a time axis converter.

Digital Delay Line

The μPD42505 can easily be used as a digital delay line of 5,048 bits or less.

After initializing the internal circuits using simultaneous $\overline{RSTW}/\overline{RSTR}$ signals, write/read cycles are executed simultaneously by supplying the same pulse to the write clock (WCK) and read clock (RCK). The write data is always read after the full 5,048-bit delay if neither write nor read operation has been inhibited. This is the essential delay line function.

If either $\overline{WE}$ or $\overline{RE}$ is set at a nonselected (high) level for several cycles while the other is maintained in a selected (low) level, the delay line length can differ from 5,048 bits.

For example, if only $\overline{WE}$ is a set to a high level (write disable) for a small number of cycles, the read operation is performed continuously and the delay line length is large [see "(5048-m)-Bit Delay Line, No. 2" timing]. Alternatively, if only $\overline{RE}$ is set to a high level (read disable) for a small number of cycles, the write operation is performed continuously and the delay line length is small. Note that the minimum delay line length is 10 bits (for maximum frequency operation) and the maximum is 5,048 bits.

A data delay of 5,048 bits or less can also be obtained by applying the $\overline{RSTW}$ and $\overline{RSTR}$ signals at different times. For example, data is loaded for "m" cycles after $\overline{RSTW}$ and then this data is read after supplying $\overline{RSTR}$. In this case, since write data can be read from the beginning after a delay of "m" cycles, the device can be used as an "m-bit" digital delay line.

The $\overline{RSTW}/\overline{RSTR}$ reset signals can also be simultaneously loaded at every 1H (horizontal line) period. In this case, write data loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay line length ranging from 10 to 5,048 bits can be obtained according to the length of the reset signals supplied. Refer to the timing diagram for an "n-Bit Delay Line."

Recommended DC Operating Conditions

$T_A = -20$ to $+70°C$; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC}	V	
Input voltage, low	V_{IL}	−1.5		0.8	V	

Capacitance

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%; f = 1 MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0}-D_{IN7}
Output capacitance	C_O			7	pF	D_{OUT0}-D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

$T_A = -20$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			60	mA	
Input leakage current	I_I	−10		10	μA	$V_I = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; $V_O = 0$ to 5.5 V
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1$ mA
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 2$ mA

Notes:

(1) All voltages are referenced to GND.

AC Characteristics

T_A = −20 to +70°C; V_{CC} = 5.0 V ±10%

		Limits									
		μPD42505-50		μPD42505-75		μPD42505-50H		μPD42505-75H			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write clock cycle time	t_{WCK}	50	990	75	990	50	3960	75	3960	ns	
WCK pulse width	t_{WCW}	20		30		20		30		ns	
WCK precharge time	t_{WCP}	20		30		20		30		ns	
Read clock cycle time	t_{RCK}	50	990	75	990	50	3960	75	3960	ns	
RCK pulse width	t_{RCW}	20		30		20		30		ns	
RCK precharge time	t_{RCP}	20		30		20		30		ns	
Access time	t_{AC}		40		55		40		55	ns	
Access time after a reset cycle	t_{ACR}		40		55		40		55	ns	
Output hold time	t_{OH}	5		5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		5		ns	(Note 7)
Output active time	t_{LZ}	5	40	5	55	5	40	5	55	ns	(Note 4)
Output disable time	t_{HZ}	5	40	5	55	5	40	5	55	ns	(Note 4)
Data-in setup time	t_{DS}	15		20		15		20		ns	
Data-in hold time	t_{DH}	5		5		5		5		ns	
Reset active setup time	t_{RS}	15		20		15		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		5		ns	(Note 8)
Reset inactive hold time	t_{RN1}	5		5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	15		20		15		20		ns	(Note 9)
Write enable setup time	t_{WES}	15		20		15		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		5		ns	(Note 10)
Write enable high delay from WCK	t_{WEN1}	5		5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	15		20		15		20		ns	(Note 11)
Read enable setup time	t_{RES}	15		20		15		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		5		ns	(Note 10)
Read enable high delay from RCK	t_{REN1}	5		5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	15		20		15		20		ns	(Note 11)
Write disable pulse width	t_{WEW}	0		0		0		0		ms	(Note 6)
Read disable pulse width	t_{REW}	0		0		0		0		ms	(Note 6)
Write reset time	t_{RSTW}	0		0		0		0		ms	(Note 6)
Read reset time	t_{RSTR}	0		0		0		0		ms	(Note 6)
Transition time	t_T	3	35	3	35	3	35	3	35	ns	

AC Characteristics (cont)

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ± 200 mv from the steady state voltage with the load specified in figure 2. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the next equations in one line cycle operation:
$t_{WEW} + t_{RSTW} + 5048t_{WCK} \leq 5$ ms (20 ms for H versions)
$t_{REW} + t_{RSTR} + 5048t_{RCK} \leq 5$ ms (20 ms for H versions)

(7) This parameter applies when $t_{RCK} \geq t_{ACR}$ (max).

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 1. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

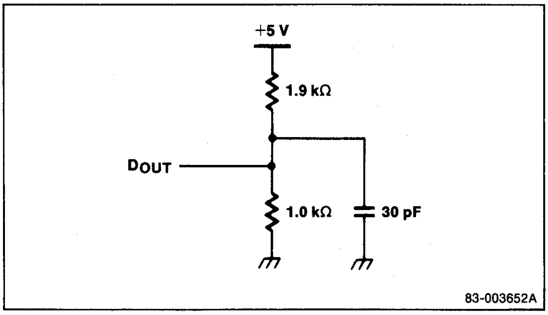
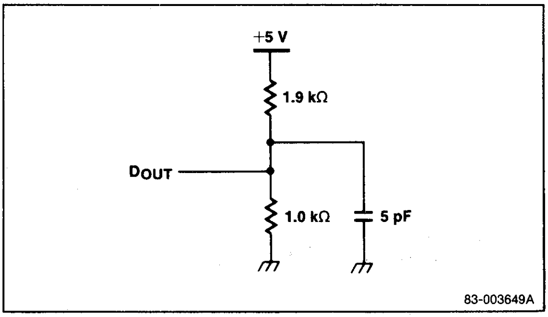
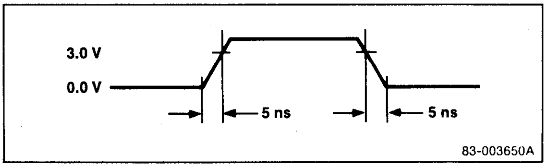


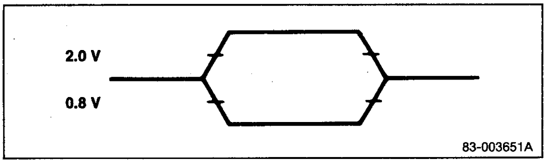
Figure 2. Output Load for t_{LZ} and t_{HZ}



AC Input Timing Reference Waveform



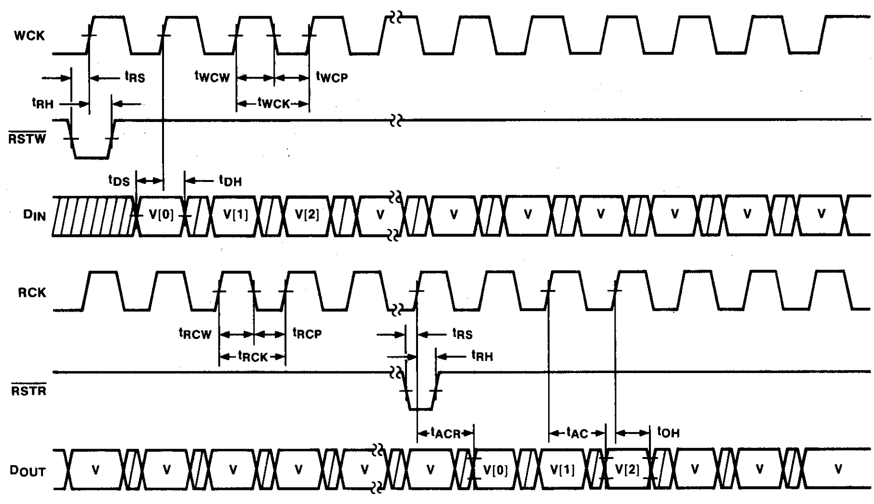
AC Output Timing Reference Waveform



3

Timing Waveforms

Time Axis Conversion



Notes:

[1] $\overline{WE} = \overline{RE} = V_{IL}$.

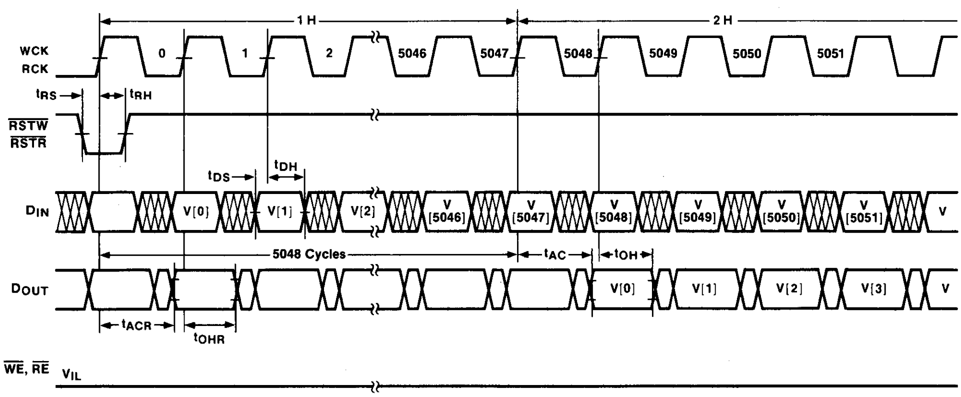
[2] V = valid data.

[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-004024B

5048-Bit Delay Line



Notes:

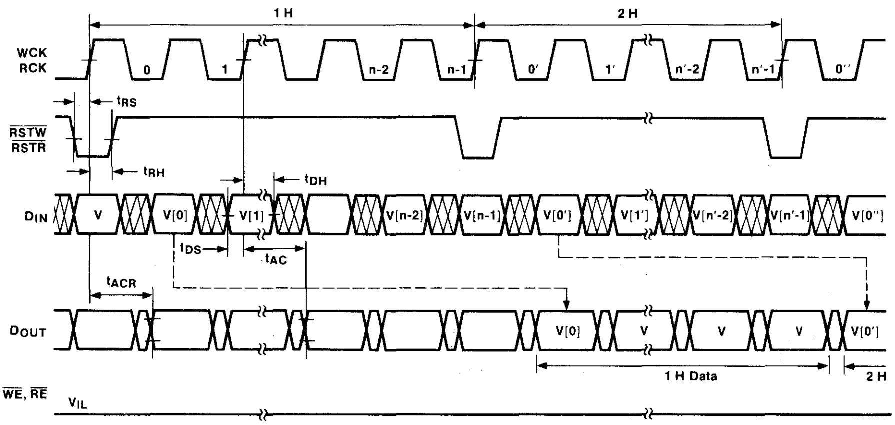
[1] V = valid data.

[2] 1H = the first group of 5048 bits.
2H = the second group of 5048 bits.

83-004025B

Timing Waveforms (cont)

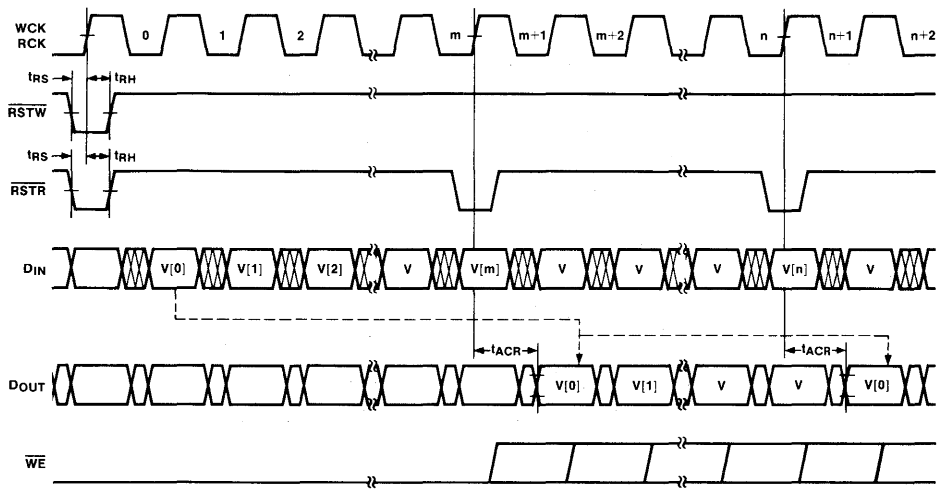
n-Bit Delay Line



Notes:
[1] V = valid data.
[2] 1H = the first group of "n" bits.
2H = the second group of "n" bits.

83-003643B

Re-Read Operation



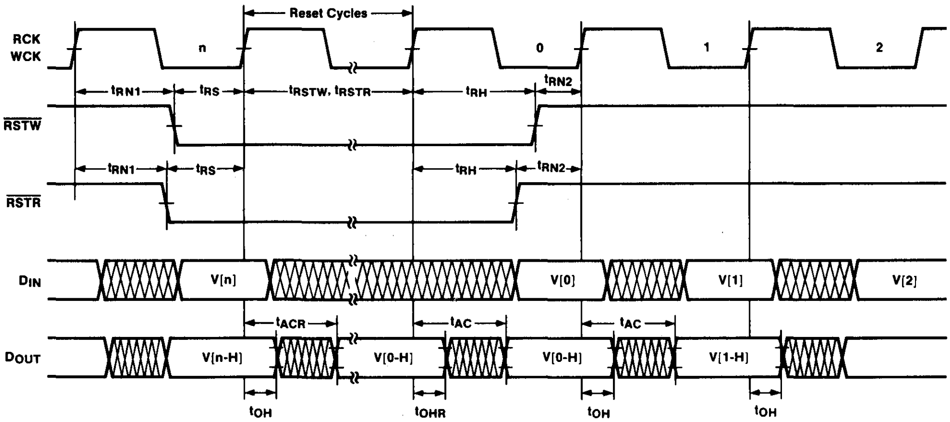
Notes:
[1] RE = V_{IL}.
[2] V = valid data.
[3] The data stored in any location can be re-read as many times as desired within a period of 5 ms following the writing of data into that location, provided that a second write operation has not re-written new data into that location.

83-004029B

3

Timing Waveforms (cont)

Read or Write Reset



Notes:

[1] $\overline{WE} = \overline{RE} = V_{IL}$ above to show the relationship of reset cycles to the reading and writing of data [D_{OUT} and D_{IN}]. If reading and writing are not needed during reset, then $\overline{WE} = \overline{RE}$ = don't care.

[2] V = valid data.

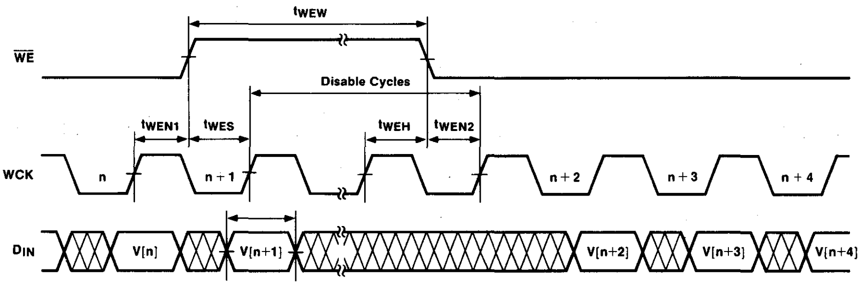
[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 5048 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83-004030B

Write Disable



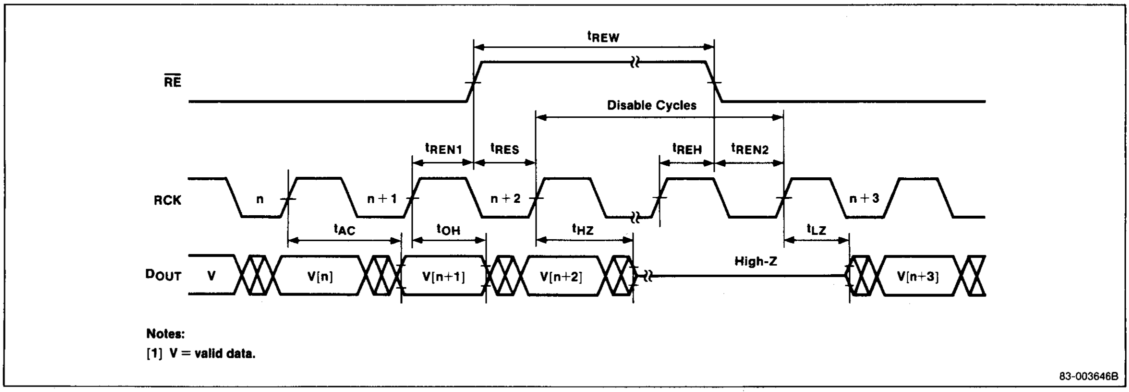
Notes:

[1] V = valid data.

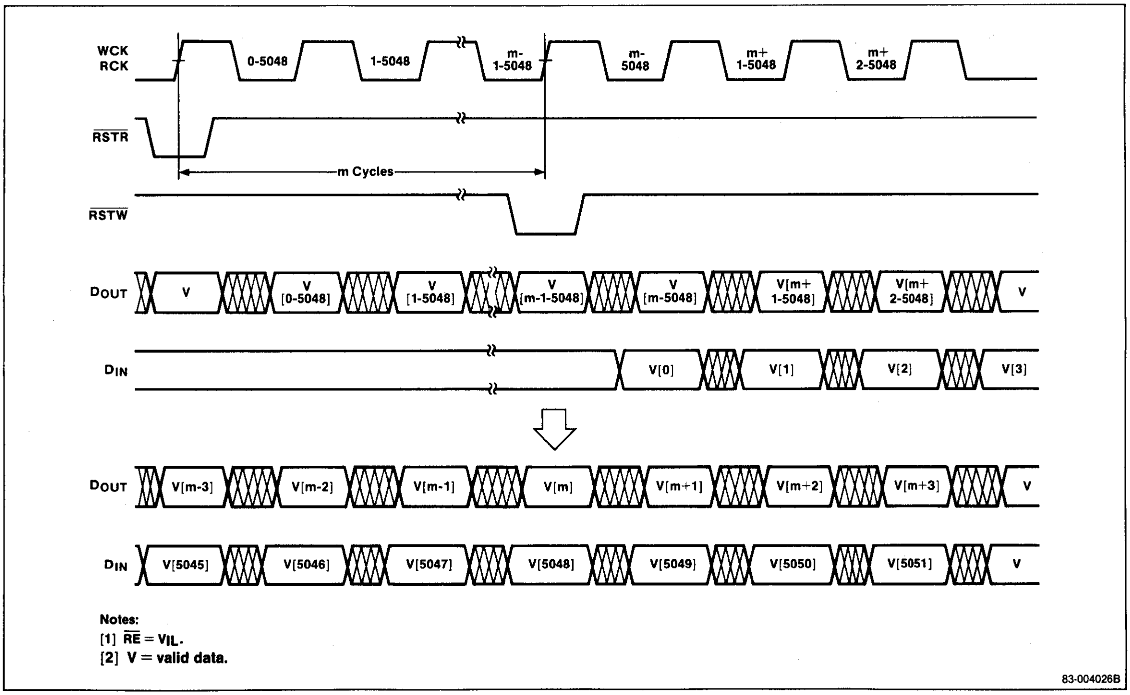
83-003723B

Timing Waveforms (cont)

Read Disable



(5048-m)-Bit Delay Line, No. 1



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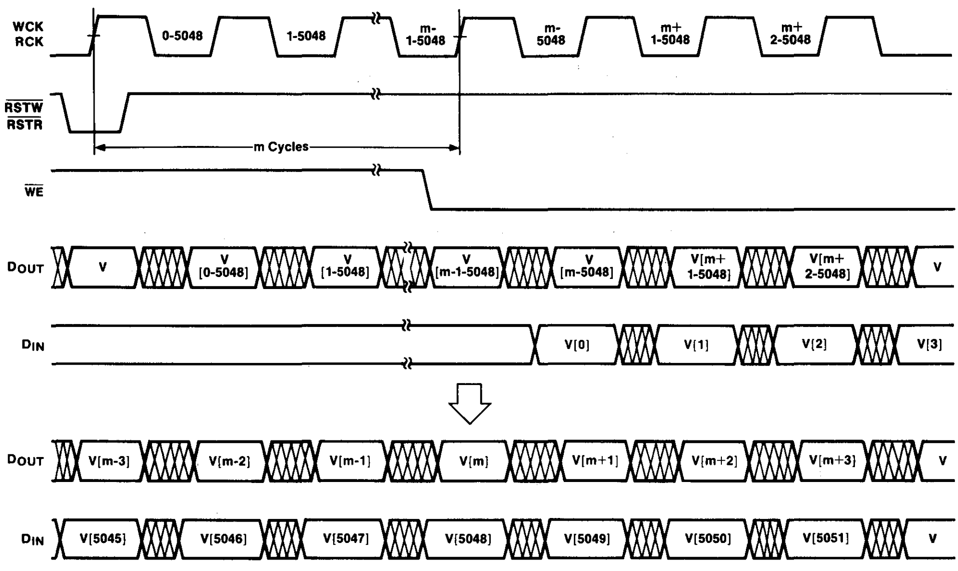
NEC

Timing Waveforms (cont)

(5048-m)-Bit Delay Line, No. 2



Notes:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

83-004027B

NEC
NEC Electronics Inc.

μPD42532 32,768 x 8-BIT BIDIRECTIONAL DATA BUFFER

PRELIMINARY INFORMATION

Description

The μPD42532 bidirectional data buffer features 32,768-word by 8-bit organization and CMOS dynamic circuitry that provides for high-speed, asynchronous, simultaneous write and read operation at a minimum cycle time of 100 ns. Two sets of write and read registers between the I/O pins and the storage cells enable all data to be parallel-transmitted as a single register group when the registers are either full or empty. The device's main application is data transmission between devices having different processing speeds, such as between a central processor and a disk.

Automatic refreshing by means of an internal capability is performed regularly for the μPD42532—without any influence on write and read operation. A built-in arbitration circuit performs each required read, write, or refresh operation sequentially (even if transparent refreshing overlaps with the transmission of data) to simplify the device's external timing requirements.

The μPD42532 operates from a single +5-volt power supply and is packaged in a 600-mil, 40-pin plastic DIP. Four FLAG pins, plus $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins, are provided to monitor the amount of data accumulated in storage.

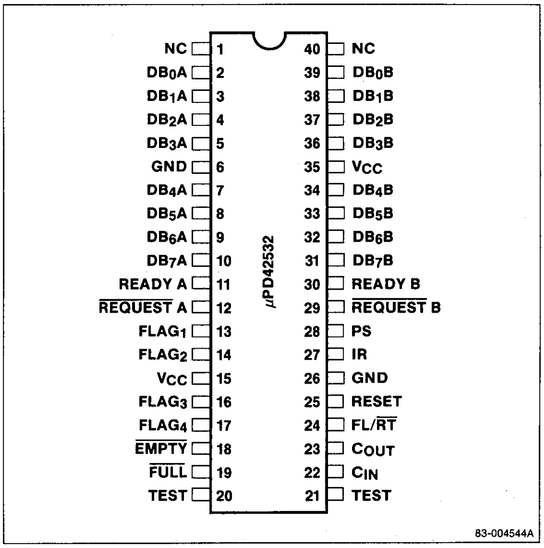
The μPD42532 is capable of bidirectional input/output by means of a port select function. Input and output pins are also supplied for cascade connection. Cascade connection allows any number of μPD42532s to be linked together so as to expand word width and length without limit.

Features

- ☐ 32,768-word by 8-bit organization
- ☐ CMOS technology
- ☐ Single +5-volt power supply
- ☐ Independent, asynchronous write/read operation
- ☐ Bidirectional transmission of input and output data (exchange of port functions)
- ☐ Automatic, regular refreshing
- ☐ Internal addressing
- ☐ Flag pin monitoring of accumulated data
- ☐ Unlimited expansion of word width and depth (cascade connection)
- ☐ Retransmit (re-read) function
- ☐ High-speed operation
  - — Access time: 50 ns maximum
  - — Cycle time: 100 ns minimum
- ☐ 600-mil, 40-pin plastic DIP packaging

Pin Configuration

40-Pin Plastic DIP



Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42532C-10	50 ns	100 ns	40-pin plastic DIP

Pin Identification

Symbol	Function
DB_0A-DB_7A	Port A input/output data buses
DB_0B-DB_7B	Port B input/output data buses
RESET	Reset input
$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B	Port A/Port B request input
READY A/READY B	Port A/Port B ready output
$\overline{\text{EMPTY}}$	Empty output
$FLAG_1$-$FLAG_4$	Flag outputs
$\overline{\text{FULL}}$	Full output
PS	Write/read port select input
IR	Interrupt read request input
FL/$\overline{\text{RT}}$	First load/retransmit input
C_{IN}	Cascade connection input
C_{OUT}	Cascade connection output
TEST	Test pin (connect to GND in system)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Functions

DB_0A-DB_7A/DB_0B-DB_7B. These pins function as 8-bit data buses for write input or read output depending on the status of the PS pin. The output drivers are three-state outputs.

RESET. This pin initializes the internal counters and pointers.

$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. To initiate a write or read cycle, the signal goes low for the respective port (if READY A or READY B is low, the corresponding $\overline{\text{REQUEST}}$ input is ignored internally). These pins can be connected to the WR and RD pins of a CPU.

READY A/READY B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. When a write or read cycle is possible, the READY signal is high for the respective port. These pins can be connected to the READY pins of a CPU or DMA controller.

$\overline{\text{EMPTY}}$. The signal from this pin is low whenever the amount of data accumulated is exactly 0 bytes, and high in all other cases.

$FLAG_1$-$FLAG_4$. These pins reflect the amount of data accumulated in the storage array. By combining the output signals, it is possible to monitor (in 2K byte steps) data quantities of up to 32K bytes.

$\overline{\text{FULL}}$. The signal from this pin is low when the storage cells are full of accumulated data, and high in all other cases.

PS. This pin is used to specify the direction of data transfer. When PS is high, Port A serves as the write port and Port B as the read port. When PS is low, the functions of the two ports are reversed.

IR. If the data accumulated in storage is less than 64 bytes (i.e., one register's capacity), the READY signal for the read port goes low to inhibit reading. However, forcing IR high makes it possible to read all stored data.

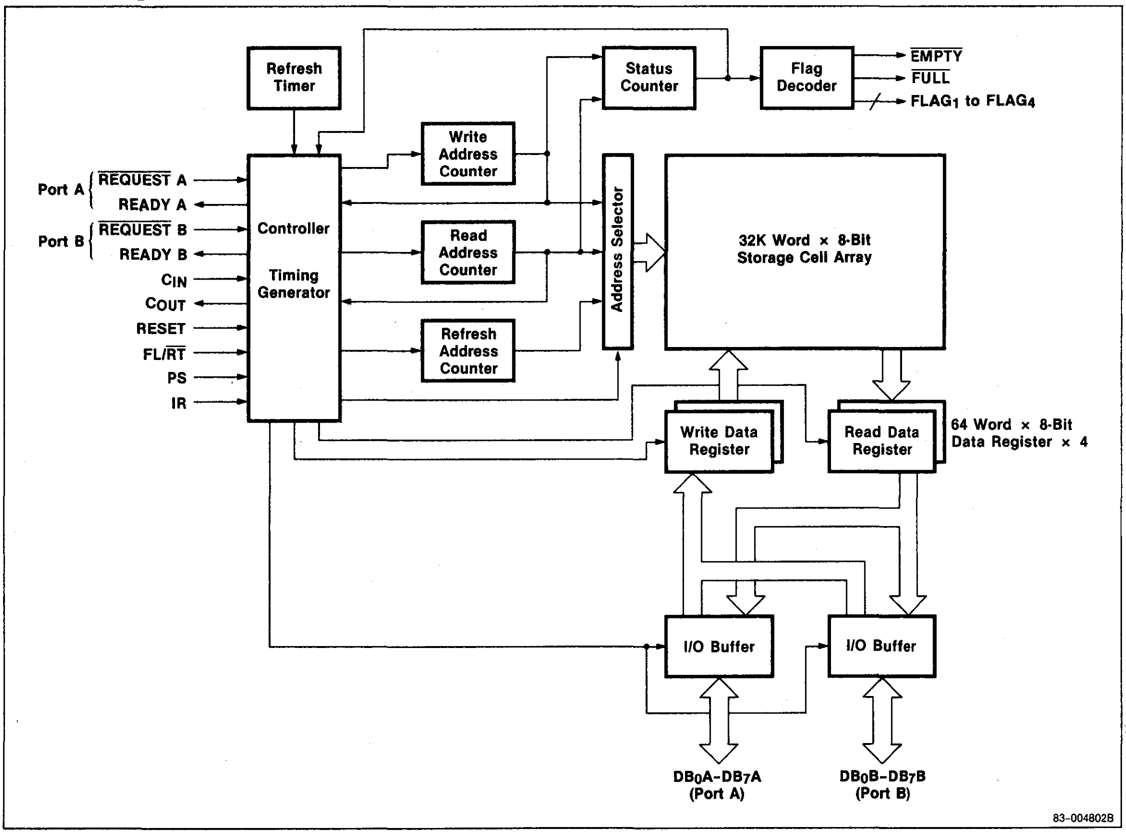
Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, all remaining data must be read using the interrupt read option.

FL/$\overline{\text{RT}}$. This pin designates the lead device when multiple devices are cascade connected. It is high only for that device and low for all others. If the device is not cascaded, a low FL/$\overline{\text{RT}}$ controls the retransmit (re-read) function; other than during retransmission, FL/$\overline{\text{RT}}$ must be high.

C_{IN}. This pin is used to expand word depth and is connected to the C_{OUT} pin of the device preceding it in cascade connections. If word depth is not expanded, C_{IN} is connected to C_{OUT} of the same device.

C_{OUT}. This pin is used to expand word depth and is connected to the C_{IN} pin of the device following it in cascade connections. If word depth is not expanded, C_{OUT} is connected to C_{IN} of the same device.

Block Diagram



Operation

Reset Cycle

After power is applied to the μPD42532, it is necessary to clear the internal counters and initialize the write and read address pointers by executing a reset cycle. A reset cycle can be executed at any time by setting the RESET pin to a high logic level. However, once this cycle is initiated, RESET, $\overline{\text{REQUEST}}$, and FL/$\overline{\text{RT}}$ must be kept high for a minimum time of t_{SW} before the RESET signal goes low again (see waveform for "Reset Cycle"). The RESET, $\overline{\text{REQUEST}}$, and FL/$\overline{\text{RT}}$ signals are all high at the start of a reset, except in cascade connections, in which case a high FL/$\overline{\text{RT}}$ is required only in the first stage.

After a reset, the READY signal for the write port, READY (W), is driven high to prepare for a write cycle. Subsequently, the $\overline{\text{REQUEST}}$ signal for the write port, $\overline{\text{REQUEST}}$ (W), can be set low to commence writing.

A standard read cycle can be executed once data written to one of the 64-byte registers has filled that register and been transferred to the storage cells. The READY signal for the read port, READY (R), goes high to prepare for the cycle. Subsequently, the $\overline{\text{REQUEST}}$ signal for the read port, $\overline{\text{REQUEST}}$ (R), can be set low to commence reading.

Write Cycle

In a write cycle, data is written to one of two 64-byte write registers before being transferred to the storage cells. Whenever 64 bytes have been written into one register, write operation automatically shifts to the other and the contents of the first are transferred to storage. High-speed write cycles are thus executed continuously by alternating registers repeatedly. Write data must satisfy the requirements for setup and hold times as measured against the rising edge of $\overline{\text{REQUEST}}$ (W) [see waveform for "Write Cycle"].

A write cycle can be initiated any time READY (W) is high by setting $\overline{\text{REQUEST}}$ (W) low. To allow a write cycle to be executed in one port even while the other port may be executing a read cycle, READY (W) is always high after a reset, except in the following cases:

- Whenever the storage cells are full of accumulated data
- While the device is executing a forced read cycle (see **Interrupt Read Cycle**)
- When a retransmit operation is being performed (see **Retransmit Cycle**)

While READY (W) is off, the $\overline{\text{REQUEST}}$ (W) signal is ignored internally and no write cycle is executed.

Figure 1. Write Register Operation

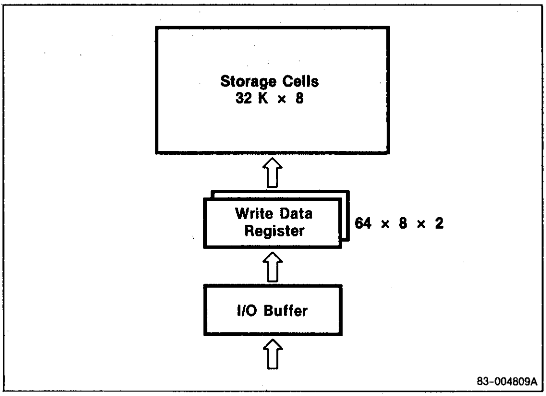
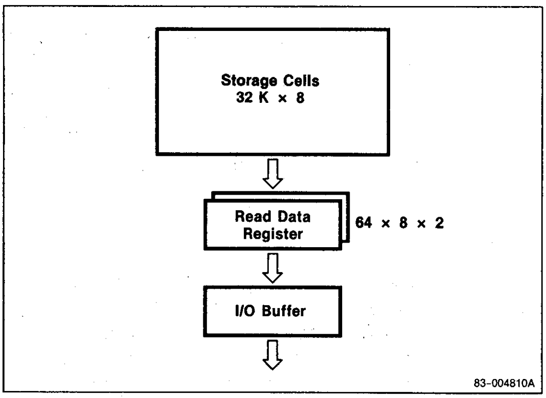


Figure 2. Read Register Operation



Read Cycle

In a read cycle, data is not read directly from the storage cells but rather from one of two 64-byte read registers. After 64 bytes of data have been read from one register, read operation automatically shifts to the other and the contents of the first are subsequently replaced by data from the storage cells. High-speed read cycles are thus executed continuously by alternating registers repeatedly.

Data is output after a maximum access time of t_{AC}, measured from the falling edge of $\overline{\text{REQUEST}}$ (R). When $\overline{\text{REQUEST}}$ (R) is high or READY (R) is low, the outputs are in a state of high impedance (see waveform for "Read Cycle").

A standard read cycle can be initiated any time READY (R) is high by setting $\overline{\text{REQUEST}}$ (R) low. To allow a read cycle to be executed in one port even while the other port may be executing a write cycle, the READY (R) signal is always high, except in the following cases:

- Whenever the data accumulated is less than 64 bytes
- While a retransmit operation is being performed (see **Retransmit Cycle**).

While READY (R) is low, $\overline{\text{REQUEST}}$ (R) is ignored internally and no read cycle is executed.

Flags

The μPD42532 supplies signals from the $\overline{\text{EMPTY}}$ pin, the $\overline{\text{FULL}}$ pin, and the four FLAG pins to indicate the amount of stored data in units of approximately 2K bytes. Accumulated data is reflected as the difference between the write address counter and the read address counter. Thus, if a total of 16K bytes have been read while 32K bytes have been written since the most recent reset, the amount of data in storage is 16K bytes.

The $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins are used to prevent overwriting and overreading. To control write operation on data units of register length (64 bytes), the $\overline{\text{FULL}}$ pin outputs a low signal when stored data reaches the 32,705- to 32,768-byte range. Whenever write cycles are executed continuously and the storage cells become full, $\overline{\text{REQUEST}}$ (W) is ignored and the signals of $\overline{\text{FULL}}$ and READY (W) are driven low to inhibit writing. Meanwhile if read cycles are executed and the data decreases to 32,704 bytes or less, READY (W) goes high again to enable write operation.

The $\overline{\text{EMPTY}}$ pin goes low whenever stored data is exactly 0 bytes. Since standard read cycles cannot be executed if the quantity of data drops below 64 bytes, READY (R) goes low to inhibit read operation. Whenever write cycles are executed and stored data increases to 64 bytes or more, READY (R) goes high again to enable read operation.

The status of the FLAG pins depends on the internal status of the write and read address counters. These counters are incremented as data is transferred to or from the storage array. Since the logic levels of the FLAG pins reflect movement of blocks of data on a 64-byte-register basis rather than on a single-byte basis, the status indicated by these pins can be in error by a maximum of 255 bytes with respect to the actual amount of data accumulated [i.e., the sum of the write register (63 bytes), the read registers (128 bytes), and the 64 bytes currently being transferred]. This discrepancy means that two adjacent ranges of stored data, as indicated by the FLAGs, can overlap by up to 191 bytes.

The following table shows the combination of signals output from these pins.

Table 1. Stored Data as Indicated by Flag Pins

Amount of Stored Data (bytes)	$\overline{\text{FULL}}$	$\overline{\text{EMPTY}}$	FLAG 1	FLAG 2	FLAG 3	FLAG 4
32705 to 32768	0	1	1	1	1	1
30721 to 32767	1	1	1	1	1	1
28673 to 30911	1	1	0	1	1	1
26625 to 28863	1	1	1	0	1	1
24577 to 26815	1	1	0	0	1	1
22529 to 24767	1	1	1	1	0	1
20481 to 22719	1	1	0	1	0	1
18433 to 20671	1	1	1	0	0	1
16385 to 18623	1	1	0	0	0	1
14337 to 16575	1	1	1	1	1	0
12289 to 14527	1	1	0	1	1	0
10241 to 12479	1	1	1	0	1	0
8193 to 10431	1	1	0	0	1	0
6145 to 8383	1	1	1	1	0	0
4097 to 6335	1	1	0	1	0	0
2049 to 4287	1	1	1	0	0	0
1 to 2239	1	1	0	0	0	0
0	1	0	0	0	0	0

Notes:

(1) 1 = high level

(2) 0 = low level

Interrupt Read Cycle

Whenever the amount of stored data drops below 64 bytes (i.e., one register's capacity), or 2K bytes for devices with process code K, READY (R) is driven low to inhibit reading. Any data remaining in a write register can only be read by means of an interrupt (or forced) read cycle.

An interrupt read cycle can be executed by forcing the IR pin high. At this point, data is transferred from the write register to one of the read registers via the storage array, and write operation is disabled until all stored data has been read. If this cycle is initiated after READY (R) goes low, read operation will be delayed until all data has been transferred to one of the read registers.

Once the device completes reading of its last address, the $\overline{\text{EMPTY}}$ and READY (R) signals are driven low and READY (W) goes high to enable write operation again (unless a retransmit cycle has been requested). Read cycles will be executed only after 64 bytes or more have been written and transferred to storage.

Retransmit Cycle

The μPD42532 will execute a retransmit cycle whenever a low-level pulse is applied to $\overline{\text{RT}}$. A retransmit cycle initializes the read address counter to starting address 0. Although retransmission can be executed at any time, $\overline{\text{REQUEST}}$ (W) and $\overline{\text{REQUEST}}$ (R) must be high before and after the low $\overline{\text{RT}}$ signal is applied.

During this cycle, the READY signals are pulsed low to temporarily inhibit writing and reading, and the FLAG and $\overline{\text{EMPTY}}$ signals vary in accordance with the amount of data in storage. After READY (W) goes high again, the retransmit preparation cycle is complete. Write operation can resume after an extra delay to ensure stability of the FLAG and $\overline{\text{EMPTY}}$ pins. If an interrupt read signal is applied during retransmission, the interrupt read cycle is executed after termination of the retransmit cycle.

The retransmit function is only useful in systems where less than 32K bytes of data are written between resets. If a retransmit cycle is executed after more than 32K bytes are written, old data cannot be retransmitted.

Since the $\overline{\text{RT}}$ pin is multiplexed as the first load (FL) pin in cascade connections, cascaded devices cannot be used for retransmission. In single-device configuration, this pin is always high except during a retransmit cycle.

Port Select Function

The μPD42532 is able to change the direction of data transfer according to the logical level of the signal applied to the PS pin. When a high-level input is applied to PS, Port A becomes the write port and Port B the read port. When PS is low, the functions of the two ports are reversed. While port functions are being assigned, the $\overline{\text{REQUEST}}$ signals must be kept high.

Since register and storage cell data are preserved during port selection, data written to a particular port can also be read from that same port.

Cascade Connection

The μPD42532 can be used in a single-device, 32K by 8-bit configuration or it can be cascade connected by means of the C_{IN} and C_{OUT} pins to allow unlimited expansion of word width and length.

Single-Device Configuration. When using the μPD42532 as a single 32K by 8-bit data buffer, connect C_{OUT} to C_{IN} and set the FL pin to a high logic level (see figure 3).

Expanded Word Width. When using multiple devices to expand word width, connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals. Each C_{OUT} pin should be connected to its own C_{IN} pin (as in the single-device configuration) and a high-level input applied to each FL. The flag pins of a single μPD42532 can be used to represent the entire system (see figure 4).

Expanded Word Length. When using multiple devices to expand word length, set a high-level input to FL of the lead μPD42532 and a low-level input to FL of all the others. Each C_{OUT} pin should be connected to C_{IN} of the device following it; C_{OUT} on the last device should be connected to C_{IN} of the lead device. Connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals.

The $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY pins of each device, respectively, can be ORed together by external logic. 'OR' outputs are composite $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY signals for all data buffers (see figure 5).

Operation. To enable operation of μPD42532s in cascade connection, set the RESET signal(s) high to clear the internal counters and initialize the write and read address pointers. When the reset is complete, start writing to the lead device. While data is being written to the first, all other devices output low READY signals and ignore the $\overline{\text{REQUEST}}$ signals. When write operation in the first μPD42532 (n) reaches the last address, its C_{OUT} pin outputs a high-level signal and forces C_{IN} of the next device high. Write operation shifts to the next device in succession (n + 1). The READY (W) signal of the first device (n) is driven low, and the READY (W) signal of the succeeding device (n + 1) goes high.

If only write cycles are being executed, each data buffer outputs a low $\overline{\text{FULL}}$ signal as writing is completed for that device. At the point where the last device finishes writing to its last address, all μPD42532s output low-level $\overline{\text{FULL}}$ and READY (W) signals. The ORed composite of these signals should be used to inhibit write operation.

If write and read cycles are being executed simultaneously, and the storage cells in the lead device are not full of accumulated data when the last device completes writing to its last address, write operation shifts to the lead μPD42532 again. Writing continues in this manner until every data buffer is full.

Read cycles also begin with the lead device (n) and shift to the next (n + 1) once the last address has been read. When all devices have been completely emptied of data, the ORed composite of the $\overline{\text{EMPTY}}$ signals is low. If the expanded word length configuration has less than 64 bytes of data in a write register, $\overline{\text{EMPTY}}$ will not be at a low level; READY (R) will be low to indicate that standard read operation may not proceed. Forced read or dummy write cycles will be required to continue reading any accumulated data of less than 64 bytes.

Figure 3. Single-Device Configuration Block Diagram

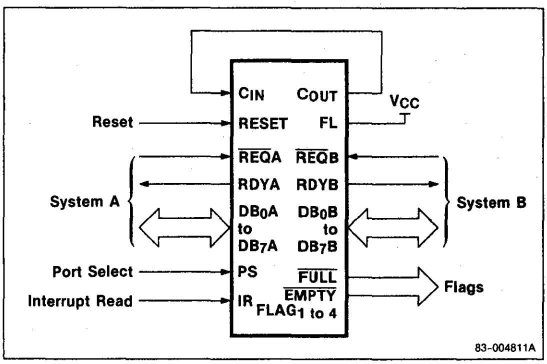


Figure 4. Expanded Word Width Block Diagram

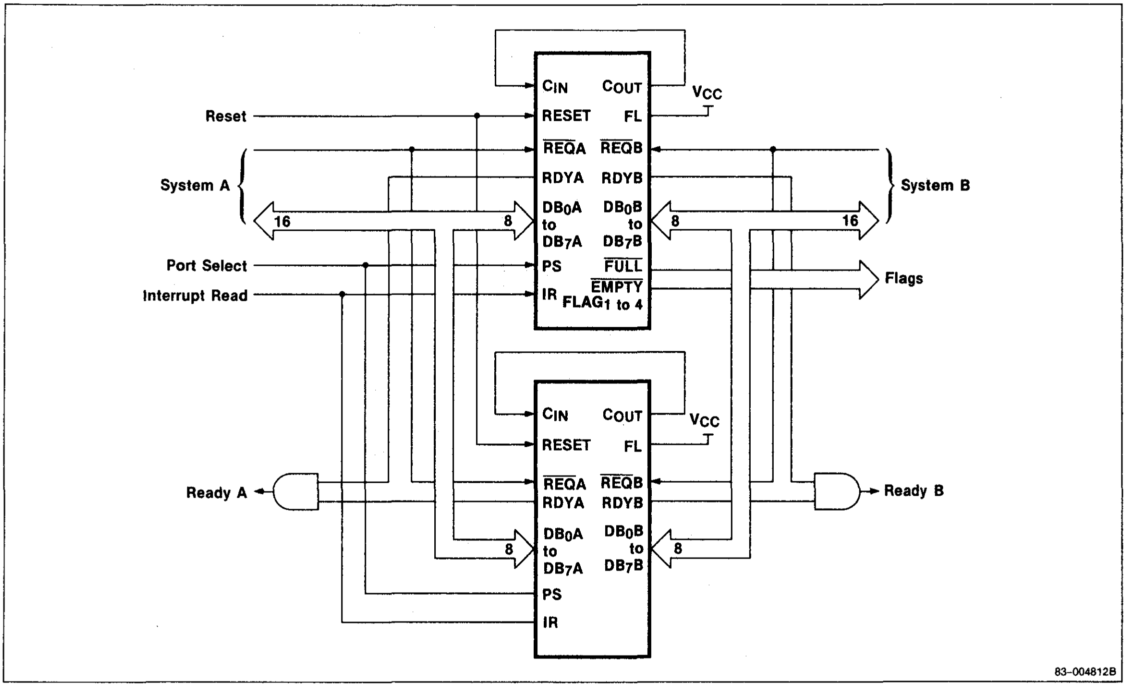
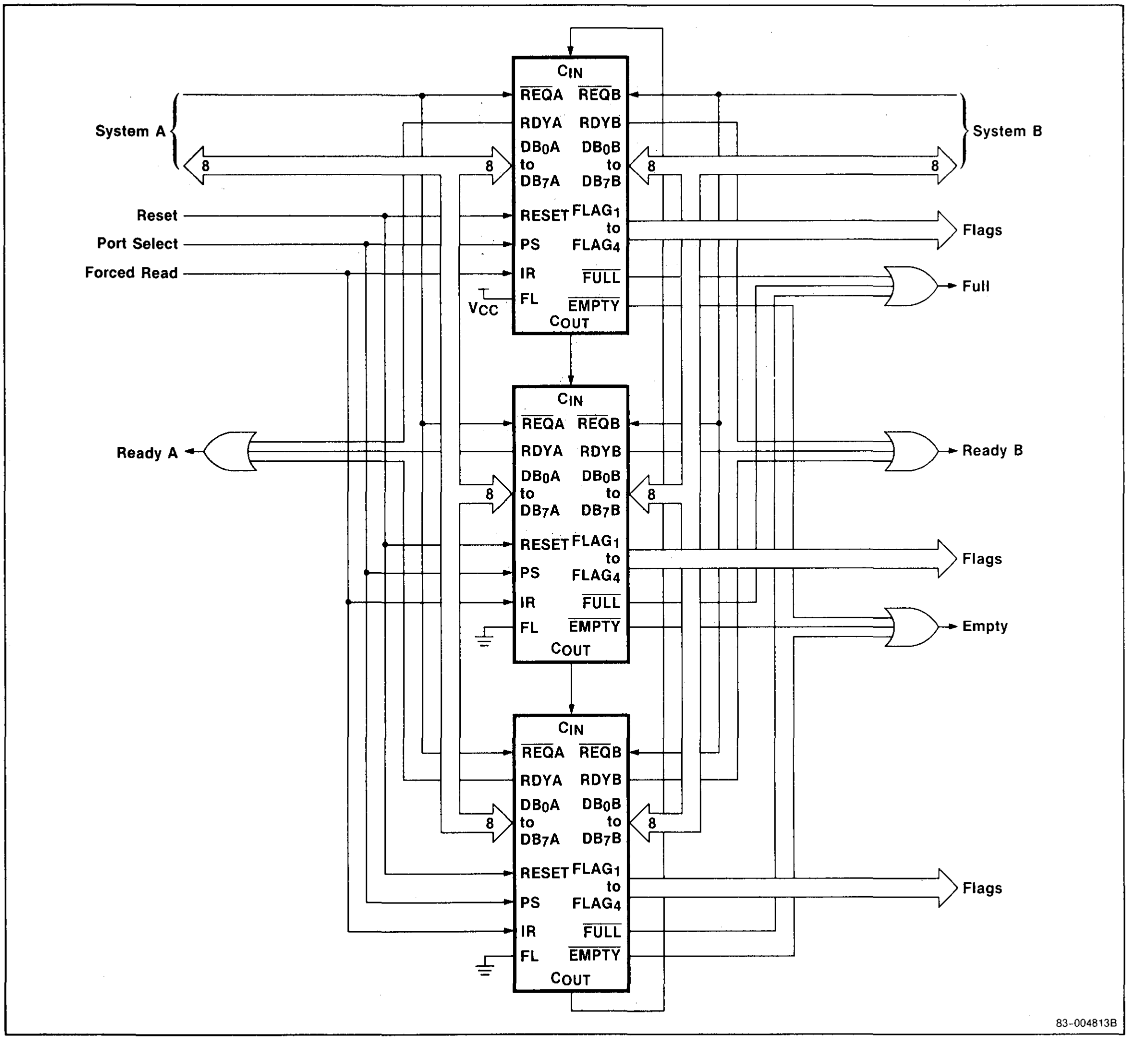


Figure 5. Expanded Word Length Block Diagram



Absolute Maximum Ratings

Terminal voltage, V_T	−1.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Output current, I_O	50 mA
Power supply voltage, V_{CC}	−1.5 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended DC Operating Conditions

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.0		0.8	V

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby supply current	I_{CC1}			20	mA	$\overline{\text{REQUEST}}$ A, B = V_{IH}
Write/read cycle supply current	I_{CC2}			80	mA	t_{WC} = 100 ns; t_{RC} = 100 ns
Write cycle supply current	I_{CC3}			60	mA	t_{WC} = 100 ns; $\overline{\text{REQUEST}}$ (R) = V_{IH}
Read cycle supply current	I_{CC4}			60	mA	t_{RC} = 100 ns; $\overline{\text{REQUEST}}$ (W) = V_{IH}
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{CC}; other inputs = 0 V
Output leakage current	I_O	−10		10	μA	V_O = 0 to V_{CC}; output disabled
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4 mA

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			10	pF	$\overline{\text{REQUEST}}$, $\overline{\text{RESET}}$, PS, C_{IN}, IR, FL/$\overline{\text{RT}}$
Output capacitance	C_O			10	pF	READY, $FLAG_1$-$FLAG_4$, C_{OUT}, $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$
Input/output capacitance	$C_{I/O}$			10	pF	DB_0-DB_7

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Read cycle time	t_{RC}	100		ns	
$\overline{REQUEST}$ (R) pulse width	t_{RQW}	50	10000	ns	(Note 5)
$\overline{REQUEST}$ (R) precharge time	t_{RQP}	30		ns	
$\overline{REQUEST}$ (R) low hold time after READY (R) high	t_{RQN}	50	10000	ns	(Note 6)
READY (R) low output time	t_{RRF}		30	ns	(Note 14)
Access time	t_{AC}		50	ns	
Access time after READY (R) high	t_{ACR}		50	ns	
Output data hold time	t_{OH}	10		ns	
Output data off time	t_{OFF}		40	ns	
Low-impedance output delay	t_{LZ}	5		ns	
Low-impedance output delay after READY (R) high	t_{LZR}	0		ns	
READY (R) low time when empty	t_{SRR}		4800 + 64 t_{WC}	ns	(Note 8)
READY (R) low time when almost empty	t_{EMR}	0	4800 + 63 t_{WC}	ns	(Note 8)
Write cycle time	t_{WC}	100		ns	
$\overline{REQUEST}$ (W) pulse width	t_{WQW}	50	10000	ns	(Note 5)
$\overline{REQUEST}$ (W) precharge time	t_{WQP}	30		ns	
$\overline{REQUEST}$ (W) low hold time after READY (W) high	t_{WQN}	50	10000	ns	(Note 6)
READY (W) low output time	t_{WRF}		30	ns	
Write data setup time	t_{DW}	30		ns	
Write data hold time	t_{DH}	10		ns	
$\overline{REQUEST}$ high setup time	t_{QRP}	t_T + 30		ns	(Note 6)
READY (W) low time when full	t_{FLW}	0	3200 + 64 t_{RC}	ns	
$FLAG_1$-$FLAG_4$ output times	t_{FLO}		4800	ns	
$\overline{EMPTY}$ and $\overline{FULL}$ output valid times	t_{EFO}		40	ns	
$\overline{EMPTY}$ and $\overline{FULL}$ output hold times	t_{EFH}	0		ns	
$\overline{FULL}$ output off time	t_{FOF}		3200	ns	(Note 9)
C_{OUT} output off time when read request is executed	t_{COR}		40	ns	
C_{OUT} output on time when write request is executed	t_{COW}		40	ns	
C_{IN} setup time for $\overline{REQUEST}$ (R)	t_{CIR}	10		ns	
C_{IN} setup time for $\overline{REQUEST}$ (W)	t_{CIW}	10		ns	
Reset pulse width	t_{SW}	100		ns	
READY, $\overline{FULL}$, and $\overline{EMPTY}$ output times after reset	t_{SWR}		80	ns	
$FLAG_1$-$FLAG_4$ output times after reset	t_{SSF}		100	ns	
$\overline{REQUEST}$ precharge hold time after reset	t_{SWQ}	30		ns	
$\overline{RT}$ disable hold time after reset	t_{SRT}	800		ns	

AC Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
C_{OUT} output low time after reset	t_{SWC}		100	ns	
READY (R) on time after interrupt read is executed	t_{FRR}	0	6400	ns	(Note 7)
READY (W) off time after interrupt read is executed	t_{FWR}		50	ns	(Note 7)
READY (W) on time after interrupt read	t_{IRW}		100	ns	(Note 11)
$\overline{\text{REQUEST}}$ (W) hold time after IR input	t_{FQA}	60		ns	(Note 13)
$\overline{\text{REQUEST}}$ (W) setup time before IR input	t_{FQB}	60		ns	
IR pulse width	t_{FW}	50	2000	ns	(Notes 4, 12, 13)
$\overline{\text{REQUEST}}$ hold time after PS input	t_{PAQ}	100		ns	
$\overline{\text{REQUEST}}$ setup time before PS input	t_{PBQ}	100		ns	
READY output time after port selection	t_{PSR}		50	ns	
$\overline{\text{RT}}$ pulse width	t_{RTW}	50	2000	ns	(Note 4)
$\overline{\text{REQUEST}}$ setup time before $\overline{\text{RT}}$ input	t_{BRT}	60		ns	(Note 10)
$\overline{\text{REQUEST}}$ hold time after $\overline{\text{RT}}$ input	t_{RTQ}	60		ns	
READY (R) on time after retransmit is executed	t_{RTR}		6400	ns	(Note 7)
READY (W) on time after retransmit is executed	t_{WRT}		4800	ns	(Note 7)
READY off time after retransmit is executed	t_{RRT}		50	ns	
$\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ output hold times after retransmit is executed	t_{FSRT}	0		ns	
$\overline{\text{EMPTY}}$ reset time after retransmit is executed	t_{RTE}		3200	ns	
$FLAG_1$-$FLAG_4$ output valid times after retransmit is executed	t_{RTF}		8000	ns	
Input transition time	t_T	5	50	ns	

Notes:

(1) All voltages are referenced to GND.

(2) All ac measurements assume input pulse rise and fall times of 5 ns.

(3) The input voltage reference levels for timing ratings are V_{IH} (min) and V_{IL} (max). Transition time t_T is defined between V_{IH} and V_{IL}.

(4) IR and $\overline{\text{RT}}$ inputs cannot be applied simultaneously. A timing delay of at least 100 ns is required. See figures 6 and 7 for acceptable input methods.

(5) The maximum pulse width of 10,000 ns applies only when the READY signal is on.

(6) $\overline{\text{REQUEST}}$ cannot be raised to a high level during the t_{QRP} + t_{RQN} (or t_{WQN}) interval.

(7) If an $\overline{\text{RT}}$ (IR) pulse is applied during IR ($\overline{\text{RT}}$) operation, the $\overline{\text{RT}}$ (IR) operation is delayed until IR ($\overline{\text{RT}}$) operation is released.

(8) "Empty" is defined as the state where the amount of stored data is zero, and "almost empty" is defined as the state where the amount of data is 1 to 63 bytes.

(9) t_{FOF} is defined from the rising edge of the $\overline{\text{REQUEST}}$ (R) signal when the amount of stored data reaches the prescribed value (that is, the value at which the FULL signal changes from a low level to a high level as defined in Table 1).

(10) t_{BRT} = 4800 ns minimum for the devices with process code K.

Figure 6. Input Timing for IR and $\overline{\text{RT}}$: Method 1

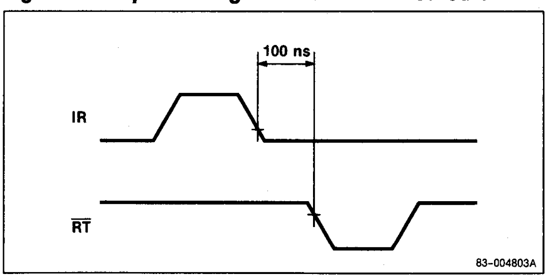
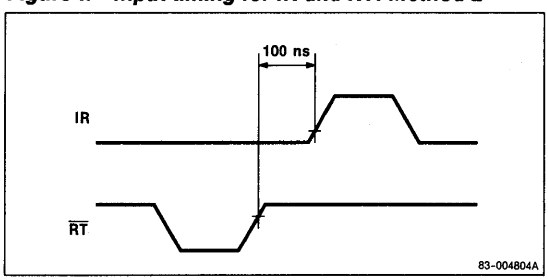


Figure 7. Input timing for IR and $\overline{\text{RT}}$: Method 2



3

AC Characteristics (cont)

Notes [cont]:

(11) After all data has been read in an IR cycle for devices with process code K, always input a $\overline{RESET}$ signal to initialize the internal circuitry before proceeding to the next operation. See figure 8.

(12) The IR signal is invalid whenever the $\overline{EMPTY}$ signal is low on devices with process code K.

(13) If an IR input signal is applied in a cascade connection for devices with process code K, the $\overline{REQUEST}$ (W) signal must stay at a high level until all data has been read.

(14) Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, read all of the remaining data using the interrupt read option.

Figure 8. Reset Pulse After IR Operation

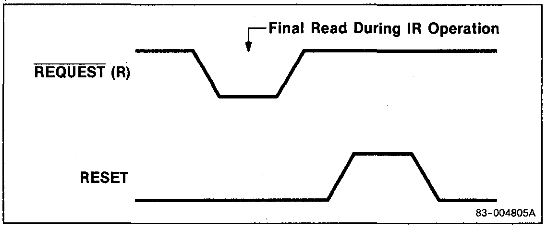


Figure 9. Input Timing

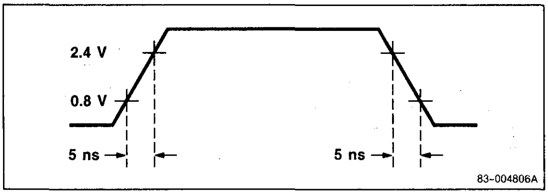


Figure 10. Output Timing

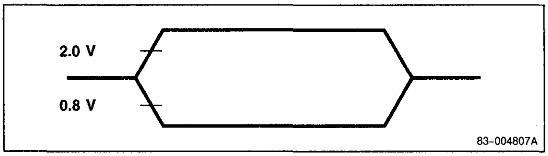
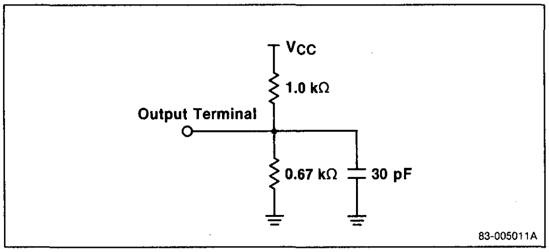
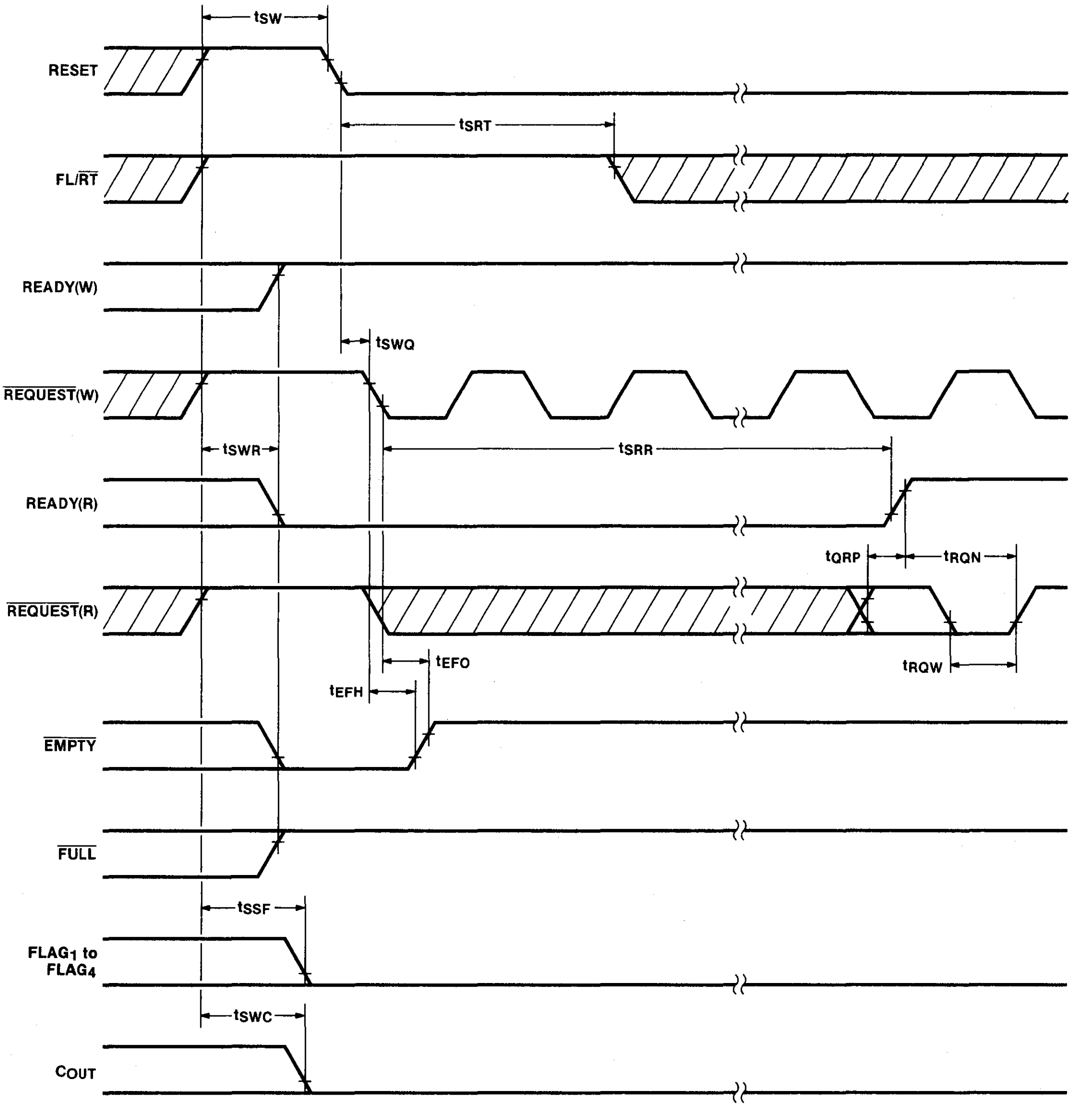


Figure 11. Output Loads



Timing Waveforms

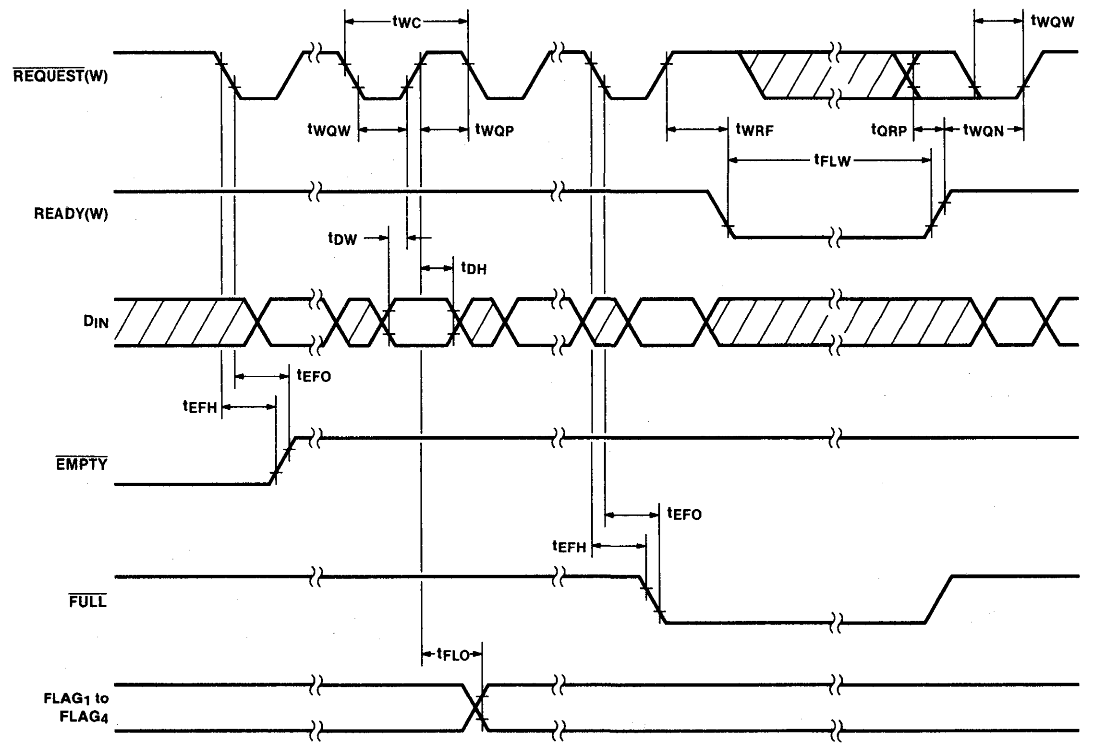
Reset Cycle



Notes:
(1) IR = low
(2) PS = high or low

Timing Waveforms (cont)

Write Cycle

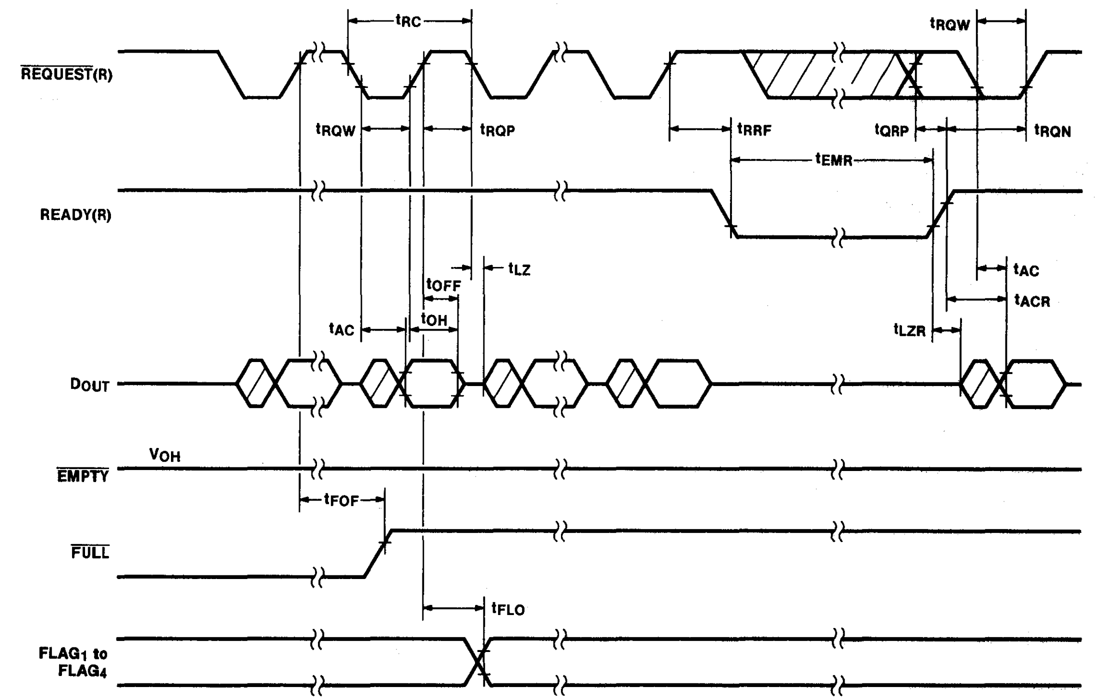


Notes:
(1) IR = low
(2) FL/$\overline{RT}$ = high
(3) PS = high or low
(4) RESET = low

83-004815B

Timing Waveforms (cont)

Read Cycle



Notes:

(1) IR = low

(2) FL/$\overline{RT}$ = high

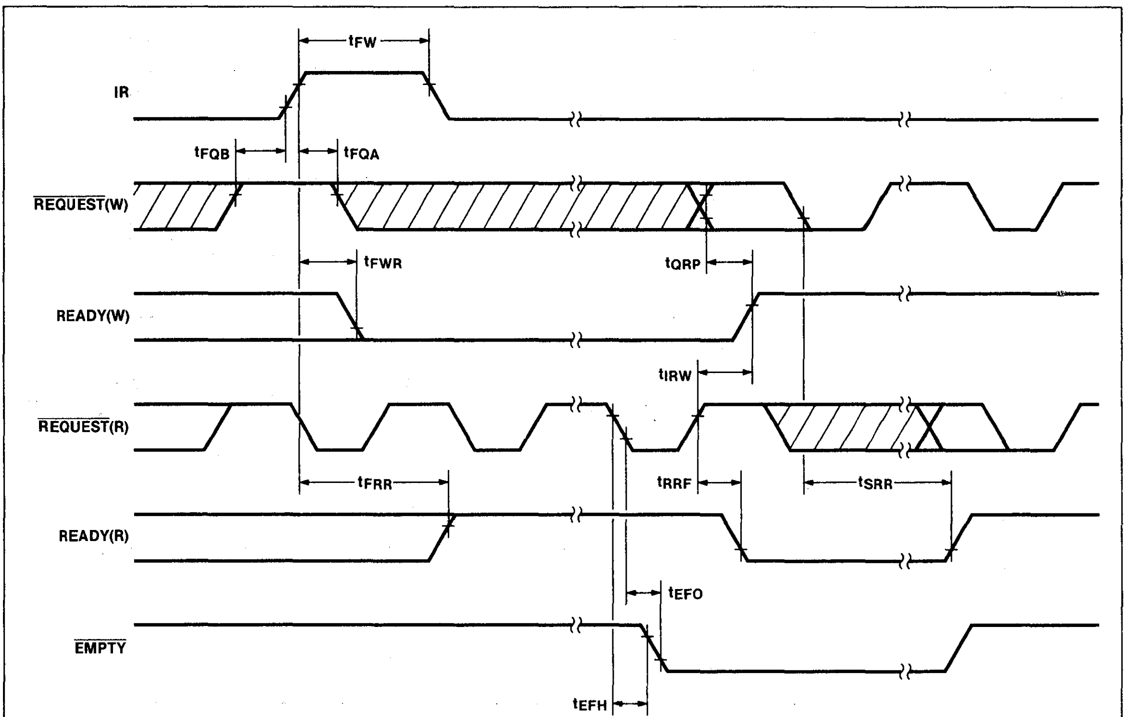
(3) PS = high or low

(4) $\overline{RESET}$ = low

83-004816B

Timing Waveforms (cont)

Interrupt Read Cycle



Notes:

(1) PS = high or low

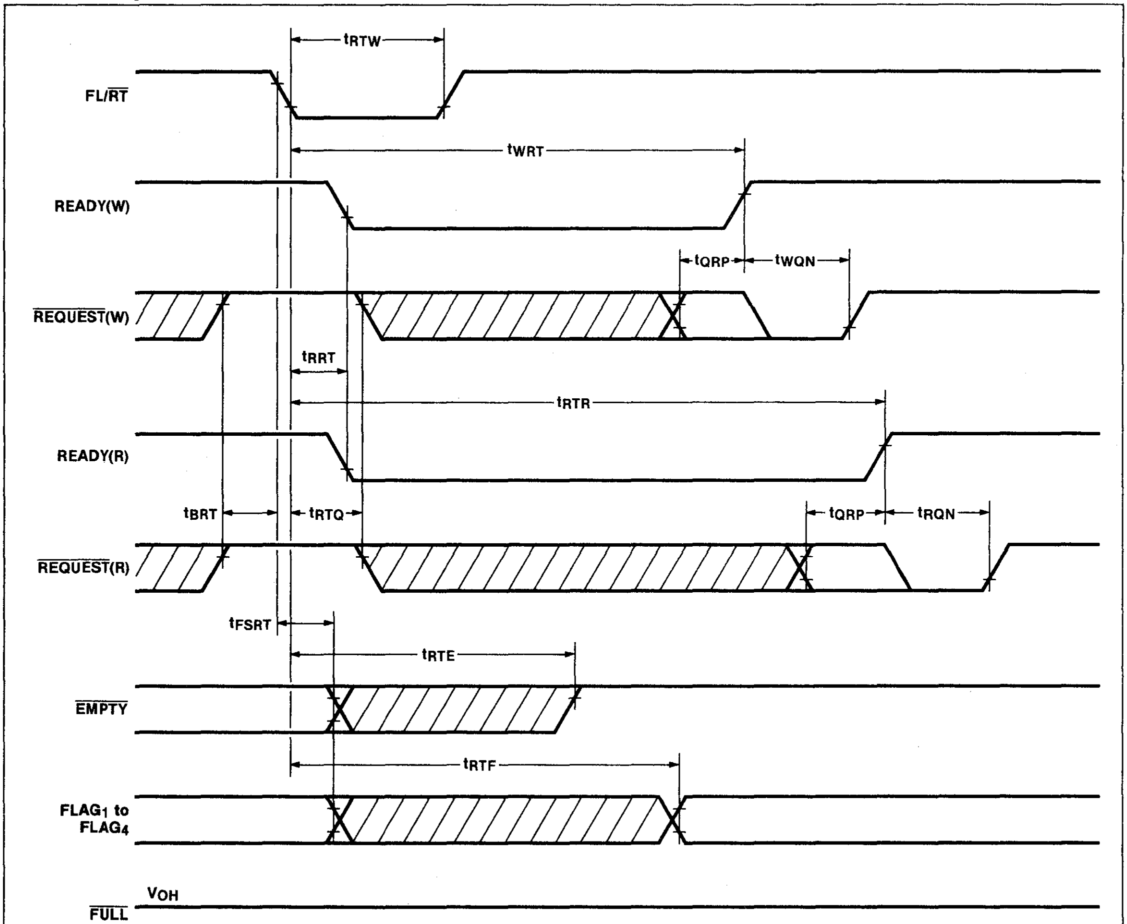
(2) FL/$\overline{RT}$ = high

(3) RESET = low

83-004818B

Timing Waveforms (cont)

Retransmit Cycle

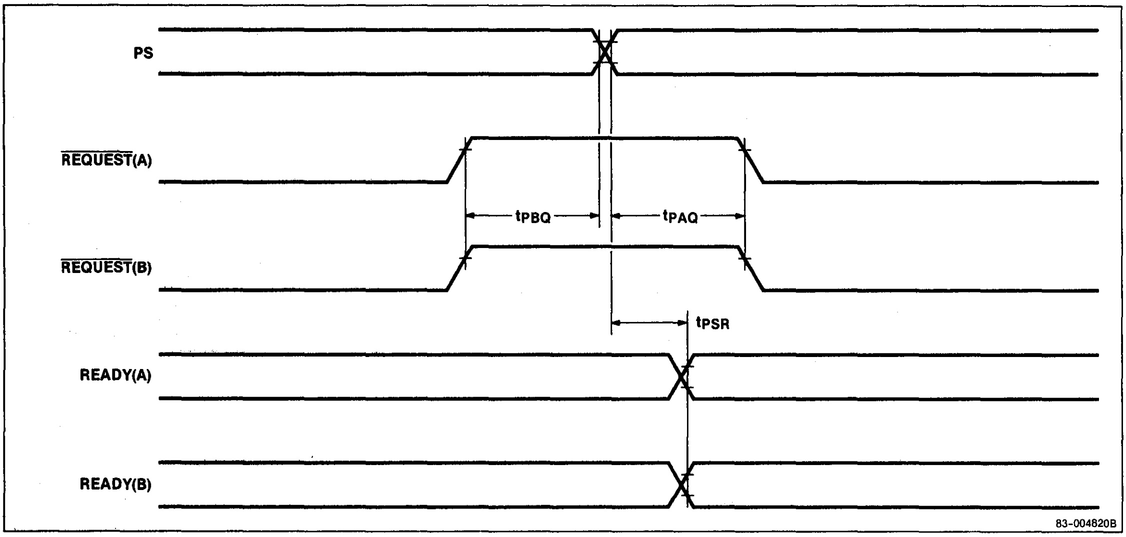


Notes:
(1) PS = high or low
(2) IR = low
(3) RESET = low

3

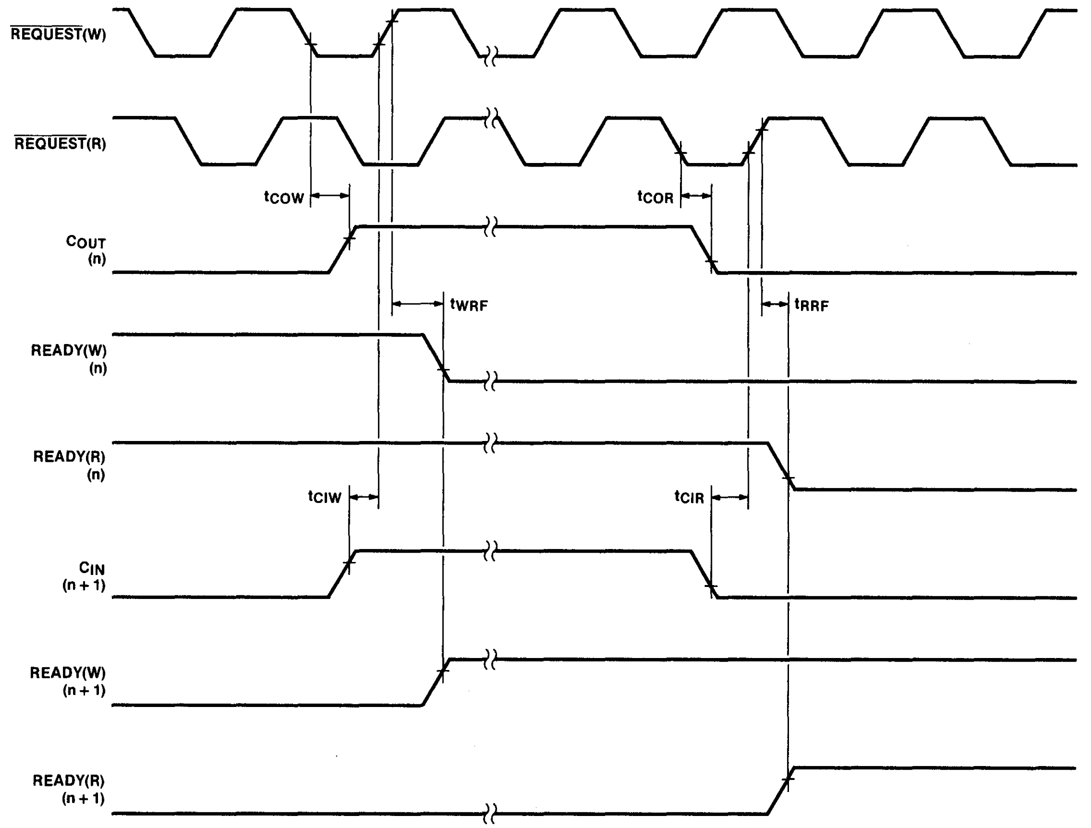
Timing Waveforms (cont)

Port Select Cycle



Timing Waveforms (cont)

Cascade Cycle



Notes:

(1) IR = low

(2) FL/$\overline{RT}$ = high or low

(3) PS = high or low

(4) RESET = low

83-004817B

μPD42601 1,048,576 x 1-BIT SILICON FILE

PRELIMINARY INFORMATION

Description

The μPD42601 silicon file is an economical mass storage device specifically designed to replace magnetic disk drives in silicon disk, solid-state recording, and system backup applications in a variety of computer systems. Organized as 1,048,576 words by 1 bit, the μPD42601 provides a battery backup feature for enhanced system performance and a substantial savings in power consumption.

The device is capable of executing standard access or page-mode write and read cycles. Refreshing is accomplished by means of $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $\overline{RAS}$-only refresh cycles, self-refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during a 32-ms period.

The μPD42601 is uniquely suitable for battery backup systems because it requires a very low power supply current for extended periods of self-refresh operation. If ambient temperature is limited to 50°C (max), as little as 30 μA (max) is required to maintain all data.

The μPD42601 is available in high-density 18-pin plastic DIP, 20-pin plastic ZIP, or 26/20-pin plastic SOJ packaging.

Features

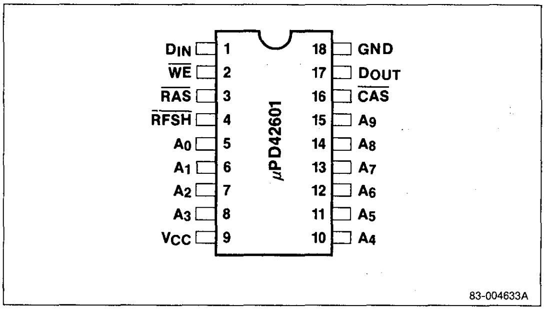
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ CMOS technology
- ☐ Low operating power: 12 mA maximum
- ☐ 30 μA maximum self-refresh current at 0 to 50°C
- ☐ Read or write cycle time: 1000 ns minimum
- ☐ Page-mode cycle time: 200 ns minimum
- ☐ $\overline{CAS}$ before $\overline{RAS}$ refreshing
- ☐ 512 refresh cycles during 32-ms period
- ☐ Automatic self-refreshing by $\overline{RAS}$ input cycling

Ordering Information

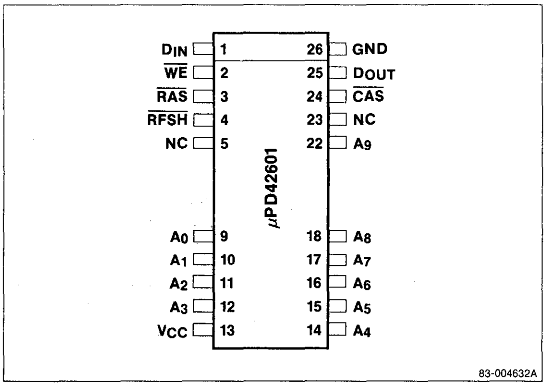
Part Number	Page-Mode Cycle (min)	Self-Refresh Current (max, 50°C)	Package
μPD42601C-60	200 ns	120 μA	18-pin plastic DIP
C-60L	200 ns	30 μA	
μPD42601LA-60	200 ns	120 μA	26/20-pin plastic SOJ
LA-60L	200 ns	30 μA	
μPD42601V-60	200 ns	120 μA	20-pin plastic ZIP
V-60L	200 ns	30 μA	

Pin Configurations

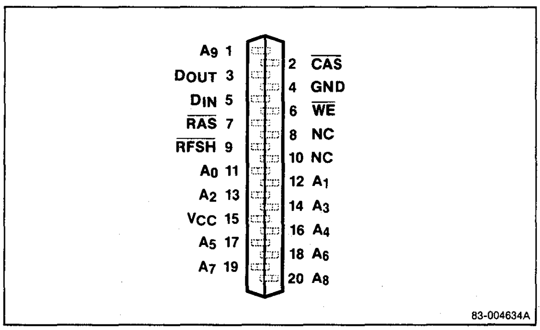
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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Pin Identification

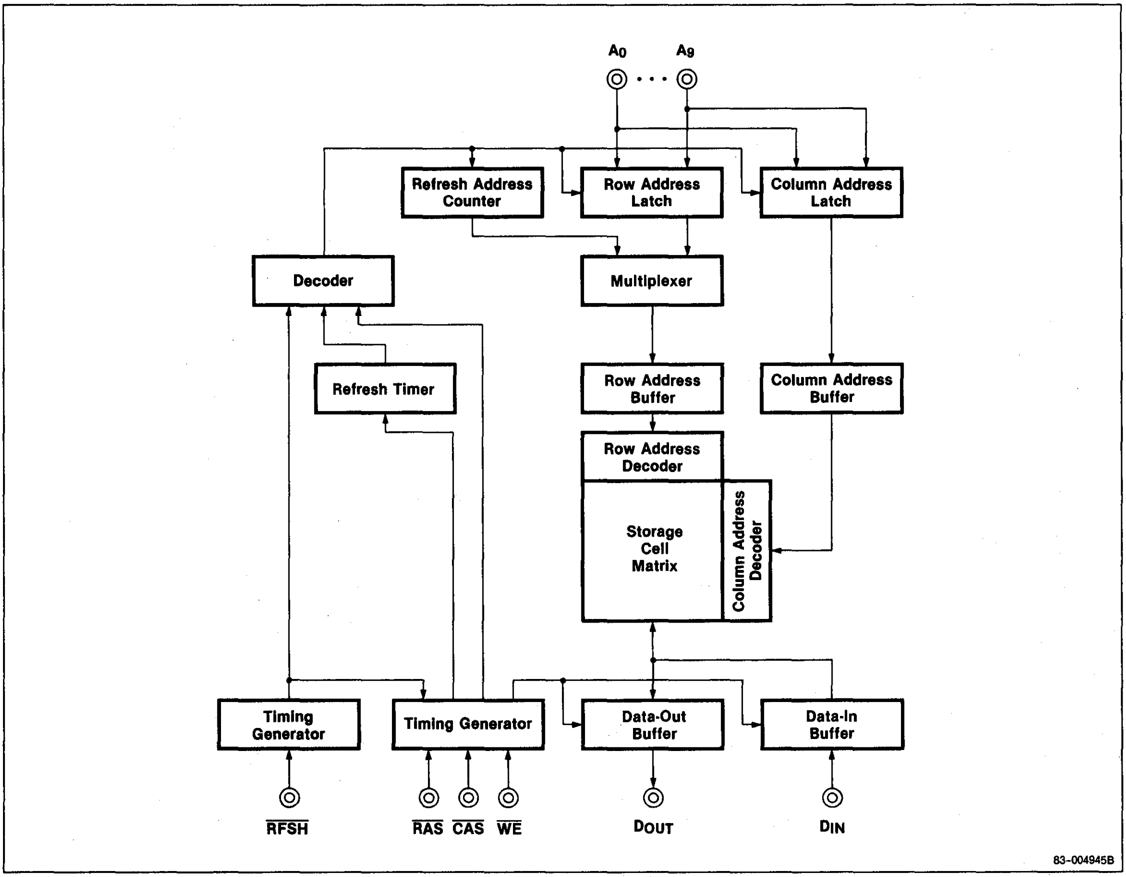
Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{RFSH}$	Self-refresh control
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W
Supply voltage, V_{CC}	−1.0 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Operation

Write and Read Operation

The μPD42601 is capable of standard write and read operation as well as page-mode operation. The ten row address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{RAS}$. Subsequently, ten column address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{CAS}$. An appropriate write or read cycle is executed according to the logical level of $\overline{WE}$: a high $\overline{WE}$ initiates a read cycle and low $\overline{WE}$ initiates a write cycle.

Page-mode operation may be executed by pulsing $\overline{CAS}$ repeatedly while maintaining a low $\overline{RAS}$. The first word is accessed in the same manner as in standard write and read operation, with row addresses latched onto the chip by $\overline{RAS}$ and column addresses latched by $\overline{CAS}$. Subsequent column addresses are accessed for each $\overline{CAS}$ cycle, repeated during a period up to the maximum $\overline{RAS}$ pulse width.

Refresh Operation

$\overline{CAS}$ before $\overline{RAS}$ Refreshing. This cycle may be initiated by bringing $\overline{CAS}$ low before $\overline{RAS}$ and holding it low after $\overline{RAS}$ falls. A built-in address counter makes external addressing unnecessary.

$\overline{RAS}$-Only Refreshing. $\overline{RAS}$-only refreshing is executed by holding $\overline{CAS}$ high as the row addresses are latched onto the chip by $\overline{RAS}$. Using this cycle, all storage cells are refreshed by the 512 address combinations of A_0 through A_8 during a 32-ms period.

Self-Refreshing. A self-refresh cycle is initiated for the addresses generated by the internal counter whenever $\overline{RFSH}$ is active low and the $\overline{RAS}$ input is cycling (see figure 1). Since the minimum required $\overline{RAS}$ cycling frequency depends on ambient temperature, power consumption will also vary with temperature as shown in the AC and DC Characteristics. For extended periods of self-refresh operation, a low supply current is required; e.g., if ambient temperature is limited to 50°C (max), as little as 30 μA (max) is required to maintain all data.

Recommended DC Operating Conditions

$T_A = 0$ to $+70$°C; GND = 0 V

		Limits			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} +1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V

Capacitance

$T_A = 25$°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$
Output capacitance	C_D	7	pF	D_{OUT}

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DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Operating current, average	I_{CC1}			12	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling; $I_O = 0$ mA; $t_{RC} = t_{RC}$ (min)
Standby current	I_{CC2}			2.0	mA	$\overline{\text{RAS}} = \overline{\text{CAS}} = \overline{\text{RFSH}} = V_{IH}$
				0.5	mA	$\overline{\text{RAS}} = \overline{\text{CAS}} = \overline{\text{RFSH}} \geq V_{CC} - 0.4$; A_0-A_9, D_{IN} and $\overline{\text{WE}} \geq V_{CC} - 0.4$ or ≤ 0.4 V
Operating current, $\overline{\text{RAS}}$-only refresh, average	I_{CC3}			10	mA	$t_{RC} = t_{RC}$ (min); $I_O = 0$ mA
Operating current, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, average	I_{CC4}			10	mA	$t_{RC} = t_{RC}$ (min); $I_O = 0$ mA
Operating current, self-refresh mode, average	I_{CC5}			30	μA	$\overline{\text{RAS}}$ cycling at 50 kHz (Notes 1, 2, 3, 4)
				60	μA	$\overline{\text{RAS}}$ cycling at 100 kHz (Notes 1, 2, 3, 4)
				120	μA	$\overline{\text{RAS}}$ cycling at 200 kHz (Notes 1, 2, 3)
Operating current, page mode, average	I_{CC6}			12	mA	$t_{PC} = t_{PC}$ (min); $I_O = 0$ mA
Input leakage current	I_{IL}	−1		1	μA	$V_{IN} = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−1		1	μA	D_{OUT} disabled; $V_{OUT} = 0$ to V_{CC}
Output voltage, low	V_{OL}			0.4	V	$I_O = 4.2$ mA
Output voltage, high	V_{OH1}	2.4			V	$I_O = -5$ mA
	V_{OH2}	0.7 V_{CC}			V	$I_O = -0.5$ mA

Notes:

(1) When $t_{FAS} \leq 2.5$ ms, I_{CC5} does not depend on the $\overline{\text{RAS}}$ clock; I_{CC5} (max) = 500 μA. When $t_{FAS} \geq 2.5$ ms, I_{CC5} (max) = 500 μA in the first 2.5 ms after $\overline{\text{RFSH}}$ falls (it does not depend on the $\overline{\text{RAS}}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

(2) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max] μPD42601-L	μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

(3) Average power supply current required for self refreshing is measured according to the following conditions: $\overline{\text{RAS}}$ is cycling at 50, 100 or 200 kHz; $V_{IH} \geq V_{CC} - 0.4$ V; $V_{IL} \leq 0.4$ V; $t_T \leq 50$ ns; A_0 to A_9, D_{IN}, $\overline{\text{WE}}$ and $\overline{\text{CAS}} = V_{CC}$ to GND; RFSH = V_{IL}. When $\overline{\text{RFSH}} = V_{IL}$ (≤ 0.4 V), the $\overline{\text{RAS}}$ input must be cycled at or exceeding the minimum frequency requirements.

(4) This specification applies to the μPD42601-L only. For the non-L version, I_{CC5} is 120 μA, maximum, at all T_A.

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	1000		ns	(Note 5)
Page-mode cycle time	t_{PC}	200		ns	(Notes 5, 15)
Access time from $\overline{\text{RAS}}$	t_{RAC}		600	ns	(Notes 6, 7)
Access time from $\overline{\text{CAS}}$ (falling edge)	t_{CAC}		100	ns	(Notes 6, 8)
Output buffer turnoff delay	t_{OFF}	0	100	ns	(Note 9)
Transition time (rise and fall)	t_T	3	50	ns	(Notes 3, 4)
$\overline{\text{RAS}}$ precharge time	t_{RP}	390		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	600	100000	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	100		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	100	10000	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	600		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	150	500	ns	(Note 10)
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	30		ns	(Note 11)
$\overline{\text{CAS}}$ precharge time (non-page cycle)	t_{CPN}	90		ns	
$\overline{\text{CAS}}$ precharge time (page cycle)	t_{CP}	90		ns	(Note 15)
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t_{RPC}	0		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	90		ns	
Column address setup time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	90		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	590		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	75		ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	(Note 12)
Write command hold time	t_{WCH}	90		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	590		ns	
Write command pulse width	t_{WP}	90		ns	
Data-in setup time	t_{DS}	0		ns	(Note 14)
Data-in hold time	t_{DH}	90		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	590		ns	
Write command setup time	t_{WCS}	0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	30		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	105		ns	
Refresh period	t_{REF}		32	ms	Addresses A_0-A_8
Self-Refresh Cycle					
$\overline{RFSH}$ pulse width	t_{FAS}	810		ns	(Note 13)
$\overline{RAS}$ to $\overline{RFSH}$ delay time	t_{RFD}	100		ns	
$\overline{RAS}$ setup time to $\overline{RFSH}$	t_{FRS}	200		ns	
$\overline{RAS}$ cycle time in self-refresh mode	t_{RCF}	1000		ns	(Note 16)
$\overline{RAS}$ precharge time in self-refresh mode	t_{RPF}	390		ns	

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Self-Refresh Cycle (cont)					
$\overline{RAS}$ pulse width in self-refresh mode	t_{RSF}	600		ns	
$\overline{RFSH}$ to $\overline{RAS}$ delay time	t_{FRD}	100		ns	
$\overline{RAS}$ hold time in self-refresh mode	t_{FRH}	200		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up (V_{CC} = +5.0 V ±10%), followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. $\overline{RAS}$, $\overline{CAS}$, and $\overline{RFSH}$ must equal V_{IH} during the initial pause.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(6) Load = 2 TTL loads and 100 pF (V_{OH} = 2.4 V, V_{OL} = 0.4 V).

(7) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(8) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(9) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(10) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) When $t_{FAS} \leq$ 2.5 ms, I_{CC5} does not depend on the $\overline{RAS}$ clock; I_{CC5} (max) = 500 μA. When $t_{FAS} \geq$ 2.5 ms, I_{CC5} (max) = 500 μA for the first 2.5 ms after $\overline{RFSH}$ falls (it does not depend on the $\overline{RAS}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

Notes [cont]:

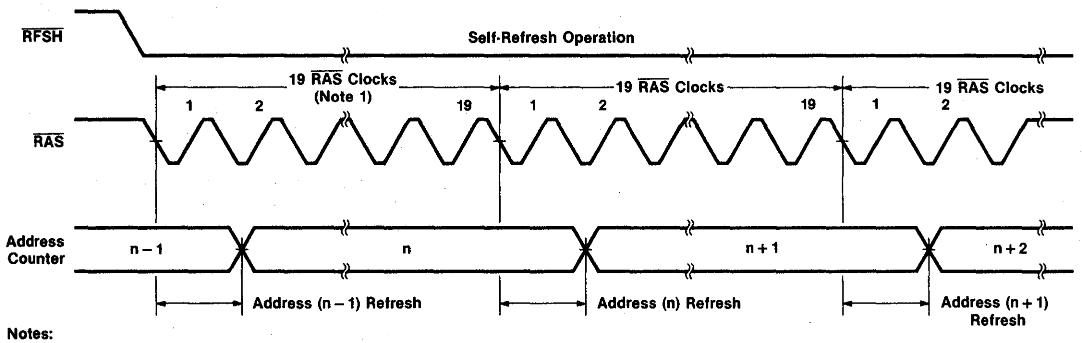
(14) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(15) This parameter is applicable to page-mode operation.

(16) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max] μPD42601-L	t_{RCF} [max] μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

Figure 1. Internal Address Generation in Self-Refresh Operation



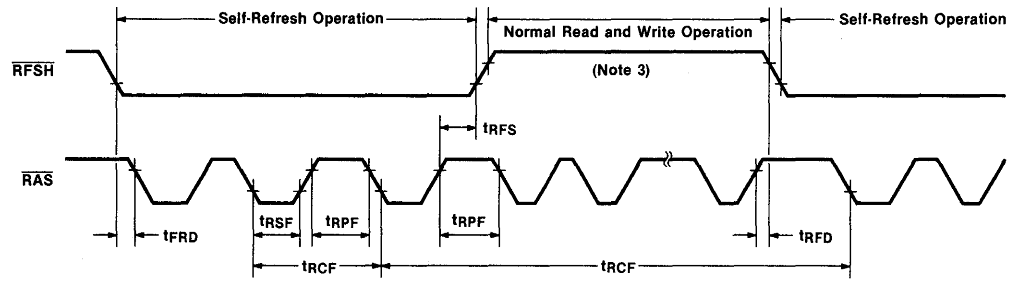
Notes:

(1) One internal address is refreshed every 19 $\overline{RAS}$ pulses.

(2) The self-refresh mode is intended primarily for long periods of refresh-only operation.

83-004503B

Figure 2. Special Requirement for t_{RCF} Near Periods of Limited Standard Refresh Cycles



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

T_A	t_{RCF} [max] μPD42601-L	t_{RCF} [max] μPD42601
50°C	20 μs	5 μs
60°C	10 μs	5 μs
70°C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

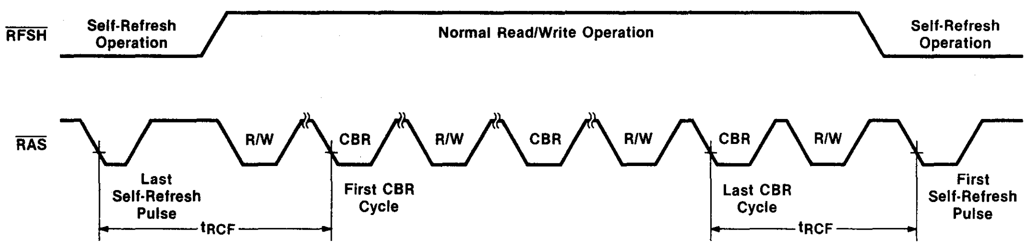
[3] In this period of normal read/write operation, there are no CBR refresh cycles or less than 512 $\overline{RAS}$-only refresh cycles.

[4] The time delay between the last self-refresh pulse in one self-refresh cycle, and the first self-refresh pulse in the next cycle, is defined by t_{RCF} [max] when the intervening period of read and write operation meets the conditions in Note 3.

[5] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004502B

Figure 3. Timing Restrictions for Entering and Exiting Self-Refresh Operation



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

T_A	t_{RCF} [max] μPD42601-L	t_{RCF} [max] μPD42601
50°C	20 μs	5 μs
60°C	10 μs	5 μs
70°C	5 μs	5 μs

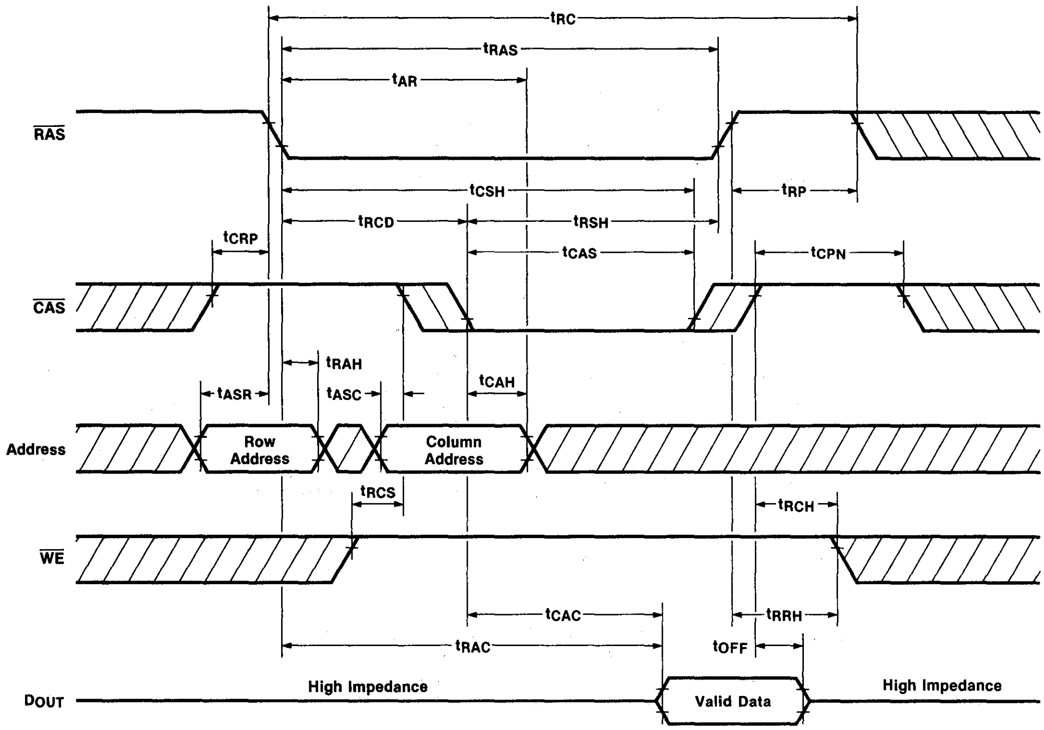
[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004501B

Timing Waveforms

Read Cycle



Note:
(1) $\overline{RFSH}$ = V_{IH}.

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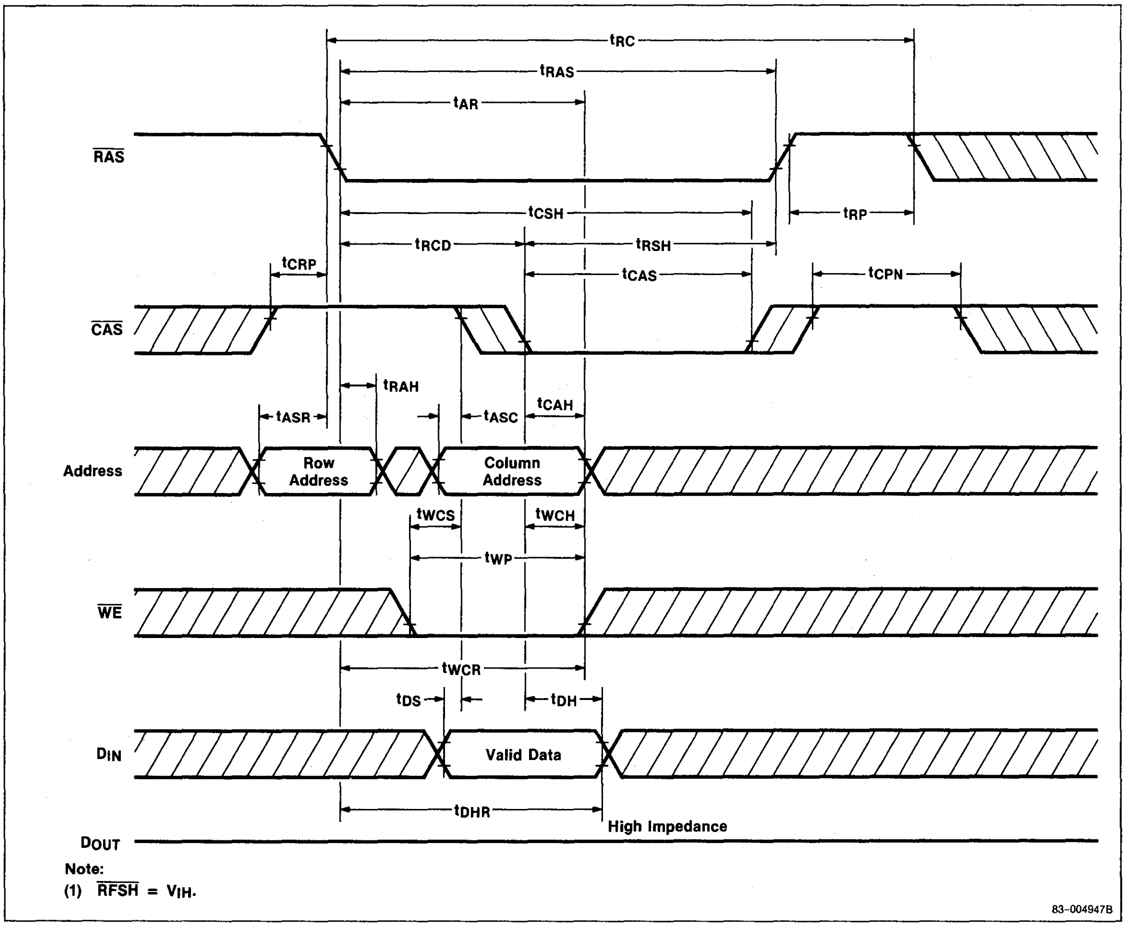
Timing Waveforms (cont)

Write Cycle (Early Write)



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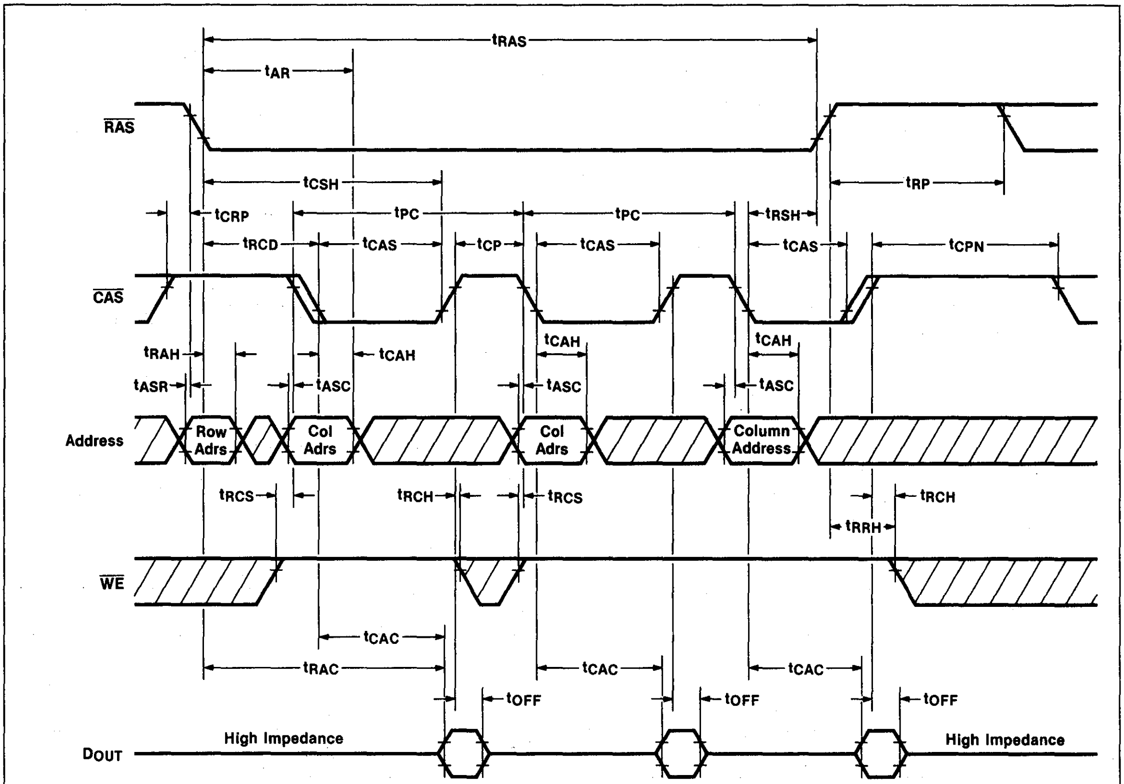
Timing Waveforms (cont)

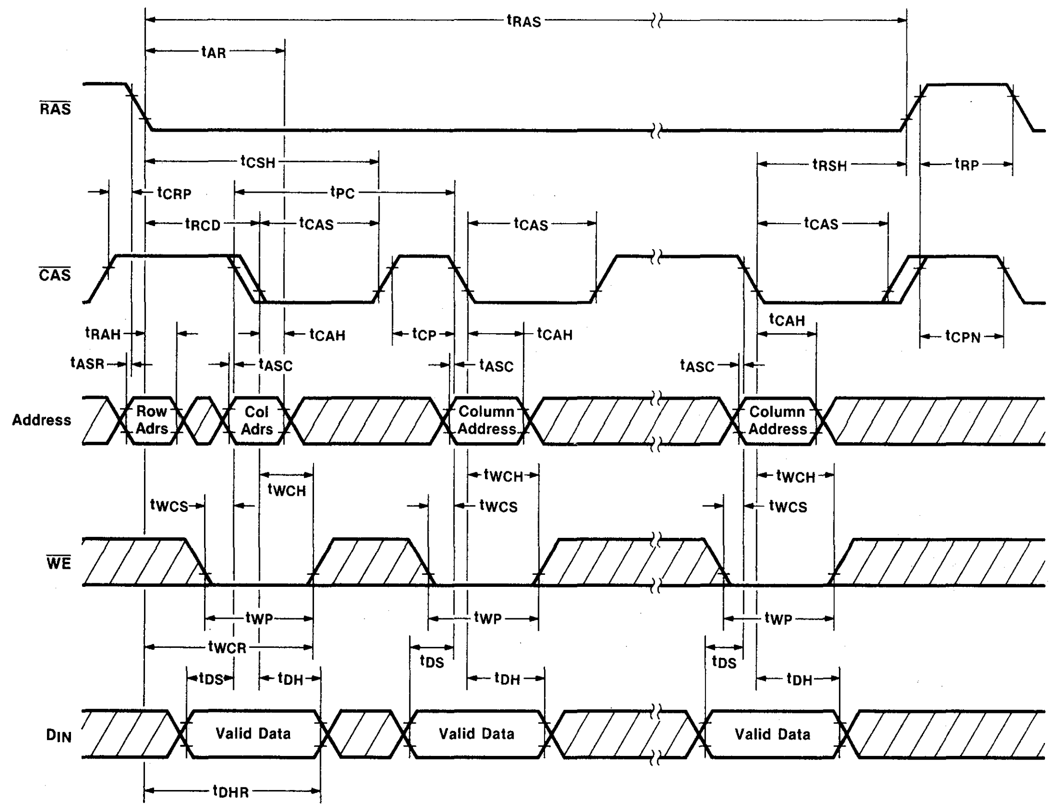
Page-Mode Read Cycle



Note:
(1) $\overline{RFSH}$ = V_{IH}.

Timing Waveforms (cont)

Page-Mode Write Cycle (Early Write)



Note:
(1) $\overline{RFSH}$ = V_{IH}.

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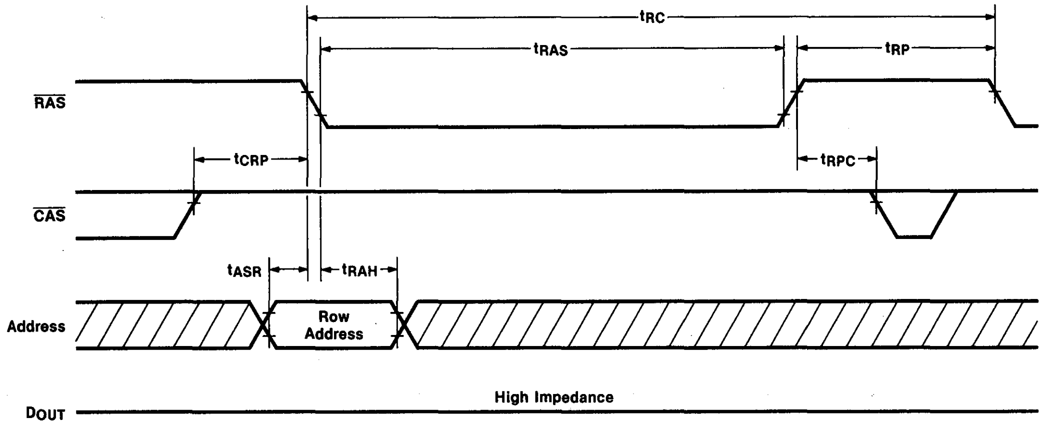
NEC

Timing Waveforms (cont)

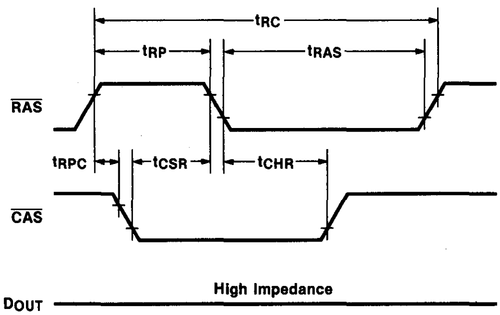
$\overline{RAS}$-Only Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$ and D_{IN} = don't care.

83-004951B

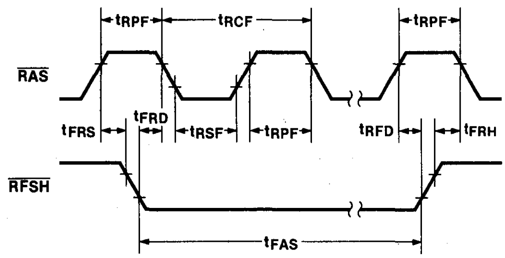
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$, D_{IN}, Addresses = don't care.

83-004950A

Self-Refresh Cycle



Note:
(1) $\overline{CAS}$, $\overline{WE}$, D_{IN}, Address = don't care.

83-004952A

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μPD43501 1,024-CHANNEL TIME DIVISION SWITCH

PRELIMINARY INFORMATION

Description

The μPD43501 is a time-switch device designed for use in a high-performance digital communications network. Features include a time-switch function by which up to 1,024 channels can be exchanged using a 16-bit data width, and a tone output function by which an 8-bit tone signal can be output to an arbitrary channel.

Two planes of 1-kword by 8-bit storage area and one plane of 1-kword by 10-bit control storage area for the time-switch function enable the μPD43501 to realize switching modes in which arbitrary 1,024 or 512 input channels can be connected to arbitrary 1,024 or 512 output channels. The configuration of the tone signal output section, one plane of 64-word by 8-bit tone storage area and one plane of 1-kword by 8-bit tone control storage area, allows the device to output up to 64 different tone signals to an arbitrary output channel as 8-bit voice/tone data.

Ordering Information

Part Number	Data Transfer Rate (max)	Package
μPD43501R	8.192 Mbps	132-pin ceramic pin grid array (PGA)

Features

- ☐ Separate switch storage and control storage to allow construction with one VLSI device of a non-blocking switching network having a maximum capacity of 1,024 channels
- ☐ Selectable operation
  - — 1,024 by 1,024 serial input and output
  - — 1,024 by 1,024 parallel input and output
    - • 16.384 MHz operating frequency
    - • 8.192 Mbps data transfer rate
  - — 512 by 512 parallel input and output
    - • 8.192 MHz operating frequency
    - • 4.096 Mbps data transfer rate
- ☐ Switching flexibility
  - — 8- or 16-bit data width
  - — n by 64 kbps connection
- ☐ Tone signal output function
- ☐ 8 by 8 space switch for an 8.192 Mbps, 128-channel multiplexed line
- ☐ CPU interfaces for the control storage and tone control storage
- ☐ Low power consumption: 1000 mW (typ)
- ☐ TTL-compatible inputs and outputs
- ☐ 132-pin ceramic pin grid array packaging

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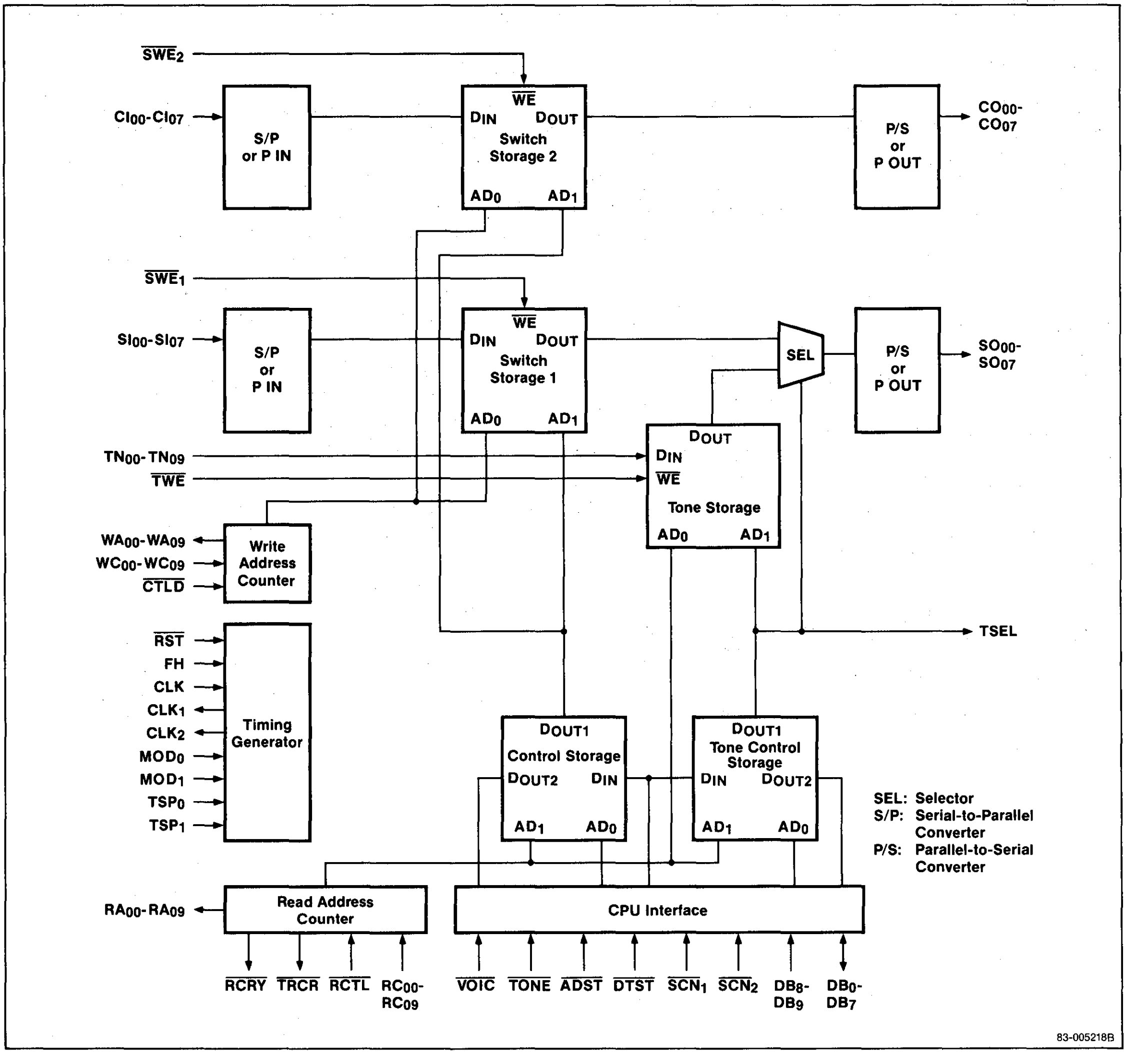
Block Diagram



Switching Functions

Mode 0

In this mode, the μPD43501 inputs eight 128-channel multiplexed lines from ports SI_{00} through SI_{07} (or from CI_{00} through CI_{07}) and outputs eight 128-channel multiplexed lines to ports SO_{00} through SO_{07} (or CO_{00} through CO_{07}). Refer to figure 1 for a functional pin diagram.

Serial input data from the input ports first is converted to parallel data by the serial-to-parallel converters in the receive section, and then multiplexed and sent to the input section of the switch storage area. Since the write address counter is synchronized with input data, the write address of the switch storage area corresponds to the time slot number of the input signal. Writing multiplexed data to the switch address specified by the write address counter causes input data in the time slot corresponding to the switch address always to be stored at that address (figure 2).

Conversely, a control storage address corresponds to an output-side time slot number, and the data in control storage indicates the switch storage address, i.e., the input-side time slot number is stored at the control storage address corresponding to the output-side time slot to which the input-side is transferred.

The address signal is sent from the read address counter to control storage in synchronization with each output-side time slot. Data read out by this operation is then sent to the switch storage area as the address signal, and the data in the specified address (input-side time slot) is then read out on the output side and switched. Switched data is sent to the parallel-to-serial converters in the transmission section, where it is converted to serial data and then output to the appropriate output ports.

With this switching function, the data in an arbitrary time slot on the input side can be output as data in an arbitrary time slot on the output side. Furthermore, in addition to the time division switch function, a space switch function enables switching time slots on any of the eight input ports to be output on any of the eight output ports. This means that a nonblocking 8 x 8 space switch for 128-channel multiplexed lines can be realized.

Mode 1

Mode 1 makes it possible for the μPD43501 to input 512-channel multiplexed lines (4.096 Mbps by 8 bits), 8 bits in parallel, and output 512-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are then performed.

Mode 2

In Mode 2, the μPD43501 inputs 1,024-channel multiplexed lines (8.192 Mbps by 8 bits), 8 bits in parallel, and outputs 1,024-channel multiplexed lines, 8 bits in parallel. The input signals received on the input ports are sent to the switch storage area in parallel, after which the same switching functions described in Mode 0 are performed.

Figure 1. Functional Pin Diagram

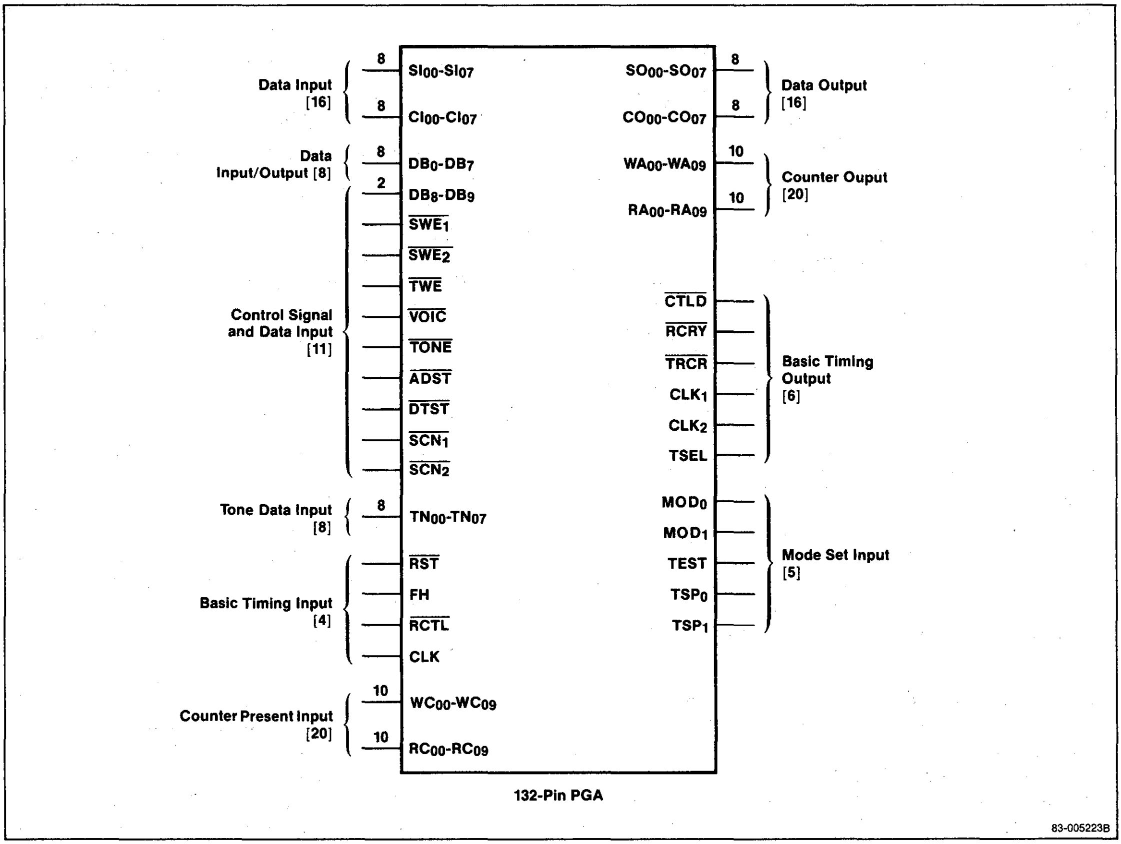
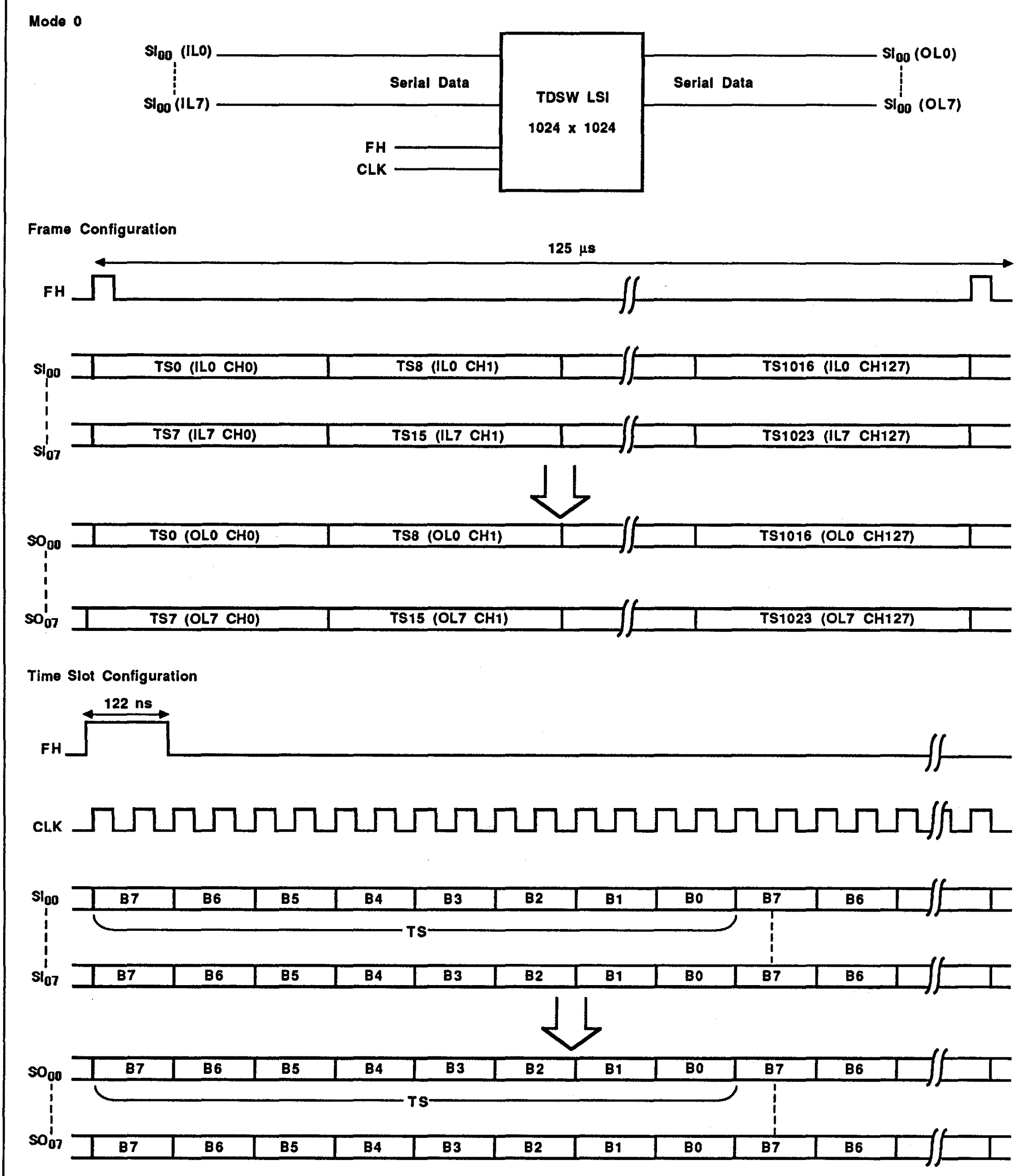


Figure 2. Time Slot Versus Frame Configuration



Notes:
[1] IL = input line
[2] OL = output line
[3] TS = time slot
[4] CH = channel

83IH-5215B

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μPD43608 SINGLE-CHIP CACHE SUBSYSTEM

PRELIMINARY INFORMATION

Description

The μPD43608 is an integrated cache subsystem that provides the microprocessor system designer with a high-performance, single-chip, general-purpose cache solution. The μPD43608 consists of a CPU interface, directory storage (including address tag and validity bit storage), 8K bytes of on-chip data storage, 128 x 6-bit least recently used (LRU) replacement storage, internal address and data paths for cache bypass operations, an asynchronous 32-bit system bus interface, and several features optimizing cache write and miss operations. The μPD43608 is also able to interface with a number of 16- and 32-bit general-purpose microprocessors operating at 16 or 20 MHz.

Features

- ☐ High-performance 16- and 20-MHz operation
- ☐ 16- and 32-bit microprocessor interface capability
- ☐ Integrated cache architecture
  - — 8K bytes of on-chip data storage
  - — 16-byte cache block size
  - — 4-way set associative placement algorithm
- ☐ Bus monitoring circuit
- ☐ LRU replacement algorithm
- ☐ Prefetch on miss—one block lookahead
- ☐ Fetch bypass and wraparound load
- ☐ Asynchronous 32-bit system bus interface
- ☐ Multichip configuration increases cache size
- ☐ Write-through storage update policy with one-level write buffer
- ☐ 132-pin ceramic pin grid array packaging
- ☐ CMOS circuit technology

Ordering Information

Part Number	Ready Output Time (max)	Cycle Time (min)	Package
μPD43608R-2	70 ns	125 ns	132-pin ceramic pin grid array
R-3	50 ns	100 ns	

Organization

The μPD43608 is organized as a 4-way set associative cache, with 8K bytes of on-chip data storage organized as 128 sets by four 16-byte data blocks. When the CPU executes a read cycle, the address tag field of the physical CPU address is compared to the address tag in the cache directory. If a hit occurs, the selected data is sent to the CPU. Otherwise, the μPD43608 initiates a miss cycle to access main storage and update the cache with the replacement block. This architecture ensures a high hit ratio of 95% in most microprocessor applications.

3

Optimizing the Miss Cycle

The hit rate is an important parameter for measuring performance. Since a high hit rate of 95% requires that the μPD43608 access the main storage array for 5% of all read cycles, the penalty in system performance incurred during a miss cycle may be significant. The μPD43608 provides a number of on-chip features that optimize system performance during a miss cycle.

Data Transfer Cycles

The μPD43608 cache subsystem provides two data transfer modes for accessing main storage during a miss cycle: (1) burst data transfer mode uses the nibble access feature of a DRAM in main storage to optimize system bus bandwidth; (2) in single data transfer mode, an address is transmitted with each read cycle to main storage for systems that don't use nibble access DRAMs.

Block Load and Fetch Bypass Buffers

Once the replacement block has been read from main storage, the block load buffer is used to reduce the replacement block transfer time by providing a temporary buffer for storing the replacement block while the cache data storage is being updated.

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Concurrently, the CPU throughput is optimized by loading the missed word into the fetch bypass buffer as soon as it is read from main storage. The CPU directly accesses the fetch bypass buffer and can fetch the missed word without having to wait for the replacement block to be stored in cache data storage. If the CPU attempts to read the next word in the replacement block, the cache searches the directory and the block load buffer to determine whether or not a hit has occurred. Once the entire replacement block is loaded into the block load buffer, the data is wraparound-loaded into cache data storage.

Prefetch on Miss

On cache miss cycles, the μPD43608 implements a one-block lookahead algorithm that prefetches the next sequential cache data block, thus increasing the cache hit rate. Although prefetching can improve cache performance, a check must be made to determine that the block is not currently stored in the cache. The μPD43608 performs this check during each prefetch cycle, searching the cache directory for the desired prefetch block. If a hit occurs, the prefetch logic aborts the cycle. This function, which ensures that the cache is not polluted with duplicate data, can be enabled or disabled by controlling the cache status code signals during each read cycle.

Replacement Algorithm

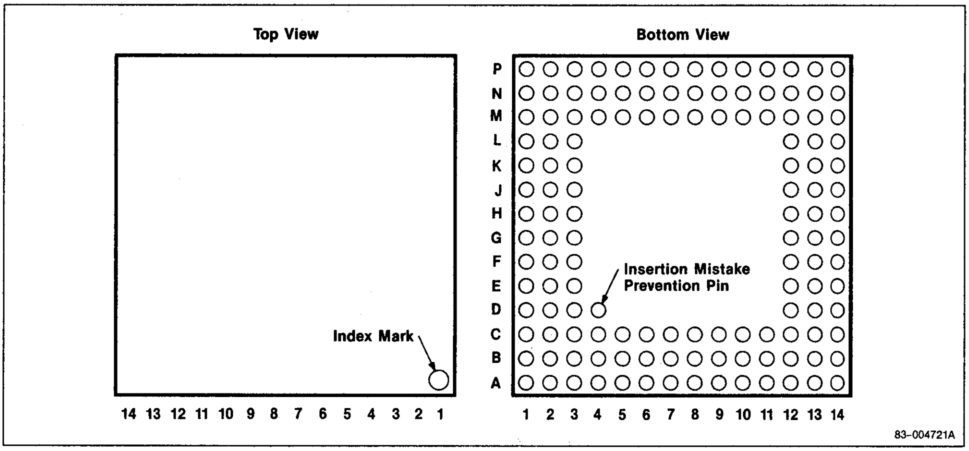
The μPD43608 uses a least recently used (LRU) replacement algorithm to determine which data block should be overwritten during a cache miss cycle. This algorithm improves cache performance by choosing the data block with the least usage to optimize the hit rate.

Main Storage Update Policies

To maintain data consistency in the storage hierarchy during each cache write cycle, the μPD43608 uses a write-through method that updates the main storage as soon as the CPU writes data to cache storage. CPU throughput is optimized by means of a one-level write buffer, which temporarily stores write data and initiates the write cycle to main storage, allowing the CPU to concurrently execute the next instruction.

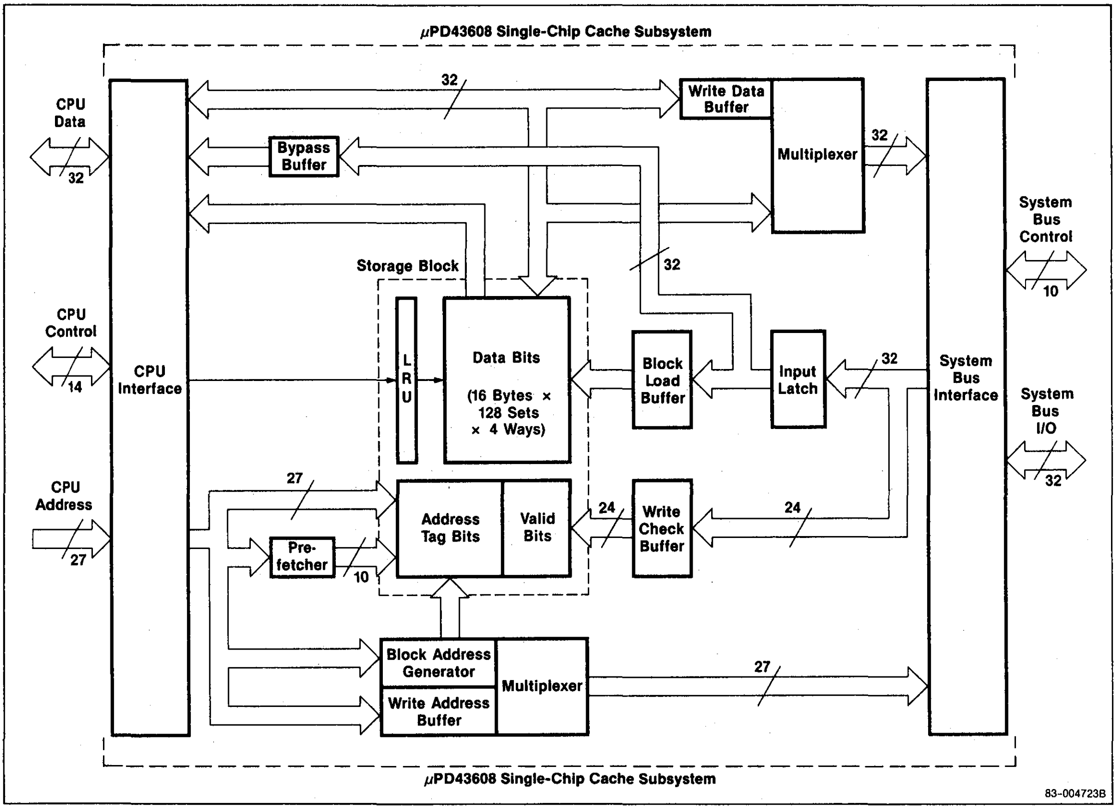
Pin Configuration

132-Pin Ceramic Pin Grid Array



Pin Number	Function	Pin Number	Function	Pin Number	Function	Pin Number	Function
A_1	D_{15}	C_6	V_{CC}	H_1	D_{30}	M_{10}	AD_{21}
A_2	D_{12}	C_7	GND	H_2	D_{31}	M_{11}	AD_{17}
A_3	D_{10}	C_8	V_{CC}	H_3	GND	M_{12}	AD_{15}
A_4	D_9	C_9	A_4	H_{12}	GND	M_{13}	AD_{13}
A_5	D_7	C_{10}	A_8	H_{13}	AD_2	M_{14}	AD_9
A_6	D_5	C_{11}	A_{11}	H_{14}	AD_1	N_1	$\overline{PBE_2}$
A_7	D_3	C_{12}	A_{14}	J_1	$\overline{PRDY}$	N_2	$\overline{SMC}$
A_8	D_2	C_{13}	A_{16}	J_2	$\overline{PAS}$	N_3	$\overline{AMC}$
A_9	A_1	C_{14}	A_{20}	J_3	$\overline{PCS}$	N_4	$\overline{BRQ}$
A_{10}	A_2	D_1	D_{24}	J_{12}	AD_7	N_5	$\overline{BACK}$
A_{11}	A_5	D_2	D_{21}	J_{13}	AD_4	N_6	$\overline{MBE_2}/\overline{WAIT}$
A_{12}	A_7	D_3	D_{18}	J_{14}	AD_3	N_7	AD_{31}
A_{13}	A_{10}	D_{12}	A_{15}	K_1	$PRD/\overline{PWT}$	N_8	AD_{29}
A_{14}	A_{12}	D_{13}	A_{19}	K_2	$\overline{CAEN}$	N_9	AD_{27}
B_1	D_{20}	D_{14}	A_{21}	K_3	ST_2	N_{10}	AD_{24}
B_2	D_{17}	E_1	D_{25}	K_{12}	AD_{11}	N_{11}	AD_{22}
B_3	D_{13}	E_2	D_{23}	K_{13}	AD_6	N_{12}	AD_{19}
B_4	D_{11}	E_3	V_{CC}	K_{14}	AD_5	N_{13}	AD_{16}
B_5	D_8	E_{12}	A_{18}	L_1	ST_1	N_{14}	AD_{12}
B_6	D_6	E_{13}	A_{22}	L_2	ST_0	P_1	$\overline{ERR}$
B_7	D_4	E_{14}	A_{24}	L_3	$\overline{PBE_0}$	P_2	$\overline{WBSY}$
B_8	D_1	F_1	D_{27}	L_{12}	AD_{14}	P_3	$MAS/\overline{MBS}$
B_9	D_0	F_2	D_{26}	L_{13}	AD_{10}	P_4	$\overline{MBE_0}/\overline{EOC}$
B_{10}	A_3	F_3	GND	L_{14}	AD_8	P_5	$\overline{MBE_1}/\overline{UERR}$
B_{11}	A_6	F_{12}	A_{23}	M_1	$\overline{PBE_3}$	P_6	$\overline{MBE_3}/\overline{CERR}$
B_{12}	A_9	F_{13}	A_{25}	M_2	$\overline{PBE_1}$	P_7	$\overline{MWA}$
B_{13}	A_{13}	F_{14}	A_{26}	M_3	PCLK	P_8	AD_{30}
B_{14}	A_{17}	G_1	D_{29}	M_4	$\overline{RST}$	P_9	AD_{28}
C_1	D_{22}	G_2	D_{28}	M_5	BCLK	P_{10}	AD_{26}
C_2	D_{19}	G_3	GND	M_6	$\overline{MDS}$	P_{11}	AD_{25}
C_3	D_{16}	G_{12}	GND	M_7	V_{CC}	P_{12}	AD_{23}
C_4	D_{14}	G_{13}	AD_0	M_8	GND	P_{13}	AD_{20}
C_5	GND	G_{14}	A_{27}	M_9	V_{CC}	P_{14}	AD_{18}

Block Diagram



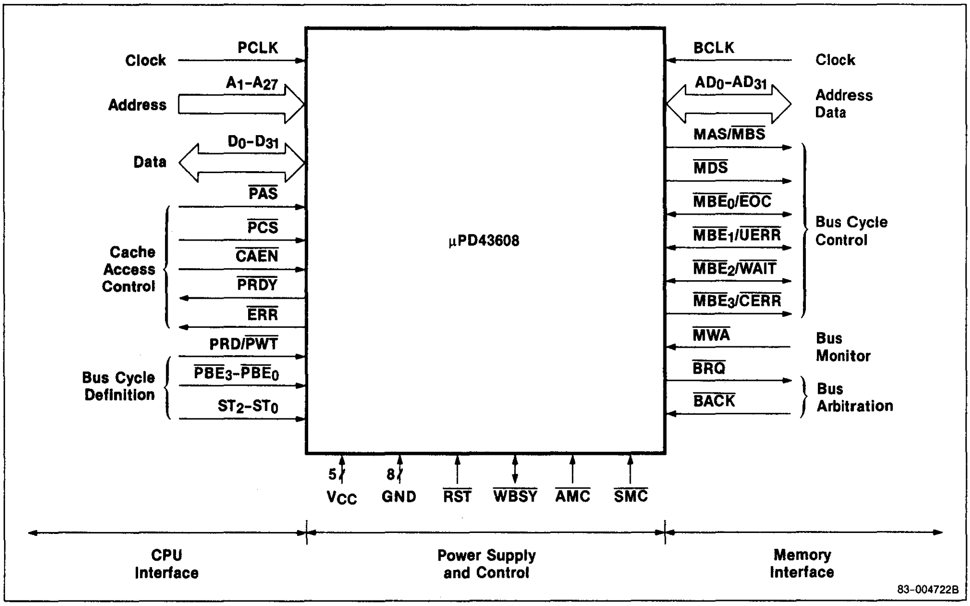
System Bus Interface

The integrated system bus interface provides an interface to contemporary microprocessor system bus architectures. The interface circuit consists of a 32-bit multiplexed address and data bus, asynchronous bus control signals, a bus lock signal, a wait signal, a correctable error function, two data transfer modes—burst and single, and a system bus clock signal. The size of the cache can be increased by connecting additional μPD43608 devices in parallel. A write buffer busy signal is daisy-chained between the parallel devices and automatically controls data transfers in multichip configurations.

Bus Monitoring

In multiprocessor system applications, maintaining data consistency is a major concern. In such a system architecture, an integrated circuit is required to monitor the system bus for any updates to main storage. When a bus master updates a location in its cache storage and writes that change to main storage, all slave processors must invalidate any stale cache data. The monitoring circuit latches all write addresses on the system bus and invalidates any cache data blocks that are not consistent with main storage.

Functional Pin Diagram



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Signal Summary

CPU Interface

Signal Name	Input/ Output	Signal Function
PCLK	I	Processor clock
A_1-A_{27}	I	Address bus
D_0-D_{31}	I/O	Data bus
$\overline{PAS}$	I	Address strobe
$\overline{PCS}$	I	Command strobe
$\overline{CAEN}$	I	Cache output enable
PRD/$\overline{PWT}$	I	Read/write
$\overline{PBE_3}$-$\overline{PBE_0}$	I	Byte enable
ST_2-ST_0	I	Status
$\overline{PRDY}$	O	Ready
$\overline{ERR}$	O	Error

Control

Signal Name	Input/ Output	Signal Function
$\overline{RST}$	I	Reset
$\overline{WBSY}$	I/O	Write buffer busy
$\overline{AMC}$	I	Test pin
$\overline{SMC}$	I	Scan path mode

Memory Interface

Signal Name	Input/ Output	Signal Function
AD_0-AD_{31}	I/O	Address/data bus
AD_{31} = MEM/$\overline{IO}$	O	Memory/IO — During an address cycle
AD_{30} = MRD/$\overline{MWT}$		Read/write — During an address cycle
AD_{29} = LOCK		Bus lock — During an address cycle
AD_{28} = PRF		Prefetch — During an address cycle
MAS/$\overline{MBS}$	O	Address strobe/bus strobe
$\overline{MDS}$	O	Data strobe
$\overline{MBE_0}$/$\overline{EOC}$	O	Byte enable 0/end of cycle
$\overline{MBE_1}$/$\overline{UERR}$	I/O	Byte enable 1/uncorrectable error
$\overline{MBE_2}$/$\overline{WAIT}$	I/O	Byte enable 2/wait
$\overline{MBE_3}$/$\overline{CERR}$	I/O	Byte enable 3/correctable error
$\overline{MWA}$	I	Main memory write check address
$\overline{BRQ}$	O	Bus request
$\overline{BACK}$	I	Bus acknowledge
BCLK	I	Bus clock

μPD71641 CACHE CONTROLLER

Description

The μPD71641 cache controller is an LSI chip whose advanced features, unequalled flexibility, and built-in reliability make the use of sophisticated caches in microprocessor-based systems practical and economical. Configurable as direct mapping, or two- or four-way, set-associative mapping, the μPD71641 supports up to 128 Kbytes of cache storage, as well as sub-block and burst mode features for efficient execution of cache updates. Implementation of the cache controller is transparent to the application program.

The μPD71641 can be easily interfaced to many general-purpose, high-performance 16- or 32-bit microprocessors. Bus monitoring and dual-comparator techniques ensure data consistency, and a write-through strategy to update main memory guarantees the best cache consistency in multiprocessor and multimaster systems. External data storage which is flexible in size and organization also means that the μPD71641 can operate with any word width. Other unique features such as multiple reliability checking, address tag parity checking, multiple hit detection, and self-diagnosis of directories greatly facilitate the implementation of a highly reliable cache subsystem. If an erroneous condition is detected, the cache controller can be degraded or disabled.

Ordering Information

Part Number	Package
μPD71641R	132-pin ceramic grid array

Features

- General-purpose interface compatibility to many high-performance 16- and 32-bit microprocessors
- Transparent implementation
- Flexible placement algorithm: direct 2- or 4-way set-associative
- Large tag storage
  - 1024 sets x 1 way x 2 sub-blocks
  - 512 sets x 2 ways x 2 sub-blocks
  - 256 sets x 4 ways x 2 sub-blocks
- Programmable sub-block size
  - Up to 64 bytes (max)
  - From 1 to 16 words
- Up to 128 Kbytes of cache storage
- Up to 4 Gbytes of main storage
- Least recently used (LRU) replacement algorithm
- Write-through strategy
- Data consistency check by means of bus monitoring
- External PURGE input to flush tag storage
- Internal error detection
  - Parity checking on tag storage
  - Incorrect match checking
  - Multiple hit checking
  - LRU output checking
- Level degradation to maximize cache system up time
- 16- and 20-MHz operation
- 132-pin ceramic pin grid array packaging

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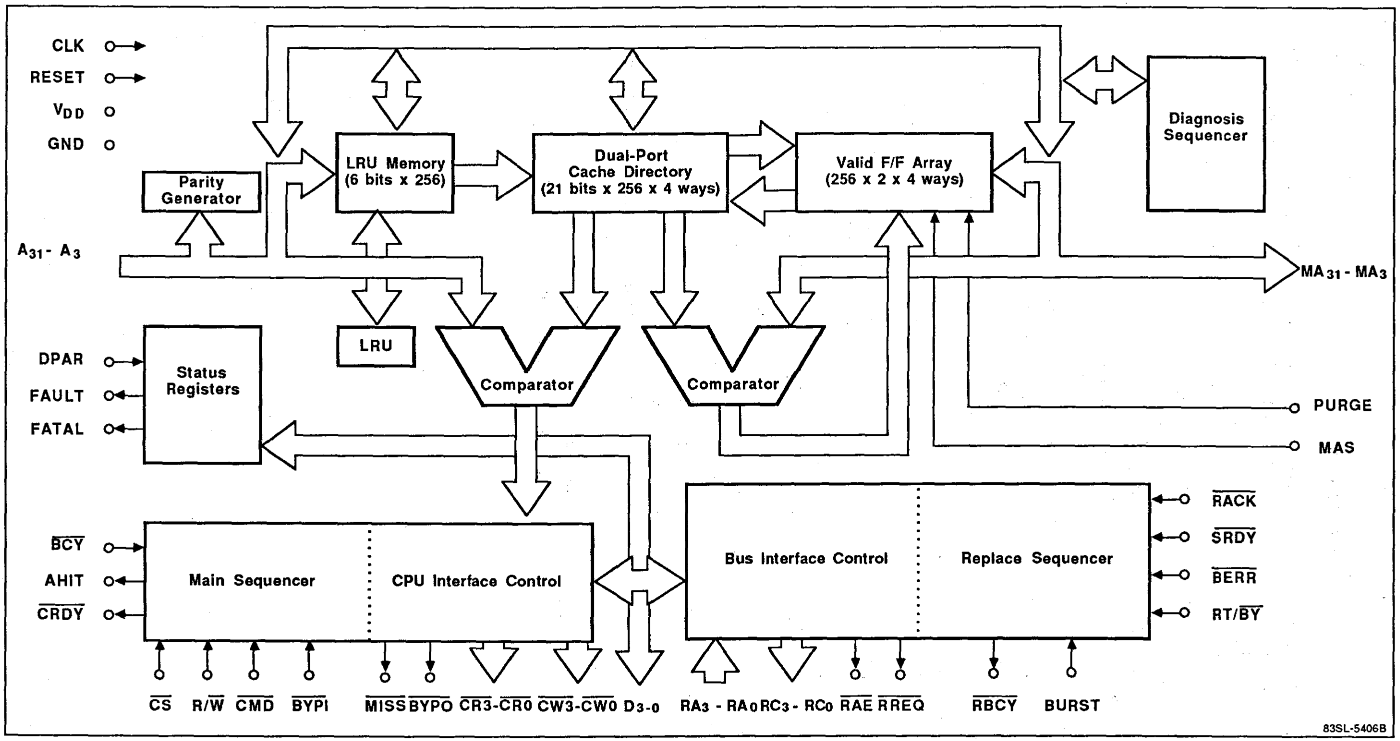
Block Diagram



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μPD7220A HIGH-PERFORMANCE GRAPHICS DISPLAY CONTROLLER

Description

The μPD7220A high-performance graphics display controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

For a more detailed description of the HGDC's operation, please refer to the 7220/7220A design manuals.

System Considerations

The HGDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the HGDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the HGDC generates the basic video raster timing, including sync and blanking signals. Partitioning areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the HGDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the HGDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the HGDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

Features

- ☐ Microprocessor interface
  - — DMA transfers with 8257- or 8237-type controllers
  - — FIFO command buffering
- ☐ Display memory interface
  - — Up to 256K words of 16-bits
  - — Read-modify-write (RMW) display memory cycles as fast as 500 ns
  - — Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light pen input
- ☐ Drawing hold input
- ☐ External video synchronization mode
- ☐ Graphic mode
  - — Four megabit, bit-mapped display memory
- ☐ Character mode
  - — 8K character code and attributes display memory
- ☐ Mixed graphics and character mode
  - — 64K if all characters
  - — 1 megapixel if all graphics
- ☐ Graphics capabilities
  - — Figure drawing of lines, arc/circles, rectangles, and graphics characters in 500 ns per pixel
  - — Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - — Two independently scrollable areas
- ☐ Character capabilities
  - — Auto cursor advanced
  - — Four independently scrollable areas
  - — Programmable cursor height
  - — Characters per row: up to 256
  - — Character rows per screen: up to 100
- ☐ Video display format
  - — Zoom magnification factors of 1 to 16
  - — Panning
  - — Command-settable video raster parameters
- ☐ NMOS technology
- ☐ Single +5 V power supply
- ☐ DMA capability
  - — Bytes or word transfers
  - — 4 clock periods per byte transferred
- ☐ On-chip pull-up resistor for VSYNC/EXT, HSYNC and $\overline{\text{DACK}}$, and a pull-down resistor for LPEN/DH

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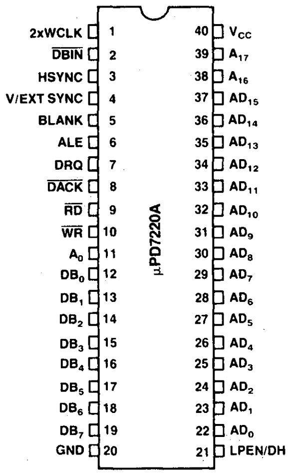
Contact your NEC sales representative for a copy of the complete data sheet.

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7220AD	40-pin ceramic DIP	6 MHz
μPD7220AD-1	40-pin ceramic DIP	7 MHz
μPD7220AD-2	40-pin ceramic DIP	8 MHz

Pin Configuration



Character Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Line counter bits 0 to 2 outputs
38	AD_{16}	Line counter bit 3 output
39	AD_{17}	Cursor output and line counter bit 4

Mixed Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Address and data bits 13 to 15
38	A_{16}	Attribute blink and clear line counter output
39	A_{17}	Cursor and bit-map area flag output

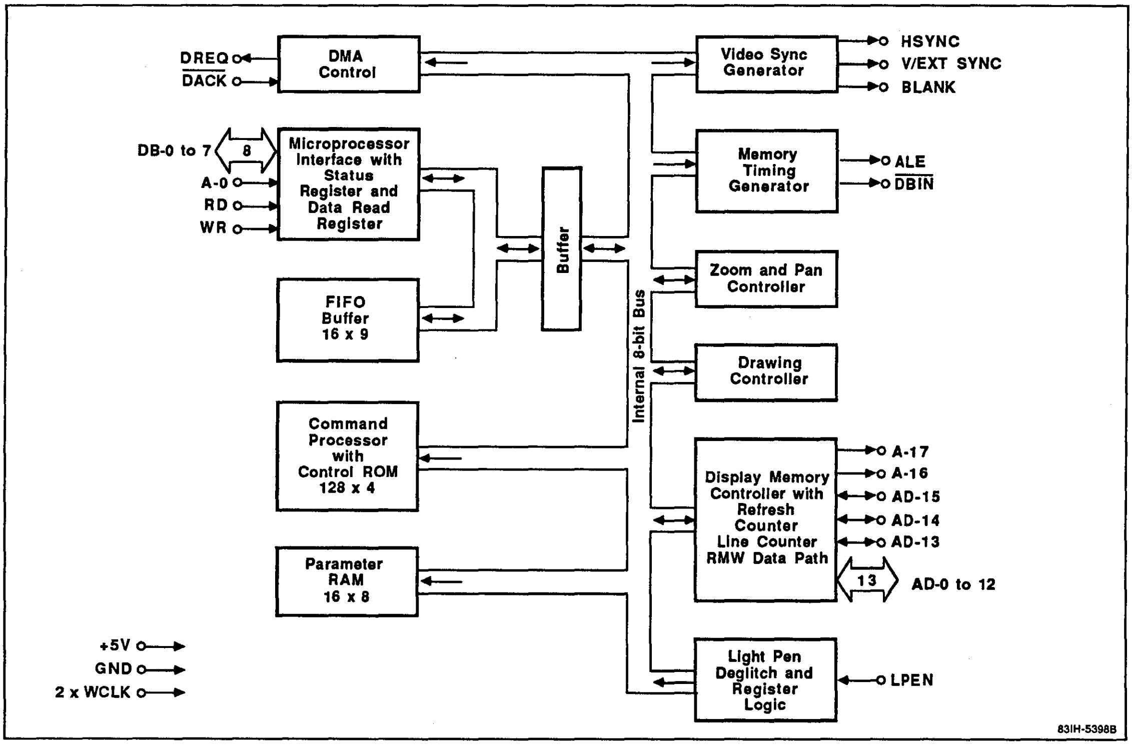
Pin Identification

Pin No.	Pin Symbol	Function
1	2xWCLK	Clock input
2	$\overline{\text{DBIN}}$	Display memory read input flag
3	HSYNC	Horizontal video sync output
4	V/EXT SYNC	Vertical video sync output or external VSYNC input
5	BLANK	CRT blanking output
6	ALE	Address latch enable output
7	DRQ	DMA request output
8	$\overline{\text{DACK}}$	DMA acknowledge input
9	$\overline{\text{RD}}$	Read strobe input for microprocessor interface
10	$\overline{\text{WR}}$	Write stobe input for microprocessor interface
11	A_0	Address select input for microprocessor interface
12-19	DB_0-DB_7	Bidirectional data bus to host micro-processor
20	GND	Ground
21	LPEN/DH	Light pen detect input drawing hold input
22-34	AD_0-AD_{12}	Address data lines to display memory
35-37	AD_{13}-AD_{15}	Utilization varies with mode of operation
38	A_{16}	Utilization varies with mode of operation
39	A_{17}	Utilization varies with mode of operation
40	V_{CC}	+5 V ±10% power supply

Graphics Mode Pin Utilization

Pin No.	Pin Symbol	Function
35-37	AD_{13}-AD_{15}	Address and data bits 13 to 15
38	A_{16}	Address bit 16 output
39	A_{17}	Address bit 17 output

Block Diagram



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NEC
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μPD72120 ADVANCED GRAPHICS DISPLAY CONTROLLER

Description

The μPD72120 advanced graphics display controller displays characters and graphics on a raster scan device from commands and parameters received from a host processor or CPU. Features of the μPD72120 include high-speed graphic drawing capabilities, video timing signal generation, large-capacity display storage control (including video buffers), and a versatile CPU interface. The features allow the μPD72120 to control graphics drawing and display of bit-mapped systems.

Features

- High-speed graphics drawing functions
  - Dot, straight line, rectangle, circle, arc, sector, and segment
  - Ellipse, ellipse arc, ellipse sector, and ellipse segment
- Filling
  - Area filling (high-speed processing in word units) of triangle, trapezoid, circle, ellipse, and rectangle
  - Painting of any arbitrary enclosed area (bit boundary retrieval)
- Data transfer in display storage
  - Multiplane transfers
  - Data transformation (90°, 180°, 270° rotation and reversal)
  - Multiwindow transfers
  - Maximum word transfer speed of 500 ns
- Image processing
  - Slant
  - Arbitrary angle rotation
  - 16/n enlargement and n/16 shrinkage (where n is any integer from 1 through 16)
- Position specification by X-Y coordinates
- Logical operations between planes
- Video timing signal generation
  - Display clock for video synchronizing signal generation
  - Graphics drawing clock for high-speed processing
  - External synchronization capability
- Large-capacity display memory
  - Display memory bus interface with 24-bit address and 16-bit data bus for addressing up to 16 Mwords at 16 bits per word
  - Video buffer control
  - Display memory bus arbitration
- Host processor (CPU) interface
  - System bus interface with 20-bit address bus and 8- or 16-bit data bus
  - Data transfer with external DMA controller
    - From system memory to display memory (PUT)
    - From display memory to system memory (GET)
  - High-speed pipeline processing with preprocessor before drawing processor
  - CPU memory or I/O mapping of internal registers and display memory for efficient system interface
- 8-MHz system clock
- CMOS technology
- Single +5-volt power supply
- 84-pin PLCC, 94-pin plastic quad flatpack, and 132-pin ceramic PGA packaging

Ordering Information

Part Number	Package
μPD72120L	84-pin plastic leaded chip carrier (PLCC)
μPD72120J-5BG	94-pin plastic quad flatpack
μPD72120R	132-pin ceramic pin grid array

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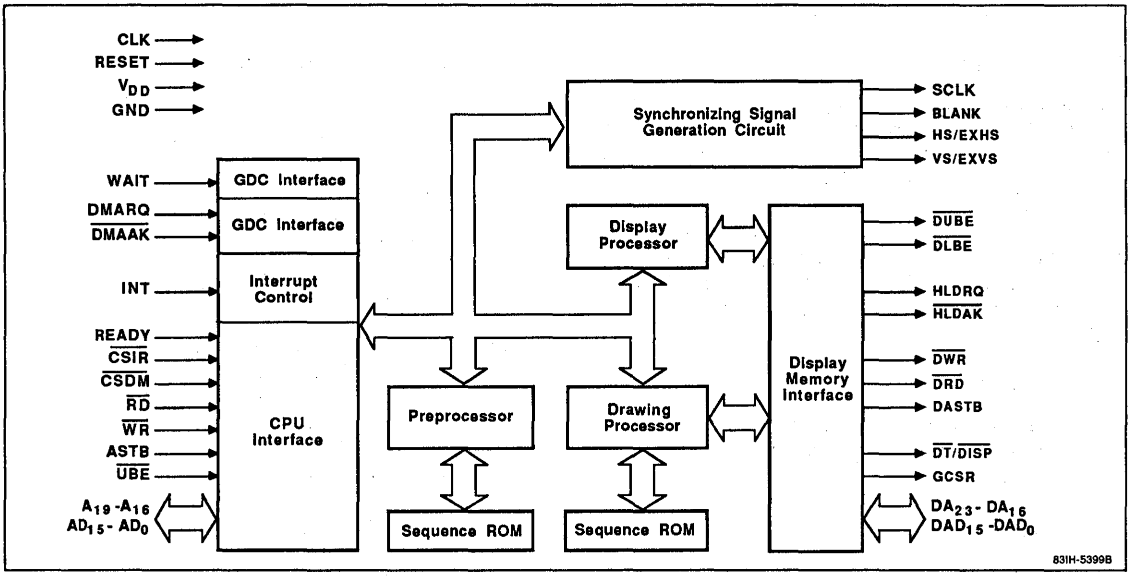
Contact your NEC sales representative for a copy of the complete data sheet.

Block Diagram



μPD72185 ADVANCED COMPRESSION/ EXPANSION PROCESSOR

Description

The μPD72185 is a high-speed processor that compresses and expands the binary image data necessary in facsimile equipment, electronic filing systems, and other image processing systems. Direct management of image memory by means of an on-chip DMA controller allows the μPD72185 to process images by line, block or page, as directed by commands from the host CPU.

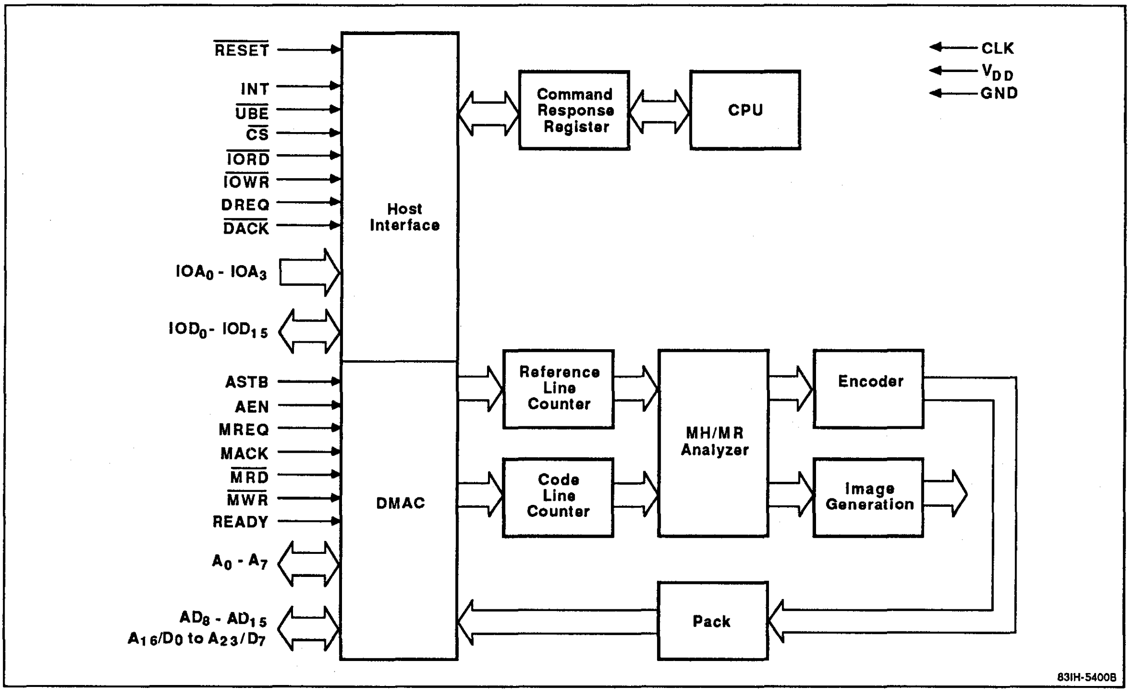
Features

- High-speed compression and expansion processing of CCITT-standard test chart (A4 size at 400 PPI x 400 LPI) in 1 second
- Encoding and decoding of CCITT-standard MH, MR, and MMR methods
- Maximum 32K pixels in main scanning section
- Main scanning direction
  - x 2 enlargement on encoding
  - x 1/2 shrinkage on decoding
- Subscanning direction
  - x 2 and x 4 enlargement on encoding
  - x 1/2 and x 1/4 shrinkage on decoding
- Bit boundary processing
- Multitasking function
- High-speed data processing (internal 4-stage basic pipeline)
- Dual bus system
  - 24-bit address bus and 8- or 16-bit data bus on image memory side
  - 8- or 16-bit data bus on host CPU side
- On-chip DMA controller
- CMOS technology
- Single +5-volt power supply
- Maximum 8-MHz system clock
- Standard 750-mil, 64-pin plastic shrink DIP and 68-pin PLCC packaging

Ordering Information

Part Number	Package
μPD72185CW	64-pin plastic shrink DIP
μPD72185L	68-pin plastic leaded chip carrier (PLCC)

Block Diagram



NEC

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APPLICATION NOTE 54 μPD42505 LINE BUFFER FOR COMMUNICATIONS SYSTEMS

Introduction

The current trend in storage devices is toward larger, faster, better-performing products. There is a complementary trend toward the development of storage devices designed for specific purposes. The video buffer is an example of a dedicated device. Line buffers, field (frame) buffers for TV and broadcast equipment, and graphics buffers for computers are examples of video storage devices. Table 1 shows some of NEC's dedicated video buffers.

Table 1. Video Buffers

Function	Product	Storage Configuration	Serial Cycle Time	Application in Video/Optical Systems
Line buffers	μPD42505	5048 x 8	50 or 75 ns	Line storage in facsimile machines, copiers, and scanners
	μPD41101/μPD42101	910 x 8	34 or 69 ns	Double-speed scan conversion for NTSC TV, luma/chroma separation
	μPD41102/μPD42102	1135 x 8	28 or 56 ns	Double-speed scan conversion for PAL TV, luma/chroma separation
Field buffer	μPD42270	263 x 910 x 4	60 ns	Image field storage
Dual-port graphics buffers	μPD41264	64K x 4/256 x 4	40 or 60 ns	High-speed drawing device
	μPD42274/μPD42273	256K x 4/512 x 4	30 or 40 ns	
Triple-port graphics buffer	μPD42232	32K x 8/256K x 1/128 x 8	40 or 60 ns	High-speed drawing/image processing device
Bidirectional data buffer	μPD42532	32K x 8	100 ns	Data transfer rate conversion

This application note introduces the μPD42505, a high-speed serial access device with the same general interface specifications as those of the μPD41101. The μPD42505 was developed specifically for office automation equipment that handles a large amount of data in each horizontal line, equipment such as G3 and G4 digital facsimile machines, high-performance copiers, and image scanners.

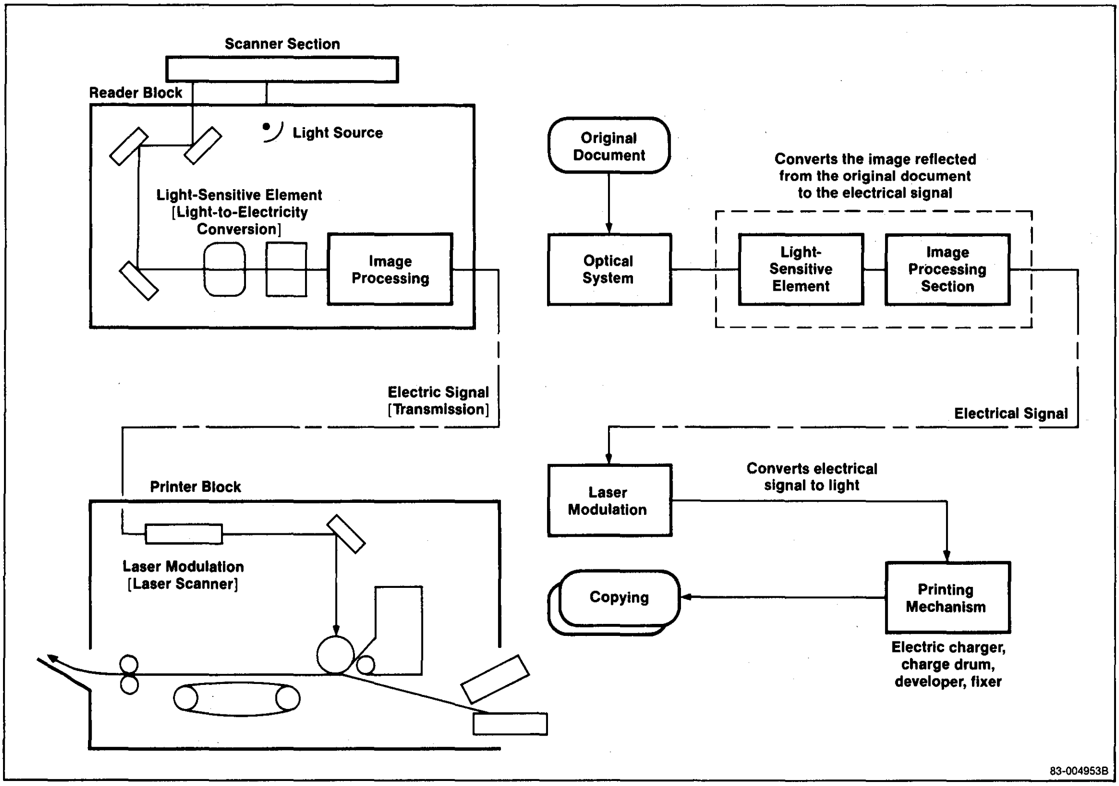
There has been a great deal of technical progress toward higher quality and performance in the development of this image-processing equipment. For example, there are already advances in image quality using two-dimensional filtering, image contraction and expansion, and high-speed video signal transfer. The μPD42505 achieves optimal processing with a storage array of 5048 x 8 bits, and by use of an internal algorithm to read out data in the order in which it was input. The fast cycle time of 50 ns allows the μPD42505 to perform various types of image processing.

Figure 1 shows a typical application for the μPD42505 using a digital copier as an example.

A digital copier mainly consists of a reader and a printer section. The image reflected from the original document placed in the scanner section is input to an image sensor (e.g., a CCD or contact-type image sensor) and photoelectrically converted to a digital signal. The digital signal is then input to the image processing section for image quality improvement and processing. The electronic image signal processed in the reader block is sent to the printer block, converted to light in the laser modulation section, developed, fixed, and printed out. If a communication facility is added to this copier, it can function as a facsimile machine.

Digital copiers and facsimile machines configured in this way can use dedicated video buffers in the image processing or transmission section.

Figure 1. Configuration and Data Flow in a Digital Copier

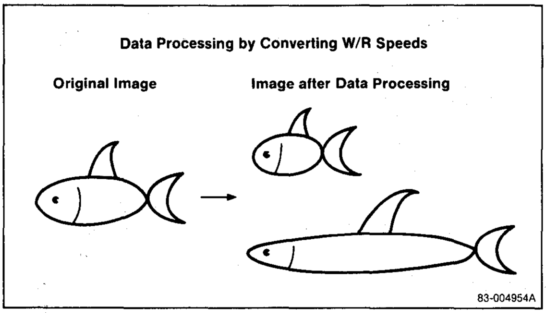


Uses for the μPD42505

The following discussion describes the types of applications for which the μPD42505 was developed: frequency (speed) conversion, a data delay line for one horizontal scanning line, and buffering for data transfer operations in a simple configuration with simple control.

Consider the need for a device that asynchronously converts the read and write speed for frequency conversion, e.g., a serial access device used for image contraction or expansion, with a word length of one to two horizontal lines. The buffer must be written to and read from asynchronously and at different rates. High speed is also a requirement. Figure 2 illustrates a frequency conversion application.

Figure 2. Frequency Conversion



Another application might require a data delay line with a delay length of one to two lines. This type of buffer could be used for image quality improvement in two-dimensional filtering, especially for filtering in the vertical direction, because it could be written to and read from simultaneously in synchronization with a single clock signal. Figure 3 illustrates two-dimensional filtering.

A third application is a buffer for data transfer operations. This application requires a device large enough to store the amount of data handled, with the capability to read and write asynchronously, simultaneously, and at different speeds. An output such as a flag to indicate the amount of data in the storage array might also be required. Figure 4 illustrates buffering for data transfer.

Figure 3. Two-Dimensional Filtering

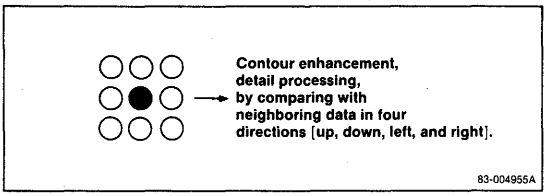
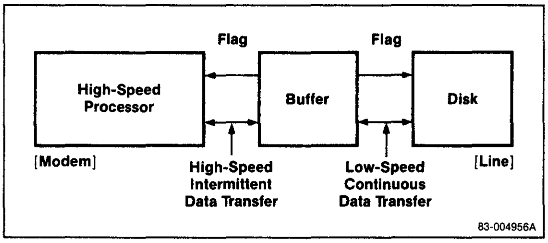


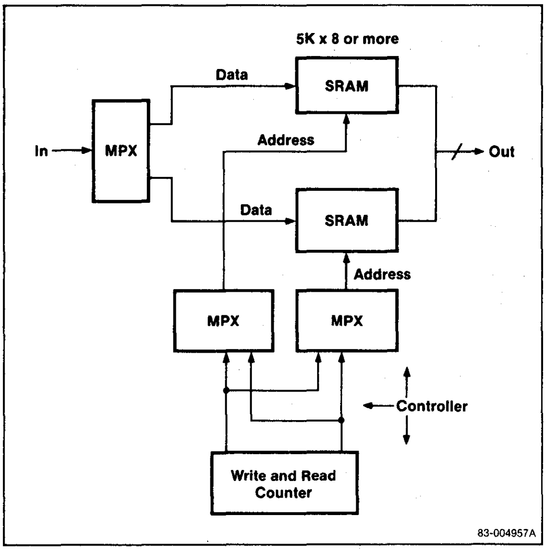
Figure 4. Data Transfer Buffering



These applications typically require a double-buffer configuration using high-speed SRAMs for data storage in bits, as shown in figure 5.

In the first phase, data is written to the first SRAM while data in the second SRAM is read simultaneously, alternating operations between the two SRAMs. However, this operation requires components such as read and write address counters, a multiplexer to switch address signals according to the read and write state of each device, a multiplexer to switch write data input and read data output, and a sophisticated controller to control the SRAMs and the other components. The μPD42505, by performing some of these functions itself, considerably simplifies these applications.

Figure 5. Typical System Using High-Speed SRAMs



Features of the μPD42505

The μPD42505 is a 5048-word x 8-bit high-speed serial access device that uses 1.5-μm CMOS processing and dual-port storage cell circuits allowing simultaneous, asynchronous read and write cycles at different speeds. An internal algorithm makes an external address signal unnecessary.

Read and write operations are fully and independently controlled by their own set of control signals. The storage array length of 5048 words meets the size required to sample one line of JIS A3-size paper on the shorter side (297 mm) with a sampling rate of 16 dots/mm (400 dots/in). On the longer side (418 mm), the sampling rate is 12 dots/mm (300 dots/in). The μPD42505 can easily process document data for each line. The configuration of 8 bits to 1 word corresponds to the number of bits for one sampling point, which allows the device to process natural-looking images.

The μPD42505 can be used in video applications that require high-speed processing because of its minimum simultaneous write/read cycle time of 50 ns and maximum access time of 40 ns. For example, the cycle time of 50 ns is fast enough to digitally process an NTSC or PAL composite video signal at a sampling rate of four times the color subcarrier frequency ($4f_{SC}$).

The μPD42505 is particularly suitable for use as a digital delay line with a delay length of up to 5048 cycles in one-cycle steps. The device is mounted in a 300-mil, 24-pin plastic slim DIP. The 300-mil width allows high-density mounting.

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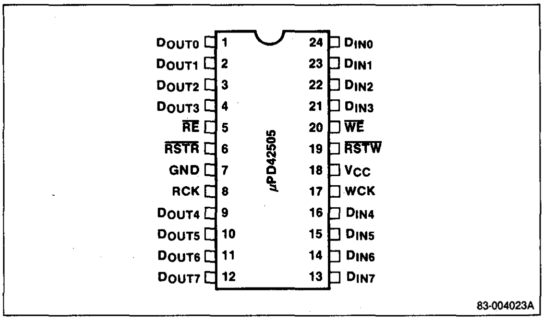
μPD42505 Pinout

Pins 1 through 12 control read operation (D_{OUT0}-D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK) and the GND pin. Pins 13 through 24 control write operation (D_{IN0}-D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK) and the power supply (V_{CC}).

$\overline{RSTW}$ and $\overline{RSTR}$ are control signal inputs that reset the internal read and write address pointers to starting address 0. These pins are useful for initializing the chip after power-on or for returning the address to 0.

Figure 6. μPD42505 Pin Configuration



$\overline{WE}$ and $\overline{RE}$ are control signals that enable (low) or disable (high) write and read operation. When $\overline{WE}$ is high, write operation is disabled and the write address stops at the current value. When $\overline{RE}$ is high, read operation is disabled, the read address stops at the current value, and the output goes to high impedance. $\overline{WE}$ and $\overline{RE}$ may be input at any time, but they are latched in each cycle at the rising edge of WCK or RCK, respectively.

WCK and RCK are the write and read system clock inputs. One write or read cycle is executed in synchronization with each WCK or RCK input when $\overline{WE}$ or $\overline{RE}$ is low. The write or read address is incremented internally in single steps and wraps around automatically from 5047 to 0.

D_{IN0}-D_{IN7} are the write data input pins. Write data is clocked into the chip at the rising edge at the end of the WCK cycle. D_{OUT0}-D_{OUT7} are the read data output pins. Read data is output when the access time has elapsed from the rising edge at the beginning of the RCK cycle.

Read and Write Timing

Input a low-level signal to $\overline{\text{RSTW}}$ (for writing) or $\overline{\text{RSTR}}$ (for reading) to satisfy the setup and hold times measured from the rising edge at the beginning of the WCK or RCK cycle. This returns the cycle to starting address 0. Figure 7 shows read and write timing for the μPD42505.

As the figure shows, the $\overline{\text{RSTW}}$ or $\overline{\text{RSTR}}$ signal can end in one write or read cycle or can be repeated for successive write or read cycles. Repeating the reset cycle holds the address at 0. The address is incremented to address 1 only in a cycle when $\overline{\text{RSTW}}$ or $\overline{\text{RSTR}}$ is set high at the rising edge of the WCK (RCK) cycle. For write reset, the write data clocked in the last reset cycle is written to address 0. For read reset, the data in address 0 is output continuously. After the reset, write or read operation continues as the address is incremented by 1 for each cycle in synchronization with its appropriate clock. When the internal address reaches 5,047 (i.e., when write or read cycles are executed 5,048 times), the address returns to address 0 and the write or read operation starts over at that point.

Speed Conversion. Independently controlling the read and write operations of the μPD42505 allows you to perform speed conversion. For example, when the read and write addresses are initialized by $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$, data is written in synchronization with WCK and the write data is written to the chip from device address 0. Data written can be read out from address 0. In this case, the reset signal input timing and the clock signal speed (cycle time) can be independently controlled for read and write operation. The μPD42505 can be used for speed (frequency or time axis) conversion by outputting the data previously input with an arbitrary drive frequency and time at a different drive frequency and time.

Digital Delay Line. To use the μPD42505 as a digital delay line, input the same clock to WCK and RCK and reset the read and write cycles in parallel. Written data is read out after 5,048 cycles to provide a 5,048-cycle digital delay line.

There are three ways to control the delay length:

- By controlling the $\overline{\text{WE}}$ and $\overline{\text{RE}}$ signals
- By inputting $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ at different times (the delay length is determined by the offset between the signals)
- By changing the reset signal interval when $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ are concurrently controlled (the delay length is determined by the reset signal input interval)

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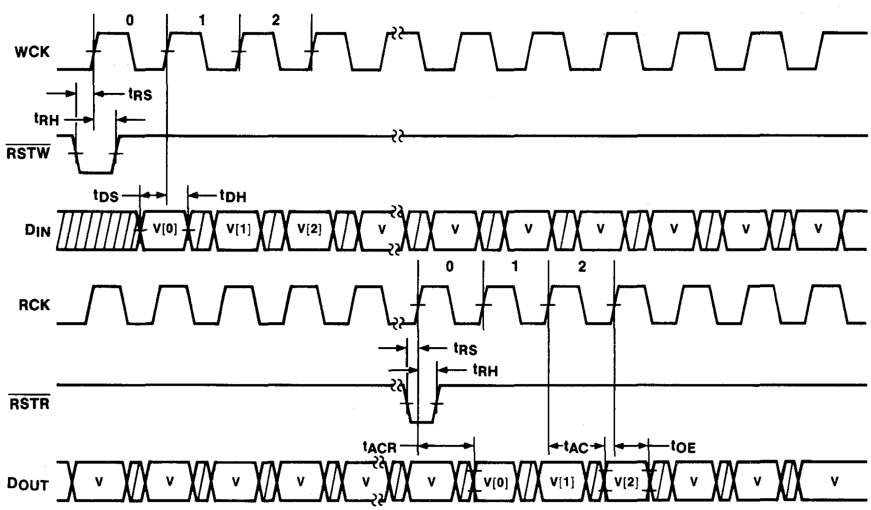
Figure 7. Read and Write Timing



Notes:
[1] $\overline{\text{WE}}$ = $\overline{\text{RE}}$ = V_{IL}.
[2] V = Valid data.

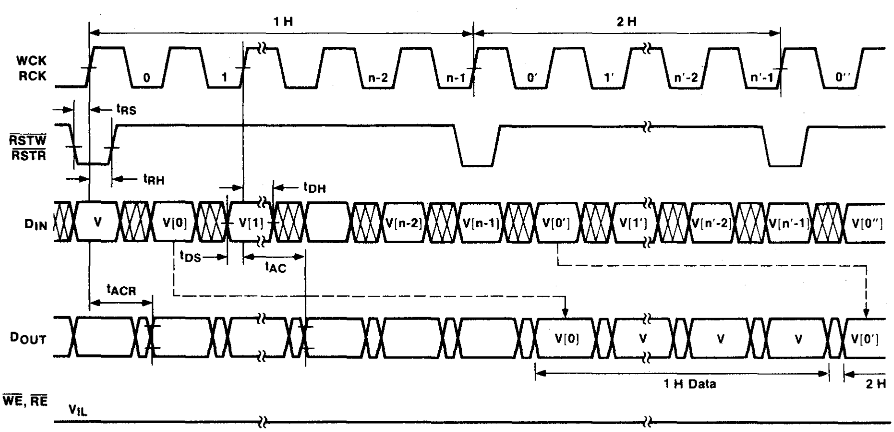
83-004958B

The delay length can be changed in one-cycle steps by controlling $\overline{WE}$ and $\overline{RE}$. When $\overline{WE}$ and $\overline{RE}$ are high, write and read operation is disabled. The write and read addresses remain where they were when the operations were disabled, regardless of WCK and RCK.

When $\overline{RSTW}$ and $\overline{RSTR}$ are used to control the delay length, the data written at address 0 when $\overline{RSTW}$ is input is read out from address 0 when $\overline{RSTR}$ is next input. The offset between $\overline{RSTW}$ and $\overline{RSTR}$ determines the delay length.

In the third method, changing the reset signal input interval, the same signal is used for WCK and RCK so that $\overline{RSTW}$ and $\overline{RSTR}$ are controlled together. The data, written after a reset signal, is read out after the next reset signal in the order it was written. This interval determines the delay length. For example, if the reset signal is input every 4,800 cycles, the delay length is 4,800 cycles. Figure 8 shows the timing for this method.

Figure 8. Controlling Delay Length with the Reset Interval



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

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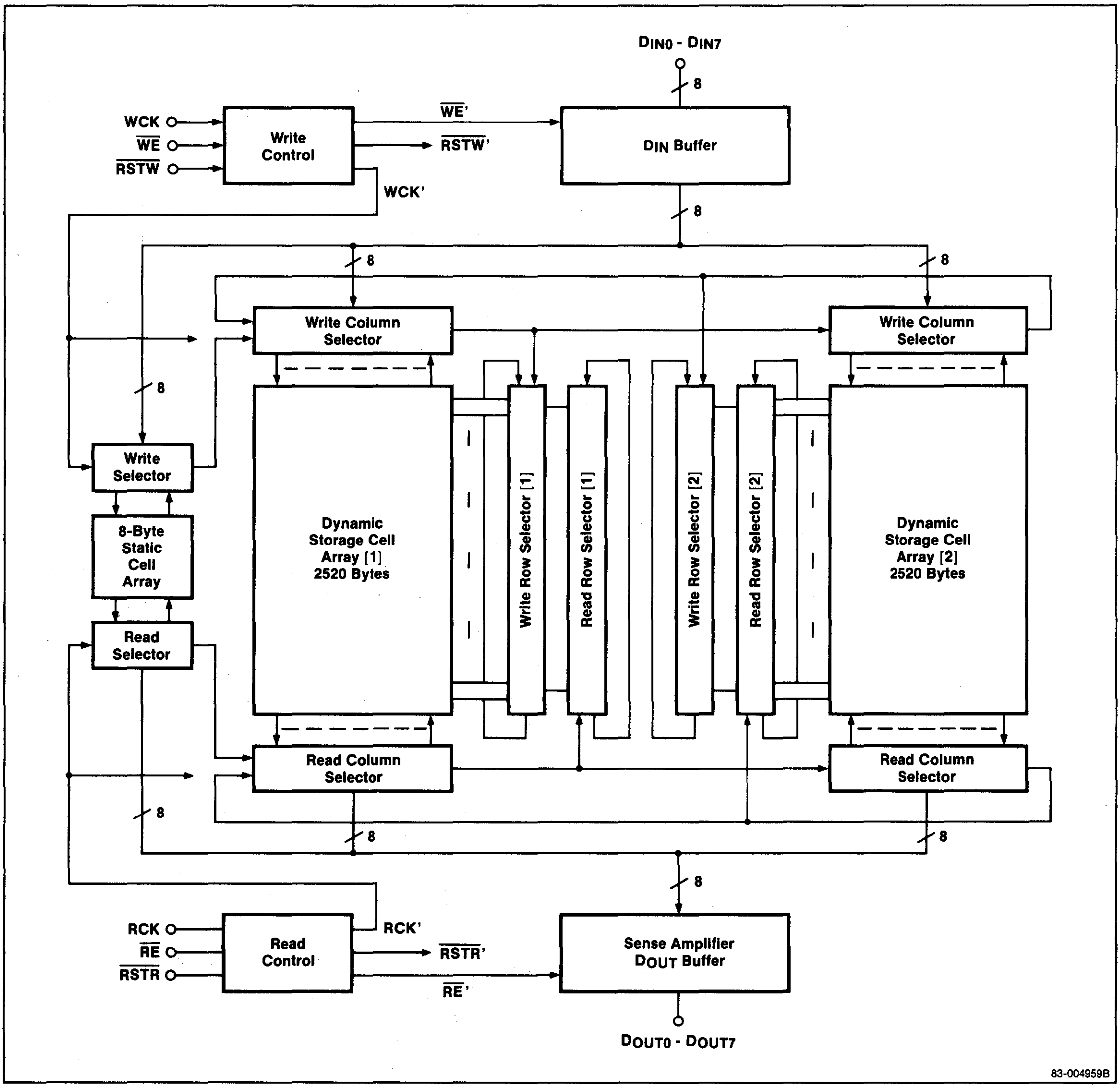
Functional Blocks

The write data input from pins D_{IN0}-D_{IN7} goes through the D_{IN} buffer and is serially written to either a static cell in an 8-byte configuration, or a dynamic cell in a 5,040-byte configuration, one byte (8 bits) at a time, in synchronization with WCK. The data read out from these cells is serially output from the D_{OUT} pins through the sense amplifier and the D_{OUT} buffer, one byte at a time, in synchronization with RCK. The read and write control circuits control these operations.

Figure 9. μPD42505 Block Diagram



Storage Cells

The μPD42505 uses dual-port storage cells to allow read and write cycles to be executed asynchronously and at different speeds. Figure 10 shows a circuit diagram of a static dual-port storage cell, and figure 11 shows a dynamic dual-port storage cell.

In the static cell, read and write data are input as a differential signal so that it can operate at a higher speed. The circuit size is larger because it requires more components.

Figure 10. Static Dual-Port Storage Cell

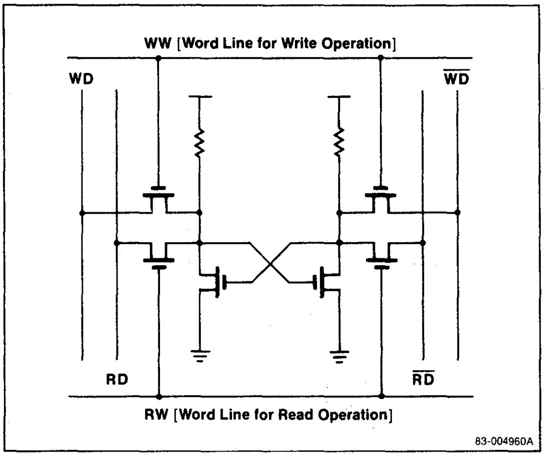
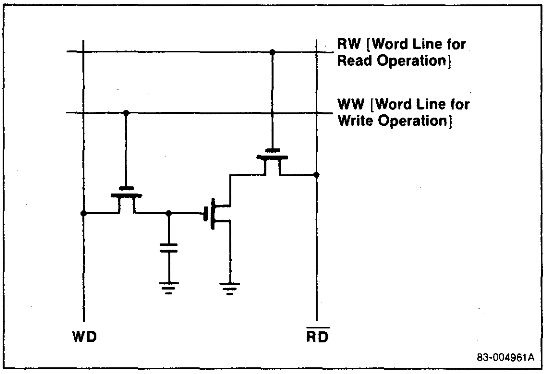


Figure 11. Dynamic Dual-Port Storage Cell



The dynamic cell has only one bit line for read operation and one for write operation. It requires a longer data sense phase, reducing the speed. However, it can be configured with fewer components.

Both types of cells are used in the μPD42505 to exploit the advantages of each. Other than initializing the internal address pointer to the starting address with the reset signal, the μPD42505 is configured so that the internal address is incremented one bit at a time and data is serially accessed. After a reset operation (immediately changing the addressing sequence), a static dual-port storage cell that can operate at higher speed is accessed. Simultaneously or subsequently, a dynamic cell is used as a pipeline, allowing both types of cells to be accessed at high speed.

Pipeline operation refers to an instance where the word line (row) to be selected next is set to the selected level in advance, so that it can be written or read at high speed in the time required to select a column in dynamic static-column mode.

Shift registers are used as read and write column and row selectors to enable the sequential selection of write or read addresses in pipeline processing.

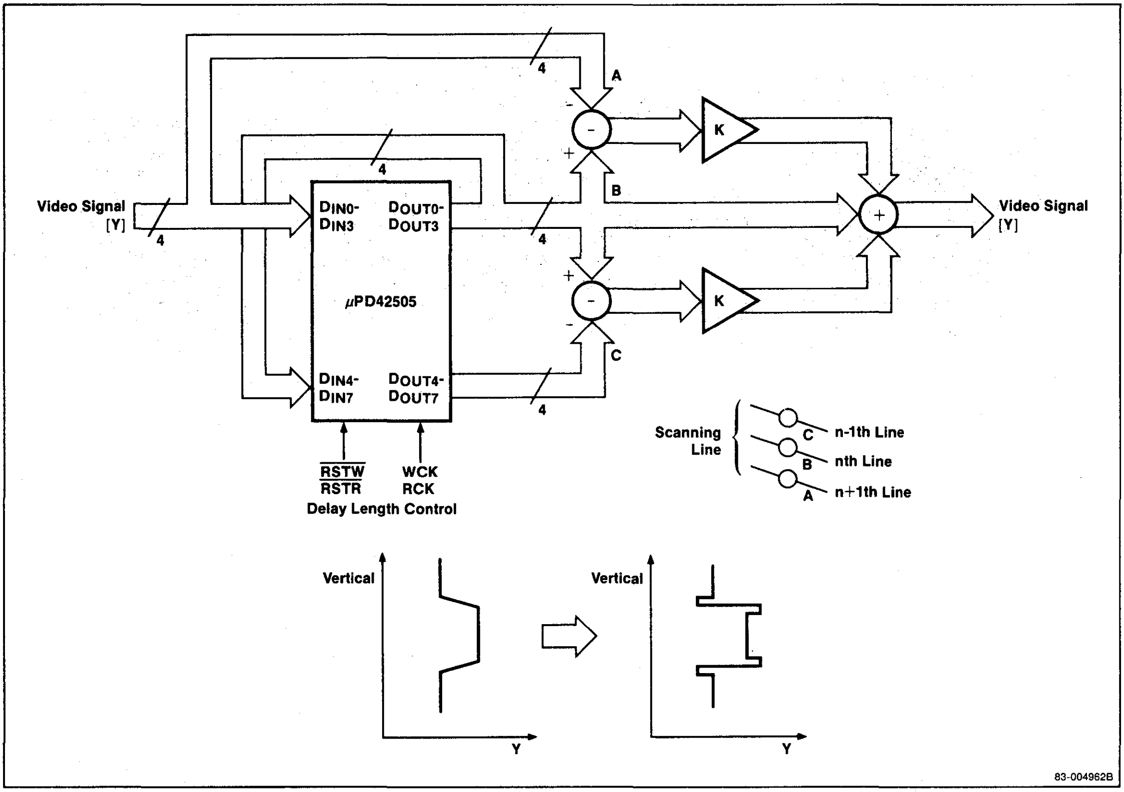
Applications

Signal processing technology aims toward higher quality in the development of digital copiers and facsimile machines. As examples, consider image quality improvement processing such as the adaptive bilevel control technique, which produces a stable and accurate binarization regardless of the original document type, and the two-dimensional equalizing filter, which corrects fading in photoelectric signal conversion. The μPD42505 fits easily into these processes. It can also reduce system size and cost.

Two-Dimensional Filter

In handling an image with half-tones, e.g., a photograph, there is some deterioration in the image quality, such as thin lines and small characters fading out; fading is usually caused by the lens or photoelectric signal conversion system in a CCD sensor. A two-dimensional filter is very effective in enhancing contours where contrast changes sharply and in reducing the fading problems. Figure 12 shows a contour enhancement circuit.

Figure 12. Contour Enhancement Circuit

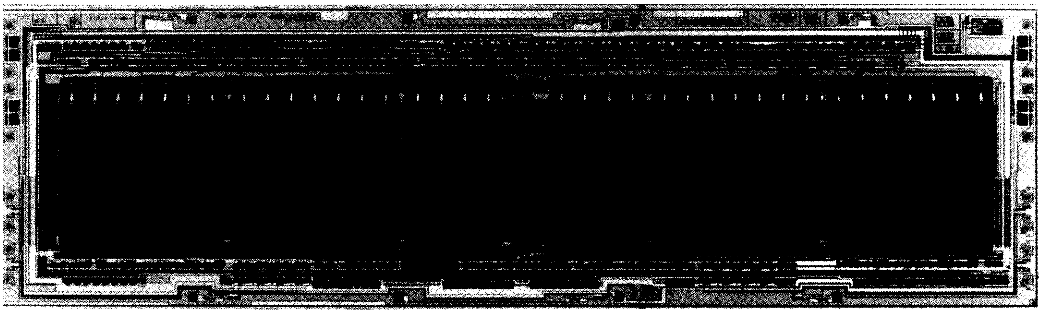


In this example, the video input is handled as a 4-bit signal so that a circuit with a delay length equal to two scanning lines can be configured with a single µPD42505. Adding adders or subtractors and multipliers to the µPD42505 completes the contour enhancement configuration.

The video signal of the n+1th line (delayed by one scanning line) is input to D_{IN0}-D_{IN3} and output from D_{OUT0}-D_{OUT3} as the nth line. Applying this output directly to D_{IN4}-D_{IN7} delays the video signal another scanning line before it is output from D_{OUT4}-D_{OUT7} as the n−1th line. There is a delay of one scanning line between the signal input to D_{IN0}-D_{IN3} and the signal output from D_{OUT0}-D_{OUT3}, and a delay of another scanning line between the signal input to D_{IN4}-D_{IN7} and the signal output from D_{OUT4}-D_{OUT7}. Processing these signals in the adders and multipliers provides contour enhancement in the vertical direction. You can control the delay length by controlling the reset signals ($\overline{RSTW}$ and $\overline{RSTR}$) and the clock signals (WCK and RCK) in common, and by controlling the reset signal input interval.

The delay length of one scanning line is used in various applications for two-dimensional data processing. The µPD42505 can also be used in applications such as VTR jitter compensation (time axis variation) caused by the variance in head drum rotation rate or the expansion or shrinkage of the tape, applications requiring variable-length delay lines to contract or expand a video image in the horizontal direction, applications involving the synchronization of two or more digital signal inputs, and as a line buffer in data transfer operations between devices using different data transfer rates.

Figure 13. μPD42505 5048 x 8 Line Buffer



NEC

NEC Electronics Inc.

APPLICATION NOTE 55
μPD41101/μPD41102
HIGH-SPEED LINE BUFFERS

Introduction

The μPD41101 and μPD41102 are high-speed serial access line buffers organized as 910 words x 8 bits and as 1135 words x 8 bits, respectively. An algorithm that enables data to be read out in the order in which it was input makes these devices suitable for use as data delay lines or for converting data transfer rates, e.g., as buffer storage used for data transfer between devices with different data processing rates.

The μPD41101 can process an NTSC composite video signal (the TV system used in Japan and North America) that has been previously digitized. The fast access times of the device allow a sampling frequency of four times the color signal subcarrier frequency (where f_{SC} = 3.58 MHz and $4f_{SC}$ = 14.32 MHz) for each scanning line to be used. This means that 910 addresses are required for each scanning line when sampling at $4f_{SC}$.

The μPD41102 can process a PAL composite video signal (the TV system used in European countries other than France) that has been previously digitized. This device also uses a sampling frequency of four times the color signal subcarrier frequency (where f_{SC} = 4.43 MHz and $4f_{SC}$ = 17.72 MHz) for each scanning line, which means that 1135 addresses are required for each scanning line when sampling at $4f_{SC}$.

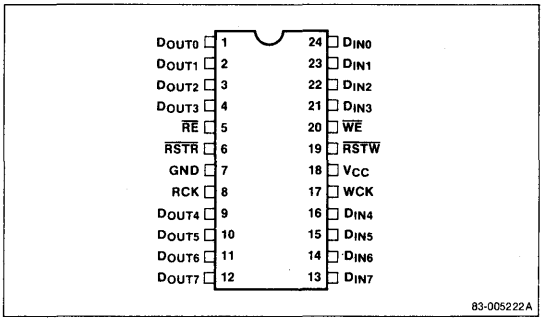
Figure 1 shows the pin configuration for these devices. The D_{IN0}-D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK pins control write operation, while D_{OUT0}-D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK control read operation. The pins are organized to operate asynchronously and at different speeds simultaneously. A built-in serial address generator automatically generates read and write addresses so that an address need not be supplied externally.

High-Speed Operation

Write and Read Operation

Write and read cycles are executed identically. One address of data (8 bits) is written or read in one cycle in synchronization with WCK or RCK when $\overline{WE}$ or $\overline{RE}$ is low. The write or read address is incremented by 1 at the falling edge of each write or read clock. Write data must satisfy setup and hold times as measured from the rising edge of WCK.

Figure 1. Pin Configuration



The $\overline{RSTW}$ and $\overline{RSTR}$ reset signals initialize the write and read address pointers to 0. A reset signal must be input to satisfy the setup and hold times as measured from the rising edge of WCK or RCK. Once the address is initialized, a write or read cycle is executed in synchronization with its respective clock and the pointer is incremented by 1. In the μPD41101, the pointer returns to 0 after address 909. In the μPD41102, the pointer returns to 0 after address 1134.

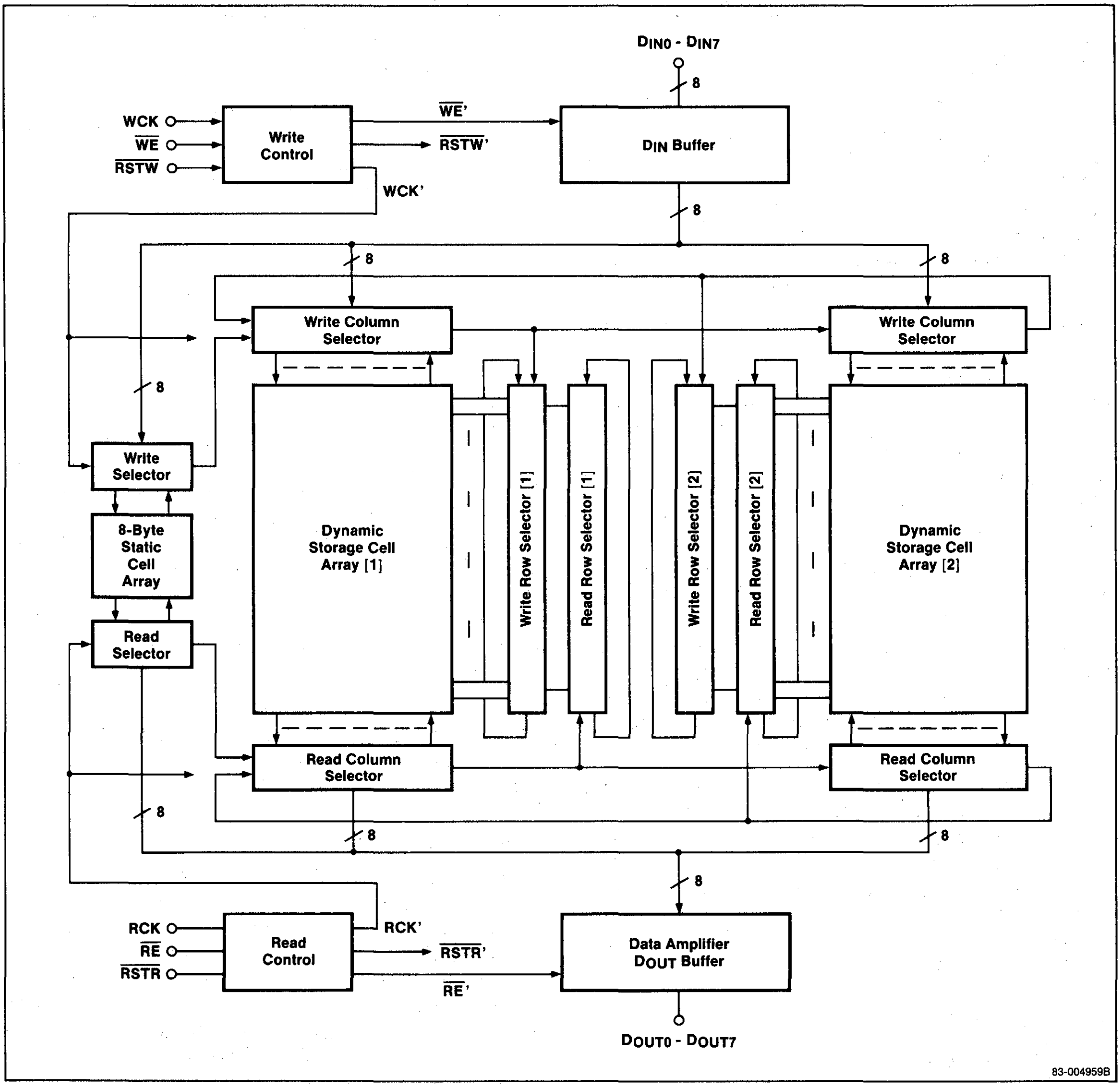
When $\overline{WE}$ is high, write operation is disabled and the line address is held regardless of the status of WCK. When $\overline{RE}$ is high, read operation is disabled, the output goes to high impedance, and the line address is held regardless of the status of RCK.

Functional Blocks

The write data from D_{IN0}-D_{IN7} goes through an input buffer and is serially written to either a static cell in an 8-byte configuration, or a dynamic cell in an 1136-byte configuration, one byte (8 bits) at a time, in synchronization with WCK. The data read from these cells is serially output from the D_{OUT} pins through a sense amplifier and the output buffer, one byte at a time, in synchronization with RCK. The read and write circuits control these operations.

WCK, $\overline{WE}$, and $\overline{RSTW}$ are input to the write control circuit. RCK, $\overline{RE}$, and $\overline{RSTR}$ are input to the read control circuit. These segments are composed of simple gate circuits (figure 2).

Figure 2. Block Diagram of the μPD41101 and μPD41102



Storage Cells

The μPD41101 and μPD41102 use dual-port storage cells to execute read and write cycles asynchronously and at different speeds (figures 3 and 4).

Static Cell Organization. In the static cell, two pairs of transfer gates (one pair each for read and write operation) are connected to the flip-flop in the middle. The other end is connected to a pair of bit lines for read operation (RD, $\overline{RD}$), and another pair for write operation (WD, $\overline{WD}$). One word line each for RW and WW are connected to the transfer gate pins.

When the word line for a write cycle (WW) goes to the selected level, and write data is applied to the pair of bit lines (WD, $\overline{WD}$) of the selected column, a write cycle is executed on the cell where the row (word line) and column (bit line) intersect.

A read cycle is executed independently. When the word line goes to the selected level (RW), data is transferred to the bit line pair (RD, $\overline{RD}$) through a transfer gate. Data is selected by the column signal and read externally. Data in the storage cell at the intersection of the selected row and column is also read.

Read and write data are input as a differential signal so that the static dual-port cell can operate at a higher speed. The circuit size is larger because it requires more components.

Dynamic Cell Organization. Each dynamic array in the μPD41101 and μPD41102 consists of two subarrays with 71 rows apiece. Each row of the subarray consists of 8 (number of bits) x 8 addresses (bytes). Each row of each subarray therefore has 8 subword lines. Figure 5 shows the organization of a dynamic array.

Figure 3. Dual-Port Static Storage Cell

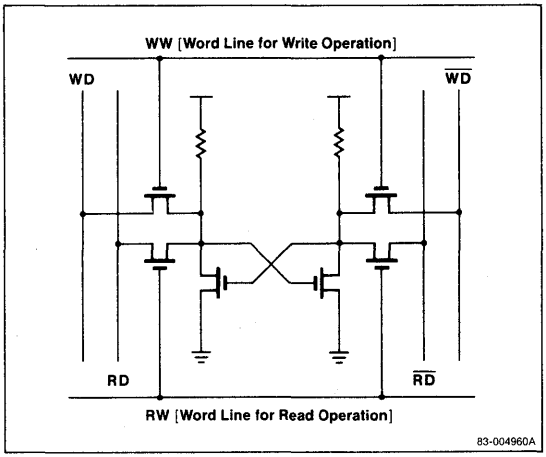


Figure 4. Dual-Port Dynamic Storage Cell

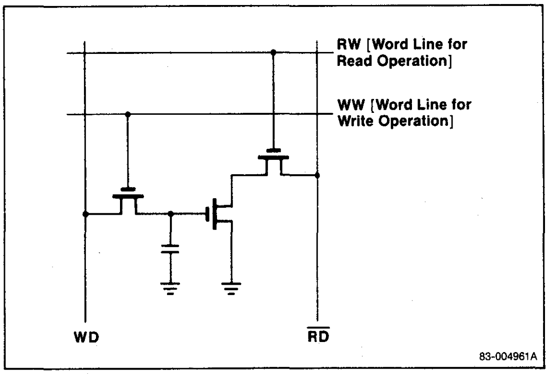


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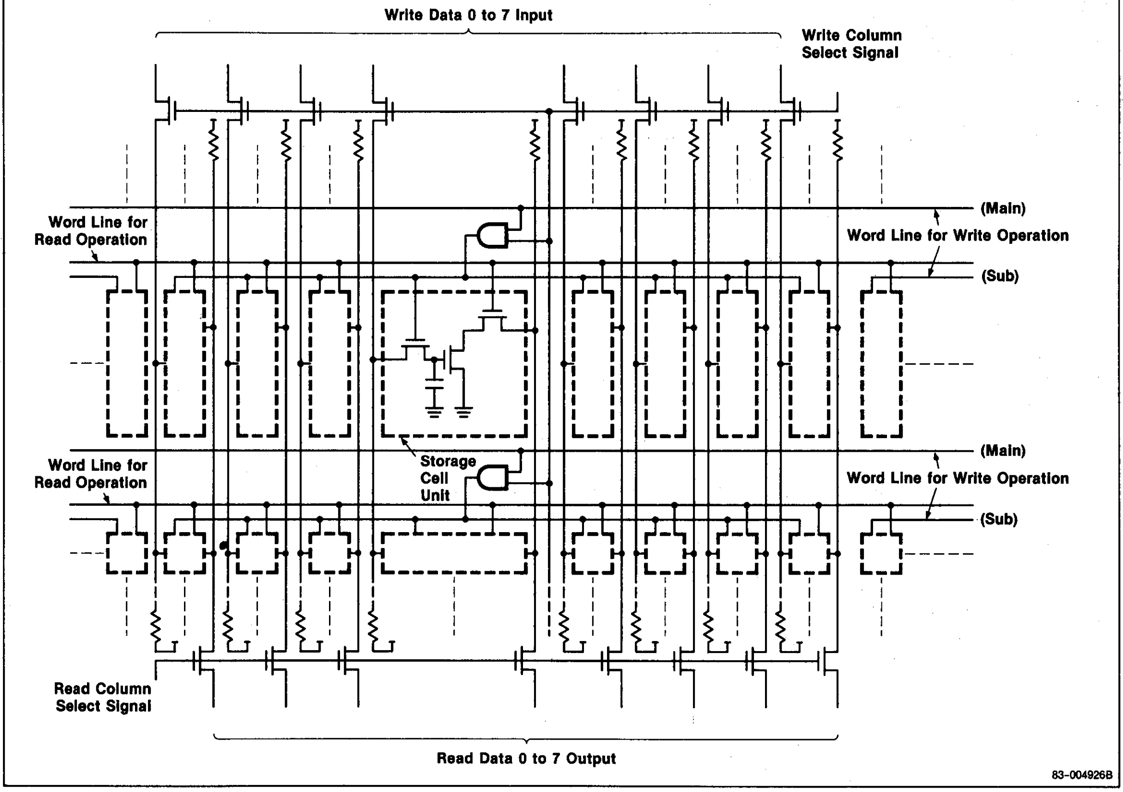
Figure 5. Organization of Dynamic Storage Array



The dynamic cell has only one bit line for each read ($\overline{RD}$) and write (WD) operation, one word line for each read (RW) and write (WW) operation, three transistors, and one capacitor. Although the longer data sense phase reduces its speed, a dynamic cell can be configured with fewer components and used for high-density integration.

In a write cycle, write data input through the bit line (WD) is guided through a transfer gate made conductive by the word line (WW). The gate charges or discharges the storage capacitor.

In a read cycle, the transistor with the gate connected to one end of the storage capacitor is turned on or off depending on whether or not the capacitor is charged. Data is transferred to the bit line ($\overline{RD}$) through the transfer gate, made conductive by the word line (RW), and then read externally. Word and bit lines for each operation are independent of each other so that read and write cycles can be executed asynchronously.

Data Transfer

The μPD41101 and μPD41102 are configured so that the internal address is incremented one bit at a time and data is accessed serially. After a reset signal initializes the device, a static cell that can operate at higher speed is accessed. Simultaneously or later, a dynamic cell is used as a pipeline, allowing access to both types of cells at high speed.

Stored information is defined by the state of the storage capacitor. When the word line for the write cycle goes to a selected level, the write transfer gate of each storage cell connected to the word line becomes conductive, and the data (electrical level) given to the bit line is rewritten to the capacitor connected to the end of the transfer gate. The precharge level of the write bit line (typically a high level) is rewritten to the storage cells on the selected word line, other than the one to which the column signal applies data, thereby destroying data stored there.

The μPD41101 and μPD41102 prevent this destruction of data by using a main word line and a subword line. The subword line is driven by the ANDed signals of the main word line and the write column. The transfer gate of each cell corresponding to each address is connected to a subword line. Therefore, the write word line of the storage cells at the selected row and column address is the only one which goes to a high level, preventing the destruction of data in other cells on the same write line.

Address Selection

A dynamic storage array consists of subarrays 1 and 2, each of which is 568 (71 x 8) bytes. A column selector and a row selector circuit are provided for independent read and write operation for each subarray.

The first step of address selection involves the accessing of an 8-byte static cell immediately after a reset cycle. The address selector moves to the first row of the subarray, and subarray 1 is accessed from left to right, one byte at a time. When 8 bytes of subarray 1 have been accessed, the address selector moves to the first row of subarray 2, also accessed from left to right, one byte at a time. When 8 bytes of subarray 2 have been accessed, the address selector alternately selects 8 bytes from addresses in both subarrays, so that rows are selected from the higher row to the lower row.

When the number of access cycles to the static cell array (8 addresses) and the dynamic cell array reaches 910 (for the μPD41101) or 1135 (for the μPD41102), the pointer moves to address 0 of the static array.

This method of sequential address selection increases the access speed of the dynamic cell by selecting row addresses in the pipeline method. Pipeline operation occurs when the word line (row) to be selected next is set to the selected level in advance so that it can be written or read at high speed, i.e., in the time required to select one column in static-column mode.

After a reset cycle, when 8 bytes of the static cell are being accessed, the first row of subarray 1, which is accessed next, is set to the selected level in advance. When the selected address moves to the first row of subarray 1 (after 8 bytes of static storage are accessed), a read or write cycle can be executed at high speed for that row. The first row of subarray 1 can be accessed at high speed even after the static array is selected. This process continues with the first row of subarray 2, the second row of subarray 1, and so on.

While the static cell is being accessed immediately after a reset cycle, the address on the dynamic cell is held on the first column and row of subarray 1. The dynamic array is not accessed at this time. Pipeline operation is performed independently for write and read cycles by the row and column selectors for each subarray.

Shift registers are used as read and write column and row selectors for the sequential selection of write or read addresses and pipeline processing. Shift registers are provided for each column and row, and each node level is set in advance so that when reset, each shift register outputs a high signal for the first column or row and a low signal for other columns or rows.

The column selector (shift register) is driven by WCK or RCK and the address is incremented by 1 for each clock cycle, i.e., the node that outputs a high signal changes in synchronization with the clock, and the column selector changes with it.

The row selector (shift register) is related to pipeline control and is driven by the pulse generated when the column address selector moves from subarray 1 to subarray 2 or vice versa. The row selector is incremented by one row address after the change from one subarray to another.

Each shift register used as a column or row selector is configured as a ring counter so that when the last column or row is reached, it automatically returns to the first column or row.

Applications

For the most part, the applications described below pertain to noninterlaced digital TV. The descriptions apply to NTSC systems, unless otherwise specified.

Comb Filter

A composite TV signal (output of a TV tuner) is the sum of the luminance (Y) and chrominance (R-Y, B-Y) color signals. The Y, R-Y, and B-Y signals must be separated, and the R, G, and B signals input to the picture tube generated from them.

A comb filter with line buffers derives the color or luminance signal by cancelling it from the composite signal, using the correlation between neighboring lines. This filtering fully separates the color and luminance signals, especially when there is a strong correlation between lines, to produce a clear picture.

If the signals are not well separated, the color signal may interfere with the luminance signal and cause dot crawl. The luminance signal may also interfere with the color signal and cause cross-color. This interference degrades the picture quality, especially where color or luminance changes sharply. Figure 6 shows a typical comb filter using line correlation.

This example compares target line B with neighboring lines A and C. Two μPD41101s are used as 910-bit delay lines. The color signal (C = R-Y, B-Y) is separated by subtracting the data of the upper and lower lines (A + C) from the target line data (B) and filtering the separated signal through the 3.58-MHz bandpass filter. The luminance signal is the result of subtracting the separate color signal from the original data (B). See the description of the "Variable-Length Delay Line" application for information on controlling a delay line of 910 bits or less.

Double-Speed Scan Conversion

The current NTSC and PAL TV systems use interlaced scanning to eliminate the flickering caused by field transition. Scanning is performed every two lines, reducing the pixel density and doubling the field frequency (number of fields-per-second), as illustrated in figure 7.

In interlaced scanning in the NTSC system, a complete frame consists of two fields of 262.5 scanning lines each. The field frequency is 60 Hz, i.e., the sum of 30 first fields-per-second and 30 second fields-per-second. In the PAL system, a complete frame is comprised of two fields of 312.5 scanning lines each. The field frequency is 50 Hz, the sum of 25 first fields-per-second and 25 second fields-per-second. In both cases, interlaced scanning reduces the flicker in motion scenes caused by field transition. The pixel density in the vertical direction is also reduced, diminishing the level of detail.

Figure 6. Interline Y/C Separation with a Comb Filter

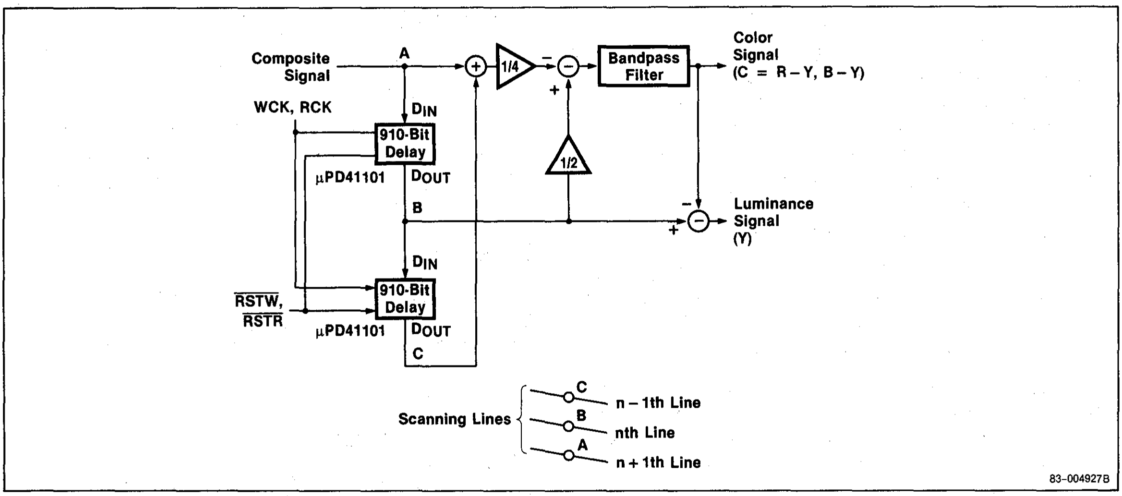
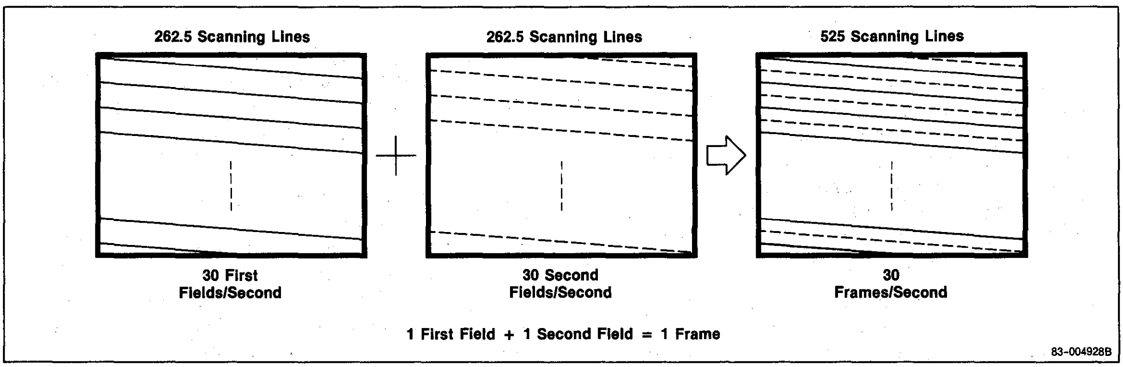


Figure 7. Relationship of Field to Frame in NTSC Systems



The μPD41101 or μPD41102 can be used to convert interlaced scanning to noninterlaced scanning. Doubling the pixel density (number of scanning lines) in the vertical direction without changing the field frequency produces clear and precise images (figure 8). In interlaced scanning, the first field of solid lines and the second field of broken lines are scanned alternately at 30 fields-per-second (25 fields-per-second in PAL). In noninterlaced scanning, the number of scanning lines per field is doubled, and 60 fields-per-second are scanned (50 fields-per-second in PAL).

In noninterlaced scanning, the data of the skipped line is created using the buffer. It is read at twice the sampling frequency of interlaced scanning ($8 f_{SC}$ if the interlaced sampling rate is $4 f_{SC}$). Noninterlaced scanning scans two lines in the time that one line is scanned in interlaced scanning. The horizontal frequency of the CRT must also be doubled for noninterlaced scanning.

The data of the skipped line can be created

- Using the data of the previous line (reading out the same data twice)
- Using the average value of the lines before and after the skipped line
- Using data that is one-field-old (the data for 262 lines before for NTSC, or 312 lines before for PAL)

In the first option, one μPD41101 (or one μPD41102 for PAL) is used for one input signal. The data is written at $4 f_{SC}$ and read out at $8 f_{SC}$. Reading starts when data is written to half of the line (455 bytes). The same data is read twice (910 bytes x 2) at $8 f_{SC}$. Data read in the latter half is used as interpolated data (figure 9).

In the second method, one μPD41101 delays the data of one line, and two μPD41101s convert the current data and the interpolated data for double-speed scanning.

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Figure 8. Interlaced and Noninterlaced Scanning

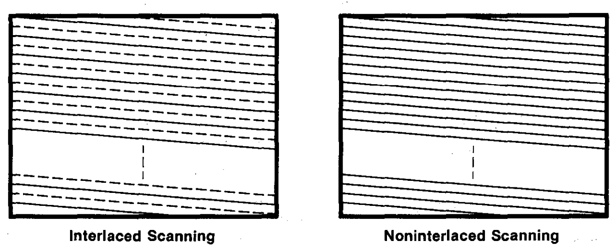
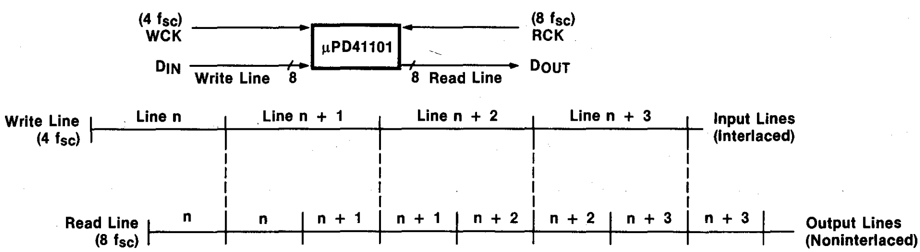


Figure 9. Using the Previous Line as Interpolated Data



The two μPD41101s used for scan conversion are written at 4 f_{SC} and read at 8 f_{SC}. The $\overline{RE}$ signal is controlled to first read the μPD41101 to which the current line data is written, and then read the μPD41101 to which the interpolated data is written (figure 10).

In the last option, as in the previous one, one buffer delays the data for one field and two other μPD41101s perform scan conversion. The control sequence is the same as described in the second method. Using data from a line of the previous field produces a clear image, especially in a still scene (figure 11).

Figure 10. Using the Average of the Previous and Following Lines

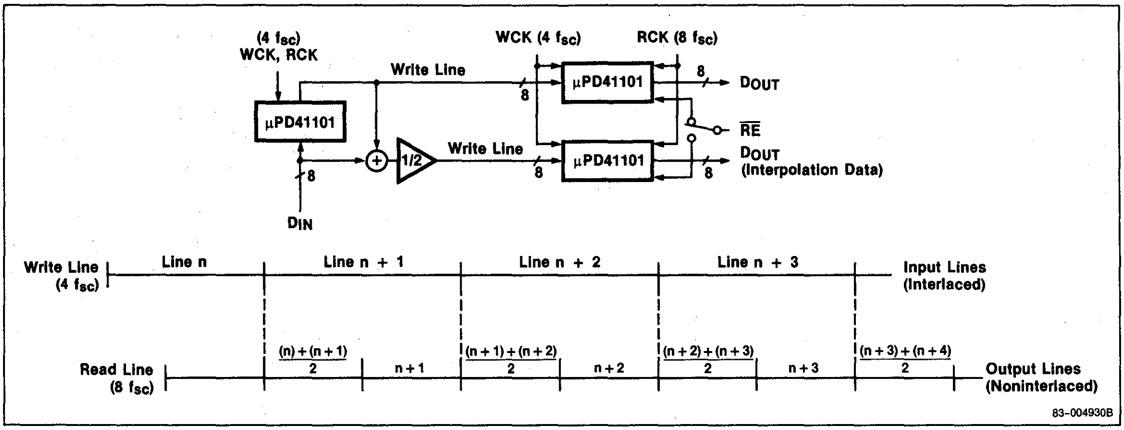
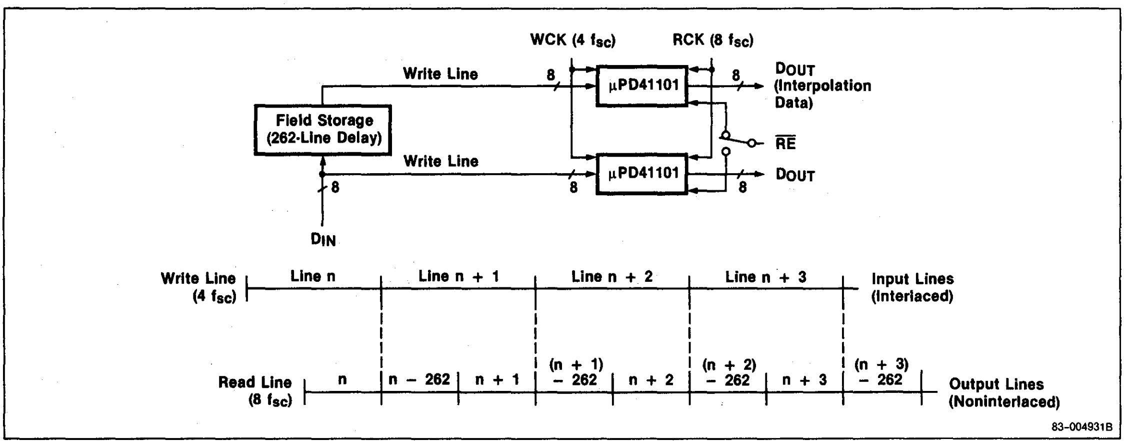


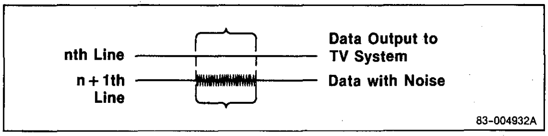
Figure 11. Using a Line from the Previous Field



Dropout Compensation

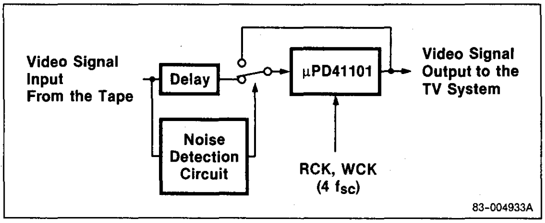
Dropout compensation cancels the noise in a VTR picture reproduction. If a line contains noise, the portion of the previous line in the same position as the noise is reproduced instead, eliminating the noise from the reproduced image (figure 12).

Figure 12. Example of Dropout Compensation



Video data from a tape normally is written to the μPD41101, delayed for one scanning line (910 bits), and then used as image data to a TV system. The noise-detection circuit senses noise in the video signal. When data containing noise is input to the μPD41101, the input is switched to the data already in the buffer so that the previous data line is written again. Data containing the noise is not output to the TV system (figure 13).

Figure 13. Dropout Compensation Circuit

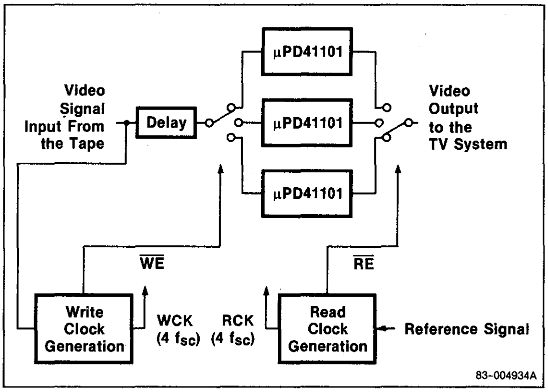


The μPD41101 can also be used as a 910-bit (one scanning line) delay. If the write data fed back by switching is delayed, the delay length must be reduced to compensate for it. For example, if switching causes two bits of delay, the delay length must be adjusted to 908 bits.

Jitter Compensation [Time Base Correction]

In a VTR, variation in head drum rotation speed or tape contraction or expansion can cause jitter in the reproduced image. The image can be reproduced clearly when jitter is adjusted and the image is reproduced with accurate clocks (figure 14).

Figure 14. Basic Jitter Compensation Circuit

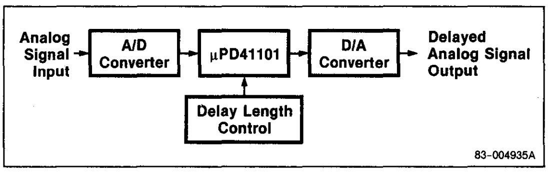


The video signal input from the tape is written to the μPD41101 with a clock that can be accurately slaved to the time axis variation of the input video signal. Video data with the same time axis is reproduced by reading data using the synchronized read clock as a reference. If a jitter compensation circuit is configured so that the device to which the data is written, or from which it is read, is selected from among two or more devices by the $\overline{RE}$ or $\overline{WE}$ signal, the circuit can have a delay length of two or more lines.

Variable-Length Delay Line

The μPD41101, driven at 8 f_{SC}, can be used as a variable-length delay line with a delay length of 10 to 910 bits (12 to 1135 bits for the μPD41102). Driven at 4 f_{SC}, it can produce a delay of 5 to 910 bits (6 to 1135 bits for the μPD41102). If an analog-to-digital (A/D) and a digital-to-analog (D/A) converter are connected to the input and output sides, respectively, it can also be used as an analog signal delay line (figure 15).

Figure 15. Analog Signal Delay Line



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When reading data at a certain address, the µPD41101 requires 300 ns + 0.5 write cycles (maximum) to read data once the write cycle is complete. For example, when the µPD41101 operates on a 34-ns clock, the minimum delay length is (300 + 34/2)/34 = 9.3, or 10 cycles. When the µPD41102 operates on a 28-ns clock, the minimum delay length is (300 + 28/2)/28 = 11.2, or 12 cycles. The maximum delay length of the µPD41101 is 910 cycles and 1135 cycles for the µPD41102.

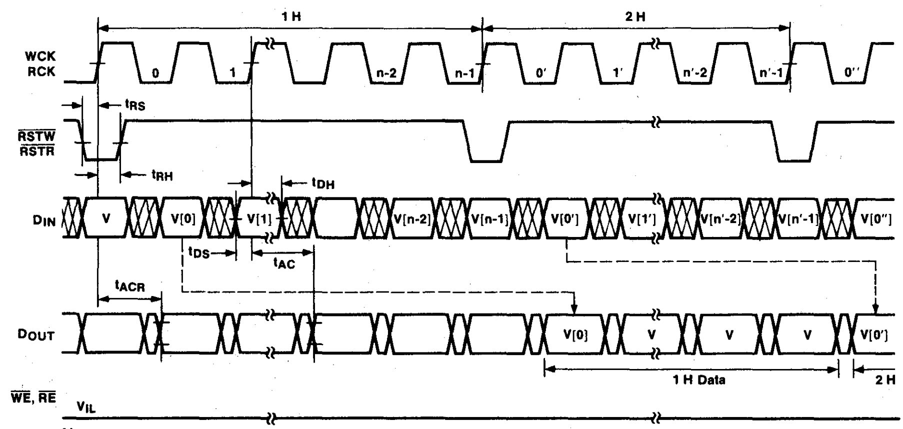
Delay length can be controlled by

- Controlling the reset input interval
- Inputting the write and read reset signals at different times (the delay length is determined by the offset between the inputs)
- Controlling the $\overline{WE}$ and $\overline{RE}$ signals

In the first method, the same signal is used for WCK and RCK. $\overline{RSTW}$ and $\overline{RSTR}$ are controlled together. Data written after a reset signal is read after the next reset interval. If the reset signal is input every 900 cycles, the delay length is 900 bits. This option produces a delay length determined by the reset interval to control the delay length (figure 16).

In the second method, using the write and read reset signals, data written from address 0 by the $\overline{RSTW}$ signal is read out from address 0 when the next $\overline{RSTR}$ signal is input. The delay length is determined by the offset between the write reset signal and the next read reset signal input (figure 17).

Figure 16. Controlling Delay Length with the Reset Interval



Notes:
[1] V = valid data.
[2] 1H = the first group of "n" bits.
[3] 2H = the second group of "n" bits.

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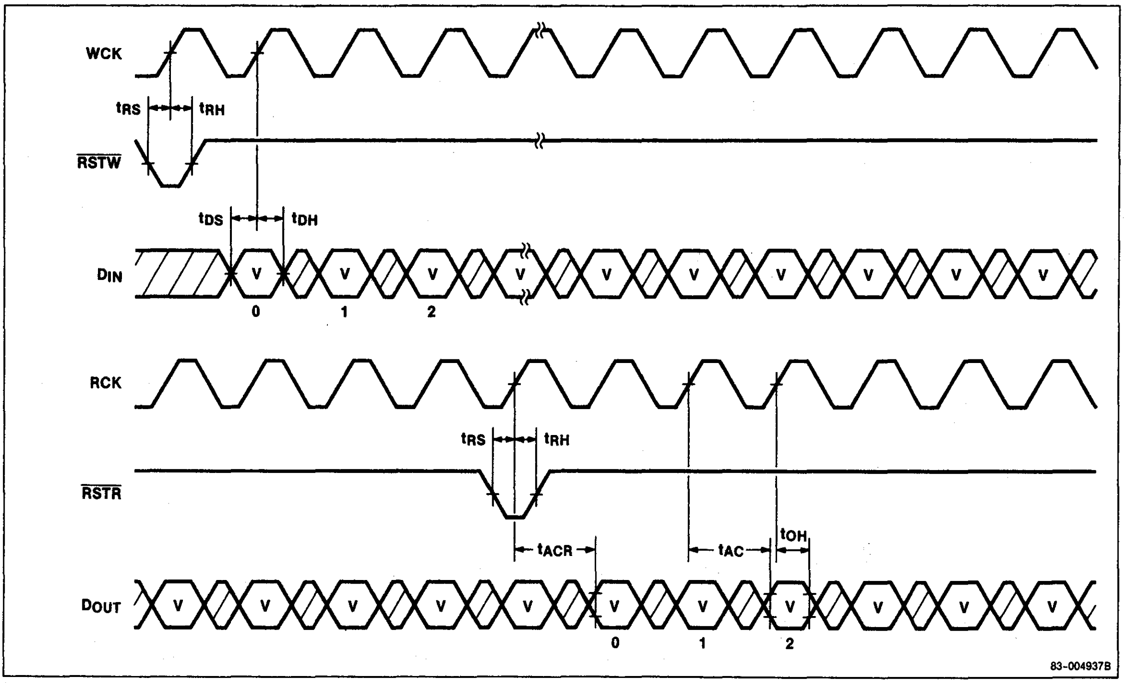
Figure 17. Controlling Delay Length with $\overline{RSTW}$ and $\overline{RSTR}$



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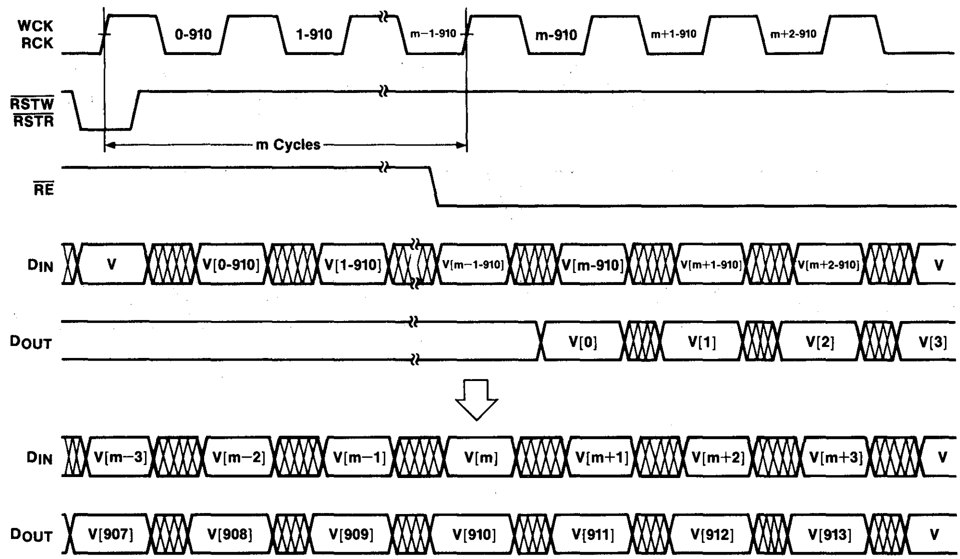
In the third method, using the $\overline{WE}$ and $\overline{RE}$ signals, write or read operation is disabled when $\overline{WE}$ or $\overline{RE}$ is high; the interval pointer remains at the address where operation is disabled, regardless of the status of WCK or RCK. The delay length can be controlled in one-cycle units by controlling $\overline{WE}$ and $\overline{RE}$. After the reset interval, read data is delayed by 910 cycles (1135 cycles for the μPD41102) from the write data (figure 18).

Time Axis Conversion

You can use the μPD41101 for time axis conversion by changing the write clock frequency (WCK) and the read clock frequency (RCK). One application for time axis conversion involves image contraction or expansion in the horizontal direction. The image contracts if the read clock frequency is higher than the write clock frequency, and it expands if WCK is higher than RCK (figure 19).

Figure 18. Controlling Delay Length with $\overline{WE}$ and $\overline{RE}$ in the μPD41101



Notes:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

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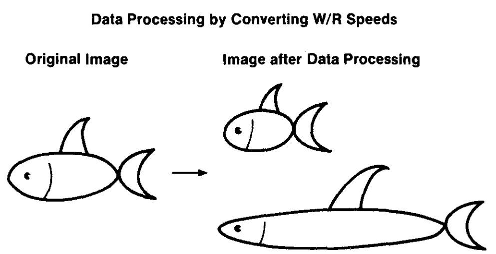
Figure 19. Time Access Conversion Application



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Digital Signal Input Synchronization

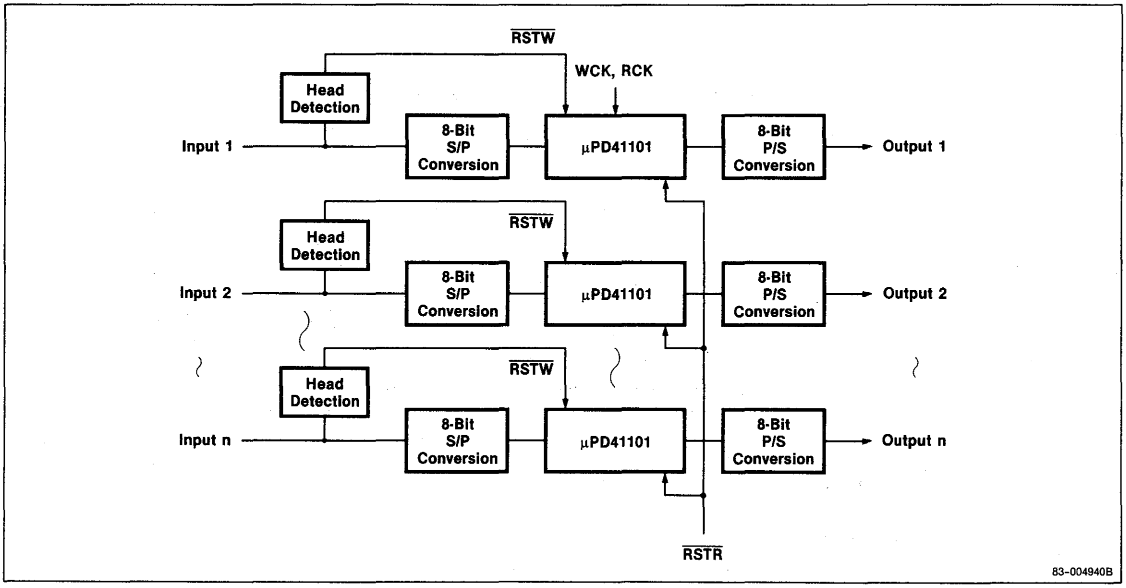
When performing timeshared data processing in an electronic telephone exchanger or in a star-configured local area network, the phase between input streams may be offset because of differences between the terminal and the central line exchange module. The μPD41101 can be used to correct the phase offset (figure 20).

Inputs 1 to n are serial data input streams. However, the frame heads (flags indicating the beginning of the data) of each input stream are not synchronized.

The solution requires controlling write operation for each stream. When a frame head is detected, the write address is reset to 0. A clock extracted from each input can be used as the clock for that write cycle. When data is written to all μPD41101s, the read address is reset to 0 by inputting $\overline{\text{RSTR}}$ with appropriate timing. All data streams then can be read out in the same phase by reading all μPD41101s simultaneously, even if the input streams are not synchronized.

The serial-to-parallel and parallel-to-serial conversion circuits shown in figure 20 may be used only when serial data is handled at each input and output.

Figure 20. Digital Signal Input Synchronization



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General Application

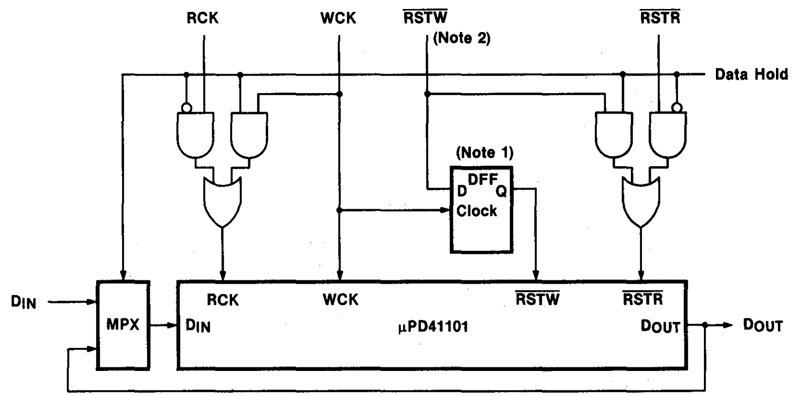
The μPD41101 and μPD41102 are suitable for use as buffer storage in data transfer operations between devices of different speeds. Because they use dynamic circuits, the maximum hold time for storage cell data is 1 ms. To hold data longer than 1 ms, you must rewrite it to the same address within 1 ms (figure 21).

The read and write addresses must coincide when rewriting data. If the feedback data is not delayed by a multiplexer, input the $\overline{RSTW}$ and $\overline{RSTR}$ signals simultaneously so that the output data of address n is fed back to the input as it is, and then written again to address n.

If the feedback data is delayed, adjust the input timing of $\overline{RSTW}$ and $\overline{RSTR}$, depending on the delay (number of cycles) of the feedback data. $\overline{RSTR}$ must be advanced according to the feedback data delay.

In either case, WCK and RCK must be the same. To read the data written to an address after the write cycle for that address is complete, 300 ns + one-half write cycle is required.

Figure 21. Static Hold Circuit for Storage Cell Data



Notes:

[1] A D-type flip-flop must be provided when the data is delayed.

[2] $\overline{RSTW}$ must be input at least once while Data Hold is at a true (high) logic level.

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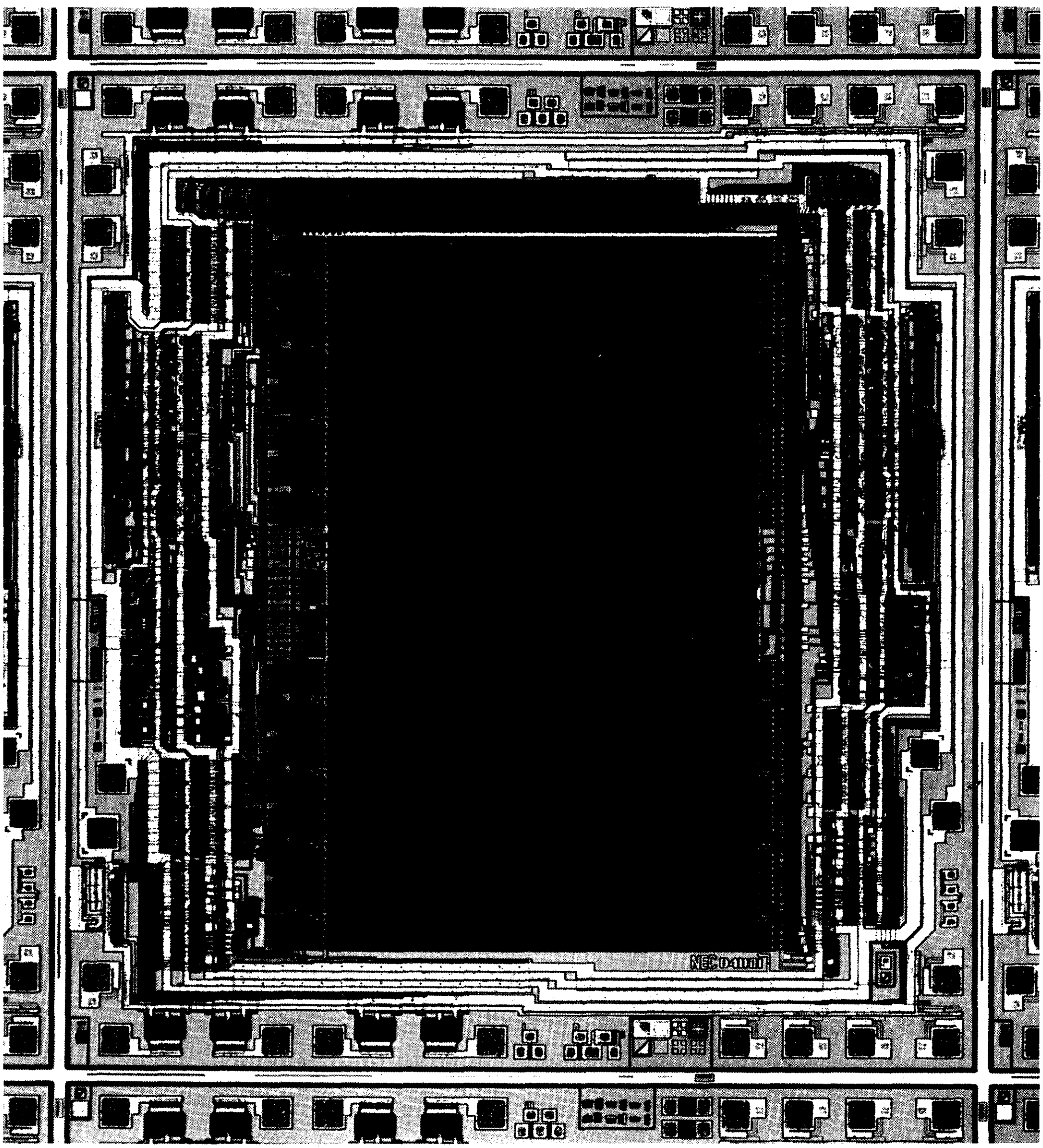
Figure 22. μPD41101/μPD41102 High-Speed Line Buffer



APPLICATION NOTE 56
μPD42601
SILICON FILE

Introduction

In the field of computer-aided design and manufacturing (CAD/CAM), running software with many utility programs results in time-consuming disk accesses. Workstations operating in a local area network (LAN) also are performance-limited by the heavy burden on magnetic disks serving multiple users. These systems receive a performance boost when the magnetic disk is replaced with a solid-state disk.

NEC developed the μPD42601 silicon file, a 1,048,576 x 1-bit semiconductor disk, precisely for such applications. The CMOS-fabricated μPD42601 operates much faster than hard disks, with simplified circuitry and fewer sense amplifiers than standard DRAMs. Although access times from $\overline{RAS}$ (t_{RAC}) and $\overline{CAS}$ (t_{CAC}) of 600 ns and 100 ns, respectively, make this device slower than standard DRAMs such as NEC's μPD421000, the use of word-width system architecture and page-cycle accesses achieves very high data transfer rates and can therefore improve system efficiency.

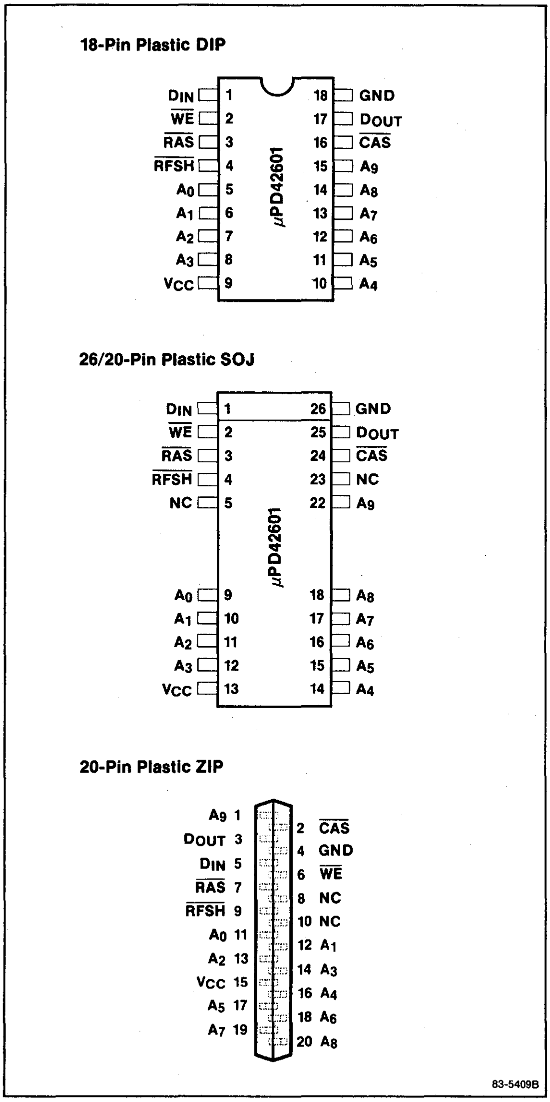
Applications

Because the device's high capacity, battery-supportable nonvolatility, and environmental hazard resistance are expected to challenge the niche previously defined by bubble devices, the μPD42601 should find its major market in large solid-state disk applications. However, as shown in table 1, other potential markets exist. For example, the μPD42601's very low data retention current, which reduces heat buildup and simplifies thermal design, means that a cool die operating in a 300-mil SOJ offers greater flexibility in packaging and stimulates new ideas for other product applications (see figure 1 for packaging options and pin assignments of the μPD42601).

Table 1. Potential Markets for μPD42601 Silicon File

Market	Requirements	Applications
Solid-state disks	High capacity Reliability Battery backup	High-end engineering workstation (100 Mbytes to 1 Gbyte)
Portable handheld products	Light weight Low power Small size	Personal computers Retail point-of-sale terminals
Industrial	Immunity to a hazardous environment: vapors, dust, vibration	Process control Robotics

Figure 1. Pin Configurations



Power and Speed Enhancements

All access cycles and timing specifications for the μPD42601 are similar to those of generic DRAMs. However, the μPD42601 requires only 25% of the operating power and 5% of the standby power of a standard DRAM, and therefore provides a better silicon solution for the aforementioned applications. The silicon file has a specified access time from $\overline{RAS}$ (t_{RAC}) of 600 ns. A quick page access time from $\overline{CAS}$ (t_{CAC}) of 100 ns is also available. Heavy system use of page cycles makes the best choice for two reasons: the first is speed enhancement over standard $\overline{RAS}/\overline{CAS}$ cycles and the second is disk sector size, which closely matches the number of bits accessible in page cycles.

In target applications for the μPD42601, low power is required. Both operating and standby power are important: low operating power results in cooler device temperatures and higher reliability, while standby currents in the microampere range allow for battery backup and small packaging options.

Self-Refreshing

The μPD42601 has a self-refresh feature similar to the one found in pseudostatic DRAMs. Bringing the $\overline{RFSH}$ pin low and clocking $\overline{RAS}$ permits the silicon file to retain data while using only 30 μA of power. In large solid-state systems, the solid-state disk would use byte-wide or word-wide banks of silicon file storage, with only one bank of devices active at a time, and all others in a state of self-refreshing. In this low-power operation, total power consumption of the system would be very low, making battery backup possible with compact batteries.

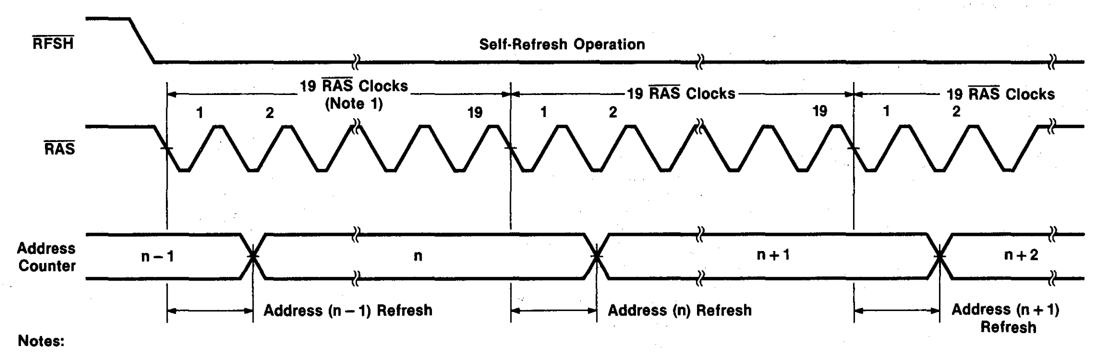
During self-refresh cycles, a relatively slow $\overline{RAS}$ clock can be applied and data integrity still be maintained. To enter this power-down quiescent state, the user can pull $\overline{RFSH}$ low and start the $\overline{RAS}$ clock at a slow cycle time (t_{RCF}). Since data loss is caused by leakage, and leakage current increases with temperature, NEC has specified the t_{RCF} rating at 50 °C, 60 °C and 70 °C. Each temperature rating has a corresponding refresh current (directly proportional to the refresh rate) which is required to maintain data, with faster rates required for higher temperatures (table 2).

Table 2. Self-Refresh Conditions

T_A	t_{RCF} (max)	Self-Refresh Current (max)
50 °C	20 μs	30 μA
60 °C	10 μs	60 μA
70 °C	5 μs	120 μA

It is important to make a distinction between self-refresh cycles and the more familiar $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. When low, the $\overline{RFSH}$ pin enables self-refreshing and disables most of the internal circuits. Only those circuits required for self-refresh operation are active. Because of the rate of t_{RCF} required for substrate bias generation, nineteen $\overline{RAS}$ clocks are used in the μPD42601 to refresh one row (figure 2).

Figure 2. Internal Address Generation in Self-Refresh Operation



Notes:
(1) One internal address is refreshed every 19 $\overline{RAS}$ pulses.
(2) The self-refresh mode is intended primarily for long periods of refresh-only operation.

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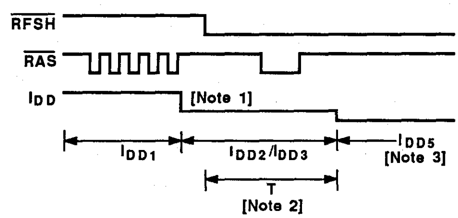
Figure 3 shows a simplified block diagram of the μPD42601 during self-refresh operation. The low level of $\overline{RFSH}$ disables the ring oscillator and initializes the $\overline{RAS}$ buffer and 19-bit counter. The external $\overline{RAS}$ clock is reduced in frequency by the 19-bit counter. The outputs of the counter and the timing generator are then used to generate the slow-speed timing, decoding, and sensing operations, while the substrate bias generator functions at a reduced frequency to keep the substrate stabilized but minimize power consumption.

Figure 4 shows the transition and delay times for I_{DD1}, I_{DD2}, I_{DD3}, and I_{DD5}. When $\overline{RFSH}$ goes low, a 2.5-ms delay occurs before the device enters true self-refreshing. The timing shown in figure 4 depends on internal temperature-compensated delay circuits and is required to allow the die to stabilize at a lower temperature. During this 2.5-ms period, the standby current is specified as I_{DD3}, or 500 μA. After the die cools, the substrate bias generator operates at a lower frequency and power consumption is composed of five components: the $\overline{RAS}$ buffer, the 19-bit counter, the decoder, the substrate bias generator, and the sense amplifiers. All other peripheral circuits are disabled.

Figure 4. Transition and Delay Timing in Self-Refresh Operation



[1] Power is reduced to standby after the last $\overline{RAS}$ cycle.
[2] After $\overline{RFSH}$ goes low, the internal delay circuit determines the length of T.
[3] The substrate bias generator operates at a lower frequency to reduce the current.

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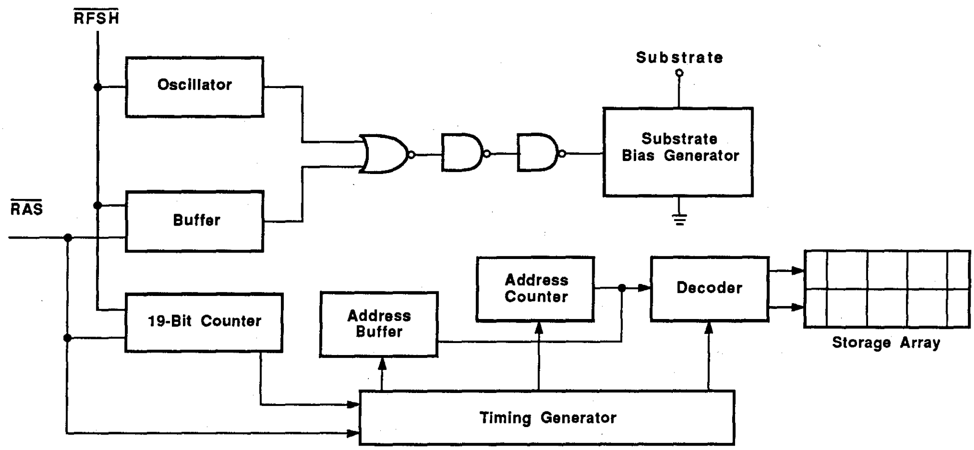
Figure 3. Circuit Operation in Self-Refresh Operation



3

$\overline{CAS}$ Before $\overline{RAS}$ Refreshing

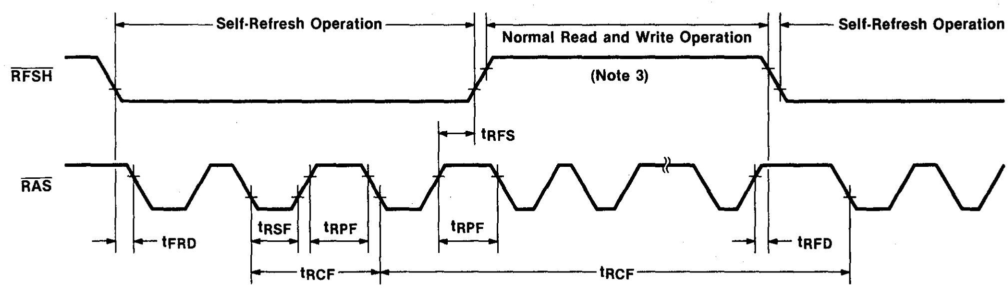
The μPD42601 does not incorporate its own automatic refresh circuits on-chip, but requires pulsing $\overline{RAS}$ in the self-refresh state to hold data. Another more descriptive term for this function is "pulse refreshing." In most pulse-refreshed devices, the method of entering and exiting self-refresh operation is crucial; however, the 1M x 1 silicon file makes transitioning between operating and self-refresh modes simpler than previous-generation pseudostatic devices.

In the case shown in figure 5, no $\overline{CAS}$ before $\overline{RAS}$ cycles are executed during a period of normal write and read cycles. Re-entering self-refresh operation after short write/read bursts limits the number of bits that could have been accessed in the relatively short time specified for t_{RCF} (i.e., the maximum cycle time for $\overline{RAS}$ in self-refresh operation).

If system timing remains in normal write or read operation longer than t_{RCF} (max), then refresh logic is needed to control $\overline{CAS}$ before $\overline{RAS}$ refreshing. Every 32 ms, 512 refresh cycles are needed to refresh the 512 row addresses, an average rate of one every 62 μs. Because of the reduced operating current and the resultant lower die temperature, the refresh period can be extended to four times the 8-ms value specified for most 1M x 1 DRAMs.

In $\overline{CAS}$ before $\overline{RAS}$ cycles, addresses need not be supplied because an internal counter supplies them to the decoders. Since the clocks for both $\overline{CAS}$ before $\overline{RAS}$ refresh cycles and self-refresh cycles increment the same internal address counter, there are orderly and sequential transitions from self-refreshing to $\overline{CAS}$ before $\overline{RAS}$ refreshing and back to self-refreshing. Ensuring that the row addresses are refreshed in a timely fashion is the function of the refresh counter, which is clocked by $\overline{CAS}$ before $\overline{RAS}$ during normal cycles and at the rate of 1/(19 x t_{RCF}) during self-refresh cycles. The μPD42601 runs cooler than other self-refreshing devices and does not require a burst of extra $\overline{CAS}$ before $\overline{RAS}$ cycles before self-refreshing to ensure data integrity.

Figure 5. Special Requirements for t_{RCF} Near Periods of Limited Standard Refresh Cycles



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50°C	20 μs	5 μs
60°C	10 μs	5 μs
70°C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] In this period of normal read/write operation, there are no CBR refresh cycles or less than 512 $\overline{RAS}$-only refresh cycles.

[4] The time delay between the last self-refresh pulse in one self-refresh cycle, and the first self-refresh pulse in the next cycle, is defined by t_{RCF} [max] when the intervening period of read and write operation meets the conditions in Note 3.

[5] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

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As discussed earlier, a lower die temperature permits both a relaxed refresh rate and simplified transition timing between self-refresh and normal write and read cycles. The die temperature is a function of the ambient temperature, operating power, and the junction-to-ambient thermal resistance (θ_{JA}). The calculations showing the increase of junction temperature (T_J) over ambient temperature (T_A) at maximum power consumption (P_D max) are shown in the sequence below.

(1) $T_J = (\theta_{JA} \times P_D) + T_A$

(2) $T_J = [95\,°C/W \times (5.5\ V \times 12\ mA)] + 55\,°C$

(3) $T_J = 61.27\,°C$

In a solid-state disk system where the air temperature stabilizes at 55°C, the silicon file chip temperature would not exceed 61.27°C, comparing favorably with the die temperature of 81°C or more for a standard DRAM encapsulated in a plastic SOJ and operating in similar conditions.

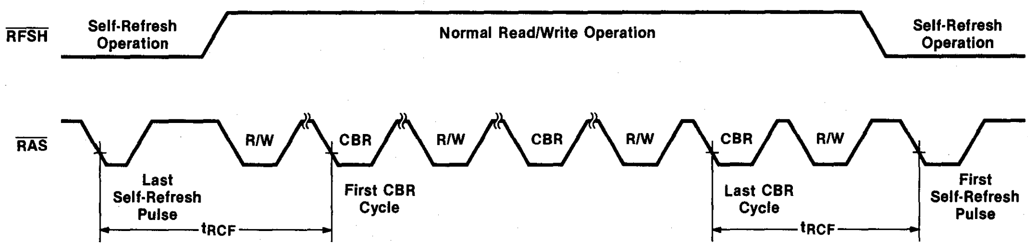
Figure 6 shows the maximum specification for t_{RCF}, the critical parameter when transitioning between $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ and self-refresh cycles. When exiting self-refresh operation, t_{RCF} (max) is measured between the falling edges of $\overline{\text{RAS}}$, from the last self-refresh cycle to the first $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. After transitioning from self-refresh operation to a period of normal write or read cycles, writing and reading can proceed for only 5 μs (at 70°C) before a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle is required. When transitioning from write and read operation to self-refresh operation, the process is simply reversed, with t_{RCF} (max) referenced between the last $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle and the first self-refresh cycle.

$\overline{\text{RAS}}$-only refreshing does not increment the refresh counter, complicating the procedure for moving between refresh modes. In refresh methods other than $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a burst of 512 refresh cycles is required before entering and also after exiting self-refresh operation. Complete refreshing of all rows is needed since, in refresh modes other than $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, the status of the refresh counter is unknown and the maximum specification for t_{RCF} may be exceeded. When the self-refresh capability is used, then $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing is recommended.

Soft Error Performance

Like the 1M x 1 DRAM, the μPD42601 uses the trench cell for a small die size and excellent immunity to alpha particles. Accelerated soft error results are less than 1000 FITs (Failures In Time, or errors in 10^9 device-hours). With low manufacturing cost as an objective, the device includes no error correction circuit (ECC), parity, or data checking functions on-chip. Most customers prefer to implement these functions off-chip.

Figure 6. Timing Restrictions Entering and Exiting Self-Refresh Operation



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50°C	20 μs	5 μs
60°C	10 μs	5 μs
70°C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004501

Silicon File-Based Solid-State Disk System

To assist our customers in the design-in of the μPD42601, NEC undertook a 20-Mbyte solid-state disk hardware project, a block diagram of which appears in figure 7 and a photograph in figure 8 (the hardware enclosure was designed for expansion to 40 Mbytes). Contained within the same package form factor as a 5.25-inch Winchester, the solid-state disk system includes batteries, a power supply, and the necessary power fail logic to provide complete nonvolatility for up to one month. The error correction device is a gate array developed at NEC and is not commercially available. A specification summary of this application project is shown in table 3.

Table 3. Specification Summary

Parameter	Specification
Capacity	20 Mbytes
Interface	SCSI (host)
Data transfer rate	1.5 Mbytes/sec (max)
Access time	0.1 ms (max)
Error correction	1-bit correction and 2-bit detection
Sector size	256 or 512 bytes
Power supply	5 volts, 2 amps
Package size	5.25-inch disk
Battery voltage	4.8 volts
Battery backup	One month
Operating temperature	5 to 50°C

Description of the Block Diagram

For the purpose of explanation, the block diagram in figure 7 and the following system description are detailed according to the format shown in table 4.

Table 4.

Major Functional Blocks	Major Components
Power source/switch	Battery, power control circuits
Silicon file and ECC	μPD42601LA, ECC gate array
Timing generator circuits	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ logic
Data/address control	V40™, WD33C93™, RAM, ROM

Power Supply and Power Fail Circuits

The upper left corner of the block diagram consists of the battery, power switch, voltage detector, and power fail circuits. Included in the power switch is a 5-volt switching regulator and the power conversion circuits. When the detector senses the falling power supply voltage, the power switch supplies the battery voltage to the components shown within the shaded block (battery backup). At the same time, the power fail logic sends a nonmaskable interrupt (NMI) to the V40, which initiates an internal subroutine and places the microprocessor in the low-current HALT mode.

When system power is restored, the rising voltage is detected. After a delay, the power switch disconnects the battery source and allows the 5-volt supply to power the system. Once the V40 receives the second NMI and resets the processor, $\overline{RFSH}$ goes inactive and normal timing resumes.

To ensure nonvolatility and reduced battery current drain, the silicon file devices must be placed in self-refresh operation when system power fails. In figure 7, the power fail logic has two outputs: one called self-refresh, which pulls $\overline{RFSH}$ low on all the storage chips, and a second output connected to the control pins of the V40 and the timing generator block. This output is actually two lines: one for the V40 NMI input initializing HALT mode and the second for initializing the timing generator circuits. When this output signal is active, the power fail logic switches the timing for $\overline{RAS}$ from normal read/write/refresh timing to the self-refresh oscillator. For this application, the self-refresh frequency is set at 50 kHz because this system is specified to operate at 50°C (maximum).

Storage Organization with ECC

The solid-state disk is organized as five banks of 39 devices, a 32-bit internal data word and an additional 7 bits for the ECC check bits. The ECC device is capable of 2-bit detection and 1-bit correction.

A 32-bit data bus is acceptable for the ECC chip, but the V40 and the SCSI interface controller require a byte-wide bus. The lower right corner of figure 7 shows a four-section register to accomplish this 32- to 8-bit conversion. This register is composed of eight octal bus transceivers with eight enable lines generated in the timing generator block. Four of these transceivers are used for the input side and four are used for the output side. The four octal bus transceivers (4 x 8 bits) comprise the 32-bit-wide data bus. The enable signals select one of the four transceivers receiving and sending each byte to or from the 8-bit data bus.

V40 is a trademark of NEC Corporation.
WD33C93 is a trademark of Western Digital.

Figure 7. Block Diagram of Silicon File Disk

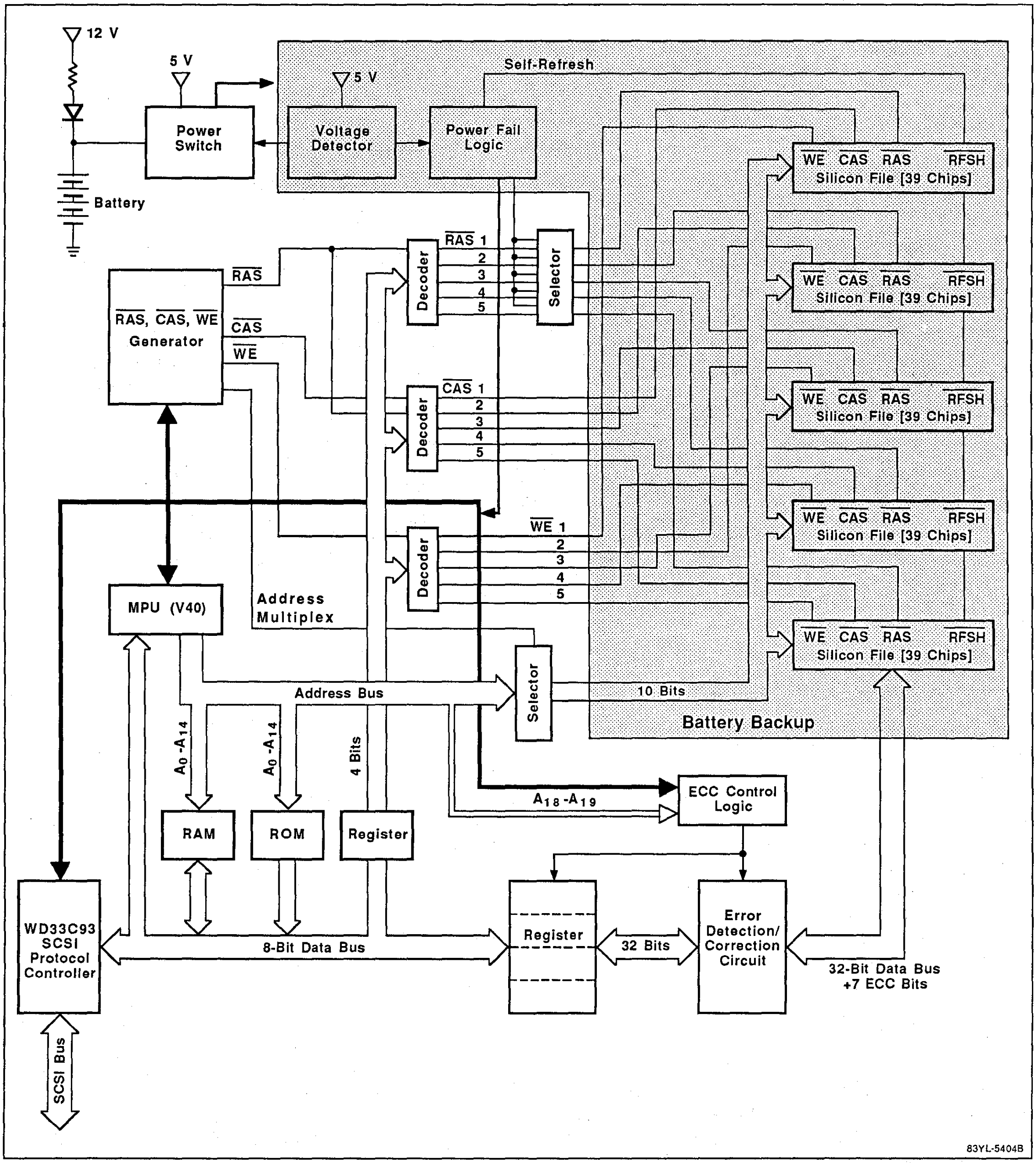
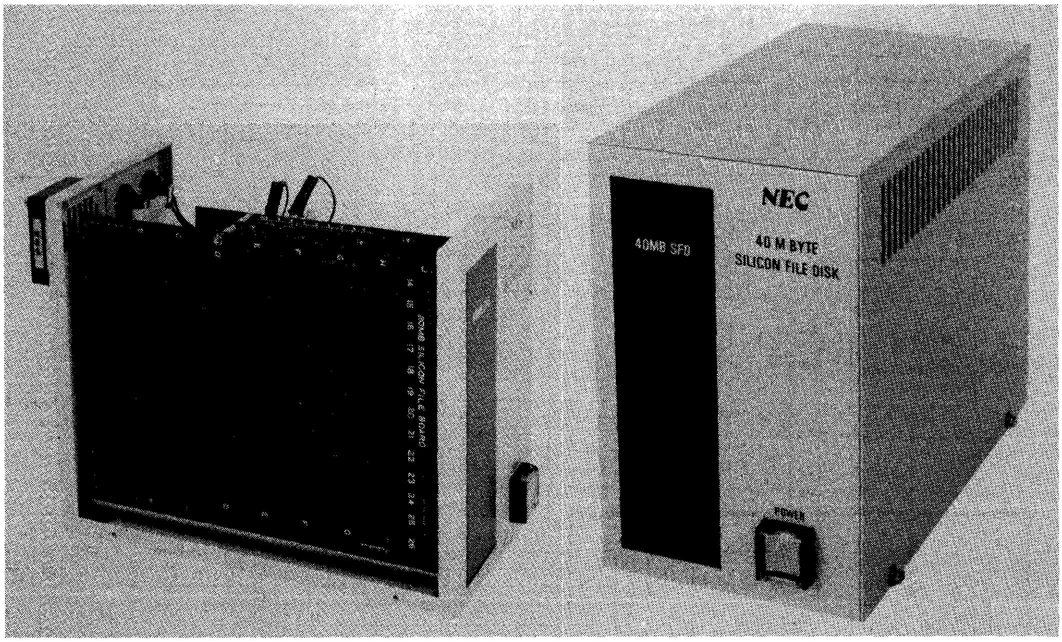


Figure 8. Photograph of Silicon File Disk



Timing Generation and Decoding

The timing generator block consists of a delay line, several PALs®, and glue logic. Its purpose is to control write and read operation and $\overline{CAS}$ before $\overline{RAS}$ timing. One of the PALs is used for decoding the eight enable signals used in the 32- to 8-bit multiplexing and demultiplexing operation discussed in the preceding section. Selecting one of five of the storage banks is accomplished by decoding $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. This function, together with the selection of the self-refresh oscillator, is contained in the logic blocks shown to the left of the storage array. The self-refresh oscillator is contained in the power fail logic block.

Data Transfer Control [V40 and SCSI Controller]

In this system, the SCSI controller is the target and the host computer connected to the SCSI controller is the initiator. Although a solid-state device is not a disk in that it has no cylinders, heads, or sectors, the V40 has been designed to handle all the control, data transfer, and address translation functions. Used as a microcontroller, the V40 makes the silicon disk look like a magnetic disk to the WD33C93.

Read Operation

Upon receiving the input/output command from the host system, the host adapter arbitrates and wins bus control. The target, the SCSI controller in this case, is selected and receives the read instruction and starting address from the host adapter. This information is stored as part of the command data block in the SCSI controller's internal register. At this point, the host disconnects. The V40 first recognizes the read command and the address and then sets the proper bits in the WD33C93 address register. Under V40 control, data is accessed from the correct logical address in the silicon file and moved to the μPD43256A buffer RAM.

Once the silicon file has started filling the RAM, the SCSI adapter can reconnect to the host. During this phase, the target arbitrates for the bus and wins control of it. The host is selected and the target sends the message that it is reconnecting. Under control of the V40, data is moved from the RAM to the SCSI controller and is received by the host adapter completing the operation. With this fast semiconductor disk, the data transfer rate depends more on arbitration time than on device access time.

PAL is a registered trademark of Advanced Micro Devices, Inc.

NEC
NEC Electronics Inc.

APPLICATION NOTE 57
μPD41101/μPD41102/μPD42505 HIGH-SPEED LINE BUFFERS

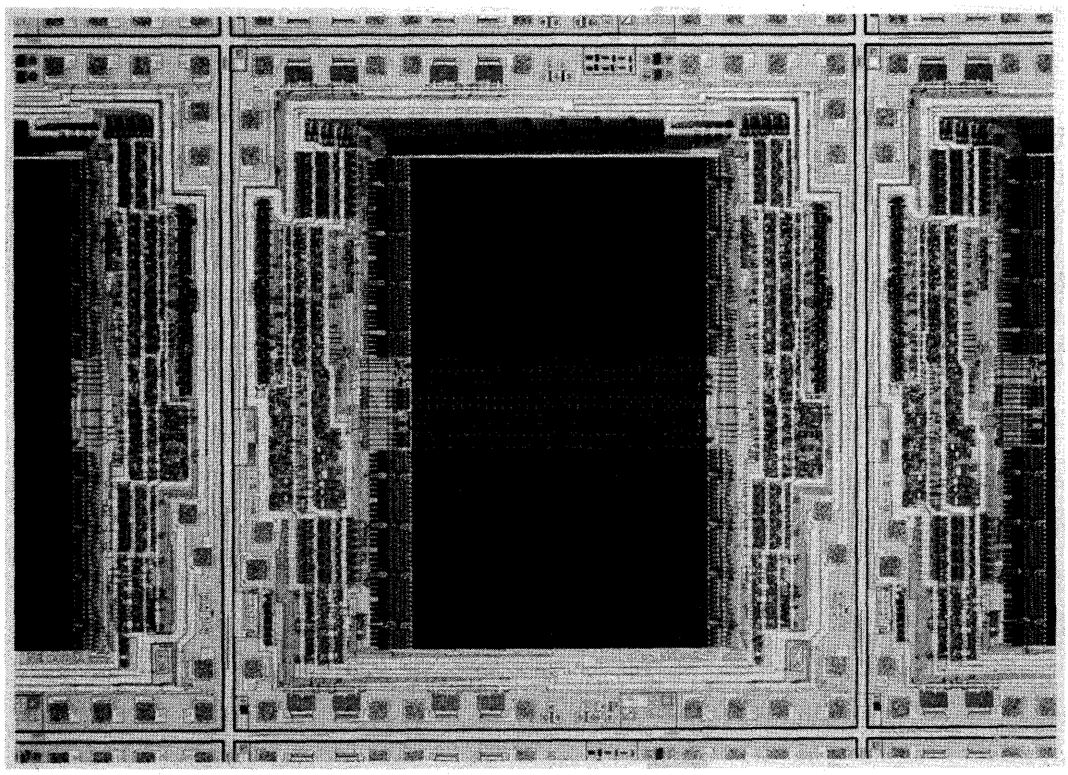
Introduction

The need for storage devices to provide delay and speed conversion in a variety of computer, telecommunication, and consumer applications has led to NEC's development of several new high-speed line buffers. The synchronous or asynchronous operation of these devices allows them to be used as elastic storage to synchronize data flow between two asynchronous parts of a system, e.g., between communication and microcomputer chips.

In graphics systems, line storage devices can act as high-speed source and destination registers during raster operations. In television and VCR products, the 1K x 8 buffers provide the raster line storage required for luminance and chrominance separation and noninterlaced scan conversion. The larger 5K x 8 devices are perfectly suited for facsimile and printer applications because they can store a line of information or a page of text at high speed.

This application note describes NEC's μPD41101, μPD41102 and μPD42505, three functionally equivalent buffers with different capacities and speeds. Each device has independent, 1-byte write and read ports with separate write and read clocks. High-speed performance is achieved by means of unique circuitry rather than a submicron process. Fast access times

Figure 1. Die Photograph of the μPD41101 and μPD41102



and low cost are possible because of specialized dynamic circuit designs using the best of MOS technology (figures 1 and 2).

Features

The μPD41101, μPD41102, and μPD42505 are identical except in organization and cycle times (table 1). The following discussion applies to the three devices collectively, unless noted otherwise.

Serial Addressing. Addresses are generated automatically by an internal address counter and need not be supplied externally. The clocks provided by the WCK and RCK signals increment the respective write and read address counters, enabling data to be read out in the order in which it was input.

Wraparound Addresses. The internal address pointers are implemented as ring counters; they return to address 0 after the last byte in a line has been accessed.

Asynchronous Operation. Separate write and read clocks, coupled with their respective enable inputs, allow for independent write and read operation.

Reset Function. The $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ pins reset the internal pointers to address 0. Resetting of the read pointer can be initiated after "n" write cycles to provide an adjustable delay line of "n" cycles.

High-Speed Address Selection. By interleaving the internal storage arrays and using a novel pipelining technique for high-speed address selection, the devices achieve very fast access times. The μPD41102-3, for example, has a specified minimum cycle time of 28 ns.

Large Capacity. All devices are 1-byte wide. Their line lengths vary as shown in table 1. The μPD42505 is configured as 5048 by 8 bits to store a page of information.

Table 1. Configurations and Cycle Times

Part Number	Organization	Cycle Times
μPD41101	910 x 8 bits	34 or 69 ns
μPD41102	1135 x 8 bits	28, 34, or 56 ns
μPD42505	5048 x 8 bits	50 or 75 ns

Functional Description

Historically, line buffers were designed with shift registers that suffered from fall-through delay as data tumbled down the stack. With NEC's new generation of buffers, which provide independent write and read clocks for asynchronous writing and reading, the write data requires a delay of at least 10 or 11 cycles before appearing at the output. The minimum line delay (specified in the individual data sheets for each device) is not a problem in most applications because the required delay is usually longer than the specified minimum delay.

In synchronous operation, where write and read cycles are controlled together (and write and read addresses coincide), the internal logic causes a write cycle to be delayed by one-half cycle from the read cycle. Read data is output from the previous line, while new input data is written just one-half cycle later.

Storage Arrays

Unlike other devices based solely on static cells, NEC's line buffers have two types of storage elements: a static cell for high-speed operation and a dynamic cell for achieving large capacity in a small die area. To operate at high speed, the fast static cell is used as a prefetch buffer. While the first 8 bytes of data are being accessed from the static cell, the first row of the dynamic cell is preselected for subsequent access (see **Addressing**).

Figure 2. Die Photograph of the μPD42505

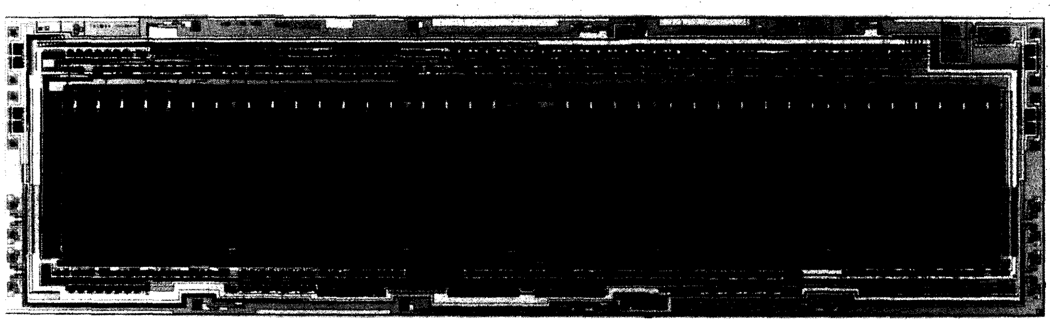


Figure 3. Dual-Port Static Storage Cell Array

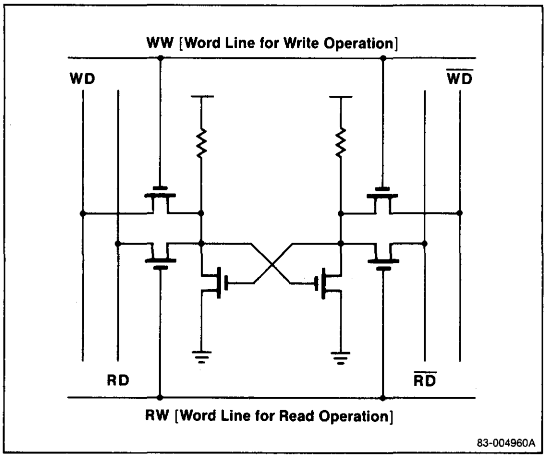
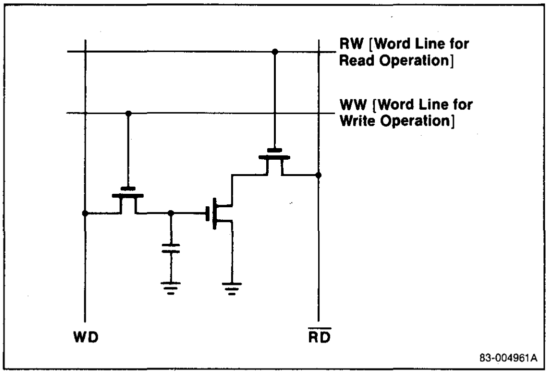


Figure 4. Dual-Port Dynamic Storage Cell Array



The static storage cell has separate word lines for write and read cycles (RW and WW), as well as differential data inputs (RD/$\overline{RD}$ and WD/$\overline{WD}$) for high-speed operation (figure 3). The three-transistor, one-capacitor dynamic storage cell contains separate write and read data and word lines, two access transistors, and a third transistor for cell signal pre-amplification (figure 4). Pre-amplification is required since there are only eight data amplifiers, one each for the eight input/output ports.

Unlike the static cell, the dynamic cell uses only one write and read data line and cannot take advantage of differential sensing. Although the speed is slower, its fewer components make this cell more suitable for compact layout and high device integration. The success of these high-speed buffers lies in the matching of the static and dynamic cells to achieve high performance at a low cost (figure 5).

Addressing

On a cold start, initial writing and reading to the device requires fast access times from the six-transistor static cell. While the first eight bytes are being accessed from the static cell, the first row of the dynamic cell is preselected. To achieve relatively fast dynamic access, the dynamic array is split into two segments and storage interleaving is employed.

From a functional point of view, the line buffer is a long, eight-bit-wide shift register. Its layout is compacted to produce a small die size. The chip has two arrays, each representing one-half of the line length. For the 1135 x 8 device, each subarray is organized as 568 bytes (71 x 8 bytes).

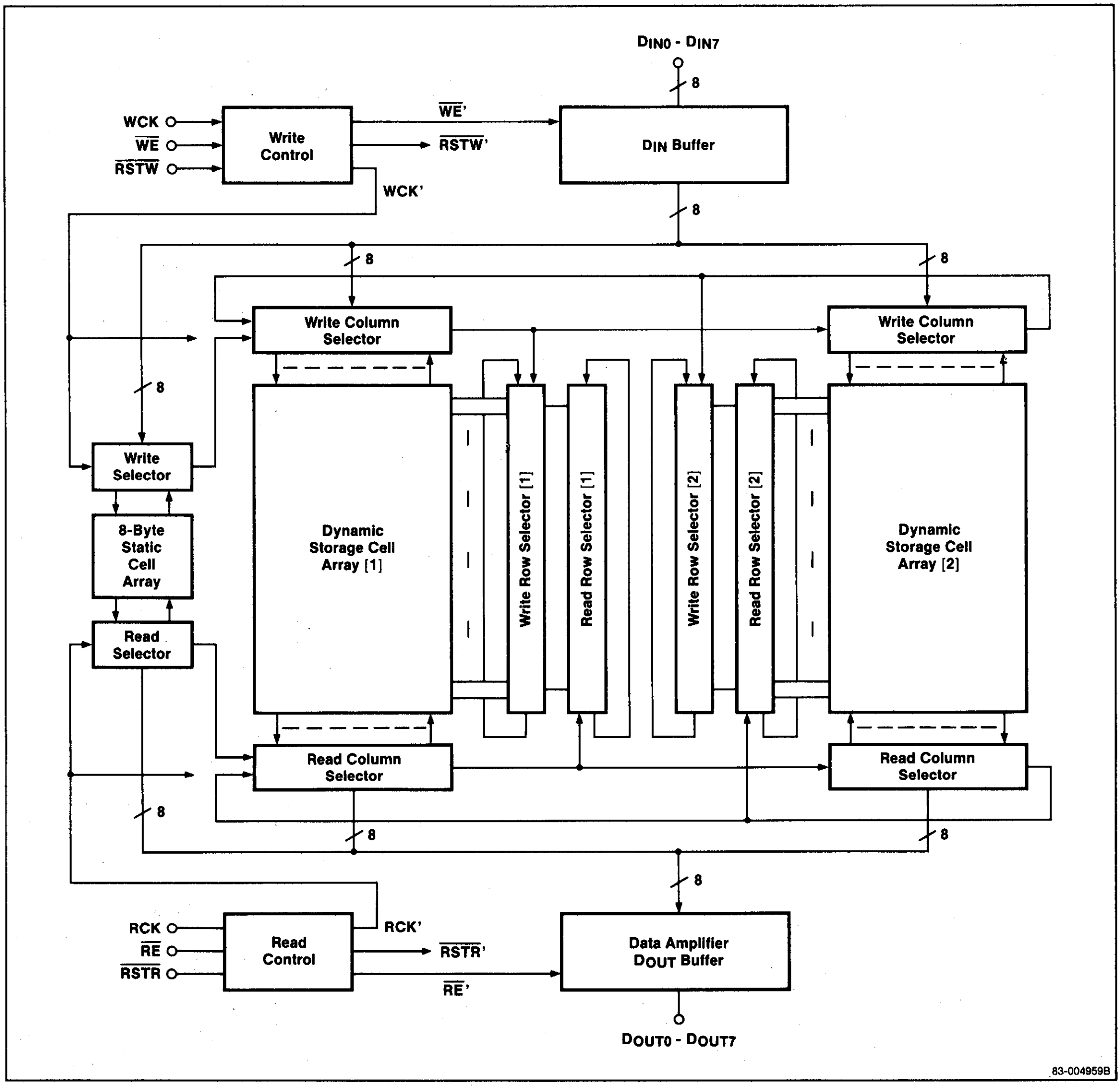
The serial addresses are generated automatically using column and row selectors for both write and read operation. The following steps summarize the interleaving sequence.

- In a reset cycle, data is read from the 8-byte static cell, and the first row of subarray 2 is preselected.
- Row 1 of dynamic subarray 2 is accessed, and the address pointer moves to subarray 1 for preselection.
- Row 1 of subarray 1 is read, and row 2 of subarray 2 is preselected.
- Interleaving continues between the subarrays until the last address is accessed, at which time the internal pointer automatically resets to address 0.

The address pointers are shift registers wired as ring counters and clocked in a wraparound fashion to control writing and reading of data at specific locations. The shift registers are incremented by one address for each WCK or RCK clock. Separate write and read address pointers are required to execute write and read cycles independently and at different speeds.

3

Figure 5. Block Diagram



Write and Read Timing

The μPD41101, μPD41102, and μPD42505 are equipped with the following pins: D_{IN0} through D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK for write operation and D_{OUT0} through D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK for read operation (figures 6 and 7). Serial addresses are automatically generated by an internal address counter. When $\overline{WE}$ is low, one byte is written to each address in synchronization with the WCK write clock (refer to the individual data sheets for timing diagrams); the internal write address pointer increments by 1 with each falling edge of WCK. Write data must meet the specified setup and hold times as measured from the rising edge of WCK.

Figure 6. Configuration of 24-Pin Plastic DIP (and Miniflat for μPD41101, μPD41102 only)

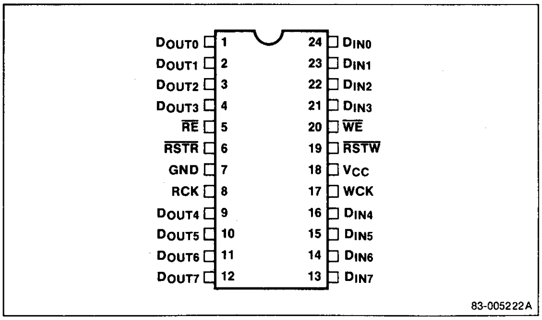
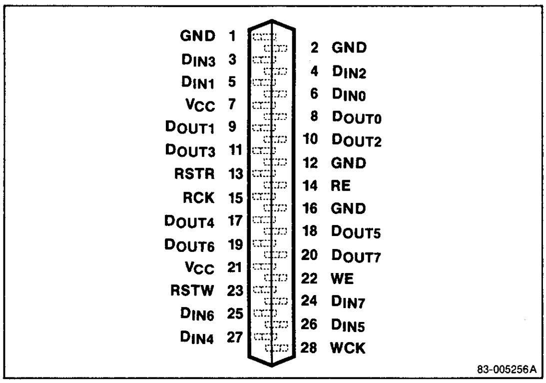


Figure 7. Configuration of 28-Pin Plastic ZIP (μPD42505 only)



The signal on $\overline{RSTW}$, which is used to reset the write address pointer to 0, also has setup and hold requirements with respect to the write clock.

When the signal on the read enable ($\overline{RE}$) pin is low, one byte of data is read out of the device for each RCK clock cycle, and the read address pointer increments by 1. The read address pointer is totally independent of the write address pointer.

The control functions of $\overline{WE}$ and $\overline{RE}$ are shown in figure 8. Bringing these two signals high (inactive) stops the internal address pointers; activating them again causes the internal pointers to increment to the next sequential address.

Synchronous Operation

Figure 8 shows the internal timing sequences, including those for address transitions and write cycles, during synchronous operation of these devices. With a common write and read clock, the internal write period is delayed from the write address. This delay, required when the write and read addresses are identical, allows a read cycle and then a write cycle to be executed to the same cell location. Read data is taken from the previously written line.

Designing with NEC's Line Buffers

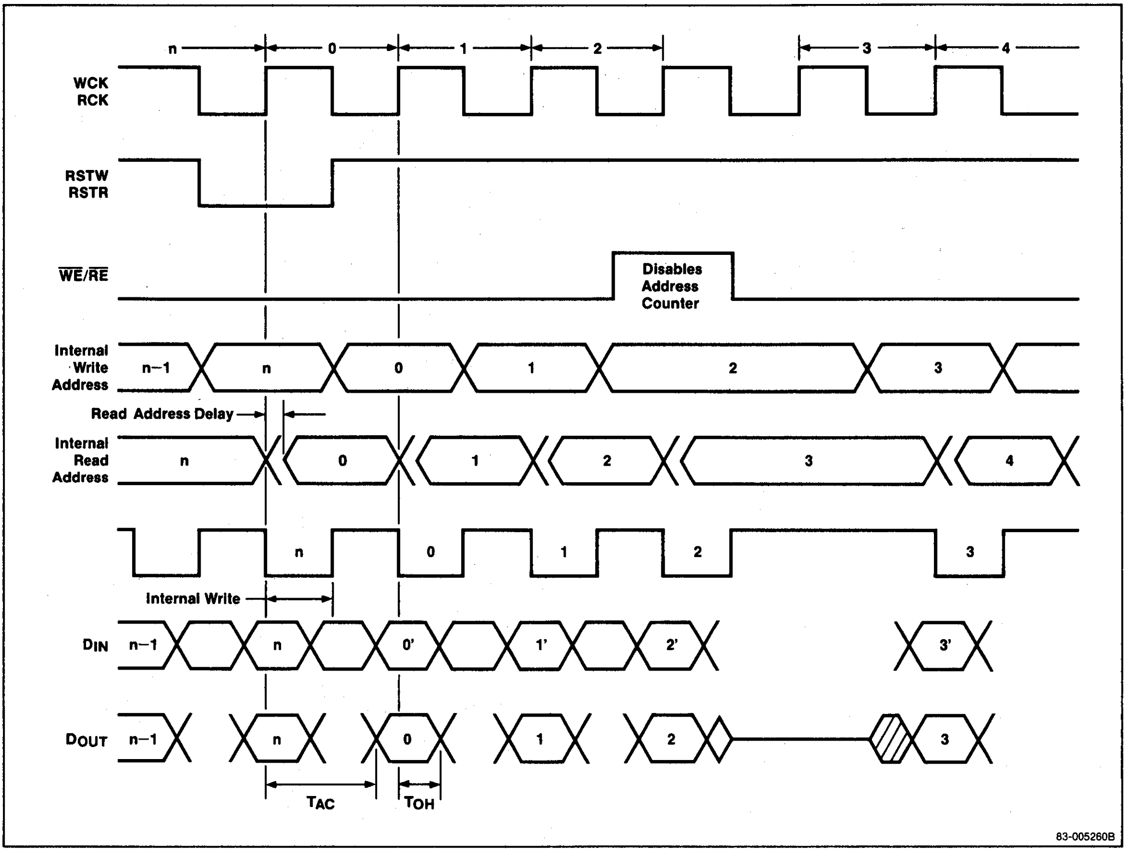
Initialization

After power has been applied, the write and read address pointers are undefined and therefore need to be set to address 0. Proper timing for a $\overline{RSTR}$ or $\overline{RSTW}$ reset cycle is described in the individual data sheet for each device.

Refreshing

Refreshing of the dynamic storage cells must be performed at regular intervals. Data remains valid for 1 or 5 ms, depending on the line length of the device (1 ms for the μPD41101 or μPD41102 and 5 ms for the μPD42505). Since NEC's line buffers contain only data amplifiers and no sense amplifiers, a standard read cycle does not refresh the storage cell. If longer hold times are required, the original data must be rewritten to the same address.

Figure 8. Internal Timing for Synchronous Operation



Minimum Delay Length

Unlike register-based line buffers, which use a data flow-through cycle, NEC's line storage elements are not capable of reading data immediately after it has been written. Each device requires a minimum delay, as calculated by the equations shown in table 2.

Table 2. Calculating Minimum Delay

Part Number	Equation
μPD41101	1/2 write cycle + 300 ns (34 ns/2 + 300 ns)/34 = 9.3 or 10 cycles
μPD41102	1/2 write cycle + 300 ns (28 ns/2 + 300 ns)/28 = 11.2 or 12 cycles
μPD42505	1/2 write cycle + 500 ns (50 ns/2 + 500 ns)/50 = 10.5 or 11 cycles

Delay length, as measured by the number of cycles, is dependent on the speed of the clock, i.e., at 14.3 MHz, the minimum delay for the μPD41101 would be 5 cycles.

Storage Contention

In asynchronous operation, when write and read cycles contend for the same line, the last "n" bytes (where "n" may be 5-12 bytes) of line output are taken from the previous line. This type of contention occurs most frequently when executing continuous write and read cycles at different rates, such as when converting video images from interlaced to noninterlaced scanning. In this case, the read clock operates at twice the speed of the write clock. Near the end of the line, the read cycle catches up and contends with the write cycle.

Setting Delay Length

Varying the Reset Interval in Synchronous Operation. Depending on the application, some schemes for implementing delay length suit system timing better than others (see individual data sheets for timing). In synchronous operation, the delay is set simply by varying the interval between the reset pulses. In this case, the reset clocks are tied together. Since write and read clocks are common, line delay is determined by the offset between resets.

Varying the Reset Interval in Asynchronous Operation. In asynchronous operation, the reset interval can be varied using independent clocks and reset signals. Delay length is calculated as the timing difference between the write and read reset pulses.

Controlling the $\overline{RE}$ Pin. In the third option, the read enable pin ($\overline{RE}$) can be used to control read operation and the read address counter. When $\overline{RE}$ is high (disabled), the read address counter does not increment and no data is output. After the desired delay, $\overline{RE}$ can be brought low to begin executing read cycles. For delays exceeding one line length, care must be taken to ensure that new data is not written into an address before the old data is read.

3

μPD42505 Large-Capacity Line Buffer

The μPD42505 was designed for applications where a large amount of data is handled per line, e.g., in high-performance digital copiers and G3 or G4 facsimile machines requiring buffer storage for image compression, expansion, data transmission, and in some cases, image enhancement using filtering techniques for digital signal processing. The 5K x 8 line length has also been used in some designs to hold the data tokens in digital filtering arrays.

Although line buffering can be achieved using fast static RAMs as shown in figure 9, the need for two devices and other complicated peripheral circuits necessarily increases the cost of a system and makes it more difficult to implement. The μPD42505 eliminates the complexity and high cost by providing the same functions and more advantages in one package.

Figure 9. System Design Using Static RAMs Versus High-Speed Line Buffer

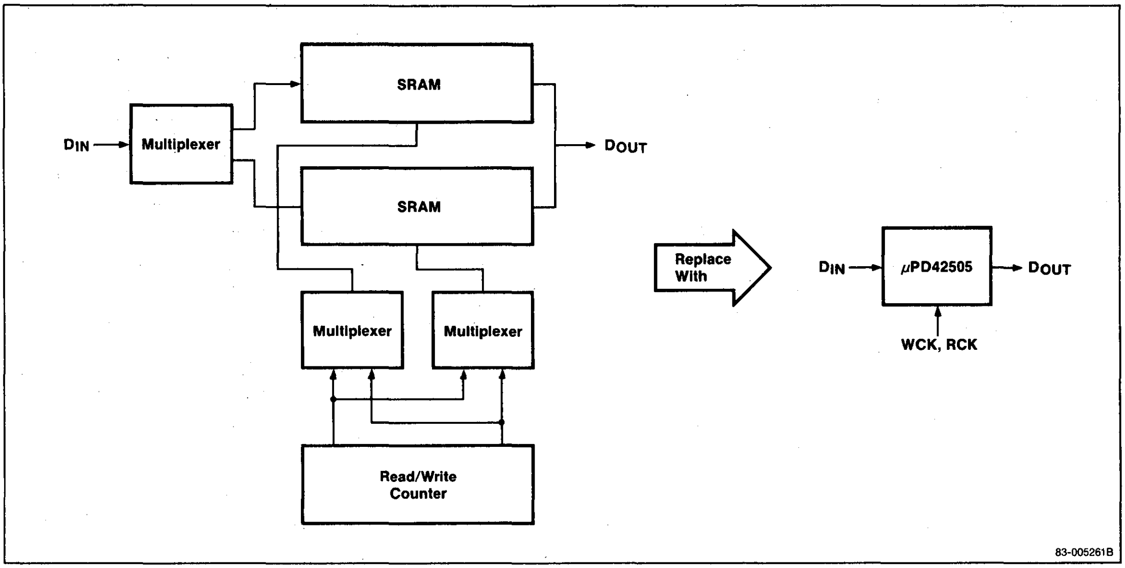
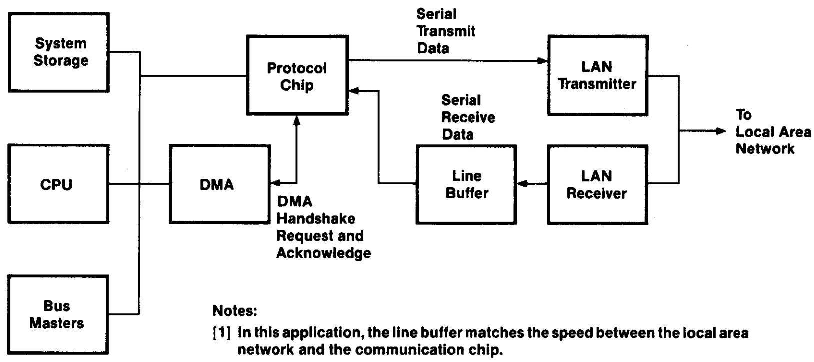


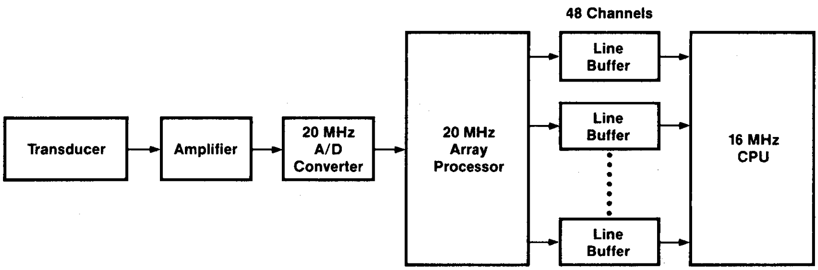
Figure 10. Line Buffering in Local Area Networks



Notes:
[1] In this application, the line buffer matches the speed between the local area network and the communication chip.

83-005262B

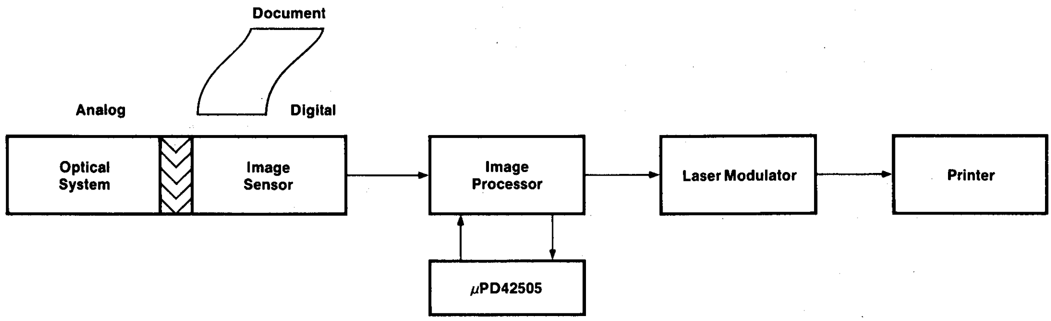
Figure 11. Elastic Storage for Digital Signal Processing Applications



Notes:
[1] Line buffers synchronize data flow between two asynchronous processors.

83-005263B

Figure 12. Image Enhancement Techniques in High-Performance Digital Copiers



Notes:
[1] In this application, a large-capacity line buffer is used to hold token data for digital signal processing.

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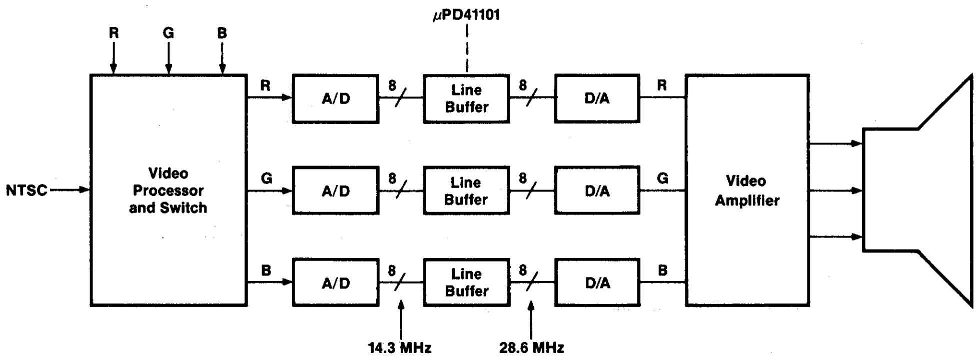
Figure 13. Doubling the Line Rate in Scan Conversion



Notes:
[1] In high-definition TV applications, the line buffer is used to double the scan rate by reading at twice the write frequency.

83-005265B

NEC
NEC Electronics Inc.

APPLICATION NOTE 58 INTERLACED TO NONINTERLACED VIDEO SCANNING USING THE μPD41101 HIGH-SPEED LINE BUFFER

Introduction

Interlaced scanning is used in television, videotape, and videocassette recording applications to reduce bandwidth and maintain an acceptable amount of screen flicker in video signals. The procedure involves lowering the vertical resolution and doubling the number of fields so that one complete frame is formed from the first and second fields. When a video signal subsequently is decoded and ready for display on a monitor or TV, bandwidth generally is no longer a problem and the higher vertical resolution of a noninterlaced signal may be used to produce a sharper image on the screen.

In NTSC TV systems, there are 262.5 scan lines per field, 2 fields per frame, and 30 frames per second (figure 1). With the resolution per field in the vertical direction lowered by interlaced scanning, the lines become rougher and the gap between scanned lines more visible. This drawback becomes all the more conspicuous in larger-screen TVs.

Vertical resolution problems caused by interlaced scanning can be resolved by first repeating the signal of each scan line. The number of scan lines per field then can be doubled by doubling the horizontal frequency and keeping the vertical frequency intact. Subsequently, an interlaced signal can be converted to a noninterlaced signal to increase the resolution of the picture in the vertical direction (figure 2).

The conversion from interlaced to noninterlaced scanning can be achieved by temporarily storing each line in a buffer and then displaying it twice to double the number of lines per field (figure 3).

3

Figure 1. Relationship of Field to Frame in Interlaced Scanning

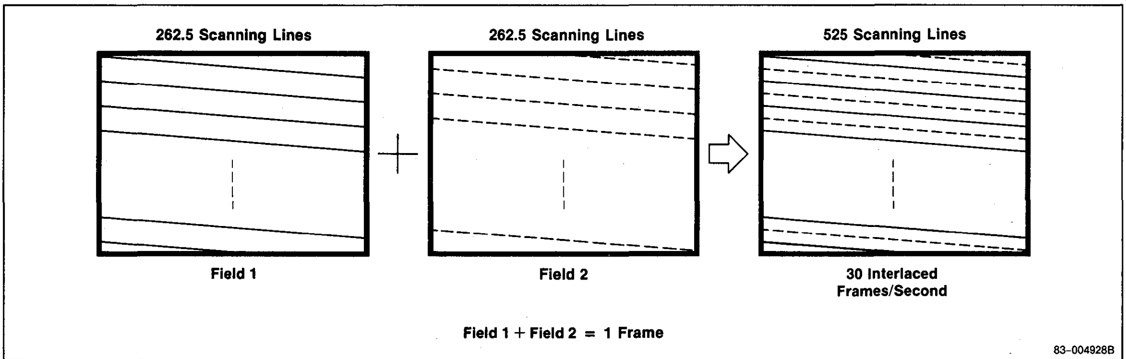


Figure 2. Difference Between Interlaced and Noninterlaced Scanning

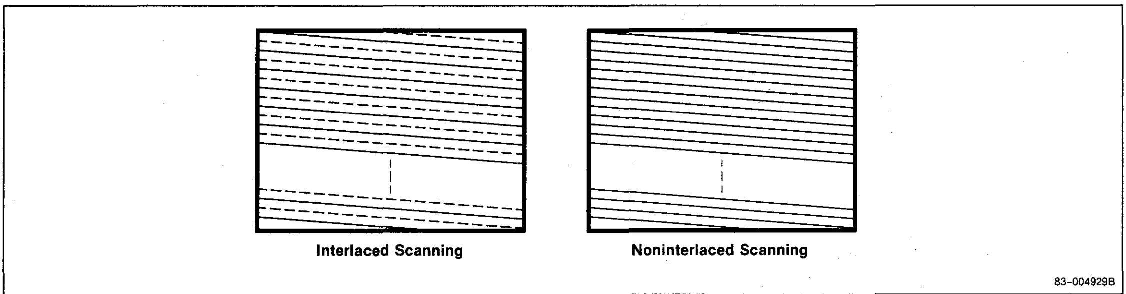


Figure 3. Doubling the Line Rate

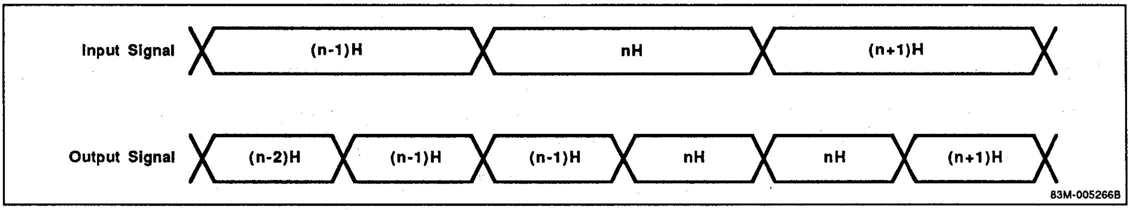
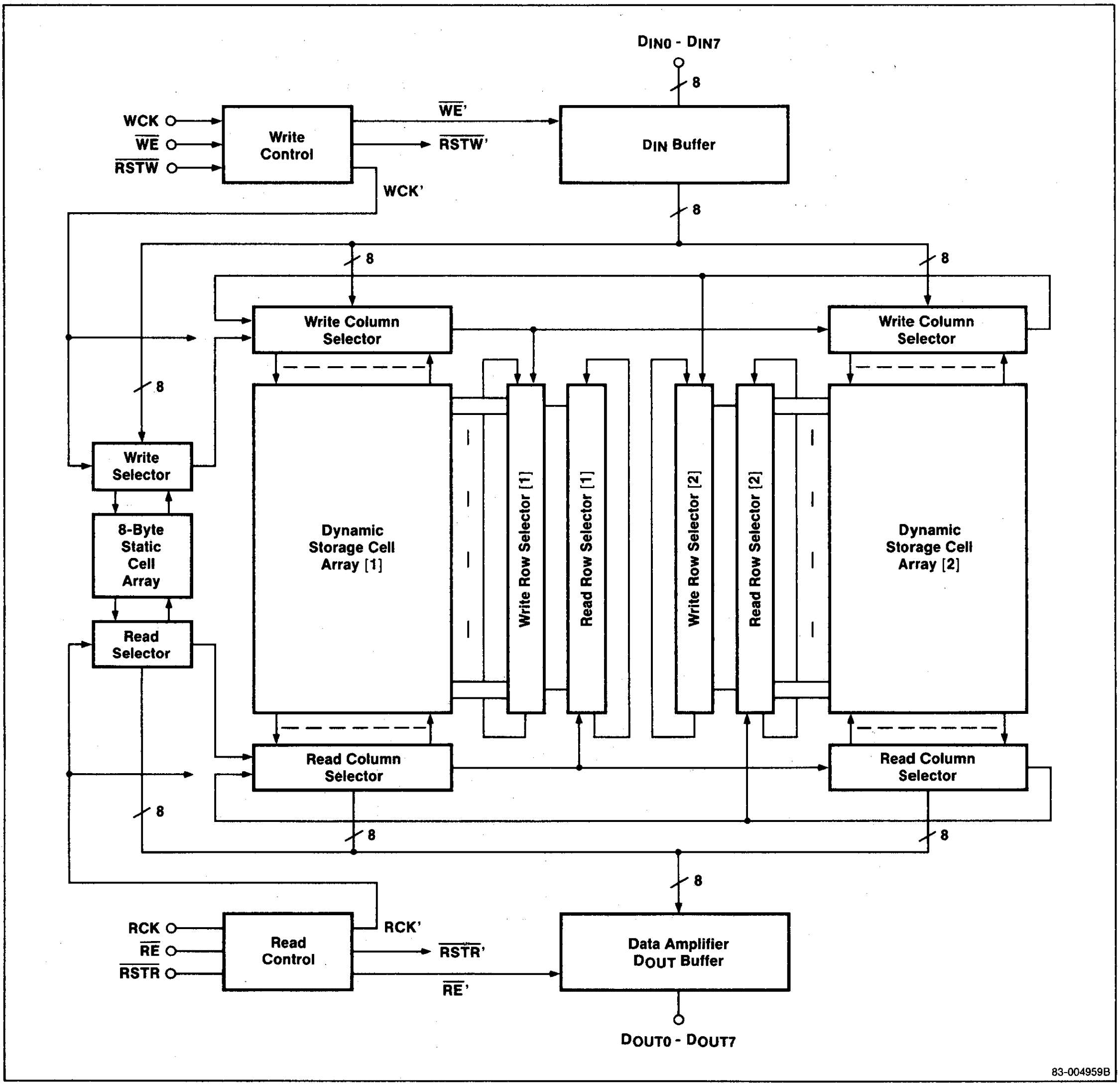


Figure 4. Block Diagram



The μPD41101 High-Speed Line Buffer

The type of scan conversion described in this application note requires buffer storage for each line. Required storage is calculated by dividing the scanning period per line by the sampling period to determine the number of samples per line. Required storage for NTSC systems is computed as shown in the following sequence.

(1) Scanning period per line:

$$\frac{1}{\left(\frac{525\text{ lines}}{\text{frame}} \times \frac{30\text{ frames}}{\text{second}}\right)} = 63.5\,\mu s$$

(2) Minimum sampling frequency:

$$3.58\text{ MHz} \times 4 = 14.32\text{ MHz} = 69.83\text{ ns}$$

(3) Samples per line:

$$63.5\,\mu s/69.8\text{ ns} = 909.7\text{ samples}$$

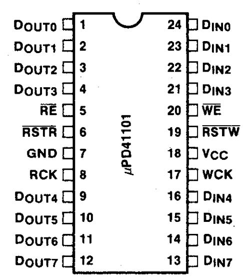
This application requires the storing of 910 words, exactly one horizontal scanning line of data. NEC's μPD41101 high-speed line buffer, configured as 910 words by 8 bits, is ideally suited for the digital processing of video signals because one-line delays and time axis conversions can be executed easily.

The μPD41101 differs from general-purpose static devices in that it doesn't require a double-buffer configuration (figure 4). Writing and reading can be executed independently and asynchronously. Since an internal address pointer eliminates the need for external address generation, the only external controls required are those for the WCK and RCK write and read clocks and the $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ write and read reset signals (see figure 5 for pin assignments). As shown in table 1, three versions of the μPD41101 are available.

Table 1. Access and Cycle Times of the μPD41101

Part Number	Access Time (max)	Write Cycle Time (min)	Read Cycle Time (min)
μPD41101-3	27 ns	34 ns	34 ns
μPD41101-2	27 ns	69 ns	34 ns
μPD41101-1	49 ns	69 ns	69 ns

Figure 5. μPD41101 Pin Configuration



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Operation

Write and Read Reset Cycles. After power is applied to the μPD41101, its internal address pointers are undefined and must be initialized to address 0. As shown in figure 6, the inputs on $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ have required setup and hold times as measured from the rising edges of WCK and RCK, respectively.

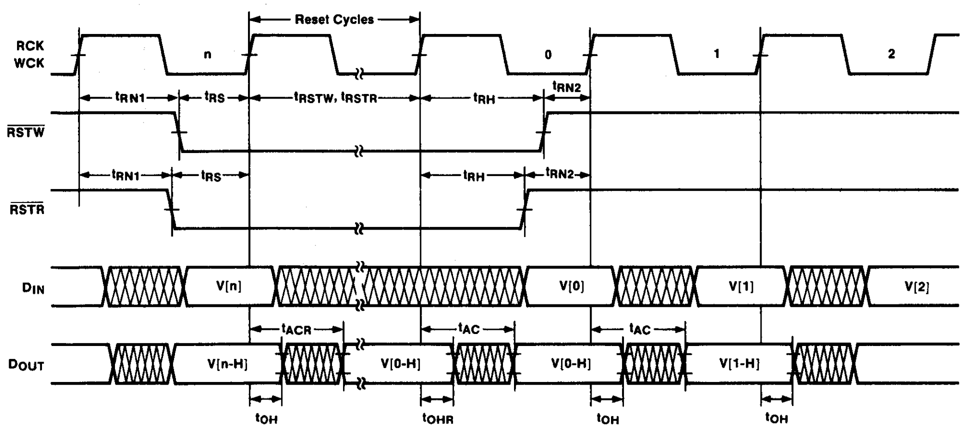
Write Cycles. Write cycles are executed in synchronization with the WCK clock (figure 7). When $\overline{\text{WE}}$ is low, 8 bits of data are sampled from D_{IN0}-D_{IN7} at the rising edge of WCK and the internal write pointer increments to the next sequential address. When the pointer reaches the last address, it wraps around to address 0 again. When high, $\overline{\text{WE}}$ disables write operation and inhibits the write address pointer. Write data must satisfy required setup and hold times as specified from the rising edge of WCK.

Read Cycles. When $\overline{\text{RE}}$ is low, read cycles are executed in synchronization with the RCK clock (figure 7). Read data is output from D_{OUT0}-D_{OUT7} after a specified access time as measured from the rising edge of RCK. The internal read pointer functions identically to the write pointer, except that the read address increments sequentially with each RCK clock.

Example of System Configuration

The block diagram in figure 8 shows a hardware system designed to convert a standard NTSC interlaced video signal to a noninterlaced signal. In this configuration, described on the following pages, the input signals derive either from an NTSC composite signal (video input), from a TV/VTR/VCR, or from the R-G-B signal output of a personal computer.

Figure 6. Write or Read Reset Cycle



Note:

[1] $\overline{\text{WE}} = \overline{\text{RE}} = V_{IL}$.

[2] V = Valid Data.

[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 910 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

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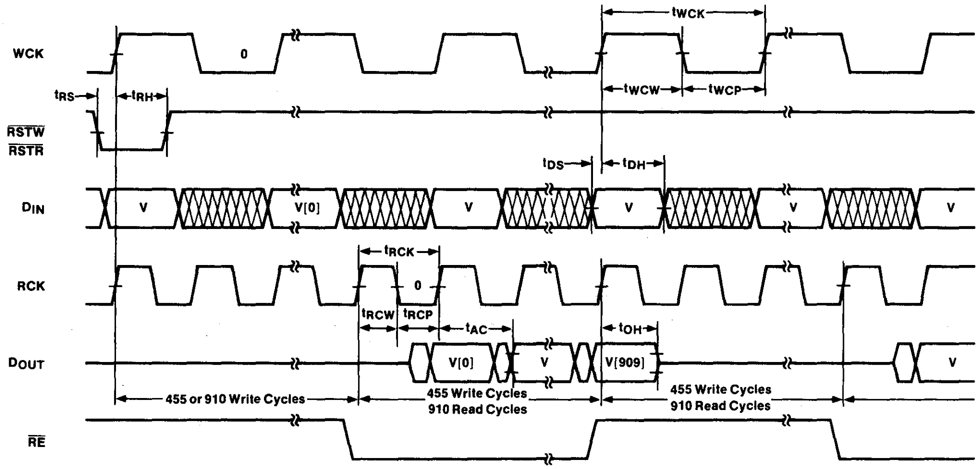
Figure 7. Write or Read Cycle



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

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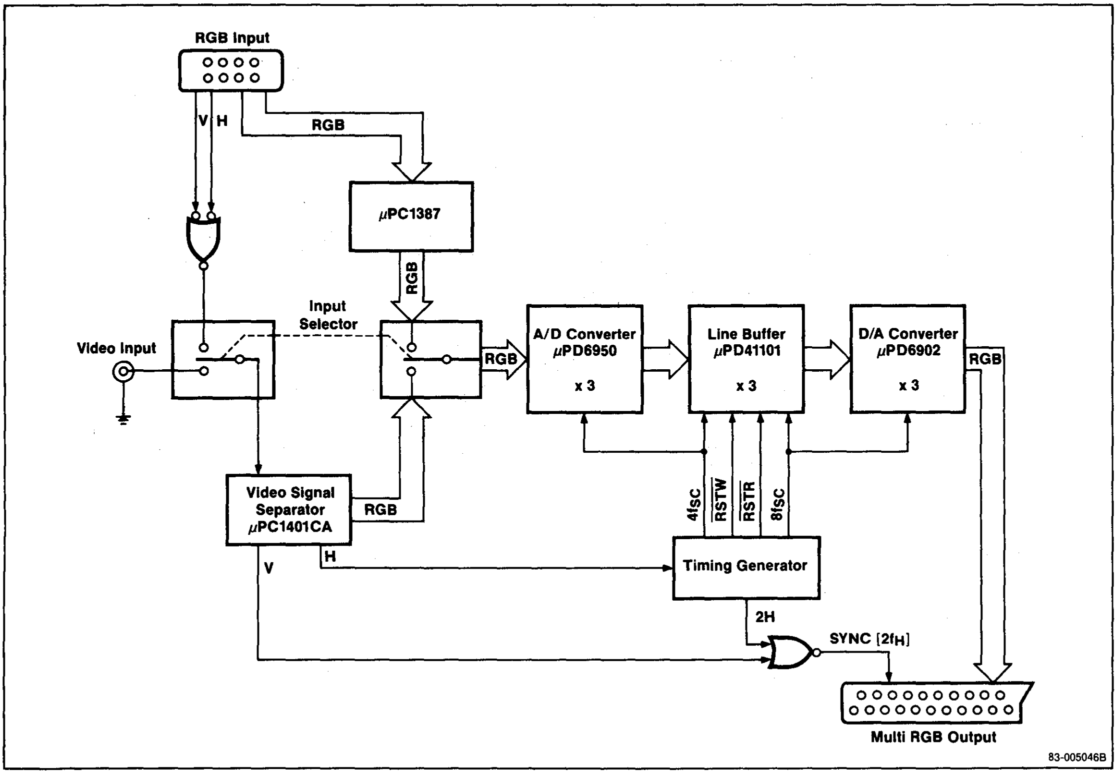
3

Figure 8. Scan Converter Block Diagram



Video Signal Processor

The video signal is decoded from the R-G-B inputs by NEC's μPC1401, a device specifically designed to process the color, video, and synchronizing signals used in NTSC color TV systems (figures 9 and 10). By separating the signals, the μPC1401 can independently control them and thereby reduce the number of peripheral devices usually required in this phase.

Figure 9. μPD1401 Block Diagram

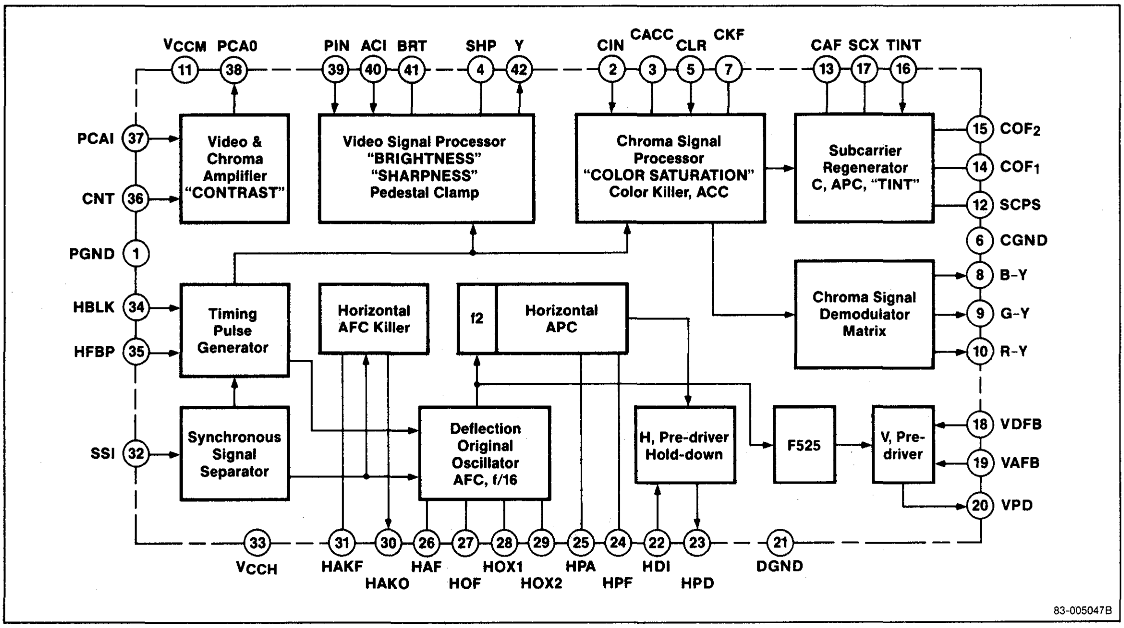


Figure 10. μPD1401 Pin Configuration

Picture Ground	PGND	1	42	Y	Video Output
Chroma Input	CIN	2	41	BRT	"BRIGHTNESS"
ACC Capacitor	CACC	3	40	ACI	Aperture Correction Input
"SHARPNESS"	SHP	4	39	PIN	Video Input
"COLOR SATURATION"	CLR	5	38	PCAO	Video & Chroma Amplified Output
Chroma Ground	CGND	6	37	PCAI	Video & Chroma Amplifier Input
Color Killer Filter	CKF	7	36	CNT	"CONTRAST"
B-Y Output	B-Y	8	35	HFBP	Horizontal Flyback Pulse Input
G-Y Output	G-Y	9	34	HBLK	Horizontal Blanking Input
R-Y Output	R-Y	10	33	V_{CCH}	Horizontal Power Supply
Master Power Supply	V_{CCM}	11	32	SSI	Synchronous Signal Separator Input
Subcarrier Phase Shifter	SCPS	12	31	HAKF	Horizontal AFC Killer Filter
Chroma APC Filter	CAF	13	30	HAKO	Horizontal AFC Killer Output
Chroma VCO Filter 1	COF_1	14	29	HOX2	Horizontal VCO Resonator 2
Chroma VCO Filter 2	COF_2	15	28	HOX1	Horizontal VCO Resonator 1
"TINT"	TINT	16	27	HOF	Horizontal VCO Filter
Subcarrier Resonator	SCX	17	26	HAF	Horizontal AFC Filter
Vertical DC Feedback	VDFB	18	25	HPA	Horizontal Phase Adjuster
Vertical AC Feedback	VAFB	19	24	HPF	Horizontal APC Filter
Vertical Predrive Output	VPD	20	23	HPD	Horizontal Predrive Output
Deflection Ground	DGND	21	22	HDI	Hold Down Circuit Input

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3

R-G-B Signal Processor

The level of the R-G-B output signals from the personal computer are adjusted by a μPC1387 (figures 11 and 12). An interface between the digital R-G-B signals and the TV color signal output, the μPC1387 provides high-speed switching by means of a built-in R-G-B signal converter and sophisticated circuitry that blanks the signal levels. The horizontal (H) and vertical (V) synchronizing signals from the personal computer are combined into a composite synchronizing signal. When the selector switches to the R-G-B input position, the composite signal is applied to the μPC1401 in place of a TV signal.

Figure 12. μPD1387 Pin Configuration

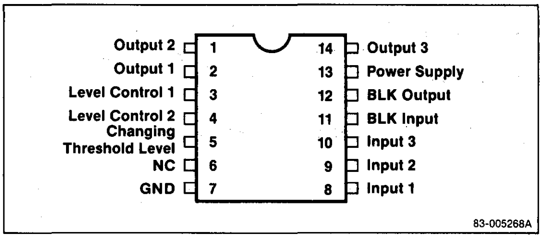
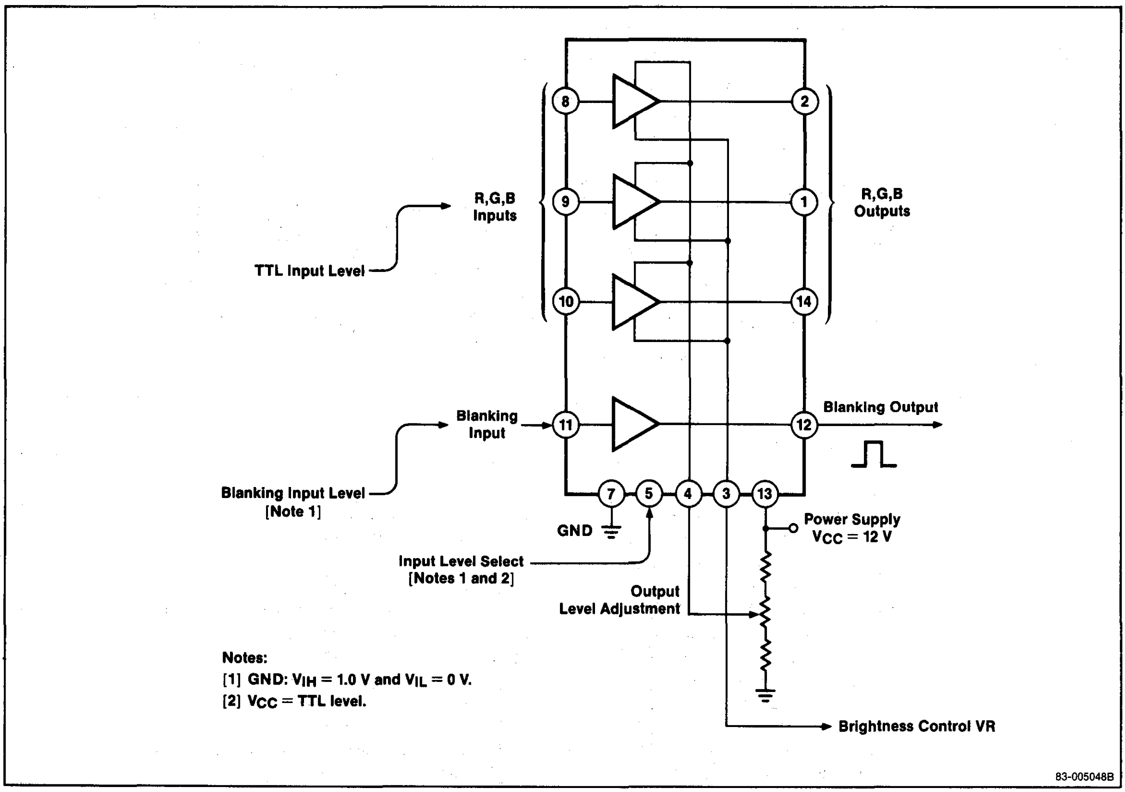


Figure 11. μPD1387 Block Diagram



Analog-to-Digital Converter

The input selector chooses one of the two R-G-B signals from the μPC1401 and μPC1387 and passes it to the μPD6950, where it first is sampled at a clock frequency equal to $4f_{SC}$ (14.3 MHz) and then written to the μPD41101 line buffer. The CMOS-fabricated μPD6950 is an analog-to-digital (A/D) converter whose high speed and low power consumption are particularly suited to video applications (figures 13 and 14).

Figure 13. μPD6950 Pin Configuration

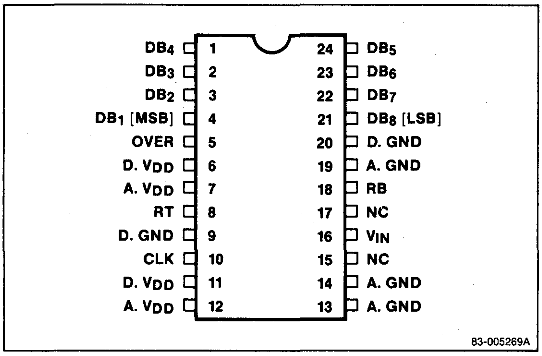
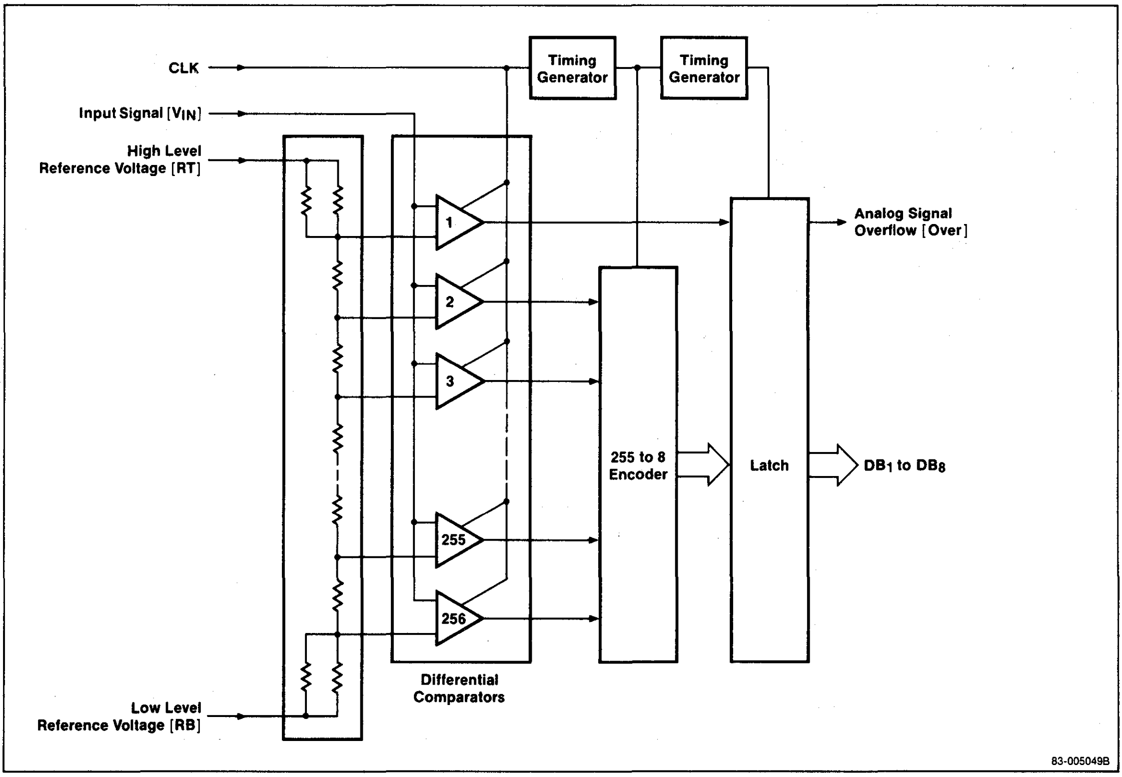


Figure 14. μPD6950 Block Diagram



Line Buffer

This configuration uses a total of three μPD41101 line buffers, one each for the R-G-B inputs. Independent control of write and read operation by the μPD41101 allows the inputs to be written at a $4f_{SC}$ sampling rate and subsequently read at twice that frequency ($8f_{SC}$). Reading the scanned image twice doubles the number of lines sent to the TV monitor, fills the gaps between lines of an interlaced signal, and increases the vertical resolution.

Digital-to-Analog Converter

After being read at a frequency of $8f_{SC}$ (28.6 MHz), the digital signal from the μPD41101 is converted to an analog signal by the μPC6902 (figures 15 and 16). The CMOS-fabricated μPC6902 D/A converter is designed to handle 50 million samples per second.

Timing Generator

The $8f_{SC}$ and $4f_{SC}$ clocks and $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ signals are output by the timing generator. The horizontal (H) signal from the μPC1401 passes to a phase-locked loop circuit, where it is compared and locked with a horizontal signal obtained by dividing the $8f_{SC}$ clock. After the horizontal frequency has been multiplied by 2 (2H), this signal is combined with the vertical drive signal (V) from the μPC1401 for use as the composite synchronizing signal in noninterlaced scanning. Together with the R-G-B output signals, it is then passed to the TV monitor.

Figure 15. µPD6902 Pin Configuration

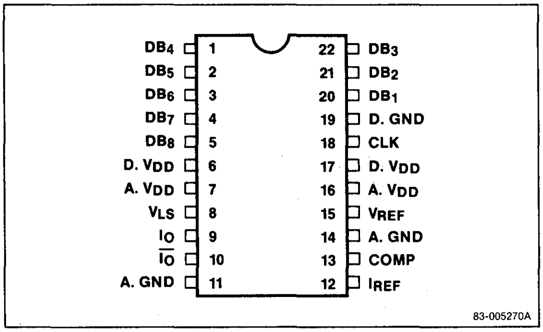
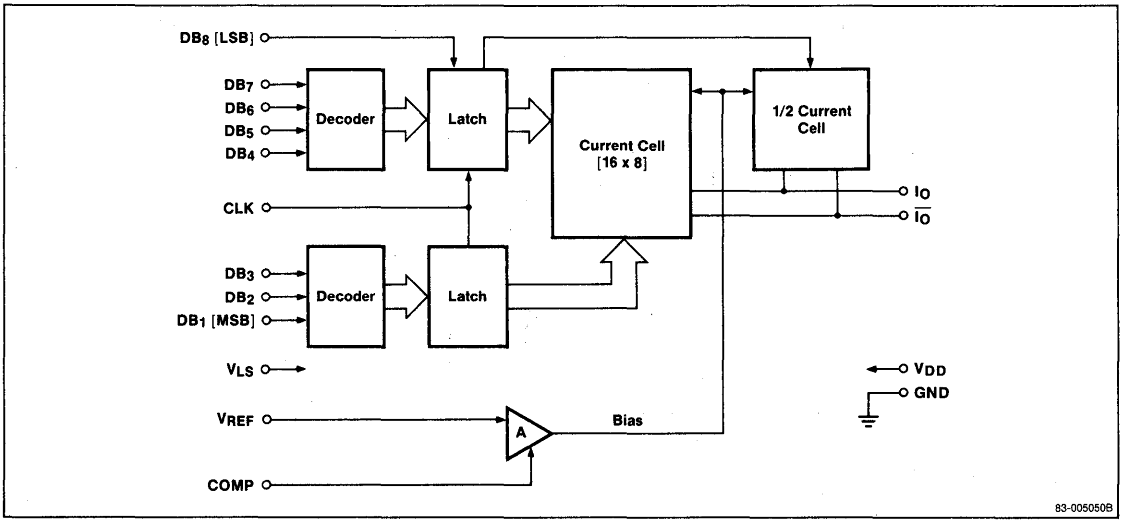


Figure 16. µPD6902 Block Diagram



Operation

A circuit diagram for the scan converter is shown in figure 17. The operation in each block is described below.

Video Signal Input Stage

Switch SW_1 selects the NTSC video signal and applies it to the μPC1401, which decodes the composite signal and outputs R-G-B horizontal and vertical synchronizing signals. The μPC1401 integrated circuit separates color types (Y, R-Y, B-Y, G-Y) to form a matrix using three external transistors (Tr_3-Tr_5) to produce the R-G-B signal.

A 4528BC one-shot multivibrator sets the horizontal synchronizing signal to a suitable pulse width. One of the pulse signals is applied to pins 34 and 35 of the μPC1401 as the burst gate and blanking pulses; the other signal is applied to the MC4044 phase comparator for clock generation comparison purposes.

R-G-B Signal Input Stage

The R-G-B input signal passes to a 74LS08 two-input positive AND gate and then to the μPC1387 which, together with Tr_6 and the 74LS08, ensures that no signal is applied during the horizontal retracing period.

The R-G-B signal applied to the μPC1387 is adjusted to a suitable level prior to being output from that device. Conversely, the vertical and horizontal synchronizing signals are combined in the 74LS08 to form the composite synchronizing signal passed to the μPC1401 by selection switch SW_1.

A/D Conversion Stage

The R-G-B signal selected by SW_1 is passed to the μPC6950 through a 7-MHz low-pass filter to cut frequencies in excess of one-half the sampling frequency of 14.3 MHz (figure 18). This analog signal is converted by the 14.3-MHz clock and then passed to the μPC1401 as an 8-bit digital signal.

Line Buffer Stage

The 8-bit digital input is written at 14.3 MHz before being passed to the μPC6902 for D/A conversion at 28.6 MHz. The WCK, RCK, $\overline{RSTW}$, and $\overline{RSTR}$ controls for the line buffer are supplied from the timing generator (figure 19).

D/A Conversion Stage

The digital input from the μPD41101 is converted to an analog signal by the 28.6-MHz clock to reproduce an R-G-B signal of twice the horizontal line frequency.

Timing Generation Stage

An LC oscillator circuit uses a 74F04 inverter to generate the 28.6-MHz signals required for driving the line buffer and D/A converter clocks, as well as the 14.3-MHz signals required for driving the line buffer and A/D converter clocks.

The horizontal signal from the μPC1401 is passed to the MC4044 phase frequency detector for phase comparison with the horizontal signal obtained by dividing the clock from the clock generator. The resultant signal is then transferred through a low-pass filter to the 1SV164 varactor diode of a voltage-controlled oscillator to adjust the oscillating frequency (figure 20).

Three 74LS163 synchronous 4-bit counters divide the 14.3-MHz clock by a factor of 455. The resultant 31.5-kHz clock ($2f_H$) is timed by the 28.6-MHz clock and passed to the line buffer as the $\overline{RSTR}$ signal.

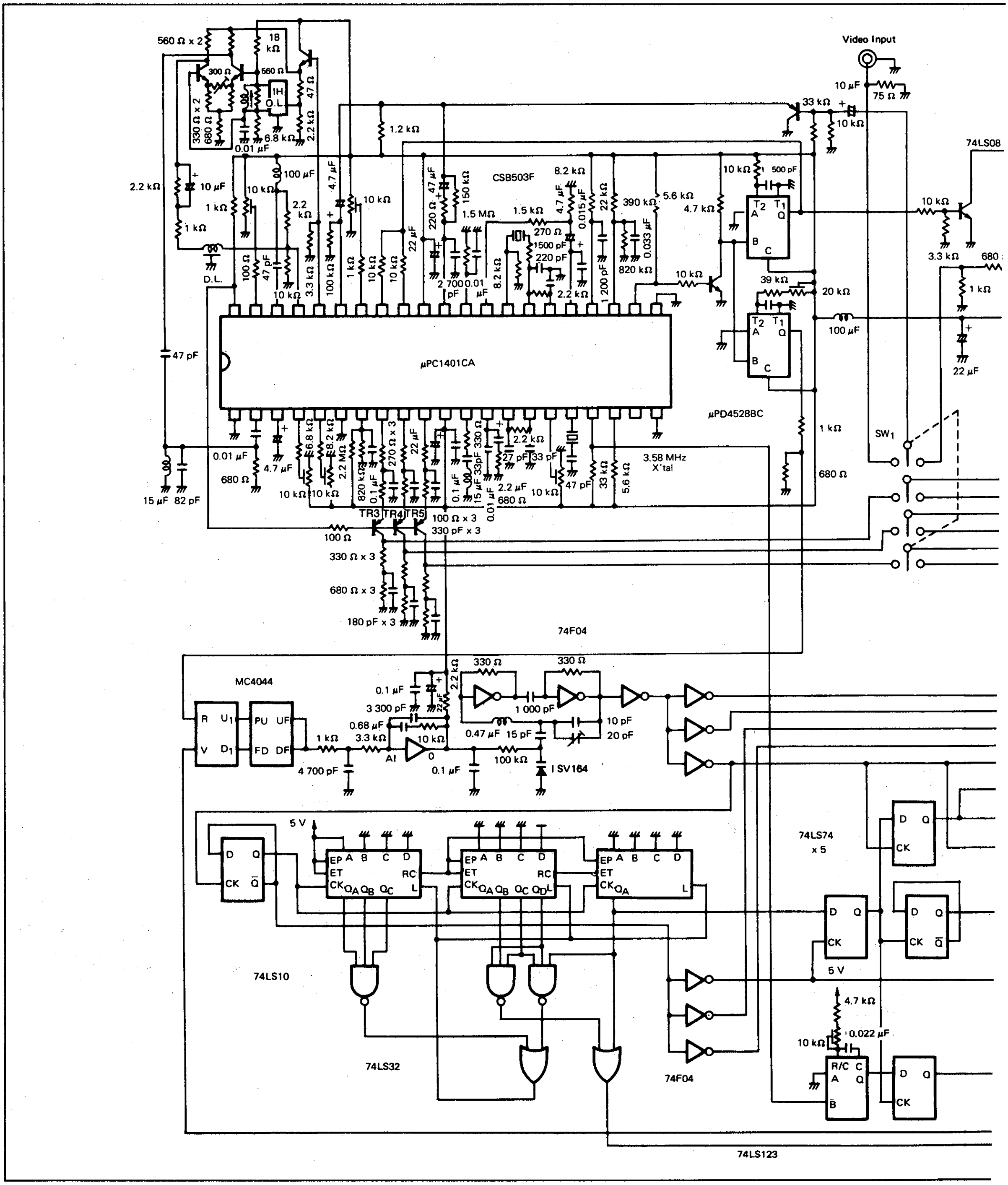
The vertical synchronizing signal from the μPC1401 is adjusted to a suitable pulse width by a 74LS123 retriggerable monostable multivibrator. The signal timed by this $2f_H$ clock is then combined with the $2f_H$ clock to obtain the composite synchronizing signal for noninterlaced scanning purposes. The $2f_H$ clock is subsequently divided in half and timed by the 14.3-MHz clock to become the $\overline{RSTW}$ signal passed to the line buffer and MC4044 (figures 21 and 22).

R-G-B Output Stage

The noninterlaced R-G-B signal and the composite synchronizing signal output to the TV monitor are adjusted to levels of 0.7 and 0.3 V_{PP}, respectively, by a 75-ohm terminating resistor. Switch SW_2 is used to select external or internal display. When on, the switch allows a noninterlaced picture to be displayed externally on a TV monitor.

In this application, the TV monitor must be capable of operating at a horizontal scanning frequency of 31.5 kHz. Suitable monitors include the PC-TV451 and PC-TV471 from NEC Home Electronics.

Figure 17. μPD41101 Composite Schematic



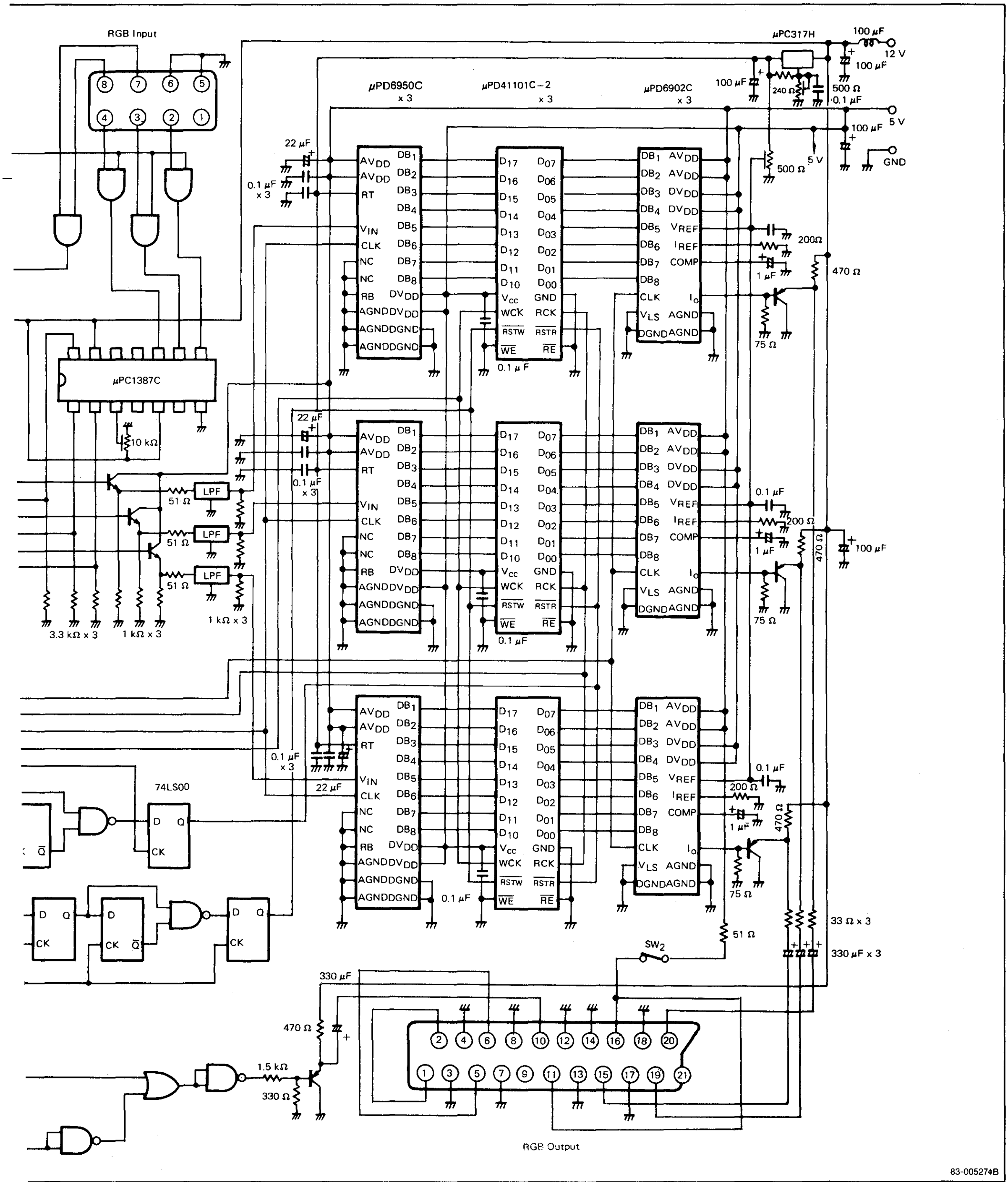
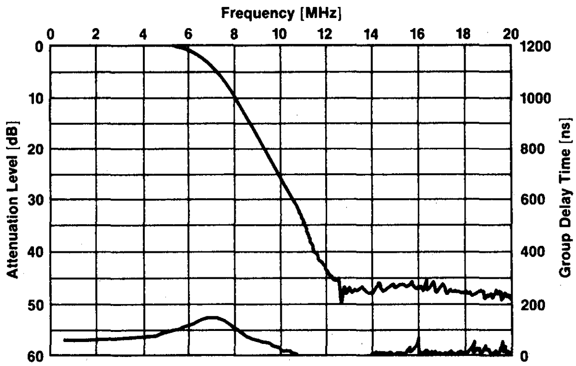

RGB Input
μPC317H
100 μF
12 V
100 μF
500 Ω
0.1 μF
240 Ω
5 V
GND
μPD6950C x 3
μPD41101C-2 x 3
μPD6902C x 3
22 μF
0.1 μF x 3
μPC1387C
10 kΩ
LPF
51 Ω
3.3 kΩ x 3
1 kΩ x 3
200Ω
470 Ω
1 μF
75 Ω
74LS00
33 Ω x 3
330 μF x 3
SW2
330 μF
1.5 kΩ
330 Ω
RGB Output
83-005274B

Figure 18. Characteristics of LT15LP7.0M01-32 Low-Pass Filter



Frequency [MHz]	Attenuation Level [dB]
0.2	0
7.0	3±2
14.0	40 or more

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Figure 19. ***Scan Conversion Timing***

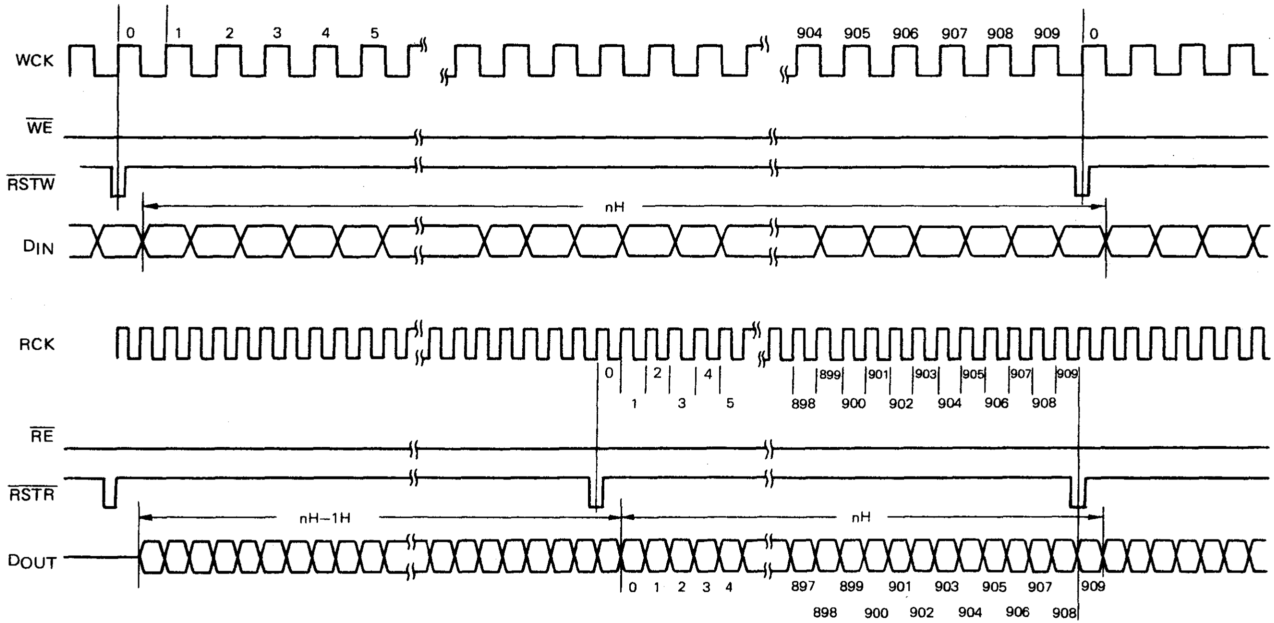

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Figure 20. Characteristic Curve of 1SV164

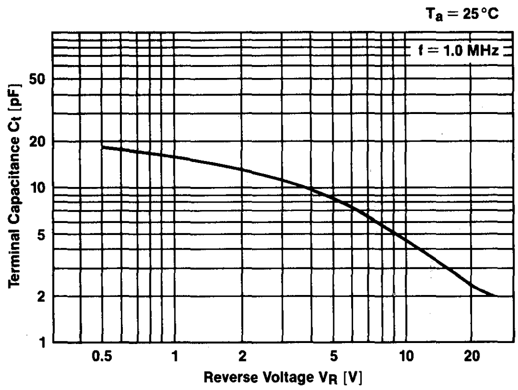


Figure 21. ***Counter Stage of Timing Generator***

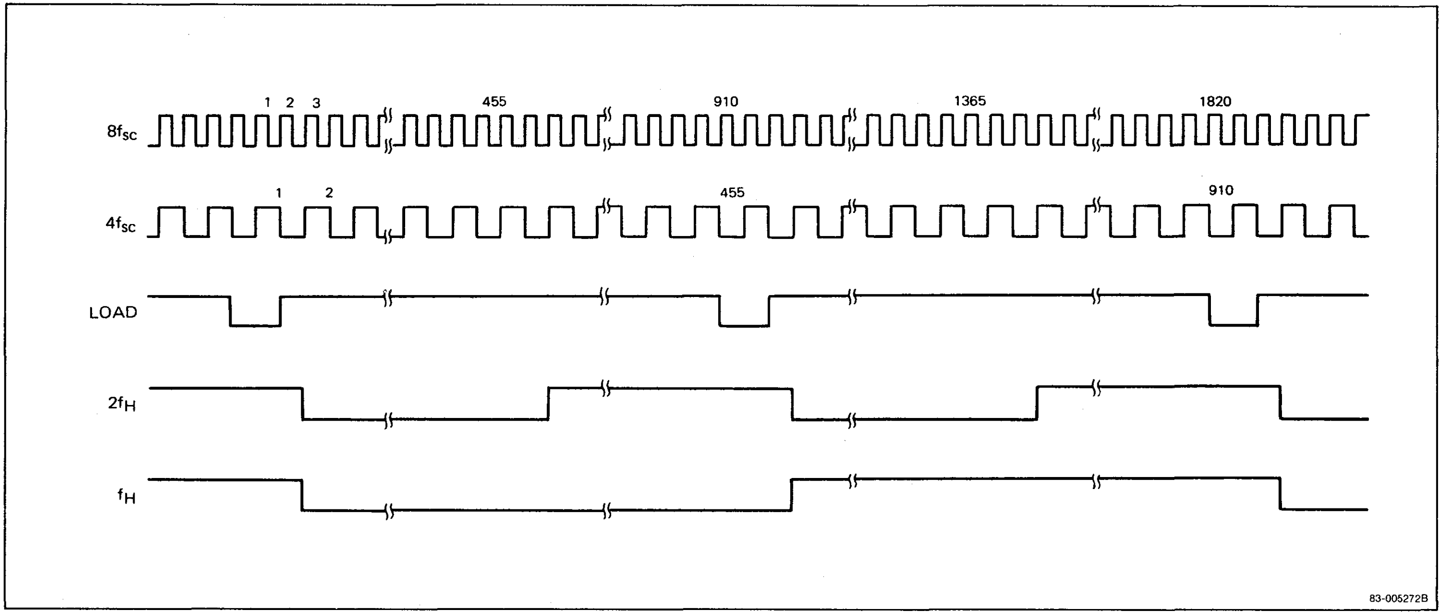
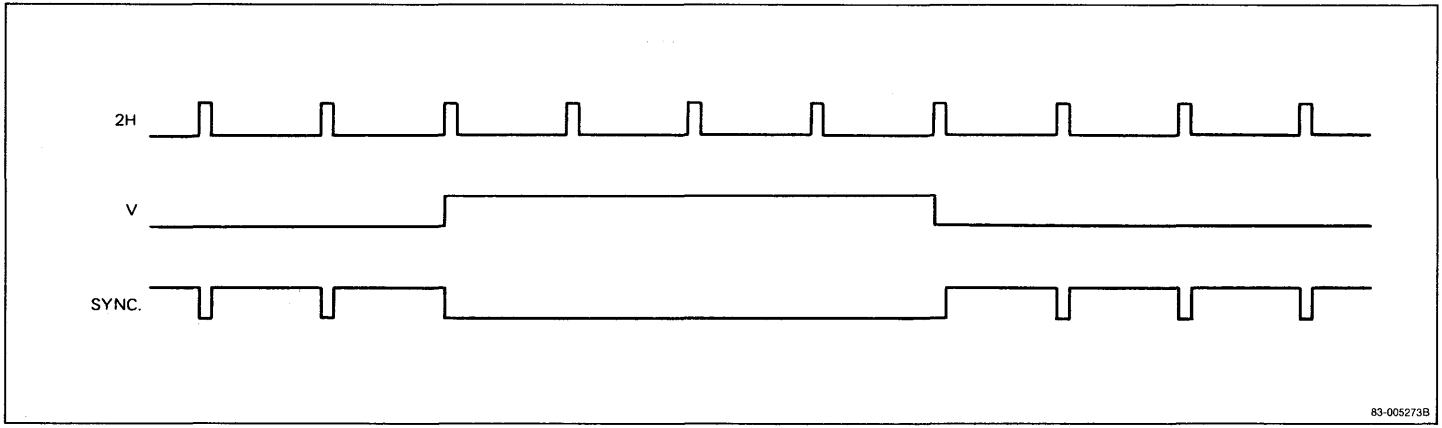


Figure 22. ***Synchronizing Signal Generator***



DYNAMIC RAM MODULES

4

Section 4
Dynamic RAM Modules

NEC
NEC Electronics Inc.

MC-41256A8
262,144 x 8-BIT
DYNAMIC NMOS RAM MODULE

Description

The MC-41256A8 is a 262,144-word by 8-bit NMOS RAM module designed to operate from a single +5-volt power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-41256A8 is functionally equivalent to eight μPD41256 standard 256K DRAMs. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-41256A8 includes eight μPD41256s in PLCC packages and eight power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

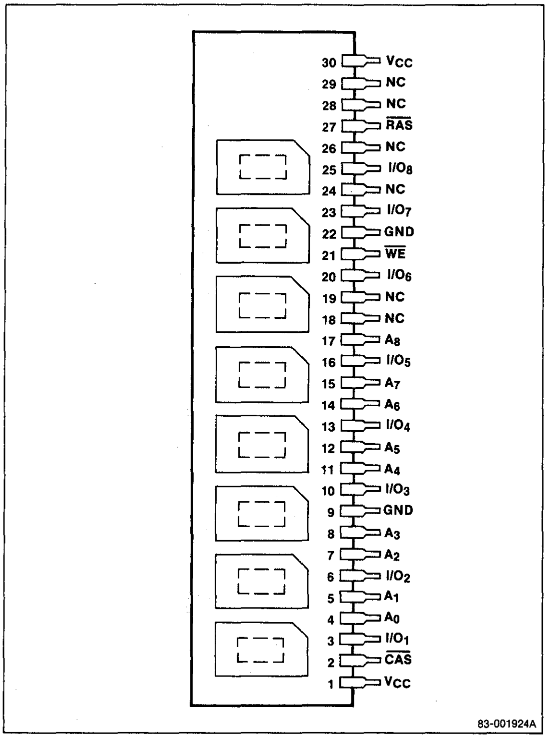
- ☐ 262,144-word by 8-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) packaging
- ☐ Eight 256K dynamic RAMs incorporated in high-density PLCC packaging
- ☐ Eight power supply decoupling capacitors included
- ☐ Low power dissipation: 220 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page-mode capability

Ordering Information

Part Number	Access Time (max)	Read/Write Cycle Time (min)	Page-Mode Cycle Time (min)	Package
MC-41256A8A-12	120 ns	220 ns	120 ns	30-pin leaded SIMM
A-15	150 ns	260 ns	145 ns	
MC-41256A8B-12	120 ns	220 ns	120 ns	30-pin socketable SIMM
B-15	150 ns	260 ns	145 ns	

Pin Configurations

30-Pin SIMM, MC-41256A8A



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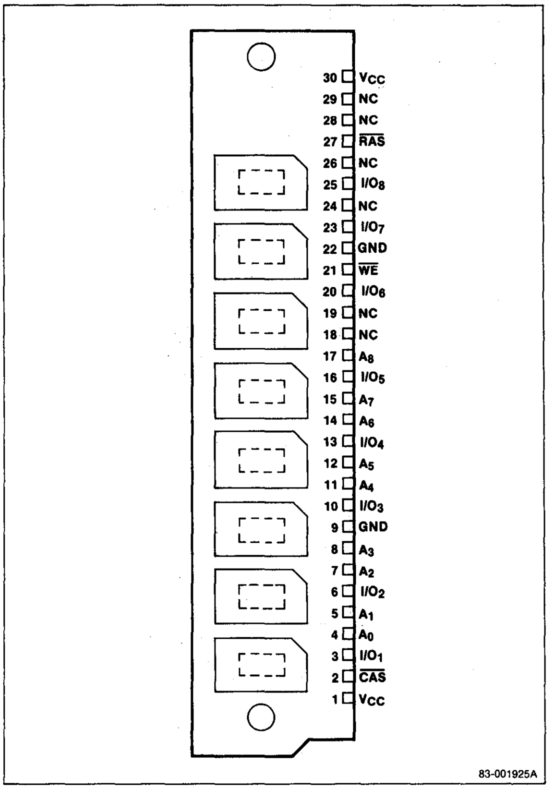
Pin Configurations (cont)

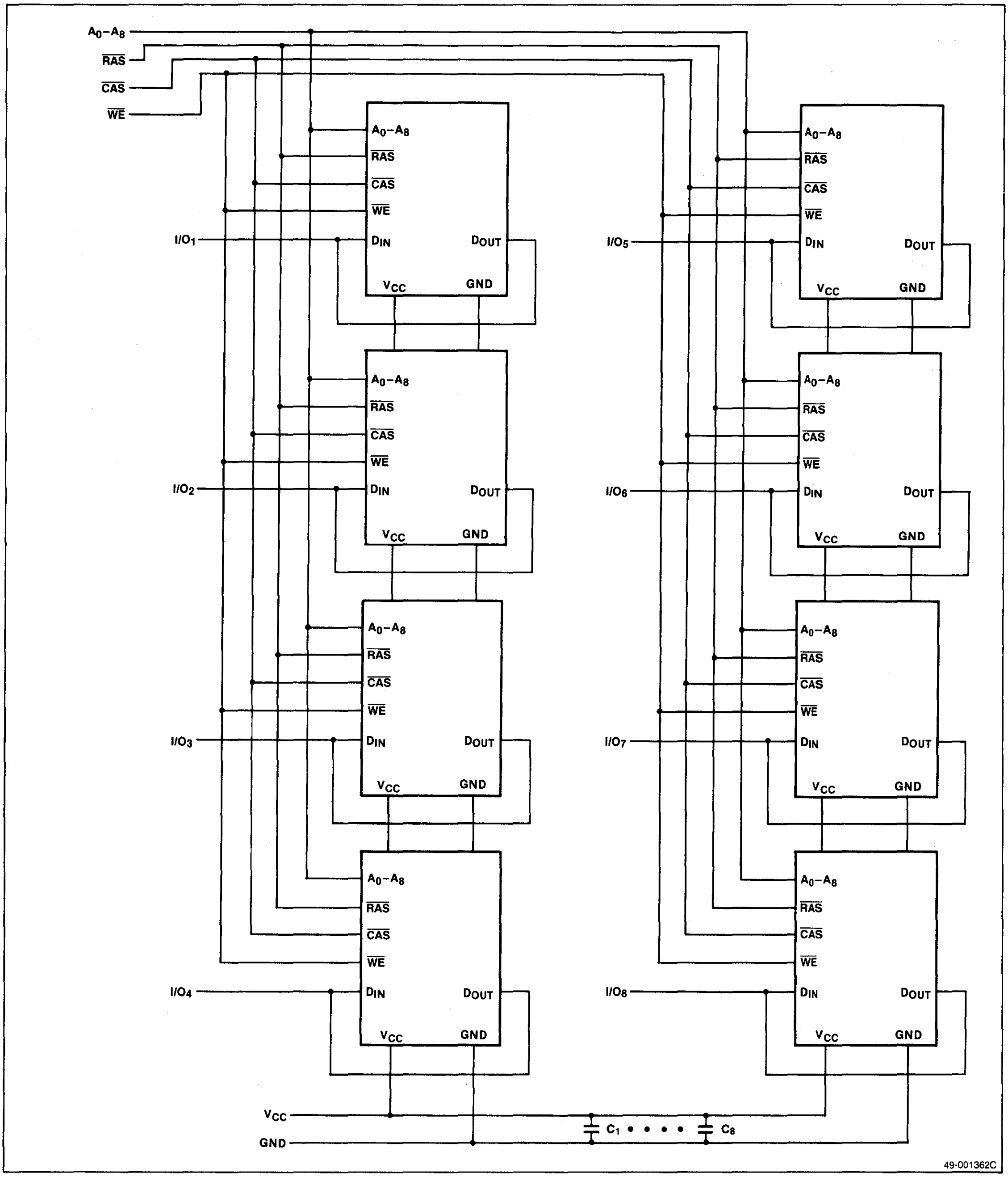
30-Pin SIMM, MC-41256A8B



Pin Identification

Symbol	Function
A_0-A_8	Address inputs
I/O_1-I/O_8	Common data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IA}			55	pF	A_0-A_8
	C_{IR}			70	pF	$\overline{RAS}$, $\overline{WE}$
	C_{IC}			70	pF	$\overline{CAS}$
Input/output capacitance	C_{DQ}			17	pF	For I/O_1-I/O_8: $\overline{CAS} = V_{IH}$ to disable D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} +1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			40.0	mA	$\overline{RAS} = V_{IH}$; D_{OUT} = high-Z
Input leakage current	I_{IL}	−80		80	μA	V_{IN} = 0 to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		Limits					
		MC-41256A8-12		MC-41256A8-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		560		480	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Refresh operating current, average	I_{CC3}		480		400	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Page-mode operating current, average	I_{CC4}		400		320	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min (Note 5)
$\overline{CAS}$ before $\overline{RAS}$ refresh operating current, average	I_{CC5}		480		400	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IL}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Page-mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

		Limits					
		MC-41256A8-12		MC-41256A8-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		ns	(Note 15)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	30		30		ns	(Note 15)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

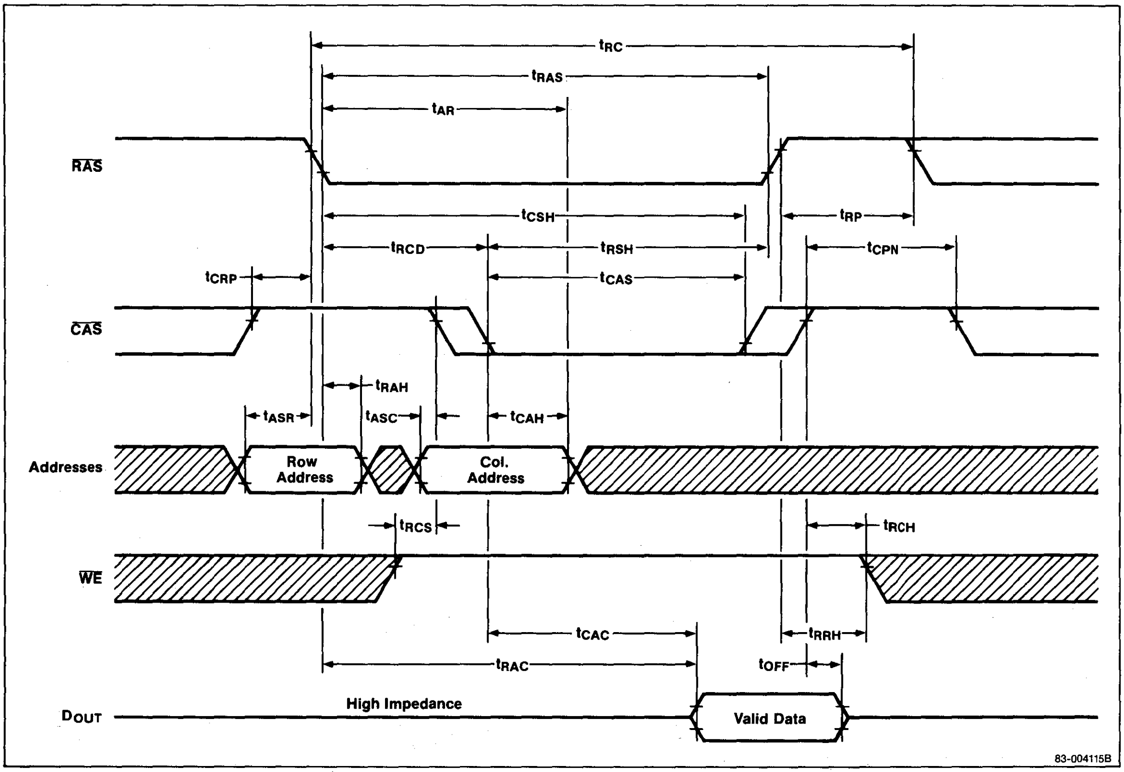
(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$.

(15) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

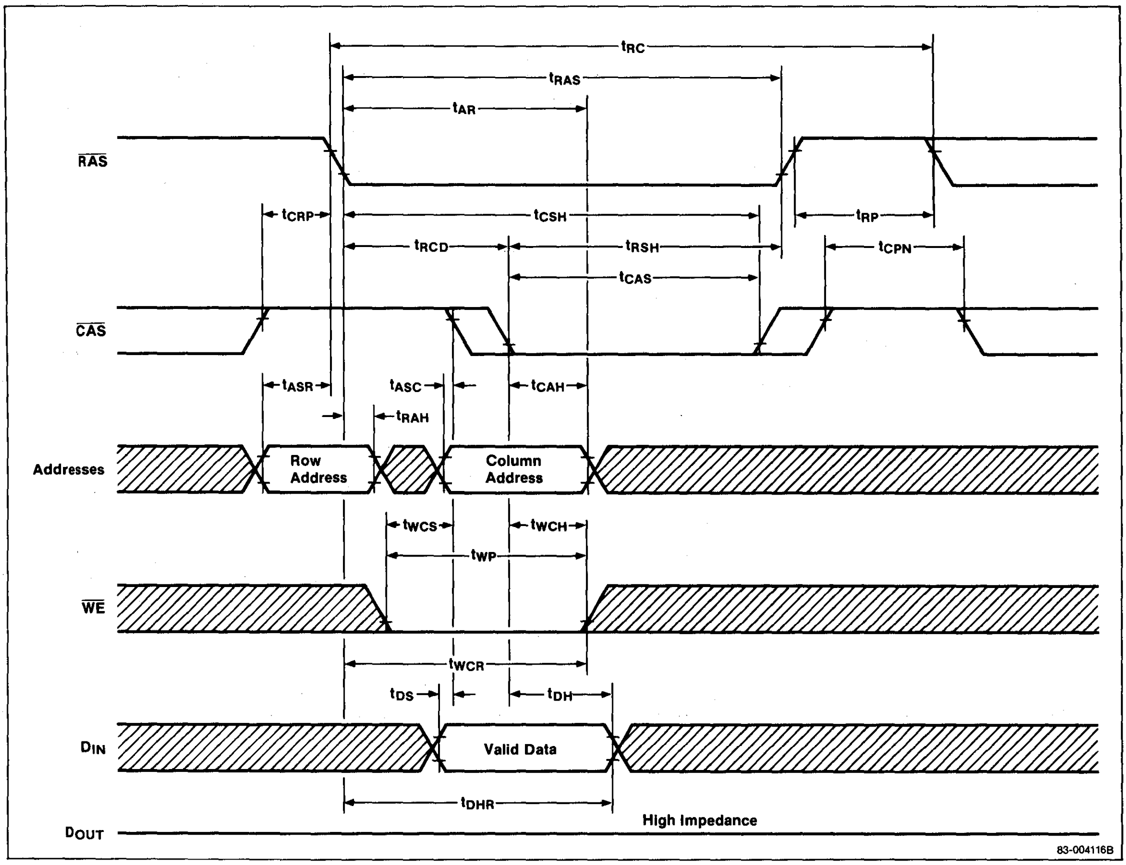
Timing Waveforms

Read Cycle



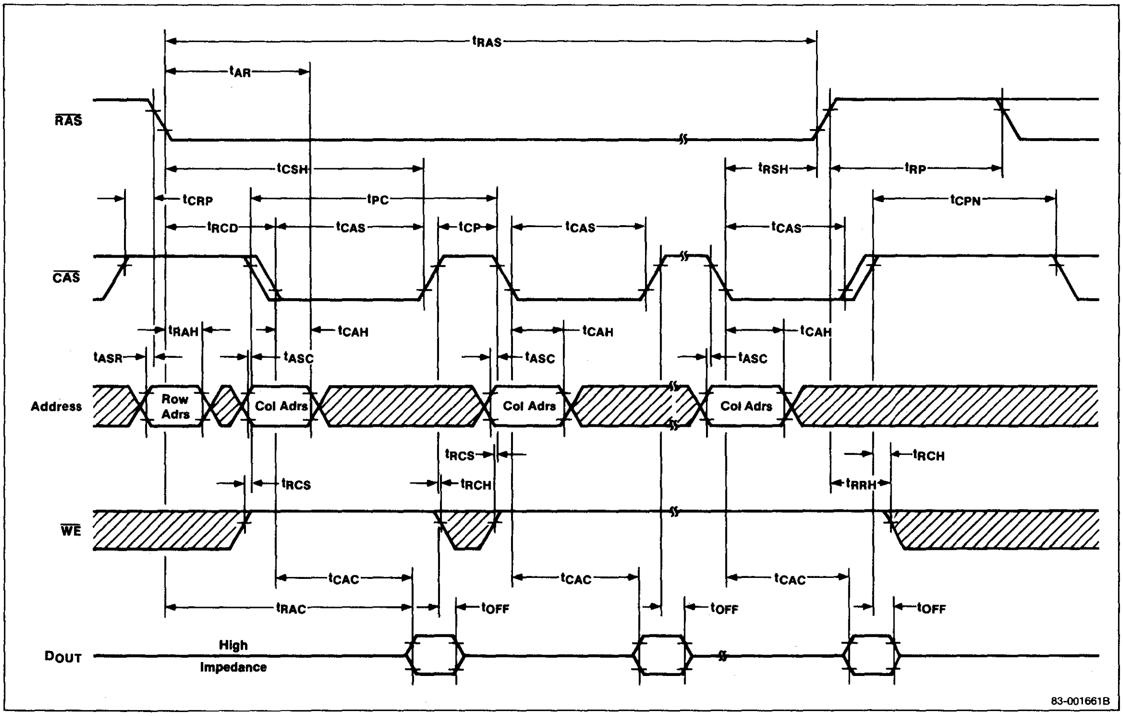
Timing Waveforms (cont)

Write Cycle (Early Write)



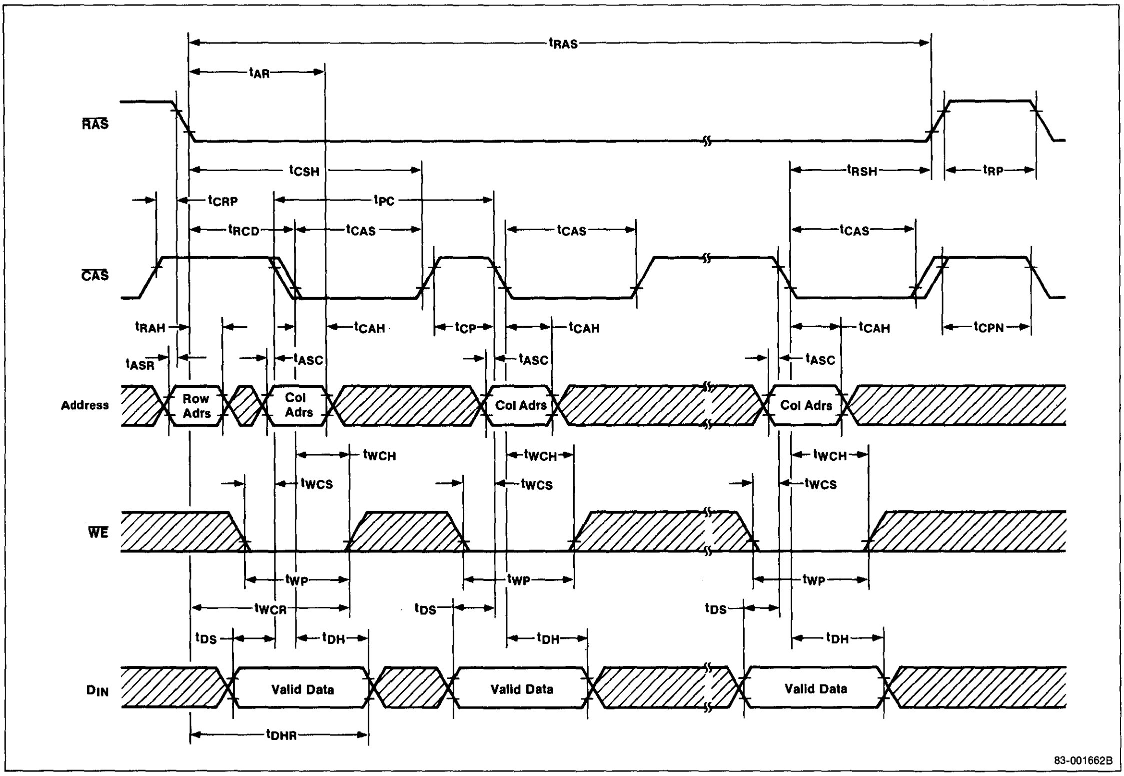
Timing Waveforms (cont)

Page Read Cycle



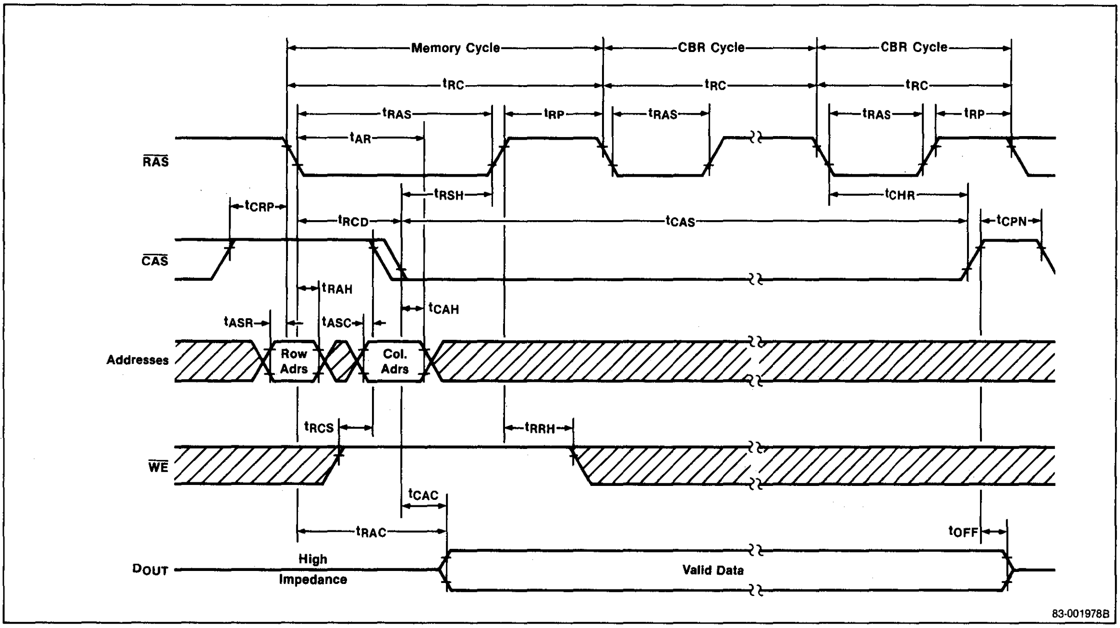
Timing Waveforms (cont)

Page Write Cycle (Early Write)

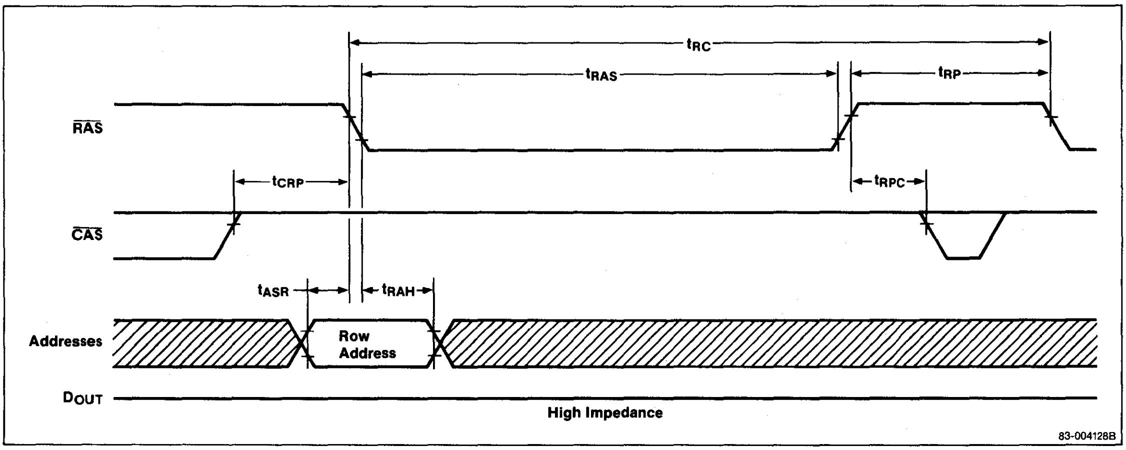


Timing Waveforms (cont)

Hidden Refresh Cycle

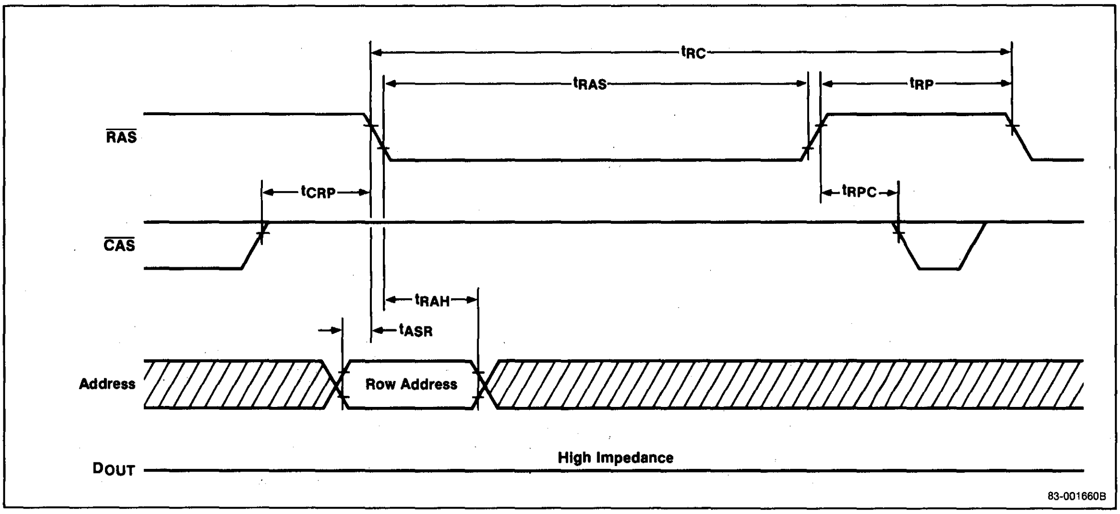


$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



NEC

NEC Electronics Inc.

MC-41256A9
262,144 x 9-BIT
DYNAMIC NMOS RAM MODULE

Description

The MC-41256A9 is a 262,144-word by 9-bit NMOS RAM module designed to operate from a single +5-volt power supply. Advanced dynamic circuitry, including a single-transistor storage cell, 1024 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-41256A9 is functionally equivalent to eight μPD41256 standard 256K DRAMs with a parity bit. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-41256A9 includes nine μPD41256s in PLCC packages and nine power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

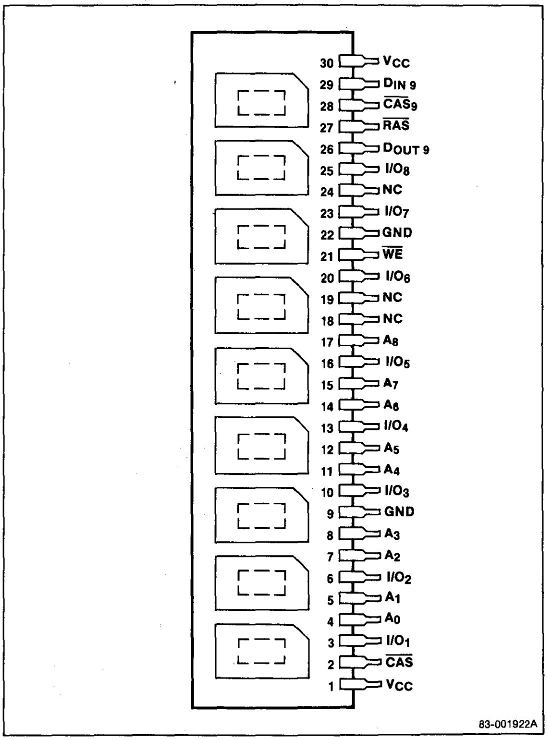
- ☐ 262,144-word by 9-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) packaging
- ☐ Nine 256K dynamic RAMs incorporated in high-density PLCC packaging
- ☐ Nine power supply decoupling capacitors included
- ☐ Low power dissipation: 248 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page-mode capability

Ordering Information

Part Number	Access Time (max)	Read/Write Cycle Time (min)	Page-Mode Cycle Time (min)	Package
MC-41256A9A-12	120 ns	220 ns	120 ns	30-pin leaded SIMM
A-15	150 ns	260 ns	145 ns	
MC-41256A9B-12	120 ns	220 ns	120 ns	30-pin socketable SIMM
B-15	150 ns	260 ns	145 ns	

Pin Configurations

30-Pin SIMM, MC-41256A9A



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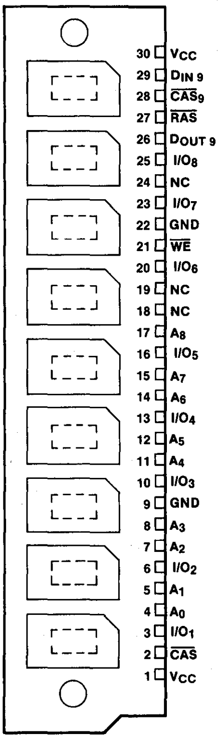
Pin Configurations (cont)

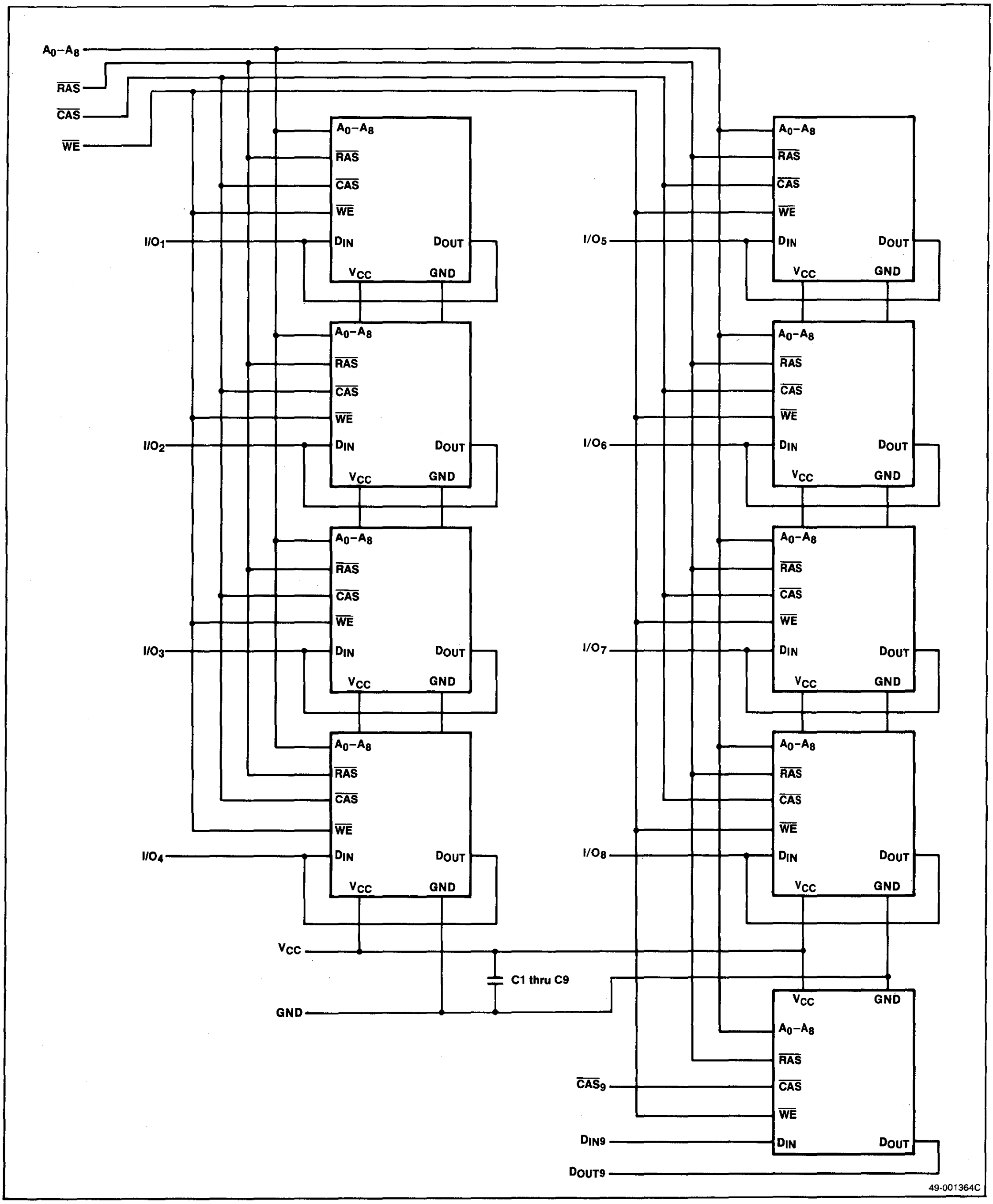
30-Pin SIMM, MC-41256A9B



Pin Identification

Symbol	Function
A_0-A_8	Address inputs
I/O_1-I/O_8	Common data inputs and outputs
$D_{IN\ 9}$	Data input 9
$D_{OUT\ 9}$	Data output 9
$\overline{CAS}$	Column address strobe
$\overline{CAS}_9$	Column address strobe for data output 9
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}, ambient	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_{IA}			60	pF	A_0-A_8
	C_{IR}			75	pF	$\overline{RAS}$, $\overline{WE}$
	C_{IC}			70	pF	$\overline{CAS}$
	$C_{IC\,9}$			13	pF	$\overline{CAS_9}$
	$C_{IN\,9}$			10	pF	$D_{IN\,9}$
Input/output capacitance	$C_{I/O}$			17	pF	For I/O_1-I/O_8: $\overline{CAS}$ = V_{IH} to disable D_{OUT}
Output capacitance	$C_{OUT\,9}$			12	pF	For $D_{OUT\,9}$: $\overline{CAS_9}$ = V_{IH} to disable $D_{OUT\,9}$

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} +1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			45.0	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high-Z
Input leakage current	I_{IL}	−90		90	μA	For A_0-A_8, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$: V_{IN} = 0 to V_{CC}; all other pins = 0 V
	$I_{IL\,9}$	−10		10	μA	For $\overline{CAS_9}$ and $D_{IN\,9}$: V_{IN} = 0 to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1-I/O_8: D_{OUT} disabled; V_{OUT} = 0 to V_{CC}
	$I_{OL\,9}$	−10		10	μA	For $D_{OUT\,9}$: $D_{OUT\,9}$ disabled, V_{OUT} = 0 to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		Limits					
		MC-41256A9-12		MC-41256A9-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		630		540	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min (Note 5)
Refresh operating current, average	I_{CC3}		540		450	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Page-mode operating current, average	I_{CC4}		450		360	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
$\overline{CAS}$ before $\overline{RAS}$ operating current, average	I_{CC5}		540		450	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IL}; t_{RC} = t_{RC} min (Note 5)
Random read or write cycle time	t_{RC}	220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		ns	(Notes 6, 17)
Page-mode cycle time	t_{PC}	120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	30	0	35	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	25		25		ns	
$\overline{CAS}$ precharge time (page mode)	t_{CP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	15		15		ns	
Column address setup time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		Limits					
		MC-41256A9-12		MC-41256A9-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		ns	
Write command pulse width	t_{WP}	20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 15, 17)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		ns	(Note 15, 17)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		ns	(Note 15, 17)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		ns	(Note 16)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	30		30		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values were obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

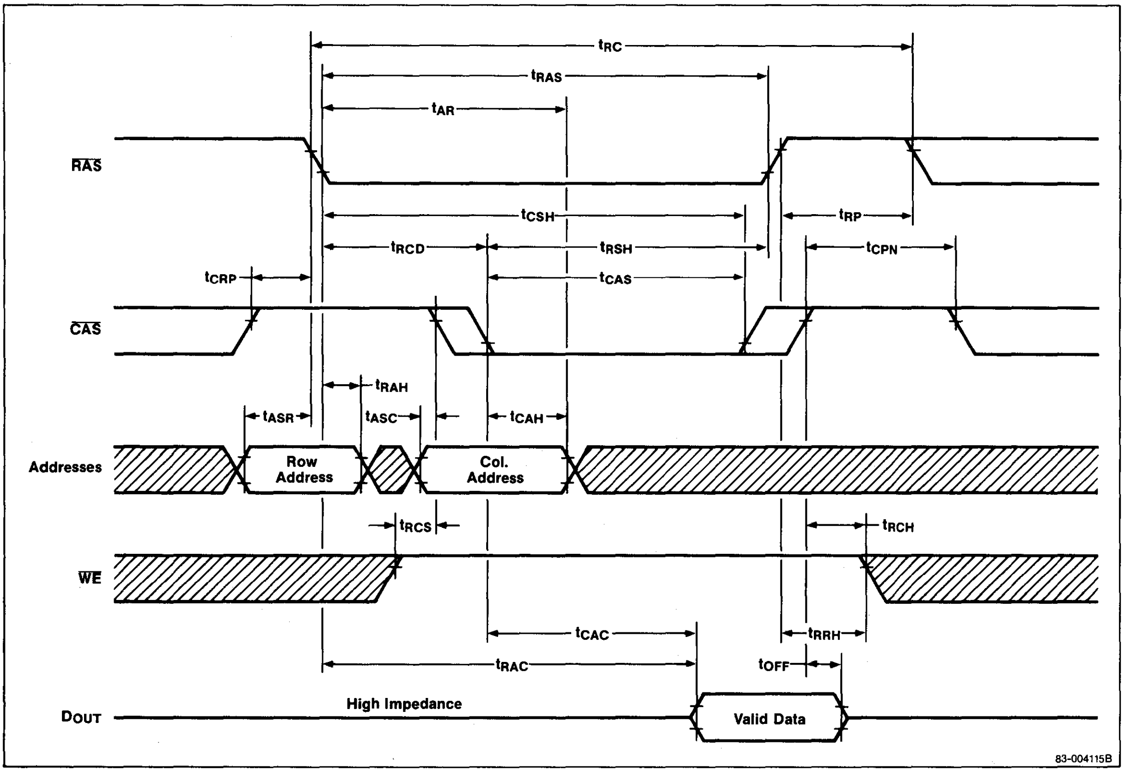
(15) For $D_{OUT\ 9}$, t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\ 9}$ (at access time and until $\overline{CAS}_9$ returns to V_{IH}) is indeterminate.

(16) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

(17) Read-write/read-modify-write operation can be performed only by the PLCC controlled by $\overline{CAS}_9$ because of its separate data input and output pins.

Timing Waveforms

Read Cycle



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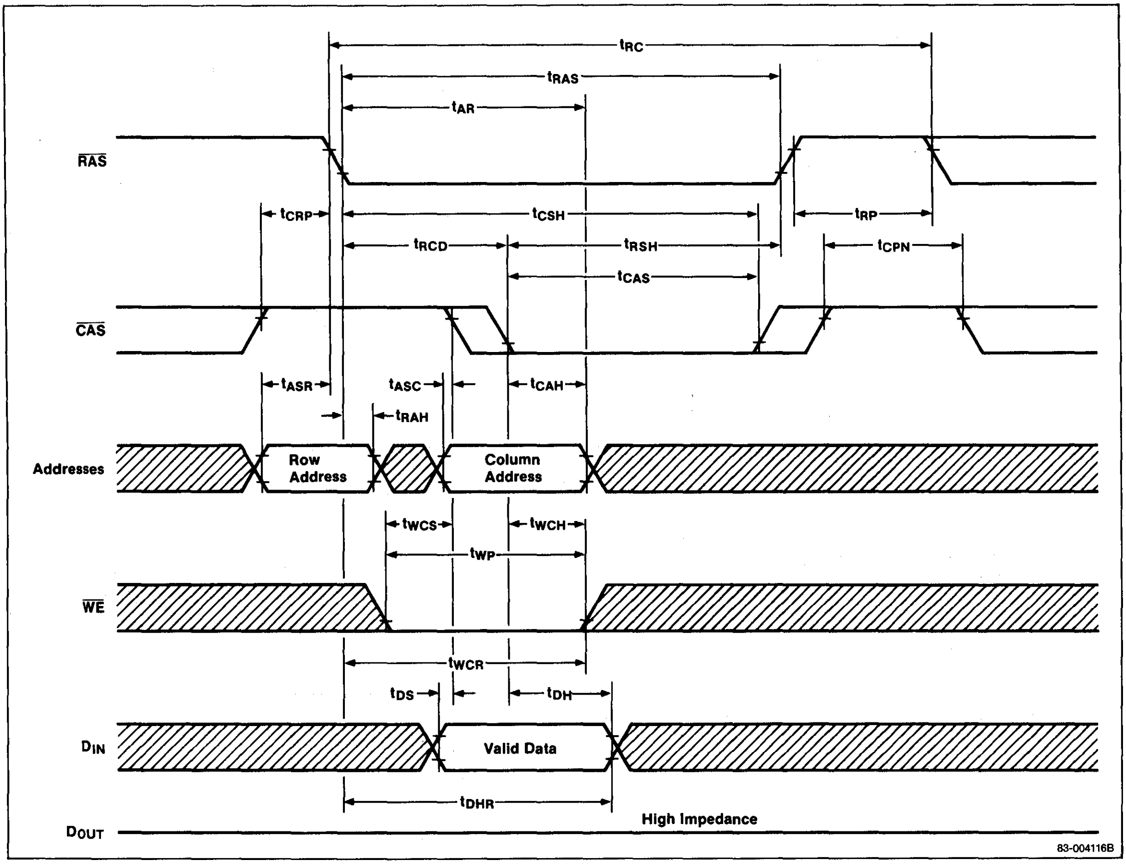
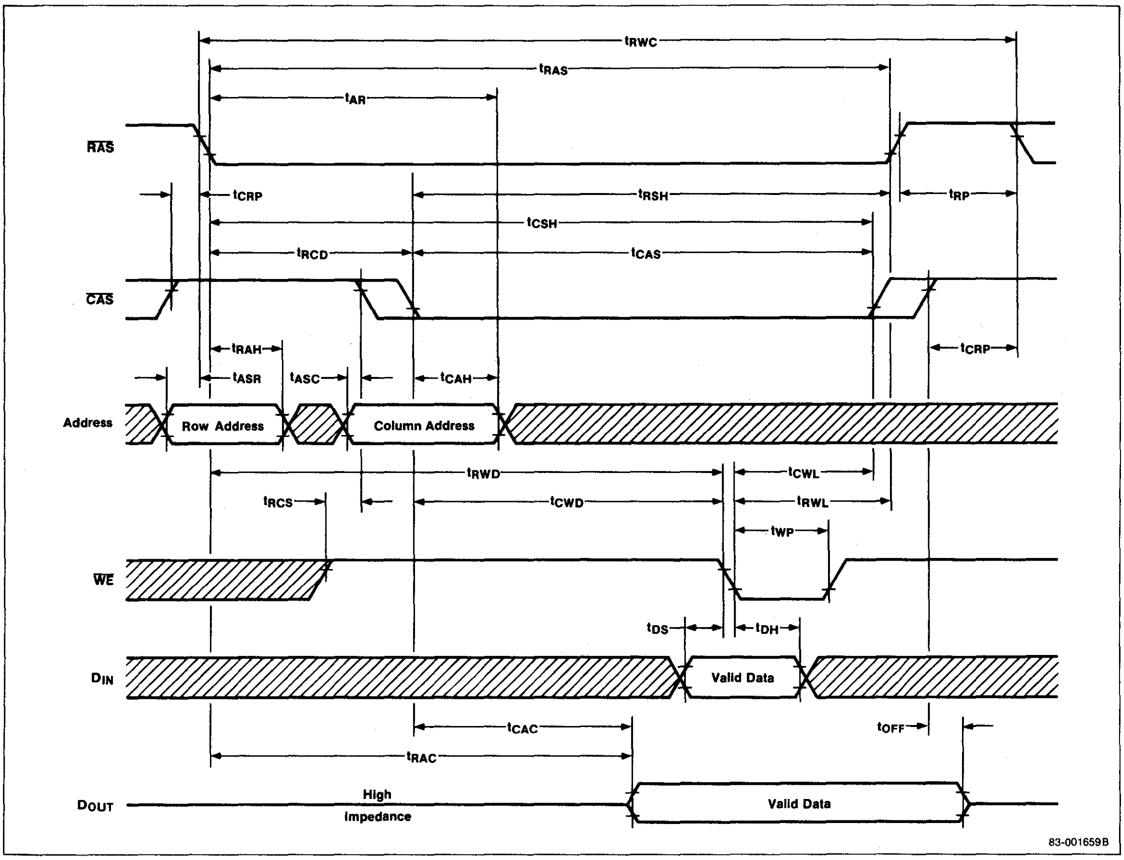
Timing Waveforms (cont)

Write Cycle (Early Write)



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT} 9 only)



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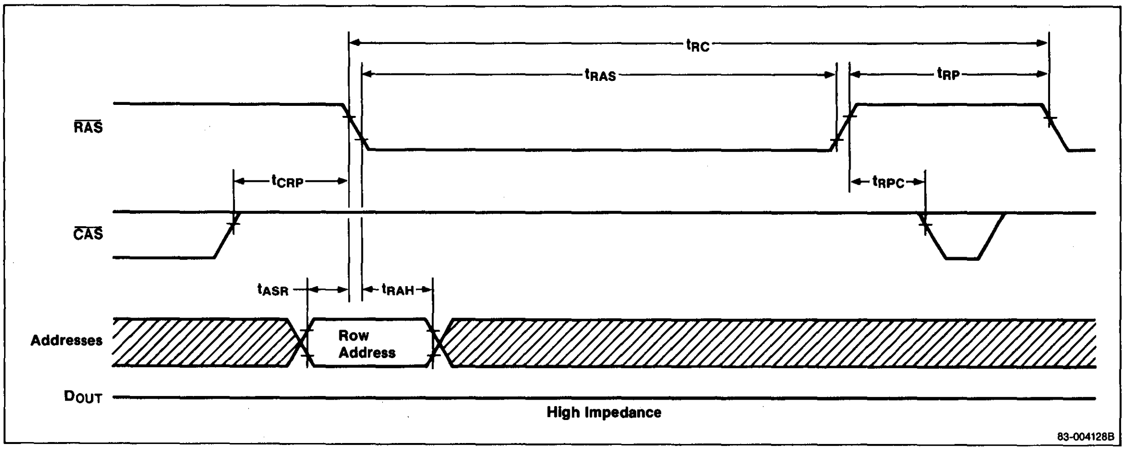
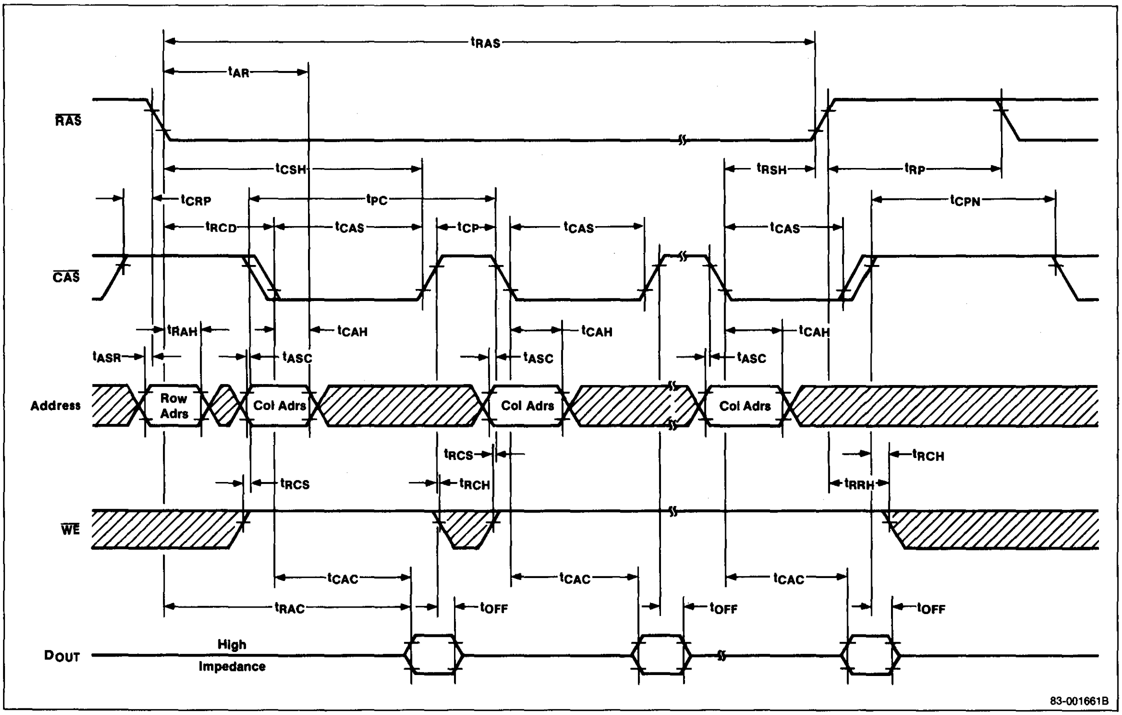
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle

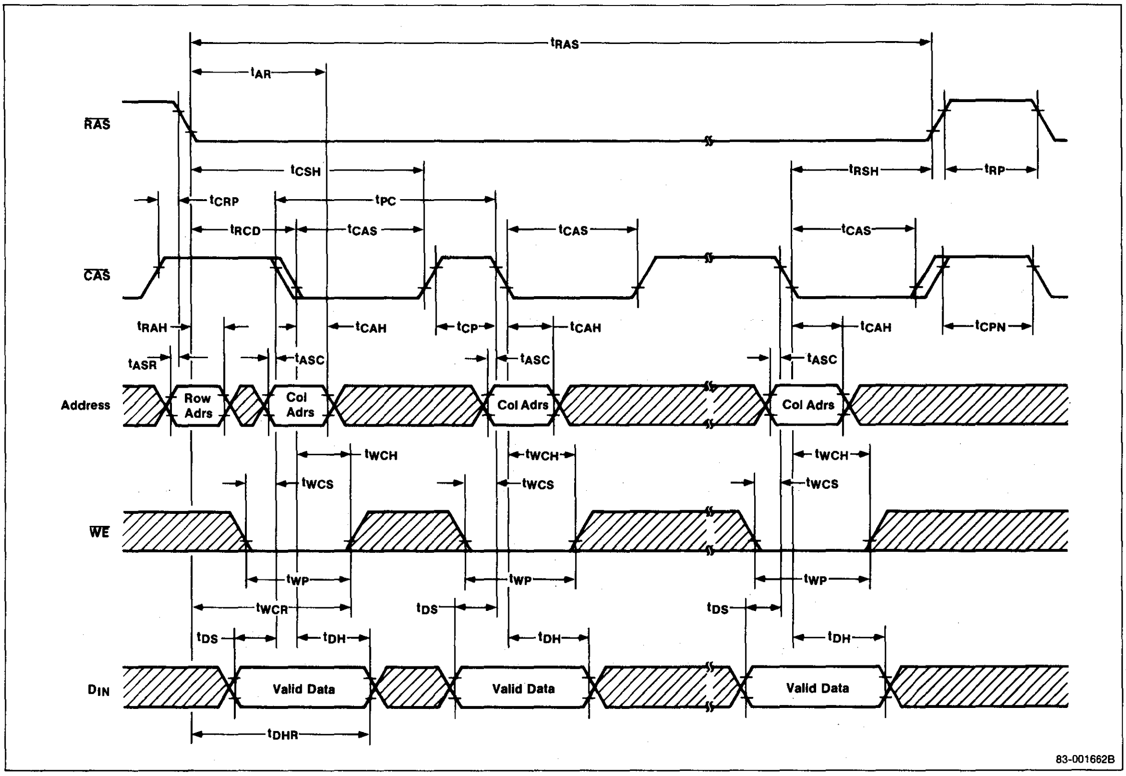


Page Read Cycle



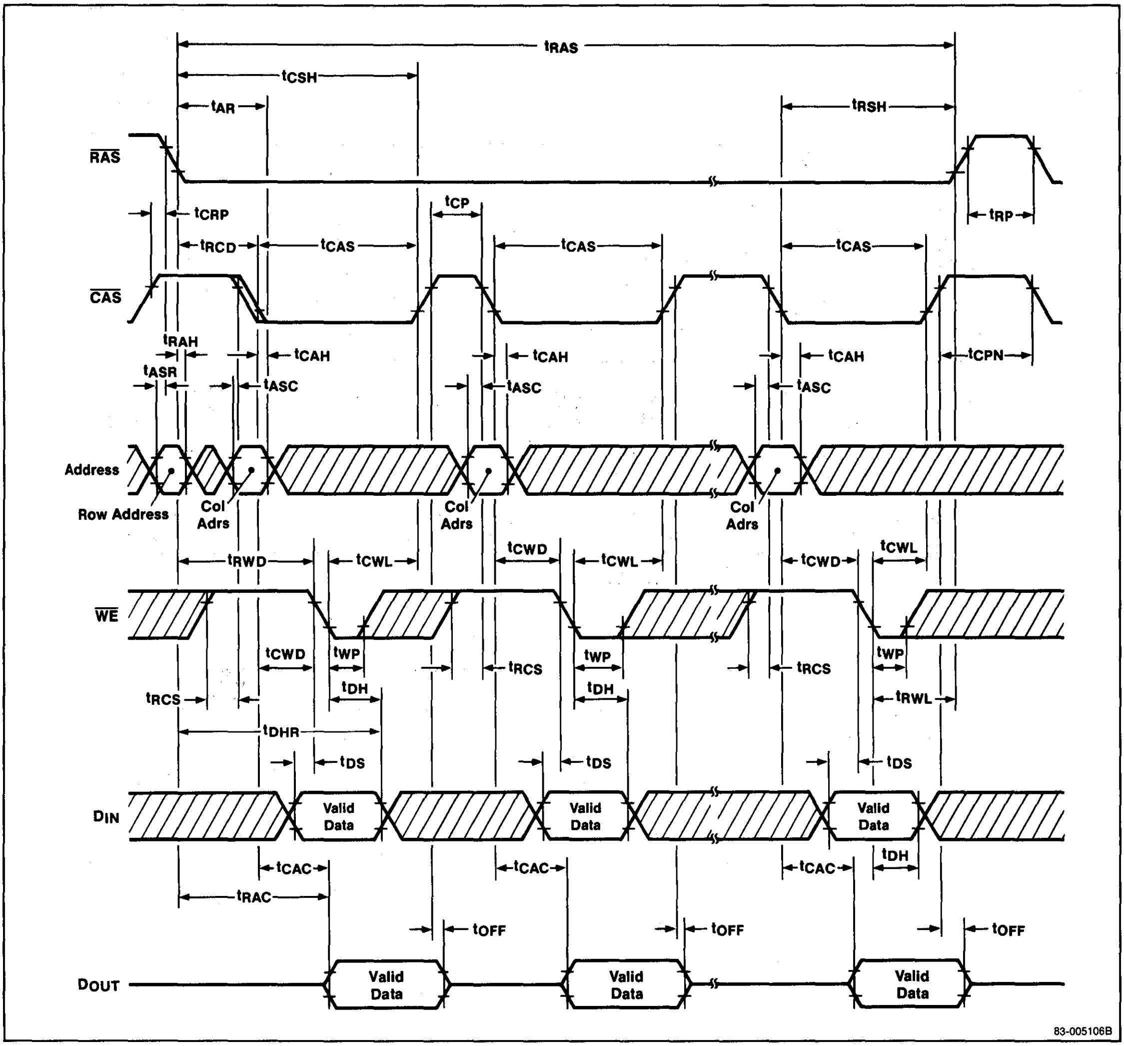
Timing Waveforms (cont)

Page Write Cycle (Early Write)



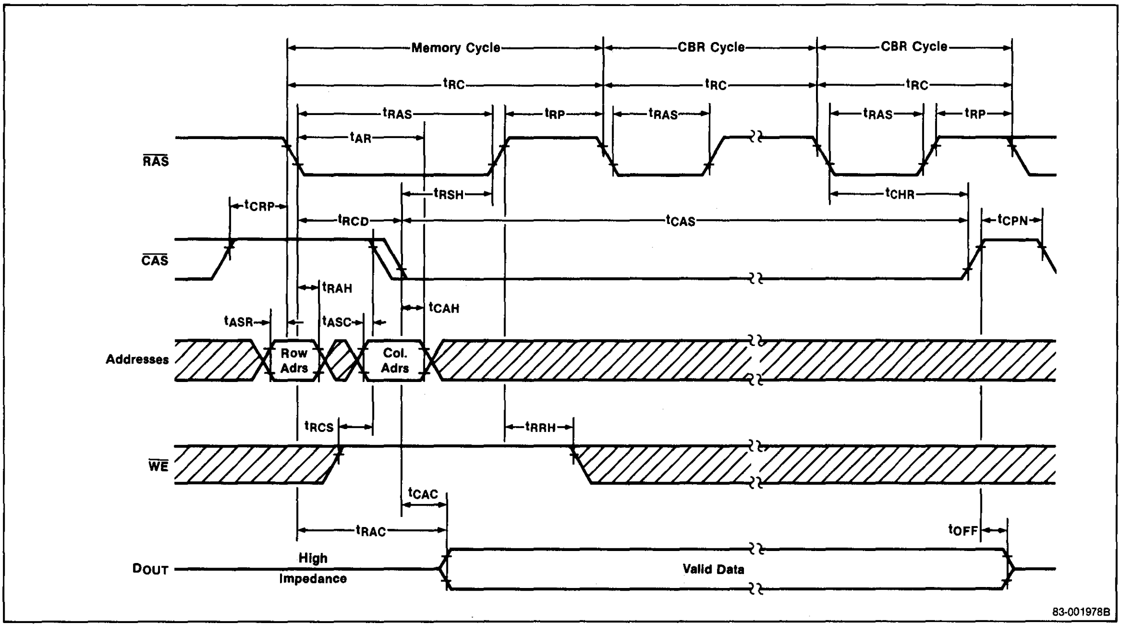
Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle (D_{OUT9} only)

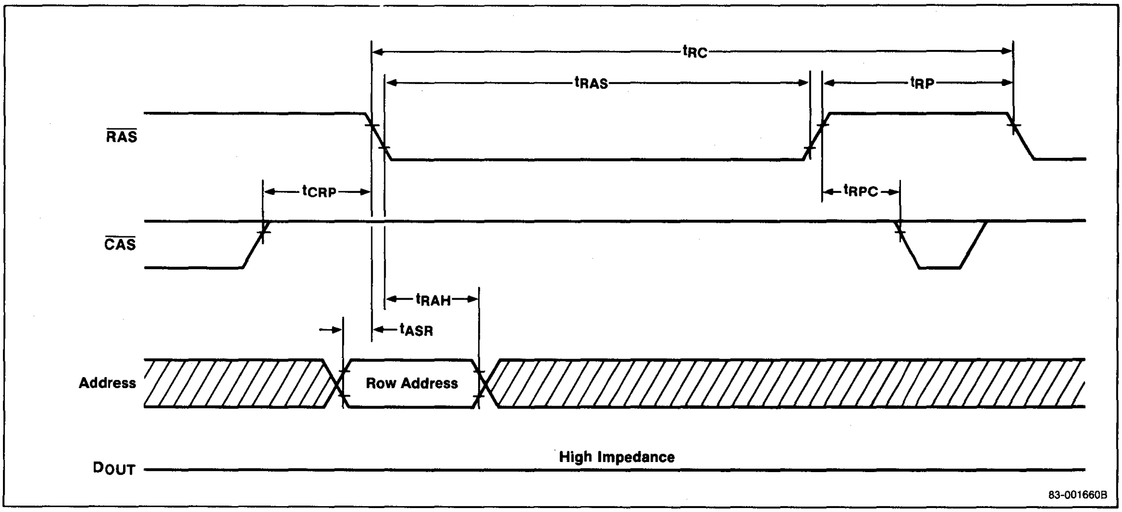


Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



4

NEC
NEC Electronics Inc.

MC-421000A8
1,048,576 x 8-BIT
CMOS DYNAMIC RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-421000A8 is a fast-page 1,048,576-word by 8-bit CMOS dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000A8 is functionally equivalent to eight μPD421000 standard 1M DRAMs. Refreshing is accomplished by means of $\overline{\text{RAS}}$-only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-421000A8 includes eight μPD421000s in SOJ packages and eight power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

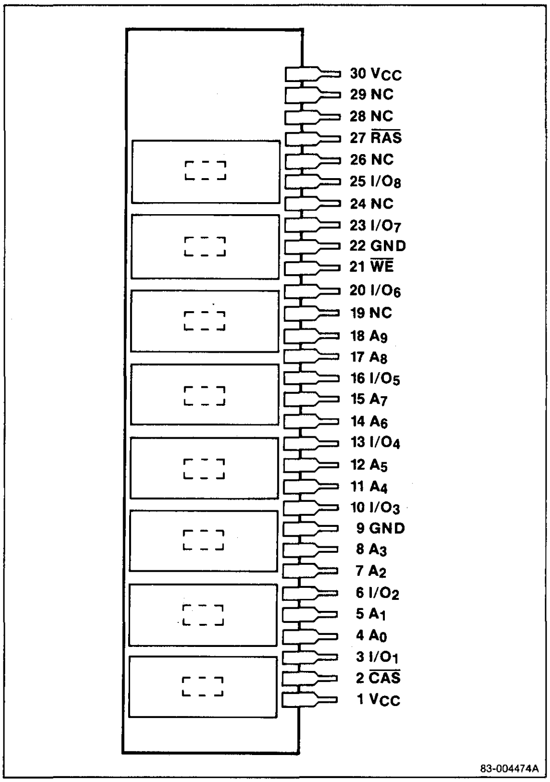
- ☐ 1,048,576-word by 8-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) packaging
- ☐ Eight 1M dynamic RAMs incorporated in high-density SOJ packaging (μPD421000LA)
- ☐ Eight power supply decoupling capacitors
- ☐ Low power dissipation: 44 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Fast-page capability

Ordering Information

Part Number	Row Access Time (max)	Column Access Time (max)	Address Access Time (max)	Package
MC-421000A8A-80	80 ns	20 ns	45 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	55 ns	
A-12	120 ns	30 ns	65 ns	
MC-421000A8B-80	80 ns	20 ns	45 ns	30-pin socket-able SIMM
B-10	100 ns	25 ns	55 ns	
B-12	120 ns	30 ns	65 ns	

Pin Configurations

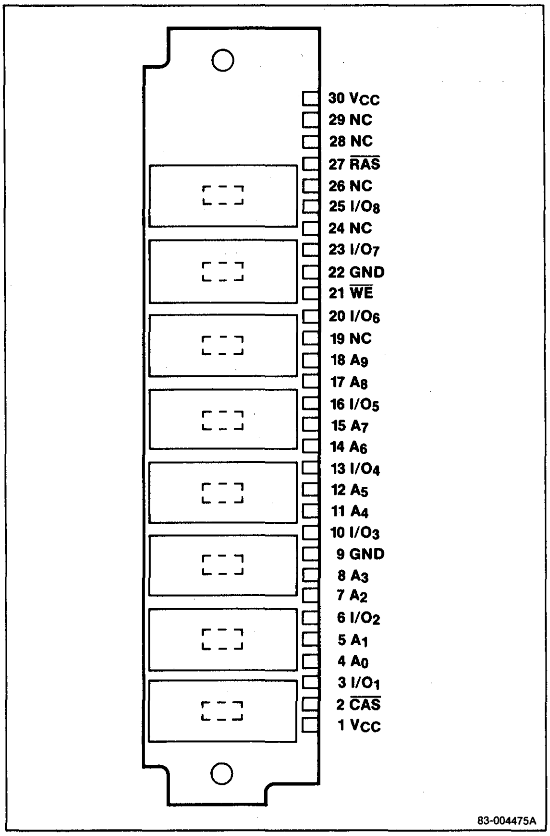
30-Pin SIMM, MC-421000A8A



NEC

Pin Configurations (cont)

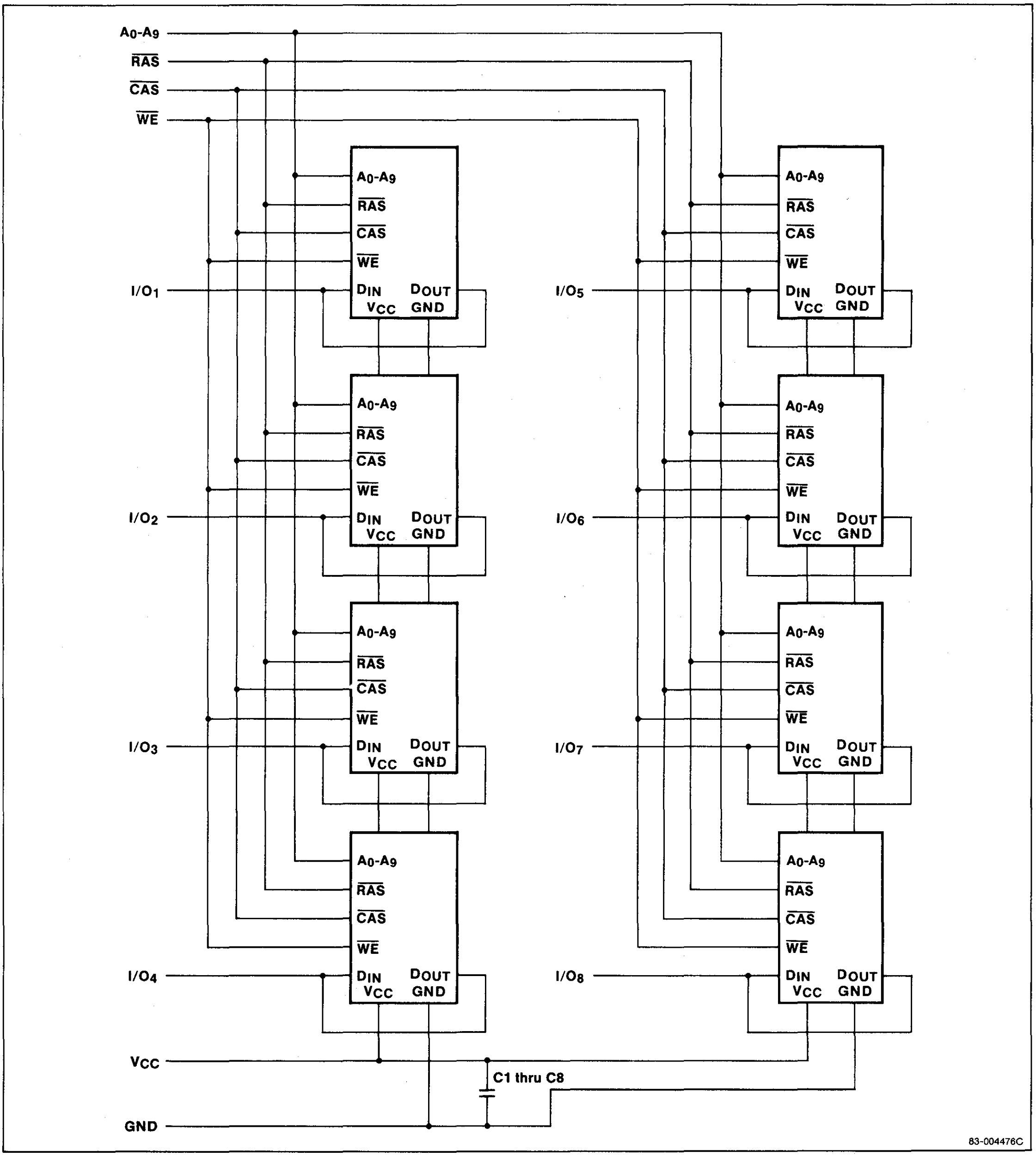
30-Pin SIMM, MC-421000A8B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



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Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		$V_{CC} + 1.0$	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			24	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min)
				8	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Input leakage current	I_{IL}	−80		80	μA	For A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: $V_{IN} = 0$ to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1-I/O_8: D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V $\pm 10\%$

		Limits							
		MC-421000A8-80		MC-421000A8-10		MC-421000A8-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		560		480		400	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Refresh operating current, average	I_{CC3}		560		480		400	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Fast-page operating current, average	I_{CC4}		480		400		320	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $I_O = 0$ mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		560		480		400	mA	$t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10, 11)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		65	ns	(Notes 7, 11)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 12)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ precharge time (non-page cycle)	t_{CPN}	10		10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	10	25	15	30	ns	(Note 11)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	(Note 11)
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	MC-421000A8-80 Min	MC-421000A8-80 Max	MC-421000A8-10 Min	MC-421000A8-10 Max	MC-421000A8-12 Min	MC-421000A8-12 Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		55		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 18)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 18)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

Notes [cont]:

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

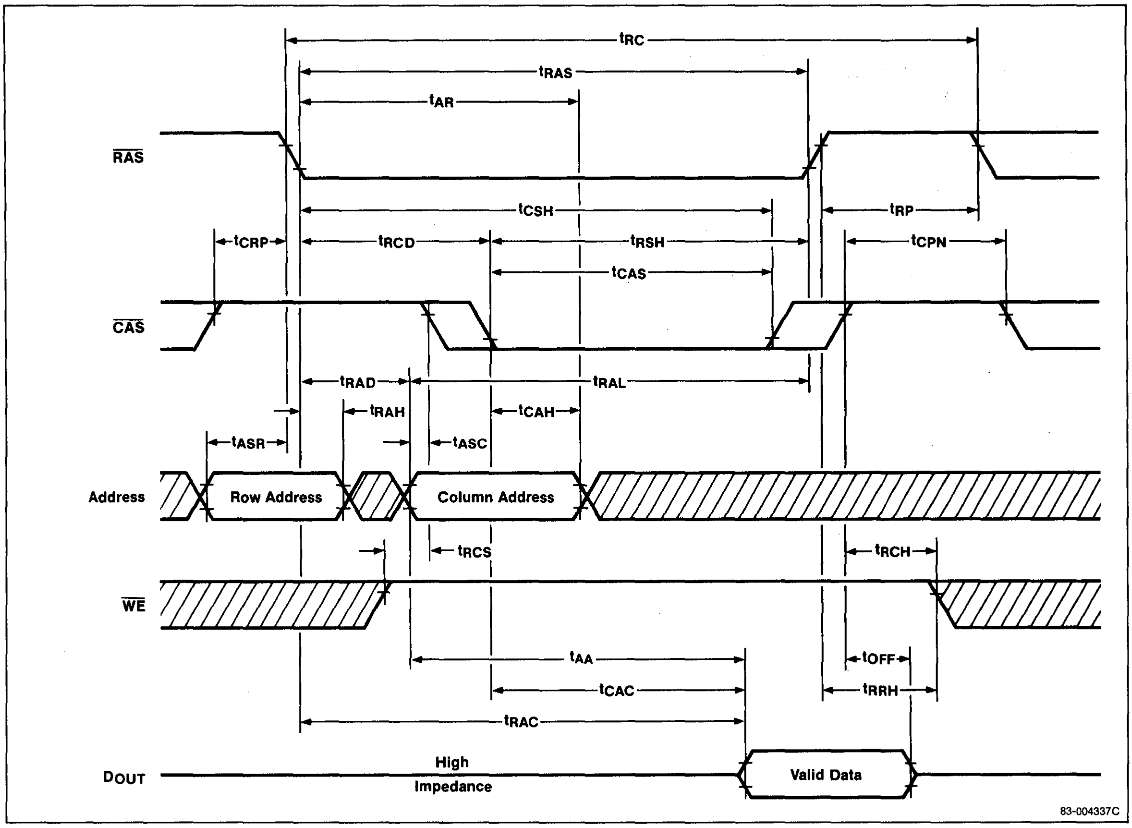
(16) For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(18) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

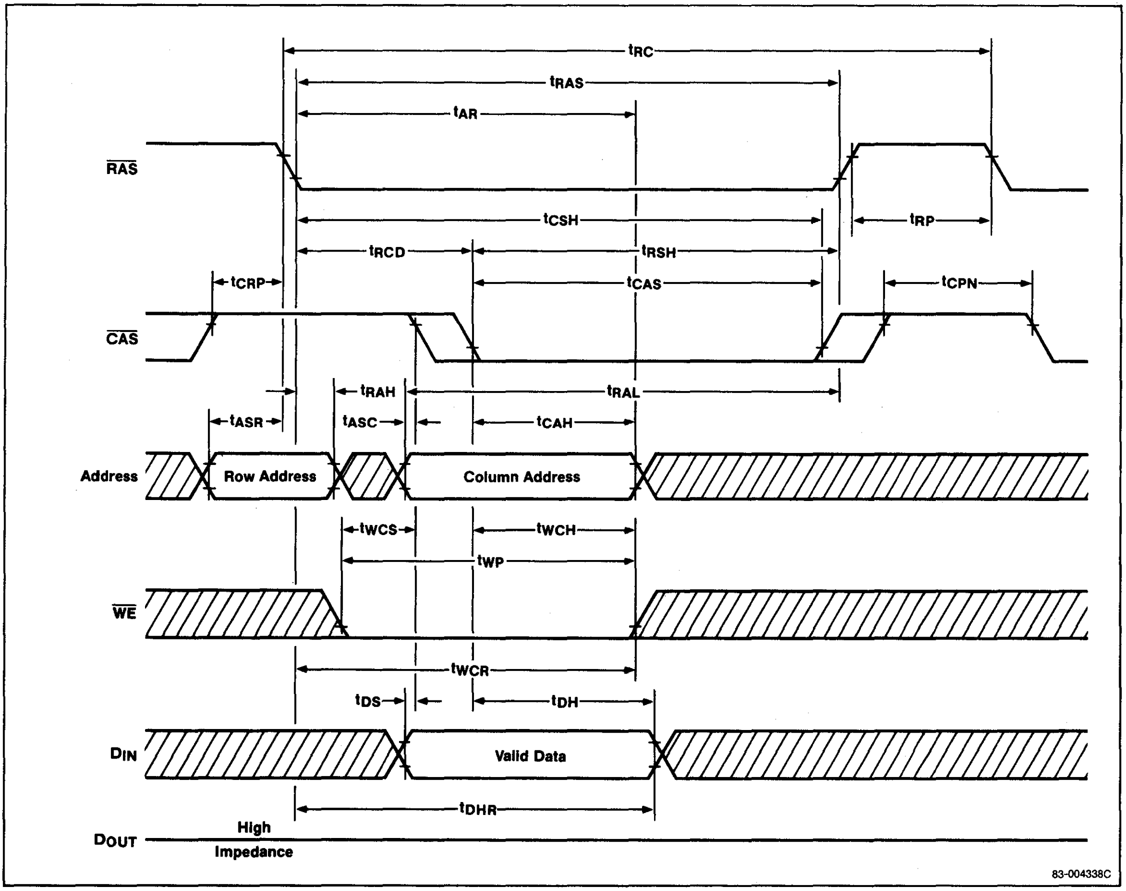
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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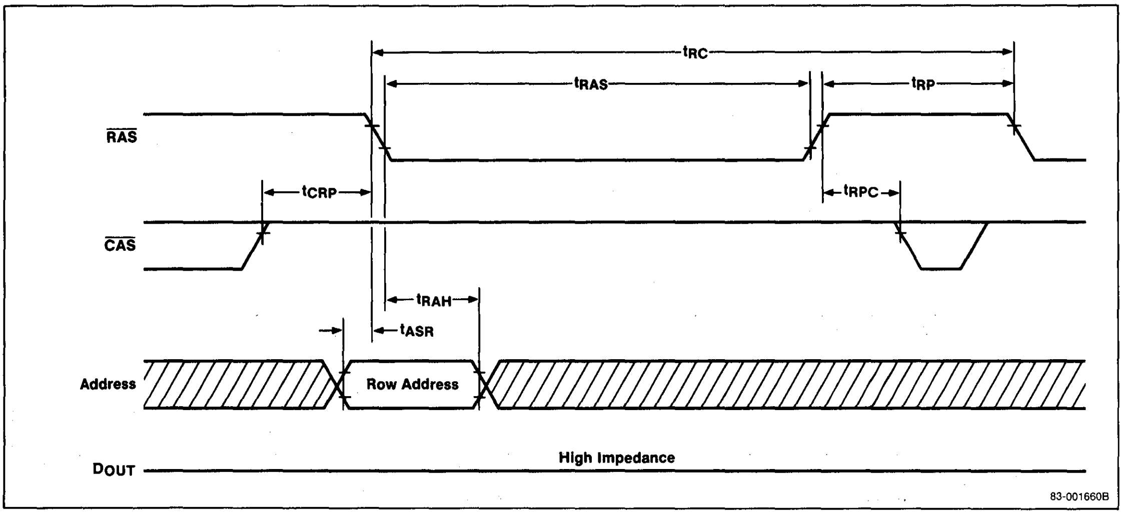
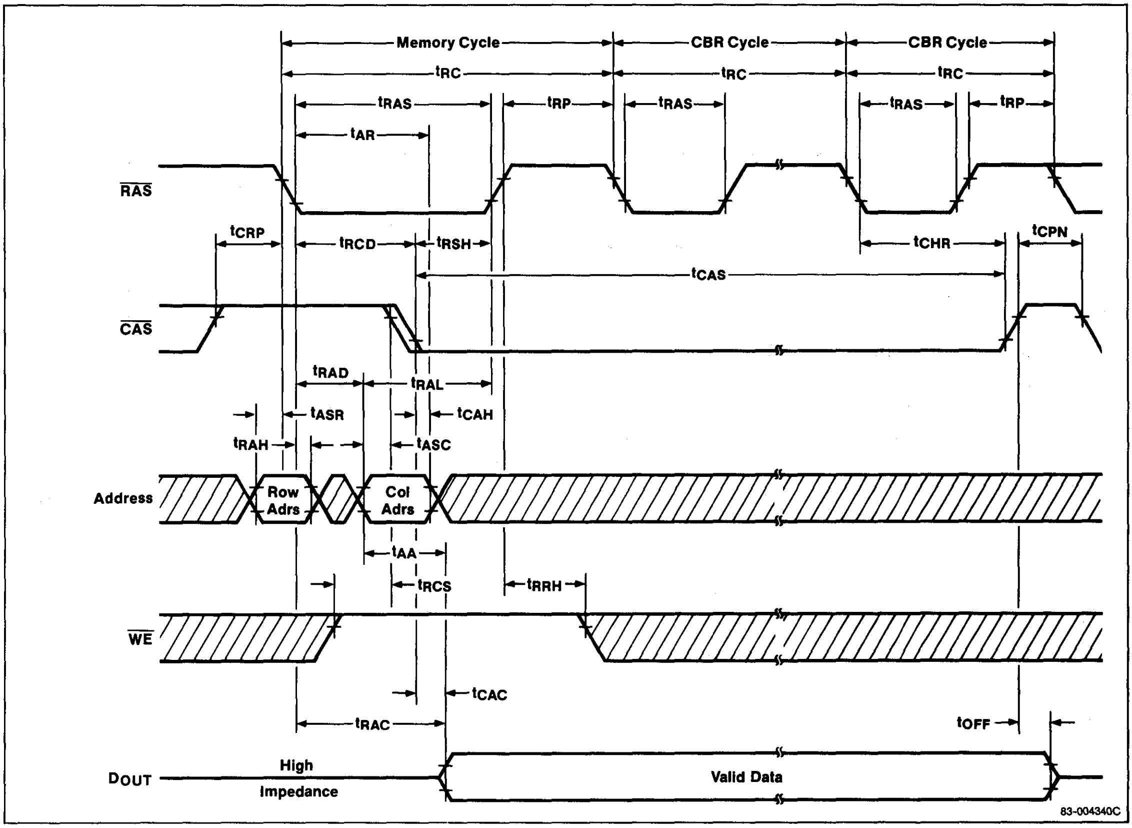
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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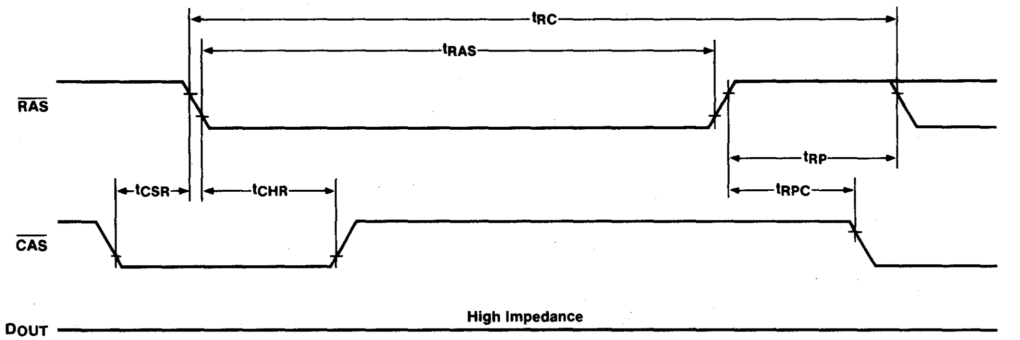
Timing Waveforms (cont)

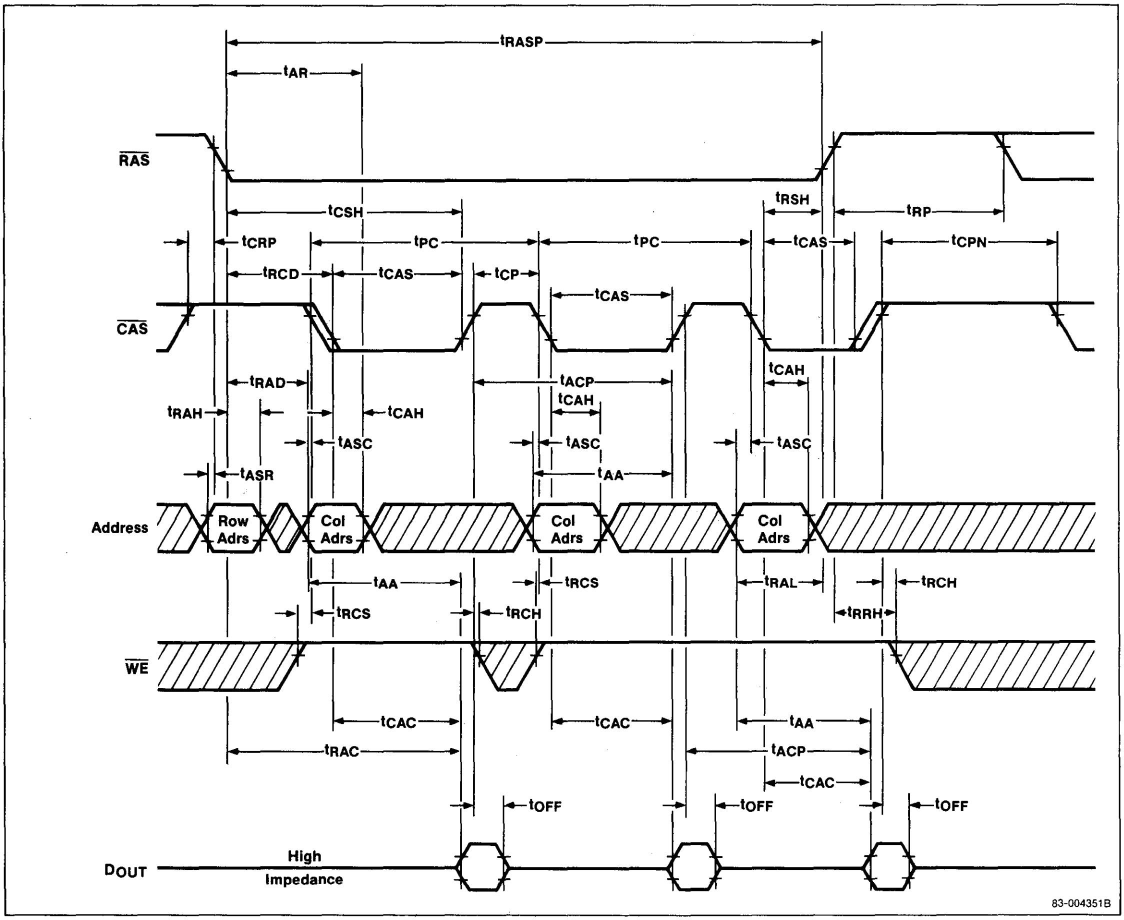
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

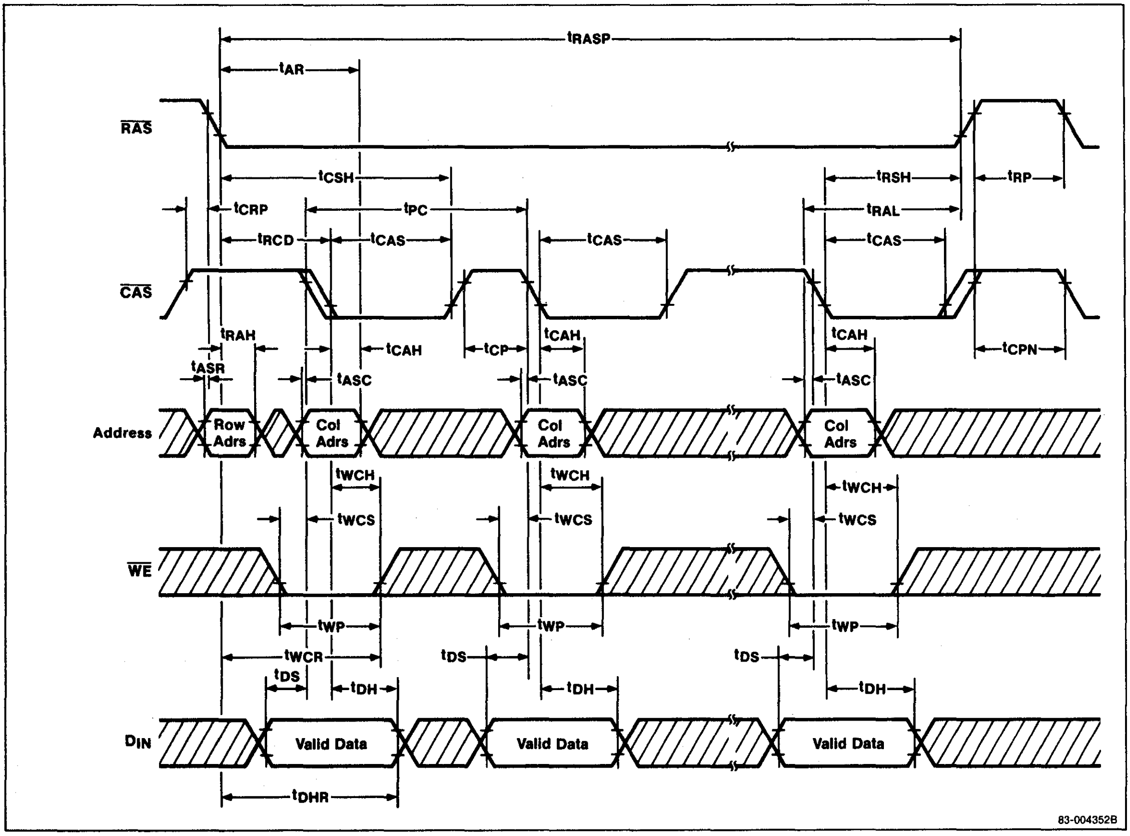
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Write Cycle (Early Write)



NEC

NEC Electronics Inc.

MC-421000A9
1,048,576 x 9-BIT
CMOS DYNAMIC RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-421000A9 is a fast-page, 1,048,576-word by 9-bit CMOS dynamic RAM module, designed to operate from a single +5 volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000A9 is functionally equivalent to eight μPD421000 standard 1M DRAMs plus a parity bit. Refreshing is accomplished by performing $\overline{\text{RAS}}$-only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes nine μPD421000s in SOJ packages and nine power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

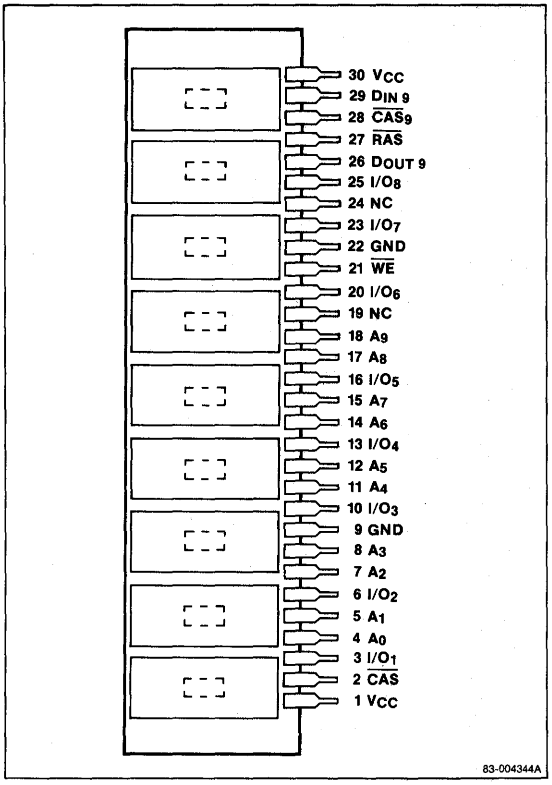
- ☐ 1,048,576-word by 9-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) packaging
- ☐ Incorporates nine 1M dynamic RAMs in high-density SOJ packaging (μPD421000LA)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 49.5 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Fast-page capability

Ordering Information

Part Number	Row Access Time (max)	Column Access Time (max)	Address Access Time (max)	Package
MC-421000A9A-80	80 ns	20 ns	45 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	55 ns	
A-12	120 ns	30 ns	65 ns	
MC-421000A9B-80	80 ns	20 ns	45 ns	30-pin socket-able SIMM
B-10	100 ns	25 ns	55 ns	
B-12	120 ns	30 ns	65 ns	

Pin Configurations

30-Pin SIMM, MC-421000A9A



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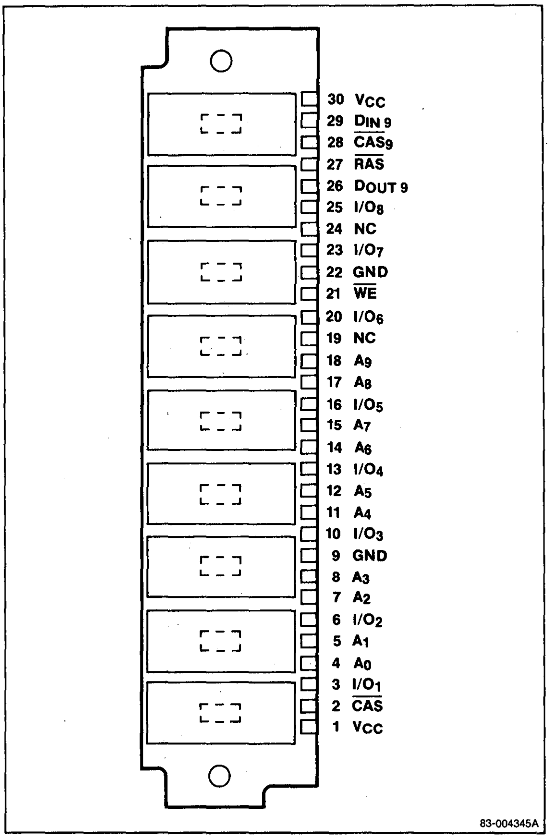
Pin Configurations (cont)

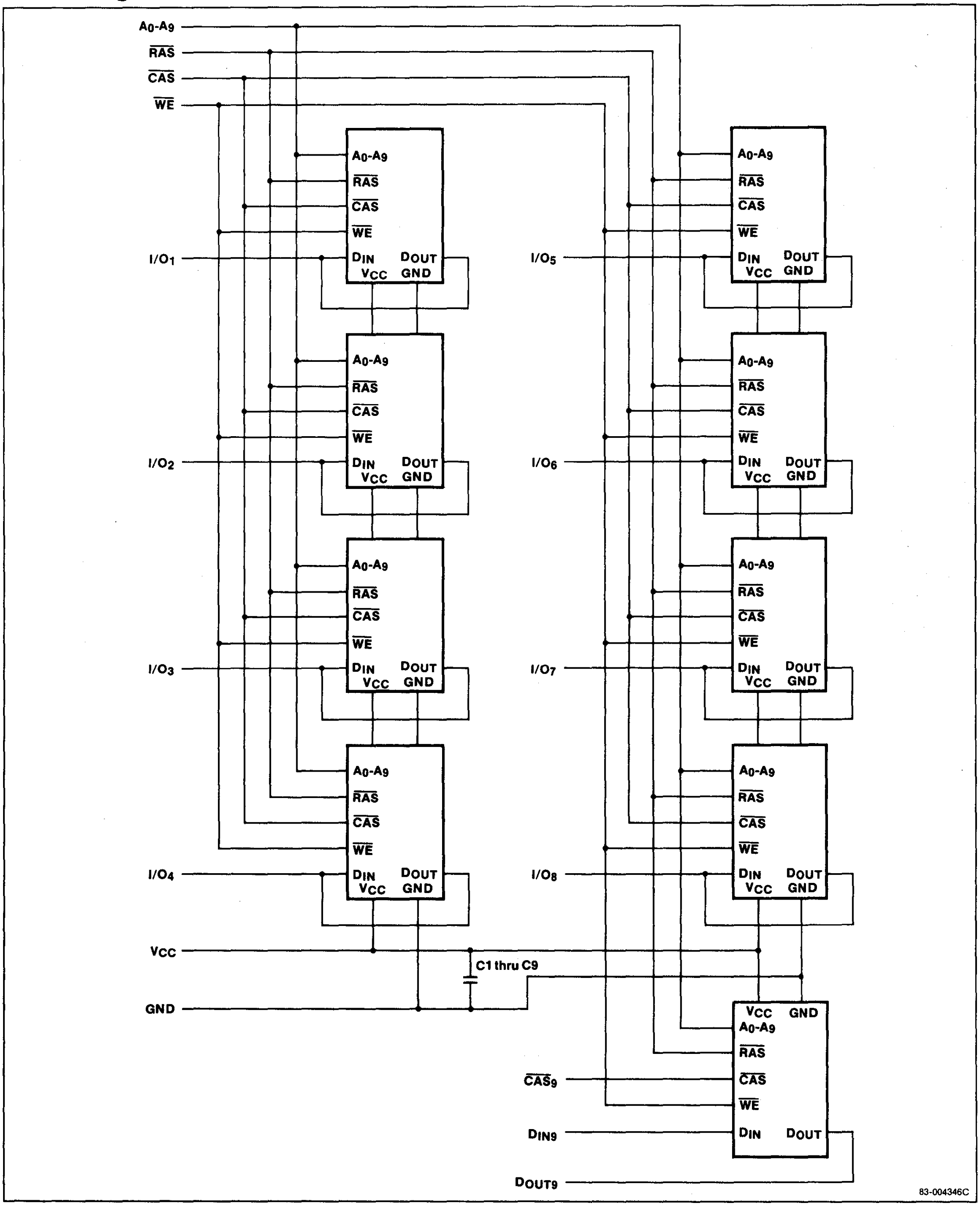
30-Pin SIMM, MC-421000A9B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$D_{IN\,9}$	Data input 9
$D_{OUT\,9}$	Data output 9
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{CAS_9}$	Column address strobe for data output 9
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
	C_{I2}	7	pF	$\overline{CAS}_9$, D_{IN9}
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8
Output capacitance	C_O	10	pF	$D_{OUT\,9}$

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5$ V ±10%; GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		$V_{CC} + 1.0$	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			27	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$
				9	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Input leakage current	I_{IL}	−90		90	µA	For A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: $V_{IN} = 0$ to 5.5 V; other pins = 0 V
Input leakage current	I_{IL9}	−10		10	µA	For $\overline{CAS}_9$, $D_{IN\,9}$; $V_{IN} = 0$ to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	µA	For I/O_1-I/O_8 and $D_{OUT\,9}$: D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000A9-80		MC-421000A9-10		MC-421000A9-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating current, average	I_{CC1}		630		540		450	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		630		540		450	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$, $t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Fast-page operating current, average	I_{CC4}		540		450		360	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; $I_O = 0$ mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		630		540		450	mA	$t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Notes 6, 20)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10, 11)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		65	ns	(Notes 7, 11)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 12)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	10		10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	10	25	15	30	ns	(Note 11)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	(Note 11)
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000A9-80		MC-421000A9-10		MC-421000A9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		55		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 18)
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20		25		30		ns	(Notes 18, 20)
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80		100		120		ns	(Notes 18, 20)
Column address to $\overline{WE}$ delay time	t_{AWD}	45		55		65		ns	(Notes 18, 20)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 19)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 19)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

Notes [cont]:

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For $D_{OUT\ 9}$, parameters t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\ 9}$ (at access time and until $\overline{CAS}_9$ returns to V_{IH}) is indeterminate.

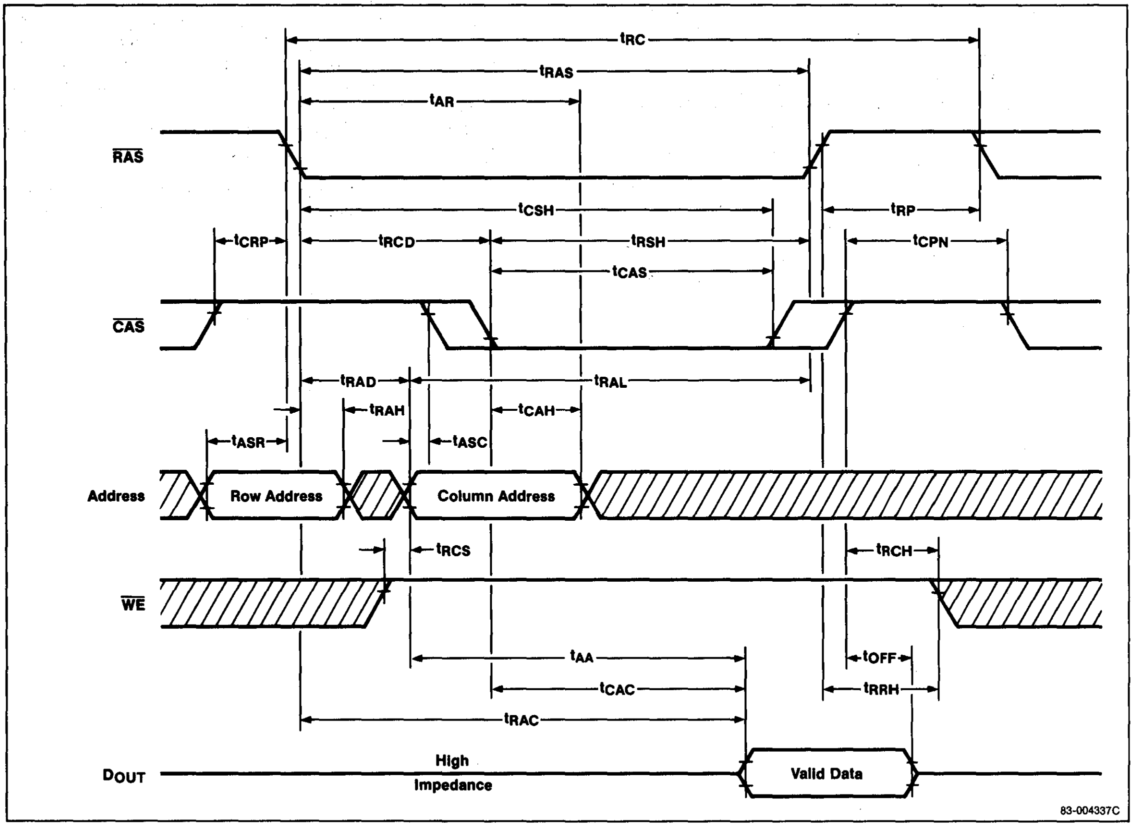
(19) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

(20) Read-write/read-modify-write operation can be performed only by the SOJ controlled by $\overline{CAS}_9$ because of its separate data input and output pins.

4

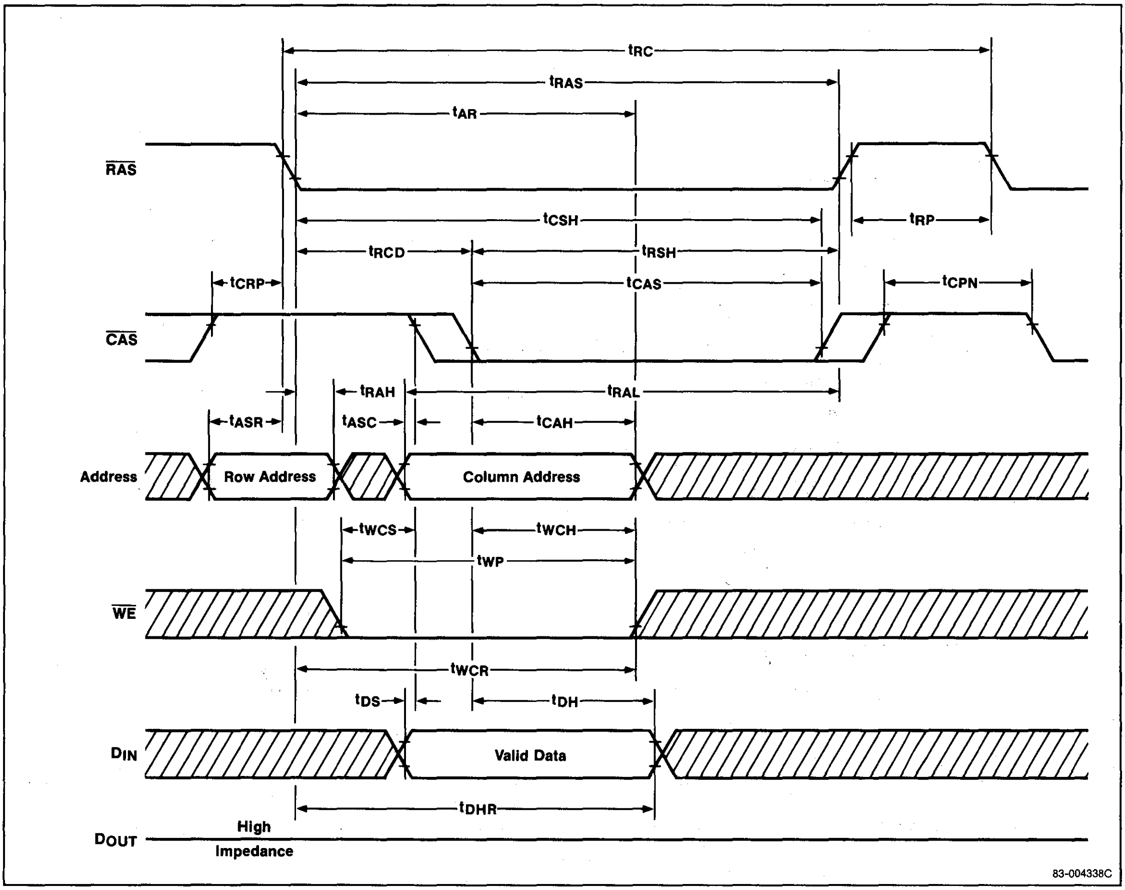
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

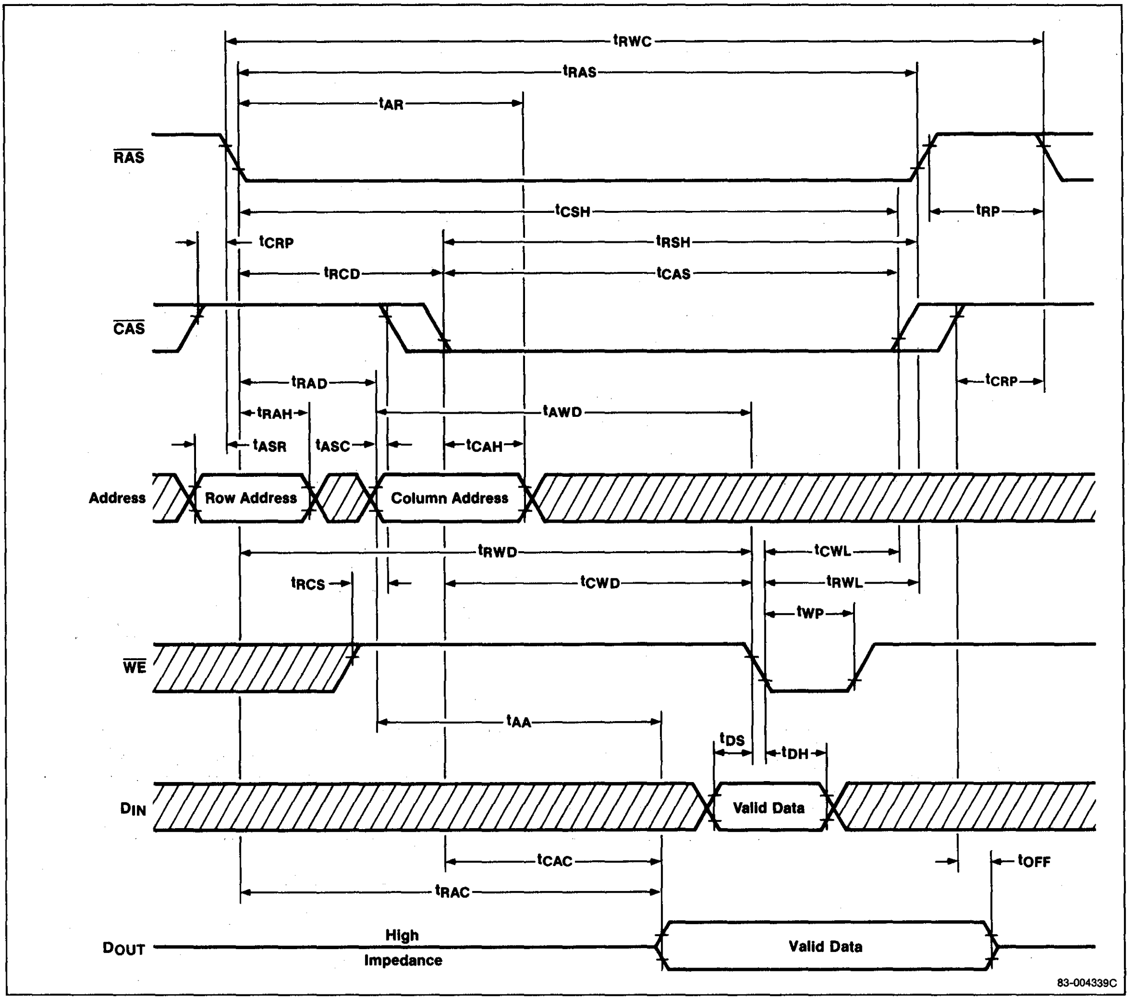
Write Cycle (Early Write)



4

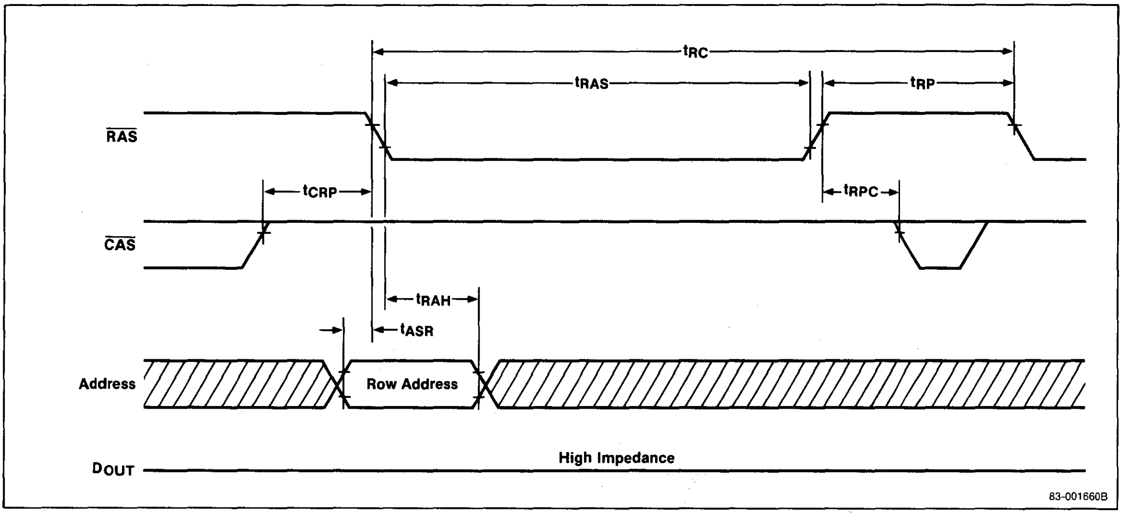
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT} 9 only)



Timing Waveforms (cont)

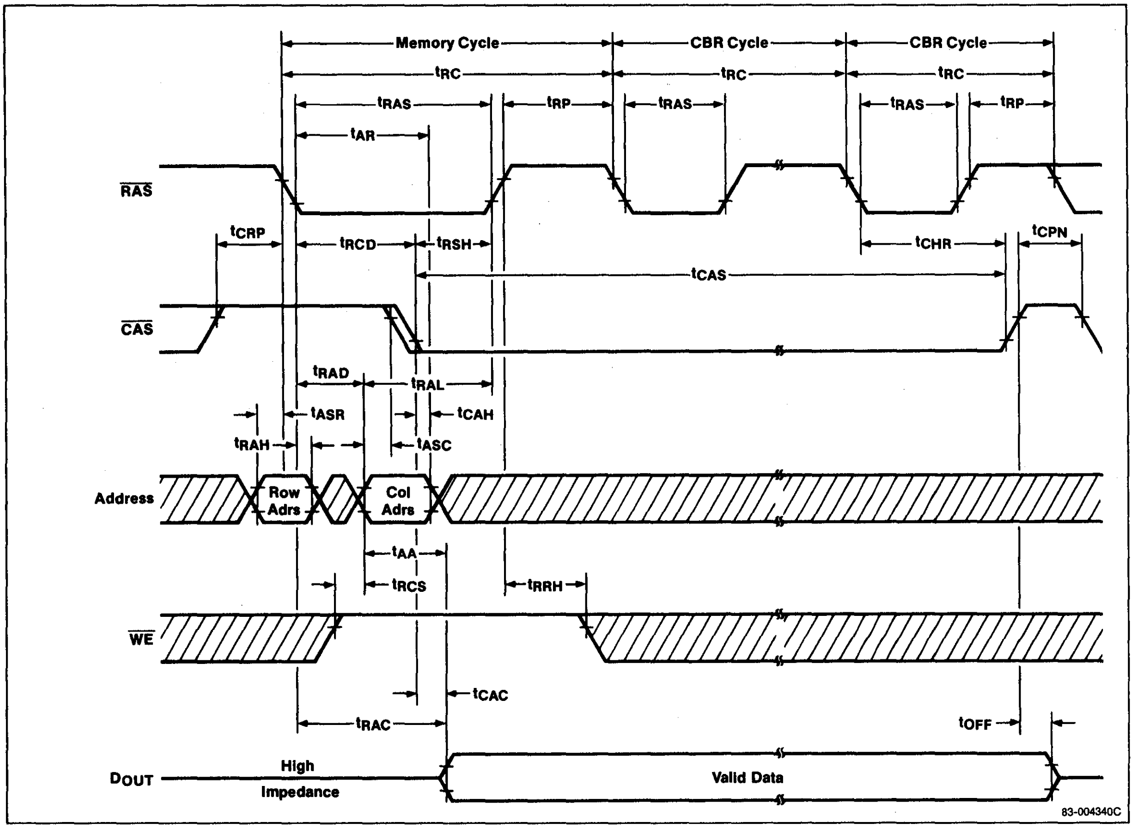
$\overline{RAS}$-Only Refresh Cycle



4

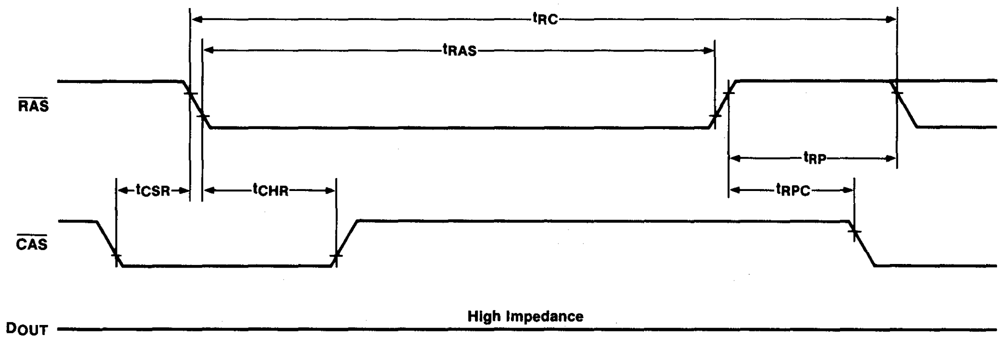
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

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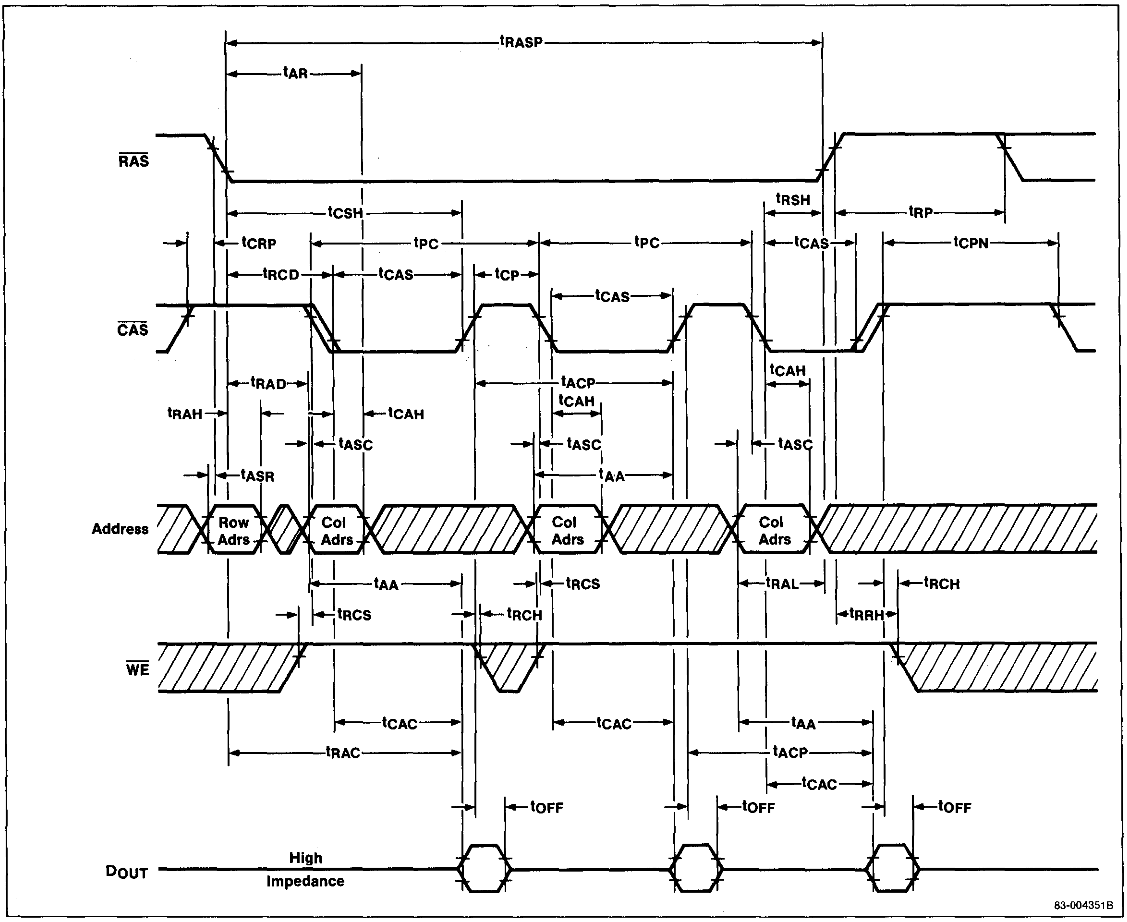
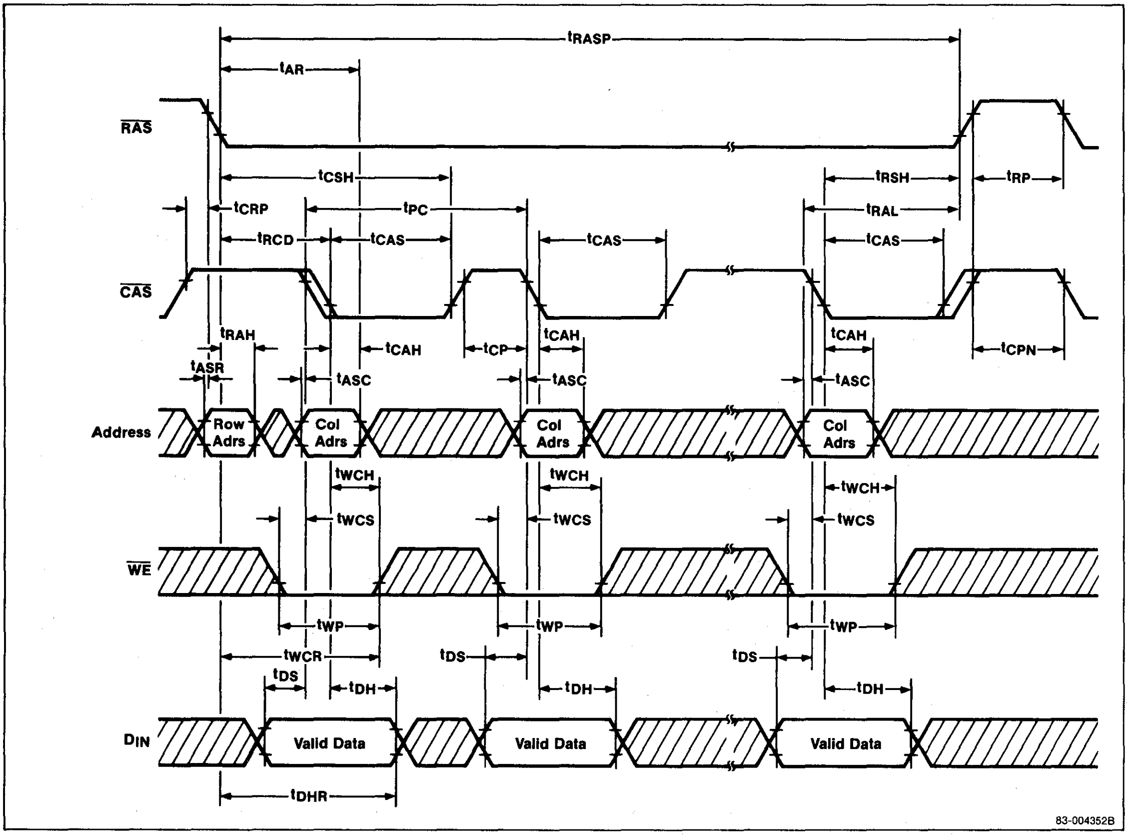
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

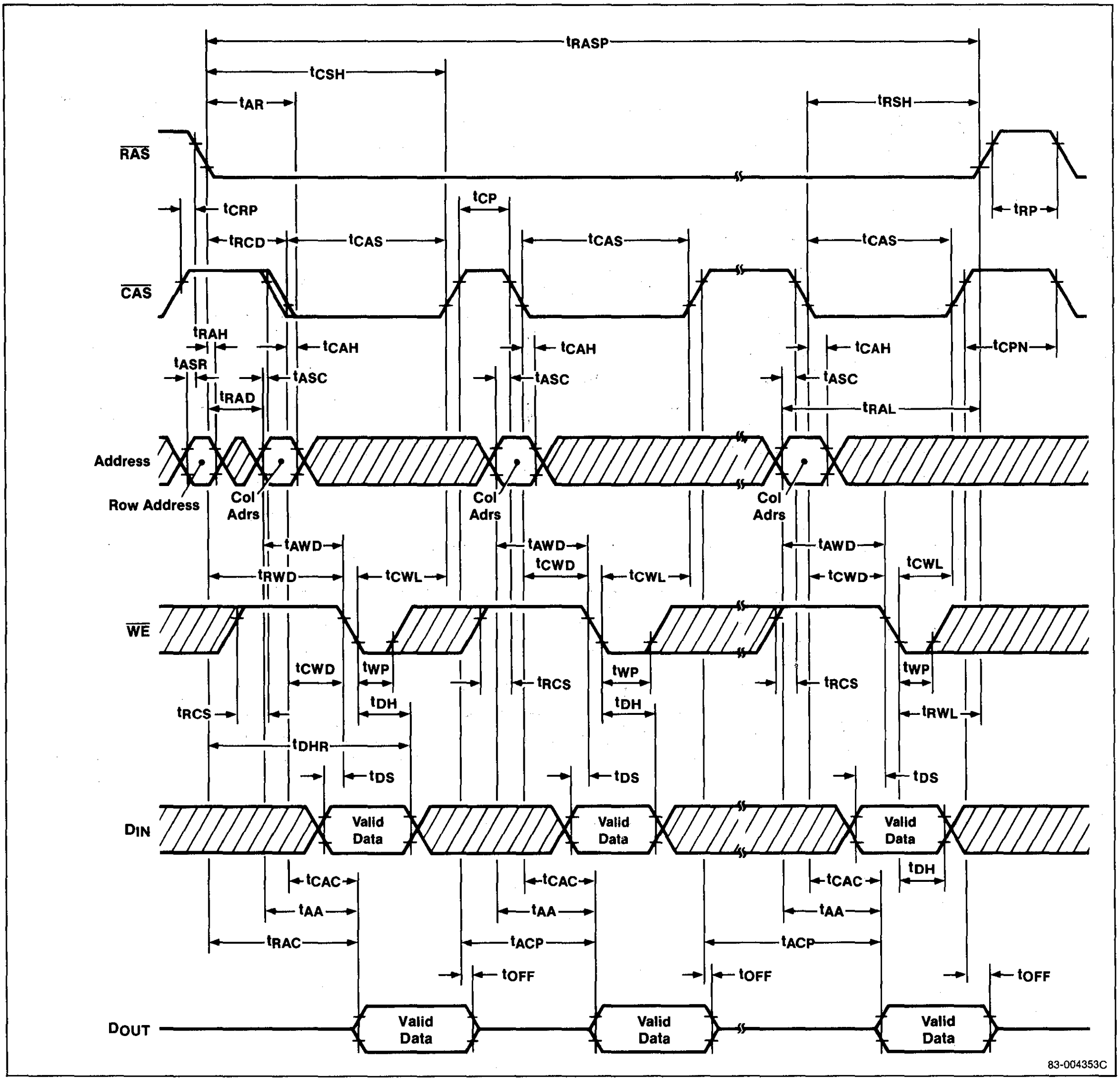
Fast-Page Write Cycle (Early Write)



4

Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle (D_{OUT9} only)



NEC

NEC Electronics Inc.

MC-421000B8
1,048,576 x 8-BIT
CMOS DYNAMIC RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-421000B8 is a nibble-mode 1,048,576-word by 8-bit dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000B8 is functionally equivalent to eight μPD421001 standard 1M DRAMs. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-421000B8 includes eight μPD421001s in SOJ packages and eight power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

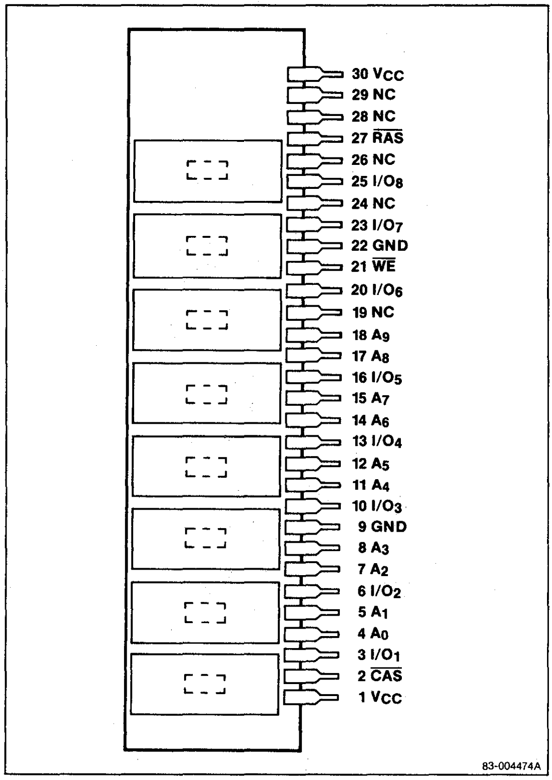
- ☐ 1,048,576-word by 8-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM)
- ☐ Eight 1M dynamic RAMs incorporated in high-density SOJ packaging (μPD421001LA)
- ☐ Eight power supply decoupling capacitors
- ☐ Low power dissipation: 44 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Nibble-mode capability

Ordering Information

Part Number	Row Access Time (max)	Column Access Time (max)	Address Access Time (max)	Package
MC-421000B8A-80	80 ns	20 ns	45 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	55 ns	
A-12	120 ns	30 ns	65 ns	
MC-421000B8B-80	80 ns	20 ns	45 ns	30-pin socketable SIMM
B-10	100 ns	25 ns	55 ns	
B-12	120 ns	30 ns	65 ns	

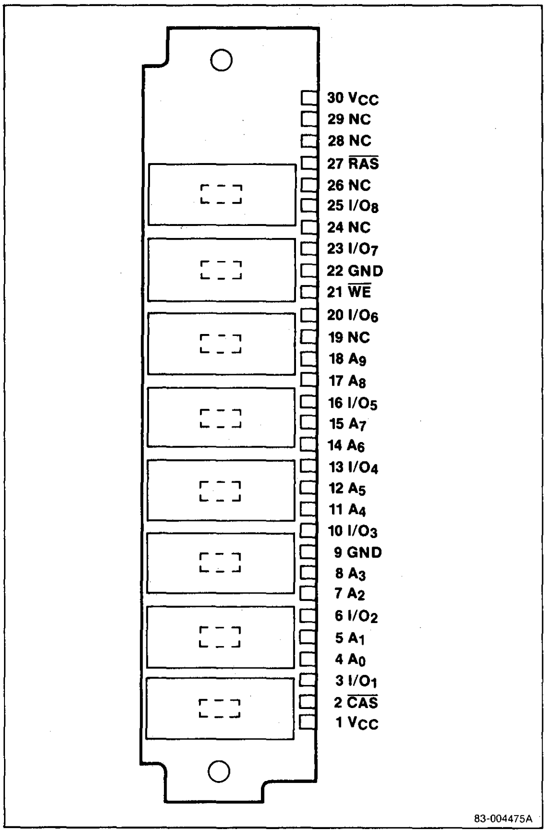
Pin Configurations

30-Pin SIMM, MC-421000B8A



Pin Configurations (cont)

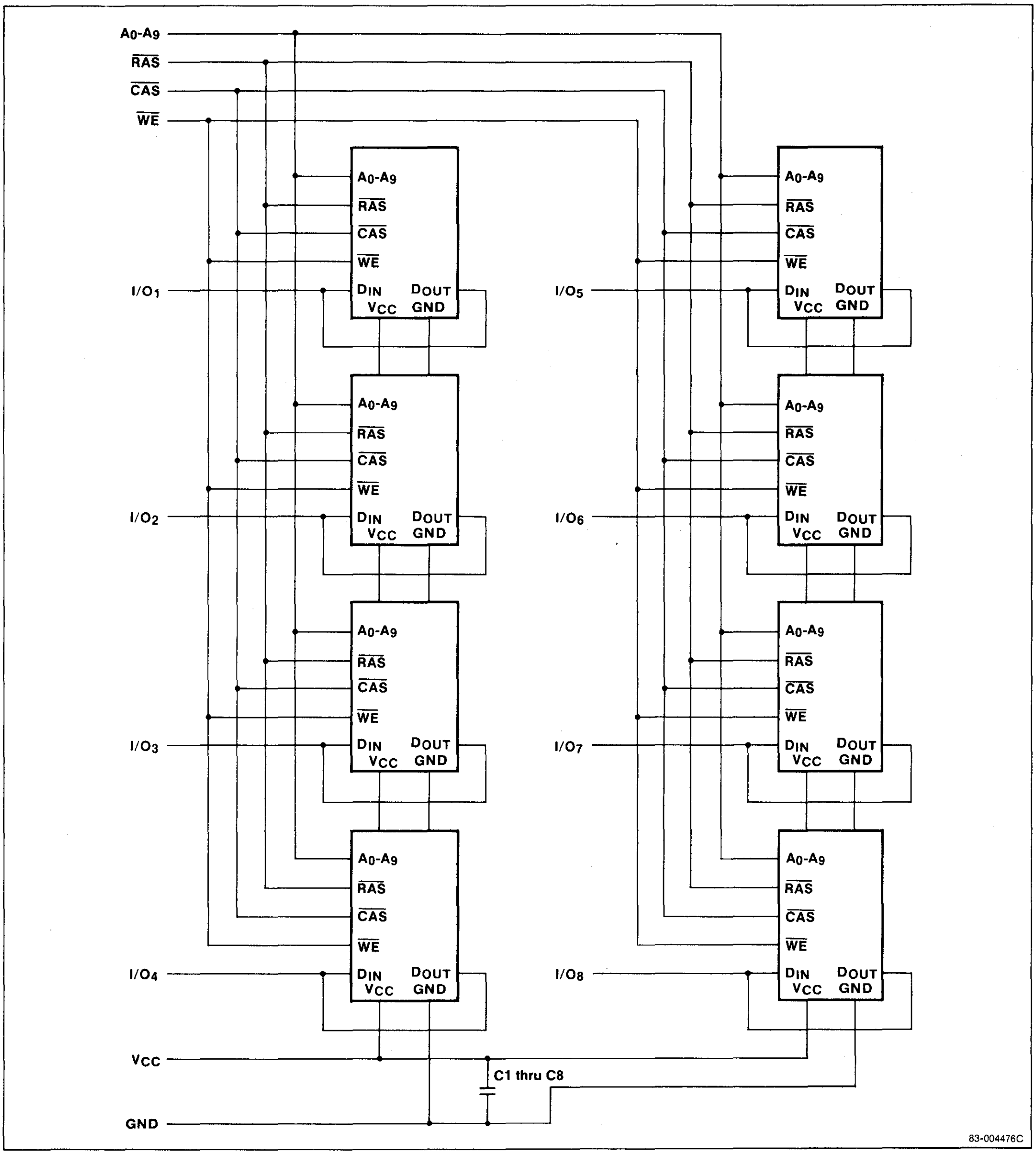
30-Pin SIMM, MC-421000B8B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



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Absolute Maximum Ratings

Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	–1.0		0.8	V	
Standby current	I_{CC2}			24	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$ (min)
				8	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V
Input leakage current	I_{IL}	–80		80	µA	For A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: $V_{IN} = 0$ to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	–10		10	µA	For I/O_1-I/O_8: D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

$T_A = 0$ to $+70\,°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits MC-421000B8-80 Min	Max	MC-421000B8-10 Min	Max	MC-421000B8-12 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		560		480		400	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		560		480		400	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		560		480		400	mA	$t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 11)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ pulse width (nibble mode)	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 12)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 13)
$\overline{CAS}$ precharge time (non-nibble mode)	t_{CPN}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	

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AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	MC-421000B8-80 Min	MC-421000B8-80 Max	MC-421000B8-10 Min	MC-421000B8-10 Max	MC-421000B8-12 Min	MC-421000B8-12 Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 14)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 14)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 15)
Write command to RAS lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 16)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 16)
Data-in hold time referenced to RAS	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	(Note 17)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	15		20		25		ns	(Note 17)
Nibble Mode									
Operating current, nibble mode, average	I_{CC4}		480		400		320	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{NC} = t_{NC}$ min; $I_O = 0$ mA (Note 5)
Nibble-mode cycle time	t_{NC}	40		45		55		ns	(Note 6)
Nibble-mode access time	t_{NAC}		20		25		30	ns	(Note 7)
$\overline{CAS}$ precharge time (nibble mode)	t_{NP}	10		10		15		ns	
$\overline{CAS}$ pulse width (nibble mode)	t_{NAS}	20		25		30		ns	
$\overline{RAS}$ hold time (nibble-mode read cycle)	t_{NRRSH}	20		25		30		ns	
$\overline{RAS}$ hold time (nibble-mode write cycle)	t_{NWRSH}	20		25		30		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70$°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles that are preceded by any cycle.

(14) Specifications for either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

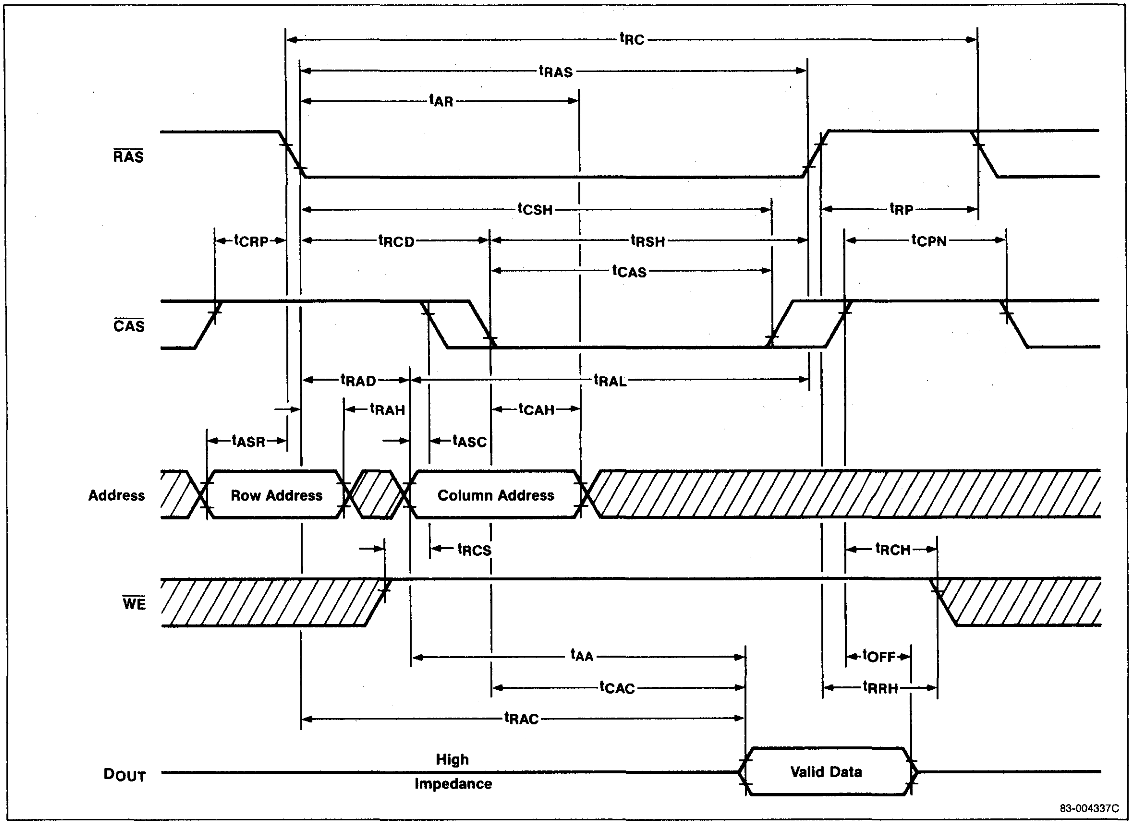
(15) For early write operation, specifications for both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(17) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

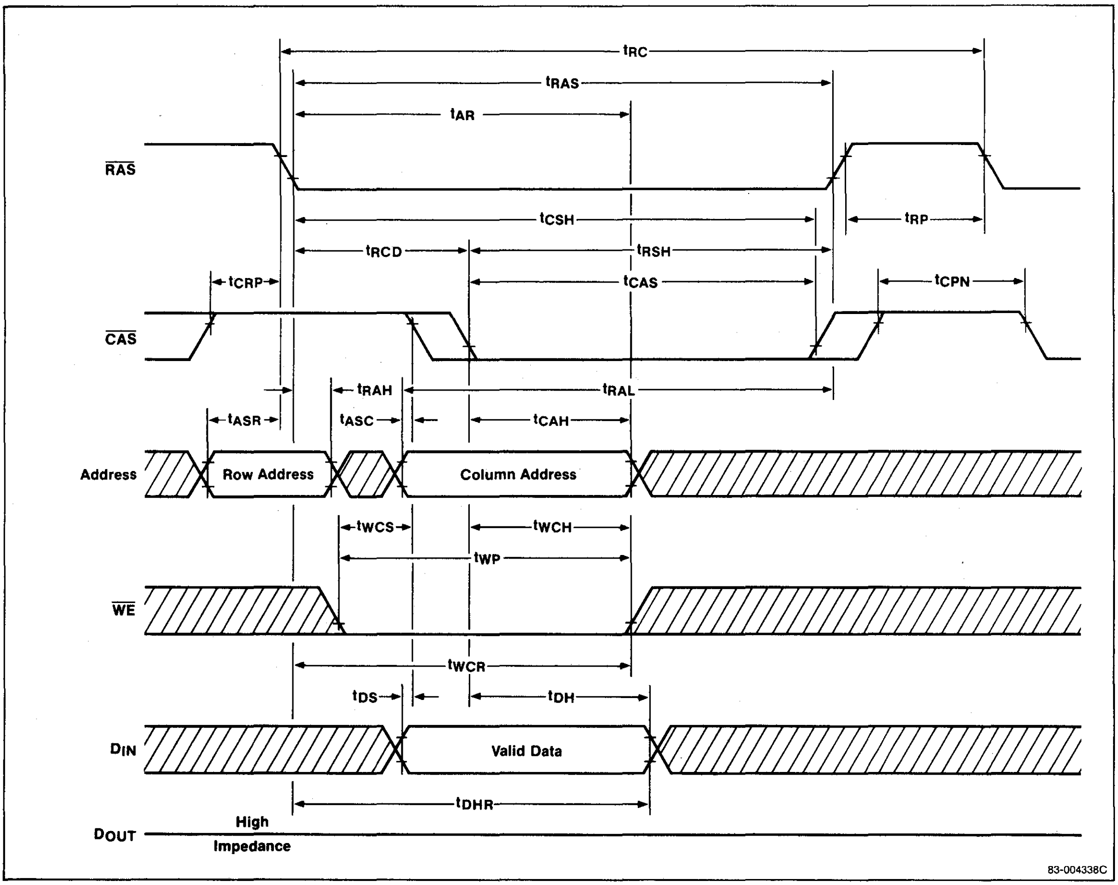
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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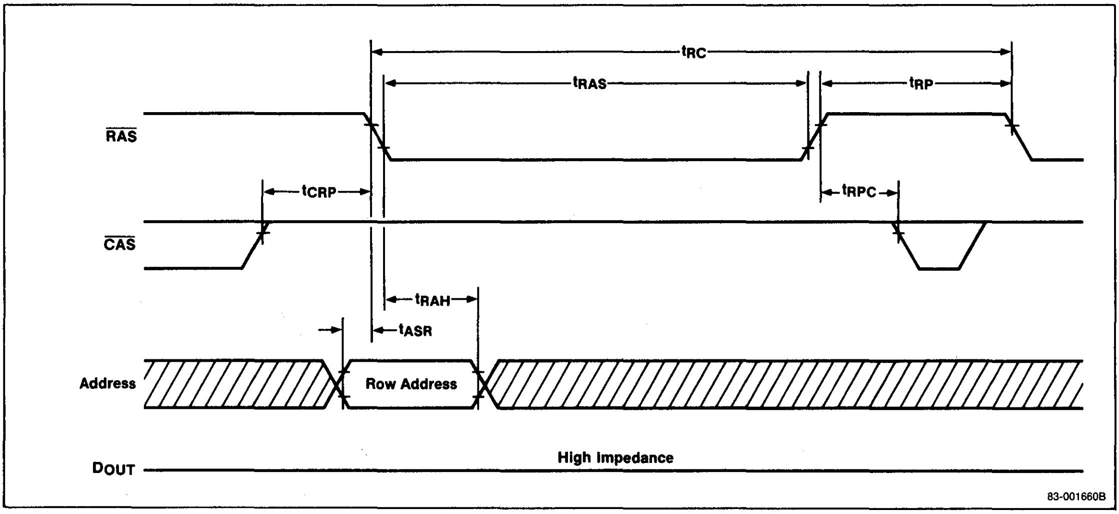
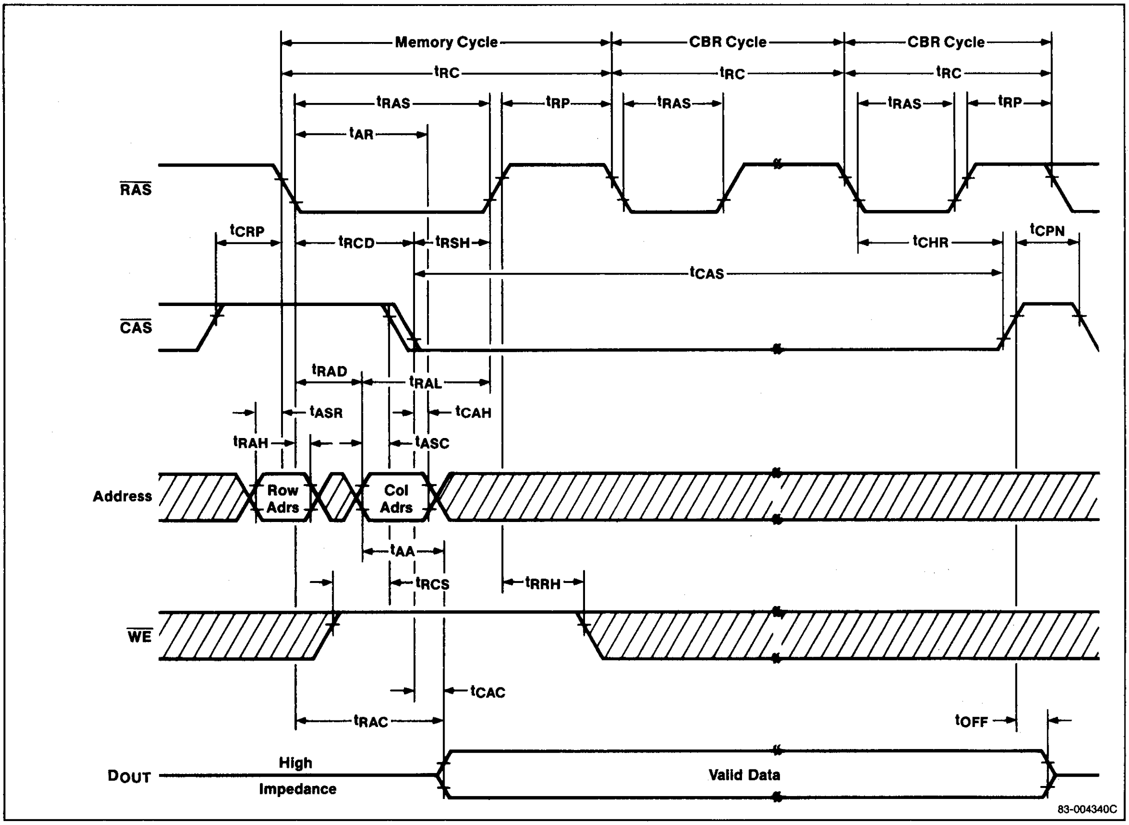
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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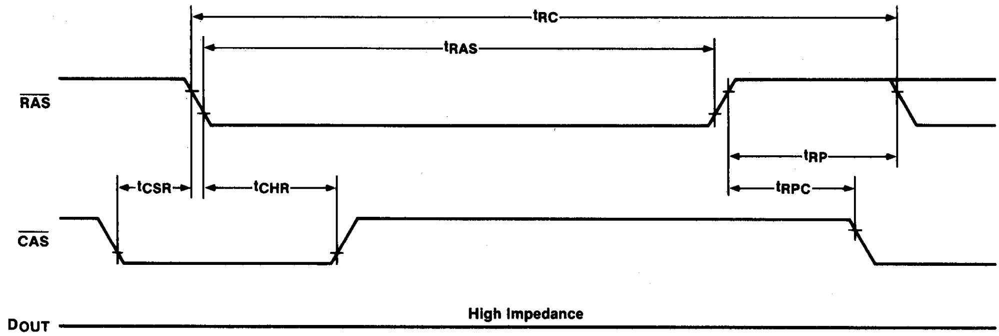
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

83-001979B

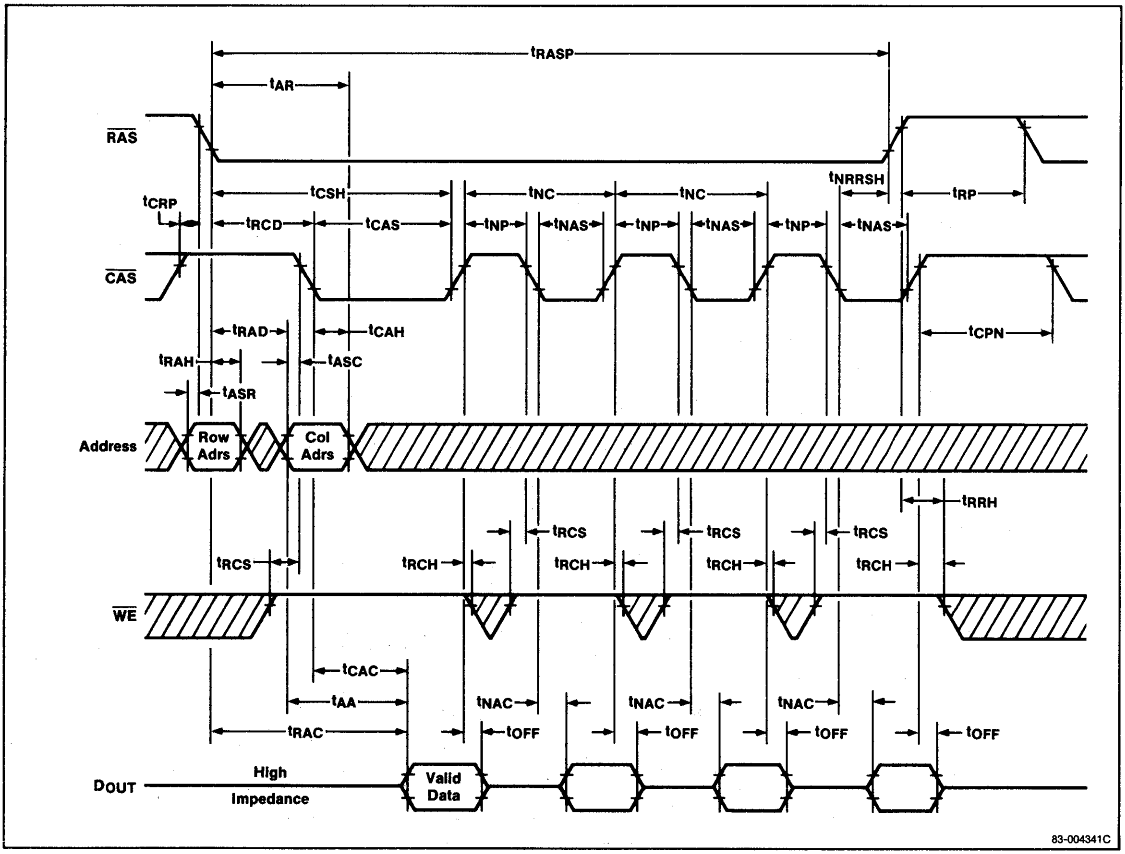
Nibble Mode

The μPD421000B8 is capable of executing nibble-mode read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of a maximum of 4 data bits per data output. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling $\overline{CAS}$ while $\overline{RAS}$ is held low. The addresses of nibble bits are determined by the combination of row address A_9 and column address A_9 in the following sequence.

		Row Address										Column Address										
Sequence	Nibble Bit	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}$/$\overline{CAS}$	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Example: external address input
$\overline{CAS}$ cycling	2	1	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Internal address generated
$\overline{CAS}$ cycling	3	0	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	4	1	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Repeated sequence

Timing Waveforms (cont)

Nibble-Mode Read Cycle



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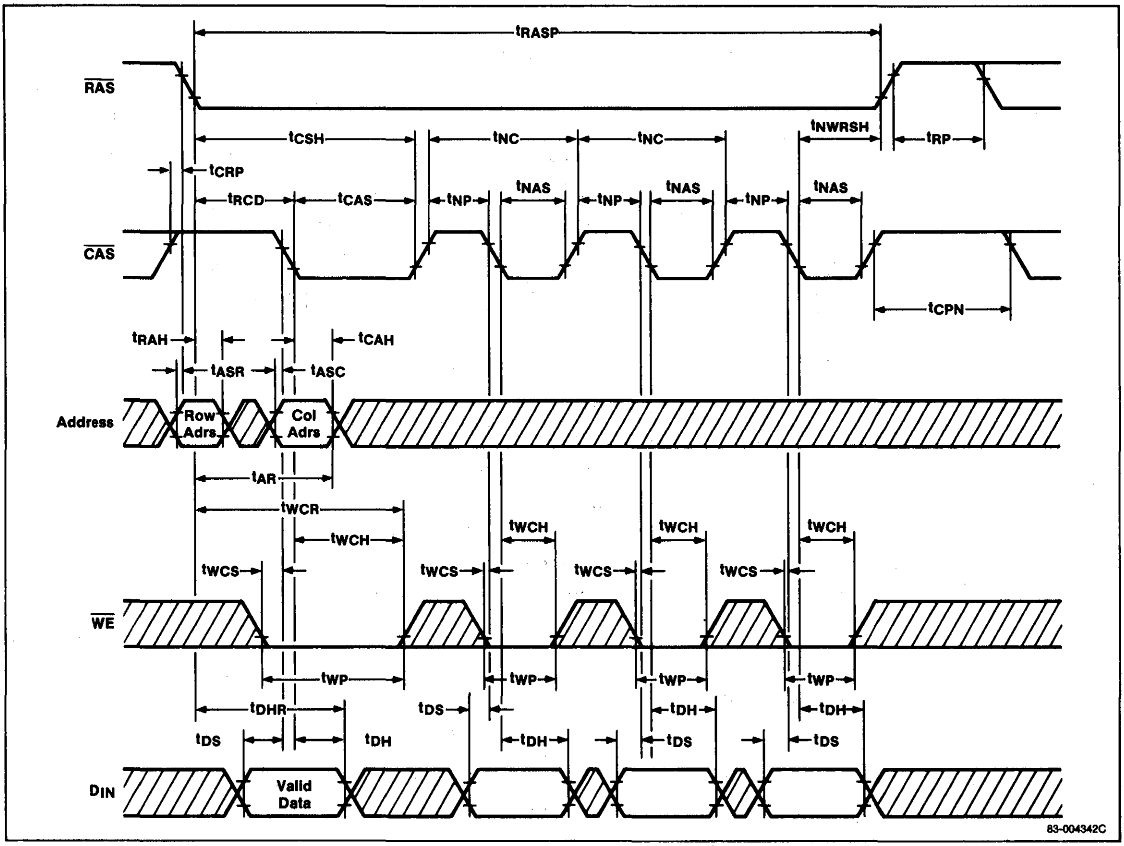
Timing Waveforms (cont)

Nibble-Mode Write Cycle (Early Write)



NEC
NEC Electronics Inc.

MC-421000B9
1,048,576 x 9-BIT
CMOS DYNAMIC RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-421000B9 is a nibble-mode 1,048,576-word by 9-bit CMOS dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000B9 is functionally equivalent to eight μPD421001 standard 1M DRAMs plus a parity bit. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-421000B9 includes nine μPD421001s in SOJ packages and nine power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

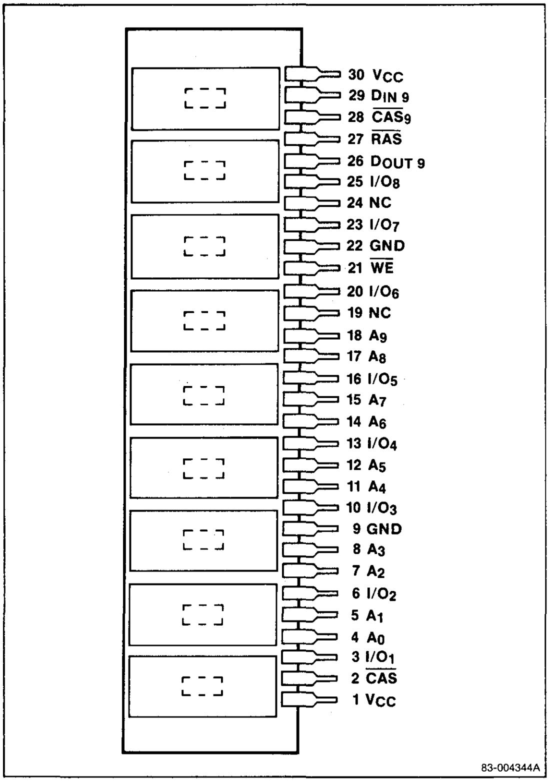
- ☐ 1,048,576-word by 9-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM)
- ☐ Nine 1M dynamic RAMs incorporated in high-density SOJ packaging (μPD421001LA)
- ☐ Nine power supply decoupling capacitors
- ☐ Low power dissipation: 49.5 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Nibble-mode capability

Ordering Information

Part Number	Row Access Time (max)	Column Access Time (max)	Address Access Time (max)	Package
MC-421000B9A-80	80 ns	20 ns	45 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	55 ns	
A-12	120 ns	30 ns	65 ns	
MC-421000B9B-80	80 ns	20 ns	45 ns	30-pin socket-able SIMM
B-10	100 ns	25 ns	55 ns	
B-12	120 ns	30 ns	65 ns	

Pin Configurations

30-Pin SIMM, MC-421000B9A



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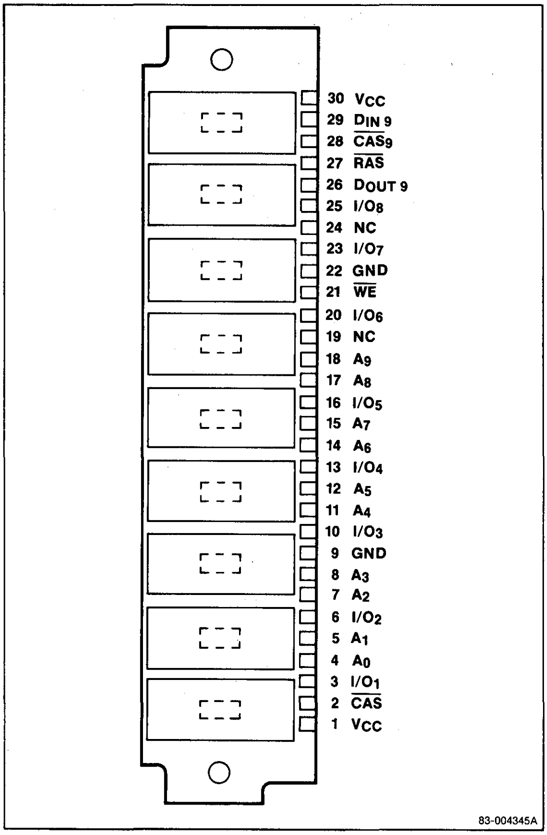
Pin Configurations (cont)

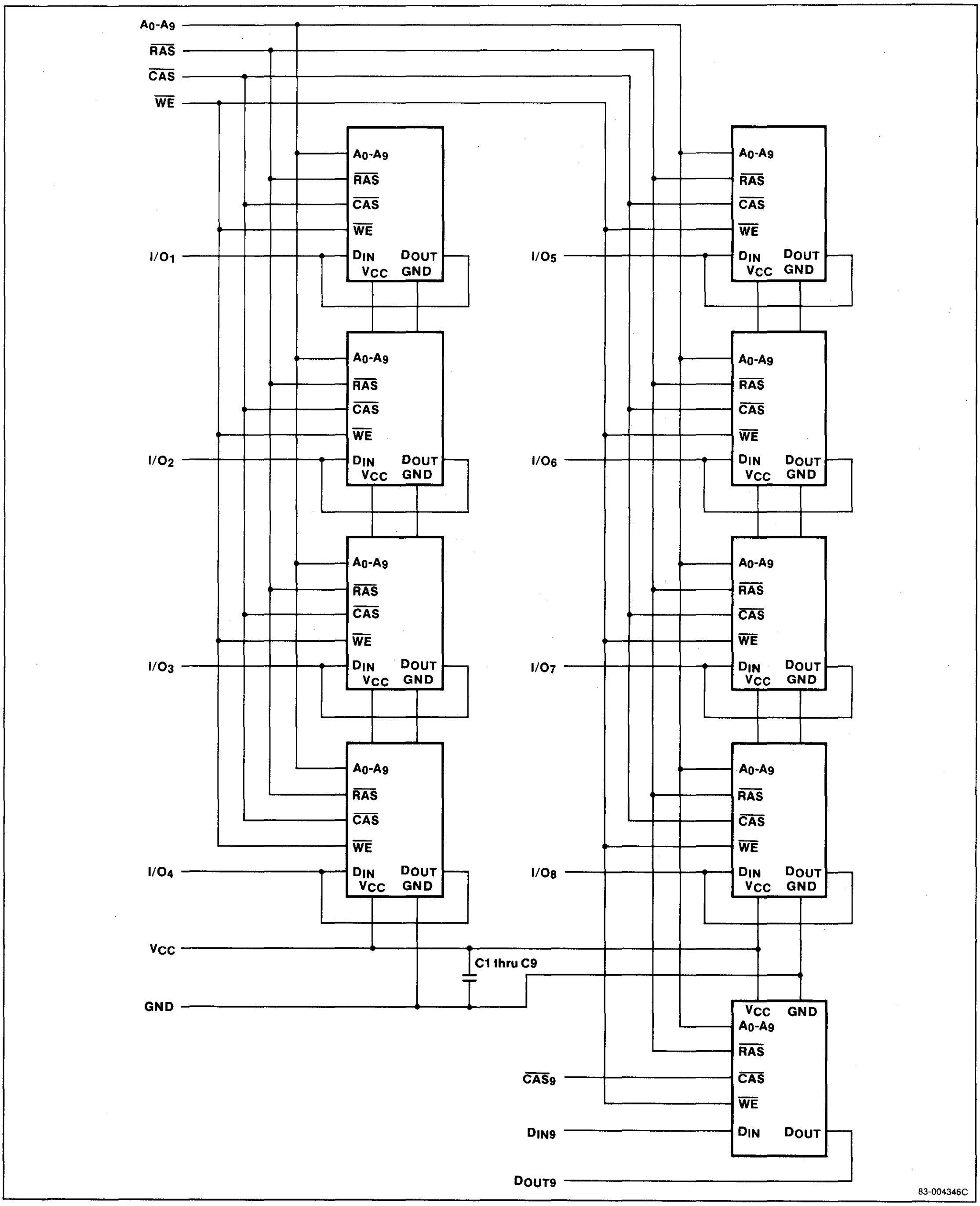
30-Pin SIMM, MC-421000B9B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$D_{IN\ 9}$	Data input 9
$D_{OUT\ 9}$	Data output 9
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{CAS_9}$	Column address strobe for data output 9
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25\,°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
	C_{I2}	7	pF	$\overline{CAS}_9$, $D_{IN\,9}$
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8
Output capacitance	C_O	10	pF	$D_{OUT\,9}$

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		$V_{CC} + 1.0$	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			27	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$
				9	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2\ V$
Input leakage current	I_{IL}	−90		90	µA	For A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: $V_{IN} = 0$ to 5.5 V; other pins = 0 V
Input leakage current	I_{IL9}	−10		10	µA	For $\overline{CAS}_9$ and $D_{IN\,9}$: $V_{IN} = 0$ to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	µA	For I/O_1-I/O_8 and $D_{OUT\,9}$: D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		MC-421000B9-80		MC-421000B9-10		MC-421000B9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		630		540		450	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		630		540		450	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		630		540		450	mA	$t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Notes 6, 19)
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 11)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ pulse width (nibble mode)	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 12)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 13)
$\overline{CAS}$ precharge time (non-nibble mode)	t_{CPN}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm10\%$

		Limits							
		MC-421000B9-80		MC-421000B9-10		MC-421000B9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 14)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 14)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 15)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 16)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 17)
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20		25		30		ns	(Note 17, 19)
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80		100		120		ns	(Note 17, 19)
Column address to $\overline{WE}$ delay time	t_{AWD}	45		50		60		ns	(Note 17, 19)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 18)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 18)
Nibble Mode									
Operating current, nibble mode, average	I_{CC4}		540		450		360	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{NC} = t_{NC}$ min; $I_O = 0$ mA (Note 5)
Nibble-mode cycle time	t_{NC}	40		45		55		ns	(Note 6)
Nibble-mode access time	t_{NAC}		20		25		30	ns	(Note 7)
$\overline{CAS}$ precharge time, nibble mode	t_{NP}	10		10		15		ns	
$\overline{CAS}$ pulse width, nibble mode	t_{NAS}	20		25		30		ns	

AC Characteristics (cont)

$T_A = 0$ to $+70\,°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000B9-80		MC-421000B9-10		MC-421000B9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Nibble Mode (cont)									
$\overline{RAS}$ hold time (nibble-mode read cycle)	t_{NRRSH}	20		25		30		ns	
$\overline{RAS}$ hold time (nibble-mode write cycle)	t_{NWRSH}	20		25		30		ns	
$\overline{CAS}$ to $\overline{WE}$ delay (nibble mode)	t_{NCWD}	20		25		30		ns	(Note 17)
Write command to $\overline{CAS}$ lead time (nibble mode)	t_{NCWL}	20		25		30		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70\,°C$) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) For $D_{OUT\,9}$, parameters t_{WCS}, t_{CWD}, t_{NCWD}, t_{RWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write and nibble-mode read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write or nibble-mode early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If $t_{NCWD} \geq t_{NCWD}$ (min), the cycle is a nibble-mode read-write cycle and the data output will contain data from the selected cell. If none of the above conditions are met, the condition of $D_{OUT\,9}$ (at access time and until $\overline{CAS}_9$ returns to V_{IH}) is indeterminate.

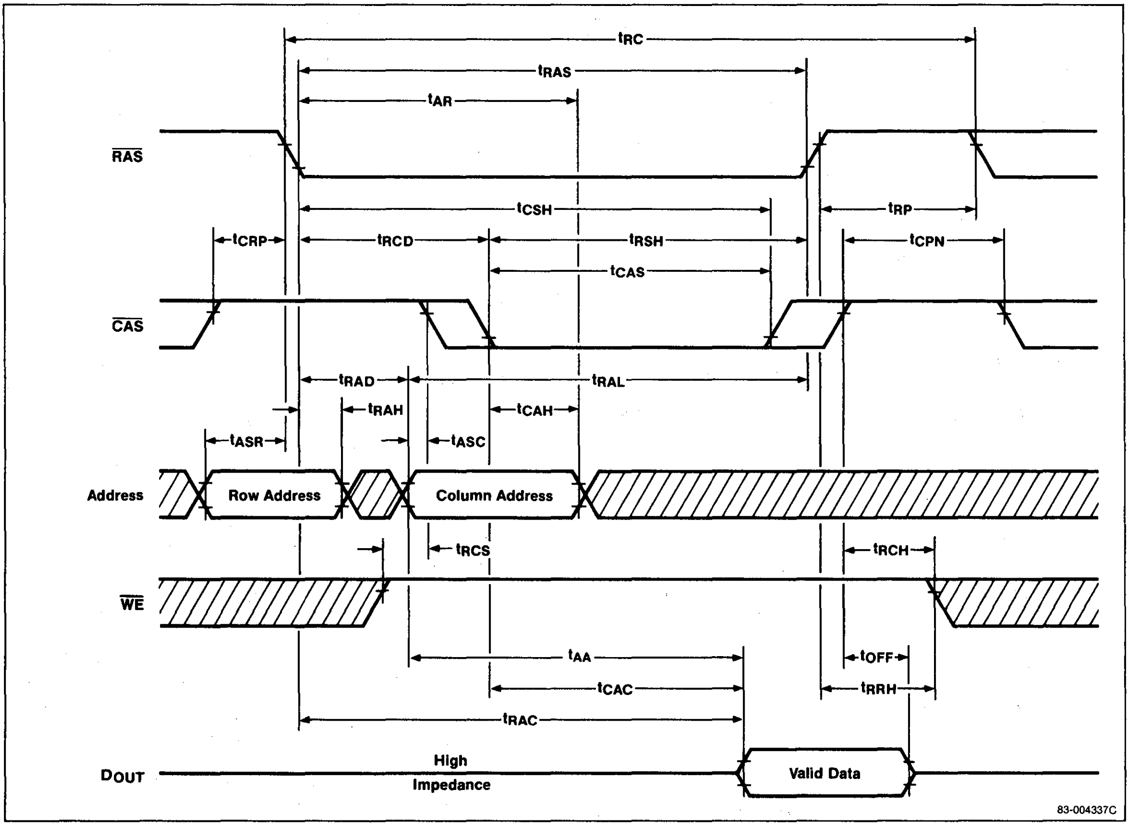
(18) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

(19) Read-write/read-modify-write operation can be performed only by the SOJ controlled by $\overline{CAS}_9$ because of its separate data input and output pins.

4

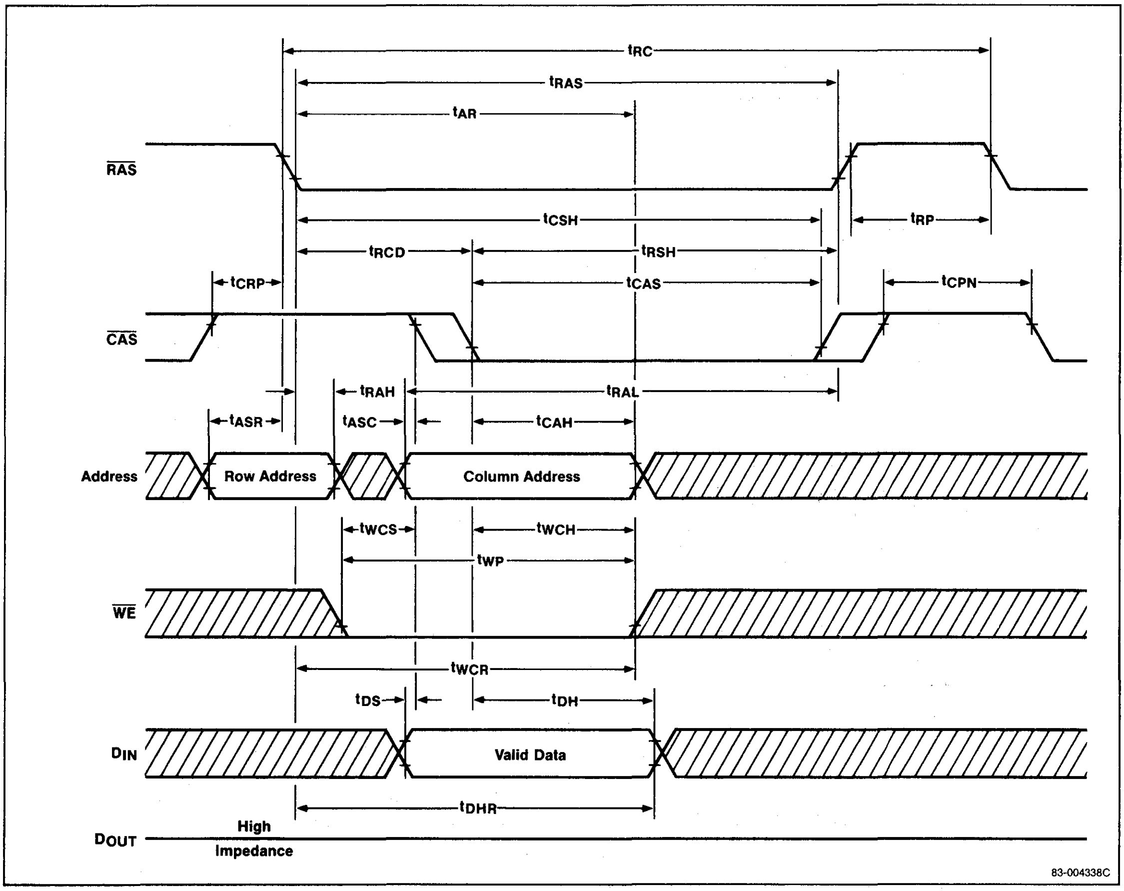
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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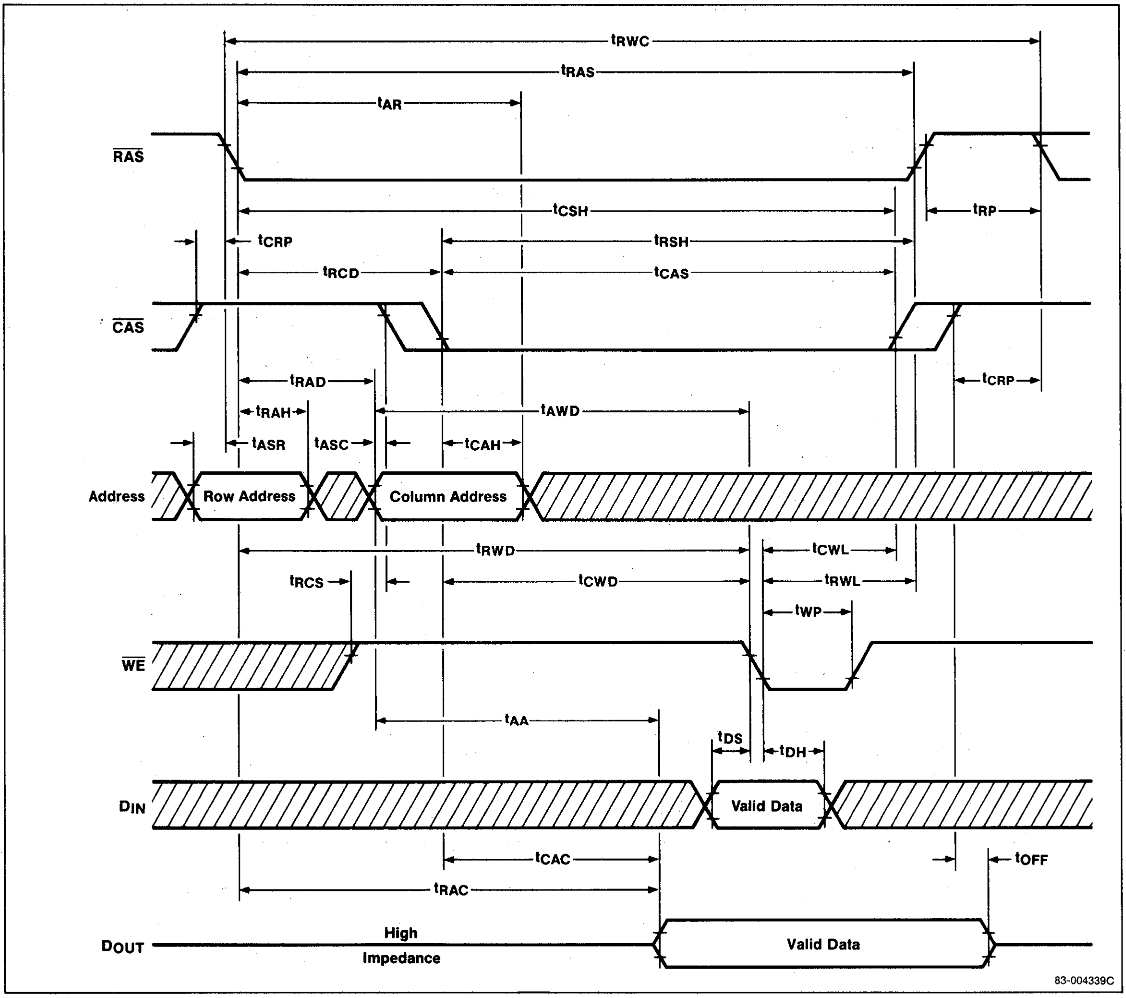
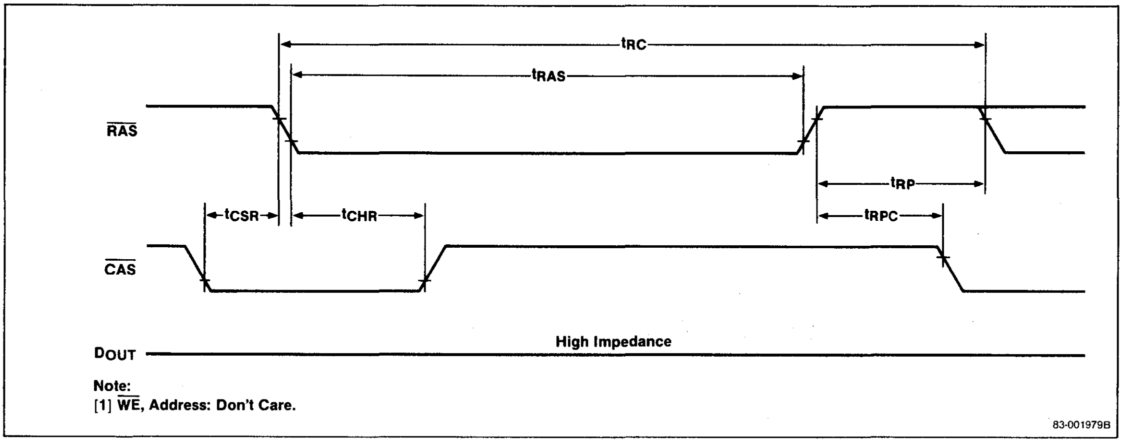
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT9} only)

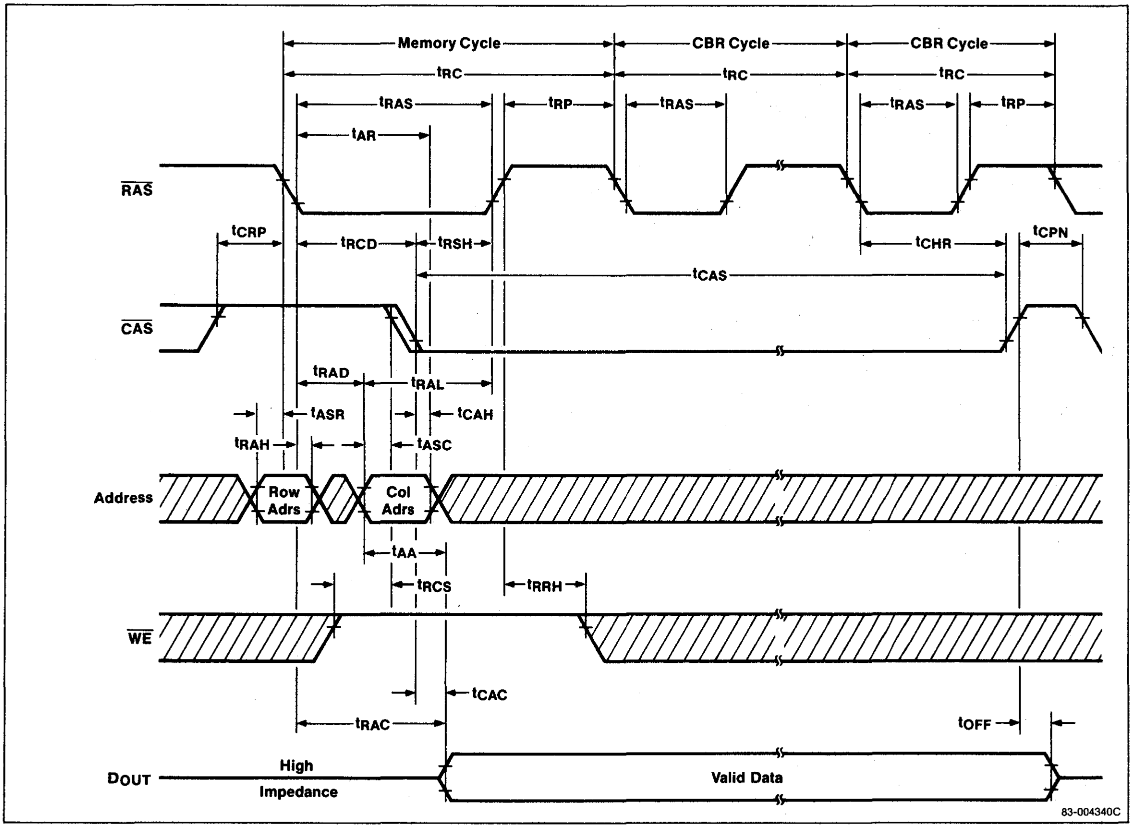


Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

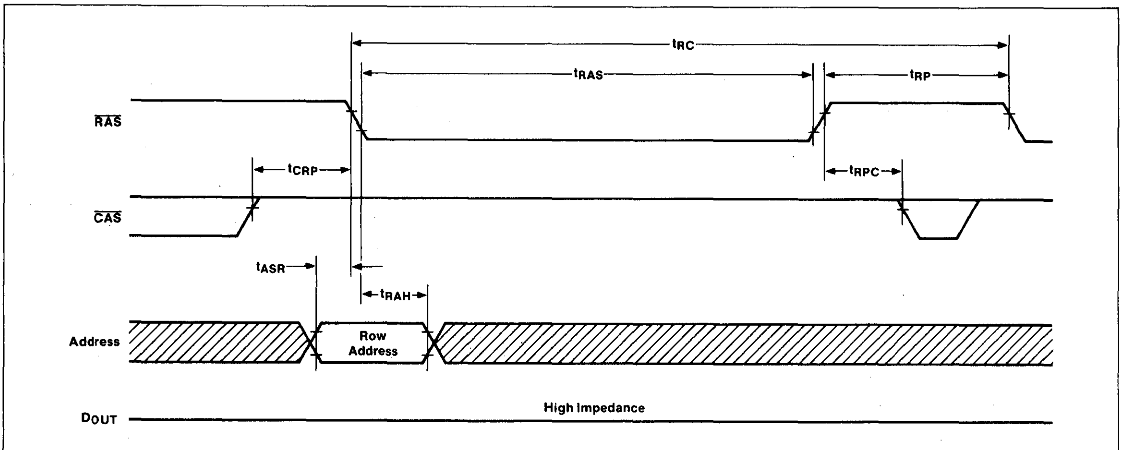


Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



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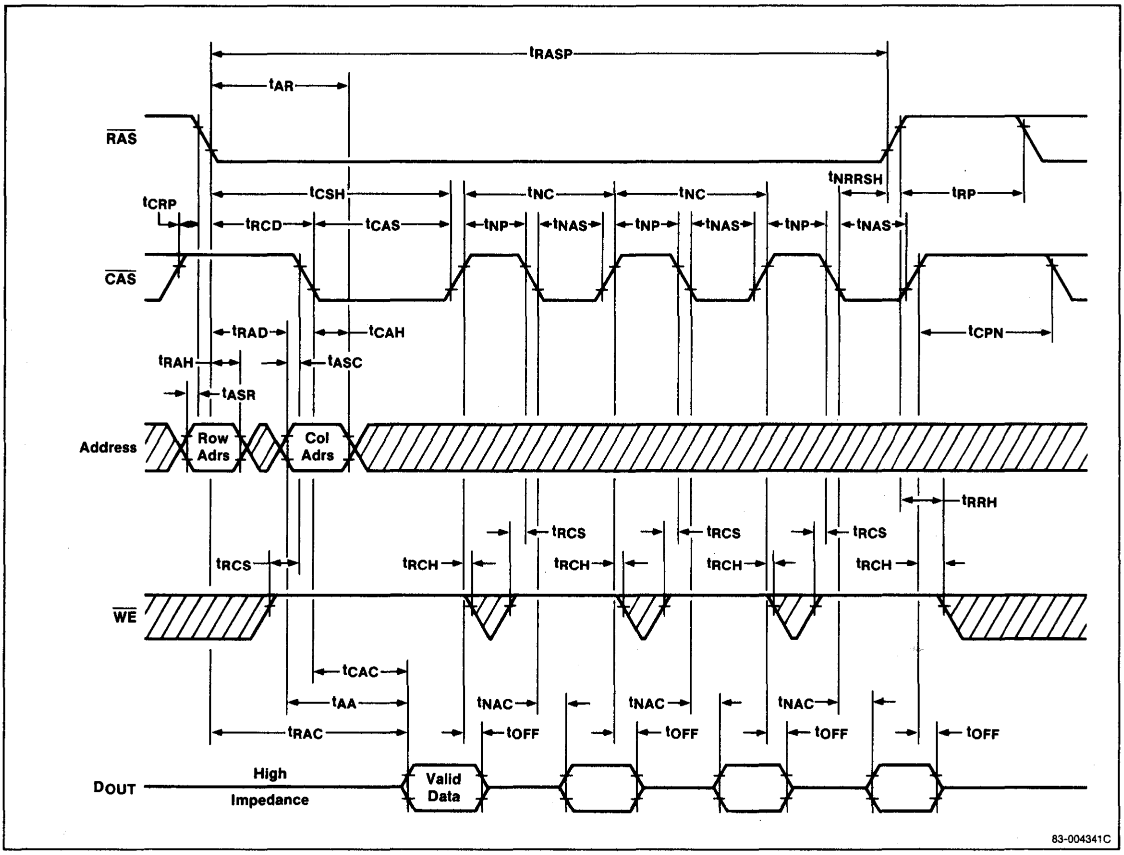
Nibble Mode

The μPD421000B9 is capable of executing nibble-mode read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of a maximum of 4 data bits per data output. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling $\overline{CAS}$ while $\overline{RAS}$ is held low. The addresses of nibble bits are determined by the combination of row address A_9 and column address A_9 in the following sequence.

		Row Address										Column Address										
Sequence	Nibble Bit	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}$/$\overline{CAS}$	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Example: external address input
$\overline{CAS}$ cycling	2	1	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Internal address generated
$\overline{CAS}$ cycling	3	0	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	4	1	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Repeated sequence

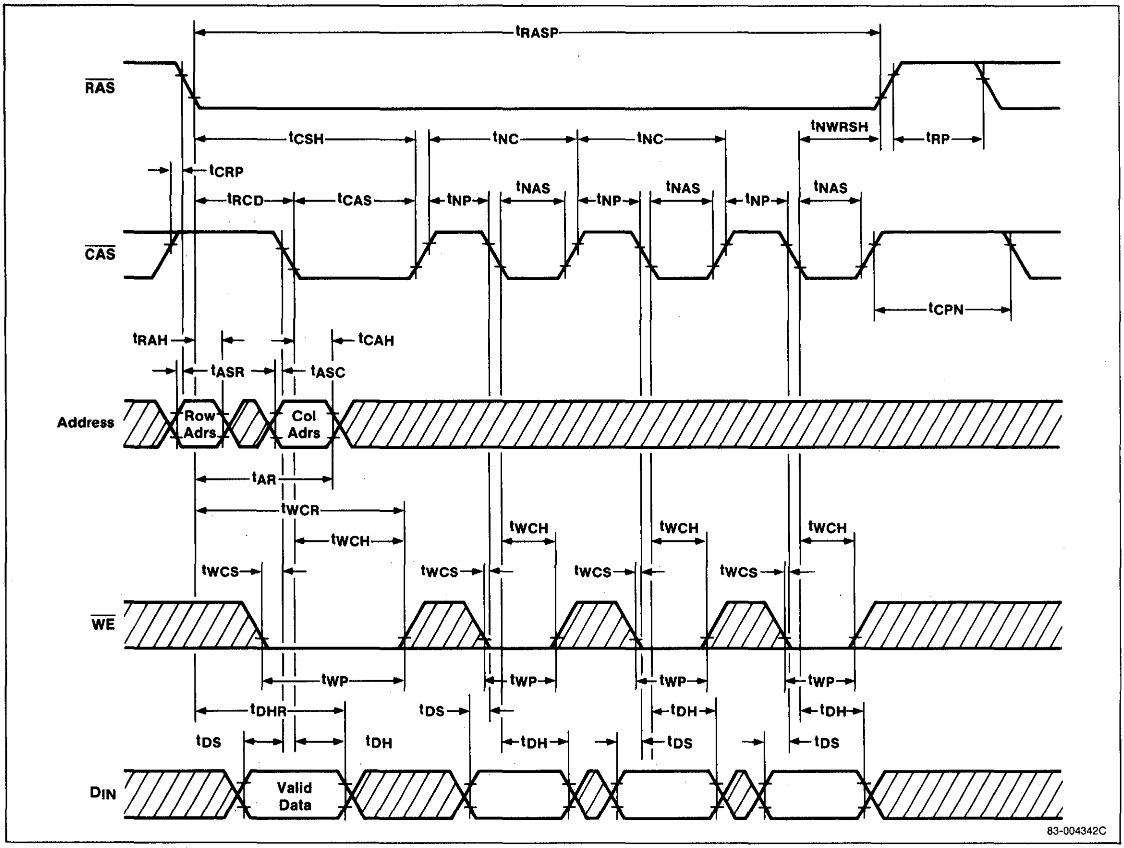
Timing Waveforms (cont)

Nibble Read Cycle



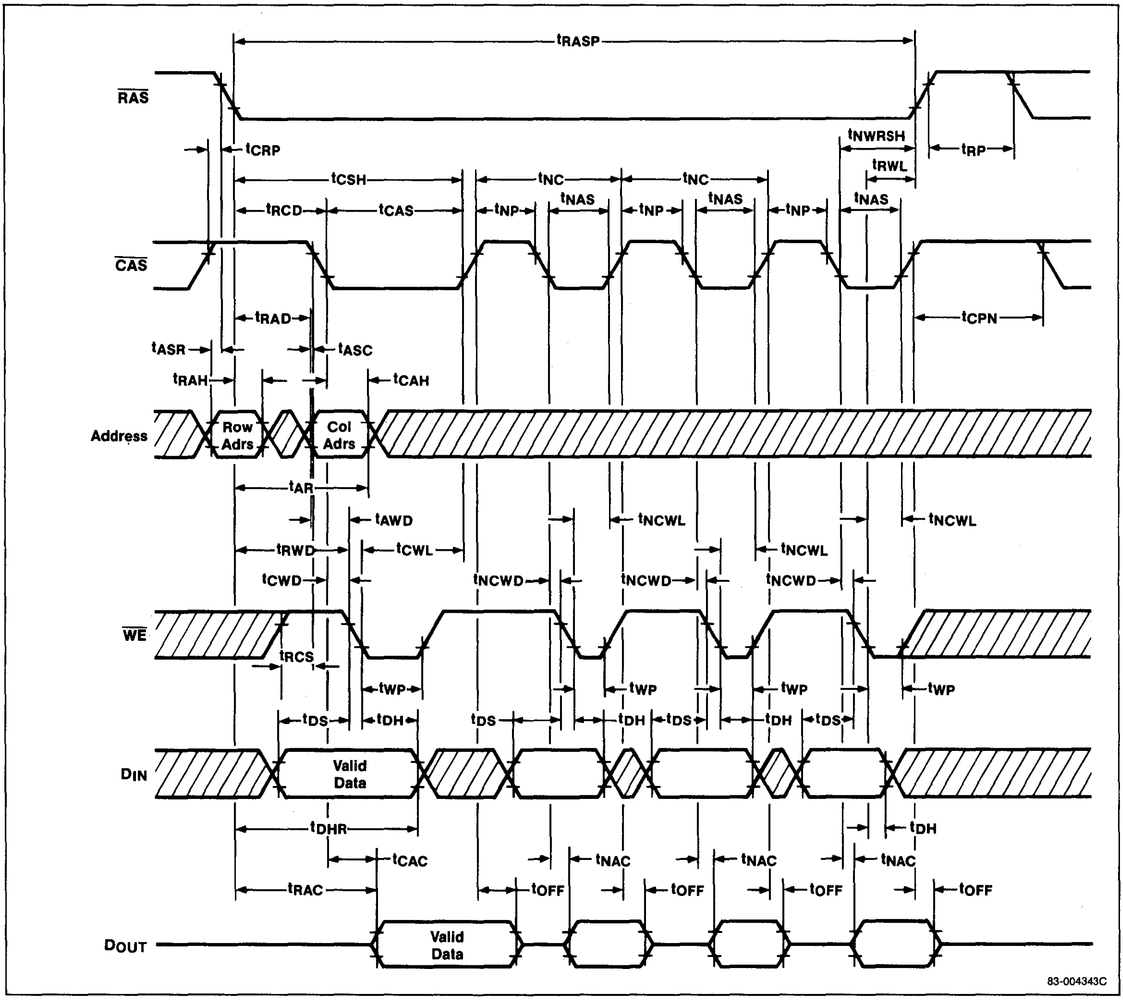
Timing Waveforms (cont)

Nibble Write Cycle (Early Write)



Timing Waveforms (cont)

Nibble Read-Write/Read-Modify-Write Cycle ($D_{OUT\,9}$ only)



NEC

NEC Electronics Inc.

MC-421000C8
1,048,576 x 8-BIT
CMOS DYNAMIC RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-421000C8 is a static-column, 1,048,576-word by 8-bit dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000C8 is functionally equivalent to eight μPD421002 standard 1M DRAMs. Refreshing is accomplished by means of $\overline{\text{RAS}}$-only refresh cycles, hidden refresh cycles, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-421000C8 includes eight μPD421002s in SOJ packages and eight power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

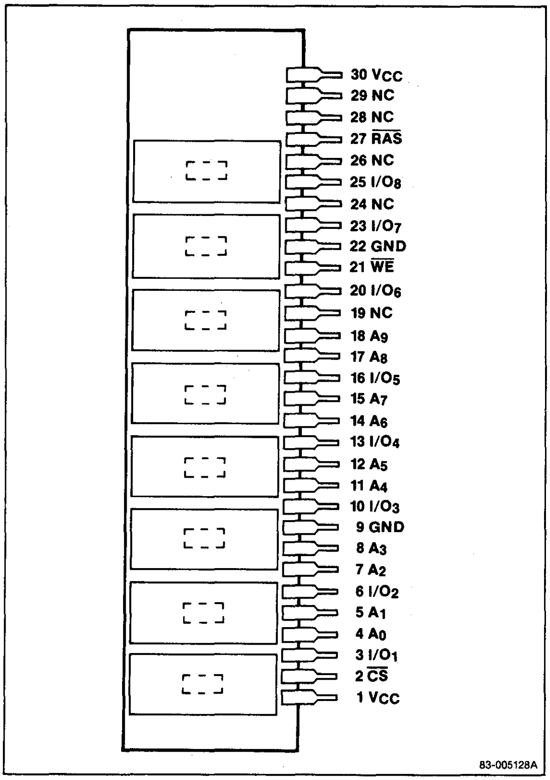
- ☐ 1,048,576-word by 8-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM)
- ☐ Eight 1M dynamic RAMs incorporated in high-density SOJ packaging (μPD421002LA)
- ☐ Eight power supply decoupling capacitors
- ☐ Low power dissipation: 44 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Static-column capability

Ordering Information

Part Number	Row Access Time (max)	Column Access Time (max)	Address Access Time (max)	Package
MC-421000C8A-80	80 ns	20 ns	45 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	55 ns	
A-12	120 ns	30 ns	65 ns	
MC-421000C8B-80	80 ns	20 ns	45 ns	30-pin socket-able SIMM
B-10	100 ns	25 ns	55 ns	
B-12	120 ns	30 ns	65 ns	

Pin Configurations

30-Pin SIMM, MC-421000C8A



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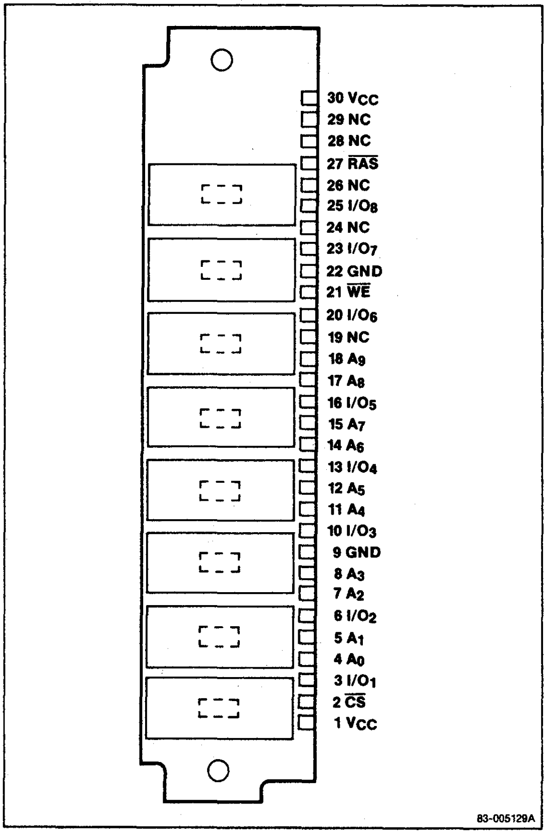
Pin Configurations (cont)

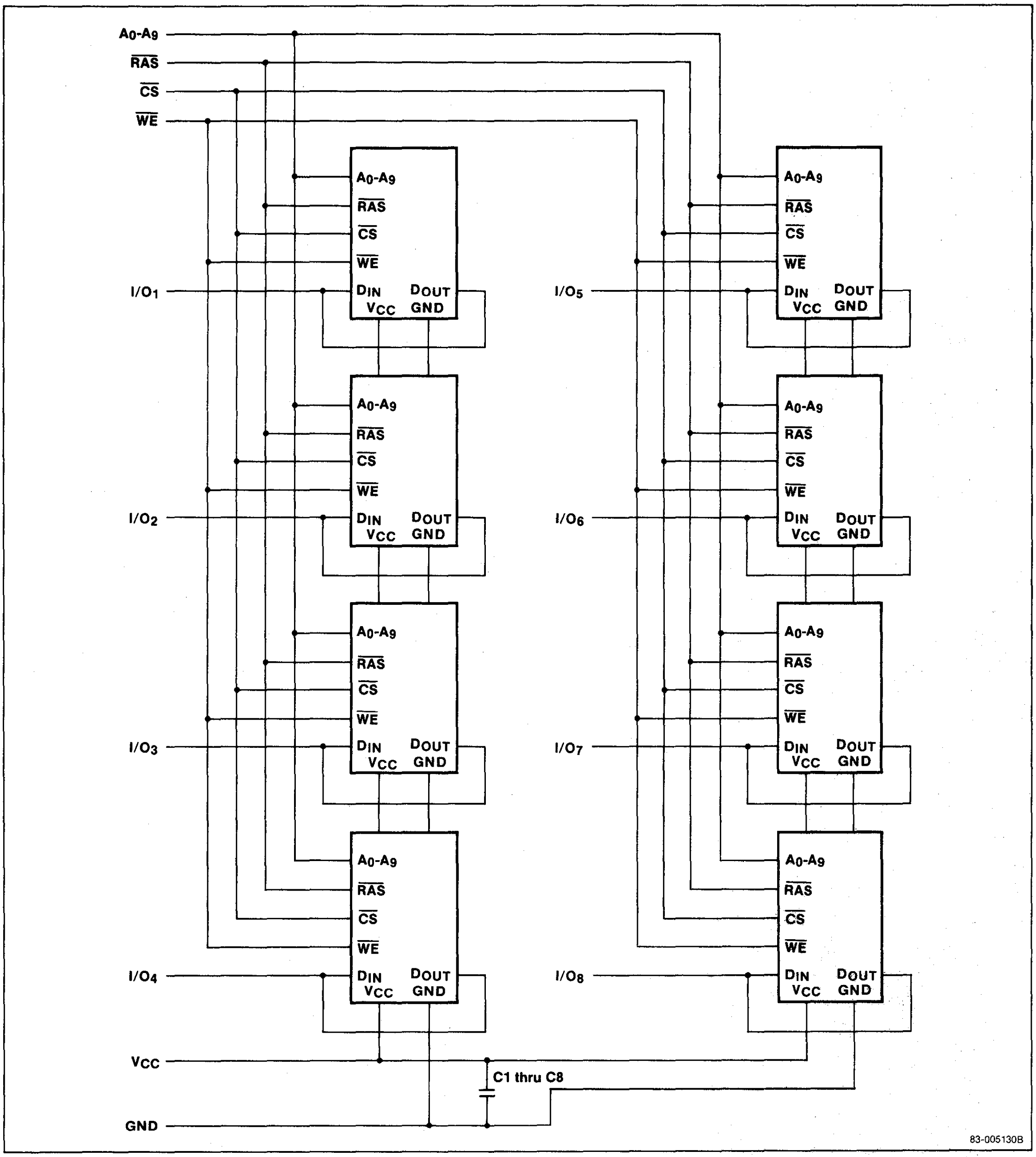
30-Pin SIMM, MC-421000C8B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



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Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	8.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	60	pF	A_0-A_9, $\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			16	mA	$\overline{RAS} = \overline{CS} \geq V_{IH}$ (min)
				8	mA	$\overline{RAS} = \overline{CS} \geq V_{CC} - 0.2$ V
Input leakage current	I_{IL}	−80		80	μA	For A_0-A_9, $\overline{RAS}$, $\overline{CS}$, $\overline{WE}$: $V_{IN} = 0$ to V_{CC}; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1-I/O_8: D_{OUT} disabled; $V_{OUT} = 0$ to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits MC-421000C8-80 Min	Max	MC-421000C8-10 Min	Max	MC-421000C8-12 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		560		480		400	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		560		480		400	mA	$\overline{RAS}$ cycling; $\overline{CS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		560		480		400	mA	$t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CS}$	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 11)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CS}$ pulse width	t_{CS}	20	100000	25	100000	30	100000	ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 12)
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 13)
$\overline{CS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		120		ns	

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AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000C8-80		MC-421000C8-10		MC-421000C8-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{RAS}$ to column address hold time	t_{AH}	15		15		15		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 14)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	(Note 14)
Column address hold time referenced to $\overline{RAS}$ (write cycle)	t_{AWR}	60		70		85		ns	
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 15)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 16)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 16)
Data-in hold time referenced to RAS	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 17)
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 17)
Static-Column Operation									
Static-column operating current, average	I_{CC4}		480		400		320	mA	$\overline{RAS} = \overline{CS} = V_{IL}$; addresses cycling; $t_{RSC} = t_{RSC}$ min or $t_{WSC} = t_{WSC}$ min (Note 5)
Static-column read cycle time	t_{RSC}	50		60		70		ns	(Note 6)
Static-column write cycle time	t_{WSC}	50		60		70		ns	(Note 6)
Static-column $\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	120	100000	ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		MC-421000C8-80		MC-421000C8-10		MC-421000C8-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Static-Column Operation (cont)									
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSW}	95		115		135		ns	
Write invalid time	t_{WI}	10		10		10		ns	
Output hold time from address	t_{OH}	5		5		5		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles that are preceded by any cycle.

(14) Specifications for either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, specifications for both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) $\overline{CS}$ before $\overline{RAS}$ operation is specified.

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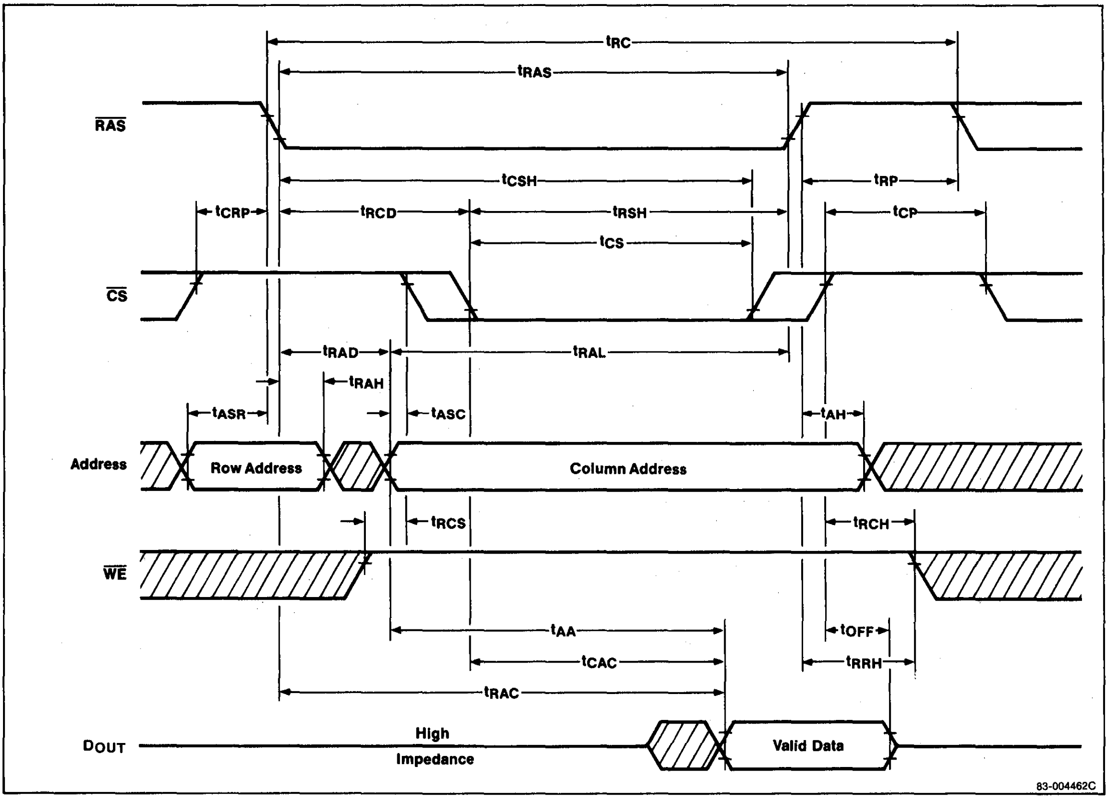
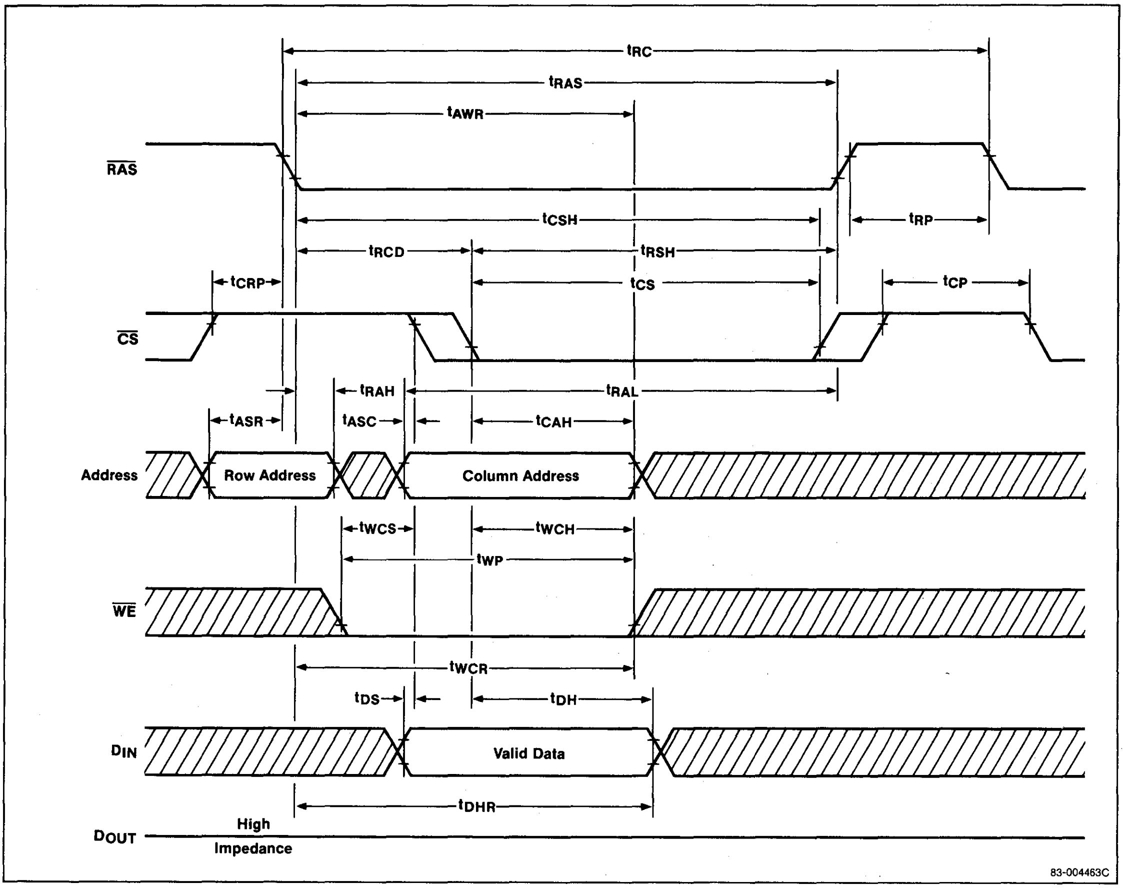
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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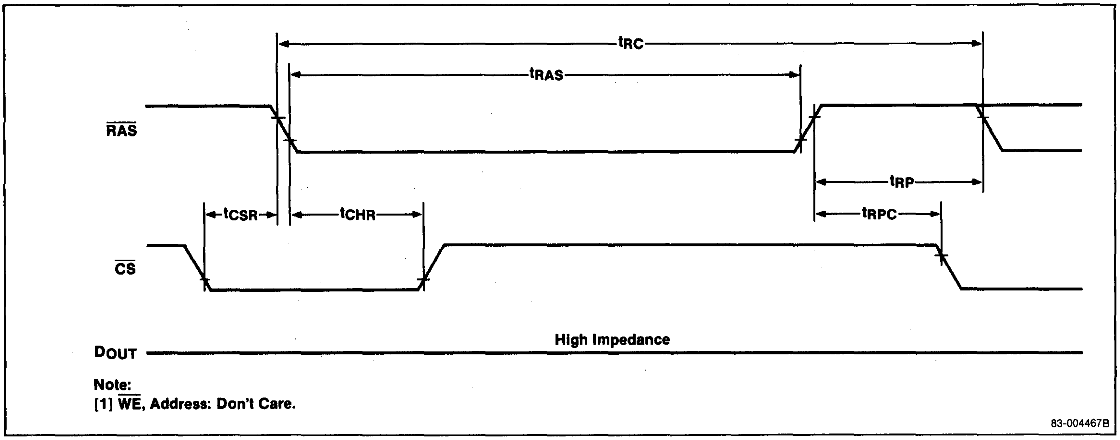
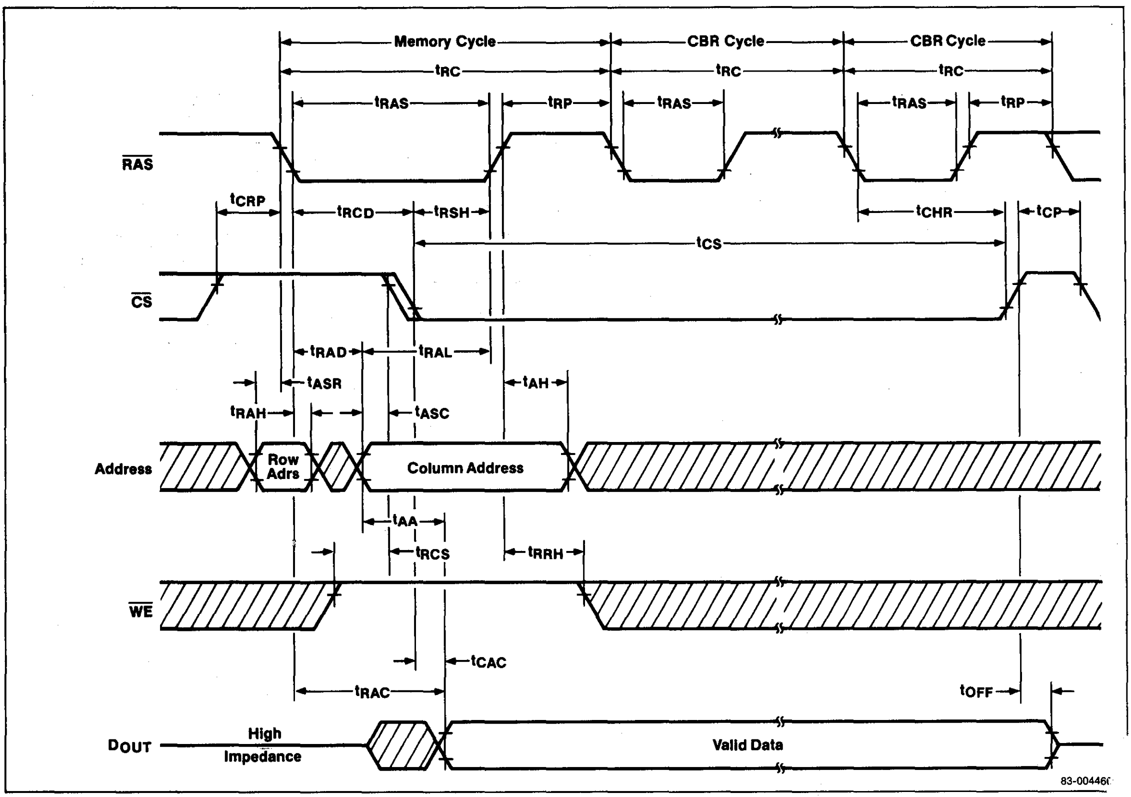
Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

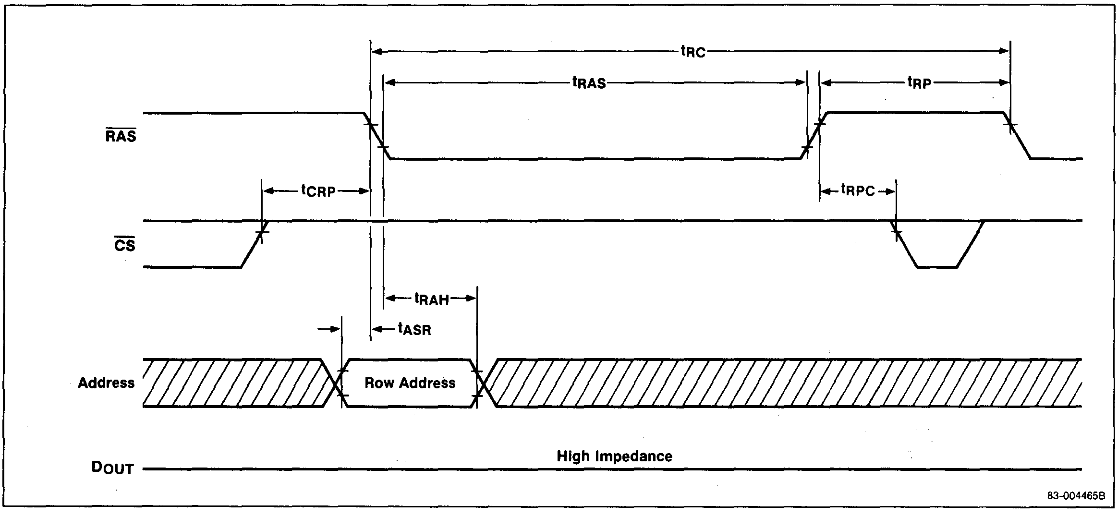


Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



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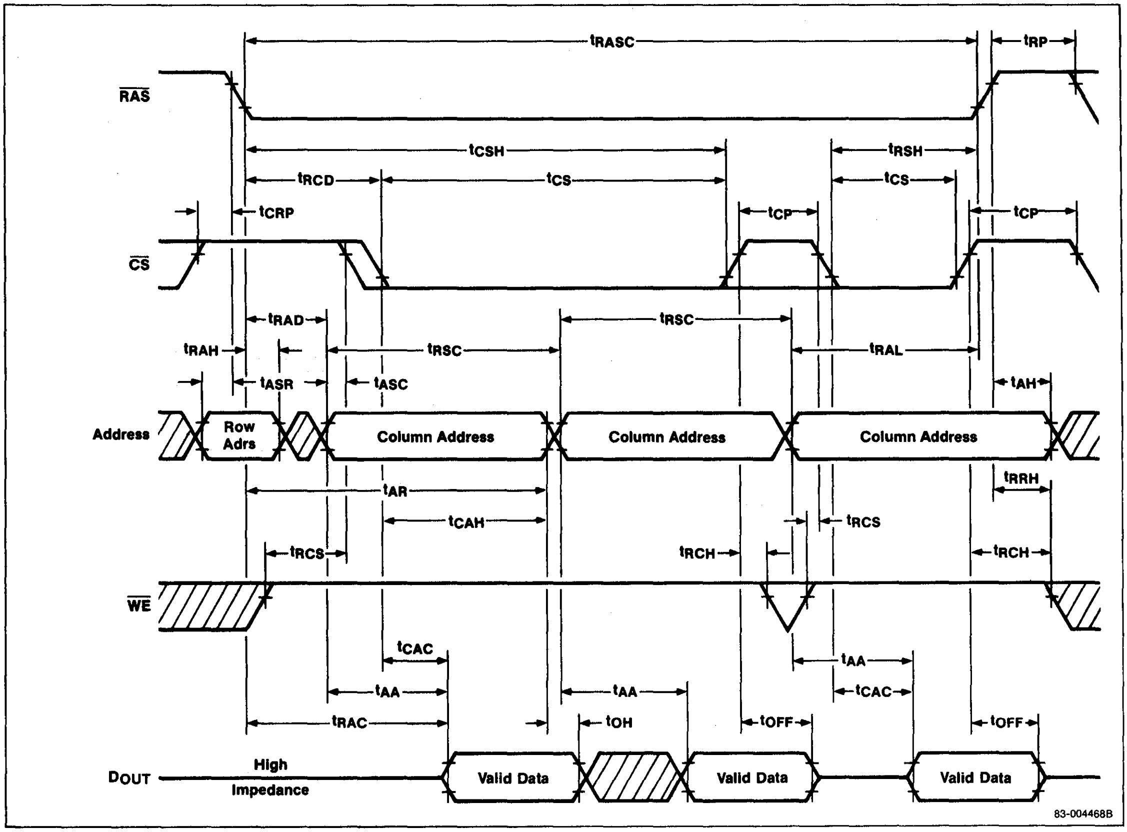
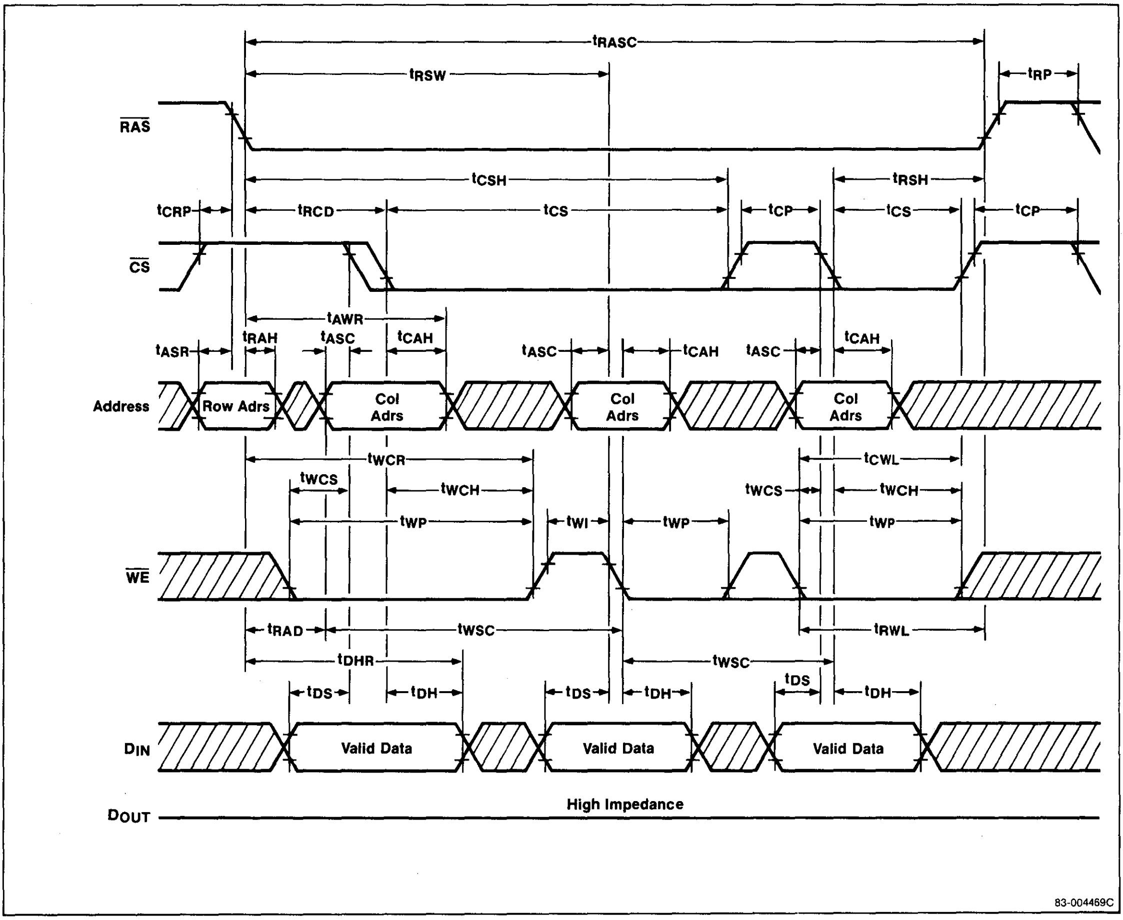
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Write Cycle (Early Write)



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NEC
NEC Electronics Inc.

MC-421000C9
1,048,576 x 9-BIT
CMOS DYNAMIC RAM MODULE

PRELIMINARY INFORMATION

Description

The MC-421000C9 is a static-column 1,048,576-word by 9-bit dynamic RAM module designed to operate from a single +5-volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000C9 is functionally equivalent to eight μPD421002 standard 1M DRAMs plus a parity bit. Refreshing is accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Packaged in a Single Inline Memory Module (SIMM™) to enhance reliability and reduce the size, weight and cost of a system, the MC-421000C9 includes nine μPD421002s in SOJ packages and nine power supply decoupling capacitors.

SIMM is a trademark of Wang Laboratories.

Features

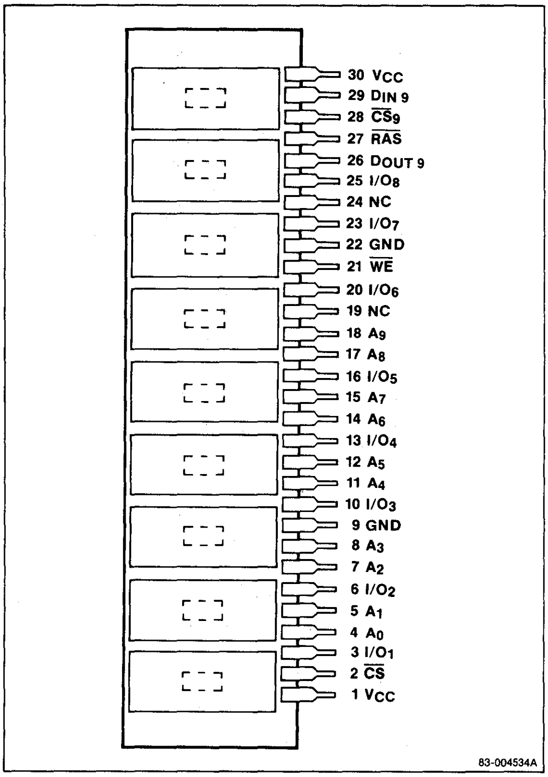
- ☐ 1,048,576-word by 9-bit organization
- ☐ Single +5-volt ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM)
- ☐ Nine 1M dynamic RAMs incorporated in high-density SOJ packaging (μPD421002LA)
- ☐ Nine power supply decoupling capacitors
- ☐ Low power dissipation: 49.5 mW standby (max)
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Static-column capability

Ordering Information

Part Number	Row Access Time (max)	Column Access Time (max)	Address Access Time (max)	Package
MC-421000C9A-80	80 ns	20 ns	45 ns	30-pin leaded SIMM
A-10	100 ns	25 ns	55 ns	
A-12	120 ns	30 ns	65 ns	
MC-421000C9B-80	80 ns	20 ns	45 ns	30-pin socket-able SIMM
B-10	100 ns	25 ns	55 ns	
B-12	120 ns	30 ns	65 ns	

Pin Configurations

30-Pin SIMM, MC-421000C9A



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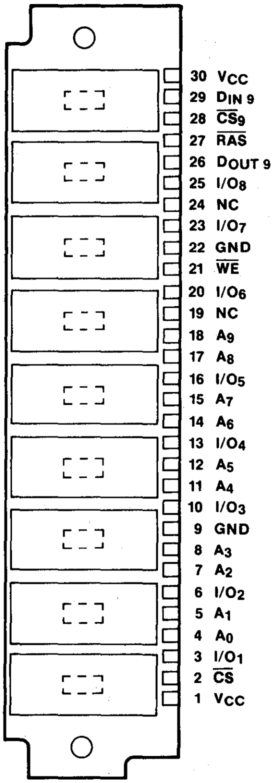
NEC

Pin Configurations (cont)

30-Pin SIMM, MC-421000C9B

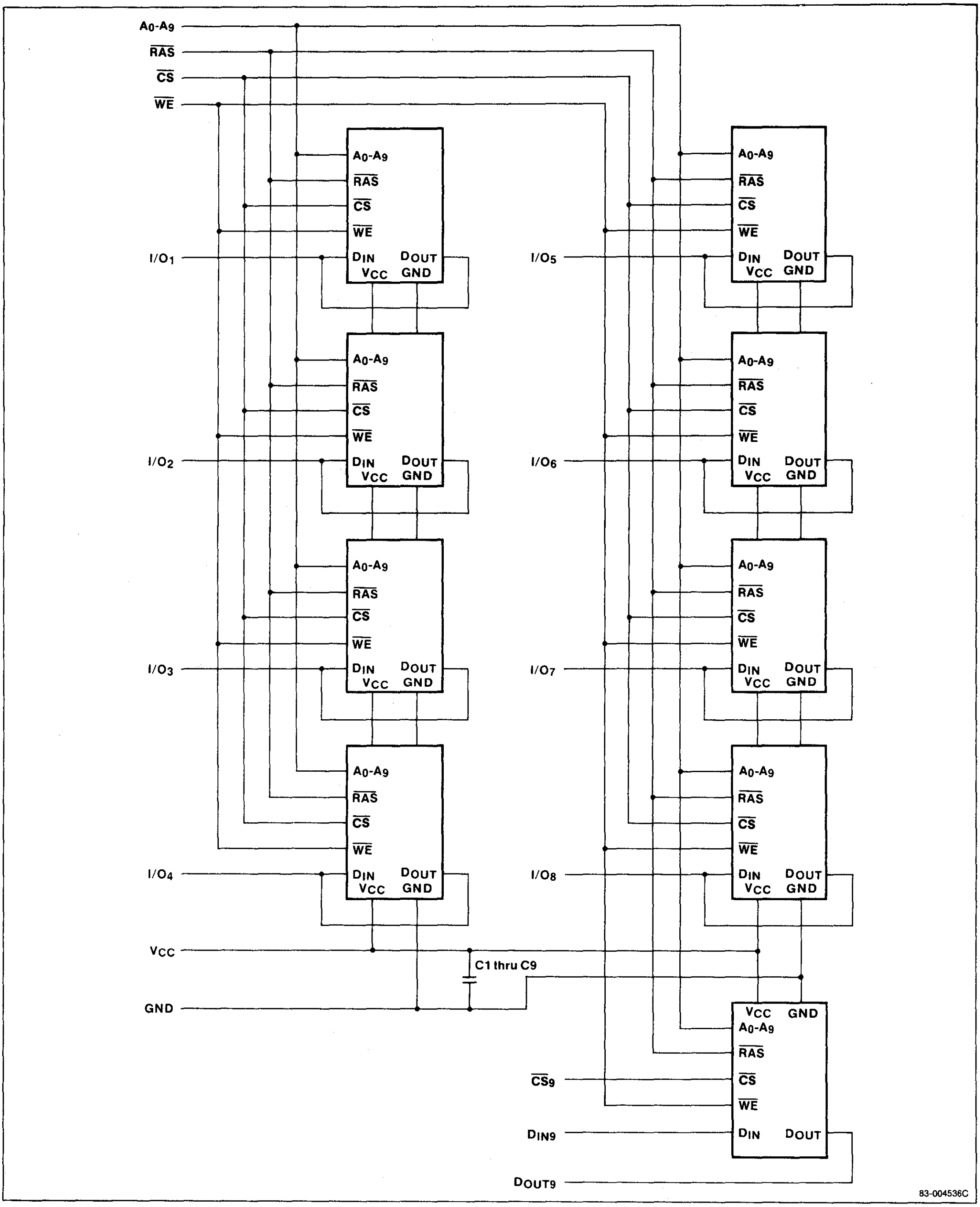


83-004535A

Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$D_{IN\,9}$	Data input 9
$D_{OUT\,9}$	Data output 9
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{CS}_9$	Chip select for data output 9
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	A_0-A_9, $\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
	C_{I2}	7	pF	$\overline{CS}_9$, $D_{IN\,9}$
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8
Output capacitance	C_O	10	pF	$D_{OUT\,9}$

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		$V_{CC} + 1.0$	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			27	mA	$\overline{RAS} = \overline{CS} \geq V_{IH}$
				9	mA	$\overline{RAS} = \overline{CS} \geq V_{CC} - 0.2\ V$
Input leakage current	I_{IL}	−90		90	µA	For A_0-A_9, $\overline{RAS}$, $\overline{CS}$, $\overline{WE}$: $V_{IN} = 0$ to 5.5 V; other pins = 0 V
	I_{IL9}	−10		10	µA	For $\overline{CS}_9$ and $D_{IN\,9}$: $V_{IN} = 0$ to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	µA	For I/O_1-I/O_8 and $D_{OUT\,9}$: D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000C9-80		MC-421000C9-10		MC-421000C9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		630		540		450	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		630		540		450	mA	$\overline{RAS}$ cycling; $\overline{CS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		630		540		450	mA	$t_{RC} = t_{RC}$ min; $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Notes 6, 19)
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CS}$	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 11)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CS}$ pulse width	t_{CS}	20	100000	25	100000	30	100000	ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 12)
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 13)
$\overline{CS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		120		ns	

AC Characteristics (cont)

$T_A = 0$ to $+70\,°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		MC-421000C9-80		MC-421000C9-10		MC-421000C9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{\text{RAS}}$ to column address hold time	t_{AH}	15		15		15		ns	
Column address lead time referenced to $\overline{\text{RAS}}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	10		10		10		ns	(Note 14)
Read command hold time referenced to $\overline{\text{CS}}$	t_{RCH}	0		0		0		ns	(Note 14)
Column address hold time referenced to $\overline{\text{RAS}}$ (write cycle)	t_{AWR}	60		70		85		ns	
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 15)
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{\text{CS}}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 16)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 16)
Data-in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 17)
$\overline{\text{CS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	20		25		30		ns	(Notes 17, 19)
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	80		100		120		ns	(Notes 17, 19)
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	45		50		60		ns	(Notes 17, 19)
Output hold time from $\overline{\text{WE}}$	t_{OHW}	10		10		10		ns	
$\overline{\text{CS}}$ setup time for $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refreshing	t_{CSR}	10		10		10		ns	(Note 18)
$\overline{\text{CS}}$ hold time for $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refreshing	t_{CHR}	15		20		25		ns	(Note 18)

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		MC-421000C9-80		MC-421000C9-10		MC-421000C9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Static-Column Operation									
Static-column operating current, average	I_{CC4}		540		450		360	mA	$\overline{RAS} = \overline{CS} \leq V_{IL}$; addresses cycling; $t_{RSC} = t_{RSC}$ min or $t_{WSC} = t_{WSC}$ min; I_O = 0 mA (Note 5)
Static-column read cycle time	t_{RSC}	50		60		70		ns	(Note 6)
Static-column write cycle time	t_{WSC}	50		60		70		ns	(Note 6)
Static-column read-write cycle time	t_{RWSC}	95		115		135		ns	(Notes 6, 19)
Access time from previous $\overline{WE}$ (falling edge)	t_{PWA}		90		110		130	ns	(Notes 7, 19, 20)
Static-column $\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSW}	95		115		135		ns	
Previous $\overline{WE}$ (falling edge) to column address delay time	t_{WAD}	20	45	25	55	25	65	ns	(Notes 19, 20)
Column address hold time from previous $\overline{WE}$ (falling edge)	t_{PWH}	90		110		130		ns	(Note 19)
Write invalid time	t_{WI}	10		10		10		ns	
Output hold time from address	t_{OH}	5		5		5		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100µs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles that are preceded by any cycle.

(14) Specifications for either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, specifications for both t_{WCS} and t_{WCH} must be met.

(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) For $D_{OUT\ 9}$, parameters t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\ 9}$ (at access time and until $\overline{CS}_9$ returns to V_{IH}) is indeterminate.

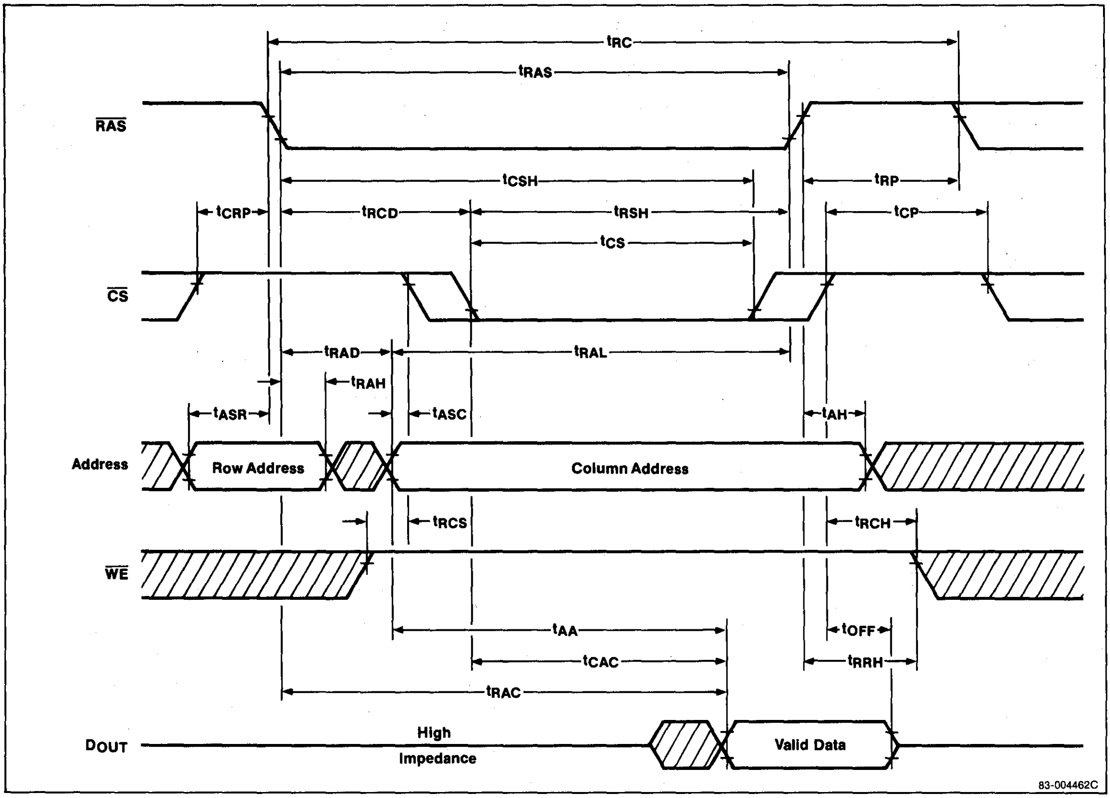
(18) $\overline{CS}$ before $\overline{RAS}$ operation is specified.

(19) A read-write/read-modify-write operation can be performed only by the SOJ controlled by $\overline{CS}_9$ because of its separate data input and output pins.

(20) If $t_{WAD} \leq t_{WAD}$ (max), then the access time is defined by t_{PWA}.

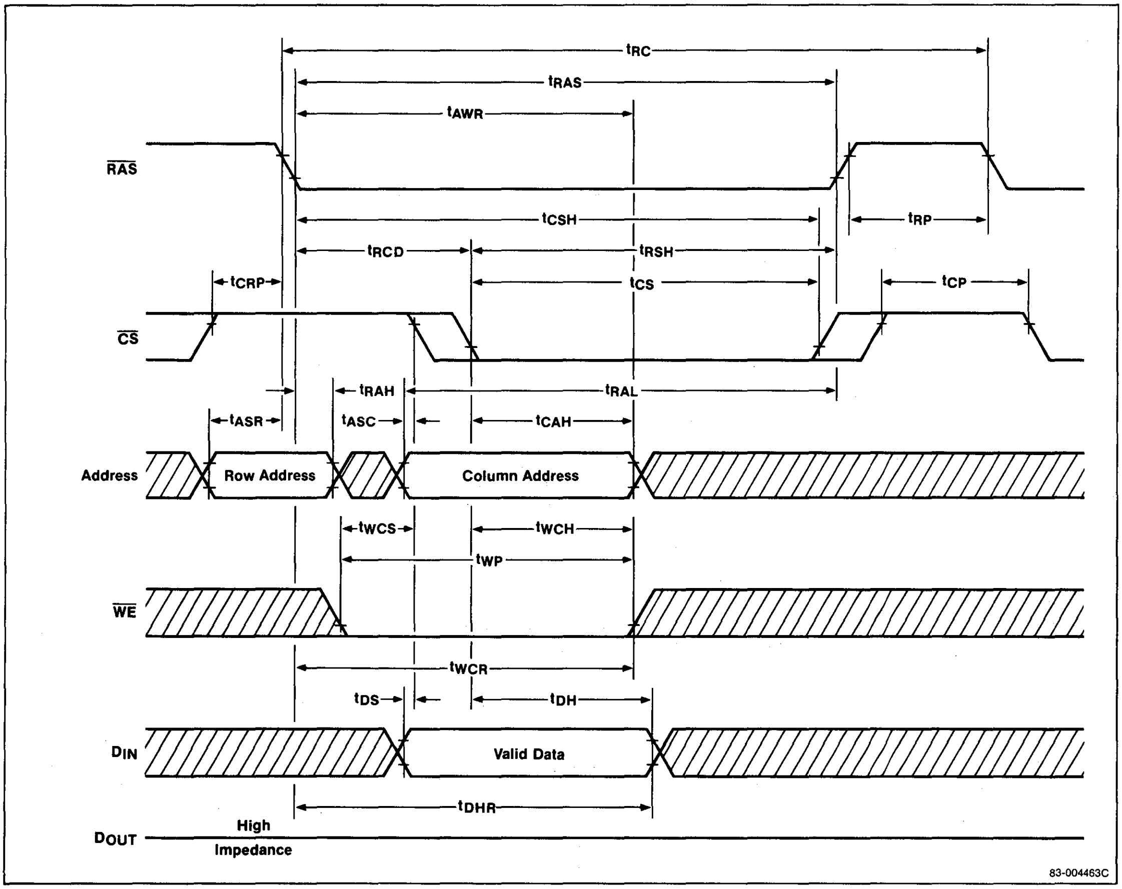
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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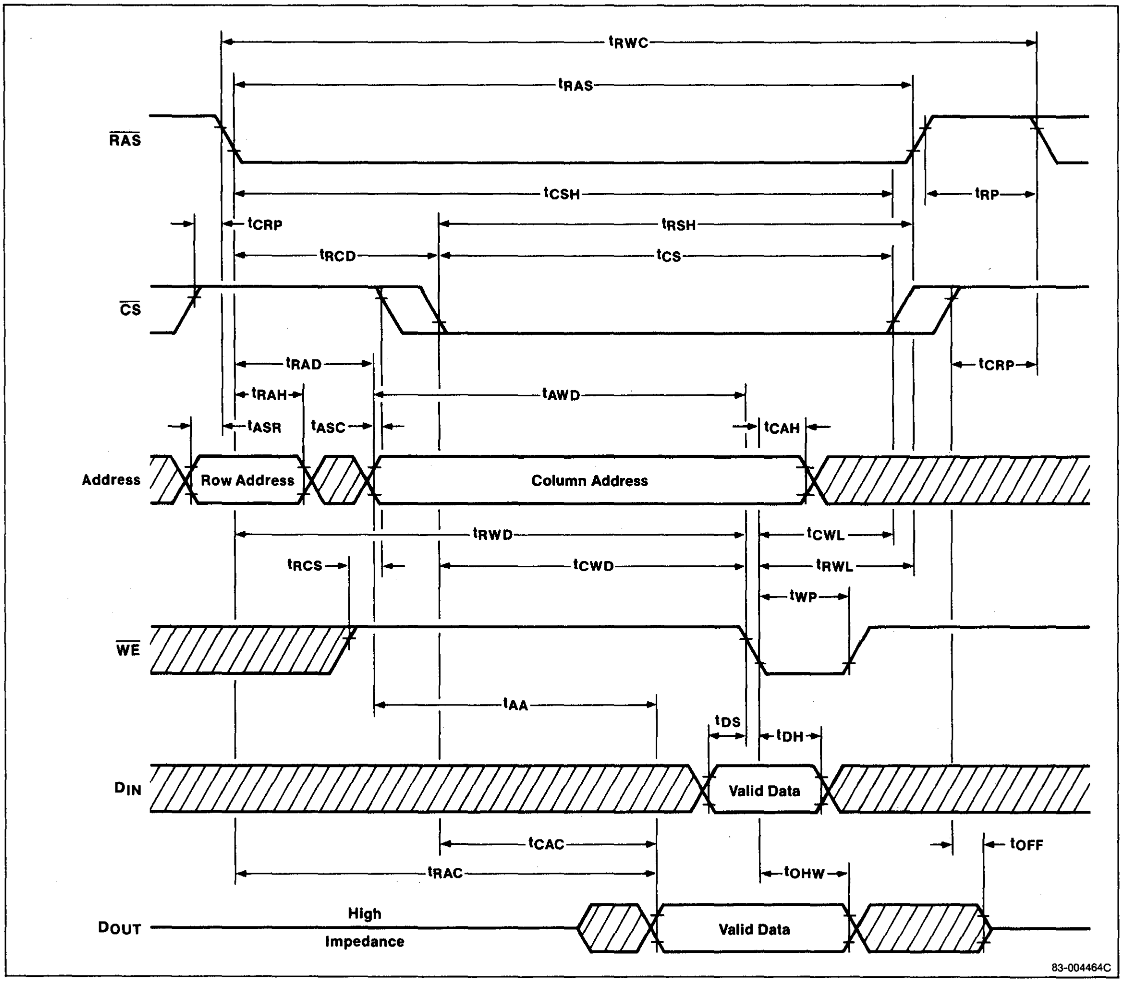
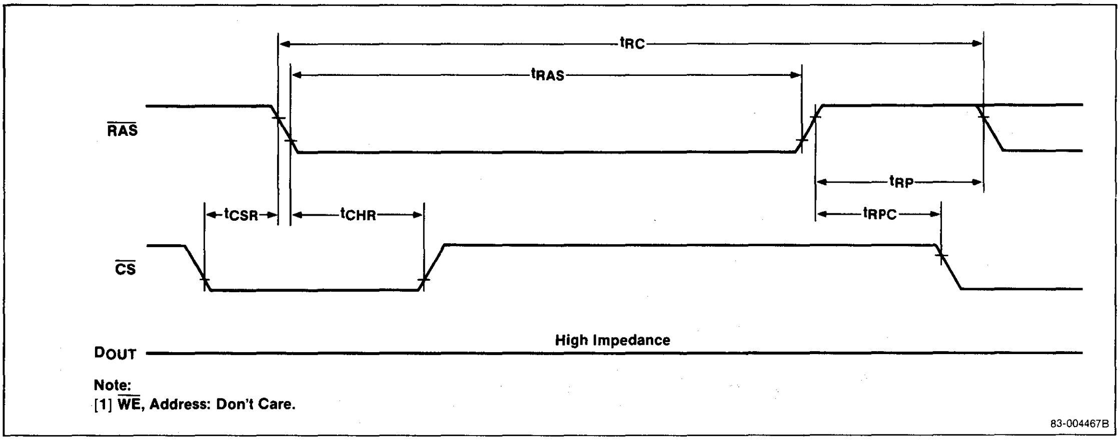
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle ($D_{OUT\,9}$ only)

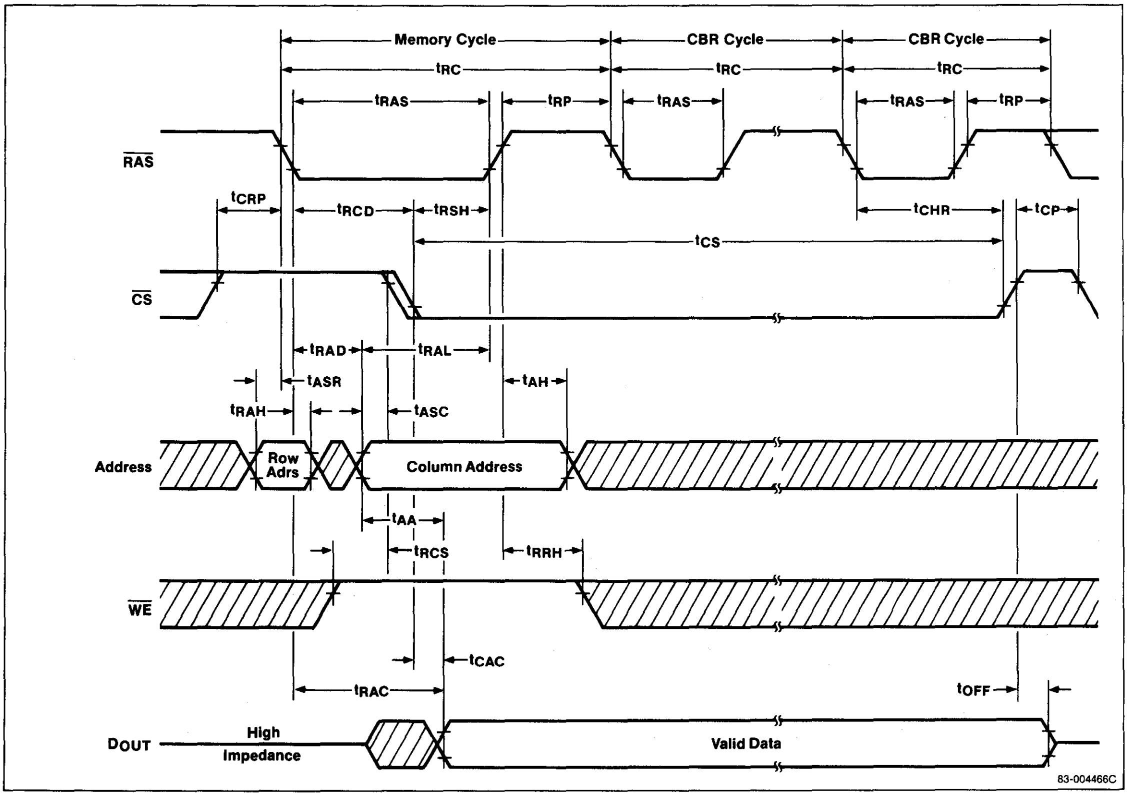


Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

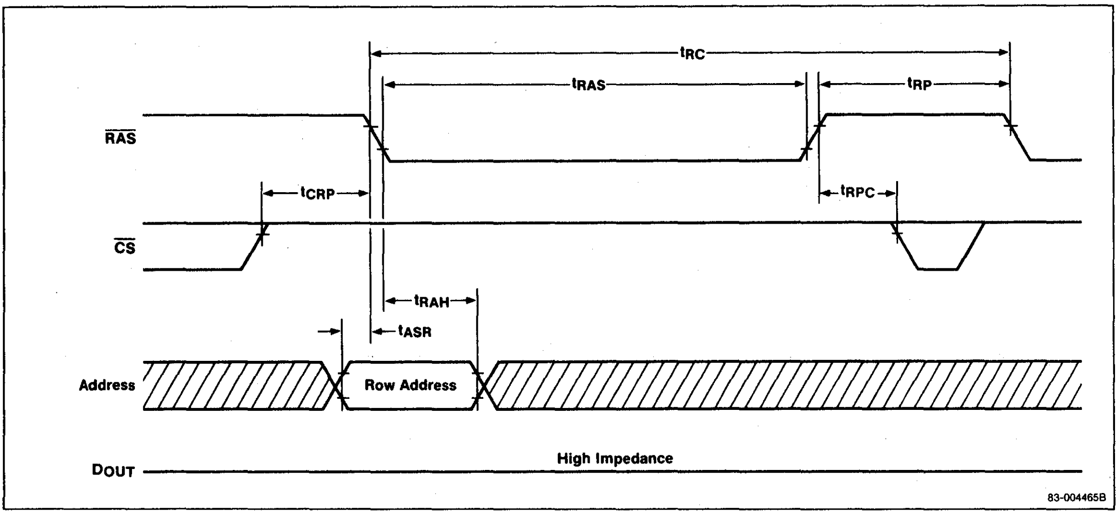


Hidden Refresh Cycle



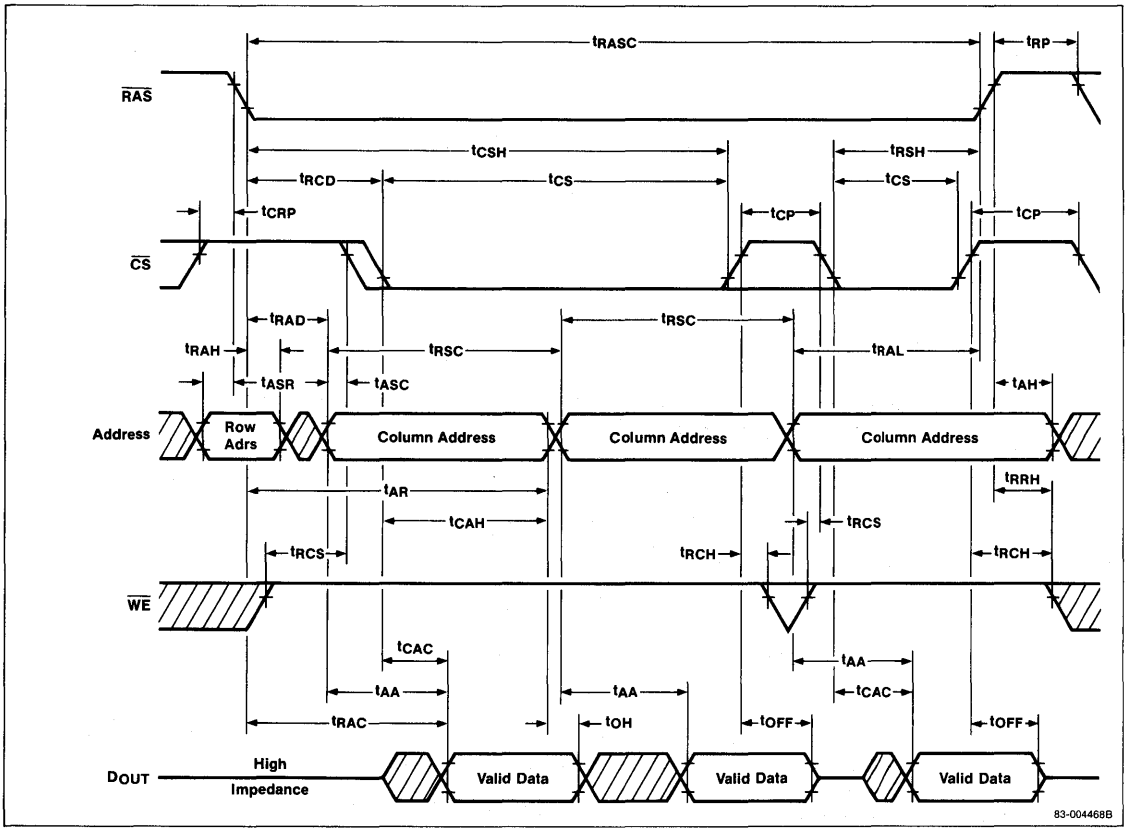
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



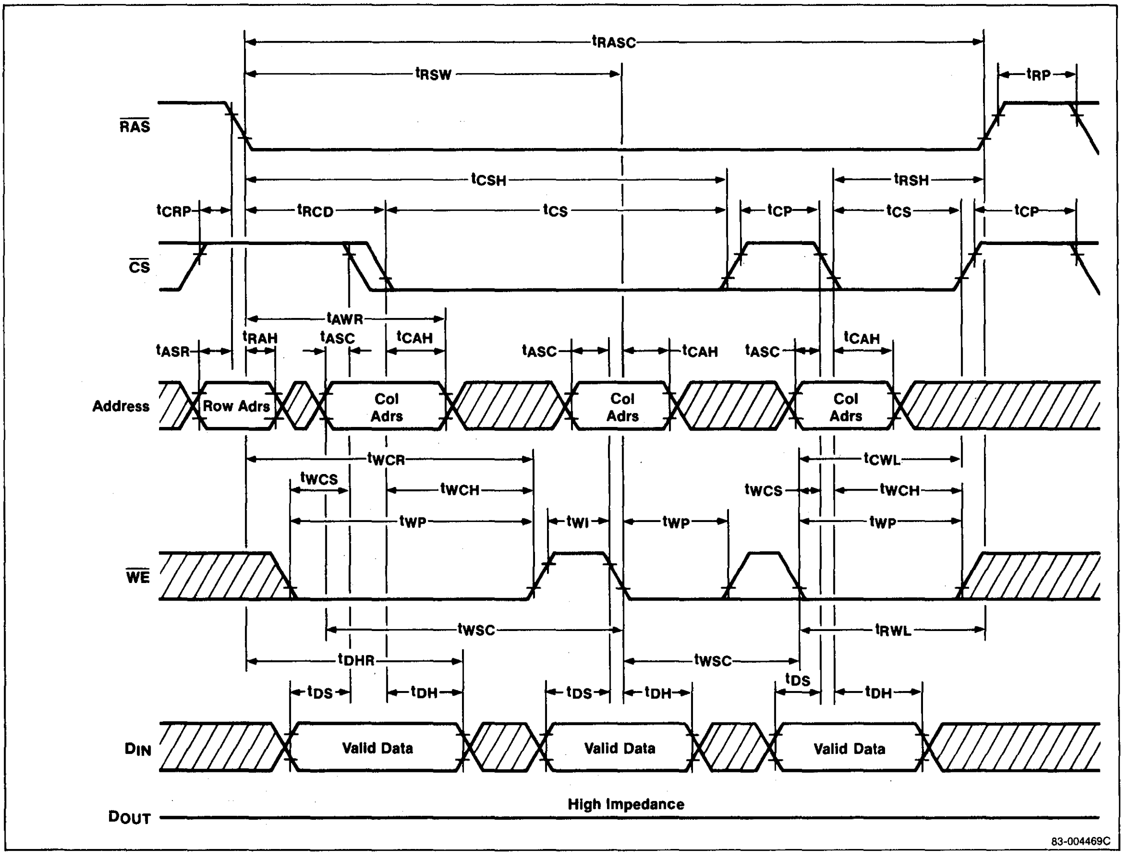
Timing Waveforms (cont)

Static-Column Read Cycle



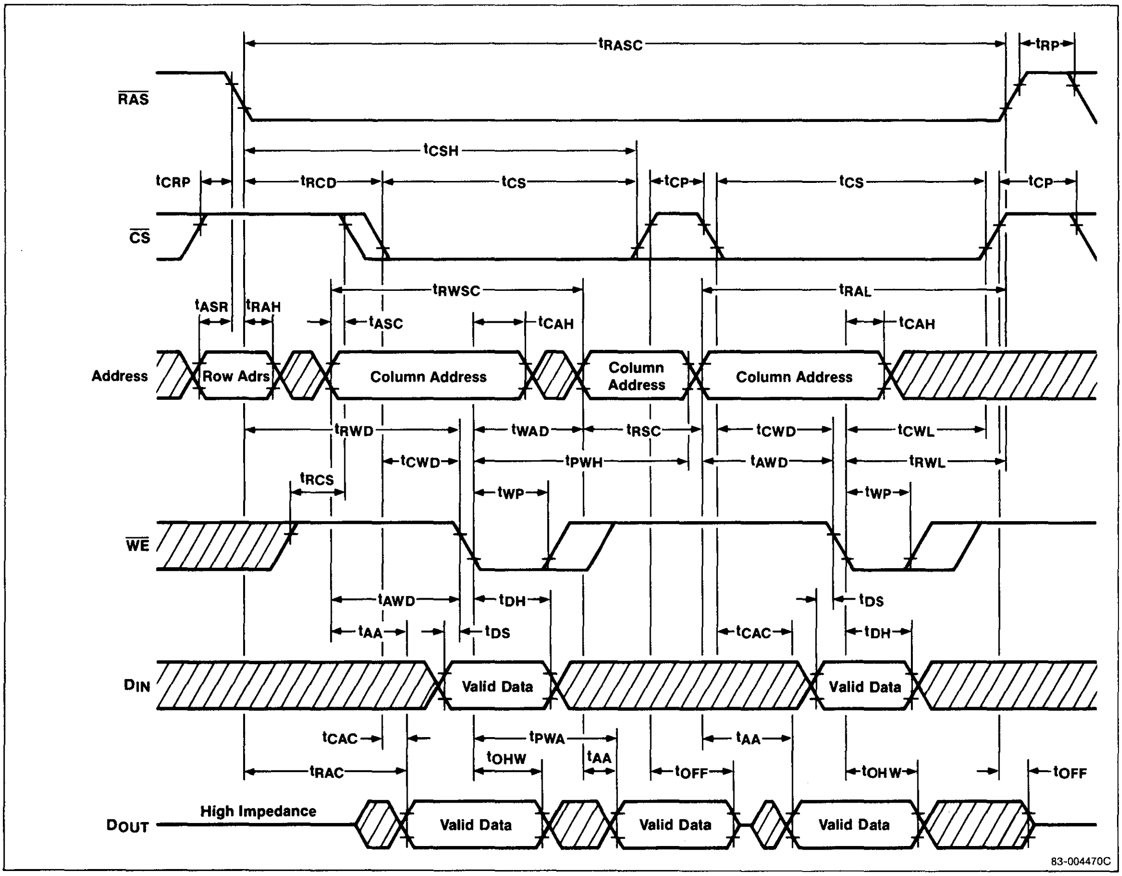
Timing Waveforms (cont)

Static-Column Write Cycle (Early Write)



Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle ($D_{OUT\,9}$ only)



4

NEC

DYNAMIC RAMs

5

NEC

Section 5
Dynamic RAMs

NEC
NEC Electronics Inc.

μPD41256
262,144 x 1-BIT
DYNAMIC NMOS RAM

Description

The μPD41256 is a 262,144-word by 1-bit dynamic NMOS RAM designed to operate from a single +5-volt power supply. The negative voltage substrate bias is automatically generated internally.

The μPD41256 is fabricated with double polylayer, N-channel, silicon-gate processing to provide high storage cell density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, ensure that power dissipation is minimized.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{\text{CAS}}$ low. The data output then is returned to high impedance by returning $\overline{\text{CAS}}$ high. A hidden refresh feature allows $\overline{\text{CAS}}$ to be held low to maintain output data while $\overline{\text{RAS}}$ is used to execute refresh cycles.

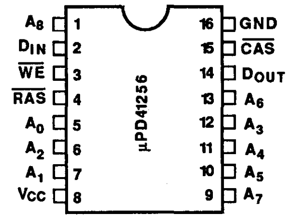
Refreshing is accomplished by means of $\overline{\text{RAS}}$-only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4-ms period.

Features

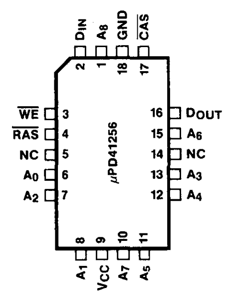
- ☐ 262,144-word x 1-bit organization
- ☐ High-density plastic DIP and PLCC packaging
- ☐ Multiplexed address inputs
- ☐ Single +5-volt ±10% power supply
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation: 28 mW standby (max)
- ☐ Nonlatched, three-state outputs
- ☐ Fully TTL-compatible inputs and outputs
- ☐ Low input capacitance
- ☐ 256 refresh cycles (A_0-A_7 are refresh address pins)
- ☐ Page-mode operation
- ☐ $\overline{\text{RAS}}$-only refresh, hidden refresh, and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles

Pin Configurations

16-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



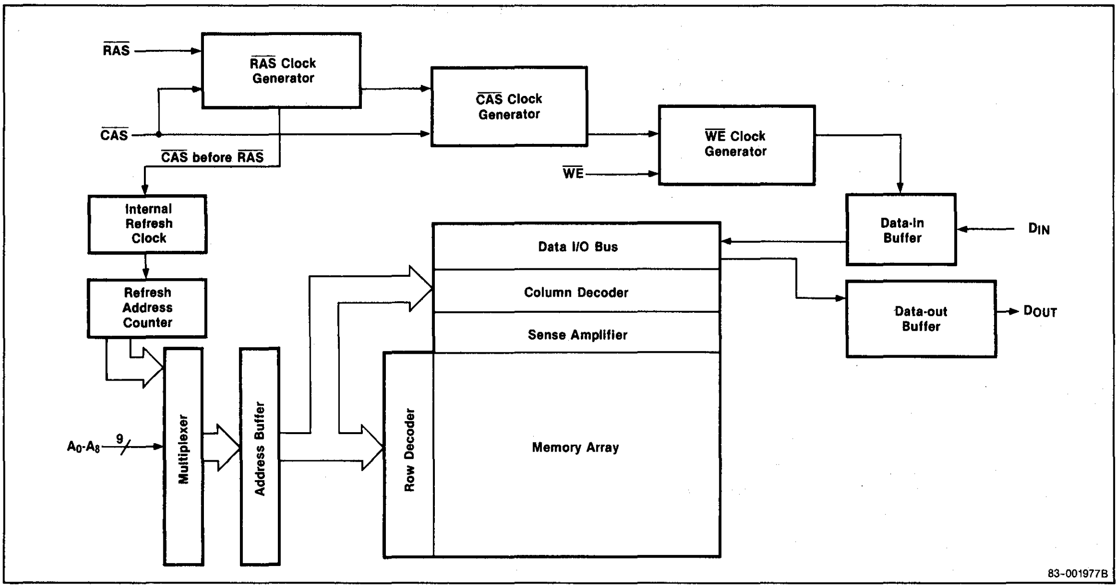
Ordering Information

Part Number	Access Time (max)	R/W Cycle (min)	Page Cycle (min)	Package
μPD41256C-10	100 ns	200 ns	100 ns	16-pin plastic DIP
C-12	120 ns	220 ns	120 ns	
C-15	150 ns	260 ns	145 ns	
μPD41256L-10	100 ns	200 ns	100 ns	18-pin plastic leaded chip carrier
L-12	120 ns	220 ns	120 ns	
L-15	150 ns	260 ns	145 ns	

Pin Identification

Symbol	Function
A_0-A_8	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CAS}$	Column address strobe
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	−1.0 to +7.0 V
Operating temperature, T_A (ambient)	0 to 70°C
Storage temperature, T_{STG}	−55 to 125°C
Power dissipation, P_D	1.0 W
Short-circuit output current, I_{OS}	50 mA

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1.0 MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_{I1}			5	pF	A_0-A_8, D_{IN}
	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_{OUT}			7	pF	D_{OUT}

DC Characteristics

T_A = 0 to 70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby supply current	I_{CC2}			5.0	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA
Input voltage, low	V_{IL}	−1.0		0.8	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	

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AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

		Limits							
		μPD41256-10		μPD41256-12		μPD41256-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating supply current, average	I_{CC1}		80		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); $I_O = 0$ mA (Note 5)
Operating supply current, $\overline{RAS}$-only refresh, average	I_{CC3}		65		60		50	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ (min); $I_O = 0$ mA (Note 5)
Operating supply current, page mode, average	I_{CC4}		60		50		40	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min); $I_O = 0$ mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh, average	I_{CC5}		65		60		50	mA	$\overline{CAS} = V_{IL}$; $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); $I_O = 0$ mA (Note 5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	240		265		310		ns	(Note 6)
Page-mode cycle time	t_{PC}	100		120		145		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	25	0	30	0	35	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		20		20		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		Limits							
		μPD41256-10		μPD41256-12		μPD41256-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	25		30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Refresh period	t_{REF}		4		4		4	ms	
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	50		60		75		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	100		120		150		ns	(Note 15)
$\overline{CAS}$ setup time for CBR refresh	t_{CSR}	10		10		10		ns	(Note 16)
$\overline{CAS}$ hold time for CBR refresh	t_{CHR}	20		30		30		ns	(Note 16)
Read or write cycle time (counter test cycle)	t_{TRC}	220		250		285		ns	(Note 18)
Read-write cycle time (counter test cycle)	t_{TRWC}	260		295		335		ns	(Note 18)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to 70°C) is assured.

(7) Output load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

(16) DIP products with process codes E, K, and P do not have the $\overline{CAS}$ before $\overline{RAS}$ refresh feature. All other package types and process codes do have $\overline{CAS}$ before $\overline{RAS}$ refreshing.

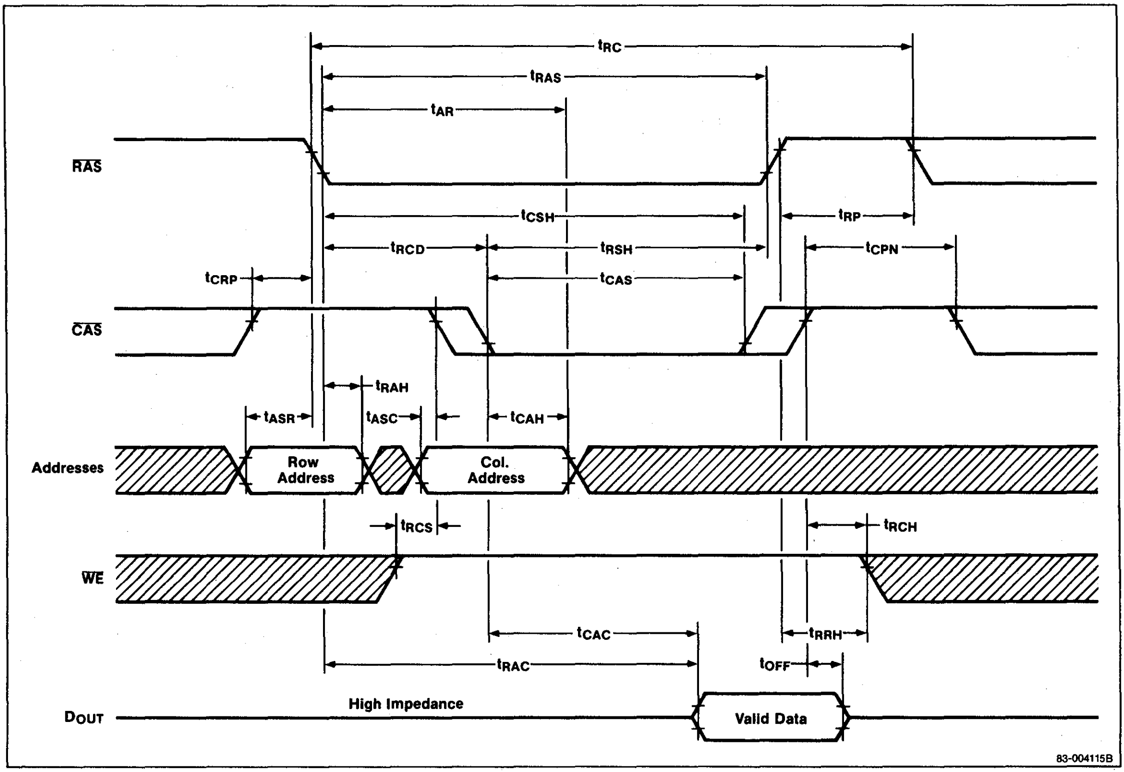
On DIP products with process codes E, K, and P, the external address inputs are required in hidden refresh cycles and the address timing must satisfy t_{ASR} and t_{RAH}, which are specified with respect to the falling edge of $\overline{RAS}$.

(17) t_{WP} is applicable for a delayed write cycle. If the cycle is early write, it should be satisfied with the specified value of t_{WCH}.

(18) t_{TRC} and t_{TRWL} are applicable for a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle.

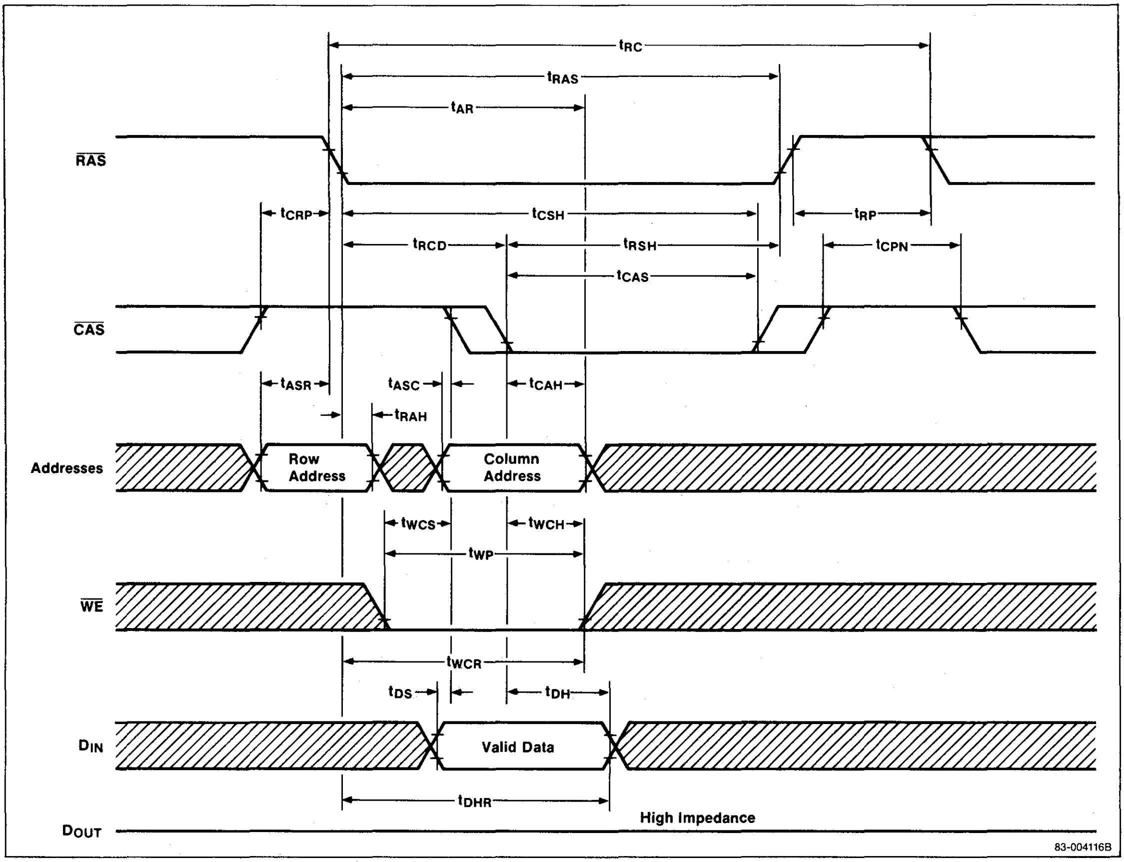
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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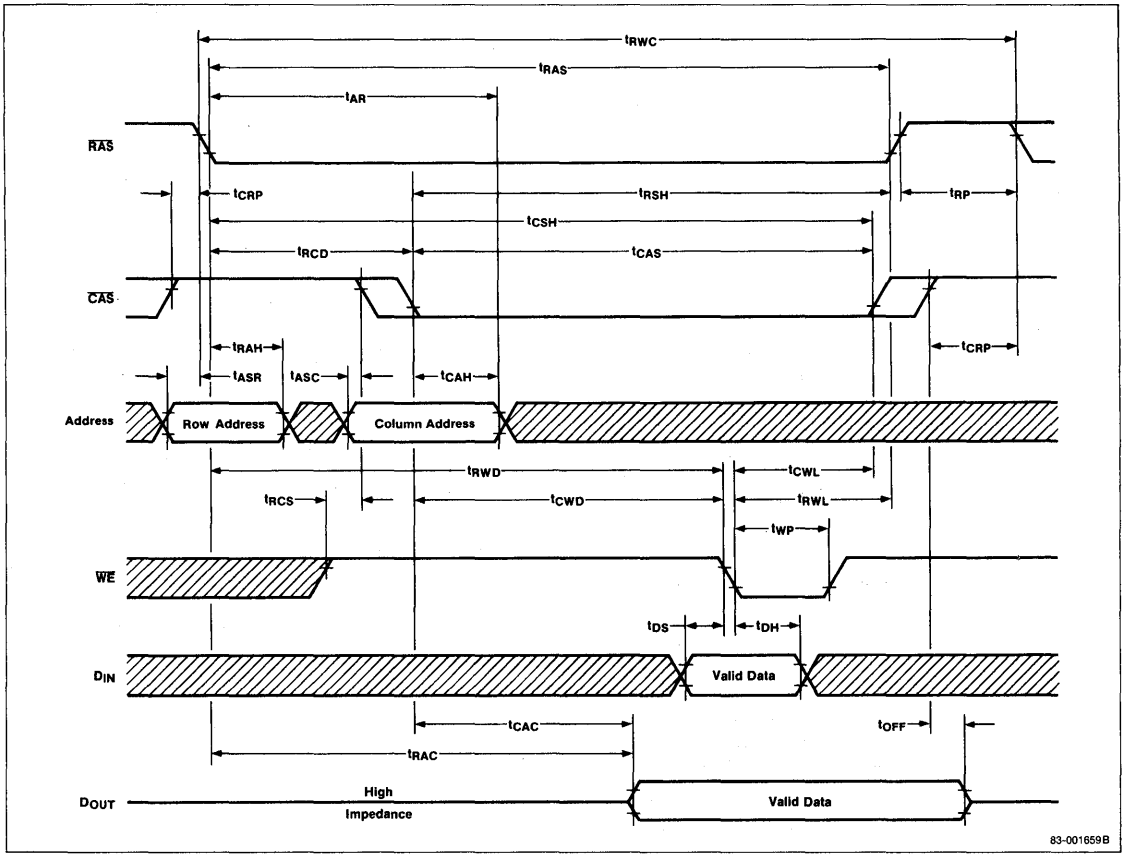
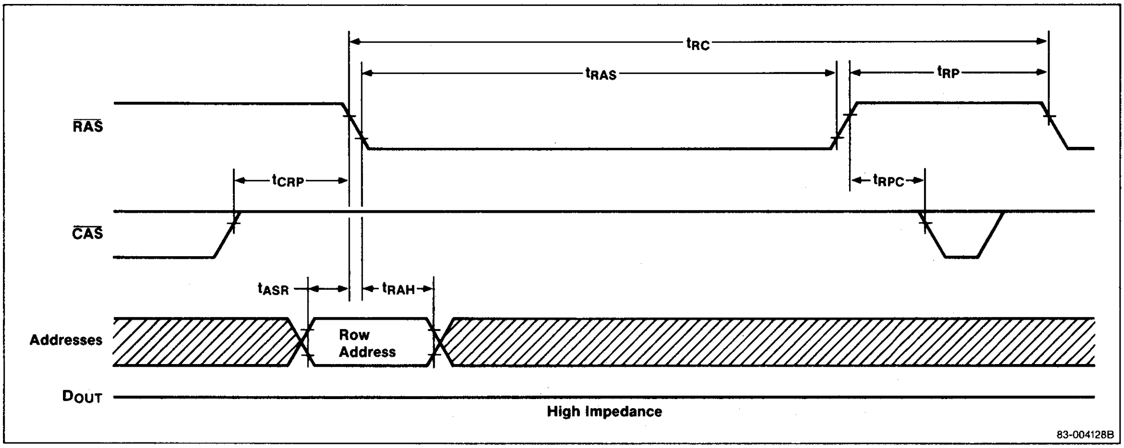
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

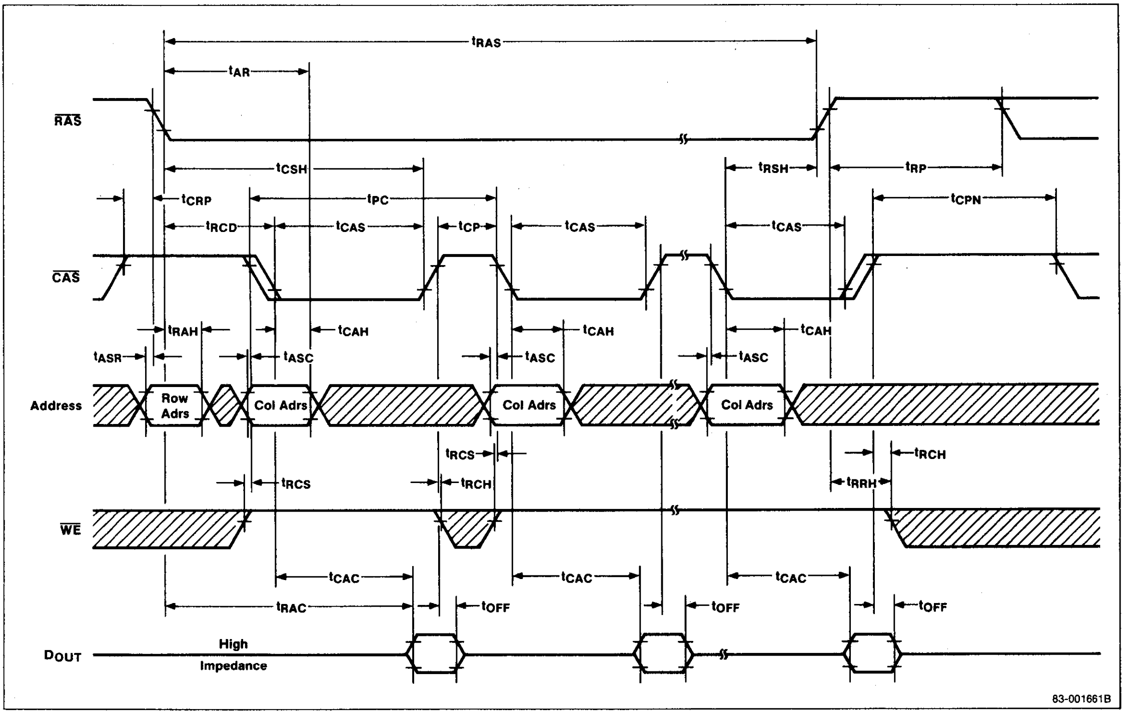


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Page-Mode Read Cycle



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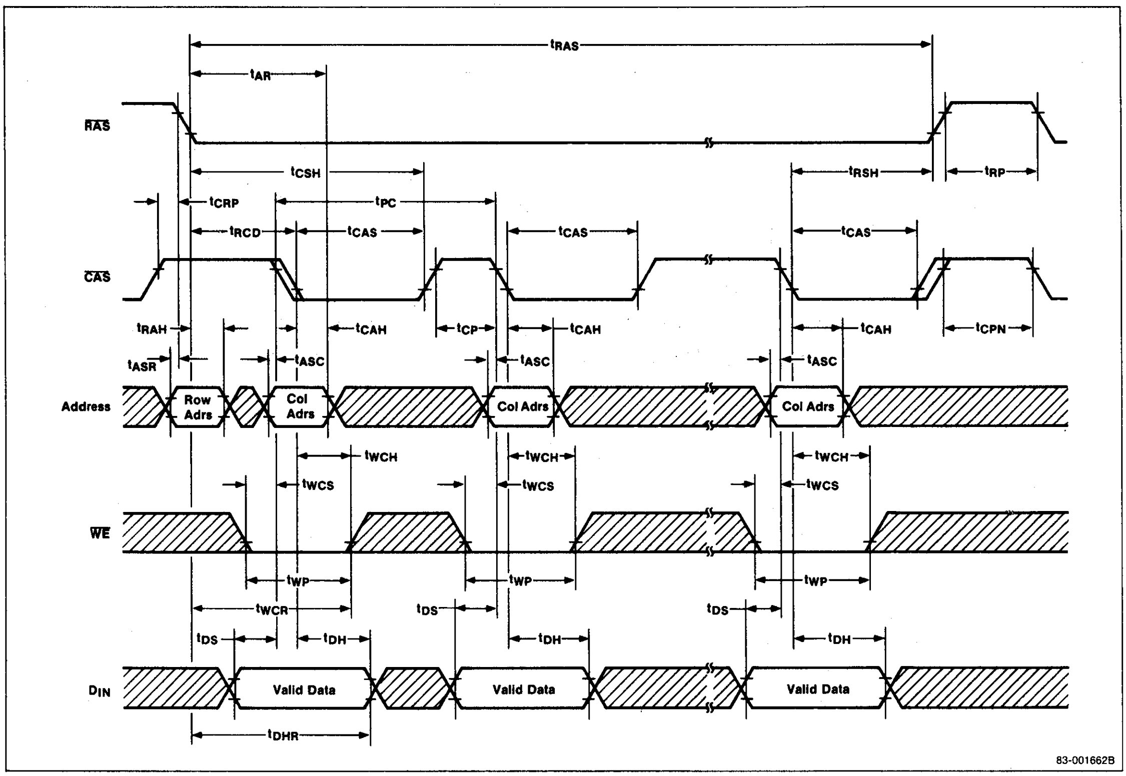
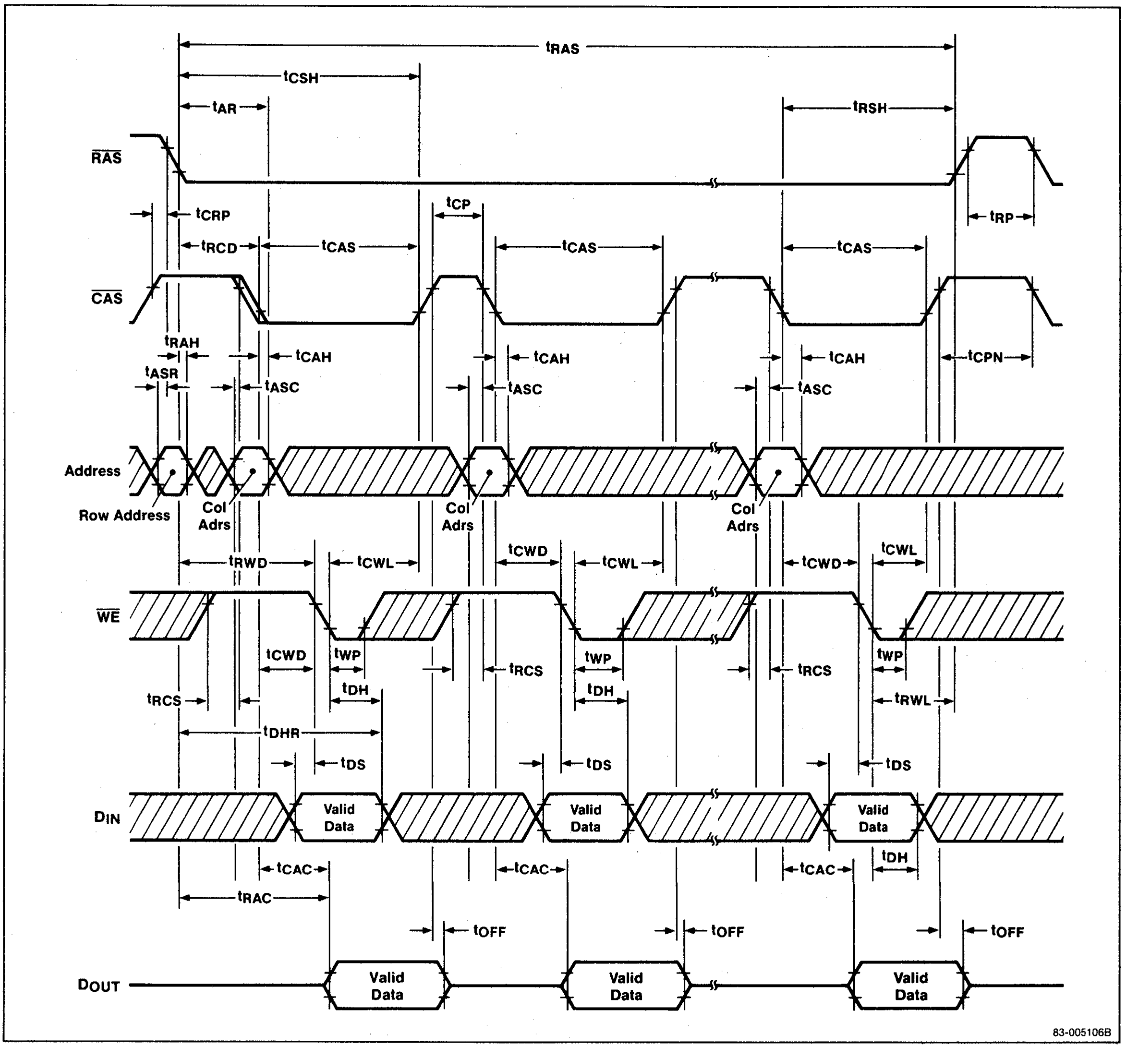
Timing Waveforms (cont)

Page-Mode Write Cycle (Early Write)



Timing Waveforms (cont)

Page-Mode Read-Write/Read-Modify-Write Cycle



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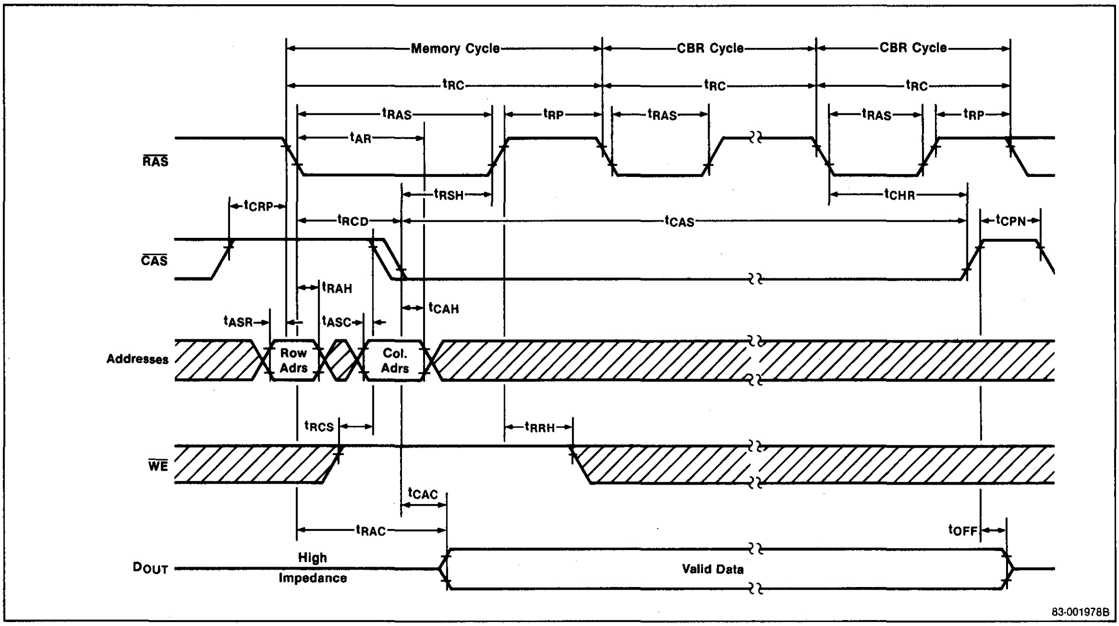
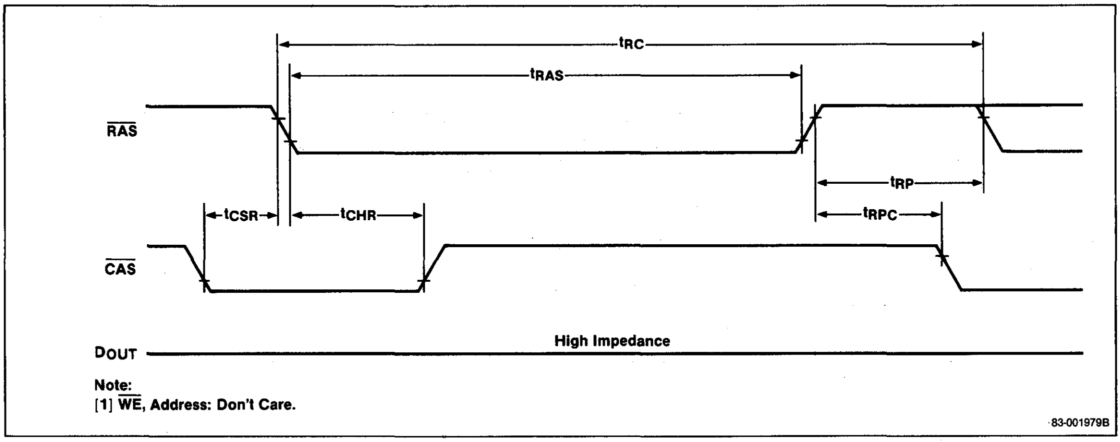
Timing Waveforms (cont)

Hidden Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

The μPD41256 provides a method to verify proper operation of the internal address counter used in $\overline{CAS}$ before $\overline{RAS}$ refreshing. After a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is initiated, $\overline{CAS}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{RAS}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{CAS}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{RAS}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{CAS}$ before $\overline{RAS}$ refresh counter test write cycles. Use the same column address in each cycle.

(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.

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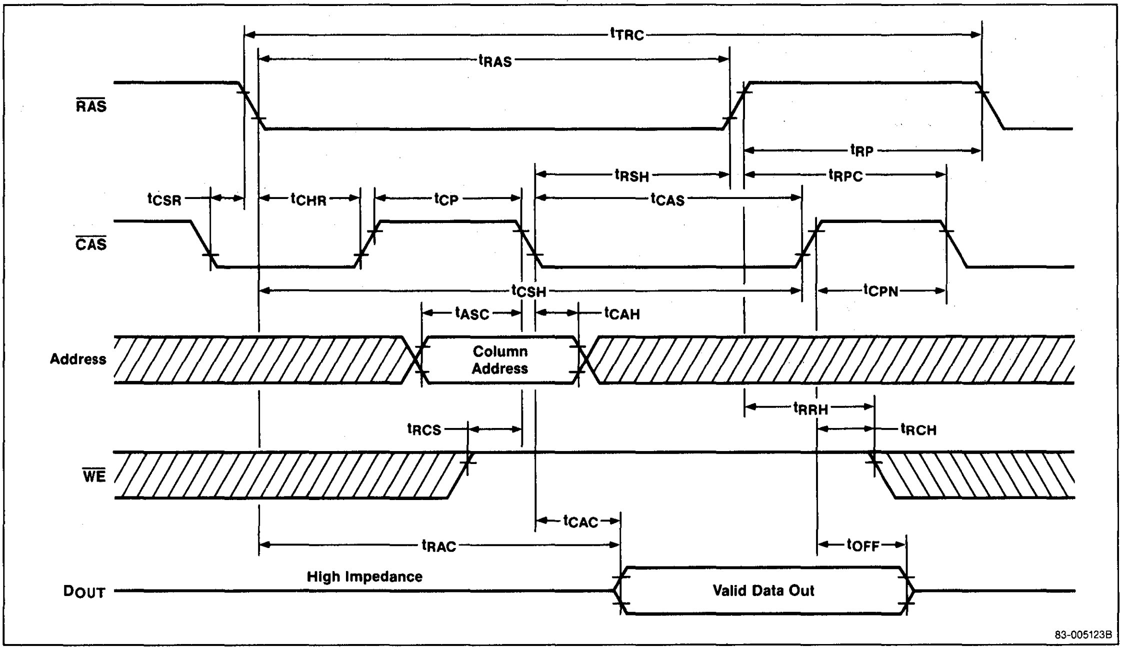
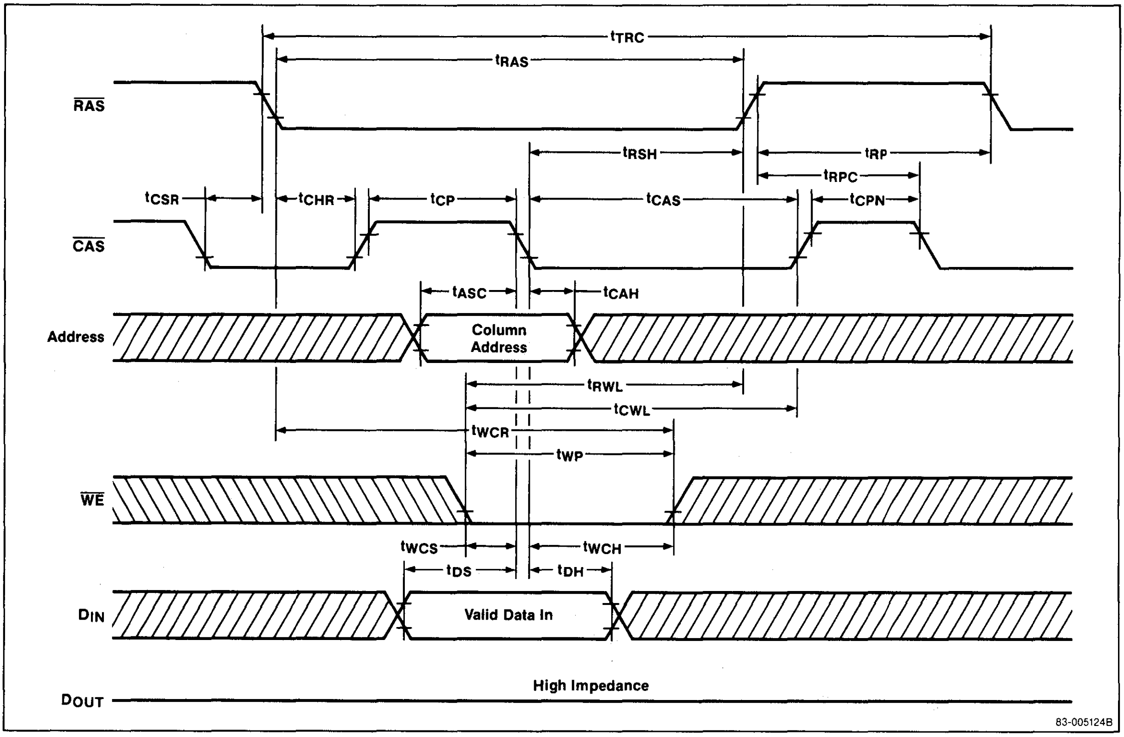
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle



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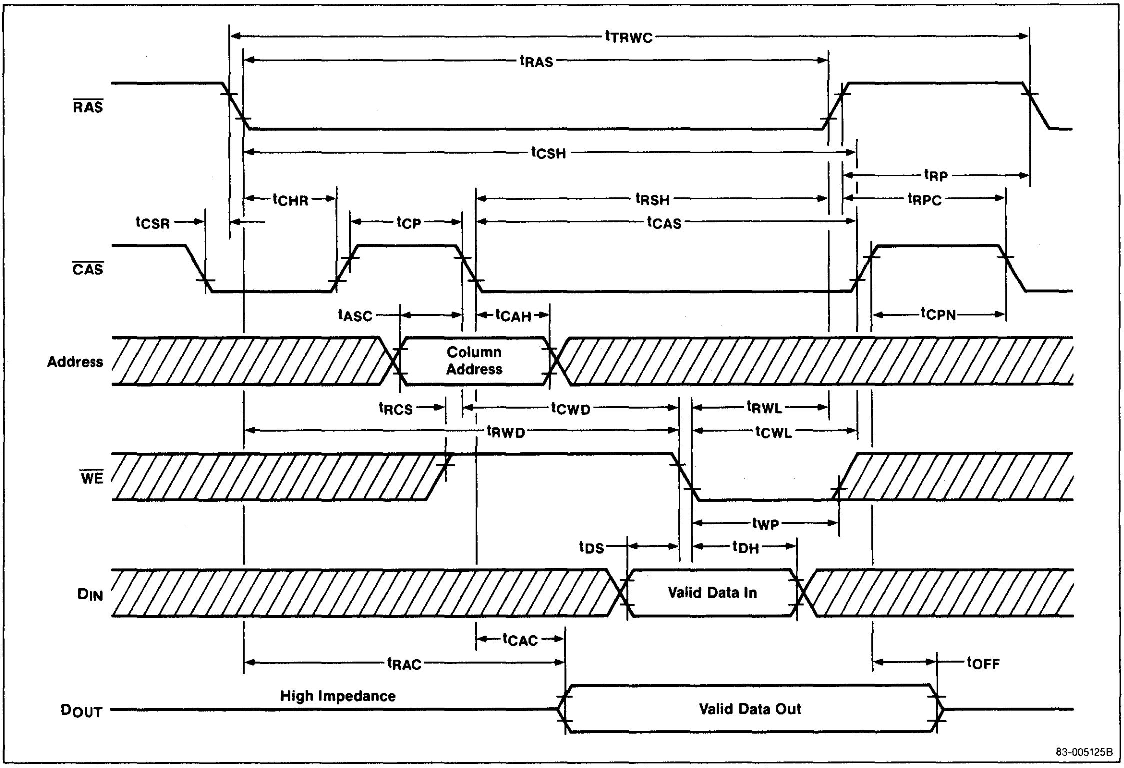
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



NEC
NEC Electronics Inc.

μPD41257 262,144 x 1-BIT DYNAMIC NMOS RAM

Description

The μPD41257 is a 262,144-word by 1-bit dynamic NMOS RAM designed to operate from a single +5-volt power supply. A double-polylayer N-channel silicon gate fabrication process provides for high storage cell density, high performance, and high reliability.The device also uses a single-transistor dynamic storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, which ensure that power dissipation is minimized. The negative voltage substrate bias is automatically generated internally.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. Nibble mode read or write cycles are available by cycling $\overline{CAS}$.

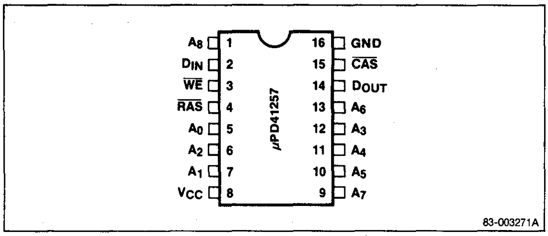
Refreshing is initiated by a $\overline{CAS}$ before $\overline{RAS}$ cycle that enables internal generation of the refresh address. Refreshing is also accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4-ms period.

Features

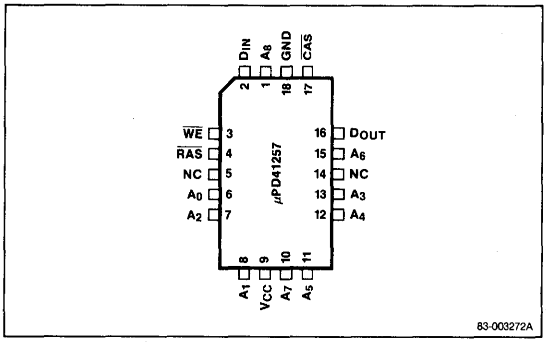
- □ 262,144-word x 1-bit organization
- □ Multiplexed address inputs
- □ Single +5-volt ±10% power supply
- □ Nibble read, write, or read-modify-write cycles
- □ $\overline{CAS}$ before $\overline{RAS}$ internal refreshing
- □ Low power dissipation
  - 28 mW max (standby)
  - 413 mW max (active, t_{RC} = 220 ns)
- □ Nonlatched, three-state output
- □ TTL-compatible inputs with low input capacitance
- □ 256-cycle/4-ms refresh period(A_0-A_7 are refresh addresses)
- □ High-density plastic DIP and PLCC packaging

Pin Configurations

16-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



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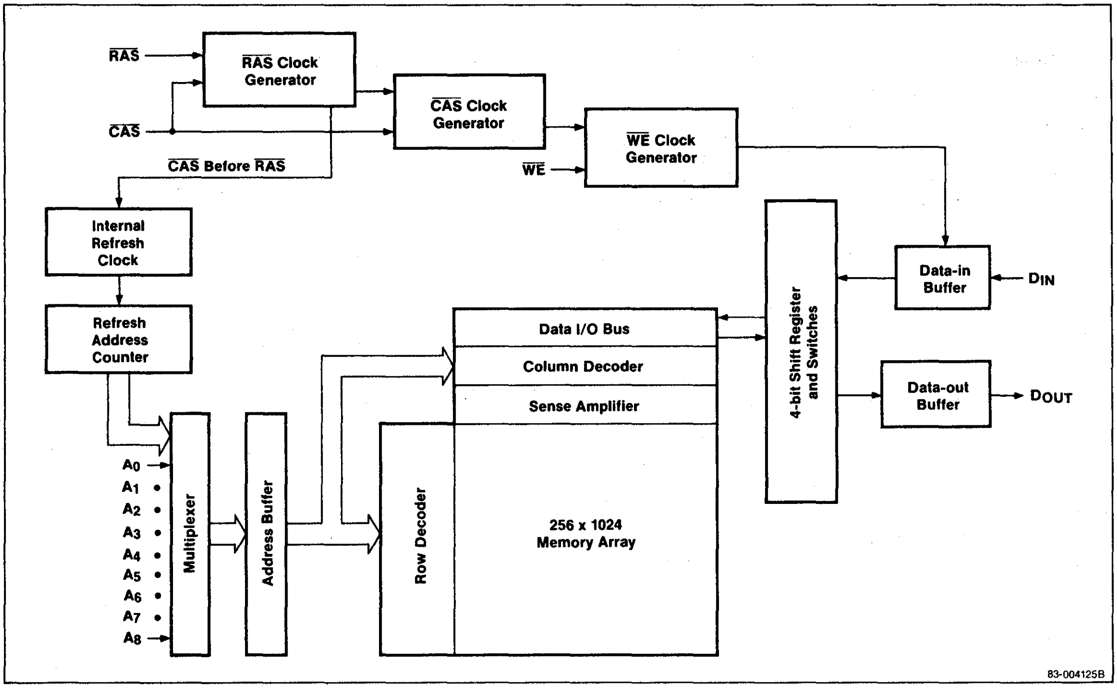
NEC

Block Diagram



Pin Identification

Symbol	Function
A_0-A_8	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{WE}$	Write enable
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
GND	Ground
V_{CC}	+5.0-volt power supply

Capacitance

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{I1}			5	pF	A_0-A_8, D_{IN}
	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_O			7	pF	D_{OUT}

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Short-circuit output current	50 mA
Power dissipation, P_D	1 W
Operating temperature, T_A	0 to +70°C
Storage temperature, T_{STG}	−55 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	Access Time (max)	R/W Cycle (min)	Package
μPD41257C-12	120 ns	220 ns	16-pin plastic DIP
C-15	150 ns	260 ns	
C-20	200 ns	330 ns	
μPD41257L-12	120 ns	220 ns	18-pin PLCC
L-15	150 ns	260 ns	
L-20	200 ns	330 ns	

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Standby power supply current	I_{CC2}			5	mA	$\overline{RAS} = V_{IH}$; D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10		10	μA	Any input $V_{IN} = 0$ V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OUT} = -5$ mA
Output voltage, low	V_{OL}	0		0.4	V	$I_{OUT} = 4.2$ mA
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input voltage, high	V_{IH}	2.4		5.5	V	All inputs
Input voltage, low	V_{IL}	−1.0		0.8	V	All inputs

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		μPD41257-12		μPD41257-15		μPD41257-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Standard Operation									
Average power supply operating current	I_{CC1}		75		70		60	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Average power supply current, refresh cycle	I_{CC3}		60		55		55	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	220		260		330		ns	(Note 6)
Read-write cycle time	t_{RWC}	265		310		390		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	30	0	40	0	50	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	90		100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	120	10,000	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	60	10,000	75	10,000	100	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	120		150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	35	100	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time	t_{CPN}	30		30		35		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41257-12 Min	μPD41257-12 Max	μPD41257-15 Min	μPD41257-15 Max	μPD41257-20 Min	μPD41257-20 Max	Unit	Test Conditions
Standard Operation (cont)									
Row address hold time	t_{RAH}	15		15		25		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	20		25		55		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		155		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		25		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	30		40		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	90		115		155		ns	
Write command pulse width	t_{WP}	20		25		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		55		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	30		40		55		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	90		115		155		ns	
Refresh period	t_{REF}		4		4		4	ms	
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	60		75		100		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	120		150		200		ns	(Note 15)
Nibble Mode									
Average power supply current, nibble mode	I_{CC6}		35		27		27	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{NC} = t_{NC}$ min (Note 5)
Nibble-mode cycle time	t_{NC}	60		70		100		ns	(Note 6)
Nibble-mode access time	t_{NAC}		30		35		50	ns	(Note 7)
Nibble-mode precharge time	t_{NP}	20		25		40		ns	
Nibble-mode $\overline{WE}$ pulse width	t_{NWP}	20		25		40		ns	
Nibble-mode $\overline{CAS}$ pulse width	t_{NAS}	30		35		50		ns	
Nibble-mode $\overline{RAS}$ hold time (read cycle)	t_{NRRSH}	30		35		50		ns	
Nibble-mode $\overline{RAS}$ hold time (write cycle)	t_{NWRSH}	35		35		50		ns	
Nibble-mode $\overline{CAS}$ to $\overline{WE}$ delay	t_{NCWD}	30		35		50		ns	
Nibble-mode $\overline{WE}$ to $\overline{CAS}$ lead time	t_{NCWL}	30		35		50		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41257-12 Min	μPD41257-12 Max	μPD41257-15 Min	μPD41257-15 Max	μPD41257-20 Min	μPD41257-20 Max	Unit	Test Conditions
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle									
Average power supply current, $\overline{CAS}$ before $\overline{RAS}$ refreshing	I_{CC4}		65		60		55	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IL}$; $t_{RC} = t_{RC}$ min (Note 5)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	25		30		30		ns	
Read or write cycle time (counter test cycle)	t_{TRC}	245		285		350		ns	
Read-write cycle time (counter test cycle)	t_{TRWC}	290		335		410		ns	
$\overline{CAS}$ precharge time (counter test cycle)	t_{TCP}	50		60		80		ns	

Notes:

(1) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(2) Ac measurements assume $t_T = 5$ ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(4) All voltages are referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown. For the $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle, t_{RAC} is specified as $t_{RAC} = t_{CHR} + t_{TCP} + t_{CAC} + 2t_T$ and is greater than the maximum specified value shown in this table.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. Time t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, t_{NCWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only.

If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle or a nibble mode early write cycle and the data output pin will remain open-circuit throughout the entire cycle.

If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output pin will contain data read from the selected cell.

If $t_{NCWD} \geq t_{NCWD}$ (min), the cycle is a nibble mode read-write cycle and the data output pin will contain data read from the selected cell.

If none of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

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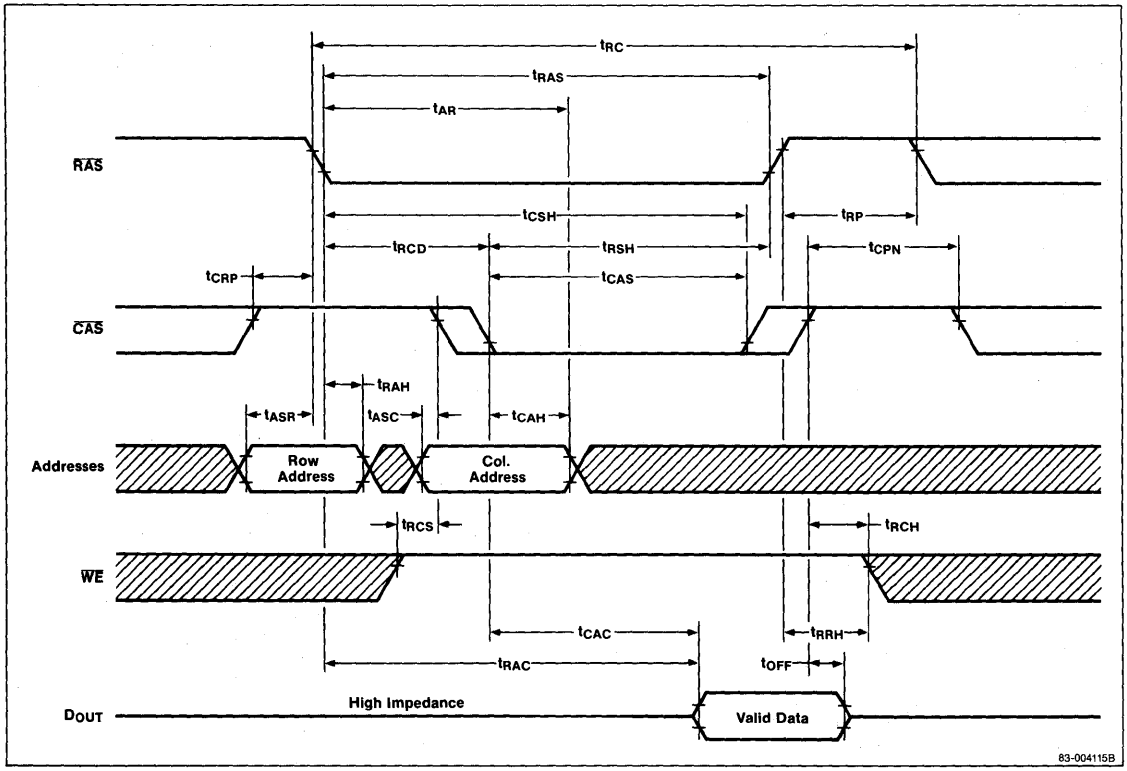
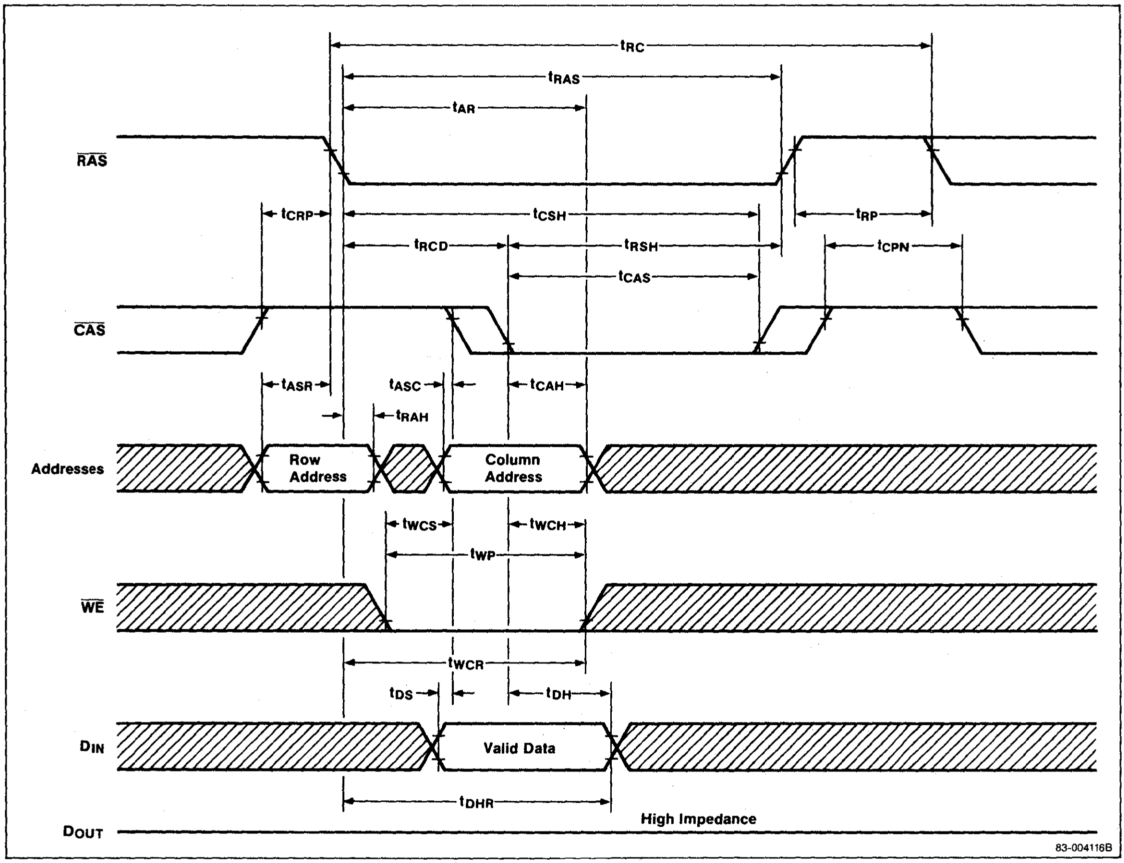
Timing Waveforms

Read Cycle



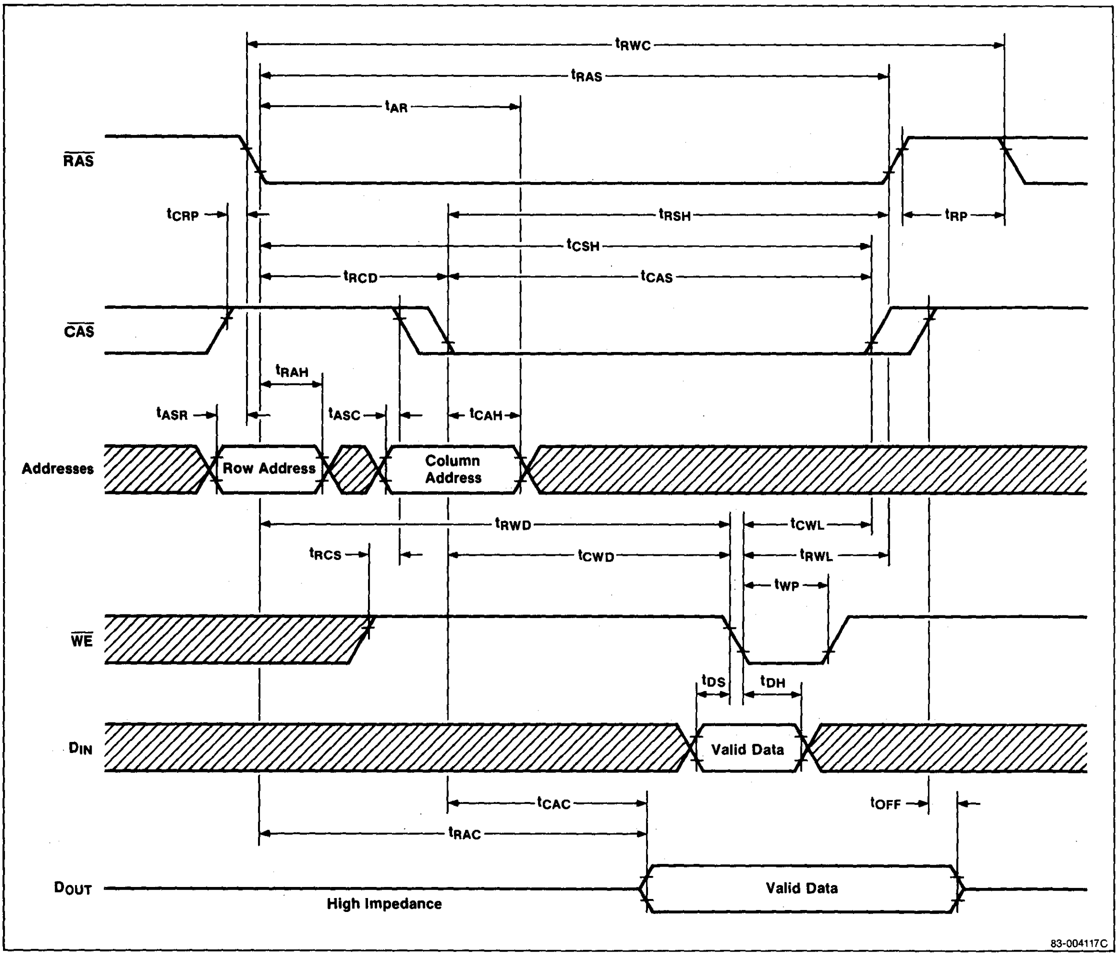
Timing Waveforms (cont)

Write Cycle (Early Write)



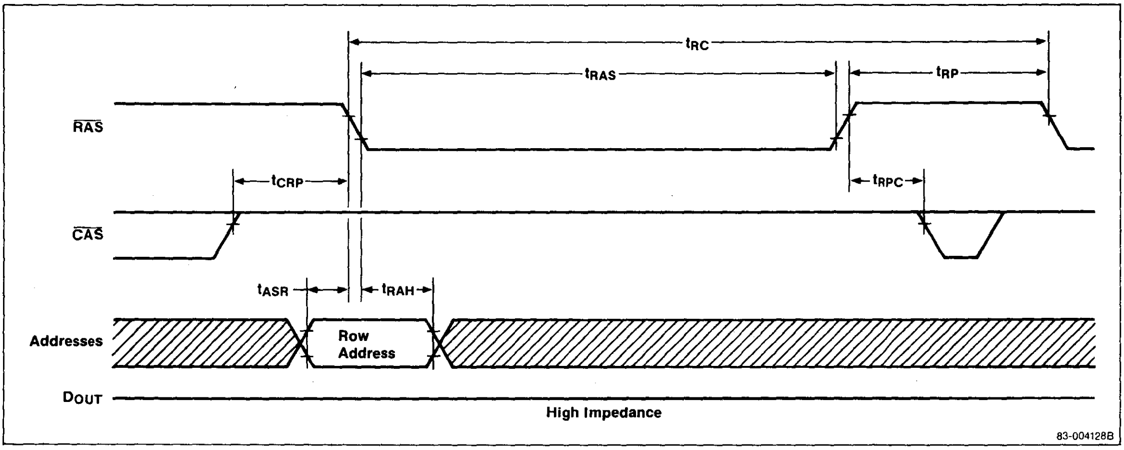
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

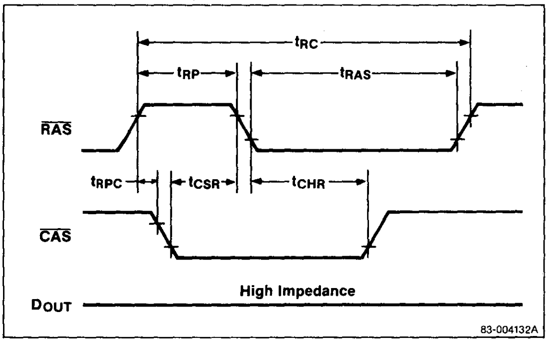


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



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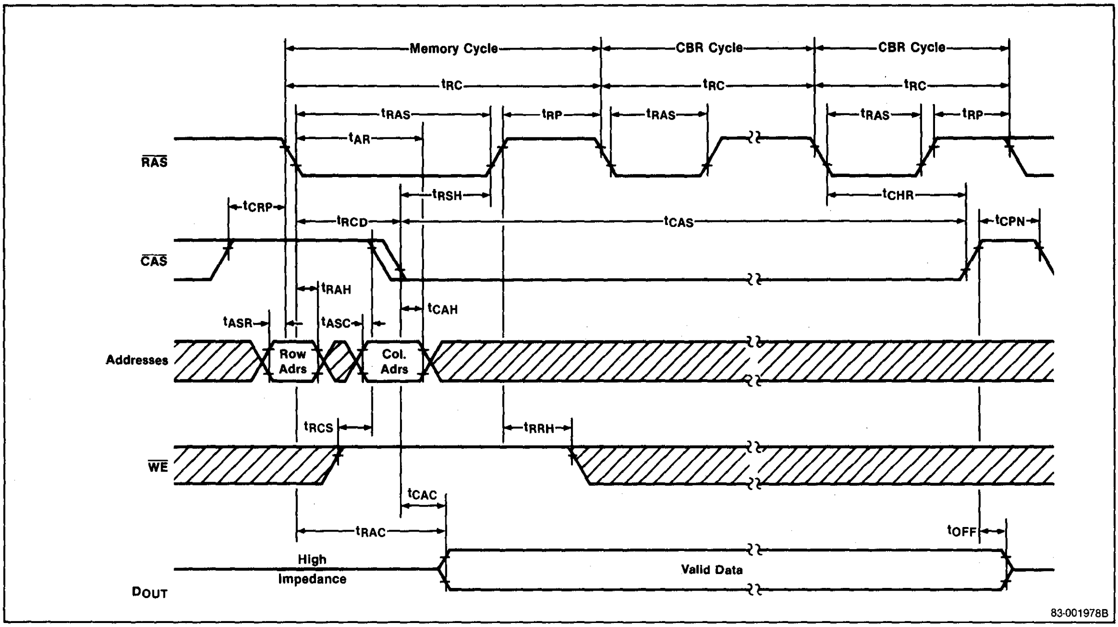
Timing Waveforms (cont)

Hidden Refresh Cycle



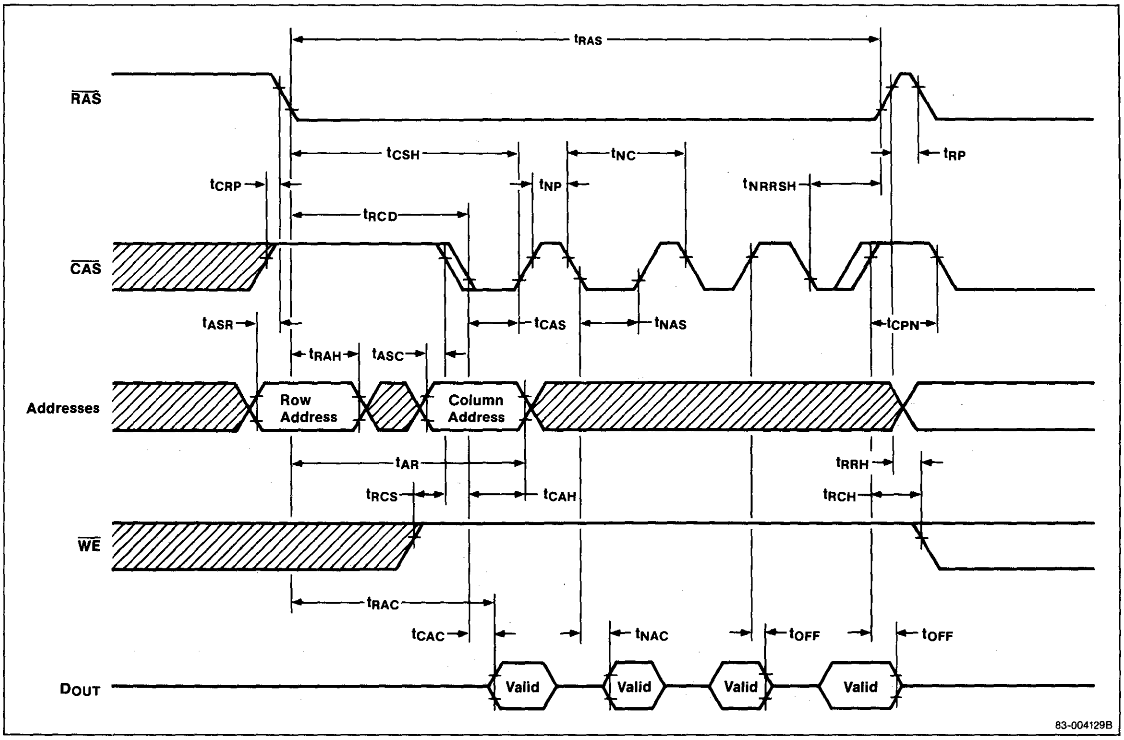
Nibble Mode

The µPD41257 is capable of executing nibble read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of a maximum of 4 data bits. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling $\overline{CAS}$ while $\overline{RAS}$ is held low. The addresses of nibble bits are determined by the combination of row address A_8 and column address A_8 in the following sequence.

		Row Address									Column Address									
Sequence	Nibble Bit	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}/\overline{CAS}$	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Example: external address input
$\overline{CAS}$ cycling	2	1	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Internal address generated
$\overline{CAS}$ cycling	3	0	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	4	1	1	0	0	0	1	0	1	0	1	1	0	1	0	1	0	0	0	
$\overline{CAS}$ cycling	1	0	1	0	0	0	1	0	1	0	0	1	0	1	0	1	0	0	0	Repeated sequence

Timing Waveforms (cont)

Nibble Mode Read Cycle



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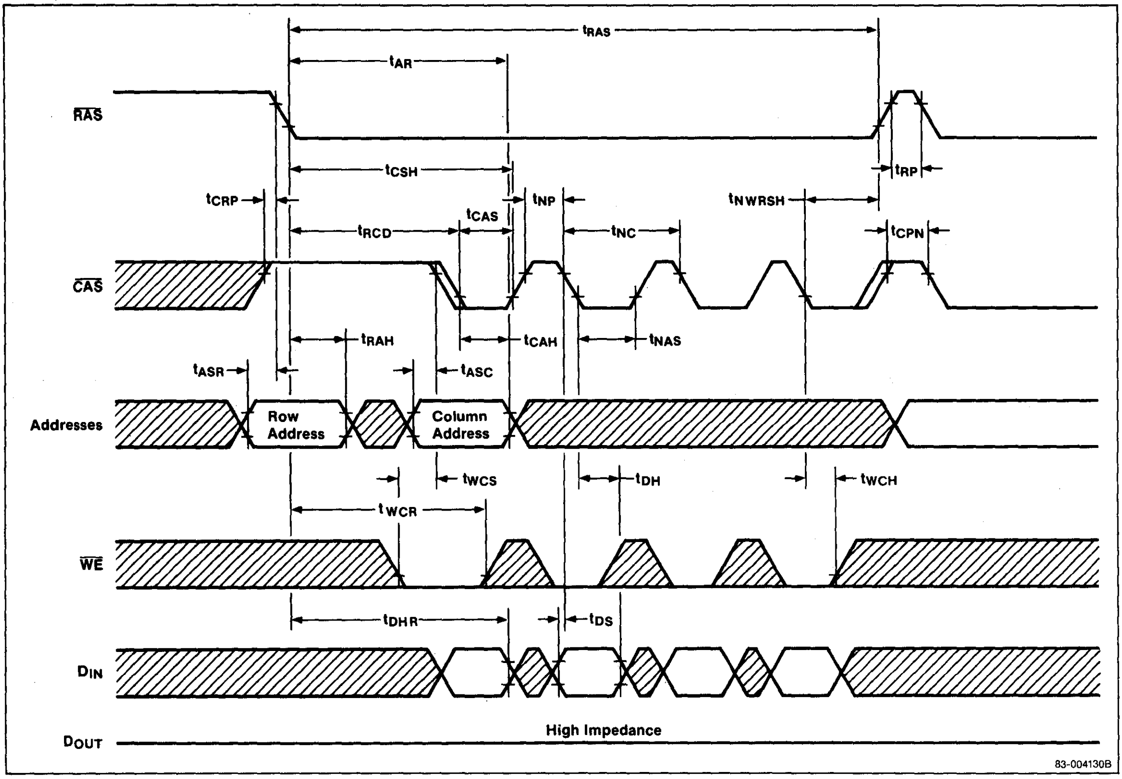
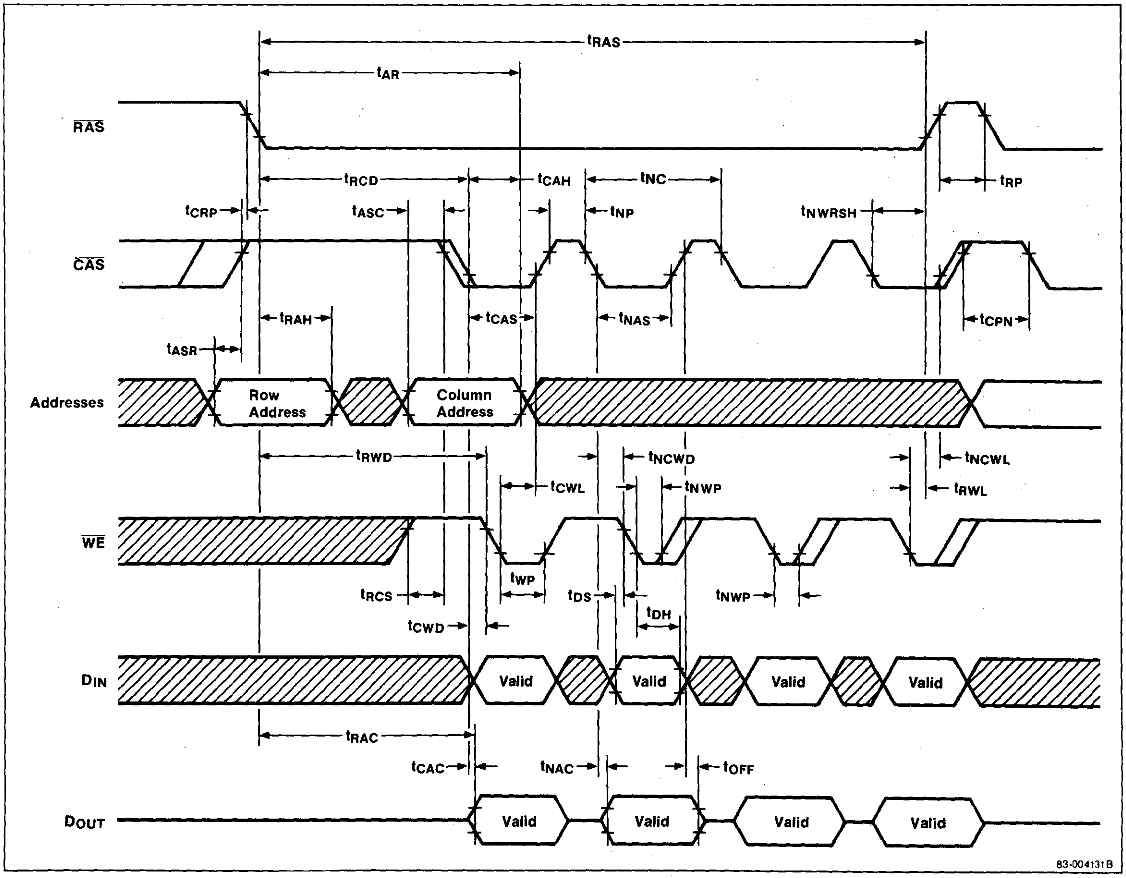
Timing Waveforms (cont)

Nibble Mode Write Cycle



Timing Waveforms (cont)

Nibble Mode Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test

The $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter functionality is verified by using the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle. After $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation, $\overline{\text{CAS}}$ goes to a high level (after prescribed time t_{CHR}) and then goes to a low level (after prescribed time t_{TCP}) while $\overline{\text{RAS}}$ is held at a low level. The read, write, and read-modify-write operations are enabled as shown in the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test timing diagrams. A row address is defined by the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh internal address counter, and a column address is defined by latching the external address at the second falling edge of $\overline{\text{CAS}}$.

Suggested $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test pattern:

(1) Initialize the internal refresh counter using 8 $\overline{\text{RAS}}$-only refresh cycles after power-on.

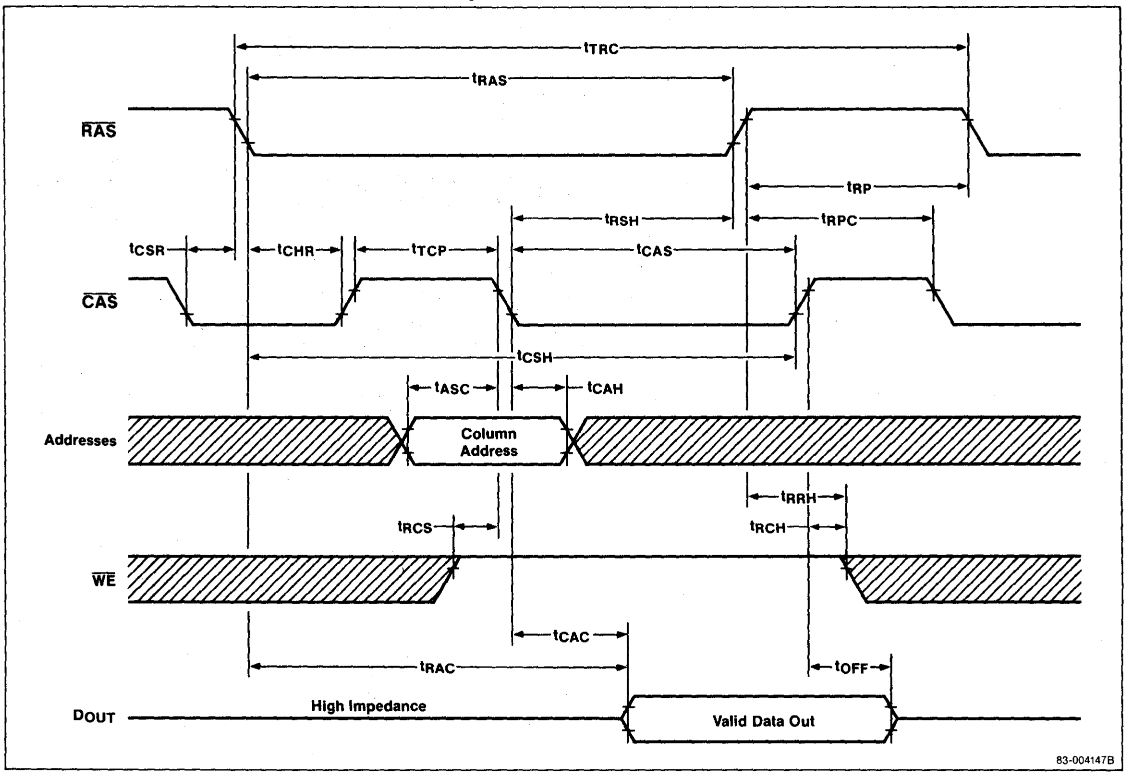
(2) Write a test pattern of zeros into 256 memory cells at a single fixed column address using 256 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test write cycles.

(3) Using the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test read-modify-write cycle, read the "0" previously written during operation (2) and write a new "1" in the same cycle. Repeat this 256 times to write a pattern of ones into the 256 memory cells.

(4) Read the "1" written in operation (3) using the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test read cycle.

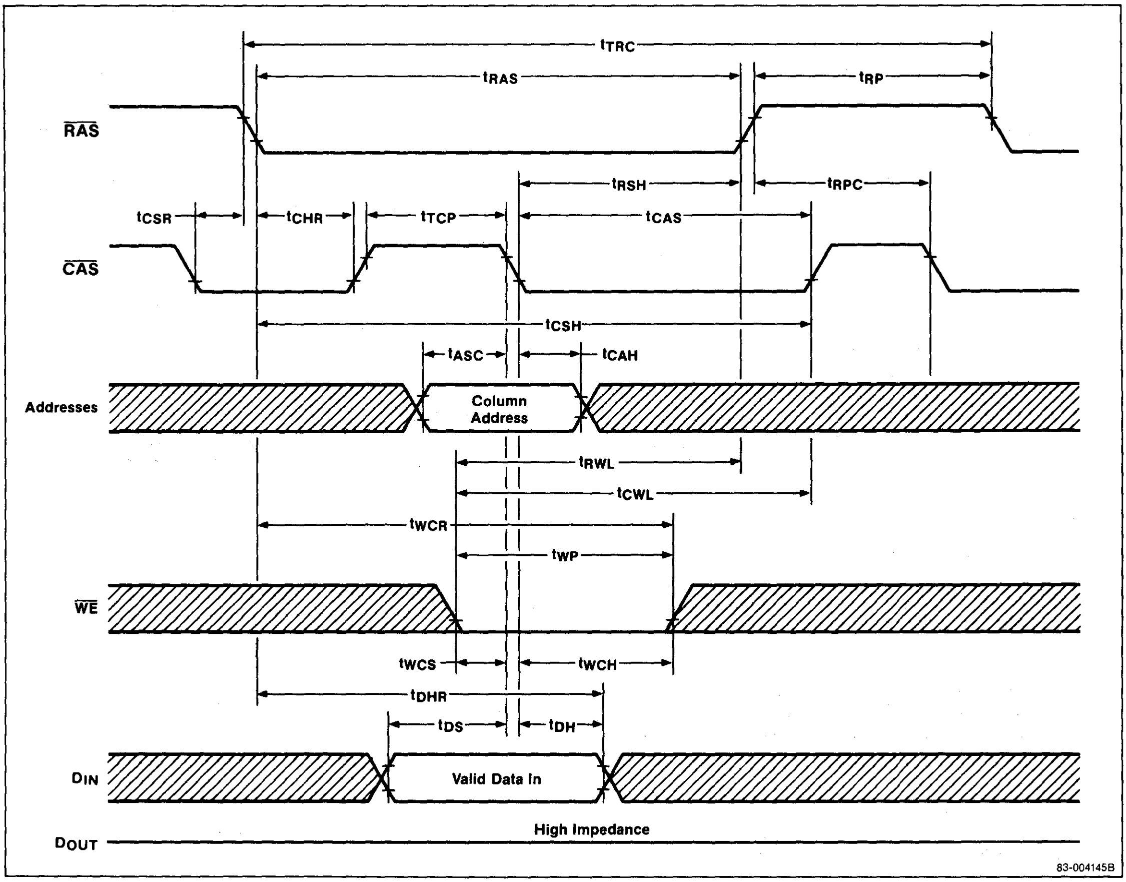
(5) Complement the test pattern data and repeat operations (2), (3), and (4).

$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Read Cycle



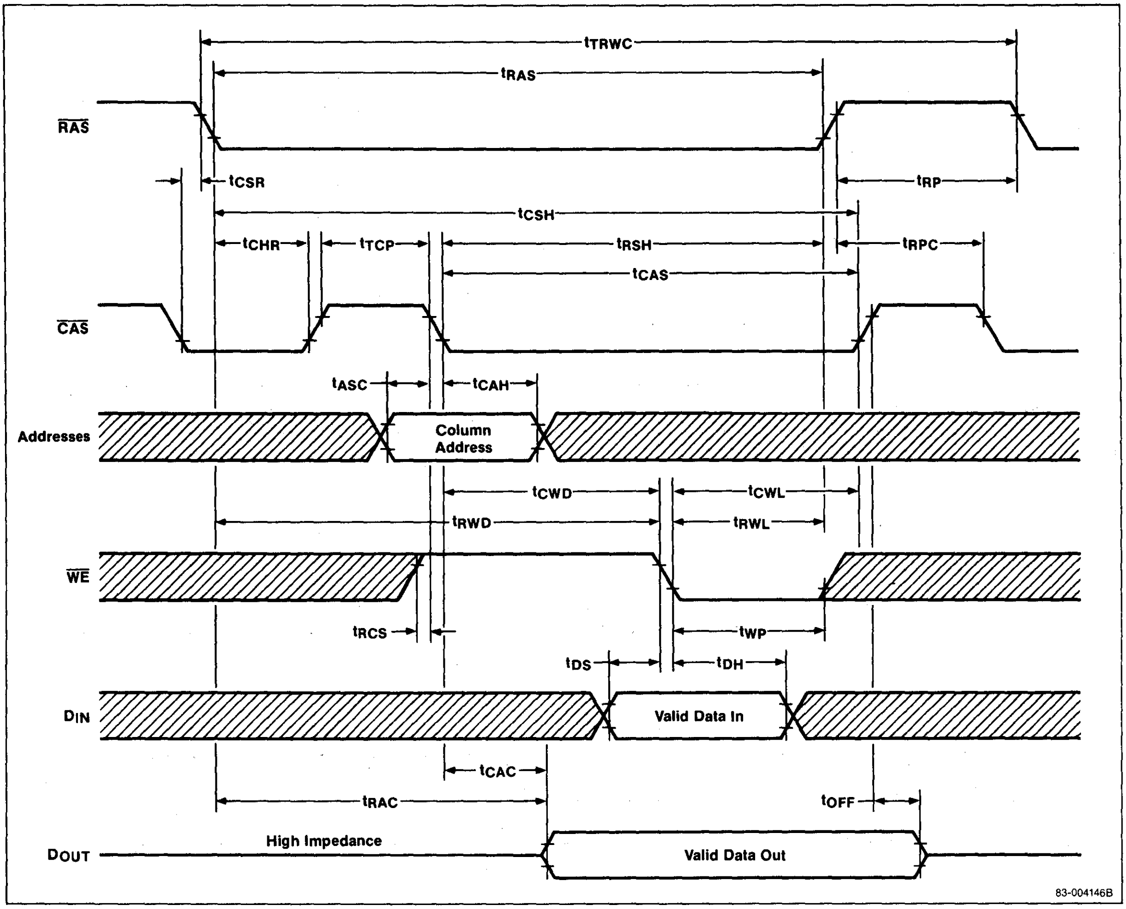
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



μPD41464 65,536 x 4-BIT DYNAMIC NMOS RAM

Description

The μPD41464 is a 65,536-word by 4-bit dynamic NMOS RAM designed to operate from a single +5-volt power supply. The negative voltage substrate bias is generated internally; its operation is automatic and transparent. The μPD41464 is fabricated with double-polylayer, N-channel silicon gate processing to provide high storage cell density, high performance, and high reliability. A single-transistor dynamic storage cell and advanced dynamic circuitry throughout ensure minimum power dissipation.

The three-state I/O is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or hidden refresh cycle, data is held by holding $\overline{\text{CAS}}$ low. Input and output is returned to a state of high impedance by returning $\overline{\text{CAS}}$ high. Hidden refreshing allows $\overline{\text{CAS}}$ to be held low to maintain output data while $\overline{\text{RAS}}$ is used to execute $\overline{\text{RAS}}$-only refresh cycles.

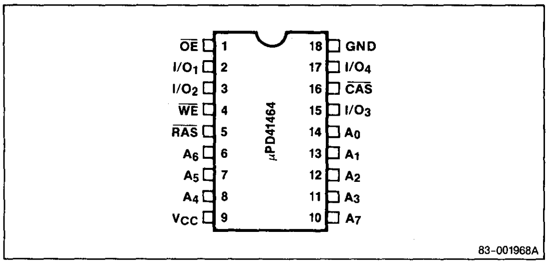
Automatic refreshing of internally generated refresh addresses is accomplished by means of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles. Refreshing can also be accomplished by means of $\overline{\text{RAS}}$-only refresh cycles or by normal read or write cycles on the 256 address combinations of A_0-A_7 during a 4-ms period.

Features

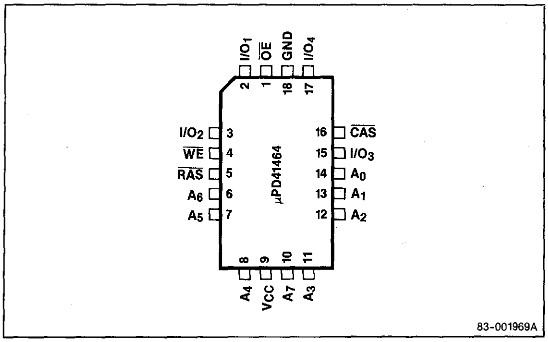
- ☐ 65,536-word by 4-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ internal refreshing
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation
  - — 28 mW (standby)
  - — 440 mW (active, $t_{RC} = t_{RC}$ min)
- ☐ Nonlatched, TTL-compatible inputs and outputs
- ☐ Low input capacitance
- ☐ 256 refresh cycles during 4-ms period
- ☐ Standard plastic DIP, PLCC, and ZIP packaging

Pin Configurations

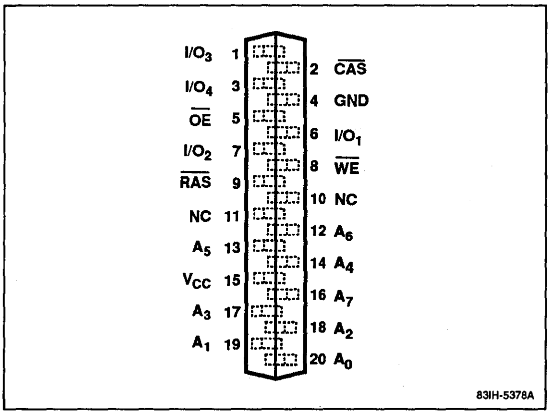
18-Pin Plastic DIP



18-Pin PLCC



20-Pin Plastic ZIP



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Pin Identification

Symbol	Function
A_0-A_7	Address inputs
I/O_1-I/O_4	Data I/O
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (Max)	Package
μPD41464C-10	100 ns	18-pin plastic DIP
C-12	120 ns	
C-15	150 ns	
μPD41464L-10	100 ns	18-pin PLCC
L-12	120 ns	
L-15	150 ns	
μPD41464V-10	100 ns	20-pin ZIP
V-12	120 ns	
V-15	150 ns	

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1 W

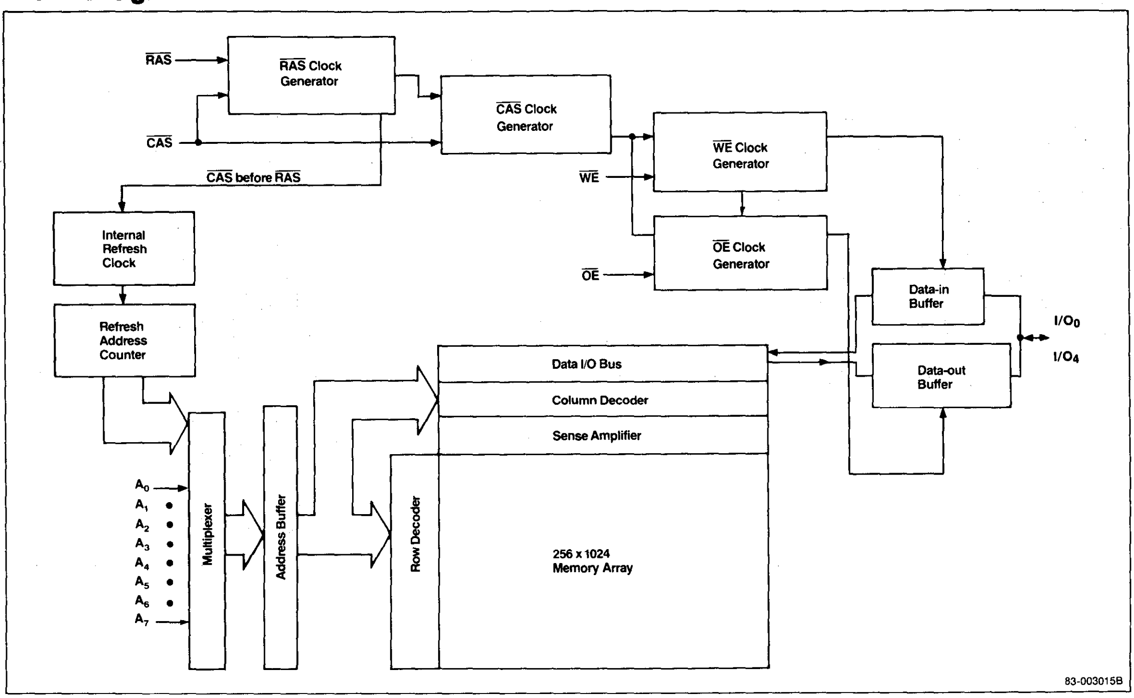
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Pins Under Test
Input capacitance	C_{I1}			5	pF	A_0-A_7
	C_{I2}			8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O			7	pF	I/O_1-I/O_4

Block Diagram



DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input voltage, high	V_{IH}	2.4		$V_{CC} + 1.0$	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			5.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
Input leakage current	$I_{I(L)}$	−10		10	μA	$V_{IN} = 0$ to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	I/O is high-Z; $V_{I/O} = 0$ to V_{CC}
Output voltage, low	V_{OL}	0		0.4	V	$I_{OL} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -5$ mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		μPD41464-10		μPD41464-12		μPD41464-15			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		80		75		70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		65		60		55	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, page cycle, average	I_{CC4}		55		50		45	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		70		65		60	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	200		220		260		ns	(Note 6)
Read-write cycle time	t_{RWC}	270		300		355		ns	(Note 6)
Page cycle time	t_{PC}	100		120		145		ns	(Note 6)
Refresh period	t_{REF}		4		4		4	ms	
Access time from $\overline{RAS}$	t_{RAC}		100		120		150	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		50		60		75	ns	(Notes 7, 9)
Output buffer turnoff delay	t_{OFF}	0	25	0	30	0	40	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Notes 2, 3)
$\overline{RAS}$ precharge time	t_{RP}	90		90		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)

AC Characteristics (cont)

Parameter	Symbol	μPD41464-10 Min	μPD41464-10 Max	μPD41464-12 Min	μPD41464-12 Max	μPD41464-15 Min	μPD41464-15 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	40		50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		15		15		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	65		80		100		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	25		30		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	75		90		115		ns	
Write command pulse width	t_{WP}	15		20		25		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	25		30		40		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	75		90		115		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	130		155		195		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	80		95		120		ns	(Note 15)
Access time from $\overline{OE}$	t_{OEA}		25		30		40	ns	
Data delay time	t_{OED}	25		30		40		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	25	0	30	0	40	ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	10		10		10		ns	
Read or write cycle time (counter test cycle)	t_{TRC}	220		245		285		ns	(Note 16)
Read write cycle time (counter test cycle)	t_{TRWC}	290		325		380		ns	(Note 16)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	20		25		30		ns	

Notes:

(1) An initial pause of 100 μs ($\overline{RAS}$ inactive) is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(2) AC measurements assume $t_T = 5$ ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals.

(4) All voltages are referenced to GND.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns and $I_{CC3} = 60$ mA.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70\,°C$) is assured. For lot code K of the μPD41464-15, t_{RC} (min) must be 270 ns.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown. For a $\overline{CAS}$ before RAS refresh counter test cycle, t_{RAC} is specified as $t_{RAC} = t_{CHR} + t_{CP} + t_{CAC} + 2t_T$ and is greater than the maximum specified value shown in this table.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

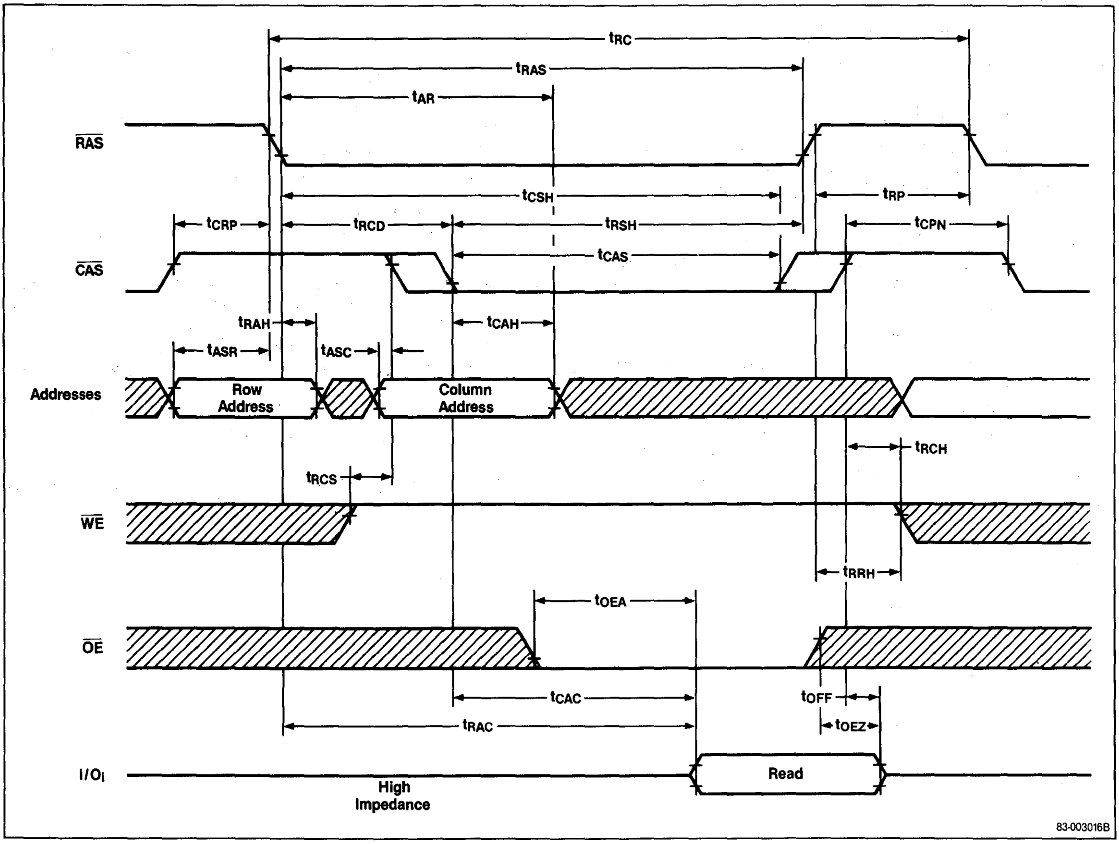
(14) These parameters are referenced to the leading edge of $\overline{CAS}$ for early write cycles and to the leading edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) t_{TRC} and t_{TRWC} are applicable for $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycles.

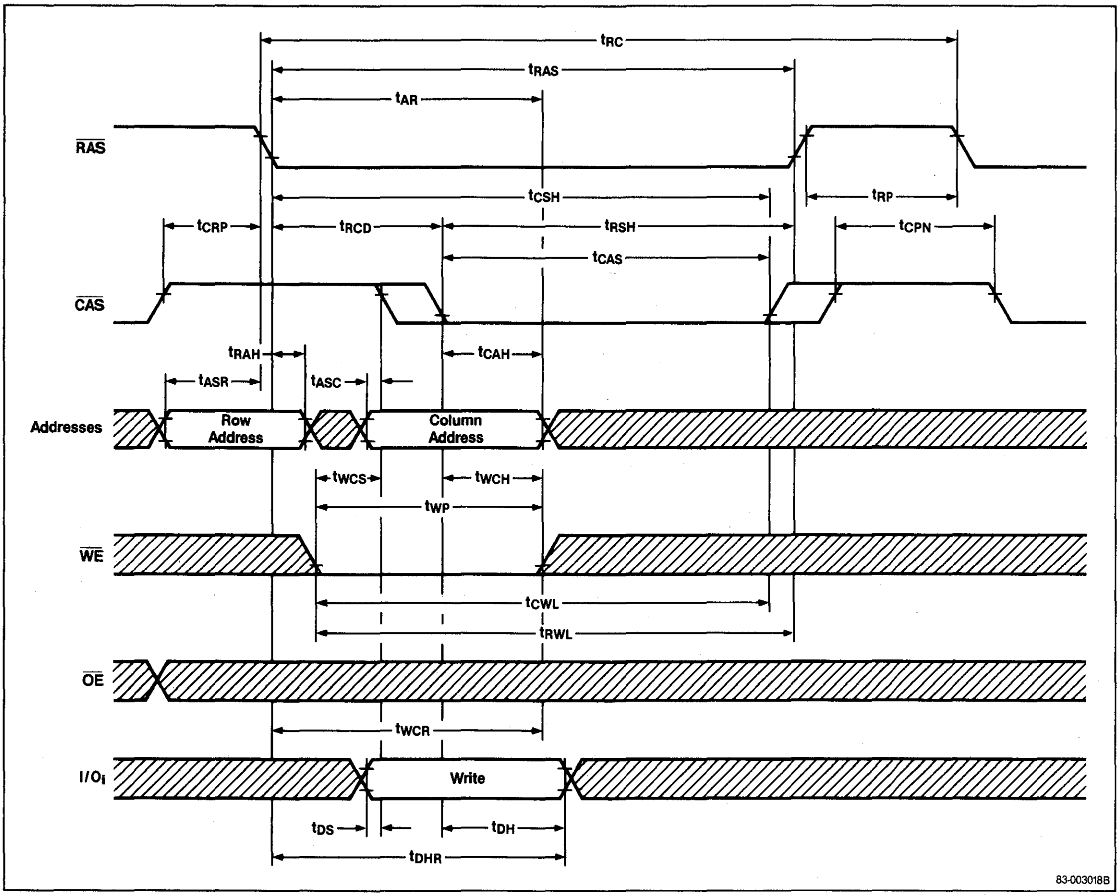
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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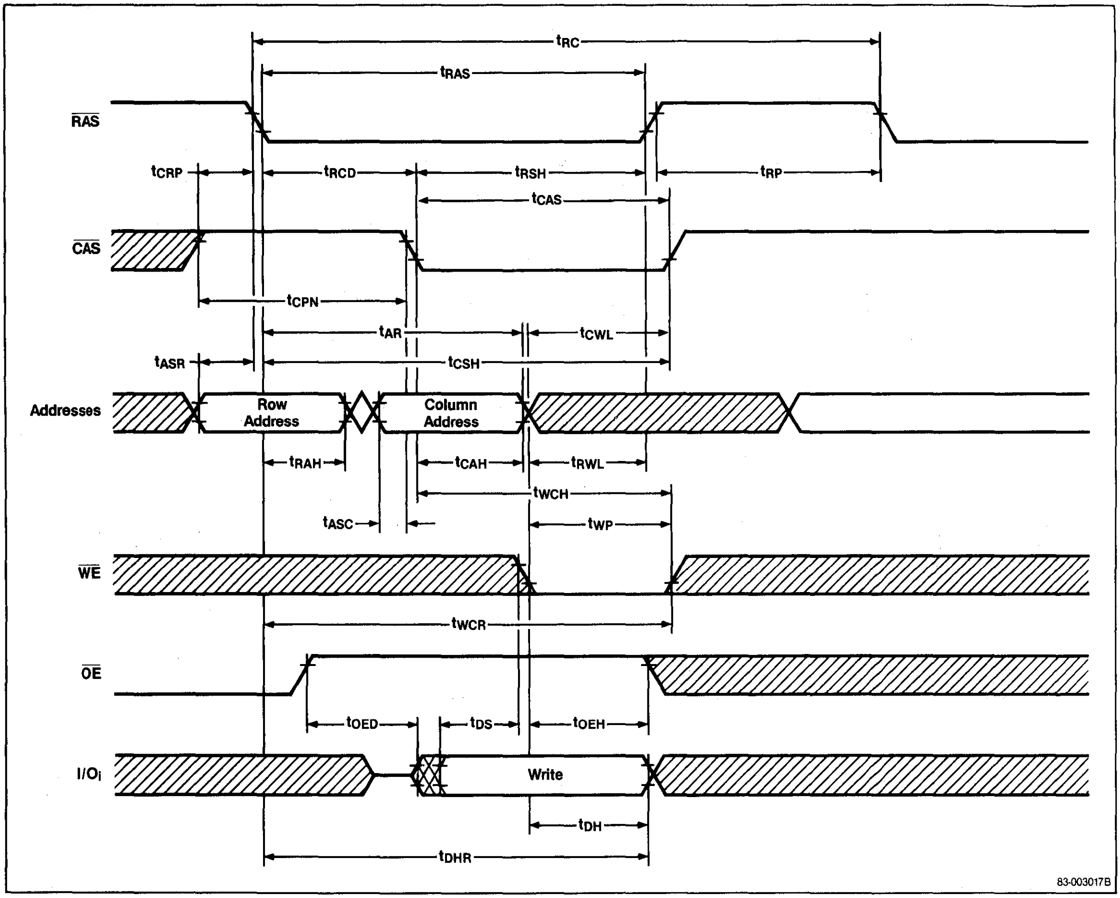
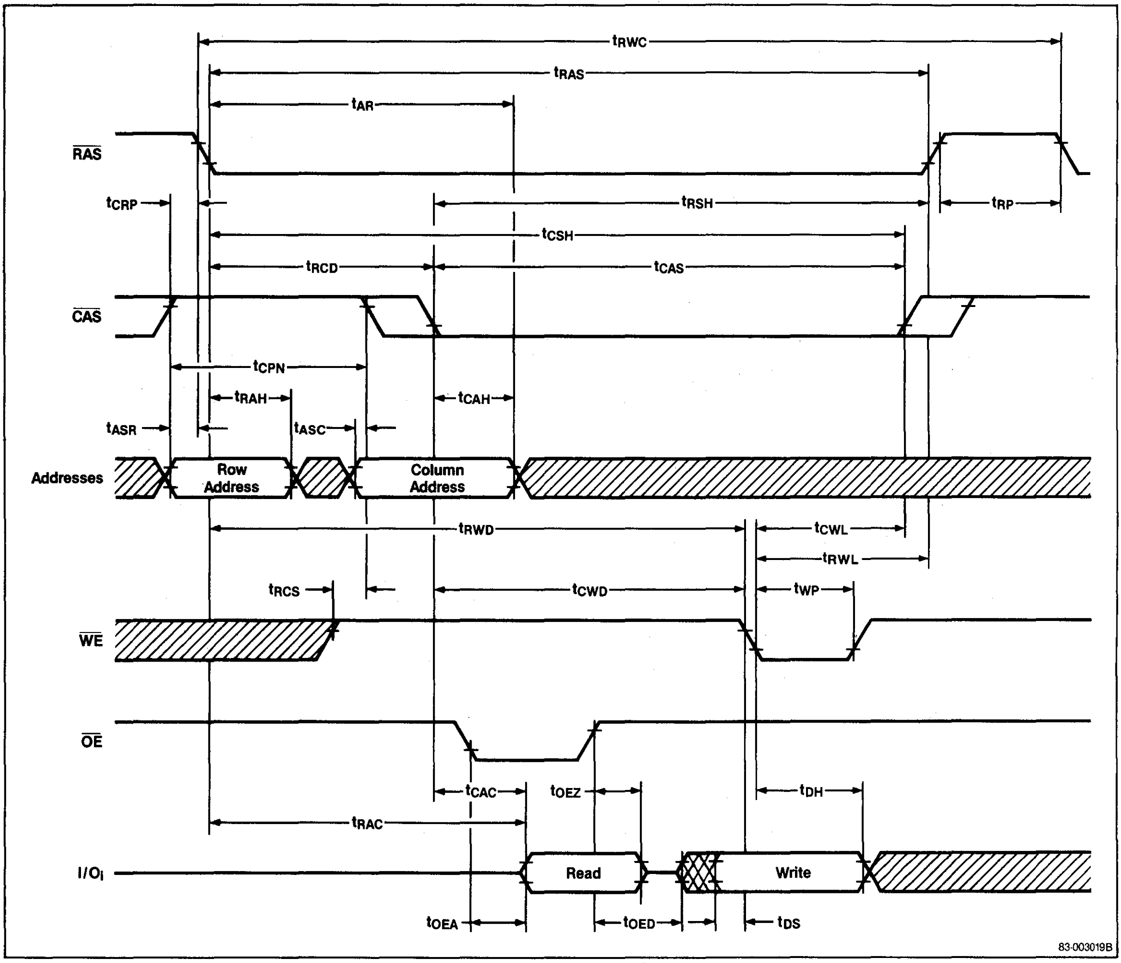
Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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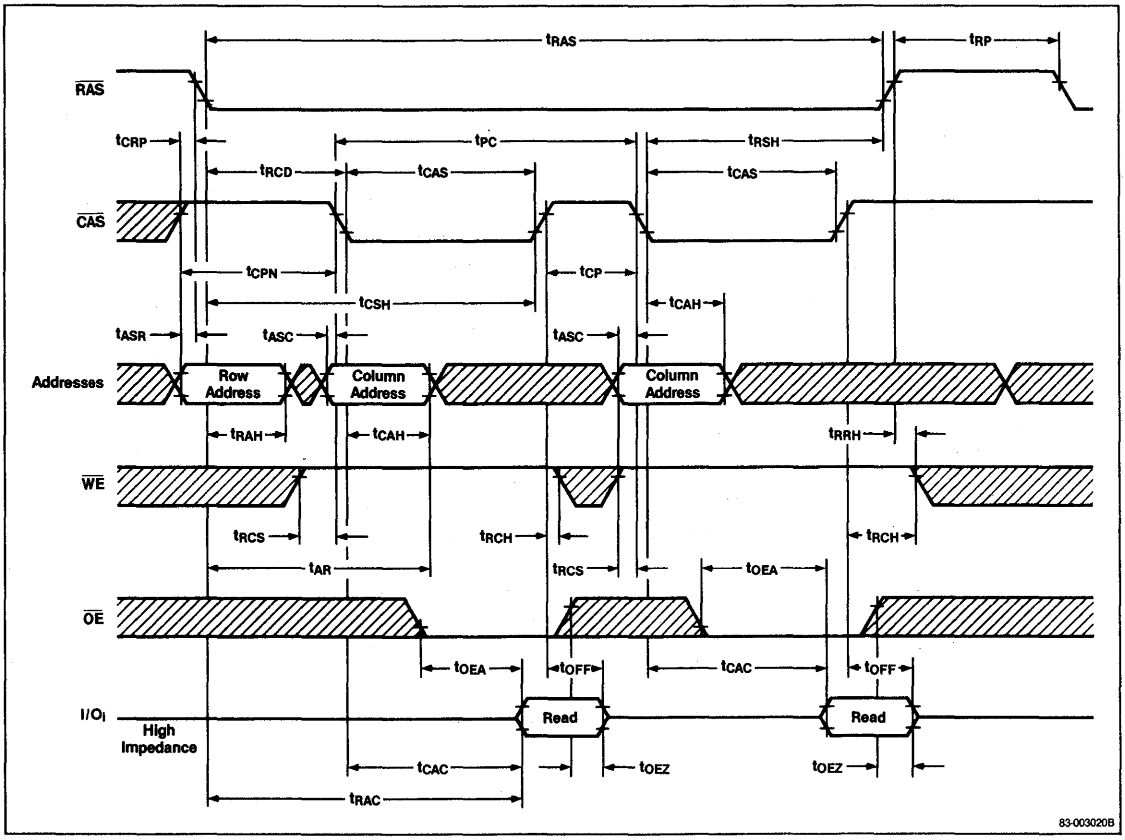
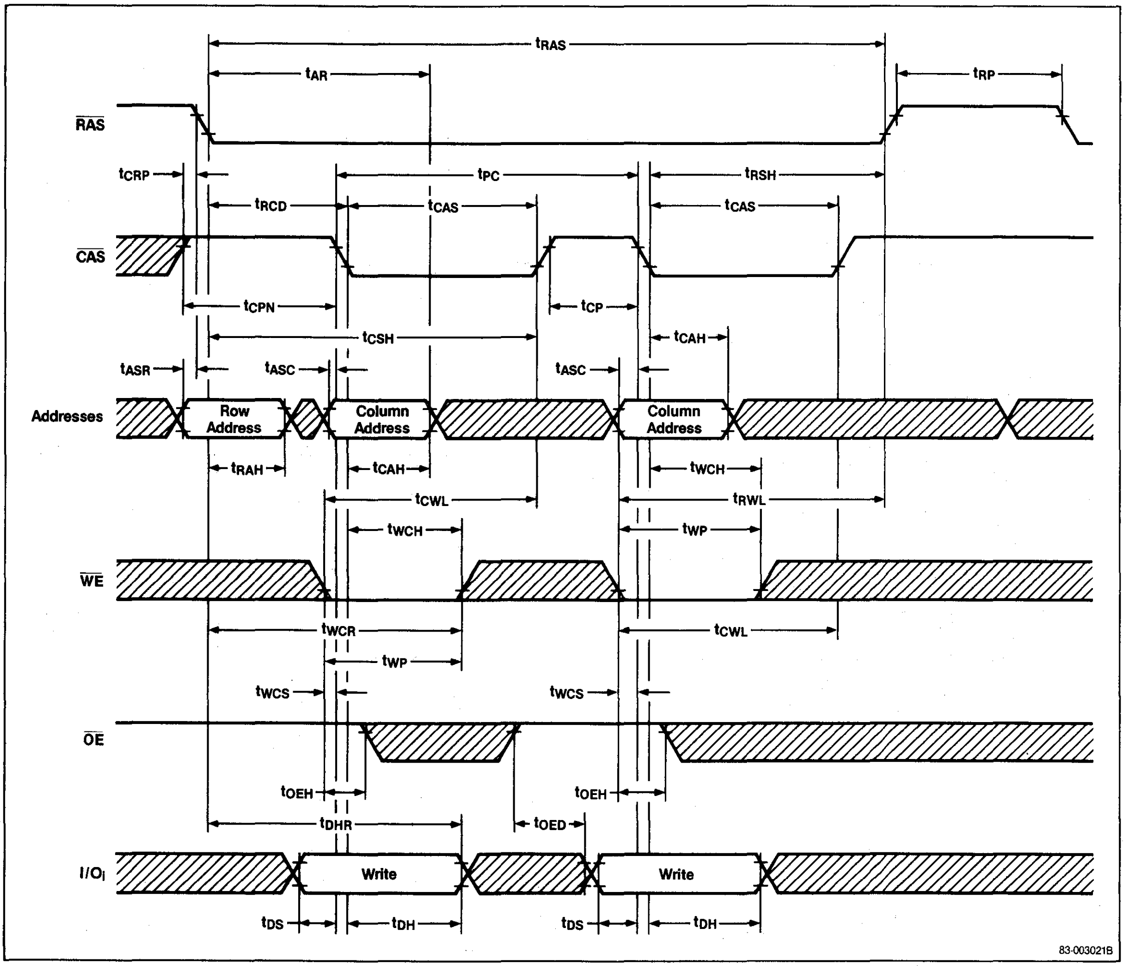
Timing Waveforms (cont)

Page Mode Read Cycle



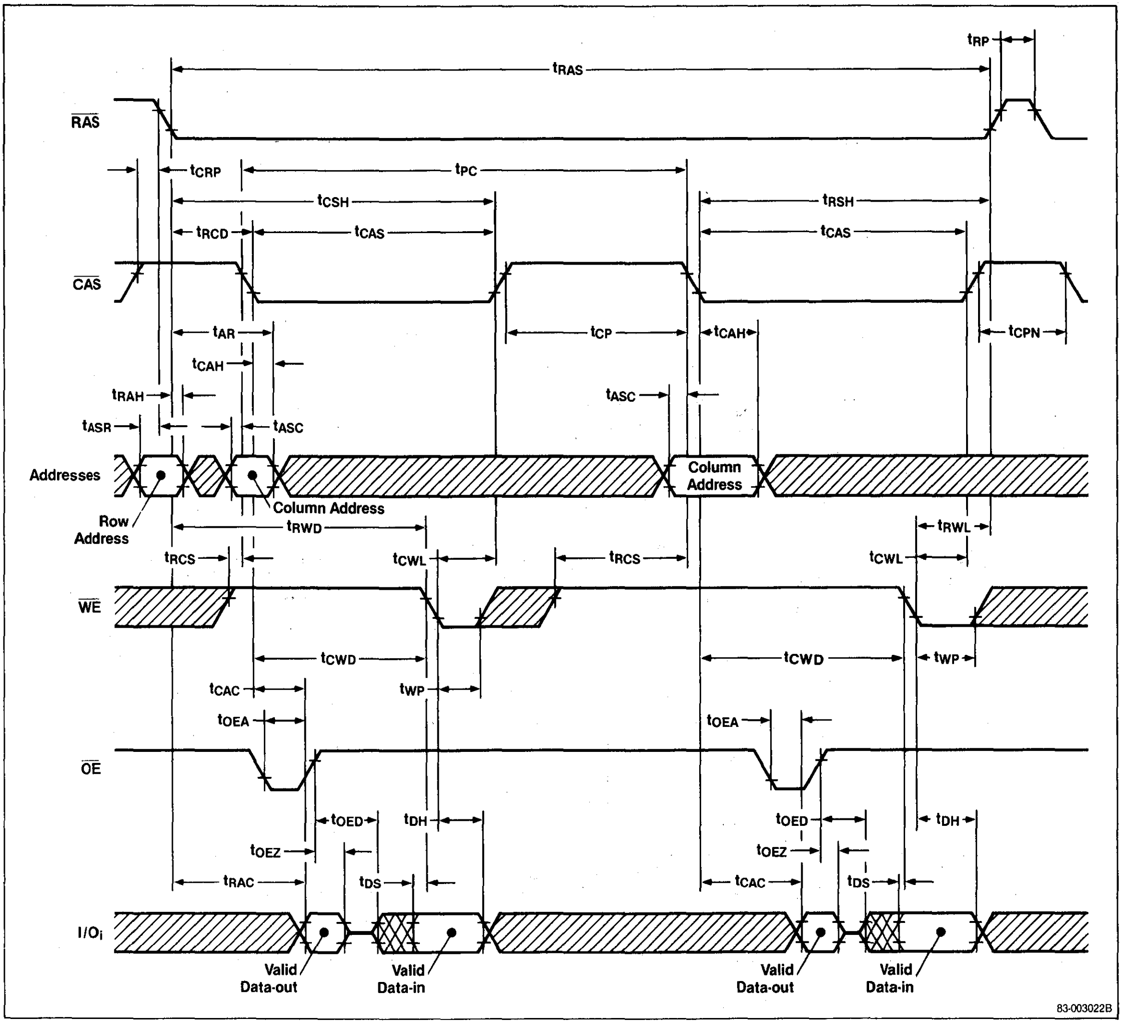
Timing Waveforms (cont)

Page Mode Write Cycle (Early Write)



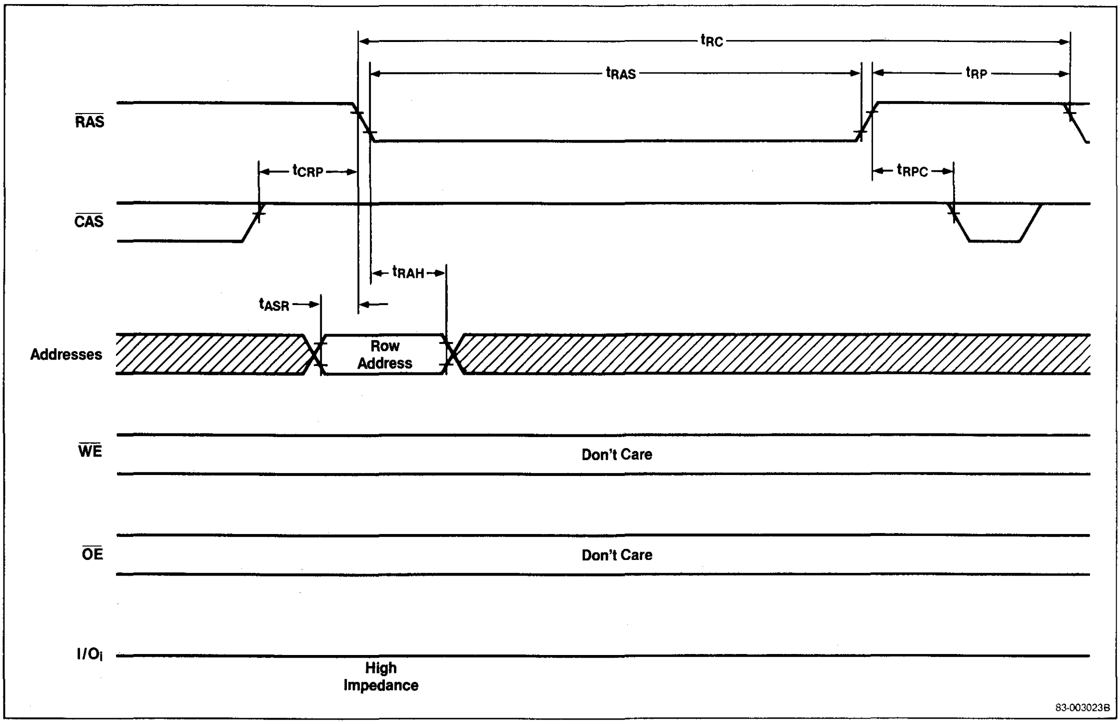
Timing Waveforms (cont)

Page Mode Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



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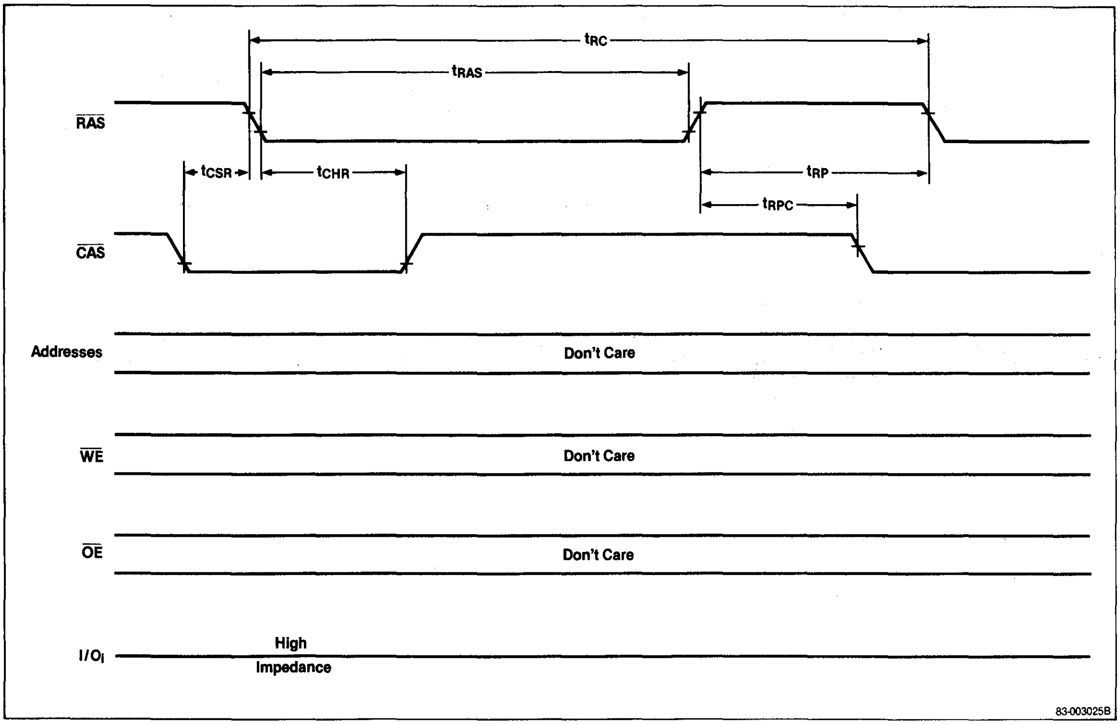
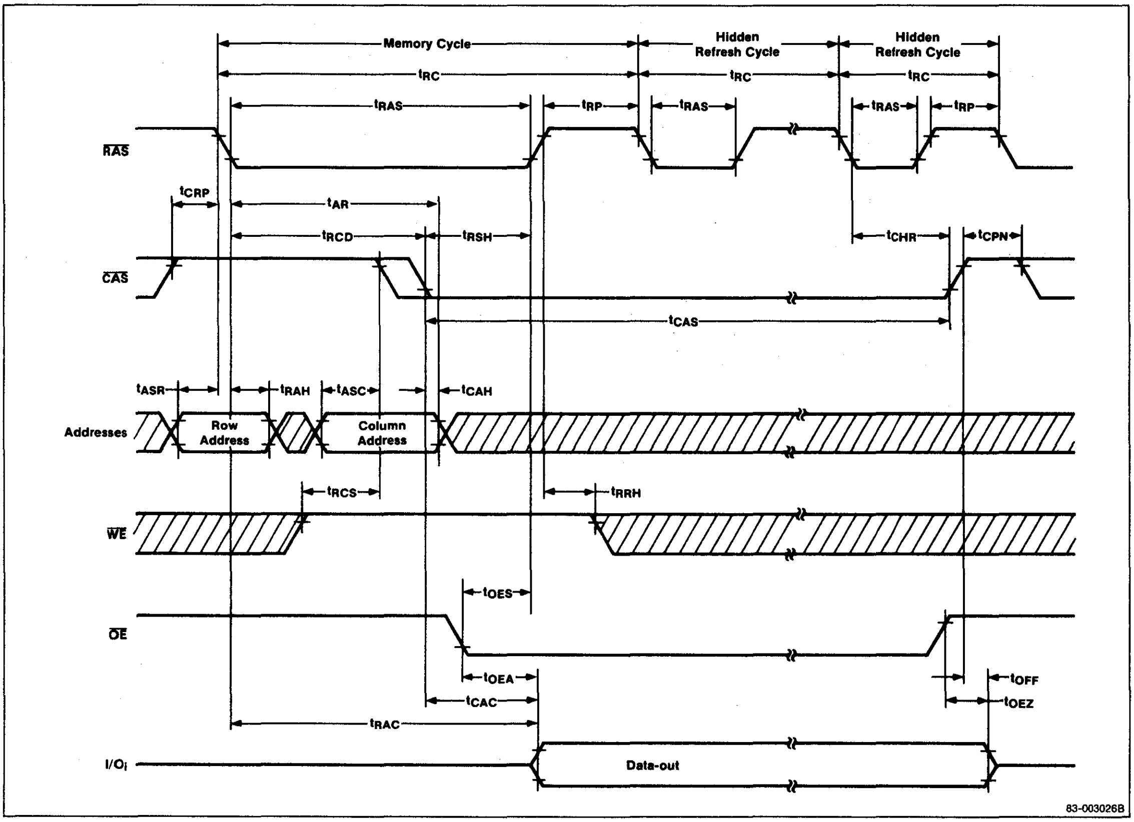
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Timing Waveforms (cont)

Hidden Refresh Cycle



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$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test

The μPD41464 provides a method to verify proper operation of the internal address counter used in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing. After a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle is initiated, $\overline{\text{CAS}}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{\text{RAS}}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{\text{CAS}}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{\text{RAS}}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test write cycles. Use the same column address in each cycle.

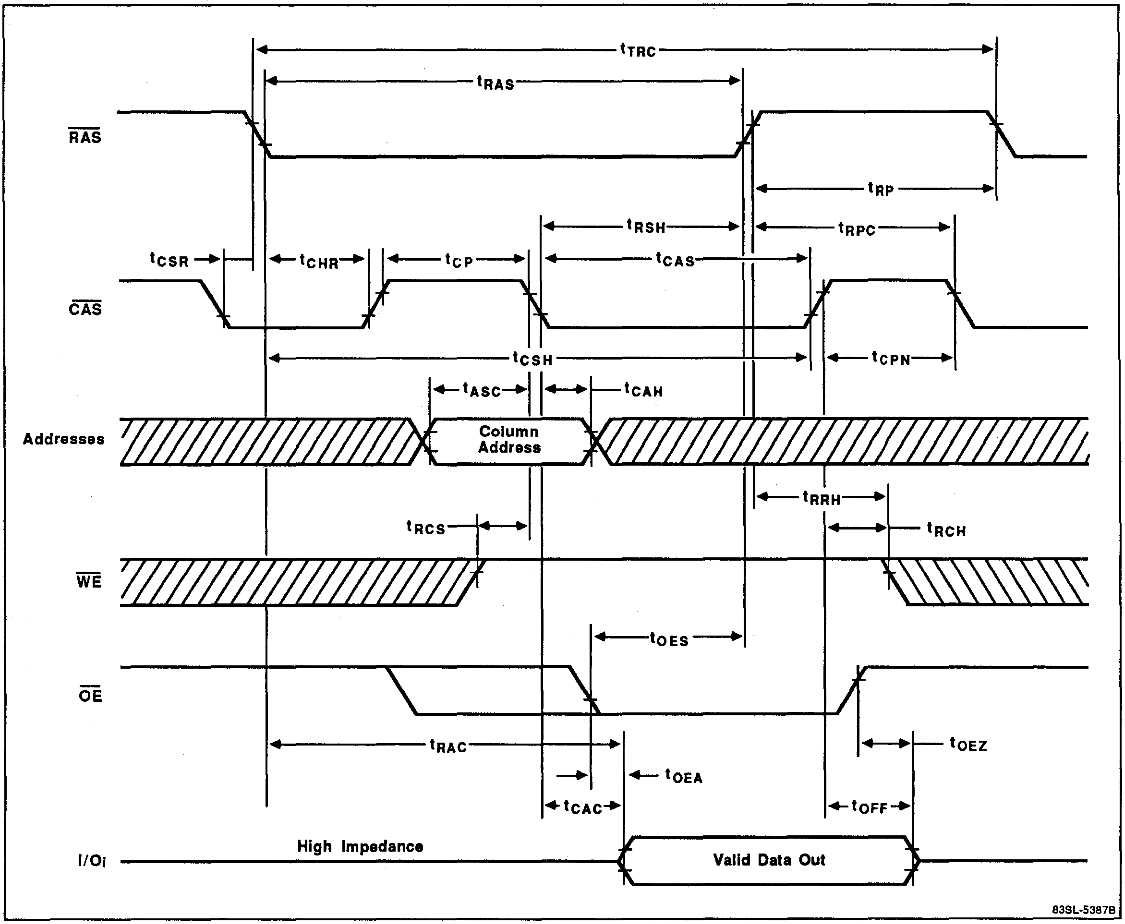
(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



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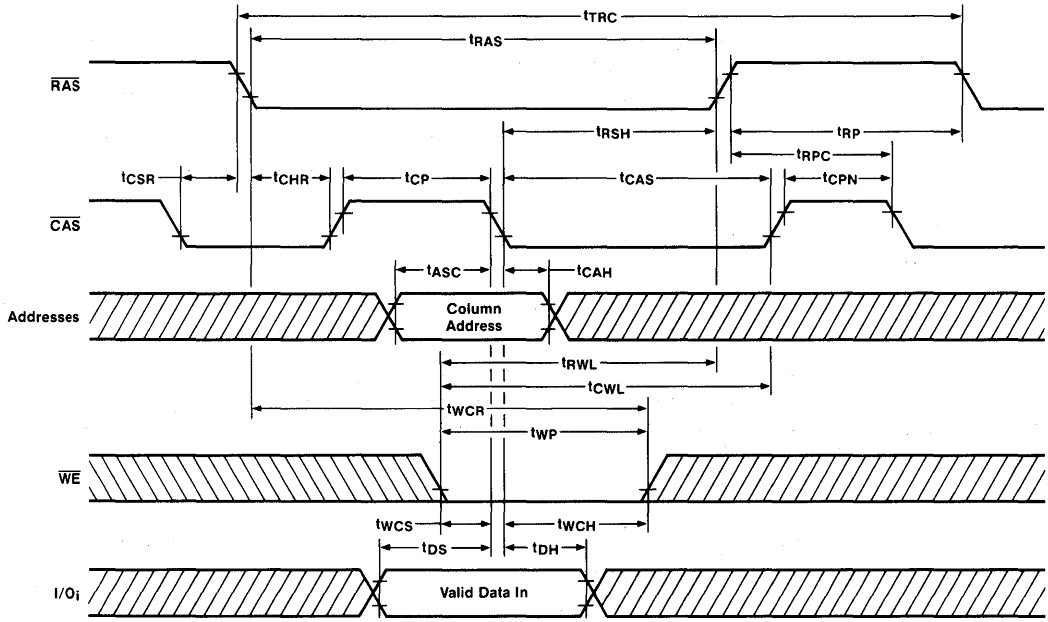
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle



Note:
[1] $\overline{OE}$ = don't care

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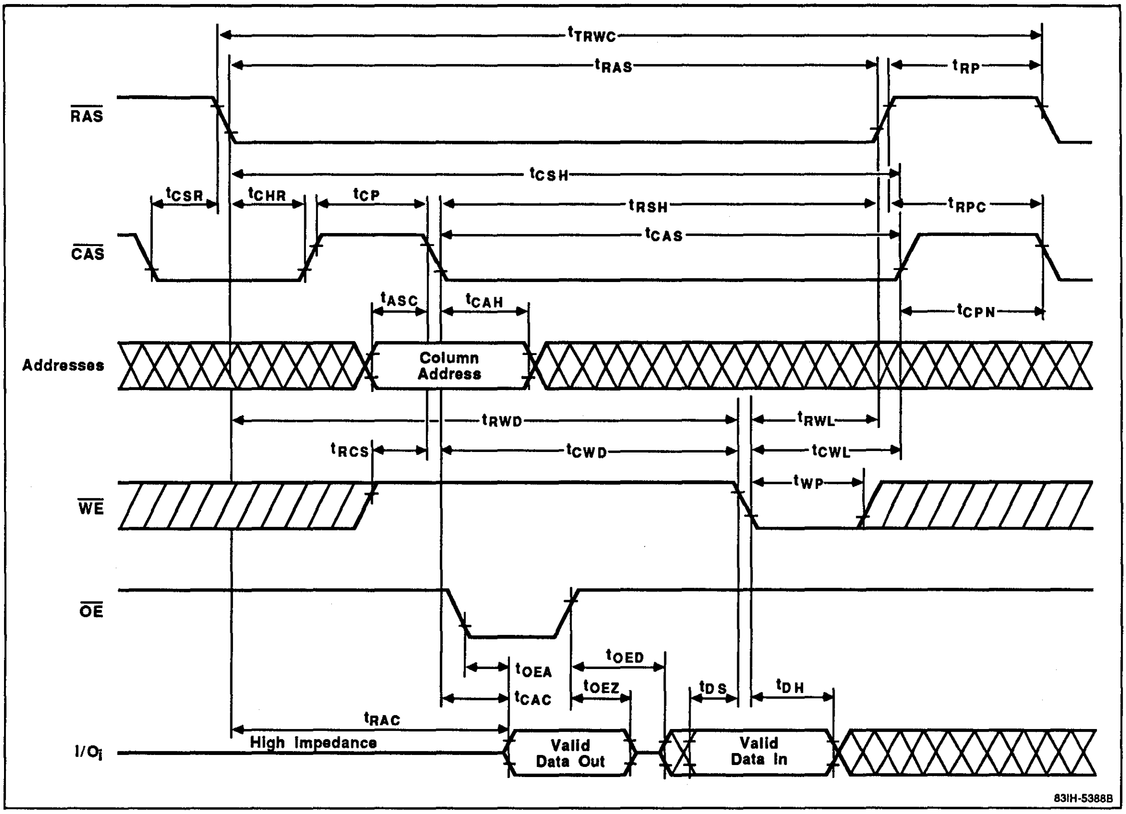
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



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μPD421000 1,048,576 x 1-BIT DYNAMIC CMOS RAM

Description

The μPD421000 is a fast-page, 1,048,576-word by 1-bit dynamic CMOS RAM designed to operate from a single +5-volt power supply. The device is fabricated with advanced polycide technology using trench capacitors to minimize silicon area and provide high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation. The negative-voltage substrate bias is automatically generated internally.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{\text{CAS}}$ low. The data output is returned to high impedance by returning $\overline{\text{CAS}}$ high. Fast-page read and write cycles can be executed by cycling $\overline{\text{CAS}}$.

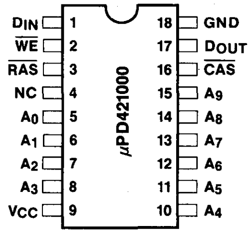
Refreshing may be accomplished by means of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle, enabling internal generation of the refresh address. Refreshing can also be accomplished by means of $\overline{\text{RAS}}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms refresh period.

Features

- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ Fast-page operation
- ☐ Low power dissipation:
  - — 70 mA max (active), 80 ns version
  - — 1 mA max (standby)
- ☐ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Nonlatched, three-state outputs
- ☐ Low input capacitance
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles during 8-ms period
- ☐ High-density 18-pin plastic DIP, 26/20-pin SOJ, or 20-pin plastic ZIP packaging

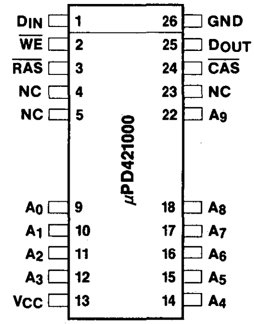
Pin Configurations

18-Pin Plastic DIP



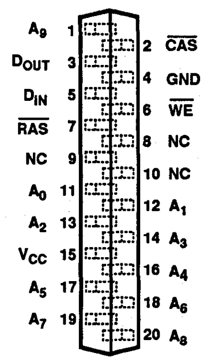
83-004648A

26/20-Pin Plastic SOJ



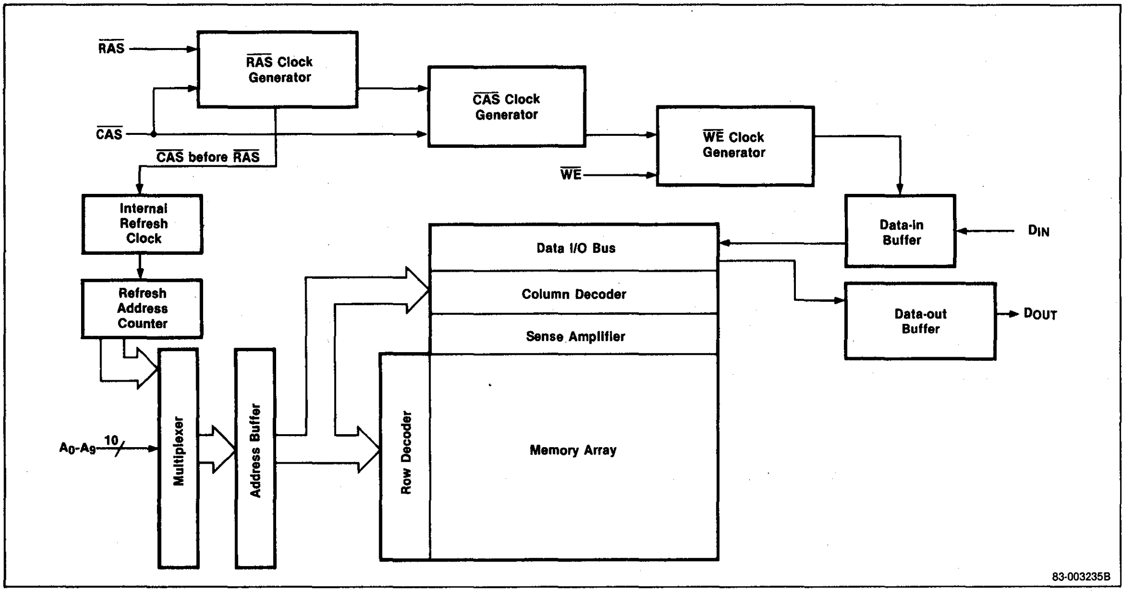
83-004649A

20-Pin Plastic ZIP



83IH-5377A

Block Diagram



Pin Identification

Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Page-Mode Cycle (min)	Package
μPD421000C-80	80 ns	160 ns	50 ns	18-pin plastic DIP
C-10	100 ns	190 ns	60 ns	
C-12	120 ns	220 ns	70 ns	
μPD421000LA-80	80 ns	160 ns	50 ns	26/20-pin plastic SOJ
LA-10	100 ns	190 ns	60 ns	
LA-12	120 ns	220 ns	70 ns	
μPD421000V-80	80 ns	160 ns	50 ns	20-pin plastic ZIP
V-10	100 ns	190 ns	60 ns	
V-12	120 ns	220 ns	70 ns	

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current	50 mA
Power dissipation, P_D	1W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			3.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
				1.0	mA	$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OH} = −5 mA

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	6	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD421000-80		μPD421000-10		μPD421000-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		70		60		50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		60		50		40	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Note 6)
Page cycle time	t_{PC}	50		60		70		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10, 11)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		65	ns	(Notes 7, 11)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 12)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD421000-80		μPD421000-10		μPD421000-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{RAS}$ pulse width (page cycle)	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		15		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	10	20	10	25	15	30	ns	(Note 11)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	(Note 11)
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 18)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		120		ns	(Note 18)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		25		30		ns	(Note 18)
Column address to $\overline{WE}$ delay time	t_{AWD}	45		50		60		ns	(Note 18)

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD421000-80		μPD421000-10		μPD421000-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		25		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

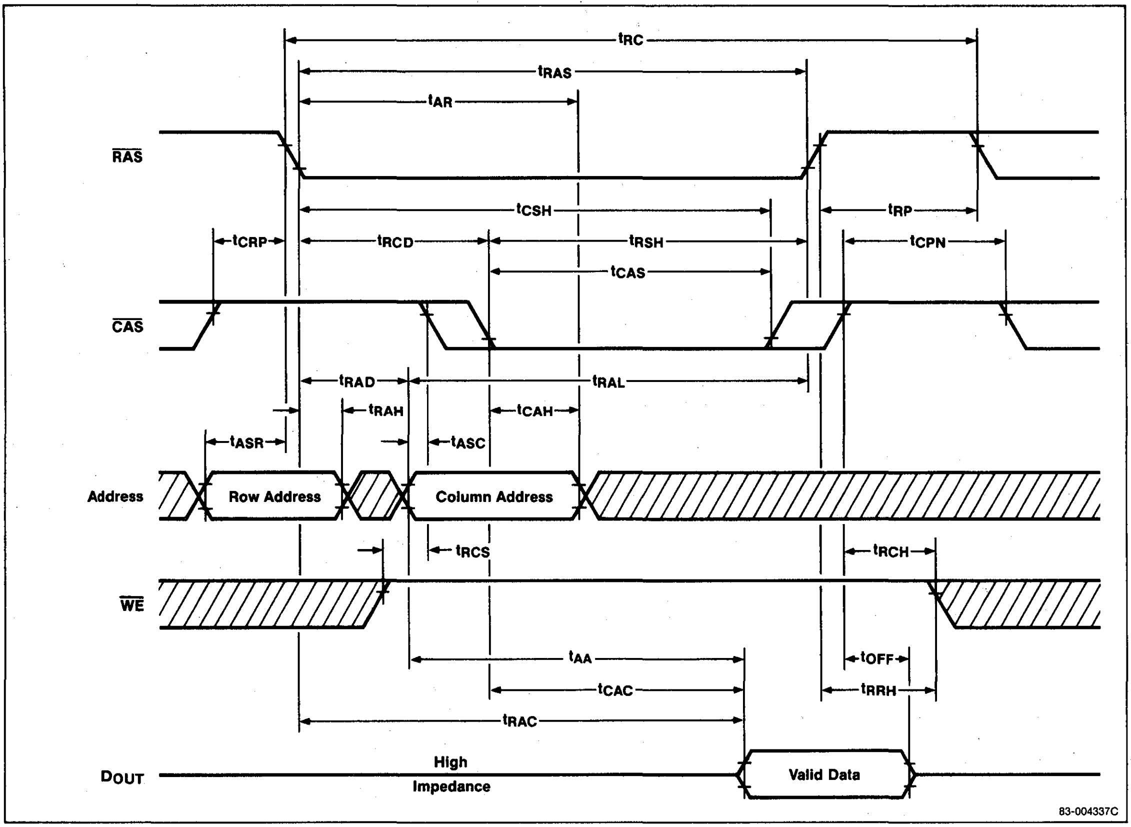
(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

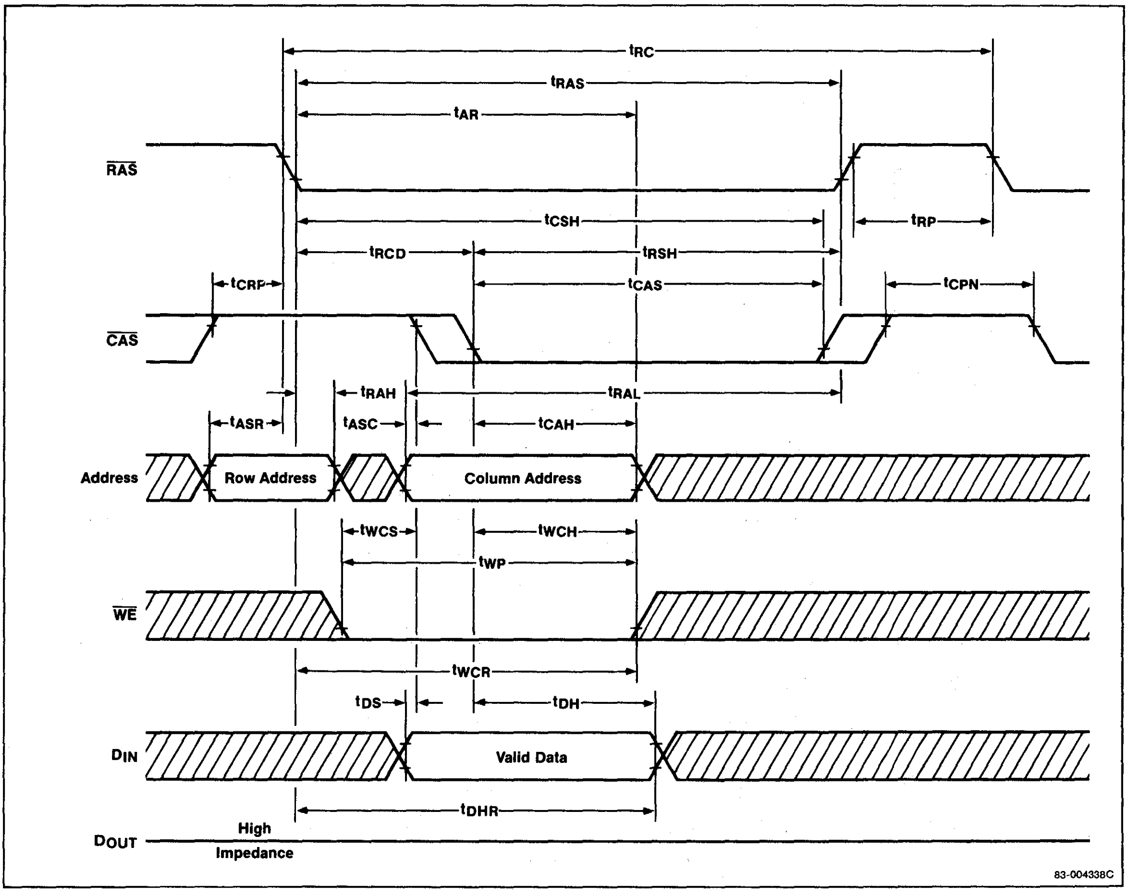
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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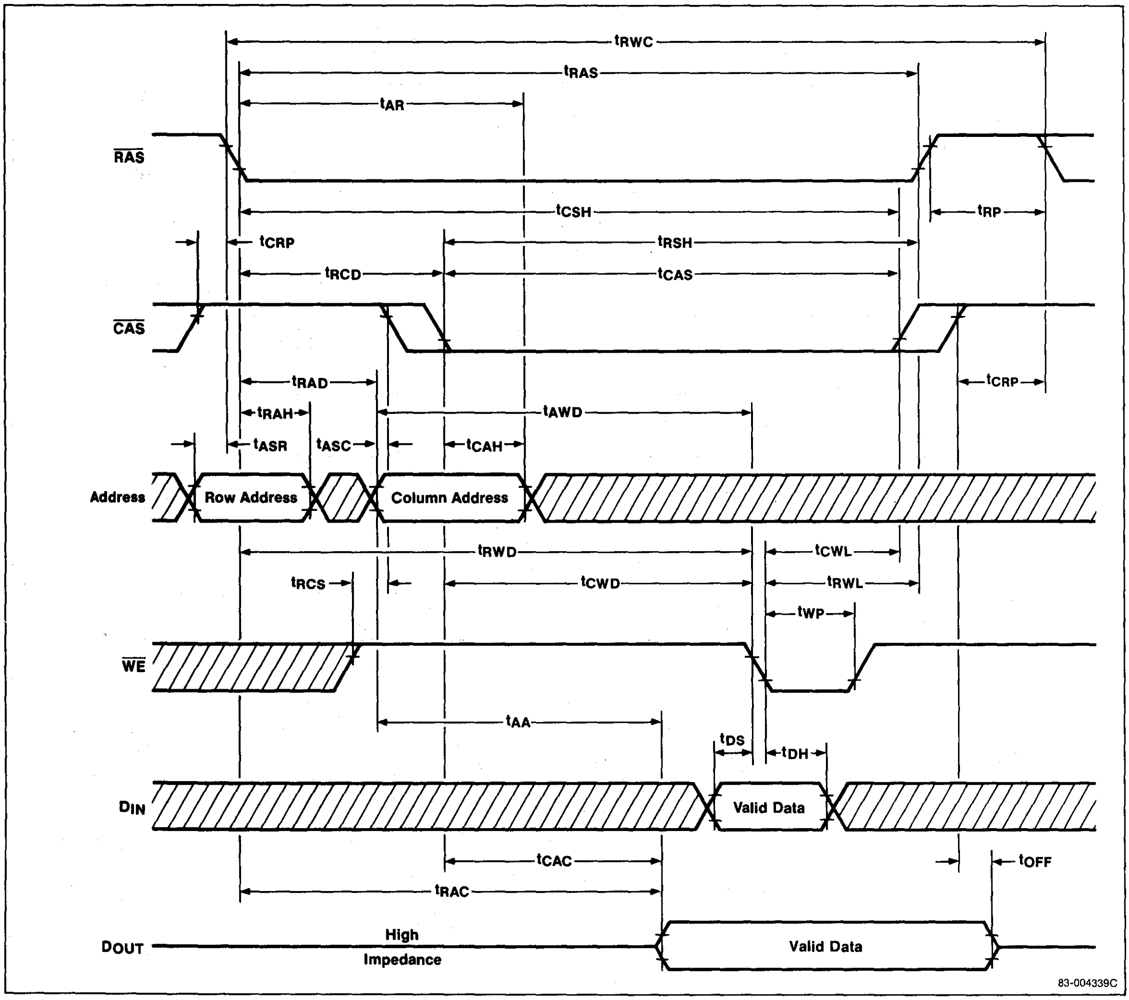
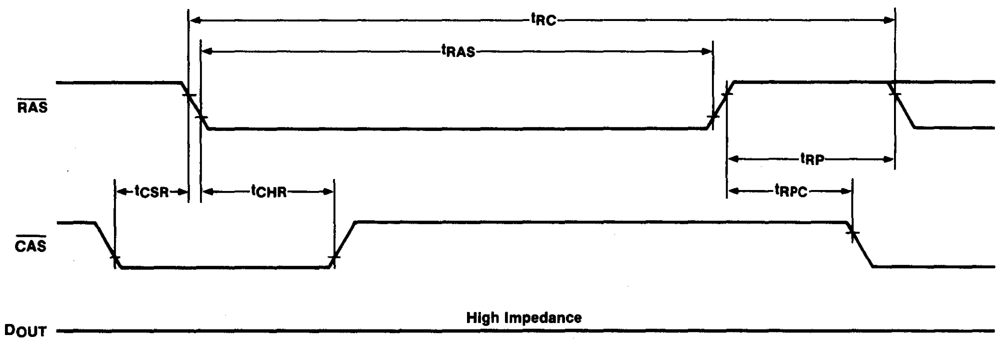
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

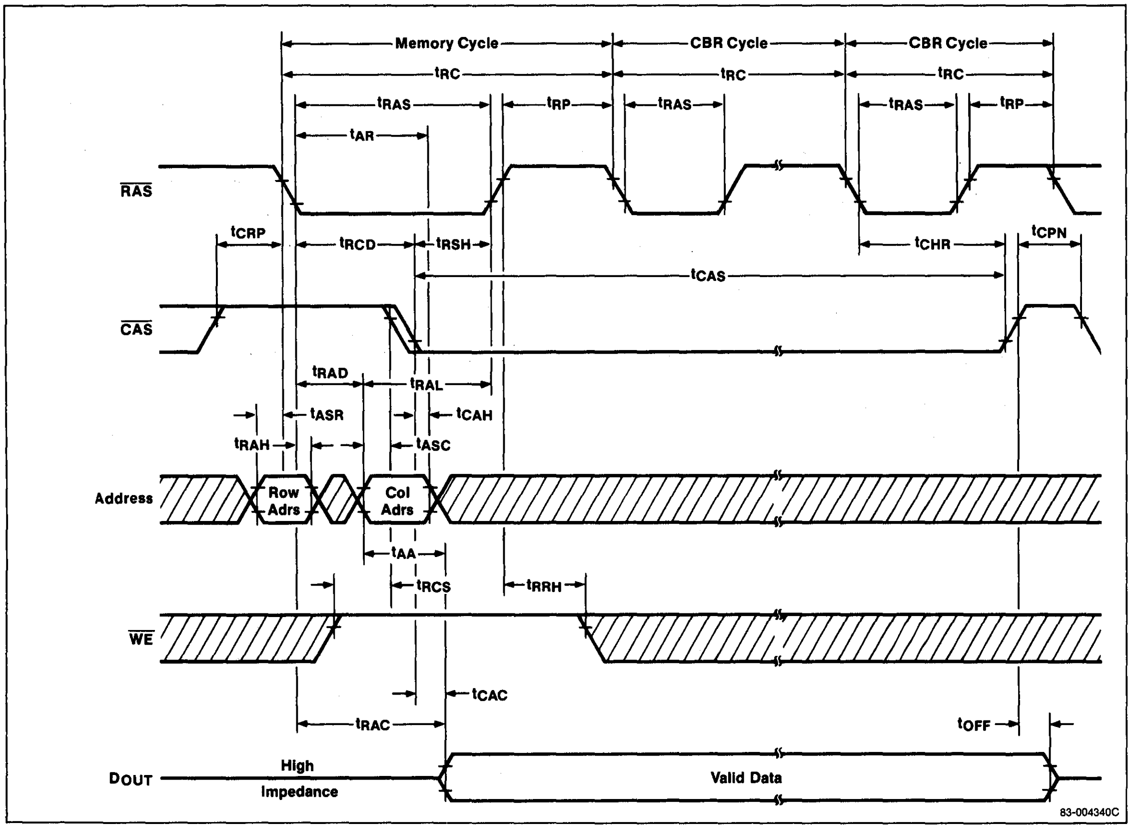
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

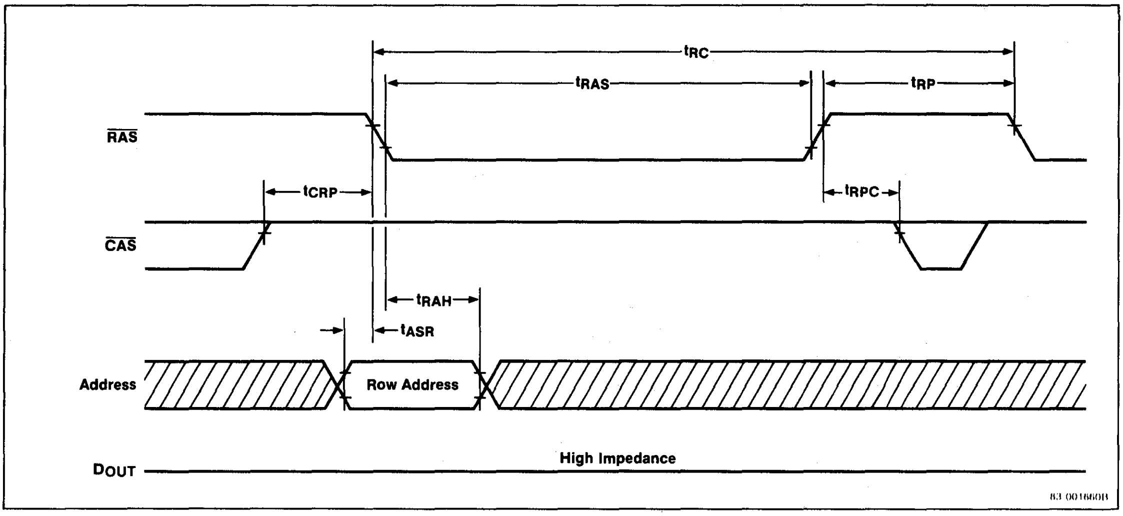
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



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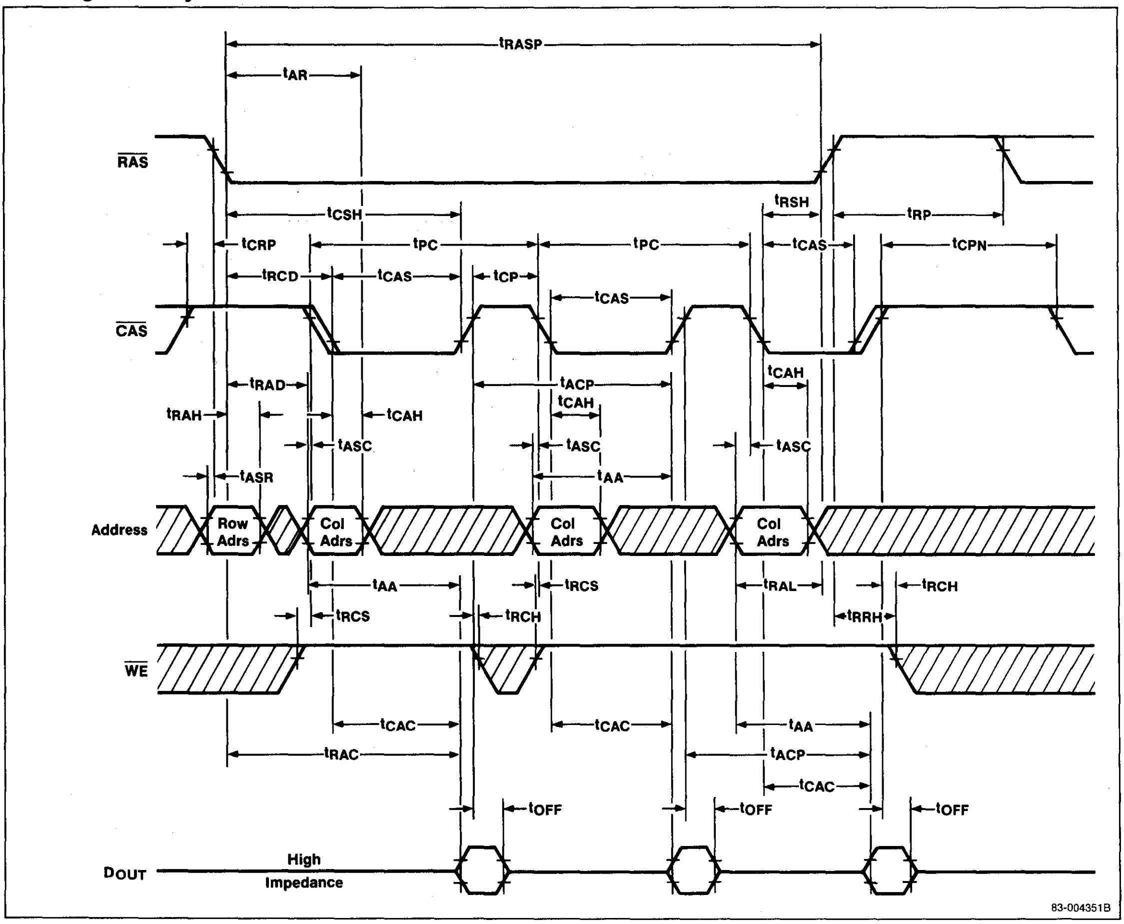
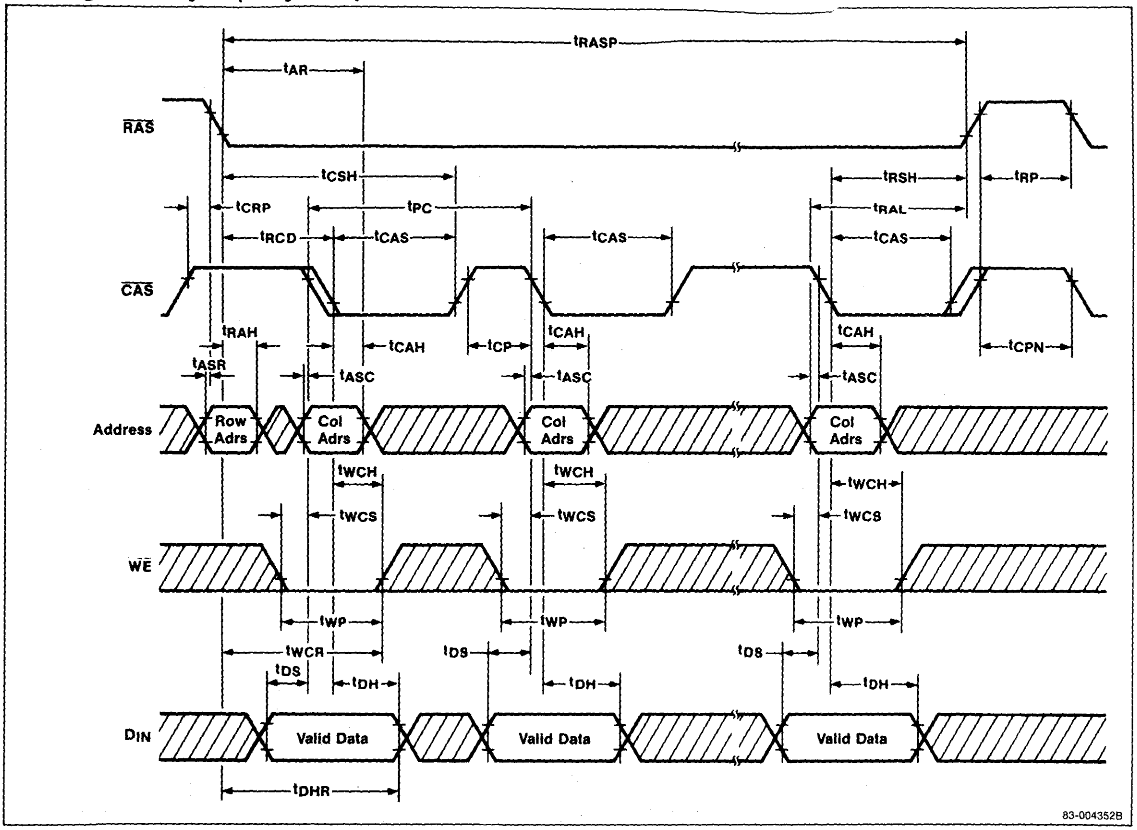
Timing Waveforms (cont)

Fast-Page Read Cycle



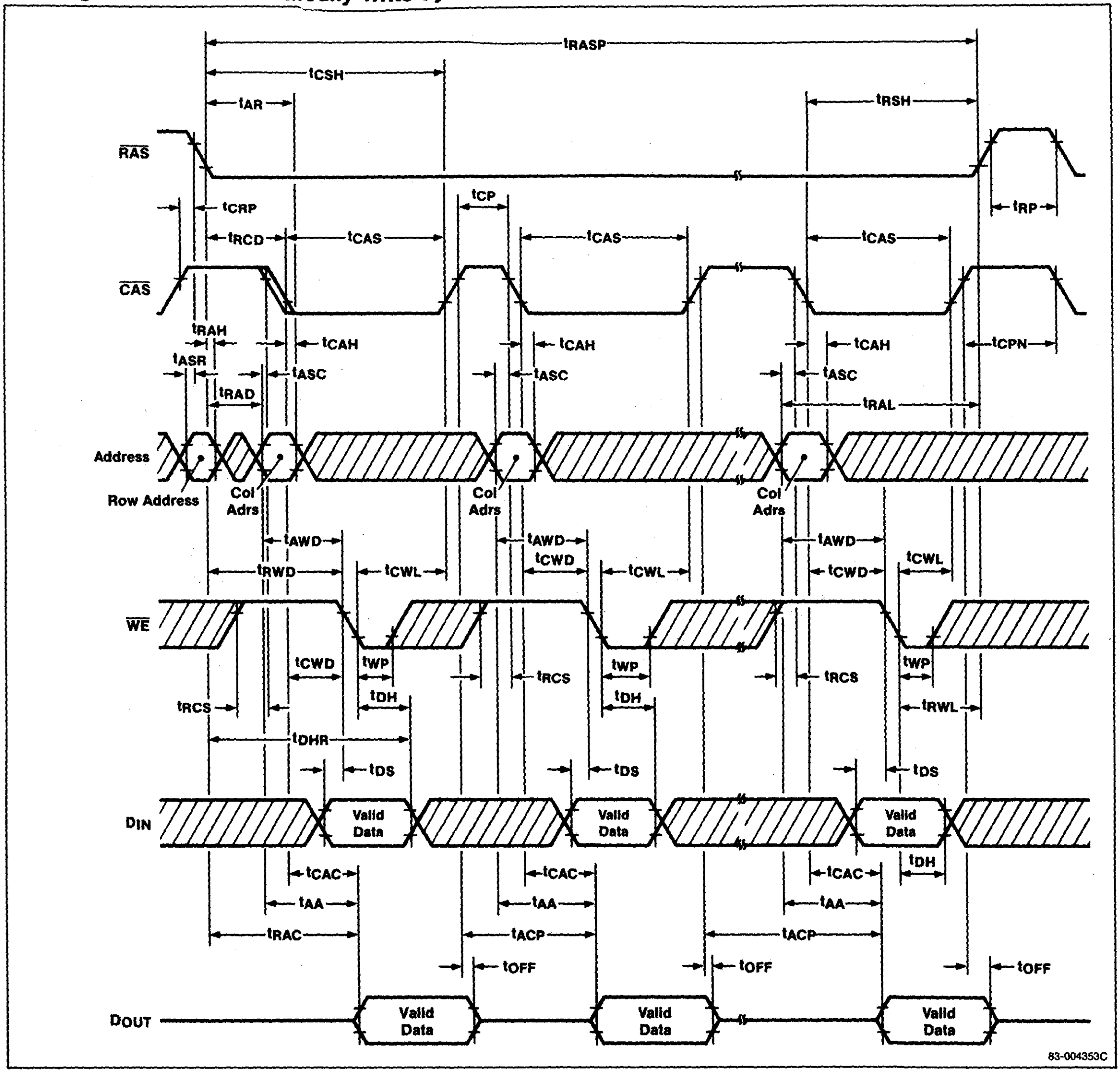
Timing Waveforms (cont)

Fast-Page Write Cycle (Early Write)



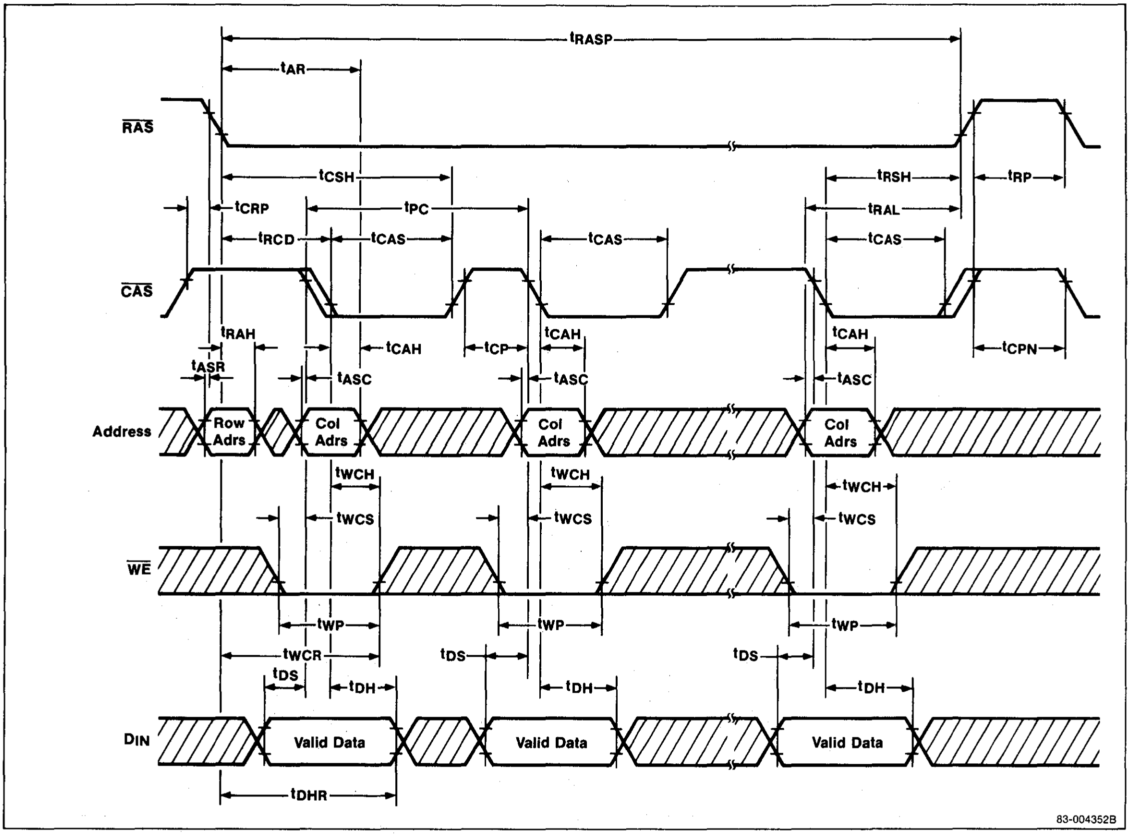
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Fast-Page Write Cycle (Early Write)



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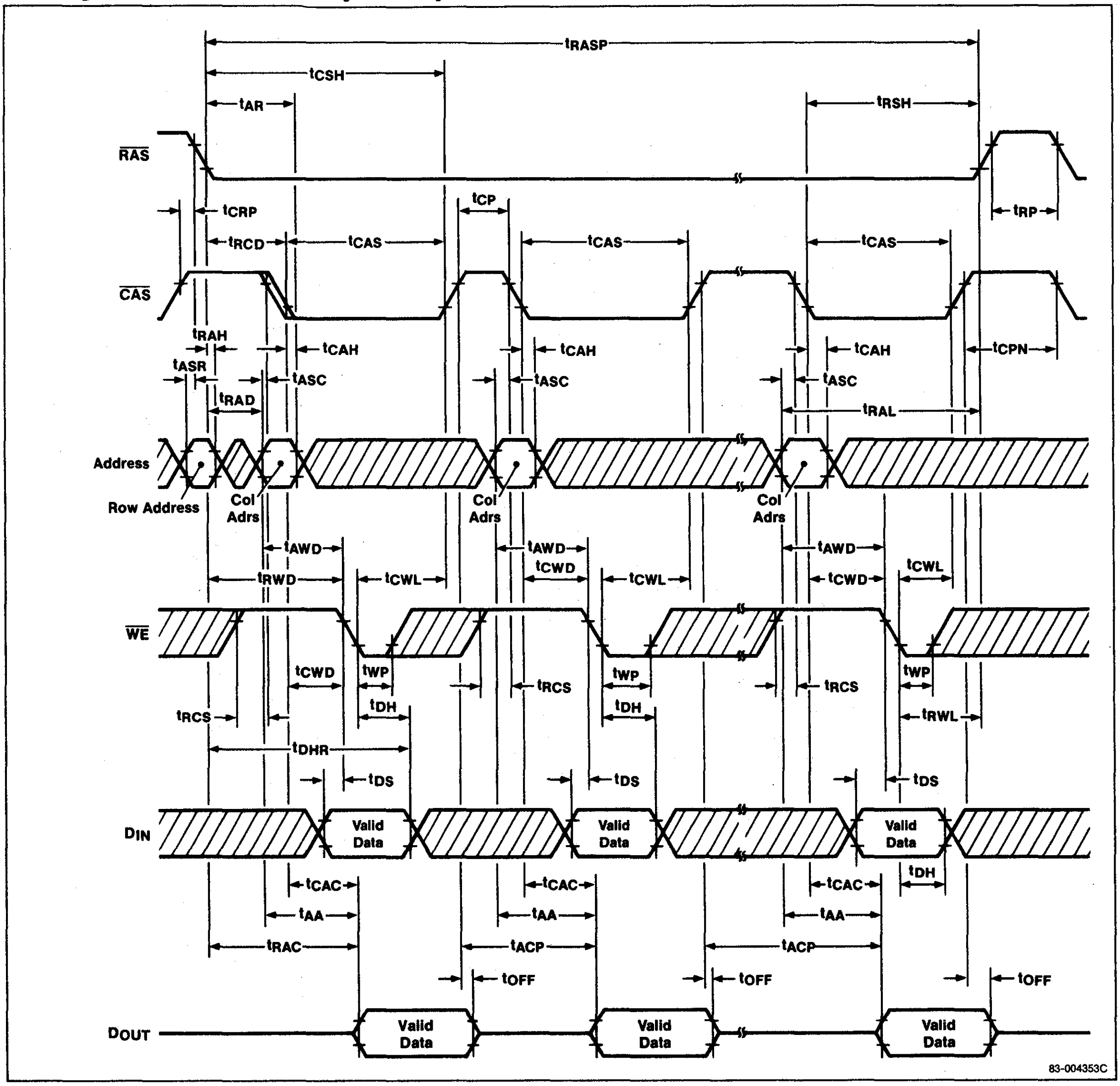
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



NEC
NEC Electronics Inc.

μPD421001
1,048,576 x 1-BIT DYNAMIC CMOS RAM

Description

The μPD421001 is a nibble version, 1,048,576-word by 1-bit dynamic CMOS RAM designed to operate from a single +5-volt power supply. Advanced polycide technology using trench capacitors to minimize silicon area provides high storage cell capacity, high performance, and high reliability. The device also uses a single-transistor dynamic storage cell and advanced CMOS circuitry throughout, ensuring minimum power dissipation. The negative-voltage substrate bias is automatically generated internally.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{\text{CAS}}$ low. Data output is returned to high impedance by returning $\overline{\text{CAS}}$ high. The device is capable of executing nibble read and write cycles by cycling $\overline{\text{CAS}}$.

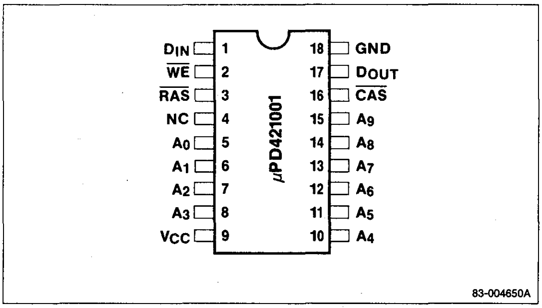
Refreshing may be accomplished by means of $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles, enabling internal generation of the refresh address. Refreshing can also be accomplished by means of $\overline{\text{RAS}}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

Features

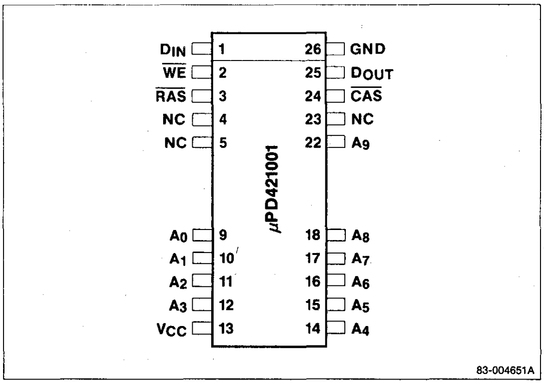
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ Nibble operation
- ☐ Low power dissipation:
  - — 70 mA max (active), 80 ns version
  - — 1 mA max (standby)
- ☐ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Nonlatched, three-state outputs
- ☐ Low input capacitance
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles during 8-ms period
- ☐ High-density 18-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

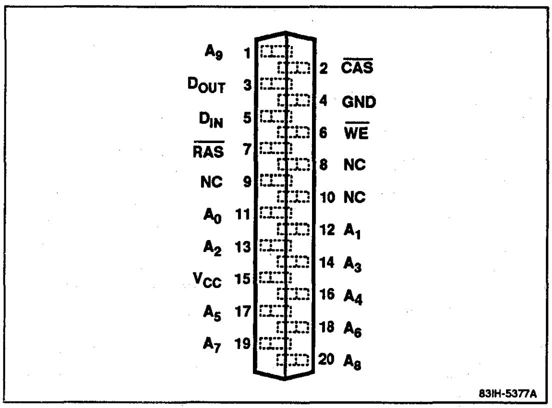
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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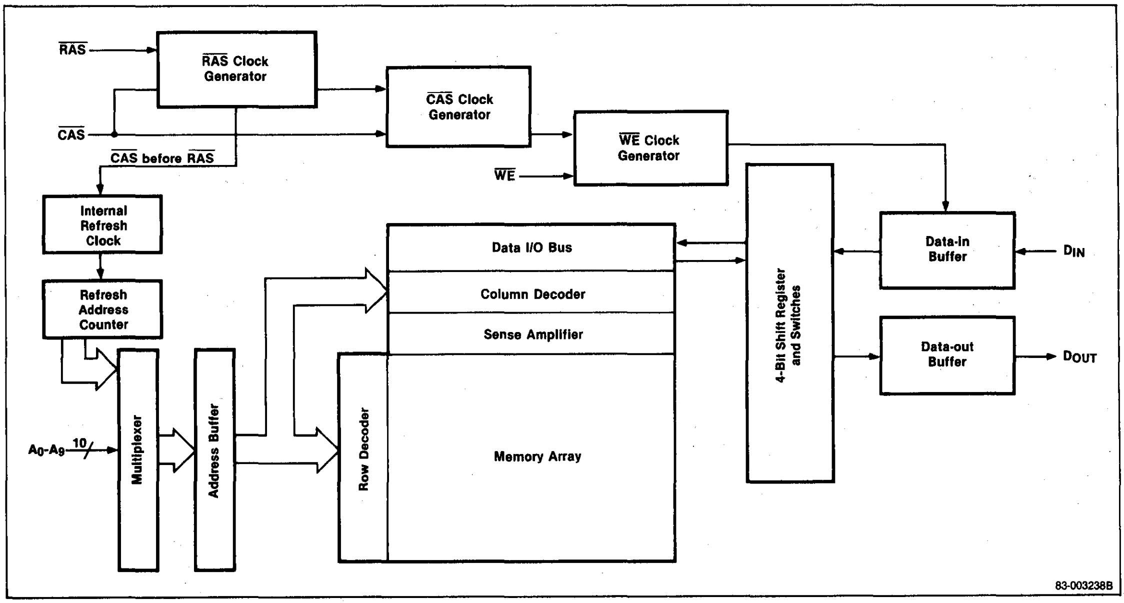
Block Diagram



Pin Identification

Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Nibble-Mode Cycle (min)	Package
μPD421001C-80	80 ns	160 ns	40 ns	18-pin plastic DIP
C-10	100 ns	190 ns	45 ns	
C-12	120 ns	220 ns	55 ns	
μPD421001LA-80	80 ns	160 ns	40 ns	26/20-pin plastic SOJ
LA-10	100 ns	190 ns	45 ns	
LA-12	120 ns	220 ns	55 ns	
μPD421001V-80	80 ns	160 ns	40 ns	20-pin plastic ZIP
V-10	100 ns	190 ns	45 ns	
V-12	120 ns	220 ns	55 ns	

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current	50 mA
Power dissipation, P_D	1W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			3.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
				1.0	mA	$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OH} = −5 mA

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	6	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

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AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	μPD421001-80 Min	μPD421001-80 Max	μPD421001-10 Min	μPD421001-10 Max	μPD421001-12 Min	μPD421001-12 Max	Unit	Test Conditions
Operating current, average	I_{CC1}		70		60		50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from falling edge of $\overline{CAS}$ (non-nibble cycle)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 16)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 16)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ pulse width (nibble cycle)	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width (non-nibble cycle)	t_{CAS}	20	10000	25	10000	30	10000	ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD421001-80		μPD421001-10		μPD421001-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time (non-nibble cycle)	t_{CPN}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 16)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time (non-nibble cycle)	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		120		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay (non-nibble cycle)	t_{CWD}	20		25		30		ns	(Note 15)
Column address to $\overline{WE}$ delay time	t_{AWD}	45		50		60		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		25		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		μPD421001-80		μPD421001-10		μPD421001-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Nibble Mode									
Operating current, average (nibble cycle)	I_{CC4}		60		50		40	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{NC} = t_{NC}$ min (Note 5)
Nibble cycle time	t_{NC}	40		45		55		ns	(Note 6)
Nibble access time	t_{NAC}		20		25		30	ns	(Note 7)
$\overline{CAS}$ precharge time (nibble cycle)	t_{NP}	10		10		15		ns	
$\overline{CAS}$ pulse width (nibble cycle)	t_{NAS}	20		25		30		ns	
$\overline{RAS}$ hold time (nibble read cycle)	t_{NRRSH}	20		25		30		ns	
$\overline{RAS}$ hold time (nibble write cycle)	t_{NWRSH}	20		25		30		ns	
$\overline{CAS}$ to $\overline{WE}$ delay (nibble cycle)	t_{NCWD}	20		25		30		ns	(Note 15)
Write command to $\overline{CAS}$ lead time (nibble cycle)	t_{NCWL}	20		25		30		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

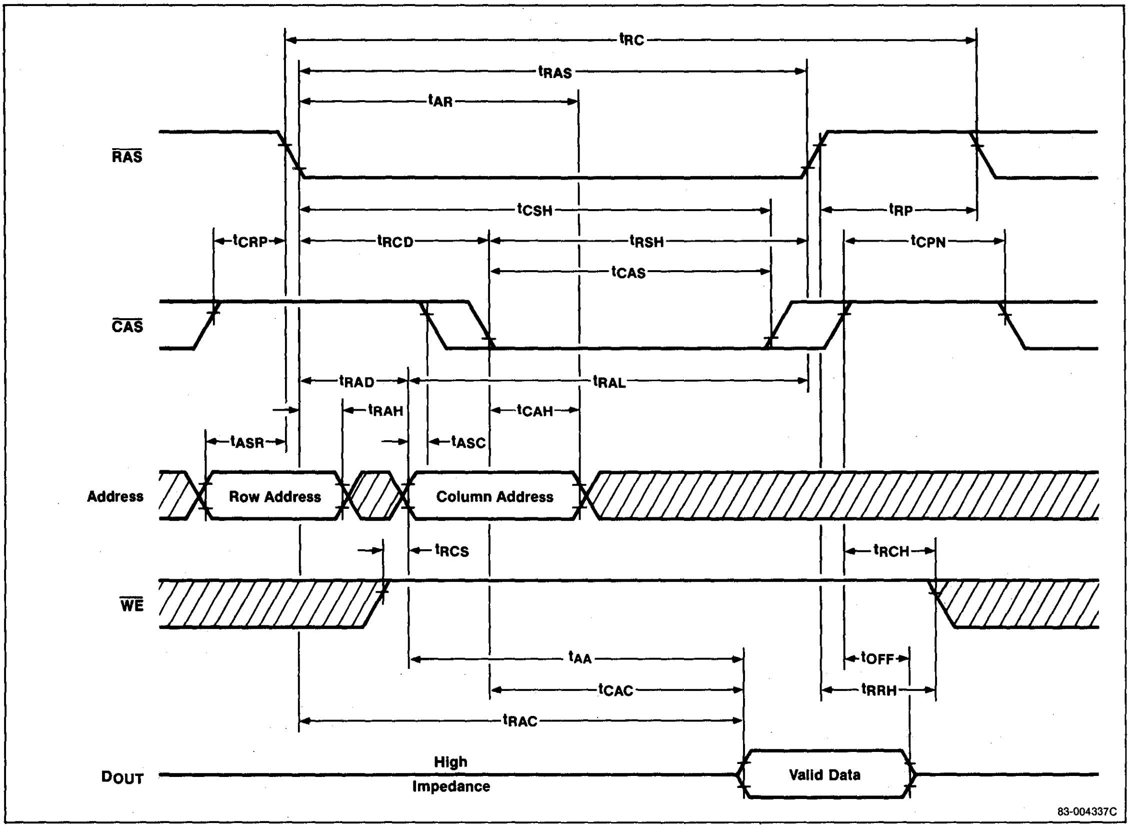
(15) t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{NCWD} are restrictive operating parameters in read-write/read-modify-write and nibble read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write or nibble early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If $t_{NCWD} \geq t_{NCWD}$ (min), the cycle is a nibble read-write cycle and the data output will contain data read from the selected cell. If none of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(16) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(17) Parameter t_{WP} is applicable for a delayed write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

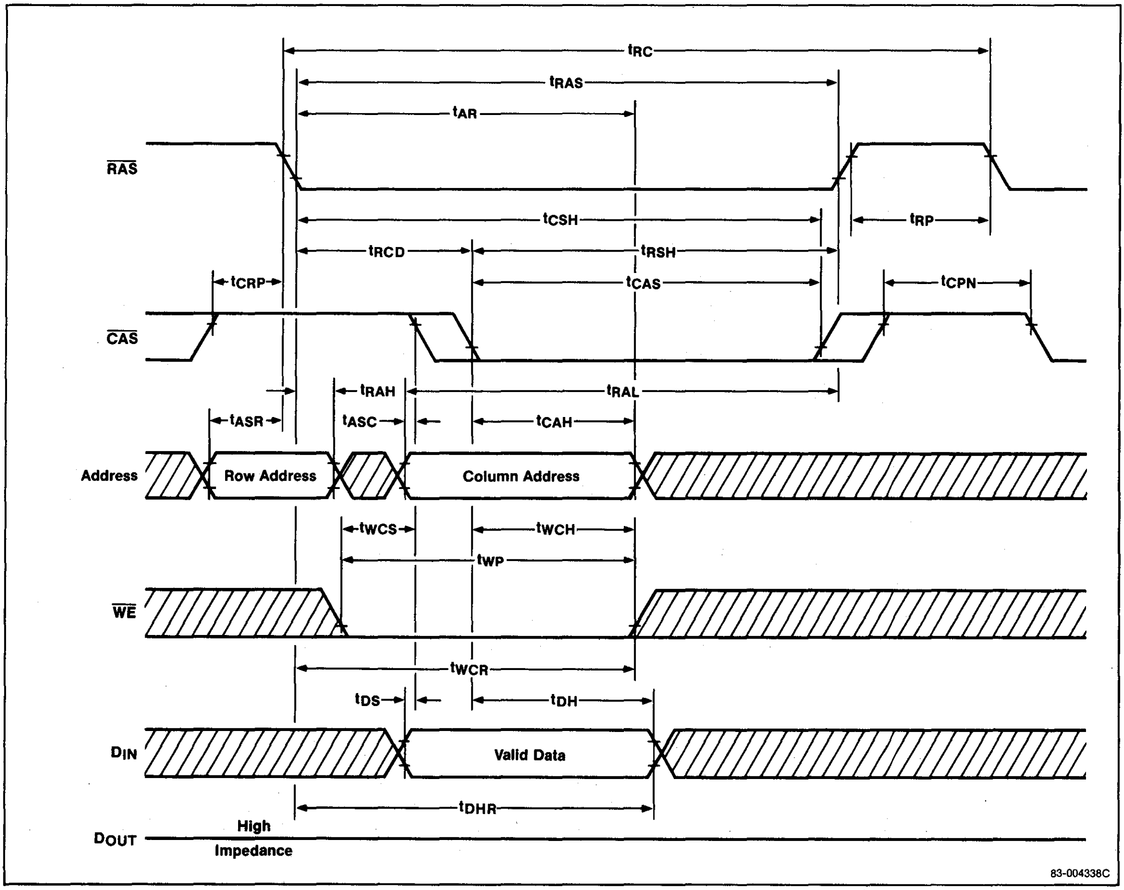
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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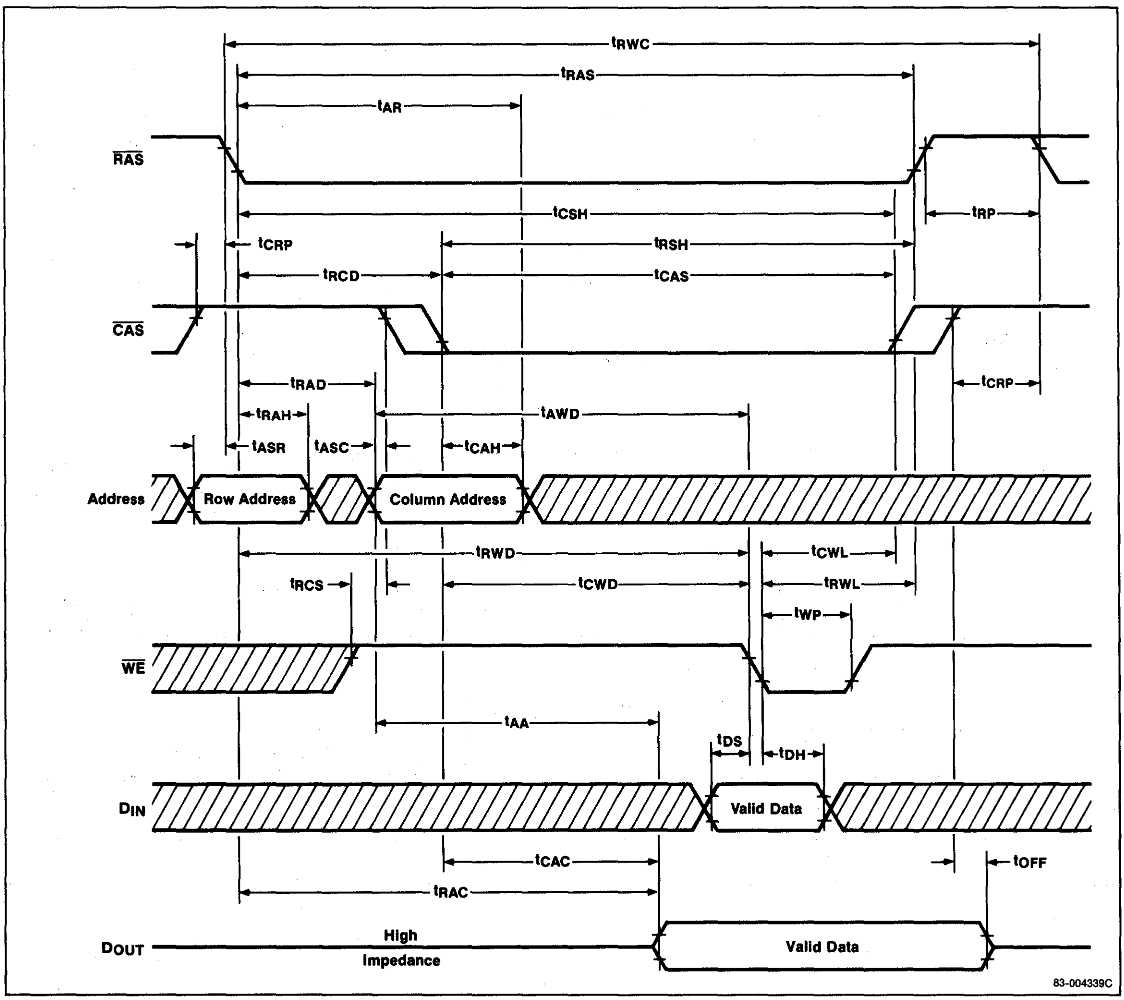
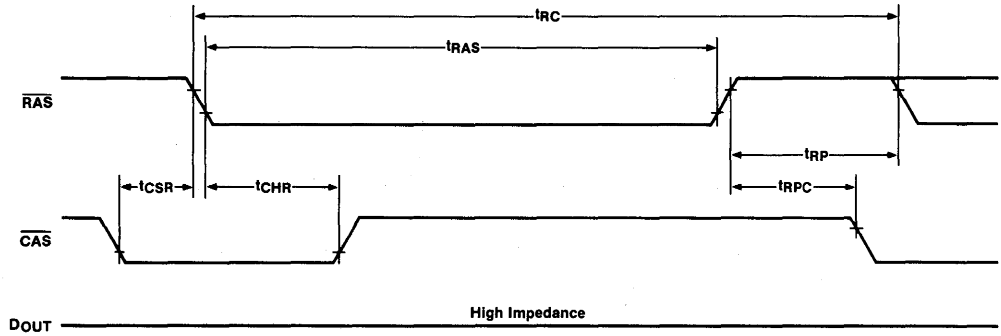
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

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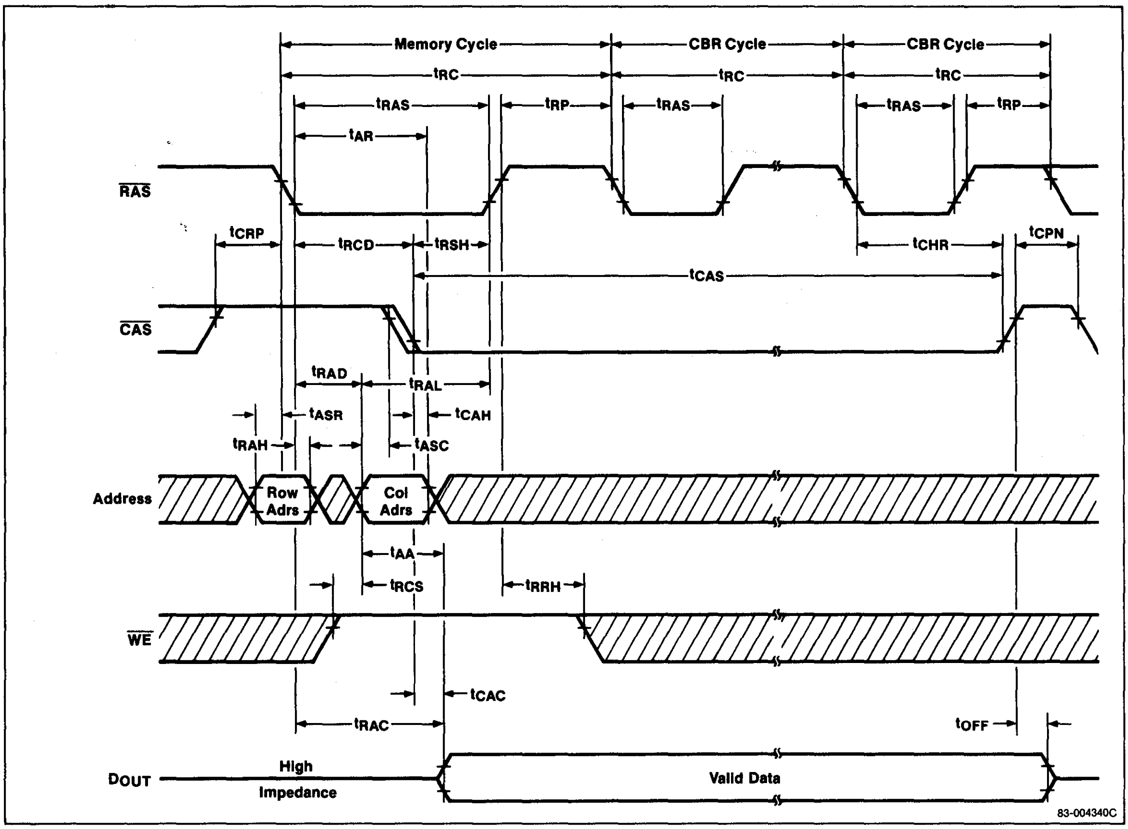
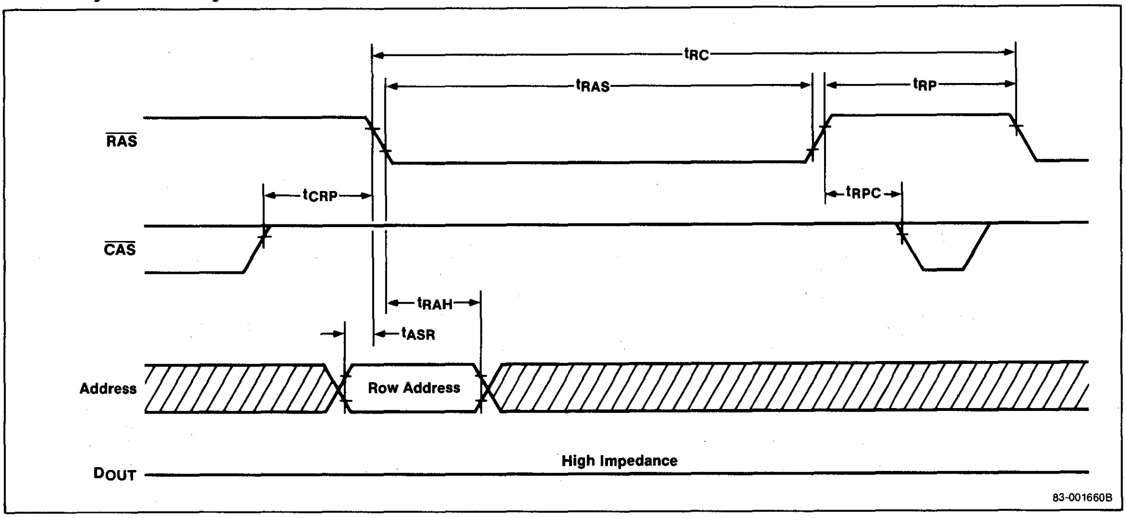
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

RAS-Only Refresh Cycle



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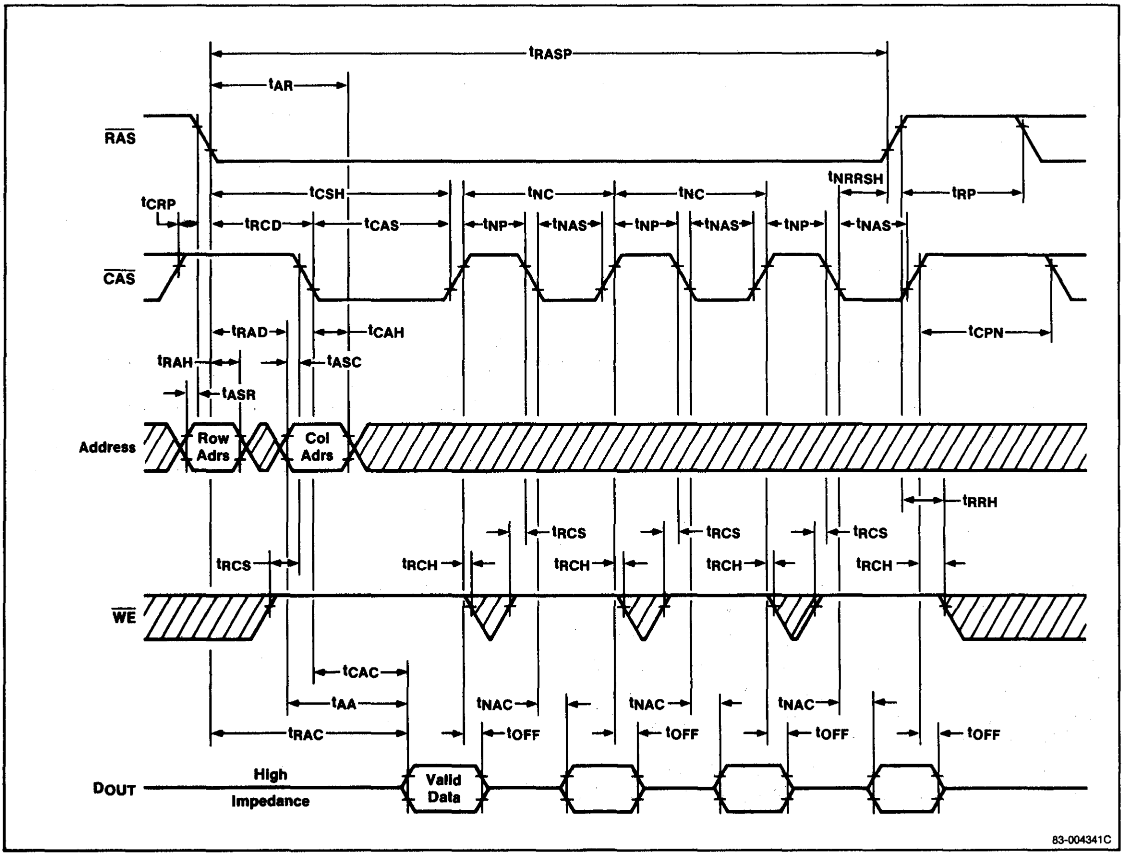
Nibble Mode

The μPD421001 is capable of executing nibble read, write, or read-modify-write cycles. Nibble mode allows high-speed serial access of a maximum of 4 data bits. The first bit is determined by the row and column addresses, and the next bits are accessed automatically by cycling CAS while RAS is held low. The addresses of nibble bits are determined by the combination of row address A_9 and column address A_9 in the following sequence.

		Row Address										Column Address										
Sequence	Nibble Bit	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
RAS/CAS	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Example: external address input
CAS cycling	2	1	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Internal address generated
CAS cycling	3	0	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
CAS cycling	4	1	0	1	0	0	0	1	0	1	0	1	1	1	0	1	0	1	0	0	0	
CAS cycling	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1	0	0	0	Repeated sequence

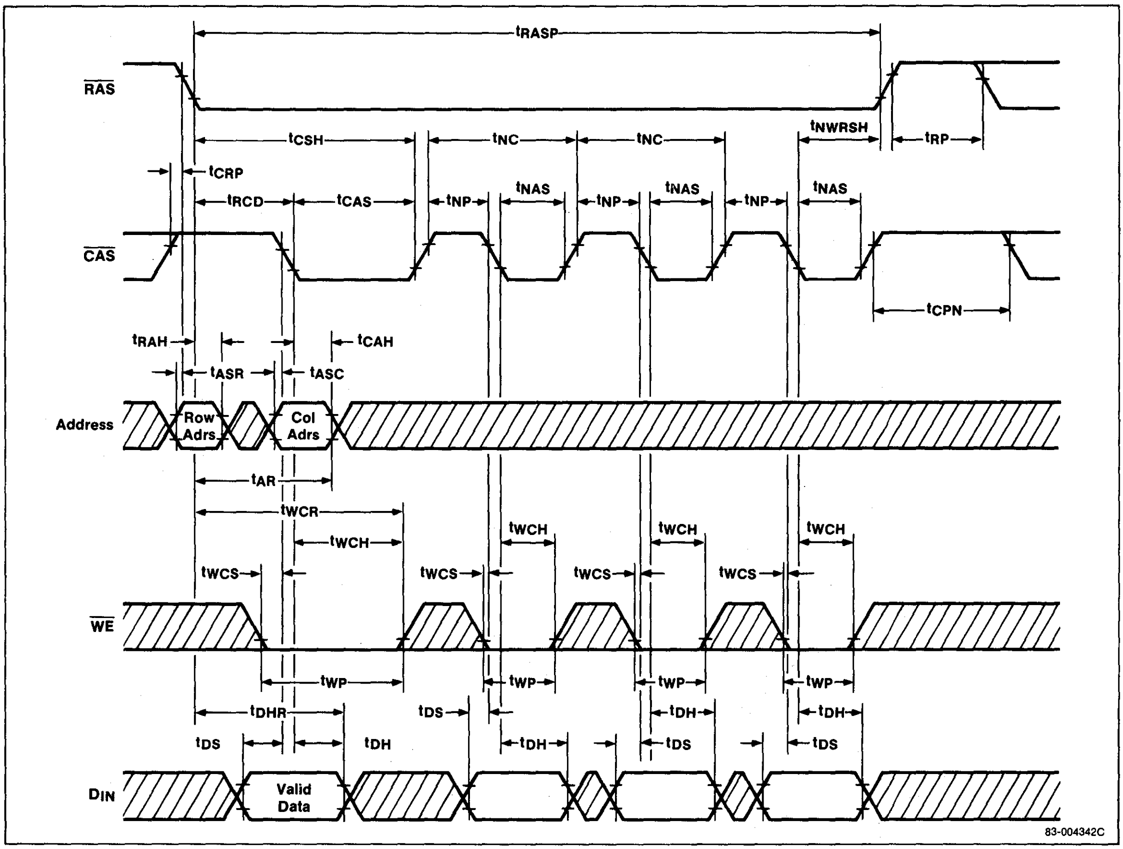
Timing Waveforms (cont)

Nibble Mode Read Cycle



Timing Waveforms (cont)

Nibble Mode Write Cycle (Early Write)



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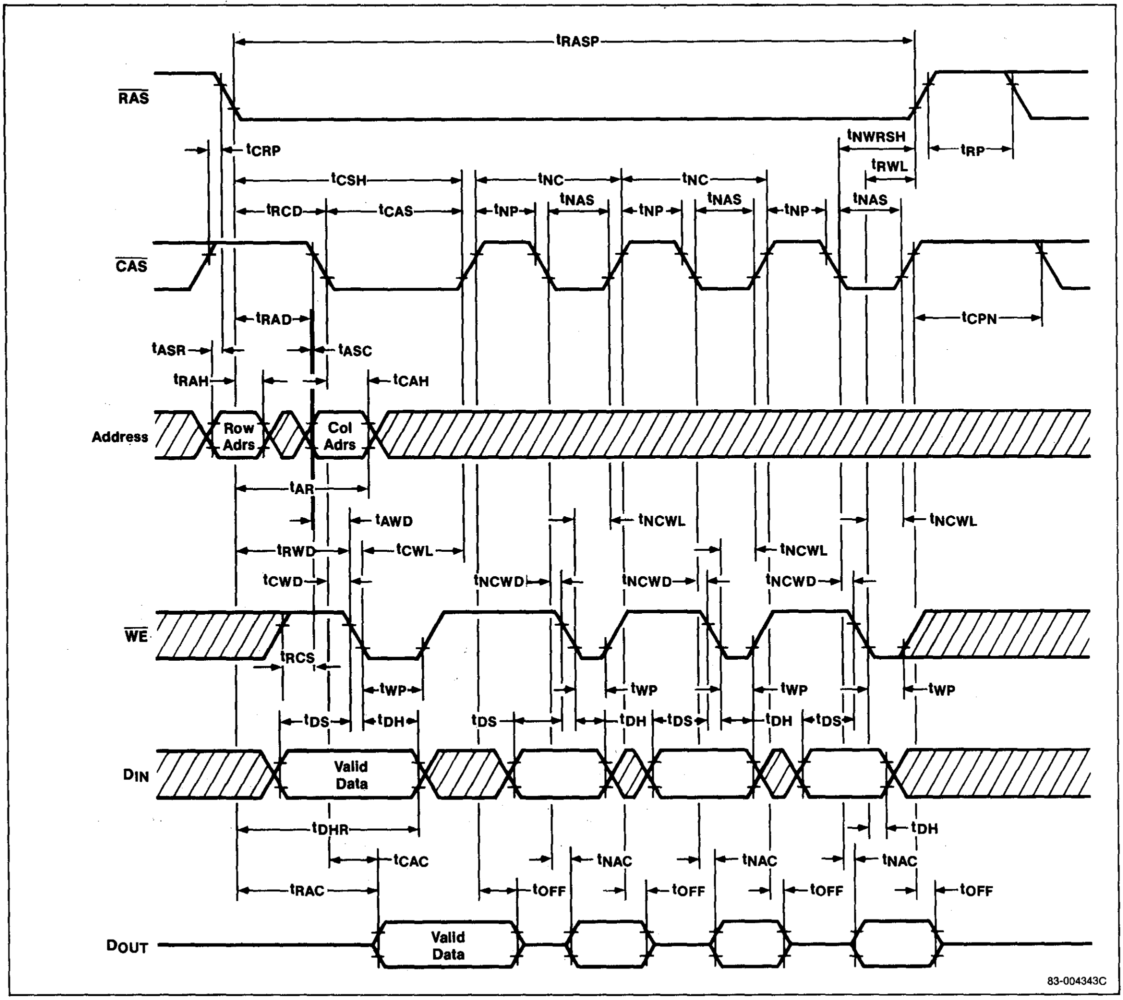
NEC

Timing Waveforms (cont)

Nibble Mode Read-Write/Read-Modify-Write Cycle



NEC
NEC Electronics Inc.

μPD421002 1,048,576 x 1-BIT DYNAMIC CMOS RAM

PRELIMINARY INFORMATION

Description

The μPD421002 is a static-column, 1,048,576-word by 1-bit dynamic CMOS RAM designed to operate from a single +5-volt power supply. The device is fabricated with advanced polycide technology using trench capacitors to minimize silicon area and provide high storage cell capacity, high performance, and high reliability. The μPD421002 uses a single-transistor dynamic storage cell and advanced CMOS circuitry throughout, ensuring minimum power dissipation. The negative-voltage substrate bias is automatically generated internally.

The three-state output is controlled by $\overline{\text{CS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{\text{CS}}$ low. The data output is returned to a state of high impedance by returning $\overline{\text{CS}}$ to a high logic level. The device is capable of executing static-column read and write cycles by switching the column address inputs.

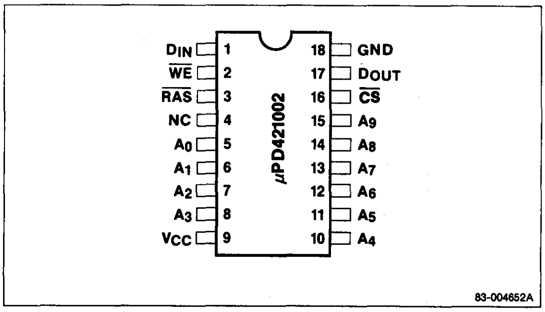
Refreshing may be accomplished by means of a $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ cycle, enabling internal generation of the refresh address. Refreshing can also be accomplished by means of $\overline{\text{RAS}}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms refresh period.

Features

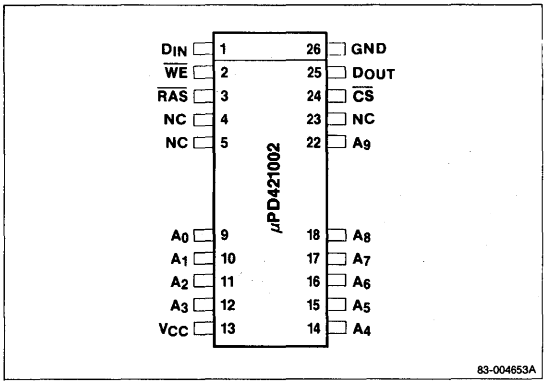
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ Static-column operation
- ☐ Low power dissipation
  - — 70 mA max (active), 80 ns version
  - — 1 mA max (standby)
- ☐ $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refreshing
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Nonlatched, three-state outputs
- ☐ Low input capacitance
- ☐ TTL-compatible inputs and outputs
- ☐ 512 refresh cycles during 8-ms period
- ☐ High-density 18-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

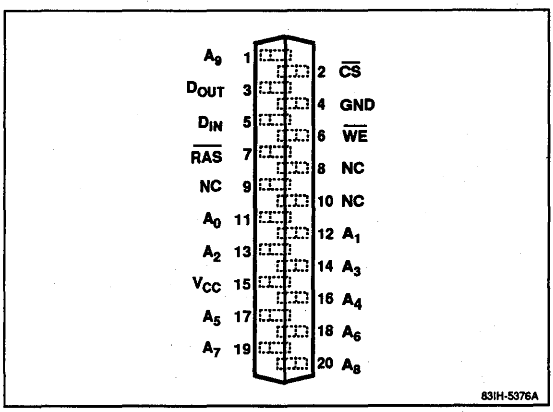
18-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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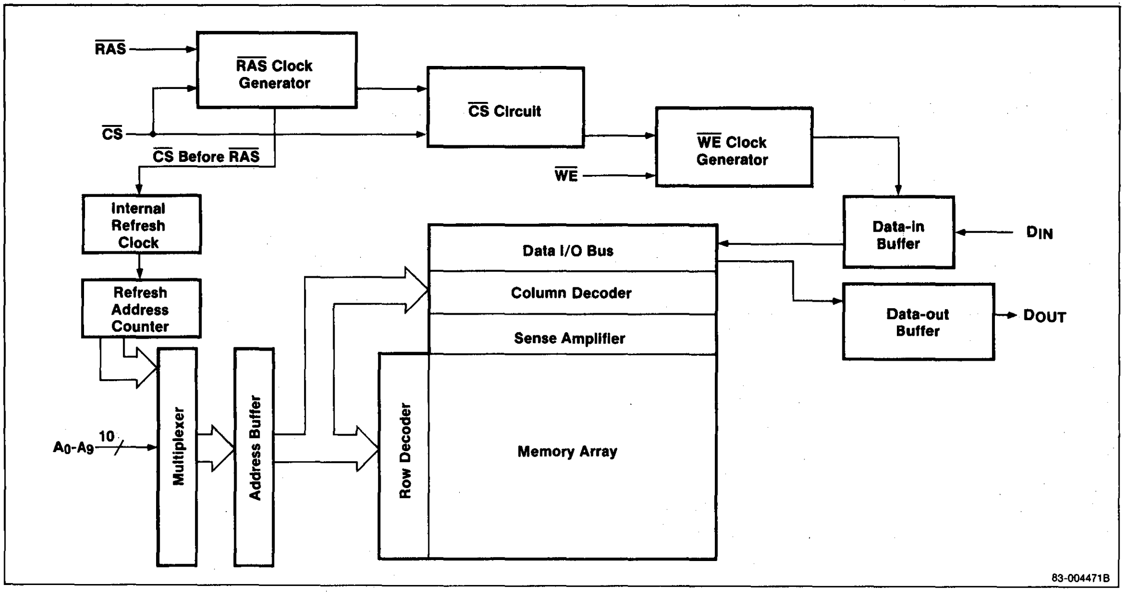
Block Diagram



Pin Identification

Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Static Column Cycle (min)	Package
μPD421002C-80	80 ns	160 ns	50 ns	18-pin plastic DIP
C-10	100 ns	190 ns	60 ns	
C-12	120 ns	220 ns	70 ns	
μPD421002LA-80	80 ns	160 ns	50 ns	26/20-pin plastic SOJ
LA-10	100 ns	190 ns	60 ns	
LA-12	120 ns	220 ns	70 ns	
μPD421002V-80	80 ns	160 ns	50 ns	20-pin plastic ZIP
V-10	100 ns	190 ns	60 ns	
V-12	120 ns	220 ns	70 ns	

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	Referenced to GND
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			3.0	mA	$\overline{RAS} = \overline{CS} = V_{IH}$
				1.0	mA	$\overline{RAS} = \overline{CS} = V_{CC} - 0.2$
Input leakage current	$I_{I(L)}$	−10		10	μA	$V_{IN} = 0$ to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	$I_{OL} = 4.2$ mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	$I_{OH} = -5$ mA

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	6	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$
Output capacitance	C_D	7	pF	D_{OUT}

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AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		μPD421002-80		μPD421002-10		μPD421002-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		70		60		50	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{CS}$ before RAS refresh cycle, average	I_{CC5}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CS}$ before $\overline{RAS}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CS}$	t_{CAC}		20		25		30	ns	(Notes 7, 9, 16)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 16)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 10)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CS}$ pulse width	t_{CS}	20	100000	25	100000	30	100000	ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD421002-80		μPD421002-10		μPD421002-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
$\overline{CS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 11)
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 16)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
$\overline{RAS}$ to column address hold time	t_{AH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		120		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to RAS	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	(Note 13)
Column address hold time referenced to $\overline{RAS}$ (write cycle)	t_{AWR}	60		70		85		ns	
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 17)
Write command to RAS lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		100		120		ns	(Note 15)
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	20		25		30		ns	(Note 15)

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		μPD421002-80		μPD421002-10		μPD421002-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Column address to $\overline{WE}$ delay time	t_{AWD}	45		50		60		ns	(Note 15)
Output hold time from $\overline{WE}$	t_{OHW}	10		10		10		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		25		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Static-Column Operation									
Operating current, static-column cycle, average	I_{CC4}		60		50		40	mA	$\overline{RAS} = \overline{CS} = V_{IL}$; addresses cycling; $t_{RSC} = t_{RSC}$ min or $t_{WSC} = t_{WSC}$ min (Note 5)
Static-column read cycle time	t_{RSC}	50		60		70		ns	(Note 6)
Static-column write cycle time	t_{WSC}	50		60		70		ns	(Note 6)
Static-column read-write cycle time	t_{RWSC}	95		115		135		ns	(Note 6)
Access time from previous $\overline{WE}$ (falling edge)	t_{PWA}		90		110		130	ns	(Notes 7, 18)
$\overline{RAS}$ pulse width (static-column cycle)	t_{RASC}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSW}	95		115		135		ns	
Previous $\overline{WE}$ (falling edge) to column address delay time	t_{WAD}	20	45	25	55	25	65	ns	(Note 18)
Column address hold time from previous $\overline{WE}$ (falling edge)	t_{PWH}	90		110		130		ns	
Write invalid time	t_{WI}	10		10		10		ns	
Output hold time from address	t_{OH}	5		5		5		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

Notes [cont]:

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

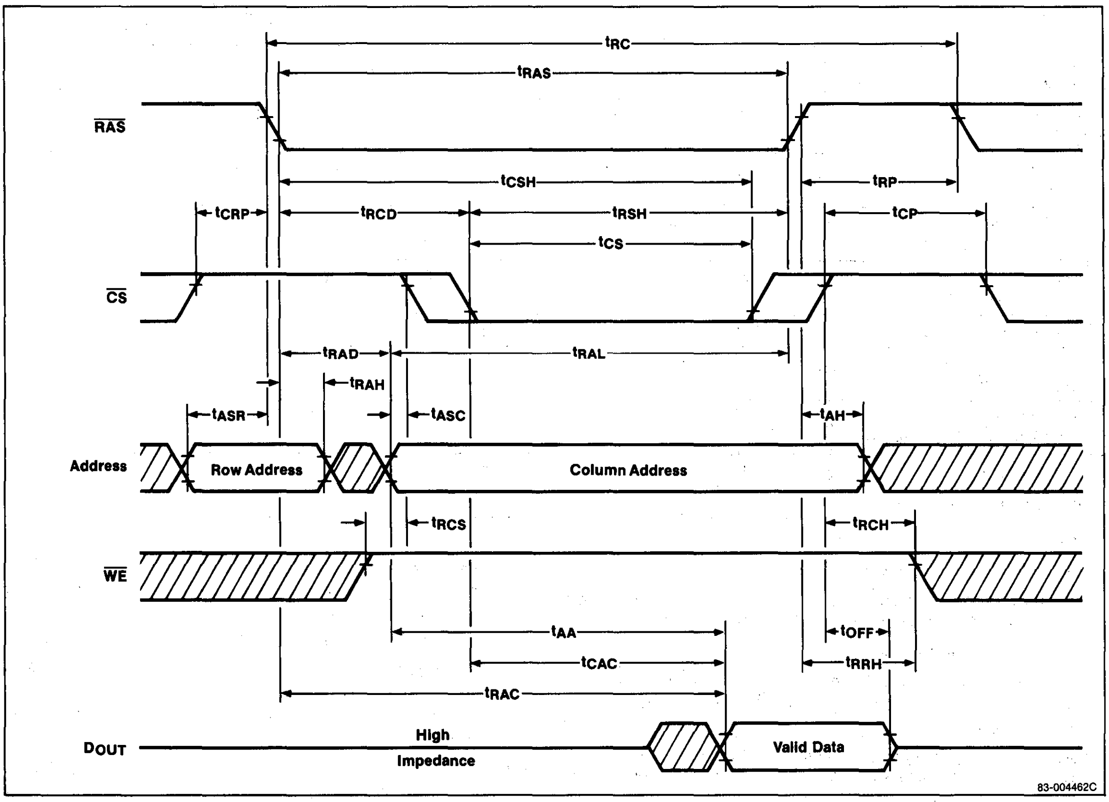
(16) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(17) Parameter t_{WP} is applicable for a delayed write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(18) If $t_{WAD} \leq t_{WAD}$ (max), then the access time is defined by t_{PWA}.

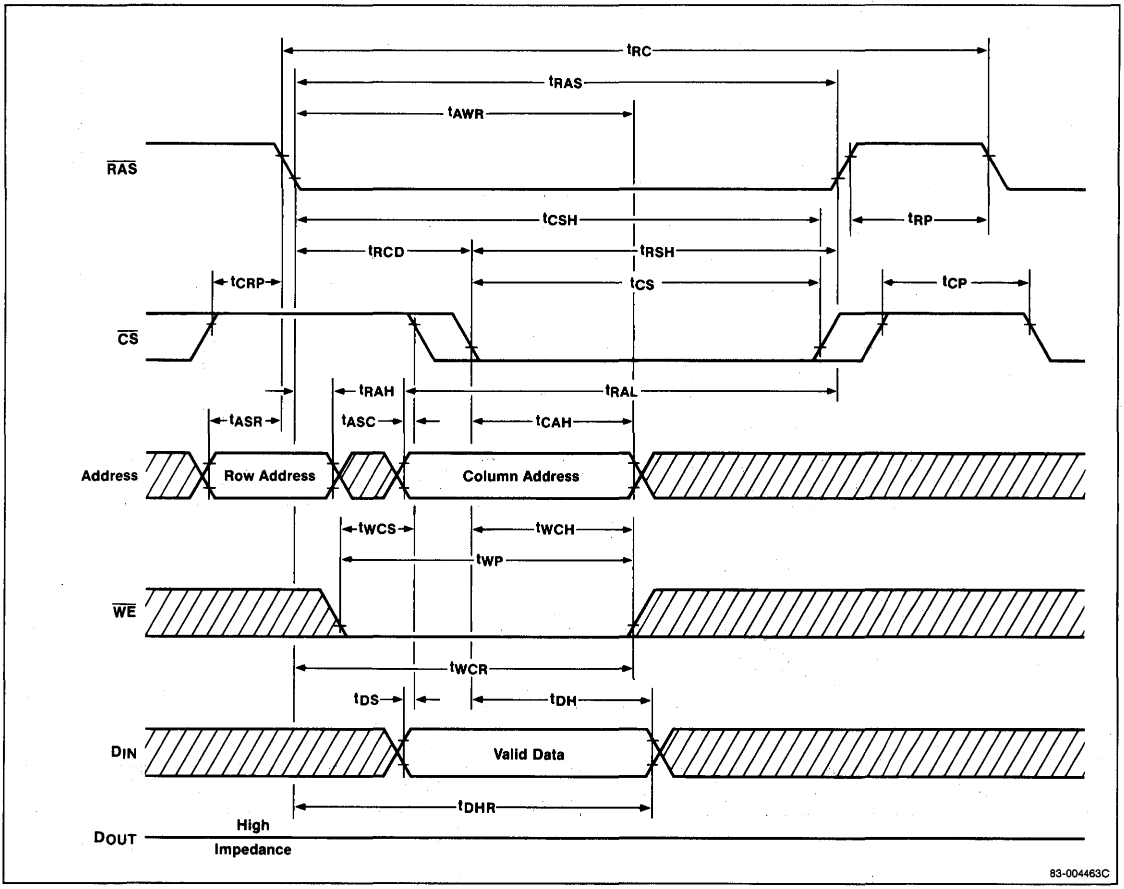
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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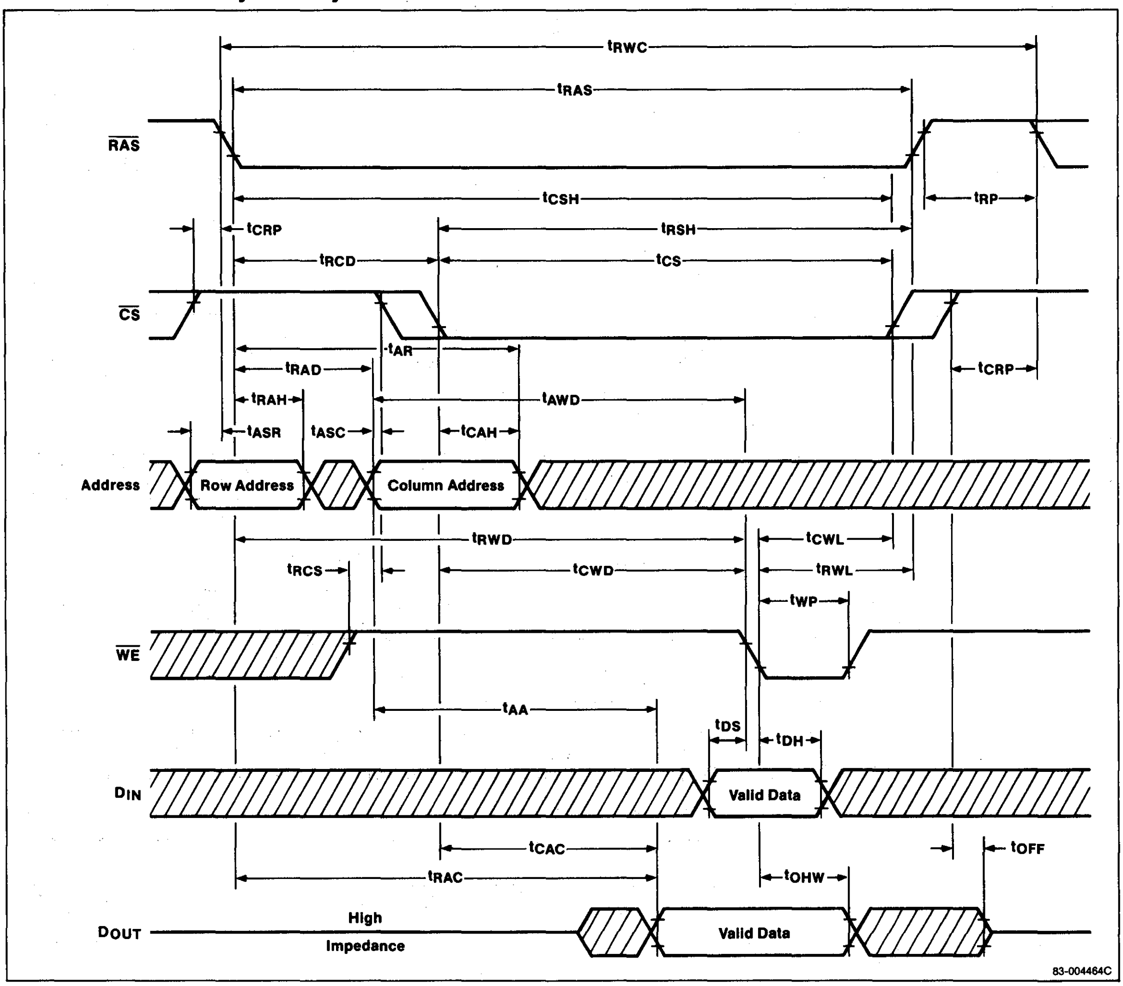
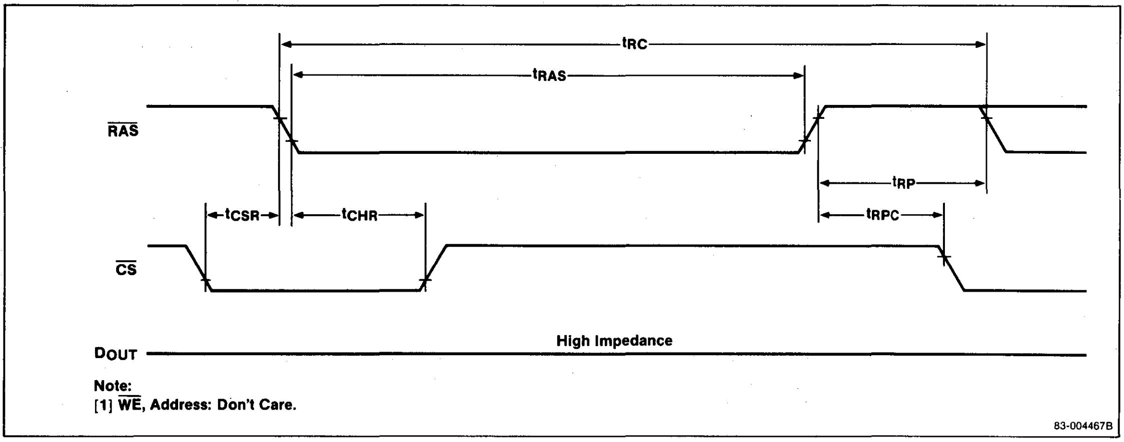
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle

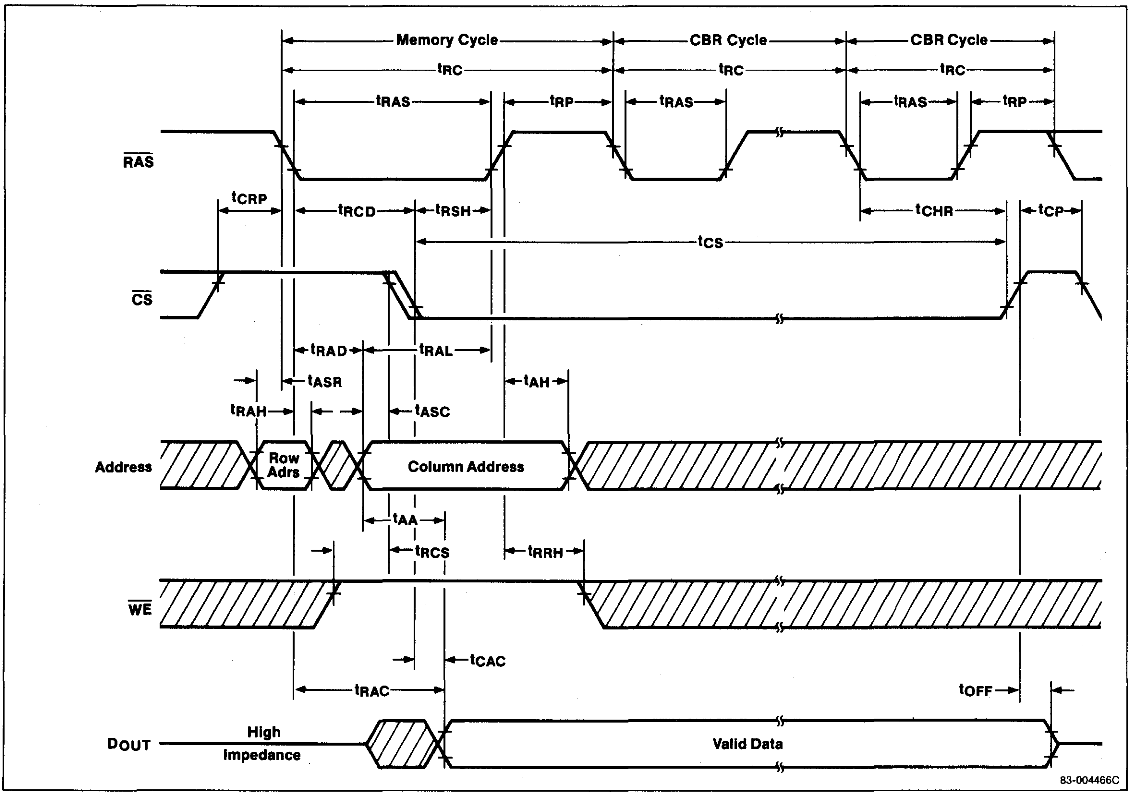


Timing Waveforms (cont)

$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle

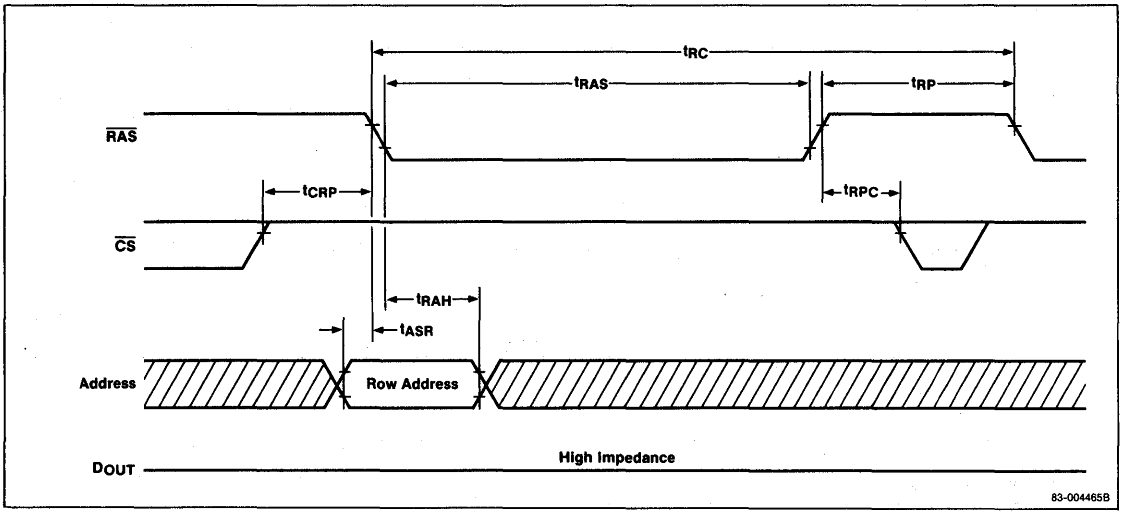


Hidden Refresh Cycle



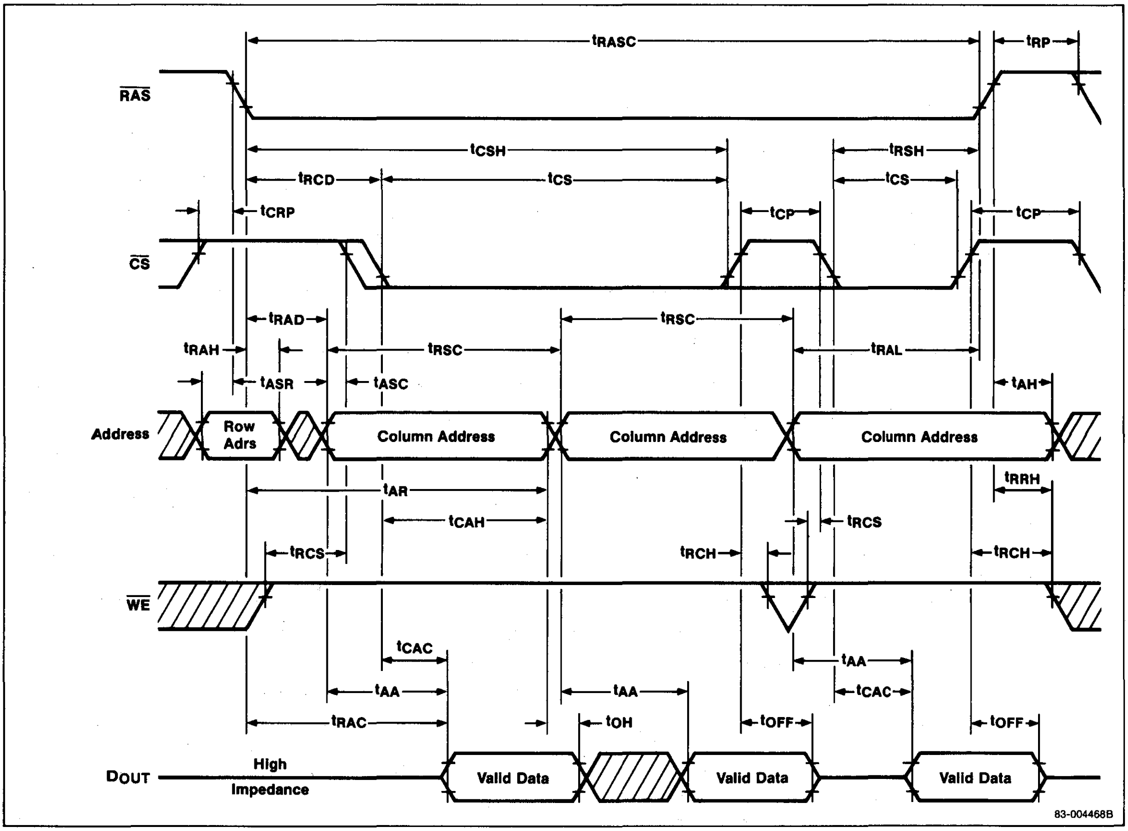
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



Timing Waveforms (cont)

Static-Column Read Cycle



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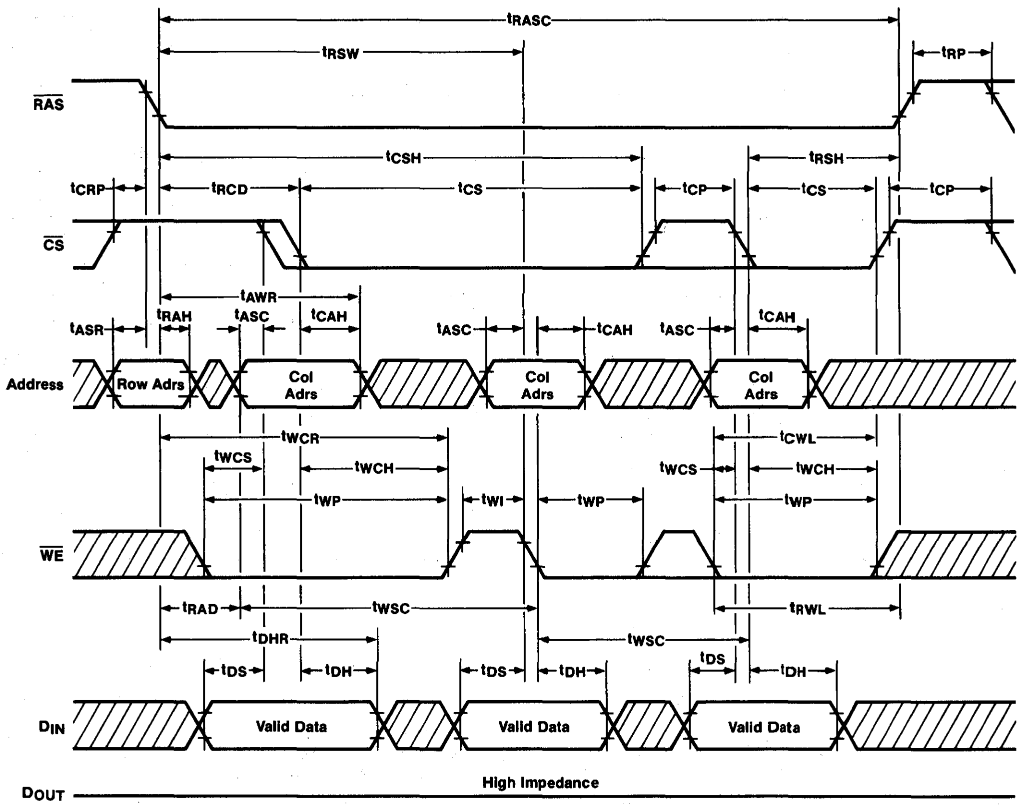
Timing Waveforms (cont)

Static-Column Write Cycle (Early Write)



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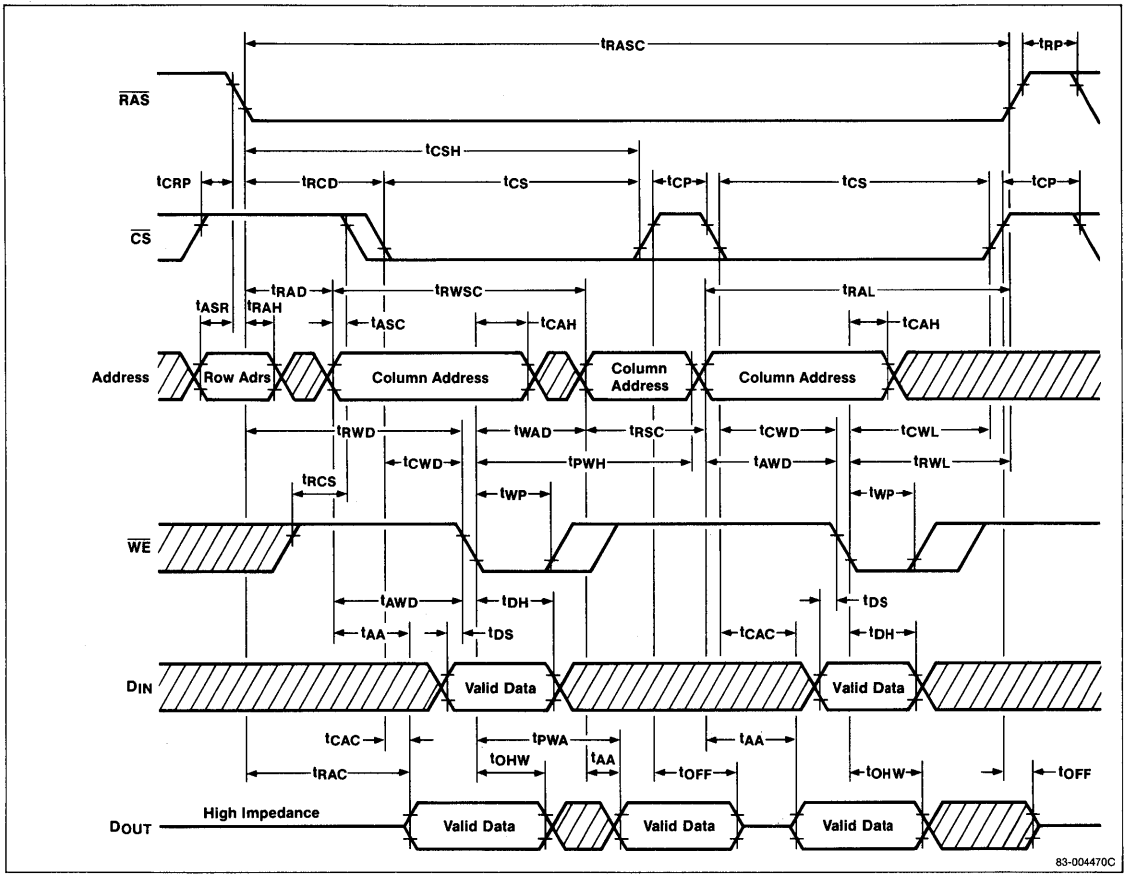
Timing Waveforms (cont)

Static-Column Read-Write/Read-Modify-Write Cycle



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NEC
NEC Electronics Inc.

μPD424256 262,144 x 4-BIT DYNAMIC CMOS RAM

Description

The μPD424256 is a fast-page, 262,144-word by 4-bit dynamic CMOS RAM designed to operate from a single +5-volt power supply. The device is fabricated with advanced polycide technology using trench capacitors to minimize silicon area and provide high storage cell capacity, high performance, and high reliability. The μPD424256 also uses a single-transistor dynamic storage cell and advanced CMOS circuitry throughout, ensuring minimum power dissipation. The negative-voltage substrate bias is automatically generated internally.

The three-state I/O pins are controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining a low $\overline{\text{CAS}}$. The data outputs are returned to a state of high impedance by returning $\overline{\text{CAS}}$ to a high logic level. The device is also capable of performing fast-page read and write cycles by cycling $\overline{\text{CAS}}$.

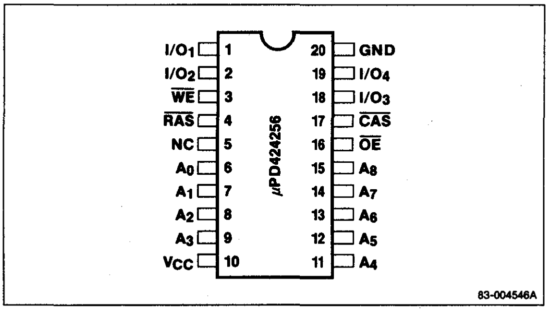
Refreshing may be accomplished by means of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle, enabling the internal generation of a refresh address. Refreshing may also be accomplished by means of $\overline{\text{RAS}}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms refresh period.

Features

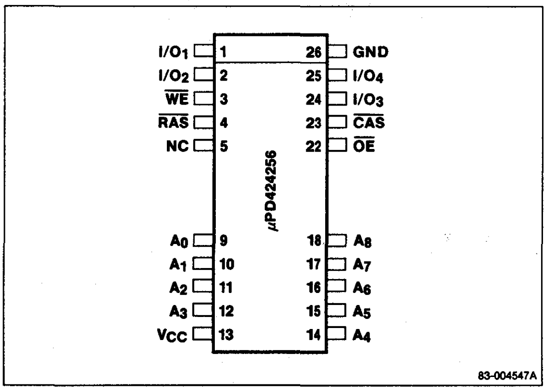
- □ 262,144-word by 4-bit organization
- □ Single +5-volt ±10% power supply
- □ Fast-page operation
- □ Low power dissipation
  - — 70 mA max (active), 80 ns version
  - — 1 mA max (standby)
- □ $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ internal refreshing capability
- □ Multiplexed address inputs
- □ On-chip substrate bias generator
- □ Nonlatched, TTL-compatible, three-state I/O
- □ Low input capacitance
- □ TTL-compatible inputs
- □ 512 refresh cycles during an 8-ms period
- □ High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

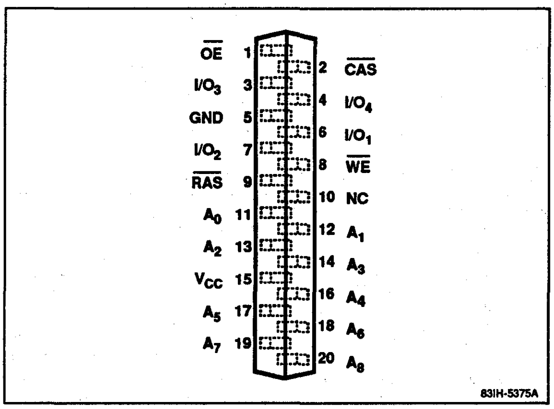
20-Pin Plastic DIP



26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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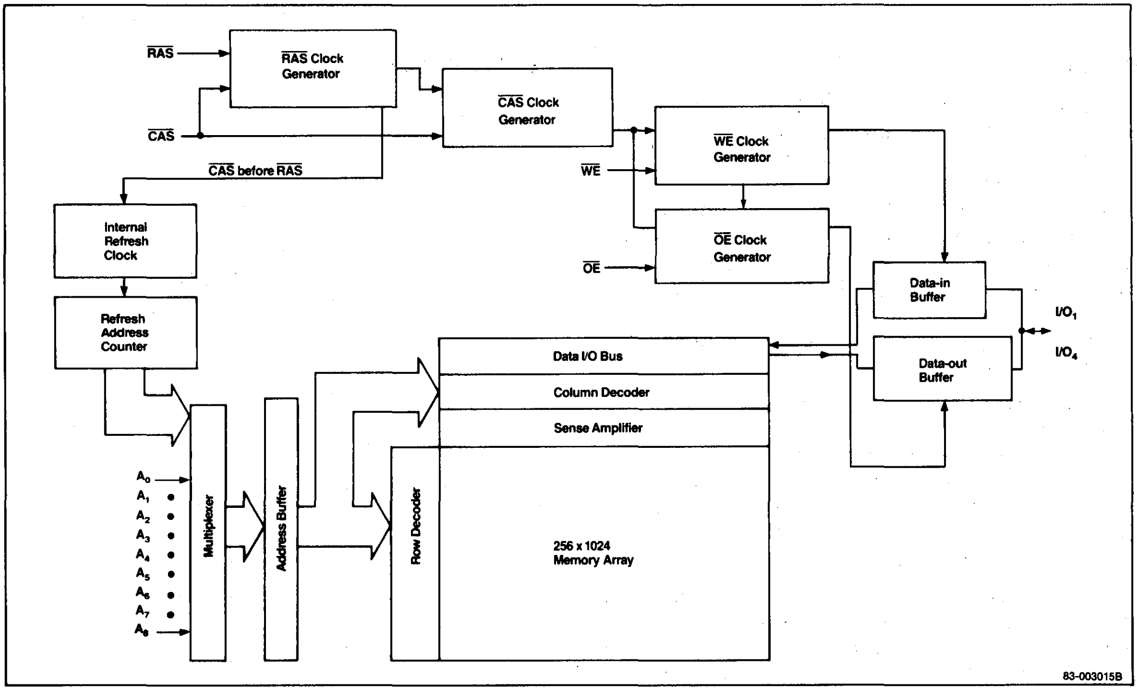
Block Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data input/output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	$\overline{CAS}$ Access Time (max)	Column Address Access (max)	Package
μPD424256C-80	80 ns	20 ns	45 ns	20-pin plastic DIP
C-10	100 ns	25 ns	50 ns	
C-12	120 ns	30 ns	60 ns	
μPD424256LA-80	80 ns	20 ns	45 ns	26/20-pin plastic SOJ
LA-10	100 ns	25 ns	50 ns	
LA-12	120 ns	30 ns	60 ns	
μPD424256V-80	80 ns	20 ns	45 ns	20-pin plastic ZIP
V-10	100 ns	25 ns	50 ns	
V-12	120 ns	30 ns	60 ns	

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.4		V_{CC} +1.0	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} = \overline{CAS} = V_{IH}$
				1.0	mA	$\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$
Input leakage current	$I_{I(L)}$	−10		10	μA	$V_{IN} = 0$ to 5.5 V; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; $V_{OUT} = 0$ to 5.5 V
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 4.2$ mA
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -5$ mA

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_D	7	pF	I/O

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AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		μPD424256-80		μPD424256-10		μPD424256-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		70		60		50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refreshing, average	I_{CC3}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Fast-page operating current, average	I_{CC4}		60		50		40	mA	$\overline{RAS} = V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CAS} = V_{IL}$; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	215		255		295		ns	(Note 6)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10, 11)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		65	ns	(Notes 7, 11)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 12)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD424256-80		μPD424256-10		μPD424256-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
$\overline{RAS}$ pulse width (page mode)	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ precharge time, non-page cycle	t_{CPN}	10		10		15		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	10	20	10	25	15	30	ns	(Note 11)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	(Note 11)
Column address hold time	t_{CAH}	20		20		25		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 18)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 18)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		65		ns	(Note 18)
Column address to $\overline{WE}$ delay time	t_{AWD}	70		80		95		ns	(Note 18)

AC Characteristics (cont)

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V $\pm10\%$

		Limits							
		μPD424256-80		μPD424256-10		μPD424256-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	15		20		25		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	
$\overline{OE}$ data delay time	t_{OED}	20		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	(Note 12)
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured by assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range ($T_A = 0$ to $+70°C$) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF ($V_{OH} = 2.0$ V, $V_{OL} = 0.8$ V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{ASC}$ (max)	t_{CAC}

(12) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

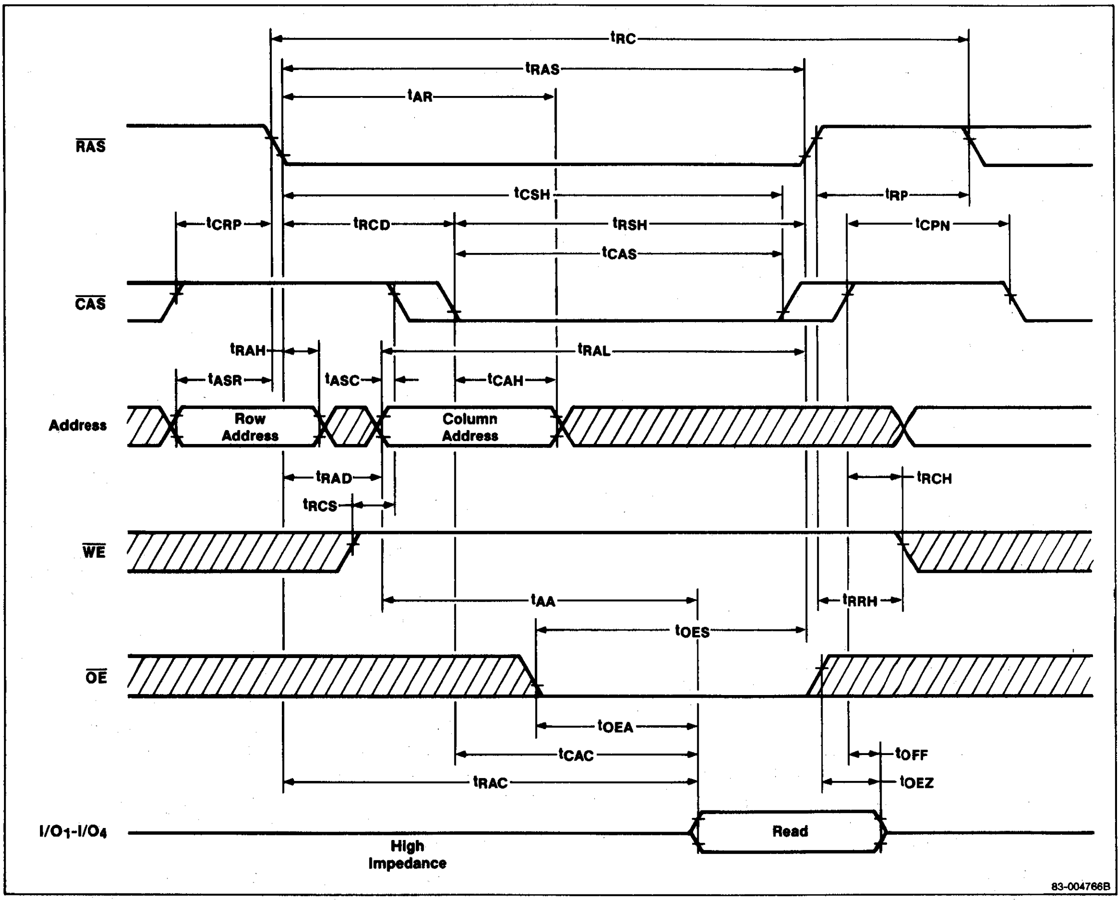
(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

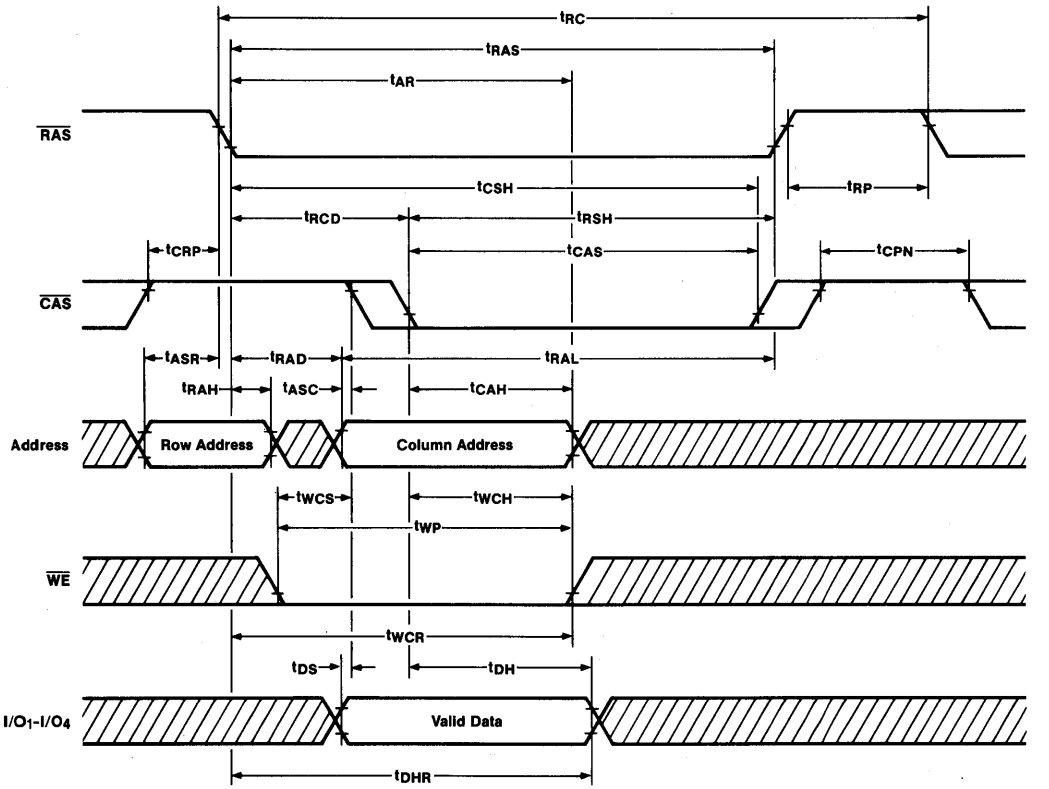
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



Notes:
[1] $\overline{OE}$ = V_{IH} or V_{IL}.

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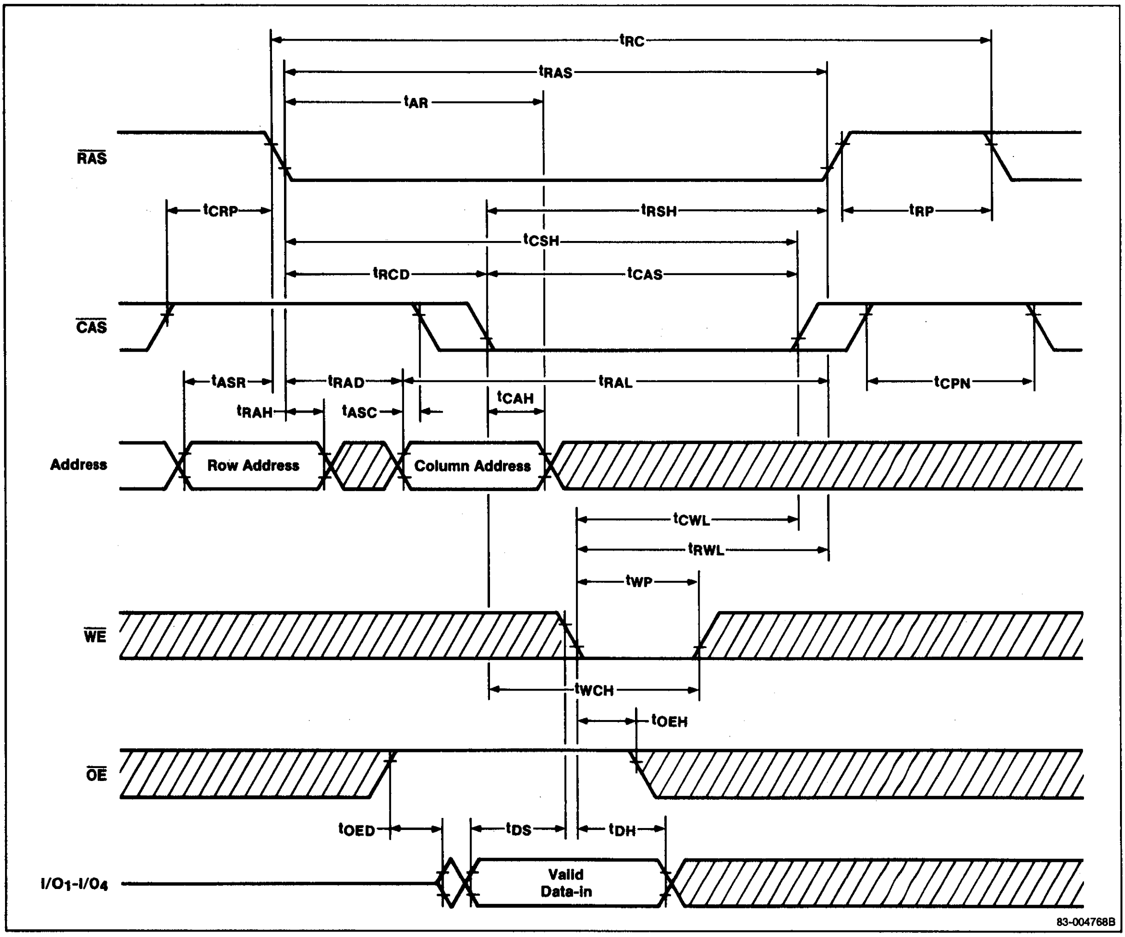
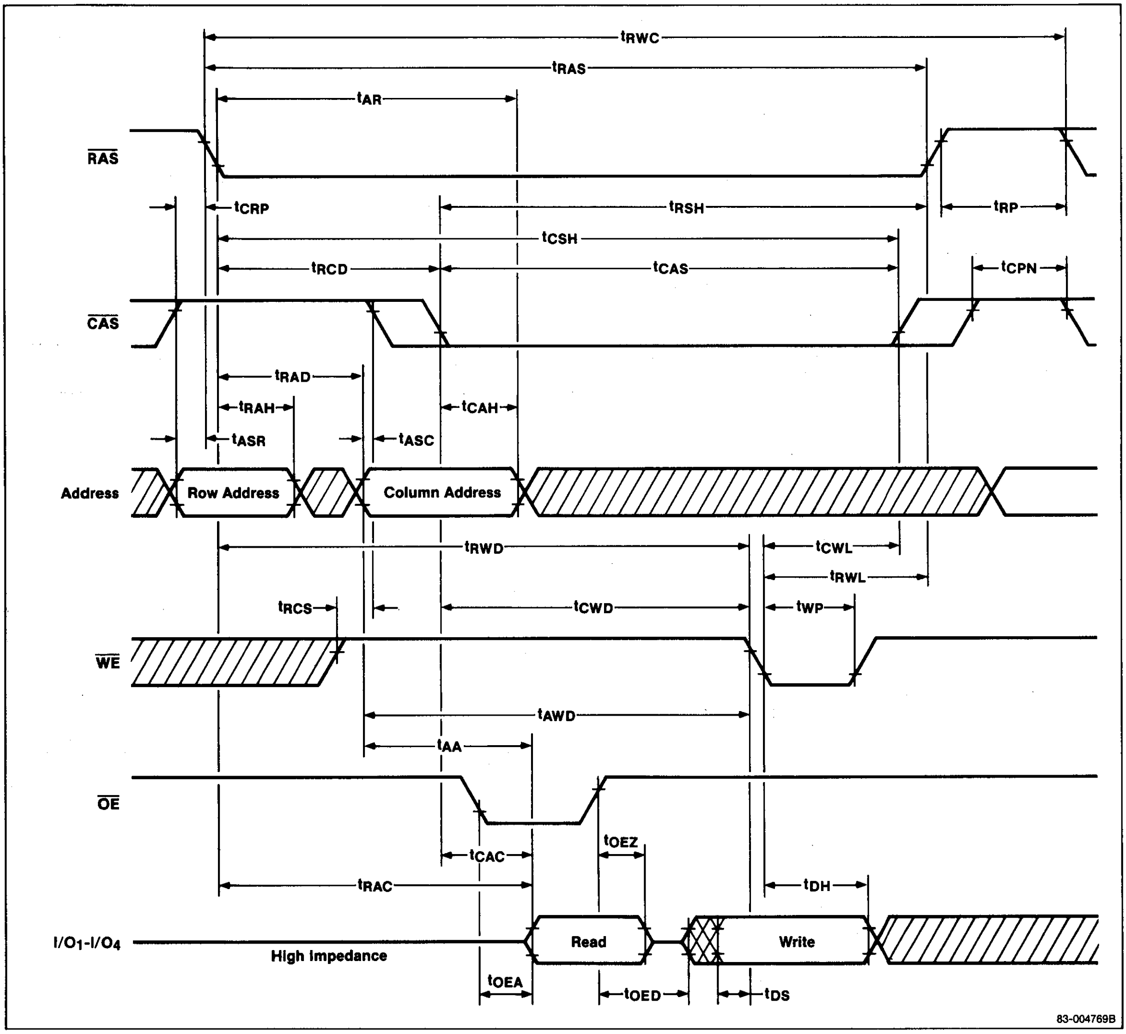
Timing Waveforms (cont)

$\overline{OE}$-Controlled Write Cycle



Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



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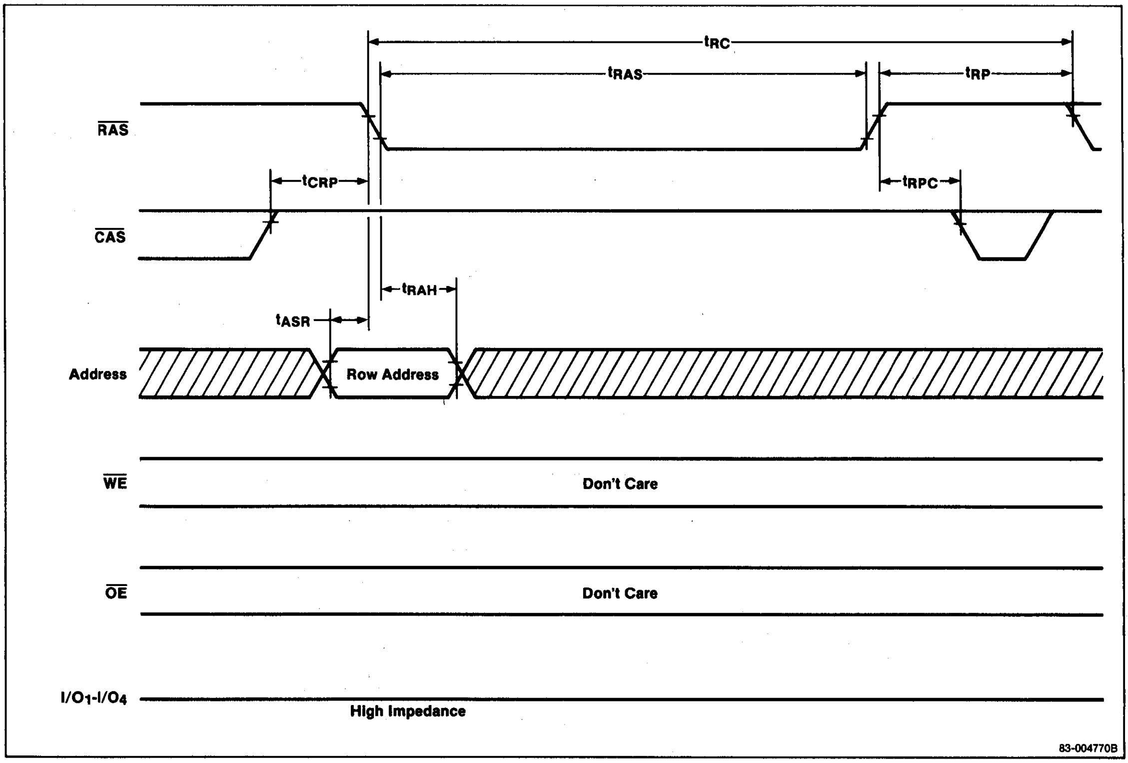
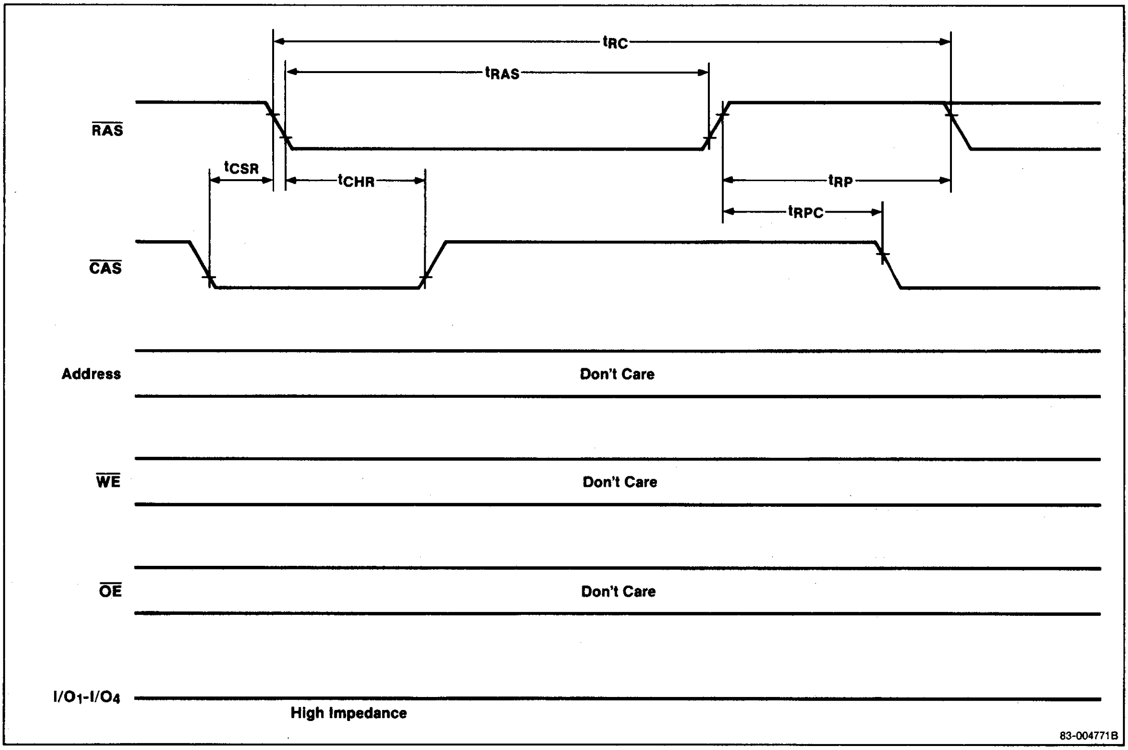
Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



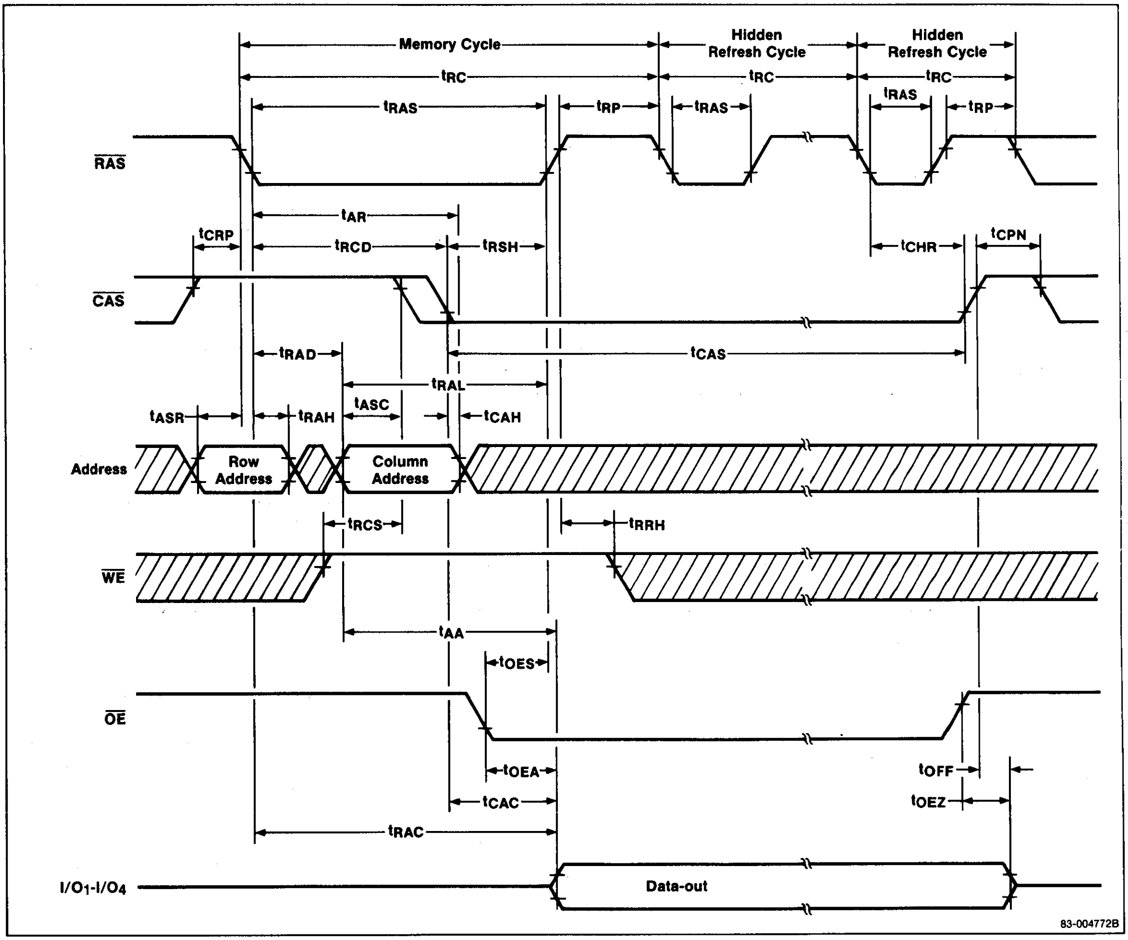
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



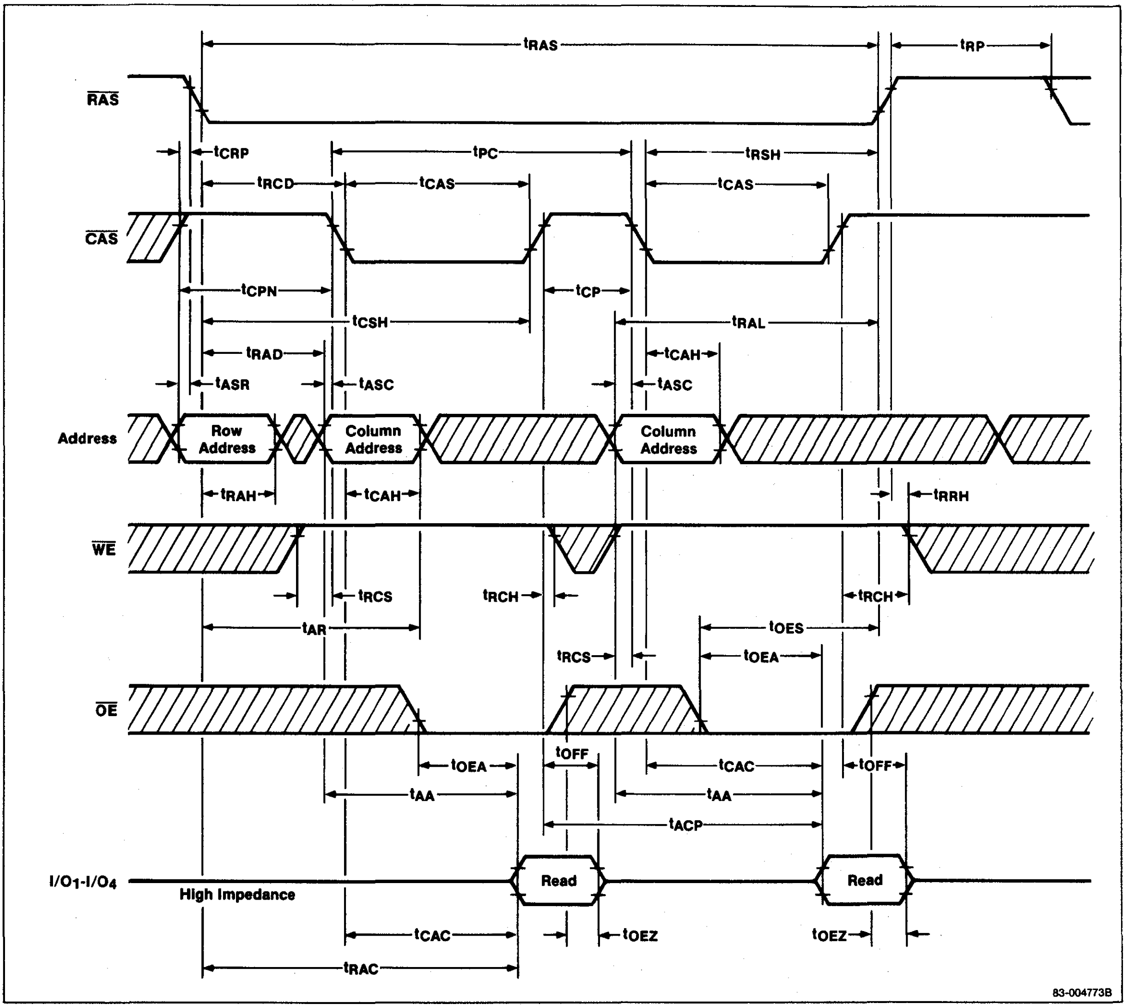
Timing Waveforms (cont)

Hidden Refresh Cycle



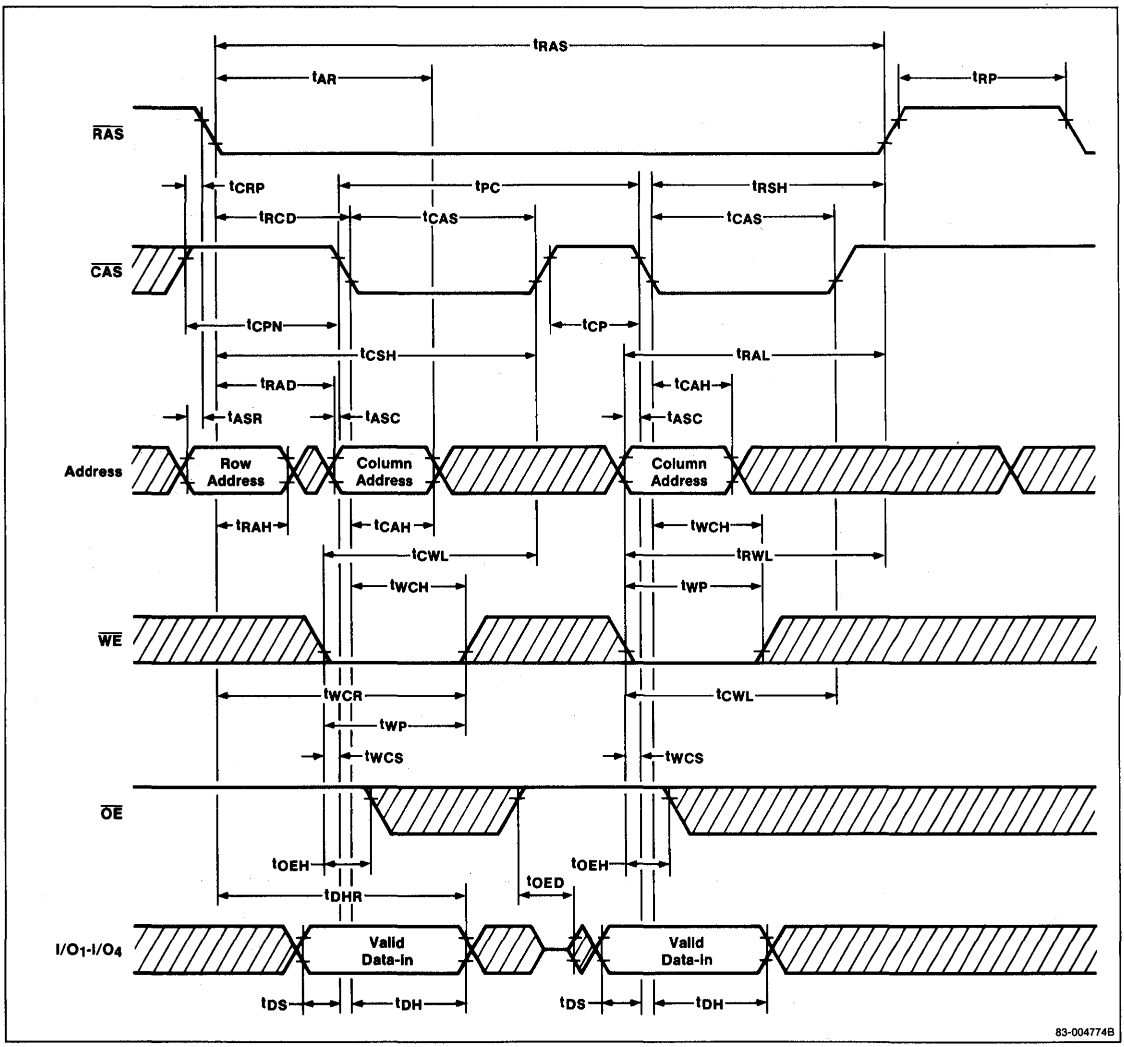
Timing Waveforms (cont)

Page Mode Read Cycle



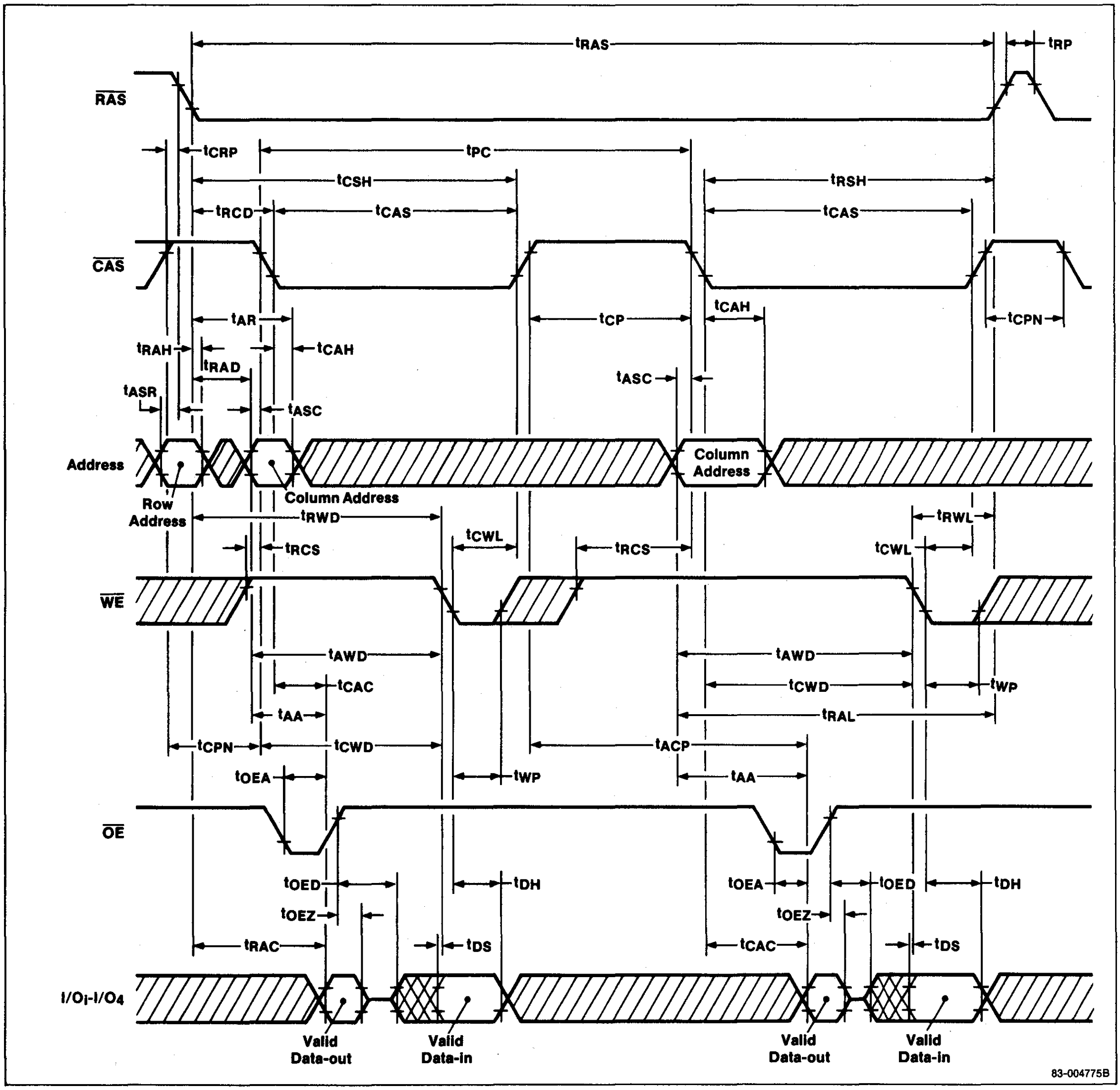
Timing Waveforms (cont)

Page Mode Write Cycle (Early Write)



Timing Waveforms (cont)

Page Mode Read-Write/Read-Modify-Write Cycle



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μPD424258 262,144 x 4-BIT DYNAMIC CMOS RAM

PRELIMINARY INFORMATION

Description

The μPD424258 is a static-column, 262,144-word by 4-bit dynamic RAM designed to operate from a single +5-volt power supply. The device is fabricated with advanced polycide technology using trench capacitors to minimize silicon area and provide high storage cell capacity, high performance, and high reliability. The μPD424258 also uses a single-transistor dynamic storage cell and advanced CMOS circuitry throughout, ensuring minimum power dissipation. The negative-voltage substrate bias is automatically generated internally.

The three-state I/O pins are controlled by $\overline{CS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining a low $\overline{CS}$. The data outputs are returned to a state of high impedance by returning $\overline{CS}$ to a high logic level. The device is also capable of executing static-column read and write cycles by switching the column address inputs.

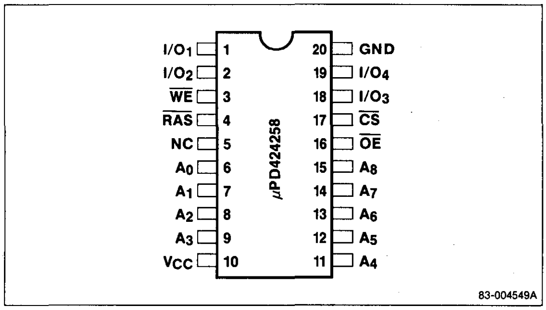
Refreshing may be accomplished by means of a $\overline{CS}$ before $\overline{RAS}$ cycle, enabling the internal generation of a refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms refresh period.

Features

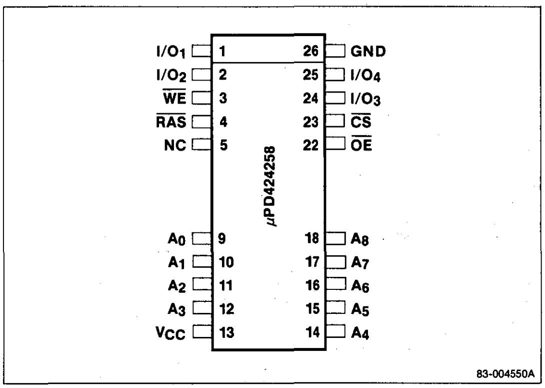
- ☐ 262,144-word by 4-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ Static-column operation
- ☐ Low power dissipation
- ☐ $\overline{CS}$ before $\overline{RAS}$ internal refreshing
- ☐ Multiplexed address inputs
- ☐ On-chip substrate bias generator
- ☐ Nonlatched, TTL-compatible, three-state I/O
- ☐ Low input capacitance
- ☐ TTL-compatible inputs
- ☐ 512 refresh cycles during an 8-ms period
- ☐ High-density 20-pin plastic DIP, 26/20-pin plastic SOJ, or 20-pin plastic ZIP packaging

Pin Configurations

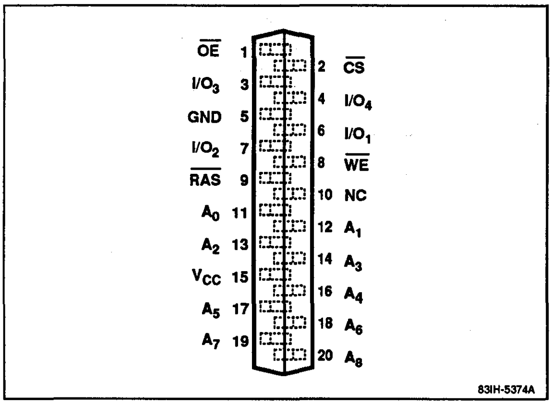
20-Pin Plastic DIP



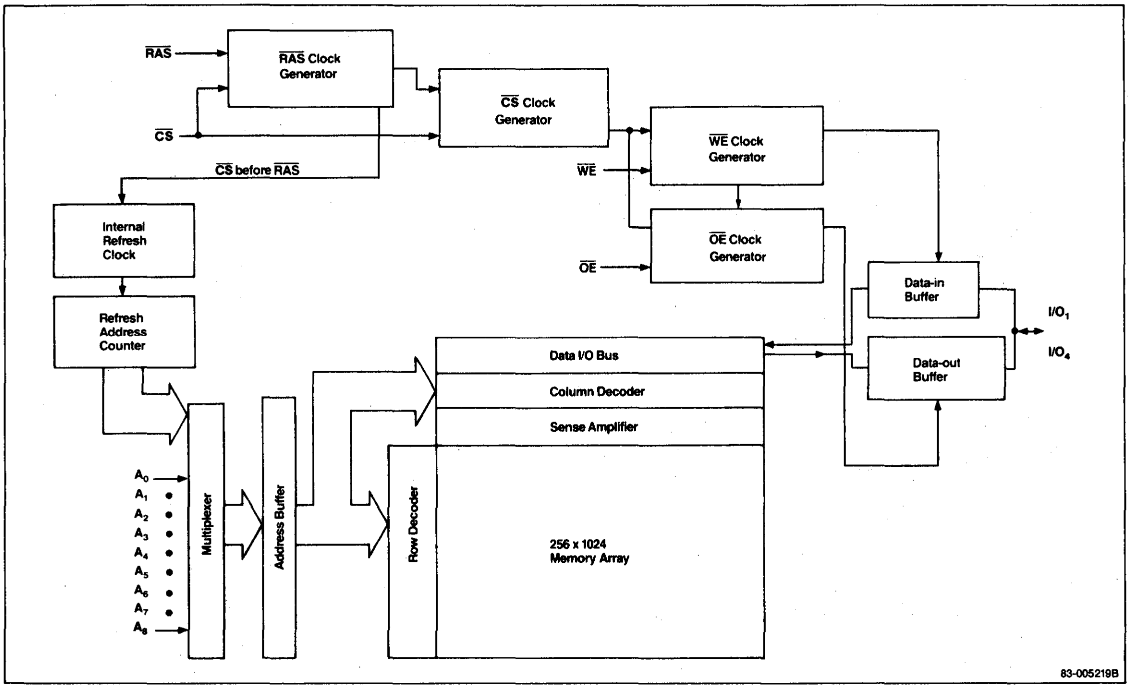
26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



Block Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
I/O_1 - I/O_4	Data input/output
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	Row Access Time (max)	R/W Cycle Time (min)	Address Access Time (max)	Static-Column Cycle Time (min)	Package
μPD424258C-80	80 ns	160 ns	45 ns	50 ns	20-pin plastic DIP
C-10	100 ns	190 ns	50 ns	60 ns	
C-12	120 ns	220 ns	60 ns	70 ns	
μPD424258LA-80	80 ns	160 ns	45 ns	50 ns	26/20-pin plastic SOJ
LA-10	100 ns	190 ns	50 ns	60 ns	
LA-12	120 ns	220 ns	60 ns	70 ns	
μPD424258V-80	80 ns	160 ns	45 ns	50 ns	20-pin plastic ZIP
V-10	100 ns	190 ns	50 ns	60 ns	
V-12	120 ns	220 ns	60 ns	70 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.4		V_{CC} +1.0	V	Referenced to GND
Input voltage, low	V_{IL}	−1.0		0.8	V	Referenced to GND
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} = \overline{CS} = V_{IH}$
				1.0	mA	$\overline{RAS} = \overline{CS} \geq V_{CC} - 0.2$
Input leakage current	$I_{I(L)}$	−10		10	μA	V_{IN} = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −5 mA

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_D	7	pF	I/O_1-I/O_4

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD424258-80		μPD424258-10		μPD424258-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		70		60		50	mA	$\overline{RAS}$, $\overline{CS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{RAS}$-only refresh, average	I_{CC3}		70		60		50	mA	$\overline{RAS}$ cycling; $\overline{CS} = V_{IH}$; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, $\overline{CS}$ before $\overline{RAS}$ refresh, average	I_{CC5}		70		60		50	mA	$\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	215		255		295		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CS}$	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 11)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CS}$ pulse width	t_{CS}	20	100000	25	100000	30	100000	ns	
$\overline{CS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 12)
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 13)
$\overline{CS}$ precharge time	t_{CP}	10		10		15		ns	
$\overline{RAS}$ precharge $\overline{CS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$ (rising edge)	t_{AH}	15		15		15		ns	
Column address hold time referenced to $\overline{RAS}$ (write cycle)	t_{AWR}	60		70		85		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		50		60		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 14)
Read command hold time referenced to $\overline{CS}$	t_{RCH}	0		0		0		ns	(Note 14)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD424258-80		μPD424258-10		μPD424258-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Write command pulse width	t_{WP}	15		20		25		ns	(Note 15)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 16)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 16)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 17)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		155		ns	(Note 17)
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		65		ns	(Note 17)
Column address to $\overline{WE}$ delay time	t_{AWD}	70		80		95		ns	(Note 17)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	80		100		120		ns	
$\overline{CS}$ setup time for $\overline{CS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		10		ns	
$\overline{CS}$ hold time for $\overline{CS}$ before $\overline{RAS}$ refresh	t_{CHR}	15		20		25		ns	
Refresh period	t_{REF}		8		8		8	ms	Addresses A_0-A_8
Access time from $\overline{OE}$	t_{OEA}		20		25		30	ns	(Note 7)
$\overline{OE}$ data delay time	t_{OED}	20		25		30		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns	(Note 11)
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		0		ns	
Static-Column Mode									
Operating current, static-column operation, average	I_{CC4}		60		50		40	mA	$\overline{RAS}$ = $\overline{CS}$ = V_{IL}; addresses cycling; t_{RSC} = t_{RSC} min or t_{WSC} = t_{WSC} min (Note 5)
Read cycle time	t_{RSC}	50		60		70		ns	(Note 6)
Write cycle time	t_{WSC}	50		60		70		ns	(Note 6)
Read/write cycle time	t_{RWSC}	120		145		170		ns	(Note 6)
Access time from $\overline{WE}$	t_{PWA}		90		110		130	ns	(Notes 7, 18)
$\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSW}	95		115		135		ns	
$\overline{WE}$ to column address delay time	t_{WAD}	20	45	25	55	25	65	ns	(Note 18)
Column address hold time referenced to $\overline{WE}$	t_{PWH}	90		110		130		ns	

AC Characteristics (cont)

T_A = 0 to +70 °C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD424258-80		μPD424258-10		μPD424258-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write invalid time	t_{WI}	10		10		10		ns	
Output hold time from address	t_{OH}	5		5		5		ns	
Output enable time from $\overline{WE}$	t_{OW}		25		30		35	ns	(Note 7)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured by assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured by assuming that all column address inputs are switched only once each static-column cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open-circuit condition and are not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}, t_{AA}, or t_{OEA}.

(13) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CS}$ cycles preceded by any cycle.

(14) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(15) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

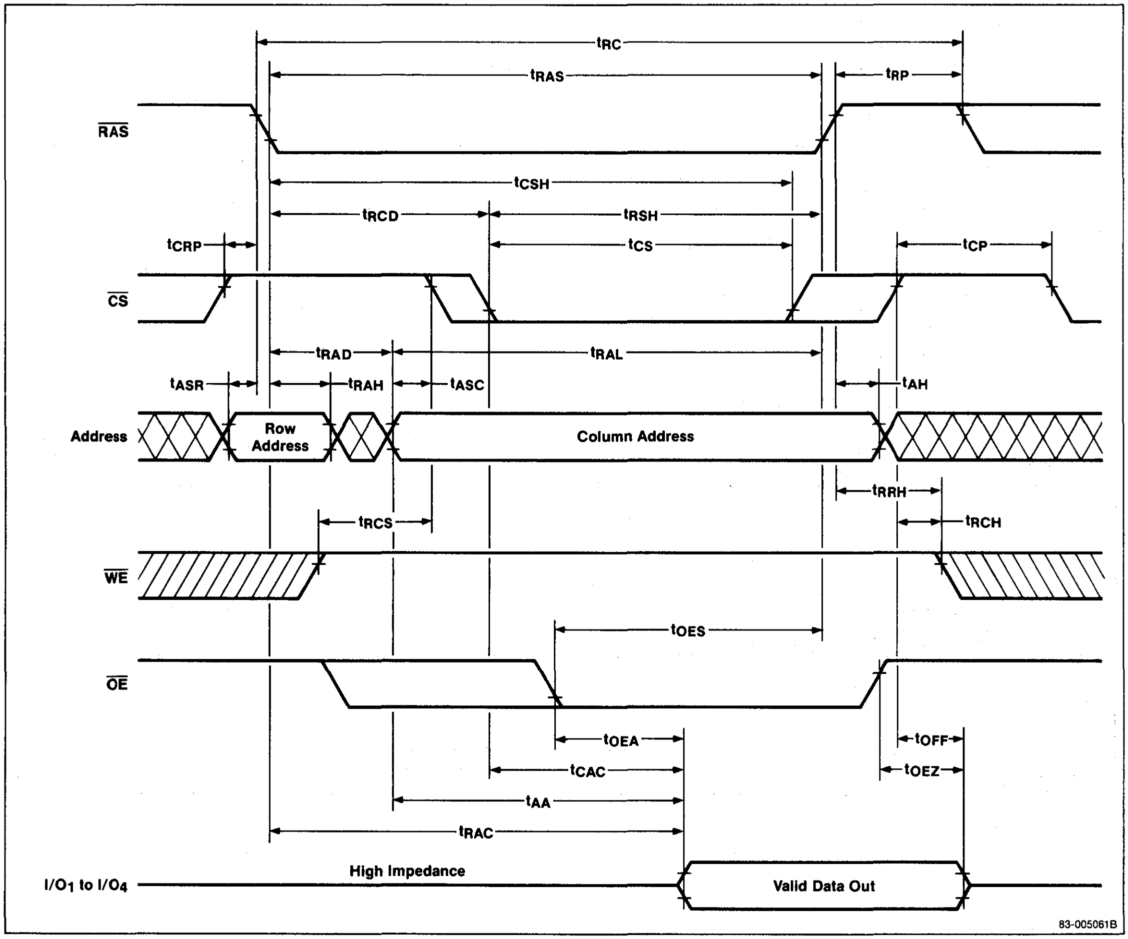
(16) These parameters are referenced to the falling edge of $\overline{CS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(17) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CS}$ returns to V_{IH}) is indeterminate.

(18) If $t_{WAD} \leq t_{WAD}$ (max), then the access time is defined by t_{PWA}.

Timing Waveforms

Read Cycle



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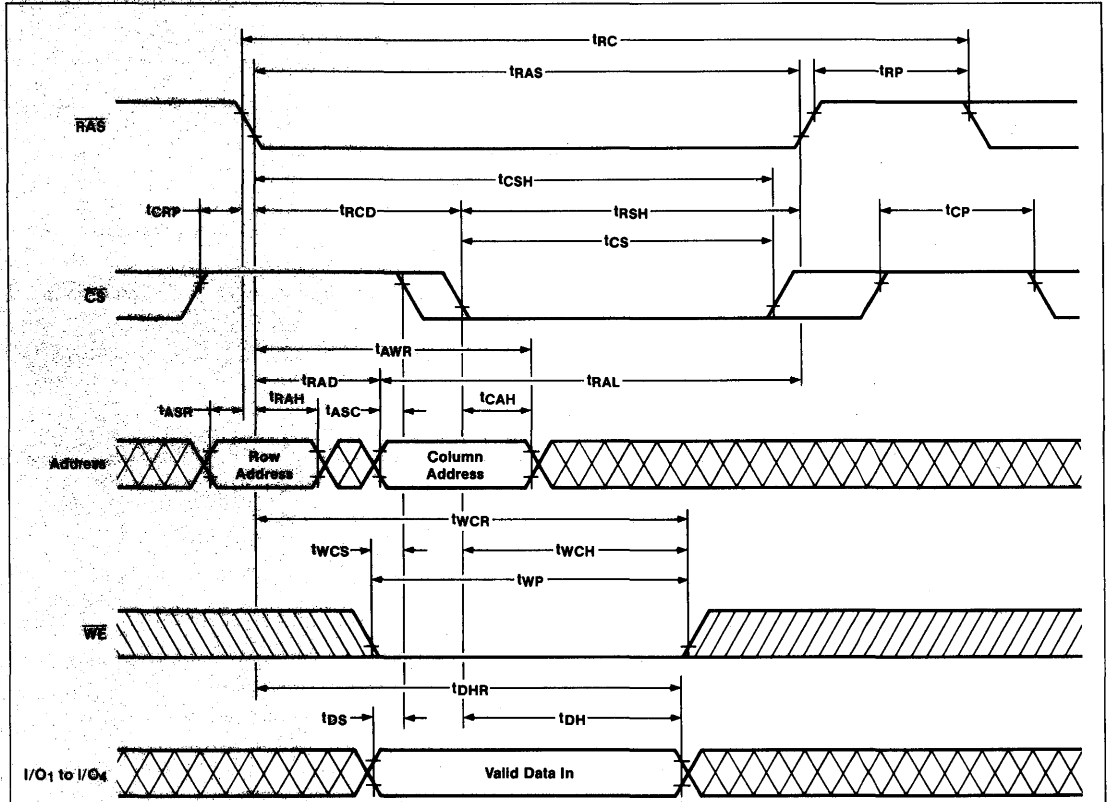
Timing Waveforms (cont)

Write Cycle (Early Write)



Note:
[1] $\overline{OE}$ = don't care.

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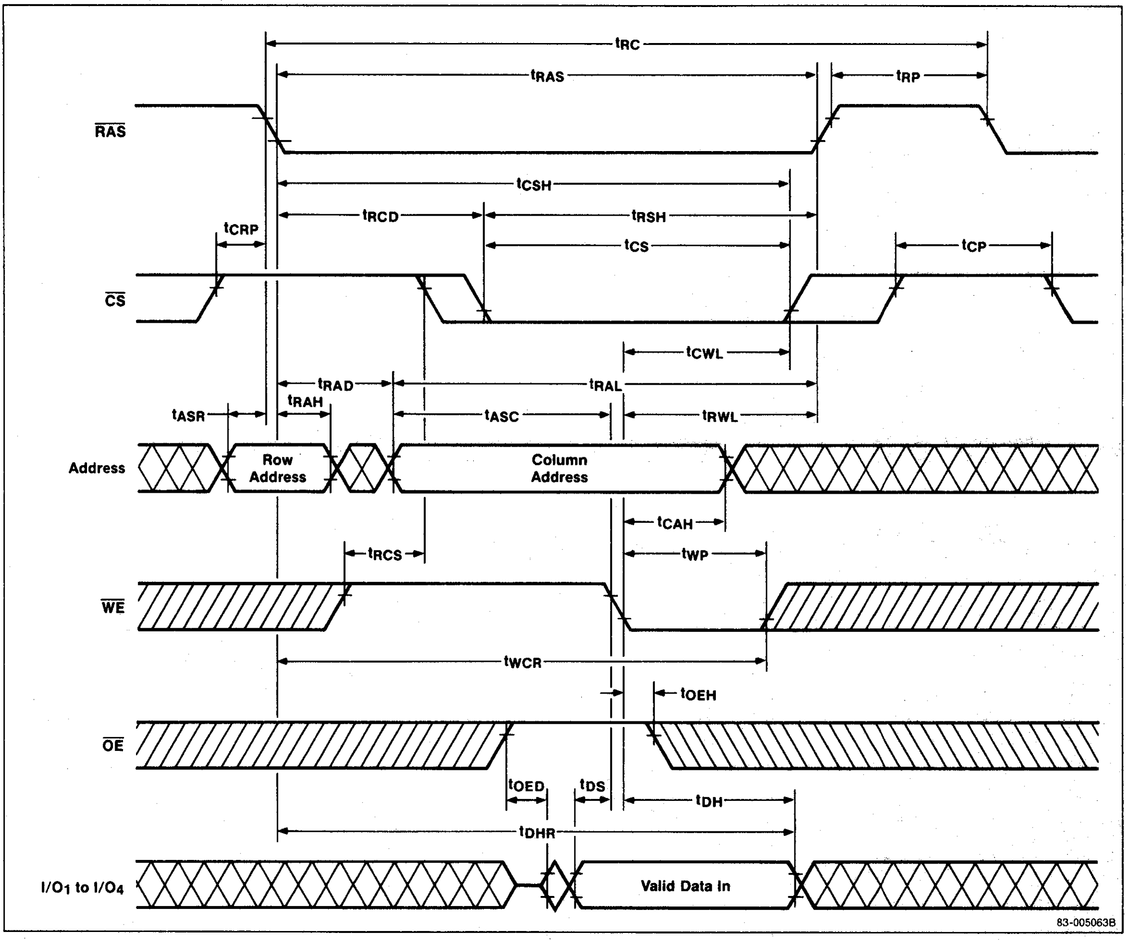
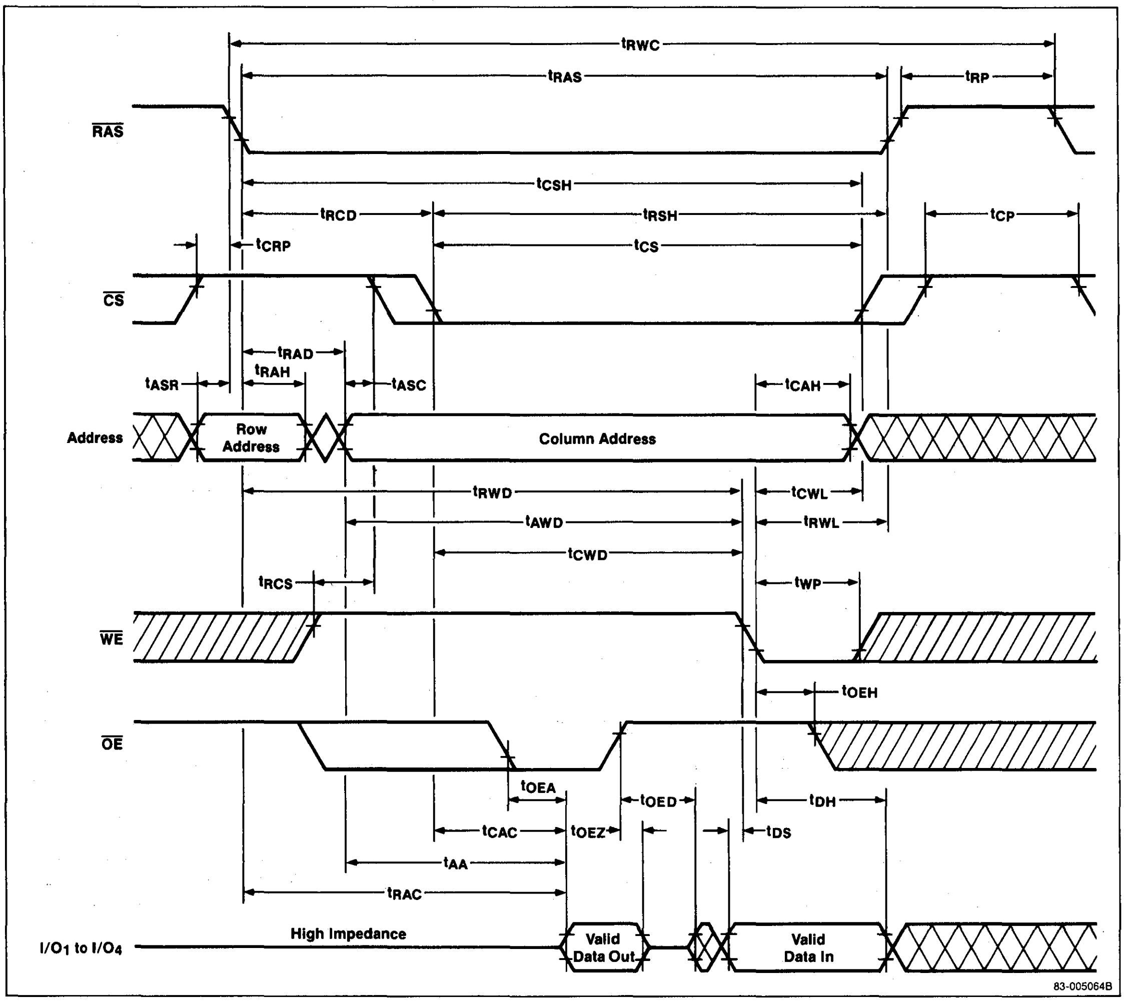
Timing Waveforms (cont)

Write Cycle (Late Write)



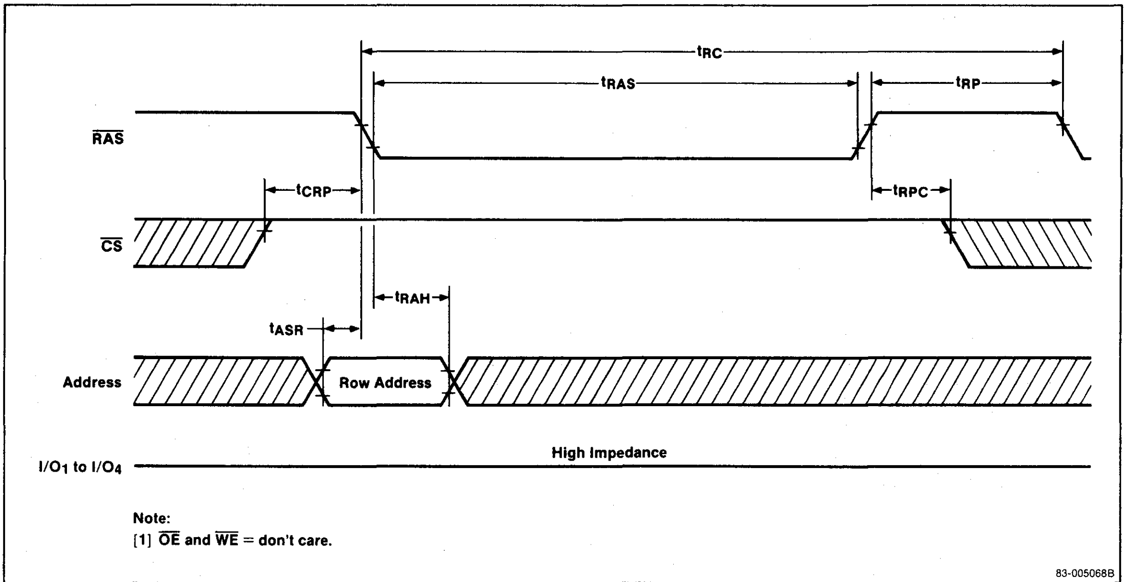
Timing Waveforms (cont)

Read-Modify-Write Cycle

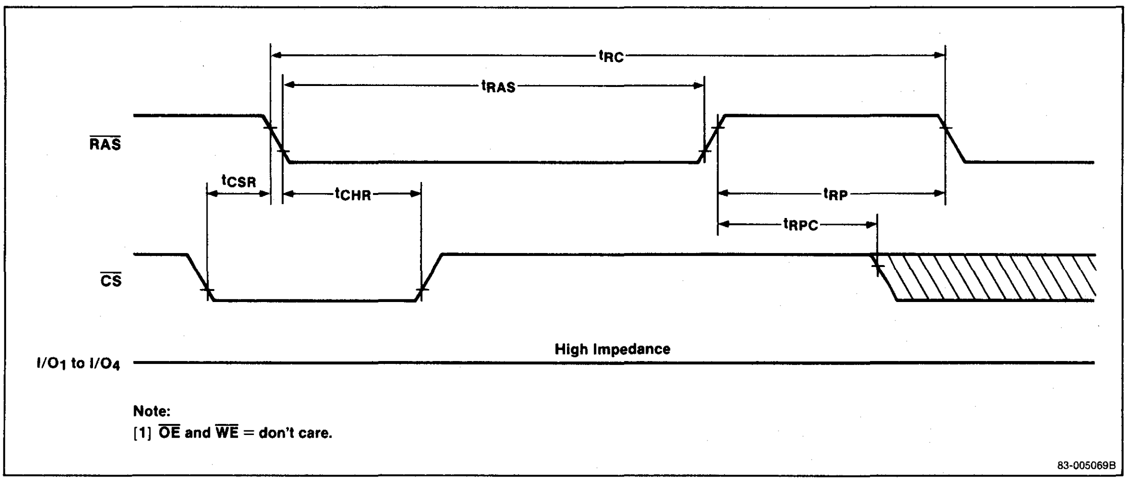


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle



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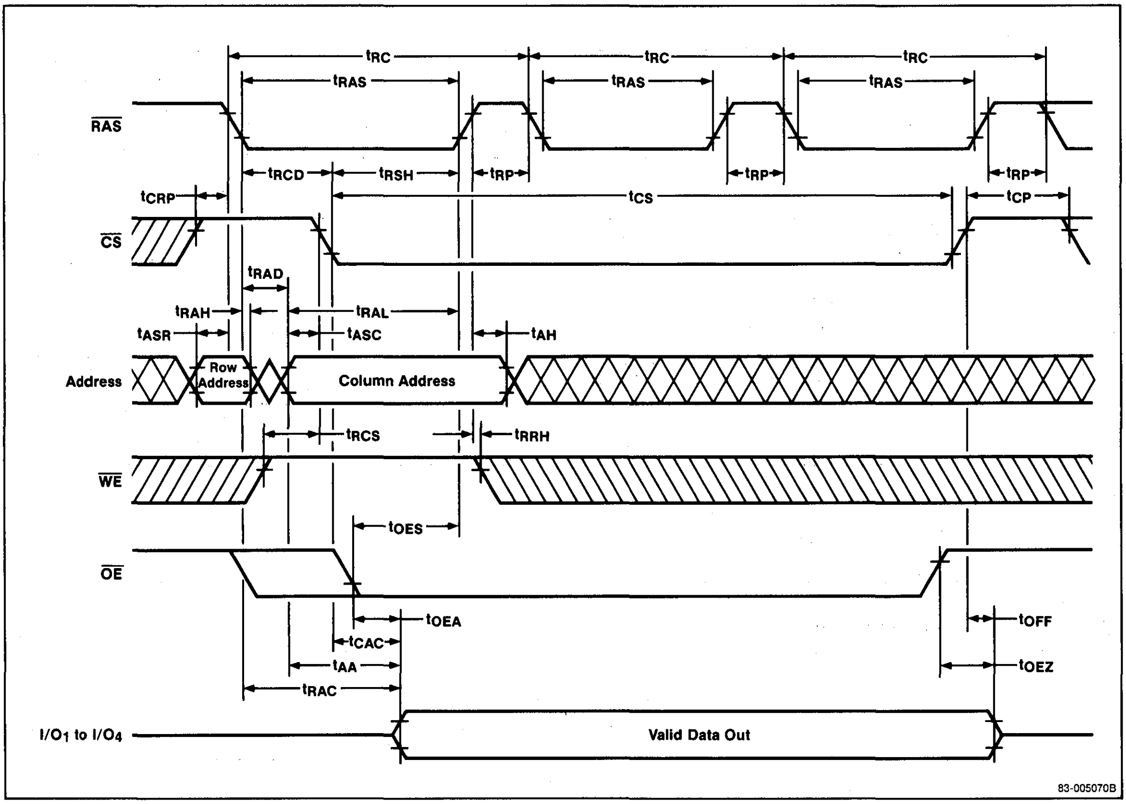
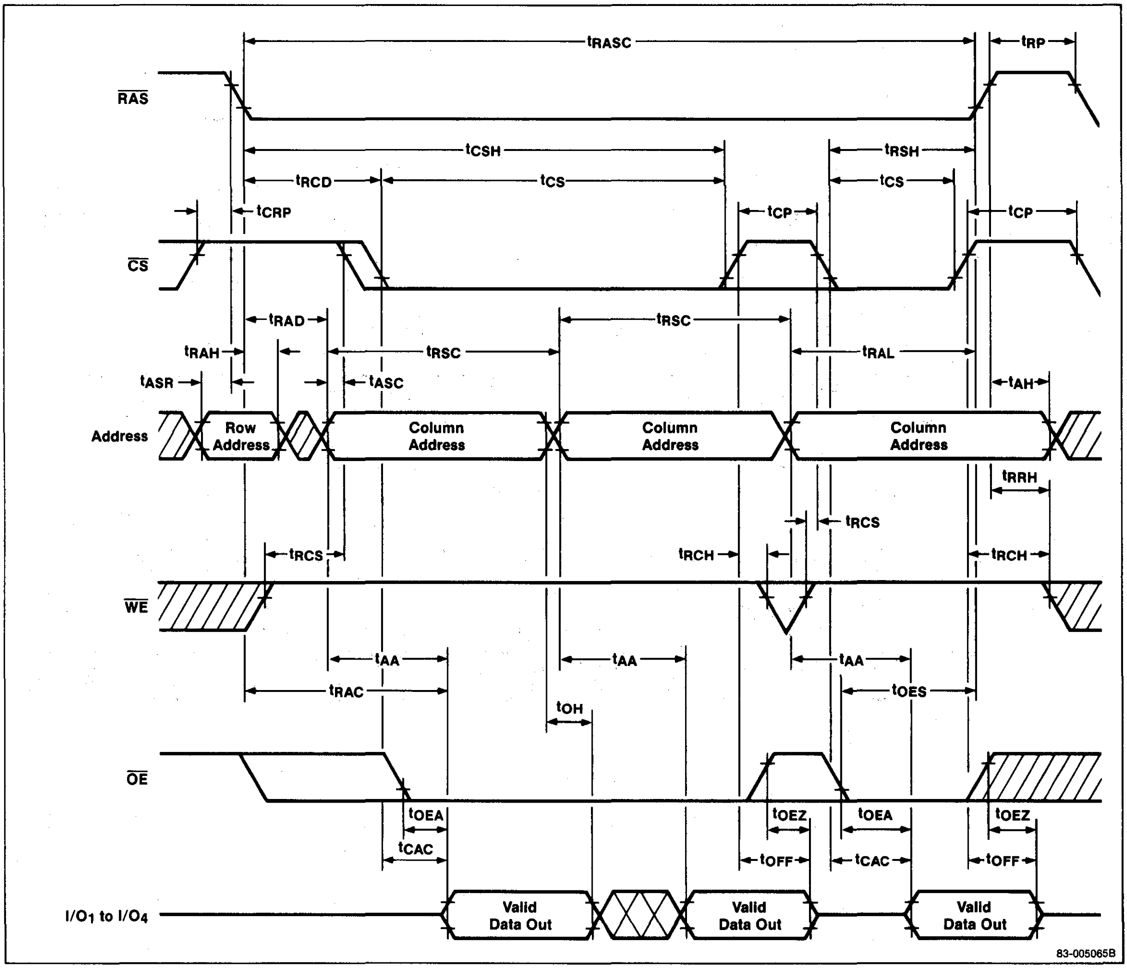
Timing Waveforms (cont)

Hidden Refresh Cycle



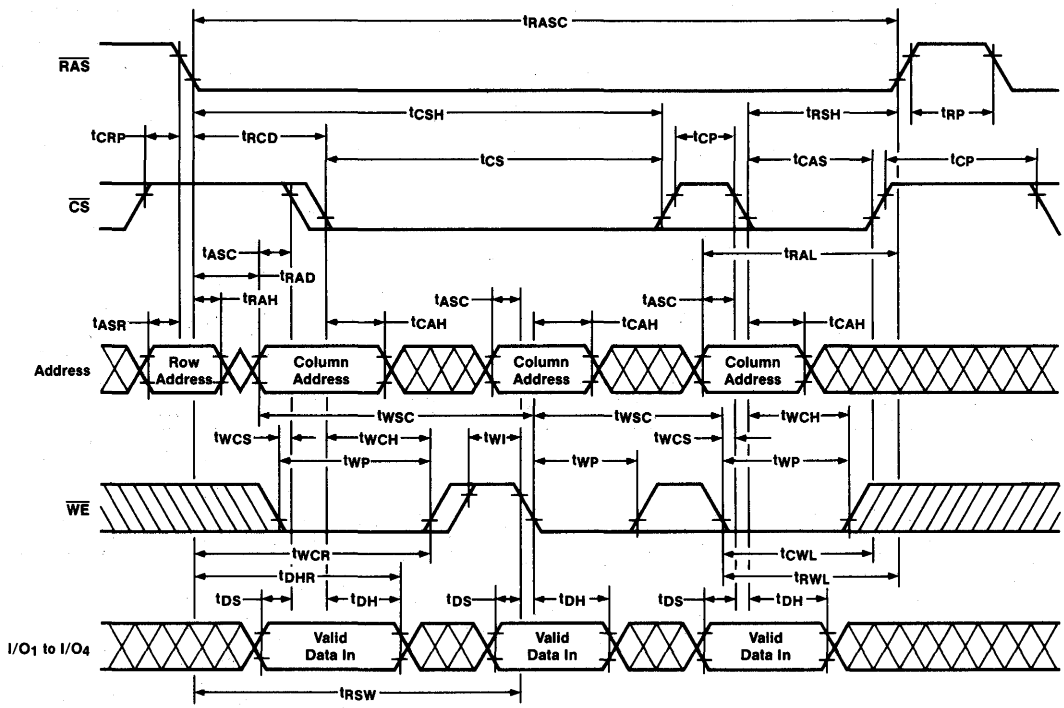
Timing Waveforms (cont)

Static-Column Read Cycle



Timing Waveforms (cont)

Static-Column Write Cycle (Early Write)



Note:
[1] $\overline{OE}$ = don't care.

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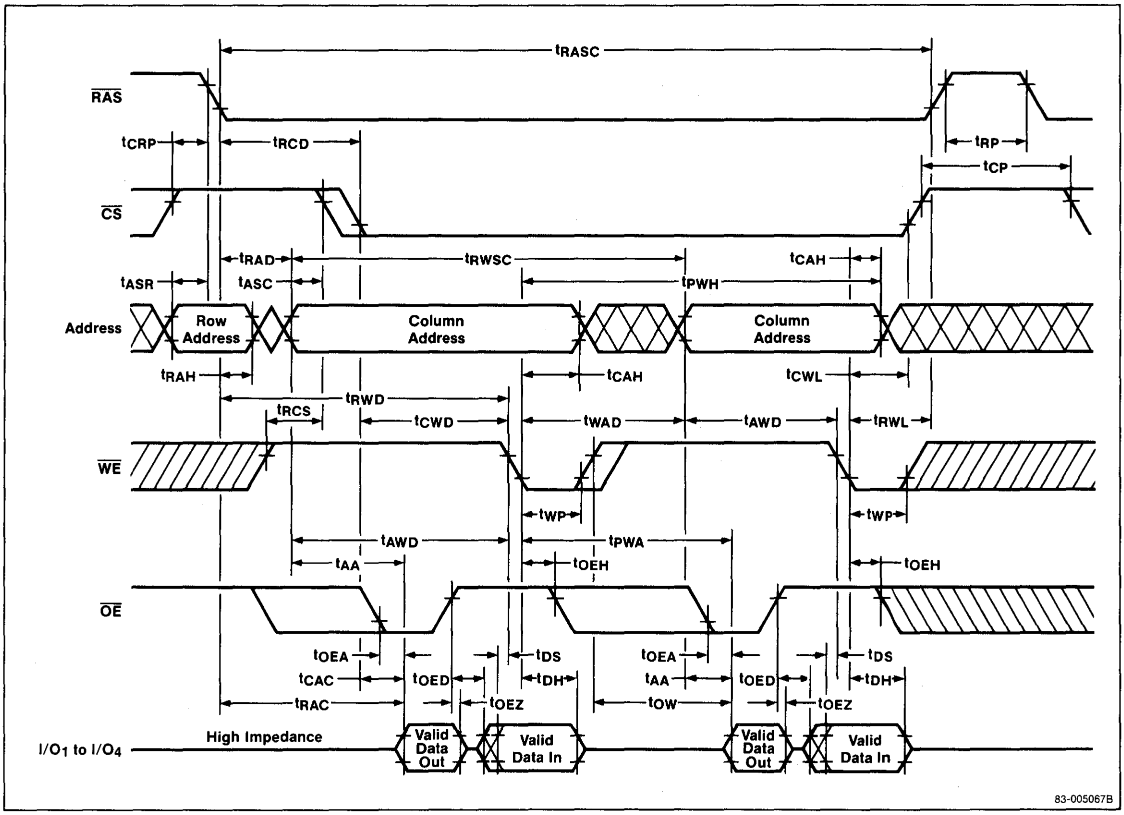
Timing Waveforms (cont)

Static-Column Read-Modify-Write Cycle



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APPLICATION NOTE 53
μPD421000/μPD421001/μPD421002 1-MEGABIT DYNAMIC RAMs

Description

NEC's μPD421000, μPD421001, and μPD421002 are 1-megabit dynamic RAMs (DRAMs) manufactured with the CMOS 1-μm fine-pattern process and configured as 1,048,576 x 1 bit. As shown in table 1, this family of DRAMs has been developed in a variety of speeds and packages. The package pin layouts appear in figure 1.

Configurations

The μPD421000, μPD421001, and μPD421002 (figures 2, 3, and 4) consist of memory cell arrays, input and output buffers, clock generators, refresh address counters, and row and column decoders.

The basic layout of the chips is shown in figure 5. As can be seen from the diagram, the whole memory cell array is divided into 16 smaller 64-kilobit arrays that are accessed separately.

Memory Cell Structure

Dynamic RAMs generally feature one-transistor memory cells, which require only about one-fourth of the area used by four-transistor and six-transistor (flip-flop) memory cells in static RAMs. Although a one-transistor cell provides a big advantage in reducing chip size, data must be rewritten (refreshed) at regular intervals for proper data storage on the memory cell capacitor. A cross-sectional view of the trench-type, one-transistor memory cell used in the μPD421000-series DRAMs is shown in figure 6.

This trench design uses three-dimensional rather than planar capacitors, thereby achieving a larger capacitance in a smaller surface area than in conventional circuits. The capacitance of this type of cell is determined by total trench area, the dielectric constant, and the thickness of the insulating film. To reduce soft errors caused by α-particles, an effective capacitance in excess of 50 femtofarads (fF) is used in the μPD421000, μPD421001, and μPD421002.

Figure 1. Pin Layouts

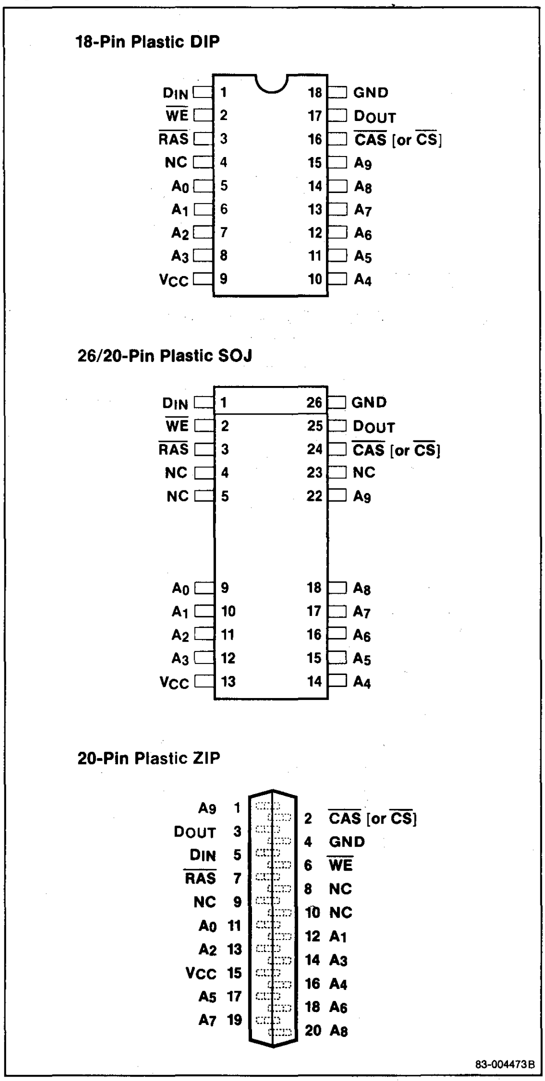

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Table 1. 1,048,576 x 1-Bit DRAM Family

Device	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (min)	Operating Current (max)	Standby Current (max)	High-Speed Mode	Packages
μPD421000-80	80 ns	160 ns	70 mA	1 mA	Fast Page	C = 18-pin plastic DIP
-10	100 ns	190 ns	60 mA	1 mA		V = 20-pin plastic ZIP
-12	120 ns	220 ns	50 mA	1 mA		LA = 26/20-pin plastic SOJ
μPD421001-80	80 ns	160 ns	70 mA	1 mA	Nibble	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		
μPD421002-80	80 ns	160 ns	70 mA	1 mA	Static Column	
-10	100 ns	190 ns	60 mA	1 mA		
-12	120 ns	220 ns	50 mA	1 mA		

Figure 2. μPD421000 Block Diagram

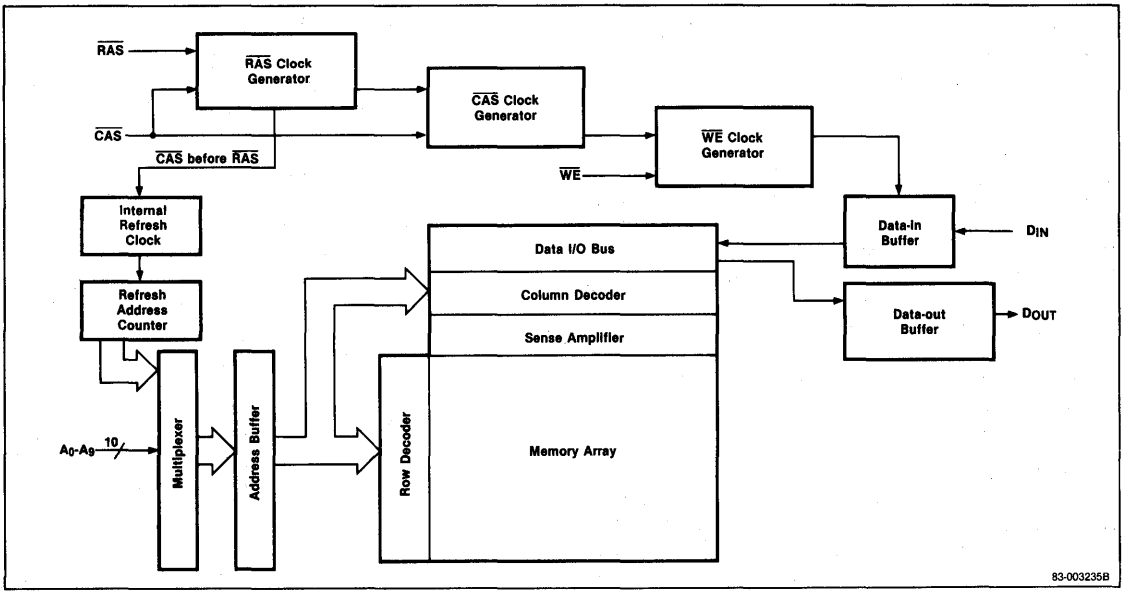

Figure 3. µPD421001 Block Diagram

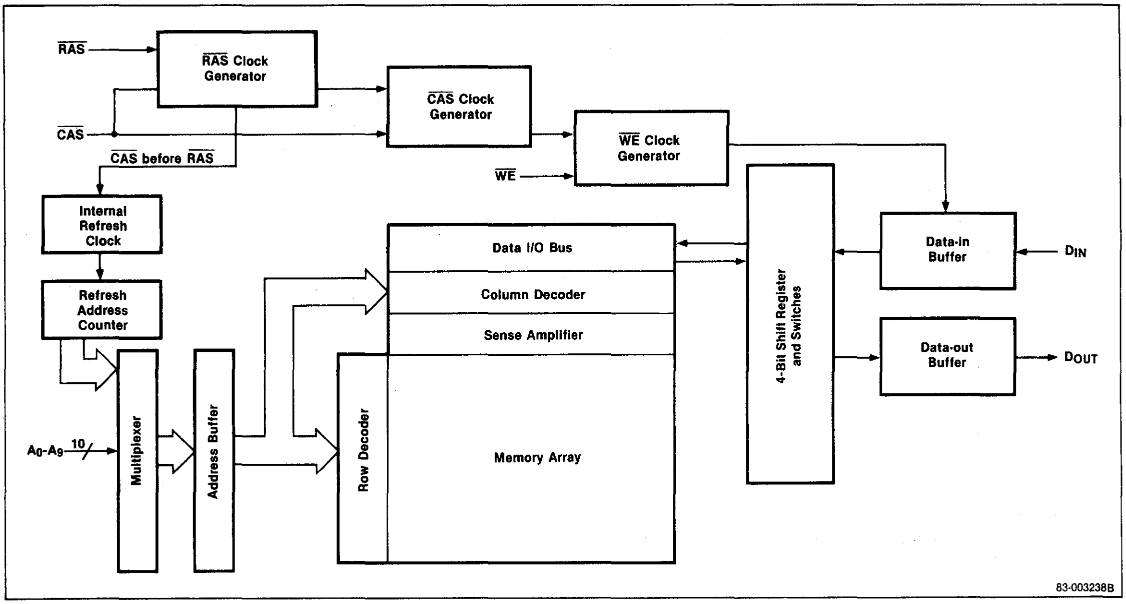

Figure 4. µPD421002 Block Diagram

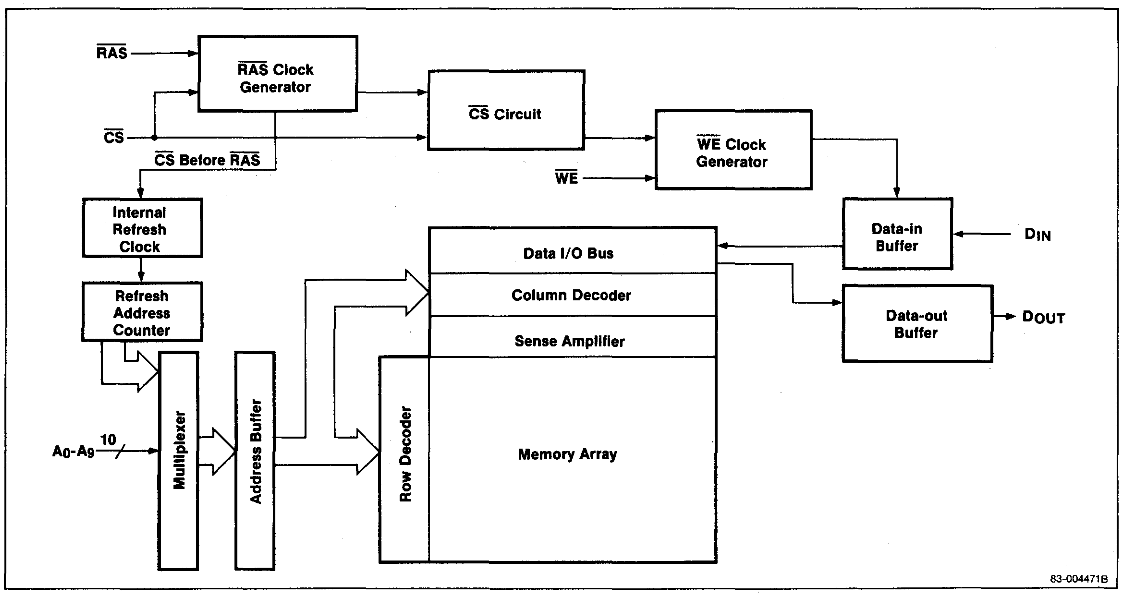

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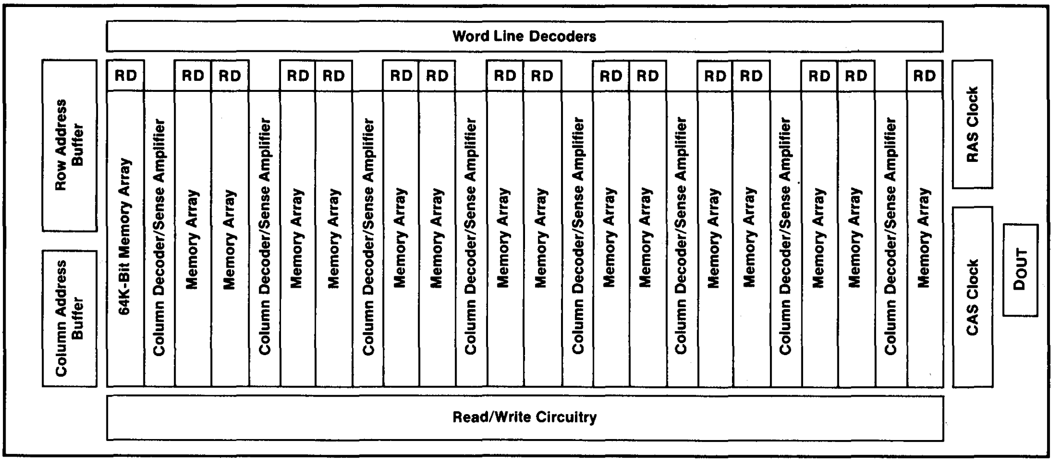
Figure 5. Chip Layout of μPD421000-Series DRAMs



Notes:
[1] The memory is divided into sixteen 64-kbit memory cell arrays.
[2] RD = row decoder/word driver.

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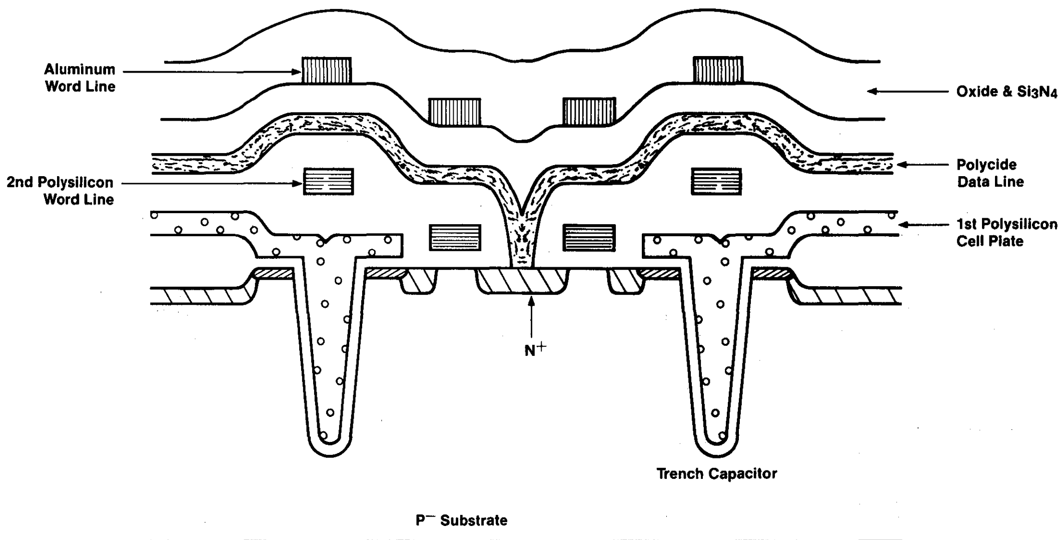
Figure 6. Cross Section of 1-Transistor Memory Cell



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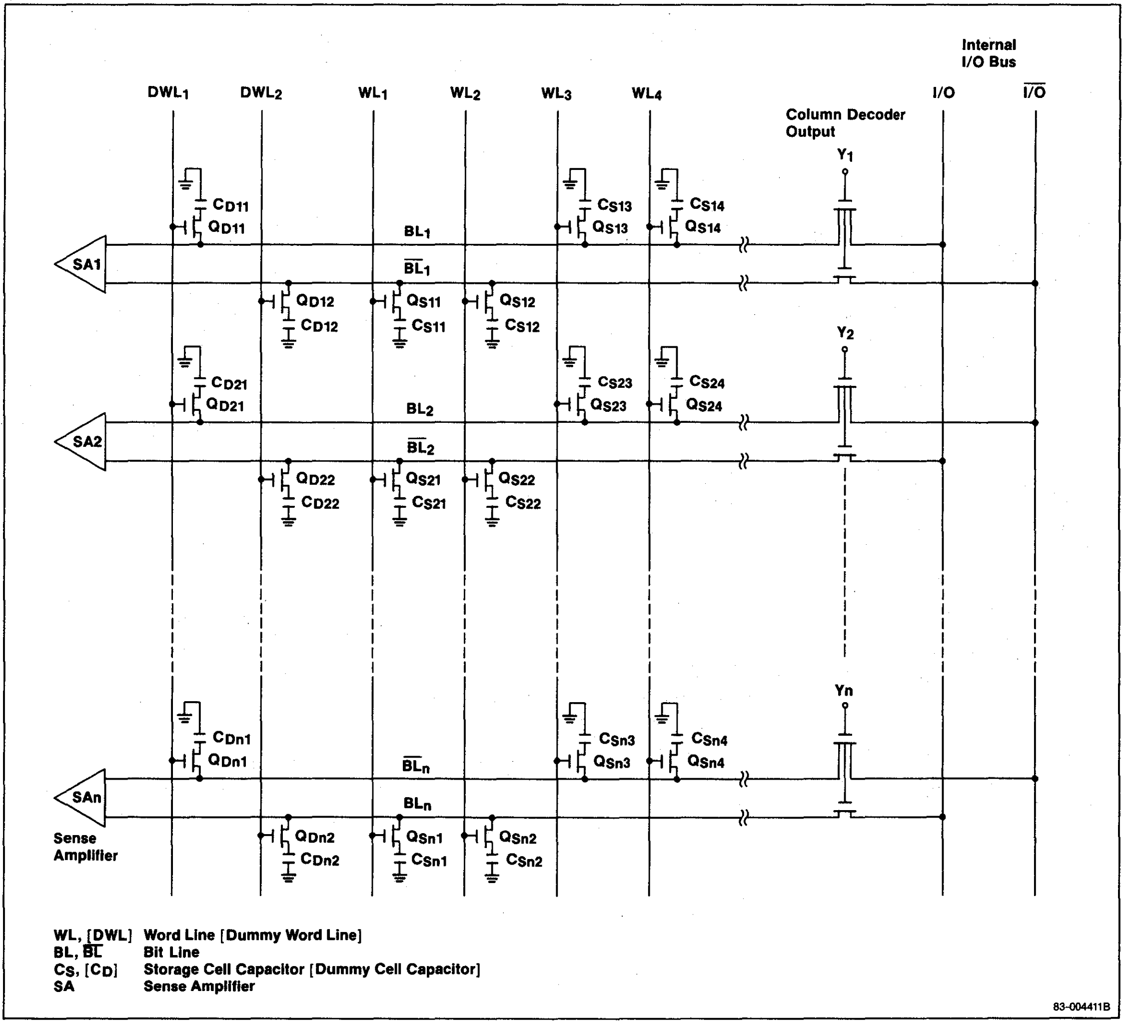
Read/Write Operation

In dynamic RAMs, changes in bit line potential caused by the minute charging and discharging of memory cells are amplified by a sense amplifier to be read as either 1 or 0. Memory cell and sense amplifier equivalent circuits are shown in figure 7.

To read the data from storage cell C_{S11}, the row address selects word line WL_1, and data from memory cells C_{S11}, C_{S21}, . . . , C_{Sn1} connected to WL_1 is passed to bit lines BL_1, BL_2, . . . , BL_n. These data signals are passed to the sense amplifiers, where they first are compared with data from dummy cells C_{D11}, C_{D21}, . . . , C_{Dn1}, connected simultaneously with the memory cells, and then amplified. At the same time, the original data is rewritten to memory cells C_{S11}, C_{S21}, . . ., C_{Sn1}. Switch Y_1 is then selected by the column address, and the C_{S11} data on the BL_1 line is passed via the I/O bus and a data amplifier to external circuits.

Write and read operations are identical, up to amplification and rewriting of memory cell data selected by a row address. After being passed to the bit line selected by the column address, write data is written into a target memory cell (such as C_{S11}). Since the number of memory cells selected by one row address in the devices is 2048, 2048 memory cells are refreshed simultaneously in each memory or refresh cycle.

Figure 7. Memory Cell and Sense Amplifier Equivalent Circuits



Pin Functions

$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ [or $\overline{\text{CS}}$]. The μPD421000-series DRAMs include two chip activator inputs: $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$), row address strobe and column address strobe (or chip select). In addition to reading row addresses A_0 through A_9, selecting the relevant word line, and activating the sense amplifiers for read and write operation, the $\overline{\text{RAS}}$ input also refreshes the 2048 bits selected by row addresses A_0 through A_8. The $\overline{\text{CAS}}$ input latches in column addresses (on the μPD421000 and the μPD421001) and connects the chip's internal I/O bus to the sense amplifiers activated by the $\overline{\text{RAS}}$ clock, thereby executing data input or output operations.

A_0 through A_9. Selection of an individual cell from the 1,048,576-word x 1-bit memory cell array requires a 20-bit address input. The three devices all feature an address multiplexing method in which an address is divided into two parts, the lower 10 bits (row address) and the upper 10 bits (column address).

The row address is latched into memory at the falling edge of the $\overline{\text{RAS}}$ clock. After an internal timing delay, the column address input circuits become active. Flow-through latches (voltage-level activated, not edge-triggered) for column addresses are enabled on the μPD421000 or μPD421001, and the column addresses immediately begin propagating through the latches to the column decoders. A column address is held in the latches by the falling edge of $\overline{\text{CAS}}$. For read cycles on the μPD421002, the column address input circuitry is not controlled by $\overline{\text{CS}}$, and column addresses must be held valid until data is read out.

Setup times (t_{ASR} and t_{ASC}) and hold times (t_{RAH} and t_{CAH}) for address inputs are defined in relationship to the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ ($\overline{\text{CS}}$ or $\overline{\text{WE}}$ for write cycles on the μPD421002). In actual operation, a row address is specified before the $\overline{\text{RAS}}$ input is activated; once the address bus switches to column addresses, $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) is activated.

$\overline{\text{WE}}$ [Write Enable]. Read and write cycles are executed by activating the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) inputs and controlling $\overline{\text{WE}}$. An early write cycle is executed if $\overline{\text{WE}}$ is activated before the falling edge of $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) during a write cycle, and a late write (read-modify-write) cycle is executed if the $\overline{\text{WE}}$ input is activated later.

Read and Write Cycles

Read cycles are executed by activating $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) with the $\overline{\text{WE}}$ input at a high level (inactive). The $\overline{\text{RAS}}$ access time of t_{RAC} is valid if the delay from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) is less than t_{RCD} (max), and the delay from $\overline{\text{RAS}}$ to the column address is less than t_{RAD} (max). The $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) access time of t_{CAC} is valid if the delay from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) is greater than t_{RCD} (max), and the delay from the column address to $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) is greater than t_{ASC} (max). The address access time of t_{AA} is valid if the delay from $\overline{\text{RAS}}$ to the column address is greater than t_{RAD} (max), and the delay from the column address to $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) is less than t_{ASC} (max). Output data is held valid until $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) becomes inactive again (figure 8).

Write cycles are executed by activating the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$), and $\overline{\text{WE}}$ inputs. Write data is latched by the falling edge of $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) or $\overline{\text{WE}}$, whichever occurs later.

A $\overline{\text{WE}}$ input applied before the $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) input initiates an early write cycle, whereby write data is latched by the falling edge of $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$).

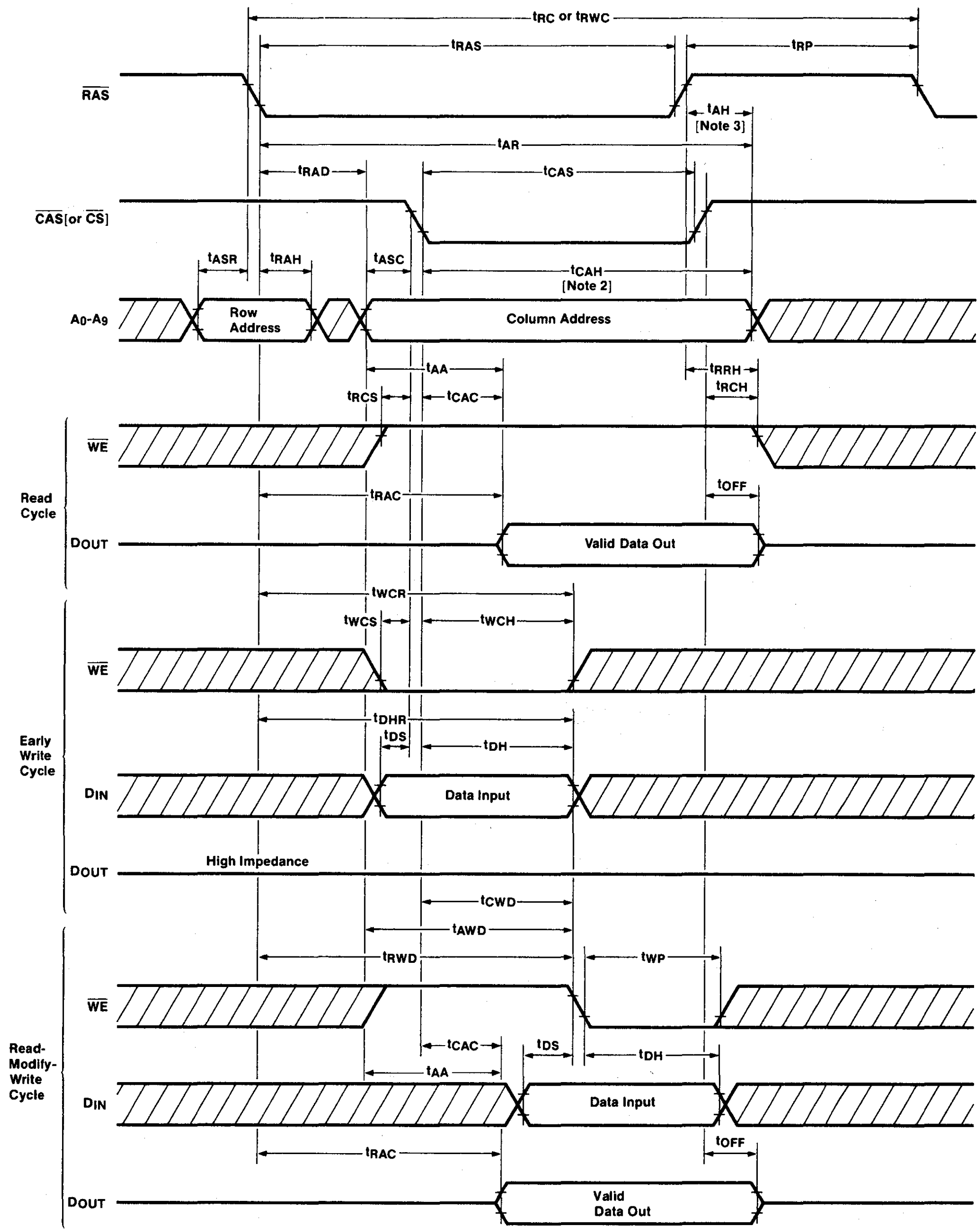
Conversely, a $\overline{\text{WE}}$ input applied after the $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) input initiates a late write cycle (read-modify-write cycle), whereby write data is latched into the chip by the falling edge of $\overline{\text{WE}}$. The status of D_{OUT} is not guaranteed in this case, but depends on the timing of $\overline{\text{WE}}$ with respect to $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$). If $\overline{\text{WE}}$ is activated at least t_{CWD} after the $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) input, and at least t_{RWD} after the $\overline{\text{RAS}}$ input, write operation is enabled in the same memory cycle during which the read data is valid.

Refresh Cycles

The process of rewriting data held in a memory cell, refreshing, is performed by a sense amplifier in the μPD421000-series DRAMs. The three devices are capable of executing the same $\overline{\text{RAS}}$-only and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$)-before-$\overline{\text{RAS}}$ refresh cycles as are executed in other conventional, general-purpose DRAMs. All 512 rows of memory cells must be refreshed within any 8-ms period.

Since in image memory applications, row addresses A_0 through A_8 are read or written sequentially within 8 ms, the accessing itself initiates refreshing and no additional refresh cycles are required.

Figure 8. Access Timing



Notes:
[1] In a read-modify-write cycle, cycle time is defined as $t_{RWC} = t_{RWD} + t_{RWL} + 3\,t_T + t_{RP}$.
[2] Timing t_{CAH} applies to the μPD421000 and the μPD421001.
[3] Timing t_{AH} applies to the μPD421002.

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$\overline{\text{RAS}}$-Only Refresh Cycle. $\overline{\text{RAS}}$-only refreshing is executed simply by leaving the $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) input inactive (high level) during a $\overline{\text{RAS}}$ clock cycle. This cycle uses the 512 lower addresses specified by row addresses A_0 through A_8 to ensure that all memory cell bits are refreshed. Hence, 2048 bits of memory are refreshed in a single cycle (figure 9).

$\overline{\text{CAS}}$ [or $\overline{\text{CS}}$]-Before-$\overline{\text{RAS}}$ Refresh Cycle. This type of refreshing is executed using the addresses generated by the chip's internal address counter when $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) is activated (low level) in advance of the $\overline{\text{RAS}}$ input (figure 10).

Even in systems without an address output from the microprocessor, no additional external address counter or refresh address selector is required. $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$)-before-$\overline{\text{RAS}}$ refreshing allows refreshing to be accomplished with a minimum of peripheral circuits (figure 11).

High-Speed Access Cycles

In addition to being capable of standard access, the μPD421000 is equipped with fast-page access, the μPD421001 with nibble access, and the μPD421002 with static-column access (table 2).

Figure 9. $\overline{\text{RAS}}$-Only Refresh Cycle

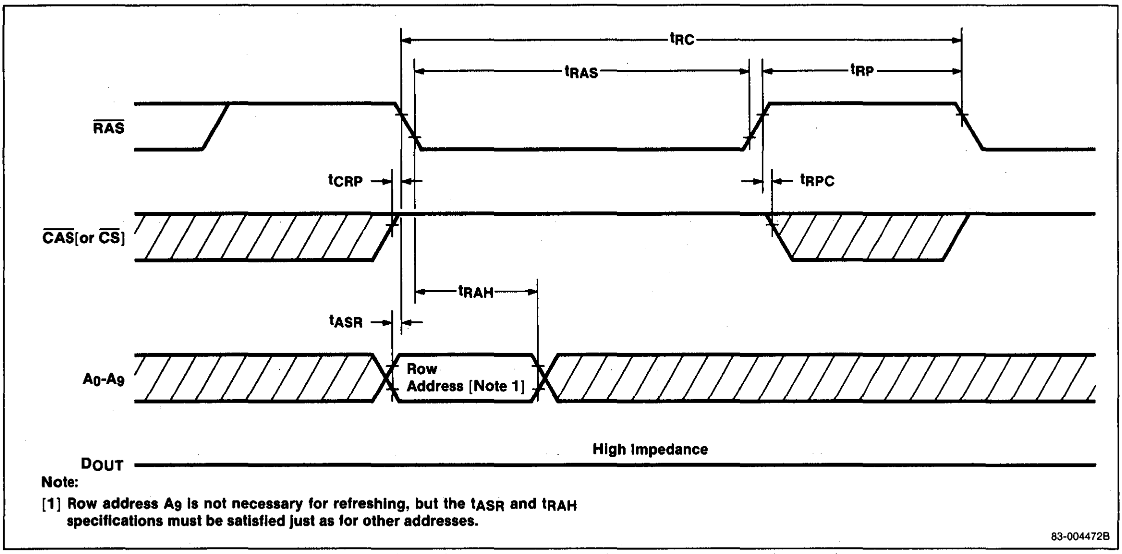

Figure 10. $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$)-Before-$\overline{\text{RAS}}$ Refresh Cycle

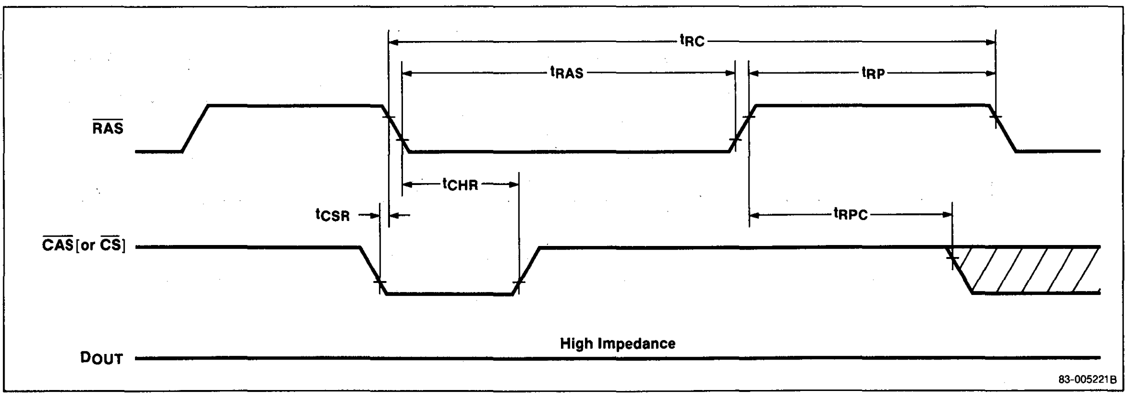

Figure 11. Address Multiplexing

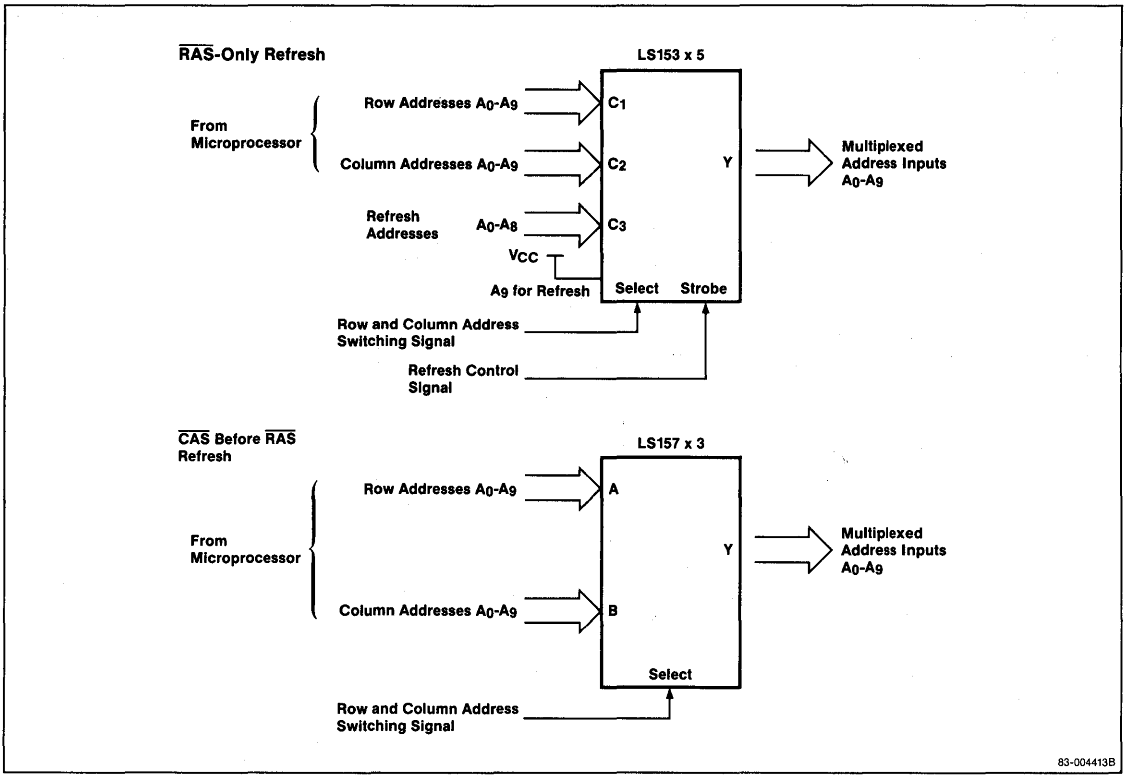

Table 2. Major Characteristics of Fast-Page, Nibble, and Static-Column Modes

Device	Access Time (max)	Cycle Time (min)	Internal Address Usage	High-Speed Access
μPD421000-80	45 ns	50 ns	Row: Page selection Column: Individual cell access on one page	Random access on one page selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		
μPD421001-80	20 ns	40 ns	Row, Column: A_9 inputs set starting location for nibble-mode access	Serial access (4 bits maximum)
-10	25 ns	45 ns		
-12	30 ns	55 ns		
μPD421002-80	45 ns	50 ns	Row: Row selection Column: Individual cell access on one row	Random access on one row selected by A_0 through A_9
-10	50 ns	60 ns		
-12	60 ns	70 ns		

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Fast-Page Mode. Fast-page mode makes it possible to randomly access data in the same row address (figures 12 and 13). The 1024 bits of memory are obtained from the combinations of column address inputs A_0 through A_9 within one row address in the μPD421000. Up to 1998 continuous accesses can be executed on the 80-ns version before the maximum interval for t_{RASP} (100 μs) is reached.

The t_{PC} cycle time for random fast-page read or write cycles is equivalent to $t_{CAS} + t_{CP} + 2t_T$.

Figure 12. Memory Cell/Sense Amplifier Block of the μPD421000

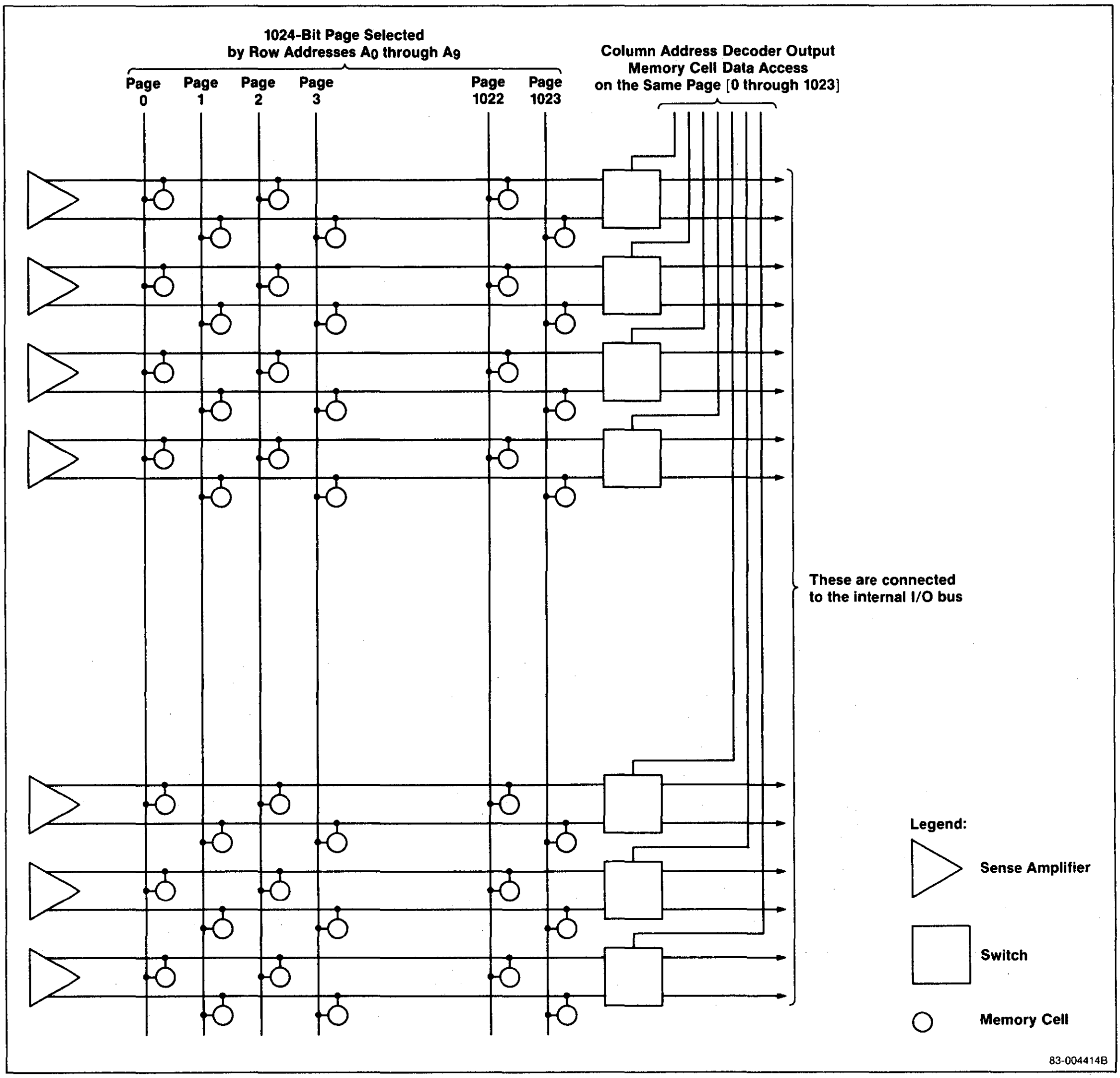
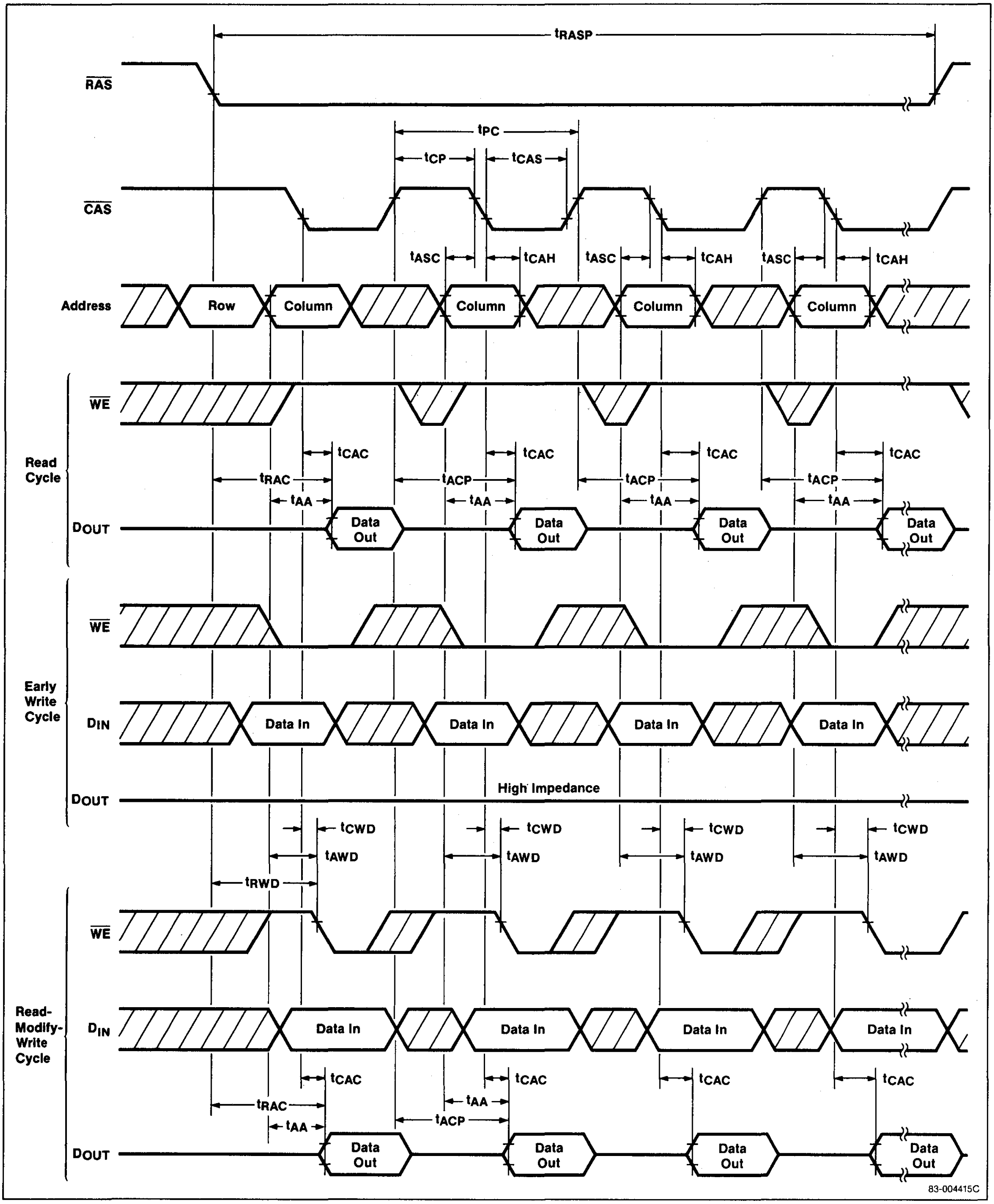
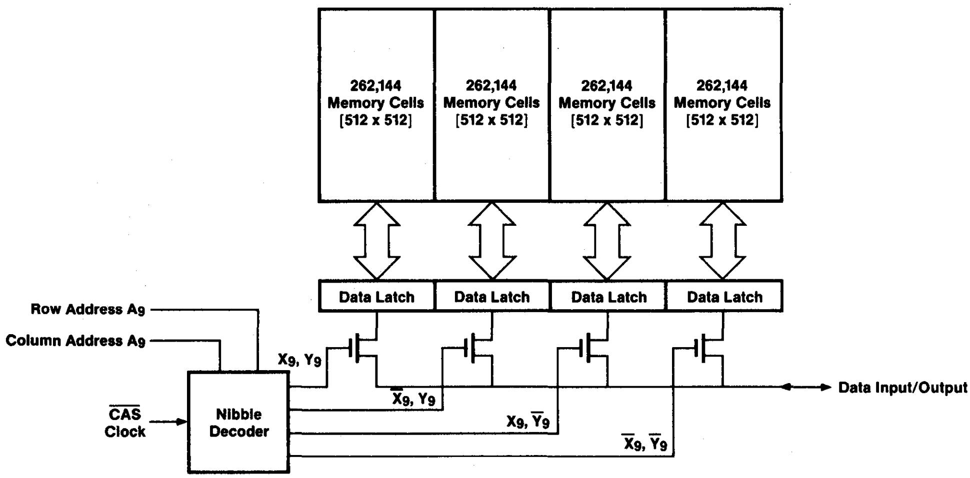


Figure 13. Fast-Page Timing



Nibble Mode. In nibble-mode cycles, the first data location is specified by row and column addresses A_0 through A_9 during a read or write cycle (table 2 and figures 14 and 15). When the μPD421001 internally sequences the two highest-order addresses (A_9) during the next $\overline{CAS}$ clock cycle, read and write cycles can be executed in less time than in fast-page operation.

Figure 14. Nibble-Mode Block Diagram and Example of Access Sequence



Sequence	Nibble Bit	Row Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Column Address A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Comment
$\overline{RAS}$/$\overline{CAS}$	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	External address
$\overline{CAS}$ Cycling	2	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	3	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	Internal address
$\overline{CAS}$ Cycling	4	1	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	
$\overline{CAS}$ Cycling	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	Repeated sequence

Notes:

[1] X_9 = Row address A_9

[2] Y_9 = Column address A_9

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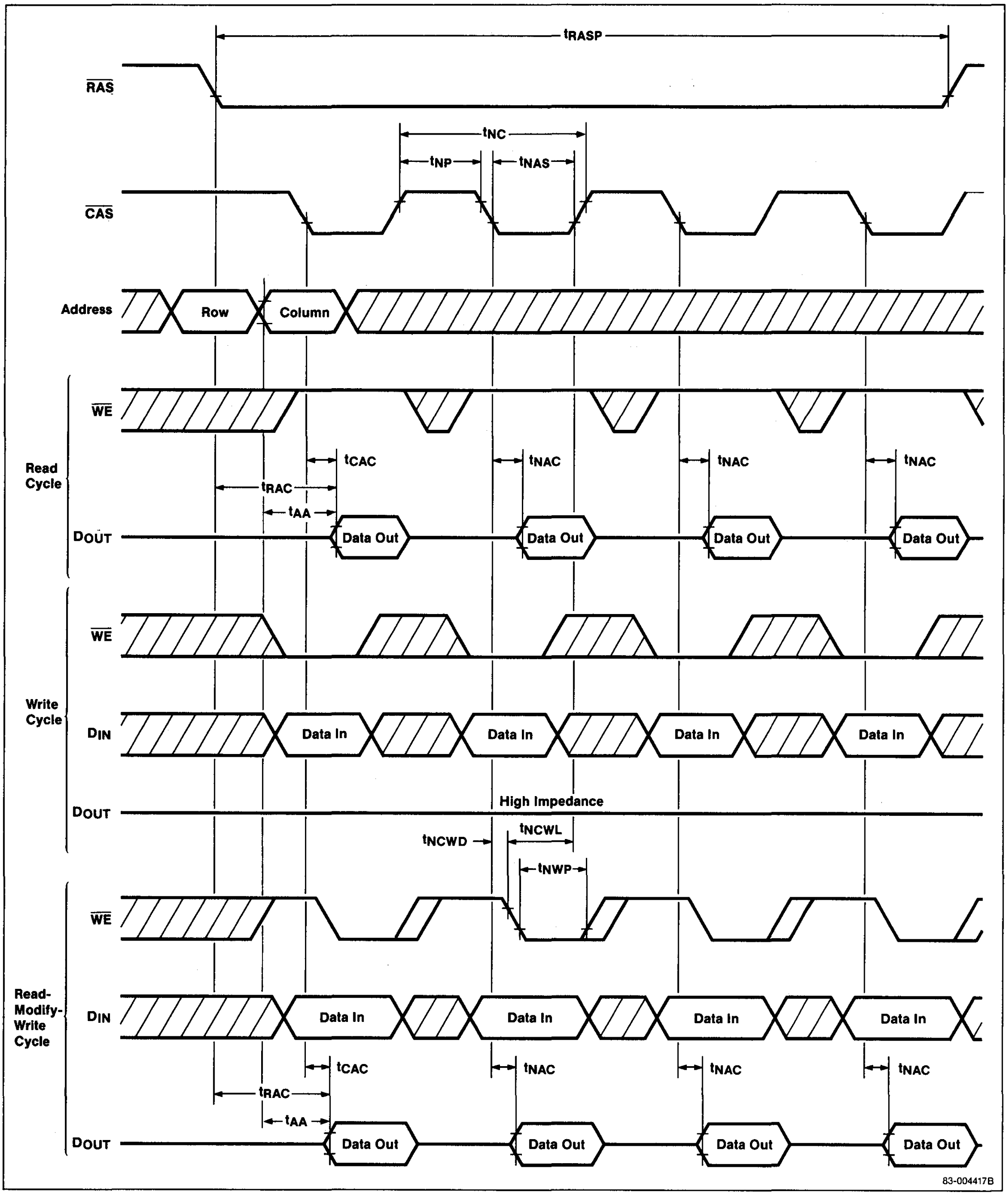
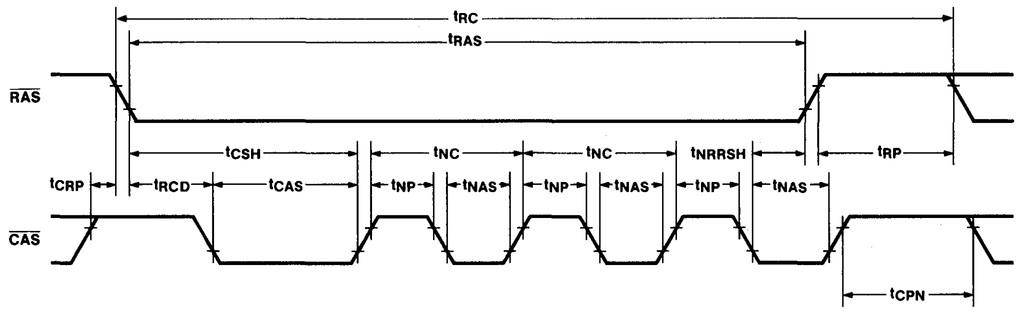
Figure 15. Nibble-Mode Timing



For the 80-ns version, the average cycle time per bit in nibble mode is 70 ns, when 4 bits are accessed during a long t_{RAS} cycle (figure 16). By using multiple μPD421001 devices, high-speed cache and frame buffer applications are possible (figure 17).

Figure 16. Average Data Rate in Nibble Access



Notes:

[1] **Minimum t_{RC} [ns] in nibble mode:**

$= t_{CSH} + t_{NC} \times 2 + t_{NP} + t_{NRRSH}$ or $t_{NWRSH} + t_{RP} + t_T \times 4$

$= 80 + 40 \times 2 + 10 + 20 + 70 + 20$

$= 280$ ns [for 4 bits]

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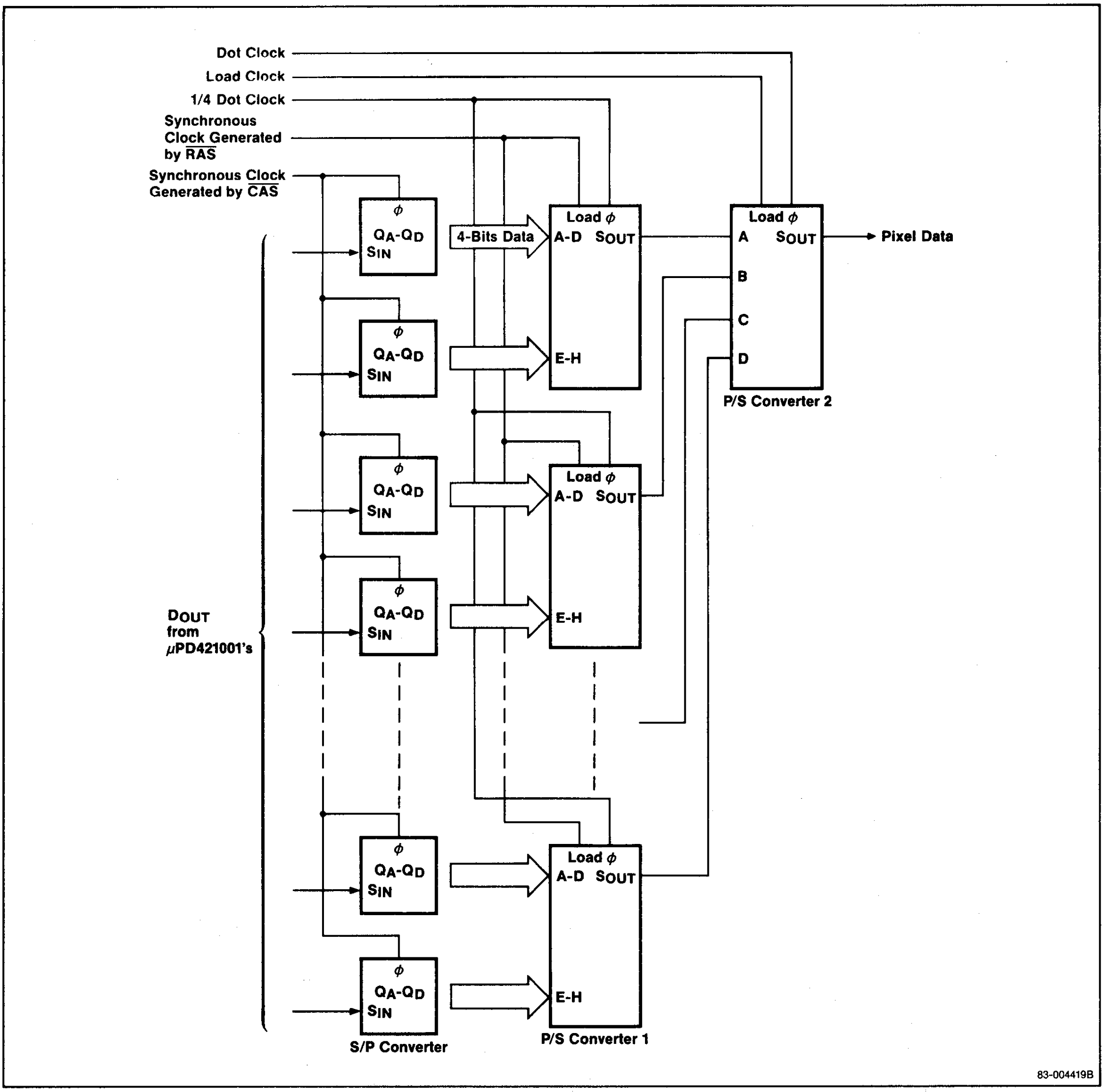
Figure 17. High-Speed Data Access Using Nibble Mode



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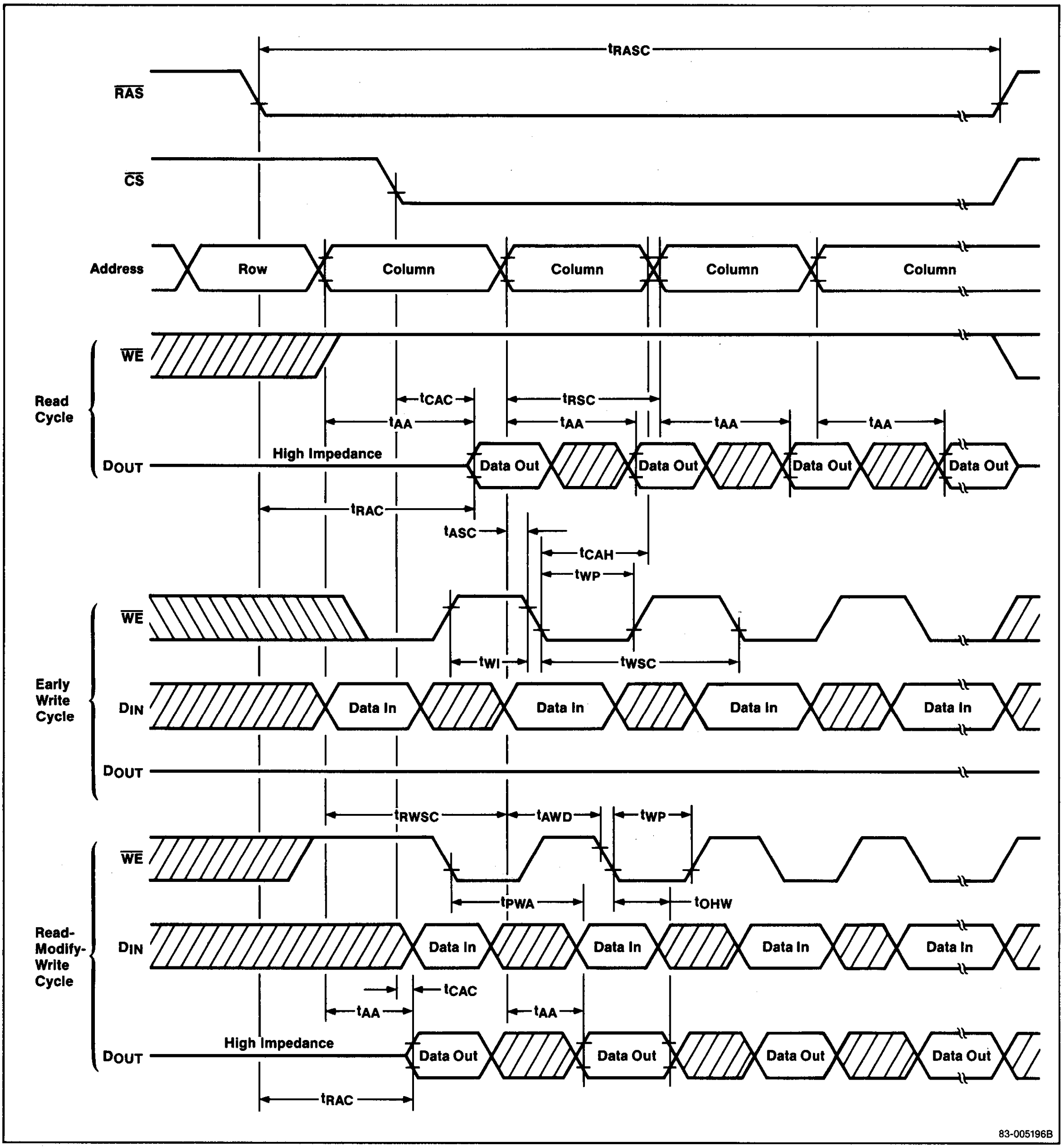
Static-Column Mode. Row and column addresses are functionally equivalent in static-column and fast-page access. The available number of continuous accesses on one row, and the cycle timing, are also similar to fast-page operation.

In a static-column device, there are no setup or hold timing requirements for read addresses; $\overline{CS}$ may be held low continuously in the ON-state. To allow this feature, the column addresses must be maintained as valid inputs for the duration of each cycle. There are few other restrictions on timing (figure 18).

Figure 18. Static-Column Timing



Precautions

Precautions when using the μPD421000, μPD421001, μPD421002, and other DRAMs should be carefully observed in the areas listed below:

- Power-on and initialization
- Supply voltage fluctuations caused by peak currents
- Relationships between address/data inputs and drivers
- $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) generation

Power-On and Initialization. Dynamic RAMs operate by the charging and discharging of gate and internal circuit capacitances. Therefore, dummy $\overline{\text{RAS}}$ clock cycles must be executed to charge internal potentials to the prescribed levels when power is applied. Dummy $\overline{\text{RAS}}$ cycles are also necessary when there has been no accessing (reading, writing, or refreshing) for periods longer than the refresh interval (figure 19).

To control transistor threshold voltages and decrease internal stray capacitance, DRAMs are usually equipped with a substrate voltage generator circuit to supply the chip's interior with negative voltage. Approximately 100 μs is required to generate an adequate negative voltage level after power is applied and $V_{CC} \geq 4.5$ V.

When the power is switched on, a peak current dependent on the levels of $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$), and $\overline{\text{WE}}$ is reached during the rising of V_{CC}. This peak current—maximum when $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) are active and $\overline{\text{WE}}$ is inactive—can be minimized by using clock input pullups on $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) so that their rise times correspond to the rise time of the power supply.

Supply Voltage Fluctuations. Since 1 and 0 logic (storage) operations are executed by the charging and discharging of capacitances, including the memory cells, the peak current generated is dependent on charge and discharge timing.

This peak current is concentrated just after $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ (or $\overline{\text{CS}}$) transition intervals (figure 20) with a peak value of about 120 mA. Since this current is a source of noise (voltage drop) in the memory system supply voltage, decoupling by multilayer ceramic capacitors with excellent frequency response is necessary. If the average of the 120-mA peak current pulse lasts about 100 ns, the capacitance required to keep the drop in the supply voltage line at about 0.1 V will be calculated as follows:

$$C = \frac{120\ (\text{mA}) \times 100\ (\text{ns})}{0.1\ (\text{V})}$$

$$= 120 \times 10^3\ \text{pF}$$

$$= 0.12\ \mu\text{F}$$

Therefore, when designing the memory board, keep the power and ground leads as short as possible for low inductance. Decoupling capacitors of about 0.2 μF must be inserted between the power supply lines for each memory device. With careful board layout, the use of fewer but larger capacitors is possible. Capacitors used in one of every two memory device locations, with a value of perhaps 0.33 μF, can provide satisfactory decoupling in many cases.

Figure 19. Dummy Cycles after Power Is Applied

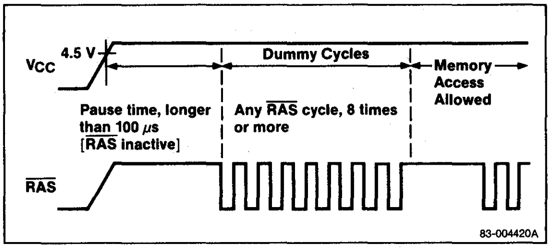
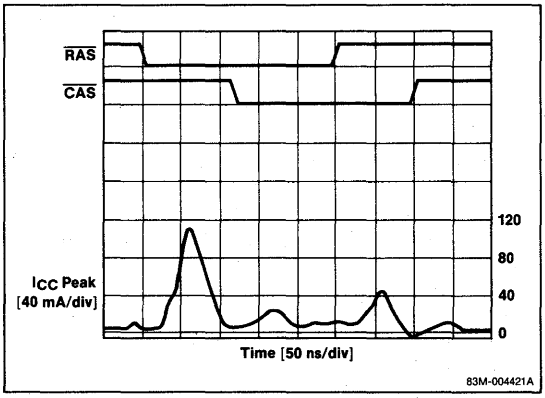


Figure 20. Operating Current Waveform



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Address/Data Inputs and Drivers. Probably the most important consideration in DRAM timing is the relationship between address/data inputs and the external drivers. In address-multiplexed DRAMs such as the μPD421000, μPD421001, and μPD421002 (where row and column addresses are supplied as two sets of inputs), addresses supplied externally have to be switched by a multiplexer.

The sequence of this timing must be designed very carefully. A timing sequence starts with the setting of row addresses. Next, $\overline{RAS}$ falls. After the specified hold time for row addresses is met, the addresses are switched to set up column address input. Once $\overline{CAS}$ (or $\overline{CS}$) falls, the specified hold time for column addresses must be satisfied.

When $\overline{CAS}$ (or $\overline{CS}$) is activated within the time specified for t_{RCD} (max), the setup time for column addresses is more difficult to guarantee than when t_{RCD} is longer than t_{RCD} (max), because one external address driver has to drive more than one address pin in an array of DRAMs. The address multiplexer's delay time is increased by load capacitances larger than the typical value.

For illustration, measurements of output delay times for certain drive load capacitances are shown in figure 21.

In the design of high-density memory boards having a large number of memory devices, partitioning of drivers becomes necessary because of wiring and through-hole capacitances. Special care must be taken to ensure that the setup and hold times for addresses conform with the specifications. Otherwise, invalid or undefined addresses may be latched into the chip, and data may be destroyed even if nothing is written.

$\overline{RAS}$ and $\overline{CAS}$ [or $\overline{CS}$] Generation. In addition to reading the address inputs, $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) also generate the basic timing for all DRAM circuit operations. The internal timing generators are connected in daisy-chain fashion, and are completely controlled by the basic $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs. Because of this control, the memory system design must prevent noise glitches from being generated in the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) inputs.

$\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is specified in terms of minimum values. High- or low-level pulses that do not satisfy these minimum values can result in incorrect output data (because there is insufficient time for sense amplifier operation), and can also lead to destruction of write data. Therefore, the prevention of noise glitches must be carefully considered in logic and circuit design.

Figure 21. Effect of Load Capacitance on TTL (7404) Output

Delay and Transition Times

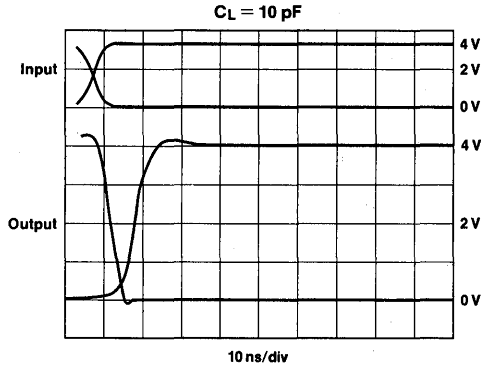
Parameter	Time [ns] $C_L = 10$ pF	$C_L = 110$ pF	$C_L = 210$ pF
t_{PLH}	9	16.5	26
t_{PHL}	5.5	12.5	17
t_R	3.2	7.8	15
t_F	1.5	3.8	5.5

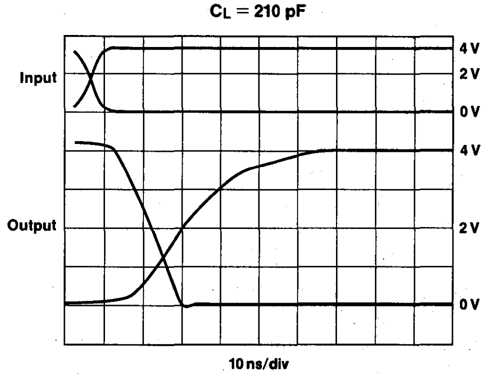
Notes:

[1] t_{PLH}, t_{PHL} are defined as the delay time from $V_{IN} = 1.5$ V to $V_{OUT} = 2.4$ V or 0.8 V.

[2] t_R and t_F are defined as the transition time between V_{OH} [min] and V_{OL} [max].

[3] Load capacitance C_L includes the oscilloscope input capacitance.





83-005257B

V40™ MICROPROCESSOR APPLICATION

Features

The μPD70208 (also known as V40) is a high-performance 8-bit CMOS microprocessor featuring 16-bit architecture in the CPU, and including a number of other peripheral devices within the same chip. The CPU is equipped with a powerful set of instructions that cover bit processing and multiple-length, packed-BCD operations, high-speed multiplications and divisions, and variable-length bit and field manipulations.

This device combines high-speed processing with flexibility in a variety of applications. The on-chip peripherals include a clock generator with a timer/counter and programmable wait control, refresh control, serial control, interrupt control, and DMA control units. In addition to allowing more compact microcomputer systems, the V40 has a simplified system design.

When connected to the μPD421000-series DRAMs, the V40 does not require an external refresh timer or other peripherals, which means a big reduction in the number of external devices required.

Memory Mapping

In the V40, memories of up to 1 megaword can be accessed using address information (A_{19} through A_0) output from the 20-bit address bus (figure 22).

The first 1024 bytes, 0 through 3FFH, are allocated to interrupt vectors (although areas that cannot be used by the system can be used elsewhere). Addresses FFFF0H through FFFFBH are used for starting and resetting purposes; FFFFCH through FFFFFH are reserved for future use and cannot be used here. The remaining address space, 400H through FFFEFH, is not allocated and may be used as desired.

As shown in figure 23, with a data bus width of 8 bits in the V40, CPU connections to the memory require only that the 20-bit address output from the CPU be accepted in the 1-megabyte address space. Byte data is accessed in one bus cycle, and word data is accessed in two bus cycles.

V40 is a trademark of NEC Corporation.

Because of this simple connection requirement, it is only necessary to allocate the system control ROM to addresses of at least FFFF0H and disable the ROM-area RAM (since 1 megabyte is already taken up by eight 1-megabit DRAMs). The method used may involve either deselecting the ROM-area RAM by a decoder, or executing bank switching to use the entire area as RAM area. The example included for this application shows the former method because it is simpler.

Figure 22. V40 Memory Mapping

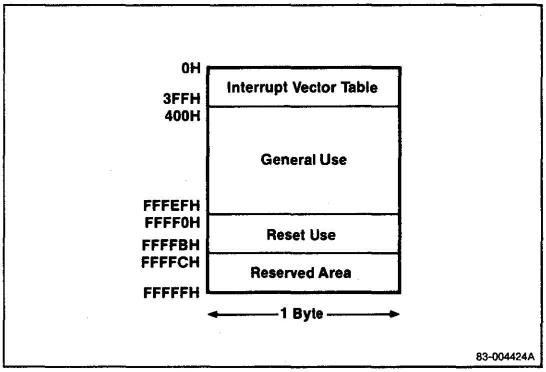
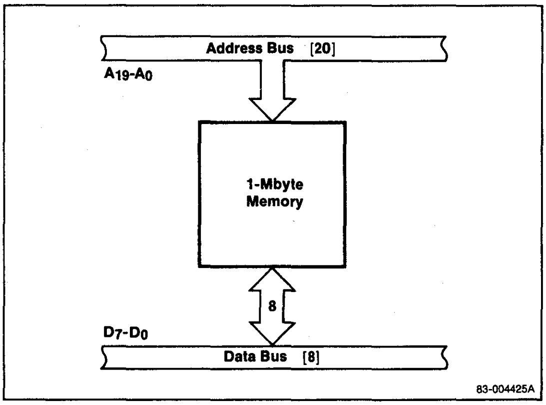


Figure 23. V40 Memory Interface



Hardware Configuration

Since refresh addresses and the timing control outputs can be supported by programming on-chip circuits, the generation of $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing is the only major DRAM support not provided directly by the V40 (figure 24).

Memory Access Timing Generation

Although V40 memory access timing can be generated from either the bus status or MWR/$\overline{MRD}$, the μPD71088 system bus controller is used in this application example to enable connections to slightly slower-speed memories. The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) signals are thus generated by decoding the bus status.

The $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) generator is shown in figure 25, and the operation timing in figure 26. To generate the control timing with this system controller, bus status signal BS_2 is sampled by the CPU clock output (ϕ_{OUT}) at the rising edge of the T_1 cycle, and $\overline{RAS}$ is generated from FF2 at the falling edge of ϕ_{OUT} at the end of T1. The multiplex control signal (MPX) used in address switching during memory cycles is generated by $\overline{RAS}$. After $\overline{RAS}$ is generated, it is delayed by the rising edge of the external 16-MHz clock to create MPX, which is then passed to the data selector input.

As can be seen from figure 26, memory access time is equal to $2/f(\phi_{OUT}) - (t_{SDK} + \text{TTL delay time})$. Even if an external clock of 16 MHz is used, a -12 device is sufficient ($\overline{RAS}$ access time in the -12 device is 120 ns).

Figure 24. Hardware Configuration for the Use of 1M DRAMs

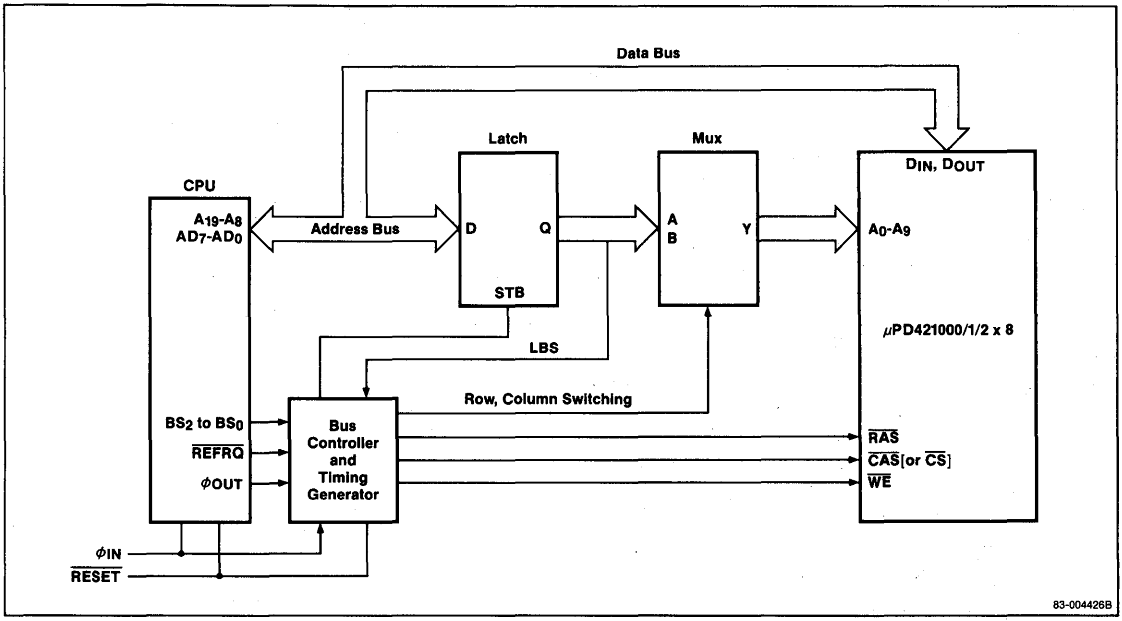


Figure 25. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Generator

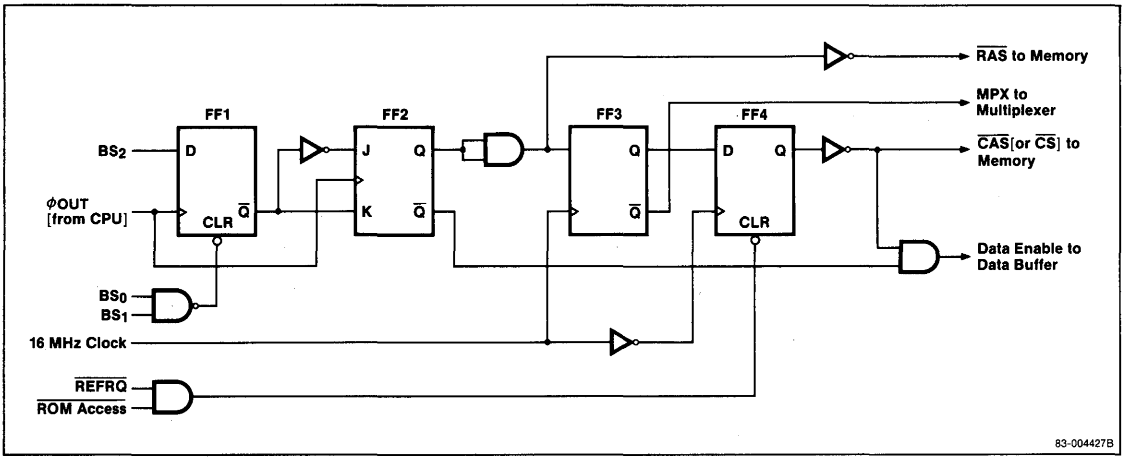
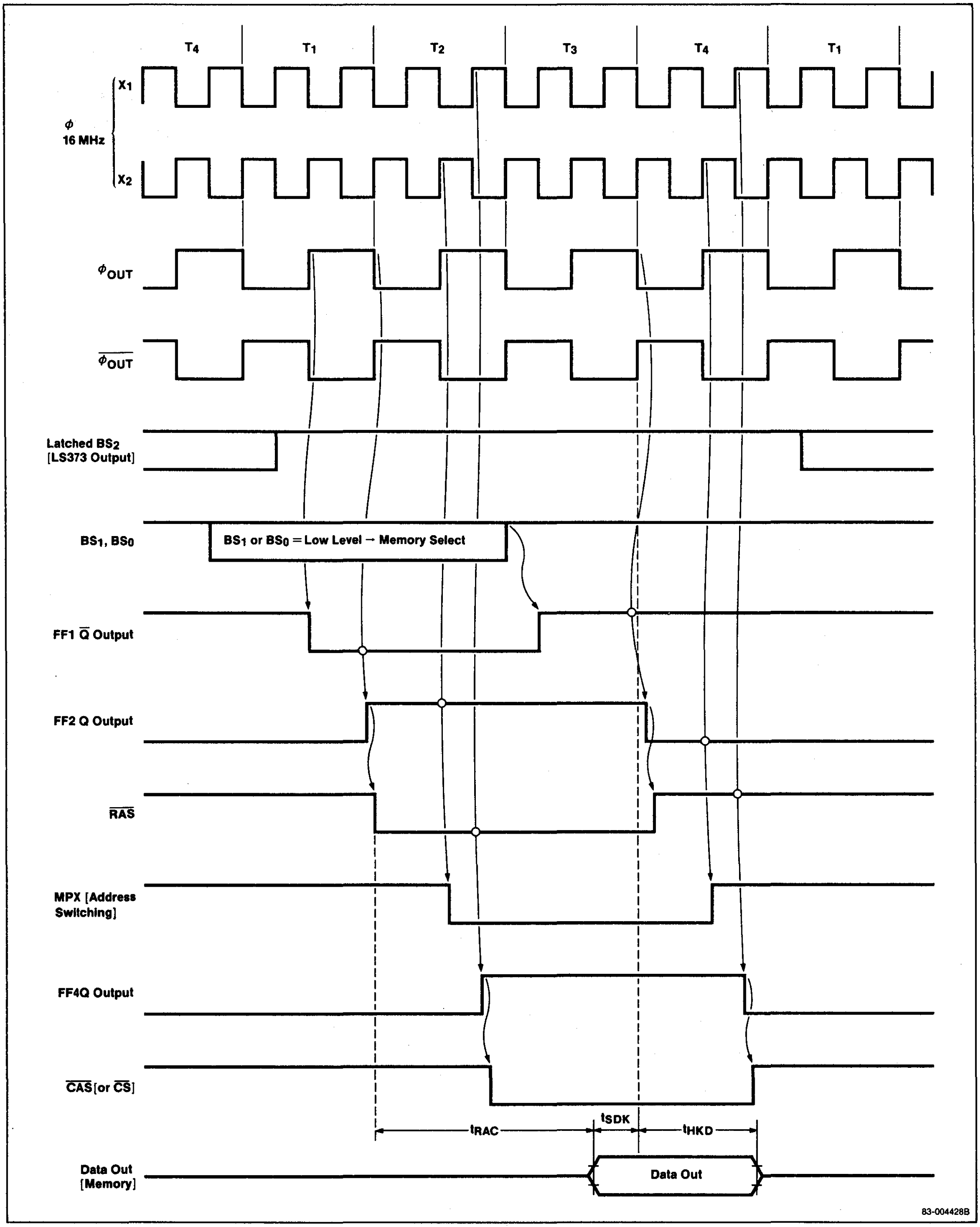


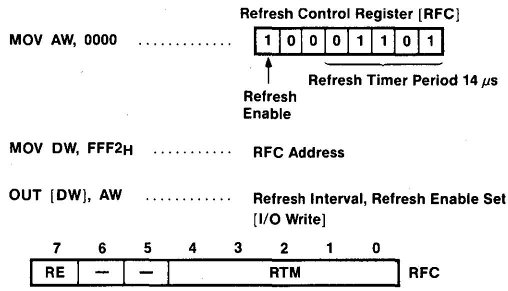
Figure 26. $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) Timing Sequence



Refresh Timing Generation

Refreshing for the μPD421000, μPD421001, and μPD421002 is executed by selecting 512 lines in 8 ms. In the V40, memory refreshing can be handled easily by outputting the $\overline{\text{REFRQ}}$ control signal and the A_0 through A_8 refresh addresses. These signals are controlled by programming the refresh control register (RFC), allocated to I/O address FFF2H (figure 27).

Figure 27. Programming of Refresh Control Register



RE [Refresh Enable]

RE	Function
0	Disable
1	Enable

RTM [Refresh Timer]

RTM	N[Timer Factor]
00000	17
00001	18
00010	19
00011	20
00100	5
00101	6
⋮	⋮
11110	31
11111	32

Refresh Interval [μs] = 8 x N x Clock Cycle Time [μs]

83-005258A

This function generates the $\overline{REFRQ}$ control signal in accordance with the programmed interval. In this application example, $\overline{REFRQ}$ is used to disable generation of the $\overline{CAS}$ (or $\overline{CS}$) clock during refresh cycles, thereby initiating $\overline{RAS}$-only refreshing. Figures 28 and 29 show how to generate memory addresses and how to control data input and output by using control signals generated by the $\overline{RAS}$ and $\overline{CAS}$ (or $\overline{CS}$) timing generator. Figure 30 shows the timing for V40-generated refresh addresses.

The programmed values for the control register appear in figure 27 (also refer to the *μPD70208/μPD70216 User's Manual).*

Authorization for the μPD70208/μPD70216 refresh control unit to use the memory bus can be set either to top priority or lowest priority, depending on the hold status of the refresh request. Top priority is set if seven refresh requests are being held, and refreshing is executed consecutively until the number of requests is reduced to three.

Although a wait interval of maximum duration (three clocks) is inserted by the built-in wait control unit, if a reset input is applied after power is applied, no wait interval need be inserted in actual applications. Therefore, the wait control register has to be reset when the V40 is used at 8 MHz.

Wait control registers WCY2 (FFF6H), WCY1 (FFF5H), and WMB (FFF4H) write program data at these I/O addresses using an I/O write instruction (figure 31).

Figure 28. Memory Access Generation

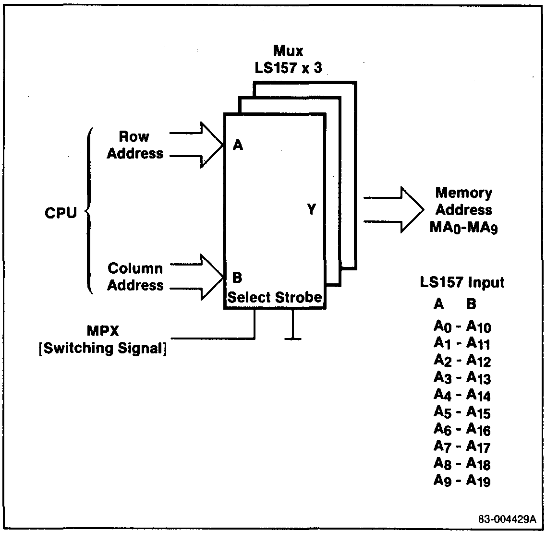


Figure 29. Data Input and Output Control

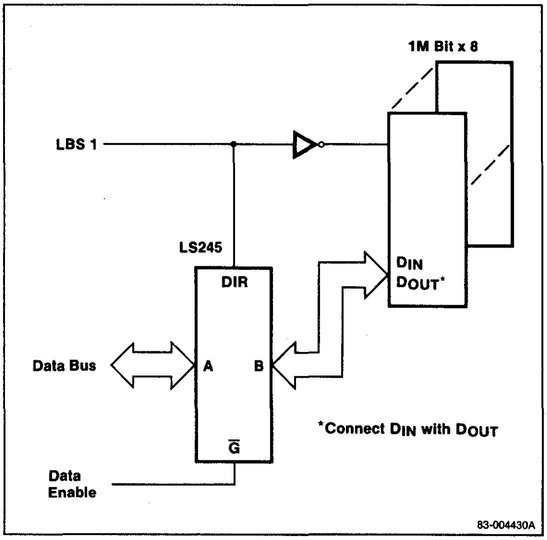
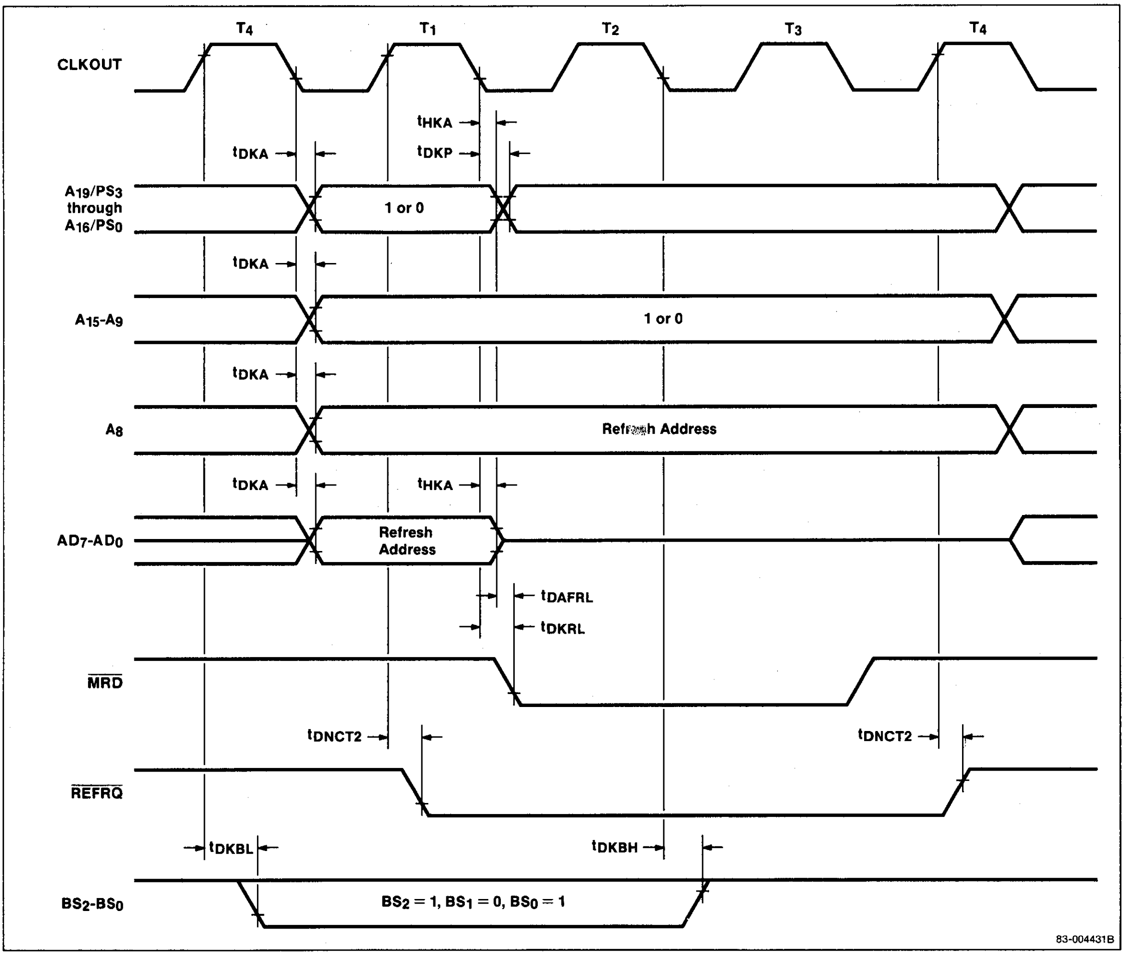


Figure 30. Refresh Timing Cycle



5

Dummy Cycles

As explained previously, dummy cycles are required to charge certain internal voltage potentials to proper operating levels in the DRAM's internal circuits after power has been applied.

In the following application example, these dummy cycles are implemented by executing eight write (or read) cycles, from 0000H to 00007H, in the memory .

```
        MOV   AL,0000H
LOOP:   MOV   (BL),0000H
        INC   AL
        CMP   AL,00007H
        JNZ   LOOP
```

Composite Schematic

Figure 32 shows the complete schematic. The V40 and 1M CMOS DRAMs are included, as well as circuits to control timing and refreshing.

Figure 31. Register Programming

WCY1 [Wait Cycle Register 1] .... I/O Address $FFF5_H$

7	6	5	4	3	2	1	0	
IOW		UMW		MMW		LMW		WCY1

WCY2 [Wait Cycle Register 2] .... I/O Address $FFF6_H$

7	6	5	4	3	2	1	0	
—	—	—	—	DMAW		RFW		WCY2

IOW [I/O Wait]
UMW [Upper Memory Block Wait]
MMW [Middle Memory Block Wait]
LMW [Lower Memory Block Wait]

IOW/UMW/MMW/LMW	Number of Wait States
00	0 [No Wait]
01	1
10	2
11	3

DMAW [DMA Wait]
RFW [Refresh Wait]

DMAW/RFW	Number of Wait States
00	0
01	1
10	2
11	3

WMB [Wait Memory Boundary Register] .... I/O Address $FFF4_H$

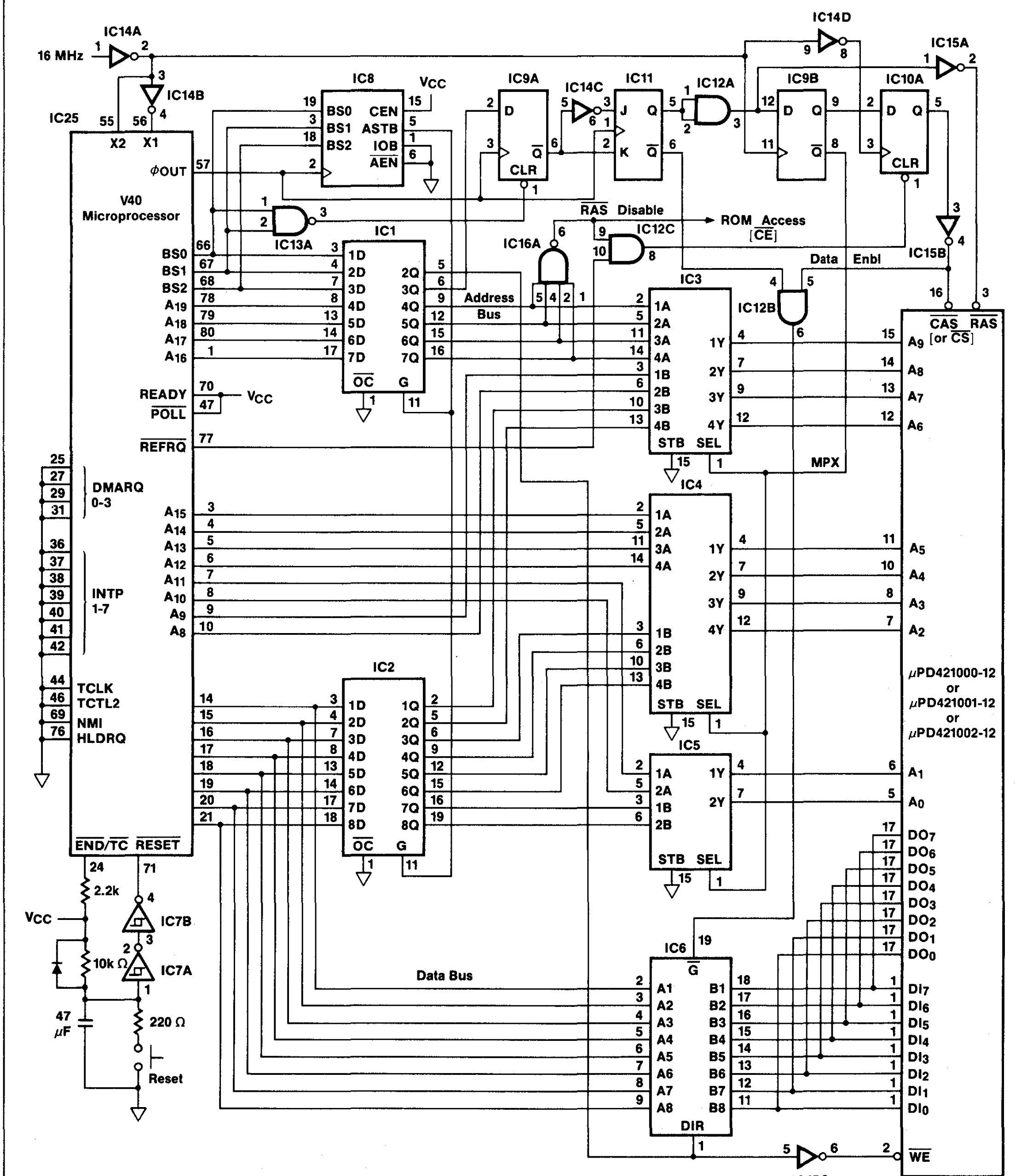
7	6	5	4	3	2	1	0	
	LMB				UMB			WMB

LMB [Lower Memory Block]
UMB [Upper Memory Block]

LMB/UMB	Memory Block Size
000	32KB
001	64KB
010	96KB
011	128KB
100	192KB
101	256KB
110	384KB
111	512KB

83-005259B

Figure 32. Composite Schematic



IC1, IC2	LS373	IC9, IC10	LS74	IC16	LS20
IC3-IC5	LS157	IC11	LS112	ICC17-IC24	μPD421000-12, μPD421001-12, or μPD421002-12
IC6	LS245	IC12	LS08		
IC7	LS14	IC13	LS00	IC25	V40, μPD70208
IC8	μPD71088	IC14, IC15	LS04		

83-004432C

5

NEC

STATIC RAMs

6

Section 6
Static RAMs

NEC
NEC Electronics Inc.

μPD4311
16,384 x 1-BIT STATIC CMOS RAM

Description

The μPD4311 is a 16,384-word by 1-bit static random access memory fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4311 a high-speed device that requires very low power and no clock or refreshing to operate.

The μPD4311 is packaged in a 20-pin plastic DIP.

Features

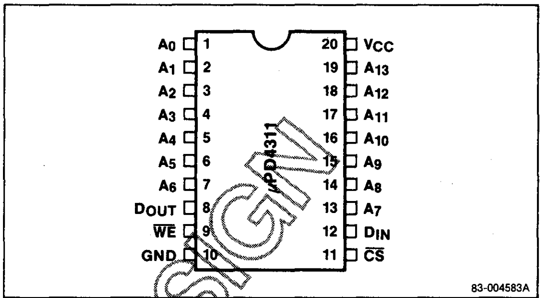
- ☐ Single +5-volt supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Separated data input and output
- ☐ Three-state output
- ☐ Low power dissipation
  - — 80 mA max (active)
  - — 2 mA max (standby)
- ☐ Standard 300-mil, 20-pin plastic DIP

Ordering Information

Part Number	Access Time (max)	Package
μPD4311C-35	35 ns	20-pin plastic DIP
C-45	45 ns	
C-55	55 ns	

Pin Configuration

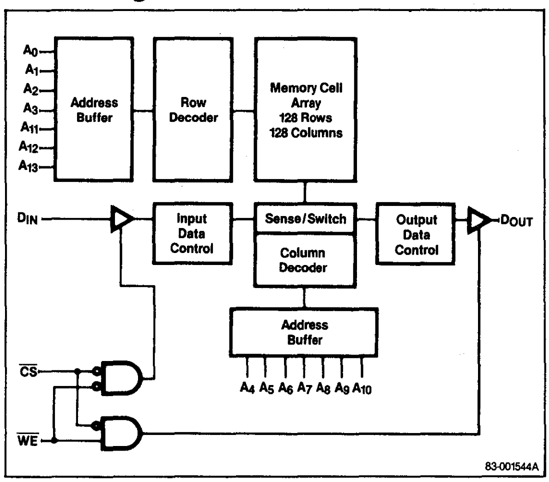
20-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{13}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



6

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +7.0 V
Output voltage, V_{OUT}	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Notes:

(1) V_{IN} = −3.0 V min for 20 ns maximum pulse.

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1)

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Data output capacitance	C_{DOUT}			6	pF	V_{DOUT} = 0 V

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not selected	Hi-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	Hi-Z	Active

Recommended DC Operating Conditions

T_A = 0 to +70°C

		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		6.0	V

Notes:

(1) V_{IL} = −3.0 V min for 20 ns maximum pulse.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}; V_{CC} = max
Operating supply current	I_{CC}			80	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			15	mA	$\overline{CS}$ = V_{IH}
Standby supply current	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} − 0.2 V; $V_{IN} \leq$ 0.2 V or $\geq V_{CC}$ − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		μPD4311-35		μPD4311-45		μPD4311-55			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Cycle									
Read cycle time	t_{RC}	35		45		55		ns	(Note 2)
Address access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in Lo-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselect to output in Hi-Z	t_{HZ}	0	20	0	25	0	30	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	35	0	40	0	45	ns	
Write Cycle									
Write cycle time	t_{WC}	35		45		55		ns	(Note 2)
Chip select to end of write	t_{CW}	35		40		45		ns	
Address valid to end of write	t_{AW}	35		40		45		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	25		30		35		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		25		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in Hi-Z	t_{WZ}	0	20	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V
Input pulse rise and fall times = 5 ns
Timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady state voltage with the loading shown in figure 2.

(4) The transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with the loading shown in figure 2.

Figure 1. Output Load

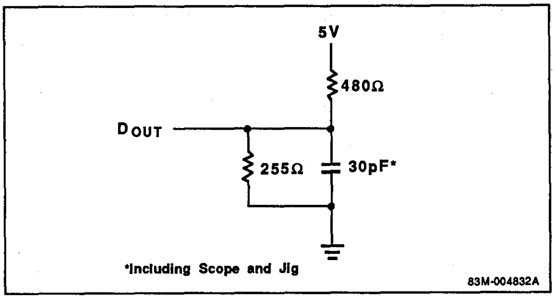
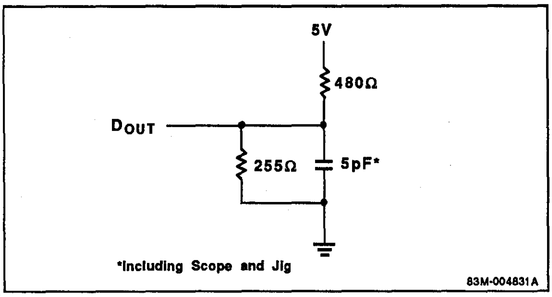


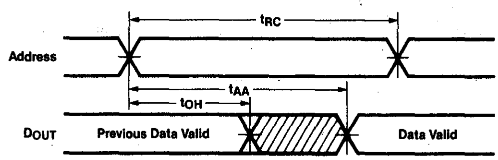
Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}



6

Timing Waveforms

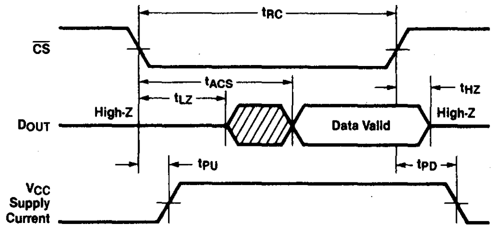
Read Cycle No. 1 (Address Access)



Notes:
[1] $\overline{WE}$ is held high for read cycle.
[2] Device is continuously selected, $\overline{CS} = V_{IL}$.

83-001636A

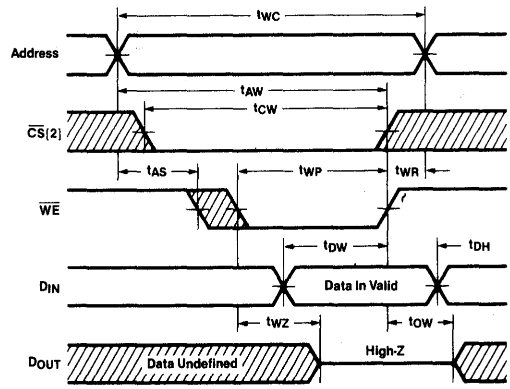
Read Cycle No.2 (Chip Select Access)



Notes: [1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

83-001548A

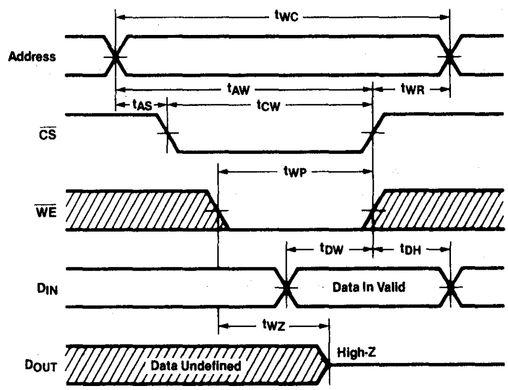
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in a high-impedance state.

83-001637A

Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-001549A

NEC
NEC Electronics Inc.

μPD4314
4,096 x 4-BIT
STATIC CMOS RAM

Description

The μPD4314 is a 4,096-word by 4-bit static random access memory fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4314 a high-speed device that requires very low power and no clock or refreshing to operate.

The μPD4314 is packaged in a standard 20-pin plastic DIP.

Features

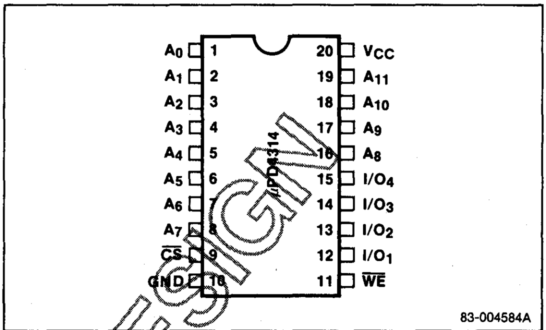
- ☐ Single +5-volt power supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Common I/O using three-state output
- ☐ Low power dissipation
  - — 80 mA max (active)
  - — 2 mA max (standby)
- ☐ Standard 300-mil, 20-pin plastic DIP

Ordering Information

Part Number	Access Time (max)	Package
μPD4314C-35	35 ns	20-pin plastic DIP
C-45	45 ns	
C-55	55 ns	

Pin Configuration

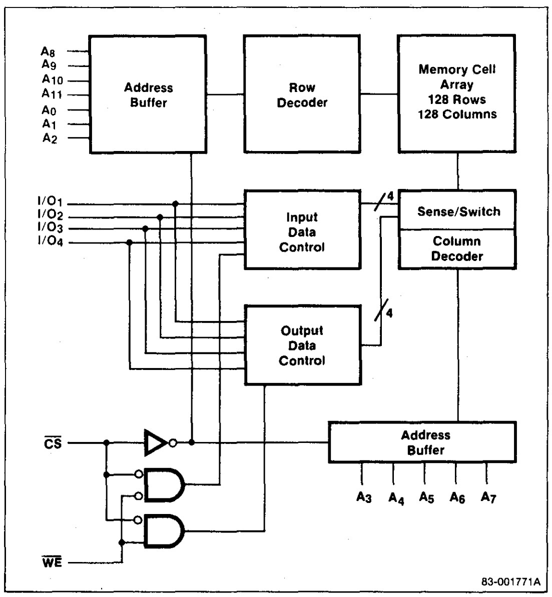
20-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{11}	Address inputs
I/O_1-I/O_4	Data input/output
$\overline{CS}$	Chip select input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



6

Absolute Maximum Ratings

Power supply voltage, V_{CC}	–0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	–0.5 to +7.0 V
Output voltage, V_{OUT}	–0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	–55 to 125°C
Power dissipation, P_D	1.0 W

Notes:

(1) V_{IN} = –3.0 V min for 20 ns maximum pulse.

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1)

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Data output capacitance	C_{DOUT}			7	pF	V_{DOUT} = 0 V

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not selected	Hi-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	Hi-Z	Active

Recommended DC Operating Conditions

T_A = 0 to +70°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	–0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V

Notes:

(1) V_{IL} = –3.0 V min for 20 ns maximum pulse.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input leakage current	I_{LI}	–2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	–2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}; V_{CC} = max
Operating supply current	I_{CC}			80	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			15	mA	$\overline{CS}$ = V_{IH}
Standby supply current	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} – 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} – 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –4.0 mA

AC Characteristics

$T_A = 0$ to $70°C$; $V_{CC} = 5.0\ V \pm 10\%$

		Limits							
		μPD4314-35		μPD4314-45		μPD4314-55			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Cycle									
Read cycle time	t_{RC}	35		45		55		ns	(Note 2)
Address access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in Lo-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselect to output in Hi-Z	t_{HZ}	0	20	0	25	0	30	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	35	0	45	0	55	ns	
Write Cycle									
Write cycle time	t_{WC}	35		45		55		ns	(Note 2)
Chip select to end of write	t_{CW}	35		40		45		ns	
Address valid to end of write	t_{AW}	35		40		45		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	30		40		50		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in Hi-Z	t_{WZ}	0	20	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V
Input pulse rise and fall times = 5 ns
Timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady state voltage with the loading shown in figure 2.

(4) The transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with the loading shown in figure 2.

Figure 1. Output Load

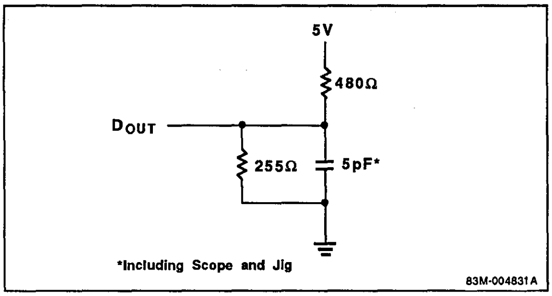
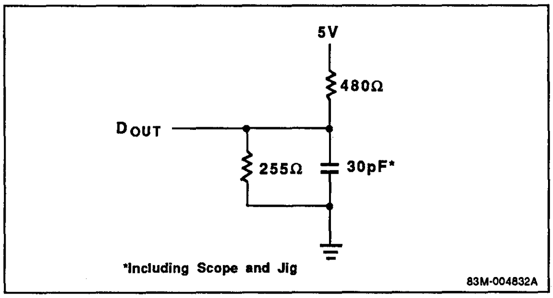


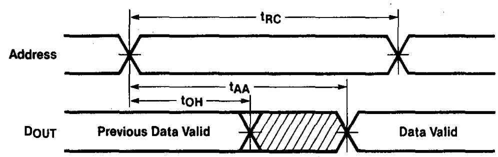
Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}



6

Timing Waveforms

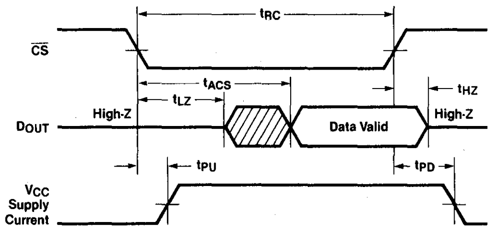
Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is held high for read cycle.
[2] Device is continuously selected, $\overline{CS} = V_{IL}$.

83-001636A

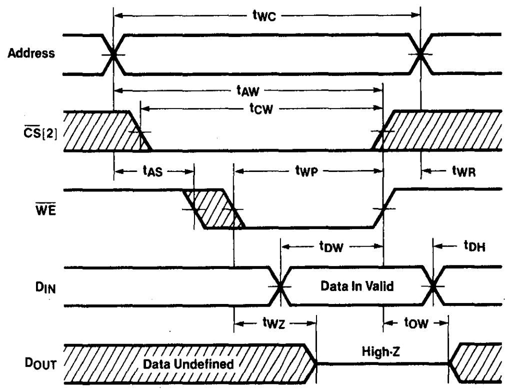
Read Cycle No. 2 (Chip Select Access)



Notes:
[1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

83-001548A

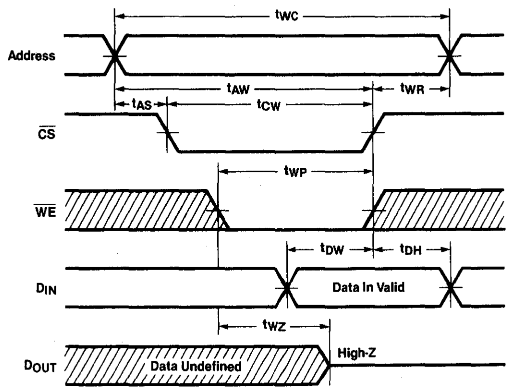
Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in a high-impedance state.

83-001637A

Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: [1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-001549A

NEC
NEC Electronics Inc.

μPD4361
65,536 x 1-BIT
STATIC CMOS RAM

Description

The μPD4361 is a 65,536-word by 1-bit static random access memory fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4361 a high-speed device that requires very low power and no clock or refreshing to operate.

The μPD4361 is packaged in a 300-mil-wide, 22-pin plastic DIP and a 290-mil x 490-mil, 22-pin ceramic leadless chip carrier. The μPD4361 has two types of access times, address and chip select. In addition, the μPD4361C-L features low-power data retention.

Features

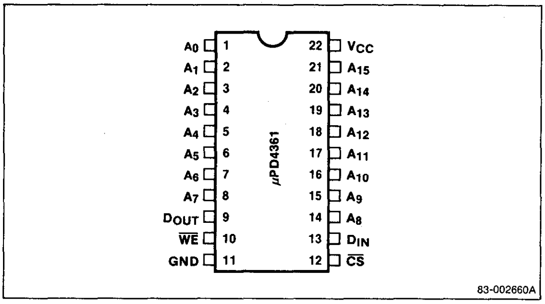
- ☐ 65,536 x 1-bit organization
- ☐ Single +5-volt power supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible — all inputs and outputs
- ☐ Separated data input and output
- ☐ Three-state output
- ☐ Data retention current of 50 μA max available
- ☐ Standard 300-mil, 22-pin plastic DIP and 290-mil x 490-mil ceramic LCC
- ☐ Standard JEDEC pin configurations

Ordering Information

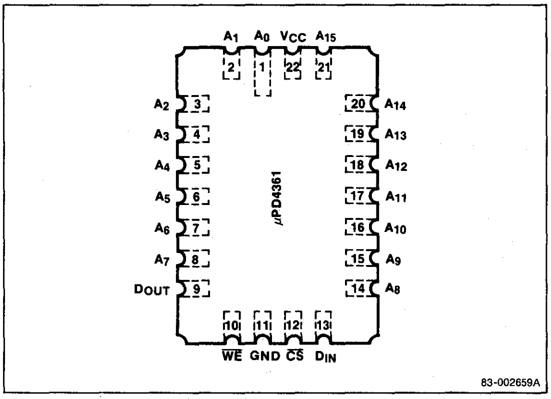
Part Number	Access Time (max)	Power Supply (max) Standby	Power Supply (max) Data Ret.	Package
μPD4361C-45	45 ns	2 mA	N/A	22-pin plastic DIP
C-55	55 ns			
C-70	70 ns			
μPD4361C-45L	45 ns	2 mA	50 μA	
C-55L	55 ns			
C-70L	70 ns			
μPD4361K-40	40 ns	2 mA	N/A	22-pin ceramic LCC
K-45	45 ns			
K-55	55 ns			

Pin Configurations

22-Pin Plastic DIP



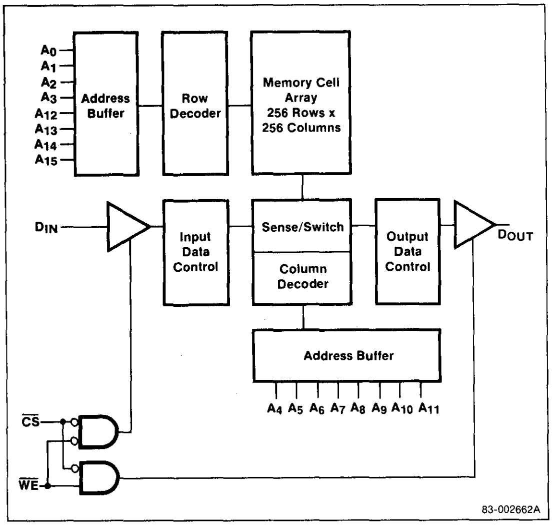
22-Pin Ceramic LCC



Pin Identification

Symbol	Function
A_0-A_{13}	Address inputs
D_{IN}	Data input
D_{OUT}	Three-state data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	–0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	–0.5 to +7.0 V
Operating temperature, T_{OPR} (Note 2)	0 to +70°C
Storage temperature, T_{STG} (Note 3)	–55 to +125°C
Power dissipation, P_D	1.0 W

Notes:

(1) V_{IN} = –3.0 V min for 20 ns maximum pulse.

(2) T_{OPR} for 4361K = –10 to +85°C

(3) T_{STG} for 4361K = –65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC characteristics.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	V_{IN} = 0 V
Data output capacitance	C_{DOUT}			7	pF	V_{DOUT} = 0 V

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended DC Operating Conditions

T_A = 0 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	–0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V

Notes:

(1) V_{IL} = –3.0 V min for 20 ns maximum pulse.

DC Characteristics

T_A = 0 to 70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	–2		2	μA	V_{OUT} = 0 V to V_{CC}, $\overline{CS}$ = V_{IH}; V_{CC} = max
Operating supply current	I_{CC}			120	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} – 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} – 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –4.0 mA

AC Characteristics

T_A = 0 to 70°C; V_{CC} = 5.0 V ±10%

		Limits									
		μPD4361-40 (Note 2)		μPD4361-45		μPD4361-55		μPD4361-70 (Note 3)			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Cycle											
Read cycle time	t_{RC}	40		45		55		70		ns	(Note 4)
Address access time	t_{AA}		40		45		55		70	ns	
Chip select access time	t_{ACS}		40		45		55		70	ns	
Output hold from address change	t_{OH}	5		5		5		5		ns	
Chip select to output in Low-Z	t_{LZ}	5		5		5		5		ns	(Note 5)
Chip deselect to output in High-Z	t_{HZ}	0	22	0	25	0	30	0	30	ns	(Note 6)
Chip select to power-up time	t_{PU}	0		0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	27	0	30	0	40	0	40	ns	
Write Cycle											
Write cycle time	t_{WC}	40		45		55		70		ns	(Note 4)
Chip select to end of write	t_{CW}	37		40		50		60		ns	
Address valid to end of write	t_{AW}	37		40		50		60		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	23		25		30		40		ns	
Write recovery time	t_{WR}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	23		25		25		30		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write enable to output in High-Z	t_{WZ}	0	22	0	25	0	25	0	30	ns	(Note 6)
Output active from end of write	t_{OW}	0		0		0		0		ns	(Note 5)

Notes:

(1) Input pulse levels = GND to 3.0 V
Input pulse rise and fall times = 5 ns
Timing reference levels = 1.5 V;
see figures 1 and 2 for the output load.

(2) Available for μPD4361K only.

(3) Available for μPD4361C or μPD4361C-L only.

(4) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(5) The transition is measured ±200 mV from steady state voltage with the loading shown in figure 2.

(6) The transition is measured at V_{OL} +200 mV and V_{OH} −200 mV with the loading shown in figure 2.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	High-Z	Active

6

Figure 1. Output Load

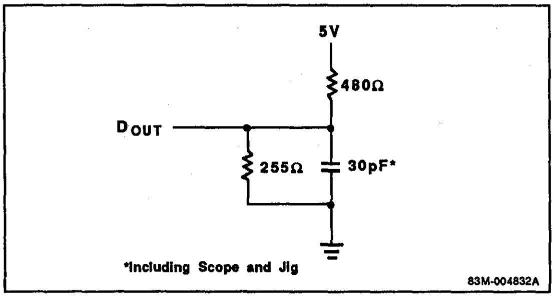
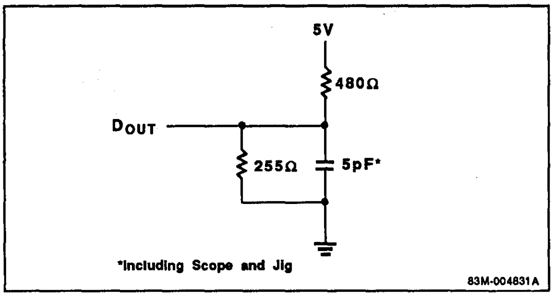


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}



Low V_{CC} Data Retention Characteristics

$T_A = 0$ to 70°C (Note 1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	(Note 2)
Data retention supply current	I_{CCDR}		1	50	μA	(Note 3)
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

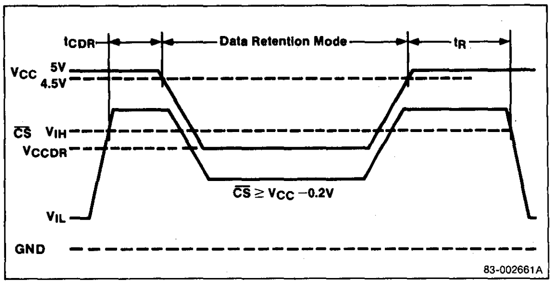
Notes:

(1) For μPD4361C-L only

(2) $\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \geq V_{CC} - 0.2$ V or 0 V $\leq V_{IN} \leq 0.2$ V

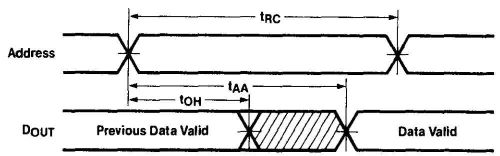
(3) $V_{CC} = 3.0$ V; $\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \geq V_{CC} - 0.2$ V or 0 V $\leq V_{IN}$ ≤ 0.2 V

Data Retention



Timing Waveforms

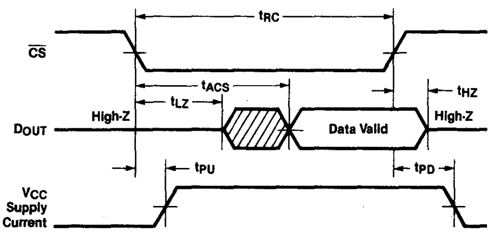
Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{\text{WE}}$ is held high for read cycle.
[2] Device is continuously selected, $\overline{\text{CS}} = V_{IL}$.

83-001636A

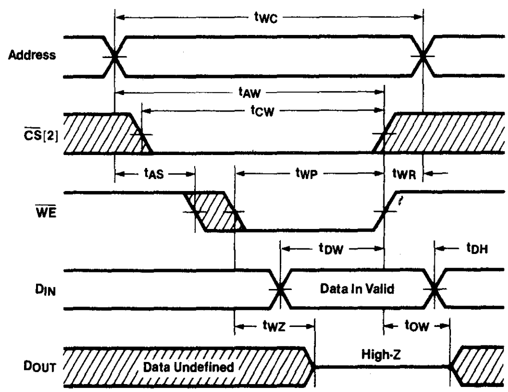
Read Cycle No. 2 (Chip Select Access)



Note: [1] $\overline{\text{WE}}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{\text{CS}}$ transition low.

83-001548A

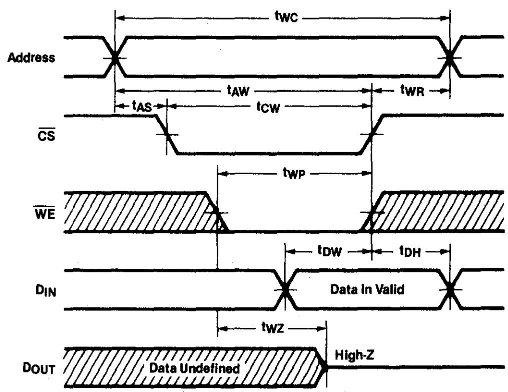
Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)



Note:
[1] $\overline{\text{CS}}$ or $\overline{\text{WE}}$ must be high during address transition.
[2] If $\overline{\text{CS}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the outputs remain in a high-impedance state.

83-001637A

Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled)



Note: [1] $\overline{\text{CS}}$ or $\overline{\text{WE}}$ must be high during address transition.

83-001549A

6

NEC

NEC Electronics Inc.

µPD4362
16,384 x 4-BIT
STATIC CMOS RAM

Description

The µPD4362 is a 16,384-word by 4-bit static RAM fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the µPD4362 a high-speed device that requires very low power and no clock or refreshing to operate.

The µPD4362 is packaged in a standard 22-pin plastic DIP.

Features

- ☐ Single +5-volt power supply
- ☐ Fully static operation—no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Common I/O capability
- ☐ Standard 300-mil, 22-pin plastic DIP

Ordering Information

Part Number	Access Time (max)	Package
µPD4362C-45	45 ns	22-pin plastic DIP
C-55	55 ns	
C-70	70 ns	

Absolute Maximum Ratings

Supply voltage, V_{CC}	–0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	–0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Power dissipation, P_D	1.0 W

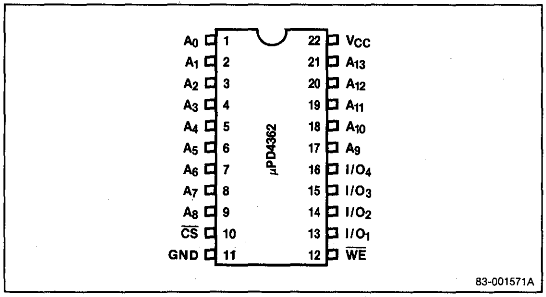
Notes:

(1) $V_{IN} = -3.0$ V for 20 ns pulse.

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configuration

22-Pin Plastic DIP

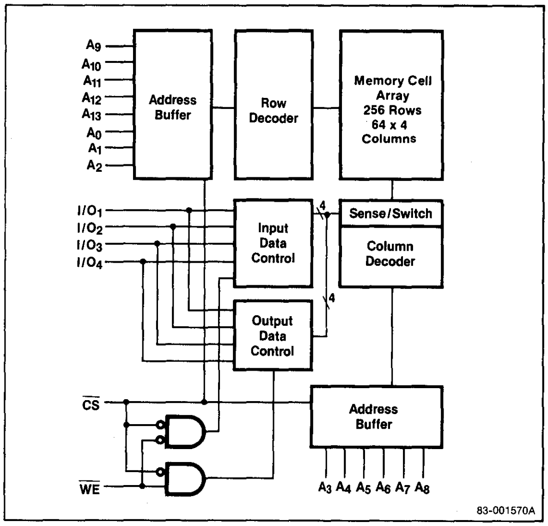


Pin Identification

Symbol	Function
A_0-A_{13}	Address inputs
I/O_1-I/O_4	Data inputs/outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

6

Block Diagram



Recommended DC Operating Conditions

$T_A = 0$ to $70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		$V_{CC} + 0.3$	V

Notes:

(1) $V_{IL} = -3.0$ V for 20 ns pulse

Capacitance

$T_A = 25°C$; f = 1 MHz (Note 1)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	$V_{IN} = 0$ V
I/O capacitance	C_{DOUT}			7	pF	$V_{DOUT} = 0$ V

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	D_{IN}	Active

Notes:

(1) X = don't care

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	$V_{IN} = 0$ to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2		2	μA	$V_{OUT} = 0$ to V_{CC}; $\overline{CS} = V_{IH}$; V_{CC} = max
Operating supply current	I_{CC}			90	mA	$\overline{CS} = V_{IL}$; $I_{DOUT} = 0$ mA
Standby supply current	I_{SB}			20	mA	$\overline{CS} = V_{IH}$
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 8.0$ mA
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -4.0$ mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		Limits							
		μPD4362-45		μPD4362-55		μPD4362-70			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Cycle									
Read cycle time	t_{RC}	45		55		70		ns	(Note 2)
Address access time	t_{AA}		45		55		70	ns	
Chip selection access time	t_{ACS}		45		55		70	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip selection to output in low-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselection to output in high-Z	t_{HZ}	0	25	0	25	0	30	ns	(Note 4)
Chip selection to power-up time	t_{PU}	0		0		0		ns	
Chip deselection to power-down time	t_{PD}	0	45	0	55	0	55	ns	
Write Cycle									
Write cycle time	t_{WC}	45		55		70		ns	(Note 2)
Chip selection to end of write	t_{CW}	40		50		60		ns	
Address valid to end of write	t_{AW}	40		50		60		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	40		50		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	20	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} +200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

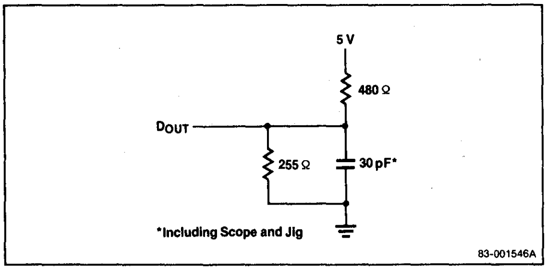
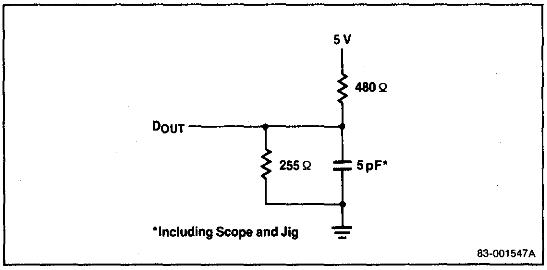
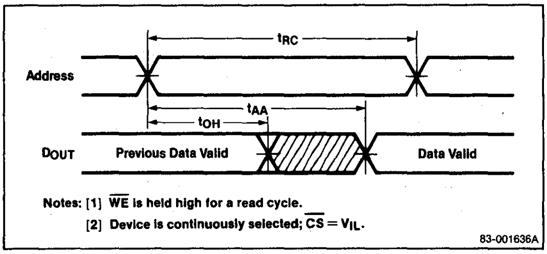


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}

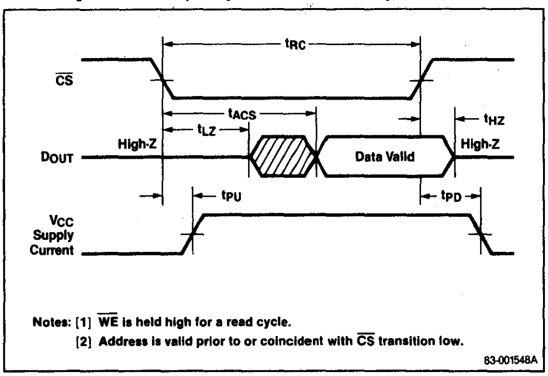


Timing Waveforms

Read Cycle No. 1 (Address Access)

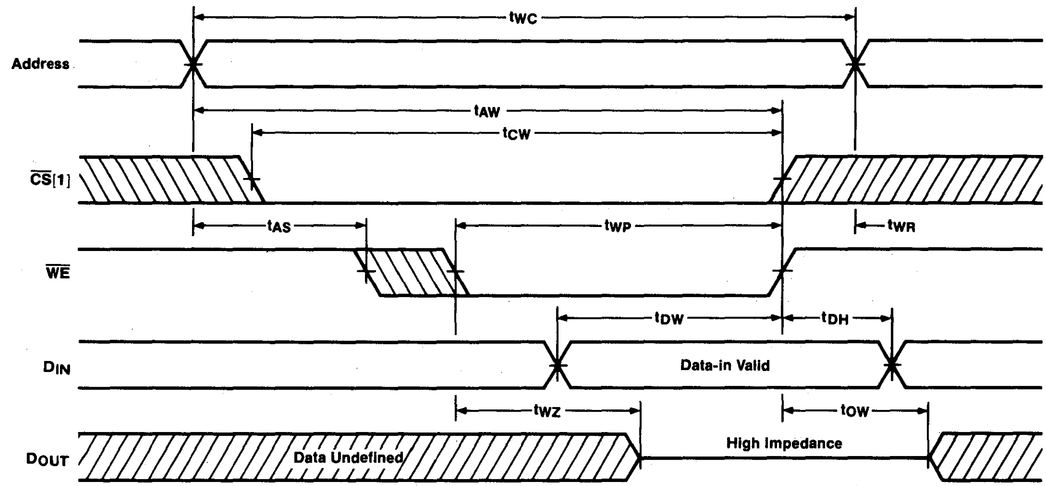


Read Cycle No. 2 (Chip Select Access)



Timing Waveforms (cont)

Write Cycle No. 1 ($\overline{WE}$-Controlled)



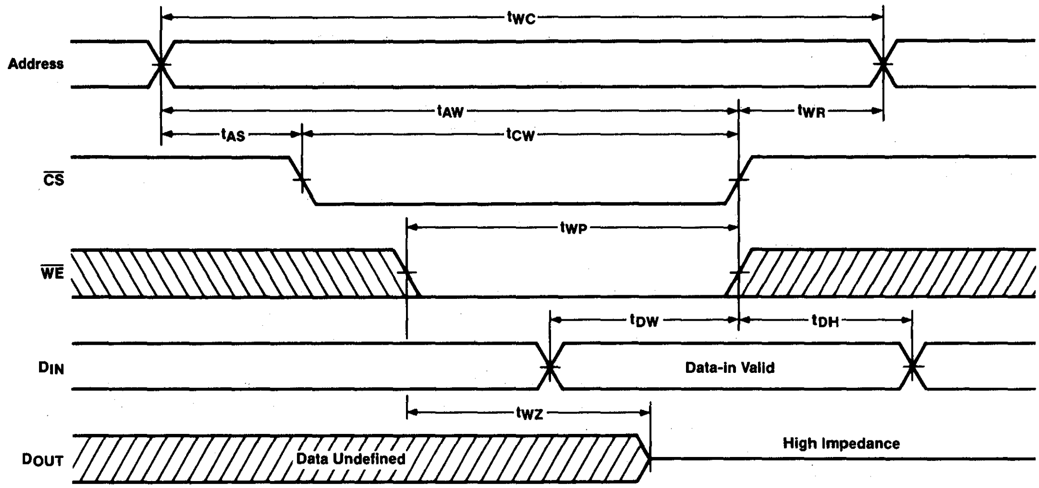
Notes:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-005098B

6

Timing Waveforms (cont)

Write Cycle No. 2 ($\overline{CS}$-Controlled)



Notes:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-005099B

NEC
NEC Electronics Inc.

μPD4363 16,384 x 4-BIT STATIC CMOS RAM

Description

The μPD4363 is a 16,384-word by 4-bit static RAM fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4363 a high-speed device that requires very low power and no clock or refreshing to operate.

The μPD4363 is packaged in a standard 300-mil, 24-pin plastic DIP.

Features

- ☐ Single +5-volt supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Common I/O capability
- ☐ $\overline{OE}$ eliminates the need for external bus buffers
- ☐ Three-state outputs
- ☐ Low power dissipation
  - — 90 mA max (active)
  - — 2 mA max (standby)
- ☐ Standard 300-mil, 24-pin plastic DIP packaging

Ordering Information

Device	Access Time (max)	Package
μPD4363C-45	45 ns	24-pin plastic DIP
C-55	55 ns	
C-70	70 ns	

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to 7.0 V
All input and ouput voltages, V_{IN} (Note 1)	−0.5 to 7.0 V
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C
Power dissipation, P_D	1.0 W

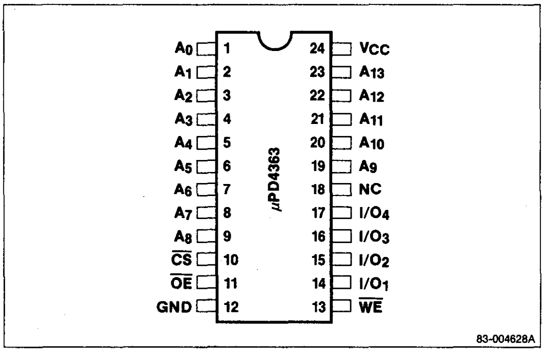
Notes:

(1) Minimum V_{IN} = −3.0 V for 20-ns pulse

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configuration

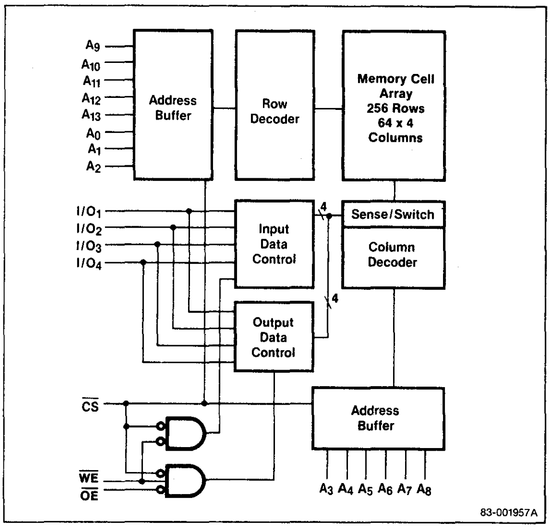
24-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{13}	Address input
I/O_1-I/O_4	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



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Recommended DC Operating Conditions

$T_A = 0$ to $+70°C$

		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		$V_{CC} + 0.3$	V

Notes:

(1) $V_{IL} = -3.0$ V for 20-ns pulse.

Capacitance

$T_A = 25°C$; $f = 1$ MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	$V_{IN} = 0$ V
I/O capacitance	C_{DOUT}			7	pF	$V_{DOUT} = 0$ V

Notes:

(1) These parameters are sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	L	Read	D_{OUT}	Active
L	H	H	D_{OUT} disabled	High-Z	Active
L	L	X	Write	D_{IN}	Active

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ± 10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	$V_{IN} = 0$ to V_{CC}; $V_{CC} = \max$
Output leakage current	I_{LO}	−2		2	μA	$V_{OUT} = 0$ to V_{CC}; $\overline{CS}$ or $\overline{OE} = V_{IH}$; $V_{CC} = \max$
Operating supply current	I_{CC}			90	mA	$\overline{CS} = V_{IL}$; $I_{DOUT} = 0$ mA
Standby supply current	I_{SB}			20	mA	$\overline{CS} = V_{IH}$
	I_{SB1}			2	mA	$\overline{CS} = V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 8.0$ mA
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -4.0$ mA

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5\ V \pm 10\%$

		Limits							
		μPD4363-45		μPD4363-55		μPD4363-70			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Cycle									
Read cycle time	t_{RC}	45		55		70		ns	(Note 2)
Address access time	t_{AA}		45		55		70	ns	
Chip select access time	t_{ACS}		45		55		70	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip selection to output in low-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselection to output in high-Z	t_{HZ}	0	20	0	25	0	30	ns	(Note 4)
Output enable access time	t_{OE}		20		25		30	ns	
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	(Note 3)
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	0	35	ns	(Note 4)
Chip selection to power-up time	t_{PU}	0		0		0		ns	
Chip deselection to power-down time	t_{PD}	0	30	0	40	0	40	ns	
Write Cycle									
Write cycle time	t_{WC}	45		55		70		ns	(Note 2)
Chip selection to end of write	t_{CW}	40		50		60		ns	
Address valid to end of write	t_{AW}	40		50		60		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	40		50		60		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enabled to output in high-Z	t_{WZ}	0	20	0	25	0	30	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) The read and write cycle times are referenced from the last valid address to the first transitioning address.

(3) Transition is measured ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

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Figure 1. Output Load

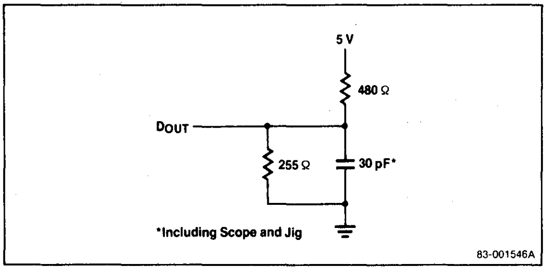
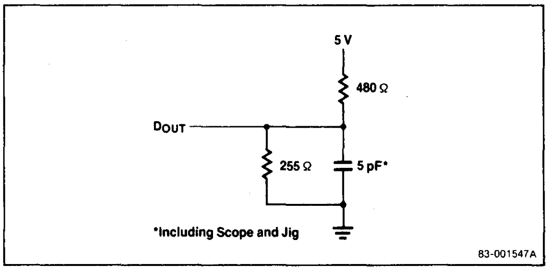
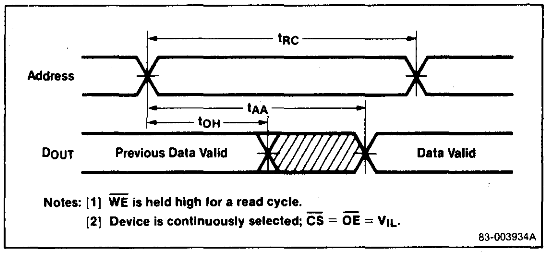


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{OLZ}, t_{OHZ}, t_{WZ}, and t_{OW}

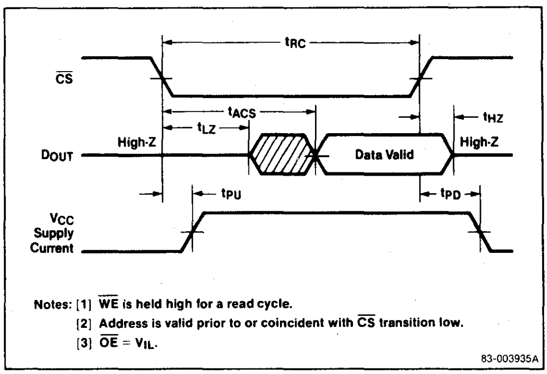


Timing Waveforms

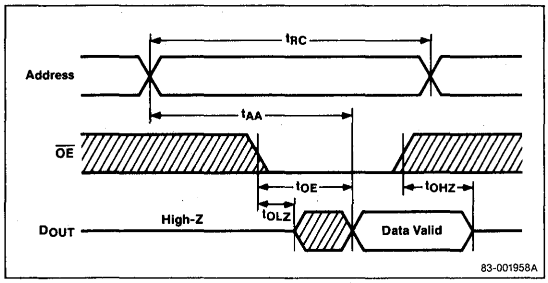
Read Cycle No. 1 (Address Access)



Read Cycle No. 2 (Chip Select Access)

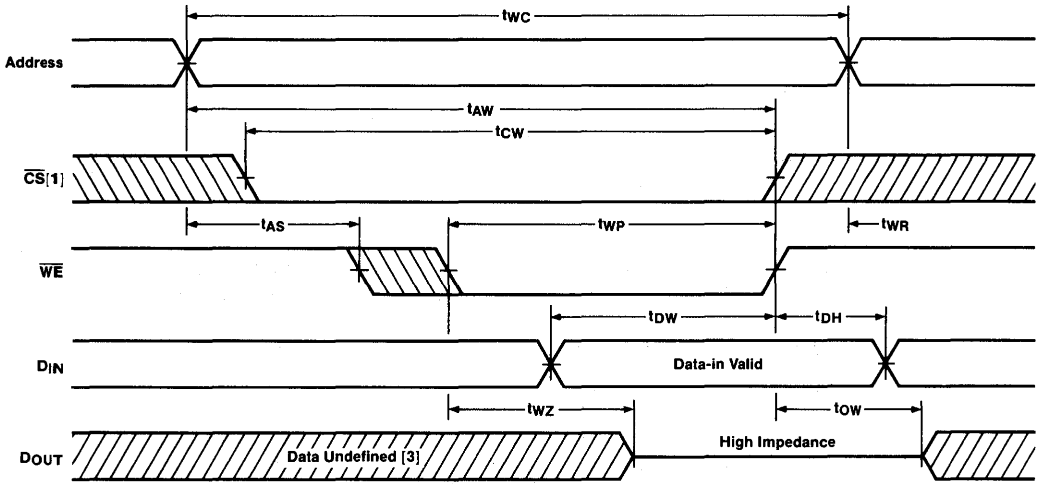


Read Cycle No. 3 ($\overline{OE}$ Access)



Timing Waveforms (cont)

Write Cycle No. 1 ($\overline{WE}$-Controlled)



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[3] During this period, the I/O may be active [OE low]. Therefore, data input signals of opposite polarity to the outputs must not be applied.

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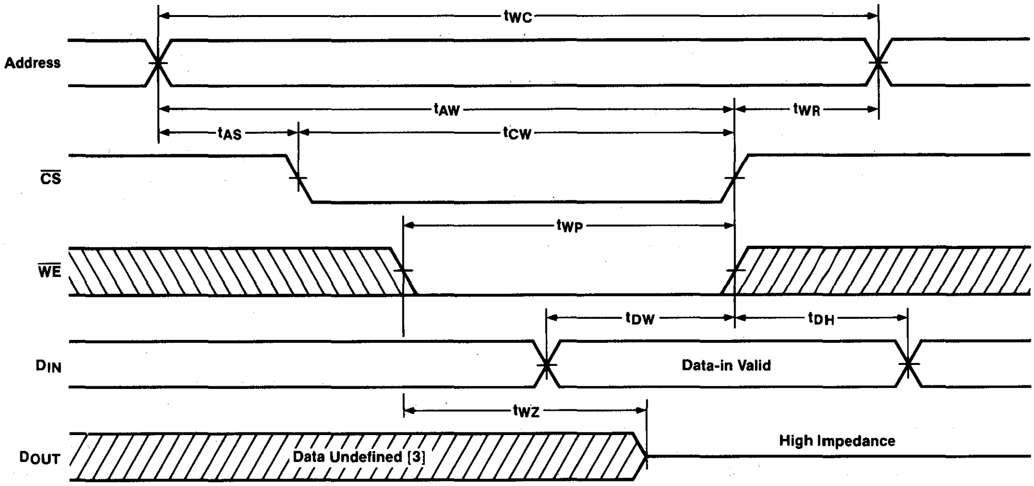
Timing Waveforms (cont)

Write Cycle No. 2 ($\overline{CS}$-Controlled)



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[3] During this period, the I/O may be active [OE low]. Therefore, data input signals of opposite polarity to the outputs must not be applied.

83-005055B

μPD4364 8192 x 8-BIT STATIC CMOS RAM

Description

The μPD4364 is a high-speed, 8192-word by 8-bit static RAM. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD4364 a very low-power device that requires no clock or refreshing to operate.

Two chip enable pins are provided for battery backup application, and an output enable pin is provided for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 V (-xxL and -xxLL versions).

The μPD4364 is packaged in standard and slim 28-pin plastic DIP, as well as plastic miniflat packages that are plug-in compatible with 2764-type EPROMs.

Features

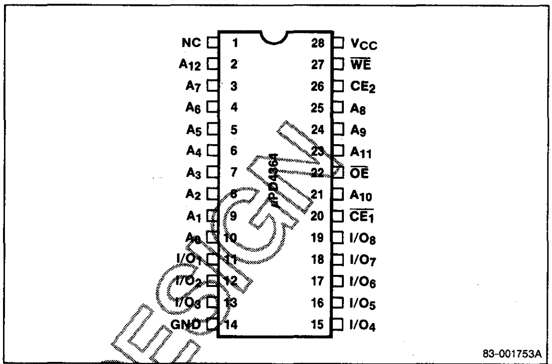
- ☐ Single +5-volt power supply
- ☐ Fully static operation—no clock or refreshing required
- ☐ TTL-compatible—all inputs and outputs
- ☐ Common I/O using three-state outputs
- ☐ One output enable and two chip enable pins for easy application
- ☐ Data retention voltage: 2 V min for -xxL and -xxLL versions
- ☐ Plug-in compatible with 2764-type EPROMs
- ☐ Standard 28-pin plastic DIP
- ☐ 28-pin 300 mil plastic slim DIP
- ☐ 28-pin plastic miniflat package

Pin Identification

Name	Function
A_0-A_{12}	Address input
I/O_1-I/O_8	Data input/output
$\overline{CE}_1$	Chip enable input, active low
CE_2	Chip enable input, active high
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

28-Pin Plastic DIP or Miniflat



Ordering Information

Part Number (Notes 1, 2, 3)	Standby Current (max)	Access Time (max)	Package
μPD4364C-xx	2 mA	(Notes 1,4)	28-pin DIP
C-xxL	100 μA		
C-xxLL	50 μA		
CX-xx	2 mA	(Notes 1,5)	28-pin slim DIP
CX-xxL	100 μA		
μPD4364G-xx	2 mA	(Notes 1,4)	28-pin miniflat
G-xxL	100 μA		
G-xxLL	50 μA		

Notes:

(1) The symbol "xx" in the part number denotes access time.

xx	Access Time (max)
10	100 ns
12	120 ns
15	150 ns
20	200 ns

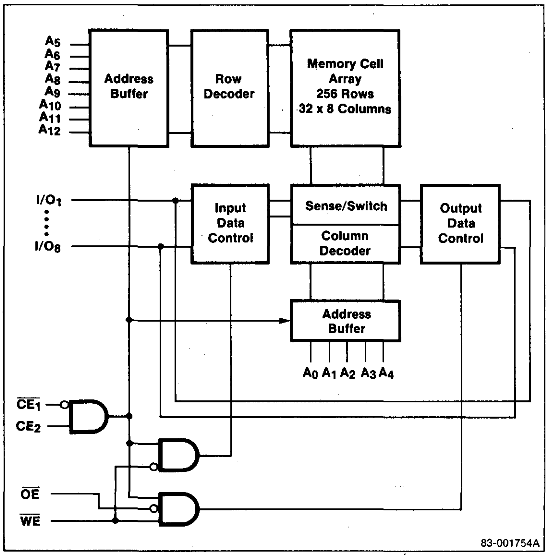
(2) The symbol C, CX, or G in the part number denotes a 28-pin plastic package.
C = 600-mil DIP
CX = 300-mil slim DIP
G = Miniflat

(3) Part number example: μPD4364CX-12L denotes a 300-mil DIP package, 120-ns maximum access time, and 100-μA maximum standby current.

(4) Contact your NEC sales representative for availability of a -10LL version.

(5) A 200-ns access time is not available in the CX package.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	–0.5 to 7.0 V
Input voltage, V_{IN} (Note 1)	–0.5 V to V_{CC} + 0.5 V
Output voltage, V_{OUT} (Note 1)	–0.5 V to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	–55 to 125°C
Power dissipation, P_D	1.0 W

Notes:

(1) –3.0 V min (pulse width of 50 ns max)

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under Recommended DC Operating Conditions.

Capacitance

T_A = 25°C; f = 1.0 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			(1)	pF	V_I = 0 V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O}$ = 0 V

Notes:

(1) Maximum input capacitance
CX package: 5 pF
C or G package, 100-ns version: 5 pF
C or G package, except 100-ns version: 6 pF

Recommended DC Operating Conditions

T_A = 0 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	–0.3 (Note 1)		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V

Notes:

(1) –3.0 V min (pulse width 50 ns max)

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}			1	μA	$V_{I/O}$ = 0 V to V_{CC} $\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}			(1)	mA	$\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, Min cycle
	I_{CCA2}		5	10	mA	$\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0$, DC current
	I_{CCA3}		3	5	mA	$\overline{CE}_1 \leq 0.2$ V, $CE_2 \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, f = 1 MHz, $I_{I/O} = 0$
Standby supply current	I_{SB}			(2)	mA	$\overline{CE}_1 \geq V_{IH}$ or $CE_2 = V_{IL}$
	I_{SB1}			(3)	mA	$\overline{CE}_1 \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
	I_{SB2}			(3)	mA	$CE_2 \leq 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –1.0 mA

Notes:

(1) μPD4364-10/10L: 45 mA max
μPD4364-12/12L/12LL: 40 mA max
μPD4364-15/15L/15LL: 40 mA max
μPD4364-20/20L/20LL: 35 mA max

(2) μPD4364-xx: 5 mA max
μPD4364-xxL: 3 mA max
μPD4364-xxLL: 3 mA max

(3) μPD4364-xx: 2 mA max
μPD4364-xxL: 100 μA max
μPD4364-xxLL: 50 μA max

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%

		Limits								
		μPD4364 -10/10L		μPD4364 -12/12L/12LL		μPD4364 -15/15L/15LL		μPD4364 -20/20L/20LL		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read Cycle										
Read cycle time	t_{RC}	100		120		150		200		ns
Address access time	t_{AA}		100		120		150		200	ns
$\overline{CE}_1$ access time	t_{CO1}		100		120		150		200	ns
CE_2 access time	t_{CO2}		100		120		150		200	ns
Output enable to output valid	t_{OE}		50		60		70		100	ns
Output hold from address change	t_{OH}	10		10		15		15		ns
Chip enable ($\overline{CE}_1$) to output in low-Z	t_{LZ1}	10		10		15		15		ns
Chip enable (CE_2) to output in low-Z	t_{LZ2}	10		10		15		15		ns
Output enable to output in low-Z	t_{OLZ}	5		5		5		5		ns
Chip enable ($\overline{CE}_1$) to output in high-Z	t_{HZ1}		35		40		50		100	ns
Chip enable (CE_2) to output in high-Z	t_{HZ2}		35		40		50		100	ns
Output enable to output in high-Z	t_{OHZ}		35		40		50		80	ns
Write Cycle										
Write cycle time	t_{WC}	100		120		150		200		ns
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	80		85		100		180		ns
Chip enable (CE_2) to end of write	t_{CW2}	80		85		100		180		ns
Address valid to end of write	t_{AW}	80		85		100		180		ns
Address setup time	t_{AS}	0		0		0		0		ns
Write pulse width	t_{WP}	60		70		90		140		ns
Write recovery time	t_{WR}	5		5		5		5		ns
Data valid to end of write	t_{DW}	40		50		60		80		ns
Data hold time	t_{DH}	0		0		0		0		ns
Write enable to output in high-Z	t_{WHZ}		35		40		50		100	ns
Output active from end of write	t_{OW}	5		5		10		10		ns

Notes:

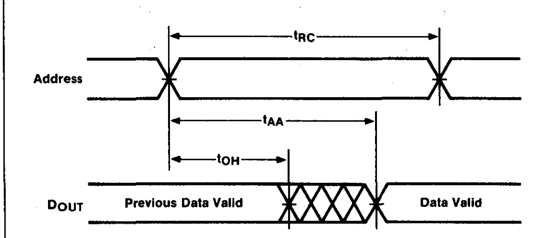
(1) Input pulse levels: 0.8 to 2.4 V
Input pulse rise and fall times: 5 ns
Timing reference levels: 1.5 V
Output load: 1 TTL gate and C_L = 100 pF

Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	D_{OUT} disable	High-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Timing Waveforms

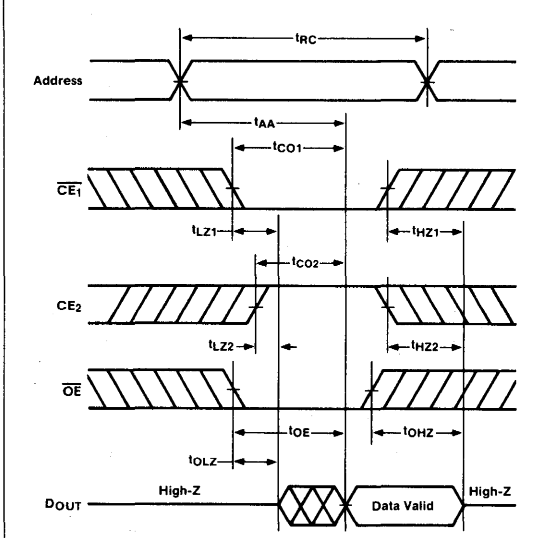
Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The device is continuously selected; $\overline{CE}_1 = \overline{OE} = V_{IL}$, $CE_2 = V_{IH}$.

83-001755A

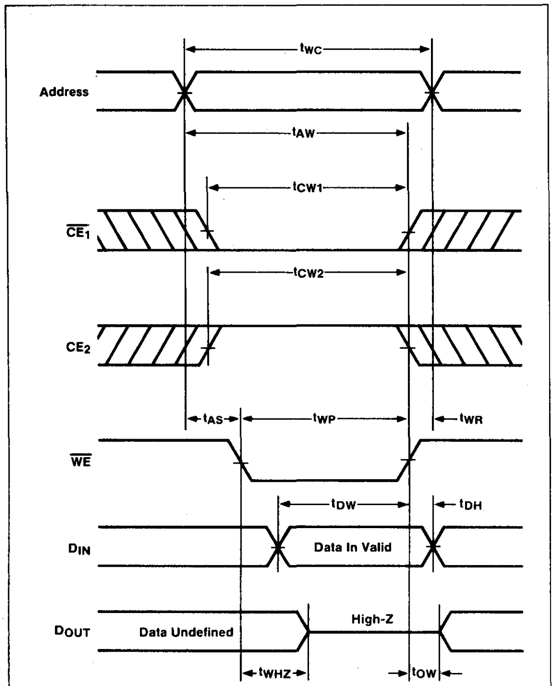
Read Cycle No. 2 (Chip Enable Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The address inputs are valid prior to or coincident with the $\overline{CE}_1$ transition low and the CE_2 transition high.

83-001756A

Write Cycle No. 1 ($\overline{WE}$ Controlled)

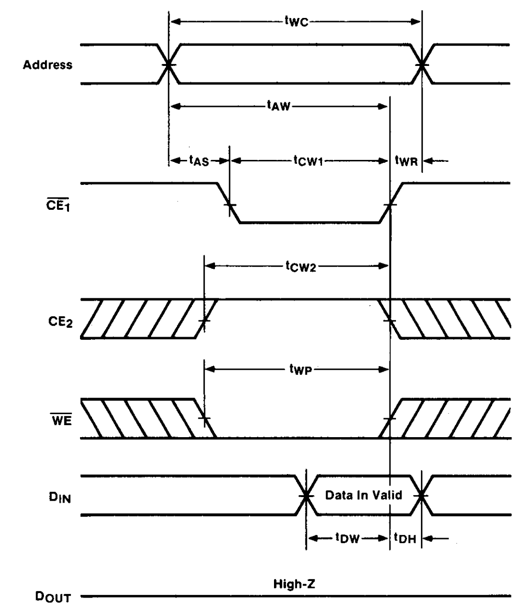


Note:
[1] A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.
[3] If $\overline{OE}$ is high the I/O pins remain in a high impedance state.

83-001757A

Timing Waveforms (cont)

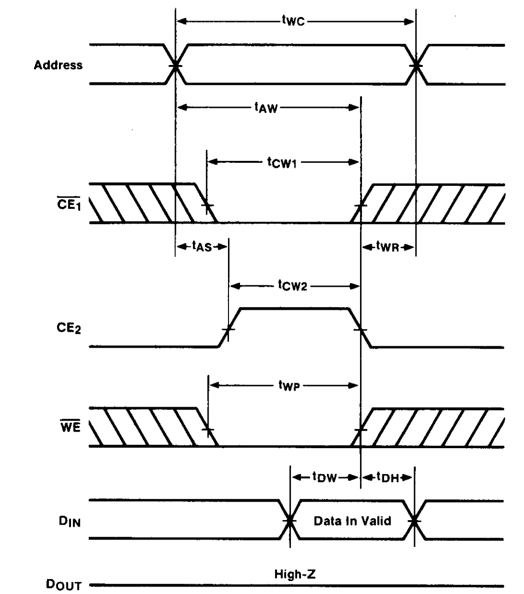
Write Cycle No. 2 ($\overline{CE_1}$ Controlled)



Note:
[1] A write occurs during the overlap of a low $\overline{CE_1}$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE_1}$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.

83-001758A

Write Cycle No. 3 (CE_2 Controlled)



Note:
[1] A write occurs during the overlap of a low $\overline{CE_1}$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE_1}$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.

83-001759A

Low V_{CC} Data Retention Characteristics

$T_A = 0$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2.0		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
	V_{CCDR2}	2.0		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		1	(2)	μA	$V_{CC} = 3.0$ V $\overline{CE}_1 \geq V_{CC} - 0.2$ V $CE_2 \geq V_{CC} - 0.2$ V
	I_{CCDR2}		1	(2)	μA	$V_{CC} = 3.0$ V $CE_2 \leq 0.2$ V
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC} Note 3			ns	

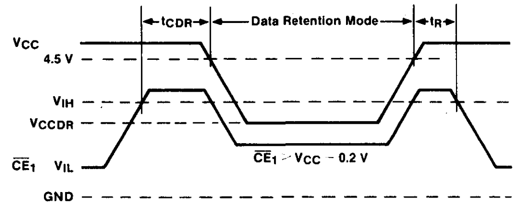
Notes:

(1) This table is applicable to μPD4364-xxL and -xxLL only.

(2) μPD4364-xxL: 50 μA max; 15 μA (0 to 40°C)
μPD4364-xxLL: 20 μA max; 5 μA (0 to 40°C)

(3) t_{RC} is read cycle time.

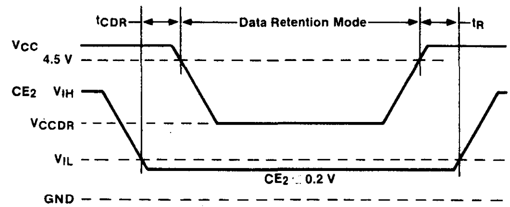
Data Retention ($\overline{CE}_1$ Controlled)



[1] CE_2 must be equal to or higher than V_{CC} −0.2 V, or less than 0.2 V. The other inputs [Addresses, $\overline{OE}$, $\overline{WE}$, I/Os] can be in a high impedance state.

83-001760A

Data Retention (CE_2 Controlled)



Note:

(1) The other inputs (Addresses, $\overline{CE}_1$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

83-001761A

NEC

NEC Electronics Inc.

µPD4464 8,192 x 8-BIT STATIC CMOS RAM

Description

The µPD4464 is a high-speed 8,192-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Full CMOS storage cells with six transistors make the µPD4464 a very low-power device that requires no clock or refreshing to operate.

Two chip enable pins are provided for battery backup application, and an output enable pin is included for easy interface. Data retention is guaranteed at a power supply voltage as low as 2 volts.

The µPD4464 is available in standard 28-pin plastic DIP or miniflat packaging.

Features

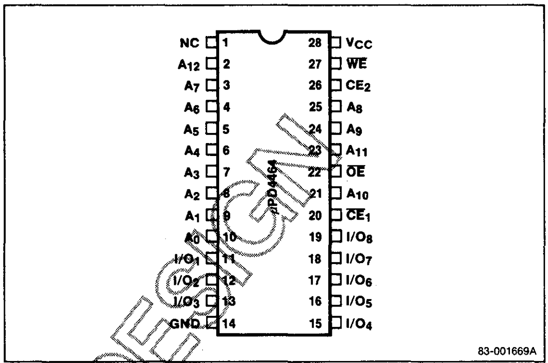
- ☐ Operating temperature range: −40 to 85 °C
- ☐ Single +5-volt power supply
- ☐ Fully static operation — no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Common I/O using three-state output
- ☐ One output enable pin and two chip enable pins for easy application
- ☐ Data retention voltage: 2 V minimum
- ☐ Standard 28-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Active Current (max)	Standby Current (max)	Package
µPD4464C-12	120 ns	40 mA	10 µA	28-pin plastic DIP
C-15	150 ns	40 mA		
C-20	200 ns	35 mA		
µPD4464C-12L	120 ns	40 mA	1 µA (at $T_A = 60$ °C)	28-pin plastic DIP
C-15L	150 ns	40 mA		
C-20L	200 ns	35 mA		
µPD4464G-12	120 ns	40 mA	10 µA	28-pin plastic miniflat
G-15	150 ns	40 mA		
G-20	200 ns	35 mA		
µPD4464G-12L	120 ns	40 mA	1 µA (at $T_A = 60$ °C)	28-pin plastic miniflat
G-15L	150 ns	40 mA		
G-20L	200 ns	35 mA		

Pin Configuration

28-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0-A_{12}	Address inputs
I/O_1-I/O_8	Data inputs/outputs
$\overline{CE}_1$	Chip enable (active low)
CE_2	Chip enable (active high)
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

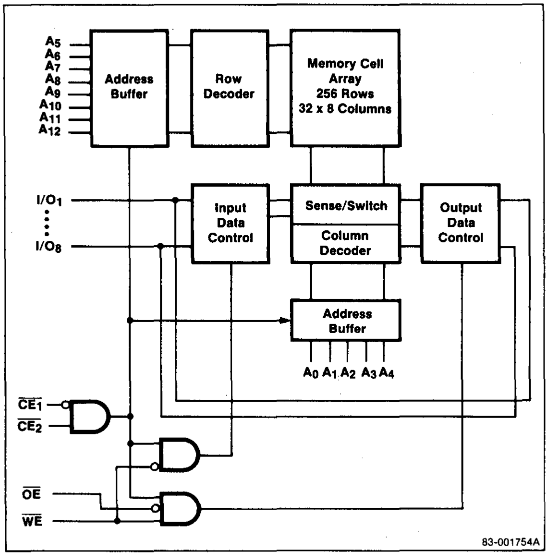
Power supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, V_{OUT} (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	−40 to 85 °C
Storage temperature, T_{STG}	−55 to 125 °C
Power dissipation, P_D	1.0 W

Notes:

(1) −3.0 V minimum (pulse width = 50 ns maximum)

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Recommended DC Operating Conditions

$T_A = -40$ to 85°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		$V_{CC} + 0.5$	V

Notes:

(1) −3.0 V minimum (pulse width = 50 ns maximum)

Capacitance

$T_A = 25$°C; f = 1.0 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}			6	pF	$V_{IN} = 0$ V
I/O capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

DC Characteristics

$T_A = -40$ to 85°C; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input leakage current	I_{LI}			1	μA	$V_{IN} = 0$ V to V_{CC}
I/O leakage current	I_{LO}			1	μA	$V_{I/O} = 0$ V to V_{CC}; $\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
Operating supply current	I_{CCA1}			40 (Note 1)	mA	$\overline{CE} = V_{IL}$; $CE_2 = V_{IH}$; $I_{I/O} = 0$ (min cycle)
	I_{CCA2}		5	10	mA	$\overline{CE} = V_{IL}$; $CE_2 = V_{IH}$; $I_{I/O} = 0$ (dc current)
Standby supply current	I_{CCS1}		0.004	10 (Note 2)	μA	$\overline{CE} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V
	I_{CCS2}		0.004	10 (Note 2)	μA	$CE_2 \leq 0.2$ V
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 2.1$ mA
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1.0$ mA

Notes:

(1) μPD4464-20/-20L: 35 mA max

(2) μPD4464-12L/-15L/-20L: 1.0 μA max (−40 to 60°C)
0.2 μA max (−40 to 25°C)

Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	X	X	Not selected	High-Z	Standby
X	L	X	X	Not selected	High-Z	Standby
L	H	H	H	D_{OUT} disabled	High-Z	Active
L	H	L	H	Read	D_{OUT}	Active
L	H	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care

AC Characteristics

$T_A = -40$ to $85°C$; $V_{CC} = +5.0$ V ±10%

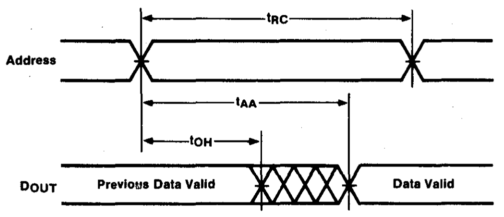
		Limits							
		μPD4464-12		μPD4464-15		μPD4464-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Cycle									
Read cycle time	t_{RC}	120		150		200		ns	
Address access time	t_{AA}		120		150		200	ns	
$\overline{CE}_1$ access time	t_{CO1}		120		150		200	ns	
CE_2 access time	t_{CO2}		120		150		200	ns	
Output enable to output valid	t_{OE}		60		75		100	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
Chip enable ($\overline{CE}_1$) to output in low-Z	t_{LZ1}	10		10		100		ns	
Chip enable (CE_2) to output in low-Z	t_{LZ2}	10		10		10		ns	
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	
Chip enable ($\overline{CE}_1$) to output in high-Z	t_{HZ1}		40		75		100	ns	
Chip enable (CE_2) to output in high-Z	t_{HZ2}		40		75		100	ns	
Output enable to output in high-Z	t_{OHZ}		40		60		80	ns	
Write Cycle									
Write cycle time	t_{WC}	120		150		200		ns	
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	85		130		180		ns	
Chip enable (CE_2) to end of write	t_{CW_2}	85		130		180		ns	
Address valid to end of write	t_{AW}	85		130		180		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	70		100		140		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	50		70		80		ns	
Data hold time	t_{DH}	5		5		5		ns	
Write enable to output in high-Z	t_{WHZ}		40		75		100	ns	
Output active from end of write	t_{OW}	5		10		10		ns	

Notes:

(1) Input pulse levels = 0.8 V to 2.4 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; output load = 1 TTL gate and C_L = 100 pF.

Timing Waveforms

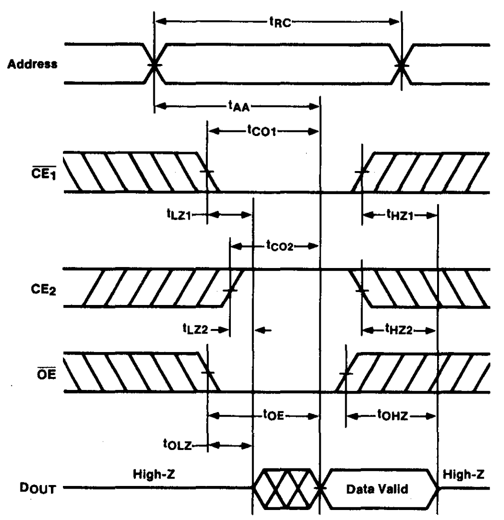
Read Cycle No. 1 (Address Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The device is continuously selected; $\overline{CE}_1 = \overline{OE} = V_{IL}$, $CE_2 = V_{IH}$.

83-001755A

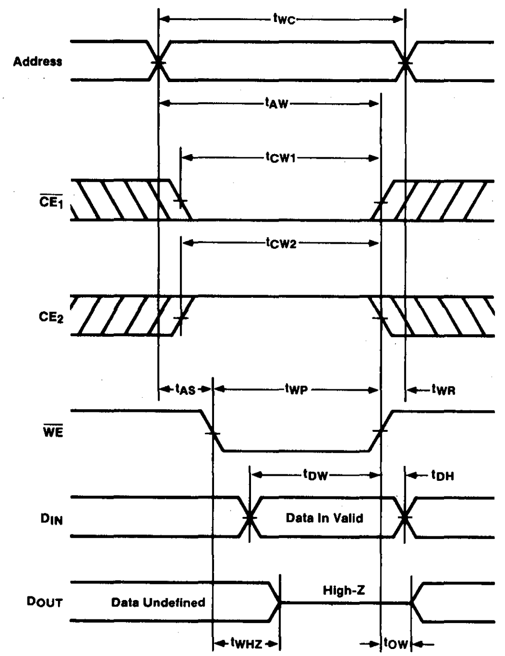
Read Cycle No. 2 (Chip Enable Access)



Note:
[1] $\overline{WE}$ is a high for a read cycle.
[2] The address inputs are valid prior to or coincident with the $\overline{CE}_1$ transition low and the CE_2 transition high.

83-001756A

Write Cycle No. 1 ($\overline{WE}$-Controlled)

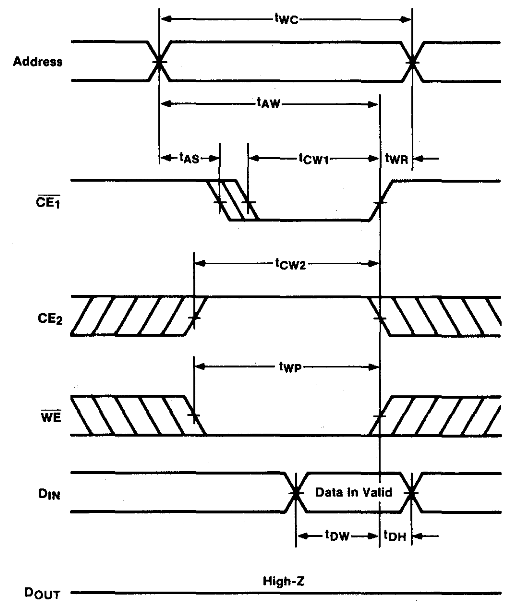


Note:
[1] A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.
[3] If $\overline{OE}$ is high the I/O pins remain in a high impedance state.

83-001757A

Timing Waveforms (cont)

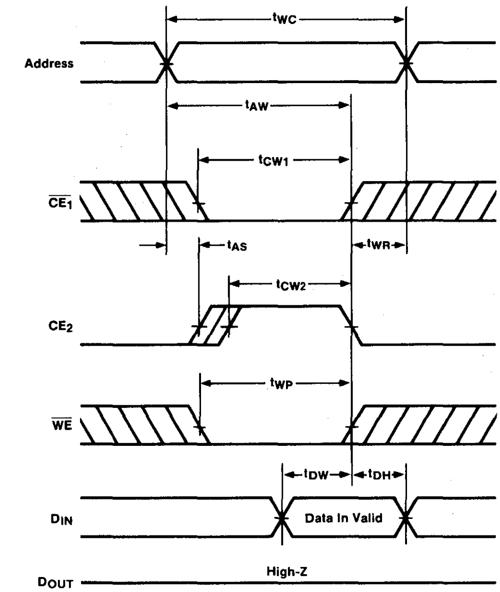
Write Cycle No. 2 ($\overline{CE}_1$-Controlled)



Note:
[1] A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.

83-004999A

Write Cycle No. 3 (CE_2-Controlled)



Note:
[1] A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
[2] $\overline{CE}_1$ or $\overline{WE}$ [or CE_2] must be high [low] during any address transition.

83-00500A

6

Low V_{CC} Data Retention Characteristics

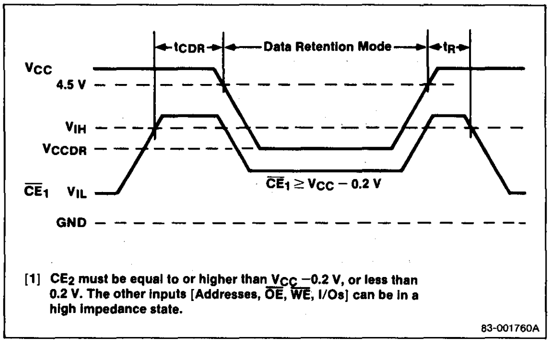
$T_A = -40$ to $85°C$

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Data retention supply voltage	V_{CCDR1}	2.0		5.5	V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V
	V_{CCDR2}	2.0		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		0.003	10 (Note 1)	μA	$V_{CC} = 3.0$ V; $\overline{CE}_1 \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V
	I_{CCDR2}		0.003	10 (Note 1)	μA	$V_{CC} = 3.0$ V; $CE_2 \leq 0.2$ V
Chip deselect to data retention time	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

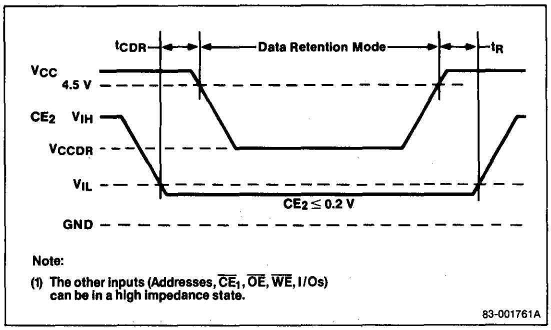
Notes:

(1) μPD4464-12L/-15L/-20L: 1.0 μA max (−40 to 60°C)
0.2 μA max (−40 to 25°C)

Data Retention ($\overline{CE}_1$-Controlled)



Data Retention (CE_2-Controlled)



NEC
NEC Electronics Inc.

μPD43254 65,536 x 4-BIT STATIC CMOS RAM

PRELIMINARY INFORMATION

Description

The μPD43254 is a 65,536-word by 4-bit static RAM fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD43254 a high-speed device that requires very low power and no clock or refreshing to operate.

The μPD43254 is packaged in a standard 24-pin plastic DIP.

Features

- ☐ 65,536-word x 4-bit organization
- ☐ Single +5-volt power supply
- ☐ Fully static operation—no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Common I/O capability
- ☐ Low power consumption
  - — Active: 120 mA
  - — Standby: 2 mA
- ☐ Standard 300-mil, 24-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD43254C-35	35 ns	24-pin plastic DIP
C-45	45 ns	
C-55	55 ns	

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

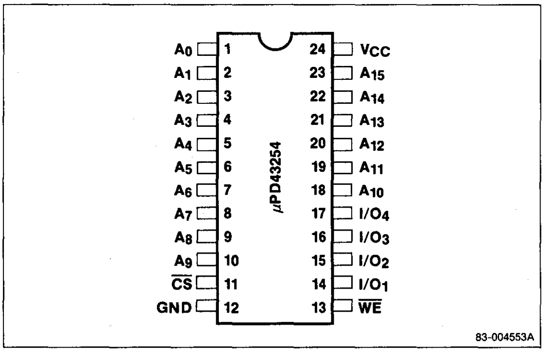
Notes:

(1) $V_{IN} = -3.0$ V minimum for 20 ns pulse.

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configuration

24-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{15}	Address inputs
I/O_1-I/O_4	Data inputs/outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Recommended Operating Conditions

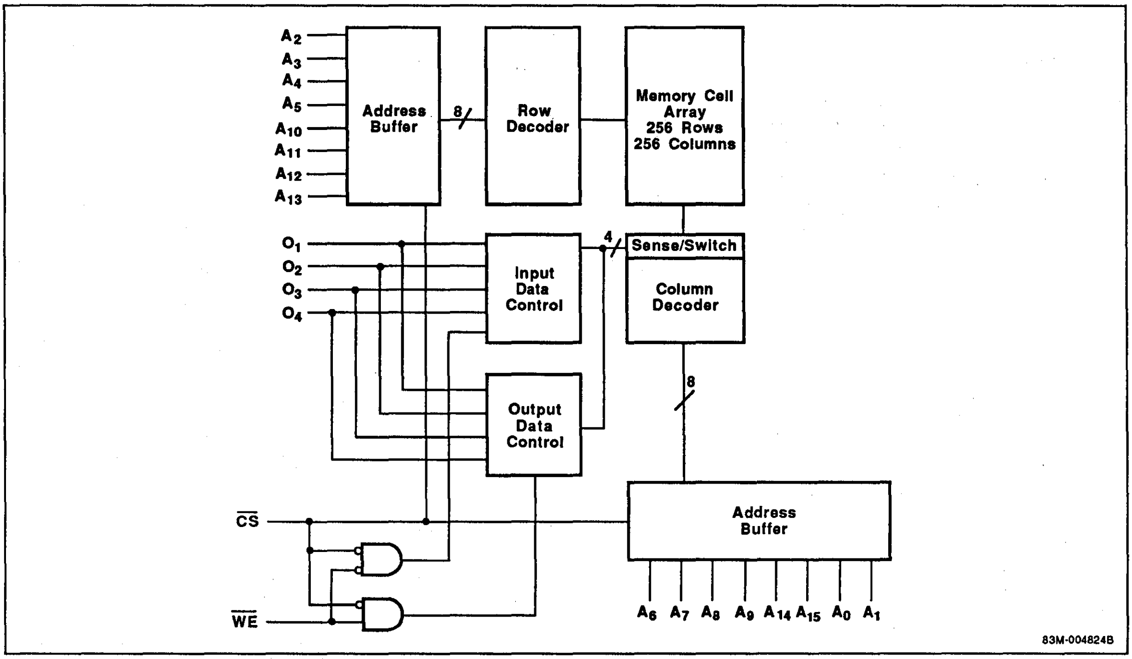
		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) $V_{IL} = -3.0$ V minimum for 20 ns pulse

6

Block Diagram



Capacitance

$T_A = 25°C$; f = 1 MHz (Note 1)

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			5	pF	$V_{IN} = 0$ V
I/O capacitance	C_{DOUT}			7	pF	$V_{DOUT} = 0$ V

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	D_{OUT}	Active
L	L	Write	D_{IN}	Active

Notes:

(1) X = don't care

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ± 10%

		Limits			
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2	2	μA	$V_{IN} = 0$ to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2	2	μA	$V_{OUT} = 0$ to V_{CC}; $\overline{CS} = V_{IH}$; V_{CC} = max
Operating supply current	I_{CC}		120	mA	$\overline{CS} = V_{IL}$; $I_{DOUT} = 0$ mA
Standby supply current	I_{SB}		20	mA	$\overline{CS} = V_{IH}$
	I_{SB1}		2	mA	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}		0.4	V	$I_{OL} = 8.0$ mA
Output voltage, high	V_{OH}	2.4		V	$I_{OH} = -4.0$ mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD43254-35 Min	μPD43254-35 Max	μPD43254-45 Min	μPD43254-45 Max	μPD43254-55 Min	μPD43254-55 Max	Unit	Test Conditions
Read Cycle									
Read cycle time	t_{RC}	35		45		55		ns	(Note 2)
Address access time	t_{AA}		35		45		55	ns	
Chip select access time	t_{ACS}		35		45		55	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip selection to output in low-Z	t_{LZ}	5		5		5		ns	(Note 3)
Chip deselection to output in high-Z	t_{HZ}	0	15	0	20	0	25	ns	(Note 4)
Chip selection to power-up time	t_{PU}	0		0		0		ns	
Chip deselection to power-down time	t_{PD}	0	35	0	45	0	55	ns	
Write Cycle									
Write cycle time	t_{WC}	35		45		55		ns	(Note 2)
Chip select to end of write	t_{CW}	30		40		50		ns	
Address valid to end of write	t_{AW}	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	25		35		45		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	15		20		25		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	15	0	20	0	25	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} +200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

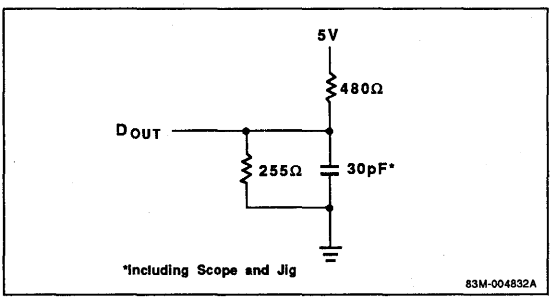
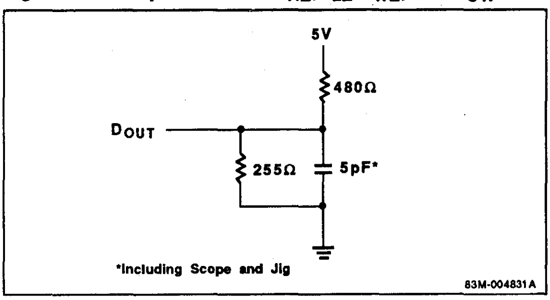


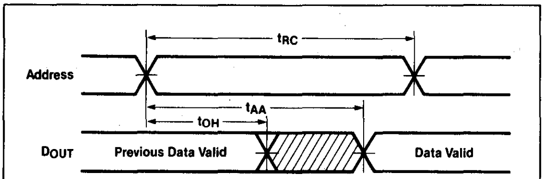
Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}



6

Timing Waveforms

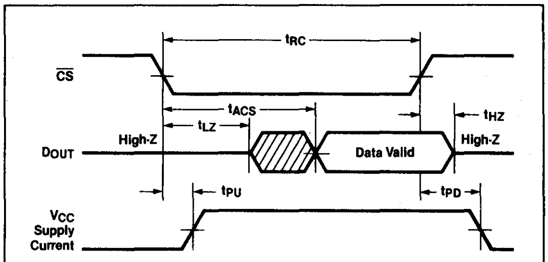
Read Cycle No. 1 (Address Access)



Notes:
[1] $\overline{WE}$ is held high for read cycle.
[2] Device is continuously selected; $\overline{CS} = V_{IL}$.

83-001636A

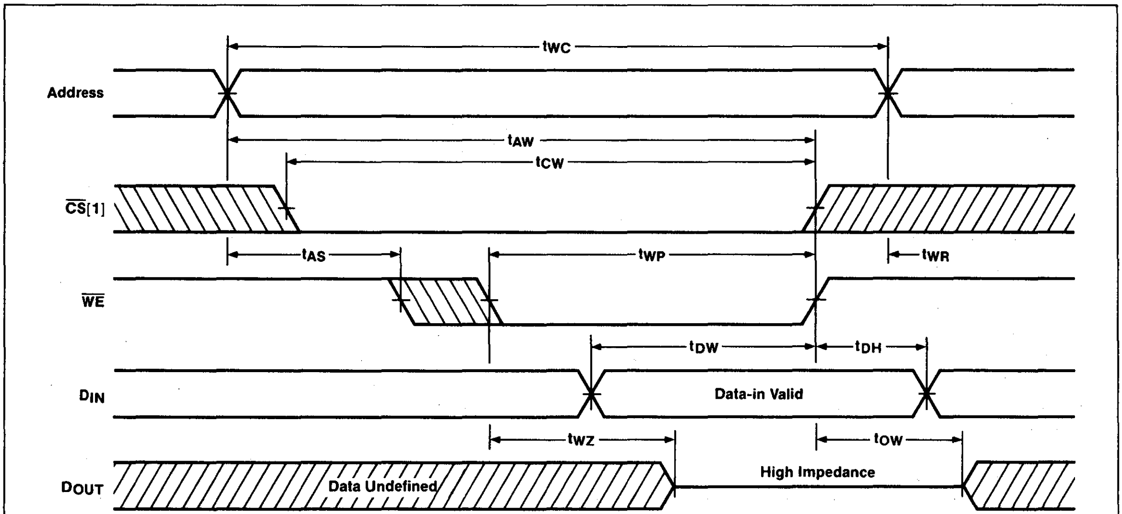
Read Cycle No. 2 (Chip Select Access)



Note: [1] $\overline{WE}$ is held high for read cycle.
[2] Address valid prior to or coincident with $\overline{CS}$ transition low.

83-001548A

Write Cycle No. 1 ($\overline{WE}$-Controlled)

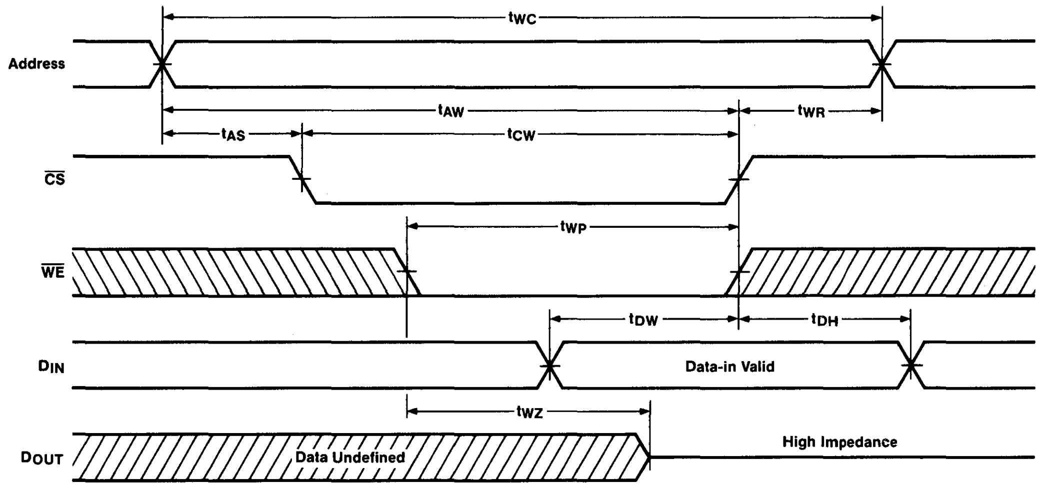


Notes:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-005098B

Timing Waveforms (cont)

Write Cycle No. 2 ($\overline{CS}$-Controlled)



Notes:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83-005099B

μPD43256A 32,768 x 8-BIT STATIC CMOS RAM

Description

The μPD43256A is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique circuitry, using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors, makes the μPD43256A a high-speed device that requires very low power and no clock or refreshing to operate.

Minimum standby power is drawn when $\overline{CS}$ is at a high level, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 V. The μPD43256A is available in standard 28-pin plastic DIP or 28-pin plastic miniflat packaging.

Features

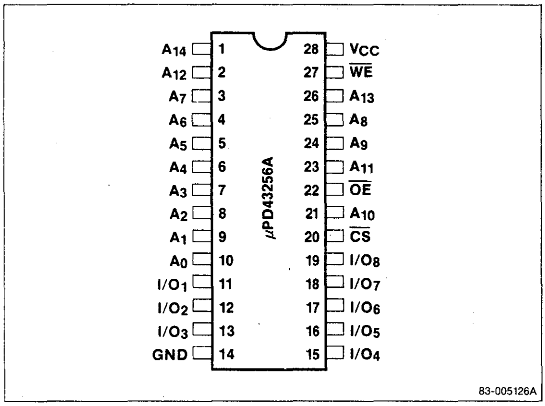
- ☐ Single +5-volt power supply
- ☐ Fully static operation—no clock or refreshing required
- ☐ TTL-compatible inputs and outputs
- ☐ Common I/O using three-state outputs
- ☐ One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- ☐ Data retention voltage: 2 V minimum
- ☐ Standard 28-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Data Retention Current (max) $T_A = 0\text{-}70°C$	Package
μPD43256AC-85L	85 ns	50 μA	28-pin plastic DIP (600 mil)
C-10L	100 ns		
C-12L	120 ns		
C-15L	150 ns		
μPD43256AC-85LL	85 ns	20 μA	28-pin plastic DIP (600 mil)
C-10LL	100 ns		
C-12LL	120 ns		
C-15LL	150 ns		
μPD43256AGU-85L	85 ns	50 μA	28-pin plastic miniflat
GU-10L	100 ns		
GU-12L	120 ns		
GU-15L	150 ns		
μPD43256AGU-85LL	85 ns	20 μA	28-pin plastic miniflat
GU-10LL	100 ns		
GU-12LL	120 ns		
GU-15LL	150 ns		

Pin Configuration

28-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0-A_{14}	Address inputs
I/O_1-I/O_8	Data inputs/qutputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

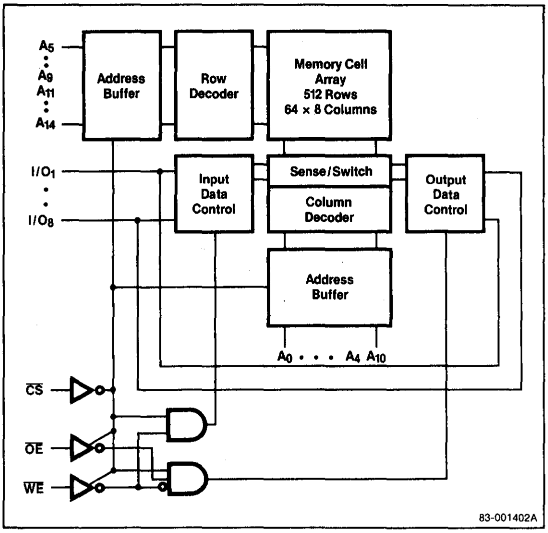
Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Not selected	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to 70°C
Storage temperature, T_{STG}	−55 to 125°C
Power dissipation, P_D	1.0 W

Notes:

(1) −3.0 V minimum (pulse width 50 ns)

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

$T_A = 25°C$; f = 1 MHz

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_{IN}			5	pF	$V_{IN} = 0$ V
Input/output capacitance	$C_{I/O}$			8	pF	$V_{I/O} = 0$ V

Recommended Operating Conditions

		Limits			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width 50 ns)

DC Characteristics

T_A = 0 to 70°C; V_{CC} = +5.0 V ±10%

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input leakage current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
I/O leakage current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CCA1}			45	mA	$\overline{CS} \leq V_{IL}$ (min cycle); $I_{I/O} = 0$ (Note 1)
	I_{CCA2}			10	mA	$\overline{CS} = V_{IL}$; $I_{I/O} = 0$
	I_{CCA3}			10	mA	$\overline{CS} \leq 0.2$ V; f = 1 MHz; $I_{I/O} = 0$; $V_{IL} \leq 0.2$ V; $V_{IH} \geq V_{CC} - 0.2$ V
Standby supply current	I_{SB}			3	mA	$\overline{CS} \geq V_{IH}$
	I_{SB1}		0.002	0.1	mA	$\overline{CS} \geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −0.1 mA

Notes:

(1) μPD43256A-10L/-10LL/-12L/-12LL: 40 mA (max)
μPD43256A-15L/-15LL: 35 mA (max)

AC Characteristics

T_A = 0 to 70°C; V_{CC} = +5.0 V ±10%

		Limits									
		μPD43256A-85L/-85LL		μPD43256A-10L/-10LL		μPD43256A-12L/-12LL		μPD43256A-15L/-15LL			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Cycle											
Read cycle time	t_{RC}	85		100		120		150		ns	
Address access time	t_{AA}		85		100		120		150	ns	(Note 2)
Chip select access time	t_{ACS}		85		100		120		150	ns	(Note 2)
Output enable to output valid	t_{OE}		40		50		60		70	ns	(Note 2)
Output hold from address change	t_{OH}	10		10		10		10		ns	
Chip select to output in low-Z	t_{CLZ}	10		10		10		10		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	5		5		5		5		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		30		35		40		50	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		30		35		40		50	ns	(Note 3)
Write Cycle											
Write cycle time	t_{WC}	85		100		120		150		ns	
Chip select to end of write	t_{CW}	70		80		85		100		ns	
Address valid to endof write	t_{AW}	70		80		85		100		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	65		70		70		90		ns	
Write recovery time	t_{WR}	5		5		5		5		ns	
Data valid to end of write	t_{DW}	35		40		50		60		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		30		35		40		50	ns	(Note 3)
Output active from end of write	t_{OW}	10		10		10		10		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output loading.

(3) See figure 2 for output loading.

Figure 1. Output Load

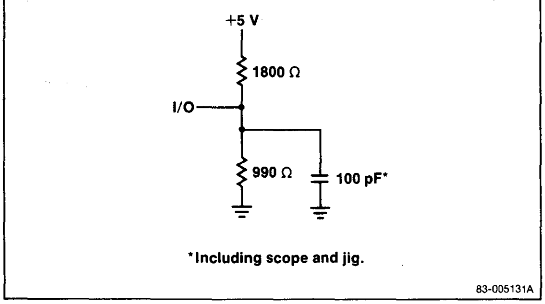
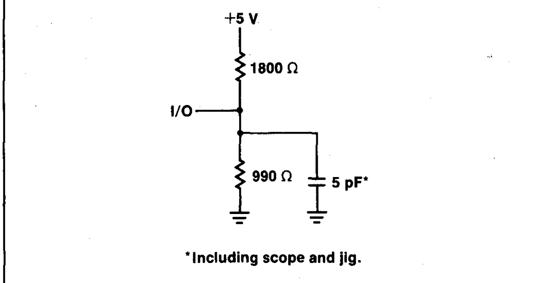
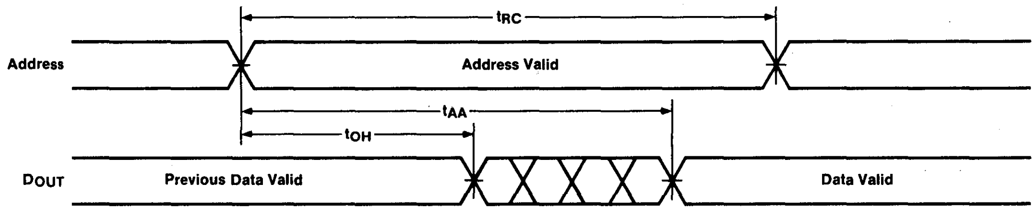


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

Read Cycle No. 1 (Address Access)



Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] The device is continuously selected; $\overline{CS} = \overline{OE} = V_{IL}$.

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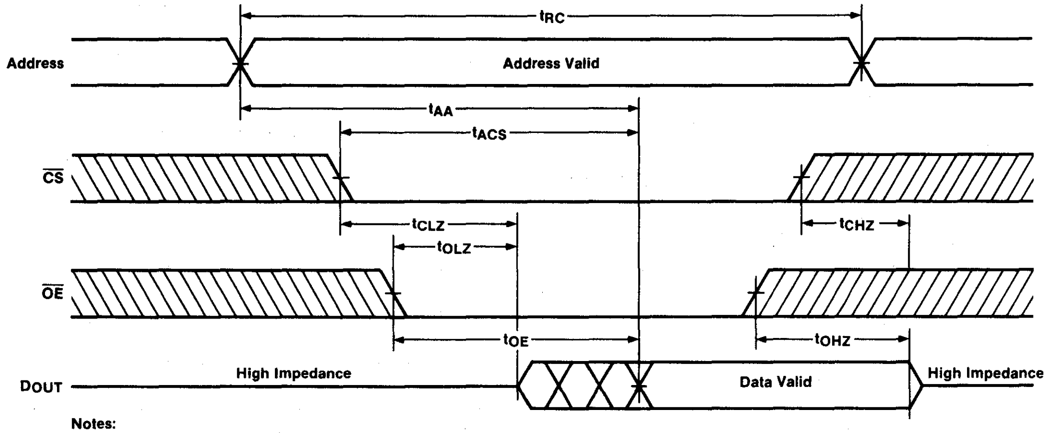
Timing Waveforms (cont)

Read Cycle No. 2 (Chip Select Access)



Notes:

[1] $\overline{\text{WE}}$ is high for a read cycle.

[2] Address valid prior to or coincident with $\overline{\text{CS}}$ transition low.

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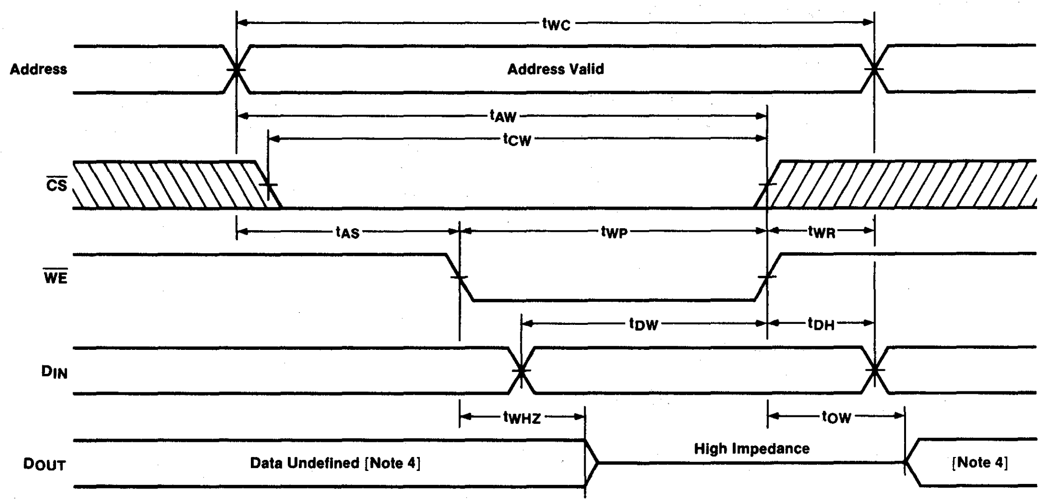
Write Cycle No. 1 ($\overline{\text{WE}}$-Controlled)



Notes:

[1] A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.

[2] $\overline{\text{CS}}$ or $\overline{\text{WE}}$ must be high during address transition.

[3] If $\overline{\text{OE}}$ is high, the I/O pins remain in a high-impedance state.

[4] During this period, the I/O pins may be in the output state; therefore, input signals of opposite phase to the outputs must not be applied.

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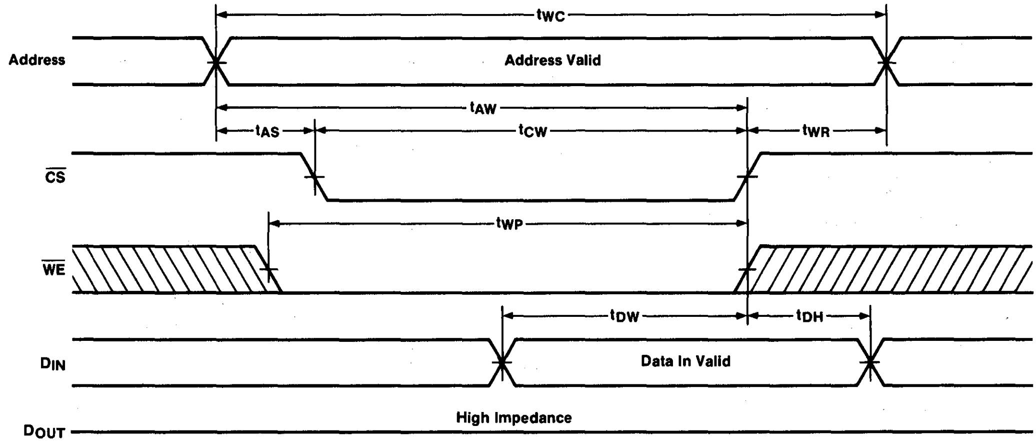
Timing Waveforms (cont)

Write Cycle No. 2 ($\overline{CS}$-Controlled)



Notes:

[1] **A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.**

[2] **$\overline{CS}$ or $\overline{WE}$ must be high during address transition.**

[3] **If $\overline{OE}$ is high, the I/O pins remain in a high-impedance state.**

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Low V_{CC} Data Retention Characteristics

$T_A = 0$ to 70°C

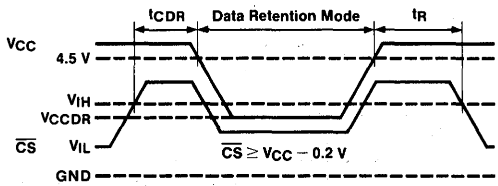
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$CS \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	$V_{CC} = 3.0$ V; $CS \geq V_{CC} - 0.2$ V (Notes 1, 2)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) For μPD43256A-LL, $I_{CCDR} = 20$ μA (max) for $T_A = 0$ to 70°C and 3 μA (max) for $T_A = 0$ to 40°C.

(2) For μPD43256A-L, $I_{CCDR} = 15$ μA (max) for $T_A = 0$ to 40°C.

Data Retention Timing Chart



Note:

[1] **The other inputs [Addresses, $\overline{OE}$, $\overline{WE}$, I/Os] can be in a high-impedance state.**

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APPLICATION NOTE 50 BATTERY BACKUP CIRCUITS FOR SRAMs

Introduction

The evolution of low-power, high-capacity, high-speed memory technologies has led the system designer to novel and highly portable computer designs. As technology has advanced to low-power devices, it has become possible to make an entire system nonvolatile for the life of the product.

To provide this nonvolatile function, secondary power sources are mounted on a printed circuit board controlled by a backup circuit that switches from the primary power to secondary power during power failures. The backup issue is considered as part of the overall system design, and the choice of a secondary power source and backup circuit are based on the unique characteristics of each application.

This application note deals with the issues of providing a nonvolatile memory system. A review of the evolution of static RAMs (SRAMs) with regard to state-of-the-art, low-power SRAM technology is followed by an example of secondary power sources, as well as several sample backup circuit designs.

SRAM Technology

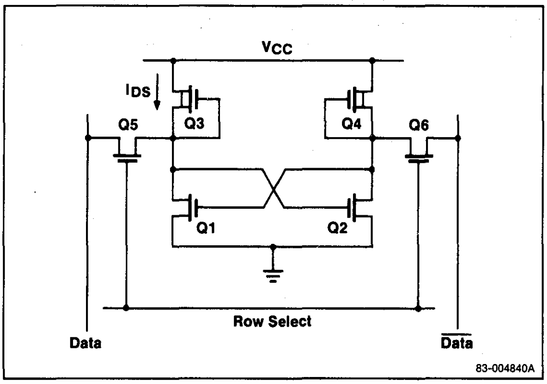
The SRAM historically has been used by system designers to provide a high-speed, low-power data storage function for a variety of computer architectures. The higher cost-per-bit compared to dynamic memories is offset by a simpler circuit design that features a nonmultiplexed address structure, simple timing signals, and no refresh requirement.

Six-Transistor Cell

The development of the SRAM memory cell has followed the trail of bipolar, NMOS, and CMOS technologies in that large-capacity memory devices require minimal cell size, not only to reduce power requirements, but also to be able to fit the die into the package.

The static memory cell is basically a cross-coupled flip-flop circuit requiring no clocks or refreshing. Early six-transistor NMOS static memory cell designs employed the use of enhancement or depletion mode FETs as load devices. Figure 1 shows an example using depletion loads. Q3 and Q4 are depletion-type devices fabricated such that they are always conductive when their respective gate and source nodes are shorted together. If the gate of enhancement device Q2 is written to a low level using Q5 and the data line, Q2 turns off. This allows load device Q4 to pull its source node high and turn on Q1; the write operation using Q6 also helps this action. The cell is designed so that Q1 has much lower "on" resistance than its load Q3. After the write operation ends, and Q5 and Q6 are off, Q1 keeps its drain node at a low level to maintain Q2 in the off state, while the drain node of Q2 is maintained high by Q4. The stored voltages are stable.

Figure 1. Six-Transistor Cell—Depletion



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Four-Transistor Cell

As NMOS technology evolved, the active device for the load was replaced with polysilicon resistors (see figure 2). With the polysilicon load resistor, current levels of less than 1 nA are achievable. Because of these low-current levels, the cell can be used in advanced SRAMs with very high memory density and low standby current. NEC uses this technology in its low-power family of SRAMs to facilitate their use in battery backup applications. This type of core cell is used in both NMOS and CMOS SRAMs from NEC.

CMOS Cell

CMOS technology, with its high-speed, low-power characteristics, makes an attractive choice for memory backup systems.

In figure 3, Q1-Q3 and Q2-Q4 form two CMOS inverters that are cross-coupled to form the conventional flip-flop of the SRAM cell. Unlike the enhancement or polysilicon resistor cells, the CMOS cell does not have a dc current path (other than leakage) in either of its quiescent logic states. While the potentially lower-leakage and wider-voltage operating range makes the six-transistor CMOS cell very desirable for battery backup operation, the large die area required makes it less competitive in cost and memory density.

Figure 2. Four-Transistor Cell—Polysilicon Resistor

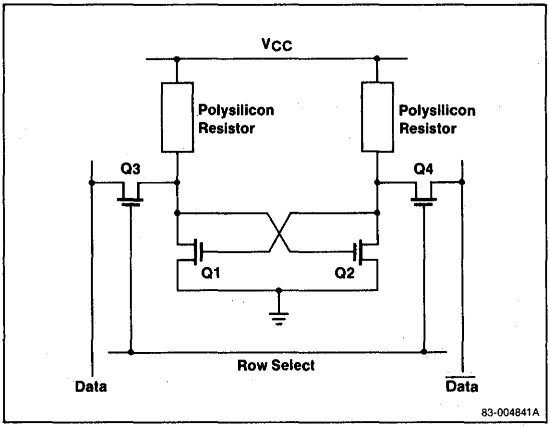
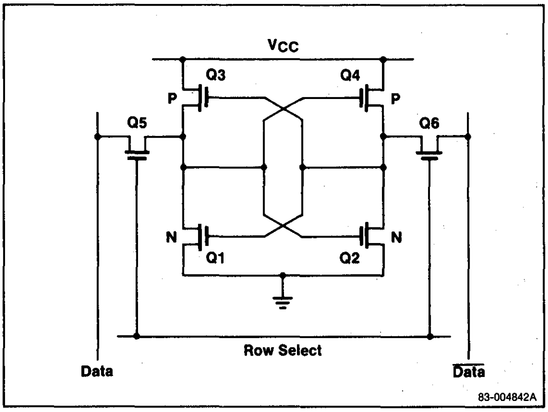


Figure 3. CMOS Cell



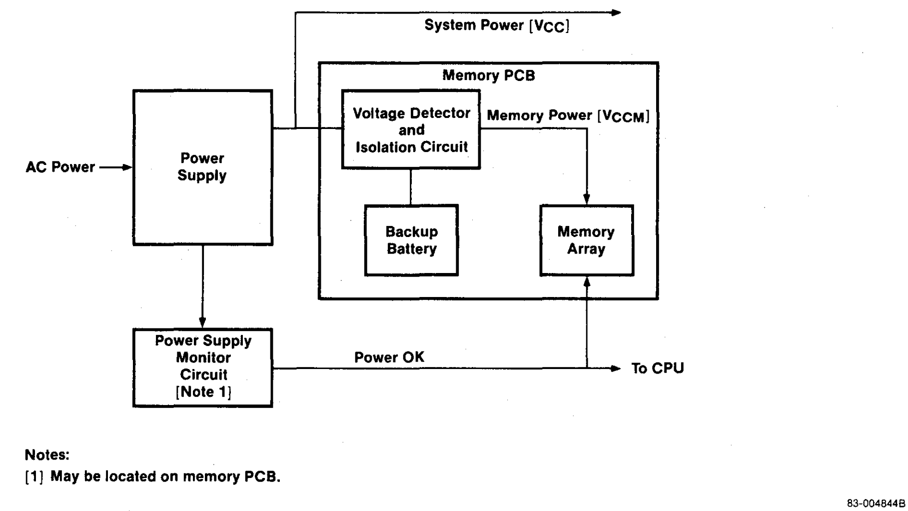
Battery Backup Concept

The goal of a memory backup system design is to guarantee memory data retention for days, months, or years. In the past, these memory backup circuits were implemented as part of the computer's power supply circuit. Today, the memory backup function is designed as part of the individual memory circuit, where each provides a constant secondary (backup) power source and the necessary circuitry to detect power failures and isolate the main power supply from the backup power source (battery). The battery backup circuit must be an integral part of printed circuit board layout. Furthermore, SRAM technology must be able to guarantee the requirements of the memory battery backup function. The following sections discuss in detail the aspects of memory battery backup circuit design using NEC's low-power SRAM technology.

A typical functional block diagram for a memory battery backup system is illustrated in figure 4. The power supply converts ac voltage into a regulated dc voltage, which powers all of the system components (V_{CC}). The power supply monitor circuit detects a power failure and generates an interrupt to the CPU. This circuit also signals the memory circuit to deselect the memory array, thus protecting the memory from false CPU commands. The power supply monitor circuit may be centralized to the power supply or decentralized to each memory circuit.

On the memory circuit, power failure is sensed by a voltage-detector circuit, which isolates the system power from the memory power, allowing the backup battery to become active.

Figure 4. Battery Backup System Block Diagram



Backup Battery Selection

Battery Type

Nickel-cadmium batteries and lithium batteries were compared for use in a memory battery backup application. Although nickel-cadmium batteries have been a popular choice for this application, recent years have seen the development of lithium batteries. Some characteristics of these two types of batteries are contrasted in table 1. For additional comparison, the characteristics of current drain versus operating time for nickel-cadmium and lithium batteries are shown in figures 5 and 6, respectively.

Since lithium batteries provide a constant current for up to 10 years in this type of low-power application, they were chosen over nickel-cadmium for this design example. A single 3-volt lithium battery is adequate for most CMOS SRAM applications. If higher voltage is required, batteries may be connected in series.

Physical characteristics of a battery are determined by the manufacturer according to common system requirements. The designer must select a battery of the proper size and shape to meet the requirements of printed circuit board technology. Such requirements may include terminal connections and solderability.

Table 1. Lithium Versus Nickel-Cadmium Battery Characteristics

Characteristic	Lithium	Nickel-Cadmium
Shelf life	10 years	6 months
Rechargeable	no	yes
Energy density	5000 mAh*	4000 mAh*
Cost	moderate	moderate
PCB-compatible	yes	yes

*milliampere hours

Figure 5. Current Drain Versus Operating Time—Nickel Cadmium Battery

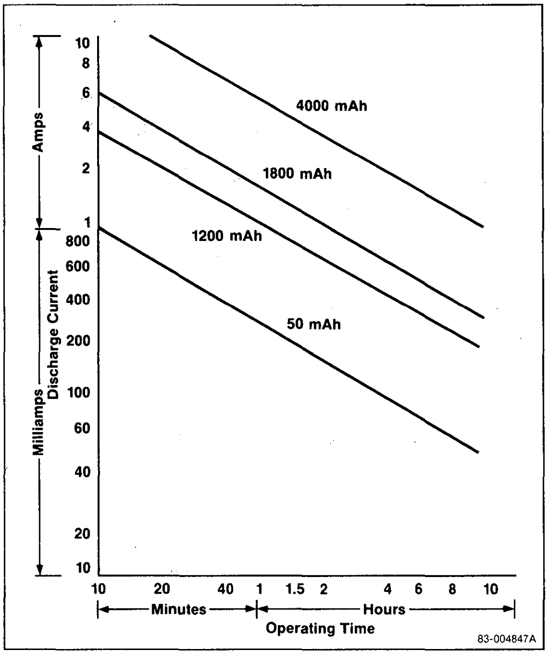
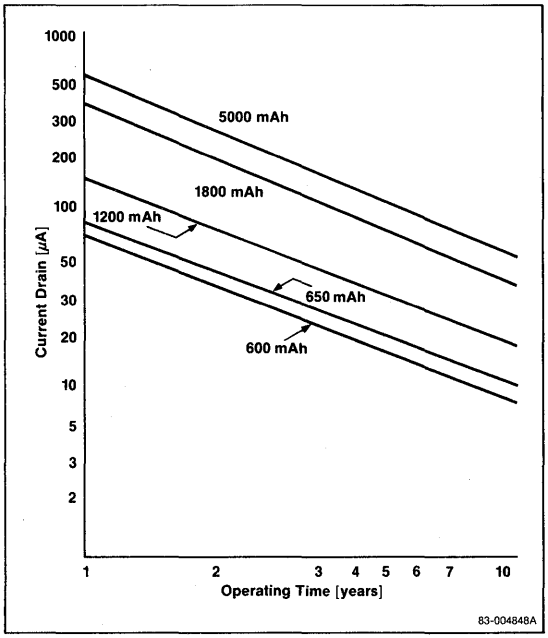


Figure 6. Current Drain Versus Operating Time—Lithium Battery



Battery Capacity

Battery capacity defines the current drive of the battery over a period of time, measured in milliampere hours (mAh). Required capacity of the battery selected for the memory backup circuit can be determined from the following formula:

Current required (mA) x time in backup mode (hours/day) x 365 days/year x number of years

Battery capacity is affected by temperature, humidity, and load conditions. The designer must ensure that these conditions do not degrade the operating life (discharge characteristics) of the battery. Figures 7 and 8 show the effects of temperature and load current variations on lithium battery discharge characteristics.

Figure 7. Lithium Discharge Characteristics— ≃ 20 μA Load

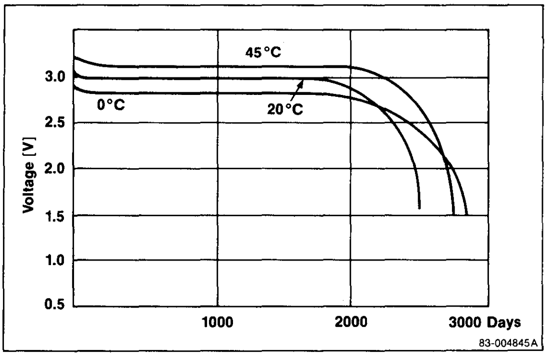
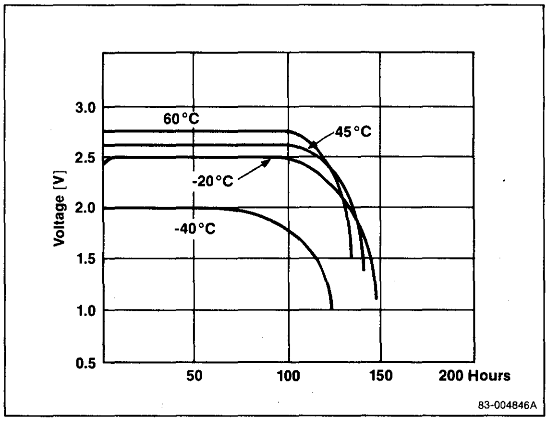


Figure 8. Lithium Discharge Characteristics— ≃ 8.5 mA Load



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Design Example

This section presents and documents a detailed battery backup design example. The discussion encompasses SRAM memory array design, current and voltage requirements, voltage-detector and isolation circuitry, and memory protection design considerations.

SRAM Memory Array

For the battery backup design example, NEC's μPD43256A-15LL (a CMOS-fabricated, 150-ns SRAM memory device) is used to implement the memory array, configured as 32K by 32 bits using four 32K x 8-bit memory devices (figure 9). The memory array's interface of common address lines, common I/O lines, and control signals are asserted by control logic common to all devices. However, the power supply connection to the memory array requires special consideration. The power plane of the memory array must be isolated from the system power supply to ensure that the backup battery drives only the memory array (see "Voltage-Level Detector and Isolation Circuit Design").

Current and Voltage Requirements

The first task for the designer is to define the required battery capacity. Table 2 shows data retention characteristics for the μPD43256A SRAM. The maximum data retention current for this device is 20 μA at 0 to 70°C. For a circuit with four memory devices, total memory array current is 4 x 20 μA = 80 μA.

The battery's operating period is assumed to be 10 years at 12 hours-per-day. Using the formula shown under "Battery Capacity," the required capacity of the battery can be derived from this calculation.

80 μA x 12 hours/day x 365 days/year x 10 years = 3504 mAh

Requirements for the data retention voltage of the μPD43256A SRAM are defined in table 2, while figure 10 shows timing requirements for data retention with respect to the $\overline{CS}$ chip select signal.

Table 2. μPD43256A SRAM Data Retention Characteristics

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	$V_{CC} = 3.0$ V; $\overline{CS} \geq V_{CC} - 0.2$ V (Notes 1, 2)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) μPD43256A-LL: I_{CCDR} = 20 μA (max) for T_A = 0 to 70°C and 3 μA (max) for T_A = 0 to 40°C.

(2) μPD43256A-L: I_{CCDR} = 15 μA (max) for T_A = 0 to 40°C.

Figure 9. SRAM Memory Array

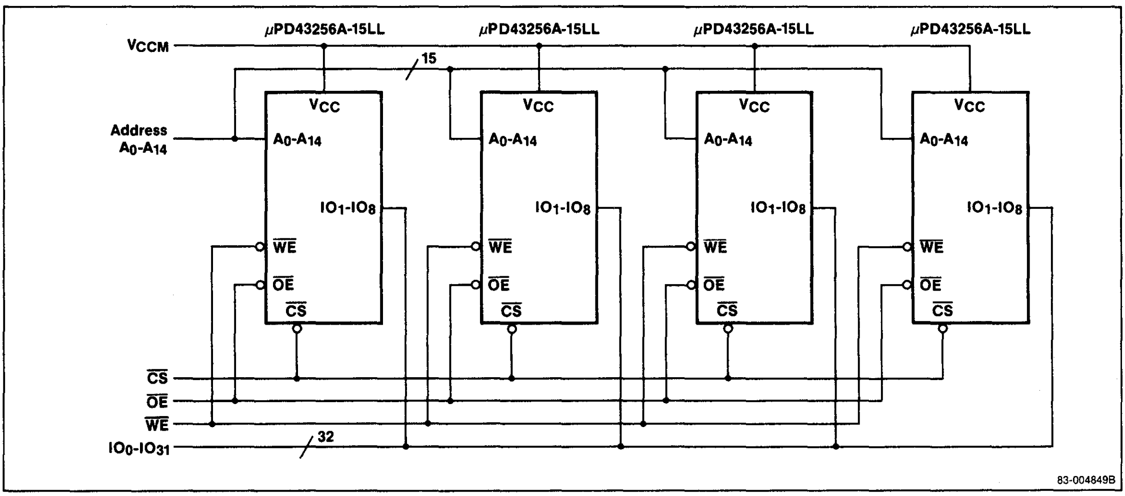
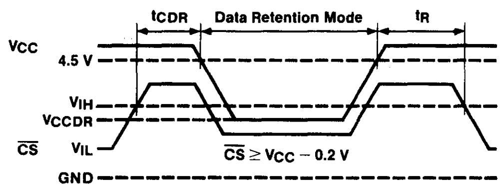


Figure 10. Data Retention Timing Waveforms



Note:
[1] The other inputs [Addresses, OE, WE, I/Os] can be in a high-impedance state.

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Battery Protection. Figure 11 shows the battery portion of the memory battery backup circuit. This portion of the circuit must be designed to provide the required data retention voltage and energy capacity for the memory backup function, yet protect the battery from reverse (charging) current. The diode and resistor shown in figure 11 were selected to protect the battery according to UL standards.

Since lithium batteries are not rechargeable, current-limiting protection must be provided to control the amount of current from the main power supply. For this purpose, the designer must select a diode that protects against charging current, yet provides sufficient voltage for memory battery backup.

The UL-allowable charging current for a lithium battery is specified as 1% of the battery capacity, calculated as follows:

1% x capacity of battery (mAh) ÷ (amount of time charging may occur (hours/day) x 365 days/year x number of years)

In this design example, a minimum capacity of 3504 mAh is required. The closest standard-size lithium battery has a capacity of 5000 mAh. The allowed charging current of this battery for a 10-year period is calculated in this way:

1% x 5000 mAh ÷ (12 hours/day x 365 days/year x 10 years) = 1.1 μA

Therefore, the diode selected to protect the battery must have a maximum reverse leakage current rating of 1.1 μA. To maintain the required data retention voltage at the memory device, a diode with a small forward-voltage drop must be selected. A Schottky diode, with a forward-voltage drop of 0.2 volt, provides a 2.7-volt battery backup voltage and also meets the reverse leakage current specification for this circuit.

According to UL standards, the battery must also be protected against charging current in case the protection diode is damaged. The designer must select a current-limiting resistor for this purpose. Resistor value is determined according to this formula:

$(V_{CC} - V_{Battery})$ ÷ maximum charging current

UL standards specify a maximum charging current of 5 mA. Therefore, for the circuit in this design example, the minimum resistor value is specified as follows:

(5.5 − 3 V) ÷ 5 mA = 500 Ω

Selecting the aforementioned Schottky diode and a standard 10% resistor value of 560 Ω would guarantee minimum data retention voltage for the battery backup circuit. Total voltage drop across the protection diode and current-limiting resistor is equal to 0.245 volt, which provides a memory backup voltage of 2.755 volts—well above the minimum data retention voltage of 2 volts.

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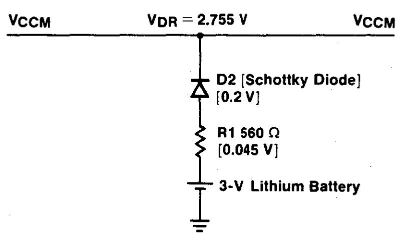
Figure 11. Backup Energy Source Circuit



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Voltage-Level Detector and Isolation Circuit Design

The designer must also determine the best method for detecting power failures and isolating the main power supply from the backup battery. The circuit designed for these functions must fulfill two requirements: 1) sustain maximum operating current for the memory array, and 2) provide isolation protection during battery backup operation. Several design alternatives for voltage-level detector and isolation circuits are discussed in this section. The standards of comparison between these circuits are relative simplicity of design and voltage drop of the isolation element.

Note: In applications that are subjected to brownouts or extreme temperatures, these voltage-level detector and isolation circuits will minimize unnecessary cycling of the backup battery. However, considerations must be made to protect the memory devices from unstable circuit conditions, especially during power failure. For a discussion of memory protection under these circumstances, refer to "System Power Failure Design Considerations," following this section.

The designer must first determine maximum operating current of the memory array. Since maximum operating current for the μPD43256A SRAM is specified as 35 mA, total operating current is calculated as 4 x 35 mA = 140 mA for the memory array in this design example.

Diode Isolation Circuit. The diode isolation circuit in figure 12 provides a simple approach to memory battery backup. The isolation diode (D1) must be able to sustain the maximum memory operating current, yet minimize voltage skew between V_{CC} and V_{CCM} by limiting forward-voltage drop. A large voltage skew could cause illegal conditions to occur in normal system operations. A typical silicon diode with a forward-voltage drop of 0.7 V at a 140-mA load current would provide a large voltage skew between V_{CC} and V_{CCM}. Since SRAM V_{CC} is 0.7 V less than the level of a logic signal from a device not in the backup system, V_{CC} would have to be adjusted to a nonstandard level of 5.7 V to maintain V_{CC} at 5 V.

In contrast, a Schottky diode typically provides a forward-voltage drop of 0.2 V at a 3-A load current. This low voltage drop minimizes voltage skew and maintains logic input levels to within 0.2 V of V_{CC}, which makes the Schottky diode an ideal choice for the diode isolation circuit.

Voltage-Level Detector Circuit. The diode isolation circuit provides a simple means of battery backup, but some applications may require a circuit that minimizes voltage skew and has a more defined threshold level. The voltage-level detector circuit shown in figure 13 would allow the designer to fulfill these system requirements.

The voltage-level detector circuit isolates the supply voltage from the memory voltage when the voltage level falls below V_{CC} minimum. Threshold voltage is specified by using a zener diode in the voltage-divider circuit of figure 13. Care must be taken to ensure that marginal V_{CC} levels do not cause unnecessary cycling of the backup battery.

Figure 12. Diode Isolation Circuit

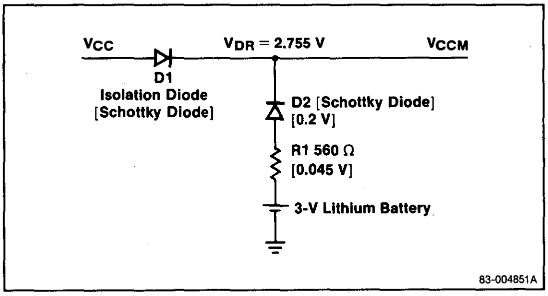
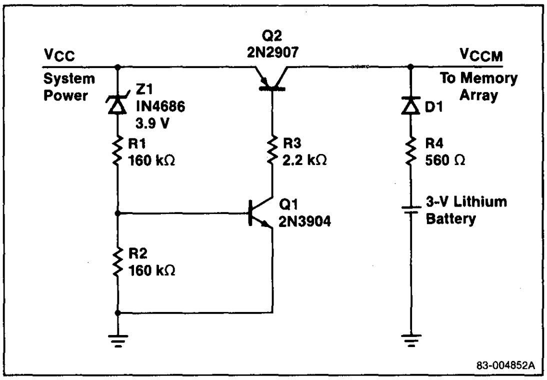


Figure 13. Voltage-Level Detector Circuit



The voltage-level detector circuit consists of zener diode Z1, switching transistor Q1, and the R1 and R2 voltage-divider network. The collector of Q1 is connected to the base of PNP isolation transistor Q2, isolating V_{CC} from V_{CCM} when the V_{CC} voltage level falls below threshold. Threshold voltage (V_{TH}) is determined by $V_{TH} = V_Z + V_{BE1}$, where V_Z is zener voltage and V_{BE1} is the base-to-emitter voltage drop of Q1. The threshold voltage in figure 13 is 3.9 + 0.6 V = 4.5 V, which is the specification for minimum V_{CC}. When V_{CC} drops below minimum specification, the zener diode operates in its forward-voltage region, and no base current flows into Q1. Q1 is then forced into cutoff. With Q1 in cutoff, no base current flows into Q2, consequently forcing Q2 into cutoff and isolating V_{CC} from V_{CCM}.

Isolation transistor Q2 must be capable of supplying a maximum memory operating current of 140 mA and also must provide a minimum V_{SAT} to reduce voltage skew. The PNP 2N2907 medium-power transistor chosen for this application can drive up to 150 mA with a dc gain range of 100 to 300. The maximum base current needed to turn on Q2 is calculated as follows:

$I_{BQ2} = I_{CQ2} \div h_{fe} = 140 \text{ mA} \div 100 = 1.4 \text{ mA}$

Since the base of Q2 is connected to the collector of Q1, and $I_{BQ2} = I_{CQ1}$, Q1 must be capable of driving a collector current of 1.4 mA or greater. The choice for Q1 is an NPN 2N3904, a general-purpose transistor with an I_C maximum of 10 mA and an h_{fe} of 100. The base current needed to turn on Q1 is calculated at 3 mA ÷ 100 = 30 μA, which is much less than the maximum I_{BQ1} provided by the R1-R2 network. The voltage divider R1-R2 must also forward-bias the base-emitter junction of Q1 to allow the transistor to operate in its active region. The voltage at the Q1 base node is 4.1 volts, which keeps Q1 turned on until threshold voltage is reached.

The circuit in figure 13 was characterized, and the relationship between the input and output voltage for two output loads is shown in figure 14. At an input voltage level of 4.5 V, the output voltage maintains a voltage level higher than the minimum data retention voltage of 2 V.

Schmitt Trigger Voltage-Level Detector. The voltage-level detector circuit is an improvement over the diode isolation circuit. However, the threshold point is sensitive to variations in Q1 gain, and could cause oscillations around the trigger point, draining the backup battery. The circuit shown in figure 15 reduces threshold sensitivity by adding an operational amplifier, thereby improving threshold margin by introducing hysteresis into the threshold region. This comparator circuit is commonly referred to as a Schmitt trigger.

Figure 14. Voltage-Level Detector/Transfer Function

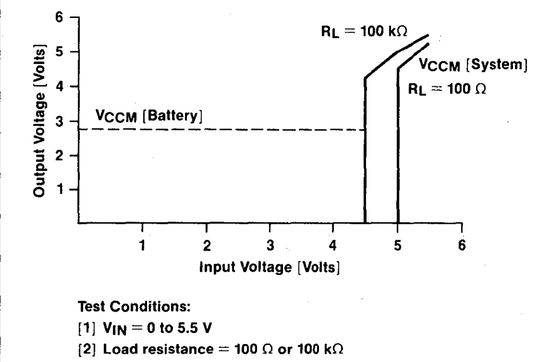
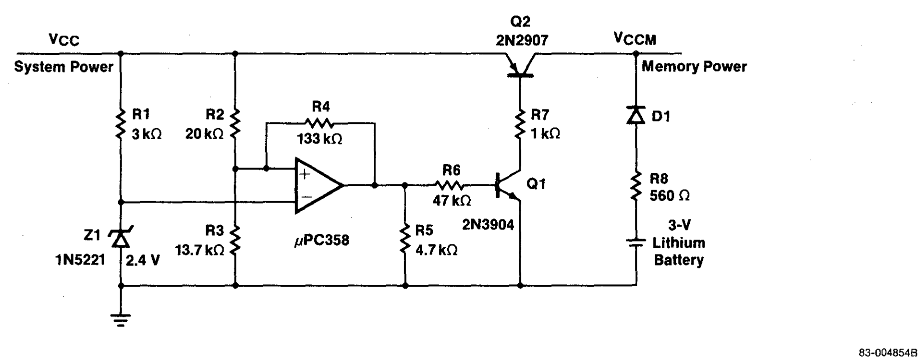


Figure 15. Schmitt Trigger Voltage-Level Detector Circuit



The noninverting input of the μPC358 is connected to a reference-voltage network consisting of R4 and R5. This reference voltage, when compared to the input voltage on the inverting input, determines when the output of the operational amplifier will transition. If a loop gain in excess of unity is chosen, the output waveform continues to be virtually discontinuous at the comparison voltage. However, at this point, the circuit would exhibit a phenomenom called hysteresis. Hysteresis voltage is determined by the resistor network of R4 and R5.

Figure 16 illustrates the response of the Schmitt trigger voltage-level detector circuit to the input signals connected to the noninverting input of the μPC358. When the input voltage reaches the value V1, the output goes high, and when the input is at V2, the output transitions to the low state. The difference between the input signals (V1 − V2) is called the hysteresis voltage (V_H). Therefore, the threshold voltage is dependent upon two input values, increasing the threshold sensitivity by the difference between the two voltages. For the circuit in figure 15, V_H is equal to 0.34 V. This circuit provides the best response of the three backup circuits, but at a cost of increased device count.

The circuit in figure 15 was characterized, and the relationship between input voltage and output voltage for a 100-kΩ output load is shown in figure 17. When the input voltage reaches 4.5 V (V1), the output voltage is set at a level higher than the minimum data retention voltage. Output voltage does not change until input voltage reaches a value of 4.1 V (V2).

System Power Failure Design Considerations

As shown in figure 18, V_{CC} decays slowly after power failure, providing time for an orderly system shutdown. Even during an orderly shutdown, the system may generate spurious memory commands, causing viable data to be overwritten. The designer can use the status signal generated by the system's power supply monitor circuit to protect the memory from false CPU commands after power failure. (The power supply monitor circuit is shown as part of the memory battery backup system in figure 4.)

Figure 16. Response of the Schmitt Trigger to an Arbitrary Signal

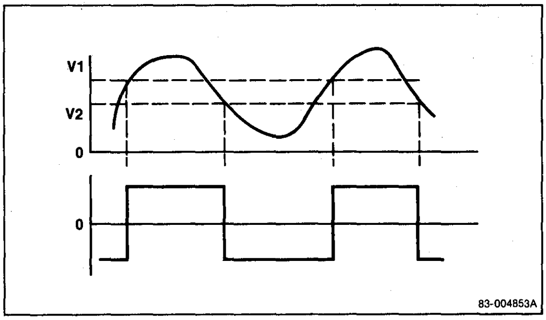


Figure 17. Schmitt Trigger Detector/Transfer Function

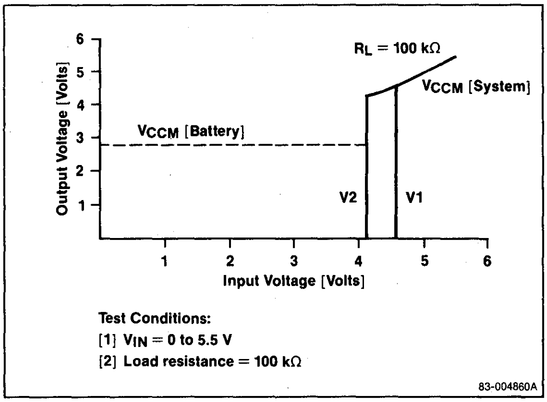
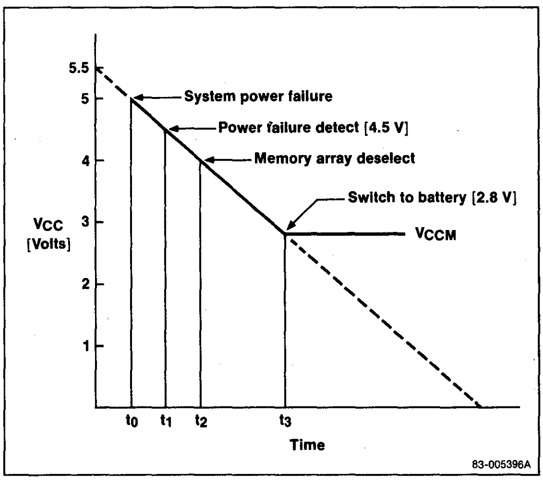


Figure 18. Power Failure V_{CC} Profile



BATTERY BACKUP CIRCUITS FOR SRAMs

The power supply status signal generates a nonmaskable interrupt to the CPU, initiating an orderly system shutdown. This status signal also is sent to the NAND gate of the memory circuit ("Power OK" in figure 19). The memory circuit "ands" this status signal with the other control signals and deselects the memory array before any false commands are generated.

Once the backup circuit has taken over and the memory array has been deselected, $\overline{CS}$ must be maintained at $V_{CC} - 0.2$ V. The power supply status signal (Power OK) must remain low during the entire time V_{CC} is off to force the output of the NAND gate to remain high. The 1 kΩ resistor ensures that the requirement for $\overline{CS} \geq V_{CCM} - 0.2$ V is met.

If a power supply monitor circuit is not provided, the designer may design one. The circuit shown in figure 20 uses a voltage-level detector design to detect when V_{CC} falls below 4.5 V. This circuit is similar to the voltage-level detector circuit used in the battery backup design example. Rather than control an isolation transistor, this power supply monitor circuit generates a power supply status signal (Power OK) to the memory select logic. Threshold voltage is determined by the zener diode and base-emitter voltage drop.

The circuit shown in figure 20 is subject to oscillations due to variations in Q1 gain and limited threshold margins. The addition of a Schmitt trigger to the power supply monitor circuit (figure 21) increases threshold margins by introducing hysteresis into the threshold region. The amount of hysteresis is determined by the values of R4 and R5. When input voltage falls below 4.5 V, the circuit generates a low signal (Power OK) to the memory select logic, and the memory array is deselected. Power OK remains low, because R5 pulls it down as long as V_{CC} is off.

Figure 19. Memory Array Deselect Circuit

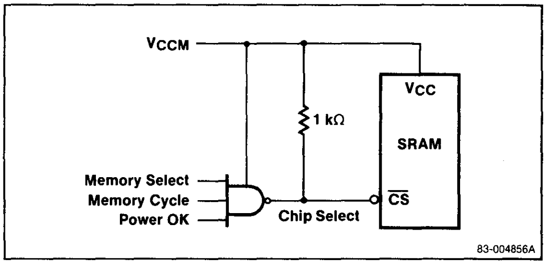


Figure 20. Power Supply Monitor Circuit

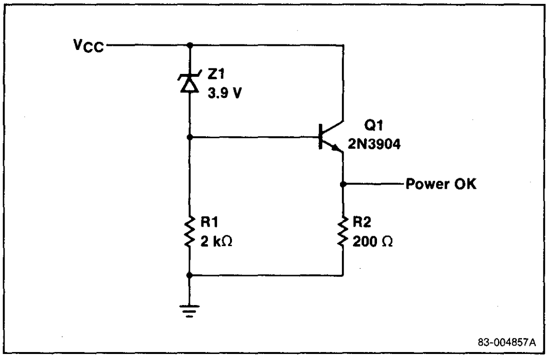
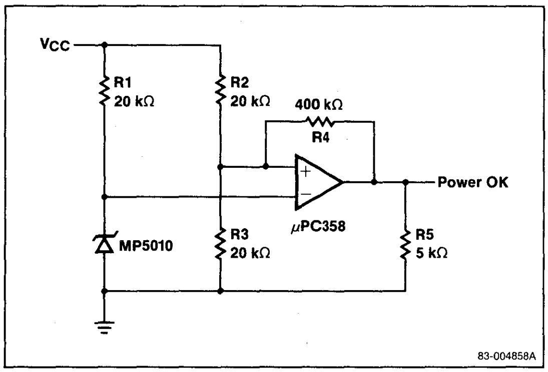


Figure 21. Power Supply Monitor Circuit With Schmitt Trigger



6

NEC

ECL RAMs

7

NEC

Section 7
ECL RAMs

NEC
NEC Electronics Inc.

μPB10422 256 x 4-BIT 10K ECL RAM

Description

The μPB10422 is a very high-speed 10K interface ECL RAM. It is organized as 256 words by 4 bits with noninverted, open-emitter outputs and low power consumption. Two fast access time versions are available: 7 ns max and 10 ns max.

Features

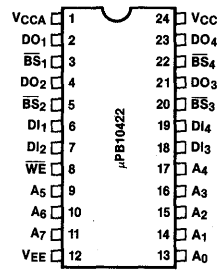
- ☐ 256-word x 4-bit organization
- ☐ 10K interface ECL
- ☐ Noninverted, open-emitter output
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in a 24-pin ceramic DIP

Ordering Information

Part Number	Access Time (max)	Supply Current (min)	Package
μPB10422D-7	7 ns	−220 mA	24-pin ceramic DIP
D-10	10 ns		

Pin Configuration

24-Pin Ceramic DIP

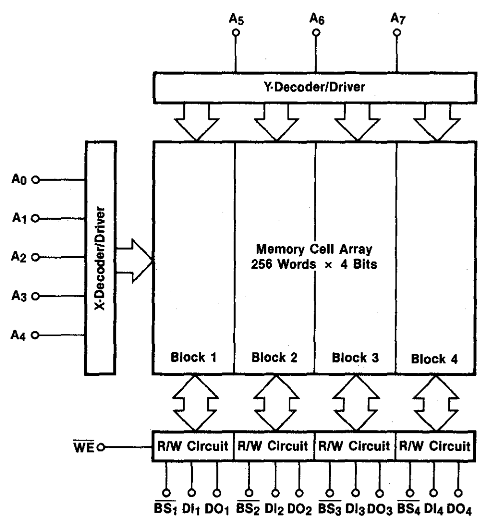


83-003220A

Pin Identification

Symbol	Function
A_0-A_7	Addresses
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{BS}_1$-$\overline{BS}_4$	Block select inputs
$\overline{WE}$	Write enable
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply

Block Diagram



83-003215A

7

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, T_{STG} (bias)	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. Operating conditions should be within the limits specified under DC and AC Characteristics.

DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000	−840	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
		−960	−810	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
		−900	−720	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870	−1665	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
		−1850	−1650	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
		−1830	−1625	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020		mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
		−980		mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
		−920		mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}		−1645	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
			−1630	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
			−1605	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145	−840	mV	For all inputs: T_A = 0°C
		−1105	−810	mV	For all inputs: T_A = 25°C
		−1045	−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870	−1490	mV	For all inputs: T_A = 0°C
		−1850	−1475	mV	For all inputs: T_A = 25°C
		−1830	−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}		220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5	170	μA	$\overline{BS}_1$-$\overline{BS}_4$; $V_{IN} = V_{IL}$ min
		−50		μA	All others: $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220		mA	All inputs and outputs open

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Capacitance

Parameter	Symbol	µPB10422-7 Typ	µPB10422-7 Max	µPB10422-10 Typ	µPB10422-10 Max	Unit
Input capacitance	C_{IN}	4		4		pF
Output capacitance	C_{OUT}	5		5		pF

AC Characteristics

$T_A = 0$ to $+75\,°C$; $V_{EE} = -5.2\ V \pm 5\%$; output load $= 50\ \Omega$ to $-2\ V$

Parameter	Symbol	µPB10422-7 Min	µPB10422-7 Typ	µPB10422-7 Max	µPB10422-10 Min	µPB10422-10 Typ	µPB10422-10 Max	Unit
Read Mode								
Block select access time	t_{ABS}			5			5	ns
Block select recovery time	t_{RBS}			5			5	ns
Address access time	t_{AA}			7			10	ns
Write Mode								
Write pulse width	t_W	5			6			ns
Data setup time	t_{WSD}	1			2			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	1			2			ns
Address hold time	t_{WHA}	1			2			ns
Block select setup time	t_{WSBS}	1			2			ns
Block select hold time	t_{WHBS}	1			2			ns
Write disable time	t_{WS}			5			5	ns
Write recovery time	t_{WR}			6			9	ns
Output Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

(3) See figures 1 and 2.

Figure 1. Loading Conditions Test Circuit

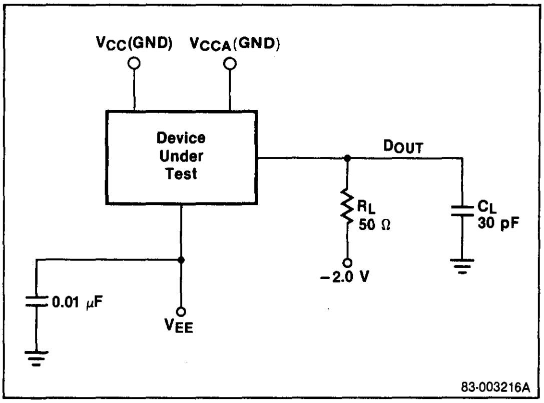
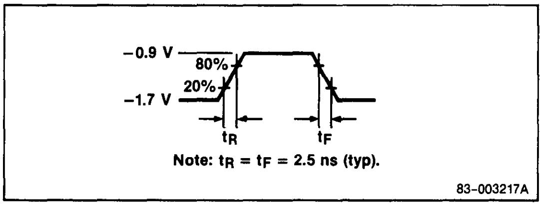


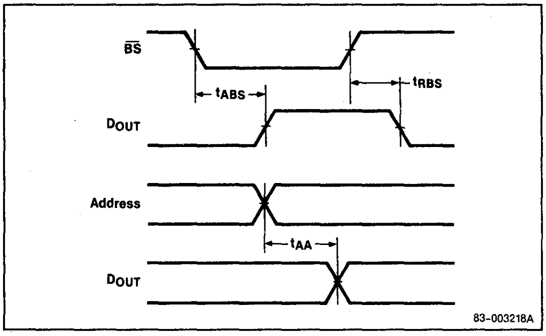
Figure 2. Input Pulse



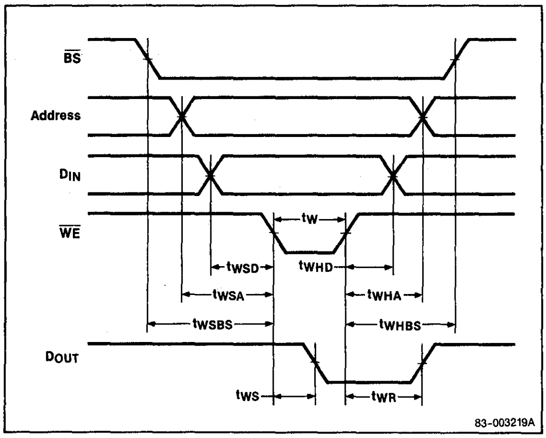
7

Timing Waveforms

Read Mode



Write Mode



NEC

NEC Electronics Inc.

μPB10470 4,096 x 1-BIT 10K ECL RAM

Description

The μPB10470 is a very high-speed 10K interface ECL random access memory. The device is organized as 4K words by 1 bit, with an open emitter output (noninverted) and low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB10470 is available in a hermetic, 300-mil, 18-pin ceramic DIP.

Features

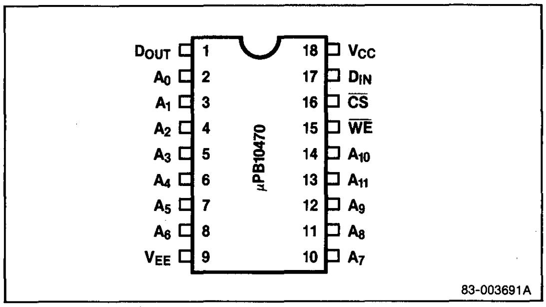
- ☐ 4K-word x 1-bit organization
- ☐ 10K ECL interface
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ 300-mil, 18-pin ceramic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10470D-10	10 ns	18-pin ceramic DIP
D-15	15 ns	

Pin Configuration

18-Pin Ceramic DIP



Pin Identification

Symbol	Function
A_0-A_{11}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	–5.2-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (bias)	–55 to +125°C

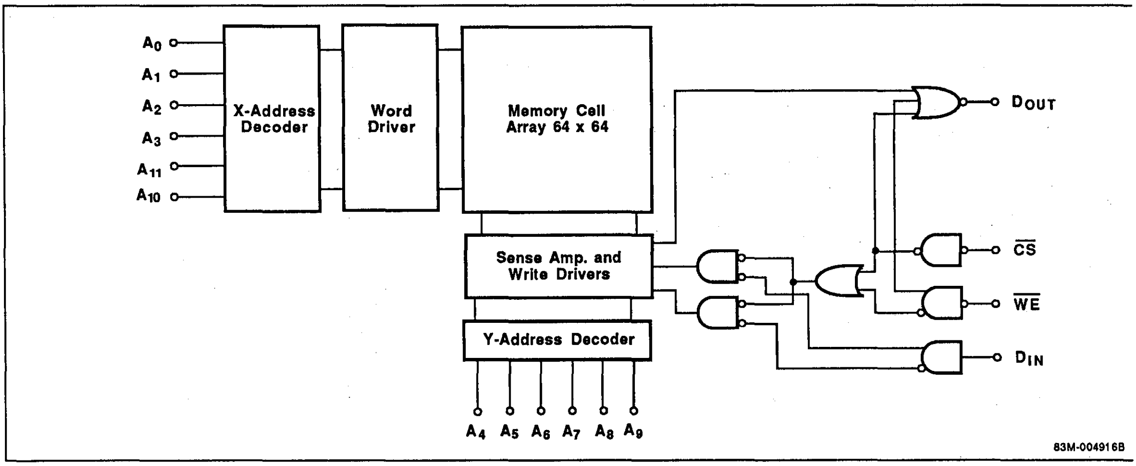
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

7

Block Diagram



DC Characteristics

$T_A = 0$ to $+75$°C; $V_{EE} = -5.2$ V; output load = 50 Ω to −2.0 V

Parameter	Symbol	T_A (°C)	Limits Min	Limits Max	Unit	Test Conditions
Output voltage, high	V_{OH}	0	−1000	−840	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
		+25	−960	−810	mV	
		+75	−900	−720	mV	
Output voltage, low	V_{OL}	0	−1870	−1665	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
		+25	−1850	−1650	mV	
		+75	−1830	−1625	mV	
Output threshold voltage, high	V_{OHC}	0	−1020		mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
		+25	−980		mV	
		+75	−920		mV	
Output threshold voltage, low	V_{OLC}	0		−1645	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
		+25		−1630	mV	
		+75		−1605	mV	
Input voltage, high	V_{IH}	0	−1145	−840	mV	Guaranteed input voltage high for all inputs
		+25	−1105	−810	mV	
		+75	−1045	−720	mV	
Input voltage, low	V_{IL}	0	−1870	−1490	mV	Guaranteed input voltage low for all inputs
		+25	−1850	−1475	mV	
		+75	−1830	−1450	mV	
Input current, high	I_{IH}	0 to +75		220	μA	$V_{IN} = V_{IH}$ (max)
Input current, low	I_{IL}	0 to +75	0.5	170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ (min)
		0 to +75	−50		μA	For all others: $V_{IN} = V_{IL}$ (min)
Supply current	I_{EE}	0 to +75	−220		mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

$T_A = 0$ to $+75°C$; $V_{EE} = -5.2\ V \pm 5\%$

Parameter	Symbol	μPB10470-10 Min	μPB10470-10 Typ	μPB10470-10 Max	μPB10470-15 Min	μPB10470-15 Typ	μPB10470-15 Max	Unit
Read Mode								
Address access time	t_{AA}			10			15	ns
Chip select access time	t_{ACS}			6			8	ns
Chip select recovery time	t_{RCS}			6			8	ns
Write Mode								
Write pulse width	t_W	10			15			ns
Data setup time	t_{WSD}	2			2			ns
Data hold time	t_{WHD}	2			2			ns
Address setup time	t_{WSA}	3			3			ns
Address hold time	t_{WHA}	2			2			ns
Chip select setup time	t_{WSCS}	2			2			ns
Chip select hold time	t_{WHCS}	2			2			ns
Write disable time	t_{WS}			6			8	ns
Write recovery time	t_{WR}			10			10	ns
Output Rise and Fall Times								
Rise time	t_R		2			2		ns
Fall time	t_F		2			2		ns

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Mode	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care

Figure 1. Loading Conditions Test Circuit

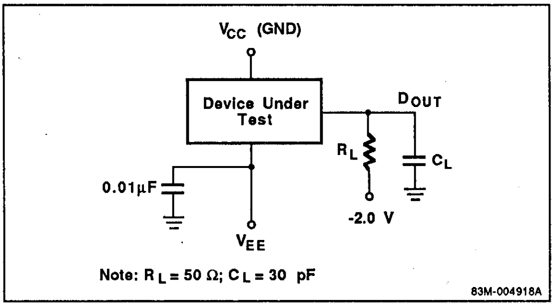
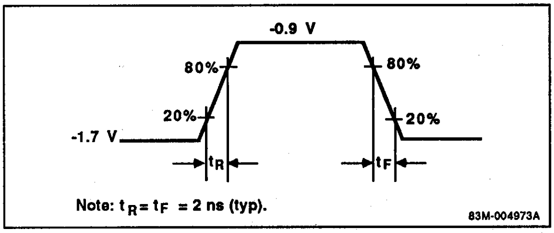
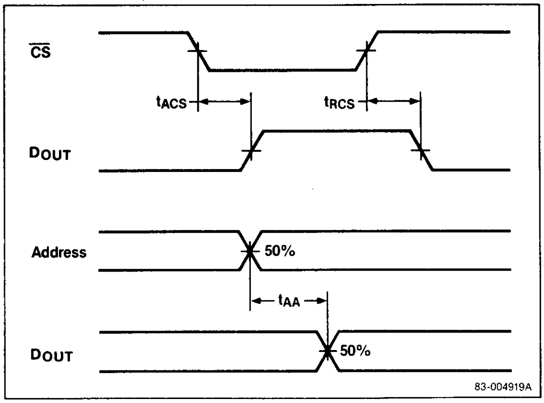


Figure 2. Input Pulse Waveform for Test

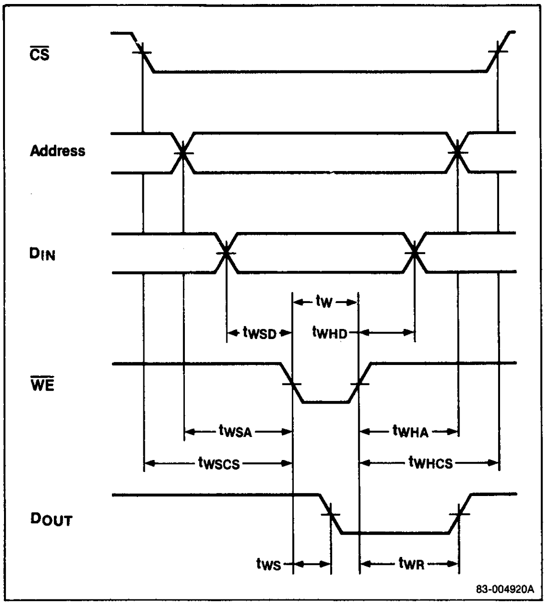


Timing Waveforms

Read Mode



Write Mode



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NEC

NEC Electronics Inc.

μPB10474
1,024 x 4-BIT
10K ECL RAM

Description

The μPB10474 is a very high-speed, 10K interface ECL RAM. It is organized as 1,024 words by 4 bits with noninverted, open-emitter outputs and low power consumption. Three access time versions are available: 8 ns max, 10 ns max, and 15 ns max. The μPB10474 is available in a hermetic, 400-mil, 24-pin ceramic DIP.

Features

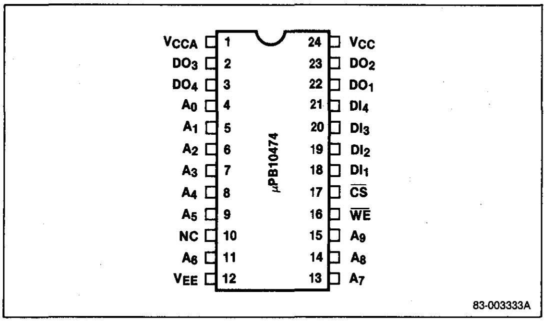
- ☐ 1,024-word x 4-bit organization
- ☐ 10K ECL interface
- ☐ Noninverted, open-emitter outputs
- ☐ Fast access times
- ☐ Low power consumption
- ☐ 400-mil, 24-pin ceramic DIP

Ordering Information

Part Number	Access Time (max)	Package
μPB10474D-8	8 ns	24-pin ceramic DIP
D-10	10 ns	
D-15	15 ns	

Pin Configuration

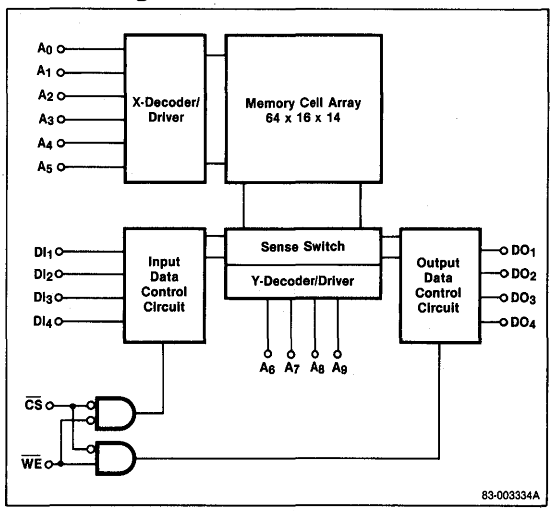
24-Pin Ceramic DIP



Pin Identification

Symbol	Function
A_0-A_9	Addresses
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG} Under bias, $T_{STG\,(bias)}$	−65 to +150°C −55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_{IN}		4		pF	f = 1 MHz
Output capacitance	C_{OUT}		5		pF	f = 1 MHz

DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2 V

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Output voltage, high	V_{OH}	−1000		−840	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
	V_{OH}	−960		−810	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
	V_{OH}	−900		−720	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
	V_{OL}	−1850		−1650	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
	V_{OL}	−1830		−1625	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
	V_{OHC}	−980			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
	V_{OHC}	−920			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
	V_{OLC}			−1630	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
	V_{OLC}			−1605	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
	V_{IH}	−1105		−810	mV	For all inputs: T_A = 25°C
	V_{IH}	−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
	V_{IL}	−1850		−1475	mV	For all inputs: T_A = 25°C
	V_{IL}	−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ min
	I_{IL}	−50			μA	For all others: $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

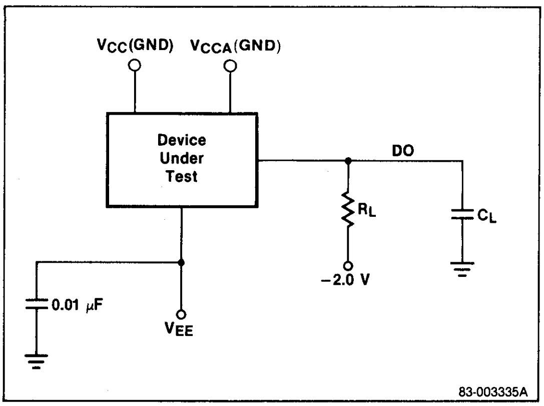
T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2 V

		Limits									
		μPB10474-8			μPB10474-10			μPB10474-15			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Read Mode											
Chip select access time	t_{ACS}			5			6			8	ns
Chip select recovery time	t_{RCS}			5			6			8	ns
Address access time	t_{AA}			8			10			15	ns
Write Mode											
Write pulse width	t_W	6			10			15			ns
Data setup time	t_{WSD}	1			2			2			ns
Data hold time	t_{WHD}	1			2			2			ns
Address setup time	t_{WSA}	1			3			3			ns
Address hold time	t_{WHA}	1			2			2			ns
Chip select setup time	t_{WSCS}	1			2			2			ns
Chip select hold time	t_{WHCS}	1			2			2			ns
Write disable time	t_{WS}			5			6			8	ns
Write recovery time	t_{WR}			8			10			10	ns
Output Rise and Fall Times											
Output rise time	t_R		2			2			2		ns
Output fall time	t_F		2			2			2		ns

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

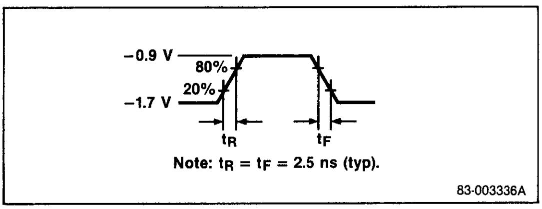
Figure 1. Loading Conditions Test Circuit



Truth Table

Input				
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Figure 2. Input Pulse



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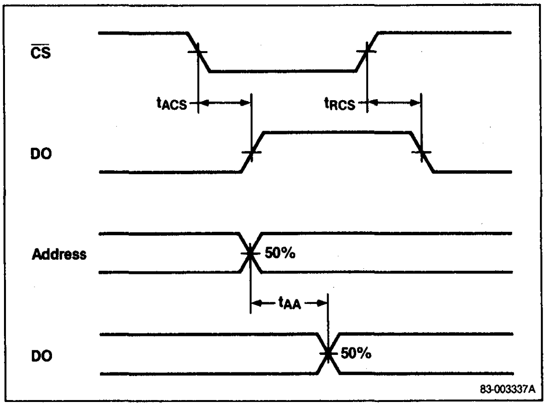
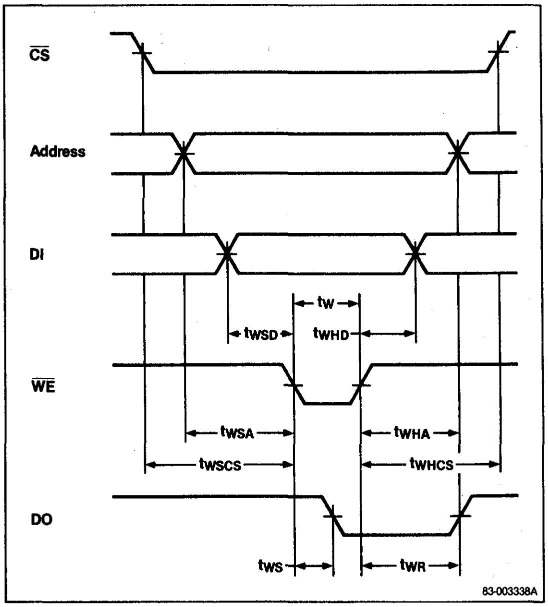
Timing Waveforms

Read Mode



Write Mode



NEC

NEC Electronics Inc.

μPB10474A
1,024 x 4-BIT
10K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB10474A is a very high-speed 10K interface ECL RAM. It is organized as 1,024 words by 4 bits with noninverted, open emitter outputs and low power consumption. Two access time versions are available: 5 ns maximum and 7 ns maximum. The device is packaged in a hermetic, 400-mil, 24-pin cerdip.

Features

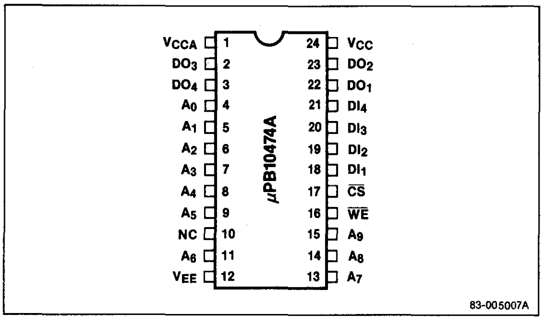
- ☐ 1,024-word x 4-bit organization
- ☐ 10K ECL interface
- ☐ Noninverted, open-emitter outputs
- ☐ Fast access times
- ☐ Low power consumption
- ☐ 400-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10474AD-5	5 ns	24-pin cerdip
AD-7	7 ns	

Pin Configuration

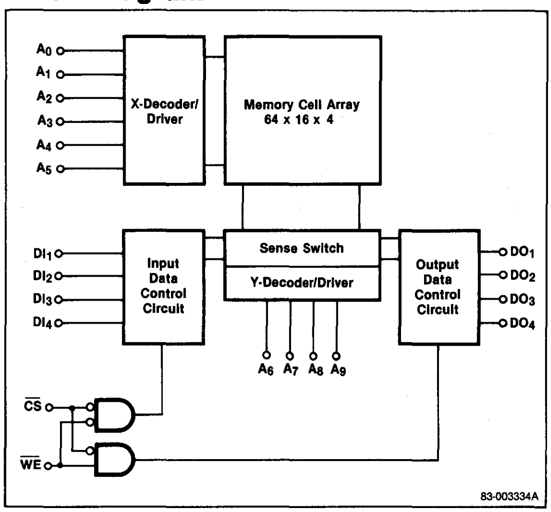
24-Pin Cerdip



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{WE}$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	−5.2-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, T_{STG} (Bias)	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	
Output capacitance	C_{OUT}		5		pF	

DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min); T_A = 0°C
		−960		−810	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min); T_A = 25°C
		−900		−720	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min); T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min); T_A = 0°C
		−1850		−1650	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min); T_A = 25°C
		−1830		−1625	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min); T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max); T_A = 0°C
		−980			mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max); T_A = 25°C
		−920			mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max); T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max); T_A = 0°C
				−1630	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max); T_A = 25°C
				−1605	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max); T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ (min)
		−50			μA	For all others: $V_{IN} = V_{IL}$ (min)
Supply current	I_{EE}	−250			mA	All inputs and outputs open

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75 °C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2.0 V; $V_{CC} = V_{CCA}$ = 0 V

		Limits						
		μPB10474A-5			μPB10474A-7			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Read Mode								
Address access time	t_{AA}			5			7	ns
Chip select access time	t_{ACS}			3			5	ns
Chip select recovery time	t_{RCS}			3			5	ns
Write Mode								
Write pulse width	t_W	5			7			ns
Data setup time	t_{WSD}	1			1			ns
Data hold time	t_{WHD}	1			1			ns
Address setup time	t_{WSA}	1			1			ns
Address hold time	t_{WHA}	1			1			ns
Chip select setup time	t_{WSCS}	1			1			ns
Chip select hold time	t_{WHCS}	1			1			ns
Write disable time	t_{WS}			3			5	ns
Write recovery time	t_{WR}			6			8	ns
Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

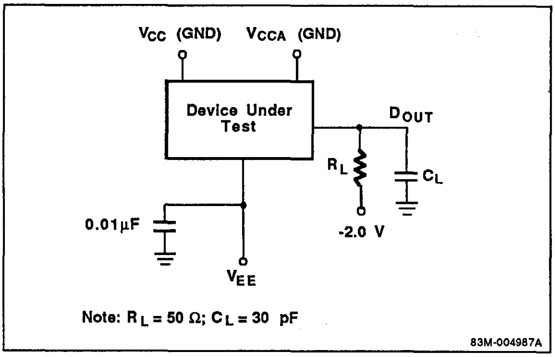
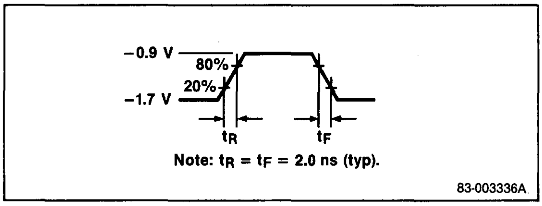


Figure 2. Input Pulse



Truth Table

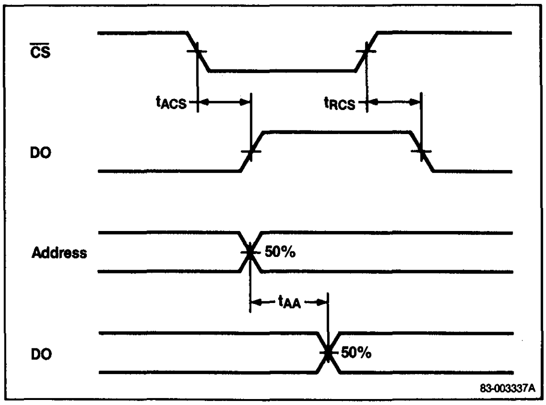
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

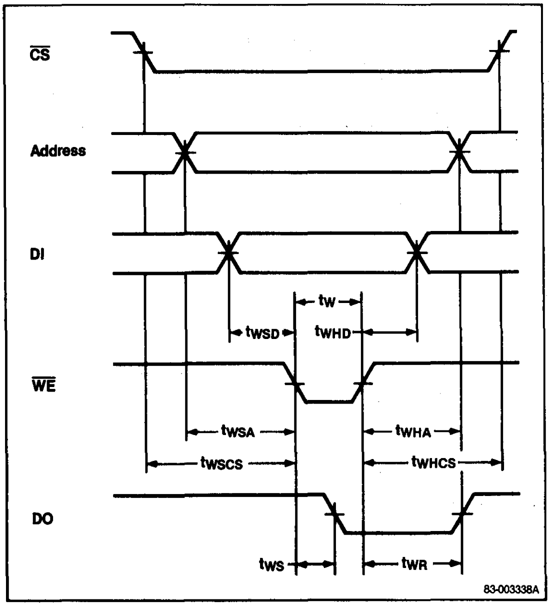
(1) X = don't care.

Timing Waveforms

Read Mode



Write Mode



NEC
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μPB10480
16,384 x 1-BIT
10K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB10480 is a very high-speed 10K interface ECL RAM. The device is organized as 16,384 words by 1 bit, with an open emitter output (noninverted) and low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB10480 is available in a hermetic, 300-mil, 20-pin cerdip or 20-pin ceramic flatpack.

Features

- ☐ 16,384-word x 1-bit organization
- ☐ 10K ECL interface
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPB10480D-10	10 ns	1.4 W	20-pin cerdip
D-15	15 ns	1.3 W	
μPB10480B-10	10 ns	1.4 W	20-pin ceramic flatpack
B-15	15 ns	1.3 W	

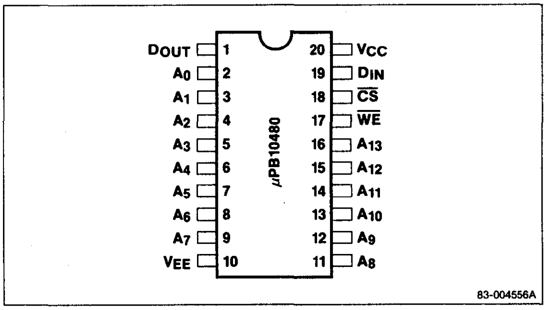
Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

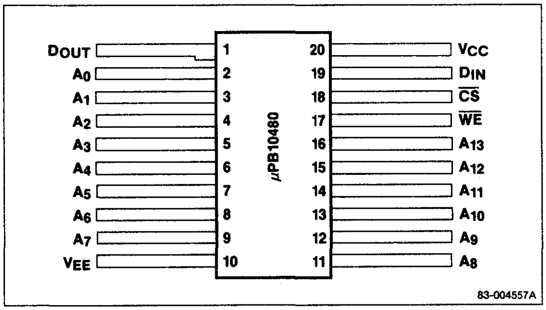
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configurations

20-Pin Cerdip



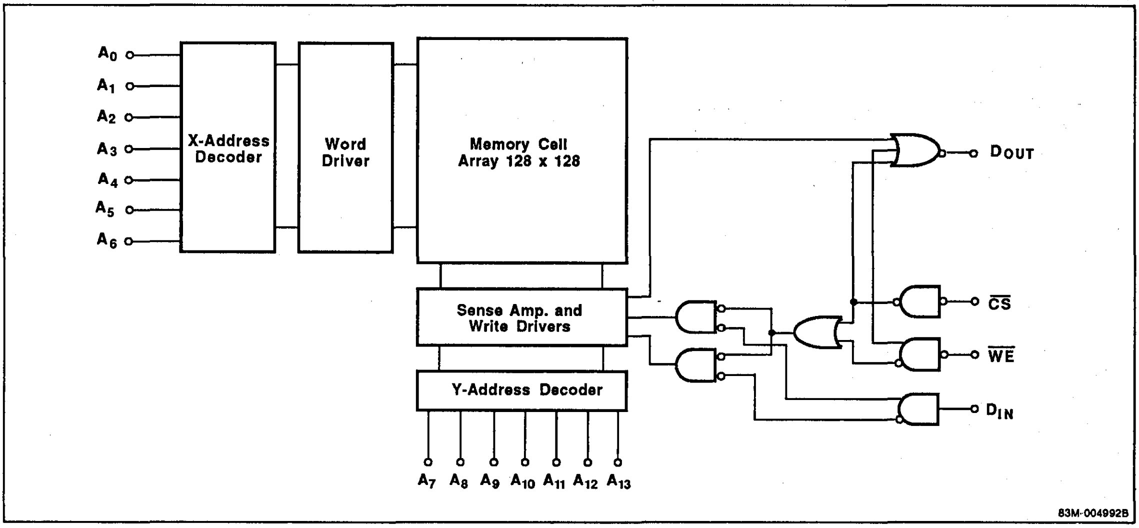
20-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0-A_{13}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−5.2-volt power supply

Block Diagram



Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Mode	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care

Capacitance

		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Figure 1. Loading Conditions Test Circuit

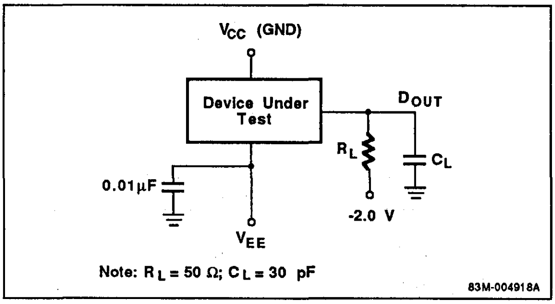
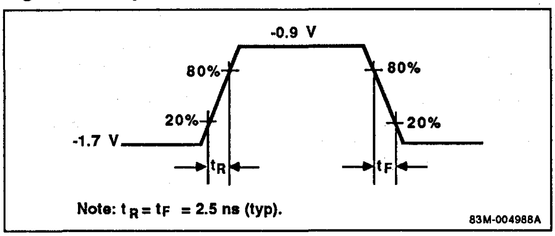


Figure 2. Input Pulse Waveform for Test



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	T_A (°C)	Limits Min	Limits Max	Unit	Test Conditions
Output voltage, high	V_{OH}	0	−1000	−840	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
		+25	−960	−810	mV	
		+75	−900	−720	mV	
Output voltage, low	V_{OL}	0	−1870	−1665	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
		+25	−1850	−1650	mV	
		+75	−1830	−1625	mV	
Output threshold voltage, high	V_{OHC}	0	−1020		mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
		+25	−980		mV	
		+75	−920		mV	
Output threshold voltage, low	V_{OLC}	0		−1645	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
		+25		−1630	mV	
		+75		−1605	mV	
Input voltage, high	V_{IH}	0	−1145	−840	mV	Guaranteed input voltage high for all inputs
		+25	−1105	−810	mV	
		+75	−1045	−720	mV	
Input voltage, low	V_{IL}	0	−1870	−1490	mV	Guaranteed input voltage low for all inputs
		+25	−1850	−1475	mV	
		+75	−1830	−1450	mV	
Input current, high	I_{IH}	0 to +75		220	μA	$V_{IN} = V_{IH}$ (max)
Input current, low	I_{IL}	0 to +75	0.5	170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ (min)
		0 to +75	−50		μA	For all others: $V_{IN} = V_{IL}$ (min)
Supply current	I_{EE}	0 to +75	−260		mA	For μPB10480-10: all inputs and outputs open
		0 to +75	−240		mA	For μPB10480-15: all inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

$T_A = 0$ to $+85\,°C$; $V_{EE} = -4.5\ V \pm 5\%$

Parameter	Symbol	μPB100480-10 Min	μPB100480-10 Typ	μPB100480-10 Max	μPB100480-15 Min	μPB100480-15 Typ	μPB100480-15 Max	Unit
Read Mode								
Address access time	t_{AA}			10			15	ns
Chip select access time	t_{ACS}			5			8	ns
Chip select recovery time	t_{RCS}			5			8	ns
Write Mode								
Write pulse width	t_W	10			15			ns
Data setup time	t_{WSD}	2			3			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	2			3			ns
Address hold time	t_{WHA}	1			2			ns
Chip select setup time	t_{WSCS}	2			3			ns
Chip select hold time	t_{WHCS}	1			2			ns
Write disable time	t_{WS}			5			8	ns
Write recovery time	t_{WR}			11			17	ns
Output Rise and Fall Times								
Rise time	t_R		2			2		ns
Fall time	t_F		2			2		ns

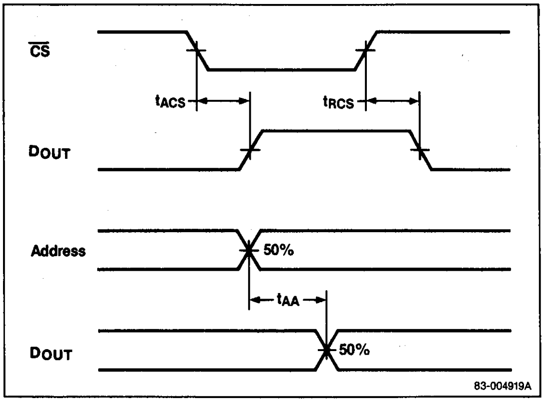
Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

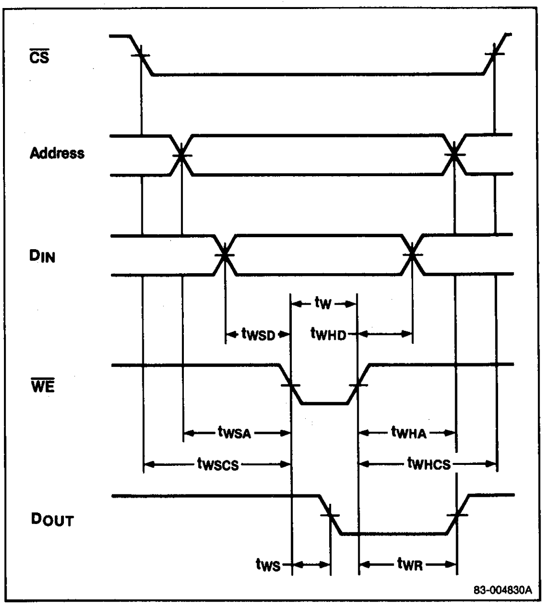
(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference levels = 50%.

Timing Waveforms

Read Mode



Write Mode



NEC
NEC Electronics Inc.

μPB10484
4,096 x 4-BIT
10K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB10484 is a very high-speed 10K interface ECL RAM. It is organized as 4,096 words by 4 bits with noninverted, open-emitter outputs and low power consumption. Two access time versions are available: 10 ns and 15 ns maximum. The μPB10484 is available in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

- ☐ 4,096-word x 4-bit organization
- ☐ 10K ECL interface
- ☐ Noninverted, open-emitter outputs
- ☐ Fast access times: 10 and 15 ns maximum
- ☐ Low power consumption: 1.4 W maximum
- ☐ 400-mil, 28-pin cerdip or 28-pin ceramic flatpack packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10484D-10	10 ns	28-pin cerdip
D-15	15 ns	
μPB10484B-10	10 ns	28-pin ceramic flatpack
B-15	15 ns	

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, $T_{STG\ (bias)}$	−55 to +125°C

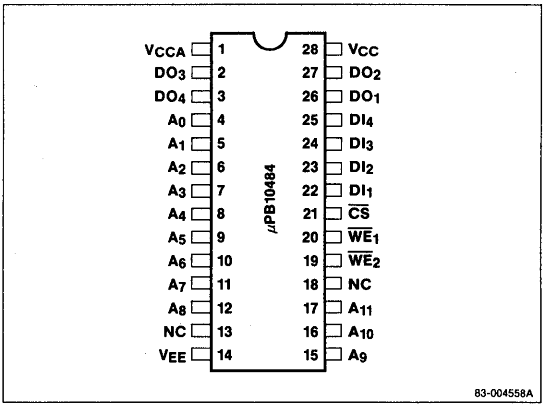
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

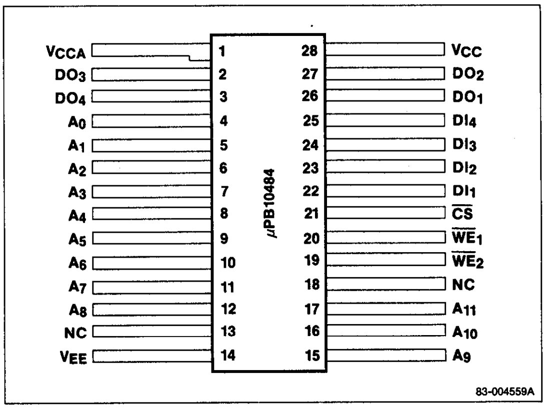
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	f = 1 MHz
Output capacitance	C_{OUT}		6		pF	f = 1 MHz

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0-A_{11}	Address inputs
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	−5.2-volt power supply
NC	No connection

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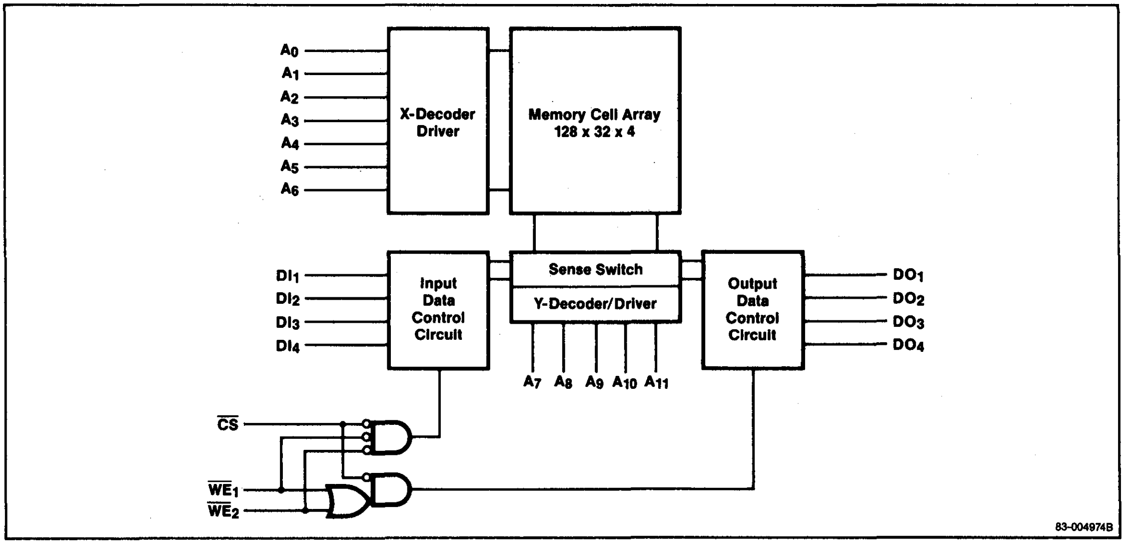
Block Diagram



DC Characteristics

$T_A = 0$ to $+75\,°C$; $V_{EE} = -5.2$ V; output load = 50 Ω to −2 V; $V_{CC} = V_{CCA} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; $T_A = 0\,°C$
		−960		−810	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; $T_A = 25\,°C$
		−900		−720	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; $T_A = 75\,°C$
Output voltage, low	V_{OL}	−1870		−1665	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; $T_A = 0\,°C$
		−1850		−1650	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; $T_A = 25\,°C$
		−1830		−1625	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; $T_A = 75\,°C$
Output threshold voltage, high	V_{OHC}	−1020			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; $T_A = 0\,°C$
		−980			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; $T_A = 25\,°C$
		−920			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; $T_A = 75\,°C$
Output threshold voltage, low	V_{OLC}			−1645	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; $T_A = 0\,°C$
				−1630	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; $T_A = 25\,°C$
				−1605	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; $T_A = 75\,°C$
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: $T_A = 0\,°C$
		−1105		−810	mV	For all inputs: $T_A = 25\,°C$
		−1045		−720	mV	For all inputs: $T_A = 75\,°C$
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: $T_A = 0\,°C$
		−1850		−1475	mV	For all inputs: $T_A = 25\,°C$
		−1830		−1450	mV	For all inputs: $T_A = 75\,°C$
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ min
		−50			μA	For all others: $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−260			mA	For μPB10484-10: all inputs and outputs open
		−240			mA	For μPB10484-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2 V; V_{CC} = V_{CCA} = 0 V

		Limits						
		μPB10484-10			μPB10484-15			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Read Mode								
Address access time	t_{AA}			10			15	ns
Chip select recovery time	t_{RCS}			5			8	ns
Chip select access time	t_{ACS}			5			8	ns
Write Mode								
Write pulse width	t_W	10			15			ns
Data setup time	t_{WSD}	2			3			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	2			3			ns
Address hold time	t_{WHA}	1			2			ns
Chip select setup time	t_{WSCS}	2			3			ns
Chip select hold time	t_{WHCS}	1			2			ns
Write disable time	t_{WS}			5			8	ns
Write recovery time	t_{WR}			11			17	ns
Output Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference level = 50%.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$, and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Figure 1. Loading Conditions Test Circuit

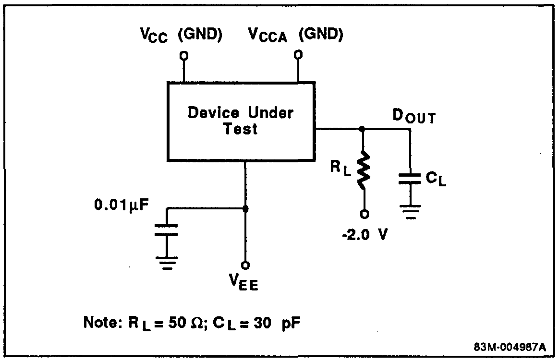
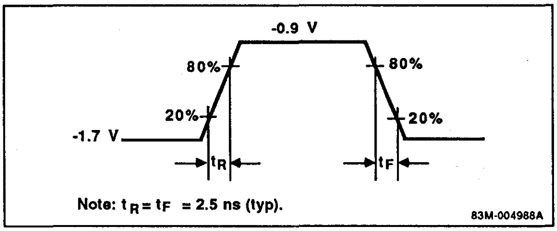
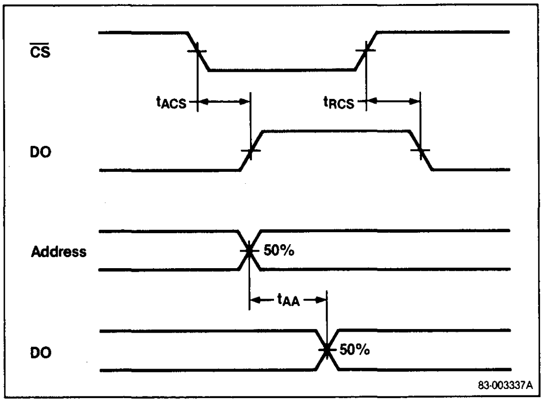


Figure 2. Input Pulse Waveform for Test

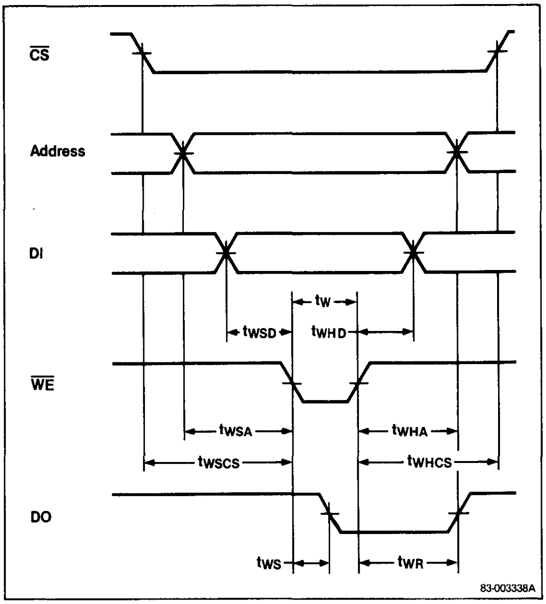


Timing Waveforms

Read Mode



Write Mode



7

NEC

NEC Electronics Inc.

μPB100422 256 x 4-BIT 100K ECL RAM

Description

The μPB100422 is a very high-speed, 100K interface ECL RAM. It is organized as 256 words by 4 bits with noninverted, open-emitter outputs and low power consumption. Two fast access time versions are available: 7 ns max and 10 ns max.

Features

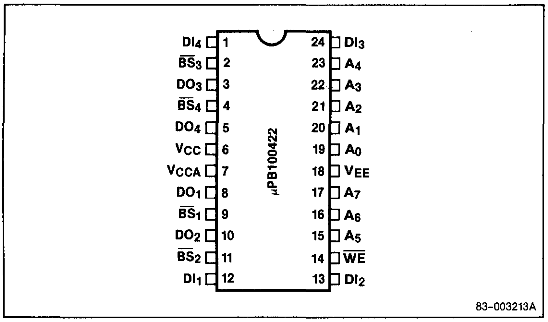
- ☐ 256-word x 4-bit organization
- ☐ 100K ECL interface
- ☐ Noninverted, open-emitter output
- ☐ Fast access times
- ☐ Low power consumption
- ☐ Available in a 24-pin, 400-mil ceramic DIP or a 24-pin ceramic flatpack

Ordering Information

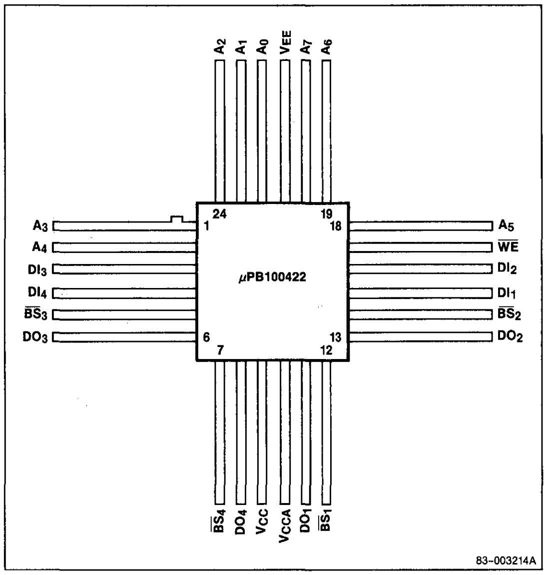
Part Number	Supply Current (min)	Access Time (max)	Package
μPB100422D-7	7 ns	−220 mA	24-pin ceramic DIP
D-10	10 ns		
B-7	7 ns	−220 mA	24-pin ceramic flatpack
B-10	10 ns		

Pin Configurations

24-Pin Ceramic DIP



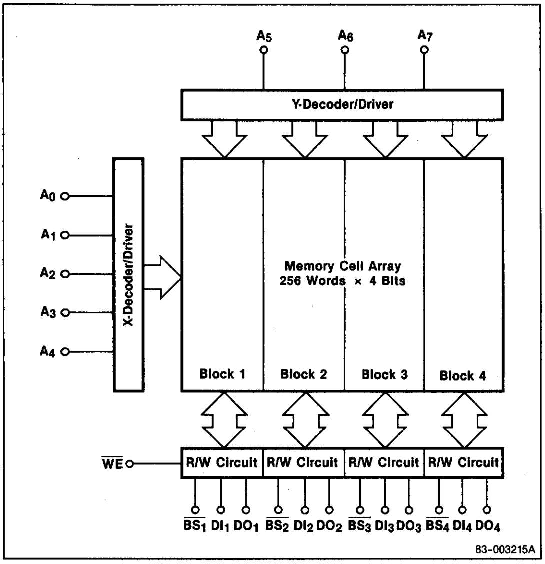
24-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0-A_7	Addresses
$\overline{BS}_1$-$\overline{BS}_4$	Block select inputs
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{WE}$	Write enable
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, $T_{STG\ (bias)}$	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

		Limits						
		μPB100422-7			μPB100422-10			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4			4		pF
Output capacitance	C_{OUT}		5			5		pF

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	For all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	For all inputs
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	$\overline{BS}_1$-$\overline{BS}_4$, $V_{IN} = V_{IL}$ min
	I_{IL}	−50			μA	All others, $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%

		Limits						
		μPB100422-7			μPB100422-10			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Read Mode								
Block select access time	t_{ABS}			5			5	ns
Block select recovery time	t_{RBS}			5			5	ns
Address access time	t_{AA}			7			10	ns
Write Mode								
Write pulse width	t_W	5			6			ns
Data setup time	t_{WSD}	1			2			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	1			2			ns
Address hold time	t_{WHA}	1			2			ns
Block select setup time	t_{WSBS}	1			2			ns
Block select hold time	t_{WHBS}	1			2			ns
Write Mode (cont)								
Write disable time	t_{WS}			5			5	ns
Write recovery time	t_{WR}			6			9	ns
Output Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

(3) The output load is shown in figure 1.

(4) Input transition times are shown in figure 2.

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Figure 1. Loading Conditions Test Circuit

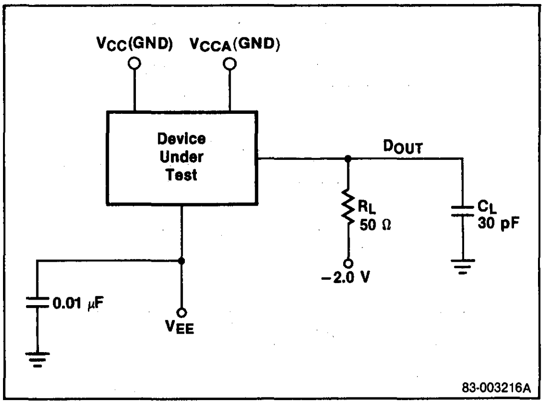
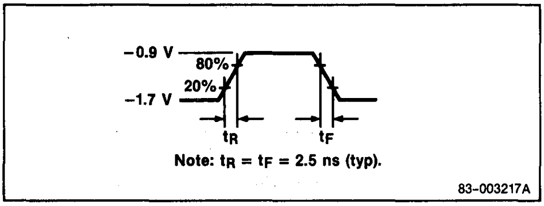
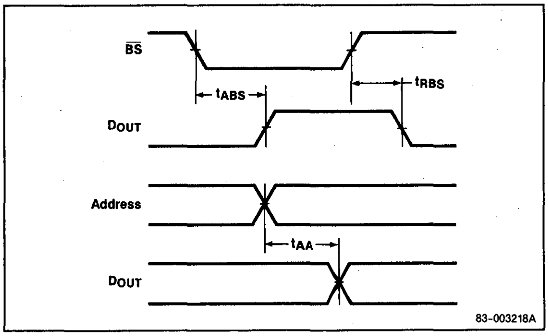


Figure 2. Input Pulse

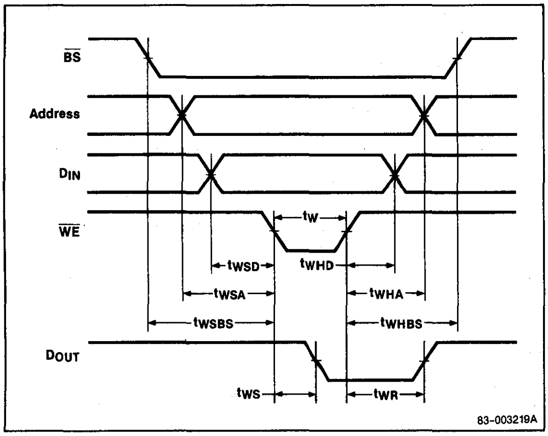


Timing Waveforms

Read Mode



Write Mode



μPB100470 4,096 x 1-BIT 100K ECL RAM

Description

The μPB100470 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 4K words by 1 bit, with an open emitter output (noninverted) and low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB100470 is available in a hermetic, 300-mil, 18-pin ceramic DIP.

Features

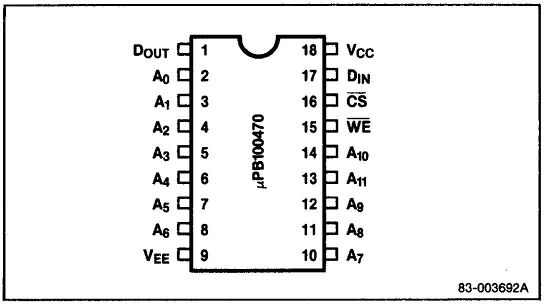
- ☐ 4K-word x 1-bit organization
- ☐ 100K ECL interface with full voltage and temperature compensation
- ☐ Open emitter output (noninverted)
- ☐ Fast access times
- ☐ Low power consumption
- ☐ 300-mil, 18-pin ceramic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB100470D-10	10 ns	18-pin ceramic DIP
D-15	15 ns	

Pin Configuration

18-Pin Ceramic DIP



Pin Identification

Symbol	Function
A_0-A_{11}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	–4.5-volt power supply

Absolute Maximum Ratings

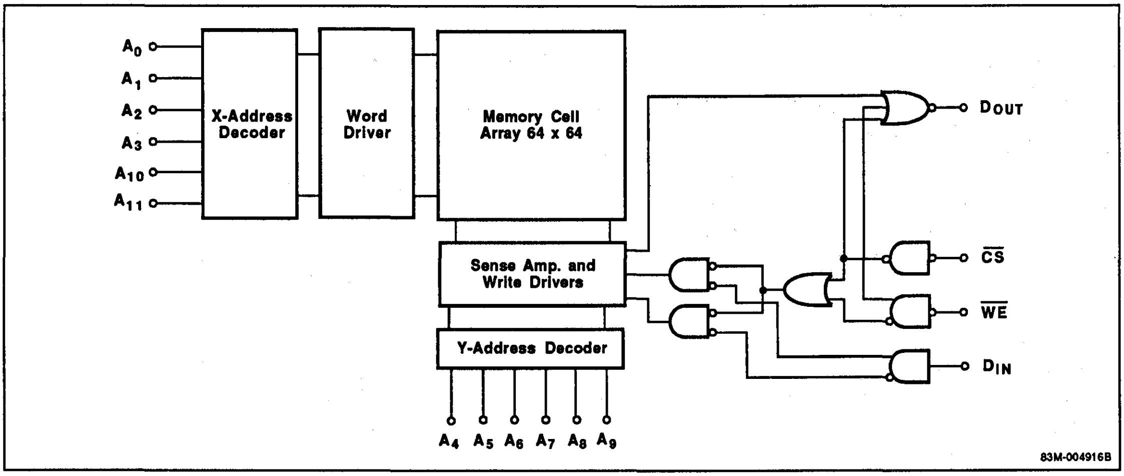
Supply voltage, V_{EE} to V_{CC}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Under bias, T_{STG} (bias)	–55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810	−1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035		mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}		−1610	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	µA	$V_{IN} = V_{IH}$ (max)
Input current, low	I_{IL}	0.5	170	µA	For $\overline{CS}$: $V_{IN} = V_{IL}$ (min)
		−50		µA	For all others: $V_{IN} = V_{IL}$ (min)
Supply current	I_{EE}	−220		mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Mode	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%

Parameter	Symbol	µPB100470-10 Min	Typ	Max	µPB100470-15 Min	Typ	Max	Unit
Read Mode								
Address access time	t_{AA}			10			15	ns
Chip select access time	t_{ACS}			6			8	ns
Chip select recovery time	t_{RCS}			6			8	ns
Write Mode								
Write pulse width	t_W	10			15			ns
Data setup time	t_{WSD}	2			2			ns
Data hold time	t_{WHD}	2			2			ns
Address setup time	t_{WSA}	3			3			ns
Address hold time	t_{WHA}	2			2			ns
Chip select setup time	t_{WSCS}	2			2			ns
Chip select hold time	t_{WHCS}	2			2			ns
Write disable time	t_{WS}			6			8	ns
Write recovery time	t_{WR}			10			10	ns
Output Rise and Fall Times								
Rise time	t_R		2			2		ns
Fall time	t_F		2			2		ns

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

NEC

Figure 1. Loading Conditions Test Circuit

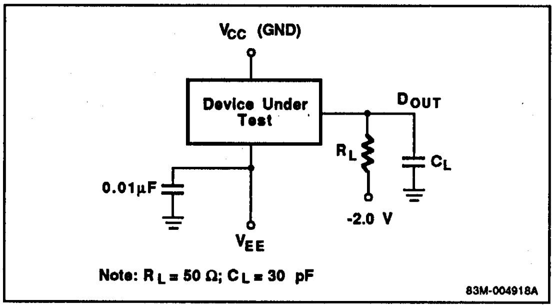
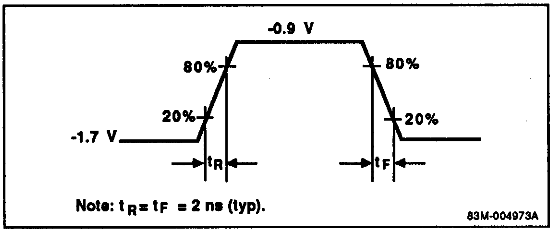
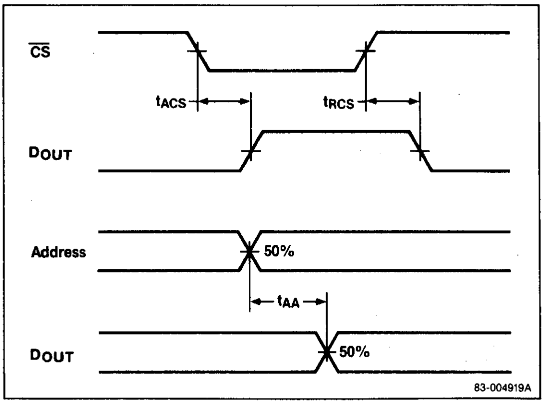


Figure 2. Input Pulse Waveform for Test

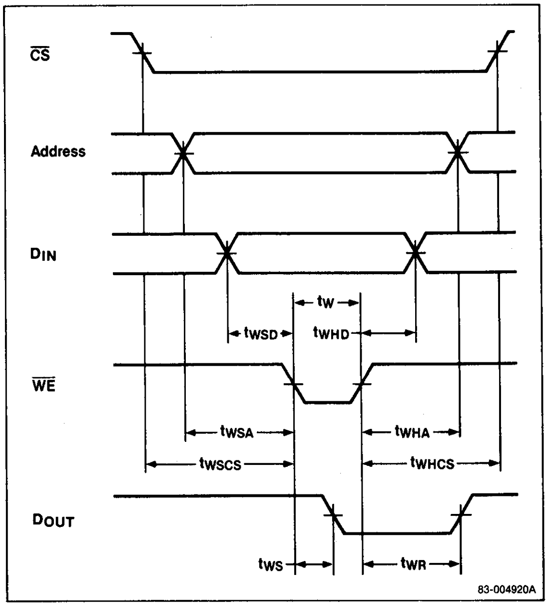


Timing Waveforms

Read Mode



Write Mode



μPB100474 1,024 x 4-BIT 100K ECL RAM

Description

NEC's μPB100474 is a very high-speed ECL 100K interface random access memory. The μPB100474 is organized as 1K words by 4 bits with open-emitter outputs (noninverted). It is available in a 24-pin cerdip, 24-pin ceramic LCC, or 24-pin ceramic flatpack package.

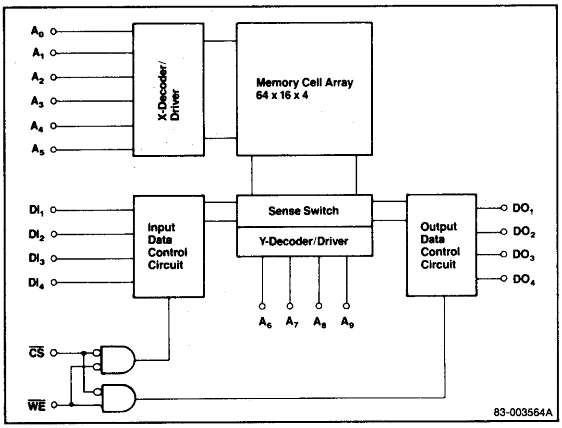
Features

- ☐ 1K-word bx 4-bit organization
- ☐ ECL 100K interface
- ☐ Full voltage and temperature compensation
- ☐ Open emitter outputs (noninverted)
- ☐ Fast access times
- ☐ Available in cerdip, LCC, and flatpack packaging

Ordering Information

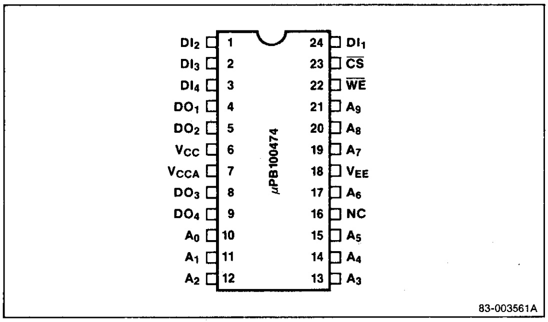
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474B-6	6 ns	−450 mA	24-pin ceramic flatpack
B-8	8 ns	−220 mA	
B-10	10 ns		
B-15	15 ns		
μPB100474D-8	8 ns	−220 mA	24-pin cerdip
D-10	10 ns		
D-15	15 ns		
μPB100474K-4.5	4.5 ns	−450 mA	24-pin ceramic LCC
K-6	6 ns		

Block Diagram

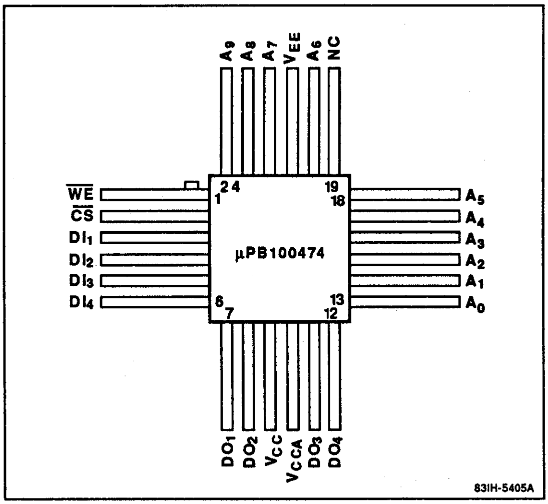


Pin Configurations

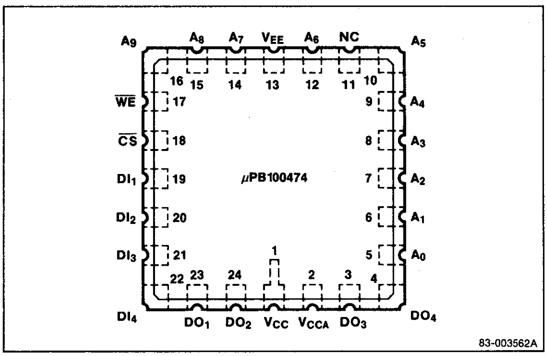
24-Pin Cerdip



24-Pin Ceramic Flatpack



24-Pin Ceramic LCC



NEC

Pin Identification

Symbol	Function
A_0-A_9	Addresses
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	+0.5 to −7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to −30 mA
Storage temperature, T_{STG} Under bias, T_{STG} (Bias)	−65 to +150°C −55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Truth Table

Input				
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Capacitance

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	
Output capacitance	C_{OUT}		5		pF	

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; Output load = 50 Ω to −2 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	$V_{IN} = V_{IH}$ max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	$V_{IN} = V_{IH}$ min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	$\overline{CS}$: $V_{IN} = V_{IL}$ min
		−50			μA	Others: $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220			mA	t_{AA} = 8/10/15 ns; all inputs and outputs open
		−450			mA	t_{AA} = 4.5/6 ns; all inputs and outputs open (Note 2)

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) For the μPB100474-4.5/6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90°C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

Figure 1. Loading Conditions Test Circuit

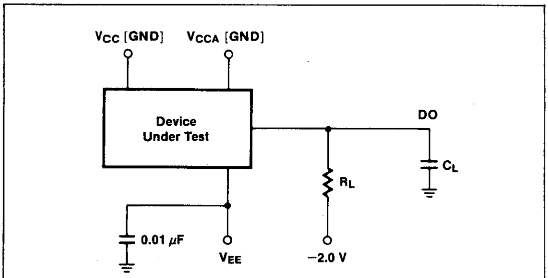
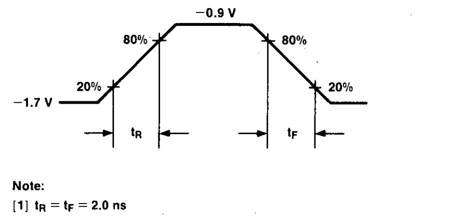


Figure 2. Input Pulse



AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%

		Limits										
		μPB100474-4.5		μPB100474-6		μPB100474-8		μPB100474-10		μPB100474-15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Read Mode												
Chip select access time	t_{ACS}		4		4		5		6		8	ns
Chip select recovery time	t_{RCS}		4		4		5		6		8	ns
Address access time	t_{AA}		4.5		6		8		10		15	ns
Write Mode												
Write pulse width	t_W	4.5		6		6		10		15		ns
Data setup time	t_{WSD}	1		1		1		2		2		ns
Data hold time	t_{WHD}	1		1		1		2		2		ns
Address setup time	t_{WSA}	1		1		1		3		3		ns
Address hold time	t_{WHA}	2		2		1		2		2		ns
Chip select setup time	t_{WSCS}	1		1		1		2		2		ns
Chip select hold time	t_{WHCS}	1		1		1		2		2		ns
Write disable time	t_{WS}		4		4		5		6		8	ns
Write recovery time	t_{WR}		4.5		6		8		10		10	ns

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) For the μPB100474-4.5/6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90°C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

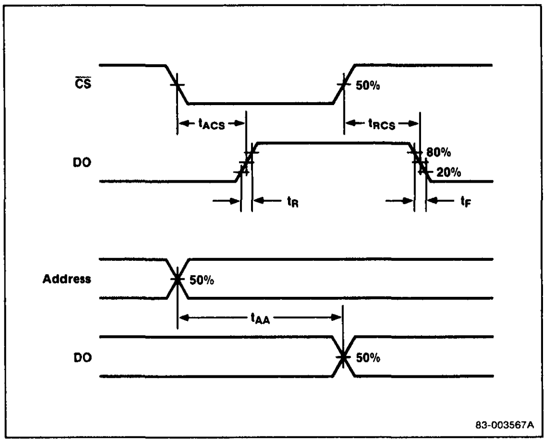
(3) See figures 1 and 2 for loading conditions and input pulse timing. For the μPB100474-4.5/6, C_L = 5 pF. For the μPB100474-8/10/15, C_L = 30 pF.

(4) Output rise and fall times = 2 ns (typ).

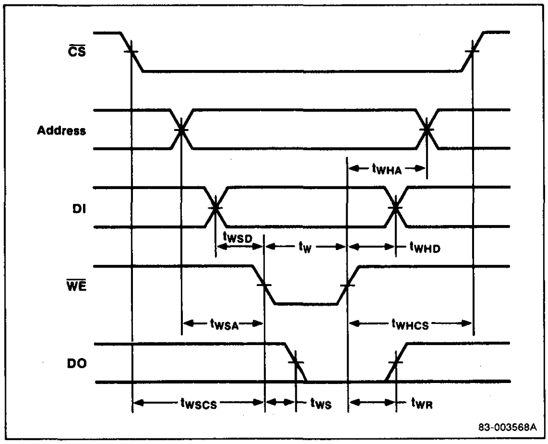
7

Timing Waveforms

Read Mode



Write Mode



NEC
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μPB100474A
1,024 x 4-BIT
100K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB100474A is a very high-speed 100K interface ECL RAM. It is organized as 1K words by 4 bits with noninverted, open emitter outputs and full voltage and temperature compensation. The device is packaged in a 24-pin cerdip or flatpack.

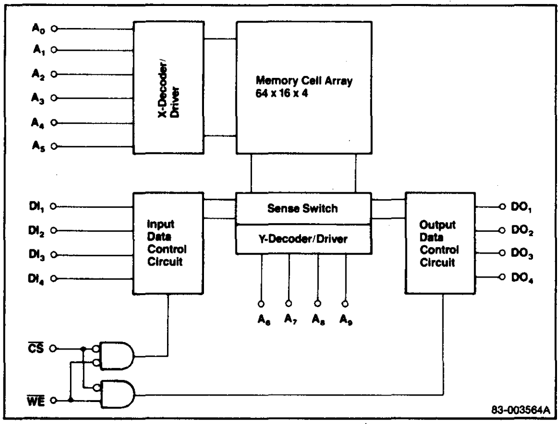
Features

- ☐ 1K-word bx 4-bit organization
- ☐ 100K ECL interface
- ☐ Full voltage and temperature compensation
- ☐ Open emitter outputs (noninverted)
- ☐ Fast access times
- ☐ 24-pin cerdip and flatpack packaging

Ordering Information

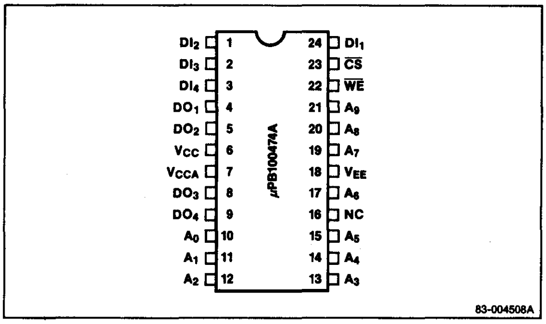
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474AB-5	5 ns	−250 mA	24-pin ceramic flatpack
AB-7	7 ns		
μPB100474AD-5	5 ns	−250 mA	24-pin cerdip
AD-7	7 ns		

Block Diagram

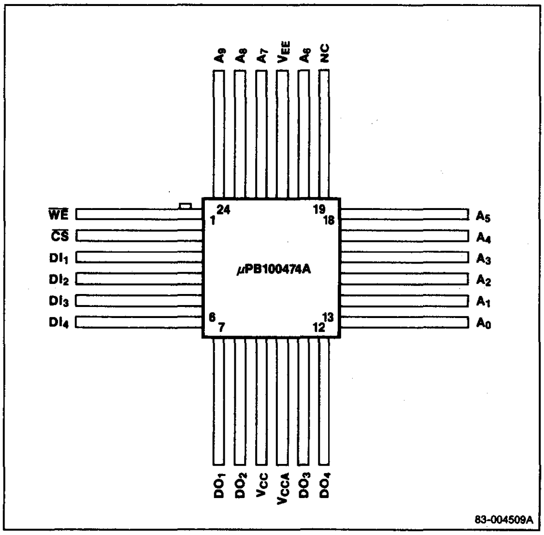


Pin Configurations

24-Pin Cerdip



24-Pin Ceramic Flatpack



7

Pin Identification

Symbol	Function
A_0-A_9	Address inputs
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	−4.5-volt power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Under bias, T_{STG} (Bias)	−55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ (min)
		−50			μA	For all others: $V_{IN} = V_{IL}$ (min)
Supply current	I_{EE}	−250			mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

Capacitance

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	
Output capacitance	C_{OUT}		5		pF	

Figure 1. Loading Conditions Test Circuit

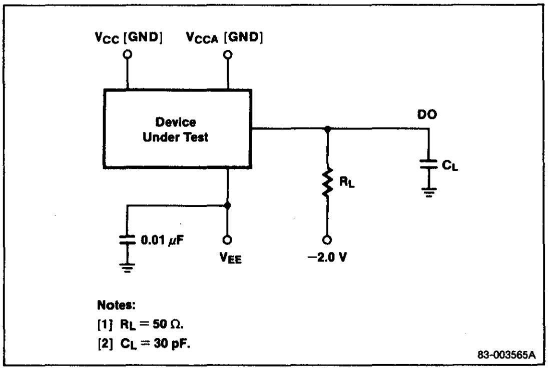
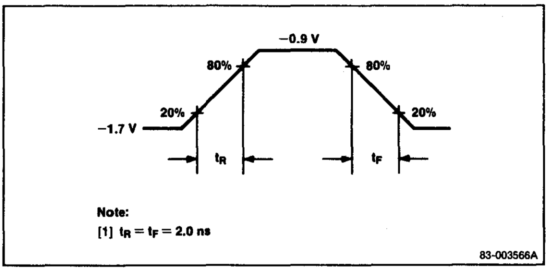


Figure 2. Input Pulse



AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		Limits						
		μPB100474A-5			μPB100474A-7			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Read Mode								
Address access time	t_{AA}			5			7	ns
Chip select access time	t_{ACS}			3			5	ns
Chip select recovery time	t_{RCS}			3			5	ns
Write Mode								
Write pulse width	t_W	5			7			ns
Data setup time	t_{WSD}	1			1			ns
Data hold time	t_{WHD}	1			1			ns
Address setup time	t_{WSA}	1			1			ns
Address hold time	t_{WHA}	1			1			ns
Chip select setup time	t_{WSCS}	1			1			ns
Chip select hold time	t_{WHCS}	1			1			ns
Write disable time	t_{WS}			3			5	ns
Write recovery time	t_{WR}			6			8	ns
Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

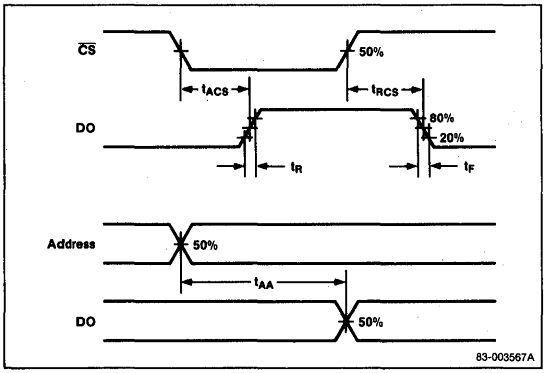
Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

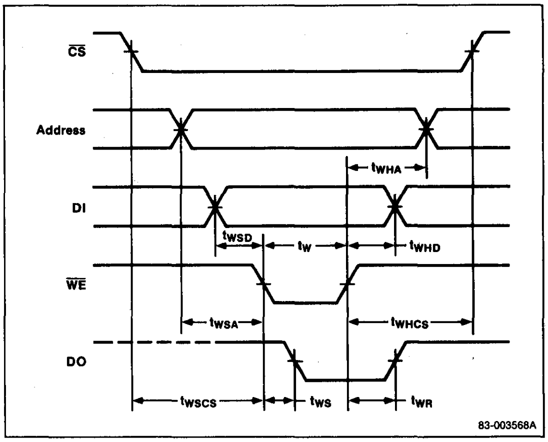
(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Timing Waveforms

Read Mode



Write Mode



NEC

NEC Electronics Inc.

μPB100480 16,384 x 1-BIT 100K ECL RAM

PRELIMINARY INFORMATION

Description

The μPB100480 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 16,384 words by 1 bit, with an open emitter output (noninverted) and low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB100480 is available in a hermetic, 300-mil, 20-pin cerdip or 20-pin ceramic flatpack.

Features

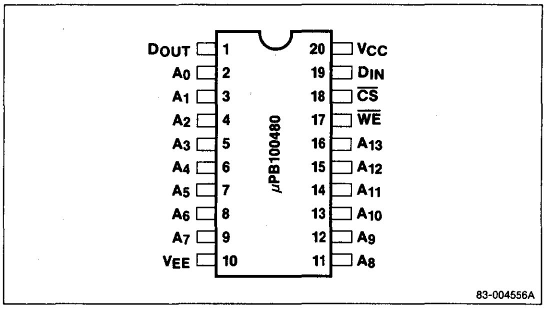
- ☐ 16,384-word x 1-bit organization
- ☐ 100K ECL interface with full voltage and temperature compensation
- ☐ Open emitter output (noninverted)
- ☐ Fast access times: 10 and 15 ns maximum
- ☐ Low power consumption
- ☐ 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging

Ordering Information

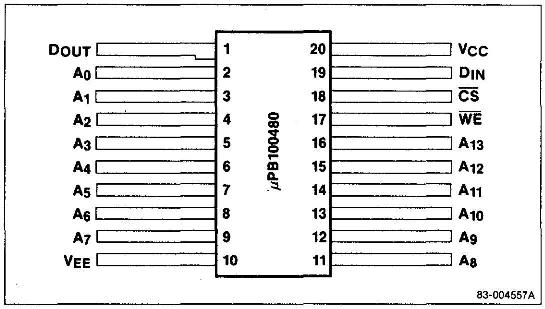
Part Number	Access Time (max)	Power Consumption (max)	Package
μPB100480D-10	10 ns	1.2 W	20-pin cerdip
D-15	15 ns	1.1 W	
μPB100480B-10	10 ns	1.2 W	20-pin ceramic flatpack
B-15	15 ns	1.1 W	

Pin Configurations

20-Pin Cerdip



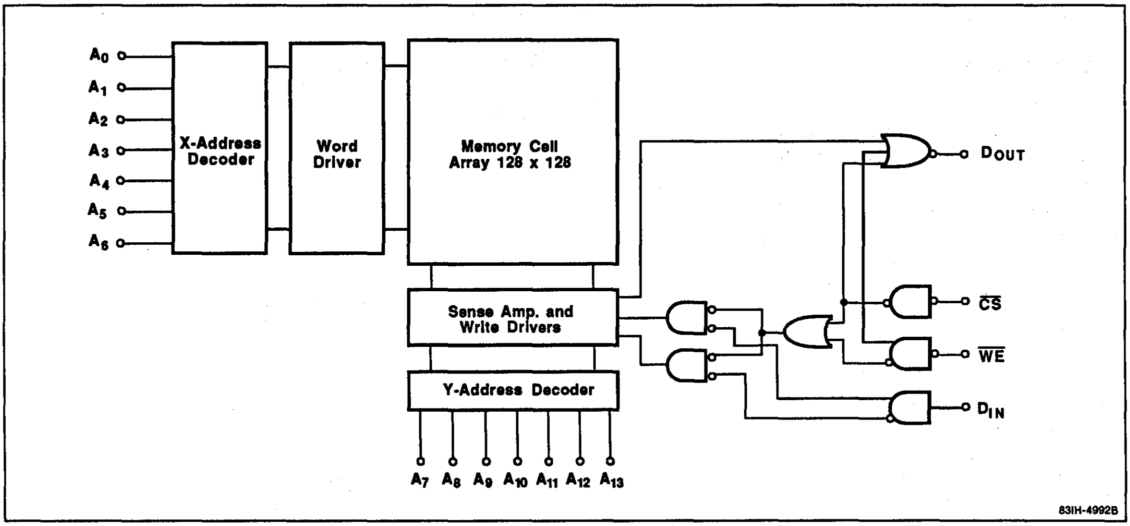
20-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0-A_{13}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Under bias, T_{STG} (bias)	–55 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

DC Characteristics

T_A = 0 to +85°C; V_{EE} = –4.5 V; output load = 50 Ω to –2.0 V; V_{CC} = 0 V

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	–1025	–880	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
Output voltage, low	V_{OL}	–1810	–1620	mV	$V_{IN} = V_{IH}$ (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	–1035		mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}		–1610	mV	$V_{IN} = V_{IH}$ (min) or V_{IL} (max)
Input voltage, high	V_{IH}	–1165	–880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	–1810	–1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	$V_{IN} = V_{IH}$ (max)
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ (min)
		–50		μA	For all others: $V_{IN} = V_{IL}$ (min)
Supply current	I_{EE}	–260		mA	For μPB100480-10: all inputs and outputs open
		–240		mA	For μPB100480-15: all inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = –5.2 V ± 5%

		Limits						
		μPB10480-10			μPB10480-15			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Read Mode								
Address access time	t_{AA}			10			15	ns
Chip select access time	t_{ACS}			5			8	ns
Chip select recovery time	t_{RCS}			5			8	ns
Write Mode								
Write pulse width	t_W	10			15			ns
Data setup time	t_{WSD}	2			3			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	2			3			ns
Address hold time	t_{WHA}	1			2			ns
Chip select setup time	t_{WSCS}	2			3			ns
Chip select hold time	t_{WHCS}	1			2			ns
Write disable time	t_{WS}			5			8	ns
Write recovery time	t_{WR}			11			17	ns
Output Rise and Fall Times								
Rise time	t_R		2			2		ns
Fall time	t_F		2			2		ns

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = –1.7 to –0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference levels = 50%.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Mode	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care

Figure 1. Loading Conditions Test Circuit

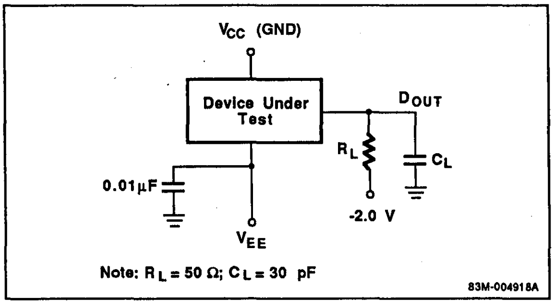
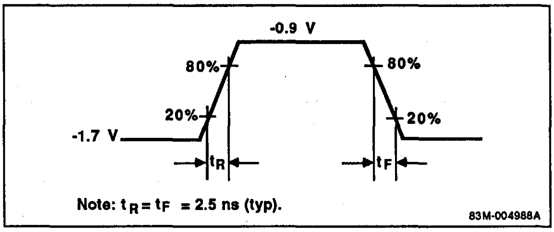
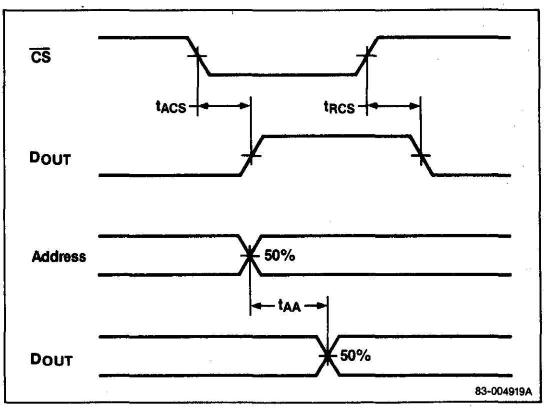


Figure 2. Input Pulse Waveform for Test

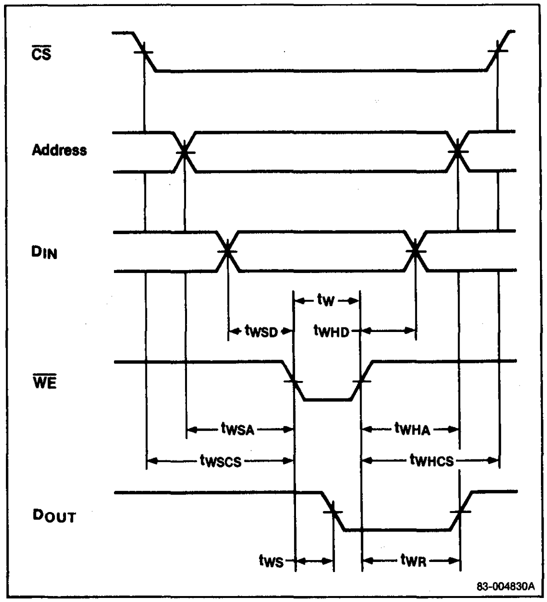


Timing Waveforms

Read Mode



Write Mode



NEC
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μPB100484
4,096 x 4-BIT 100K ECL RAM

Description

The μPDB100484 is a very high-speed 100K interface ECL random access memory. The device is organized as 4K words by 4 bits with open emitter outputs (noninverted). It is available in 28-pin cerdip or flatpack versions.

Features

- ☐ 4K-word x 4-bit organization
- ☐ 100K ECL interface
- ☐ Full voltage and temperature compensation
- ☐ Open emitter outputs (noninverted)
- ☐ Fast access times and low power consumption
- ☐ 28-pin cerdip and flatpack packaging

Ordering Information

Part Number	Access Time (max)	Supply Current (min)	Package
μPB100484B-10	10 ns	–260 mA	28-pin ceramic flatpack
B-15	15 ns	–240 mA	
μPB100484D-10	10 ns	–260 mA	28-pin cerdip
D-15	15 ns	–240 mA	

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	+0.5 to –7.0 V
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	+0.1 to –30 mA
Storage temperature, T_{STG}	–65 to +150°C
Under bias, T_{STG} (Bias)	–55 to +125°C

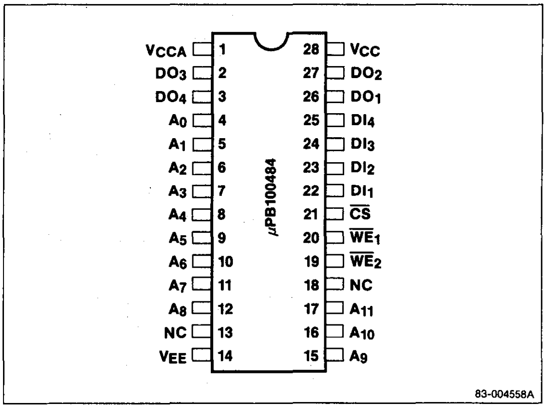
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

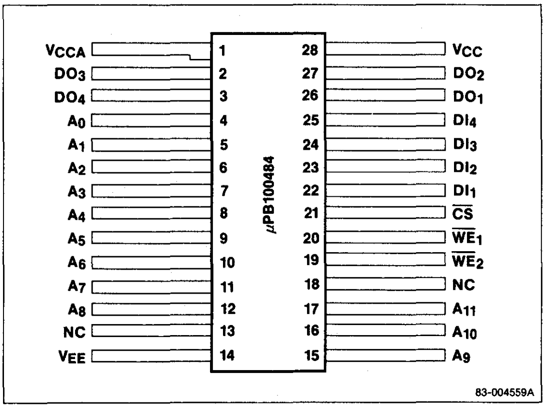
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	
Output capacitance	C_{OUT}		6		pF	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack

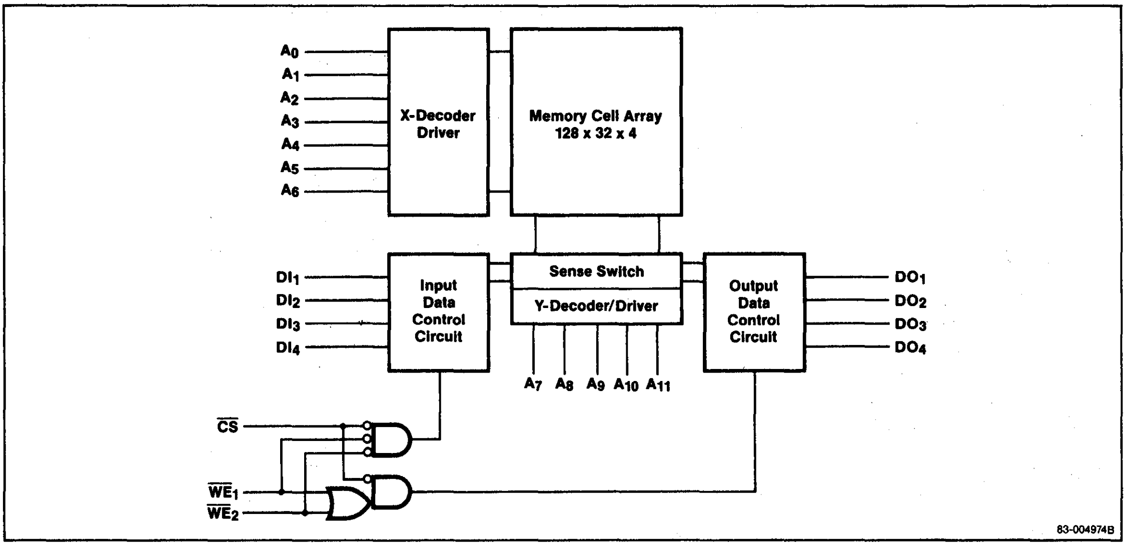


Pin Identification

Symbol	Function
A_0-A_{11}	Address inputs
DI_1-DI_4	Data inputs
DO_1-DO_4	Data outputs
$\overline{WE_1}$, $\overline{WE_2}$	Write enable inputs (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–4.5-volt power supply
NC	No connection

7

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	−260			mA	μPB100484-10: all inputs and outputs open
		−240			mA	μPB100484-15: all inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2 V; V_{CC} = V_{CCA} = 0 V

		Limits						
		μPB100484-10			μPB100484-15			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Read Mode								
Address access time	t_{AA}			10			15	ns
Chip select recovery time	t_{RCS}			5			8	ns
Chip select access time	t_{ACS}			5			8	ns
Write Mode								
Write pulse width	t_W	10			15			ns
Data setup time	t_{WSD}	2			3			ns
Data hold time	t_{WHD}	1			2			ns
Address setup time	t_{WSA}	2			3			ns
Address hold time	t_{WHA}	1			2			ns
Chip select setup time	t_{WSCS}	2			3			ns
Chip select hold time	t_{WHCS}	1			2			ns
Write disable time	t_{WS}			5			8	ns
Write recovery time	t_{WR}			11			17	ns
Output Rise and Fall Times								
Output rise time	t_R		2			2		ns
Output fall time	t_F		2			2		ns

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

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Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE_1}$ and $\overline{WE_2}$ must be low to initiate write operation. For read operation, either $\overline{WE_1}$ or $\overline{WE_2}$ or both must be high.

Figure 1. Loading Conditions Test Circuit

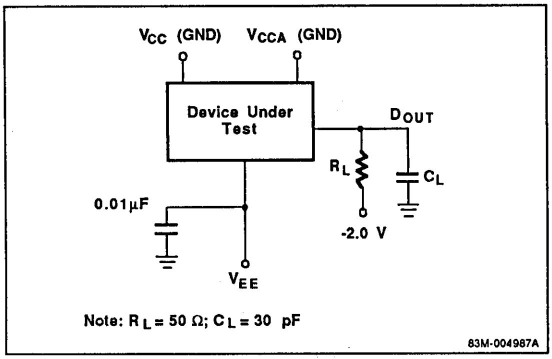
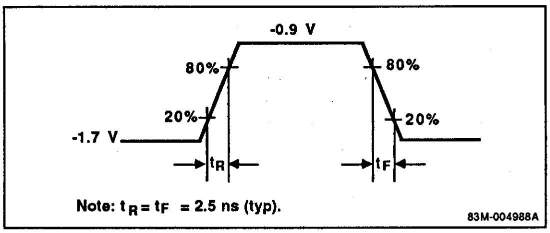
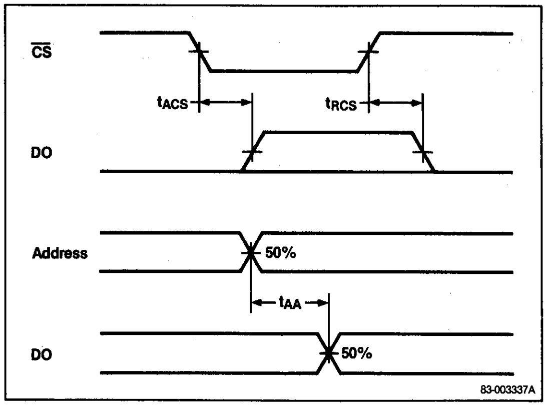


Figure 2. Input Pulse Waveform

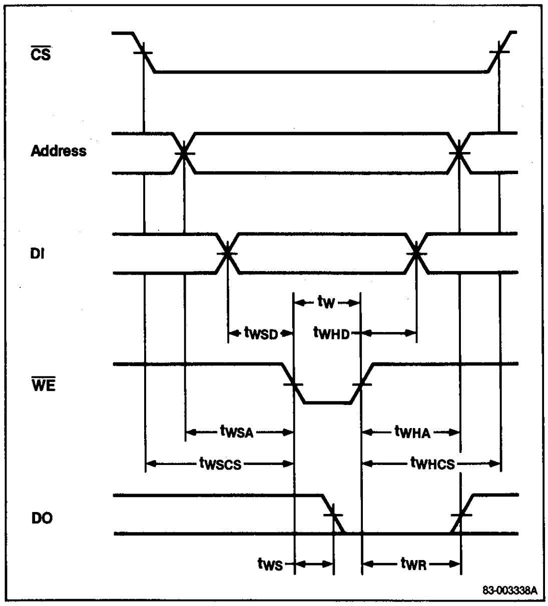


Timing Waveforms

Read Mode



Write Mode



NEC

EPROMs and EEPROMs

8

NEC

Section 8
EPROMs and EEPROMs

NEC

NEC Electronics Inc.

µPD27C256A
32,768 x 8-BIT
CMOS UV EPROM

Description

The µPD27C256A is a 262,144-bit ultraviolet erasable and electrically programmable read-only memory fabricated with double-polysilicon CMOS technology. The device is organized as 32K words by 8 bits and operates from a single +5-volt power supply.

The µPD27C256A has a single-location programming feature, three-state outputs, fully TTL-compatible inputs and outputs, and a program voltage (V_{PP}) of 12.5 volts.

The µPD27C256A is available in a cerdip package with a quartz window as an ultraviolet (UV) erasable EPROM.

Features

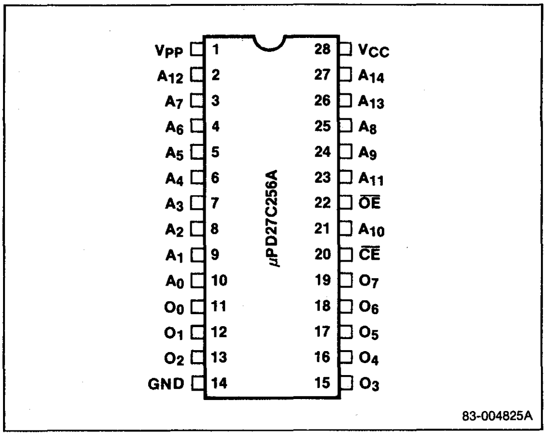
- ☐ 32K-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Single location programming
- ☐ High-speed programming
- ☐ Low power dissipation
  - — 165 mW (active)
  - — 550 µW (standby)
- ☐ TTL-compatible I/O for reading and programming
- ☐ Single +5-volt power supply
- ☐ JEDEC vendor identification
- ☐ Double-polysilicon CMOS technology
- ☐ 28-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
µPD27C256AD-15	150 ns	28-pin cerdip
D-20	200 ns	

Pin Configuration

28-Pin Cerdip



Pin Identification

Symbol	Function
A_0-A_{14}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage

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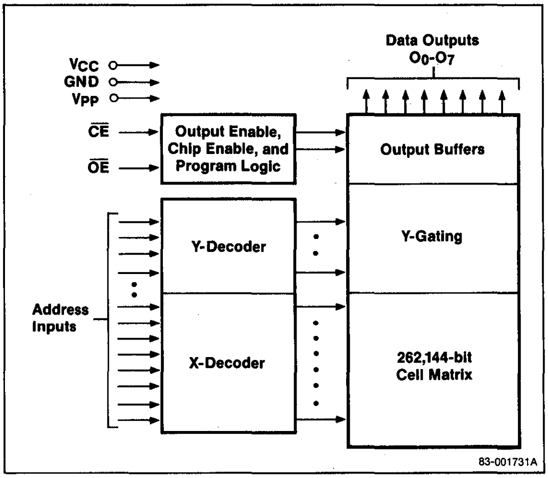
Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	–0.6 to +7.0 V
Input voltage, V_{IN} (Note 1)	–0.6 V to V_{CC} + 0.6 V
Output voltage, V_{OUT}	–0.6 V to V_{CC} + 0.6 V
Operating temperature, T_{OPR}	–25 to 85°C
Storage temperature, T_{STG}	–65 to 125°C
Program voltage, V_{PP}	–0.6 to +13.0 V
ID read voltage on pin 24, V_{ID}	–0.6 to +13.5 V

Note:

(1) V_{IN} = –3.0 V min for 20 ns pulse.

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1)

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4	6	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Notes:

(1) This parameter is sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC}

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read and Standby Modes						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	–0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
Operating supply current	I_{CCA2}			30	mA	f = 5 MHz; I_{OUT} = 0 mA
Standby supply current	I_{SB1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}		1	100	μA	$\overline{CE}$ = V_{CC}
Program voltage current	I_{PP1}		1	100	μA	V_{PP} = V_{CC}

DC Characteristics (cont)

T_A = 25 ±5°C; V_{CC} = +6 ±0.25 V; V_{PP} = +12.5 ±0.3 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Program, Program Verify, and Program Inhibit Modes						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	–0.3		0.8	V	
ID read voltage	V_{ID}	11.5		12.5	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5\ V \pm 10\%$; $V_{PP} = V_{CC}$

		Limits					
		μPD27C256A-15		μPD27C256A-20			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions (Note 2)
Read and Standby Modes							
Address to output delay	t_{ACC}		150		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ low to data output delay	t_{OE}		75		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to data output float delay	t_{DF}	0	60	0	60	ns	$\overline{CE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes:

(1) See figure 1 for output load; input rise and fall times = 0.45 V to 2.4 V; input and output timing measurement levels = 0.8 V and 2.0 V.

AC Characteristics (cont)

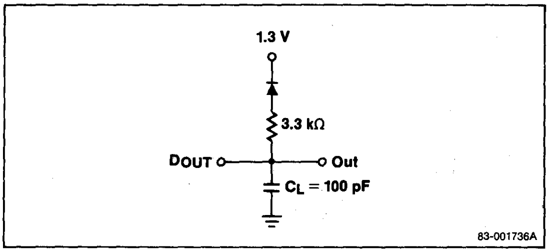
$T_A = 25 \pm 5°C$; $V_{CC} = +6 \pm 0.25\ V$; $V_{PP} = +12.5 \pm 0.3\ V$

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Program, Program Verify, and Program Inhibit Modes						
Address setup time	t_{AS}	2			μs	(Note 1)
Data setup time	t_{DS}	2			μs	(Note 1)
Address hold time	t_{AH}	2			μs	(Note 1)
Data hold time	t_{DH}	2			μs	(Note 1)
Output enable to output float delay	t_{DF}	0		130	ns	(Note 1)
V_{PP} setup time	t_{VPS}	2			μs	(Note 1)
Program pulse width	t_{PW}	0.95	1	1.05	ms	(Note 1)
V_{CC} setup time	t_{VCS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	(Note 1)
Overprogram pulse width	t_{OPW}	2.85		78.75	ms	
Data valid from $\overline{OE}$	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 V to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times = 20 ns.

Figure 1. Loading Conditions Test Circuit



Truth Table

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Read disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High-Z
ID read	V_{IL}	V_{IL}	V_{ID}	V_{CC}	V_{CC}	D_{OUT}

Notes:

(1) X can be either V_{IL} or V_{IH}.

Programming Operation

High-Speed Programming Mode

Begin programming by erasing all data; this sets all bits at a high logic level (1). To enter data, program a low-level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the eight output pins. Raise V_{CC} to +6 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V.

Apply a 1-ms (±5%) program pulse to $\overline{CE}$ as shown in the programming portion of the timing waveform. Verify the bit prior to making a program/no-program decision. If the bit is not programmed, apply another 1-ms pulse to $\overline{CE}$, up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of 3x ms (where "x" equals the number of tries) and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to +5 V ±10% and verify all data again.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C256As connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low-level (0) TTL pulse to the $\overline{CE}$ input of the device to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

To verify that the device was correctly programmed, set $\overline{OE}$ at logic level 0. To verify data on multiple μPD27C256As connected in parallel with a common $\overline{OE}$ input applied to all devices, first reduce V_{PP} to V_{CC}. Then the normal read mode can be used with a logic level 0 applied to the $\overline{CE}$ input of the device to be verified. Apply a logic level 1 to the $\overline{CE}$ input of all other devices.

Erasure

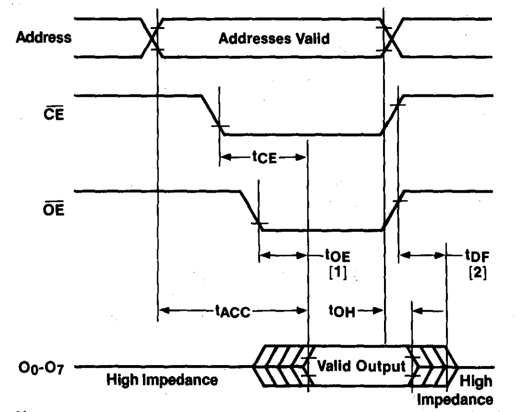
Erase data on the μPD27C256A by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by ultraviolet rays of 254 nm. A lighting level of 15 W-sec/cm² (min) is required to completely erase written data (ultraviolet ray intensity multiplied by exposure time).

An ultraviolet lamp rated at 12,000 μW/cm² takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C256A within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

Read Mode



Notes:

[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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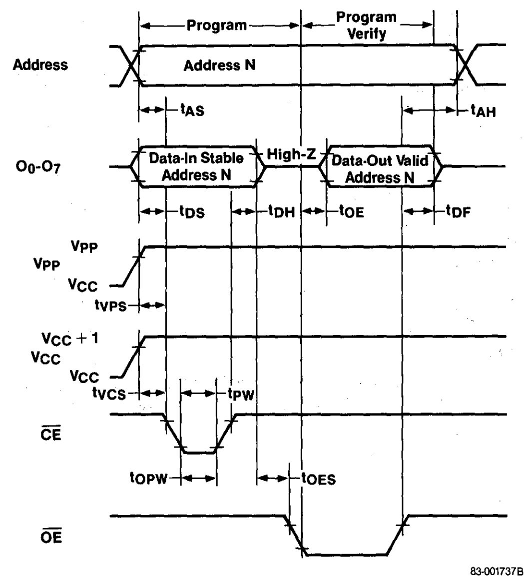
Program Mode



NEC
NEC Electronics Inc.

μPD27C512
65,536 x 8-BIT
CMOS UV EPROM

Description

The μPD27C512 is an ultraviolet erasable, electrically programmable 524,288-bit ROM fabricated with an advanced CMOS process for substantial power savings. The device is organized as 64K words by 8 bits and operates from a single +5-volt power supply. All inputs and outputs are TTL-compatible. The device is available in a 28-pin cerdip package with quartz window.

Features

- ☐ 64K x 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High-speed programming mode
- ☐ Low power dissipation
  - — 30 mA max (active)
  - — 100 μA max (standby)
- ☐ TTL-compatible inputs and outputs
- ☐ Single +5-volt power supply
- ☐ Three-state outputs
- ☐ Advanced CMOS technology
- ☐ 28-pin cerdip with quartz window

Ordering Information

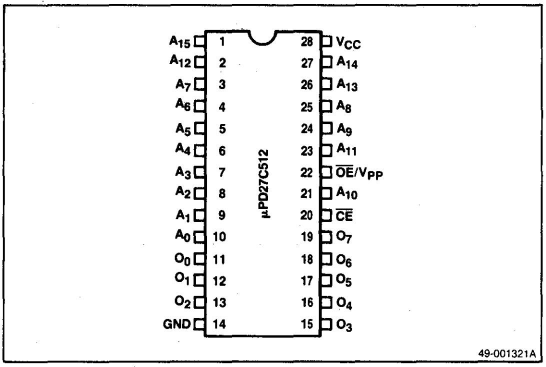
Part Number	Access Time (max)	Package
μPD27C512D-15	150 ns	28-pin cerdip with quartz window
D-20	200 ns	

Pin Identification

Symbol	Function
A_0-A_{15}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}/V_{PP}$	Output enable/program voltage
GND	Ground
V_{CC}	Power supply

Pin Configuration

28-Pin Cerdip

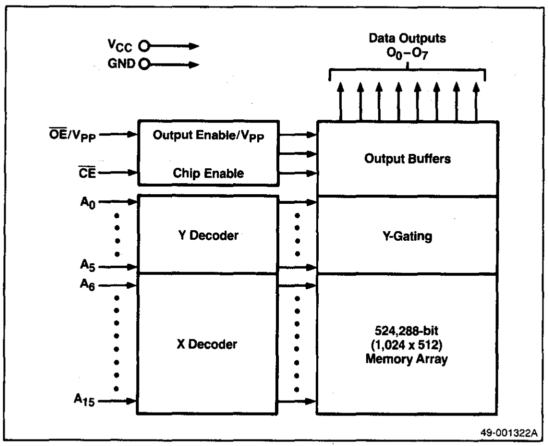


Absolute Maximum Ratings

Output voltage, V_O	−0.6 to +7.0 V
Input voltage, V_I	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Supply voltage, V_{CC}	−0.6 to +7.0 V
Supply voltage, V_{PP}	−0.6 to +13.5 V
Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



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Mode Selection

Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	+5 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	+5 V	High-Z
Standby	V_{IH}	X	+5 V	High-Z
Program	V_{IL}	V_{PP}	+6 V	D_{IN}
Program verify	V_{IL}	V_{IL}	+6 V	D_{OUT}
Program inhibit	V_{IH}	V_{PP}	+6 V	High-Z

Notes:

(1) X = V_{IL} or V_{IH}

Capacitance

$T_A = 25°C$; f = 1 MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN1}			6	pF	$V_I = 0$ V
	C_{IN2}			20	pF	$\overline{OE}/V_{PP}$; $V_I = 0$ V
Output capacitance	C_{OUT}			12	pF	$V_O = 0$ V

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read and Standby Modes						
Input voltage, high	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	$V_{CC} - 0.7$			V	$I_{OH} = -100\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output leakage current	I_{LO}			10	μA	$V_O = 0$ to V_{CC}; $\overline{OE} = V_{IH}$
Input leakage current	I_{LI}			10	μA	$V_I = 0$ to V_{CC}
V_{CC} current, active	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$; $V_I = V_{IH}$
	I_{CCA2}			30	mA	f = 5 MHz; $I_{OUT} = 0$ mA
V_{CC} current, standby	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$; $V_I = 0$ to V_{CC}
Programming Modes $T_A = 25 \pm 5°C$; $V_{CC} = 6.0 \pm 0.25$ V; $V_{PP} = 12.5 \pm 0.3$ V						
Input voltage, high	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_I = V_{IL}$ or V_{IH}
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
V_{PP} current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$; $\overline{OE}/V_{PP} = V_{IH}$
V_{CC} current	I_{CC}			30	mA	

AC Characteristics, Read and Standby Modes

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits					
		μPD27C512-15		μPD27C512-20			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Address to output delay	t_{ACC}		150		200	ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200	ns	$\overline{OE}/V_{PP} = V_{IL}$
$\overline{OE}/V_{PP}$ to output delay	t_{OE}		75		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}/V_{PP}$ high to output float	t_{DF}	0	60	0	60	ns	$\overline{CE} = V_{IL}$
Output hold from address, $\overline{CE}$ or $\overline{OE}$, whichever transition occurs first	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$

Notes:

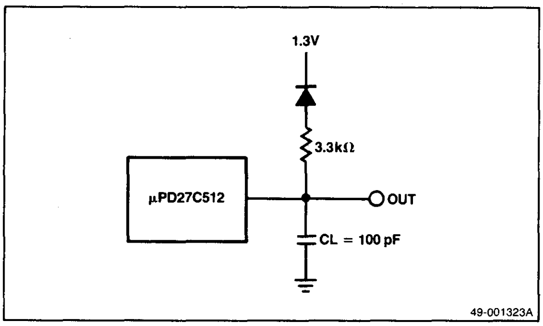
(1) Output load: see figure 1. Input rise and fall times ≤ 20 ns. Input pulse levels: 0.45 and 2.4 V. Timing measurement reference levels: inputs and outputs = 0.8 and 2.0 V

AC Characteristics, Programming Modes

T_A = 25 ±5°C; V_{CC} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{CE}$ to output float time	t_{DF}	0		130	ns	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.95	1.0	1.05	ms	
Overprogram pulse width	t_{OPW}	2.85		78.75	ms	
$\overline{CE}$ to output delay	t_{DV}			1	μs	$\overline{OE}/V_{PP} = V_{IL}$
$\overline{OE}/V_{PP}$ hold time	t_{OEH}	2			μs	
$\overline{OE}/V_{PP}$ recovery time	t_{VR}	2			μs	
$\overline{OE}/V_{PP}$ rise time	t_{PRT}	50			ns	

Figure 1. Loading Conditions Test Circuit



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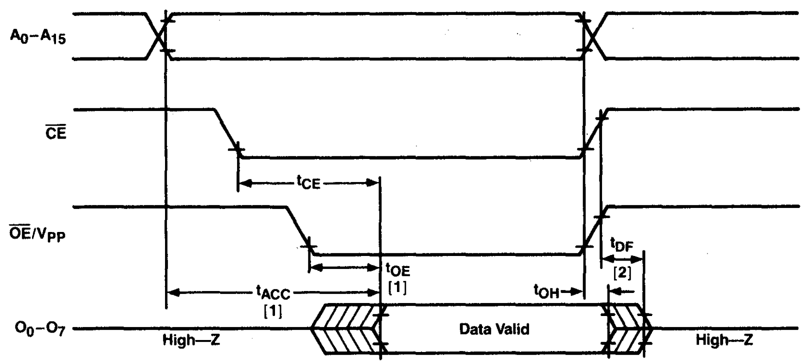
Timing Waveforms

Read Mode



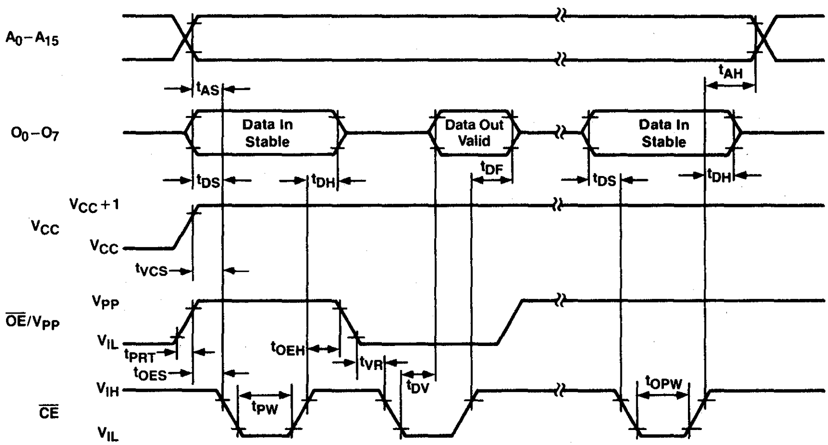
Notes:

[1] $\overline{OE}/V_{PP}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read cycles without affecting t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}/V_{PP}$ or $\overline{CE}$, whichever occurs first.

49-001324B

Programming Mode



Notes:

[1] V_{CC} must be applied before or simultaneously with $\overline{OE}$/Vpp and removed after or simultaneously with $\overline{OE}$/Vpp.

[2] Vpp must not be greater than +13.0 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to pin Vpp may affect device reliability.

49-001325B

Programming Operation

High-Speed Programming Mode

Begin programming by erasing all data; this places all bits in the high-level (1) state. Enter data by programming a low-level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the eight output pins. Raise V_{CC} to +6 V ±0.25 V; then raise $\overline{OE}/V_{PP}$ to +12.5 V ±0.3 V. Apply a 1-ms (±5%) program pulse to $\overline{CE}$ as shown in the programming mode timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 1-ms pulse to $\overline{CE}$, up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of "x" ms (where "x" equals the number of tries multiplied by 3) and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C512s connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}/V_{PP}$) may be common. Program individual devices by applying a low-level (0) TTL pulse to the $\overline{CE}$ input of the μPD27C512 to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

Perform verification on the programmed bits to determine that the data was correctly programmed. The program verification can be performed with $\overline{CE}$ and $\overline{OE}/V_{PP}$ at low levels (0).

Erasure

Erase data on the μPD27C512 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254-nm ultraviolet rays. A minimum lighting level of 15 W sec/cm^2 (ultraviolet ray intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C512 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

μPD27C1000A 131,072 x 8-BIT CMOS UV EPROM

Description

The μPD27C1000A is a 1,048,576-bit ultraviolet erasable and electrically programmable read-only memory fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 131,072 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C1000A has both page and single-location programming features, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage (V_{PP}) of 12.5 volts and is available in a 32-pin cerdip with a quartz window.

Features

- ☐ 131,072-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High-speed programming capability
  - — Page programming
  - — Single byte programming
- ☐ Low power dissipation
  - — 40 mA maximum (active)
  - — 100 μA maximum (standby)
- ☐ TTL-compatible I/O for reading and programming
- ☐ Single +5-volt power supply
- ☐ Double-polysilicon CMOS technology
- ☐ 32-pin cerdip packaging
- ☐ Pinout compatibility with 28-pin, mask-programmable μPD23C1000s

Ordering Information

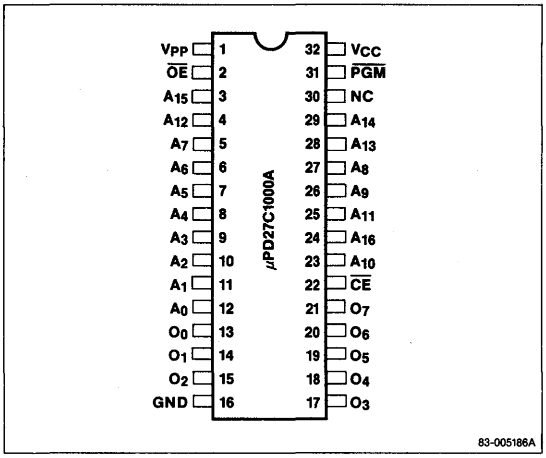
Part Number	Access Time (max)	Package
μPD27C1000AD-12	120 ns	32-pin cerdip with a quartz window
D-15	150 ns	
D-20	200 ns	

Pin Identification

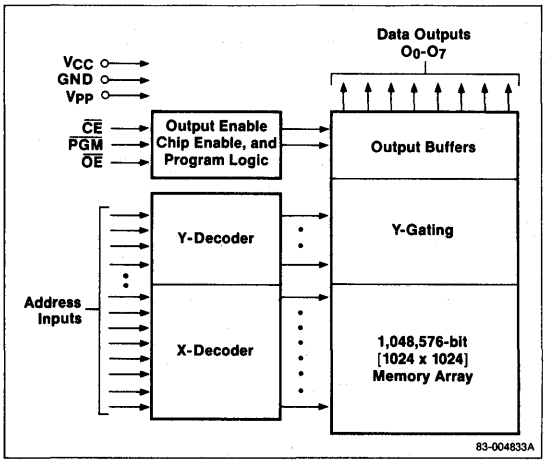
Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

Pin Configuration

32-Pin Cerdip



Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	–0.6 to +7.0 V
Input voltage, V_{IN}	–0.6 to +7.0 V
Input voltage, A_9	–0.6 to +13.5 V
Output voltage, V_{OUT}	–0.6 to +7.0 V
Operating temperature, T_{OPR}	–10 to +80°C
Storage temperature, T_{STG}	–65 to +125°C
Program voltage, V_{PP}	–0.6 to +13.5 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			14	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			16	pF	V_{OUT} = 0 V

Truth Table

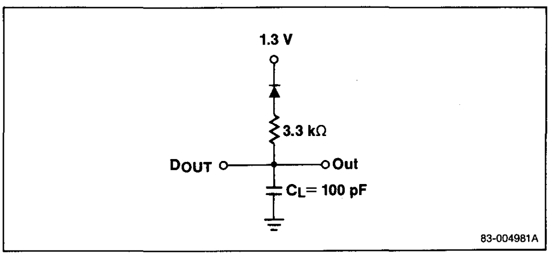
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (Note 2)	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	X	+5.0 V	+5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	High-Z
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{OUT}
Byte program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	D_{IN}
Program inhibit	X	V_{IL}	V_{IL}	+12.5 V	+6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) "X" can be either V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times or switched from V_{IL} to V_{IH} at least 2 μs before $\overline{OE}$ or $\overline{CE}$ becomes V_{IH}.

Figure 1. Loading Conditions Test Circuit



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC} ±0.6

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read, Output Disable, and Standby Modes						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	–0.3		0.8	V	
Output leakage current	I_{LO}	–10		10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			15	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			40	mA	f = 8.4 MHz; t_{ACC} = 120 ns; I_{OUT} = 0 mA
				30	mA	f = 6.7 MHz; t_{ACC} = 150 ns; I_{OUT} = 0 mA
				25	mA	f = 5 MHz; t_{ACC} = 200 ns; I_{OUT} = 0 mA
Standby supply current	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}
Program voltage current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
All Program Modes T_A = +25 ±5°C; V_{CC} = +6.5 ±0.25 V; V_{PP} = +12.5 ±0.3 V						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	–0.3		0.8	V	
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC}

Parameter	Symbol	μPD27C1000A-12 Min	μPD27C1000A-12 Max	μPD27C1000A-15 Min	μPD27C1000A-15 Max	μPD27C1000A-20 Min	μPD27C1000A-20 Max	Unit	Test Conditions
Read and Standby Modes									
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ high to data output float delay	t_{DF}	0	50	0	50	0	60	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes:

(1) See figure 1 for output load; input rise and fall times ≤ 20 ns; input pulse levels = 0.45 V and 2.4 V; input and output timing measurement levels = 0.8 V and 2.0 V.

AC Characteristics (cont)

T_A = +25 ±5°C; V_{CC} = +6.5 ±0.25 V; V_{PP} = +12.5 ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions (Note 1)
Page Data Latch, Page Program, Program Verify, and Program Inhibit Modes						
Address setup time	t_{AS}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
Output enable to output float delay	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
V_{CC} setup time	t_{VCS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ hold time	t_{OEH}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data valid from $\overline{OE}$	t_{OE}			150	ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions (Note 1)
Byte Programming Mode						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 V to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

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Programming Operation

Begin programming by erasing all data; this sets all bits at a high logic level (1). The μPD27C1000A is originally shipped in this condition. To enter data, program a low-level (0) TTL signal into the chosen location.

Address the first byte or page location and apply valid data at the eight output pins. Raise V_{CC} to +6.5 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V.

Byte Programming

For byte programming, $\overline{CE}$ should be set at 0 and $\overline{OE}$ at 1 to start programming at the initial address. Apply a 0.1-ms program pulse to $\overline{PGM}$ as shown in the byte programming portion of the timing waveforms. Set $\overline{OE}$ to 0 to verify the eight bits prior to making a program/no program decision. If the byte is not programmmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Page Programming

For page programming, $\overline{CE}$ and $\overline{PGM}$ should be set to 1. $\overline{OE}$ pulses low four times to latch the addressed 4-byte, one-page data. Subsequently, $\overline{CE}$ and $\overline{OE}$ should be set to a high level and a 0.1-ms program pulse applied to $\overline{PGM}$ as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Program Inhibit

Use the programming inhibit option to program multiple μPD27C1000As connected in parallel. All like inputs except $\overline{PGM}$ and $\overline{OE}$ may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{PGM}$ pin of the device to be programmed. Applying a high-level signal to the $\overline{PGM}$ pins of the other devices prevents them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read operation can be used with a logic level 1 applied to the $\overline{PGM}$ pin and a logic level 0 applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. A logic level 1 should be applied to the $\overline{CE}$ and $\overline{OE}$ pins of all other devices.

Erasure

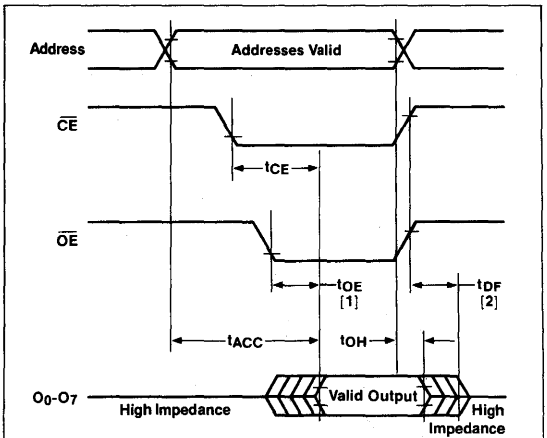
Erase data on the μPD27C1000A by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C1000A within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

83-004835A

Timing Waveforms (cont)

Page Programming

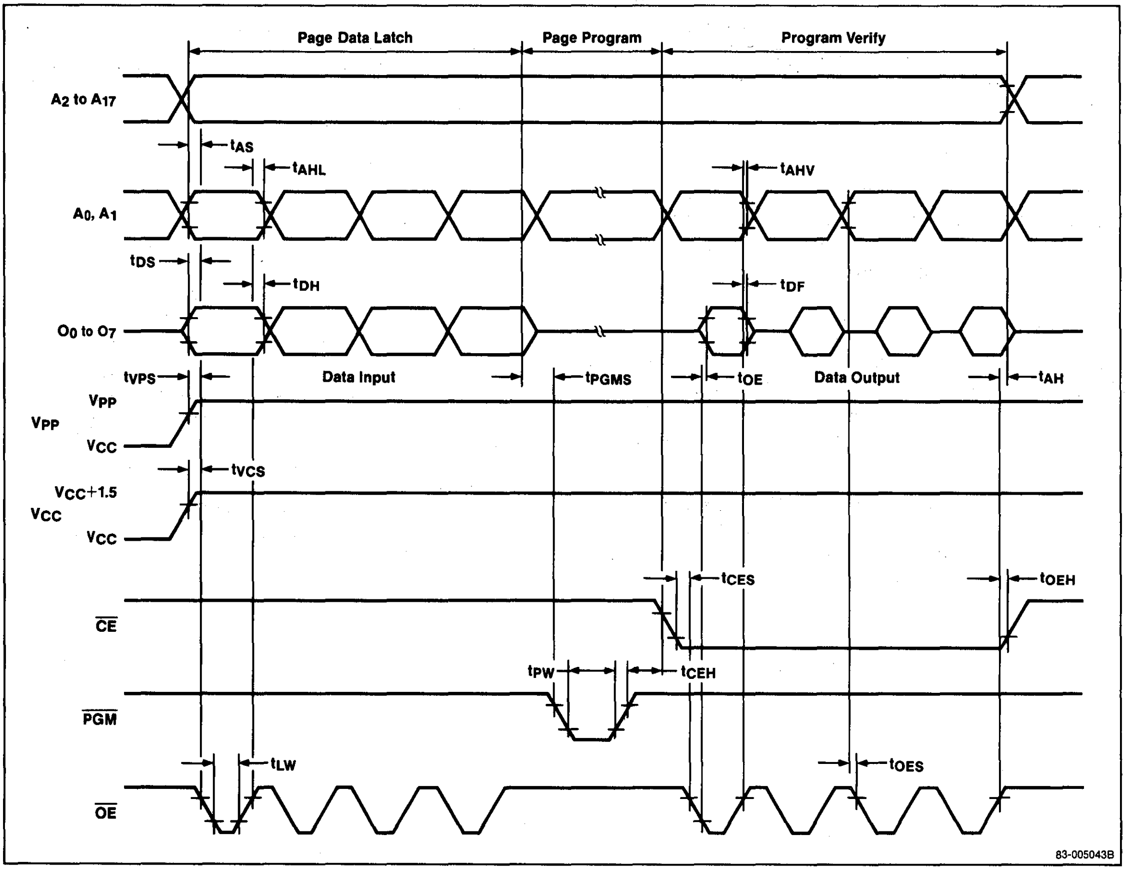
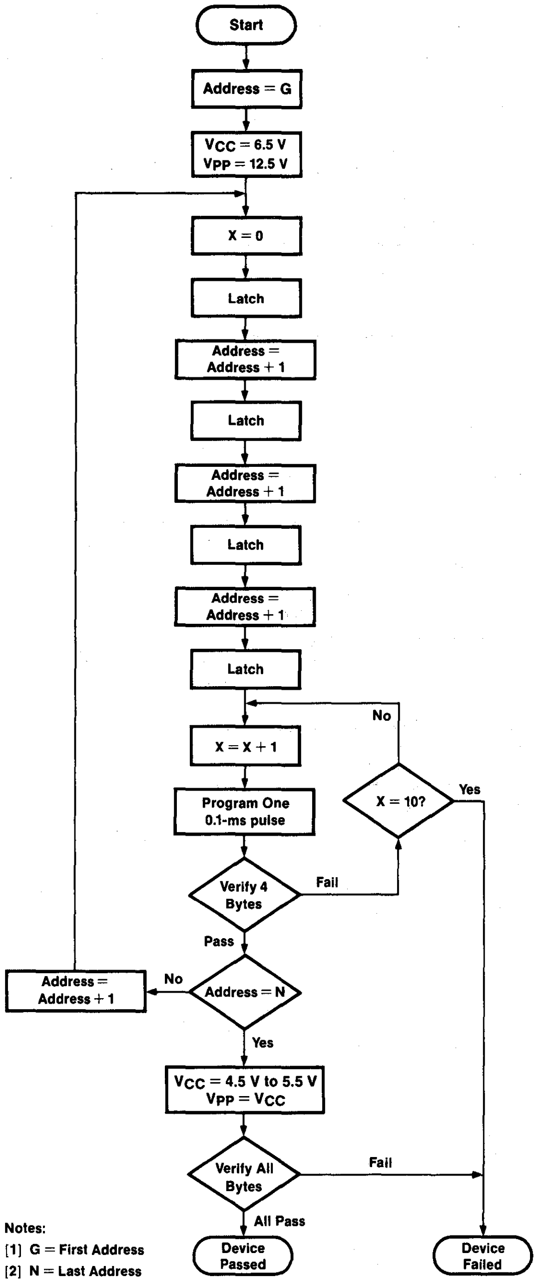


Figure 2. Page Programming Flowchart

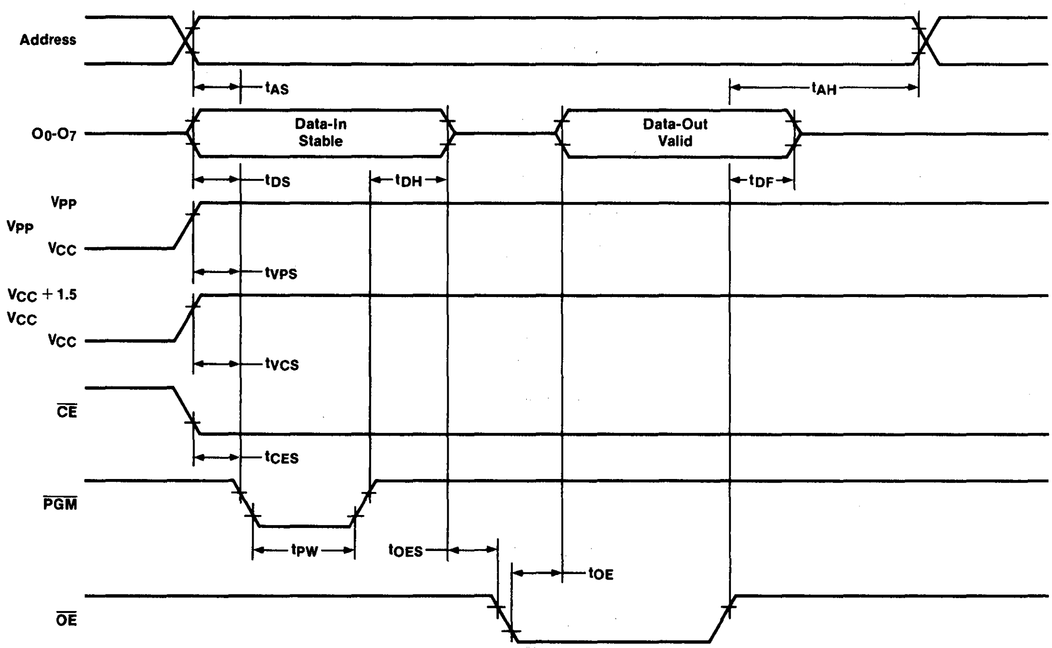


Notes:
[1] G = First Address
[2] N = Last Address

8

Timing Waveforms (cont)

Byte Programming



Notes:

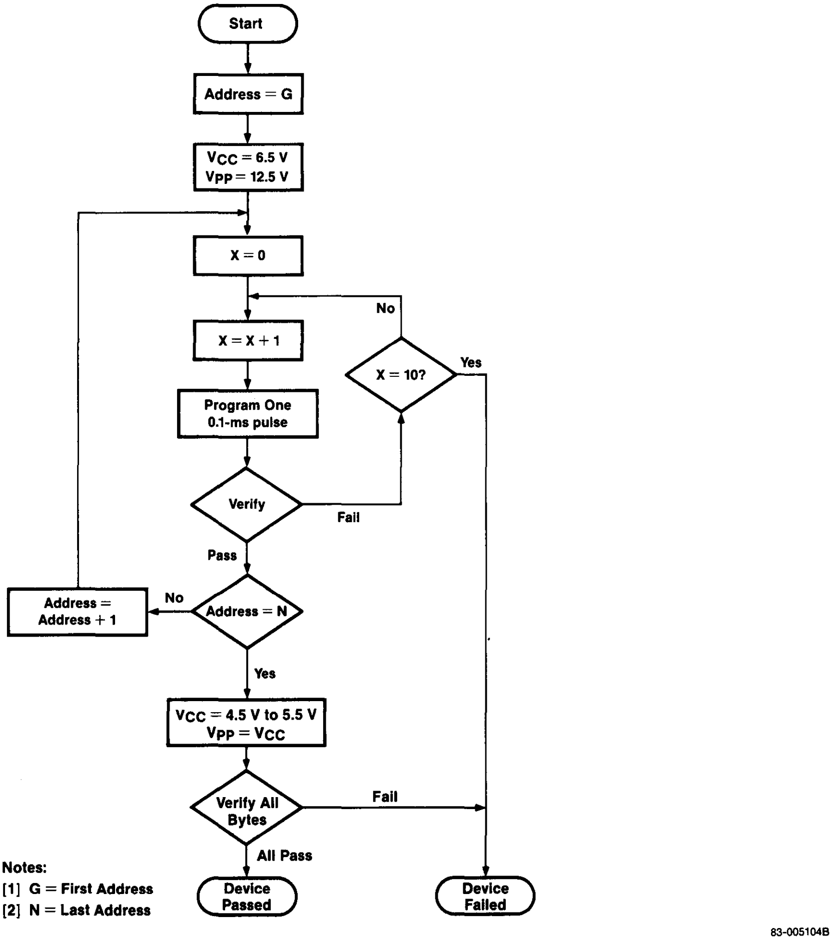
[1] V_{CC} must be applied before or simultaneously with Vpp and removed after or simultaneously with Vpp.

[2] Vpp must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to Vpp may affect device reliability.

83-005116B

Figure 3. Byte Programming Flowchart



Notes:
[1] G = First Address
[2] N = Last Address

8

NEC
NEC Electronics Inc.

μPD27C1001A 131,072 x 8-BIT CMOS UV EPROM

Description

The μPD27C1001A is a 1,048,576-bit ultraviolet erasable and electrically programmable read-only memory fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 131,072 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C1001A has both page and single-location programming features, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage (V_{PP}) of 12.5 volts and is available in a 32-pin cerdip with a quartz window.

Features

- ☐ 131,072-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High-speed programming capability
  - — Page programming
  - — Single byte programming
- ☐ Low power dissipation
  - — 40 mA maximum (active)
  - — 100 μA maximum (standby)
- ☐ TTL-compatible I/O for reading and programming
- ☐ Single +5-volt power supply
- ☐ Double-polysilicon CMOS technology
- ☐ 32-pin cerdip packaging
- ☐ JEDEC-compatible pinout

Ordering Information

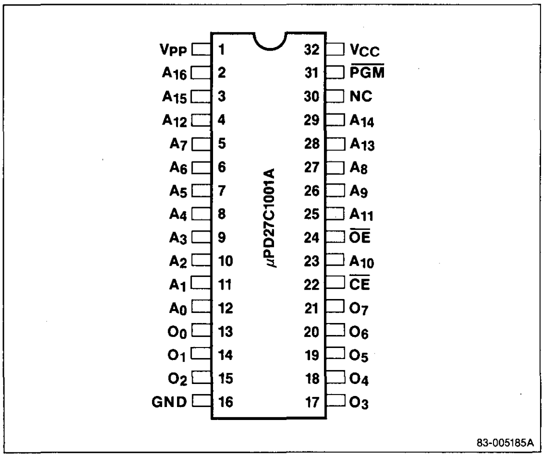
Part Number	Access Time (max)	Package
μPD27C1001AD-12	120 ns	32-pin cerdip with a quartz window
D-15	150 ns	
D-20	200 ns	

Pin Identification

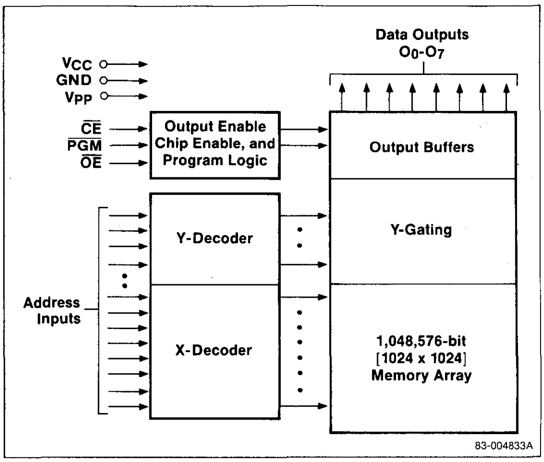
Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

Pin Configuration

32-Pin Cerdip



Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	–0.6 to +7.0 V
Input voltage, V_{IN}	–0.6 to +7.0 V
Input voltage, A_9	–0.6 to +13.5 V
Output voltage, V_{OUT}	–0.6 to +7.0 V
Operating temperature, T_{OPR}	–10 to +80°C
Storage temperature, T_{STG}	–65 to +125°C
Program voltage, V_{PP}	–0.6 to +13.5 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A =25°C; f = 1 MHz

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			14	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			16	pF	V_{OUT} = 0 V

Truth Table

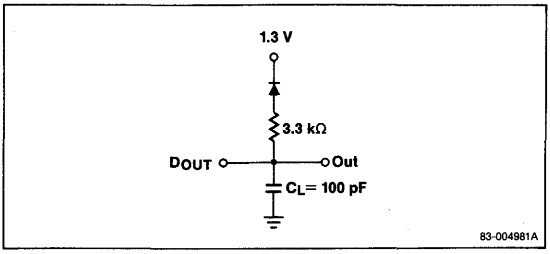
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (Note 2)	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	X	+5.0 V	+5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	High-Z
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{OUT}
Byte program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	D_{IN}
Program inhibit	X	V_{IL}	V_{IL}	+12.5 V	+6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) "X" can be either V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times or switched from V_{IL} to V_{IH} at least 2 μs before $\overline{OE}$ or $\overline{CE}$ becomes V_{IH}.

Figure 1. Loading Conditions Test Circuit



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC} ±0.6

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Read, Output Disable, and Standby Modes						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = –400 μA
	V_{OH2}	V_{CC} – 0.7			V	I_{OH} = –100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	–0.3		0.8	V	
Output leakage current	I_{LO}	–10		10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			15	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			40	mA	f = 8.4 MHz; t_{ACC} = 120 ns; I_{OUT} = 0 mA
				30	mA	f = 6.7 MHz; t_{ACC} = 150 ns; I_{OUT} = 0 mA
				25	mA	f = 5 MHz; t_{ACC} = 200 ns; I_{OUT} = 0 mA
Standby supply current	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}
Program voltage current	I_{PP}		1	100	μA	V_{PP} = V_{CC}
All Program Modes T_A = +25 ±5°C; V_{CC} = +6.5 ±0.25 V; V_{PP} = +12.5 ±0.3 V						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	–0.3		0.8	V	
Input leakage current	I_{LI}	–10		10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = +5.0\ V \pm10\%$; $V_{PP} = V_{CC}$

Parameter	Symbol	μPD27C1001A-12 Min	μPD27C1001A-12 Max	μPD27C1001A-15 Min	μPD27C1001A-15 Max	μPD27C1001A-20 Min	μPD27C1001A-20 Max	Unit	Test Conditions
Read and Standby Modes									
Address to output delay	t_{ACC}		120		150		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		120		150		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ high to data output float delay	t_{DF}	0	50	0	50	0	60	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes:

(1) See figure 1 for output load; input rise and fall times ≤ 20 ns; input pulse levels = 0.45 V and 2.4 V; input and output timing measurement levels = 0.8 V and 2.0 V.

AC Characteristics (cont)

$T_A = +25 \pm5°C$; $V_{CC} = +6.5 \pm0.25\ V$; $V_{PP} = +12.5 \pm0.3\ V$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions (Note 1)
Page Data Latch, Page Program, Program Verify, and Program Inhibit Modes						
Address setup time	t_{AS}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
Output enable to output float delay	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
V_{CC} setup time	t_{VCS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ hold time	t_{OEH}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data valid from $\overline{OE}$	t_{OE}			150	ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions (Note 1)
Byte Programming Mode						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 V to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

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Programming Operation

Begin programming by erasing all data; this sets all bits at a high logic level (1). The μPD27C1001A is originally shipped in this condition. To enter data, program a low-level (0) TTL signal into the chosen location.

Address the first byte or page location and apply valid data at the eight output pins. Raise V_{CC} to +6.5 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V.

Byte Programming

For byte programming, $\overline{CE}$ should be set at 0 and $\overline{OE}$ at 1 to start programming at the initial address. Apply a 0.1-ms program pulse to $\overline{PGM}$ as shown in the byte programming portion of the timing waveforms. Set $\overline{OE}$ to 0 to verify the eight bits prior to making a program/no program decision. If the byte is not programmmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Page Programming

For page programming, $\overline{CE}$ and $\overline{PGM}$ should be set to 1. $\overline{OE}$ pulses low four times to latch the addressed 4-byte, one-page data. Subsequently, $\overline{CE}$ and $\overline{OE}$ should be set to a high level and a 0.1-ms program pulse applied to $\overline{PGM}$ as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Program Inhibit

Use the programming inhibit option to program multiple μPD27C1001As connected in parallel. All like inputs except $\overline{PGM}$ and $\overline{OE}$ may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{PGM}$ pin of the device to be programmed. Applying a high-level signal to the $\overline{PGM}$ pins of the other devices prevents them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read operation can be used with a logic level 1 applied to the $\overline{PGM}$ pin and a logic level 0 applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. A logic level 1 should be applied to the $\overline{CE}$ and $\overline{OE}$ pins of all other devices.

Erasure

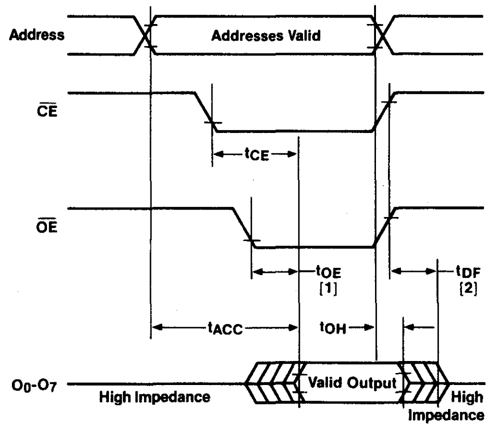
Erase data on the μPD27C1001A by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C1001A within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

83-004835A

Timing Waveforms (cont)

Page Programming

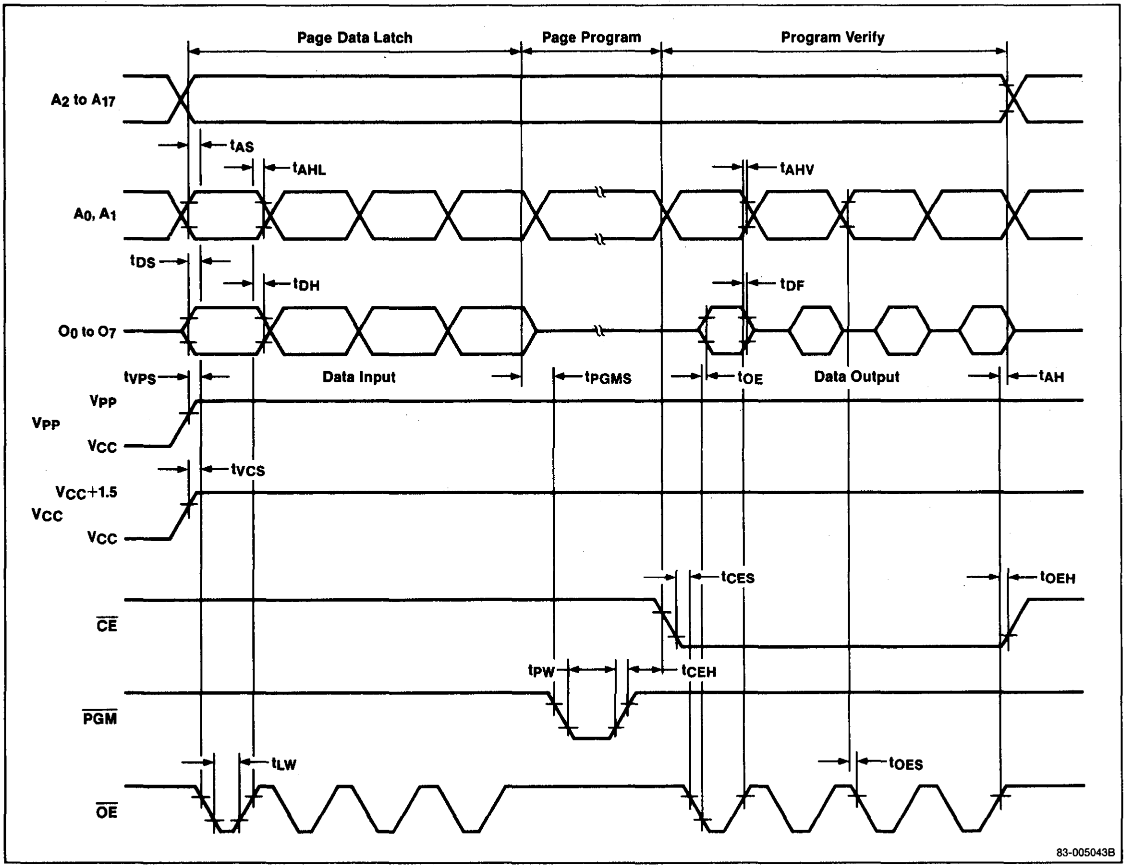
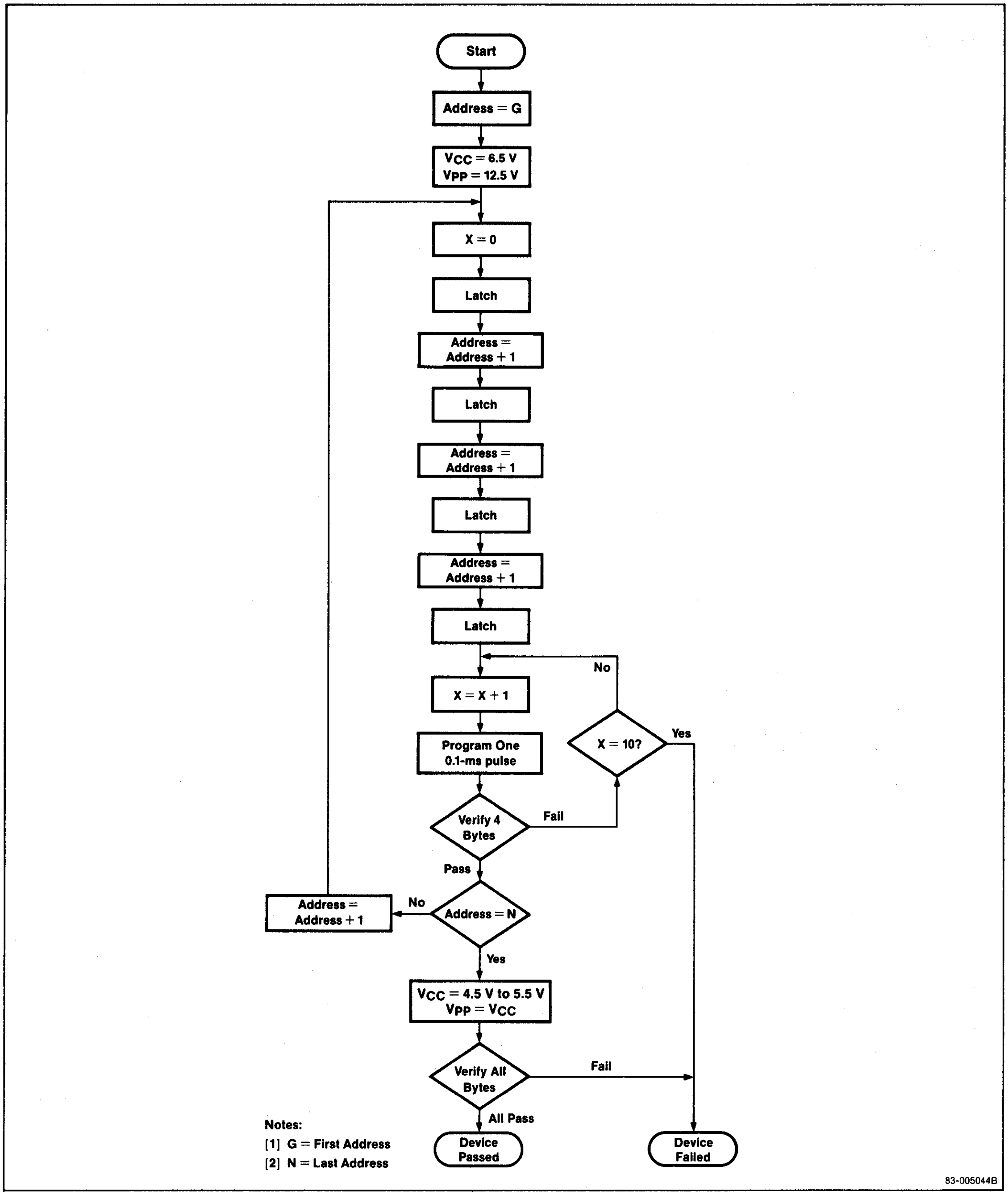
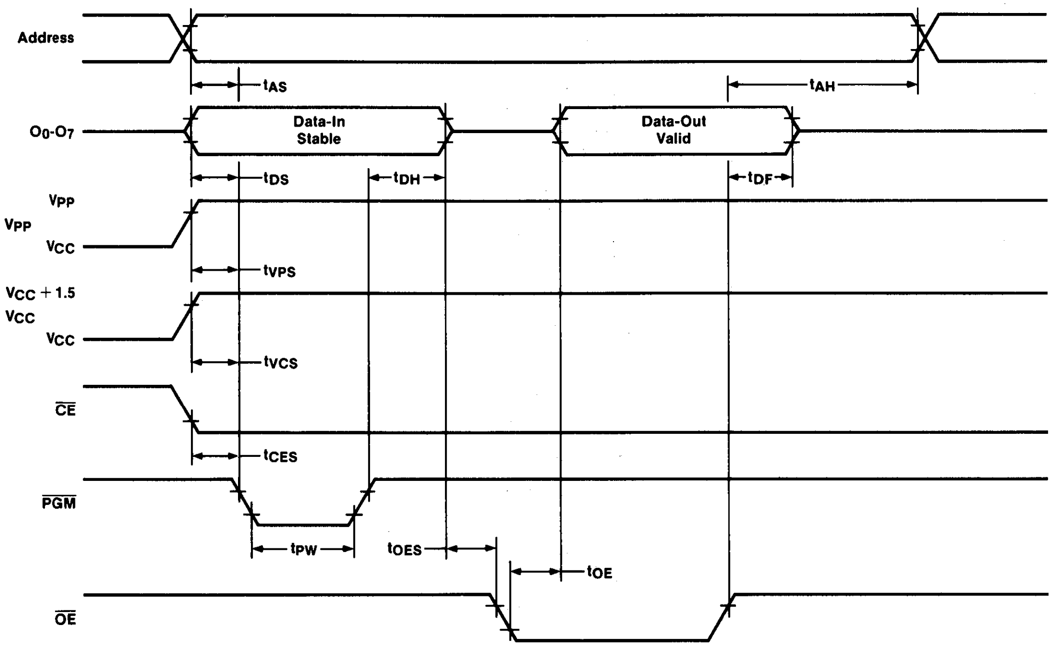


Figure 2. Page Programming Flowchart



Timing Waveforms (cont)

Byte Programming



Notes:

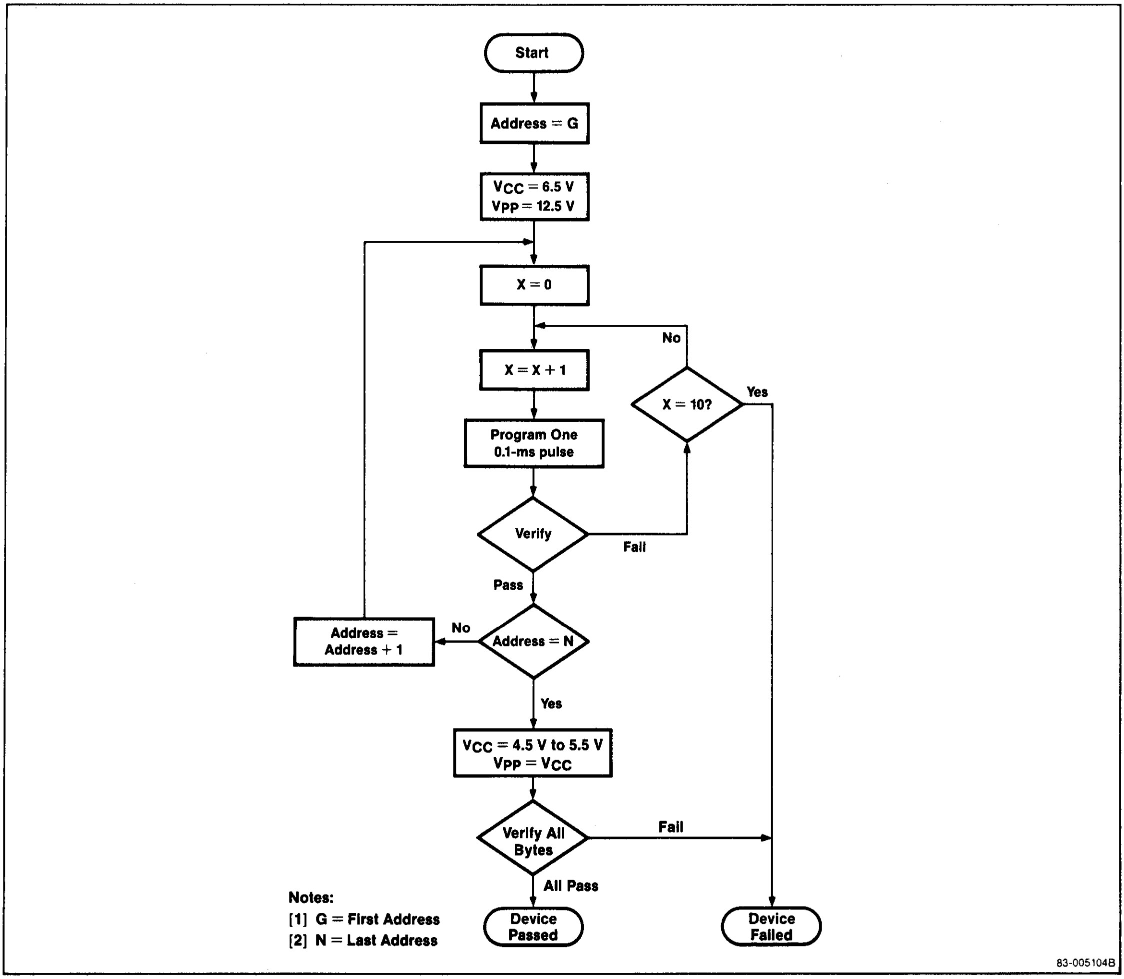
[1] V_{CC} must be applied before or simultaneously with V_{PP} and removed after or simultaneously with V_{PP}.

[2] V_{PP} must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to V_{PP} may affect device reliability.

83-005116B

Figure 3. Byte Programming Flowchart



NEC
NEC Electronics Inc.

μPD27C1024 65,536 x 16-BIT CMOS UV EPROM

Description

The μPD27C1024 is a 1,048,576-bit, ultraviolet erasable and electrically programmable ROM fabricated with an advanced CMOS process for substantial power savings. The device is organized as 64K words by 16 bits and operates from a single +5-volt ±10% power supply. All inputs and outputs are TTL-compatible.

The μPD27C1024 is available in a 40-pin cerdip with a quartz window.

Features

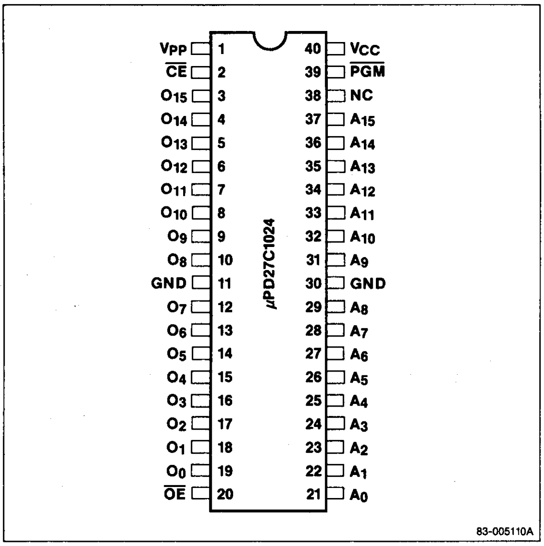
- ☐ 64K x 16-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ High-speed programming
- ☐ Low power dissipation
  - — 50 mA max (active)
  - — 100 μA max (standby)
- ☐ TTL-compatible inputs and outputs
- ☐ Single +5-volt ±10% power supply
- ☐ Three-state outputs
- ☐ Advanced CMOS technology
- ☐ 40-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD27C1024D-15	150 ns	40-pin cerdip
D-20	200 ns	
D-25	250 ns	

Pin Configuration

40-Pin Cerdip



Pin Identification

Symbol	Function
A_0-A_{15}	Address inputs
O_0-O_{15}	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage
NC	No connection

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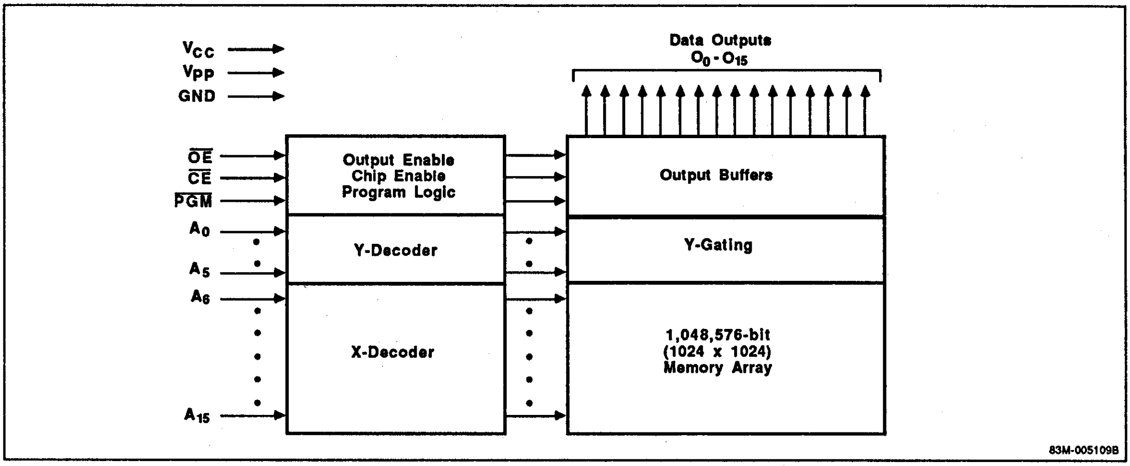
Block Diagram



Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	X	+5.0 V	+5.0 V	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6.0 V	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6.0 V	D_{OUT}
Program inhibit	V_{IH}	X	X	+12.5 V	+6.0 V	High-Z

Notes:

(1) X = V_{IL} or V_{IH}.

Capacitance

T_A = 25 °C; f = 1 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}		4	6	pF	$V_I = 0$ V
Output capacitance	C_{OUT}		8	12	pF	$V_O = 0$ V

Absolute Maximum Ratings

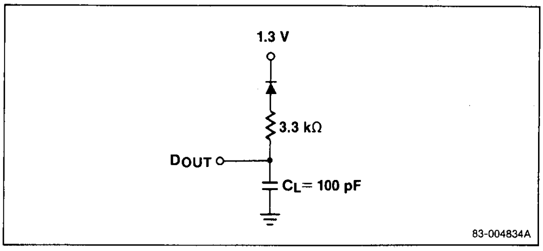
Operating temperature, T_{OPR}	−10 to +80 °C
Storage temperature, T_{STG}	−65 to +125 °C
Output voltage, V_O	−0.6 to +7.0 V
Input voltage, V_I	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Supply voltage, V_{CC}	−0.6 to +7.0 V
Supply voltage, V_{PP}	−0.6 to +13.5 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Read and Standby Modes $T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ±10%; $V_{PP} = V_{CC}$						
Input voltage, high	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	$V_{CC} - 0.7$			V	$I_{OH} = -100\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output leakage current	I_{LO}			10	μA	$V_O = 0$ to V_{CC}; $\overline{OE} = V_{IH}$
Input leakage current	I_{LI}			10	μA	$V_I = 0$ to V_{CC}
V_{PP} current	I_{PP}		1	100	μA	$V_{PP} = V_{CC}$
V_{CC} current (active)	I_{CCA1}			30	mA	$\overline{CE} = V_{IL}$; $V_I = V_{IH}$
	I_{CCA2}			50	mA	f = 5 MHz; $I_{OUT} = 0$ mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}		1	100	μA	$\overline{CE} = V_{CC}$; $V_I = 0$ to V_{CC}
Programming Modes $T_A = 25 \pm 5°C$; $V_{CC} = +6.0$ V ±0.25; $V_{PP} = +12.5$ V ±0.3						
Input voltage, high	V_{IH}	2.0		$V_{CC} + 0.3$	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	$V_I = V_{IL}$ or V_{IH}
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
V_{PP} current	I_{PP}			100	mA	$\overline{CE} = \overline{PGM} = V_{IL}$
V_{CC} current	I_{CC}			30	mA	

Figure 1. Loading Conditions Test Circuit



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AC Characteristics

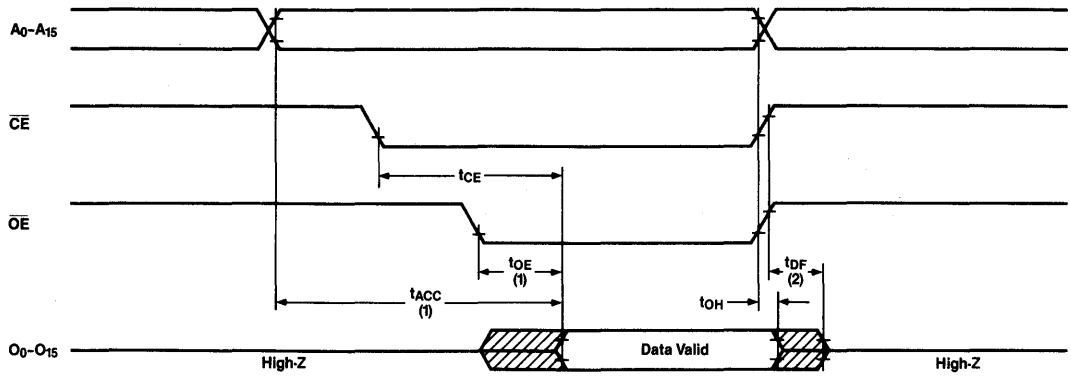
Parameter	Symbol	μPD27C1024-15 Min	μPD27C1024-15 Max	μPD27C1024-20 Min	μPD27C1024-20 Max	μPD27C1024-25 Min	μPD27C1024-25 Max	Unit	Test Conditions
Read and Standby Modes $T_A = 0$ to $+70°C$; $V_{CC} = +5.0$ V ±10%; $V_{PP} = V_{CC}$									
Address to output delay	t_{ACC}		150		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}		75		75		100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	t_{DF}	0	60	0	60	0	85	ns	$\overline{CE} = V_{IL}$
Output hold from address, $\overline{CE}$, or $\overline{OE}$, whichever transition occurs first	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
Programming Modes $T_A = 25 \pm 5°C$; $V_{CC} = +6.0$ V ±0.25; $V_{PP} = +12.5$ V ±0.3									
Address setup time	t_{AS}	2		2		2		μs	
$\overline{OE}$ setup time	t_{OES}	2		2		2		μs	
Data setup time	t_{DS}	2		2		2		μs	
Address hold time	t_{AH}	2		2		2		μs	
Data hold time	t_{DH}	2		2		2		μs	
$\overline{OE}$ to output float time	t_{DF}	0	130	0	130	0	130	ns	
V_{PP} setup time	t_{VPS}	2		2		2		μs	
V_{CC} setup time	t_{VCS}	2		2		2		μs	
Initial program pulse width	t_{PW}	0.095	0.105	0.095	0.105	0.095	0.105	ms	
Overprogram pulse width	t_{OPW}	0.38	4.2	0.38	4.2	0.38	4.2	ms	
$\overline{CE}$ setup time	t_{CES}	2		2		2		μs	
$\overline{OE}$ to output delay	t_{OE}		150		150		150	ns	

Notes:

(1) See figure 1 for output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 V and 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V.

Timing Waveforms

Read Mode

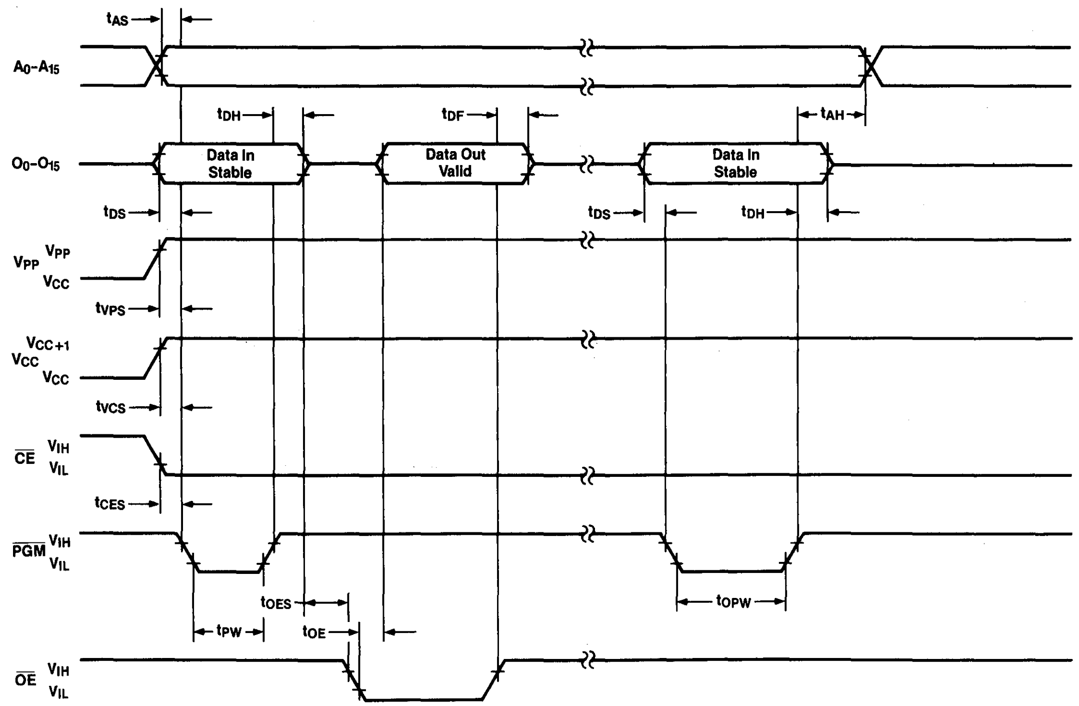


Note:
1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read cycles without affecting t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

83-004063B

Timing Waveforms (cont)

Programming Mode



Note:
1. V_{CC} must be applied before or simultaneously with V_{PP} and removed after or simultaneously with V_{PP}.
2. V_{PP} must not be greater than +13 V, including overshoot.

83-004064B

Programming Operation

High-Speed Programming

Begin programming by erasing all data; this places all bits in the high-level (1) state. Enter data by programming a low-level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the 16 output pins. Raise V_{CC} to +6 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V. Apply a 0.1-ms (±5%) pulse to $\overline{PGM}$ as shown in the pertinent timing waveform. The bit is verified and the program/no-program decision is made. If the bit is not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times. If the bit is programmed within 10 tries, apply an additional over-program pulse of "x" ms (where "x" equals 0.4 multiplied by the number of tries). If the bit is not programmed in 10 tries, apply another pulse of 4 ms. If the bit is not programmed at this stage, reject the device as a failure. If the bit is programmed, input the next address and repeat the procedure until all addresses are programmed.

Program Inhibit

Use this option to program multiple μPD27C1024s connected in parallel. All like inputs (except $\overline{CE}$ or $\overline{PGM}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{CE}$ input of the μPD27C1024 to be programmed. Applying a high level to the $\overline{CE}$ or $\overline{PGM}$ input of the other devices prevents them from being programmed.

Program Verification

Verification of the programmed bits to determine that the data was correctly programmed can be performed with $\overline{CE}$ and $\overline{OE}$ at low levels and $\overline{PGM}$ at a high level.

Erasure

Erase data on the μPD27C1024 by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by 254-nm ultraviolet rays. A lighting level of 15 W•sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity multiplied by exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C1024 within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

μPD27C2001 262,144 x 8-BIT CMOS UV EPROM

Description

The μPD27C2001 is a 2,097,152-bit ultraviolet erasable EPROM fabricated with double-polysilicon CMOS technology for a substantial savings in both operating and standby power. The device is organized as 262,144 words by 8 bits and operates from a single +5-volt power supply.

The μPD27C2001 has a single-location programming feature, three-state outputs, and fully TTL-compatible inputs and outputs. It also has a program voltage (V_{PP}) of 12.5 volts and is available in a 32-pin cerdip with a quartz window.

Features

- □ 262,144-word by 8-bit organization
- □ Ultraviolet erasable and electrically programmable
- □ High-speed page or byte programming
- □ Low power dissipation
  - — 30 mA (active)
  - — 100 μA (standby)
- □ TTL-compatible I/O for reading and programming
- □ Single +5-volt power supply
- □ Double-polysilicon CMOS technology
- □ 32-pin cerdip packaging with a quartz window
- □ JEDEC-compatible pinout

Ordering Information

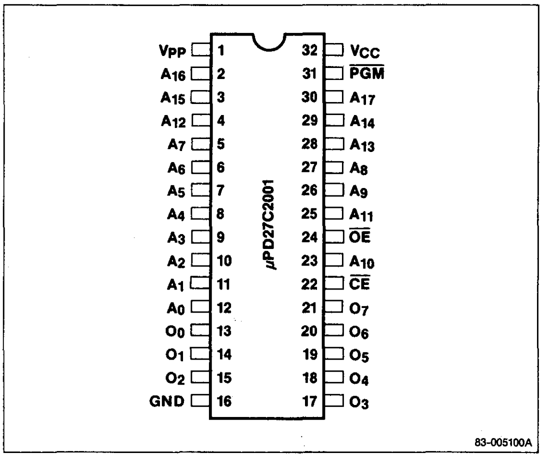
Part Number	Access Time (max)	Package
μPD27C2001D-15	150 ns	32-pin cerdip with quartz window
D-17	170 ns	
D-20	200 ns	

Pin Identification

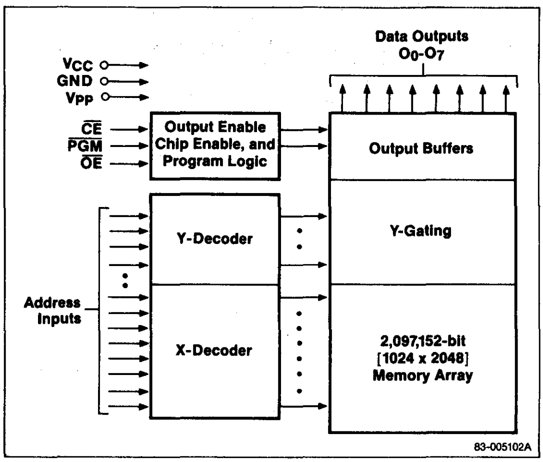
Symbol	Function
A_0-A_{17}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Program
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage

Pin Configuration

32-Pin Cerdip



Block Diagram



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Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +80°C
Storage temperature, T_{STG}	−65 to +125°C
Program voltage, V_{PP}	−0.6 to +13.5 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A =25°C; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			14	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}			16	pF	V_{OUT} = 0 V

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC} ±0.6

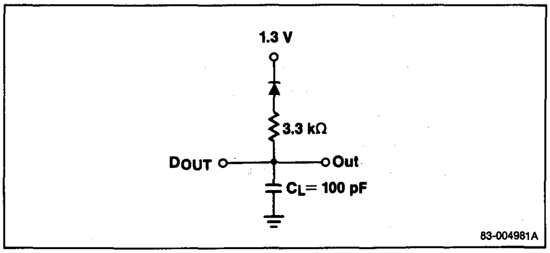
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Read, Output Disable, and Standby Modes						
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			30	mA	f = 6.7 MHz; I_{OUT} = 0 mA
Standby supply current	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}		1	100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}
Program voltage current	I_{PP}		1	100	μA	V_{PP} = V_{CC}

DC Characteristics (cont)

T_A = +25 ±5°C; V_{CC} = +6.5 ±0.25 V; V_{PP} = +12.5 ±0.3 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
All Program Modes						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP}			50	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Figure 1. Loading Conditions Test Circuit



Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (Note 2)	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5.0 V	+5.0 V	D_{OUT}
Output disable	V_{IL}	V_{IH}	X	+5.0 V	+5.0 V	High-Z
Standby	V_{IH}	X	X	+5.0 V	+5.0 V	High-Z
Page data latch	V_{IH}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{IN}
Page program	V_{IH}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	High-Z
Program verify	V_{IL}	V_{IL}	V_{IH}	+12.5 V	+6.5 V	D_{OUT}
Byte program	V_{IL}	V_{IH}	V_{IL}	+12.5 V	+6.5 V	D_{IN}
Program inhibit	X	V_{IL}	V_{IL}	+12.5 V	+6.5 V	High-Z
	X	V_{IH}	V_{IH}			

Notes:

(1) "X" can be either V_{IL} or V_{IH}.

(2) In read operation, $\overline{PGM}$ must be set to V_{IH} at all times or switched from V_{IL} to V_{IH} at least 2 μs before $\overline{OE}$ or $\overline{CE}$ becomes V_{IH}.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC}

Parameter	Symbol	Limits μPD27C2001-15 Min	Max	μPD27C2001-17 Min	Max	μPD27C2001-20 Min	Max	Unit	Test Conditions
Read and Standby Modes									
Address to output delay	t_{ACC}		150		170		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		150		170		200	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}		70		70		75	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ high to data output float delay	t_{DF}	0	55	0	55	0	60	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Address to output hold time	t_{OH}	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes:

(1) See figure 1 for output load; input rise and fall times ≤ 20 ns; input pulse levels = 0.45 V and 2.4 V; input and output timing measurement levels = 0.8 V and 2.0 V.

AC Characteristics (cont)

T_A = +25 ±5°C; V_{CC} = +6.5 ±0.25 V; V_{PP} = +12.5 ±0.3 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions (Note 1)
Page Data Latch, Page Program, Program Verify, and Program Inhibit Modes						
Address setup time	t_{AS}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
	t_{AHL}	2			μs	
	t_{AHV}	0			μs	
Data hold time	t_{DH}	2			μs	
Output enable to output float delay	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
Program pulse width	t_{PW}	0.095	0.1	0.105	ms	
V_{CC} setup time	t_{VCS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
$\overline{OE}$ hold time	t_{OEH}	2			μs	
$\overline{CE}$ hold time	t_{CEH}	2			μs	
$\overline{OE}$ pulse width during data latch	t_{LW}	1			μs	
$\overline{PGM}$ setup time	t_{PGMS}	2			μs	
$\overline{CE}$ setup time	t_{CES}	2			μs	
Data valid from $\overline{OE}$	t_{OE}			150	ns	

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions (Note 1)
Byte Programming Mode						
Address setup time	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data setup time	t_{DS}	2			μs	
Address hold time	t_{AH}	2			μs	
Data hold time	t_{DH}	2			μs	
$\overline{OE}$ to output float time	t_{DF}	0		130	ns	
V_{PP} setup time	t_{VPS}	2			μs	
V_{CC} setup time	t_{VCS}	2			μs	
Initial program pulse width	t_{PW}	0.095	0.1	0.105	ms	
$\overline{CE}$ setup time	t_{CES}	2			μs	
$\overline{OE}$ to output delay	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 V to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times ≤ 20 ns. See figure 1 for output load.

Programming Operation

Begin programming by erasing all data; this sets all bits at a high logic level (1). The μPD27C2001 is originally shipped in this condition. To enter data, program a low-level (0) TTL signal into the chosen location.

Address the first byte or page location and apply valid data at the eight output pins. Raise V_{CC} to +6.5 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V.

Byte Programming

For byte programming, $\overline{CE}$ should be set at 0 and $\overline{OE}$ at 1 to start programming at the initial address. Apply a 0.1-ms program pulse to $\overline{PGM}$ as shown in the byte programming portion of the timing waveforms. Set $\overline{OE}$ to 0 to verify the eight bits prior to making a program/no program decision. If the byte is not programmmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next address. If the bits are not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 ±10% V and verify all data again.

Page Programming

For page programming, $\overline{CE}$ and $\overline{PGM}$ should be set to 1. $\overline{OE}$ pulses low four times to latch the addressed 4-byte, one-page data. Subsequently, $\overline{CE}$ and $\overline{OE}$ should be set to a high level and a 0.1-ms program pulse applied to $\overline{PGM}$ as shown in the page programming portion of the timing waveforms. Verify the data prior to making a program/no program decision. If all four bytes of page data are not programmed, apply another 0.1-ms pulse to $\overline{PGM}$, up to a maximum of 10 times, and input the next page address. If the page is not programmed in 10 tries, reject the device as a program failure.

After all addresses are programmed, lower both V_{CC} and V_{PP} to +5.0 V ±10% and verify all data again.

Program Inhibit

Use the programming inhibit option to program multiple μPD27C2001s connected in parallel. All like inputs except $\overline{PGM}$ and $\overline{OE}$ may be common. Program individual devices by applying a low-level TTL pulse to the $\overline{PGM}$ pin of the device to be programmed. Applying a high-level signal to the $\overline{PGM}$ pins of the other devices prevents them from being programmed.

Program Verification

To verify that the device is correctly programmed, normal read operation can be used with a logic level 1 applied to the $\overline{PGM}$ pin and a logic level 0 applied to the $\overline{CE}$ and $\overline{OE}$ pins of the device to be verified. A logic level 1 should be applied to the $\overline{CE}$ and $\overline{OE}$ pins of all other devices.

Erasure

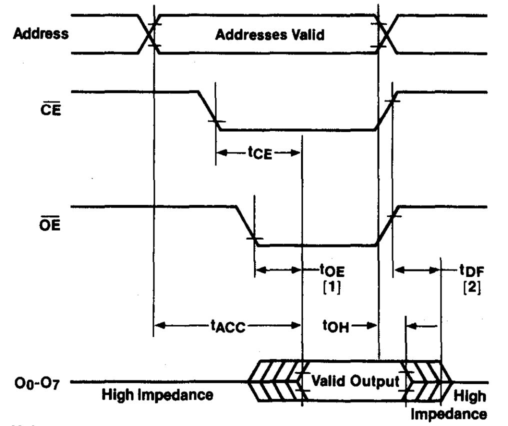
Erase data on the μPD27C2001 by exposing it to light with a wavelength shorter than 400 nm. Since exposure to direct sunlight or room-level fluorescent light could also erase the data, mask the window to prevent unintentional erasure by ultraviolet rays. Opaque labels are supplied with every device.

Data is typically erased by ultraviolet rays with a wavelength of 254 nm. A minimum integrated dose of 15 W-sec/cm^2 (ultraviolet lighting intensity multiplied by exposure time) is required to completely erase written data.

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C2001 within 2.5 cm of the lamp tubes and remove any filter on the lamp.

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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Timing Waveforms (cont)

Page Programming

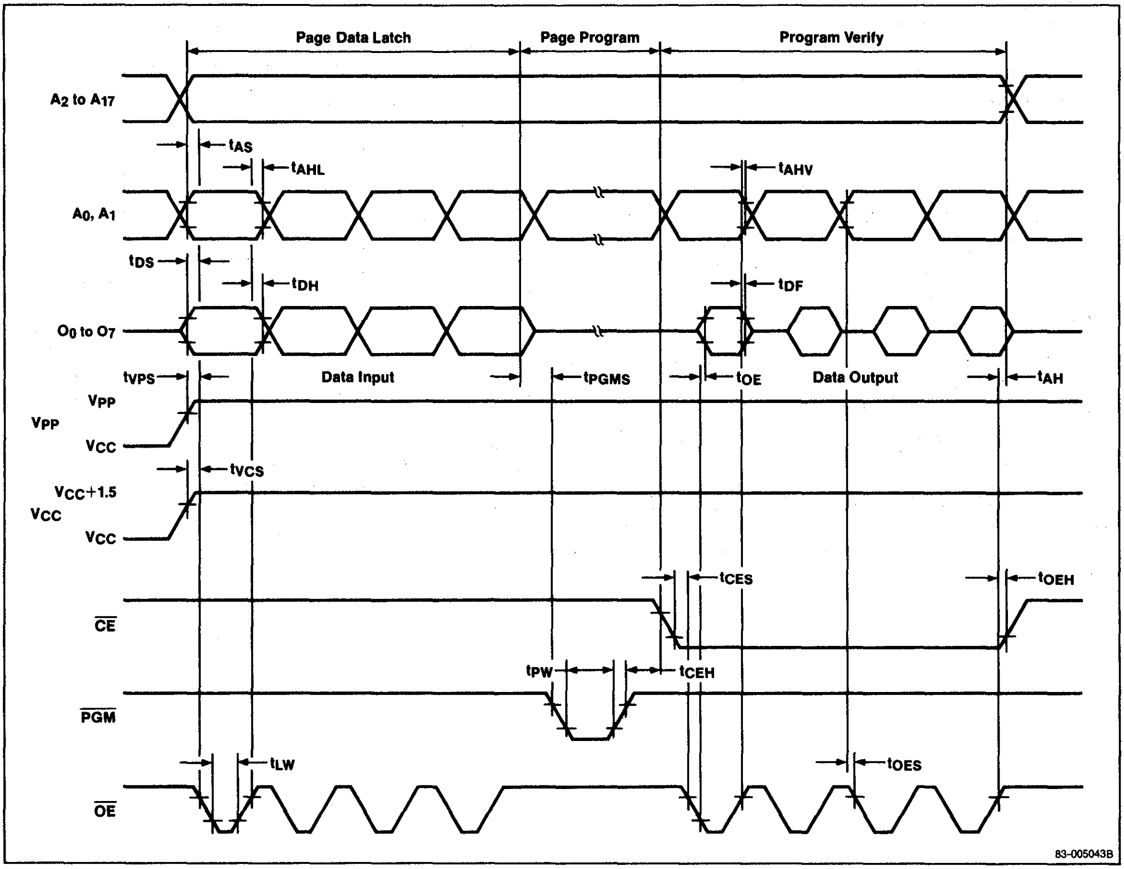
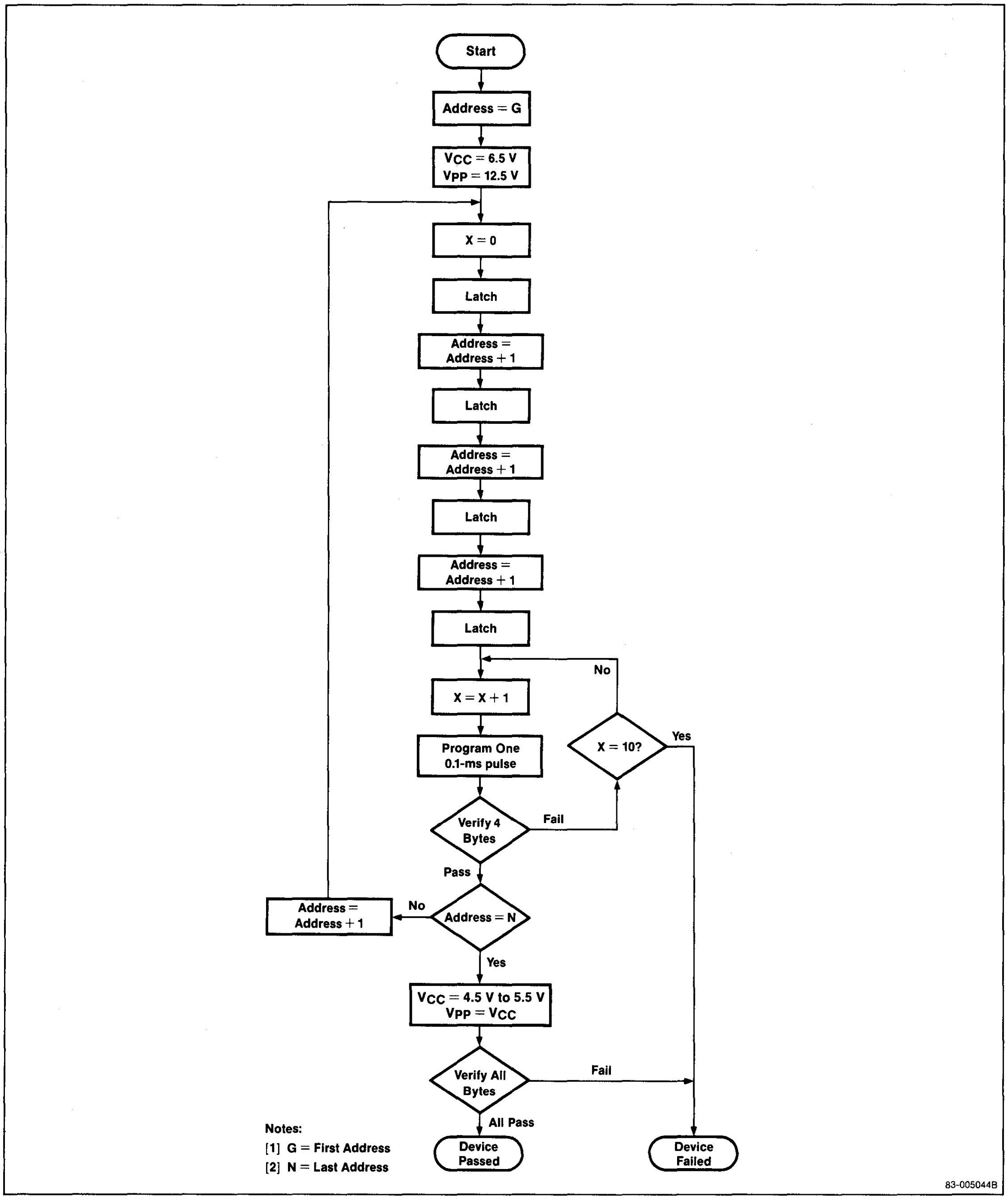
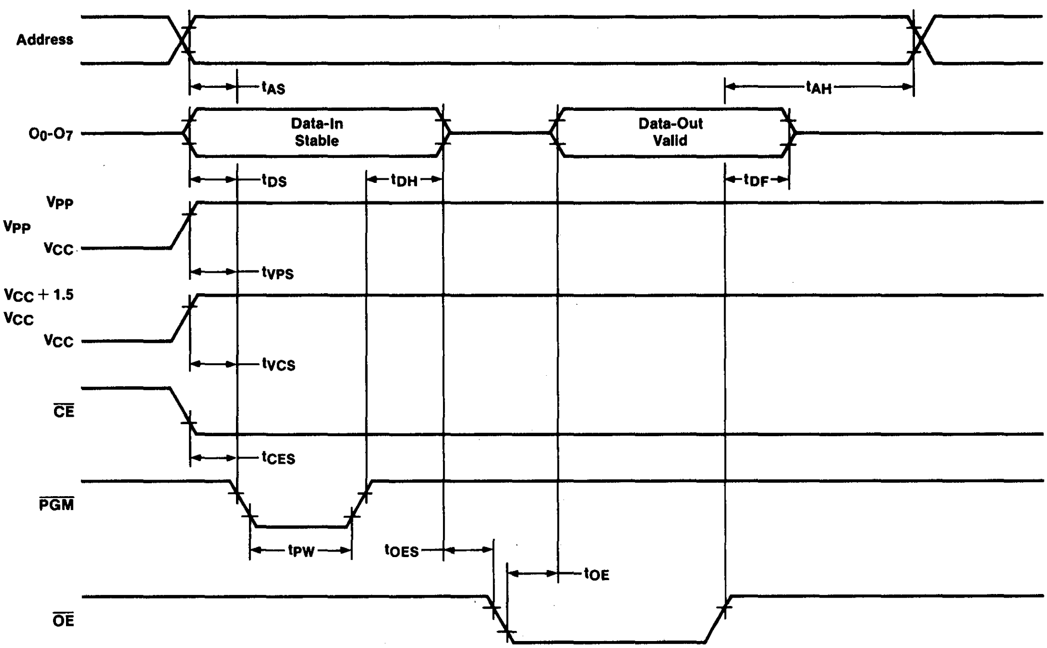


Figure 2. Page Programming Flowchart



Timing Waveforms (cont)

Byte Programming



Notes:

[1] V_{CC} must be applied before or simultaneously with Vpp and removed after or simultaneously with Vpp.

[2] Vpp must not be greater than +13.5 V, including overshoot.

[3] Removing and reinserting the device while a voltage of 12.5 V is applied to Vpp may affect device reliability.

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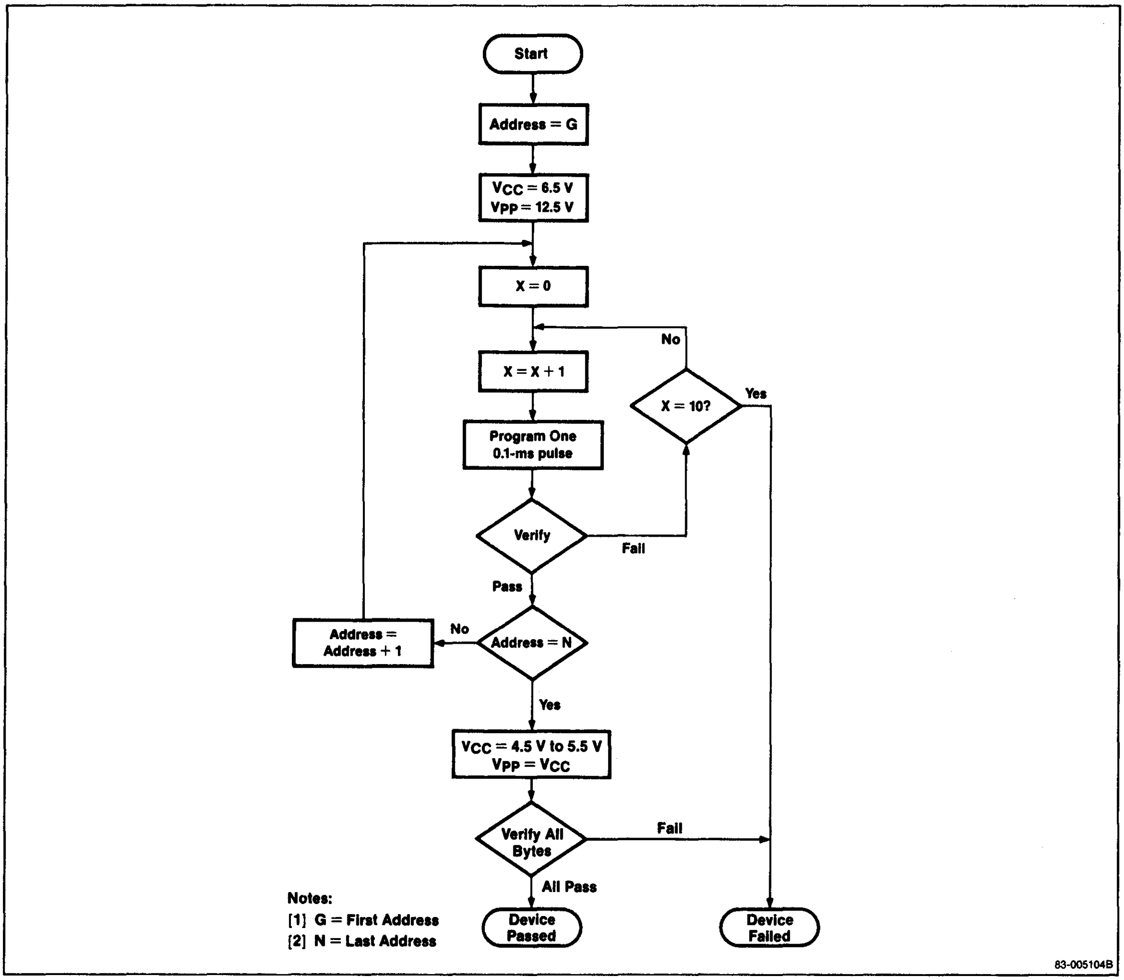
Figure 3. Byte Programming Flowchart



μPD28C04 512 x 8-BIT CMOS EEPROM

PRELIMINARY INFORMATION

Description

The μPD28C04 is a 4,096-bit (512 x 8-bit), electrically erasable and programmable read-only memory (EEPROM). The device is fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C04 provides a $\overline{\text{DATA}}$ polling function to indicate the precise end of write cycles. Additional functions include chip erase, auto erase and programming.

The μPD28C04 is available in standard 24-pin plastic DIP or miniflat packaging.

Features

- □ Fast access times: 200 ns and 250 ns maximum
- □ Single +5-volt power supply
- □ Chip erase feature
- □ Auto erase and programming: 10 ms max
- □ $\overline{\text{DATA}}$ polling verification
- □ Low power dissipation
  - — 17 mA max (active)
  - — 100 μA max (standby)
- □ Endurance: 100,000 erase/write cycles per byte
- □ TTL-compatible inputs and outputs
- □ Three-state outputs
- □ Advanced CMOS technology
- □ 24-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C04C-20	200 ns	24-pin plastic DIP
C-25	250 ns	
μPD28C04G-20	200 ns	24-pin plastic miniflat
G-25	250 ns	

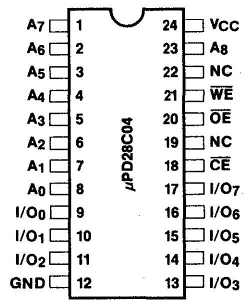
Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I		7	12	pF	$V_{IN} = 0$ V
Output capacitance	C_O			10	pF	$V_{OUT} = 0$ V

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0-A_8	Address inputs
I/O_0-I/O_7	Data inputs/outputs
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{I1}	−0.6 to +7.0 V
Input voltage, V_{I3} ($\overline{\text{OE}}$)	−0.6 to +16.5 V
Output voltage, V_O	−0.6 to +7.0 V
Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

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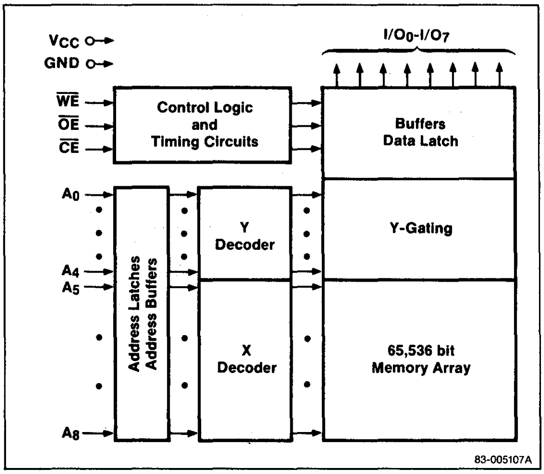
Block Diagram



Recommended DC Operating Conditions

T_A −40 to +85°C

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		$V_{CC}+0.3$	V
Input voltage, low	V_{IL}	−0.3		0.7	V

DC Characteristics

T_A −40 to +85°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	$I_{OH} = -400\ \mu A$
	V_{OH2}	$V_{CC} - 0.7$			V	$I_{OH} = -100\ \mu A$
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output leakage current	I_{LO}			10	μA	$V_{OUT} = 0$ to V_{CC}
Input leakage current	I_{LI}			10	μA	$V_{IN} = 0$ to V_{CC}
V_{CC} current (active)	I_{CCA1}			4.1	mA	$\overline{CE} = 0.1$ V; $\overline{OE} = V_{CC} - 0.1$ V
	I_{CCA2}			17	mA	f = 5 MHz; $I_{OUT} = 0$ mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}			100	μA	$\overline{CE} = V_{CC}$; $V_{IN} = 0$ to V_{CC}

AC Characteristics

$T_A = -40$ to $+85\,°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	μPD28C04-20 Min	μPD28C04-20 Max	μPD28C04-25 Min	μPD28C04-25 Max	Unit	Test Conditions
Read Mode							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}	10	80	10	100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	65	0	80	ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$
Output hold	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$ (Note 2)

Parameter	Symbol	Limits Min	Limits Max	Unit
Write Mode				
Write cycle time	t_{WC}	10		ms
Address setup time	t_{AS}	10		ns
Address hold time	t_{AH}	200		ns
Write setup time	t_{CS}	0		ns
Write hold time	t_{CH}	0		ns
$\overline{CE}$ pulse width	t_{CW}	150		ns
$\overline{OE}$ high setup time	t_{OES}	10		ns
$\overline{OE}$ high hold time	t_{OEH}	10		ns
$\overline{WE}$ pulse width	t_{WP}	150		ns
$\overline{WE}$ high hold time	t_{WPH}	50		ns
Data valid time	t_{DV}		300	ns
Data setup time	t_{DS}	100		ns
Data hold time	t_{DH}	20		ns
Chip Erase Mode				
$\overline{CE}$ setup time	t_{CS}	500		ns
$\overline{OE}$ setup time	t_{OES}	500		ns
Data setup time	t_{DS}	500		ns
Data hold time	t_{DH}	100		ns
$\overline{WE}$ pulse width	t_{WP}	10		ms
$\overline{CE}$ hold time	t_{CH}	5		μs
$\overline{OE}$ hold time	t_{OEH}	$t_{CH} + 3$		μs

Notes:

(1) See figure 1 for the output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 V and 2.4 V; timing measurement reference levels = 0.8 V and 2.0 V for both inputs and outputs.

(2) Output hold time is specified from address, $\overline{OE}$ or $\overline{CE}$, whichever goes invalid first.

Truth Table

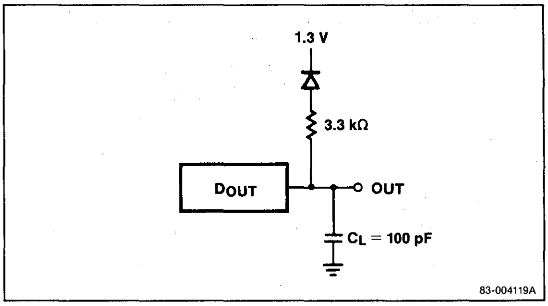
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0-I/O_7	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

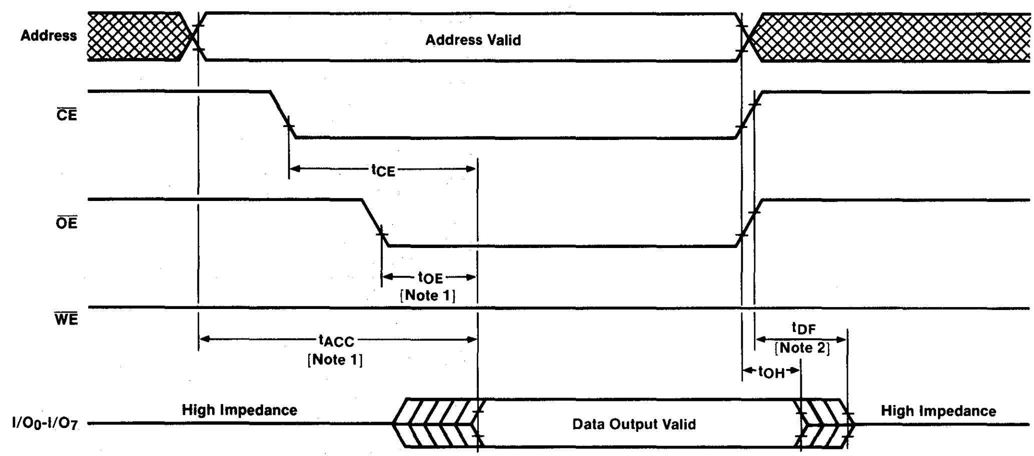
(2) $V_{IHH} = +15$ V ±0.5.

Figure 1. Output Load



Timing Waveforms

Read Cycle



Notes:

[1] For the read mode, $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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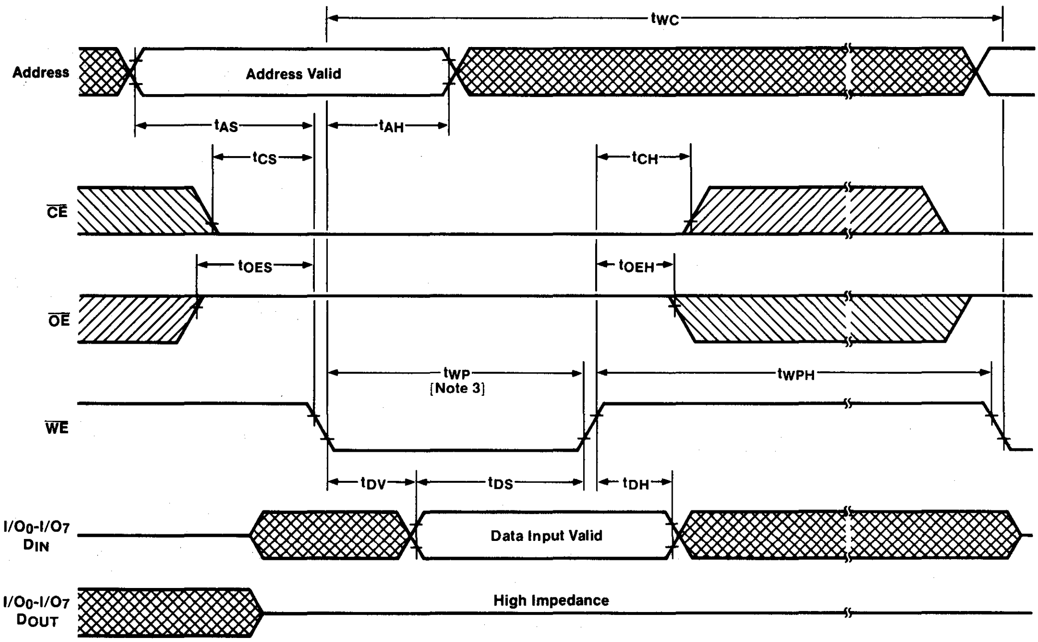
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] The write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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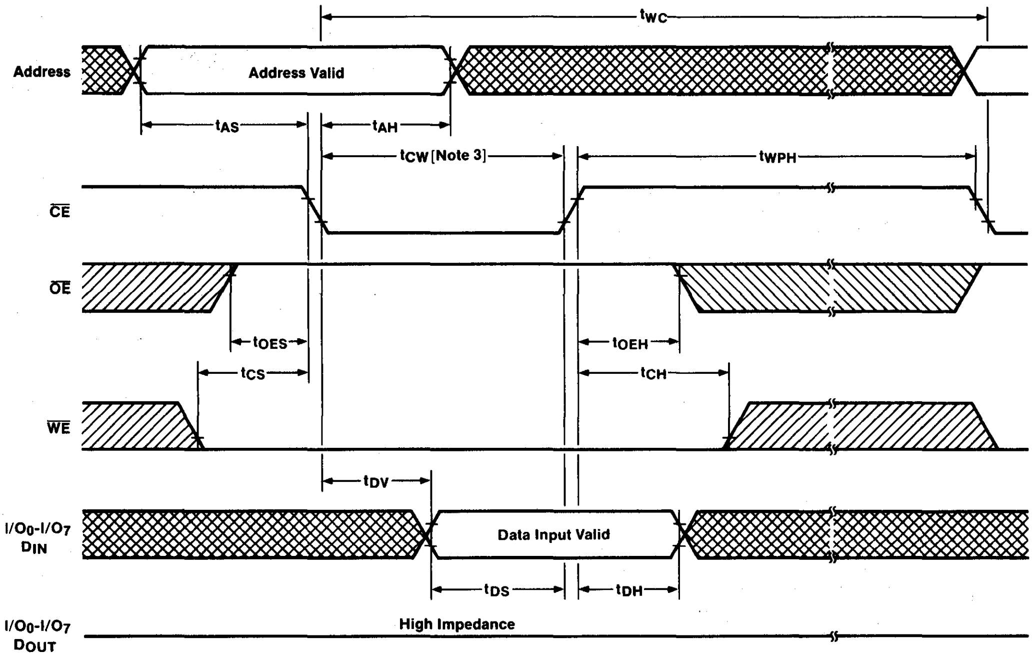
Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] The write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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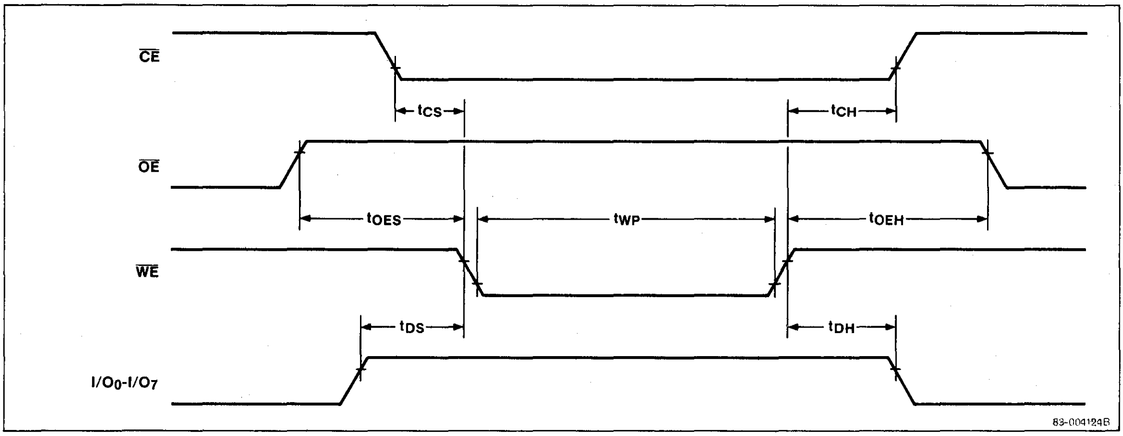
Timing Waveforms (cont)

Chip Erase Cycle



Device Operation

Read Mode

Both $\overline{CE}$ and $\overline{OE}$ must be at V_{IL} in order to read stored data. While the device is in read mode, bringing either of these inputs to V_{IH} will place the outputs in a state of high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Mode

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C04 in write mode. The write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, internal circuits assume all timing control and the byte being addressed is automatically erased and then programmed. The operation is completed within a write cycle time (t_{WC}) of 10 ms.

Chip Erase Mode

All bytes of the μPD28C04 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} after $\overline{OE}$ has been increased to V_{IHH} (15 ±0.5 V). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase operation begins.

$\overline{\text{DATA}}$ Polling Feature

This feature supports system software by indicating the precise end of byte write cycles. $\overline{\text{DATA}}$ polling can be used to reduce the total programming time of the μPD28C04 to a minimum value which varies with the system environment.

While the internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write operation is complete, a read cycle will result in true data being output on I/O_7.

Write Protect Functions

The μPD28C04 provides three functions to prevent invalid write operations.

- Noise immunity: write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage level detection: write operation is inhibited when V_{CC} is 2.5 V or less.
- Write protection logic: if $\overline{OE}$ is held low, or $\overline{CE}$ or $\overline{WE}$ is held high during power-on or power-off of the V_{CC} supply voltage, then write operation is inhibited.

NEC
NEC Electronics Inc.

μPD28C64 8192 x 8-BIT CMOS EEPROM

Description

The μPD28C64 is a 65,536-bit (8192 x 8-bit), electrically erasable and programmable read-only memory (EEPROM). The device is fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C64 provides a $\overline{\text{DATA}}$ polling function to indicate the precise end of write cycles. Additional functions include chip erase, auto erase and programming, and 32-byte page write operations.

The μPD28C64 is available in a standard 28-pin plastic DIP.

Features

- ☐ Single +5-volt power supply
- ☐ Chip erase mode
- ☐ Auto erase and programming mode: 10 ms max
- ☐ Page programming mode: 32-byte
- ☐ $\overline{\text{DATA}}$ polling verification
- ☐ Low power dissipation
  - — 50 mA max (active)
  - — 100 μA max (standby)
- ☐ Endurance: 100,000 erase/write cycles per byte
- ☐ Silicon signature
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Advanced CMOS technology
- ☐ 28-pin plastic DIP

Ordering Information

Part Number	Access Time (max)	Package
μPD28C64C-20	200 ns	28-pin plastic DIP
C-25	250 ns	

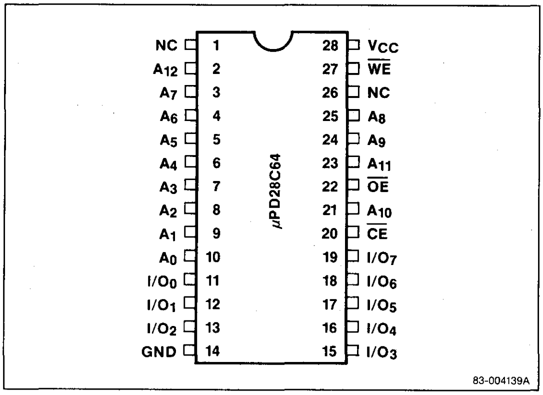
Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage	−0.6 to +7.0 V
Input voltage (A_9)	−0.6 to +13.5 V
Input voltage ($\overline{OE}$)	−0.6 to +16.5 V
Output voltage	−0.6 to +7.0 V
Operating temperature	−10 to +85°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under Recommended Operating Conditions.

Pin Configuration

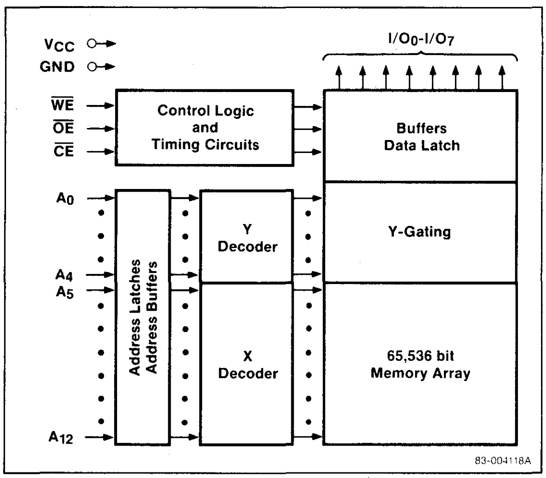
28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{12}	Address inputs
I/O_0-I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



8

Capacitance

$T_A = 25°C$; f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I		7	12	pF	$V_{IN} = 0$ V
Output capacitance	C_O			10	pF	$V_{OUT} = 0$ V

Recommended Operating Conditions

$T_A = 0$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		$V_{CC} + 0.3$	V
Input voltage, low	V_{IL}	−0.3		0.8	V

DC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	$I_{OH} = -400$ μA
	V_{OH2}	$V_{CC} - 0.7$			V	$I_{OH} = -100$ μA
Output voltage, low	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output leakage current	I_{LO}			10	μA	$V_{OUT} = 0$ to V_{CC}; $\overline{CE}$ or $\overline{OE} = V_{IH}$
Input leakage current	I_{LI}			10	μA	$V_{IN} = 0$ to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE} = V_{IL}$; $\overline{OE} = V_{IH}$
	I_{CCA2}			50	mA	f = 5 MHz; $I_{OUT} = 0$ mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE} = V_{IH}$
	I_{CCS2}			100	μA	$\overline{CE} = V_{CC}$; $V_{IN} = 0$ to V_{CC}

AC Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = 5.0$ V ±10%

Parameter	Symbol	μPD28C64-20 Min	μPD28C64-20 Max	μPD28C64-25 Min	μPD28C64-25 Max	Unit	Test Conditions
Read Mode							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	60	0	80	ns	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$
Output hold*	t_{OH}	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

*from address, $\overline{OE}$, or $\overline{CE}$, whichever transition occurs first

μPD28C64-20/25	Symbol	Min	Max	Unit
Write Mode				
Write cycle time	t_{WC}	10		ms
Address setup time	t_{AS}	10		ns
Address hold time	t_{AH}	200		ns
Write setup time	t_{CS}	0		ns
Write hold time	t_{CH}	0		ns
$\overline{CE}$ pulse width	t_{CW}	150		ns
$\overline{OE}$ high setup time	t_{OES}	10		ns
$\overline{OE}$ high hold time	t_{OEH}	10		ns
$\overline{WE}$ pulse width	t_{WP}	150		ns
$\overline{WE}$ high hold time	t_{WPH}	50		ns
Data valid time	t_{DV}		300	ns
Data setup time	t_{DS}	100		ns
Data hold time	t_{DH}	20		ns
Byte load cycle time	t_{BLC}	3	100	μs
Chip Erase Mode				
$\overline{CE}$ setup time	t_{CS}	500		ns
$\overline{OE}$ setup time	t_{OES}	500		ns
Data setup time	t_{DS}	500		ns
Data hold time	t_{DH}	100		ns
$\overline{WE}$ pulse width	t_{WP}	10		ms
$\overline{CE}$ hold time	t_{CH}	5		μs
$\overline{OE}$ hold time	t_{OEH}	$t_{CH} + 3$		μs

Notes:

(1) See figure 1 for the output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 V and 2.4 V; timing measurement reference levels = 0.8 V and 2.0 V for both inputs and outputs.

Truth Table

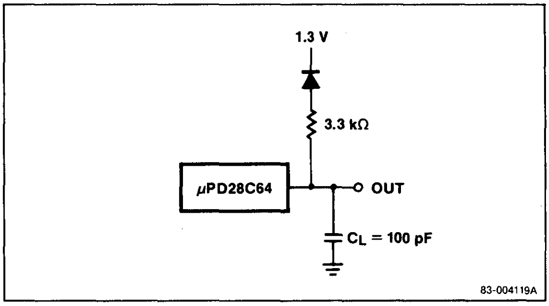
Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O_0-I/O_7	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

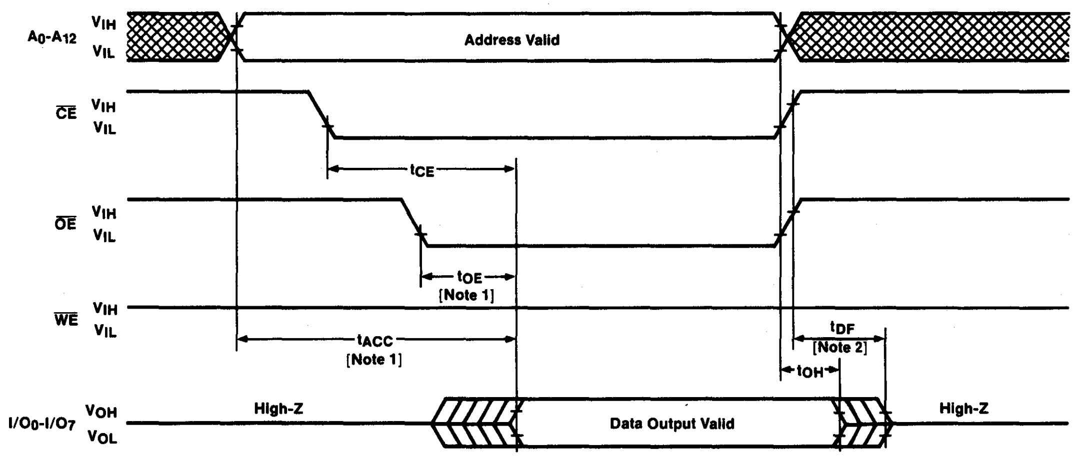
(2) $V_{IHH} = +15\ V\ -0.5\ V$.

Figure 1. Output Load



Timing Waveforms

Read Cycle



Notes:

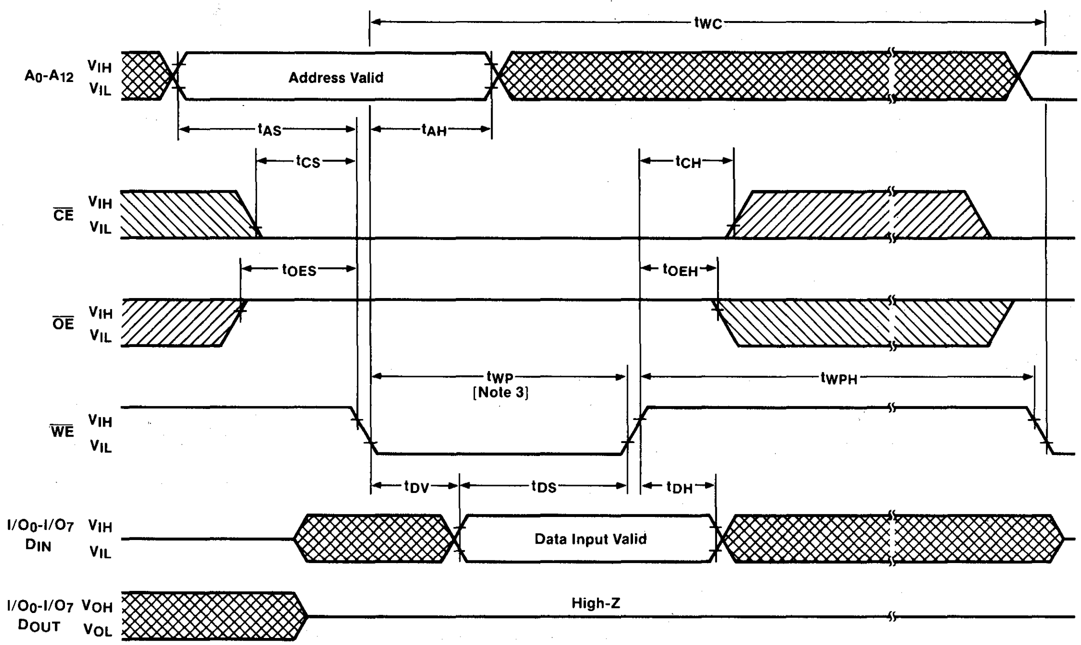
[1] For the read mode, $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

83-004120B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

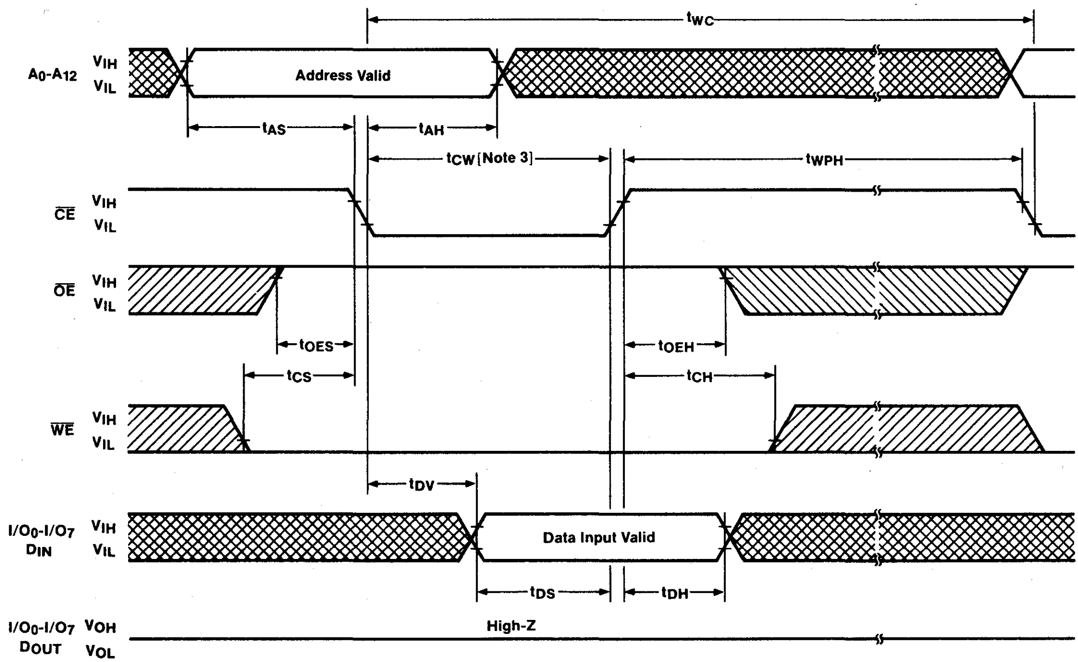
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] The write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83-004121B

Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] **The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.**

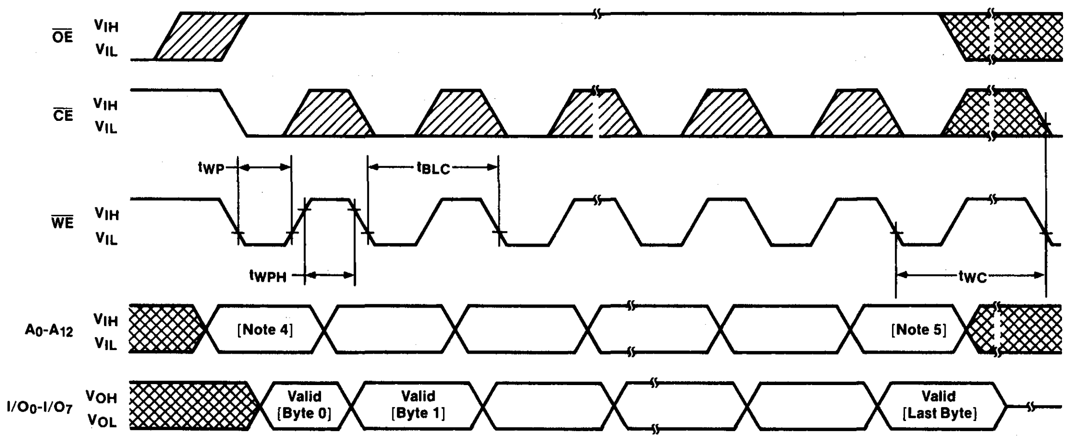
[2] **The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.**

[3] **The write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.**

83-004122B

Timing Waveforms (cont)

Page Mode Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

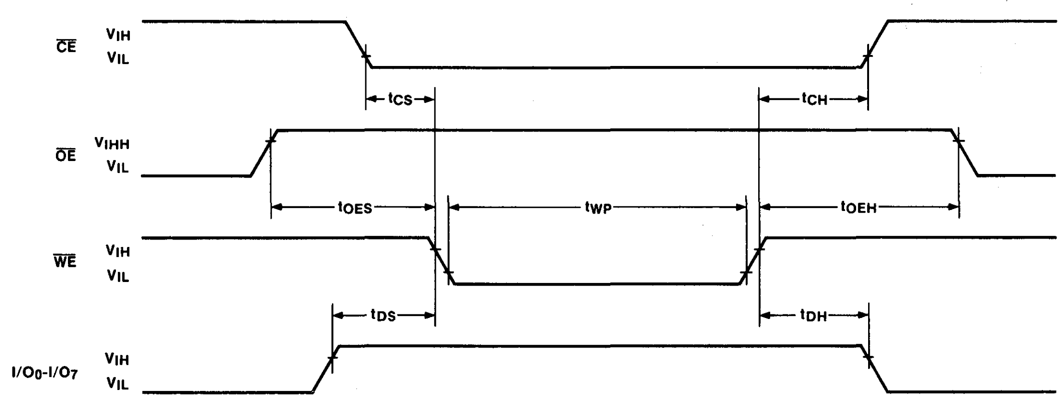
[3] The write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page mode write cycle. Address inputs A_5-A_{12} must be supplied for every byte load cycle and must remain the same throughout the page mode write cycle to prevent writes to an unknown address location. Address inputs A_0-A_4 are altered for each byte load cycle and determine the individual byte to be written within the page.

[5] A maximum of 32 bytes may be loaded in a single page mode write cycle.

83-004123B

Chip Erase Cycle



83-004124B

Device Operation

Read Mode

Both $\overline{CE}$ and $\overline{OE}$ must be at V_{IL} in order to read out stored data. While the device is in the read mode, bringing either of these inputs to V_{IH} will place the outputs in a state of high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Mode

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C64 in the write mode. The write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once the byte write operation has begun, internal circuits assume all timing control. The byte being addressed is automatically erased and then programmed. The operation is completed within a write cycle time (t_{WC}) of 10 ms.

Page Write Mode

This mode allows the μPD28C64 to be completely programmed in a much shorter time than by using only the byte write mode. By loading up to 32 bytes of data before the internal write operation programs all of these bytes simultaneously, the μPD28C64 can be completely written in a maximum of 2.6 seconds.

The page address is specified by the inputs A_5-A_{12}; once set, this address cannot be changed during a page write cycle. Within the page, address inputs A_0-A_4 can be used sequentially or in random order to specify individual bytes.

The beginning of a page write cycle is the same as a $\overline{WE}$-controlled byte write cycle. If the next falling edge of $\overline{WE}$ occurs within a byte load cycle time of 100 μs, the internal byte load register will be loaded with another byte of input data. This cycle can be repeated; a maximum of 32 bytes of data can be loaded. At any point in the sequence, if $\overline{WE}$ does not have a new falling edge within the byte load cycle time of 100 μs, the byte load operation will terminate and automatic erasing and programming operations will begin.

Chip Erase Mode

All bytes of the μPD28C64 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} after $\overline{OE}$ has been increased to V_{IHH} (15 V ±0.5 V). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase operation begins.

$\overline{\text{DATA}}$ Polling Feature

This feature supports system software by indicating the precise end of byte write and page write cycles. $\overline{\text{DATA}}$ polling can be used to reduce the total programming time of the μPD28C64 to a minimum value which varies with the system environment.

While the internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write operation is complete, a read cycle will result in true data being output on I/O_7.

Write Protect Functions

The μPD28C64 provides three functions to prevent invalid write operations.

- Noise immunity: write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage level detection: write operation is inhibited when V_{CC} is 2.5 V or less.
- Write protection logic: if $\overline{OE}$ is held low, or $\overline{CE}$ or $\overline{WE}$ is held high during power-on or power-off of the V_{CC} supply voltage, then write operation is inhibited.

NEC

MASK-PROGRAMMABLE ROMs

Section 9
Mask-Programmable ROMs

NEC
NEC Electronics Inc.

μPD23C1000A 131,072 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C1000A is a 131,072-word by 8-bit static ROM fabricated with CMOS silicon-gate technology. Designed to operate from a single +5-volt power supply, the device has three-state outputs and fully TTL-compatible inputs and outputs, and is available in 28-pin plastic DIP or miniflat packaging.

Features

- ☐ 131,072-word by 8-bit organization
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Low power dissipation
  - — 220 mW (active)
  - — 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1000AC	200 ns	28-pin plastic DIP
μPD23C1000AG	200 ns	28-pin plastic miniflat

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} +0.3 V
Output voltage, V_O	−0.3 V to V_{CC} +0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

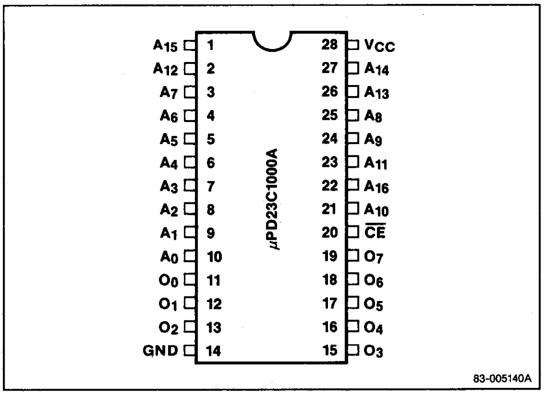
Capacitance

$T_A = 25°C$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Units	Test Conditions
Input capacitance	C_I			15	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

Pin Configuration

28-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
GND	Ground
V_{CC}	+5-volt power supply

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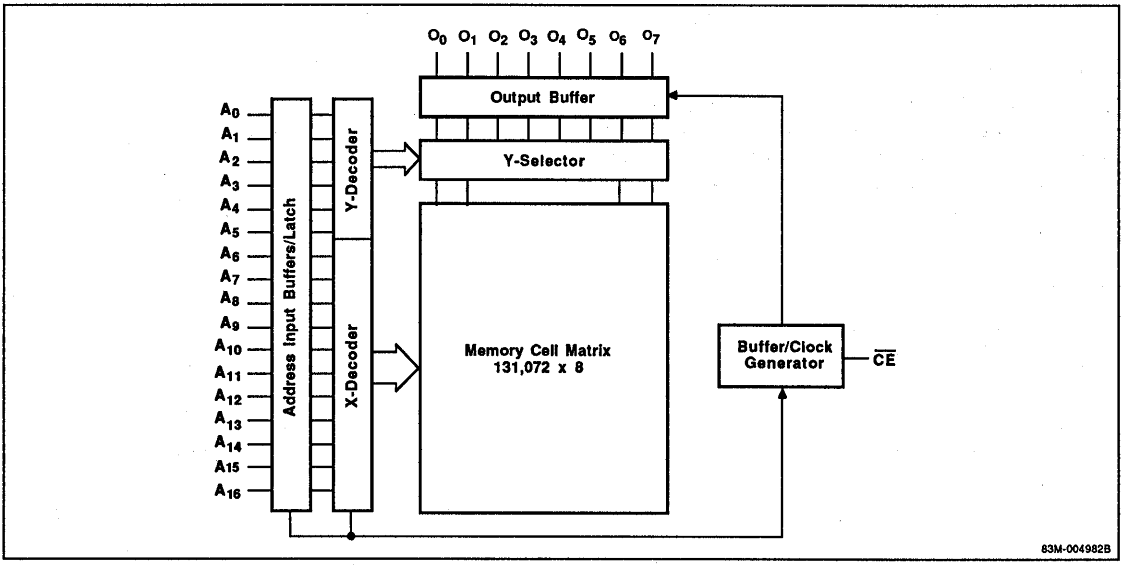
Block Diagram



DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2		V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = +2.5$ mA
Input leakage current, high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}			−10	μA	$V_I = 0$ V
Output leakage current, high	I_{LOH}			10	μA	$V_O = V_{CC}$ (chip deselected)
Output leakage current, low	I_{LOL}			−10	μA	$V_O = 0$ V (chip deselected)
Power supply current	I_{CC1}			40	mA	$\overline{CE} = V_{IL}$
	I_{CC2}			1.5	mA	$\overline{CE} = V_{IH}$ (standby)
	I_{CC3}			100	μA	$\overline{CE} = V_{CC} - 0.2$ V (standby)

AC Characteristics

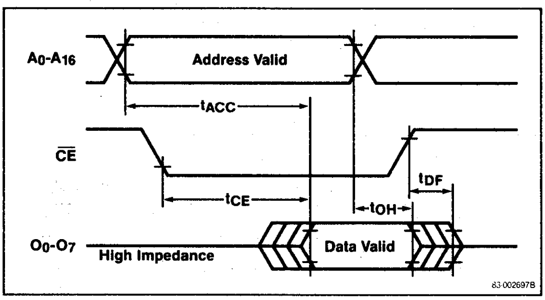
$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits Min	Max	Unit
Address access time	t_{ACC}		200	ns
Chip enable access time	t_{CE}		200	ns
Output hold time	t_{OH}	0		ns
Output disable time	t_{DF}	0	60	ns

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveform



μPD23C1000EA 131,072 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C1000EA is a 131,072-word by 8-bit static ROM fabricated with CMOS silicon-gate technology. Designed to operate from a single +5-volt power supply, the device has three-state outputs, fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 32-pin plastic DIP.

Features

- ☐ 131,072-word by 8-bit organization
- ☐ Fast access time: 200 ns maximum
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Low power dissipation
  - — 220 mW (active)
  - — 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1000EAC	200 ns	32-pin plastic DIP

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70 °C
Storage temperature, T_{STG}	−65 to +150 °C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

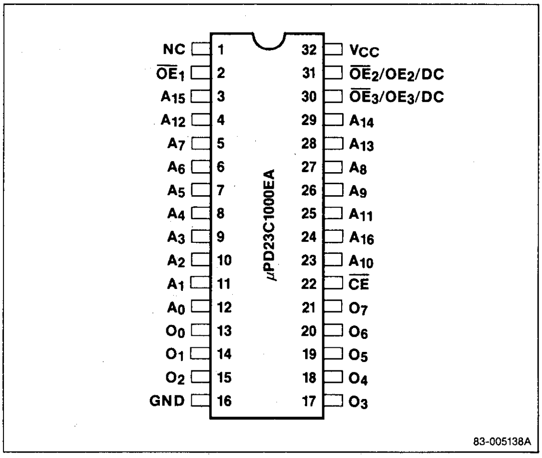
Capacitance

$T_A = 25$ °C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Units	Test Conditions
Input capacitance	C_I			15	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

Pin Configuration

32-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}_1$	Output enable 1
$\overline{OE}_2$/OE_2/DC	Output enable 2 (Note 1)
$\overline{OE}_3$/OE_3/DC	Output enable 3 (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care" (in the cases of $\overline{OE}_2$/OE_2/DC and $\overline{OE}_3$/OE_3/DC).

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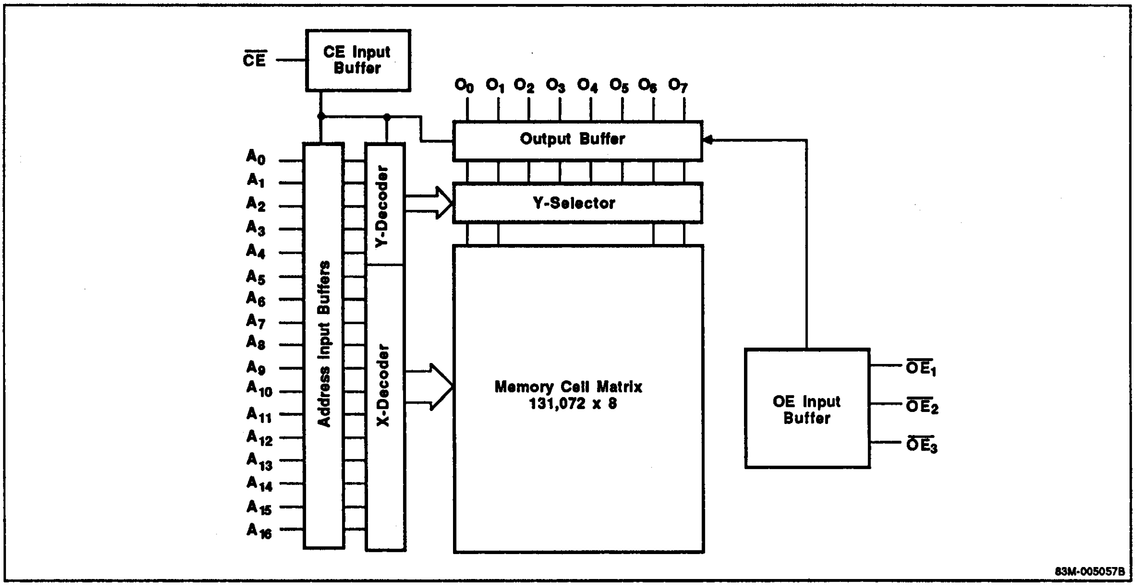
Block Diagram



DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

		Limits			
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2	V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3	0.8	V	
Output voltage, high	V_{OH}	2.4		V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}		0.4	V	$I_{OL} = +2.5\ mA$
Input leakage current, high	I_{LIH}		10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}		−10	μA	$V_I = 0\ V$
Output leakage current, high	I_{LOH}		10	μA	$V_O = V_{CC}$ (outputs disabled)
Output leakage current, low	I_{LOL}		−10	μA	$V_O = 0\ V$ (outputs disabled)
Power supply current	I_{CC1}		40	mA	$\overline{CE} = V_{IL}$
	I_{CC2}		1.5	mA	$\overline{CE} = V_{IH}$
	I_{CC3}		100	μA	$\overline{CE} = V_{CC} - 0.2\ V$

AC Characteristics

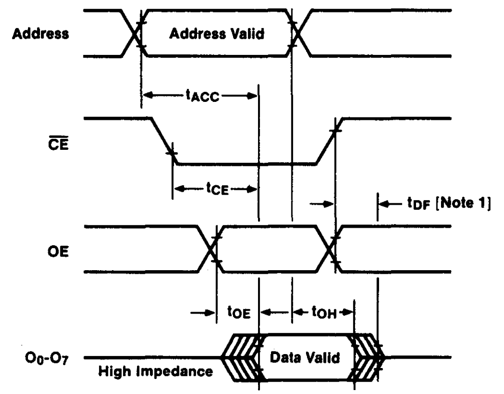
$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$ (Note 1)

		Limits			
Parameter	Symbol	Min	Typ	Max	Unit
Address access time	t_{ACC}			200	ns
Chip enable access time	t_{CE}			200	ns
Output enable access time	t_{OE}			100	ns
Output hold time	t_{OH}	0			ns
Output disable time	t_{DF}	0		60	ns

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveform



Note:
[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

83-004134A

9

NEC
NEC Electronics Inc.

μPD23C1001E 131,072 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C1001E is a 131,072-word by 8-bit static ROM fabricated with CMOS silicon-gate technology. Designed to operate from a single +5-volt power supply, the device has three-state outputs and fully TTL-compatible inputs and outputs, and is packaged in a 600-mil, 32-pin plastic DIP.

Features

- ☐ 131,072-word by 8-bit organization
- ☐ Fast access time: 200 ns maximum
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Low power dissipation
  - — 220 mW (active)
  - — 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C1001EC	200 ns	32-pin plastic DIP

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

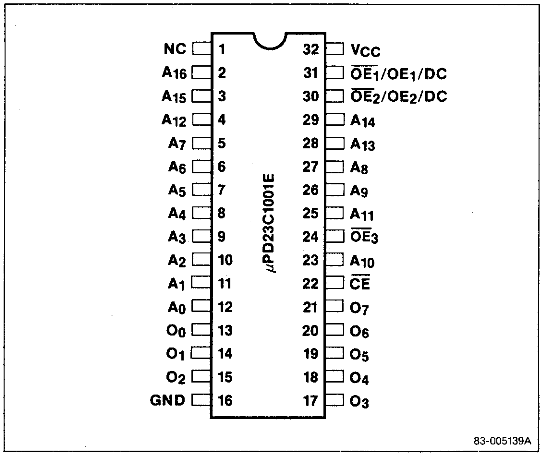
Capacitance

$T_A = 25°C$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Units	Test Conditions
Input capacitance	C_I			15	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

Pin Configuration

32-Pin Plastic DIP



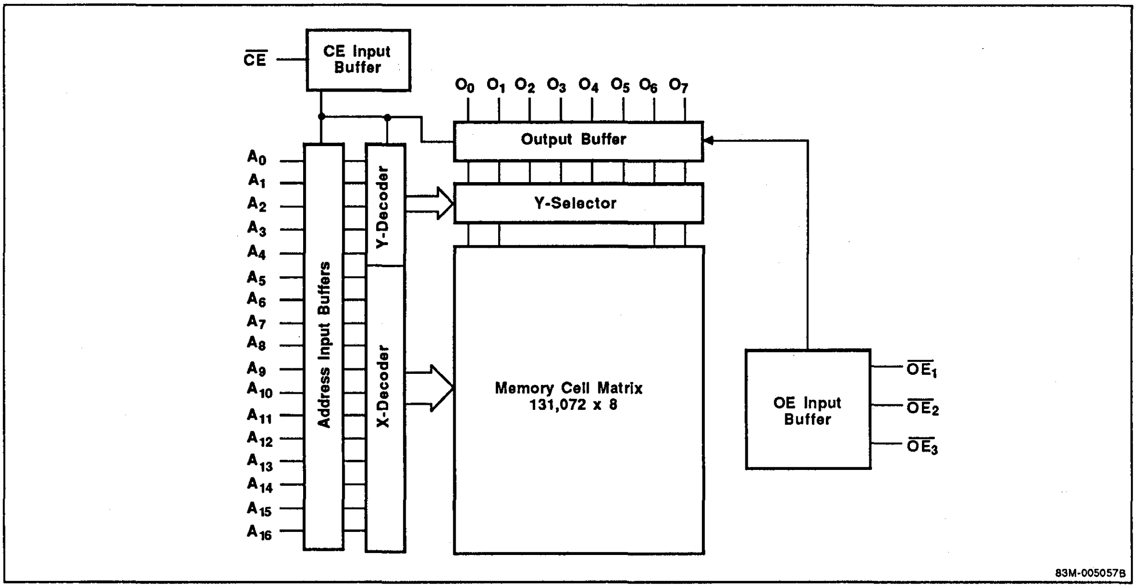
Pin Identification

Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}_1/OE_1/DC$	Output enable 1 (Note 1)
$\overline{OE}_2/OE_2/DC$	Output enable 2 (Note 1)
$\overline{OE}_3$	Output enable 3
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care" (in the cases of $\overline{OE}_1/OE_1/DC$ and $\overline{OE}_2/OE_2/DC$).

Block Diagram



DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2	V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3	0.8	V	
Output voltage, high	V_{OH}	2.4		V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}		0.4	V	$I_{OL} = +2.5\ mA$
Input leakage current, high	I_{LIH}		10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}		−10	μA	$V_I = 0\ V$
Output leakage current, high	I_{LOH}		10	μA	$V_O = V_{CC}$ (outputs disabled)
Output leakage current, low	I_{LOL}		−10	μA	$V_O = 0\ V$ (outputs disabled)
Power supply current	I_{CC1}		40	mA	$\overline{CE} = V_{IL}$
	I_{CC2}		1.5	mA	$\overline{CE} = V_{IH}$
	I_{CC3}		100	μA	$\overline{CE} = V_{CC} - 0.2\ V$

AC Characteristics

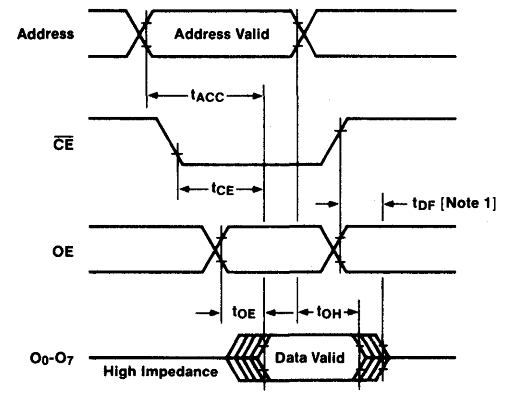
$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$ (Note 1)

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Address access time	t_{ACC}			200	ns
Chip enable access time	t_{CE}			200	ns
Output enable access time	t_{OE}			100	ns
Output hold time	t_{OH}	0			ns
Output disable time	t_{DF}	0		60	ns

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveform



Note:
[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

83-004134A

9

NEC
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μPD23C1010A 131,072 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C1010A is a 1,048,576-bit ROM fabricated with CMOS silicon-gate technology. The device is static in operation and organized as 131,072 words by 8 bits. It has three-state outputs and fully TTL-compatible inputs and outputs. The μPD23C1010A is available in a 28-pin plastic DIP.

Features

- ☐ 131,072 words by 8-bit organization
- ☐ Fast access time
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS technology
- ☐ Fully static operation
- ☐ Low power dissipation: 220 mW

Ordering Information

Part Number	Address Access Time (max)	Output Enable Access Time (max)	Package
μPD23C1010AC	200 ns	100 ns	28-pin plastic DIP

Absolute Maximum Ratings

$T_A = 25°C$

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

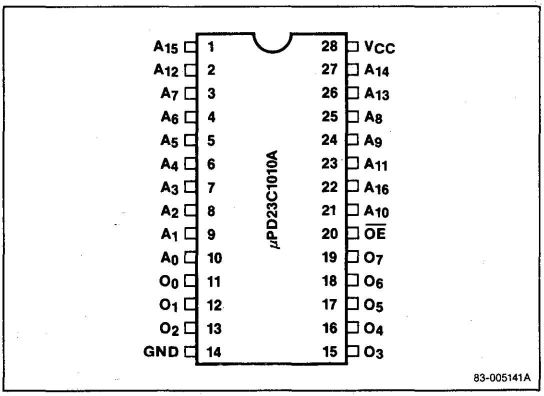
Capacitance

$T_A = 25°C$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

Pin Configuration

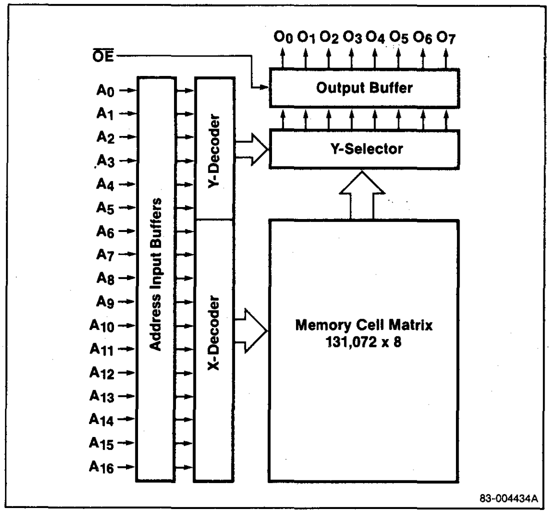
28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_7	Data outputs
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2		V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = +2.5\ mA$
Input leakage current, high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}			−10	μA	$V_I = 0\ V$
Output leakage current, high	I_{LOH}			10	μA	$V_O = V_{CC}$; output disabled
Output leakage current, low	I_{LOL}			−10	μA	$V_O = 0\ V$; output disabled
Power supply current	I_{CC1}			40	mA	

AC Characteristics

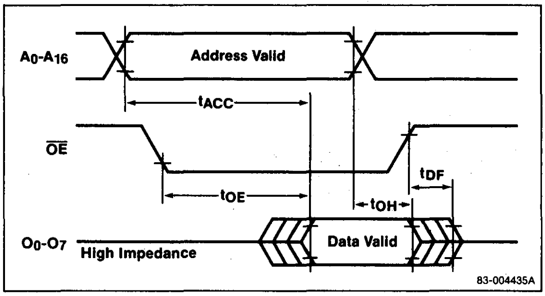
$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Max	Unit
Address access time	t_{ACC}		200	ns
Output enable access time	t_{OE}		100	ns
Output hold time	t_{OH}	0		ns
Output disable time	t_{DF}	0	60	ns

Notes:

(1) AC test conditions: input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveform



µPD23C2000 2,097,152-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The µPD23C2000 is a 2,097,152-bit ROM fabricated with CMOS silicon-gate technology. Static in operation and organized as 131,072 words by 16 bits (word mode) or 262,144 words by 8 bits (byte mode), the device has three-state outputs and fully TTL-compatible inputs and outputs. The output enable pin is mask-programmable and can be specified by selecting "1", "0", or "don't care" data.

The µPD23C2000 is available in 40-pin plastic DIP or 52-pin plastic miniflat packaging.

Features

- ☐ Programmable organization
  - — 131,072 words by 16 bits (word)
  - — 262,144 words by 8 bits (byte)
- ☐ Fast access time: 250 ns maximum
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS technology
- ☐ Fully static operation
- ☐ Low power dissipation
  - — 220 mW (active)
  - — 550 µW (standby)

Ordering Information

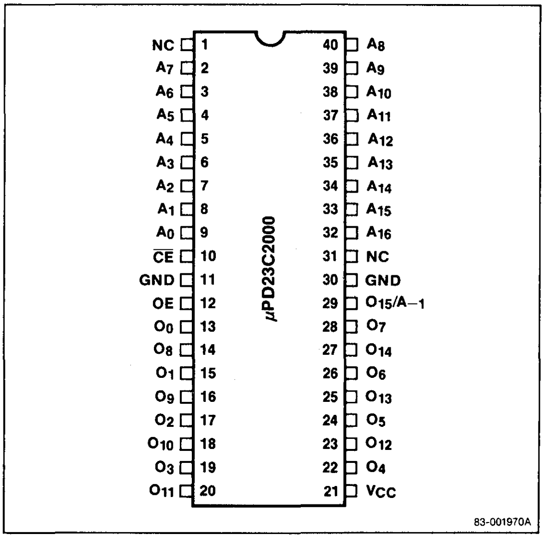
Part Number	Access Time (max)	Power Consumption (max) Active	Power Consumption (max) Standby	Package
µPD23C2000C	250 ns	40 mA	100 µA	40-pin plastic DIP
µPD23C2000G	250 ns	40 mA	100 µA	52-pin plastic miniflat

Pin Identification

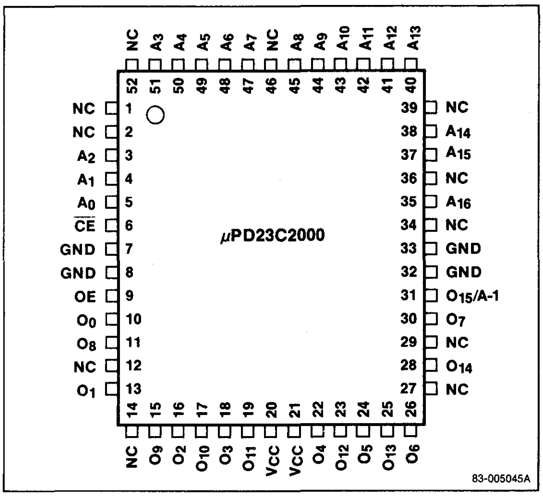
Symbol	Function
A_0-A_{16}	Address inputs
O_0-O_{14}	Outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
$\overline{CE}$	Chip enable
OE	Output enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations

40-Pin Plastic DIP



52-Pin Plastic Miniflat



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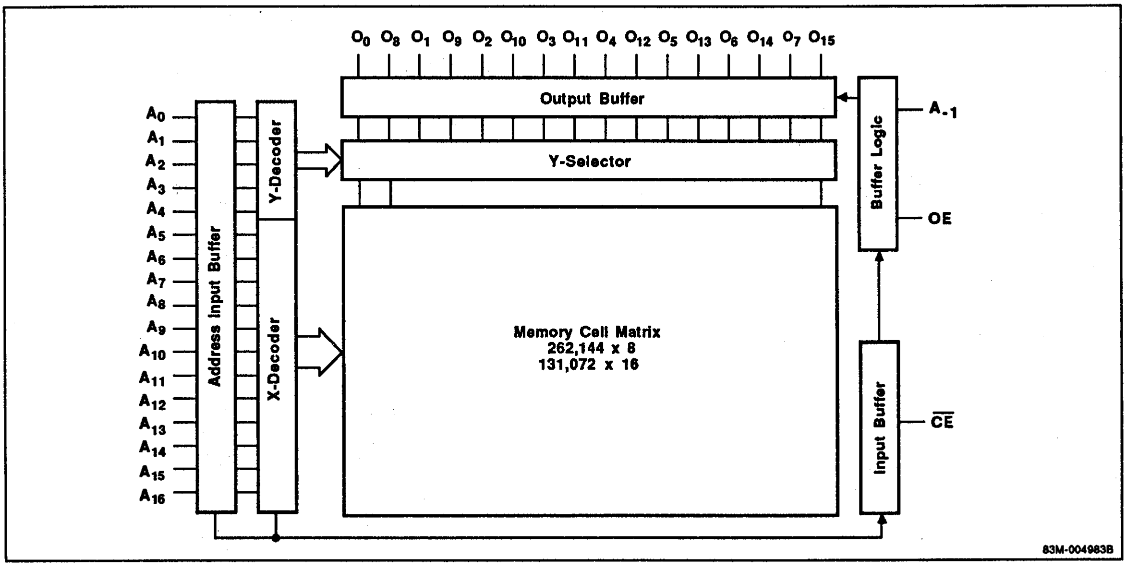
Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} +0.3 V
Output voltage, V_O	−0.3 V to V_{CC} +0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2		V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = +3.2 mA
Input leakage current, high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}			−10	μA	V_I = 0 V
Output leakage current, high	I_{LOH}			10	μA	$V_O = V_{CC}$; chip deselected
Output leakage current, low	I_{LOL}			−10	μA	V_O = 0 V; chip deselected
Power supply current	I_{CC1}			40	mA	$\overline{CE} = V_{IL}$
	I_{CC2}			1.5	mA	$\overline{CE} = V_{IH}$ (standby)
	I_{CC3}			100	μA	$\overline{CE} \geq V_{CC}$ − 0.2 V (standby)

AC Characteristics

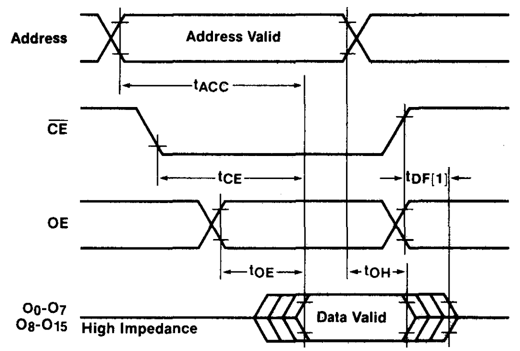
$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Address access time	t_{ACC}			250	ns
Chip enable access time	t_{CE}			250	ns
Output enable access time	t_{OE}	10		110	ns
Output hold time	t_{OH}	0			ns
Output disable time	t_{DF}	0		90	ns

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveform



Notes:
[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

83-004984A

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NEC

NEC Electronics Inc.

μPD23C2001 262,144 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C2001 is a 262,144-word by 8-bit static ROM fabricated with CMOS silicon-gate technology. Designed to operate from a single +5-volt power supply, the device has three-state outputs and fully TTL-compatible inputs and outputs. The μPD23C2001 is packaged in a 32-pin plastic DIP.

Features

- ☐ 262,144-word by 8-bit organization
- ☐ Fast access time: 250 ns maximum
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Low power dissipation
  - — 220 mW (active)
  - — 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C2001C	250 ns	32-pin plastic DIP

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

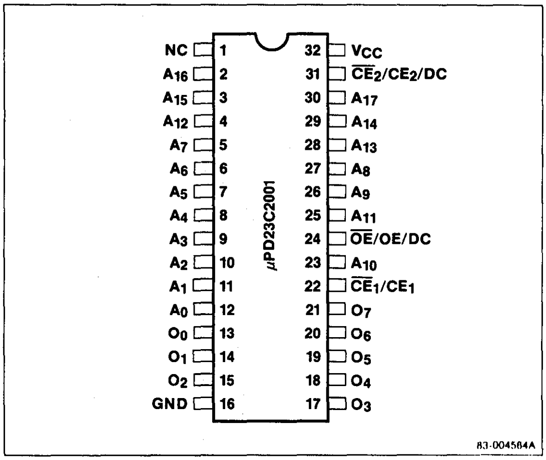
Capacitance

$T_A = 25°C$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Units	Test Conditions
Input capacitance	C_I			15	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

Pin Configuration

32-Pin Plastic DIP



Pin Identification

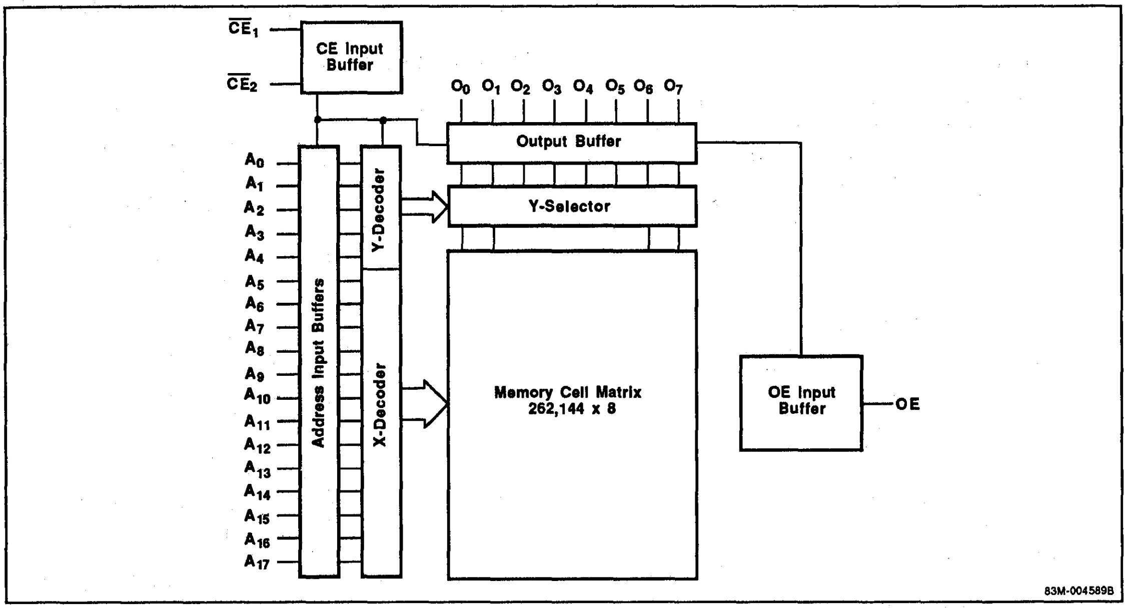
Symbol	Function
A_0-A_{17}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}_1/CE_1$	Chip enable 1 (Note 1)
$\overline{CE}_2/CE_2/DC$	Chip enable 2 (Note 1)
$\overline{OE}/OE/DC$	Output enable (Note 1)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Notes:

(1) This pin is user-definable as active low, active high, or "don't care" (in the cases of $\overline{CE}_2/CE_2/DC$ and $\overline{OE}/OE/DC$).

9

Block Diagram



DC Characteristics

$T_A = -10$ to $+70$°C; $V_{CC} = +5.0$ V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2	V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3	0.8	V	
Output voltage, high	V_{OH}	2.4		V	$I_{OH} = -400$ μA
Output voltage, low	V_{OL}		0.4	V	$I_{OL} = +2.1$ mA
Input leakage current, high	I_{LIH}		10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}		−10	μA	$V_I = 0$ V
Output leakage current, high	I_{LOH}		10	μA	$V_O = V_{CC}$ (outputs disabled)
Output leakage current, low	I_{LOL}		−10	μA	$V_O = 0$ V (outputs disabled)
Power supply current	I_{CC1}		40	mA	Both $\overline{CE}_1$ and $\overline{CE}_2$ active
	I_{CC2}		1.5	mA	Either $\overline{CE}_1$ or $\overline{CE}_2$ inactive (V_{IL}, V_{IH})
	I_{CC3}		100	μA	Either $\overline{CE}_1$ or $\overline{CE}_2$ inactive (both ≤ 0.2 V or ≥ V_{CC} − 0.2 V)

AC Characteristics

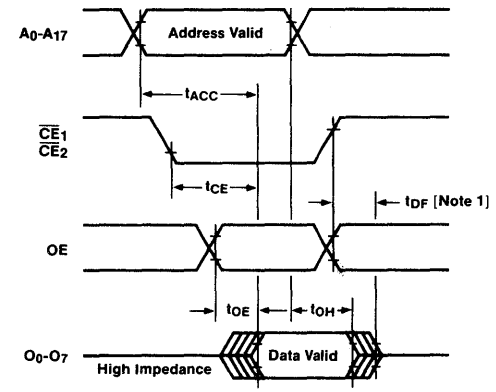
$T_A = -10$ to $+70$°C; $V_{CC} = +5.0$ V ±10% (Note 1)

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Address access time	t_{ACC}			250	ns
Chip enable access time	t_{CE}			250	ns
Output enable access time	t_{OE}			110	ns
Output hold time	t_{OH}	0			ns
Output disable time	t_{DF}	0		60	ns

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveform



Note:
[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

83-004590A

9

NEC

NEC Electronics Inc.

μPD23C4000 4,194,304-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C4000 is a 4,194,304-bit ROM fabricated with CMOS silicon-gate technology. Static in operation, the device has three-state outputs and fully TTL-compatible inputs and outputs. The output enable pin is mask-programmable and can be specified as active high, active low, or don't care.

The μPD23C4000 can be hardware-configured as either 256K x 16 bits or as 512K x 8 bits by tying the WORD/$\overline{\text{BYTE}}$ pin high or low, respectively. In the word configuration, pins O_0-O_{15} are active. In the byte configuration, pins O_0-O_7 are active, pins O_8-O_{14} are high impedance, and pin O_{15}/A_{-1} becomes the additional bit required to address 512K bytes.

The μPD23C4000 is available in a 40-pin plastic DIP and a 64-pin plastic QFP.

Features

- ☐ Programmable organization
  - — 262,144 words by 16 bits (word)
  - — 524,288 words by 8 bits (byte)
- ☐ Fast access time: 250 ns maximum
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS technology
- ☐ Fully static operation
- ☐ Low power dissipation
- ☐ 40-pin plastic DIP or 64-pin plastic QFP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD23C4000C	250 ns	40-pin plastic DIP
μPD23C4000GF	250 ns	64-pin plastic QFP

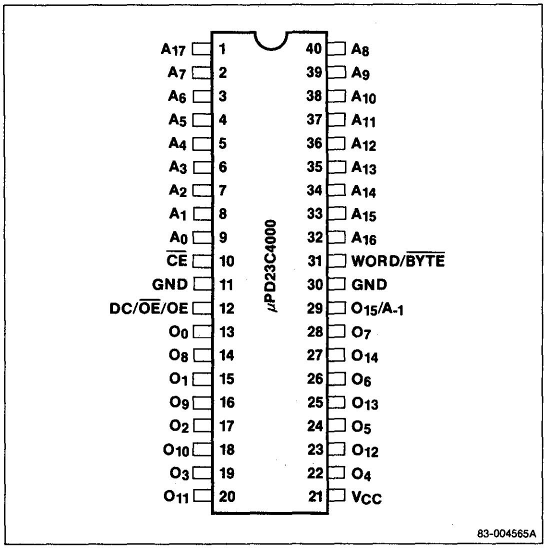
Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} +0.3 V
Output voltage, V_O	−0.3 V to V_{CC} +0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

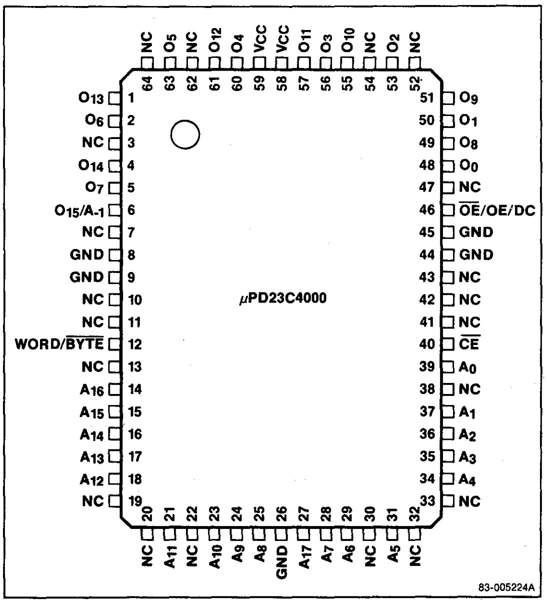
Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configurations

40-Pin Plastic DIP



64-Pin Plastic QFP



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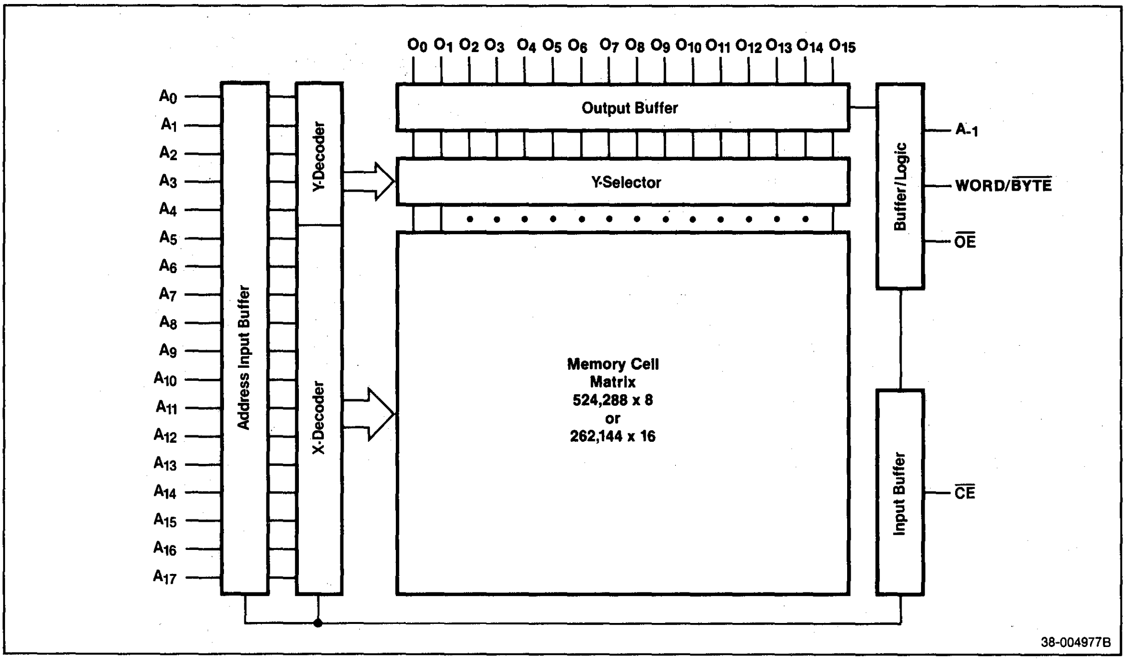
Block Diagram



Pin Identification

Symbol	Function
A_0-A_{17}	Address inputs
O_0-O_{14}	Outputs
O_{15}/A_{-1}	Output 15 (word)/LSB address (byte)
WORD/$\overline{BYTE}$	Word/byte selection
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
DC	Don't care
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

$T_A = 25°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

DC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2		V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = +2.5$ mA
Input leakage current, high	I_{LIH}			10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}			−10	μA	$V_I = 0$ V
Output leakage current, high	I_{LOH}			10	μA	$V_O = V_{CC}$; chip deselected
Output leakage current, low	I_{LOL}			−10	μA	$V_O = 0$ V; chip deselected
Power supply current	I_{CC1}			40	mA	$\overline{CE} = V_{IL}$
	I_{CC2}			1.5	mA	$\overline{CE} = V_{IH}$; chip deselected
	I_{CC3}			100	μA	$\overline{CE} = V_{CC} - 0.2$ V; chip deselected

AC Characteristics

$T_A = -10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$

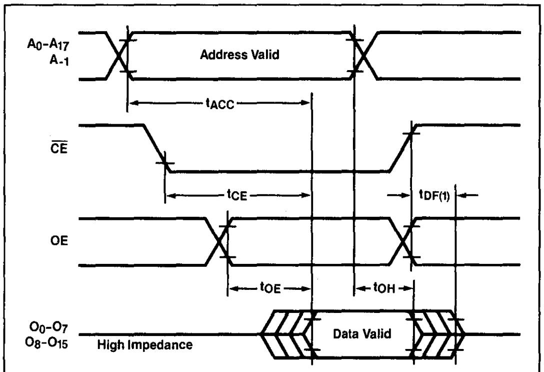
Parameter	Symbol	Limits Min	Typ	Max	Unit
Address access time	t_{ACC}			250	ns
Chip enable access time	t_{CE}			250	ns
Output enable access time	t_{OE}			110	ns
Output hold time	t_{OH}	0			ns
Output disable time	t_{DF}	0		70	ns
Output disable time for O_8-O_{15} referenced to WORD/$\overline{BYTE}$	t_{HDF}			100	ns
Output enable access time referenced to WORD/$\overline{BYTE}$	t_{WB}			250	ns

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

Timing Waveforms

Read Cycle



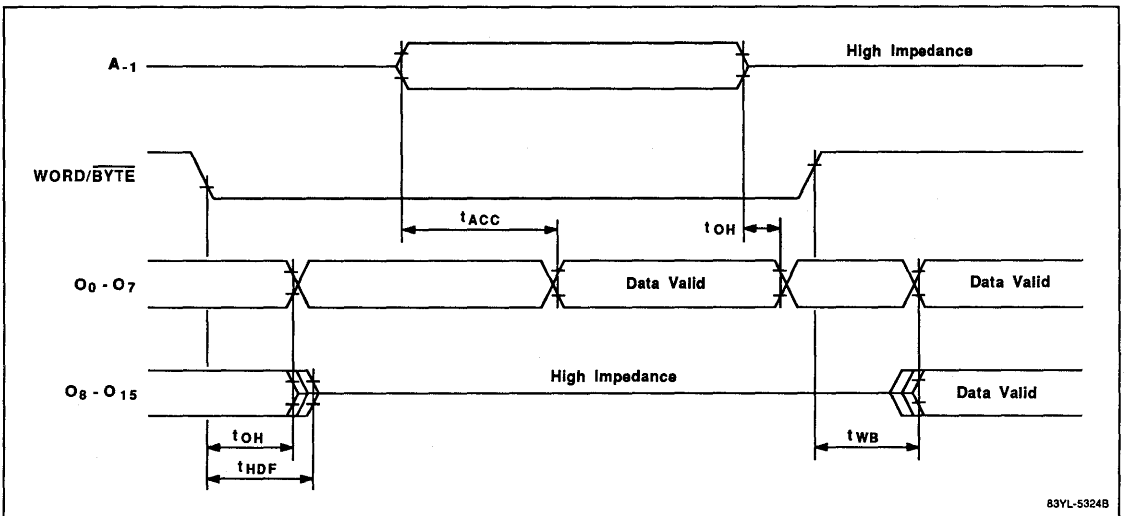
Notes:

[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

[2] When WORD/$\overline{BYTE}$ is low, O_8-O_{14} are high impedance. Pin O_{15}/A_{-1} becomes an additional address input.

83-004978A

WORD/$\overline{BYTE}$ Selection Timing



NEC
NEC Electronics Inc.

μPD23C4001E 524,288 x 8-BIT MASK-PROGRAMMABLE CMOS ROM

Description

The μPD23C4001E is a 524,288-word by 8-bit static ROM fabricated with CMOS silicon-gate technology. Designed to operate from a single +5-volt power supply, the device has three-state outputs and fully TTL-compatible inputs and outputs. The μPD23C4001E is packaged in a 600-mil, 32-pin plastic DIP.

Features

- ☐ 524,288-word by 8-bit organization
- ☐ Fast access time: 250 ns maximum
- ☐ TTL-compatible inputs and outputs
- ☐ Three-state outputs
- ☐ Single +5-volt power supply
- ☐ CMOS process technology
- ☐ Fully static operation
- ☐ Low power dissipation
  - — 220 mW (active)
  - — 550 μW (standby)

Ordering Information

Part Number	Access Time (max)	Package
μPD23C4001EC	250 ns	32-pin plastic DIP

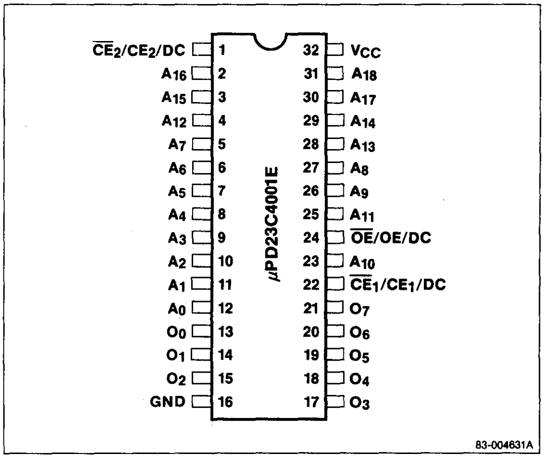
Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Pin Configuration

32-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0-A_{18}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}_1$/CE_1/DC	Chip enable 1 (Note 1)
$\overline{CE}_2$/CE_2/DC	Chip enable 2 (Note 1)
$\overline{OE}$/OE/DC	Output enable (Note 1)
GND	Ground
V_{CC}	+5-volt power supply

Notes:

(1) This pin is user-definable as active low, active high, or "don't care."

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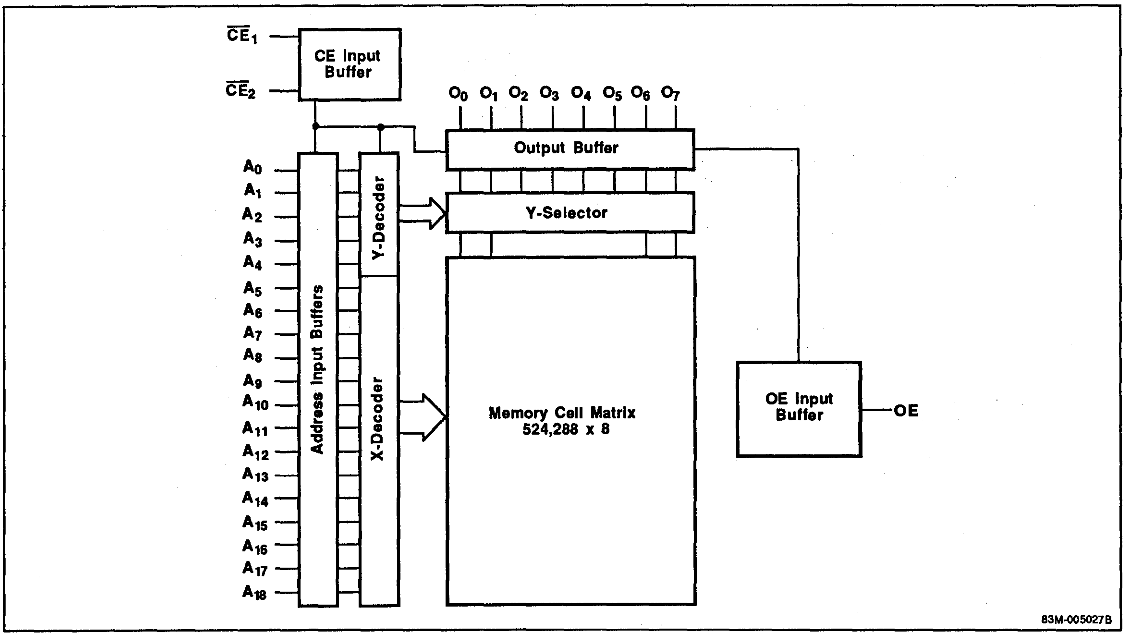
Block Diagram



DC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	2.2	V_{CC} +0.3	V	
Input voltage, low	V_{IL}	−0.3	0.8	V	
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −400 μA
Output voltage, low	V_{OL}		0.4	V	I_{OL} = +2.1 mA
Input leakage current, high	I_{LIH}		10	μA	$V_I = V_{CC}$
Input leakage current, low	I_{LIL}		−10	μA	V_I = 0 V
Output leakage current, high	I_{LOH}		10	μA	$V_O = V_{CC}$ (outputs disabled)
Output leakage current, low	I_{LOL}		−10	μA	V_O= 0 V (outputs disabled)
Power supply current	I_{CC1}		40	mA	Both $\overline{CE}_1$ and $\overline{CE}_2$ active
	I_{CC2}		1.5	mA	Either $\overline{CE}_1$ or $\overline{CE}_2$ inactive; $\overline{CE} = V_{IH}$
	I_{CC3}		100	μA	Either $\overline{CE}_1$ or $\overline{CE}_2$ inactive (both ≤ 0.2 V or ≥ V_{CC} − 0.2 V)

Capacitance

T_A = 25°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Units	Test Conditions
Input capacitance	C_I			15	pF	f = 1 MHz
Output capacitance	C_O			15	pF	f = 1 MHz

AC Characteristics

T_A = −10 to +70°C; V_{CC} = +5.0 V ±10% (Note 1)

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit
Address access time	t_{ACC}			250	ns
Chip enable access time	t_{CE}			250	ns
Output enable access time	t_{OE}			110	ns
Output hold time	t_{OH}	0			ns
Output disable time	t_{DF}	0		70	ns

Notes:

(1) Input voltage rise and fall times = 20 ns; input and output timing reference levels = 0.8 V and 2.0 V; output load = 1 TTL + 100 pF.

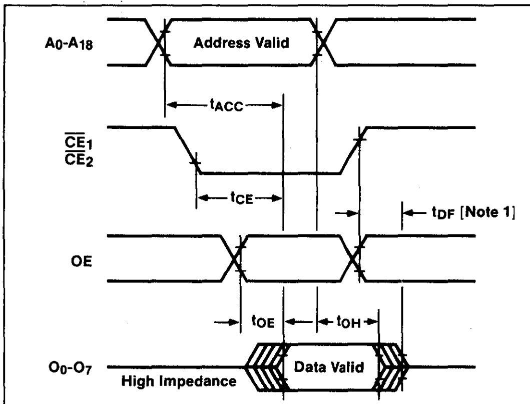
Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{OE}$
L	L	L
H	H	H
X	X	X

Notes:

(1) X = don't care

Timing Waveform



Note:
[1] t_{DF} is specified from OE or $\overline{CE}$, whichever occurs first.

83-005016A

PACKAGING INFORMATION

10

Section 10
Packaging Information

Device/Package Cross Reference

Part Number	Package	Ordering Designation	Page
MC-41256A8	30-pin leaded SIMM #1	A	10-23
	30-pin socket-mountable SIMM #1	B	10-24
MC-41256A9	30-pin leaded SIMM #2	A	10-23
	30-pin socket-mountable SIMM #2	B	10-25
MC-421000A8	30-pin leaded SIMM #4	A	10-24
	30-pin socket-mountable SIMM #4	B	10-26
MC-421000A9	30-pin leaded SIMM #3	A	10-24
	30-pin socket-mountable SIMM #3	B	10-25
MC-421000B8	30-pin leaded SIMM #4	A	10-24
	30-pin socket-mountable SIMM #4	B	10-26
MC-421000B9	30-pin leaded SIMM #3	A	10-24
	30-pin socket-mountable SIMM #3	B	10-25
MC-421000C8	30-pin leaded SIMM #4	A	10-24
	30-pin socket-mountable SIMM #4	B	10-26
MC-421000C9	30-pin leaded SIMM #3	A	10-24
	30-pin socket-mountable SIMM #3	B	10-25
μPB100422	24-pin ceramic DIP (400 mil)	D	10-14
	24-pin ceramic flatpack	B	10-16
μPB100470	18-pin ceramic DIP (300 mil)	D	10-7
μPB100474	24-pin cerdip (400 mil)	D	10-14
	24-pin ceramic flatpack	B	10-16
	24-pin ceramic LCC	K	10-17
μPB100474A	24-pin cerdip (400 mil)	D	10-14
	24-pin ceramic flatpack	B	10-16
μPB100480	20-pin cerdip (300 mil)	D	10-9
	20-pin ceramic flatpack	B	10-10
μPB100484	28-pin cerdip (400 mil)	D	10-19
	28-pin ceramic flatpack	B	10-22
μPB10422	24-pin ceramic DIP (400 mil)	D	10-14
μPB10470	18-pin ceramic DIP (300 mil)	D	10-7
μPB10474	24-pin ceramic DIP (400 mil)	D	10-14
μPB10474A	24-pin cerdip (400 mil)	D	10-14

Device/Package Cross Reference (cont)

Part Number	Package	Ordering Designation	Page
μPB10480	20-pin cerdip (300 mil)	D	10-9
	20-pin ceramic flatpack	B	10-10
μPB10484	28-pin cerdip (400 mil)	D	10-19
	28-pin ceramic flatpack	B	10-22
μPD23C1000A	28-pin plastic DIP (600 mil)	C	10-19
	28-pin plastic miniflat #1	G	10-21
μPD23C1000EA	32-pin plastic DIP (600 mil)	C	10-26
μPD23C1001E	32-pin plastic DIP (600 mil)	C	10-26
μPD23C1010A	28-pin plastic DIP (600 mil)	C	10-19
μPD23C2000	40-pin plastic DIP (600 mil)	C	10-28
	52-pin plastic miniflat	G	10-29
μPD23C2001	32-pin plastic DIP (600 mil)	C	10-26
μPD23C4000	40-pin plastic DIP (600 mil)	C	10-28
	64-pin plastic quad flatpack	GF	10-30
μPD23C4001E	32-pin plastic DIP (600 mil)	C	10-26
μPD27C1000A	32-pin cerdip (600 mil) #1	D	10-27
μPD27C1001A	32-pin cerdip (600 mil) #1	D	10-27
μPD27C1024	40-pin cerdip (600 mil)	D	10-28
μPD27C2001	32-pin cerdip (600 mil) #2	D	10-27
μPD27C256A	28-pin cerdip (600 mil)	D	10-20
μPD27C512	28-pin cerdip (600 mil)	D	10-20
μPD28C04	24-pin plastic DIP (600 mil)	C	10-13
	24-pin plastic miniflat	G	10-15
μPD28C64	28-pin plastic DIP (600 mil)	C	10-19
μPD41101	24-pin plastic DIP (300 mil) #1	C	10-12
	24-pin plastic miniflat	G	10-15
μPD41102	24-pin plastic DIP (300 mil) #1	C	10-12
	24-pin plastic miniflat	G	10-15
μPD41256	16-pin plastic DIP (300 mil)	C	10-5
	18-pin plastic leaded chip carrier	L	10-7

Device/Package Cross Reference (cont)

Part Number	Package	Ordering Designation	Page
μPD41257	16-pin plastic DIP (300 mil)	C	10-5
	18-pin plastic leaded chip carrier	L	10-7
μPD41264	24-pin plastic DIP (400 mil)	C	10-13
	24-pin plastic ZIP	V	10-15
μPD41464	18-pin plastic DIP (300 mil) #2	C	10-6
	18-pin plastic leaded chip carrier	L	10-7
	20-pin plastic ZIP #1	V	10-9
μPD421000	18-pin plastic DIP (300 mil) #1	C	10-6
	26/20-pin plastic SOJ	LA	10-17
	20-pin plastic ZIP #2	V	10-10
μPD421001	18-pin plastic DIP (300 mil) #1	C	10-6
	26/20-pin plastic SOJ	LA	10-17
	20-pin plastic ZIP #2	V	10-10
μPD421002	18-pin plastic DIP (300 mil) #1	C	10-6
	26/20-pin plastic SOJ	LA	10-17
	20-pin plastic ZIP #2	V	10-10
μPD42101	24-pin plastic DIP (300 mil) #1	C	10-12
	24-pin plastic miniflat	G	10-15
μPD42102	24-pin plastic DIP (300 mil) #1	C	10-12
	24-pin plastic miniflat	G	10-15
μPD42270	28-pin plastic DIP (400 mil)	C	10-18
μPD42273	28-pin plastic SOJ	LE	10-22
	28-pin plastic ZIP	V	10-20
μPD42274	28-pin plastic SOJ	LE	10-22
	28-pin plastic ZIP	V	10-20
μPD424256	20-pin plastic DIP (300 mil) #2	C	10-8
	26/20-pin plastic SOJ	LA	10-17
	20-pin plastic ZIP #2	V	10-10
μPD424258	20-pin plastic DIP (300 mil) #2	C	10-8
	26/20-pin plastic SOJ	LA	10-17
	20-pin plastic ZIP #2	V	10-10

Device/Package Cross Reference (cont)

Part Number	Package	Ordering Designation	Page
μPD42505	24-pin plastic DIP (300 mil) #1	C	10-12
μPD42532	40-pin plastic DIP (600 mil)	C	10-28
μPD42601	18-pin plastic DIP (300 mil) #1	C	10-6
	26/20-pin plastic SOJ	LA	10-17
	20-pin plastic ZIP #2	V	10-10
μPD4311	20-pin plastic DIP (300 mil) #1	C	10-8
μPD4314	20-pin plastic DIP (300 mil) #1	C	10-8
μPD43254	24-pin plastic DIP (300 mil) #2	C	10-12
μPD43256A	28-pin plastic DIP (600 mil)	C	10-19
	28-pin plastic miniflat #2	GU	10-21
μPD4361	22-pin plastic DIP (300 mil)	C	10-11
	22-pin ceramic leadless chip carrier	K	10-11
μPD4362	22-pin plastic DIP (300 mil)	C	10-11
μPD4363	24-pin plastic DIP (300 mil) #2	C	10-12
μPD4364	28-pin plastic DIP (300 mil)	CX	10-18
	28-pin plastic DIP (600 mil)	C	10-19
	28-pin plastic miniflat #1	G	10-21
μPD4464	28-pin plastic DIP (600 mil)	C	10-19
	28-pin plastic miniflat #1	G	10-21

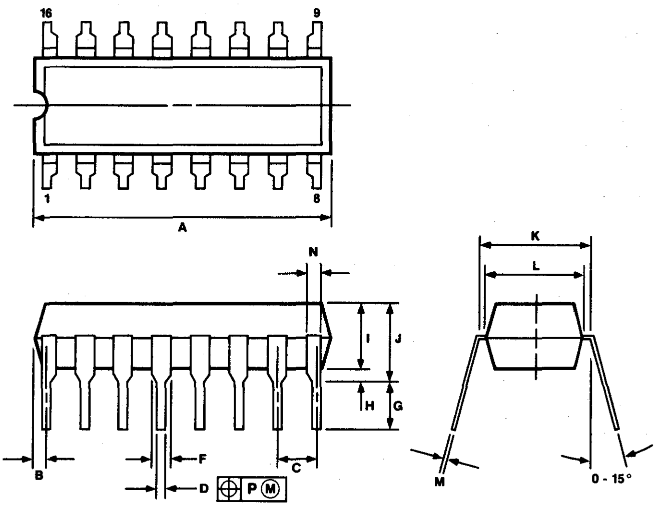
16-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020 ^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	$.126 \pm .012$
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.7	.264
M	$0.25 ^{+0.10}_{-0.05}$	$.010 ^{+.004}_{-.003}$
N	1.0 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003634B

10

NEC

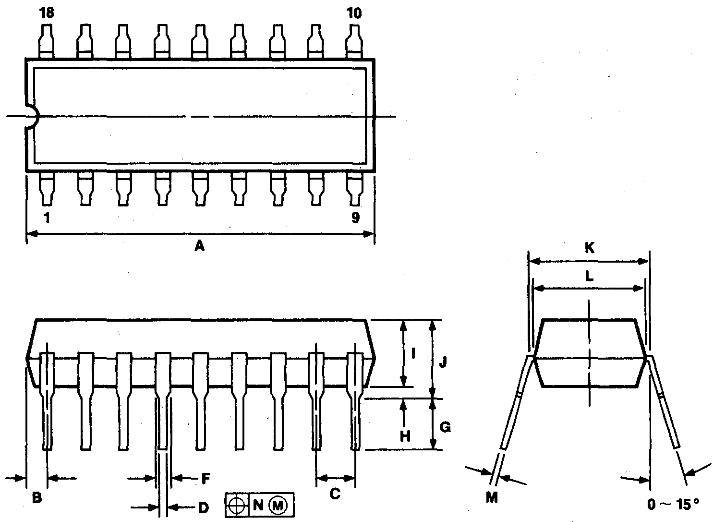
18-Pin Plastic DIP (300 mil) #1

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020 ^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	$.126 \pm .012$
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.35	.289
M	$0.25 ^{+0.10}_{-0.05}$	$.010 ^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003586B

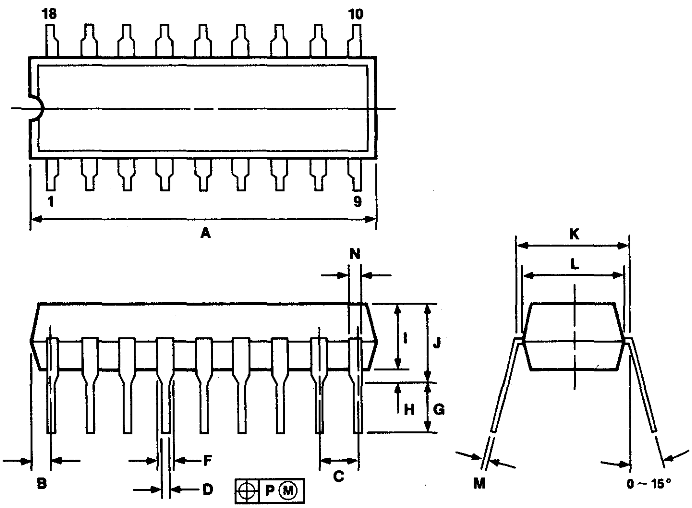
18-Pin Plastic DIP (300 mil) #2

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020 ^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	$.126 \pm .012$
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.7	.264
M	$0.25 ^{+0.10}_{-0.05}$	$.010 ^{+.004}_{-.003}$
N	1.0 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003588B

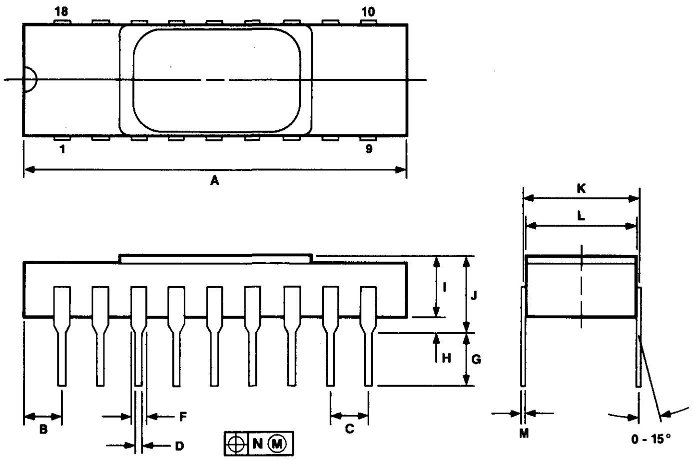
18-Pin Ceramic DIP (300 mil)

Item	Millimeters	Inches
A	25.40 max	1.000 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.46 ± .05	.018 ± .002
E	20.32	.800
F	1.25 min	.049 min
G	3.5 ± .3	.138 ± .012
H	.51 min	.020 min
I	2.90	.114
J	4.57 max	.180 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	.25 ± .05	.010 $^{+.002}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

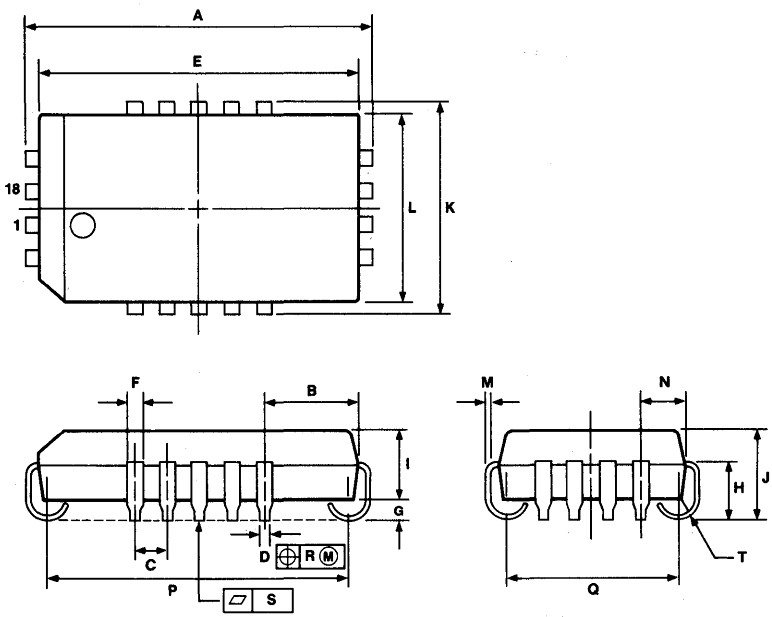
[2] Item "K" to center of leads when formed parallel.



83-003628B

18-Pin Plastic Leaded Chip Carrier

Item	Millimeters	Inches
A	13.4 ± 0.20	.528 $^{+.008}_{-.009}$
B	3.71 ± 0.15	.146 $^{+.006}_{-.007}$
C	1.27 [TP]	.050 [TP]
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	12.5	.492
F	0.60	.024
G	0.8 min	.031 min
H	2.40 ± 0.20	.094 $^{+.009}_{-.008}$
I	2.6	.102
J	3.50 ± 0.20	.138 $^{+.008}_{-.009}$
K	8.30 ± 0.20	.327 $^{+.008}_{-.009}$
L	7.40	.291
M	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$
N	1.80 ± 0.15	.071 $^{+.006}_{-.007}$
P	11.68 ± 0.20	.460 $^{+.008}_{-.009}$
Q	6.6 ± 0.20	.260 $^{+.008}_{-.009}$
R	0.12	.005
S	0.15	.006
T	R 0.8	R .031



83-003581B

NEC

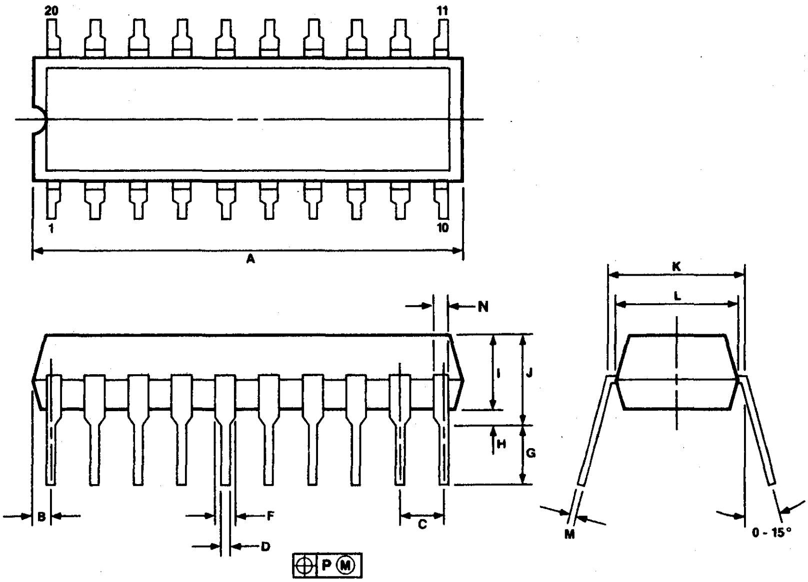
20-Pin Plastic DIP (300 mil) #1

Item	Millimeters	Inches
A	25.40 max	1.00 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020 {}^{+.004}_{-.005}$
F	1.10 min	.043 min
G	3.50 ± 0.30	$.138 \pm .012$
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.4	.252
M	$0.25 {}^{+0.10}_{-0.05}$	$.010 {}^{+.004}_{-.003}$
N	0.90 min	.035 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-001491B

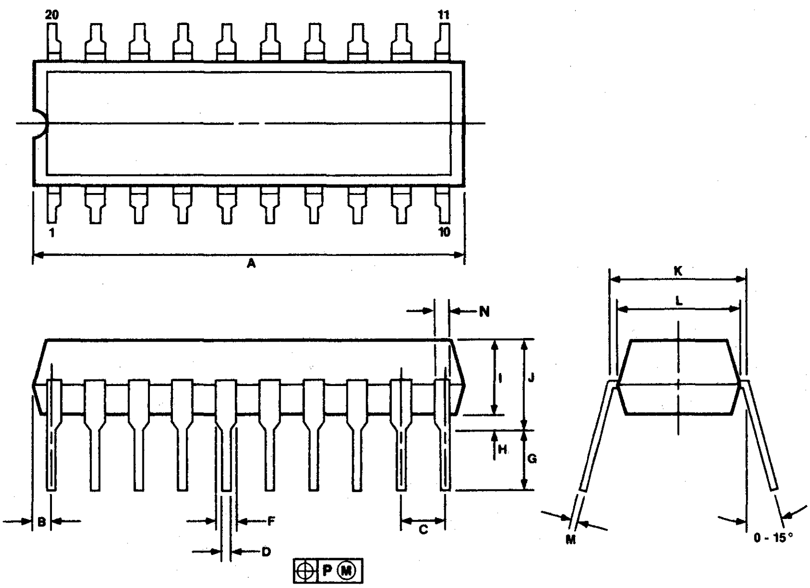
20-Pin Plastic DIP (300 mil) #2

Item	Millimeters	Inches
A	25.40 max	1.000 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020 {}^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.30	$.126 \pm .012$
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.35	.289
M	$0.25 {}^{+0.10}_{-0.05}$	$.010 {}^{+.004}_{-.003}$
N	1.0 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003626B

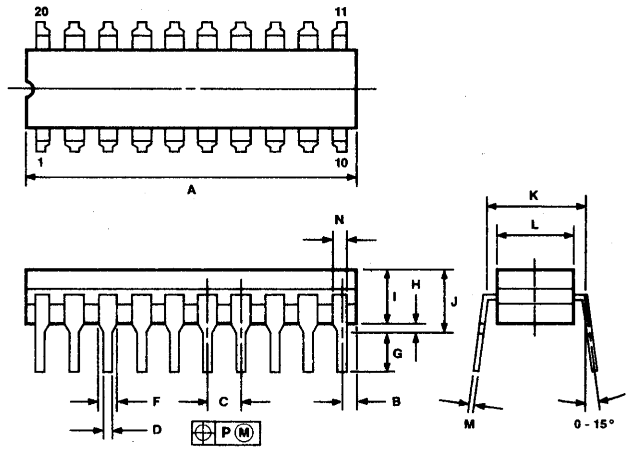
20-Pin Cerdip (300 mil)

Item	Millimeters	Inches
A	25.4 max	1.00 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.06	.018 ± .002
F	1.42 min	.055 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



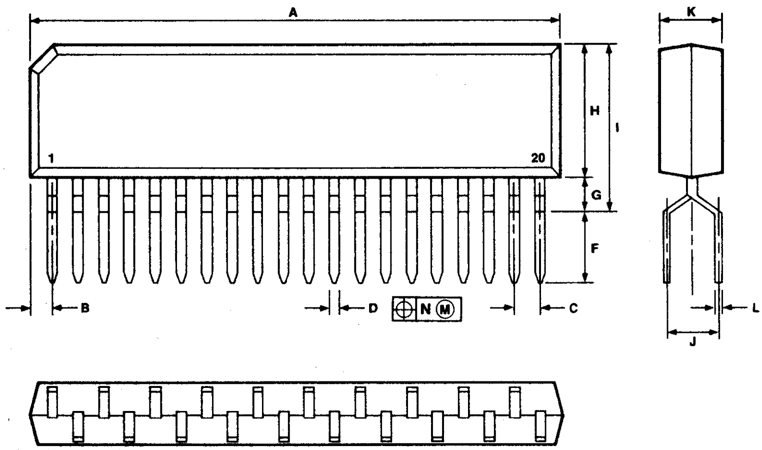
83-003849B

20-Pin Plastic ZIP #1

Item	Millimeters	Inches
A	26.0 max	1.024 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	3.00 min	.118 min
G	0.90 min	.035 min
H	6.60	.260
I	8.26 max	.325 max
J	2.54 [TP]	.100 [TP]
K	2.80 ± 0.20	.110 ± .008
L	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	ϕ 0.12	ϕ .005

Notes:

[1] Each lead centerline is located within 0.12 mm [.005 inch] of its true position [TP] at maximum material condition.



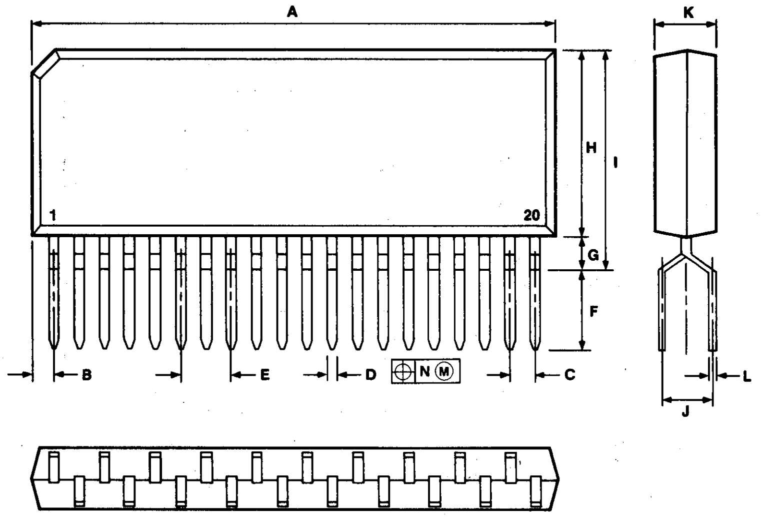
83-004226B

20-Pin Plastic ZIP #2

Item	Millimeters	Inches
A	26.67 max	1.050 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	0.50 ± 0.10	$.020 {}^{+.004}_{-.005}$
E	2.54 [TP]	.100 [TP]
F	3.3 ± 0.5	$.130 \pm .020$
G	1.0 min	.039 min
H	8.9 max	.350 max
I	10.16 max	.400 max
J	2.54 [TP]	.100 [TP]
K	2.8 ± 0.2	$.110 {}^{+.009}_{-.008}$
L	$0.25 {}^{+0.10}_{-0.05}$	$.010 {}^{+.004}_{-.003}$
N	ϕ 0.25	ϕ .010

Note:

[1] Each lead centerline is located within 0.25 mm [0.010 inch] of its true position [TP] at maximum material condition.



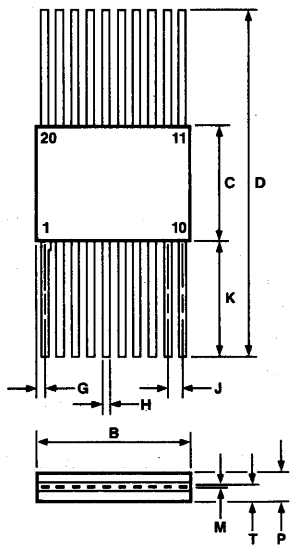
83-004263B

20-Pin Ceramic Flatpack

Item	Millimeters	Inches
B	$12.6 {}^{+0.4}_{-0.1}$	$.496 {}^{+.016}_{-.004}$
C	$9.8 {}^{+0.4}_{-0.1}$	$.388 {}^{+.016}_{-.005}$
D	29.0	1.142
G	0.6	.024
H	0.43	.169
J	1.27	.050
K	9.6	.378
M	0.13	.005
P	2.18 max	.086 max
T	1.14 max	.045 max

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.



83-005014B

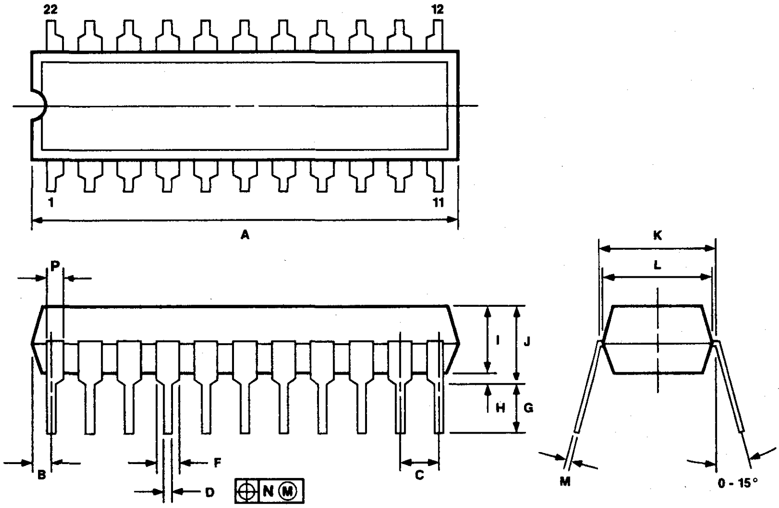
22-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	27.94 max	1.100 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 +.004 −.005
F	1.2 min	.047 min
G	3.20 ± 0.30	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.35	.289
M	0.25 +0.10 −0.05	.010 +.004 −.003
N	0.25	.010
P	0.9 min	.035 min

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

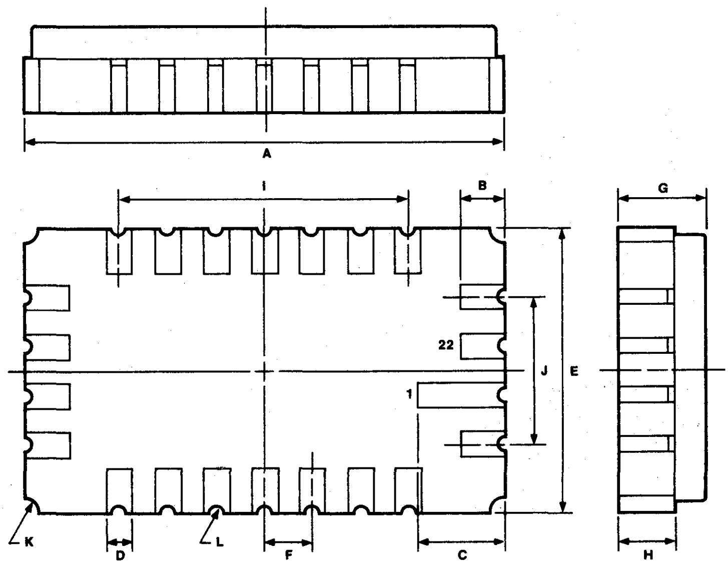
[2] Item "K" to center of leads when formed parallel.



83-003577B

22-Pin Ceramic LCC

Item	Millimeters	Inches
A	12.45 ± .35	.490 ± .014
B	1.14	.045
C	2.29	.090
D	.64	.025
E	7.37 ± .35	.290 ± .014
F	1.27	.050
G	2.26 max	.089 max
H	1.40	.055
I	7.62	.300
J	3.81	.150
K	.3 rad	.012 rad
L	.2 rad	.008 rad



83-003578B

10

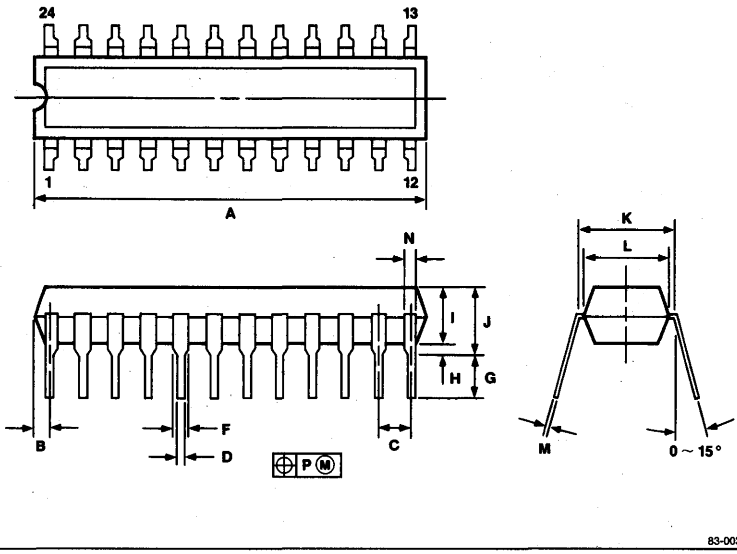
24-Pin Plastic DIP (300 mil) #1

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020 {}^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.50 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.4	.252
M	$0.25 {}^{+0.10}_{-0.05}$	$.010 {}^{+.004}_{-.003}$
N	1.0 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



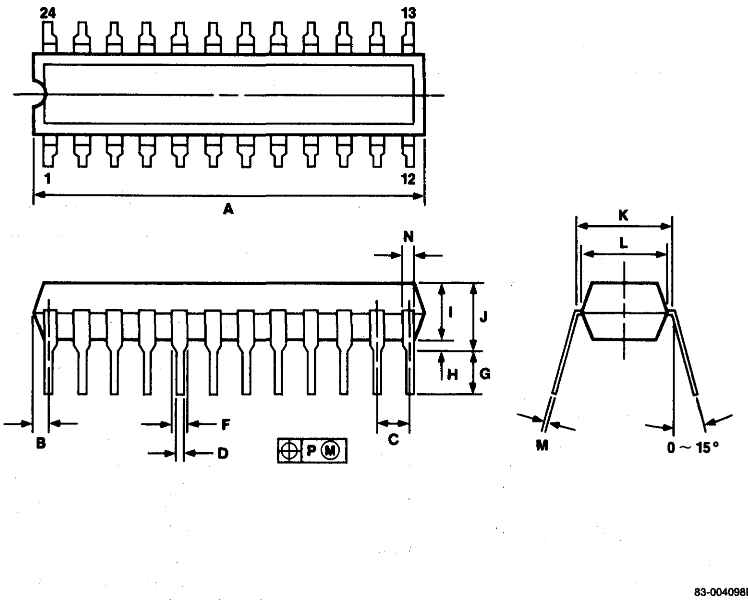
24-Pin Plastic DIP (300 mil) #2

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ±0.10	$.020 {}^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.20 ±0.3	.126 ±.012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.35	.289
M	$0.25 {}^{+0.10}_{-0.05}$	$.010 {}^{+.004}_{-.003}$
N	0.9 min	.035 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



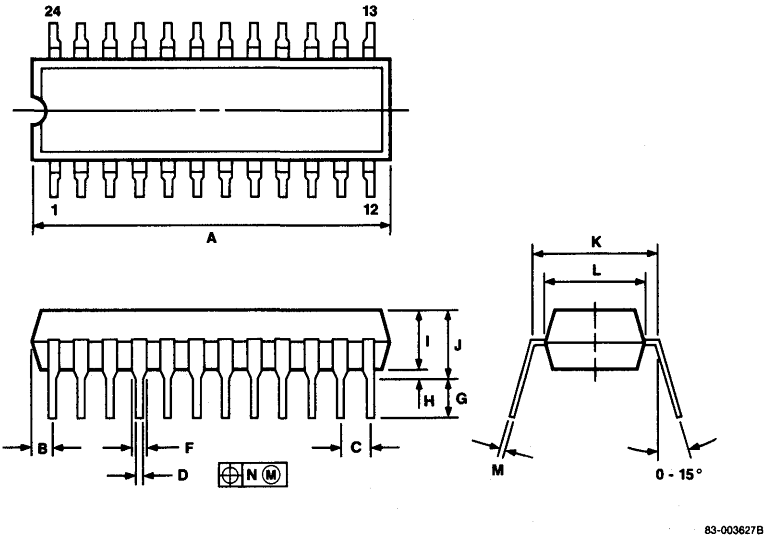
24-Pin Plastic DIP (400 mil)

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



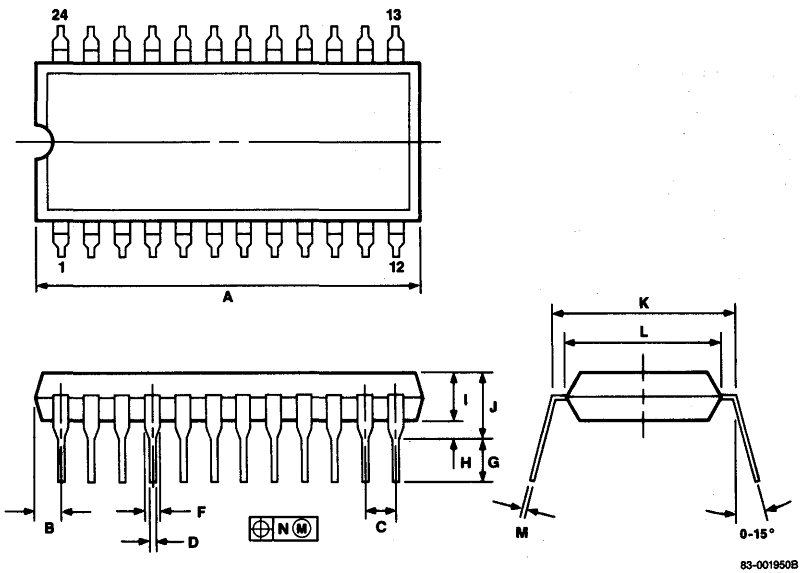
24-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



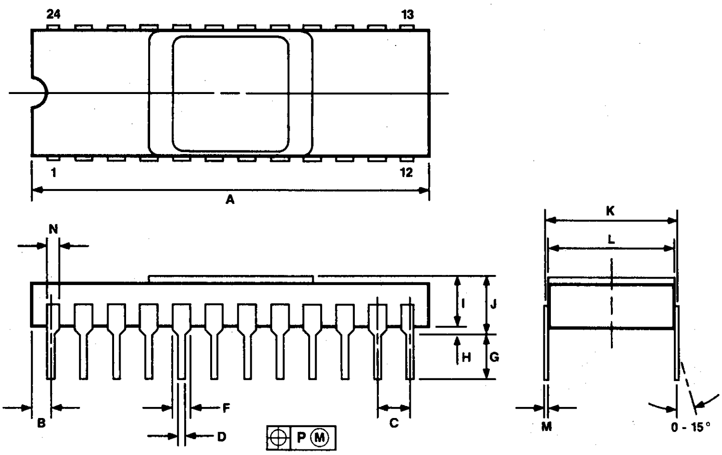
24-Pin Ceramic DIP (400 mil)

Item	Millimeters	Inches
A	33.02 max	1.30 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ± .002
F	1.25 min	.049 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	2.74	.108
J	4.57 max	.180 max
K	10.16 [TP]	.400 [TP]
L	10.0	.394
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	1.00 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003579B

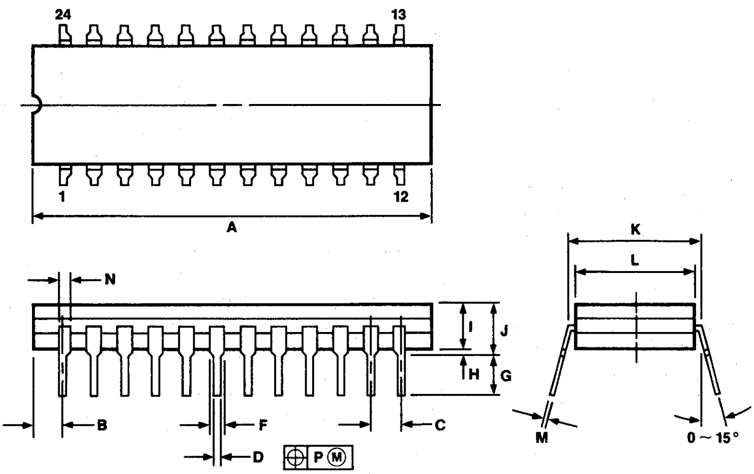
24-Pin Cerdip (400 mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.70	.382
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



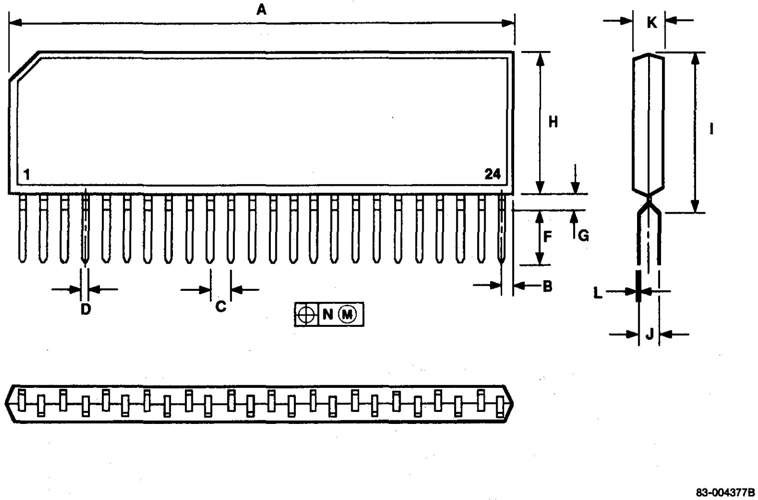
83-005012B

24-Pin Plastic ZIP

Item	Millimeters	Inches
A	31.75 max	1.25 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	0.50 ± 0.10	$.020 {}^{+.004}_{-.005}$
F	3.30 ± 0.50	$.130 \pm .02$
G	1.00 min	.039 min
H	8.90 max	.350 max
I	10.16 max	.400 max
J	2.54 [TP]	.100 [TP]
K	2.80 ± 0.20	$.110 {}^{+.009}_{-.008}$
L	$0.25 {}^{+0.10}_{-0.05}$	$.010 {}^{+.004}_{-.003}$
N	ϕ 0.25	ϕ .010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

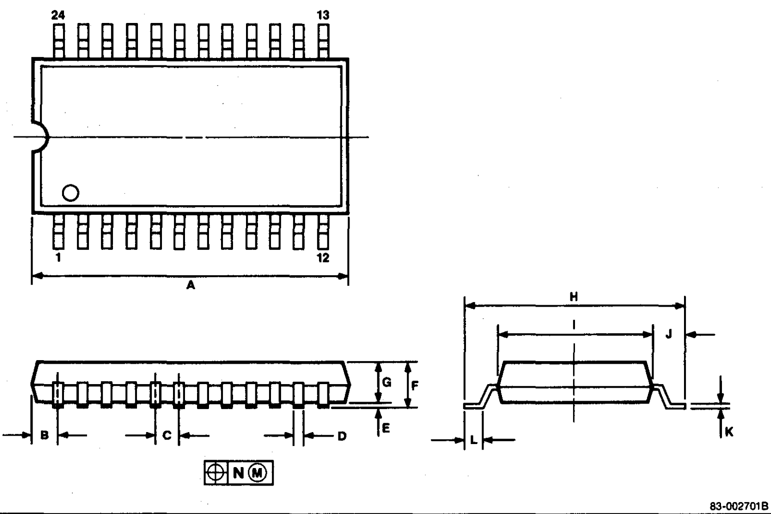


24-Pin Plastic Miniflat

Item	Millimeters	Inches
A	16.51 max	.650 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	0.40 ± 0.10	$.016 {}^{+.004}_{-.005}$
E	$0.1 {}^{+0.2}_{-0.1}$	$.004 {}^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	12.2 ± 0.3	$.480 {}^{+.013}_{-.012}$
I	8.4	.331
J	1.9	.075
K	$0.15 {}^{+0.10}_{-0.05}$	$.006 {}^{+.004}_{-.002}$
L	0.9 ± 0.2	$.035 {}^{+.009}_{-.008}$
N	0.12	.005

Notes:

[1] Each lead centerline is located within 0.12 mm [.005 inch] of its true position [TP] at maximum material condition.



10

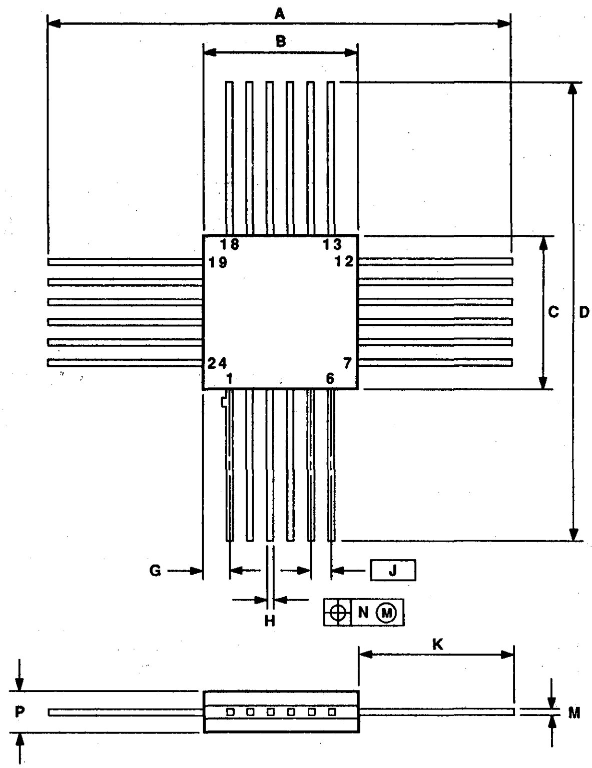
 NEC

24-Pin Ceramic Flatpack

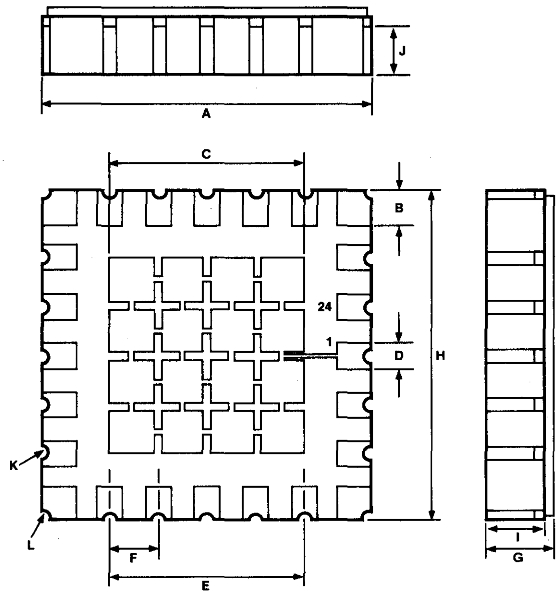
Item	Millimeters	Inches
A	28.5 ± 1.0	1.122 ± .040
B	9.6	.378
C	9.6	.378
D	28.5 ± 1.0	1.122 ± .040
G	1.62	.064
H	0.4 ± 0.1	$.016 {}^{+.004}_{-.005}$
J	1.27 [TP]	.050 [TP]
K	9.45 ± 1.0	.372 ± .040
M	$0.15 {}^{+0.10}_{-0.05}$	$.006 {}^{+.004}_{-.002}$
N	0.25	.010
P	2.6 max	.103 max

Note:

[1] Each lead centerline is located within 0.25 mm [0.010 inch] of its true position [TP] at maximum material condition.



24-Pin Ceramic LCC



Item	Millimeters	Inches
A	8.51 ±0.4	.335 ±.016
B	.89 ±0.2	.035 ±.008
C	5.14	.202
D	.64 ±0.1	.025 $^{+.005}_{-.004}$
E	5.08	.200
F	1.27	.050
G	2.0 max	.079 max
H	8.51 ±0.4	.335 ±.016
I	1.4	.055
J	1.02	.040
K	0.2R	.008R
L	0.3R	.012R

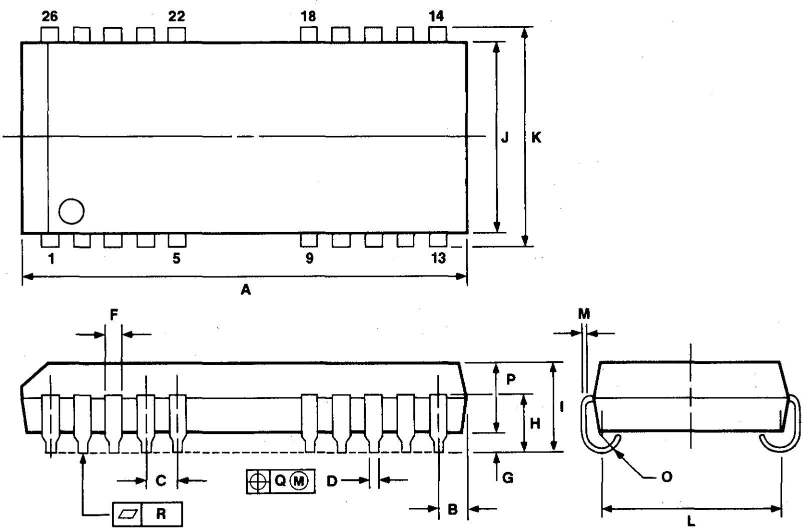
83-003582B

26/20-Pin Plastic SOJ

Item	Millimeters	Inches
A	17.4 $^{+0.20}_{-0.35}$	.685 $^{+.008}_{-.013}$
B	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
C	1.27 [TP]	.050 [TP]
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
F	0.60	.024
G	0.8 min	.031 min
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	3.5 ± 0.2	.138 ± .008
J	7.57	.298
K	8.47 ±0.2	.333 $^{+.009}_{-.008}$
L	6.73 ± 0.2	.265 ± .008
M	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$
O	0.85 rad	.033 rad
P	2.60	.102
Q	0.12	.005
R	0.15	.006

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.



83-003635B

10

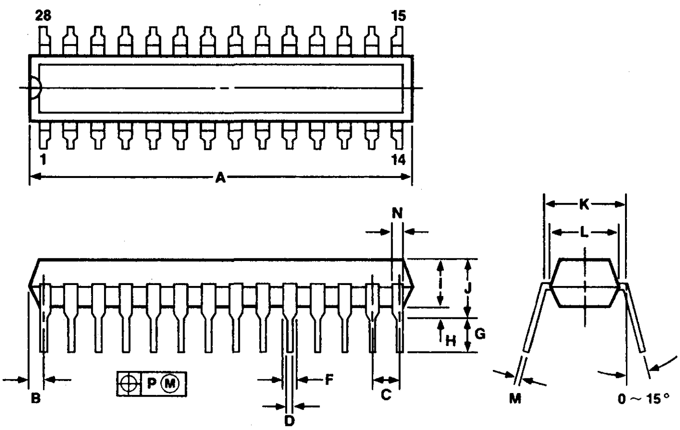
28-Pin Plastic DIP (300 mil)

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	1.0 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-004152B

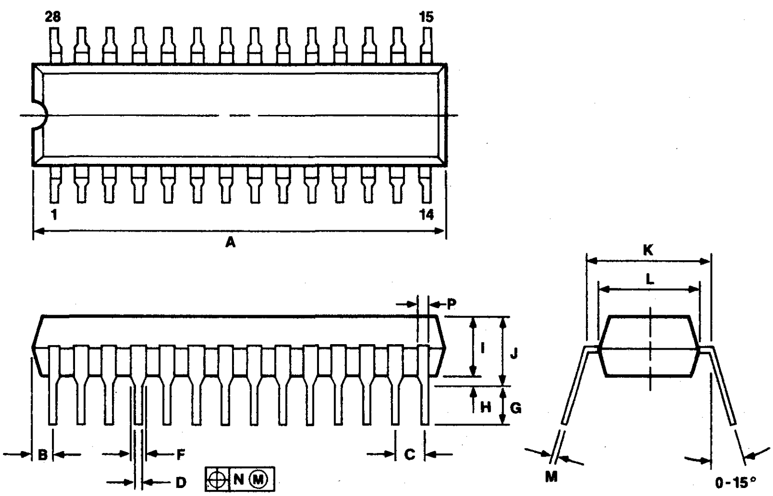
28-Pin Plastic DIP (400 mil)

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.10 min	.043 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	10.16 [TP]	.400 [TP]
L	8.60	.339
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.90 min	.035 min

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-004720B

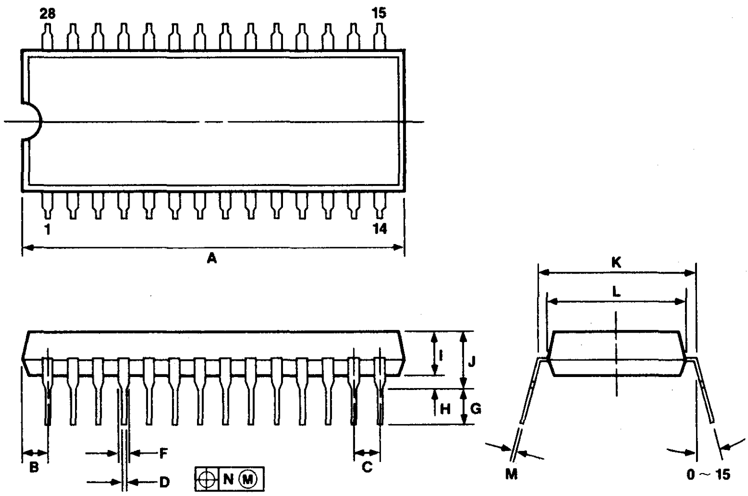
28-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.5 ± 0.1	$.020^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.6 ± 0.30	.142 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.20	.520
M	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-001675B

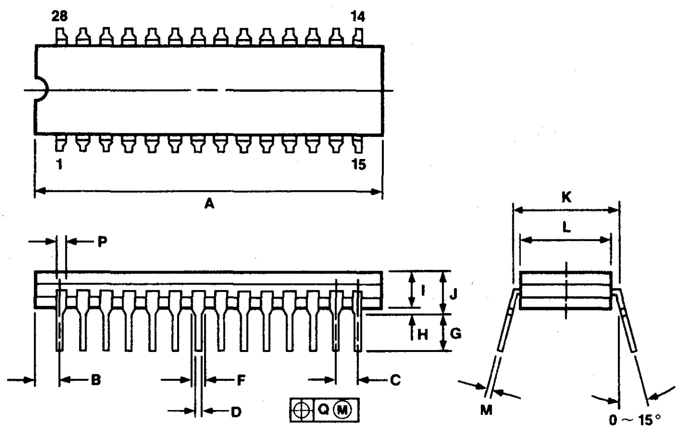
28-Pin Cerdip (400 mil)

Item	Millimeters	Inches
A	38.10 max	1.50 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	4.00	.157
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.65	.380
M	0.25 ± 0.05	$.010^{+.002}_{-.003}$
N	0.25	.010
P	0.89 min	.035 min
Q	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-005015B

10

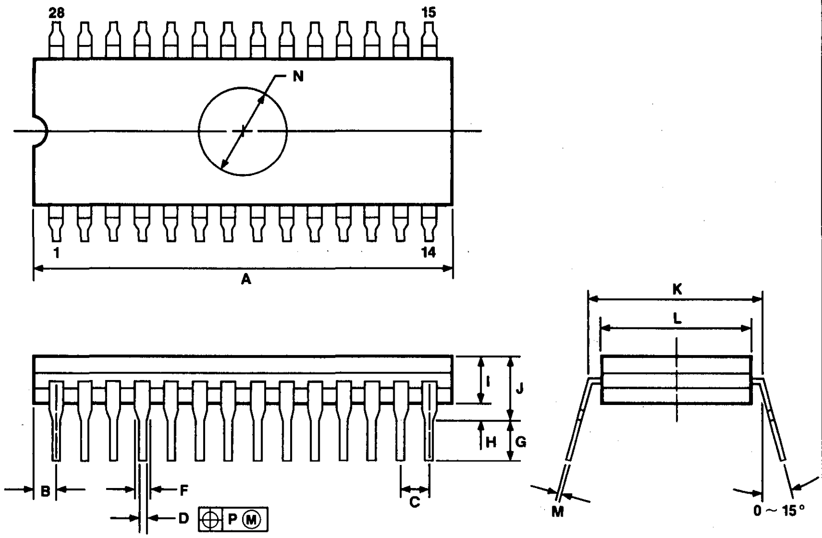
28-Pin Cerdip (600 mil)

Item	Millimeters	Inches
A	38.10 max	1.50 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	$.010^{+.002}_{-.003}$
N	ϕ 8.89 dia	ϕ .350 dia
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



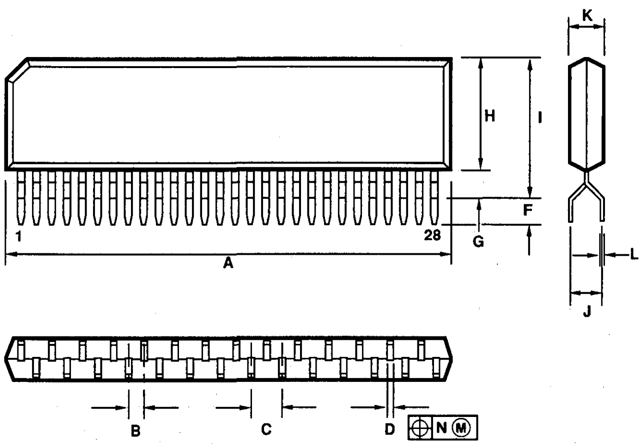
83-001795B

28-Pin Plastic ZIP

Item	Millimeters	Inches
A	36.83 max	1.45 max
B	1.27 [TP]	.050 [TP]
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	3.30 ± 0.50	.130 ± .020
G	1.00 min	.039 min
H	8.90 max	.350 max
I	10.16 max	.400 max
J	2.54 [TP]	.100 [TP]
K	2.80± 0.20	$.110^{+.009}_{-.008}$
L	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
N	ϕ 0.25	ϕ .010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.



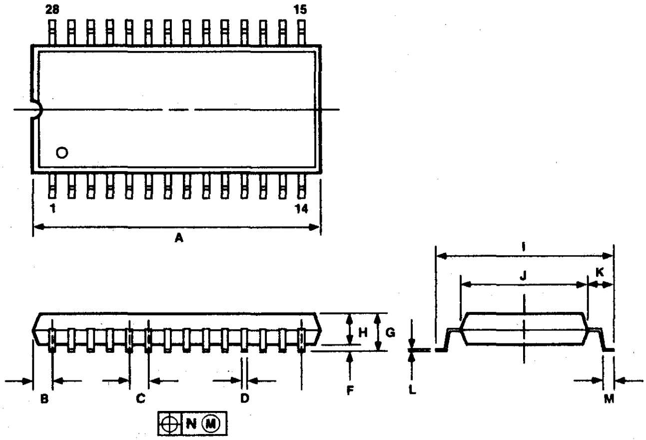
83-004898B

28-Pin Plastic Miniflat #1

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	.40 ± .10	$.016\ ^{+.004}_{-.005}$
E	16.51	.650
F	$.1\ ^{+.2}_{-.1}$	$.004\ ^{+.008}_{-.004}$
G	2.5 max	.099 max
H	2.00	.079
I	11.8 ± .3	$.465\ ^{+.012}_{-.013}$
J	8.4	.331
K	1.7	.067
L	$.15\ ^{+.10}_{-.05}$	$.006\ ^{+.004}_{-.002}$
M	.7 ± .2	$.028\ ^{+.008}_{-.009}$

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.



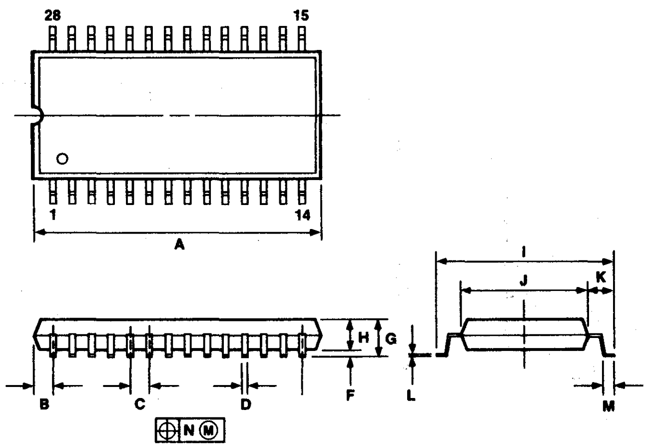
83-001676B

28-Pin Plastic Miniflat #2

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 [TP]	.050 [TP]
D	0.40 ± 0.10	$.016\ ^{+.004}_{-.005}$
F	0.1 ± 0.1	$.004\ ^{+.005}_{-.004}$
G	3.0 max	.118 max
H	2.55	.100
I	11.8 ± 0.3	$.465\ ^{+.012}_{-.013}$
J	8.4	.331
K	1.7	.067
L	$0.15\ ^{+0.10}_{-0.05}$	$.006\ ^{+.004}_{-.002}$
M	0.7 ± 0.2	$.028\ ^{+.008}_{-.009}$
N	0.12	.005

Notes:

[1] Each lead centerline is located within 0.12 mm [.005 inch] of its true position [TP] at maximum material condition.



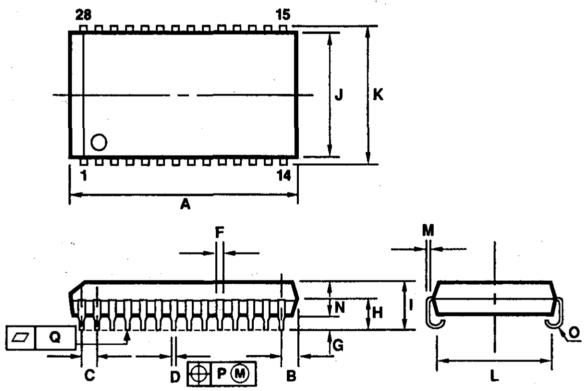
83-004114B

28-Pin Plastic SOJ

Item	Millimeters	Inches
A	18.67 $^{+0.20}_{+0.35}$	.735 $^{+.008}_{-.014}$
B	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
C	1.27 [TP]	.050 [TP]
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
F	0.600	.024
G	0.800 min	.031 min
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	3.5 ± 0.2	.138 ± .008
J	10.16	.400
K	11.18 ± 0.20	.440 ± .008
L	9.40 ± 0.20	.370 ± .008
M	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$
N	2.6	.102
O	0.85R	.033R
P	0.12	.005
Q	0.15	.006

Notes:

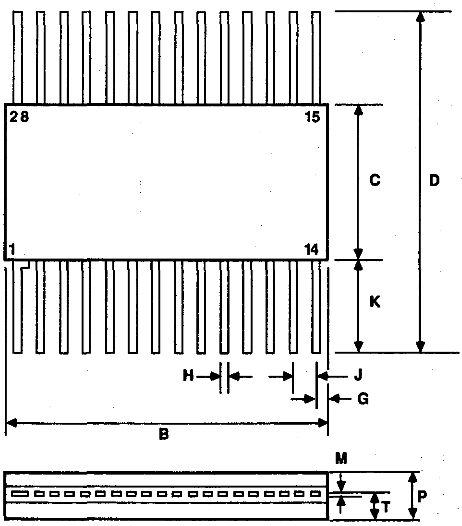
[1] Each lead centerline is located within 0.12 mm [.005 inch] of its true position [TP] at maximum material condition.



83-004897B

28-Pin Ceramic Flatpack

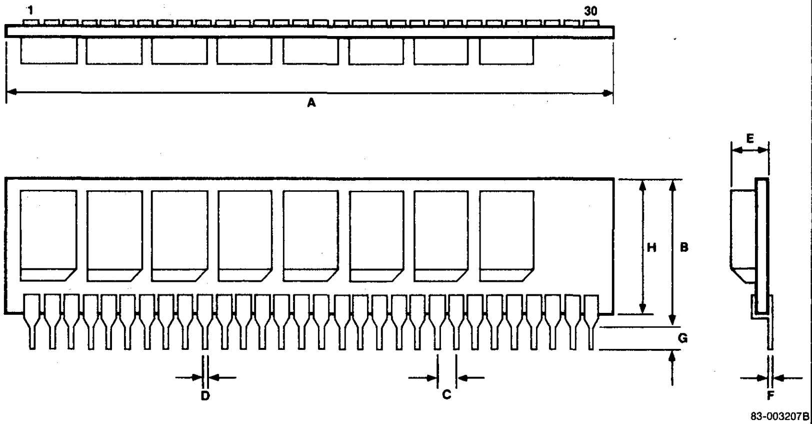
Item	Millimeters	Inches
B	17.5	.689
C	9.84	.387
D	29.0	1.142
G	0.50	.020
H	0.43	.017
J	1.27	.050
K	9.58	.377
M	0.15	.006
P	2.18 max	.086 max
T	1.14 max	.045 max



83IH-4510B

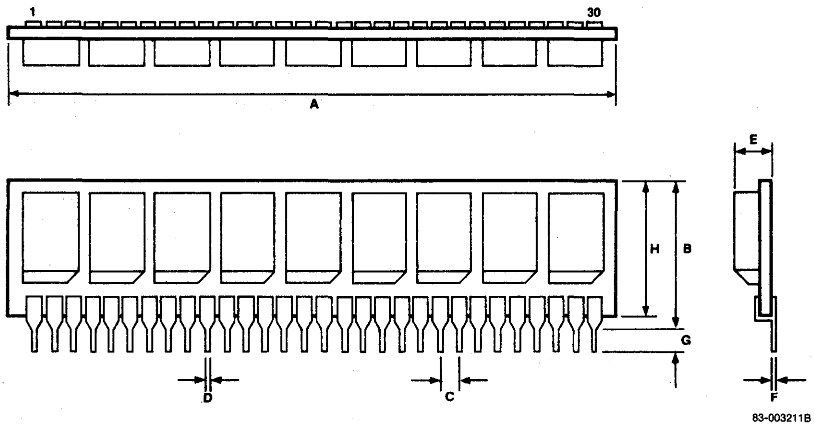
30-Pin SIMM (Leaded) #1

Item	Millimeters	Inches
A	78.90	3.106
B	18.00 max	.709 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157
H	16.76	.660



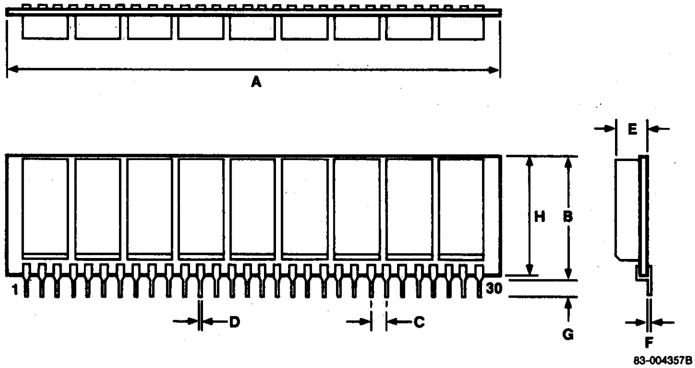
30-Pin SIMM (Leaded) #2

Item	Millimeters	Inches
A	78.90	3.106
B	18.00 max	.709 max
C	2.54	.100
D	.45	.018
E	5.30 max	.209 max
F	.25	.010
G	4.00	.157
H	16.76	.660



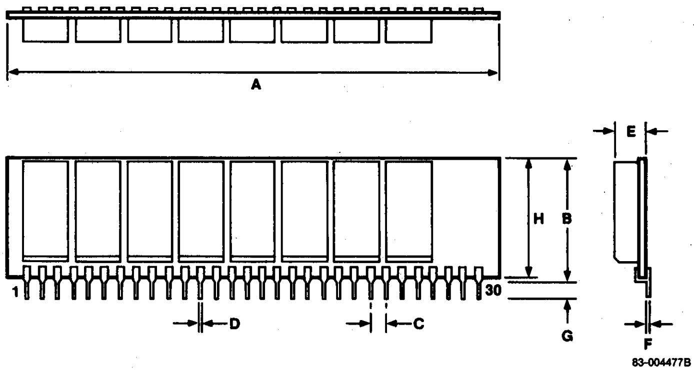
30-Pin SIMM (Leaded) #3

Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 +.021 −.020
B	21.6 max	.851 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.217 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	20.0	.787



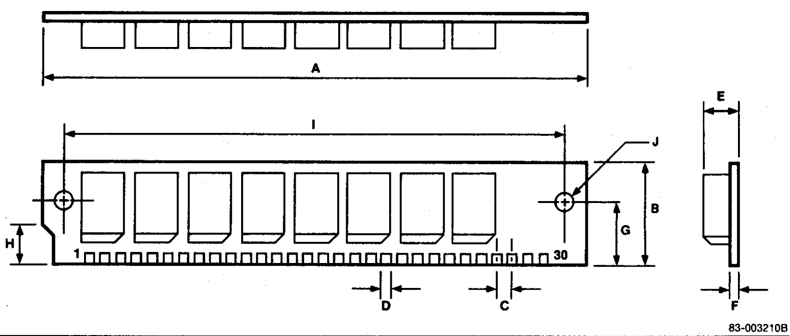
30-Pin SIMM (Leaded) #4

Item	Millimeters	Inches
A	80.3 ± 0.5	3.161 +.021 −.020
B	21.6 max	.851 max
C	2.54 [TP]	.100 [TP]
D	0.50	.020
E	5.5 max	.217 max
F	0.25	.010
G	3.4 ± 0.7	.134 ± .028
H	20.0	.787



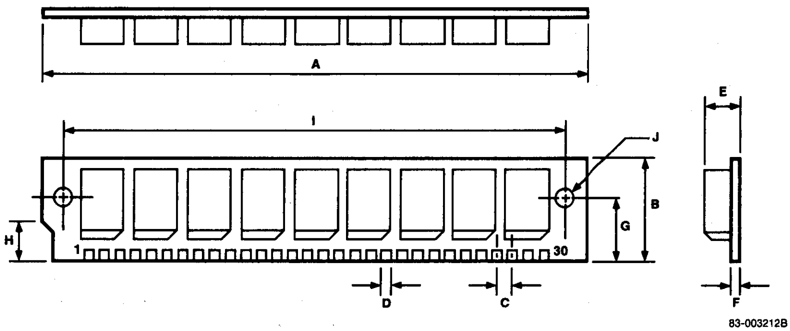
30-Pin SIMM (Socket Mountable) #1

Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



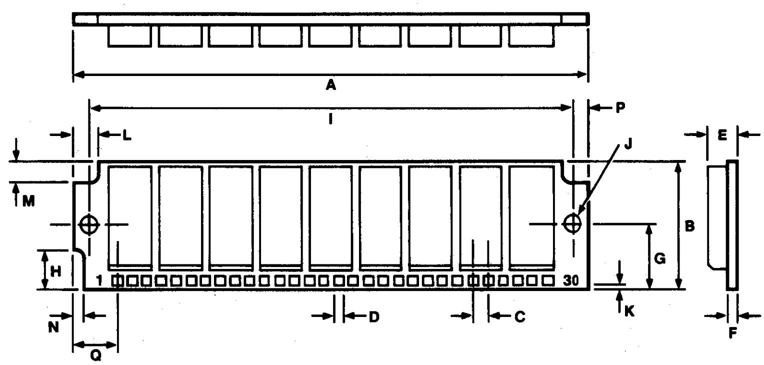
30-Pin SIMM (Socket Mountable) #2

Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



30-Pin SIMM (Socket Mountable) #3

Item	Millimeters	Inches
A	88.90 ± 0.5	3.500 ± .020
B	20.0	.787
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ± 0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300



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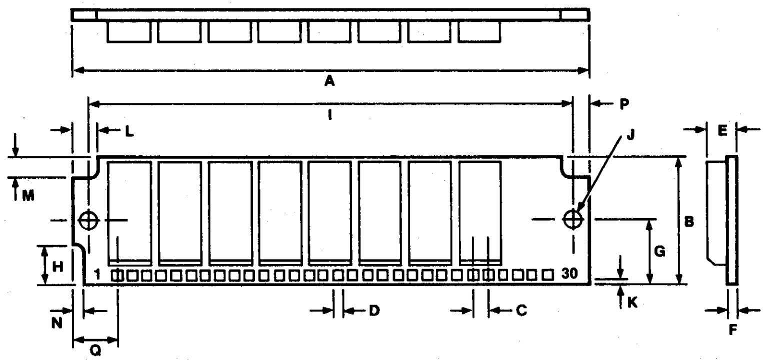
30-Pin SIMM (Socket Mountable) #4

Item	Millimeters	Inches
A	88.90 ± 0.5	3.500 ± .020
B	20.0	.787
C	2.54 [TP]	.100 [TP]
D	1.77	.070
E	5.28 max	.208 max
F	1.27 ± 0.15	.050 ± .006
G	10.16	.400
H	6.35	.250
I	82.14	3.234
J	3.18 dia	.125 dia
K	0.2	.008
L	3.56	.140
M	3.5	.138
N	2.03	.080
P	3.38	.133
Q	7.62	.300



83-004478B

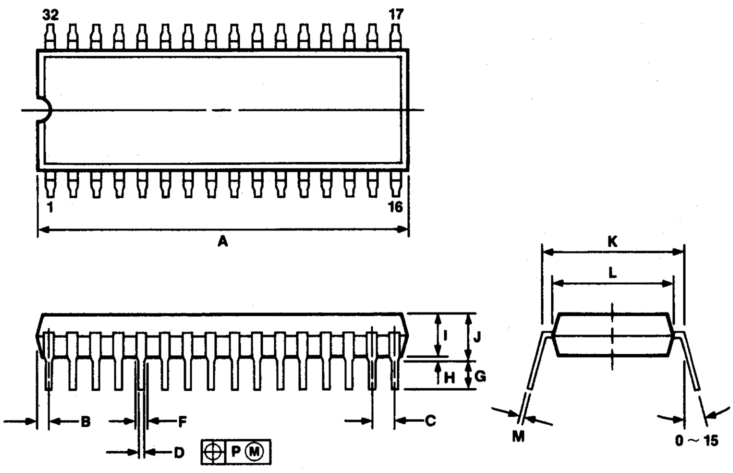
32-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	40.64 max	1.6 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.2 ± 0.30	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.9 min	.035 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

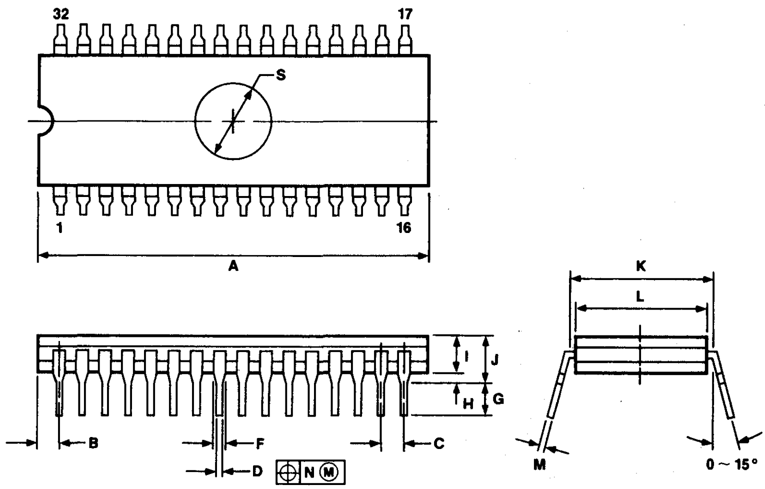


83-005024B

32-Pin Cerdip (600 mil) #1

Item	Millimeters	Inches
A	43.18 max	1.700 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
S	ϕ 9.66	ϕ .380

Notes:
[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.

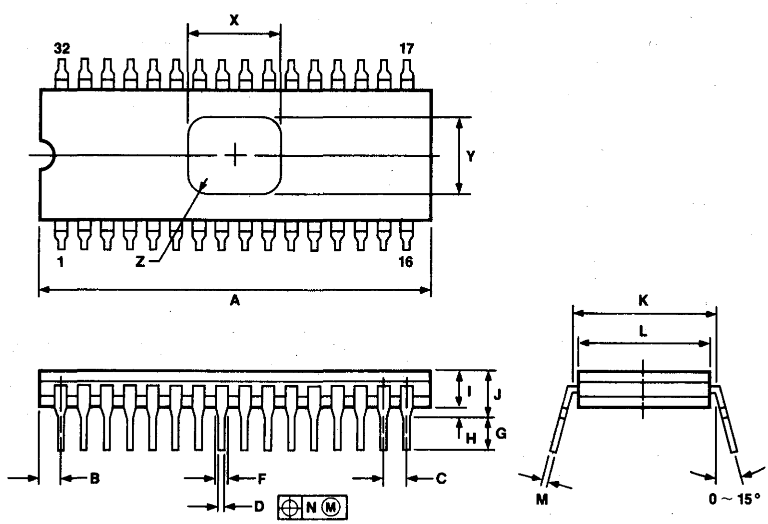


83-005013B

32-Pin Cerdip (600 mil) #2

Item	Millimeters	Inches
A	43.18 max	1.700 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
X	12.50	.492
Y	8.50	.335
Z	4-R2.0	4-R0.079

Notes:
[1] Each lead centerline is located within 0.25 mm [.01 inch] of its true position [TP] at maximum material condition.
[2] Item "K" to center of leads when formed parallel.



83-005105B

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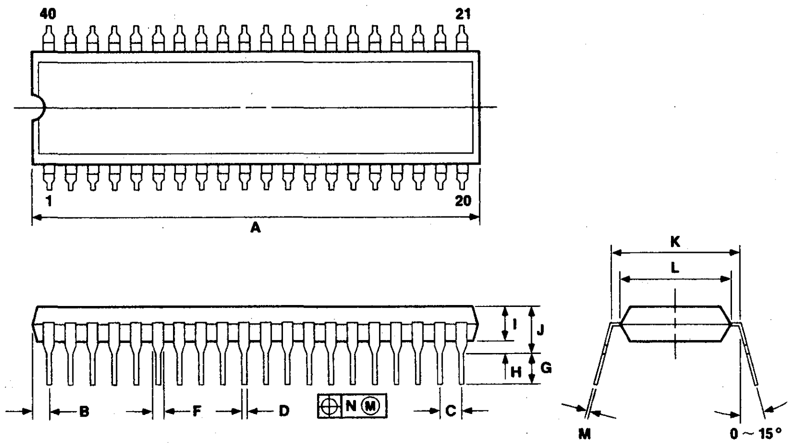
40-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.6 ± 0.3	.142 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-001399B

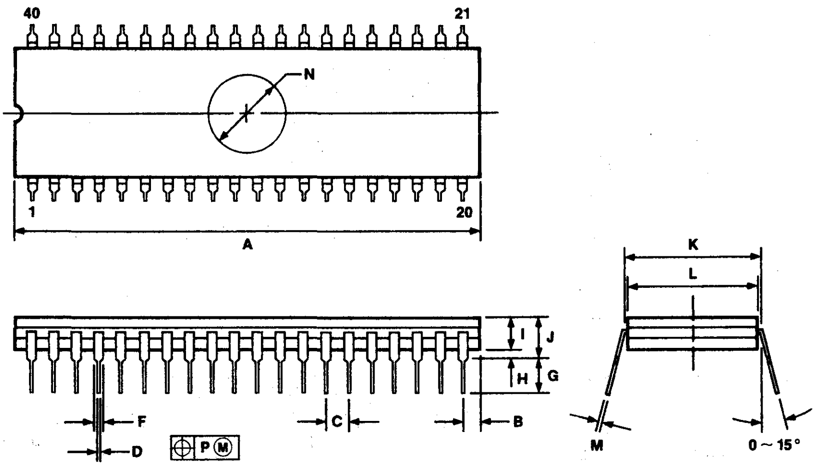
40-Pin Cerdip (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	14.66	.577
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	8.89 dia	.350 dia
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003631B

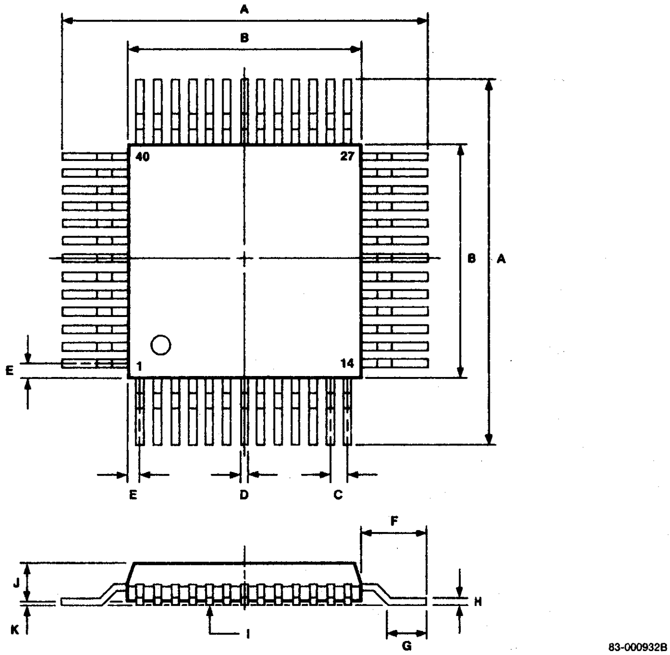
52-Pin Plastic Miniflat

Item	Millimeters	Inches
A	21.04 ± 0.4	.827 ± .016
B	14 ± 0.2	.551 $^{+.009}_{-.008}$
C	1.0 [TP]	.039 [TP]
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	1.0	.039
F	3.5 ± 0.2	.138 $^{+.008}_{-.009}$
G	2.2 ± 0.2	.087 $^{+.008}_{-.009}$
H	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
I	0.15	.006
J	2.6 $^{+0.2}_{-0.1}$	.102 $^{+.009}_{-.004}$
K	0.1 ± 0.1	.004 ± .004

Notes:

[1] Each lead centerline is located within 0.20 mm [.008 inch] of its true position [TP] at maximum material condition.

[2] Flat within 0.15 mm [.006 inch] total.



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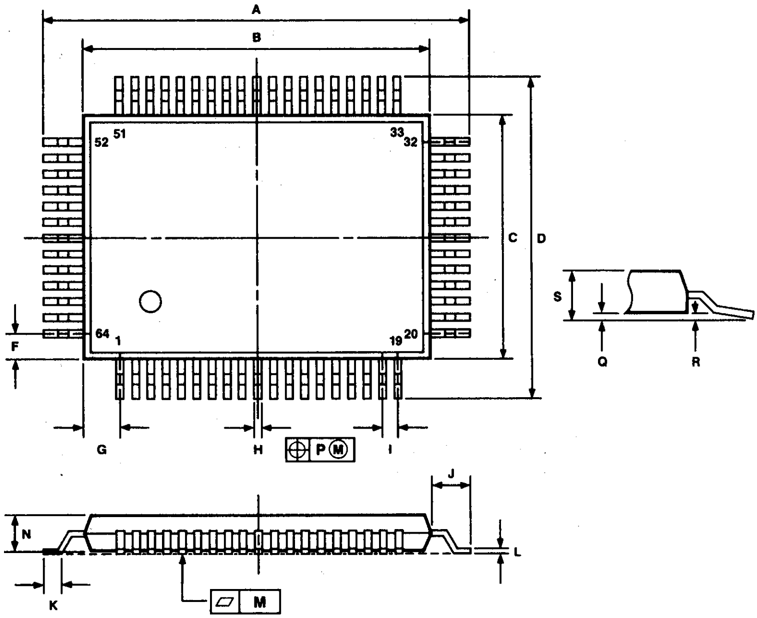
64-Pin Plastic Quad Flatpack

Item	Millimeters	Inches
A	23.6 ± 0.40	.929 ± .016
B	20 ± 0.20	.787 $^{+.009}_{-.008}$
C	14 ± 0.20	.551 $^{+.009}_{-.008}$
D	17.6 ± 0.40	.693 ± .016
F	1.0	.039
G	1.0	.039
H	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
I	1.0 [TP]	.039 [TP]
J	1.8 ± 0.20	.071 ± .008
K	0.8 ± 0.20	.031 $^{+.009}_{-.008}$
L	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
M	0.15	.006
N	2.70	.106
P	0.20	.008
Q	0.1 ± 0.10	.004 ± .004
R	0.1 ± 0.10	.004 ± .004
S	3.0 max.	.119 max.

Notes:

[1] Each lead centerline is located within 0.20 mm [.008 inch] of its true position [TP] at maximum material condition.

[2] Flat within 0.15 mm [.006 inch] total.



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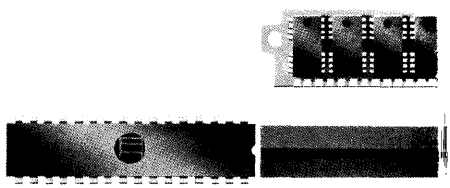

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