μPD7763D

SBB-2-7735
Feb. 1, '85

Speech Spectrum Analysis LSI

Outline

The μPD7763 is a speech spectrum analysis LSI, designed for speech recognition system. The device contains a pre-amplifier, 16-channel BPF , an A/D converter and parallel data interface. A compact and high performance speech recognition system can be constructed with μPD7763 and μPD7764 which performs pattern matching.

Features

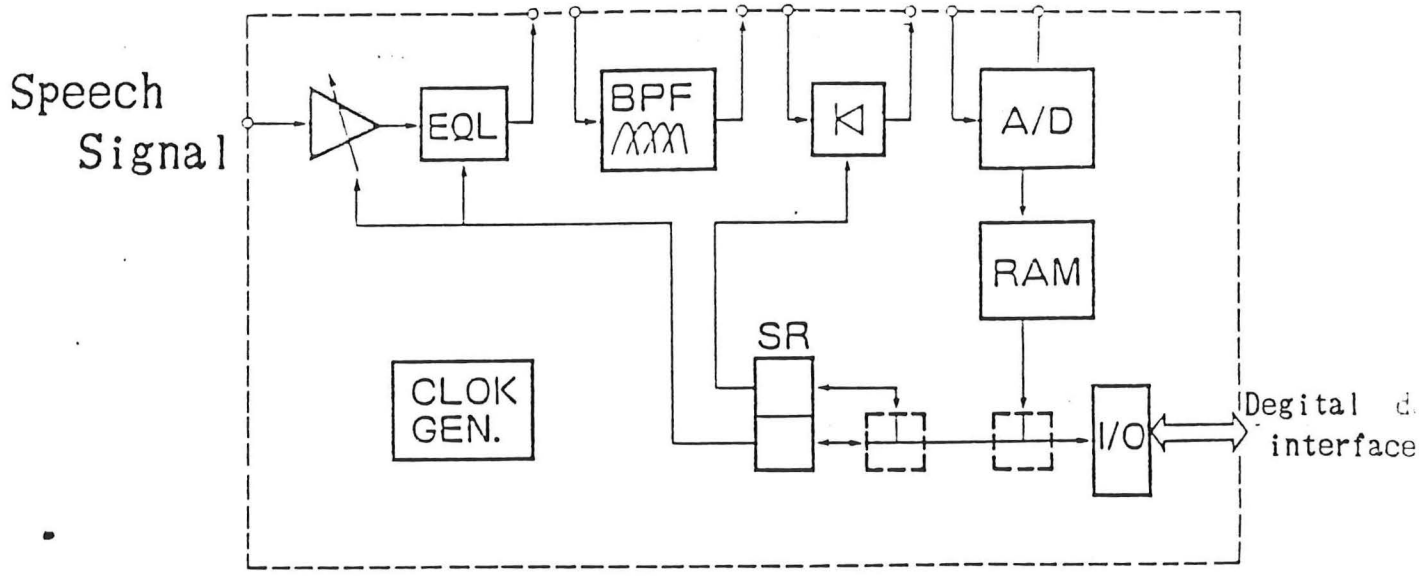
* Single-chip high performance speech spectrum analysis LSI
* Analog interface capable of speech signal input
* CPU paralell bus interface is provided

Specification

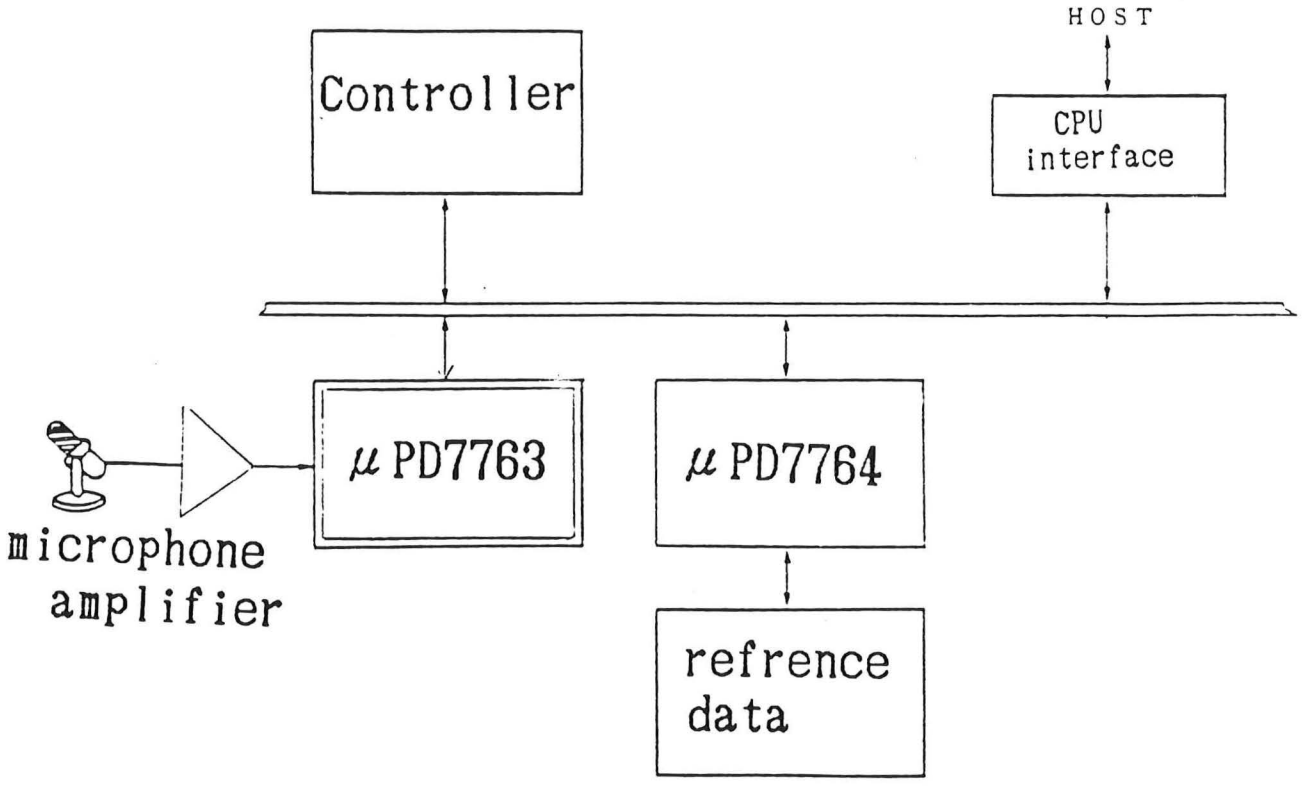
* SPEECH SPECTRUM ANALYSIS
  method : 16 channel BPF
  (center frequency of each BPF : 250 ~ 5400 Hz)
  resolution : 8 bit (8 bit A/D converter)
* ANALOG INTERFACE
  A variable gain pre-amplifier and speech spectrum analyzer are equipped.
  (range of pre-amlifier gain : -11 to 33 dB)

* DIGITAL INTERFACE : 8 bit paralell bus-interface
* PROCESS : CMOS
* POWER SUPPLY : +5V
* PACKAGE : 28 pin ceramic DIP

FUNCTIONAL DIAGRAM



A CONFIGURATION OF RECONGTION SYSTEM



uPD7763

SPEECH SPECTRUM ANALIZER

FUNCTION & FEATURES

(1) 16-Channel BPF Analysis Using Switched Capacitor Filter

(2) 8-bit A/D Converter on-chip

(3) BUS compatible with 8-bit standard CPU

(4) Programmable AMP on-chip (0 to 46.5 dB by 1.5 dB)

(5) Equalizer on-chip

(6) Variable Frame Period (1, 2, 4, 8, 16 or 32 msec)

(7) 4 MHz System Clock

(8) CMOS Technology

(9) +5V Single Power Supply

(10) 28 pin DIP

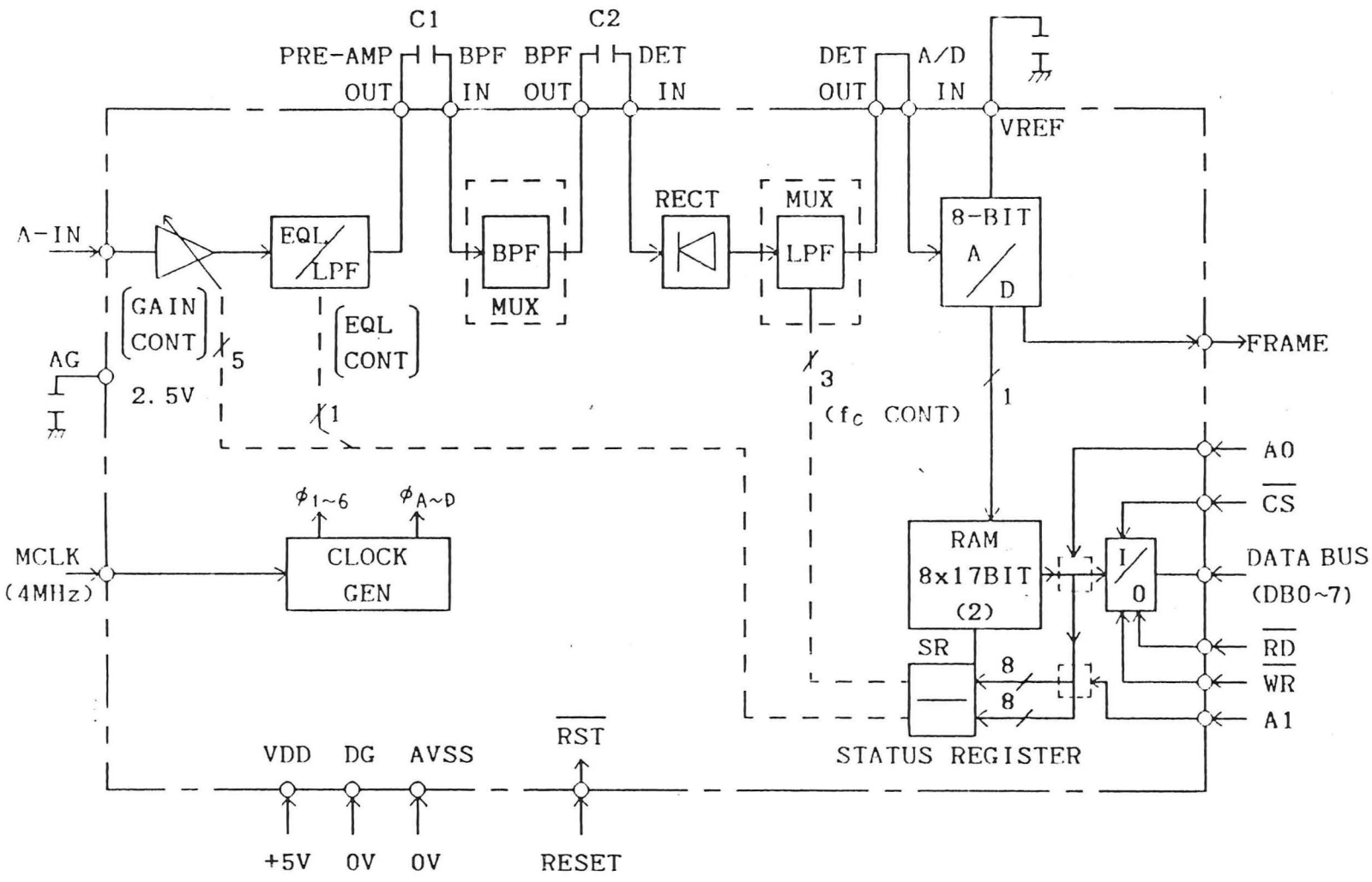


Fig. 1 BLOCK DIAGRAM OF THE uPD7763

f_{sw} = 400 KHz

expand 22 channel

$\frac{400KHz}{22}$ = 18.18k

1 channel switch

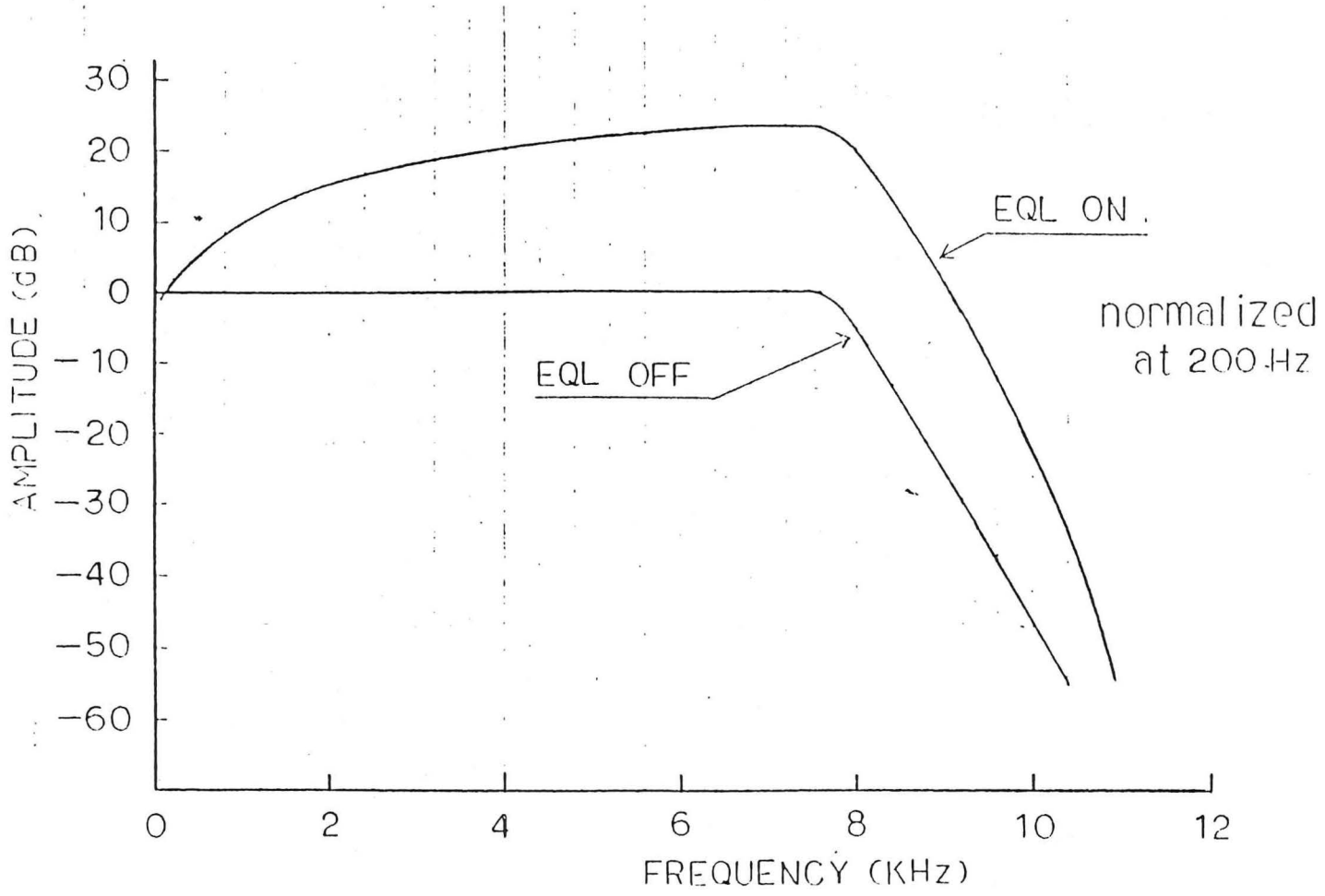


Fig.2 Responses of the pre-amp section

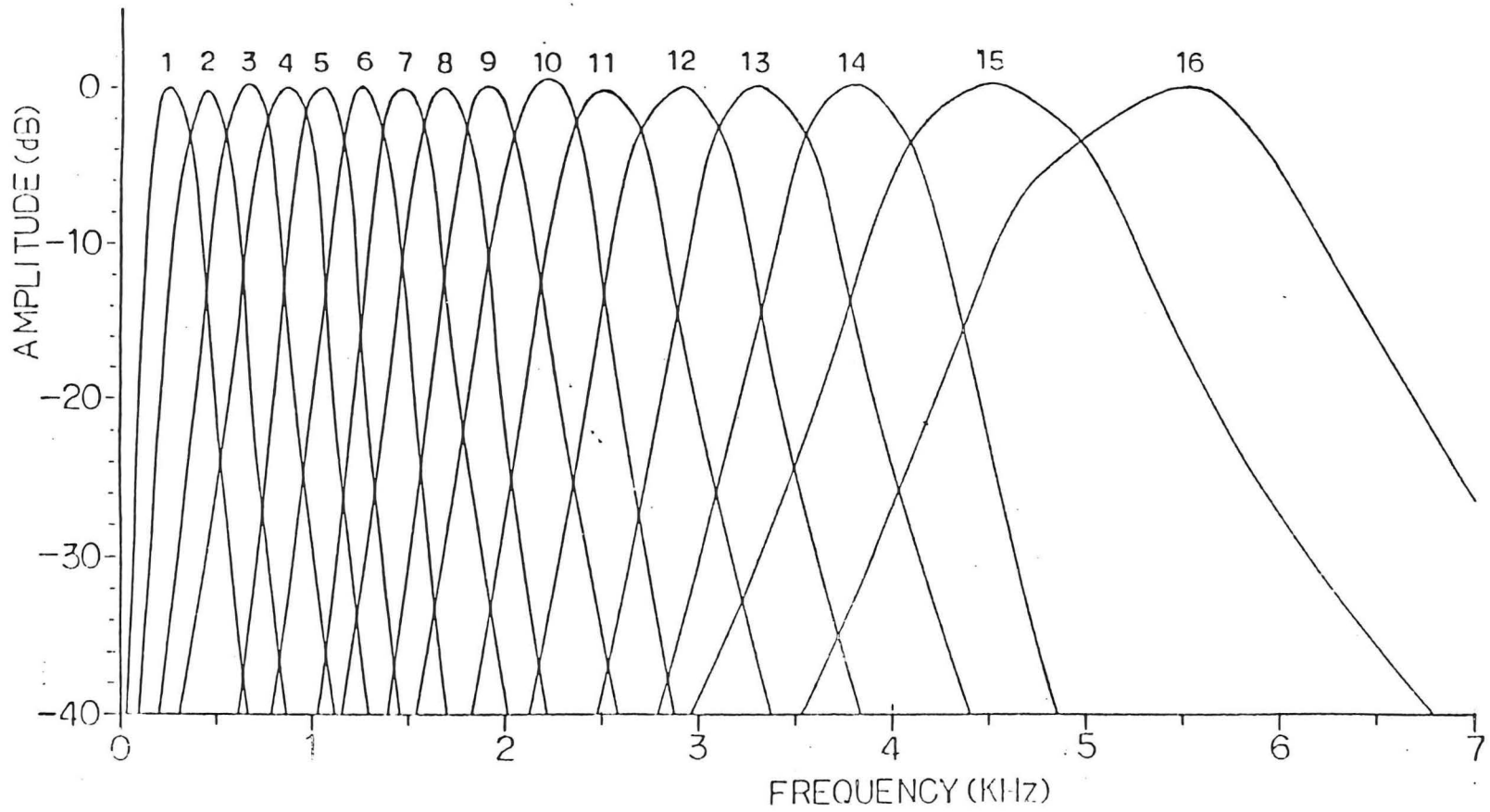


Fig.3 Spectral response of the 16 channel BPF bank

(READ/WRITE OPERATION)

CONTROL TERMINALS					MODE	FUNCTION
CS	RD	WR	A0	A1		
0	1	0	—	0	Write mode	Write status register 0
0	1	0	—	1	Write mode	Write status register 1
0	0	1	1	0	Read mode	Read status register 0
0	0	1	1	1	Read mode	Read status register 1
0	0	1	0	—	Read mode	Read A/D conversion data

STATUS REGISTER BIT FUNCTIONS

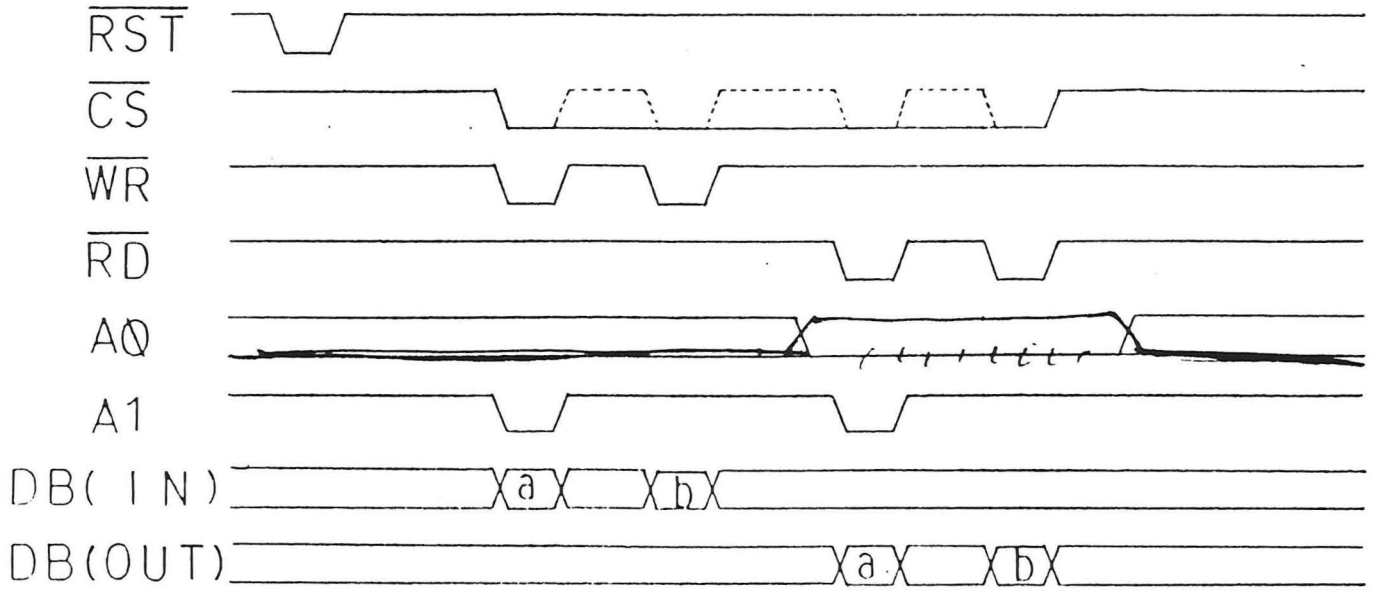
(Status register 0) (A1=0)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
					0	0	0	··· 1 ms	Frame period
					0	0	1	··· 2 ms	
					0	1	0	··· 4 ms	
					0	1	1	··· 8 ms	
					1	0	0	··· 16 ms	
					1	0	1	··· 32 ms	
0	0	0	0	0	·····			0 dB	Level Adjuster relative gain
0	0	0	0	1	·····			1.5 dB	
0	0	0	1	0	·····			3.0 dB	
0	0	0	1	1	·····			4.5 dB	
⋮	⋮	⋮	⋮	⋮	1.5 dB steps				
1	1	1	1	0	·····			45.0 dB	
1	1	1	1	1	·····			46.5 dB	

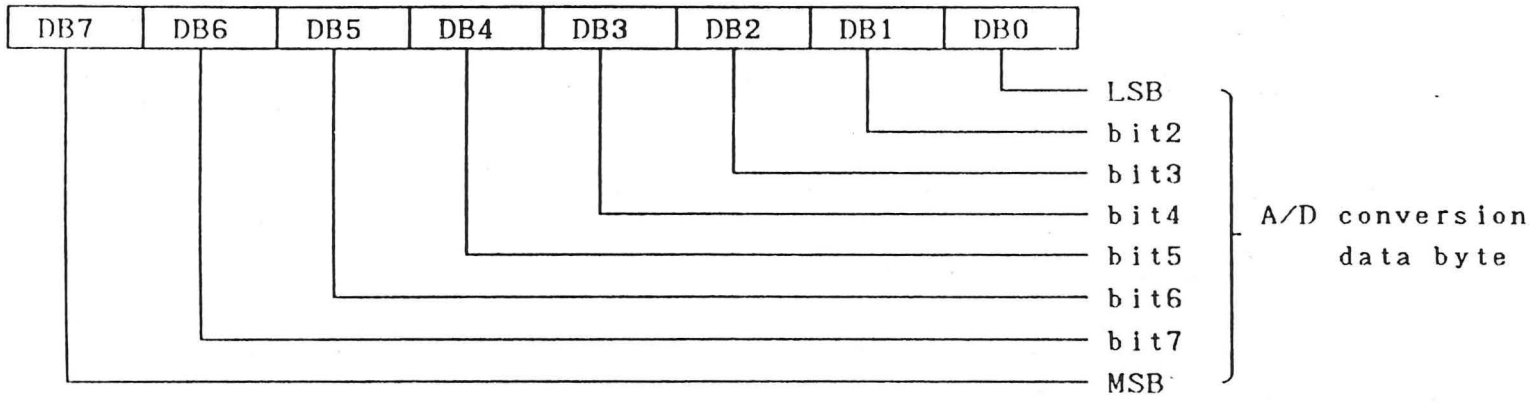
(Status register 1) (A1=1)

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
							0	Equalizer OFF
							1	Equalizer ON
				0	0	0	12.5 HZ	LPF bank Cut off frequency
				0	0	1	25.0 HZ	
				0	1	0	50.0 HZ	
				0	1	1	Null code	
				1	0	0	100 HZ	
				1	0	1	200 HZ	
				1	1	0	400 HZ	

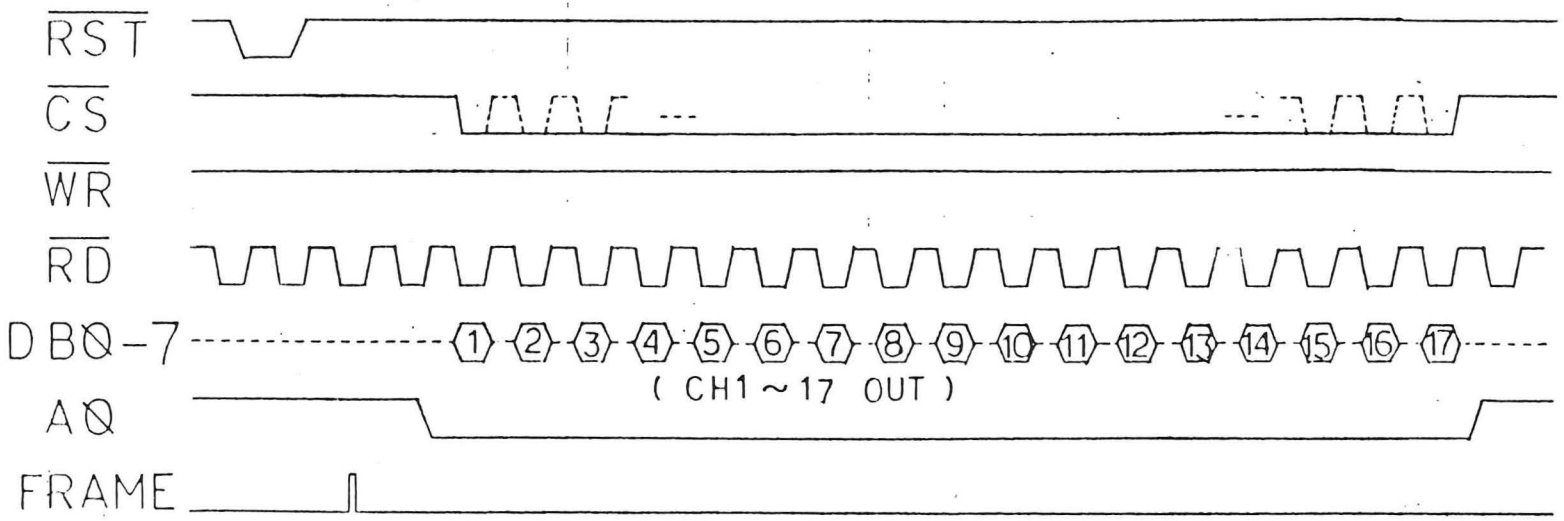
[STATUS REGISTER READ & WRITE MODE]



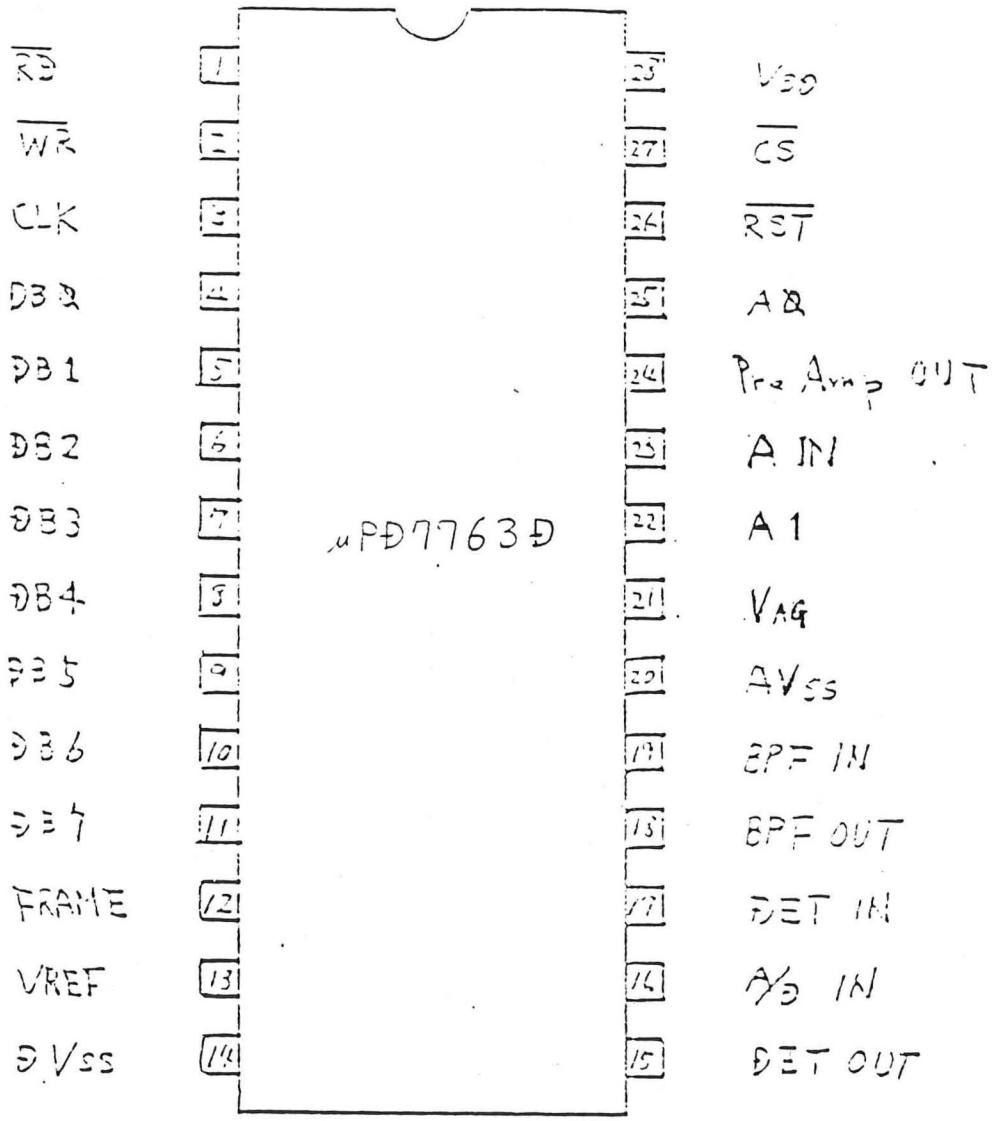
A/D CONVERSION DATA FORMATS



[A/D READ MODE]


RST
CS
WR
RD
DB0-7
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
(CH1 ~ 17 OUT)
A0
FRAME

Pin Connections



μPD7763

Speech Spectrum Analyzer

FUNCTION & FEATURES

- 16-Channel BPF Analysis Using
  Switched Capacitor Filter
- Programmable AMP on-chip
  0 to 46.5 dB by 1.5 dB
- Equalizer on-chip
- 9-bit A/D Converter on-chip
- Variable Frame Period
  1,2,4,8,16 or 32 msec
- 4 MHz System Clock
- CMOS Technology
- +5V Single Power Supply
- 28 pin DIP

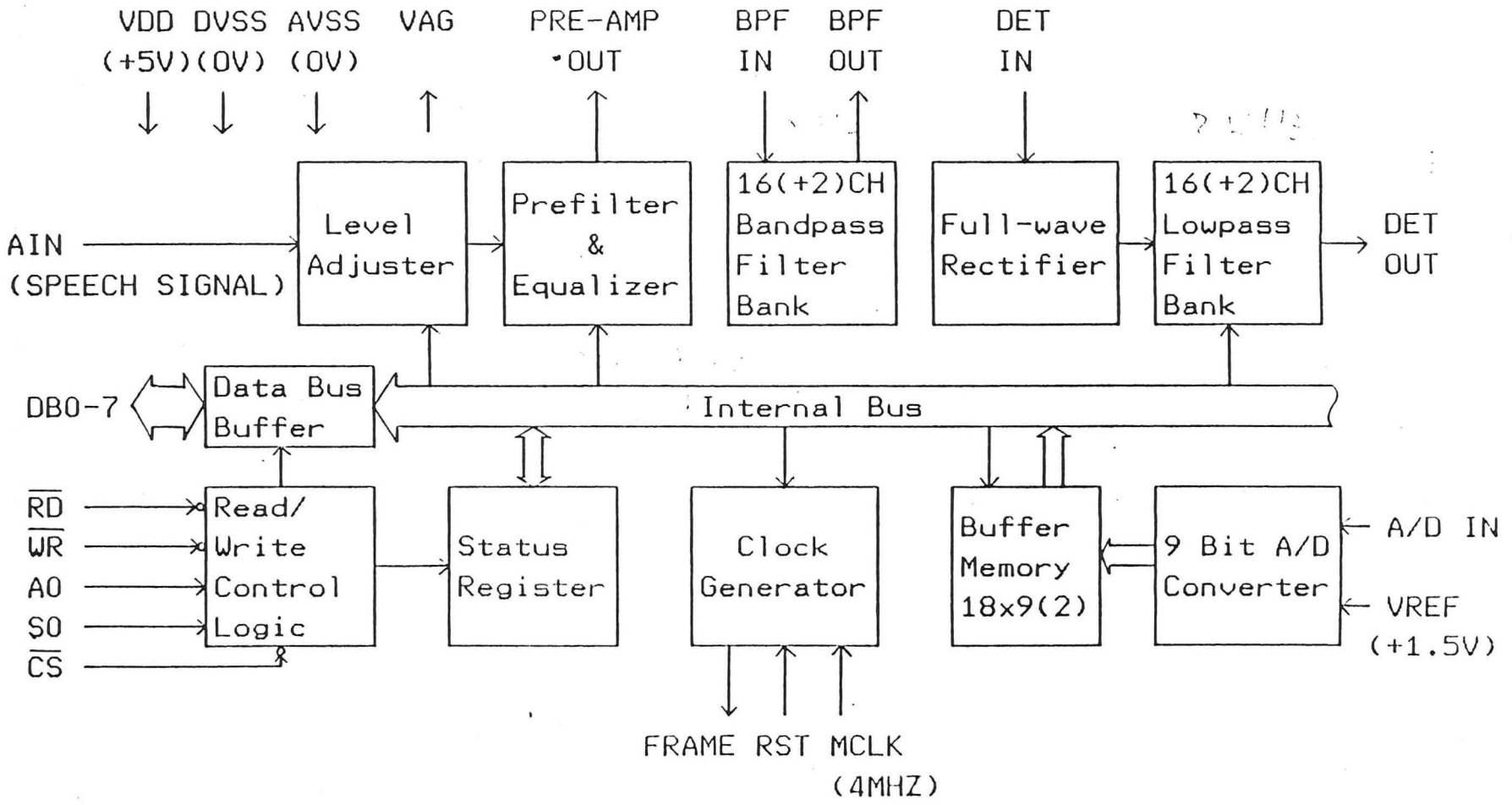


Fig.1 Block Diagram of the μPD7763

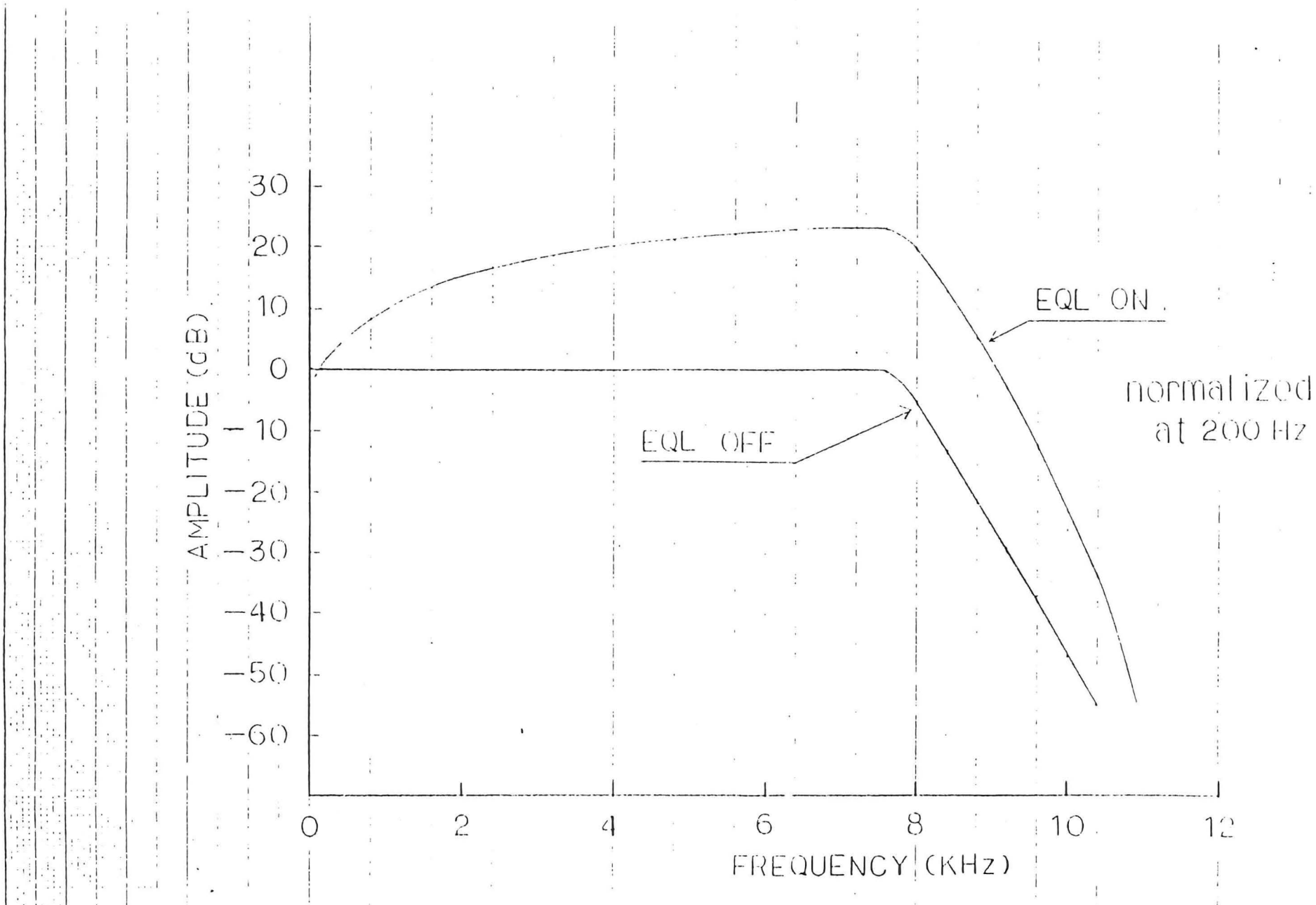


Fig.2 Responses of the pre-amp section

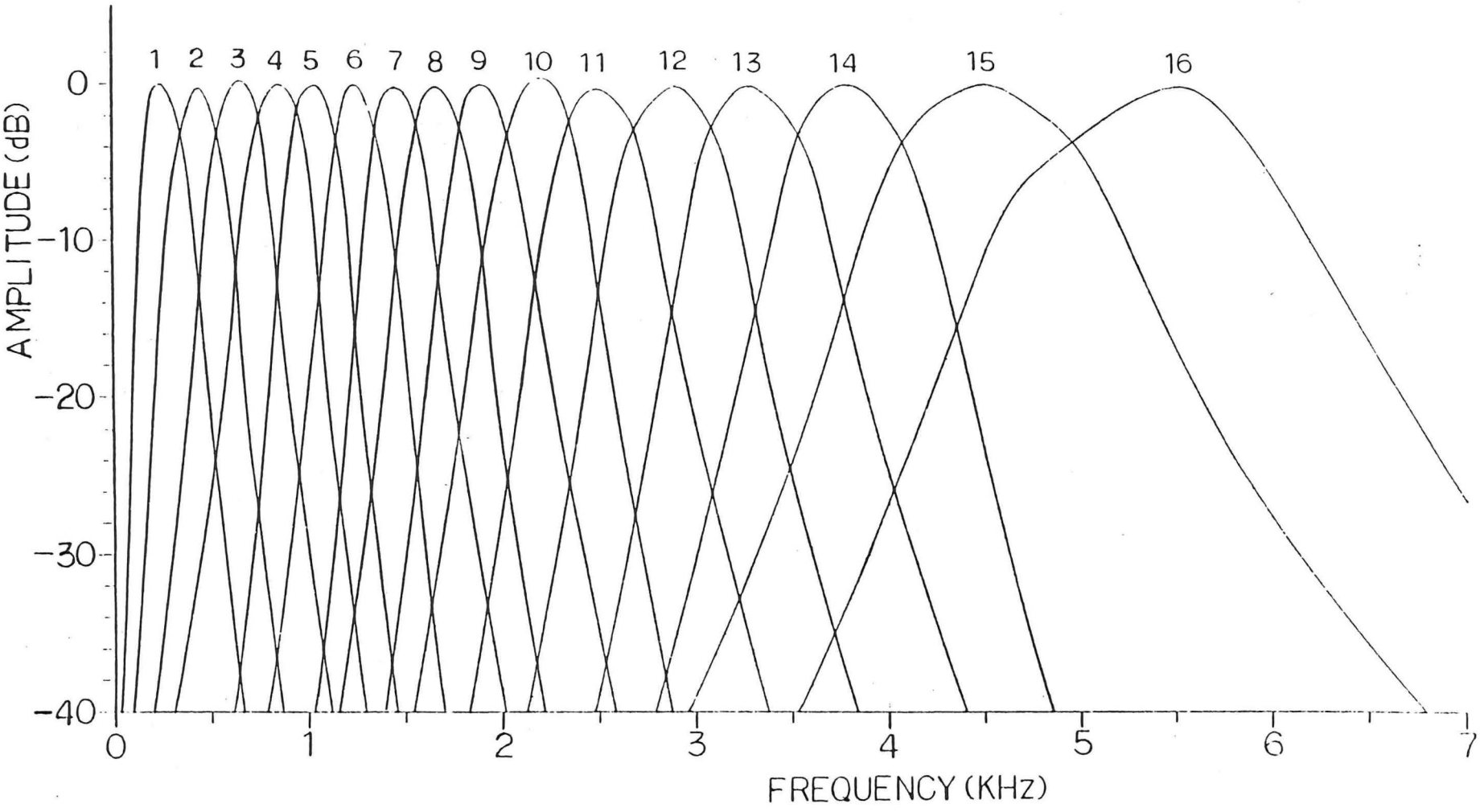


Fig.3 Spectral response of the 16 channel BPF bank

[READ/WRITE OPERATION]

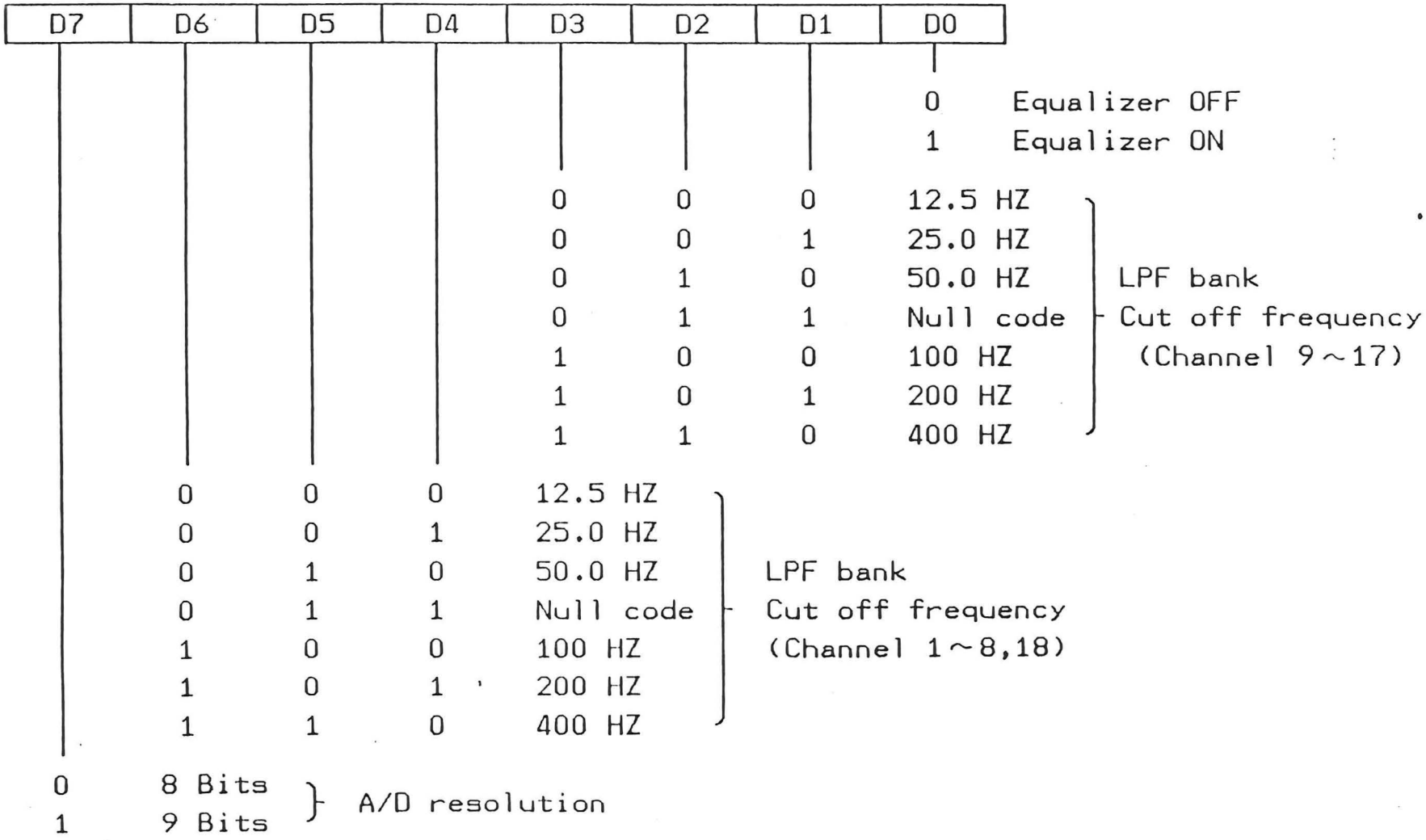
CONTROL TERMINALS					MODE	FUNCTION
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A0	S0		
0	1	0	—	0	Write mode	Write status register 0
0	1	0	—	1	Write mode	Write status register 1
0	0	1	1	0	Read mode	Read status register 0
0	0	1	1	1	Read mode	Read status register 1
0	0	1	0	—	Read mode	Read A/D conversion data

STATUS REGISTER BIT FUNCTIONS

[Status register 0]

D7	D6	D5	D4	D3	D2	D1	D0		
					0	0	0	1 ms	Frame period
					0	0	1	2 ms	
					0	1	0	4 ms	
					0	1	1	8 ms	
					1	0	0	16 ms	
					1	0	1	32 ms	
0	0	0	0	0				0 dB	Level Adjuster relative gain
0	0	0	0	1				1.5 dB	
0	0	0	1	0				3.0 dB	
0	0	0	1	1				4.5 dB	
.	.	.	.	.				1.5 dB steps	
.	.	.	.	.					
.	.	.	.	.					
.	.	.	.	.					
.	.	.	.	.					
1	1	1	1	0				45.0 dB	
1	1	1	1	1				46.5 dB	

[Status register 1]



A/D conversion data formats