Linear Circuits

Panasonic®

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Linear Circuits Op-Amp/ Comparator/Regulator Data Book

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Table of Contents

Index of Parts

Product Number **Page**

CROSS REFERENCE

	Industry Part Number	PANASONIC Part Number
Old Panasonic Part Numbers	AN6914	AN1393
	AN6552	AN4558
	AN6554	AN4136
	AN6564	AN1324
	AN6562	AN1358
	AN6570	AN1741
	AN6572	AN1458
	AN6912	AN1339
RCA	CA1458E	AN1458
	CA1458G	AN1458
	CA324E	AN1324
	CA324G	AN1324
	CA339E	AN1339
	CA339AE	AN1339
	CA358E	AN1358
	CA358G	AN1358
	CA741E	AM1741
	CA741G	AN1741
National Semiconductor	LM1458N	AN1458
	LM2902N	*AN4136
	LM2901D	*AN1339
	LM2904N	*AN1358
	LM2903N	*AN1393
	LM324N	AN1324
	LM3302N	*AN1339
	LM339N	AN1339
	LM339AN	AN1339
	LM358N	AN1358
	LM393N	AN1393
	LM741CN	AN1741
	LM78XXT	AN78XX
	LM78LXXZ	AN78LXX
	LM78MXXP	*AN78MXX
	LM79XXT	AN79XX
	LM320TXX	*AN79XX
	LM340TXX	*AN78XX
	LM4250C	AN4250

	Industry Part Number	PANASONIC Part Number
Hitachi	HA17458PS	AN1458
	HA17741PS	AN1741
	HA17902PS	AN1324
	HA17901P	*AN1339
	HA17904PS	*AN1338
	HA17904PS	*AN1358
Fairchild	μA1458HC	AN1458
	μA258C	AN4558
	μA324C	AN1324
	μA3302C	*AN1339
	μA339C	AN1339
	μA393C	AN1393
	μA4136N	AN4136
	μA4558N	AN4558
	μA741N	AN1741
	μA776	AN4250
Motorola	MC1458P	AN1458
	MC1741CP1	AN1741
	MC2902P	*AN4136
	MC2901P	*AN1339
	MC4558P	AN4558
	MC78XXP	AN78XX
	MC78LXXP	AN78LXX
	MC78MXXP	AN78MXX
	MC79XXP	AN79XX
	MLM324P	AN1324
	MLM324PC	AN1324
	MLM339P	AN1339
	MLM339AP	AN1339
	MLM358P1	AN1358

*Panasonic Functional Equivalent

	Industry Part Number	PANASONIC Part Number
JRC	MJM2902D	AN1324
	MJM2902M	AN1324NS
	MJM2901D	*AN1339
	MJM2904D	*AN1358
	MJM2904M	*AN1358S
	MJM2904D	*AN1358
	MJM2904M	*AN1358S
	MJM2903	*AN1393
	MJM4558D	AN4558
	NJM4558M	AN4558
	NJM4559D	AN6556
NEC	μPCC177C	AN1339
	μPC1251C	AN1358
	μPC1458C	AN1458
	μPC151	AN1741
	μPC151G	AN1741S
	μPC251C	AN1458
	μPC251G	AN1458S
	μPC258C	AN4558
	μPC277C	AN1393
	μPC324C	AN1324
	μPC324G	AN1324NS
	μPC339C	AN1339
	μPC339G	AN6912S
	μPC358L	AN1358
	μPC358G	AN1358S
	μPC358P	AN1358
	μPC393C	AN1393
	μPC393G	AN1393S
	μPC451C	AN1324
	μPC458C	AN4136
	μPC458G	AN6554NS
	μPC4558C	AN4558
	μPC4558G	AN4558S
	μPC4559C	AN6556
	μPC4741C	AN4136
	μPC741C	AN1741

	Industry Part Number	PANASONIC Part Number
Others	HA2720	AN4250
	MA78XXU	AN78XX
	MA78LXXW	AN78LXX
	MA78MXXU	AN78MXX
	MA79XXU	AN79XX
	MAC78XX	AN78XX
	RC4136	AN4136
	RC4558P	AN4558
	RC4559N	AN5556
	SG4250	AN4250
	SN72558P	AN1458
	SN72741N	AN1741
	TA17590P	AN1324
	TA7504P	AN1741
	TA75339P	AN1339
	TA7538P	AN1358
	TA7538P1	AN1358
	TA75458P	AN1458
	TA7559P	AN6556
	1458N	AN1458
	2901N	*AN1339
	2904N	*AN1358
	324N	AN1324
	3302P	*AN1339
	339N	AN1339
	358N	AN1358
	393N	AN1393
	4136N	AN4136
	4558N	AN4558
	4559N	AN6556
	741N	AN1741

*Panasonic Functional Equivalent

Quick Selection Guide BY FUNCTION

Operational Amplifiers

				Package	Supply Voltage (V)		Power Consumption (mw)	Input Offset Voltage MAX (mV)	Input Offset Current MAX (nA)	Input Bias Current MAX (nA)	Output Voltage MIN (V)	Slew Rate TYP (V/μs)	Equiv. Vn (Input) TYP (μVrms)
Dual Power Supply	Low Noise Types	Dual	AN6550	9 − SIP	±2 to ±12	4 to 24	15	6	200	500	±1	0.8	2.5
			AN6551		±4 to ±15	8 to 30	170	6	200	500	±10	1.0	2.5
			AN6555		±4 to ±15	8 to 30	170	6	200	500	±10	2.0	1.5
			AN6557	9-SIP(LP)	±4 to ±15	8 to 30	240	3	200	—	±10	6.0	0.9
			AN4558 (AN6552)	8 − DIP	±4 to ±15	8 to 30	170	6	200	500	±10	1.0	2.5
			AN6553		±4 to ±15	8 to 30	170	6	200	500	±10	2.0	2.5
			AN6556		±4 to ±15	8 to 30	170	6	200	500	±10	2.0	1.5
			AN6558		±4 to ±15	8 to 30	240	3	200	—	±10	6.0	0.9
			AN4558S	SO − 8D	±4 to ±15	8 to 30	170	6	200	500	±10	1.0	2.5
			AN6556S		±4 to ±15	8 to 30	170	6	200	500	±10	2.0	.5
		Quad	AN4136 (AN6554)	14 − DIP	±2 to ±15	4 to 30	240	5	50	300	±10	1.6	2.5
			AN4136S	SO − 14D	±2 to ±15	4 to 30	240	5	50	300	±10	1.6	2.5
	General Purpose	Single	AN6573	7 − SIP	±2 to ±15	4 to 30	85	4	100	250	±10	0.7	4.0
			AN6593	9-SIP(LP)	±1 to ±18	2 to 36	3	6	20	75	±12	—	—
			AN1741 (AN6570)	8 − DIP	±2 to ±15	4 to 30	85	4	100	250	±10	0.7	4.0
			AN4250		±1 to ±18	2 to 36	3	6	20	75	±12	—	—
			AN1741S	SO − 8D	±2 to ±15	4 to 30	85	4	100	250	±10	0.7	4.0
			AN4250S	SO − 8D	±1 to ±18	2 to 36	3	6	20	75	±12	—	—
		Dual	AN6571	9-SIP(LP)	±2 to ±15	4 to 30	170	4	100	250	±10	0.7	4.0
			AN1458 (AN6572)	8 − DIP	±2 to ±15	4 to 30	170	4	100	250	±10	0.7	4.0
			AN1458S	SO − 8D	±2 to ±15	4 to 30	170	4	100	250	±10	0.7	4.0
Single Power Supply	General Purpose	Dual	AN6561	9 − SIP	±1.5 to ±15	3 to 30	6	7	50	250	Vcc − 1.5	0.3	6.0
			AN1358 (AN6562)	8 − DIP	±1.5 to ± 15	3 to 30	6	7	50	250	Vcc − 1.5	0.3	6.0
			AN1358S	SO − 8D	±1.5 to ±15	3 to 30	6	7	50	250	Vcc − 1.5	0.3	6.0
		Quad	AN1324 (AN6564)	14 − DIP	±1.5 to ±15	3 to 30	10	7	50	250	Vcc − 1.5	0.3	6.0
			AN1324NS	SO − 14D	±1.5 to ±15	3 to 30	10	7	50	250	Vcc − 1.5	0.3	6.0

Comparators

		Package	Supply Voltage (V)		Supply Current MAX (mA)	Input Offset Voltage MAX (mV)	Input Offset Current MAX (nA)	Input Bias Current MAX (nA)	Output Current MIN (mA)	Response Time TYP (ms)
Dual	AN6913	9 – SIP	±1 to ±18	2 to 36	1.5	5	50	250	10	1.3
	AN6915		±1 to ±18	2 to 36	5.3	5	50	200	70	2.0
	AN1393 (AN6914)	8 – DIP	±1 to ±18	2 to 36	1.5	5	50	250	10	1.3
	AN6916		±1 to ±18	2 to 36	5.3	5	50	200	70	2.0
	AN1393S	SO – 8D	±1 to ±18	2 to 36	1.5	5	50	250	10	1.3
	AN6916S		±1 to ±18	2 to 36	5.8	5	50	200	70	2.0
Quad-ruple	AN1339	14 – DIP	±1 to ±18	2 to 36	1.5	5	50	250	6	1.3
	(AN6912)		±1 to ±18	2 to 36	1.5	5	50	250	6	1.3
	AN6918		±1 to ±18	2 to 36	10.0	5	50	200	70	2
	AN1339S	SO – 14D	±1 to ±18	2 to 36	1.5	5	50	250	6	1.3

Voltage Regulators

Positive Output 3 Terminals (AN7800/AN78M00/AN78L00 Series)

I_0	Output Voltage (V)											
	4	5	6	7	8	9	10	12	15	18	20	24
1A	—	AN7805	AN7806	AN7807	AN7808	AN7809	AN7810	AN7812	AN7815	AN7818	AN7820	AN7824
0.5A	—	AN78M05	AN78M06	AN78M07	AN78M08	AN78M09	AN78M10	AN78M12	AN78M15	AN78M18	AN78M20	AN78M24
0.1A	AN78L04	AN78L05	AN78L06	AN78L07	AN78L08	AN78L09	AN78L10	AN78L12	AN78L15	AN78L18	AN78L20	AN78L24

ʾackage: AN7800/AN78M00 Series = TO-220, AN78L00 Series = TO-92

\egative Output 3 Terminals (AN7900 Series)

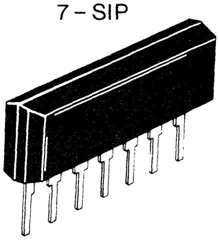
I_0	Output Voltage (V)										
	–5	–6	–7	–8	–9	–10	–12	–15	–18	–20	–24
1A	AN7905	AN7906	AN7907	AN7908	AN7909	AN7910	AN7912	AN7915	AN7918	AN7920	AN7924

ackage: TO-220

Quick Selection Guide BY PACKAGE

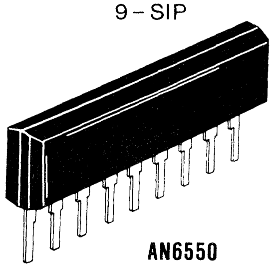
Operational Amplifiers

7-SIP



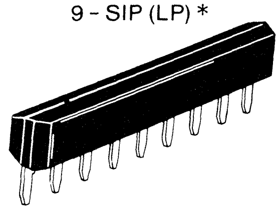
AN6573

9-SIP



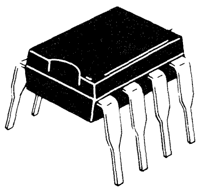
AN6550
AN6551
AN6555
AN6561

9-SIP (LP)*



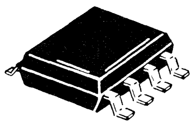
AN6557
AN6571
AN6593

8-DIP



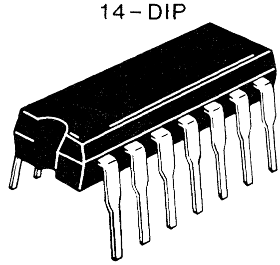
AN4558 (AN6552)
AN6553, AN6556
AN6558, AN4250
AN1358 (AN6562)
AN1741 (AN6570)
AN1458 (AN6572)

SO-8D



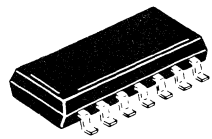
AN4558S
AN6556S
AN1358S
AN1741S
AN1458S
AN4250S

14-DIP



AN4136 (AN6554)
AN1324 (AN6564)

SO-14D

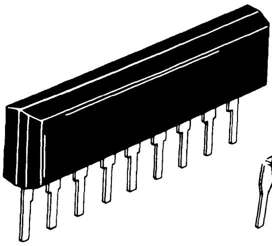


AN4136S
AN1324NS

*Low Profile

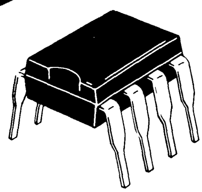
Comparators

9-SIP



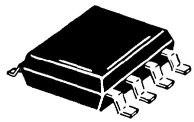
AN6913
AN6915

8-DIP



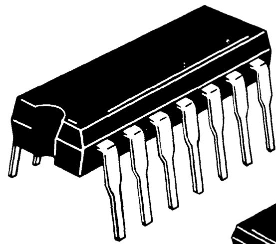
AN1393 (AN6914)
AN6916

SO-8D



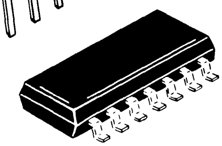
AN1393S
AN6916S

14-DIP



AN1339
(AN6912)
AN6918

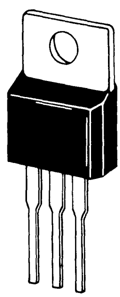
SO-14D



AN1339S

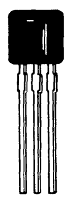
Voltage Regulators

TO-220



AN78XX
AN78MXX
AN79XX

TO-92

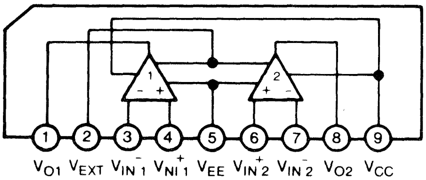


AN78LXX

Product Block Diagrams

Operational Amplifiers

AN6550



VEXT IS TERMINAL FOR BIAS

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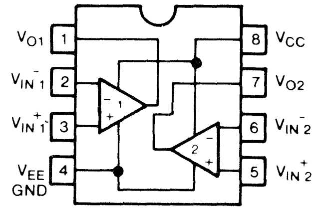
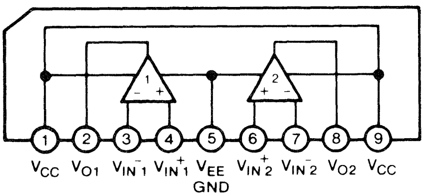
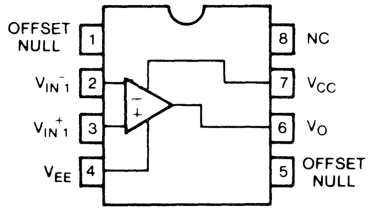


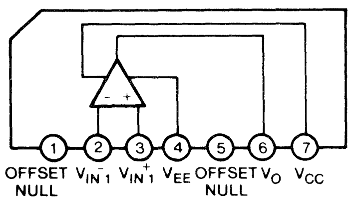
AN6551, AN6555, AN6561, AN6571, AN6557



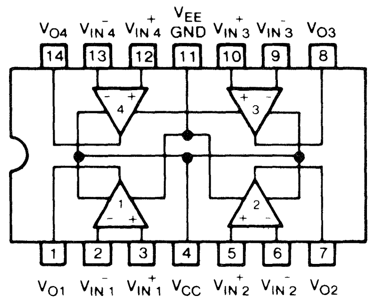
AN1741 (AN6570), AN1741S



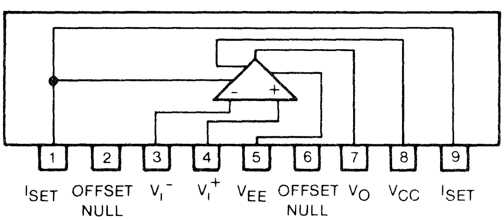
AN6573



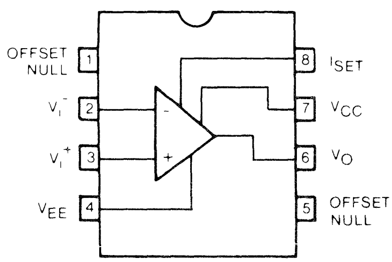
AN4136 (AN6554), AN4136S AN1324 (AN6564), AN1324NS,



AN6593

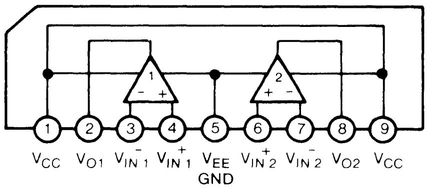


AN4250, AN4250S

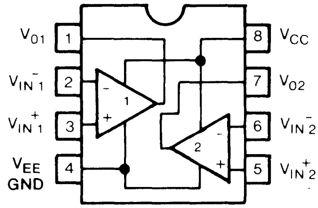


Comparators

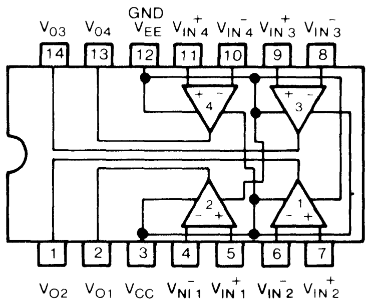
AN6913, AN6915



AN1393 (AN6914), AN1393S, AN6916, AN6916S

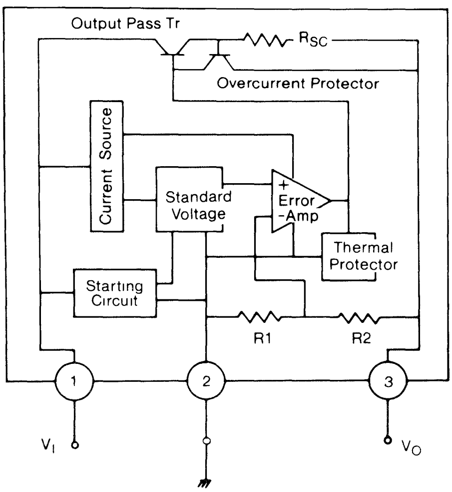


AN6912, AN6912S, AN1339S, AN6918

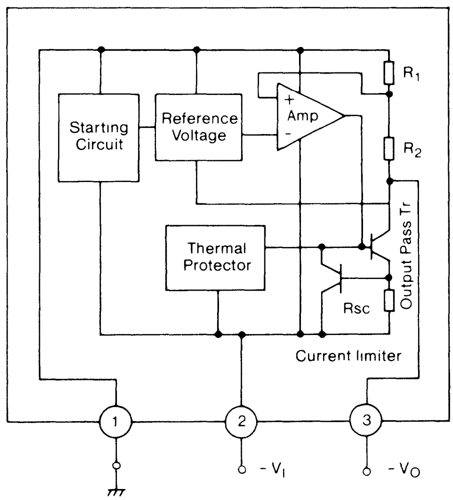


Voltage Regulators

AN7800, AN78M00, AN78L00 Series



AN7900 Series



General Information

Panasonic Panaflat™ Package

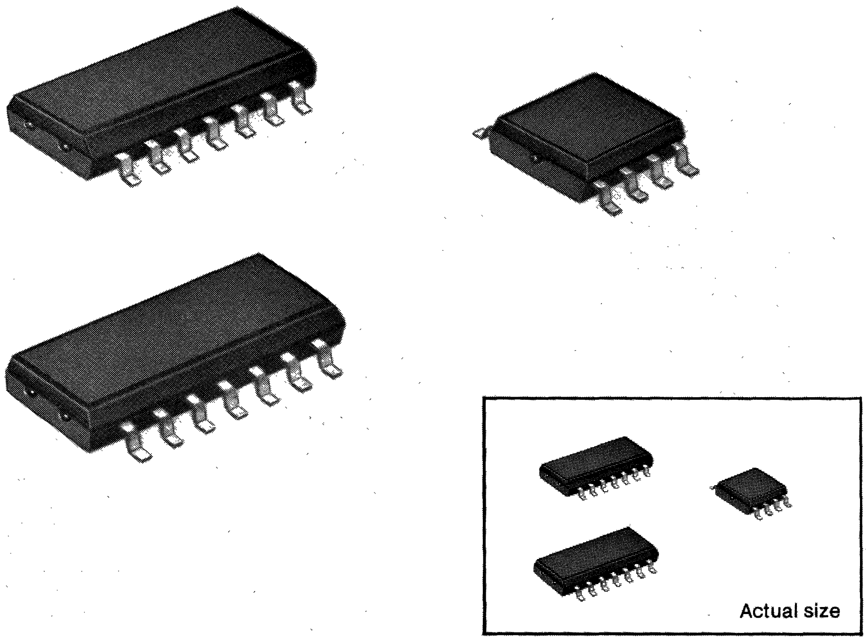


Fig. 1 External view of Panaflat package

In addition to the space-saving single-in-line package, Panasonic uses both the standard DIL plastic package and the compact Panaflat package and distinguishes between the two as follows:
(1) Standard DIL package products: AN1741
(2) Panaflat package products: AN1741S
"S" indicates Panaflat package.

The Panasonic Panaflat package is a new ultra-compact package for ICs and LSI developed for devices requiring hybrid ICs or that have to be ultra-thin. Recently, the advancement of electronics in all fields and the miniaturization and reduction in weight of electronic devices for both consumer and industrial use has drawn attention to the miniaturization of electronic parts beginning with transistors and ICs due to the demands of high-density mounting. Panaflat package ICs are a family of ultra-compact ICs which satisfy those demands because thay are ideal for mounting on a circuit board or assembly into hybrid ICs.

Fig. 1 is an external view of some Panaflat packages. Recent tendencies have been to assemble monolithic IC chips into hybrid ICs; however the assembly of plain chips is difficult when various factors such as handling, mass production, their electrical performance, and gua antee of quality are considered.
Panaflat package ICs compensate for these drawbacks.

1. Features of Panaflat package ICs

Panaflat package ICs have the following advantages when compared with conventional IC chips used in hybrid ICs and beam leads.

- High mounting density making possible the extensive miniaturization and increased density of hybrid ICs and circuit boards
- Easier to handle than IC chips and soldering is done by reflow
- Sufficient electrical characteristics can be guaranteed
- Encased in a special magazine for automatic insertion

2. Production of Panaflat package ICs

Production of Panaflat ICs is based on the technology of conventional plastic molded ICs and the mini-type molded transistors and incorporates a completely automatic sealing system developed by Panasonic and an automated production line which makes use of precise processing technologies.

3. Electrical characteristics

The absolute maximum ratings and electrical characteristics of Panaflat package ICs are basically the same as that of conventional plastic DIL package products.

By mounting a Panaflat IC on the circuit board of a hybrid IC and then coating it further with resin, the thermal resistance is improved over that of a single unit because of the increased conduction of heat from the single unit from the leads and resin surface.

Table 1 shows a comparison of the thermal resistance of different types of mountings. For example, by mounting on a ceramic circuit board and coating with resin, an allowance equivalent to or better than that of conventional 14-pin plastic DIL packages (DIL-14) may be achieved.

Please evaluate the actual mounting conditions concerning heat dissipation during actual use.

4. Reliability

To insure the reliability of Panaflat package ICs, testing is performed periodically according to the evaluation method in Table 2, "Reliability tests", as is done with conventional plastic packages. The level of reliability is the same as that of conventional plastic package products.

Table 1

Comparison of the thermal resistance for the mounting of Panaflat packages (SO-14D)

Values represent the improvement in thermal resistance using the thermal resistance of a single IC placed at 1 as a reference.

	Epoxy circuit board (55 x 10 x 0.7mm)	General use ceramic circuit board (37 x 12 x 0.6mm)
Mounted on the circuit board	0.68 (1.45)	0.57 (1.75)
Coated with resin after mounting on the circuit board	0.52 (1.81)	0.40 (2.47)

(Values in parenthesis indicate ratio of allowable loss P_D.)

Table 2. Reliability tests

Test	Condition
External dimensions	According to individual package
Vibration test	100 to 2000Hz 20G, 4 min/1 time (X, Y, Z each 4 times)
Drop test	Maple board, 1 m, 3 times
Terminal pull	0.5kg in direction of lead axis for 10 sec
Terminal bending	0.25kg to 45° back and forth 2 times
Saltwater spray	35°C at 5% for 24 hours
Temperature cycle (gaseous phase)	Tstg. max ↔ Tstg. min, 10 cycles (30 min) (30min)
Thermal shock (liquid phase)	100°C ↔ 0°C, 10 cycles (5min) (5min)
Boiling test	Pure water at 100°C for 100 hours
Pressure cooker	Steam saturation at 2atm for 60 hours
Solderability	230°C, 1 time for 5 sec with flux
Solder-heat resistance	260°C, 5 sec
High-temperature storage	Ta = Tstg. max 1000 hours
Low-temperature storage	Ta = Tstg. min 1000 hours
High-temperature, high-humidity storage	Ta = 85°C, RH = 85% for 500 hours
Operating life	Ta = Topr max 1000 hours, maximum loss and T_j (max)
High-temperature, high-humidity bias	Ta = 85°C and RH = 85% for 500 hours, steady bias.

5. Mounting precautions

Compared with conventional packages, the structure of the Panaflat package is much smaller and thinner, and so particular attention should be given to the mounting procedures. These products are susceptible to the thermal and mechanical stress applied during mounting. Attention must be given to the following points.

(1) Soldering

Because of their small size, SO ICs are susceptible to the influence of heat applied from outside and respond rapidly as shown in Fig. 2. For this reason, the influence of thermal stress should be minimized. Thermal stress causes expansion and contraction of the resin which causes stress inside the package. Therefore, when exposing to high temperatures of soldering, keep the operation as short as possible.

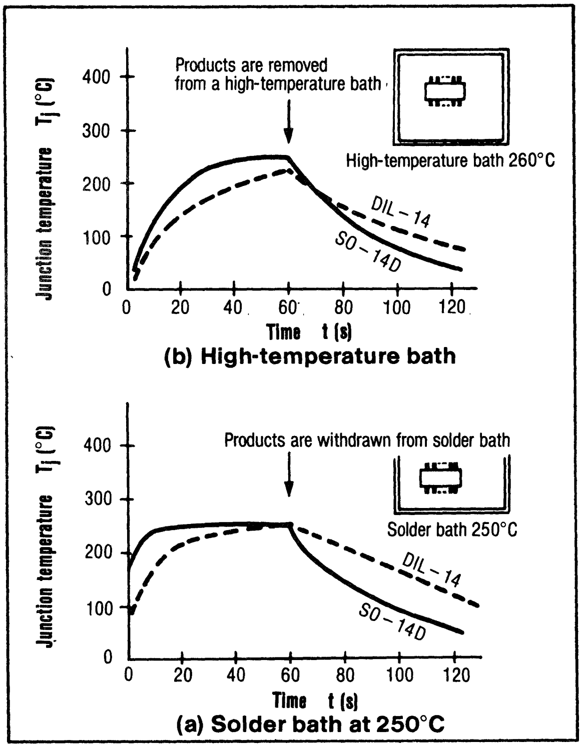


Fig. 2 Comparison of junction temperatures according to the external conditions of the Panaflat package (SO-14D) and the conventional package (DIL-14)

Requirements for soldering

(1) Use a reflow method such as that in Fig. 3 to keep the temperature as low (below 260°C), and the time as short (less than 10 seconds) as possible.
Please use a soldering paste conforming to these requirements.

(2) For fluxing after soldering, momentarily wash with Tri-Ethane or a similar solution.

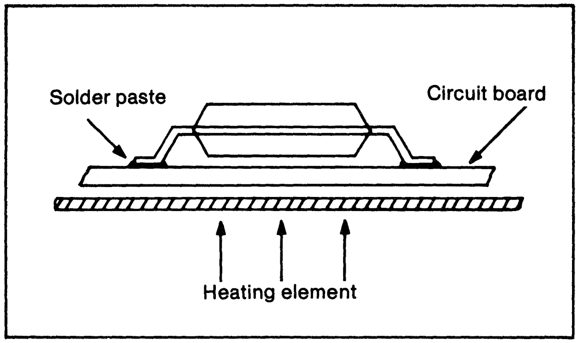


Fig. 3 Diagram showing reflow-system soldering

(2) Mechanical stress

- Because of the small, thin structure of the SO IC, the strength of the lead wires, in comparison with conventional plastic packages is as shown in Fig. 4. Thus, particular attention must be paid to their handling.
- Furthermore, because of their thin shape, they are susceptible to stress applied during mounting or through the resin surface after mounting, and this may change their characteristics. Be careful that no stress is applied to the resin surface.

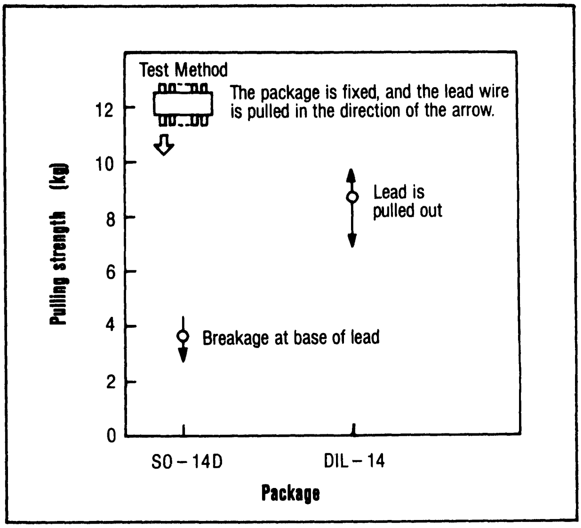


Fig. 4 Results of lead terminal pulling test

(3) Heat discharge after mounting

The heat discharge of SO ICs is greatly influenced by mounting to the circuit board and coating with resin, and so please determine the heat discharge with the IC in its mounting condition. The following is a simple estimation method for the chip temperature in the mounted condition.

Estimation of the chip temperature by measuring the package surface temperature.

By putting the Panaflat package IC in an operating condition, the chip temperature (T_j) rises. After sufficient time (approx. 10 min) the package surface temperature (T_S) becomes saturated and the T_S is measured and used to estimate T_j.

$T_S < T_j(max) - (Rthj\text{-}c \times Ptot) - (Topr - Ta)$

T_S: Package surface temperature
Ta: Measured ambient temperature
T_j(max): Storage temperature noted in the product's ratings
Topr: Operating temperature noted in the products's rating
Rthj-c: Thermal resistance between the chip and package = 40°C/W
Ptot: Power consumption of IC during operation (under most unfavorable conditions)

When the estimated value of T_S is smaller than the calculated value on the right, even at Topr (max) T_j will be below T_j(max).

(4) Moisture considerations

Because SO ICs are ultra-compact and the resin thickness is very thin, the leakage path is short, and so it is necessary to pay particular attention to moisture. Generally accepted air-tight sealing or damp-proof resin coating may be used as measures to prevent moisture from entering, but when coating with a resin, particular care should be given to selecting a resin that will satisfy the requirements of reliability.

Reliability Information

Panasonic is dedicated to maintain and improve high standards of product quality. Table 1, "Quality Control and Guarantee System", shows the many steps taken to control our IC product quality. Ideally, quality could be built in and forgotten. However well this may be done, the quality levels must be constantly monitored as shown at each step of Table 1. In addition, the tests marked "*sample", are accelerated life tests designed to yield potential problems prior to product release, ("Real-Time" life indicators), so that life defective IC's are not shipped and problems can be promptly addressed and corrected.

At the "Reliability Tests" stage of Table 1, we use two types of tests used to check both new and existing products to confirm their reliability, consistent high quality, and long life under severe environmental conditions: life tests and environmental tests. In order to design tests with conditions which can be repeated, Panasonic uses MIL and other standards such as EIAJ.
For the conditions of these reliability tests, refer to Table 2, "Reliability test parameters and standards".

For these reliability tests, products are separated intro matrices, classified as diffusion process (wafer family) and assembly process (package). These are then divided into sub-groups and representative products of each sub-group are then selected to undergo tests. The testing frequency varies from one to six months, depending on the type and the history of that product.

Even though Panasonic linear products are in plastic packages, these products are capable of being used in severe industrial environments through the development of high-purity resin, the introduction of a new sealing method and the development of a new technology for chip protective films. We at Panasonic are not going to stop at the present high level of reliability our products have achieved, and we are constantly working to attain even greater improvement.
To accompany the high reliability of our products we have made advancements in the development of a system of tests to confirm reliability in as short a time as possible and to quickly relay the information to the factory. This system includes the accumulation of test data, analysis of statistical and physical information on the quality of products on the market, and feedback of all this to the pertinent sections. This is done to assure our users of consistently improved quality levels of Panasonic products.

Table 1. Quality Control and Guarantee System

Stage	Frequency of Tests	Quality Tests
Product Plan ⇩		
Product Design ⇩		1. Design and layout circuit 2. Develop as needed: New process, package, automated machinery.
Quality Approval of Design ⇩		
Production		
Wafer Fabrication	100% and *Sample	● Sheet Resistance ● Diffusion Profile ● Oxide quality ● Metalization ● Mask Alignment
Wafer Probe	100%	● D.C. tests ● Visual Inspection
I.C. Assembly: Die Bond, Packaging, Lead Forming, Branding	100% and *Sample	● Bond Strength ● Pre-Seal Visual ● Solderability ● Lead Pull ● Branding Integrity
Quality Screen	*Sample	● Thermal Stress tests
Final Test	100%	● All D.C. and Parametric tests
Reliability Tests	*Sample	● Table 2 tests ● All New Parts as well as periodic tests as indicated in table
Warehouse, Package To Ship	*Sample	● Visual inspection ● Special customer tests ● D.C. and parametric tests ● Periodic inventory tests to above items
Customer Use	Customer tests	● Field data ● Failure analysis of returns → Product improvement

*Accelerated Life Test to show results prior to product shipment ("Real-Time" Life indicator)

Reliability Information

Table 2. Reliability Evaluation Test Parameters and Passing Standards

Group	Parameter	Test Conditions	Judging standards LPTD(r/N)	Testing Standards	
				New products test	Periodic reliability test
1	Initial characteristics	All parameters of inspection ratings specified for each product type.	5%(0/45)	●	
	Temperature characteristics	Characteristics test of product's rated operating ambient temperature range.	50% (0/5)	●	
	Voltage characteristics	Characteristics test of product's rated power supply voltage range.	50% (0/5)	●	
	Heat resistance		50% (0/5)	●	
2	Soldering	Immersed for 5 ± 0.5 seconds in 230 ± 5°C solder bath up to 1.5mm from the main part of the unit. Flux used is 35% pine oil solution.	15% (0/15)	●	●
	External dimensions	According to the product's rated external dimensions.	15%(0/15)	●	
3	Thermal shock	10 cycles T(min.) (-65°C, 1 min or more) Both testing baths are liquid baths. T(max.) (150°C, 1 min or more)			
	Thermal fatigue	Conditions at T_j(max) or $P_D$max determined according to configuration type.	15% (0/15)	●	
	Soldering thermal stability	Immersed for 10 ± 1 seconds in 300 $^{+0}_{-10}$ °C solder bath up to 1 ± 0.1mm from the main part of the unit.	15% (0/15)	●	
4	Drop Test	Dropped 3 times from a height of 1 m onto a maple board.	50%(0/5)	●	
	Lead Bend	Bent 90°C with an applied force of 230g and then returned.	50% (0/5)	●	
	Lead Pull	2kg of force applied for 30 ± 1 seconds in lead axial direction.	50% (0/5)	●	

Note: The testing conditions listed above are "official" values; the actual tests are carried out under even stricter conditions according to our own internal standards.

Table 2. Reliability Evaluation Test Parameters (continued)

Group	Parameter	Test Conditions	Judging standards LPTD(r/N)	Testing Standards	
				New products test	Periodic reliability test
5	Salt water spraying	Sprayed continuously for 24 hours at concentration of 5%, temperature 35°C.	50% (0/5)	●	●
6	High temperature and humidity	Kept for 1000 hours at Ta = 85°C, RH ≤ 85°C. RH ≥ 85%.	15% (0/15)	●	
	T.H.B.	Kept for 1000 hours at Ta = 85°C, Testing circuits normal actual use, ON/OFF = 1h/3h.	15%(0/15)	●	●
	Pressure cooker	Kept for 60 hours at 2 atmospheres of pressure and then allowed to cool naturally for 16 hours.	15% (0/15)	●	●
	Boiling	Kept at boiling for 50 hours.	15% (0/15)	●	
	Hermeticity	He leakage < 1 x 10^{-7}cc/s Used only on ceramic or metal packages.	15% (0/15)	●	
7	Low Temperature	Kept at Ta = –55°C for 1000 hours.	15% (0/15)	●	
	High Temperature	Kept at Ta = 150°C for 1000 hours.	15% (0/15)	●	
8	Operating life	1000 hours at V_{CC} (max) of T_j (max) conditions at maximum ambient temperature; ON/OFF = 2.5h/0.5h.	15% (0/15)	●	●
9	Fireproofing	Because plastic material used passed UL94 and V-0, test on completed products omitted.	50% (0/5)	●	

Note: The testing conditions listed above are "official" values; the actual tests are carried out under even stricter conditions according to our own internal standards.

Glossary of Terms and Symbols

Symbol	Description of Terms	Typical Units
A_{OL}	Output Voltage Gain, Open Loop	dB
BW	Bandwidth	Hz
C	Capacitance, Capacitor	μf
C_i	Input Capacitance	μf
C_o	Output Capacitance	μf
CMRR	Common-mode Rejection Ratio	dB
CS	Channel Separation	dB
f	Frequency	Hz
f_I	Input Frequency	Hz
I	Current (D.C.)	mA, μA, nA
I_B	Bias Current	mA, μA, nA
I_{CC}	Positive Supply Current	mA
I_{EE}	Negative Supply Current	mA
I_I	Input Current (D.C.)	μA
I_{IH}	Input Current, Input High	mA
I_{IL}	Input Current, Input Low	mA
I_{IO}	Input Offset Current	μA
I_L	Load Current	mA
I_{LEAK}	Output Leakage Current	mA
I_O	Output Current	mA
I_{OH}	Output Current, Output High	mA
I_{OL}	Output Current, Output Low	mA
I_{OS}	Output Current, Output Shorted	mA
I_Q	Quiescent Current	μA
NF	Noise Figure	$\mu V/\sqrt{Hz}$
P_C	Power Consumption	W, mW
P_D	Power Dissipation	W, mW
P_{TOT}	Total Power	W, mW
ΔI	Current Change	mA, μA, nA
PSRR	Power Supply Rejection Ratio	dB
R	Resistance, Resistor	Ohms, Ω
R_i	Input Resistance	Ohms, Ω
R_L	Load Resistance	Ohms, Ω

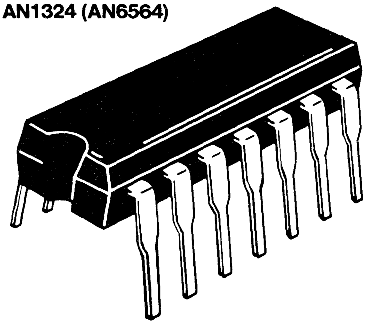
Symbol	Description of Terms	Typical Units
R_O	Output Resistance	Ohms, Ω
RR	Rejection Ratio	dB
SR	Slew Rate	V/μS
T	Temperature	°C
T_a, T_A	Ambient Temperature	°C
T_j	Junction Temperature	°C
ΔT	Temperature Change	°C
t	Time (signal)	Sec, μ Sec, n Sec
t_f	Fall Time	μSec, n Sec
t_r	Rise Time	μ Sec, n Sec
t_R	Response Time	μSec, n Sec
t_s	Set-up Time	μSec, n Sec
t_{stg}	Storage Time	μSec, n Sec
V	Voltage	Volts, μV, nV
V_{CC}	Positive Supply Voltage	V
V_{CM}	Common-mode Voltage	V
V_{EE}	Negative Supply Voltage	V
V_{EXT}	External Bias Voltage	V
V_I	Input Voltage, (D.C.)	V
V_i	Input Voltage, (A.C.)	V
V_{ICM}	Input Common-mode Voltage	V
V_{ID}	Differential Input Voltage	V
V_{IH}	Input Voltage, Input High	V
V_{IL}	Input Voltage, Input Low	V
V_{IO}	Input Offset Voltage	mV
V_n	Noise Voltage (see also N.F.)	$\mu V/\sqrt{Hz}$
V_O	Output Voltage	V
V_{OH}	Output Voltage, Output High	V
V_{OL}	Output Voltage, Output Low	V
V_{OM}	Maximum Output Voltage	V
V_{OR}	Output Voltage Range	V
V_Z	Zener Voltage	V
ΔV	Change in Voltage	mV

AN1324/AN1324S(AN6564) OPERATIONAL AMPLIFIER

General Description

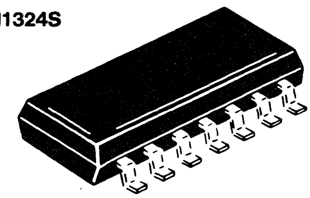
The AN1324 consists of four independent, high gain, internally frequency compensated operational amplifiers designed to operate from a single or dual power supply over a wide range of voltages.It is available in 14 - pin small outline (S.O.) package for high-density design and replaces any standard "324" circuit.

AN1324 (AN6564)



14 - DIP PACKAGE

AN1324S



SO - 14D PACKAGE

Features

- Internally frequency compensated
- Large output voltage swing: 0 to V+ - 1.5V
- Wide power supply range -
  Single supply: 3 to 30V
  Dual supplies: ± 1.5V to ± 15V

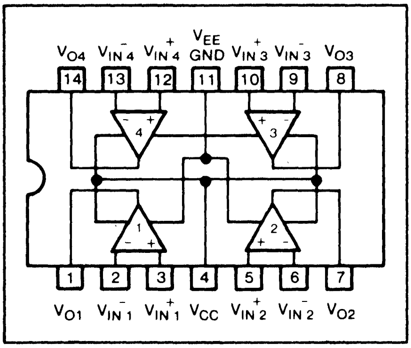
Absolute Maximum Ratings (T_a = 25°C)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	32 or ± 16	V
Power Dissipation	(14 DIP)	P_D	570	mW
	(14 SO)	P_D	370	mW
Input Differential Voltage		V_{ID}	32	V
Input Common -Mode Voltage		V_{ICM}	- 0.3 to 32	V
Operating Temperature		Topr	- 20 to + 75	°C
Storage Temperature		Tstg	- 55 to + 150	°C
Output Voltage		V_O	24	V

Electrical Characteristics (V_{CC} = 5V, T_a = 25°C)

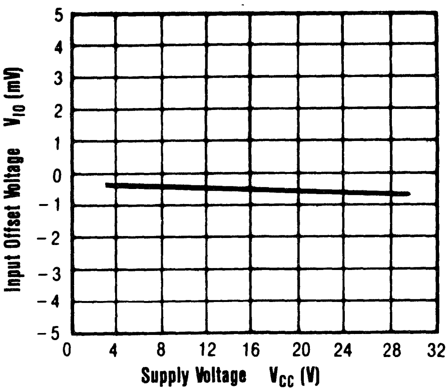
Item		Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage		V_{IO}	1	R_S = 50Ω		2	7	mV
Input Offset Current		I_{IO}	1				50	nA
Input Bias Current		I_B	1				500	nA
Voltage Gain		A_{OL}	1	R_L ≒ 2kΩ		100		dB
Output Current	(Sink)	$I_{O\,(SINK)}$	7	V_{IN} = 0V, V_{IN} = 1V	10	20		mA
	(Source)	$I_{O\,(SOURCE)}$	6	V_{IN} = 1V, V_{IN} = 0V	20	40		mA
Supply Current		I_{CC}	3	R_L + ∞		0.8	2	mA
Maximum Output Voltage		V_{OM}	4	R_L = 2kΩ	V_{CC} - 1.5			V
Common-Mode Rejection Ratio		CMRR	1			85		dB
Supply Voltage Rejection Ratio		PSRR	1			100		dB
Common-Mode Input Voltage		V_{ICM}	2		0		±15	V
Channel Separation		CS	5	f = 1kHz to 20kHz		120		dB

Connection Diagram

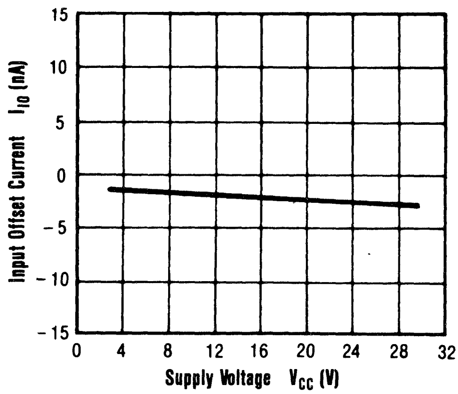


Typical Electrical Performance Curves

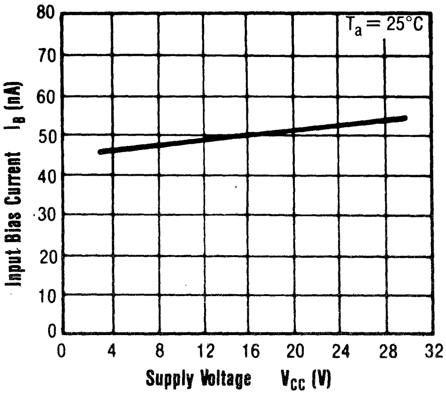
Input Offset Voltage vs Supply Voltage



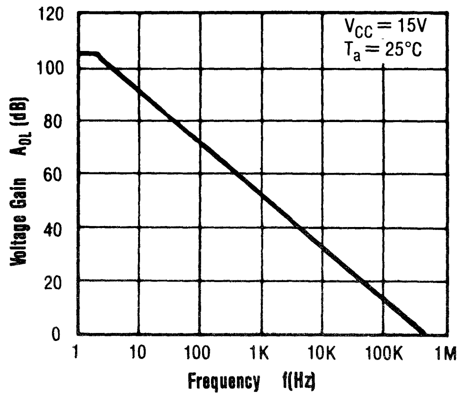
Input Offset Current vs Supply Voltage



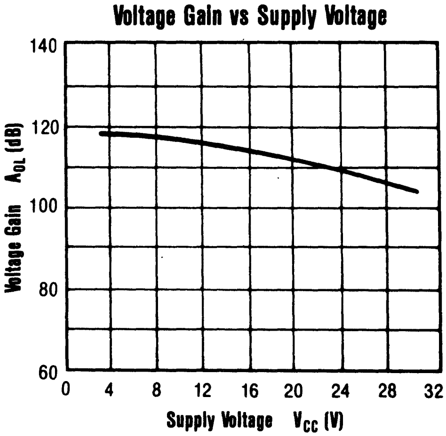
Input Bias Current vs Supply Voltage

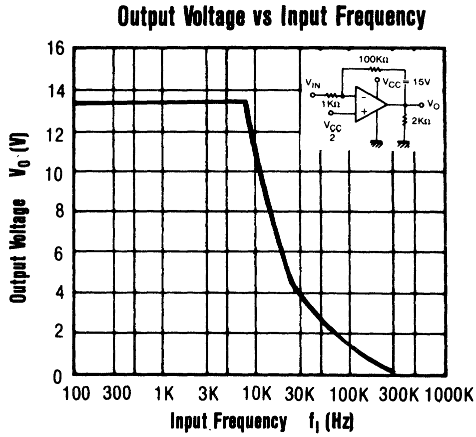


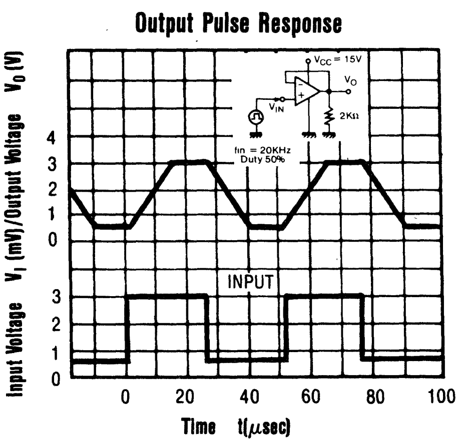
Voltage Gain vs Frequency

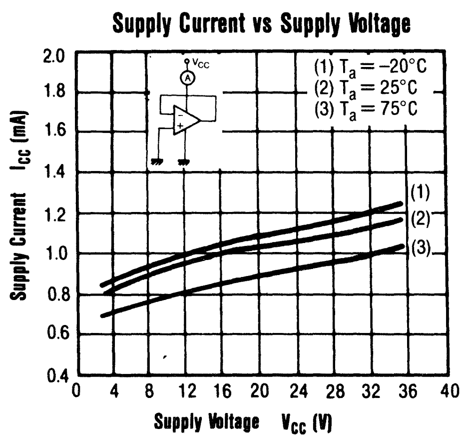


Typical Electrical Performance Curves (continued)



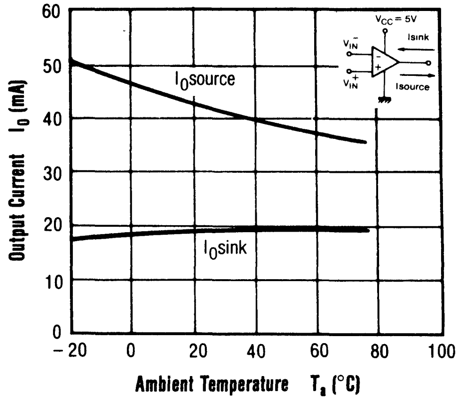




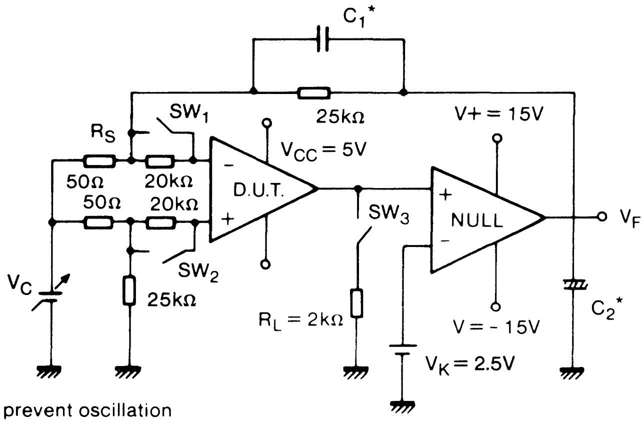


Typical Electrical Performance Curves (continued)

Output Current vs Ambient Temperature

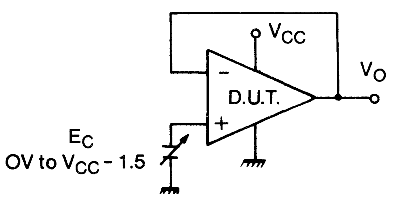


Test Circuit 1 (1/4 circuit)

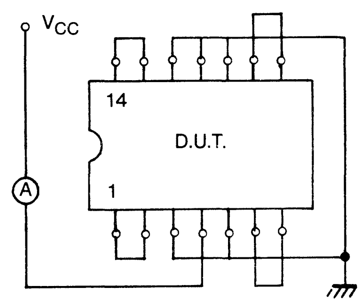


*C_1 and C_2 to prevent oscillation

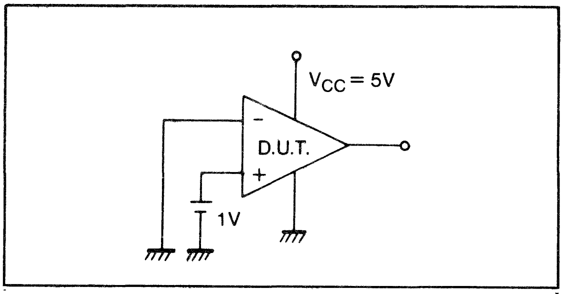
Test Circuit 2 (1/4 circuit)



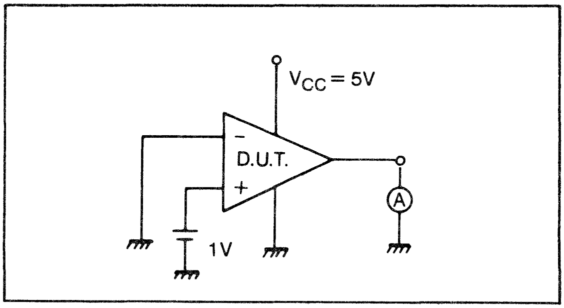
Test Circuit 3



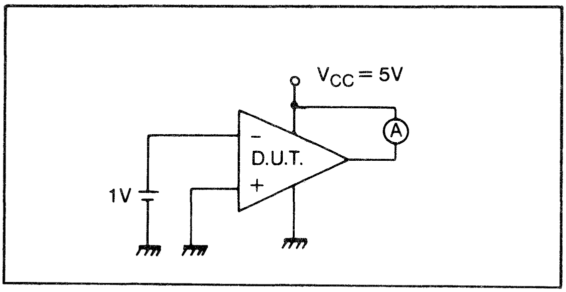
Test Circuit 4 (1/4 circuit)



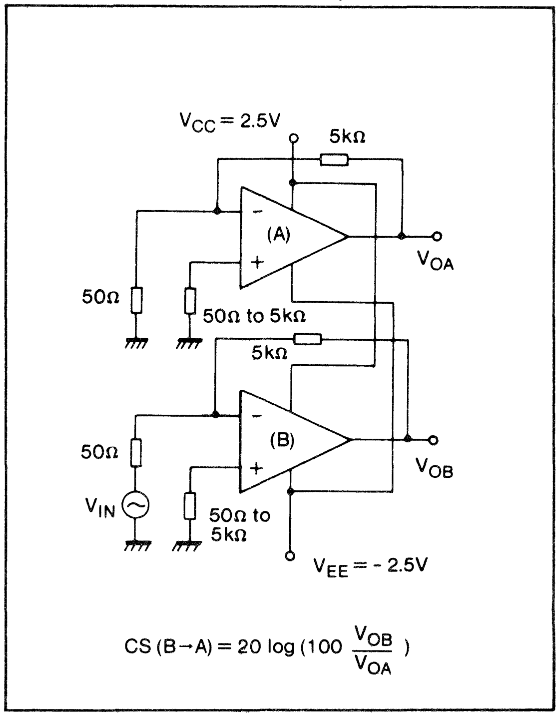
Test Circuit 6 (1/4 circuit)



Test Circuit 7 (1/4 circuit)



Test Circuit 5 (1/2 circuit)



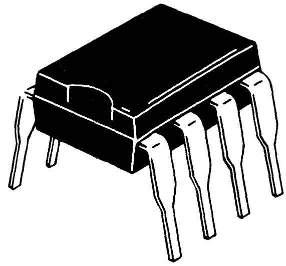
Item	Test Conditions For Circuit 1
Input Offset Voltage	Turn on SW1, SW2, and measure V_{F1} (E_C = 0), where $V_{IO} = V_{F1}/500$ (V)
Input Offset Current	Turn off SW1, SW2, and measure V_{F2} (E_C = 0), where $I_{IO} = \frac{\lvert V_{F2} - V_{F1} \rvert}{10^7}$ (A)
Input Bias Current	SW1 on, SW2 off, and measure V_{F3}, SW1, off SW2 on measure V_{F4}. $I_B = \frac{\lvert V_{F4} - V_{F3} \rvert}{2 \times 10^7}$ (A)
Voltage Gain	SW1, SW2 on, E_K = 1.4V, and measure V_{F5}. E_K = 3.4V, measure V_{F5} SW3 on $A_{OL} = 20 \log \left(\frac{1000}{V_{F1} - V_{F5}}\right)$
Common-Mode Rejection Ratio	SW1, SW2 on,and measure V_{F6} ($E_K = E_{C1}$), measure V_{F7} ($E_C = E_{C2}$) CMRR $= 20 \log \left(500 \times \left\lvert \frac{E_{C1} - E_{C2}}{V_{F6} - V_{F7}} \right\rvert\right)$
Supply Voltage (−) Rejection Ratio (+)	SW1, SW2 on, E_C = 0, and measure V_{F8} ($V_{CC} = V_{C1}$), measure V_{F9} ($V_{CC} = V_{C2}$), PSRR $= 20 \log \left(500 \times \left\lvert \frac{V_{C1} - V_{C2}}{V_{F8} - V_{F9}} \right\rvert\right)$

AN1358/AN1358S (AN6562) DUAL OPERATIONAL AMPLIFIER

General Description

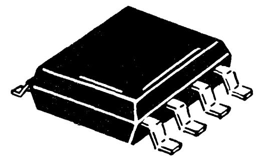
The AN1358 consists of two independent, high gain internally frequency compensated operational amplifiers which were designed to operate from a single power supply over a wide range of voltage

AN1358 (AN6562)



8-DIP PACKAGE

AN1358S



SO-8D PACKAGE

Features

- Internally frequency compensated for unity gain
- Large output voltage swing: OV to V_{CC} - 1.5V
- Wide power supply range:
  Single supply: 3 to 30V or
  Dual supplies: ± 1.5V to ± 15V

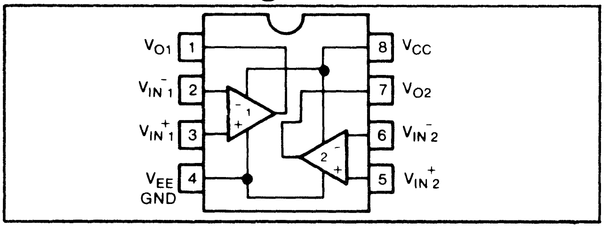
Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	32	V
Power Dissipation	P_D	350	mW
Input Differential Voltage	V_{ID}	32	V
Input Common-Mode Voltage	V_{ICM}	- 0.3 to 32	V
Operating Temperature	Topr	- 20 to 75	°C
Storage Temperature	Tstg	- 55 to ± 150	°C
Output Voltage	V_O	24	V

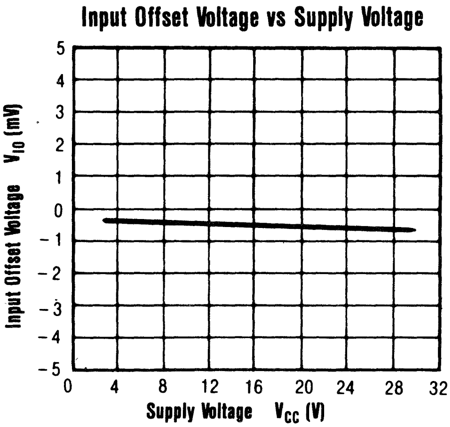
Electrical Characteristics (V_{CC} = 5V, T_a = 25°C)

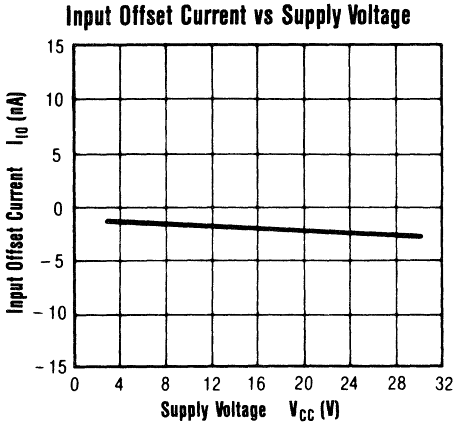
Item		Symbol	Test Circuit	Condition	Limit			Unit
					min.	typ.	max.	
Input Offset Voltage		V_{IO}	1	R_S = 50Ω		2	7	mV
Input Offset Current		I_{IO}	1				50	nA
Input Bias Current		I_B	1				250	nA
Voltage Gain		A_{OL}	1	R_L = 2kΩ	88	100		dB
Output Current	(Sink)	$I_{O\,(SINK)}$	7	V_{IN} = 0V, V_{IN} = 1V	10	20		mA
	(Source)	$I_{O\,(SOURCE)}$	6	V_{IN} = 1V, V_{IN} = 0V	20	40		mA
Maximum Output Voltage		V_{OM}	4	R_L = 2kΩ	V+ - 1.5			V
Common-Mode Rejection Ratio		CMRR	1		65	85		dB
Supply Voltage Rejection Ratio		PSRR	1		65	100		dB
Supply Current		I_{CC}	3	R_L + ∞		0.6	1.2	mA
Common-Mode Input Voltage		V_{ICM}	2				V+ - 15V	V
Channel Separation		CS	5	f = 1kHz to 20kHz		120		dB

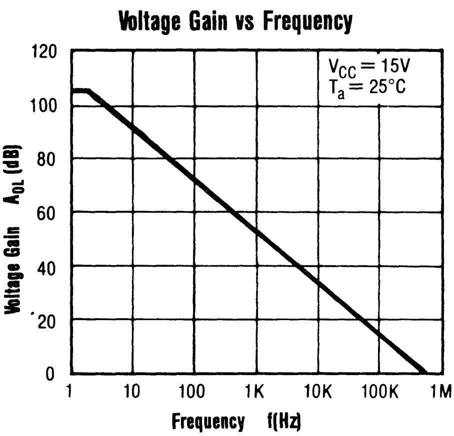
Connection Diagram

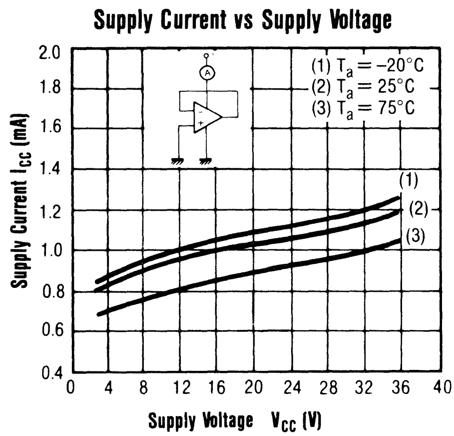


Typical Electrical Performance Curves

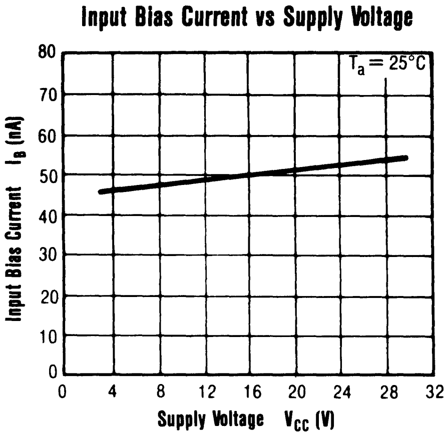


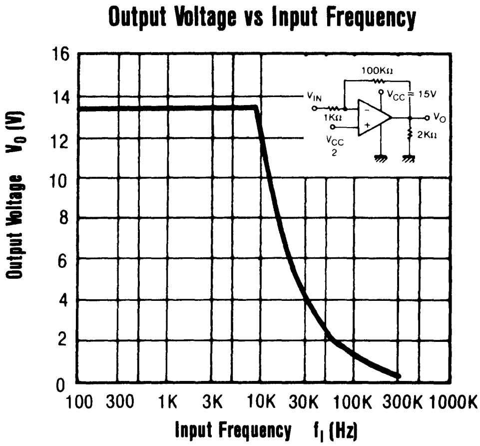


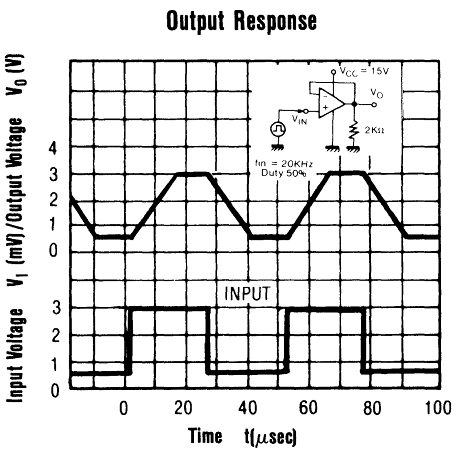


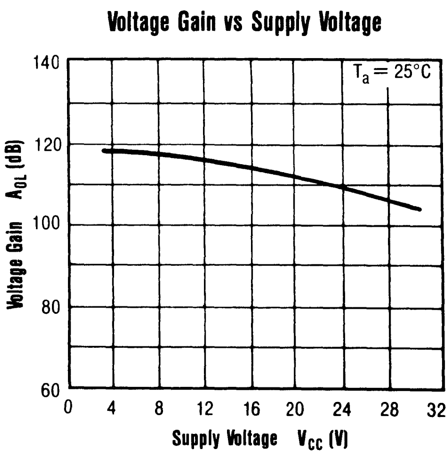


Typical Electrical Performance Curves (continued)

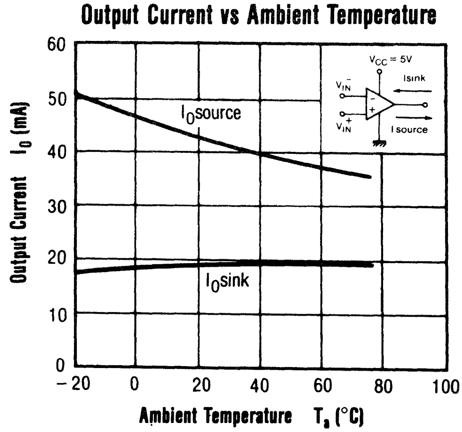




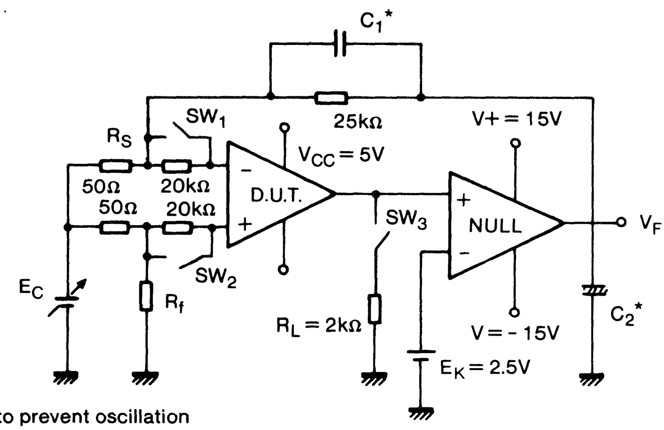




Typical Electrical Performance Curves (continued)

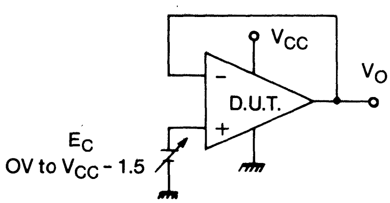


Test Circuit 1 (½ circuit)

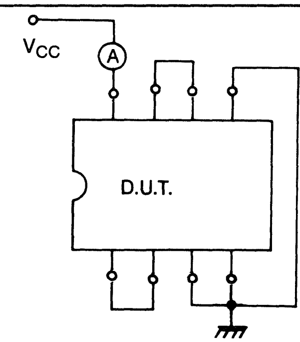


*C1 and C2 to prevent oscillation

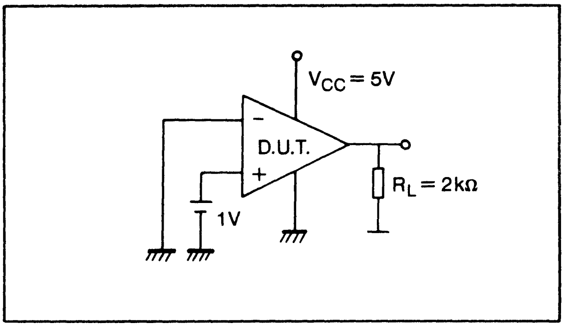
Test Circuit 2 (½ circuit)



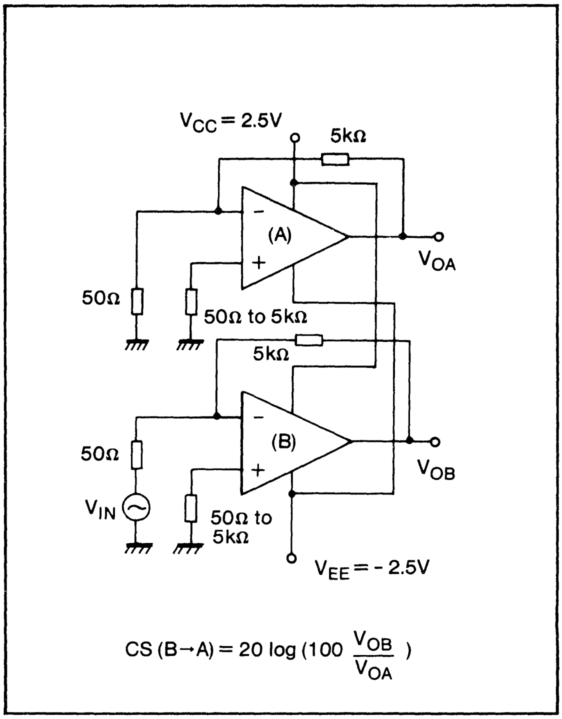
Test Circuit 3



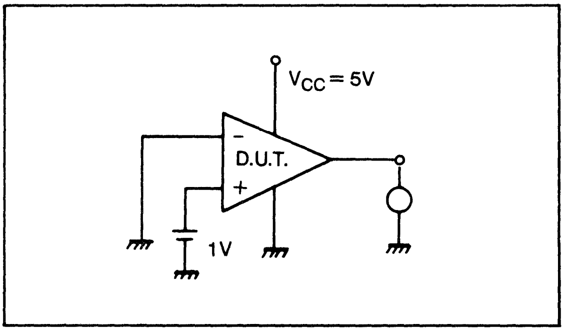
Test Circuit 4 (½ circuit)



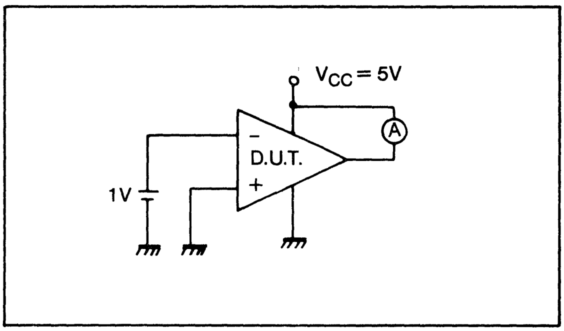
Test Circuit 5



Test Circuit 6 (½ circuit)



Test Circuit 7 (½ circuit)



Item	Test conditions for Circuit 1
Input Offset Voltage	Turn on SW1, SW2, and measure V_{F1} (E_C =0), where $V_{IO} = V_{F1}/500$ (V)
Input Offset Current	Turn off SW1, SW2, and measure V_{F2} (E_C = 0), where $I_{IO} = \frac{\lvert V_{F2} - V_{F1} \rvert}{10^7}$ (A)
Input Bias Current	SW1 on, SW2 off, and measure V_{F3}, SW1, off SW2 on measure V_{F4}. $I_B = \frac{\lvert V_{F4} - V_{F3} \rvert}{2 \times 10^7}$ (A)
Voltage Gain	SW1, SW2 on, E_K = 1.4V, and measure V_{F5}. E_K = 3.4V, measure V_{F5} SW3 on $A_{OL} = 20 \log \left(\frac{1000}{V_{F1} - V_{F5}}\right)$
Common-Mode Rejection Ratio	SW1, SW2 on,and measure V_{F6} ($E_K = E_{C1}$), measure V_{F7} ($E_C = E_{C2}$) $CMRR = 20 \log \left(500 \times \left\lvert \frac{E_{C1} - E_{C2}}{V_{F6} - V_{F7}} \right\rvert\right)$
Supply Voltage (–) Rejection Ratio (+)	SW1, SW2 on, E_C = 0, and measure V_{F8} ($V_{CC} = V_{C1}$), measure V_{F9} ($V_{CC} = V_{C2}$), $PSRR = 20 \log \left(500 \times \left\lvert \frac{V_{C1} - V_{C2}}{V_{F8} - V_{F9}} \right\rvert\right)$

AN1458/AN1458S (AN6572) DUAL OPERATIONAL AMPLIFIER

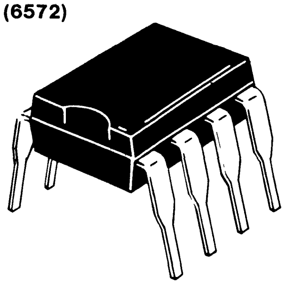
General Description

The AN1458 is an internally compensated dual operational amplifier. It is equivalent to most industry standard "1458" applications and has the added feature of "S.O." package availability.

Features

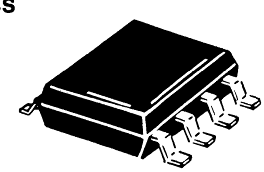
- No compensation required
- Short-circuit protection
- Low power consumption
- 8 - pin DIP and S.O. plastic packages

1458 (6572)



8 - DIP PACKAGE

1458S



SO - 8D PACKAGE

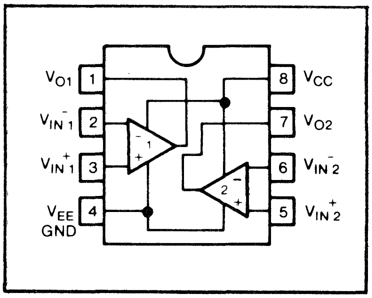
Absolute Maximum Ratings ($T_a = 25°C$)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	± 18	V
Power Dissipation	(8 DIP)	P_D	500	mW
	(8 SO)	P_D	360	mW
Input Differential Voltage		V_{ID}	± 30	V
Input Common –Mode Voltage		V_{ICM}	± 15	V
Operating Temperature		T_{opr}	– 20 to + 75	°C
Storage Temperature	(8 DIP)	T_{stg}	– 55 to + 150	°C
	(8 SO)	T_{stg}	– 55 to + 125	°C

Electrical Characteristics ($V_{CC} = -V_{EE} = 15V$, $T_a = 25°C$)

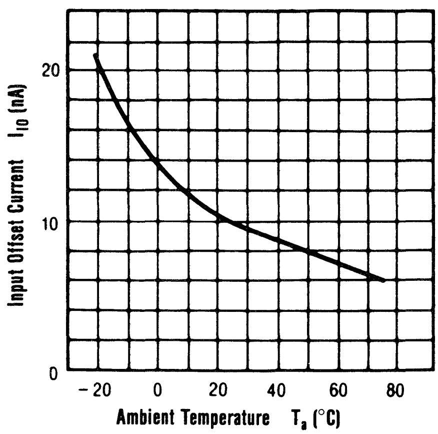
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		1	5	mV
Input Offset Current	I_{IO}	1			20	200	nA
Input Bias Current	I_B	1			80	500	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm10V$	86	106		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±13		V
Common-Mode Rejection Ratio	CMRR	1	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	PSRR	1	$R_S \leq 10k\Omega$		30	150	μV/V
Power Consumption	P_C	4			96	170	mW
Slew Rate	SR	5			0.8		V/μs
Supply Current	I_{CC}	4			3.2	5.6	mA
Output Short-Circuit Current	$I_{O(SHORT)}$	2			20		mA
Input Resistance	R_i			0.3	1		mΩ

Connection Diagram

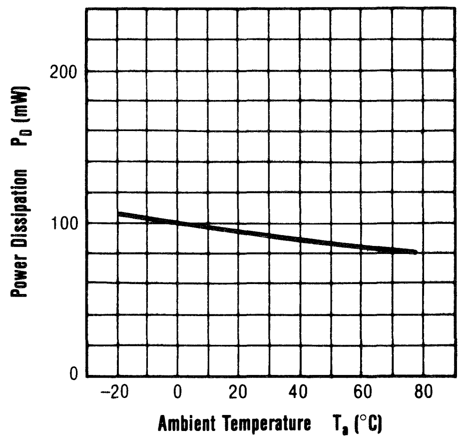


Typical Electrical Performance Curves

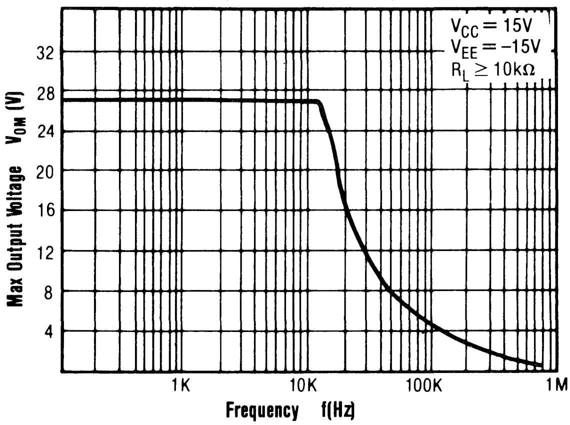
Input Offset Current vs Ambient Temperature



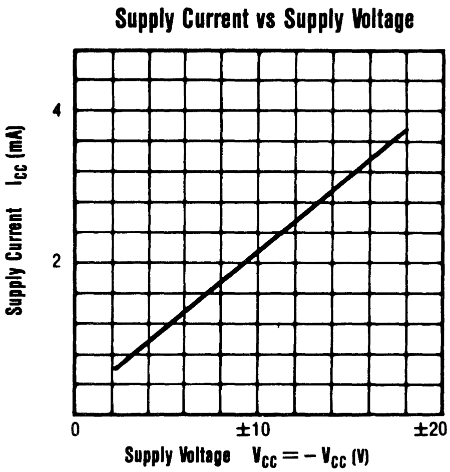
Power Dissipation vs Ambient Temperature

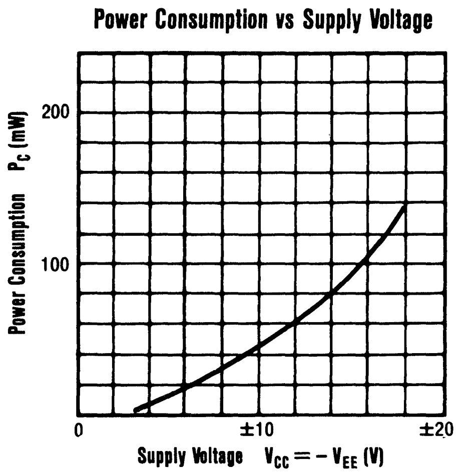


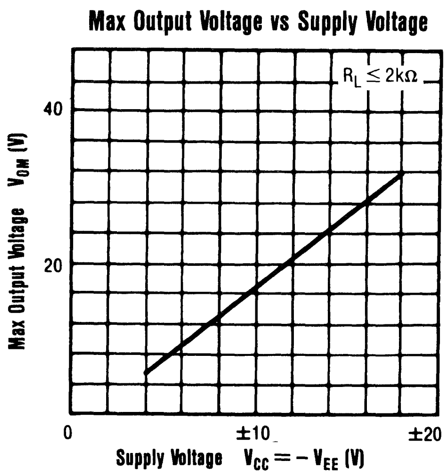
Max Output Voltage vs Frequency

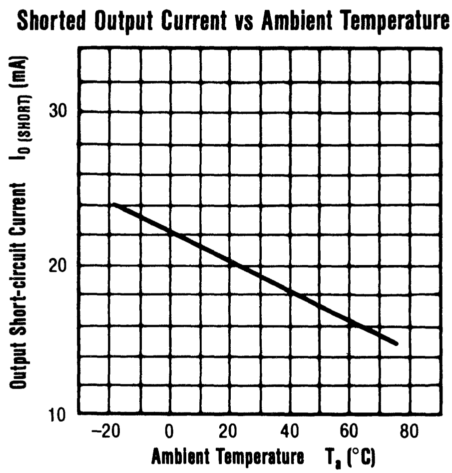


Typical Electrical Performance Curves (continued)



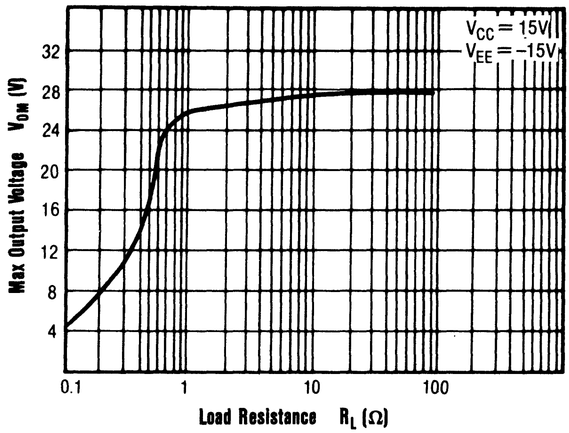




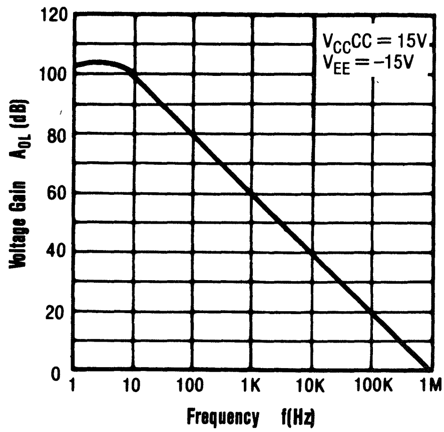


Typical Electrical Performance Curves (continued)

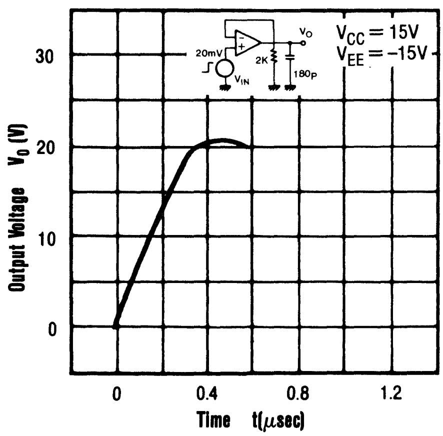
Max Output Voltage vs Load Resistance



Voltage Gain vs Frequency

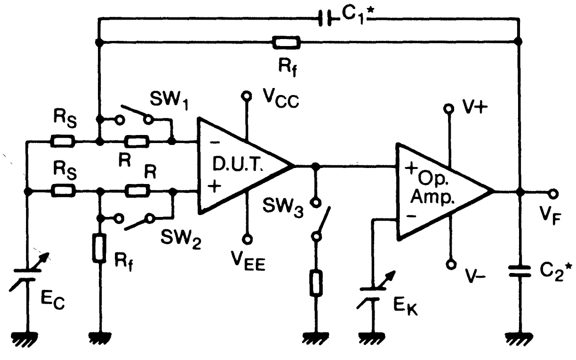


Response Time



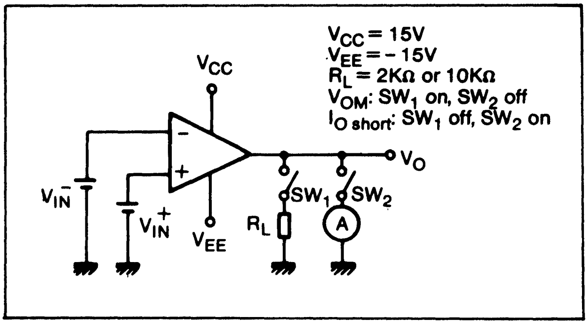
Test Circuit 1 (½ circuit)

R_S = 50Ω V_{EE} = −15V
R = 10KΩ V+ = 15V
R_f = 20KΩ V− = −15V
V_{CC} = 15V

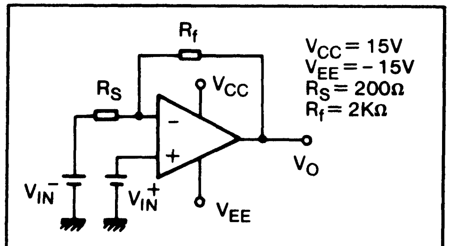


*C_1 and C_2 to prevent oscillation

Test Circuit 2 (½ circuit)

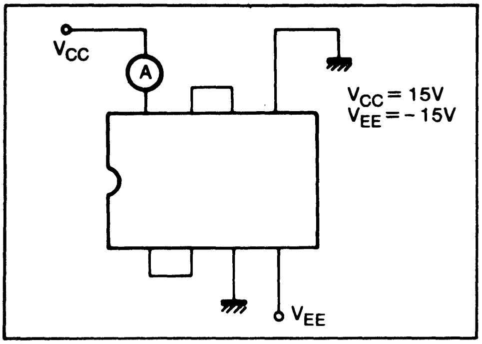


Test Circuit 3 (½ circuit)

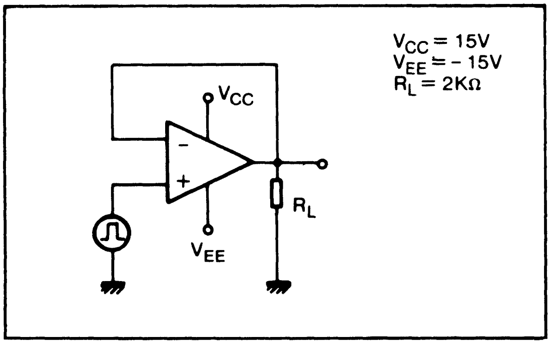


Apply $\|V_{IN}\|$> 12V voltage and make sure that it is $V_O = V_{IN}^+ + \frac{R_f}{R_S}(V_{IN}^+ - V_{IN}^-)$

Test Circuit 4

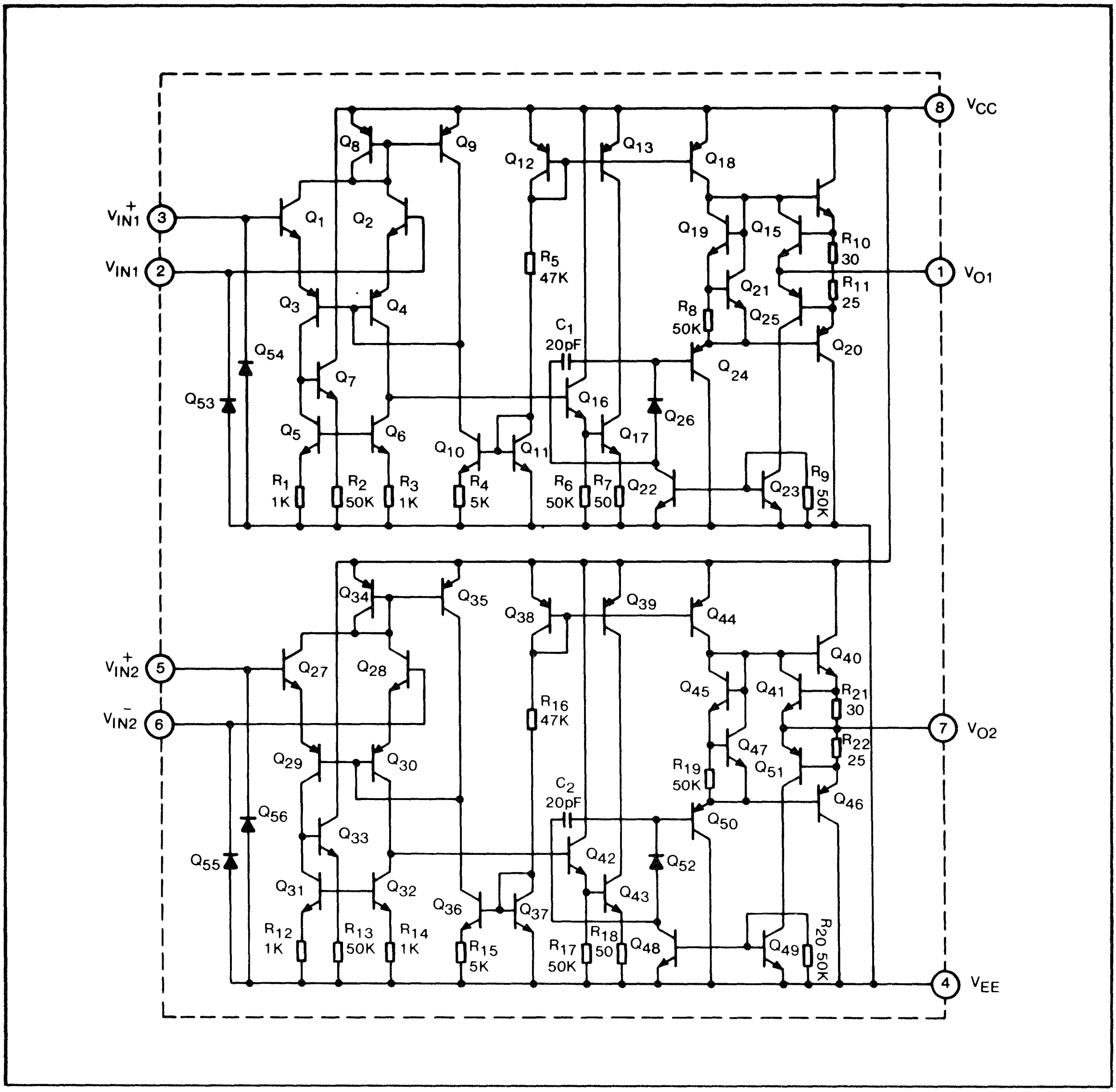


Test Circuit 5 (½ circuit)



Item	Test conditions for Circuit 1
Input Offset Voltage	With SW1, SW2, and SW3 off, V_{F1} is measured on the basis of $E_C = E_K = 0$, where $V_{IO} = V_{F1}/400$ (V).
Input Offset Current	With SW1, SW2 on and SW3 off, V_{F2} is measured on the basis of $E_C = E_K = 0$, where $I_{IO} = \|V_{F2} - V_{F1}\| /4 \times 10^6$ (A).
Input Bias Current	With SW3 off while $E_C = E_K = 0$ and SW1, on, SW2, off, V_{F3} is measured. V_{F4} is measured with SW1 and SW2 inverse. Where $I_B = \|V_{F3} - V_{F4}\|/8 \times 10^6$ (A).
Voltage Gain	With SW1, SW2 and SW3 on and $E_C = 0$, $E_K = 10V$, V_{F5} is measured and V_{F5} is measured again with $E_K = -10V$. Where $A_{OL} = 20 \log \left(\frac{8000}{V_{F5} - V_{F5}}\right)$
Common-Mode Rejection Ratio	With SW1 and SW2 on, SW3 off, and $E_K = 0$, $E_C = 5V$, V_{F6} is measured. With $E_C = -5V$, V_{F6} is measured again. Where: $CMRR = \left(\frac{4000}{V_{F6} - V_{F6}}\right)$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on, SW3 off, $E_K = E_C = 0$, $V_{CC} = 10V$, V_{F7} is measured. Where: PSRR (+) = $\|V_{F7} - V_{F2}\|/2 \times 10^3$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on SW3, off and $E_K = E_C = 0$ $V_{EE} = -10V$, V_{F8} is measured, Where: PSRR (−) = $\|V_{F8} - V_{F2}\|$ 2×10^3

Schematic Diagram

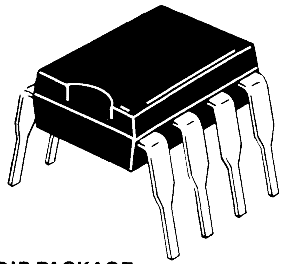


AN1741/AN1741S (AN6570) OPERATIONAL AMPLIFIER

General Description

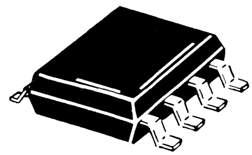
The AN1741 is a high performance general purpose operational amplifier. It has internal phase compensation and high gain making it a suitable replacement for most standard "741" applications

AN1741 (AN6570)



8 - DIP PACKAGE

AN1741S



SO - 8D PACKAGE

Features

- No frequency compensation required
- Short circuit protection
- Low power consumption
- Both 8 - pin DIP and 8 - pin S.O. packages available

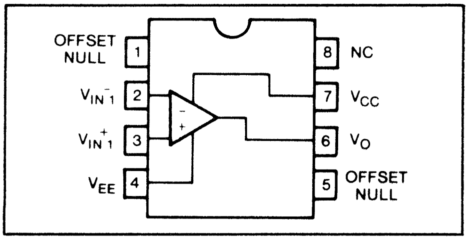
Absolute Maximum Ratings ($T_a = 25°C$)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	±18	V
Power Dissipation	(8 DIP)	P_D	500	mW
	(8 SO)	P_D	370	mW
Input Differential Voltage		V_{ID}	±30	V
Input Common−Mode Voltage		V_{ICM}	±15	V
Operating Temperature		Topr	− 20 to.+ 75	°C
Storage Temperature	(8 DIP)	Tstg	− 55 to + 150	°C
	(8 SO)	Tstg	− 55 to + 125	°C

Electrical Characteristics ($V_{CC} = -V_{EE} = 15V$, $T_a = 25°C$)

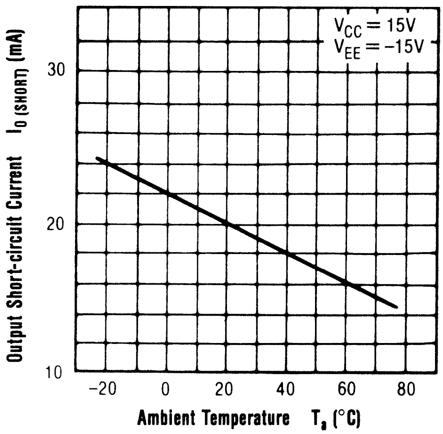
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	4	mV
Input Offset Current	I_{IO}	1			10	100	nA
Input Bias Current	I_B	1			50	250	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	106		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±13		V
Common-Mode Rejection Ratio	CMRR	1	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	PSRR	1	$R_S \leq 10k\Omega$		30	150	μV/V
Power Consumption	P_C	4				85	mW
Slew Rate	SR	5			0.7		V/μs
Supply Current	I_{CC}	4				2.8	mA
Output Short-Circuit Current	$I_{O(SHORT)}$	2			±20		mA

Connection Diagram

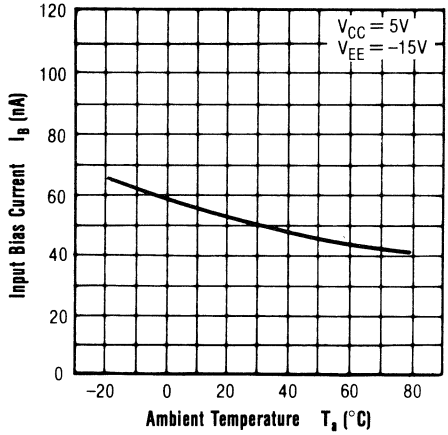


Typical Electrical Performance Curves

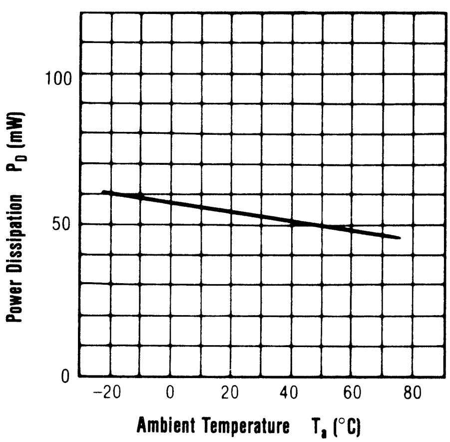
Output Short-circuit vs Ambient Temperature



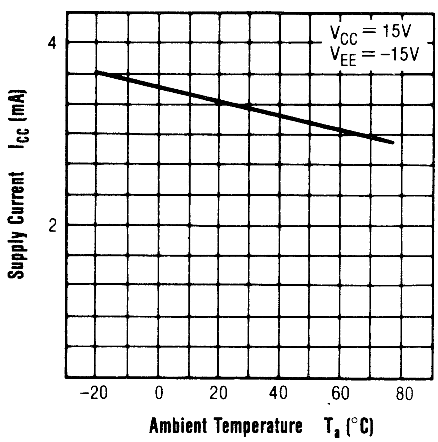
Input Bias Current vs Ambient Temperature



Power Dissipation vs Ambient Temperature

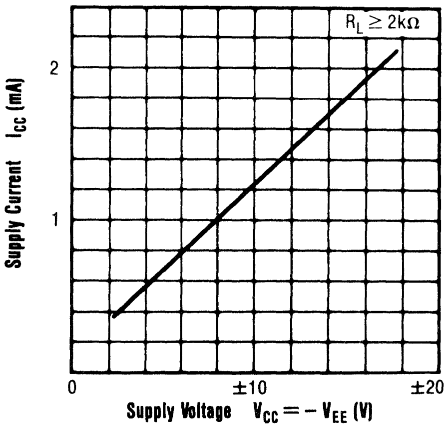


Supply Current vs Ambient Temperature

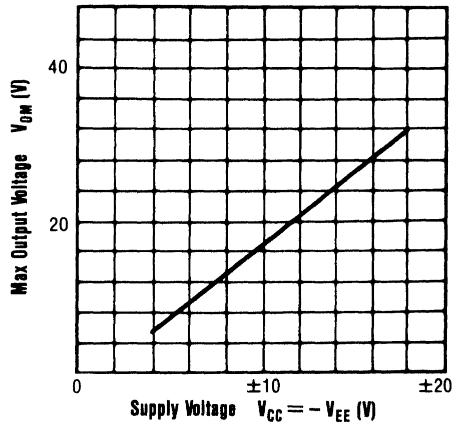


Typical Electrical Performance Curves (continued)

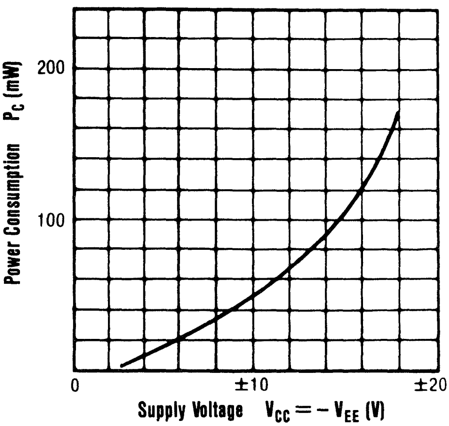
Supply Current vs Supply Voltage



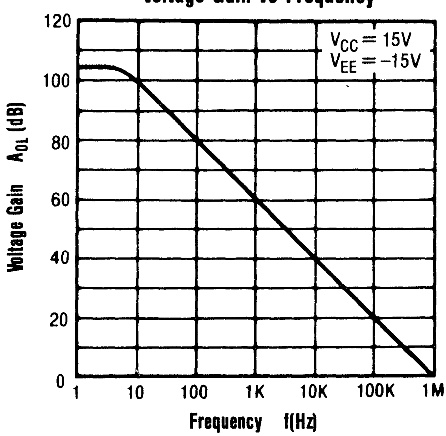
Max Output Voltage vs Load Resistance



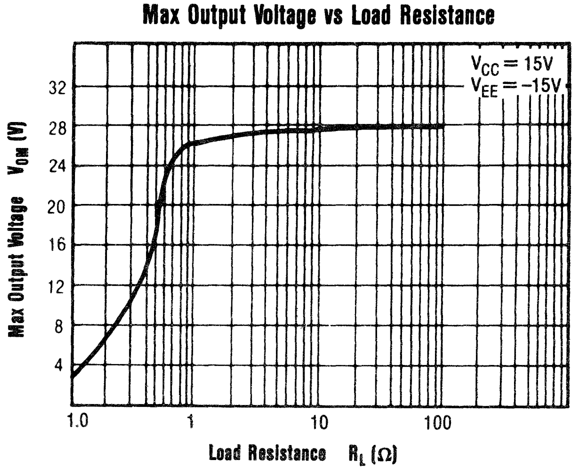
Power Consumption vs Supply Voltage

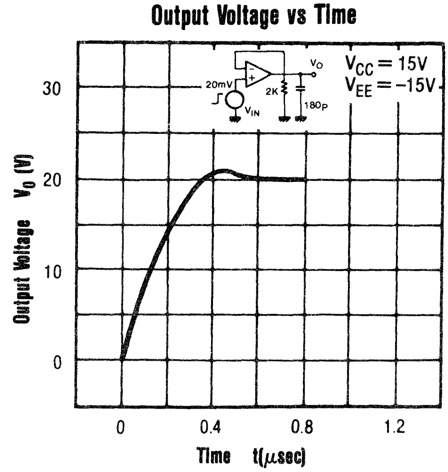


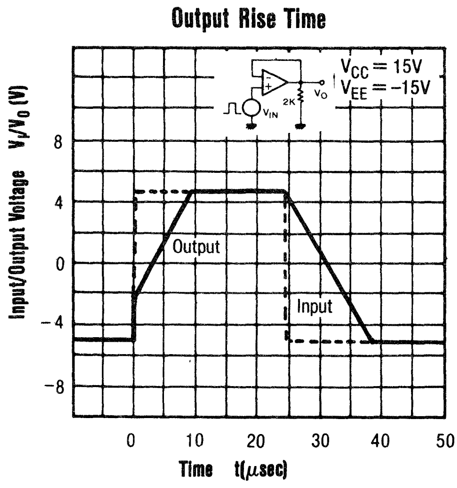
Voltage Gain vs Frequency

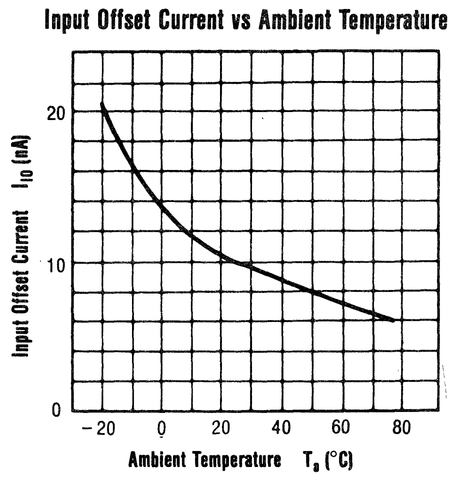


Typical Electrical Performance Curves (continued)

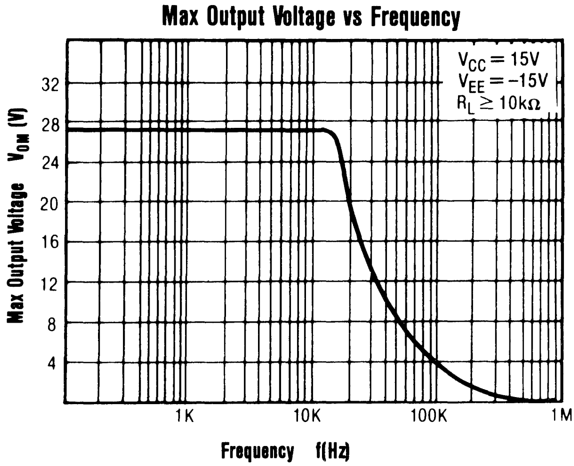




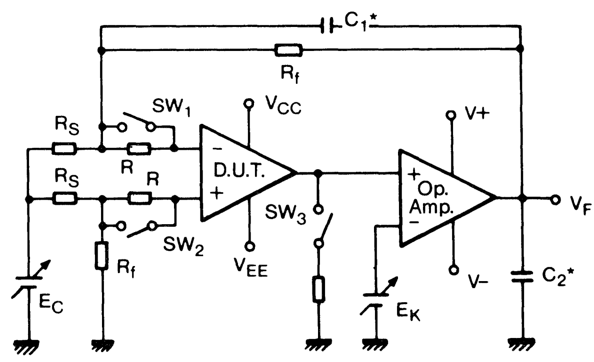




Typical Electrical Performance Curves (continued)



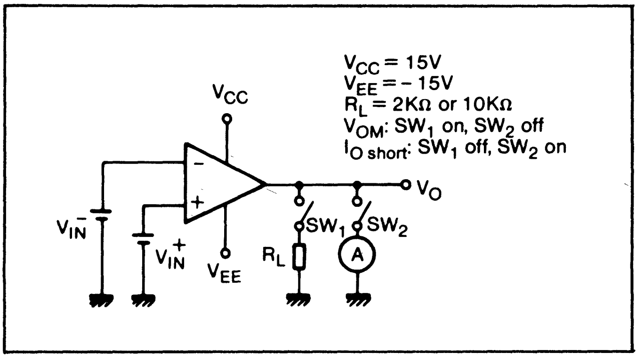
Test Circuit 1



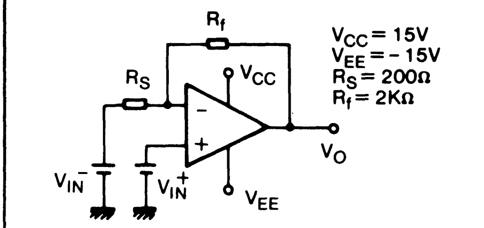
$R_S = 50\Omega$
$R = 10K\Omega$
$R_f = 20K\Omega$
$V_{CC} = 15V$
$V_{EE} = -15V$
$V+ = 15V$
$V- = -15V$

*C_1 and C_2 to prevent oscillation

Test Circuit 2

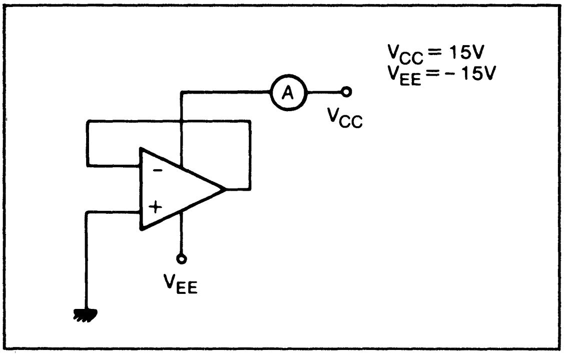


Test Circuit 3

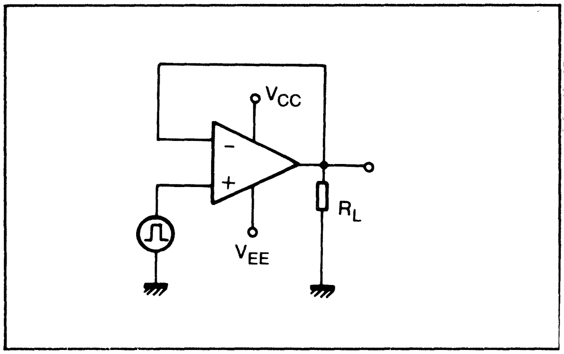


Apply $||V_{IN}||$ > 12V voltage and make sure that it is $V_O = V_{IN}^+ + \frac{R_f}{R_S}(V_{IN}^+ - V_{IN}^-)$

Test Circuit 4

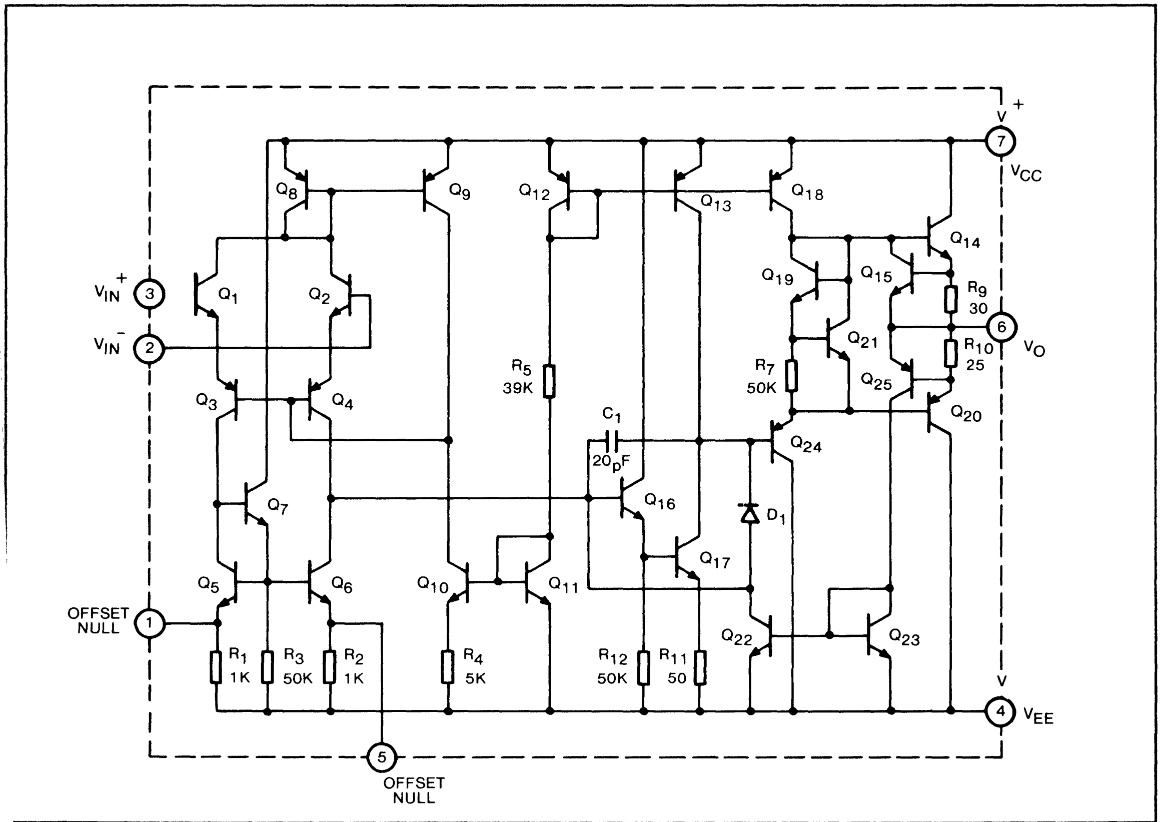


Test Circuit 5



Item	Test conditions for Circuit 1
Input Offset Voltage	With SW1, SW2, and SW3 off, V_{FI} is measured on the basis of $E_C = E_K = 0$, where $V_{IO} = V_{F1}/400$ (V).
Input Offset Current	With SW1, SW2 on and SW3 off, V_{F2} is measured on the basis of $E_C = E_K = 0$, where $I_{IO} = \|V_{F2} - V_{F1}\| / 4 \times 10^6$ (A).
Input Bias Current	With SW3 off while $E_C = E_K = 0$ and SW1, on, SW2, off, V_{F3} is measured. V_{F4} is measured with SW1 and SW2 inverse. Where $I_B = \|V_{F3} - V_{F4}\| / 8 \times 10^6$ (A).
Voltage Gain	With SW1, SW2 and SW3 on and $E_C = 0$, $E_K = 10V$, V_{F5} is measured and V_{F5} is measured again with $E_K = -10V$. Where $A_{OL} = 20 \log \left(\frac{8000}{V_{F5} - V_{F5}}\right)$
Common-Mode Rejection Ratio	With SW1 and SW2 on, SW3 off, and $E_K = 0$, $E_C = 5V$, V_{F6} is measured. With $E_C = -5V$, V_{F6} is measured again. Where: CMRR $= \left(\frac{4000}{V_{F6} - V_{F6}}\right)$
Supply Voltage (–) Rejection Ratio (+)	With SW1,.SW2 on, SW3 off, $E_K = E_C = 0$, $V_{CC} = 10V$, V_{F7} is measured. Where: PSRR (+) $= \|V_{F7} - V_{F2}\| / 2 \times 10^3$
Supply Voltage (–) Rejection Ratio (+)	With SW1, SW2 on SW3, off and $E_K = E_C = 0$ $V_{EE} = -10V$, V_{F8} is measured, Where: PSRR (–) $= \|V_{F8} - V_{F2}\|$ 2×10^3

Schematic Diagram



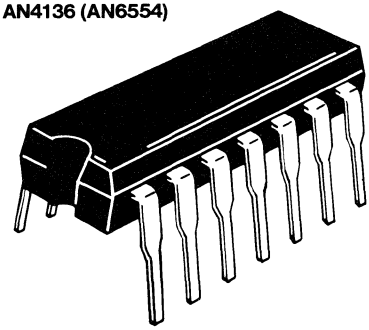
General Description

AN4136 is a quadruple operational amplifier that includes internal phase compensation. Its high gain and low noise characteristics make it suitable for many applications.

Features

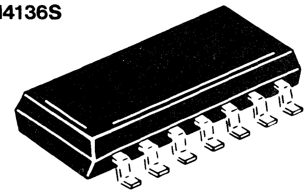
- Internal phase compensation
- High gain, low noise
- Output short protection circuit
- Available in 14 - pin DIP or 14 - lead S.O. packages

AN4136 (AN6554)



14 - DIP PACKAGE

AN4136S



SO - 14D PACKAGE

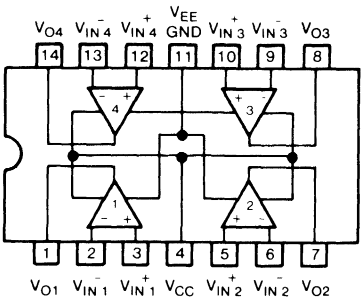
Absolute Maximum Ratings (T_a = 25°C)

Item		Symbol	Ratings	Unit
Supply Voltage		Vcc, VEE	36	V
Power Dissipation	(14 DIP)	PD	570	mW
	(14 SO)	PD	380	mW
Input Differential Voltage		VID	±30	V
Input Common –Mode Voltage		VICM	±15	V
Operating Temperature		Topr	– 20 to + 75	°C
Storage Temperature	(14 DIP)	Tstg	– 55 ~ + 150	°C
	(14 SO)	Tstg	– 55 to + 125	°C

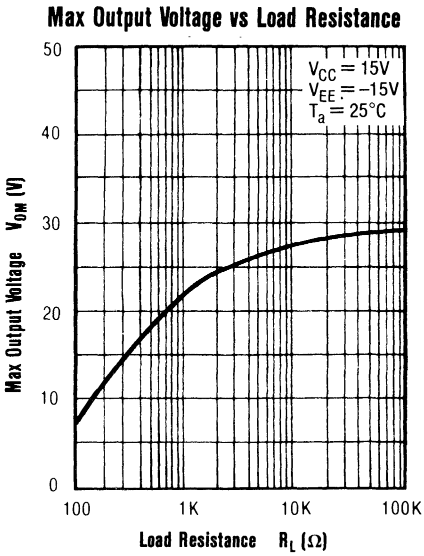
Electrical Characteristics (Vcc = 15V, VEE = - 15V, Ta = 25°C)

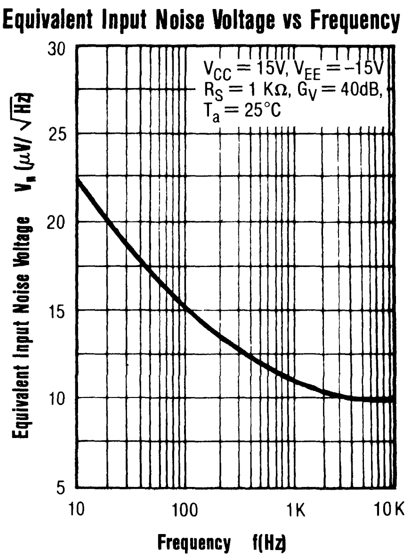
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	VIO	1	RS ≤ 10kΩ		0.5	5	mV
Input Offset Current	IIO	2			5	50	nA
Input Bias Current	IB	2			100	300	nA
Voltage Gain	AOL	3	RL ≥ 2kΩ, VO = ±10V	88	100		dB
Output Voltage (max)	VO1	4	RL ≥ 10kΩ	±12	±14		V
	VO2	4	RL ≥ 2kΩ	±10	±13		V
Common-Mode Input Voltage	VCM	5		±12	±14		V
Common-Mode Rejection Ratio	CMRR	6		70	90		dB
Supply Voltage Rejection Ratio	PSRR	7			30	100	μV/V
Power Consumption	PC	8				240	mW
Slew Rate	SR	9			1.6		V/μs
Equivalent Input Noise Voltage	Vn	10	RS = 1kΩ, B: 10Hz to 30kHz		2.5		μVrms
Channel Separation	CS	11	f = 10kHz		110		dB

Connection Diagram

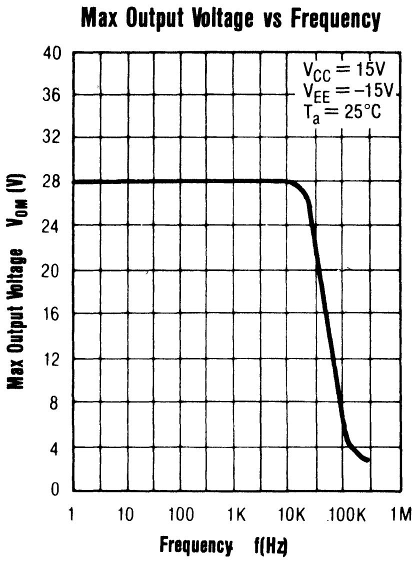


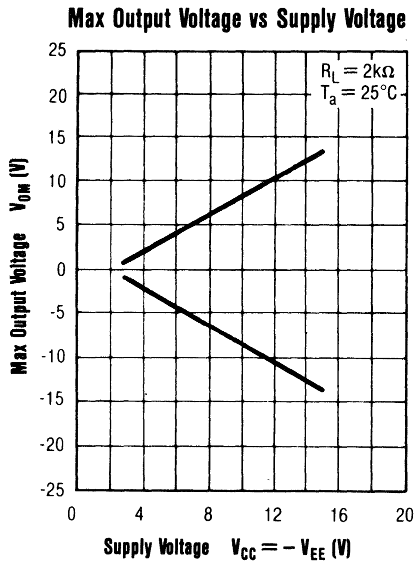
Typical Electrical Performance Curves

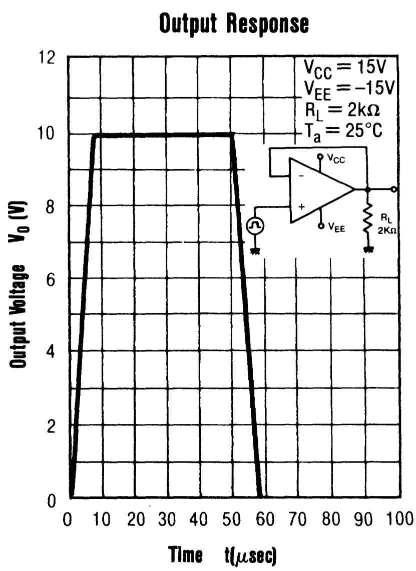


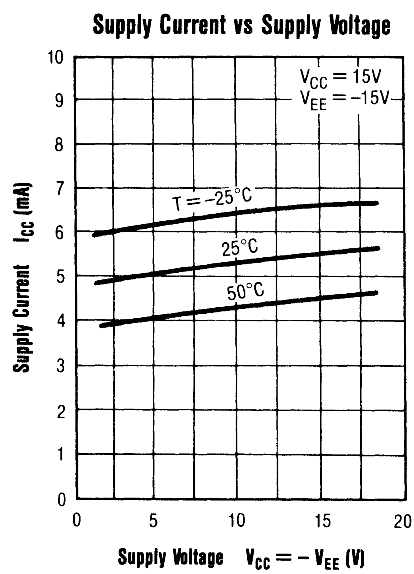


Typical Electrical Performance Curves (continued)

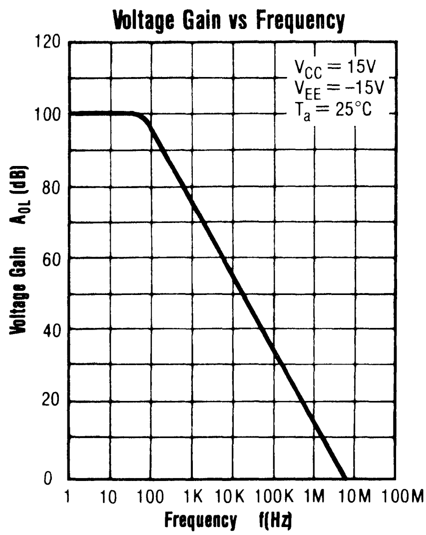


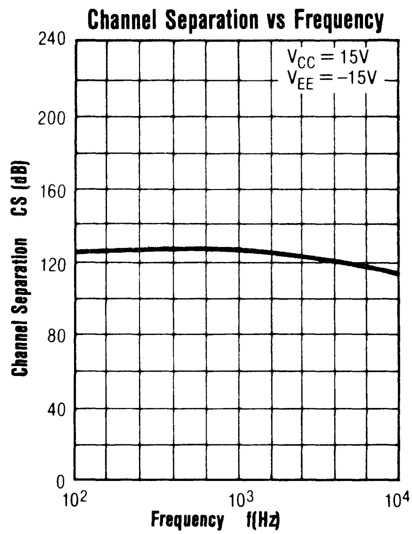




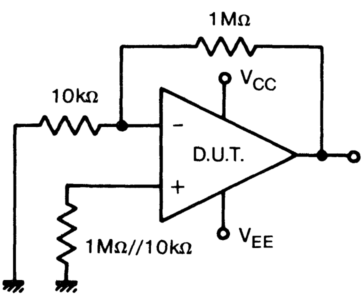


Typical Electrical Performance Curves (continued)

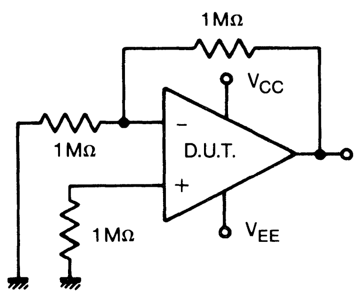




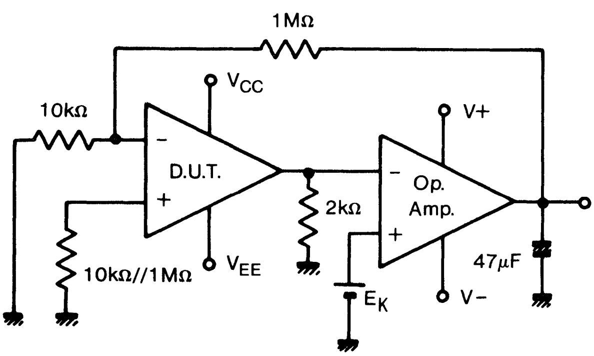
Test Circuit 1 (¼ circuit)



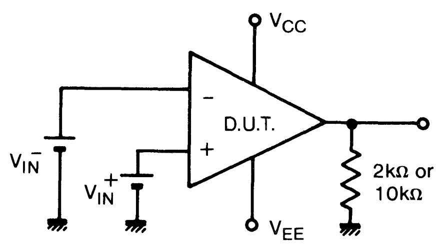
Test Circuit 2 (¼ circuit)



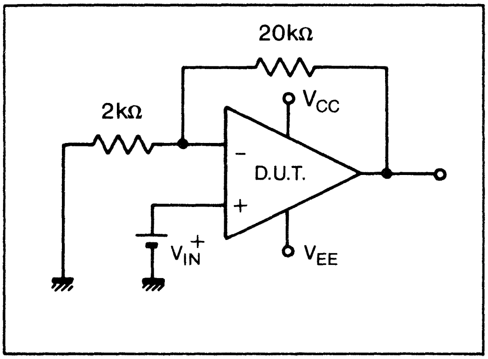
Test Circuit 3 (¼ circuit)



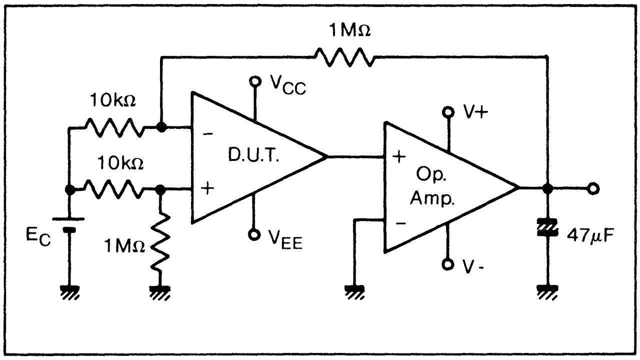
Test Circuit 4 (¼ circuit)



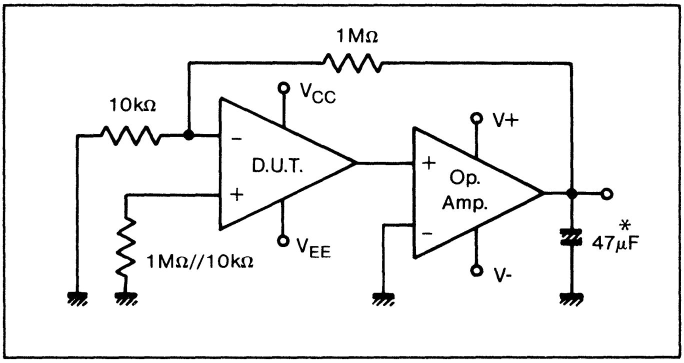
Test Circuit 5 (1/4 circuit)



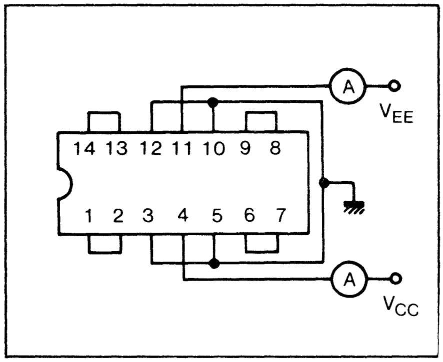
Test Circuit 6 (1/4 circuit)



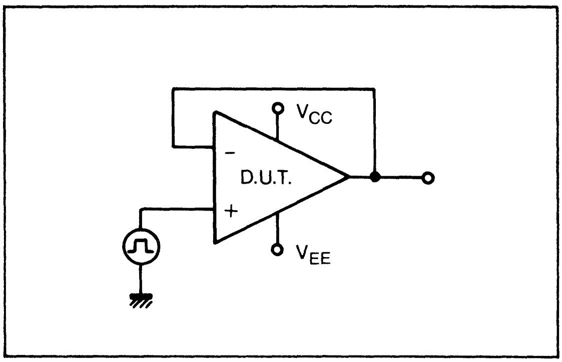
Test Circuit 7 (1/4 circuit)



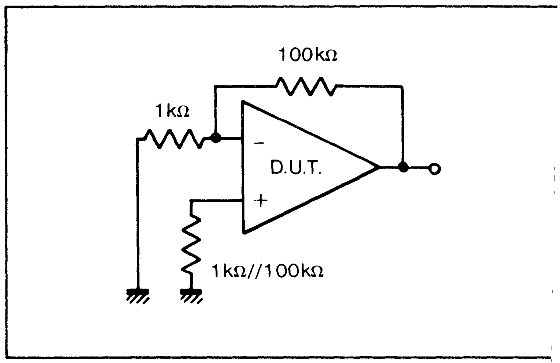
Test Circuit 8



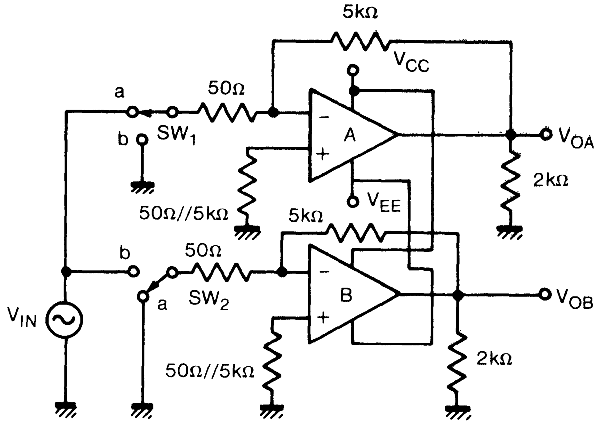
Test Circuit 9 (1/4 circuit)



Test Circuit 10 (1/4 circuit)



Test Circuit 11 (½ circuit)



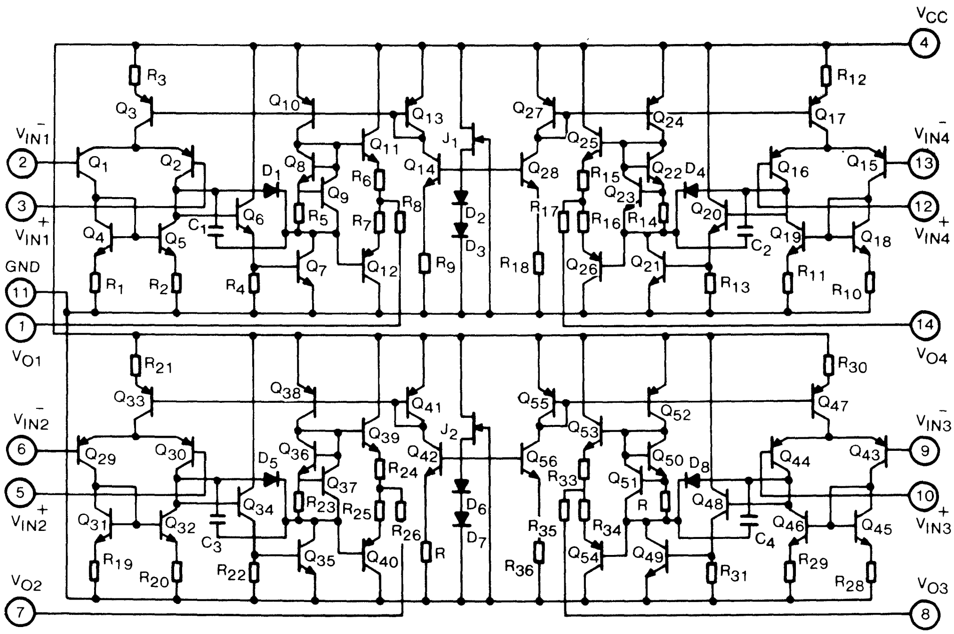
Turn SW1/SW2 to A side

$$S_{EP}(A \rightarrow B) = 20 \log \frac{100V_{OA}}{V_{OB}}$$

Turn SW1/SW2 to B side

$$S_{EP}(B \rightarrow A) = 20 \log \frac{100V_{OB}}{V_{OA}}$$

Schematic Diagram

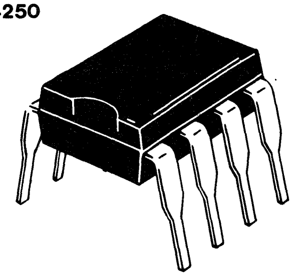


AN4250/AN4250S OPERATIONAL AMPLIFIER

General Description

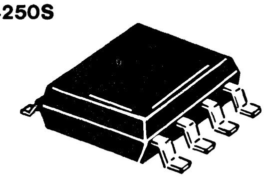
The AN4250 is a versatile, programmable, operational amplifier. A single external bias current, setting resistor programs: the bias current, offset current, quiescent power consumption, slew rate, input noise and the gain-bandwidth product.

AN4250



8 - DIP PACKAGE

AN4250S



SO - 8D PACKAGE

Features

- Operates from ± 1V to ± 18V
- Electric characteristics can be programmed by changing set current
- Phase compensation circuit is built-in
- Output short circuit protection circuit is built-in
- Off-set is externally adjustable

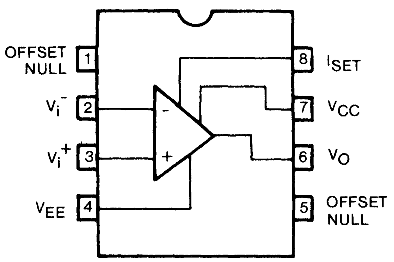
Absolute Maximum Ratings ($T_a = 25°C$)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	± 18	V
Power Dissipation	(8 DIP)	P_D	500	mW
	(8 SO)	P_D	360	mW
Input Differential Voltage		V_{ID}	± 30	V
Input Common –Mode Voltage		V_{ICM}	± 15	V
Operating Temperature		Topr	– 20 to + 75	°C
Storage Temperature	(8 DIP)	Tstg	– 50 to + 150	°C
	(8 SO)	Tstg	– 50 to + 125	°C

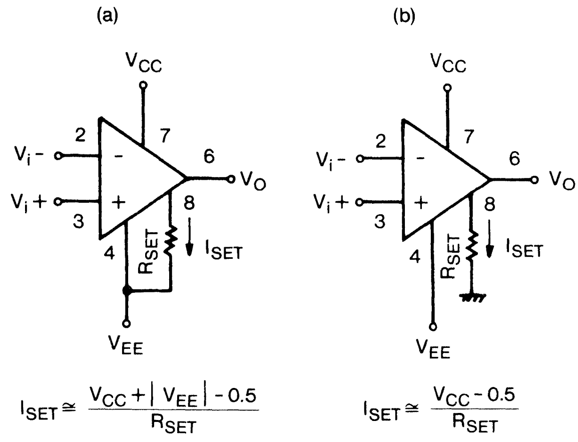
Electrical Characteristics ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25°C$)

Item	Symbol	Condition	$I_{SET} = 1\mu A$		$I_{SET} = 10\mu A$		Unit
			min.	max.	min.	max.	
Input Offset Voltage	V_{IO}	$R_S \leq 100k\Omega$		5		6	mV
		$V\pm = \pm 1.5V$, $R_S \leq 100k\Omega$		5		6	
Input Offset Current	I_{IO}			6		20	nA
Input Bias Current	I_B			10		75	nA
		$V\pm = \pm 1.5$		10		75	
Large Signal Voltage Gain	A_{OL}	$V_O = \pm 10V$, $R_L = 100k\Omega$	96				dB
		$V_O = \pm 10V$, $R_L = 10k\Omega$			96		
Supply Current	I_{CC}			11		100	µA
		$V\pm = \pm 1.5V$		8		90	
Power Consumption	P_C			330		3000	µW
		$V\pm = \pm 1.5V$		24		270	
Input Common-Mode Voltage	V_{CM}		± 13.5		± 13.5		V
		$V\pm = \pm 1.5V$	± 0.6		± 0.6		
Output Voltage (max)	V_{OM}	$R_L = 100k\Omega$	± 12				V
		$V\pm = \pm 1.5V$, $R_L = 100k\Omega$	± 0.6				
Common-Mode Rejection Ratio	CMRR	$R_L = 10k\Omega$			± 12		V
		$V\pm = \pm 1.5V$, $R_L = 10k\Omega$			± 0.6		
Supply Voltage Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	70		70		dB
		$R_S \leq 10k\Omega$	74		74		

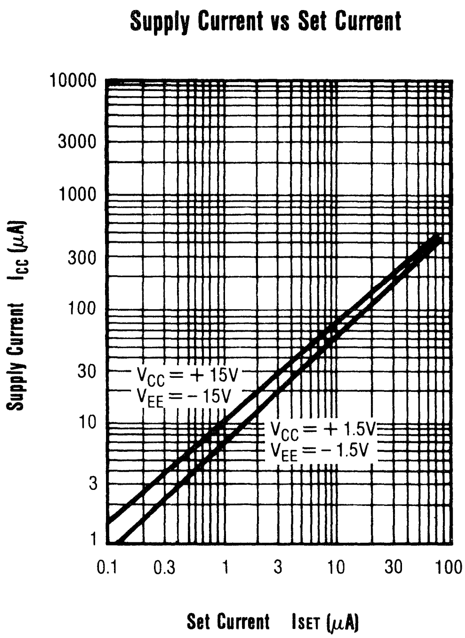
Connection Diagram

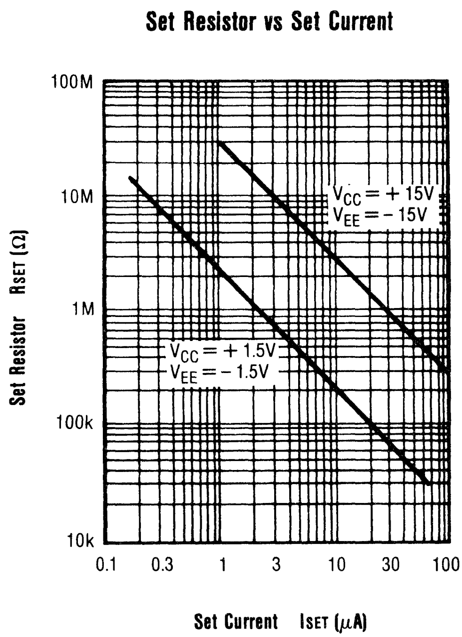


Connections for I_{SET}



Typical Characteristics for I_{SET}



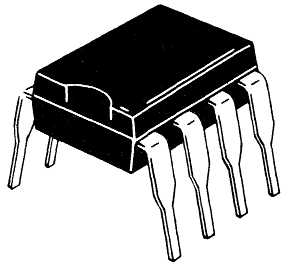


AN4558/AN4558S (AN6552) DUAL OPERATION AMPLIFIER

General Description

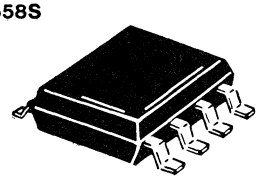
The AN4558 is a dual operational amplifier which has internal phase compensation. It is designed to be a general purpose circuit.

AN4558 (AN6552)



8 - DIP PACKAGE

AN4558S



SO - 8D PACKAGE

Features

- Internal phase compensation
- High gain, low noise
- Output short protection circuit
- Slew rate: 1.0V/μ typ.
- Available in an 8 - pin DIP or 8 - pin S.O. plastic packages

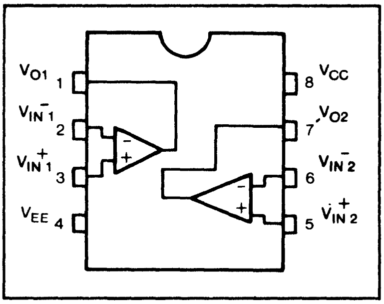
Absolute Maximum Ratings ($T_a = 25°C$)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	± 18	V
Power Dissipation	(8 DIP)	P_D	500	mW
	(8 SO)	P_D	360	mW
Input Differential Voltage		V_{ID}	± 30	V
Input Common−Mode Voltage		V_{ICM}	± 15	V
Operating Temperature		Topr	− 20 to + 75	°C
Storage Temperature	(8 DIP)	Tstg	− 55 to + 150	°C
	(8 SO)	Tstg	− 55 to + 125	°C

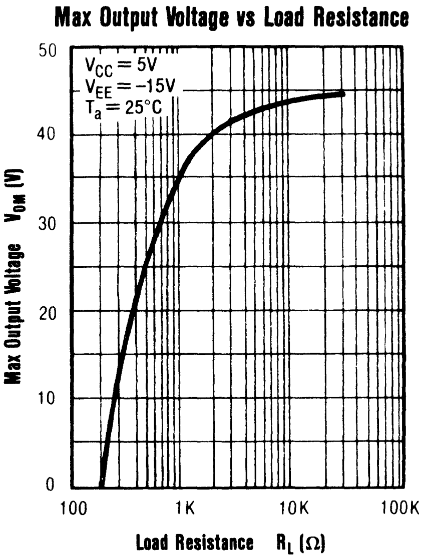
Electrical Characteristics ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25°C$)

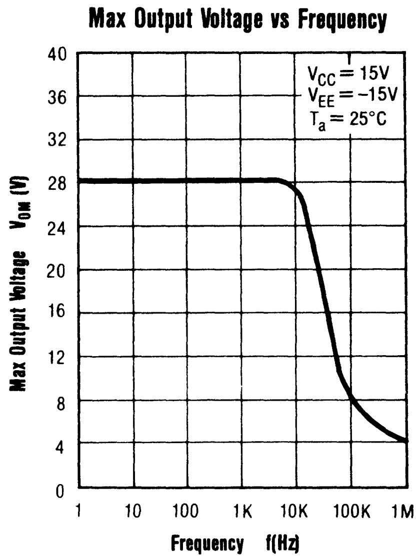
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_B	1				500	nA
Voltage Gain	G_V	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	100		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±14		V
Common-Mode Rejection Ratio	CMRR	1		70	90		dB
Supply Voltage Rejection Ratio	PSRR	1			30	150	μV/V
Power Consumption	P_C	4	$R_L = \infty$		90	170	mW
Slew Rate	SR	5	$R_L = \geq 2k\Omega$		1.0		V/μs
Equivalent Input Noise Voltage	V_{NI}	60	$R_S = 1k\Omega$, B: 10Hz ~ 30kHz		2.5		μVrms

Connection Diagram

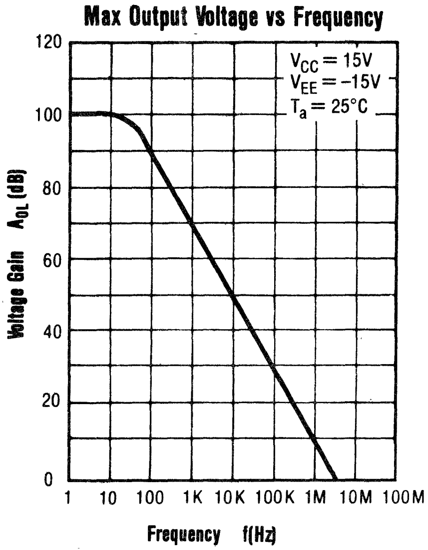


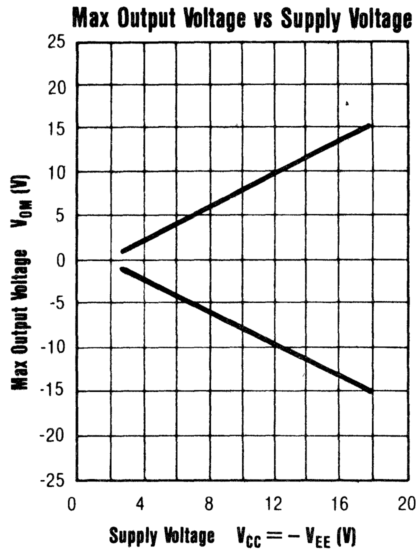
Typical Electrical Performance Curves

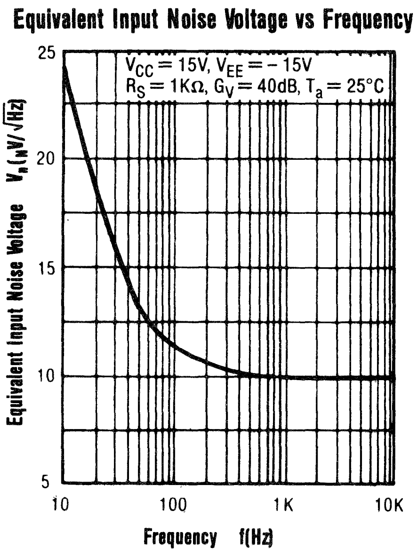


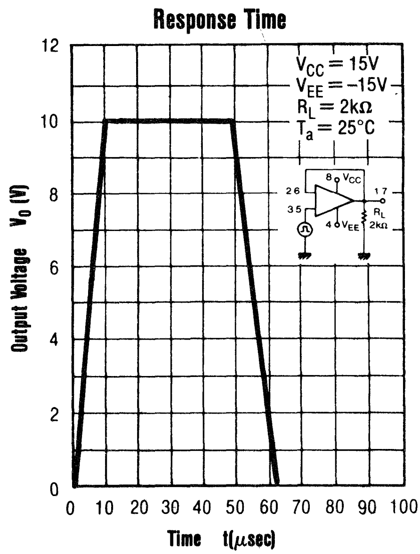


Typical Electrical Performance Curves (continued)

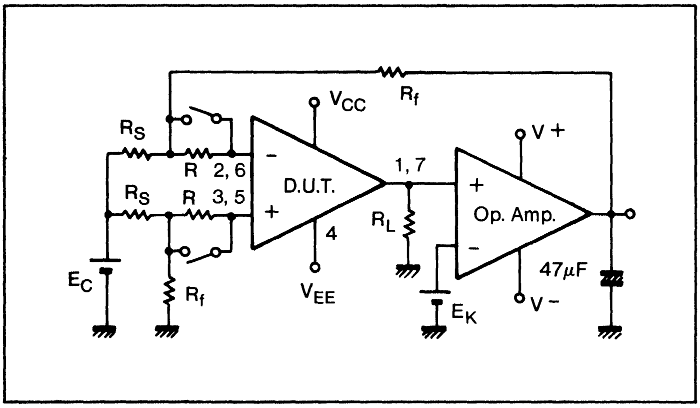




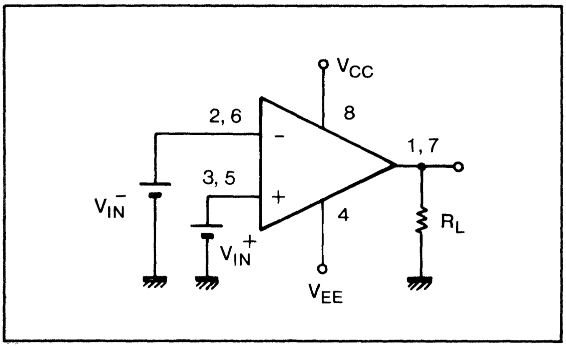




Test Circuit 1 (½ circuit)



Test Circuit 2 (½ circuit)



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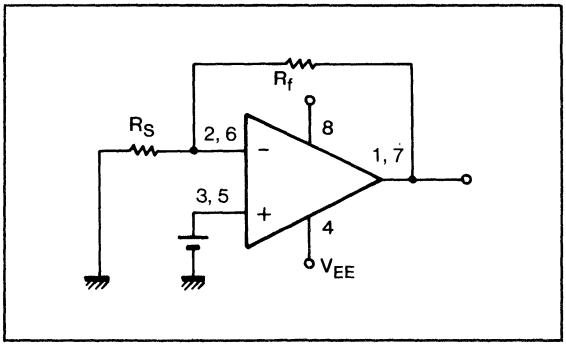
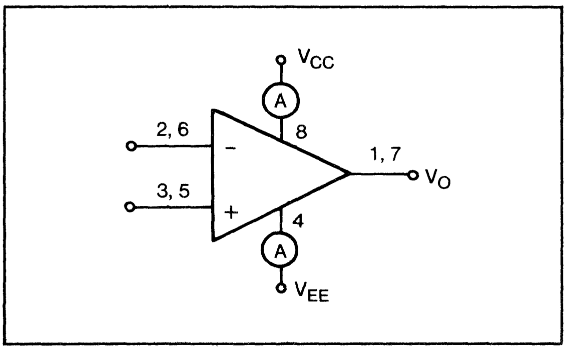
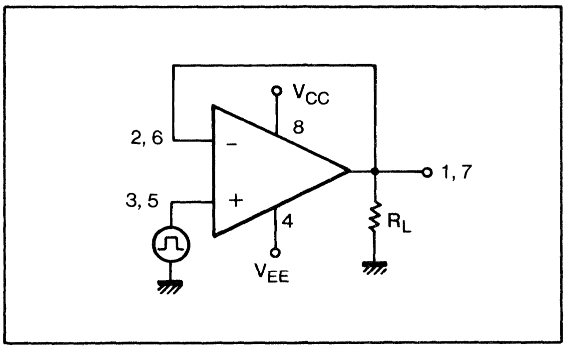


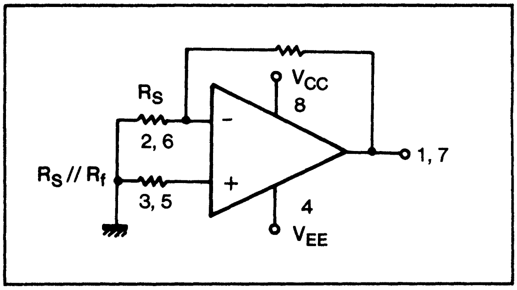
Test Circuit 4 (½ circuit)



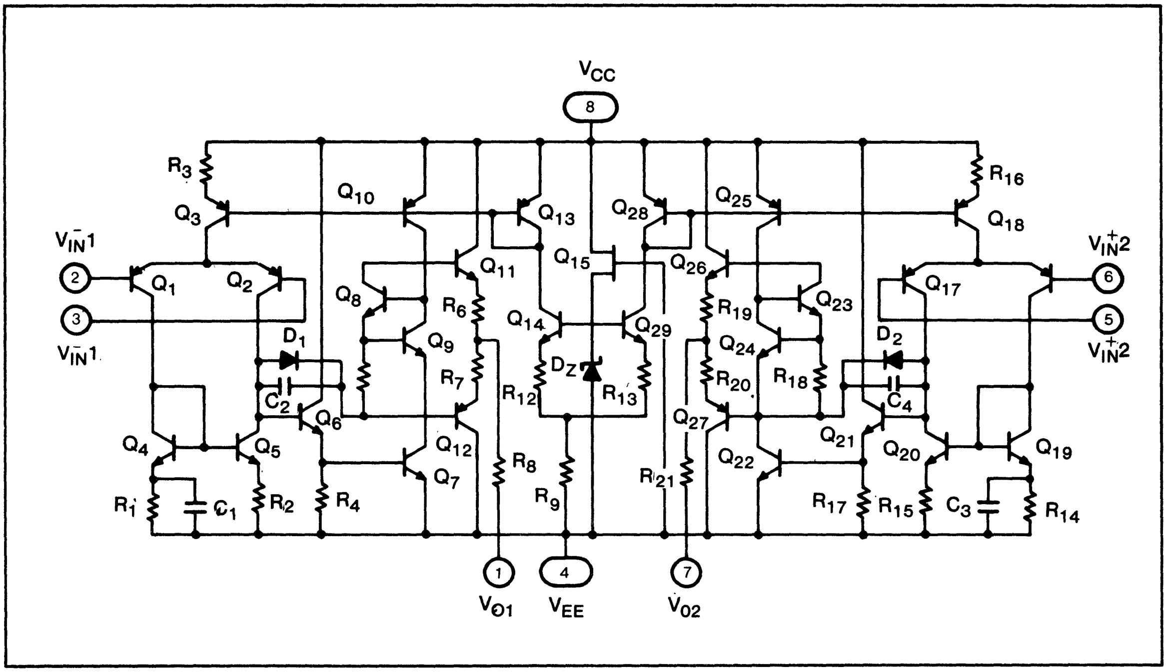
Test Circuit 5 (½ circuit)



Test Circuit 6 (½ circuit)



Schematic Diagram

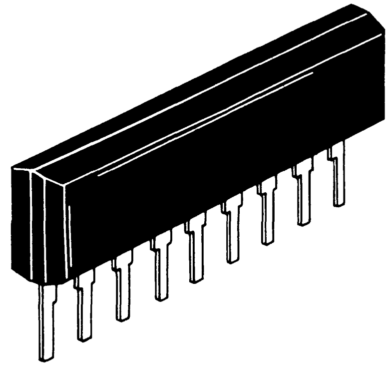


AN6550 DUAL OPERATIONAL AMPLIFIER

General Description

The AN6550 is a dual internally compensated high performance amplifier specifically designed for low-voltage applications. Its gain and noise characteristics are useful in active filter and low-level audio designs. Also, the SIL package is ideal for compact layouts.

AN6550



9-SIP PACKAGE

Features

- No frequency compensation required
- High Gain and low noise operation
- Output short-circuit protected
- Low voltage operation (±2V to ±12V)
- Single-in-line package

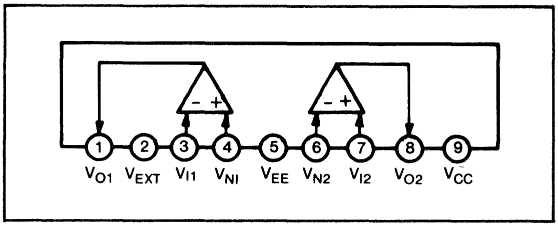
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}, V_{EE}	± 12	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	± 24	V
Input Common –Mode Voltage	V_{ICM}	± 12	V
Operating Temperature	Topr	– 20 to + 75	°C
Storage Temperature	Tstg	– 55 to + 150	°C
External Bias Voltage	V_{EXT}	V_{EE} to V_{CC}	V

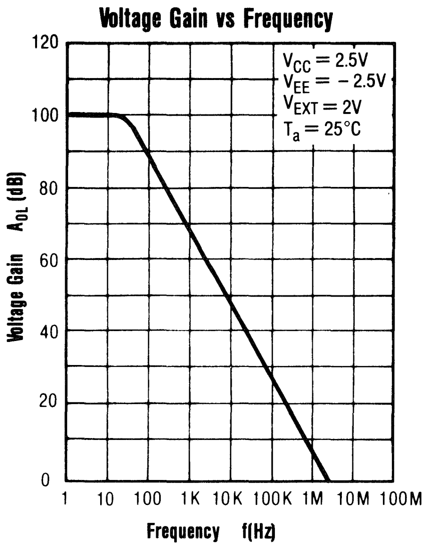
Electrical Characteristics ($V_{CC} = 2.5V$, $V_{EE} = -2.5V$, $V_{EXT} = 2.0V$, $T_a = 25°C$)

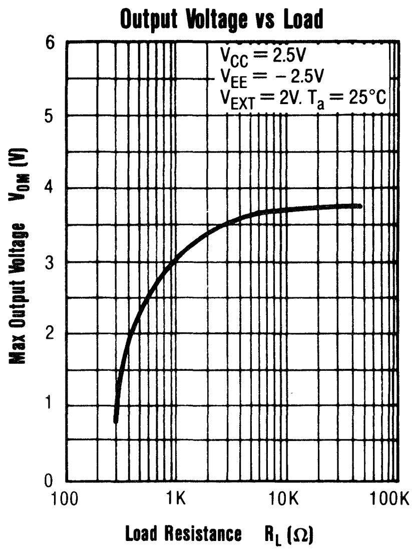
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		1.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_B	1			150	500	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$	65	100		dB
Equivalent Input Noise Voltage	V_n	5	$R_S = 1k\Omega$, BW: 10Hz ~ 30kHz		2.5		µVrms
Max. Output Voltage	V_{OM}	2	$R_L \geq 2k\Omega$	±10	±15		V
Common-Mode Rejection Ratio	CMRR	1		70	80		dB
Supply Voltage Rejection Ratio	PSRR	1			100	300	µV/V
Power Consumption	P_C	3	$R_L = \infty$		8	15	mW
Slew Rate	SR	4	$R_L = \geq 2k\Omega$		0.8		V/µs

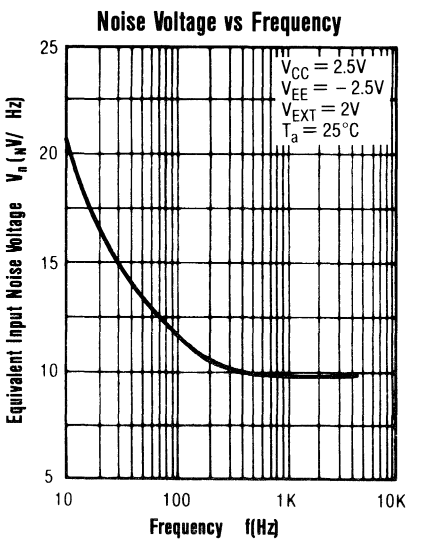
Connection Diagram

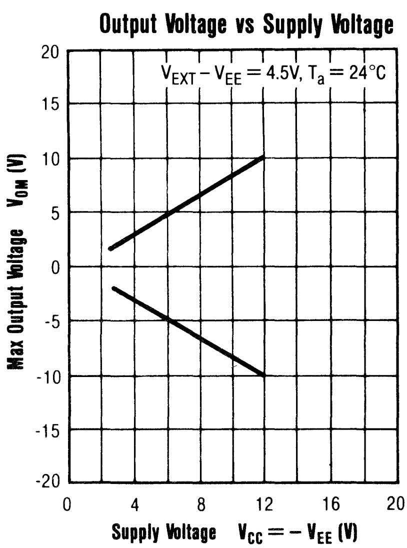


Typical Electrical Performance Curves

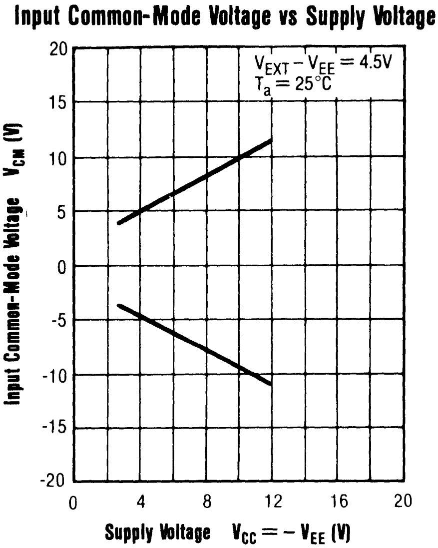


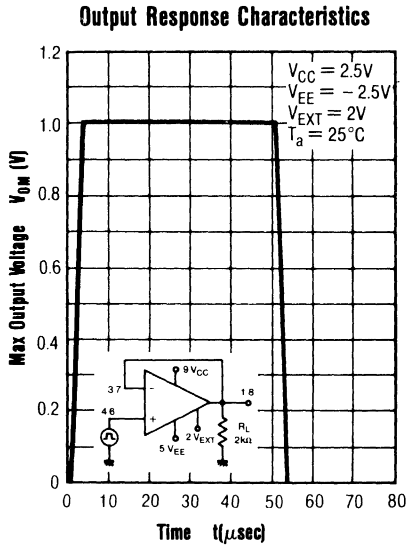


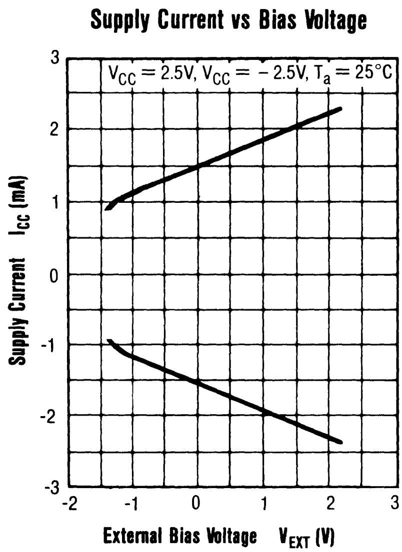


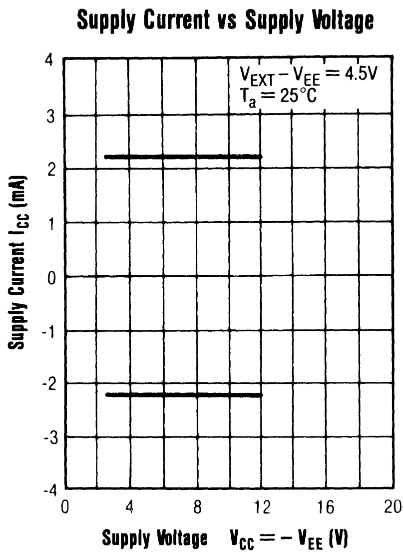


Typical Electrical Performance Curves (continued)

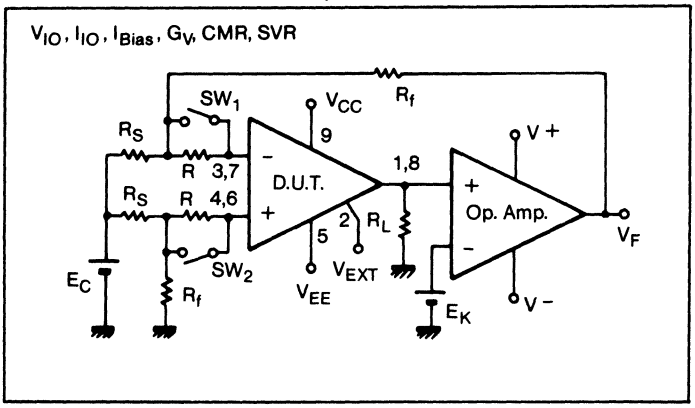








Test Circuit 1 (½ circuit)



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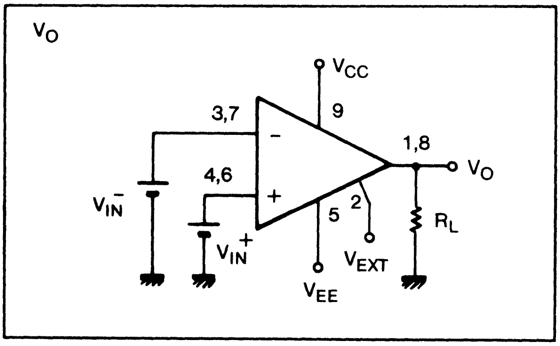
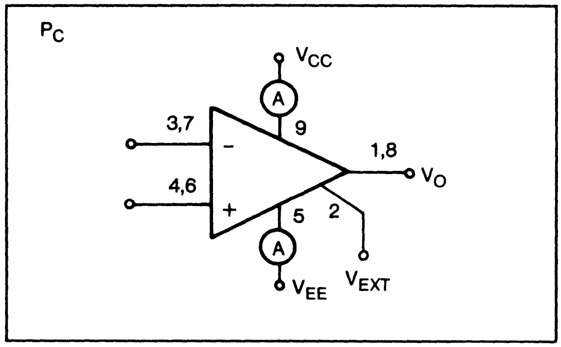
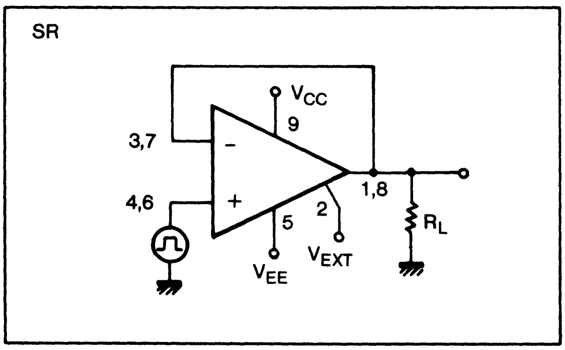


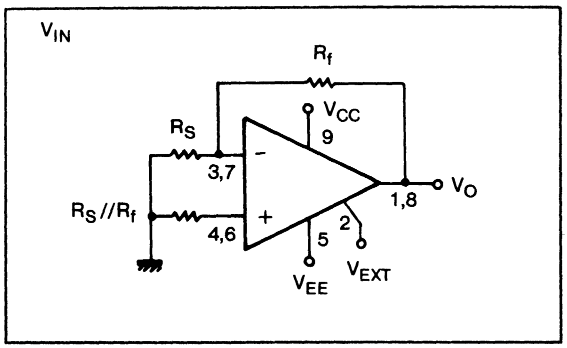
Test Circuit 3 (½ circuit)



Test Circuit 4 (½ circuit)

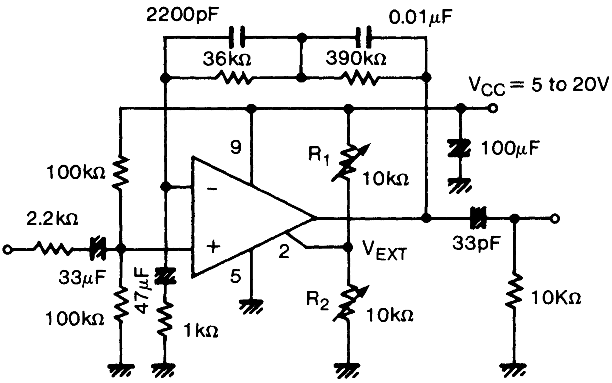


Test Circuit 5 (½ circuit)



Applications

- RIAA audio pre-amplifier (single-supply operation)



R1/R2 are used to adjust bias of amplifier. Typical range of VEXT should be from +2 to +6 Volts with 4.5 Volts recommended.

- BIAS ADJUSTMENT: Altering VEXT will change current consumption and operating Bandwidth. Some suggested methods are shown below:

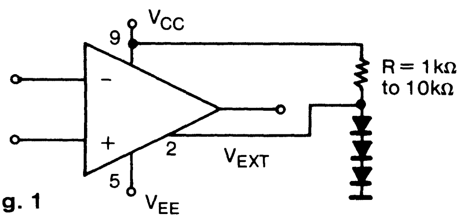


Fig. 1

Derive V_{EXT} by diodes ($V_{EE} = -V_{CC}$)

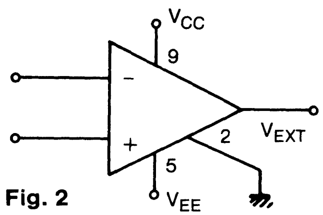


Fig. 2

Connect V_{EXT} to GND ($V_{EE} = -V_{CC}$)

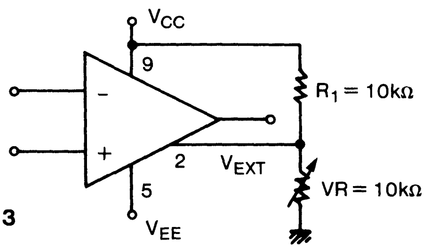


Fig. 3

Derive V_{EXT} voltage by resistor divider

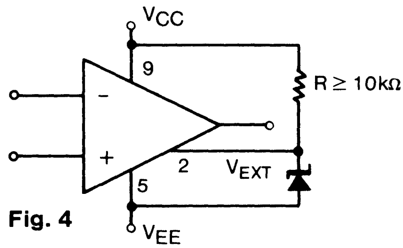
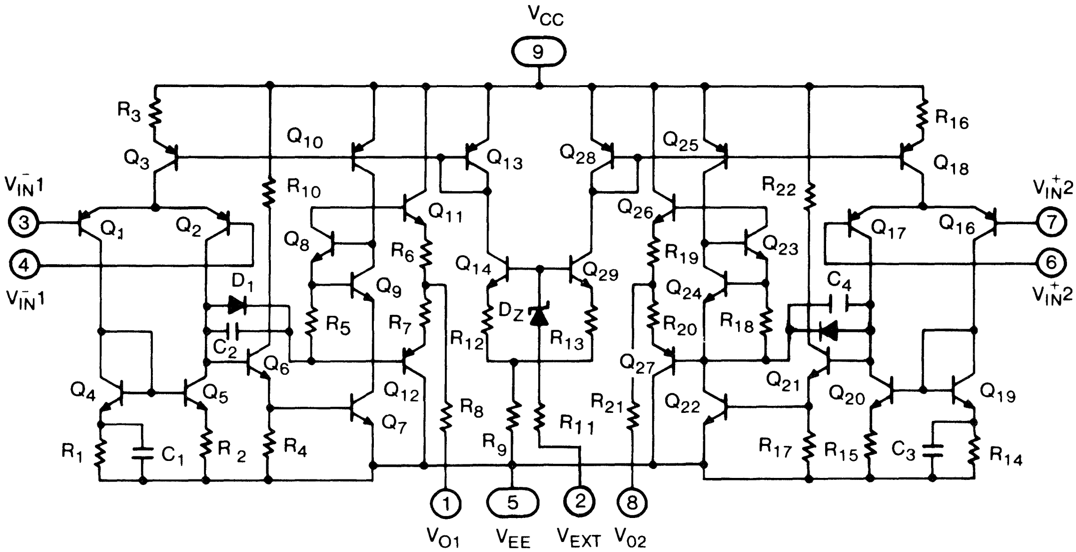


Fig. 4

Derive V_{EXT} voltage from zener diode

Schematic Diagram

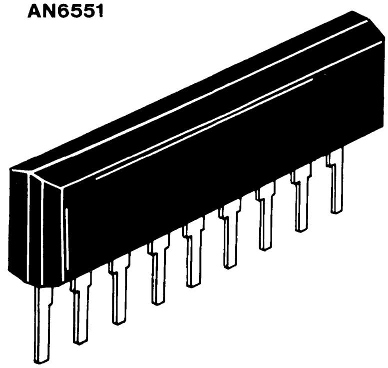


AN6551 DUAL OPERATIONAL AMPLIFIER

General Description

The AN6551 is a dual internally compensated high performance operational amplifier. Its high gain and low noise characteristics over a wide supply voltage range make the AN6551 ideal for many commercial and industrial uses.

AN6551



9 - SIP PACKAGE

Features

- ●No frequency compensation required
- ●High gain, low noise operation
- ●Output short circuit protection
- ●Symmetrical dual circuit pin-out in 9-pin SIL package

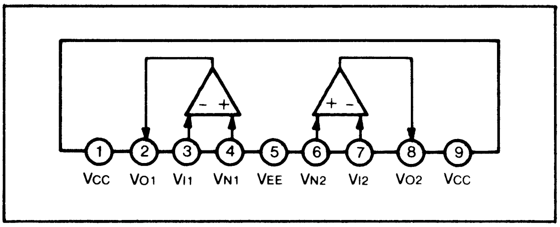
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}, V_{EE}	± 18	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	± 30	V
Input Common –Mode Voltage	V_{ICM}	± 15	V
Operating Temperature	Topr	– 20 to + 75	°C
Storage Temperature	Tstg	– 55 to + 150	°C

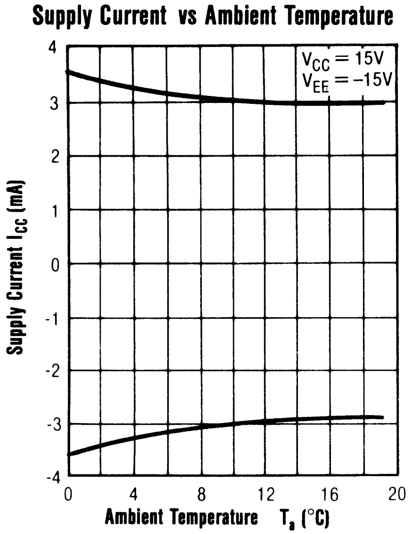
Electrical Characteristics ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25°C$)

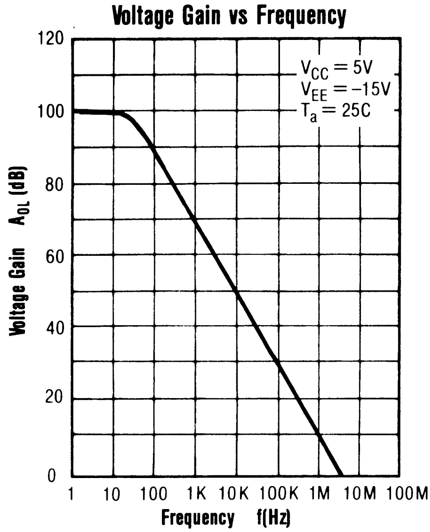
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_B	1				500	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm10V$	86	100		dB
Equivalent Input Noise Voltage	V_n	5	$R_S = 1k\Omega$, BW: 10Hz to 30kHz		2.5		μVrms
Max. Output Voltage	V_{OM}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Rejection Ratio	CMRR	1		70	90		dB
Supply Voltage Rejection Ratio	PSRR	1			30	150	μV/V
Power Consumption	P_C	3	$R_L = \infty$		90	70	mW
Slew Rate	SR	4	$R_L = \geq 2k\Omega$		1.0		V/μs

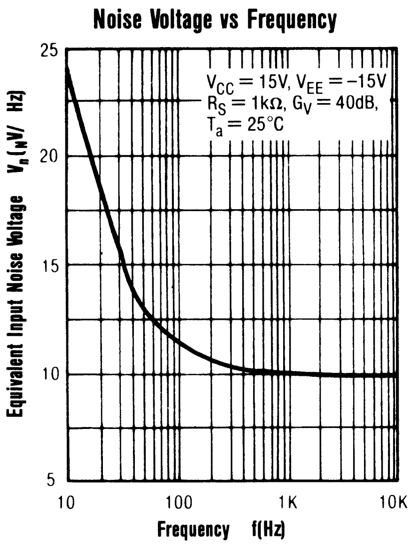
Connection Diagram

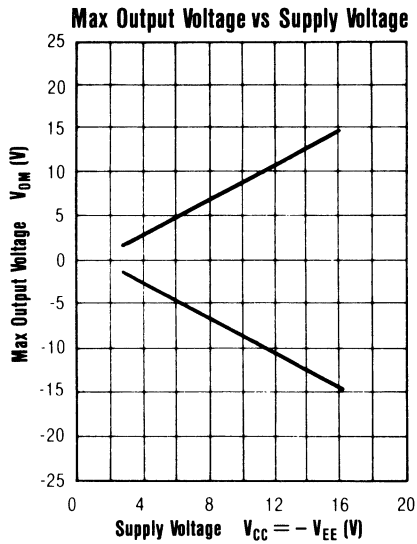


Typical Electrical Performance Curves

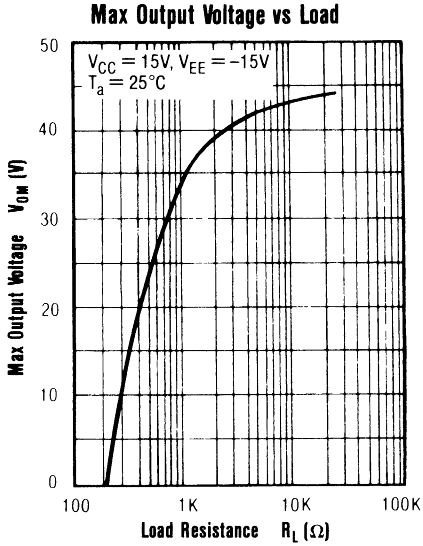


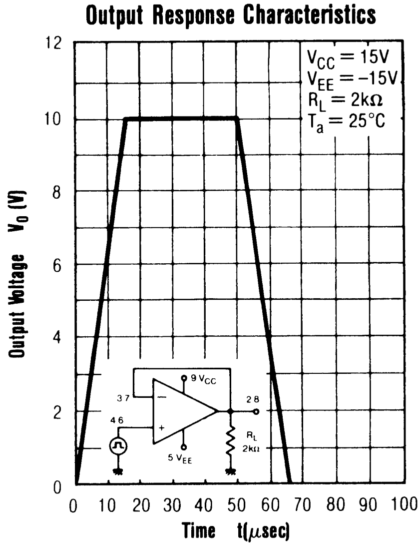


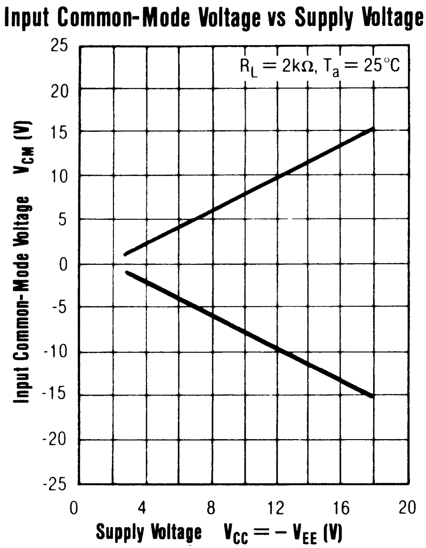


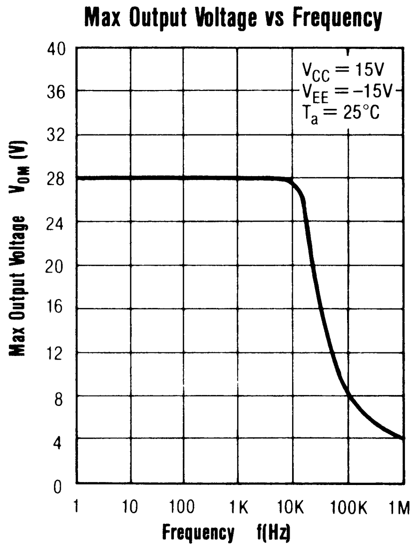


Typical Electrical Performance Curves (continued)

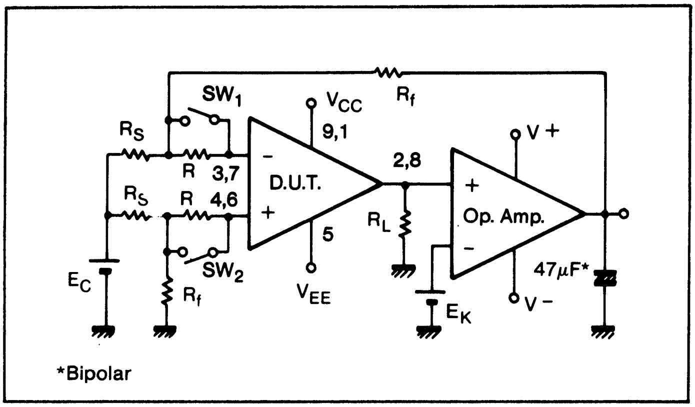




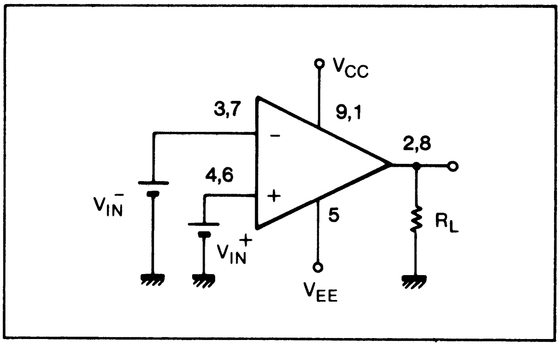




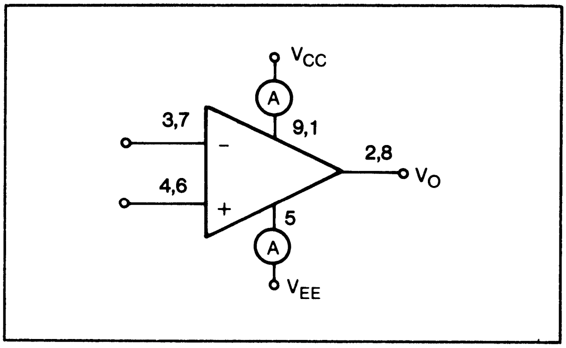
Test Circuit 1 (½ circuit)



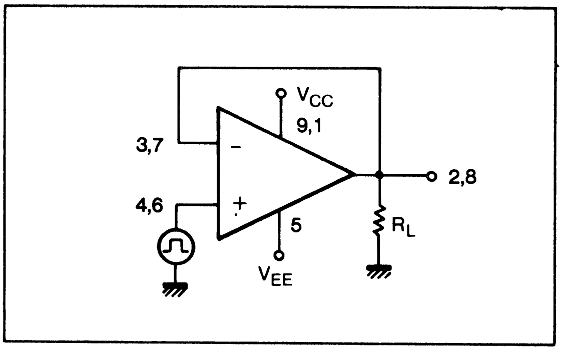
Test Circuit 2 (½ circuit)



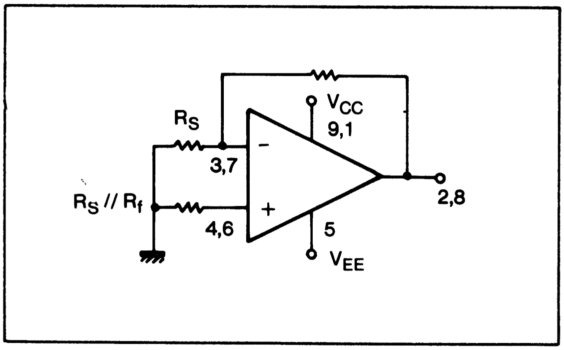
Test Circuit 3 (½ circuit)



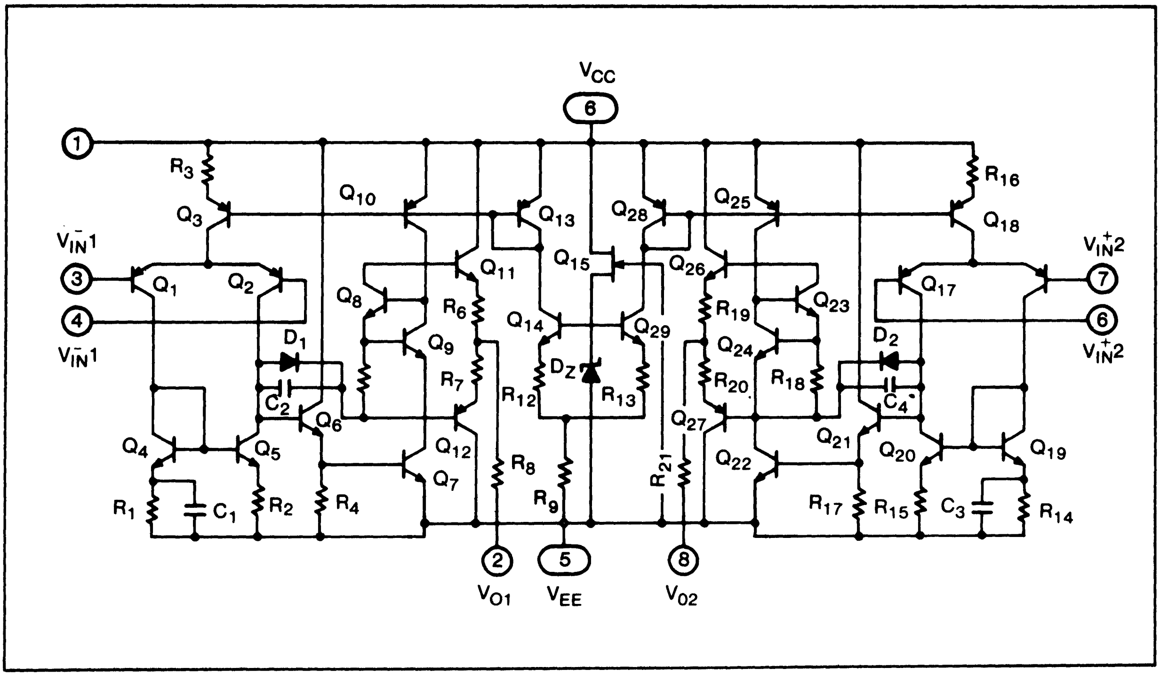
Test Circuit 4 (½ circuit)



Test Circuit 5 (½ circuit)



Schematic Diagram

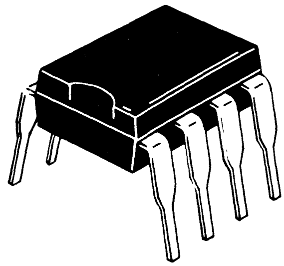


AN6553/AN6553S DUAL OPERATIONAL AMPLIFIERS

General Description

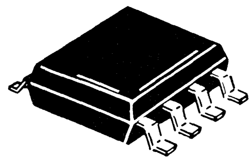
The AN6553 is a dual operational amplifier which has internal phase compensation. It is designed to be a general purpose circuit.

AN6553



8 - DIP PACKAGE

AN6553S



SO - 8D PACKAGE

Features

- Internal phase compensation
- High gain, low noise
- Output short protection circuit
- Slew rate: 1.0V/μ typ.
- Available in an 8 - pin DIP or 8 - pin S.O. plastic packages

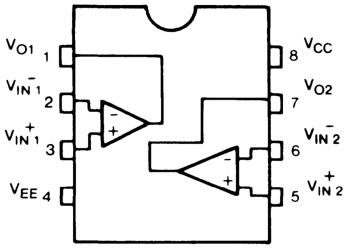
Absolute Maximum Ratings ($T_a = 25°C$)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	± 18	V
Power Dissipation	(8 DIP)	P_D	500	mW
	(8 SO)	P_D	360	mW
Input Differential Voltage		V_{ID}	± 30	V
Input Common –Mode Voltage		V_{ICM}	± 15	V
Operating Temperature		Topr	– 20 to + 75	°C
Storage Temperature	(8 DIP)	Tstg	– 55 to + 150	°C
	(8 SO)	Tstg	– 55 to + 125	°C

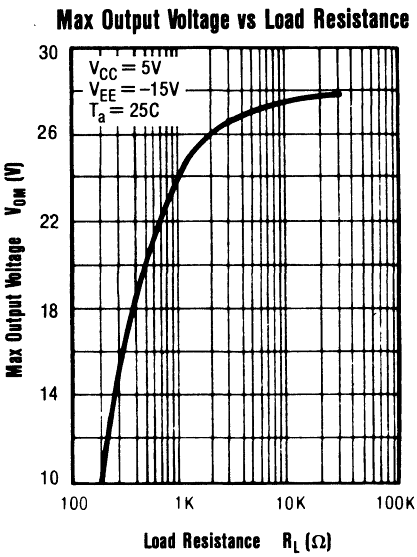
Electrical Characteristics ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25°C$)

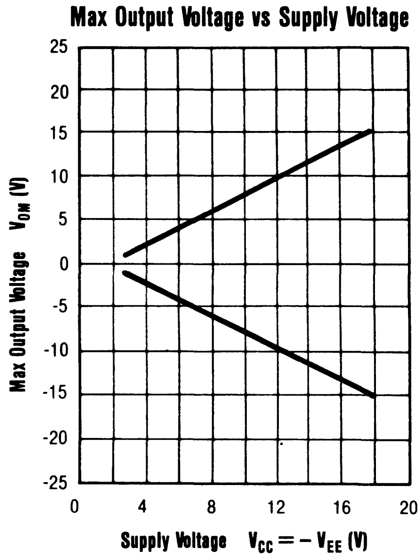
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_B	1				500	nA
Voltage Gain	G_V	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	100		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±14		V
Common-Mode Rejection Ratio	CMRR	1		70	90		dB
Supply Voltage Rejection Ratio	PSRR	1			30	150	μV/V
Power Consumption	P_C	4	$R_L = \infty$		90	170	mW
Slew Rate	SR	5	$R_L = \geq 2k\Omega$		2.0		V/μs
Equivalent Input Noise Voltage	V_n	60	$R_S = 1k\Omega$, B: 10Hz to 30kHz		2.5		μVrms

Connection Diagram

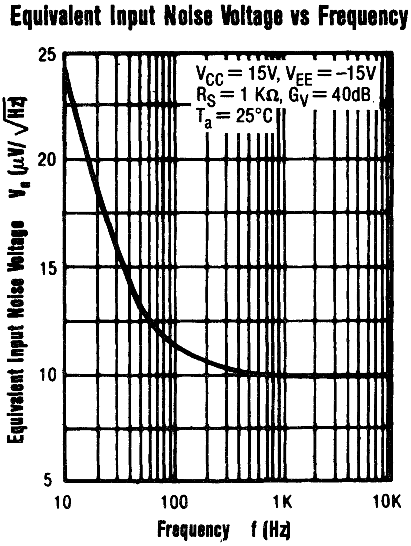


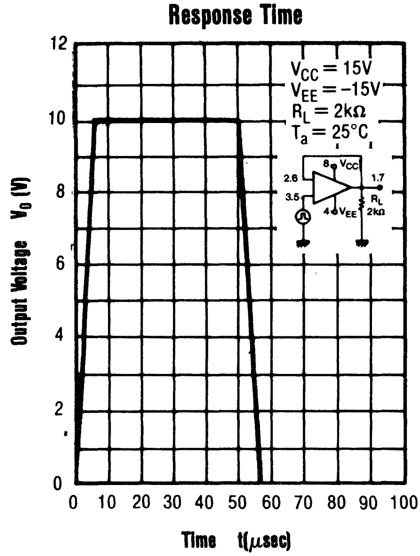
Typical Electrical Performance Curves

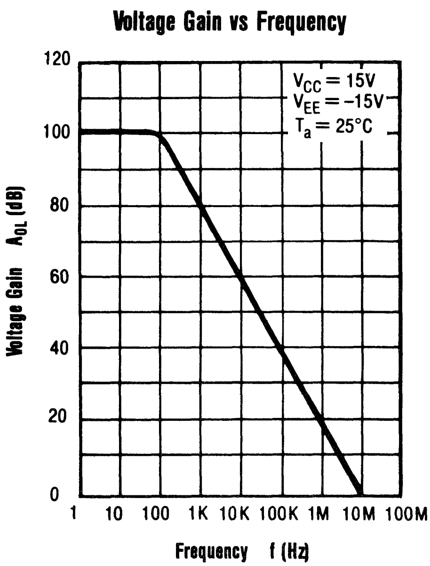


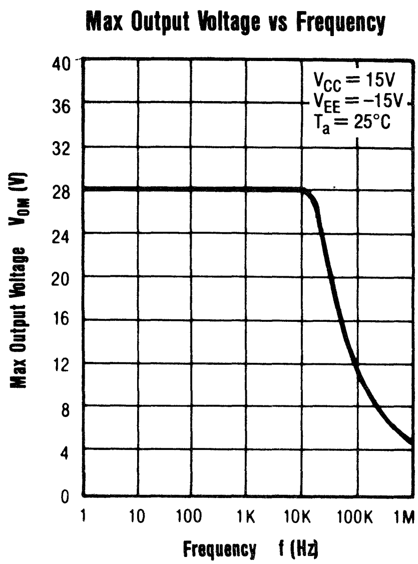


Typical Electrical Performance Curves (continued)

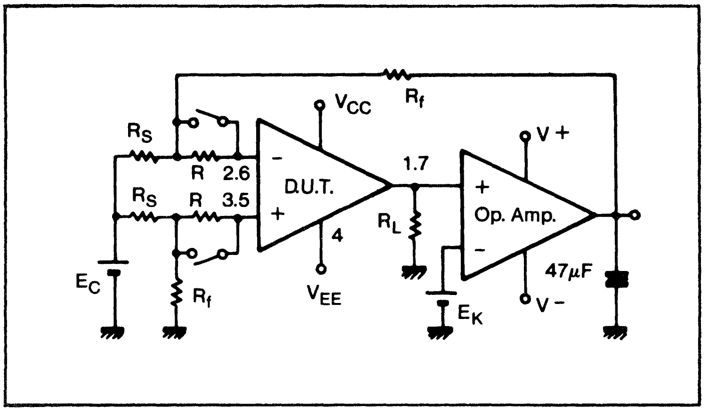




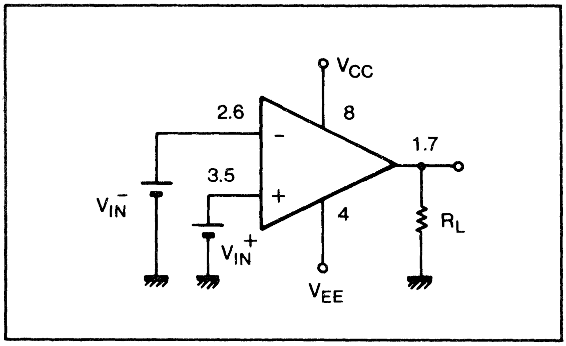




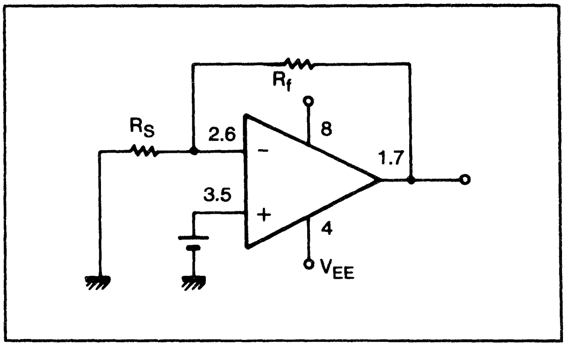
Test Circuit 1 (½ circuit)



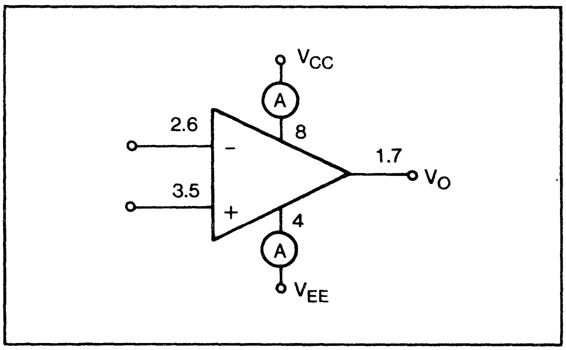
Test Circuit 2 (½ circuit)



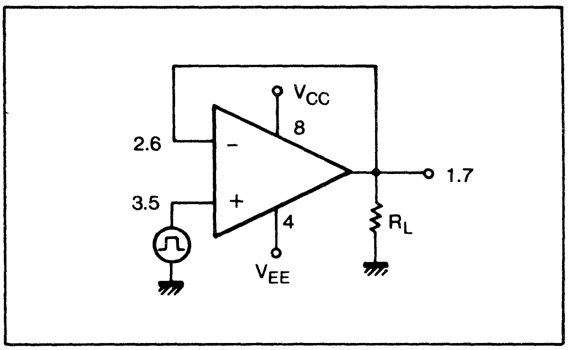
Test Circuit 3 (½ circuit)



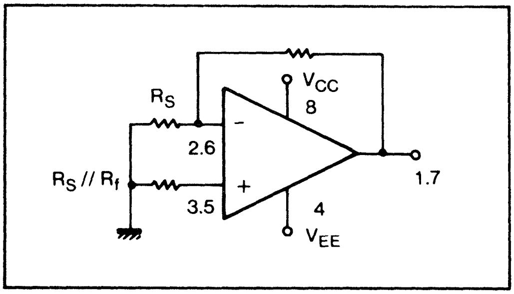
Test Circuit 4 (½ circuit)



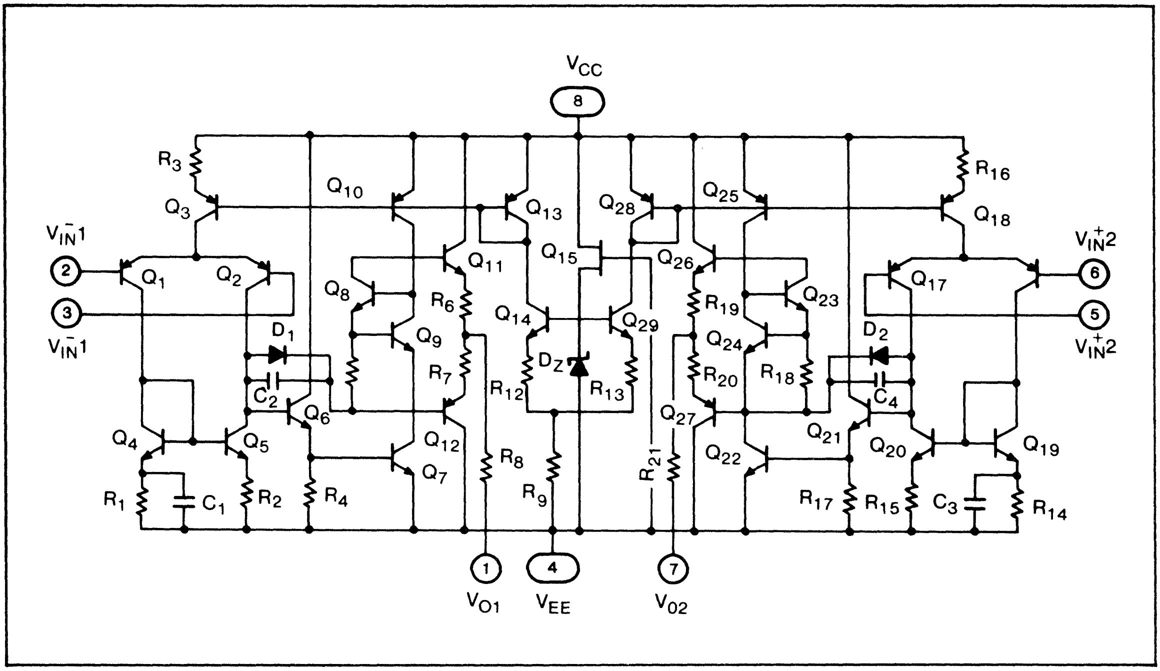
Test Circuit 5 (½ circuit)



Test Circuit 6 (½ circuit)



Schematic Diagram

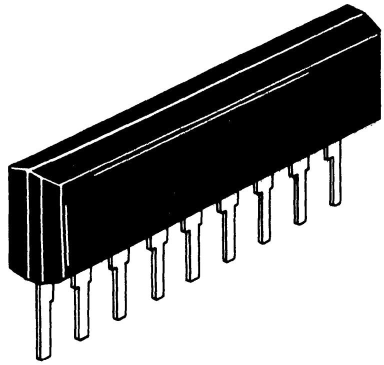


AN6555 DUAL OPERATIONAL AMPLIFIER

General Description

The AN6555 is a dual operational amplifier in a space-saving single-in-line package. It requires no external phase compensation and its low noise and high gain make the AN6555 suitable for many applications.

AN6555



9 - SIP PACKAGE

Features

- No frequency compensation required
- High gain, low noise
- Short circuit protection
- Dual operational amplifiers in a symmetrical 9 - pin SIP package

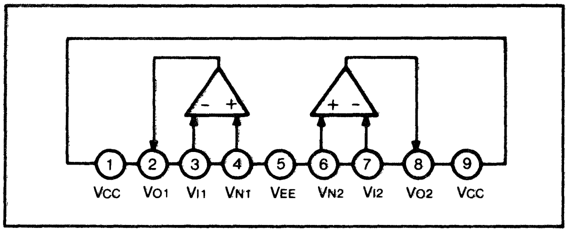
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	± 18	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	± 30	V
Input Common –Mode Voltage	V_{ICM}	± 15	V
Operating Temperature	Topr	– 20 to 75	°C
Storage Temperature	Tstg	– 55 to 150	°C

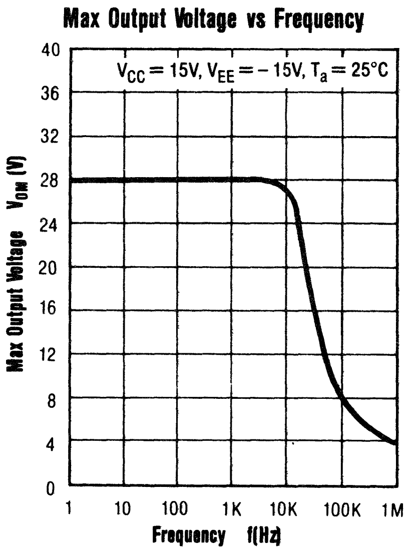
Electrical Characteristics ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25°C$)

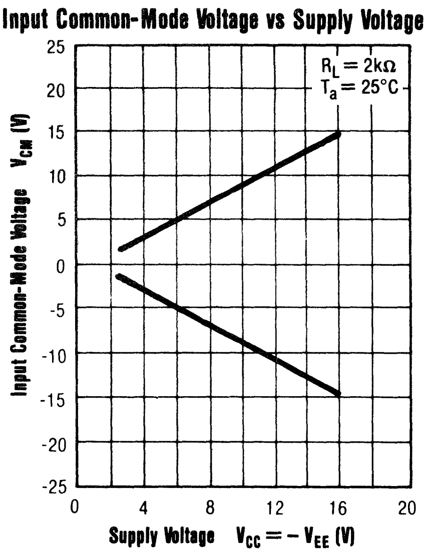
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_B	1				500	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	100		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±13		V
Common-Mode Rejection Ratio	CMRR	1		70	90		dB
Supply Voltage Rejection Ratio	PSRR	1			30	150	μV/V
Power Consumption	P_C	4			90	170	mW
Slew Rate	SR	5			1.8		V/μs
Equivalent Input Noise Voltage	V_n	6	$R_S = 1k\Omega$, DIN/AUDIO		1.5		μVrms

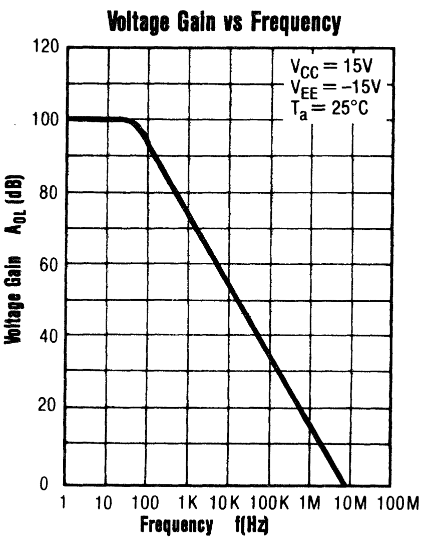
Connection Diagram

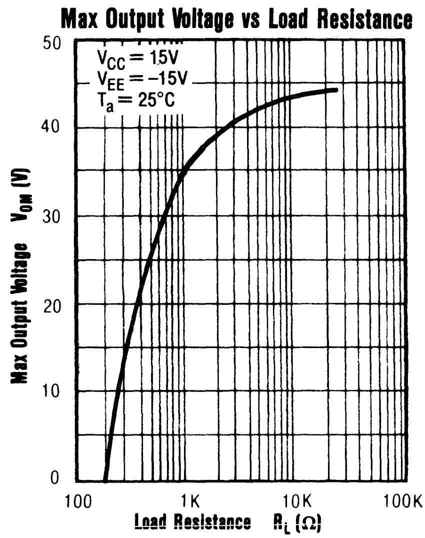


Typical Electrical Performance Curves



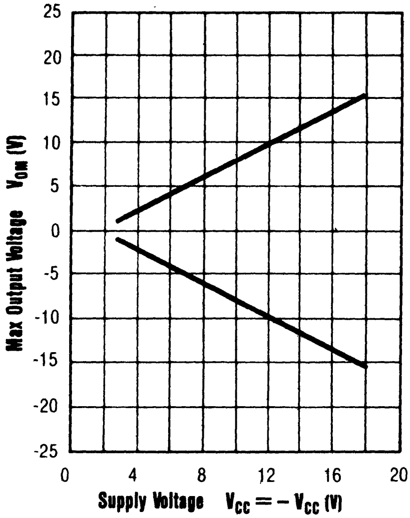




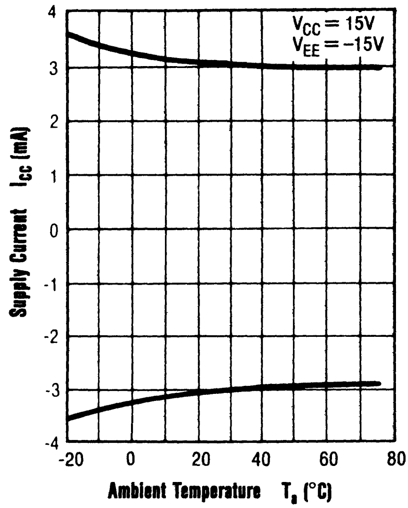


Typical Electrical Performance Curves (continued)

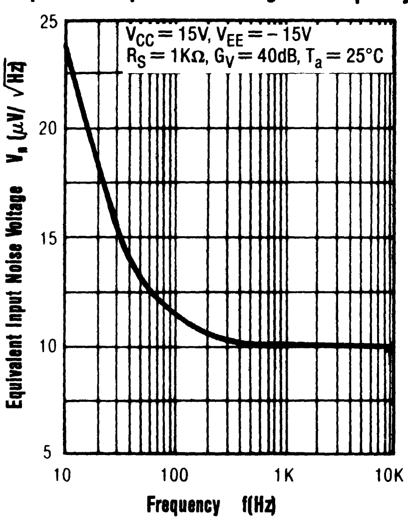
Max Output Voltage vs Supply Voltage



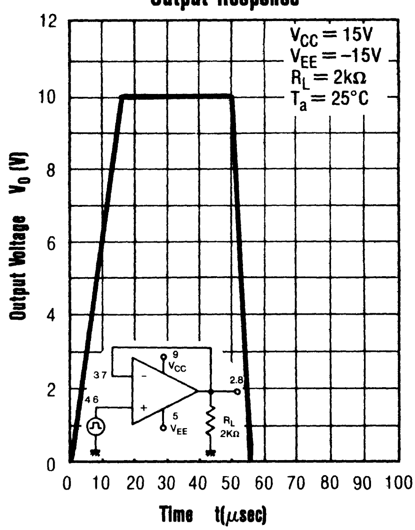
Supply Current vs Supply Voltage



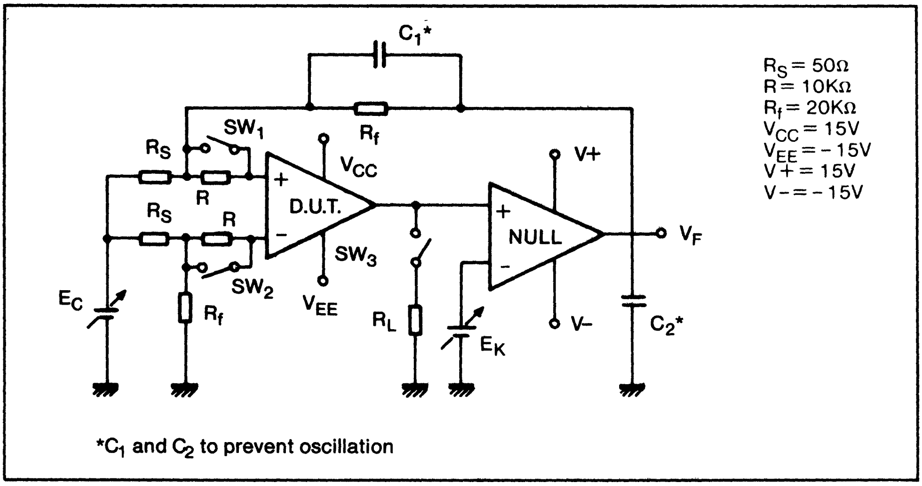
Equivalent Input Noise Voltage vs Frequency



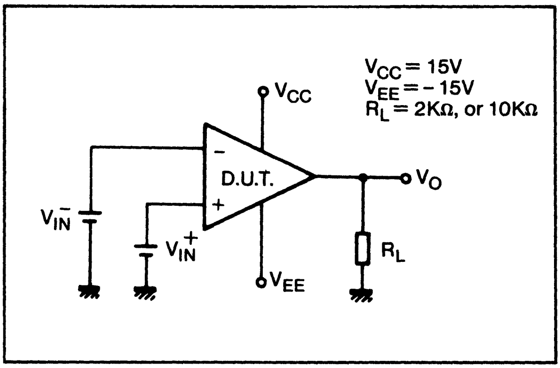
Output Response



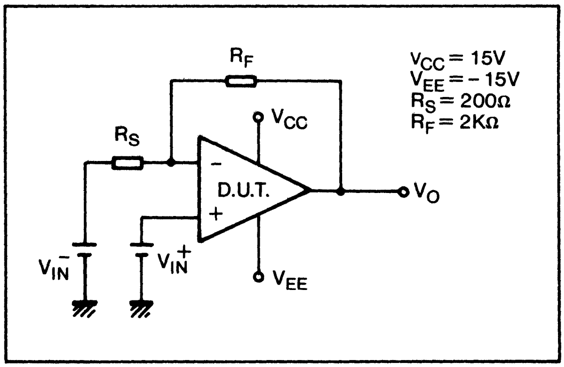
Test Circuit 1 (½ circuit)



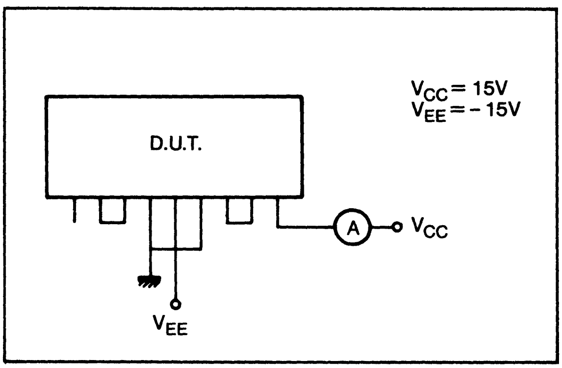
Test Circuit 2 (½ circuit)



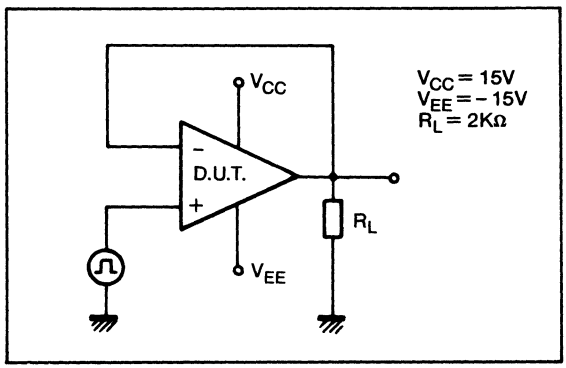
Test Circuit 3 (½ circuit)



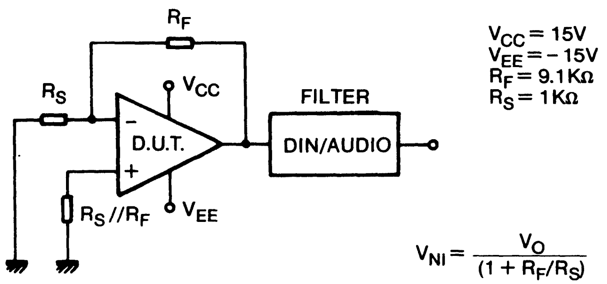
Test Circuit 4



Test Circuit 5 (½ circuit)



Test Circuit 6 (½ circuit)



$$V_{NI} = \frac{V_O}{(1 + R_F/R_S)}$$

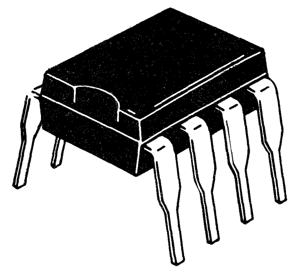
Item	Test conditions for Circuit 1
Input Offset Voltage	With SW1, SW2, and SW3 off, V_{FI} is measured on the basis of $E_C = E_K = 0$, where $V_{IO} = V_{F1}/400$ (V).
Input Offset Current	With SW1, SW2 on and SW3 off, V_{F2} is measured on the basis of $E_C = E_K = 0$, where $I_{IO} = \lvert V_{F2} - V_{F1} \rvert / 4 \times 10^6$ (A).
Input Bias Current	With SW3 off while $E_C = E_K = 0$ and SW1, on, SW2, off, V_{F3} is measured. V_{F4} is measured with SW1 and SW2 inverse. Where $I_B = \lvert V_{F3} - V_{F4} \rvert / 8 \times 10^6$ (A).
Voltage Gain	With SW1, SW2 and SW3 on and $E_C = 0$, $E_K = 10V$, V_{F5} is measured and V_{F5} is measured again with $E_K = -10V$. Where $A_{OL} = 20 \log \left(\frac{8000}{V_{F5} - V_{F5}} \right)$
Common-Mode Rejection Ratio	With SW1 and SW2 on, SW3 off, and $E_K = 0$, $E_C = 5V$, V_{F6} is measured. With $E_C = -5V$, V_{F6} is measured again. Where: $CMRR = \left(\frac{4000}{V_{F6} - V_{F6}} \right)$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on, SW3 off, $E_K = E_C = 0$, $V_{CC} = 10V$, V_{F7} is measured. Where: PSRR (+) = $\lvert V_{F7} - V_{F2} \rvert / 2 \times 10^3$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on SW3, off and $E_K = E_C = 0$ $V_{EE} = -10V$, V_{F8} is measured, Where: PSRR (−) = $\lvert V_{F8} - V_{F2} \rvert$ 2 x 10^3

AN6556/AN6556S DUAL OPERATIONAL AMPLIFIER

General Description

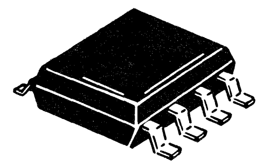
The AN6556 is a dual operational amplifier. It requires no external phase compensation and its low noise and high gain make the AN6556 suitable for many applications.

AN6556



8-DIP PACKAGE

AN6556S



SO-8D PACKAGE

Features

- No frequency compensation required
- High gain, low noise
- Short circuit protection
- Dual operationsl amplifiers in a 8-pin DIP or S.O. package

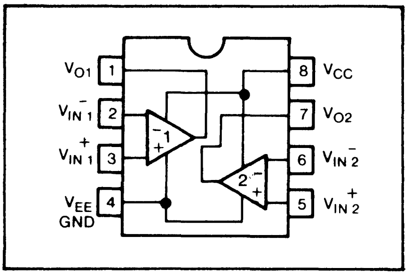
Absolute Maximum Ratings ($T_a = 25°C$)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}	±18	V
Power Dissipation	(8 DIP)	P_D	500	mW
	(8 SO)	P_D	360	mW
Input Differential Voltage		V_{ID}	±30	V
Input Common-Mode Voltage		V_{ICM}	±15	V
Operating Temperature		T_{opr}	−20 to +75	°C
Storage Temperature	(8 DIP)	T_{stg}	−55 to +150	°C
	(8 SO)	T_{stg}	−55 to +125	°C

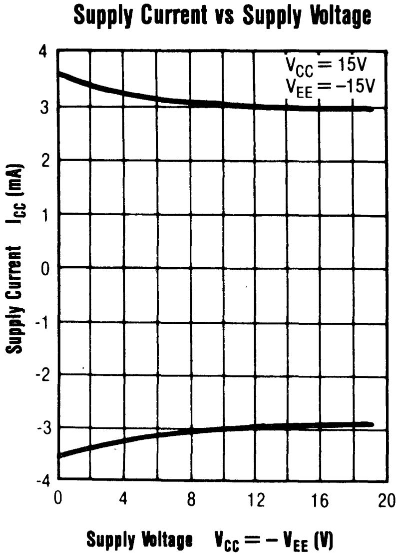
Electrical Characteristics ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25°C$)

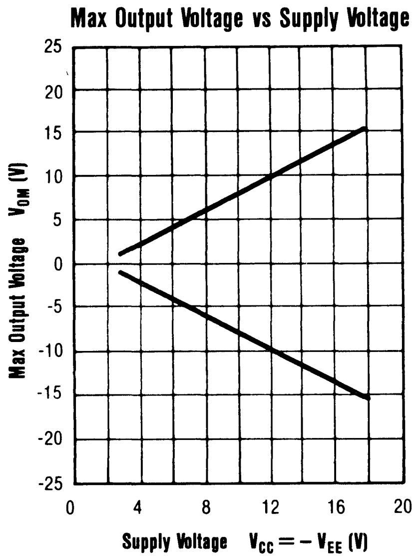
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	6	mV
Input Offset Current	I_{IO}	1			5	200	nA
Input Bias Current	I_B	1				500	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	100		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±13		V
Common-Mode Rejection Ratio	CMRR	1		70	90		dB
Supply Voltage Rejection Ratio	PSRR	1			30	150	μV/V
Power Consumption	P_C	4			90	170	mW
Slew Rate	SR	5			2.0		V/μs
Equivalent Input Noise Voltage	V_n	6	$R_S = 1k\Omega$, DIN/AUDIO		1.5		μVrms

Connection Diagram



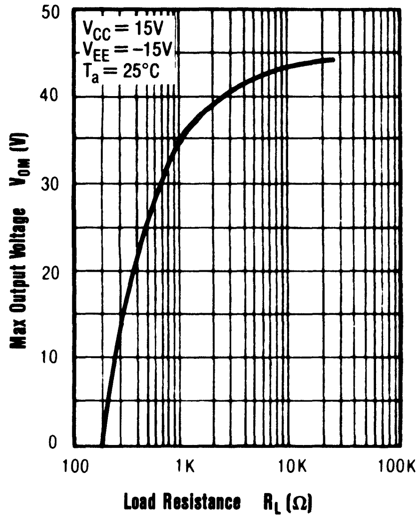
Typical Electrical Performance Curves



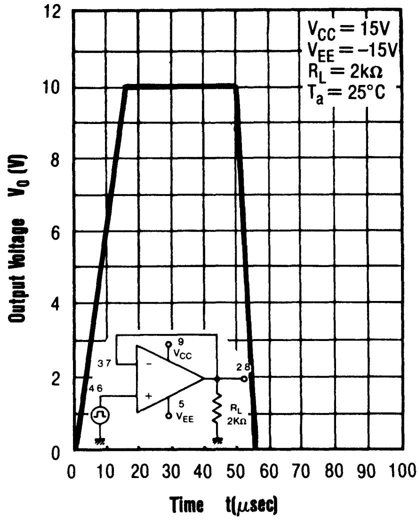


Typical Electrical Performance Curves (continued)

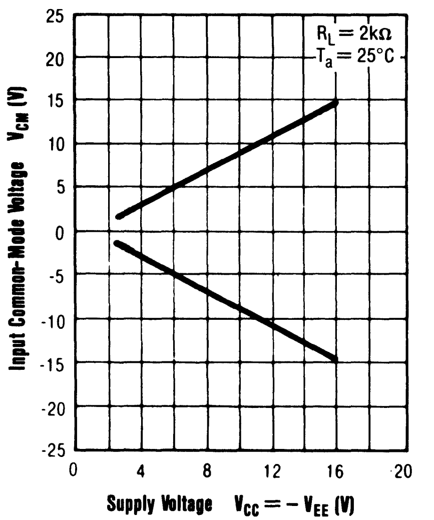
Max Output Voltage vs Load Resistance



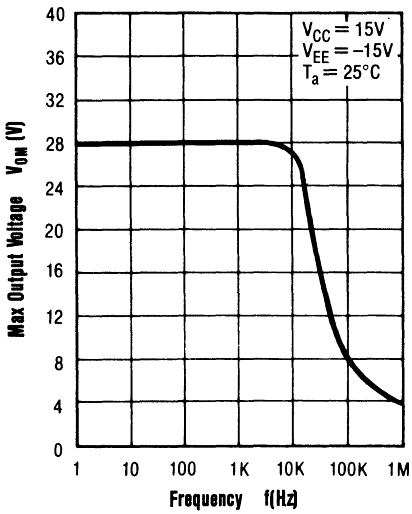
Output Response



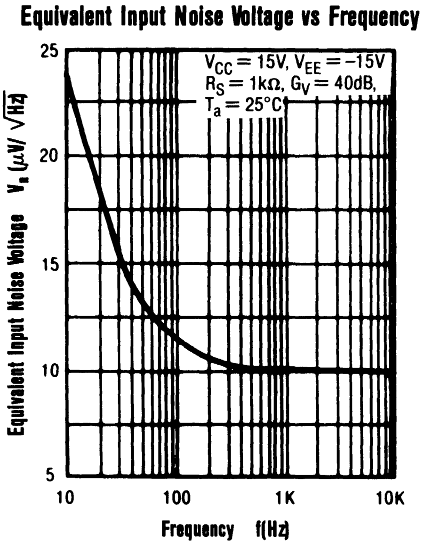
Input Common-Mode Voltage vs Supply Voltage

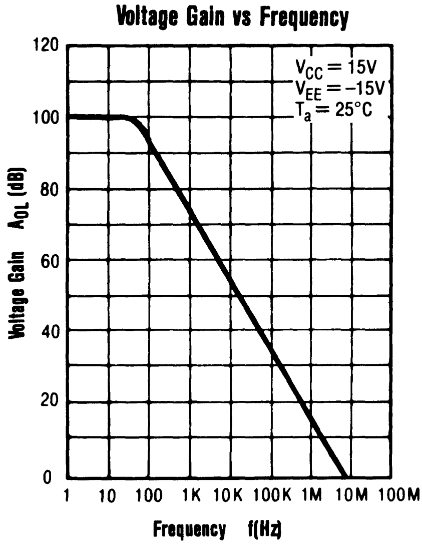


Max Output Voltage vs Frequency

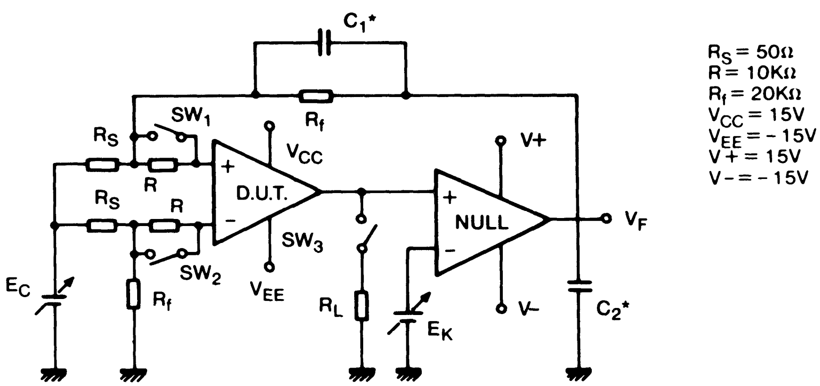


Typical Electrical Performance Curves (continued)



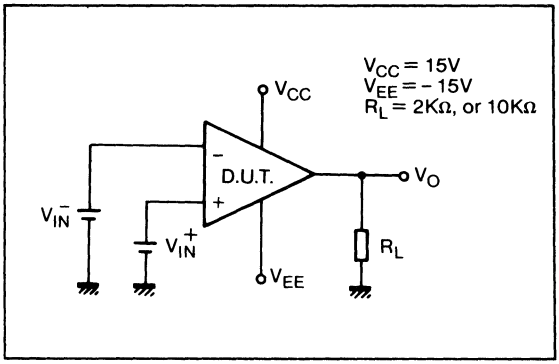


Test Circuit 1 (½ circuit)

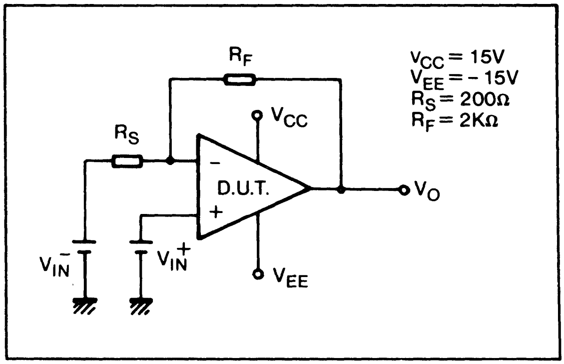


*C_1 and C_2 to prevent oscillation

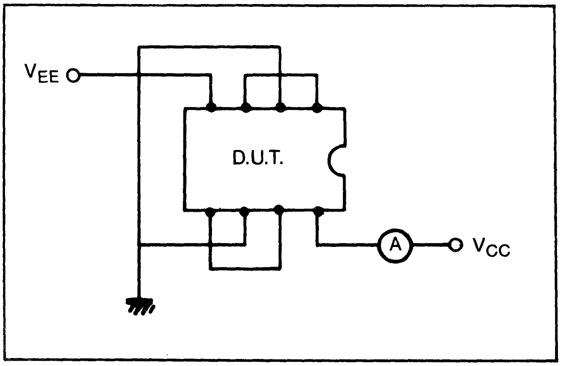
Test Circuit 2 (½ circuit)



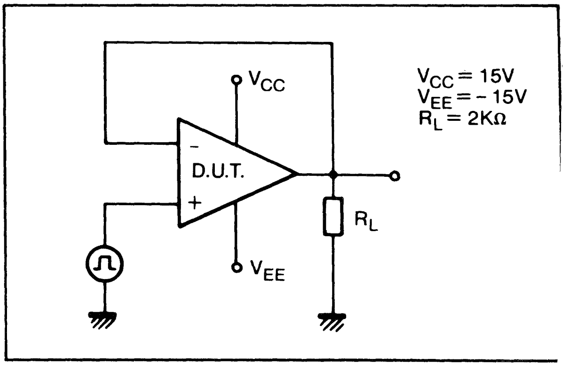
Test Circuit 3 (½ circuit)



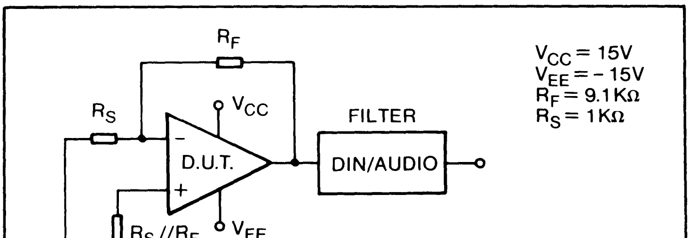
Test Circuit 4



Test Circuit 5 (½ circuit)



Test Circuit 6 (½ circuit)



$$V_{NI} = \frac{V_O}{(1 + R_F/R_S)}$$

Item	Test conditions for Circuit 1
Input Offset Voltage	With SW1, SW2, and SW3 off, V_{FI} is measured on the basis of $E_C = E_K = 0$, where $V_{IO} = V_{F1}/400$ (V).
Input Offset Current	With SW1, SW2 on and SW3 off, V_{F2} is measured on the basis of $E_C = E_K = 0$, where $I_{IO} = \mid V_{F2} - V_{F1} \mid /4 \times 10^6$ (A).
Input Bias Current	With SW3 off while $E_C = E_K = 0$ and SW1, on, SW2, off, V_{F3} is measured. V_{F4} is measured with SW1 and SW2 inverse. Where $I_B = \mid V_{F3} - V_{F4} \mid /8 \times 10^6$ (A).
Voltage Gain	With SW1, SW2 and SW3 on and $E_C = 0$, $E_K = 10V$, V_{F5} is measured and V_{F5} is measured again with $E_K = -10V$. Where $A_{OL} = 20 \log \left(\frac{8000}{V_{F5} - V_{F5}} \right)$
Common-Mode Rejection Ratio	With SW1 and SW2 on, SW3 off, and $E_K = 0$, $E_C = 5V$, V_{F6} is measured. With $E_C = -5V$, V_{F6} is measured again. Where: $CMRR = \left(\frac{4000}{V_{F6} - V_{F6}} \right)$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on, SW3 off, $E_K = E_C = 0$, $V_{CC} = 10V$, V_{F7} is measured. Where: $PSRR(+) = \mid V_{F7} - V_{F2} \mid /2 \times 10^3$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on SW3, off and $E_K = E_C = 0$ $V_{EE} = -10V$, V_{F8} is measured, Where: $PSRR(-) = \mid V_{F8} - V_{F2} \mid \ 2 \times 10^3$

AN6557 DUAL OPERATIONAL AMPLIFIER

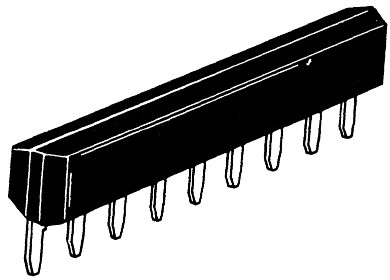
General Description

The AN6557 is a dual operational amplifier with high gain, high slew rate and low noise characteristics.

Features

- Low noise
- High slew rate: 6.0V V/μ typ.
- Low profile, single-in-line package for compact layouts
- Low offset voltage

AN6557



9 – SIP PACKAGE (Low Profile)

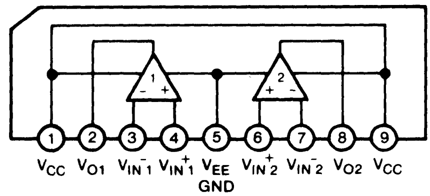
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	± 18	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	± 30	V
Input Common –Mode Voltage	V_{ICM}	± 15	V
Operating Temperature	Topr	– 20 to 75	°C
Storage Temperature	Tstg	– 55 to 150	°C

Electrical Characteristics ($V_{CC} = -V_{EE} = 15V$, $T_a = 25°C$)

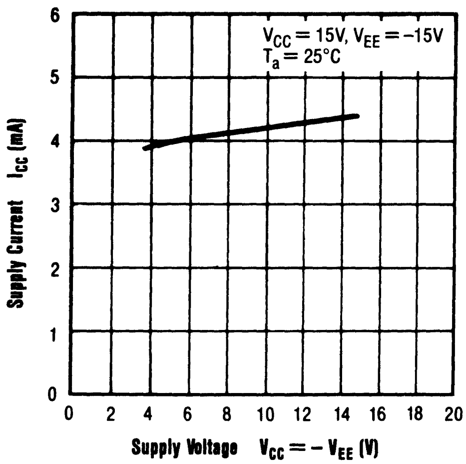
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.3	3	mV
Input Offset Current	I_{IO}	1			10	200	nA
Input Bias Current	I_B	1			1300	2000	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	100		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$I_O = 25mA$	±10	±12		V
Common-Mode Input Voltage	V_{CM}	3		±12	±14		V
Common-Mode Rejection Ratio	CMRR	1		70	100		dB
Supply Voltage Rejection Ratio	PSRR	1			10	150	μV/V
Power Consumption	P_C	4	$R_L = \infty$		150	240	mW
Slew Rate	SR	5	$R_L \geq 1k\Omega$		6		V/μs
Equivalent Input Noise Voltage	V_n	6	$R_S = 1k\Omega$, DIN/AUDIO		0.9		μVrms

Connection Diagram

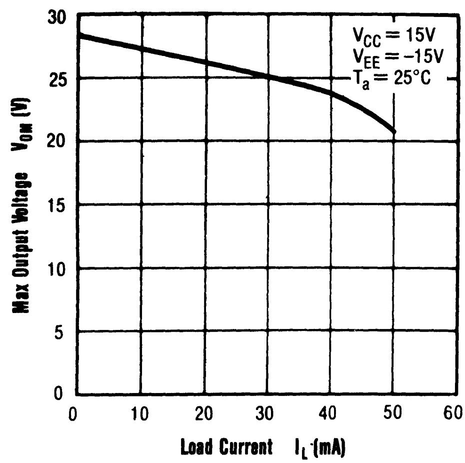


Typical Electrical Performance Curves

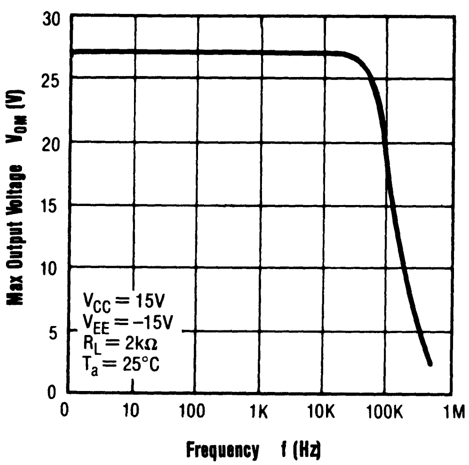
Supply Current vs Supply Voltage



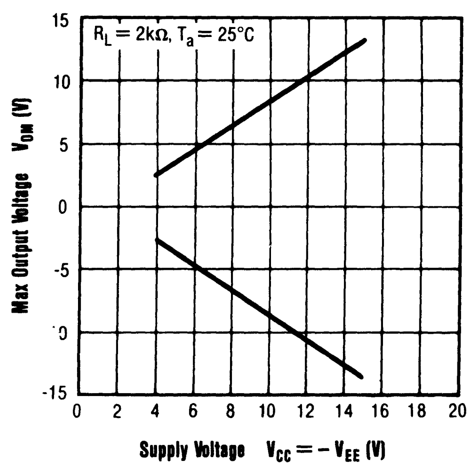
Max Output Voltage vs Load Current



Max Output Voltage vs Frequency

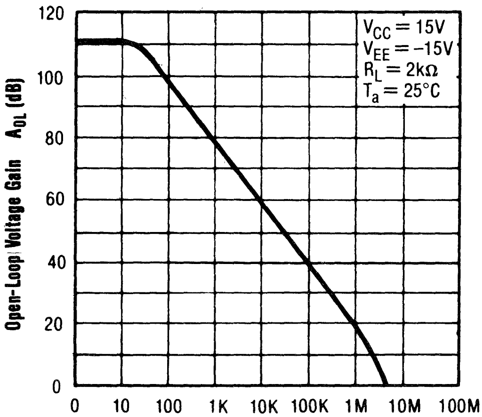


Max Output Voltage vs Supply Voltage

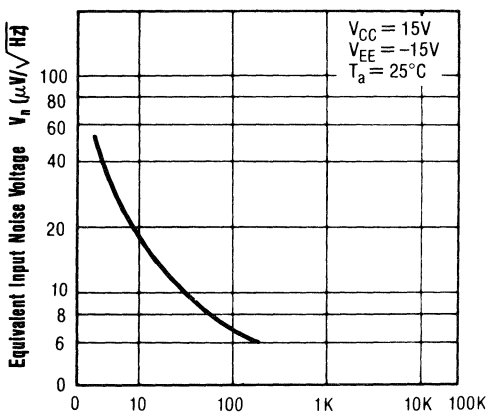


Typical Electrical Performance Curves (continued)

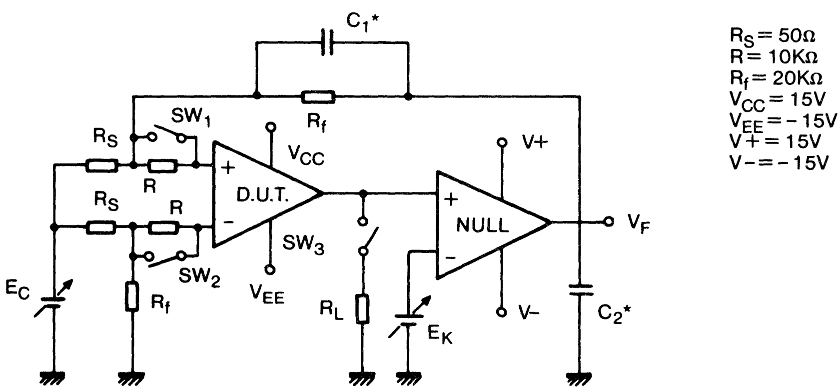
Voltage Gain vs Frequency



Equivalent Input Noise Voltage vs Frequency

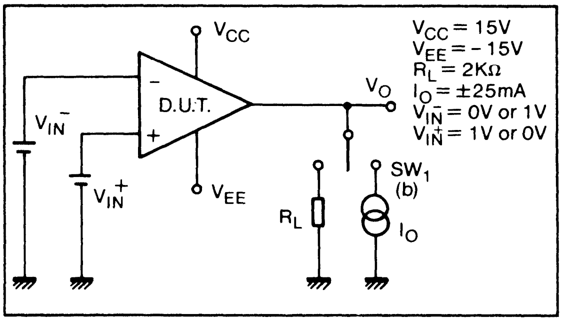


Test Circuit 1 (½ circuit)

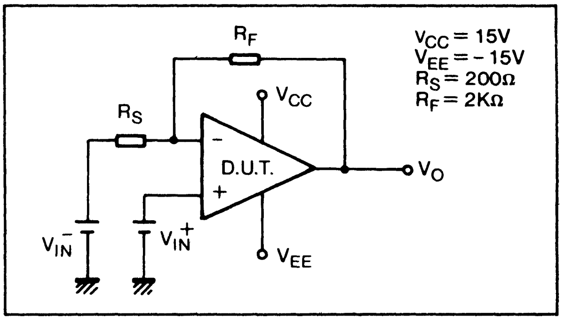


*C_1 and C_2 to prevent oscillation

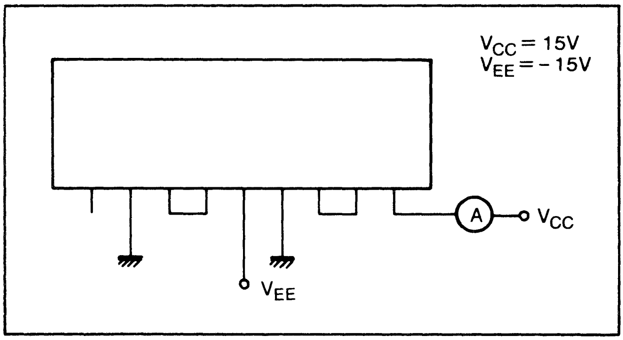
Test Circuit 2 (½ circuit)



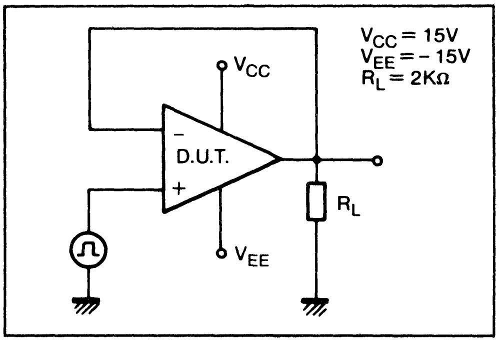
Test Circuit 3 (½ circuit)



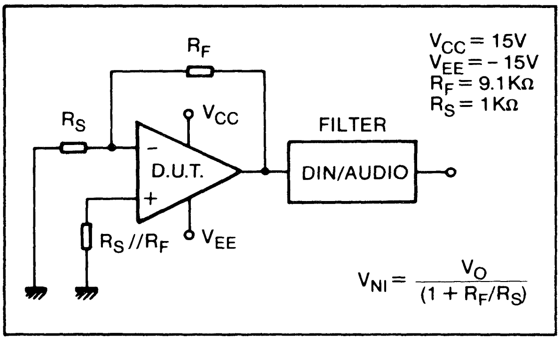
Test Circuit 4



Test Circuit 5 (½ circuit)



Test Circuit 6 (½ circuit)



Item	Test conditions for Circuit 1
Input Offset Voltage	With SW1, SW2, and SW3 off, V_{FI} is measured on the basis of $E_C = E_K = 0$, where $V_{IO} = V_{F1}/400$ (V).
Input Offset Current	With SW1, SW2 on and SW3 off, V_{F2} is measured on the basis of $E_C = E_K = 0$, where $I_{IO} = \|V_{F2} - V_{F1}\| / 4 \times 10^6$ (A).
Input Bias Current	With SW3 off while $E_C = E_K = 0$ and SW1, on, SW2, off, V_{F3} is measured. V_{F4} is measured with SW1 and SW2 inverse. Where $I_B = \|V_{F3} - V_{F4}\| / 8 \times 10^6$ (A).
Voltage Gain	With SW1, SW2 and SW3 on and $E_C = 0$, $E_K = 10V$, V_{F5} is measured and V_{F5} is measured again with $E_K = -10V$. Where $A_{OL} = 20 \log \left(\frac{8000}{V_{F5} - V_{F5}} \right)$
Common-Mode Rejection Ratio	With SW1 and SW2 on, SW3 off, and $E_K = 0$, $E_C = 5V$, V_{F6} is measured. With $E_C = -5V$, V_{F6} is measured again. Where: $CMRR = \left(\frac{4000}{V_{F6} - V_{F6}} \right)$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on, SW3 off, $E_K = E_C = 0$, $V_{CC} = 10V$, V_{F7} is measured. Where: $PSRR (+) = \|V_{F7} - V_{F2}\| / 2 \times 10^3$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on SW3, off and $E_K = E_C = 0$ $V_{EE} = -10V$, V_{F8} is measured, Where: $PSRR (-) = \|V_{F8} - V_{F2}\|$ 2×10^3

AN6558 DUAL OPERATIONAL AMPLIFIER

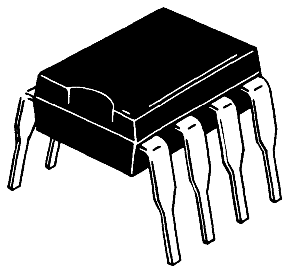
General Description

The AN6558 is a dual operational amplifier with high gain, high slew rate and low noise characteristics.

Features

- No frequency compensation required
- High gain, low noise
- 8 - pin DIP plastic package
- High slew rate: 6.0V V/μ typ.

AN6558



8 - DIP PACKAGE

Absolute Maximum Ratings ($T_a = 25°C$)

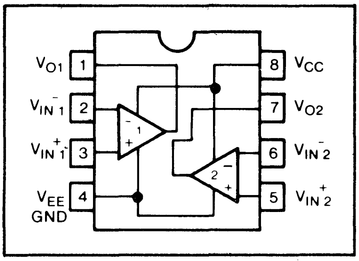
Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	± 18	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	± 30	V
Input Common –Mode Voltage	V_{ICM}	± 15	V
Operating Temperature	Topr	– 20 to 75	°C
Storage Temperature	Tstg	- 55 to 150	°C

Electrical Characteristics ($V_{CC} = 15V$, $V_{EE} = -15V$, $T_a = 25°C$)

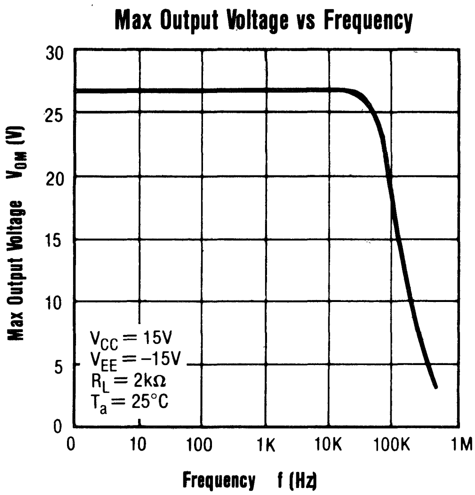
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.3	3	mV
Input Offset Current	I_{IO}	1			10	200	nA
Input Bias Current	I_B	1			1300	2000	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm10V$	86	100		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$I_O = 25mA$	±10	±12		V
Common-Mode Input Voltage	V_{CM}	3		±12	±14		V
Common-Mode Rejection Ratio	CMRR	1		70	100		dB
Supply Voltage Rejection Ratio	PSRR	1			10	150	μV/V
Power Consumption	P_C	4	$R_L = \infty$		150	240	mW
Slew Rate	SR	5	$R_L \geq 2k\Omega$		6		V/μs
Equivalent Input Noise Voltage	V_n	6	$R_S = 1k\Omega$, DIN/AUDIO		0.9		μVrms

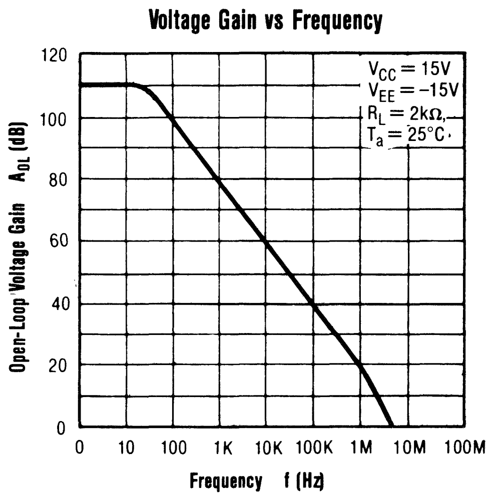
Note: Operate with more than 20dB gain.

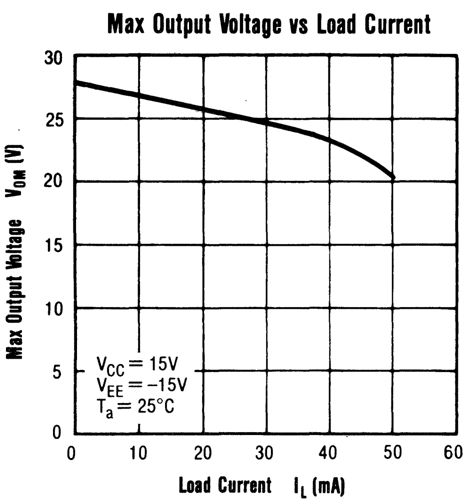
Connection Diagram

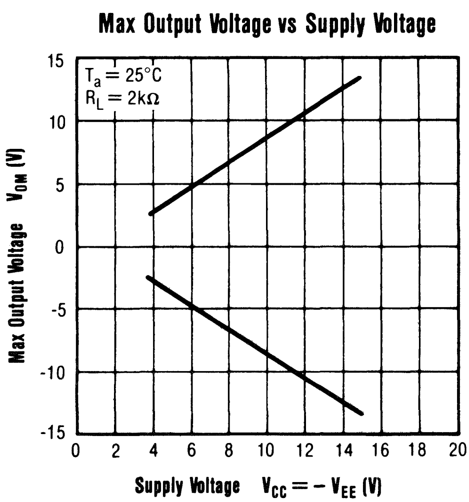


Typical Electrical Performance Curves



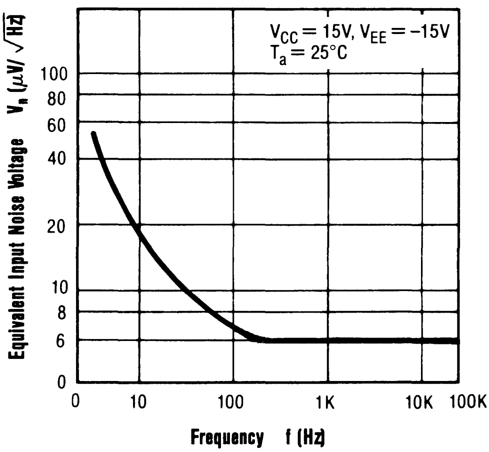




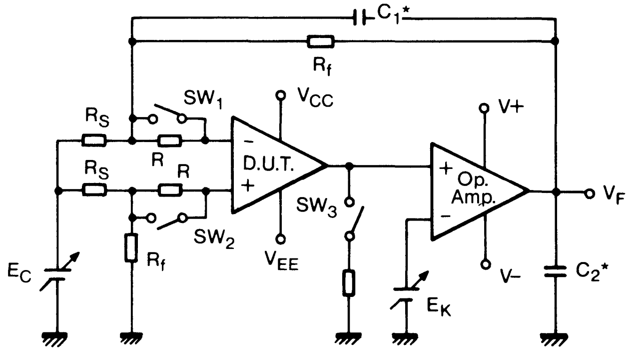


Typical Electrical Performance Curves (continued)

Equivalent Input Noise Voltage vs Frequency



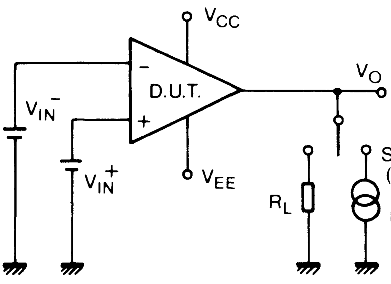
Test Circuit 1 (½ circuit)



*C_1 and C_2 to prevent oscillation

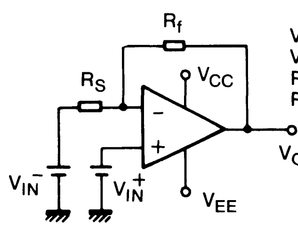
R_S = 50Ω
R = 10KΩ
R_f = 20KΩ
V_{CC} = 15V
V_{EE} = − 15V
V+ = 15V
V− = − 15V

Test Circuit 2 (½ circuit)



V_{CC} = 15V
V_{EE} = − 15V
R_L = 2KΩ
I_O = ±25mA
V_{IN}^- = 0V or 1V
V_{IN}^+ = 1V or 0V

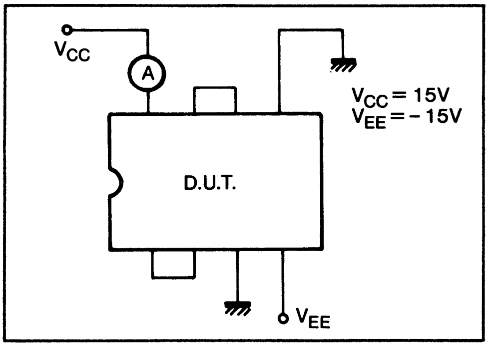
Test Circuit 3 (½ circuit)



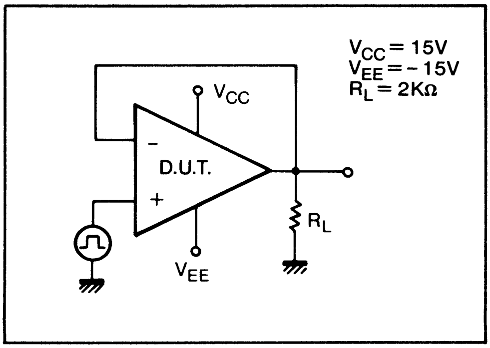
V_{CC} = 15V
V_{EE} = − 15V
R_S = 200Ω
R_f = 2KΩ

Apply $\|V_{IN}\|$ > 12V voltage and make sure that it is $V_O = V_{IN}^+ + \frac{R_f}{R_S}(V_{IN}^+ - V_{IN}^-)$

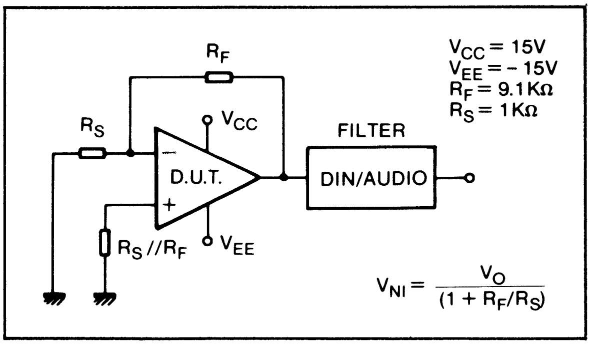
Test Circuit 4 (½ circuit)



Test Circuit 5 (½ circuit)

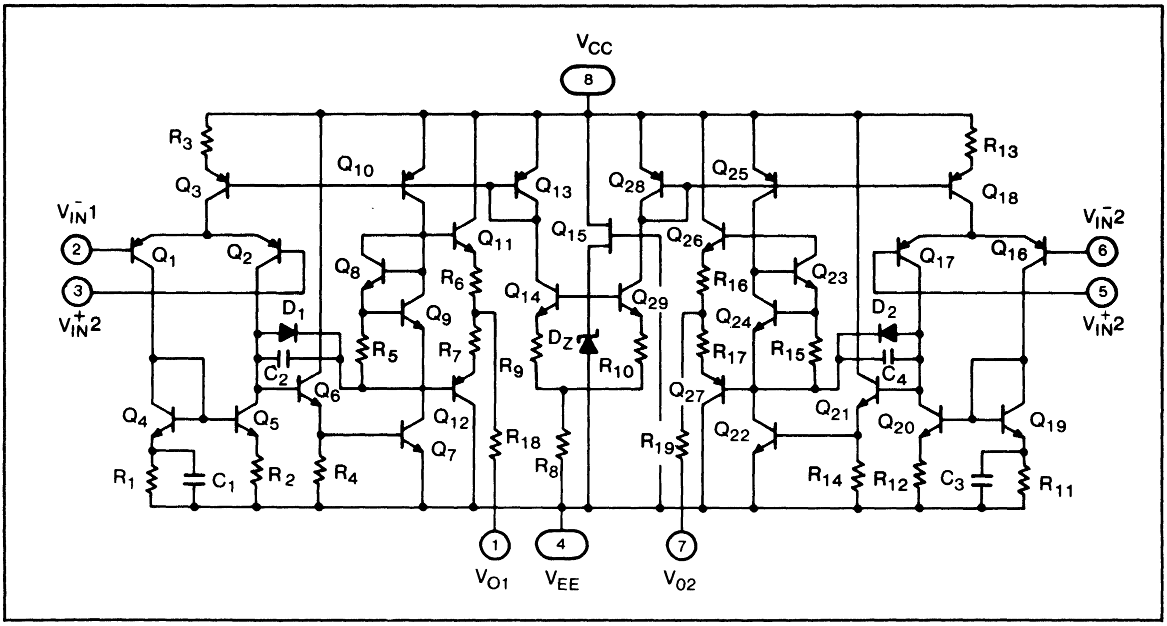


Test Circuit 6 (½ circuit)



Item	Test conditions for Circuit 1
Input Offset Voltage	With SW1, SW2, and SW3 off, V_{F1} is measured on the basis of $E_C = E_K = 0$, where $V_{IO} = V_{F1}/400$ (V).
Input Offset Current	With SW1, SW2 on and SW3 off, V_{F2} is measured on the basis of $E_C = E_K = 0$, where $I_{IO} = \lvert V_{F2} - V_{F1} \rvert / 4 \times 10^6$ (A).
Input Bias Current	With SW3 off while $E_C = E_K = 0$ and SW1, on, SW2, off, V_{F3} is measured. V_{F4} is measured with SW1 and SW2 inverse. Where $I_B = \lvert V_{F3} - V_{F4} \rvert / 8 \times 10^6$ (A).
Voltage Gain	With SW1, SW2 and SW3 on and $E_C = 0$, $E_K = 10V$, V_{F5} is measured and V_{F5} is measured again with $E_K = -10V$. Where $A_{OL} = 20 \log \left(\frac{8000}{V_{F5} - V_{F5}} \right)$
Common-Mode Rejection Ratio	With SW1 and SW2 on, SW3 off, and $E_K = 0$, $E_C = 5V$, V_{F6} is measured. With $E_C = -5V$, V_{F6} is measured again. Where: $CMRR = \left(\frac{4000}{V_{F6} - V_{F6}} \right)$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on, SW3 off, $E_K = E_C = 0$, $V_{CC} = 10V$, V_{F7} is measured. Where: $PSRR(+) = \lvert V_{F7} - V_{F2} \rvert / 2 \times 10^3$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on SW3, off and $E_K = E_C = 0$ $V_{EE} = -10V$, V_{F8} is measured, Where: $PSRR(-) = \lvert V_{F8} - V_{F2} \rvert$ 2×10^3

Schematic Diagram

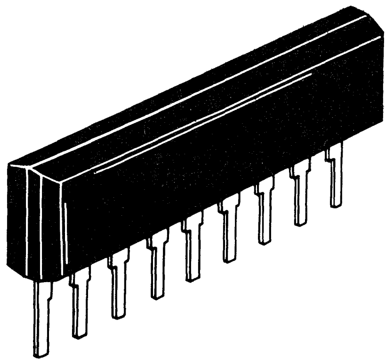


AN6561 DUAL OPERATIONAL AMPLIFIER

General Description

The AN6561 consists of two independent, high gain internally frequency compensated operational amplifiers which were designed to operate from a single power supply over a wide range of voltage

AN6561



9 - SIP PACKAGE

Features

- Internally frequency compensated for unity gain
- Large output voltage swing: 0V to V_{CC} - 1.5V
- Wide power supply range:
  Single supply: 3 to 30V or
  Dual supplies: ± 1.5 to ± 15V

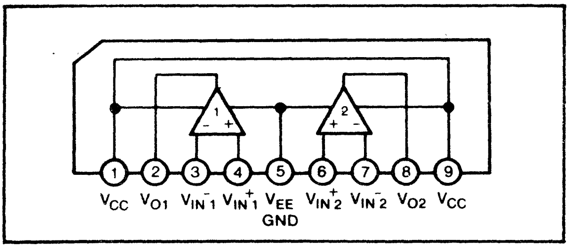
Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	32	V
Power Dissipation	P_D	350	mW
Input Differential Voltage	V_{ID}	32	V
Input Common –Mode Voltage	V_{ICM}	– 0.3 to 32	V
Operating Temperature	Topr	– 20 to 75	°C
Storage Temperature	Tstg	– 55 to ± 150	°C
Output Voltage	V_O	24	V

Electrical Characteristics (V_{CC} = 5V, T_a = 25°C)

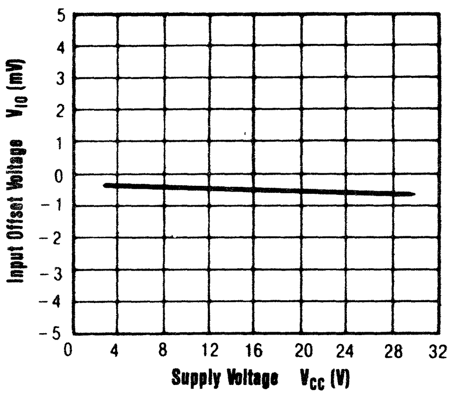
Item		Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage		V_{IO}	1	R_S = 50Ω		2	7	mV
Input Offset Current		I_{IO}	1				50	nA
Input Bias Current		I_B	1				250	nA
Voltage Gain		A_{OL}	1	R_L = 2kΩ	88	100		dB
Output Current	(Sink)	$I_{O (SINK)}$	7	V_{IN} = 0V, V_{IN} = 1V	10	20		mA
	(Source)	$I_{O (SOURCE)}$	6	V_{IN} = 1V, V_{IN} = 0V	20	40		mA
Maximum Output Voltage		V_{OM}	4	R_L = 2kΩ	Vcc – 1.5			V
Common-Mode Rejection Ratio		CMRR	1		65	85		dB
Supply Voltage Rejection Ratio		PSRR	1		65	100		dB
Supply Current (Source)		I_{CC}	3	R_L + ∞		0.6	1.2	mA
Common-Mode Input Voltage		V_{ICM}	2				Vcc – 1.5	V
Channel Separation		CS	5	f = 1kHz to 20kHz		120		dB

Connection Diagram

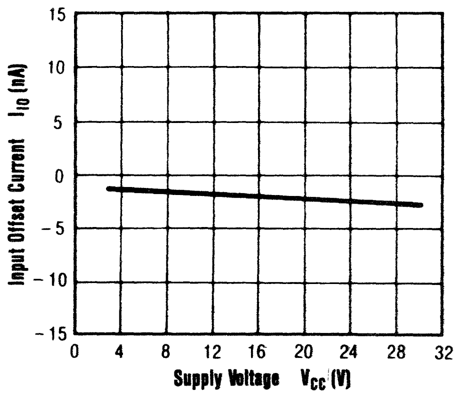


Typical Electrical Performance Curves

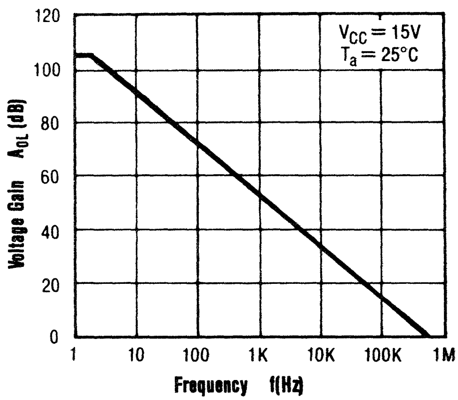
Input Offset Voltage vs Supply Voltage



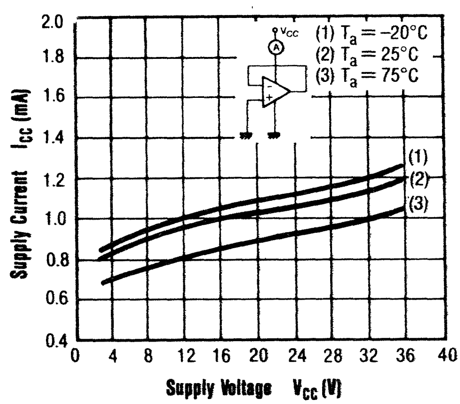
Input Offset Current vs Supply Voltage



Voltage Gain vs Frequency

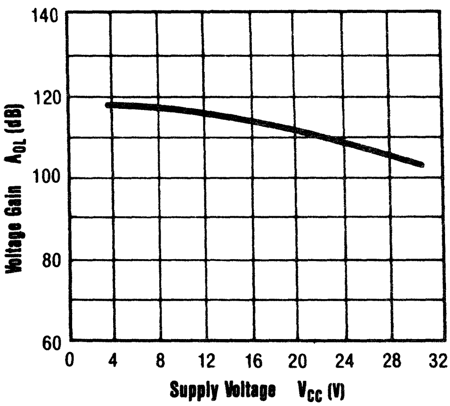


Supply Current vs Supply Voltage

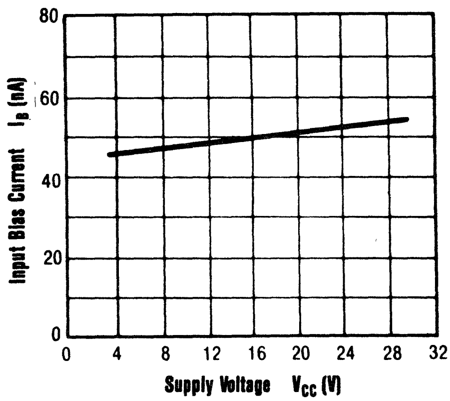


Typical Electrical Performance Curves (continued)

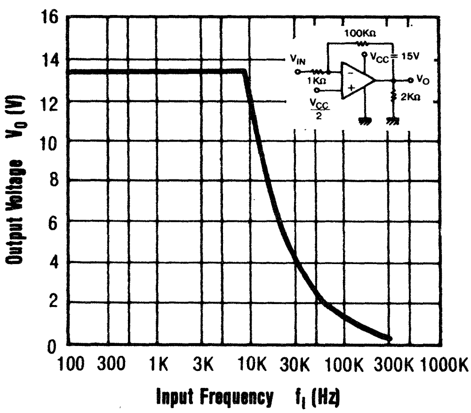
Voltage Gain vs Supply Voltage



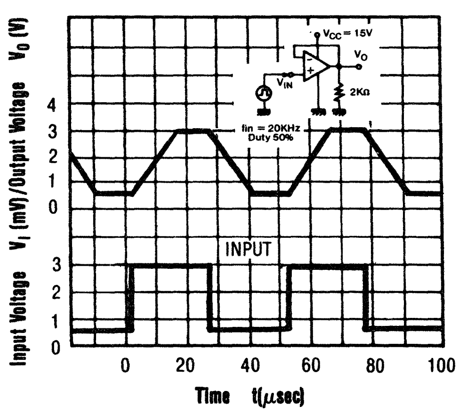
Input Bias Current vs Supply Voltage



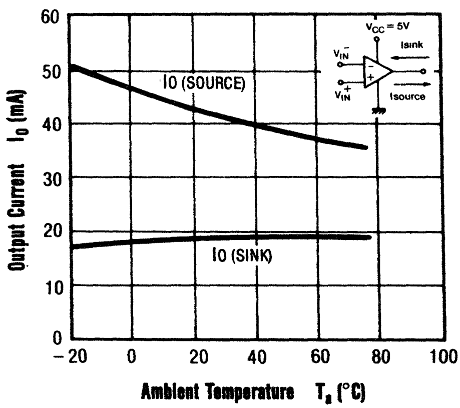
Output Voltage vs Input Frequency



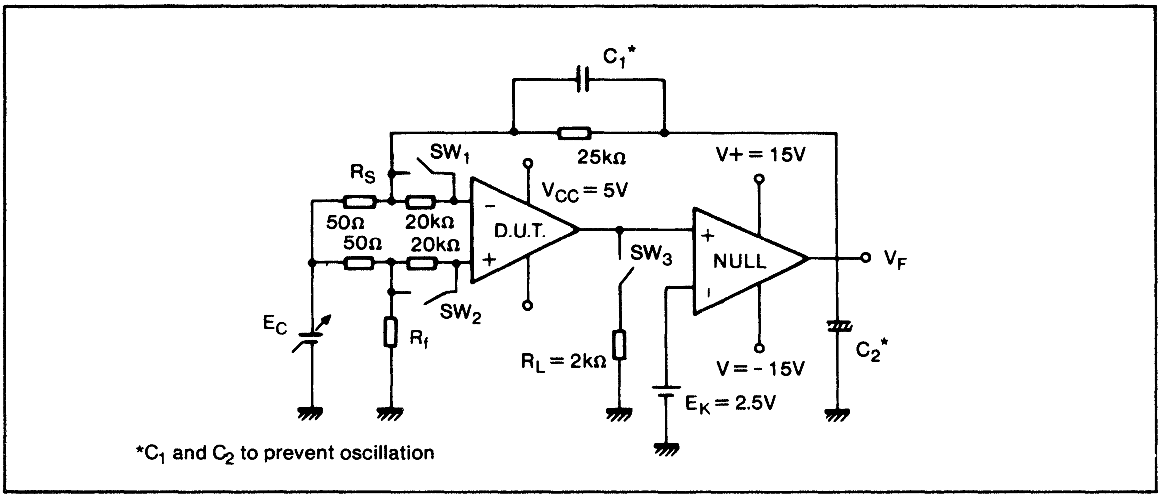
Output Response



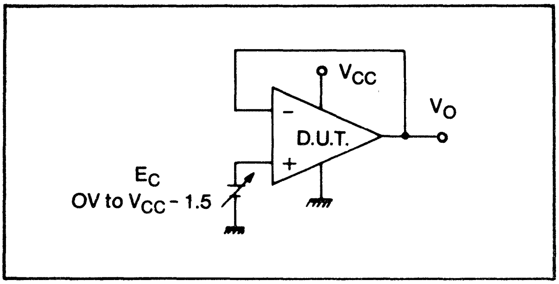
Output Current vs Ambient Temperature



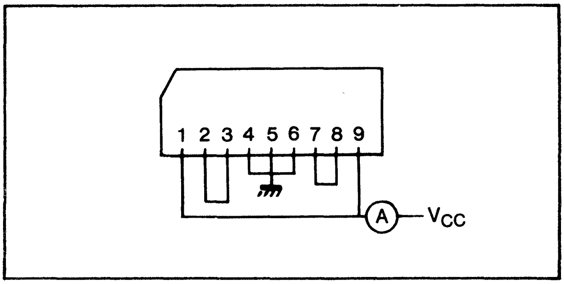
Test Circuit 1 (½ circuit)



Test Circuit 2 (½ circuit)

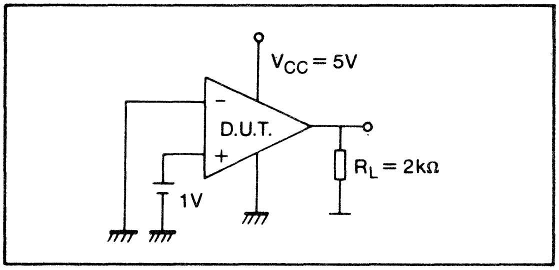


Test Circuit 3

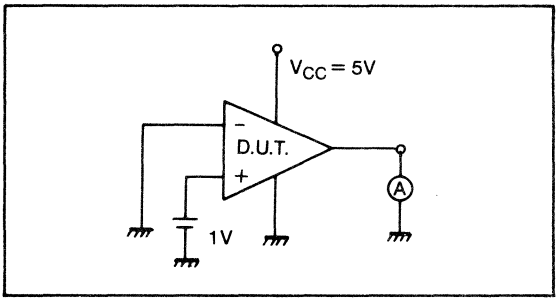


Item	Test Conditions For Circuit 1
Input Offset Voltage	Turn on SW1, SW2, and measure V_{F1} ($E_C = 0$), where $V_{IO} = V_{F1}/500$ (V)
Input Offset Current	Turn off SW1, SW2, and measure V_{F2} ($E_C = 0$), where $I_{IO} = \frac{\lvert V_{F2} - V_{F1} \rvert}{10^7}$ (A)
Input Bias Current	SW1 on, SW2 off, and measure V_{F3}, SW1, off SW2 on measure V_{F4}. $I_B = \frac{\lvert V_{F4} - V_{F3} \rvert}{2 \times 10^7}$ (A)
Voltage Gain	SW1, SW2 on, $E_K = 1.4V$, and measure V_{F5}. $E_K = 3.4V$, measure V_{F5} SW3 on $A_{OL} = 20 \log \left(\frac{1000}{V_{F1} - V_{F5}} \right)$
Common-Mode Rejection Ratio	SW1, SW2 on, and measure V_{F6} ($E_K = E_{C1}$), measure V_{F7} ($E_C = E_{C2}$) CMRR $= 20 \log \left(500 \times \left\lvert \frac{E_{C1} - E_{C2}}{V_{F6} - V_{F7}} \right\rvert \right)$
Supply Voltage (-) Rejection Ratio (+)	SW1, SW2 on, $E_C = 0$, and measure V_{F8} ($V_{CC} = V_{C1}$), measure V_{F9} ($V_{CC} = V_{C2}$), PSRR $= 20 \log \left(500 \times \left\lvert \frac{V_{C1} - V_{C2}}{V_{F8} - V_{F9}} \right\rvert \right)$

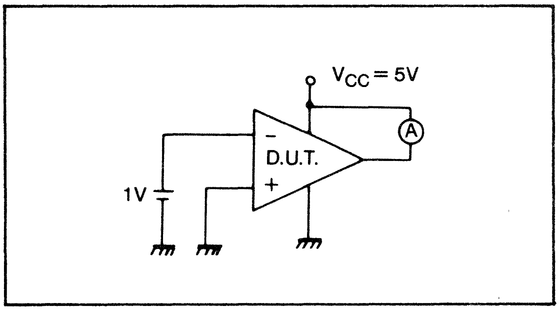
Test Circuit 4 (½ circuit)



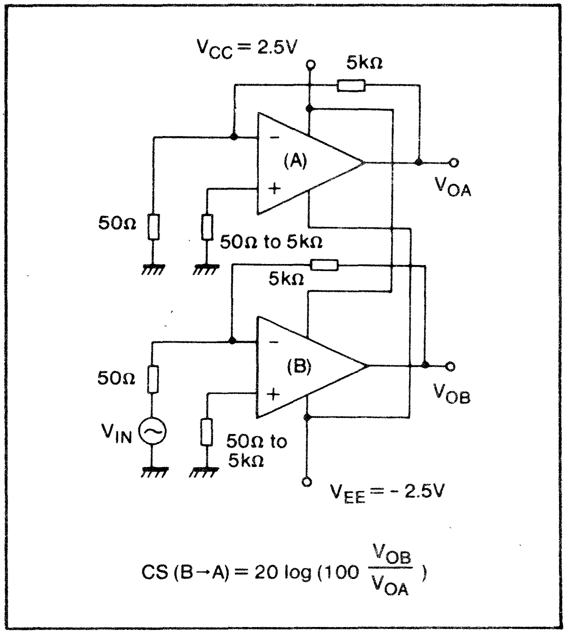
Test Circuit 6 (½ circuit)



Test Circuit 7 (½ circuit)



Test Circuit 5

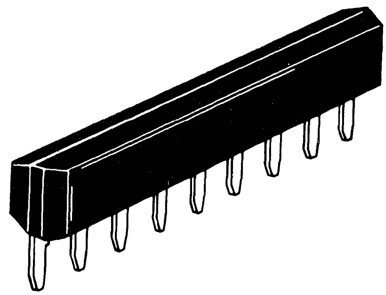


AN6571 DUAL OPERATIONAL AMPLIFIER

General Description

The AN6571 is a dual operational amplifier with general purpose characteristics in a low profile SIL package.

AN6571



9 - SIP PACKAGE (Low Profile)

Features

- General purpose
- Slew rate: 0.7 V/μ typ.
- Low offset voltage
- Low-profile SIL-9 package for compact layouts

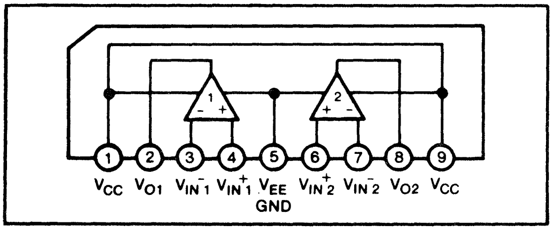
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	± 18	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	± 30	V
Input Common –Mode Voltage	V_{ICM}	± 15	V
Operating Temperature	Topr	– 20 to 75	°C
Storage Temperature	Tstg	– 55 to 150	°C

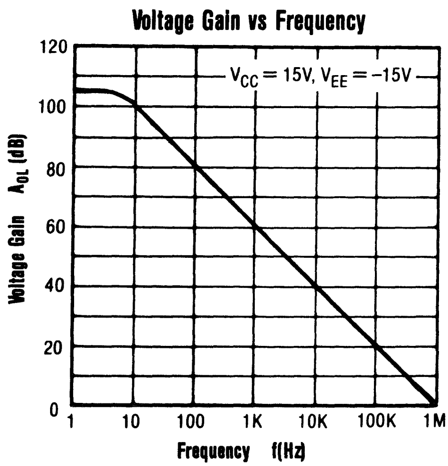
Electrical Characteristics ($V_{CC} = -V_{EE} = 15V$, $T_a = 25°C$)

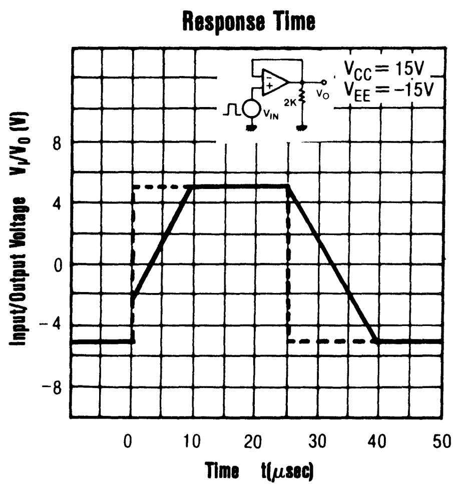
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	4	mV
Input Offset Current	I_{IO}	1			10	100	nA
Input Bias Current	I_B	1			50	250	mA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	106		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±13		V
Common-Mode Rejection Ratio	CMRR	1	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	PSRR	1	$R_S \leq 10k\Omega$		30	150	μV/V
Power Consumption	P_C	4				170	mW
Slew Rate	SR	5			0.7		V/μs
Supply Current	I_{CC}	4				5.6	mA
Output Short-Circuit Current	$I_{O (SHORT)}$	2			±20		mA

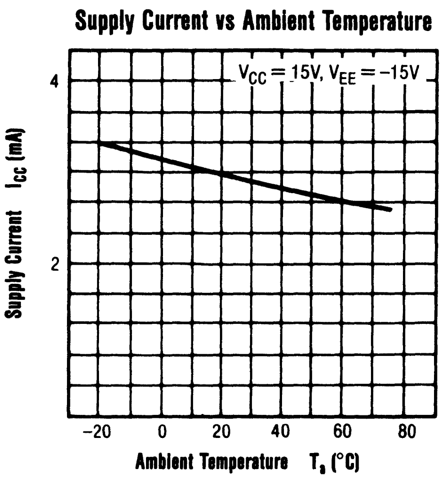
Connection Diagram

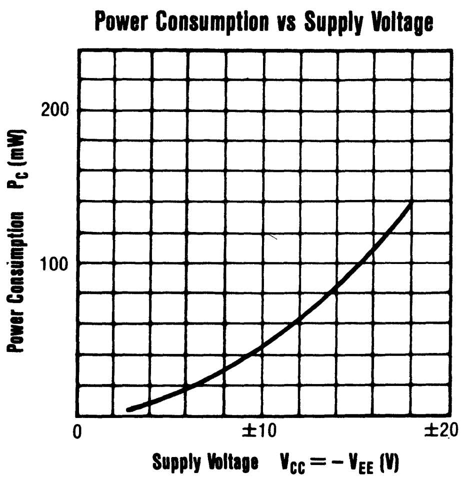


Typical Electrical Performance Curves



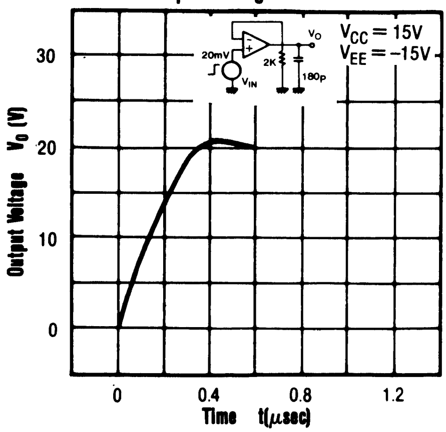




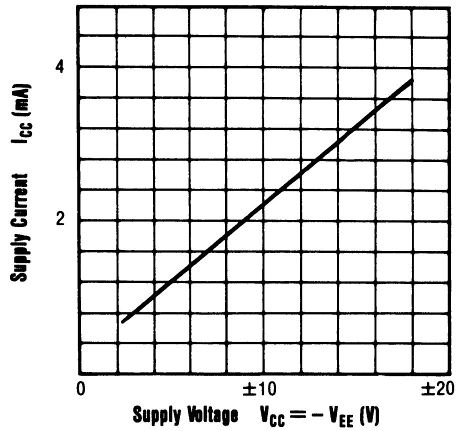


Typical Electrical Performance Curves (continued)

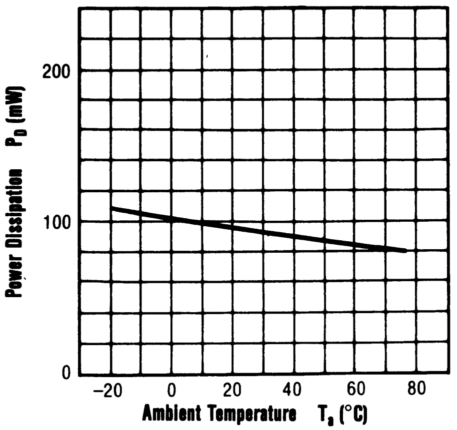
Output Voltage vs Time



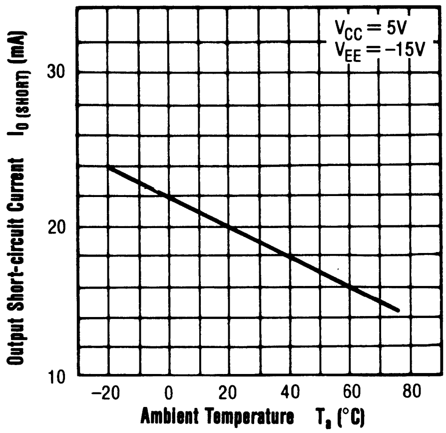
Supply Current vs Supply Voltage



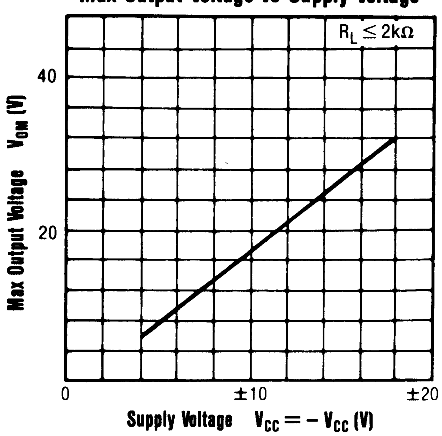
Power Dissipation vs Ambient Temperature



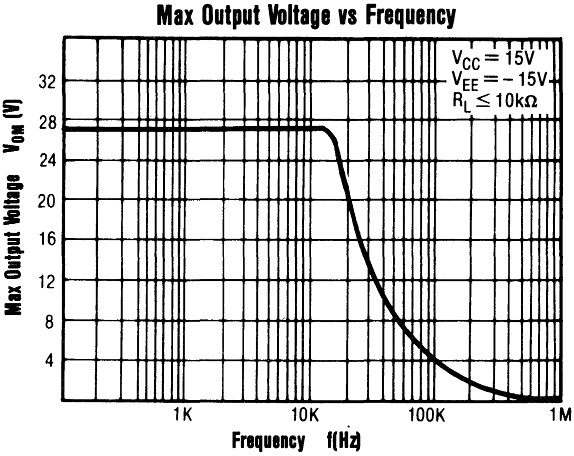
Shorted Output Current vs Ambient Temperature

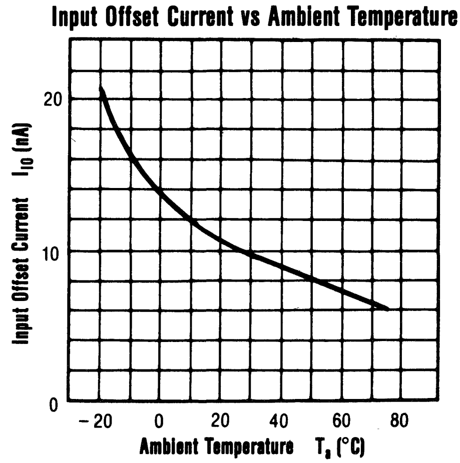


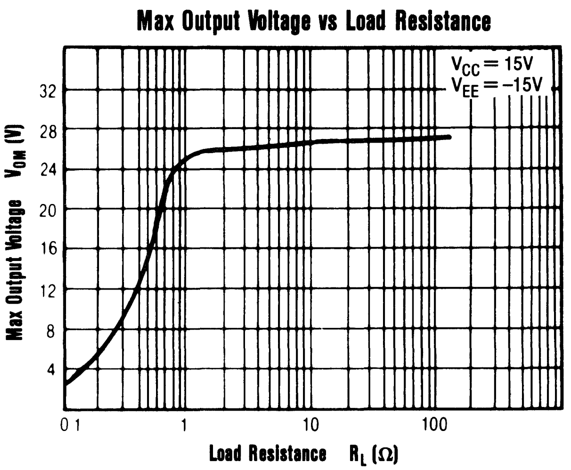
Max Output Voltage vs Supply Voltage

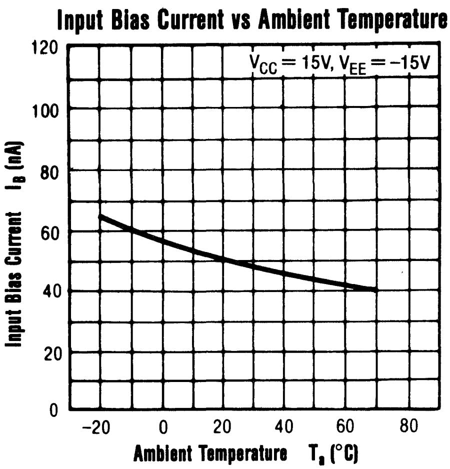


Typical Electrical Performance Curves (continued)

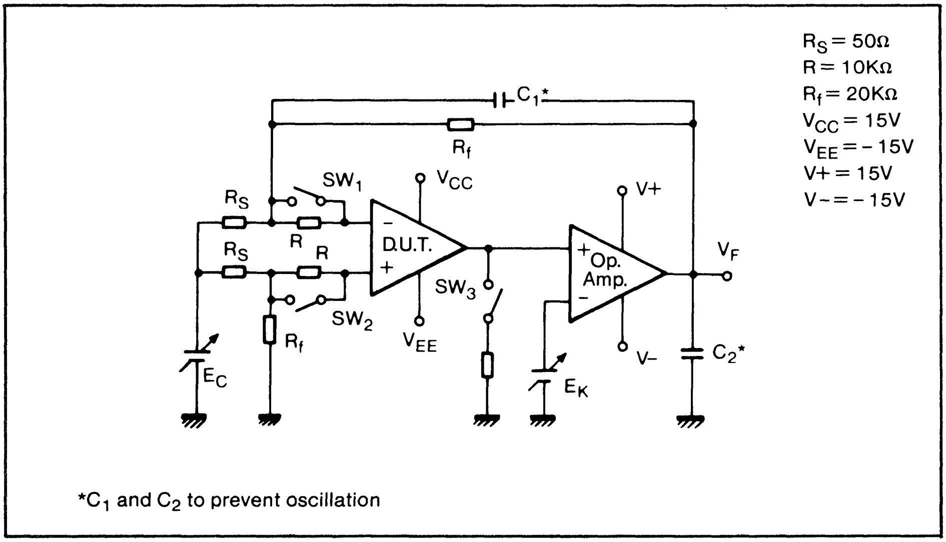




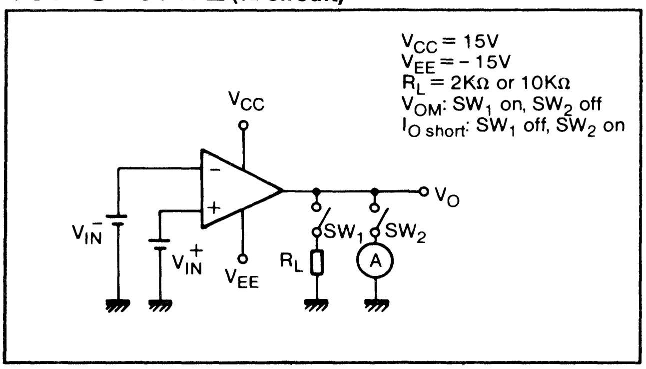




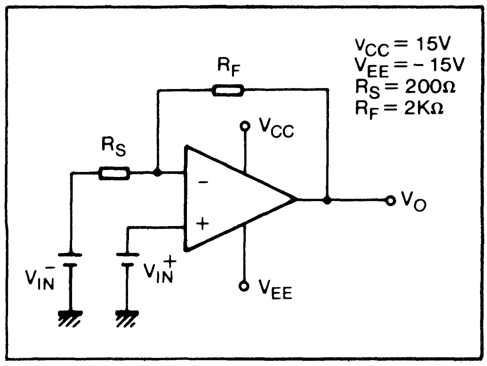
Test Circuit 1 (½ circuit)



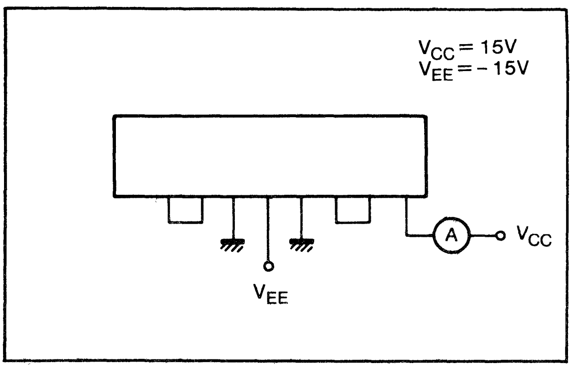
Test Circuit 2 (½ circuit)



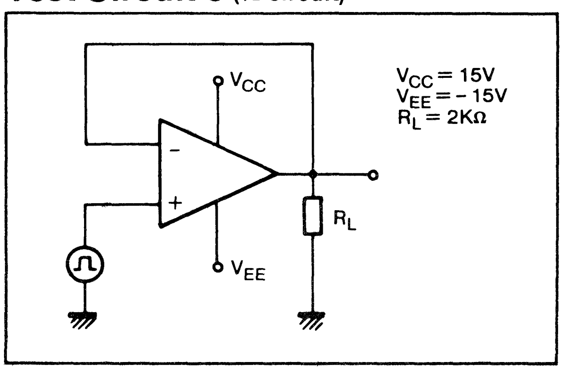
Test Circuit 3 (½ circuit)



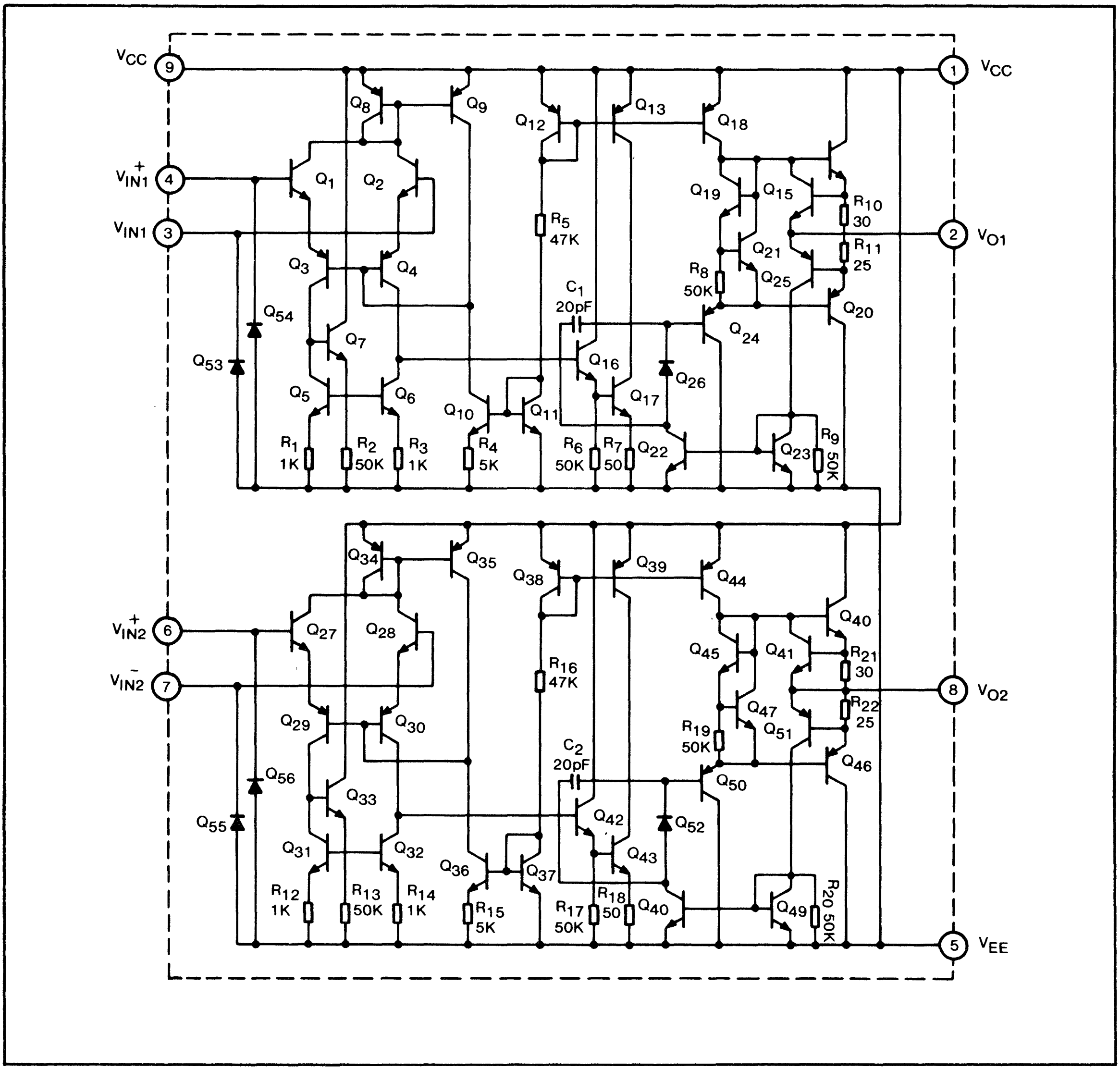
Test Circuit 4



Test Circuit 5 (½ circuit)



Schematic Diagram



AN6573 OPERATIONAL AMPLIFIER

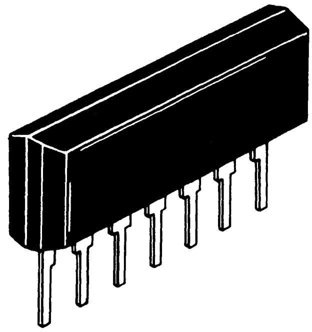
General Description

The AN6573 is a single general purpose operational amplifier in a 7 - pin single-in-line package electrically identical to "741" (AN1741) circuits.

Features

- Slew rate: 0.7 V/μ typ.
- Dual power supply operation
- 7 - pin SIL package
- Low offset voltage

AN6573



7 - SIP PACKAGE

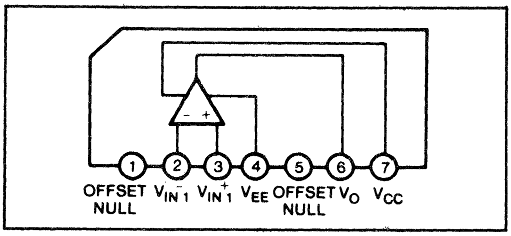
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	± 18	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	± 30	V
Input Common –Mode Voltage	V_{ICM}	± 15	V
Operating Temperature	Topr	– 20 to 75	°C
Storage Temperature	Tstg	– 55 to 150	°C

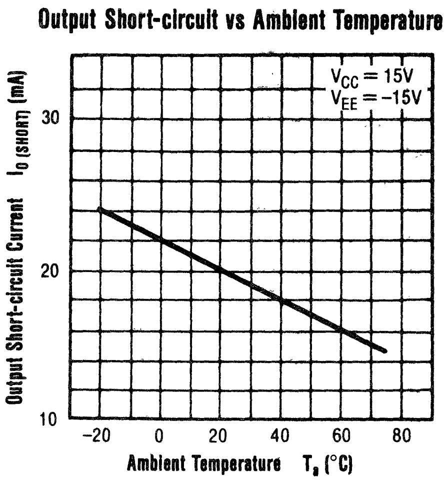
Electrical Characteristics ($V_{CC} = 15V$, $T_a = 25°C$)

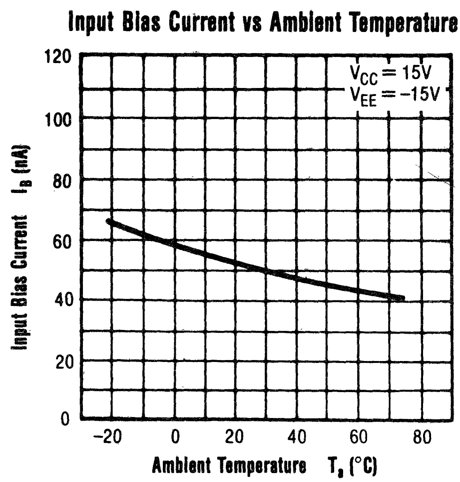
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1	$R_S \leq 10k\Omega$		0.5	4	mV
Input Offset Current	I_{IO}	1			10	100	nA
Input Bias Current	I_B	1			50	250	nA
Voltage Gain	A_{OL}	1	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	86	106		dB
Output Voltage (max)	V_{O1}	2	$R_L \geq 10k\Omega$	±12	±14		V
	V_{O2}	2	$R_L \geq 2k\Omega$	±10	±13		V
Common-Mode Input Voltage	V_{CM}	3		±12	±13		V
Common-Mode Rejection Ratio	CMRR	1	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	PSRR	1	$R_S \leq 10k\Omega$		30	150	μV/V
Power Consumption	P_C	4				85	mW
Slew Rate	SR	5			0.7		V/μs
Supply Current	I_{CC}	4				2.8	mA
Output Short-Circuit Current	$I_{O(SHORT)}$	2			±20		mA

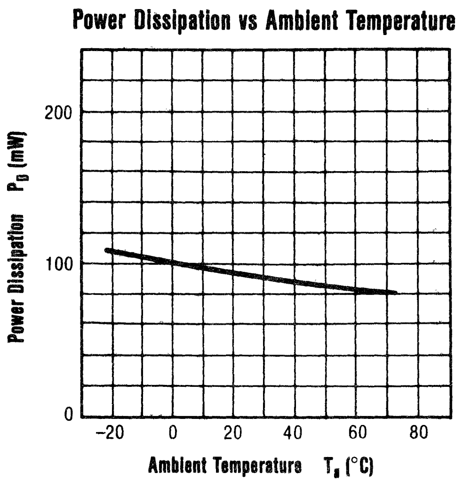
Connection Diagram

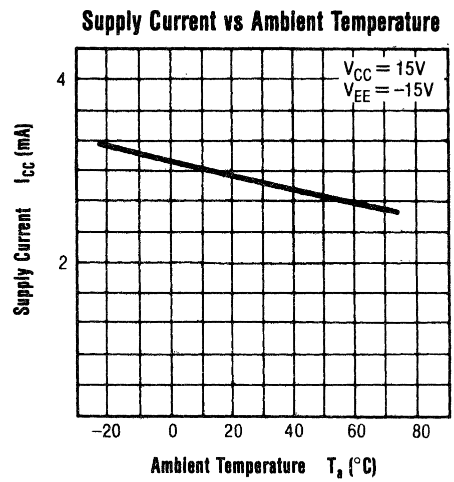


Typical Electrical Performance Curves



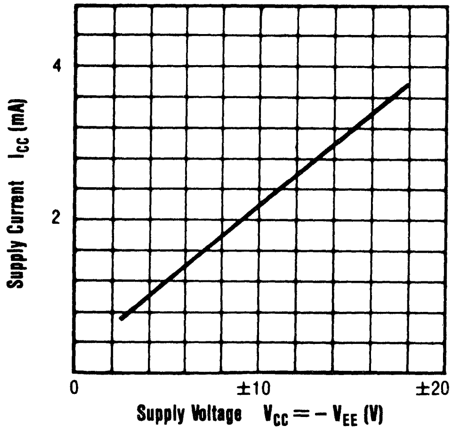




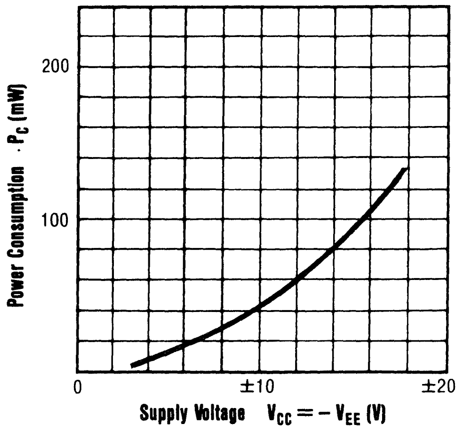


Typical Electrical Performance Curves (continued)

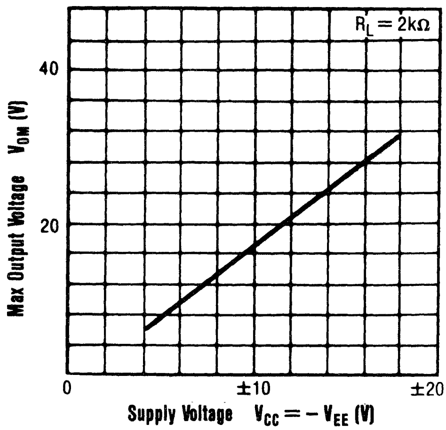
Supply Current vs Supply Voltage



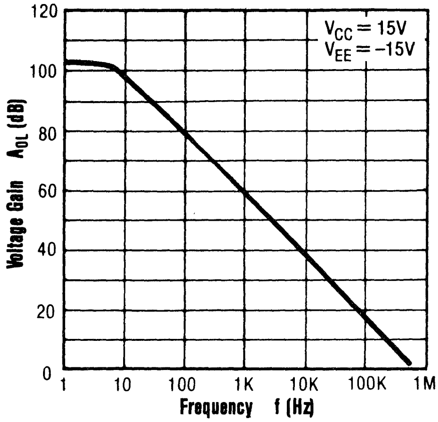
Power Consumption vs Supply Voltage



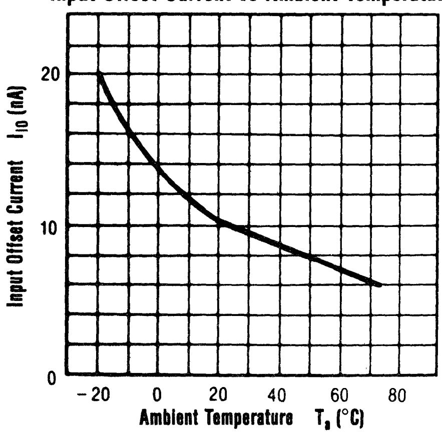
Max Output Voltage vs Supply Voltage



Voltage Gain vs Frequency

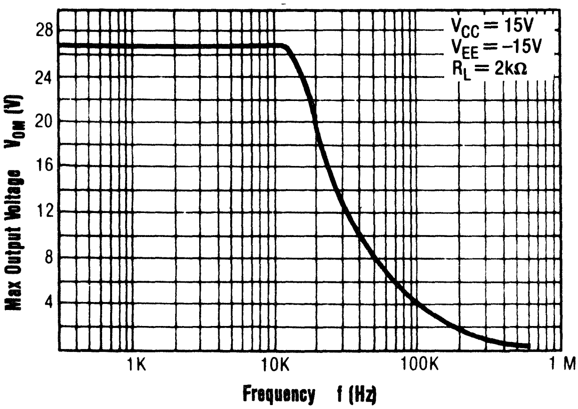


Input Offset Current vs Ambient Temperature

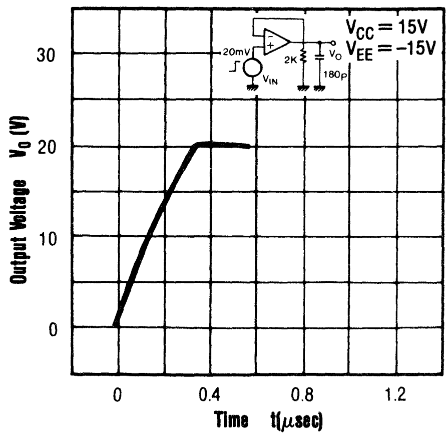


Typical Electrical Performance Curves (continued)

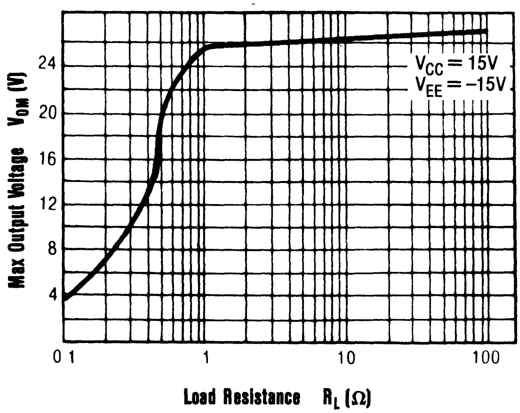
Max Output Voltage vs Frequency



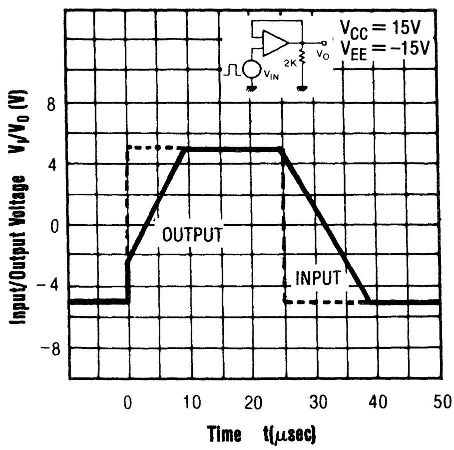
Output Voltage vs Time



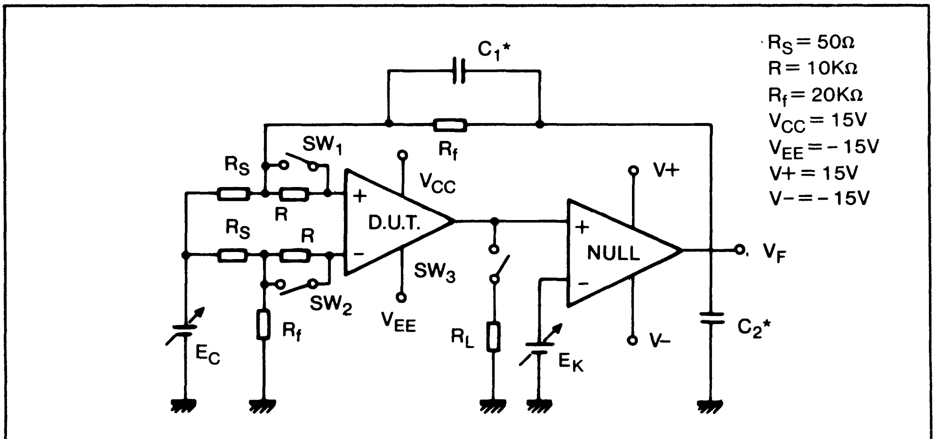
Max Output Voltage vs Load Resistance



Response Time



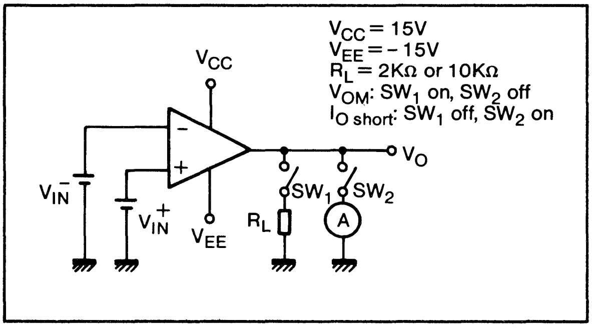
Test Circuit 1



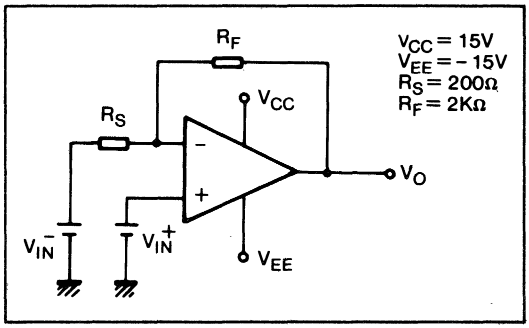
*C_1 and C_2 to prevent oscillation

Item	Test Conditions For Circuit 1
Input Offset Voltage	With SW1, SW2, and SW3 off, V_{FI} is measured on the basis of $E_C = E_K = 0$, where $V_{IO} = V_{F1}/400$ (V).
Input Offset Current	With SW1, SW2 on and SW3 off, V_{F2} is measured on the basis of $E_C = E_K = 0$, where $I_{IO} = \lvert V_{F2} - V_{F1} \rvert / 4 \times 10^6$ (A).
Input Bias Current	With SW3 off while $E_C = E_K = 0$ and SW1, on, SW2, off, V_{F3} is measured. V_{F4} is measured with SW1 and SW2 inverse. Where $I_B = \lvert V_{F3} - V_{F4} \rvert / 8 \times 10^6$ (A).
Voltage Gain	With SW1, SW2 and SW3 on and $E_C = 0$, $E_K = 10V$, V_{F5} is measured and V_{F5} is measured again with $E_K = -10V$. Where $A_{OL} = 20 \log \left(\frac{8000}{V_{F5} - V_{F5}} \right)$
Common-Mode Rejection Ratio	With SW1 and SW2 on, SW3 off, and $E_K = 0$, $E_C = 5V$, V_{F6} is measured. With $E_C = -5V$, V_{F6} is measured again. Where: $CMRR = \left(\frac{4000}{V_{F6} - V_{F6}} \right)$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on, SW3 off, $E_K = E_C = 0$, $V_{CC} = 10V$, V_{F7} is measured. Where: $PSRR (+) = \lvert V_{F7} - V_{F2} \rvert / 2 \times 10^3$
Supply Voltage (−) Rejection Ratio (+)	With SW1, SW2 on SW3, off and $E_K = E_C = 0$ $V_{EE} = -10V$, V_{F8} is measured, Where: $PSRR (-) = \lvert V_{F8} - V_{F2} \rvert \; 2 \times 10^3$

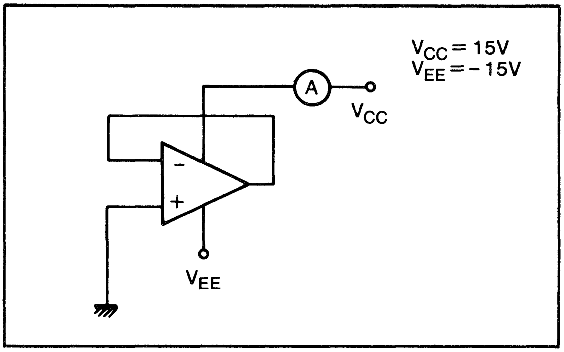
Test Circuit 2



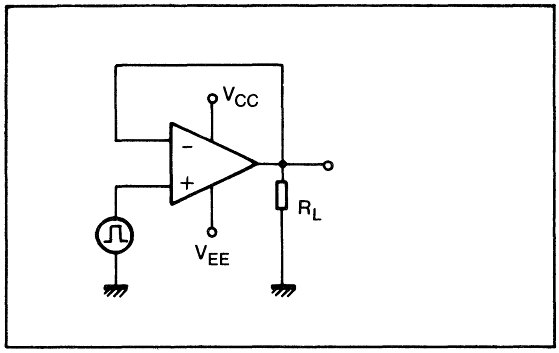
Test Circuit 3



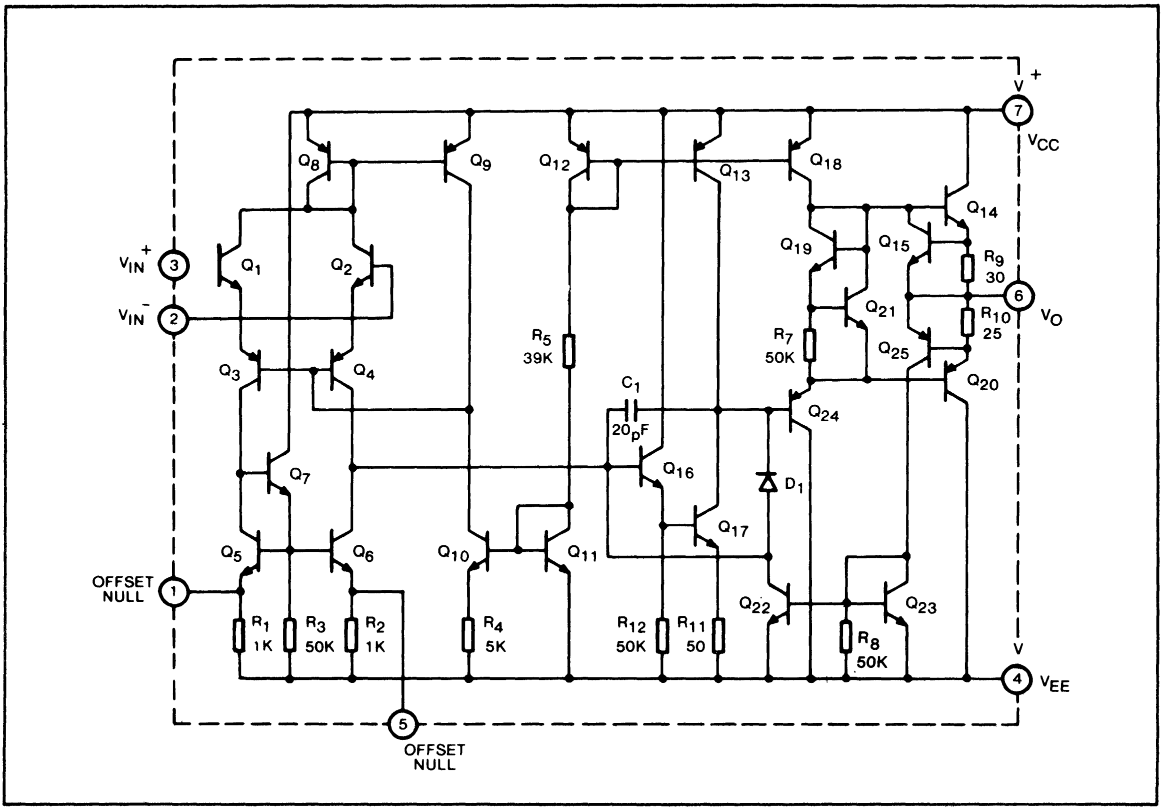
Test Circuit 4



Test Circuit 5



Schematic Diagram

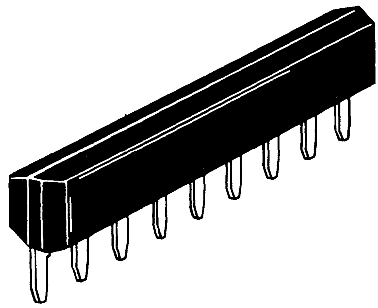


AN6593 OPERATIONAL AMPLIFIER

General Description

The AN6593 is a versatile, programmable, operational amplifier. A single external bias current, setting resistor programs: the bias current, offset current, quiescent power consumption, slew rate, input noise and the gain-bandwidth product.

AN6593



9 - SIP PACKAGE (Low Profile)

Features

- Operates from ± 1V to ± 18V
- Electric characteristics can be programmed by changing set current
- Phase compensation circuit is built-in
- Output short circuit protection circuit is built-in
- Off-set is externally adjustable

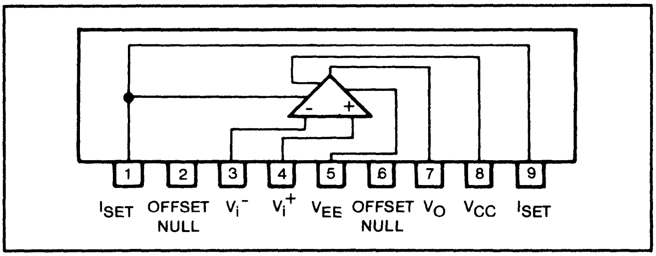
Absolute Maximum Ratings ($T_a = 25$)

Item	Symbol	Ratings	Unit
Supply Voltage	Vcc	± 18	V
Power Dissipation	PD	500	mW
Input Differential Voltage	VID	± 30	V
Input Common-Mode Voltage	VICM	± 15	V
Operating Temperature	Topr	− 20 to + 75	°C
Storage Temperature	Tstg	− 50 to + 150	°C

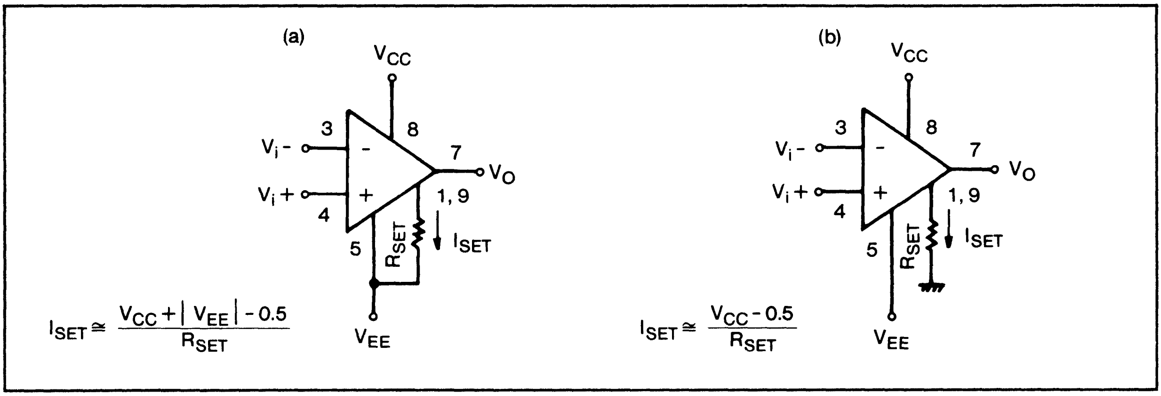
Electrical Characteristics (Vcc = 15V, VEE = − 15V, Ta = 25°C)

Item	Symbol	Condition	ISET = 1μA		ISET = 10μA		Unit
			min.	max.	min.	max.	
Input Offset Voltage	VIO	Rs ≤ 100kΩ		5		6	mV
		V± = ± 1.5V, Rs ≤ 100kΩ		5		6	
Input Offset Current	IIO			6		20	nA
Input Bias Current	IB			10		75	nA
		V± = ± 1.5		10		75	
Large Signal Voltage Gain	AOL	Vo = ± 10V, RL = 100kΩ	96				dB
		Vo = ± 10V, RL = 10kΩ			96		
Supply Current	Icc			11		100	μA
		V± = ± 1.5V		8		90	
Power Consumption	Pc			330		3000	μW
		V± = ± 1.5V		24		270	
Input Common-Mode Voltage	VCM		± 13.5		± 13.5		V
		V± = ± 1.5V	± 0.6		± 0.6		
Output Voltage (max)	VOM	RL = 100kΩ	± 12				V
		V± = ± 1.5V, RL = 100kΩ	± 0.6				
Common-Mode Rejection Ratio	CMRR	RL = 10kΩ			± 12		V
		V± = ± 1.5V, RL = 10kΩ			± 0.6		
Supply Voltage Rejection Ratio	PSRR	Rs ≤ 10kΩ	70		70		dB
		Rs ≤ 10kΩ	74		74		

Connection Diagram



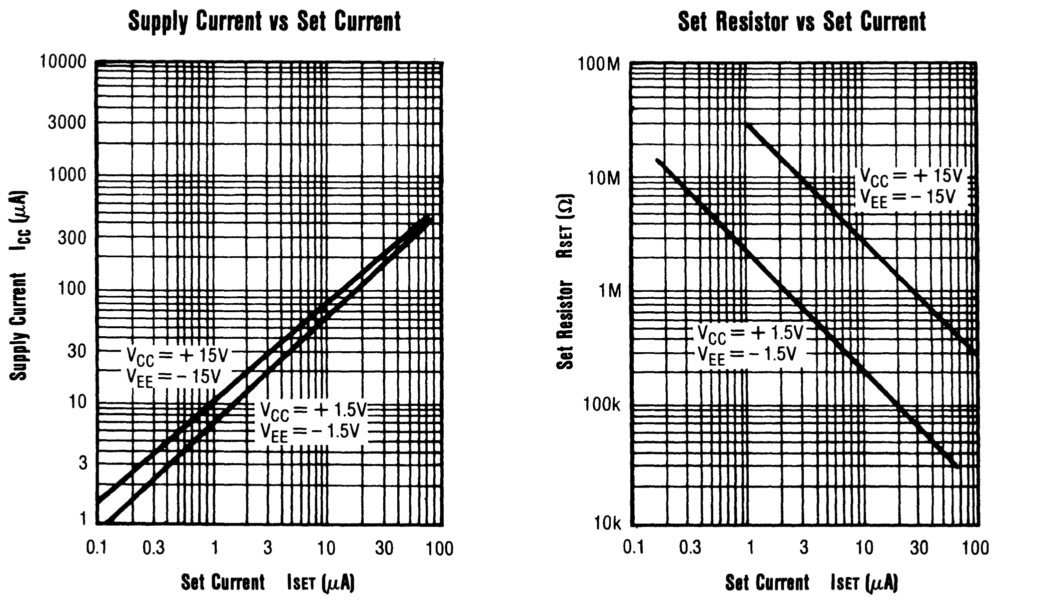
Connections for ISET



(a) $$I_{SET} \cong \frac{V_{CC} + |V_{EE}| - 0.5}{R_{SET}}$$

(b) $$I_{SET} \cong \frac{V_{CC} - 0.5}{R_{SET}}$$

Typical Characteristics for ISET



AN1339/AN1339S (AN6912) QUADRUPLE COMPARATOR

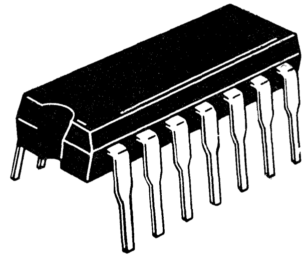
General Description

AN1339 is a quadruple comparator which has a wide range of supply voltage, dual and single supply. It is equivalent to most "339" circuits

Features

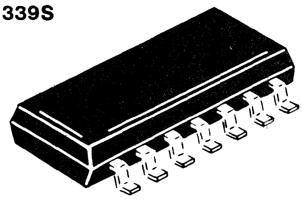
- A wide range of supply voltage
  Single supply: 2 to 36V
  Dual supply: ± 1 to ± 18V
- Low circuit current: 0.8 mA typ.
- A wide range of common-mode input voltage:
  0V to V_{CC} - 1.5V (single supply)
- Open collector output

AN1339 (AN6912)



14 - DIP PACKAGE

AN1339S



SO - 14D PACKAGE

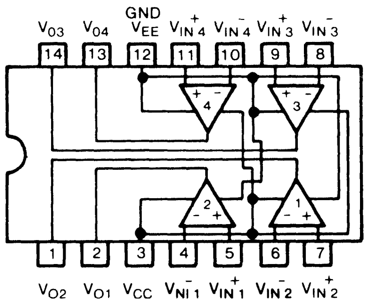
Absolute Maximum Ratings (T_a = 25°C)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}, V_{EE}	36	V
Power Dissipation	(14 DIP)	P_D	570	mW
	(14 SO)	P_D	360	mW
Input Differential Voltage		V_{ID}*2	36	V
Input Common−Mode Voltage		V_{ICM}*1	− 0.3 to + 36	V
Operating Temperature		Topr	− 20 to + 75	°C
Storage Temperature		Tstg	− 55 to + 150	°C

Electrical Characteristics (V_{CC} = 5V, T_a = 25°C)

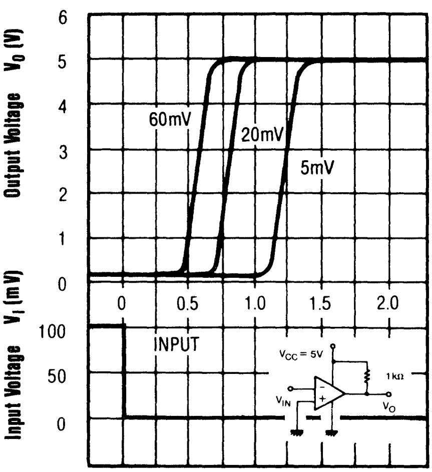
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	1			2	5	mV
Input Offset Current	I_{IO}	1				50	nA
Input Bias Current	I_B	1				250	nA
Voltage Gain	A_{OL}	1	R_L = 15kΩ		200		V/mV
Common-Mode Input Voltage	V_{CM}	2		0		V − 1.5	V
Response Time	t_R	4	R_L = 5.1kΩ V_{RL} = 5V		1.3		μs
Output Current (Sink)	$I_{O (SINK)}$	5	V_{REF} = 0V V_{IN} = 1V $V_O \leq$ 1.5V	6			mA
Output Saturation Voltage	V_{OL}	6	V_{REF} = 0V V_{IN} = 1V I_{SINK} = 3mA		0.2	0.4	V
Output Leakage Current	I_{LEAK}	7	V_{IN} = 0V V_{REF} = 1V V_O = 5V		0.1		nA
Supply Current	I_{CC}	3	R_L = ∞		0.8	2	mA

Connection Diagram



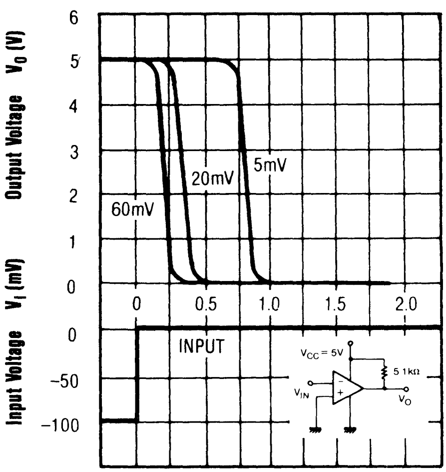
Typical Electrical Performance Curves

Output Response Chart (1)



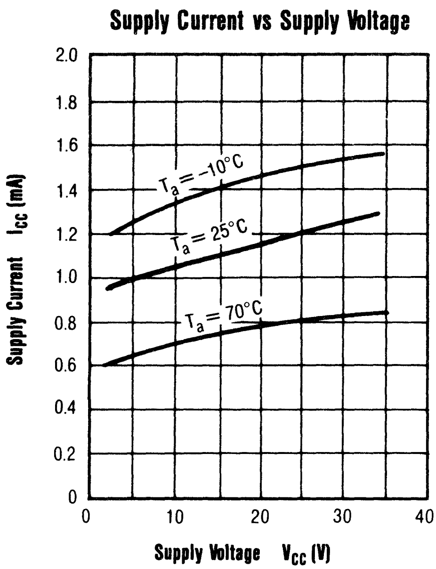
Time t_{PHL} (μsec)
(Negative Transition)

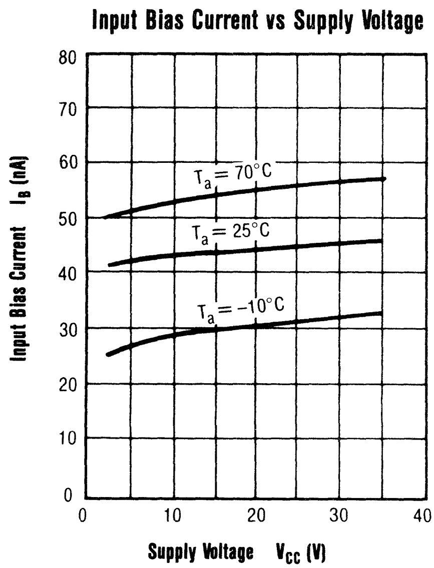
Output Response Chart (2)

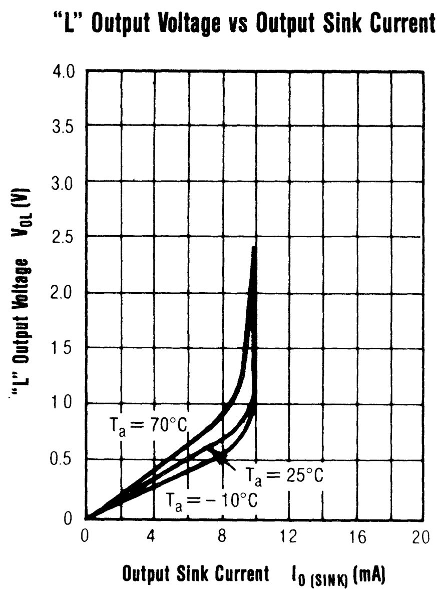


Time t_{PLH} (μsec)
(Positive Transition)

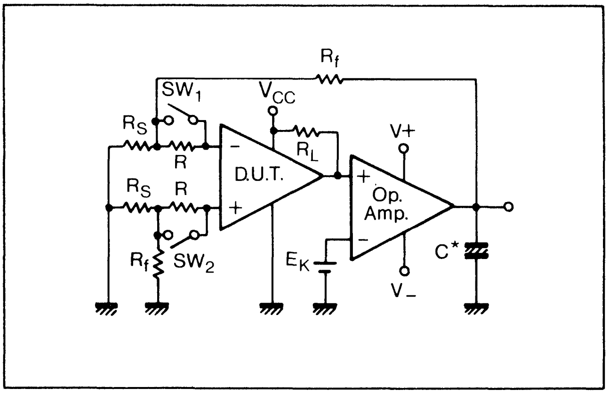
Typical Electrical Performance Curves (continued)



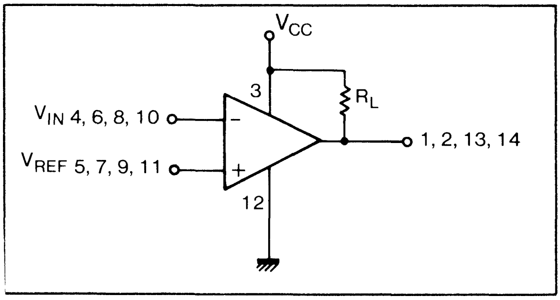




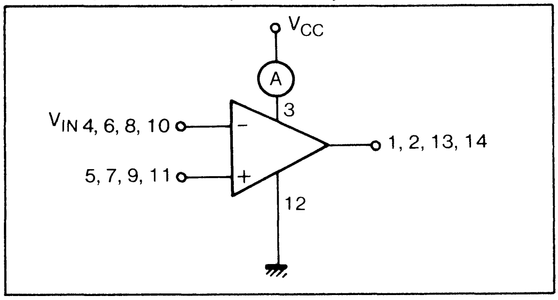
Test Circuit 1 (¼ circuit)



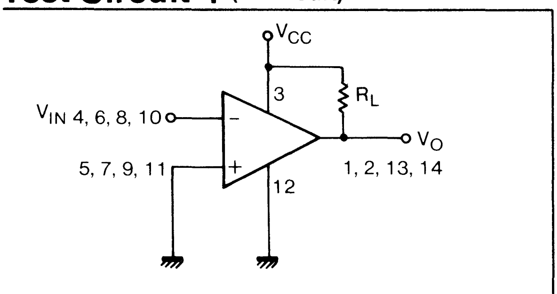
Test Circuit 2 (¼ circuit)



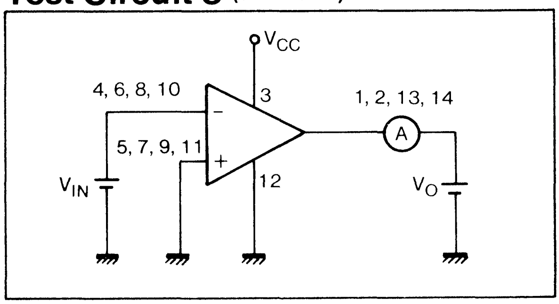
Test Circuit 3 (¼ circuit)



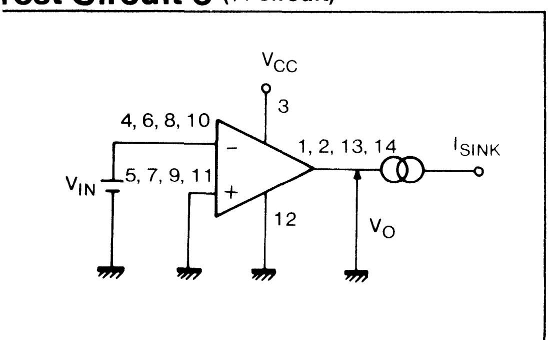
Test Circuit 4 (¼ circuit)



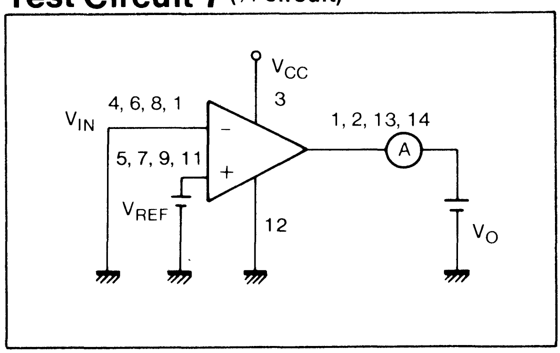
Test Circuit 5 (¼ circuit)



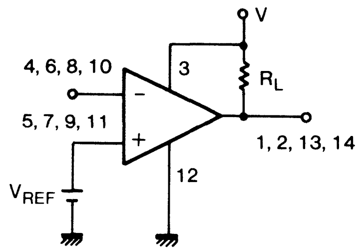
Test Circuit 6 (¼ circuit)



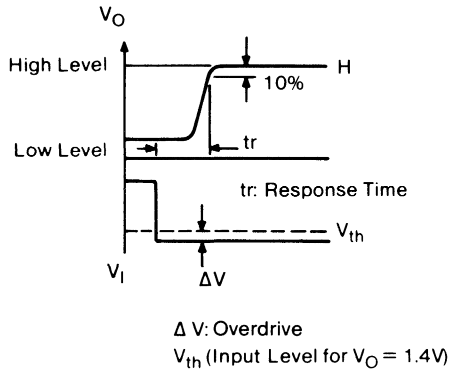
Test Circuit 7 (¼ circuit)



Application Circuit (1/4 circuit)

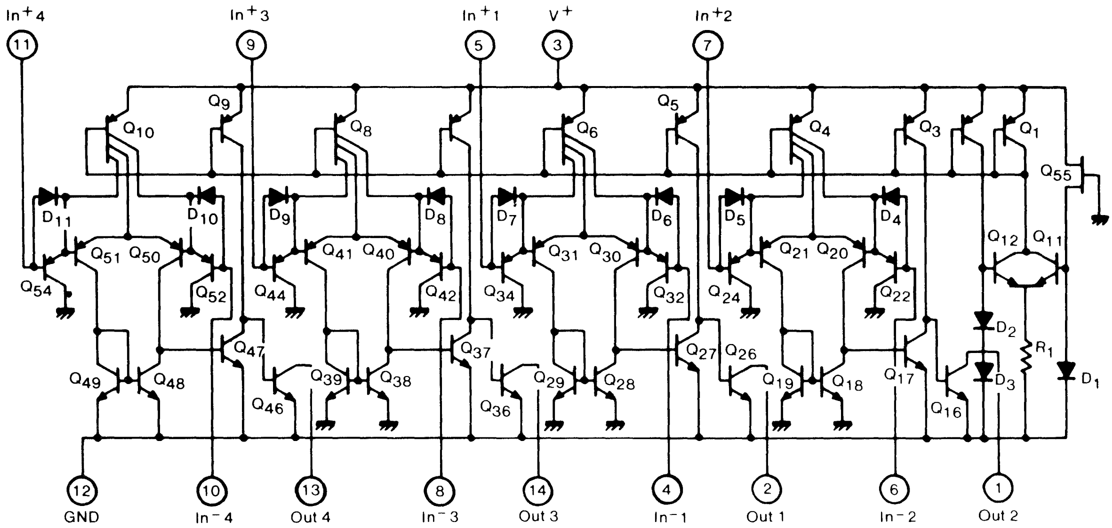


Definition of the Response Time



Item	Test Conditions For Circuit 1
Input Offset Voltage	With SW1, and SW2 on, V_{F1} is measured. Where $V_{IO} = V_{F1}/500$ (V).
Input Offset Current	With SW1, and SW2 off, V_{F2} is measured. Where $I_{IO} = \left(\frac{V_{F2} - V_{F1}}{10^7}\right)$
Input Bias Current	With SW1 on, and SW2, off, SW2, off, V_{F3} is measured.With SW1 off, and SW2 on, V_{F4} is measured. Where $I_B = \mid V_{F4} - V_{F3} \mid /2 \times 10$ (A)
Voltage Gain	With SW1, and SW2 on, and $E = E_K = 3$ V_{F5} is measured. Where $A_{OL} = \left(\frac{1000}{V_{F1} - V_{F5}}\right)$

Schematic Diagram

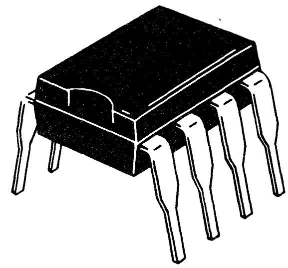


AN1393/AN1393S (AN6914) DUAL COMPARATOR

General Description

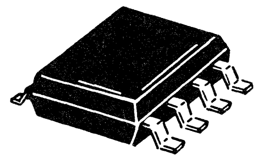
The AN1393 consists of two independent precision voltage comparators with low offset voltages. It is available in both DIL low S.O. packages. The AN1393 is equivalent to most "393" circuits.

AN1393 (AN6914)



8 - DIP PACKAGE

AN1393S



SO - 8D PACKAGE

Features

- Wide supply voltage range
  Single supply: 2 to 36V
  Dual supplies: ± 1 to ± 18V
- Low supply current: 0.6 mA (typ.)
- Wide common-mode voltage range:
  OV to V_{CC} - 1.5V (single supply)
- Open collector output
- 8 - pin DIP or 8 - pin S.O. plastic package

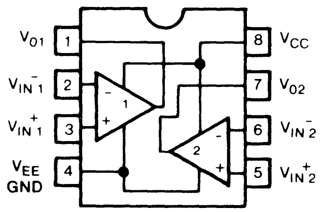
Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}, V_{EE}	36	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	36	V
Input Common –Mode Voltage	V_{ICM}	– 0.3 to 36	V
Operating Temperature	Topr	– 30 to 85	°C
Storage Temperature	Tstg	– 55 to 150	°C
Output Voltage	V_O	24	V

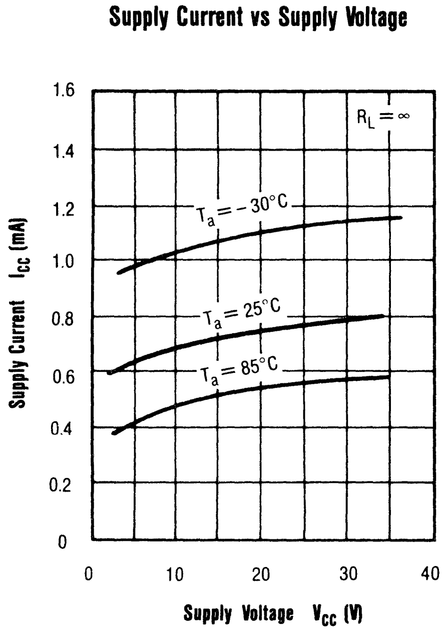
Electrical Characteristics (V_{CC} = 5V, T_a = 25°C)

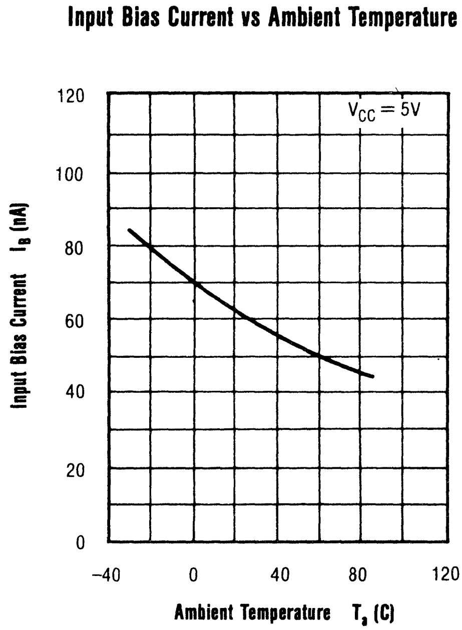
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	1			(1)	5	mV
Input Offset Current	I_{IO}	1				50	nA
Input Bias Current	I_B	1				250	nA
Voltage Gain	A_{OL}	1	R_L = 15kΩ		200		V/mV
Common-Mode Input Voltage	V_{CM}	2		0		V_{CC} – 1.5V	V
Response Time	t_R	4	R_L = 5.1kΩ V_{RL} = 5V		1.3		μs
Output Current (Sink)	$I_{O(SINK)}$	5	V_{REF} = 0V V_{IN} = 1V V_O = 1.5V	10			mA
Output Saturation Voltage	V_{OL}	6	V_{REF} = 0V V_{IN} = 1V I_{SINK} = 3mA		0.2	0.4	V
Output Leakage Current	I_{LEAK}	7	V_{IN} = 0V V_{REF} = 1V V_O = 5V		0.1		nA
Supply Current	I_{CC}	3	R_L = ∞		0.6	1.5	mA

Connection Diagram



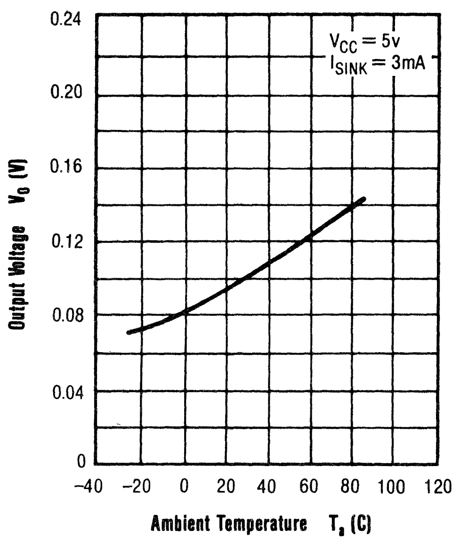
Typical Electrical Performance Curves



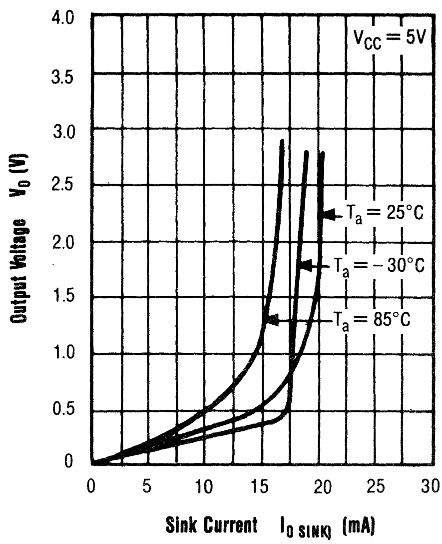


Typical Electrical Performance Curves (continued)

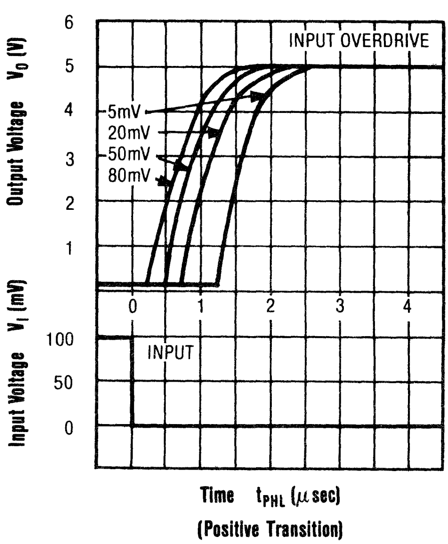
Output Voltage vs Ambient Temperature



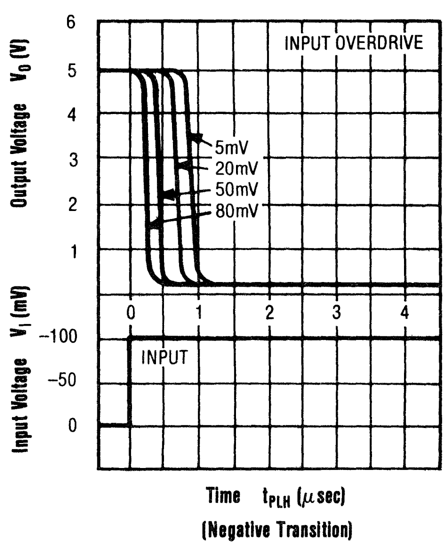
Output Voltage vs Sink Current



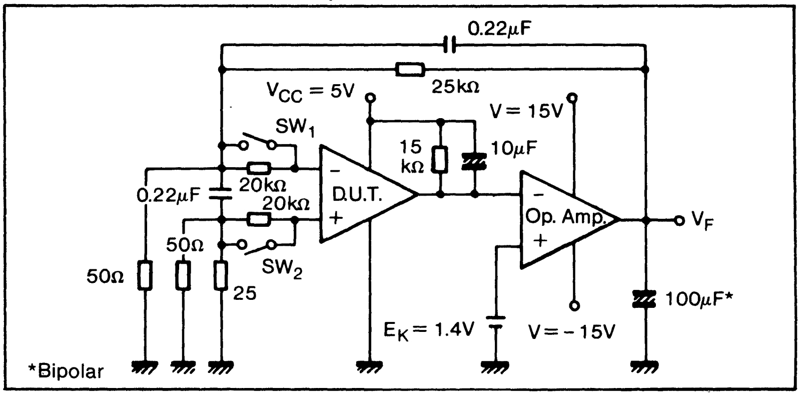
Output Response (1)



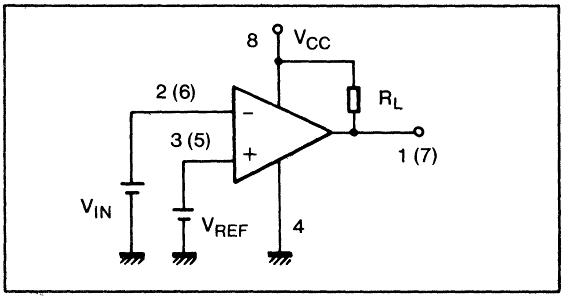
Output Response (2)



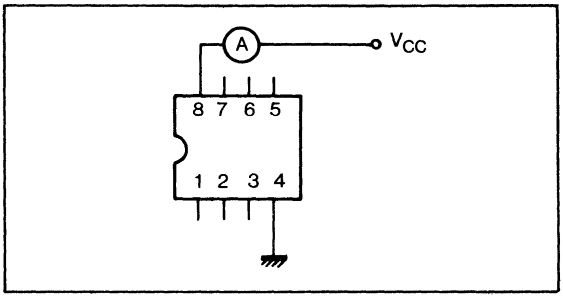
Test Circuit 1 (½ circuit)



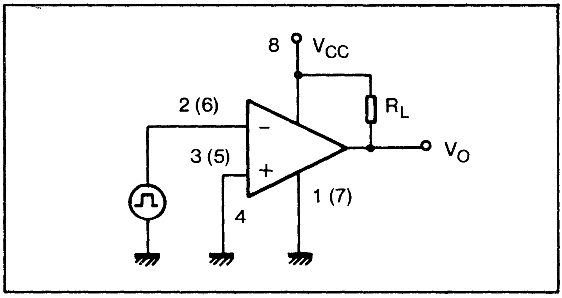
Test Circuit 2 (½ circuit)



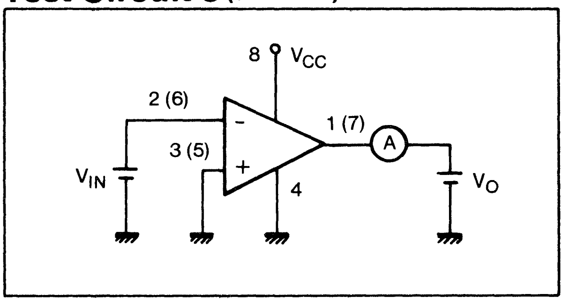
Test Circuit 3



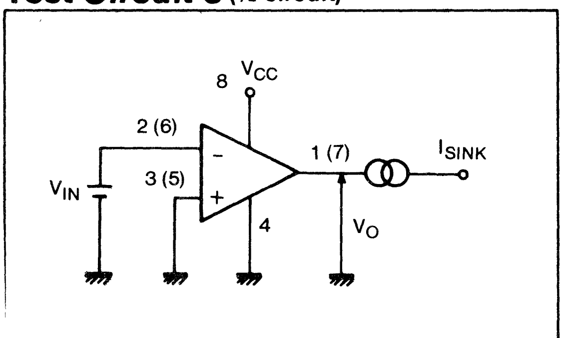
Test Circuit 4 (½ circuit)



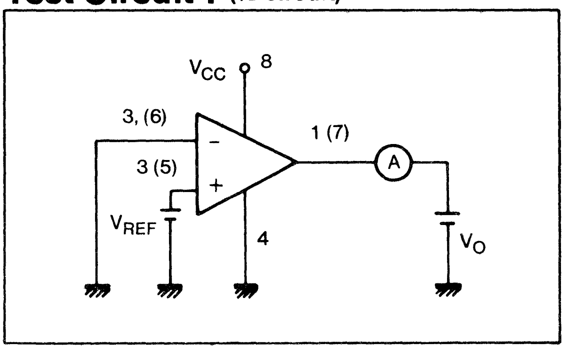
Test Circuit 5 (½ circuit)



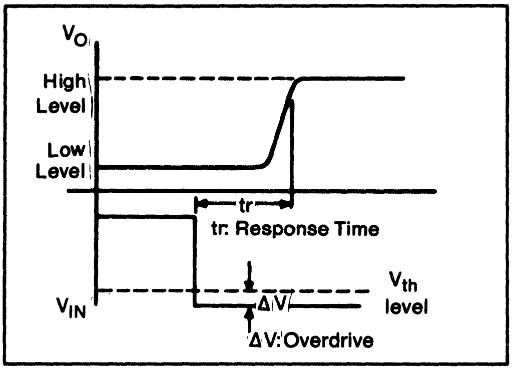
Test Circuit 6 (½ circuit)



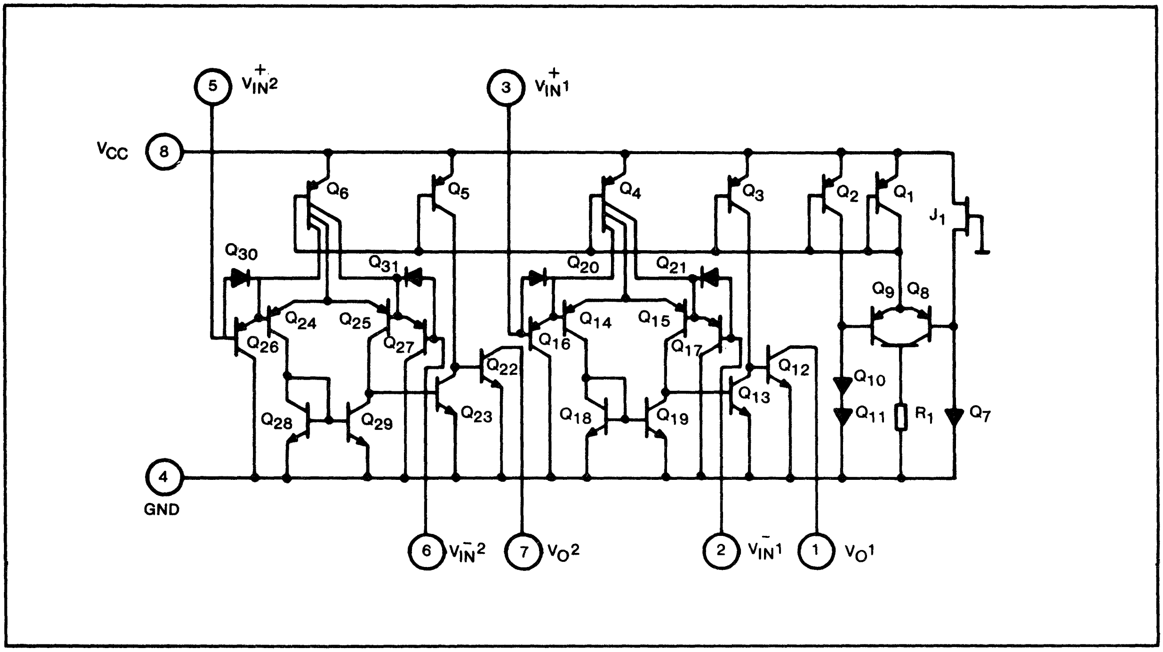
Test Circuit 7 (½ circuit)



Definition of the Response Time



Schematic Diagram



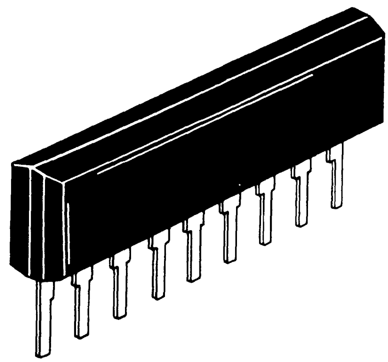
Item	Test Conditions For Circuit 1
Input Offset Voltage	With SW1, and SW2 on, V_{F1} is measured. Where $V_{IO} = V_{F1}/500$ (V).
Input Offset Current	With SW1, and SW2 off, V_{F2} is measured. Where $I_M = \left(\frac{V_{F2} - V_{F1}}{10^7}\right)$
Input Bias Current	With SW1 on, and SW2, off, SW2, off, V_{F3} is measured.With SW1 off, and SW2 on, V_{F4} is measured. Where $I_B = \lvert V_{F4} - V_{F3} \rvert /2 \times 10$ (A)
Voltage Gain	With SW1, and SW2 on, and $E = E_K = 3$ V_{F5} is measured. Where $A_{OL} = \left(\frac{1000}{V_{F1} - V_{F5}}\right)$

AN6913 DUAL COMPARATOR

General Description

The AN6913 consists ot two independent precision voltage comparators with low offset voltages in a 9-pin SIL package

AN6913



9-SIP PACKAGE

Features

- Wide supply voltage range - Single supply: 2 to 36V Dual supplies: ± 1 to ± 18V
- Low supply current: 0.6 mA (TYP)
- Wide common-mode voltage range: 0V to V_{CC} - 1.5V (single supply)
- Open collector output
- 9 - pin SIL package

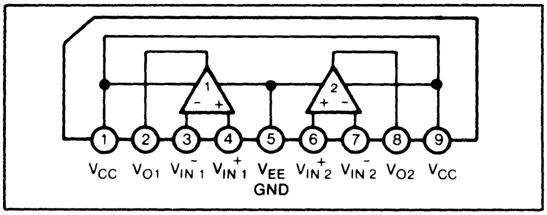
Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	36	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	36	V
Input Common-Mode Voltage	V_{ICM}	-0.3 to 36	V
Operating Temperature	Topr	-30 to 85	°C
Storage Temperature	Tstg	-55 to 150	°C
Output Voltage	V_O	24	V

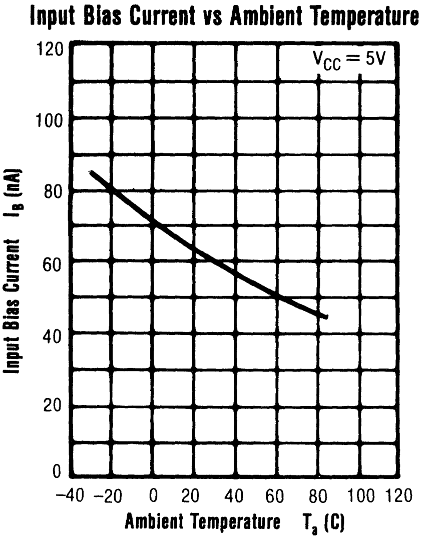
Electrical Characteristics (V_{CC} = 5V, T_a = 25°C)

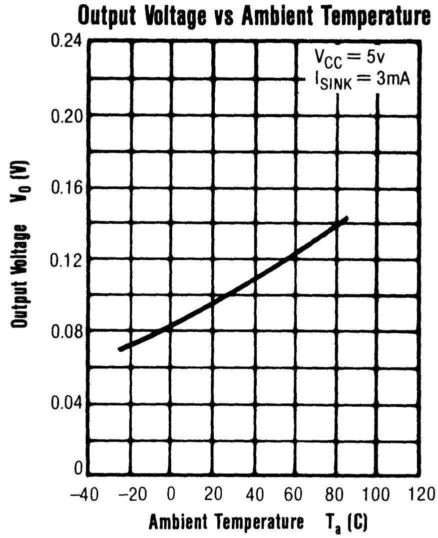
Item	Symbol	Test Circuit	Condition	Limit min.	Limit typ.	Limit max.	Unit
Input Offset Voltage	V_{IO}	1			1	5	mV
Input Offset Current	I_{IO}	1				50	nA
Input Bias Current	I_B	1				250	nA
Voltage Gain	A_{OL}	1	$R_L = 15k\Omega$		200		V/mV
Common-Mode Input Voltage	V_{CM}	2		0		$V_{CC} - 1.5$	V
Response Time	t_R	4	$R_L = 5.1k\Omega$ $V_{RL} = 5V$		1.3		μs
Output Current (Sink)	$I_{O(SINK)}$	5	$V_{REF} = 0V$ $V_{IN} = 1V$ $V_O \leq 1.5V$	10			mA
Output Saturation Voltage	V_{OL}	6	$V_{REF} = 0V$ $V_{IN} = 1V$ $I_{SINK} = 3mA$		0.2	0.4	V
Output Leakage Current	I_{LEAK}	7	$V_{IN} = 0V$ $V_{REF} = 0V$ $V_O = 5V$		0.1		nA
Supply Current	I_{CC}	3	$R_L = \infty$		0.6	1.5	mA

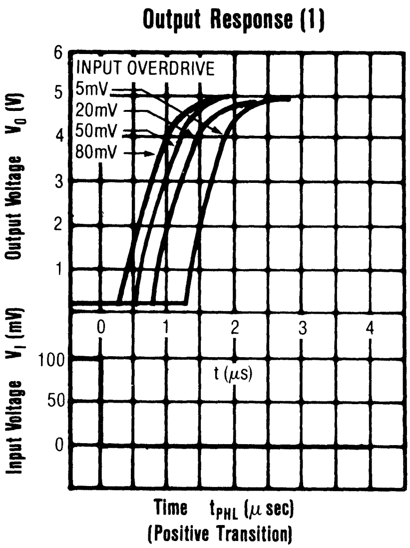
Connection Diagram

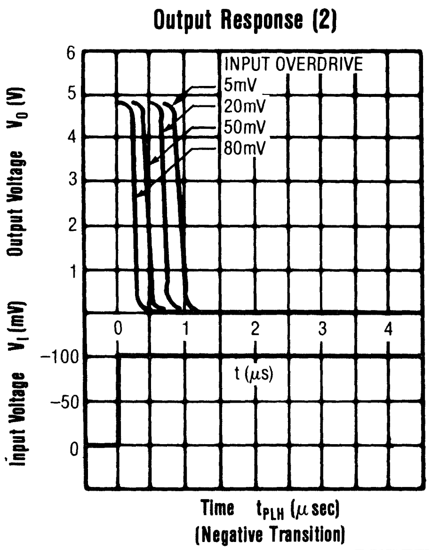


Typical Electrical Performance Curves

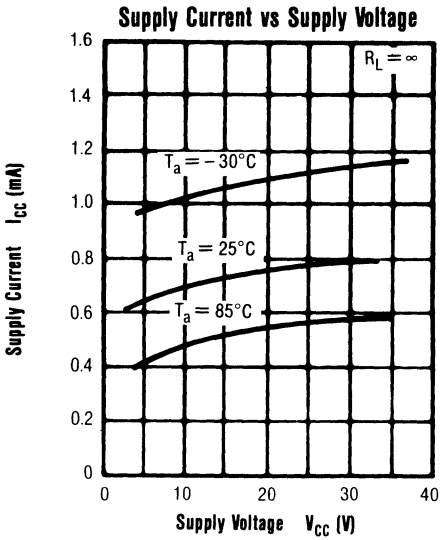


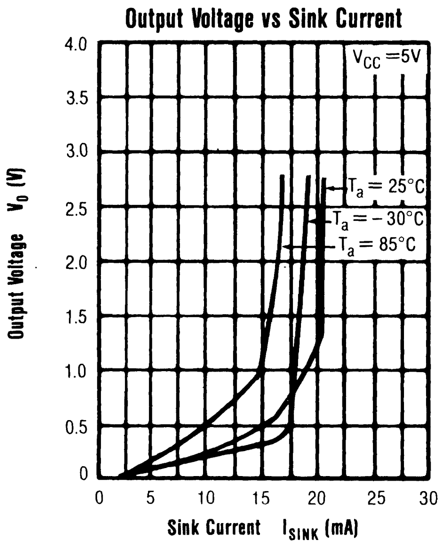




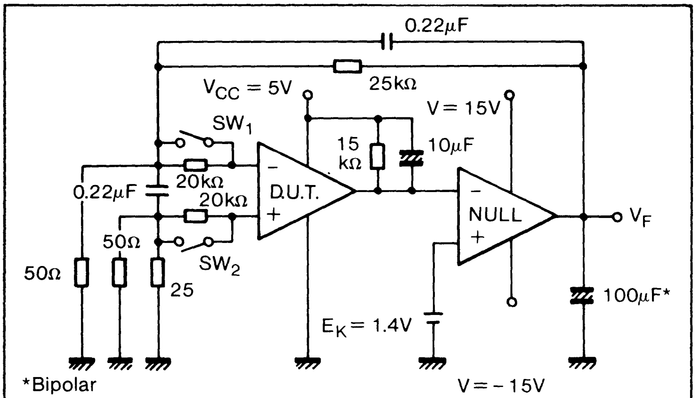


Typical Electrical Performance Curves (continued)

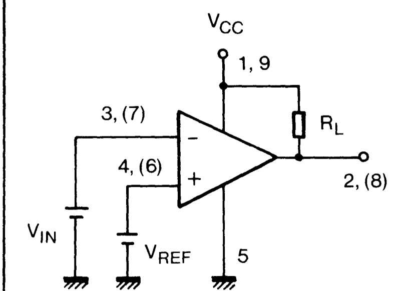




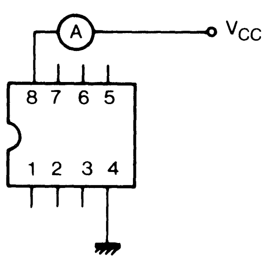
Test Circuit 1 (½ circuit)



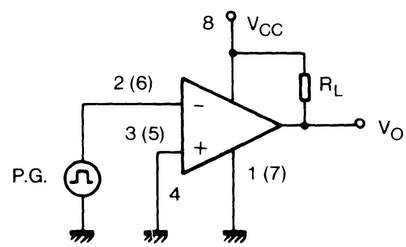
Test Circuit 2 (½ circuit)



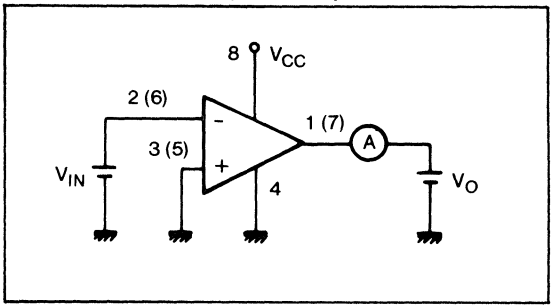
Test Circuit 3



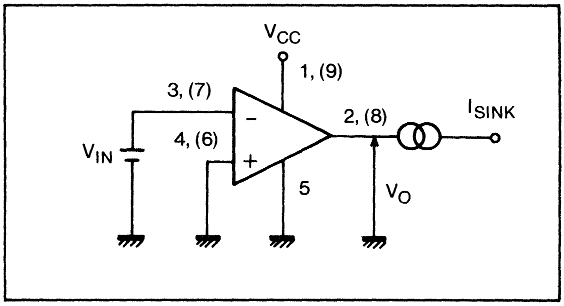
Test Circuit 4 (½ circuit)



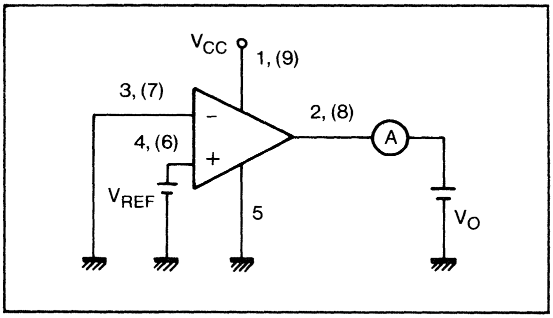
Test Circuit 5 (½ circuit)



Test Circuit 6 (½ circuit)

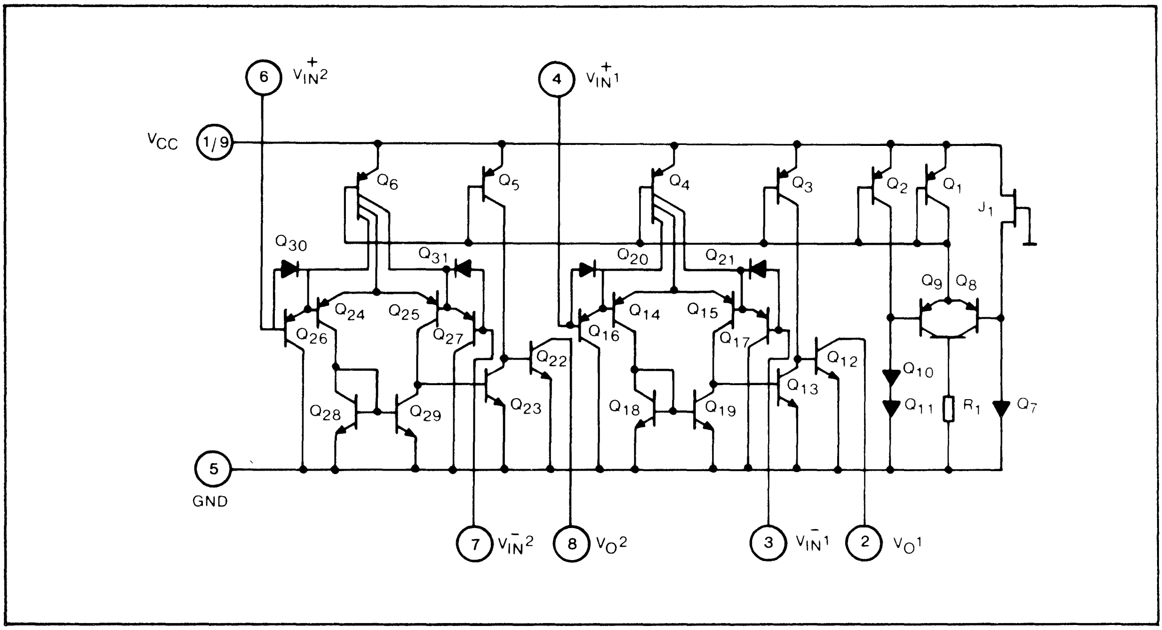


Test Circuit 7 (½ circuit)



Item	Test Conditions For Circuit 1
Input Offset Voltage	With SW1, and SW2 on, V_{F1} is measured. Where $V_{IO} = V_{F1}/500$ (V).
Input Offset Current	With SW1, and SW2 off, V_{F2} is measured. Where $I_M = \left(\frac{V_{F2} - V_{F1}}{10^7} \right)$
Input Bias Current	With SW1 on, and SW2, off, SW2, off, V_{F3} is measured.With SW1 off, and SW2 on, V_{F4} is measured. Where $I_B = \mid V_{F4} - V_{F3} \mid /2 \times 10$ (A)
Voltage Gain	With SW1, and SW2 on, and $E = E_K = 3$ V_{F5} is measured. Where $A_{OL} = \left(\frac{1000}{V_{F1} - V_{F5}} \right)$

Schematic Diagram



AN6915 DUAL COMPARATOR (High Current)

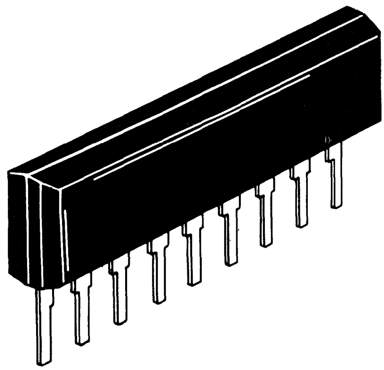
General Description

AN6915 is a dual comparator with high current capability.

Features

- High output sink current (70mA), direct drive of relays or lamps is possible
- Wide supply voltage range: 2 to 36V
- Wide common-mode input voltage range: 0 to V_{CC} - 1.5V
- Open collector output

AN6915



9 - SIP PACKAGE

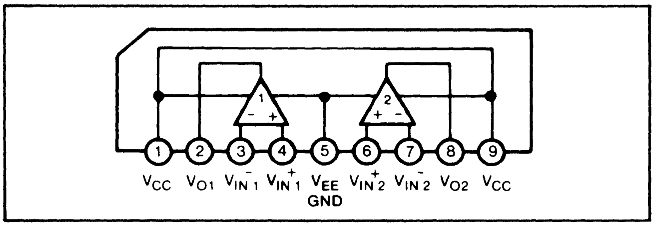
Absolute Maximum Ratings (T_a = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	36	V
Power Dissipation	P_D	500	mW
Input Differential Voltage	V_{ID}	36	V
Input Common –Mode Voltage	V_{ICM}	– 0.3 to + 36	V
Operating Temperature	Topr	– 30 to + 85	°C
Storage Temperature	Tstg	– 55 to +150	°C

Electrical Characteristics (V_{CC} = 5V, T_a = 25°C)

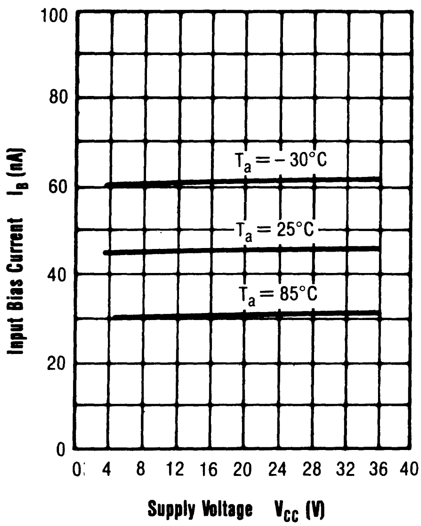
Item	Symbol	Condition	Limit			Unit
			min.	typ.	max.	
Input Offset Voltage	V_{IO}			1	5	mV
Input Offset Current	I_{IO}			1	50	nA
Input Bias Current	I_B			50	250	nA
Voltage Gain	A_{OL}	R_L = 15KΩ		200		V/mV
Common-Mode Input Voltage	V_{CM}		0		V±1.5	V
Response Time	t_R	R_L + 1KΩ		2		μS
Output Current (Sink)	$I_{O(SINK)}$	V_{REF} = 0V, V_{IN} = 1V, V_O = 0.4V	70			mA
Output Saturation Voltage	V_{OL}	V_{REF} = 0V, V_{IN} = 1V, I_{SINK} = 70mA		0.2	0.4	V
Output Leakage Current	I_{LEAK}	V_{REF} = 1V, V_{IN} = 0V, V_O = 5V		0.1		nA
Supply Current	I_{CC}	R_L = ∞		3.8	5.3	mA

Connection Diagram

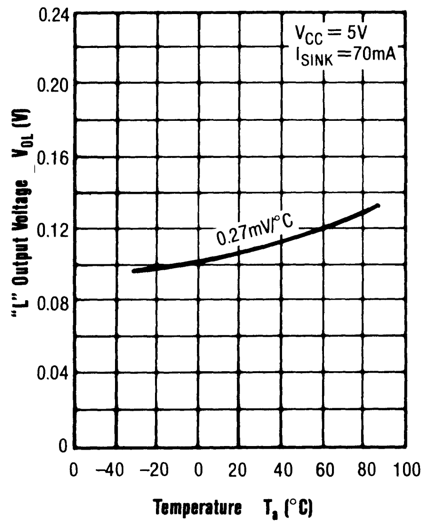


Typical Electrical Performance Curves

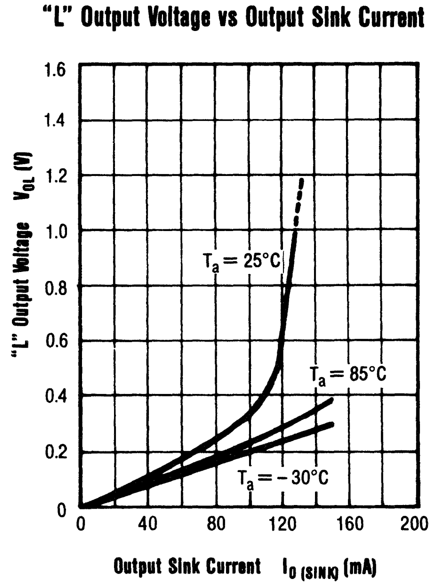
Input Bias Current vs Supply Voltage

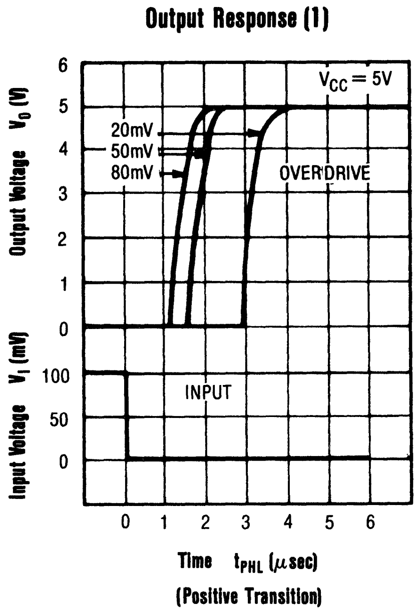


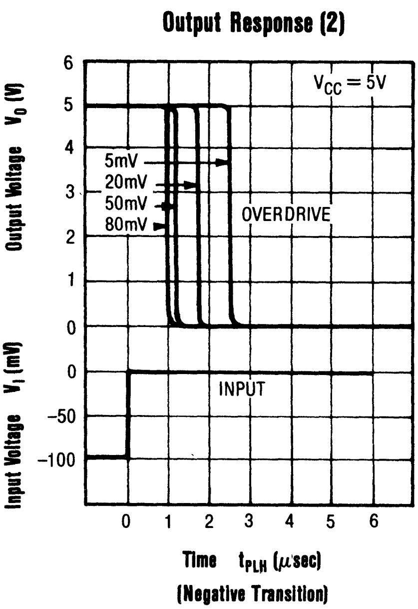
"L" Output Voltage vs Temperature

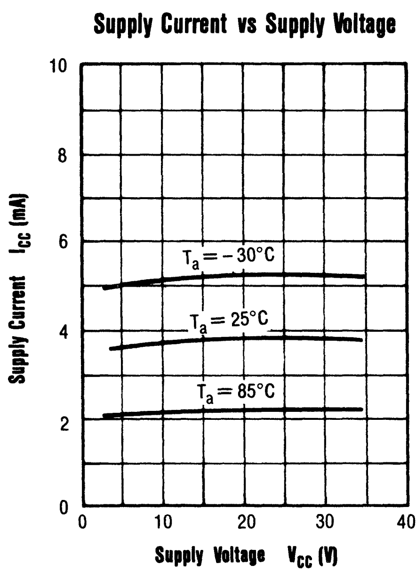


Typical Electrical Performance Curves (continued)

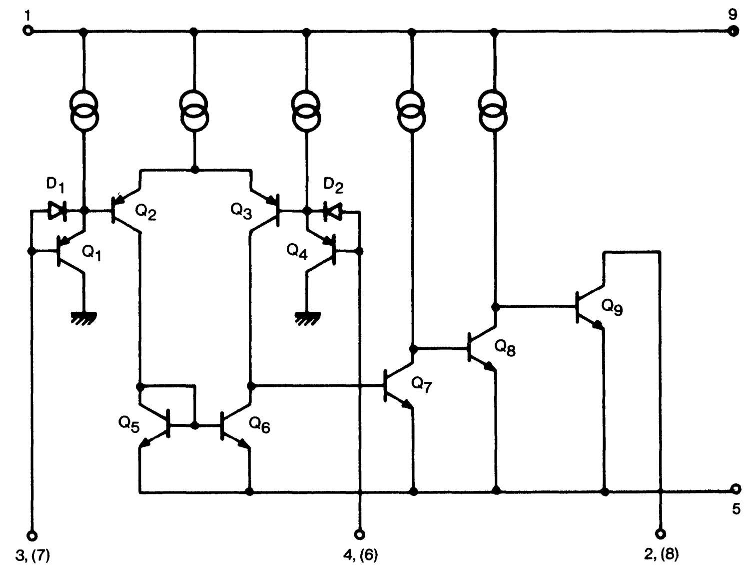








Schematic Diagram



AN6916/AN6916S DUAL COMPARATOR (High Current)

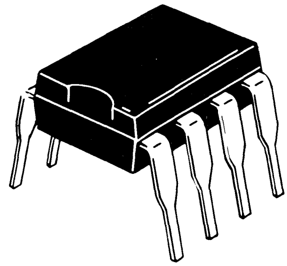
General Description

AN6916 and AN6916S are dual comparators of high current which have wide range of supply voltage.

Features

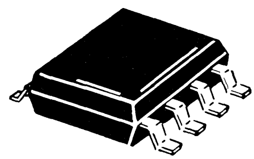
- High output sink current (70mA), direct drive of relays or lamps is possible
- Wide supply voltage range: 2 to 36V
- Wide common-mode input voltage range: 0 to V_{CC} - 1.5V
- Open collector output
- 8 - pin DIP or SO package

AN6916



8 - DIP PACKAGE

AN6916S



SO - 8D PACKAGE

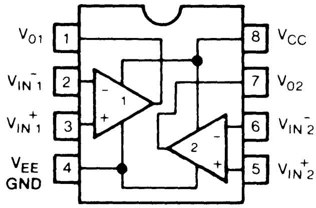
Absolute Maximum Ratings (T_a = 25°C)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{CC}, V_{EE}	36	V
Power Dissipation	(8 DIP)	P_D	500	mW
	(8 SO)	P_D	350	mW
Input Differential Voltage		V_{ID}	36	V
Input Common −Mode Voltage		V_{ICM}	− 0.3 to + 36	V
Operating Temperature		Topr	− 30 to + 85	°C
Storage Temperature		Tstg	− 55 to + 150	°C

Electrical Characteristics (V_{CC} = 5V, T_a = 25°C ± 2°C)

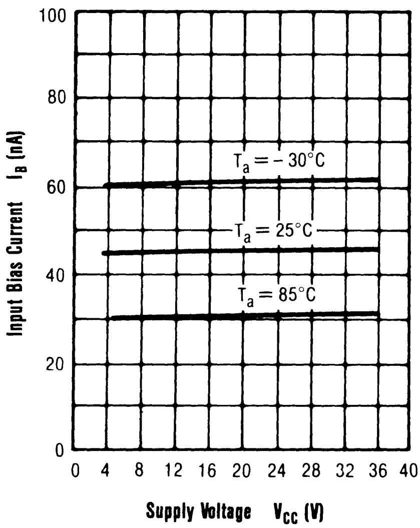
Item	Symbol	Condition	Limit			Unit
			min.	typ.	max.	
Input Offset Voltage	V_{IO}			1	5	mV
Input Offset Current	I_{IO}			1	50	nA
Input Bias Current	I_B			50	250	nA
Voltage Gain	A_{OL}	R_L = 15KΩ		200		V/mV
Common-Mode Input Voltage	V_{CM}		0		V±1.5	V
Response Time	t_R	R_L + 5.1KΩ		2		μS
Output Current (Sink)	$I_{O(SINK)}$	V_{REF} = 0V, V_{IN} = 1V, V_O = 0.4V	70			mA
Output Saturation Voltage	V_{OL}	V_{REF} = 0V, V_{IN} = 1V, I_{SINK} = 70mA		0.2	0.4	V
Output Leakage Current	I_{LEAK}	V_{REF} = 1V, V_{IN} = 0V, V_O = 5V		0.1		nA
Supply Current	I_{CC}	R_L = ∞		3.8	5.3	mA

Connection Diagram

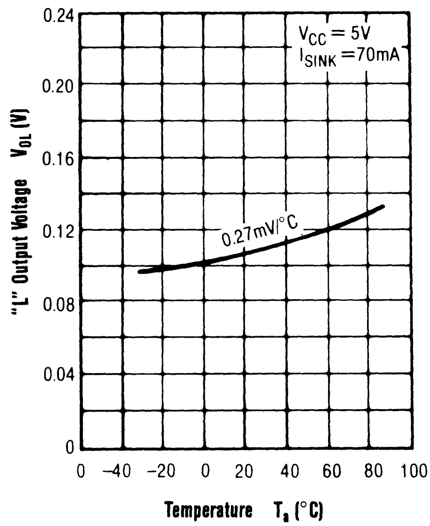


Typical Electrical Performance Curves

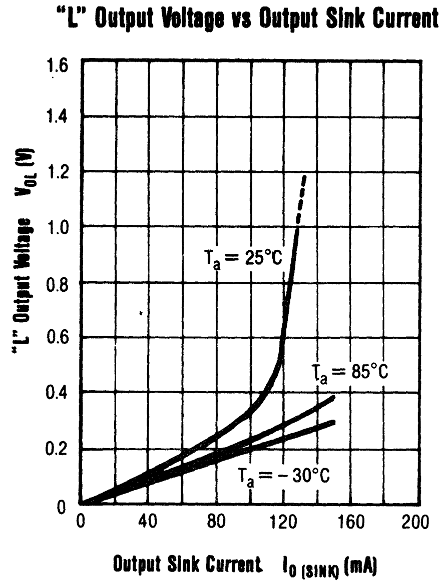
Input Bias Current vs Supply Voltage

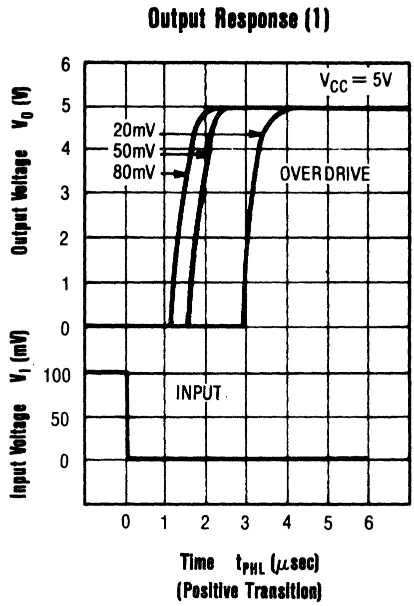


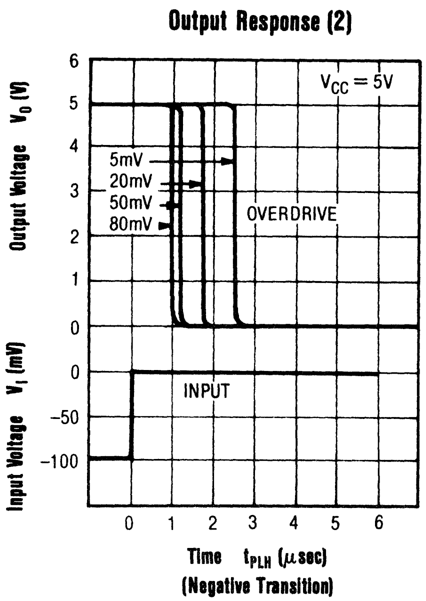
"L" Output Voltage vs Temperature

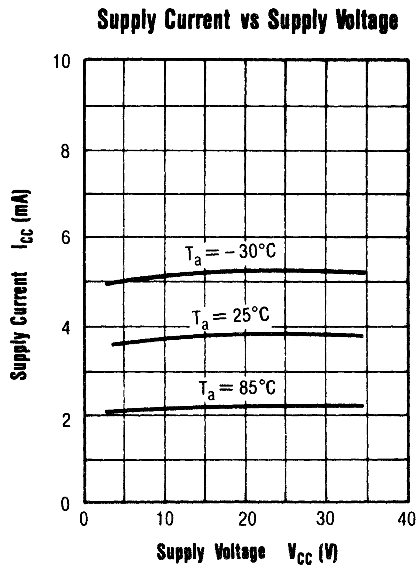


Typical Electrical Performance Curves (continued)

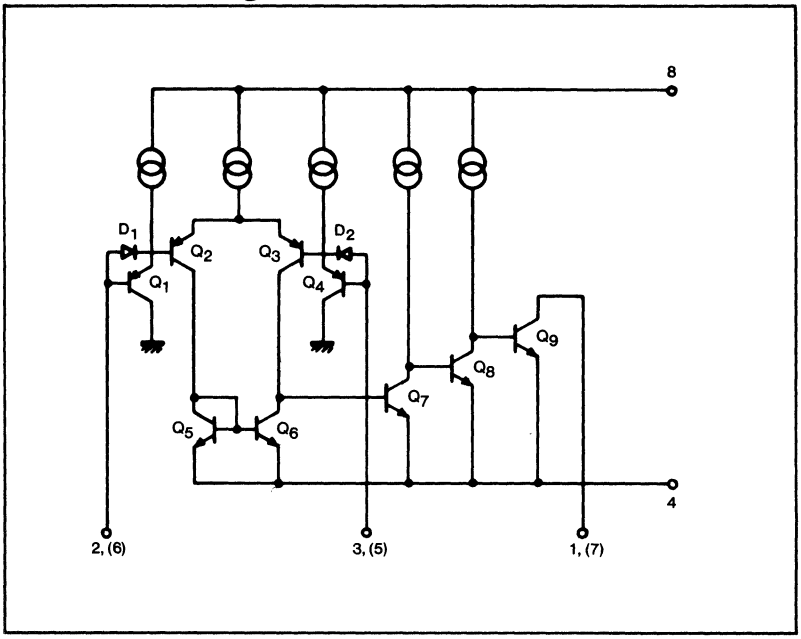








Schematic Diagram

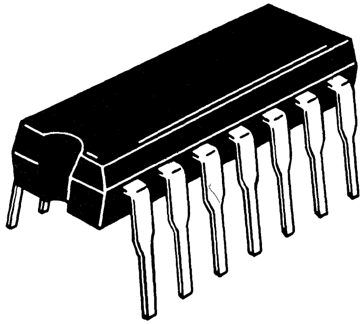


AN6918 QUADRUPLE COMPARATOR (High Current)

General Description

The AN6918 is a quadruple comparator with high current (70mA) capability. It is also pin-compatible with the AN1339.

AN6918



14 - DIP PACKAGE

Features

- A wide range of supply voltage
  Single supply: 2 to 36V
  Dual supply: ± 1 to ± 18V
- Supply current: 11 mA typ.
- Common-mode input voltage: V_{CC} - 1.5V max.

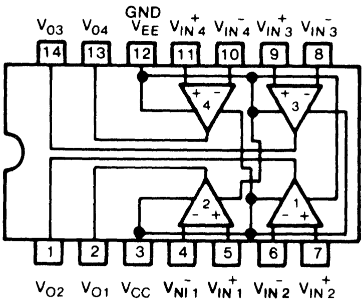
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{CC}	36	V
Power Dissipation	P_D	570	mW
Input Differential Voltage	V_{ID}	36	V
Input Common-Mode Voltage	V_{ICM}	−0.3 to 36	V
Operating Temperature	Topr	−30 to 85	°C
Storage Temperature	Tstg	−55 to 150	°C
Supply Current	I_{CC}	11	mA
Output Voltage (max)	V_O	24	V
Output Sink Current	I_{OL}	150	mA

Electrical Characteristics ($V_{CC} = 5V$, $T_a = 25°C$)

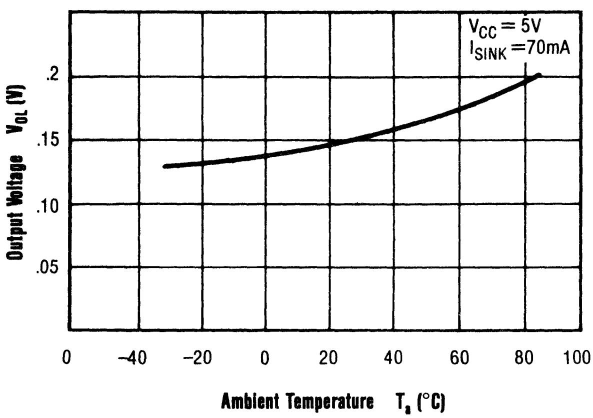
Item	Symbol	Test Circuit	Condition	Limit			Unit
				min.	typ.	max.	
Input Offset Voltage	V_{IO}	3			1	5	mV
Input Offset Current	I_{IO}	3			1	50	nA
Input Bias Current	I_B	3			50	200	nA
Voltage Gain	A_{OL}	3	$R_L = 15k\Omega$		200		V/mV
Common-Mode Input Voltage	V_{CM}	2		0		$V_{CC} - 1.5V$	V
Output Current (Sink)	$I_{O(SINK)}$	5	$V_{REF} = 0V$ $V_{IN} = 1V$ $V_O \leq 0.4V$	70			mA
Output Saturation Voltage	V_{OL}	4	$V_{REF} = 0V$ $V_{IN} = 1V$ $I_{SINK} = 70mA$		0.15	0.4	V
Output Leakage Current	LEAK	7	$V_{REF} = 1V$ $V_{IN} = 0V$ $V_O = 5V$			0.1	nA
Supply Current	I_{CC}	1	$R_L = \infty$ $V_{CC} = 5V$		6.8	10	mA
L, H Propagation Delay Time	t_{PLH}	6	$R_L = 1k\Omega$		2		μs
H, L Propagation Delay Time	t_{PHL}	6	$R_L = 1k\Omega$		1		μs
Zener Voltage	V_Z	8		36		43	

Connection Diagram

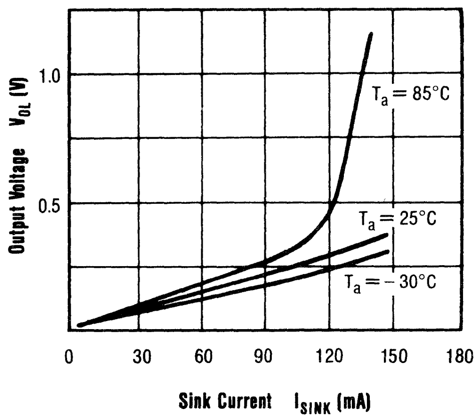


Typical Electrical Performance Curves

Output Voltage vs Output Sink Current

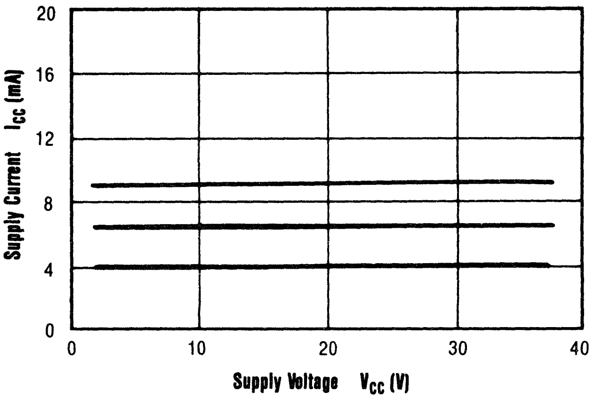


Output Voltage vs Ambient Temperature

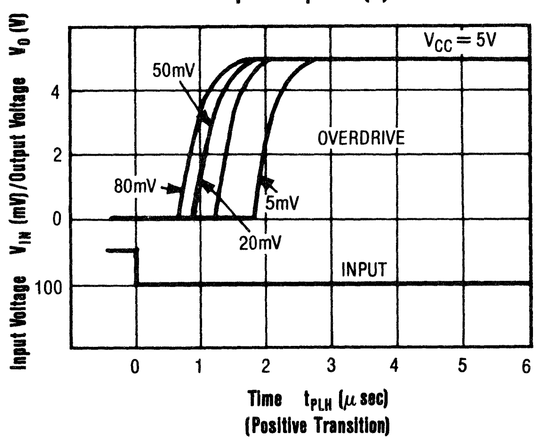


Typical Electrical Performance Curves (continued)

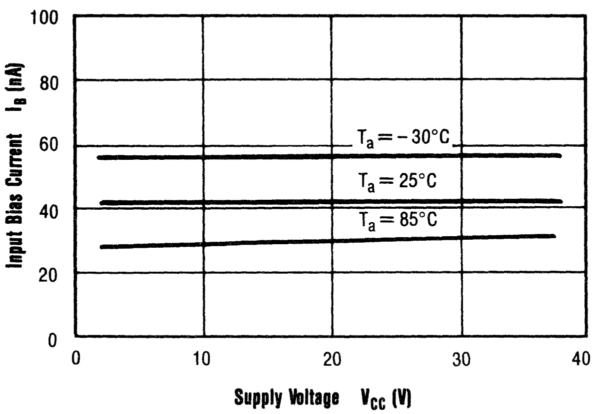
Supply Current vs Supply Voltage



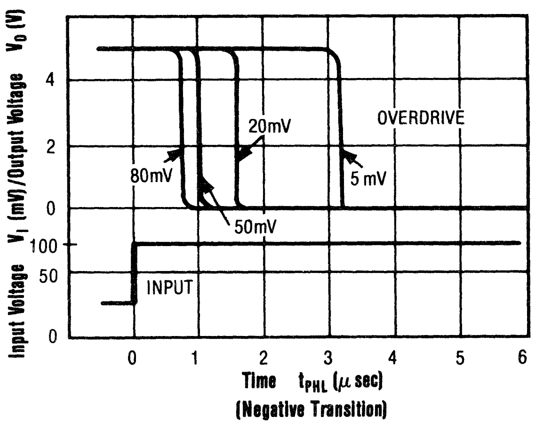
Output Response (1)



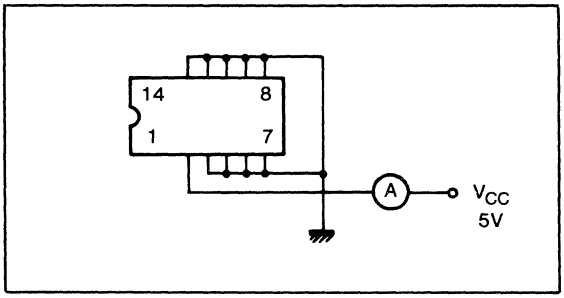
Input Bias Current vs Supply Voltage



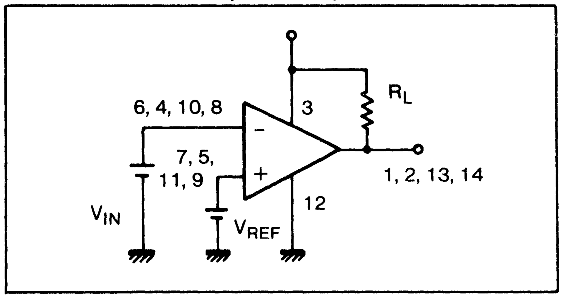
Output Response (2)



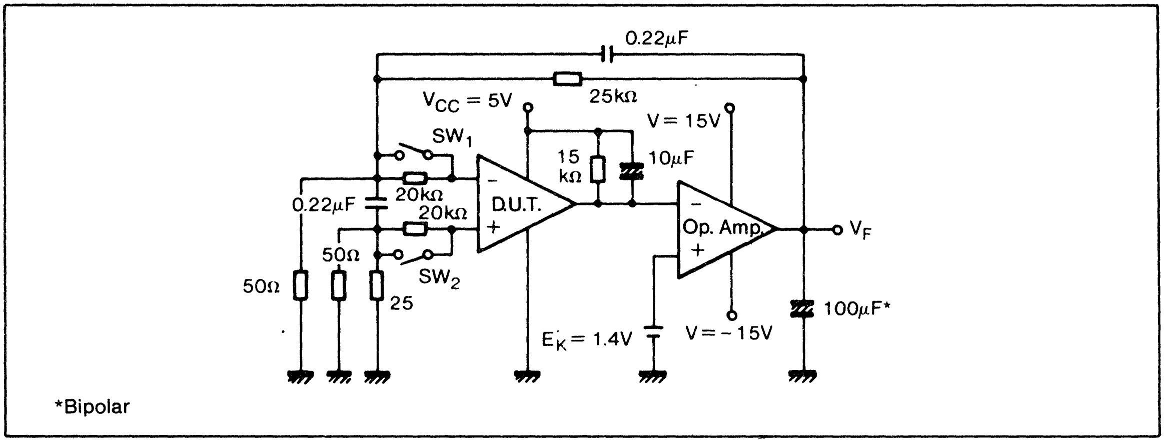
Test Circuit 1



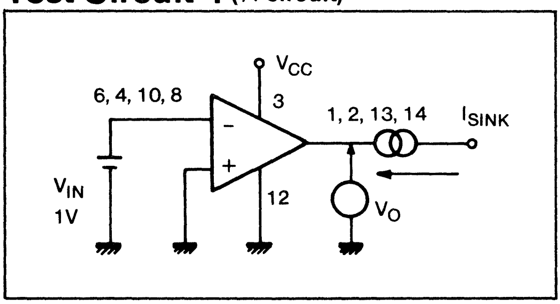
Test Circuit 2 (¼ circuit)



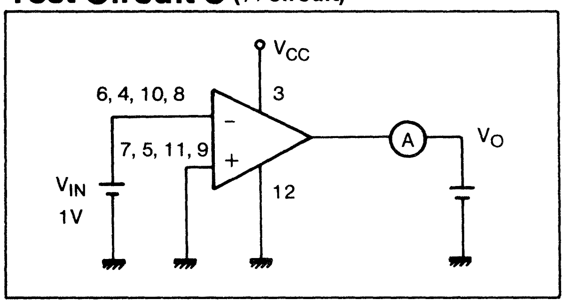
Test Circuit 3 (¼ circuit)



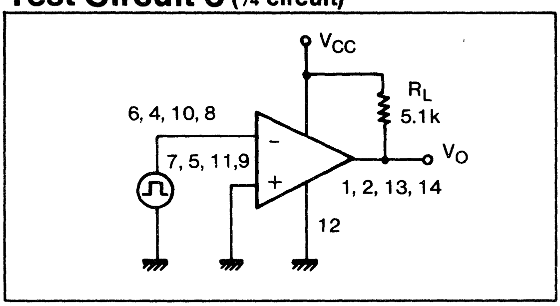
Test Circuit 4 (¼ circuit)



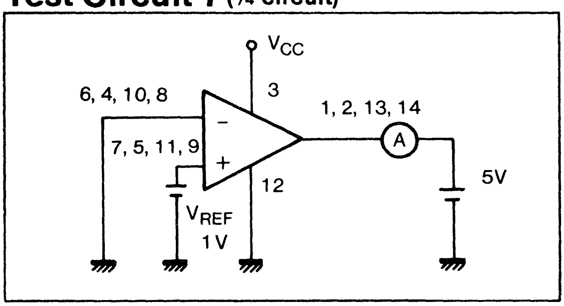
Test Circuit 5 (¼ circuit)



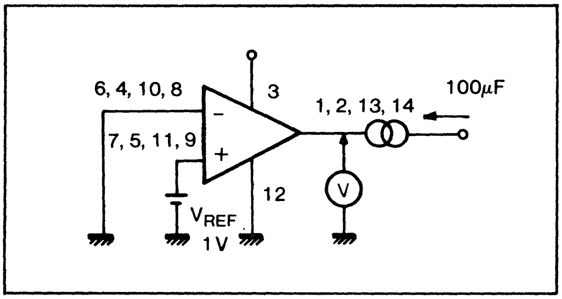
Test Circuit 6 (¼ circuit)



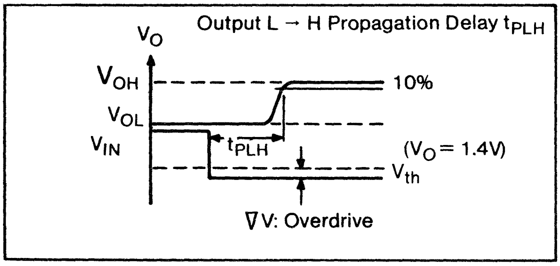
Test Circuit 7 (¼ circuit)

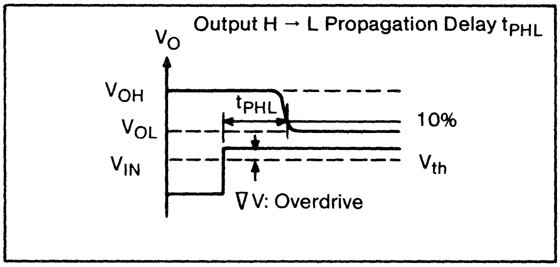


Test Circuit 8 (1/4 circuit)



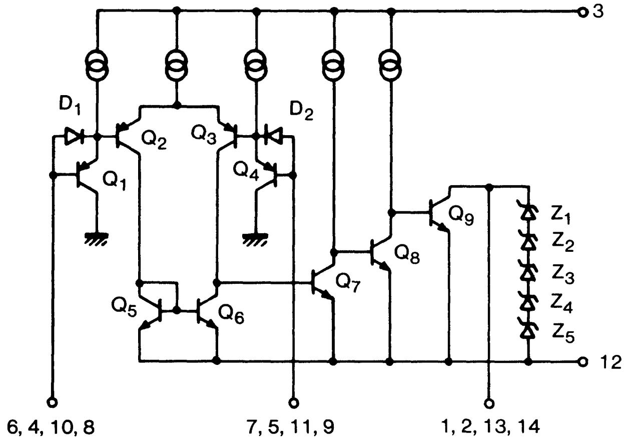
Definition of Response Time (See Test Circuit 6)





Item	Test Condition For Circuit 3
Input Offset Voltage	With SW1, and SW2 on, V_{F1} is measured. Where $V_{IO} = V_{F1}/500$ (V).
Input Offset Current	With SW1, and SW2 off, V_{F2} is measured. Where $I_M = \left(\frac{V_{F2} - V_{F1}}{10^7}\right)$
Input Bias Current	With SW1 on, and SW2, off, SW2, off, V_{F3} is measured.With SW1 off, and SW2 on, V_{F4} is measured. Where $I_B = \lvert V_{F4} - V_{F3} \rvert /2 \times 10$ (A)
Voltage Gain	With SW1, and SW2 on, and $E = E_K = 3$ V_{F5} is measured. Where $A_{OL} = \left(\frac{1000}{V_{F1} - V_{F5}}\right)$

Schematic Diagram

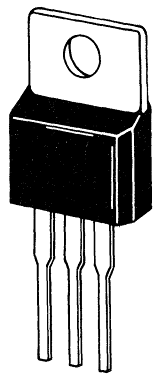


AN7800 SERIES TO-220 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

General Description

Made for long-life reliability, the Panasonic AN7800 Series of 3-terminal Voltage Regulators features internal current limiting, safe area compensation and thermal shutdown for thorough overload and overheating protection. Ideal for use as fixed voltage regulators in a wide variety of applications, the AN7800 Series can also be used with external components when adjustable output voltages and currents are desired. Available in the TO-220 package configuration, the Panasonic series is equivalent to all industry-standard 7800 series voltage regulators.

AN7800 SERIES



TO-220 PACKAGE

Features

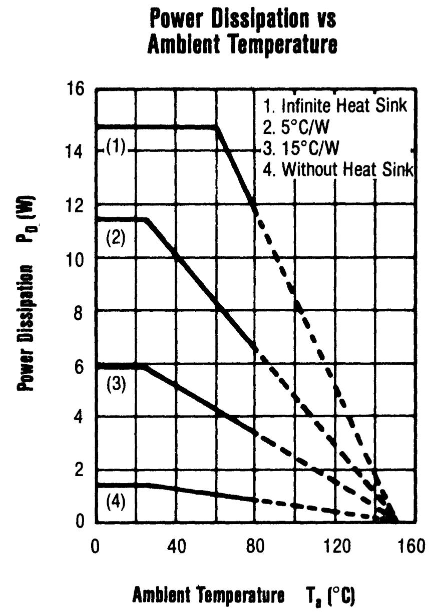
- Output current 1 A max.
- No external components necessary
- Internal thermal overload protection and short circuit current limiting
- Safe area compensation (output transistor)
- TO-220 package
- Output voltages: 5V, 6V, 7V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V

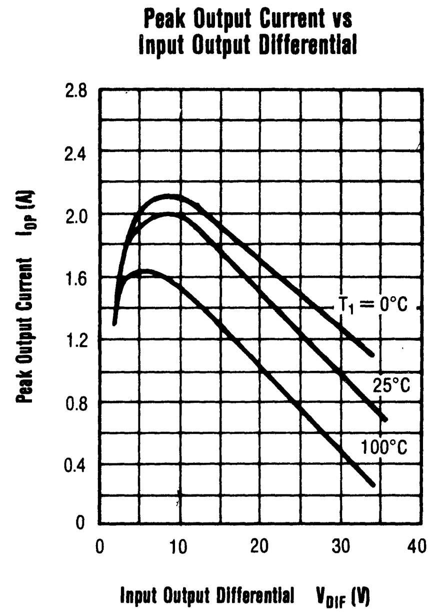
Absolute Maximum Ratings ($T_a = 25°C$)

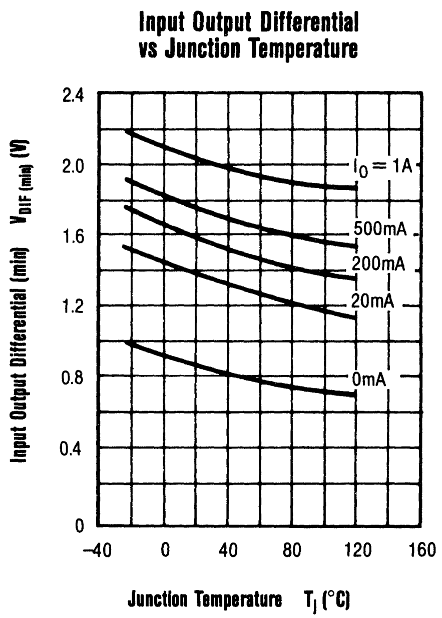
Item	Symbol	Ratings	Unit	Note
Supply Voltage	Vcc,	35	V	2
Power Dissipation	PD	15	W	1
Operating Temperature	Topr	− 20 to 80	°C	
Storage Temperature	Tstg	− 55 to 150	°C	
Supply Current	Io	2000	mA	1

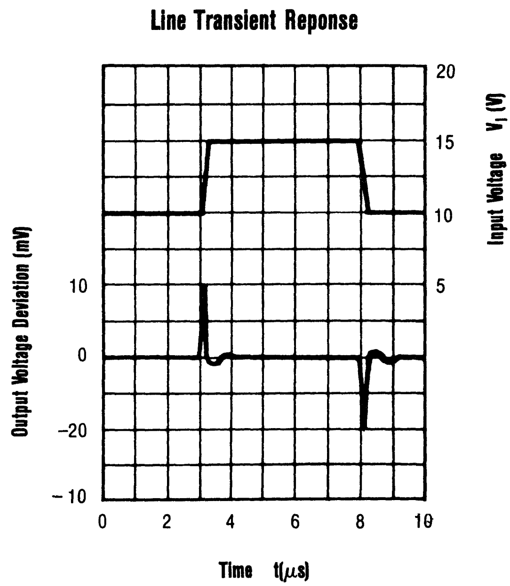
Note 1. At Tj > 150°C, internal circuit shuts off output.
Note 2. Vcc can be 40V for AN7820 and AN7824.

Typical Electrical Performance Curves

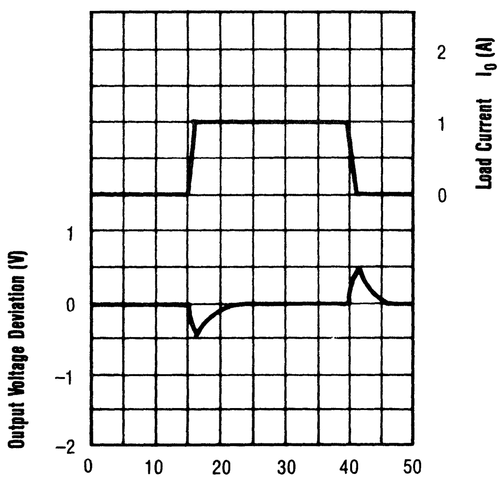


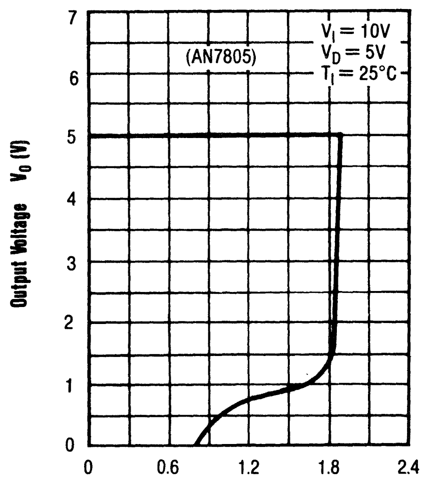




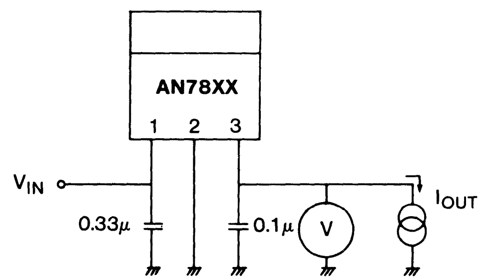


Typical Electrical Performance Curves (continued)



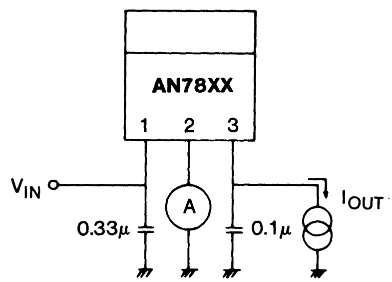


Test Circuit 1



See Note 1.

Test Circuit 2

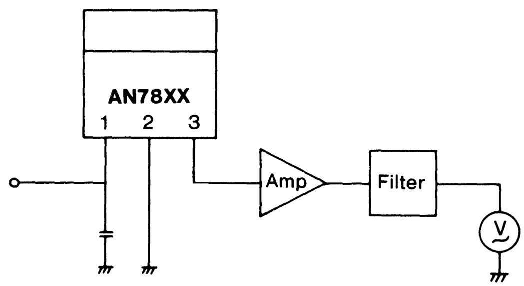


See Note 1.

Notes

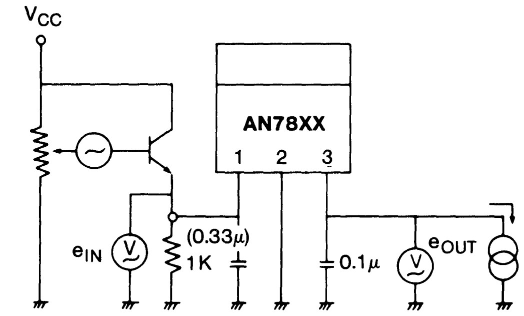
1. Test time should be short (within 10ms) so that the change of characteristics by junction temperature increase can be neglected.
2. Filter is a combination of f_C: 100HZ Secondary Low Pass.
3. $RR = 20 \log (|e_{IN}| / |e_{OUT}|)$
4. Depending on supply block or input voltage, input block may oscillate. In such case, 0.33μ can be eliminated.
5. V_{DIF} is a value when V_{OUT} is 5% lower than specific value by reducing V_{IN}.
6. $Z_{OUT} = |e_{OUT}| \bullet R / |e_{IN}|$
7. From R_L, E_{IN}, D.C. load level should be determined.

Test Circuit 3



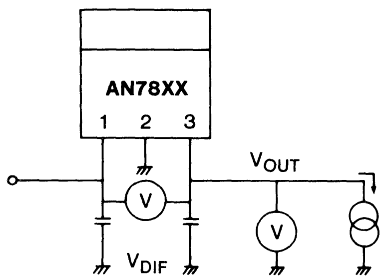
See Note 2.

Test Circuit 4



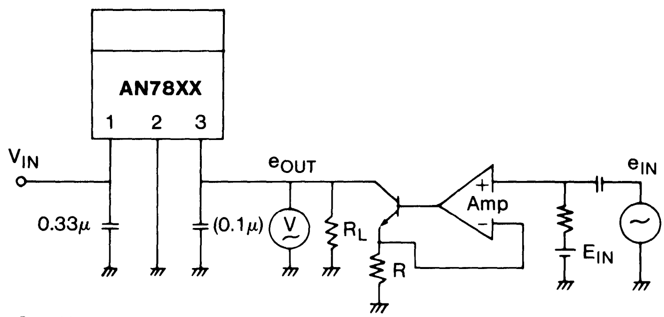
See Notes 3, 4.

Test Circuit 5



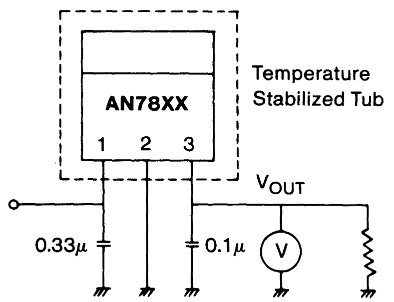
See Notes 1, 5.

Test Circuit 6

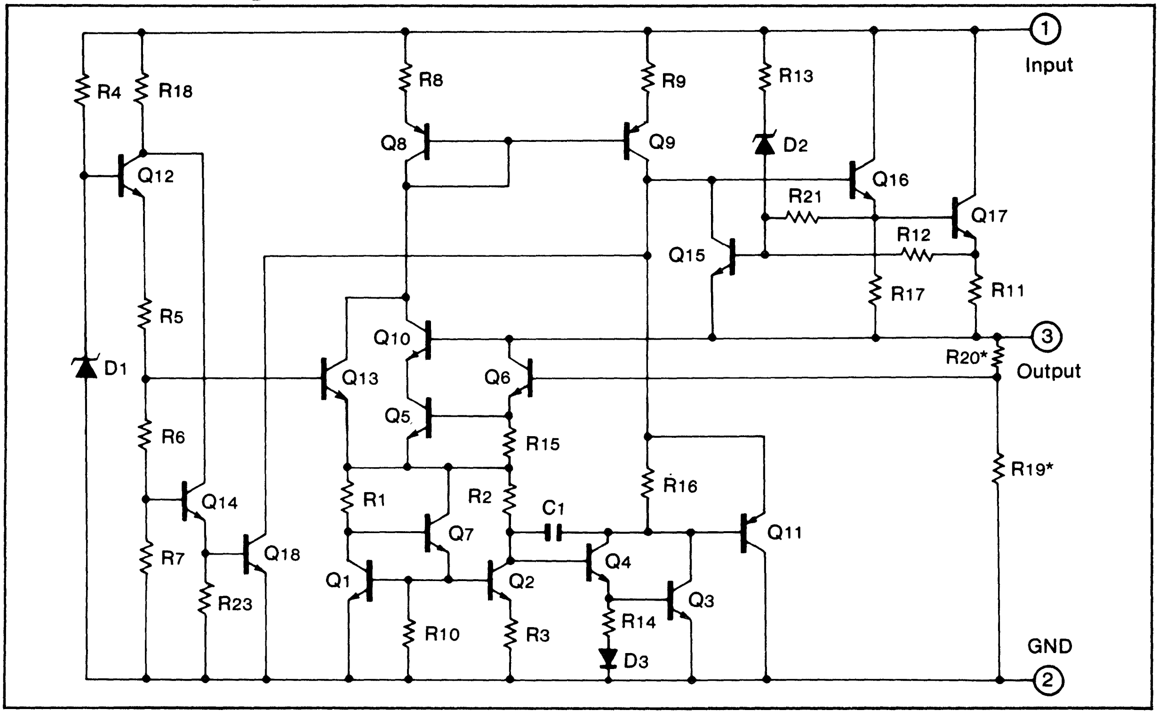


See Notes 6, 7.

Test Circuit 7



Schematic Diagram

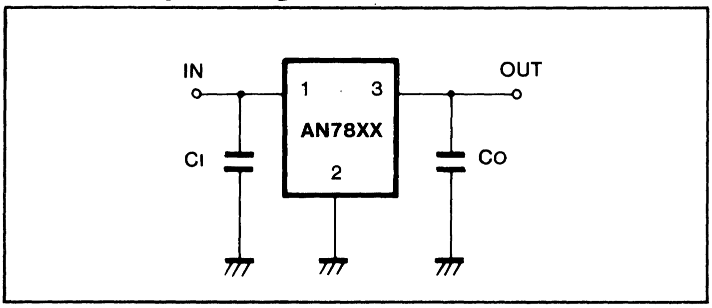


*Refer to table below

	R 19 (Ω)	R 20 (Ω)
AM7805	5K	0
AN7806	5K	1K
AN7807	5K	2K
AN7808	5K	3K
AN7809	5K	4K
AN7810	5K	5K
AN7812	5K	7K
AN7815	5K	10K
AN7818	5K	13K
AN7820	5K	15K
AN7824	5K	19K

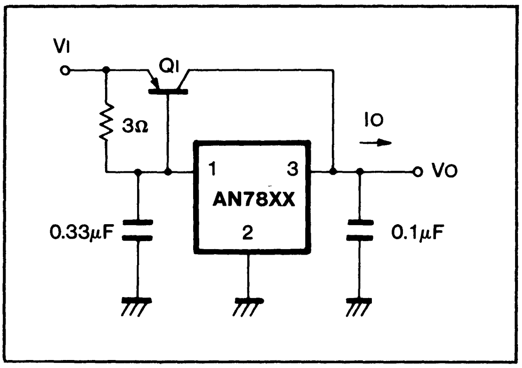
Typical Regulator Applications

Fixed Output Regulator

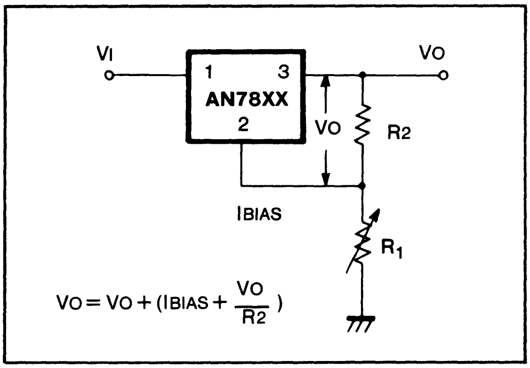


CI: Required if regulator is located an appreciable distance from power supply filter
CO: Although no output capacitor is needed for stability, it does improve transient response

High Current Voltage Regulator



Circuit for Increasing Output Voltage



Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Condition	Limit min	Limit typ	Limit max	Unit
Output Voltage	Vo	1	TJ = 25°C	4.8	5.0	5.2	V
Line Regulation	REG(LINE)	1	7.5V ≤ VI ≤ 25V TJ = 25°C		3	100	mV
			8V ≤ VI ≤ 12V TJ = 25°C		1	50	mV
Load Regulation	REG(LOAD)	1	5mA ≤ Io ≤ 1.5A TJ = 25°C		15	100	mV
			250mA ≤ Io ≤ 750mA TJ = 25°C		5	50	mV
Output Voltage Tolerance		1	8V ≤ VI ≤ 20V TJ = 25°C 5mA ≤ Io ≤ 1A, PD ≤ 15W	4.75	5.0	5.25	V
Quiescent Current	IQ	2	TJ = 25°C		3.9	8.0	mA
Quiescent Current Change (Input)	Δ IQ (LINE)	2	7.5V ≤ VI ≤ 25V TJ = 25°C			1.3	mA
(Output)	Δ IQ (LOAD)		5mA ≤ Io ≤ 1.0mA TJ = 25°C			0.5	mA
Output Noise Voltage	Vn	3	10Hz ≤ f ≤ 100kHz		40		μV
Ripple Rejection	RR	4	f = 120Hz 8V = VI ≤ 18V	62			dB
Dropout Voltage	VI − Vo	5	IOUT = 1.0A TJ = 25°C		2.0		V
Output Impedance	ZOUT	6	f = 1kHz		17		mΩ
Output Short Current	IOS	1	VI = 35V TJ = 25°C		700		mA
Output Peak Current	IOP	1	TJ = 25°C		2.0		A
Output Voltage Temperature Coefficient	Δ V/ Δ T	7	Io = 5mA 0°C ≤ TJ ≤ 125°C		−0.3		mV/°C

Unless specific note is attached, Vn = 10V, Io = 500mA, CI = 0.33μF, Co = 0.1μF, 0°C ≤ TJ ≤ + 125°.

AN7806 TO-220 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	5.75	6.0	6.25	V
Input Stability	REG (LINE)	1	$8.5V \leq V_I \leq 25V$, $T_J = 25°C$		5	120	mV
			$9V \leq V_I \leq 13V$, $T_J = 25°C$		1.5	60	mV
Load Stability	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$, $T_J = 25°C$		14	120	mV
			$250mA \leq I_O \leq 750mA$, $T_J = 25°C$		4	60	mV
Output Voltage Tolerance		1	$9V \leq V_I \leq 25V$, $T_J = 25°C$, $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	5.7	6.0	6.3	V
Bias Current	I_Q	2	$T_J = 25°C$		3.9	8.0	mA
Change of Bias Current (Input)	ΔI_Q (LINE)	2	$8.5V \leq V_I \leq 25V$, $T_J = 25°C$			1.3	mA
〃 〃 (Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1.0A$, $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		40		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$, $9V \leq V_I \leq 19V$	59			dB
Min. Difference of Input and Output Voltage	$V_I - V_O$	5	$I_O = 1A$, $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		17		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$, $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$, $0°C \leq T_J \leq 125°C$		−0.4		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Condition	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	6.7	7.0	7.3	V
Line Regulation	$REG_{(LINE)}$	*1	$9.5V \leq V_I \leq 25V$ $T_J = 25°C$		5	140	mV
			$10V \leq V_I \leq 15V$ $T_J = 25°C$		1.5	70	mV
Load Regulation	$REG_{(LOAD)}$	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		14	140	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	70	mV
Output Voltage Tolerance		1	$10V \leq V_I \leq 23V$ $T_J = 25°C$ $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	6.6	7.0	7.4	V
Quiescent Current	I_Q	2	$T_J = 25°C$		3.9	8.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q(LINE)}$	2	$9.5V \leq V_I \leq 25V$ $T_J = 25°C$			1.0	mA
(Output)	$\Delta I_{Q(LOAD)}$		$5mA \leq I_O \leq 1.0A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		46		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$ $10V \leq V_{IN} \leq 20V$	57			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1.0A$ $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		16		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	7.7	8.0	8.3	V
Line Regulation	$REG_{(LINE)}$	1	$10.5V \leq V_I \leq 25V$, $T_J = 25°C$		6.0	160	mV
			$11V \leq V_I \leq 17V$, $T_J = 25°C$		2.0	80	mV
Load Regulation	$REG_{(LOAD)}$	1	$5mA \leq I_O \leq 1.5A$, $T_J = 25°C$		12	160	mV
			$250mA \leq I_O \leq 750mA$, $T_J = 25°C$		4.0	80	mV
Output Voltage Tolerance		1	$11V \leq V_I \leq 23V$ $T_J = 25°C$, $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	7.6	8.0	8.4	V
Quiescent Current	I_Q	2	$T_J = 25°C$		3.9	8.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q(LINE)}$	2	$10.5V \leq V_I \leq 25V$, $T_J = 25°C$			1.0	mA
(Output)	$\Delta I_{Q(LOAD)}$		$5mA \leq I_O \leq 1.0A$, $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		52		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$, $11.5V \leq V_I \leq 21.5$	56			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1.0A$, $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		16		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$, $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$, $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Condition	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	8.65	9.0	9.35	V
Line Regulation	$REG_{(LINE)}$	1	$11.5V \leq V_I \leq 26V$, $T_J = 25°C$		7	180	mV
			$12V \leq V_I \leq 18V$, $T_J = 25°C$		2	90	mV
Load Regulation	$REG_{(LOAD)}$	1	$5mA \leq I_O \leq 1.5A$, $T_J = 25°C$		12	180	mV
			$250mA \leq I_O \leq 750mA$, $T_J = 25°C$		4	90	mV
Output Voltage Tolerance		1	$12V \leq V_I \leq 24V$ $T_J = 25°C$, $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	8.55	9.0	9.45	V
Quiescent Current	I_Q	2	$T_J = 25°C$		3.9	8.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q(LINE)}$	2	$11.5V \leq V_I \leq 26V$, $T_J = 25°C$			1.0	mA
(Output)	$\Delta I_{Q(LOAD)}$		$5mA \leq I_O \leq 1.0A$, $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		57		V
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$, $12V \leq V_I \leq 22$	56			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1.0A$, $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		16		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$, $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$, $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

AN7810 TO-220 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	9.6	10.0	10.4	V
Line Regulation	REG (LINE)	1	$12.5V \leq V_I \leq 27V$ $T_J = 25°C$		8	200	mV
			$13V \leq V_I \leq 19V$ $T_J = 25°C$		2.5	100	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	200	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	100	mV
Output Voltage Tolerance		1	$13V \leq V_I \leq 25V$, $T_J = 25°C$ $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	9.5	10.0	10.5	V
Quiescent Current	I_Q	2	$T_J = 25°C$		3.9	8.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$12.5V \leq V_I \leq 27V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1.0A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		63		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$ $13V \leq V_I \leq 23V$	56			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1A$ $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		16		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		20		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.6		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

AN7812 TO-220 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Condition	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	11.5	12.0	12.5	V
Line Regulation	$REG_{(LINE)}$	1	$14.5V \leq V_I \leq 30V$ $T_J = 25°C$		10	240	mV
			$16V \leq V_I \leq 22V$ $T_J = 25°C$		3	120	mV
Load Regulation	$REG_{(LOAD)}$	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	240	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4.0	120	mV
Output Voltage Tolerance		1	$15V \leq V_I \leq 27V$ $T_J = 25°C$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	11.4	12.0	12.6	V V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.0	8.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q (LINE)}$	2	$14.5V \leq V_I \leq 30V$ $T_J = 25°C$			1.0	mA
(Output)	$\Delta I_{Q (LOAD)}$		$5mA \leq I_O \leq 1.0A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		75		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$ $15V \leq V_I \leq 25V$	55			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1.0A$ $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1kHz$		18		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–0.8		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Condition	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	14.4	15.0	15.6	V
Line Regulation	$REG_{(LINE)}$	1	$17.5V \leq V_I \leq 30V$ $T_J = 25°C$		11	300	mV
			$20V \leq V_I \leq 26V$ $T_J = 25°C$		3	150	mV
Load Regulation	$REG_{(LOAD)}$	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	300	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	150	mV
Output Voltage Tolerance		1	$18V \leq V_I \leq 30V$ $T_J = 25°C$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	14.25	15.0	15.75	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.0	8.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q (LINE)}$	2	$17.5V \leq V_I \leq 30V$ $T_J = 25°C$			1.0	mA
(Output)	$\Delta I_{Q (LOAD)}$		$5mA \leq I_O \leq 1.0A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		90		μV
Ripple Rejection	RR	4	$f = 120Hz$ $18.5V \leq V_I \leq 28.5V$	54			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1.0A$ $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1kHz$		19		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.0		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Condition	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	17.3	18.0	18.7	V
Line Regulation	$REG_{(LINE)}$	1	$21V \leq V_I \leq 33V$ $T_J = 25°C$			360	mV
			$24V \leq V_I \leq 30V$ $T_J = 25°C$			180	mV
Load Regulation	$REG_{(LOAD)}$	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$			360	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$			180	mV
Output Voltage Tolerance		1	$21V \leq V_I \leq 33V$ $T_J = 25°C$ $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	17.1	18.0	18.9	V
Quiescent Current	I_Q	2	$T_J = 25°C$			8.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q(LINE)}$	2	$21V \leq V_I \leq 33V$ $T_J = 25°C$			1.0	mA
(Output)	$\Delta I_{Q(LOAD)}$		$5mA \leq I_O \leq 1.0A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		110		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$ $22V \leq V_I \leq 32V$	53			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1.0A$ $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		16		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V/\Delta T$	7	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.1		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

AN7820 TO-220 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Condition	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	19.2	20.0	20.8	V
Line Regulation	REG(LINE)	1	$23V \leq V_I \leq 35V$ $T_J = 25°C$		15	400	mV
			$26V \leq V_I \leq 32V$ $T_J = 25°C$		5	200	mV
Load Regulation	REG(LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	400	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	200	mV
Output Voltage Tolerance		1	$24V \leq V_I \leq 35V$ $T_J = 25°C$ $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	19.0	20.0	21.0	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.1	8.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q(LINE)}$	2	$23V \leq V_I \leq 35V$ $T_J = 25°C$			1.0	mA
(Output)	$\Delta I_{Q(LOAD)}$		$5mA \leq I_O \leq 1.0A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		110		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$ $24V \leq V_I \leq 34V$	53			dB
Dropout Voltage	$V_I - V_O$	5	$I_{OUT} = 1.0A$ $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		22		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.2		mV/°C

Unless specific note is attached, $V_n = 10V$, $I_O = 500mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	23.0	24.0	25.0	V
Line Regulation	REG (LINE)	1	$27V \leq V_I \leq 38V$ $T_J = 25°C$		18	480	mV
			$30V \leq V_I \leq 36V$ $T_J = 25°C$		6	240	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	480	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	240	mV
Output Voltage Tolerance		1	$28V \leq V_I \leq 38V$, $T_J = 25°C$ $5mA \leq I_O \leq 1.0A$, $P_D \leq 15W$	22.8		25.2	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.1	8.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$27V \leq V_I \leq 38V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1.0A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	3	$10Hz \leq f \leq 100kHz$		170		μV
Ripple Rejection	RR	4	$f = 120Hz$, $I_O = 100mA$ $28V \leq V_I \leq 38V$	50			dB
Dropout Voltage	$V_I - V_O$	5	$I_O = 1.0A$ $T_J = 25°C$		2.0		V
Output Impedance	Z_{OUT}	6	$f = 1.0kHz$		28		mΩ
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		700		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.0		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	7	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.4		mV/°C

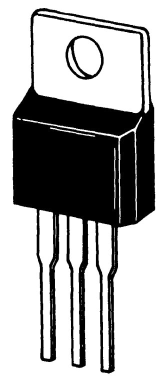
Unless specific note is attached, $V_I = 33V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

AN78M00 SERIES TO-220 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

General Description

Made for long-life reliability, the Panasonic AN78M00 Series of 3-terminal Voltage Regulators features internal current limiting, safe area compensation and thermal shutdown for thorough overload and overheating protection. Ideal for use as fixed voltage regulators in a wide variety of applications, the AN78M00 Series can also be used with external components when adjustable output voltages and currents are desired. Available in the TO-220 package configuration, the Panasonic series is equivalent to all industry-standard 78M00 series voltage regulators.

AN78M00 SERIES



TO-220 PACKAGE

Features

- Output current in excess of 0.5A
- No external components necessary
- Internal thermal overload protection and short circuit current limiting
- Safe area compensation (output transistor)
- TO-220 package
- Output voltages: 5V, 6V, 7V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V

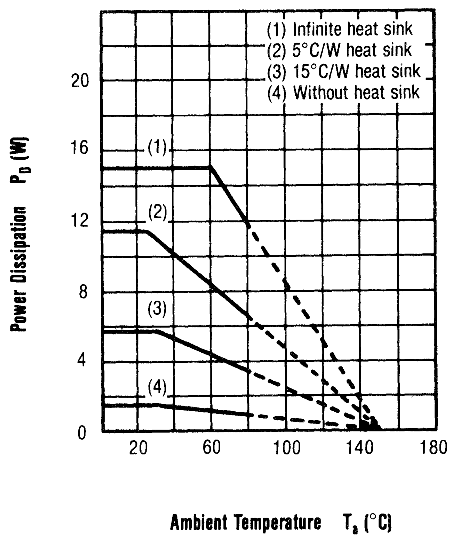
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	Vcc	35* 40**	V	2
Power Dissipation	PD	15	W	1
Operating Temperature	Topr	−20 to 80	°C	
Storage Temperature	Tstg	−55 to 150	°C	

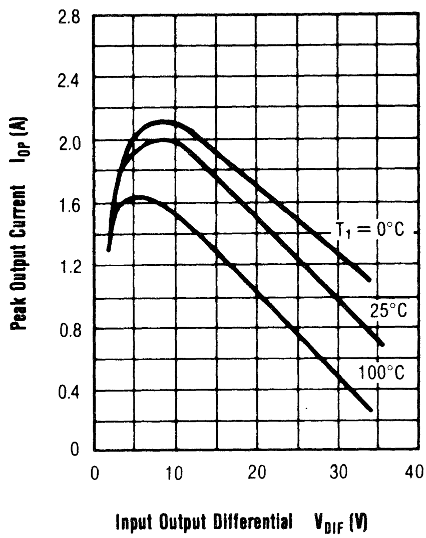
Note 1. The internal circuit cuts off the output at $T_j > 150°C$.
Note 2. * Applicable to 5, 6, 7, 8, 9, 10, 12, 15, 18V.
** Applicable to 20, 24V.

Typical Electrical Performance Curves

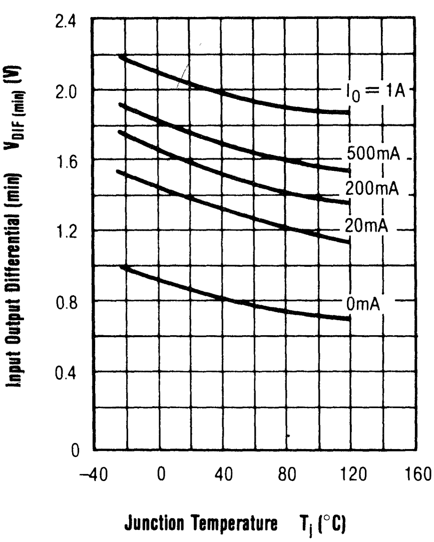
Power Dissipation vs Ambient Temperature



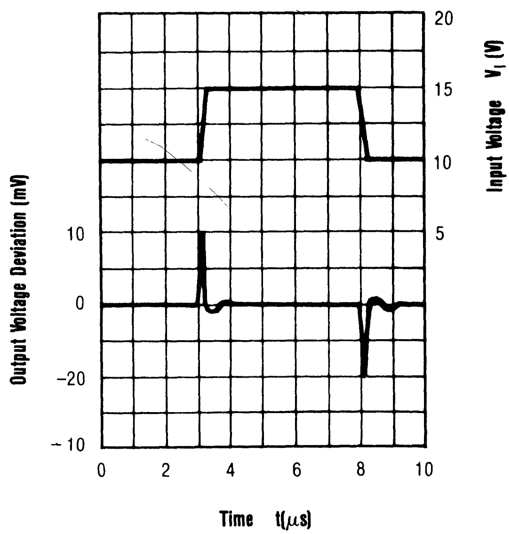
Peak Output Current vs Input Output Differential



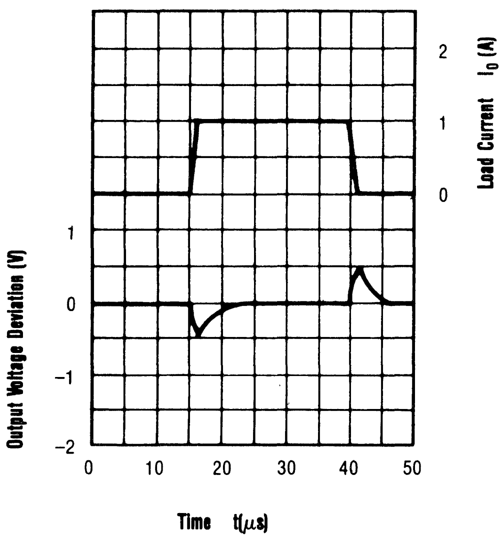
Input Output Differential vs Junction Temperature

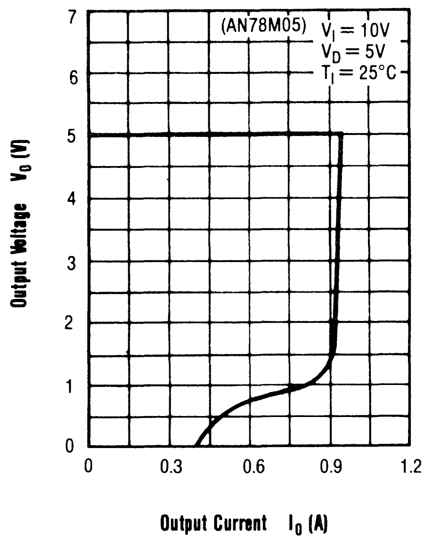


Line Transient Reponse

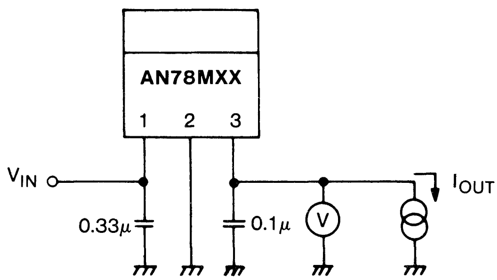


Typical Electrical Performance Curves (continued)



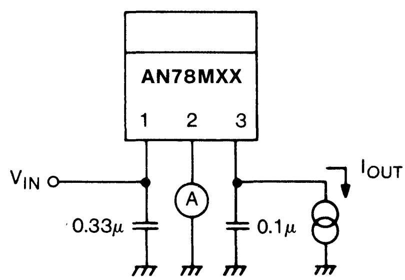


Test Circuit 1



See Note 1.

Test Circuit 2

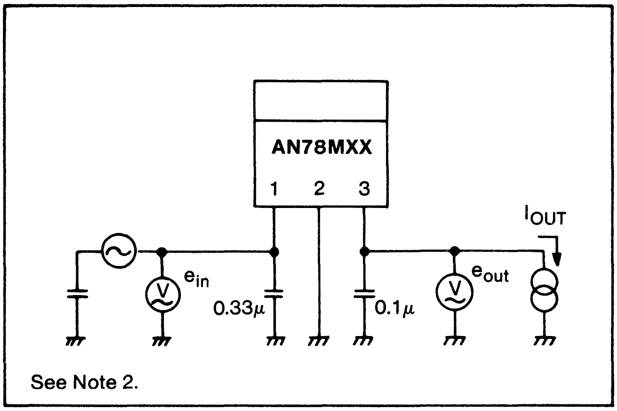


See Note 1.

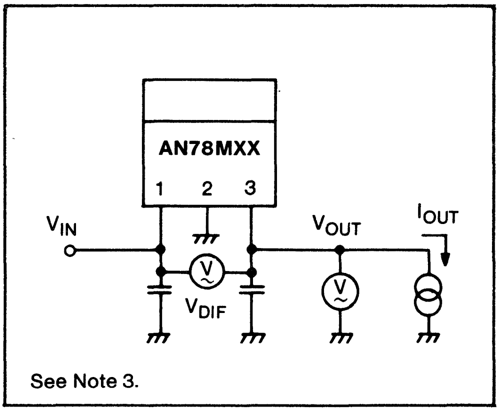
Notes

1. Test period should be short (less than 10ms) so that the change of characteristics by junction temperature increase can be neglected.
2. RR = 20 log (| e_{in} / e_{out} |)
3. V_{DIE} is at the time when V_{OUT} becomes 5% lower than the specified value by decreasing V_{IN}.

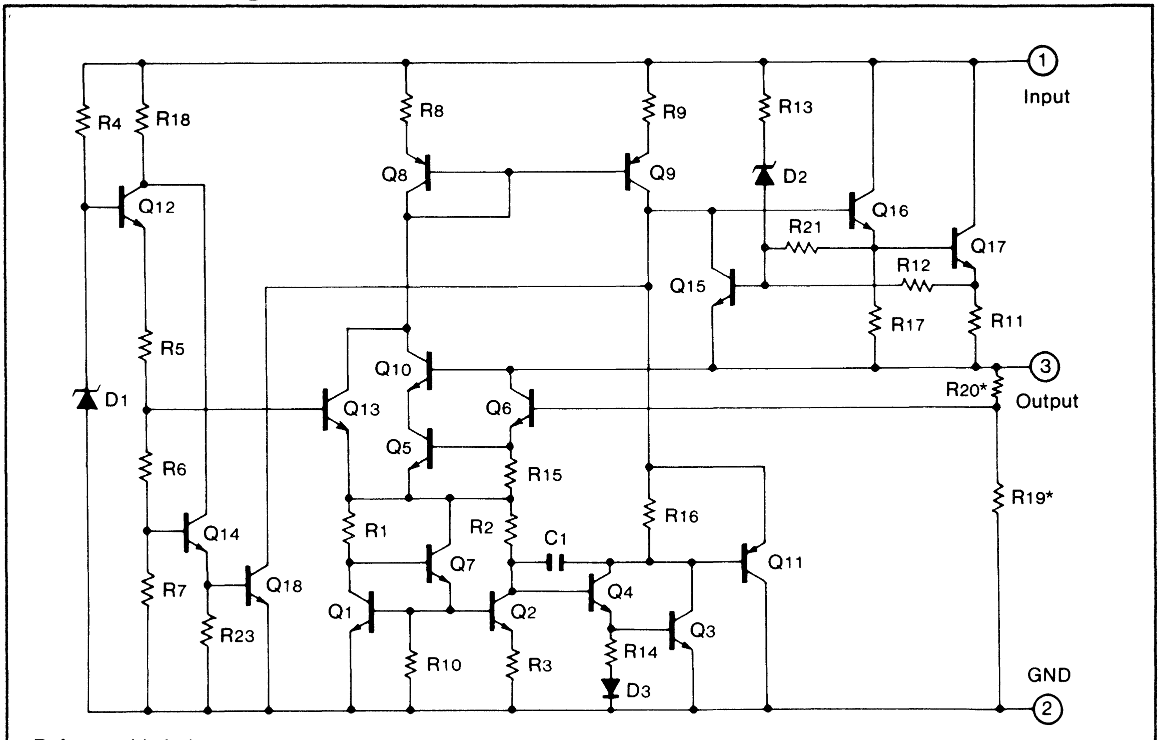
Test Circuit 3



Test Circuit 4



Schematic Diagram



*Refer to table below

	R 19 (Ω)	R 20 (Ω)
AM78M05	5K	0
AN78M06	5K	1K
AN78M07	5K	2K
AN78M08	5K	3K
AN78M09	5K	4K
AN78M10	5K	5K

	R 19 (Ω)	R 20 (Ω)
AN78M12	5K	7K
AN78M15	5K	10K
AN78M18	5K	13K
AN78M20	5K	15K
AN78M24	5K	19K

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	4.8	5.0	5.2	V
Line Regulation	REG (LINE)	1	$7.5V \leq V_I \leq 25V$ $T_J = 25°C$		3	100	mV
			$8V \leq V_I \leq 25V$ $T_J = 25°C$		1	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$ $T_J = 25°C$		20	100	mV
			$5mA \leq I_O \leq 200mA$ $T_J = 25°C$		10	50	mV
Output Voltage Tolerance		1	$7.5V \leq V_I \leq 20V$ $T_J = 25°C$ $5mA \leq I_O \leq 350mA$	4.75	5.0	5.25	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4	6	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$8V \leq V_I \leq 25V$ $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		40		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $8V \leq V_I \leq 18V$	62			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$ $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 25V$ $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_I = 10V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	5.75	6.0	6.25	V
Line Regulation	REG (LINE)	1	$8.5V \le V_I \le 25V$ $T_J = 25°C$		5	100	mV
			$9V \le V_I \le 25V$ $T_J = 25°C$		1.5	50	mV
Load Regulation	REG (LOAD)	1	$5mA \le I_O \le 500mA$ $T_J = 25°C$		20	120	mV
			$5mA \le I_O \le 200mA$ $T_J = 25°C$		10	60	mV
Output Voltage Tolerance		1	$8.5V \le V_I \le 21V$ $T_J = 25°C$ $5mA = I_O = 350mA$	5.7	6.0	6.3	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4	6	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$9V \le V_I \le 25V$ $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \le I_O \le 350mA$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \le f \le 100kHz$		45		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $9V \le V_I \le 19V$	59			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$ $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 25V$ $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \le T_J \le 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_I = 11V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \le T_J \le +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	6.7	7.0	7.3	V
Line Regulation	REG (LINE)	1	$9.5V \leq V_I \leq 25V$, $T_J = 25°C$		6	100	mV
			$10V \leq V_I \leq 25V$, $T_J = 25°C$		2	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$, $T_J = 25°C$		20	140	mV
			$5mA \leq I_O \leq 200mA$, $T_J = 25°C$		10	70	mV
Output Voltage Tolerance		1	$9.5V \leq V_I \leq 22V$ $T_J = 25°C$, $5mA \leq I_O \leq 350mA$	6.65	7.0	7.35	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4	6	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$10V \leq V_I \leq 25V$, $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$, $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		48		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$, $10V \leq V_I \leq 20V$	57			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$, $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 25V$, $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$, $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_I = 12V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	7.7	8.0	8.3	V
Line Regulation	REG (LINE)	1	$10.5V \leq V_I \leq 25V$ $T_J = 25°C$		6	100	mV
			$11V \leq V_I \leq 25V$ $T_J = 25°C$		2	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$ $T_J = 25°C$		25	160	mV
			$5mA \leq I_O \leq 200mA$ $T_J = 25°C$		10	80	mV
Output Voltage Tolerance		1	$10.5V \leq V_I \leq 23V$ $T_J = 25°C$ $5mA = I_O = 350mA$	7.6	8.0	8.4	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.1	6.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$10.5V \leq V_I \leq 25V$ $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		52		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $11.5V \leq V_I \leq 21.5V$	56			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$ $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 25V$ $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_I = 14V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

AN78M09 TO-220 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	8.65	9.0	9.35	V
Line Regulation	REG (LINE)	1	$11.5V \leq V_I \leq 25V$, $T_J = 25°C$		7	100	mV
			$12V \leq V_I \leq 25V$, $T_J = 25°C$		2	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$, $T_J = 25°C$		25	180	mV
			$5mA \leq I_O \leq 200mA$, $T_J = 25°C$		10	90	mV
Output Voltage Tolerance		1	$11.5V \leq V_I \leq 24V$ $T_J = 25°C$, $5mA = I_O = 350mA$	8.55	9.0	9.45	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.1	6.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$12V \leq V_I \leq 25V$, $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$, $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		60		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$, $12V \leq V_I \leq 22V$	56			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$, $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 26V$, $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$, $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_I = 15V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	9.6	10.0	10.4	V
Line Regulation	REG (LINE)	1	$12.5V \leq V_I \leq 30V$ $T_J = 25°C$		7	100	mV
			$13V \leq V_I \leq 25V$ $T_J = 25°C$		2	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$ $T_J = 25°C$		25	200	mV
			$5mA \leq I_O \leq 200mA$ $T_J = 25°C$		10	100	mV
Output Voltage Tolerance		1	$12.5V \leq V_I \leq 25V$ $T_J = 25°C$ $5mA \leq I_O \leq 350mA$	9.5	10.0	10.5	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.1	6.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$13V \leq V_I \leq 25V$ $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		65		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $13V \leq V_I \leq 23V$	56			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$ $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 27V$ $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.5		mV/°C

Unless specific note is attached, $V_I = 15V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	11.5	12.0	12.5	V
Line Regulation	REG (LINE)	1	$14.5V \leq V_I \leq 30V$ $T_J = 25°C$		8	100	mV
			$16V \leq V_I \leq 30V$ $T_J = 25°C$		2	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$ $T_J = 25°C$		25	240	mV
			$5mA \leq I_O \leq 200mA$ $T_J = 25°C$		10	120	mV
Output Voltage Tolerance		1	$14.5V \leq V_I \leq 27V$ $T_J = 25°C$ $5mA \leq I_O \leq 350mA$	11.4	12.0	12.6	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.3	6.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$14.5V \leq V_I \leq 30V$ $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		75		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $15V \leq V_I \leq 25V$	55			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$ $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 30V$ $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.8		mV/°C

Unless specific note is attached, $V_I = 19V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	14.4	15.0	15.6	V
Line Regulation	REG (LINE)	1	$17.5V \leq V_I \leq 30V$, $T_J = 25°C$		10	100	mV
			$20V \leq V_I \leq 30V$, $T_J = 25°C$		3	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$, $T_J = 25°C$		25	300	mV
			$5mA \leq I_O \leq 200mA$, $T_J = 25°C$		10	150	mV
Output Voltage Tolerance		1	$17.5V \leq V_I \leq 30V$ $T_J = 25°C$, $5mA = I_O = 350mA$	14.25	15.0	15.75	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.3	6.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$17.5V \leq V_I \leq 30V$, $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$, $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		90		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$, $18.5V \leq V_I \leq 28V$	54			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$, $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 30V$, $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$, $0°C \leq T_J \leq 125°C$		−1.0		mV/°C

Unless specific note is attached, $V_I = 23V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	17.3	18.0	18.7	V
Line Regulation	$REG_{(LINE)}$	1	$21V \leq V_I \leq 33V$, $T_J = 25°C$		10	100	mV
			$22V \leq V_I \leq 33V$, $T_J = 25°C$		5	50	mV
Load Regulation	$REG_{(LOAD)}$	1	$5mA \leq I_O \leq 500mA$, $T_J = 25°C$		30	360	mV
			$5mA \leq I_O \leq 200mA$, $T_J = 25°C$		10	180	mV
Output Voltage Tolerance		1	$21V \leq V_I \leq 33V$ $T_J = 25°C$, $5mA = I_O = 350mA$	17.1	18.0	18.9	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.4	6.0	mA
Quiescent Current Change (Input)	$\Delta I_{Q(LINE)}$	2	$21V \leq V_I \leq 33V$, $T_J = 25°C$			0.8	mA
(Output)	$\Delta I_{Q(LOAD)}$		$5mA \leq I_O \leq 350mA$, $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		100		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$, $22V \leq V_I \leq 32V$	53			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$, $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 35V$, $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V/\Delta T$	1	$I_O = 5mA$, $0°C \leq T_J \leq 125°C$		−1.0		mV/°C

Unless specific note is attached, $V_I = 27V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit			Unit
				min	typ	max	
Output Voltage	V_O	1	$T_J = 25°C$	19.2	20.0	20.8	V
Line Regulation	REG (LINE)	1	$23V \leq V_I \leq 35V$ $T_J = 25°C$		10	100	mV
			$24V \leq V_I \leq 35V$ $T_J = 25°C$		5	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$ $T_J = 25°C$		30	400	mV
			$5mA \leq I_O \leq 200mA$ $T_J = 25°C$		10	200	mV
Output Voltage Tolerance		1	$23V \leq V_I \leq 35V$ $T_J = 25°C$ $5mA = I_O \leq 350mA$	19	20.0	21	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.4	6.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$23V \leq V_I \leq 35V$ $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		110		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $24V \leq V_I \leq 34V$	53			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$ $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 35V$ $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.0		mV/°C

Unless specific note is attached, $V_I = 29V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit			Unit
				min	typ	max	
Output Voltage	V_O	1	$T_J = 25°C$	23	24	25	V
Line Regulation	REG (LINE)	1	$27V \leq V_I \leq 38V$ $T_J = 25°C$		10	100	mV
			$28V \leq V_I \leq 38V$ $T_J = 25°C$		5	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 500mA$ $T_J = 25°C$		30	480	mV
			$5mA \leq I_O \leq 200mA$ $T_J = 25°C$		10	240	mV
Output Voltage Tolerance		1	$27V \leq V_I \leq 38V$ $T_J = 25°C$ $5mA = I_O = 350mA$	22.8	24.0	25.2	V
Quiescent Current	I_Q	2	$T_J = 25°C$		4.5	6.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$27V \leq V_I \leq 38V$ $T_J = 25°C$			0.8	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 350mA$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		170		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $28V \leq V_I \leq 38V$	50			dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 500mA$ $T_J = 25°C$		2		V
Output Short Current	I_{OS}	1	$V_I = 38V$ $T_J = 25°C$		300		mA
Output Peak Current	I_{OP}	1	$T_J = 25°C$		0.7		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.2		mV/°C

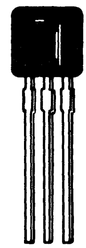
Unless specific note is attached, $V_I = 33V$, $I_O = 350mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

AN78L00 SERIES TO-92 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

General Description

Made for long-life reliability, the Panasonic AN78L00 Series of 3-terminal Voltage Regulators features internal current limiting, safe area compensation and thermal shutdown for thorough overload and overheating protection. Ideal for use as fixed voltage regulators in a wide variety of applications, the AN78L00 Series can also be used with external components when adjustable output voltages and currents are desired. Available in the TO-92 package configuration, the Panasonic series is equivalent to all industry-standard 78L00 series voltage regulators.

AN78L00 SERIES



TO-92 PACKAGE

Features

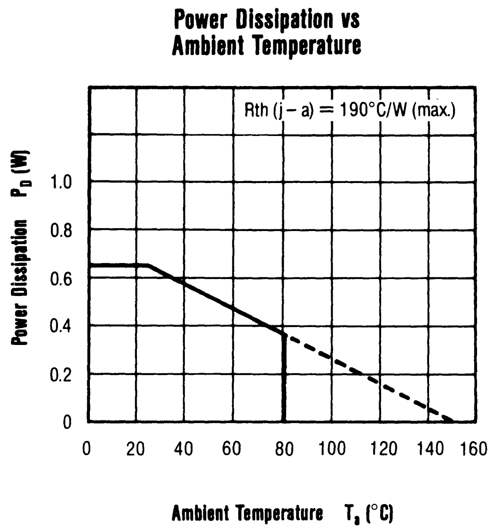
- Output current 100mA max.
- No external components necessary
- Internal thermal overload protection and short circuit current limiting
- TO-92 package
- Output voltages: 4V, 5V, 6V, 7V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V

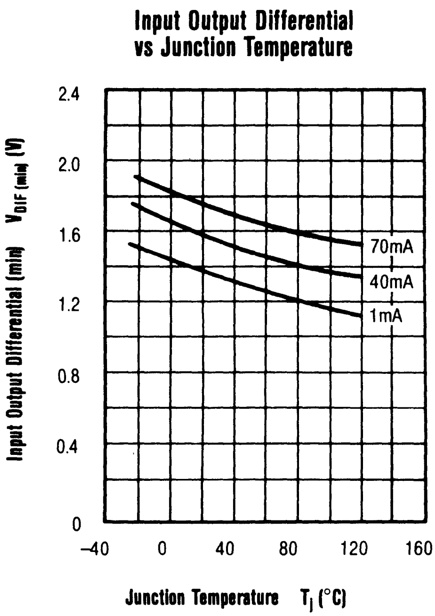
Absolute Maximum Ratings ($T_a = 25°C$)

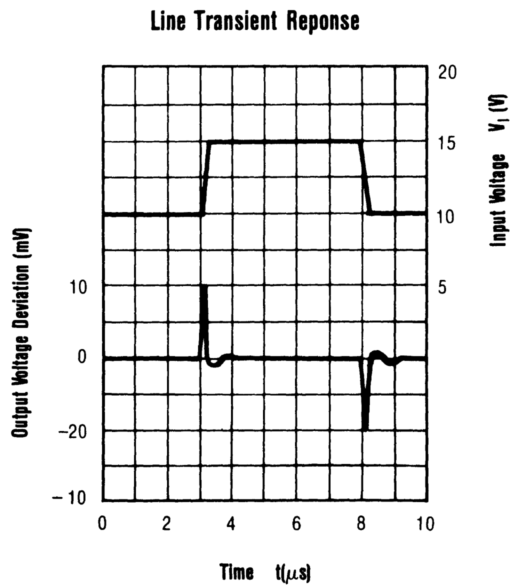
Item	Symbol	Ratings	Unit	Note
Supply Voltage	V_{CC}	35	V	
Power Dissipation	P_D	650	mW	1
Operating Temperature	Topr	−30 to +80	°C	
Storage Temperature	Tstg	−55 to +150	°C	

Note 1. At $T_j > 150°C$, internal circuit shuts off input.

Typical Electrical Performance Curves

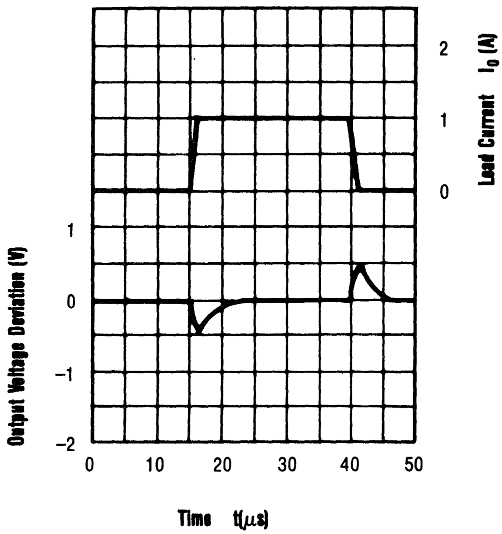




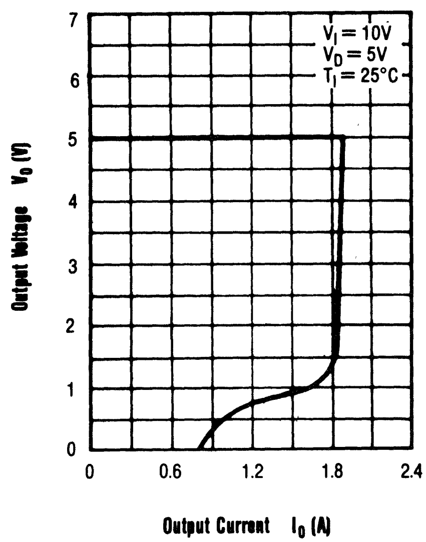


Typical Electrical Performance Curves (continued)

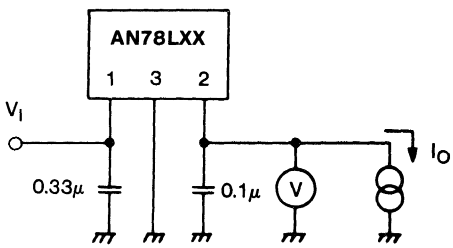
Load Transient Response



Current Limitation Characteristic

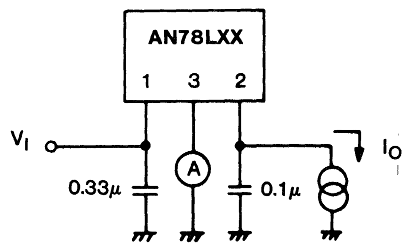


Test Circuit 1



See Note 1.

Test Circuit 2

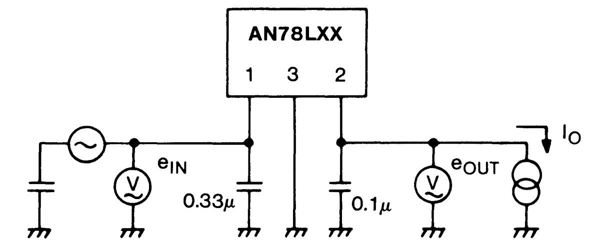


See Note 1.

Notes

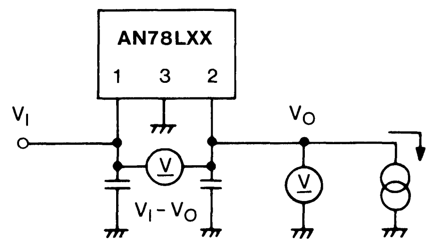
1. Test time should be short (within 10ms) so that the change of characteristics by junction temperature increase can be neglected.
2. $RR = 20 \log (| e_{in} | / | e_{out} |)$
3. $V_I - V_O$ is a value when V_O is 5% lower than specific value by reducing V_I.

Test Circuit 3



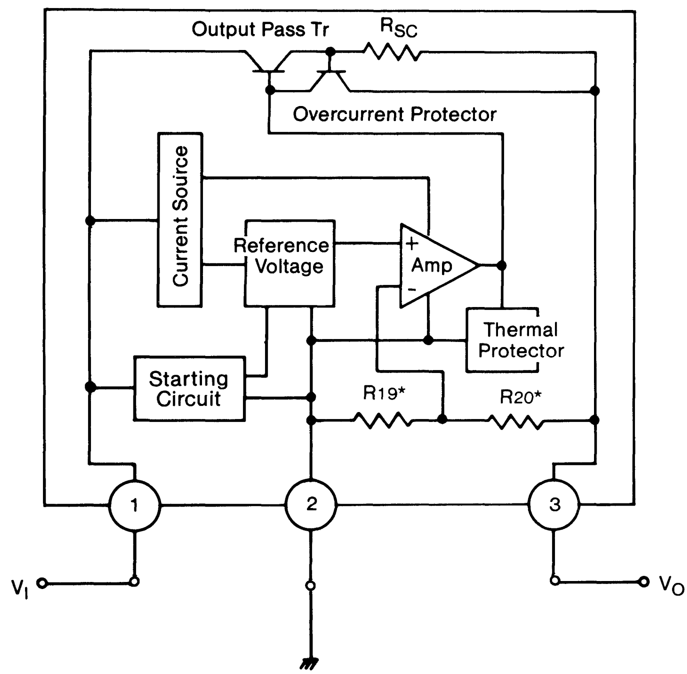
See Note 2.

Test Circuit 4



See Note 1, 3.

Schematic Diagram



*Refer to table

	R 19 (Ω)	R 20 (Ω)
AN78L04	4K	0
AN78L05	4K	1K
AN78L06	4K	2K
AN78L07	4K	3K
AN78L08	4K	4K
AN78L09	4K	5K
AN78L10	4K	6K
AN78L12	4K	8K
AN78L15	4K	11K
AN78L18	4K	14K
AN78l20	3K	12K
AN78L24	3K	15K

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	3.84	4.0	4.16	V
			$6.5V \leq V_I \leq 19V$ $1mA \leq I_O \leq 70mA$	3.8	4.0	4.2	V
Line Regulation	REG (LINE)	1	$6.5V \leq V_I \leq 19V$ $T_J = 25°C$		50	145	mV
			$7V \leq V_I \leq 19V$ $T_J = 25°C$		40	95	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		10	55	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		4.5	30	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$7V \leq V_I \leq 19V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		40		μV
Ripple Rejection	RR	3	$f = 120Hz, I_O = 40mA$ $7V \leq V_I \leq 17V$	48	58		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V/\Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.6		mV/°C

Unless specific note is attached, $V_I = 9V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	4.8	5.0	5.2	V
			$7.5V \leq V_I \leq 20V$ $1mA \leq I_O \leq 70mA$	4.75	5.0	5.25	V
Line Regulation	REG (LINE)	1	$7.5V \leq V_I \leq 20V$ $T_J = 25°C$		55	150	mV
			$8V \leq V_I \leq 20V$ $T_J = 25°C$		45	100	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		11	60	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		5.0	30	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$8V \leq V_I \leq 20V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		40		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $8V \leq V_I \leq 18V$	47	57		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.65		mV/°C

Unless specific note is attached, $V_I = 10V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

AN78L06 TO-92 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	5.76	6.0	6.24	V
			$8.5V \leq V_I \leq 21V$ $1mA \leq I_O \leq 70mA$	5.7	6.0	6.3	V
Line Regulation	REG (LINE)	1	$8.5V \leq V_I \leq 21V$ $T_J = 25°C$		60	155	mV
			$9V \leq V_I \leq 21V$ $T_J = 25°C$		50	105	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		12	65	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		5.5	35	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$9V \leq V_I \leq 21V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		50		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $9V \leq V_I \leq 19V$	46	56		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.7		mV/°C

Unless specific note is attached, $V_I = 11V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	6.72	7.0	7.28	V
			$9.5V \leq V_I \leq 22V$ $1mA \leq I_O \leq 70mA$	6.65	7.0	7.35	V
Line Regulation	REG (LINE)	1	$9.5V \leq V_I \leq 22V$ $T_J = 25°C$		70	165	mV
			$10V \leq V_I \leq 22V$ $T_J = 25°C$		60	115	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		13	75	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		6.0	35	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$10V \leq V_I \leq 22V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		50		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $10V \leq V_I \leq 20V$	45	55		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.75		mV/°C

Unless specific note is attached, $V_I = 12V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	7.7	8.0	8.3	V
			$10.5V \leq V_I \leq 23V$ $1mA \leq I_O \leq 70mA$	7.6	8.0	8.4	V
Line Regulation	REG (LINE)	1	$10.5V \leq V_I \leq 23V$ $T_J = 25°C$		80	175	mV
			$11V \leq V_I \leq 23V$ $T_J = 25°C$		70	125	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		15	80	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		7.0	40	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$11V \leq V_I \leq 23V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		60		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $11V \leq V_I \leq 21V$	44	54		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.8		mV/°C

Unless specific note is attached, $V_I = 14V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

AN78L09 TO-92 PACKAGE 3-TERMINAL VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	8.64	9.0	9.36	V
			$11.5V \leq V_I \leq 24V$ $1mA \leq I_O \leq 70mA$	8.55	9.0	9.45	V
Line Regulation	REG (LINE)	1	$11.5V \leq V_I \leq 24V$ $T_J = 25°C$		90	190	mV
			$12V \leq V_I \leq 24V$ $T_J = 25°C$		80	140	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		16	85	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		8.0	45	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$12V \leq V_I \leq 24V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		65		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $12V \leq V_I \leq 22V$	43	53		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.85		mV/°C

Unless specific note is attached, $V_I = 15V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	9.6	10.0	10.4	V
			$12.5V \leq V_I \leq 25V$ $1mA \leq I_O \leq 70mA$	9.5	10.0	10.5	V
Line Regulation	REG (LINE)	1	$12.5V \leq V_I \leq 25V$ $T_J = 25°C$		100	210	mV
			$13V \leq V_I \leq 25V$ $T_J = 25°C$		90	160	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		17	90	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		9.0	45	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$13V \leq V_I \leq 25V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		70		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $13V \leq V_I \leq 23V$	42	52		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–0.9		mV/°C

Unless specific note is attached, $V_I = 16V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	11.5	12.0	12.5	V
			$14.5V \leq V_I \leq 27V$ $1mA \leq I_O \leq 70mA$	11.4	12.0	12.6	V
Line Regulation	REG (LINE)	1	$14.5V \leq V_I \leq 27V$ $T_J = 25°C$		120	250	mV
			$15V \leq V_I \leq 27V$ $T_J = 25°C$		100	200	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		20	100	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		10	50	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.5	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$15V \leq V_I \leq 27V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		80		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $15V \leq V_I \leq 25V$	40	50		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.0		mV/°C

Unless specific note is attached, $V_I = 19V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	14.4	15.0	15.6	V
			$17.5V \leq V_I \leq 30V$ $1mA \leq I_O \leq 70mA$	14.3	15.0	15.8	V
Line Regulation	REG (LINE)	1	$17.5V \leq V_I \leq 30V$ $T_J = 25°C$		130	300	mV
			$18V \leq V_I \leq 30V$ $T_J = 25°C$		110	250	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		25	150	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		12	75	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.5	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$18V \leq V_I \leq 30V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		90		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $18V \leq V_I \leq 28V$	38	48		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.3		mV/°C

Unless specific note is attached, $V_I = 23V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	17.3	18.0	18.7	V
			$20.5V \leq V_I \leq 33V$ $1mA \leq I_O \leq 70mA$	17.1	18.0	18.9	V
Line Regulation	REG (LINE)	1	$20.5V \leq V_I \leq 33V$ $T_J = 25°C$		45	300	mV
			$21V \leq V_I \leq 33V$ $T_J = 25°C$		35	250	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		30	170	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		15	85	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.5	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$21V \leq V_I \leq 33V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		150		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $21V \leq V_I \leq 31V$	36	46		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.5		mV/°C

Unless specific note is attached, $V_I = 27V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	19.2	20.0	20.8	V
			$22.5V \leq V_I \leq 35V$ $1mA \leq I_O \leq 70mA$	19.0	20.0	21.0	V
Line Regulation	REG (LINE)	1	$22.5V \leq V_I \leq 35V$ $T_J = 25°C$		50	300	mV
			$23V \leq V_I \leq 35V$ $T_J = 25°C$		40	250	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		35	180	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		17	90	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.5	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$23V \leq V_I \leq 35V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		170		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $23V \leq V_I \leq 33V$	34	44		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.7		mV/°C

Unless specific note is atttached, $V_I = 29V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	23.0	24.0	25.0	V
			$26.5V \leq V_I \leq 39V$ $1mA \leq I_O \leq 70mA$	22.8	24.0	25.2	V
Line Regulation	REG (LINE)	1	$26.5V \leq V_I \leq 39V$ $T_J = 25°C$		60	300	mV
			$27V \leq V_I \leq 39V$ $T_J = 25°C$		50	250	mV
Load Regulation	REG (LOAD)	1	$1mA \leq I_O \leq 100mA$ $T_J = 25°C$		40	200	mV
			$1mA \leq I_O \leq 40mA$ $T_J = 25°C$		20	100	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	3.5	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$27V \leq V_I \leq 39V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$1mA \leq I_O \leq 40mA$ $T_J = 25°C$			0.1	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		200		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 40mA$ $27V \leq V_I \leq 37V$	34	44		dB
Dropout Voltage	$V_I - V_O$	4	$T_J = 25°C$		1.7		V
Output Short Current	I_{OS}	1	$T_J = 25°C$		140		mA
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−2.0		mV/°C

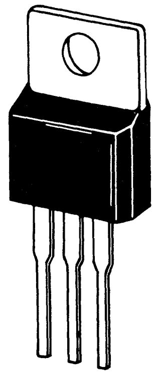
Unless specific note is atttached, $V_I = 33V$, $I_O = 40mA$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, $0°C \leq T_J \leq +125°C$.

AN7900 SERIES TO-220 3-TERMINAL NEGATIVE VOLTAGE REGULATOR

General Description

Made for long-life reliability, the Panasonic AN7900 Series of 3-terminal Voltage Regulators features internal current limiting, safe area compensation and thermal shutdown for thorough overload and overheating protection. Ideal for use as fixed voltage regulators in a wide variety of applications, the AN7900 Series can also be used with external components when adjustable output voltages and currents are desired. Available in the TO-220 package configuration, the Panasonic series is equivalent to all industry-standard 7900 series voltage regulators.

AN7900 SERIES



TO-220 PACKAGE

Features

- Output current 1A max.
- No external components necessary
- Internal thermal overload protection and short circuit current limiting
- Safe area compensation (output transistor)
- TO-220 package
- Output voltages: 5V, 6V, 7V, 8V, 9V, 10V, 12V, 15V, 18V, 20V, 24V

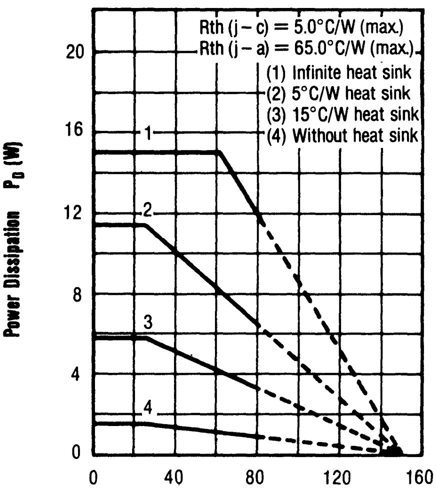
Absolute Maximum Ratings ($T_a = 25°C$)

Item	Symbol	Ratings	Unit	Note
Supply Voltage	Vcc	−35	V	2
Power Dissipation	PD	15	W	1
Operating Temperature	Topr	−30 to +80	°C	
Storage Temperature	Tstg	−55 to +150	°C	

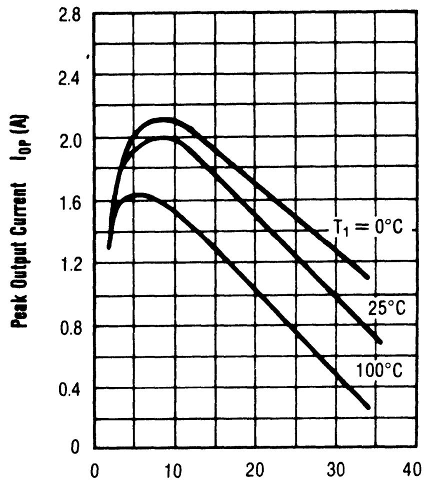
Note 1. At Tj > 150°, internal shuts off output.
Note 2. Vcc can be −40V for AN7920 and AN7924.

Typical Electrical Performance Curves

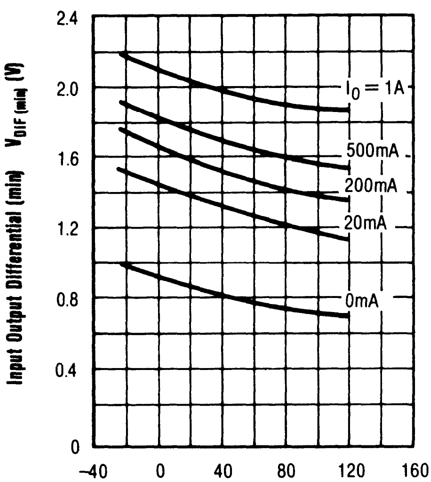
Power Dissipation vs Ambient Temperature



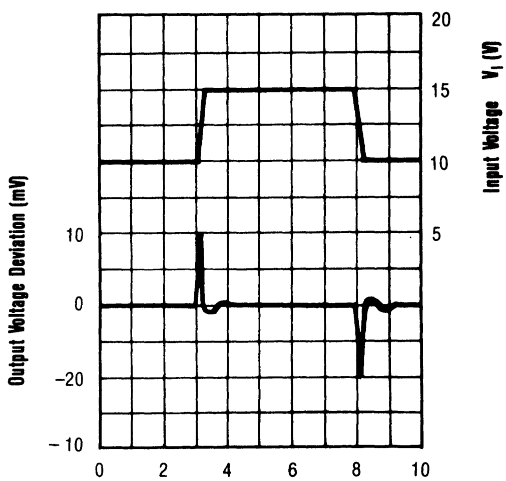
Peak Output Current vs Input Output Differential



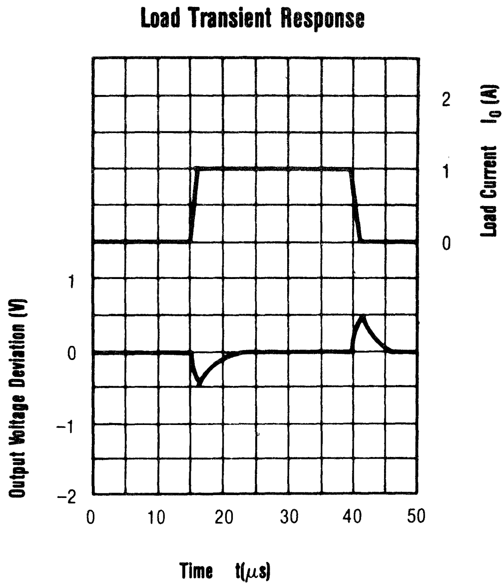
Input Output Differential vs Junction Temperature

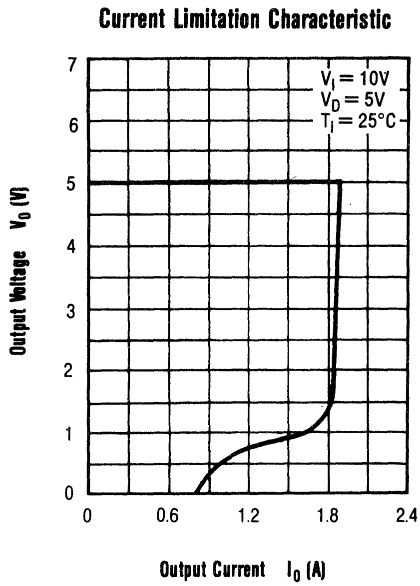


Line Transient Reponse

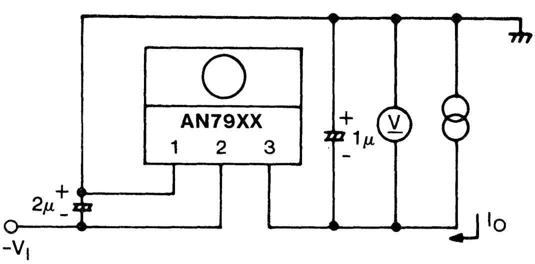


Typical Electrical Performance Curves (continued)



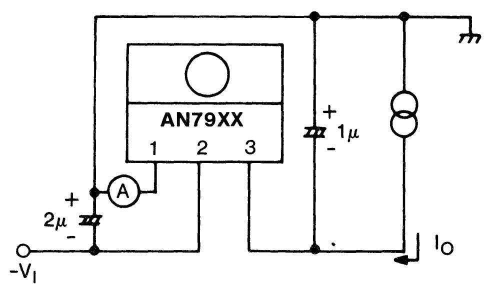


Test Circuit 1



See Note 1.

Test Circuit 2

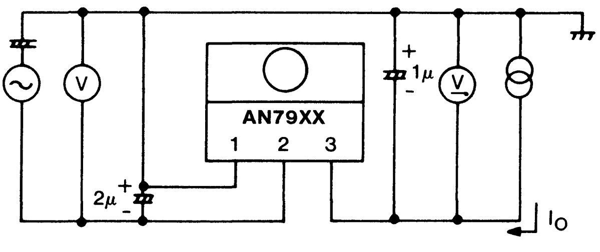


See Note 1.

Notes

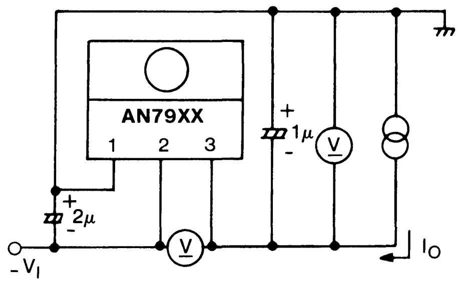
1. Test time should be short (within 10ms) so that the change of characteristics by junction temperature increase can be neglected.
2. RR = 20 log (| e_{in} | / | e_{out} |)
3. $V_I - V_O$ is a value when V_O is 5% lower than specific value by reducing V_I.

Test Circuit 3



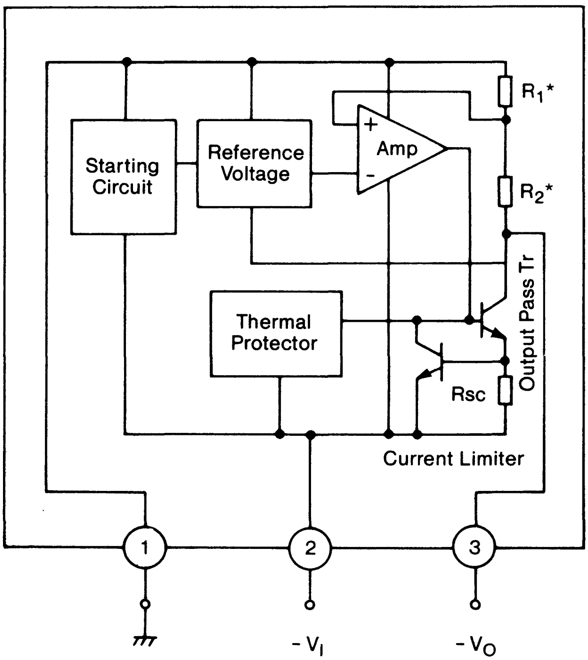
See Note 2.

Test Circuit 4



See Note 1, 3.

Schematic Diagram



*Refer to table

	R 1 (Ω)	R 2 (Ω)
AN7905	3K	2K
AN7906	3K	3K
AN7907	3K	4K
AN7908	3K	5K
AN7909	3K	6K
AN7910	3K	7K
AN7912	3K	9K
AN7915	3K	12K
AN7918	3K	15K
AN7920	3K	17K
AN7924	3K	21K

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	–4.8	–5.0	–5.2	V
			$-7V \leq V_I \leq -20V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	–4.75	–5.0	–5.25	V
Line Regulation	REG (LINE)	1	$-7V \leq V_I \leq -25V$ $T_J = 25°C$		3.0	100	mV
			$-8V \leq V_I \leq -12V$ $T_J = 25°C$		1.0	50	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		10	100	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		3	50	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	4.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-7V \leq V_I \leq -25V$ $T_J = 25°C$			1.3	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		40		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-8V \leq V_I \leq -18V$	62	74		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–1.4		mV/°C

Unless specific note is attached, $V_I = 10V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

AN7906 TO-220 3-TERMINAL NEGATIVE VOLTAGE REGULATOR

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	–5.75	–6.0	–6.25	V
			$-8V \leq V_I \leq -21V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	–5.7	–6.0	–6.3	V
Line Regulation	REG (LINE)	1	$-8V \leq V_I \leq -25V$ $T_J = 25°C$		4.0	120	mV
			$-9V \leq V_I \leq -13V$ $T_J = 25°C$		1.5	60	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		10	120	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		3	60	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	4.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-8V \leq V_I \leq -25V$ $T_J = 25°C$			1.3	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		44		µV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-9V \leq V_I \leq -19V$	60	73		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–0.5		mV/°C

Unless specific note is attached, $V_I = 11V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	–6.7	–7.0	–7.3	V
			$-9V \leq V_I \leq -22V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	–6.65	–7.0	–7.35	V
Line Regulation	REG (LINE)	1	$-9V \leq V_I \leq -25V$ $T_J = 25°C$		5.0	140	mV
			$-10V \leq V_I \leq -14V$ $T_J = 25°C$		1.5	70	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	140	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	70	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.0	4.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-9V \leq V_I \leq -25V$ $T_J = 25°C$			1.3	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		48		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-10V \leq V_I \leq -20V$	58	72		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–0.5		mV/°C

Unless specific note is attached, $V_I = 12V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	−7.7	−8.0	−8.3	V
			$-10.5V \leq V_I \leq -23V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	−7.6	−8.0	−8.4	V
Line Regulation	REG (LINE)	1	$-10.5V \leq V_I \leq -25V$ $T_J = 25°C$		6.0	160	mV
			$-11V \leq V_I \leq -17V$ $T_J = 25°C$		2.0	80	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	160	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	80	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.2	4.5	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-10.5V \leq V_I \leq -25V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		52		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-11V \leq V_I \leq -21V$	56	71		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V/\Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.6		mV/°C

Unless specific note is attached, $V_I = -14V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	–8.65	–9.0	–9.35	V
			$-11.5V \leq V_I \leq -24V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	–8.55	–9.0	–9.45	V
Input Stability	REG (LINE)	1	$-11.5V \leq V_I \leq -26V$ $T_J = 25°C$		7.0	180	mV
			$-12V \leq V_I \leq -18V$ $T_J = 25°C$		2.0	90	mV
Load Stability	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	180	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	90	mV
Bias Current	I_Q	2	$T_J = 25°C$		2.2	4.5	mA
Change of Bias Current (Input)	ΔI_Q (LINE)	2	$-11.5V \leq V_I \leq -26V$ $T_J = 25°C$			1.0	mA
" " (Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		58		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-12V \leq V_I \leq -22V$	56	71		dB
Min. Difference of Input and Output Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V/\Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–0.6		mV/°C

Unless specific note is attached, $V_I = -15V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	–9.6	–10.0	–10.4	V
			$-12.5V \leq V_I \leq -25V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	–9.5	–10.0	–10.5	V
Line Regulation	REG (LINE)	1	$-12.5V \leq V_I \leq -27V$ $T_J = 25°C$		8.0	200	mV
			$-13V \leq V_I \leq -19V$ $T_J = 25°C$		2.5	100	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	200	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	100	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.5	5.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-12.5V \leq V_I \leq -27V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		64		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-13V \leq V_I \leq -23V$	56	71		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–0.7		mV/°C

Unless specific note is attached, $V_I = -16V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	−11.5	−12.0	−12.5	V
			$-14.5V \leq V_I \leq -27V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	−11.4	−12.0	−12.6	V
Line Regulation	REG (LINE)	1	$-14.5V \leq V_I \leq -30V$ $T_J = 25°C$		10	240	mV
			$-16V \leq V_I \leq -22V$ $T_J = 25°C$		3.0	120	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	240	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	120	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.5	5.0	mA
Quiescent Current Change (Input)	ΔI_{Q} (LINE)	2	$-14.5V \leq V_I \leq -30V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_{Q} (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		75		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-15V \leq V_I \leq -25V$	55	70		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.8		mV/°C

Unless specific note is attached, $V_I = -19V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	−14.4	−15.0	−15.6	V
			$-17.5V \leq V_I \leq -30V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	−14.25	−15.0	−15.75	V
Line Regulation	REG (LINE)	1	$-17.5V \leq V_I \leq -30V$ $T_J = 25°C$		11	300	mV
			$-20V \leq V_I \leq -26V$ $T_J = 25°C$		3.0	150	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	300	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	150	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.5	5.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-17.5V \leq V_I \leq -30V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		90		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-18.5V \leq V_I \leq -28.5V$	54	69		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−0.9		mV/°C

Unless specific note is attached, $V_I = -23V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	–17.3	–18.0	–18.7	V
			$-21V \leq V_I \leq -33V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	–17.1	–18.0	–18.9	V
Line Regulation	REG (LINE)	1	$-21V \leq V_I \leq -33V$ $T_J = 25°C$		15	360	mV
			$-24V \leq V_I \leq -30V$ $T_J = 25°C$		5.0	180	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	360	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	180	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		2.5	5.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-21V \leq V_I \leq -33V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		110		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-22V \leq V_I \leq -32V$	53	68		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / T \Delta$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		–1.0		mV/°C

Unless specific note is attached, $V_I = -27V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	−19.2	−20.0	−20.8	V
			$-23V \leq V_I \leq -35V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	−19.0	−20.0	−21.0	V
Line Regulation	REG (LINE)	1	$-23V \leq V_I \leq -35V$ $T_J = 25°C$		16	400	mV
			$-26V \leq V_I \leq -32V$ $T_J = 25°C$		5.5	200	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	400	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	200	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		3.0	5.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-23V \leq V_I \leq -35V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		135		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-24V \leq V_I \leq -34V$	52	67		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / T \Delta$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.0		mV/°C

Unless specific note is attached, $V_I = -29V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

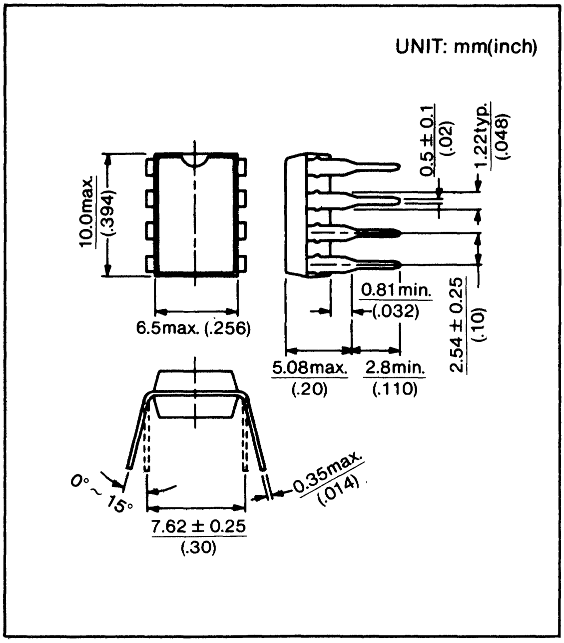
Electrical Characteristics ($T_a = 25°C$)

Item	Symbol	Test Circuit	Conditions	Limit min	Limit typ	Limit max	Unit
Output Voltage	V_O	1	$T_J = 25°C$	−23.0	−24.0	−25.0	V
			$-27V \leq V_I \leq -38V$ $5mA \leq I_O \leq 1A$, $P_D \leq 15W$	−22.8	−24.0	−25.2	V
Line Regulation	REG (LINE)	1	$-27V \leq V_I \leq -38V$ $T_J = 25°C$		18	480	mV
			$-30V \leq V_I \leq -36V$ $T_J = 25°C$		6.0	240	mV
Load Regulation	REG (LOAD)	1	$5mA \leq I_O \leq 1.5A$ $T_J = 25°C$		12	480	mV
			$250mA \leq I_O \leq 750mA$ $T_J = 25°C$		4	240	mV
Quiescent Current	I_Q	2	$T_J = 25°C$		3.0	5.0	mA
Quiescent Current Change (Input)	ΔI_Q (LINE)	2	$-27V \leq V_I \leq -38V$ $T_J = 25°C$			1.0	mA
(Output)	ΔI_Q (LOAD)		$5mA \leq I_O \leq 1A$ $T_J = 25°C$			0.5	mA
Output Noise Voltage	V_n	1	$10Hz \leq f \leq 100kHz$		170		μV
Ripple Rejection	RR	3	$f = 120Hz$, $I_O = 100mA$ $-28V \leq V_I \leq -38V$	50	65		dB
Dropout Voltage	$V_I - V_O$	4	$I_O = 1A$ $T_J = 25°C$		1.1		V
Output Peak Current	I_{OP}	1	$T_J = 25°C$		2.1		A
Output Voltage Temperature Coefficient	$\Delta V / \Delta T$	1	$I_O = 5mA$ $0°C \leq T_J \leq 125°C$		−1.0		mV/°C

Unless specific note is attached, $V_I = 33V$, $I_O = 500mA$, $C_I = 2\mu F$, $C_O = 1\mu F$, $0°C \leq T_J \leq +125°$.

Package Details

8 – DIP Package



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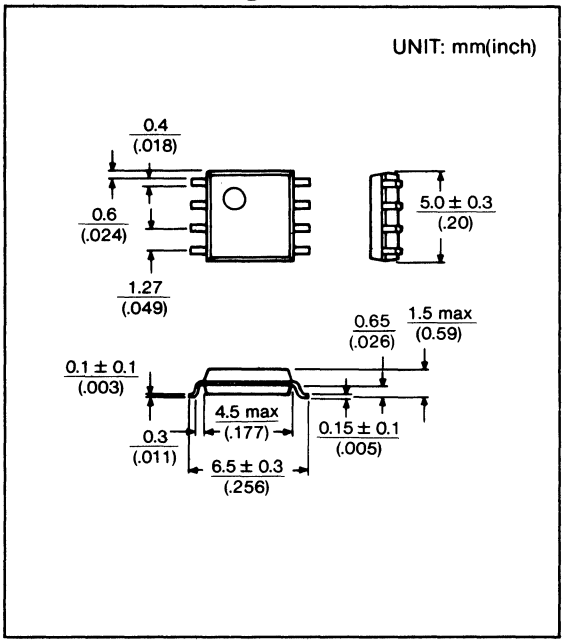

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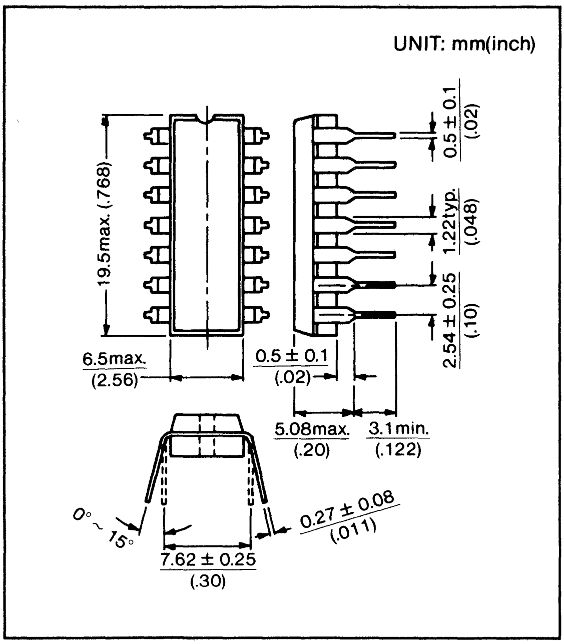

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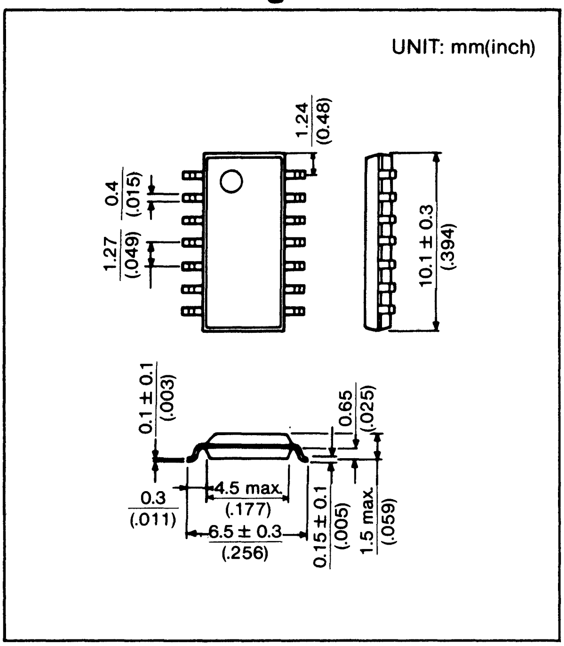
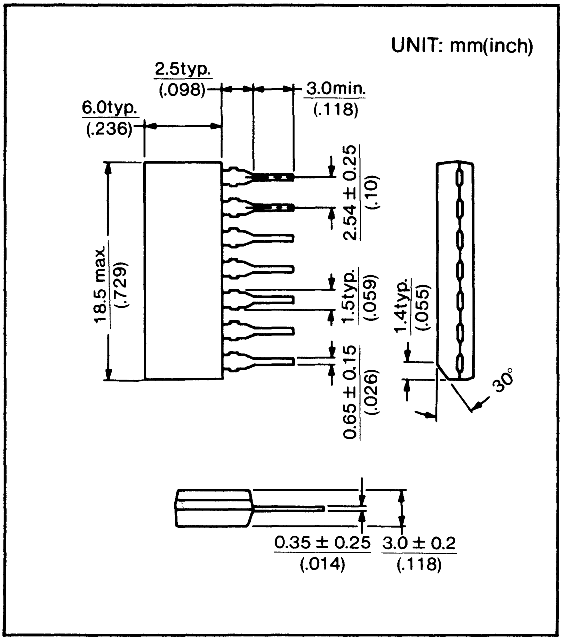


Package Details

7 – SIP Package



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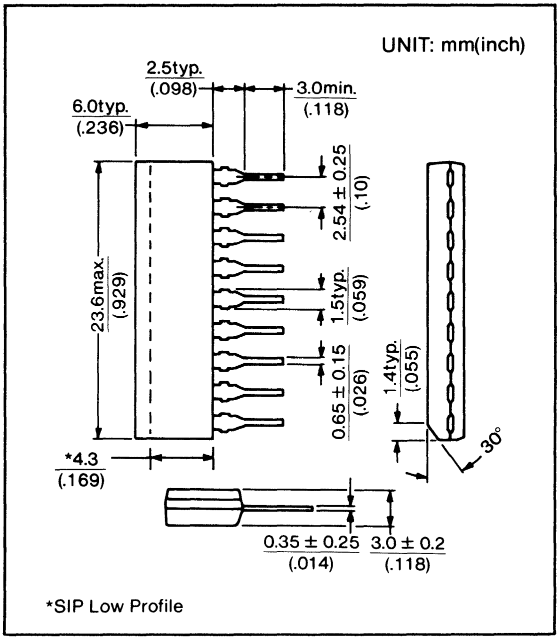
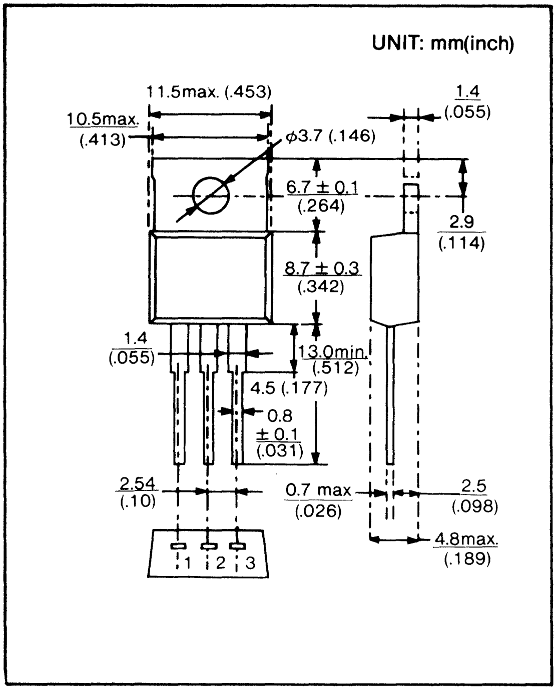
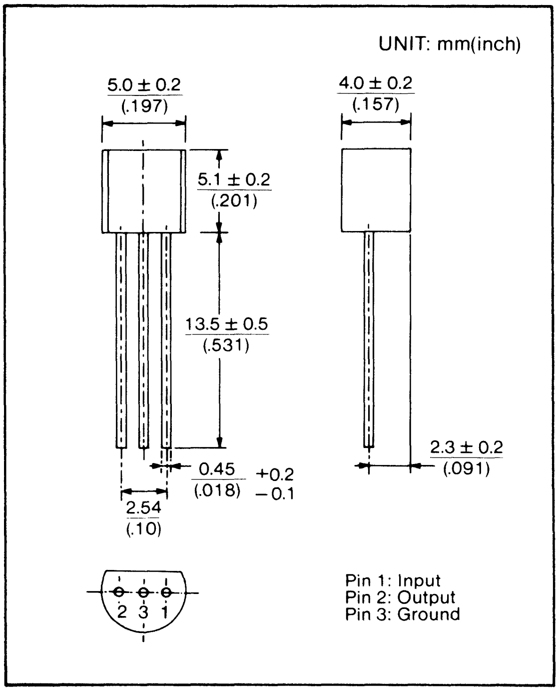


TO - 220 Package



TO - 92 Package



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Notes

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