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DIGITAL INTEGRATED CIRCUITS

SP8000 SERIES HIGH SPEED DIVIDERS

MOS

MNOS (NON-VOLATILE MEMORY ELEMENTS)

digital

Process control circuits
Interface circuits

SP520B

GRAY CODE COUNTER

The SP520 digital integrated circuit is an RTL 5-bit up/down counter in positive logic with both Gray code and natural binary code TTL-compatible outputs. Other inputs and outputs use modified RTL to give improved noise immunity.

SP520 counters can be cascaded by suitable external connections to give a counter with any multiple of 5 bits. The counter is of a non-overflow design and will operate with an input frequency in excess of 1MHz. It can be reset to the 00000 state and the Gray O/Ps can be inhibited for "wired OR" applications.

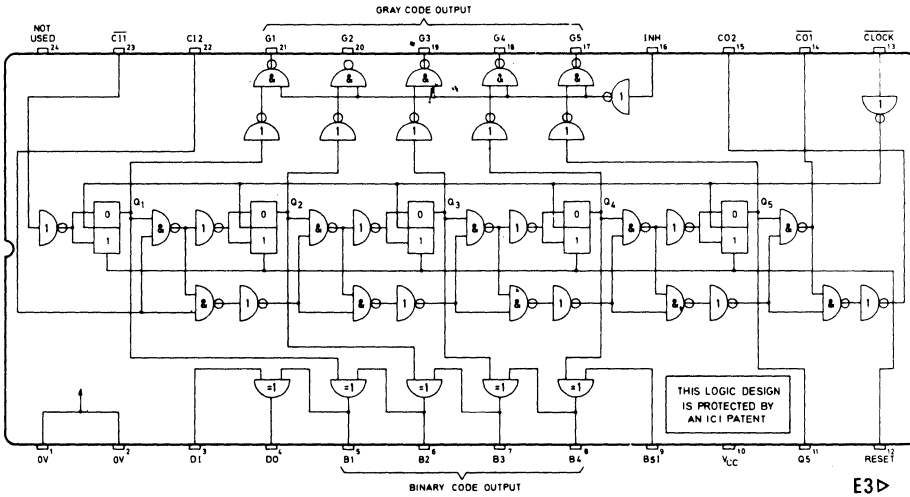


Fig.1 Logic diagrams

Pin No.	Function	Pin No.	Function
1	Common rail (0V)	14	Inhibit carry O/P to 1st flip-flop of next counter (C_{O1})
2	Common rail (0V)		
3	Counter external direction control (Logic '0' = up)	15	Enable carry O/P to gate chain of next counter (C_{O2})
4	Binary code O/P direction (D_O)	16	Inhibit I/P for all Gray O/Ps except auxiliary Gray code O/P Bit 5 (INH)
5	Binary code O/P Bit 1 (B1)		
6	Binary code O/P Bit 2 (B2)	17	Gray code O/P Bit 5 (G5)
7	Binary code O/P Bit 3 (B3)	18	Gray code O/P Bit 4 (G4)
8	Binary code O/P Bit 4 (B4)	19	Gray code O/P Bit 3 (G3)
9	Binary code I/P Bit 5 (B5I)	20	Gray code O/P Bit 2 (G2)
10	Positive supply rail (V_{CC})	21	Gray code O/P Bit 1 (G1)
11	Auxiliary Gray code O/P Bit 5 (Q5)	22	Enable gate chain I/P (CI_2)
12	Reset I/P for all flip-flop stages (forces 00000 state)	23	Inhibit I/P to 1st flip-flop (CI_1)
		24	No connection
13	$\overline{\text{Clock}}$ I/P		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to +70°C
V_{CC} = 5.0V ±0.25V

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
INPUT REQUIREMENTS					
Counter external direction control (pin 3), Binary code I/P bit 5 (pin 9), and Enable gate chain I/P (pin 22):					
Input voltage 'High'	3.0			V	
Input voltage 'Low'			1.0	V	
Input current			25	μA	V_{in} = 3.0V
Inhibit I/P for Gray O/Ps (pin 16)					
Input voltage 'High'	3.0			V	
Input voltage 'Low'			1.0	V	
Input current 'High'			250	μA	V_{in} = 3.0V
Input current 'Low'			50	μA	V_{in} = 1.0V
Reset I/P for all flip-flops (pin 12)					
Input voltage 'High'	2.3			V	with voltage drive
Input voltage 'Low'			0.8	V	with voltage drive
Input current			3.5	mA	with voltage drive
Input current 'High'	1.0			mA	With current drive
Clock I/P (pin 13)					
Input voltage 'High'	3.0			V	See note 1
Input voltage 'Low'			1.0	V	
Input current			200	μA	V_{in} = 3.0V
Input clock frequency			1	MHz	1:1 mark = space ratio
Input slew rate	20			V/μs	See note 2
Inhibit I/P to 1st flip-flop (pin 23)					
Input voltage 'High'	2.3			V	See note 3
Input voltage 'Low'			0.8	V	
Input current			2.0	mA	T_{amb} = +70°C, V_{in} = 2.3V
Input slew rate	20			V/μs	See note 2
OUTPUT CHARACTERISTICS					
Binary code O/P bits 1-4 (pins 5-8)					
Output voltage 'Low'			0.4	V	Sink current = 6.4mA
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state		6.0	8.0	kΩ	
Binary code O/P direction (pin 4)					
Output voltage 'Low'			0.4	V	Sink current = 6.4mA
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state			2.6	kΩ	
Aux. Gray code O/P bit 5 (pin 11)					
Output voltage 'Low'			0.4	V	Sink current = 3.2V
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state			8.0	kΩ	
Gray code O/Ps bits 1-5 (pins 17-21)					
Output voltage 'Low'			0.4	V	Sink current = 8.0mA
Output voltage 'High'		4.2		V	I_{out} = 0mA
Output impedance in 'High' state			3.4	kΩ	
Output leakage to earth in inhibited state			20	μA	T_{chip} = 100°C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Inhibit carry O/P to 1st flip-flop of next counter.					
Output voltage 'Low' **(pin 14)**			0.4	V	R_{pd} = 4kΩ (see notes 4 and 5)
Output voltage 'High'	2.4	2.75	3.2	V	
Enable carry O/P to gate chain of next counter					
Output voltage 'Low' **(pin 15)**			0.4	V	Sink current = 3.2mA
Output voltage 'High'		V_{CC}		V	I_{out} = 0mA
Output impedance in 'High' state			4.8	kΩ	
Power supply drain current (pin 10)		70	96	mA	V_{CC} = 5.0V, clock I/P = 0V

NOTES

1. In the high state the input level affects the overall power consumption. The chip power consumption increases by approximately 12.5mW and it might therefore be desirable to limit the clock input voltage with, say, a zener diode.
2. The flip-flops need fast edges for reliable toggling.
3. In the high state the input current is directly proportional to the input voltage and increases at approximately 1mA/V. It might therefore be desirable to limit the maximum input voltage.
4. An emitter follower output will not sink current and is not therefore suitable for interfacing directly with TTL or DTL.
5. This output is an emitter follower with no internal pulldown resistor – when counters are cascaded the emitter follower pulldown is provided by the next stage.

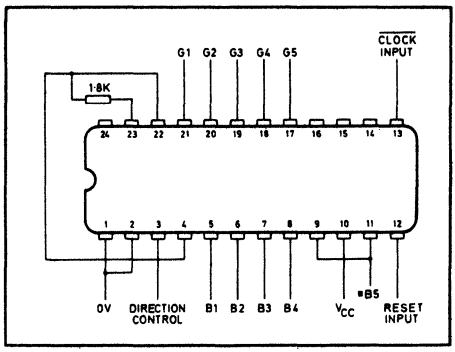


Fig.2 SP520 connected as a 5-bit counter

ABSOLUTE MAXIMUM RATINGS

Continuous +ve supply voltage	+7V
Continuous +ve input voltage	not greater than the supply voltage in use
Max. operating junction temp	+175°C
Storage Temperature	−50°C to +175°C

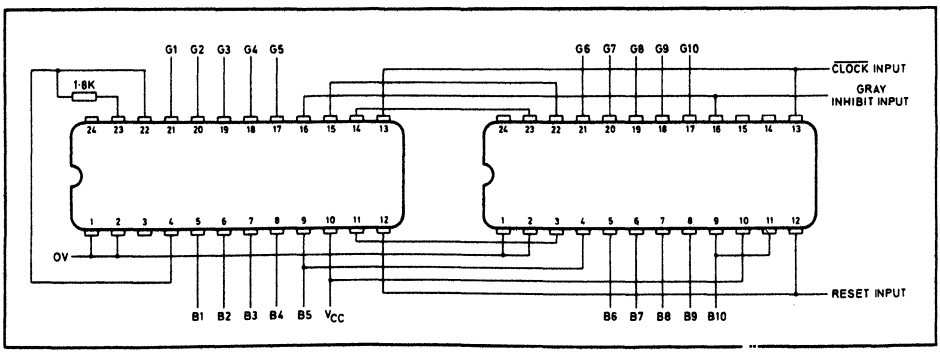


Fig.3 Two SP520s connected as a 10-bit counter

SP521B

BINARY RATE MULTIPLIER

A binary rate multiplier (BRM) is a form of programmable divider in which the number of pulses appearing at the output for each full period of the counter is equal to the value of the binary number present on the binary inputs. Thus, if the binary word input to a BRM is, say, 10101 (=21) then, for every 32 clock pulses counted only 21 will be gated onto the output.

The SP521 is a binary rate multiplier with two sets of binary control inputs, each associated with its own clock phase. The phase 1 controls operate in conjunction with the counter chain clock (ϕ1). The phase 2 controls operate in conjunction with a separate clock (ϕ2) which can be antiphase with ϕ1 clock and interlaced with it. Phase 1 and phase 2 outputs can be combined by wiring them together.

The operating temperature range of the SP521 is 0°C to +70°C and the nominal supply voltages are 0V and +5V. The device ,is available in 24-lead D.I.L 0.6 inch spacing ceramic packages.

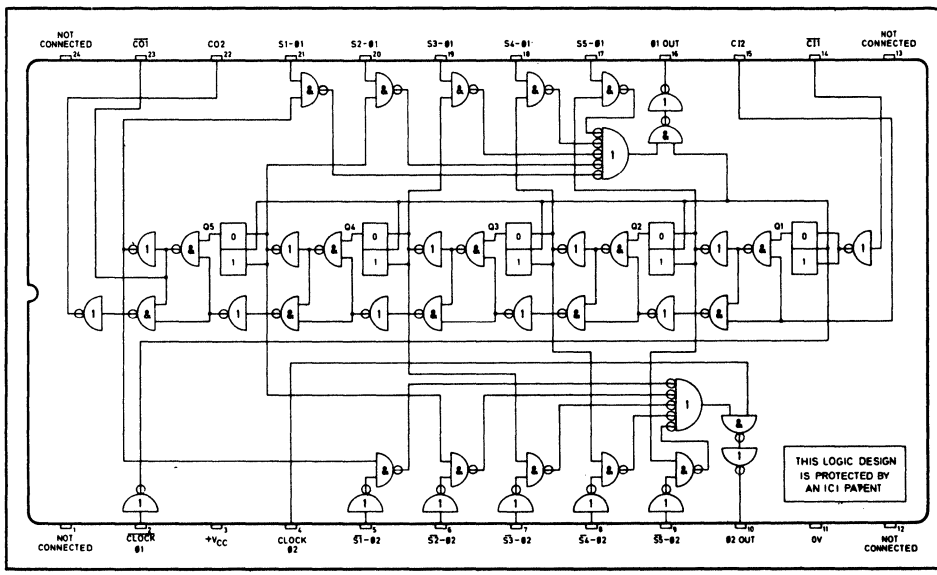


Fig.1 Logic Diagram

E3▷

OPERATING NOTES

The phase 1 controls operate in conjunction with the master clock pulses of the BRM counter chain (ϕ1 clock). The inputs operate with true positive logic and have CCSL-compatible input requirements. The phase 2 controls have standard RTL type inputs and operate with inverse positive logic in conjunction with the ϕ2 clock.

Phase 1 and phase 2 outputs are emitter followers with non-standard logic levels – the logic levels being set by the logic levels of the phase 1 inputs and the ϕ2 clock input respectively. In a multiple-package BRM (i.e. > 5 bits) the phase 1 outputs are wired together to give the required output. If the ϕ2 clock input is interlaced with the φ1 clock, the phase 2 outputs can be wire-ORed with the phase 1 outputs to give a continuous pulse train. The maximum ϕ1 and ϕ2 clock input frequency is in excess of 1MHz

PIN CONNECTIONS

Pin No.	Function	Pin No.	Function
1	No connection	14	Inhibit I/P to 1st flip-flop (CI_1)
2	Clock I/P $\phi 1$ (BRM drive)	15	Enable gate chain I/P (CI_2)
3	Positive supply rail (V_{CC})	16	Phase 1 O/P ($\phi 1_{OUT}$)
4	Clock I/P $\phi 2$	17	Phase 1 Binary Control Input (true) Bit 5 ($S5\phi 1$)
5	Phase 2 Binary control input (inverse) Bit 1 ($\overline{S1}\phi 2$)	18	Phase 1 Binary Control Input (true) Bit 4 ($S4\phi 1$)
6	Phase 2 Binary control input (inverse) Bit 2 ($\overline{S2}\phi 2$)	19	Phase 1 Binary Control Input (true) Bit 3 ($S3\phi 1$)
7	Phase 2 Binary control input (inverse) Bit 3 ($\overline{S3}\phi 2$)	20	Phase 1 Binary Control Input (true) Bit 2 ($S2\phi 1$)
8	Phase 2 Binary control input (inverse) Bit 4 ($\overline{S4}\phi 2$)	21	Phase 1 Binary Control Input (true) Bit 1 ($S1\phi 1$)
9	Phase 2 Binary control input (inverse) Bit 5 ($\overline{S5}\phi 2$)	22	Enable carry O/P to gate chain of next BRM (CO_2)
10	Phase 2 O/P ($\phi 2_{OUT}$)	23	Inhibit carry O/P to 1st flip-flop of next BRM (CO_1)
11	Common Rail, 0 volts	24	No connection
12	No connection		
13	No connection		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Tamb = 0°C to +70°C
V_{CC} = 5.0V ±0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
INPUT CONDITIONS					
Clock $\overline{\phi 1}$ I/P pin 2					
Input voltage 'high'	3.0			V	See note 1
Input voltage 'low'			1.0	V	
Input current			200	μA	V_{IN} = 3.0V
Input slew rate	20			V/μS	See note 2
Clock $\phi 2$ I/P (pin 4)					
Input voltage 'high'	3.1			V	
Input voltage 'low'			1.0	V	
Input current			150	μA	V_{IN} = 3.1V
Binary phase 1 control inputs, bits 1 to 5 (pins 17 to 21)					
Input voltage 'high'	3.1			V	See note 3
Input voltage 'low'			1.0	V	
Input current			20	μA	V_{IN} = 3.1V
Phase 2 Binary control inputs, bits 1 to 5 (pins 5 to 9)					
Input voltage 'high'	1.0			V	Voltage drive
Input voltage 'low'			0.5	V	Voltage drive
Input current			0.5	mA	V_{IN} = 1V Voltage drive
Input base resistor	1.0			kΩ	
Input current 'high'	200			μA	Current drive
Inhibit I/P to 1st flip-flop (pin 14)					
Input voltage 'high'	2.0			V	See note 1
Input voltage 'low'			1.0	V	
Input current			2.0	mA	V_{IN} = 2.0V
Input slew rate	20			V/μS	See note 2

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Enable gate chain I/P (pin 15)					
Input voltage 'high'	3.1			V	
Input voltage 'low'			1.0	V	
Input current			20	μA	V_{IN} = 3.1V
OUTPUT CHARACTERISTICS					
Phase 1 and phase 2 O/P's (pins 10 & 16) (Emitter follower outputs. See notes 3 and 4.)					
Output high level	3.0			V	Phase 1 I/Ps & Clock 02 I/P connected to V_{CC}(+5V) via 8 kΩ resistor. R_{pd} = 4kΩ
Output low level			0.4	V	
Enable carry O/P to gate chain of next BRM (pin 22)					
Output low level			0.4	V	Sink current = 1.6mA
Output high level		V_{CC}		V	I_{OUT} = 0mA
Output impedance			4.4	kΩ	
Inhibit carry O/P to 1st flip-flop of next BRM (pin 23)					
Output voltage 'high'	2.1		3.1	V	R_{pd} = 4kΩ
Output voltage 'low'			0.8	V	See note 4
Power supply drain current (pin 3)		35	60	mA	V_{CC} = +5V, Clock 01 I/P = 0V Inhibit I/P = 0V

1. In the high state these inputs affect the overall chip power consumption. In the case of the clock $\phi 1$ input the power consumption increases with increasing input voltage level at approximately 12.5 mW/V. In the case of the Inhibit I/P to 1st flip flop the input current is directly proportional to the input voltage in the high state, and increases at approximately 1mA/V.
2. The flip-flops need fast input edges for reliable toggling.
3. The voltage levels of the high states of the phase 1 and phase 2 outputs depend on the input voltages of the phase 1 binary inputs and the clock $\phi 2$ input respectively. In each case the output voltage level will be approximately $2V_{BE}$ more positive than the appropriate input. voltage. These outputs have no internal pulldown resistors.
4. An emitter follower output will not sink current and is not therefore suitable for interfacing directly with TTL or DTL.

ABSOLUTE MAXIMUM RATINGS

Continuous +ve supply voltage (V_{CC})	+7V	Operating ambient temperature	0°C to +70°C
Continuous +ve input voltage	not greater than the supply voltage in use	Storage temperature	−50°C to +175°C

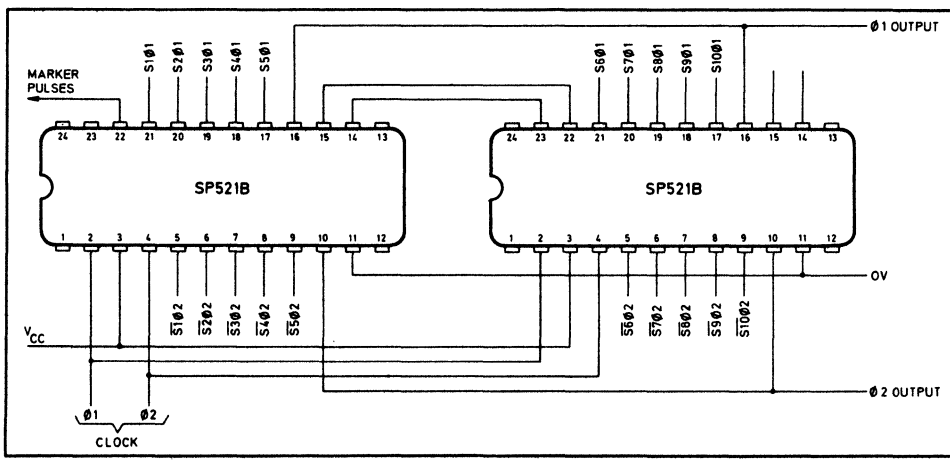


Fig.2 Two SP521s connected as a 10-bit BRM (packages viewed from above)

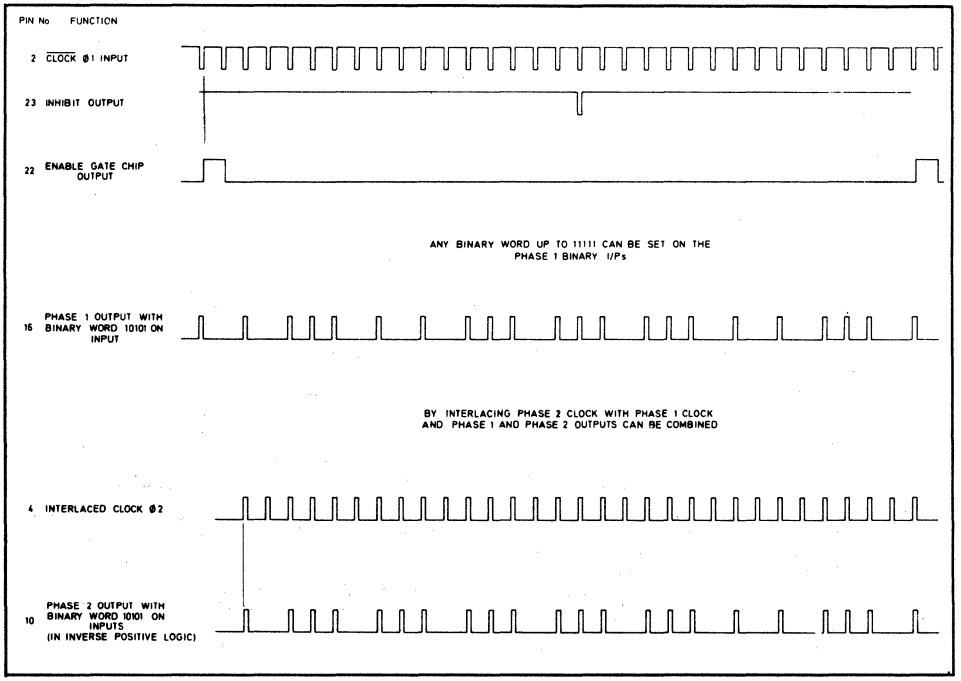


Fig.3 SP521 logic states (5-bit BRM). Enable gate chain input held at logic '1', Inhibit 1st flip-flop held at logic '0'.

SP522B

PHASE LOCK, DIVIDER & COMPARATOR

The SP522B is the most specialised of the SP520 series of RTL digital integrated circuits. It contains a frequency divide-by-eight and interlacing circuit, a frequency comparator and digital filter, and an input phase-locking circuit.

Frequency divider

The clock input frequency of the dividing circuit is referred to as 8f. An output is provided at a quarter of the clock frequency (2f), and 2 interlaced outputs are provided at one eighth of the clock frequency, 1fϕ1 and 1fϕ2. The maximum clock frequency of the divider chain is in excess of 2MHz.

Frequency comparator and filter

The frequency comparator is a five-state up/down counter which can be reset to the central symmetrical state. The reset input to the comparator is NORed with the 1fϕ1 signal. There is one count up input to the counter and two alternative count down inputs, one of which is compatible with CCSL logic. Two direction outputs are provided and one difference frequency output.

When the counter has been set into the central state by the reset there must be a difference of three pulses between the count up and count down inputs before there is a pulse in the difference frequency output. This means that a small amount of jitter in one input relative to the other will not appear at the output.

Phase lock circuit

The phase lock circuit accepts a random phase input (e.g. from a flowmeter transducer) and locks it to the phase of the master clock (8f input). The maximum frequency at which the phase lock circuit will work satisfactorily is 3.2f. A race condition can occur on switching on, but if the master clock and the input signal are phase independent it clears itself very quickly. The phase-locked output at pin 3 is intended to be used as the count up input to the frequency comparator, and is then connected externally to pin 10.

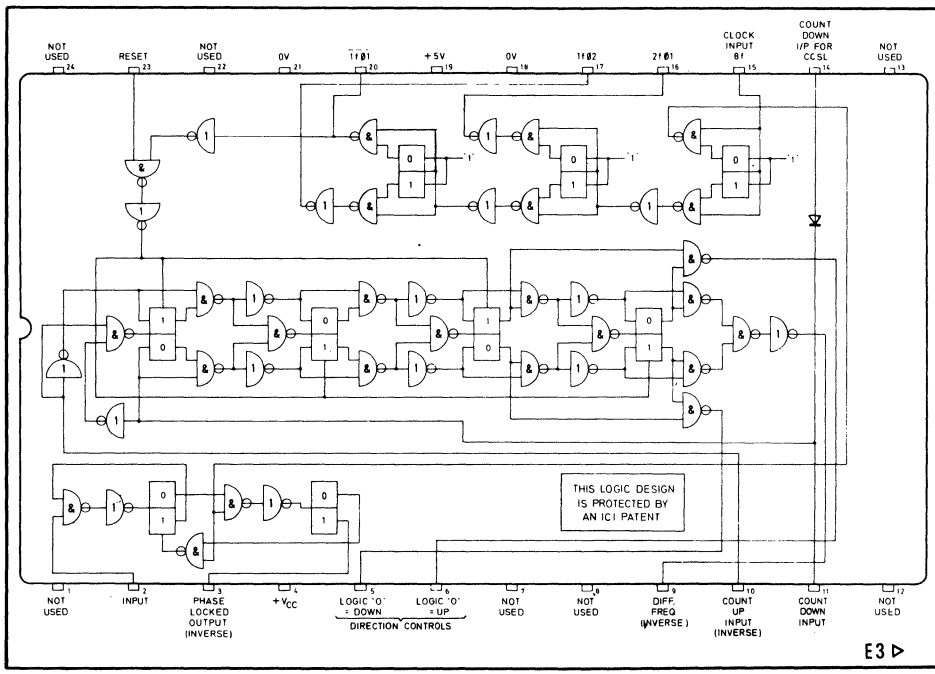


Fig. 1 SP522B Logic diagram

PIN CONNECTIONS

Pin No.	Function	Pin No.	Function
1	No connection	13	No connection
2	Input frequency signal (inverse phase)	14	Additional comparator count down I/P for CCSL logic
3	Phase lock O/P (inverse phase)		
4	Positive supply rail $+V_{CC}$	15	Master clock I/P (8f)
5	Direction control O/P (logic '0' = down)	16	2f ϕ1 O/P
6	Direction control O/P (logic '0' = up)	17	1f ϕ2 O/P
7	No connection	18	Common rail 0V
8	No connection	19	Positive supply rail $+V_{CC}$
9	Difference frequency – comparator O/P (inverse phase)	20	1f ϕ1 O/P
		21	Common rail 0V
10	Comparator count up I/P (inverse phase)	22	No connection
11	Comparator count down I/P	23	Reset comparator I/P (true)
12	No connection	24	No connection

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C
V_{CC} = 5.0V± 0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
INPUT CONDITIONS					
Input frequency signal (pin 2)					See note 1
Input voltage 'high'	2.7			V	
Input voltage 'low'			1.0	V	
Input current			20	µA	V_{IN} = 2.7V
Input slew rate	1			V/µS	See note 2
Comparator count-up input (pin 10)					
Input voltage 'high'	0.95			V	Voltage drive
Input voltage 'low'			0.5	V	Voltage drive
Input current		0.75	1.0	mA	V_{IN} = 0,95V
Input base resistor	420			Ω	
I/P current 'high'	150			µA	Current drive
Comparator count-down I/P (pin 11)					
Input voltage 'high'	1.0			V	Voltage drive
Input voltage 'low'			0.5	V	Voltage drive
Input current		1.0	2.0	mA	V_{IN} = 1.0V, T_{amb} = 70°C
Input base resistor	350			Ω	
Input current 'high'	900			µA	Current drive

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Additional count down I/P (pin 14)					
Input voltage 'high'	2.2			V	
Input voltage 'low'			1.0	V	
Input current			30	μA	V_{IN} = 2.2V
Master clock I/P (pin 15)					
Input voltage 'high'	2.7			V	
Input voltage 'low'			1.0	V	
Input current			20	μA	V_{IN} = 2.7V
Input slew rate	1			V/μS	See note 2
Reset comparator I/P (pin 23)					
Input voltage 'high'	2.7			V	
Input voltage 'low'			1.0	V	
Input current			20	μA	V_{IN} = 2.7V
OUTPUT CHARACTERISTICS					
Phase Lock O/P (pin 3)					See note 4
Output 'low'			0.4	V	Sink current = 1.6mA
Output 'high'	1.1			V	I_{OUT} = 0mA
Output impedance in high state			7.2	kΩ	
Direction control O/PS (Pins 5 & 6)					
Output 'low'			0.4	V	Sink current = 1.6mA
Output 'high'		V_{CC}		V	I_{OUT} = 0mA
Output impedance in high state			6.5	kΩ	
Difference frequency-comparator O/P (pin 9)					
Output voltage 'high'	3.1	3.5	3.8	V	
Output voltage 'low'		0.0	0.4	V	See note 5
2f ϕ1 O/P (pin 16)					
Output voltage 'low'			0.4	V	Sink current = 1.6mA
Output voltage 'high'		V_{CC}		V	I_{OUT} = 0mA
Output impedance in high state			5.2	kΩ	
1f ϕ2 O/P (pin 17)					
Output voltage 'high'	3.5			V	
Output voltage 'low'			1.0	V	See note 5
1f $\overline{\phi 1}$ O/P (pin 20)					
Output voltage 'high'	3.1		3.8	V	
Output voltage 'low'		0.0	0.4	V	See note 5
Power supply drain current		70	82	mA	V_{CC} = 5V

NOTES

1 There is a 25% probability of a race condition occurring in the phase lock circuit when power is first applied. To ensure that the circuit is brought into its correct operating condition an input clock transition ('1' → '0') must occur while the 4fϕ1 clock is in the logic '1' state. In most systems, where the input clock and the master clock are not synchronous, this happens very quickly.

2 The input flip-flops need fast edges for reliable toggling.

3 For the count-down input there is an option of an RTL input (pin 11) or a CCSL compatible input (pin 14). When the RTL input is used the CCSL input should be connected to the 0V rail. When the CCSL input is used, the RTL input should be left open circuit.

4 The logic '1' level of this output is very low and is only suitable for driving an RTL input directly. If required, however, special interface techniques (such as grounded base, emitter input cascode type circuit) can be used to extract the O/P from this pin without further loading the logic '1' level.

5 Pins 9, 17 and 20 are emitter follower outputs and will not sink current. These outputs are not therefore suitable for interfacing directly with TTL or DTL.

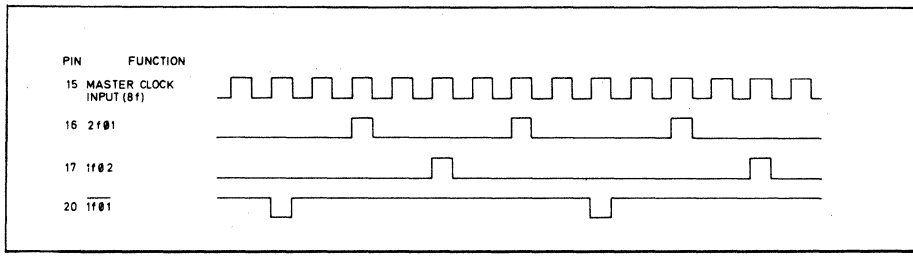


Fig. 2 Frequency divider logic timing

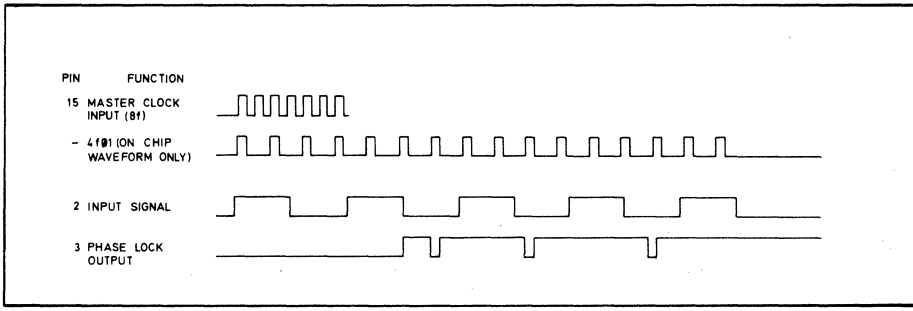


Fig. 3 Phase lock timing, illustrating recovery from race condition

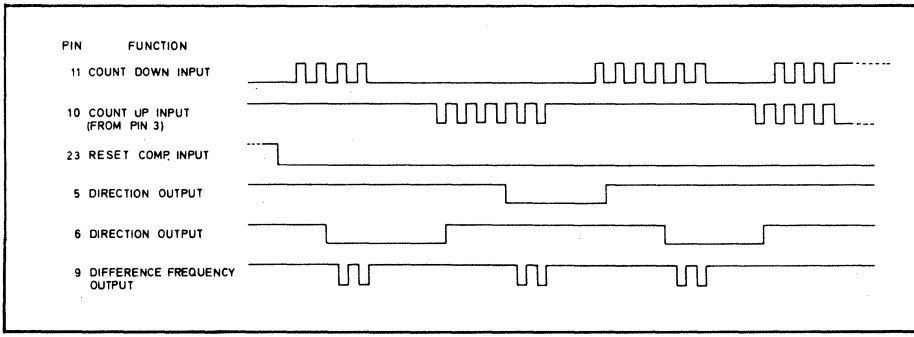


Fig. 4 Frequency comparator and filter timing

ABSOLUTE MAXIMUM RATINGS

Continuous +ve supply voltage	+7V
Continuous +ve input voltage	not greater than the supply voltage in use
Operating ambient temperature	0°C to +70°C
Storage temperature	−50°C to +175°C

APPLICATION NOTES

Fig. 5 shows a 10-bit frequency-to-digital encoder using the SP522B together with other elements of the SP520 series. The encoder provides continuous parallel digital output in non-ambiguous Gray code, and is capable of giving an immediate correct response to an interrogation signal at any time. This application note should be read in conjunction with the SP520B and SP521B data sheets.

The encoder employs the continuous feedback principle. The input frequency is first phased-locked to the master clock input to the SP522B then applied, together with the feedback frequency from the binary rate multiplier (SP521B), to the frequency comparator in the SP522B. Any difference frequency that results is applied to the clock inputs of the SP520B Gray code counter. A direction control signal is also applied to one SP520B (least significant 5 bits) to determine the up/down mode of the counter.

Binary-coded outputs from the SP520B's form the numerical multipliers that determine the number of output pulses in each cycle (i.e. the feedback frequency) of the binary rate multipliers.

The feedback frequency is taken from pin 16 of each SP521B to pin 14 of the SP522B and is in phase with the 1fϕ1 clock signal. The phase 2 outputs of the SP521B's (pin 10) are in phase with 1fϕ2 clock and are interlaced with the main feedback frequency signal when pins 10 and pins 16 are wired-ORed. Negative binary inputs (pins 5 to 9 on each SP521B) determine the number of pulses in this stream and can therefore be used to provide a zero elevation facility.

The Gray code outputs of each SP520B are interrogated by taking the 'inhibit Gray output' (pin 14) to logic '0'; the outputs can, however, be continuously displayed using the binary-coded outputs (pins 5 to 9) to drive numerical indicators via a suitable interface.

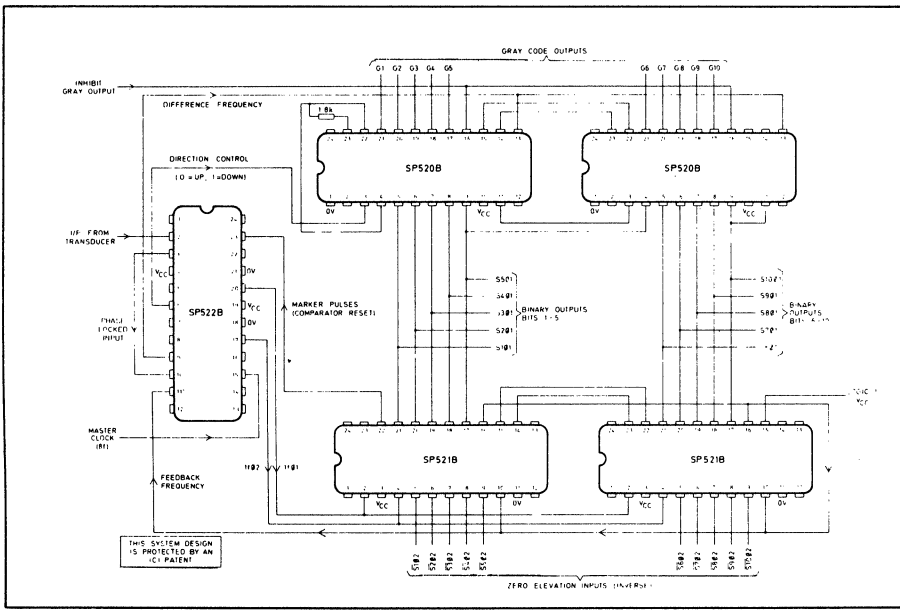


Fig. 5 Frequency-to-digital encoder

PROVISIONAL DATA

SP705B

CRYSTAL CONTROLLED INTEGRATED CIRCUIT OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency f as follows: $f/2$, $f/4$, $\overline{f/2}$ and $\overline{f/4}$. The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications

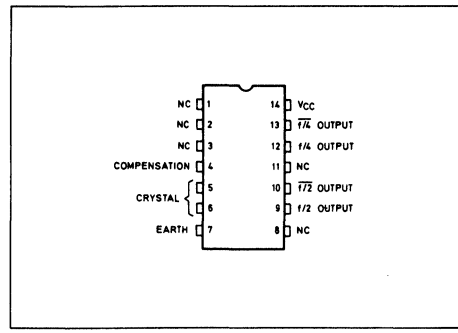


Fig.1 Pin connections

FEATURES

- Operating Frequency up to 10 MHz
- $f/2$ and $f/4$ outputs
- 4 TTL Level outputs
- Operates from +5V TTL Supply

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +5V

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
High state output voltage	V_{OH}	2.6		V	V_{CC} = 4.75V I_{OH} = 0.2 mA
Low state output voltage	V_{OL}		0.4	V	V_{CC} = 5.25V I_{OL} = 8 mA
Supply current	I_{CC}		35	mA	V_{CC} = 5V
Output rise time (10% to 90%)	t_R		20	ns	V_{CC} = 5V
Output fall time (90% to 10%)	t_F		20	ns	V_{CC} = 5V
Operating frequency (f)			10	MHz	
Operating temp range		0	70	°C	

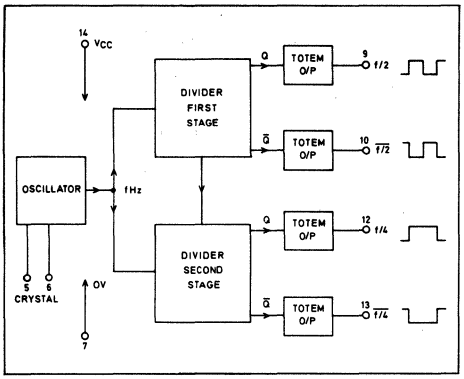


Fig. 2 SP705B block diagram

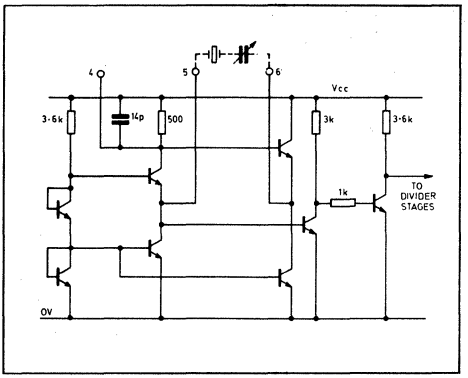


Fig. 3 Circuit diagram of SP705B oscillator

CIRCUIT DESCRIPTION

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with a 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig. 3.

The circuit is designed to provide low crystal drive levels – typically, less than 0.15mW at 5MHz. This is well within crystal manufacturers' limit of 0.5mW.

The compensation point, pin 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

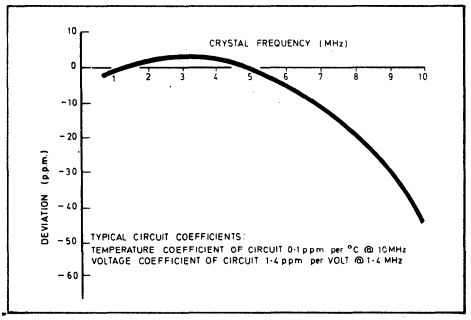
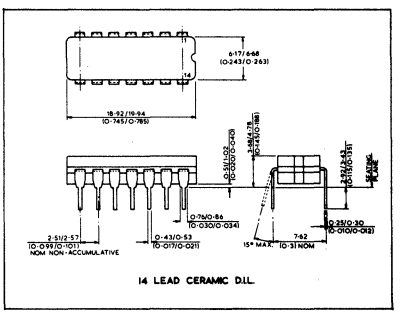


Fig. 4 Deviation from nominal crystal frequency

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



Publication No. P.S. 1402 Feb. 1975

SP721B BALANCED LINE DRIVER **SP722B** BALANCED LINE RECEIVER

SP723B BALANCED LINE RECEIVER WITH COMPLEMENTARY OUTPUTS

SP724B DUAL BALANCED LINE RECEIVER

The SP721B, SP722B, SP723B and SP724B circuits are designed for interfacing between TTL/DTL logic and balanced transmission lines. The SP721B line driver produces an output which is essentially a current sink into one of the two lines. The magnitude of the current is nominally twice that of an externally programmed source current. The receiver circuits will accept antiphase signals from a line with a d.c. level several volts remote from earth potential.

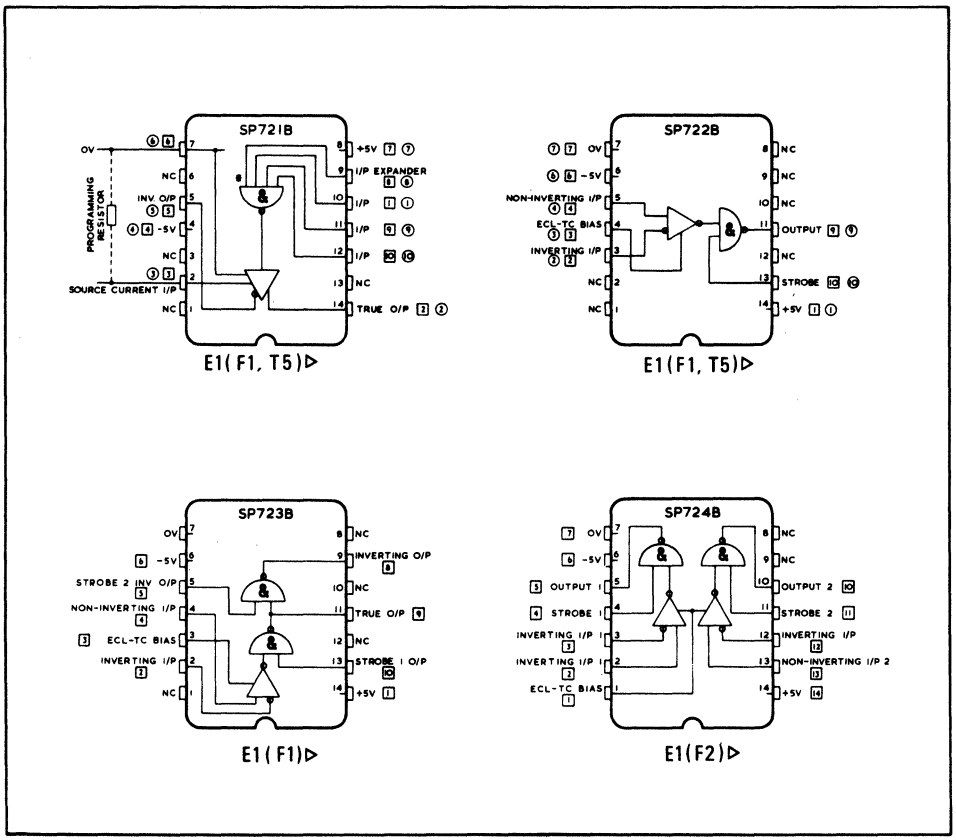


Fig. 1 Logic and dual-in-line package connection diagrams. Connections for package options shown thus: □ = Flatpack, ○ = TO-5.

Absolute Maximum Ratings (all devices unless otherwise stated)

Storage temperature range	−55°C to +175°C	Line input excursion (receivers)	±5V, or power supply rail values, whichever are the lower
Operating temperature range	0°C to +70°C		
Dissipation (at T_{amb} = 70°C) (SP721B)	300 mW		
Positive supply	+6·5V	Line output excursion (SP721B)	+5V to neg. supply
Negative supply	−6·5V	Line input differential voltage (receivers)	6V
Logic input excursion	+5V to −0.5V	Source current input (SP721B)	20mA

Electrical Characteristics (SP721B) @ V_{CC} = +5V ±5%, V_{EE} = −5V ±5%, T = 0 to 70°C

Characteristic	Value			Units	Test conditions
	Min.	Typ.	Max.		
Input voltage for logic '0' O/P	0		800	mV	–
Input current for logic '0' O/P			1·6	mA (neg.)	V_{IN} = 0·4V
Input voltage for logic '1' O/P	2·0			V	–
Input current for logic '1' O/P			40	μA	V_{IN} = 2·4V
Output current at pin 5 for logic '0' O/P			1·0	μA	
Output current at pin 14 for logic '0' O/P	1·4	2·0	2·6	/unit source current	Note 1
Output current at pin 14 for logic '1' O/P			1·0	μA	Note 1
Output current at pin 5 for logic '1' O/P	1·4	2·0	2·6	/unit source current	Note 1
Output current difference between logic '0' and logic '1'			100	μA	Note 1
Permissible output voltage excursion	−3		+3	V	Notes 1 and 2
Mean propagation delay $(t_{pu} + t_{pd})/2$		15		nS	Note 3
Propagation delay skew			5	nS	Note 4
Dissipation		150	260	mW	Note 5
Supply current (+5V)		5·5	7·0	mA	I_{SOURCE} = 10mA
Supply current (−5V)		33	45	mA	I_{SOURCE} = 10mA

SP721B Test Notes (D.I.L. package pins quoted)

1. This result holds for the source current in the range 1 to 10mA (pin 2) and this current is normally determined by a resistor from pin 2 to ground (see fig. 2).
2. The voltage indicated is an absolute voltage and to determine the common mode value, the signal voltage must be subtracted from the absolute voltage. The maximum signal voltage=2·6 x source current x effective load resistor.
3. The time period measured, is from the time when the input passes through the threshold of the circuit, until the output currents at pins 14 and 5, are equal.
4. The propagation delay skew is the time for which the sum of the current at pins 14 and 5 differs from the d.c. value by more than 50% on switching the output state.
5. A duty cycle of 50% is assumed, but if the output is permanently in the logic '1' state the dissipation will be 10mW higher. The source current is set at 10mA.

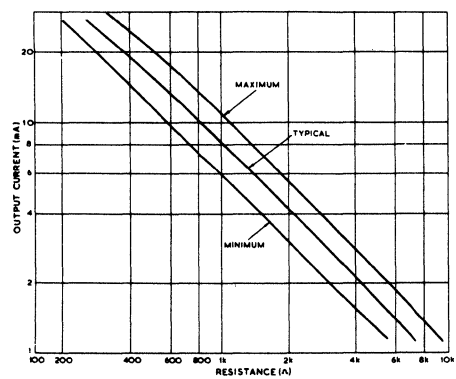


Fig. 2 Output current v. resistance between pin 2 and OV, assuming 5% tolerance on resistance

Electrical Characteristics (SP722/3/4B) @ V_{cc} = +5V ±5%, V_{ee} = −5V ±5%, T = 0 to 70°C.

Characteristic	Circuit	Value			Units	Test conditions
		Min.	Typ.	Max.		
Input voltage (common mode)	All	−3	0	+3	V	–
Input offset	SP722		4·5	15	mV	V_{OUT} = 1·5V
	SP723/724	5	10	15	mV	"
Input threshold	All		4·5		mV	Note 1
Input current	All			100	μA	–
Input capacitance	All		1	2	pF	Note 2
Input current for logic '0' I/P	All			1·6	mA (neg.)	V_{IN} = 0·4V
Input current for logic '1' I/P	All			120	μA	V_{IN} = 2·4V
Output voltage for logic '0' O/P	All			400	mV	I_O = 0 to 16mA
Output voltage for logic '1' O/P	All	2·4			V	I_O = 0 to 400μA
Mean propagation delay	All		20		nS	–
Dissipation	SP722			145	mW	–
	SP723			155	mW	–
	SP724		170	230	mW	–
Short circuit output current	All	18		55	mA	Note 3
Supply current (+5V)	SP722		12	16	mA	–
	SP723		13	18	mA	–
	SP724		19	27	mA	–
Supply current (−5V)	All		9	12·5	mA	–

SP722B, SP723B and SP724B Test Notes

1. Measured from offset to give full logic '0' or logic '1' at output.
2. As input passes through threshold, capacitance temporarily rises to 10pF.
3. Not more than one output should be shorted at any one time. This parameter is measured at the maximum recommended supply voltage.

Operating Notes

The SP721B Balanced line driver, accepts TTL logic inputs, and its output to line is in the form of a differential current sink. The current flows from the line into one of the two output terminals, setting up a differential voltage on the line. The magnitude of this current sink is determined by the value of external programming resistor between pins 7 and 2 (Fig. 1), and is nominally twice the current flowing into pin 2. The size of the differential voltage produced on the line, is dependent on the current chosen and the differential impedance of the line.

A recommended standard is 8mA (minimum) into a 100 Ω line giving an 800mV differential signal.

The line receivers will accept up to a 3V common mode input without being affected, responding only to differential signals producing TTL compatible outputs.

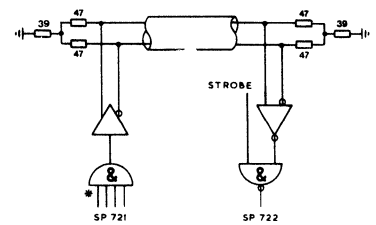
Point to Point Working

Fig. 3 shows a typical configuration with balanced matched lines terminated at both ends. It is possible to match only the differential impedance, but problems may arise from reflected common mode signals which may then exceed the 3V limit. To overcome this problem, the network shown gives a common mode termination of about 60 Ω, corresponding to a typical screened sheath pair cable. Using low loss cable in this way, signals can be transmitted a distance of at least 150 metres, at clock rates up to 5 MHz.

The common mode line figure of 3V can be improved by attenuating the cable signals to the receiver, at the expense of differential sensitivity. Typically an attenuation up to 5 times (14 dB) may be used before the differential error becomes excessive.

When more than one receiver or transmitter are used it is important that all transmitters and receivers connected to a line are always connected to common power supplies.

continued . . .



NOTE: THIS TERMINATION NETWORK CORRESPONDS TO A TWISTED PAIR TRANSMISSION LINE WITH A 100 Ω DIFFERENTIAL CHARACTERISTIC IMPEDANCE AND AN APPROXIMATELY 60 Ω COMMON MODE CHARACTERISTIC IMPEDANCE.

Fig. 3 Typical application

Distribution of Multiple Receivers

Each receiver has only a small disturbing influence, so several receivers may be connected on to one line at different points. However it is possible that common mode problems may be accentuated, so it is often advisable to carry out attenuation as suggested in the paragraph on point to point working.

Multiple Transmitters for Highway Working

By strobing the programming current supplied to pin 2 of the SP721B, the output from that transmitter can be switched on or off. This however produces a large common mode shock which takes time to decay, the decay time depending on the line length and line characteristics. Thus the SP721B can be used for block data transfer, provided sufficient time is allowed between blocks, for the common mode shocks to decay.

NEW PRODUCT DATA

SP761B

12V POWER INTERFACE CIRCUIT

SP762B

5V POWER INTERFACE CIRCUIT

The SP761B and SP762B are bipolar integrated circuits, each incorporating five current amplifiers for interfacing between MOS/TTL devices and loads requiring high drive currents. The SP761B is designed to operate from a +12V supply rail and the SP762B from +5V.

Both types are provided with a strobe input which drives two of the amplifiers so that their outputs may be connected in parallel for higher output current capability.

The circuits operate over a temperature range of 0°C to +70°C and are mounted in 14-lead ceramic DIL package.

Although primarily designed to drive printing solenoids in calculators, these circuits can be used in a variety of applications requiring high drive currents.

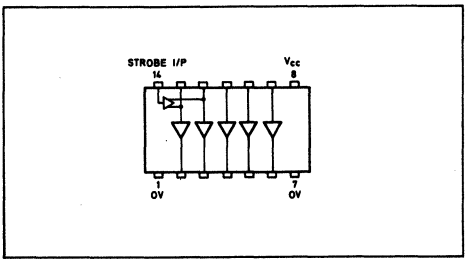


Fig. 1 Pin connections (top)

FEATURES

- Input – MOS/TTL Capability
- Output – 200 mA Capability
- Five Channels per Package
- Open Collector Output

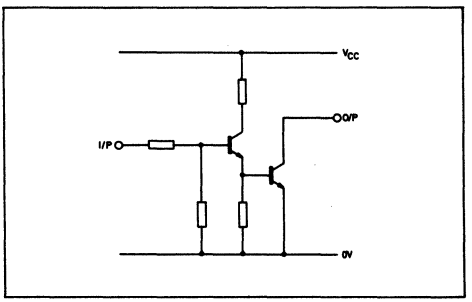


Fig. 2 Functional diagram (one driver)

APPLICATIONS

- Driving Solenoids
- Driving Relays
- Driving LEDs
- Driving Filament Lamps
- Driving Cores
- TTL-to-MOS Translator

ABSOLUTE MAXIMUM RATINGS

Output collector voltage	26V
Supply voltage, SP761B	+15V
Supply voltage ,SP762B	+7V
Storage temp.	−55°C to +125°C
Chip operating temp.	+125°C
Ambient operating temp.	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristic	Type	Value (note 1)			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC}	SP761B	11	12	13	V	See note 2
	SP762B	4.5	5	5.5	V	See note 2
Quiescent supply current	SP761B		8		mA	All inputs low
	SP762B		10		mA	All inputs low
On state supply current, per element	Both		12		mA	I_{IH} = 1mA
Input current I_{IH}	SP761B	1		4	mA	I_{out} = 150mA
Input voltage V_{IH}	SP761B		4		V	I_{IH} = 1mA
Input current I_{IL}	SP761B			50	μA	
Input voltage V_{IH}	SP762B	2.7		5.5	V	I_{out} = 200mA
Input current I_{IH}	SP762B		1		mA	V_{IH} = 2.7V
Input voltage V_{IL}	SP762B			1	V	
Output current I_{out}	SP761B			150	mA	I_{IH} = 1mA
	SP762B			200	mA	V_{IH} = 2.7V
Output voltage V_{OL}	SP761B		1.0	1.2	V	I_{out} = 150mA
	SP762B		1.3	1.6	V	I_{out} = 200mA
Output voltage V_{OH}	Both			26	V	
Output breakdown voltage	Both	26			V	See note 3
Duty cycle	SP761B			40	%	All outputs at I_{out} max.
	SP762B			33	%	
On time				2	s	

NOTES

1. Both 0V supply pins 1 and 7 must be connected at all times.
2. Min. and max. limits apply to the temperature range 0°C to +70°C. All typical values are quoted for V_{CC} = Typical and T_{amb} = +25°C.
3. External clamping diodes must be used when driving inductive loads.

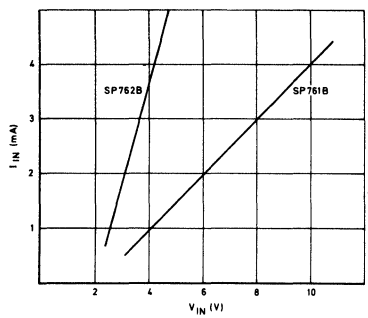


Fig. 3 Input characteristic (including strobe) T_{amb} = +25°C

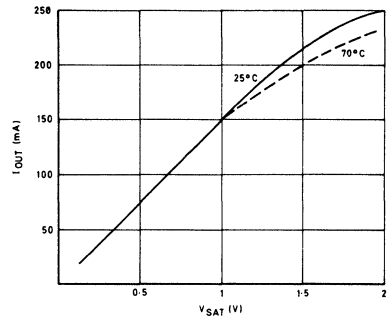


Fig. 4 Output characteristic

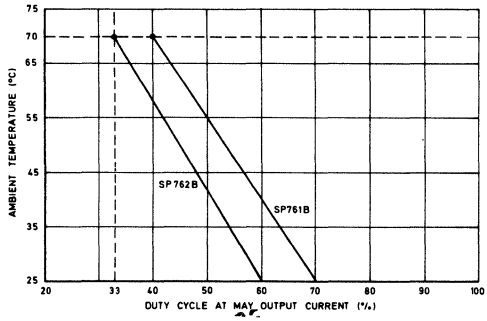


Fig. 5 Operating characteristics

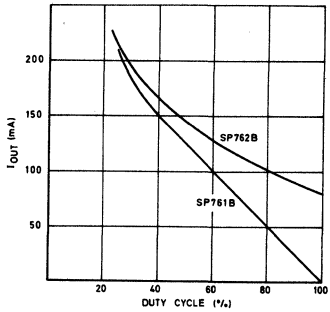


Fig. 6 Operating characteristics at +70°C

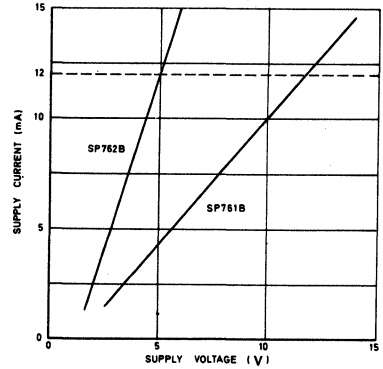


Fig. 7 On state supply current drain per element

OPERATING NOTES

Interfacing

The SP761B is designed to interface directly with MOS devices, accepting free drain input currents in the range 1 mA to 4 mA. Current limiting input resistors are incorporated on-chip to reduce power dissipation in the MOS circuit. The resistor is approximately 2 kΩ, giving an input voltage of 4V at 1 mA.

Fig. 8 shows (i) a direct interface to MOS and (ii) an interface using an external resistor to further limit input current when driven from a high voltage source.

The SP762B will interface directly with standard TTL over the temperature range 0°C to +70°C, a TTL logic '1' making current available at the SP762B output. Although TTL is not specified to source more than 400 μA at logic '1' level, the majority of gates will in fact supply approximately 5 mA and still maintain a logic '1' level in excess of 2.7V. Since the input resistors of the SP762B are approximately 600Ω, then one TTL output is capable of driving up to 5 SP762B inputs. When driving only one input of an SP762B, the input current will limit at approximately 2 mA at 3.4V. Open-collector TTL gates can also be used to drive the SP762B, provided that each TTL output has an external load resistor, the value of which will depend on the fanout required.

The characteristics of the strobe input are the same as for the individual inputs and therefore the above comments also apply to this input.

Unused Inputs

When using the strobe input, inputs 1 and 2 must be left floating. However, inputs 1 and 2 can be used completely independently in the same way as the other inputs. Any other unused inputs can either be left floating or tied to the negative supply rail.

Output Capability

The output capability of each channel is 150 mA for the SP761B and 200 mA for the SP762B. With all five drivers operating at these current levels, a duty cycle of 40% for the SP761B and 33% for the SP762B will allow operation over the temperature range 0°C to +70°C.

If the device is to be operated at a lower ambient temperature, or at a lower output current, then the duty cycle may be increased as shown in Fig. 6 and 7. Likewise, if some of the outputs are unused the duty cycle of the remaining outputs may be proportionally increased provided that the drivers are used symmetrically within the package.

The package has a thermal time constant such that the chip temperature will rise above the permitted maximum of +125°C if all the drivers are allowed to remain on at maximum output current for more than 2 seconds.

The drivers will operate at up to 1 MHz but at such frequencies the input mark/space ratio will have to be modified because the effective output duty cycle is higher than that at the inputs due to stored charge in the output transistors.

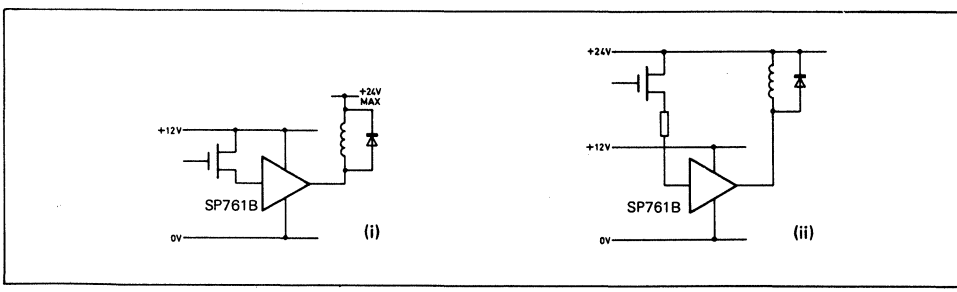
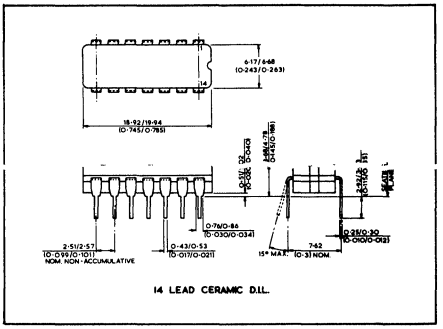


Fig. 8 Interfacing to MOS

PACKAGE DETAILS

Dimensions are shown thus: mm (in.)



14 LEAD CERAMIC D.I.L.

NEW PRODUCT DATA

SP763 B SP764 B SP765 B

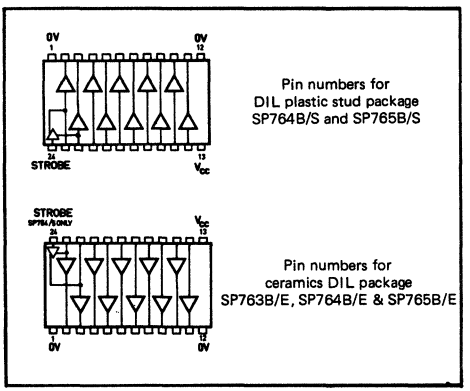
POWER INTERFACE CIRCUITS

The SP763/4/5 are bipolar integrated circuits each incorporating 10 current amplifiers for interfacing between MOS/TTL devices and loads requiring high drive currents. The SP763 and SP764 are designed to operate from an MOS compatible supply of typically +12V whereas the SP765 is designed for a TTL supply rail of +5V.

The SP764/5 are provided with a strobe input which drives two of the amplifiers so that their outputs can be connected in parallel for higher output current capability.

The circuits operate over a temperature range of 0°C to +70°C and are available in 24-lead DIL ceramic package or 24-lead DIL plastic stud (SP764B and SP765B only), for applications requiring higher dissipation.

Although primarily designed to drive printing solenoids in calculators, these circuits can be used in a variety of applications – including driving filament lamps, L.E.D.s, relays, cores and other devices requiring high drive currents e.g., power transistors.



FEATURES

- 200mA Output Capability
- MOS/TTL Compatible
- On-Chip Input Current Limiting Resistors
- Zero Standby Power
- Direct interface to Seiko and similar printers

APPLICATIONS

- Driving Solenoids
- Driving Relays
- Driving L.E.D.s
- Driving Filament Lamps
- Driving Cores
- TTL-to-MOS Translator

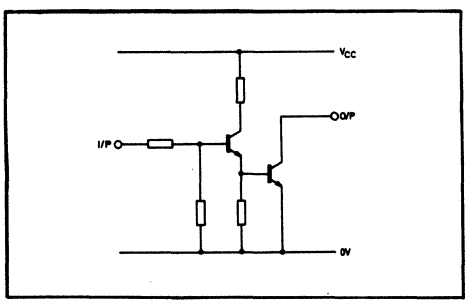


Fig. 1 One driver element

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	
SP763B & SP764B	+15V
SP765B	+7V
Storage temperature	−55°C to +125°C
Chip operating temperature	+125°C
Ambient operating temperature	0°C to +70°C

ELECTRICAL CHARACTERISTICS

Characteristic	Type	Value (note 1)			Units	Conditions
		Min.	Typ.	Max.		
Operating supply voltage, V_{CC}	SP763B					
	SP764B	11.0	12.0	13.0	V	Note 2
Operating supply voltage, V_{CC}	SP765B	4.5	5.0	5.5	V	
Supply current per element	SP764/765B		12.0		mA	I_{in} = 1mA
Supply current per element	SP763B		5		mA	I_{in} = 1mA
Input current, I_{IH}	SP763/764B	1		4	mA	
Input voltage, V_{IH}	SP763/764B		4		V	I_{in} = 1mA
Input current, I_{IL}	SP763/764B			50	μA	
Input voltage, V_{IH}	SP765B	2.7		5.5	V	
Input current, I_{IH}	SP765B		1		mA	V_{in} = 2.7V
Input voltage, V_{IL}	SP765B			1	V	
Strobe high input current, I_{SH}	SP764/765B	1		4	mA	
Strobe high input voltage, V_{SH}	SP764/765B		4		V	I_{SH} = 1mA
Output current, I_{out}	SP763B			50	mA	I_{in} = 1mA
Output current, I_{out}	SP764B			150	mA	I_{in} = 1mA
Output current, I_{out}	SP765B			200	mA	I_{in} = 1mA
Output voltage low, V_{OL}	SP764B		1.0	1.2	V	I_{out} = 150mA
(saturation voltage)	SP765B		1.3	1.6	V	I_{out} = 200mA
Output breakdown	SP763B	12			V	Note 3
voltage, B_{VO}	SP764/765B	26			V	Note 3
Duty cycle Ceramic package	SP763B			100	%	I_{out} = Max.
Ceramic package	SP764B			25	%	At I_{out} = Max.
Ceramic package	SP765B			25	%	I_{in} = 1mA
Plastic package	SP764B			40	%	T_A = +70°C
Plastic package	SP765B			40	%	V_{CO} = Typ.
ON time	SP764/765B			2	sec.	

NOTES

1. Min. and Max. limits apply to the guaranteed temperature range of 0°C to +70°C unless otherwise specified. All typical values are quoted for V_{CC} = Typ. and T_A = +25°C.
2. Both 0V supply pins 1 and 12 must be connected at all times.
3. External clamping diodes must be used when driving inductive loads.

Typical Performance Characteristics

In the following characteristics (Figs. 3 to 10), V_{CC} = + 12V (SP763, SP764B) or + 5V (SP765B).

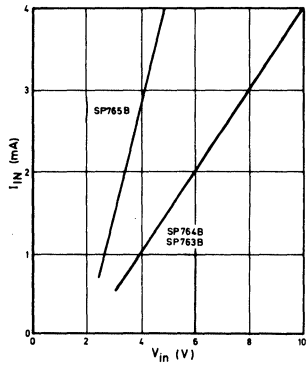


Fig. 3 Input characteristics (T_A = +25°C)

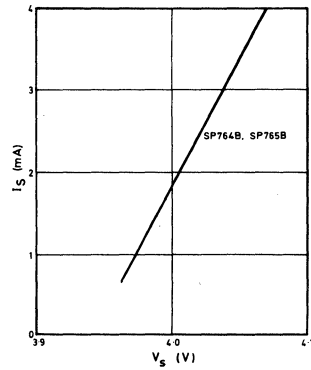


Fig. 4 Strobe input characteristics (T_A = +25°C)

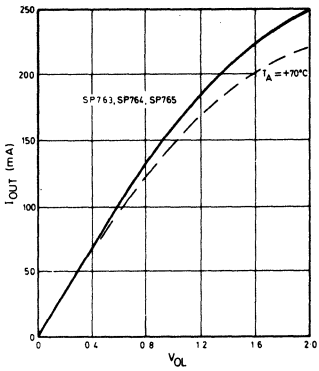


Fig. 5 Output characteristics (T_A = +25°C)

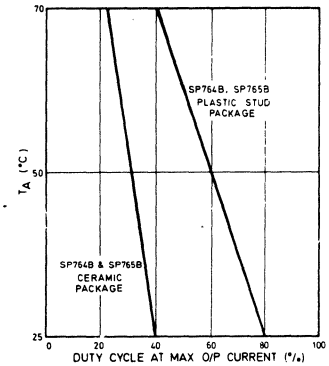


Fig. 6 Operating characteristics (T_A = +25°C to +70°C)

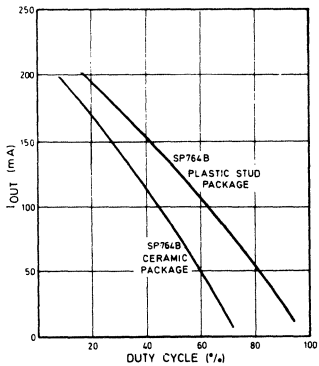


Fig. 7 SP764 operating characteristics (T_A = +70°C max.)

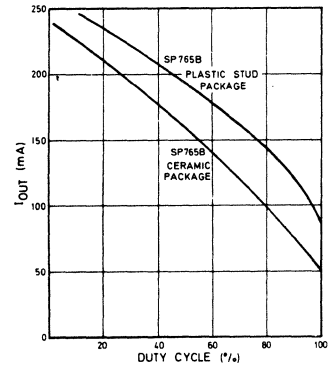


Fig. 8 SP765 operating characteristics (T_A = +70°C max.)

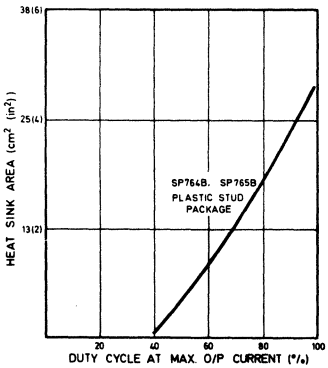


Fig. 9 Operating characteristics, stud package with heatsink (T_A = +70°C max.)

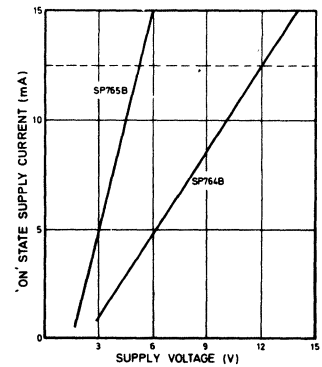
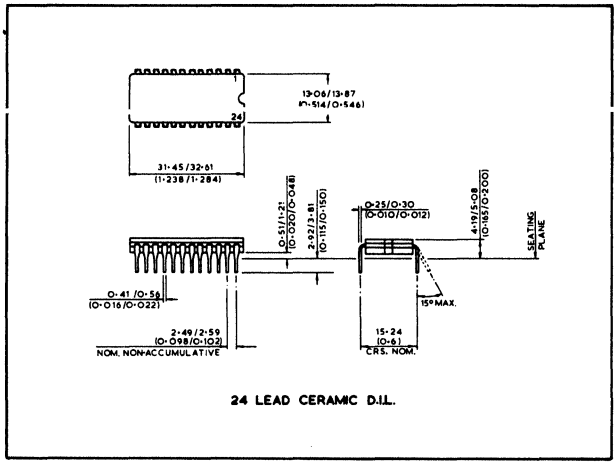


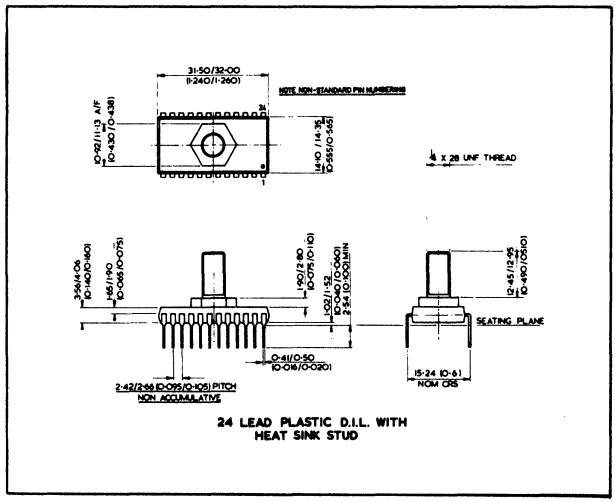
Fig.10 Current drain per element (T_A = +70°C max.)

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



24 LEAD CERAMIC D.I.L.



24 LEAD PLASTIC D.I.L. WITH HEAT SINK STUD

Publication No. P.S. 1432 Feb. 1975

OPERATING NOTES

Interfacing

The SP763/764 are designed to interface directly with MOS devices, accepting free drain input currents in the range 1mA to 4mA. Current-limiting input resistors are incorporated on-chip to reduce power dissipation in the MOS circuit. The resistor is approximately 2kΩ giving an input voltage of 4V at 1mA (see Figs.3 and 4).

Fig.11 shows (i) a direct interface to MOS and (ii) an interface using an external resistor to further limit input current when driven from a high voltage source.

The SP765B will interface directly with standard TTL over the temperature range 0°C to +70°C, a TTL logic '1' making current available at the SP765 driver output. Although TTL is not specified to source more than 400μA at the logic '1' level, a typical gate will in fact supply approximately 5mA and still maintain a logic '1' level of about +2.7V. Since the input current – limiting resistors on the SP765 are approximately 700Ω (giving an input voltage of +2.7V at 1mA) then one TTL output is capable of driving up to 5 SP765 inputs. If, however, a TTL gate is used to drive only one SP765 input, then the current will limit at approximately 2mA, corresponding to an input voltage of +3.4V. Open-collector TTL gates can also be used to drive SP765s but in such cases each TTL output must have an external load resistor, the value of which will depend on the fanout required.

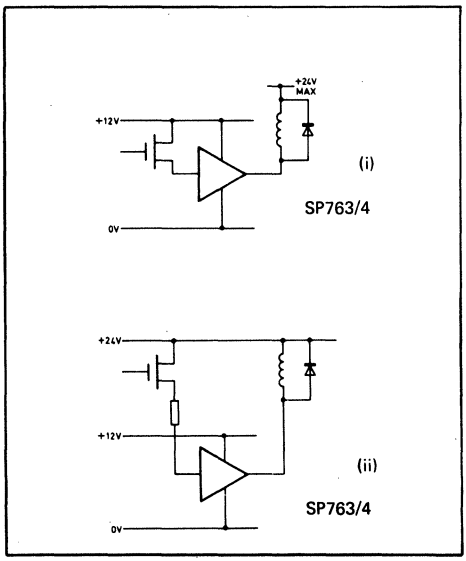


Fig. 11 Interfacing SP763/SP764 to MOS

Strobe Input

A positive voltage (as defined in the Electrical Characteristics) applied to the strobe input (pin 24) enables drivers 1 and 2 simultaneously. Thus, using this input permits output current sinking of up to 300 mA (SP764B) and 400 mA (SP765B) by connecting together outputs 1 and 2 (pins 2 and 3).

No current limiting resistor is provided at the strobe input as the input voltage at 1mA is 4V on all circuit variants (see Fig.4). When using the SP765B, therefore, the strobe input must be driven either from an open-collector TTL gate with an appropriate load resistor or from a normal TTL gate with an external 1kΩ resistor between its output and V_{CC} as shown in Fig.12.

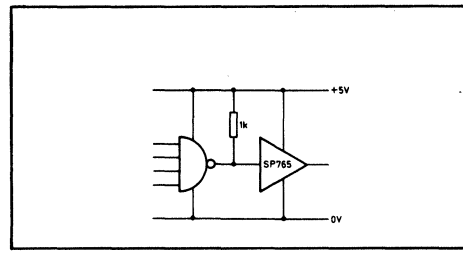


Fig.12 TTL interface to SP765 strobe input

Unused Inputs

When using the strobe input, inputs 1 and 2 must be left floating. However, inputs 1 and 2 can be used completely independently, in the same way as the other inputs. Any other unused inputs can either be left floating or tied to the negative supply rail.

Output Capability

The SP763B has an output rating for each driver of 50mA and may be used over the full temperature range of 0°C to +70°C at 100% duty cycle.

The SP764B has an output rating of 150mA for each driver and the SP765B a rating of 200mA. With all ten drivers operating at these current levels a duty cycle of 25% for the ceramic package and 40% for the plastic stud package will allow operation over the temperature range 0°C to +70°C.

If a lower ambient operating temperature can be tolerated, then the duty cycle may be increased up to a maximum of 40% (ceramic) and 80% (plastic stud) at +25°C. Operation of the drivers at lower output currents will also allow the duty cycle to be increased, as shown in Figs.6, 7, 8 and 9. In addition, if some of the outputs are unused, then the duty cycle of the remaining outputs may be increased, provided that the drivers are used symmetrically within the package. For example, if outputs 5 and 6 are not used, then the duty cycle of the remaining 8 outputs can be increased in the ratio 10:8.

The drivers will operate at up to 1MHz but at such frequencies the input signal mark/space ratio will have to be modified because the effective output duty cycle is higher than that of the inputs due to charge storage in the output transistors.

Because of the high current levels which the drivers are capable of making it is essential that both the O_V pins should be connected. The track resistance to each pin should be approximately equal to ensure equal current sharing.

Plastic Stud Package

With the addition of a heat risk of thermal resistance not greater than 12°C/Watt, operation at up to 100% duty cycle (i.e. D.C. operation at maximum output current) can be achieved over the full temperature range 0°C to +70°C. A suitable heat sink consists of 25 cm^2 (4 in^2) of 16 SWG Aluminium folded as shown in Fig. 13.

Note: On the stud package, the stud is connected to the negative rail.

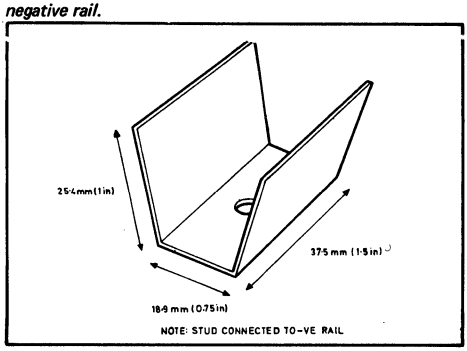


Fig. 13 Heatsink details for stud package

Typical Application

A typical calculator application for SP764/SP765 devices is shown in Fig.14. In this, two packages are required to drive the 18 printing solenoids and the paper/ribbon feed solenoid. The 10 drivers in one package are used to drive 10 printing solenoids and the remaining 8 solenoids are driven by outputs 3 to 10 of the second package. The paper/ribbon feed solenoid is controlled by the strobe input of the second package and driven by the parallel outputs 1 and 2.

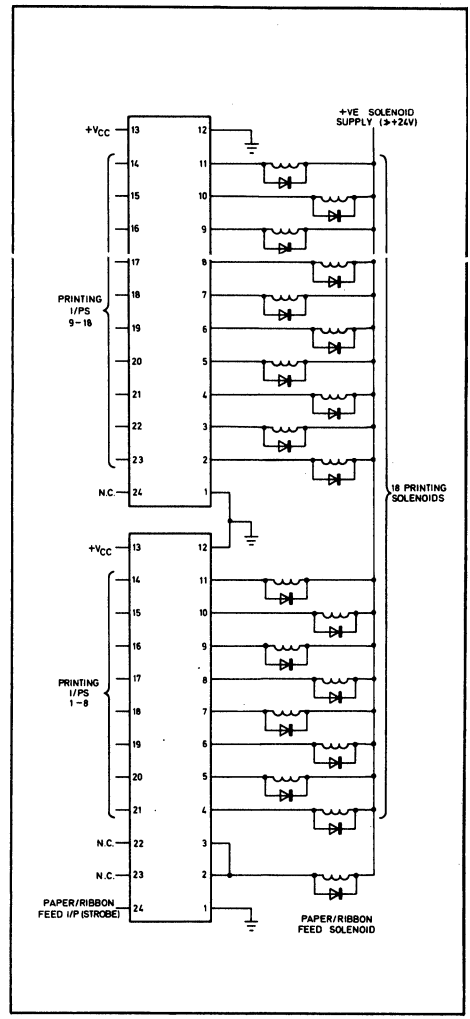


Fig. 14 Typical printing calculator application

ORDERING INFORMATION

The type number, for ordering purposes, consists of the basic number SP763B, SP764B or SP765B followed by /E for ceramics DIL or /S for the plastic stud package, e.g. SP765B/S.

The package code is for ordering purposes only and does not appear on the device itself.

PECL II

FEATURES

- Propagation typically 4ns per logic decision.
- Excellent noise immunity characteristics
- Simultaneous OR/NOR outputs
- High fan-in and fan-out capabilities
- Internally temperature compensated

The PECL II series of monolithic integrated logic circuits are a direct second source of the Motorola MECL II series. The family has been designed as a non-saturating form of logic so as to eliminate transistor storage time as a speed limiting characteristic and permits high speed operation.

PECL II circuits feature fast propagation delay times with commensurate rise and fall times, simultaneous complementary outputs, and excellent noise immunity as a result of near constant power supply drain.

FUNCTIONS AND CHARACTERISTICS @ V_{CC} = OV, V_{EE} = −5.2V, T_A = +25°C

Type 0°C to +75°C	Type −55°C to +125°C	Function	D.C. output loading factor, each output	Propagation delay ns typ.	Total power dissipation mW typ.
SP1001	SP1201	Single 6 I/P gate, 3 OR O/P with pulldowns 3 NOR O/P with pulldowns	25	4.0	115
SP1002	SP1202	Single 6 I/P gate, 3 OR O/P with pulldowns 3 NOR O/P without pulldowns			80
SP1003	SP1203	Single 6 I/P gate, 3 OR O/P without pulldowns 3 NOR O/P without pulldowns			40
SP1004	SP1204	Dual 4-I/P gate, 2 OR with pulldowns 2 NOR with pulldowns			95
SP1005	SP1205	Dual 4-I/P gate, 2 OR with pulldowns 2 NOR without pulldowns			65
SP1006	SP1206	Dual 4-I/P gate, 2 OR without pulldowns 2 NOR without pulldowns			45
SP1007	SP1207	Triple 3-I/P gate, 3 NOR with pulldowns			110
SP1008	SP1208	Triple 3-I/P gate, 1 NOR with pulldowns 2 NOR without pulldowns			75
SP1009	SP1209	Triple 3-I/P gate, 3 NOR without pulldowns			60
SP1010	SP1210	Quad 2-I/P gate, 4 NOR with pulldowns		4.5	115
SP1011	SP1211	Quad 2-I/P gate, 2 NOR with pulldowns 2 NOR without pulldowns			95
SP1012	SP1212	Quad 2-I/P gate, 4 NOR without pulldowns			65
SP1013	SP1213	85 MHz a.c. coupled J-K flip-flop		6.0	125
SP1014	SP1214	Dual R-S flip-flop (+ve clock)			140
SP1015	SP1215	Dual R-S flip-flop (−ve clock)			
SP1016	SP1216	Dual R-S flip-flop (single rail, +ve clock)			
SP1020	SP1220	Quad line receiver		4.0	115
SP1023	SP1223	Dual 4-I/P OR/NOR clock driver		2.0	250
SP1026	SP1226	Dual 3-4I/P Transmission line and clock driver		2.0	140
SP1027	SP1227	120 MHz a.c. coupled J-K flip-flop		4.0	250
SP1030	SP1230	Quad exclusive OR gate		5.0	130
SP1031	SP1231	Quad exclusive NOR gate		5.0	130

continued . . . .

FUNCTIONS AND CHARACTERISTICS @ V_{CC} = OV, V_{EE} = −5.2V, T_A = +25°C (continued)

Type 0°C to +75°C	Type −55°C to +125°C	Function	D.C. output loading factor, each output	Propagation delay ns typ.	Total power dissipation mW typ.
SP1032*	SP1232*	100 MHz a.c. coupled Dual J-K flip-flop	25	4·5	180
SP1033	SP1233	Dual R-S flip-flop (single rail, −ve clock)		6·0	140
SP1034	SP1234	Type D flip-flop		4·0	185
SP1035	SP1235	Triple line receiver		5·0	140
SP1039*	SP1239*	Quad level translator (PECL to saturated logic)	7 (DTL)	12	200
SP1040	SP1240	Quad latch with pulldowns	25	8·0	250
SP1047	SP1247	Quad 2-I/P AND gate		5·0	130
SP1048	SP1248	Quad 2-I/P NAND gate		5·0	130
SP1062*	SP1262*	Quad 2-I/P NOR gate		2·0	320
SP1063	SP1263	Quad 2-I/P NOR gate		2·0	320
SP1070	SP1270	Quad latch without pulldowns		8·0	200

* In 16– lead D.I.L. All other types are in 14– lead D.I.L.

General Parameters

COMMON CHARACTERISTICS

Characteristic	SP1200 −55° Min.	SP1200 −55° Max.	SP1200 +25°C Min.	SP1200 +25°C Max.	SP1200 +125°C Min.	SP1200 +125°C Max.	SP1000 0°C Min.	SP1000 0°C Max.	SP1000 +25°C Min.	SP1000 +25°C Max.	SP1000 +75°C Min.	SP1000 +75°C Max.
Input current I_{in}				100 μA						100 μA		
Input leakage I_R				0·2μA		1μA				0·2μA		1μA
Output voltage[2]												
Logic '1' (V_{OH})	−0·990	−0·825	−0·85	−0·70	−0·70	−0·53	−0·895	−0·74	−0·85	−0·70	−0·775	−0·615
Logic '0' (V_{OL})	−1·89	−1·58	−1·8	−1·5	−1·72	−1·38	−1·83	−1·525	−1·8	−1·5	−1·76	−1·435

NOTES 1. The above characteristics apply unless otherwise stated under individual product information.
2. Outputs without pulldown resistors are tested with 1·5kΩ resistor to V_{ee} and V_{OH} limits apply from no load (0 mA) to full load (−2·5 mA).
3. General parameters only apply to basic gates and flip-flops.

TEST CONDITIONS

Test Temp. °C	Test Voltage/Current Values V_{IL}(V) Min.	V_{IL}(V) Max.	V_{IH}(V) Min.	V_{IH}(V) Max.	V_{IH} (max.) (V)	Vee (V)	I_L (m.Ad.c.)
−55	−5·2 to −1·405		−1·165 to −0·825		–	−5·2	−2·5
+25	to −1·325		−1·025 to −0·700		−0·700		
+125	to −1·205		−0·875 to −0·530		–		
0	to −1·350		−1·070 to −0·740		–		
+25	to −1·325		−1·025 to −0·700		−0·700		
+75	to −1·260		−0·950 to −0·615		–		

Logic Diagrams

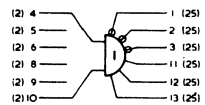
The logic diagrams describe the circuits of the PECL II series and permit quick selection of those circuits required to implement a particular logic system. The Logic equations and truth tables shown with the logic diagrams, together with typical propagation delay times (t_{pd}) and typical power dissipation per package given in the characteristics table demonstrate series compatibility.

Package pin numbers are identified by numbers directly adjacent to the device terminals, whereas the numbers in parentheses indicate d.c. loading factors at each terminal. PECL II circuits contain internal bias networks, ensuring that the transition point is always in the centre of the transfer characteristic curves over the temperature range

V_{CC} = pin 14 and V_{EE} = pin 7 for all devices (14- lead D.I.L.) except SP1032/1232, SP1039/1239 and SP1062/1262, where V_{CC} = pin 16 and V_{EE} = pin 8 (16- lead D.I.L.)

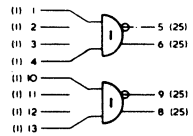
GATES

SP1001, SP1002, SP1003
SP1201, SP1202, SP1203
6– Input Gate



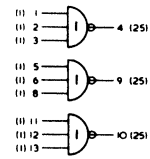
$1 = \overline{4 + 5 + 6 + 8 + 9 + 10}$
$11 = \overline{4 + 5 + 6 + 8 + 9 + 10}$

SP1004, SP1005, SP1006
SP1204, SP1205, SP1206
Dual 4– Input Gate



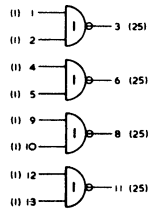
$5 = \overline{1 + 2 + 3 + 4}$
$6 = \overline{1 + 2 + 3 + 4}$

SP1007, SP1008, SP1009
SP1207, SP1208, SP1209
Triple 3– Input Gate



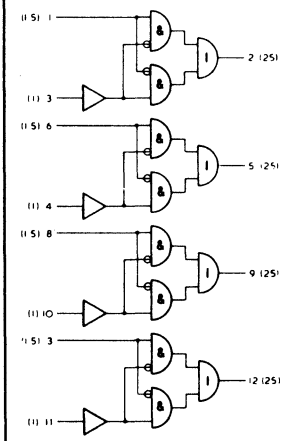
$4 = \overline{1 + 2 + 3}$

SP1010, SP1011, SP1012
SP1210, SP1211, SP1212
SP1063, SP1263
Quad 2– Input NOR Gate



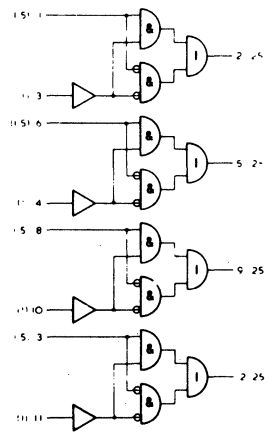
$3 = \overline{1 + 2}$

SP1030, SP1230
Quad Exclusive OR Gate



$2 = 1 \cdot \overline{3} + \overline{1} \cdot 3$

SP1031, SP1231
Quad Exclusive NOR Gate

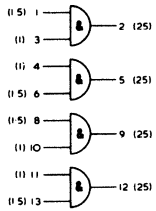


$2 = 1 \cdot 3 + \overline{1} \cdot \overline{3}$

GATES (continued)

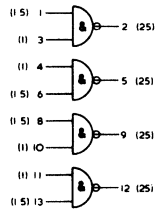
SP1047, SP1247
Quad 2– Input AND Gate

$2 = 1 \cdot 3$



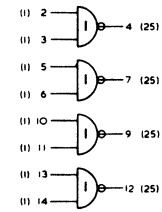
SP1048, SP1248
Quad 2– Input NAND Gate

$2 = \overline{1 \cdot 3}$



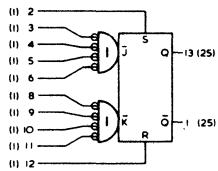
SP1062, SP1262
Quad 2– Input NOR Gate

$4 = \overline{2 + 3}$

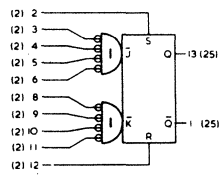


FLIP-FLOPS

SP1013, SP1213
A.C. – Coupled J–K Flip-Flop
(85 MHz typ.)



SP1027, SP1227
A.C. – Coupled J–K Flip-Flop
(127 MHz typ.)



CLOCKED J–K OPERATION			
$\overline{J}$	$\overline{K}$	$\overline{C}_D$	$Q^n + 1$
Δ	Δ	0	Q^n
0	0	1	$\overline{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

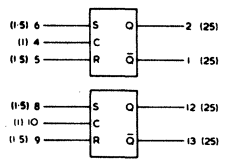
Δ = Either logic level

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels whereas the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to logic '1' only while $\overline{C}_D$ is in the logic '1' state. ($\overline{C}_D$ maximum '1' level = V_{CC} –0·6V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

R–S OPERATION		
R	S	$Q^n + 1$
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

N.D. = Not defined

SP1014, SP1015
SP1214, SP1215
Dual Clocked R–S Flip-Flop



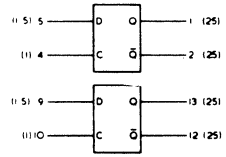
SP1014/1214			
C	R	S	$Q^n + 1$
1	0	0	Q^n
1	0	1	1
1	1	0	0
1	1	1	N.D.
0	Δ	Δ	Q^n

SP1015/1215			
C	R	S	$Q^n + 1$
0	0	0	Q^n
0	0	1	1
0	1	0	0
0	1	1	N.D.
1	Δ	Δ	Q^n

Δ = Either logic state
N.D. = Not defined

FLIP-FLOPS (continued)

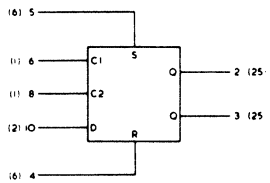
SP1016, SP1033
SP1216, SP1233
Dual Clocked, Single Rail, R–S Flip-Flop



SP1016/1216		
C	D	Q^{n+1}
0	0	Q^n
0	1	Q^n
1	0	0
↓	*	*

SP1033/1233		
C	D	Q^{n+1}
1	0	Q^n
1	1	Q^n
0	0	0
↓	*	*

SP1034, SP1234
Type D Flip-Flop



P_D = 185 mW using external 600Ω pulldown resistors
= 240 mW using internal pulldown resistors.

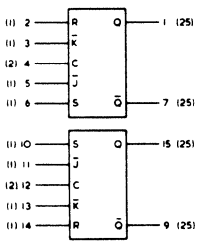
R–S TRUTH TABLE			
R	S	Q^{n+1}	Q^{n+1}
4	5	2	3
0	0	Q^n	$\bar{Q}^n$
0	1	1	0
1	0	0	1
1	1	N.D.	N.D.

N.D. = Not defined

CLOCKED TRUTH TABLE			
D	C	Q^{n+1}	Q^{n+1}
10	6 or 8	2	3
0	0	Q^n	$\bar{Q}^n$
1	0	Q^n	$\bar{Q}^n$
0	1*	0	1
1	1*	1	0

* A '1' or clock input is defined for this flip-flop as a change in level from low to high.

SP1032, SP1232
100 MHz AC-Coupled Dual
J–K Flip-Flop



$\bar{J}_D - \bar{K}_D$ TRUTH TABLE		
$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
*	*	1 & 15
0	0	Q^n
0	1	0
1	0	1
1	1	$\bar{Q}^n$

All Clock/R–S inputs are at a '0' Level.

R–S TRUTH TABLE		
R	S	Q^{n+1}
2 & 14	6 & 10	1 & 15
0	0	Q^n
0	1	1
1	0	0
1	1	N.D.

All $\bar{J}$–$\bar{K}$ inputs and Clock inputs are static
N.D. = Output state not defined

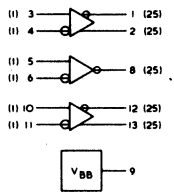
CLOCKED $\bar{J}$–$\bar{K}$ TRUTH TABLE			
$\bar{J}$	$\bar{K}$	Clock	Q^n
*	*	4 & 12	1 & 15
Δ	Δ	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	$\bar{Q}^n$

* Any $\bar{J}$ or $\bar{K}$ input
All other $\bar{J}$ –$\bar{K}$ inputs and the R–S inputs are at a '0' Level
Δ = Either logic level will result in the desired output.

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the clock input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logic '1' only while the clock input is in a logic '1' state (Clock maximum '1' level = V_{CC} –0·7 V).

TRIPLE LINE RECEIVER

SP1035, SP1235
Triple Line Receiver



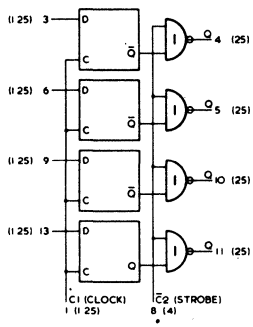
TRUTH TABLE			
INPUTS		OUTPUTS	
3	4	1	2
5	6	8	–
10	11	12	13
H	V_{BB}	L	H
L	V_{BB}	H	L
V_{BB}	H	H	L
V_{BB}	L	L	H

OR ▭
NOR ■

The output polarities shown in the logic diagrams are true only when V_{BB} is applied to pins 4, 6 and 11

LATCH

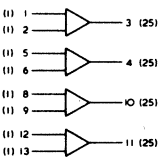
SP1040, SP1070
SP1240, SP1270
Quad Latch



TRUTH TABLE			
D	C1	$\overline{C2}$	Q^{n+1}
0	0	0	Q^n
1	0	0	Q^n
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

RECEIVER

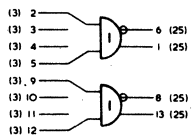
SP1020, SP1220
Quad Line Receiver



DRIVERS

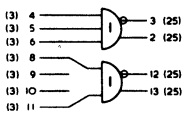
SP1023, SP1223
Dual 4– Input Clock Driver

$6 = \overline{2+3+4+5}$
$1 = \overline{2+3+4+5}$



SP1026, SP1226
Dual 3–4 Input Transmission Line and Clock Driver

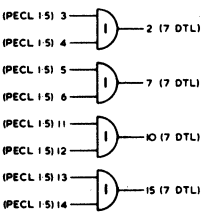
$3 = \overline{4+5+6}$
$2 = \overline{4+5+6}$



LEVEL TRANSLATOR

SP1039, SP1239
Quad Level Translator

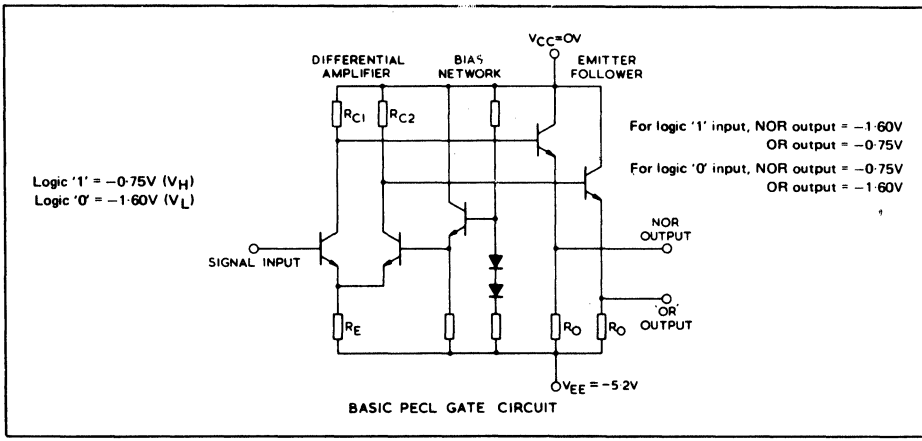
$2 = \overline{3+4}$
or $2 = \overline{3+4}$



CIRCUIT DESCRIPTION

The PECL II line of monolithic integrated logic circuits was designed as a non-saturating form of logic which eliminates transistor storage time as a speed limiting characteristic, and permits extremely high-speed operation.

The typical PECL II circuit comprises a differential-amplifier input with internal bias reference and with emitter-follower output to restore dc levels. High fan-out operation is possible because of the high input impedance of the differential amplifier and the low output impedance of the emitter followers Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the function and its complement.



BASIC PECL GATE CIRCUIT

POWER-SUPPLY CONNECTIONS

As shown in the schematic diagram above, it is recommended that −5·2 V be applied at V_{EE} with V_{CC} = Gnd.

SYSTEM LOGIC SPECIFICATIONS

The nominal output logic swing of 0·85 V then varies from a low state of V_L = −1·60 V to a high state of V_H = −0·75 V with respect to ground.

If Positive logic is used when reference is made to logical zeros or ones then

'0' = −1·60 V
'1' = −0·75 V typical

Dynamic logic refers to a change of logic states. Dynamic '0' is a negative going voltage excursion and a dynamic '1' is a positive going voltage excursion.

CIRCUIT OPERATION

An internal bias of −1·175 V is applied to the 'bias input' of the differential amplifier and the logic signals are applied to the 'signal input'. If a logical '0' is applied, the current through R_E is supplied by the internally biased transistor. A drop of 0·85 V occurs across R_{C2}. The OR output then is −1·60 V, or one V_{BE} drop below 0·85 V. Since no current flows in the 'signal input' transistor, the NOR output is a V_{BE} drop below ground, or −0·75 V. When a logical '1' level is applied to the 'signal input' the current through R_{C2} is switched to the 'signal input' transistor and a drop of 0·85 V occurs across R_{C1}. The OR output then goes to −0·75 V and the NOR output goes to −1·60 V.

Note: Any unused input should be connected to V_{EE}.

BIAS VOLTAGE SOURCE

The bias voltage applied to the bias input is obtained from an internal regulated, temperature compensated bias network. The temperature characteristics of the bias network compensate for any variations in circuit operating point over the temperature-range or supply voltage changes, and ensure that the threshold point is always in the centre of the transfer characteristic curves.

MAXIMUM RATINGS

Ratings above which device life may be impaired

Characteristic	Symbol	Rating
Power supply voltage (V_{CC} = 0)	V_{ee}	−10V d.c.
Input voltage (V_{CC} = 0)	V_{in}	0 to V_{ee}
Output source current	I_O	20mA d.c.
Storage temperature range	$T_{stg.}$	−65°C to +175°C

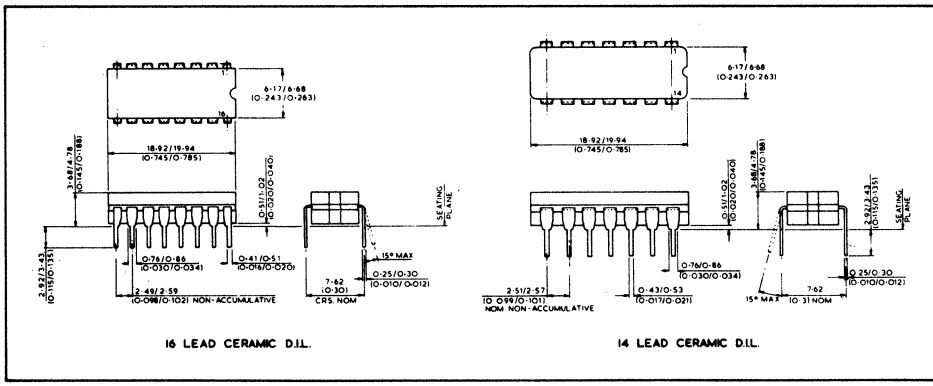
Recommended Maximum ratings above which performance may be degraded

Characteristic		Rating
Operating temperature range		
	SP1000	0°C to +75°C
	SP1200	−55°C to +125°C
A.C. fanout* (gates and flip-flops)		15

* Minimum d.c. fanout is guaranteed at 25; an a.c. fanout of 15 is recommended for high-speed operation.

PACKAGE OUTLINES AND DIMENSIONS

Note: Dimensions are shown thus: mm (inches).



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PLESSEY
SEMICONDUCTORS

Publication No. P.S.1445 Feb. 1975

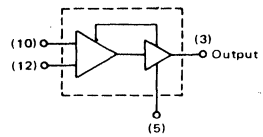
PECL III

LOW Z DEVICES ALSO AVAILABLE ARE:

SP1661
SP1663
SP1665
SP1667
SP1669
SP1671
SP1673
SP1675

VOLTAGE-CONTROLLED
OSCILLATOR

SP1648



Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silcon chip. Output levels are compatible with PECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The SP1648 is used in the Phase-Locked Loop shown in Figure 9. This device may be used in many applications requiring a fixed or variable frequency clock source of high spectral purity (See figure 2).

The SP1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC

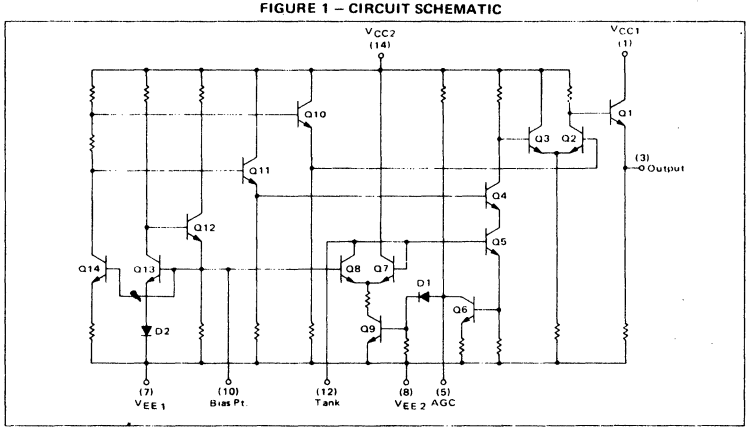
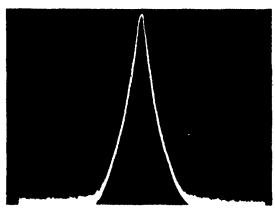
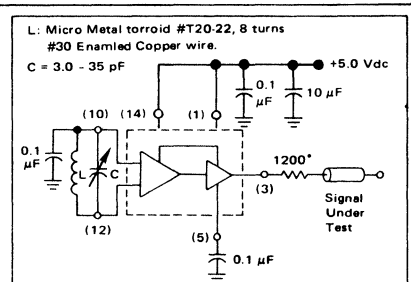


FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT

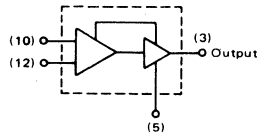


B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts



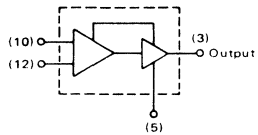
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+85°C	+1.680	+1.180	5.0	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	40	—	—	mAdc	—	—	1, 14	—	7, 8
Logic "1" Output Voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	1, 14	3	7, 8
Logic "0" Output Voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	—	1, 14	3	7, 8
Bias Voltage	V_{Bias}*	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	—	—	1, 14	—	7, 8
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	1, 14	3	7, 8
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	1, 14	3	7, 8
Oscillation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	1, 14	3	7, 8

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 volts

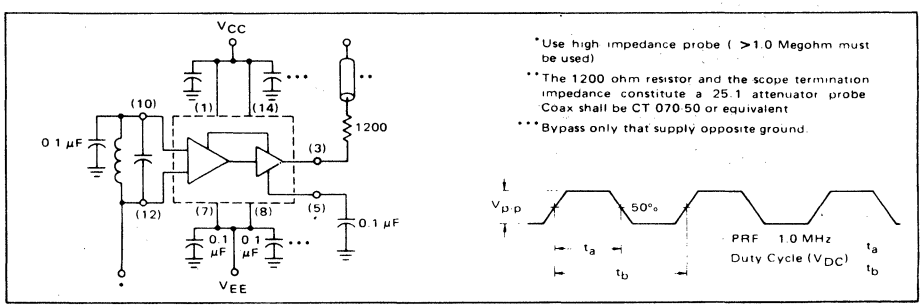


@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
-30°C	-3.300	-3.800	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+85°C	-3.500	-4.000	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	41	—	—	mAdc	—	—	7, 8	—	1, 14
Logic "1" Output Voltage	V_{OH}	3	-1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	—	12	7, 8	3	1, 14
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	7, 8	3	1, 14
Bias Voltage	V_{Bias}*	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	—	—	7, 8	—	1, 14
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak-to-Peak Tank Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	7, 8	3	1, 14
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	7, 8	3	1, 14
Oscillation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	7, 8	3	1, 14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



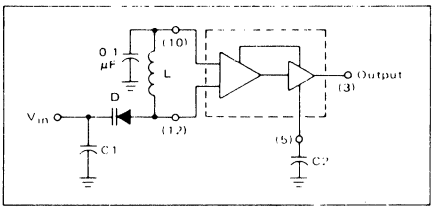
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

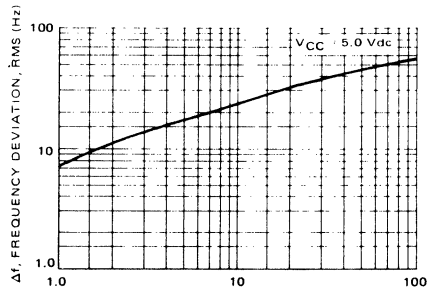
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

FIGURE 4 – THE SP1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



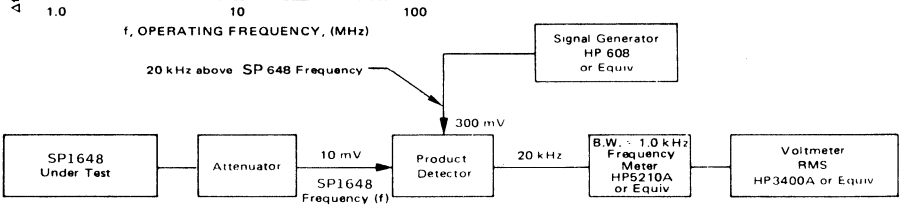
When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



Oscillator Tank Components
(Circuit of Figure 4)

f MHz	D	L μH
1.0 10	MV2115	100
10 60	MV2115	2.3
60-100	MV2106	0.15



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimzed prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE
USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

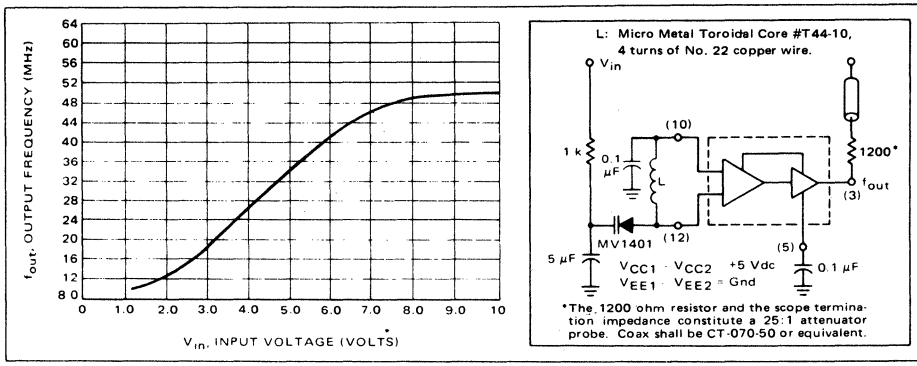


FIGURE 7

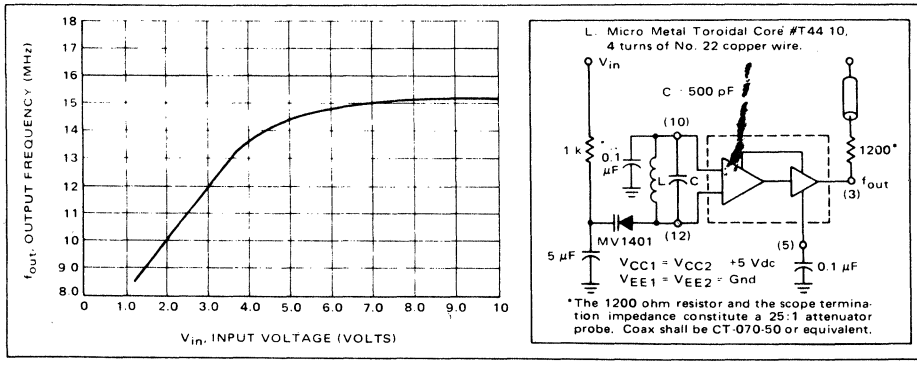
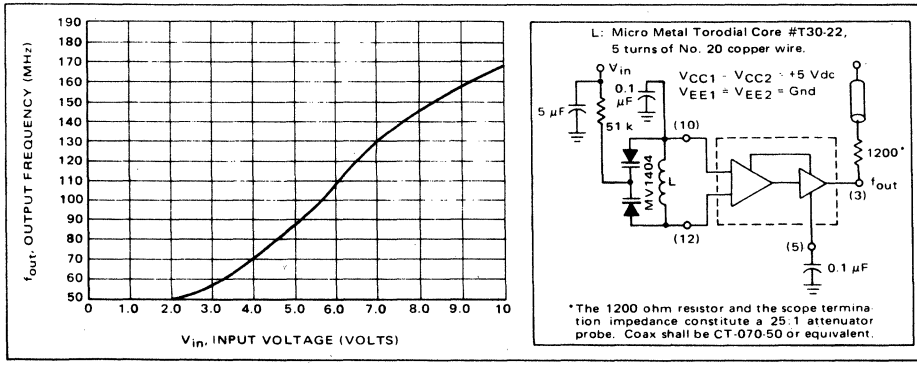


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (pluse the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\ (max) + C_S}}{\sqrt{C_D\ (min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L\ (C_D\ (max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the SP1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

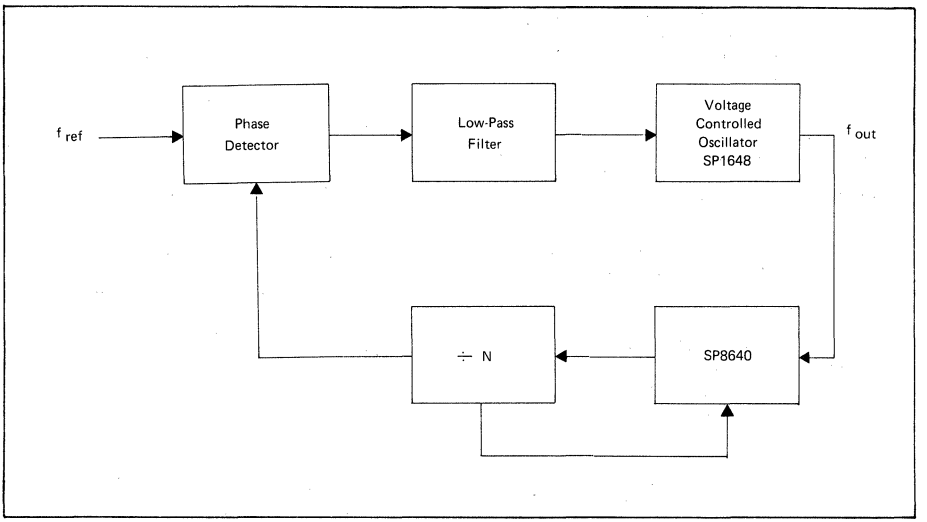


Figure 10 shows the SP1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the SP1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the SP1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the PECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

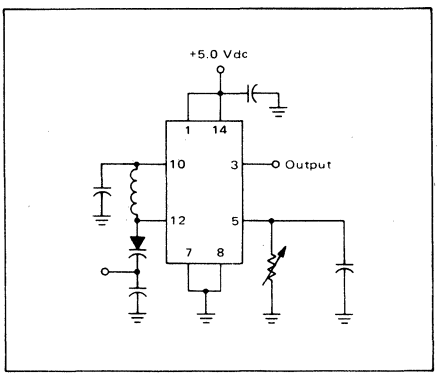


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE SP1648 (SQUARE WAVE OUTPUT)

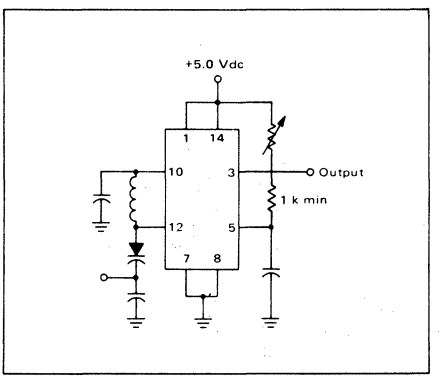


FIGURE 12 – CIRCUIT SCHEMATIC USED FOR COLLECTOR OUTPUT OPERATION

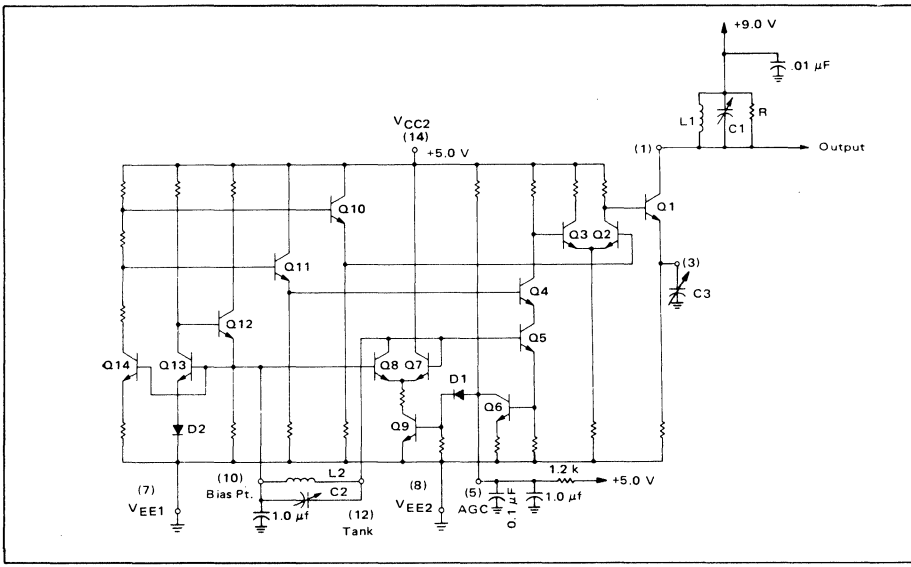


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 100 MHz
C3 = 3.0 - 35 pF
Collector Tank
L1 = 0.22 µH C1 = 1.0 - 7.0 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 11 kΩ @ 100 MHz Resonance
Oscillator Tank
L2 = 4 turns #20 AWG 3/16" ID
C2 = 1.0 - 7.0 pF

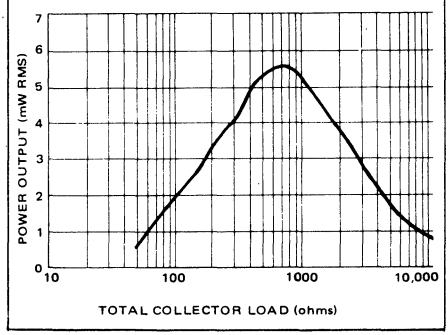
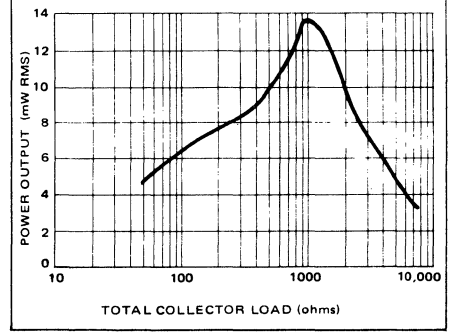


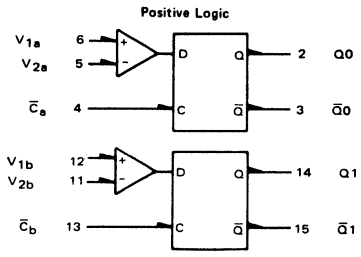
FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD

See test circuit, Figure 12, f = 10 MHz
C3 = 470 pF
Collector Tank
L1 = 2.7 µH C1 = 24 - 200 pF
R = 50 Ω - 10 kΩ
Rp of L1 and C1 = 6.8 kΩ @ 10 MHz Resonance
Oscillator Tank
L2 = 2.7 µH
C2 = 16 - 150 pF



DUAL A/D COMPARATOR

SP1650 • SP1651



V_{CC} = +5.0 V = Pin 7,10
V_{EE} = -5.2 V = Pin 8
Gnd = Pin 1,16

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (**SP1650**)
  = 3.0 ns typ (**SP1651**)
- Input Slew Rate = 350 V/μs (**SP1650**)
  = 500 V/μs (**SP1651**)
- Differential Input Voltage:
  -5.0 V to +5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (**SP1650**)
  -2.5 V to +3.0 V (-30°C to +85°C) (**SP1651**)
- Resolution: ≤20 mV (-30°C to +85°C)
- Drives 50 Ω lines

The **SP1650** and the **SP1651** are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The **SP1650** provides high impedance Darlington inputs, while the **SP-1651** is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from PECL III or PECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

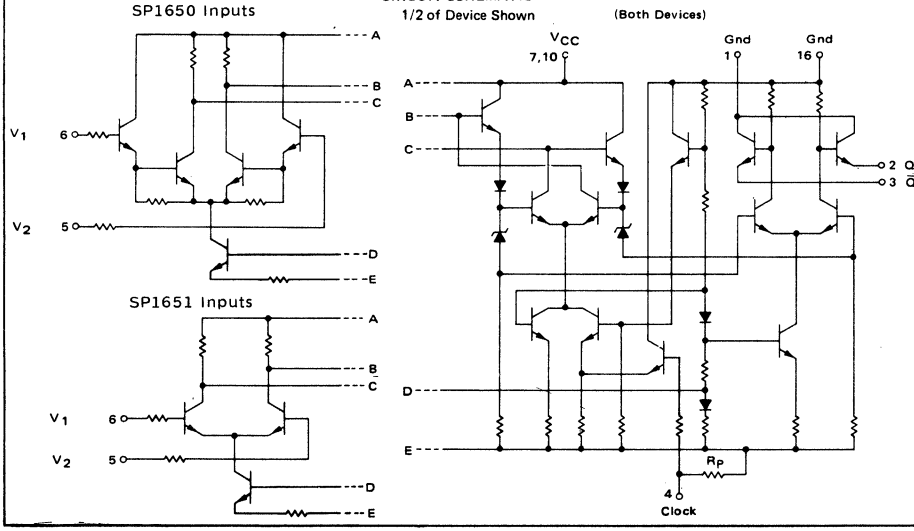
Assessment of the performance differences between the **SP1650** and the **SP1651** may be based upon the relative behaviors shown in Figures 3 and 6.

TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

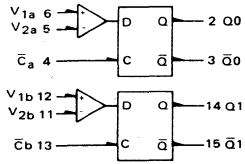
CIRCUIT SCHEMATIC
1/2 of Device Shown (Both Devices)



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

POSITIVE LOGIC



CERAMIC PACKAGE **E**

@ Test Temperature	TEST VOLTAGE VALUES (Volts)											
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020					+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020		See Note ④			+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

Characteristic	Symbol	Pin Under Test	SP1650/SP1651 Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
Power Supply Drain Current																						
Positive	I_{CC}	7,10	–	–	–	25*	–	–	mAdc	–	4,13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Negative	I_E	8	–	–	–	55*	–	–	mAdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
Input Current	I_{in}																					
SP1650		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
SP1651		6	–	–	–	40	–	–	μAdc	4	13	–	–	12	–	6	–	–	–	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
SP1650		6	–	–	–	7	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
SP1651		6	–	–	–	10	–	–	μAdc	4	13	–	–	12	–	–	–	6	–	7,10	8	1,5,11,16
Input Clock Current	I_{inH}	4	–	–	–	350	–	–	μAdc	4	13	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
	I_{inL}	4	–	–	0.5	–	–	–	μAdc	–	13	–	–	6,12	–	–	–	–	–	7,10	4,8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4,13	–	–	–	6,12	–	–	–	–	–	7,10	8	1,5,11,16
		2									–	–	–	–	5,11	–	–	–	–			1,6,12,16
		2									–	–	–	–	–	6,12	5,11	–	–			1,16
		2									–	–	–	–	–	–	–	5,11	6,12			1,16
		3									–	–	–	–	6,12	–	–	–	–			1,5,11,16
		3									–	–	–	5,11	–	–	–	–	–			1,6,12,16
		3									–	–	–	–	–	5,11	6,12	–	–			1,16
		3									–	–	–	–	–	–	–	6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13	–	–	–	–	6,12	–	–	–	–	7,10	8	1,5,11,16
		2									–	–	–	5,11	–	–	–	–	–			1,6,12,16
		2									–	–	–	–	–	5,11	6,12	–	–			1,16
		2									–	–	–	–	–	–	–	6,12	5,11			1,16
		3									–	–	–	6,12	–	–	–	–	–			1,5,11,16
		3									–	–	–	–	5,11	–	–	–	–			1,6,12,16
		3									–	–	–	–	–	6,12	5,11	–	–			1,16
		3									–	–	–	–	–	–	–	5,11	6,12			1,16
Logic "1" Threshold Voltage ②	V_{OHA}	1	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		2		–		–		–		–	–	–	4	–	6	–	–	–	–			
		3		–		–		–	*	–		4	–	6	–	–	–	–	–			
		4		–		–		–		–	–	–	4	6	–	–	–	–	–			
Logic "0" Threshold Voltage ②	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	4	–	6	–	–	–	–	–	7,10	8	1,5,16
		3	–		–		–			–	–	–	4	–	6	–	–	–	–			
		2	–		–		–			–		4	–	6	–	–	–	–	–			
		2	–		–		–			–	–	–	4	6	–	–	–	–	–			

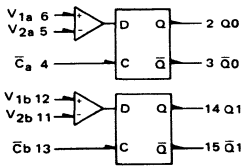
NOTES: ① All data is for a SP1650 or SP1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired)
$|V_{EE}| + |V_{CC}| \leq 12$ Vdc.

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
SP1650	+3.000	+2.980	-2.500	-2.480
SP1651	+2.500	+2.480	-3.000	-2.980

SWITCHING TIMES

POSITIVE LOGIC



CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

Characteristic	Symbol	Pin Under Test	SP1650/1651 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	P1	P2	P3	P4
Switching Times Propagation Delay (50% to 50%) V-Input to Output	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{6+2-}	2								–	5	–					–	6	–	–
	t_{6+3+}	2								–	–	5					–	–	6	–
	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6-2+}	3								–	5	–					–	6	–	–
	t_{6-2-}	3								–	–	5					–	–	6	–
	t_{6-3+}	2								5	–	–					6	–	–	–
	t_{6-3-}	2								–	5	–					–	6	–	–
		2								–	–	5					–	–	6	–
		3								5	–	–					6	–	–	–
		3								–	5	–					–	6	–	–
		3								–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2								6	–	–	–				5	–	–	
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time (10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time (10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

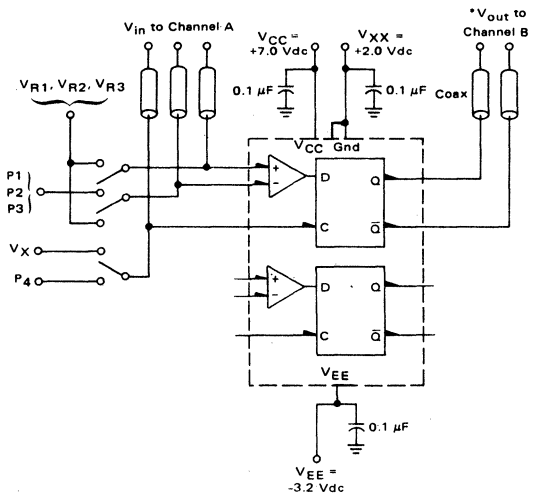
See Figure 2

NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired:
$|V_{CC}| + |V_{EE}| \leq 12$ Vdc.
② Unused clock inputs may be tied to ground.
③ See Figure 8.

④

All Temperatures	V_{R2}	V_{R3}
SP1650	+4.900	-0.400
SP1651	+4.400	-0.900

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



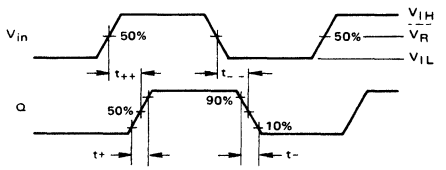
50-ohm termination to ground located in each scope channel input
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

*Complement of output under test should always be loaded with 50-ohms to ground.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

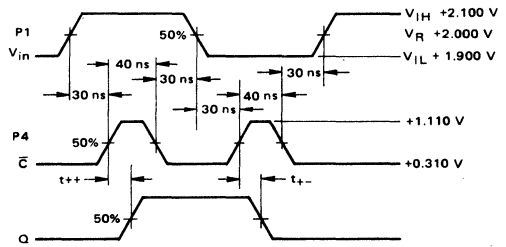


Test pulses: $t_+, t_- = 1.5 \pm 0.2$ ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\overline{C}$ during tests.

TEST PULSE LEVELS

	Pulse 1		Pulse 2		Pulse 3	
	SP1650	SP1651	SP1650	SP1651	SP1650	SP1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

Clock to Output



P4: $t_+, t_- = 1.5 \pm 0.2$ ns.

FIGURE 3 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE

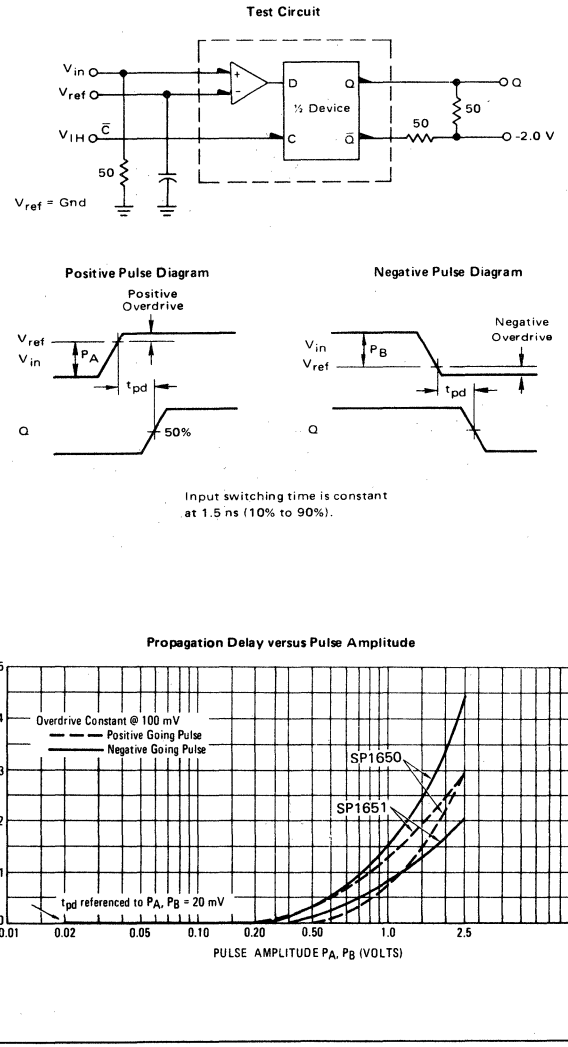


FIGURE 3 (continued)

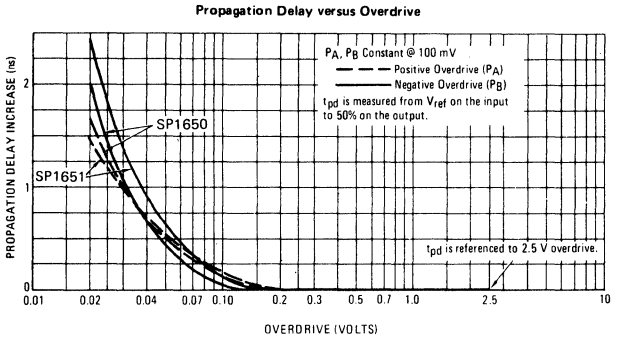
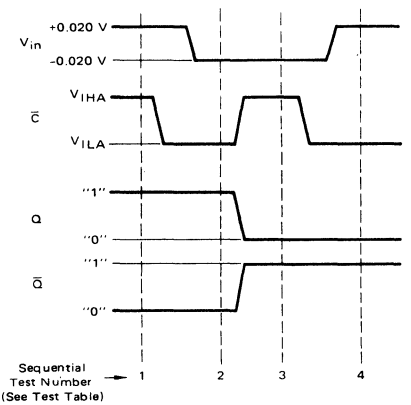
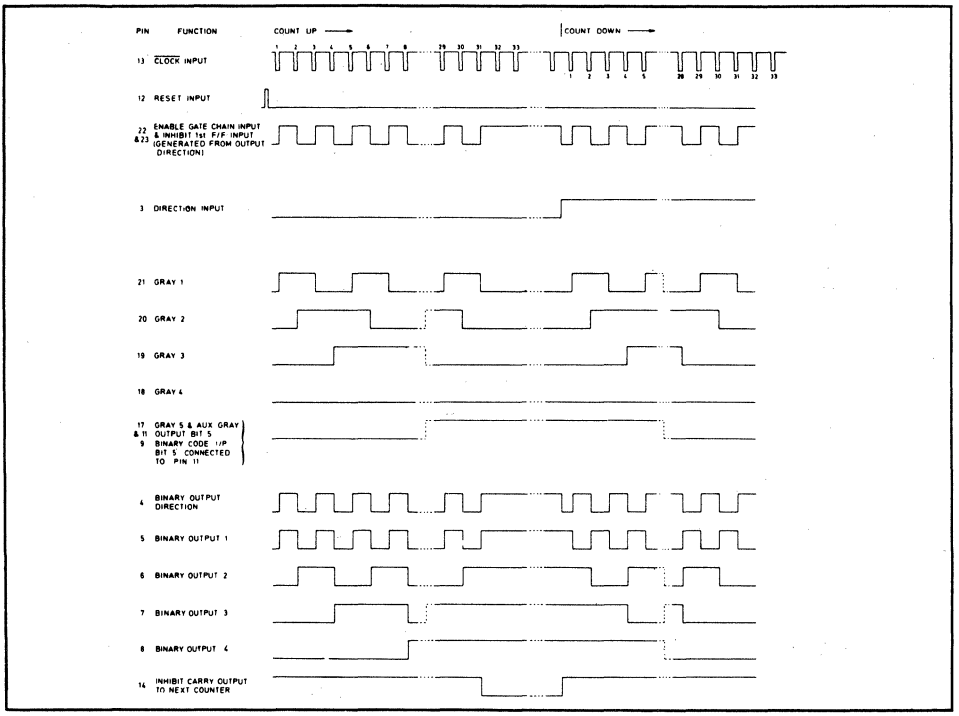


FIGURE 4 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)



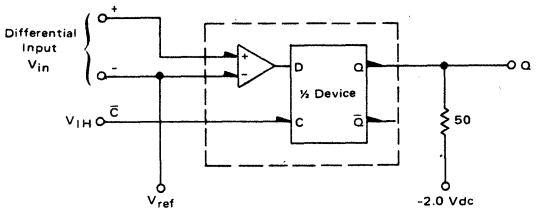


The enable gate chain output is normally in the '0' state and goes to the '1' state only when all the Gray outputs are low and the enable input high.

Fig.4 Logic states for 5-bit counter

FIGURE 5 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



$-2.5\ Vdc \leqslant V_{ref} \leqslant +2.5\ Vdc$

Typical Transfer Curves

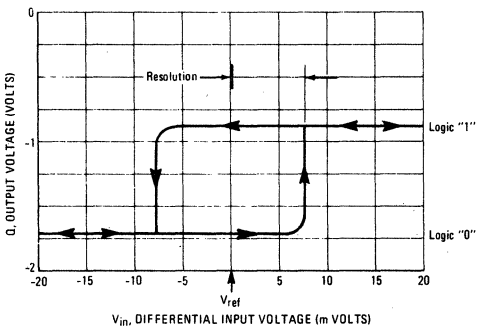
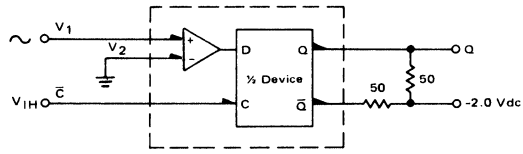
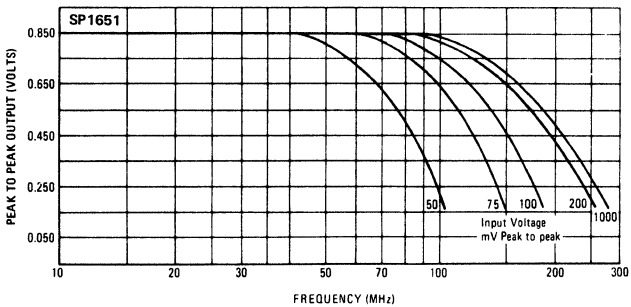


FIGURE 6 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



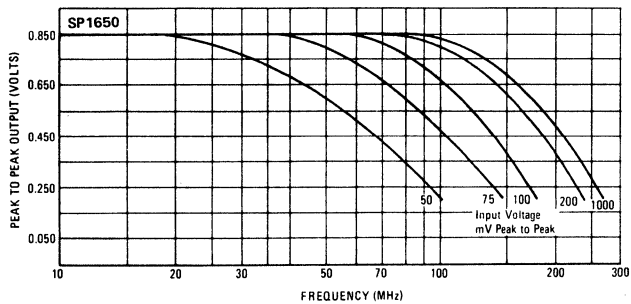
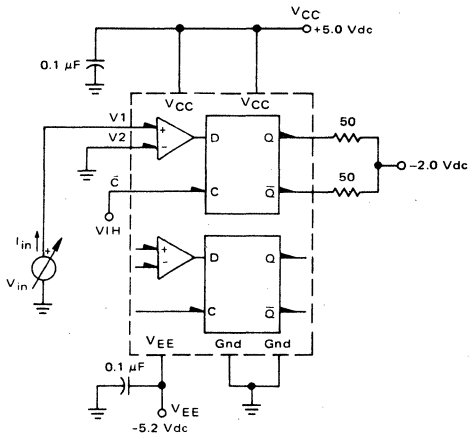
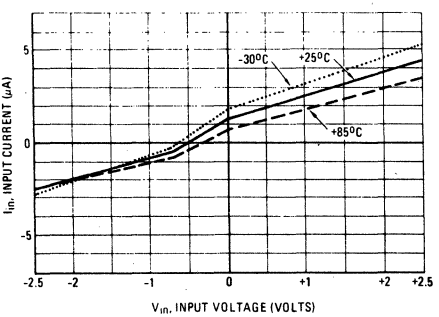


FIGURE 7 – INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT



Typical SP1650 (Complementary Input Grounded)



Typical SP1651 (Complementary Input Grounded)

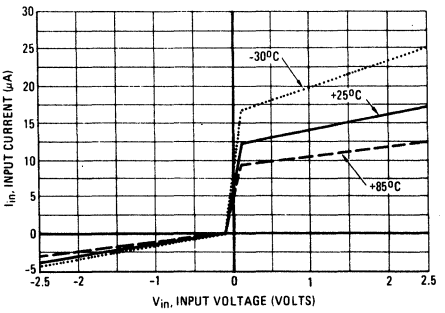
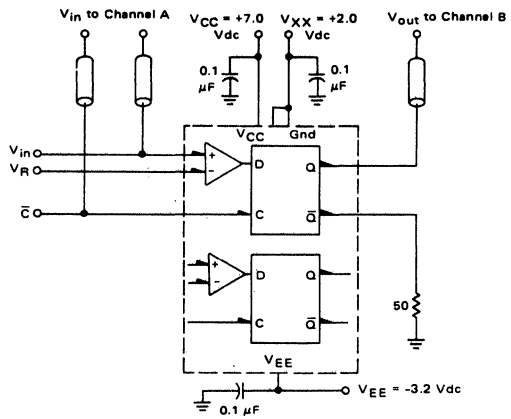


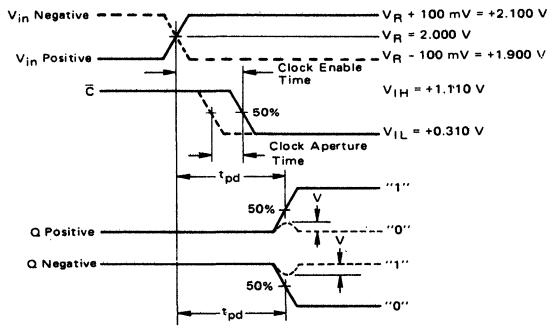
FIGURE 8 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case

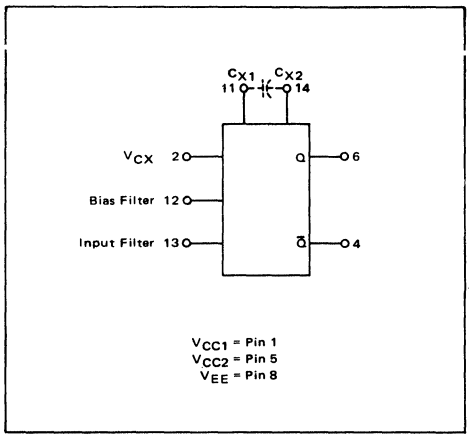


——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

VOLTAGE-CONTROLLED MULTIVIBRATOR

SP1658

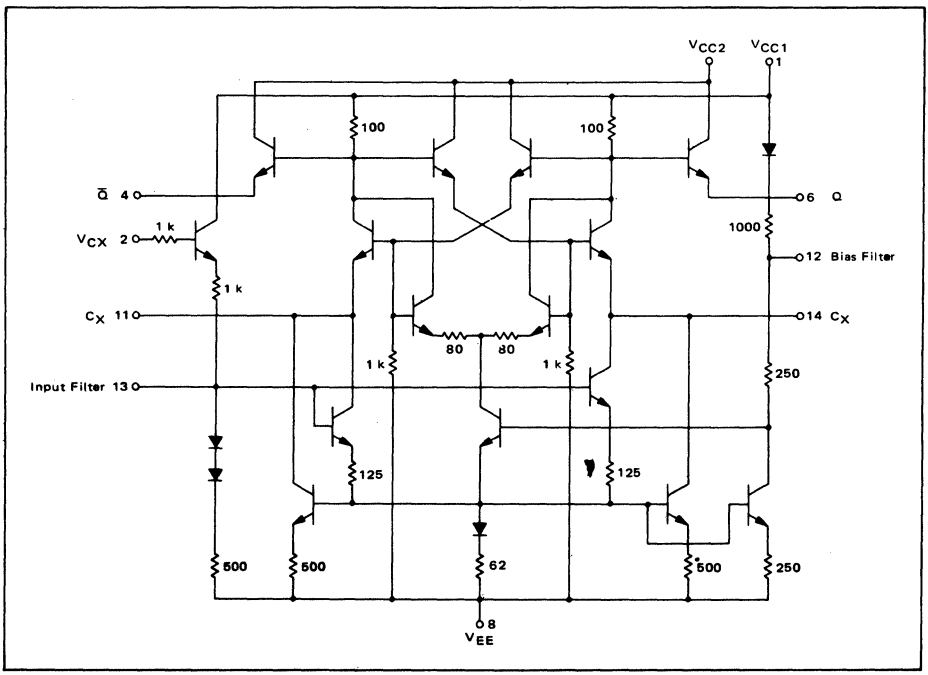


The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with RECL III and RECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

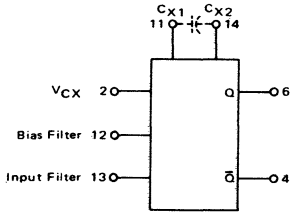
FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

CERAMIC PACKAGE E



@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1% V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}
-30°C	0.0	-2.0	-1.0	+2.0	-5.2
+25°C	0.0	-2.0	-1.0	+2.0	-5.2
+85°C	0.0	-2.0	-1.0	+2.0	-5.2

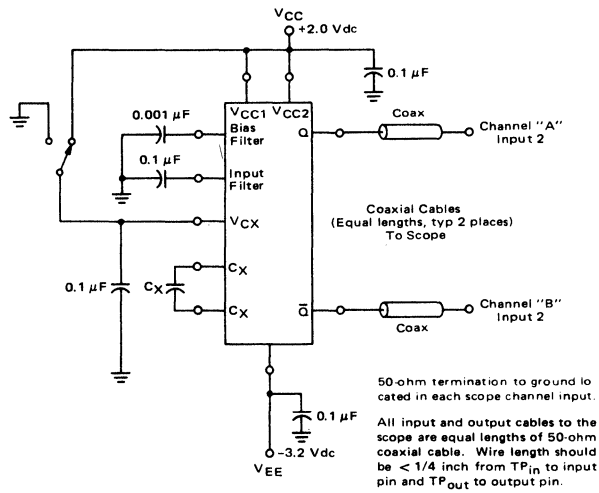
Characteristic	Symbol	Pin Under Test	SP1658 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8*	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
		8**	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
Input Current	I_{inH}	2*	–	–	–	–	350	–	–	μAdc	2	–	–	–	8	1,5
Input Leakage Current	I_{inL}	2*	–	–	0.5	–	–	–	–	μAdc	–	2	–	–	8	1,5
"Q" High Output Voltage	V_{OH}	4*	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
		6**	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
"$\overline{Q}$" Low Output Voltage	V_{OL}	4*	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
		6**	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
AC Characteristics (Figure 2) (Tests shown for one output, but checked on both)											C_{X1}	C_{X2}	Gnd		V_{EE} -3.2 V	V_{CC} +2.0 V
Rise Time (10% to 90%)	t_+	6	–	2.7	–	1.6	2.7	–	3.0	ns	–	11,14	–	2	8	1,5
Fall Time (10% to 90%)	t_-	6	–	2.7	–	1.4	2.7	–	3.0	ns	–	11,14	–	2	8	1,5
Oscillator Frequency	f_{osc1}	–	130	–	130	155	175	110	–	MHz	–	11,14	–		8	1,5
	f_{osc2}	–	–	–	78	90	100	–	–	MHz	11,14	–	–		8	1,5
Tuning Ratio Test †	TR	–	–	–	3.1	4.5	--	–	–	–	11,14	–	–		8	1,5

*Germanium diode (0.4 drop) forward biased from 11 to 14 (11 —▶|— 14).
**Germanium diode (0.4 drop) forward biased from 14 to 11 (11 —|◀— 14).

†$TR = \frac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\text{ V}}$

C1 = 0.01 μF connected from pin 12 to Gnd.
C2 = 0.001 μF connected from pin 13 to Gnd.
C_{X1} = 10 pF connected from pin 11 to pin 14.
C_{X2} = 5 pF connected from pin 11 to pin 14.

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



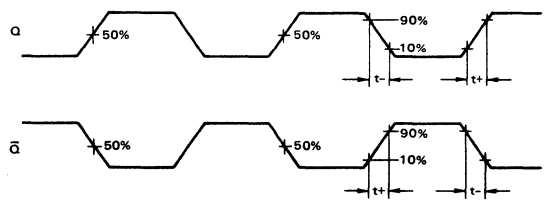


FIGURE 3 – OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

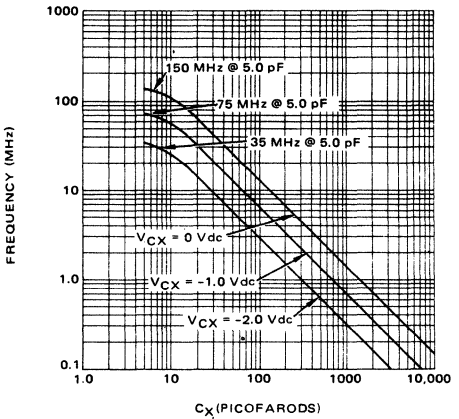


FIGURE 4 – RMS NOISE DEVIATION versus OPERATING FREQUENCY

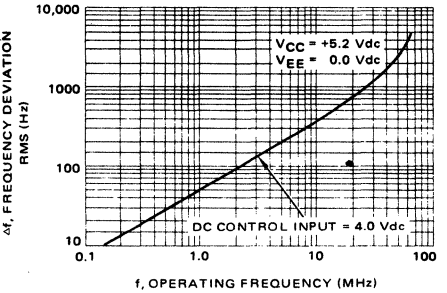
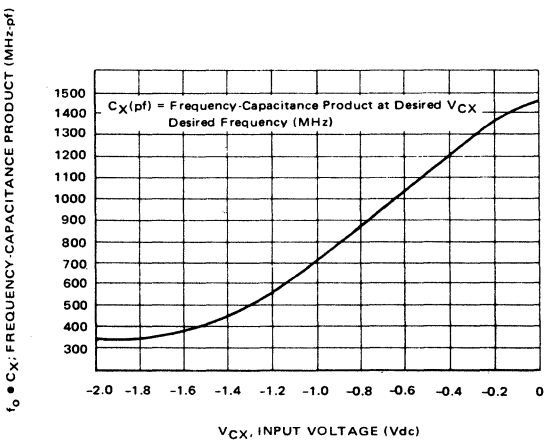


FIGURE 5 – FREQUENCY-CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})

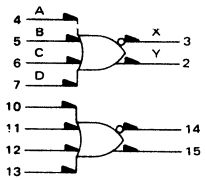


DUAL 4-INPUT GATE

SP1660

SP1660 provides simultaneous OR-NOR or AND-NAND output functions with the capability of driving 50-ohm lines. These devices contain an internal bias reference voltage insuring that the threshold point is always in the center of the transition region over the temperature range (-30° to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}

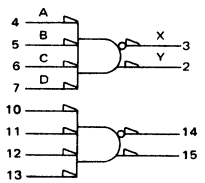
POSITIVE LOGIC



$X = \overline{A + B + C + D}$

$Y = A + B + C + D$

NEGATIVE LOGIC

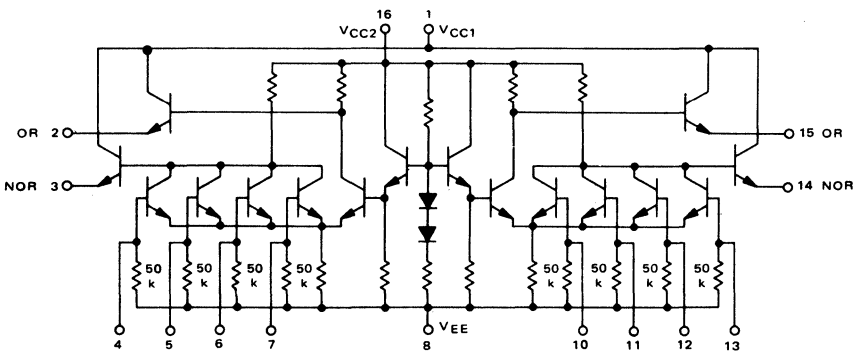


$X = \overline{A \bullet B \bullet C \bullet D}$

$Y = A \bullet B \bullet C \bullet D$

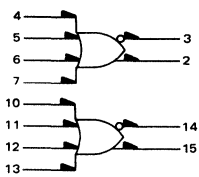
t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (LIC21 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1660 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
NOR Logic "1" Output Voltage	$V_{OH}\phi$	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "0" Output Voltage	$V_{OL}\phi$	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "1" Output Voltage	$V_{OH}\phi$	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic "0" Output Voltage	$V_{OL}\phi$	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic "1" Threshold Voltage	$V_{OHA}\phi$	3	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic "0" Threshold Voltage	$V_{OLA}\phi$	3	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic "1" Threshold Voltage	$V_{OHA}\phi$	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic "0" Threshold Voltage	$V_{OLA}\phi$	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	1.8	–	1.7	–	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9			2	–	–		
	t_{4+2+}	2	–	1.6	–	1.5	–	1.7			2	–	–		
	t_{4-3+}	3	–	1.6	–	1.5	–	1.7			3	–	–		
Rise Time	t_{3+}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to the input under test.

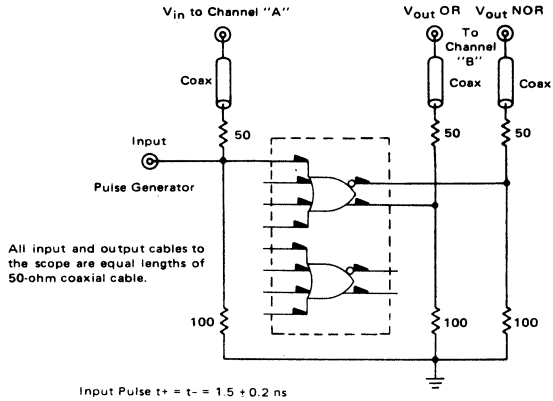
φ NOTES

The electrical specifications shown above apply to the SP1660 under the following conditions:

1. The package is housed in a suitable heat sink.†
   or
2. Air is blown transversely over the package. See general information section for more details.

†A suitable heat sink is an IERC LIC214A2WCB or equivalent.

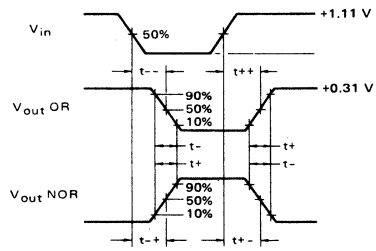
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse t+ = t- = 1.5 +0.2 ns

Unused outputs connected to a 50-ohm resistor to ground

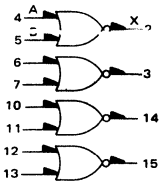
PROPAGATION DELAY



QUAD 2-INPUT "NOR" GATE

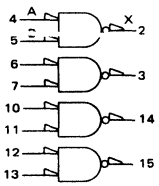
SP1662

POSITIVE LOGIC



$X = \overline{A + B}$

NEGATIVE LOGIC



$X = \overline{A \bullet B}$

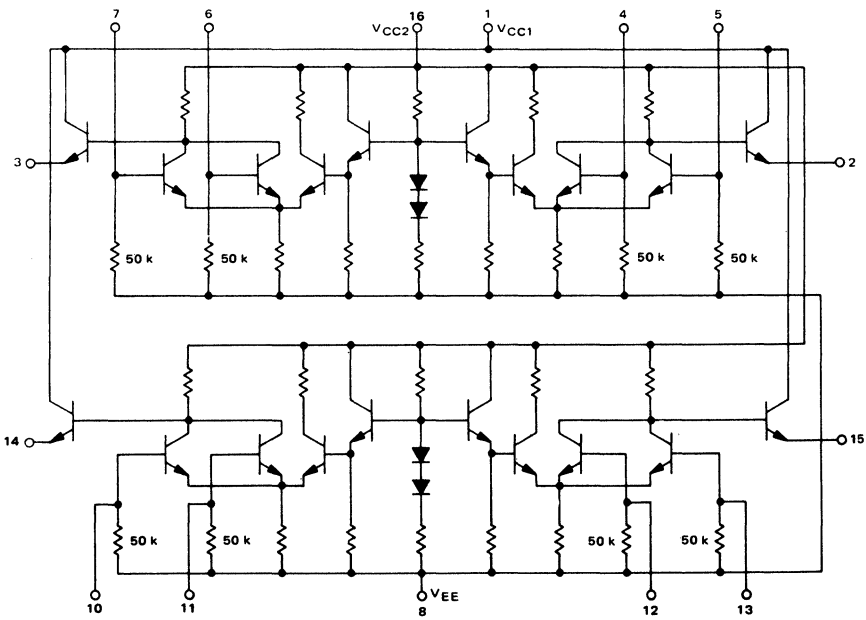
Four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (-30 to +85°C).

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

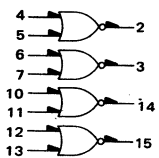
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

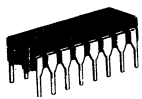
CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink(IERC-21 4 A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





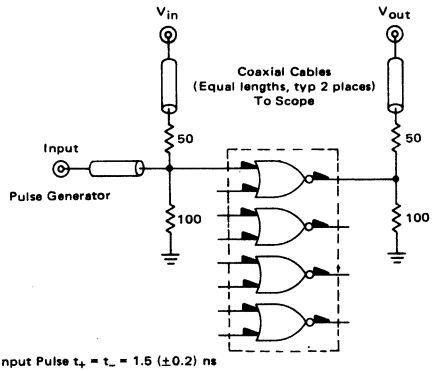
CERAMIC PACKAGE E

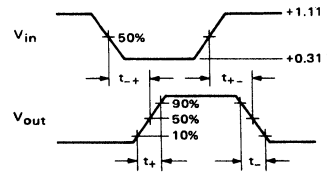
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1662 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\,H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\,L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	1.0	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	1.1	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	1.4	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	1.2	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





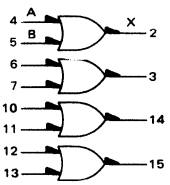
Input Pulse $t_+ = t_- = 1.5$ (±0.2) ns

Unused outputs connected to a 50-ohm resistor to ground.

QUAD 2-INPUT "OR" GATE

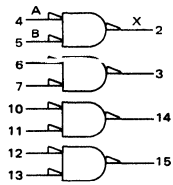
SP1664

POSITIVE LOGIC



X = A + B

NEGATIVE LOGIC



X = A • B

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

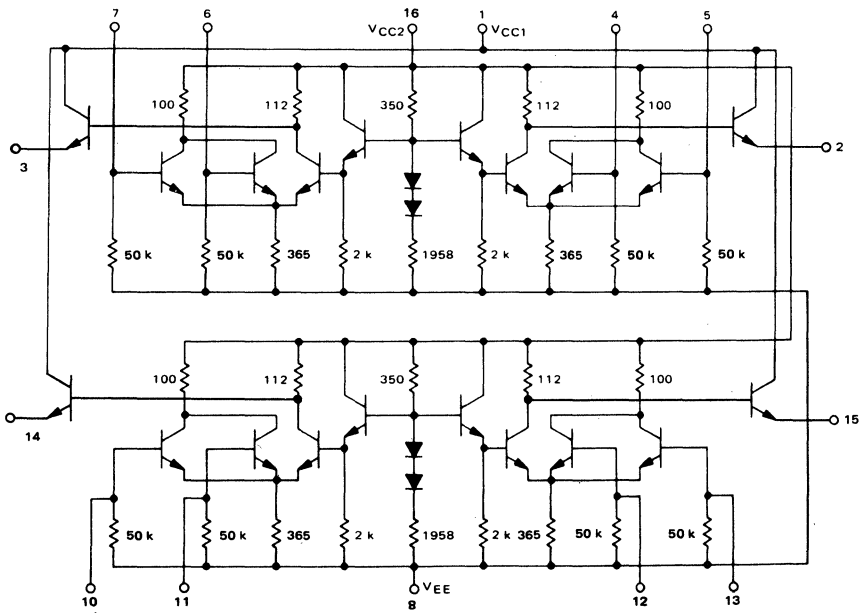
Four 2-input OR or AND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range -30 to +85°C.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

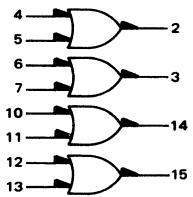
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

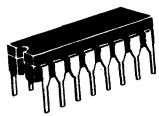
CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink(IERC-21 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





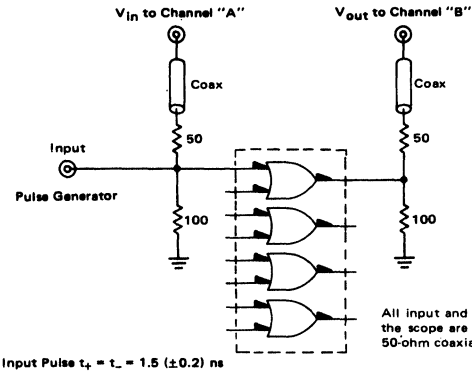
CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

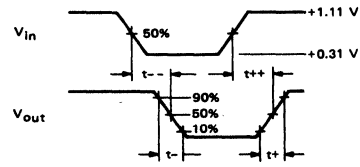
Characteristic	Symbol	Pin Under Test	SP1664 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\,H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\,L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	5	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	–	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.



Input Pulse $t_+ = t_- = 1.5$ (±0.2) ns

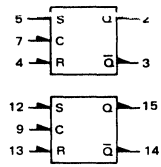
Unused outputs connected to a 50-ohm resistor to ground.

DUAL CLOCKED R-S FLIP-FLOP

SP1666

This device consists of two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage. The device is useful as a high-speed dual storage element.

POSITIVE LOGIC



t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

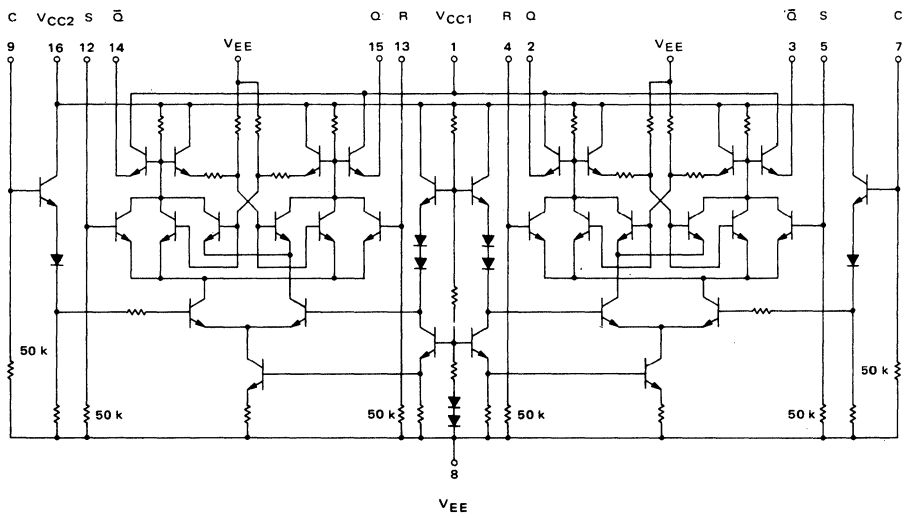
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care
N.D. = Not Defined

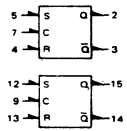
CIRCUIT SCHEMATIC

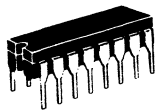


Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 21 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





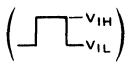
CERAMIC PACKAGE E

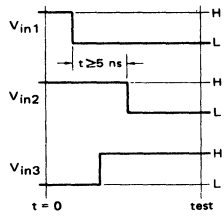
@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1666 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85 Min	+85 Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E ①	8	–	–	–	55	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	–	–	0.370	–	–	mAdc	9,12	–	–	–	8	1,16
		13	–	–	–	0.370	–	–	mAdc	9,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	I_{inL}	12	–	–	0.500	–	–	–	µAdc	–	12	–	–	8	1,16
		9,13	–	–	0.500	–	–	–	µAdc	–	9,13	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	13	–	–	8	1,16
		15 ③	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q" Logic "0" Output Voltage	V_{OL}	15 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "1" Output Voltage	V_{OH}	14 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"$\bar{Q}$" Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	9	–	8	1,16
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15 ⑤	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
"$\bar{Q}$" Logic "1" Output Threshold Voltage	V_{OHA}	14 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
"$\bar{Q}$" Logic "0" Output Threshold Voltage	V_{OLA}	14 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	9	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
[redacted]	t_{9+15-}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9-15+}	15	↓	↓	↓	↓	↓	↓	↓	↓	15	–	–	↓	↓
	t_{9-14+}	14									14	–	–		
	t_{9+14-}	14									14	–	–		
Set Input	t_{12+15+}	15	1.0	2.5	1.0	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	↓	↓	↓	↓	↓	↓	ns	12	14	–	–	8	1,16
Reset Input	t_{13-14-}	14							ns	13	14	–	–	8	1,16
	t_{13-15+}	15							ns	13	15	–	–	8	1,16
Rise Time	t_+	14,15	0.8	2.8	0.8	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–	–	8	1,16

○ Notes appear on page following Electrical Characteristics tables.

NOTES





① I_E is measured with no output pull-down resistors.

② Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

③ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

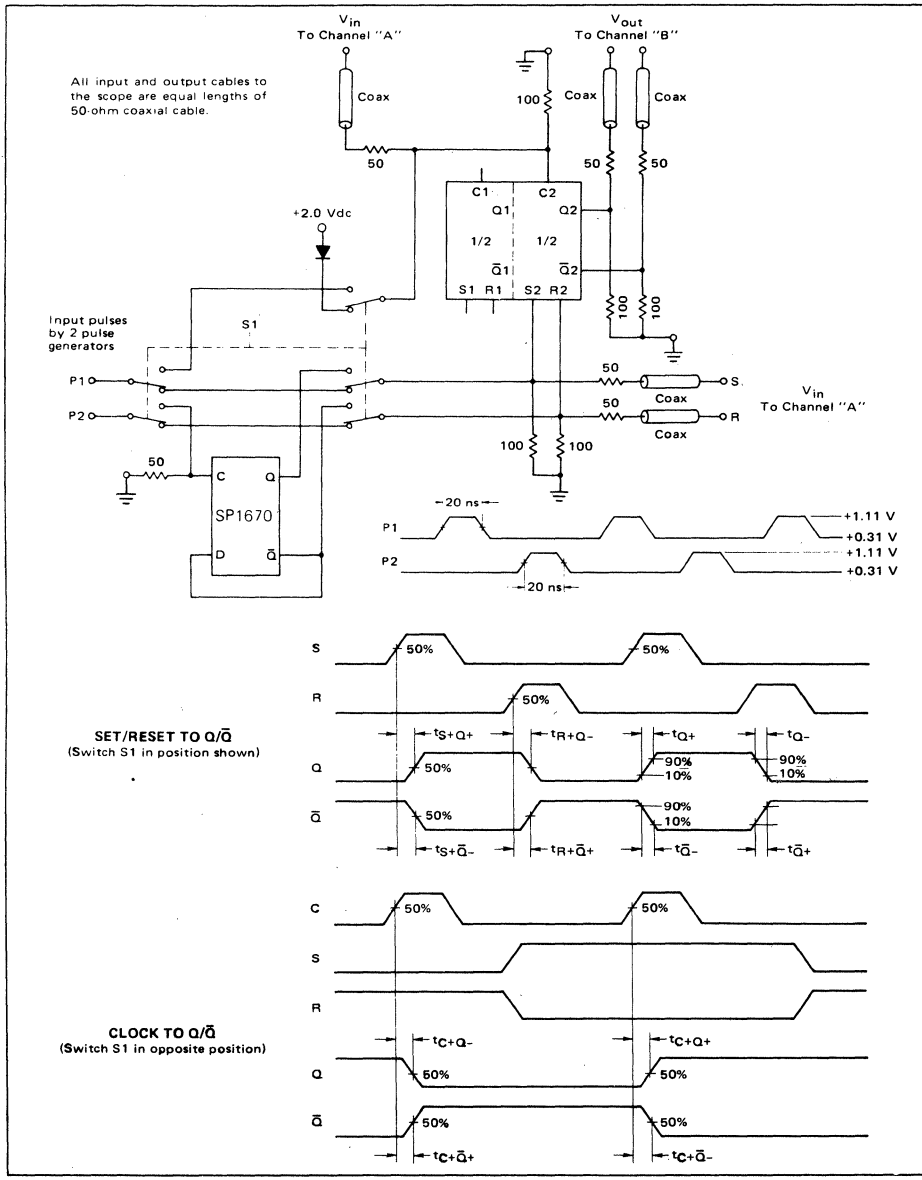
④ Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑤ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑥ Apply V_{in3} to C (V_{IH} to V_{IL})

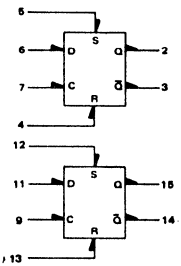
⑦ Apply V_{in3} to S (V_{IH} to V_{IL})

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



SP1668

POSITIVE LOGIC



This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.

TRUTH TABLE

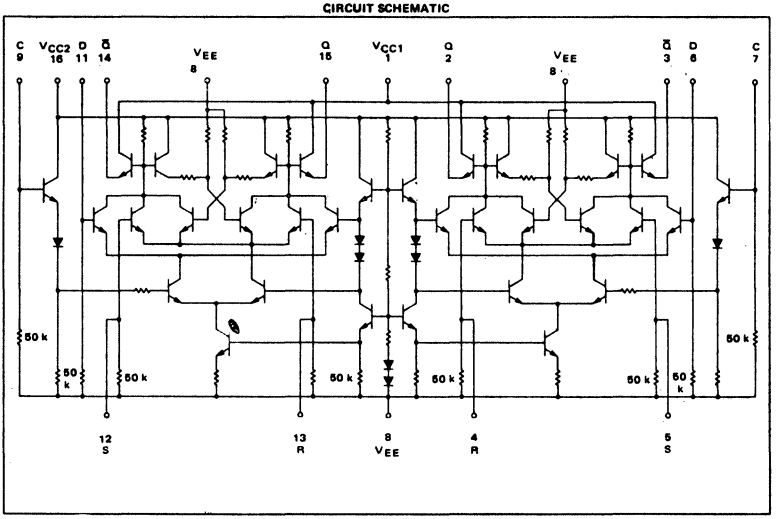
S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

**Output state not defined ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

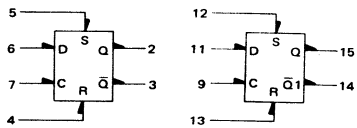
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



CERAMIC PACKAGE E

@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

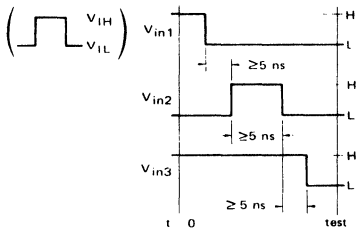
Characteristic	Symbol	Pin Under Test	SP1668 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E (Hi-Z)	8				55			mAdc	7,9				8	1,16
Input Current	I_{in} H	11,12,13②				0.370			mAdc	11,12,13				8	1,16
		9				0.225			mAdc	9				8	1,16
	I_{in} L	11,12,13②			0.500				μAdc		11,12,13			8	1,16
		9			0.500				μAdc		9			8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15③	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc		13			8	1,16
		15④	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	9				8	1,16
"Q" Logic "0" Output Logic	V_{OL}	15⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc		12			8	1,16
		15⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9				8	1,16
"Q̄" Logic "1" Output Voltage	V_{OH}	14⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc		12			8	1,16
		14⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9				8	1,16
"Q̄" Logic "0" Output Voltage	V_{OL}	14③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc		13			8	1,16
		14④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9				8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15	-1.065		-0.980		-0.910		Vdc			12	13	8	1,16
		15⑦										11			
		15⑤								11		9			
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15		-1.630		-1.600		-1.555	Vdc			13	12	8	1,16
		15⑥											11		
		15③									11	9			
"Q̄" Logic "1" Output Threshold Voltage	V_{OLA}	14	-1.065		-0.980		-0.910		Vdc			13	12	8	1,16
		14⑥											11		
		14③									11	9			
"Q̄" Logic "0" Output Threshold Voltage	V_{OLA}	14		-1.630		-1.600		-1.555	Vdc			12	13	8	1,16
		14⑦										11			
		14⑤										9			
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{g+15+}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15			8	1,16
	t_{g+15-}	15									15				
	t_{g+14-}	14									14				
	t_{g+14+}	14									14				
Rise Time	t_+	14,15	0.8	2.8	0.9	2.5	0.9	2.9	ns	9	14,15			8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15			8	1,16
Set Input	t_{12+15+}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	15			8	1,16
	t_{12+14-}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	14			8	1,16
Reset Input	t_{13+14+}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	14			8	1,16
	t_{13+15-}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	15			8	1,16

○Notes appear on page following Electrical Characteristics tables.

NOTES

① I_E is measured with no output pulldown resistors.

② Test voltage applied to pin under test.



③ Apply V_{in1} to S (V_{IH} to V_{IL}).

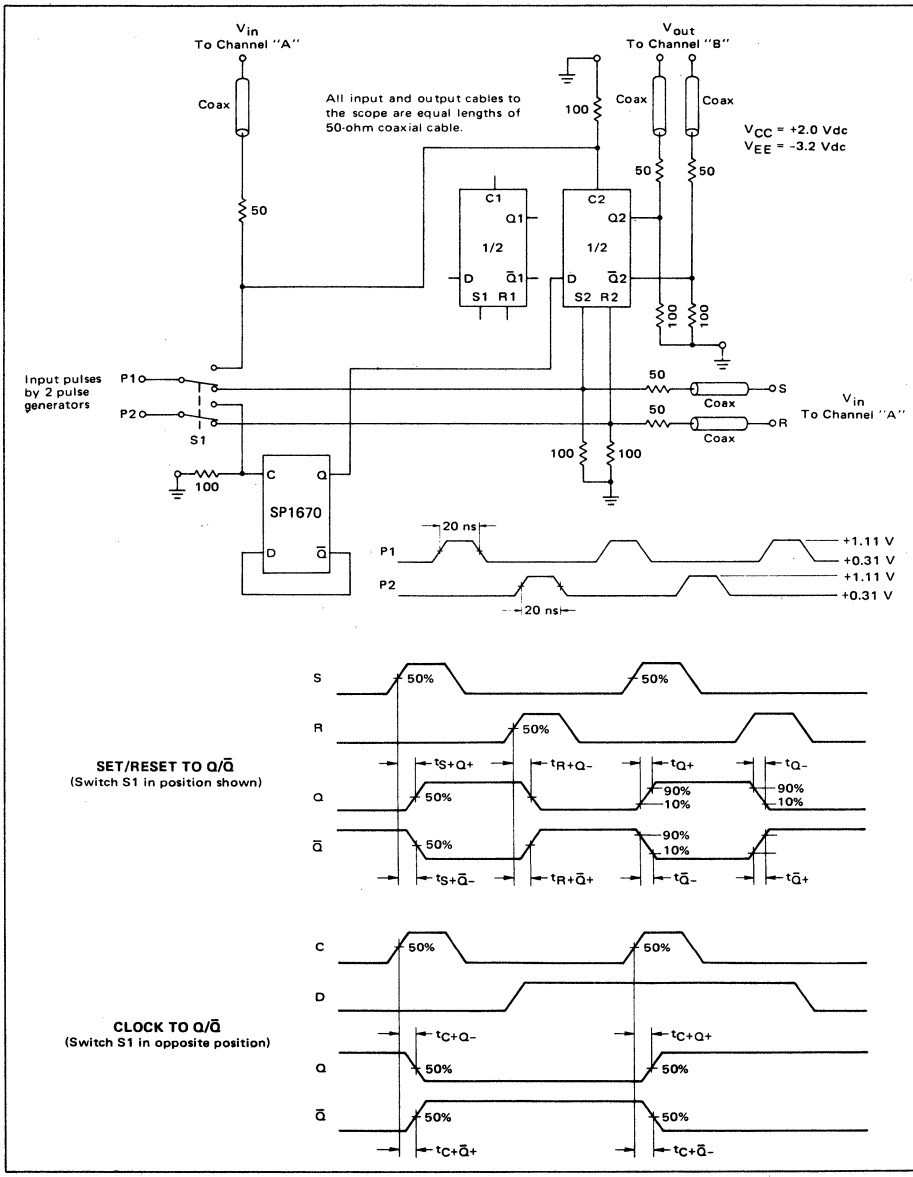
④ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})
V_{in3} to D (V_{IH} to V_{IL})

⑤ Apply V_{in1} to R (V_{IH} to V_{IL})

⑥ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

⑦ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS @ 25°C



MASTER-SLAVE
TYPE D FLIP-FLOP

SP1670

The SP1670 is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

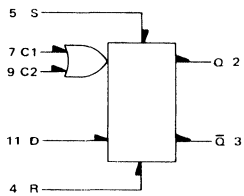
When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

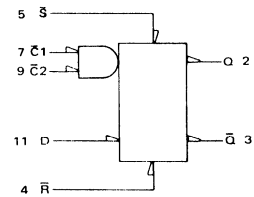
Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

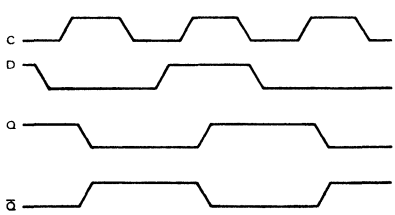
Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↗	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↗	H
L	L	H	H	Q_n

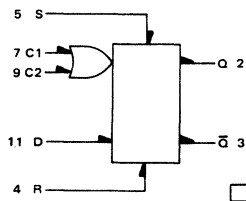
ϕ = Don't Care
ND = Not Defined
C = C1 + C2

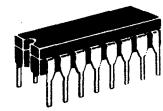
TIMING DIAGRAM



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-*214A2WC8 or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.005	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP 1670 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48	–	–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–			7	–				–	–		
		11				270				11								
	$I_{in\ L}$	4	–		0.5	–	–		μAdc	9	4			8			–	1,16
		5	–	–				–		9	5				–	–	–	
		9	–	–		–	–	–		7	9				–	–		
		7	–	–		–	–	–		9	7		–		–			
		11	–	–		–	–	–		9	11	–	–			–	–	
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4		
		2								11	5,7	–	–		4	9		
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5		
		2								–	4,7,11	–	–		5	9		
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–			7	–	4	
		2		–		–		–		11	5,7	–			4	–	9	
		3		–		–		–		–	4,9,11	–			5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	11	5,7	–	–	8	9	–	4	1,16
		3								–	4,9,11				7	–	5	
		2								–	4,7,11				5	–	9	
		3								11	5,9	–			4	–	7	
		2								–	4,7		11		5	9	–	
		3								–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t_{7+2+}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–		–	–	8		–	–	1,16
(See Figure 1)	t_{7-2-}	9,2								–		–			–		–	
	t_{7+3-}	9,3								–	–	–				–		
	t_{7-3+}	9,3								–	–	–	–		–			
Set to Output Delay	t_{5+2+}	5,2								–		–			–			
(See Figure 2)	t_{5+3-}	5,3								–	–		–		–		–	
Reset to Output Delay	t_{4+2-}	4,2								–	–	–				–	–	
(See Figure 2)	t_{4+3+}	4,3								–	–	–	–		–	–	–	
Output Rise Time	$t_{2+.t3+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–		–	–		–	–	–	
Fall Time	$t_{2-.t3-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–		–	
(See Figure 2)																		
Set Up Time	t_{S}"1"	2		–	–	0.4	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_{S}"0"	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Hold Time	t_{H}"1"	2	–	–	–	0.3	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_{H}"0"	2	–	–	–	0.5	–	–		–	6	–	–		–	–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	2	270		300	–	270	–	MHz	–	–	–	–		–	–	–	–

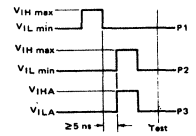


FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT

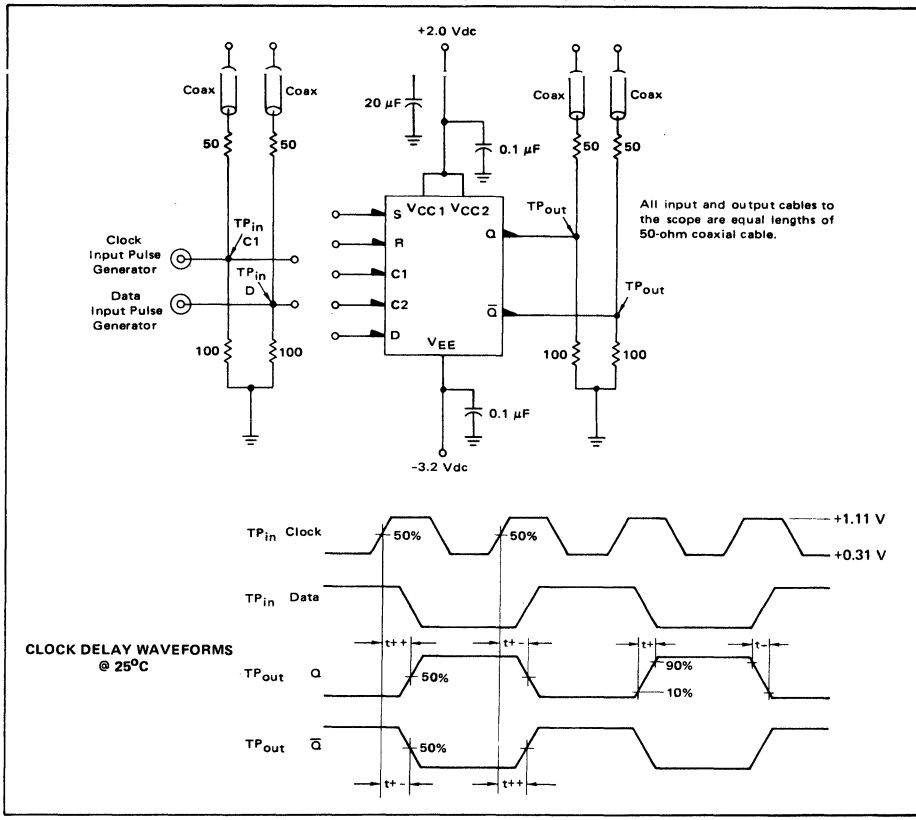


FIGURE 2 – SET-RESET DELAY WAVEFORMS @ 25°C

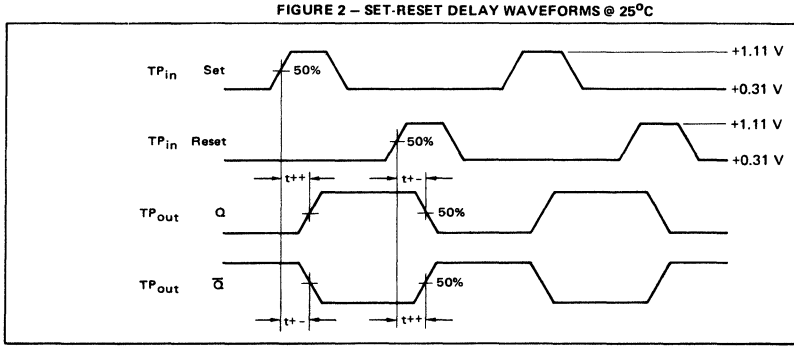
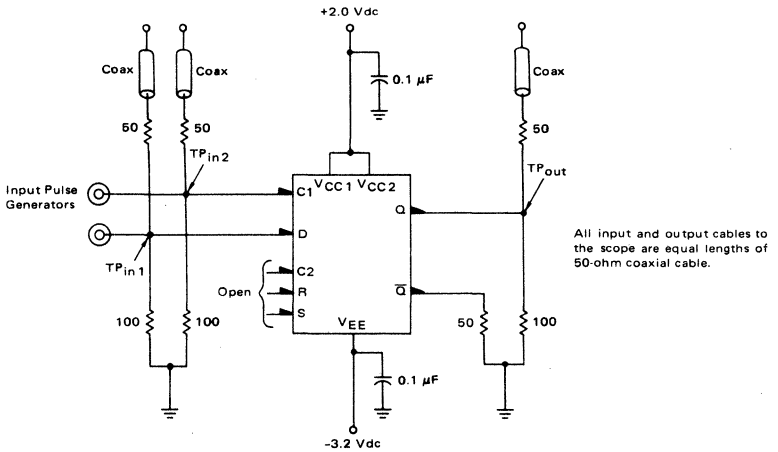
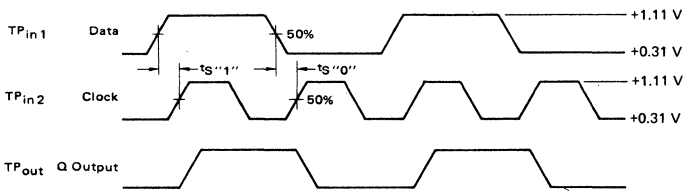


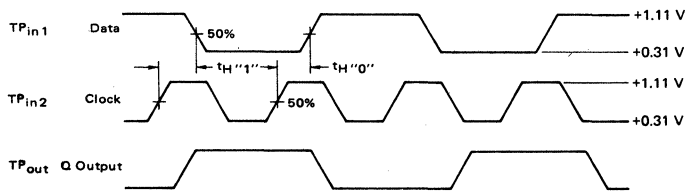
FIGURE 3 – SET UP AND HOLD TIME TEST CIRCUIT



SET UP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 4 – TOGGLE FREQUENCY TEST CIRCUIT

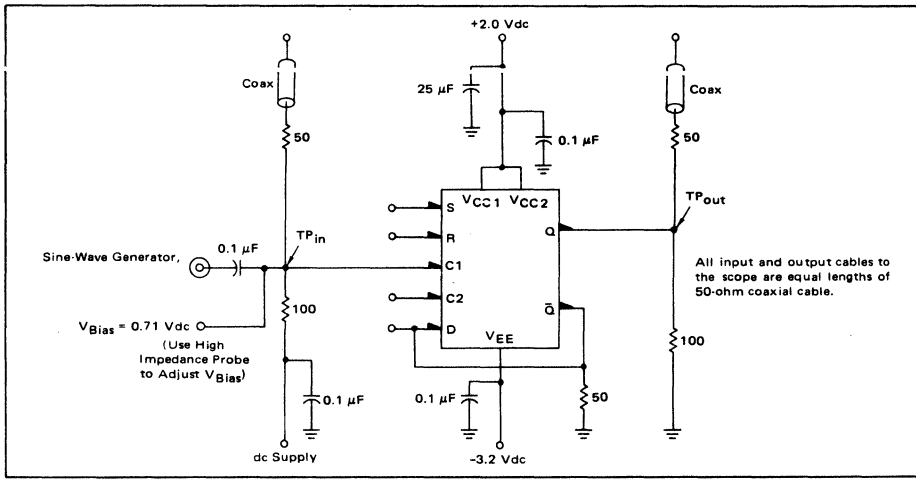


FIGURE 5 – TOGGLE FREQUENCY WAVEFORMS

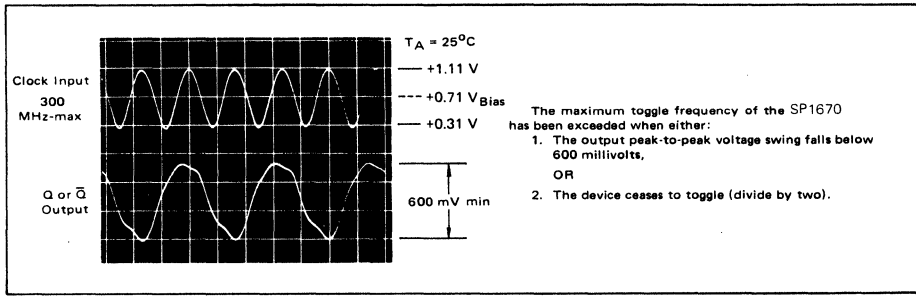


FIGURE 6 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

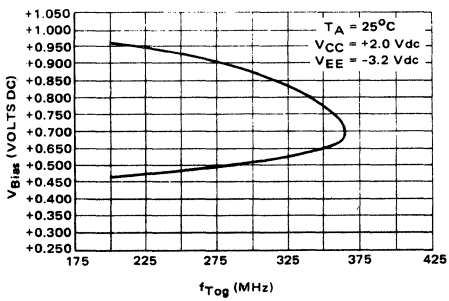
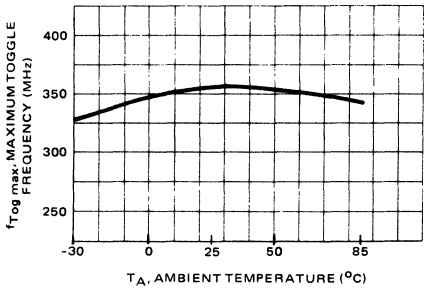


Figure 6 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal. V_{Bias} is defined by the test circuit in Figure 4, and waveform Figure 5.

Figures 8 and 9 illustrate minimum clock pulse width recommended for reliable operation of the SP1670.

FIGURE 7 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

FIGURE 8 – MINIMUM "DOWN TIME" TO CLOCK
OUTPUT LOAD = 50 Ω

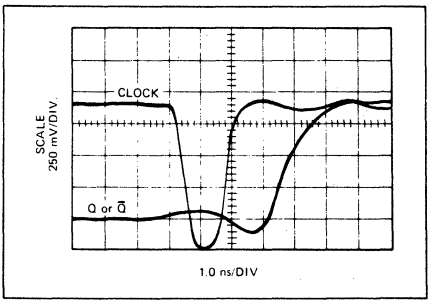
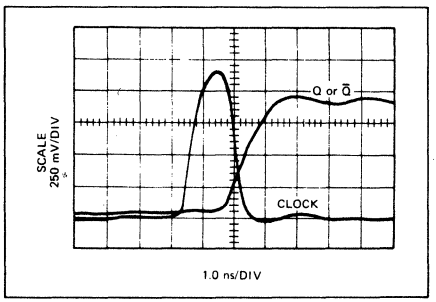


FIGURE 9 – MINIMUM "UP TIME" TO CLOCK
OUTPUT LOAD = 50 Ω



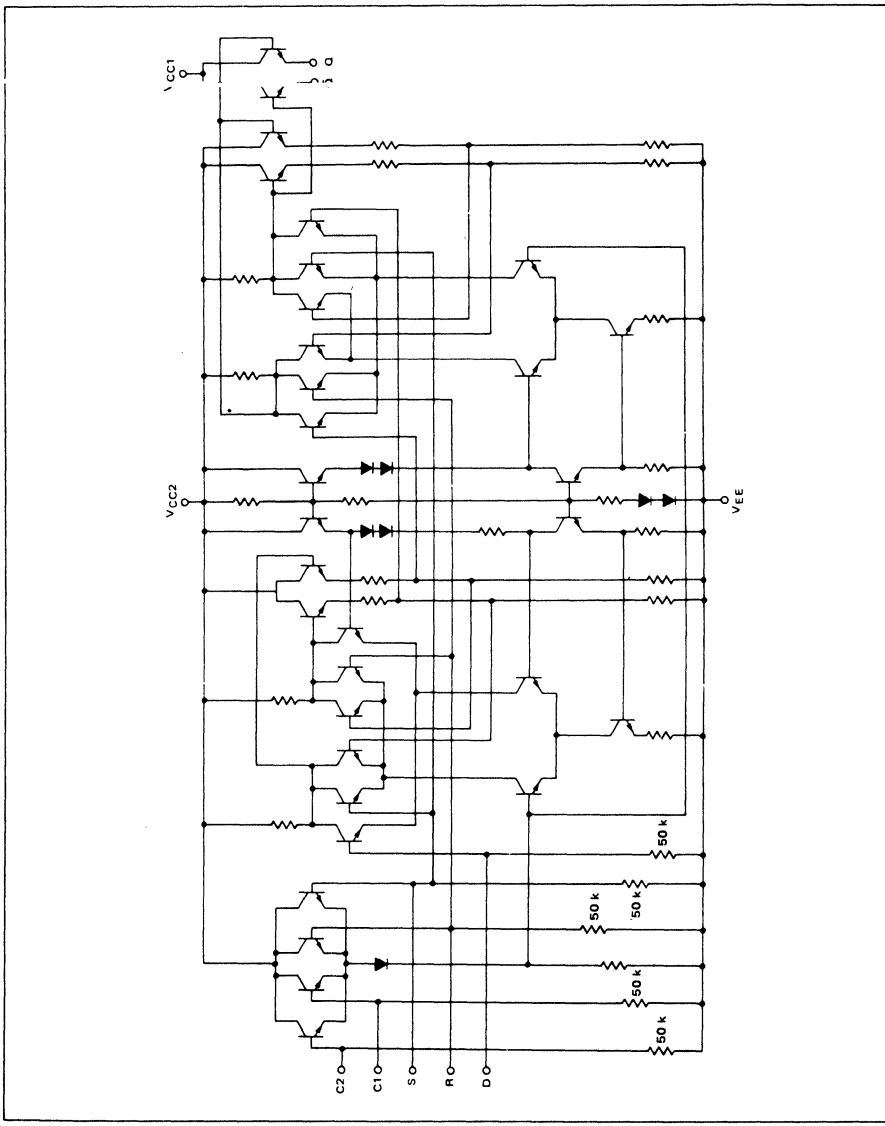
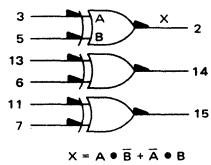


FIGURE 10 – SP1670 CIRCUIT SCHEMATIC

TRIPLE 2-INPUT
EXCLUSIVE-OR GATE

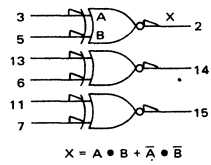
SP1672

POSITIVE LOGIC



$X = A \bullet \overline{B} + \overline{A} \bullet B$

NEGATIVE LOGIC



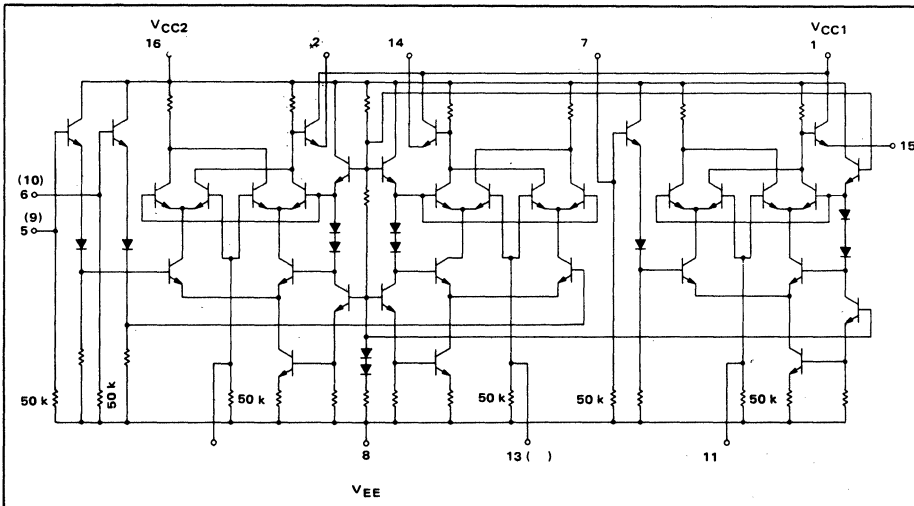
$X = A \bullet B + \overline{A} \bullet \overline{B}$

This three gate array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

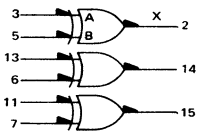
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

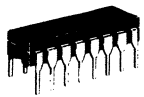
CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.





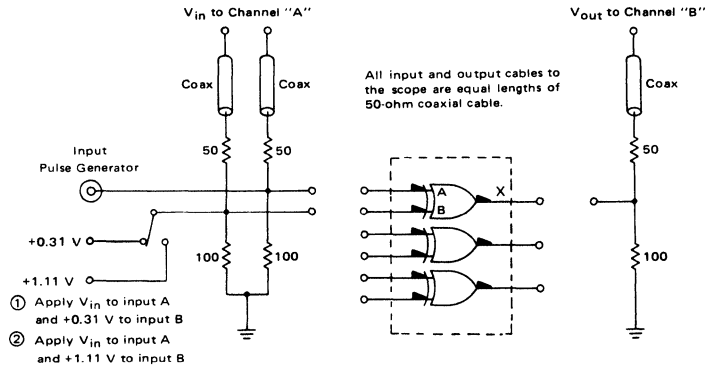
CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1672 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–		55	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	$I_{in\ H}$	3,11,13	–	–	–	350	–	–	µAdc	*	–	–	–	8	1,16
	0.75 $I_{in\ H}$	5,6,7	–	–	–	270	–		µAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–		0.5	–	–		µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3	5	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	3	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3,5	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	3,5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3	5	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	3	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3,5	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	3,5	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max				Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{2+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{2-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

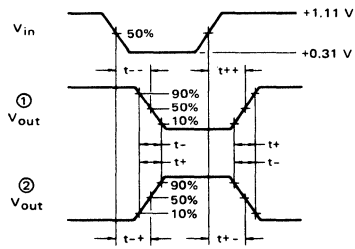
*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Unused outputs connected to a 50-ohm resistor to ground.

PROPAGATION DELAY

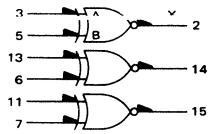


TRIPLE 2-INPUT
EXCLUSIVE-NOR GATE

SP1674

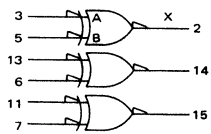
This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30° to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



$X = A \bullet B + \bar{A} \bullet B$

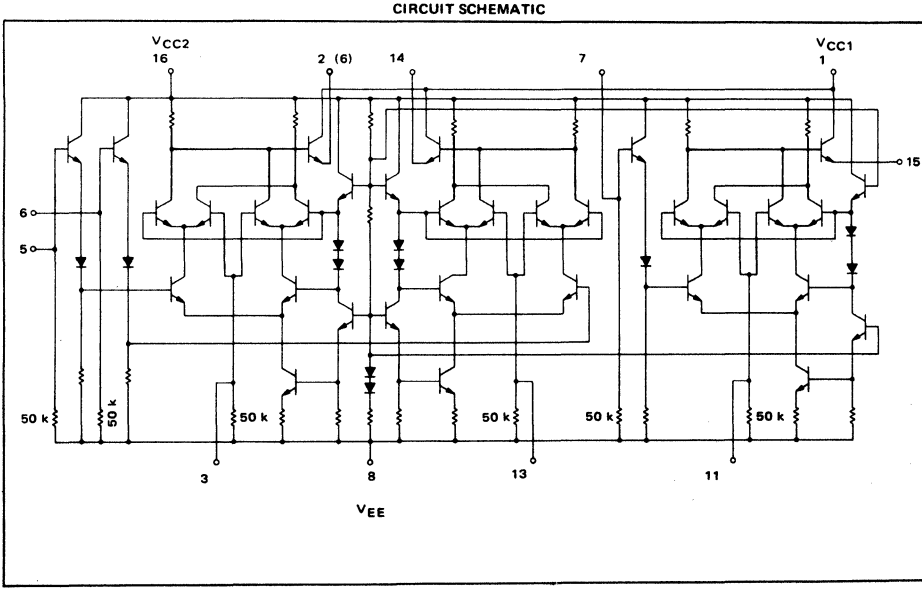
NEGATIVE LOGIC



$X = \bar{A} \bullet B + A \bullet \bar{B}$

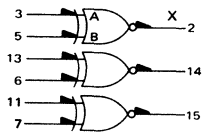
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



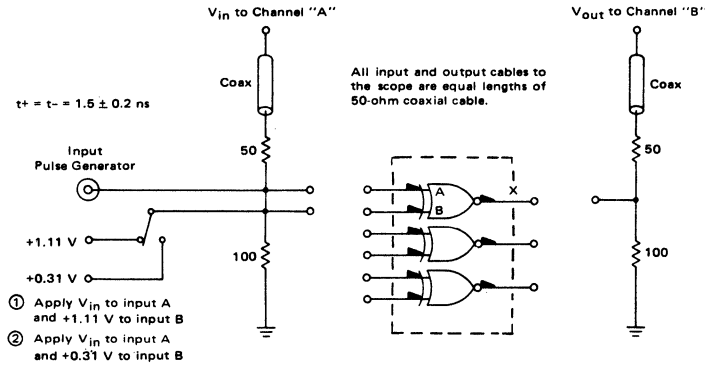
CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1674 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	I_{inH}	3,11,13	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	0.75 I_{inH}	5,6,7	–	–	–	270	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	$V_{OH\phi}$	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3,5	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	3,5	–	–	8	1,16
Logic "0" Output Voltage	$V_{OL\phi}$	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3	5	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	3	–	–	8	1,16
Logic "1" Threshold Voltage	$V_{OHA\phi}$	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3,5	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	3,5	8	1,16
Logic "0" Threshold Voltage	$V_{OLA\phi}$	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3	5	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	3	8	1,16
Switching Times (50 Ω Load)												Pulse In	Pulse Out		
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{6+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{6-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

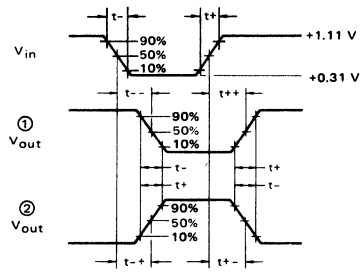
*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Unused outputs connected to a 50-ohm resistor to ground.

PROPAGATION DELAY



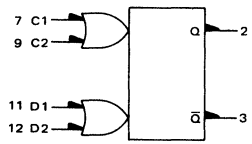
UHF PRESCALER
TYPE D FLIP-FLOP

SP1690

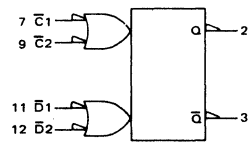
P_D = 200 mW typ/pkg (No Load)
f_{tog} = 500 MHz min

The SP1690 is a high speed D master-slave flip-flop capable of toggle rates over 500 MHz. Designed primarily for high speed prescaling applications in communications and instrumentation, this device employs two data inputs, two clock inputs and complementary Q and $\overline{Q}$ outputs. It is a higher frequency replacement for the SP1670 (350 MHz) D flip-flop. There are no set or reset inputs and an extra data input is provided.

POSITIVE LOGIC

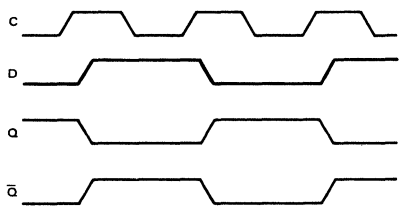


NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

TIMING DIAGRAM



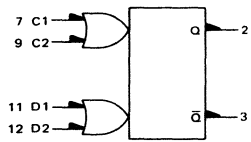
TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⎍	L	L
⎍	H	H

C = C1 + C2 ϕ = Don't Care
D = D1 + D2

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



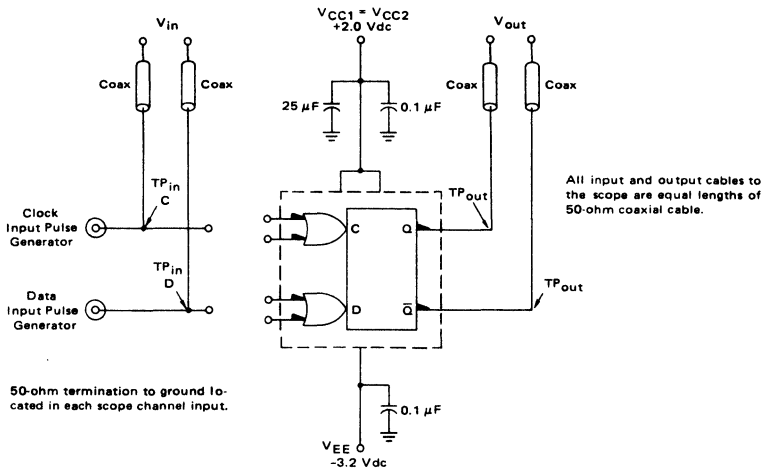
CERAMIC PACKAGE E

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1690. Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P1	P2	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	--	--	--	59	--	--	mAdc	7,9,11,12	--	--	--	8	--	--	1,16
Input Current	$I_{in\ H}$	7	--	--	--	250	--	--	µAdc	7	--	--	--	8	--	--	1,16
		11	--	--	--	270	--	--	µAdc	11	--	--	--	8	--	--	1,16
	$I_{in\ L}$	7	--	--	0.5	--	--	--	µAdc	--	7	--	--	8	--	--	1,16
		11	--	--	0.5	--	--	--	µAdc	--	11	--	--	8	--	--	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	11	--	--	--	8	7	--	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	--	11	--	--	8	7	--	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	--	-0.980	--	-0.910	--	Vdc	11	--	--	--	8	--	7	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	--	-1.630	--	-1.600	--	-1.555	Vdc	--	11	--	--	8	--	7	1,16
Switching Parameters					Min	Typ	Max							-3.2 Vdc			+2.0 Vdc
Clock to Output Delay (See Figure 1)	t_{7+2+}	2	--	--	--	1.5	--	--	ns	--	--	--	--	8	--	--	1,16
	t_{9+2+}		--	--	--	1.5	--	--	ns	--	--	--	--		--	--	
Output Rise Time	t_+		--	--	--	1.3	--	--	ns	--	--	--	--		--	--	
Fall Time	t_-		--	--	--	1.3	--	--	ns	--	--	--	--		--	--	
Setup Time	$t_{setup\ H}$		--	--	--	0.3	--	--	ns	--	--	--	--		--	--	
(See Figure 2)	$t_{setup\ L}$		--	--	--	0.3	--	--	ns	--	--	--	--		--	--	
Hold Time	$t_{hold\ H}$		--	--	--	0.2	--	--	ns	--	--	--	--		--	--	
(See Figure 2)	$t_{hold\ L}$		--	--	--	0.3	--	--	ns	--	--	--	--		--	--	
Toggle Frequency (See Figure 3)	f_{tog}	2	500	--	500	540	--	500	--	MHz	--	--	--	8	--	--	1,16

P1 $V_{IH\ max}$ / $V_{IL\ min}$ P2 $V_{IHA\ min}$ / $V_{ILA\ max}$

FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT



CLOCK DELAY WAVEFORMS @ 25°C

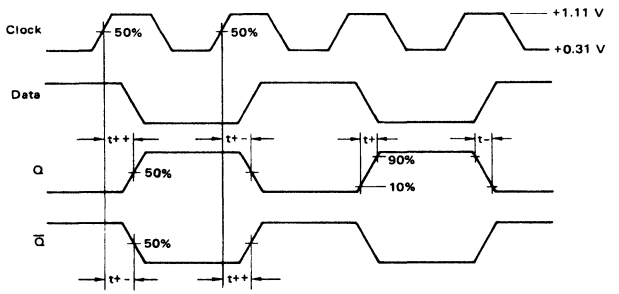
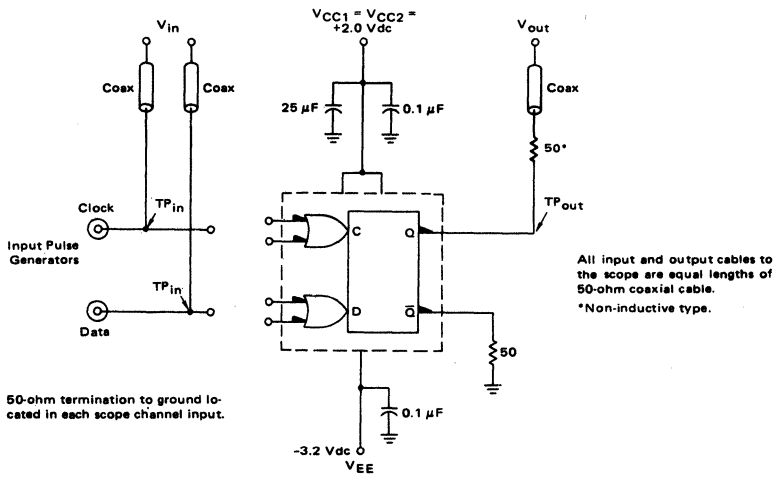
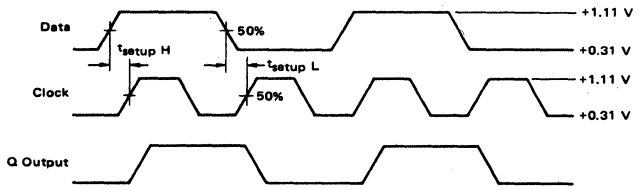


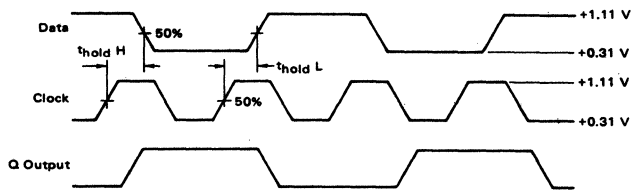
FIGURE 2 – SETUP AND HOLD TIME TEST CIRCUIT



SETUP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Setup time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 3 – TOGGLE FREQUENCY TEST CIRCUIT

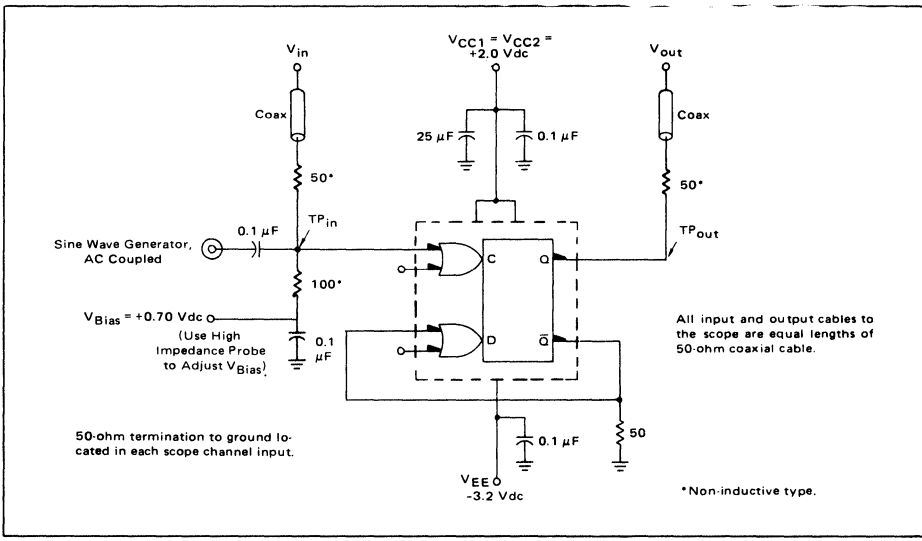
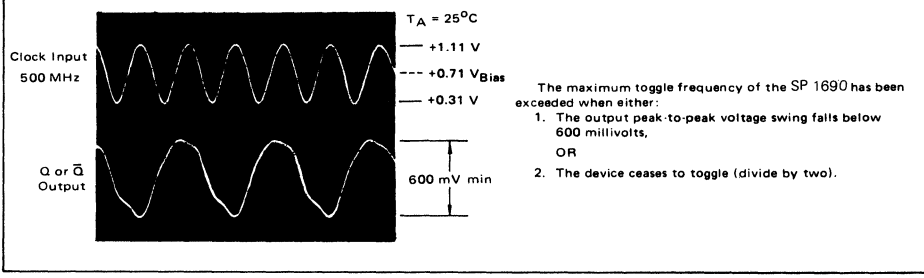


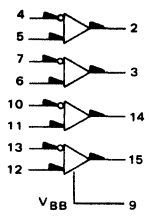
FIGURE 4 – TOGGLE FREQUENCY WAVEFORMS



QUAD LINE RECEIVER

SP1692

Four differential amplifiers with emitter followers intended for use in sensing differential signals over long lines.

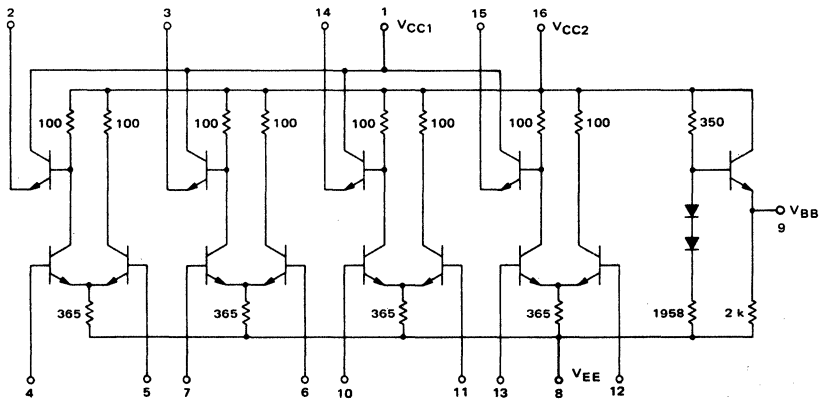


V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

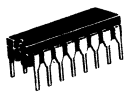
CIRCUIT SCHEMATIC



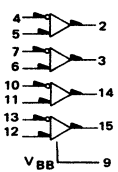
See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



CERAMIC PACKAGE E



● Test Temperature	TEST VOLTAGE VALUES					
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	From Pin 9	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485		-5.2
+85°C	-0.700	-1.830	-1.025	-1.440		-5.2

Characteristic	Symbol	Pin Under Test	SP1692 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	50	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	I_{in}	4	–	–	–	250	–	–	μAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Input Leakage Current	I_R	4	–	–	–	100	–	–	μAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.375	1.275	-1.35	-1.25	1.30	1.20	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out				
Propagation Delay	t_{4-2+}	2	–	1.6	–	1.5	–	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	–	1.8	–	1.7	–	1.9								
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3								
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3								

APPLICATIONS INFORMATION

The SP1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a SP1660 OR/NOR gate. The SP1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the SP1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.60 ns/foot.

The SP1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The SP1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

FIGURE 1 – LINE DRIVER/RECEIVER

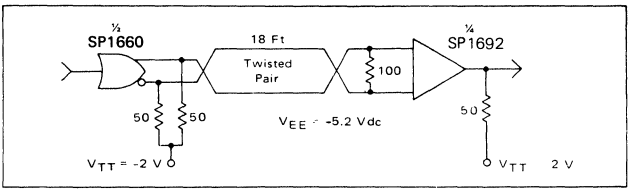


FIGURE 2 – 400 MBS WAVEFORMS

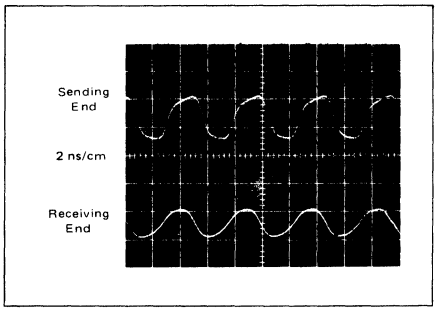
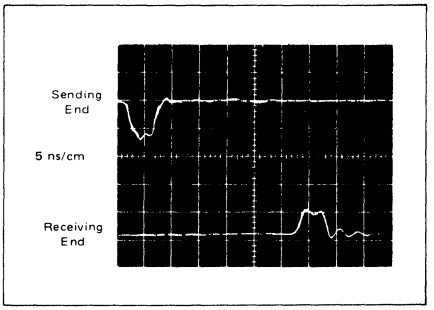


FIGURE 3 – PULSE PROPAGATION WAVEFORMS



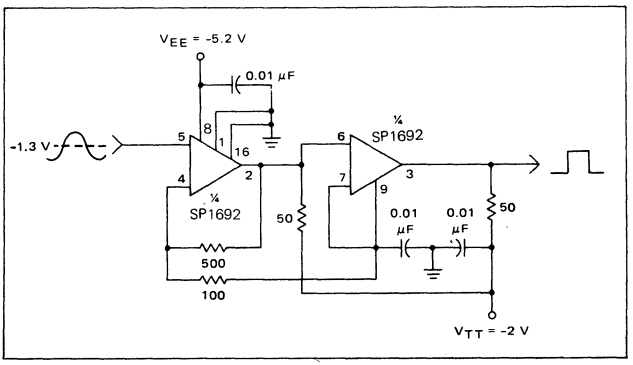


FIGURE 4 – 200 MHz SCHMITT TRIGGER

SP8600A & B

250MHz ÷ 4 COUNTER

The SP8600 is a fixed ratio emitter coupled logic ÷ 4 counter with a specified input frequency range of 15—250 MHz. The operating temperature range is specified by the device code suffix letter: 'A' denotes – 55°C to + 125°C, 'B' denotes 0°C to + 70°C operation.

Intended for use with an external bias arrangment and capacitive coupling to the signal source, the SP8600 can be either single driven, or double driven with two complimentary input signals.

The outputs are complementary free collectors that can have their load resistors taken to any bias voltage up to 12V more positive than V_{EE}.

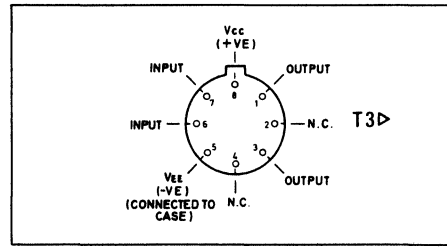


Fig. 1 Pin connections (viewed from beneath)

FEATURES

- Low Power
- Free Collector Outputs to Interface to TTL
- 250 MHz ÷ 4 Over Full Military Temp. Range

APPLICATIONS

- Synthesizers – Mobile and Fixed
- Counters
- Timers

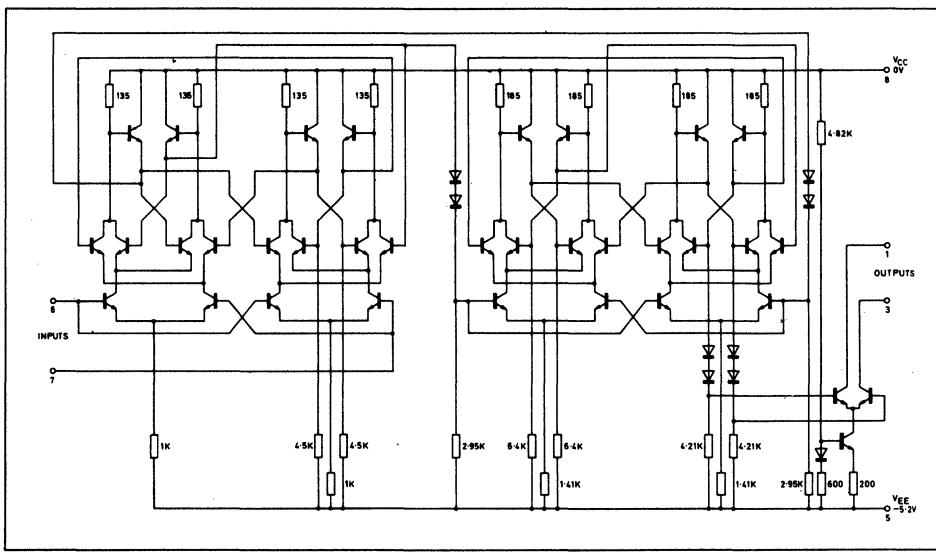


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 'A' Types	−55°C to +125°C
T_{amb} 'B' Types	0°C to +70°C
Supply voltage V_{CC}	0V
V_{EE}	−5.2V ±0.5V
Input voltage (single driven – other input decoupled to ground plane)	400 to 800 mV p-p
Input voltage (double complementary input drive)	250 to 800 mV p-p
Input bias voltage	Bias chain as in test circuit (see Fig. 3 and OPERATING NOTES)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. input frequency	250	390*		MHz	
Min. input frequency with sinusoidal input			25	MHz	
Min. slew rate of square wave input for correct operation			20	V/μs	Single input drive
Output current	2			mA	Input f = 250 MHz
Power supply drain current		16*	23	mA	V_{EE} = −5.2V, V_{BIAS} as Fig. 3

*At +25°C

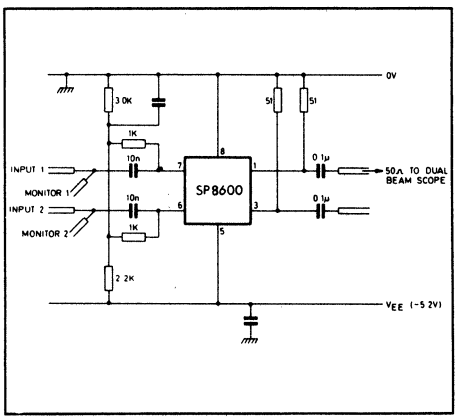


Fig. 3 Test circuit

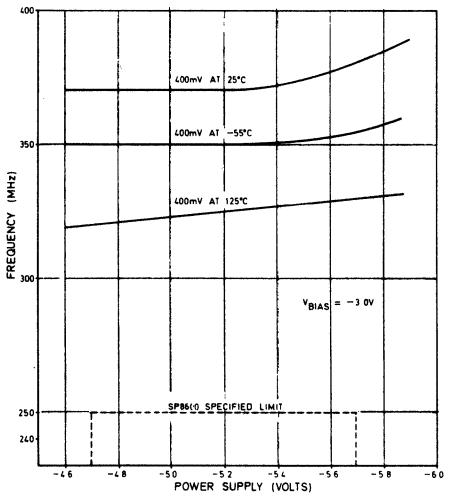


Fig. 4 Maximum input frequency v. power supply voltage (typical)

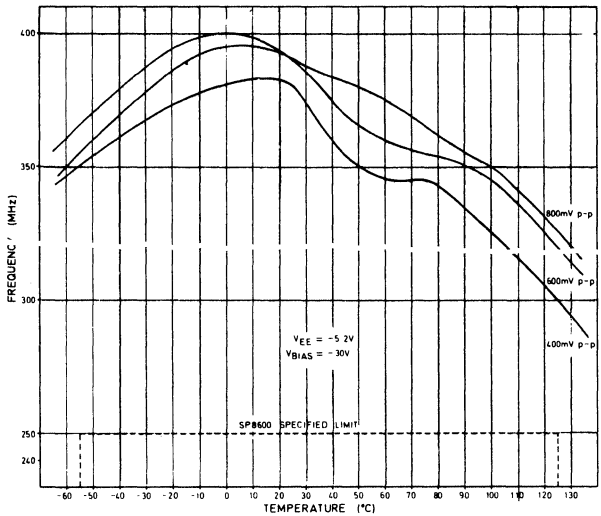


Fig. 5 Maximum input frequency v. temperature

OPERATING NOTES

The circuit performance obtained from the SP8600 is optimized if normal high frequency rules for circuit layout are obeyed – leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally AC coupled to one of the inputs or, if complementary signals are available, to both inputs. The inputs require an external bias chain to set the DC potential on the inputs (see Fig.3). No appreciable change in performance is observed over a range of DC bias from −2.5V to −3.5V.

Any tendency for the circuit to self-oscillate in the absence of input signal (or when the input signal is very small) can be overcome by offsetting the two inputs by approximately 40mV, using, for example, the bias arrangement shown in Fig.6. The input wave form may be sinusoidal, but below 25MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate greater than 20V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with at least 2mA available from them. For satisfactory high frequency interfacing to ECL or Schottky TTL the circuit techniques illustrated in Fig.7 are recommended.

For maximum frequency operation, it is essential that the output load resistor values be such that the output transistors do not saturate. If the load resistors are connected to the OV rail, then saturation can occur with resistance values greater than 600Ω. Of course, if the load resistors are taken to a more positive potential, then higher values can be used. N.B. If only one output is used, the other output should be connected to OV.

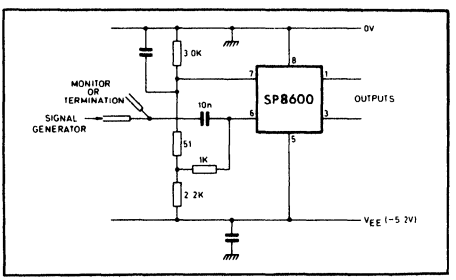


Fig. 6 Bias arrangement to prevent self-oscillation under no-signal conditions.

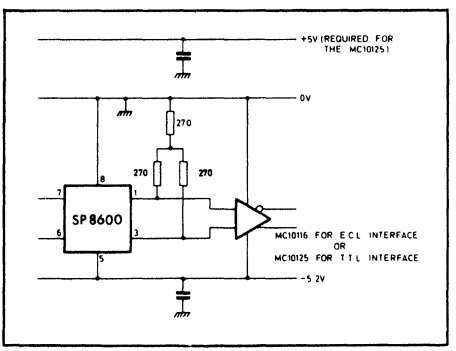
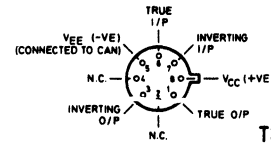


Fig. 7 ECL and Schottky TTL interfacing

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	10V
Input voltage V_{IN}	Not greater than supply voltage in use
Bias voltage on o/p's $V_{OUT} - V_{EE}$	14V
Operating junction temperature	+175°C max.
Storage temperature	−55°C to +175°C

SP8601A & B 150MHz÷4



T3▷

GENERAL DESCRIPTION

The SP8601 is a fixed ratio emitter coupled logic ÷ 4 counter with a maximum specified input frequency of 150 MHz. but with a typical maximum operating frequency well in excess of this (see Typical Operating Characteristics). The operating temperature range is specified by the final coding letter: A denotes −55°C to +125°C, and B denotes 0°C to +70°C.

The SP8601 can be operated with single input drive or with double, complementary, I/P drive. It can be driven with direct coupling from ECL II levels (or from an SP8602 device), or it can be capacitively coupled to the signal source if an external bias is provided.

There are complementary free collector outputs that can have their external load resistor connected to any bias up to 12 volts more positive than V_{EE}.

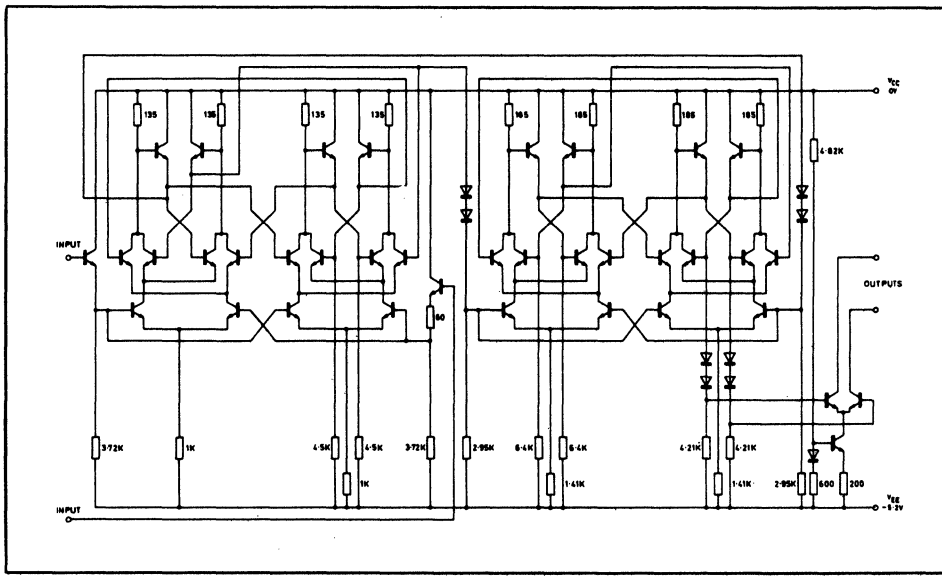


Fig.1 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb}: A variant	−55°C to +125°C
B variant	0°C to +70°C
Operating supply voltage V_{CC}	0V.
V_{EE}	−5.2V ± 0.5V
Input voltage (single drive – other input decoupled to ground plane)	400 to 800 mV (p-p)
Input voltage (double drive)	250 to 800 mV (p-p)
Bias voltage	Bias chain as in test circuit (see Fig.2)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max. input frequency	150			MHz.	
Min. input freq. with sinusoidal input.			10	MHz.	
Min. slew rate of square wave input for correct operation			20	V/μs	Single input drive
Output current	2			mA	Input freq. = 150 MHz, R_{load} = 50Ω
Power supply drain current		18	23	mA	V_{EE} = −5.2V

OPERATING NOTES

Circuit performance obtained from the SP8601 is optimised if normal high frequency rules for circuit layout are obeyed – leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

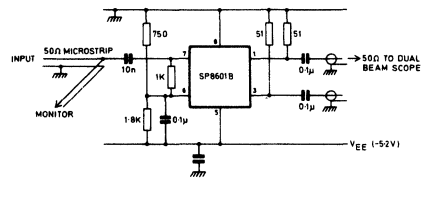
The signal source is normally directly coupled into the device, which will tolerate a wide range of input bias voltages, but was designed for inputs from ECL II levels and can therefore be satisfactorily driven from SP8602 range of counters. The bias voltage on the input marginally affects the overall power consumption of the device (For typical operating characteristics with varying bias voltages see Fig. 3).

If it is not practicable to directly couple the input signal, then a bias chain similar to the one shown in Fig.2 can be used.

The input waveform may be sinusoidal, but below about 10 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate of greater than 20 V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with 2 mA min. available from them. The output voltage swing obviously depends on the value of load resistor used and also the frequency of operation. The following table gives some typical examples of output voltage for different load resistors. With careful board layout to minimise capacitance these figures can easily be exceeded.

Min. Output Voltage	Load Resistor	Input Frequency
1.5 V	1 kΩ	120 MHz
400 mV	200Ω	150 MHz
100 mV	50Ω	180 MHz



NOTE: The value of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

Fig.2 Test circuit

Typical Operating Characteristics

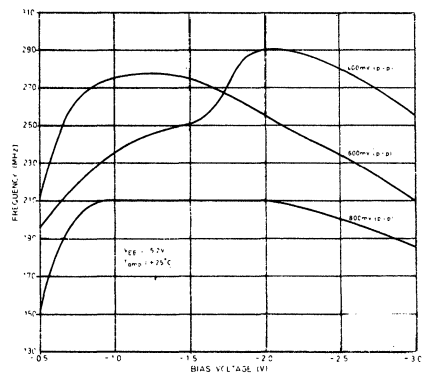


Fig.3 Maximum input frequency v. bias voltage at single input drive levels of 400, 600 and 800 mV (typical device)

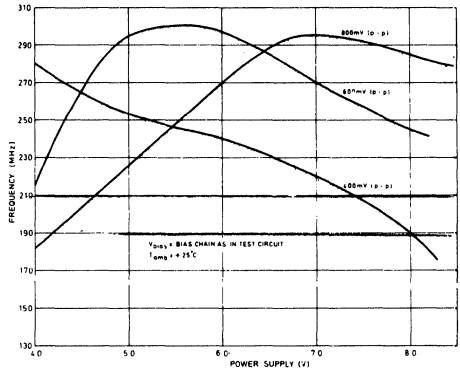


Fig.4 Maximum input frequency v. power supply voltage at single input drive levels of 400, 600 and 800 mV (typical device)

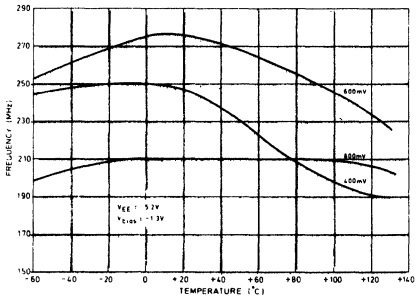


Fig.5 Maximum input frequency v. temperature at single input drive levels of 400, 600 and 800 mV (typical device)

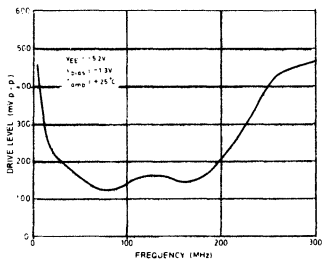


Fig.6 Minimum single input drive level for correct operation v. input frequency (typical device)

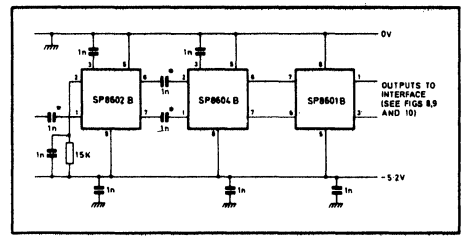


Fig.7 Divide-by-sixteen prescaler

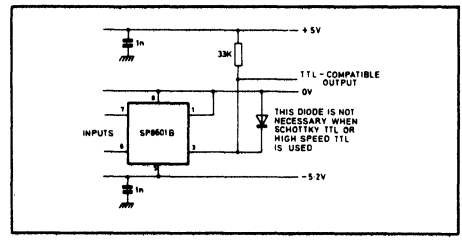


Fig.8 TTL interface (fanout = 1 TTL gate)

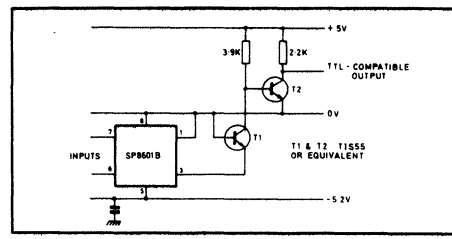


Fig.9 High fanout TTL interface

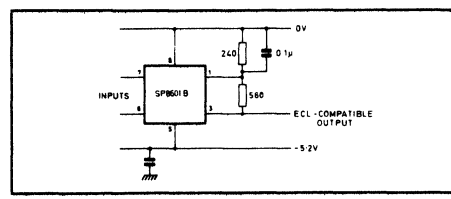


Fig.10 ECL II interface

APPLICATION NOTES

The SP8601 used with two SP8602 series ÷ 2 counters to give a 500 MHz divide-by-sixteen prescaler is shown in Fig.7. Capacitors marked thus * may need to be increased in value for low frequency operation.

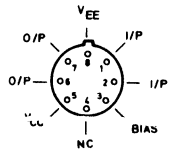
For correct operation when interfacing with TTL and ECL II the circuits shown in Figs.8, 9 and 10 are recommended.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	10 V
Input voltage V_{in}	Not greater than the supply voltage in use
Bias voltage on outputs $V_{out} - V_{EE}$ (see Operating Notes)	14 V
Operating junction temperature	+175°C
Storage temperature	−55°C to +175°C

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8602A & B	**500MHz÷2**
SP8603A & B	**400MHz÷2**
SP8604A & B	**300MHz÷2**



PIN CONNECTIONS (BOTTOM VIEW) T3▷

GENERAL DESCRIPTION

The SP8602, SP8603 and SP8604 are fixed ratio ECL ÷ 2 counters with maximum specified I/P frequencies of 500, 400 and 300 MHz, respectively. The operating temperature range is specified by the final coding letter: A denotes −55°C to +125°C and B denotes 0°C to +70°C.

The devices can be operated with single input drive or with double, complementary, input drive; in both cases the input is normally capacitively coupled to the signal source. Two complementary emitter follower outputs are provided.

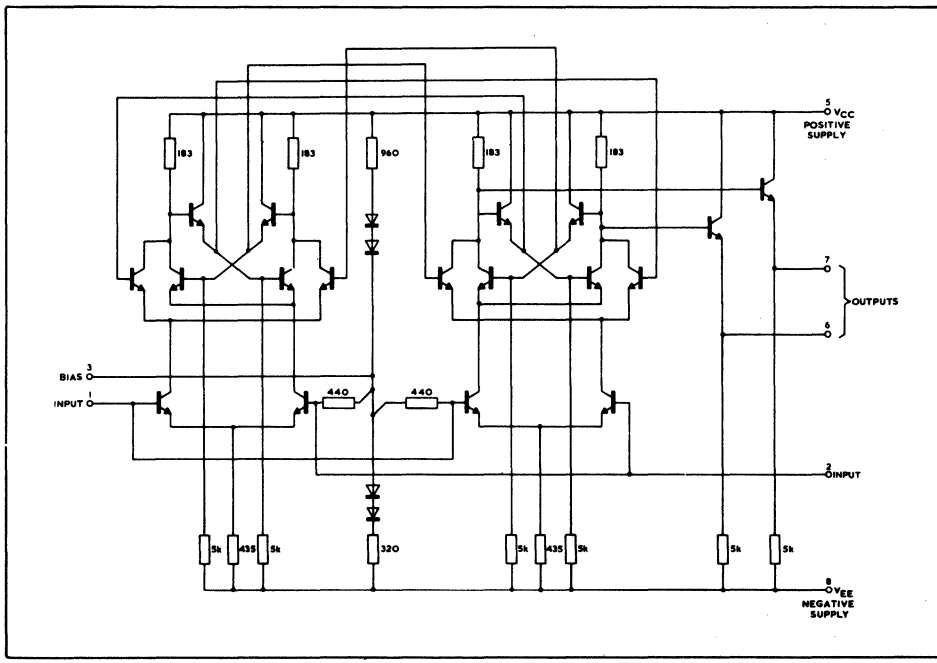


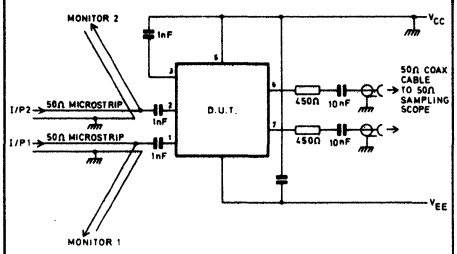
Fig.1 Circuit diagram (all resistor values are nominal)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb}: A variant	−55°C to +125°C
B variant	0°C to +70°C
Operating supply voltage: V_{cc}	0V
V_{ee}	−5.2V ±0.5V
Input voltage (single drive- other input and bias decoupled to ground plane)	400 to 800 mV p-p
Input voltage (double drive- bias decoupled to ground plane)	250 to 800 mV p-p
Output load	500Ω and 3pF

Characteristic	Type	Value				Conditions
		Min.	Typ.	Max.	Units	
Max. input freq.	SP8602A,B	500			MHz	V_{ee} = −5.2V
	SP8603A,B	400			MHz	V_{ee} = −5.2V
	SP8604A,B	300			MHz	V_{ee} = −5.2V
Min. input freq. with sinusoidal input	All		20	40	MHz	
Min. slew rate of square wave input for correct operation	All		30	100	V/μS	single input drive
Output voltage swing	All	400			mV	V_{ee} = −5.2V T_{amb} = −55°C to +70°C
Output voltage swing	SP8602A	350			mV	V_{ee} = −5.2V T_{amb} = +125°C I/P freq. = 500 MHz
Power supply drain current	All		12	18	mA	V_{ee} = −5.2V



Note: The values of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

Fig.2 Test circuit

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{cc} - V_{ee}$	8V
Input voltage V_{in}	Not greater than the supply voltage in use
Output current I_{out}	10 mA
Operating junction temperature	+150°C
Storage temperature range	−55°C to +150°C

OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the output emitter followers are inadvertently shorted to ground. All components used in the circuit layout should be suitable for the frequencies involved, and outside a controlled impedance environment, leads and connections should be kept short to minimise stray inductance.

The signal source is normally capacitively coupled to the input. A 1000pF capacitor is usually sufficient. If the input signal is likely to be interrupted a 10KΩ resistor should be connected between the input and the negative rail. In the single drive case it is preferable to connect the resistor to the input not in use – in the double drive case either input can be used. The addition of the input pulldown resistor causes a slight loss of input sensitivity, but it prevents circuit oscillation under no-signal conditions.

The input waveform may be sinusoidal, but below about 40 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than the amplitude. A square wave input with a slew rate of more than 100 V/μS will permit correct operation down to DC.

The output voltage swing can be increased by the addition of a DC load to the output emitter followers. Pulldown resistors of 1.5 K to the negative rail provide an increase of typically 25% in the output voltage swing.

APPLICATION NOTES

SP8602B and SP8604B interfacing to E C L 10 000 and E C L III

By increasing the output voltage swing using external pulldown resistors (see operating notes), the SP8604B can be coupled directly into an E C L III or E C L 10 000 gate, but there is a reduction of the noise immunity. Where noise immunity is important the device can be connected to an E C L 10 000 or E C L III line receiver.

Divide-by-16 frequency scaler.

The SP8602B and SP8604B interfacing with the SP8601B and high-speed TTL to give a divide-by-16 frequency scaler is shown in Fig. 3.

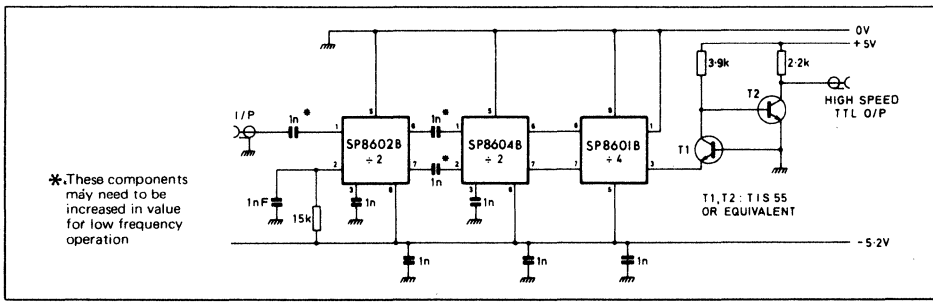


Fig.3 Divide-by-16 frequency scaler

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8616B 1 GHz ÷4 SP8616D 950MHz÷4
SP8615B 900MHz÷4 SP8614B 800MHz÷4
SP8613B 700MHz÷4

The SP8616 series of UHF counters are fixed ratio ÷ 4 asynchronous emitter coupled logic counters with, in the case of the SP616B a maximum operating frequency in excess of 1GHz, over a temperature range of 0°C to +70°C. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100Ω lines and interfacing to ECL with the same positive supply. The SP8616 series require supplies of 0V and −7.4V (± 0.4V).

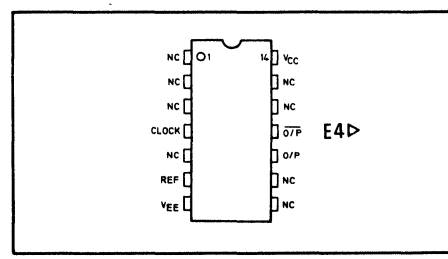


Fig. 1 Pin connections

FEATURES

- DC to 1GHz operation.
- 0°C to 70°C operation guaranteed at maximum specified frequency and over a wide dynamic input range.
- Complementary emitter follower O/Ps, ECL compatible.

APPLICATIONS

- UHF Instrumentation, Including Counters and Timers
- Prescaling for UHF Synthesisers.

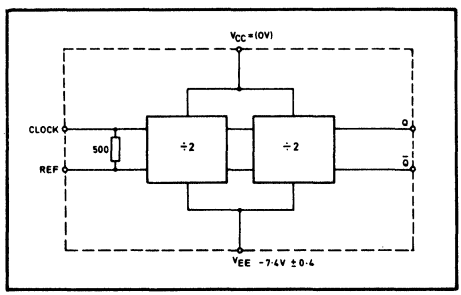


Fig. 2 Functional diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$V_{CC} - V_{EE}$	10 volts
Input voltage	V_{INac}	2.5 volts p-p
Output current		15mA
Storage temperature range		−55°C to +150°C
Maximum operating function temperature		+150°C

QUICK REFERENCE DATA

- V_{CC} = 0V
- V_{EE} = −7.4V ± 0.4V
- Input Voltage Range 400mV to 1.2V (see Fig. 3)
- Temperature Range 0°C to +70°C
- Output Voltage Swing 700mV Typ.

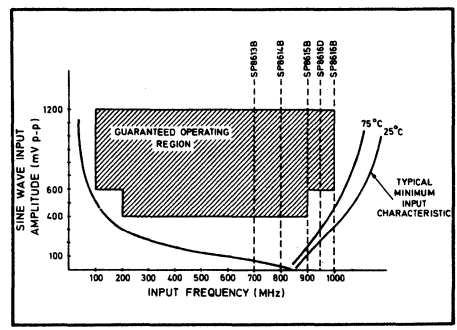


Fig. 3 Specified range of operation

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated).

T_{amb} = 0°C to +70°C
Supply voltage
V_{CC} = 0V
V_{EE} = −7.4V ± 0.4V

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max.toggle frequency	SP8616B	1000			MHz	V_{IN} = 600mV to 1.2Vp-p (see Fig. 3)
	SP8616D	950			MHz	
	SP8615B	900			MHz	V_{IN} = 400MHz to 1.2V p-p
	SP8614B	800			MHz	V_{IN} = 400MHz to 1.2V p-p
	SP8613B	700			MHz	V_{IN} = 400MHz to 1.2V p-p
Min.toggle frequency for correct operation with sine wave input	ALL			200	MHz	V_{IN} = 400mV to 1.2V p-p
Min.toggle frequency for correct operation with sine wave input	ALL			100	MHz	V_{IN} = 600mV to 1.2V p-p
Min slew rate for square wave input to guarantee operation to 0Hz	ALL			200	V/μs	
Output voltage swing	ALL	500	700		mV	
Power supply drain current	ALL		45	60	mA	V_{EE} = −7.4V

Toggle Frequency Test Board Layout

1. All connections to the device are kept short.
2. The capacitors are leadless ceramic types.
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

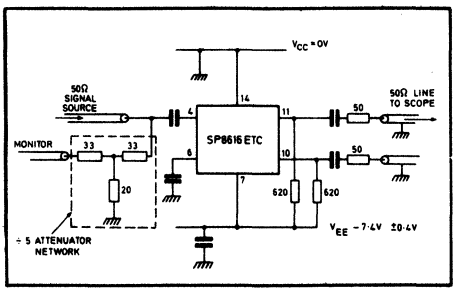


Fig. 4 Toggle frequency test circuit

OPERATING AND APPLICATION NOTE

The SP8616 series of dividers are very simple to use but normal high frequency rules should be followed for optimum performance, for example, all connections should be kept short, the capacitors and resistors should be types suitable for the frequencies involved, etc.

The input is normally capacitively coupled to the signal source. There is an internal 500Ω resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane.

The sensitivity of the device can be increased by DC coupling the input signal about earth (see Fig. 5).

$V_{CC} - V_{EE}$ should be kept inside the specified 7.4 volts ± 0.4 volts but the actual value of V_{CC} relative to earth is not very critical and can be varied between 4.0V and 6.0V with only a small effect on performance. A V_{CC} of about 5.2V is the optimum for full temperature range operation.

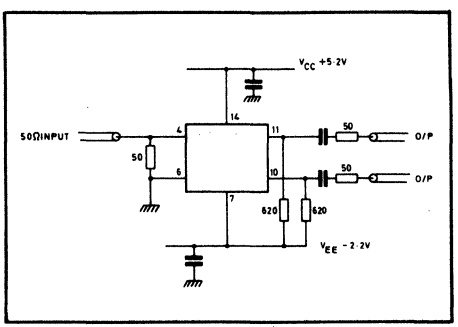


Fig. 5 Circuit for using the input signal about earth potential

In the absence of an input signal both the DC coupled and the capacitively coupled circuits will self oscillate with an output frequency of approximately 200MHz. This can be prevented by connecting a 10kΩ resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8616 will miscount with low frequency sinewave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL II directly and to ECL III using two resistors. (See Fig. 6)

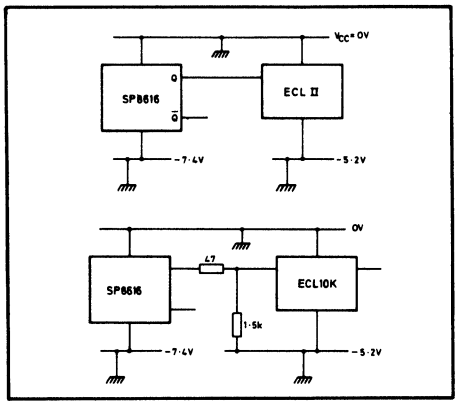


Fig. 6 Interfacing SP8616 series to ECL II and ECL III

The input impedance of the SP8616 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is usually enough signal to operate the device satisfactorily when the input impedance is at a minimum input signal requirement. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

A commercially available hybrid amplifier can be used to drive the SP8616 (see Fig. 7).

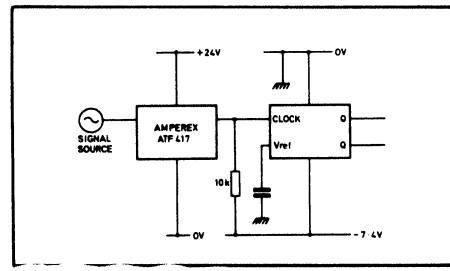


Fig. 7 The SP8616 driven by a commercially available hybrid amplifier. The Amperex ATF417 output is internally capacitively coupled.

Note: The Amperex ATF 417 output is internally capacitively coupled.

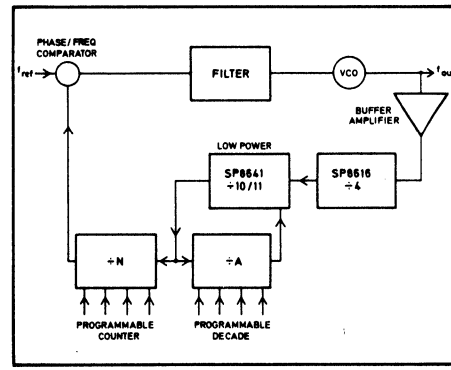


Fig. 8 A 1GHz synthesiser loop

The SP8616 series can be used in instrumentation for direct counting applications up to 1GHz and in frequency synthesisers.

In a frequency synthesiser, the SP8616 and the SP8641 can be used together (see Fig. 8).

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

÷5 COUNTERS

SP8621B (300MHz) SP8622B (200MHz)

The SP8621B and SP8622B are fixed-ratio emitter-coupled logic ÷5 counters with specified input frequency ranges of DC to 300 MHz (SP8621B) and 200 MHz (SP8622B). The operating temperature range is from 0°C to +70°C.

The counter is normally capacitively coupled to the signal source and is specified with an input signal range of 400–800mv p-p (–4dBm to +22dBm). There are two bias points on the circuit that should be capacitively decoupled to the ground plane.

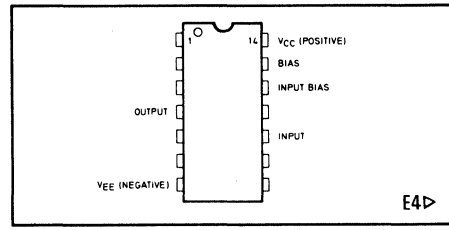


Fig. 1 Pin connections

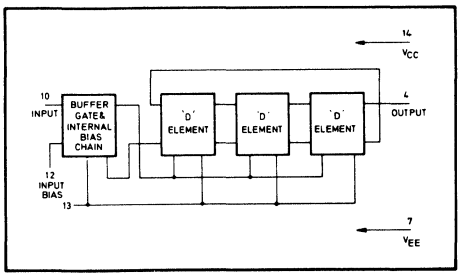


Fig. 2 Functional diagram

FEATURES

- D.C. to 400MHz Operation.
- 0°C to +70°C Over Full Specified Input Range and Frequency

APPLICATIONS

- Frequency Counters and Timers
- Frequency Synthesisers

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

T_{amb}	0°C to +70°C
Supply voltage V_{CC}	0V
V_{EE}	–5.2V ± 0.25V
Input voltage	400 to 800mV p-p

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage V_{IN}	Not greater than supply
Output current I_{OUT}	15mA
Operating junction temperature	+150°C
Storage temperature	–55° to +150°C

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. input frequency	SP8621	300			MHz	
	SP8622	200			MHz	
Min. input frequency with sinusoidal input	All		20	40	MHz	
Min. slew rate of square wave input for correct operation	All		30	100	V/μS	
Output voltage swing	All	400	800		mV	V_{EE} = –5.2V
Power supply drain current	All		55		mA	V_{EE} = –5.2V

OPERATING NOTES

It is recommended that a positive earth plane is used for the circuit layout, thus preventing damage if the output is short-circuited to earth.

The signal source is normally capacitively coupled to the input (see Fig. 3). A 1000pF capacitor is suitable at high frequencies, but if lower frequency operation is also required, say below 10MHz, then an additional capacitor should be connected in parallel. The device can be DC coupled if it is required – see Fig. 4.

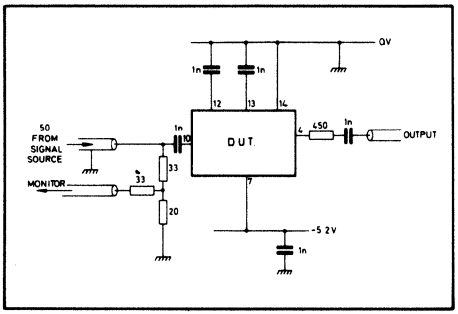


Fig. 3 Test circuit

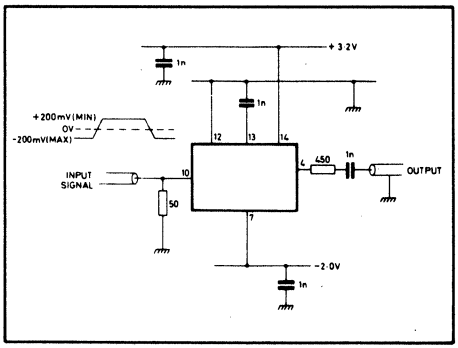


Fig. 4 Directly connecting the input signal (a useful technique at low frequencies)

The circuit may self oscillate when there is no input signal or when the input signal is well below the specified input signal. This can be prevented by connecting a 15kΩ resistor between the input and the negative rail. This causes a loss in sensitivity of up to 100mV p-p.

The input waveform may be sinusoidal, but below about 20MHz the circuit tends to malfunction on minimum amplitude input signals and the condition becomes worse as the frequency is decreased. This is because correct operation of the circuit depends on the slew rate of the input signal. A square wave input with a slew rate greater than 100V/μS ensures correct operation down to DC.

The output swing of the devices can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5kΩ will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8620 devices to interface directly to ECL II devices with no loss in noise immunity. If the devices are required to interface to ECL III or ECL 10,000 then an interface similar to Fig. 5 should be used.

The values of the decoupling capacitors are not critical, but they should be of a type suitable for the frequencies involved.

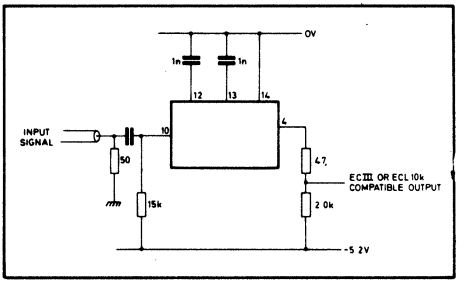


Fig. 5 Interfacing to ECL III or ECL 10,000

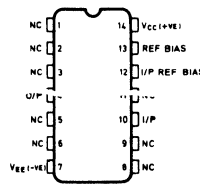
PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8630B 600MHz DECADE COUNTER

SP8631B 500MHz DECADE COUNTER

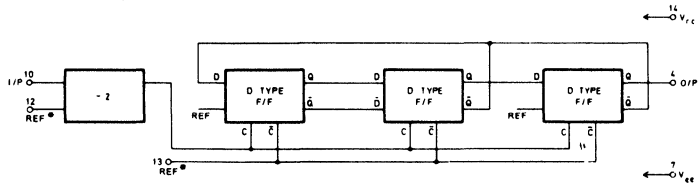
SP8632B 400MHz DECADE COUNTER



PIN CONNECTIONS
(TOP VIEW) E4▷

GENERAL DESCRIPTION

The SP8630/1/2 counters are fixed ratio ÷ 10 circuits using emitter coupled logic, with maximum specified counting frequencies of 600, 500 and 400 MHz respectively, over a temperature range of 0°C to +70°C. A 6:4 mark/space square wave is provided at the emitter follower output. The input is normally single driven and capacitively coupled to the signal source. There are two bias points on the circuit which should be capacitively decoupled to the ground plane.



NOTE:
1. All reference levels are internally generated and temperature compensated.
2. Reference points marked * are bonded out and should be decoupled with a capacitor of between 15 and 1000pF

Fig.1 Block diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless stated otherwise):

T_{amb}	0°C to + 70°C
Operating supply voltage	
V_{CC}	0V
V_{EE}	−5.2V ± 0.25V
Input voltage	400 to 800 mV (p-p)
Output load	500Ω & 3pF.

NOTE: The maximum input frequency is guaranteed at V_{EE} = −5.2V. For typical operating characteristics with power supply variations see Fig.5, which shows that the maximum operating frequency of a typical device increases with increasing power supply voltage

Characteristic	Type	Value			Units	Conditions
		Min	Typ	Max		
Max input freq.	SP8630B	600			MHz	
	SP8631B	500			MHz	
	SP8632B	400			MHz	
Min input freq. with sinusoidal input	All		20	40	MHz	
Min. slew rate of square wave I/P for correct operation	All		30	100	V/μs	
Output voltage swing	All	400	600		mV	V_{EE} = −5.2V
Power supply drain current			70		mA	V_{EE} = −5.2V

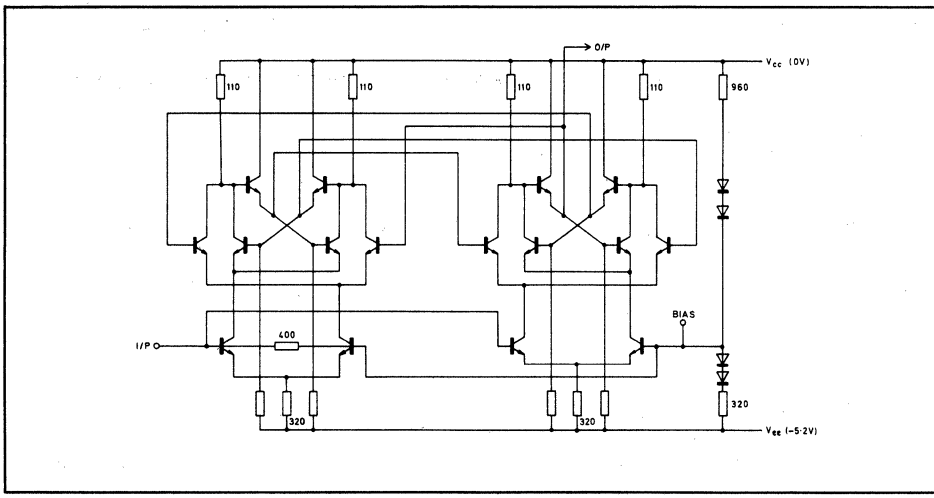


Fig.2 Circuit diagram of 1st element (÷2) showing input biassing arrangement.

OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the emitter follower outputs are inadvertantly shorted to ground.

The signal source is normally capacitively coupled to the input: 1000 pF is usually sufficient. If the input signal is likely to be interrupted a 15 k ohm resistor should be connected between the input pin and the negative rail to prevent circuit oscillation under no-signal conditions. The addition of the pulldown resistor causes a slight loss of sensitivity of the device, but this does not normally cause problems in practice.

The input waveform may be sinusoidal, but below 40 MHz the operation of the circuit becomes dependent on the slew rate of the waveform rather than the amplitude. A square wave input with a slew rate of 100 V/μs will allow correct operation down to DC. At high frequencies, increasing drive level above minimum typically increases the max. operating frequency by up to 25%

The output swing of the device can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5k ohms will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8630 series devices to drive directly into ECL II devices with no loss in noise immunity.

The value of capacitance needed for the decoupling capacitors is not critical. Values down to 15 pF have been found satisfactory in practice.

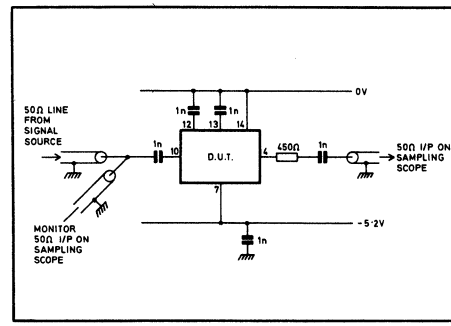


Fig.3 Test circuit.

Test Circuit Notes

The values of the coupling and decoupling capacitors are uncritical but they should be of a type and value suitable for the frequencies involved.

All connections should be physically short when not in a 50Ω environment to minimise reflections due to mismatching.

The +ve pin should be connected to a low impedance earth plane to minimise feed-through of the input signal to the output.

Typical Operating Characteristics

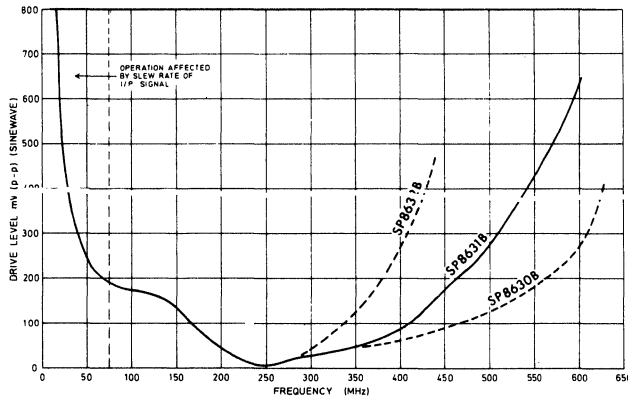


Fig.4 Minimum drive level v. I/P frequency at +25°C.

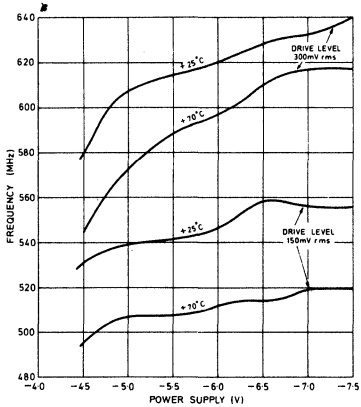


Fig.5 Max. operating frequency v. power supply voltage for a typical SP8631B.

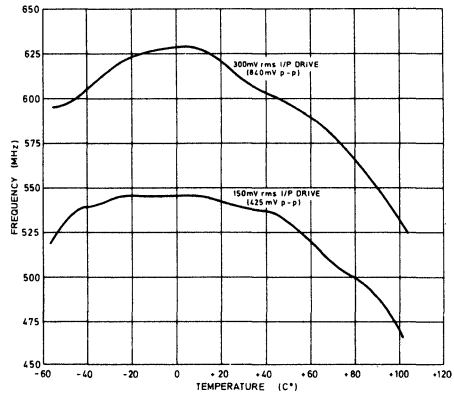


Fig.6 Max. operating frequency v. ambient temperature for a typical SP8631B (V_{CC} = −5.2V).

APPLICATION NOTES

Direct coupling to the SP8630 series.

It can be seen from the circuit diagram that the input arrangement of the SP8630 series is not compatible with the normal ECL logic levels. The input reference level is approximately −3.2 volts but it is not well defined and has a temperature coefficient of approximately −1.6 mV/°C. If DC coupling is required, the input would have to be larger than would be the case with capacitive coupling.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	8V.
Input voltage V_{IN}	Not greater than the supply voltage in use
Output current I_{OUT}	15 mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8634B ÷ 10 700 MHz
SP8636B ÷ 10 500 MHz
SP8635B ÷ 10 600 MHz
SP8637B ÷ 10 400 MHz

The SP8634B, SP8635B, SP8636B and SP8637B are divide-by-ten circuits with binary coded decimal outputs for operation from DC up to specified input frequencies of 700, 600, 500 and 400 MHz, respectively, over a guaranteed temperature range of 0°C to +70°C.

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The BCD outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10k-compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

FEATURES
- Direct gating capability at up to 700 MHz
- TTL- compatible BCD outputs
- TTL- and ECL-compatible carry outputs
- Power consumption less than 500 mW
- Wide dynamic input range

APPLICATIONS
- Counters
- Timers
- Synthesisers

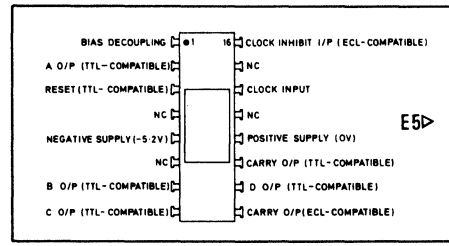


Fig. 1 Pin connections (top)

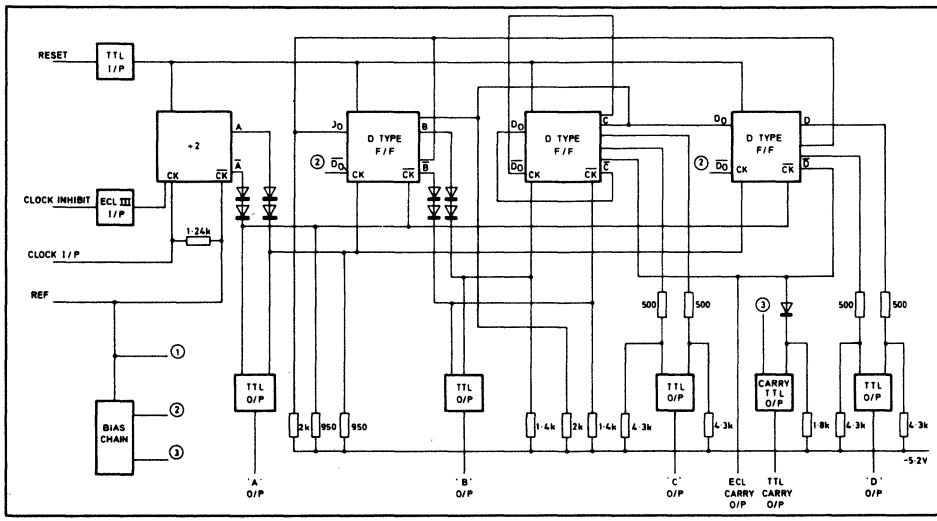


Fig. 2 Logic diagram

QUICK REFERENCE DATA

Power Supplies	V_{CC}	0V
	V_{EE}	−5.2V ± 0.25V
Range of clock input amplitude		400-800mV p-p
Operational temperature range		0°C to +70°C
Frequency range with sinusoidal I/P		40-700 MHz (SP8634B)
Frequency range with square wave I/P		DC to 700 MHz (SP8634B)

ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

Test Conditions (unless otherwise stated)

T_{amb}		0°C to +70°C
Power Supplies	V_{CC}	0V
	V_{EE}	−5.2V ± 0.25V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock Input (pin 14)					
Max. input frequency					
SP8634B	700			MHz	Input voltage 400-800mV p-p
SP8635B	600			MHz	
SP8636B	500			MHz	
SP8637B	400			MHz	
Min. input frequency with sinusoidal I/P			40	MHz	
Min. slew rate of square wave for correct operation down to DC			100	V/μs	
Clock inhibit input (pin 16)					
Logic levels					
High (inhibit)	−0.960			V	T_{amb} = +25°C
Low			−1.650	V	(see Note 1)
Edge speed for correct operation at maximum clock I/P frequency			2.5	ns	10%–90%
Reset input (pin 3)					
Logic levels					
High (reset)	See Note 2				
Low			+0.4	V	
Reset ON time	100			ns	
TTL outputs ABCD (pins 2,7,8,10)					
Output Voltage					
High	+2.4			V	10k Ω resistor and TTL gate from O/P
Low			+0.4	V	to +5V rail
TTL carry output (pin 11)					
Output Voltage					
High state	+2.4			V	5kΩ resistor and 3 TTL gates from o/p
Low			+0.4	V	to 5V rail
ECL carry output (pin 9)					
Output Voltage					
High	−0.975			V	T_{amb} = +25°C External current
Low			−1.375	V	= 0mA (See Note 4)
Power supply drain current		75	90	mA	V_{EE} = 5.2V

NOTES

1. The clock inhibit input levels are compatible with ECL III and ECL 10000 levels throughout the temperature range 0°C to +70°C.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL V_{OH} of +2.4V. Resetting should be done by connecting a 1.8kΩ resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series device.
3. These outputs are current sources which can be readily made TTL-compatible voltages by connecting them to +5V via 10kΩ resistors.
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

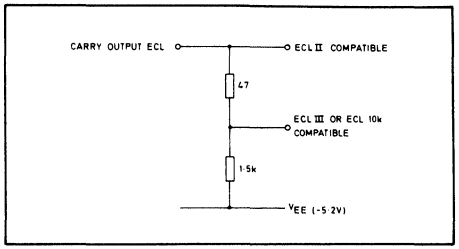


Fig. 3 ECL III/ECL 10000 interfacing

OPERATING NOTES

The devices are intended to be used with TTL and ECL in a counting system – the ECL and the decade counter being connected between voltage rails of 0V and –5.2V and the TTL between voltage rails of 0V and +5.2V. Provided that this is done ECL and TTL compatibility is achieved (see Fig. 4).

The clock is normally capacitively coupled to the signal source: a 1000pF UHF capacitor is normally adequate. If low frequency operation is required the 1000pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor – preferably a chip type – but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV pk/pk. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the V_{CC} connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 68kΩ resistor between the clock input and the negative supply. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason, the input slew rates should be greater than 100 V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit input will clock the device, provided that the other input is in the low state.

The BCD outputs give TTL-compatible outputs (fanout = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the decade and so the state on the BCD outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 4.

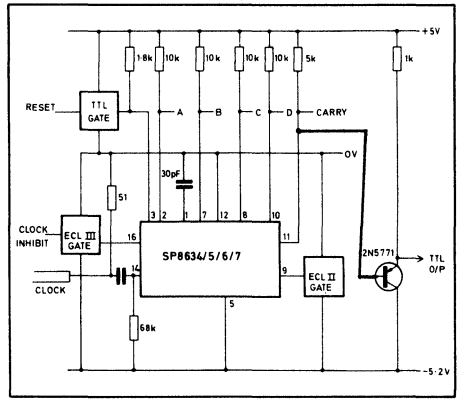


Fig. 4 Typical application configuration

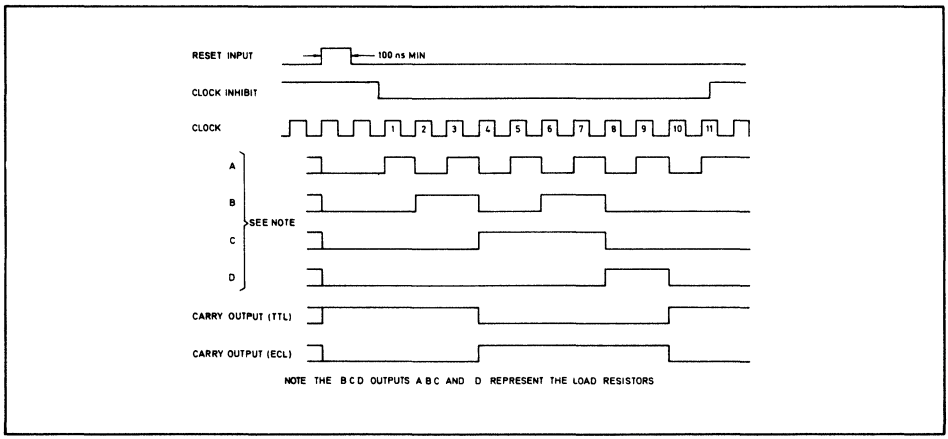


Fig. 5 Decade counter timing diagram

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Clock inhibit voltage	Not greater than the supply voltage in use
Clock input voltage	2V pk/pk
Bias voltage (V_{OUT}) on BCD outputs, $V_{OUT} - V_{EE}$ (10kΩ resistor in series with output)	11V
Bias voltage (V_{OUT}) on TTL carry output, $V_{OUT} - V_{EE}$ (1.2kΩ resistor in series with output)	11V
Output current from ECL carry output (I_{OUT}) (Note: the device will be destroyed if the ECL output is shorted to the negative rail)	10mA
Operating junction temperature	+150°C
Storage temperature range	−55°C to +150°C

UHF PROGRAMMABLE DIVIDERS ÷10/11

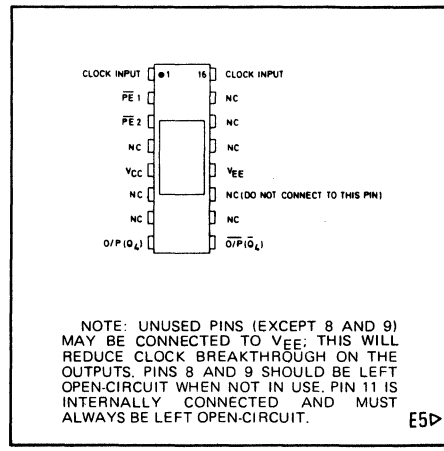
SP8640A & B 200 MHz SP8641A & B 250MHz
SP8642A & B 300MHz SP8643B 350MHz

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8640 series are UHF integrated circuits that can be logically programmed to divide by either 10 or 11, with input frequencies up to 350 MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

All inputs and outputs are ECL-compatible throughout the temperature range: the clock inputs and programming inputs are ECL III-compatible while the two complementary outputs are ECL II-compatible to reduce power consumption in the output stage. ECL III output compatibility can be achieved very simply, however (see Operating Notes).

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either $\overline{PE}$ input is in the high state and by 11 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to V_{EE} (negative rail).



NOTE: UNUSED PINS (EXCEPT 8 AND 9) MAY BE CONNECTED TO V_{EE}; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. PINS 8 AND 9 SHOULD BE LEFT OPEN-CIRCUIT WHEN NOT IN USE. PIN 11 IS INTERNALLY CONNECTED AND MUST ALWAYS BE LEFT OPEN-CIRCUIT. E5▷

Fig. 1 Pin connections (top)

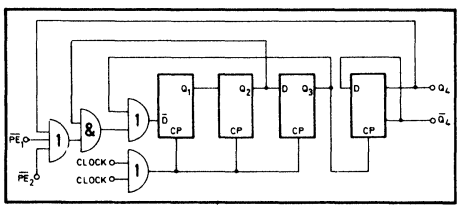


Fig. 2 Logic diagram (positive logic)

FEATURES

- Military and Industrial Variants.
- 350 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs

ABSOLUTE MAXIMUM RATINGS

Supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Input voltage V_{in} (d.c.)	Not greater than the supply voltage in use.
Output current I_{out}	20mA
Max. junction temperature	+150°C
Storage temperature range	−55°C to +175°C

QUICK REFERENCE DATA

- Temperature Ranges:
  'A' Variant −55°C to +125°C
  'B' Variant 0°C to +70°C
- Supply Voltage
  $\lvert V_{CC} - V_{EE} \rvert$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.

Clock Pulse	Q_1	Q_2	Q_3	Q_4
1	L	H	H	H
2	L	L	H	H
3	L	L	L	H
4	H	L	L	H
5	H	H	L	H
6	L	H	H	L
7	L	L	H	L
8	L	L	L	L
9	H	L	L	L
10	H	H	L	L
11	H	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

The maximum possible loop delay for control is obtained if the L→H transition from Q_4 or the H→L transition from $\overline{Q_4}$ is used to clock the stage controlling the ÷10/11. The loop delay is 10 clock periods minus the internal delays of the ÷10/11 circuit.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb}: 'A' Variant −55°C to +125°C
'B' Variant 0°C to +70°C
Supply voltage (see note 1): V_{CC} 0V
V_{EE} −5.2V

Static Characteristics (all SP8640 series devices)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Clock and $\overline{PE}$ input voltage levels					
V_{INH}	−1.10		−0.81	V	T_{amb} = +25°C,
V_{INL}	−1.85		−1.50	V	see Note 2
Input pulldown resistance, between pins 1, 2, 3, and 16 and V_{EE} (pin 12)		4.3		KΩ	
Output voltage levels					
V_{OH}	−0.85			V	T_{amb} = +25°C,
V_{OL}			−1.50	V	see Note 3. I_{out} (external) = 0mA (There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output)
Power supply drain current		50	65	mA	

NOTES

1. The devices are specified for operation with the power supplies of V_{CC} = 0V and V_{EE} = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of V_{CC} = +5V ± 0.25V and V_{EE} = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

Dynamic Characteristics

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock input voltage levels						
V_{INH}	All	−1.10		−0.90	V	T_{amb} = +25°C,
V_{INL}	All	−1.70		−1.50	V	see Note 4
Max. toggle frequency	SP8643	350			MHz	
	SP8642	300			MHz	
	SP8641	250			MHz	
	SP8640	200			MHz	
Min. frequency with sinewave clock input	All			50	MHz	
Min. slew rate of square wave input for correct operation down to 0MHz	All			100	V/μs	
Propagation delay (clock input to device output)	All		3		ns	
Set-up time	All		1.5		ns	See note 5
Release time	All		1.5		ns	See note 6

NOTES

4. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the imput reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse (see Fig. 3).
6. Release time is defined as the mimimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse (see Fig. 4).

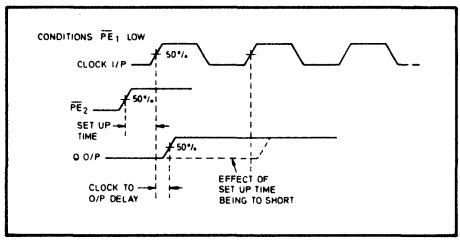


Fig. 3 Set-up timing diagram

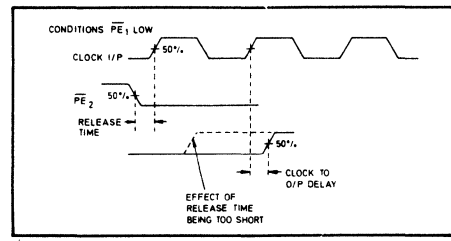


Fig. 4 Release timing diagram

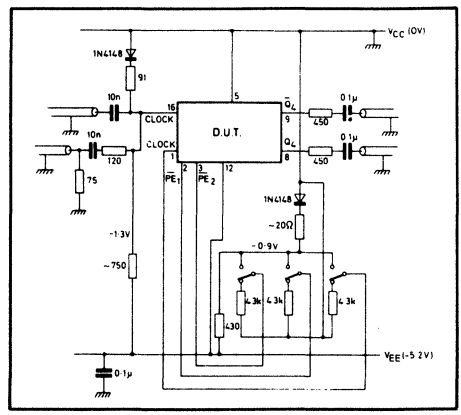


Fig. 5 Test circuit for dynamic measurements

OPERATING NOTES

The SP8640 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control imputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

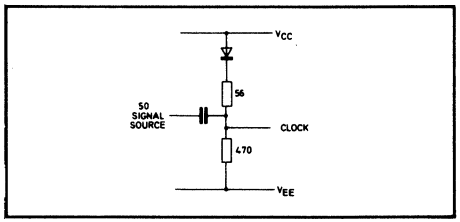


Fig. 6 Recommended input bias configuration for capacitive coupling to a continuous 50Ω signal source.

The ÷10/11 can be controlled by a TTL fully-programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface requires some gain and therefore uses a transistor. This interface as shown on Fig. 7, gives the true output; the inverse can be obtained by interchanging the Q_4 and $\overline{Q_4}$ outputs. The output interface will operate satisfactorily over the full military temperature range (−55°C to +125°C) at frequencies in excess of 35MHz. It has a fan out of one and the propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10ns. At an input frequency of 350 MHz this would only leave about 16ns for the fully-programmable counter to control the ÷10/11. The loop delay can be increased by extending the ÷10/11 function to, say, ÷20/21 or ÷40/41 (see Application Notes).

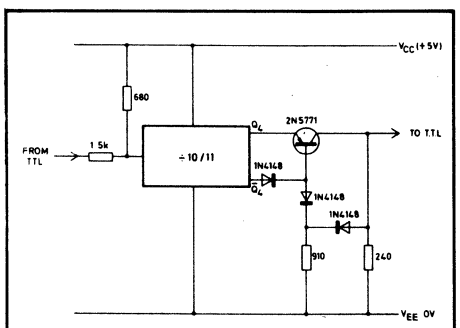


Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8640 devices and TTL operating from the same supply rails)

The SP8640 device O/Ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can also be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

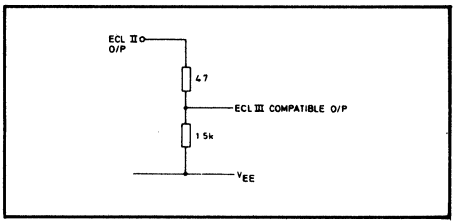


Fig. 8 ECL II to ECL III interface

APPLICATION NOTES

In the divider chain of a frequency synthesiser it is desirable to start programmable division at as high a frequency as possible. The ÷10/11 function permits programmable division to begin at a higher frequency than would be possible with a fully programmable divider. It also means that high frequency prescaling occurs without any reduction in comparison frequency, since it is no longer necessary to divide the reference frequency by the modulus of the prescaler. The disadvantages of the technique are that a fully programmable divider is required to control the ÷10/11, and that a minimum limit is set on the division ratio possible — although the latter is not a serious problem in a practical loop.

Using the ÷10/11

Consider the system shown in Fig. 9. If the ÷P/P+1 is a ÷10/11, the ÷A counter counts the units and the ÷M counter counts the tens.

The mode of operation depends on the type of programmable counter used, but the system might operate as follows. If the number loaded in A is greater than zero then the ÷P/P+1 counter is set up to divide by P+1 at the start of the cycle. The output from the ÷P/P+1 counter clocks both A and M. When A is full it ceases counting and sets the ÷P/P+1 into the ÷P mode. Only M is then clocked and when it is full it resets both A and M and the cycle re-starts.

The divider chain therefore divides by:−

$$\begin{aligned} & (M - A)\,P + A\,(P + 1) \\ = \; & MP + A \\ \therefore f_{out} \; = \; & (MP + A) f_{ref} \end{aligned}$$

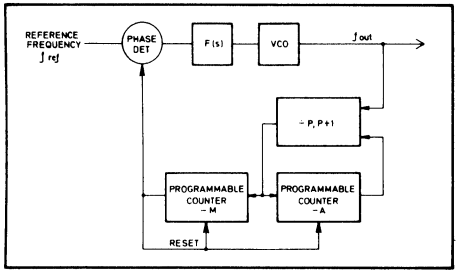


Fig. 9 Synthesiser block diagram (simplified)

Therefore, if A is incremented by one, the output frequency changes by f_{ref}. In other words, the channel spacing = f_{ref}. This is the channel spacing that would be obtained with a fully-programmable divider operating at the same frequency as the ÷P/P+1.

For this system to work, the ÷A counter must fill up before the ÷M counter, otherwise the ÷P/P+1 will stay permanently in the ÷P+1 mode. There is therefore a minimum system division ratio below which the ÷P/P+1 system will not function. In order to find that minimum ratio, consider the following argument.

The ÷A counter must be capable of counting all numbers up to and including P–1 if every division ratio is to be possible, or:

$$A_{max} = P-1$$
$$M_{min} = P, \text{ since } M>A$$

The divider chain divides by MP + A,

$$\therefore \text{Min. division ratio} = M_{min}P + A_{min}$$
$$= P.P+0$$
$$= P^2$$

Using a ÷10/11, therefore, the minimum practical division ratio of the system is 100, which would not normally be an embarassment.

In the system shown in Fig. 9, the fully programmable counter A has to be quite fast. With a 350 MHz clock to the ÷10/11, there is only about 23ns available for counter A to control the ÷10/11. For cost reasons it would be desirable to use a TTL fully programmable counter but when the delays through the ECL to TTL translators have been taken into account there is very little time left for the fully programmable counter. The ÷10/11 function can be extended easily, however, to give a ÷N/N+1 counter with a longer control time for a given input frequency, as shown in Figs. 10 and 11. Using the ÷20/21 system shown in Fig. 10, the time available to control ÷20/21 is typically 87ns at 200MHz and 44ns at 350MHz. The time available to control the ÷40/41 (Fig. 11) is approximately 180ns at 200MHz and 95ns at 350MHz.

This technique can, of course, be extended to give ÷80/81, which would allow the control to be implemented with CMOS but which would increase the minimum division ratio to 6400 (80^2). This is too large a ratio for many synthesiser applications but it can be reduced to 3200 by making the counter a ÷80/81/82. Similarly, a ÷40/41 can be extended to ÷40/41/42 as shown in Fig. 12

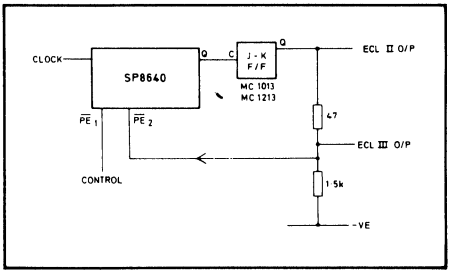


Fig. 10 A ÷20/21 system

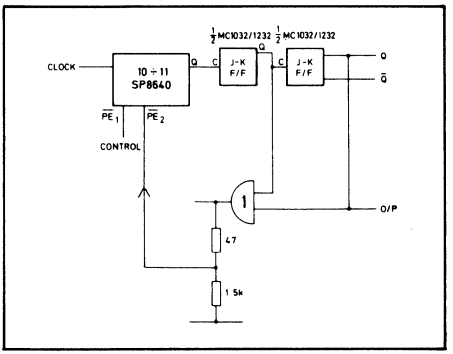


Fig. 11 A ÷40/41 system

to reduce the minimum division ratio from 1600 to 800. The time available to control the ÷40/41/42 is a full 40 clock pulses, i.e. 200ns at 200 MHz input clock or 110ns at 350MHz.

The principle of operation is as follows:

Min. division ratio 800 = (20 x 40) + (0 x 41) + (0 x 42)
801 = (19 x 40) + (1 x 41)
802 = (19 x 40) + (2 x 42)

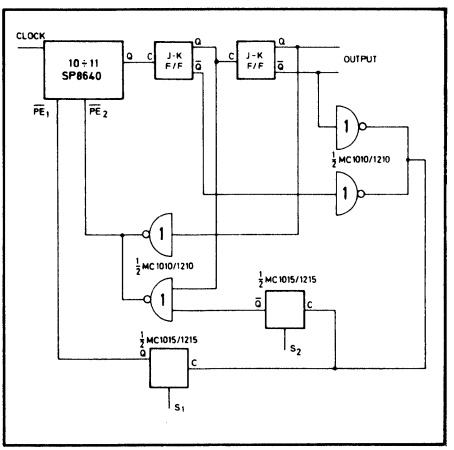


Fig. 12 A ÷40/41/42 system

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8650D 600MHz÷16 SP8651B 500MHz÷16

SP8652B 400MHz÷16

The SP8650 series of UHF ÷ 16 counters are fixed ratio synchronous emitter coupled logic counters with, in the case of the SP8650B, a maximum operating frequency in excess of 600 MHz over a temperature range of 0°C to +70°C. The input is normally capacitively coupled to the signal source but the circuits can be DC driven if required. The inputs can be either single driven relative to the on-chip reference voltage or differentially driven.

There are two complementary emitter follower outputs.

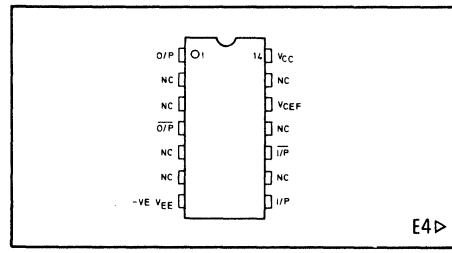


Fig. 1 Pin connections

FEATURES

- Low Power – Typically 250mW
- ECL II & ECL III Output Compatibility
- Easy Operation From UHF Signal Source

APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

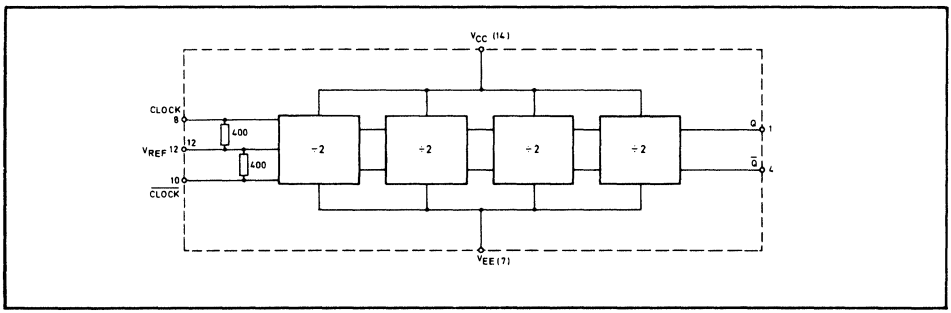


Fig. 2 Functional diagram

QUICK REFERENCE DATA

■	Power Supplies	V_{CC} = 0V V_{EE} = –5.2V ± 0.25V
■	Temp Range	0°C to +70°C
■	Input Amplitude range	400mV to 800mV p-p
■	Output Voltage Swing	800mV typ. p-p

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} = 0°C to +70°C
Supply Voltage
V_{CC} = 0V
V_{EE} = −5.2V ± 0.25V
Output load = 500Ω line in parallel with approx. 3pF

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
						Test circuit as in fig. 2
Max. Toggle frequency	SP8650B	600			MHz	V_{IN} = 400 to 800mV p-p
	SP8651B	500			MHz	V_{IN} = 400 to 800mV p-p
	SP8652B	400			MHz	V_{IN} = 400 to 800mV p-p
Min. toggle frequency for correct operation with a sinewave input	All			40	MHz	V_{IN} = 400 to 800mV p-p
Min. slew rate for square wave input to guarantee correct operation to 0Hz	All			100	V/μs	
Input reference voltage	All		2.6		V	
Output voltage swing (dynamic)	All	500	800		mV	p-p
Output voltage (static)						
high state	All	−8.95		.615	V	
Low state	All	−1.83		−1.435	V	
Power supply drain current	All		45	60	mA	

Toggle Frequency Test Circuit

1. All leads are kept short to minimise stray capacitance and induction.
2. Resistors and capacitors are non-inductive UHF types.
3. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

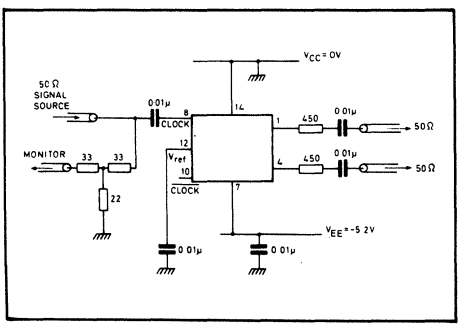


Fig. 3 Toggle frequency test circuit

OPERATING NOTE

Normal UHF layout techniques should be used if the SP8650 series of dividers are to operate satisfactorily. If the positive supply is used as the earth connection, noise immunity is improved and the risk of damage due to inadvertently shorting the output emitter followers to the negative rail is reduced.

The circuit is normally capacitively coupled to the signal source. In the absence of an input signal the circuit will self-oscillate. This can be prevented by connecting a 10KΩ resistor between one of the inputs and the negative rail.

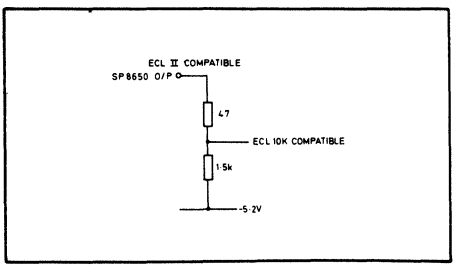


Fig. 4 SP8650 to ECL 10K interface

The device will also miscount if the input transitions are slow – a slew rate of 100V/μs or greater is necessary for low frequency operation.

The outputs interface directly to ECL II or to ECL 10K with a potential divider (see Fig. 4).

A typical application of the SP8650 series devices would be in the divider chain of a synthesiser operating in the military frequency range 225 MHz to 512 MHz. A binary division rate is optimum where power is at a premium and so the SP8650 series would normally be used in low power applications.

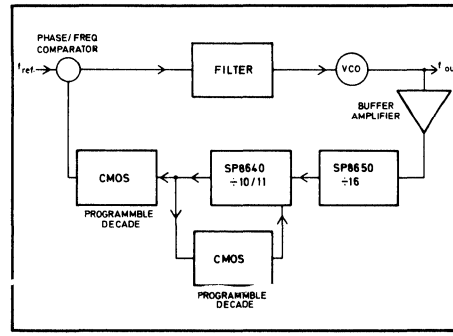


Fig. 5 A low power synthesiser loop

ABSOLUTE MAXIMUM RATINGS

Power supply voltage	$\|V_{CC} - V_{EE}\|$	8 volts
Input voltage	V_{INac}	2.5V p-p
Output source curr	I_{out}	10mA
Storage temperature range		−55°C to +125°C
Operating junction temperature		150°C max.

PLESSEY
SEMICONDUCTORS

SP8000 SERIES
HIGH SPEED DIVIDERS

SP8655A & B (÷32)

SP8657A & B (÷20) SP8659A & B (÷16)

The SP8655A & B, SP8657A & B and SP8659A & B are fixed ratio (divide by 32, 20 and 16) low power counters for operation at frequencies in excess of 100MHz over the temperature ranges −55°C to +125°C (suffix 'A' devices) and 0°C to +70°C (suffix 'B' devices).

In all cases, the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used, the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should also be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible
- Military and Commercial Temperature Ranges

APPLICATIONS

- Low Power VHF Communications
- Portable Counters

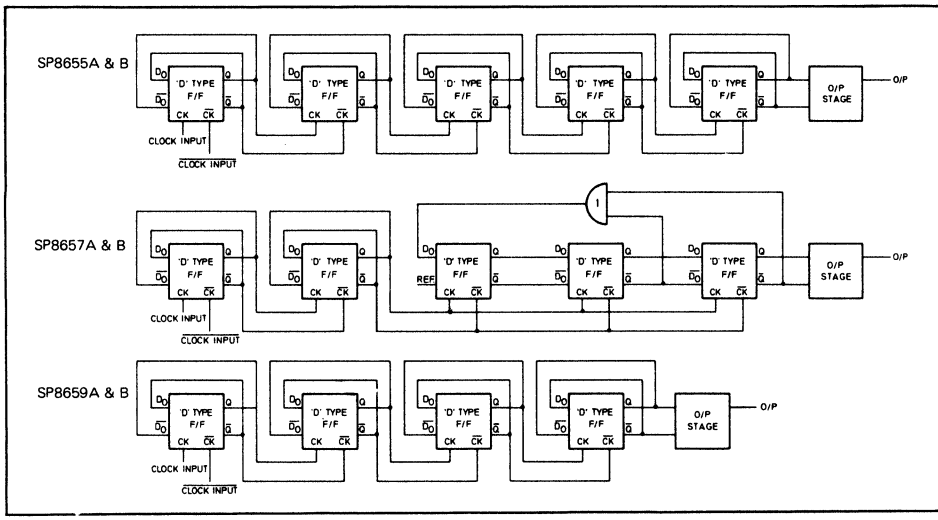


Fig.1 Logic diagrams

ABSOLUTE MAXIMUM RATINGS

Power supply voltage, $V_{CC} - V_{EE}$	8V
Input voltage V_{in}	Not greater than supply voltage in use
Output sink current, I_o	10mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

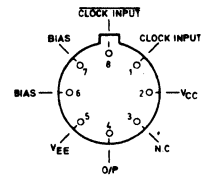


Fig.2 Pin connections (viewed from beneath)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

Operating ambient temperature T_A
'A' Types: −55°C to +125°C; 'B' Types: 0°C to 70°C
Operating supply voltages
V_{CC}: +5.2V ± 0.25V; V_{EE}: OV
Input voltage
Single drive: 400mV to 800mV p-p; double drive: 250mV to 800mV p-p
Output load 3.3kΩ to +10V, in parallel with 7pF.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Maximum input frequency	100	200		MHz	
Minimum sinusoidal input frequency		20	40	MHz	
Minimum slew rate of square wave input		30	100	V/μs	
Power supply drain current		10	13	mA	V_{CC} = +5.2V
Output level (high)	9.0			V	
Output level (low)			400	mV	

OPERATING NOTES

Fig.3 gives capacitor values for AC and DC coupling of the input and bias points on the test circuit; these values are not critical and will depend on the operating frequency.

The devices will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39kΩ pulldown resistor from either input (double drive) to V_{EE}; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3kΩ (or less) to +10V will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

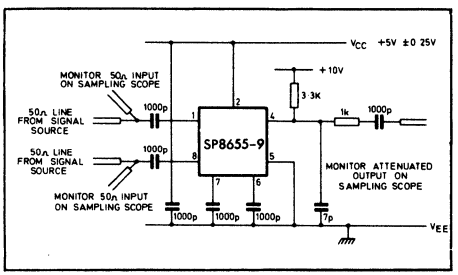
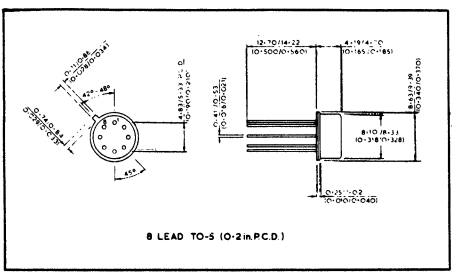


Fig.3 Test circuit

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



UHF DECADE COUNTERS

SP8665B 1.0GHz ÷ 10 SP8666B 1.1GHz ÷ 10

SP8667B 1.2GHz ÷ 10

The SP8665/6/7 high speed decade counters operating at an input frequency of up to 1GHz over the temperature range 0°C to +70°C.

The device has a typical power dissipation of 550mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15kΩ resistor from the input to V_{EE} (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common V_{CC} to the SP8665/6/7. A 6kΩ pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8665/6/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

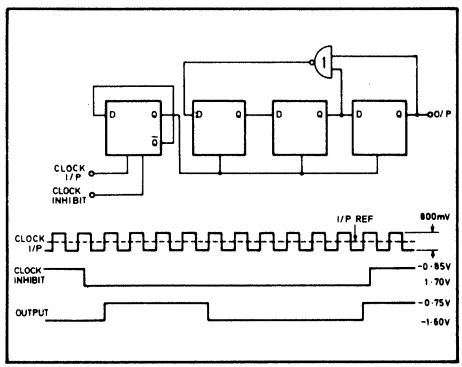


Fig. 2 Logic diagram

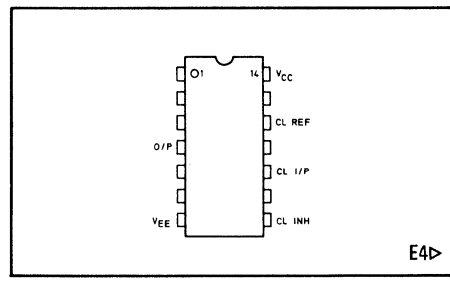


Fig. 1 Pin connections

FEATURES

- Guaranteed operation over large temperature range 0°C to 70°C
- Wide input dynamic range
- Self biasing clock input
- Clock inhibit input for direct gating capability

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +10V
Input voltage inhibit input	V_{EE} to V_{CC}
Input voltage CP input	2.5V p-p
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to 150°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

Supply voltage	6.8V ± 0.3V
Clock input	AC coupled, self-biasing
Clock inhibit input	ECL III compatible
Output	ECL II compatible
T_{amb}	0°C to +70°C
Supply voltage	V_{CC} = 0V V_{EE} = −6.8V
Clock input voltage	400mV to 1.2V (peak to peak)

Characteristics		Value			Units	Conditions
		Min.	Typ.	Max.		
Max. i/p frequency	SP8665	1.0			GHz	400mV to 1.2V p-p
	SP8666	1.1			GHz	600mV to 1.2V p-p
	SP8667	1.2			GHz	600mV to 1.2V p-p
Min. i/p frequency				200	MHz	Sine wave input 400mV p-p
Min. i/p frequency				100	MHz	Sine wave input 600mV p-p
Min. slew rate for square wave input				200	V/μsec	
Clock i/p impedance			400		Ω	At low frequency
Inhibit input reference level			−1.3		V	At 25°C compatible with ECL III throughout the temperature range.
Inhibit input pulldown resistor (internal)			6		kΩ	
Output pulldown resistor (internal)			3		kΩ	
Power supply drain current			80	105	mA	At 25°C

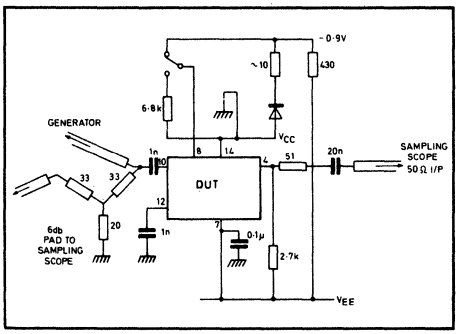


Fig. 3 Test circuit

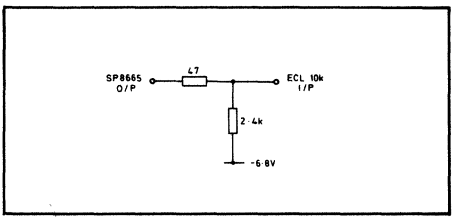


Fig. 4 SP8665 to ECL 10K

SP8685A & B

UHF PROGRAMMABLE DIVIDER 500MHz ÷ 10/11

The SP8685 A & B are high speed, programmable ÷10/11 counters operating at an input frequency of up to 500 MHz over the temperature ranges −55°C to +125°C and 0°C to +70°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either input is in the high state, and by 11 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-ten prescaler the inverse output (o/p) should be connected to a PE input.

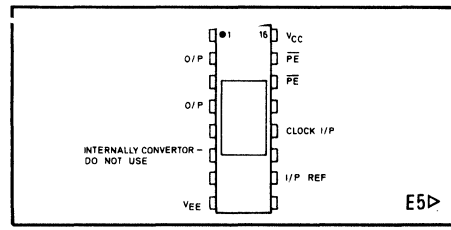


Fig. 1 Pin connections

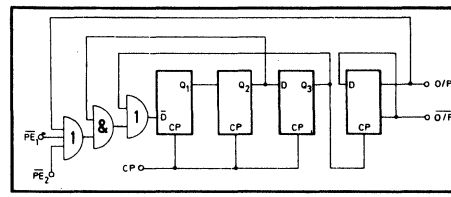


Fig. 2 Logic diagram SP8685

Clock Pulse	Q_1	Q_2	Q_3	Q_4
1	L	H	H	H
2	L	L	H	H
3	L	L	L	H
4	H	L	L	H
5	H	H	L	H
6	L	H	H	L
7	L	L	H	L
8	L	L	L	L
9	H	L	L	L
10	H	H	L	L
11	H	H	H	H

Extra state

Table 1 Count sequence

$\overline{PE_1}$	$\overline{PE_2}$	Div Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Table 2 Truth table for control inputs

FEATURES

- Full temperature range operation:
  'A' variant −55°C to +125°C
  'B' variant 0°C to +70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC} - V_{EE}$	0V to +8V
Input voltage, PE inputs	0V to V_{CC}
Input voltage, CP input	2V peak-to-peak
Output current	20mA
Operating junction temperature	+150°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

Test conditions (unless otherwise stated)

T_{amb} 'A' Type: −55°C to +125°C
'B' Type: 0°C to +70°C
Supply voltages: V_{CC} = +5.2V ±0.25V
V_{EE} = 0V
Clock input voltage: 400mV to 800mV (p-p)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Max i/p frequency	500			MHz	V_{cc} = +5.2V
Min i/p frequency			40		Sinewave Input
Min. slew rate for square wave input			100	V/μs	
Propogation delay					
(clock i/p to device o/p)		4		ns	
$\overline{PE}$ input reference level		+3.9		V	V_{cc} = +5.2V, 25°C
Power supply drain current		45	60	mA	V_{cc} = +5.2V, 25°C
$\overline{PE}$ input pulldown					
Resistors		4.3		KΩ	
Clock i/p impedance					
(i/p to i/p ref low frequency)		400		Ω	

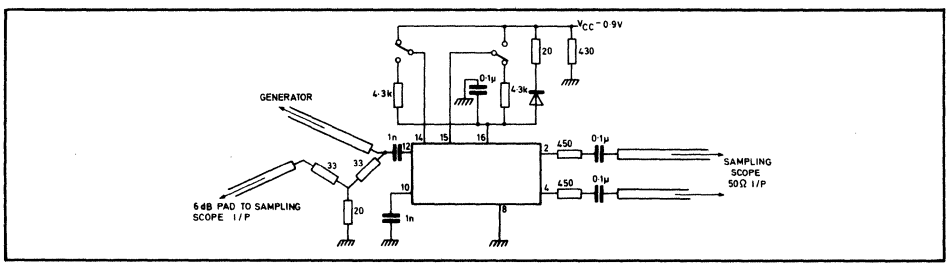


Fig. 3 Test circuit

APPLICATION NOTES

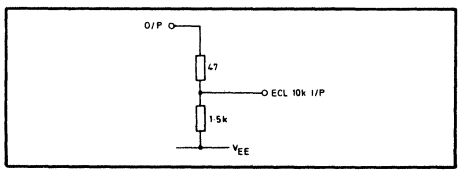


Fig. 4 SP8685 output – ECL 10K i/p and ECLII (or ECL 10K o/ps unloaded) – ECL 10K i/p

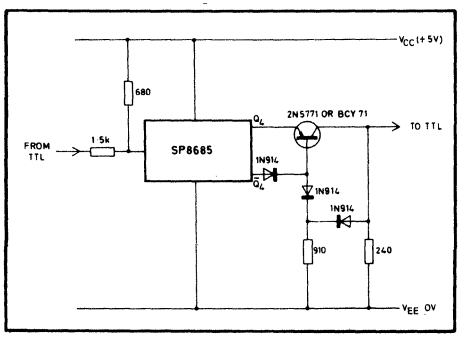


Fig. 5 TTL o/p – SP8685 $\overline{PE}$ i/p; SL8685 o/p – TTL i/p. (Total delay from SP8685 clock i/p to Schottky gate o/p = 15ns, typ.)

At an input frequency of 500 MHz the control loop delay time (SP8685 o/p to PE i/p) is approximately 16 ns. This will be a severe problem if TTL is used in the control loop.

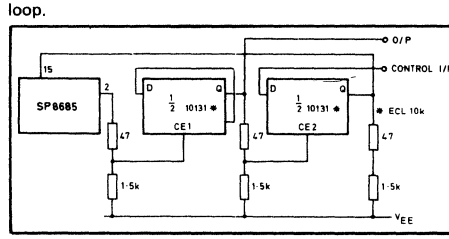


Fig. 6 Divide-by-20/22. Control loop delay time approximately 40ns.

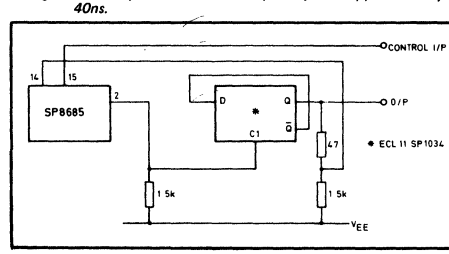


Fig. 7 Divide-by-20/21. Control loop delay time approximately 30ns using SP1034.

VHF, LOW POWER, PROGRAMMABLE DIVIDERS, ÷ 10/11
SP8690 A&B 100 MHz, ÷ 10/11

FEATURES

- Full temperature range operation
  "A" variant −55°C to +125°C
  "B" variant 0°C to +70°C
- Toggle frequency > 200MHz typical
- Power dessipation 70mW typical
- Capacitively coupled clock input for synthesiser and counter applications
- ECL compatibility on the programming inputs.
- True and inverse outputs available with ECL compatibility
- Output available for driving TTL or CMOS

GENERAL DESCRIPTION

The SP8690 A&B are divider circuits that can be logically programmed to divide by either 10 or 11.

The device is available over two temperature ranges, "A" variant is −55°C to +125°C and the "B" variant is 0°C to +70°C.

The clock inputs can be either single or differentially driven and must be a.c. coupled to the signal source. If single driven, then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present. To prevent this a 68K resistor should be connected from pins 1 or 16 to OV. This will reduce the sensitivity of the device by approximately 100MV peak to peak.

The division ratio is controlled by two PE inputs which are ECL II, 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of two resistors as shown in Figure 3. There is a free collector saturating output stage for interfacing with either TTL or CMOS together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Figure 4.

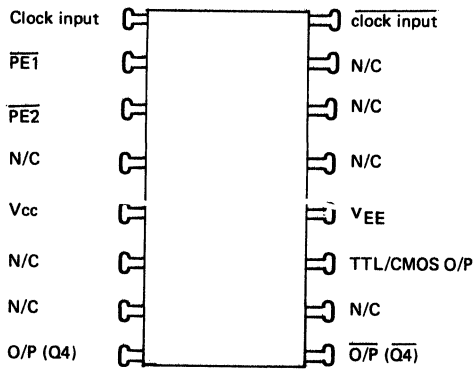
The device may be used as a fixed ÷ 10 by connecting Q4 to one PE input.

If the O→1 transition of Q4 or the 1→O transition of the $\overline{Q4}$ is used to clock the next stage, then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

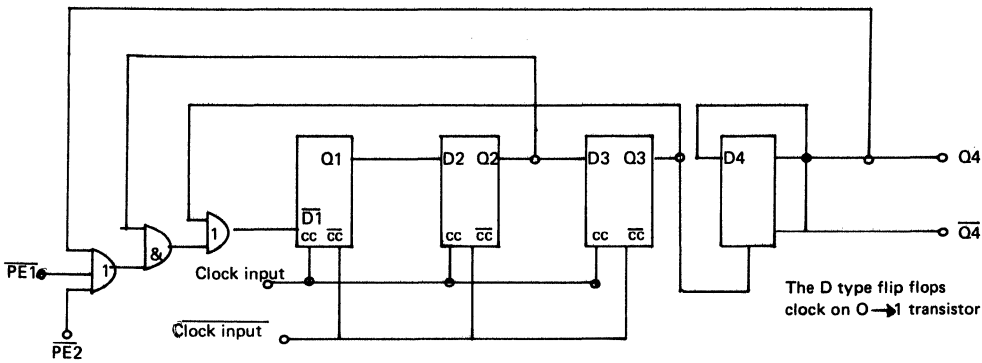
ELECTRICAL CHARACTERISTICS

CHARACTERISTIC *	TYPE	VALUE			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
Max. toggle frequency	SP8690 A&B SP8691 A&B	100	200		MHz	
Min frequency with sine wave clock input	ALL		15		MHz	
Min. slew rate of sq. wave input for correct operation	ALL		40		v/us	
$\overline{PE}$ input levels	ALL					Vcc = +5v
Vinh		+4.1		+4.5	volts	Tamb = 25°C
Vinl		0.0		+3.5	volts	(see note 1)
Q4 or $\overline{Q4}$ output voltage levels	ALL					Vcc = +5v Tamb = +25°C (see note 2) Iout (extend) = OmA
VOH		4.15			volts	(There is internal circuitry equiva
VOL			3.5		volts	lent to a 3.8K pulldown resistor or each o/p)
Max. Output Current TTL/CMOS output Voltage levels	ALL		5		mA	
VOH			0.4		volts	Sink current = 3 mA
VOL			See note 3		volts	
Input pulldown resistor between pins 2 or 3 and -ve Rail			10		KΩ	
Impedance of clock inputs			1–6		KΩ	Fin = OHz
Power supply drain current			14		mA	Tamb = +25°C

PIN CONNECTIONS – Figure 1



LOGIC DIAGRAM - Figure 2 (+ve logic)



COUNT SEQUENCE

	Q1	Q2	Q3	Q4	
1	L	H	H	H	
2	L	L	H	H	
3	L	L	L	H	
4	H	L	L	H	
5	H	H	L	H	
6	L	H	H	L	
7	L	L	H	L	
8	L	L	L	L	
9	H	L	L	L	
10	H	H	L	L	
11	H	H	H	H	←Extra Slate

Truth Table for Division Retic

$\overline{PE1}$	$\overline{PE2}$	Div. Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Note 1

The $\overline{PE}$ reference voltage level has the same temperature coefficient as ECL II and ECL 10K.

Note 2

The Q4 and $\overline{Q4}$ output levels have the same temperature coefficient as ECL II and ECL 10K.

Note 3

The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply voltage that the collecter load is taken to. This should not exceed +12V.

*Test conditions (unless stated otherwise).

Tamb

"A" variant $-55^{o}C$ to $+125^{o}C$
"B" variant $0^{o}C$ to $+70^{o}C$

Supply voltage

V_{CC} = +5v $\pm$ 0.25v
V_{EE} = OV

Clock input voltage 400 mV to 800 mV peak to peak
(Clock input decoupled to OV)

Interfaces

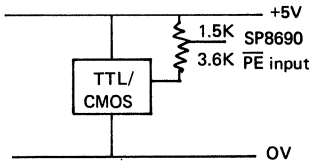


FIGURE 3

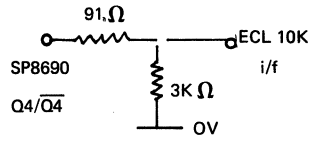
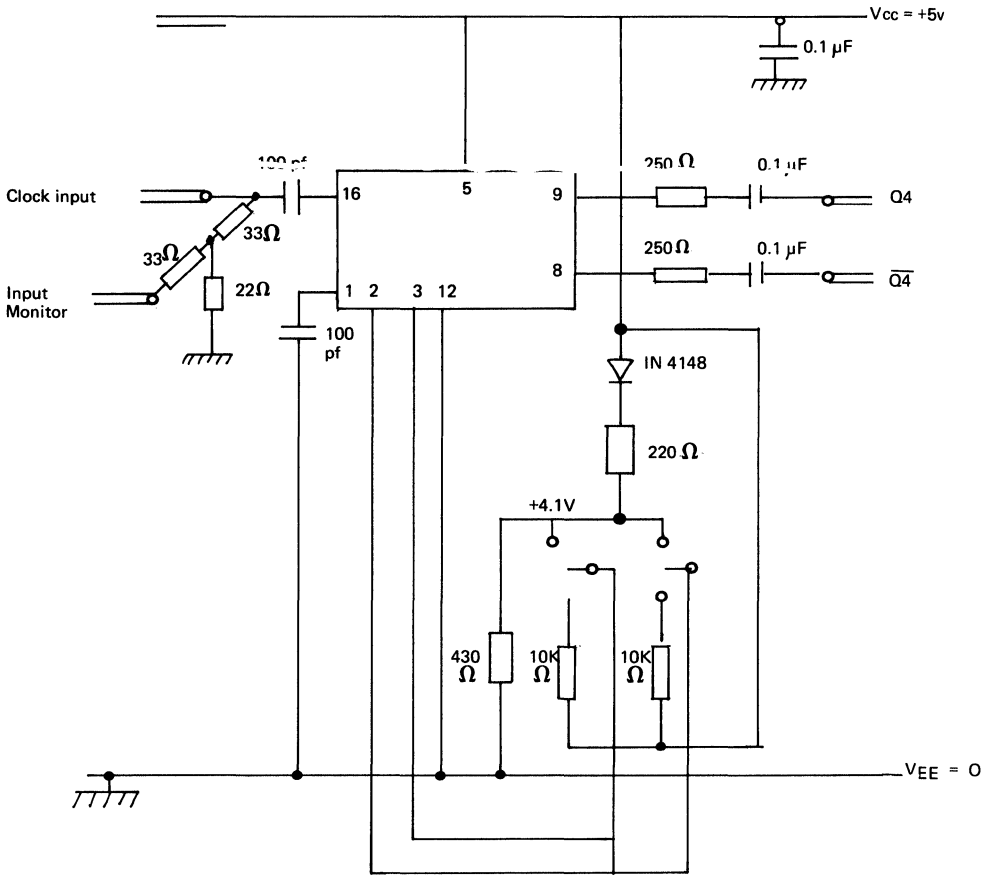


FIGURE 4

FIGURE 4



Absolute Maximum Rating

Supply voltage	Vcc – V_{EE}	8v
Input voltage	Vin d.c.	Not greater than the supply voltage in use
Output current	Iout	10mA
Maximum junctic temperature		~150°C
Storage temperature range		–55°C to +150°C

Package details

16 lead black ceramic
Thermal resistance 90°C/W

mos

PROVISIONAL DATA

MP1013A

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

The MP 1013A is a monolithic MOS/LSI integrated circuit UART subsystem using low threshold p-channel technology. Independent clocks are provided for receiver and transmitter, allowing simultaneous data reception and transmission at differing baud rates.

Transmitter data is input in parallel on the pins TD1-TD8 and output in serial form from the SO output, together with the start bit, parity bit (if required), and selected number of stop bits. The number of data bits is variable from 5 to 8, depending on the state of control input pins. Other control pins select the type of parity (or no parity if not required) and the number of stop bits. All control inputs are common to receiver and transmitter sections of the device.

Receiver data is input in serial form at SI and output in parallel at RD1-RD8. The received word is examined for correct parity and valid stop bits as selected by the control inputs. Error flag outputs indicate faults in parity and stop bits.

Double buffering of input and output data permits data to be loaded or read whilst another word is being sent or received. If a received word has not been read by the time another complete word has been received, an overrun error flag is enabled.

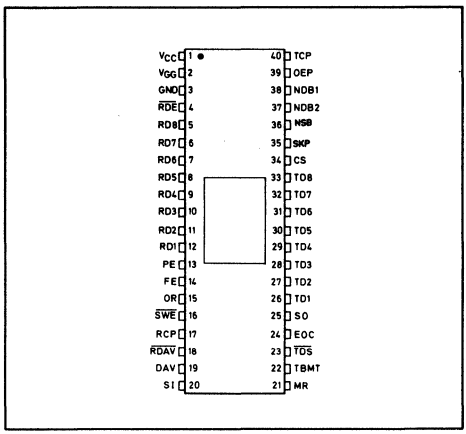


Fig.1 Pin connections

FEATURES

- Fully Programmable.
  External selection of word length (5, 6, 7 or 8 Bits), 1 or 2 stop bits, odd, even or no parity bits.
- Simple Interfacing
  Inputs and outputs fully TTL/DTL compatible
- Full or Half Duplex Operation
  Separate clocks permit transmission and reception at different baud rates simultaneously.
- Receiver Centre Sampling
  46% distortion immunity.
- Bus structure Capability
  Data outputs and status flags are tri-state
- External Reset
  Resets error flags, clears shift registers
- High Speed Operation
  40 kBaud Data Rate
- Double Buffered
  Eliminates need for external synchronisation.
- Static Circuitry
  Data stable with DC – 640 KHz clocks

APPLICATIONS

- Keyboard Interfaces
- Modems
- Data Concentrators
- Minicomputers
- Card and Tape Readers
- Data Acquisition Systems
- Asynchronous Data Cassettes
- Asynchronous Data Multiplexers

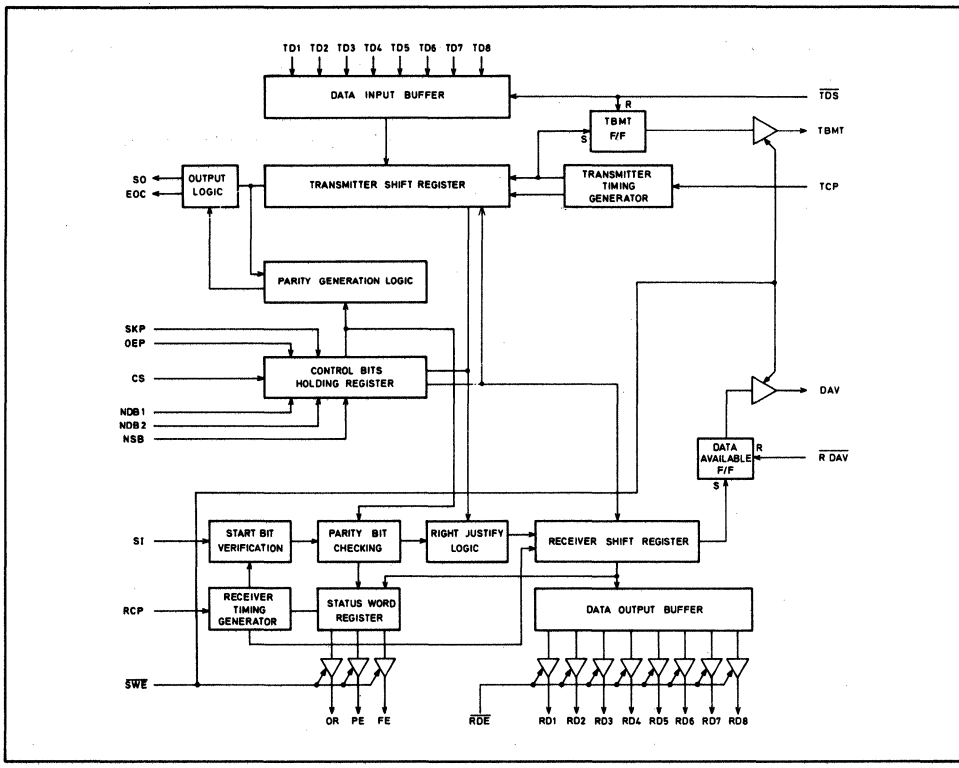


Fig.2 Functional block diagram

PIN FUNCTIONS

Pin No.	Symbol	Name	Function
1	V_{CC}	V_{CC} power supply	+5V supply
2	V_{GG}	V_{GG} power supply	−12V supply
3	GND	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	Controls the tri-state outputs RD1-RD8. A low level will place the receiver buffer register contents on RD1-RD8.
5-12	RD8-RD1	Receiver Data outputs	These 8 tri-state outputs are enabled by $\overline{RDE}$. Received characters always have the LSB on the RD1 output. If less than 8 digits are selected by NDB1 and NDB2, unused outputs are low.
13	PE	Parity Error	Tri-state output enabled by $\overline{SWE}$. Goes high if the received character parity does not agree with that selected by SKP and OEP.
14	FE	Framing Error	Tri-state output enabled by $\overline{SWE}$. Goes high if the received character has no valid stop bit.
15	OR	Overrun	Tri-state output enabled by $\overline{SWE}$. Goes high if the previous character has not been read ($\overline{RDAV}$ not strobed) before the current character is fed into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable	A low level will enable the five tri-state outputs PE, FE, OR, DAV and TBMT.

17	RCP	Receiver Clock	The receiver clock frequency must be 16 times the desired receiver baud rate.
18	$\overline{\text{RDAV}}$	Reset Data Available	A low level input resets the DAV output.
19	DAV	Data Available	Tri-state output enabled by $\overline{\text{SWE}}$. Goes high when an entire character has been transferred to the receiver buffer register.
20	SI	Receiver Serial Input	Accepts the serial input data stream. A high-to-low level (mark-to-space) transition will initiate data reception.
21	MR	Master Reset.	Should be pulsed high after power turnon. Sets SO, EOC and TBMT high, PE, FE, OR and DAV low. Clears input data buffers and resets shift registers.
22	TBMT	Transmitter Buffer Empty	Tri-state output enabled by $\overline{\text{SWE}}$. Goes high when the transmitter buffer may be loaded with a new character.
23	$\overline{\text{TDS}}$	Transmitter Data Strobe.	A low level strobe which enters the data bits into the holding register. Transmission is initiated on the rising edge of $\overline{\text{TDS}}$.
24	EOC	End of Character	Goes high whenever a complete character is transmitted, remains high until the start of the next character. In continuous transmission goes high for ½ TCP period only.
25	SO	Serial Output	Serially outputs the transmitted data. At a high level when no data is being transmitted.
26-33	TD1-TD8	Transmitter Data Inputs	The eight data input lines are strobed by $\overline{\text{TDS}}$. The LSB should always be placed on TD1. Unused data lines as selected by NDB1 and NDB2 may be in either logic state.
34	CS	Control Strobe	A high level strobe enters the control bits (NDB1, NDB2, NSB, SKP, OEP) into the holding register. May be hard-wired high if the control bits are constant.
35	SKP	Skip parity bit	A high level signal prevents the parity bit from being transmitted, i.e. the stop bit follows the last data bit. The receiver will look for the stop bit after the last data bit, and PE is forced to a low level.
36	NSB	Number of Stop Bits	This pin fixes the number of stop bits which are sent by the transmitter or detected by the receiver. A high level gives two stop bits, and a low level one.
37-38	NDB1 NDB2	Number of Data Bits per character	These two pins select the number of data bits to be sent or received, as shown below:
39	OEP	Odd/Even Parity	The signal on this pin determines the type of parity which will be sent by the transmitter or checked by the receiver. A high level represents even parity and a low level odd parity.
40	TCP	Transmitter Clock Pulse	The transmitter clock frequency must be 16 times the desired transmitter baud rate.

NDB1	NDB2	Bits/character
L	L	5
H	L	6
L	H	7
H	H	8

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

V_{GG} = −12V ± 5%, V_{cc} = +5V ± 5%, T_A = 0°C to +70°C

All voltages are measured w.r.t. ground

Positive current is defined as that flowing into the pin under consideration.

DC Characteristics

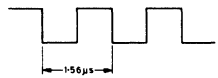
Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input voltage levels					
Low level, V_{IL}	V_{DD}		0.8	V	I_{IL} = −1.6mA
High level, V_{IH}	V_{cc}−1.5		V_{cc} +0.3	V	(Internal pull up resistor)
Output voltage levels					
Low level, V_{OL}			0.4	V	I_{OL} = 1.6mA, V_{cc} = Max.
High level, V_{OH}	V_{cc}−1			V	I_{OH} = -300μA
Output current					
Leakage, I_{OT} (tri-state outputs)			−1	μA	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}
Shortcircuit, I_{OS}	2.5			mA	V_{out} = OV (Note 1)
Power supply current					
I_{CC}		16		mA	T_A = +25°C
I_{DD}		20		mA	T_A = +25°C

AC Characteristics

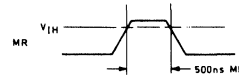
Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Clock frequency	DC		640	kHz	TCP, RCP
Baud rate			40	K baud	
Pulse widths, t_{pw}					
Clock (TCP, RCP)	780			ns	See Fig.. 3(a)
Reset (MR)	500			ns	See Fig. 3(b)
Control strobe (CS)	300			ns	See Fig. 3(c)
Data strobe ($\overline{TDS}$)	200			ns	See Fig. 3(d)
Tri-state O/P enables ($\overline{SWE}$, $\overline{RWE}$)	500			ns	See Fig. 3(e)
Data Available Reset ($\overline{RDAV}$)	250			ns	See Fig. 3(f)
Setup and hold times					
Data inputs	0			ns	See Fig. 3(d)
Control inputs	0			ns	See Fig. 3(c)
Propagation delays $t_{pd}1$ and $t_{pd}0$					
Tri-state output enables to outputs			500	ns	See Fig. 3(f)
Input capacitance C_{in} (all inputs)			20	pF	Bias = 0V, f = 1MHz
Output capacitance C_o (all outputs)		10	15	pF	$\overline{SWE}$ = $\overline{RDE}$ = V_{IH}

NOTES

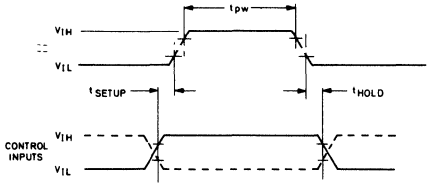
1. Not more than one output should be shorted at a time.
2. If the transmitter is inactive (TEOC = TBMT = V_{OH}) the start bit will appear on the SO line within one transmitter clock period of the trailing edge of $\overline{TDS}$
3. The start bit will always be detected within one receiver clock period. This will guarantee a maximum slippage of the start bit of one-sixteenth of a bit time.



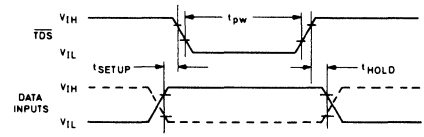
(a) *Clock pulse. TCP or RCP at maximum clock frequency (640 kHz). At lower data rate, minimum positive or negative pulse width is 780 ns.*



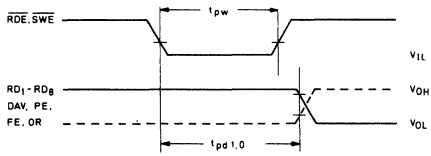
(b) *Reset pulse*



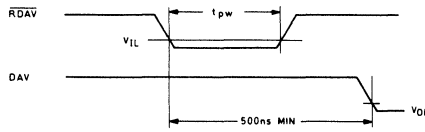
(c) *Control strobe. Control input information need only be valid during the last t_{pw} (min) of the control strobe.*



(d) *Data strobe. Data need only be valid during the last t_{pw} (min.) of the input strobes.*



(e) *Tri-state outputs, t_{pw} (min.) is the shortest pulse required to present valid data on the outputs.*



(f) *Data available reset.*

Fig.3 Timing diagrams

TRANSMITTER OPERATION

After the power has been turned on and the clock (at a frequency of 16X the desired baud rate) is applied , the Master Reset pin is pulsed, which sets TBMT, EOC and SO high.

When EOC and TBMT are high the control and data bits may be set up. It is normal procedure to strobe in the control bits prior to the data, but, if minimum pulse width specifications are observed, $\overline{TDS}$ and CS may occur simultaneously. TBMT goes low on the positive edge of $\overline{TDS}$, indicating that the buffer is full and not available to receive new data.

If, as in the case after reset, the transmitter shift register is empty, the buffer is read into this register within one clock cycle of the data strobe and data transmission commences. SO goes low (start bit), EOC goes low and TBMT goes high to indicate that a fresh character may now be loaded.

If new data is now loaded, TBMT will stay low until the current word has been completely read out, when EOC will go high for half a clock cycle, as the new data is immediately transferred from the buffer to the main register and transmission of the new word commenced.

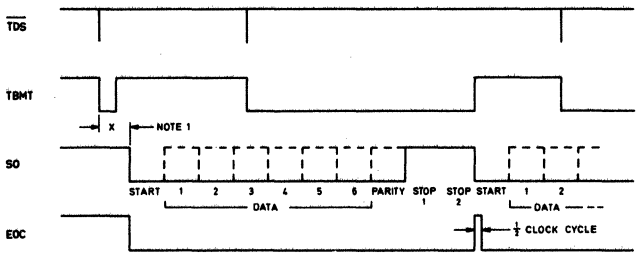
The order of transmission of data is start bit – selected number of data bits – parity bit (if required) and stop bit(s). When the last stop bit has been on the line for one bit-time, EOC goes high, and, providing TBMT is high, new control bits may be loaded.

RECEIVER OPERATION

After the power has been turned on and the 16X baud rate clock applied, the Master Reset pin is pulsed, which sets PE, FE, OR and DAV low. The control bits are common with the transmitter, and may now be set.

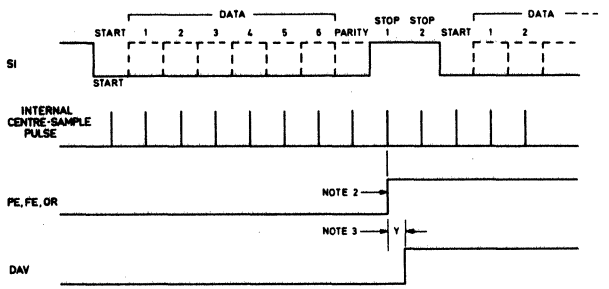
Data reception is initiated when the serial input changes from mark to space (high to low). Centre sampling of the start bit is then carried out. If the start bit is verified (by SI still being low at the centre sample point), reception of the data on SI proceeds.

The error flags PE, FE and OR go high, if errors are detected, after the centre sample pulse of the first stop-bit. DAV goes high after one more clock cycle to indicate that the received data may now be read out. It should be noted that DAV must be reset when the data is read out, otherwise an overrun will be detected after the next word is read in. A full character time is available to read out data due to the double buffering of the outputs.



NOTES
1. If transmitter inactive, interval X is less than one TCP cycle.
2. Code shown is 6 level, with parity and two stop bits.
3. Double buffering permits the strobing in of new data at any time during the transmission of character 1.

Fig.4 Transmitter timing



NOTES
1. Code shown is 6 level, with parity and two stop bits.
2. If an error condition is detected, this is the point at which the error outputs go high.
3. Time Y is a maximum of one receiver clock cycle.
4. Data may be read at any time until DAV tries to set for the next clock cycle.

Fig.5 Receiver timing

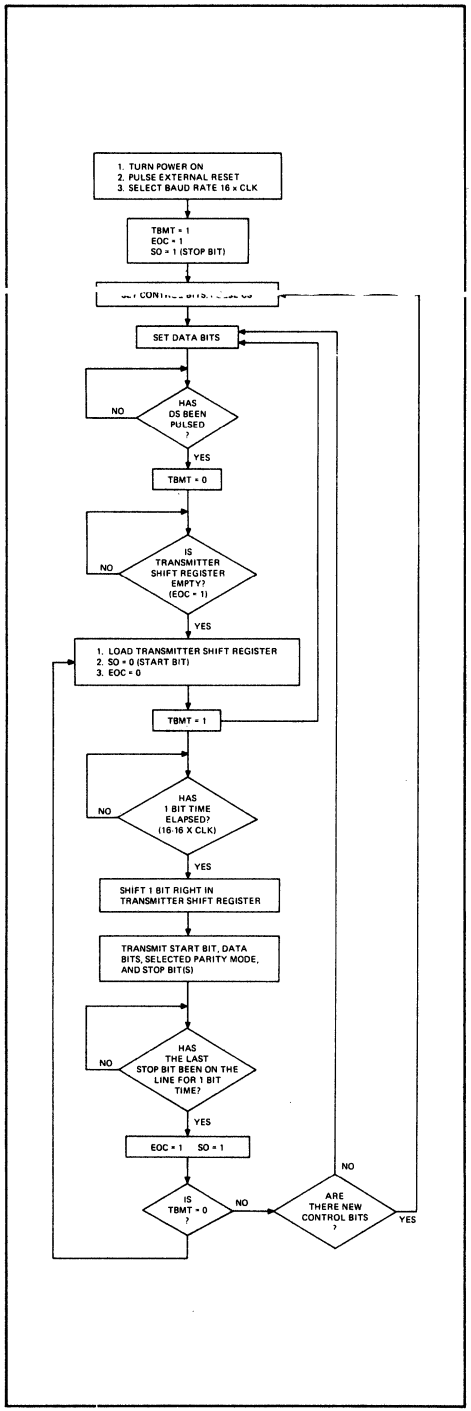


Fig.6 Transmitter flow chart

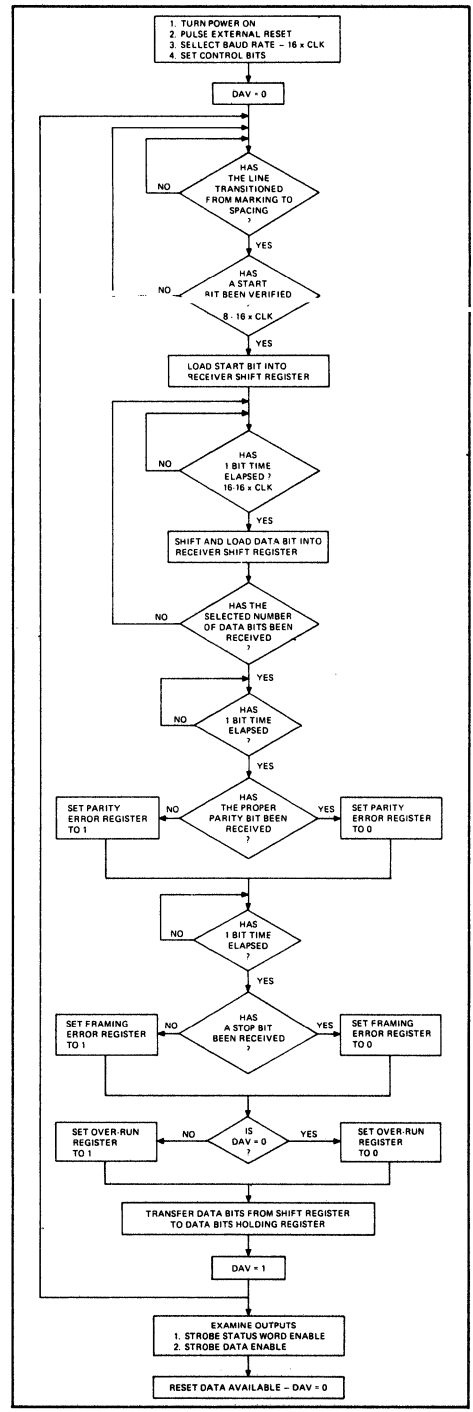


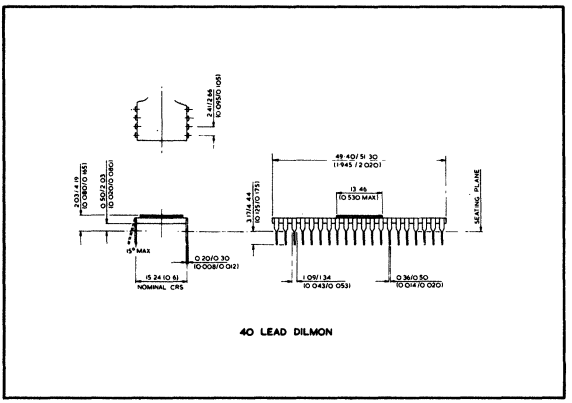
Fig.7 Receiver flow chart

ABSOLUTE MAXIMUM RATINGS

Operating temperature range 0°C to 70°C
Storage temperature range −55°C to +125°C
Lead Temperature (soldering, 10 secs max.) 330°C
Negative voltage on any pin (with respect to V_{cc}) −25V
Positive voltage on any pin (with respect to V_{cc}) +0.3V

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



40 LEAD DILMON

Publication No. P.S. 1446 March 1975

PROVISIONAL DATA

MP3409B

QUAD 80-BIT DYNAMIC SHIFT REGISTER

MP3417B

QUAD 64-BIT DYNAMIC SHIFT REGISTER

The MP3409B and MP3417B are p-channel MOS quad 80-bit (MP3409B) and 64-bit (MP3417B) dynamic shift registers.

The four registers have individually controlled logic for recirculating data in each register. A single clock generator provides two clock phases to all 4 registers. The Clock input, Recirculate Enable and Data inputs are all TTL compatible, and each output interfaces directly with TTL without the use of external circuitry.

The low threshold thick oxide MOS p-channel enhancement mode circuitry has been used to reduce power dissipation and permit easy interfacing between bipolar circuits.

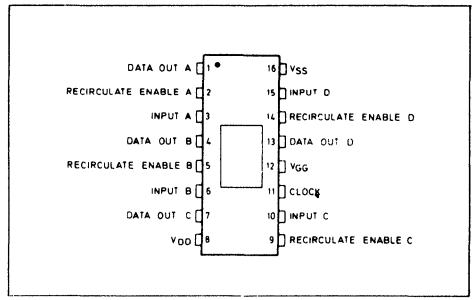


Fig. 1 Pin connections

FEATURES

- 3 MHz Shift Rate
- Logic Recirculation
- +5V, OV, -12V Power Supplies
- TTL Compatible Inputs & Outputs
- Single Clock (TTL Compatible)
- Low Power Dissipation -300 mW
- Low Threshold P-channel Technology
- Dual-in-line Packages

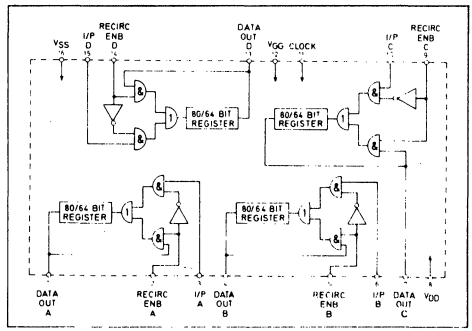


Fig. 2 Functional block diagram

APPLICATIONS

- Sequential Access Memories
- CRT Alpha-Numeric Displays
- CRT Refresh Memories
- Buffer Memories

ABSOLUTE MAXIMUM RATINGS

Operating temperature Range ..... -25°C to +85°C
Storage temperature Range ..... -55°C to +150°C
Negative voltage on any pin (with respect to V_{SS}) .-20V
Positive voltage on any pin (with respect to V_{SS}) .+0.3V
Lead temperature (soldering, 10 secs max.) .....330°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the electrical characteristics below apply for any combination of the following characteristics:

V_{SS} = +5.0V ± 5%
V_{GG} = -12.0V ± 5%
V_{DD} = 0V
Temperature range -25°C to +85°C
Maximum power dissipation = 300mW

All voltages are measured with respect to ground. Positive current is defined as flowing into the pin under consideration.

DC Characteristics

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Input voltage levels					
Low level, V_{IL}	V_{DD}		+0.8	V	I_{IL} = -1.6mA
High level, V_{IH}	V_{SS} -1.3		V_{SS}	V	
Clock low level, $V_{\phi L}$	V_{DD}		+0.4	V	
Clock high level, $V_{\phi H}$	V_{SS} -1.3		V_{SS}	V	
Output voltage levels					
Low level, V_{OL}	V_{DD}	+0.3	+0.4	V	I_{sink} = +1.6mA
High level, V_{OH}	V_{SS} -1.0	V_{SS} -0.5	V_{SS}	V	I_{load} = -0.5mA
Input current					
Inputs, I_{IL}			100	nA	V_{in} = OV
Clocks, $I_{\phi L}$			100	nA	V_{ϕ} = OV
Power supply current					
Substrate supply, I_{SS}			35	mA	f = 1MHz
Gate supply, I_{GG}		10	25	mA	f = 1MHz

AC Characteristics

Characteristic	Value			Units	Condition
	Min.	Typ.	Max.		
Clock frequency	0.01		3	MHz	
Data frequency	DC		3	MHz	
Output logic transitions					
Rise time t_r		40	60	ns	TTL load + 10pF
Fall time t_f		30	50	ns	TTL load + 10pF
Output propagation delay					
Low-to-high level O/P t_{OH}		70	100	ns	TTL load + 10pF
High-to-low level O/P t_{OL}		70	100	ns	TTL load + 10pF
Pulse timing (input)					
Clock pulse transition, $t_{r\phi}$, $t_{f\phi}$		10	100	ns	
Clock pulse width high, $PW_{\phi H}$	0·125		50	μs	
Clock pulse width low, $PW_{\phi L}$	0·175		50	μs	
$PW_{\phi H} \div PW_{\phi L}$	0.02		50	ns	
Pulse spacing (input)					
Data setup, t_{DS}	100			ns	
Data hold, t_{DH}	100			ns	
Recirculate Enable setup, t_{RS}	200			ns	
Recirculate Enable hold, t_{RH}	100			ns	
Input capacitance					
Inputs (Data + Recirc. Enb.), C_{in}			10	pF	V_{in} = V_{SS} f = 1MHz
Clocks, C_{ϕ}			10	pF	V_{ϕ} = V_{SS} f = 1MHz

OPERATION

Data is transferred into the register when the internal clock ϕ_1 is on. This clock is on when the external clock is high, but the changes of level occur some 100 ns after the external drive. Data must be held true at least 100 ns after the external clock drive has changed state, for data to be entered.

The true output data becomes available about 100 ns after the TTL clock goes low.

During the recirculate mode, information in the register continues to be read out.

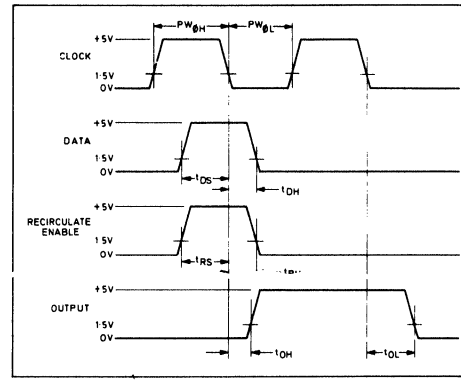
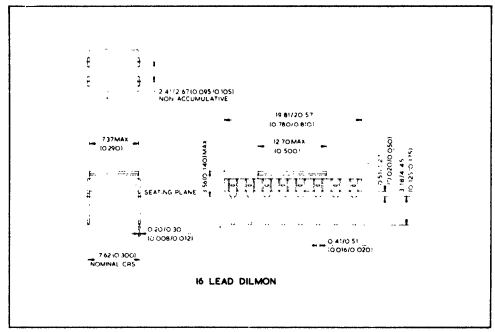


Fig. 3 Timing diagram and voltage wave forms

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



PLESSEY
SEMICONDUCTORS

MOS CIRCUITS

NEW PRODUCT DATA

MP9100

PUSH BUTTON TELEPHONE DIALLER

The MP9100 is a p-channel low threshold MOS integrated circuit containing the logic required to interface between a keyboard and a Strowger-type telephone system.

Up to 20 digits and 'dial tone waits' can be stored — dialled directly or re-dialled.

The use of 4-phase dynamic logic minimises power consumption, thus allowing line-powered or battery operation.

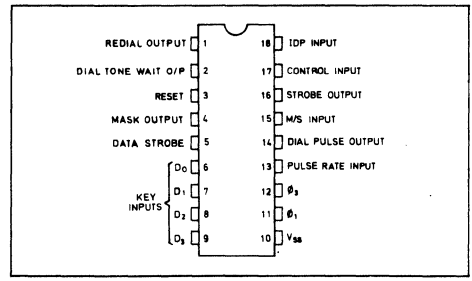


Fig. 1 Pin connections (top)

FEATURES

- 20 Digit Capability
- Low Power Consumption
- Re-dialling Facility
- Direct Interface With Standard MF Keyboard
- Can Be Used With MP9200 To Form A Repertory Dialling System
- Dial Tone Wait Facility
- Programmable Dialling Speed, Dial Pulse Mark/Space Ratio, and Inter-Digit Pause

QUICK REFERENCE DATA

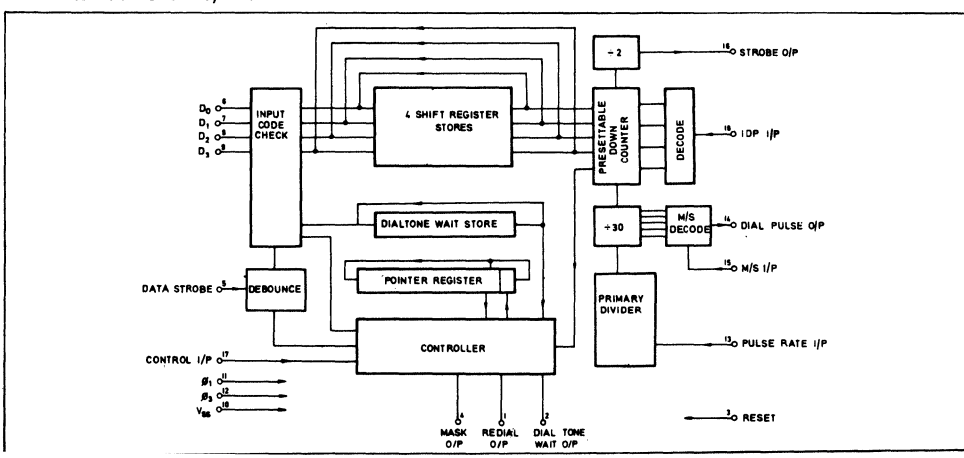
- Clock Levels: −15 ± 2V (2Ø, 25% Duty Cycle)
- Clock Rate: 18 kHz (Nominal)
- Free Drain Output Current: 1 mA (Min.)
- Power Consumption: 2 mW (Max.)

APPLICATIONS

- Telephones (Mains, Battery or Line-power)
- Repertory Diallers
- Automatic Security Alarms

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin w.r.t. V_{SS}: +0.3V to −20V
Storage temperature: −55°C to +125°C
Ambient operating temperature: −55°C to +80°C



ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = −55°C to +80°C
Clock frequency = 18 kHz
V_{SS} = 0V
Negative logic convention used

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Inputs					
Logic '0' level	+0.3		−1	V	
Logic '1' level	−4		−17	V	
Data strobe pulse width	10			ms	
Reset pulse width	3			ms	After clocks reach full amplitude
Clocks					
Logic '0' level	+0.3		−1	V	Clocks must be matched
Logic '1' level	−13	−15	−17	V	to within 0.2V
Frequency	10	18	30	kHz	
Edge time (t_d)	0.1		4	μs	
Width (t_w)	5		40	μs	See Fig. 3
Separation (t_s)	5		40	μs	
Capacitance		90	150	pF	Per clock phase
Leakage			30	μA	T_{amb} = 80°C, V_ϕ = −17V
Outputs					
Logic '0' current	1			mA	V_{out} = −1V
Logic '1' current			10	μA	V_{out} = −10V
Power consumption		0.9	2	mW	

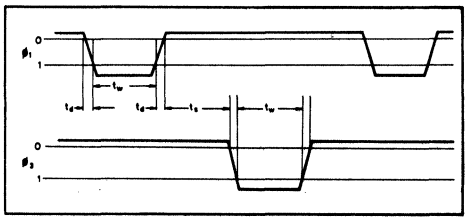


Fig. 3 Clock waveforms

OPERATING NOTES (See Fig. 2)

Keyboard Entry and Dialling Out

The MP9100 must be reset at power-on in order to clear the stores and reset all bistables. This is achieved by applying a logic '0' at the RESET pin for at least 3 ms after the clocks have reached full amplitude. Numbers may then be entered from a keyboard by applying the appropriate 4-bit code to the input pins $D_0 - D_3$ (according to the code given in Table 1) and applying a logic '0' pulse to INPUT DATA STROBE. This strobe input must be stable for at least 10 ms, otherwise it will be rejected by the anti-bounce circuitry. After the required time has elapsed, the 4-bit code is read into the recirculating stores, invalid codes being ignored.

DIGIT	D_0	D_1	D_2	D_3
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	0	1	1	1
8	0	1	1	0
9	0	1	0	1
0	1	1	0	0
DIAL TONE WAIT	0	0	1	1

Table 1 Keyboard input coding

Up to 20 digits may be entered, the control logic ensuring that each digit is placed sequentially in the store. In addition, DIAL TONE WAIT inputs can be entered between digits, being one of the valid keyboard codes but read into a separate store.

As soon as the first digit is entered, the MASK OUTPUT will go to logic '0', allowing external circuitry to mask the handset. An interdigit pause is then counted out, followed by the DIAL PULSE output going to logic '0' to produce a loop disconnect signal for the duration of the mark period of the programmed mark/space ratio (see Table 2). This is then repeated a number of times, corresponding to the value of the digit. Further digits may be entered at any time; the control logic aligns a pointer to indicate the next digit in the store to be dialled out, thus ensuring complete intput/output asynchronism.

If a DIAL TONE WAIT has been entered in the number sequence, the MASK OUTPUT will go to logic '1' and the DIAL TONE WAIT O/P will go to '0' as soon as the preceding digit has been dialled. DIAL TONE WAIT must, through external circuitry, cause the CONTROL INPUT to go to logic '1' to stop further dialling. When a dial tone has been detected, the CONTROL INPUT should be taken to logic '0': the remaining digits will then be dialled out (see Fig. 4).

FUNCTION	VALUE	REQUIRED INPUT
Pulse rate	600 i.p.s. 20 i.p.s. 10 i.p.s.	ϕ_1 ϕ_3 V_{SS}
Mark/Space	70:30 $66\frac{2}{3}:33\frac{1}{3}$ 60:40 50:50	ϕ_1 V_{SS} V_{DD}* ϕ_3
Interdigit Pause (at 10 i.p.s.)	400 ms 800 ms 1000 ms	ϕ_2 V_{SS} ϕ_1

* V_{DD} is negative supply for external circuitry.

Table 2 Programmable input coding (at 18 kHz clock frequency)

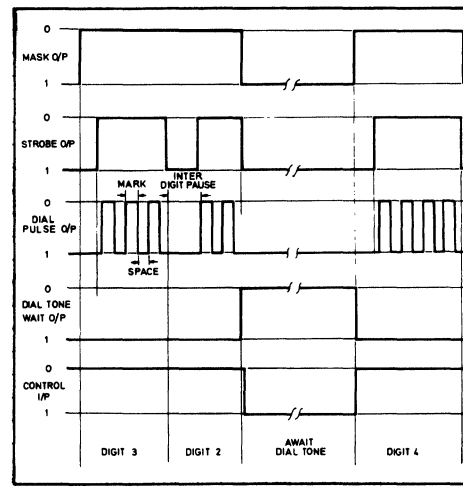


Fig. 4 Waveforms

Redial Mode

If the CONTROL INPUT is taken to logic '1' together with a DATA STROBE pulse, the circuit will lock into the redial mode of operation, causing the REDIAL OUTPUT to go to logic '0'. The same signals must be removed and re-applied in order to revert to normal operation.

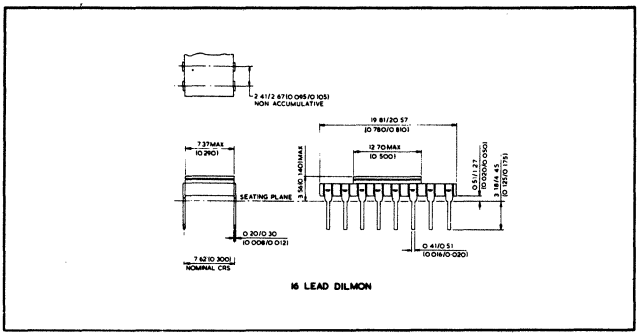
Putting the circuit into redial mode while a number is being dialled out will cause dialling to cease after the current digit. When normal mode is restored, the remaining digits will be dialled out.

If redial mode is entered before any digits have been keyed, digits will be accepted into the store but will not be dialled out until normal operation is restored.

Finally, if redial mode is entered and then removed after a complete dialling sequence, the whole sequence will be repeated.

PACKAGE DETAILS

Dimensions are shown thus: mm (in.)



16 LEAD DILMON

Publication No. P.S. 1424 December 1974

PLESSEY
SEMICONDUCTORS

MOS CIRCUITS

NEW PRODUCT DATA

MP9200

REPERTORY TELEPHONE STORE

The MP9200 is a p-channel low threshold MOS integrated circuit containing the logic and storage capability to form a self-contained repertory telephone number store of up to ten 22-digit numbers.

The use of 4-phase dynamic logic minimises power consumption, thus allowing stand-by battery operation.

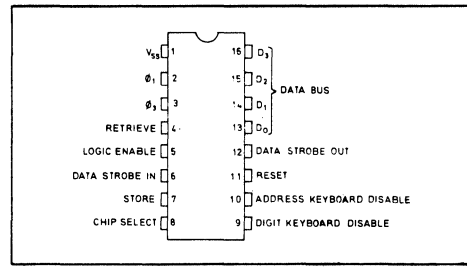


Fig. 1 Pin connections (top)

FEATURES

- Stores 10 Numbers Of Up To 22 Digits
- Low Power Consumption (5 mW Typ.)
- Can Be Used With MP9100 To Form A Repertory Dialling System
- Output Format Suitable For MF Signalling Systems
- Can Be Cascaded For Increased Storage
- Interfaces With Standard Keyboards

APPLICATIONS

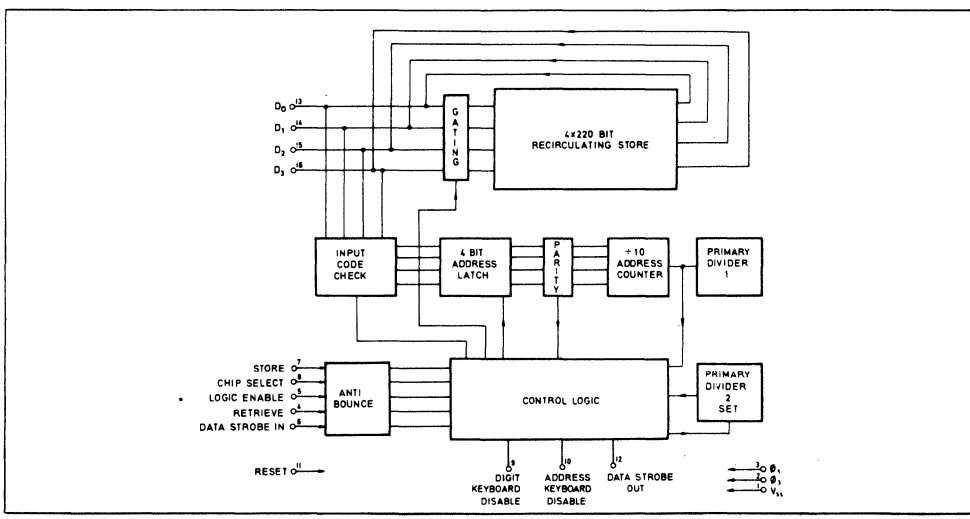
- Domestic And Business Repertory Telephone Diallers
- General Purpose Numeric Code Storage

QUICK REFERENCE DATA

- Clock Levels: $-15V \pm 2V$ (2Ø, 25% Duty Cycle)
- Clock Rate: 18 kHz (Nominal)
- Free Drain output current: 1 mA (Min.)
- Power Consumption: 10 mW (Max.)

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin w.r.t. V_{SS}: +0.3V to −20V
Storage temperature: −55°C to +125°C
Ambient operating temperature: −55°C to +80°C



ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = −55°C to +80°C
Clock frequency: 18 kHz
V_{SS} = 0V
Negative logic convention used

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Inputs					
Logic '0' level	+0.3		−1	V	
Logic '1' level	−4		−17	V	
Key depression time	40			ms	
Reset pulse width	5			ms	After clocks reach full amplitude
Clocks					
Logic '0' level	+0.3		−1	V	Clocks must be matched
Logic '1' level	−13	−15	−17	V	to within 0.2V
Frequency	10	18	30	kHz	
Edge time (t_d)	0.2		8	μs	
Width (t_w)	5		40	μs	See Fig. 3
Separation (t_s)	5		40	μs	
Capacitance			500	pF	Per clock phase
Leakage			50	μA	T_{amb} = 80°C, V_ϕ = −17V
Outputs					
Logic '0' current	1			mA	V_{out} = −1V
Logic '1' leakage			10	μA	V_{out} = −10V
Power consumption		5	10	mW	

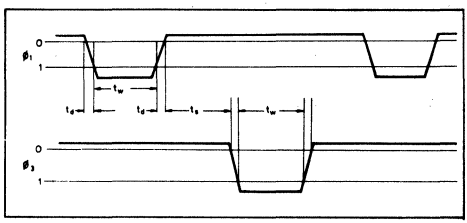


Fig. 3 Clock waveforms

OPERATING NOTES (see Fig. 2)

The MP9200 must be reset at initial power-on in order to clear the counters and reset all bistables. This is achieved by applying a logic '0' at the RESET pin for at least 5 ms after the clocks reach full amplitude.

Address information and input/output data are fed through a 4-bit bus $D_0 - D_3$. The control logic, together with disabling output signals ensure that there is no confliction of data.

Store Mode

STORE input must be held at logic '1' for the duration of the store operation. CHIP SELECT and LOGIC ENABLE must also be held at logic '1', the latter ensuring that data output strobes are inhibited. The appropriate address code (see Table 1) is applied to the 4-bit data bus and a logic '0' pulse applied to the DATA STROBE IN. This pulse must be stable for at least 40 ms. The address code, if valid, is then read into an address latch. The ADDRESS KEYBOARD DISABLE output will go to logic '0' and thus, via external circuitry, prevent further address inputs. At the same time, the addressed store location is cleared.

Up to 22 4-bit numbers (i.e. digits and 'dial tone waits') may now be successively entered into the opened store location via the data bus, each digit having a corresponding DATA STROBE IN pulse. When the number sequence has been completed, the STORE, LOGIC ENABLE and CHIP SELECT inputs may be removed.

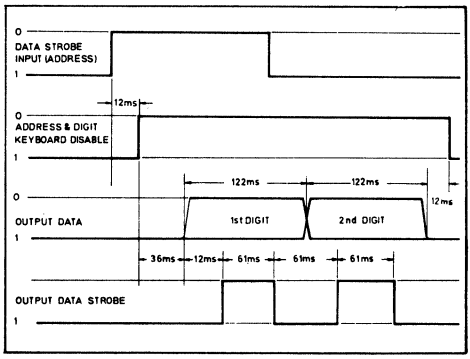


Fig. 4 Output timing Note: times specified are minimum.

ADDRESS	D_0	D_1	D_2	D_3
1	1	1	1	1
2	1	1	1	0
3	1	1	0	1
4	1	0	1	1
5	1	0	1	0
6	1	0	0	1
7	0	1	1	1
8	0	1	1	0
9	0	1	0	1
10	1	1	0	0

Table 1 Address coding

Retrieve Mode

LOGIC ENABLE must be at logic '1' for the duration of the 'retrieve' operation. The RETRIEVE and CHIP SELECT inputs must both be at a stable logic '1' for a minimum of 40 ms to ensure that the circuit is locked in the retrieve mode. These inputs may then be removed if required.

The appropriate address code is then applied to the data bus, together with a logic '0' DATA STROBE IN pulse of at least 40 ms duration. The valid code is latched in the same manner as in the 'store' operation and both the DIGIT KEYBOARD DISABLE and ADDRESS KEYBOARD DISABLE outputs will go to logic '0'.

The circuit will then sequentially output the contents of the addressed store location on the data bus, together with a DATA STROBE OUT pulse for each new digit (see Fig. 4). The data and strobe pulse durations are suitable for direct interfacing with the Push Button Dialler circuit MP9100, or with an MF Tone Generator.

At the end of the data transfer, the digit and address keyboards are again enabled.

Erase Mode

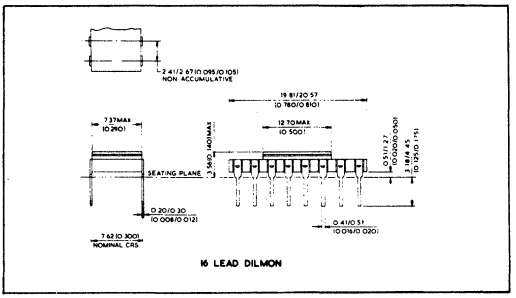
Although it is not necessary to erase an old number before storing a new one in the same location, it can be achieved simply by performing a 'store' operation in the particular address but entering no digits.

Extended Storage

The storage capacity of any system can be increased in multiples of 10 numbers by using several MP9200 circuits in parallel, using the individual CHIP SELECT to address each store.

PACKAGE DETAILS

Dimensions are shown thus: mm (in.)



mnos

Non-volatile memory elements

NEW PRODUCT DATA

NOM 201C NOM 202C NOM 204C

SINGLE MNOS TRANSISTOR DUAL MNOS TRANSISTOR QUAD MNOS TRANSISTOR

Plessey NOM 200C series Metal Nitride Oxide Silicon (MNOS) field effect transistors are specially designed for use in *non-volatile* data storage applications. The series comprises single, dual and quad groupings of the same basic MNOST, and replaces NOM100 series devices.

The significant difference between the MNOS transistor and the conventional insulated gate FET is that the MNOST is fabricated with a sandwich gate dielectric which can retain an injected positive or negative charge for periods of up to several years. This extremely long retention time is due to the fact that the charge is held deep within the dielectric and is not affected by surface leakage. The presence of the stored charge modifies the transistor gate threshold voltage V_T to either a low negative level or a high negative level.

The low V_T state is defined as the logic 'O' or erased state; conversely, the high V_T state is defined as logic '1'. Writing/Erasing (charge injection) is accomplished by applying a gate voltage pulse with an amplitude considerably greater than the range of V_T values. For example a +40V pulse will inject a negative charge which shifts V_T to the erased level; conversely, the application of a −40V pulse shifts V_T in the negative direction to its high (or logic '1') level.

The two states can be readily detected by the subsequent applications of a 'read' gate voltage lying between the two values of V_T: an MNOST with V_T set low is turned on, whereas one with V_T set high remains off. An MNOST therefore provides a one-bit memory element.

The physical mechanisms by which charge injection and reading are achieved are essentially non-destructive. An MNOST memory can be read an indefinite number of times, while the number of Write/Erase cycles that can be repeated without degradation of performance is conservatively rated at 10 million.

FEATURES

- Data Retention Without Power Supplies
- Total Electrical Control
- Non-Destructive Reading Ensures High Memory Integrity
- Guaranteed Useful Life of 10 Million Write/Erase Cycles

APPLICATIONS

Any situation requiring the storage of small quantities of data, where the retention of data is to be independent of power supplies, indicates an application for MNOS transistors. For example:

- Alternative for Latching Relays
- Storage of Running Totals in Cash Registers
- Numerical Control Parameter Storage
- Storing Aircraft and Weapons Systems Mission Data
- Storing Digital Set Point Information for Control Loops

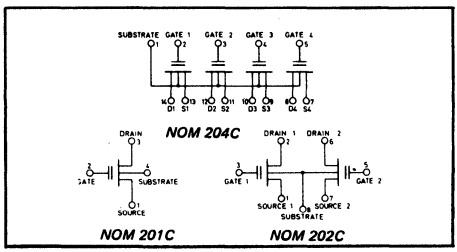


Fig.1 Transistor configurations

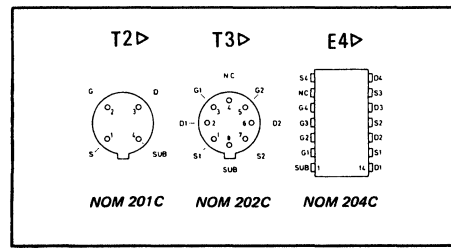


Fig.2 Pin connections (viewed from beneath)

QUICK REFERENCE DATA

- Recommended Minimum Erase Pulse: +35V for 100μs
- Recommended Minimum Write Pulse: −35V for 100μs
- Max. Recommended Erase/Write Pulse Amplitude: ± 40V
- Recommended Read Pulse Amplitude: −6V Gate/Source Voltage.
- Output Current: 0.25mA Min. Drain Current for Erased Condition, −6V Read Voltage and 5V Min. Source/Drain Voltage.
- Minimum Data Retention Time: 1 Year

ELECTRICAL CHARACTERISTICS (TYPE C DEVICES)

Test Conditions

Ambient temperature + 25°C.

Threshold voltage V_T set with voltage pulse applied between gate and substrate.

Unless otherwise stated, threshold voltages are measured 1 sec. after the setting pulse, using source/drain voltage = 1V and source/drain current = 25μA.

Characteristics	Symbol	Value				Conditions
		Min.	Typ.	Max.	Units	
Threshold voltage (Fig.3)						
High state	V_{TH}	13	14		− V	V_{TH} set by −40V, 1 sec. gate pulse
		9	11		− V	V_{TH} set by −35V, 100μs gate pulse
Low state	V_{TL}	1.5	2.5	3.5	− V	V_{TL} set by +40V, 1 sec. gate pulse
		1.4	2.5	3.6	− V	V_{TL} set by +35V, 100μs gate pulse
Threshold voltage decay (Fig.5)						
High state	$\frac{dV_{TH}}{dt}$		0.6		V/time decade	V_{TH} set with −40V, 1 sec, and stored with zero gate/substrate voltage.
Low state	$\frac{dV_{TL}}{dt}$					V_{TL} set with +40V, 1 sec. and stored with zero gate/substrate voltage
			0			Up to 10^7 sec. after gate pulse
			0.6		− V/time decade	After 10^7 sec.
Logic window $\lvert V_{TH}-V_{TL}\rvert$	V_W	5.4	8.5		V	Set with ±35V, 100μs
		2.0	5.5		V	10^7 sec. after setting with ±35V, 100μs
Drain current v gate voltage (gain factor)	β	0.1		0.2	mA/V^2	Source/drain voltage = 10V. See Note 1
Bulk effect coefficient	K		0.2		− V	See Note 2
Drain leakage	I_{DSUB}		0.1	1	nA	Gate voltage = 0V, drain/substrate voltage = −10V
Gate/substrate capacitance	C_{GSUB}		2		pF	
Gate/drain capacitance	C_{GD}		<1		pF	

NOTES

1. An approximate relationship between gate voltage and drain current in the high impedance portion of the characteristic is given by:

$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2$$

2. A reverse bias between source and substrate increases the threshold voltage negatively according to:

$$\Delta V_T = K\sqrt{V_{SUBS}}$$

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values, above which operating life may be curtailed or satisfactory performance impaired.

Voltage from any gate to any other terminal:	± 45V
Voltage from source or drain to substrate:	− 45V
Operating temperature:	− 40°C to + 100°C
Storage temperature (see Fig.6):	− 55°C to + 125°C

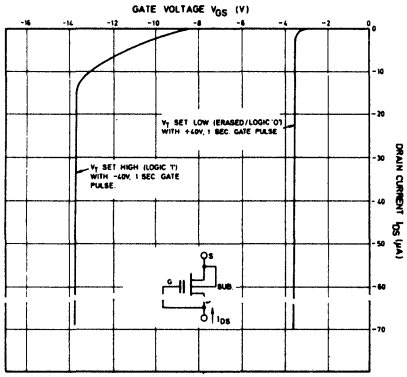


Fig.3 Gate characteristic

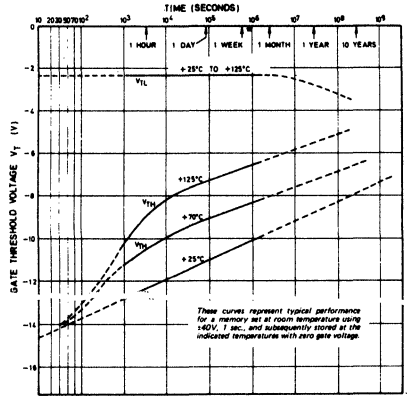


Fig.6 Threshold voltage retention at high ambient temperatures

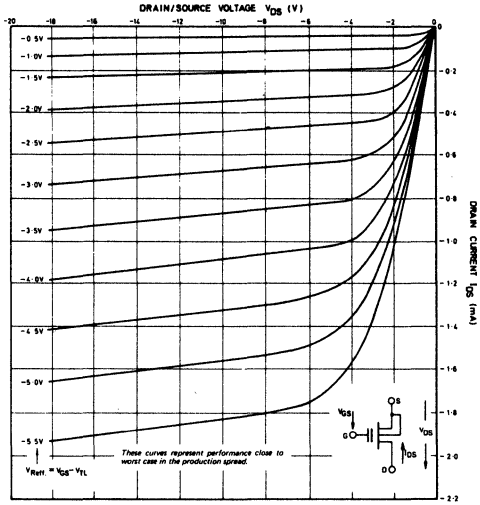


Fig.4 Drain current V. drain/source voltage with V_T set low

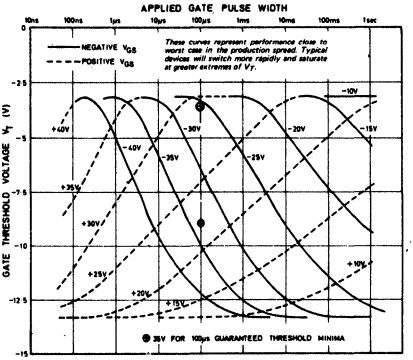


Fig.7 Write/Erase switching speed characteristics

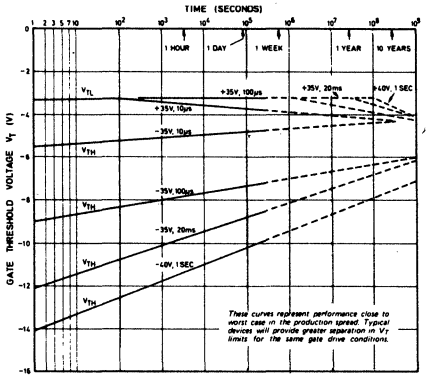


Fig.5 Threshold voltage retention at T_A = +25°C

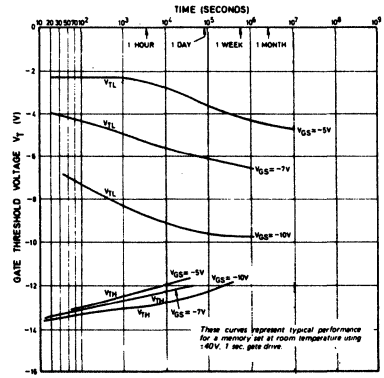


Fig.8 Threshold voltage retention with continuously applied gate read voltages at T_A = +25°C

OPERATING NOTES

These notes briefly describe the operation of a memory using MNOS transistors.

Erasing

Before writing into an MNOS memory the previous contents must be erased; i.e. setting the threshold voltage to its low extreme by applying a large positive gate voltage with respect to the substrate. A convenient method is to connect a large negative pulse to the substrate whilst holding the gate at 0V. Care must be taken, however, to avoid forward-biasing the source/substrate or drain/substrate junctions.

Writing

Writing is performed by applying a large negative pulse to the gate with respect to the substrate. If several MNOSTs were connected to form a word of memory, then all the gates would be driven negative simultaneously. The data to be written is applied as 0V (write '1') or as a negative potential equal to the gate pulse amplitude (write '0') to either the source or drain while the other diffusion is left floating. The technique depends on the fact that a conduction channel is formed between the diffusions: if the channel is at the same potential as the gate then the effective potential across the dielectric is zero. The threshold voltage then remains at its previously erased level and logic '0' is retained. Logic '1' is written when the threshold voltage is raised to the high level, which is achieved by connecting the channel to the substrate potential.

Reading

The memory is read by applying a gate voltage lying between the upper and lower threshold voltage limits. The gate 'read' voltage is chosen to be as high as necessary to ensure that sufficient drain/source output current is available from a low set V_T transistor while leaving sufficient noise margin to ensure that a high set V_T transistor remains 'off'.

CIRCUIT DESIGN NOTES

The following step-by-step procedure describes how a non-volatile memory can be designed to suit individual requirements of data retention time, ambient temperature to be encountered, and output current.

1. Refer to Fig. 4 and determine a value of V_{Reff} (The difference between gate read voltage and low threshold voltage, V_{TL}) that will give the required drain/source current.
2. Determine the minimum logic window (difference between upper and lower V_T extremes) that can be tolerated, by adding desired noise margin to V_{Reff}.
3. Refer to Fig.5, which shows the available range of logic window as a function of time, and check that the minimum logic window determined in (2) above can be accommodated at the end of the desired storage period. If elevated temperatures are anticipated, reference should also be made to Fig.6.
4. From Fig.5, establish worst case initial threshold voltages.
5. Refer to Fig.7 and select a convenient compromise between pulse amplitude and width to give the initial threshold voltages established in (4) above.

NOTE:

Fig.5 shows the minimum threshold voltage retention characteristic as being initially flat. In fact, the memory decay effect is masked by other factors. For example, if a write pulse were chosen to only just take the lower threshold to 4V, then the threshold would begin to rise immediately. The difference between the +35V, 100μs and +40V, 1 sec. write pulse V_{TL} retention curves illustrate this. In practice, the erase pulse will therefore be chosen to be greater than that minimum.

6. Determine gate read voltage i.e. V_{Reff} + worst case V_{TL}.

Design Example

The above design procedure can be illustrated by considering the following, fairly typical, application, in which it is required that data be retained for one week at an ambient temperature of +25°C, and that the output (drain/source) current available at the end of that period should be 0.3mA.

Fig.4 shows that an effective read voltage, V_{Reff}, of −2.0V is required to give an output current of 0.3mA. If a noise margin of 1.0V is assumed, therefore, the minimum logic window that can be tolerated is 3.0V ($|V_{Reff}|$ + noise margin), a value well within the logic window of 6.5V (9.7V−3.2V) available at the 1 week intersects on Fig.5.

By interpolation Fig.5 shows that initial threshold voltages of $V_{TL} \approx -3.5V$ and $V_{TH} \approx -8.0V$ will in one week provide a logic window of something over the 3.0V required. Fig.7 shows that these initial threshold voltages could be achieved with an erase pulse of +25V, 100ms and a write pulse of −30V, 400μs.

Finally, a gate read voltage of −5.5V is chosen to ensure that the worst case V_{TL} of −3.5V is exceeded by the required −2.0V V_{Reff}.

Continuous Reading

If the read voltage is maintained on the gate of an MNOS transistor instead of being pulsed, then the V_{TL} decay rate will be substantially increased as shown by Fig.8. Sometimes it is convenient to operate a memory in this fashion, in which case the read voltage should be as low as possible, say, −5V and the data will remain stored and detectable for a few days only.

APPLICATION EXAMPLE

Fig.9 shows a TTL – compatible single – bit memory constructed from discrete components. The memory may be extended to an arbitrary number of bits simply by repeating the circuit enclosed by the chain dotted boundary. Resistor values may be calculated from following the procedure given in the design notes.

Data to be written should be steady state immediately before and after the write pulse to avoid false writing. The data output is disturbed during writing; if necessary, this disturbance may be masked by strobing the data output with the read command using conventional gating methods.

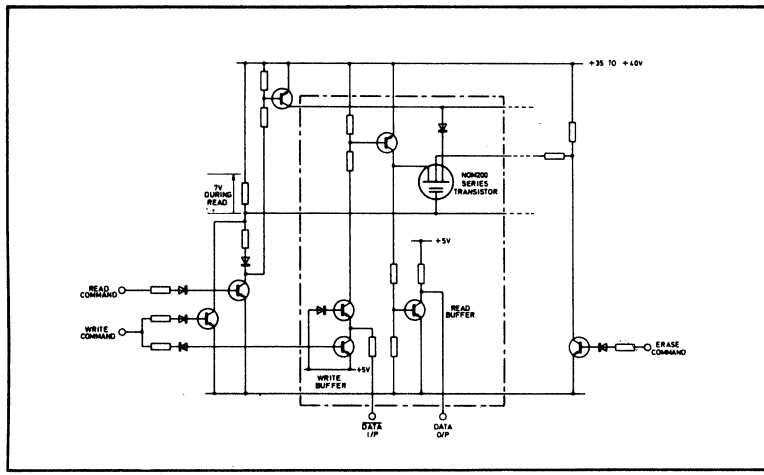


Fig.9 TTL – compatible memory application

CAUTION

These devices have low input capacitance and extremely high input resistance. This means that a very small charge of static electricity can cause the gate voltage to exceed its absolute maximum rating, resulting in permanent damage to the device.

The leads of an MNOS device should be kept shorted together until the device is incorporated into its circuit. Care should be taken to prevent static charge build-up in a circuit during assembly, e.g. the soldering iron used should have an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

The NOM 401 is the simplest device in the Plessey NOM 400 series of undecoded MNOS (Metal-Nitride-Oxide-Semiconductor) transistor arrays. It is an 8 x 8 – bit electrically-alterable, **NON-VOLATILE** memory of particular use in applications where data retention is essential in unpowered equipment or during power interruptions in data processing systems.

Typical applications include: non-volatile data storage, programmable R.O.M.s, and numerical control.

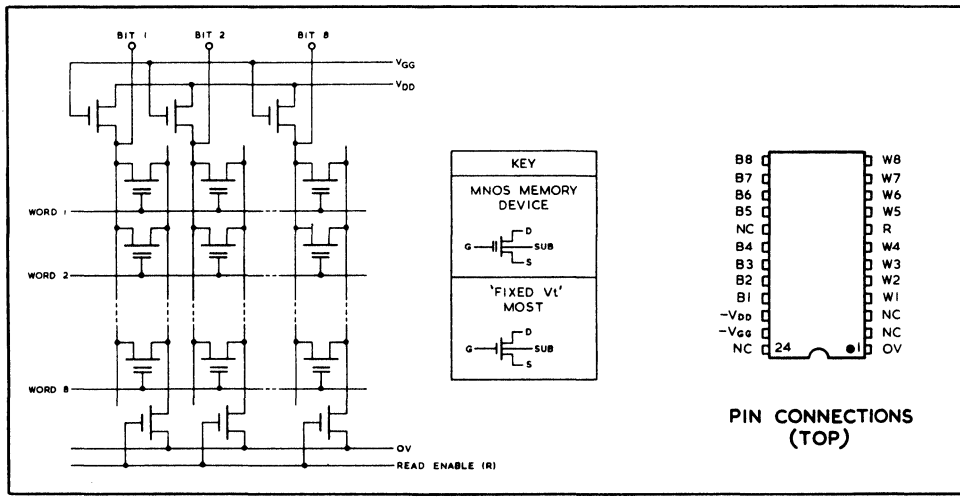
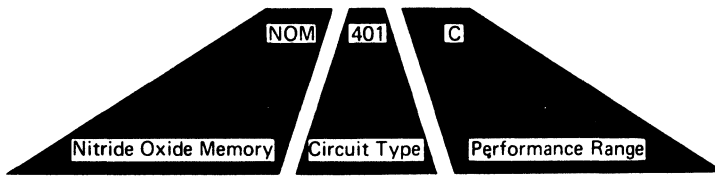


Fig.1 NOM401C circuit and pin connections

PRODUCT IDENTIFICATION

Plessey MNOS devices are coded as shown in the following example:



The term performance range' refers to the relationship between storage time and writing conditions. All devices are available, as standard, in performance grade C, which provides a minimum storage time of 1 year with typical write conditions of 35V for 100μs. Other performance grades offering 100 years minimum storage time or 1μs write time can be made available to special order.

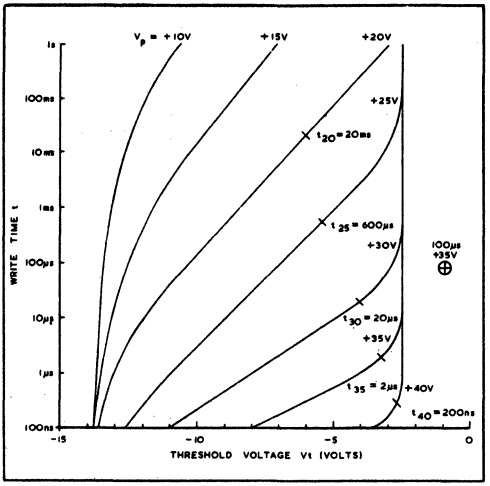


Fig.2 Speed curves for positive values of V_p

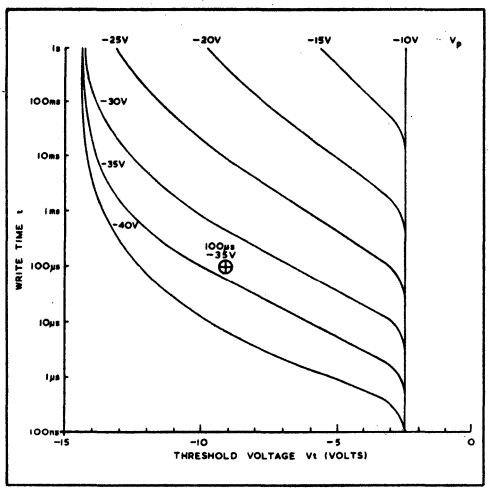


Fig.3 Speed curves for negative values of V_p

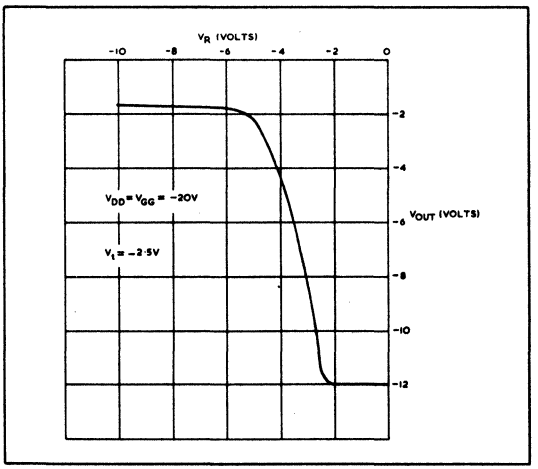


Fig.4 Typical transfer characteristic

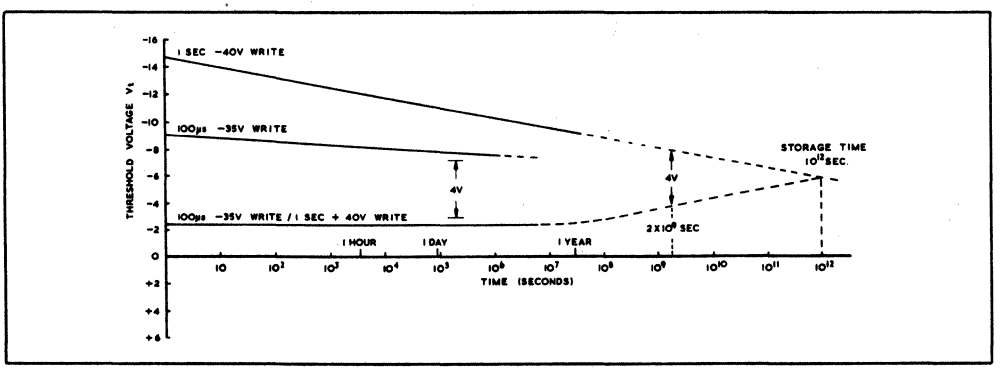
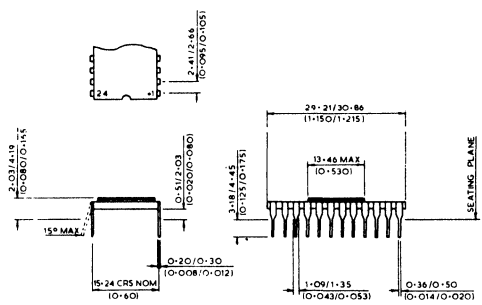


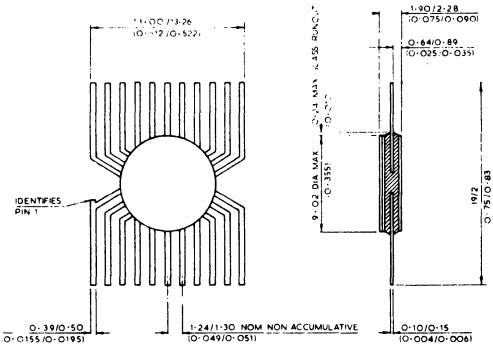
Fig.5 Memory retention characteristic

PACKAGE DETAILS

The NOM 401 is supplied in 24 lead DIL package. It can also be made available to special order in a 22 lead flatpack Dimensions are show thus: mm (in)



24 LEAD DILMON



22 LEAD FLATPACK

CAUTION

These devices have very low input capacitance, they also have an extremely high input resistance. A very small charge can therefore cause the gate voltage to exceed its absolute maximum rating and cause permanent damage to the device. When handling the device, the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

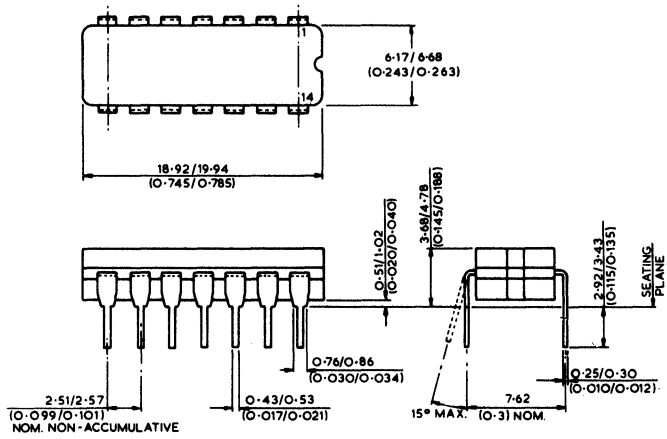
To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

package diagrams

package diagrams

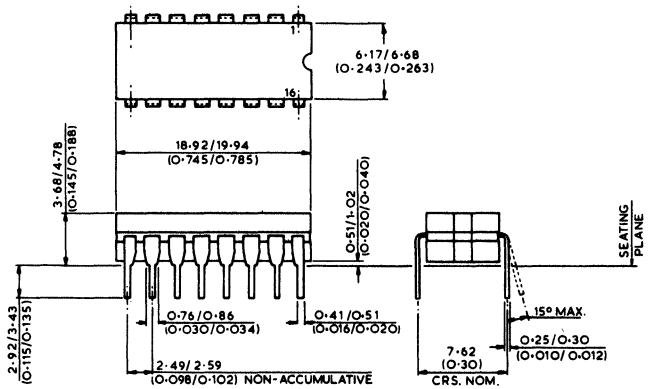
Dimensioned outline diagrams of the packages currently available for standard products are given on this and the following pages. Whilst every effort is made to ensure that the packages offered conform to these diagrams, certain changes may occur from time to time dependent on the supplies of piece parts. However, Plessey Semiconductors will attempt to ensure that such changes, should they occur, shall be minimal.

Note: Dimensions are shown thus: mm (inches).



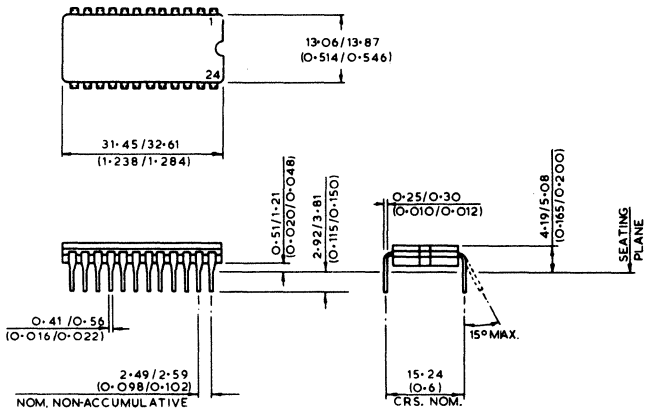
14 LEAD CERAMIC D.I.L.

E1



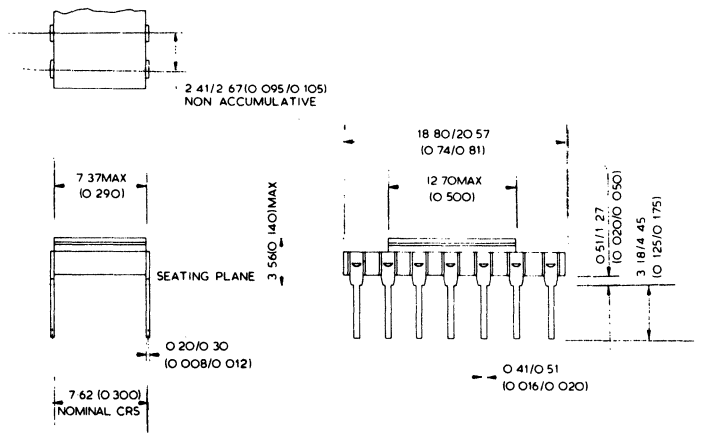
16 LEAD CERAMIC D.I.L.

E2



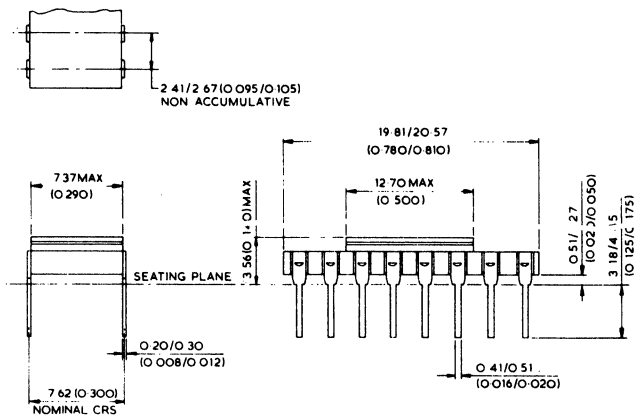
24 LEAD CERAMIC D.I.L.

E3



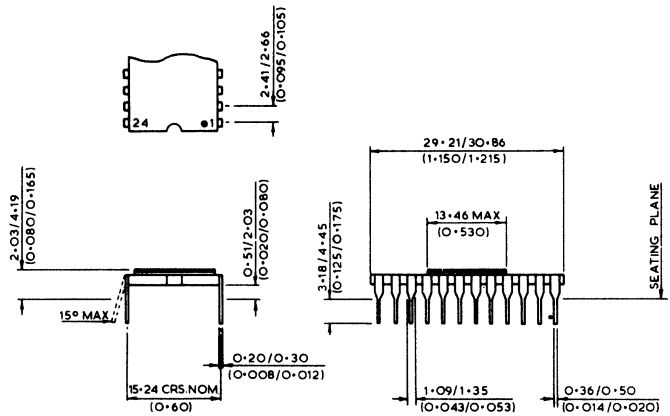
14 LEAD DILMON

E4



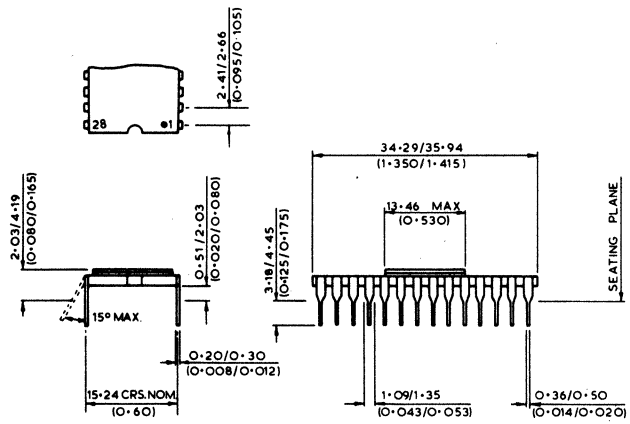
16 LEAD DILMON

E5

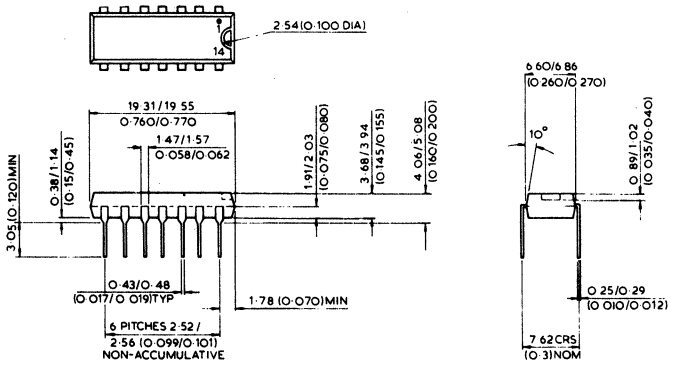


24 LEAD DILMON

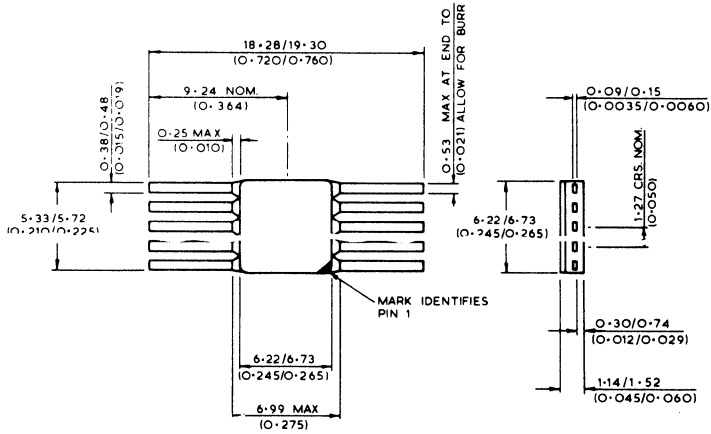
E6



28 LEAD DILMON

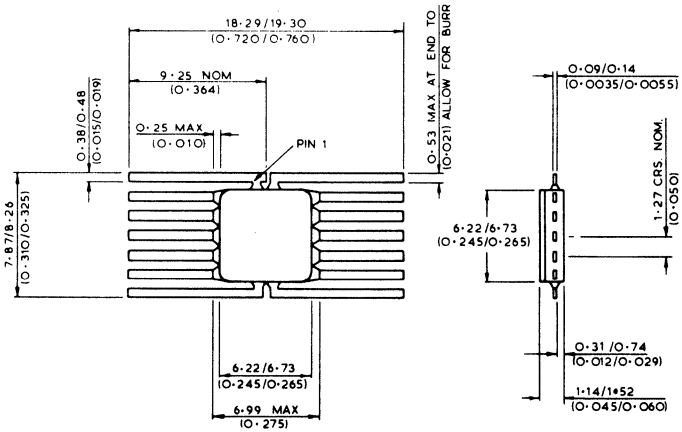


14 LEAD PLASTIC D.I.L.



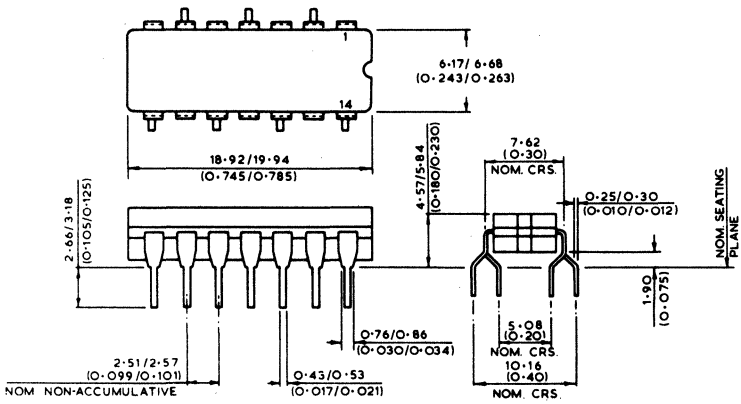
10 LEAD FLAT PACK

F1



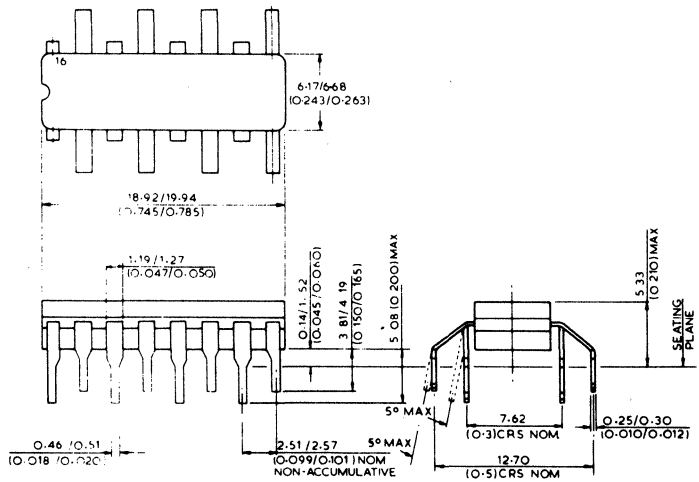
14 LEAD FLAT PACK

F2



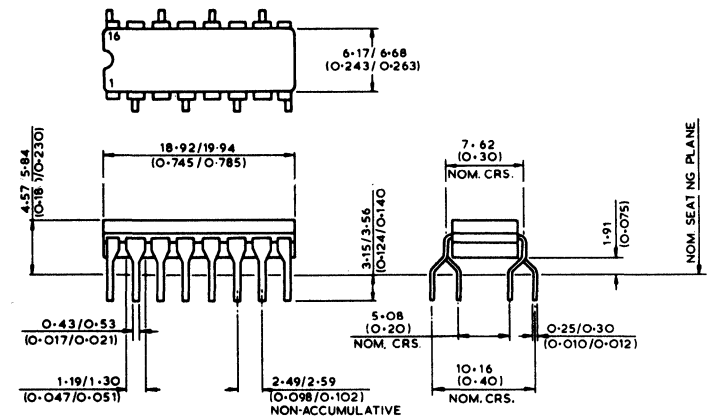
14 LEAD (ZIG-ZAG) CERAMIC Q.I.L.

Q1



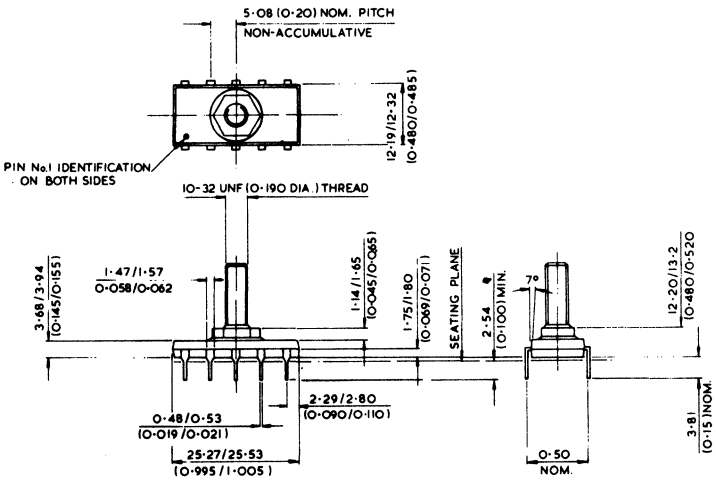
16 LEAD CERAMIC Q.I.L.

Q2



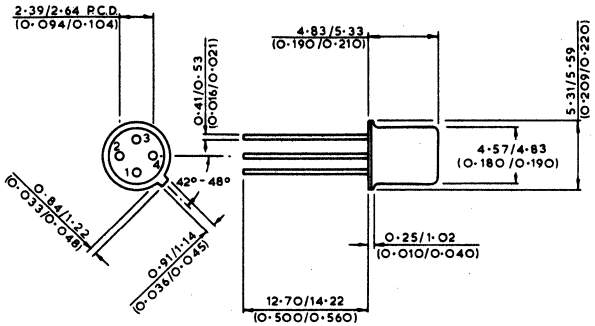
16 LEAD (ZIG-ZAG) CERAMIC Q.I.L.

Q3

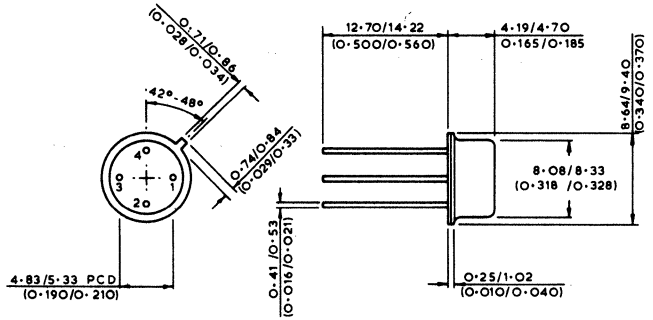


10 LEAD STUD D.I.L.

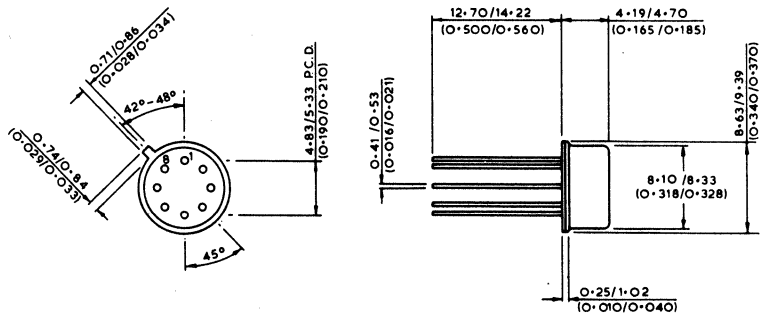
S1



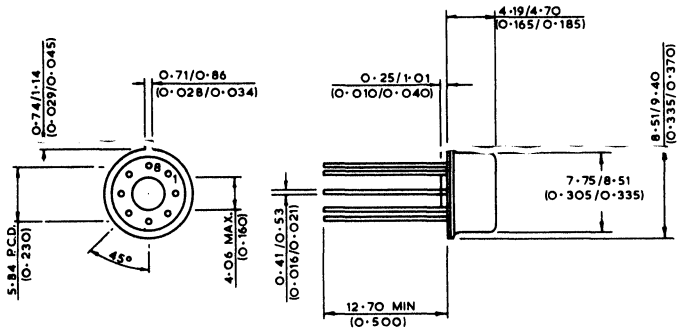
4 LEAD TO-18 **T1**



4 LEAD TO-5 **T2**

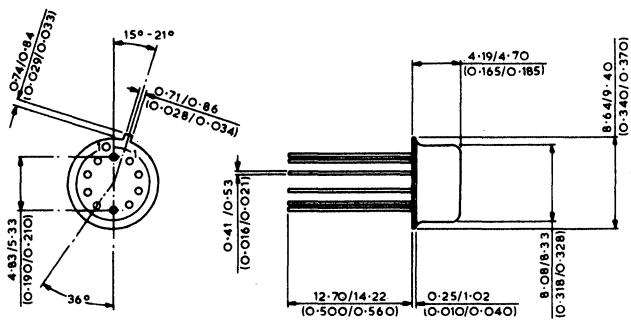


8 LEAD TO-5 (5·08mm P.C.D.) **T3**



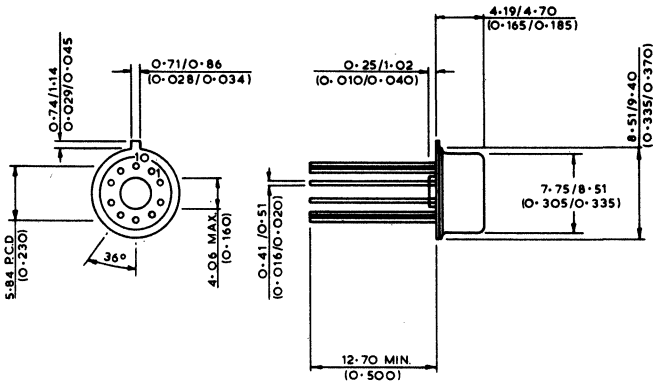
8 LEAD TO-5 (5·84mm P.C.D.) WITH STANDOFF

T4



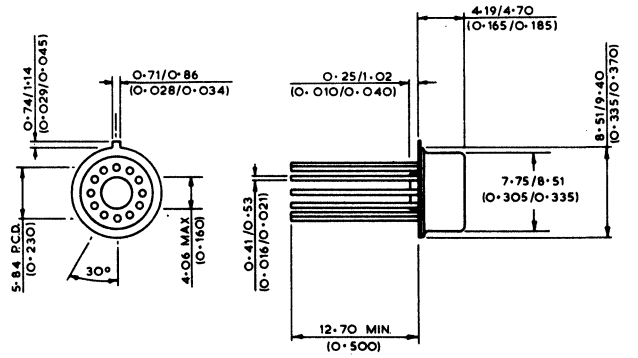
10 LEAD TO-5

T5



10 LEAD TO-100(5·84mm P.C.D.) WITH STANDOFF

T6



12 LEAD TO-5 (5·84mm P.C.D.) WITH STANDOFF

T7

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