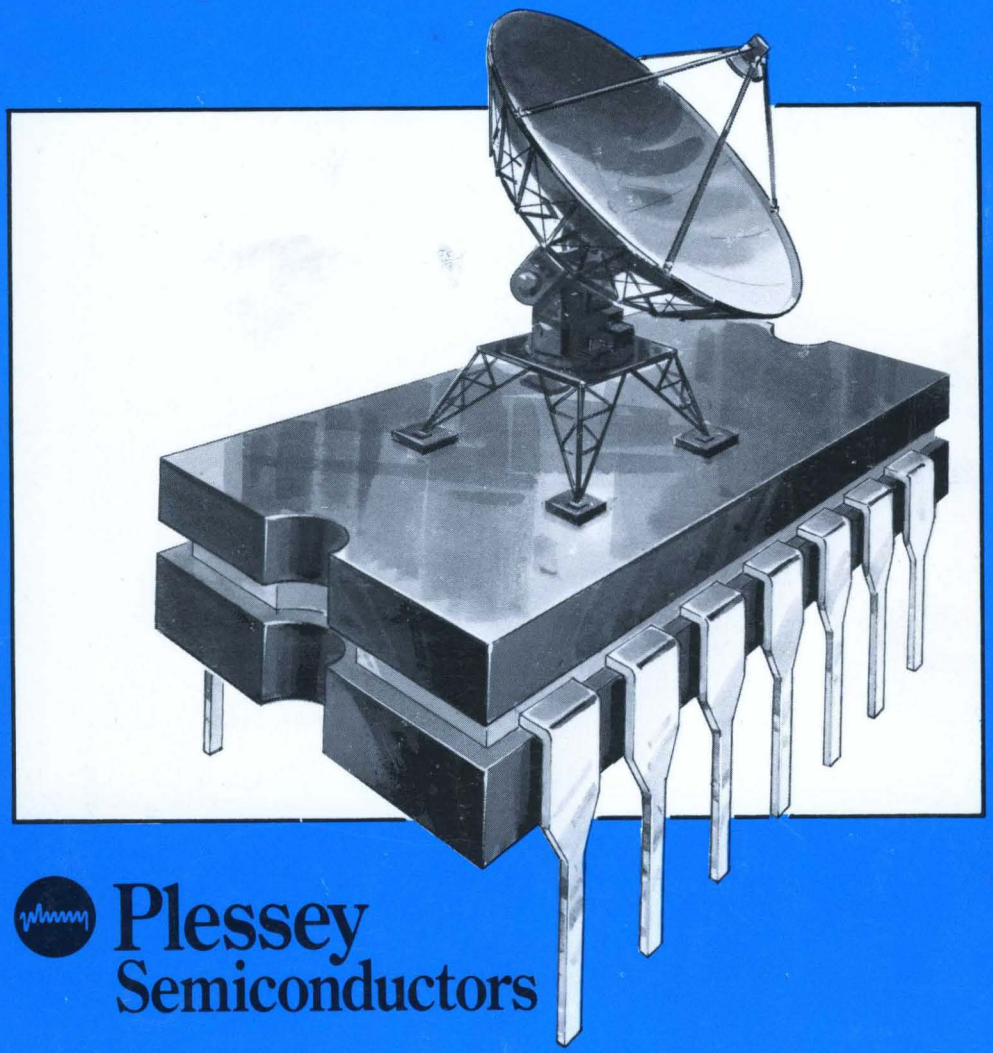
Radar & Radio Communications IC Handbook



Plessey
Semiconductors

RADAR & RADIO COMMUNICATIONS IC HANDBOOK

JULY 1981

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

$4.00

PSI 1806

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ODULATORS

NEAR RF AMPLIFIER

HASE-LOCKED LOOP CIRCUITS

MITING WIDEBAND AMPLIFIERS

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PRODUCT RANGE INFORMATION

Building Block IC's

Plessey integrated circuits are on the leading edge of technology without pushing the ragged edge of capability.

We developed the first 2 GHz counter. And a family of prescalers and controllers for your TV, radio and instrumentation frequency synthesizers.

We have a monolithic 1 GHz amplifier. And a complete array of complex integrated function blocks for radar signal processing and radio communications.

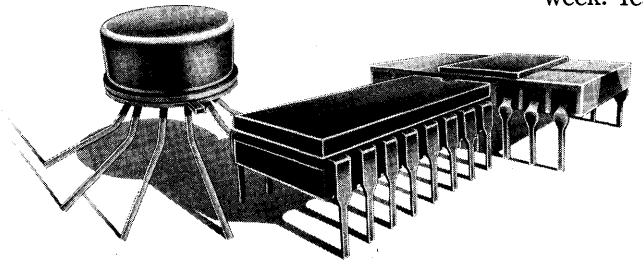
We can supply data conversion devices with propagation delays of just 2½ nanoseconds.

And a range of MNOS logic that stores data for a year when you remove the power, yet uses only standard supplies and is fully TTL/CMOS-compatible.

To develop this edge, we developed our own processes, both bipolar and MOS. The processes were designed for quality and repeatability, then applied to our high volume lines. Most of our IC's are available screened to MIL-STD-883B, and our quality levels exceed the most stringent military, TV and automotive requirements.

Millions of Plessey complex function building block IC's are being used in TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.

Our global scope of operations, our high volume manufacturing facilities, our proprietary processes ensure that we will continue to deliver state-of-the-art technology and reliability in IC devices at the appropriate prices and in the required volumes. Day after day. Week after week. Year after year.



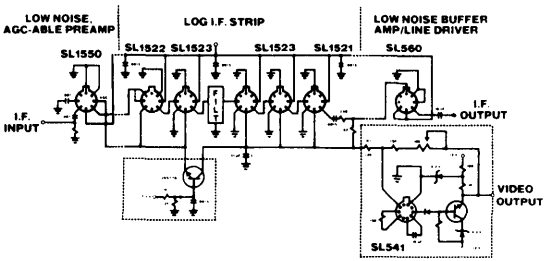
Plessey Semiconductors

1641 Kaiser Avenue, Irvine, CA 92714. (714) 540-9979

Radar Signal Processing

Since the performance of a radar receiver is critically dependent on the performance of its I.F. strip, we offer a range of "building block" IC's that can be used in systems with different performance requirements and configurations.

The logarithmic I.F. strip shown is an example of a low cost, high performance strip fabricated with Plessey IC's. It uses only five devices and a single interstage filter to achieve a logging range of 90 dB, ±1 dB accuracy, −90 dBm tangential sensitivity and a video rise time of 20 ns or less.



Three other Plessey IC's complete the system simply and economically. The AGC-able SL1550 on the front end improves noise figure, dynamic range and sensitivity. The SL541 lets you vary video output levels, with on-chip compensation making it easy to use. And the SL560 is a "gain block" that replaces your hybrid and discrete amplifiers, usually with no external components.

Another advanced system function block is the Plessey SL531 True Log Amplifier. A 6-stage log strip requires a minimum of external components (one capacitor, one resistor per stage), yet has a band-width of 500 MHz, a dynamic range of 70 dB and has a phase shift of only ±3° over its entire range. As with most of our other devices, it operates over the full MIL-temp range and is available screened to MIL-STD-883.

The chart summarizes our Radar Signal Processing IC's. Whether you're working with radar and ECM, weapons control or navigation and guidance systems, our IC's are a simpler, less expensive, more flexible alternative to whatever you're using now for any I.F. strip up to 160 MHz.

For more details, please use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

PLESSEY IC'S FOR RADAR I.F.'S

Wideband Amplifiers for Successive Detection Log Strips

SL521	30 to 60 MHz center frequency, 12 dB gain.
SL523	Dual SL521 (series).
SL1521	60 to 120 MHz center frequency, 12 dB gain.
SL1522	Dual SL1521 (parallel).
SL1523	Dual SL1521 (series).

Low Phase Shift Amplifiers

SL531	True log I.F. amplifier, 10-200 MHz, ±0.5°/10 dB max phase shift.
SL532	400 MHz bandwidth limiting amplifier, 1° phase shift max. when overdriven 12 dB.

Linear Amplifiers

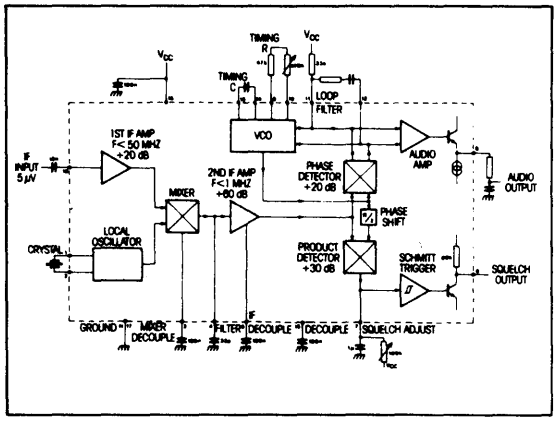
SL550	125 MHz bandwidth, 40 dB gain, 25 dB swept gain control range, 1.8 dB noise figure, interfaces to microwave mixers.
SL1550	320 MHz bandwidth version of SL550.
SL560	300 MHz bandwidth, 10 to 40 dB gain, 1.8 dB noise figure drives 50 ohm loads, low power consumption.

Video Amplifiers and Detectors

SL510	Detector (DC to 100 MHz) and video amplifier (DC to 24 MHz) may be used separately, 11 dB incremental gain 28 dB dynamic range.
SL511	Similar to SL510 with DC to 14 MHz video amplifier, 16 dB incremental gain.
SL541	High speed op amp configuration, 175 V/μs slew rate 50 ns settling time, stable 70 dB gain, 50 ns recovery from overload.

Radio Communications

Our comprehensive line of radio system function blocks is cutting costs, increasing reliability and reducing the size of systems



in applications that range from commercial communications to military manpack radios.

Using our bipolar Process I, the Plessey SL600 Series (hermetic) and SL1600 Series (plastic DIP) feature a high degree of integration, low power consumption and exceptional system design flexibility for I.F.'s up to 10.7 MHz.

Our SL6000 Series uses our bipolar Process III to extend our building block concept even further. Devices all feature advanced circuit design techniques that permit higher levels of integration, lower power consumption and exceptional performance.

Typical is our SL6600, a monolithic IC that contains a complete IF amplifier, detector, phase locked loop and squelch control. Power consumption is a meager 1.5 mA at 6 V, S/N ratio is 50 dB, dynamic range is 120 dB and THD is just 1.3% for 5 kHz peak deviation. The SL6600 can be used at I.F. frequencies up to 50 MHz, with deviations up to 10 kHz.

If any of the Plessey devices appear interesting, use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK. The Handbook includes full details on our integrated circuits, along with a number of applications circuits and design tips that will help you get the maximum system benefits from Plessey products.

Or if your need is more urgent, contact your nearest Plessey Semiconductors representative.

PLESSEY RADIO IC'S

Amplifiers		
SL610	SL1610	140 MHz bandwidth, 20 dB gain, 50 dB AGC range, low 4 dB N.F., low distortion.
SL611	SL1611	100 MHz bandwidth, 26 dB gain, sim. to SL610.
SL612	SL1612	15 MHz bandwidth, 34 dB gain, 70 dB AGC range, 20 mW power consumption.
SL613		145 MHz bandwidth, 12 dB gain, limiting amp/detector.
Mixers		
SL640	SL1640	Double balanced modulator eliminates diode rings up to 75 MHz, standby power 75 mW typical.
Detectors and AGC Generators		
SL620	SL1620	AGC with VOGAD (Voice Operated Gain Adjusting Device).
SL621	SL1621	AGC from detected audio.
SL623	SL1623	AM SSB detector and AGC from carrier.
	SL1625	AM detector and AGC from carrier.
SL624		AM/FM/SSB/CW detector with audio amplifier.
Audio Amplifiers		
SL622		Microphone amp. with VOGAD and sidetone amp.
SL630	SL1630	250 mW microphone/headphone amplifier.
I.F. Amplifiers/Detectors		
SL6600		FM double conversions with PLL detector.
SL6640		FM single conversion, audio stage (10.7 MHz).
SL6650		FM single conversion (10.7 MHz).
SL6690		FM single conversion, low power for pagers (455 kHz).
SL6700		AM double conversion.
Audio Amplifiers		
SL6270		Microphone amplifier with AGC.
SL6290	SL6270	with speech clipper, buffer and relay driver.
SL6310		Switchable audio amplifier (400 mW/9V/8 ohms).
SL6440		High-level mixer.

R. F. Hybrids

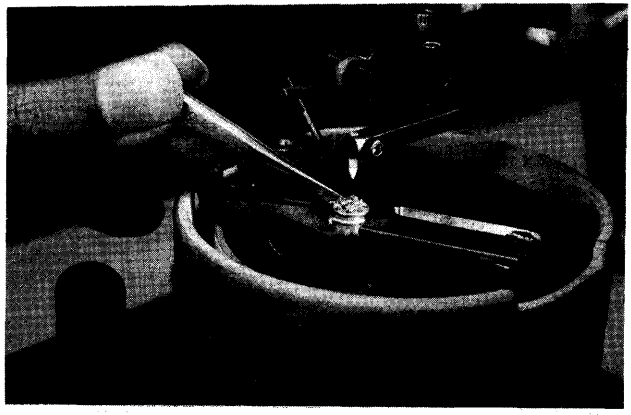
To enhance your systems even further, we have established an R.F. hybrid manufacturing facility in our Irvine, California, U.S.A. headquarters.

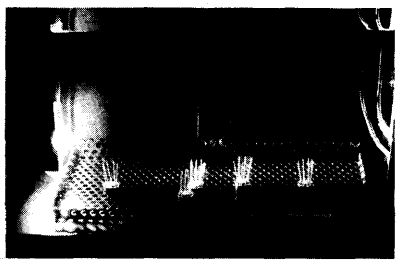
For small production quantities or extremely complex functions, our hybrid capabilities can save you time and money while improving your system performance, reducing system size and increasing system reliability. We can help with your I.F. strips, instrumentation front ends, synthesizer subsystems, high speed A-to-D and D-to-A converters and other complex high-frequency functions.

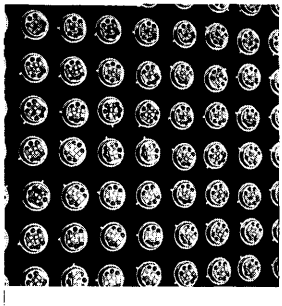
They can be fabricated to MIL-STD-883 using thick and thin film techniques, using our own integrated circuits in combination with discrete transistors, diodes and other components.

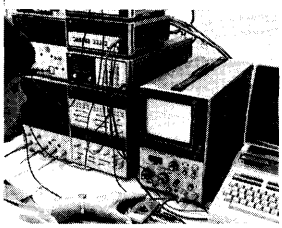
Our IC functions represent the state-of-the-art in high frequency integration, with f_t's as high as 5 GHz. The chips are backed by an in-depth in-house systems knowledge that encompasses radar, radio communications, telecommunications analog and digital conversion, frequency synthesis and a broad range of applications experience.

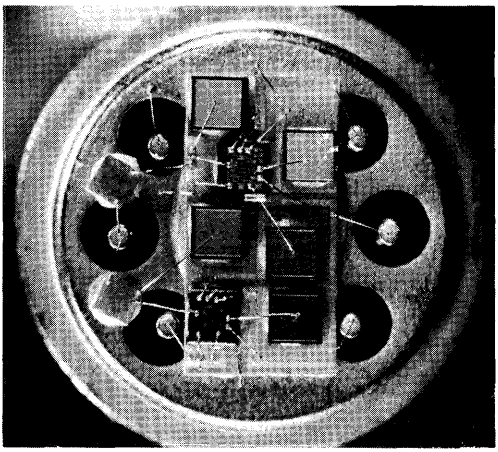
We can work to your prints, or we can design a full system based on your "black box" specifications. For more information, please contact: Plessey Semiconductors, 1641 Kaiser Avenue, Irvine CA 92714, (714) 540-9979.











Frequency Synthesis

Plessey's IC's offer a quick and easy way to lower synthesizer costs while increasing loop response and channel spacing all the way from dc through the HF, VHF, UHF, TACAN and satellite communications bands.

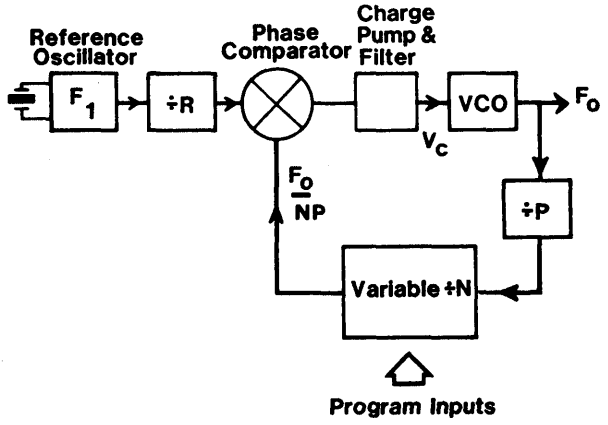
Our single-modulus prescalers operate at frequencies all the way up to 1.8 GHz. They feature self-biasing clock inputs, TTL/CMOS-compatibility and all guaranteed to operate to at least the frequencies shown, most of them over the temperature range from −55°C to +125°C.

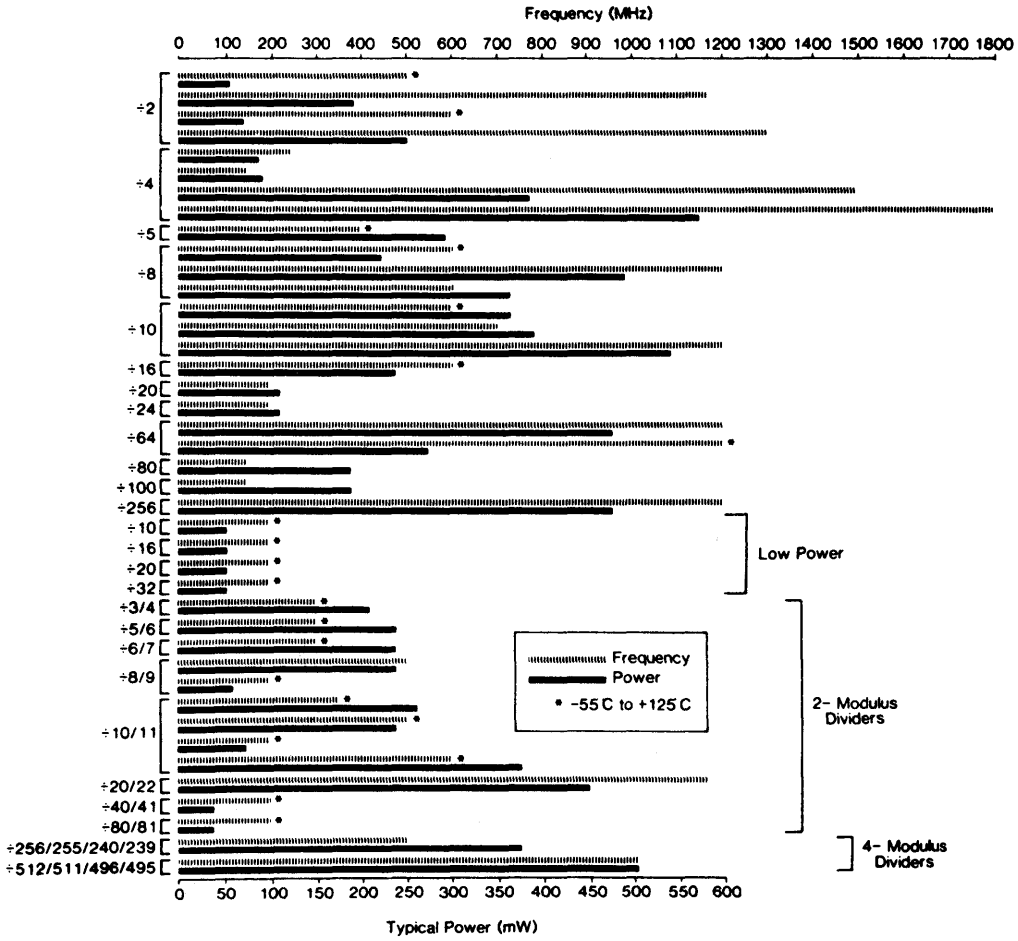
Our 2-modulus and 4-modulus dividers expand your system flexibility and allow even tighter channel spacing. All of them provide low power consumption, low propagation delay and ECL-compatibility.

To simplify your systems even further, we also offer highly integrated control chips. Our NJ8811, for example, includes a crystal oscillator maintaining circuit, a programmable reference divider, a programmable divider to control the four-modulus prescaler and a high performance phase/frequency comparator so that you can phase lock your synthesizer to a crystal with none of the usual headaches and hassles.

We've put together a FREQUENCY SYNTHESIZER IC HANDBOOK that details all of the Plessey IC's and includes a number of applications circuits, practical examples of how Plessey integrated circuits can simplify your designs and improve system performance.

For your copy of the Handbook, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.




Frequency (MHz)
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800
÷2
÷4
÷5
÷8
÷10
÷16
÷20
÷24
÷64
÷80
÷100
÷256
÷10
÷16
÷20
÷32
÷3/4
÷5/6
÷6/7
÷8/9
÷10/11
÷20/22
÷40/41
÷80/81
÷256/255/240/239
÷512/511/496/495
Low Power
Frequency
Power
* -55 C to +125 C
2- Modulus Dividers
4- Modulus Dividers
0 50 100 150 200 250 300 350 400 450 500 550 600
Typical Power (mW)

Telecommunications

Plessey functional building block IC's are exceptionally versatile. Designed from a systems standpoint, they reduce complexity and lower costs while increasing the performance of telecommunications systems.

Our SL600 Modulator/Phase Locked Loops are used in waveform generators and in AM, PAM, FM, FSK, PSK, PWM, tone burst and Delta modulators.

Our SL1000 Series amplifiers meet the most stringent demands of telephone transmission equipment.

Our transistor arrays with up to five electrically and thermally matched transistors on a chip are ideal for discrete and hybrid amplifiers and mixers. In addition to standard second-source devices that plug directly into your designs, we have a number of devices designed for your low noise and ultra-high frequency applications.

The Plessey TELECOMMUNICATIONS IC HANDBOOK contains complete information on all of these devices, as well as application notes, to help you get the most out of them. To get your copy, please use the postage-paid reply card at the back of this book or call your nearest Plessey Semiconductors representative.

Telecommunications Devices

MJ1440	HDB3 encoder/decoder
MJ1444	PCM synchronizing word generator
MJ1445	PCM synchronizing word receiver
MJ1471	HDB3/AMI encoder/decoder

Data Communications MOS

MP3812	32 x 8-bit FIFO memory, serial or parallel, up to 0.25 MHz data rates, easily stacked.
MJ2841	64 x 4-bit FIFO memory, 5 MHz clock rate.

Modulator/Phase Locked Loops

SL650	Modulator/PLL for AM, PAM, SCAM, FM, FSK, PSK, tone-burst and Delta modulation; VFO variable 100:1.
SL651	Similar to SL650 without auxiliary amplifier.
SL652	Similar to SL650, low cost.

Telephone Circuits

SL1001	Modulator/demodulator, 50 dB carrier and signal suppression, −112 dBm noise level.
SL1021	3 MHz channel amplifier, stable remote gain control.
SL1025	FDM balanced modulator, 50 dB carrier and signal suppression, 5 dB conversion gain.
SL1030	200 MHz wideband amplifier, programmable gain, low noise.

Transistor Arrays

PLESSEY PART NO.	2ND-SOURCE PART NO.	PLESSEY PART NO.	2ND-SOURCE PART NO.
SL3081	CA3081	SL3051	CA3951
SL3082	CA3082	SL355	NONE
SL3083	CA3083	TBA673	TBA673
SL3183	CA3183	SL1495	CA1495L
SL3146	CA3146	SL1496	MC1496G
SL3093	CA3093	SL1496	MC1496L
SL3018	CA3018	SL1595	MC1595L
SL3018A	CA3018A	SL1596	MC1596G
SL3118A	CA3118A	SL1596	MC1596L
SL3118	CA3118	SL3054	CA3054
SL3050	CA3050	SL3086	CA3086

SL360	High frequency matched pair, f_t=2.5 GHz.
SL363	Low noise matched pair, f_t=2.2 GHz.
SL2363/4	5GHz dual long-tailed pair.
SL3145	Five transistor array, f_t=2.5 GHz.

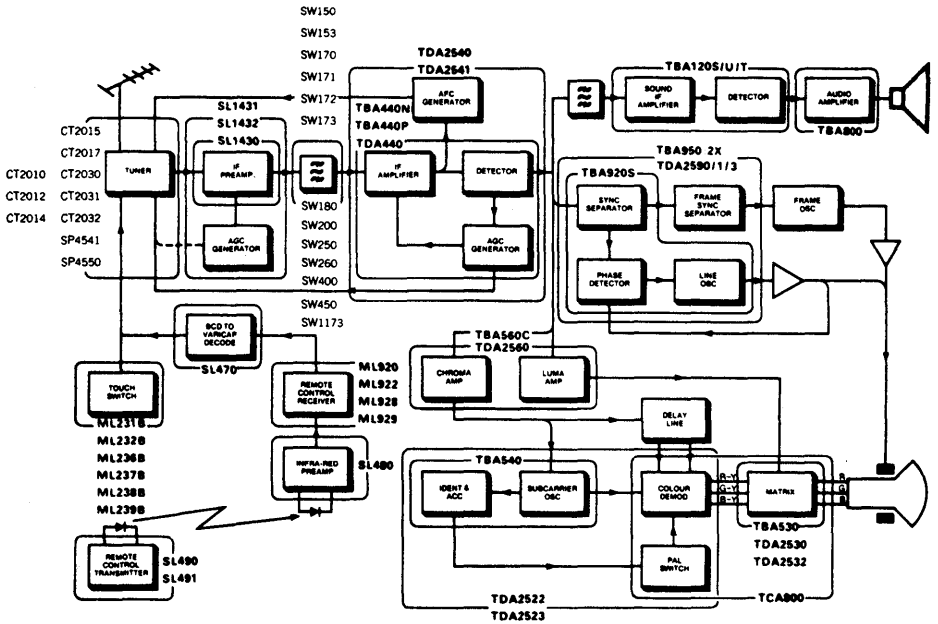
Television IC's

Plessey integrated circuits are in millions of homes, in television sets around the world.

Economical and reliable, our devices cover the range from remote controls to touch tuners to frequency synthesizers, as well as a range of second-source devices for the IF color processing and line oscillators.

For the 1980's, we have introduced the Plessey KEY System, designed for maximum flexibility, simplicity and ease of manufacture. The KEY System frequency synthesizer offers accurate, high stability frequency selection, channel and program identification, and the very finest digital fine tuning. It can be configured to receive up to four completely different standards (PAL, SECAM, SECAMF, and NTSC) in a single TV set. It has 100 channel capability per standard, and includes a 32-program non-volatile memory that contains channel, fine tuning and standards information. And it can be interfaced to a Plessey or other microprocessor for games, Teletext or similar applications.

Complete data on all our television devices has been assembled in our TELEVISION IC HANDBOOK, along with application notes to make them even easier to use. Please use the postage-paid reply card at the back of this book to order your copy, or simply contact your nearest Plessey Semiconductors representative.



ALL TBA, TCA, TDA DEVICES ARE SECOND-SOURCED.

ECL III Logic and Data Conversion

As radar and communications systems become faster and more complex, the need arises for digital processing. We have developed a family of functions with speeds unequalled anywhere.

Part of our family is a range of ECL III logic that is a direct plug-in replacement for MECL logic, including low impedance as well as high impedance devices. We extended the range by adding functions with lower delays and much higher operating speeds. Our SP16F60, for example, is the world's fastest dual 4-input OR/NOR gate, with a switching speed of just 500 picoseconds. Devices can also be selected for certain specifications (such as threshold voltage or slew rate on our SP1650/1, toggle rates or delays on our SP1670) to handle your most demanding applications. We've also developed a family of high speed comparators and circuits for ultra-high speed A-to-D converters. Our latching SP9750 high speed comparator features a maximum settling time of 2 ns, a propagation delay of 3.5 ns and is capable of operating at rates up to 100 million samples per second.

Currently, our devices are being used in radar and video processing, nucleonics systems, transient recorders and secure speech transmission systems. We have compiled a number of application notes and details on the devices in our ECL III LOGIC AND DATA CONVERSION IC HANDBOOK. To get your copy, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.

HIGH SPEED ECL III LOGIC

SP1648	Voltage controlled oscillator
SP1650	Dual A/D comparator, Hi-Z
SP1651	Dual A/D comparator, Lo-Z
SP1658	Voltage controlled multivibrator
SP1660	Dual 4-I/P OR/NOR gate, Hi-Z
SP1661	Dual 4-I/P OR/NOR gate, Lo-Z
SP1662	Quad 2-I/P NOR gate, Hi-Z
SP1663	Quad 2-I/P NOR gate, Lo-Z
SP1664	Quad 2-I/P OR gate, Hi-Z
SP1665	Quad 2-I/P OR gate, Lo-Z
SP1666	Dual clocked R-S Flip-Flop, Hi-Z
SP1667	Dual clocked R-S Flip-Flop, Lo-Z
SP1668	Dual clock latch, Hi-Z
SP1669	Dual clock latch, Lo-Z
SP1670	Master-slave D Flip-Flop, Hi-Z
SP1671	Master-slave D Flip-Flop, Hi-Z
SP1672	Triple 2-I/P exclusive-OR gate, Hi-Z
SP1673	Triple 2-I/P exclusive-OR gate, Lo-Z
SP1674	Triple 2-I/P exclusive-NOR gate, Hi-Z
SP1675	Triple 2-I/P exclusive-NOR gate, Lo-Z
SP1692	Quad line receiver
SP16F60	Dual 4-I/P OR/NOR gate

HIGH SPEED DATA CONVERSION PRODUCTS

SP9680	High speed latched comparator.
SP9685	Ultra-fast comparator; 0.5 ns typical set-up time; typical 2.2 ns propagation delay; excellent CMR.
SP9687	Dual SP 9685.
SP9750	High speed latched comparator with precision current source, wired-OR decoding; 2 ns min. set-up time; 2.5 ns propagation delay.
SP9752	2-bit ADC expandable to 6-bit ADC; very fast 125 MHz clock.
SP9754	4-bit ADC expandable to 8-bit ADC; very fast 100 MHz clock.
SP9768	8-bit DAC; extremely fast; available 3rd quarter 1980.
SP9778	8-bit SAR; works with SP9768 to make a two-chip successive approximation ADC (20 MHz clock); available 4th quarter 1980.

MNOS Non-Volatile Logic

As semiconductors become more pervasive in military and commercial applications, the need for non-volatile data retention becomes more and more critical.

Plessey NOVOL MNOS devices answer that need, and will retain their data for at least a year (−40°C to +70°C) in the event of "power down" or a system crash.

Our devices all operate from standard MOS supplies and are fully compatible with your TTL/CMOS designs. The high voltages normally associated with electrically-alterable memories are generated on-chip to make system interface simpler and less expensive.

Plessey NOVOL devices provide a reliable, sensible alternative to CMOS with battery back-up or mechanical, electro-mechanical and magnetic devices. Applications include metering, security code storage, microprocessor back-up, elapsed time indicators, counters, latching relays and a variety of commercial, industrial and military systems.

For more information, contact your nearest Plessey Semiconductors representative, or use the postage-paid reply card at the back of this brochure to order your copy of the Plessey NOVOL literature package.

PLESSEY NOVOL MNOS

MN9102	**4-bit Data Latch (+5V, −12V)**
MN9105	**4-Decade Up/Down Counter (+5V, −12V)**
MN9106	**6-Decade Up Counter (12V only)**
MN9107	**100-Hour Timer (12V only)**
MN9108	**10,000-Hour Timer (12V only)**
MN9110	**6-Decade Up Counter with Carry (12V only)**
MN9210	**64 x 4-Bit Memory**
*	**8 x 4-Bit Memory**
*	**6-Decade Up/Down Counter, BCD Output**
*	**6-Decade Up/Down Counter with Preset BCD Output**

*** COMING SOON**

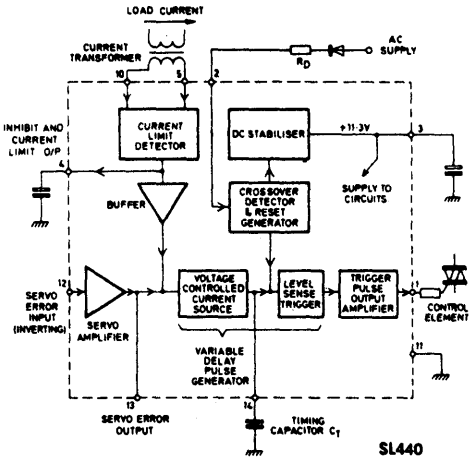
Power Control

Plessey power control devices are highly integrated not just to solve the problems, but to solve them at a lower cost than any other available method.

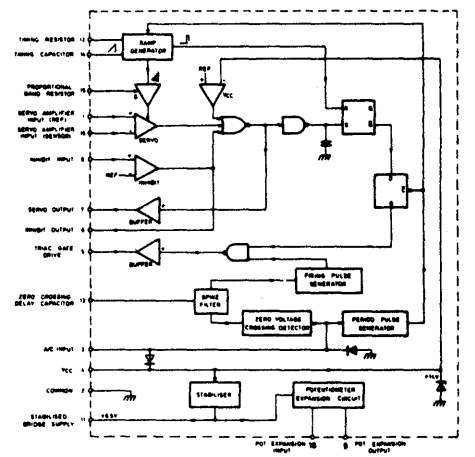
For timing, our devices use a pulse integration technique that eliminates the need for expensive electrolytic capacitors, thus increasing accuracy and repeatability while reducing costs. An integral supply voltage sensing circuit inhibits triac gate drive circuitry if the supply is dangerously low to prevent half-wave firing and firing without achieving complete bulk conduction. A zero-voltage spike filter prevents misfiring on noise inputs. Symmetrical control prevents the introduction of dc components onto the power lines.

Devices have been tailored for specific applications as indicated in the chart. For more information, please use the postage-paid reply card at the back of this book to order our POWER CONTROL IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

SL440	**Proportional phase control for motors, lamps and lower power, fast response heating.**
SL441	**Similar to SL440, with proportional temperature control and thermister malfunction sensing, for hairdryers, soldering irons and food warmers.**
SL442	**Switch mode power supply control, up to 40 kHz, integral oscillator, variable ratio space/mark pulses, soft-start, dynamic current limiting, OVP.**
SL443	**Similar to SL441 with manual power control, long timing periods for hot plates, electric blankets and traffic lights.**
SL444	**Similar to SL441 for 240V permanent magnet motor with thermal trip, current limit detector.**
SL445	**Proportional or On/Off control, temperature trip/inhibit circuitry, LED and alarm drive facilities, for ovens, heaters, industrial temperature controllers.**
SL446	**On/Off servo loop temperature controller, low external component count, for water and panel heaters, refrigerators, irons.**
TBA1085	**Motor speed control**



SL440

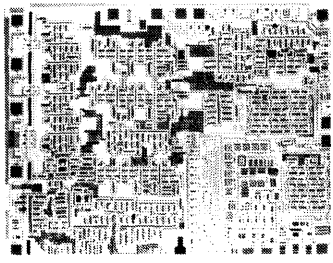

SL445

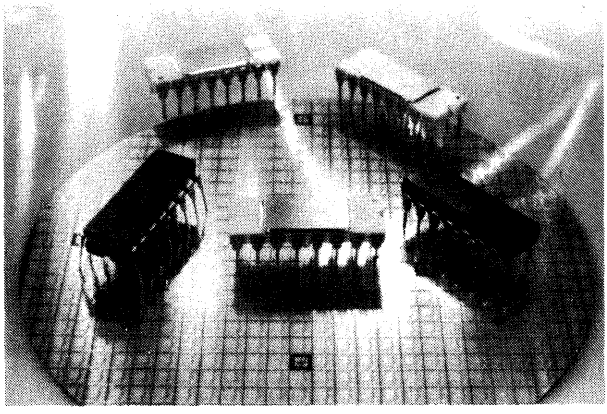
Processes, Testing and Quality Control

Just as we applied our systems knowledge to the partitioning of functions to make our IC's extremely flexible and cost effective, we also developed an internal system concept to ensure that we could deliver our state-of-the-art solutions year after year.

Our concept of standard processes and rigid design rules ensures that our devices are reproducible this year, next year and five years from now. Our continuing investment in research and development ensures that any new products we introduce will be on the leading edge of technology, yet with the same high performance and reliability that our customers have come to expect as the Plessey standard.

The result is that millions of Plessey devices have been built into TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.



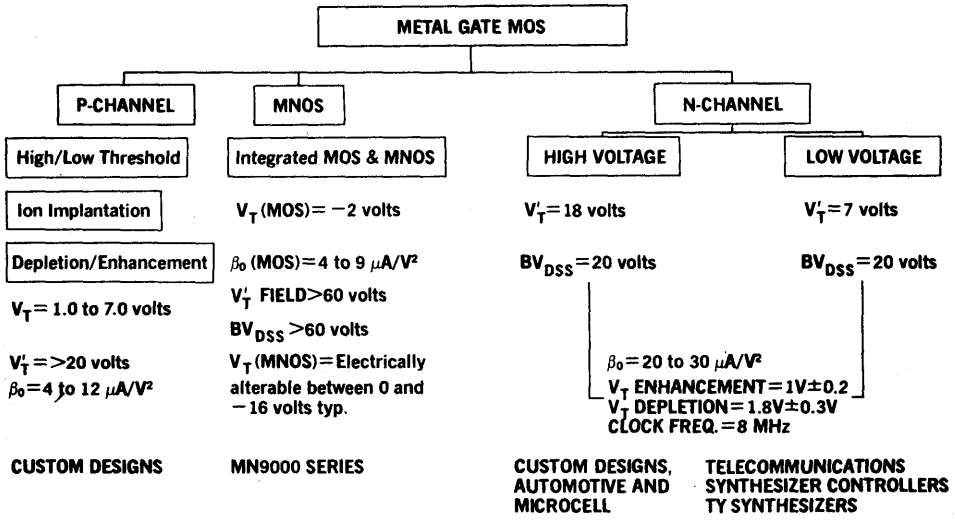


Plessey MOS Processes

P-channel metal gate MOS has been in production for years and is used for both standard Plessey products and custom LSI. Using ion implantation to modify transistor and field threshold voltages, we can reproduce virtually any p-channel metal gate process, with or without depletion loads.

MNOS (non-volatile) is essentially a p-MOS process with variable threshold memory transistors fabricated alongside conventional MOS transistors. A modified oxide-nitride gate dielectric permits the injection and retention of charge to change the threshold voltage. Current Plessey products will retain an injected charge for at least a year, and include an on-chip high voltage generator so that they may be used with standard supply voltages.

N-channel metal gate MOS uses an auto-registration co-planar process with layout similar to our p-MOS. Ion implantation is used to define the threshold voltage of the depletion and enhancement transistors. The constant-current-like characteristics of depletion load devices give the most effective driving capability, and enhancement-depletion technology simplifies design and increases packing density. The field threshold voltage is also controlled by an ion implant, allowing the use of a lightly doped substrate. This reduces both the body constant and the junction capacitance and results in faster switching speeds.



Plessey Bipolar Processes

Bipolar Process I is a conventional buried +N layer diffusion process with f_t=600 MHz and other characteristics similar to industry-standard processes. Applications range from high reliability military devices to high volume consumer products.

Process Variant	A	B	G	D
Application	General Purpose	Non Saturating Logic	Saturating Logic	Linear Consumer
BV_{CBO} @ 10μA	20V min.	10V min.	10V min.	45V min.
BV_{EBO} @ 10μA	5.3V to 5.85V	5.15V min.	5.15V min.	6.8V to 7.4V
LV_{CEO}	12V min.	8V min.	8V min.	20V min.
$V_{CE\,(SAT)}$ @ I_B=1mA, I_C=10mA	0.43V max.	0.32V max.	0.43V max.	0.6V max.
h_{FE} @ I_C=5mA, V_{CE}=5V	40 to 200	50 min.	50 min.	50 to 200
f_T @ I_C=5mA, V_{CE}=5V	500 MHz	500 MHz min.	500 MHz min.	350 MHz min.

Bipolar High Voltage (HV) Process is a variant of Process I that yields an LV_{ceo} greater than 45 volts. Doping levels can be controlled and an extra diffusion used to fabricate a buried avalanche diode with a 40 V breakdown for absorbing powerful noise transients without being destroyed.

Process Variant	CA
BV_{CBO} @ 10μA	80V min.
BV_{EBO} @ 10μA	7.2V to 8.0V
LV_{CEO}	45V min.
$V_{CE\,(SAT)}$ @ I_B=1mA, I_C=10mA	0.4V max.
h_{FE} @ I_C=5mA V_{CE}=5V,	80 to 300
f_T @ I_C=5mA, V_{CE}=5V	250 MHz min.

Bipolar Process III uses very shallow diffusion and extremely narrow spacing for high frequency integrated circuits with unusually low power consumption and high packing densities. An f_t of 2.5 GHz allows us to routinely produce analog amplifiers with bandwidths as high as 300 MHz and low power dividers and prescalers that operate at frequencies up to 1.2 GHz. Process variants allow us to produce devices with an extended β, higher breakdown voltages and very small geometries.

Process Variant	WE
Application	Digital
BV_{CBO} @ 10μA	10V min.
BV_{EBO} @ 10μA	5.1V to 5.8V
LV_{CEO}	7V min.
$V_{CE\,(SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=5mA, V_{CE}=2V	40 to 200
f_T @ I_C=5mA, V_{CE}=2V	1.8 GHz

Bipolar Process 3V is an extension of our Process III. Ion implantation and washed emitters have given the process an f_t=6.5 GHz, allowing us to produce dividers working at 2 GHz, logic gates with delays of less than 500 picoseconds and linear amplifiers at 1 GHz.

Process Variant	WV
Application	Digital
BV_{CBO} @ 10μA	8V min.
BV_{EBO} @ 10μA	3.0V to 5.0V
LV_{CEO}@ 5mA	6V min.
$V_{CE\,(SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=10mA, V_{CE}=5V	40 to 120
f_T @ I_C=5mA, V_{CE}=2V	6.5 GHz

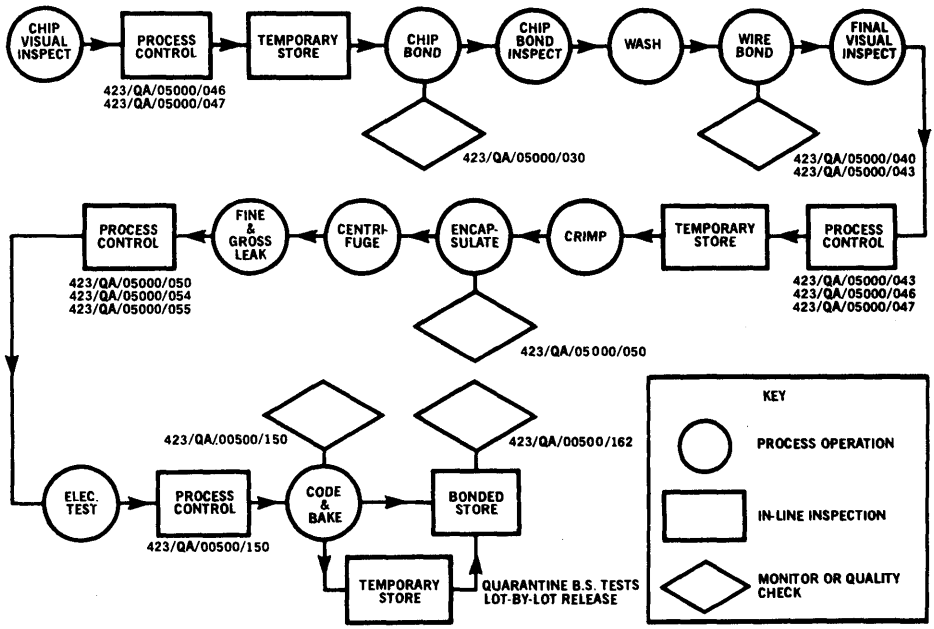
Testing and Quality Control

A major thrust of our development work is to ensure that our processes will routinely produce reliable devices. Our Process III has a projected MTBF of 400,000 hours while our Process I is even better.

Our facilities include the latest test equipment (such as the Macrodata MD501, Teradyne J324 and Fairchild Sentry VII and Sentinel) to allow us to perform all the necessary functional and parametric testing in-house. We have an internal capability to provide specific applications-oriented screening, and most Plessey IC's are available screened to MIL-STD-883 and other international specifications. Our quality levels exceed the most stringent military, TV and automotive requirements as a matter of course.

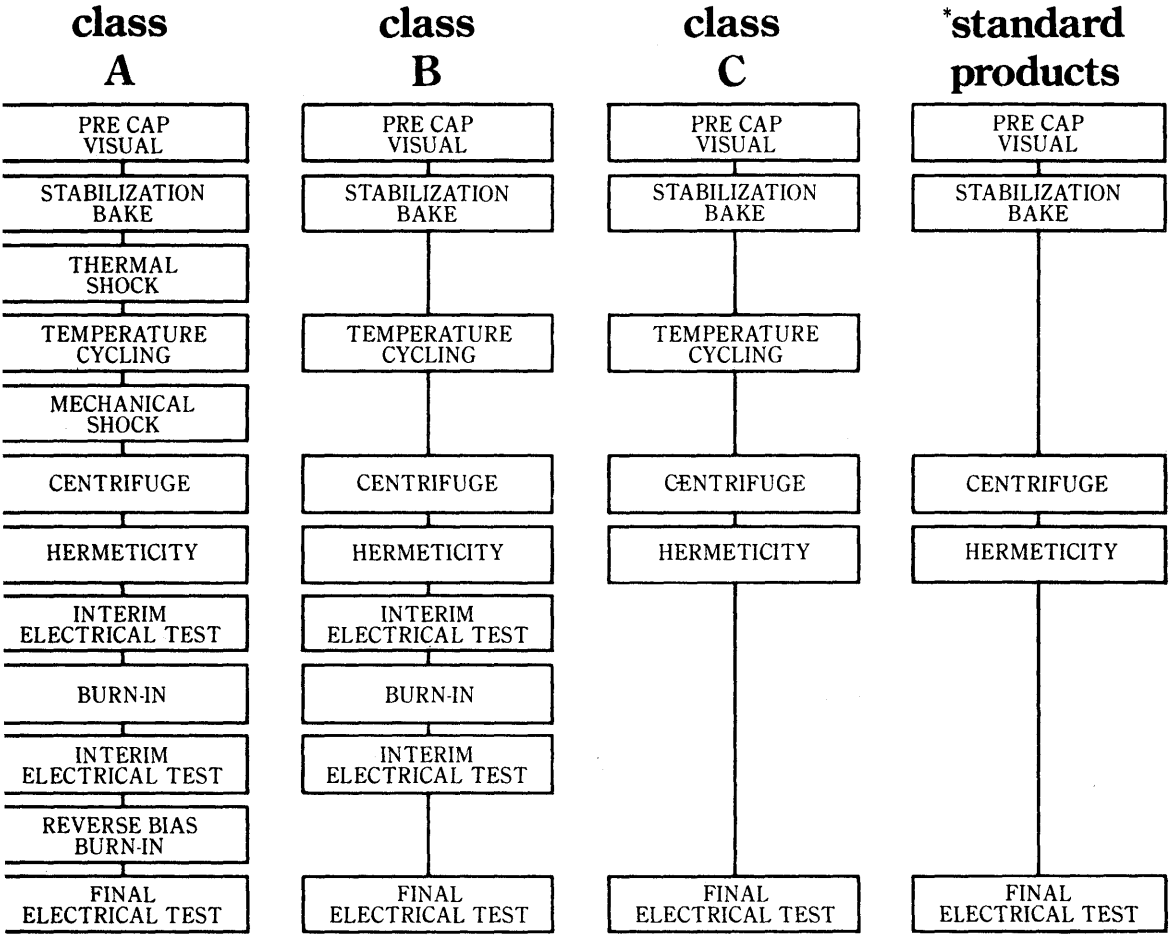
But the best proof of all these claims is our products themselves. After you've reviewed the products that could help you with your systems, use the postage-paid reply card or contact your nearest Plessey representative for complete details.

ASSEMBLY OF INTEGRATED CIRCUITS
QUALITY ASSURANCE



I.C. Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Introducing Plessey CMOS

Plessey Semiconductors new range of high performance CMOS products form an important addition to its range of established Bipolar and metal gate MOS integrated circuits.

With the active co-operation of the Mitel Corporation of Canada - where CMOS products are in volume production - Plessey Semiconductors has chosen the ISO-CMOS® process, an isolated polysilicon gate process that results in low power, high packing densities and high speeds. In fact,ISO-CMOS products are among the fastest in the world.

The products and facilities listed in this shortform have been chosen to serve the four areas of application for which CMOS is today one of the essential technologies:

Telecommunications, page **1**.

EDP products pages **2** and **3**.

Semi-Custom Design, page **3**.

Full Custom Design - especially for Radio Communications - see pages **3** and **4** for full process details.

Over 25 Plessey Semiconductors CMOS types are available now, with a further 17 (including a high performance version of the popular 6802 microprocessor,a 16K ROM and a 4K static RAM) becoming available through 1981.

Full technical information on these products is available on request.

Product list

Planned introduction

Available now

MV4320, MV4322, MV4323, MV4325, MV4326	Family of loop disconnect push-button telephone circuits
MV8820, MV8860, MV8865	Family of DTMF telephone dialling decoders and filters
MV41SC04	Quad 5V to 12V level shifter
MV4330, MV4331, MV4332	30 and 32-bit static shift registers/ 7-segment LCD display drivers
MV4311, MV4368, MV4511	7-segment LED drivers
MV74SC137/138/139 MV74SC237/238/239 MV74SC240/241/244/540/541 MV74SC245/545	Family of octal pin-for-pin replacements for 74LS series TTL

Available Mid-1981

MV5087, MV5089, MV5091, MV5093	DTMF telephone tone generator circuits
MV8862, MV8863	Extensions to family of DTMF decoders
MV74SC373/573, MV74SC533/563 MV74SC374/574, MV74SC534/564	Extensions to family of octal bus circuits equivalent to 74LS TTL

Telecommunications

Telephone dialling - loop disconnect

Each of the circuits in the **MV43XX** family of keypad pulse diallers contains all the logic necessary to interface a 2 of 7 keypad and convert this key information to control and mute pulses simulating a telephone rotary dial. The circuits all store up to 20 digits with redial option and feature wide supply voltage range, low power dissipation, and are available in standard 18-lead ceramic DIL (DG) packages.

MV4320 — KEYPAD PULSE DIALLER

- Pin-for-pin replacement for DF320
- Selectable pulse mark/space ratio 2:1 or 3:2
- Selectable outpulsing rates of 10, 16, 20 or 932Hz
- M1 masking output
- Supply range: +2.5V to +5.5V
- Low power: 375µW at 3V

MV4322 As **MV4320** except M2 masking replaces M1

MV4323 As **MV4320** except selectable interdigit pause (4T or 8T) with fixed 2:1 pulse mark/space ratio

MV4325 — PROGRAMMABLE KEYPAD PULSE DIALLER

- 300Hz keytone output during valid key
- Pulse rate fixed at 10Hz
- Supply range: +2V to +7V
- Lower power: 300µW at 3V
- Programmable access pause
- M1 masking output

MV4326 As **MV4325** except M2 masking replaces M1

Telephone dialling - DTMF or MF4

Plessey Semiconductors offer a complete range of CMOS circuits for the generation, filtering and decoding of Dual Tone Multi-Frequency (DTMF) tones.

The **MV88XX** family of DTMF decoders are designed to operate in conjunction with a DTMF filter (for example the **MV8865**, accepting all 16 DTMF combinations (with excellent voice talk-off performance) and converting then to digital output codes which represent the number originated at the transmitting unit. The **MV88XX** family presents the system designer with a variety of output code formats and facilities from which to choose.

The range of decoders is complemented by the **MV8865** DTMF filter, which filters, separates and squares the dual-tone input to provide High Group and Low Group outputs.

The **MV5087/89** generates the high-accuracy tones required for DTMF transmission.

All these Plessey Semiconductors DTMF circuits feature wide supply range, low power dissipation, contain an on-chip clock oscillator which requires only an inexpensive 3.58MHz crystal and are available in standard DIL packages.

MV8820 — DTMF DECODER

- +5V or +12V to +15V supply
- Low power: 1.5mW at 5V, 18mW at 12V, 30mW at 15V
- Selectable 2 of 8-bit binary or Hex. plus GI AY-5-9100 output codes

MV8860

- +5V or +8V to +13V supply
- Low power: 6.5mW at 5V, 30mW at 12V
- 4-bit binary output

MV8862/3

- +5V or +8V to +13V supply
- Low power: 6.5mW at 5V, 30mW at 12V
- Selectable 2 of 8-bit binary or Hex. output code formats
- **MV8862** and **MV8863** differ only in output code formats

MV8865 DTMF FILTER

- High and low group filtering
- 38dB intergroup attenuation
- +5V or +12V supply
- Logical power down facility
- Low operating power: 6mW at 5V, 60mW at 12V
- Very low standby power: 0.5mW at 5V, 1.5mW at 12V

MV5087/MV5089 DTMF GENERATOR

- +3.5V to +10V supply
- Low standby power: 200µA at 10V supply
- High accuracy tones requiring no trimming
- On-chip regulation of tone amplitudes
- 2nd source MK 5087, 5089

EDP products

CMOS Octal Family

A family of 21 CMOS MSI devices, particularly suited to bus buffering, interfacing, decoding and selecting applications in high speed low power microprocessor and memory subsystems.

Features of this family include: •Improved noise margins with input hysteresis. •High speed (25ns typical tpd), •Low quiescent power (0.5mW typical), •High sink/source current capability (12mA typical), •16 and 20-pin 0.3 inch ceramic DIL (DG) packages, •Pin-for-pin compatible with 74LS series TTL counterparts, •Operating voltage range 3V to 7V.

MV74SC137/8, 237/8, 139/239 DECODERS/DEMULTIPLEXERS

- One of eight with latched/unlatched inputs, inverted outputs **(137/138)**
- One of eight with latched/unlatched inputs, non-inverted outputs **(237/238)**
- Dual one of four with unlatched inputs, inverted/non-inverted outputs **(139/239)**

MV74SC240/244, 241, 540/541 BUFFERS/LINE DRIVERS

- Bi-directional connections, inverting/non-inverting **(240/244)**
- Bi-directional connections, non-inverting, complementary enable **(241)**
- Uni-directional connections, inverting/non-inverting **(540/541)**

MV74SC245/545 TRANSCEIVERS

- Non-inverting/inverting

MV74SC373/573, 533/563 TRANSPARENT LATCHES

- Bi-directional/uni-directional connections, non-inverted outputs **(373,573)**
- Bi-directional/uni-directional connections, inverted outputs **(533/563)**

MV74SC374/574, 534/564 EDGE TRIGGERED D FLIP FLOPS

- Bi-directional/uni-directional connections, non-inverted outputs **(374/574)**
- Bi-directional/uni-directional connections, inverted outputs **(534/564)**

CMOS Interface and Display Driver Family

MV41SC04 QUAD 5V to 12V LEVEL SHIFTER

- High speed
- Latchup protected
- 3-state inverting and non-inverting outputs
- 16-pin ceramic DIL (DG) package
- 3V to 12V operation

MV4330/4331 30-BIT STATIC SHIFT REGISTERS

MV4332 32-BIT STATIC SHIFT REGISTER

- Cascadable static shift registers with true/complement outputs
- Will direct drive four 7-segment LCD displays
- Will direct drive two 16-segment alphanumeric LCD displays
- 40 pin plastic DIL (DP) package
- 3V to 18V operation
- Synchronous reset on **MV4330**

MV4311/MV4368 LATCHED HEX TO 7-SEGMENT LED DRIVER

MV4511 LATCHED BCD TO 7-SEGMENT LED DRIVER

- Bipolar NPN outputs guaranteed at 20mA for bright display
- Direct drive of common cathode LED display
- 16-pin plastic DIL (DP) package
- 3V to 18V operation
- **MV4311/MV4511** have lamp test and blanking inputs
- **MV4368** has ripple blanking for leading zero suppression in multidigit displays

CMOS semi-custom design

Semi-custom techniques enable users to have circuits dedicated to their application without incurring the costs associated with a full custom design. This makes the techniques especially attractive to users with moderate size of production potential. Semi-custom falls into either the **ULA** (Uncommitted Logic Array) in which logic elements are pre-positioned and the design task is to interconnect those elements within the space allocated, or Cell-Based systems where a wider selection of cells is held in a computer library and called up, placed and interconnected by the designer.

Building upon considerable success with **Microcell**, Plessey Semiconductors' N-Channel MOS cell-based layout system, it is now planned to introduce semi-custom techniques in CMOS as follows:

Mid- 1981 A 1400-gate **CMOS ULA** with full design and characterisation information, supporting simulation and checking software.

Fall 1981 **CMOS Microcell** with capability up to 2000 gates
Also add further extensions to the ULA range

Spring 1982 Add two-layer metal to the **ULA** programme.

CMOS full custom design

ISO-CMOS technology

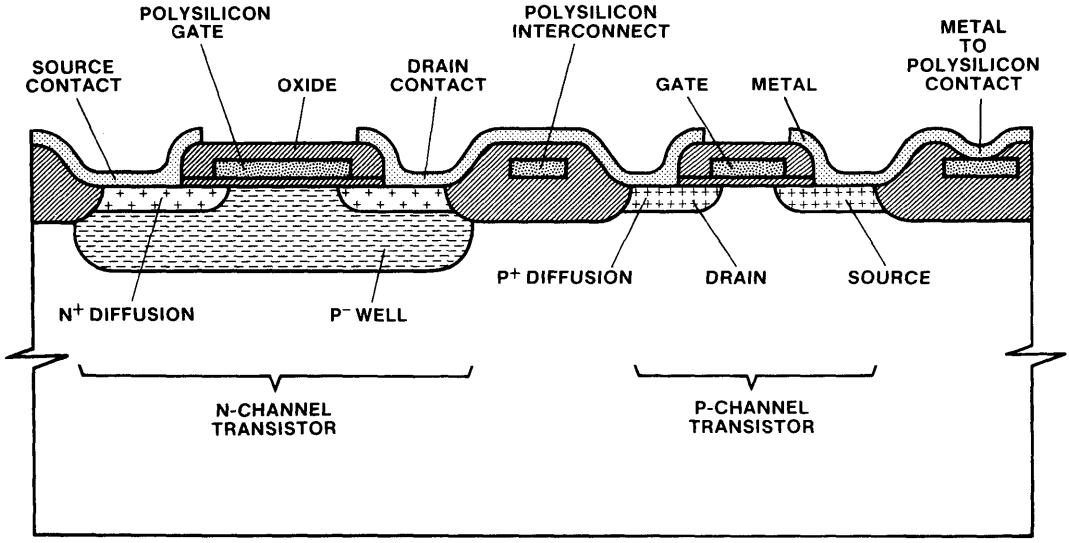
ISOPLANAR—using an oxide-nitride sandwich to define regions for local oxidation, which is recessed by etching away silicon.

REDUCED CAPACITANCE, INCREASED SPEED The recessing technique reduces sidewall capacitance. The process is also self-aligned to reduce overlap capacitance.

ACCURATE CONTROL OF THRESHOLDS Both P-channel and N-channel transistor thresholds are determined by implant levels for precise control.

Process electrical parameters

Parameter	P-channel	N-channel	Unit	Conditions
Threshold voltage,Vbo	0.4 to 0.9	0.4 to 0.9	V	Id=0,Vb=0
Junction breakdown voltage,Vbds	10	10	V	Id=1μA, Vg=Vs=Vb=0
Diffusion resistivity	60 to 120	5 to 12	Ω/□	
1st polysilicon layer resistivity	20 to 70	15 to 40	Ω/□	
2nd polysilicon layer resistivity	30 to 80	30 to 80	Ω/□	



ISO-CMOS, simplified cross-section

RADIO APPLICATION NOTES

Radio Linear Circuits

INTRODUCTION TO SL600 AND SL1600 SERIES

Plessey Semiconductors originally developed the SL600 series for use in military SSB systems. For such applications, hermetic packages and full-temperature operation are necessary: the SL600 series devices meet such specifications. As the range expanded, requirements arose for less expensive versions of SL600 devices and the SL1600 series was introduced. The SL1600 series consists of the same chips as are used in the SL600 series but packaged in plastic DIL packages (mostly 8-lead minidips) tested to less stringent specifications, and supplied with a —30°C to +70°C temperature specification. In a few cases some of the pins present in the SL600 devices are omitted in the SL1600 devices in order to allow a chip previously supplied in a 10-lead TO-5 to be encapsulated in an 3-lead minidip.

SL600 and SL1600 type numbers are used in section headings but to avoid tedious repetition, only the SL600 type numbers will be used in the text unless there are significant differences between the SL600 and SL1600 devices. Pin numbers generally refer to both types; in cases where pin numbers differ, the pin numbers for the SL1600 device is given in brackets, e.g. Pin 6(7).

SL600/1600 PRODUCT RANGE

AMPLIFIERS	SL610 SL611 SL612	SL1610 SL1611 SL1612	140MHz, 20dB 100MHz, 26dB 15MHz, 34dB
MIXERS	SL640 SL641	SL1640 SL1641	
DETECTORS AND AGC GENERATORS	SL621 SL623	SL1621 SL1623 SL1625	AGC from detected audio AMSSB detector and AGC from carrier AM detector and AGC from carrier
AUDIO	SL630	SL1630	200mW headphone amplifier

SL610C, SL611C, SL612C, SL1610C, SL1611C & SL1612C

RF/IF amplifiers

The SL610C, SL611C and SL612C integrated RF amplifiers are similar circuits, having typical voltage gains of 10, 20 and 50 and upper 3dB gain points at 140MHz, 100MHz and 15MHz respectively. The first two draw a supply current of about 15mA at 6V and have some 50dB AGC range while the SL612C draws 3.5mA and has 70dB of AGC. All three are intended to use with +6V supplies and have internal decoupling. They will drive an output signal of about 1V rms.

The cross-modulation of the circuits is 40dB down on signal at 1V rms output with no AGC, and at 250mV rms input with full AGC. The input and output admittances of the circuits are not greatly affected by AGC level.

CIRCUIT APPLICATIONS

There are seven connections to each circuit: an input, an input bias point, an AGC input, the output, the positive supply pin and two earths — for input and output respectively.

The positive supply should be 6V, but the devices will function at supplies of up to 9V. Since internal HF supply decoupling is incorporated a certain amount of HF ripple can be tolerated in the supply. LF ripple should be kept down as it can cause intermodulation — especially at large HF signal levels — and 10mV rms of LF ripple should be considered a maximum.

The AGC characteristic is shown in Fig. 1. It is temperature dependent, so that while a potentiometer may be used to provide a gain control voltage the gain so defined will not be temperature stable to better than ± 2dB. The AGC terminal will normally draw about 200 microamps at 5V — in some SL610C and SL611C devices this may be as high as 600 microamps.

There are two earth connections: pin 4 is the input earth and pin 8 the output earth. When several devices are cascaded pin 8 of one stage and pin 4 of the next should have a common earth point — also high common earth impedances to pin 4 and pin 8 of the same device should be avoided. Fig. 2a shows a circuit where common earth impedance could cause instability and Fig. 2b shows one where the input and output signals have correct point earthing. If extra supply decoupling is used the capacitor should ground to the output earth point. The can should be separately earthed in applications at VHF or in the presence of a large RF field.

The input bias point (pin 6) is normally connected directly to the input (pin 5) and the signal applied through a capacitor but occasionally, when the signal is obtained from a tap on a coil, the arrangement in Fig. 2b may be used to give slightly improved noise performance. C_D is a decoupling capacitor. The SL610/611 noise figure is approximately 4dB at 300 ohms source impedance and 6dB at 50 ohms and at 2.5 kilohms the noise figure for the SL612 is 3dB at 800 ohms source impedance.

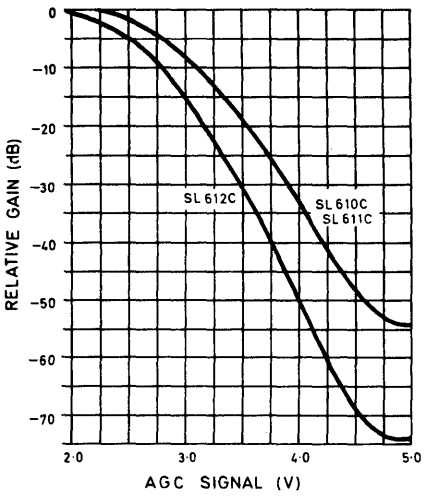


Fig. 1 SL610/11/12 AGC characteristics

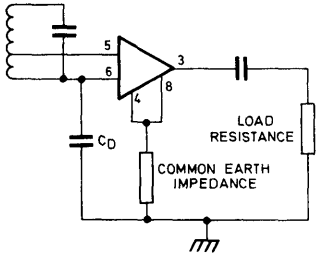


Fig. 2(a) Incorrect connections of earths

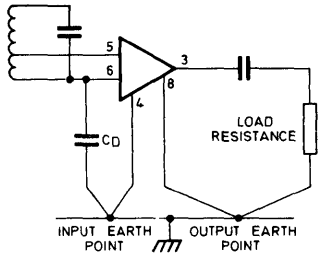
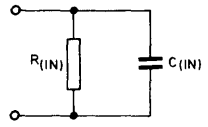
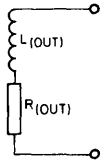


Fig. 2(b) Correct connection of earths



(a) input circuit



(b) Output circuit

Fig. 3 Equivalent circuits

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output respectively are shown in Figs. 3a and 3b and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Figs. 4 and 5. It will be seen that for the SL610C and the SL611C, R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL612C, R_{in} is not negative and R_{out} is negative only below 700kHz.

If an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and if R1 is higher than R_{in}. Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input is inductive, therefore, it may be shunted by a 1k resistor; where the load is capacitive, 47 ohms should be placed in series with the output.

Suitable input arrangements for the amplifiers are shown in Fig. 2b and Fig. 6. The method shown in Fig. 6a is representative of all inputs — the input and bias points are directly-connected and the signal is coupled via a capacitor. If the input is inductive the 1k resistor shown in Fig. 6b may be required, although usually it can be omitted. If a crystal filter is used it should be correctly terminated, allowing for the impedance of the IC, and coupling made via a capacitor.

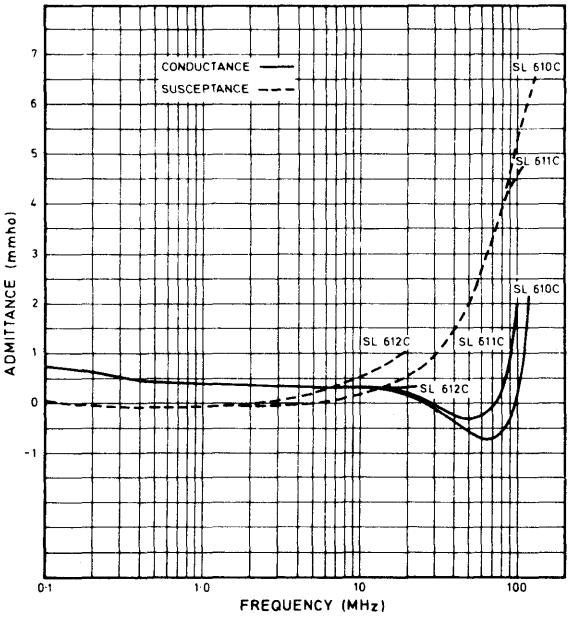


Fig. 4 Input admittance with o/c output (G_{11})

The output is a voltage source, with the impedance characteristics mentioned above. Output coupling is via a capacitor, with a series resistor if necessary to preserve stability (Fig. 6c). If a current output to a tuned circuit is required the arrangement in Fig. 6d is suitable, using almost any small signal NPN transistor with an f_T of over 300MHz and low C_{OB}. To drive particularly low impedances, e.g. a 50 ohm coaxial cable, this impedance should be increased somewhat by a series output resistor (say, 100 ohms) as, if the output is loaded directly by low impedance, most of the negative feedback will be removed — with consequently poor linearity and constancy of gain. Examples of the use of these amplifiers are shown in Fig. 7.

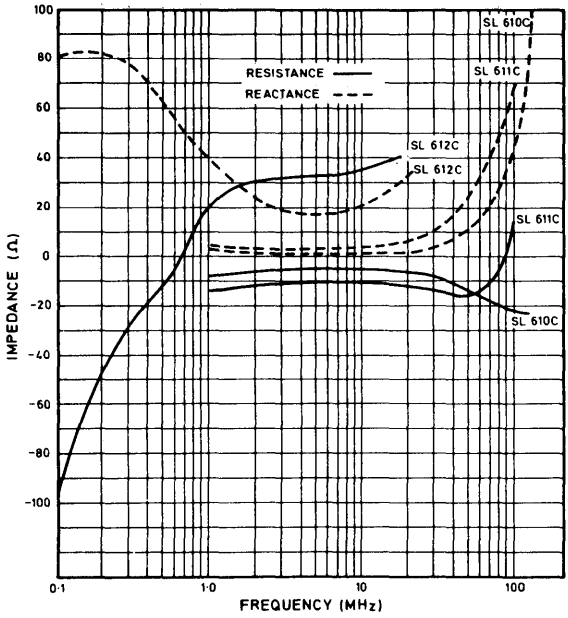


Fig. 5 Output impedance with s/c input (G_{22})

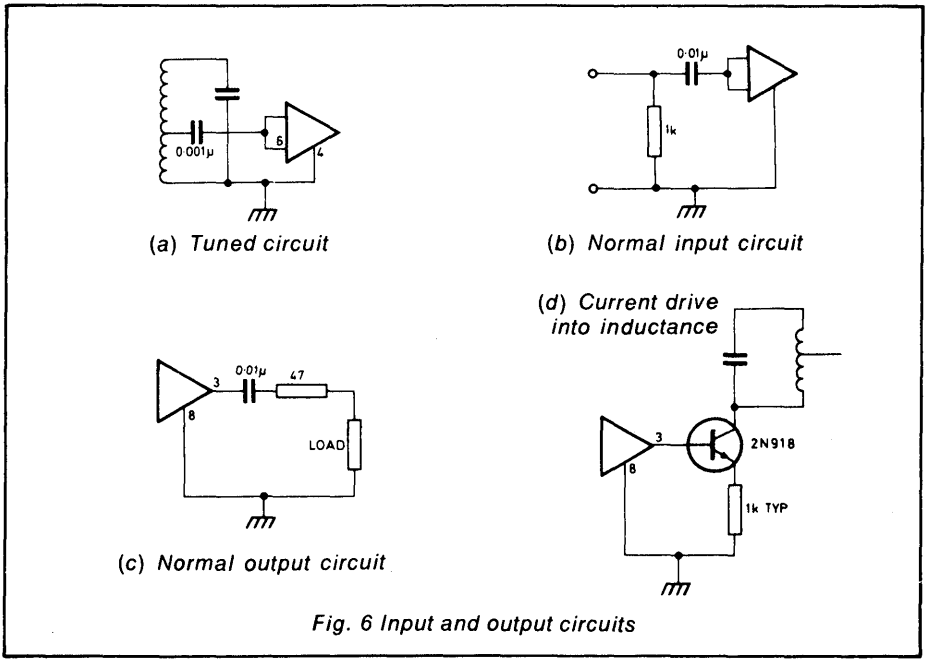
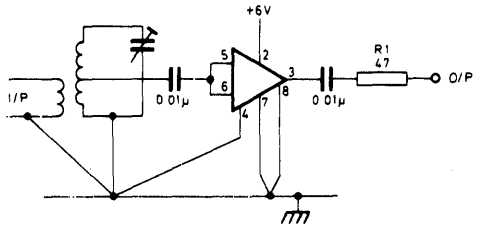
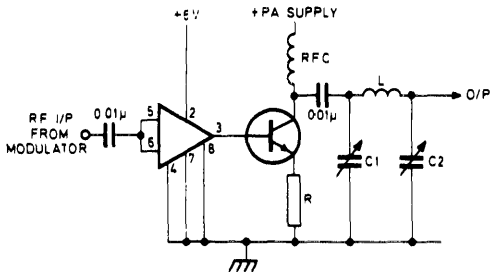


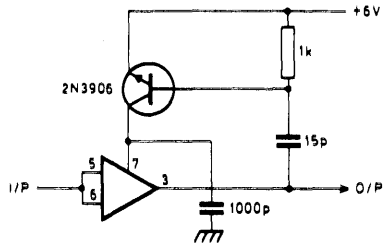
Fig. 6 Input and output circuits



(a) *RF preamplifier. Use SL610C up to 140MHz, SL611C up to 70MHz, SL612C up to 12MHz. R1 may be omitted if the load is neither capacitive nor very low impedance.*



(b) *Linear power amplifier for low power SSB transceivers. L, C1 and C2 form the output π tank circuit. The values of PA supply and R should be chosen to suit the transistor used. C_{ob} should be as low as possible.*



(c) *Constant level RF amplifier stabilising at approximately 500mV rms output over a range of inputs greater than 20dB. SL610C, 611C or 612C may be used. With tuned feedback, this circuit makes an excellent constant level oscillator.*

Fig. 7 SL610/11/12

Double balanced modulators

PRINCIPLES OF OPERATION

A simple double-balanced modulator is shown in Fig. 8 . It is evident that the sum of the two output currents equals the tail current and that, from considerations of symmetry, if either V1=V2 or V3=V4 then I1=I2. Also if R is much greater than R_e the collector currents of TR1 and TR2 will differ by an amount proportional to the difference between V1 and V2. If, therefore, a small input at frequency f_1 is applied between V1 and V2 and a large signal at f_2 is applied between V3 and V4, sufficient to turn the transistors TR3, TR3, and TR4, and TR4, fully on and off, it is evident that switching modulation, similar to that of a diode ring will occur and frequencies $|f_1 \pm f_2|$ will occur at the output as will sums and differences of f_1 and the odd harmonics of f_2 i.e. $|f_1 \pm 3f_2|$, $|f_1 \pm 5f_2|$, etc.

CIRCUIT DESCRIPTION AND APPLICATIONS

The circuits of the SL640C and SL641C are very similar but have different signal input and output configurations — these are fully discussed below.

The circuits require a single, well-decoupled positive supply of between 6 and 9 volts and consume about 12mA. Pin 2, an internal bias point, must also be decoupled by a low-leakage (less than 100nA) capacitor having a low reactance at the lowest signal or carrier input frequency.

Pin 1, which is connected to the can, should be earthed to prevent HF pickup.

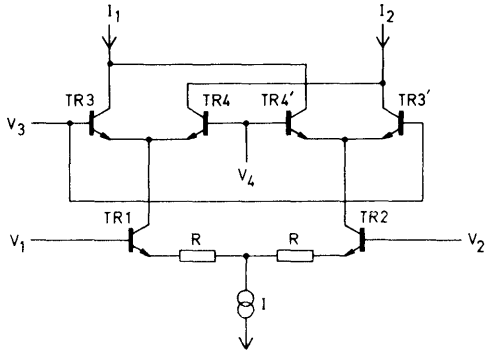


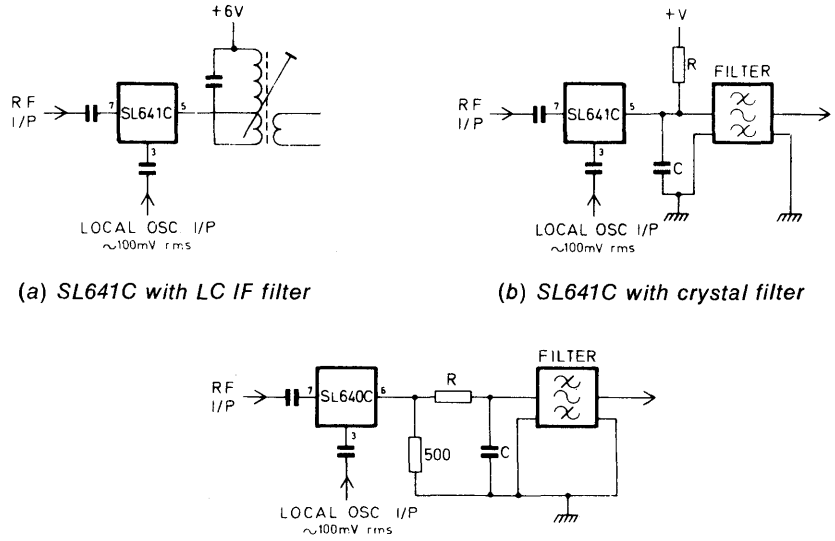
Fig. 8 A transistor double-balanced modulator

The input and carrier signals, which should not exceed 200mV rms, are applied to pins 7 and 3 respectively. Both the SL640C and the SL641C have a carrier input impedance of 1 kilohm and 4pF and the SL641C has a similar signal input impedance. The signal input impedance of the SL640C is 500 ohms and 5pF. The input coupling capacitors should have a leakage of less than 100nA and an impedance of less than 100 ohms at the lowest frequency they will carry. This should be reduced to less than 10 ohms above 10MHz.

The output of the SL641C is intended as a current drive to a tuned circuit. If both sidebands are developed across this load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course, increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output, which requires a discrete load resistor of not less than 560 ohms. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

The circuits will operate with input frequencies between 1Hz and 70MHz with the specified performance; the SL641C will operate at up to about



(a) *SL641C with LC IF filter*

(b) *SL641C with crystal filter*

(c) *SL640C with crystal filter*

Fig. 9 SL640/41C receiver mixer circuits

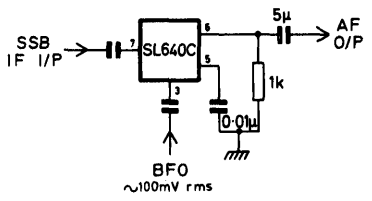
150MHz with reduced performance. To use them at frequencies below 100Hz precautions must be taken to prevent leakage in the input coupling capacitor from altering the device bias.

Some applications of the SL640C and SL641C are shown in Figs. 9 and 10 Power, decoupling, and earth connections are not shown.

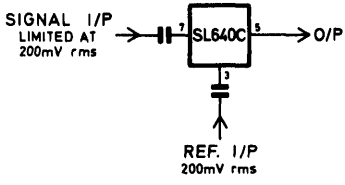
Fig. 9a shows the SL641C used as a receiver mixer driving a wound IF coil. Fig. 9b shows it driving a crystal filter. R and C must be selected to match the filter. If R is less than 800 ohms it may be connected to the +6V line supplying power to the SL641C; if it is between 800 ohms and 1.8 kilohms it should be connected to +9V (while the SL641C supply must remain at +6V). If R is greater than 1.8 kilohms the circuit in Fig. 9b is unsuitable and the SL640C circuit illustrated in Fig. 9c should be used.

The SL640C and SL641C have a noise figure of about 10dB at 100 ohms source impedance. When used as receiver mixers they have better than —40dB intermodulation products so long as unwanted signals do not exceed 30mV rms. Thus, either can be used as a receiver mixer at HF without an RF amplifier since atmospheric noise will far exceed device noise at these frequencies if the antenna is reasonably good. If an SL610C RF amplifier is used the intermodulation threshold will be reduced to 3mV rms (since the SL610C has a gain of 10). The SL640/41 is then less attractive as a mixer and a diode ring mixer should be used.

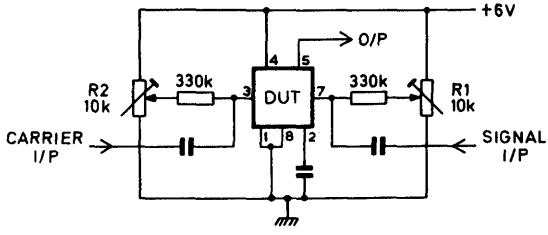
Fig. 10a shows the SL640C used as an SSB detector. The capacitor connected to output pin 5 decouples the sum frequency $|f_1 + f_2|$, while the audio difference frequency $|f_1 - f_2|$ is taken from pin 6. The phase comparator shown in Fig. 10b is more useful — it may be used as a detector for phase modulated signals or as a comparator in phase-locking systems such as frequency synthesisers.



(a) *SL640C SSB detector*



(b) *SL640C phase comparator*



(c) *Signal and carrier leak adjustment*

Fig. 10 SL640/41C detector circuits

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig. 10c. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

Fig. 11a shows the SL640C or SL641C used as a sideband generator. Both sidebands are produced so that if a single sideband is required it must be obtained by subsequent filtering (Fig. 11b). If pin 2 is earthed by a resistor of about 15 kilohms (its actual value may need to be selected) the device's carrier leak is increased to a point where the DSB signal becomes AM. This is useful where it is desired to select sideband or AM. In the circuit shown in Fig. 11c a single sideband only is produced. It is important that both the audio and carrier reference and quadrature signals should be accurately 90 degrees out of phase. The amplitude of one phase of audio should be adjusted to obtain maximum second sideband rejection.

If the carrier reference is connected to input A, and the carrier quadrature to input B, LSB output results. If the carrier quadrature is connected to input A, and reference to input B, USB output results.

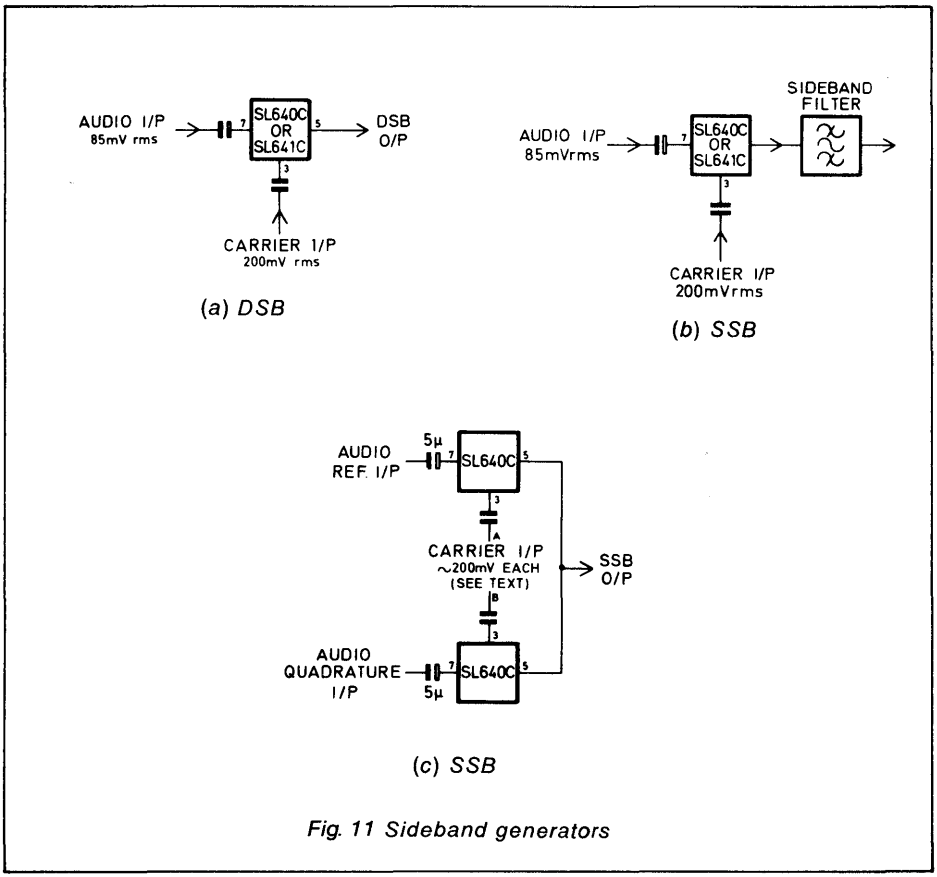


Fig. 11 Sideband generators

SL621C & SL1621C

AGC generators

The SL621C is an audio-operated AGC generator designed for use with the SL610/11/12 RF amplifiers in SSB receivers.

An ideal single sideband AGC generator must set the AGC rapidly when a new signal appears and follow a rising or fading signal but, if the signal disappears altogether (as in pauses in speech), retain the AGC level until the signal recommences. If the signal remains absent for more than a preset time, however, the system should rapidly revert to full gain. The SL621C will perform these functions and will also produce short-lived pulses of AGC to suppress noise bursts.

CIRCUIT DESCRIPTION

The operation of the circuit is described with reference to Fig. 12, which also illustrates the dynamic response of a system controlled by an SL621C AGC generator.

The SL621C consists of an input AF amplifier, TR1-TR4, coupled to a DC output amplifier, TR16-TR19, by means of a voltage back-off circuit, TR5, and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

An audio signal applied to the input rapidly establishes an AGC level, via TR14, in time t_1. Meanwhile the long time constant detector output (TR15) will rise and after t_3 will control the output because this detector is the more sensitive. If the signals at the SL621C input are greater than approximately 4mV rms they will actuated the trigger circuits TR6-TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate which corresponds to a rise in receiver gain of 20dB/sec. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as in pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector (TR14) falls to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, thus holding off TR12 via TR11. When the pulses cease, C3 discharges and after t_5 turns on TR12, rapidly discharging C2 (in time t_4) thus restoring full receiver gain. The hold time, t_5, is approximately one second with C3=100 microfarads. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses. Fig. 12 also shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

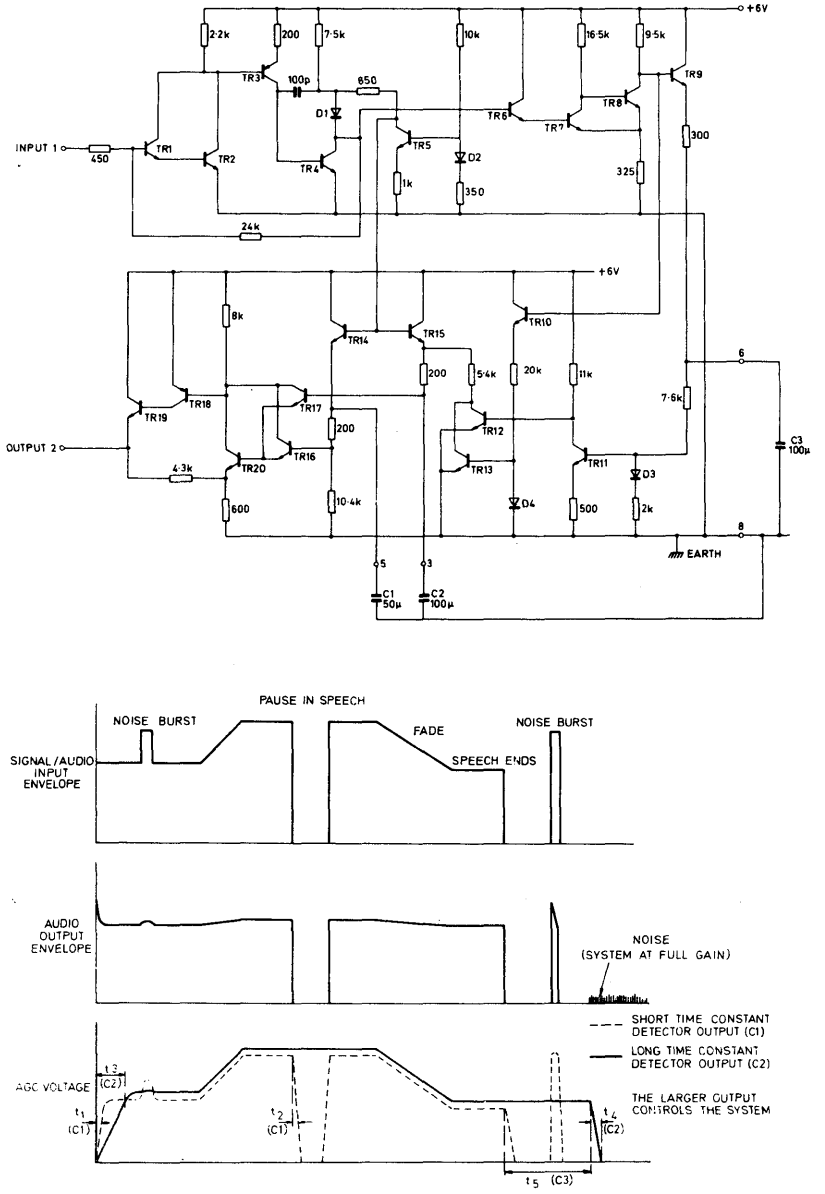


Fig. 12 Circuit diagram of SL621C and dynamic response of an AGC system controlled by an SL621C

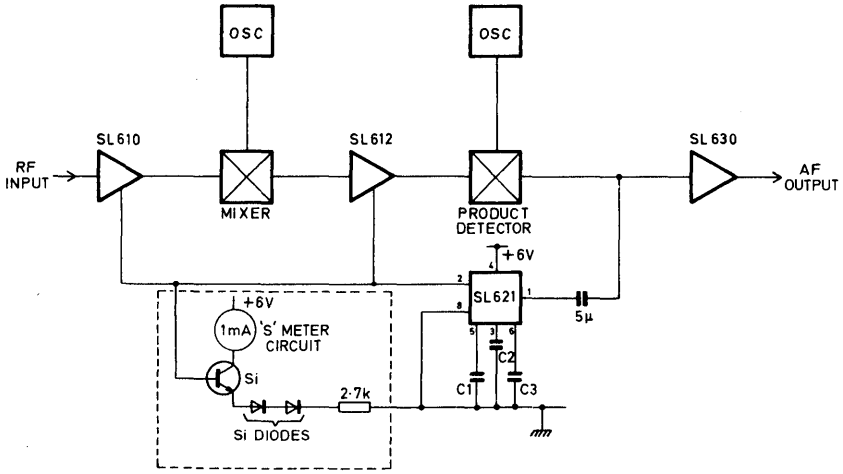


Fig. 13 An SL621C used to control an SSb receiver

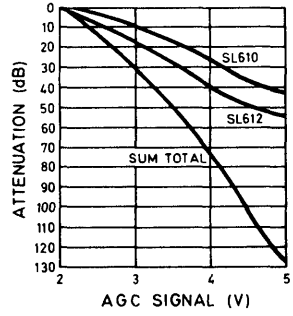


Fig. 14 Attenuator AGC signal

The various time constants quoted are for C1=50 microfarads and C2=C3=100 microfarads. These time constants may be altered by varying the appropriate capacitors.

CIRCUIT APPLICATIONS

The SL621 is used in an SSB receiver as shown in Fig. 13. AGC need only be applied to two of the gain stages even if there are more than two such stages in the receiver since AGC applied to two stages only will result in over 120dB AGC range. It is usual to apply AGC to the first RF stage and the first IF stage and it will be seen from Fig. 14 that an SL612 IF amplifier reacts earlier to an increasing AGC voltage than an SL610C RF amplifier. This has the effect of delaying the AGC to the input stage, thus improving the receiver signal to noise ratio at low AGC levels.

Fig. 14 also shows the total attenuation to be expected at any AGC voltage when AGC is applied to one SL610C and one SL612C in a system; from this one can calculate the calibration of an 'S' meter for use with the SL621C. Such a meter, as shown in Fig. 13, should have a sensitivity of 2.6V FSD and be calibrated linearly from 0 to 120dB.

The output current capability of the SL621 is not high and it should not be expected to drive more than three SL610/11/12 devices in addition to an 'S' meter circuit similar to that shown in Fig. 13.

There are two other important points to observe when using the SL621C: supply de-coupling and input coupling. Since capacitors C1 and C3 may need to charge very quickly, the source impedance of the 6V supply line at low frequencies should be very low, if necessary being decoupled by a low impedance 1000 microfarad capacitor placed near the SL621C.

The input should be applied to pin 1 via a capacitor of not more than 470 ohms reactance at the lowest input frequency encountered, and should never exceed 1Vrms. Input voltages in excess of this level may cause the internal amplifier to block, with consequent failure of the AGC voltage. The condition can be avoided, if necessary, by using a diode limiter at the input.

In the presence of RF fields the AGC line may need to be decoupled: a 5000pF capacitor from pin 7 of each RF amplifier to earth and a 100 ohm resistor from each pin 7 to the AGC line should be adequate. It is, however, important not to use a capacitance greater than 15000pF, otherwise the impulse suppression characteristic of the circuit will be degraded.

The SL621 may be used with supply voltages between +6V and +9V.

SL623C, SL1623C & SL1625C

AM detector, AGC amplifier and SSB demodulators

The SL623C consists of an AM detector, an SSB detector and an AGC generator designed for use with AM. The SL623C was introduced to enable the small-signal sections of an HF AM/SSB transceiver to be completely integrated — all functions with the exception of the power amplifier can be realised with SL600 series integrated circuits. The outputs of the SL623C will drive most audio output stages with input impedances over 10 kilohms, and are particularly suitable for driving the SL630C.

In addition to its audio outputs, the SL623C AGC generator is designed to control SL610/11/12 RF/IF amplifier strips, but, unlike the SL621C AGC generator, which operates from an audio signal, the SL623C control voltage is carrier-derived. It is therefore less suitable for use with SSB or CW. However, the AGC output pins of an SL621C and an SL623C may be connected together for an SSB/AM receiver, the gain then being controlled by the device with the higher output voltage.

The SL1625C is an SL1623C without its SSB detector.

CIRCUIT DESCRIPTION (Fig. 15)

The IF input is applied directly to one input of a full-wave detector and, via a unity-gain inverting amplifier, to the other input of the full-wave detector and to the signal input of a balanced demodulator. Two outputs from the full-wave detector are brought out of the package: audio and AGC. The AGC signal is used as the input to the AGC amplifier of the device. The AGC amplifier consists of two amplifiers in series. The first has a gain which may be varied between —0.25 and —5 by an external resistor and the second has a fixed gain of —20 and a frequency compensation point. The SSB detector, which requires a carrier input of 100mV rms, consists of a simple balanced demodulator.

A single positive supply of between +6V and +9V is required. The supply should be decoupled close to the can by a 0.1 microfarad capacitor. Current consumption is approximately 10mA at 6V supply and zero AGC voltage, but rises with both supply voltage and AGC output level.

CIRCUIT APPLICATIONS

AM Detector

The detected AM output has an output impedance of about 1 kilohm and should be decoupled at RF with a 0.01 microfarad capacitor (C1). It should be connected to the audio stage via a dc blocking capacitor. The other detector output is similar but should be decoupled with a 50 microfarad capacitor (C2) to remove AF, and connected via a preset potentiometer R28 to the AGC amplifier input to provide rectified carrier for amplification as AGC. C1 and C2 should be connected directly to the earth pin via the shortest possible leads, which should not be common to any other components. C2 should have an AF series resistance of under 1 ohm and, if it does not also have a low RF impedance, should be shunted by a 0.01 microfarad RF bypass capacitor (C3). These measures prevent instability due to possible RF current loops.

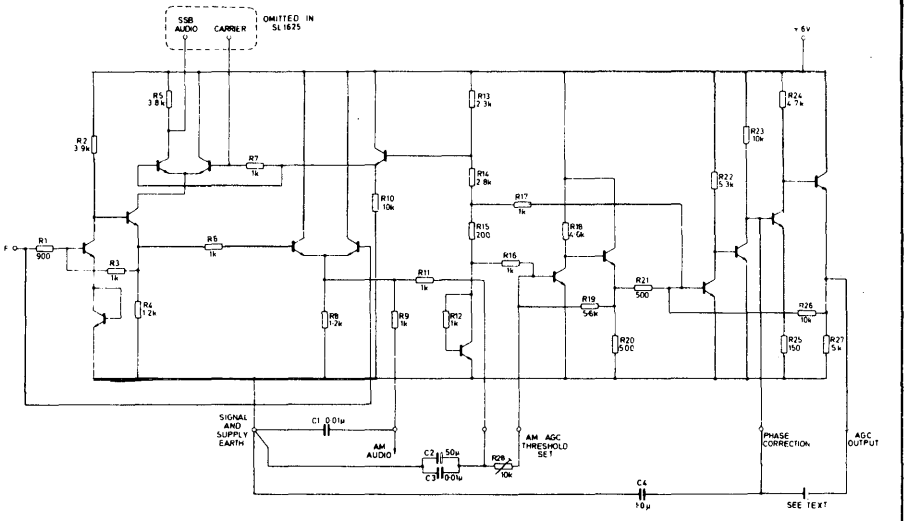


Fig. 15 SL623C circuit diagram

AGC Generator

Pin 3, the AGC amplifier phase correction point, should be decoupled to ground by a 1 microfarad capacitor (C4) ,keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

A capacitor connected to the phase correction point and the output of the AGC amplifier helps to reduce the ripple on the AGC output. Its value varies from system to system and with intermediate varying frequencies. Normally-used values vary between 0.1 and 10 microfarads. As there is no easy way to predict suitable values for particular systems, this component must be 'selected on test'.

The AGC output (pin 4) will drive at least two SL610/11/12 amplifiers and the 'S' meter circuit shown in Fig. 13. The SL623 AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623C will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from the SSB to the AM detector.

Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets different filters are used for AM and SSB; these will also need to be switched.

The 10 kilohm gain-setting preset potentiometer R28 is adjusted so that a DC output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL623C for a 4dB increase in input. A fixed resistor of 1.5 kilohms can often be used instead of the potentiometer.

SSB Demodulator

The carrier input is applied to pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the DC level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01 microfarad capacitor. The output impedance of the detector is 3 kilohm and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs — no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting the SL623C to the SL621C via a 2 kilohm resistor in series with a 0.5 microfarad capacitor.

Input Conditions

The input impedance is about 800 ohms in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the DC bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

SL630C & SL1630C

Microphone/headphone amplifier

The SL630C is an audio amplifier having 40dB gain and an internal gain control of approximately 60dB, and an output capability of 200mW into a 40 ohm load when used with a 12V supply.

CIRCUIT DESCRIPTION AND APPLICATIONS

To maintain HF stability — particularly on negative half-cycles — the output (pin 1) should be decoupled by a 1,000pF, low series inductance, capacitor placed directly between pins 1 and 10 (8) with leads cut as short as possible. This component must be on the integrated circuit side of the output coupling capacitor. At high supply voltages and/or low temperatures 10 ohms must be placed in series with this capacitor and 100pF connected from pin 4 to earth. The output is coupled to its load with a capacitor of a low impedance relative to the load at the lowest frequency to be used. The load may be resistive or reactive and, for maximum power output, should lie on the load/supply voltage line. *Any higher value of load impedance is quite safe but the device will over-dissipate and eventually destroy itself by overheating if the output is short-circuited.* The optimum load therefore, at any rate with supplies of over 9V, can be regarded as a safe minimum. The circuit shown in Fig. 16 which shows the SL630C used as a headphone amplifier, may also be used with loudspeakers having suitable impedances. The distortion is about 0.5 per cent at full output.

The power supply, to pin 2, should be between +6V and +12V and adequately decoupled both at HF and LF. The quiescent power consumption at various supply voltages is shown in the Power characteristics, as is the relation of the supply voltage to the optimum load and the maximum power available.

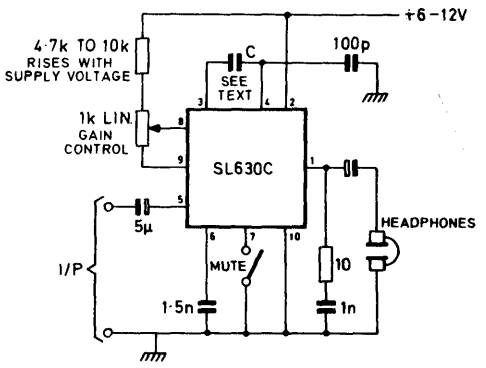


Fig. 16 Headphone amplifier using the SL630C

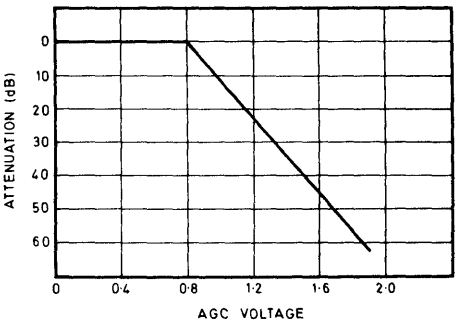


Fig. 17 AGC characteristics

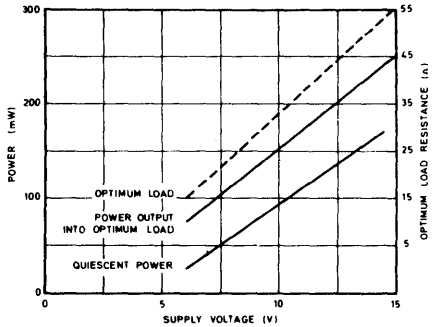


Fig. 18 Power characteristics

A capacitor connected to pins 3 and 4 defines the high frequency response of the amplifier. The upper 3dB frequency, f, is given by the formula:

$$f = \frac{16000}{C+20} \text{ kHz. (C is in picofarads)}$$

Pins 5 and 6 are input terminals. They may be used together as a differential input, in which mode they present an impedance of approximately 2 kilohms and result in a voltage gain (without gain control) of 100 (40dB). When the input is obtained from a magnetic transducer or a transformer it is desirable to use the differential input mode since the signal winding may be connected directly between pins 5 and 6 and no other components are required.

An input may also be applied between pin 5 and earth. In this case the gain is 200 (46dB) and the input impedance 1 kilohm. Pin 6 should be earthed by 1500pF. A coupling capacitor is required between the input and pin 5.

The circuit is muted by earthing pin 7. A muted circuit attenuates an input by about 100dB. There is no mute facility on the SL1630.

Gain control is applied to pin 8, (7) which has an input impedance of 3.6 kilohms. It must be appreciated that even with full gain control the input cannot exceed 50mV rms without clipping so that at high control levels the output level is limited. The AGC characteristics will vary with temperature but, as shown in Fig. 16 a potentiometer to give manual gain control can be connected to the internal bias point at pin 9 which provides a temperature-compensated reference at the voltage at which gain control commences. This reference pin is omitted on the SL1630C. Pin 10 (8) is the signal earth and negative power supply connection.

Applications

The first part of this handbook describe Plessey Semiconductors' range of integrated circuits for Radio Communications and general techniques of using them. This section describes a number of specific applications of these circuits which have been developed at various times in our Applications Laboratory.

These applications cover receivers and transceivers of several types and some frequency synthesisers. Some of these applications have been developed in great detail and are engineered practically to pre-production status, others are merely ideas which have been shown to be practical but have not been taken further.

An AM receiver using SL1600 circuits

This receiver is a single conversion superhet using SL1600 devices with an IF of 455kHz. It was designed for use in 27MHz CB receivers, possibly following another conversion to a first IF of about 10.7MHz. The receiver has a sensitivity of about 1 microvolt and delivers 3 watts to an 8 ohm loudspeaker.

The block diagram of the receiver is shown in Fig. 60. It consists of a normal single conversion superhet with a 455kHz intermediate frequency. An SL1641 double-balanced modulator acts as a mixer and is followed by a ceramic ladder filter with a $\pm$3kHz passband.

The intermediate frequency amplifier consists of three SL1612 amplifiers with a simple interstage ceramic filter between the second and third stages. This amplifier has a gain of over 100dB and AGC is applied to all three stages. It is followed by an SL1623 detector which also provides AGC.

The AGC line may be fed to an external 'S' meter and also goes to an SL748 used in a squelch system. After passing the squelch gate the audio goes to a TBA800 3-watt amplifier.

Fig. 61 is a detailed circuit diagram of the receiver.

THE MIXER

The mixer consists of an SL1641 double-balanced modulator. The SL1641 has a free collector output which is used to drive a 2 kilohm resistive load to provide the correct match to the Murata CFR 455H ceramic filter.

The SL1641 is intended to drive a load with a DC resistance which does not exceed 800 ohms. To prevent saturation of the output transistors of the SL1641, the 2 kilohm resistor must be connected to a +12V supply while the SL1641 itself runs from +6V. Furthermore, it is essential to decouple the supply to the 2 kilohm load most throroughly to prevent IF feedback via the supply line.

This mixer has several advantages — it has a conversion gain of 9dB (which is sufficient to overcome the loss of a CFR 455H filter), a low noise figure, and it requires only 200mV rms of local oscillator injection. It has a signal input impedance of 1 kilohm in parallel with 5pF, which means that it can be driven from a ceramic filter in dual conversion receivers. The local oscillator port also has a high input impedance: 1 kilohm in parallel with 4pF.

The other feature important in a receiver mixer is intermodulation. While the SL1641 cannot compete with hot carrier diode or FET ring mixers, it has considerably better performance than the transistor or FET mixers generally used in Citizens' Band receivers. Its third order intercept point is around +8dBm.

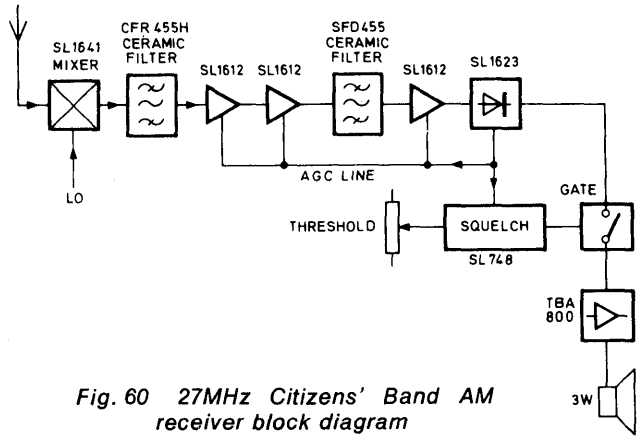


Fig. 60 27MHz Citizens' Band AM receiver block diagram

THE IF AMPLIFIER

The IF amplifier consists of three cascaded SL1612s, giving a maximum gain of over 100dB. Since SL1612 amplifiers are broadband devices, a 100dB untuned strip would have over 20mV of broadband noise at its output, and any local oscillator signal getting through the first filter would be amplified. Extra filtering is therefore necessary, and is provided by a simple SFD 455 between the second and third stages.

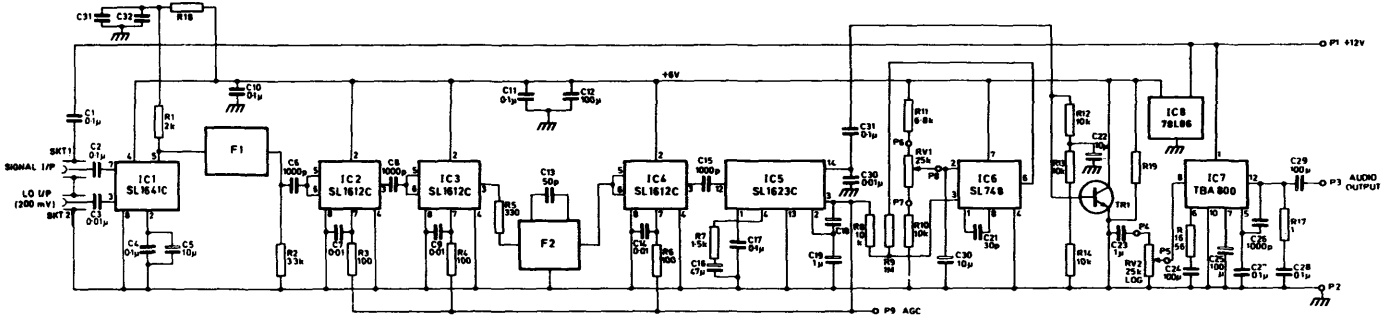
Although the three SL1612s have a maximum gain of over 100dB, the IF strip is stable without any particular precautions — provided that the supply rail is adequately decoupled and the ground layout is adhered to. The receiver may be built on single-sided circuit board without trouble or it may be built on ground-plane double-sided board, in which case both sides of each integrated circuit ground connection must be soldered.

AGC is applied to all three stages. This is not absolutely necessary since two stages will give 140dB gain control range but it is better to have distributed AGC. If AGC is applied to only two stages it should be applied to the first two.

This IF amplifier has excellent performance and uses few discrete components. Although the integrated circuits are more complex than the discrete transistor equivalent, the saving in tuned circuits, discrete components, and adjustment makes the integrated circuit amplifier far superior in both performance and cost.

THE DETECTOR AND SQUELCH

The detector consists of an SL1623. The circuit detects AM and provides carrier-derived AGC which may also be used to drive an 'S' meter. The 'S'



Resistor values are in ohms, capacitor values in microfarads unless otherwise stated.

IC1	SL1641C	R13	10k	C14	0.01	SKT1	Signal input
IC2	SL1612C	R14	10k	C15	1000pF	SKT2	LO input (200mv)
IC3	SL1612C	R15	1k	C16	47 TANT		
IC4	SL1612C	R16	56	C17	0.1	P1	+12V supply
IC5	SL1623C	R17	1	C18	0.1 TANT	P2	Ground
IC6	SL748C	R18	100	C19	1 TANT	P3	Audio output
IC7	TBA800	R19	10k	C20	0.01 TANT		
IC8	78L06	C1	0.1	C21	30pF	P4 }	Volume control
R1	2k	C2	0.01	C22	10 TANT	P5 }	
R2	3.3k	C3	0.01	C23	1 TANT	P6 }	
R3	100	C4	0.1	C24	100 TANT	P7 }	Squelch control
R4	100	C5	10 TANT	C25	100 TANT	P8 }	
R5	330	C6	1000pF	C26	1000pF	P9	AGC line
R6	100	C7	0.01	C27	0.1	VR1	25k lin squelch control
R7	1.5k	C8	1000pF	C28	0.1	VR2	25k log volume control
R8	10k	C9	0.01	C29	100 TANT	T1	Small sjgnal audio si NPN
R9	1M	C10	0.1	C30	10 TANT	F1	455kHz Murata ladder filter boards
R10	10k	C11	0.1	C31	0.1 TANT		will accept CFS, CFR or CFM types.
R11	6.8k	C12	100 TANT	C32	10 TANT		Recommended is CFR 455H.
R12	10k	C13	56pF			F2	Murata SFD 455D

Fig. 61 27MHz Citizens' Band AM receiver circuit diagram

meter should consist of a voltmeter with a 2V offset reading from 2V (no deflection) to 3.5V (full deflection). It should not draw more than 600 milliamps and should be calibrated linearly.

The AGC is also applied to an SL748 operational amplifier which is used as a squelch circuit. The SL748 is connected as a trigger circuit with a variable threshold so that, as the AGC output rises past the threshold, the squelch output goes high. This high output applies bias to an emitter follower in the audio line which allows the detected audio to pass, via the volume control, to the output stage.

The squelch output may also be used to turn on a lamp to indicate the presence of a signal.

The SL1623 is an AM and SSB detector and has 14 pins. As the SSB facility is not needed it may be replaced by the SL1625 — a version of the SL1623 without the SSB facility and encapsulated in an 8-lead minidip.

THE OUTPUT STAGE

The output stage uses standard 3 watt integrated circuit output stage which will drive an 8 ohm loudspeaker.

POWER SUPPLIES

The mixer and the output stage require a +12V supply, the rest of the circuits a +6V supply. The +6V supply is obtained from the +12V supply with a 78L06 voltage regulator.

LAYOUT

The layout and component placing of the prototypes of this receiver are shown in Figs. 62a and 62b. Other layouts may be used to occupy available space, but two considerations are necessary — the mixer and IF strip should be separated as much as possible (at least 2cm), and the topology of the IF strip layout should be retained to prevent ground loop instability.

PERFORMANCE

The overall performance of this receiver depends on the system in which it is used. Dual conversion systems have good image and spurious performance but single conversion systems have better intermodulation performance. In this performance summary parameters influenced by the external design are therefore ignored.

In the Citizens' Band service at 27MHz the noise figure of a receiver is less important than its strong signal performance. This receiver has a sensitivity of 1 microvolt at the SL1641 input for a 20dB S/N ratio, which is adequate, and a third order intercept point of +8dBm. Its dynamic range is well over 100dB.

On standby the power consumption is about 600mW, although this rises during periods of high audio output.

Receiver passband and adjacent channel rejection depend on the filter used — with a CFR 455H the passband is ±3kHz and adjacent (±10kHz) channel rejection is 65dB.

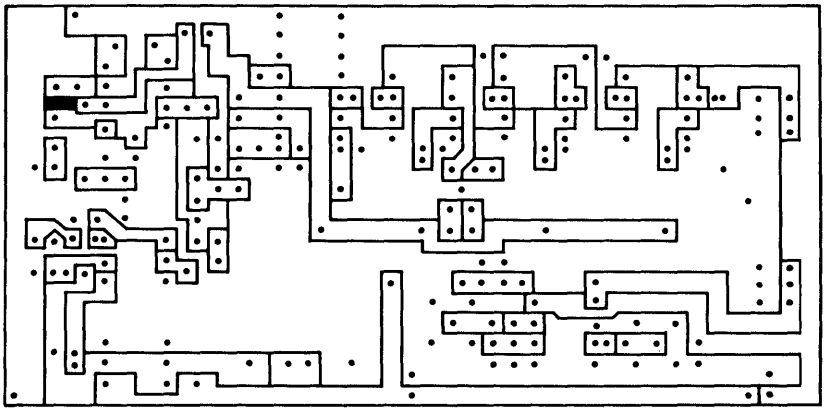


Fig. 62a Printed circuit layout for SL1600C AM Citizens' Band receiver. Scale 1:1

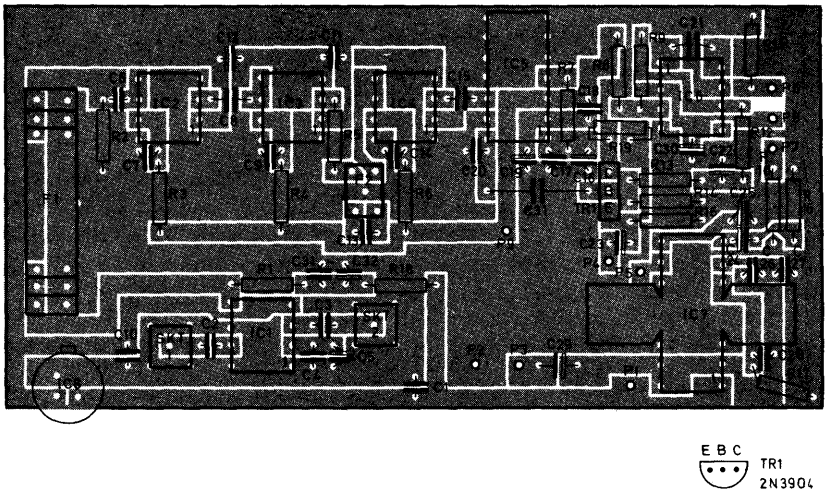


Fig. 62b Component layout for SL1600C AM Citizens' Band receiver. Scale 1:1

Simple SSB transceiver

SL600 VERSION

This transceiver, shown in Fig.63, consists of a single conversion superhet receiver with a 9MHz IF and a very efficient audio-derived AGC system, and a filter type SSB generator, also working at 9MHz. Audio AGC in the modulator path gives constant level output. The transmitter and receiver are arranged so that no signal switching is required between transmit and receive, and the RF components are common to both.

The RF input is direct to an Anzac MD-108 (or similar) hot carrier diode ring mixer. This has 50 ohm ports and is also driven by the local oscillator, at about +7dBm (500mV). The output is connected via a 3: 1 step-up transformer to a 9MHz crystal filter. This filter has the 2.4kHz bandwidth required for SSB and a 90dB stopband. Filters with 60dB stopband can be used, but additional filters may be required at low local oscillator frequencies to keep the local oscillator signal out of the IF amplifier (and the overall receiver performance will, of course, be degraded).

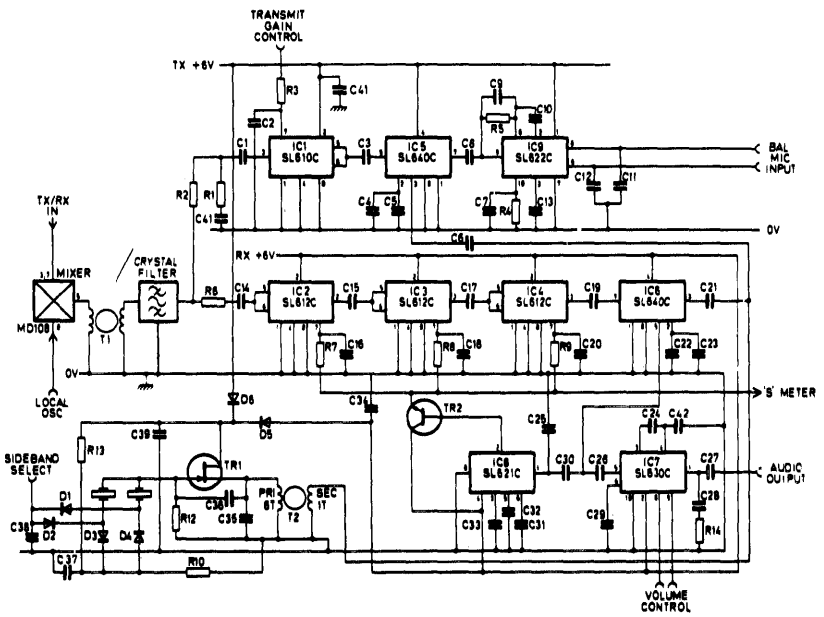


Fig. 63 Simple SSB transceiver circuit diagram

The filter used, an SEI QC1246AX or a KVG XF9-B, has a terminating impedance of 500 ohms, but only within the passband of the filter. At frequencies outside the passband it may be very different, which means that the impedance that the filter presents to the diode ring mixer via the transformer will vary from 50 ohms. Such a mismatch will degrade the cross-modulation and carrier leak performance of the diode ring. However, it was decided on balance, that it was better to tolerate such degradation — which is not excessive — than to complicate the design by incorporating a broadband impedance match (which would probably not be bidirectional and hence would have to be switched between transmit and receive).

The present design allows the same arrangement to operate in opposite directions during receive and transmit without any switching. On the other side of the crystal filter the transmit and receive signal paths diverge but are still not switched.

The Receiver

The incoming RF signal is mixed with the local oscillator in the mixer described above and then passes through an SSB bandwidth 9MHz crystal filter. It is then amplified by three cascaded SL612C IF amplifiers, IC2, 3 and 4. These amplifiers are untuned and since the strip has a maximum gain of 102dB careful attention must be paid both to noise and to stability. The SL612C has a 3dB noise figure which means that the broadband noise at the output of the three-stage strip is about 10mV RMS. This is not sufficient to affect a product detector, which is only concerned with the component within a few kHz of the BFO frequency, but would cause trouble if a diode detector were to be used.

A broadband amplifier with 102dB gain is a likely candidate for stability problems. The three-stage strip used in this receiver is less liable to power supply feedback than most since the SL612C has internal supply decoupling. Nevertheless it must be carefully laid out to minimise earth loops and input/output feedback. The simplest way to do this is to use a double-sided printed circuit board with the components side a continuous ground plane to which all earth connections are made. If this is done the layout on the conductor side of the board is not very critical but if single-sided board is used with the earth conductors on the same side as the other conductors then it does become so. The design of board in Fig. 64 is the most stable layout yet developed for such strips on single-sided board, and it is strongly recommended that it be copied exactly.

There are two other possible causes of instability in this transceiver: inadequate supply switching and inadequate supply decoupling. Since the only on-board transmit/receive switching is by means of power switching it is essential that the transmit supply be not only isolated but earthed during receive, and vice versa. Both supplies should also be well decoupled at RF.

The IF strip has AGC applied to it by an SL621C audio AGC circuit, IC8.AGC is applied via an emitter follower, which has the effect of reducing the AGC range of each SL612C by 0.7V. The overall AGC range could be reduced to less than 90dB were only two SL612Cs to have AGC applied to them. AGC is therefore applied to all three to give 130dB, of which the usable AGC range is about 115dB.

The IF output is applied to an SL640C double-balanced modulator (IC6), used here as a product detector. When AGC is operating, the audio output of

the detector is about 10mV RMS. The audio is fed to IC7, an SL630C audio amplifier which has a voltage gain control. The SL630C can supply up to about 60mW to headphones, to a small loudspeaker or to an external amplifier.

The detected audio also goes to the SL621C audio AGC system (IC8). This has an ideal characteristic for SSB reception. It operates from the receiver audio, not from RF, and it has fast attack and fast decay unless a signal disappears altogether — as in speech pauses — when it does not decay at all for a second and then, if the signal has not reappeared, decays quickly. This enables it to track rising or fading signals but prevents it overloading after each brief speech pause. The circuit also incorporates very fast AGC action to suppress brief noise bursts.

An FET oscillator is used to supply carrier to the product detector and to the double-balanced modulator in the transmitter. The voltage applied to the 'sideband select' terminal determines which crystal is used — upper or lower sideband — but the terminal must not be left unconnected: it must either be connected to +6V or to earth. The oscillator is supplied via diodes from both the transmit and receive lines so that it continues to operate on transmit or receive.

The most basic receiver does not have an 'S' meter but if one is required it may be connected to the emitter of the AGC buffer transistor. It should consist of a moving coil meter connected in series with a resistor such that FSD corresponds to 2.5V and three forward biased silicon diodes. This 'S' Meter circuit has a rather compressed scale for signals more than 40dB above the AGC threshold. If a more linear scale is necessary the more complex system described in the multimode transceiver should be used.

This receiver has a sensitivity of 1.0 microvolts for 10dB S/N. This means that at HF with adequate antennas no RF amplifier is required since atmospheric noise will limit system performance. At higher frequencies, or in systems where small antennas are used, RF gain may be necessary to prevent the performance being gain-limited rather than noise limited. Such amplifiers increase gain but degrade intermodulation performance. In general, without the RF amplifier, the receiver will tolerate about 200mV of adjacent channel signal on the mixer without significant intermodulation. This is, of course, a property of the mixer rather than of the rest of the circuit, although the filter characteristics are also involved.

The Transmitter

The transmitter uses the standard filter method of generating SSB. Audio from the microphone is fed to an SL622C microphone amplifier (IC9), which has AGC giving a constant 100mV output over 60dB of input. The AGC ensures an almost constant output from the transmitter, but can be inconvenient in noisy environments when the transmitter will give full modulation on noise in the absence of a speech input. Such noise modulation is avoided by the addition of a single extra resistor (R5, between pins 8 and 9 of the SL622C) which reduces the dynamic range of the AGC.

The constant-level audio from IC9 is applied to the signal input of an SL640C double-balanced modulator (IC5). The output of the FET carrier oscillator is applied to the carrier input of IC5 and a double sideband suppressed carrier signal appears at its output. Carrier suppression is of the order of 40dB.

This DSB signal is amplified in an SL610C (ICI). The AGC pin of ICI is brought out from the board and may be used either to preset the system gain or as an ALC connection. The amplified DSB from IC1 is then passed through

the crystal filter, which removes one sideband, leaving SSB. The SSB is mixed to the final transmitter frequency in the diode ring mixer and then goes to a linear amplifier which raises it to the transmitter output level. The output from the diode ring is, of course. lower than the input to the filter and is about 100mV or less into 50 ohms.

The output of IC5 and the input of the first SL612C (IC2) are connected to the same point on the filter via resistors. R6 is merely a buffer resistor but R2 and R1 set the impedance which the filter sees in operation. This varies from 480 ohms on transmit to about 530 ohms on receive, but this small variation does not affect filter performance. The loading effects of a turned-off SL612C during transmission and a turned-off SL610C during reception are similarly insignificant.

The transmitter output (at the diode ring) consists of an SSB signal with carrier below — 55dB and opposite sideband below — 60dB, provided that the carrier oscillator is at the correct frequency. The degree of off-channel spurious signals depends on the crystal filter used: 90dB stopband type gives excellent performance but a cheaper one can sometimes cause trouble.

The Transceiver

The transceiver board needs few extra sub-systems to make a complete transceiver. They are: a power supply, microphone, volume control and loudspeaker and also a filter, local oscillator and linear amplifier. These are connected as shown in Fig. 65.

Much of the performance of the final system will depend upon the standard of design of the local oscillator, pre-selector, RF amplifier (if used) and linear amplifier, but the performance of the transceiver board itself is excellent. The Anzac MD-108 mixer used is capable of the required performance between 10kHz and 500MHz. If other diode rings were used the transceiver might be used over an even wider range. Its power consumption is about 400mW on either transmit or receive.

The most attractive feature of this transceiver, despite its high performance, is its simplicity. It uses only 80 components and contains no tuned circuits or other components requiring adjustment. It was designed for two purposes: (a) to demonstrate the usefulness and versatility of the SL600 Series in SSB applications and (b) as a ready-engineered SSB transceiver suitable for those inexperienced in SSB design. It is capable of giving good performance but can be constructed and commissioned by relatively inexperienced personnel.

Physical Construction

The board and component layouts are shown in Fig. 64. The board is single-sided and there are two jumper links on it carrying power supplies. As mentioned above the layout on a single-sided board carrying such a high gain broadband IF strip is critical and it should not be changed. All passive component leads should be as short as possible and integrated circuits should not be mounted more than 6mm above the board.

The two transformers T1 and T2 are both wound on small toroids of high frequency ferrite. The exact size and material are not important but the material must be low loss up to at least 45MHz and it is essential that it has a linear B/H characteristic, otherwise it will cause intermodulation at the receiver

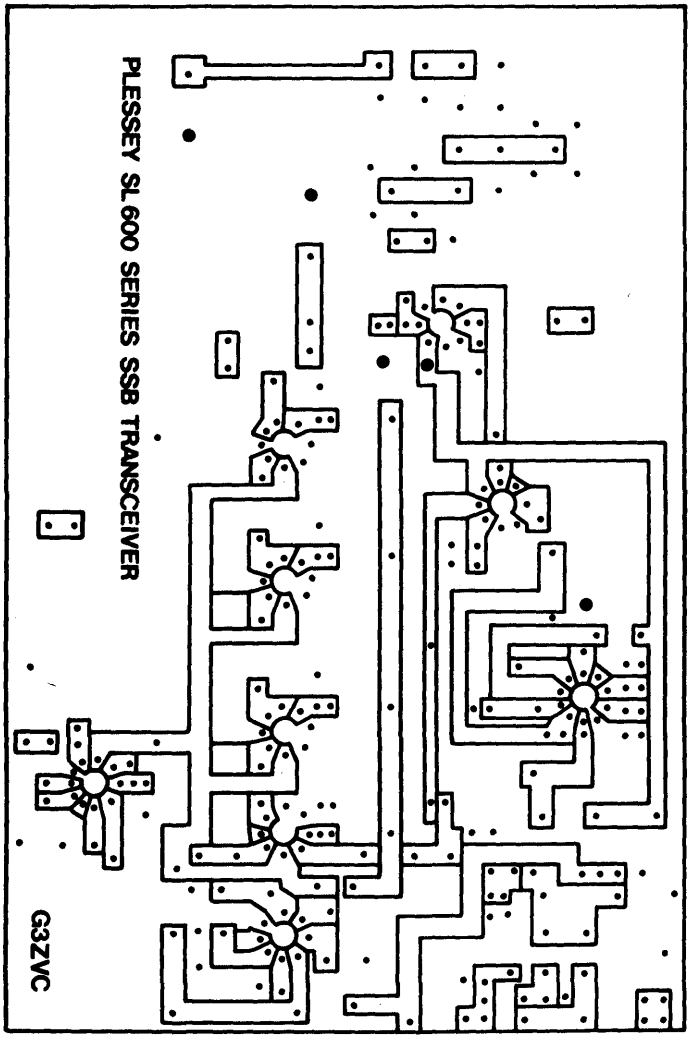


Fig. 64a Copper side of PCB for simple SSB transceiver

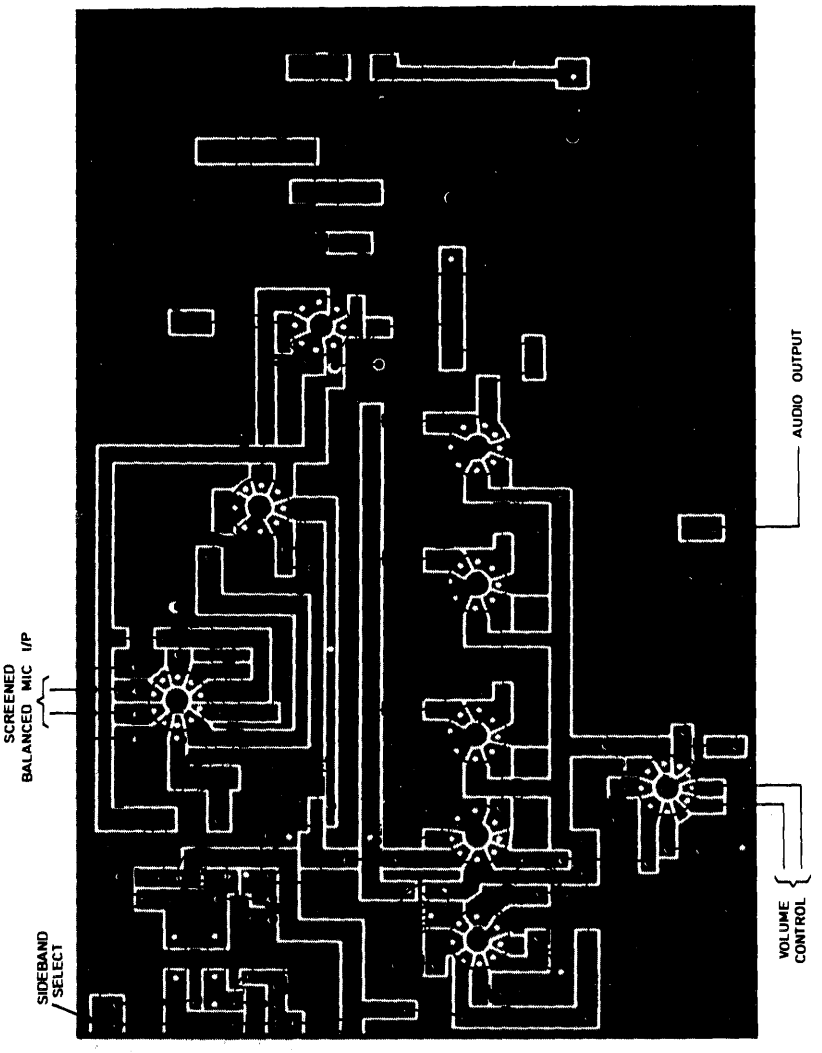


Fig. 64b PCB for simple SSB transceiver

input. T2 is a simple transformer with a six-turn primary and a single turn secondary but T1 is more complex. T1 is made from four 5cm lengths of 26 SWG (0.46mm dia.) enamelled copper wire twisted together. The length of twist is used to wind two turns on the toroid and the ends are separated. Three lengths are then connected in series in the same sense to form the filter winding and the last length is used as the diode ring winding.

There are few other constructional details that need mentioning, but if a receiver without a transmitter is required one may be built by omitting the three transmitting integrated circuits (SL610C, SL622C and the SL640C) between them), R1 to R5 inclusive and C1 to C13 and C40. To preserve the filter impedance match a 500 ohm resistor should be connected from the filter side of R6 to earth.

Component	Value	Rating	Type
R1	100	1/8 W	Hi-Stab.
R2	430	1/8 W	Hi-Stab.
R3	100	1/8 W	Hi-Stab.
R4	680K	1/8 W	Hi-Stab.
R5	1K	1/8 W	Hi-Stab.
R6	50	1/8 W	Hi-Stab.
R7-R9	100	1/8 W	Hi-Stab.
R10	330	1/8 W	Hi-Stab.
R11	10	1/8 W	Hi-Stab.
R12	100K	1/8 W	Hi-Stab.
R13	330	1/8 W	Hi-Stab.
D1-D6			1N4148 } Or similar
TR1			2N3819 } devices
TR2			2N706 }
T1, T2	See text.		
Mixer	Anzac MD-108		
Crystals	9.0015 MHz & 8.9985 MHz		Parallel (30p) resonant
IC1	SL610C		
IC2-IC4	SL612C		
IC5-IC6	SL640C		
IC7	SL630C		
IC8	SL621C		
IC9	SL622C		
C1-C4	1nF	50V	Weecon (Min Ceramic)
C5	10µF	6.3V	Min. Tantalum
C6	100pF	50	Ceramic
C7	47µF	6.3V	Min. Tantalum
C8	10µF	6.3V	Min. Tantalum
C9	4.7nF	50V	Weecon
C10	2µF	6.3V	Min. Tantalum
C11-C12	1nF	50V	Weecon
C13	100nF	50V	Weecon
C14-C15	100pF	50V	Ceramic
C16	4.7nF	50V	Weecon

Table 4 Components list for the Simple SSB Transceiver (Fig. 63)

Component	Value	Rating	Type
C17	100pF	50V	Ceramic
C18	4.7nF	50V	Weecon
C19	100pF	50V	Ceramic
C20	4.7nF	50V	Weecon
C21	100pF	50V	Ceramic
C22	1nF	50V	Weecon
C23	10µF	6.3V	Min. Tantalum
C24	4.7nF	50V	Weecon
C25	100nF	50V	Weecon
C26	10µF	6.3V	Min. Tantalum
C27	100µF	6.3V	Min. Tantalum
C28	10nF	50V	Weecon
C29	1nF	50V	Weecon
C30	1µF	6.3V	Min. Tantalum
C31	100µF	6.3V	Min. Tantalum
C32	47µF	6.3V	Min. Tantalum
C33	100µF	6.3V	Min. Tantalum
C34	400µF	16V	Min. Al. Elect.
C35-C36	68pF	50V	Ceramic
C37-C38	10nF	50V	Weecon
C39-C41	100nF	50V	Weecon
C42	100pF	50V	Ceramic

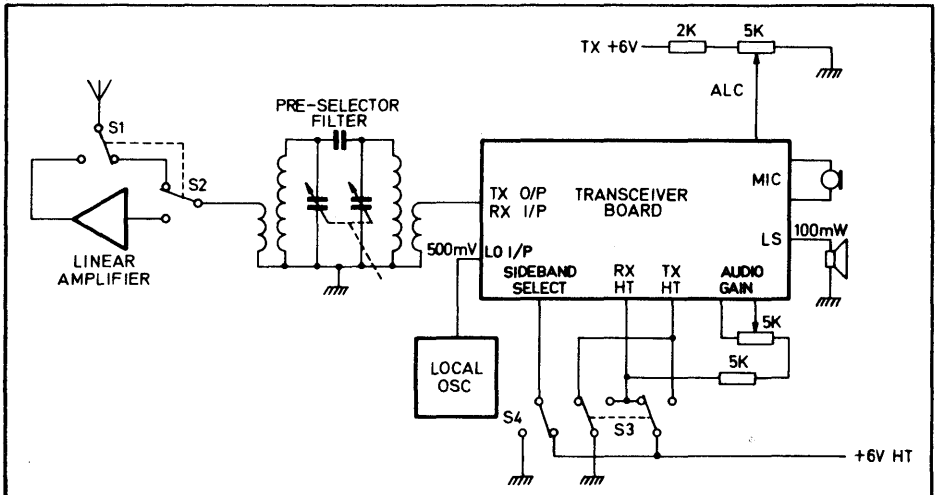
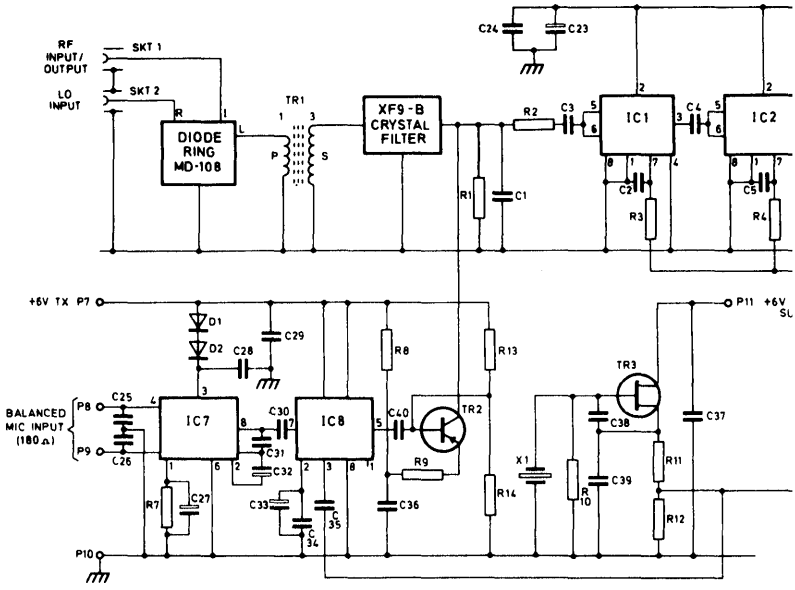


Fig. 65 Block diagram of complete SSB transceiver

SL1600 VERSION OF THE SSB TRANSCEIVER

Figs. 66 and 67 show the circuit diagram and board layout respectively of a version of the SSB transceiver which has been designed to use the SL1600 devices. In addition to the use of the SL1600 series circuits a single PNP transistor is used in place of the SL610 in the transmitter and has only one BFO crystal on the board.



Resistor values are in ohms, capacitor values in microfarads unless otherwise stated.

IC1	SL1612C
IC2	SL1612C
IC3	SL1612C
IC4	SL1640C
IC5	SL1621C
IC6	SL1630C
IC7	SL1622C
IC8	SL1640C
TR1	Si NPN – 2N706, BC108 etc.
TR2	High frequency Si PND – 2N3906 etc.
TR3	High frequency N-channel FET – 2N3819, BF244B etc.
D1 D2	Almost any small Si diode – 1N914 etc.
Diode ring – ANZAC MD-108	

Filter – KVG Xf9-B	
X1	30pF parallel resonant 8998 5kHz in HC18 or HC25
T1	P 2 turns 2 hole S 5 turns ferrite bead
R1	470
R2	47
R3	120
R4	120
R5	120
R6	10
R7	470k
R8	100
R9	100
R10	100k
R11	1k
R12	Select to give 200mV rms at pin 4 of IC4
R13	2.7k
R14	8.2k

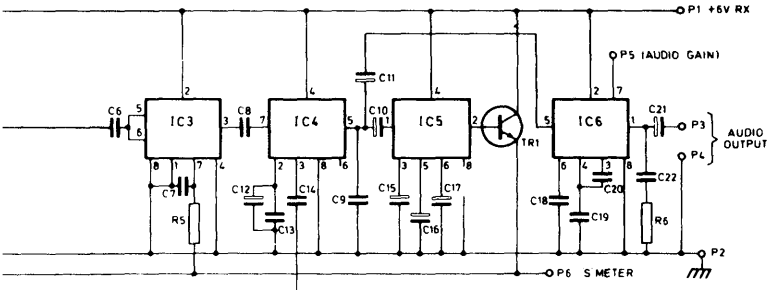


Fig. 66 SL1600 SSB transceiver circuit diagram

16V receive supply
Ground
Audio output
Audio ground
Audio gain control
'S' meter (if used)
+6V transmit supply
Balanced microphone
input (180 ohms)
Ground
+6V common supply

resistors 5 per cent $\frac{1}{4}$W

capacitors miniature ceramic
cept ones marked TANT which are
ad tantalum.

22pF	C31	5000pF
0.01	C32	2 TANT
1000pF	C33	10 TANT
1000pF	C34	0.1
0.01	C35	1000pF
1000pF	C36	0.1

C7	0.01
C8	1000pF
C9	0.1
C10	1 TANT
C11	1 TANT
C12	10 TANT
C13	0.1
C14	1000pF
C15	100 TANT
C16	47 TANT
C17	100 TANT
C18	1000pF
C19	100pF
C20	5000pF
C21	100 TANT
C22	0.01pF
C23	100 TANT
C24	0.1pF
C25	1000pF
C26	1000pF
C27	47 TANT
C28	0.1
C29	0.1pF
C30	1 TANT

C37	0.1
C38	56pF
C39	56pF
C40	0.1

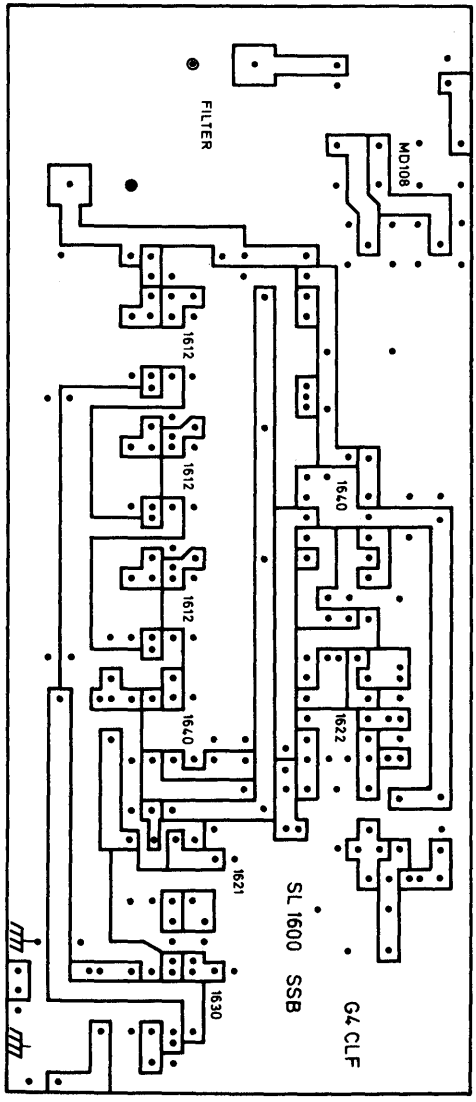


Fig. 67a SL1600 SSB transceiver printed circuit layout. Scale 2:1

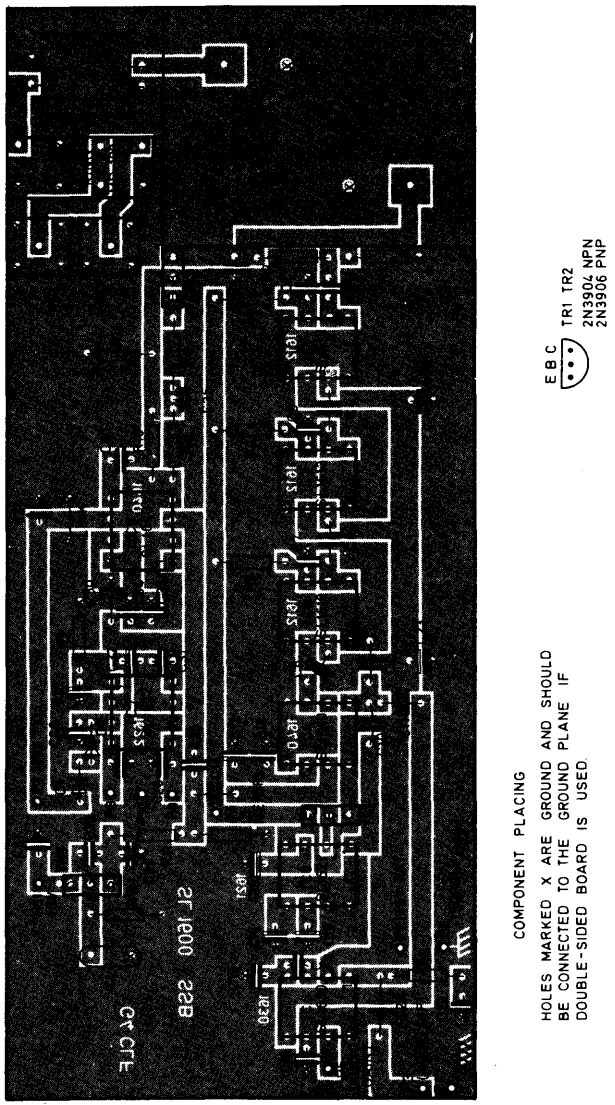


Fig. 67b SL1600 SSB transceiver component locations. Scale1:1. Holes marked X are ground and should be connected to the ground plane if double sided board is used

Like the simple SSB transceiver this multimode transceiver consists of a single printed circuit board and requires the addition of a local oscillator, pre-selector, power amplifier, microphone, loudspeaker and volume control, as well as power supplies and possibly an RF amplifier, to make a complete transceiver.

The board, the block diagram of which is shown in Fig. 68, contains nearly all the signal processing of the transceiver, including a noise blanker, VOX, dual time constant AGC, an 'S' meter/squelch control and RF compression during transmission. Since most sub-systems work independently the board may be built without such refinements and used — either temporarily as a stage in construction and evaluation, or permanently if particular functions are not required. Thus the board may be used to build many different receivers or transceivers.

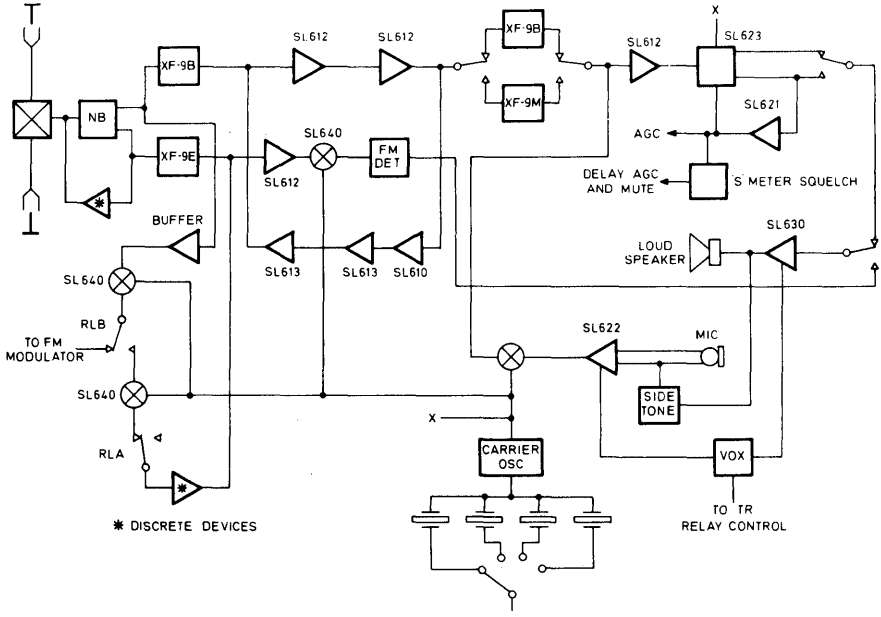


Fig. 68 Multimode transceiver block diagram

RECEIVER DESIGN CONSIDERATIONS

The major problem of receiver design is that of strong signal handling during weak signal reception. There is no single cure for it but designs of high performance receivers usually have as little RF gain as possible, followed by a mixer with good strong signal performance followed at once by a crystal filter. The crystal filter removes the majority of unwanted signals and the rest of the receiver is unlikely to be troubled by them.

The crystal filters do not follow the mixer directly in this receiver, for two reasons: first, to improve the impedance match between the mixer and the filter, and secondly to permit the use of a noise blanker to suppress impulse interference.

A suitable mixer for high performance receivers must have low noise, as little conversion loss as possible, and be able to handle strong unwanted signals without intermodulation. In this transceiver (as a reasonable compromise between cost and performance) a hot carrier diode ring mixer, the MD-108 has again been chosen. Such ring mixers perform best when they are terminated in 50 ohm resistive loads at all ports, but the input impedance of crystal filters, besides being generally higher than 50 ohms, is reactive at frequencies away from the filter passband.

In the Simple SSB Transceiver a transformer matching system was used between the mixer and the filter and the reactive mismatch was ignored. In this system a buffer amplifier, which is in fact also part of the noise blanker, is used to terminate both the mixer and the filter correctly.

A major reason for the failure of receivers to produce weak AM and SSB signals is man-made noise, typically ignition interference, at the antenna. This noise is frequently in the form of very narrow pulses of very high amplitude which can cause the crystal filter to ring at its resonant frequency. Once the filter has been thus stimulated it will stretch the pulse so that it cannot be distinguished from the wanted signal, which it swamps. Only by stopping the ignition pulse before it reaches the filter can this interference be suppressed. The noise blanker must therefore be somewhere in the receiver before the crystal filter and the best place is between the mixer and the filter.

After the crystal filters the receiver design is quite conventional. There are two filters, each feeding its own IF strip. One has a 12kHz passband and feeds the FM IF system, which is a double conversion system with a 455kHz second IF and a quadrature detector. This receiver was designed before the introduction of the SL665, which would allow the use of a single 9MHz IF.

The other filter has a 2.4kHz passband and its output goes to the CW/SBB/AM IF strip. This strip has a broadband gain of about 70dB followed by another crystal filter, which is of 2.4kHz bandwidth for AM and SSB and 500Hz for CW. There is then another IF amplifier stage followed by two detectors. For SSB and CW there is a product detector and for AM there is an envelope detector.

On AM the envelope detector provides carrier AGC to the system but on CW and SSB an audio derived AGC system is used. Squelch and 'S' meter signals are derived from the AGC line.

The decision to use a 2.4kHz filter for AM, removing one sideband, was taken on cost grounds, as was the decision to use only one 500Hz CW filter halfway down the IF strip, whereas two such filters, one at the input to the strip, would certainly improve strong signal rejection in the CW mode. Ideally

there should be four filters at the input (with bandwidths of 12, 6, 2.4 and 0.5kHz respectively for NBFM, AM SSB and CW) and a further three filters halfway down the AM/SBB/CW IF strip to reduce IF noise to a minimum. This would entail an extra three expensive crystal filters compared with the present system — for only a marginal increase in system performance.

The use of two filters halfway down the IF strip is well justified, however. The CW filter in this position removes both unwanted CW signals in the 2.4 kHz passband and also much of the broadband noise which can cause difficulty in copying very weak signals. The 2.4kHz filter is essential to remove the broadband noise between 100kHz and 30MHz generated by the first two IF stages which, if allowed into the AM diode detector, would greatly degrade its performance.

The improvement due to this filter on the SSB product detector is much less, since product detectors produce supersonic outputs from broadband noise and these can be filtered without loss of wanted signal. There is nevertheless a 3dB improvement in S/N ratio in systems where IF noise is the limiting factor on system performance.

TRANSMITTER DESIGN CONSIDERATIONS

The transmitter has to generate all the modes that the receiver has to receive. This is not particularly difficult, but several complexities have been introduced to minimise spurious outputs and broadband noise while making the transmitter as effective as possible.

The modulation envelope of SSB does not resemble the audio producing it and normal audio speech processing techniques do not greatly improve the S/N ratio at the receiver. RF clipping, however, reduces the peak/mean power ratio of the signal and hence improves its mean power and readability.

It is also convenient to use the RF clipper for NBFM and AM, these signals being demodulated from clipped SSB back to audio and the audio signal applied to the NBFM or AM modulators. This technique gives up to 12dB apparent signal to noise ratio improvement and the resulting received audio, while obviously 'processed', is not unpleasant.

The audio input to the transmitter passes through an audio preamplifier with AGC to ensure a roughly constant modulation signal regardless of microphone or audio level. It is converted to DSB in a double-balanced modulator and filtered to SSB which is then applied to a limiting amplifier which removes all amplitude variations. This clipped signal is, of course, rich in both harmonics and intermodulation products and must be filtered in a 2.4kHz bandwidth filter to remove them. The quality of this filter determines the spectral purity of the resulting clipped SSB and is more important than the first filter producing the sideband.

The 2.4kHz bandwidth filter reintroduces amplitude variations into the signal which must be amplified by a linear amplifier. The signal is then either further amplified and mixed to the final transmitter frequency or demodulated to yield processed audio which can be applied to the AM or FM modulators.

The FM system uses this audio to modulate the external VFO while the transceiver board supplies a steady 9MHz output to the transmitter mixer. The AM modulator – which also supplies this unmodulated carrier during FM transmission – consists of a double-balanced modulator with deliberate carrier leak. All transmitted signals pass through a 12kHz filter as they leave the board – this costs nothing since the filter is already present in the FM receiver,

and removes any broadband noise which the buffer amplifiers may have introduced.

The CW transmitter uses the complete SSB system except that a keyed tone is used as the audio input and the 500Hz filter is used instead of the 2.4kHz filter in the SSB generator. This allows only a single frequency to go to the RF clipper, rather than the several frequencies caused by harmonics from the tone generator, which would result from the use of the 2.4kHz filter.

Like the simple SSB transceiver the majority of the transmit/receive switching is performed by switching power supplies and not signal lines. The power switching itself, however, is performed by a relay which can be driven either from a transmit/receive switch or by the VOX system. Mode switching, however, is performed by relays, so that when the transmitter and receiver are in different modes some relays change state between transmission and reception.

TRANSCEIVER SYSTEMS

To use the transceiver board it is built into a system very similar to that used for the Simple SSB Transceiver illustrated in Fig. 65. A small difference is that if FM transmission is required provision must be made for the processed audio from the board to modulate the VFO. Otherwise the two systems are identical – except that rather more power supplies and function switching are required with the multimode transceiver.

Sub-systems may be omitted if a simple transceiver, or just a receiver, is required. Similarly, the board may be built and operated as an SSB receiver, then expanded to an SSB transceiver without RF clipping, then RF clipping added, etc., as required.

CIRCUIT DETAILS

The circuit diagram of the complete transceiver board is shown in Fig. 69. The whole circuit will be described but where sub-systems are built entirely of SL600 devices conventionally used no explanation of circuit configuration will be given. If this is required the reader is referred to Section 1.

The sub-systems into which the board has been divided are described below.

The Mixer

The Anzac MD-108 mixer was chosen for its performance coupled with its low price, but any hot carrier diode ring modulator with 50 ohm ports and adequate strong signal performance (the MD-108 will handle over 200mV RMS adjacent channel signal) combined with low noise and under 7dB conversion loss could be used euqally well. The MD-108 has two ports with 5–500MHz bandwidth and one with DC to 500MHz bandwidth. If the transceiver is used with signals or VFO of under 5MHz it is important to ensure that this signal is applied to the correct port.

It might be thought that the receiver performance on strong signals would be improved by using a better diode ring, able to handle larger signals. This is not in fact so: if the mixer is improved the noise blanker and filter become the limiting factors in the strong signal performance. A mixer with better high or low frequency performance may, however, be substituted if required.

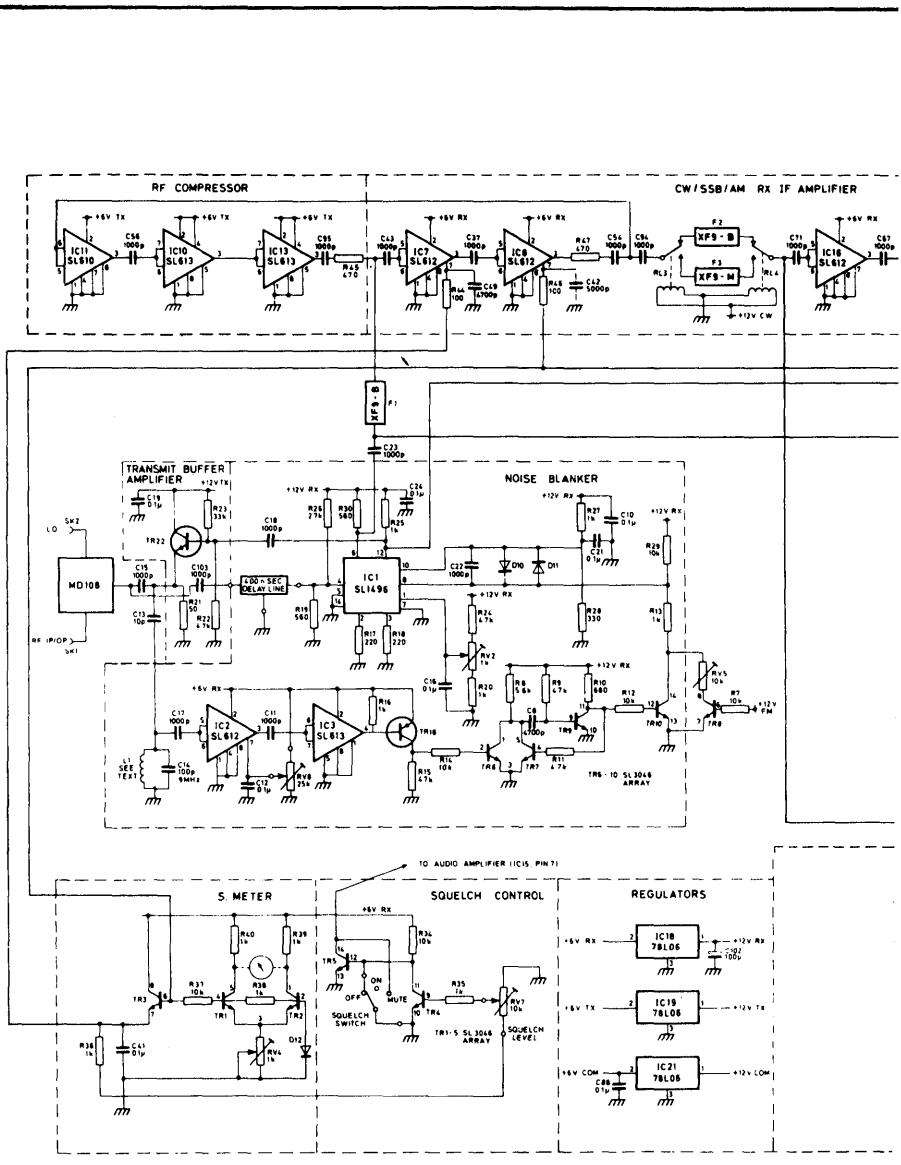
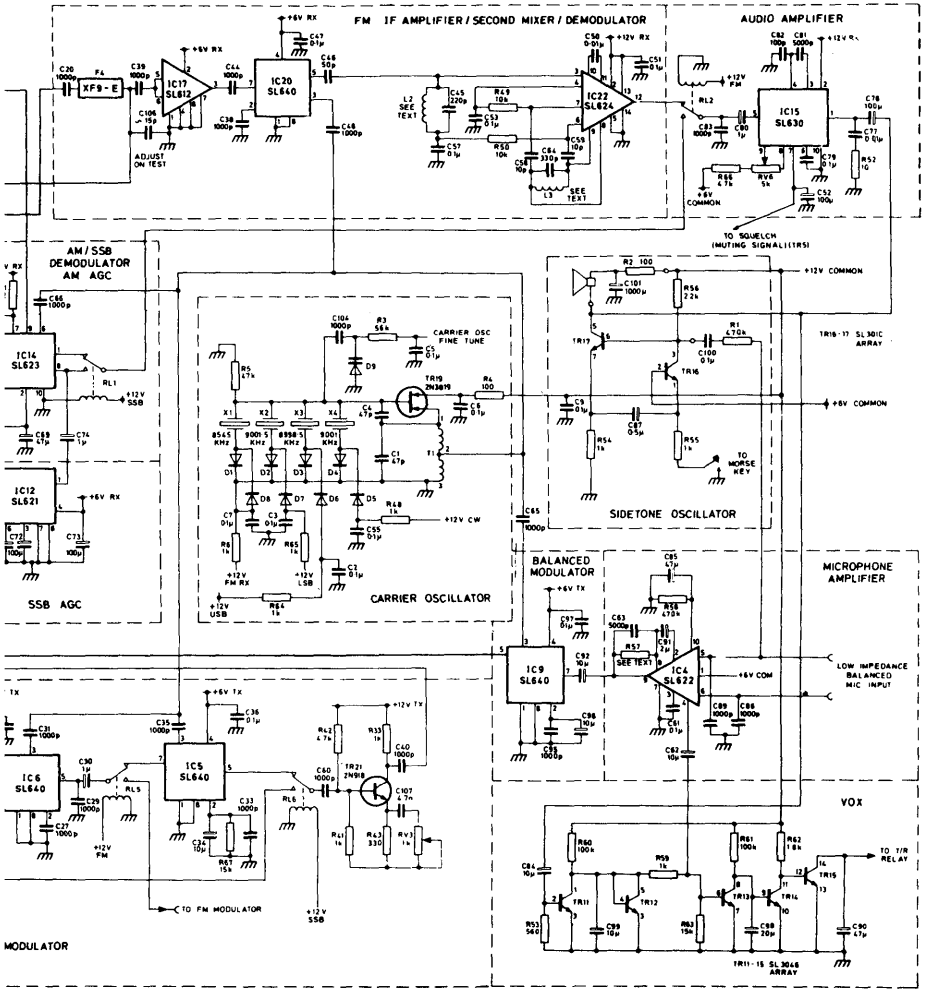


Fig. 69 Multimode transceiver circuit diagram


FM IF AMPLIFIER / SECOND MIXER / DEMODULATOR
AUDIO AMPLIFIER
IC17 SL612
IC20 SL640
IC22 SL624
IC15 SL630
XF9-E
ADJUST ON TEST
AM / SSB DEMODULATOR AM AGC
IC14 SL623
IC12 SL621
SSB AGC
CARRIER OSC FINE TUNE
CARRIER OSCILLATOR
SIDETONE OSCILLATOR
TO MORSE KEY
TO SQUELCH (MUTING SIGNAL) (TR5)
TR16-17 SL301C ARRAY
BALANCED MODULATOR
IC9 SL640
IC4 SL622
MICROPHONE AMPLIFIER
LOW IMPEDANCE BALANCED MIC INPUT
VOX
TO T/R RELAY
TR11-15 SL3046 ARRAY
IC6 SL640
IC5 SL640
TO FM MODULATOR
MODULATOR

The Noise Blanker

Probably as much work went into the development of this noise blanker as into the rest of the receiver. It has excellent performance and causes very little degradation of the receiver strong signal characteristics.

A noise blanker is a receiver which receives noise pulses, amplifies and shapes them, and uses them to turn off the main receiver while noise is present. As noise is not evenly distributed throughout the frequency spectrum the noise blanker receiver should be operated in the same frequency band as the main receiver.

This in turn suggests that the noise receiver and the main receiver be common and that the blanking pulse be applied late in the main receiver. However if a noise pulse is applied to a crystal filter it is stretched from its original length of a few microseconds to as much as several milliseconds. Blanking must therefore be applied before the crystal filters.

The noise blanker must therefore stop a noise pulse before it can reach the crystal filter from the mixer. Furthermore if a blanking pulse has sharp (large dV/dt) edges these will themselves act as noise pulses, negating the effect of blanking the received noise.

There are therefore two conflicting requirements: the noise blanker must act very quickly to prevent the leading edge of a noise spike from reaching the crystal filter, and it must apply a blanking pulse with a slow rise time to the noise gate to prevent the blanking pulse from acting as a noise pulse. The only way these requirements can be met is to delay the signal between the mixer and the filter in a linear delay line and to place the noise gate between the delay line and the crystal filter.

Various forms of blanking gate were tried during the development of the noise blanker – including diode modulators and single and balanced FETs – but none of them gave better performance than an SL1496 double-balanced modulator. The circuit diagram of an SL1496 is shown in Fig. 70 and a diagram of the noise gate in Fig. 71. Transistors designated TR followed by a lower case letter subscript are those internal to the SL1496. Transistor designations using numerals are employed for all other devices.

In this application pins 5 and 14 of the SL1496 (IC1) are connected together and the emitters of TRa and TRb are thus open-circuited. They are then connected externally to the rest of the circuit. When there is no blanking pulse TR10 is turned off and TRc and TRf are turned hard on. With TRc hard on TRa acts as an amplifier to signals on its base and its output goes, via TRc to the XF9-B crystal filter. Since TRd and TRe are off no signal is applied to the XF9-E filter.

When a blanking pulse is applied to TR10 it is turned on and TRc and TRf turn off (slowly because of the resistor in TR10 collector and the 1 nF capacitor between inputs 8 and 10 of the SL1496) and TRd and TRe turn on. The signal path is now to F4 and the F1 is isolated – noise cannot pass to the CW/SSB/AM IF strip.

The noise blanker is not effective during FM reception and is not used. Instead TR8 is turned on and this balances the modulator so that TRc, TRd, TRe and TRf are turned on and signals go to both IF strips. This is necessary because the squelch is derived from the CW/SSB/AM strip in all modes, including FM.

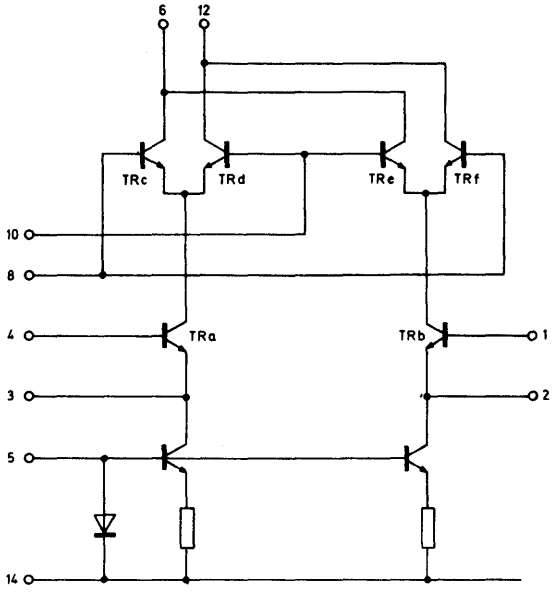


Fig. 70 SL1496C circuit diagram

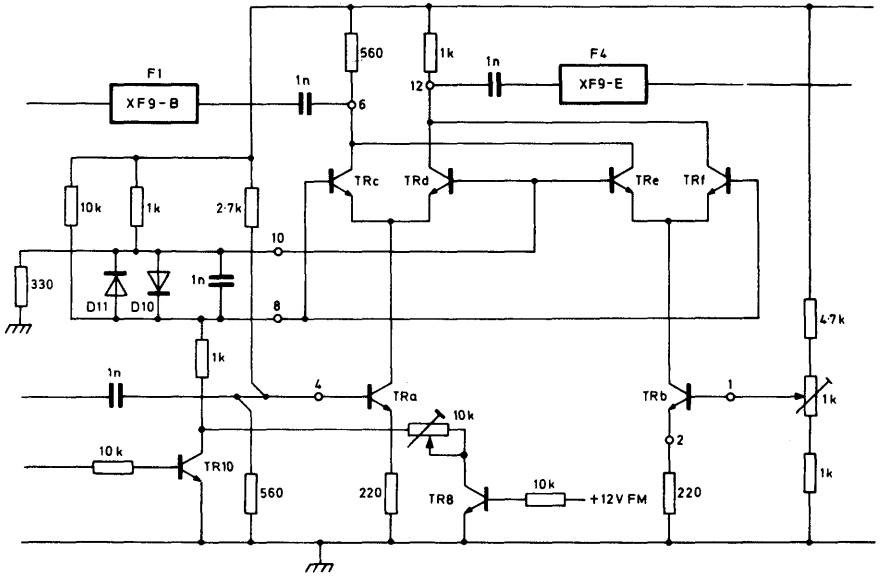


Fig. 71 The noise gate

The diodes between pins 8 and 10 of the SL1496 ensure that the switching drive is at the correct level and the preset current source TR8 keeps the DC current in the filter loads constant as the system switches from the unblanked to the blanked condition.

The whole system is shown in Fig. 72. The noise receiver has its input via a tuned circuit to prevent local oscillator leak from the mixer triggering the system. The noise IF amplifier consists of an SL612C (IC2) and an SL613C (IC3) which acts as a detector. Gain control is applied to IC2 to set the blanking level.

Pulse outputs from the detector in IC3 are buffered by a PNP transistor TR18 to a simple monostable (TR6, TR7 and TR9) with a 10 microsecond pulse. This pulse operates the noise gate. A 400 ns delay line between the mixer and the noise gate ensures that the system is blanked before the pulse that triggers the monostable arrives at the noise gate.

Lastly, a feature of the system is that it acts as a matching amplifier between the 50 ohm mixer and the 500 ohm filters.

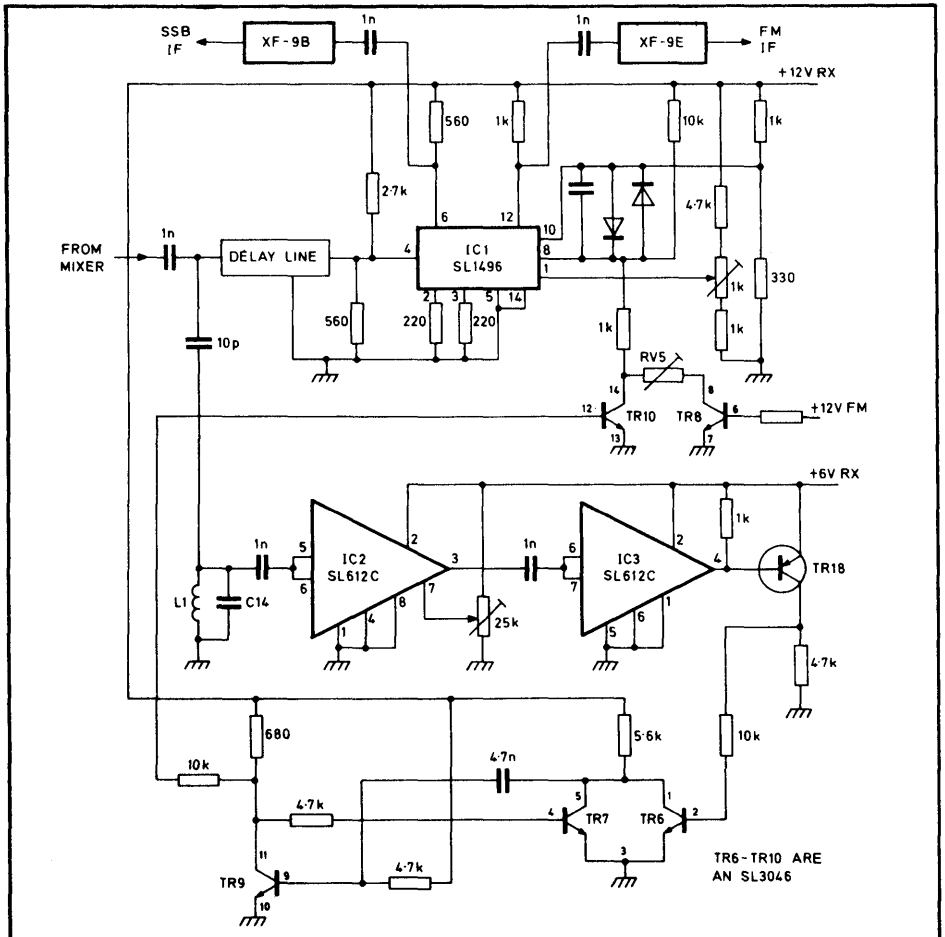


Fig. 72 The noise blanker

The AGC 'S' Meter and Squelch Circuit

As mentioned above the SL623C (IC14) operates as a carrier AGC system during AM reception. It also operates in the same mode during FM reception but does not apply AGC to the FM IF, the AGC line being used only for squelch and to drive the 'S' meter. When the carrier oscillator is turned on, the product detector in IC14 operates and a signal is applied to an SL621C (IC12) connected to its output. The SL621C is more sensitive than the SL623C and so it takes over as AGC source to provide an audio derived AGC system for CW and SSB reception. Since the output impedance of both the SL621C and the SL623C AGC systems are high when they have no input they are both connected to the AGC line and do not load each other.

If fast AGC is required during tuning in the SSB and CW modes, the IC12 may be turned off and control restored to the IC14. This will result in higher outputs but faster decay when tuning from a strong signal. Some professional receivers using SL621C circuits have facilities for dumping AGC from the timing capacitors but it was felt unnecessary to this design.

The AGC line from these two devices drives the second SL612C (IC8) in the CW/SSB/AM IF strip directly and also goes to the squelch and 'S' meter circuitry shown in Fig. 73. TR3 acts as a buffer to drive the squelch circuitry, and also as a diode drop (0.7V) to delay the AGC to IC7. The output of TR3 is filtered by 1 kilohm and 100 nF and applied to a potentiometer ('Squelch Level') and thence to the base of TR4, which acts as an inverter. The inverter output drives TR5 which mutes the SL630C audio amplifier (IC15), by connecting pin 7 of IC15 to earth. A three-position switch which earths either TR4 collector (to disable the Squelch) or TR5 collector (to mute the receiver) is included. Its centre position neither mutes the receiver nor disables the squelch. If a mute position is not required, a single pole on/off switch may be used.

As the AGC characteristic of SL600s is somewhat non-linear, a simple voltmeter on the AGC line does not make a good 'S' meter since it tends to be too sensitive to signal changes near the AGC threshold and not sensitivie enough to large signals. The long-tailed pair TR1 and TR2 with the diode D12 form a compensating circuit. All five transistors in this block of circuitry are on a single chip, the SL3046, in a 14-lead DIL package. This saves board space and gives a good match between TR1 and TR2.

The FM IF Strip and Detector

Double conversion is used in the FM receiver because of the difficulty of providing adequate 'Q' at 9MHz for an NBFM quadrature detector. The 9MHz output from the 12kHz-wide XF9-E filter F4 is amplified by an SL612C (IC17) and is then mixed to 455kHz in an SL640C (IC20). A single tuned circuit is used to remove the image and the signal is then passed to an SL624C working as a limiting amplifier/quadrature detector. This receiver was developed before the SL665 became available – otherwise a single 9MHz filter would have been used and the SL624C replaced by an SL665C.

The CW SSB AM IF Strip

The IF strip is quite conventional. The output of the XF9-B 2.4kHz filter F1 is applied to two cascaded SL612C amplifiers. The output of the second SL612C (IC8) goes either to a 2.4kHz XF9-A or to a 500Hz XF9-M filter, (F3), depending

on whether the receiver is in SSB/AM or in CW mode. The filters are switched by two small relays. After the filter there is another SL612C (IC12) and an SL623C detector (IC14). Without a carrier oscillator IC14 acts as an envelope detector for AM and generates carrier-derived AGC in this mode. When the carrier oscillator is applied IC14 acts as a product detector for SSB and CW and an SL621C (IC12) at the product detector output takes over the AGC. The audio output line must be switched between the two detectors.

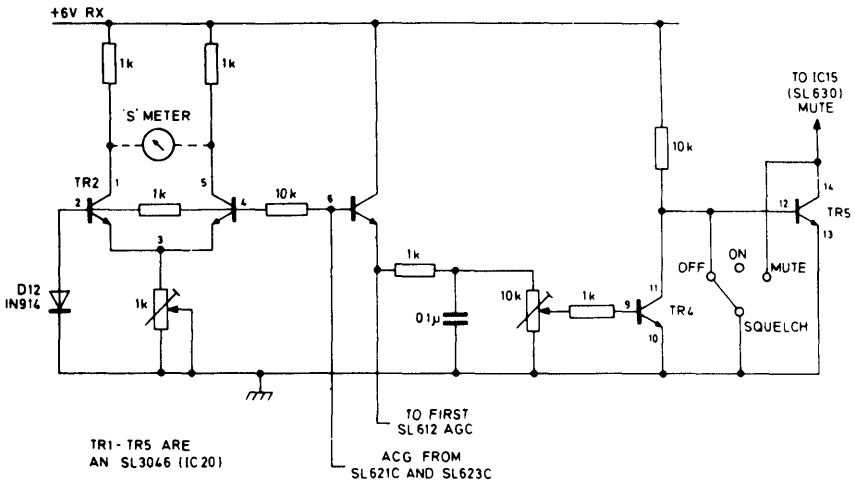


Fig. 73a AGC "S" meter and squelch circuit

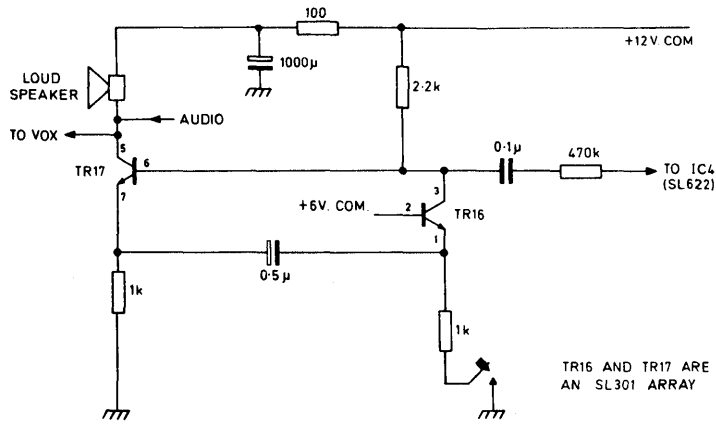


Fig. 73b Sidetone oscillator

The Carrier Oscillator

The carrier oscillator has four different frequencies: 8545kHz for the second mixer in the FM IF system, 8998.5kHz for USB, 9001.5KHz for LSB and 9001 kHz for CW. The circuit is a conventional FET Colpitts oscillator (TR19) and uses diode switching to select one of four crystals.

The output of the oscillator is about 1 volt RMS and is therefore reduced in a potentiometer to the 200mV RMS required by SL640Cs. This potentiometer acts as a virtually constant load to the oscillator and an output buffer is not required.

If the crystals used do not oscillate at their nominal frequency, either the two 47pF capacitors between gate and source and source and ground may be changed in value while remaining equal. Alternatively, where only one or two crystals need trimming, provision is made for crystal trimming by a varicap and a potentiometer for each sideband crystal.

The Audio Amplifier and Sidetone Oscillator

The SL630C audio amplifier (IC15) is driven from a +12V line. It is capable of providing up to 200mW to a small loudspeaker but if a greater output is necessary an additional audio amplifier should be provided. The output of the SL630C is also applied to the VOX circuitry, TR11 to TR15. Gain is controlled by a voltage applied to pin 8 of IC15.

Since the output impedance of the SL630C is quite high when it is turned off, and likewise that of the sidetone oscillator, the loudspeaker is connected directly to both. The sidetone oscillator shown in Fig. 73, is an emitter-coupled multivibrator keyed in the emitter of TR16. A signal is taken from the collector of TR17 and applied to the transmitter audio input.

The sidetone frequency is 1kHz and the system relies on the CW filter to produce a single tone output from the transmitter. If the 500Hz CW filter is omitted the frequency should be raised to about 1750Hz to place the second harmonic well down the SSB filter characteristic. In amateur transceivers an accurate 1750Hz may have an additional use as a repeater access tone.

The Microphone Amplifier and SSB Generator

The audio from the microphone (or the CW from the sidetone oscillator) is amplified by an SL622C (IC4). The SL622C contains its own AGC circuitry with fast attack and slow decay so that its output is around 100mV RMS for over 60dB range of input. There is also a sidetone output which is not affected by the AGC and is used to operate the VOX. R57 sets the microphone AGC threshold and dynamic range. If R57 is open circuit, the threshold is 100 microvolts and the dynamic range is 60dB; if it is 1 kilohm the values are 1mV and 40dB, and if it is 330 ohms they are 3mV and 30dB. C63 should be increased to 0.05 microfarad if R57 is 1 kilohms and to 0.15 microfarad if it is 330 ohms.

The output from the SL622C is applied to the signal input of an SL640C double-balanced modulator (IC9) whose carrier input is 8.9985 MHz or 9.0015 MHz from the carrier oscillator. The output is DSB which is applied to the 2.4kHz bandwidth 9MHz filter (F2) and one sideband removed to produce SSB (USB if 8.9985 MHz is used, LSB if 9.0015).

The RF Compressor

The SSB produced in the system above is normal SSB. Its peak/mean power ratio is fairly large, even though its mean power level is quite constant as a result of the audio AGC. It is therefore amplified in a three-stage amplifier consisting of an SL610C (IC11) followed by two SL613Cs (IC10 and IC13). The SL610C is merely to provide gain but the SL613Cs are high performance limiting amplifiers with symmetrical limiting. The signal emerging from this limiting amplifier preserves its phase information but has had practically all amplitude variation removed from it.

Such a clipped signal is rich in both harmonics and intermodulation products, so it is immediately filtered in another 2.4kHz bandwidth filter (F1) which removes both, but reintroduces some amplitude variation.

The above system is used to process all signals which are to be transmitted, in whatever mode the transmitter is operating. However if a CW signal is being sent, the first 2.4kHz filter (F2) is replaced with a 500Hz filter (F3) to ensure that a single tone is applied to the clipper. After the second filter, however, different modes are processed in different ways.

Single-sideband and CW signals are amplified in a two stage linear amplifier, applied to a 12kHz filter to remove noise and sent to the mixer via the transmit buffer.

When the transmitter is operating in AM or FM mode the clipped SSB is demodulated in an SL640C product detector (IC6) to yield clipped audio, which is then applied to the AM or FM modulators. The SSB clipping produces audio with a slightly artificial sound which, however, is not unpleasant under strong signal conditions, and is particularly easy to copy through noise.

The AM modulator is another SL640C (IC5) with carrier leak deliberately introduced so that the output is AM rather than suppressed carrier DSB. This modulator is used both in the AM and FM modes, but in the FM mode no signal is applied to the signal input and the output is an unmodulated carrier. In either case the output is amplified, filtered in the 12kHz filter (F4), and sent to the transmitter via the transmit buffer and the mixer.

In FM mode the circuit transmits an unmodulated carrier. Frequency modulation is performed off the board by using the processed audio to modulate the transceiver VFO during transmission.

The carrier on AM and FM is not, as one might expect, 9MHz. There is only one carrier oscillator on the board and it is used during transmission to produce clipped SSB. It is therefore working at 9001.5kHz or 8998.5kHz, depending on the position of the sideband selector. The AM or FM carrier is at the same frequency.

The Buffer Amplifiers

The buffer amplifiers used between the various parts of the transmitter are simple transistor or FET circuits. The first designs of the transceiver used integrated circuits to perform these functions but this led to unnecessary complexity and cost with no corresponding increase in performance.

The VOX (Voice Operated Transmit Relay)

A VOX circuit is one which switches a transceiver from receive to transmit when it detects speech at the microphone. The obvious problem with such circuits is to prevent them from reacting to signals from the loud speaker.

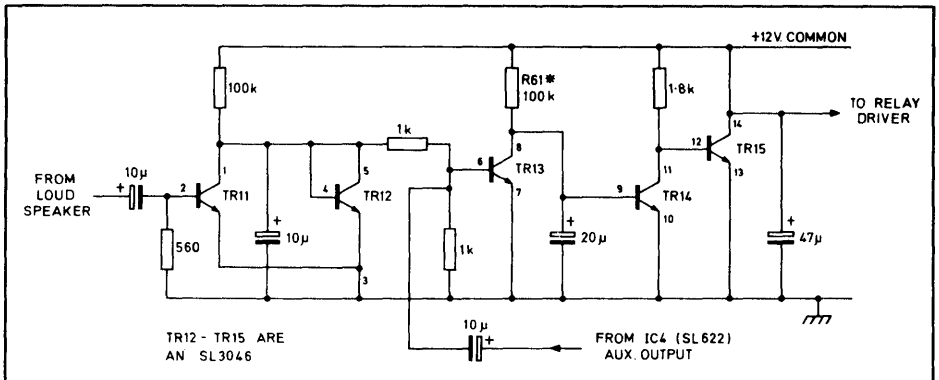


Fig. 74 VOX circuit

The simplest way to do this is to feed the loudspeaker signals to the VOX circuit so that only microphone signals which are not also present in the loudspeaker circuit affect its operation. This is quite difficult and is often liable to cause spurious switching unless the system is carefully adjusted by the operator to compensate for the microphone and the acoustics of the surroundings.

The system used in this transceiver is slightly different. The signal from the microphone is gated by the internal signal to the loudspeaker so that no input to the microphone will affect the VOX while there is a signal to the loudspeaker. The only drawback to this system is that the VOX cannot operate during the reception of non-syllabic noise. Such conditions are, however, unusual.

The circuit is shown in Fig. 74 and uses another SL3046 five transistor monolithic array. Positive half-cycles from the microphone amplifier SL622C (which is powered during reception) turn on TR13 unless prevented by the presence of a loudspeaker signal on TR11. The time constant of the gate circuit is such that VOX action can occur in the spaces between words in normal speech.

TR13 turns on TR15 via TR14. An integrator consisting of R61 and C98 controls the time which elapses between the cessation of speech and the reversion to reception. For breakthrough CW operation (when the operator listens between the dots and dashes of his own transmission) the time constant may be reduced. If the relay is a low power one it may be connected between TR15 collector and +12V, otherwise a PNP driver should be used with an input resistor in its base circuitry.

Power Supplies and Switching

The transceiver board uses three +12V supplies. One is present during reception, one during transmission, and one is common. There are three +6V integrated circuit regulators on the board, one for each +12V line, to supply the appropriate SL600s. This type of regulation greatly reduces cross-talk via the supplies.

Mode switching is accomplished by applying +12V to the relevant one of the three mode lines: CW, FM, or SSB. The two unwanted lines are earthed.

Construction

The transceiver board is constructed of double-sided printed circuit material and earth connections are made on both sides of the board – plated through holes would remove this necessity but were not used in the prototype for reasons of cost and ease of modification. As the board is very small for the complexity of circuitry it carries some of the relay connections were wired. The board diagram is Fig. 75a and the component location is given in Fig. 75b.

It would be almost impossible to make such a system stable on single-sided board but systems derived from this one and built on double-sided board should not present any particular layout problems.

Table 5 Components for the multimode transceiver (Fig. 69)

INTEGRATED CIRCUITS

IC1	SL1496
IC2	SL612C
IC3	SL613C
IC4	SL622C
IC5	SL640C
IC6	SL640C
IC7	SL612C
IC8	SL612C
IC9	SL640C
IC10	SL613C
IC11	SL610C
IC12	SL621C
IC13	SL613C
IC14	SL623C
IC15	SL630C
IC16	SL612C
IC17	SL612C
IC18	78L06
IC19	78L06
IC20	SL640C
IC21	78L06
IC22	SL624

RESISTORS (ohms)

R1	470(NOB)
R2	100(NOB)
R3	56K
R4	100
R5	47K
R6	1K
R7	10K
R8	5.6K
R9	4.7K
R10	680
R11	4.7K
R12	10K
R13	1K
R14	10K
R15	4.7K
R16	1K
R17	220
R18	220
R19	560
R20	1K
R21	50
R22	4.7K
R23	33K
R24	4.7K
R25	1K
R26	2.7K
R27	1K
R28	330
R29	10K
R30	560
R31	10K
R32	560
R33	1K
R34	10K
R35	1K
R36	1K
R37	10K
R38	1K
R39	1K
R40	1K
R41	1K
R42	4.7K
R43	330
R44	100
R45	470
R46	100
R47	470
R48	1K
R49	10K
R50	10K
R51	82
R52	10
R53	560
R54	1K
R55	1K
R56	2.2K
R57	See text
R58	470K
R59	1K
R60	100K
R61	100K
R62	1.8K
R63	15K
R64*	1K
R65*	1K
R66	4.7K(NOB)
R67†	15K

* Vertical on board
† May need selection

VARIABLE RESISTORS

RV1	10K
RV2	1K
RV3	1K
RV4	1K
RV5	10K
RV6	5K Lin.(NOB)
RV7	10K Lin.(NOB)
RV8	25K Lin.(NOB)

CAPACITORS

C1	47p
C2	0.1µF
C3	0.1µF
C4	47pF
C5	0.1µF
C6	0.1µF
C7	0.1µF
C8	4700pF
C9	0.1µF
C10	0.1µF
C11	1000pF
C12	0.1µF
C13	10pF
C14	100pF
C15	1000pF
C16	0.1µF
C17	1000pF
C18	1000pF
C19	0.1µF
C20	1000pF
C21	0.1µF
C22	1000pF
C23	1000pF
C24	0.1µF
C25	1000pF
C26	0.1µF
C27	1000pF
C28	1000pF
C29	1000pF
C30	1µF(T)
C31	1000pF
C32	0.1µF
C33	1000pF
C34	10µF(T)
C35	1000pF
C36	0.1µF
C37	1000pF
C38	1000pF
C39	1000pF
C40	1000pF
C41	0.1µF
C42	4700pF
C43	1000pF
C44	1000pF
C45	220pF
C46	50pF
C47	0.1µF
C48	1000pF
C49	4700pF
C50	0.01µF
C51	0.1µF
C52	100µF(T)
C53	0.1µF
C54	1000pF
C55	0.1µF
C56	1000pF
C57	0.1µF
C58	10pF
C59	10pF
C60	1000pF
C61	0.1µF
C62	10µF(T)
C63	4700pF
C64	330pF
C65	1000pF
C66	1000pF
C67	1000pF
C68	1µF(T)
C69	47µF(T)
C70	0.1µF
C71	1000pF
C72	100µF(T)
C73	100µF(T)
C74	1µF(T)
C75	100µF(T)
C76	47µF(T)
C77	0.01µF(T)
C78	100µF(T)
C79	0.1µF
C80	1µF(T)
C81	4700pF
C82	100pF
C83	1000pF
C84	10µF(T)
C85	47µF(T)
C86	1000pF
C87	0.5µF(T)

Table 5 (continued)

C88	0.1µF
C89	1000pF
C90	100µF(T)
C91	2.2µF(T)
C92	10µF(T)
C93	1000pF
C94	1000pF
C95	1000pF
C96	10µF(T)
C97	0.1µF
C98	20µF(T)
C99	10µF(T)
C100	0·1µF(NOB)
C101	1000µF(NOB)
C102	100µF(T)
C103	1000pF
C104	1000pF
C105	10µF(T)
C106	15pF(SOT)
C107	4.7nF

NOB = Not on board
All ¼W film types
Tolerance 5%

SOT = Select on test

All capacitors except C101 (which is aluminium electrolytic) are either bead tantalum (marked T) or miniature ceramic; tolerance 20%

TI	6:1 Toroidal RF transformer	
L1	3.1µH Nominal, slug tuned screened RF coil.	
L2	550µH Nominal, slug tuned screened RF coil.	
L3	370µH Nominal, slug tuned screened RF coil.	
F1	XF9-B	
F2	XF9-B	KVG crystal filters
F3	XF9-M	
F4	XF9-E	
X1	8545KH	
X2	9001.5KHz	Parallel (30p) resonant
X3	8998.5KHz	HC18 or HC25 crystals
X4	9001Khz	

RL1–6 National R5-12V miniature relays

Diode ring – Anzac MD108

TRANSISTORS

TR1–5	SL3046C
TR6–10	SL3046C
TR11–15	SL3046C
TR16–17	SL301C Dual transistor
TR18	2N3906 or similar PNP
TR19	2N3819 or similar N-FET
TR20	2N3819 or similar N-FET
TR21	2N918 or similar fast NPN
TR22	2N706 or similar NPN
D1–8	1N914 or similar low capacity Si switching diode
D9	MV1 1
D10–11	MBD101
D12	1N914

Delay line
Belfuse 0420-0400-05, or any delay line with 500 ohm ports, 300 to 800ns delay and less than 8dB insertion loss at 9MHz.

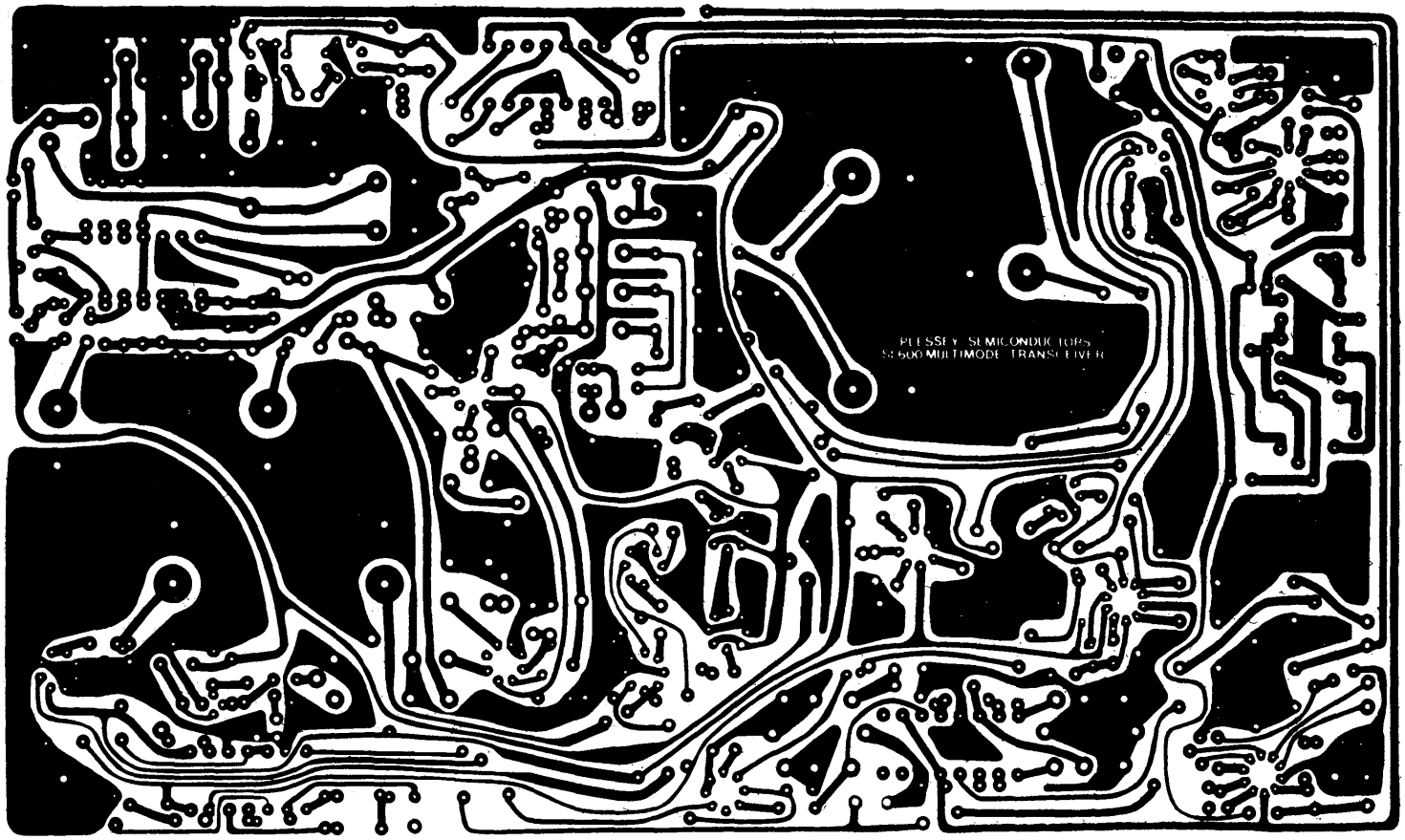
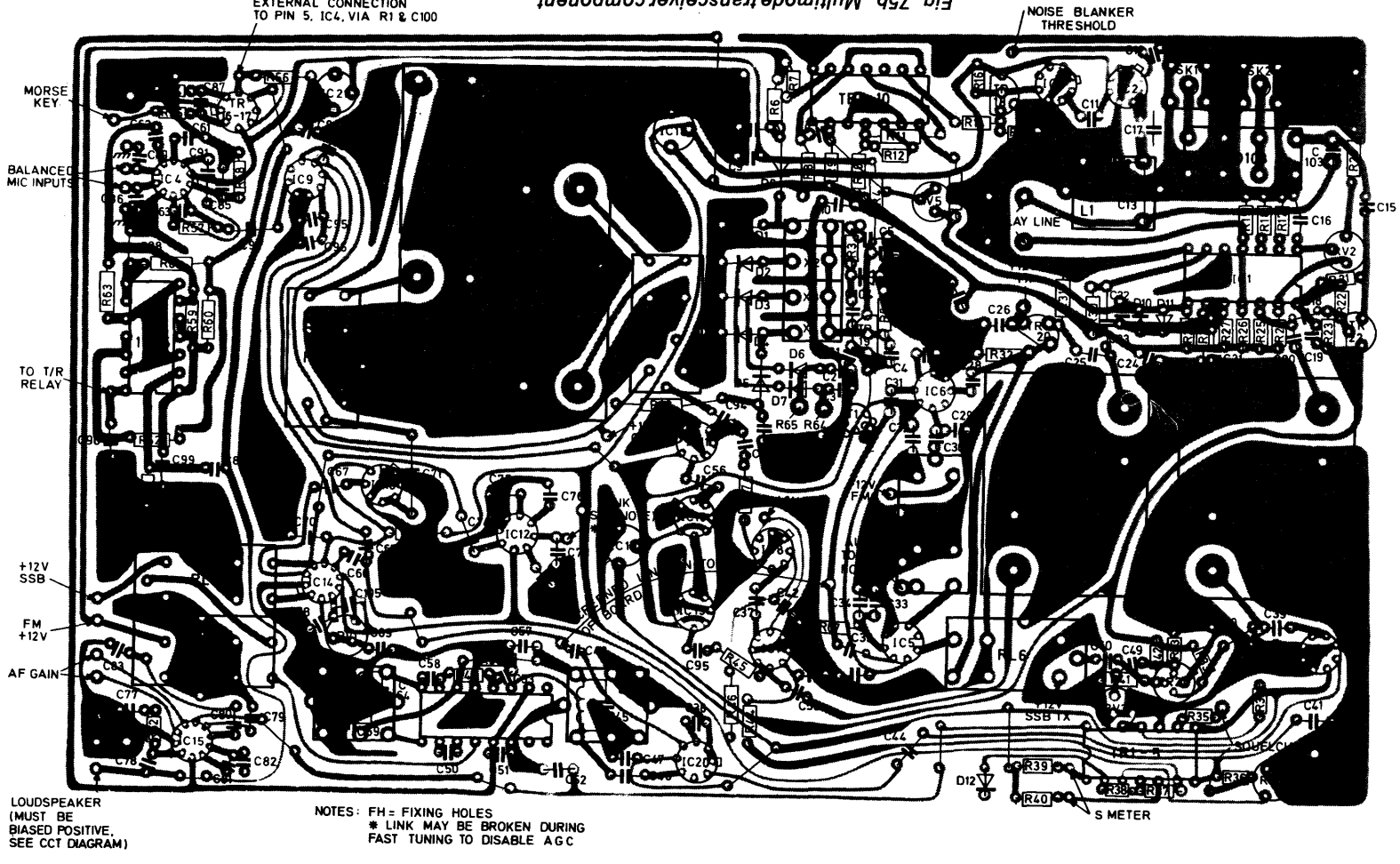


Fig. 75a Multimode transceiver PCB

Fig. 75b Multimode transceiver component layout



27MHz AM/SSB transceiver

Fig. 76 shows the circuit diagram of a dual converion AM/SSB transceiver intended for use on 27MHz Citizens' Band. It has evolved from the versatile multimode transceiver described above but where the multimode transceiver is optimised for performance, this transceiver, being primarily intended for the CB market, is optimised for economy.

Like the multimode transceiver, this system is equipped with a noise blanker but instead of a delay line uses a low-cost ceramic 10.7MHz IF filter (which also acts as the first IF filter) as the delay element. The filter has a delay of about 1.5 microseconds.

The receiver is conventional. A 27MHz tuned circuit is followed by an SL1610C RF amplifier and an SL1641C mixer to the first IF of 10.695MHz. After a 10.695MHz filter (which also acts as a noise blanker delay) the signal passes through an SL1496C noise gate and on to the SL1641C second mixer. The noise blanker receiver is driven at 27MHz by the SL1610C RF amplifier and consists of an SL1613C amplifier and detector followed by a CMOS 4011 acting as a monostable to generate the blanking pulse to the SL1496C.

The output from the second mixer, at 455kHz, is switched by diode switches to one or other of two ceramic ladder filters – one with 2.4kHz bandwidth for SSB and the other with 6kHz bandwidth for AM. The IF strip following the filter consists of an SL1611C and two SL1612Cs and contains a simple ceramic filter to minimise broadband noise. An SL1623C AM/SSB detector is used which generates AGC during AM reception and an SL1621C generates AGC during SSB reception.

Squelch is obtained from the AGC line by an SL748C op. amp. acting as a threshold switch. Its output switches the audio path by turning on and off the bias to a transistor amplifier. The audio output stage uses a TBA800 3 watt integrated circuit audio amplifier.

The transmitter uses an SL1626C as a microphone AGC amplifier and an SL1641C as either an AM modulator or as a DSB generator, depending on switching. The 455kHz AM or DSB is passed through the appropriate filter and mixed to 10.695MHz, where it is refiltered and mixed again to its final 27MHz frequency. Both mixers are SL1600 devices – the SL1640C and the SL1641C respectively.

The transceiver, like the others described above, requires the addition of oscillators, an RF power amplifier and power supplies. It is intended for use with the Plessey SP8921/8922 CB synthesiser but also requires an oscillator which may be switched between 453.5kHz, 455kHz and 456.kHz for use as the receiver BFO and the carrier oscillator in the transmitter.

Power supplies of +6V and +12V are required, which are switched in various ways during transmission and reception. All supplies must be well decoupled at HF and LF.

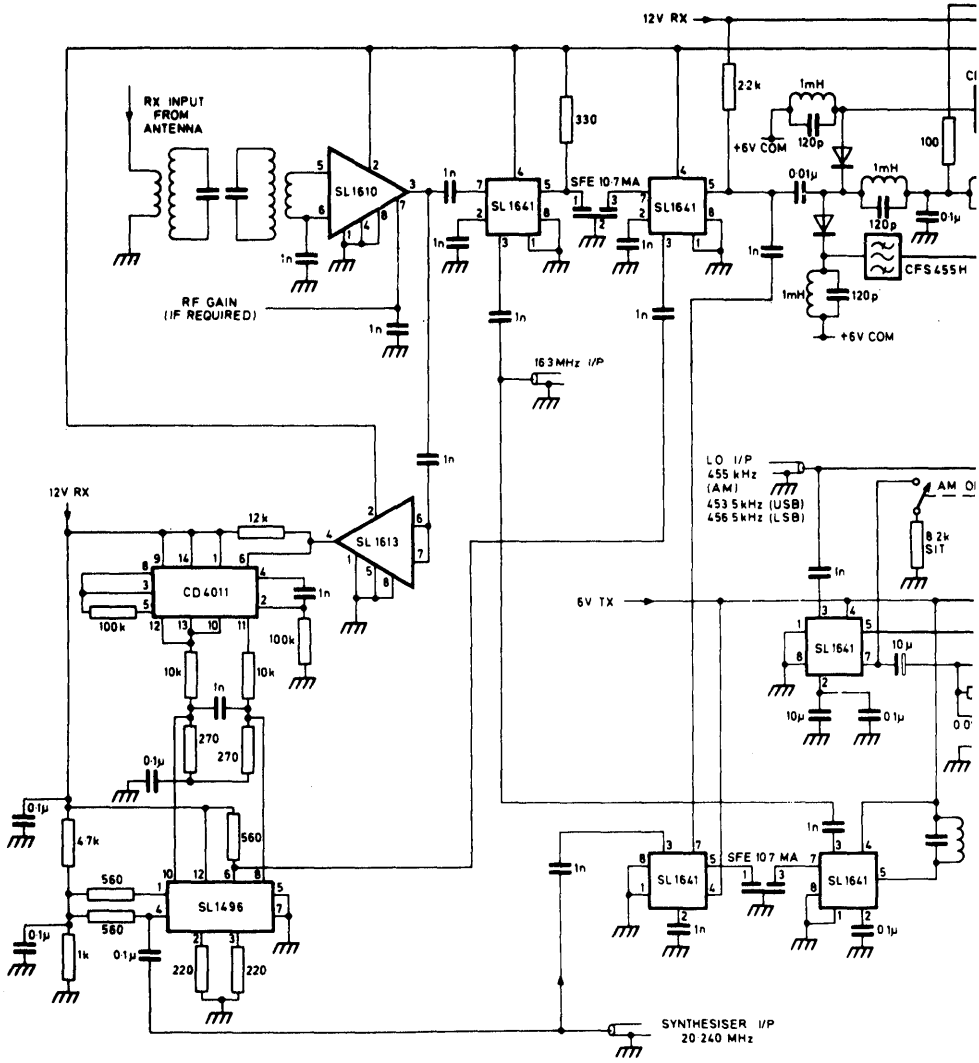
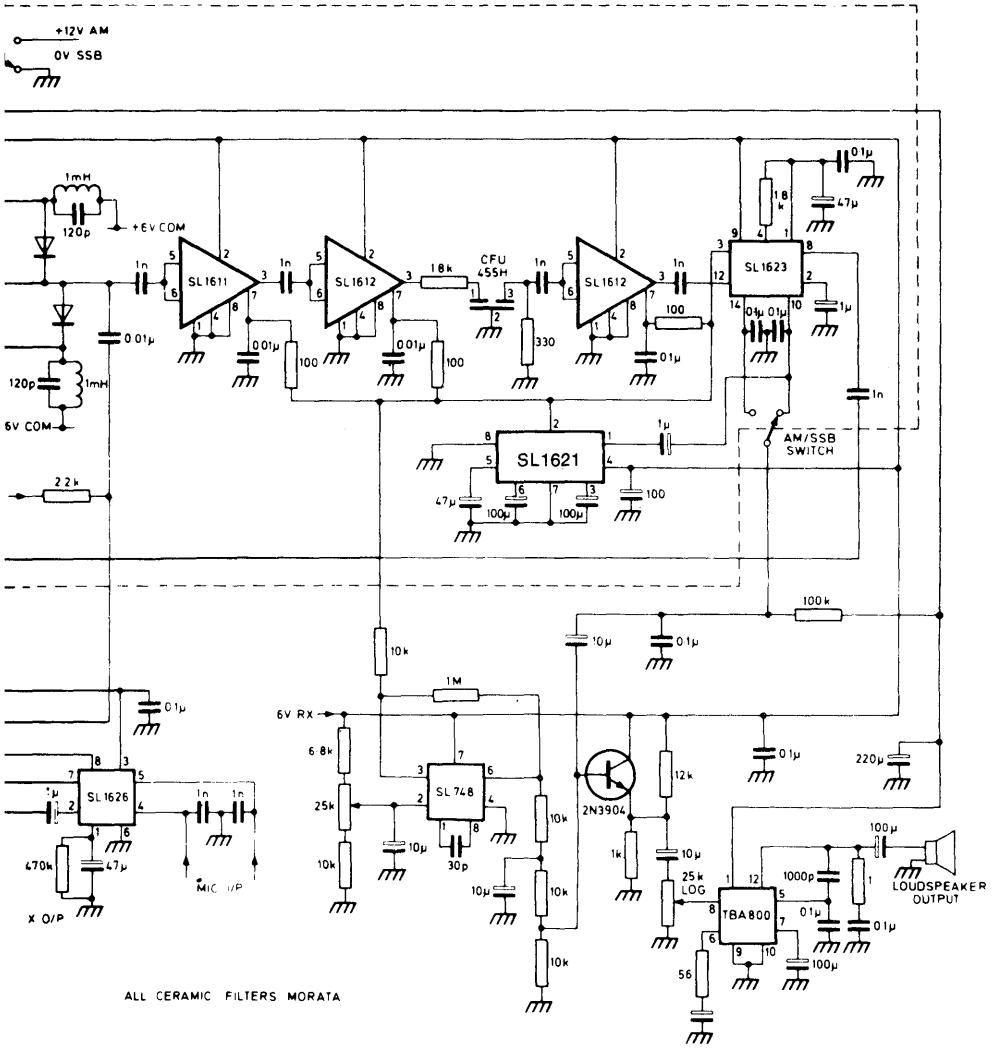


Fig. 76 Dual conversion AM/SSB Citizens' Band transceiver


+12V AM
0V SSB
1mH
120p
+6V COM
SL1611
SL1612
SL1612
SL1623
SL1621
SL1626
SL748
TBA800
2N3904
CFU
455H
18k
330
100
100k
10k
1M
6V RX
6V COM
22k
6.8k
25k
10k
470k
X O/P
MIC I/P
30p
1k
25k
LOG
56
220µ
1000p
AM/SSB
SWITCH
LOUDSPEAKER
OUTPUT
ALL CERAMIC FILTERS MORATA

Introduction to SL6000 Series

The Plessey Semiconductors SL6000 series of radio linear circuits extends the concept of the 'building block' approach to wider systems. Each device features advanced circuit techniques which result in higher levels of integration, lower power consumption or exceptional performance. All products are available in plastic and metal can or ceramic packages.

SL6000 PRODUCT RANGE	
IF AMPLIFIERS/DETECTORS	
SL6600	FM Double Conversion with PLL Detector
SL6640	FM Single Conversion, audio stage (10.7MHz)
SL6650	FM Single Conversion (10.7MHz)
SL6690	FM Single Conversion, low power for pagers (455kHz)
SL6700	AM Double Conversion
AUDIO	
SL6270	Microphone Amplifier with AGC to give 'constant' output
SL6290	SL6270 plus speech clipper, buffer and relay driver
SL6310	Switchable audio amplifier (400mW/9V/8ohms)

SL6600C

LOW POWER IF/AF PLL CIRCUIT FOR NARROW BAND FM

The SL6600 is a single or double conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits the SL6600 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with a second IF frequency of less than 1MHz. Normally the SL6600 will be fed with a first IF signal of 10.7 or 21.4MHz; there is a crystal oscillator and mixer for conversion to the second IF amplifier, a PLL detector and squelch system.

IF Amplifiers and Mixer

The SL6600 can be operated either as a single conversion circuit with a maximum recommended input frequency of 800kHz or in a double conversion mode with a first IF of the input frequency (50MHz max.) and a second IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IFs; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 25 MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used.

When a single conversion circuit is required a 6.8k resistor should be connected in place of the crystal and a further 2.7k resistor connected between pin 1 and earth. The overall gain of the circuit will be reduced by 12dB with this technique.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz.

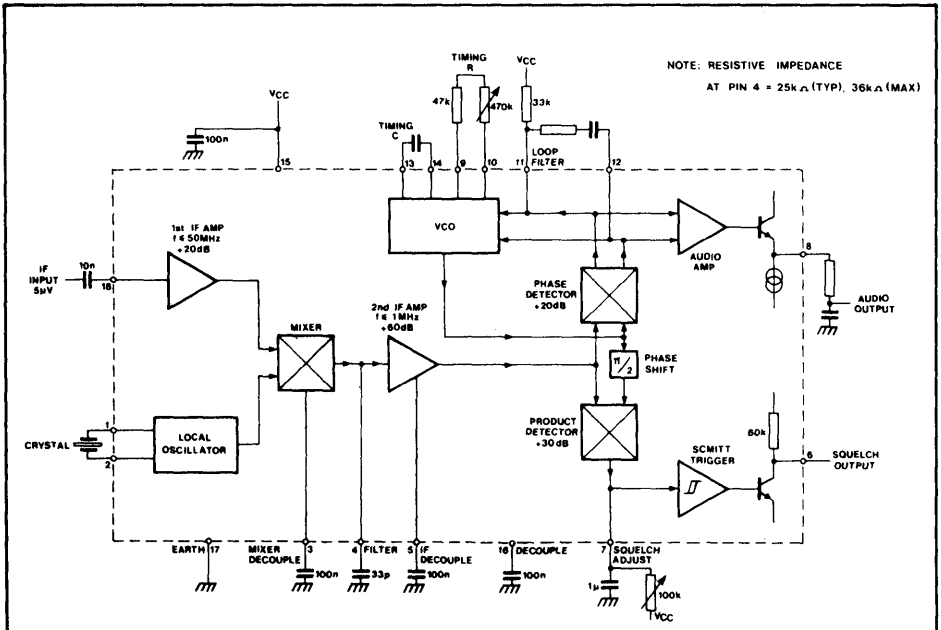


Fig. 22 SL6600 Block diagram

Phase Locked Loop.

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor according to the formula (30/f)pF where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine +10% frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 47k (recommended minimum value) increases the frequency by approx. 10%.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R2 and capacitor C1 must be calculated so that the natural loop frequency fn and damping factor ξ are suitable for the FM deviation and modulation bandwidth required. Values of 6.2k and 2.2nF are recommended for ±5kHz maximum deviation and 3kHz audio bandwidth when the second IF frequency is 100kHz. These give fn = 20kHz ξ = 0.707.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. This feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and Vcc to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7k and 4.7nF may be used.

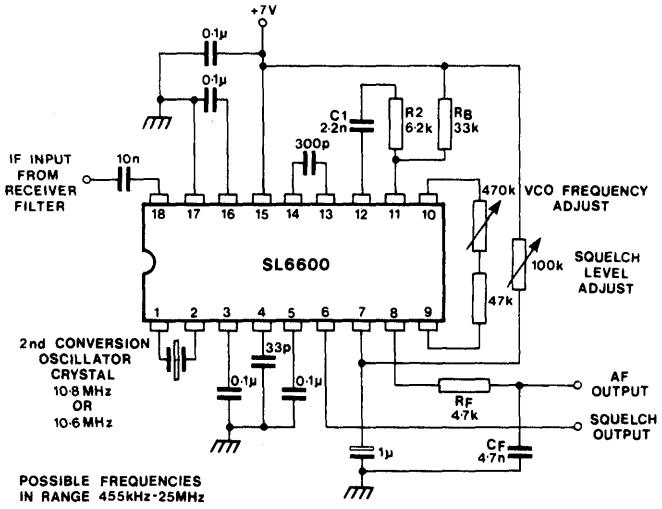
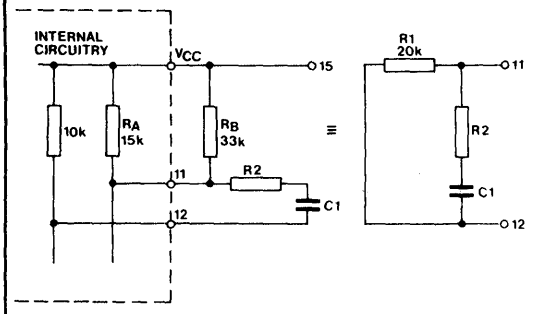


Fig. 23 SL6600 application diagram (1st IF=10.7MHz, 2nd IF=100 kHz)

LOOP FILTER DESIGN

The design of the loop filter determines the allowable deviation of the received FM, the bandwidth of the modulating audio and the signal-to-noise ratio which may be achieved. With wide-deviation signals the filter may be omitted altogether and the system will work perfectly well, but with a somewhat reduced signal-to-noise ratio which is nevertheless quite acceptable in many applications. The filter (Fig.24) consists of a resistor and capacitor (R2 and C1) in series between pins 11 and 12. The external 30 kΩ resistor mentioned above produces a composite resistor, R1, of 20 kΩ formed by the series connection of the two resistors on the chip and the external resistor in parallel with one of them.



$$2\pi f_n = \left(\frac{K_o K_D}{\tau_1 + \tau_2}\right)^{\frac{1}{2}}$$

$$= \tfrac{1}{2}\left(\frac{K_o K_D}{\tau_1 + \tau_2}\right)^{\frac{1}{2}}\left(\tau_2 + \frac{1}{K_o K_D}\right)$$

Fig. 24 SL6600 loop filter circuit

The loop constants of the SL6600 are:–

K_O = 2.4f_O Radians/Volt second
K_D = 2.8 Volts/Radian
R1 = 20k Ω
$K_O K_D$ = 6.7f_O sec^{-1}

Other variables used in driving the loop filter are:–

f_O The VCO centre frequency
Δf The peak deviation
f_n The natural frequency of the loop
f_m The maximum modulation frequency
ϕe The maximum phase error in the loop
ξ The damping Factor

The values of f_m and Δf are part of the system specification and together with f_O specify ϕe. The VCO centre frequency is generally chosen to be 100kHz or 10Δf, whichever is the greater. Maximum frequency is 1MHz. The damping factor, ξ, is usually chosen to be 0.707. Fig.25 shows the relationship between ϕe, f_m and Δf for ξ = 0.707.

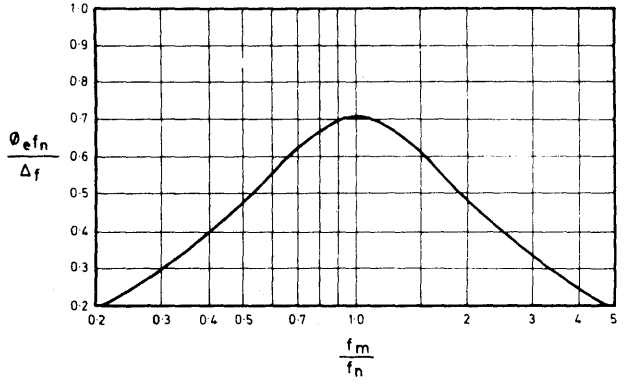


Fig. 25 Phase error for damping factor = 0.707

XAMPLE $\Delta f = 5kHz; f_m = 3kHz, f_o = 100kHz$

$$\text{Therefore } \phi_e \max = \frac{0.93\Delta f}{f_o} = \frac{0.93 \times 5 \times 10^3}{100 \times 10^3} = 0.046 \text{ radians}$$

The problem now is to deduce the value of f_n from Fig. 4; this is an iterative process.

) Put $f_n = 10kHz$. Therefore $\frac{f_m}{f_n} = \frac{3}{10} = 0.3$

from Fig. 4 $\phi_e = \frac{0.3 \times 5 \times 10^3}{10 \times 10^3} = 0.15$ radians (too large)

) Put $f_n = 20kHz$. Therefore $\frac{f_m}{f_n} = \frac{3}{20} = 0.15$

from Fig 25 $\phi_e = \frac{0.17 \times 5 \times 10^3}{20 \times 10^3} = 0.043$ radians,

hich agrees closely with the required value. Knowing the natural frequency the loop ne constants can now be evaluated :–

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2} = \frac{6.77 \times 10^3}{(2 \times \pi \times 20 \times 10^3)^2} = 42.9\mu s$$

$$t_2 = \frac{2D}{2\pi f_n} = \frac{0.707}{\pi \times 20 \times 10^3} = 11.2\mu s$$

$$t_1 = 31.7\mu s \; C = \frac{t_1}{R_1} = 1.6nF$$

$$R_2 = \frac{t_2}{C} = 7k\Omega$$

SL6640 and SL6650

for single conversion receivers with quadrature detectors

The SL6640 and SL6650 are illustrated in Fig.26. Each consists of an IF limiting preamplifier, a main limiting amplifier, a quadrature detector, a squelch system, and a DC audio gain control. In addition, the SL6640 contains a low-power audio output stage.

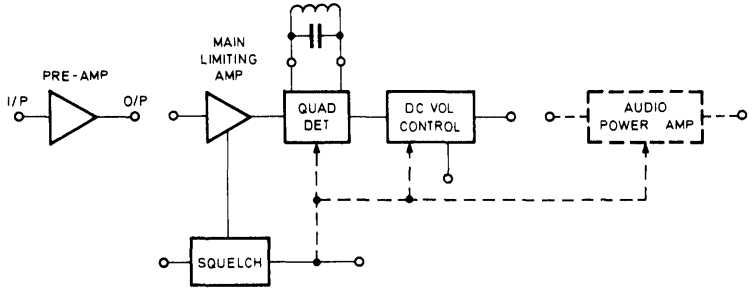


Fig. 26 Block of SL6640 and SL6650 (broken line applies to SL6640 Only)

The IF preamplifier has a bandwidth of 25 MHz, a gain of about 46 dB (200 times), and an input impedance of 5 kΩ shunted by 2 pF. It consists of five cascaded long-tailed pairs and has excellent limiting characteristics.

The main IF amplifier also has a bandwidth of 25 MHz but its gain before limiting is about 60 dB (1000) and it consists of six long-tailed pairs. The third and sixth of these stages contain detectors, the outputs of which drive the squelch system. The output of the limiting amplifier feeds a double-balanced modulator and also an external phase-shift circuit which in turn feeds the other port of the double-balanced modulator. This double-balanced modulator thus acts as a quadrature detector. The quadrature detector in the SL6640 and SL6650 has very good performance when demodulating narrow band FM signals, even when working with intermediate frequencies of up to 21.4 MHz. This is because at over 50 kΩ, the impedance of the quadrature port is high and so the Q of the quadrature circuit is not impaired by being loaded, as is so often the case with integrated circuit quadrature detectors.

The external phase shift circuit is fed via internal capacitors of only 2 pF and so the quadrature circuit works well only at about 4.5MHz and above. The SL6640 and SL6650 cannot, therefore, be used at the common 455kHz IF. The SL6690 (see below) works very well at this frequency, however, and should be used when 455kHz operation is required.

The audio output from the quadrature circuit goes to an audio amplifier which is DC-controlled to allow the use of remote gain control. The output of the SL6650 is taken from this gain control, but the SL6640 has an extra audio amplifier capable of driving a small 8Ω loudspeaker.

The squelch system is driven by the detectors in the IF strip and contains a comparator which requires an input to set the squelch level. A resistor between

this programming input and the squelch output provides hysteresis to the system. In the SL6650 the squelch system merely provides a DC output to indicate the presence of a signal larger than the squelch threshold but in the SL6640 the squelch controls the power supply to both the detector and the audio stages. The standby power of the SL6640 is thus the lower even though it is the more complex circuit.

The SL6640 is manufactured in an 18 lead DIL package and the SL6650 in a 16 lead DIL. The devices are designed so that as many as possible of their pins are common i.e., pins 1 to 6 are identical and pins 13 to 18 of the SL6640 are equivalent to pins 11 to 16 of the SL6650 and only the pins around the audio stages differ. This allows similar board layout to be used in radios using the SL6640 or the SL6650. In the pin-by-pin description which follows, pin numbers are given for the SL6640, those of the SL6650, where they differ, are given in brackets e.g., pin 18 (16).

Pin 1 is the bias point for the main IF amplifier. It must be decoupled effectively by an RF capacitor to ground and connected by a coil or resistor to the IF input, pin 14 (12). If a resistor is used, it should provide the correct match for the interstage filter; if a coil is used it will probably be part of the filter and must not have any DC connection to ground. The decoupling capacitor must be at least 0.01 μF.

Pin 2 is the squelch programming point and pin 3 the squelch output pin. The squelch level is set by a 470 kΩ variable resistor (which should be increased to 1 MΩ if supplies of over 6V are used) in series with a 47 kΩ resistor between pin 2 and ground. Squelch sensitivity increases with the value of the variable resistor. Pin 3 is at a high potential when no signal is present and drops to near ground potential when a signal is detected. The output current from pin 3 is less than 2 mA but it may, of course, be buffered if necessary.

The decoupling capacitor of 0.33 μF on pin 3 prevents brief breaks in signal (such as mobile flutter) from squelching the circuit. Hysteresis in the squelch is obtained by a resistor connected between pins 2 and 3. The amount of

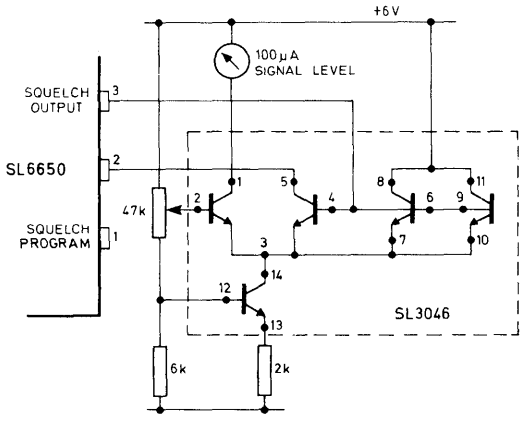


Fig. 27 'S' meter circuit for use with SL6650

hysteresis depends on the squelch threshold, the resistor value and the supply voltage. At 6V supply a 390 kΩ resistor gives 3 to 4 dB hysteresis at 10 μV squelch level and about 10 dB at 100 μV squelch level. Larger resistors are necessary at higher supply voltages and the minimum possible hysteresis rises to about 7 dB with a 1.5 MΩ resistor and a 9 V supply. Despite its variation with supply voltage, the squelch is quite stable with temperature and alters by only 1 to 2 dB as the circuit is temperature cycled. If squelch is not required the SL6650 squelch pins may be used, with an SL3046 transistor array, to drive an S meter as shown in Fig.27. The system consists of a negative feedback amplifier and is not possible with an SL6640, where the internal squelch must always be used.

The quadrature circuit is connected between pins 4 and 5. This can consist of an LC tuned circuit resonant at the centre of the IF passband, or one of the commercial crystal quadrature circuits for NBFM, or even a ceramic interstage filter such as is made for broadcast receiver applications. Ceramic filters usually need to be tuned by a parallel trimmer capacitor and their efficiency as quadrature elements can vary widely from batch to batch. They are not, therefore, the best quadrature elements to choose although they are non-microphonic and smaller than most coils. The resistive element of the impedance between pins 4 and 5 is over 50 kΩ and so has little effect on the Q of a wound quadrature element. Narrow FM can thus be demodulated, even with an LC quadrature element, with an excellent signal-to-noise ratio – 50 dB or better. If a lower Q is required the resistance between the pins may be reduced by the use of an external resistor.

No DC path must exist between pins 4 and 5 and any other point, but they themselves may be connected together if required. It is better to have a DC path between them than not, so long as it is not at the expense of the Q of the quadrature element.

The DC volume control consists of a fixed resistor of 47 kΩ in series with a variable resistor of 470 kΩ connected between pin 6 and ground. The gain range is typically 70 dB (3000:1) and gain is minimum when resistance is minimum.

Pins 12 and 13 of the SL6640 and pin 11 of the SL6650 are the supply pins. SL6640 pin 12 is the audio output stage supply while pin 13 supplies the remainder of the circuit. In the case of the SL6650 pin 11 is the supply connection for the entire circuit. The supply voltage is normally +6V but the circuits will work with supplies between +5V and +9V. Consumption of the SL6640 at 6V is 3.5mA (squelched) and 10mA (unsquelched), or more if audio power is being supplied, while the SL6650 draws 6mA in either case. Pin 12 of an SL6640 may be left unconnected if for any reason the audio stage is not required but it must not be used with more than 0.5V difference in potential between pins 12 and 13.

The power supplies must be well decoupled at RF with at least 0.1μF having low inductance and short leads. The supplies should also have low audio ripple and it is necessary to decouple the SL6640 supply very thoroughly at LF if the audio stage is to operate at its highest powers and retain its AM rejection.

Pin 14 (12) is the input of the main IF amplifier and should be biased by being connected to pin 1 as described above. The input impedance is 5 kΩ shunted by 2 pF.

Pins 15 (13) and 17 (15) are decoupling points within the circuit and should be decoupled to earth by good RF capacitors, preferably 0.1 μF and at least 0.01 μF. Inadequate decoupling of these pins causes poor AM rejection and can cause instability.

Bias circuitry for both the main amplifier and the preamplifier is shown in Fig.28. The preamplifier input is pin 16 (14). It is not self biased but is fed with bias from pin 18 (16) via a total of about 15 kΩ. The input impedance of the preamplifier is 5 kΩ shunted by 2 pF. If, as is common, the preamplifier is fed from a filter requiring a precise match, the value of resistor R2 should be chosen to provide this. The source impedance driving the preamplifier should be 750 Ω or less to prevent instability. The input signal should be fed to pin 16 (14) via a capacitor or other DC block. The sum of resistors R1 and R2 should be 15 kΩ and their junction well decoupled at HF. The noise figure of the preamplifier is 7 dB when driven by 350 Ω.

The preamplifier output is pin 18 (16) and it has an output impedance of 300 Ω. Signal is taken from the output of the preamplifier to the input of the

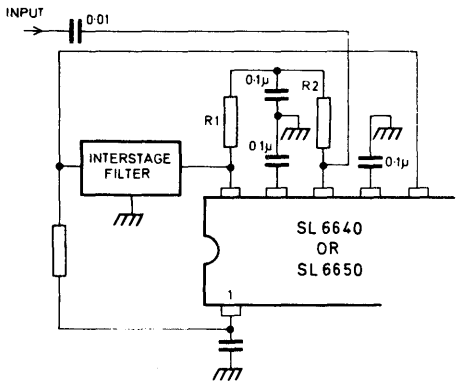


Fig. 28 Bias circuit for SL6640 and SL6650

main amplifier via an interstage filter. This is a roofing filter to provide some limitation of noise bandwidth, not the primary selectivity of the receiver which must be provided by a high performance filter placed before the preamplifier. This filter, therefore, need have neither a good shape factor nor large stop-band attenuation. Any simple filter is suitable but at 10.7 MHz, cheap ceramic filters are particularly useful since they are small and require no setting-up. Much work with the SL6640 and SL6650 has used Murata SFE 10.7 MA filters since they match the output impedance of the preamplifier.

The final part of this section deals with those pins whose functions differ between the SL6640 and the SL6650. First the SL6640. Pin 7 is the output of the DC controlled audio preamplifier and is an emitter follower with a low current tail. It will only drive high impedance loads and needs an HF rolloff capacitor to earth of $\frac{0.01\ \mu F}{f}$ where f is the desired rolloff frequency in kHz.

In normal use pin 7 is connected to pin 8, the input to the output stage, by a 0.1 μF capacitor. Pin 8 is biased by connecting it to the centre of two 220 kΩ resistors connected between the positive supply and ground in series.

Pin 9 of the SL6640 is the inverting input to the output stage and is used to provide negative feedback to define both DC operating point and stage gain. The feedback resistor from the output pin 11 is 120 kΩ and the gain-defining resistor (which is connected from pin 9 to ground via an isolating capacitor of 1 μF) can be any value greater than 1.2 kΩ. The gain is equal to the ratio of these two resistors, and hence when the smaller is 1.2 kΩ the gain is 40 dB (100). Attempts to achieve higher gain leads to instability and, more important, excessive distortion since the open loop gain of the output stage is only some 55 dB.

Pin 10 is earth and pin 11 is the audio power output. Pin 11 is decoupled to earth with 0.22 μF to ensure HF stability and drives its load via a 100 μF capacitor. With care, and a 9V supply, the SL6640 will drive an 8Ω loudspeaker at 250mW but a more practical figure is around 175mW. A complete circuit diagram of an SL6640 in use is shown in Fig.29.

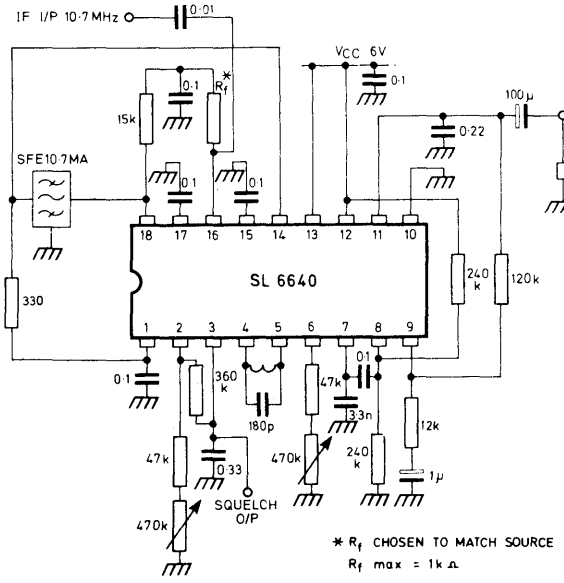


Fig. 29 10.7MHz application of SL6640

Pins 7 and 9 of the SL6650 are unused. Pin 8 of the SL6650 is earth and pin 10 is the audio output. This output appears on the open collector of a transistor and so must be connected to the positive supply by a resistor – generally 10kΩ. Audio is taken through a capacitor and the pin is also decoupled at HF.

by a capacitor of $\frac{0.015\ \mu F}{f}$ where f is the cutoff frequency in kHz.

SL6690

ultra-low power consumption quadrature detector system

The SL6690 block diagram is shown in Fig. 30. The circuit consists of a limiting IF amplifier which drives a quadrature detector, an LF amplifier and Schmitt trigger (which can be used either as a signal-to-noise squelch system or as a squarer when the circuit is used in a pager), and a voltage regulator which uses an external PNP transistor.

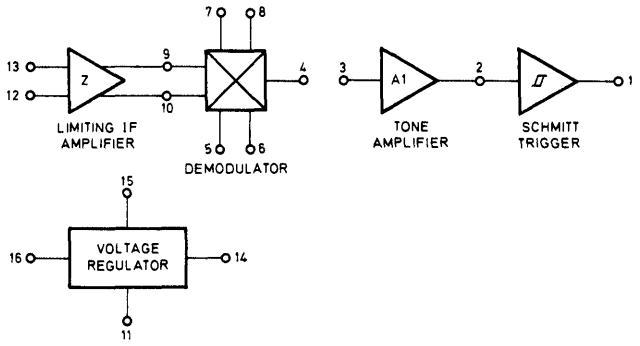


Fig. 30 SL6690 block diagram

The IF amplifier has a bandwidth of 1.5 MHz, making the circuit particularly useful at the popular communications and paging IF of 455 KHz. Its input impedance is 20 kΩ shunted by 2 pF and its output impedance is about 2 kΩ. Bias is obtained by DC feedback from the outputs to the inputs.

The quadrature detector is a conventional double-balanced modulator using transistor tree techniques. The quadrature circuit is an external LC tuned circuit and the capacitors driving the quadrature circuit are also external, which allows the detector to be used down to VLF as well as up to about 1.5 MHz.

The LF amplifier has a gain of 54 dB and is biased by a DC connection from its output to its input. It is an inverting amplifier so its gain and frequency characteristics may be defined by negative feedback. The Schmitt trigger is driven directly by the LF amplifier. Its output is a free collector which may be connected to either V_{CC} (the regulated supply) or the unregulated supply rail. In its ON state it will sink up to 150 μA.

The regulator, which requires an external series PNP transistor, allows the SL6690 to work from supplies between +2.5 and +6V. The external transistor is necessary because monolithic PNP transistors have poor h_{fe} at very low current levels.

Pin 1 is the Schmitt trigger output, a free collector which can sink up to 150 μA when the transistor is turned on and can rise to either V_{CC} or some other positive rail up to +6V when turned off. The input to the Schmitt trigger and the output of the LF amplifier are connected internally and the node brought out to pin 2. Bias must be taken from this pin to the LF amplifier input, pin 3,

via a resistance of 50 kΩ or less. The LF amplifier inverts and its gain and passband may be defined by negative feedback. An output may be taken from pin 2 and the Schmitt trigger left unused in which case no connection need be made to pin 1. The bias of the amplifier/Schmitt combination is sufficiently accurate to give the Schmitt an output mark-space ratio of between 0.9:1 and 1.1:1 with a sine wave input to the amplifier. The LF amplifier input impedance is 50 kΩ and its open loop gain roughly 54 dB.

No DC connections should be made from pin 3 except the bias connection to pin 2; all inputs should be coupled via capacitors. To prevent HF instability 2.2 kΩ in series with 120 pF should be connected from pin 2 to ground.

The output of the quadrature detector is pin 4 and its output impedance is 1 kΩ. The detector will give an output of 10 mV/Degree phase change and distortion of about 3 per cent (more if a ceramic resonator is used as a quadrature element). A single filter capacitor removes RF from the detected output.

The quadrature circuit is connected between pins 5 and 6 and may be a parallel tuned LC circuit or a ceramic resonator. The port has an input impedance of 50 kΩ shunted by 2 pF. The quadrature circuit may or may not present a DC path between the two pins. Use of ceramic quadrature elements usually results in greater distortion than the use of LC elements but such ceramic elements occupy less space and do not require adjustment. The quadrature circuit is driven by the output from pins 7 and 8 via two capacitors. Pin 7 drives pin 5 and pin 8 drives pin 6. The value of the capacitors depends on the frequency of operation and the quadrature circuit used.

Pins 9 and 10 are the outputs of the IF amplifier and are used to provide bias to its inputs. A 100 kΩ resistor is connected from pin 10 to pin 12 and pin 12 is grounded at AC by a capacitor. Pin 9 is connected to pin 13, the signal input pin, by another 100 kΩ resistor in series with a resistor of the correct value to terminate the IF source. The junction of the two resistors is decoupled at RF by a low inductance capacitor. The IF input is applied to pin 13 from the IF filter, via a coupling capacitor if necessary to isolate pin 13 at DC.

Pin 11 is earth and pins 14, 15, and 16 the supply/regulator pins. The supply, which may be between 2.5V and 6V is applied to pin 16 and to the emitter of a high gain PNP transistor whose base is connected to pin 15 and collector to pin 14. Pin 14 is stabilised at 2V and must be thoroughly decoupled at RF by a 0.1μF capacitor. The SL6690 may be turned on in 12 milliseconds or less so the power supply may be strobed in paging applications so that the mean power dissipation in the circuit is an order of magnitude lower than its normal 2mW (1mA @ 2V).

FM RECEIVERS USING SL6000 SERIES

The SL6600, SL6640, SL6650 and SL6690 are intended for use in NBFM receivers – mobile, hand-portable, base station and paging. They are all intended for use as IF Amplifier/Detector/Squelch modules and, of course, the SL6640 has a low power audio output stage.

The circuits, having low power consumption and, indeed, limiting amplifiers, have low resistance to intermodulation (although they have excellent dynamic range) and must be used after the main selectivity of the receiver. Modern receiver design emphasises strong signal performance even at the expense of sensitivity and hence front ends having much gain are not popular. This can

leave an uncomfortable gap between the 2 to 4 μV output from a receiver filter and the 10 μV or so that these circuits require to give an adequate signal-to-noise ratio. Redesign of the front end to give slightly more gain is possible and certainly the easiest solution but it may produce an unacceptable reduction in intermodulation performance. An amplifier is therefore needed between the filter and the SL6600/40/50/90.

This amplifier can be a convenience (some filters have matching impedances so high that even the input impedances of these circuits are embarassingly low) but, preceeding as it does a very high gain integrated circuit, it can suffer from stubborn instability. It also increases the power consumption of the receiver which is annoying in a hand-portable, although a hand-portable with its limited antenna is most likely to be able to tolerate a higher gain front end and hence least likely to need an extra stage of IF gain.

Suitable amplifiers may be made with a single transistor or FET and two circuits are shown in Fig.31. The FET circuit uses more current and an FET with a good performance at 1 mA and a low pinch-off voltage is required. The transistor circuit is far less demanding but has a lower input impedance (which depends on h_{fe} and C_{ob} and will vary from device to device). These amplifiers must be very well isolated if the receiver is to be stable and the powerful decoupling of the transistor circuit is a point in its favour.

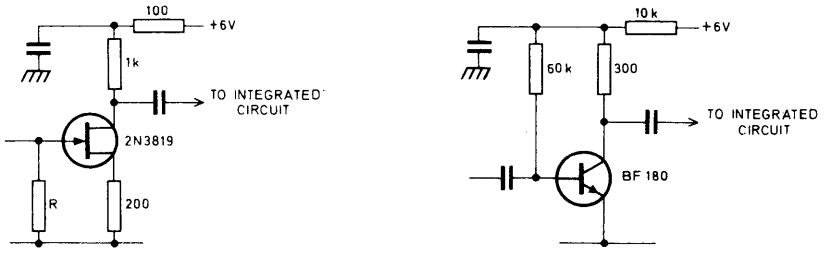


Fig. 31 FET and bipolar buffer amplifier

Apart from the occasional necessity for a low-gain preamplifier these circuits present few problems and are very easy to use. As mentioned above, some attention must be paid to layout to isolate input and output, particularly at the same frequency, as much as possible. Other points to be remembered are the use of non-inductive capacitors (many capacitors are inductive at frequencies as low as 5 MHz) and adequate decoupling of all bias points and power supplies – in connection with this it is worth remembering that it is useless to use a good RF capacitor with short leads if the printed connection to it is long and narrow.

It is not intended to describe in detail the design of any complete receivers using these circuits. However, a review of the various types of receiver where these circuits may be used and the considerations affecting such use is given below.

LAND MOBILE RADIOS

In the VHF or UHF bands land mobiles use narrow deviation FM (between 1.5 and 12kHzΔf) and generally use a first IF of 10.7 or 21.4MHz. Transceivers can be hand-held or vehicle mounted. For hand-held transceivers the choice is between the SL6600 which has low power consumption and can be strobed and the SL6640 which has an integral output stage. The signal-to-noise ratio of either circuit is adequate when used with the recommended circuitry but there is a performance difference. The capture effect of a PLL detector is much better than that of a quadrature detector: a receiver using an SL6600 will capture the stronger of two co-channel signals even if it is only stronger by 2 to 4dB. The SL6640 will be affected by a co-channel interfering signal until it is 20dB or more below the wanted signal. Both features can be valuable; some (including military) users need to know of other signals on-channel while others, particularly in areas where channels are shared with space diversity, prefer systems which ignore low-level co-channel interference.

An advantage of the SL6640 is that it has only one conversion, saving a crystal (although the crystal used with the SL6600 need not be expensive since the main selectivity of the receiver preceeds the SL6600 and slight frequency drift in the second crystal oscillator will not move the signal out of the detector or squelch passband) and eliminating the possibility of 'birdies' from a second oscillator. Most manufacturers' quadrature detectors, having been designed primarily for TV use, require a low IF if they are to give an adequate signal-to-noise ratio at low deviations but the SL6640 and SL6650 are capable of giving over 50dB signal-to-noise ratio with deviations as low as 1.5kHz at an IF of 10.7MHz.

In land mobile applications with FM deviations in the range 1.5 to 12kHz the SL6600 is used with a second IF of 100kHz. The design of the loop filter depends on the deviation and audio bandwidth (generally 3kHz for speech) as mentioned above. The double conversion can ease problems of instability if it is necessary to use an amplifier between the quartz filter and the SL6600 since the total gain of the first IF is not so high.

PAGING RECEIVERS

Using the SL6690 a paging receiver can run on only two cells and consumes only 2 mW, which may be further reduced to as little as 100μW if the receiver is strobed. Such pagers are small, simple, inexpensive, and use few components.

BROADCAST F.M. RECEIVERS AND TV SOUND IF SYSTEMS

These can use the SL6640/50 merely by using a quadrature element with lower Q to accommodate the wider deviation. The circuit alteration can be as simple as the addition of a resistor between pins 4 and 5 to load the quadrature coil, although the main selectivity of the receiver must be suitable for the bandwidth of the new type of signal. The SL6640 is especially useful in portable FM receivers in that it will supply adequate power to a loudspeaker but consumes only a few milliamps, porlonging battery life.

The SL6600 is less suitable for broadcast applications, although it works very well when it is used with a second IF around 800kHz and gives particularly low distortion due to its PLL detector. Its disadvantage is the cost of the crystal in the second converter although this is not too great and might be overcome by the use of a series resonant LC tuned circuit.

OTHER APPLICATIONS

These circuits can be used in various applications, including microwave and telemetry receivers and, with the SL6640/50, simple SSB receivers requiring very low power.

The choice of circuit in any application depends on a number of factors including deviation and type of modulation. In general, providing the shift is not too great, the SL6600 is better for RF FSK, although the loop filter design requirements will differ from those described above when the modulation departs so far from sinusoidal. On the other hand the SL6640/50 will cope with deviations of 2 to 3MHz providing an IF of twenty-odd MHz is used and the quadrature element has low enough Q.

Using the SL6640/50 as an SSB receiver involves replacing the quadrature circuit with a BFO so that the detector works as a product detector, and applying the AGC, preferably audio-derived with an SL621 or similar system, to an amplifier preceeding the SL6640/50 to prevent its IF amplifier from limiting.

HIGH SPEED DIVIDERS

Introduction to SP8000 series

The SP8000 Series is a range of high speed digital dividers using ECL techniques. Devices with division ratios from ÷2 to ÷256 are available and some types operate at frequencies up to 1.5GHz. To describe the various types in full is outside the scope of this book. However, since high speed dividers have numerous applications in radio systems, a brief description of the range and some notes on applications for the circuits will be given.

SP8000 PRODUCT RANGE

Divide by	Product	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Control input		Output		Package		
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	TTL	ECL	Metal can	Ceramic	Plastic
3/4	SP8720A	●				300		●			40		●		●		●	
5/6	SP8692A	●				200	●				14	●	●	●	●		●	
	SP8692B				●	200	●				14	●	●	●	●		●	
	SP8740A	●				300		●			45		●		●		●	
	SP8740B				●	300		●			45		●		●		●	
6/7	SP8741A	●				300		●			45		●		●		●	
	SP8741B				●	300		●			45		●		●		●	
8/9	SP8691A	●				200	●				14	●	●	●	●		●	
	SP8691B				●	200	●				14	●	●	●	●		●	
	SP8743A	●				500		●			45	●	●		●		●	
	SP8743B				●	500		●			45	●	●		●		●	
10/11	SP8690A	●				200	●				14	●	●	●	●		●	
	SP8690B				●	200	●				14	●	●	●	●		●	
	SP8647A	●				250	●	●			50		●	●	●		●	
	SP8647B				●	250	●	●			50		●	●	●		●	
	SP8643A	●				350	●	●			50		●		●		●	
	SP8685A	●				500		●			45	●	●		●		●	
	SP8685B				●	500		●			45	●	●		●		●	
	SP8680A	●				600		●			90	●	●	●	●		●	
	SP8680B				●	600		●			90	●	●	●	●		●	
20/22	SP8785M		●			1000		●			85		●		●		●	
	SP8785B				●	1000		●			85		●		●		●	
	SP8786M		●			1300		●			85		●		●		●	
	SP8786B				●	1300		●			85		●		●		●	

Table 2 Two-Modulus SP8000 series high speed dividers

Divide by	Product	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	Metal can	Ceramic	Plastic
2	SP8604A	●				300		●			12		●	●		
	SP8604B				●	300		●			12		●	●		
	SP8602A	●				500		●			12		●	●		
	SP8602B				●	500		●			12		●	●		
	SP8607A	●				600		●			14		●	●		
	SP8607B				●	600		●			14		●	●		
	SP8605M		●			1000		●			70		●		●	
	SP8605B				●	1000		●			70		●		●	
	SP8608M		●			1000			●		70		●		●	
	SP8608B				●	1000			●		70		●		●	
	SP8606M		●			1300		●			70		●		●	
	SP8606B				●	1300		●			70		●		●	
	SP8609M		●			1300			●		70		●		●	
	SP8609B				●	1300			●		70		●		●	
4	SP8790A	●				60	●	●			8	●		●		
	SP8790B				●	60	●	●			8	●		●		
	SP8601A	●				150		●			18	●	●	●		
	SP8601B				●	150		●			18	●	●	●		
	SP8600A	●				250		●			16	●	●	●		
	SP8600B				●	250		●			16	●	●	●		
	SP8610M		●			1000		●			70		●		●	
	SP8610B				●	1000		●			70		●		●	
	SP8617M		●			1300			●		80		●		●	
	SP8617B				●	1300			●		80		●		●	
	SP8611M		●			1500		●			70		●		●	
	SP8611B				●	1500		●			70		●		●	
	SP8619M		●			1500			●		80		●		●	
	SP8619B				●	1500			●		80		●		●	
5	SP8620A	●				400		●			55		●		●	
	SP8620B				●	400		●			55		●		●	
8	SP8794A	●				120	●	●			10	●		●		
	SP8794B				●	120	●	●			10	●		●		
	SP8670A	●				600		●			45		●		●	
	SP8670B				●	600		●			45		●		●	
	SP8735B				●	600		●			70	ⓑ	●		●	
	SP8677M		●			1200			●		70		●		●	
	SP8677B				●	1200			●		70		●		●	

Table 3 Fixed-Modulus SP8000 high speed dividers

Divide by	Product	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)				Supply current (mA)	Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8	7.4		TTL	ECL	Metal can	Ceramic	Plastic
10	SP8660A	●				200	●	●			10	●		●		
	SP8660B				●	200	●	●			10	●		●		
	SP8660			●		200	●	●			10	●				●
	SP8632B				●	400		●			70		●		●	
	SP8637B				●	400		●			75	ⓑ	●		●	
	SP8630A	●				600		●			70		●		●	
	SP8630B				●	600		●			70		●		●	
	SP8635B				●	600		●			75	ⓑ	●		●	
	SP8634B				●	700		●			75	ⓑ	●		●	
	SP8665B				●	1000			●		80		●		●	
	SP8667B				●	1200			●		80		●		●	
16	SP8659A	●				200	●	●			10	●		●		
	SP8659B				●	200	●	●			10	●		●		
	SP8650A	●				600		●			45		●		●	
	SP8650B				●	600		●			45		●		●	
20	SP8657A	●				200	●	●			10	●		●		
	SP8657B				●	200	●	●			10	●		●		
	SP8658			●		200	●				20	●				●
24	SP8656			●		200	●				20	●				●
32	SP8655A	●				200	●	●			10	●		●		
	SP8655B				●	200	●	●			10	●		●		
64	SP8755A	●				1200	●				45	●			●	
	SP8755B				●	1200	●				45	●			●	
	SP8750B				●	1000			●		68	●			●	
	SP8752M		●			1200			●		68	●			●	
80	SP8627			●		150	●	●			33	●				●
100	SP8628			●		150	●	●			33	●				●
	SP8629			●		150	●	●			33	●				●

Table 3 *(continued)*

CIRCUIT DESCRIPTIONS

Table 3 summarises the SP8000 range of fixed modulus dividers (i.e. those which divide by a single ratio) and Table 2 summarises the two-modulus programmable dividers (i.e. those dividing by N or N + 1 depending on the state of a control input). It will be seen that there are a wide number of division ratios and input/output interfaces but all the devices in the SP8000 range use emitter coupled logic (ECL) chip circuitry.

The signal inputs of SP8000 devices can be differential or single-ended and DC or AC coupled depending on the particular device. Signal is supplied to AC coupled devices via an isolating capacitor (usually about 1000pF) but DC coupled devices have no internal bias circuitry and may be driven either from ECL II or ECL III or be driven with AC via a capacitor and biased by a separate external resistor network.

The datasheet for each device states which of the two ECL families is appropriate and also describes the bias network. Devices with balanced inputs may be driven with a differential signal, or a single signal may be applied to one input and the other decoupled to ground by a 1000pF capacitor.

If no signal is applied to a balanced input the device will tend to oscillate at some ill-defined but high frequency. This may be prevented by applying a bias to one of the inputs by means of a resistor connected from the input to one or other of the supplies. This has the effect of desensitising the input but preventing oscillation – the exact value of the resistor depends on the device used but is generally around 10 kilohms. SP8000 series devices will operate with sinewave inputs at high frequencies but low frequency sine inputs may cause malfunction.

Dividers specified to have maximum operating frequencies of 700 MHz or more should not be used with sine inputs under 80MHz. At frequencies lower than this they should be driven with square wave inputs having rise and fall rates in excess of 200V/microsecond. Lower frequency dividers may be used with sine inputs down to 40MHz and then with square waves with 100 microsecond rise and fall times. Some SP8000 circuits are less demanding – details are given in their respective data sheets.

The input signal required by SP8000 series circuits for satisfactory operation is between 400 and 800mV peak-to-peak except in the case of one or two of the very high speed dividers which require a minimum of 600mV. Many dividers will operate with inputs well outside this range but it is unwise to allow them to do so as the circuit configurations used in the counters can lead to miscounting at certain frequencies if too high or too low an input level is used.

The control inputs of the two-modulus dividers are ECL-compatible.

The majority of SP8000 outputs are emitter followers, usually ECL-compatible, but some of the series have free collector or TTL compatible outputs. Many of the devices have both Q and $\overline{Q}$ and some of the decades have BCD outputs.

No particular problems arise in the output circuitry although the emitter follower outputs should not be used to drive capacitivie loads.

The SP8000 series circuits require 5.2V supplies except a few of the faster circuits, which require higher voltages such as 6.8V or 7.4V. The data sheets suggest the use of positive ground supplies; this has the advantage of minimising the risk of damage due to output short circuits but can be inconvenient if the dividers are to be used in conjunction with other integrated

circuits using the more conventional negative ground. But whether positive or negative ground is used it is most important that the power supplies be adequately decoupled. Quite small capacitors may be used — 100pF is more than ample and in some applications as little as 15pF has been shown to be sufficient.

The capacitors used must, however, be RF types having minimal lead and package inductance. The capacitors should be sited as close to the integrated circuits as possible and leads kept short. It is not use ensuring that a capacitor lead is short if the printed track to it is long and thin — board tracks must also be kept short and as wide as possible. A ground plane on one side of the circuit board with all ground connections made to it minimises lead inductance problems and is the best way to ensure satisfactory operation of any high speed or high frequency circuitry.

Similar care to that spent on decoupling should be lavished on the bias points in the circuit and the unused inputs. Capacitors need not be particularly large but must have good high frequency performances and very short leads and tracks.

MODULUS EXTENDERS FOR TWO-MODULUS DIVIDERS THE SP8790 AND SP8794

The SP8790 and the SP8794 are designed for use with two-modulus dividers to extend their division ratios and hence make them more suitable for use with CMOS and low power TTL. The SP8790 converts a $\div N/N+1$ counter to a $\div 4N/4N+1$ counter and the SP8794 converts it into a $\div 8N/8N+1$ counter.

Each device consists of a counter with a balanced AC-coupled input, a CMOS or TTL compatible output, and a control output designed to drive the control inputs of the SP8000 series of two-modulus dividers. There is also a control input which is CMOS or TTL compatible (but needs a 5 kilohm pullup resistor when used with TTL).

In use, the control input from the programmable divider goes to the control input of the SP8790 (or the SP8794) and is gated to the two-modulus divider once every four (or eight) counts. Fig. 32 shows an SP8790 used with an SP8690 to give a $\div 40/41$ counter; similar systems may be used with any of the SP8000 two-modulus dividers.

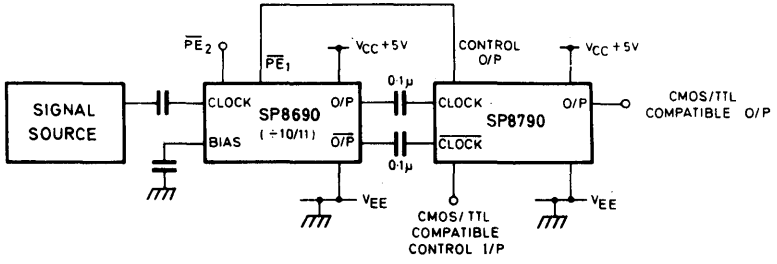


Fig. 32 SP8790 with SP8690 to give a ÷40/41

The SP8790 and SP8794 will normally be driven by SP8000 high speed dividers which have fast output edges. If other sources are used, however, the notes on input waveform slew rate in the preceding section should be observed. Again, the input should be biased if there is likelihood of instability in the absence of a signal, and the unused input should be decoupled to ground if only one input is required. The input level should be between 300mV and 1V peak-to-peak.

The internal delays in the SP8790 and the SP8794 do not allow their operation at input frequencies (to the SP8790 or SP8794) of over 40MHz as a controller. However, if the SP8790 or SP8794 are used as simple dividers they will work at over 60MHz and 120MHz respectively.

Both devices require a single 5V supply which must, as usual, be well decoupled. Neither device has any other points which need to be decoupled with the possible exception of unused inputs.

Input characterisation for the SP8000 series

Because of the wide frequency range of the SP8000 series emitter-coupled logic dividers, the input drive and impedance should be optimized.

The input impedance from 50MHz to 600MHz is mostly capacitive. Beyond 600MHz it becomes inductive.

To optimize the circuit to handle large overloads, small signals, and changes of input impedance versus operating frequency some suggestions are offered in Figs.33, 34 and 35.

Where the frequency range to be used covers an impedance change of greater than three to one, a circuit shown in Fig. 33 could be added to the input. By using the appropriate input impedance curve and calculating the value of R & L, the total input impedance would be more constant over the required frequency range.

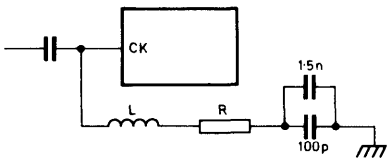


Fig. 33

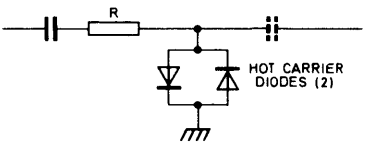


Fig. 34

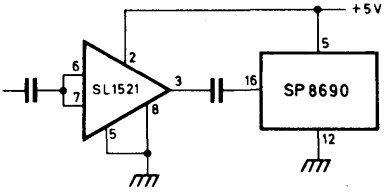


Fig. 35

In the case of large overloads the circuit shown in Fig. 34 could be used.

When using this circuit there is typically a 3dB loss in sensitivity but the dynamic range would be increased from two to one to over four to one. The value of R depends on the maximum overdrive voltage and the hot carrier diodes used.

For low level inputs an SL1521 wideband amplifier could be used as a preamplifier for a divider as shown in Fig. 35.

By using the SL1521 and the SP8690 low power 200MHz divide by 10/11 divider, as shown in Fig.35, the minimum sensitivity is reduced from 143mV RMS to 36mV RMS. Both units are self biased and require only coupling capacitors for interconnections. Also both parts operate from the same +5V supply at 145mW total power.

When using the SP8600 series it is recommended that good low inductance RF capacitors be used on all bias and power supply decoupling points.

The printed circuit board should be laid out with all input leads as short as possible, ample ground plane around the device and using other normal RF techniques.

SP8602,4,7

INPUT IMPEDANCE

The input impedance is shown in Fig.36 for the frequency range of 50MHz to 700MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.1pF.

TEST CIRCUIT

The test circuit is shown in Fig.37. All tests were made at 25°C.

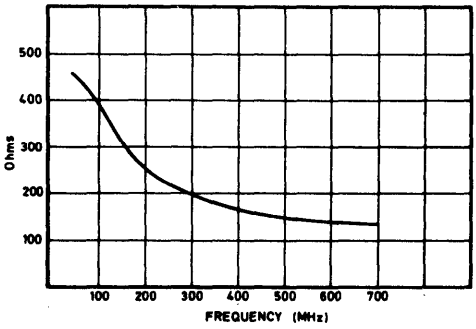


Fig. 36

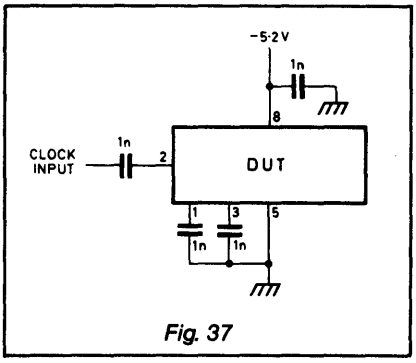


Fig. 37

SP8630,2

INPUT IMPEDANCE

The input impedance is shown in Fig.38 for the frequency range of 50MHz to 600MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.9F.

TEST CIRCUIT

The test circuit is shown in Fig. 39. All tests were made at 25°C.

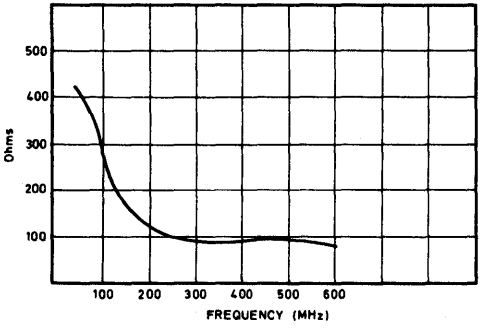


Fig. 38

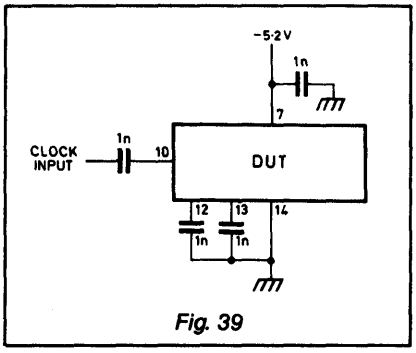


Fig. 39

SP8634,5,7

INPUT IMPEDANCE

The input impedance is shown in Fig. 40 for the frequency range of 50MHz to 700MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 4.1pF.

TEST CIRCUIT

The test circuit is shown in Fig. 41. All tests were made at 25°C.

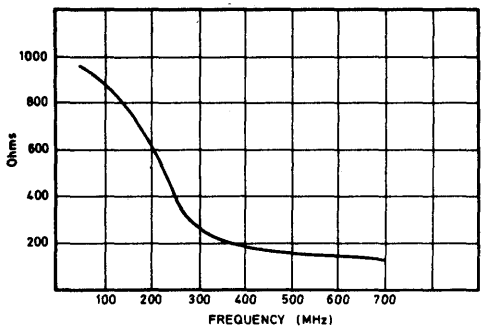


Fig. 40

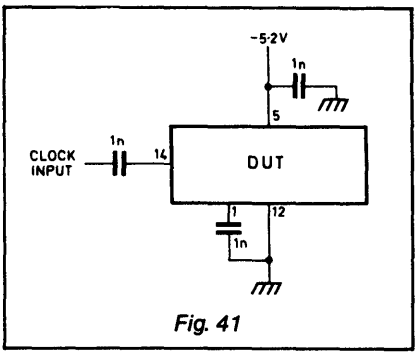


Fig. 41

SP8643,7

INPUT IMPEDANCE

The input impedance is shown in Fig. 42 for the frequency range of 50MHz to 350MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 2.4pF.

TEST CIRCUIT

The test circuit is shown in Fig. 43. All tests were made at 25°C.

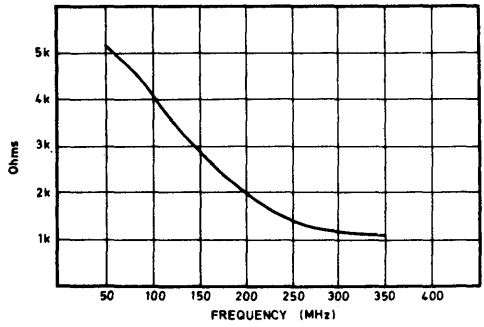


Fig. 42

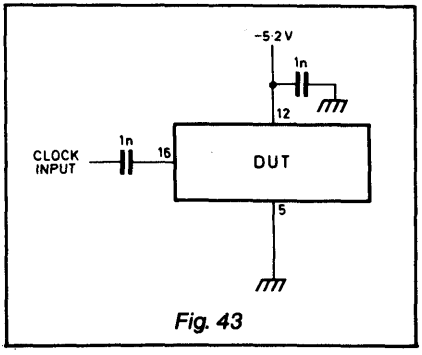


Fig. 43

SP8650

INPUT IMPEDANCE

The input impedance is shown in Fig.44 for the frequency range of 50MHz to 600MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 6.0pF.

TEST CIRCUIT

The test circuit is shown in Fig.45. All tests were made at 25°C.

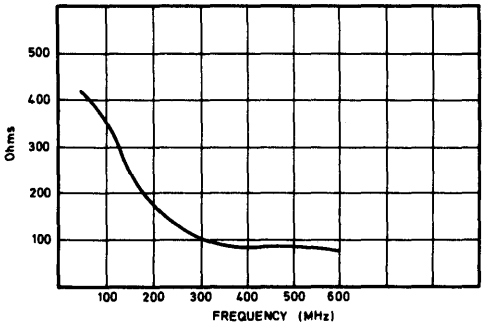


Fig. 44

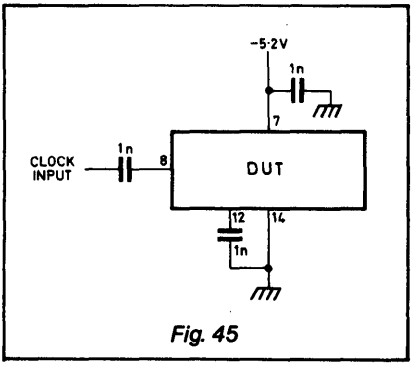


Fig. 45

SP8655,7,9

INPUT IMPEDANCE

The input impedance is shown in Fig.46 for the frequency range of 50MHz to 100MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 3.6pF.

TEST CIRCUIT

The test circuit is shown in Fig.47. All tests were made at 25°C.

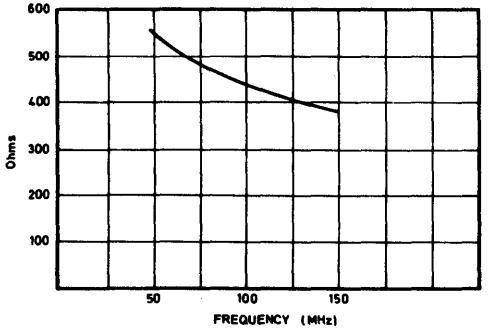


Fig. 46

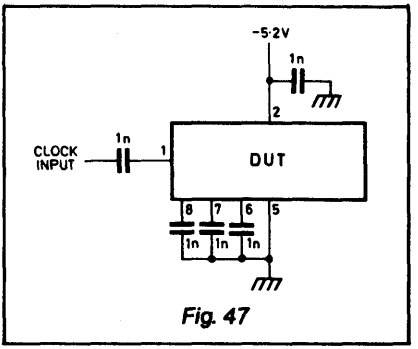


Fig. 47

SP8685

INPUT IMPEDANCE

The input impedance is shown in Fig.48 for the frequency range of 50MHz to 500MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 8.7pF.

TEST CIRCUIT

The test circuit is shown in Fig. 49. All tests were made at 25°C.

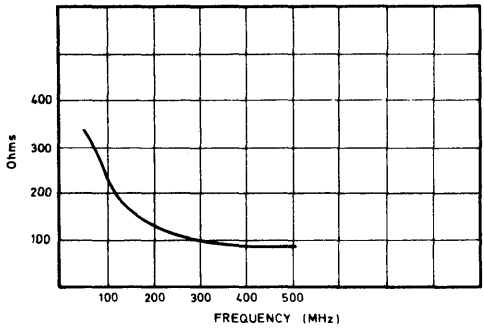


Fig. 48

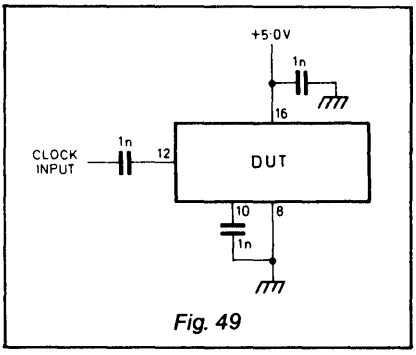


Fig. 49

SP8690

INPUT IMPEDANCE

The input impedance is shown in Fig. 50 for the frequency range of 50MHz to 200MHz.

INPUT CAPACITANCE

The capacitance at 50MHz is 6.4pF.

TEST CIRCUIT

The test circuit is shown in Fig. 51. All tests were made at 25°C.

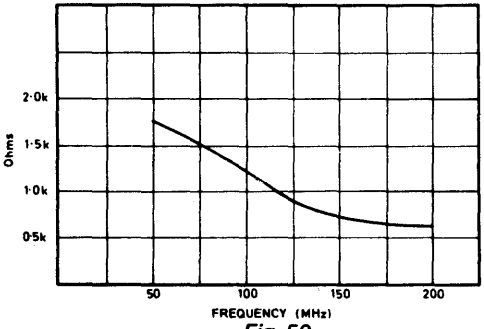


Fig. 50

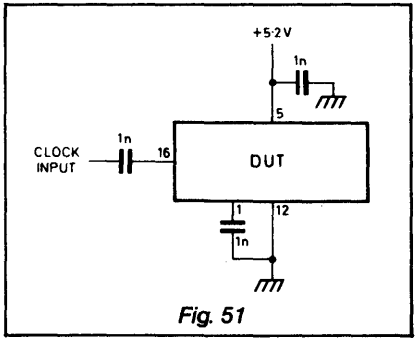


Fig. 51

Preamplifiers for SP8000 series

The availability of low-cost hybrid amplifiers with a performance extending to 1GHz, coupled with SP8000 High Speed Dividers, allows an unparalled increase in instrument performance.

For example, using an Amperex ATF 417 as a preamplifier for an SP8610 (with a Schottky barrier diode limiter), the divider's sensitivity can be improved by at least 15dB. The circuit diagram is shown in Fig.52. Typical room temperature performance is shown in Fig.53, and a suitable PCB layout is given in Fig 54.

Low end performance is limited by signal rise time requirements for the SP8610, whilst high end sensitivity is limited by the amplifier limiter performance. This can be improved by operating the ATF 417 off a higher supply. By increasing the supply to, say, +20V, a gain in sensitivity of, typically, 5dB would be expected at 1GHz.

Similar results can be obtained using the ATF 417 with other dividers such as the SP8667, 1.2GHz decade divider.

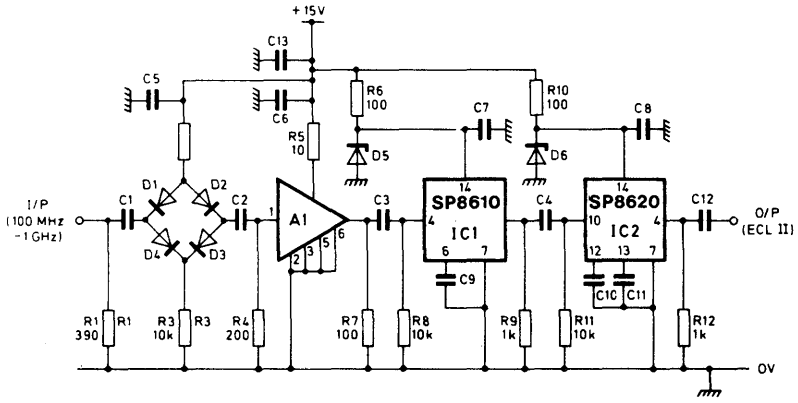


Fig. 52 UHF instrumentation ÷ 20 prescaler

COMPONENTS

D1 – D4	: Schottky barrier diodes, HP5082–2811
A1	: Hybrid amplifier, Amperex ATF417 or Philips OM185
IC1	: Plessey Semiconductors SP8610B
IC2	: Plessey Semiconductors SP8620B
D5, D6	: 1 Watt, 5.1V Zener diode
R6, R10	: 100 ohms, 5 Watt, e.g. Plessey GWT-5
C1 – C12	: 1nF ceramic, e.g. ITW EMCAPS
C13	: 0.33 microfarad

CIRCUIT DETAILS

The signal input (100MHz–1GHz) is AC-coupled to a Schottky barrier diode bridge which limits at 100mV p/p. The signal is then amplified by the hybrid

A1. This combination gives about 15dB of gain with a supply of 15V. The amplifier is AC coupled, via C3, to an SP8616 ÷4 circuit (IC1). R7 provides an input offset to prevent 'no signal' oscillation. The drive capability of IC1, is increased by R8 and its output capacitively coupled to IC2 via C4 R9 provides the input offset for IC2. The output of IC2 is suitable for driving ECL II.

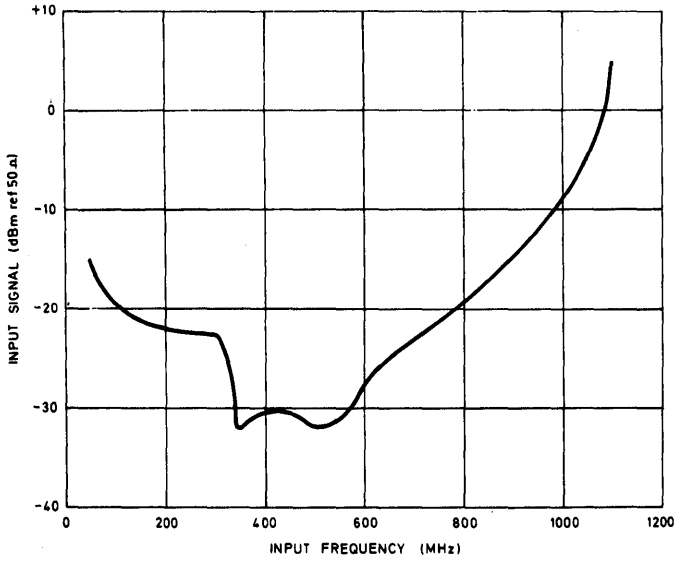


Fig. 53 Typical performance of UHF prescaler

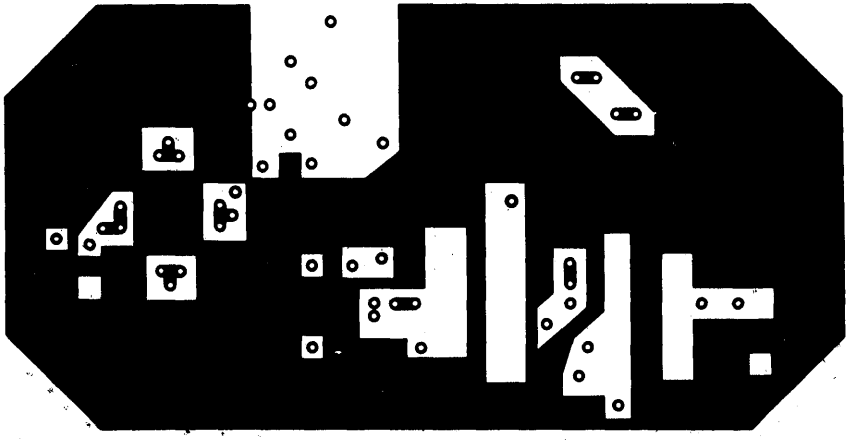


Fig. 54a Component side of board

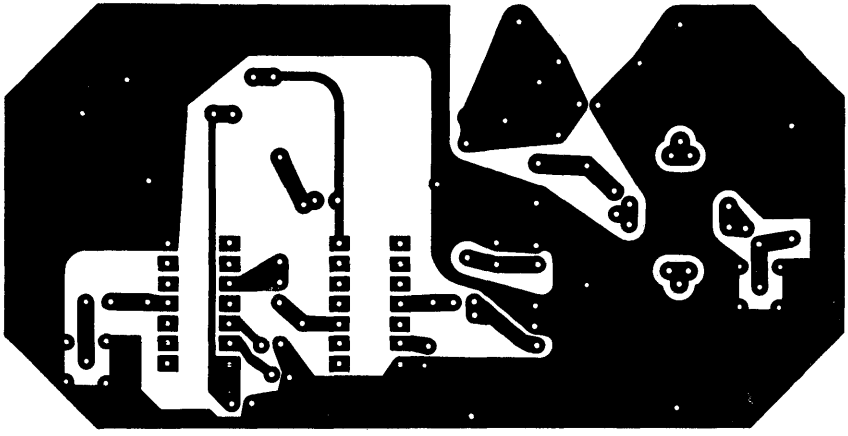


Fig. 54b Solder side of board

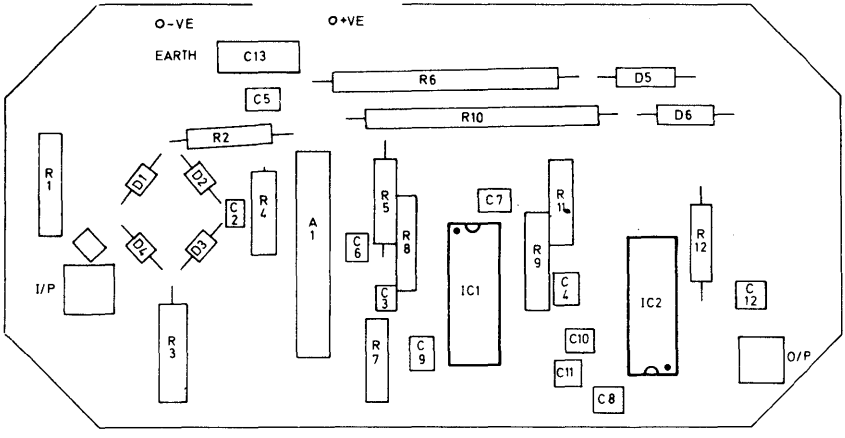


Fig. 54c Component location

SYNTHESISER CIRCUITS

Synthesiser Circuits

INTRODUCTION TO SYNTHESISER SYSTEMS

Fig. 55 shows a typical frequency synthesiser. It consists of a voltage controlled oscillator, a variable divider and a phase comparator. The output frequency of the VCO is a function of an applied control voltage. In frequency synthesisers the function is always monotonic and is generally as near linear as possible.

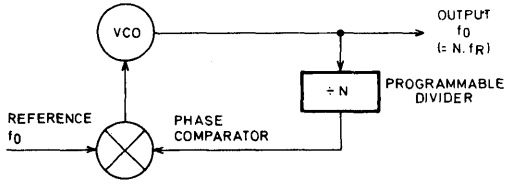


Fig. 55 Basic frequency synthesiser

The output of the phase comparator is a voltage which is proportional to the phase difference between the signals at its two inputs. This output controls the frequency of the VCO so that the phase comparator input from the VCO via the variable divider (÷N) remains in phase with the reference input, f_R, so that the frequencies are equal. The VCO frequency is thus maintained at Nf_R, Such a synthesiser will produce a number of frequencies separated by f_R and is the most basic form of phase locked synthesiser. Its stability is directly governed by the stability of the reference input f_R, although it is also related to noise in the phase detector, noise in any DC amplifier between the phase detector and the VCO and the characteristics of the low-pass filter usually placed between the phase comparator and the VCO.

The design of frequency synthesisers using the above principle involves the design of various sub-systems; including the VCO, the phase comparator any low-pass filters in the feedback path, and the programmable dividers. The following deals mainly with the design of dividers.

PROGRAMMABLE DIVISION

A typical programmable divider is shown in Fig. 56. It consists of three stages with division ratios K_1, K_2 and K_3 which may be programmed by inputs P_1, P_2 and P_3 respectively. Each stage divides by K_n except during the first cycle after the program input P_n is loaded when it divides by P (which may have any integral value from n to K). Hence the counter illustrated divides by $P_3(K_1K_2) + P_2K_1 + P_1$ and when an output pulse occurs the program inputs are reloaded. The counter will divide by any integer between 1 and $(K_1K_2K_3 - 1)$.

The commonest programmable dividers are either decades or divide-by-sixteen counters. These are readily available in various logic families, including CMOS and TTL. It is possible to buy quad decades in CMOS in a single package.

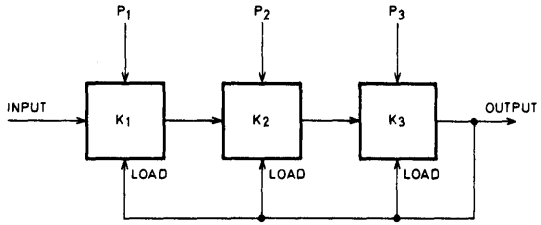


Fig. 56 Typical programmable divider

Using such a package one can program a value of N from about 3 to 9999. The theoretical minimum count of 1 is not possible because of the effects of circuit propagation delays. The use of such counters permits the design of frequency synthesisers which are programmed with decimal thumbwheel switches and use a minimum of components. If a synthesiser is required with less obvious frequencies and steps a custom programmable counter may be made using some custom logic family such as PMOS, NMOS, CMOS or I^2L.

The maximum input frequency of such a programmable counter is limited by the speed of the logic used, and more particularly by the time taken to load the programmed count. Few programmable counters of the type discussed will operate with test frequencies much above 5MHz. The faster types, operating perhaps 25 or 30MHz, use Shottky TTL which consumes considerable power and has a tendency to inject HF and VHF noise into supply lines. The output frequency of the simple synthesiser in Fig. 55 is of course limited to the maximum frequency of the programmable divider.

There are many ways of overcoming this limitation on synthesiser frequency. The VCO output may be mixed with the output of a crystal oscillator and the resulting difference frequency fed to the programmable divider; the VCO output may be multiplied from a low value in the operating range of the programmable divider to the required high output frequency. Alternatively, a fixed ratio divider capable of operating at a high frequency may be interposed between the VCO and the programmable divider. These methods are shown in Figs 57a, 57b and 57c respectively.

All the above methods have their problems although all have been used and will doubtless continue to be used in some applications. Method (a) is the most useful technique since it allows narrower channel spacing or higher reference frequencies (hence faster lock times and less loop-generated jitter) than the other two but it has the drawback that since the crystal oscillator and the mixer are within the loop, any crystal oscillator noise or mixer noise appears in the synthesiser output. Nevertheless, this technique has much to recommend it.

The other two techniques are less useful. Frequency multiplication introduces noise and both techniques must either use a very low reference frequency or rather wide channel spacing. What is needed is a programmable divider which operates at the VCO frequency — one can then discard the techniques described above and synthesise directly at whatever frequency is required.

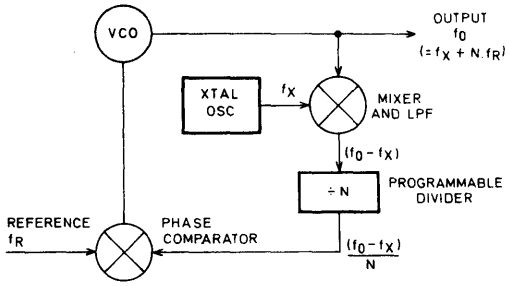


Fig. 57a Mixer synthesiser

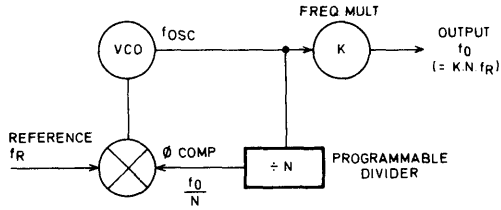


Fig. 57b Synthesiser with ouput multiplication

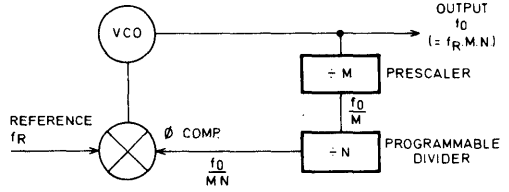


Fig. 57c Synthesiser with prescaler

TWO-MODULUS DIVIDERS

Considerations of speed and power make it impractical to design programmable counters of the type described above, even using ECL, at frequencies much into the VHF band (30 to 300MHz) or above. A different technique exists, however, using two-modulus dividers.

Fig. 58 shows a divider using a two-modulus prescaler. The system is similar to the one shown in Fig. 57c but in this case the prescaler divides either by N or N + I depending on the logic state of the control input. The output of the prescaler feeds two normal programmable counters.

Counters 1 controls the two-modulus prescaler and has division ratio A. Counter 2, which drives the output, has a division ratio M.

In operation the ÷N/N + I prescaler (Fig. 58) divides by N+I until the count in programmable counter 1 reaches A and then divides by N until the count in programmable counter 2 reaches M when both counters are reloaded, a pulse passes to output and the cycle restarts. The division ratio of the whole

system is A(N+1) + N(M—A), which equals NM+A. There is only one constraint on the system — since the two modulus prescaler does not change modulus until counter 1 reaches A the count in counter 2 (M) must never be less than A. This limits the minimum count the system may reach to A(N+1) where A is the maximum possible value of count in counter 1.

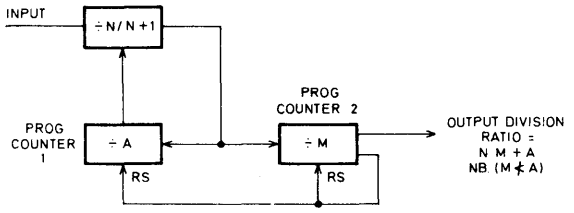
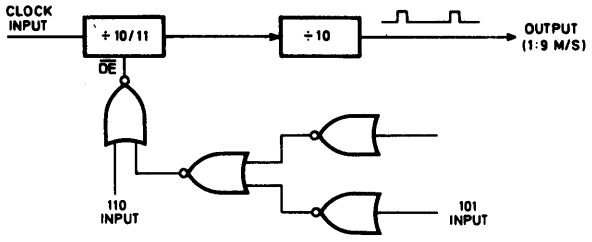


Fig. 58 Divider system with 2 modulus prescaler

The use of this system entirely overcomes the problems of high speed programmable division mentioned above. Plessey Semiconductors make a number of ÷10/11 counters working at frequencies of up to 500MHz and also ÷5/6, ÷6/7 and ÷8/9 counters working up to 500MHz. There is also a pair of circuits intended to allow ÷10/11 counters to be used in ÷40/41 and ÷80/81 counters in 25kHz and 12.5kHz channel VHF synthesisers.
It is not necessary for two-modulus prescalers to divide by N/N+1. The same principles apply to ÷N/N+Q counters where Q is any integer but ÷N/N+1 tends to be most useful.

If the limitation that M must not be less than A is unacceptable the system may be extended to use three or four modulus division. For example if a ÷10/11 prescaler is used in a VHF synthesiser to be programmed in decades the maximum value of A will be 9 and so the minimum frequency will be 99MHz (=A(N+1)). Suppose instead that a ÷100/101/110 counter (which may be made as shown in Fig. 59) is used in the system in Fig. 60. At the start of a cycle the counter divides by 110 until the programmable counter reaches A. This releases the inhibition on programmable counter 2 and the prescaler divides by 101 until counter 2 reaches A_2, at which point the prescaler divides by 100 until counter 3 reaches N and the cycle restarts. The division ratio is therefore $110A_1+101A_2+100(N—A_1—A_2)$ which, by a bit of algebra, is equal to A_2+10A_1+100N.

This system allows a minimum count in the programmable counter 3 of A_1+A_2. Since the system is decimal the maximum value of A_1 and A_2 is 9. The minimum value of N is therefore 18 and if the earlier system is replaced with this system it will work down to 18MHz. A similar, but more complex system involving ÷100/101/111 prescaler allows operation down to 10MHz.



LOGIC

INPUT		COUNT
101	110	
L	L	100
H	L	101
L	H	110
H	H	110

Fig. 59 Basic 100/101/110 prescaler

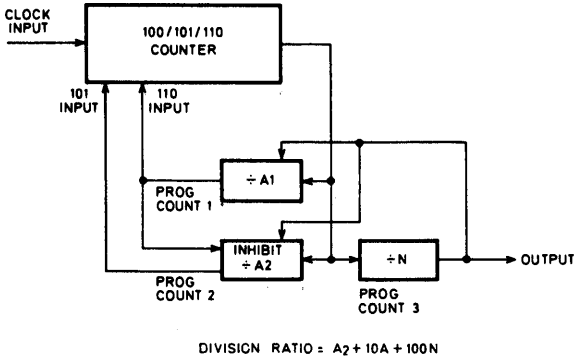


Fig. 60 Divider system with 100/101/110 prescaler

SYNTHESISER PRODUCT RANGE	
CRYSTAL OSCILLATORS	
SP705	1 to 10MHz crystal, outputs at ÷2, ÷4
CRYSTAL OSCILLATORS WITH DIVIDERS	
SP8760	also includes phase comparator
SP8921	also includes part of control circuit
CITIZENS BAND 27MHz PRODUCTS	
SP8921	
SP8922	
SP8923	
UNIVERSAL SYNTHESISER	
SP8901	4 modulus divider 1GHz
SP8906	4 modulus divider 500MHz
NJ8811	Control circuit for use with SP8901 or SP8906
LOWER POWER SYNTHESISER	
NJ8812	Control circuit for use with ÷40/41

SP705B

CRYSTAL OSCILLATOR

The SP705B is a square wave oscillator circuit designed to operate in conjunction with an AT cut quartz crystal of effective series resistance less than 300 ohms. Four TTL outputs are provided, related in frequency to the crystal frequency f as follows: f/2, f/4. $\overline{f/2}$ and $\overline{f/4}$. The SP705B is therefore ideally suited to either single or multi-phase TTL clock applications.

The crystal maintaining circuit consists of an emitter-coupled oscillator, with the emitter resistors replaced by constant-current generators. The crystal is connected, usually in series with 20pF capacitor, between pins 5 and 6. The 20pF capacitor can be replaced with a mechanical trimmer to allow small changes in frequency to be made, as shown in Fig. 62.

The circuit is designed to provide low crystal drive levels — typically, less than 0.15mW at 5MHz. This is well within crystal manufactures' limit of 0.5mW.

The compensation point, pin, 4 is made available so that the compensation capacitance can be increased if necessary. However the 14pF capacitor included on the chip is usually sufficient to prevent spurious oscillation at high frequencies.

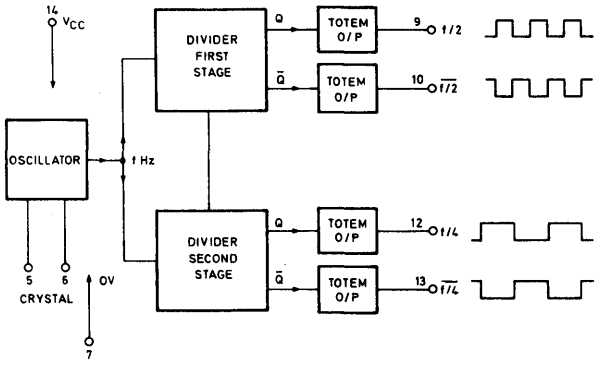


Fig. 61 SP705B block diagram

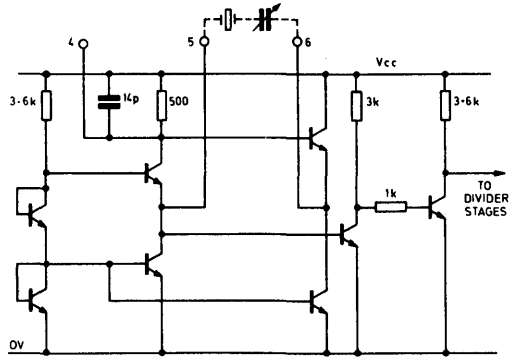


Fig. 62 Circuit diagram of SP705B oscillator

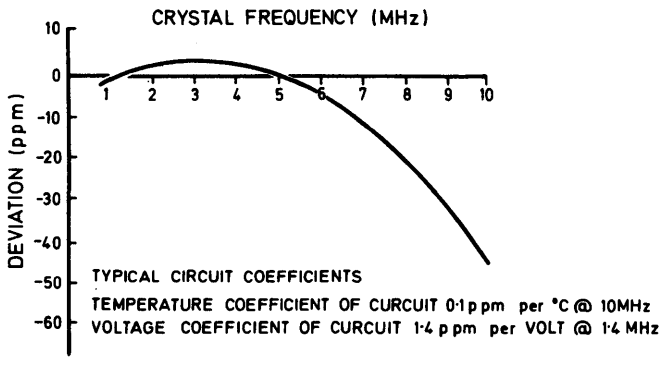


Fig. 63 Deviation from nominal crystal frequency

SP8760

General purpose synthesiser

The SP8760 is a general-purpose circuit intended for use in conjunction with CMOS or TTL programmable counters, and with high speed prescalers, in frequency synthesisers. It consists of a crystal oscillator with two-stage divider, a ÷15/16 two-modulus counter, and a high performance type II phase/frequency comparator. All three sections of the device have CMOS/TTL interfaces and the phase/frequency comparator offers better zero error and phase jitter characteristics than other such integrated circuits.

CIRCUIT DESCRIPTION (Fig.64)

The crystal oscillator uses an emitter-coupled circuit with a series resonant crystal connected between pins 4 and 5. It is internally rolled off to prevent overtone operation and will not work at frequencies much above 10MHz. This oscillator has a series resonant crystal and has a stability of about 0.2ppm/degree C, excluding the crystal itself.

If the divider is required but not the crystal oscillator, an external signal may be applied to pin 4 via a small capacitor in series with 220 ohms. Pin 5 may, in that case, either be decoupled or left open depending on the frequency and amplitude of the signal on pin 4.

The output of the oscillator is not available externally but only via a ÷4 circuit. This circuit, like the rest of the logic interfaces on the SP8760, has a CMOS/TTL compatible output, which is connected to pin 11.

The two-modulus divider (÷15/16) has a CMOS/TTL clock input on pin 6 and its output appears on pin 9. When the control input, pin 8, is high the divider divides by 16 and when it is low it divides by 15. The standard TTL fan-in of the clock input is 1 and the output fan-out is 3.

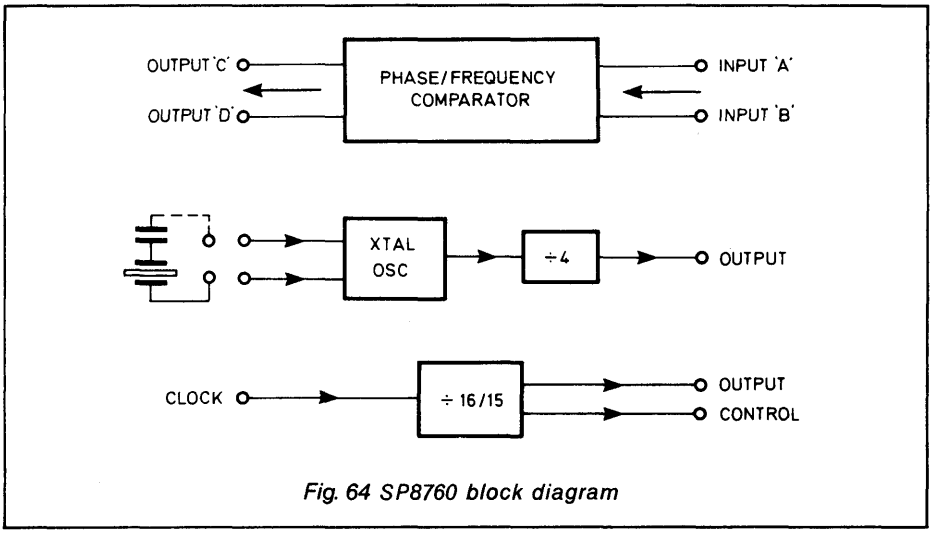


Fig. 64 SP8760 block diagram

The maximum clock frequency of the SP8760 is at least 12MHz (typically 18MHz). Hence the use of almost any family of low speed logic is permissible in the main divider of a synthesiser using the SP8760 since its output will never exceed 1MHz under proper operation.

The comparator has an infinite pull-in range (subject, of course, to an input frequency response of about 10MHz) and zero phase shift at phase-lock. The comparator pulse width at zero phase shift is under 30ns, giving minimum noise and jitter.

In operation the comparator triggers on the 1 to 0 transition of each input and gives outputs on pins 1 and 2 proportional to the phase difference between the two transitions. When the edge on pin 14 occurs before the edge on pin 13 the output on pin 1 will be low during the interval between the two transitions and the output on pin 2 will remain low whereas if the edge on pin 14 occurs after the edge on pin 13 the output on pin 2 will be high between the two transitions and pin 1 will remain high. The decision as to which is the 'first' transition is made by counting pulses at each input — if two pulses occur at one input without any ocurring at the other the second of the two is considered to be the 'first' and the relevant output changes state until a 1 to 0 transition occurs on the other input. Once an input has counted two in this way it remains the 'first' input until two transitions occur on the other input without one ocurring on it, when the other input becomes the 'first' input. The SP8760 phase comparator timing diagram is shown in Fig.65.

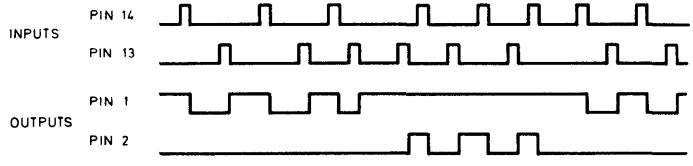


Fig. 65 Phase comparator timing diagram

The output on pin 1 consists of the collector of an NPN transistor with a 10 kilohm resistor to V_{ee}. Three ways of driving the varactor line of a voltage controlled oscillator from these outputs are shown in Fig. 66. The simplest way, shown in Fig. 66(a), is only suitable for use when the varactor voltage change is very small — say, less than 1V from 2 to 3V. The low voltage charge pump in Fig. 66(b) can be used with varactor voltages between 1V and 4V and the high voltage charge pump in Fig. 66(c) is used where large varactor voltage swings are necessary. The transistors and diodes used in these circuits should be silicon types with a fast switching speed to avoid degrading the performance of the phase comparator. The transistors used in the circuit in Fig. 66(c) need also a V_{ceo} of at least 35V.

The leakage on the varactor line must be as low as possible since any leakage leads to jitter as the charge pump replaces the lost charge. A high impedance buffer may be placed between the output of the charge pump and the varactor line and indeed is essential if varactor line losses are high.

Since noise in this buffer will itself cause oscillator jitter, it is better to use a non-leaky varactor line and no buffer if at all possible.

The SP8760 uses a single 5V supply, which must be well decoupled at HF and LF and draw about 45mA.

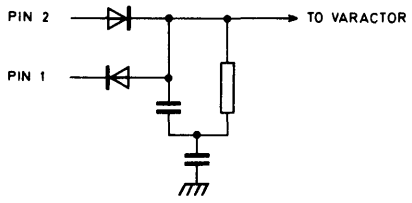


Fig. 66a Simple charge pump

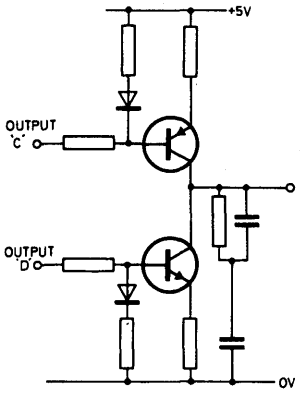


Fig. 66b Low voltage charge pump and filter. Divider clock input

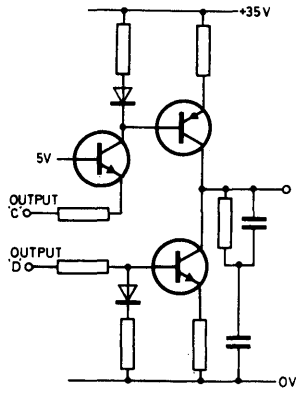


Fig. 66c High voltage charge pump and filter

SP8921/2

CITIZENS' BAND SYNTHESISER

The SP8921/22 combination is intended to synthesise the frequencies required in a 40-Channel Citizens' Band transceiver. The 40 channels are spaced at 10kHz intervals (with some gaps) between 26.965 and 27.405MHz. Local oscillator frequencies for the reception of these channels with intermediate frequencies of 455kHz, 10.240MHz, 10.695MHz and 10.700MHz are also synthesised. Table 4 shows the relationship between the program input and the channel selected. By using a program other than one of the 40 given other frequencies may be selected – in fact there are 64 channels at 10kHz separation available from 26.895 to 27.525MHz and programming starts at all zeros on inputs A through F for 26.895 and each increase of one bit to the binary number on these inputs increases the channel frequency by 10kHz until all '1's give 27.525MHz. The A input is the least significant bit, F the most significant. The programming input on pin 16 of the SP8922 is normally kept high but making it low increases the programmed frequency by 5kHz. Table 5 shows the programming required to obtain various offsets.

The circuit diagram of a CB synthesiser is shown in Fig. 67. It is intended for use in double conversion receivers with IFs of 10.695 and 455kHz and generates either the frequency programmed or the frequency programmed less 10.695MHz.

If other offsets are programmed the connections to pin 15 of the SP8921 and pin 2 of the SP8922 must be altered according to Table 5.

The synthesiser consists of the SP8921 and the SP8922 plus an SP1648 voltage controlled oscillator.

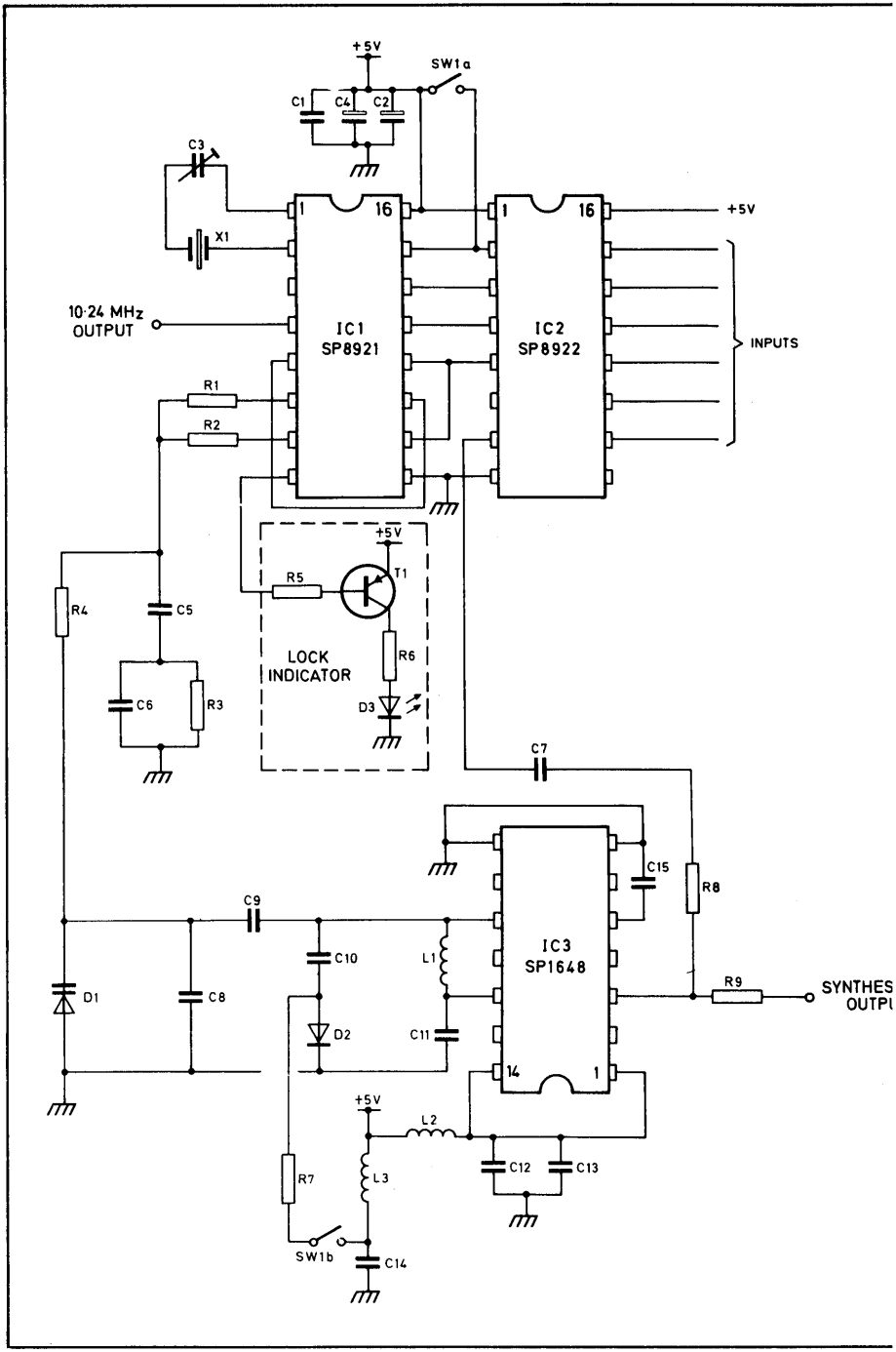
The programming inputs to the SP8922 are as shown in Table 4. Logic '1' is +3V or more, logic '0' is either ground or an open circuit. The circuit diagram of a programming input port is shown in Fig. 68. If a switch, constructed so as to select the correct combination for each channel, can be obtained this is the obvious way to program the synthesiser; otherwise a ROM may be suitably programmed and placed between the switch and the SP8922.

The crystal oscillator in the SP8921 is trimmed by a small variable capacitor, C3, which must be set up during alignment of the synthesiser so that the output frequency on pin 4 is 10.240000MHz. The only other adjustment is to set the core of L1 so that the varicap control voltage is 2.85V when the synthesiser is set to channel 30 transmit. Since the difference between transmit and receive frequencies is over 10MHz it is not possible to tune both with the same tuned circuit and an extra capacitor is switched by means of a diode during reception.

The phase/frequency comparator of the SP8921 can have an output swing from 0.5V to 3.8V but it is better to work in the range 1.5V to 3.0V as the phase-error output voltage is more linear in this region. The ZC822 tuning diode specified for this synthesiser may be replaced by any other tuning diode provided it will tune the VC0 over the required range, or a little more, as the control voltage goes from 1.5 to 3.0V. With slight coil changes the MV2105 has been used successfully in this synthesiser.

Channel No.	Input Code F E D C B A	Output frequency with R/T = 0 (MHz)
1	0 0 0 1 1 1	26.965
2	0 0 1 0 0 0	26.975
3	0 0 1 0 0 1	26.985
4	0 0 1 0 1 1	27.005
5	0 0 1 1 0 0	27.015
6	0 0 1 1 0 1	27.025
7	0 0 1 1 1 0	27.035
8	0 1 0 0 0 0	27.055
9	0 1 0 0 0 1	27.065
10	0 1 0 0 1 0	27.075
11	0 1 0 0 1 1	27.085
12	0 1 0 1 0 1	27.105
13	0 1 0 1 1 0	27.115
14	0 1 0 1 1 1	27.125
15	0 1 1 0 0 0	27.135
16	0 1 1 0 1 0	27.155
17	0 1 1 0 1 1	27.165
18	0 1 1 1 0 0	27.175
19	0 1 1 1 0 1	27.185
20	0 1 1 1 1 1	27.205
21	1 0 0 0 0 0	27.215
22	1 0 0 0 0 1	27.225
23	1 0 0 1 0 0	27.255
24	1 0 0 0 1 0	27.235
25	1 0 0 0 1 1	27.245
26	1 0 0 1 0 1	27.265
27	1 0 0 1 1 0	27.275
28	1 0 0 1 1 1	27.285
29	1 0 1 0 0 0	27.295
30	1 0 1 0 0 1	27.305
31	1 0 1 0 1 0	27.315
32	1 0 1 0 1 1	27.325
33	1 0 1 1 0 0	27.335
34	1 0 1 1 0 1	27.345
35	1 0 1 1 1 0	27.355
36	1 0 1 1 1 1	27.365
37	1 1 0 0 0 0	27.375
38	1 1 0 0 0 1	27.385
39	1 1 0 0 1 0	27.395
40	1 1 0 0 1 1	27.405

Table 4 SP8922/1 O/P frequencies with 10.240 crystal (0 = contact open, 1 = contact closed to V_{CC})


+5V
SW1a
C1
C4
C2
C3
X1
1
16
IC1
SP8921
IC2
SP8922
+5V
INPUTS
10·24 MHz
OUTPUT
R1
R2
R4
C5
C6
R3
+5V
R5
T1
LOCK
INDICATOR
R6
D3
C7
C15
R8
C9
C10
L1
IC3
SP1648
R9
SYNTHES
OUTPI
D1
C8
D2
C11
14
1
+5V
L2
C12
C13
R7
L3
SW1b
C14

esistors are in ohms and $\frac{1}{8}$W $\pm$ 10% unless otherwise stated. Capacitor values are icrofarads unless otherwise stated.

IC1	SP8921
IC2	SP8922/SP8923
IC3	SP1648
T1	2N 3906
D1	ZC822, Ferranti varactor diode
D2	1N4148 Silicon diode
D3	LED lock indicator
X1	10.240MHz crystal, series mode
L1	11 turns 30 gauge cotton covered wire on Neosid A7 assembly
L2	100 microhenries RF choke
L3	100 microhenries RF choke
R1	1.0k $\pm$ 5%
R2	1.0k $\pm$ 5%
R3	8.2k $\pm$ 5%
R4	33k
R5	10k
R6	150 (adjust for LED brightness)
R7	1k
R8	1k
R9	470 (adjust for required output level)
C1	0.1
C2	100, 10V solid tantalum
C3	2 – 22pF variable
C4	100 10V solid tantalum
C5	110V solid tantalum
C6	0.1
C7	1000pF
C8	22pF + 10%
C9	0.01
C10	100pF $\pm$ 10%
C11	0.01
C12	0.1
C13	10 solid tantalum
C14	0.1
C15	1000pF
SW1	2 pole, 1 way switch, (receive/transmit)

Offset	SP8921	SP8922
0	0	0
–455kHz	0	1
–10.240MHz	1	0
–10.695MHz	1	1

Table 5

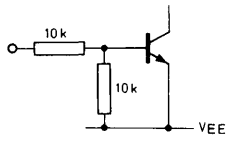


Fig. 68 Program input circuit

The low pass filter of the PLL consists of C5, C6 and R3. If faster lock (at the expense of larger noise and reference sidebands) is required the filter may be redesigned. If the synthesiser is used in a scanning receiver, a switched filter should be used to give fast lock during scanning but a slower lock and cleaner signal during normal operation. The lock output on pin 8 of the SP8921 is used to light an indicator when the loop is *not* locked and should also be used, in a transmitter or transceiver, to prevent transmission when the loop is unlocked.

Fig. 69 shows the circuit board layout and component placing of this synthesiser. It requires a single +5V supply and draws about 60mA. The performance is improved if double-sided board is used with a ground plane on one side. A small further improvement would come from the use of a grounded screening can over the whole system.

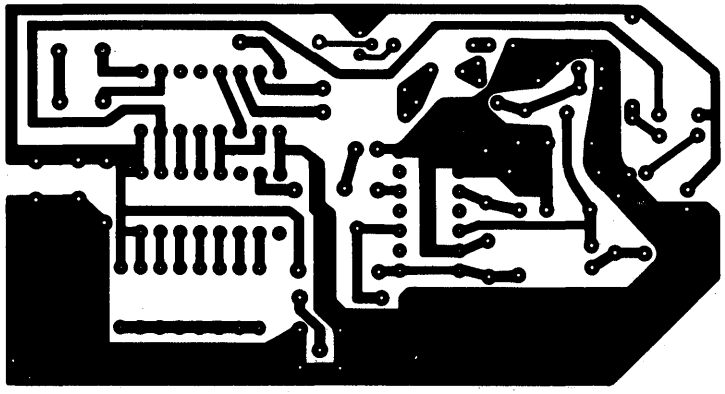


Fig. 69a Printed circuit layout for CB synthesiser

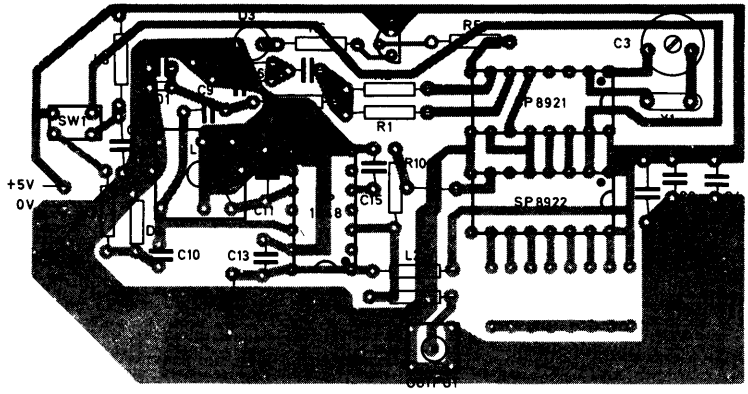


Fig. 69b PCB component layout for CB synthesiser

The synthesiser has reference frequency sidebands 50dB down at 1.25kHz from the carrier. All output over 5kHz from the carrier is over 70dB down. Lock time for a change from channel 0 to channel 40 (a frequency change of 440kHz) is around 35ms. Photographs of the output spectrum and the change of control voltage with time during a step from channel 0 to channel 40 are shown in Fig. 70. Stepping from transmit to receive or vice versa takes somewhat longer because of the much larger change of frequency but is generally complete within 75ms.

This synthesiser is quite basic but has adequate performance for the majority of CB applications. If improved performance is required there are two possibilities; an improved FET oscillator having lower floor noise instead of the SP1648 or an improved low pass filter to reduce reference frequency sidebands.

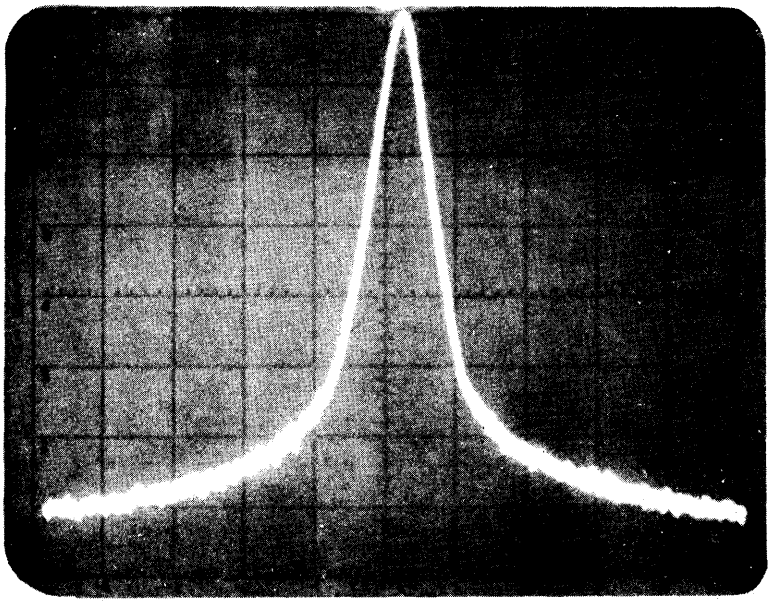


Fig. 85a Typical output spectrum of basic synthesiser (Vert.:16dB/div.,Horiz.:2kHz/div.,) BW:300Hz, fo:27.065MHz

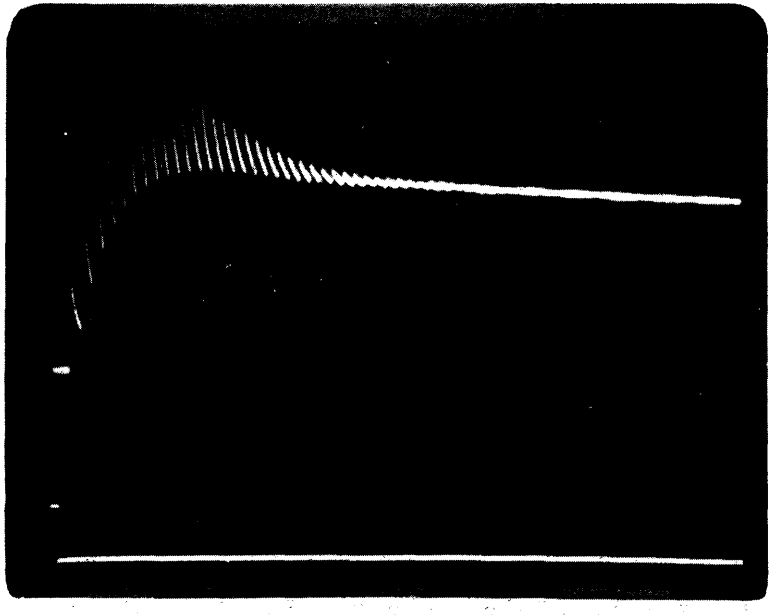


Fig. 85b Typical transient response of basic synthesiser. Response of varactor line to step program change 1–40. Vert.:200mV/div.,Horiz.:5ms/div.
N.B. Droop of response is due to the measuring instrument being AC-coupled.

RADAR APPLICATION NOTES

Introduction

The performance of a radar receiver depends very much on the performance of its IF strip. It must provide enough gain and dynamic range to allow for the expected variations in echo signal power, and without saturation. It must have a low noise figure, especially as this affects the overall noise performance of crystal mixer/amplifier combinations. The bandpass characteristic is also important: the overall receiver bandwidth is essentially determined by that of the IF stages. In addition, the IF amplifier must have a high centre frequency compared with the signal bandwidth if IF signal spectral components are not to appear within the passband of the video amplifier.

Plessey Semiconductors contribution to the design of radar IF amplifiers is a range of integrated circuits which may be regarded as building blocks from which IF systems of different requirements and configurations can be built. These circuits are summarised in Section 2, followed by detailed application information given in the remaining sections of this handbook.

Table 1 summarises the range of integrated circuits for radar applications available from Plessey Semiconductors. Full technical data for each of these circuits is given in Section 6.

1 Plessey ICs for radar IFs

Successive detection log. amplifier	
SL521	30 to 60MHz centre frequency, 12dB gain
SL523	Dual SL521 (cascade)
SL1521	120 to 160 MHz centre frequency, 12dB gain
SL1522	Dual SL1521 (parallel)
SL1523	Dual SL1521 (cascade)
Linear amplifiers	
SL550	125MHz bandwidth ,40dB gain, 25dB gain control range, 1.8dB noise figure
SL560	300MHz bandwidth, 10 to 40dB gain, 1.8dB noise figure
Video amplifiers and detectors	
SL510	Detector (DC to 100MHz), video amp. (DC to 24MHz)
SL541	Op. amp. configuration, slew rate 175V/μs, settling time 50ns, recovery from overload 50ns.
A to D conversion	
SP750B	High speed latched comparator, min. set-up time 2ns, propagation delay 3.5ns (typ.)

Table 1 Plessey ICs for radar IF systems

SUCCESSIVE DETECTION LOGARTHMIC IF STRIPS

The well established SL521 integrated circuit has been widely used in logarithmic IF strips for many years. New products have been introduced in recent years to satisfy the needs of higher IF frequencies and reduced weight/ volume. The first of these, the wide bandwidth SL1521, is described in detail (together with the design for a log. strip) in Section 4.

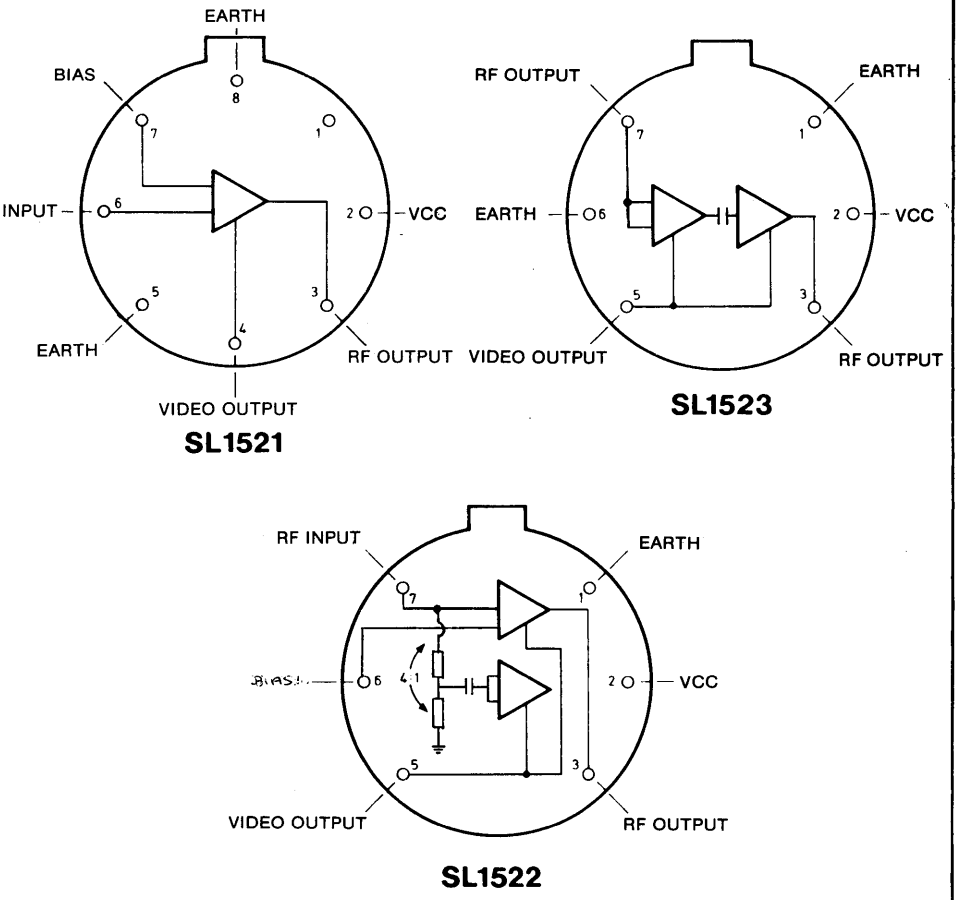


Fig. 1 Log IF amplifiers SL1521/2/3

More recently, products have been introduced which combine two SL521 or SL1521 chips in a single encapsulation. The SL523 and SL1523 contain two stages in cascade; the SL523 is pin compatible with the SL521 (see data sheet page 41). The use of the SL1523 or SL523 enables the user to obtain a major size reduction in the IF strip; for example a high performance 60MHz strip with a 90dB log. range can be built using only four SL523 packages (see Fig. 2).

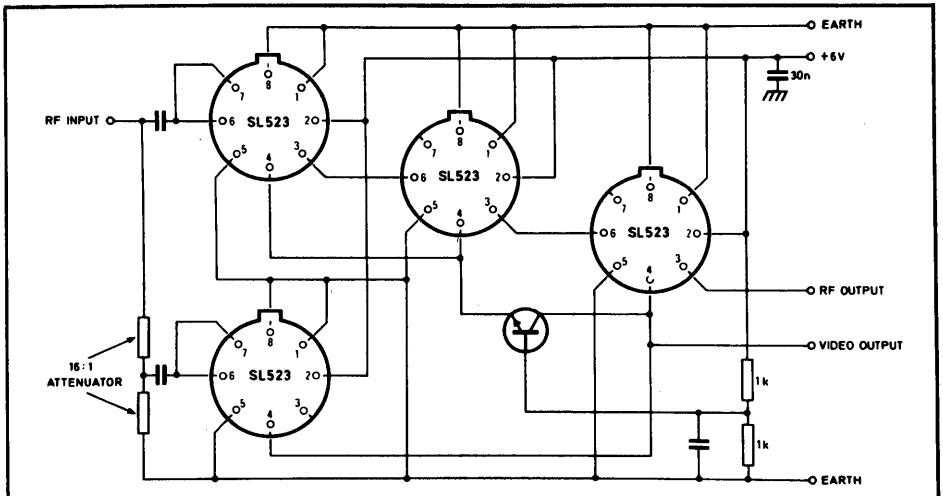


Fig. 2 Wide dynamic range IF strip

The SL1522 also contains two SL1521s, but this time they are essentially connected in parallel. It is intended that the SL1522 should be used in the first stage of a log strip; when included in this way the strip maintains its log characteristic for input signals 12dB larger than the simple strip. This is a simple example of the 'lift' technique described for the SL1521 strip below. The SL1522 can be substituted in most cases for the first SL521 or SL1521 in an existing strip with only minor changes to the board being necessary.

LINEAR AMPLIFIERS

The two most important linear radar IF amplifiers are the SL550 and SL560. The SL550 is ideal for use where variable gain is required up to 100MHz. Strips incorporating STC (sensitivity time control) or swept gain are easily built with this device. Section 3 describes the practical details of a simple strip of this type.

The versatility and high performance of the SL560 makes it ideal for fixed gain pre-amplifiers. Section 3 describes the design of a wide dynamic range, low-noise, preamplifier suitable for interfacing between a microwave mixer and an SL521 or SL1521 log strip.

VIDEO AMPLIFIERS AND DETECTORS

Two circuits are available for use in the video sections of a radar. The SL510 is a general purpose detector and video amplifier and is described in more detail in Section 5. The SL541 is a high speed video amplifier, the configuration of which follows that of an operational amplifier. Apart from the high slew rate (175 volts per microsecond) the important features of the SL541 are its fast settling time and its ability to deliver a clean video pulse with a minimum of overshoot and ringing even when severely overdriven. Positive and negative output swings are limited to $\pm$ 3 volts without saturating any transistor in the circuit so that the circuit can recover from a 10 times overload in less than 50ns.

A TO D CONVERSION

Two conversion methods dominate the field of fast analogue-to-digital conversion: the all-parallel and the parallel-series-parallel converter.

The all-parallel conversion technique provides the highest rate of conversion available. For an N-bit converter, (2^N-1) comparators compare the input with a linearly divided reference voltage. The decisions of the comparators are held by the application of a latch signal until the comparators are unlatched to receive new data. The conversion rate is therefore determined by the response time of the comparators. Fig. 3 shows the block diagram of such a converter. Using the SP750B a conversion rate of 100 Megasamples per second or more can be obtained.

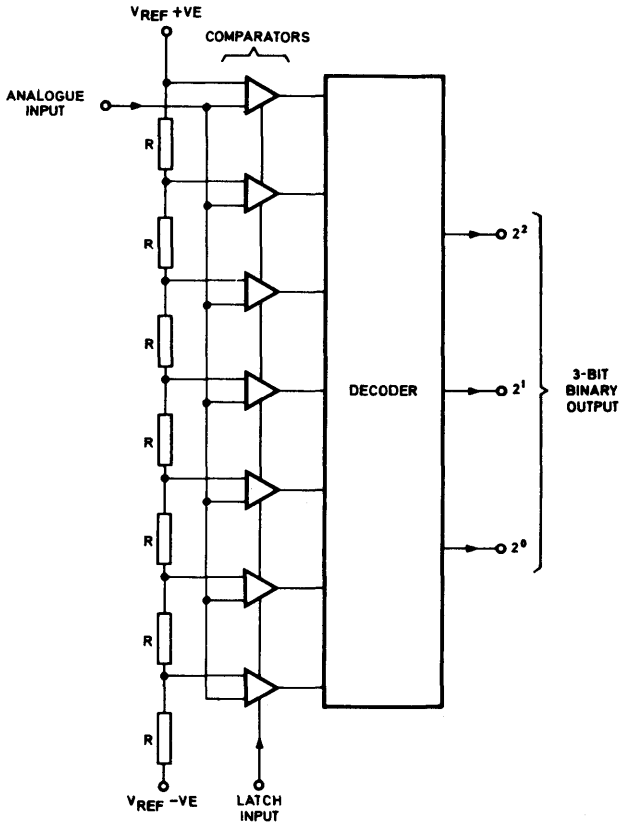


Fig. 3 3-bit all parallel A-D converter

The all-parallel converter becomes rather expensive in comparators if more than 5 or 6 bit accuracy is required, where the parallel-series-parallel technique illustrated in Fig. 4 may be preferred. Sampling rates of up to 30 Megasamples per second can be achieved with 8-bit accuracy using the SP750B.

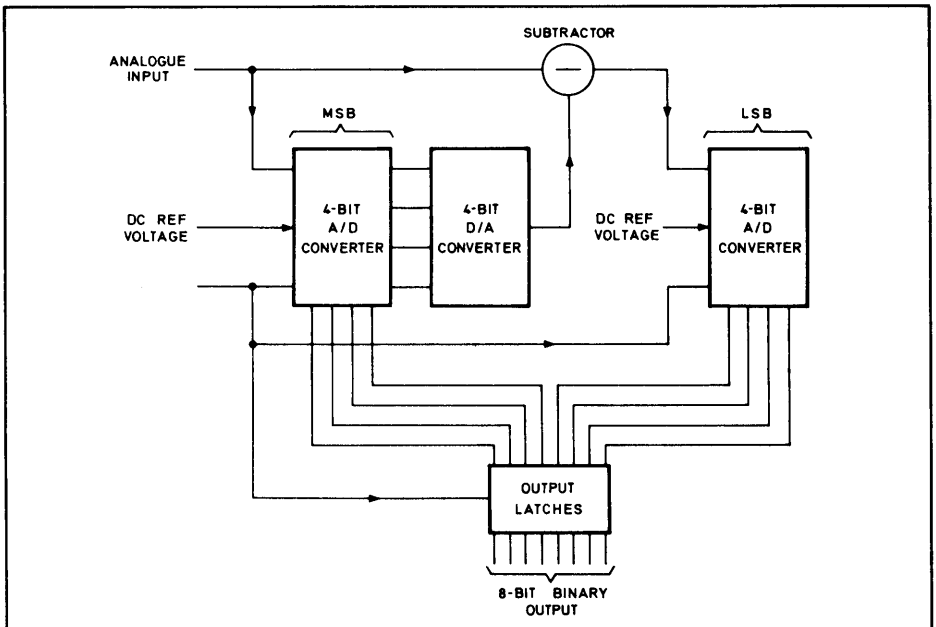


Fig. 4 4 × 4-bit parallel-series-parallel

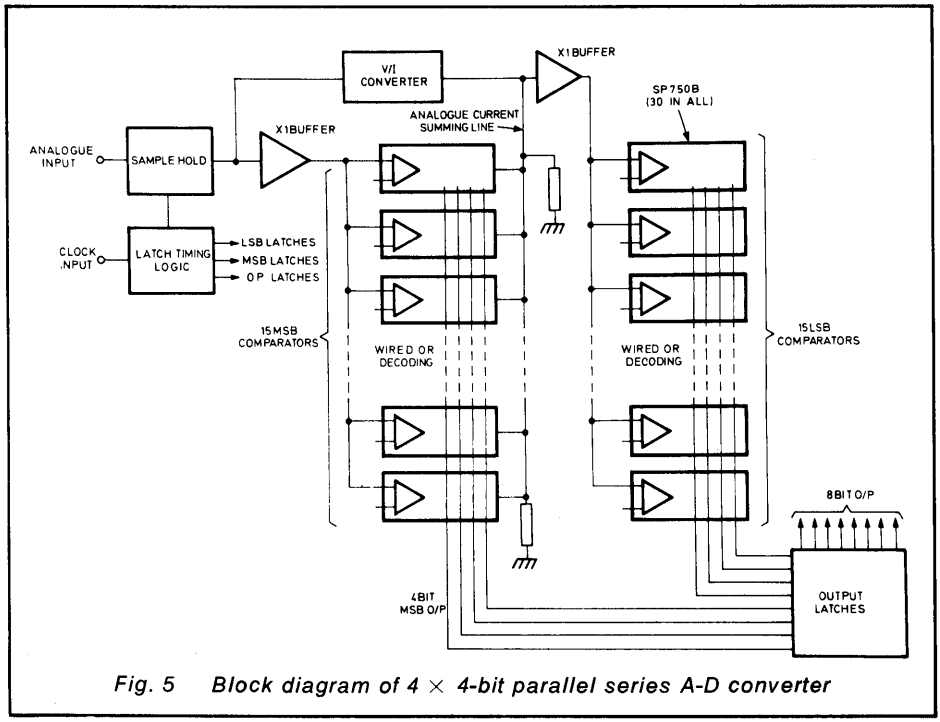


Fig. 5 Block diagram of 4 × 4-bit parallel series A-D converter

The SP750 has several features which make it more suitable for use in A-D converters of these types than other fast comparators. The basis of the SP750 is a fast comparator with a latch facility, which allows the device to be used in the sample-and-hold mode. The comparator has a relatively low gain in the follow (i.e. unlatched) mode, which assists in achieving an extremely fast response. However, due to the positive feedback action of the latch facility, the gain approaches infinity during the latch cycle, thereby permitting high resolution to be achieved.

In addition to the basic comparator, functions are included which are purpose designed to aid in optimising the design of parallel and parallel-series-parallel converters.

They are:

1. A two-input gate for simplified comparator output logic.
2. Four emitter follower outputs from the gate to provide wired OR decoding for up to 4 bits.
3. A precision current source set by an external resistor and a reference voltage.
4. A high speed switch for the current source to provide a fast and convenient reconstruction of the analogue input.

Fig. 6 shows a block diagram of the SP750 illustrating these functions.

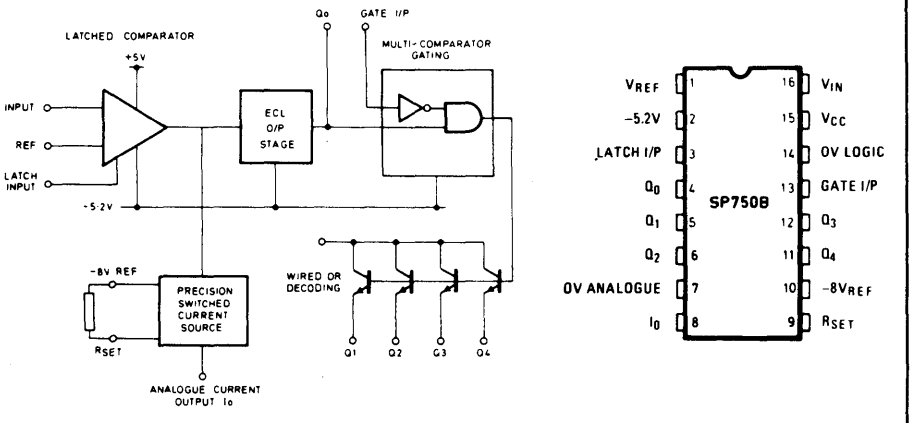


Fig. 6 SP750B block diagram

2 A wide dynamic range preamplifier

SL560 GENERAL DESCRIPTION

The SL560, containing three very high performance transistors and associated biasing components, forms a 300MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components.

A common base configuration is obtained when pin 6 is decoupled (see Fig. 7). In this form a well-defined low input impedance is obtained, which could be utilised either for a low noise/low source operation (pin 7 input) or for 50ohms input impedance (pin 8 input).

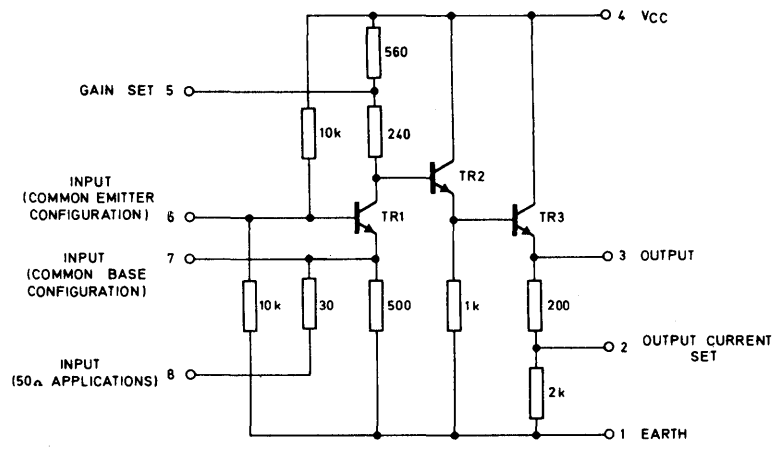


Fig. 7 SL560 circuit diagram

Operating the circuit with the input transistor in the common emitter configuration can be achieved by decoupling pin 7 and using pin 6 as the input. A gain of 35dB with a bandwidth of 75MHz and with a noise figure of 2dB can be achieved with this configuration.

To obtain maximum bandwidth from the circuit, the capacitance at the collector of the input transistor must be kept to minimum. To give some flexibility in the choice of collector loading and meet the above requirement, a split collector load has been introduced. This minimises the influence of can and bonding pad capacitances on the frequency response of the amplifier. If shaping of the amplifiers roll-off is required, then external capacitance can be connected to pin 5.

The output is taken from the emitter follower stage, pin 3; this gives a low output impedance and maximum voltage swing. If higher current swing is required, then pin 2 is earthed. Depending on the configuration, the amplifier can be operated from a supply of 2V to 15V. Additional flexibility in the selection of biasing condition of the first transistor is available by paralleling external resistors with the internal 10k bias resistors. With all the options available, care must be taken to ensure that the temperature rating of the circuit is not exceeded. The chip-to-ambient thermal resistance is 225°C/Watt, chip-to-case is 65°C/Watt, and the permitted maximum junction temperature is 150°C.

To obtain best noise performance, the SL560 would normally be operated in common emitter mode, with pin 6 as input and pin 7 decoupled; it is also important to operate the input transistor at the correct quiescent current. For a typical device, the optimum first stage current is given by $I_{opt} = 200/R_S$, where R_S is the source impedance in ohms and I_{opt} is in mA. The desired

current can be achieved by a suitable choice of supply voltage or by changing the bias voltage of pin 6 by external resistors to earth or to the positive supply.

The noise figure of the SL560 is given by the standard equations for bipolar transistors. If operated under optimum conditions a useful formula is that the noise figure will be approximately 10 log (1.3 + 20/Rs). For more detailed calculations, typical data on the transistor is given in Table 2.

Parameter	Value
h_{fe}	40 to 120
r_{bb}	17 Ω
f_T (@ 2mA)	1.0GHz
f_T (@ 10mA)	2.0GHz

Table 2 SL560 Typical transistor data

As the SL560 employs transistors with high f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size and good electrical quality must be used; the leads must be as short as possible to avoid oscillation induced by stray inductances. The use of a ground plane is recommended when using printed circuit boards.

PREAMPLIFIER CIRCUIT DESCRIPTION

The SL560 is a general purpose, low noise, high performance amplifier and as such it has numerous applications, some of which are listed in the Data Sheet (see Section 6).

An example of its uses and ease of application is best appreciated by construction of the wide dynamic range pre-amplifier shown in Fig. 8. The circuit is designed to the performance specification given in Table 3.

Characteristic	Performance
Gain	35dB
Bandwidth	> 150MHz
Noise figure (Rs = 200 Ω)	< 2.0dB
Dynamic range (BW = 1MHz)	> 80dB
Current consumption	< 50mA
Output voltage	> 1.0V rms into 100 Ω (resistive)

Table 3 Performance specification of SL560 preamp. (Fig. 8)

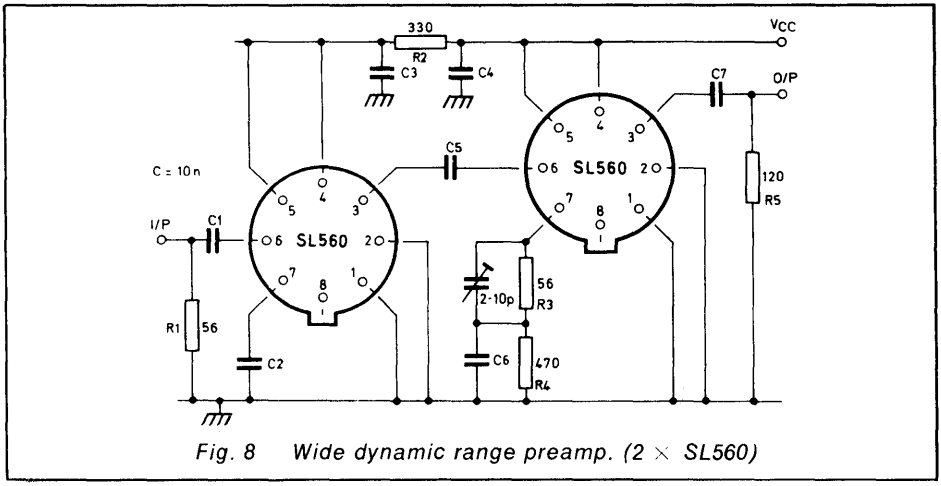


Fig. 8 Wide dynamic range preamp. (2 × SL560)

The circuit consists of 2 stages of SL560, both in common emitter configuration, with the first stage giving 20dB gain and the second 15dB. The input transistor of the first device is operated at 1.5mA, which gives a low noise figure for a source impedance around 200 ohms. The input transistor of the second SL560 has a feedback resistor in its emitter, which reduces the stage gain and degrades slightly the noise figure, but increases the bandwidth and signal handling ability.

At high frequencies, the layout of the PCB has a considerable effect on the overall frequency response of the amplifier. This is mainly due to the high f_T chip transistors and also to stray capacitance. The PCB to use, in this case, is one with the minimum of copper track removed from the reverse side and a continuous ground plane on the components side. The response is also affected by supply line decoupling and for smooth frequency-apmlitude response each stage of amplification is individually decoupled by high grade ceramic capacitors. The layout of a suitable PCB for this amplifier is shown in Fig. 9.

The influence of variations due to the PCB and the devices can be compensated by incorporating a trimmer capacitor across the second stage feedback resistor. This allows variation of emitter peaking and helps to achieve an amplitude-frequency response within ± 0.5dB up to 200MHz. Fig. 10 shows frequency response obtained with this amplifier, and Fig. 11 the power output v. frequency.

When satisfactory frequency response is obtained other characteristics of the amplifier can be measured. Typical figures obtained are given in Table 4.

Characteristic	Typical Performance
Output power for 1dB compression	10mW
Noise Figure	1.8dB
Output voltage (supply 6V)	1.1V rms
Current consumption	35mA

Table 4 Typical performance figures for Fig. 8

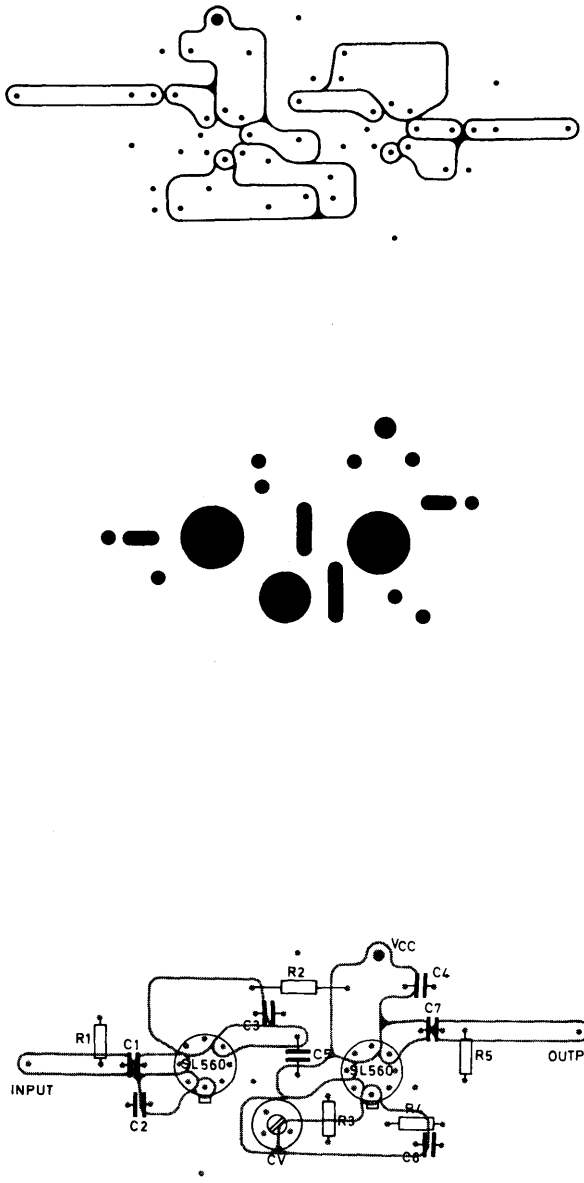


Fig. 9 Printed circuit board for 2 stage SL560 preamplifier

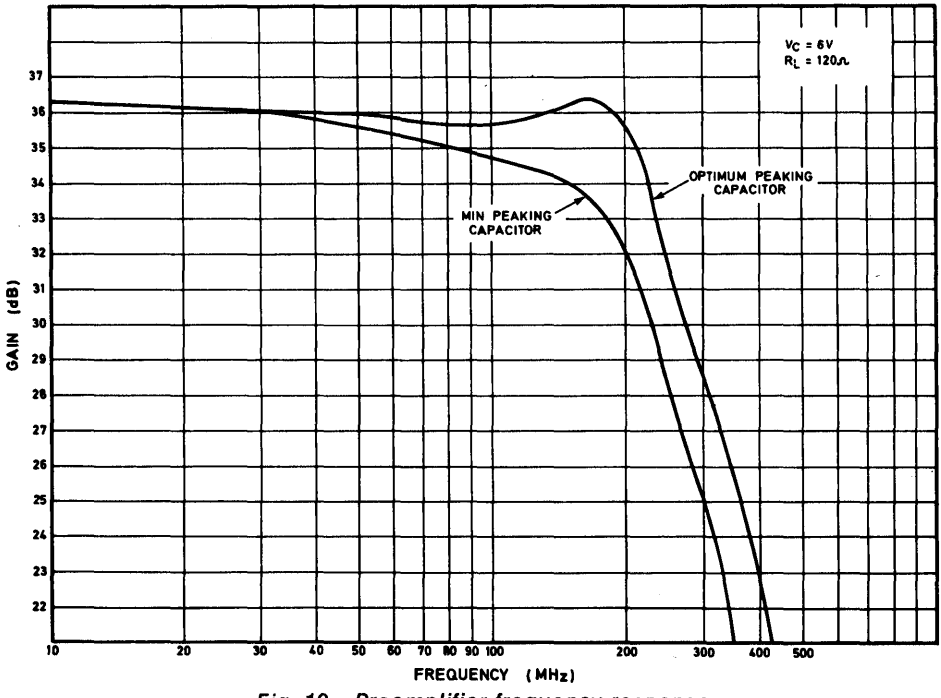


Fig. 10 Preamplifier frequency response

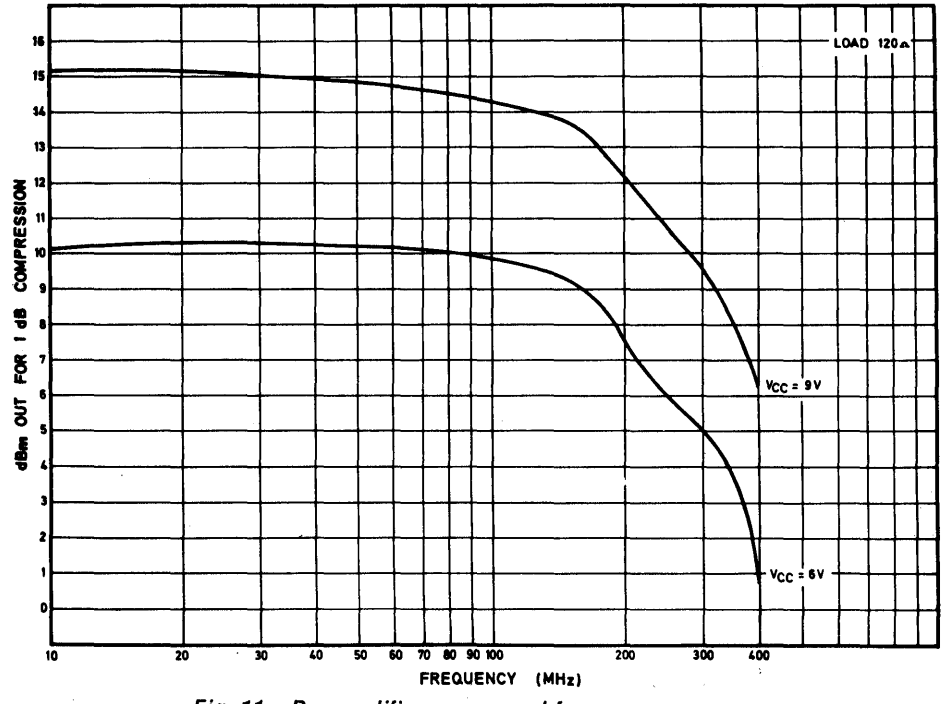


Fig. 11 Preamplifier power and frequency response

3 A 120MHz log strip using SL1521s

SL1521 GENERAL DESCRIPTION

The SL1521 is a wideband IC amplifier intended for use in successive detection logarithmic IF strips operating at centre frequencies up to 200MHz.

Many radar systems use logarithmic IF amplifiers as a simple means of compressing the dynamic range of the received signal from 90dB at the input to a more manageable range for the processing circuit. This system was chosen because in it the maximum output signal is provided by all stages working in parallel.

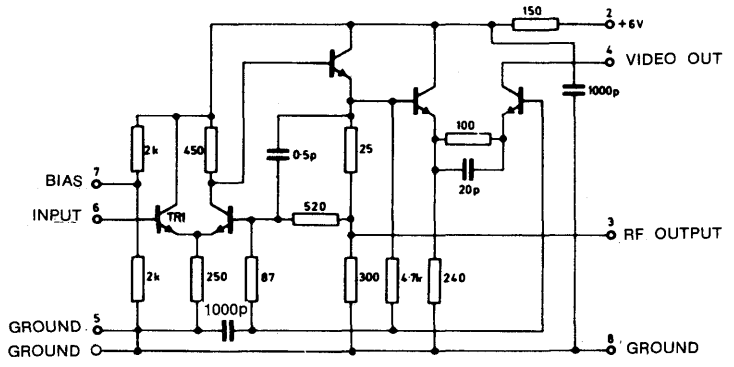


Fig. 12 SL1521 circuit diagram

A single stage of SL1521 is capable of 1mA (typ.) output when driven into saturation with 0.5V rms signal as shown in Fig. 14. The device has a defined gain and frequency response, it provides a limiting characteristic, rectified and non-rectified outputs and has a sensibly low noise figure (3dB typ.). It is also capable of handling an overload input signal of 1.5V rms without being paralysed.

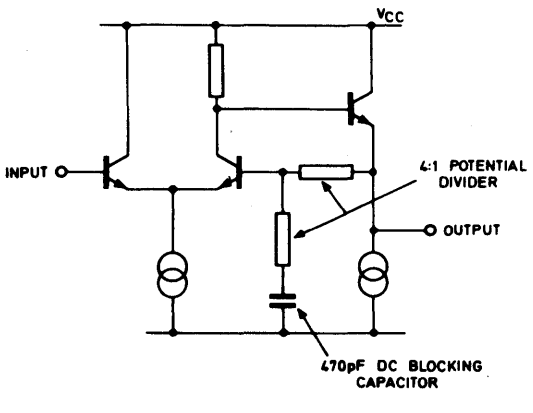


Fig. 13 Simplified circuit diagram of SL1521

The circuit, Fig. 12, consists of an emitter coupled pair amplifier-limiter with an emitter follower completing the amplifier section. The gain and frequency response are controlled by series voltage feedback; a second emitter coupled pair provides a low level detector with a current output.

Fig. 13 shows a simplified equivalent circuit of the SL1521. The potential divider defines the gain of 4 and an amplitude-frequency response of 350MHz (typ.) The 470pF blocking capacitor defines the low frequency cut-off (6MHz typ.). Careful design of both the long tailed pairs, the bias and the feedback circuitry ensures that the amplifier limits symmetrically.

The supply line is internally decoupled by a single RC network consisting of a 78 ohm resistor and 1000pF capacitor; this minimises problems of supply line decoupling when devices are cascaded.

The long tailed pair input and emitter follower output forms an amplifier with high input and low output impedances. This arrangement gives a flat frequency response when the devices are cascaded because it stimulates the condition of a voltage (low impedance) source feeding a high impedance load.

Fig. 14 Video output of SL1521 series

Some problems may occur if very fast edge IF pulses are applied to an SL521 or SL1521 strip. Fast leading edges, in general, do not cause problems but a trailing edge faster than about 30ns may give rise to a small spike on top of the video pulse just before it falls (see Fig. 15). The maximum amplitude of this spike should not exceed 5% of the pulse height under worst case

conditions. In the event of this spike being troublesome it can be eliminated by one or more of the following methods:-

1. Slowing down the trailing edge of the IF pulse.
2. Raising the low cut-off frequency of the strip by AC coupling or including a filter.
3. Video filtering

If an IF filter is used to eliminate this spike, not more than three stages should be cascaded before or after the filter.

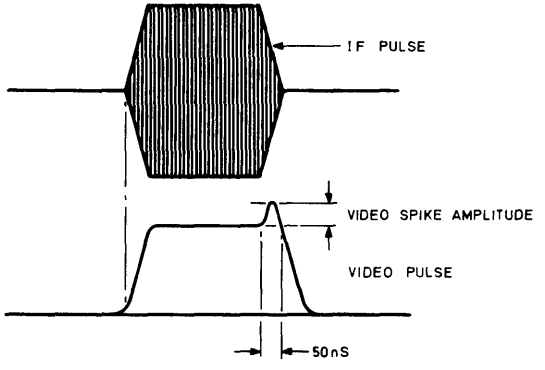


Fig. 15 Response of log amp. to a very fast pulse input

LOG IF STRIP DESCRIPTION

The circuit diagram design of an IF strip using the SL1521 is shown in Fig. 16. This amplifier consists of six stages of cascaded SL1521 integrated circuits and two additional units are employed as 'lift' stages to extend the dynamic range to over 80dB.

The IF signal is amplified by each stage in turn until a point is reached where the input to the last stage is sufficient to drive it into saturation. It then contribute no more to the video summation line. With increasing input the preceeding stage saturates and so on until all stages are saturated and there is no further increase in video output. It is this multiplying and subsequent summation that constitutes the logarithmic action. The first amplifier in the cascade gives its full output current at an input signal of about 100mV rms. The input signal could be increased to 1.8V rms without overload. This feature can be used to extend the dynamic range. If the input, as well as being applied to the first device of the main amplifier, is attenuated and fed to one or more additional ICs in such a manner as to ensure that they do not add to the output until the main amplifier is about to go into saturation, then we have a means by which the dynamic range can be extended. The limiting criterion is the maximum input signal before overload which would paralyse the main amplifier.

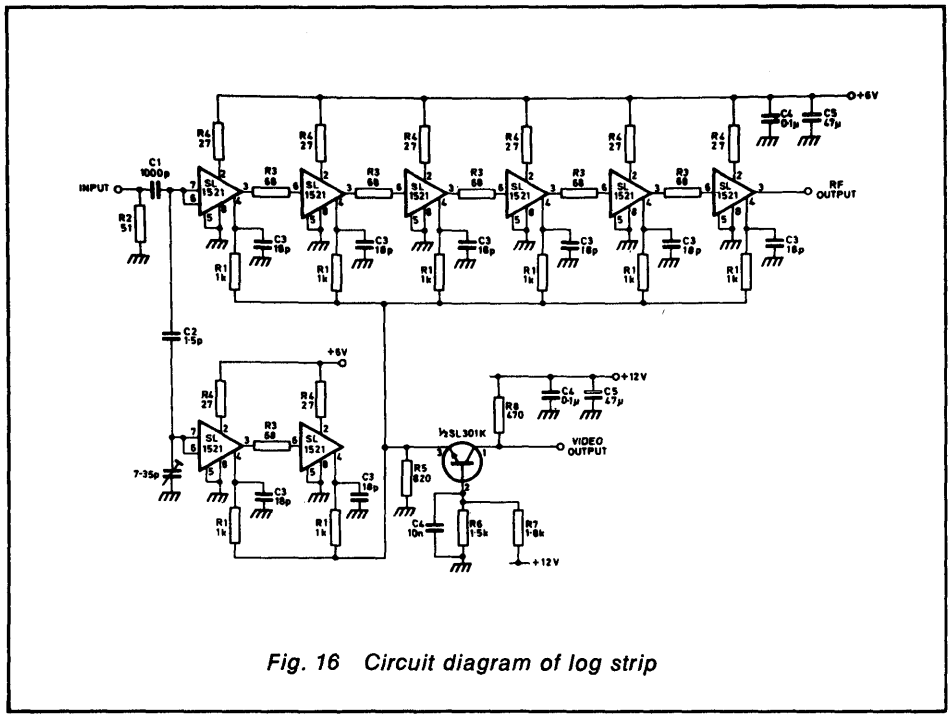


Fig. 16 Circuit diagram of log strip

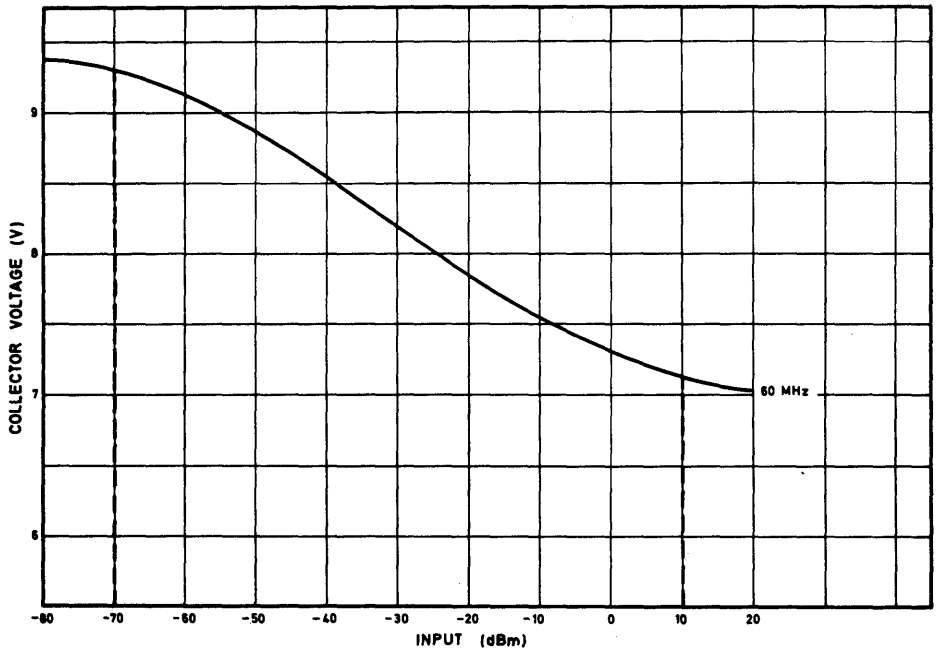


Fig. 17 Dynamic range of log strip

Included in series with each video output is a 1k ohm resistor to prevent instability caused by feedback along the summation line. A grounded base transistor stage is also used to buffer the summation line and it can be followed with a simple low pass LC filter in order to reduce IF breakthrough to a subsequent video amplifier.

The strip described above includes 'stopper' resistors in the supply line which reduce unwanted feedback along the supply line and improve stability. Interstage resistors are also included which improve the overall frequency response of the amplifier. The measurements made on the above amplifier indicate an IF bandwidth of 10 to 120MHz, with less than 3dB ripple in the passband (see Fig. 18). The dynamic range is in excess of 80dB and the log linearity $\pm$0.75dB (see Fig. 17). The amplifier uses SL1521B devices; with A grade devices a slight improvement in bandwidth (7.5MHz to 130MHz), dynamic range (85dB) and log law ($\pm$0.5dB) can be expected.

Layout of the SL1521 strip is not critical as long as short earth leads are used – a suitable printed circuit board is shown in Fig. 19.

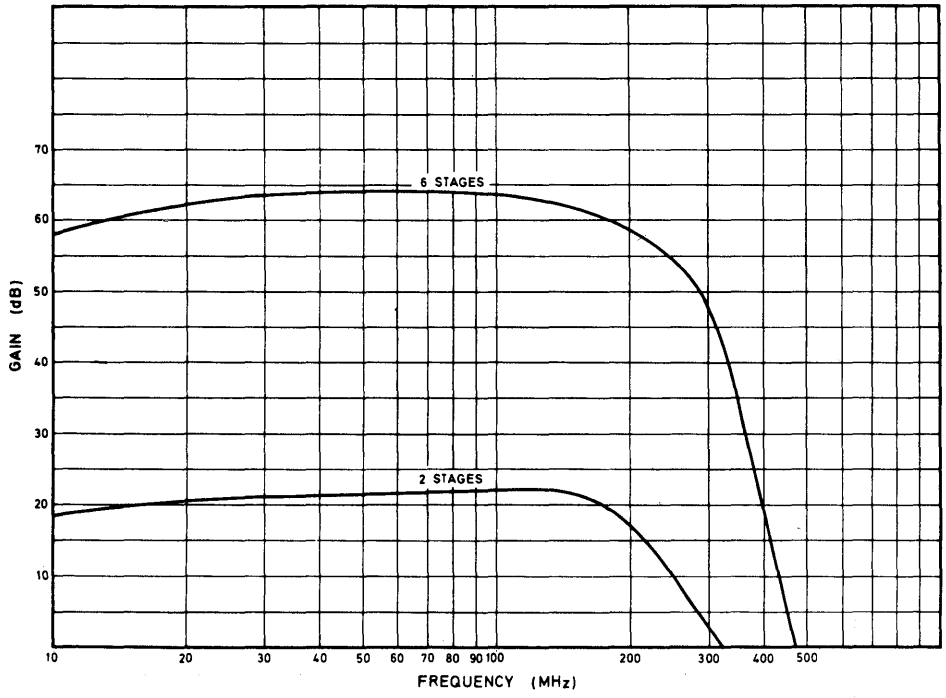


Fig. 18 Frequency response of log strip

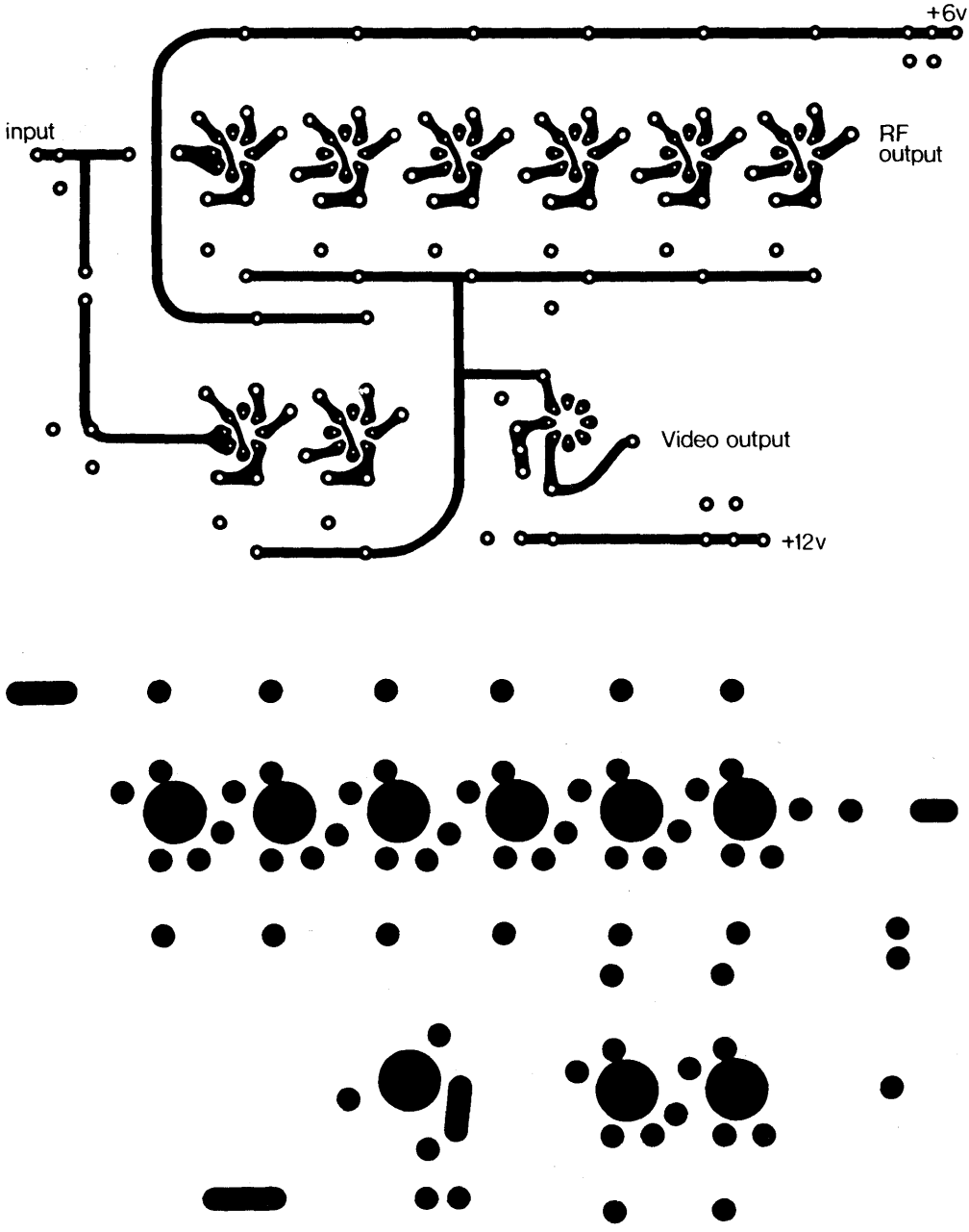
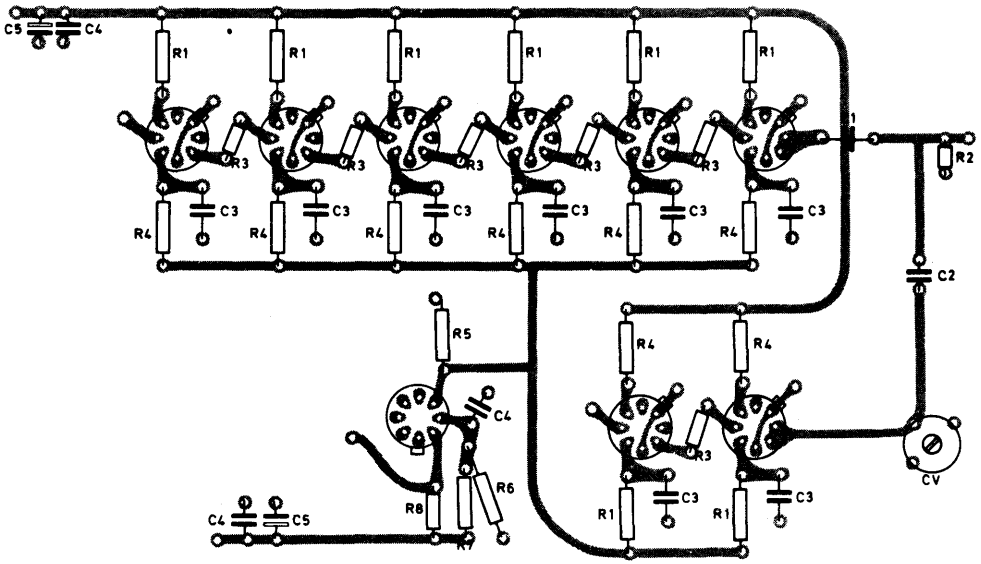


Fig. 19 Printed circuit board for log strip



4 A swept gain IF strip and detector

SL550 GENERAL DESCRIPTION

The SL550 is a general purpose wideband amplifier with an external remote gain control facility. It has been designed to operate from a 200 ohm source and it is therefore suitable for use with microwave mixers. The gain of 40dB over the band of 125MHz is obtained with good noise figure (2dB). The external gain control facility can be used to obtain a swept gain function; the SL550 is thus ideal for linear IFs or low noise pre-amplifiers in logarithmic strips.

The SL550 consists of a fixed gain amplifier, a variable amplifier together with input and output buffer stages (see Fig. 20). External gain control is performed in the feedback loop, hence the noise figure and output swing are only slightly affected as the gain is reduced. The gain is specified with an accuracy of $\pm$1dB for a given input control current, hence a defined gain-time law can be achieved.

The input transistor can be used in either common emitter or common base and the output current of the emitter follower can be increased with the addition of an external resistor to enable a low impedance load to be driven.

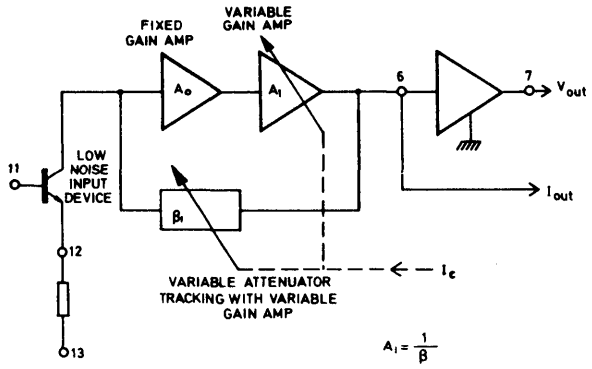


Fig. 20 Schematic of SL550

SL510 GENERAL DESCRIPTION

The SL510 consists of a detector, a voltage regulator and a video amplifier. The long tailed pair detector has both input bases accessible so it can be used as a full-wave or half-wave detector. The detector can be used either on its own or with the internal video amplifier, which in conjunction with the detector will give 5.5dB gain in the half-wave mode of operation. The detector band width is 100MHz and the video is 24MHz. The device can handle pulses as short as 16ns, has a dynamic range of 25dB and can develop 0.5V across 50 ohms.

DESIGN OF STRIP

Fig. 21 shows an amplifier using two SL550s plus an SL510 detector. The first stage is connected in the common emitter configuration which gives low noise performance when driven with a 200 ohm source which simulates a typical microwave mixer.

The second stage is connected in the common base configuration with 750 ohms at pin 7. The AGC current inputs are obtained through 3k ohm resistors. These resistors were chosen to give 30dB of gain control with optimum dynamic range.

Careful layout of circuit and selection of resistors for the AGC control lines, together with the use of physically small ceramic capacitors, ensures stable operation of the amplifier. A gain of 80dB at 30MHz is obtained with a gain reduction of 32dB with 6V control voltage.

An SL510 has been added to this strip to provide detection and video amplification. The SL510 is connected in its half-wave rectified mode using RC input coupling. The RF input is connected to pin 4, the base of the long tailed pair. The other base is earthed through a capacitor.

The positive-going half cycle of the input voltage is detected by the long tailed pair and appears as a change in the voltage at pin 8, which is connected through pin 9 to the input of the video amplifier. Due to the DC coupling between pins 8 and 9, the output quiescent voltage depends on the current flowing in the detector load. To make this less dependent on the beta of the

input pair, extra current is injected into pin 8 through a resistor R which is connected to the internal supply line.

The amplifier-detector combination will handle linearly input signals up to 2.5mV peak to peak when the gain is reduced by the AGC. The minimum input signal for a detectable video input is 2 microvolts peak to peak with maximum gain on the SL550s. Hence, the total dynamic range when used with swept gain is 62dB.

With the component values shown on the circuit diagram the minimum RF frequency is about 1MHz. At frequencies below this, the RF breakthrough would be excessive.

A printed circuit board suitable for the construction of this circuit is shown in Fig. 22 and the frequency response in Fig. 23.

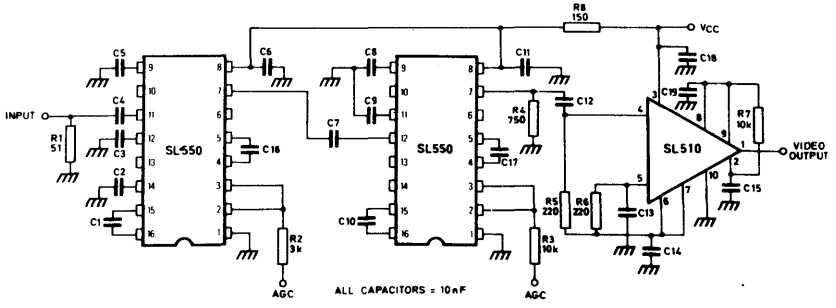


Fig. 21 Circuit diagram of variable gain amplifier

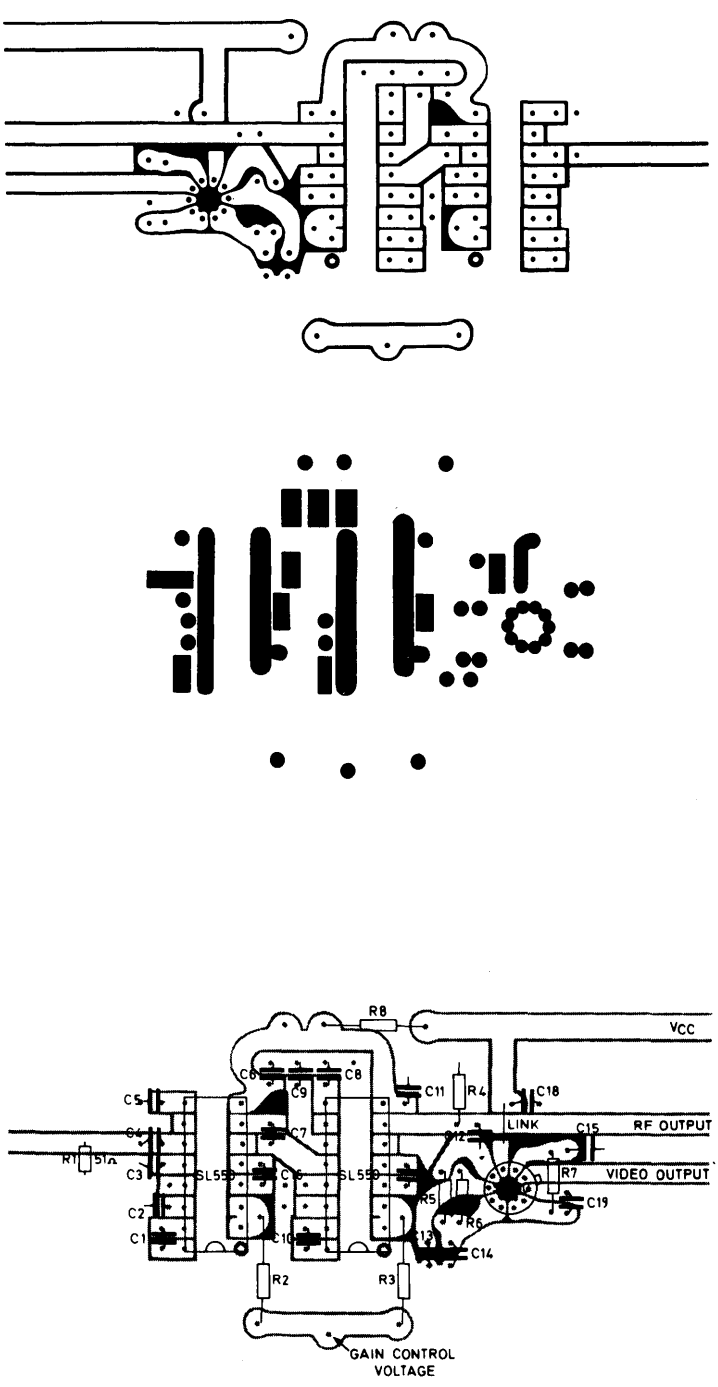


Fig. 22 Printed circuit board for variable gain amplifier

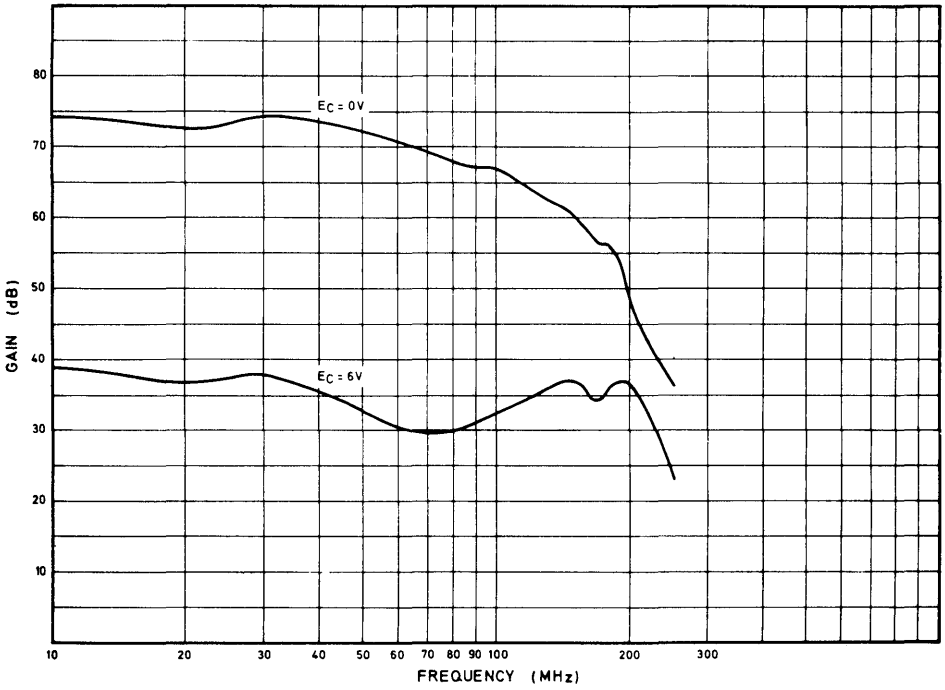


Fig. 23 Frequency response of variable gain amplifier

technical communication

Using the SL 362C low noise transistor pair

Plessey Semiconductors

The SL362C is a bipolar integrated circuit consisting of a pair of NPN transistors with exceptionally good noise performance and an f_T in excess of 1.6 GHz. It is in the same family as the SL360C, with the same close tracking of parameters inherent in a monolithic circuit, and is therefore suitable for use in circuits requiring a pair of well matched, high frequency, low noise transistors. A typical application in a DC to 200 MHz low noise amplifier is described in detail, but some general data on the noise performance of the SL362C is given first.

LOW NOISE TRANSISTOR STRUCTURE

At frequencies between the low frequency flicker noise region and the high frequency region in which the noise increases due to gain fall off effects, the dominant parameter contributing to noise in the transistor is base resistance. The base resistance inherent in a particular transistor process can be reduced by connecting a number of elementary transistors in parallel to form a larger transistor with much reduced base resistance. Using this technique, the base resistance of the SL362C has been reduced to 30Ω compared with 250Ω for the SL360C. Fig.1 shows a typical noise figure for the SL362C versus emitter current at the optimum source resistance for each current. This optimum source resistance is shown against emitter current in Fig.2.

The major trade-off in the design of this type of low noise transistor structure is noise performance against high frequency performance. However, the high f_T of the SL362C (see Fig.3) makes it possible to use the device at frequencies well in excess of 60 MHz.

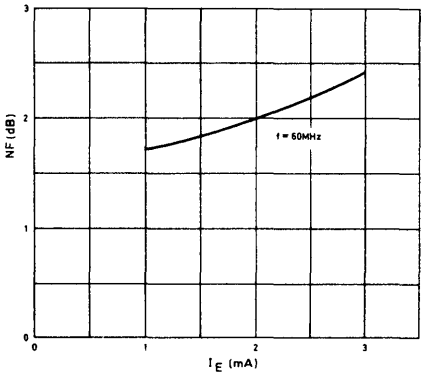


Fig.1 Typical noise figure at optimum source resistance

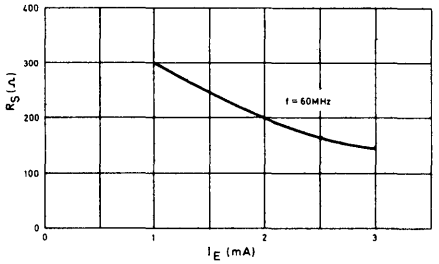


Fig.2 Optimum source resistance

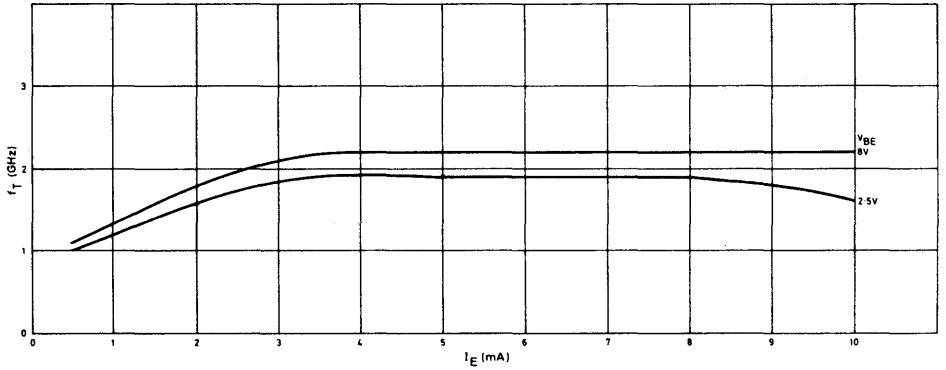


Fig. 3 Typical f_T v. emitter current

SIMPLE FEEDBACK AMPLIFIER (FIG.4)

The amplifier has a response down to DC achieved by the use of a long-tailed pair in the input stage, which also gives low offset voltages and a convenient method of applying negative feedback. The input is applied to Tr 1 and negative feedback applied to Tr 2 via resistors R 6 and R 7. Tr 3 is current-driven from the long-tailed pair and gives the output voltage across R 3. It is important to keep the stray capacitance from R 3 to ground as small as possible for the best high frequency performance. By the use of the very high f_T transistor pair SL360C for Tr 3 and Tr 4 any shunting effect of transistor capacitances across R 3 is reduced.

The frequency response of the amplifier shown in Fig.5 is flat to within ± 1 dB from DC to 240 MHz. The small peak at 200 MHz is not layout dependent but is due to parasitic lead inductance in the transistor packages. Measurements were made with a 50Ω source impedance and a load of 0.1 MΩ + 2.5 pF. The amplifier will drive a 50Ω load up to 150 MHz if required. For simplicity the noise figure was measured with a 50Ω source impedance and a spot noise figure of 4.2 dB was measured at frequencies of 30 to 200 MHz. The calculated variation of noise figure with source impedance is shown in Fig.6, which indicates an optimum noise figure of 2.5 dB at 200Ω source impedance.

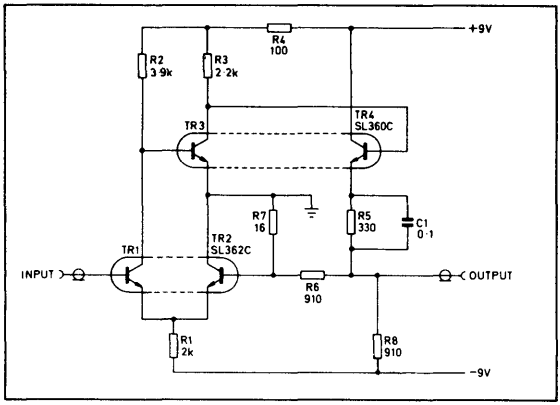


Fig.4 Circuit diagram

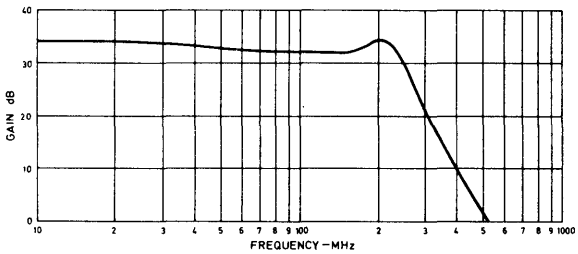


Fig.5 Frequency response of wide band amplifier

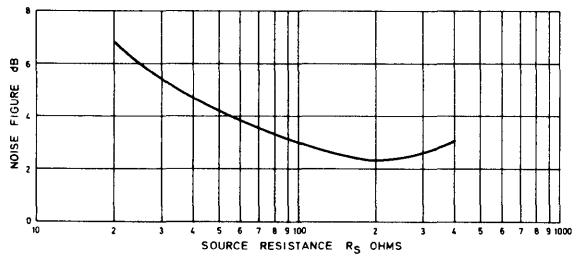


Fig.6 Calculated noise figure v. source impedance

LAYOUT

It has been found that the circuit is not particularly sensitive to layout change, but the obvious precautions in constructing VHF circuits should be observed. Transistor leads should be kept as short as possible, in particular the emitters of Tr 1, Tr 2 and Tr 3. The leads of R 7 should also be short and if accurate gain stability is not required, a carboncomposition resistor will give minimum inductance.

NOISE REDUCTION

Two techniques are available to reduce the noise figure at low source impedances. One is to use a transformer to produce a source resistance nearer to the optimum of 200Ω. The other method is to connect two transistors in parallel as shown in Figure 7. The effect of this combination is compared with a single transistor in Figure 8. The graph shows the calculated noise figure versus emitter current with a 50Ω source impedance for both long tailed pair and common emitter configurations. As can be seen, a noise figure of 1.6 dB at 50Ω source can be achieved with the arrangement of Figure 7 in a grounded emitter configuration. The parallel connected combination will, of course, have double the output capacitance of the single device, but the effect of this on the high frequency performance can be reduced by feeding into a low impedance. Also, the combination will have a lower f_T than a single transistor at a given operating current. However, if the current is doubled in the combination, little degradation will occur.

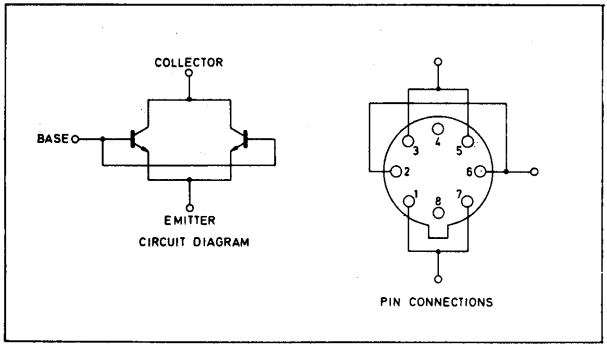


Fig.7 Parallel connection of two transistors

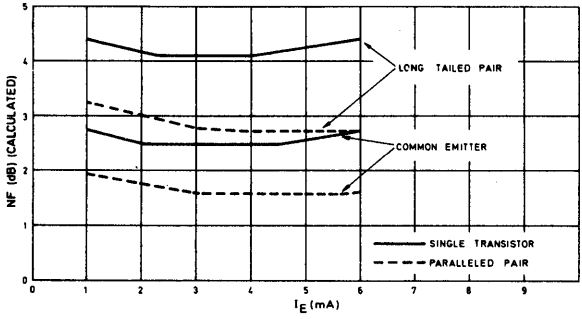


Fig.8 Noise figure at 50Ω source impedance

LOW COST LOG IF STRIP

1. INTRODUCTION

Successive detection logarithmic IF Strips have held a dominant place in professional and military pulse radars for many years. Their ability to handle signals in a very wide dynamic range without losing amplitude information is very difficult to better with other techniques.

The advantages of log IF Strips have not been available in the past to manufacturers of low cost radars due to the high price of the components required.

Now Plessey is offering low cost ICs which can be used to make a very wide dynamic range strip at a component cost below £10.

This major cost reduction has been possible by our experience in manufacturing the SL521 series of military grade log amplifiers, by the use of sophisticated automatic test equipment and the choice of an eight lead plastic package for the integrated circuit.

This note contains a brief introduction to the operation of successive detection IF Strips, a description of the circuitry used in the Plessey integrated circuits and practical details of a strip which can be used at 30 or 60 MHz. The main features of the Strip are:—

Centre Frequency	30 or 60MHz
Bandwidth	up to 15MHz
Input Signal Range	−80 to +15 dBm 20μV to 1.2 volts rms
Output Voltage Range	0.1 to 2.0 volts
Current Consumption	140mA
Video Rise Time	20ns
Noise Figure	4dB

2. SUCCESSIVE DETECTION LOG STRIPS

The basic stage used in a log strip is shown in Fig. 1. A limiting amplifier with a gain of around 10dB is followed by a low level detector. One input and two outputs are provided, an RF output and a detector output which is commonly referred to as the video output.

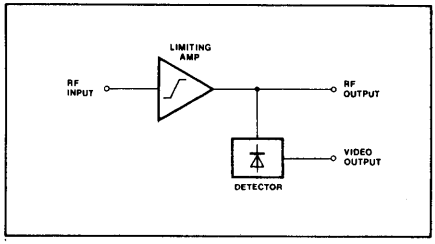


Fig. 1 Basic log stage

The responses, RF in to RF out and RF in to video out, for a typical member of the SL521 family are shown in Fig. 2. An important feature is that the video and RF outputs limit at a particular input level.

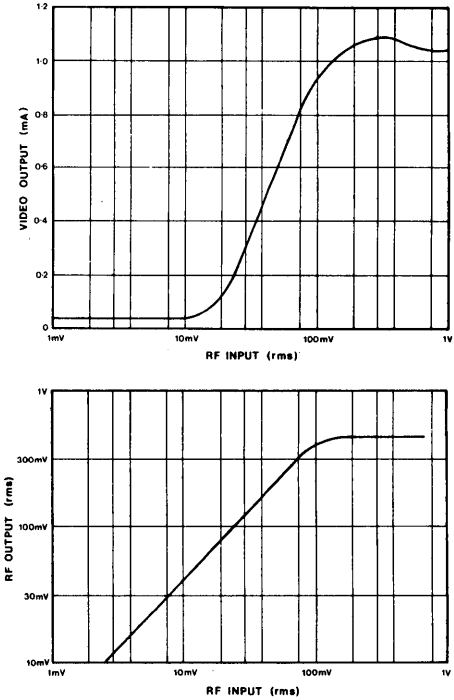


Fig. 2 SL521 transfer function

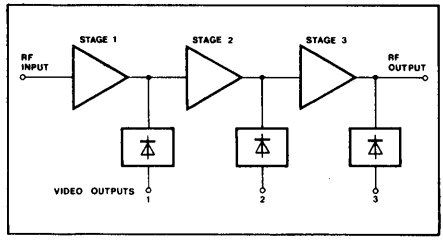


Fig. 3 Three stage strip

Consider a 3 stage strip built with circuits of this type as shown in Fig. 3. The first stage will clearly give a video output identical to the single device. The second stage receives an input signal increased by the gain of the first stage. Over the range of the detector this gain is constant so when a logarithmic scale is used for the RF input the second stage video output will be identical to that of the first stage just displaced to the left by the stage gain, as shown in Fig. 4.

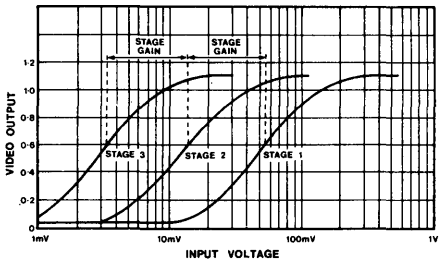


Fig. 4 Video outputs from 3-stage strip

The final step in making a log strip is to sum the video outputs from each stage. The schematic and corresponding response is shown in Fig. 5.

We now have a log response. For each increase in input level corresponding to the stage gain, a contribution equal to the maximum video output from a single stage is added to the summed video output. It is interesting to see from Fig. 5 that by careful shaping of the detector turn on characteristic (such that it goes from minimum to maximum output for an input change equal to the stage gain) a very accurate log law can be obtained.

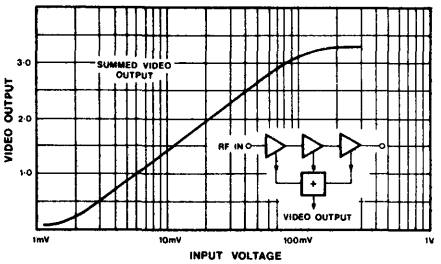


Fig. 5 Output from strip

The dynamic range of a log strip can be extended by simply increasing the number of stages. The limit is reached when the last stage in the cascade reaches full video output solely on the noise produced by the first stage.

The number of stages can then only be increased if the bandwidth of the strip is reduced. It is common practice to insert a bandpass filter in the centre of the log strip for this purpose. Another technique for increasing the dynamic range is to attenuate the input signal and apply it to another short strip operating in parallel to the main strip. The video output from this subsidiary strip is added to that from the main strip. Normally the log response limits when the input signal exceeds that necessary to produce full video output from the first stage. However the subsidiary strip is being fed with an attenuated signal so will continue to give an output change. The limit to this technique is reached when the input voltage is sufficient to cause damage to, or overload in, the first stage of the main strip.

Thus, using the techniques outlined above with a simple stage of the type shown in Fig. 1, a log IF Strip can be built with a dynamic range limited at one end by the noise and at the other by the overload level of the first stage. With well matched stages the strip will give an accurate log law and video detection is an integral part of the strip.

3. THE SL521 SERIES CIRCUITRY

The Limiting Amplifier

The circuit diagram of the SL521 is shown in Fig. 6. This IC contains all the components necessary for a single stage of the type described above. Voltage amplification is provided by the long-tailed pair TR1, TR2.

The gain (× 4 or 12dB) is defined by feedback derived directly from the RF output and applied to the base of TR2. This feedback also controls the RF output quiescent voltage. The difference between the input and output quiescent voltages is kept low so that cascaded stages can be directly coupled.

The Detector

TR4 and TR5 form a simple half wave detector with an open collector, current output.

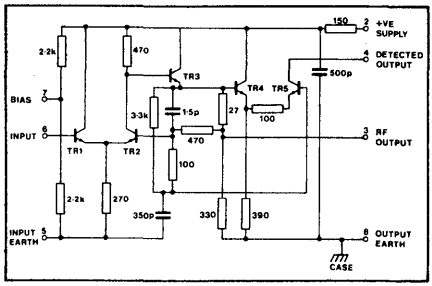


Fig. 6 SL 521 circuit diagram

In the quiescent state the base of TR5 is biased at a voltage approximately 100mV lower than the base of TR4. Hence TR5 is off and virtually no current is drawn by the detector output. When an RF voltage is applied to the input of the SL521 the base of TR4 is driven with the RF output voltage by the emitter follower TR3.

Since the base of TR5 is decoupled by the 350pF capacitor, no RF voltage will be present.

On the negative going half cycles of the RF, TR4 will switch off and TR5 will conduct.

The 100-ohm resistor between the emitter of TR4 and TR5 causes the video output current to increase gradually with increasing RF input over a 12dB range so that a straight line log characteristic can be obtained.

The open collector video output enables the video outputs to be summed by just connecting all the outputs to a common load resistor.

There is no smoothing of the video output provided internally and the video output at frequencies up to 60MHz follows closely the negative half cycles of the RF waveform. There is no internal limit on video rise time. Obviously there must be some video filtering to remove the RF component present on the video line and this can be an important part of the strip design when very fast rise times are involved. However in most cases simple R-C filtering is sufficient.

Cascading Stages

Several features of the design have been included specifically to ease problems of cascading many stages. The low input-output differential voltage means that the amplifiers can be cascaded without coupling capacitors. Internal supply line decoupling is provided by the 150-ohm resistor in series with the supply and the 500pF internal capacitor. This is sufficient to largely eliminate the problem of feedback from output to input along the supply lead. Another potential source of oscillations is feedback along the video line. The simplest way of preventing this without sacrificing video response time is to put a resistor in series with each video output and then sum the currents in a stage with a low input impedance. Fig. 7 shows a simple method of achieving this with a common base summing transistor.

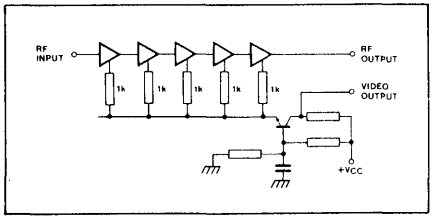


Fig. 7 Use of common base summing stage

Oscillations caused by earthing problems do not occur as long as the earth pins are connected by short leads to a good ground plane.

4. SELECTION GUIDE

The table above describes the current Plessey Semiconductors devices suitable for building successive detection log strips. The general feature of the devices is that the cost of a device depends mainly on the tightness of its specification. The premium device, the SL521A has a gain specification of 11.5dB min. and 12.5dB max. at 30MHz and the device we have used in the low cost strip is the SL1613 which has a specification of 10.4 min. to 13.3dB max.

5. GENERAL DESCRIPTION OF LOW COST STRIP

The low cost strip using the SL1613 is shown in Fig. 8. The strip basically follows the concepts outlined in previous sections. The most unconventional feature is the use of a negative supply. This feature makes decoupling and earthing a little more difficult but has been used to simplify the video output. A conventional strip will have a positive supply and the video output will be generated in a resistor connected to this supply. In many systems it is undesirable to have the output referred to the supply and a high slew rate OP amp has to be used to obtain an output voltage referred to ground. This works very satisfactorily and a circuit using the SL541C video amplifier is shown in Fig. 9. However the cost of this circuitry is significant and can be eliminated by using a negative supply and generating the video output in a resistor connected to ground. The video output is then a negative going voltage referred to ground which can be easily processed by succeeding circuits.

A detailed circuit description and constructional details are given below. Typical performance graphs are also given. Since the SL1613 has wide gain and video output variations the accuracy of the log law will be quite variable. However several strips have been built here and they all lie well within the expected ±3.5dB accuracy.

SELECTION GUIDE

Number	Type	Package	Frequency Range	Grade	Gain Accuracy	Typical Log Accuracy	Application
SL521	Single Stage	TO5	20 – 80MHz	A B C	±0.5dB ±0.7dB ±1.0dB	±1dB ±1.5dB ±2db	Military/Professional Log Strips
SL523	Dual Stage	TO5	20 – 80MHz	B C	±1.5dB ±2dB	±1.5dB ±2dB	Very small/lightweight Log Strips
SL525	Single Stage	TO5	30 – 60MHz	C	±1.5dB	±3dB	Low Cost Strips
SL1613	Single Stage	8 Lead DIL Plastic	30 – 60MHz	C	±1.7dB	±3.5dB	Very Low Cost Strips
SL1521	Single Stage	TO5	20 – 200MHz	A B C	±0.5dB ±0.8dB ±1.2dB	±1db ±1.5dB ±2.5dB	Wide Band IF Strips
SL1523	Dual Stage	TO5	20 – 200MHz	C	±2dB	±2dB	Small/lightweight Wideband Strips

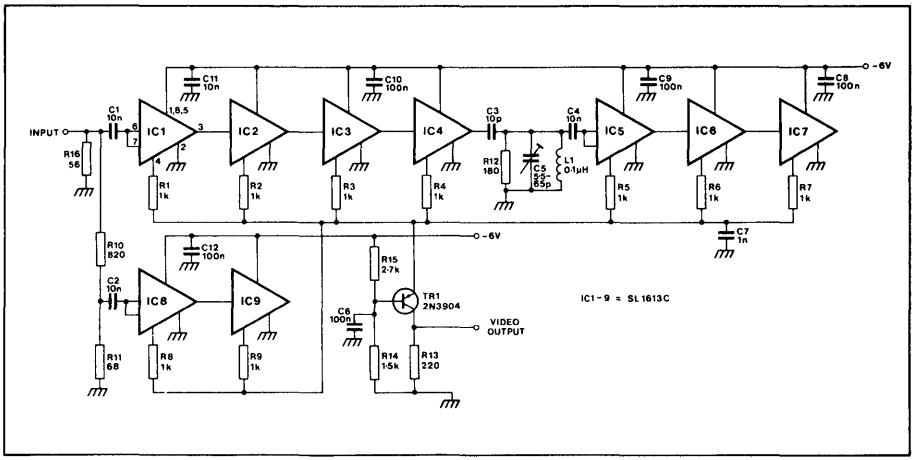


Fig. 8 Circuit diagram of low cost strip

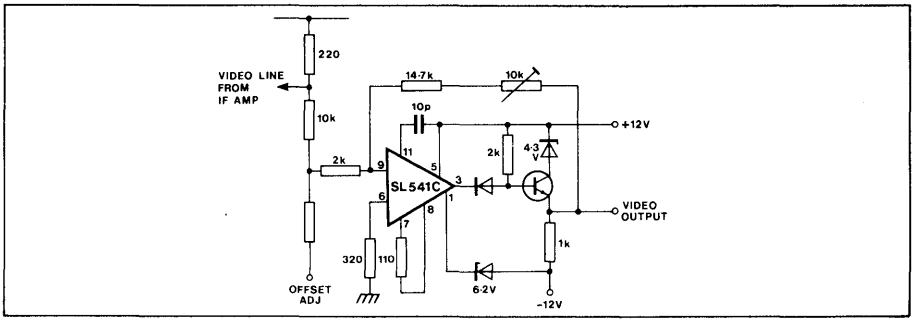


Fig. 9 Video output stage

6. CIRCUIT DESCRIPTION

The connection to each of the IC's is very similar. Pins 1, 8 and 5 are joined together and connected to the negative supply, Pin 2 is earthed and the input is applied to Pin 6. IC's 1, 5 and 8, being the first devices in directly coupled cascades, have the bias Pin 7 connected to Pin 6. The video output is taken from Pin 4 and the RF output from Pin 3. The resistors R1 to R9 prevent feedback along the video line which is decoupled by C7 and feeds into the output transistor TR1. R14 and R15 provide bias for the base of TR1 which is decoupled by C6.

The output voltage is generated across R13 which could be varied to adjust the slope of the log characteristic. The video response time is determined by C7. Lower values for this capacitor would improve the response time at the expense of IF breakthrough.

The resistor network at the input to the strip R10 and R16 provide a 50-ohm input impedance and attenuate the input signal for application to the subsidiary strip IC8 and 9. The value of R10 should be in theory be 15 times R11 but in practice it is chosen to give a straight log law at input signals greater than 0dBm. The filter between IC's 4 and 5 defines the IF bandwidth. The values given are for 60MHz operations with a bandwidth of about 15MHz. The bandwidth of the filter is a compromise between sensitivity and response time. If the bandwidth is too wide IC7 will produce full video output on the noise produced by the first stage and the dynamic range will be reduced. Another important requirement on the filter is that it should, at resonance, have unity voltage gain. Any errors in the filter will produce a kink in the log characteristic at input level between −50 and −60dBm.

The log strip is not designed to drive long lines on the video output. To prevent a degradation in video response time the load capacitance should be kept below 20pF.

7. CONSTRUCTIONAL DETAILS

The schematic of a printed circuit board is given in Fig. 10.

Double sided PCB has been used with a minimum amount of copper removed from the component side. It is advisable to solder all earth connections to both sides of the board.

The resistors used on the prototypes were 0.125W moulded carbon throughout and the capacitors were general purpose radial lead ceramic types similar to 'Erie Redcaps'. The inductor is a fixed Cambion type. The component overlay shows recommended supply line decoupling components. Provision has been made on the PCB for additional decoupling capacitors but they have not been necessary on the prototype strips. Two negative supply points are marked on the PCB which can simply be connected to a common supply.

8. PERFORMANCE

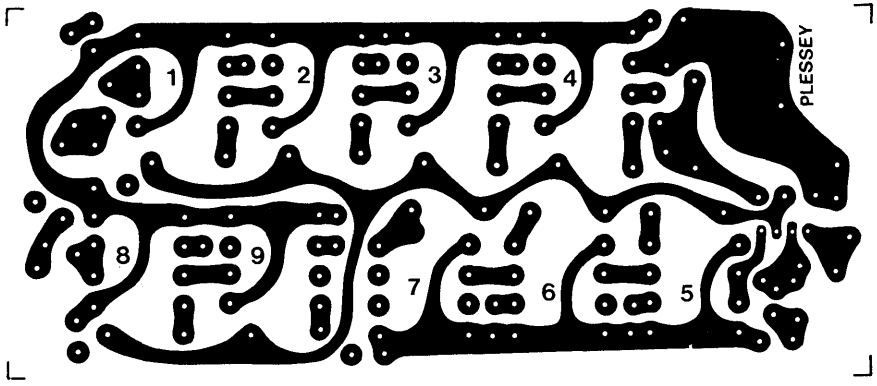
The input output characteristic of a typical SL1613 strip is shown in Fig. 11. The 60MHz input power in dBm. (dB with respect to 1 milliwatt in 50 ohms) is plotted on the X axis and the negative output voltage on the Y. It can be seen that a log range greater than 90dB is obtained from +15dBm −75dBm and that all the points are within 3dB of a best straight line. This response was measured at 60MHz with a CW source. Figure 12 shows the input/output characteristic of a typical strip as the supply voltage. The only effect over a voltage range of −5.5 to −7.0 volts is a small variation in the slope of the log characteristic.

The pulse performance of the strip is shown in Figs. 13 and 14. Figure 13 shows the pulse response with an input pulse at 60MHz of 0.5μs varying in amplitude from 0dBm to −80dBm. Figure 14 illustrates the effect of input pulse lengths from 0.1μs to 0.6μs. The video rise and fall times are about 0.05 s and the pulse is stretched by about 0.05μs at the 50% points. If these rise and fall times are not fast enough then the video smoothing capacitor can be removed, which increases the 60MHz breakthrough but approximately halves the rise and fall times. Figure 15 (a) shows the response of the normal circuit to a 0.1μs pulse and Figure 15 (b) shows the effect of removing C7. Figure 15 (c) shows the response of a strip with C7 = 0 to 60MHz pulses with widths of 0.050, 0.1 and 0.15μs. The peak video response to a 0.05μs pulse is about 20% less than that of a CW signal.

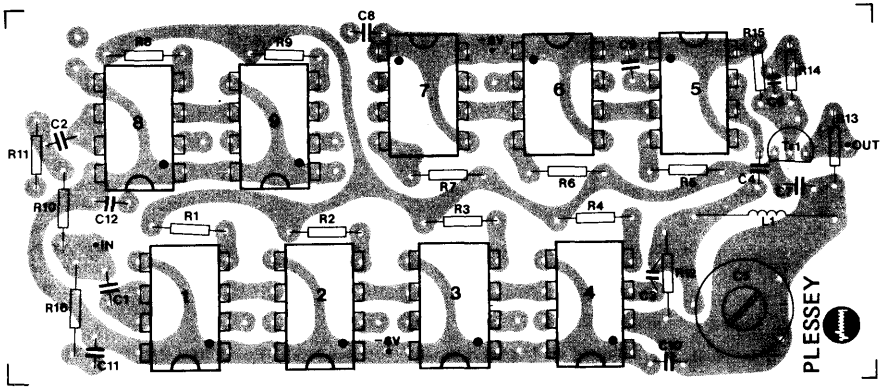
9. A FEW HINTS ON TESTING LOG STRIPS

The log characteristic such as Figure 11 is one of t most important measurements to be carried out on a log strip. This is most easily measured with a CW source, a digital voltmeter and an attenuator. A high quality attenuator is, of course, needed for measurin strips with an accurate log law. It is not uncommon find a previously unknown fault on a lab attenuator when testing an accurate log strip.

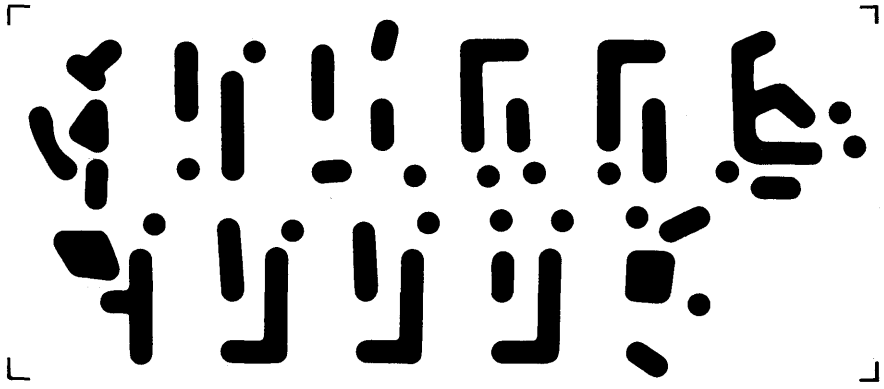
As explained in Section 6 the log characteristic ca highlight several possible faults, for instance a chan in slope above 0dBm indicates an error in the input a tenuator (R10-R11) and a kink around −50 to 60dB suggests problem with the filter. Measuring log responses by a manual point by point method can b rather tedious and a commercial log test set can be used to speed this up. It is also possible to use a sig generator which includes a programmable attenuato linked to a X Y plotter. The block diagram of the simple test system is given in Figure 16.



Printed circuit layout



Component location



PCB ground plane

Fig. 10 Printed circuit board *Scale 2:1*

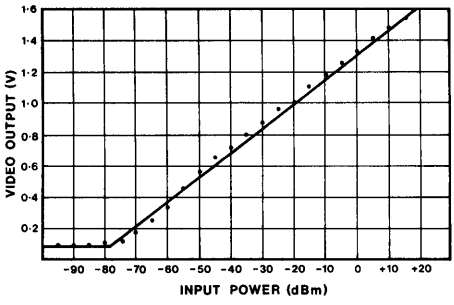


Fig. 11 Dynamic range for SL1613 strip

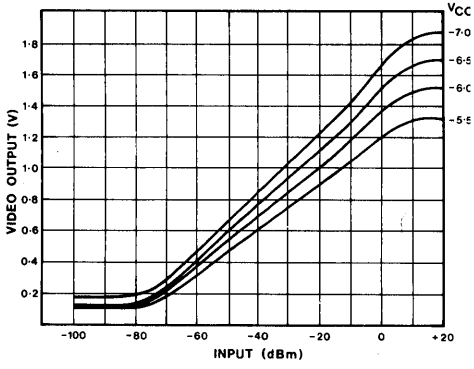


Fig. 12 Effect of supply voltage

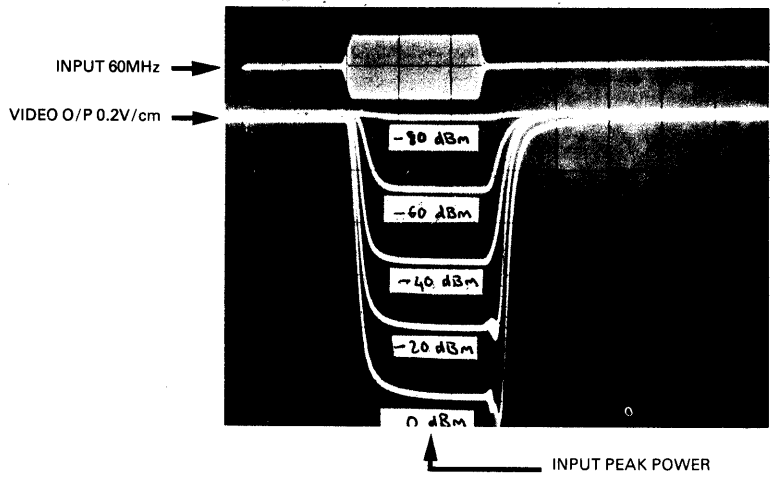


Fig. 13 Pulse response v. input power

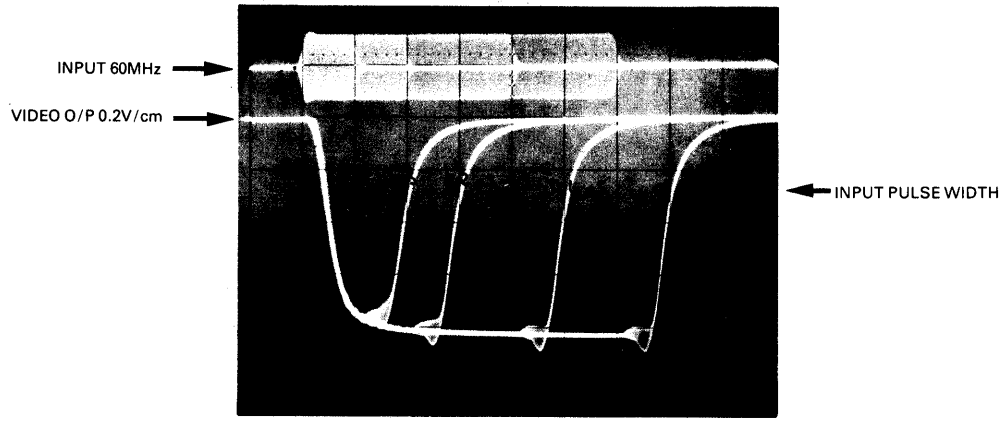


Fig. 14 Pulse response v. input width

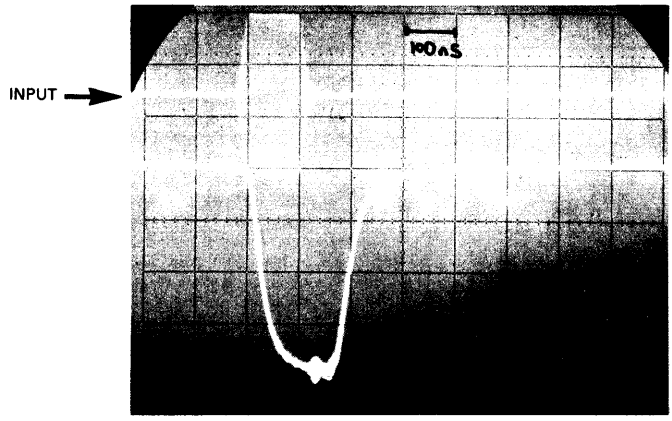


Fig. 15a Response to narrow pulses
(input 100ns/ – 20dBm, C7 = 1000pF)

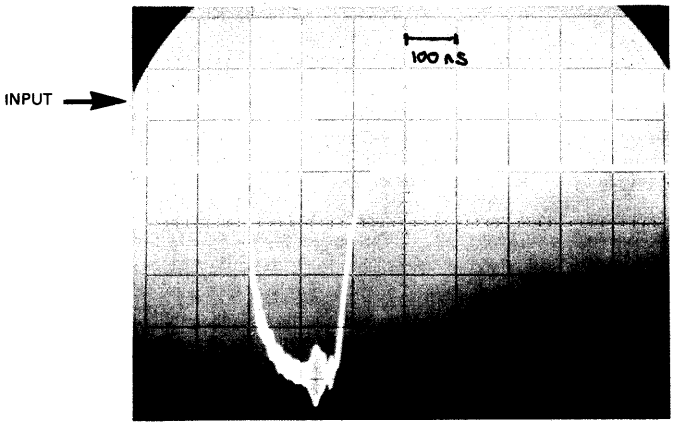


Fig. 15b Response to narrow pulses
(input 100ns/ – 20dBm, C7 = 0)

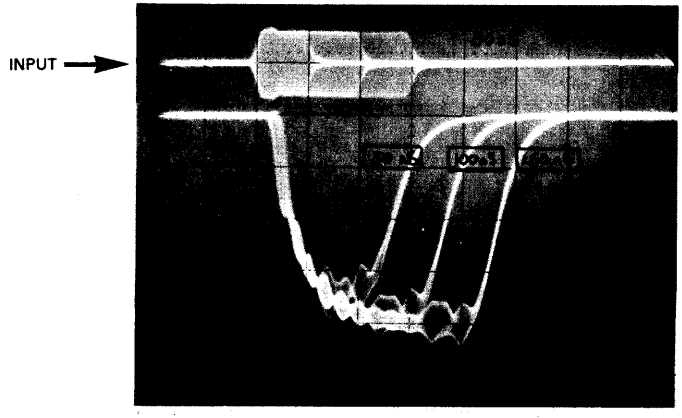


Fig. 15c Response to narrow pulses
(input 50, 100, and 150ns, C7 = 0)

The measurement of bandwidth can also be carried out with the equipment shown in Figure 16 but turning of the filter is more easily achieved with a swept tuning system such as that in Figure 17.

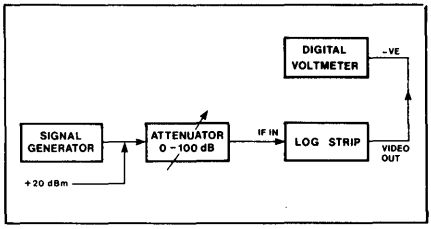


Fig. 16 Log characteristic measurement

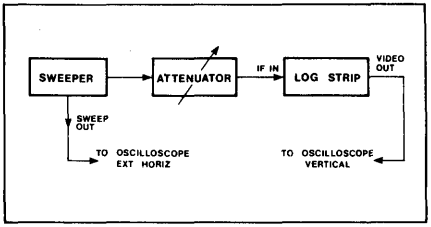


Fig. 17 Bandwidth measurement

Bandwidths can be measured by using the input attenuator and reading 3dB, 20dB widths etc. from the oscilloscope. It is much easier to measure IF to video characteristic as above than to measure from IF input to IF output. The IF output of the strip limits at just 10 to 20dB above the noise and the combination of the high IF gain and this small dynamic range makes it a rather difficult measurement.

Once the log characteristic and the bandwidth have been measured the only important characteristic left is the pulse response. The only difficulty with this measurement is the generation of a suitable IF pulse. The best method is to generate a pulse at a microwave frequency (say 2GHz) with a PIN diode modulator and then mix this down to IF. In this way a pulse with a high on-off ratio and with very small video breakthrough can be generated. This however involves a lot of expensive test equipment and simpler methods can be used to generate a usable pulse directly at IF. It should be remembered that the log amp will exaggerate any small imperfections in the pulse. An on-off ratio of 80–90dB is needed and breakthrough of the video pulse edges must be kept very low. Two cascaded double balanced mixers can generate a pulse with a high enough on-off ratio but will generally have a video breakthrough level which is too high for most measurements. High isolation solid state switches are available which will generate an adequate pulse at IF frequencies and such a switch was used for Figures 13 and 14. A log amp will have a strange effect on a pulse with exponential rise and fall shapes as shown in Figure 18. The log amp will apparently sharpen the leading edge and slow down the trailing edge of such a pulse. This effect is not caused by any deficiencies in the log amp but happens for a theoretically perfect amplifier.

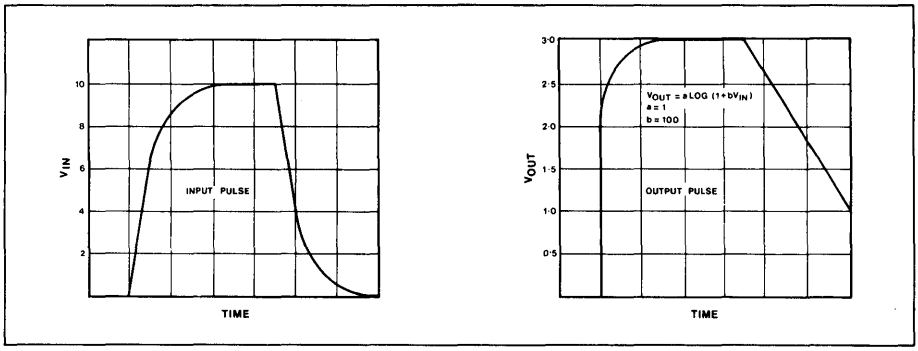


Fig. 18 Effect of log. amp on pulse response

DIGITAL SIGNAL PROCESSING APPLICATIONS

Introduction

Most variables encountered in electronic systems change in a continuous or analogue fashion, and indeed most transducers provide analogue outputs. Nevertheless, there is a growing trend to apply more and more digital control and computation hardware to commercial, industrial and military equipment. One reason for this is the increasing availability of digital logic and memory integrated circuits at very attractive prices. Recently, the high speed capability of the ECL logic family has extended the range of frequencies for which digital processing is possible. The advantages of digital processing techniques are well known, and include such benefits as high accuracy and high noise immunity in environments which could seriously impair the performance of an equivalent analogue system. Analogue to digital converters (ADCs) are an essential part of all such systems.

Digital signal processing is now practical at video and IF frequencies and is consequently being applied to television and radar systems. Other areas in which high speed analogue to digital conversion is being used are fast transient analysis, fast data transmission and secure speech transmission.

1 A to D conversion

CONVERSION METHODS

There is a great variety of conversion techniques which are at present being pursued. It is fair to say that the majority of these are more suitable for lower speeds where they have achieved low cost, low power consumption, or extremely high accuracy up to at least 14 bits. When the highest possible conversion speed is essential the choice of techniques is narrowed down considerably.

The majority of ADCs accept an AC input signal, which can occupy an equal positive and negative range, and the input/output function is usually linear. The output code is normally a binary N-bit code in which the all '0's state corresponds with the most negative input voltage and the all '1's state corresponds with the most positive input voltage. In some cases the outputs may be presented as an N-bit output code plus a sign bit, giving the converter effectively N+1 bit accuracy. ADCs do exist which differ from these formats to fit special needs, such as a Gray coded output or logarithmic transfer characteristic.

All parallel

The fastest known conversion method is the all parallel converter shown in Fig. 1. It is so called because 2^n-1 comparators compare the analogue input with an equal number of reference voltages. The reference voltages are uniformly spaced, and span an equal positive and negative range. The centre reference voltage is therefore zero. The outputs of the comparators are encoded by logic circuitry to give an N-bit logic code. A latch signal is fed to the comparators which forces them to make an unambiguous decision, i.e.

give a true logic '0' or '1' at the output, so preventing spurious output codes. In this way, a synchronous output is obtained. This is a very basic converter schematic and a practical ADC may include refinements such as output latches to re-time the output bits, an input sample and hold circuit, or the provision of a "conversion complete" timing signal. The speed of this type of converter is in principle only limited by the time the comparators take to make an unambiguous decision. There is also the advantage that if the "acquisition times" of the comparators are well matched, the system can be operated without an input sample and hold circuit.

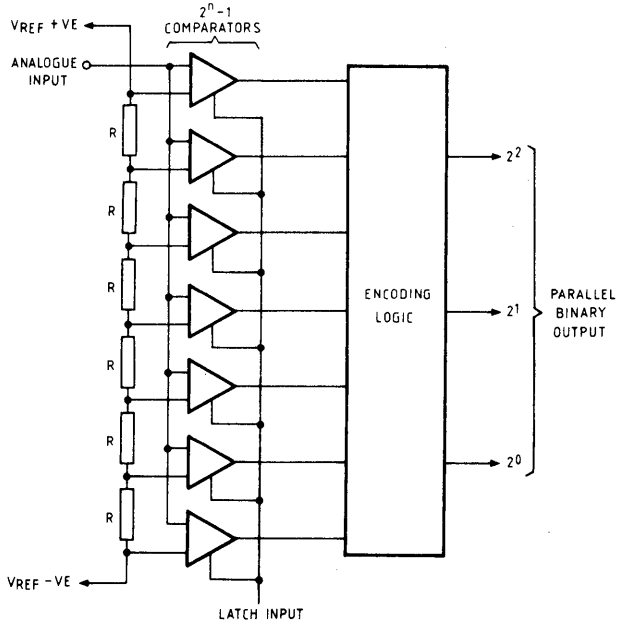


Fig. 1 The all parallel conversion method

All parallel, or "flash" converters as they are sometimes called, can be conveniently constructed using discrete comparators up to four or five bits. Beyond this it is highly desirable to have more than one comparator integrated into a single monolithic chip, to offset the problem of increasing size and cost. It is difficult to distribute the analogue input signal to a large array of discrete comparators with sufficient amplitude and phase accuracy, and to provide adequate latch timing accuracy. In addition, the output encoding gives rise to timing problems for higher bit accuracies. An integrated circuit which offers four or more comparators in a single package will considerably ease the above problems.

All-parallel converters have been built which are capable of clocking at up to 100 million samples per second, and with accuracies of up to 6 bits.

Parallel/series

The parallel/series conversion method is a hybrid form which is a compromise between the characteristics of all-parallel and all-series converters. A variety of designs are possible using 2, 3 or even more stages of conversion. Fig. 2 shows a converter in which two four-bit stages are connected in series to give eight-bit conversion accuracy. The analogue input is fed into a four-bit all-parallel converter of the type previously described, after first being sampled by a sample and hold circuit. Here, a coarse quantisation is performed which provides the four most significant bits (MSBs) of the output code. The output is fed into a four-bit digital to analogue converter (DAC), having eight-bit accuracy. The result is an analogue level which is an approximation of the input to the nearest four-bit code below the original signal. This is then fed into a subtractor circuit element together with the sampled analogue input.

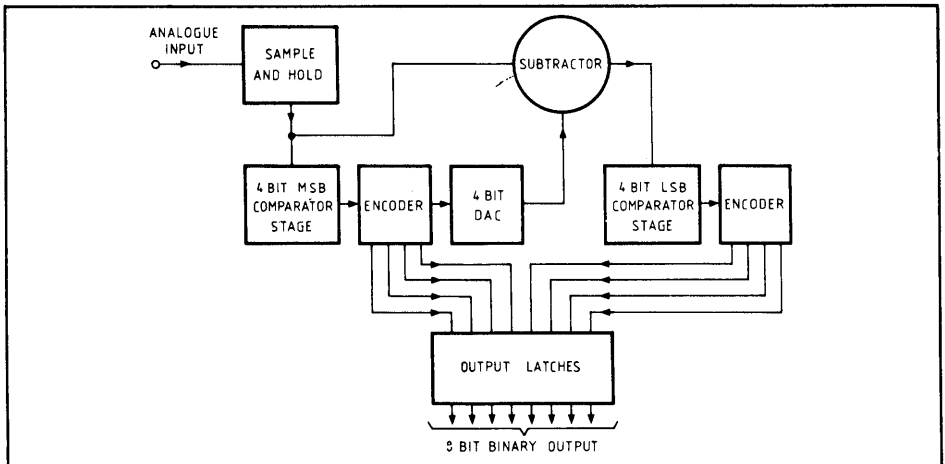


Fig. 2 The parallel series conversion method

The difference voltage will come within the range of the second four-bit ADC stage, which is again an all-parallel converter. The quantised output provides the four least significant bits (LSBs). Since the analogue signal has to propagate through an ADC and a DAC, and be compared with the input, the sample and hold is required to store the analogue signal for approximately one clock period to the full eight-bit accuracy. The outputs from the two stages are re-timed in a group of latches to give synchronous outputs.

The parallel-series converter has the advantage over the all-parallel of using less hardware, and hence less power is consumed. For example, an eight-bit all-parallel ADC uses 255 comparators, whereas a 4 × 4 bit parallel/series converter uses only 30 comparators. However, because the analogue signal has to propagate through several stages, conversion rate is lower than is possible with the all-parallel converter. The parallel/series ADC therefore provides a compromise between cost, power consumption, size and conversion speed. Other versions of the parallel/series converter may have more stages, for instance, 3 × 3 × 3 bit stages could be used to give nine-bit accuracy using 21 comparators, at correspondingly lower speed.

Successive approximation

The third converter to be described is the successive approximation type. It has been hitherto regarded as a slow conversion method, but with today's technology – ultra fast comparators, fast current switching, etc.– a very useful performance is obtainable. An attractive feature of the successive approximation technique is that it requires very little hardware. It is consequently possible to integrate an ADC of this type onto a single chip with eight-bit or higher accuracies. The successive approximation converter, shown in block form in Fig. 3 uses a DAC in a feedback loop. In operation, the shift register sets a 1 in the MSB latch, all other latches being in the logic 0 state. The DAC output is compared with the analogue input and the MSB latch remains set or is reset to 0 depending on whether the analogue input is greater or less than the DAC output. During successive clock periods this process is repeated with bits of diminishing significance. The DAC output therefore becomes a progressively more accurate approximation to the analogue input, taking N clock periods to achieve N-bit resolution. As with the parallel/series ADC a sample and hold is essential, although it may not be included in a monolithic converter. Using present-day technology, a monolithic successive approximation converter of eight-bit accuracy and a sample rate of 15MHz is feasible.

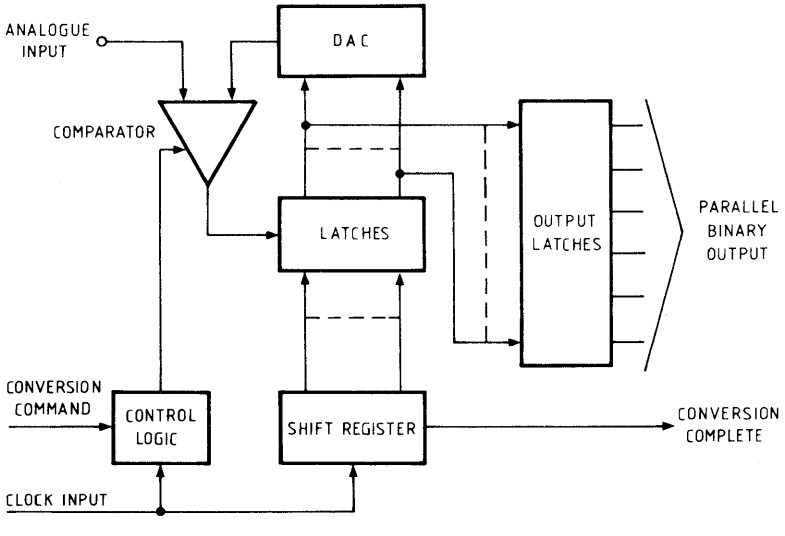


Fig. 3 The successive approximation conversion method

SPEED, RESOLUTION AND ACCURACY

The most important parameters when designing an A-D converter system are speed, resolution and accuracy. Speed is usually expressed as maximum sample rate and the maximum input frequency is limited by the Nyquist theorem to half of the maximum sample rate. In most converters, it is essential that this input limit does physically exist in the form of a low pass filter. Furthermore, the Nyquist limit point is actually 3db down, so for a flat response, the input should be rather less than half the sample rate.

Resolution of a converter is defined by the number of bits available, e.g. an eight-bit converter has a resolution of 1 part in $(2^8 - 1)$ or 1 in 255 (zero is also a step, so 256 levels are defined).

Accuracy may be equal to, or better than, the resolution, i.e. the converter may be specified as $\pm\frac{1}{2}$LSB or even $\pm\frac{1}{4}$LSB, or, exceptionally, $\pm\frac{1}{10}$LSB. While $\pm\frac{1}{2}$LSB is the minimum accuracy that will guarantee monotonicity, $\pm\frac{1}{4}$LSB may be useful when, for instance, the temperature coefficient is $\pm\frac{1}{4}$LSB over the range. In this case, the sum of a $\pm\frac{1}{4}$LSB basic accuracy, plus a $\pm\frac{1}{4}$LSB temperature shift will give a $\pm\frac{1}{2}$LSB accuracy over the temperature range. Many converters are not specified to the most desirable degree of accuracy. A common specification on eight-bit conversion is 1% i.e. $\pm$0.5% when the resolution is 1 in 255, i.e. the resolution is greater than the accuracy.

Usually, this type of converter will be monotonic over the full range, but departs from the ideal linearity in the mid-range; the error occurs at the mid-range, because the start and end points are defined by scale and offset factors. At lower speeds, specific systems may demand a higher resolution (i.e. number of bits) than can be achieved with a matching accuracy and linearity. A typical example is high quality audio in which quantisation noise and hence dynamic range is of extreme importance, but absolute accuracy is of less importance.

At video speeds, resolution and accuracy are usually equal except under transient conditions, when small inaccuracies are tolerable – an example is in video processing when the interval between fields may be used for programme source change.

THE COMPARATOR – AN IMPORTANT CIRCUIT ELEMENT

The ADCs described above use at least one comparator. Indeed all conversion techniques use a comparator of some kind. The speed performance in most, if not all, conversion systems is dependent on the response time of the comparator(s). Even low speed converters can require fast comparators, especially when very high resolution is required.

To achieve the highest possible conversion rates, a comparator with an extremely fast response is needed. To make an impact on the attainable performance of high speed converters it is essential to start with the comparator design.

Until recently, commercial comparators have used high gain (greater than 1000) to obtain the mV resolution necessary in A-D conversion.

When the converter operates in a synchronous mode (which is invariably the case in present-day converters) there will be a clock pulse available to enable the comparators to operate in the latching or sample and hold mode. In essence a latch is a positive feedback circuit: during the latch cycle, the gain tends towards infinity. This feature ensures that a comparator of even

very low gain in the sample mode will resolve a 1mV signal. By accepting a low gain, the comparator design can be optimised for a very wide bandwidth and extremely fast response time.

Later sections of this handbook describe the Plessey high speed comparators which use this principle to achieve set up times of 2ns and input to output delays of less than 3ns.

2 Practical system design

MICROSTRIP TECHNIQUES

Microstrip techniques have been used in the microwave field for many years and are now well characterised. Relatively recently, the advantages of accurate matching and minimisation of reflections associated with microstrip have been adopted for high speed digital circuitry. When the edge speed in a circuit is comparable with the propagation delay down the lines in use, microstrip is needed.

A cross-section diagram is shown in Fig. 4. Points to note are that the devices are usually mounted on the ground-plane side of the double-sided board; the presence of the ground plane accurately defines the line impedances, provides low impedance current path for the ground supply and convenient decoupling for the other rails.

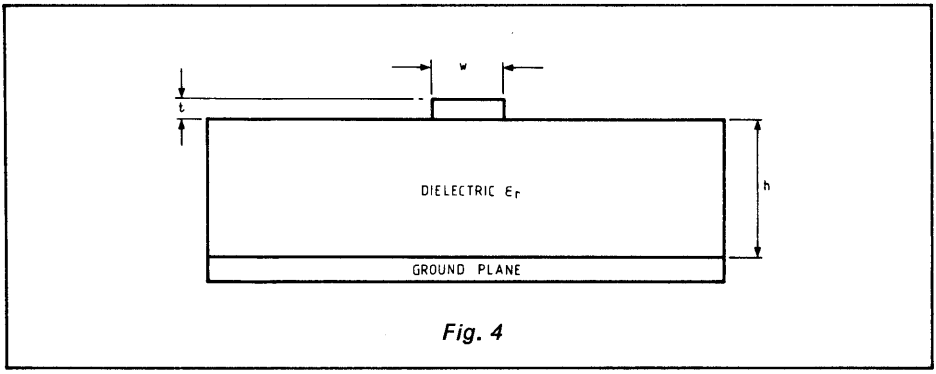


Fig. 4

The characteristic impedance, Zo, of a microstrip line is

$$Zo = \frac{87}{\sqrt{\xi r + 1.41}} \ell n \left(\frac{5.98\ h}{0.8\ w + t} \right)$$

r = relative dielectric constant of the board, typically r = 5 for glass-epoxy.

w, h and t are defined on Fig. 4.

Standard tables and graphs are available in the literature on microstrip to calculate the line width needed for a given Zo (Fig. 5).

In practice, line impedances greater than about 150 ohms are not realisable in the copper-glass-epoxy system.

The technology of microstrip board is relatively straightforward and follows good printed circuit board practice. The use of double-sided board is strongly recommended.

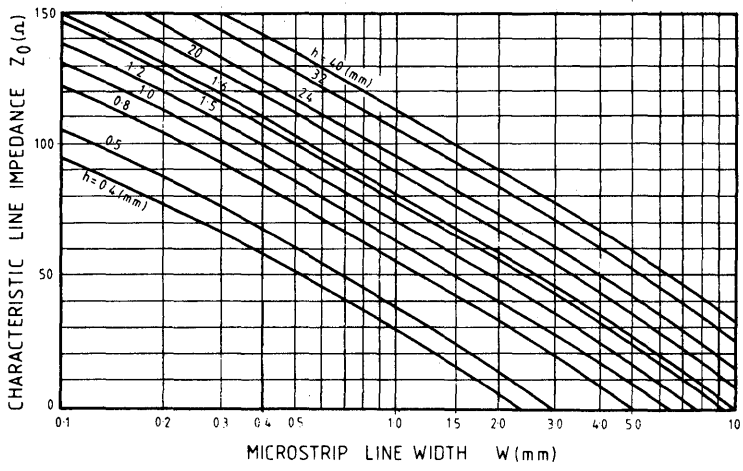


Fig. 5 Characteristic line impedance as a function of the line width for microstrip lines (Parameter is board thickness h(mm) $\xi r = 5$, $t = 35\mu$)

The choice of board thickness and specification depends primarily on the application; best results are obtained with good quality board of reproducible characteristics. The capacitance per unit length of conductor is predictable from modified parallel-plate capacitor formulae; in practice, the graph of Fig. 6 is a good guide. Variations in dielectric constant of the board change Zo in the ratio of about $\pm 2\%$ in Zo for $\pm 5\%$ in ξr.

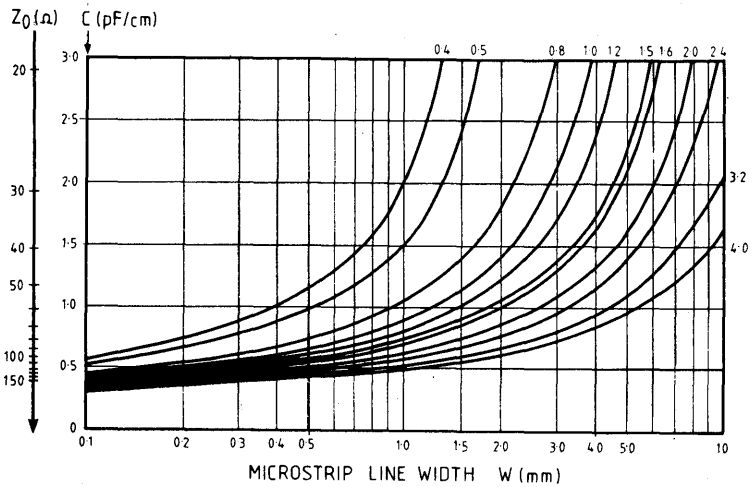


Fig. 6 Intrinsic line capacitance as a function of line width for microstrip lines. (parameter is board thickness $\xi r = 5$, $t = 35\mu$)

The inductance per unit length of the line may be calculated from the formula:

$$Lo = Zo^2 . Co$$

where Zo = characteristic impedance
Co = capacitance per unit length

The propagation delay of the line is approximately

$$t_{pd} = 3.3 \times 10^{-2} . \sqrt{0.475 \xi r + 0.67} \text{ ns/cm}$$

Most glass-epoxy board has $\xi r \simeq 5$, so $t_{pd} = 0.05\xi$ ns/cm. The relationship between t_{pd} and ξr is illustrated in Fig. 7.

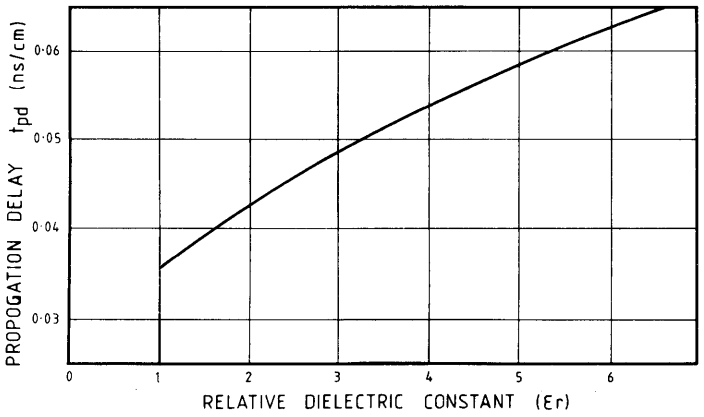


Fig. 7 Propagation delay as a function of the relative dielectric constant of the board material for microstrip lines

Line loading

Most devices connected to the microstrip load the lines capacitively. In some cases, such as logic inputs, there is only a single load capacitance on a relatively long line, and the effect can be ignored. On parallel outputs, especially where settling times are important, the effect of loading on the line must be compensated for. Basically, this means that the total load capacitance per unit length of line must be calculated and then the line designed in such a way that the loaded impedance matches the actual working impedance desired. Load capacitance per device is taken from the manufacturer's data or by measurement from the devices.

A fairly accurate assessment of the inter-device spacing is needed, and the types of device must be considered. Eventually, some figure of C_D, the

load capacitance per unit line length, can be derived. The standard equation for loaded lines is

$$Zo = \frac{Zo'}{\sqrt{1 + \frac{C_D}{Co}}}$$

where Zo′ is the characteristic unloaded impedance
Zo is the loaded impedance
C_D is the load capacitance in pF/cm
Co is the line capacitance in pF/cm

Tables and graphs for this function are shown in Fig. 8.

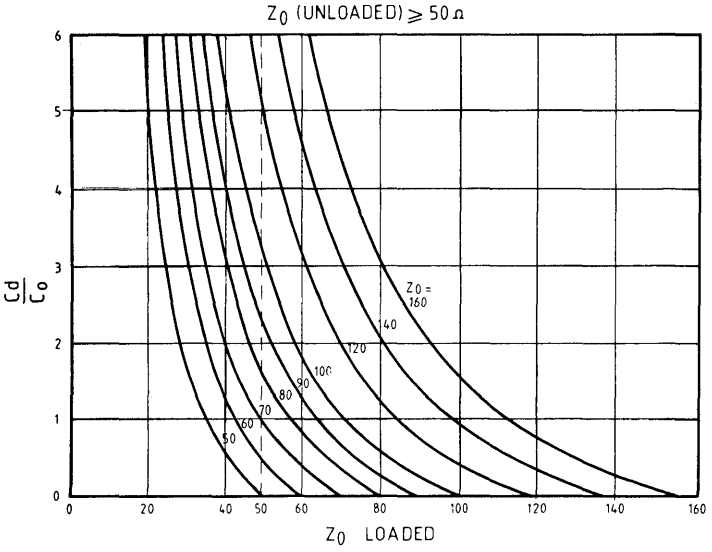


Fig. 8

Tables and graphs for this function are shown in Fig. 8.

Loading in most systems is distributed, in the way described, along the lines but, in reality, does represent discrete 'lumps' of capacitance at finite points, and so any compensation scheme cannot be perfect, but practical systems if well-designed show minimal line impedance disturbance. Of course, the propagation delay is increased by capacitive loading, in the ratio

$$t_{pd} = t'_{pd} \sqrt{1 + \frac{C_D}{C_O}}$$

where t_{pd} = final delay
t'_{pd} = delay of unloaded transmission line

This function is illustrated in Fig. 9.

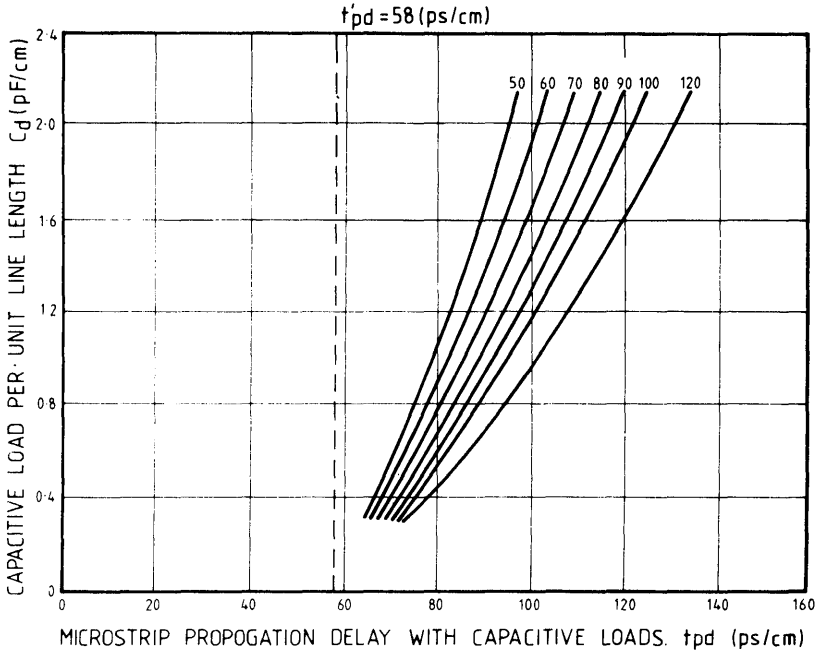


Fig. 9 Variation of the propagation delay line of a microstrip line as a function of the capacitive load per unit length. $\xi r = 5$, Parameter is Z_o

ECL IN ANALOGUE TO DIGITAL CONVERTER SYSTEMS

Plessey A-D products are ECL compatible in terms of input and output logic levels. If full use is to be made of the advantages of ECL, proper transmission line design rules must be observed. Fig. 10 shows a simple line with driver and load. Initially, we assume that the line delay is appreciably longer than the rise and fall times, so that reflections occur at full amplitude. The output voltage swing at point A is a function of the internal device voltage swing, the output impedance, and the line impedance

$$V_A = V_{INT} \times \frac{Zo}{Ro + Zo}$$

Normally, Ro is small, so $V_A \simeq V_{INT}$.

This signal arrives at point B after time t. The voltage reflection coefficient at the distant end of the line is ρL, which is given by the formula

$$\rho L = \frac{R_L - Zo}{R_L + Zo}$$

If $R_L = Zo$ there is no reflection; even if R_L is an approximation to Zo, the reflections will not be large, as a 1% change in R_L changes ρL by only 0.5%.

When a reflection occurs, however, it will return to A, arriving at a time 2t, and be reflected with a reflection coefficient

$$\rho S = \frac{Ro - Zo}{Ro + Zo}$$

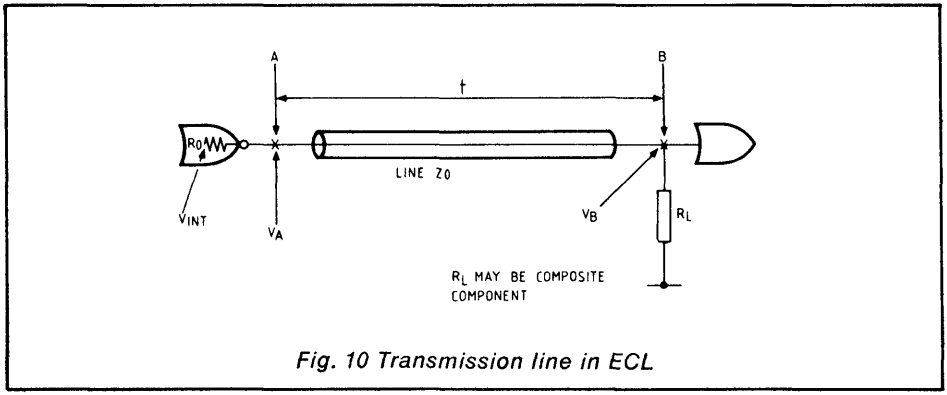


Fig. 10 Transmission line in ECL

In the worst case conditions, the signal will suffer many reflections of significant amplitude; clearly this is not permissible, as it represents 'ringing' on the line. In ECL practice, ringing should be maintained below 15% under-maintained for short runs; Table 1 illustrates the maximum lengths allowed, assuming 20%–80% rise/fall times of 3ns.

Line impedance	Fanout			
	1	2	4	8
50	21.1	19.1	17.0	14.5
68	17.8	15.7	12.7	10.2
75	17.5	15.0	11.7	9.1
82	16.8	14.5	10.7	8.4
90	16.5	13.7	9.9	7.6
100	16.0	13.0	9.1	6.6

Permissible unterminated line lengths (cm)

Table 1

The simplest termination scheme is shown in Fig. 11a. Since the input impedance of ECL parts is relatively high, R_L is made equal to Zo. Then $\rho L = 0$ and the voltage on the line is the full ECL swing. In large systems, this technique is used extensively but has the disadvantage of requiring a —2 volt rail in addition to the normal supply. Fig. 11b shows a convenient realisation of the same circuit using 0 and —5.2 volt rails only. With parallel terminated lines, the load provides the pulldown for the driving device. This termination is the fastest form for ECL. The full amplitude signal is progapated down the line, undistorted and, as $\rho L \simeq 0$, overshoot and ringing are practically eliminated. The Thevenin form (Fig. 11b) is fully equivalent to the system of Fig. 11a but operates on more convenient power rails. Clearly, the parallel combination

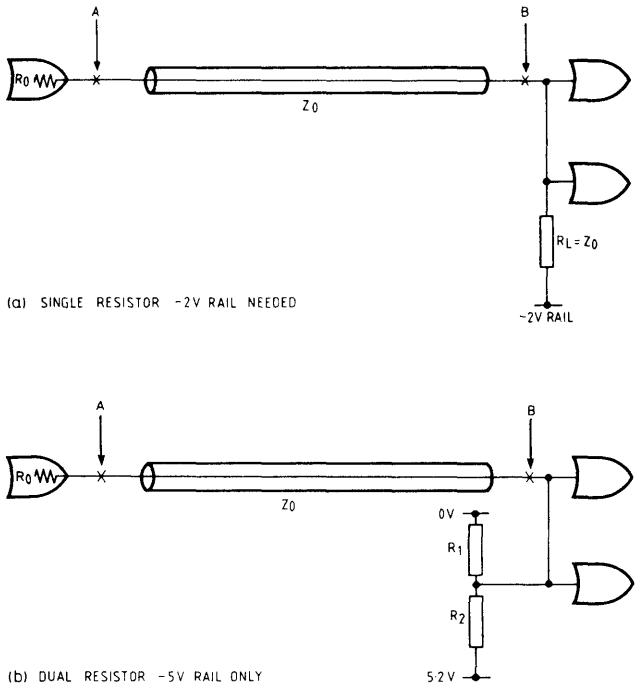


Fig. 11 Terminated line parallel termination
(a) Single resistor —2V rail needed
(b) Dual resistor —5V rail only

of R_1 and R_2 must be equal to Zo, while the defined voltage at the input must be the —2v used in Fig. 11a (when the driver output is 'low'). These conditions lead to:

$$\text{for } Z_0 = 50\Omega$$
$$R_1 = 81\Omega$$
$$\text{and } R_2 = 130\Omega$$

General results are given in Fig. 12.

When driving a large fanout, loads may be distributed along the full length of a parallel terminated line, although only a single line is permissible at 50Ω.

The other major form of line termination is the series system (Fig. 13). Reflections are eliminated at the driving end of the line by making

$$R_S + R_O = Z_O$$

The reflection coefficient of the load is —1.

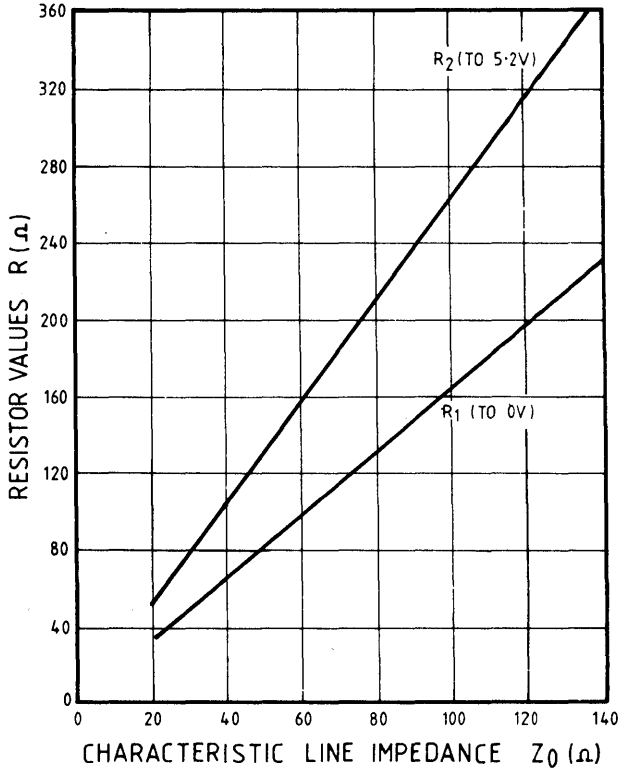


Fig. 12 Thevenin equivalent resistors for parallel line-termination

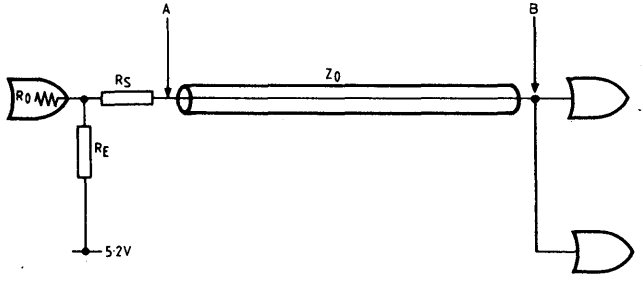


Fig. 13 Series termination

This represents a 100% reflection at the load end of the line. As the propagated signal is of only half amplitude, the 180° phase change at the load interface is essential to provide the full logic swing at this point.

Typically, R_O for ECL10k devices is 7Ω, so in 50Ω systems, $R_S = 43\Omega$. R_E is fanout dependent, and is given by

$$R_{EMAX} = \frac{10Zo - Rs}{n} \text{ where } n = \text{fanout.}$$

The advantage of series termination is in simplicity, both in configuration and power supplies. Disdavantages are that distributed loading is not permissible, although lumped loading at the line end is satisfactory.

Voltage drops across Rs limit loading to less than 10. However, multiple Zo lines, with separate Rs resistors may be used. Overall slower propagation delay in series terminated mode may be a disadvantage, partly overcome by multiple transmission lines. This leads to the final line termination form, Fig. 14.

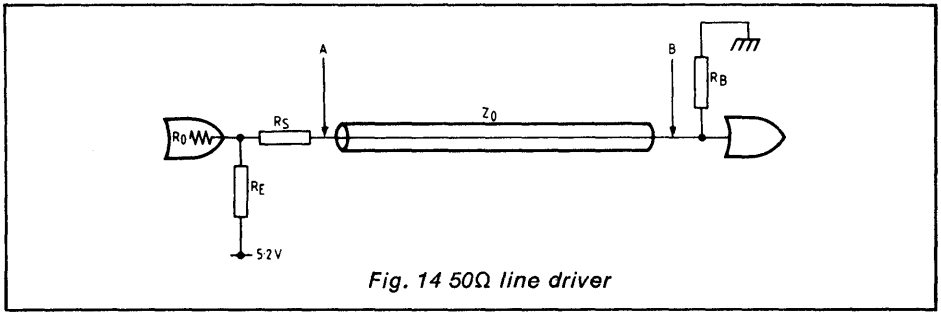


Fig. 14 50Ω line driver

It can be seen from Fig. 14 that the driver is doubly terminated, and resembles both series and parallel systems. At the distant (B) end of the line,

$$R_B = Zo$$

so there is no reflection.

At the driving end, Rs acts as a series damping resistor, and, although it is not generally possible to accurately match Zo at this point, any residual reflections on the line are further attenuated. The chief advantage of this scheme is the ability to drive a 50 ohm line terminated directly to ground, while using the conventional 0V and —5.2V supplies. Another advantage is the ability to drive long lines with low reflections; the disadvantage is that the effect of Rs and R_B is to reduce the signal amplitude on the line; the device at B should be some form of line receiver or comparator.

At the driving device output, the 'low' level must be pulled down to —2 volts. Therefore

$$\frac{Rs + R_B}{Rs + R_E + R_B} = \frac{2}{5.2}$$

and $R_B = Zo$ (usually 50Ω for output line driving)
and R_E may be set within limits, arbitrarily, to provide an adequate 'pull-down' current.

Convenient practical values are

$$\left.\begin{aligned} R_B &= 50\Omega \\ R_S &= 27\Omega \\ R_E &= 130\Omega \end{aligned}\right\} \text{ Nearest preferred values.}$$

Further information can be obtained from ECL data and applications handbooks.

A TYPICAL SYSTEM

Modern equipment practice is heavily weighted in favour of 50Ω systems, and in key items such as coaxial cable and connectors it may not be easy to procure a wide range of alternatives. In this environment, where board-to-board, or board-to-external facility connections are used, coaxial 50Ω design is strongly advised. On an individual board, interconnection at 50Ω is commonly used for analogue lines, although digital signals may be conveniently operated at higher impedances. For the ultimate in performance, however, 50Ω (loaded) systems are preferred.

System design demands a range of component blocks with, desirably, a high state of integration. However, two circuit blocks currently not economically available in integrated form are the buffer amplifier and the sample-and-hold. Typical applications of the buffer amplifier are high speed driving of 50Ω analogue lines, DAC output buffering, and sample-and-hold buffering. A commercially available hybrid buffer amplifier (LH0063) has been used with success. Discrete buffer amplifiers can be constructed, the main parameters being slew rate and phase distortion. The ability to drive 50Ω lines is essential.

A sample-and-hold is needed in those video systems where the aperture time must be short compared with the time taken for the A-D to perform the conversion. Typical examples are systems where series-parallel type converters are used; an input analogue sample-and-hold is essential, as the LSB's are encoded some time after the MSB's. Fully parallel analogue to digital converters can operate without sample-and-hold; this is sometimes known as 'sampling-on-the-fly'. In this case, the parallel converter, by virtue of its latch action, performs an effective sample-and-hold function on the digital output word.

One measure of a sample-and-hold 'quality' is the aperture time, which is the uncertainty in the time at which the sample is taken. The best analogue sample-and-holds have $t_{aperture} = 20$ ps rms. Digital sample and holds are more difficult to measure, but should be approaching this figure. The aperture time requirement of a sample-and-hold is calculated from the maximum input slew rate and the accuracy required. If the maximum input frequency is f, and the number of bits is n, then:–

$$t_{aperture} < \frac{1}{2^{n+1}.\pi.f.}$$

In an 8-bit system, if the input bandwidth is 10 MHz, and therefore the sample rate > 20 MHz, the required aperture time is calculated to be 62 ps or better.

Current analogue high speed sample-and-hold circuit design is discrete, using a ring of Schottky diodes for fast switching, usually transformer driven, The basic circuit is shown in Fig.15, A long tailed pair of very fast transistors is driven by a narrow ECL-derived pulse.

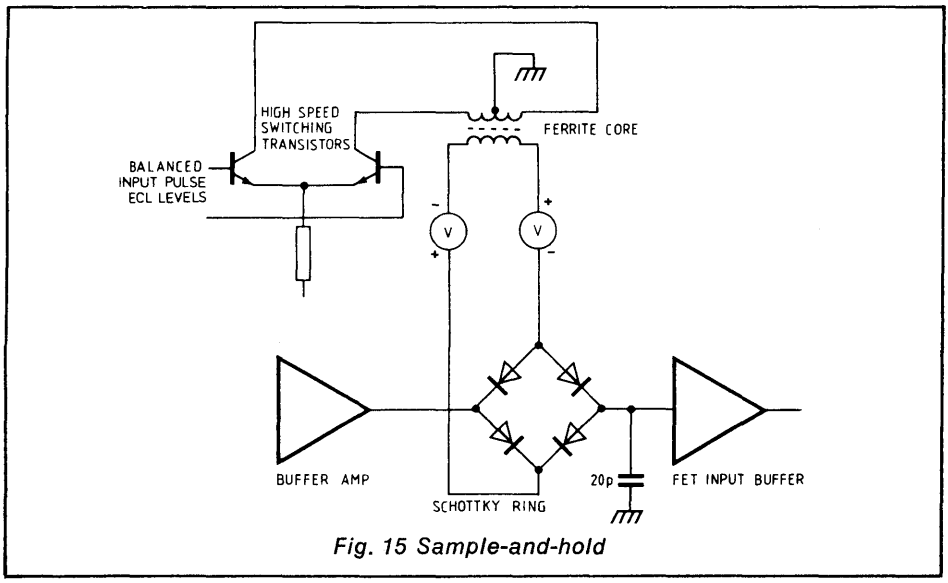


Fig. 15 Sample-and-hold

Normally, the diode ring is biased 'off' but, during the pulse, a relatively large forward current, of the order of 20–30 mA, is driven through the ring. The 'hold' capacitor charges to the voltage present at the output of the driver stage. After the pulse, the only discharge paths for the capacitor are the internal leakage, the diode ring reverse leakage, and the input current of the buffer amplifier. Low discharge rates imply low 'droop' of the signal output from the buffer amplifier; an FET input for the buffer is usually necessary. An advantage of this type of circuit is the full balance, which tends to cancel out feedthrough of the sampling pulse. The limiting factors are the time taken for the input pulse to switch the diodes, the parasitic capacitances of the diodes, and the finite input current and bandwidth of the buffer amplifier.

Digital sample-and-hold facilities are sometimes provided in all-parallel converters, by supplying a latch signal to all comparator stages in precise synchronism with the input analogue voltage. This means that the propagation delays of the lines must be accurately designed. When properly designed, digital sample-and-hold will compare favourably in aperture time with the best analogue circuits, and have the additional advantage of an indefinitely long 'hold' time, making them ideal for fast sample, long hold applications.

Testing the assembled system

The usual test instrument for high speed A-D systems is the oscilloscope, either real-time or sampling. Certainly, the oscilloscope display will illustrate whether the device is operating, and give some idea of the accuracy, limited to about six bits or so in dynamic range by the on-screen resolution. A fast D to A converter can help in A-D projects by reconverting the digital output so the difference between signals can be examined, either in the analogue mode by D-A converting the A-D output, or digitally, by D-A converting a digital input and reconverting in the A-D. In either case, the permissible error function is relatively easily described and is amenable to calculation.

The A-D and D-A test method was applied to a 5-bit A-D converter with the results shown in Figs. 16 and 17. The first of these shows the digitising of a 300 kHz ramp to 5 bits resolution; there are no missing codes and no significant glitches. Sampling near the Nyquist rate is shown in Fig. 17. The technique here is to set up for a small difference frequency between the input signal and half the clock frequency. The oscilloscope timebase is set to a relatively low sweep rate, and the output waveform observed is the 'beat' frequency between the input and half the clock rate. If the clock were to be set at precisely twice the input frequency, the display would consist of only two sample points per cycle of the input, positioned according to the phase separation between the input and the clock. With a small difference in frequency, successive conversions produce an output waveform in a manner similar to a sampling oscilloscope.

No sample-and-hold was used on the A-D; the on-chip latches proved satisfactory to a clock rate of 125 MHz.

One of the major problems in practical systems is ripples caused by reflections. A useful tool in checking line impedances is the time domain reflectometer; accuracies of 1% in line impedance measurement can be made, and line discontinuities are detected as distances in physical dimensions, so positive location is possible. Redesign of the defective components may significantly help the overall system performance.

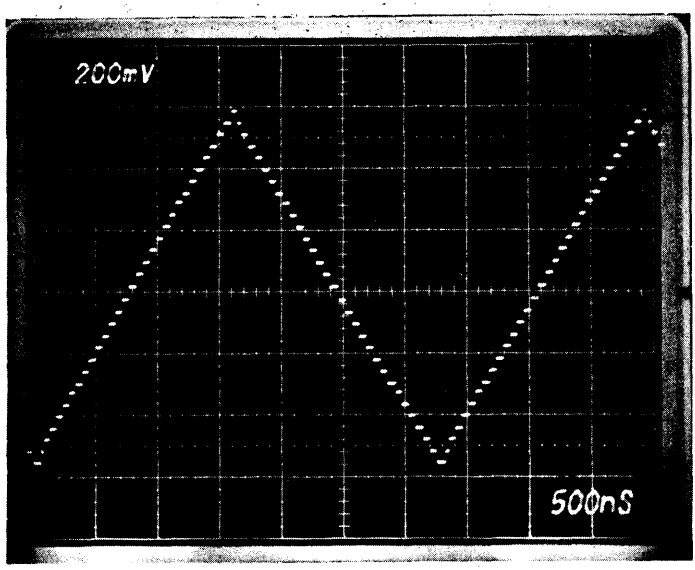


Fig. 16

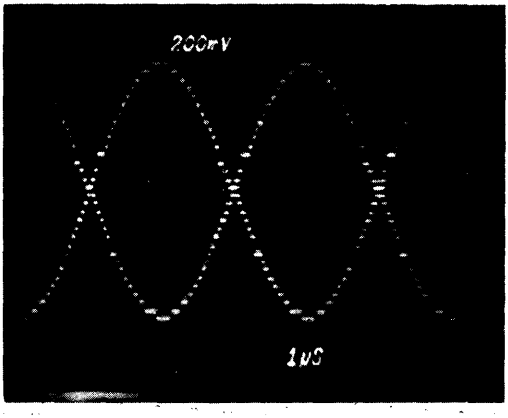


Fig. 17

3 The SP9750 comparator

GENERAL DESCRIPTION

The SP9750 is a high speed comparator tailored to the needs of the parallel/series type of converter described in Section 1.

Its most important features are:

1. The response is faster than other commercially available comparators

2. Integrated onto the comparator chip are additional features relevant to the construction of fast A-D converters.

The addition of the extra features on to the comparator not only reduces the system cost and complexity but also allows higher performance systems to be built.

Using the low gain principle already discussed, the comparator design could follow the latest high frequency amplifier practice. Fig. 18 shows the schematic diagram of the comparator section of the SP9750. It consists of a

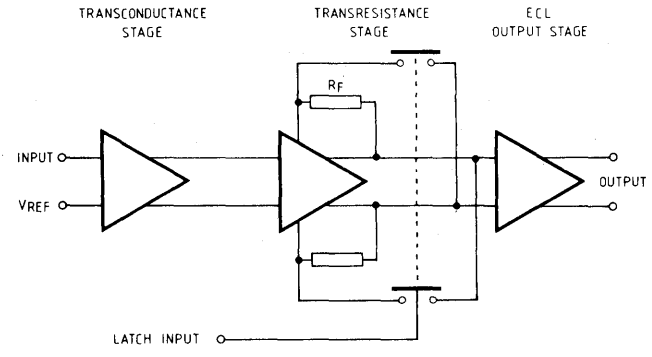


Fig. 18 Schematic diagram of the comparator section of SP9750

mutual conductance or "gm" stage, a trans-resistance second stage, finally feeding an ECL logic output stage. The trans-resistance stage is a shunt feedback amplifier in which the transfer resistance is approximately equal to the feedback resistor value. The input impedance of this stage is low and so the effect of shunt capacitance on this point is minimised. Output impedance is also low giving similar advantages. The resulting circuit has a 300MHz bandwidth in the sample mode and can acquire an input signal change in 2ns. The input offset voltage is ±5mV and the resolution is 1mV, i.e. ±0.5mV.

In the design of very high speed converters, the propagation delays between IC packages have a strong influence on the maximum conversion speed attainable. By including additional system functions on the comparator chip these are minimised, and the bonus of a lower package count and lower power dissipation also ensues. The following four functions are available:

1. A two-input gate
2. Four emitter follower outputs from (1) for wired "OR" decoding
3. A precision current source set by an external resistor
4. A high speed precision switch for (3)

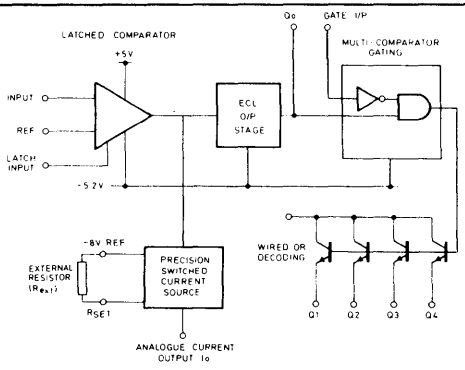


Fig. 19 SP9750 complete schematic diagram

These are shown in block form in Fig. 19. Fig. 20 shows how fifteen SP9750s can be interconnected in a four-bit converter stage. The comparators are connected to form a four-bit all-parallel ADC similar to Fig. 1. The two input gates decode the comparator outputs by detecting the highest level comparator with a logic '1' at the output. The gate at this level puts out a unique '1' to the four emitter followers which can be wired "OR" connected to give a four-bit binary code. Also shown in the diagram is the function of the precision current output. These currents, which are equally weighted for all comparators, turn on when the comparator input is above the reference voltage. Therefore by summing all of these currents, an analogue reconstruction of the input signal to the nearest four bits below the input is obtained. Only fifteen comparators are required to construct a 4-bit ADC and a 4-bit DAC. Such a stage can be used as the MSB stage of a parallel/series type converter. The temperature compensation of the current output is sufficient to allow its use in converters of at least eight-bit accuracy. Similar stages can form the LSB stage of a parallel/series system, only in this case the current output would not be used.

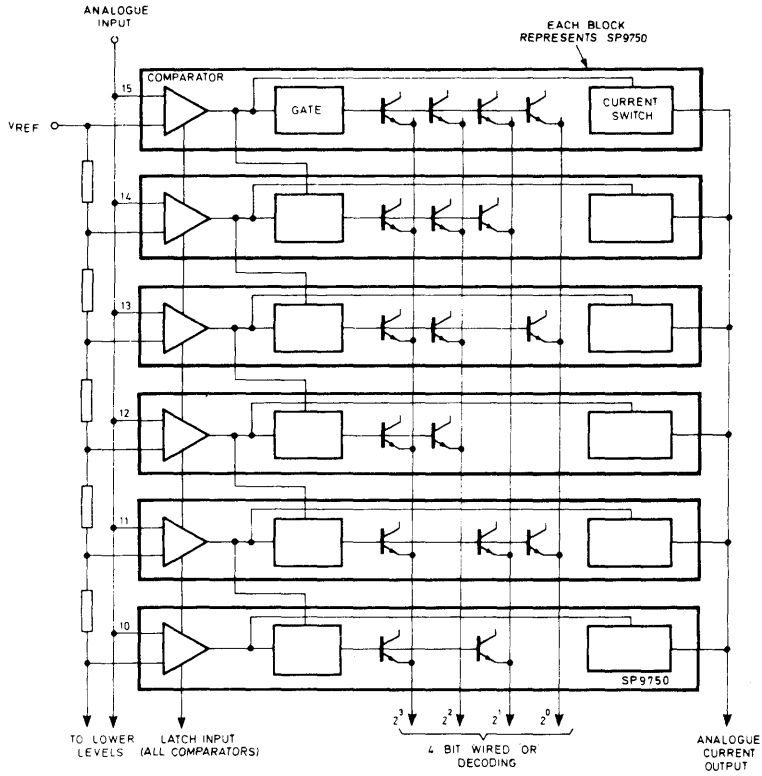


Fig. 20 A 4-bit converter using SP9750 showing the top 6 levels only

The SP9750 has been optimised for use in a four by four bit parallel/series converter system, but it is by no means limited in its application. It is not only being designed into a variety of other systems, but also its extremely fast response has found it a place in such areas as fast pulse detection and instrumentation.

Circuit description

Fig. 21 shows the complete circuit diagram of the SP9750. The inputs are buffered with emitter followers to avoid the switching effect of input currents which would exist with a direct connection to the long-tailed pair first stage. The diodes in the collectors of the first stage are for DC level shifting. The DC conditions are arranged so that for a perfectly matched circuit with the inputs shorted together, there is zero voltage across the feedback resistors (R_f).

The output from the second stage which is a swing of about 400mV is fed into the current switch via an attenuator. This direct route to the current switch gives the fastest possible D to A function. The attenuator avoids using excessive drive to the switch which would increase the settling time of the analogue current output. The analogue current source transistor uses a novel connection of transistors which minimises the effect of temperature and Hfe etc, on the output current stability.

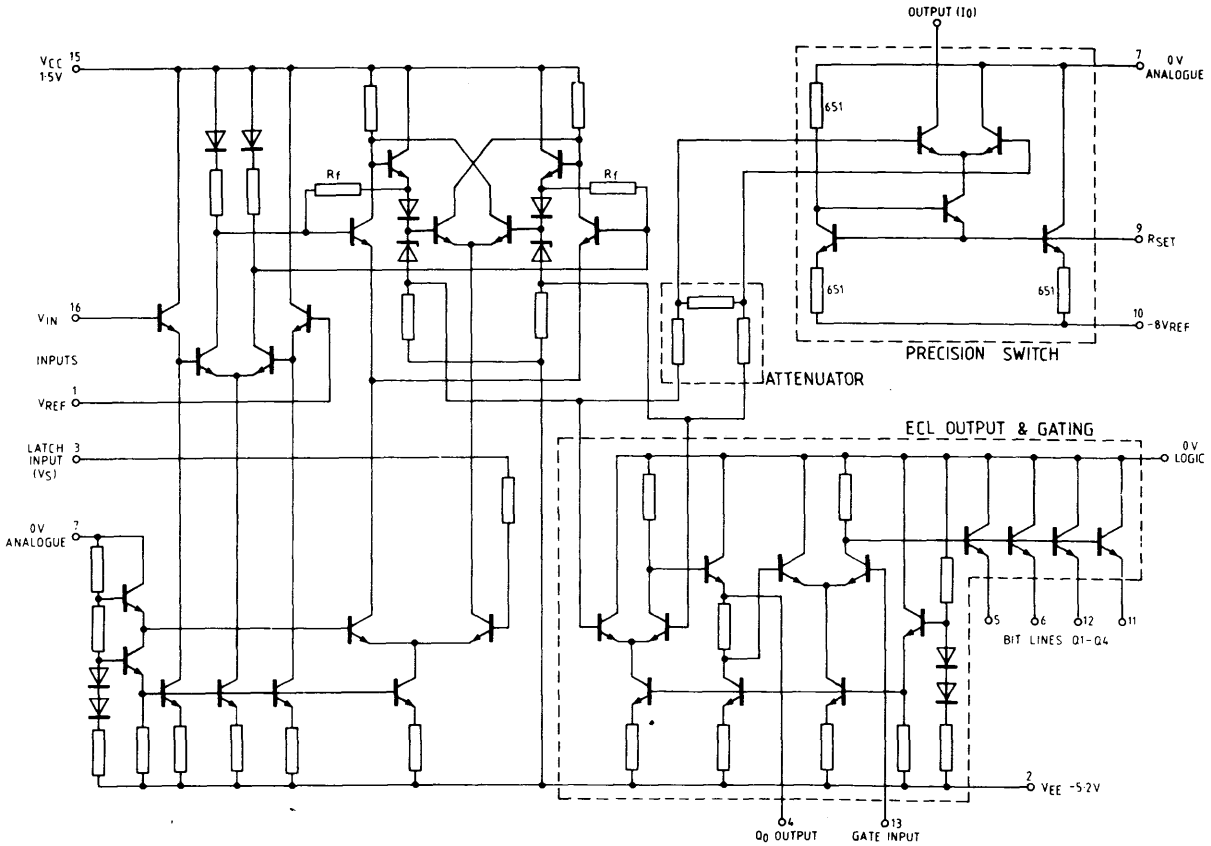

OUTPUT (IO)
VCC 15
1·5V
7
0V
ANALOGUE
651
Rf
Rf
9
RSET
651
651
10
-8VREF
PRECISION SWITCH
VIN 16
INPUTS
ATTENUATOR
VREF 1
ECL OUTPUT & GATING
LATCH 3
INPUT
(VS)
0V
LOGIC
0V 7
ANALOGUE
5
6
12
11
BIT LINES Q1-Q4
2
VEE -5·2V
4
Q0 OUTPUT
13
GATE INPUT

Fig. 21

The ECL output stage is conventional but an unusual circuit is used to provide the comparator output gating. The Boolean function required is: gate output = $\bar{A}B$, which might be described as a partial exclusive 'OR' function. It is achieved by level shifting the B input by one half of an ECL output voltage swing, and feeding this into a single ECL gate structure. This circuit uses minimal chip area. Four emitter follower outputs from the gate are provided which can be wire OR-ed as previously described.

Conversion rate/Hardware tradeoffs

An 'n' bit converter can be arranged in a number of ways using parallel and series parallel techniques. For example, three stages could be used, each resolving some of the bits.

$$\text{i.e.} \quad a + b + c = n$$

In an 'a' bits conversion, the number of comparators needed is $(2^a - 1)$. Thus the total number of comparators is:–

$$(2^a - 1) + (2^b - 1) + (2^c - 1)$$

In some circumstances, under and over-ranging may be needed, which will require two extra comparators.

Typical examples are the 4 × 4, two stage converter for eight bits, where:–

$$a + b = n$$
$$4 + 4 = 8$$

Number of comparators $= 2^4 + 2^4 - 2 = 30$

When stages are cascaded in this way, the interstage delay must be taken into account. Of primary interest is the D/A current output settling to the desired accuracy.

Each SP9750 contributes one fifteenth of the full scale current, and only one or two comparators are likely to be in a critical settling condition when the latch closes. Therefore if settling to $\frac{1}{2}$ LSB is required (0.2%) two comparators need to settle to 3% or 1.5% for individual comparators. This takes place in less than 10ns. Allowing 10ns for the interstage difference amplifier to settle and a further 10ns for the sample and hold function and logic timing errors, the total conversion period is 30ns or a sampling rate of 33MHz. The corresponding figure for 3 stage is 20–25MHz.

Improved circuit design techniques would increase these figures. For instance, analogue delay could be used between stages to equalise the settling delay of the D/A current output. Perfect cancellation would reduce the conversion period by 10ns bringing the sampling rate to 50MHz. Another technique which has been used is additional comparators in the second or subsequent stage to correct errors from the first stage brought about by latching the first stage before the sample and hold has fully settled. The improved performance offered by such circuit innovations is traded against increased circuit complexity and hence cost.

D TO A CONVERTER USING THE SP9750

When used as originally intended, in a 4 × 4 parallel-series ADC, the output currents from the first four bits of conversion are summed to produce the interstage digital-to-analog function. It is this D-A facility which is used here, but with a binary weighting for the output currents instead of the equal weighting of the A-D system.

A total of 'n' devices only are needed for the 'n' bit conversion, unless the MSB current needed is more than 10mA. If, say, 20mA MSB current is needed, two devices will run in parallel, as in the scheme to be described, giving a total of 'n + 1' devices. The D-A system block diagram is Fig. 22.

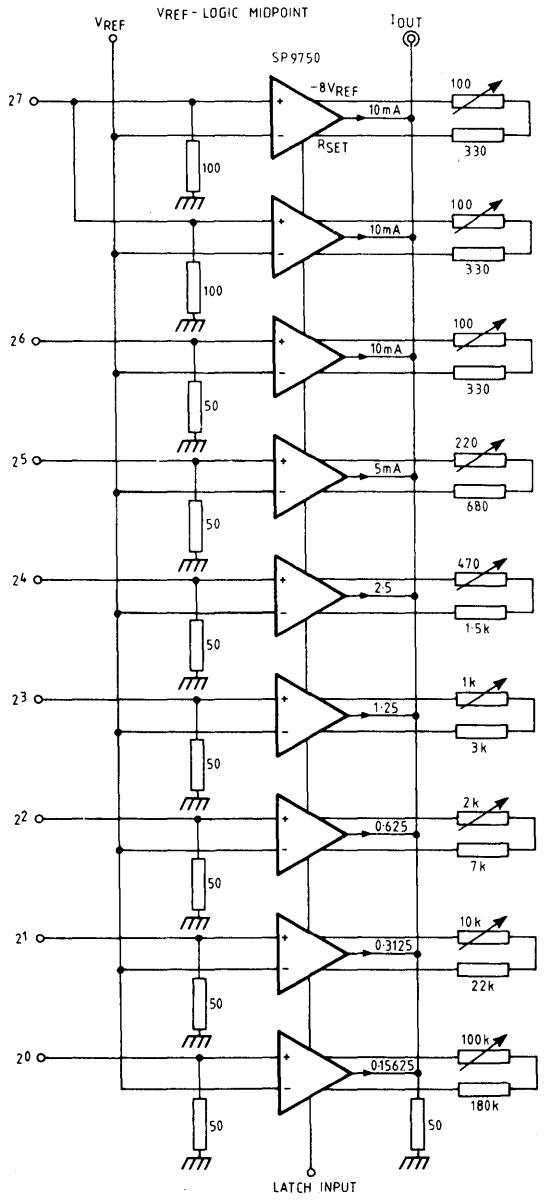


Fig. 22 8-bit DAC using SP9750s

In the D-A application, the 'analog' inputs are switched by logic signals from the 'n' bits of incoming data, giving a marginal improvement in the operating speed compared with normal analog operation. The ancillary facilities ($Q_0 - Q_4$ outputs) which are used in the ADC encoding matrix are not used in the DAC. The SP9750 incorporates a latch, as is becoming standard in high speed comparators, and this feature is exploited here to provide a fast digital sample-and-hold. The current output settling time (10ns to 0.2% for the SP9750) is the main limiting factor in this type of DAC; eight-bit accuracy should be available in about 10–15ns from the input command.

The comparator has a maximum input current of 25μA, which allows it to be set up to receive logic input swings (ECL or TTL) by connecting the reference input to the appropriate voltage. The ECL input to the latch stage is made low for follow or high for hold.

The output current is set by an external resistor and the —8 volt rail, which should be stable enough for the accuracy needed. The maximum output current from a single device should not be much more than 10mA; the relationship of output current to negative reference rail is nominally

$$I_{out} = \frac{V_{rail}}{2 \times R_{ext}}$$

In practice, deviations from this rule are found at low output currents, due to on-chip bias conditions, and a table has been drawn up (Table 2) which illustrates the values of R_{ext} for given output currents.

Output current (mA)	Tail resistor (R_{ext})	
	Fixed	Variable
(mA)	(Ω)	(Ω)
10	330	100
5	680	220
2.5	1.5k	470
1.25	3k	1k
0.625	7.5k	2.2k
0.312	22k	10k
0.156	180k	100k

Table 2

System Aspects

The most used type of high-speed DAC is probably the eight-bit system, so the description here is for eight bits, with an MSB of 20mA, which requires two SP9750s in parallel. No problems are encountered in parallel device operation. The total of nine comparators are laid out in a U-shaped configuration on $\frac{1}{16}''$ PCB with a top surface ground plane. The design value for the transmission line signal paths is 50Ω, enabling the DAC to directly drive 50Ω systems, or the 50Ω input of a fast real time or sampling scope. The option of terminating the board end of the transmission line or leaving it open is available. The latter case provides a full-scale swing of 2 volts (40mA into 50Ω) while termination of the line on the PCB halves the output voltage swing by giving an effective 25Ω load, but gives better settling time by reducing reflections on the summing line.

The device input capacitance is small, and 50Ω nominal lines are used with 50Ω terminations. The two MSB devices are fed through 100Ω lines with 100Ω terminations in parallel. Drive from ECL matched to 50Ω by terminating networks optimises the switching speed, although TTL-level (LS or S) is also possible by resetting the V_{ref} inputs rail to a mid-level point.

On the output current summing line, the typical output capacitance per device is 2pF. The line is fed from both sides, so an unloaded line impedance of 110Ω is predicted for the 50Ω loaded condition. All input lines are made of equal lengths, although some advantage may be gained by equalising the input to output delays; in either case, the MSB should be located furthest from the output connector and as close as possible to the end termination of the line.

Testing the DAC

Each comparator is configured as in Fig. 23 and the potentiometers have to be 'set up' to provide eight-bit accuracy. There are two ways to do this: either DC, using a DVM and setting each current independently of the others or dynamically, driving the inputs with a digital code. The dynamic method provides 'hands-on' practical feel for the DAC operation at high speed, and is recommended if a fast real time scope is available. A simple drive circuit uses two ECL10k Hexadecimal counters (MC10136s) in synchronous count mode, overflowing at the 256 count. For the eight-bit converter, this gives a

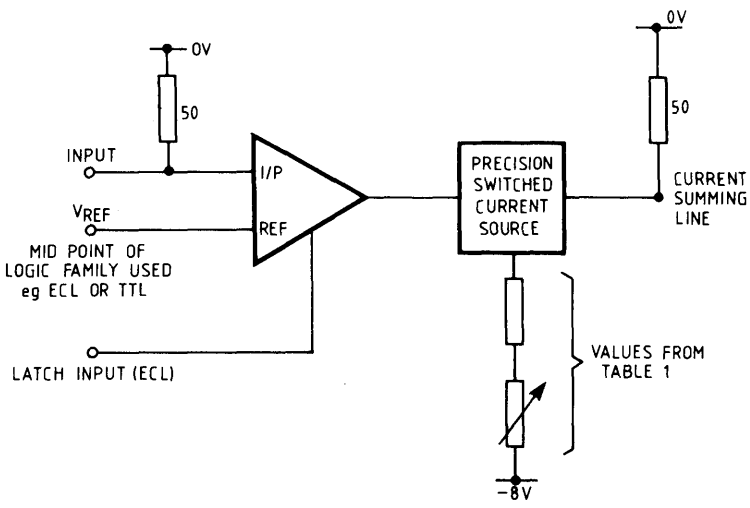


Fig. 23 Comparator configuration

full-scale ramp output, which is easily trimmed for linearity. The system diagram is shown in Fig. 24. Nominal MSB is 20mA, bit 7 is 10mA and so on down. A small overall scaling error can be trimmed out using the —8 volt rail. Independent setting of the current sources instead of the conventional R-2R ladder improves speed performance and prevents interaction between sources.

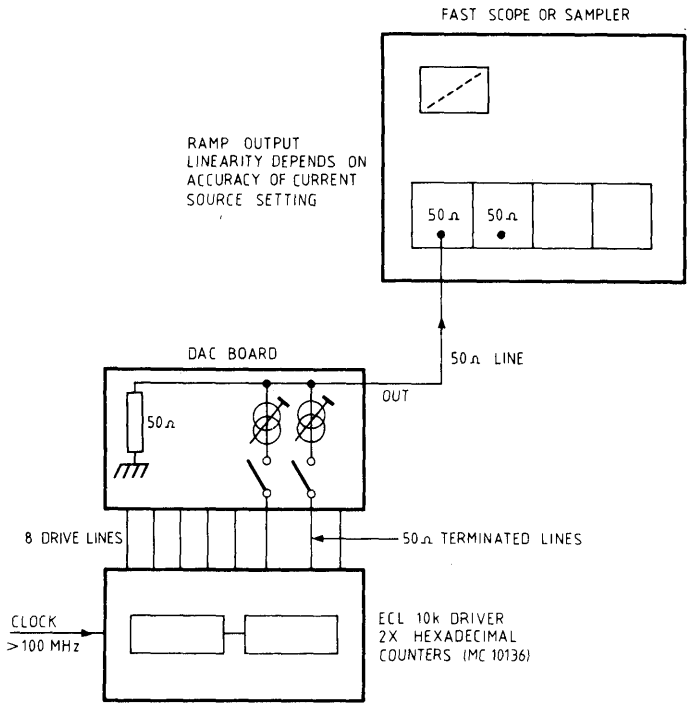


Fig. 24 Setting up the DAC

Fig. 25 shows the full-scale ramp maintaining linearity at more than 50MHz input to the LSB. The full-scale transition (Fig. 26) at the end of the ramp, takes less than 15ns, dominated of course by the MSB transition, shown clocked at about 14MHz in Fig. 27.

The limiting factor in the DAC testing is the ECL10k drivers; output glitches are seen at the MSB transition (0111 1111 to 1000 0000) and at the lower counter full transition (0000 1111 to 0001 0000); these are attributed to timing errors caused by internal 'counter full' to 'carry out' delay. The manufacturer's figures put this at 5ns, although the glitches seen are shorter, about 3ns overall. The minimum clock period accepted by the counters is 9ns so the DAC LSB state changes occur at this interval, comparable to the I_{out} settling time of the SP9750 (typically 10ns to 0.2%) indicating a maximum data rate of more than 50MHz.

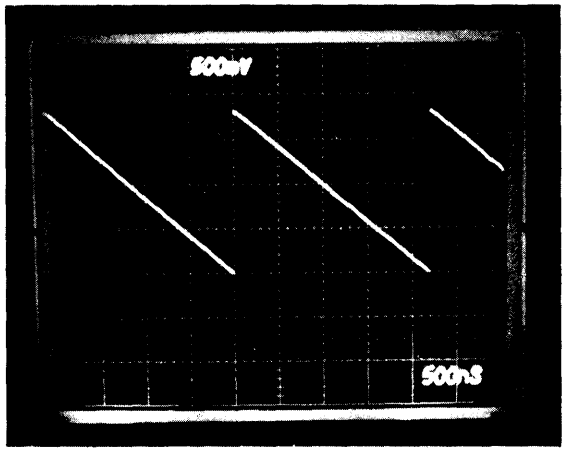


Fig. 25

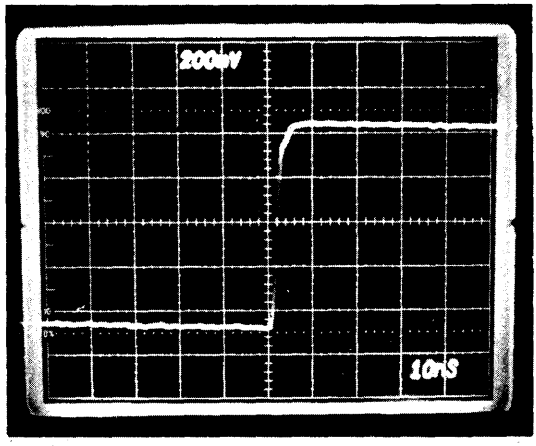


Fig. 26

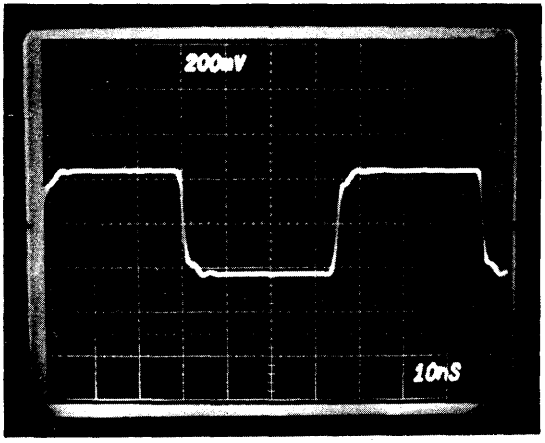


Fig. 27

4 The SP9685 comparator

GENERAL DESCRIPTION

The SP9685 is a high speed latched comparator, the circuit diagram for which is shown in Fig. 28. The unlatched gain is approximately 50dB at frequencies up to over 200MHz. The main differences between the SP9685 and the SP9750 are as follows:–

1. The SP9685 is a simple comparator and does not include the gates and precision current sources of the SP9750.
2. The unlatched gain of the SP9685 is greater than that of the SP9750.
3. The latch enable control of the SP9685 has the opposite phase of operation to that of the SP9750 latch control.
4. Two gain stages follow the latch of the SP9685 whereas only one is used on the SP9750.
5. Q and $\bar{Q}$ outputs are provided on the SP9685.

Short pulse detector

This simple circuit for the SP9685 has applications in nucleonics and high energy physics. In its simplest form, the circuit is shown in Fig. 29.

A positive going pulse of any width, down to the minimum defined by the propagation delay plus the setup time, and of any height between the maximum common mode signal and the minimum overdrive that will reliably switch the comparator can be quickly detected and will cause the circuit to

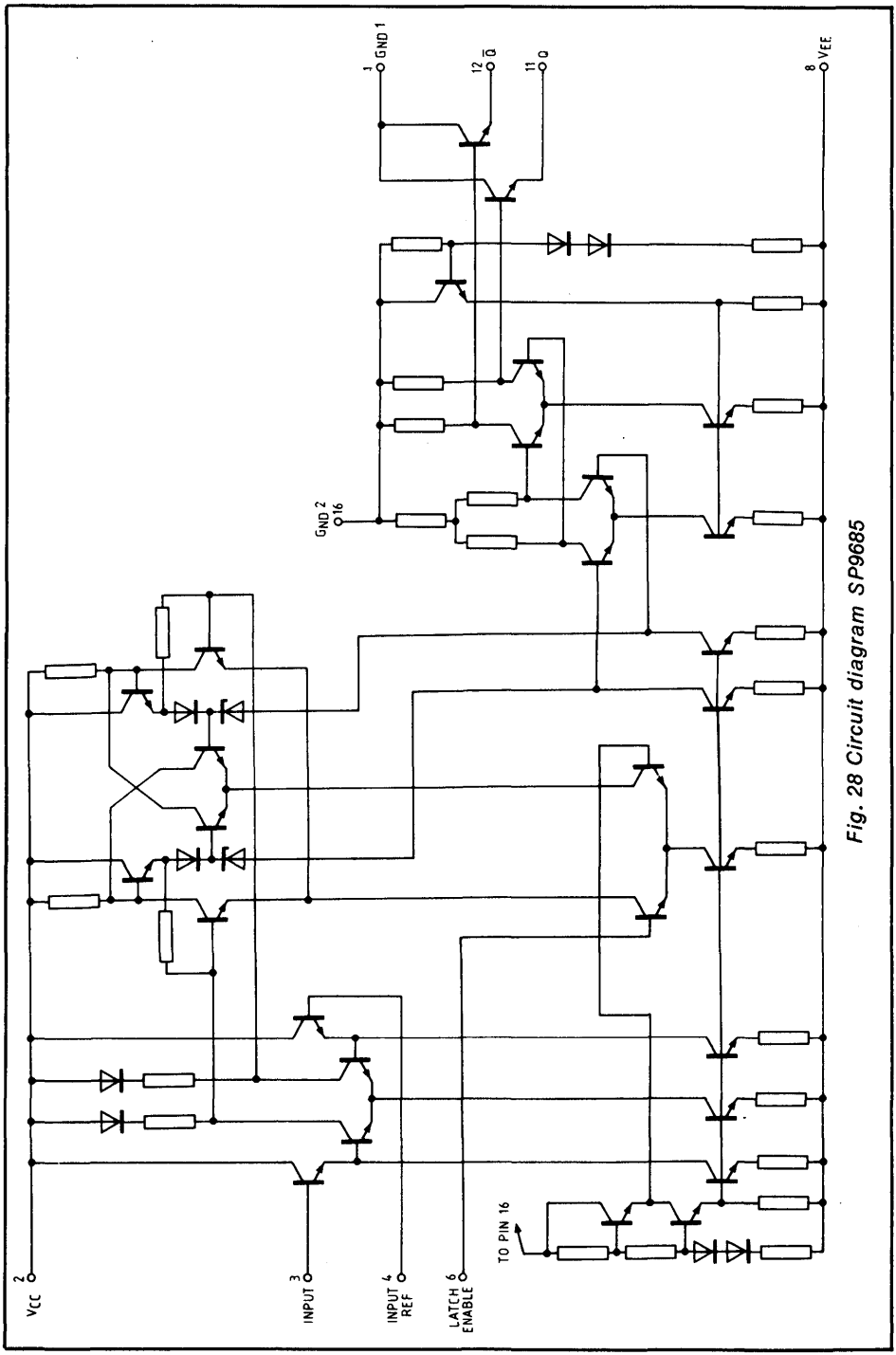


Fig. 28 Circuit diagram SP9685

latch, ignoring further inputs. Practical minimum values are a 3ns pulse width and a 10mV amplitude for reliable latching. The input biasing should be set for a mid input range threshold. Alternative forms of the same basic circuit could be used to detect negative going pulses, by feeding Q back to the latch, or detect pulses greater than a preset height, by shifting the threshold bias point.

Resetting the simple circuit can only be achieved by removing the power supplies. It is possible to produce an external resettable latch using ECLIII which will not degrade the performance if powering down is not an acceptable method.

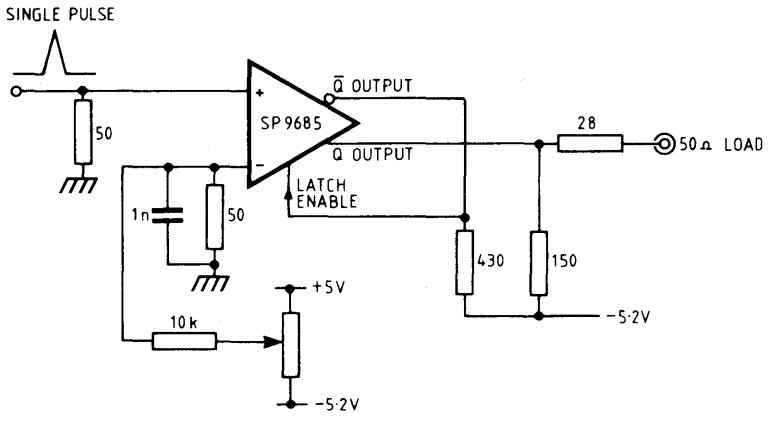


Fig. 29 Short pulse detector

An ECL two-phase clock oscillator

This simple oscillator circuit is capable of relatively high stability and wide frequency range (up to 200MHz). The maximum frequency limit is determined by the device propagation delay (typically 2ns) and the external strays. At low frequencies (below 5MHz) operation is possible, but high frequency instability on the clock edges may be seen. In practice, this is unlikely to be a restriction on the use of the device. An empirical relationship between R and C values and frequency is shown in Table 3. In the circuit shown (Fig. 30) output matching networks are included so that the device can drive 50ohm lines terminated to ground. Where higher impedance lines or short runs are used the output networks may be omitted. However, because the device edge speeds are comparable with ECLIII, good ECL practice in line matching and termination, preferably with a ground plane structure, should be employed as described in Section 3. The input bias conditions are determined by the output potentiometer R_1:R_2. It can be shown that a ratio of 3.6:1 will give a minimum of HF instability when operating at low frequency.

C_1 pf	$F_{osc}(R_3 = 1K\Omega)$MHz	$F_{osc}(R_3 = 330\Omega)$MHz
0	161	190
2.2	64	160
2.7	59	156
3.3	54	152
3.9	46	140
4.7	42	132
5.6	38	120
6.8	33	103
8.2	30	88
10	28	77

Table 3

One side of the capacitor C_1 is grounded, and all or part of the effective capacitance can be made voltage variable, producing a high frequency voltage controlled oscillator with direct ECL drive. Spectral analysis indicates that the noise sidebands from this type of oscillator are 40dB down at 50kHz away from the carrier.

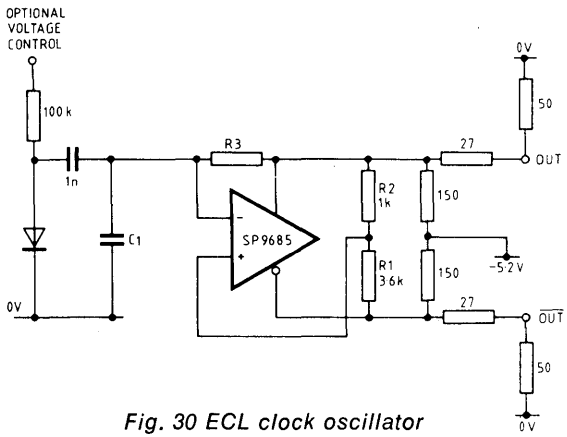


Fig. 30 ECL clock oscillator

A HIGH SPEED WINDOW DETECTOR

The SP9685 can be used to detect whether an input is within a specified voltage range. The basic circuit is well known and is shown in Fig. 31 in a form to give ECL levels. The output drives a 50Ω load to ground or, without the 27Ω series resistor, further ECL stages.

Fig. 32 illustrates the operation of the circuit which has been set up to detect a window of ±20mV about 0 volts. As the input voltage crosses zero the output changes from high to low and back again in a time mainly determined by the ECL rise and fall times. This circuit is thus detecting the crossing of the 40mV window by a signal slewing at 50V/μ sec.

Applications of the high speed window detector are in fast tracking A-D converters and high speed zero crossing detectors. The operational limit is the device propagation delay (typically 2ns) which defines the minimum width of the threshold crossing pulse.

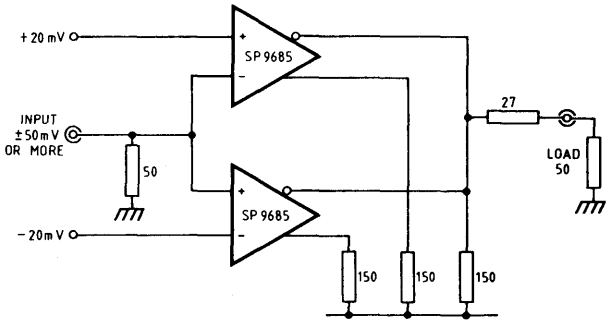


Fig. 31 High speed window detector

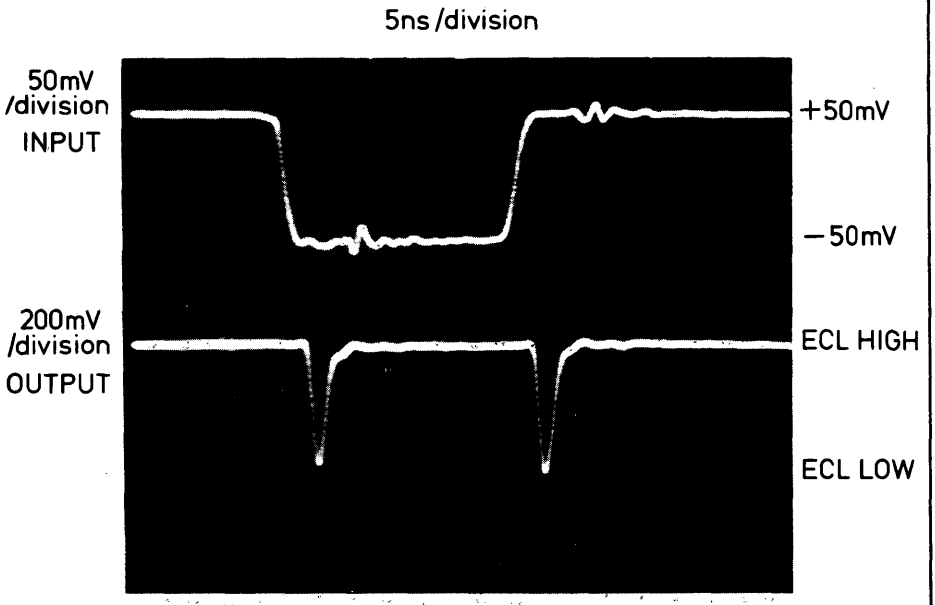


Fig. 32 Performance of high speed window detector

TECHNICAL DATA

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL301K SL301L
DUAL NPN TRANSISTORS

The SL301K and SL301L are dual NPN transistors manufactured as monolithic integrated circuits. Their close parameter matching and thermal tracking are considerably better than conventional 'two chip' duals; the frequency response is equally superior.

The SL301K and L have identical electrical specifications but differ in packaging. The SL301 is pin compatible with existing SL300 series products and available in both metal can (CM) and ceramic dual-in-line (DG) packages. The SL301K is available only in metal can (CM) and is pinned to be compatible with conventional discrete 'two chip' products. Note, however, that an extra connection is required to allow the substrate to be connected to the most negative part of the circuit.

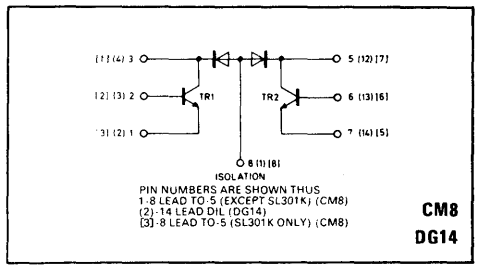


Fig. 1 SL301 circuit diagram

ORDERING CODES:

SL301K - CM
SL301L - CM
SL301L - DG

QUICK REFERENCE DATA

- Max voltage 12V to 20V
- Operating temperature range −55°C to +175°C

VOLTAGE RATING

The maximum voltage allowed between collector and emitter of each transistor is limited by dissipation and voltage breakdown. Assuming dissipation is low the rating may be determined from the following details:

(a) Forward bias condition

If the transistor is conducting the maximum collector-emitter voltage allowable is at least equal to V_{CEO} (12V). In cases where the collector current does not exceed 5mA and a resistor R is connected between base and emitter the V_{CER} rating may be determined from Fig. 8; this voltage lies between 12V and 20V depending on the value of R.

(b) Unbiased condition

If the transistor is operated with no connection to the base the maximum safe collector-emitter voltage is V_{CEO} (12V). In cases where the base emitter voltage has been reduced so the transistor is conducting at a low level it is generally permissible to increase this towards V_{CBO} (20V).

(c) Reverse biased condition

If the base of the transistor is connected via the resistor to a supply voltage equal to, or more negative than, the emitter voltage the maximum collector-emitter voltage V_{CEX} allowable (assuming negligible collector current) is limited by V_{CBO} (20V). For example, if the base is at −5V with respect to the emitter, the maximum collector voltage will be +15V.

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator
- Stable Current Source

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	250°C/W
Ceramic DIL	106°C/W
Chip-to-case thermal resistance:	
TO-5 (CM)	80°C/W
Ceramic DIL (DG)	39°C/W
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see graph)
V_{EBO}	5V
V_{CIO}	25V
I_{CM}	50mA

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Each Transistor					
BV_{CBO}	20			V	I_C = 10 µA
BV_{CEO}	12			V	I_C = 5mA
BV_{EBO}	5			V	I_E = 10 µA
BV_{CIO}	25			V	I_C = 10 µA
h_{FE}	30	50			V_{CE} = 5V, I_C = 10 µA
	40	70			V_{CE} = 5V, I_C = 100 µA
	60	100			V_{CE} = 5V, I_C = 1mA
	50	80			V_{CE} = 5V, I_C = 10mA
$V_{CE\ (SAT)}$		0.36	0.6	V	I_C = 10mA, I_B = 1mA
$V_{BE\ (SAT)}$	0.7	0.8	0.9	V	I_C = 10mA, I_B = 1mA
I_{CBO}			10	nA	V_{CB} = 10V
I_{EBO}			10	nA	V_{EB} = 2V
I_{CIO}			10	nA	V_{CI} = 10V
C_{OB}			2	pF	V_{CB} = 5V
C_{IB}			4	pF	V_{BE} = Ov
C_{CI}			6	pF	V_{CI} = 5V
f_T	400	680		MHz	V_{CE} = 5V, I_C = 5mA
Matching					
h_{FE1}/h_{FE2}	0.9		1.1		V_{CE} = 5V, I_C = 100 µA
	0.9		1.1		V_{CE} = 5V, I_C = 1mA
ΔV_{BE}			3	mV	V_{CE} = 5V, I_C = 100 µA
			3	mV	V_{CE} = 5V, I_C = 1mA
$\frac{\partial \Delta V_{BE}}{\partial T_{amb}}$			10	µV/°C	V_{CE} = 5V, I_C = 100 µA

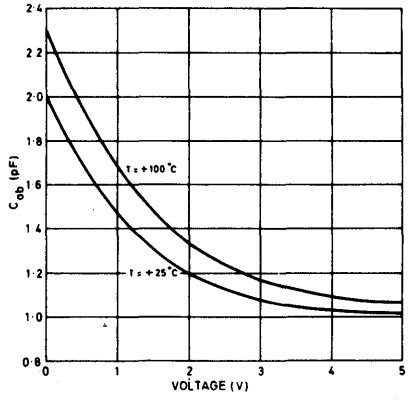


Fig. 2 Output capacitance (C_{ob}) v. voltage

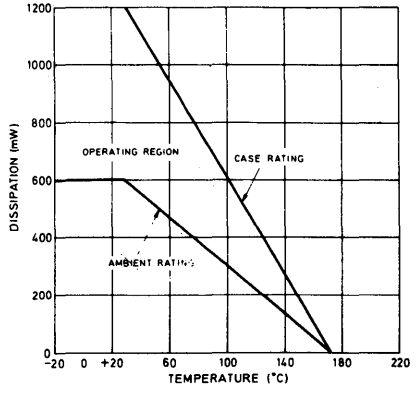


Fig. 3 Power dissipation derating curves (TO-5 package)

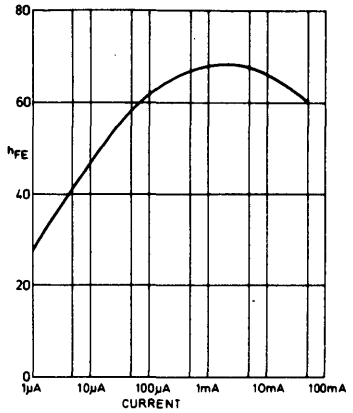


Fig. 4 Typical variation of h_{FE} with collector current

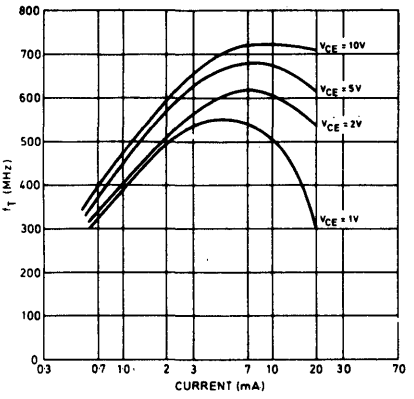


Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. f = 100 MHz)

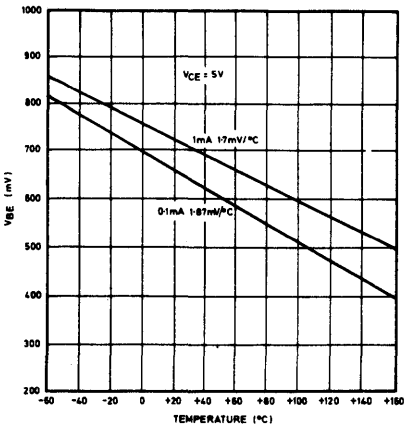


Fig. 6 V_{BE} v. temperature

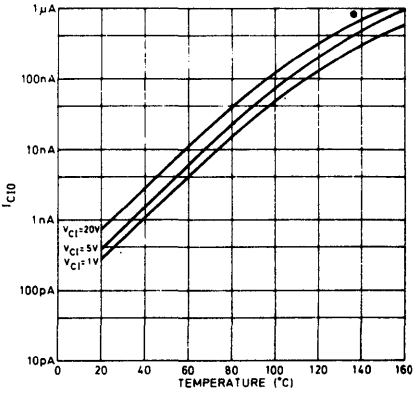


Fig. 7 Typical I_{CIO} v. temperature

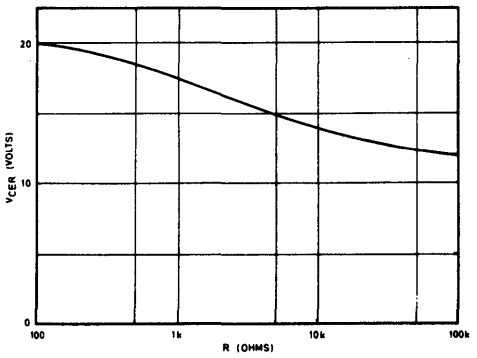


Fig. 8 Relationship between V_{CER} and R_{BE}

PLESSEY
SEMICONDUCTORS

SL300 SERIES
MATCHED TRANSISTORS

SL303L
TRIPLE NPN TRANSISTORS

The SL303 is a silicon monolithic integrated circuit comprising three separate transistors, two of which have closely matched parameters; the third transistor may be used as, for example, a tail transistor. The SL303 devices are available in 10-lead TO—5 (CM) and 14-lead dual-in-line (DG) packages.

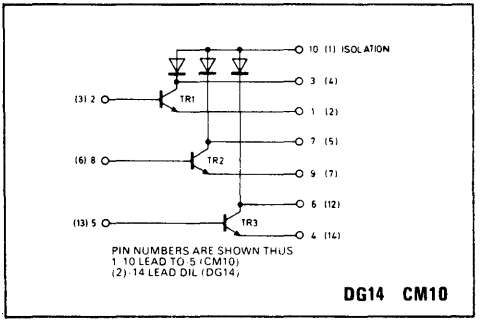


Fig. 1 Circuit diagram

ORDERING CODES:

SL303L — CM

SL303L — DG

FEATURES

- Close V_{BE} Matching
- High Gain
- Good Frequency Response
- Excellent Thermal Tracking

APPLICATIONS

- Differential Amplifier
- Comparator

QUICK REFERENCE DATA

Max voltage	12V to 20V
Operating temperature range	−55°C to +175°C

VOLTAGE RATING

The maximum voltage allowed between collector and emitter of each transistor is limited by dissipation and voltage breakdown. Assuming dissipation is low the rating may be determined from the following details:

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If the transistor is conducting the maximum collector-emitter voltage allowable is at least equal to V_{CEO} (12V). In cases where the collector current does not exceed 5mA and a resistor R is connected between base and emitter the V_{CER} rating may be determined from Fig. 8; this voltage lies between 12V and 20V depending on the value of R.

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If the transistor is operated with no connection to the base the maximum safe collector-emitter voltage is V_{CEO} (12V). In cases where the base emitter voltage has been reduced so the transistor is conducting at a low level it is generally permissible to increase this towards V_{CBO} (20V).

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If the base of the transistor is connected via the resistor to a supply voltage equal to, or more negative than, the emitter voltage the maximum collector-emitter voltage V_{CEX} allowable (assuming negligible collector current) is limited by V_{CBO} (20V). For example, if the base is at −5V with respect to the emitter, the maximum collector voltage will be +15V.

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors: thermal ratings apply to total package dissipation.

The isolation pin must always be negative with respect to the collectors.

No one transistor may dissipate more than 75% of the total power.

Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance:	
TO-5 (CM)	250°C/W
Ceramic DIL	106°C/W
Chip-to-case thermal resistance:	
TO-5 (CM)	80°C/W
Ceramic DIL (DG)	39°C/W
V_{CBO}	20V
V_{CEO}	12V
V_{CER}	12V to 20V (see graph)
V_{EBO}	5V
V_{CIO}	25V
I_{CM}	50mA

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = +25°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Each Transistor					
BV_{CBO}	20			V	I_C = 10 µA
BV_{CEO}	12			V	I_C = 5mA
BV_{EBO}	5			V	I_E = 10 µA
BV_{CIO}	25			V	I_C = 10 µA
h_{FE}	30	50			V_{CE} = 5V, I_C = 10 µA
	40	70			V_{CE} = 5V, I_C = 100 µA
	60	100			V_{CE} = 5V, I_C = 1mA
	50	80			V_{CE} = 5V, I_C = 10mA
$V_{CE\ (SAT)}$		0.36	0.6	V	I_C = 10mA, I_B = 1mA
$V_{BE\ (SAT)}$	0.7	0.8	0.9	V	I_C = 10mA, I_B = 1mA
I_{CBO}			10	nA	V_{CB} = 10V
I_{EBO}			10	nA	V_{EB} = 2V
I_{CIO}			10	nA	V_{CI} = 10V
C_{OB}			2	pF	V_{CB} = 5V
C_{IB}			4	pF	V_{BE} = Ov
C_{CI}			6	pF	V_{CI} = 5V
f_T	400	680		MHz	V_{CE} = 5V, I_C = 5mA
Matching(TR1, TR2 only)					
h_{FE1}/h_{FE2}	0.9		1.1		V_{CE} = 5V, I_C = 100 µA
	0.9		1.1		V_{CE} = 5V, I_C = 1mA
ΔV_{BE}			3	mV	V_{CE} = 5V, I_C = 100 µA
			3	mV	V_{CE} = 5V, I_C = 1mA
$\frac{\partial \Delta V_{BE}}{\partial T_{amb}}$			10	µV/°C	V_{CE} = 5V, I_C = 100 µA

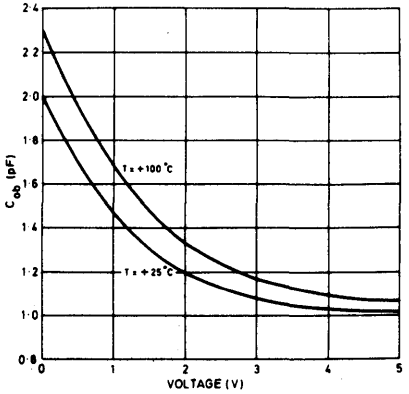


Fig. 2 Output capacitance (C_{ob}) v. voltage

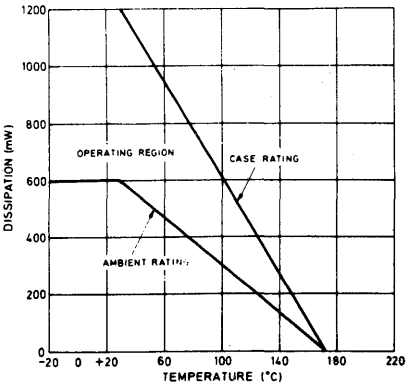


Fig. 3 Power dissipation derating curves (TO-5 package)

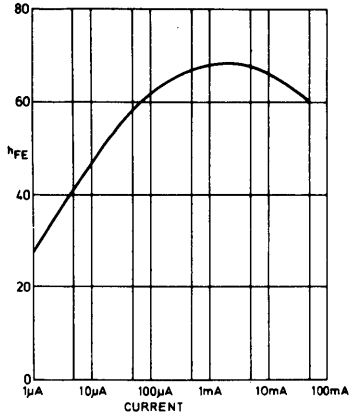


Fig. 4 Typical variation of h_{FE} with collector current

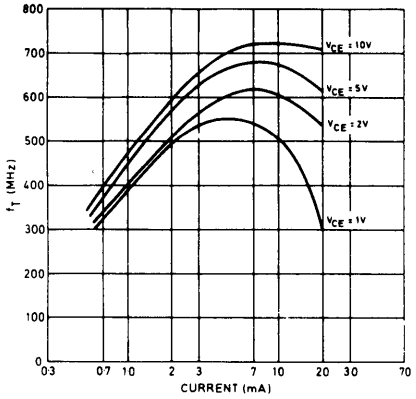


Fig. 5 f_T v. collector current ($f_T = f|h_{fe}|$. f = 100 MHz)

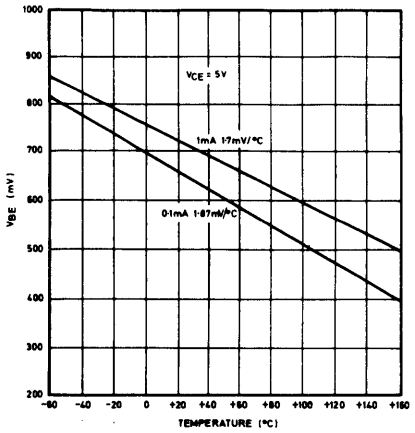


Fig. 6 V_{BE} v. temperature

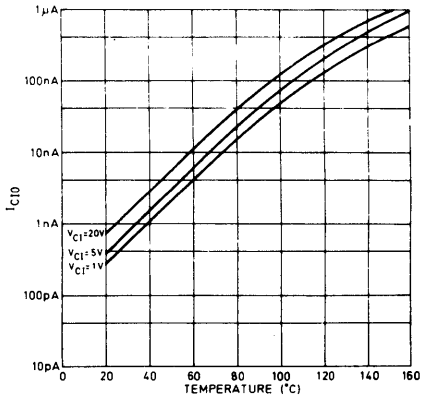


Fig. 7 Typical I_{CIO} v. temperature

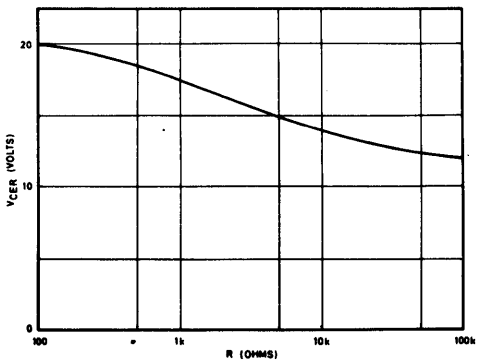


Fig. 8 Relationship between V_{CER} and R_{BE}

PLESSEY
SEMICONDUCTORS

MODULATOR DEMODULATOR

SL355C TBA673C

4-TRANSISTOR MODULATOR/DEMODULATOR

The TBA673 and SL355 are monolithic integrated 4-transistor modulator/demodulator circuits. Featuring close similarity in the characteristics of the individual transistors and optimal tracking of parameters with temperature, these devices give better balancing (and therefore less carrier leakage) than discrete circuits. The use of transistors instead of the more conventional diodes results in an improved isolation between input and output circuits.

The choice between TBA673 and SL355 will depend largely on the application. For example, the TBA673 has higher voltage characteristics than the SL355, but the SL355 would be used where high frequency performance is the prime consideration.

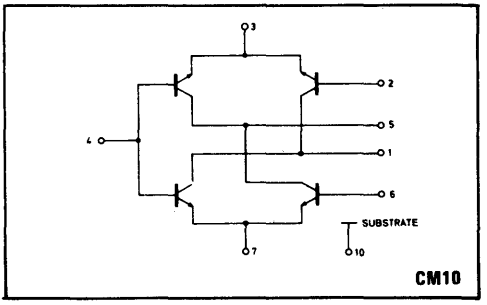


Fig. 1 Circuit diagram

FEATURES

- ΔV_{BE} = ±5mV Max.
- Close h_{FE} Matching
- High f_T : 250 MHz (TBA673)
  600 MHz (SL355)

APPLICATIONS

- DSB/DSBSC/AM Modulation
- Synchronous Detection
- FM Detection
- Choppers
- Signal Routeing
- Telephone Transmission (TBA673)

ABSOLUTE MAXIMUM RATINGS

Electrical (Each Transistor)

Rating	Symbol	TBA673	SL355	Units
Collector-emitter voltage	V_{CEO}	45	12	V
Collector base voltage	V_{CBO}	80	20	V
Emitter-base voltage	V_{EBO}	7.2	5	V
Collector-isolation voltage	V_{CI}	80	25	V
Collector current	I_C	100	20	mA

Power

Total power dissipation: See Fig. 3

Temperature

Storage temperature, T_{stg}: −35° to +125°C
Operating temperature, T_{amb}: See Fig. 3 *

NOTE

The substrate pin must be more negative than each of the collectors.

ELECTRICAL CHARACTERISTICS – TBA673

Test conditions (unless otherwise stated):
T_{amb} = +25°C
Characteristics apply to each transistor

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Each transistor						
Collector-base breakdown voltage	BV_{CBO}	80			V	I_C = 10μA, I_E = 0
Collector-emitter sustaining voltage	LV_{CEO}	45			V	I_C = 5mA, I_B = 0
Emitter-base breakdown voltage	BV_{EBO}	7.2		8.0	V	I_E = 10μA, I_C = 0
Collector-isolation breakdown voltage	BV_{CIO}	80			V	I_C = 10μA
Collector-base leakage current	I_{CBO}			10	nA	V_{CB} = 10V, I_E = 0
Emitter-base leakage current	I_{EBO}			1	nA	V_{EB} = 2V, I_C = 0
Collector-isolation leakage current	I_{CIO}			3	nA	V_{CI} = 10V
Large signal current transfer ratio	h_{FE}	80		300		I_C = 5mA, V_{CE} = 5.0V
Transition frequency	f_T	250			MHz	I_C = 5mA, V_{CE} = 5.0V
Collector-isolation capacitance	C_{CI}			6.5	pF	V_{CS} = 0V
Matching characteristics						
Base-emitter voltage difference						
TR1–TR2	$V_{BE1}-V_{BE2}$		2.0	5.0	mV	
TR3–TR4	$V_{BE3}-V_{BE4}$		2.0	5.0	mV	V_{CE} (all transistors) = 5.0V
Large signal current ratio matching						
TR1/TR2	h_{FE1}/h_{FE2}	0.9				I_E (all transistors) = 100μA
TR3/TR4	h_{FE3}/h_{FE4}	0.9				

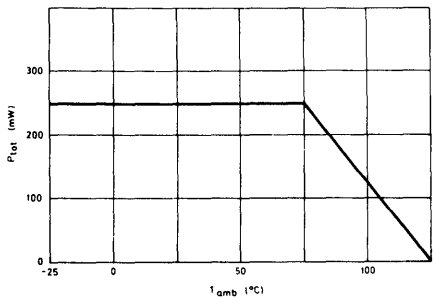


Fig. 2 Power dissipation

ELECTRICAL CHARACTERISTICS – SL355

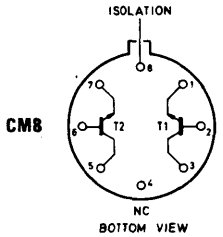
Test conditions (unless otherwise stated):
T_{amb} = +25°C
Characteristics apply to each transistor

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Each transistor						
Collector-base breakdown voltage	BV_{CBO}	25			V	I_C = 10μA, I_E = 0
Collector-emitter sustaining voltage	LV_{CEO}	12	18		V	I_C = 5mA, I_B = 0
Emitter-base breakdown voltage	BV_{EBO}	5			V	I_E = 10μA, I_C = 0
Collector-isolation breakdown voltage	BV_{CIO}	25			V	I_C = 10μA
Collector-base leakage current	I_{CBO}		0.3	1	nA	V_{CB} = 10V, I_E = 0
Emitter-base leakage current	I_{EBO}		1	10	nA	V_{EB} = 2V, I_C = 0
Collector-isolation leakage current	I_{CIO}		1	10	nA	V_{CI} = 10V
Large signal current transfer ratio	h_{FE}	10	55			I_C = 100μA, V_{CE} = 5.0V
Transition frequency	f_T		600		MHz	I_C = 5mA, V_{CE} = 5.0V
Collector-isolation capacitance	C_{CI}			6.5	pF	V_{CS} = 0V
Matching characteristics						
Base-emitter voltage difference						
TR1–TR2	$V_{BE1}-V_{BE2}$		2.0	5.0	mV	
TR3–TR4	$V_{BE3}-V_{BE4}$		2.0	5.0	mV	V_{CE} (all transistors) = 5.0V
Large signal current ratio matching						
TR1/TR2	h_{FE1}/h_{FE2}	0.9				I_E (all transistors) = 100μA
TR3/TR4	h_{FE3}/h_{FE4}	0.9				

Plessey Semiconductors

SL300 SERIES
MATCHED TRANSISTORS

SL360C
2·5GHz MATCHED TRANSISTOR PAIR



The SL360C is a bipolar monolithic chip comprising a pair of integrated circuit transistors designed for applications where close parameter matching and thermal tracking are of prime importance. They have a very high f_t (typically 2.5 GHz) and low capacitances.

ELECTRICAL CHARACTERISTICS @ T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	15	32		V	I_C = 10μA
BV_{CEO}	8	15		V	I_C = 10μA
LV_{CEO}	8	14		V	I_C = 5mA
BV_{CIO}	30	60		V	I_C = 10μA
BV_{EBO}	4.8			V	I_E = 10μA
h_{FE}	30	65			V_{CE} = 2V, I_E = 5mA
f_T	1.6	2.5		GHz	V_{CE} = 2.5V, I_E = 5mA, f = 200MHz
		3.2		GHz	V_{CE} = 5V, I_E = 25mA
$V_{BE1} - V_{BE2}$ (note 1)		3	10	mV	V_{CE} = 2V, I_E = 1mA
h_{FE1}/h_{FE2} (note 1)		1.1			V_{CE} = 2V, I_E = 5mA
V_{CE} (Sat)		0.25	0.4	V	I_E = 10mA, I_b = 1mA
C_{ob} (note 2)		0.7		pF	V_{CB} = 0V
C_{TE} (note 2)		1.5		pF	V_{BE} = 0V
C_{CI} (note 3)		2.7		pF	V_{CI} = 0V
V_{be} (on)		720		mV	I_E = 1mA, V_{CE} = 2V
I_{CBO}			1	nA	V_{CB} = 10V
I_{CIO}			1	nA	V_{CE} = 10V
I_{EBO}			1	nA	V_{EB} = 2V

NOTES

1. It is assumed here that device suffixed 1 has the greater numerical value.
2. These capacitances include stray header capacitance which is about 0.1pF.
3. These capacitances include stray header capacitance which is about 0.9pF.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Storage temperature	−55°C to +175°C
Operating junction temperature	+175°C max.

Maximum Dissipation (Note 5)

Dissipation at 25°C free air temperature	600mW
Dissipation at 100°C free air temperature	300mW

Maximum Voltages

BV_{CBO} : 15V
BV_{CEO} : 8V
BV_{EBO} : 4.8V
BV_{CIO} : 30V (note 6)

4 The maximum ratings are limiting absolute values above which life or satisfactory performance may be impaired.

5. These ratings give a junction temperature of 175° with a junction-to-ambient thermal resistance of 250°C/W (derating factor 4 mW/°C.)

6. The isolation pin should be negative with respect to the collectors.

Plessey Semiconductors

SL300 SERIES
MATCHED TRANSISTORS

SL 362C LOW NOISE TRANSISTOR PAIR

CM8

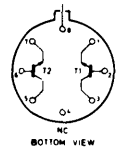


Fig.1 Pin connections

The SL362C is a bipolar monolithic integrated circuit comprising a pair of transistors designed for applications where low noise and very high frequency operation are of prime importance. A typical noise figure at 60MHz is less than 1.6dB.

ELECTRICAL CHARACTERISTICS @ T_{amb} = 25°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
BV_{CBO}	12	24		V	I_E = 10μA
BV_{CEO}	8	15		V	I_C = 10μA
BV_{CIO}	20	40		V	I_C = 10μA
BV_{EBO}	5			V	I_C = 10μA
h_{FE}	30	70			I_E = 1mA, V_{CE} = 2V
		60			I_E = 10mA, V_{CE} = 2V
f_T	1	1.6		GHz	I_E = 2mA, V_{CE} = 2V
	1.4	2.2		GHz	I_E = 10mA, V_{CE} = 10V
$V_{BE1} - V_{BE2}$		5		mV	I_E = 1mA, V_{CE} = 2V
Noise figure (note 1)		1.6	2.0	dB	I_E = 1mA, R_s = 200Ω f = 60MHz
C_{OB}		1.0		pF	V = 0
C_{CI}		0.9		pF	V = 0
C_{TE}		15.0		pF	V = 0

Note 1; The noise figures are quoted at 60MHz. Typically, they are constant from 10kHz to 200MHz.

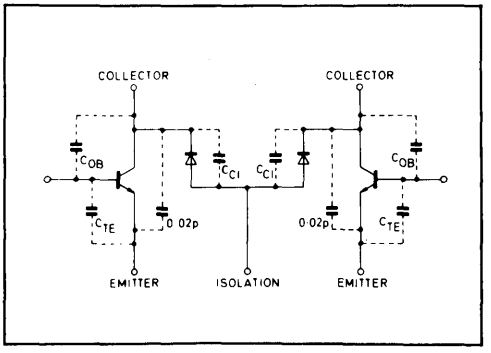


Fig.2 Equivalent circuit

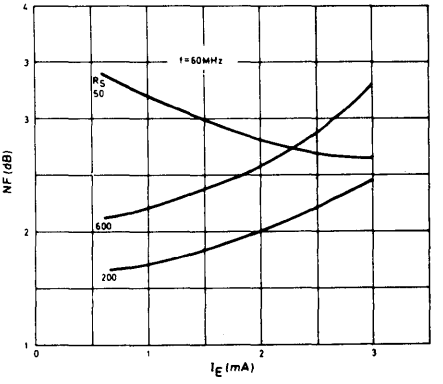


Fig.3 Typical noise figure v. emitter current

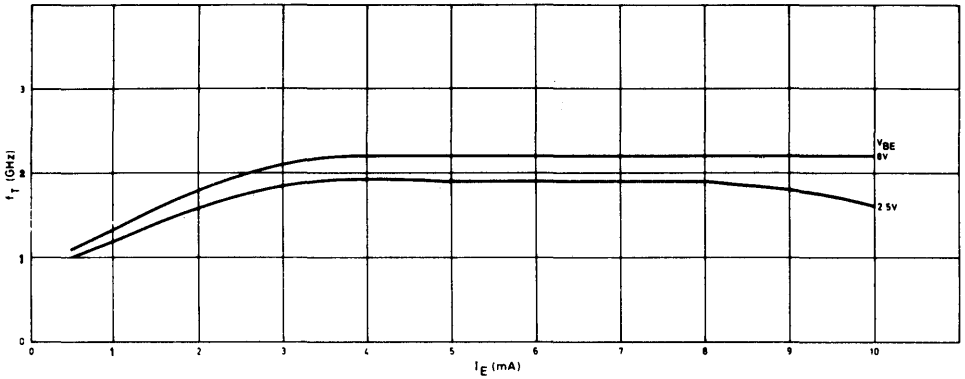


Fig.4 Typical f_T v. emitter current

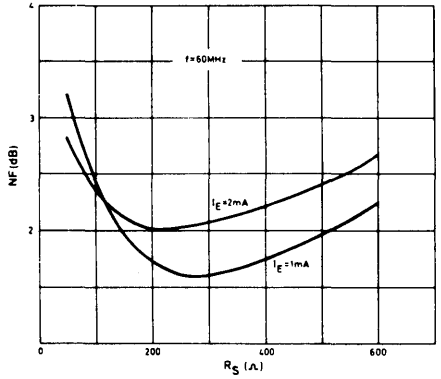


Fig. 5 Typical noise figure v. source impedance

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−55°C to +150°C
Operating Junction temperature	150°C
Total Dissipation	300mW
Collector current	50mA
BV_{CBO} :	12V
BV_{CEO} :	8V
BV_{EBO} :	5V
BV_{CIO} :	20V

Note: The isolation pin should be negative with respect to the collectors.

SIMPLE FEEDBACK AMPLIFIER (FIG.6)

The amplifier has a response down to DC achieved by the use of a long-tailed pair in the input stage, which also gives low offset voltages and a convenient method of applying negative feedback. The input is applied to Tr 1 and negative feedback applied to Tr 2 via resistors R 6 and R 7. Tr 3 is current-driven from the long-tailed pair and gives the output voltage across R 3. It is important to keep the stray capacitance from R 3 to ground as small as possible for the best high frequency performance. By the use of the very high f_T transistor pair SL360C for Tr 3 and Tr 4 any shunting effect of transistor capacitances across R 3 is reduced.

The frequency response of the amplifier shown in Fig.7 is flat to within ± 1 dB from DC to 240 MHz. The small peak at 200 MHz is not layout dependent but is due to parasitic lead inductance in the transistor packages. Measurements were made with a 50Ω source impedance and a load of 0.1 MΩ + 2.5 pF. The amplifier will drive a 50Ω load up to 150 MHz if required. For simplicity the noise figure was measured with a 50Ω source impedance and a spot noise figure of 4.2 dB was measured at frequencies of 30 to 200 MHz. The calculated variation of noise figure with source impedance is shown in Fig.8, which indicates an optimum noise figure of 2.5 dB at 200Ω source impedance.

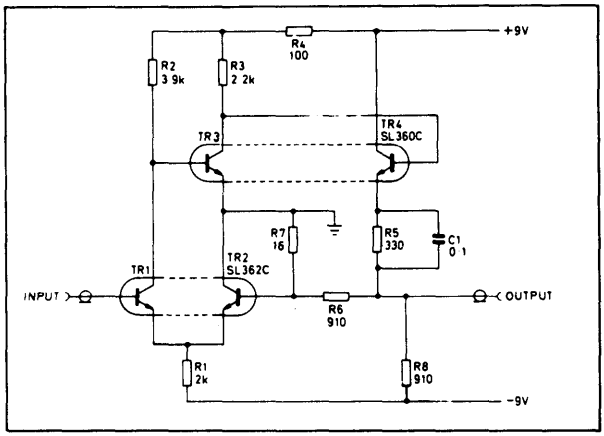


Fig. 6 Circuit diagram

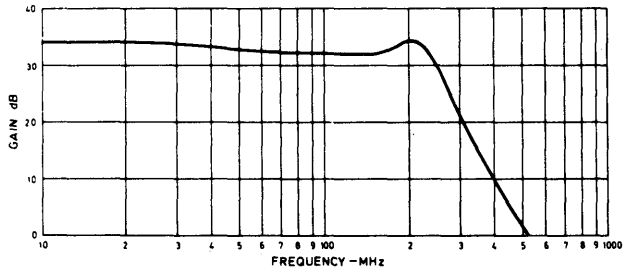


Fig. 7 Frequency response of wide band amplifier

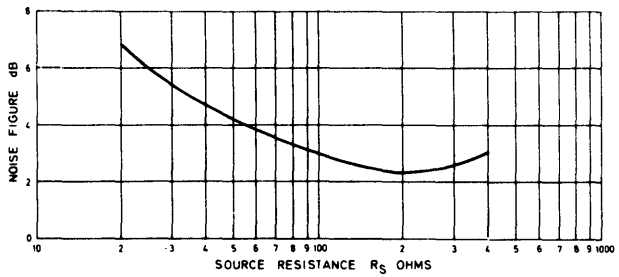


Fig. 8 Calculated noise figure v. source impedance

LAYOUT

It has been found that the circuit is not particularly sensitive to layout change, but the obvious precautions in constructing VHF circuits should be observed. Transistor leads should be kept as short as possible, in particular the emitters of Tr 1, Tr 2 and Tr 3. The leads of R 7 should also be short and if accurate gain stability is not required, a carboncomposition resistor will give minimum inductance.

NOISE REDUCTION

Two techniques are available to reduce the noise figure at low source impedances. One is to use a transformer to produce a source resistance nearer to the optimum of 200Ω. The other method is to connect two transistors in parallel as shown in Figure 9. The effect of this combination is compared with a single transistor in Figure 10. The graph shows the calculated noise figure versus emitter current with a 50Ω source impedance for both long tailed pair and common emitter configurations. As can be seen, a noise figure of 1.6 dB at 50Ω source can be achieved with the arrangement of Figure 9 in a grounded emitter configuration. The parallel connected combination will, of course, have double the output capacitance of the single device, but the effect of this on the high frequency performance can be reduced by feeding into a low impedance. Also, the combination will have a lower f_T than a single transistor at a given operating current. However, if the current is doubled in the combination, little degradation will occur.

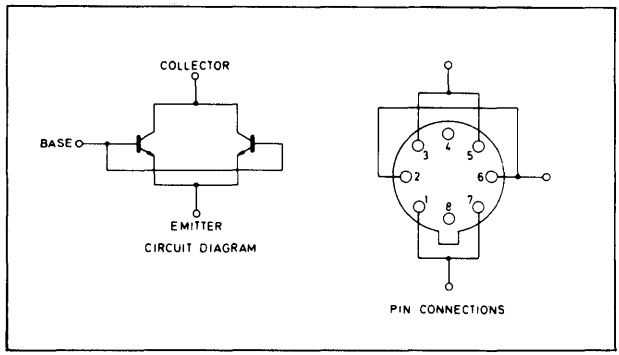


Fig. 9 Parallel connection of two transistors

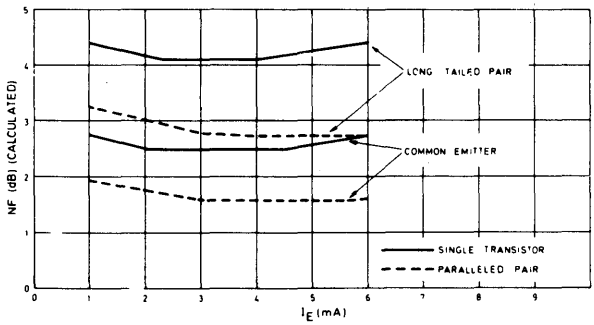


Fig. 10 Noise figure at 50Ω source impedance

PLESSEY
SEMICONDUCTORS

SL500 SERIES
WIDEBAND AMPLIFIERS

SL501A&B SL502A&B SL503A&B
SL551A&B SL552A&B SL553A&B

The SL500 series are bipolar integrated circuit wideband RF amplifiers, developed for use in linear radar IF strips operating at centre frequencies between 10 and 60 MHz. AGC facilities and supply line decoupling are incorporated in the circuits. The mid-band current gain is typically 26dB.

The SL501A and SL501B differ only in current gain and cut-off frequency tolerances. Both are supplied without an output load resistor (free collector). Flatpack versions are SL551A and SL551B, respectively. The SL502A and SL502B are similar to the SL501A and SL501B but incorporate a 1kΩ output load resistor. Flatpack versions are SL552A and SL552B, respectively.

The SL503A and SL503B are similar to the SL501A and SL501B except that the output current swing is typically 5mA. Flatpack versions of SL503A and SL503B are SL553A and SL553B, respectively.

FEATURES

- Upper Cut-off Frequency 100 MHz Typ.
- Mid-Band Current Gain 26 dB Typ.
- AGC Input
- On-chip Supply Decoupling

APPLICATIONS

- Radar IF Strips
- Wideband RF Amplifiers

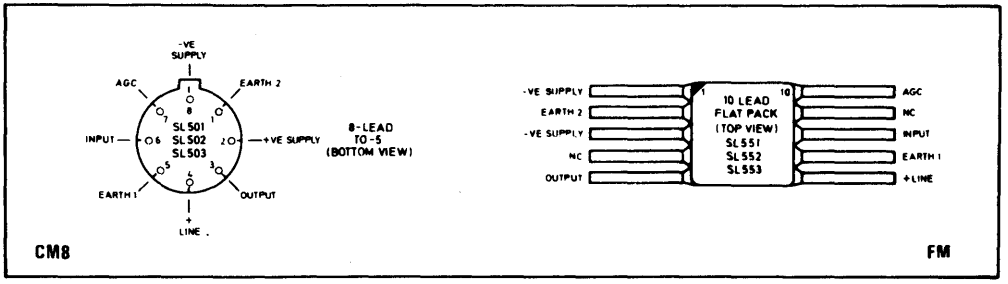
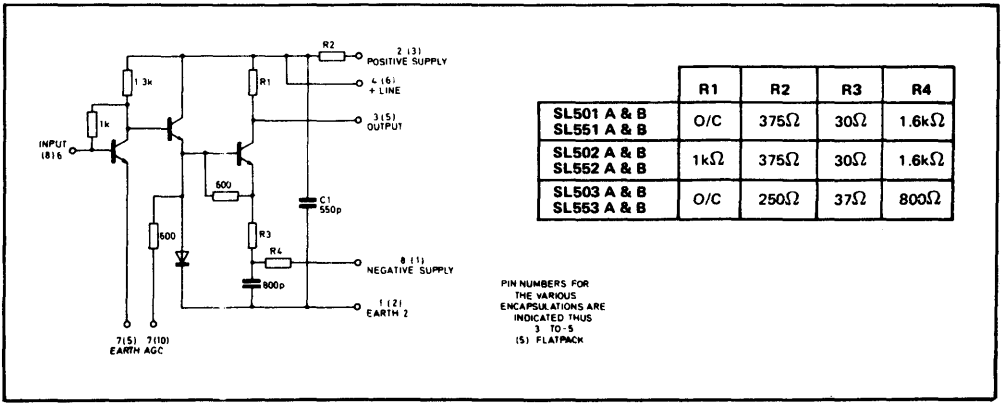


Fig. 1 Pin Connections



	R1	R2	R3	R4
SL501 A & B SL551 A & B	O/C	375Ω	30Ω	1.6kΩ
SL502 A & B SL552 A & B	1kΩ	375Ω	30Ω	1.6kΩ
SL503 A & B SL553 A & B	O/C	250Ω	37Ω	800Ω

PIN NUMBERS FOR THE VARIOUS ENCAPSULATIONS ARE INDICATED THUS 3 TO-5 (5) FLATPACK

ELECTRICAL CHARACTERISTICS

Test conditions:
Tamb +22°C ± 2°C
Positive supply +6V
Negative supply −6V
AGC not applied unless specified.
R_L = 1kΩ (SL501 and SL551); 390Ω (SL503 and SL553)

Characteristic	Circuit	Value			Units	Test conditions
		Min.	Typ.	Max.		
Current gain	SL501A, SL551A, SL502A, SL552A, SL503A, SL553A.	24	26	28	dB	f = 30MHz
	SL501B, SL551B, SL502B, SL552B, SL503B, SL553B.	23	26	29	dB	f = 30MHz
Upper cut-off frequency (see Fig. 3)	SL501A, SL551A, SL502A, SL552A, SL503A, SL553A.	80	100	120	MHz	680Ω source; 50Ω load.
	SL501B, SL551B, SL502B, SL552B, SL503B, SL553B.	60			MHz	680Ω source; 50Ω load.
Lower cut-off frequency (see Fig. 3)	All types	3	5	7	MHz	680Ω source; 50Ω load
Output swing (before clipping)	SL501A, SL551A, SL501B, SL551B, SL502A, SL552A, SL502B, SL552B.	±1.4	±2.0	±2.8	mA	
	SL503A, SL553A, SL503B, SL553B.	±4.0	±5.0	±6.5	mA	
Noise figure (see Fig. 4)	All types		6		dB	f = 60MHz; 250Ω resistive source.
AGC range (see Fig. 5)	All types		40		dB	680Ω source 50Ω load f = 60MHz AGC signal = +2V
Positive supply current	SL501A, SL551A, SL501B, SL551B, SL502A, SL552A, SL502B, SL552B.	4.1	5.5	7.0	mA	
	SL503A, SL553A, SL503B, SL553B.	6.8	8.6	11.0	mA	
Negative supply current	SL501A, SL551A, SL501B, SL551B, SL502A, SL552A, SL502B, SL552B.	2.2	3.0	3.8	mA	
	SL503A, SL553A, SL503B, SL553B.	5.0	6.3	8.0	mA	

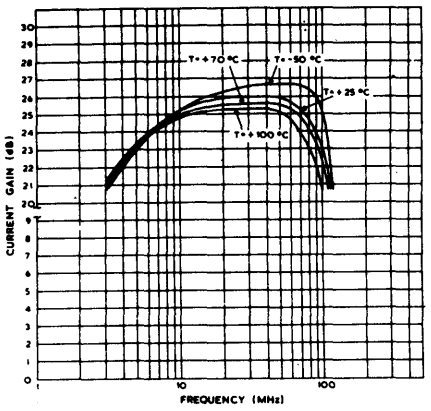


Fig. 3 Frequency response v. temperature

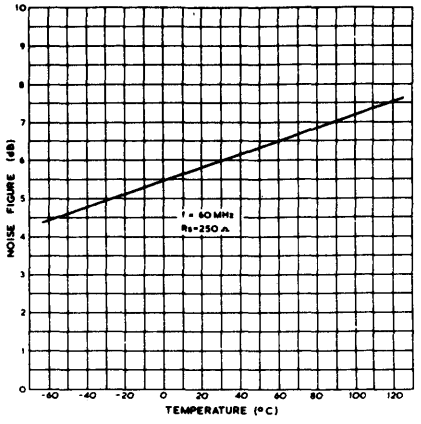


Fig. 4 Noise figure v. temperature

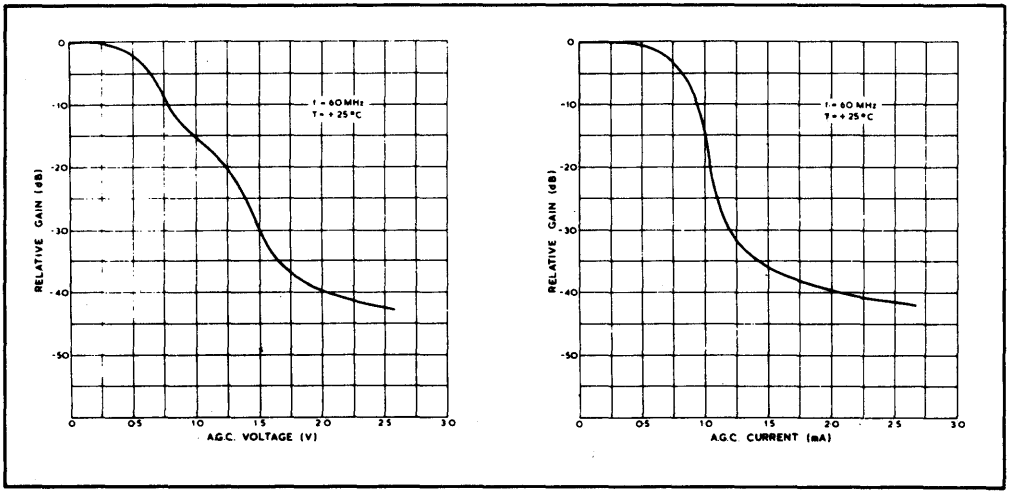
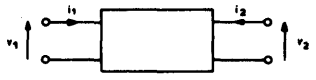


Fig. 5 A.G.C. characteristics

Characteristics of the SL500 series amplifiers expressed in Y parameters are given in Fig. 6 to 9; The parameters are defined as follows:



$$i_1 = Y_{11}v_1 + Y_{12}v_2$$

$$i_2 = Y_{21}v_1 + Y_{22}v_2$$

Where $Y_{11} = G_{11} + jB_{11}$

$$Y_{21} = |Y_{21}|e^{j\phi_{21}}$$

and $Y_{22} = G_{22} + jB_{22}$

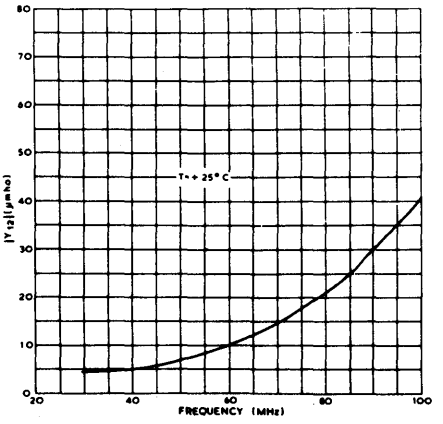
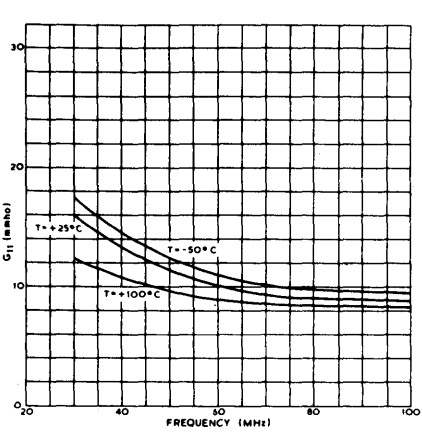
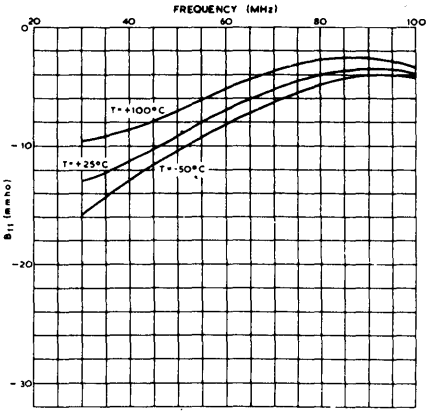
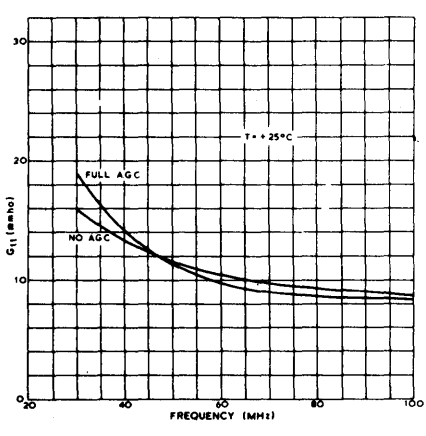


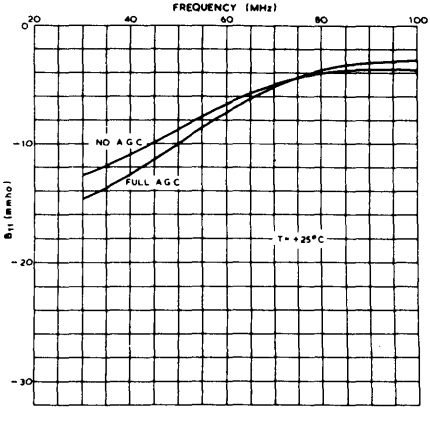
Fig. 7 Feedback admittance (Y_{12})





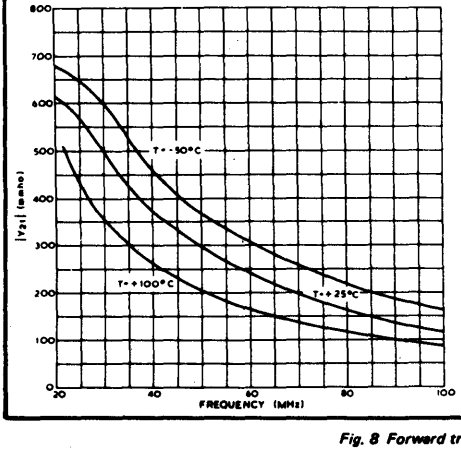
Typical input admittance v. frequency and temperature (without A.G.C.)





Typical input admittance v. frequency, with and without A.G.C.

Fig. 6 Input admittance (Y_{11})



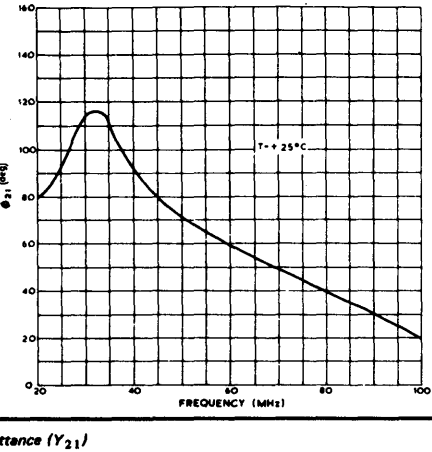
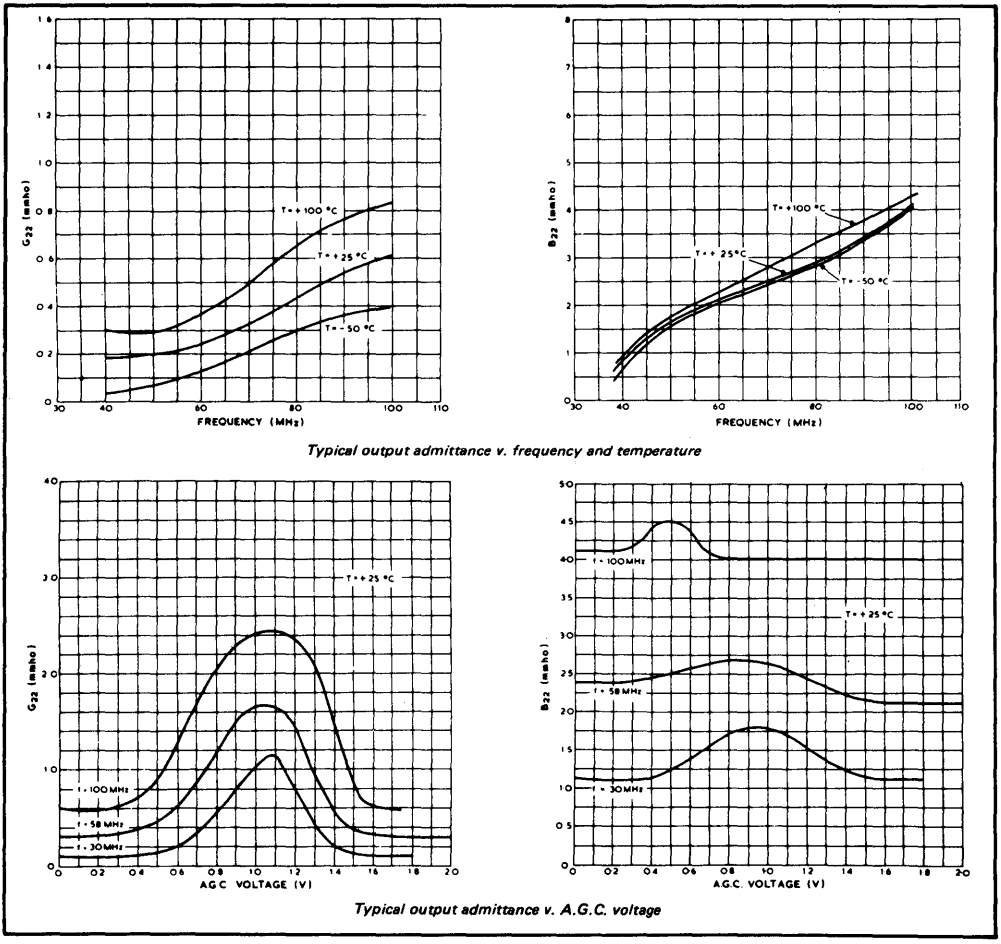


Fig. 8 Forward transfer admittance (Y_{21})



Typical output admittance v. frequency and temperature

Typical output admittance v. A.G.C. voltage

Fig. 9 Output admittance (Y_{22}). These curves apply to SL501A and B, SL503A and B, SL551A and B and SL553A and B. To obtain Y_{22} for SL502A and B and SL552A and B, increase output conductance (G_{22}) by 1mmho and output capacitance by 1pF.

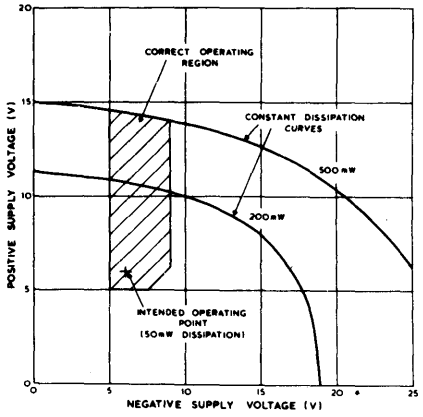


Fig. 10 Absolute maximum supply voltages.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55° to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistanc	80°C/W
Maximum AGC signal	+3.5V or 20mA
Maximum instantaneous voltage (pin 4)	+12V

OPERATING NOTES

The amplifiers are provided with two earth connections to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

The positive supply decoupling capacitor C1 has a series resistance of, typically, 10 ohms. The capacitor is a junction type having a low breakdown voltage and consequently the positive supply current increases rapidly as the supply voltage exceeds 7.5V.

AGC should not be applied to stages required to give output swings in excess of ±0.2mA unless substantial distortion can be tolerated.

SL501 and SL503 devices must be provided with a DC path between pins 3 and 4 for the collector current of the output stage. The DC resistance of this path should not exceed 1000 ohms for the SL501 and 400 ohms for the SL503. The AC load may be connected between pins 3 and 4, or pins 3 and 1. Similar conditions apply to the flatpack versions of these devices, SL551 and SL553, respectively.

Plessey Semiconductors

SL510 SERIES

RF DETECTOR/VIDEO AMPLIFIER

SL510C

INCREMENTAL GAIN 11 dB, DC-24MHz

SL511C

INCREMENTAL GAIN 16 dB, DC-14MHz

The SL510C is a bipolar integrated circuit combining the functions of r.f. detection and video amplification. The device is sectionalised to enable the r.f. detector to be used with or without the accompanying video amplifier.

The detector will accept carrier wave signals over a bandwidth from d.c. to 100 MHz. The incremental gain is typically 11dB with a video bandwidth of d.c. to 24 MHz. The circuit will handle pulse widths down to 16ns and the dynamic range is 31dB.

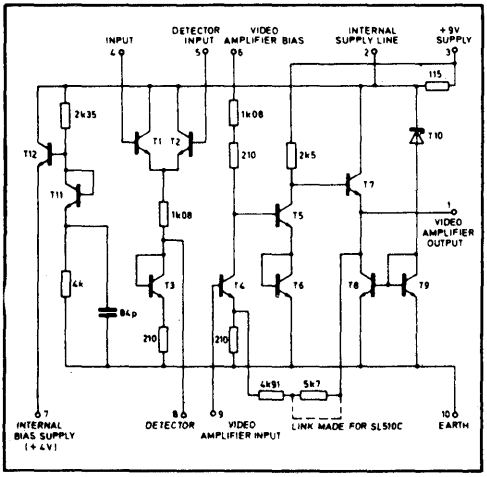


Fig. 2 Circuit diagram

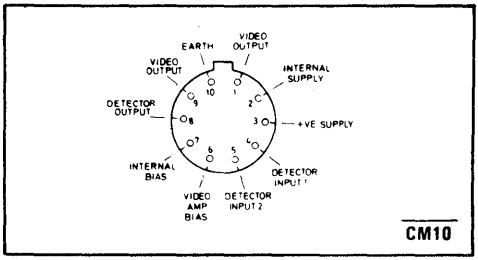


Fig. 1 Pin connections

The primary area of application is in the radar field for r.f. pulse detection, and video outputs of 6 volts and 0.5 volts can be driven into 600Ω and 50Ω loads respectively. However, the wide dynamic range of the SL510C also makes it suitable for detection of sine wave amplitude modulation.

The SL511C is of similar design, but has an incremental gain of typically 16dB over a bandwidth of d.c. to 14 MHz. The dynamic range is maintained at 28dB.

The circuits have been allocated the following NATO Stock Numbers:

Type	NATO Stock No.
SL510C	5962-99-038-0470
SL511C	5962-99-038-0471

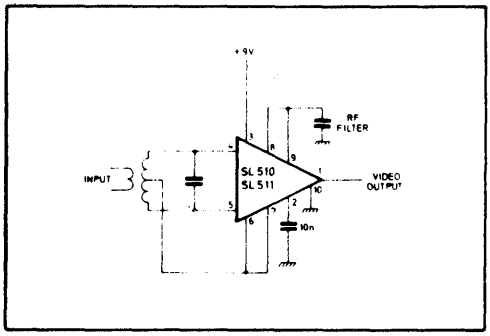


Fig. 3 Full-wave rectification

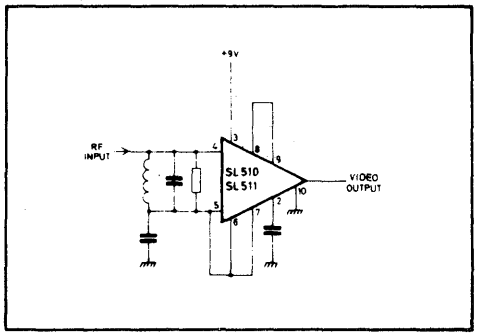


Fig. 4 Half-wave rectification

Electrical Characteristics

Test conditions (unless otherwise stated):

Temperature = +22°C ±2°C
Supply voltage = +9V
External connections: Pin 2 decoupled via 10nF capacitor to earth.
Pin 6 connected to pin 7.
Pin 8 connected to pin 9.

Characteristic	Type	Value			Units	Test Conditions
		Min.	Typ.	Max.		
Overall incremental gain (1)						
Half-wave	SL510C	3.5	5.5	7.5	dB	See Fig. 3 Detected r.f. is smoothed; centre frequency = 60 MHz
	SL511C	8.0	10.0	12.0	dB	
Full-wave	SL510C		11.5		dB	See Fig. 4
	SL511C		16.0		dB	
Pulse response	Both					
Rise time			16.0	35.0	ns	Output pulse height with respect to 0V = +5V.
Fall time			16.0	35.0	ns	Measurements are from 10% to 90% points on wave form
Positive limiting level at video outputs	Both	5.0	6.0		V	Load impedance = 600Ω; r.f. input at 60 MHz
Quiescent d.c. output voltage	SL510C		0.5	1.0	V	
	SL511C		0.6	1.0	V	
Upper cut-off frequencies						
Detector circuitry	Both		100		MHz	R_s = 25Ω, Z_L = Video input. Vin = 150mV r.m.s., 30% modulated. Output is −1dB with respect to an output at 10 MHz.
Video circuitry	SL510C		24		MHz	Output −3dB R_s = 25Ω Z_L =
			35		MHz	Output −6dB 600Ω in parallel
	SL511C		14		MHz	Output −3dB with 10pF.
			21		MHz	Output −6dB Measured with respect to an output at 2 MHz.
Overall dynamic range (2)						
Half-wave	SL510C		25		dB	See Fig. 3
	SL511C		22		dB	
Full-wave	SL510C		31		dB	See Fig. 4
	SL511C		28		dB	
Current consumption	Both		20	30	mA	
Input impedance to detector (3)	Both					Measured between pins 4 and 5 input level = 600mV r.m.s.; centre frequency = 60 MHz.
Real part		10			KΩ	
Imaginary part			3		pF	
Output impedance from video amplifier	SL510C		6		Ω	Measured at 2 MHz.
	SL511C		12		Ω	
Video amplifier small signal gain	SL510C		27		dB	Measured at 2 MHz. See Fig. 5
	SL511C		33		dB	

NOTES
1. Defined as $\frac{d(\text{video out})}{d(\text{r.f. in})}$
2. Defined as a variation of ±5% in the incremental gain.
3. This parameter is not guaranteed

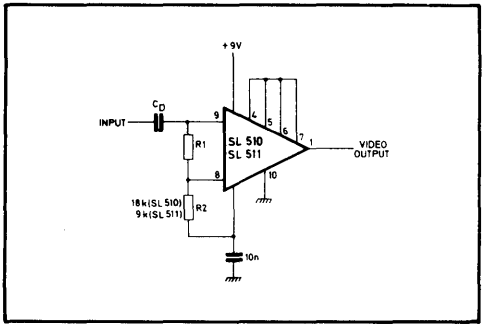


Fig. 5 Video amplification without detection

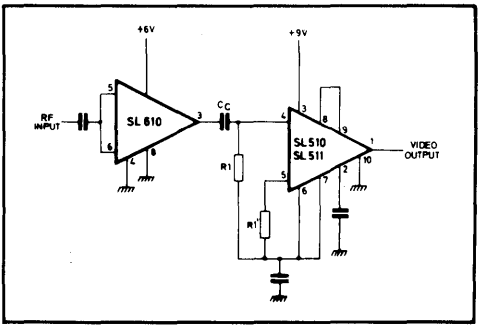


Fig. 7 R-C coupled combination (half-wave), with RF amplification.

OPERATING NOTES

Tuned circuit coupling

There are two basic methods of driving the Detector/Video when used in its normal mode; i.e. from a tuned circuit or via an R-C network. In the former case both full-wave and half-wave rectification are possible using the configurations shown in Figs. 3 & 4 respectively. When the internal bias supply is being used, as illustrated, the quiescent current level of the current source will be drawn from the supply, and the current level in the output stage of the video amplifier will be reduced accordingly. For connection to an external bias supply allowance must be made for 2mA required to drive the video amplifier bias, (pin 6).

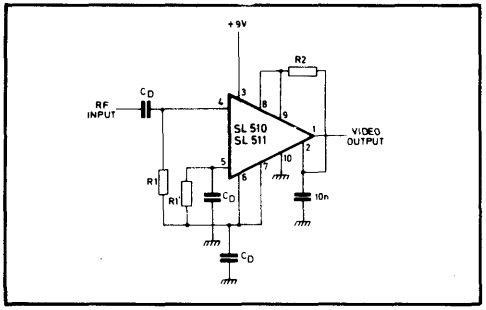


Fig. 6 R-C coupling mode (half-wave)

R-C coupling

R-C input coupling is illustrated in Fig. 6. Decoupling capacitors, C_D, should offer low a.c. impedances relative to the series resistors, R1, at the frequency of the input. Voltage drops arising through input base currents flowing in the series resistors will be amplified and will depress the d.c. quiescent output of the video amplifier. For low β devices this can be excessive and should be offset by introducing resistor R2 which injects current into pin 8 to raise the output level. With R2 connected to the internal supply line, as shown, the d.c. output voltage will be 52/R2 (±25%) for the SL510C and 26/R2 (±25%) for the SL511C where R2 is in kΩ.

Fig. 5 illustrates this technique applied to the use of the circuit for video amplification without detection, where it may be necessary to set the output quiescent voltage midway between the internal supply line and earth. Input coupling is via C_D/R2, where the reactance of C_D is chosen to be low compared with R2. Since the video amplifier response extends down to d.c. R2 must be small to limit the input voltage error due to the base current flowing in R2. This can be overcome by using an r.f. choke with low d.c. resistance.

SL610/11/12 – SL510/11 Combination

The simplest method of connection is shown in Fig. 7 using R-C coupling. In view of the bandwidths involved due care in layout must be observed (note that the output earth of the SL510 is taken forward to the video-detector earth). For tuned coupling refer to the SL610/11/12 data sheet.

Absolute Maximum Ratings

Storage Temperature	−55°C to +175°C
Operating Temperature	−55°C to +125°C
Supply Voltage	+12 Volts

CIRCUIT DESCRIPTION

The circuit (Fig. 2) incorporates a long tailed pair detector, with both input bases (pins 4 and 5) accessible so that it can be driven either full-wave or half-wave, as illustrated in the application notes. The output (pin 8) is taken from an attenuation chain at a level suitable to drive the video amplifier (input pin 9). With r.f. filtering between pins 8 and 9 (the usual mode of operation) the input level to the video amplifier will reduce to the mean value of the detected r.f. i.e. ($2/\pi$ x peak output) for full-wave rectification and ($1/\pi$ x peak output) for half-wave rectification.

The video amplifier is directly coupled throughout and essentially consists of two stages of gain TR4 and TR5, and an emitter follower output stage TR7 with overall feedback to the emitter of TR4. Pin 6, the video amplifier bias, should be taken to the same d.c. potential as pins 4 and 5 to ensure that the quiescent output level is tolerant of variations in this potential. In this condition the output is at a 'zero' quiescent level (nominally +600 mV), which allows direct coupling to the load, a convenient feature since output pulses are uni-directional when driving from the detector.

The internal bias supply at pin 7 is an emitter follower biased from the supply line and an external current drain is required to establish its quiescent current.

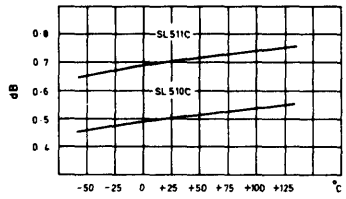


Fig. 8 Change in quiescent d.c. output voltage v. temperature

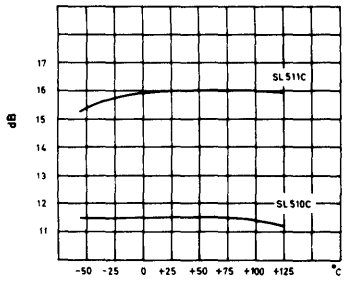


Fig. 10 Change in overall incremental gain v. temperature

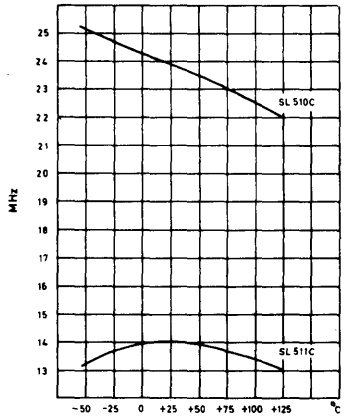


Fig. 9 Change in upper 3dB point for video amplifier v. temperature

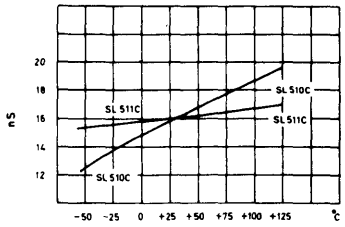


Fig. 11 Change in rise/fall time with temperature

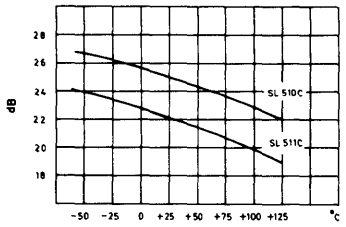


Fig. 12 Change in dynamic range (half-wave) with temperature

Plessey Semiconductors

SL521 SERIES
WIDEBAND AMPLIFIERS

SL521A, B & C

The SL521A, B and C are bipolar monolithic integrated circuit wideband amplifiers, intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 100MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL521 is typically 12 dB (4 times). The SL521A, B and C differ mainly in the tolerance of voltage gain and upper cut-off frequency. The SL521A, B and C versions have TO-5 encapsulation.

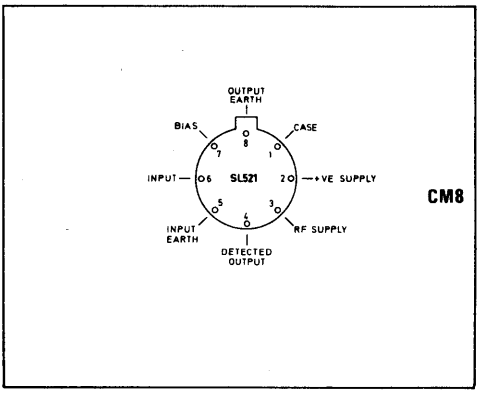


Fig. 1 Pin connections

FEATURES

- Well-defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 165MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF strips with Gains up to 108 dB and Linearity Better Than 1 dB.

ABSOLUTE MAXIMUM RATINGS (Non-simultaneous)

Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

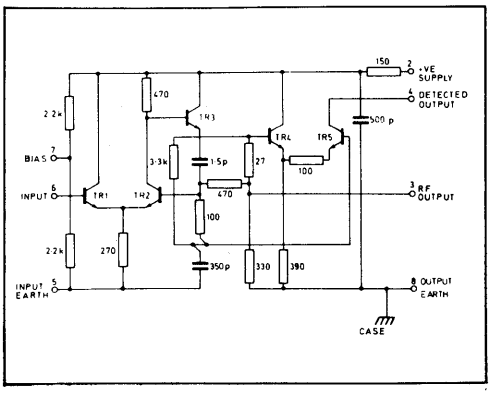


Fig. 2 SL521 Circuit diagram

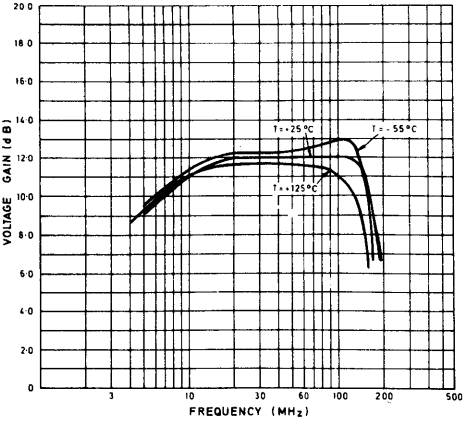


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +22°C ± 2°C
Supply voltage = +6V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 30MHz	SL521A,	11.5		12.5	dB	10 ohms source, 8pF load
	SL521B,	11.3		12.7	dB	
	SL521C,	11.0		13.0	dB	
Voltage gain, f = 60MHz	SL521A,	11.3		12.7	dB	
	SL521B,	11.0		13.0	dB	
	SL521C,	10.7		13.3	dB	
Upper cut-off frequency (Fig. 3)	SL521A,	150	170		MHz	10 ohms source, 8pF load
	SL521B,	140	170		MHz	
	SL521C,	130	170		MHz	
Lower cut-off frequency (Fig. 3)	All types		5	7	MHz	10 ohms source, 8pF load
Propagation delay	All types		2		ns	
Maximum rectified video output current (Fig. 4 and 5)	SL521A,	1.00		1.10	mA	f = 60MHz, 0.5V rms input
	SL521B,	0.95		1.15	mA	
	SL521C,	0.90		1.20	mA	
Variation of gain with supply voltage	All types		0.7		db/V	
Variation of maximum rectified output current with supply voltage	All types		25		%/V	
Maximum input signal before overload	All types	1.8	1.9		V rms	See note below
Noise figure (Fig. 6)			4	5.25	dB	f = 60MHz, Rs = 450 ohms
Supply current	SL521A, SL521B,	12.5	15.0	18.0	mA	
	SL521C,	11.5	15.0	19.0	mA	
Maxiumum RF output voltage			1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias TR1 base-collector junction on peaks.

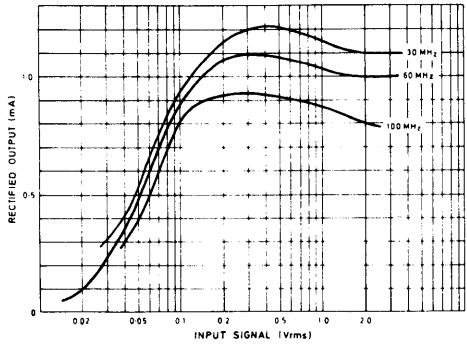


Fig. 4 Rectified output current v. input signal

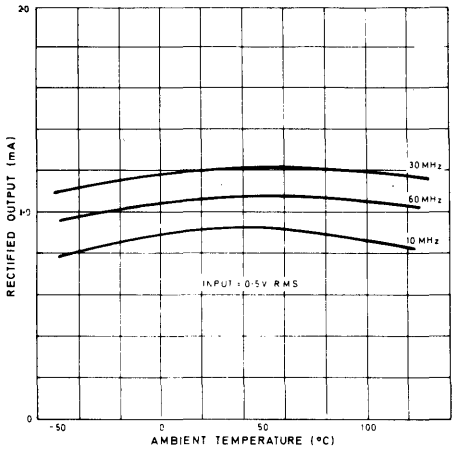


Fig. 5 Maximum rectified output current v. temperature

The 500pF supply decoupling capacitor has a resistance of, typically, 10 ohms. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see ABSOLUTE MAXIMUM RATINGS).

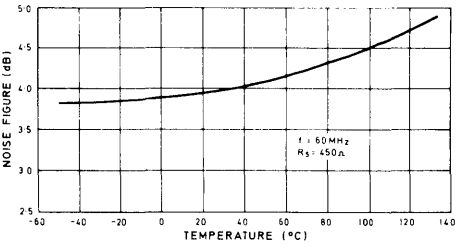


Fig. 6 Typical noise figure v. temperature

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8 (This figure shows the T0-5 version.)

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

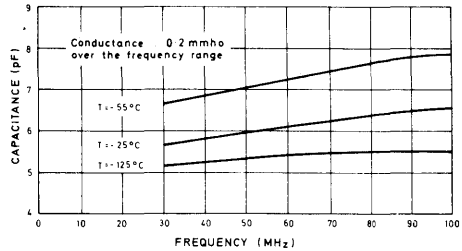


Fig. 7 Input admittance with open-circuit output

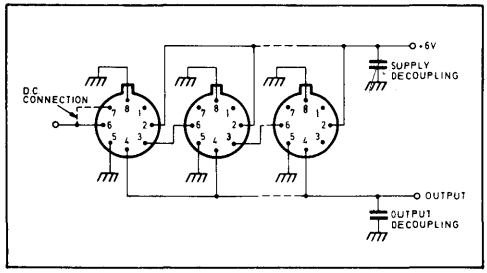


Fig. 8 Direct coupled amplifiers

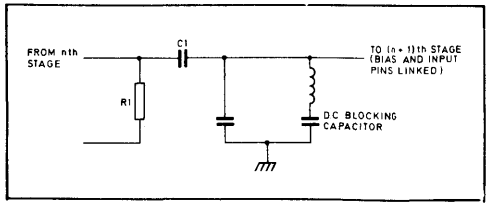


Fig. 9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guess-work.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals)

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6\text{mmhos (f = 10MHz)}$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 6 joined to pin 7 and
fed from 300 ohms source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}$ $\left[\frac{V_6}{V_2}\right]_a$ $\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6 dB/octave.

PLESSEY
Semiconductors

SL523 B,C&H

DUAL WIDEBAND LOG AMPLIFIER

The SL523B and C are wideband amplifiers for use in successive detection logarithmic IF strips operating at centre frequencies between 10 and 100MHz. They are pin-compatible with the SL521 series of logarithmic amplifiers and comprise two amplifiers, internally connected in cascade. Small signal voltage gain is 24dB and an internal detector with an accurate logarithmic characteristic over a 20dB range produces a maximum output of 2.1mA. A strip of SL523s can be directly coupled and decoupling is provided on each amplifier. RF limiting occurs at an input voltage of 25mV RMS but the device will withstand input voltages up to 1.8V RMS without damage.

The SL523H is supplied in matched sets of eight devices. The gain at 60MHz of the devices in the set is matched to 0.75dB. In all other respects the device is identical to an SL523B. This selection enables very precise log strips to be produced.

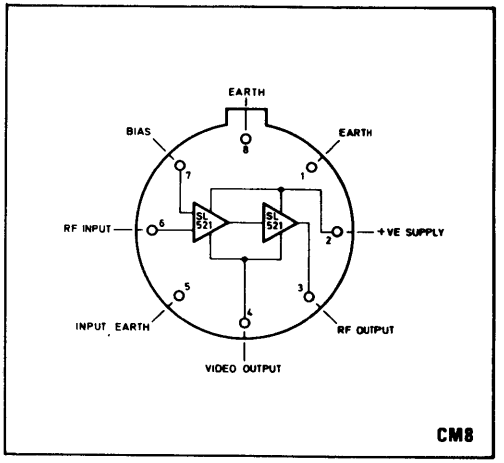


Fig. 1 Pin connections (view from beneath)

FEATURES

- Small Size/Weight
- Lower Power Consumption
- Readily Cascadable
- Accurate Logarithmic Detector Characteristic

QUICK REFERENCE DATA

Small Signal Voltage Gain	24dB
Detector Output Current	2.1mA
Noise Figure	4dB
Frequency Range	10 – 100MHz
Supply Voltage	+6V
Supply Current	30mA

ABSOLUTE MAXIMUM RATINGS

(Non simultaneous)

Storage temperature range —55°C to + 175°C
Operating temperature range —55°C to +125°C
Maximum instantaneous voltage at video output +12V
Supply voltage +9V

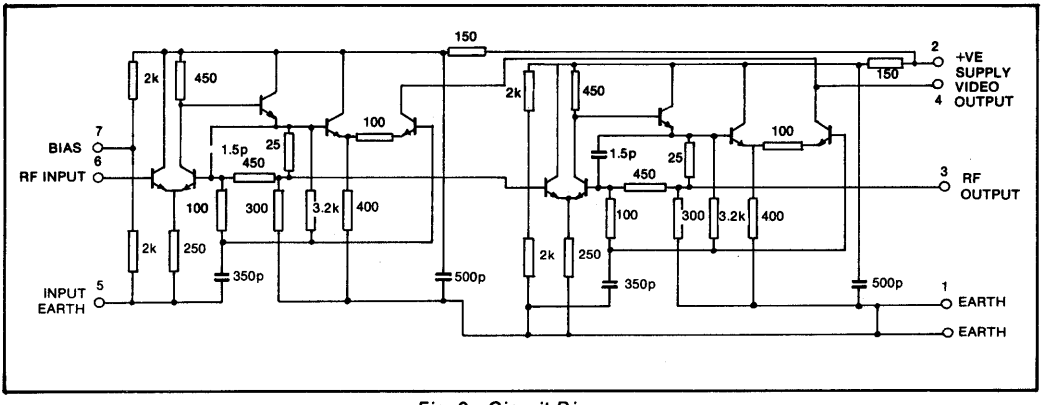


Fig. 2. Circuit Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Ambient temperature 22°C ±2°C
Supply voltage +6V
DC connection between pins 6 and 7
Source impedance 10Ω
Load impedance 8pF
Frequency 60MHz

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Small signal voltage gain	B H	22.6	24	25.4	dB	Freq. 30MHz
	C	22	24	26	dB	
Small signal voltage gain	B H	22	24	26	dB	Freq. 60MHz
	C	21.4	24	26.6	dB	
Gain variation (set of 8)	H		0.5	0.75	dB	Freq. = 60MHz
Upper cut off frequency	B C & H	120	150		MHz	
Lower cut-off frequency	B C & H		10	15	MHz	
Propagation delay	B C & H		4		ns	
Maximum rectified video output current	B H	1.9	2.1	2.3	mA	V_{in} 0.5VRMS
	C	1.8	2.1	2.4	mA	
Maximum input signal before overload	B C & H	1.8	1.9		VRMS	
Noise figure			4	5.25	dB	Source impedance 450Ω
Supply current	B H	25	30	36	mA	
	C	23	30	38	mA	
Maximum RF output voltage	B C & H		1.2		Vp-p	

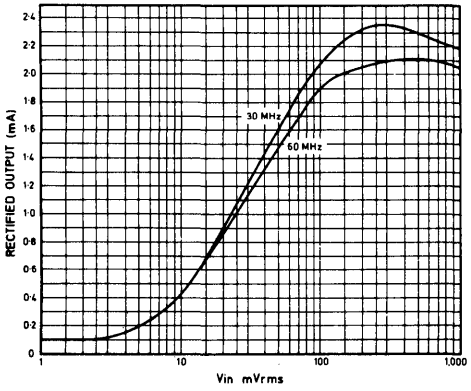


Fig. 3 Rectified output current v. input signal

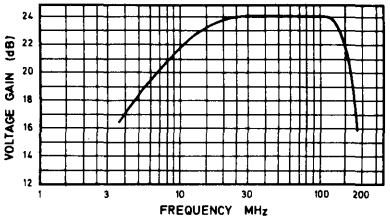
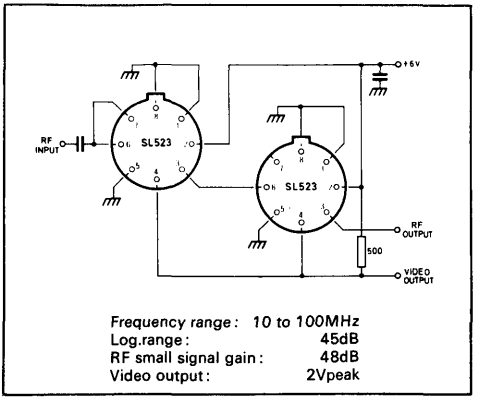


Fig. 4 Voltage gain v. frequency



Frequency range: 10 to 100MHz
Log.range: 45dB
RF small signal gain: 48dB
Video output: 2Vpeak

Fig. 5 Simple log.IF strip

OPERATING NOTES

The amplifier is designed to be directly coupled (see Fig. 5)

The fourth stage in an untuned cascade will give full output on the broad band noise generated by the first stage.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The network chosen must give unity voltage gain at resonance to avoid distorting the log law. The typical value for input impedance is 500 ohms in parallel with 5pF and the output impedance is typically 30 ohms.

Although a 1nF supply line decoupling capacitor is included in the can an extra capacitor is required when the amplifiers are cascaded. Minimum values for this capacitor are: 2 stages – 3nF, 3 or more stages – 30nF.

In cascades of 3 or more stages care must be taken to avoid oscillations caused either by inductance common to the input and output earths of the strip or by feedback along the common video line. The use of a continuous earth plane will avoid earth inductance problems and a common base amplifier in the video line isolating the first two stages as shown in Fig.6 will eliminate feedback on the video line.

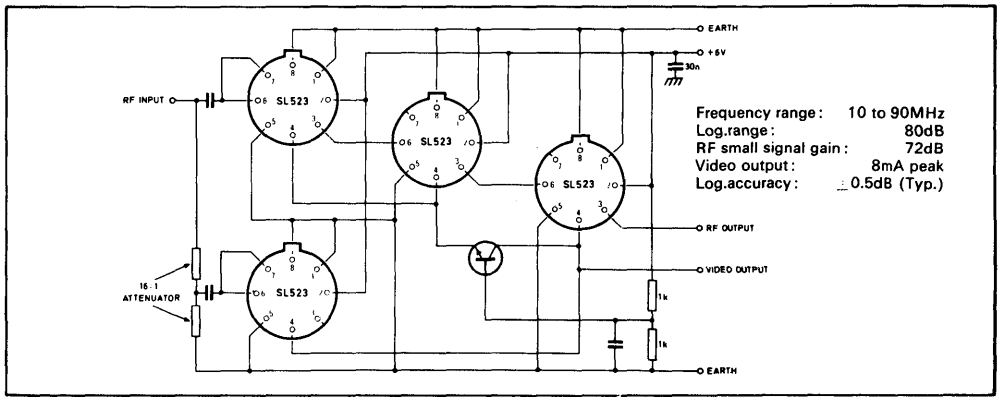


Fig. 6 Wide dynamic range log.IF strip

TYPICAL PERFORMANCE

Unselected SL523B devices were tested in a wide-band logarithmic amplifier, described in RSRE Memo. No.3027 and shown in Fig. 7.
The amplifier consists of six logarithmic stages and two 'lift' stages, giving an overall dynamic range of greater than 80dB. The response and error curves were plotted on an RHG Log Test Set and bandwidth measurements were made with a Telonic Sweeper and Tektronix oscilloscope.

Fig. 8 shows the dynamic range error curve and frequency response obtained. The stage gains of the SL523 devices used were as shown in Table 1.

Stages	f_o (MHz)	Gain (dB)	Max. Deviation (dB)
1	60	24.123	
2	60	24.089	0.235
3	60	23.888	
Lift	60	24.086	

Table 1 Stage gains of SL523 used in performance tests

The input v. output characteristic (Fig. 8a) is calibrated at 10dB/cm in the X axis and 1V/cm in the Y axis. 80dB of dynamic range was attained.

The error characteristic (Fig. 8b) is calibrated at 10dB/cm in the X axis and 1dB/cm in the Y axis; this shows the error between the log. input v. output characteristic and a mean straight line and shows that a dynamic range of 80dB was obtained with an accuracy of ±0.5dB.

As a comparison, the log amplifier of Fig. 7 was constructed with randomly selected SL521Bs (two SL521Bs replacing each SL523B). Again, a dynamic response of 80dB was obtained (Fig. 9a) with an accuracy of ±0.75dB (Fig. 9b).

Bandwidth curves are shown in Figs. 8c and 9c, where the amplitude scale is 2dB/cm, with frequency markers at 10MHz intervals from 20 to 100MHz. Using SL523Bs (Fig. 8c), the frequency response at 90MHz is 4dB down on maximum and there is a fall-off in response after 50MHz. Fig. 9c shows that the frequency response of the amplifier falls off more gradually after 40MHz but again the response at 90MHz is 4dB down on maximum.

These tests show that the SL523 is a very successful dual-stage log.amplifier element and, since it is pin-compatible with the SL521, enables retrofit to be carried out in existing log.amplifiers. It will be of greatest benefit however, in the design of new log amplifiers, enabling very compact units to be realised with a much shorter summation line.

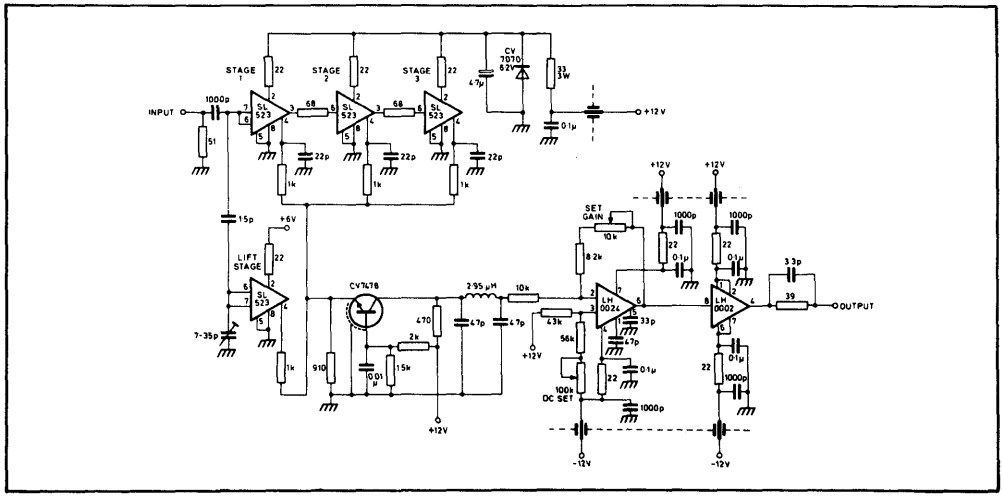


Fig. 7 Wideband logarithmic amplifier

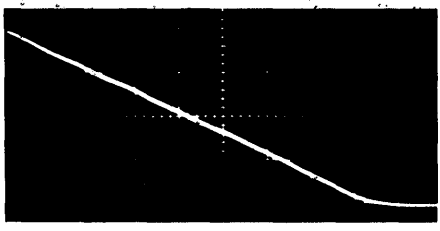


Fig. 8a Input/output

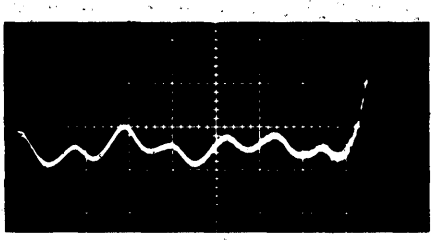


Fig. 8b Error curve

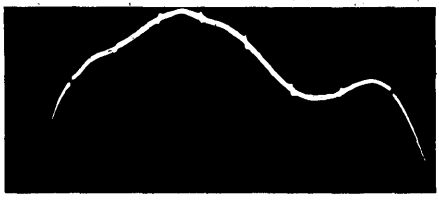


Fig. 8c Frequency response, detected output

Fig. 8 Characteristics of circuit shown in Fig. 7 using SL523Bs

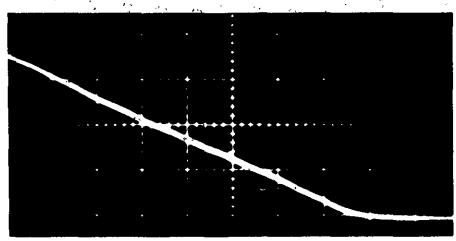


Fig.9a Input/output

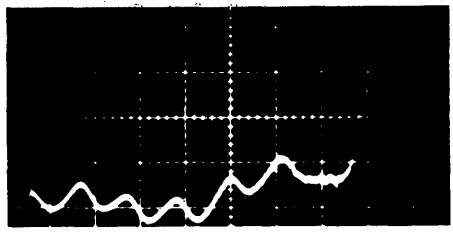


Fig. 9b Error curve

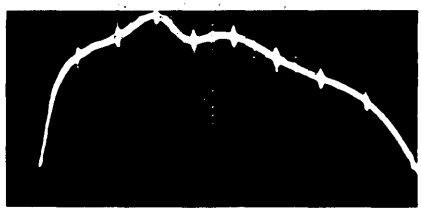


Fig. 9c Frequency response, detected output

Fig. 9 Characteristics of circuit shown in Fig. 7 using SL521Bs

Plessey Semiconductors

SL500 SERIES
WIDEBAND AMPLIFIERS

SL525C
WIDEBAND LOG IF STRIP AMPLIFIER

The SL525C is a bipolar monolithic integrated circuit wideband amplifier, intended primarily for use in successive detection logarithmic I.F. strips, operating at centre frequencies between 10MHz and 60MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL525C is typically 12dB.

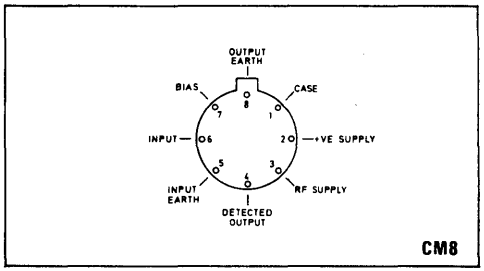


Fig. 1 Pin connections

FEATURES

- Well-defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150 MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF strips with Gains up to 108 dB and Linearity Better Than 1 dB.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Operating Temperature range	−20°C to +100°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

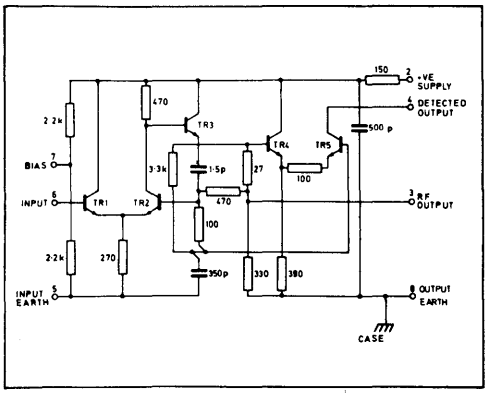


Fig. 2 Circuit diagram

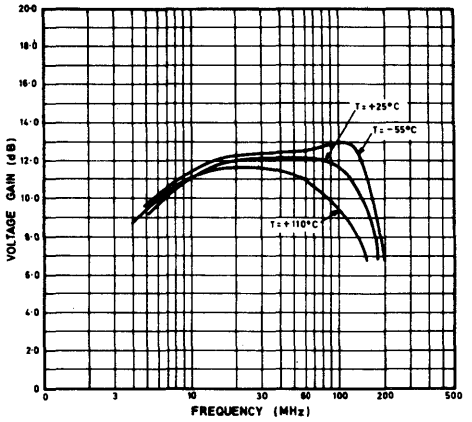


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):–
T_A = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10.5		13.5	dB	f = 30MHz, R_S = 10Ω, C_L = 8pF
	10.0		14.0	dB	f = 60MHz, R_S = 10Ω, C_L = 8pF
Upper cut-off frequency (Fig. 3)	120	150		MHz	R_S = 10Ω, C_L = 8pF
Lower cut-off frequency (Fig. 3)		5	7	MHz	R_S = 10Ω, C_L = 8pF
Propagation delay		2		ns	
Max. rectified video output current (Figs. 4 and 5)	0.85		1.25	mA	f = 60MHz, V_{in} = 500mV rms
Variation of gain with supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		%/V	
Maximum I/P signal before overload	1.8	1.9		Vrms	See note 1
Noise figure (Fig. 6)		4	5.25	dB	f = 60MHz, R_S = 450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		15		mA	

NOTE
1. Overload occurs when the input signal reaches a level sufficient to forward-bias the base-collector junction of TR1 on peak.

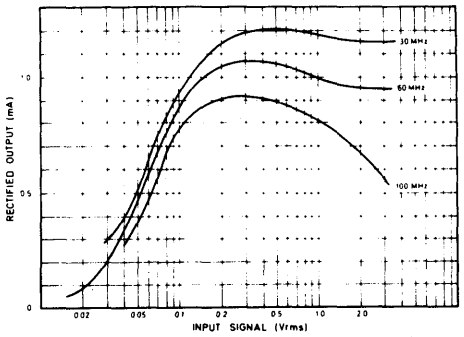


Fig. 4 Rectified output current v. input signal

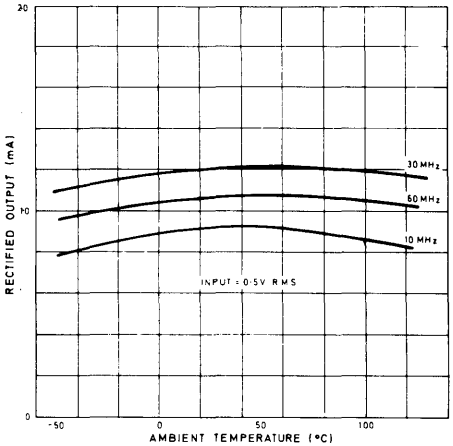


Fig. 5 Maximum rectified output current v. temperature

The 500pF supply decoupling capacitor has a resistance of, typically, 10 ohms. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see ABSOLUTE MAXIMUM RATINGS).

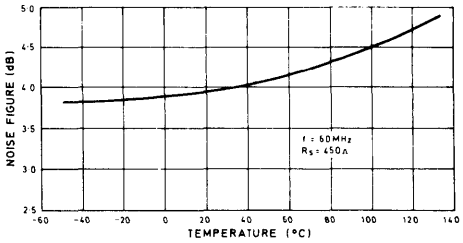


Fig. 6 Typical noise figure v. temperature

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rises times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

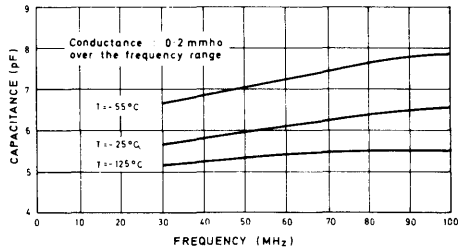


Fig. 7 Input admittance with open-circuit output

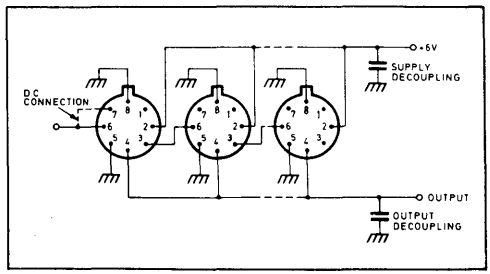


Fig. 8 Direct coupled amplifiers

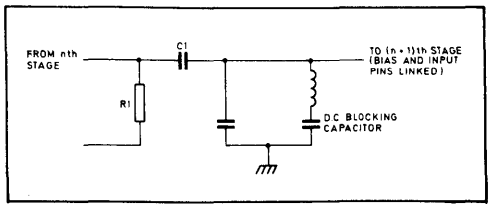


Fig. 9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guess-work.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals)

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6\text{mmhos (f = 10MHz)}$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 6 joined to pin 7 and
fed from 300 ohms source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}$ $\left[\frac{V_6}{V_2}\right]_a$ $\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6 dB/octave.

Plessey Semiconductors

SL530C

TRUE LOG. AMPLIFIER

GENERAL DESCRIPTION

The SL530C is a monolithic non-linear integrated circuit designed to realise a logarithmic transfer function in high-gain amplifier strips at frequencies between 4 and 80 MHz. THE DEVICE IS SO DESIGNED THAT INPUT SIGNAL PHASE INFORMATION IS RETAINED. A typical dynamic range of 70 dB can be achieved over a bandwidth of 10 MHz.

The operation of the SL530C relies upon the principle that amplifiers with an input/output characteristic as shown in Fig. 1 can be cascaded to produce the straight line approximation to a logarithmic law shown in Fig. 2. This may be represented by the expression:

$$V_{out} = K1 \ Log_{K2}\left(1 + \frac{V_{in}}{K3}\right)$$

Where K1, K2, K3 are scaling constants.

The logarithmic law remains true for any value of A or V_L (the breakpoint with respect to input or output) providing cascaded units are similar. It depends only upon the slope gain after limiting: this must be unity. Differences in this slope gain between the devices used in the strip will cause ripples in the log response, whilst the values of A, V_L and n determine the dynamic range available.

Dynamic Range

When Vin $\geq V_{LO}$ then all stages of the strip are operating in the unity gain mode. As n (the number of stages in the strip) is increased, the minimum input voltage for the onset of the logarithmic law is V_{LO}/A^n. The input dynamic range is therefore A^n or n20 logA dB. In other words, the dynamic range equals the low level strip gain.

If this level is as low as the effective noise input voltage, the addition of further stages does not result in any increase in dynamic range. For $R_S = 50\Omega$ the effective noise input voltage is approximately $3nV/\sqrt{Hz}$ The maximum dynamic range is thus given by:

$$\text{Dynamic Range} = \frac{V_{LO}}{3 \times 10^{-9}\sqrt{B}} \quad \text{Where B = Bandwidth}$$

$$\approx \frac{15 \times 10^6}{\sqrt{B(Hz)}} \qquad (V_{LO} \approx 45mV)$$

Hence for a bandwidth of 10 MHz, dynamic range = 73 dB, and the number of amplifier stages is six.

Unity Gain Slope

The logarithmic accuracy of a strip is dependent upon the consistent accuracy of this slope from device to device. The frequency response of the IC shows some peaking above 50 MHz but this may be reduced by a resistor in series with the output from pin 6. A typical value is between 0 and 50Ω.

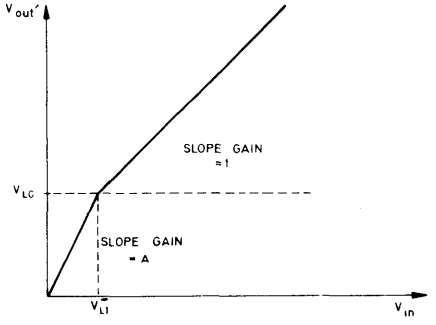


Fig. 1 Device transfer characteristic

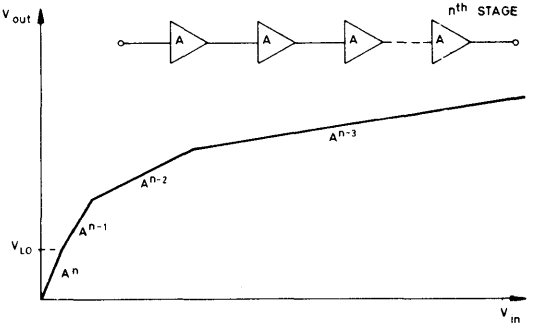


Fig. 2 n-stage strip-transfer characteristic

ELECTRICAL CHARACTERISTICS

Test Conditions: Positive supply 6 volts
Ambient temperature +22°C ± 2°C (unless otherwise stated)
D.C. connection Pin 4 to Pin 5
Output of each device loaded by input of next.

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
Midband gain low level	11.6	13.6	15.6	db	V_{in} = 2 mV rms, f = 30 MHz
Slope gain high level	−1	0	+1	dB	V_{in} = 100 mV rms, f = 30MHz
Upper cut-off frequency	60	90		MHz	−3dB w.r.t. f = 30 MHz
Lower cut-off frequency			4	MHz	−3dB w.r.t. f = 30 MHz
Phase change		±5.5	±12	Degrees	f = 30 MHz , V_{in} = 2 − 600mV rms.
Gain change		±0.5		dB	Vin = 100 mV, f = 30 MHz, T_A = −55°C to 125°C
Voltage at Pin 4 and Pin 5		1.75		V	Measured w.r.t. earth
Supply current		20	25	mA	

Note: Pins 3, 7, 8 are intended to enable system currents to be directed to their proper location, thus avoiding earth loops. All these pins must be at the same d.c. potential.

OPERATING NOTES

The layout should be in-line and compact, using physically small components. Provided this is the case an earth plane is not necessary even though the strip is boxed eventually. It may be necessary to use an input isolating transformer of 1:1 turns-ratio in which instance the box should only be connected to the outer screens of the co-axial connectors at input and output and to pin 7 of the output stage.

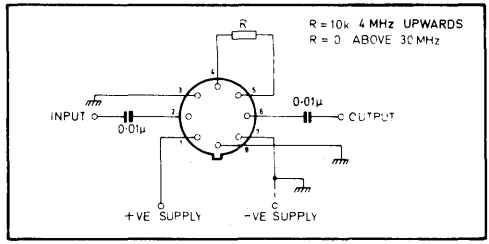


Fig. 3 Typical circuit connection

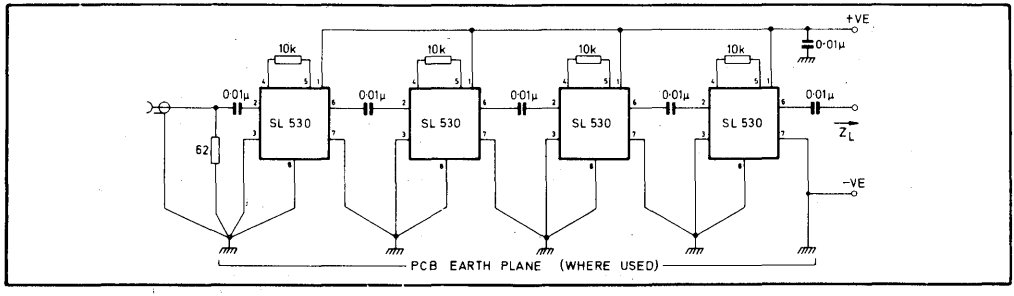


Fig. 4 Typical 4-stage strip

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	−55°C to +125°C
Storage temperature range	−55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Operating voltage Pin 2	3 V

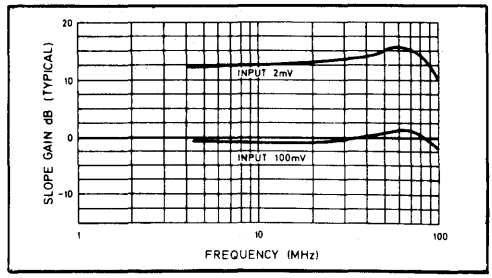


Fig. 5 Frequency response

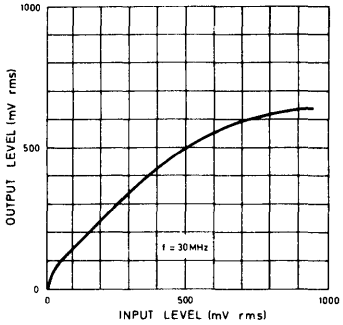


Fig. 6 Transfer characteristic

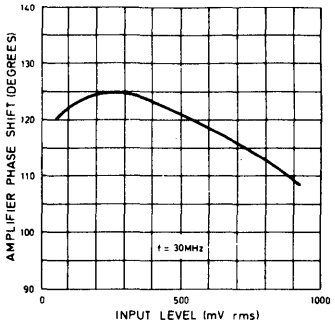


Fig. 7. Phase shift v. input

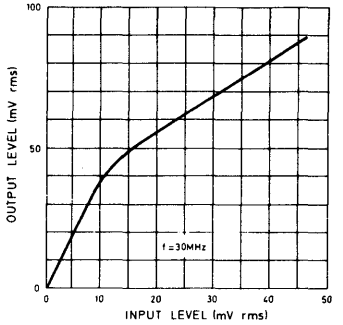


Fig. 8 Transfer characteristic

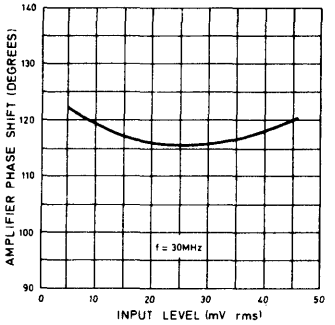


Fig. 9 Phase shift v. input

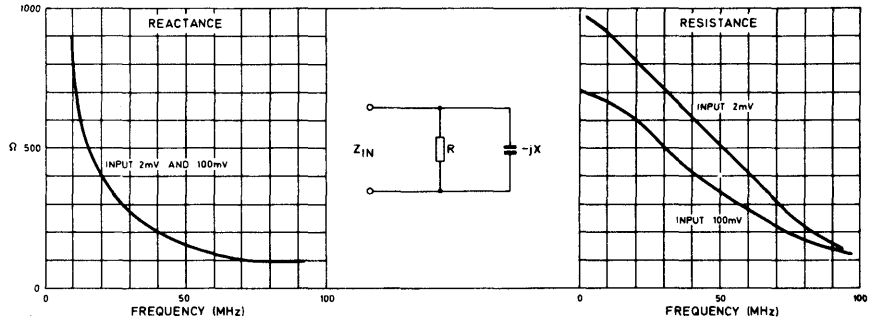


Fig. 10 Input impedance v. frequency

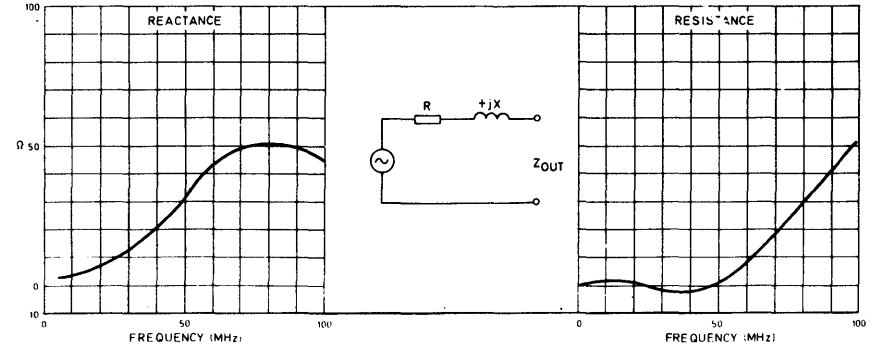


Fig. 11 Output impedance v. frequency

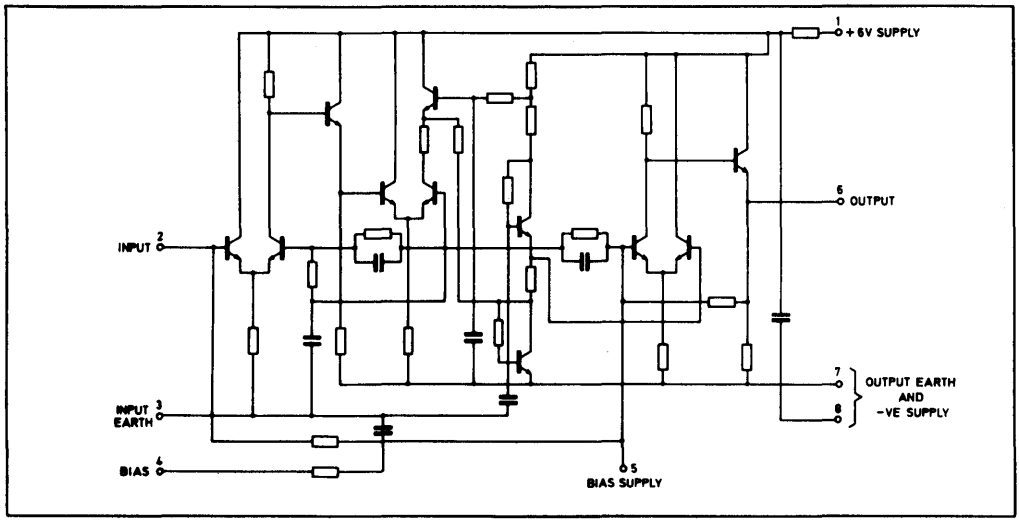


Fig. 12 SL530C circuit diagram
(equivalent only)

PLESSEY
Semiconductors

SL 500 SERIES
RADAR CIRCUITS

SL531C

TRUE LOG IF AMPLIFIER

The SL531C is a wide band amplifier designed for use in logarithmic IF amplifiers of the true log type. The input and log output of a true log amplifier are at the same frequency i.e. detection does not occur. In successive detection log amplifiers (using SL521, SL1521 types) the log output is detected.

The small signal gain is 10dB and bandwidth is over 500MHz. At high signal levels the gain of a single stage drops to unity. A cascade of such stages give a close approximation to a log characteristic at centre frequencies between 10 and 200MHz.

An important feature of the device is that the phase shift is nearly constant with signal level. Thus any phase information on the input signal is preserved through the strip.

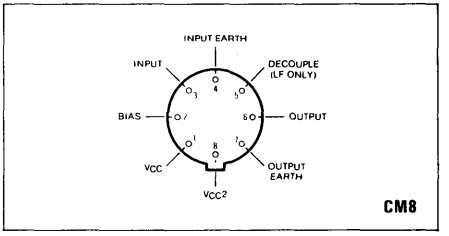


Fig. 1 Pin connections

FEATURES

- Low Phase Shift vs Amplitude
- On-Chip Supply Decoupling
- Low External Components Count

APPLICATIONS

True Log Strips with: –

- Log Range 70 dB
- Centre frequencies 10 – 200 MHz
- Phase Shift ± 0.5 degrees / 10 dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15 volts
Storage temperature range	−55°C to + 150°C
Operating temperature range	−55°C to +125°C
	See operating notes
Max junction temperature	150°C
Junction – ambient thermal resistance	220°C/Watt
Junction – case thermal resistance	80°C/Watt

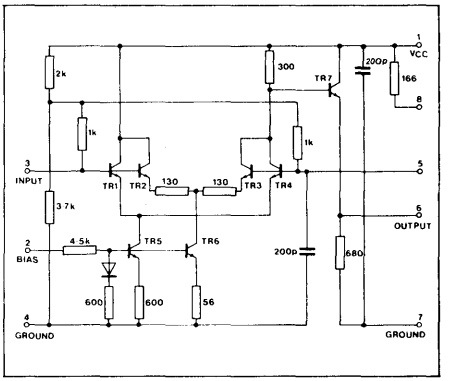


Fig. 2 Circuit diagram

CIRCUIT DESCRIPTION

The SL531 transfer characteristic has two regions. For small input signals it has a nominal gain of 10 dB, at large signals the gain falls to unity (see Fig 7). This is achieved by operating a limiting amplifier and a unity gain amplifier in parallel (see Fig 3). Tr1 and Tr4 comprise the long tailed pair limiting amplifier, the tail current being supplied by Tr5, see Fig 2. Tr2 and Tr3 form the unity gain amplifier the gain of which is defined by the emitter resistors. The outputs of both stages are summed in the 300 ohm resistor and Tr7 acts as an emitter follower output buffer. Important features are the amplitude and phase linearity of the unity gain stage which is achieved by the use of 5GHz transistors with carefully optimised geometries.

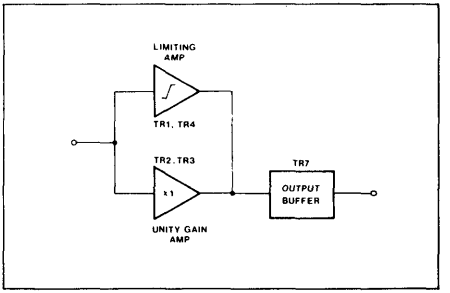


Fig. 3 Block diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Test circuit Fig (4)
Frequency 60 MHz
Supply voltage 9 volts
Ambient temperature 22± 2°C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Small signal voltage gain	8	10	12	dB	Vin = −30 dBm
High level slope gain	−1	0	+1	dB	
Upper cut off frequency	250	500		MHz	
Lower cut off frequency		3	10	MHz	−3dB w.r.t. ± 60 MHz
Supply current		17	25	mA	
Phase change with input amplitude		1.1	3	degrees	Vin − 30 dBm to + 10 dBm
Input impedance	2.5pf parallel with 1k				10 − 200MHz
Output impedance	15Ω series with 25nh				

OPERATING NOTES

1. Supply Voltage Options

An on chip resistor is provided which can be used to drop the supply voltage instead of the external 180 ohms shown in the test circuit. The extra dissipation in this resistor reduces the maximum ambient operating temperature to 100°C. It is also possible to use a 6 volt supply connected directly to pins 1 and 2. Problems with feedback on the supply line etc may occur in this connection and RF chokes may be required in the supply line between stages.

2. Layout Precautions

The internal decoupling capacitors help prevent high frequency instability, however normal high frequency layout precautions are still necessary. Coupling capacitors should be physically small and be connected with short leads. It is most important that the ground connections are made with short leads to a continuous ground plane.

3. Low Frequency Response

The LF response is determined by the on chip capacitors. It can be extended by extra external decoupling on pins 5 and 1.

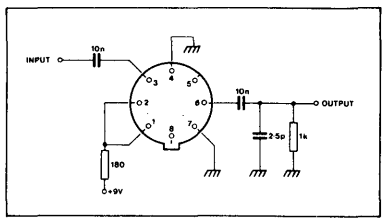


Fig. 4 Test circuit

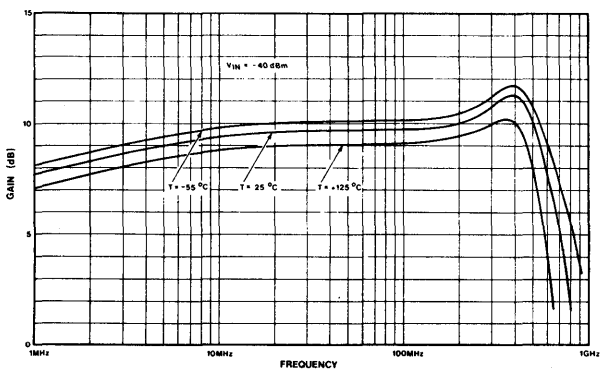


Fig. 5 Small signal frequency response

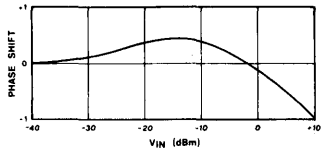


Fig. 6 Phase v. input

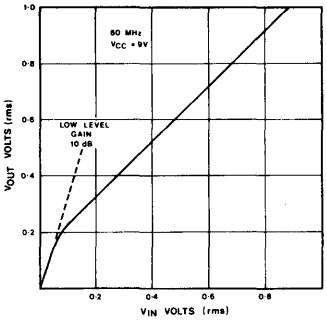


Fig. 7 Transfer characteristics linear plot

TYPICAL APPLICATION — 6 STAGE LOG STIP

Input log range 0dBm to −70dBm
Low level gain 60dB (−70dBm in)
Output dynamic range 20dB
Phase shift (over log range) ±3°
Frequency range 10 — 200MHz

The circuit shown in Fig 9 is designed to illustrate the use of the SL531 in a complete strip. The supply voltage is fed to each stage via an external 180Ω resistor to allow operation to 125°C ambient. If the ambient can be limited to + 100°C then the internal resistor can be used to reduce the external component count. Interstage coupling is very simple with just a capacitor to isolate bias levels being necessary. No connection is necessary to pin 5 unless operation below 10MHz is required. It is important to provide extra decoupling on pin 1 of the first stage to prevent positive feedback occuring down the supply line. An SL560 is used as a unity gain buffer, the output of the log strip being attenuated before the SL560 to give a nominal 0dBm output into 50Ω.

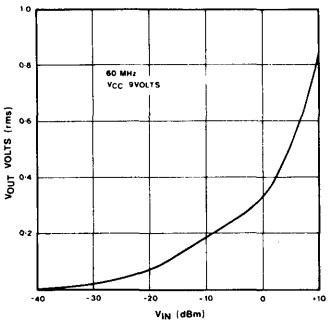


Fig. 8 Transfer characteristics logarithmic input scale

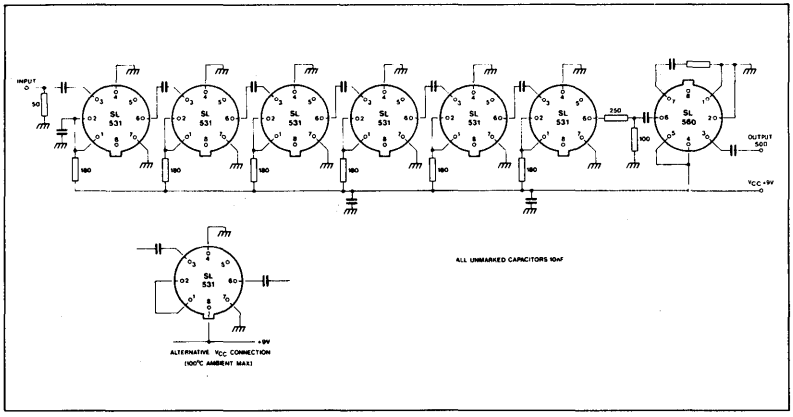


Fig. 9 Circuit diagram 6 stage strip

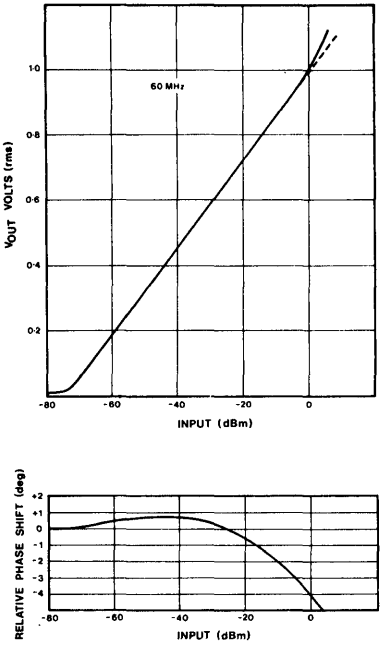


Fig. 10 Transfer function of log strip

SL532C

LOW PHASE SHIFT LIMITER

The SL532C is a monolithic integrated circuit designed for use in wide band limiting IF strips. It offers a bandwidth of over 400MHz and very low phase shift with amplitude. The small signal gain is 12dB and the limited output is 1 volt peak to peak. The use of a 5GHz IC process has produced a circuit which gives less than 1o phase shift when overdriven by 12dB. The amplifier has internal decoupling capacitors to ease the construction of cascaded strips and the number of external components required has been minimised.

FEATURES

Low phase shift vs Amplitude

Wide bandwidth

Low external components count

APPLICATIONS

Phase recovery strips in Radar and ECM systems

Limiting Amps for SAW pulse compression systems

Phase monopulse radars

Phased array radars

ABSOLUTE MAXIMUM RATINGS

Supply voltage +15 volts

Storage temperature range - 55°C to +150°C

Operating temperature range - 55°C to +125°C

CIRCUIT DESCRIPTION

The SL532C uses a long-tailed limiting amplifier which combines low phase shift with a symmetrical limiting characteristic. This is followed by a simple emitter follower output stage. Each stage of a strip is capable of driving to full output a succeeding SL532 but a buffer amplifier is needed to drive lower impedance loads. No external decoupling capacitors are normally required but for use below 10MHz extra decoupling can be added on pins 1 and 5. Bias for the long-tailed pair is provided by connecting the bias (pin 2) to the decoupled supply (pin 1).

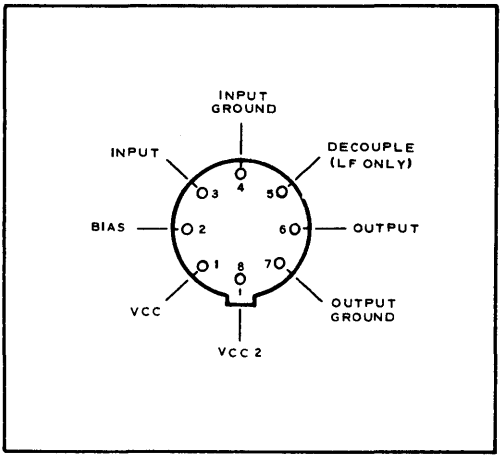


Fig 1. Pin connections

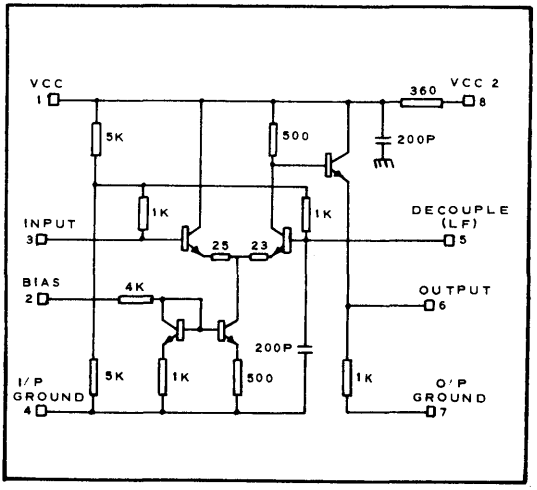


Fig 2. Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Temperature (Ambient) 25°C
Frequency 60MHz
Vcc = +9V
RL = IK

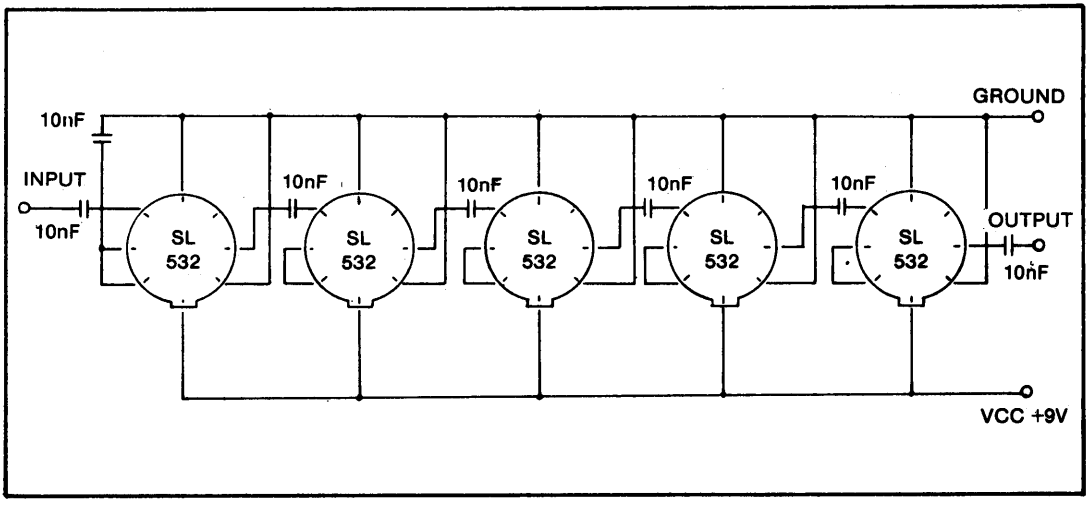
Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Small signal voltage gain	10	12	14	dB	
Limited OP voltage		1		Vpk–pk	
Upper cut off frequency		400		MHz	
Lower cut off frequency		10		MHz	Can be lowered with external capacitors
Supply current		10	15	mA	
Phase variation with signal level		±1		degree	Vin = 60dB – +10 dBm
Input Impedance		1.3		KΩ	
Output Impedance		10		Ω	
Max Input Signal before overload		+20		dBm	
Gain variation with temperature		1		dB	55°C to + 125°C

TYPICAL APPLICATION — 5 STAGE STRIP

Input signal for full limiting { 300 μV rms / –57 dBm

Limited output 1 v pk – pk

Phase shift (Vin –57→+ 19dBm) + 3°typ



Five stage IF strip.

SL541A & B

HIGH SLEW RATE OPERATIONAL AMPLIFIERS

The SL 541 is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compression is required. Both the SL541A and SL541B have a guaranteed input offset voltage of ±5V maximum.

FEATURES

- High Slew Rate: 175V/μs
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB (SL541B), 54DB(SL541A)
- Wide Bandwidth: DC to 100MHz at 20dB Gain
- Very Low Thermal Drift: 0.02dB/°C
  Temperature Coefficient of Gain
- Guaranteed 5mV input offset maximum
- Full Military Temperature Range (DIL Only)
- Package: 10 Lead TO–5
  14 Lead DIL Ceramic

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

ABSOLUTE MAXIMUM RATING

Supply voltage (V+ to V–)		24V
Input voltage (Inv. I/P to non inv. I/P)		9V
Storage temperature		–55 C to +175 C
Chip operating temperature		+175 C
Operating temperature:		TO-5: –55 C to +85 C
		DIL: –55 C to +125 C
Thermal resistances		
Chip-to-ambient:	TO-5	220 C/W
	DIL	125 C/W
Chip-to-case:	TO-5	60 C/W
	DIL	40 C/W

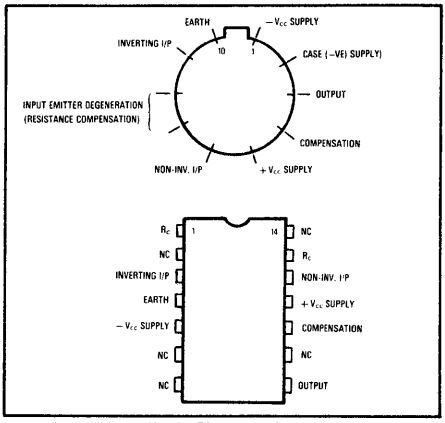


Fig. 1 Pin connections

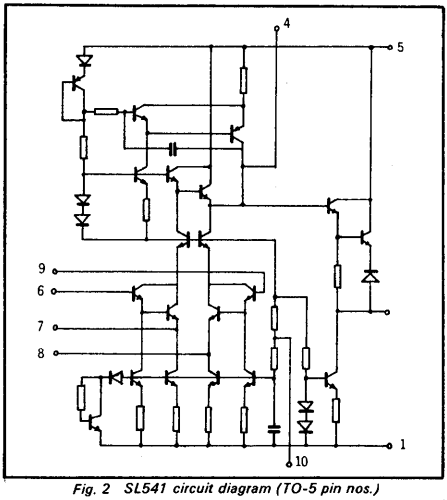


Fig. 2 SL541 circuit diagram (TO-5 pin nos.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Tamb = 25°C

SL541A
+VCC = 15V
−VCC = −4V
Pins 7 and 8 (TO−5) Short circuit
13 and 1 (DIL)
1kΩ pin 10 to 3 (TO−5)
1kΩ pin 4 to 8 (DIL)

SL541B
+VCC = 12V
−VCC = −6V
Pins 7 and 8 (TO−5) Short circuit
13 and 1 (DIL)
Pin 10 (TO−5) Earth
Pin 4 (DIL) Earth

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Stactic nominal supply current	A,B		16	21	mA	
Input bias current	A,B		7	25	uA	
Input offset voltage	A,B			5	mV	
Dynamic open loop gain	A	45	54		dB	600Ω load
Open loop temperature coefficient	A,B		−0 02		dB/°C	
Closed loop bandwidth (−3dB)	A,B		100		MHz	X10 gain
Slew rate (4V peak)	A,B	100	175		V/μs	X10 gain
Settling time to 1%	A,B		50	100	ns	
Maximum output voltage						
(+ve)	A	5.5	5 7		V	
(−ve)	A		−1.9	−1.5	V	
(+ve)	B	2. 5	3. 0		V	
(−ve)	B		−3.0	−2.5	V	
Maximum output current	A,B	4	6.5		mA	
Maximum input voltage						
(+ve)	A			5	V	Non inverting modes
(−ve)	A	−1			V	
(−ve)	B			3	V	
(+ve)	B	−3			V	
Supply line rejection						
(+ve)	A,B	54	66		dB	
(−ve)	A B	46	54		dB	

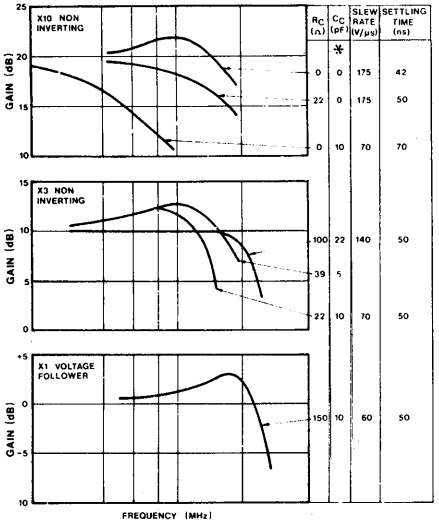


*Fig. 3 Performance graphs – gain v. frequency (load 2kΩ/10pF) * See operating note 2*

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators ect.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitros should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance (< 1kΩ), as seen from pins 6 and 9–100Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect-. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty in the clipping levels results, but the speration remains. However, the supply line rejection is improved if pin 10 can be left open−circuit.

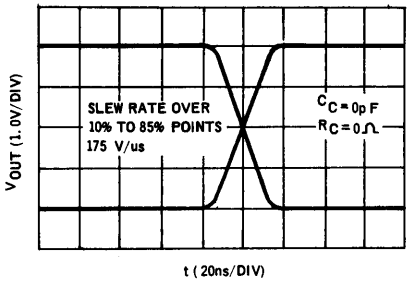


Fig. 4 Slew rate –X10 non–inverting mode Input square wave 0.4V p/p

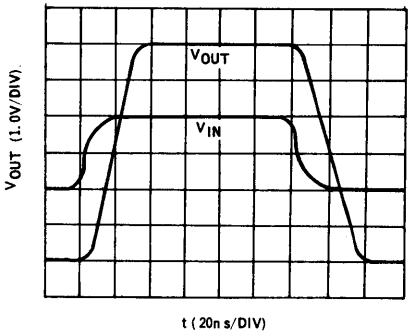


Fig. 6 Output clipping levels –X10 non– inverting mode Input moderately overdriven, so that output goes into clipping both side

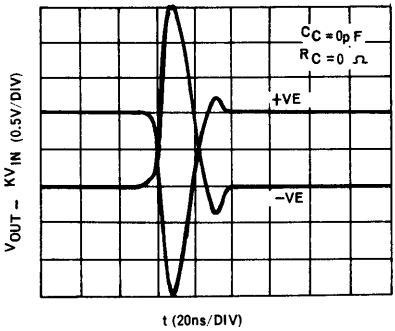


Fig. 5 Settling time –X10 non–inverting mode

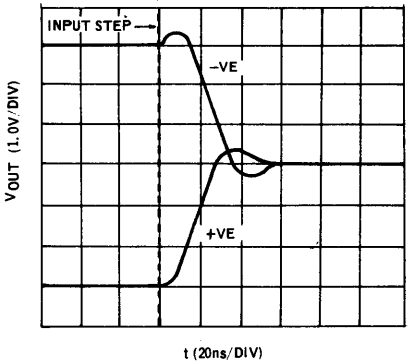


Fig. 7 Output clippings levels –X10 non–inverting mode. Output goes from clipping to zero volts. Vin=3V peak step, offset +ve or –ve.

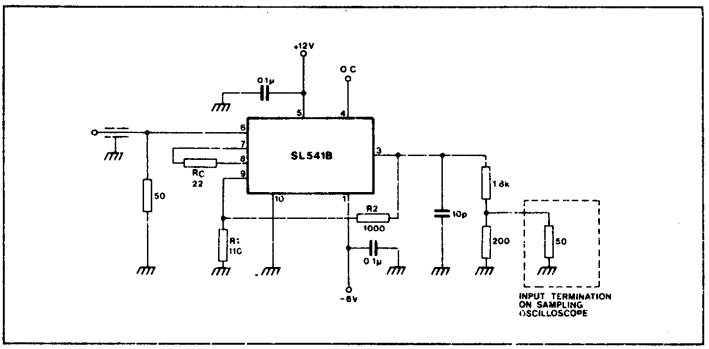


Fig. 8 Non–inverting high speed X10 amplifier test circuit. (TO–5 pin nos)

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time which is often more dependent upon the teat circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (fp) by the relationship.

$$S = 2\pi f_p E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vincinity of some value of output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for a slew rate in a X10 gain configuration.

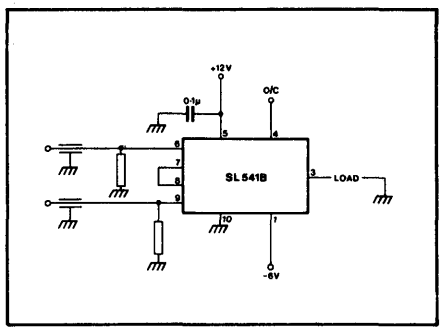


Fig. 9 Non–saturating sense amplifier (30V/μs for 5mV) Note: the output may be caught at a pre–determined level. (TO–5 pin nos.)

Plessey Semiconductors

SL500 SERIES

WIDEBAND AMPLIFIERS

SL541C & D

HIGH SPEED VIDEO AMPLIFIER

The SL541C is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain (70dB) is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required. The package of the C varient is internally connected to the negative supply. The D varient package (CM10 only) is isolated.

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

FEATURES

- High Slew Rate: 175V/μs
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB
- Wide Bandwidth: DC to 100MHz at 20dB Gain
- Very Low Thermal Drift: 0.02dB/°C Temperature Coefficient of Gain

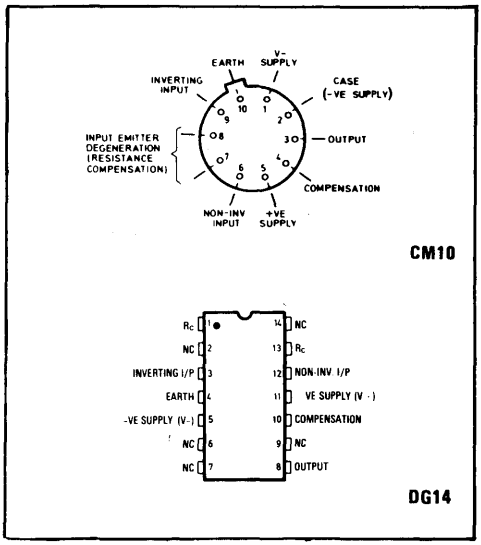


Fig. 1 Pin connections

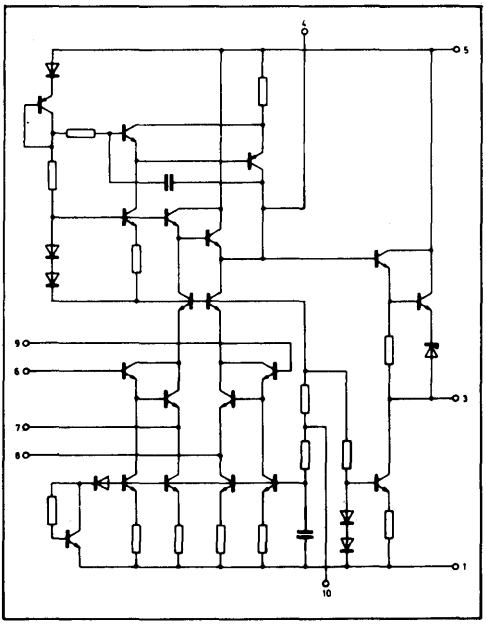


Fig. 2 SL541 circuit diagram (TO – 5 pin nos.)

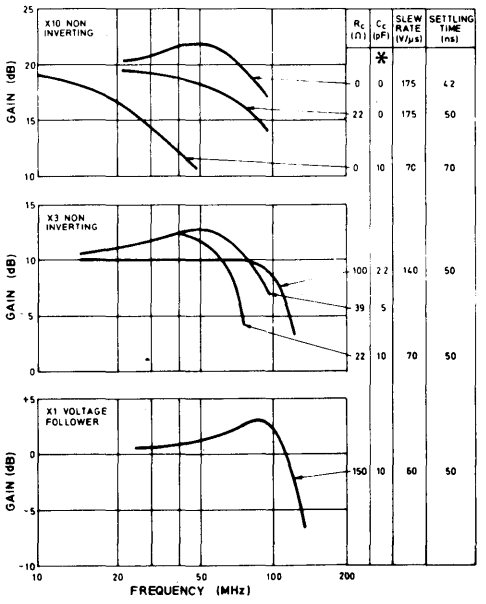


Fig. 3 Performance graphs – gain v. frequency (load = 2kΩ//10pF)

** See operating note 2*

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Pin 5: +12V
Pin 1: −6V
Pins 7 & 8: Connected together
T_{amb}: 25°C

Characteristic	Value			Units	Test Conditions
		Typ.	Max.		
Static nominal supply current	—	16	21	mA	
Input bias current	—	7	15	μA	
Dynamic open loop gain	60	71	—	dB	600Ω Load
Open loop temp. co-efficient		−0.02		dB/°C	
Closed loop bandwidth (−3dB)		100		MHz	x 10 gain
Slew rate (4V peak)	100	175		V/μs	x 10 gain
Settling time to 1%		50	100	ns	
	±2.5	±3.0		V	
	4	6.5		mA	
Maximum input voltage	—		±3	V	Non-inverting mode
Supply line rejection (pin 5)	54	66		dB	
(pin 1)	46	54		dB	

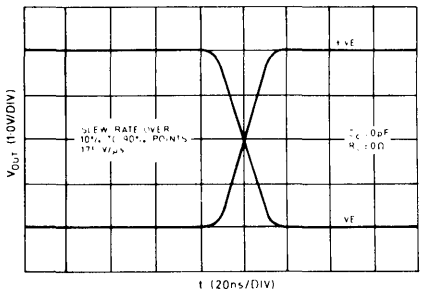


Fig. 4 Slew rate - X10 non-inverting mode

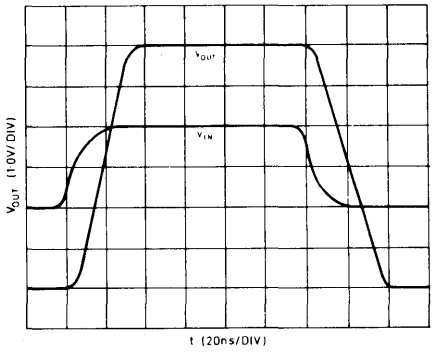


Fig. 6 Output clipping levels – X10 non-inverting mode Input moderately overdriven, so that ouput goes into clipping both sides

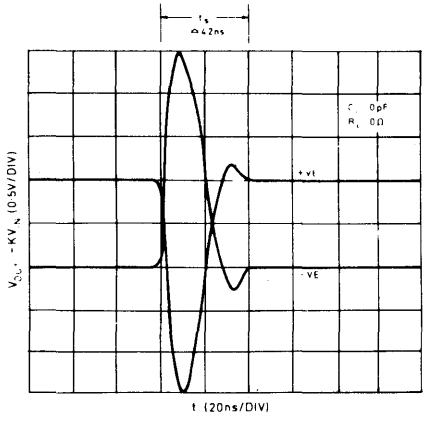


Fig. 5 Settling time – X10 non-inverting mode

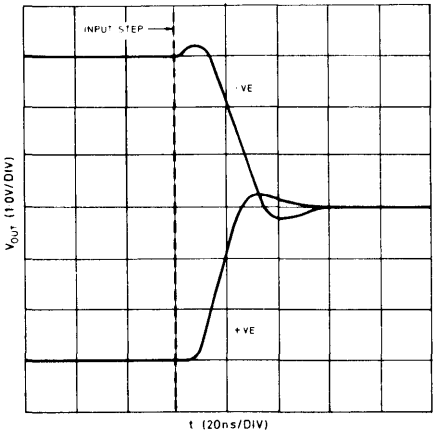


Fig. 7 Output clipping levels – X10 non-inverting mode. Output goes from clipping to zero volts. V_{in} = 3V peak step, offset +ve or −ve.

TEST CONDITIONS AND DEFINITIONS

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time, which is often more dependent upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (f_p) by the relationship.

$$S = 2\pi f_p' E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of some value of output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for slew rate in a X10 gain configuration.

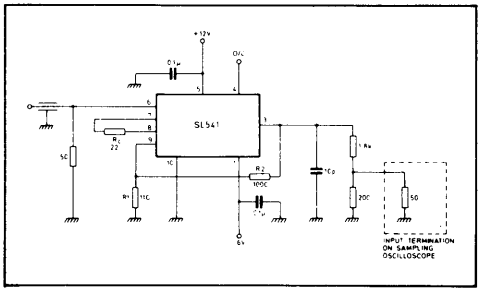


Fig. 8 Non-inverting high speed X10 amplifier test circuit. (TO – 5 pin nos.)

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance ($\leqslant 1k\Omega$), as seen from pins 6 and 9 – 100Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty in the clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open-circuit.

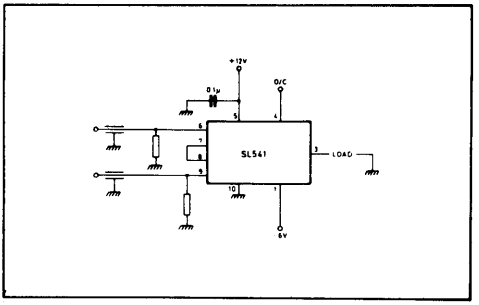


Fig. 9 Non-saturating sense amplifier (30V/μs for 5mV). Note: the output may be caught at a pre-determined level. (TO – 5 pin nos.)

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V^+ to V^-)	24V
Input voltage (Inv.I/P to non inv.I/P)	+9V
Storage temperature	—55°C to +175°C
Chip operating temperature	+175°C
Operating temperature: TO — 5	—55°C to +85°C
DIL	—55°C to +125°C

Thermal resistances

Chip-to-ambient: TO — 5	220°C/W
DIL	125°C/W
Chip-to-case: TO — 5	60°C/W
DIL	40°C/W

SL550 C & D

LOW NOISE WIDEBAND AMPLIFIER WITH EXTERNAL GAIN CONTROL

The SL550 is a silicon integrated circuit designed for use as a general-purpose wideband linear amplifier with remote gain control. At a frequency of 60 MHz, the SL550C noise figure is 1,8dB (typ.) from a 200 ohm source, giving good noise performance directly from a microwave mixer. The SL550 has an external gain control facility which can be used to obtain a swept gain function and makes the amplifier ideal for use either in a linear IF strip or as a low noise preamplifier in a logarithmic strip.

External gain control is performed in the feedback loop of the main amplifier which is buffered on the input and output, hence the noise figure and output voltage swing are only slightly degraded as the gain is reduced. The external gain control characteristic is specified with an accuracy of ±1dB, enabling a well-defined gain versus time law to be obtained.

The input transistor can be connected in common emitter or common base and the quiescent current of the output emitter follower can be increased to enable low impedance loads to be driven.

FEATURES

- 200 MHz Bandwidth
- Low Noise Figure
- Well-Defined Gain Control Characteristic
- 25dB Gain Control Range
- 40dB Gain
- Output Voltage 0.8Vp-p (Typ.)

APPLICATIONS

- Low Noise Preamplifiers
- Swept Gain Radar IFs

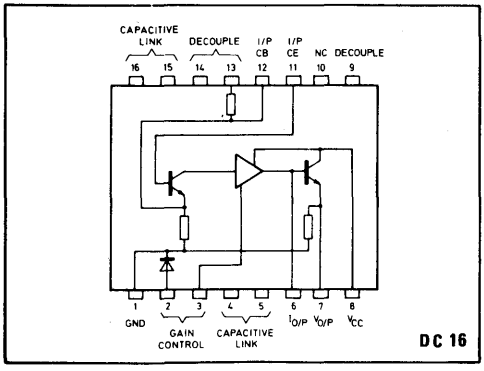


Fig. 1 Pin connections (top view)

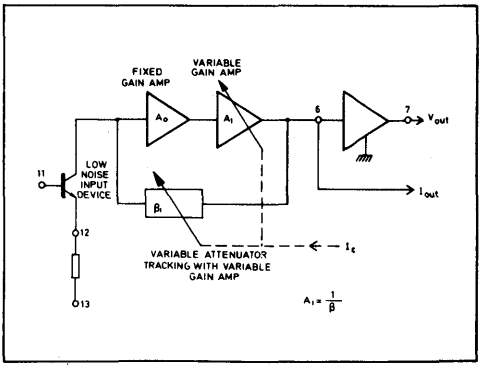


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
f=30MHz V_S = 6V, R_L = 200Ω, I_C = O, R_1 = 750Ω, T_{amb} = + 25°C

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain	SL550C	39	42	44	dB	
	SL550D	35	40	45	dB	
Gain control characteristic	Both		See note 1			
Gain reduction at mid-point	SL550C	9	10	11	db	I_C = 0.2mA
	SL550D		9		dB	I_C = 0.2mA
Max. gain reduction	SL550C	20	25		dB	I_C = 2.0mA
	SL550D		25		dB	I_C = 2.0mA
Noise figure	SL550C		2.0	2.7	dB	R_S = 200Ω
	SL550C		3.5		dB	R_S = 50Ω
	SL550D		3.0		dB	R_S = 200Ω
Output voltage	Both		0.15		Vrms	R_1 = ∞
	Both		0.3		Vrms	R_1 = 750Ω
Supply current	SL550C		11	13	mA	R_1 = ∞
	SL550C		15		mA	R_1 = 750Ω
	SL550D		11	20	mA	R_1 = ∞
Gain variation with supply voltage	Both		0.2		dB/V	V_S = 6 to 9V
Upper cut-off frequency (—3dB wrt 30MHz)	Both		125		MHz	
Gain variation with temperature (see note 2)	Both		±3		dB	T_{amb} = —55 to +125°C

NOTES
1. The external gain control characteristic is specified in terms of the gain reduction obtained when the control current (I_C) is increased from zero to the specified current.
2. This can be reduced by using an alternative input configuration (see operating note: 'Wide Temperature Range').

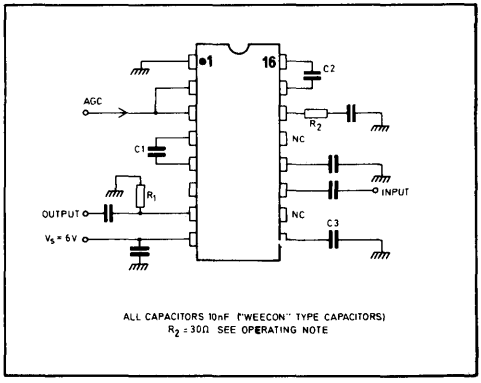


Fig. 3 Test circuit

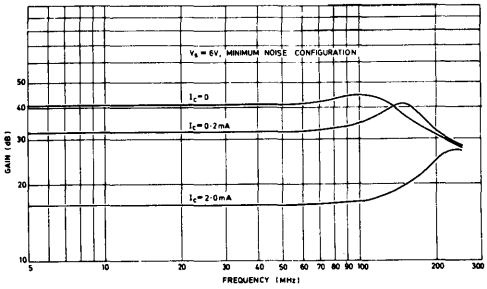


Fig. 4 Frequency response

OPERATING NOTES

Input Impedance

The input capacitance, which is typically 12pF at 60MHz, is independent of frequency. The input resistance, which is approximately 1.5k at 10MHz, decreases with frequency and is typically 500 ohms at 60MHz

Control Input

Gain control is normally achieved by a current into pin 2. Between pin 2 and ground is a forward biased diode and so the voltage on pin 2 will vary between 600 mV at I_C = 1 μA to 800 mV at I_C = 2 mA. The amplifier gain is varied by applying a voltage in this range to pin 3. To avoid problems associated with the sensitivity of the control voltage and with operation over a wide temperature range the diode should be used to convert a control current to a voltage which is applied to pin 3 by linking pins 2 and 3.

Minimum Supply Current

If the full output swing is not required, or if high impedance loads are being driven, the current consumption can be reduced by omitting R_1 (Fig. 3). The function of R_1 is to increase the quiescent current of the output emitter follower.

High Output Impedance

A high impedance current output can be obtained by taking the output from pin 6 (leaving pin 7 open-circuit). Maximum output current is 2 mA peak and the output impedance is 350Ω.

Wide Temperature Range

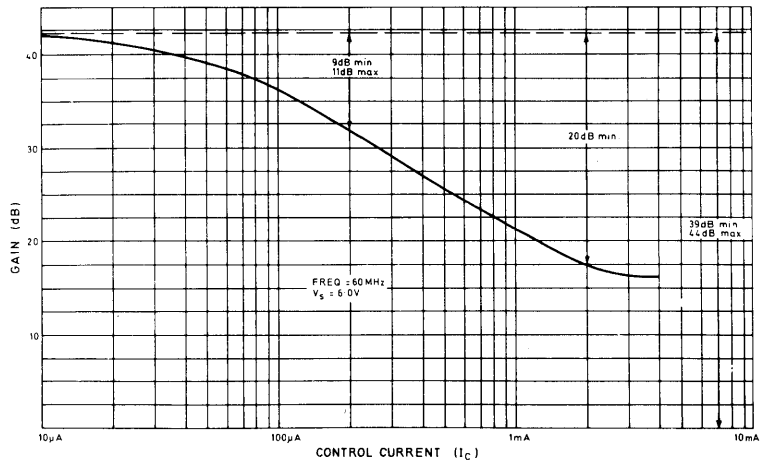
The gain variation with temperature can be reduced at the expense of noise figure by including an internal 30Ω resistor in the emitter of the input transistor. This is achieved by decoupling pin 13 and leaving pin 12 open-circuit. Gain variation is reduced from ±3dB to ±1dB over the temperature range −55°C to +125°C (Figs. 6 and 7)

Low Input Impedance

A low input impedance ($\simeq$ 25Ω) can be obtained by connecting the input transistor in common base. This is achieved by decoupling pin 11 and applying the input to pin 12 (pin 13 open-circuit).

High Frequency Stability

Care must be taken to keep all capacitor leads short and a ground plane should be used to prevent any earth inductance common between the input and output circuits. The 30Ω resistor (pin 14) shown in the test circuit eliminates high frequency instabilities due to the stray capacitances and inductances which are unavoidable in a plug-in test system. If the amplifier is soldered directly into a printed circuit board then the 30Ω resistor can be reduced or omitted completely.



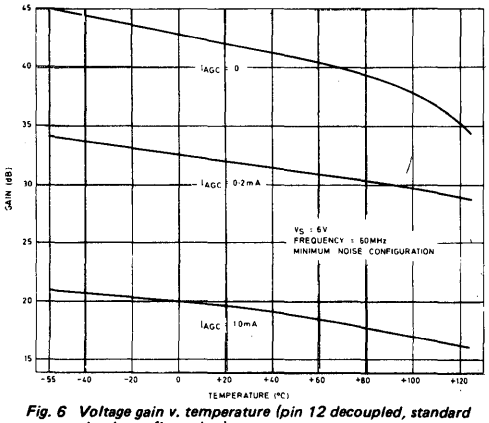


Fig. 6 Voltage gain v. temperature (pin 12 decoupled, standard circuit configuration).

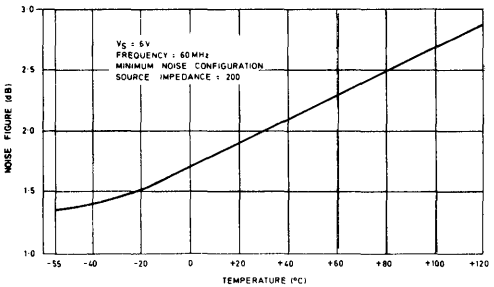


Fig.8 Typical noise figure (SL550C)

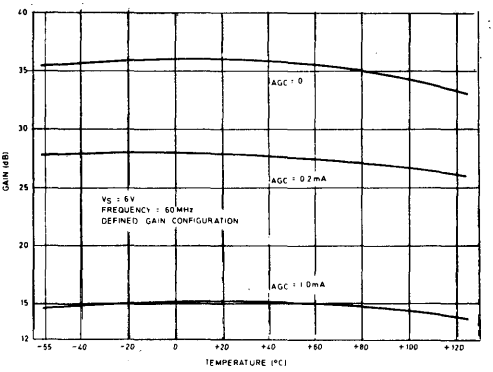


Fig. 7 Voltage gain v. temperature (pin 13 decoupled for improved gain variation with temperature – see operating notes).

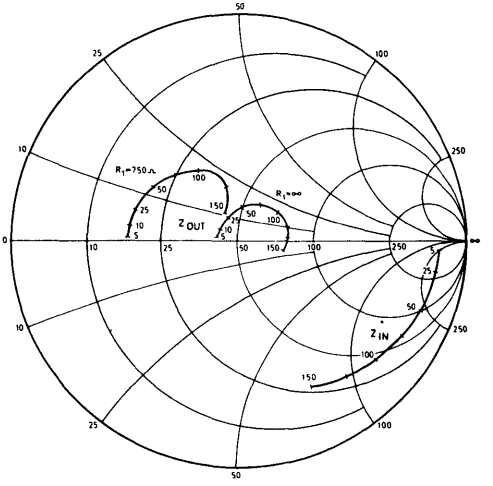


Fig. 9 Input and output impedances (V_S = 6V)

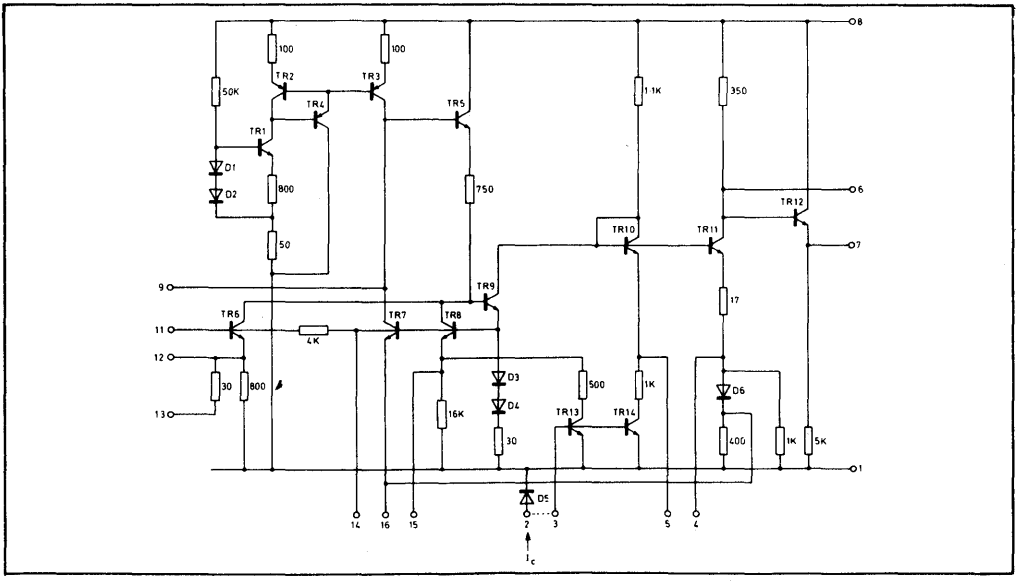


Fig. 10 Circuit diagram

APPLICATION NOTES

A wideband high gain configuration using two SL550s connected in series is shown in Fig. 11. The first stage is connected in common emitter configuration, whilst the second stage is a common base circuit. Stable gains of up to 65 dB can be achieved by the proper choice of R1 and R2. The bandwidth is 5 to 130 MHz, with a noise figure only marginally greater than the 2.0 dB specified for a single stage circuit.

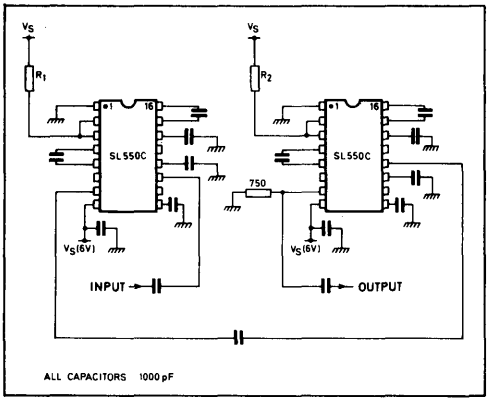


Fig. 11 A two-stage wideband amplifier

A voltage gain control which is linear with control voltage can be obtained using the circuit shown in Fig. 12. The input is a voltage ramp which is negative going with respect to ground. The output drives the control current pins 2 and 3 directly (see Fig. 13). If two SL550s in the strip are controlled as shown in Fig. 14, with a linear ramp input to the linearising circuit, a fourth power law (power gain v. time) will be obtained over a 50 dB dynamic range.

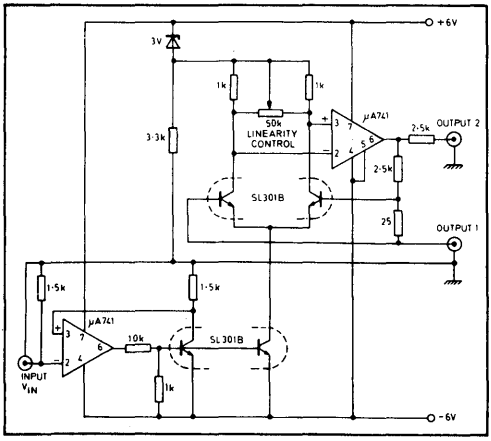


Fig. 12 Gain control linearising circuit.

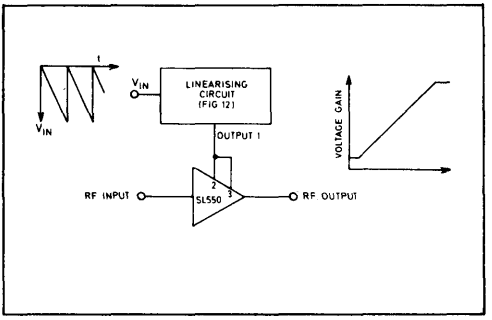


Fig. 13 Linear swept gain circuit

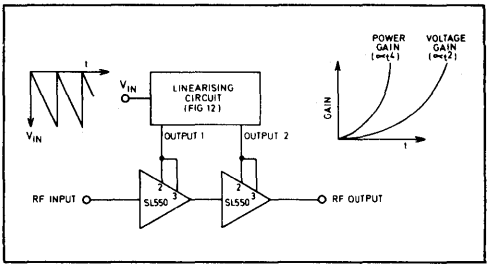
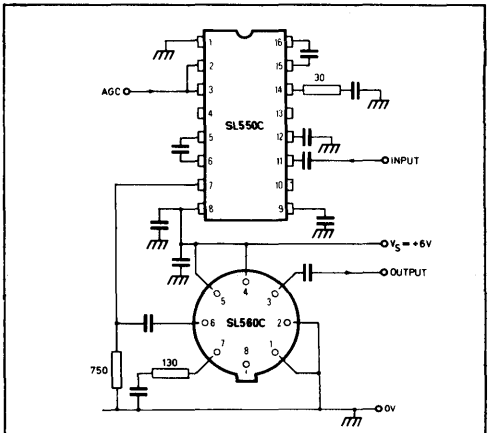


Fig. 14 Square law swept gain circuit.



All capacitors 10nF
Gain 46dB
Noise figure 2.0dB (RS = 200 Ω)
Output power +5dBm (R1 = 50 Ω)
Frequency response as SL550C
Dynamic range 70dB (1MHz bandwidth)

Fig.15 Applications example of wide dynamic range: 50 Ω load amplifier with AGC using SL500 series integrated circuit.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Ambient operating temp.	−40°C to +125°C
Max. continuous supply Voltage wrt pin 1	+9V
Max. continuous AGC current	
pin 2	10mA
pin 3	1mA

PLESSEY
Semiconductors

SL560C

300 MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300 MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL 560C is a general-purpose low noise, high frequency gain block.

FEATURES (Non-simultaneous)

- Gain up to 40 dB
- Noise Figure Less Than 2 dB (R_S 200 ohm)
- Bandwidth 300 MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

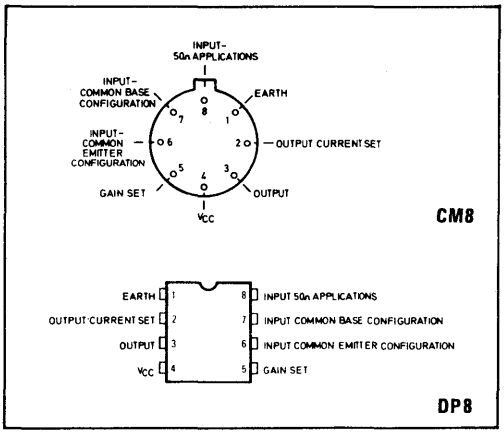


Fig. 1 Pin connections (viewed from beneath)

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range RF Amplifiers

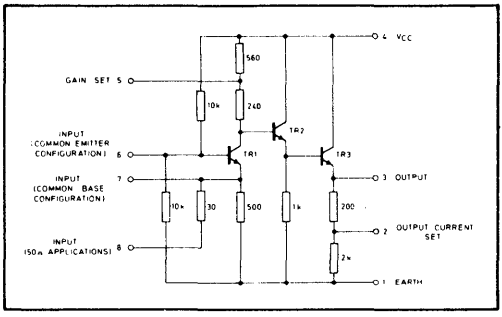


Fig. 2 SL560C circuit diagram

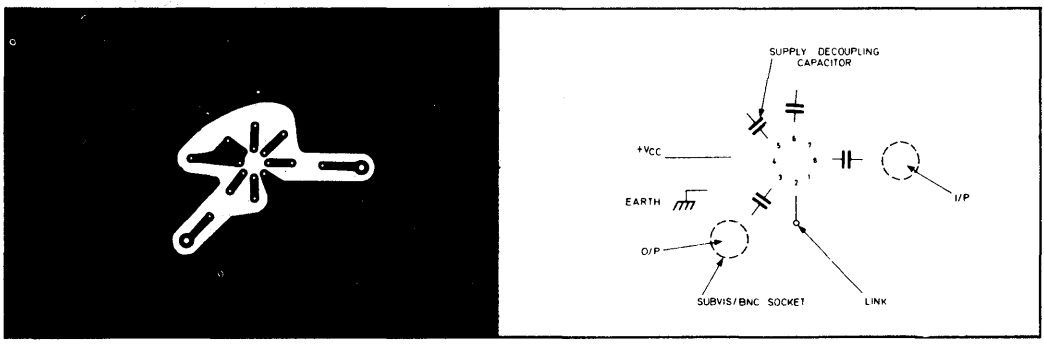


Fig. 3 PC layout for 50-Ω line driver (see Fig. 6)

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Frequency 30 MHz
V_{CC} 6V
$R_S = R_L = 50\Omega$
$T_A = 25°C$
Test Circuit: Fig. 6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	10	14	18	dB	
Gain flatness		±1.5		dB	10 MHz — 220 MHz
Upper cut-off frequency		250		MHz	
Output swing	+4	+7	+8	dBM	V_{CC} = 6V } See Fig. 5
		+11		dBm	V_{CC} = 9V }
Noise figure (common emitter)		1.8		dB	$R_S = 200\Omega$
		3.5		dB	$R_S = 50\Omega$
Supply current	15	20	32	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17 ohms (for low noise operation) with a small physical size — giving a transition frequency, f_T, in excess of 1 GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2 dB noise figure (R_S 200 Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75 MHz (see Figs. 8 and 9) or, using feedback, 14 dB with a bandwidth of 300 MHz (see Figs. 10 and 11).

Because the transistors used in the SL 560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

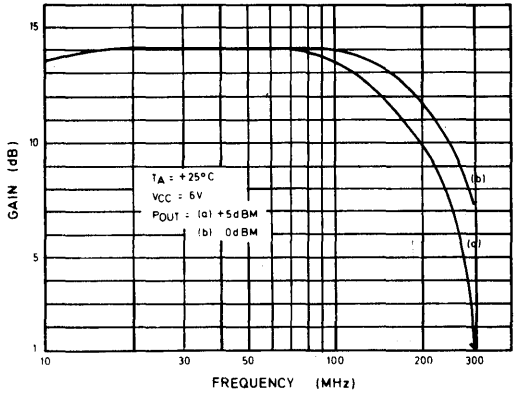


Fig. 4 Frequency response, small signal gain

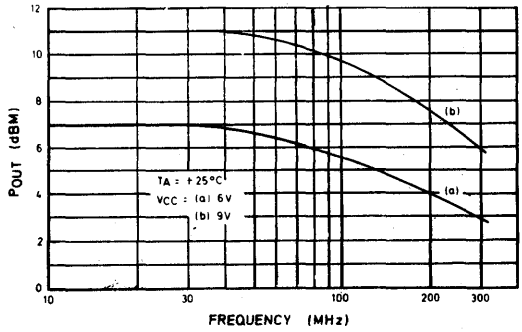


Fig. 5 Frequency response, output capability (loci of maximu output power with frequency, for 1dB gain compressic

TYPICAL APPLICATIONS

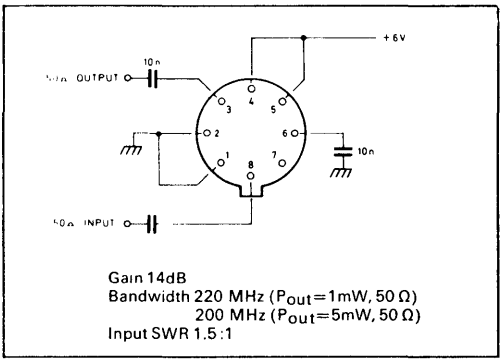


Fig. 6 50 Ω line driver. The response of this configuration is shown in Fig. 4.

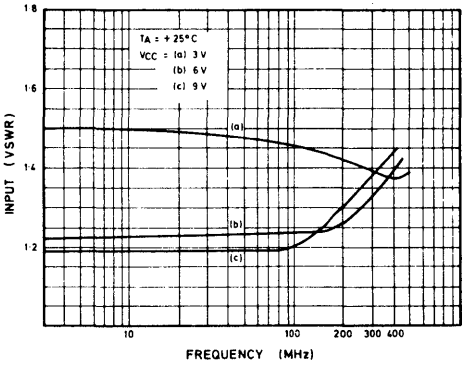


Fig. 7 Input standing wave ratio plot of circuit shown in Fig. 6

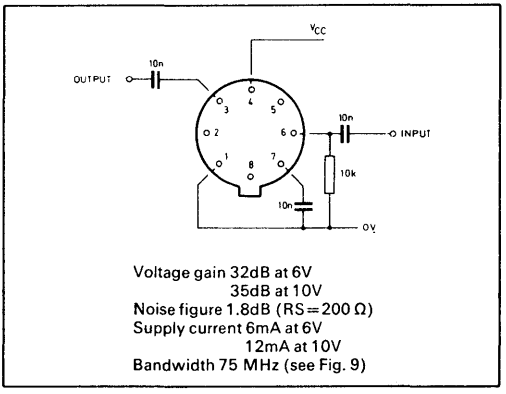


Fig. 8 Low noise preamplifier

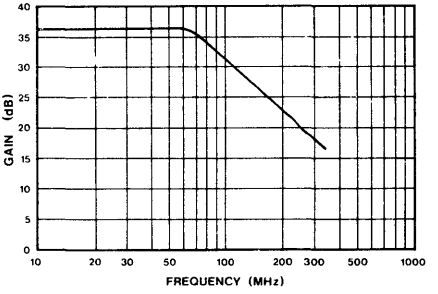


Fig. 9 Frequency response of circuit shown in Fig. 8

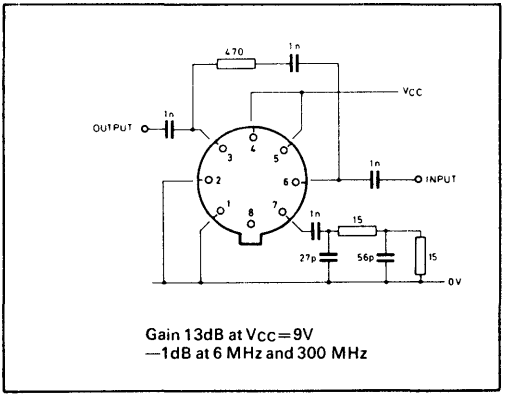


Fig. 10 Wide bandwidth amplifier

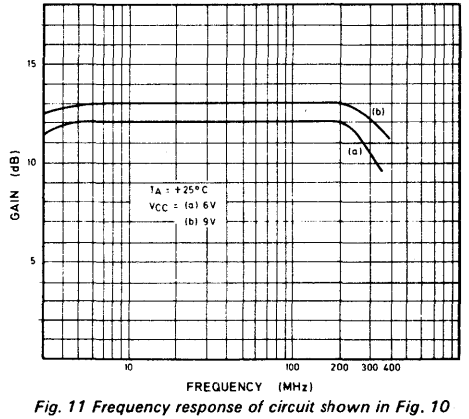


Fig. 11 Frequency response of circuit shown in Fig. 10

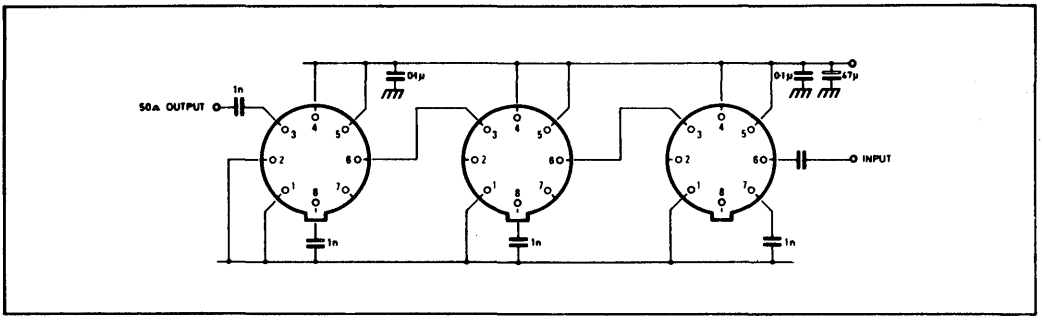


Fig. 12 Three-stage directly-coupled high gain low noise amplifier

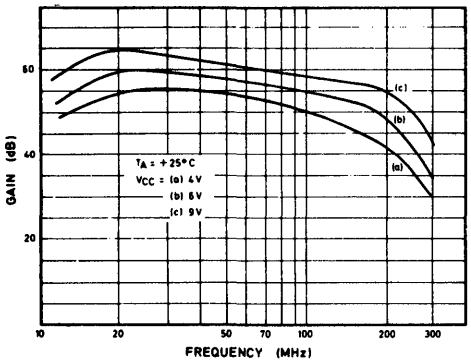
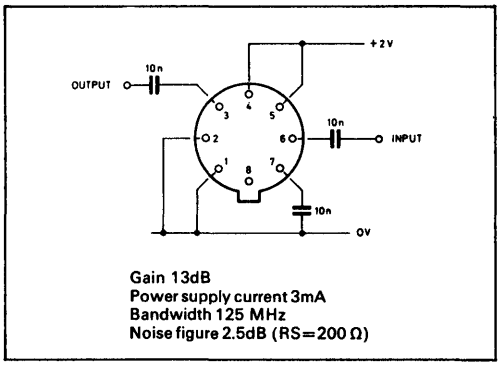


Fig. 13 Frequency response of circuit shown in Fig. 12



Gain 13dB
Power supply current 3mA
Bandwidth 125 MHz
Noise figure 2.5dB (RS=200 Ω)

Fig. 14 Low power consumption amplifier

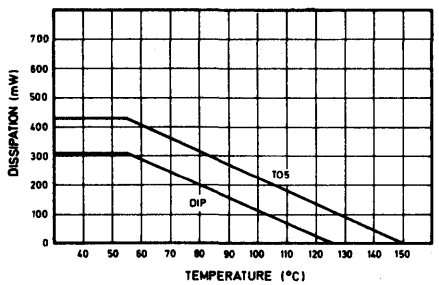


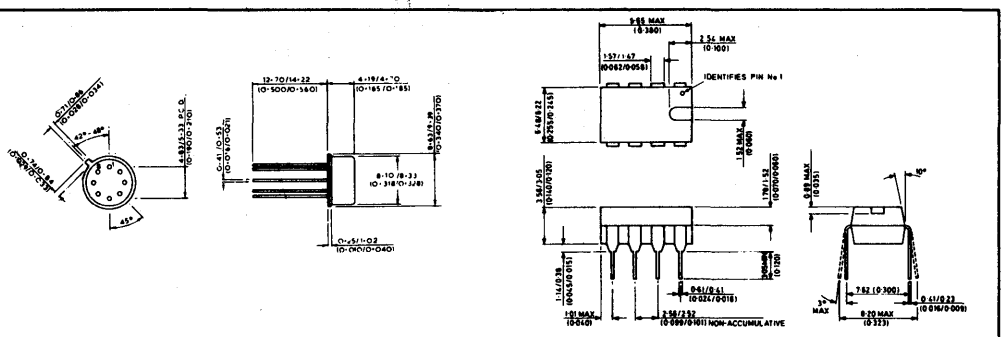
Fig. 15 Ambient operating temperature v. degrees centigrade

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 4)	+15V
Storage temperature	−55°C to 150°C (CM)
	−55°C to 125°C (DP)
Junction temperature	150°C (TO5) 125°C (DIP)
Thermal resistance	
Junction-case	60°C/W (TO5)
Junction ambient	220°C/W (T05) 230°C/W (DIP)
Maximum power dissipation	See Fig. 15
Operating temperature range	−55°C to +125°C (TO5) at 100 mW
	−55°C to +100°C (DIP) at 100 mW

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



8 LEAD TO-5(5·08mm P.C.D.) **CM8**

8 LEAD PLASTIC DIL **DP8**

Plessey
Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SL500 SERIES

WIDEBAND AMPLIFIERS

SL561C

ULTRA LOW NOISE PREAMPLIFIERS

This integrated circuit is a high gain, low noise reamplifier designed for use in audio and video systems t frequencies up to 6MHz. Operation at low frequencies ; eased by the small size of the external components nd the low 1/f noise. Noise performance is optimised or source impedances between 20Ω and 1kΩ making ne device suitable for use with a number of transducers ncluding photo-conductive IR detectors, magnetic tape eads and dynamic microphones.

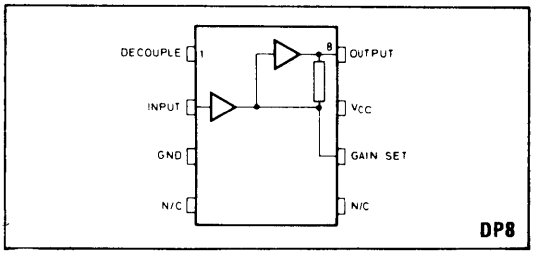


Fig. 1a. Pin Connections (viewed from the top)

APPLICATIONS

- Audio Preamplifiers (low noise from low impedance source)
- Video Preamplifier
- Preamplifier for use in Low Cost Infra-Red Systems

FEATURES

- High Gain 60dB
- Low Noise 0.8nV/√Hz (Rs 50Ω)
- Bandwidth 6MHz
- Low Power Consumption 10mW (Vcc = 5V)

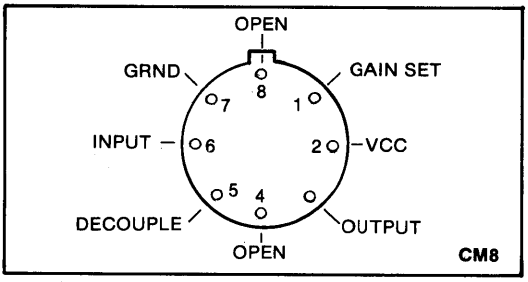


Fig. 1b. Pin Connections (viewed from the top)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc 5V
Source impedance 50Ω
Load impedance 10kΩ
Tamb 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 6 0/C
Equivalent input noise voltage		0.8		nV√Hz	100Hz to 6MHz
Input resistance		3		kΩ	
Input capacitance		15		pF	
Output impedance		50		Ω	
Output voltage	2	3		V p-p	See note 4
Supply current		2	3	mA	
Bandwidth		6		MHz	

OPERATING NOTES

1. Upper cut-off frequency

The bandwidth of the amplifier can be reduced from 6MHz to any desired value by a capacitor from pin 6 to ground. This is shown in Fig. 5. No degradation in noise or output swing occurs when this capacitor is used. The high frequency roll off is approximately 6dB/ octave.

2. Low frequency reponse

The capacitors C_2 and C_3 (Fig. 4) determine the lower cut-off frequency. C_2 decouples an internal feedback loop and if its value is close to that of C_3 an increase in gain at low frequencies can occur. For a flat response make $0.05\,C_3 > C_2 > 5C_3$.

3. Gain set facility

Provision is made to adjust the gain by means of a resistor between pin 6 and the output. Gains as low as 10dB can be selected. This resistor increases the feedback around the output stage and stability problems can result if the bandwidth of the amplifier is not reduced as indicated in Note 1. Fig.6 shows recommended values of C_1 for each gain range. Since the input stage is a common emitter stage without emitter degeneration (for best noise) at values of gain less than 40dB this input stage, rather than the output stage, determines the maximum output voltage swing. For a distortion of less than 10% the input voltage should be restricted to less than 5mV.

4. Driving low impedance loads

The quiescent current of the output emitter follower is 0.5mA. If larger voltage swings are required into low impedance loads this current can be increased by a resistor from pin 8 to ground. To avoid exceeding the ratings of the output transistor the resistor should not be less than 200Ω.

5. Noise performance

The equivalent input voltage for the amplifier is shown in Fig.7. From this the input noise voltage and current generators can be derived. They are :-

e_n 0.8nV/√Hz

i_n 2.0pA/√Hz

Flicker or 1/*f* noise is not normally a problem, the knee frequency being typically below 100Hz.

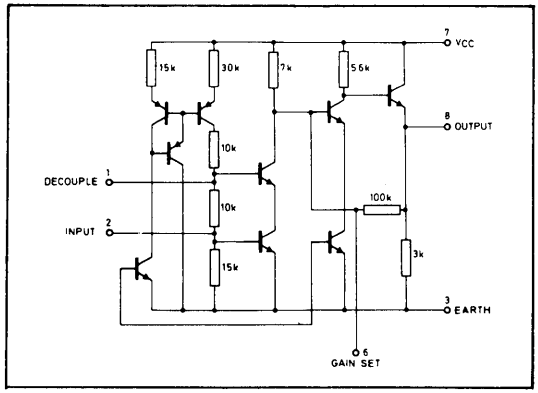


Fig. 2 Circuit diagram

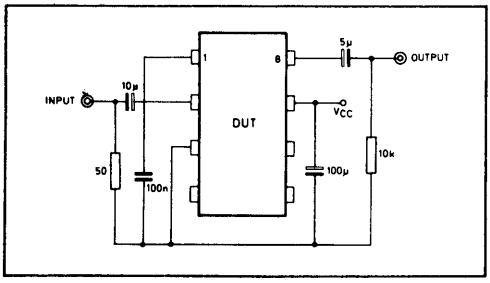


Fig. 3 Test circuit

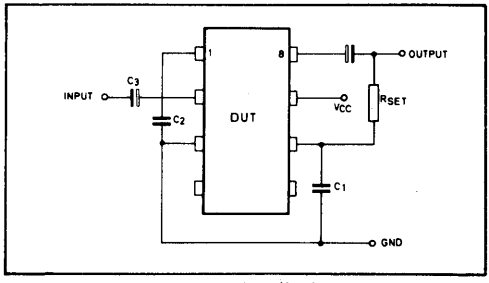


Fig. 4 Typical application

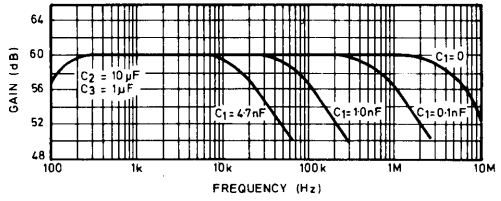


Fig. 5 Gain v. frequency

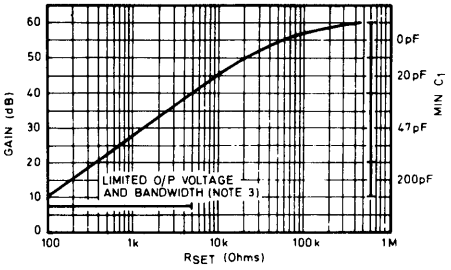


Fig. 6 Gain v. R_{set}

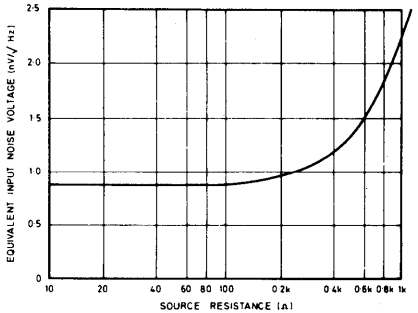


Fig. 7 Noise v. source impedance

SL565

UHF PREAMPLIFIER

The SL565 amplifier is a general purpose device
use at frequencies up 1GHz.

t features a differential input and output, and
)d linearity.

The device operates from a single 5V supply
h a minimal number of external components
l is encapsulated in an 8 lead DIL package.

:ATURES

- Low Cost
- 22dB Gain (S_{21}) Balanced I/P & O/P
- Minimal External Component Count
- Good Linearity
- Differential Input and Output
- 1GHz Response
- 5V Supply

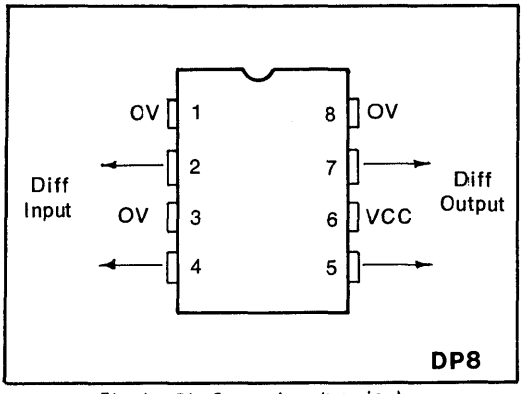


Fig. 1. Pin Connections (top view)

ABSOLUTE MAXIMUM RATINGS

- Vcc + 10V (Short Term)
- Operating temperature range 0° C to +65° C
- Storage temperature −55° C to + 125° C

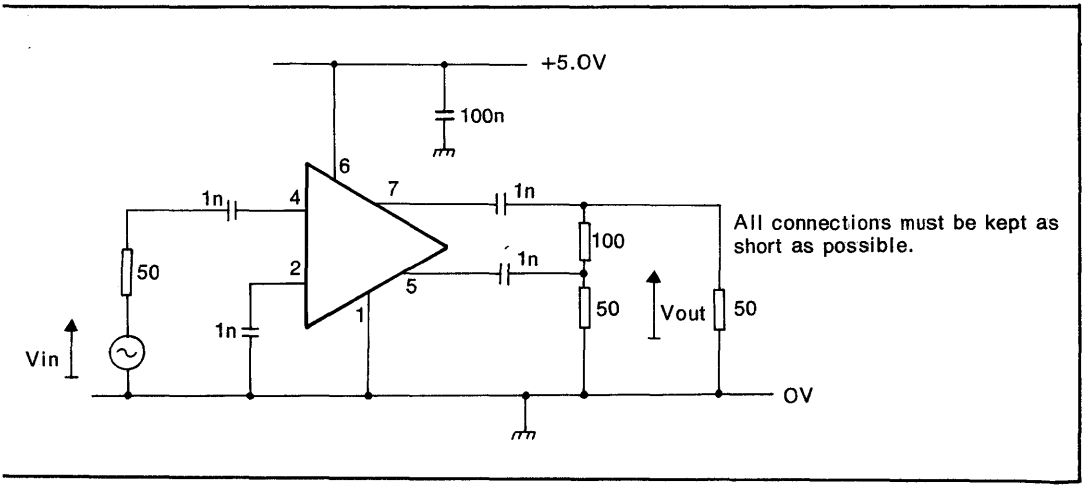


Fig. 2. Test Circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

Vcc = 5.0V, Tamb = +25° C

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage	6	4.75	5.0	5.5	V	
Supply Current	6	30	50	70	mA	
Differential Gain S21			22		dB	100 to 900MHz
Gain)Single ended)	2.4	10	16		dB	see Fig. 2
Differential Gain S21			20		dB	1GHz
Differential Gain S21			10		dB	1.3GHz
Input Signal Handling	2.4		25		mVrms	—40dB Intermodulation
Noise Figure			12		dB	

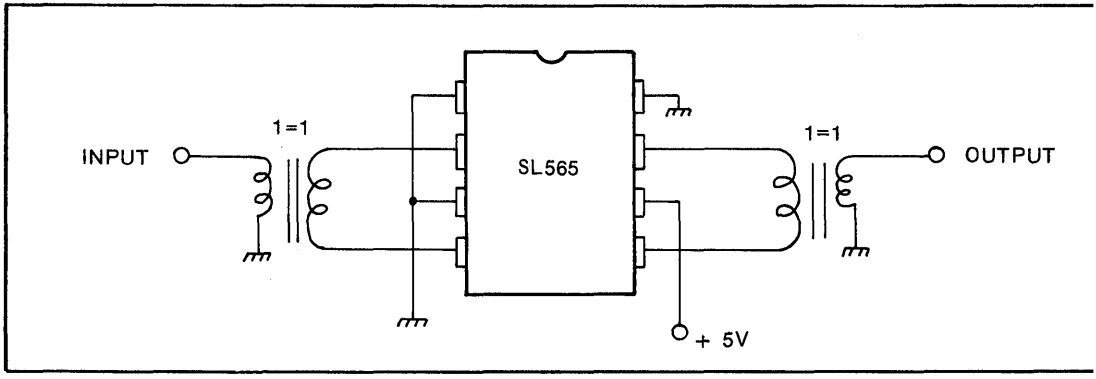


Fig. 3. Typical Application

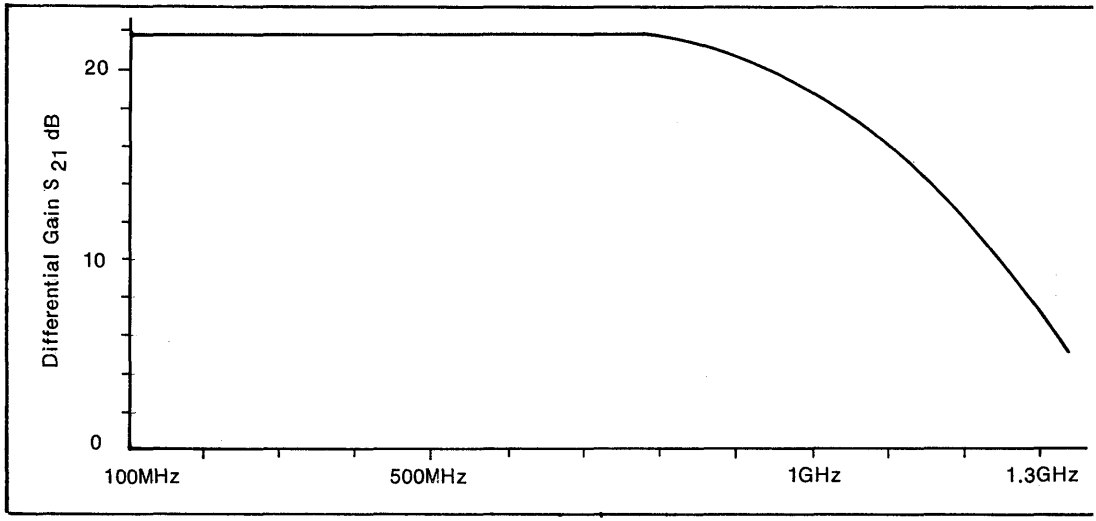


Fig. 4. Frequency Response

SL610C, SL611C & SL612C

RF/IF AMPLIFIERS

The SL610C and SL611C are low noise, low distortion, RF voltage amplifiers with integral supply line decoupling and AGC facilities. The SL610C has a voltage gain of 10 and a bandwidth of 140MHz, while the SL611C has a voltage gain of 20 and a bandwidth of 100MHz. Both circuits have a 50dB AGC range with maximum signal handling of 250mV rms. As they are voltage amplifiers they have high input impedance and low output impedance.

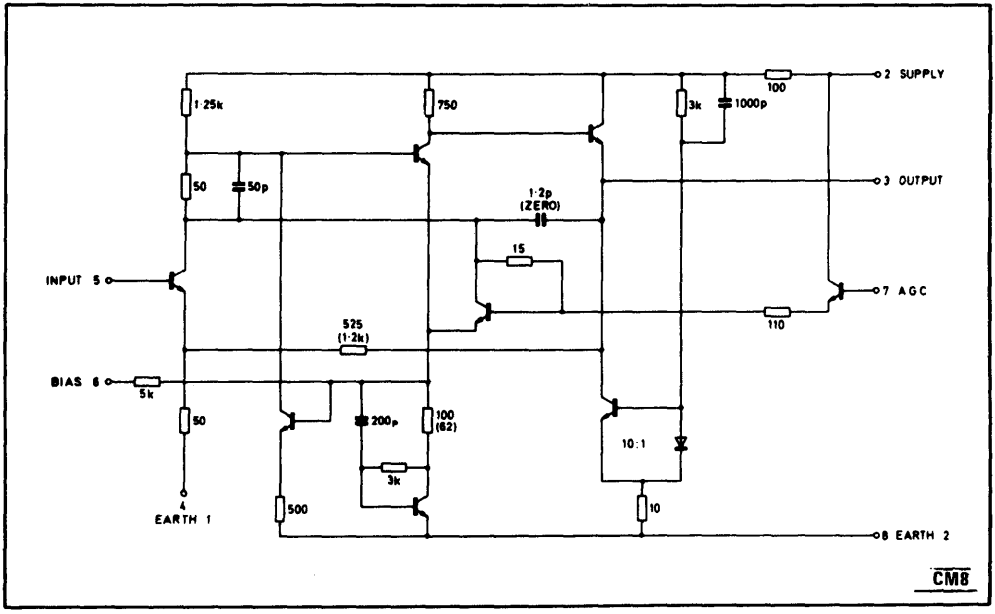


Fig. 1 Circuit diagram of SL610C and SL611C
(Component values in parentheses refer to SL611C)

The SL612C is a low noise, low distortion, IF voltage amplifier similar to the SL610C and SL611C but having a voltage gain of 50, a bandwidth of 15MHz and only 20mW power consumption. It has a 70dB AGC range with maximum signal handling of 250mV rms.

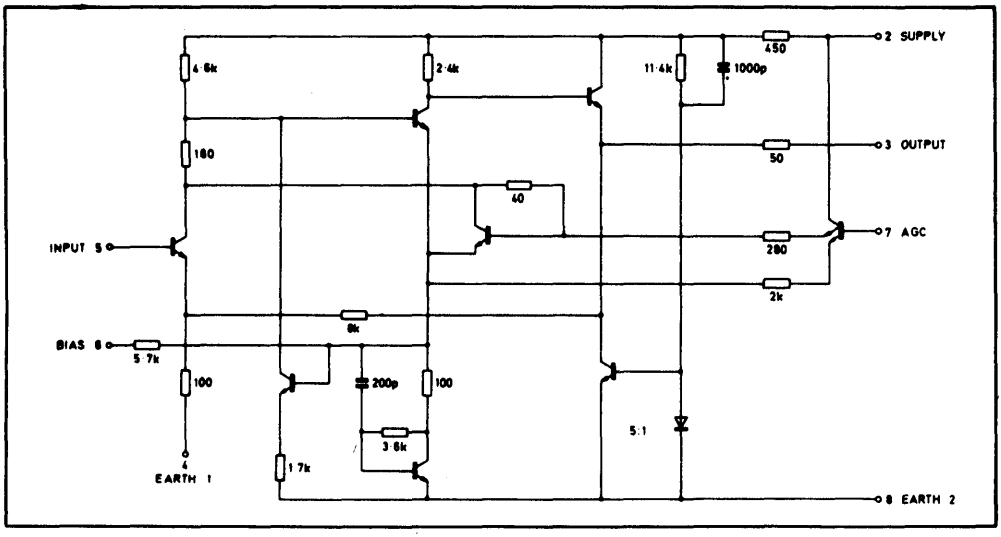


Fig. 2 Circuit diagram of SL612C

ELECTRICAL CHARACTERISTICS

Test conditions: Supply voltage = 6V
Temperature = +25°C (unless otherwise stated)
Pins 5 and 6 strapped together
AGC not applied unless specified.

Characteristic	Circuit	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
Voltage gain	SL610C	18	20	22	dB	30MHz } Source = 25Ω
	SL611C	24	26	28	dB	30MHz } Load R≥ 500Ω
	SL612C	32	34	36	dB	1.75MHz } Load C≤ 5pF
Cut-off frequency	SL610C	85	140		MHz	Source = 25Ω
(−3dB)	SL611C	50	100		MHz	Load R≥ 500Ω
(See Fig. 9)	SL612C	10	15		MHz	Load C≤ 5pF
Noise Figure	SL610C		4		dB	Source = 300Ω, f = 30MHz
	SL611C		4		dB	Source = 300Ω, f = 30MHz
	SL612C		3		dB	Source = 800Ω, f = 1.75MHz
Max. input signal	SL610C		100		mVrms	Load 150Ω, f = 10MHz
(1% cross modulation)	SL611C		50		mVrms	Load 150Ω, f = 10MHz
No AGC applied	SL612C		20		mVrms	Load 1.2kΩ, f = 1.75MHz
Max. input signal	SL610C		250		mVrms	f = 10MHz
(1% cross modulation)	SL611C		250		mVrms	f = 10MHz
Full AGC applied	SL612C		250		mVrms	f = 1.75MHz
AGC range	SL610C	40	50		dB	
(See Fig. 10)	SL611C	40	50		dB	
	SL612C	60	70		dB	
AGC current	SL610C		0.15	0.6	mA	
	SL611C		0.15	0.6	mA	AGC Voltage = 5.1V
	SL612C		0.15	0.3	mA	
Quiescent current	SL610C		15	20	mA	
consumption	SL611C		15	20	mA	Output open circuit
	SL612C		3.3	5	mA	
Change of voltage* gain with temperature	All types		±1		dB	−55°C to +125°C
Change of AGC range* with temperature	All types		±2		dB	−55°C to +125°C

*from nominal

Gain and frequency response of these circuits are relatively independent of supply voltage within the range 6 – 9V

OPERATING NOTES

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 strapped. A slight improvement in noise figure, and an increase in the LF input impedance may be obtained by making the necessary AC connection via the earthy end of an input tuned circuit in the conventional manner.

The characteristics of these units have been expressed in G parameters which are defined as shown in Fig. 3.

These parameters correspond to the normal operation of a voltage amplifier which is usually operating into a load much higher than its output impedance and from a source much lower than its input impedance. Hence the input admittance (G_{11}) and voltage gain (G_{21}) are measured with open circuit output, and the output impedance (G_{22}) with short circuit input. The parasitic feedback parameter is the current transfer (G_{12}) i.e. the current which flows in a short circuit across the input for a given current flowing in the output circuit.

Since the effects of G_{12} are small for reasonable values of load and source impedance, the approximate equivalent circuit given in Fig. 4 may be used.

Hence the typical effects of applying finite load and source impedances, real or complex, may be evaluated by the use of the graphs showing the values of the major parameters versus frequency. At lower frequencies the limitation on Z_L is dependent upon output signal; for maximum output $Z_L = 100\Omega$.

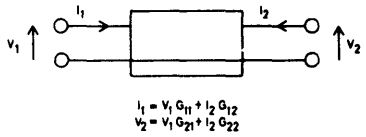


Fig. 3 Definition of G parameters

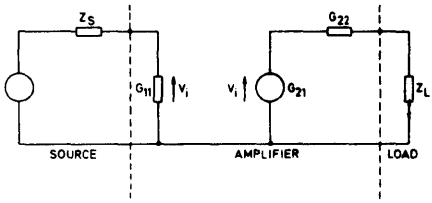


Fig. 4 Amplifier equivalent circuit

Stability

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output respectively are shown in Fig. 5 and 6 and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Fig. 7 and 8. It will be seen that, for the SL610C and the SL611C R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL612C, R_{in} is not negative and R_{out} is negative only below 700KHz.

It is evident that if an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and R1 is higher than R_{in}.

Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input may be inductive, therefore, it may be shunted by a resistor and where the load may be capacitive 47Ω should be placed in series with the output.

These devices may be used with supplies up to +9V with increased dissipation.

The AGC characteristics shown in Fig. 8 vary somewhat with temperature: a preset potentiometer should not, therefore, be used to set the gain of either of these circuits if gain stability is required.

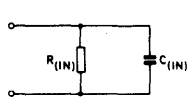


Fig. 5 Input circuit

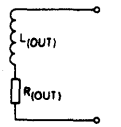


Fig. 6 Output circuit

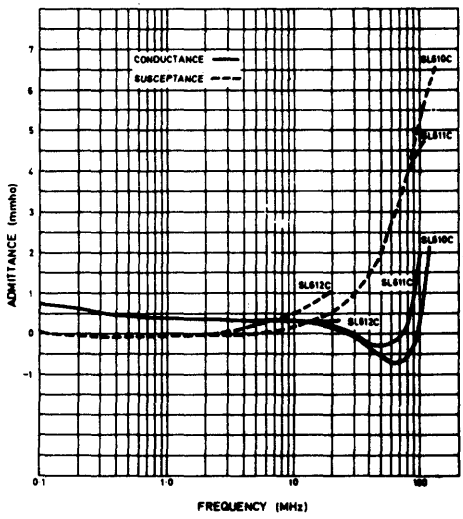


Fig. 7 Input admittance with o/c output (G_{11})

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +150°C
Operating temperature range	−55°C to +125°C
Chip-to-ambient thermal resistance	220°C/W
Chip-to-case thermal resistance	60°C/W
Supply voltage	12V

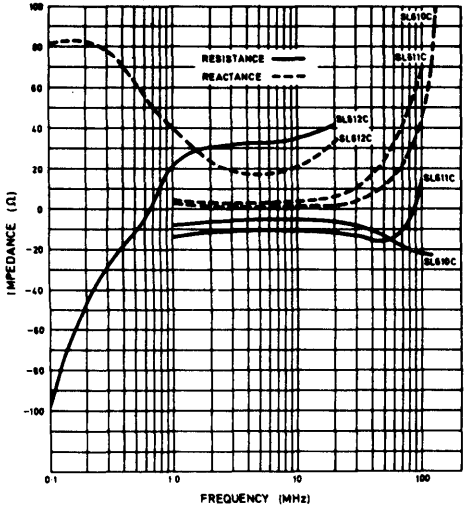


Fig. 8 Output impedance with s/c input (G_{22})

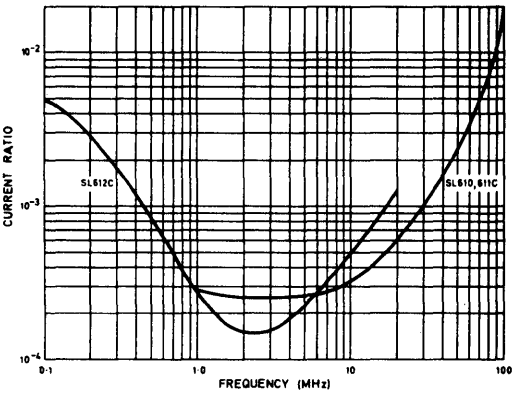


Fig. 11 Reverse current transfer ratio (G_{12})

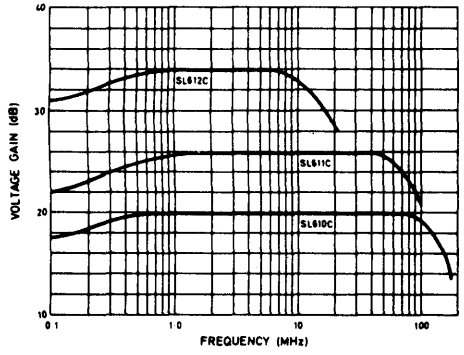


Fig. 9 Voltage gain (G_{21})

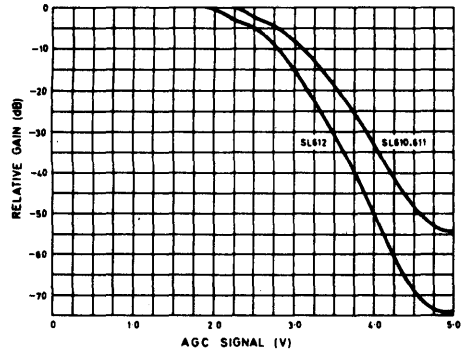


Fig. 10 AGC characteristics

TYPICAL MAX. FREE AIR OPERATING TEMPERATURES (°C)

Supply Voltage	6V		9V		12V	
AGC Voltage	None	Full	None	Full	None	Full
SL610C/611C	153	129	118	58	–	–
SL612C	171	158	165	129	149	69

Plessey Semiconductors

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL613C
LIMITING AMPLIFIER/DETECTOR

The SL613C is a low noise limiting amplifier intended for use as an RF clipper, a limiting stage in IF amplifiers, or an RF Compressor in SSB transmitters. It contains a detector which may be used to detect AM but is particularly intended for use as an AGC detector. The amplifier, which has a gain of 12 dB when not limiting, has upper and lower 3 dB points of 150 MHz and 5 MHz respectively. It limits when its input exceeds 120 mV r.m.s. The detected output during limiting is 1 mA.

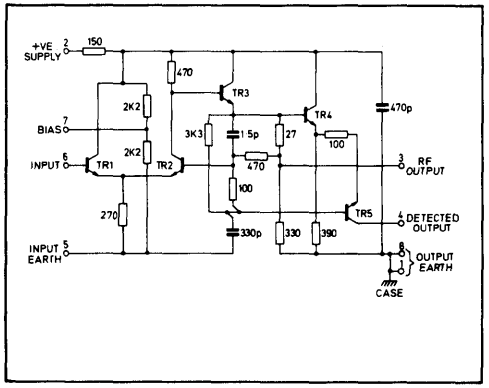


Fig. 1 Circuit diagram

FEATURES

- Wide Bandwidth
- Low Noise
- Highly Symmetrical Limiting
- Large Signal Handling Capability

APPLICATIONS

- RF Clippers
- AGC Systems
- AM Detectors
- RF Compression in SSB Transmitters

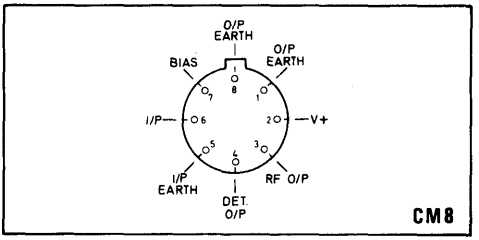


Fig. 2 Pin connections

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply +6V
Temperature +25°C
Pins 6 & 7 strapped together

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	3.3	4	4.6	–	30 MHz
Upper 3 dB frequency	120	150		MHz	
Lower 3 dB frequency		5	8	MHz	
Noise figure		4.5	5.5	dB	60 MHz 500Ω source
Supply current	11	15	20	mA	No signal
Limited RF o/p		1.25		V p-p	0.5 V input, 30 MHz
Detector current	0.85	1	1.25	mA	0.5 V input, 30 MHz
Maximum input before overload	1.5	1.75		V r.m.s.	30 MHz
Input impedance		5kΩ + 6pF			60 MHz. Open circuit o/p

OPERATING NOTES

The SL613C, like the SL610/11/12, is normally used with the input and bias pins connected directly together and the input applied through a capacitor. However, and again like the SL610/11/12, the bias may be decoupled and connected to the 'cold' end of a coil or tuned circuit, the input pin being connected to its 'hot' end or to a tap.

The supply rail is decoupled internally at RF but as the gain is dependent on supply voltage there should no appreciable LF ripple on the supply. Two separate earth connections are made in order to minimise the effects of common earth-lead inductance – such common earth-lead inductance can cause instability and care should be taken not to introduce it externally.

The RF output is capable of driving a load of 1kΩ in parallel with 10pF. If a capacitive load of more than 10pF is envisaged a resistor should be connected between the output pin and the load. Normally 50Ω is sufficient. The output should be isolated at DC by a capacitor.

The detected output consists of a current out of pin 4, which is an NPN transistor collector. This pin must always be more than 3 volts more positive than earth, even if the detected output is not required (in which case it is best to strap pins 2 and 4).

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to +85°C
Operating temperature	−30°C to +70°C
Supply voltage (pins 2 or 4)	+9V

SL620C & SL621C

AGC GENERATORS

The SL621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL610C, SL611C and SL612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL610C and one SL612C amplifier and a suitable detector, the SL621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

The SL620C VOGAD (Voice Operated Gain Adjusting Device) is an AGC generator designed to work in conjunction with the SL630C audio amplifier (particularly when the latter is used as a microphone amplifier) to maintain the amplifier output between 70mV and 87mV rms for a 35 dB range of input. A one second 'hold' period is provided which prevents any increase of background noise during pauses in speech.

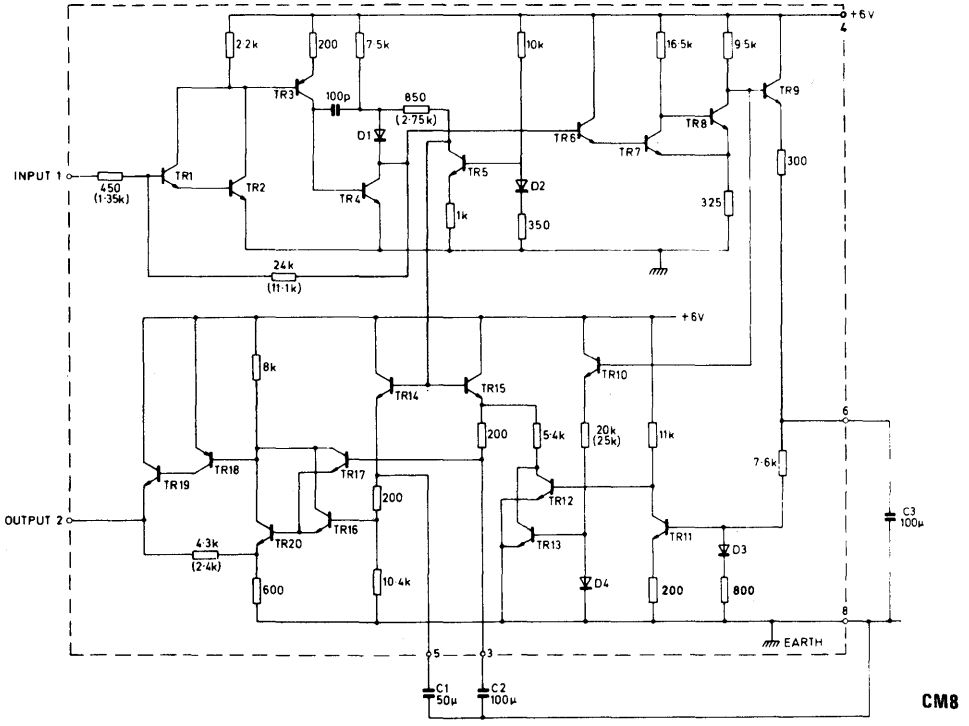


Fig. 1 Circuit diagram of SL620C and SL621C (Component values in brackets refer to SL620C)

DESCRIPTION

The operation of the SL621C is described with reference to the circuit diagram, Fig. 1, and Fig. 2 which illustrates the dynamic response of a receiver controlled by the SL621C.

The SL621C consists of an input AF amplifier TR1 – TR4 (3 dB point: 10KHz) coupled to a DC output amplifier, TR16 – TR19, by means of a voltage back-off circuit, TR5 and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

The detected audio signal at the input will rapidly establish an AGC level, via TR14, in time t_1 (see Fig. 2). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is the more sensitive.

If signals exist at the SL621C input which are greater than approximately 4mV rms they will actuate the trigger circuit TR6 – TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20 dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, so holding off TR12 via TR11. When the trigger pulses cease, C3 discharges and after t_5 turns on TR12. Capacitor C2 is discharged rapidly (in time t_4) via TR12 and so full receiver gain is restored. The hold time, t_5 is approximately one second with C3 = 100μF. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 2 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

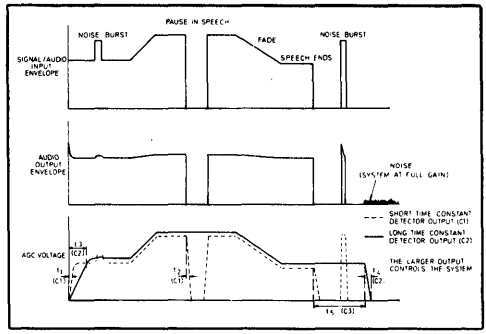


Fig. 2 Dynamic response of a system controlled by SL620C or SL621C AGC generator

OPERATING NOTES

The various time constants quoted are for C1 = 50μF and C2 = C3 = 100μF. These time constants may be altered by varying the appropriate capacitors.

An input coupling capacitor is required. This should normally be 0.33μF for an SL621C and about 1μF for an SL620C.

Fig. 3 shows how the SL621C may be connected into a typical SSB receiver.

Fig. 4 shows how the SL620C is used to control the gain of the SL630C audio amplifier. The operation of the SL620C is exactly the same as that of the SL621C and the diagram showing the dynamic response of the closed loop system, Fig. 2, is equally applicable to the SL630C/SL620C combination. Again, the time constants may be altered by varying the capacitor values.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least 500μF so that it is not affected by the current surge resulting from a sudden input on pin 1. The devices may be used with a supply of up to +9V.

In a receiver for both AM and SSB using an SL623C detector/Carrier AGC generator, the AGC outputs of the SL621C and SL623C may be connected together provided that no audio reaches the SL621C input while the SL623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output of an SL620 or SL621 should not exceed 15000pF or the impulse suppression will suffer.

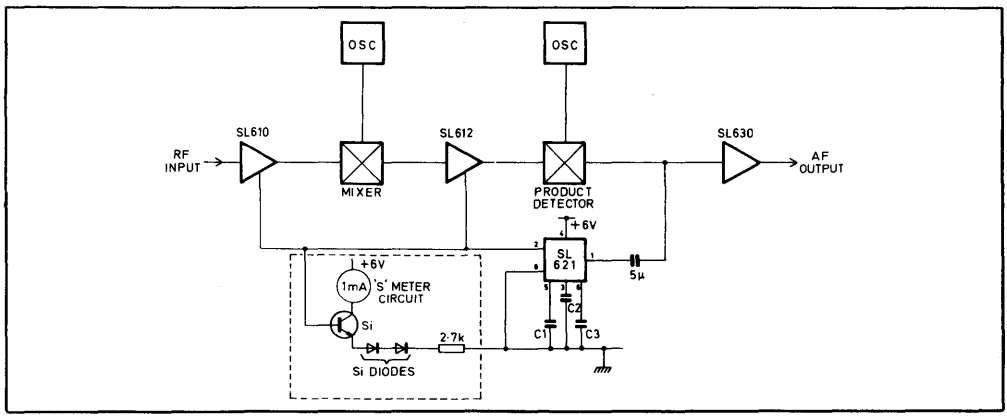


Fig. 3 SL621C used to control SSB receiver

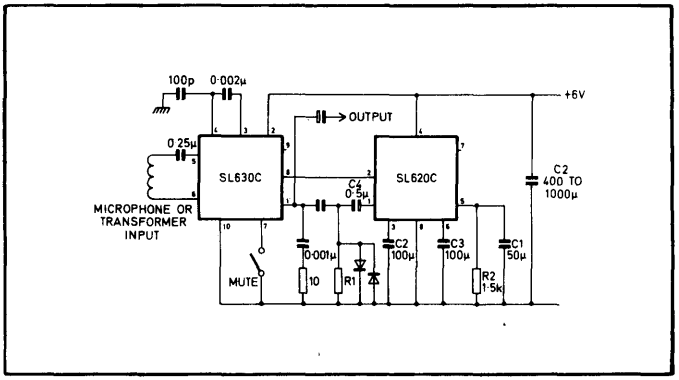


Fig. 4 SL620C used to control SL630C audio amplifier

ELECTRICAL CHARACTERISTICS SL 620C & SL 621C

Test conditions: Supply voltage = 6V
Temperature = +25°C
Input signal frequency = 1kHz

Characteristic	Circuit	Value				Test Conditions
		Min.	Typ.	Max.	Units	
Input for 0.65V dc output	SL620C	55	70	85	mVrms	See Fig.5
Input for 1.5V dc output	SL620C	70	87	105	mVrms	See Fig.5
Input for 2.2V dc output	SL621C	6.0	7.0	10.0	mVrms	See Fig.6
Input for 4.6V dc output	SL621C	9.0	11.0	16.0	mVrms	See Fig.6
						Measurement accuracy 1 dB
*Fast rise time, t_1	Both		20	30	ms	0–50% full output
*Fast decay time, t_2	Both	150	200	250	ms	100%–36% voltage on C_1
						C_1 = 50µF
*Slow rise time, t_3	Both	150	200	300	msec	Time to output transition point
Input 3 dB point	Both		10		kHz	
Maximum fade rate	SL620C		0.22		V/s	
	SL621C		0.45		V/s	
						C_2 = 100µF
*Hold collapse time, t_4	Both	150	200	250	ms	Full zero output
*Hold time, t_5	Both	0.75	1.0	1.25	s	C_3 = 100µF
A.C. ripple on output	Both		12	20	mVp-p	1kHz. Output open circuit
Maximum output voltage	SL620C	2.0			V	
	SL621C	5.1			V	
Quiescent current consumption	Both	2.5	3.1	4.1	mA	
Surge current	Both		30		mA	
Input resistance	SL620C	1	1.4	2	kΩ	
	SL621C	350	500	700	Ω	
Output resistance	SL620C	12	40	130	Ω	
	SL621C	20	70	230	Ω	

**See Figure 2*

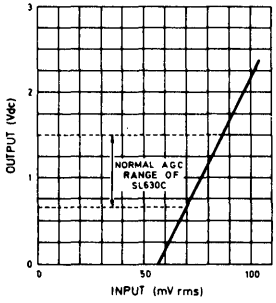


Fig. 5 Transfer characteristic of SL620C

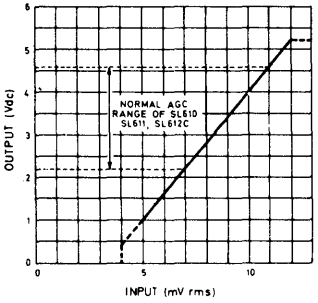


Fig. 6 Transfer characteristic of SL621C

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Free air operating temperature	−25°C to +125°C
Chip-to-ambient thermal resistance	220°C/W
Chip-to-case thermal resistance	60°C/W
Supply voltage	12V

SL622C

AF AMPLIFIER, VOGAD & SIDETONE AMPLIFIER

The SL622C is a silicon integrated circuit combining the functions of audio amplifier with voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low-sensitivity microphone and to provide an essentially constant output signal for a 60 dB range of input.

Additionally, a constant gain amplifier is incorporated which provides an amplitude-limited output for sidetone in mobile transmitter/receiver applications.

The encapsulation is a 10 lead TO-5 package and the device is designed to operate from a 6 to 12 volt supply, over a temperature range of −55°C to +125°C.

A voltage regulator produces an independent supply line at 4.7 Volts stabilised

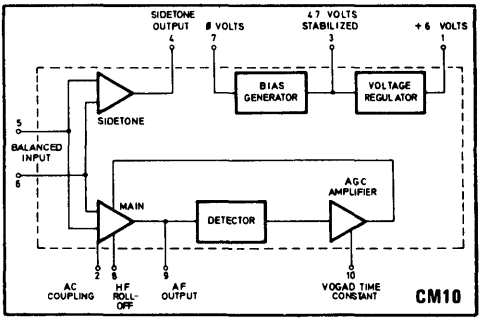


Fig. 1 Block Diagram

ELECTRICAL CHARACTERISTICS

Test Conditions: Input frequency 1KHz
Supply voltage +6V
Temperature +25°C

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Test Conditions
VOGAD output level	55	90	110	mV rms	Balanced signal input 18mV rms
Sidetone output level	600	800	900	mV p-p	
AF amplifier voltage gain	49	52	55	dB	Balanced signal input 72μV rms
Sidetone voltage gain	24.5	29	30.5	dB	
Current consumption consumption		14	16	mA	6V supply, input 1mV rms
		24		mA	12V supply, input 1mV rms
Decay time – time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched down 20dB.		1.0		s	Original balanced signal input 18mV rms; R1 = 1 MΩ, C3 = 47μF, Test cct. as Fig.2
Attack time – time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched up 20dB.		20		ms	Original balanced signal input 1.8mV rms; R1 = 1 MΩ, C3 = 47μF, Test cct. as Fig.2
Total harmonic distortion at VOGAD output.		2		%	Balanced signal input 90mV rms
Differential input impedance.		300		Ω	
Single-ended input impedance.		180		Ω	
Sidetone output impedance		200		Ω	
AF amplifier output resistance		50		Ω	
VOGAD operating threshold (Whisper threshold)		100		μV rms @ I/P	

T5▷

OPERATING NOTES

The SL622C incorporates a series regulator which will accept supply voltages between 6V and 12V and provides a supply line rejection of approximately 26 dB when operated from a 6V supply The supply line immunity increases with supply voltage.

The input stage is a differential class A-B stage with an AGC terminal. The accurate balance of the input stage give an overall common-mode rejection ratio of greater than 30 dB.

Typically the amplifier will handle differential input signals of up to 375mV p-p and unbalanced signals of up to 50mV p-p. When used in the unbalanced mode either pin 5 or pin 6 may be used as the input, the other being decoupled to earth.

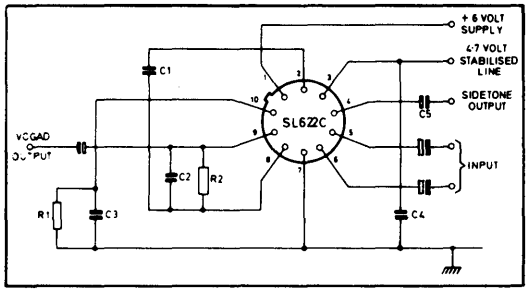


Fig. 2 Connection diagram for SL622C used as a microphone amplifier.

Fig. 2 shows the SL622C when used as a balanced microphone amplifier. The LF cut-off of the amplifier is set by C1 – and also by the values of coupling capacitors to the input pins (pin 5 and pin 6); coupling capacitors should be used if the d.c. potential of the input is not floating with respect to earth.

The HF cut-off is set by C2. The VOGAD threshold may be increased by connecting an external conductance between pins 8 and 9. The threshold is increased by approximately 20 dB for 1 millimho of conductance, the value of C2 should be adjusted in conjunction with any threshold alteration in order to obtain the desired bandwidth.

C3 and R1 set the attack and decay rates of the VOGAD. C3 = 47μF and R1 = 1Mohm gives an attack time constant (gain increasing) of 20 millisecs and a decay rate of 20 dB/sec. C1 = 2.2μF and C2 = 4.7nF give a 3 dB bandwidth of approximately 300Hz to 3kHz.

The amplifier can be muted by applying +4V to pin 10, but when the voltage is removed either C3 must be discharged or there will be an appreciable delay before the circuit functions normally again.

C4 is used for RF decoupling of the stabilised line. AF decoupling may be applied to improve supply line rejection and sidetone linearity.

The VOGAD and sidetone steady-state transfer characteristics are shown in Figs. 3 and 4.

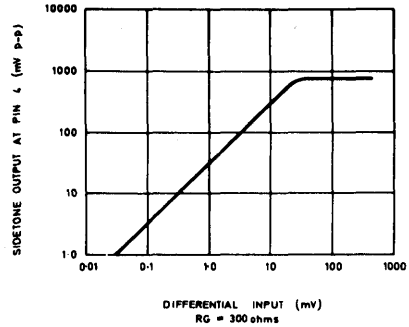


Fig. 3 Sidetone output characteristics.

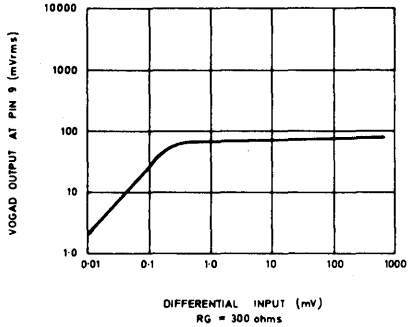


Fig. 4 VOGAD – output characteristics (1kHz sinewave input).

Pin	Function
1	+6 volts supply
2	A.C. coupling
3	+4.7V decoupling
4	Sidetone o/p
5, 6	Balanced signal input
7	OV
8	HF Roll off
9	AF o/p
10	VOGAD time constant.

ABSOLUTE MAXIMUM RATINGS

Continuous supply voltage (positive)	12V ± 0.5V
Storage temperature	−55°C to + 175°
Ambient temperature (6V operating)	−55°C to + 125°
(12V operating)	−55°C to + 100°

SL623C

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL610C, SL611C and SL612C RF and IF amplifiers. It is complementary to the SL621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL610C and one SL612C amplifier, the SL623C will maintain the output within a 5 dB range for a 90 dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100 mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies. The encapsulation is a 10 lead TO-5 package and the device is designed to operate from a 6 volt supply, over a temperature range of −55°C to +125°C.

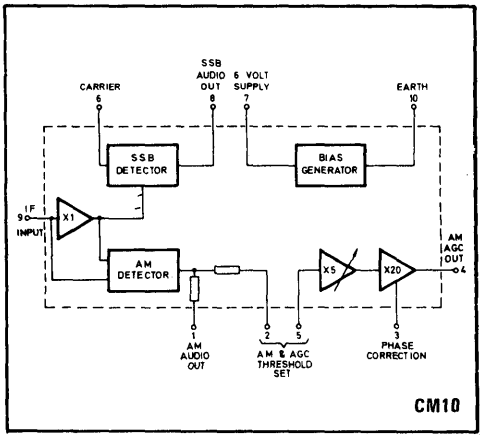


Fig. 1 Block Diagram

ELECTRICAL CHARACTERISTICS @ SUPPLY = +6V, T_{amb} = + 25°C

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
SSB Audio Output	25	30	42	mV rms	Signal Input 20mV rms @ 1.748 MHz. Ref. Signal Input 100mV rms @ 1.750 MHz
AM Audio Output	45	55	64	mV rms	Signal Input 125mV rms @ 1.75 MHz. Modulated to 80% @ 1 kHz.
AGC Range (change in input level to increase AGC output voltage from 2.0V to 4.6V)			5	dB	Initial signal input 125mV rms at 1.75 MHz. Mod. to 80% at 1 kHz Output Set with 10k Ω pot between pins 2 & 5 to 2.0V.
Quiescent Current Consumption		9	11	mA	Output open circuit
Max. operating frequency		30		MHz	
Change of SSB audio output with temperature +85°C		−0.5		dB	Signal Input 20mV rms @ 1.784 MHz. Ref. signal input 100mV rms @ 1.75 MHz.
−40°C		+0.5		dB	
Change of AM audio output with temperature +85°C		−0.25		dB	Signal Input 125mV rms @ 1.75 MHz Modulated to 80% @ 1 kHz.
−40°C		−0.25		dB	

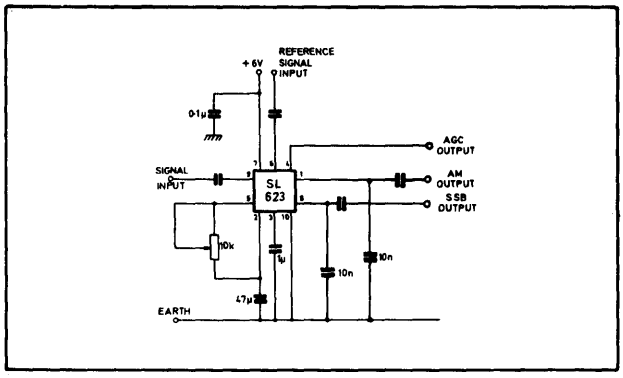


Fig. 2 Typical circuit using the SL623C as signal detector and AGC generator.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Ambient operating temperature	−55°C to +125°C
Supply voltage	−0.5V to +12V

Plessey Semiconductors

SL600 SERIES
COMMUNICATIONS CIRCUITS

SL624C
MULTIMODE DETECTOR

The SL624C is a complex integrated circuit designed for use as a detector of AM, FM, SSB or CW, acting respectively as a synchronous detector, a quadrature detector and a product detector with built-in oscillator. It also contains a voltage-controlled gain system and a separate audio amplifier capable of driving a single transistor output stage.

A major advantage of the SL624C as an AM detector is that unlike an envelope detector, it does not give an output on broad band IF noise when used in a typical receiver following a block filter and a broadband IF amplifier.

FEATURES

- Demodulates FM, AM, SSB and CW
- Operates up to 30 MHz (Typ)
- Voltage-Controlled Audio Gain
- Separate Audio Driver

APPLICATIONS

- Mobile Transceivers
- HF Transceivers
- VHF Transceivers

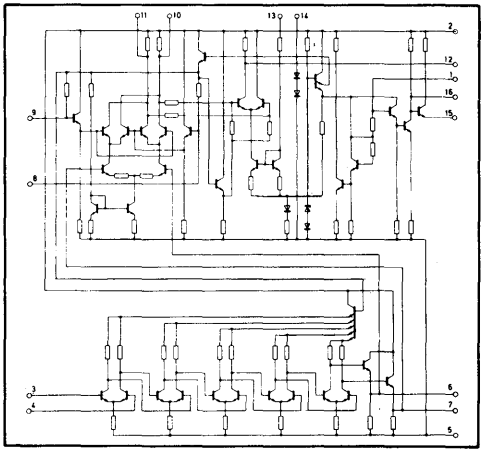


Fig. 1 Circuit diagram

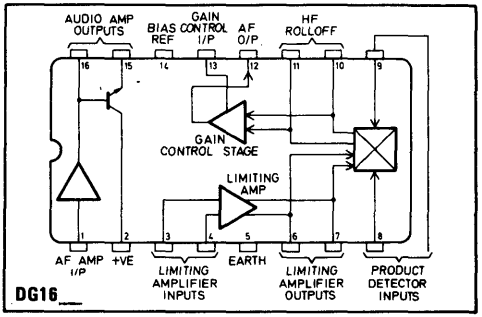


Fig. 2 Block diagram and pin connections (top)

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply +12V
Temperature +25°C (unless otherwise stated)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	9	12	15	V	
Current drain		23		mA	
Minimum input for synchronous AM detector					
+25°C		1		mV r.m.s.	9 MHz input
−55°C to +125°C		5			
Minimum input for limiting					
+25°C		100		μV r.m.s.	9 MHz input
−55°C to +125°C		300			
Detector audio gain range		80		dB	
Audio amplifier input R	20	50		kΩ	
Audio amplifier voltage gain		4		—	
Maximum operating frequency (limiting amplifier)		30		MHz	

OPERATING NOTES

Figs. 3, 4 and 5 show the SL624C used, respectively, as a synchronous AM detector, a quadrature FM detector and a self-oscillating product detector. It is evident that a multimode receiver may be made either by switching the components around one SL624C with relays or diodes, or by using three SL624Cs, one per mode.

The supply to the SL624C should be decoupled at HF by a 0.1 μF capacitor sited as near as possible to pins 2 and 5.

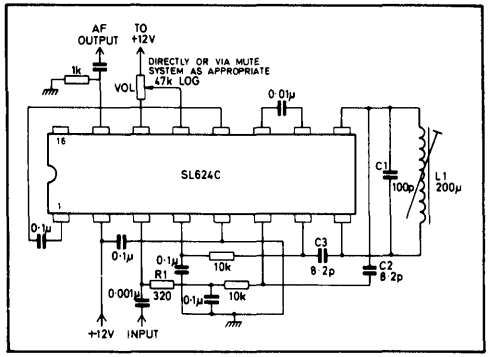


Fig. 4 FM quadrature detector

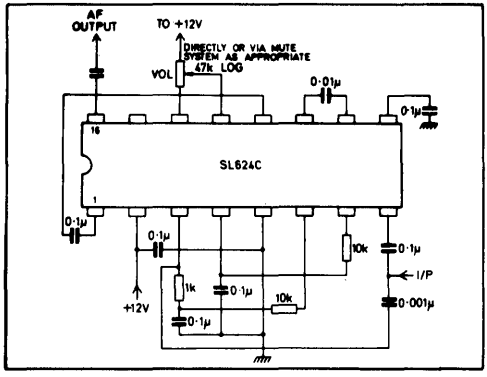


Fig. 3 Synchronous AM detector

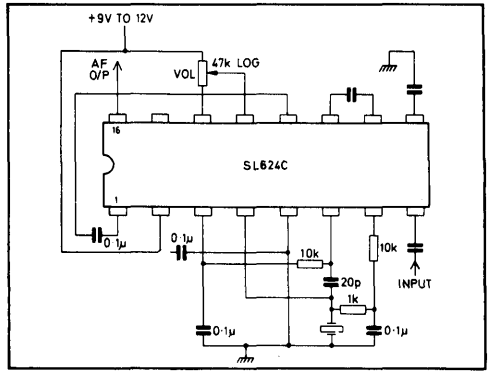


Fig. 5 Self-oscillating product detector

ABSOLUTE MAXIMUM RATINGS

Storage temperature:	–55°C to +150°C.
Operating temperature:	–55°C to +125°C.
Supply voltage (pin 2):	+18V.

SL630C

MICROPHONE/HEADPHONE AMPLIFIER

The SL630C is designed specifically for use as a microphone or headphone amplifier. It has a voltage gain of 100, will accept balanced or unbalanced inputs, and can deliver up to 250mW output from a class AB push-pull output stage.

A gain control facility with a logarithmic law allows a.g.c. to be applied when the device is used as a microphone amplifier, and also allows remote volume control with a linear potentiometer. Gain reduction of 100 dB may be obtained

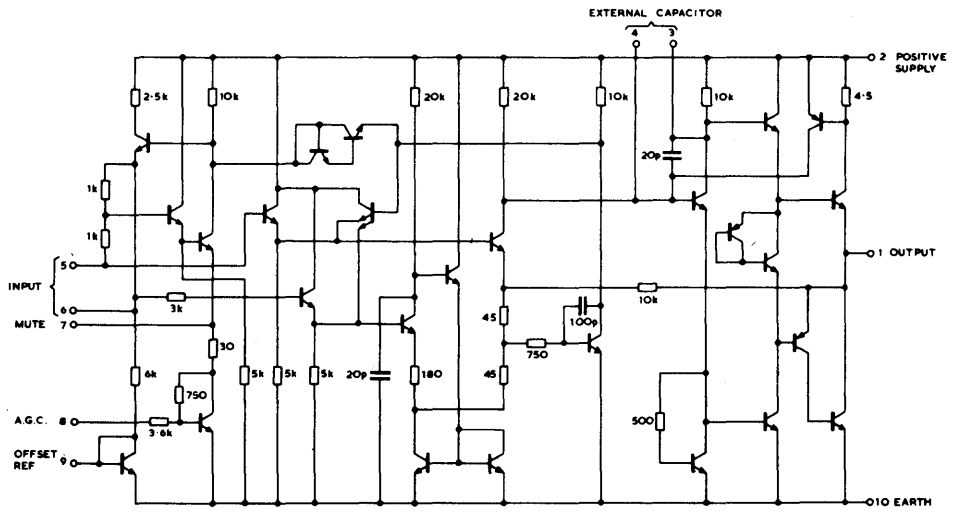


Fig 1 Circuit diagram

CM10

ELECTRICAL CHARACTERISTICS

Test conditions: Temperature = +25°C
Signal Frequency = 1kHz
Supply = 12V (unless otherwise stated)

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
Differential input voltage gain	38	40	42	dB	Input 1mVrms
Single ended input voltage gain	43	46	49	dB	Input 1mVrms
Maximum output voltage		1.2		Vrms	6V supply
	2.5	2.8		Vrms	12V supply
Maximum output power		See Fig. 6			0.5% distortion
Quiescent current (See also Fig. 6)			5	mA	6V supply
			13	mA	12V supply
Differential input impedance	1.0	2.0	3.6	kΩ	
Single ended input impedance		1.0	1.8	kΩ	
Output impedance		1.5	3.0	Ω	
Gain control range (See Fig. 5)	60	100		dB	
Maximum input (with gain reduced)		50		mVrms	10% distortion
Short circuit output current		110	200	mA	Irrespective of supply

OPERATING NOTES

Frequency Response

As with most small-signal integrated circuits, the inherent bandwidth of the SL630C is quite large. It extends from low audio frequencies up to approximately 0.5 MHz, unless restricted by a roll-off capacitor (C1) connected between pins 3 and 4. The approximate upper cut-off frequency is then given by

$$\omega_c \triangleq \frac{10^8}{C1}$$

where C1 is in picofarads

Muting

This can be achieved, in any application, by switching pin 7 directly to the negative rail

Microphone Amplifier

Fig. 2 shows the SL630C used with a balanced input on pins 5 and 6. If the load resistance increases with frequency it is necessary to stabilize the output circuitry. This is accomplished with 10Ω in series with 1nF connected between pin 1 and earth. The earth return to pin 10 must not share any common leads, particularly with the input. Decoupling pins 2 and 6 should follow normal engineering practice.

Headphone Amplifier

Fig. 3 shows the SL630C in a circuit suitable for powering a headset. The input is an unbalanced source connected to pin 5 and the device is decoupled at pins 1, 2 and 6 in the same manner as the microphone amplifier.

Manual gain adjustment using the remote gain control facility is also shown. It should be noted that the connection to pin 9 eliminates the 'dead' portion of the volume control range caused by the delayed attenuation characteristic shown in Fig. 5. R1 and R2 are chosen with regard to Fig. 5 to give the desired control range.

The input impedance at pin 8 is 3.6 kΩ.

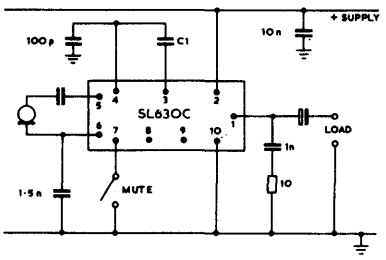


Fig 2 SL630C used as a microphone amplifier

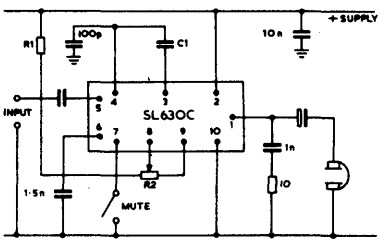


Fig 3 SL630C used as a headphone amplifier

Automatic Gain Control

To apply a.g.c., an SL620C should be used as shown in the circuit of Fig. 4. This will give effective gain control with a low audio-frequency cut-off of 200 Hz and a control response time of approximately 20 ms.

To preserve low-frequency stability and prevent motor-boating, C4 should not exceed the value given and, whilst R1 should not exceed 300Ω ,the time constant C3R1 must not be greater than 800 μs.

R2 is non-essential, but is useful if the input is likely to contain a large component below 300 Hz

C2 should be used if the power supply has a source impedance of more than a few ohms or is connected by long wires.

The system should not be tested with sinewave inputs below 300Hz as such signals can give rise to delay effects not produced by speech waveforms.

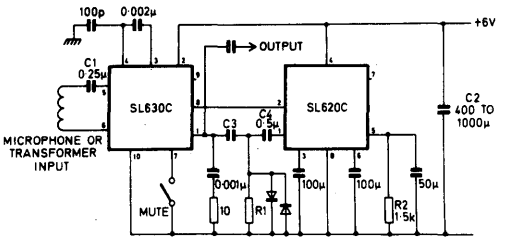


Fig 4 SL630C used with SL620C to achieve automatic gain control

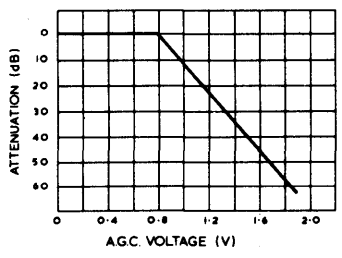


Fig 5 AGC characteristics

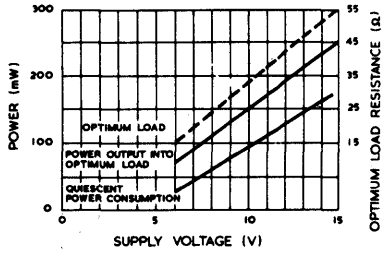


Fig 6 Power characteristics

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Free-air operating temperature range	
6V supply	−55°C to +125°C
12V supply	−55°C to +100°C
Supply voltage	+18V

SL640C & SL641C
DOUBLE BALANCED MODULATORS

The SL640C is designed to replace the conventional diode ring modulator, in RF and other communications systems, at frequencies of up to 75MHz. It offers a performance competitive with that of the diode ring while eliminating the associated transformers and heavy carrier drive power requirements.

At 30 MHz, carrier and signal leaks are typically −40dB referred to the desired output product frequency. Intermodulation products are −45dB with a 60 mV rms input signal

The SL641C is a version of the SL640C intended primarily for use in receiver mixer applications for which it offers a lower noise figure and lower power consumption. No output load resistor is included and signal leakage is higher, but otherwise the performance is identical to that of the SL640C

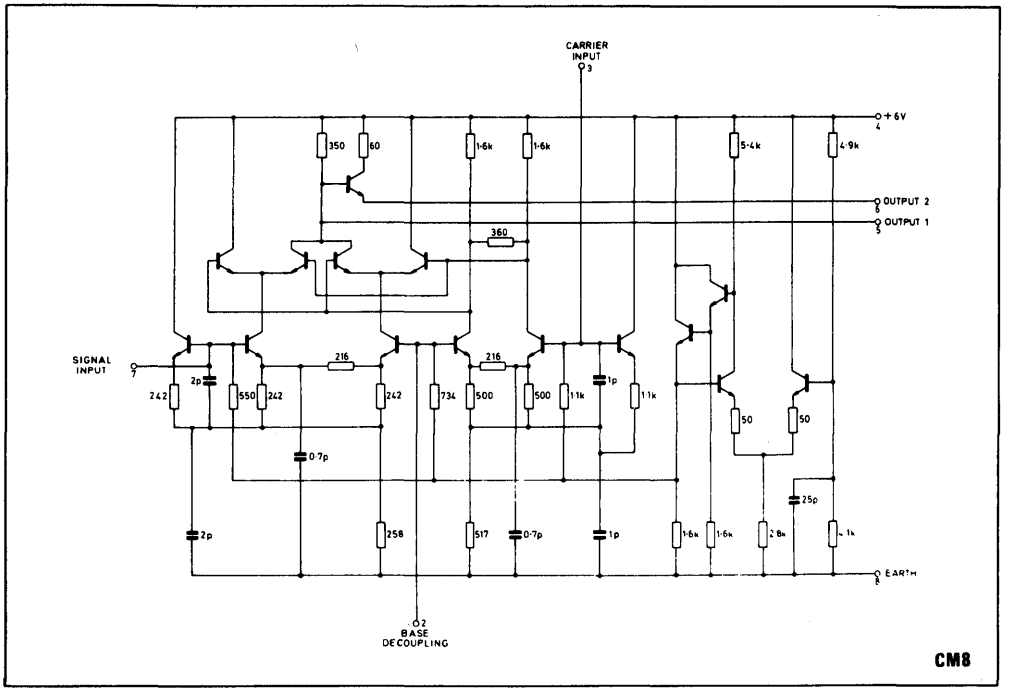


Fig. 1 Circuit diagram of SL640C

ELECTRICAL CHARACTERISTICS SL640C & SL641C

Test conditions: Supply voltage = +6V
Temperature = +25°C unless otherwise stated

Characteristic	Circuit	Value			Units	Test Conditions
		Min.	Typ.	Max.		
Conversion gain	SL640C	−2	0	+2	dB	
Signal leak	SL640C		−40	−20	dB	Signal: 70mVrms, 1.75MHz Carrier: 100mVrms, 28.25MHz Output: 30MHz
= Signal output / Desired sideband output						
Carrier leak	SL640C		−40	−20	dB	
= Carrier output / Desired sideband output						
Intermodulation products	SL640C		−45	−35	dB	Signal 1: 42.5mVrms, 1.75MHz Signal 2: 42.5mVrms, 2MHz Carrier: 100mVrms, 28.25MHz Output: 29.75MHz
Conversion transconductance	SL641C	2.2	2.5	3.5	mmho	
Signal leak	SL641C		−18	−12	dB	Signal: 70mVrms, 30MHz Carrier: 100mVrms, 28.25MHz Output: 1.75MHz
Carrier leak	SL641C		−25	−12	dB	
Intermodulation products	SL641C		−45	−30	dB	Signal 1: 42.5mVrms, 30MHz Signal 2: 42.5mVrms, 31MHz Carrier: 100mVrms, 28.25MHz Output: 3.75MHz
Carrier input impedance	Both		1kΩ & 4pF			
Signal input impedance	SL640C		500Ω & 5pF			
	SL641C		1kΩ & 4pF			
Output impedance	SL640C		350Ω & 8pF			Output 1
(see Operating Notes)	SL641C		8		pF	
Max. input before limiting	SL640C		210		mVrms	
	SL641C		250		mVrms	
Quiescent current consumption	SL640C		12	16	mA	
	SL641C		10	13	mA	
Noise figure	SL640C		15		dB	
	SL641C		12		dB	
Signal leak variation	Both		±2		dB	−55°C to +125°C
Carrier leak variation	Both		±2		dB	
Conversion gain variation	Both		±1		dB	

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Supply voltage	+9V
Free air operating temperature range	−55°C to +125°C

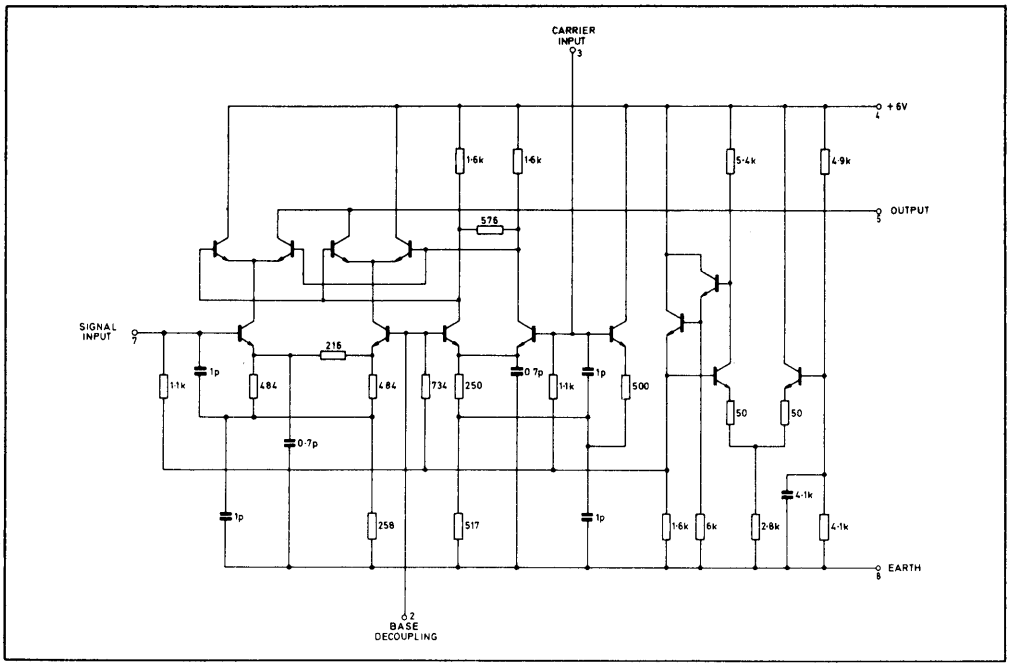


Fig. 2 Circuit diagram of SL641C

OPERATING NOTES

The SL640C circuit requires input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see electrical characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance.

Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at pin 2 would give rise to poor rejection figures and to distortion.

If the emitter follower is used, an external load resistor must be provided to supply emitter current. The quiescent output voltage from the emitter follower (pin 6) is +4.6V. To achieve maximum rejection figures at high frequencies, pin 1 (which is connected to the header) should be connected to earth and effective HT decoupling should be employed. The DC impedance should not exceed 800 ohms.

The SL641C is very similar to the SL640C but has, instead of a voltage output, a current output to enable a tuned circuit to be directly connected.

If both output sidebands are developed across the load (i.e. wideband operation), the AC impedance of the load must be less than 800Ω. If the output at one sideband frequency is negligible, the AC impedance may be raised to 1.6kΩ. It may be further raised if it is not desired to use the maximum input swing of 210mV rms.

The SL640C/641C may be used with supply voltages of up to +9 volts with increased dissipation.

Signal and carrier leaks may be minimised with 10kΩ potentiometers and 330kΩ resistors connected as shown in fig.3. R1 is adjusted to minimise signal leak; R2 to minimise carrier leak.

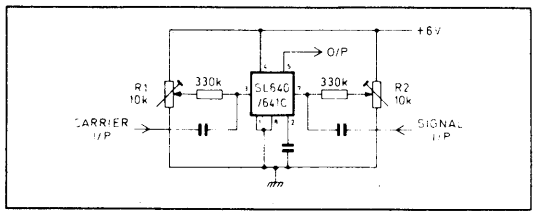


Fig. 3 Signal and carrier leak adjustments

SL650B & C SL651B & C

MODULATOR/PHASE LOCKED LOOP CIRCUITS

The SL650/1 are versatile integrated circuits capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650 or SL651, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage –, current –, or resistance – programmable from zero to greater than 10,000.

An auxiliary amplifier with a voltage gain of, typically, 5000 is incorpated in the SL650 for use when it is required to interface to specified levels and impedances. The auxiliary amplifier features low bias current (typically 25nA), fast recovery from overload, and a short-circuit output current of ±7.5mA.

The auxiliary amplifier is omitted from the SL651.

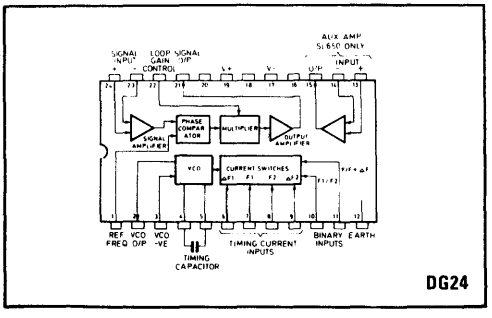


Fig.1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100:1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient:
  'B' Types 20 ppm/°C Max.
  'C' Types 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface
- Phase Comparator O/P Can Swing to Supply Voltages
- On-Chip Auxiliary Amplifier (SL650)

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	–55°C to +125°C

E3▷

ELECTRICAL CHARACTERISTICS

Test Conditions

Supply voltage: ±6V
Supply currents: 1.5mA
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	17, 19		±20		ppm/%	
Voltage at timing current inputs	6, 7, 8, 9		±10		mV	See note 2
VFO output, 'low' state	2		0	0.2	V	
VFO output, 'high' state	2	+1.1	+1.3		V	$R_L \geqslant 10k\Omega$
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	10, 11			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	10, 11	+2.4			V	
Input current	10, 11		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	23, 24		±2		mV	V_{out} = 0V
Input bias current	23, 24		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	23, 24		100		kΩ	
Common mode I/P voltage range	23, 24	±4			V	
Differential I/P to limit (AC)	23, 24		1.0	10	mV	See note 4
Output current	21, 22	±1.0	±2.0	±5.0	mA	I_{22} = 250μA
Current gain (pin 22 to pin 21)	21, 22	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	21,23,24	±100	±250		mA/V	See note 5
Output voltage, linear range	21	±5	±5.5		V	
Output current	21			±2	μA	I_{22} = 0
Phase comparator I/P 'low'	1	−4		−0.2	V	
Phase comparator I/P 'high'	1	+1.9		+5.3	V	
Auxiliary amplifier (SL650 only)						
Differential I/P offset voltage	13, 14		±2		mV	V_{out} = 0V
Input bias current	13, 14		0.025	0.5	μA	V_{in} = 0V
Differential I/P resistance	13, 14	0.2	3		MΩ	
Common mode I/P voltage range	13, 14	±4			V	
Voltage gain (13–14) to 15	13,14,15	1000	5000		–	
Output voltage range	15	±4	±4.8		V	$R_L \geqslant 2k\Omega$
Output current limit	15	±4	±6.5	±12	mA	

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL650C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin 21) voltage-limits first.
5. For a control current input to pin 22 of 250μA The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	± 7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

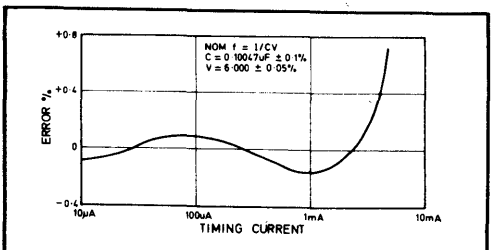


Fig.3 VFO linearity

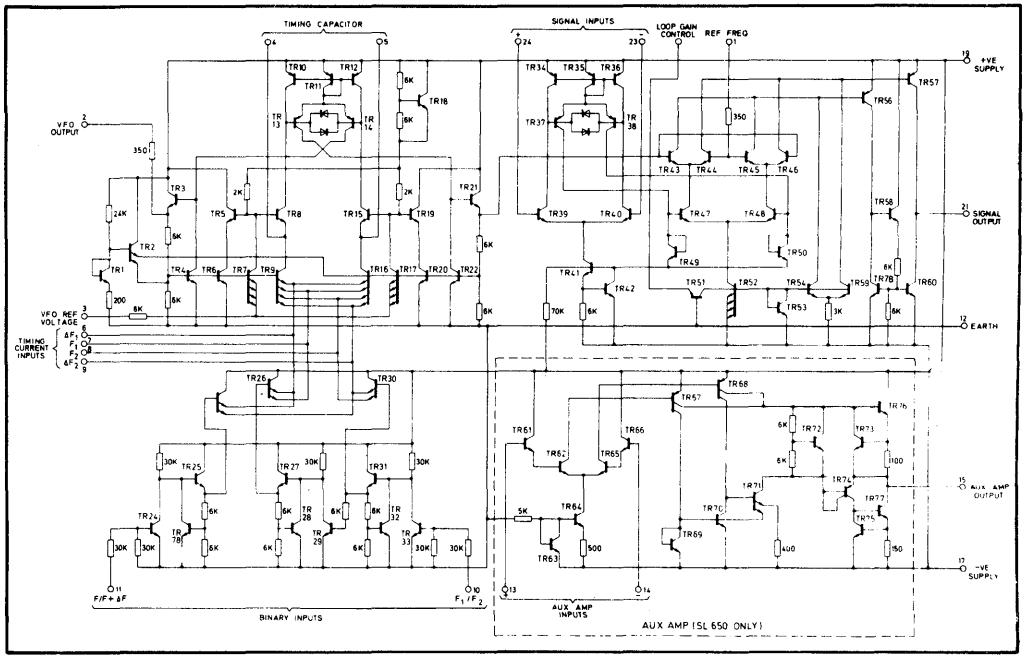


Fig. 2 Circuit diagram of SL650/SL651

OPERATING NOTES

Basic VFO Relationships

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 4 and 5, and directly proportional to the VFO timing current (see Fig.4). Four current switches, controlled by TTL-compatible logic inputs on pins 10 and 11 select a combination of external resistors (connected to pins 6, 7, 8 and 9) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to 0V however, then only the current switch associated with pin 7 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig.4), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig.5, the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR} \cdot \frac{V_R}{V_3}$$

where f is in kHz, I in mA, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 3), then

$$V_R = V_3$$

$$\text{and } f = \frac{1}{CR}$$

Pin 3 is normally connected to the chip negative supply; if, however, pin 3 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR} \cdot \frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 3

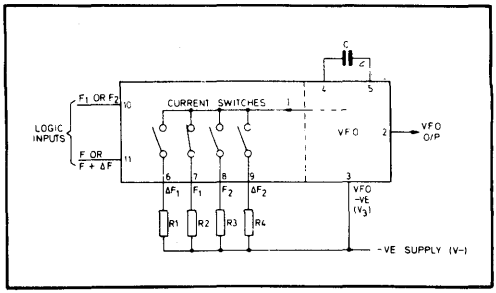


Fig.4 VFO and binary interface

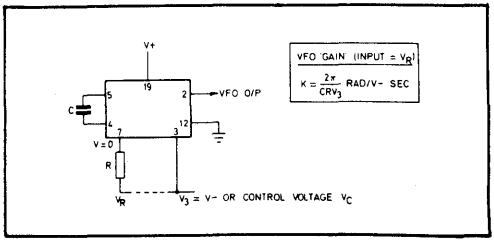


Fig.5 VFO basic configuration

The timing current I should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig.4, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 10	Pin 11	Timing Pins	VFO Frequency
LO	LO	7	$\frac{1}{CR_2}$
LO	HI	6 & 7	$\frac{1}{CR_2} + \frac{1}{CR_1}$
HI	LO	8	$\frac{1}{CR_3}$
HI	HI	8 & 9	$\frac{1}{CR_3} + \frac{1}{CR_4}$

Table 1 Binary interface relationships

Phase Comparator

The phase comparator parameters are defined as follows (see Fig.6):

$$\text{Overall transconductance} = \frac{I_{21}}{V_{24} - V_{23}}$$

$$\text{Overall voltage gain} = \frac{V_{21}}{V_{24} - V_{23}}$$

The input amplifier will limit when the peak input ($V_{24} - V_{23}$) exceed ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

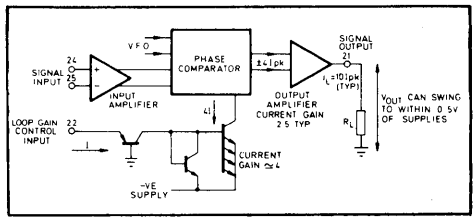


Fig.6 Phase comparator

SL652C

MODULATOR/PHASE LOCKED LOOP

The SL652C is a versatile integrated circuit capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using this device, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage – current – or resistance – programmable from zero to greater than 10,000.

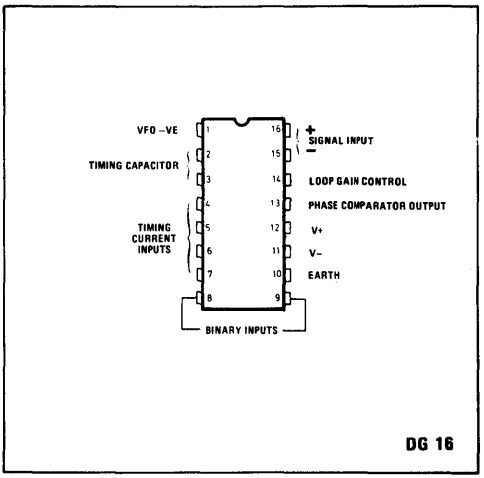


Fig. 1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100: 1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient: 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/%.Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	−55°C to +125°C
Supply Currents	1.5mA typ.

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators
- Stable Current-Controlled Oscillators

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage: ±6V
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	−	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	11, 12		±20		ppm/%	
Voltage at timing current inputs	4, 5, 6, 7		±10		mV	See note 2
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	8, 9			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	8, 9	+2.4			V	
Input current	8, 9		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	15, 16		±2		mV	V_{out} = 0V
Input bias current	15, 16		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	15, 16		100		kΩ	
Common mode I/P voltage range	15, 16	± 4			V	
Differential I/P to limit (AC)	15, 16		1.0	10	mV	See note 4
Output current	13, 14	±1.0	±2.0	±5.0	mA	I_{14} = 250μA
Current gain (pin 14 to pin 13)	13, 14	±4	±10		−	See note 5
Transconductance, O/P/diff.I/P	13, 15, 16	±100	±250		mA/V	See note 5
Output voltage, linear range	13	±5	±5.5		V	
Output current	13			±2	μA	I_{14} = 0

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL652C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin. 13) voltage-limits first.
5. For a control current input to pin. 14 of 250μA. The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

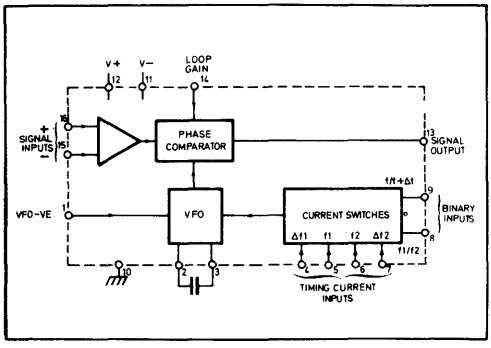


Fig. 2 SL652C block diagram

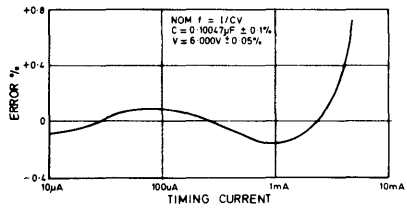


Fig. 3 VFO linearity

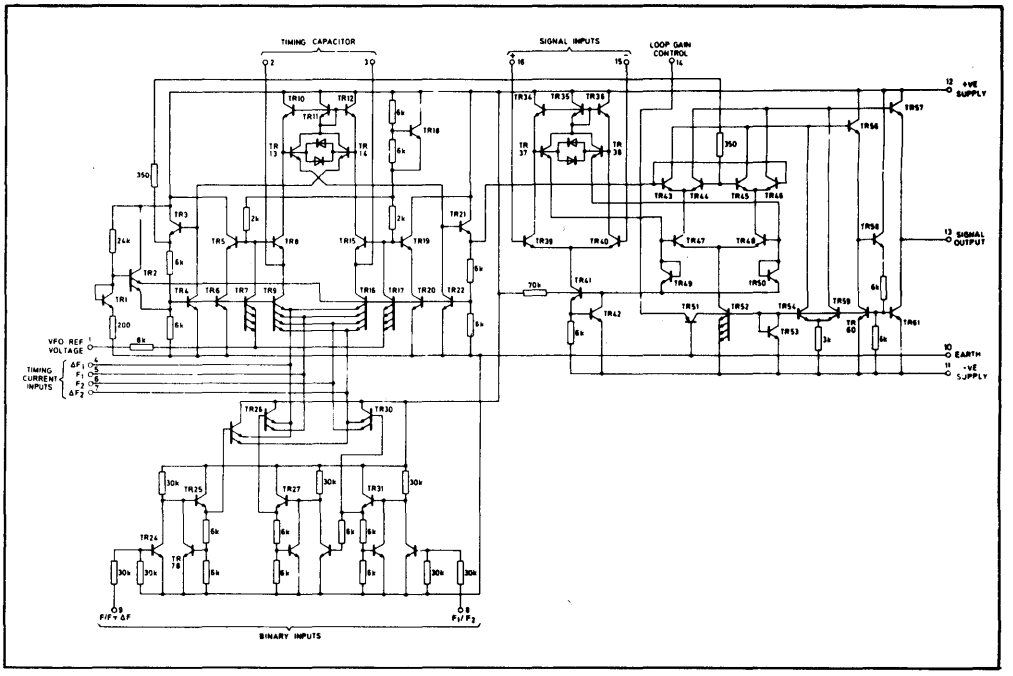


Fig. 4 Circuit diagram of SL652

OPERATING NOTES

Basic VFO Relationships

The oscillator output is normally taken from the phase comparator output by biasing the signal inputs a few hundred millivolts apart. If a direct oscillator output is required when the phase comparator is otherwise employed, it should be taken from pin 2 or 3 (which may affect oscillator stability). Alternatively, an SL651C can be used in place of the SL652C.

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 2 and 3, and directly proportional to the VFO timing current (see Fig. 5). Four current switches, controlled by TTL-compatible logic inputs on pins 8 and 9 select a combination of external resistors (connected to pins 4, 5, 6 and 7) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to OV however, then only the current switch associated with pin 5 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig. 5), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig. 6 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR}\frac{V_R}{V_1}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 1) then

$$V_R = V_1$$

$$\text{and } f = \frac{1}{CR}$$

Pin 1 is normally connected to the chip negative supply; if, however, pin 1 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR}\frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 1.

The timing current should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig. 5, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 8	Pin 9	Timing Pins	VFO Frequency
LO	LO	5	$\frac{1}{CR_2}$
LO	HI	4 & 5	$\frac{1}{CR_2}+\frac{1}{CR_1}$
HI	LO	6	$\frac{1}{CR_3}$
HI	HI	6 & 7	$\frac{1}{CR_3}+\frac{1}{CR_4}$

Table 1 Binary interface relationships

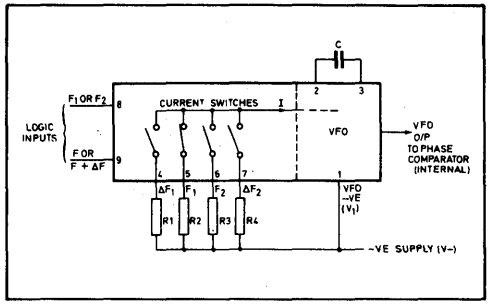


Fig. 5 VFO and binary interface

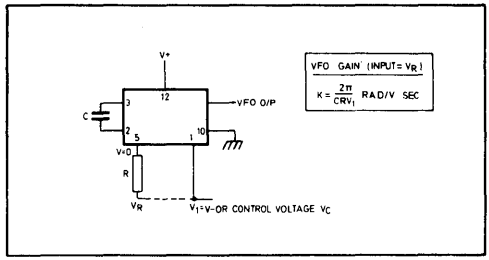


Fig. 6 VFO basic configuration

Phase Comparator

The phase comparator parameters are defined as follows (see Fig. 7):

$$\text{Overall transconductance} = \frac{I_{13}}{V_{16} - V_{15}}$$

$$\text{Overall voltage gain} = \frac{V_{13}}{V_{16} - V_{15}}$$

The input amplifier will limit when the peak input ($V_{16} - V_{15}$) exceeds ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

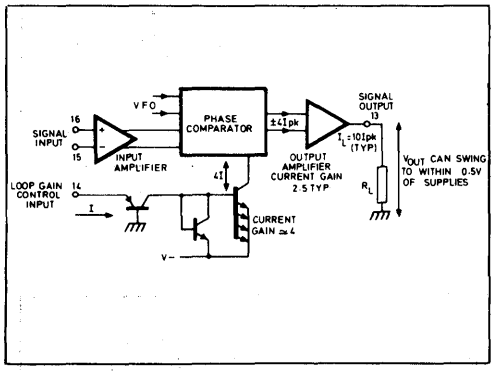


Fig. 7 Phase comparator

Plessey
Semiconductors

SL680C SL1680C

CRYSTAL OSCILLATOR MAINTAINING CIRCUITS

The SL680C and SL1680C are bipolar integrated circuits designed to maintain the oscillation of an external series resonant crystal without significant degradation of frequency stability. The sinewave output has about 3% harmonic distortion and its level is independant of crystal activity. Crystals may be used in their fundamental or overtone modes with only minor circuit changes.

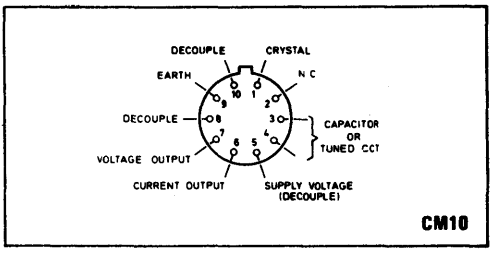


Fig. 1 Pin connections, SL680C

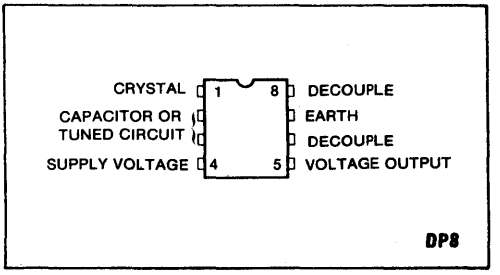


Fig. 2 Pin connections, SL1680C

FEATURES

- Insignificant Degradation of Crystal Frequency Stability.
- Frequency Range 100 kHz to 100 MHz.
- Output Level Independent of Crystal Parameters.
- Overtone Crystals Can Be Used.
- Voltage and Current Outputs Provided.
- Harmonic Distortion Typically Less Than 3%.
- Very Low Crystal Power

OPERATING NOTES

A block diagram of the SL680C/1680C is shown in Fig. 3. The circuit consists of a single transistor amplifier with the crystal decoupling its emitter. The output of this amplifier drives a fixed gain amplifier with an emitter follower output capable of voltage driving low impedance loads, and a free collector output for driving fixed impedances or tuned circuits (SL680C only).

The output from the fixed gain amplifier also goes to a detector and, via a variable attenuator, to the base of the single transistor amplifier. The variable attenuator is controlled by the detector output. The circuit contains an internal supply regulator, enabling it to be operated from a range of supply voltages.

In operation, the signal fed back to the tuned single transistor amplifier causes the system to oscillate at the resonant frequency of the crystal. A DC signal derived from the output level of the fixed gain amplifier and applied to the attenuator maintains the output at constant level irrespective of the activity of the crystal.

The phase shift through the system has been kept as low as possible and, even more importantly, varies very little with temperature or power supply voltage. Since varying phase shift is the commonest cause of varying frequency in crystal oscillators (with the exception, of course, of variations in the crystals themselves) this low phase shift ensures that the oscillator's frequency variation with temperature and supply voltage will be minimal. The actual values will depend upon the crystal used but typical temperature variation is 10^{-3} ppm/ °C over the

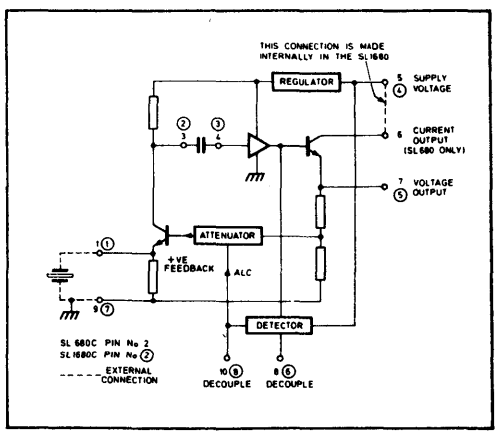


Fig. 3 SL680C/1680C block diagram

range —10 °C to + 80 C and 10—1 ppm/V over a power supply range of 6 to 10 volts. These figures are independent of any variations due to the crystal itself.

Variations in the crystal are often caused by excessive power dissipation. The SL680C/SL1680C is unlikely to suffer from this problem since the crystal dissipation is held to the order of 0.5μ Watt.

Coupling between the tuned amplifier and the fixed gain amplifier is usually by a capacitor and the circuit oscillates at the crystal's fundamental frequency. If overtone operation is required the coupling must be by a high pass filter to ensure that the loop gain at the overtone exceeds the loop gain at the fundamental. For third Overtone operation this high pass filter may be as simple as a very small value capacitor but for higher overtones a tuned circuit of some sort is necessary.

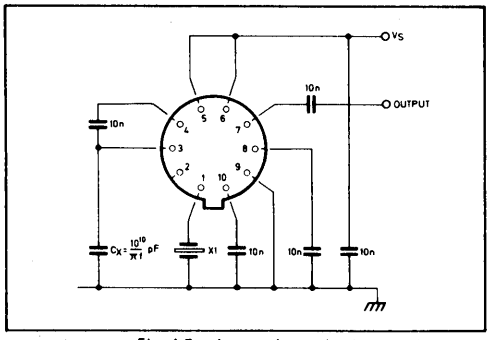


Fig. 4 Fundamental test circuit

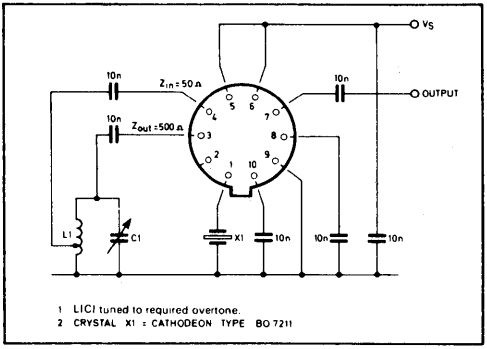


Fig. 5 Third overtone test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

Temperature	22 °C ± 2 °C
Supply Voltage	6V
Load Impedance	500Ω
Crystal Fundamental 16.3 MHz (series mode)	

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Output Voltage	0.1	0.15	0.2	Vrms	SL680C
	0.08	0.15	0.22	Vrms	SL1680C
Supply Current		7	15	mA	SL680C
		7			SL1680C
Max. operating frequency		100		MHz	
Current output		1		mAp—p	SL680C
Harmonic output		—30		dB	wrt 16.3MHz output
Frequency error (note 1)		5		ppm	
Frequency stability (note 2)		0.1		ppm/volt	Vs=6V to 10V
		10—3		ppm/ °C	—10 °C to + 80 °C
Crystal dissipation		50Rs		nW	Rs = Crystal series loss resistance

NOTES

1. The frequency error is the difference between frequency of oscillation obtained using the SL680C/SL1680C and the frequency obtained in a zero phase measurement system such as described in BS9610.
2. These stability figures are dependant on the crystal used and are given for guidance only.

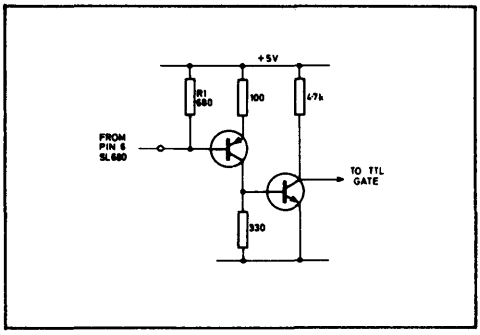


Fig. 6 Buffer for driving TTL

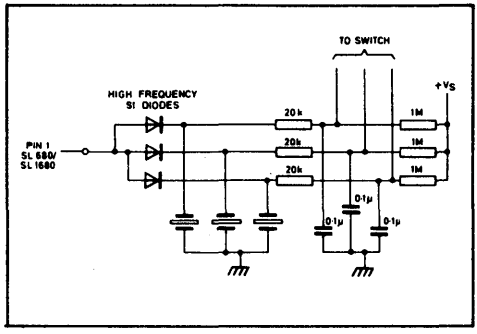


Fig. 7 Crystal selection interface

Absolute Maximum Ratings

(Non-simultaneous)

Storage temperature: SL680C —55°C to +150°C
SL1680C —30°C to +85°C
Operating temperature: SL680C —55°C to +125°C
SL1680C —30°C to +70°C
Supply voltage +12V

SL1030C

200MHz WIDEBAND AMPLIFIER

The SL1030 is a silicon integrated circuit designed for use as a general purpose very wideband amplifier. External components enable users to tailor the characteristics of the amplifier for particular applications. The gain can be selected between 20 and 60dB; the input impedance can be 50Ω, 75Ω or 1kΩ, and the compromise between current consumption and output swing can be selected by the external components.

A regulator is provided on the chip, enabling supply voltages from 8 to 15 volts to be used with no variation in characteristics. Alternatively, the regulator can be bypassed and supplies from 4.0 to 10 volts used.

The amplifier is protected against damage from input voltage transients and is stable when driving capacitive and inductive loads.

FEATURES

- Bandwidth up to 200 MHz
- Low Noise
- Single Supply
- Input Impedance Adjustable – 50Ω, 75Ω or 1kΩ
- Gain Programmable between 20dB and 60dB
- Drives Capacitive or Inductive Loads

APPLICATIONS

- Wideband Pulse Amplifiers
- Frequency Selective IF Amplifiers
- Low Noise Preamplifiers

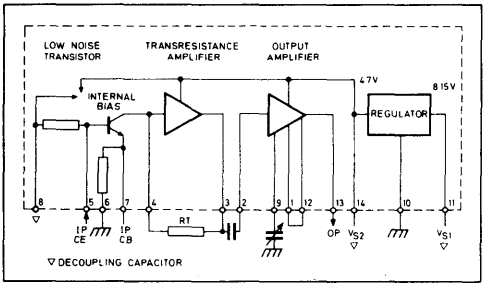


Fig. 1 General schematic

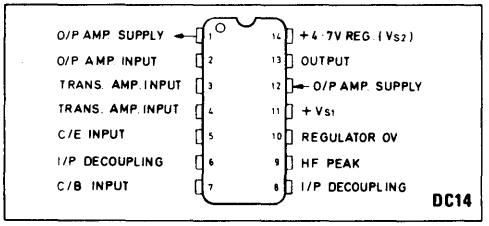


Fig. 2 Pin connections (top)

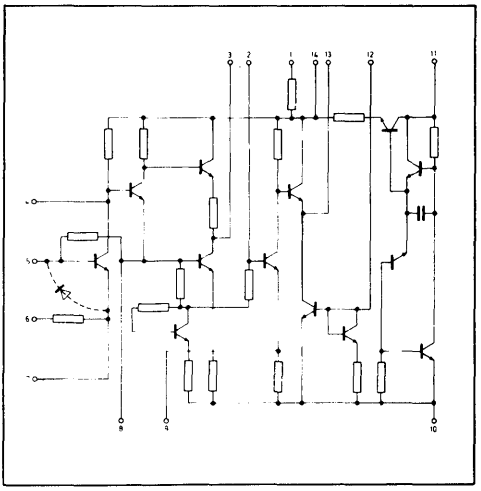


Fig. 3 Circuit diagram

QUICK REFERENCE DATA

Supply Voltage	+4V to +15V
Supply Current at V_S = 10V	20 mA (Typ.)
Voltage Gain at 100 MHz	40dB (Typ.)
Noise Figure at 100 MHz, R_S = 50Ω	3dB (Typ.)
Second Order Intermodulation Distortion	–50dB (Typ.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C
V_{S1} 10V
R_1 = 1 kilohm
R_2 = 32 kilohms

Characteristic	Test Cct.	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain	A	28	30	32	dB	f = 100 MHz
	B	37	40	43	dB	" " "
Gain flatness			± 0.5		dB	f = 10 kHz to 150 MHz (Note 1)
Noise figure	A		6.5	8.0	dB	f = 100 MHz, R_S 50Ω
	B		3.0	4.5	dB	
Gain compression	A		0.2	1.0	dB	f = 100 MHz, load impedance = 50Ω P_{out} = 0dBm
Output voltage	B		1		V pk/pk	f = 10 MHz, load impedance = 100Ω
Rise time	B		3		ns	V_{out} = 1.0 V pk/pk
Input VSWR	A		1.2			f = 10 kHz to 150MHz w.r.t. 50Ω
Supply current			20	30	mA	V_{S1} = 10V or V_{S2} = 5V
Regulation $\Delta V_{S2}/\Delta V_{S1}$			1	5	%	V_{S1} = 10V to 15V
Intermodulation distortion						
2nd order	A		−50		dB*	P_{out} = 0dBm (Note 2), V_{S2} = 10V
3rd order	A		−60		dB*	
Harmonic distortion						
2nd harmonic	A		−30		dB*	f = 100 MHz, P_{out} = 0dBm, V_{S2} = 10V, R_L = 50Ω
3rd harmonic	A		−40		dB*	
Input impedance						
Common base			16		Ω	f < 10 MHz
Common emitter			1		kΩ	" "

NOTES

1. The gain flatness is dependent on layout and on the value of the peaking capacitor. See OPERATING NOTES for details.
2. In each of two tones at 10 and 10.5 MHz, R_L = 50Ω

* Referred to output.

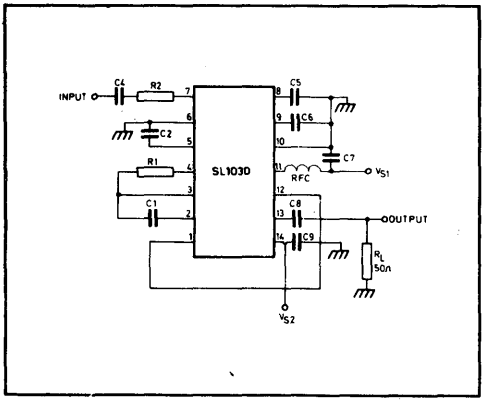


Fig. 4 Test circuit A — common base

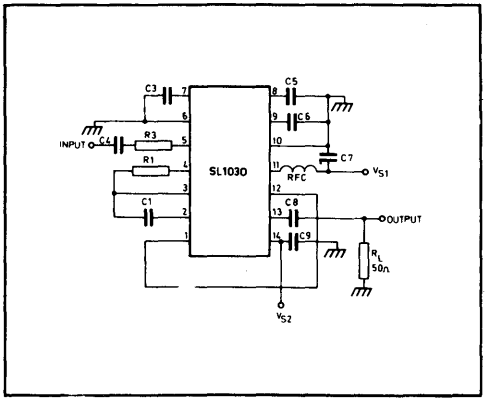


Fig. 5 Test circuit B — common emitter

TYPICAL ELECTRICAL CHARACTERISTICS

The following conditions apply to the characteristics given in Figs. 6 to 16 unless otherwise stated:

Free air temperature	22°C
Load resistance	50Ω
R_T	1 kΩ

Intermodulation products (Fig. 6) are measured with specified output power in each of two tones at 10 MHz and 10.5 MHz.

The values for C_P quoted in Figs. 12 and 13 were selected with R_L = 50Ω but will vary with load impedance and circuit layout.

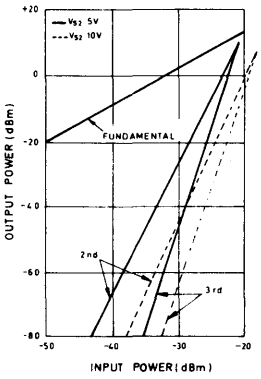


Fig. 6 Intermodulation products

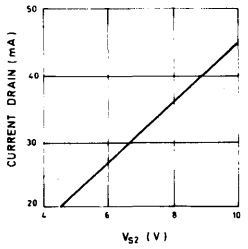


Fig. 7 Supply current v. unreg. supply voltage

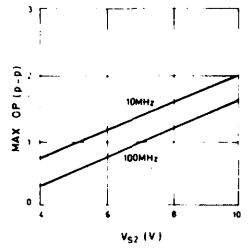


Fig. 8 Max o/p voltage v. unreg. supply voltage

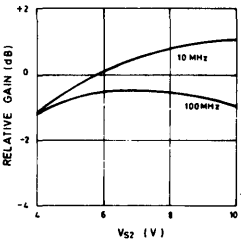


Fig. 9 Common base gain v. unreg. supply voltage

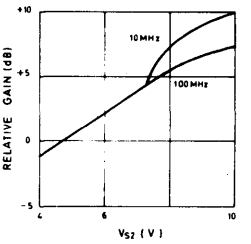


Fig. 10 Common emitter gain v. unreg. supply voltage

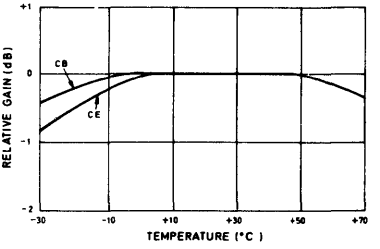


Fig. 11 Gain v. temperature

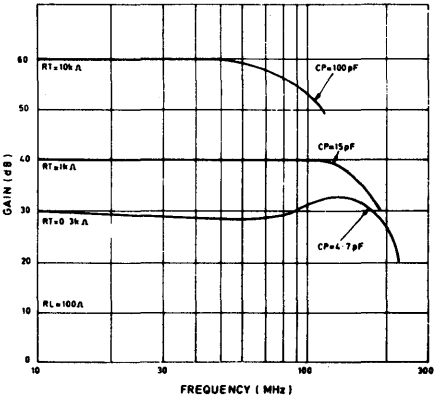


Fig. 12 Common emitter gain v. frequency

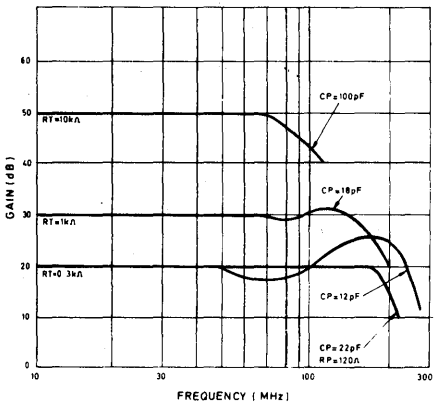


Fig. 13 Common base gain v. frequency

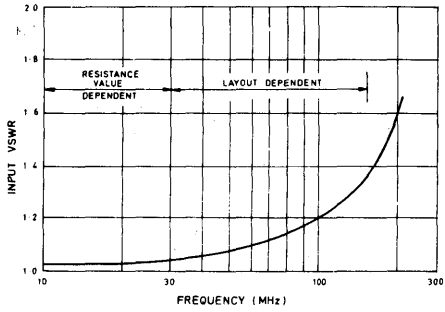


Fig. 16 Input VSWR v. frequency

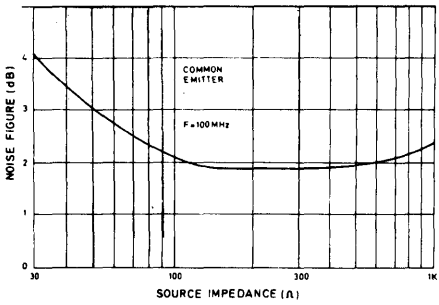


Fig. 14 Noise figure v. source impedance

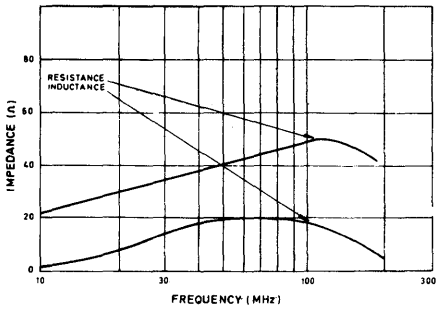


Fig. 15 Output impedance v. frequency

OPERATING NOTES

Low Noise Input Stage

As shown in Fig. 1, the input transistor can be used in common base or common emitter by using either pin 7 or pin 5 as the input, the other pin being decoupled. If a well-defined 50 or 75Ω input impedance is required, then a circuit similar to test circuit A (Fig. 4) should be used. An accuracy of ± 5% can be expected in the input impedance of this circuit since the input impedance of the common base stage is very reproducible and also is to some extent masked by the external resistor. A return loss of 30dB up to 100 MHz can be achieved with careful layout and the use of a physically small, accurate external resistor. The value of the resistor should be 56Ω for 75Ω input impedance and 33Ω if 50Ω input impedance is required.

The noise figure of this transistor is flat from the flicker noise knee around 10 Hz to over 150 MHz.

Transresistance Amplifier

The transresistance amplifier will operate correctly for values of R_T from 200Ω to 10 kΩ. The voltage gain of the complete amplifier is of course directly proportional to R_T. See Figs. 12 and 13.

Output Stage

When the internal regulator is bypassed for applying the supply voltage to pin 14, some control of the quiescent current is possible. The biasing circuitry has been designed so that the individual currents track together with the supply voltage and with each other. This enables a significant improvement to be made in the output swing into low impedance loads at the expense of increased current consumption. See Fig. 7. The quiescent current of the first device also increases, giving an increase in gain in the common emitter configuration. The quiescent current in the output stage can be varied by means of an external resistor. The link between pins 1 and 12 must be removed and a resistor added between pins 14 and 12. The current is 10 mA with 2.5 kΩ and is approximately inversely proportional to the resistor value.

Peaking Capacitor C_P

The frequency response of the amplifier is dominated by the output emitter follower which begins to roll off at about 50 MHz. The high frequency peaking capacitor is used to compensate for this roll-off and also that due to stray inductance and capacity in the external circuitry. The values of peaking capacitor used in the test circuits have been selected for best gain flatness in the test fixture but are not necessarily typical of the values required in different layouts since the stray reactances associated with a plug-in test facility are inevitably higher than in a directly wired circuit. The typical curves were measured with an SL1030 directly soldered into a PC board and the values of the peaking capacitor given will be more typical of the normal situation.

Layout and Stability

Since gains of 40dB are available up to VHF frequencies normal high frequency layout precautions are necessary with respect to grounding and decoupling. Decoupling capacitors should be low inductance ceramic types (Erie Weecons are ideal) and to ensure good earth connections a continuous ground plane should be provided around and underneath the circuit. Decoupling of pins 5 or 7 is critical and inadequate decoupling of pin 14 can cause instability. Since no overall feedback is used, the amplifier is very tolerant of load reactance and no instability has been observed even with pure capacitive loads. A certain amount of care is needed when using the internal regulator. If the decoupling on pin 11 is effective above 200 MHz, then instability can occur within the regulator. This can be completely stopped by inserting an inductance of a few hundred nanohenries between the decoupling capacitor and pin 11 as shown on the test circuits.

ABSOLUTE MAXIMUM RATINGS

V_{S1} (Pin 11)	+15V
V_{S2} (Pin 14)	+10V
Storage temperature	−55°C to +150°C
Operating temperature (ambient)	−55°C to +125°C

Plessey
Semiconductors

SL1202C SL1203C

LOW NOISE PREAMPLIFIERS

The SL1202C and SL1203C are monolithic silicon integrated circuits designed primarily for use as a low noise preamplifiers in infra-red systems. Their exceptional noise performance and high gain make these amplifiers suitable for use in systems requiring low noise amplification from a source in the range 30Ω to 120Ω. The circuit can be divided into two sections. A single-ended IN/single-ended OUT low noise preamplifier and a single-ended IN, balanced OUT post amplifier. The preamplifier alone is available in an 8-lead TO5 encapsulation as the SL1202C and the preamplifier plus post amplifier in a 16-lead DIL, as the SL1203C. The input transistor has a base resistance of less than 20Ω, enabling very good noise performance to be achieved from low impedance sources. The balanced output stage has adjustable quiescent current which gives the user the facility of minimising power consumption within the limit imposed by driving the required output voltage into the specified load impedance. This load impedance can be as low as 50Ω. The gain of the preamplifier can be set in the range 35 to 57 dB by an external resistor.

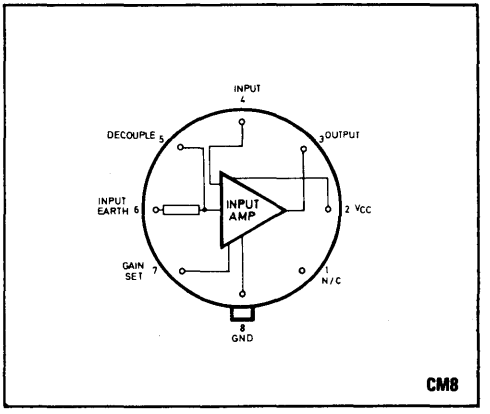


Fig. 1 Block diagram of SL1202C

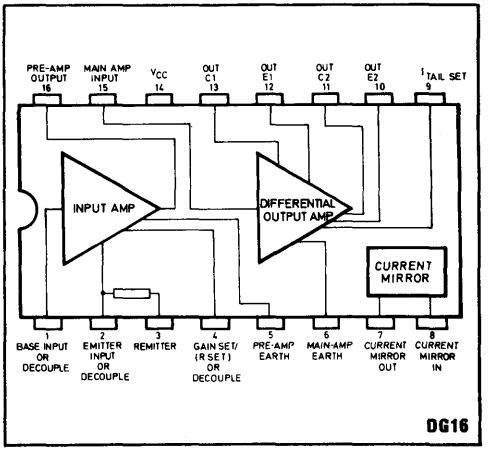


Fig. 2 Block diagram of SL1203C

FEATURES

- Gain: 35 to 67 dB (Set by external components)
- Bandwidth: 3.6 MHz
- Input Impedance: 2kΩ
- Equivalent Input Noise: (R_S = 50Ω) 0.9 nV/√Hz
- Low I/F Noise
- Balanced Output Stage
- Low Power Consumption

ABSOLUTE MAXIMUM RATINGS

V_{CC}	+ 10V
Operating temperature	−55°C to +125°C
Storage temperature	−55°C to +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

V_{CC} = +6V
Source resistance = 50Ω
T_{amb} = 25°C
Load impedance (i) SL1202 = 1MΩ (ii) SL1203 = 100Ω balanced

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Upper cut-off frequency (−3dB)	Both	2.5	3.6		MHz	
Input impedance	Both		2.0		kΩ	
Output impedance	SL1202		80		Ω	
	SL1203	See operating note 1				
Voltage gain	SL1202	52	57	62	dB	R_{set} = 0
	SL1202		35		dB	R_{set} = 6kΩ
	SL1203	62	67	72	dB	R_{set} = 0
	SL1203		37		dB	R_{set} = 20kΩ
Output voltage	SL1202	2.5	3.5		Vp-p	R_{set} = 0
	SL1202		1.0		Vp-p	R_{set} = 6kΩ
	SL1203	0.4	0.7		Vp-p	R_{set} = 0, see operating note 1
	SL1203		0.6		Vp-p	R_{set} = 20kΩ see operating note 1
Equivalent input noise voltage	Both		0.9	1.2	nV/√Hz	R_S = 50Ω
Supply current	SL1202		3	5	mA	
	SL1203		20	30	mA	See operating note 1

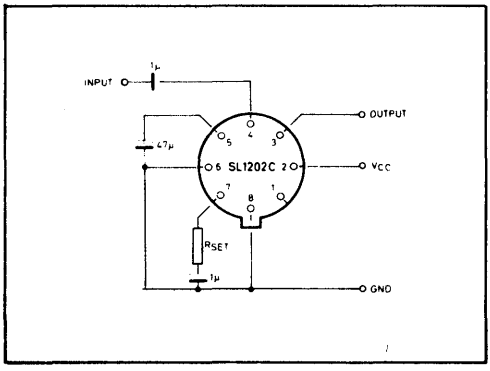


Fig. 3 SL1202C test circuit

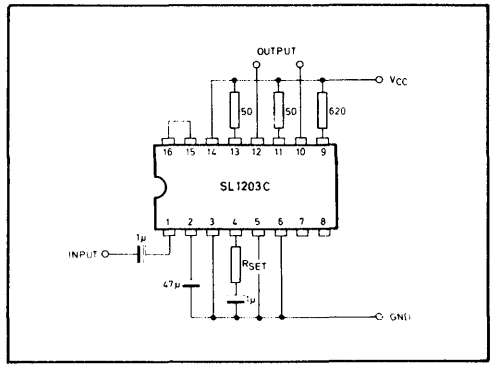


Fig. 4 SL1203C test circuit

TYPICAL ELECTRICAL CHARACTERISTICS (Figs. 5, 6 & 7)

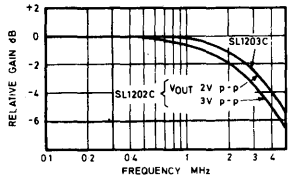


Fig. 5 Frequency response

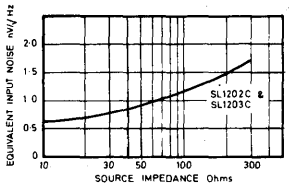


Fig. 6 Equivalent input noise v. source impedance

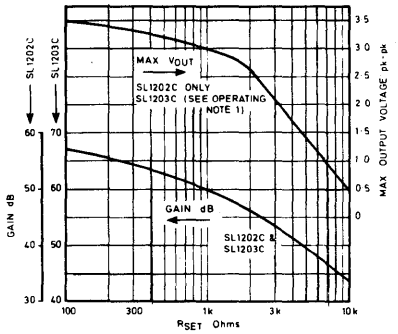


Fig. 7 Max. output voltage and gain v. R_{set}

OPERATING NOTES

1. The Output Amplifier (SL1203C)

This consists of two cascaded differential stages, and is primarily intended for driving a balanced 100Ω load (Pins 11 and 13). The tail current of the output stage may be increased from its preset value of 1 mA by connecting a resistor between Pins 9 and 14. The maximum output swing is determined by the value of the output stage tail current, up to a 1.0 volt peak-to-peak differential maximum. This resistor should be not less than 500Ω to avoid exceeding the current ratings of the transistors.

The output swing available, and the external resistor between Pins 9 and 14 are related by the expression:

$$5V_{swing} = \frac{V_{SS} - 0.75}{\frac{R.10}{10+R} + 0.75} \quad \text{where V is in volts, R is in k}\Omega$$

e.g. for R =1kΩ, V_{SS} = 6.0 volts

$$V_{swing} = \frac{5.25}{5 \times 1.74} = \mathbf{600mV}$$

for R = ∞, V_{SS} = 6.0 volts

$$V_{swing} = \frac{5.25}{5 \times 10.75} = \mathbf{100mV}$$

Asymmetric limiting, caused by differential output offsets, may reduce the usable swing below the theoretical maximum. Offset may be trimmed out by means of a resistor between Pin 16 and ground (or V_{SS}). The specifications for output swing of the SL1203C apply to untrimmed units.

Varying R_{set} reduces the output swing capability of the SL1202C as shown in the typical electrical characteristics. The output swing of the SL1203C is unaffected by R_{set} for values less than 20 kΩ. Hence a gain reduction of 30 dB can be obtained without degrading the output swing capability.

2. Input Stage

The input is uncommitted and may be arranged as common base or common emitter. Common emitter gives the highest input impedance, and thus the lowest value of input coupling capacitor for a given LF response. This is the configuration described in this data sheet. However, the common base configuration can also have certain advantages, for example a CMT detector can be directly coupled into the amplifier — the quiescent current of the first stage then provides detector bias.

3. Current Mirror

Included in the SL1203C is an NPN current mirror with 2:1 scaling (Pins 7 and 8); a bias supply for CMT infra-red detectors. The mirror is tied to the output amplifier ground rail, and thus can only be used when the output amplifier is powered.

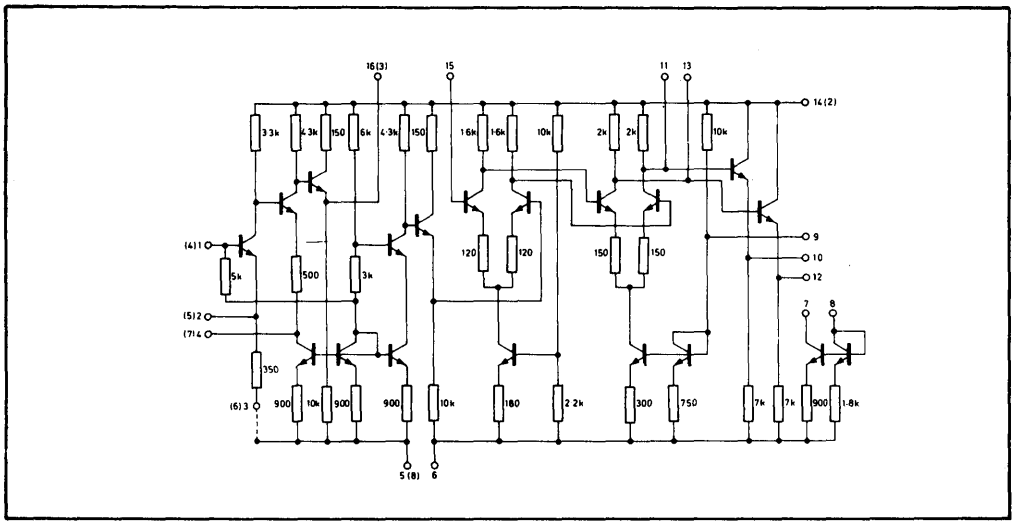


Fig. 8 Circuit diagram of SL1202C/SL1203C. (Pin numbers are shown thus: (4)-SL1202C, 4-SL1203C.)

Plessey
Semiconductors

SL1205C

LOW NOISE PREAMPLIFIER

The SL1205 is a monolithic integrated circuit designed specifically for use in infra-red systems as a low-noise preamplifier interfacing with a CMT detector.

To reduce physical size, the SL1205 is encapsulated in a TO-71 package; in addition, this design minimises the number and size of external capacitors required.

The 6.5MHz-wide bandwidth enables fully TV-compatible video response to be obtained. In such systems it is envisaged that the sweep-out mode of detector operation will be used.

Applications in other systems are not precluded: the amplifier has an input impedance of 2kΩ, an output impedance of about 50Ω and an optimum noise performance from low impedance sources (~100Ω). Power consumption is very low: 10mW at V_{cc} = 5.0 volts, and only a single positive power supply is required.

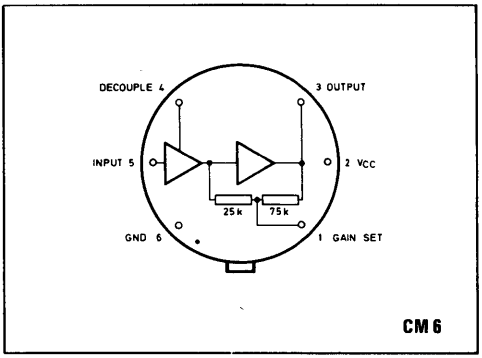


Fig. 1 Pin connections (viewed from the top)

FEATURES

- Gain 49-59dB
- Bandwidth 6.5MHz
- Equivalent Input Noise Voltage 0.8nV/√Hz
- Low IF Noise
- Small Encapsulation (TO-71)
- Minimum External Components
- Low Power Consumption

QUICK REFERENCE DATA

- Supply Voltage 5 to 9V
- Supply Current 1.8mA Typ.
- Upper Cut-Off Frequency 5 MHz Min.

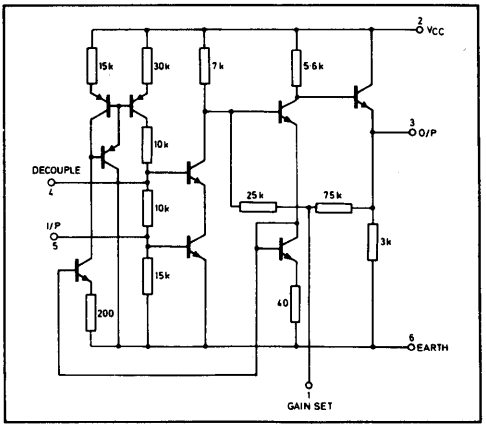


Fig. 2 Circuit diagram

OPERATING NOTES

Noise Performance

The noise performance of the SL1205 is optimum for source impedances in the range 20 to 150Ω. The quiescent current of the input transistor is approximately 0.5mA and its base resistance is 20Ω. The operating current has been chosen to give a high input impedance, hence reducing the value of input coupling capacitor required without a large degradation in noise performance. Flicker noise is not normally a problem, the knee frequency being below 100Hz.

Output Voltage

The maximum output voltage before clipping is guaranteed at 1.5V min. at V_{CC} = 5 volts into a 10kΩ. in parallel with 5 pF load. Larger output voltages can be obtained by increasing the supply voltage. Driving low impedance or capacitive loads is eased by increasing the quiescent current of the output emitter follower, achieved by connecting an external resistor between pin 3 and earth. The resistor should be greater than 200Ω to avoid exceeding the ratings of the output transistor.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
V_{CC} = 5.0V
T_{amb} = +25°C
Source Resistance = 50 Ω
Load Impedance = 10k Ω in parallel with 5pF

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	56	59	62	dB	$R_{set} = \infty$
		48			$R_{set} = 0$
Equivalent Input Noise Voltage		0.8	1.2	$nV/\sqrt{Hz}$	$R_{set} = \infty$
		0.8		$nV/\sqrt{Hz}$	$R_{set} = 0$
Output voltage	1.5	2.0		V p-p	
Supply current		1.8	3.0	mA	
Output resistance		50		Ω	
Input resistance		2		kΩ	
Input capacitance		15		pF	
Upper cut-off frequency	5	6.5		MHz	V_{out} = 10mV p-p
		6.2		MHz	V_{out} = 1.5V p-p

ABSOLUTE MAXIMUM RATINGS

V_{CC} (pin 2 wrt ground) 10.0V
Storage Temperature −55°C to +150°C
Operating Temperature −55°C to +125°C

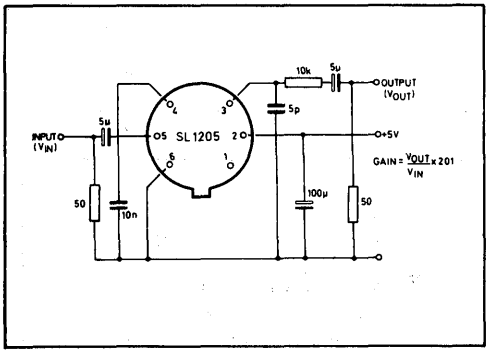


Fig.3 Test circuit

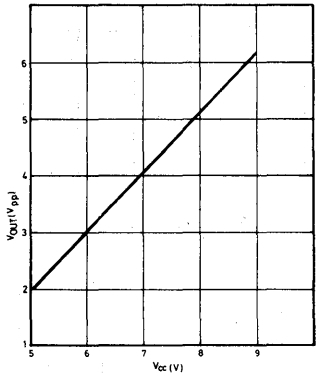


Fig.4 Output voltage v. supply voltage

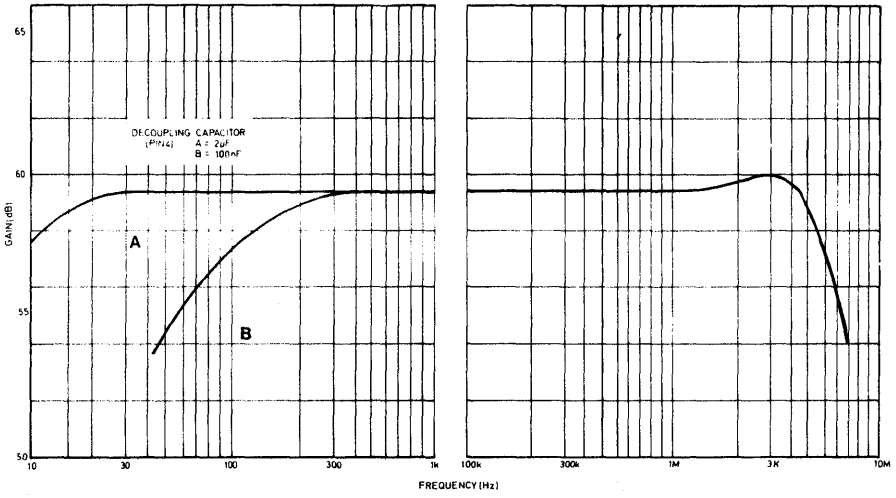


Fig.5 Gain v. frequency

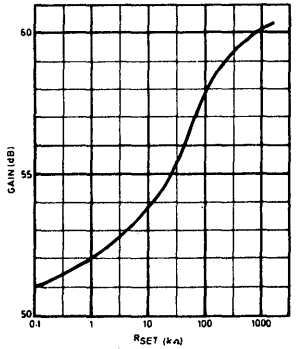


Fig.6 Gain v. R_{set}

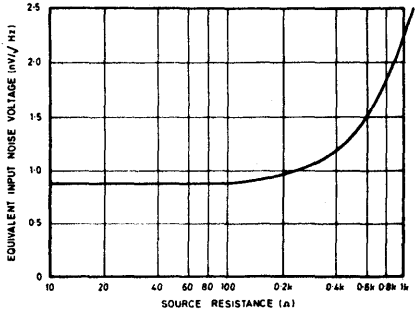


Fig.7 Noise characteristic

TYPICAL APPLICATIONS

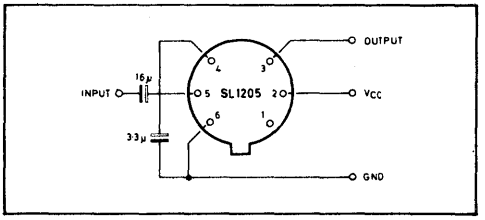


Fig.8 Gain 60 dB (fixed), frequency response 5Hz to 6.5MHz

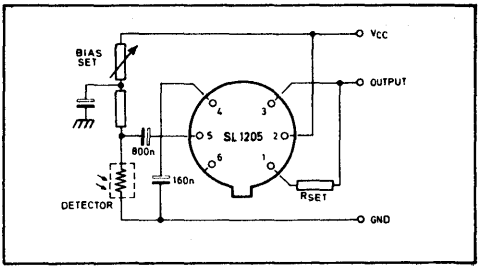
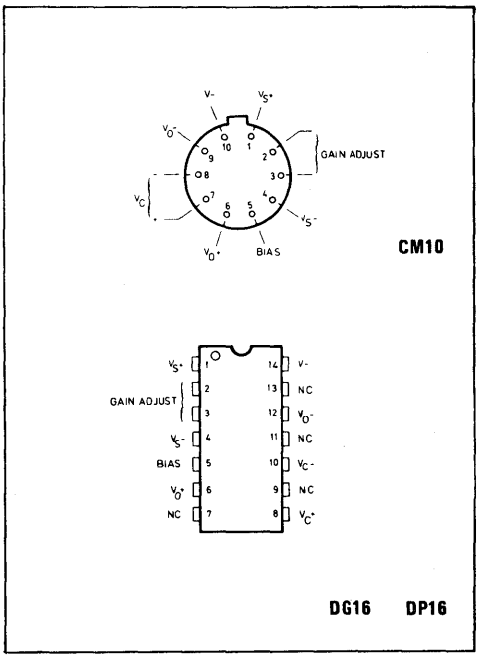


Fig.9 Gain 50 to 60 dB (set by R_{set}), frequency response 100Hz to 6.5MHz, CMT detector.

SL1496C SL1596C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1596C and SL1496C are versatile monolithic integrated circuit double balanced modulators/demodulators, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1596 has an operating temperature range of −55°C to +125°C, whilst that of the SL1496 is 0°C to +70°C.



FEATURES

- Carrier Suppression — 65dB Typ. @ 500 kHz, 50dB Typ. @ 10 MHz
- Common Mode Rejection — 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Telephone FDM Systems

ORDERING CODES

SL1496C — CM, SL1496C — DG, SL1496C — DP
SL1596C — CM, SL1596C — DG

ABSOLUTE MAXIMUM RATINGS

(Pin number reference to CM package)

Applied voltage*	30V
Differential input signal (V_7—V_8)	5V
Differential input signal (V_4—V_1)	$(5+15R_E)$V
Bias current (I_5)	10mA
Operating temperature range	
SL1496	0 °C to +70 °C
SL1596	−55 °C to +125 °C

CM Package

Storage temperature range	−55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	680mW

DG Package

Storage temperature range	−55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	600mW

DP Package

Storage temperature range	−55 °C to +125 °C
Junction temperature	+125 °C
Package dissipation (25 °C)	500mW

* Voltage between pins 6-7, 8-1

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):–
$V^+ = +12V$ DC, $V^- = -8V$ DC, $I_5 = 1.0$ mA DC, $R_L = 3.9$ kΩ, $R_e = 1.0$ kΩ $T_A = +25°C$
All input and output characteristics single-ended, unless otherwise stated.

Characteristic*	SL1596 Min	SL1596 Typ	SL1596 Max	SL1496 Min	SL1496 Typ	SL1496 Max	Units
Carrier Feedthrough							μV(rms)
V_C = 60 mV(rms) sinewave and f_C = 1.0 kHz	–	40	–	–	40	–	
offset adjusted to zero f_C = 10 MHz	–	140	–	–	140	–	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero f_C = 1.0 kHz	–	0.04	0.2	–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz	–	20	100	–	20	200	
Carrier Suppression							dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave	50	65	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sinewave	–	50	–	–	50	–	
Signal Gain	2.5	3.5	–	2.5	3.5	–	V/V
V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5 V DC							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz							
Parallel Input Resistance	–	200	–	–	200	–	kΩ
Parallel Input Capacitance		2.0		–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz							
Parallel Output Resistance		40		–	40	–	kΩ
Parallel Output Capacitance		5.0		–	5.0	–	pF
Input Bias Current							
$\frac{I_1 + I_4}{2}$; $\frac{I_7 + I_8}{2}$		12	25	–	12	30	μA
Input Offset Current							
$(I_1 - I_4)$, $(I_7 - I_8)$		0.7	5.0	–	0.7	7.0	μA
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current ($I_6 - I_9$)	–	14	50	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 V DC	–	-85	–	–	−85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	–	8.0	–	–	8.0	–	V DC
Differential Output Voltage Swing Capability	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current							mA DC
$I_6 + I_9$	–	2.0	3.0	–	2.0	4.0	
I_{10}	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	–	33	–	–	33	–	mW

*Pin numbers are given for TO-5 package.

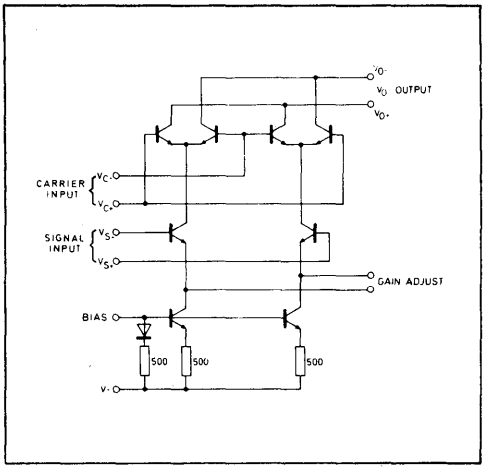


Fig. 2 ***Circuit diagram***

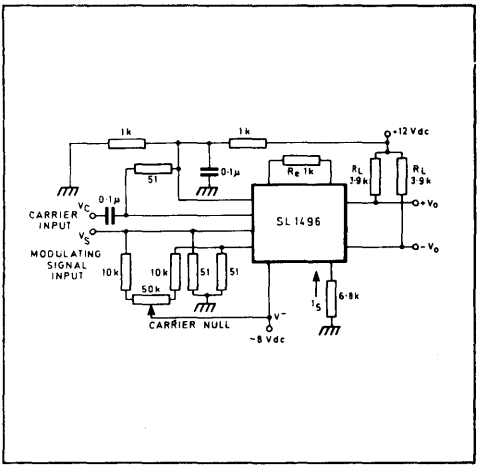


Fig. 3 ***Typical modulator circuit***

SL1521 Limiting R.F. Amplifier
SL1522 Dual Limiting R.F. Amplifiers (Parallel)
SL1523 Dual Limiting R.F. Amplifiers (Series)

DESCRIPTION

The **SL1521** A, B and C are wideband amplifiers intended for use in successive detection logarithmic I.F. strips operating at center frequencies up to 200MHz. The typical midband voltage gain of the SL1521 is 12 dB, and the A, B and C versions differ mainly in the tolerance of voltage gain.

The **SL1522** is a wideband amplifier intended for use as the first stage of a successive detection logarithmic I.F. strip, and operates at up to 200MHz. Consisting of a resistor network and two SL1521,s, the SL1522 improves the logging accuracy in the -20 to 0 dBm input range by summing additional video current from another stage.

The **SL1523** consists of two SL1521,s in series, and is intended to reduce the package count and improve the packaging density in logarithmic strips at frequencies up to 200 MHz.

ABSOLUTE MAXIMUM RATINGS (Non-Simultaneous)

The absolute maximum ratings are limiting values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature range	−55°C to +175°C
Operating temperature	−55°C to +125°C
Chip operating temperature:	
Chip-to-ambient thermal resistance	300°C/W (SL1522,SL1523) 250°C/W (SL1521)
Chip-to-case thermal resistance	95° C/W (SL1522, SL1523) 80°C/W (SL1521)
Maximum instantaneous voltage at video output	+12 V
Supply voltage	+ 9 V

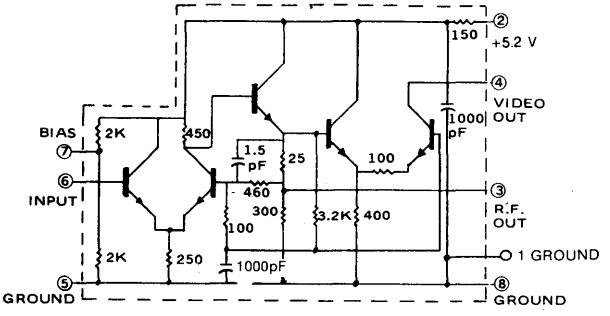


Fig 1: SL1521 circuit diagram

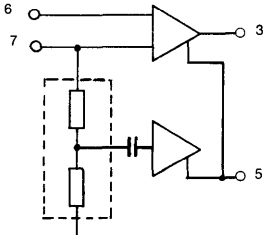


Fig 2: SL1522 block diagram

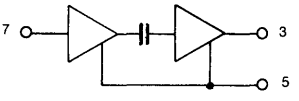


Fig 3: SL1523 block diagram

Electrical Characteristics

Test Conditions
Temperature = 22° ± 2°c
Supply voltage = +5.2V

Characteristic		SL1521 A	SL1521 B	SL1521 C	Units	Test Conditions
/oltage gain:	(Min)	11.5	11.2	10.8	dB	F=120MHz, 7mV rms
	(Max)	12.5	12.8	13.1	dB	input, 50 ohms source 8pF load + 500 ohms
Voltage gain:	(Min)	11.2	11.0	10.6	dB	F=160MHz, 7mV rms
	(Max)	12.8	13.0	13.4	dB	input, 50 ohms source 8pF load + 500 ohms
Upper cut-off frequency	(Min)	315	315	300	MHz	50 ohms source
	(Max)	350	350	350	MHz	50 phms source
Lower cut-off frequency	(Min)	6	6	6	MHz	50 ohms source
	(Max)	10	10	10	MHz	50 ohms source
Propagation delay	**(Typ)	0.6	0.6	0.6	n sec	
Maximum rectified video output current	(Min)	0.95	0.90	0.90	mA	F=120MHz, 0.5 V rms
	(Max)	1.05	1.10	1.20	mA	input, 8pF load + 500 ohms
Variation of gain with supply voltage	**(Typ)	1.0	1.0	1.0	dB/V	
Variation of maximum rectified output current with supply voltage	**(Typ)	30	30	30	%/V	
Maximum inoput signal before overload	*					
	**(Typ)	1.5	1.5	1.5	V rms	
Noise figure	**(Typ)	9.5	9.5	9.5	dB	F=120MHz, source resistance 50Ω
Supply current	(Min)	10.0	10.0	10.0	mA	
	(Typ)	15.0	15.0	15.0	mA	
	(Max)	20.0	20.0	20.0	mA	
Maximum R.F. output voltage	**(Typ)	1.0	1.0	1.0	Vp-p	F=120 MHz

NOTE: * Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction on T1 on peak.

** All typical values are given for design information, and are not 100% tested.

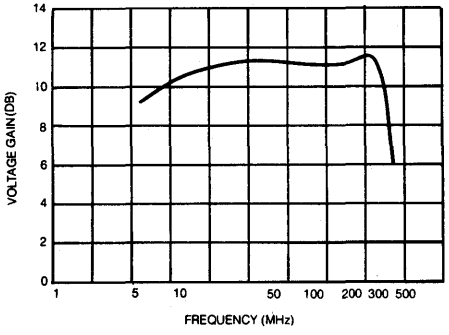


Fig 4: SL1521 Voltage gain vs. frequency.

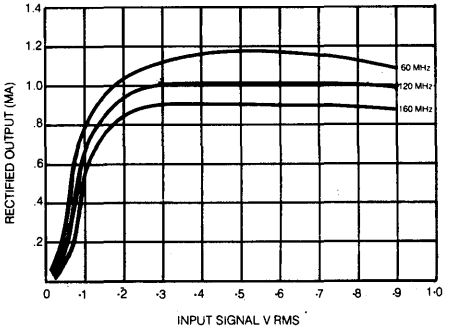


Fig 5: SL1521 rectified output current vs. input signal

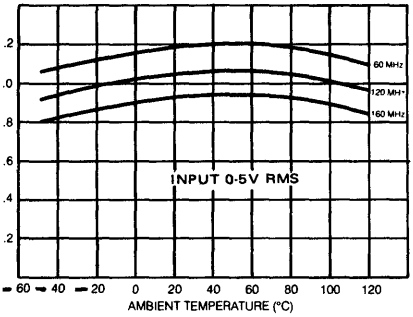
Electrical Characteristics

Test Conditions
Temperature = 22° ± 2°c
Supply voltage = +5.2V

Characteristic		SL1522 A	SL1522 B	SL1522 C	Units	Test Conditions
Voltage gain:	(Min)	11.2	10.8	10.2	dB	F=120MHz, 7mV rms
	(Max)	12.8	13.1	13.9	dB	input, 50 ohms source 8pF load + 500 ohms
Voltage gain:	(Min)	11.0	10.6	10.0	dB	F=160MHz, 7mV rms
	(Max)	13.0	13.4	14.3	dB	input, 50 ohms source 8pF load + 500 ohms
Upper cut-off frequency	(Min)	315	315	300	MHz	50 ohms source
	(Max)	350	350	350	MHz	50 ohms source
Lower cut-off frequency	(Min)	6	6	6	MHz	50 ohms source
	(Max)	10	10	10	MHz	50 ohms source
Propagation delay	**(Typ)	0.6	0.6	0.6	n sec	
Maximum rectified video output current	(Min)	1.6	1.5	1.4	mA	F=120MHz, 0.5 V rms
	(Max)	1.8	1.9	2.0	mA	input, 8pF load + 500 ohms
Variation of gain with supply voltage	**(Typ)	2.0	2.0	2.0	dB/V	
Variation of maximum rectified output current with supply voltage	**(Typ)	30	30	30	%/V	
Maximum input signal before overload	* **(Typ)	1.5	1.5	1.5	v rms	
Noise figure	**(Typ)	9.5	9.5	9.5	dB	F=120MHz, source resistance 50Ω
Supply current	(Min)	20	20	20	mA	
	(Typ)	30	30	30	mA	
	(Max)	40	40	40	mA	
Maximum R.F. output voltage	**(Typ)	1.0	1.0	1.0	Vp-p	F=120MHz

NOTE: * Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction on T1 on peak.

** All typical values are given for design information, and are not 100% tested.



6: SL1521 maximum rectified output current vs. temperature

ERATING NOTES

The amplifiers are intended for use directly ıpled, as shown in Fig. 8 (This figure shows the -5 version).

The seventh stage in an untuned cascade will giving virtually full output on noise.

Noise may be reduced by inserting a single ed circuit between in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonsnce. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in hihg frequency tuned cascades.

	Number of Stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits.

Electrical Characteristics

Test Conditions
Temperature = 22° ± 2°c
Supply voltage = +5.2V

Characteristic		SL1523 A	SL1523 B	SL1523 C	Units	Test Conditions
Voltage gain:	(Min)	23	22	21	dB	F=120MHz, 7mV rms
	(Max)	25	26	27	dB	input, 50 ohms source 8pF load + 500 ohms
Voltage gain:	(Min)	22	21	20	dB	F=160MHz, 7mV rms
	(Max)	25	26	27	dB	input, 50 ohms source 8pF load + 500 ohms
Upper cut-off frequency	(Min)	230	230	230	MHz	50 ohms source
	(Max)	280	280	280	MHz	50 ohms source
Lower cut-off frequency	(Min)	6	6	6	MHz	50 ohms source
	(Max)	10	10	10	MHz	50 ohms source
Propagation delay	**(Typ)	0.6	0.6	0.6	n sec	
Maximum rectified video output current	(Min)	1.9	1.8	1.7	mA	F=120MHz, 0.5 V rms
	(Max)	2.1	2.2	2.3	mA	input, 8pF load + 500 ohms
Variation of gain with supply voltage	**(Typ)	2.0	2.0	2.0	dB/V	
Variation of maximum rectified output current with supply voltage	**(Typ)	30	30	30	%/V	
Maximum input signal before overload	* **(Typ)	1.5	1.5	1.5	V rms	
Noise figure	**(Typ)	9.5	9.5	9.5	dB	F=120MHz, source resistance 50Ω
Supply current	(Min)	20	20	20	mA	
	(Typ)	30	30	30	mA	
	(Max)	40	40	40	mA	
Maximum R.F. output voltage	**(Typ)	1.0	1.0	1.0	Vp-p	F=120MHz

NOTE: * Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction on T1 on peak.
** All typical values are given for design information, and are not 100% tested.

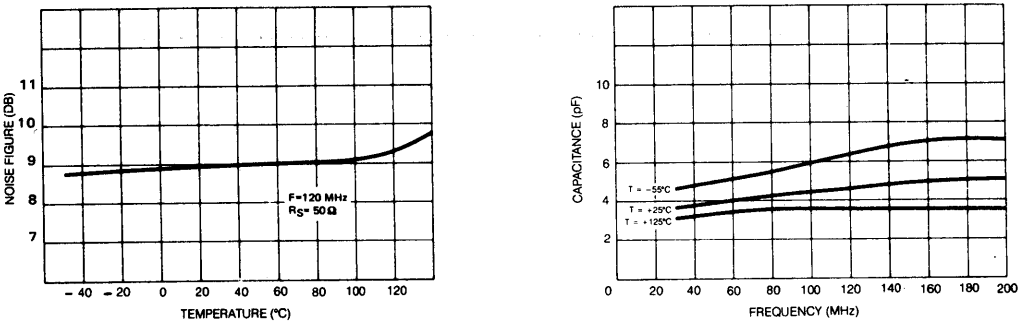


Fig 7: SL1521 input admittance with open-circuit output.

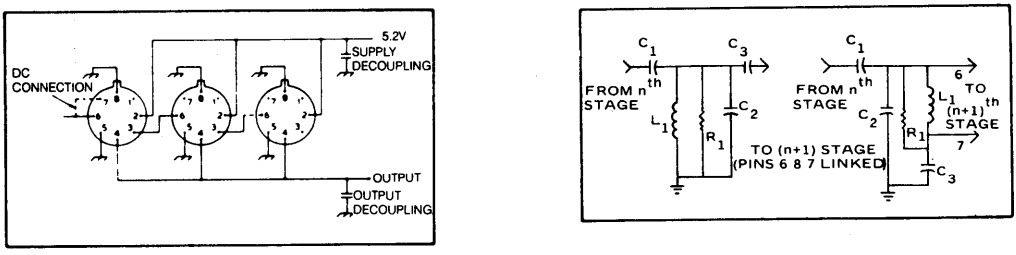


Fig. 9: Interstage filter designs (including damping resistors)

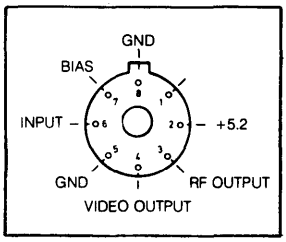


Fig 10: SL1521, bottom view
CM8 with standoff

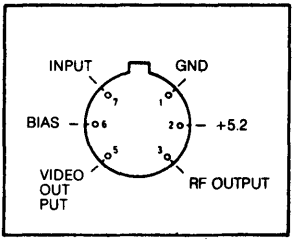


Fig 11: SL1522, bottom view

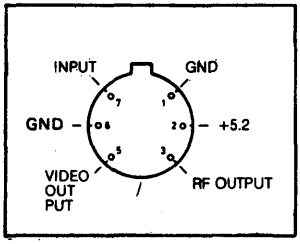


Fig 12: SL1523, bottom view

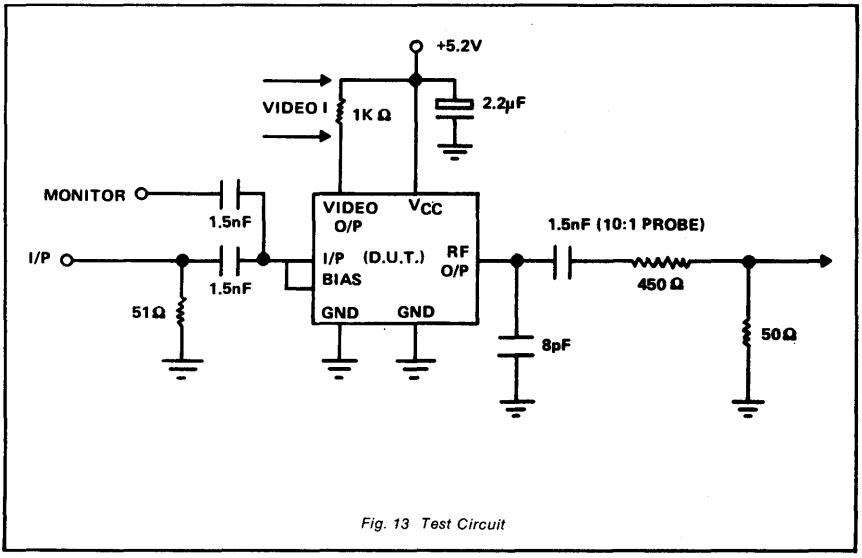


Fig. 13 Test Circuit

SL1524 Quad Limiting R.F. Amplifier (Series)
SL1525 Quad Limiting R.F. Amplifier (Parallel)

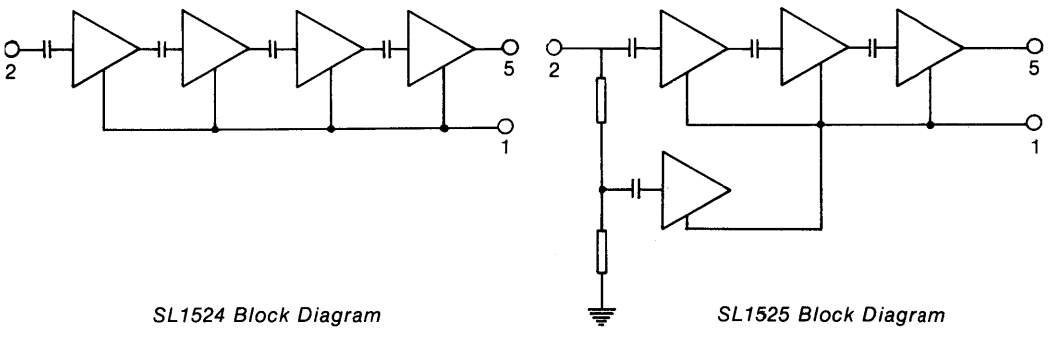
SCRIPTION

The SL1524 consists of four SL1521 s series, d is intended for use in succesive detection arithmic I.F. strips operating at center quency up to 120MHz and also intended to uce the package count and improve the cking density. The typical midband voltage n of the SL1524 is 48dB

The SL1525 is a wideband amplifier intended use as the first stage of a succesive detection arithmic I.F. strip, and operate at center quency up to 120MHz. Consisting of a resistor work and four SL1521 s, the SL1525 improves logging accurracy in the -10 to 5 dBm input ge by summing additional video current from allel stage. The typical midband voltage gain the SL1525 is 36dB

ABSOLUTE MAXIMUM RATINGS

- Storage temperature range -55° C to 175° C
- Operating temperature range -55 ° C to 125 ° C
- Maximum instantaneous voltage at video output +12V
- Supply voltage +9V



SL1524 Block Diagram

SL1525 Block Diagram

Fig. 1.

ELECTRICAL CHARACTERISTICS

Test Conditions

Temperature = 22 ^{o} ± 2 ^{o} C

Supply voltage = 5.2V

Characteristics			SL1524 A	SL1524 B	SL1524 C	Units	Test Conditions
Voltage gain:		(Min)	46	43	41	dB	F = 60MHz, 2.22m V rms
		(Max)	50	52	54	dB	input, 50 ohms source 500 ohms load
Upper cut-off frequency		(Min)	95	90	90	MHz	50 ohms source
		(Max)	120	120	120	MHz	50 ohms source
Lower cut-off frequency		(Min)	9	9	9	MHz	50 ohms source
		(Max)	15	15	15	MHz	50 ohms source
Propagation delay	**	(Typ)	2.4	2.4	2.4	nsec	
Maximum rectified video output current		(Min)	3.90	3.80	3.70	mA	F = 60MHz, 0.5 V rms
		(Max)	4.30	4.40	4.50	mA	input 500 ohms load
Variation of gain with supply voltage	**	(Typ)	3.0	3.0	3.0	dB/V	
Variation of maximum rectified output current with supply voltage	**	(Typ)	30	30	30	%/V	
Maximum input signal before overload	* **	(Typ)	1.5	1.5	1.5	V rms	
Noise figure	**	(Typ)	9.5	9.5	9.5	dB	F = 60MHz, source resistance 50Ω
Supply current		(Min)	45	45	45	mA	
		(Typ)	55	55	55	mA	
		(Max)	70	70	70	mA	
Maximum R.F. output voltage	**	(Typ)	1.0	1.0	1.0	Vp-p	F = 60MHz

Note: * Overload occurs when the input signal reaches a level sufficient to forward bias collector junction on T1 on peak.

** All typical values are given for design information, and are not 100% tested.

LECTRICAL CHARACTERISTICS

Test Conditions

Temperature = 22 °±2 °C
Supply Voltage = +5.2V

Characteristics			SL1525 A	SL1525 B	SL1525 C	Units	Test Conditions
Voltage gain		(Min)	35	32	30	dB	F = 60MHz,
		(Max)	38	40	43	dB	input, 50 ohms source 500 ohms source
Upper cut-off frequency		(Min)	135	130	130	MHz	50 ohms source
		(Max)	150	150	150	MHz	50 ohms source
Lower cut-off frequency		(Min)	9	9	9	MHz	50 ohms source
		(Max)	15	15	15	MHz	50 ohms source
Propagation delay	**	(Typ)	1.8	1.8	1.8	nsec	
Maximum rectified video output current		(Min)	3.40	3.30	3.20	mA	F = 60MHz, 0.5 V rms
		(Max)	3.80	3.90	4.00	mA	input, 500 ohms load
Variation of gain with supply voltage	**	(Typ)	2.5	2.5	2.5	dB/V	
Variation of maximum rectified output current with supply voltage	**	(Typ)	30	30	30	%/V	
Maximum input signal before overload	*						
	**	(Typ)	1.5	1.5	1.5	V rms	
Noise figure	**	(Typ)	9.5	9.5	9.5	dB	F = 60MHz, source resistance 50Ω
Supply current		(Min)	45	45	45	mA	
		(Typ)	55	55	55	mA	
		(Max)	70	70	70	mA	
Maximum R.F. output voltage	**	(Typ)	1.0	1.0	1.0	V p-p	F = 60 MHz

OTE: * Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction on T1 on peak.

** All typical values are given for design information, and are not 100% tested.

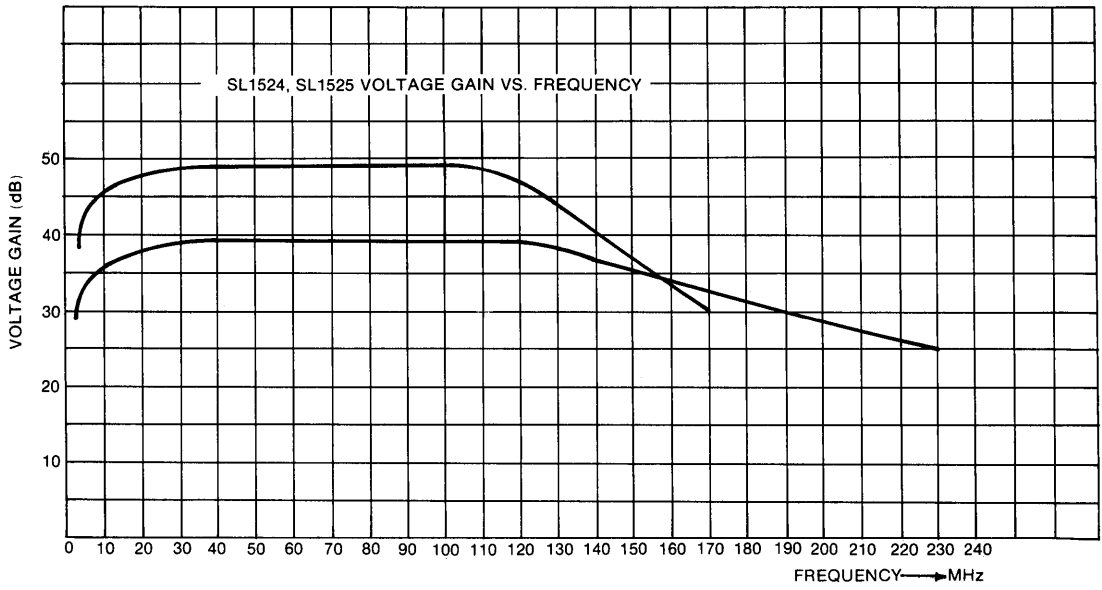


Fig. 2. Voltage Gain VS Frequency

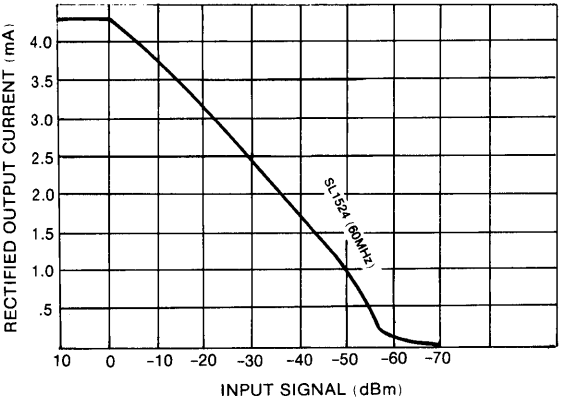


Fig. 3. SL1524 Rectified Output Current VS Input Signal

OPERATING NOTES

A double sided PCB is recommended for use with a minimum amount of copper removed from the component side; it is advisable to solder all earth connections to both sides of the board, and keep all connections as short as possible. Also a high quality attenuator is needed for measuring with an accurate log law.

APPLICATION NOTES

The SL1524 and SL1525 can be put together with a bandpass filter in between to extend the dynamic range of a log strip. The technique for increasing the dynamic range is done by the attenuator at the input inside the SL1525. Normally the log response limits when the input signal exceeds that necessary to produce fully video output from the first stage, however the parallel stage is being fed with an attenuated signal so will continue to give a video output change. Note that the bandwidth of the filter is a compromise between sensitivity and response time. If the bandwidth is too wide the dynamic range will be reduced due to the noise produced by the first stage of SL1525 any errors in the filter will produce a kink in the log characteristic at input level between -40 and -60 dBm.

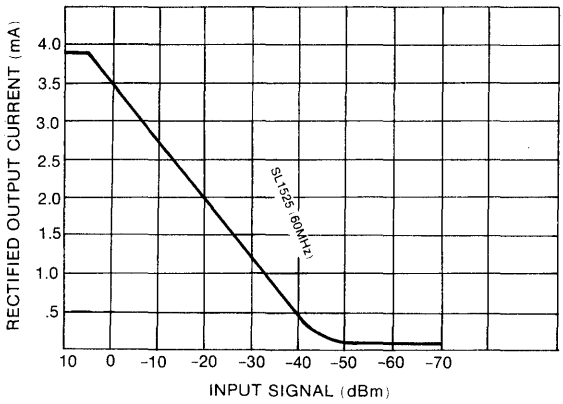


Fig. 4. SL1525 Rectified Output Current VS Input Signal

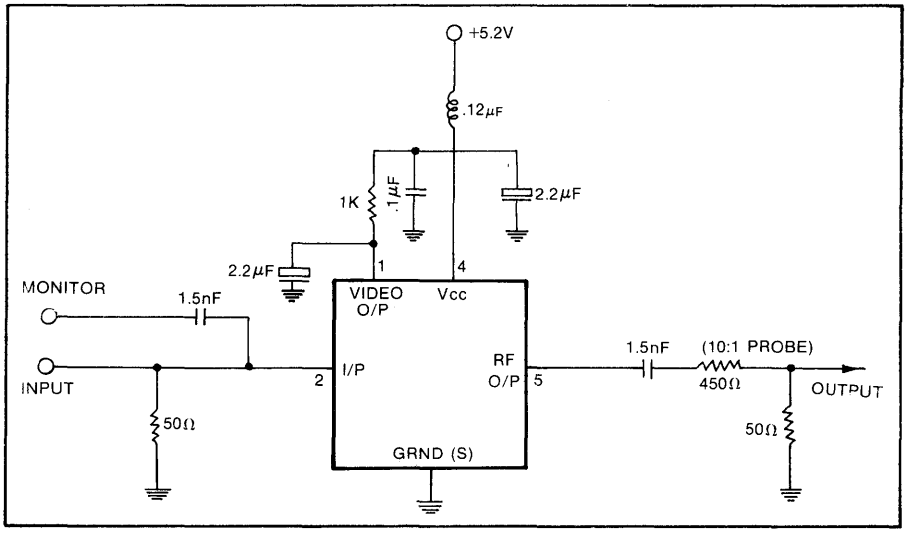


Fig. 5. Test Circuit

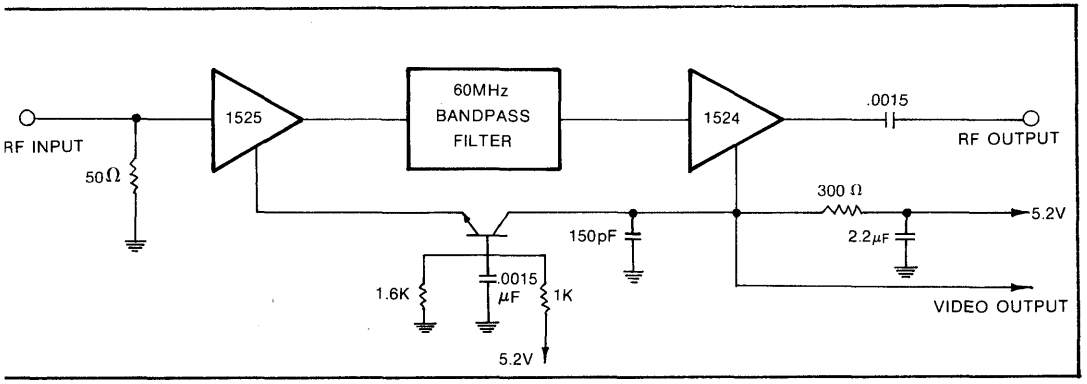


Fig. 6. Application Circuit.

SL1531

FIVE STAGE - LOG IF STRIP

The SL1531 ia a hybrid integrated circuit, it ers the bandwidth of over 160MHz and low phase ift with amplitude. The signal gain is 42 dB and e limited output is 1 volt peak to peak. The phase ift it ±5 ^{O} (Typ) when overdriven by 0dB. The cuit has the internal coupling capacitors at the outs of each stage and the minimum number of ternal components. The circuit can be changed the designer for the use of low frequency.

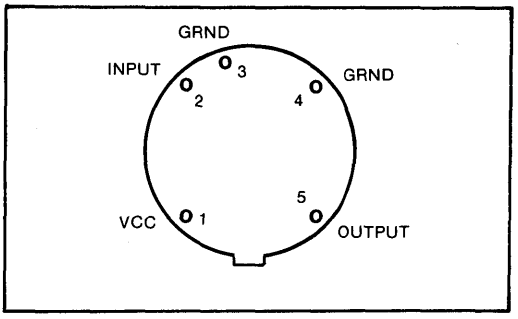


Fig. 1 Pin Connections (Bottom View)

PLICATION

MTI Radar System

I.F.'s for Raycon

Sonar Signal Amplification

Ultrasonic Medical Scanners

Crystal Video

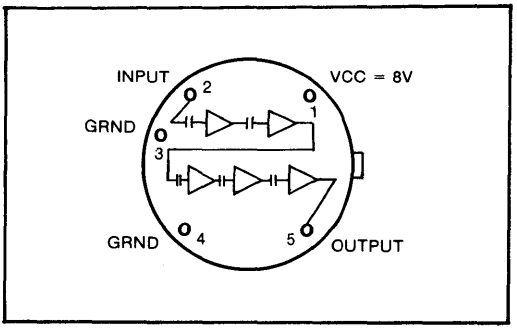


Fig. 2 SL1531 Block Diagram (Top View)

ECTRICAL CHARATERISTICS

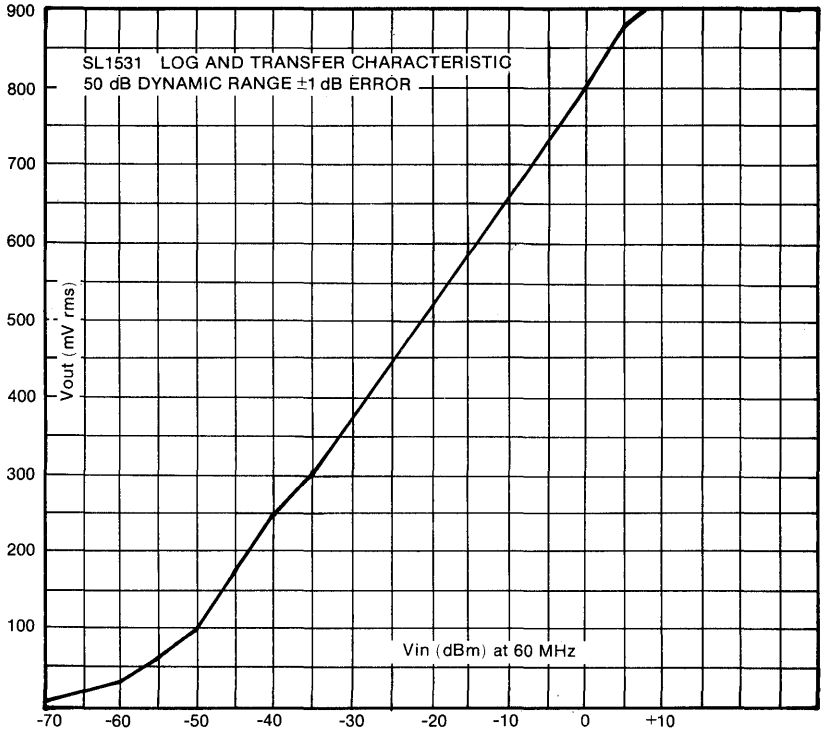
st Conditions (unless otherwise stated)

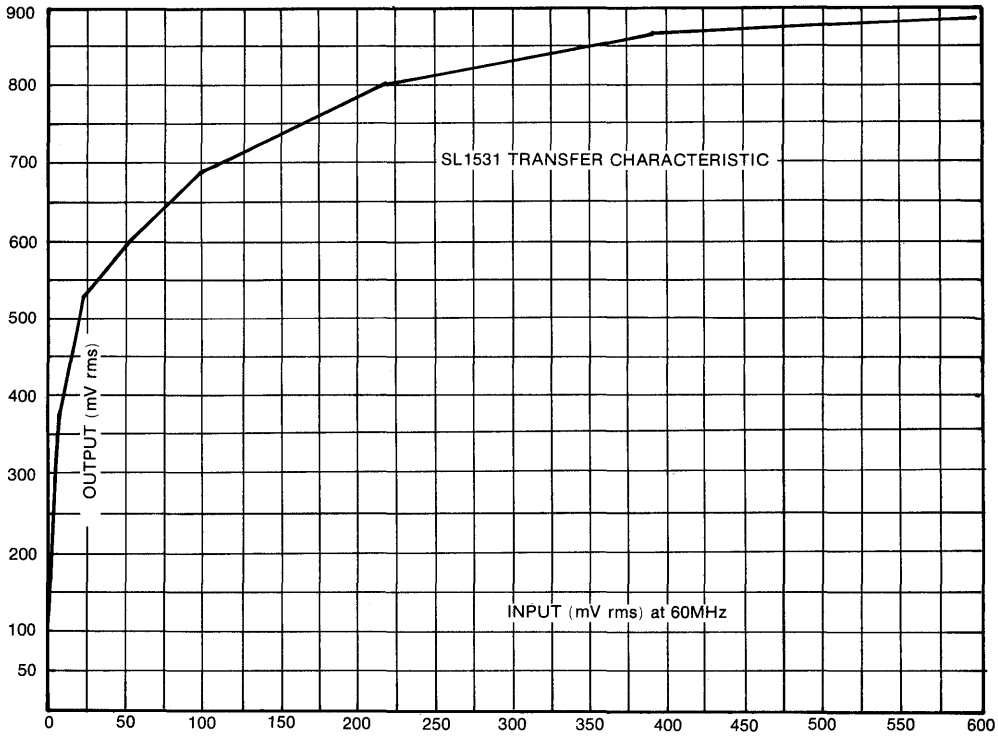
mperature (Ambient) 25^{O} C

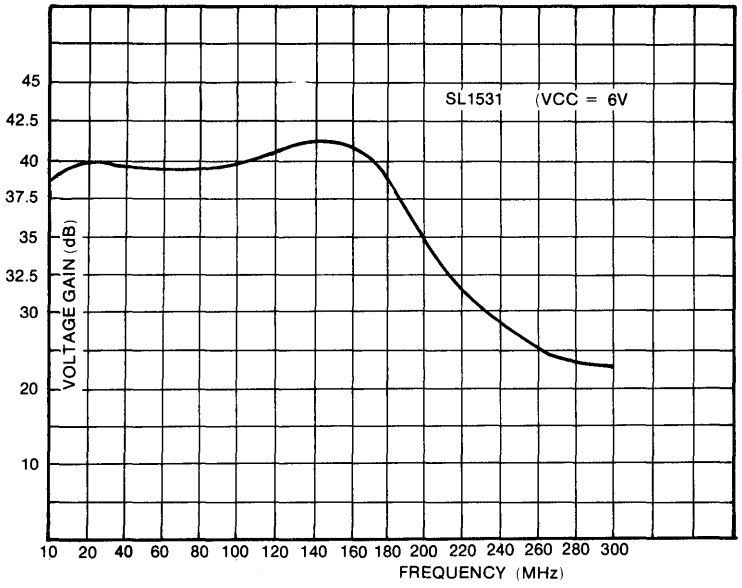
equency 60MHz

C = 6.0V

haracteristics	Value			Units	Conditions
	Min	Typ	Max		
oltage gain	40	42	46	dB	2.22mV I/P, 50Ω source
imited O.P. voltage		1		V pk-pk	
pper cut-off frequency		165		MHz	
ower cut-off frequency		10		MHz	
hase variation with signal level		±5		degree	Vin = -60dBm→0dBm @ 60MHz
nput imedance		2.5pF // 1KΩ			
utput impedance		15Ω + 25 nh			


SL1531 LOG AND TRANSFER CHARACTERISTIC
50 dB DYNAMIC RANGE ±1 dB ERROR
Vout (mV rms)
900
800
700
600
500
400
300
200
100
Vin (dBm) at 60 MHz
-70
-60
-50
-40
-30
-20
-10
0
+10


SL1531 TRANSFER CHARACTERISTIC
OUTPUT (mV rms)
900
800
700
600
500
400
300
200
100
50
INPUT (mV rms) at 60MHz
0
50
100
150
200
250
300
350
400
450
500
550
600



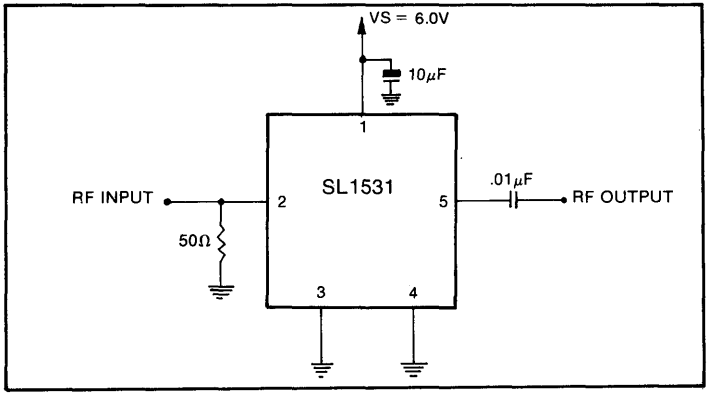
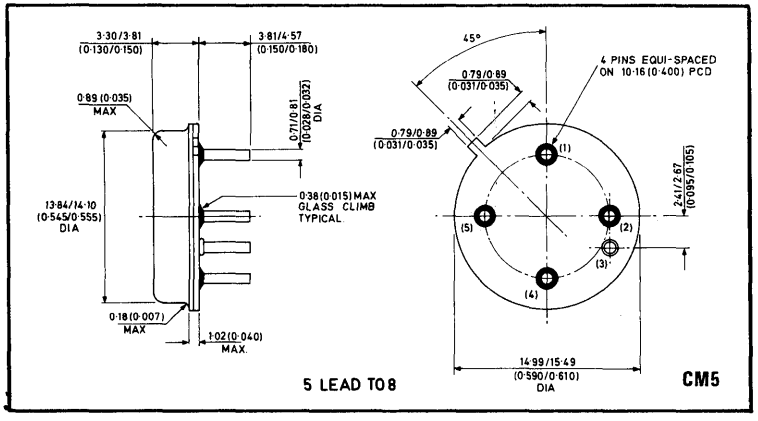


Fig. 3. Test Circuit



SL1532

FIVE STAGE - LIMITING IF STRIP

The SL1532 is a hybrid integrated circuit, it offers the bandwidth of over 120MHz and very low phase shift with amplitude. The signal gain is 56 dB and the limit output is 1 volt peak to peak. The use of a 5GHz IC process has produced a circuit which gives less than ±4 ^{o} phase shift when overdriven by 10dB. It has the internal coupling capacitors at the inputs of each stage and the minimum number of external components. The circuit can be changed by the designer for the use of low frequency.

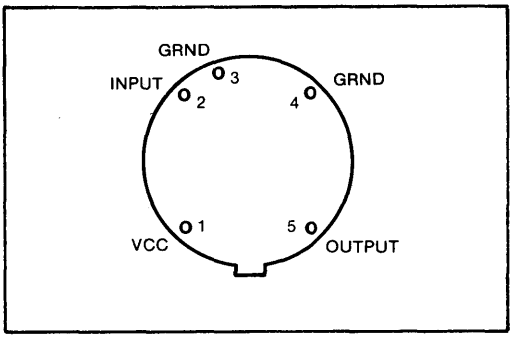


Fig. 1 Pin Connections (Bottom View)

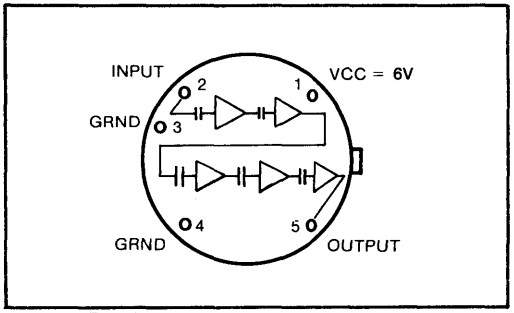


Fig. 2 Block Diagram (Top View)

APPLICATION

Microwave (or Radio) relays

TV Satelleite ground stations

Frequency discriminotors, Saw compressor/ Expanders and IF for spread spectrum radar

ELECTRICAL CHARACTERISTICS

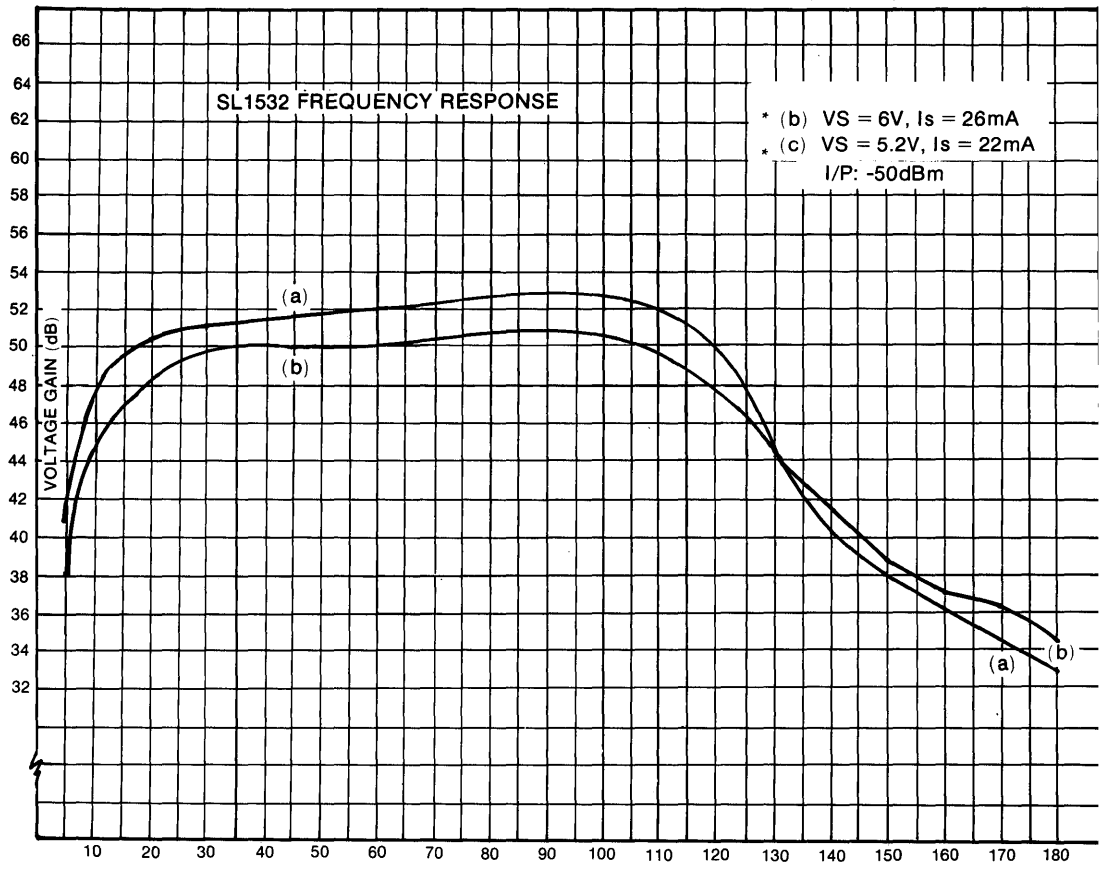
Test Conditions (unless otherwise stated)

Temperature (Ambient) 25 ^{o} C

Frequency 60MHz

VCC = 6V

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Voltage gain	50	54	58	dB	0.702mV rms I/P, 50Ω source
Limited O.P. voltage		1		V pk-pk	
Upper cut-off frequency		150		MHz	
Lower cut-off frequency		100		KHz	
Phase variation with signal level		±4		degree	Vin = -60dBm→+10dBm 60MHz
Output level variation over input range		0.8		dB	
Gain variation with temperature		5		dB	-55^{o} C to 125^{o} C
Input impedance		1.3		KΩ	
Output impedance		10		Ω	



* See note in Figure 3.

Table of performance of SL1532 at three different supply voltages.

Vs	Is	Gain *	Phase ** variation:
6.0V	26mA	52dB	$\pm 4^{o}$ (typ)
5.2V	22mA	50dB	$\pm 4^{o}$ (typ)

* : Gain reading @ 70MHz
** : -50dBm ⟶ 10dBm input @ 70MHz

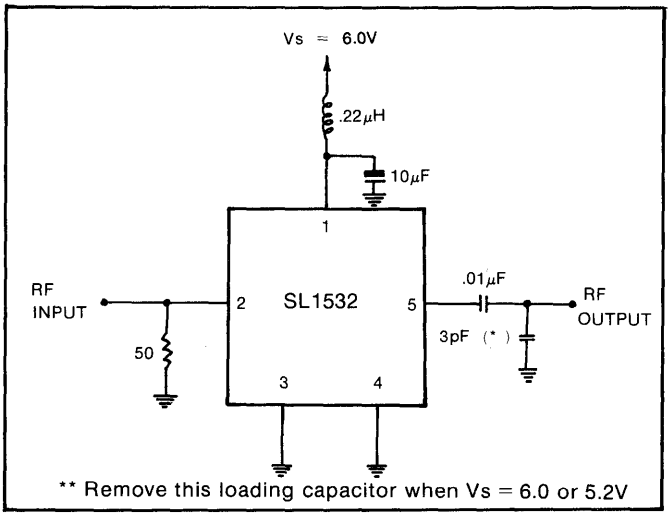


Fig. 3. Test Circuit

Plessey Semiconductors

SL1550

WIDEBAND AMPLIFIER

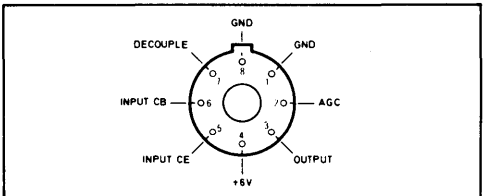
SL1550

LOW NOISE WIDEBAND AMPLIFIER WITH EXTERNAL GAIN CONTROL

The SL1550 circuit is designed for use as a general purpose wideband linear amplifier with remote gain control. At an operating frequency of 60MHz the noise figure is typically 1.8dB from a 200Ω source – giving good noise performance directly from a microwave mixer. The SL1550 has an external gain control facility which can be used to obtain a swept gain function and makes the amplifier ideal for use either in a linear IF strip or as a low noise preamplifier in a logarithmic strip.

External gain control is performed in the feedback loop of the main amplifier which is buffered on the input and output, hence the noise figure and output voltage swing are only slightly degraded as the gain is reduced. The external gain control characteristic is specified with an accuracy of ±1dB, enabling a well-defined gain versus time law to be obtained.

The input transistor can be connected in common emitter or common base.



CM8 (8 – lead TO – 5 5.84mm PCD with stand –off)

Fig. 1 Pin connections

FEATURES

Wide Bandwidth	320 MHz
Low Noise	2.0 dB at 100 MHz
Gain Control Range	25 dB
Gain	38 dB
Output Voltage	0.5 V r.m.s.

APPLICATIONS

- Low Noise Preamplifiers
- Swept Gain Radar IFs

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Ambient operating temp.	−55°C to +125°C
Max. continuous supply Voltage wrt pin 1	+9V

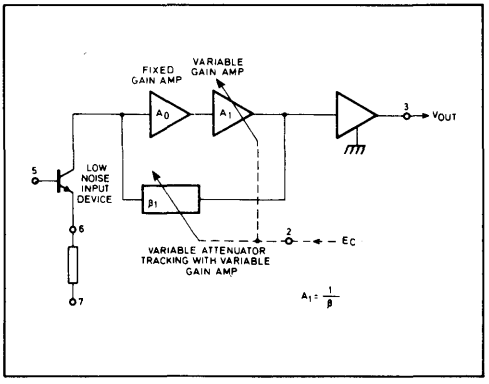


Fig. 2 Functional diagram

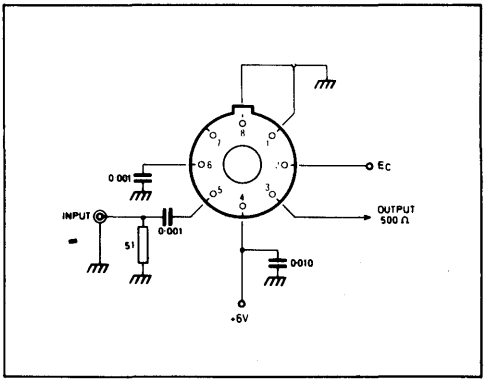


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Frequency = 60MHz $E_C = 0$
$V_S = 6$ volts
$R_L = 500\Omega$

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	36	40	44	dB	
Gain control characteristic (note 1)		See Fig. 5			
Gain reduction at mid-point		10		dB	$E_C = 1.3V$
Max. gain reduction	20	25		dB	$E_C = 5V$
Noise figure		2.0	2.7	dB	$R_S = 200\Omega$
		3.5		dB	$R_S = 50\Omega$
Output voltage		0.3		Vrms	
Supply current	12	15	18	mA	
Gain variation with supply voltage		0.2		dB/V	$V_S = 6$ to 9V.
Upper cut-off frequency (—3dB wrt 60 MHz)		125		MHz	
Gain variation with temperature (note 2)		±3		dB	T_{amb} —55°C to +125°C

NOTES
1. The external gain control characteristic is specified in terms of the gain reduction obtained when the control voltage (E_C) is increased from zero to the specified voltage.
2. This can be reduced by an alternative, input configuration (see operating note: 'Wide Temperature Range').

OPERATING NOTES

Input impedance

Typical input impedance at 60 MHz is 500Ω in parallel with 12 pF. The capacitance is independent of frequency but the resistance increases to approximately 1.5kΩ at 10 MHz.

Control input

Gain control is achieved by applying a positive voltage to pin 2.

Wide temperature range

The gain variation with temperature can be reduced at the expense of noise figure by including an internal 30Ω resistor in the emitter of the input transistor. This is achieved by decoupling pin 7 and leaving pin 6 open-circuit. Gain variation is reduced from ±3dB to ±1dB over the temperature range —55°C to +125°C (Figs. 6 and 7)

Low input impedance

A low input impedance (≃ 25Ω) can be obtained by connecting the input transistor in common base. This is achieved by decoupling pin 5 and applying the input to pin 6 (pin 7 open-circuit).

High frequency stability

Care must be taken to keep all leads short and a ground plane should be used to prevent any earth inductance common between the input and output circuits.

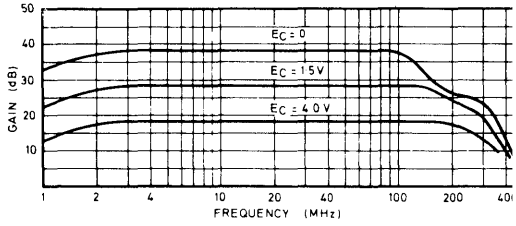


Fig. 4 Frequency response

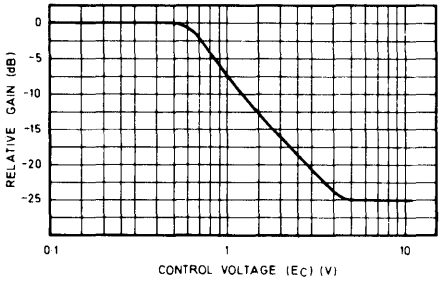


Fig. 5 Gain control characteristic

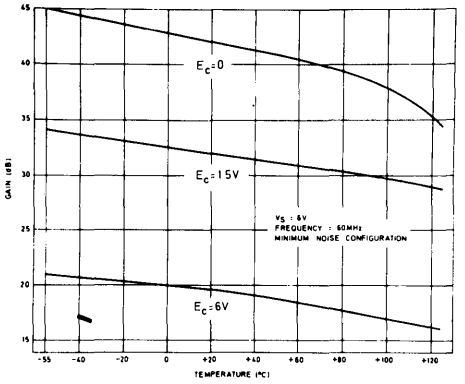


Fig. 6 Voltage gain v. temperature (pin 6 decoupled, standard circuit configuration).

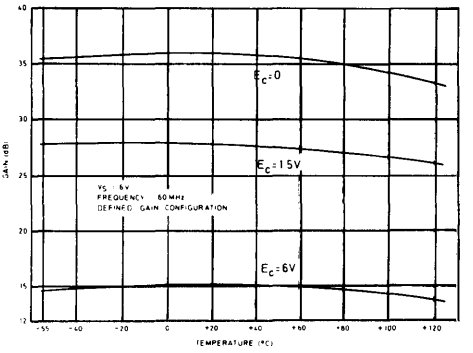


Fig. 7 Voltage gain v. temperature (pin 7 decoupled for improved gain variation with temperaturpe–see operating notes).

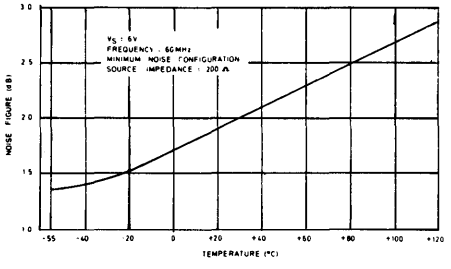


Fig.8 Typical noise figure v. temperature.

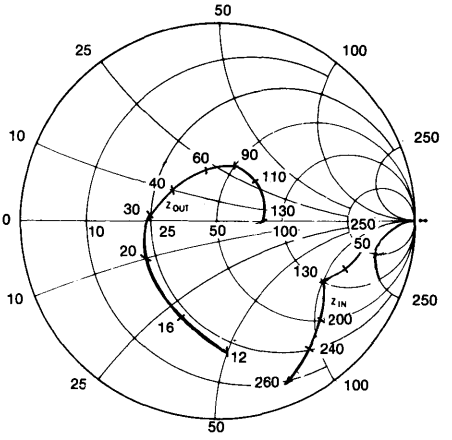


Fig. 9 Input and output impedances (V_S = 6V)

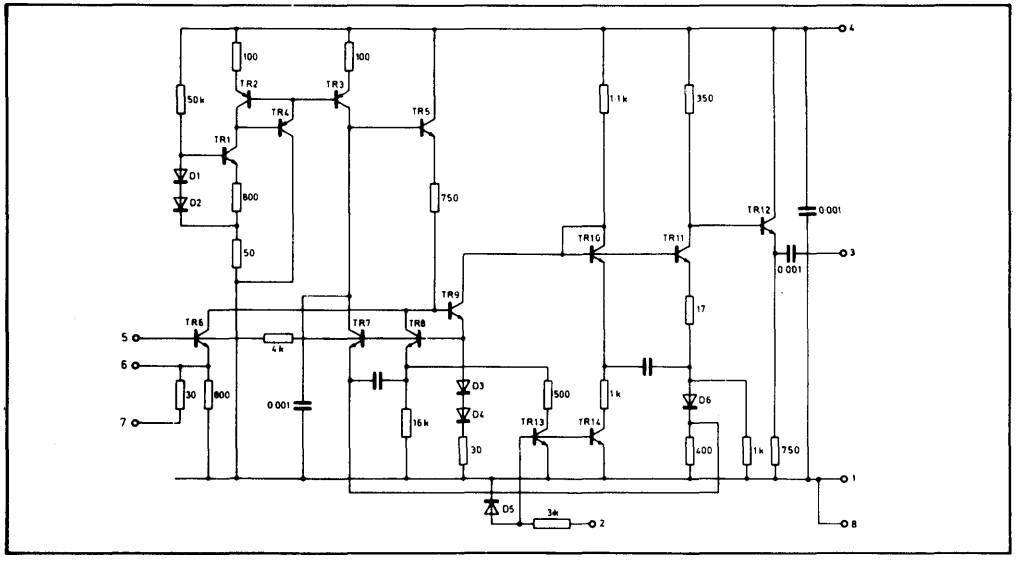


Fig. 10 Circuit diagram

SL1610C, SL1611C & SL1612C

RF/IF AMPLIFIERS

The SL1610C and SL1611C are low noise, low distortion, RF voltage amplifiers with integal supply line decoupling and AGC facilities. The SL1610C has a voltage gain of 10 and a bandwidth of 140MHz, while the SL1611C circuits have a 50dB AGC range with maximum signal handling of 250mV rms. As they are voltage amplifiers they have high input impedance and low output impedance.

The SL1612C is a low noise, low distortion, IF voltage amplifier similar to the SL1610C and SL1611C but having a voltage gain of 50, a bandwidth of 15MHz and only 20mW power consumption. It has a 70dB AGC range with maximum signal handling of 250mV rms.

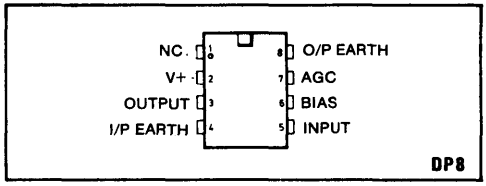


Fig. 1 Pin connections (top view)

APPLICATIONS

- IF Amplifiers
- RF Amplifiers
- AGC-Controlled Amplifiers

FEATURES

- Low Noise
- Low Distortion
- 1V rms Output
- Wide AGC Range
- On-Chip Decoupling

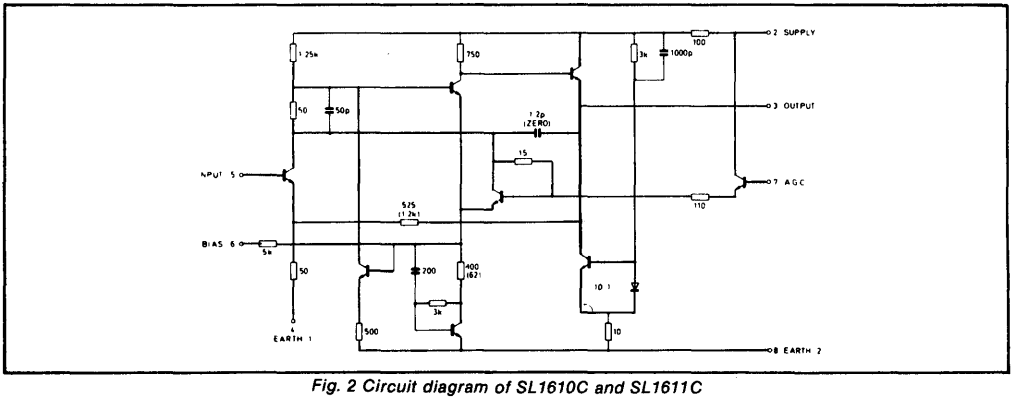


Fig. 2 Circuit diagram of SL1610C and SL1611C
(Component values of SL1611C are shown in brackets)

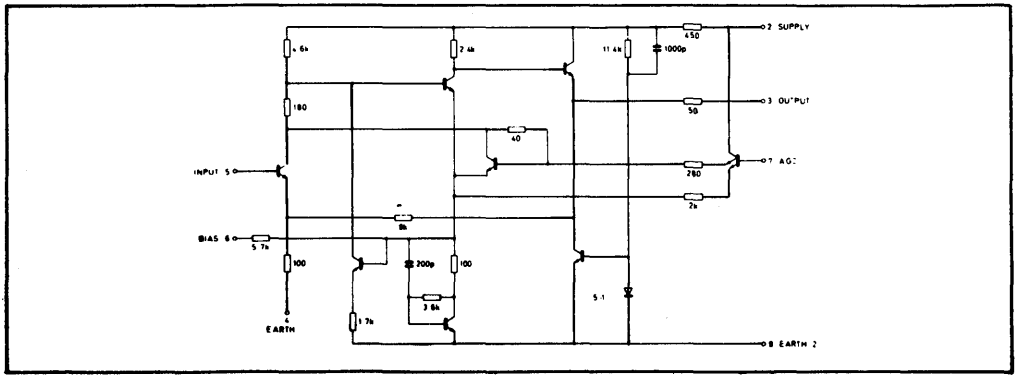


Fig. 3 Circuit diagram of SL1612C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage = 6V
Temperature = +25°C (unless otherwise stated)
Pins 5 and 6 strapped together
AGC not applied unless specified.

Characteristic	Circuit	Typical Value	Units	Test conditions
Voltage gain (see note1)	SL1610C	20	dB	30MHz, Source = 25Ω
	SL1611C	26	dB	30MHz, Load R ⩾ 500Ω
	SL1612C	34	dB	1.75MHz, Load C ⩽ 5pF
Cut-off frequency (−3dB) (See Fig. 9 and note1)	SL1610C	120	MHz	Source = 25Ω
	SL1611C	80	MHz	Load R ⩾ 500Ω
	SL1612C	12	MHz	Load C ⩽ 5pF
Noise Figure	SL1610C	4	dB	Source = 300Ω, f = 30MHz
	SL1611C	4	dB	Source = 300Ω, f = 30MHz
	SL1612C	3	dB	Source = 800Ω, f = 1.75MHz
Max. input signal (1% cross modulation) No AGC applied	SL1610C	100	mVrms	Load 150Ω, f = 10MHz
	SL1611C	50	mVrms	Load 150Ω, f = 10MHz
	SL1612C	20	mVrms	Load 1.2kΩ, f = 1.75MHz
Max. input signal (1% cross modulation) Full AGC applied	SL1610C	250	mVrms	f = 10MHz
	SL1611C	250	mVrms	f = 10MHz
	SL1612C	250	mVrms	f = 1.75MHz
AGC range (See Fig. 10)	SL1610C	50	dB	
	SL1611C	50	dB	
	SL1612C	70	dB	
AGC current	SL1610C	0.15	mA	AGC Voltage = 5.1V
	SL1611C	0.15	mA	
	SL1612C	0.15	mA	
Quiescent current consumption	SL1610C	15	mA	Output open circuit
	SL1611C	15	mA	
	SL1612C	3.3	mA	

NOTE
1. Gain and frequency response of these circuits are relatively independent of supply voltage within the range 6 to 9V

OPERATING NOTES

The SL1610C, SL1611C and SL1612C are normally used with pins 5 and 6 strapped. A slight improvement in noise figure, and an increase in the input impedance, may be obtained by feeding the device from a coil or tuned circuit, bias from pin 6 being decoupled and applied to one end of the coil and the signal being taken either from the other end or from a tap.

The characteristics of these units have been expressed in G parameters which are defined as shown in Fig. 4.

These parameters correspond to the normal operation of a voltage amplifier which is usually operating into a load much higher than its output impedance and from a source much lower than its input impedance. Hence the input admittance (G_{11}) and voltage gain (G_{21}) are measured with open circuit output, and the output impedance (G_{22}) with short circuit input. The parasitic feedback parameter is the current transfer (G_{12}) i.e. the current which flows in a short circuit across the input for a given current flowing in the output circuit.

Since the effects of G_{12} are small for reasonable values of load and source impedance, the approximate equivalent circuit given in Fig. 5 may be used.

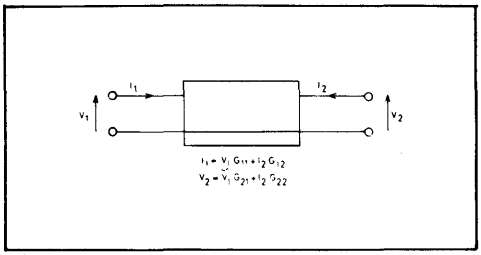


Fig. 4 Definition of G parameters

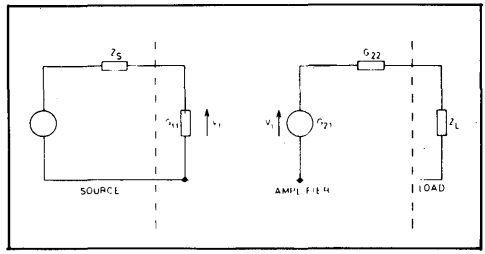


Fig. 5 Amplifier equivalent circuit

Hence the typical effects of applying finite load and source impedances, real or complex, may be evaluated by the use of the graphs showing the values of the major parameters versus frequency. At lower frequencies the limitation on Z_L is dependent upon output signal; for maximum output $Z_L = 100\Omega$.

Stability

Both the input admittance G_{11} and the output impedance G_{22} have negative real parts at certain frequencies. The equivalent circuits of input and output are shown in Fig. 6 and the values of R_{in}, R_{out}, C_{in} and L_{out} may be determined for any particular frequency from the graphs Fig. 7 and 8. It will be seen that, for the SL1610C and the SL1611C R_{in} is negative between 30 and 100MHz, and R_{out} is negative over the whole operating frequency range. For the SL1612C, R_{in} is not negative and R_{out} is negative only below 700KHz.

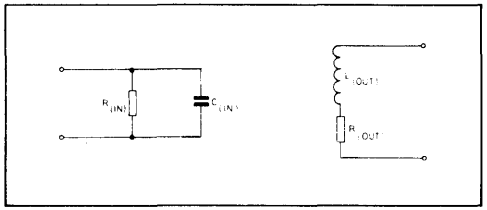


Fig. 6 Input and output equivalent circuits

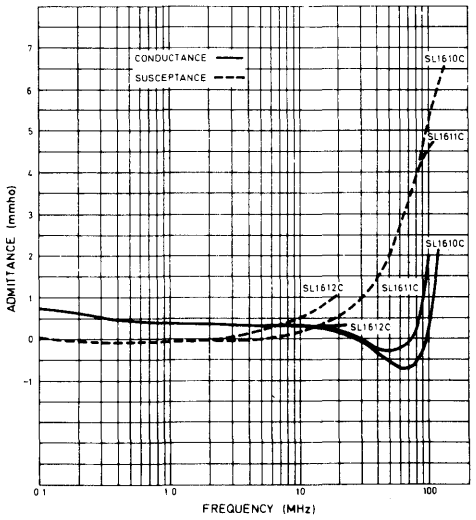


Fig. 7 Input admittance with O/C output (G_{11})

It is evident that if an inductive element having inductance L1 and parallel resistance R1 is connected across the input, oscillation will occur if R_{in} is negative at the resonant frequency of C_{in} and L1, and R1 is higher than R_{in}.

Similarly, if a capacitor C1 in series with a resistance R2 is connected across the output oscillation will occur if, at the resonant frequency of L_{out} and C1, R_{out} has a negative resistance greater than the positive resistance R2. Where the input may be inductive, therefore, it may be shunted by a resistor and where the load may be capacitive 47Ω should be placed in series with the output.

These devices may be used with supplies up to +9V with increased dissipation.

The AGC characteristics shown in Fig. 8 vary somewhat with temperature: a preset potentiometer should not, therefore, be used to set the gain of either of these circuits if accurate gain is required

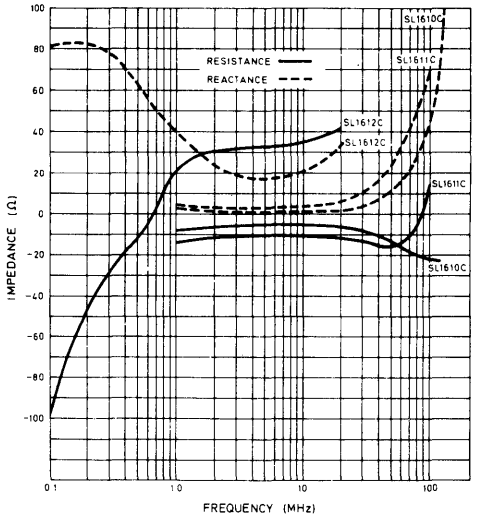


Fig. 8 Output impedance with S/C input (G_{22})

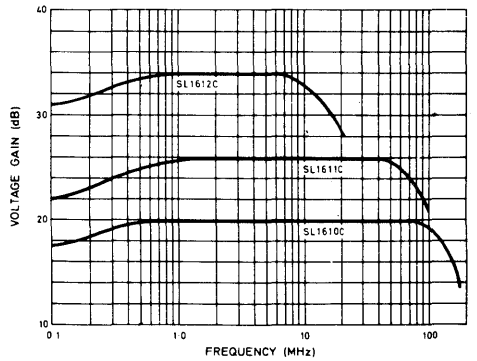


Fig. 9 Voltage gain (G_{21})

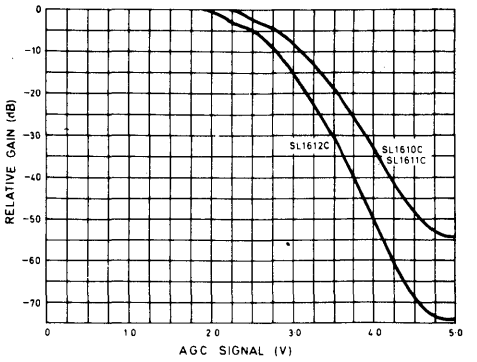


Fig. 10 AGC characteristics

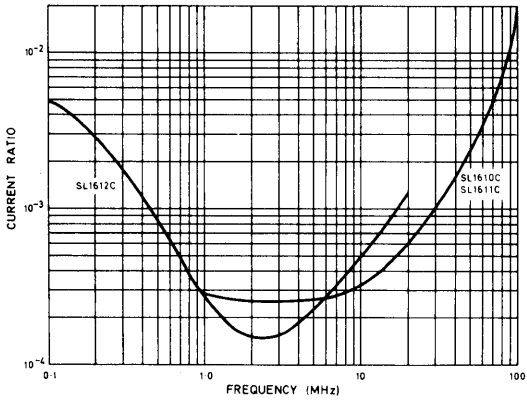


Fig. 11 Reverse current transfer ratio (G_{12})

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−30°C to + 85 °C
Supply voltage	+10V.
Operating temperature	−30°C to +70°C

Plessey Semiconductors

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1613C
LIMITING AMPLIFIER/DETECTOR

The SL1613C is a low noise limiting amplifier intended for use as an RF clipper, a limiting stage in IF amplifiers, or an RF Compressor in SSB transmitters. It contains a detector which may be used to detect AM but is particularly intended for use as an AGC detector. The amplifier, which has a gain of 12dB when not limiting, has upper and lower 3dB points of 150MHz and 5MHz respectively. It limits when its input exceeds 120mV rms. The detected output during limiting is 1mA.

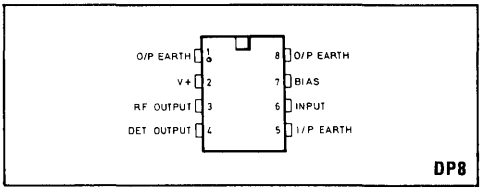


Fig. 1 Pin connections (top view)

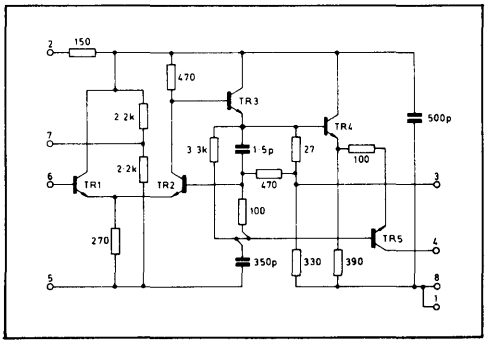


Fig. 2 Circuit diagram SL1613C

FEATURES

- Wide Bandwidth
- Low Noise
- Highly Symmetrical Limiting
- Large Signal Handling Capability

APPLICATIONS

- RF Clippers
- AGC Systems
- AM Detectors
- RF Compression in SSB Transmitters

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply +6V
Temperature +25°C
Pins 6 & 7 strapped together

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	30MHz
Upper 3dB frequency		150		MHz	
Lower 3dB frequency		5		MHz	
Noise figure		4.5		dB	60MHz 500Ω source
Supply current		15	20	mA	No signal
Limited RF o/p		1.25		V p-p	0.5V input, 30MHz
Detector current	0.8	1	1.3	mA	0.5V input, 30MHz
Maximum input before overload		1.75		V rms	30MHz
Input impedance		5kΩ// 6pF			60MHz Open circuit output

OPERATING NOTES

The SL1613C, like the SL1610/11/12, is normally used with the input and bias pins connected directly together and the input applied through a capacitor. However, and again like the SL1610/11/12, the bias may be decoupled and connected to the 'cold' end of a coil or tuned circuit, the input pin being connected to its 'hot' end or to a tap.

The supply rail is decoupled internally at RF but as the gain is dependent on supply voltage there should be no appreciable LF ripple on the supply. Two separate earth connections are made in order to minimise the effects of common earth-lead inductance – such common earth-lead inductance can cause instability and care should be taken not to introduce it externally.

The RF output is capable of driving a load of 1kΩ in parallel with 10pF. If a capacitive load of more than 10pF is envisaged a resistor should be connected between the output pin and the load. Normally 50Ω is sufficient. The output should be isolated at DC by a capacitor.

The detected output consists of a current out of pin 4, which is an NPN transistor collector. This pin must always be more than 3 volts more positive than earth, even if the detected output is not required (in which case it is best to strap pins 2 and 4).

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to +85°C
Operating temperature	−30°C to +70°C
Supply voltage (pins 2 or 4)	+9V

SL1620C & SL1621C

AGC GENERATORS

The SL1621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL1610C, SL1611C and SL1612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL1610C and one SL1612C amplifier and a suitable detector, the SL1621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

The SL1620C VOGAD (Voice Operated Gain Adjusting Device) is an AGC generator designed to work in conjunction with the SL1630C audio amplifier (particularly when the latter is used as a microphone amplifier) to maintain the amplifier output between 70mV and 87mV rms for a 35dB range of input. A one second 'hold' period is provided which prevents any increase of background noise during pauses in speech.

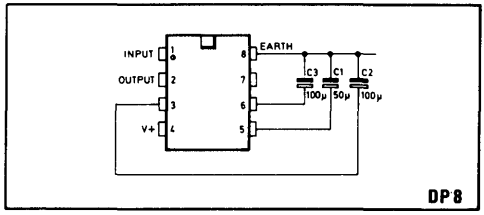


Fig. 1 Pin connections (top view)

FEATURES

- Wide Dynamic Range
- Speech Pause Memory
- Fast Attack/Adaptive Decay
- Only 4 External Components

APPLICATIONS

- Speech-Derived AGC Systems

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30 °C to +85° C
Supply voltage	−9V
Operating temperature	−30 °C to +70°C

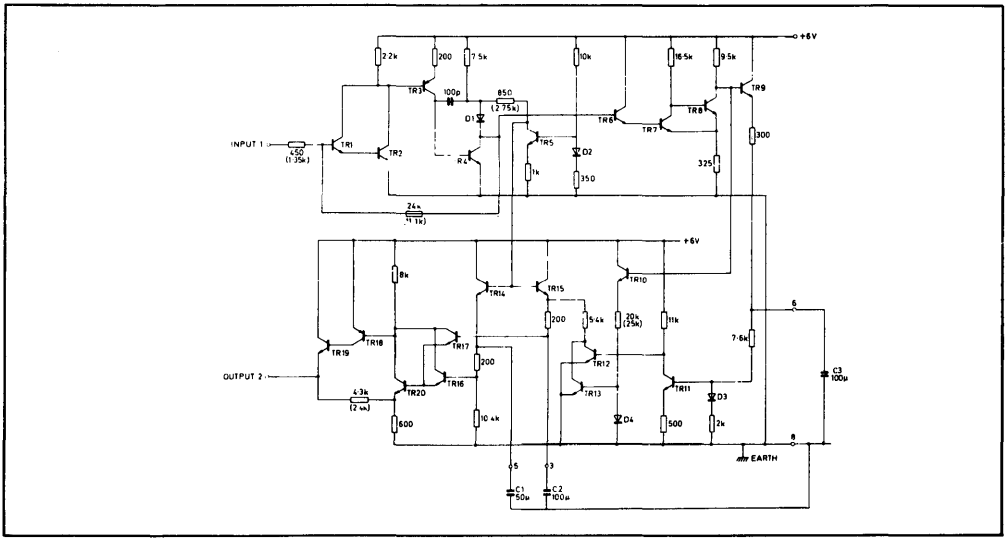


Fig. 2 Circuit diagram of SL1620C and SL1621C (component values for SL1620C are shown in brackets)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage = 6V
Temperature = +25°C
Input signal frequency = 1kHz

Characteristic	Circuit	Typical Value	Units	Test conditions
Input for 0.65V DC output	SL1620C	70	mVrms	See Fig. 6 } Measurement accuracy 1 dB
Input for 1.5V DC output	SL1620C	87	mVrms	See Fig. 6
Input for 2.2V DC output	SL1621C	7.0	mVrms	See Fig. 7
Input for 4.6V DC output	SL1621C	11.0	mVrms	See Fig. 7
*Fast rise time, t_1	Both	20	ms	0–50% full output } C_1 = 50µF
*Fast decay time, t_2	Both	200	ms	100%–36% voltage on C_1
*Slow rise time, t_3	Both	200	ms	Time to output transition point } C_2 = 100µF
Input 3 dB point	Both	10	kHz	
Maximum fade rate	SL1620C	0.22	V/s	
	SL1621C	0.45	V/s	
*Hold collapse time, t_4	Both	200	ms	Full-zero output
*Hold time, t_5	Both	1.0	s	C_3 = 100µF
AC ripple on output	Both	12	mVp-p	1kHz. Output open circuit
Maximum output voltage	SL1620C	2	V	
	SL1621C	5	V	
Quiescent current consumption	Both	3	mA	
Surge current	Both	30	mA	
Input resistance	SL1620C	1.4	kΩ	
	SL1621C	500	Ω	
Output current	SL1620C	1.7	mA	@ + 2V output
	SL1621C	2.5	mA	@ + 5.1V output

*See Fig. 3

DESCRIPTION

The operation of the SL1621C is described with reference to the circuit diagram, Fig. 2 and Fig. 3 which illustrates the dynamic response of a receiver controlled by the SL1621C.

The SL1621C consists of an input AF amplifier TR1-TR4 (3dB point: 10KHz) coupled to a DC output amplifier, TR16-TR19, by means of a voltage back-off circuit, TR5 and two detectors, TR14 and TR15, having short and long rise and fall time constants respectively.

The detected audio signal at the input will rapidly establish an AGC level, via TR14, in time t_1 (see Fig. 3). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is the more sensitive.

If signals exist at the SL1621C input which are greater than approximately 4mV rms they will actuate the trigger circuit TR6-TR8 whose output pulses will provide a discharge current for C2 via TR10, TR13.

By this means the voltage on C2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20 dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However, should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C3 via TR9, so holding off TR12 via TR11. When the trigger pulses cease, C3 discharges and after t_5 turns on TR12. Capacitor C2 is discharged rapidly (in time t_4) via TR12 and so full receiver gain is restored. The hold time, t_5 is approximately one second with C3 = 100μF. If signals reappear during t_5, then C3 will re-charge and normal operation will continue. The C3 re-charge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 3 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

OPERATING NOTES

The various time constants quoted are for C1 = 50μF and C2 = C3 = 100μF. These time constants may be altered by varying the appropriate capacitors.

An input coupling capacitor is required. This should normally be 0.33μF for an SL1621C and about 1μF for an SL1620C.

Fig. 4 shows how the SL1621C may be connected into a typical SSB receiver.

Fig. 5 shows how the SL1620C is used to control the gain of the SL1630C audio amplifier. The operation of the SL1620C is exactly the same as that of the SL1621C and the diagram showing the dynamic response of the closed loop system, Fig. 3, is equally applicable to the SL1630C/SL1620C combination. Again, the time constants may be altered by varying the capacitor values.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least 500μF so that it is not affected by the current surge resulting from a sudden input on pin 1. The devices may be used with a supply of up to +9V.

In a receiver for both AM and SSB using an SL623C detector/carrier AGC generator, the AGC outputs of the SL1621C and SL623C may be connected together provided that no audio reaches the SL1621C input while the SL623C is controlling the system

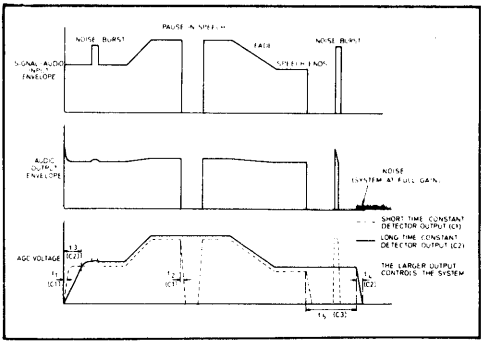


Fig. 3 Dynamic response

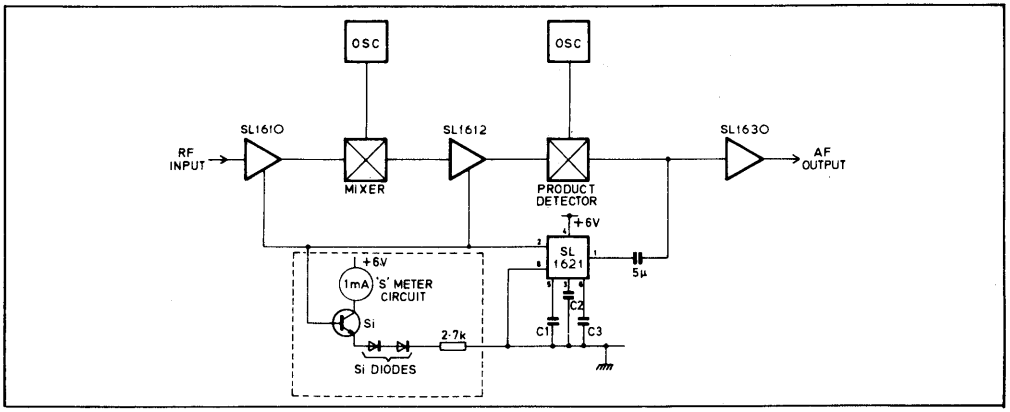


Fig. 4 SL1621C used to control an SSB receiver

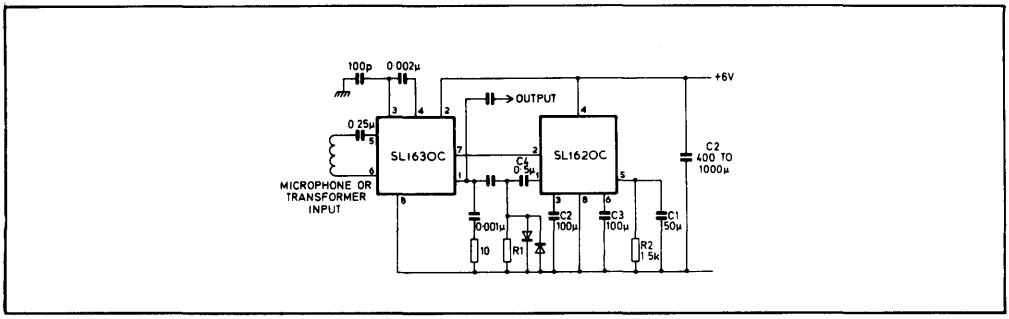


Fig. 5 SL1620C used to control an SL1630C audio amplifier

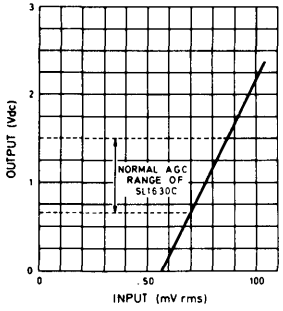


Fig. 6 Transfer characteristic of SL1620C

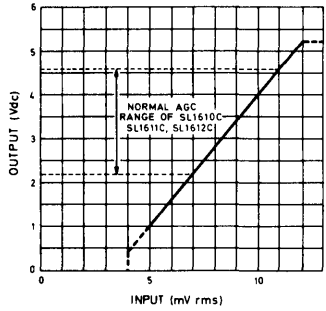


Fig. 7 Transfer characteristic of SL1621C

SL1623C

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL1623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL1610C, SL1611C and SL1612C RF and IF amplifiers. It is complementary to the SL1621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL1610C and one SL1612C amplifier, the SL1623C will maintain the output within a 5 dB range for a 90 dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100 mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL1623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies. The encapsulation is a 14 lead DIL package and the device is designed to operate from a 6 volt supply, over a temperature range of −30°C to +70°C.

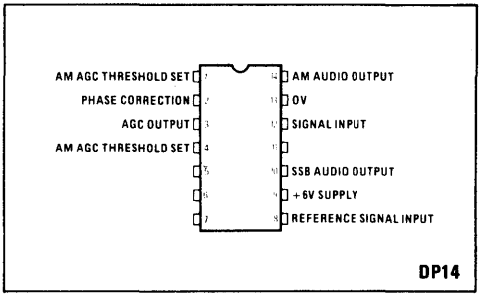


Fig. 1 Pin connection

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to +85°C
Ambient operating temperature	0°C to +80°C
Supply voltage	−0.5V to +12V

ELECTRICAL CHARACTERISTICS @ SUPPLY = +6V, Tamb = +25°C

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
SSB Audio Output		30		mV rms	Signal Input 20mV rms @ 1.748 MHz. Ref. Signal Input 100mV rms @ 1.750 MHz
AM Audio Output		55		mV rms	Signal Input 125mV rms @ 1.75 MHz. Modulated to 80% @ 1kHz.
AGC Range (change in input level to increase AGC output voltage from 2.0V to 4.6V)		5		dB	Initial signal input 125mV rms at 1.75 MHz. Mod. to 80% at 1 kHz. Output Set with 10kΩ pot between pins 1&4 to 2.0V.
Quiescent Current Consumption		9		mA	Output open circuit.
Max. operating frequency		30		MHz	

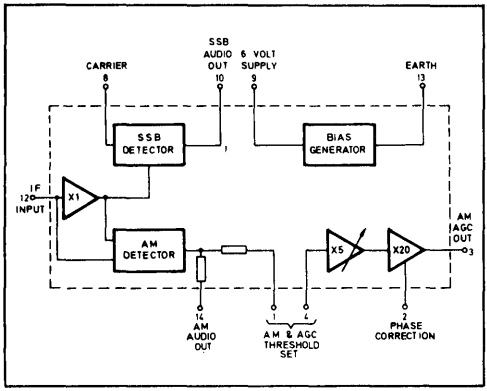


Fig. 2 Block Diagram

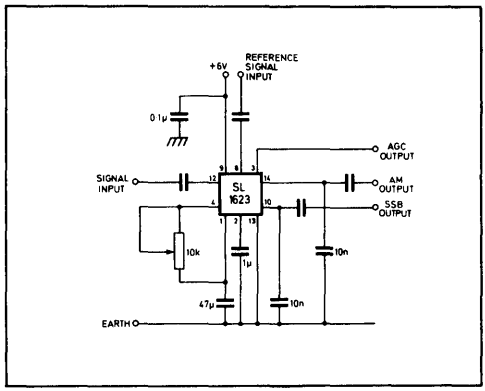


Fig. 3 Typical circuit using the SL1623C as signal detector and AGC

Plessey Semiconductors

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1625C
AM DETECTOR & AGC AMPLIFIER

The SL1625 is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator. It is designed specially for use in SSB/AM receivers in conjunction with SL1610C, SL1611C and SL1612C RF and IF amplifiers.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL1610C and SL1612C amplifier, the SL1625 will maintain the output within a 5 dB range for a 90 dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100 mV, contributes negligible distortion up to 90% modulation.

The SL1625 is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies. The encapsulation is an 8 lead DIL package and the device is designed to operate from a 6 volt supply, over a temperature range of 30°C to+70°C.

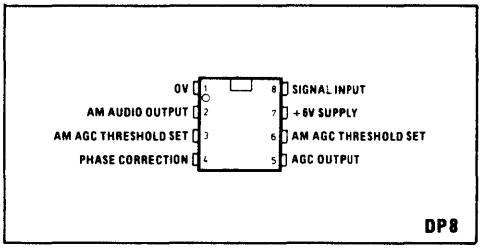


Fig. 1 Pin connection

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to + 85°C
Supply voltage	−0.5V to +12V

ELECTRICAL CHARACTERISTICS @ SUPPLY =+6V, T_{amb} = +25°C

Characteristic	Value			Units	Test Conditions
	Min.	Typ.	Max.		
AM Audio Output	40	55	70	mV rms	Signal Input 125mV rms @ 1.75 MHz. Modulated to 80% @ 1 kHz.
AGC Range (change in input level to increase AGC output voltage from 2.0V to 4.6V)		5		dB	Initial signal input 125mV rms at 1.75 MHz. Mod. to 80% at 1 kHz. Output Set with 10k pot between pins 3 & 6 to 2.0V.
Quiescent Current Consumption		9	15	mA	Output open circuit.
Max. operating frequency		30		MHz	

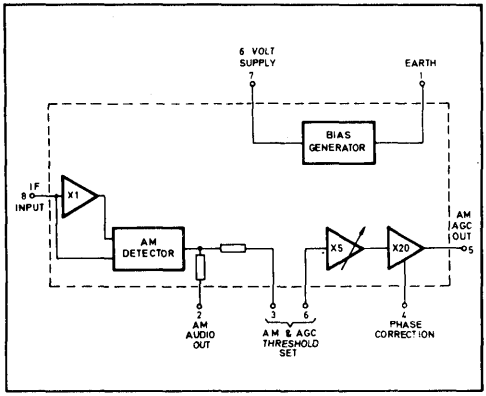


Fig. 2 Block Diagram

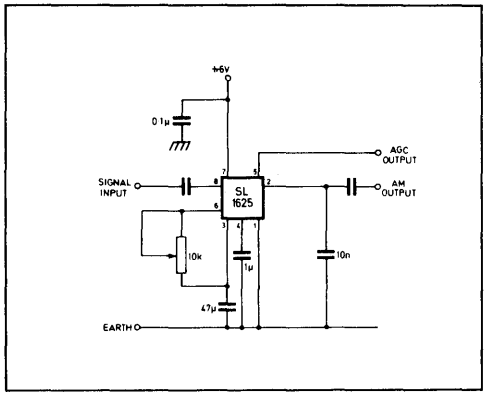


Fig. 3 Typical circuit using the SL1625 as signal detector and AGC generator.

SL1626C

AUDIO AMPLIFIER AND VOGAD

The SL1626C is a silicon integrated circuit combining the functions of audio amplifier with voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low-sensitivity microphone and to provide an essentially constant output signal for a 60dB range of input.

The encapsulation is an 8-lead plastic dual-in-line package and the device is designed to operate from a 6V ±0.5 volt supply, over a temperature range of -30°C to +70°C

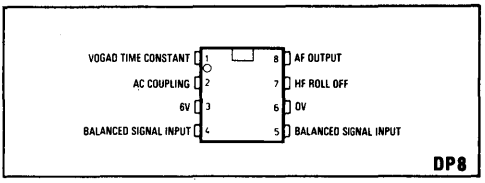


Fig. 1 Pin connections (top)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Prevention
- Speech Recording
- Level Setting Systems

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Input frequency 1kHz
Supply voltage +6V
Temperature +25°C

Characteristic	Value			Unit	Conditions
	Min.	Typ.	Max.		
VOGAD output level	55	90	140	mV rms	Balanced signal input 18mV rms
AF amplifier voltage gain		52		dB	Balanced signal input 72uV rms
Quiescent current consumption		14	20	mA	6V supply
Decay time (see note 1)		1.0		s	Original balanced signal input 18mV rms
Attack time (see note 2)		20		ms	Original balanced signal input 1.8mV rms
Total harmonic distortion of VOGAD output		2		%	Balanced signal input 90mV rms
Differential input impedance		300		Ω	
Single-ended input impedance		180		Ω	
AF amplifier output resistance		50		Ω	
Minimum load resistance — AF amplifier o/p		1000		Ω	
VOGAD operating threshold (whisper threshold) at input		100		μV rms	
Input for 10% distortion		130		mV rms	
Supply line rejection at VOGAD o/p		15		dB	
Common mode signal handling		50		mV p-p	

NOTES

1. Decay time is the time for VOGAD output to return within 10% of original absolute level when signal input voltage is switched down 20dB.
2. Attack time is the time for VOGAD output to return to within 10% of original absolute level when signal input voltage is switched up 20dB.

OPERATING NOTES

The SL1626 will operate from a range of supply voltages from 4V up to 12V.

The input stage is a differential class A-B stage with AGC terminal. The accurate balance of the input stage and high common-mode rejection ratio of the second stage gives an overall common-mode rejection ratio of greater than 30dB.

Typically, the amplifier will handle differential input signals of up to 375mV p-p. When used in the unbalanced mode either pin 4 or pin 5 may be used as the input, the other being decoupled to earth.

The LF cut-off of the amplifier is set by C1 and also by the values of coupling capacitors to the input pins (pin 4 and pin 5). Coupling capacitors should be used if the DC potential of the input is not floating with respect to earth.

The HF cut-off is set by C2 (see Fig. 3). The VOGAD threshold may be increased by connecting and external conductance between pins 7 and 8. The threshold is increased by approximately 20dB for 1 millimho of conductance; the value of C2 should be adjusted in conjunction with any threshold alteration in order to obtain the desired bandwidth.

C3 and R1 set the attack and decay rates of the VOGAD. In Fig. 3, C3=47uF and R1=1Mohm which give an attack time constant (gain increasing) of 20ms and a decay rate of 20dB/s. C1=2.2uF and C2 =4.7nF give a 3dB bandwidth of approximately 300Hz to 3kHz.

ABSOLUTE MAXIMUM RATINGS

Continuous supply voltage (positive)	12V
Storage temperature	−30°C to +85°C
Ambient operating temperature	−30°C to +70°C

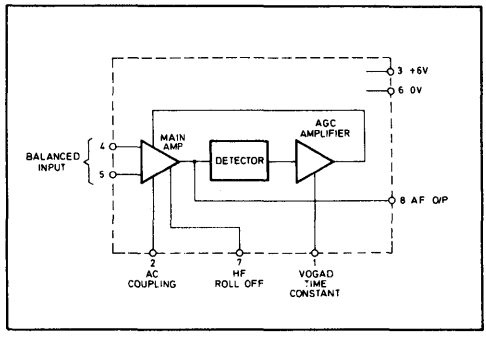


Fig. 2 Block diagram

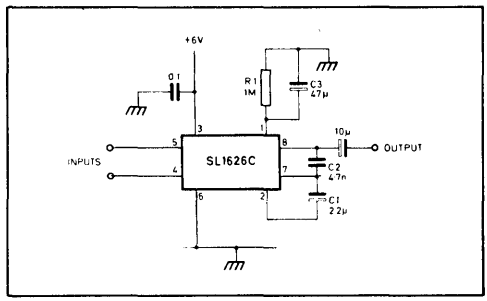


Fig. 3 Connection diagram for SL1626C used as a microphone amplifier

Plessey Semiconductors

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1630C
MICROPHONE/HEADPHONE AMPLIFIER

The SL1630C is designed specifically for use as a microphone or headphone amplifier. It has a voltage gain of 100, will accept balanced or unbalanced inputs, and can deliver up to 200 mW output from a class AB push-pull output stage.

A gain control facility with a logarithmic law allows AGC to be applied when the device is used as a microphone amplifier, and also allows remote volume control with a linear potentiometer. Gain reduction of 60dB may be obtained.

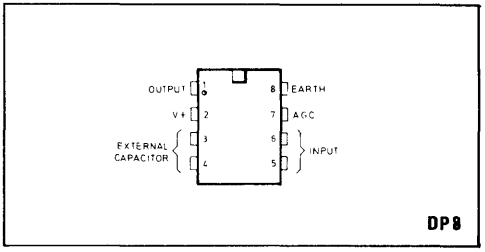


Fig. 1 Pin connections (top view)

FEATURES

- 40dB Gain
- Voltage-Controlled Gain
- 200 mW output
- Low Output Impedence

APPLICATIONS

- Low-Power Audio O/P Stages
- Preamplifiers (with or without AGC)

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to + 85°C
Operating temperature	
6V supply	−30°C to +70°C
12V supply	−30°C to +70°C
Supply voltage	+15V

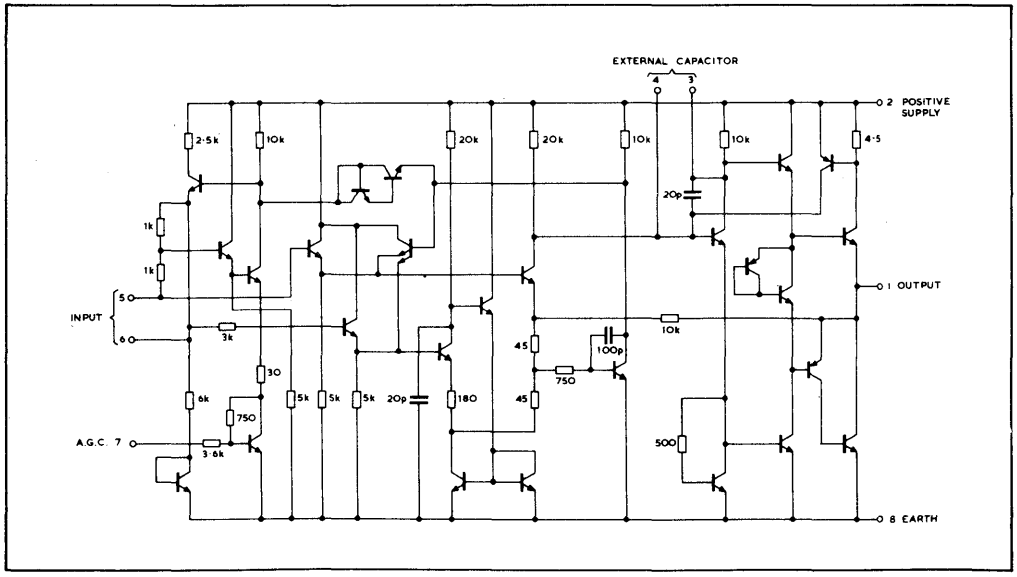


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +25°C
Signal Frequency = 1kHz
Supply = 12V

Characteristic	Typical Value	Units	Test conditions
Differential input voltage gain	40	dB	Input 1mVrms
Single ended input voltage gain	46	dB	Input 1mVrms
Maximum output voltage	1	Vrms	6V supply
	2	Vrms	12V supply
Maximum output power	See Fig. 7		0.5% distortion
Quiescent current (See also Fig. 7)	5	mA	6V supply
	12	mA	12V supply
Differential input impedance	2.0	kΩ	
Single ended input impedance	1.0	kΩ	
Output impedance	1.5	Ω	
Gain control range (See Fig. 6)	60	dB	
Maximum input (with gain reduced)	50	mVrms	10% distortion
Short circuit output current	110	mA	Irrespective of supply

OPERATING NOTES

Frequency Response

As with most small-signal integrated circuits, the inherent bandwidth of the SL1630C is quite large. It extends from low audio frequencies up to approximately 0.5 MHz, unless restricted by a roll-off capacitor (C1) connected between pins 3 and 4. The approximate upper cut-off frequency is then given by

$$\omega_c \simeq \frac{10^8}{C1}$$

Where C1 is in picofarads

Microphone Amplifier

Fig. 3 shows the SL1630C used with a balanced input on pins 5 and 6. If the load resistance increases with frequency it is necessary to stabilize the output circuitry. This is accomplished with 10Ω in series with 1nF connected between pin 1 and earth. The earth return to pin 8 must not share any common leads, particularly with the input. Decoupling pins 2 and 6 should follow normal engineering practice.

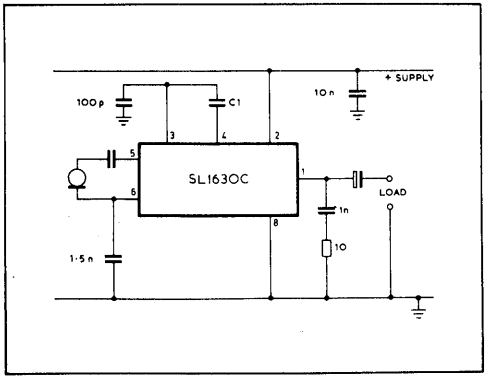


Fig. 3 SL1630C used as a microphone amplifier

Headphone Amplifier

Fig. 4 shows the SL1630C in a circuit suitable for powering a headset. The input is an unbalanced source connected to pin 5 and the device is decoupled at pins 1, 2 and 6 in the same manner as the microphone amplifier.

Manual gain adjustment using the remote gain control facility is also shown; R1 and R2 are chosen with regard to Fig. 6 to give the desired control range.

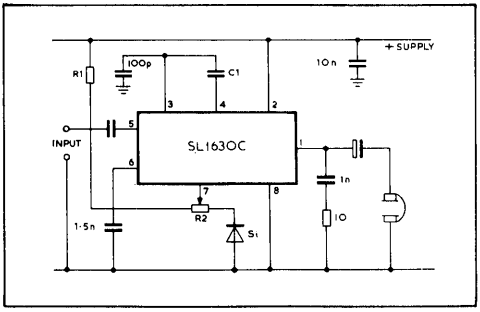


Fig. 4 SL1630C used as a headphone amplifier

Automatic Gain Control

To apply AGC, an SL1620C should be used as shown in the circuit of Fig. 5. This will give effective gain control with a low audio-frequency cut-off of 200 Hz and a control response time of approximately 20 ms.

To preserve low-frequency stability and prevent motor-boating, C4 should not exceed the value given and, whilst R1 should not exceed 300Ω, the time constant C3R1 must not be greater than 800 μs.

R2 is non-essential, but is useful if the input is likely to contain a large component below 300 Hz. C2 should be used if the power supply has a source impedance of more than a few ohms or is connected by long wires.

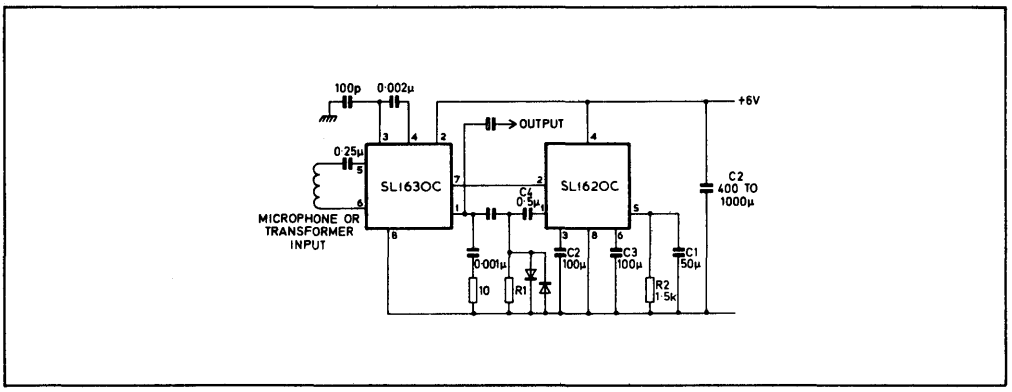


Fig. 5 SL1630C used with SL1620C to achieve automatic gain control

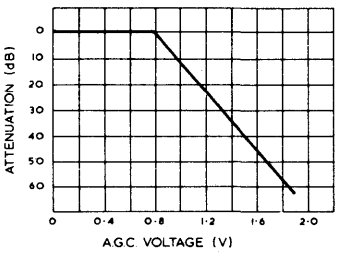


Fig. 6 AGC characteristics

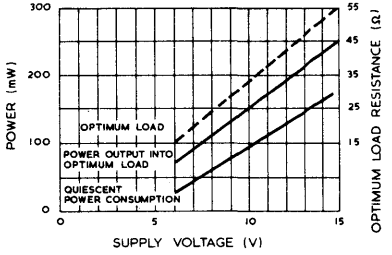


Fig. 7 Power characteristics

SL1631C

MICROPHONE/HEADPHONE AMPLIFIER

The SL1631C is designed specifically for use as a microphone or headphone amplifier. It has a voltage gain of 100, will accept balanced or unbalanced inputs, and can deliver up to 200mW output from a class AB push-pull output stage.

A gain control facility with a logarithmic law allows AGC to be applied when the device is used as a microphone amplifier, and also allows remote volume control with a linear potentiometer. Gain reduction of 60dB may be obtained.

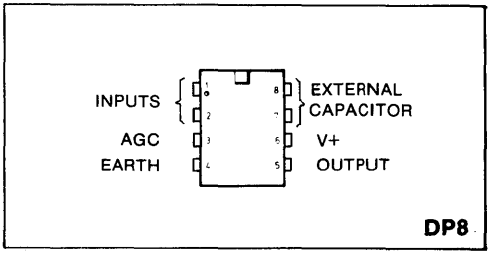


Fig. 1. Pin Connections (top view)

FEATURES

- 40dB Gain
- Voltage Controlled Gain
- 200mW output
- Low Output Impedance

APPLICATIONS

- Low-Power Audio O/P Stages
- Preamplifiers (with or without AGC)

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30°C to + 85°C
Operating temperature	
6V supply	−30°C to +70°C
12V supply	−30°C to +70°C
Supply voltage	+15V

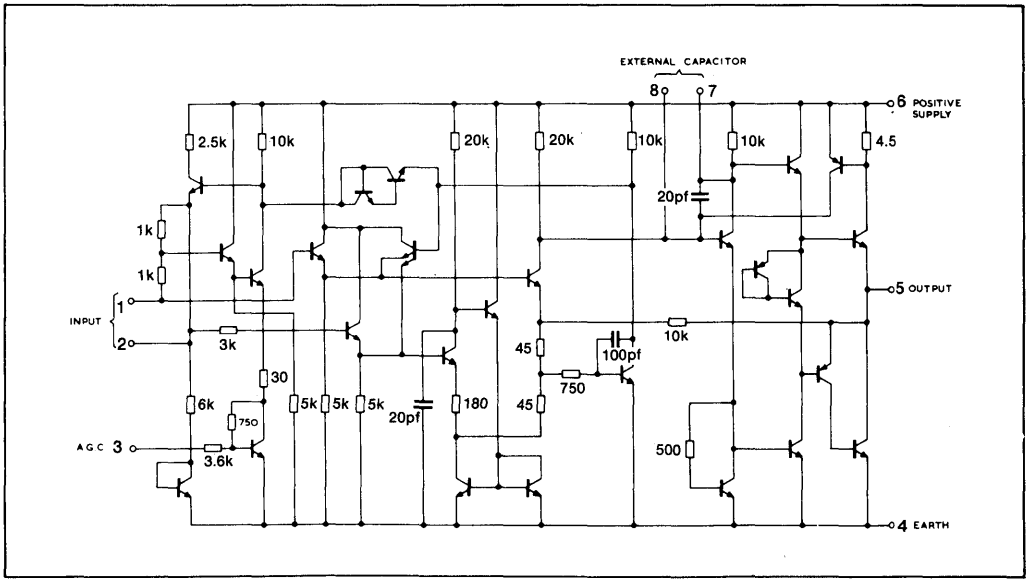


Fig. 2. Circuit Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature = +25oC
Signal Frequency = 1kHz
Supply = 12V

Characteristic	Typical Value	Units	Test conditions
Differential input voltage gain	40	dB	Input 1mVrms
Single ended input voltage gain	46	dB	Input 1mVrms
Maximum output voltage	1	Vrms	6V supply
	2	Vrms	12V supply
Maximum output power	See Fig. 7		0.5% distortion
Quiescent current (See also Fig. 7)	5	mA	6V supply
	12	mA	12V supply
Differential input impedance	2.0	kΩ	
Single ended input impedance	1.0	kΩ	
Output impedance	1.5	Ω	
Gain control range (See Fig. 6)	60	dB	
Maximum input (with gain reduced)	50	mVrms	10% distortion
Short circuit output current	110	mA	Irrespective of supply

OPERATING NOTES

Frequency Response

As with most small-signal integrated circuits, the inherent bandwidth of the SL1631C is quite large. It extends from low audio frequencies up to approximately 0.5MHz, unless restricted by a roll-off capacitor (C1) connected between pins 3 and 4. The approximate upper cut-off frequency is then given by.

$$\omega_c \simeq \frac{10^8}{C1}$$

Where C1 is in picofarads

Microphone Amplifier

Fig. 3 shows the SL1631C used with a balanced input on pins 5 and 6. If the load resistance increases with frequency it is necessary to stabilize the output circuitry. This is accomplished with 10Ω in series with 1nF connected between pin 1 and earth. The earth return to pin 8 must not share any common leads, particularly with the input. Decoupling pins 2 and 6 should follow normal engineering practice.

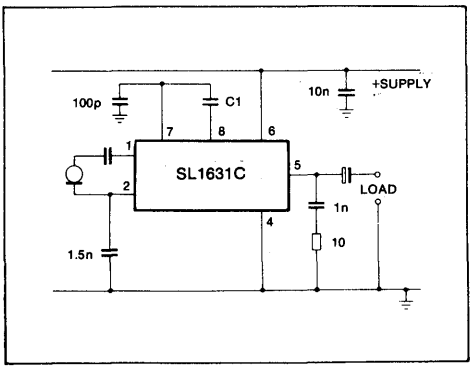


Fig. 3 SL1630C used as a microphone amplifier

Headphone Amplifier

Fig. 4. shows the SL1631C in a circuit suitable for powering a headset. The input is an unbalanced source connected to pin 5 and the device is decoupled at pins 1, 2 and 6 in the same manner as the microphone amplifier.

Manual gain adjustment using the remote gain control facility is also shown, R1 and R2 are chosen with regard to Fig. 6 to give the desired control range.

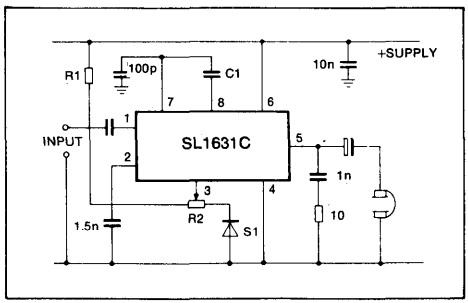


Fig. 4 SL1630C used as a headphone amplifier

Automatic Gain Control

To apply AGC, an SL1620C should be used as shown in the circuit of Fig. 5. This will give effective gain control with a low audio-frequency cut-off of 200 Hz and a control response time of approximately 20ms.

To preserve low-frequency stability and prevent motor boating, C4 should not exceed the value given whilst R1 should not exceed 300Ω, the time constant C3R1 must not be greater than 800μs.

R2 is non-essential, but is useful is the input is. likely to contain a large component below 300 Hz. C2 should be used if the power supply has a source impedance of more than a ohms or is connected by long wires.

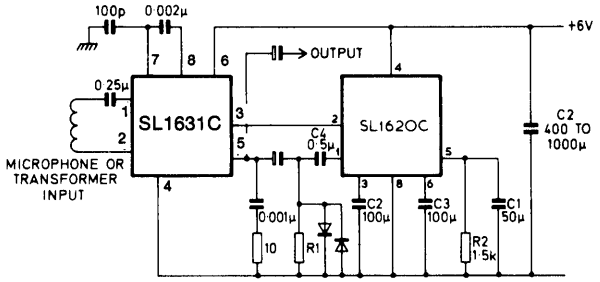


Fig. 5 SL1630C used with SL1620C to achieve automatic gain control

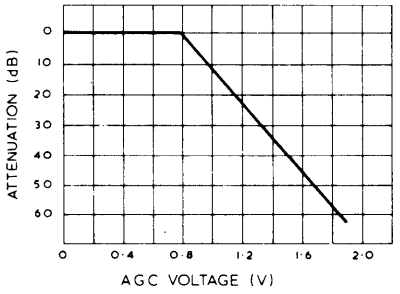


Fig. 6 AGC characteristics

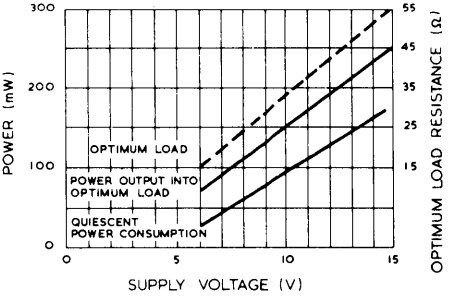


Fig. 7 Power characteristics

Plessey Semiconductors

SL1600 SERIES
COMMUNICATIONS CIRCUITS

SL1640C & SL1641C
DOUBLE BALANCED MODULATORS

The SL1640C is designed to replace the conventional diode ring modulator, in RF and other communications systems, at frequencies of up to 75MHz. It offers a performance competitive with that of the diode ring while eliminating the associated transformers and heavy carrier drive power requirements.

At 30MHz, carrier and signal leaks are typically −40dB referred to the desired output product frequency. Intermodulation products are −45dB with a 60 mV rms input signal.

The SL1641C is a version of the SL1640C intended primarily for use in receiver mixer applications for which it offers a lower noise figure and lower power consumption. No output load resistor is included and signal leakage is higher, but otherwise the performance is identical to that of the SL1640C.

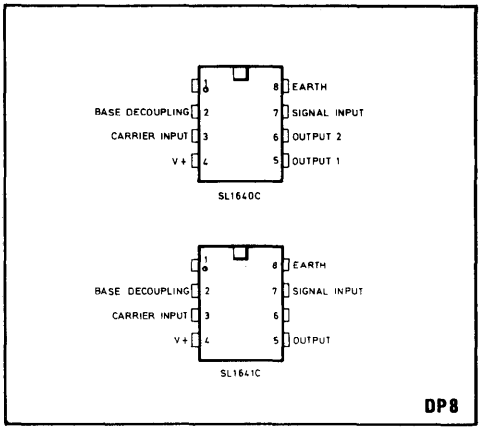


Fig. 1 Pin connections (top view)

FEATURES

- Low Carrier Leak
- Low Signal Leak
- Low Intermodulation Products
- Low Carrier Power Requirement
- Wide Bandwidth
- Minimal External Components

APPLICATIONS

- SSB and DSB Generators
- Detectors
- Phase Comparators
- Mixers

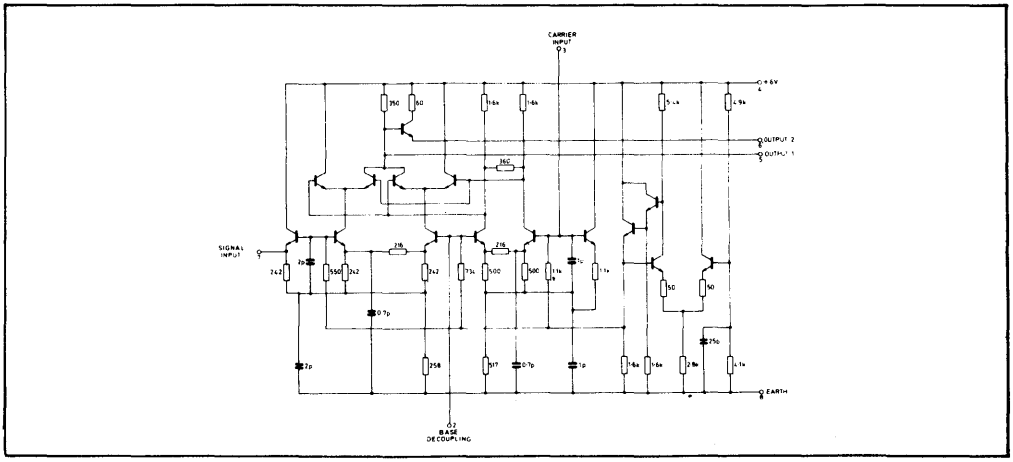


Fig. 2 Circuit diagram of SL1640C

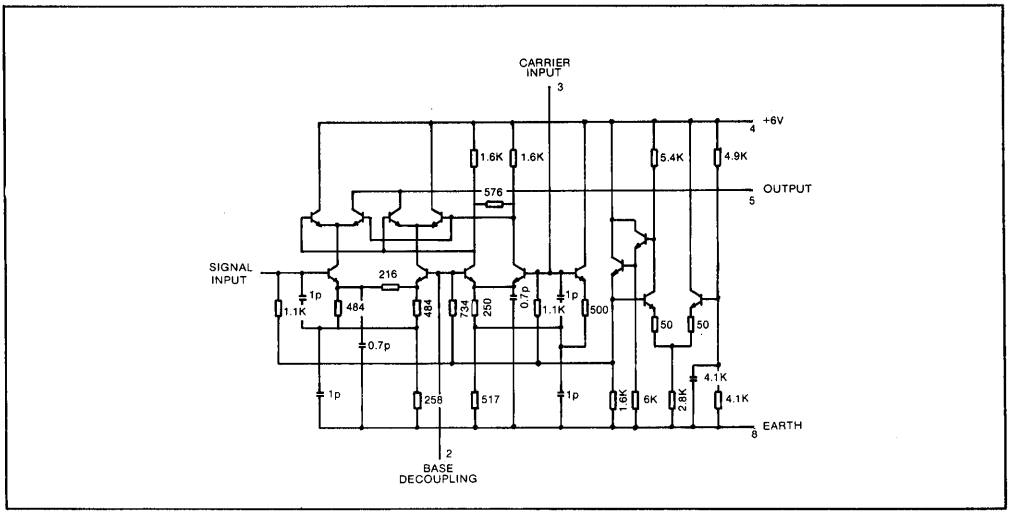


Fig. 3 Circuit diagram of SL1641C

OPERATING NOTES

The SL1640C circuit requires input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see electrical characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance.

Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at pin 2 would give rise to poor rejection figures and to distortion.

If the emitter follower is used, an external load resistor must be provided to supply emitter current. The quiescent output voltage from the emitter follower (pin 6) is +4.6V. To achieve maximum rejection figures at high frequencies, pin 1 (which is connected to the header) should be connected to earth and effective HT decoupling should be employed. The DC impedance should not exceed 800 ohms.

The SL1640C/1641C may be used with supply voltages of up to +9 volts with increased dissipation.

Signal and carrier leaks may be minimised with 10kΩ potentiometers and 330kΩ resistors connected as shown in Fig. 4. R1 is adjusted to minimise signal leak; R2 to minimise carrier leak.

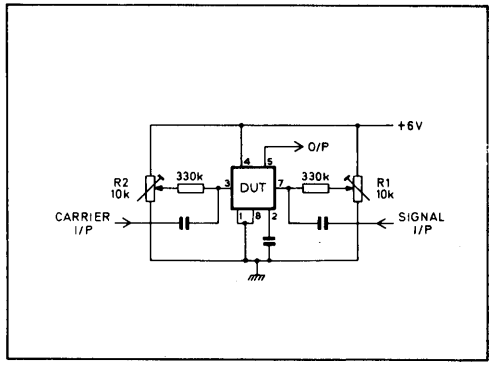


Fig. 4 Signal and carrier leak adjustments

The SL1641C is very similar to the SL1640C and similar operating notes apply. A current output is provided in the SL1641C to enable a tuned circuit to be directly connected. If both output sidebands are developed across the load (i.e. wideband operation), the AC impedance of the load must be less than 800Ω. If the output at one sideband frequency is negligible, the AC impedance may be raised to 1.6kΩ. It may be further raised if it is not desired to use the maximum input swing of 210mV rms. The DC resistance of the load should not exceed 800Ω.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage = +6V
Temperature = +25°C

Characteristics	Circuit	Typical Value	Units	Test conditions
Conversion gain	SL1640C	0	dB	
Signal leak	SL1640C	−40	dB	
$\left[\frac{\text{Signal output}}{\text{Desired sideband output}}\right]$				Signal: 70mVrms, 1.75MHz Carrier: 100mVrms, 28.25MHz Output: 30MHz
Carrier leak	SL1640C	−40	dB	
$\left[\frac{\text{Carrier output}}{\text{Desired sideband output}}\right]$				
Intermodulation products	SL1640C	−45	dB	Signal 1: 42.5mVrms, 1.75MHz Signal 2: 42.5mVrms, 2MHz Carrier: 100mVrms, 28.25MHz Output: 29.75MHz
Conversion gain	SL1641C	0	dB	400Ω load Signal: 70mVrms, 30MHz
Signal leak	SL1641C	−18	dB	Carrier: 100mVrms, 28.25MHz Output: 1.75MHz
Carrier leak	SL1641C	−25	dB	
Intermodulation products	SL1641C	−45	dB	Signal 1: 42.5mVrms, 30MHz Signal 2: 42.5mVrms, 31MHz Carrier: 100mVrms, 28.25MHz Output: 3.75MHz
Carrier input impedance	Both	1kΩ//4pF		
Signal input impedance	SL1640C	500Ω//5pF		
	SL1641C	1kΩ//4pF		
Output impedance	SL1640C	350Ω//8pF		Output 1
(see Operating Notes)	SL1641C	8pF		
Max. input before limiting	SL1640C	210	mVrms	
	SL1641C	250	mVrms	
Quiescent current consumption	SL1640C	12	mA	
	SL1641C	10	mA	
Noise figure	SL1640C	15	dB	
	SL1641C	12	dB	
Signal leak variation	Both	±2	dB	
Carrier leak variation	Both	±2	dB	
Conversion gain variation with temperature	Both	±1	dB	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Operating temperature	0°C to +70°C
Supply voltage	+9V

PLESSEY
Semiconductors

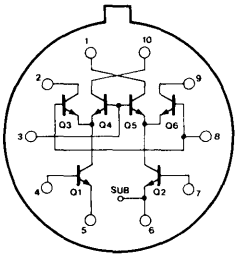
SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

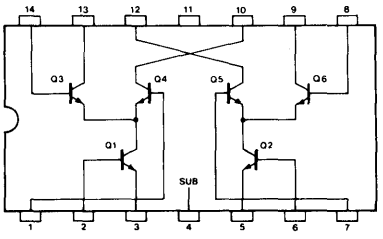
The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5 GHz, (typically 5GHz).

The SL2363 is in a 10 lead TO5 encapsulation.

The SL2364 is in a 14 lead DIL ceramic encapsulation.



SL2363C CM10



SL2364C DG14

Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10μA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10μA
BV_{CIO}	16	40		V	I_C = 10μA
h_{FE}	20	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$					I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}			0.5	pF	V_{CB} = 0
C_{CI}			1	pF	V_{CB} = 0

NOTE 1 ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

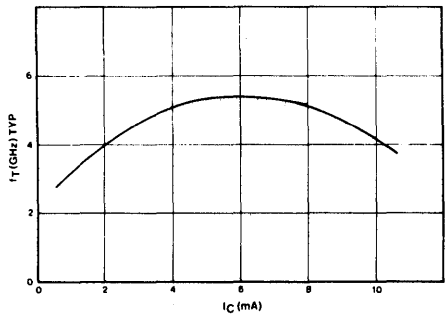


Fig. 2 Collector current

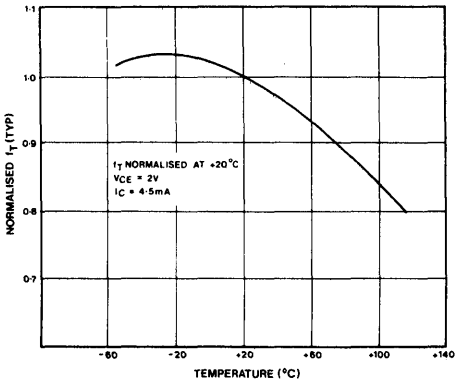


Fig. 3 Chip temperature

Plessey Semiconductors

SL3000 SERIES
TRANSISTOR ARRAYS

SL3045C SL3046C
TRANSISTOR ARRAYS

The SL3045 and SL3046 are monolithic arrays of five general purpose high frequency transistors arranged as a differential pair and three isolated transistors. The transistors feature a V_{BE} matching of, typically, better than 5mV between any pair, an f_T of 300MHz and a low noise figure.

The SL3045 is available only in a ceramic dual-in-line package; the SL3046 is packaged in plastic dual-in-line.

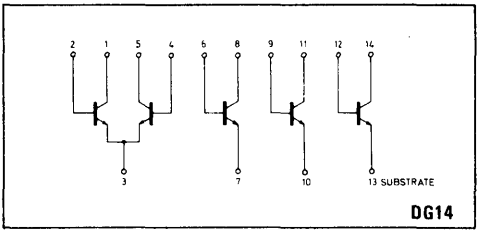


Fig. 1 Pin connections

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = +25°C

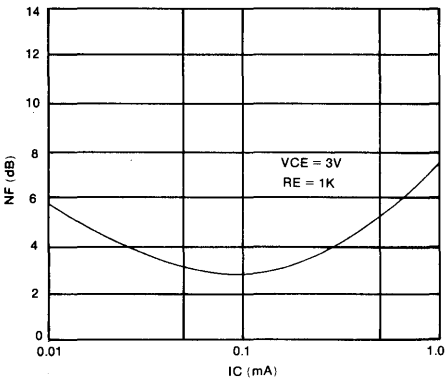
Static Characteristics

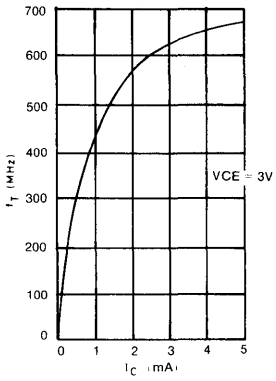
Symbol	Characteristic	Value			Units	Test conditions
		Min.	Typ.	Max.		
BV_{EBO}	Emitter-base breakdown	5			V	I_E = 10μA
BV_{CEO}	Collector-emitter breakdown	15			V	I_C = 1mA
BV_{CBO}	Collector-base breakdown	20	50		V	I_C = 10μA
BV_{CIO}	Collector-substrate breakdown	20	70		V	I_C = 10μA
I_{CEO}	Collector cut off current			0.5	μA	V_{CE} = 10V, I_B = 0
I_{CBO}	Collector cut off current			4	nA	V_{CB} = 10V, I_E = 0
$V_{BE(ON)}$	Base emitter voltage		0.71		V	V_{CE} = 3V I_C = 1mA
			0.78		V	V_{CE} = 3V I_C = 10mA
$V_{CE(SAT)}$	Collector-emitter saturation		0.3		V	I_B = 1mA I_C = 10mA
h_{FE}	Static forward current-transfer ratio		120			V_{CE} = 3V I_C = 10mA
		40	100			V_{CE} = 3V I_C = 1mA
			50			V_{CE} = 3V I_C = 10μA
I_{10}	Input offset current—differential pair		0.2	2	μA	V_{CE} = 3V I_C = 1mA
ΔV_{BE1}	Input offset voltage—differential pair		0.35	5	mV	V_{CE} = 3V I_C = 1mA
ΔV_{BE2}	Input offset voltage-isolated transistors		0.45	5	mV	V_{CE} = 3V I_C = 1mA
$\frac{\partial \Delta_{BE}}{\partial T}$	Temperature co-efficient of input offset voltage		2		μV/°C	V_{CE} = 3V I_C = 1mA
$\frac{\partial V_{BE(ON)}}{\partial T}$	Temperature co-efficient of base emitter-voltage		1.8		mV/°C	V_{CE} = 3V I_C = 1mA

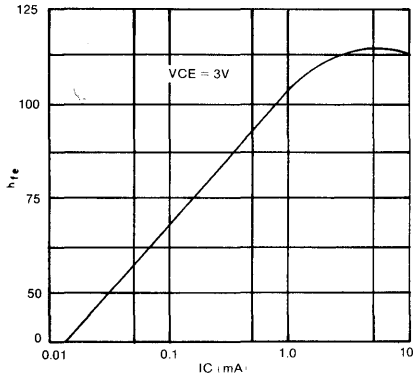
Dynamic Characteristics

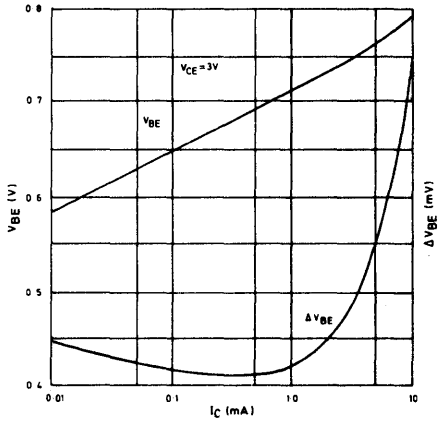
Symbol	Characteristic	Value			Units	Test conditions
		Min.	Typ.	Max.		
N.F.	Wide band noise figure		3.5		dB	f = 10Hz to 10kHz V_{CE} = 3V I_C = 100μA Source resistance = 1kΩ
Y_{fe}	Forward transfer admittance		31–j1.5		mmho	
Y_{ie}	Input admittance		0.3–j0.04		mmho	f = 1MHz
Y_{oe}	Output admittance		0.003+j0.04		mmho	V_{CE} = 3V I_C = 1mA
Y_{re}	Reverse transfer admittance		0.000–j0.003		mmho	
h_{fe}	Forward current transfer ratio		110			
h_{ie}	Short cct. input impedance		3.5		kΩ	f = 1kHz
h_{oe}	Open cct. output admittance		15.6		μmho	V_{CE} = 3V I_C = 1mA
h_{re}	Open circuit reverse voltage transfer ratio		$1.8x10^{-4}$			
f_t	Gain-bandwidth product	500	600		MHz	V_{CE} = 3V I_C = 3mA
C_{IB}	Emitter-base capacitance		1.7		pF	V_{EB} = 3V I_E = 0
C_{OB}	Collector-base capacitance		1.5		pF	V_{CB} = 3V I_C = 0
C_{CI}	Collector-substrate capacitance		3.0		pF	V_{CS} = 3V I_C = 0

CHARACTERISTIC GRAPHS









ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. The isolation pin must always be negative with respect to the collectors.

V_{CBO} = 20V V_{EBO} = 15V I_C = 50mA I_B = 25mA
V_{CEO} = 15V V_{CIO} = 20V I_E = 50mA

SL3045C — DG

Storage temperature	—55 C to +175 C
Junction temperature	+175 C
Package dissipation	750mW (derate linearly from 55 C to +175 C)

SL3046C — DP

Storage temperature	—55 C to +125 C
Junction temperature	+125 C
Package dissipation	500mW (derate linearly from 55 C to +125 C)

Plessey Semiconductors

SL3000 SERIES
TRANSISTOR ARRAYS

SL3081D SL3082D

GENERAL PURPOSE HIGH CURRENT NPN TRANSISTOR ARRAYS

The SL3081 and SL3082 consist of seven high current (100mA max) silicon NPN transistors on a common monolithic substrate. The SL3081 is connected in a common emitter configuration and the SL3082 is connected in a common collector configuration.

The SL3081 and SL3082 are capable of directly driving both incandescent seven segment displays and LED seven segment displays.

A separate substrate connection is provided, for maximum flexibility in circuit design.

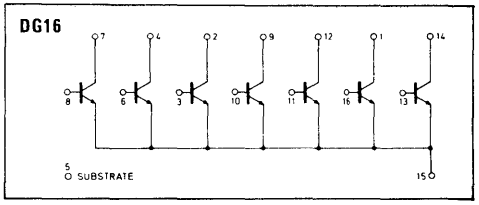


Fig. 1 SL3081 pin connections

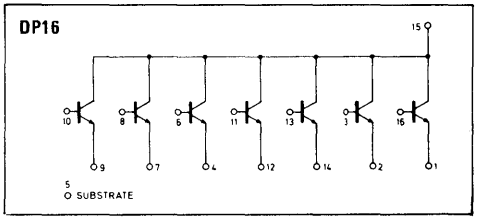


Fig. 2 SL3082 pin connections

FEATURES

- Seven Transistors Permit a Wide Range of Applications
- Common Emitter (SL3081) or Common Collector (SL3082) Configuration
- High I_C 100mA max (each transistor)
- Low $V_{CE\ SAT}$ 0.4V Typ. @ 50mA

APPLICATIONS

- Drivers for Incandescent Display Devices
- SL3081: Driver for Common Anode 7-Segment LED Displays
- SL3082: Driver for Common Cathode 7-Segment LED Displays
- MOS Clock and Calculator Display Interface Circuits
- Relay and Solenoid Drivers
- Thyristor and Triac Control Circuitry

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C

All electrical ratings apply to individual transistors; termal ratings apply to total package dissipation.

The collector of each transistor of the SL3081 and SL3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and to provide normal transistor operation. To avoid undesired coupling, the substrate (pin 5) should be maintained at either DC or signal (AC) earth.

Electrical Ratings

V_{CEO} = 12V, V_{CBO} = 20V, V_{EBO} = 5V, V_{CIO} = 20V, $I_C = I_E$ = 100mA

Power dissipation	500mW

Thermal Ratings

Storage temperature	−55°C to +175°C
Junction operating temperature	+175°C

ELECTRICAL CHARACTERISTICS @ T_A = 22°C ±2°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector-base breakdown	BV_{CBO}	20	50		V	I_C = 500μA, I_E = 0
Collector-substrate breakdown	BV_{CIO}	20	70		V	I_{CI} = 500μA I_B = 0
Collector-emitter breakdown	BV_{CEO}	12	20		V	I_C = 1mA, I_B = 0
Emitter-base breakdown	BV_{EBO}	5	5.6		V	I_E = 500μA
DC forward current transfer ratio	h_{FE}	30	68			V_{CE} = 0.5V, I_C = 30mA
		40	70			V_{CE} = 0.8V, I_C = 50mA
Collector emitter saturation	$V_{CE(SAT)}$					
SL3081, SL3082			0.27	0.5	V	I_C = 30mA, I_B = 1mA
SL3081			0.4	0.7	V	I_C = 50mA, I_B = 5mA
SL3082			0.4	0.8	V	I_C = 50mA, I_B = 5mA
Collector cut-off current	I_{CEO}			10	μA	V_{CE} = 10V, I_B = 0
Collector cut-off current	I_{CBO}			1	μA	V_{CB} = 10V, I_E = 0

Plessey Semiconductors

SL3000 SERIES
TRANSISTOR ARRAYS

SL3083D
GENERAL PURPOSE HIGH CURRENT NPN TRANSISTOR ARRAY

The SL3083 is an array of five independent high current (100mA max) NPN transistors on a common monolithic substrate. In addition, two of the transistors (TR1 and TR2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

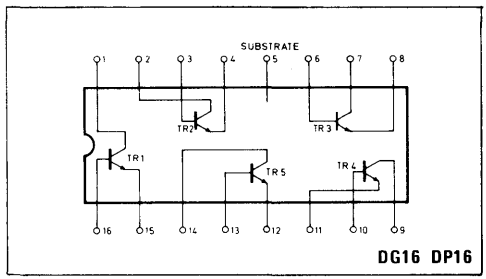


Fig. 1 SL3083 pin connections

FEATURES

- High I_C 100mA Max
- Low V_{CESAT} 0.7V Max @ 50mA
- Matched Pair (TR1 and TR2)
  - ΔV_{BE} ±5mV Max
  - I_{IO} 2.5μA Max @ 1mA
- 5 Independent Transistors plus Separate Substrate Connection

APPLICATIONS

- Signal Processing and Switching Systems Operating From DC to VHF
- Lamp, Relay, Solenoid Driver
- Differential Amplifier
- Temperature Compensated Amplifier
- Thyristor Firing

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C

Electrical Ratings

V_{CEO} = 12V V_{CBO} = 20V, V_{EEO} = 5V, V_{CIO} = 20V,
$I_C = I_E$ = 100mA
Power dissipation 500mW

Thermal Ratings

Storage temperature −55°C to +175°C
Junction operating temperature +175°C

All electrical ratings apply to individual transistors; thermal ratings apply to total package dissipation.

The collector of each transistor of the SL3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and to provide normal transistor operation. To avoid undesired coupling, the substrate (pin 5) should be maintained at either DC or signal (AC) earth.

ELECTRICAL CHARACTERISTICS @ T_A = 22°C ±2°C

Characteristic	Symbol	Value			Units	Condition
		Min.	Typ.	Max.		
Collector-base breakdown	BV_{CBO}	20	50		V	I_C = 100μA, I_E = 0
Collector-emitter breakdown	BV_{CEO}	12	20		V	I_C = 1mA, I_B = 0
Collector-substrate breakdown	BV_{CIO}	20	70		V	I_{CI} = 100μA, I_E = 0 I_B = 0
Emitter-base breakdown	BV_{EBO}	5	5.6		V	I_E = 500μA, I_C = 0
Collector cut off current	I_{CEO}			10	μA	V_{CE} = 10V, I_B = 0
Collector cut off current	I_{CBO}			1	μA	V_{CB} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}	40	120			V_{CE} = 3V I_C = 10mA
DC forward current transfer ratio	h_{FE}	40	80			V_{CE} = 3V I_C = 50mA
Base emitter voltage	$V_{BE\ (ON)}$	0.65	0.74	0.85	V	V_{CE} = 3V I_C = 10mA
Collector emitter saturation	$V_{CE\ (SAT)}$		0.4	0.7	V	I_C = 50mA, I_B = 5mA
FOR TRANSISTORS T1 AND T2 (As a differential amplifier)						
Input offset voltage	ΔV_{BE}		1.2	5	mV	V_{CE} = 3V
Input offset current	I_{10}		0.7	2.5	μA	I_C = 1mA

SL3127C

HIGH FREQUENCY NPN TRANSISTOR ARRAY

The SL3127 consists of five general-purpose silicon NPN transistors on a common substrate. The monolithic construction provides close electrical and thermal matching of the five transistors. Each of the transistors exhibits a low noise figure (3.6 dB typ. @ 60 MHz) and a value of f_T greater than 1.5 GHz. Each of the transistors is individually accessible and a separate substrate connection is provided, which is used to ensure isolation between each transistor.

The SL3127 is pin compatible with RCA CA3127E.

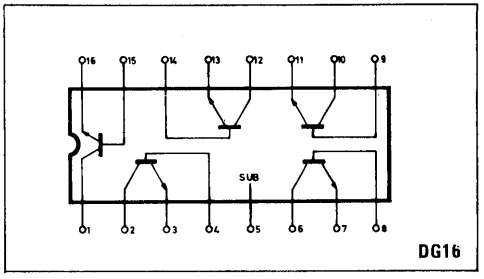


Fig. 1 Pin connections, top view

ABSOLUTE MAXIMUM RATINGS at $T_A = 25°C$

Power dissipation	
Any one transistor	150mW
Total package	300mW
Ambient temperature range	
Storage	−55 to +150°C
Operating	−55 to 125°C

The following limiting values apply to each device:

Collector to emitter voltage V_{CEO}	15V
Collector to base voltage V_{CBO}	20V
Collector to substrate V_{CIO}*	20V
Collector current I_C	20mA

*The collector of each transistor is isolated from the substrate by an integral diode. The substrate (pin 5) must be connected to the most negative point in the external circuit to maintain isolation between the transistors.

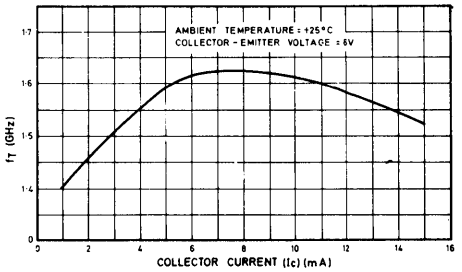


Fig. 2 Typical gain-bandwidth product (f_T) V. collector current

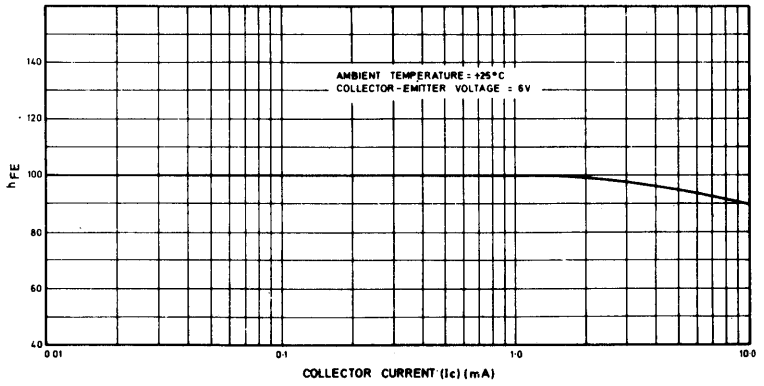


Fig. 3 DC forward current transfer ratio v. collector current

ELECTRICAL CHARACTERISTICS at T_A = +25°C for each transistor

Static characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max		
Collector-base breakdown voltage	BV_{CBO}	20	30		V	I_C = 1μA, I_E = 0
Collector-emitter breakdown voltage	BV_{CEO}	15	18		V	I_C = 1μA, I_B = 0
Collector-substrate breakdown voltage	BV_{CIO}	20	55		V	I_C = 1μA, I_B = 0, I_E = 0
Emitter-base breakdown voltage	BV_{EBO}	4.5	5.5		V	I_E = 10μA, I_C = 0
DC forward current transfer ratio	h_{FE}					V_{CE} = 6V
		40	95			I_C = 5mA
		40	100			I_C = 1mA
		40	100			I_C = 0.1mA
Base-emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector-emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Magnitude of difference in V_{BE}	ΔV_{BE}		0.5	5	mV	V_{CE} = 6V, I_C = 1mA
Magnitude of difference in I_B	ΔI_B		0.02	3	μA	V_{CE} = 6V, I_C = 1mA

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Gain-bandwidth product	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Noise Figure	NF		3.6		dB	V_{CE} = 6V, R_S = 200Ω
						f = 60MHz, I_C = 2mA
Knee of I/f noise figure curve	–		<1		kHz	V_{CE} = 6V, R_S = 200Ω
						I_C = 2mA

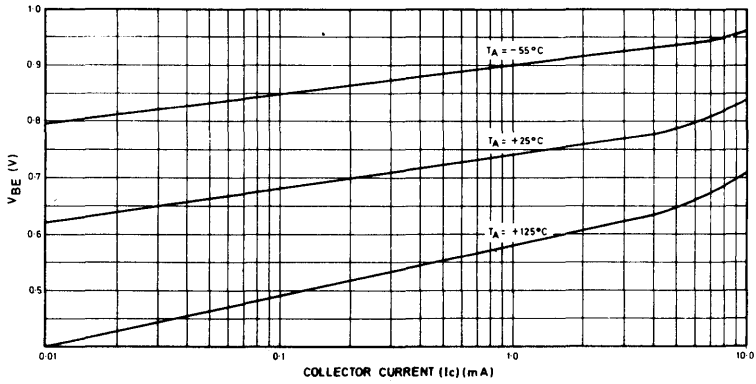


Fig. 4 Base-emitter voltage (V_{BE}) v. collector current

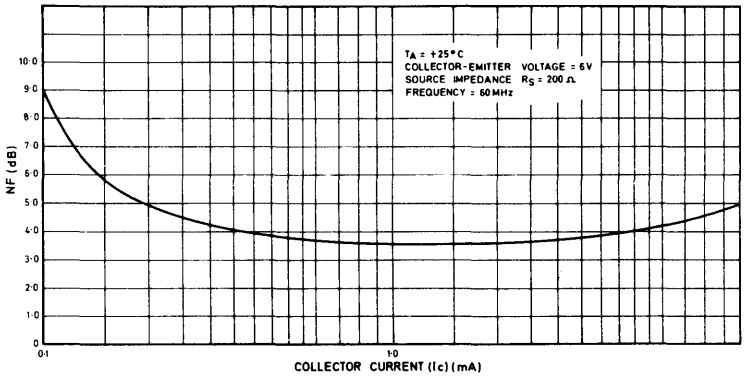


Fig. 5 Noise figure v. collector current

Plessey Semiconductors

SL300 SERIES
MATCHED TRANSISTORS

SL3145C
2·5 GHz TRANSISTOR ARRAY

The SL3145 is a monolithic array of five general purpose high frequency transistors arranged as a differential pair and three isolated transistors.

FEATURES

- f_T = 2.5 GHZ
- Wideband Noise Figure = 3dB
- V_{BE} Matching = Better than 5 mV
- Pin-Compatible with SL3045

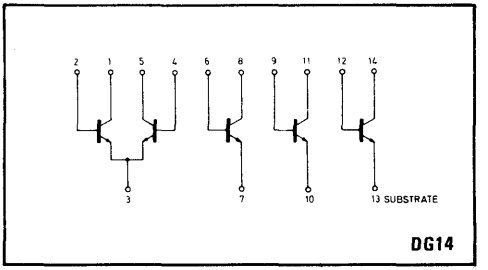


Fig. 1 Schematic and pin diagram

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):

T_{amb} = +25°C ±5°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Base-Isolation Voltage	10			V	I_B = 1μA
Emitter-base breakdown	5			V	I_C = 10μA
Collector-emitter breakdown	8	15		V	I_C = 10μA
Collector-base breakdown	12	24		V	I_E = 10μA
Collector-substrate breakdown	20	40		V	I_C = 10μA
Base-emitter voltage		0.73		V	V_{CE} = 2V, I_C = 1mA
Static forward current transfer ratio	30	80			V_{CE} = 2V, I_C = 1mA
Input offset current (differential pair)		0.2	2	μA	V_{CE} = 2V, I_C = 1mA
Input offset voltage (differential pair)		0.35	5	mV	V_{CE} = 2V, I_C = 1mA
Input offset voltage (others)		0.45	5	mV	V_{CE} = 2V, I_C = 1mA
Temperature coefficient input offset voltage		2		μV/°C	V_{CE} = 2V, I_C = 1mA
Temperature coefficient base emitter voltage		1.6		mV/°C	V_{CE} = 2V, I_C = 1mA
Wideband noise figure		3.0		dB	V_{CE} = 2V, I_C = 100μA R_S = 1kΩ
Gain-Bandwidth product		2.5		GHz	V_{CE} = 2V, I_C = 10mA
$V_{CE(SAT)}$		0.35		V	I_C = 10mA, I_B = 1mA
$V_{BE(SAT)}$		0.95		V	I_C = 10mA, I_B = 1mA
I_{CBO}		0.3		nA	V_{CB} = 16V
I_{CIO}		0.6		nA	V_{CI} = 20V
I_{BIO}		1.2		nA	V_{BI} = 10V
C_{eb}		0.4		pF	Bias = 0V
C_{cb}		0.4		pF	Bias = 0V
C_{cI}		0.8		pF	Bias = 0V

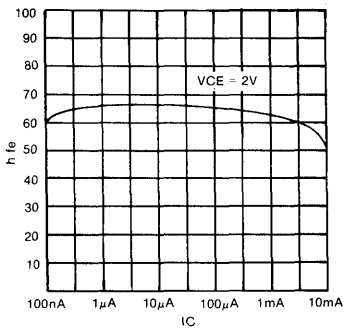


Fig. 2. Typical variation of h fe with IC

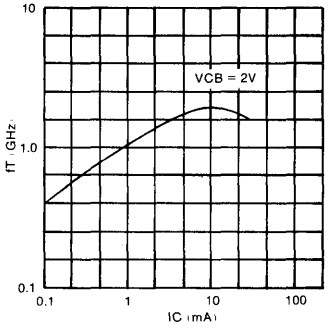


Fig. 3. Typical fTv. collector current (fT = f/h fe,f = 200MHz)

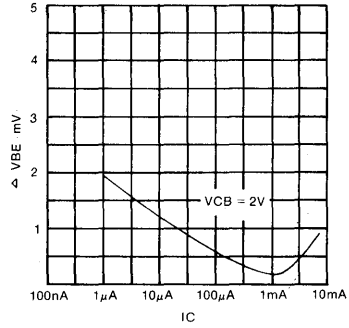


Fig 4. Typical VBE mismatch v. IC

ABSOLUTE MAXIMUM RATINGS

Storage temperature: −55°C to +150°C

Junction operating temperature: 150°C

V_{CBO}: 12V V_{EBO}: 5V I_C :20mA

V_{CEO}: 8V V_{CIO}: 20V

Maximum individual transistor dissipation: 200mW

Total package dissipation: 350mW

Plessey Semiconductors

SL3000 SERIES
TRANSISTOR ARRAYS

SL3146A, SL3146C
SL3183A, SL3183C
HIGH VOLTAGE TRANSISTOR ARRAYS

The Plessey Semiconductors SL3146A, SL3146, SL3183A and SL3183 are general-purpose high-voltage silicon NPN transistor arrays on a common monolithic substrate.

SL3146A and SL3146 (high voltage versions of SL3046) each consist of five transistors with two of the transistors connected to form a differential pair. These types are recommended for use in the DC to VHF range. The SL3146A and SL3146 are supplied in either 14 lead plastic DIL package (temperature range −40°C to +85°C) or 14-lead ceramic DIL package (temperature range −55°C to +125°C).

SL3183A and SL3183 consist of five high-current transistors with independent connections for each transistor. In addition, two of these transistors (TR1 and TR2) are matched at low current (i.e. 1mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. The SL3183A and SL3183 are high-voltage versions of the SL3083 and are supplied in either 16-lead plastic DIL package (temperature range −40°C to +85°C) or 16-lead ceramic package (temperature range −55°C to +125°C).

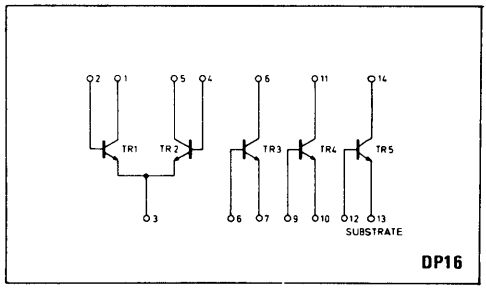


Fig. 1 SL3146/A pin connections

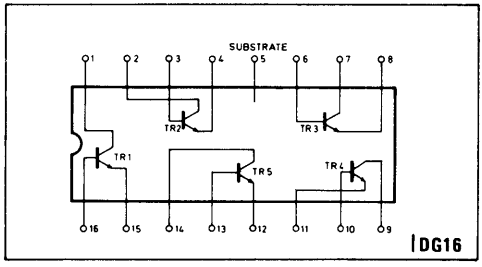


Fig. 2 SL3183/A pin connections

FEATURES

- Matched General Purpose Transistors
- V_{BE} Matched to ±5mV Max.
- Operation from DC to 120MHz (SL3146/A)
- Low Noise Figure: 3.2dB Typ. @ 1kHz (SL3146/A)
- High I_C: 75mA Max. (SL3183/A)

APPLICATIONS

- Signal Processing Systems, DC – VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (SL3183/A)
- Thyristor Firing (SL3183/A)

ELECTRICAL CHARACTERISTICS @ T_A = +25°C (SL3146/A)

Static Characteristics

Characteristic	Symbol	Value						Units	Test Conditions
		SL3146A			SL3146C				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Collector-base breakdown	BV_{CBO}	50	72		40	72		V	I_C = 10μA, I_E = 0
Collector-emitter breakdown	BV_{CEO}	40	56		30	56		V	I_C = 1mA, I_B = 0
Collector-substrate breakdown	BV_{VIO}	50	72		40	72		V	I_{CI} = 10μA, I_E = 0, I_B = 0
Emitter-base breakdown	BV_{EBO}	5	7.5		5	7.5		V	I_E = 10μA, I_C = 0
Collector cut-off current	I_{CEO}			5			5	μA	V_{CE} = 10V, I_B = 0
Collector cut-off current	I_{CBO}			100			100	nA	V_{CE} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}		85			85		–	I_C = 10mA
		30	100		30	100		–	I_C = 10μA V_{CE} = 5V
			90			90		–	I_C = 1mA
Base-emitter voltage	$V_{BE(ON)}$	0.63	0.73	0.83	0.63	0.73	0.83	V	V_{CE} = 3V, I_C = 1mA
Collector-emitter saturation	$V_{CE(SAT)}$		0.33			0.33		V	I_C = 10mA, I_B = 1mA
For Transistors TR1 and TR2 (as a Differential Amplifier)									
Input offset voltage	ΔV_{BE}		0.48	0.5		0.48	0.5	mV	V_{CE} = 5V, I_E = 1mA
Base-emitter temperature coefficient	$\frac{\partial V_{BE(ON)}}{\partial T}$		1.9			1.9		mV/°C	V_{CE} = 5V, I_E = 1mA
Input offset voltage temperature coefficient	$\frac{\partial \Delta V_{BE}}{\partial T}$		1.1			1.1		μV/°C	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA
Input offset current	I_{IO}		0.3	2		0.3	2	μA	V_{CE} = 5V, I_{C1} = I_{C2} = 1mA

Dynamic Characteristics

Low frequency noise figure	NF		3.25			3.25		dB	f = 1kHz, V_{CE} = 5V, I_C = 100μA, R_S = 1kΩ
Low Frequency Small Signal Equivalent Circuit Characteristics									
Forward current transfer ratio	h_{fe}		100			100		–	f = 1kHz, V_{CE} = 5V, I_C = 1mA
Short-circuit input impedance	h_{ie}		2.7			3.5		kΩ	
Open-circuit output admittance	h_{oe}		15.6			15.6		μmho	
Open-circuit reverse voltage transfer ratio	h_{re}		1.8×10^{-4}			1.8×10^{-4}		–	
Admittance Characteristics									
Forward transfer admittance	Y_{fe}		31–j1.5			31–j1.5		mmho	f = 1MHz, V_{CE} = 5V, I_C = 1mA
Input admittance	Y_{ie}		0.35+j0.04			0.35+j0.04		mmho	
Output admittance	Y_{oe}		0.001+j0.03			0.001+j0.03		mmho	
Reverse transfer admittance	Y_{re}		0.001–j0.001			0.001–j0.001		mmho	
Gain bandwidth product	f_t	300	500		300	500		MHz	V_{CE} = 5V, I_C = 3mA
Emitter-base capacitance	C_{BE}		0.7			0.7		pF	V_{EB} = 5V, I_E = 0
Collector-base capacitance	C_{OB}		0.37			0.37		pF	V_{CB} = 5V, I_C = 0
Collector-substrate capacitance	C_{C1}		2.2			2.2		pF	V_{CI} = 5V, I_C = 0

ELECTRICAL CHARACTERISTICS @ T_A = +25°C (SL3183/A)

Static Characteristics

Characteristic	Symbol	Value						Units	Conditions
		SL3183A			SL3183C				
		Min.	Typ.	Max.	Min.	Typ.	Max.		
For each transistor									
Collector-base breakdown voltage	BV_{CBO}	50			40			V	I_C = 100μA, I_E = 0
Collector-emitter breakdown voltage	BV_{CEO}	40			30			V	I_C = 1mA, I_B = 0
Collector-substrate breakdown voltage	BV_{CIO}	50			40			V	I_{CI} = 100μA, I_B = 0, I_E = 0
Emitter-base breakdown voltage	BV_{EBO}	5			5			V	I_E = 500μA, I_C = 0
Collector cut-off current	I_{CEO}			10			10	μA	V_{CE} = 10V, I_B = 0
Collector cut-off current	I_{CBO}			1			1	μA	V_{CE} = 10V, I_E = 0
DC forward current transfer ratio	h_{FE}	40			40				V_{CE} = 3V, I_C = 10mA
		40			40				V_{CE} = 5V, I_C = 50mA
Base-emitter voltage	V_{BE}	0.65	0.75	0.85	0.65	0.75	0.85	V	V_{CE} = 3V, I_C = 10mA
Collector-emitter saturation voltage	*$V_{CE(SAT)}$		1.7	3.0		1.7	3.0	V	I_C = 50mA, I_B = 5mA
For transistors TR1 and TR2 (as a differential amplifier)									
Absolute input offset voltage	$\lvert V_{IO} \rvert$		0.47	5.0		0.47	5.0	mV	V_{CE} = 3V, I_C = 1mA
Absolute input offset current	$\lvert I_{IO} \rvert$		0.78	2.5		0.78	2.5	μA	V_{CE} = 3V, I_C = 1mA

*A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

	SL3146C	SL3146A	SL3183C	SL3183A	
Power dissipation (per transistor)	300	300	500	500	mW
Power dissipation (total package)					
Up to +55°C	750	750	750	750	mW
Above +55°C		Derate linearity 6 - 67			mW/°C
Operating temperature range					
Plastic package	−40 to +85	−40 to +85	−40 to +85	−40 to +85	°C
Ceramic package	−55 to +125	−55 to +125	−55 to +125	−55 to +125	°C
Storage temperature range					
Plastic package	−65 to +150	−65 to +150	−65 to +150	−65 to +150	°C
Ceramic package	−65 to +175	−65 to +175	−65 to +175	−65 to +175	°C
The following ratings apply to individual transistors					
Collector-emitter voltage, V_{CEO}	30	40	30	40	V
Collector-base voltage, V_{CBO}	40	50	40	50	V
Collector-substrate voltage, V_{CIO}	40	50	40	50	V
Emitter-base coltage, V_{EBO}	5	5	5	5	V
Collector current, I_C	50	50	75	75	mA
Base current, I_B			20	20	mA

*The collector of each transistor is isolated from the substrate by an integral diode.

NOTE: The substrate pin must always be negative with respect to the collectors.

SL6270C

GAIN CONTROLLED PREAMPLIFIER

The SL6270C is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 60dB range of input. The dynamic range, attack and decay times are controlled by external components.

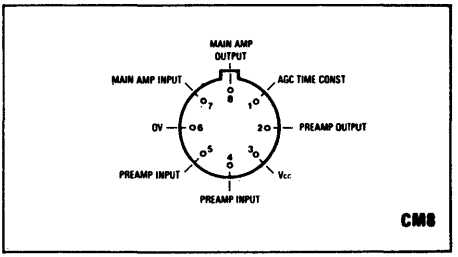


Fig. 1 Pin connections, SL6270C – CM

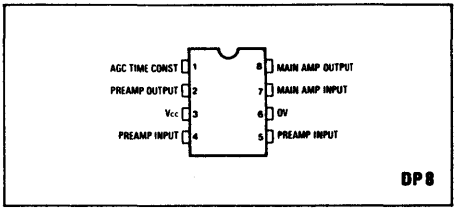


Fig. 2 Pin connections, SL6270C – DP

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +150°C
Operating temperature: −55°C to +85°C

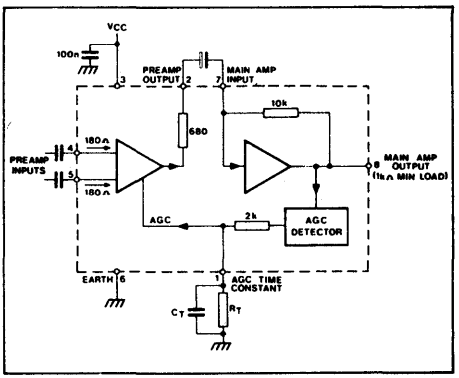


Fig. 3 SL6270C block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage Vcc: 6V ± 0.5V
Input signal frequency: 1kHz
Ambient temperature: −30°C to +85°C
Test circuit shown in Fig. 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance	100	180		Ω	Pin 4 or 5
Differential input impedance	200	300		Ω	
Voltage gain	40	52		dB	72μV rms balanced input
Output level	55	90	140	mV rms	18mV rms balanced input
THD		2	5	%	90mV rms balanced input

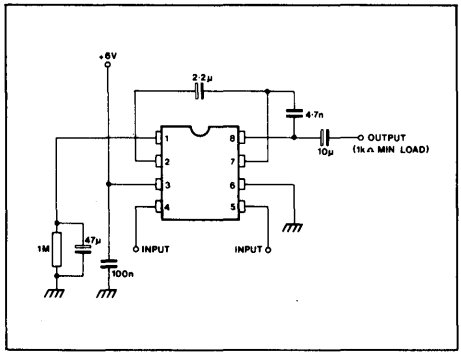
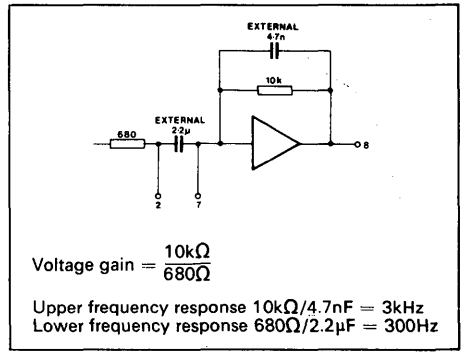


Fig. 4 SL6270C test and application circuit



Voltage gain = $\frac{10k\Omega}{680\Omega}$

Upper frequency response 10kΩ/4.7nF = 3kHz
Lower frequency response 680Ω/2.2μF = 300Hz

Fig. 5 SL6270C frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270C may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270C is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a −3dB point at 300Hz, corresponding to 2.2μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270C has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and decay times

Normally the SL6270C is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig. 4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

$$\text{Attack time} = 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

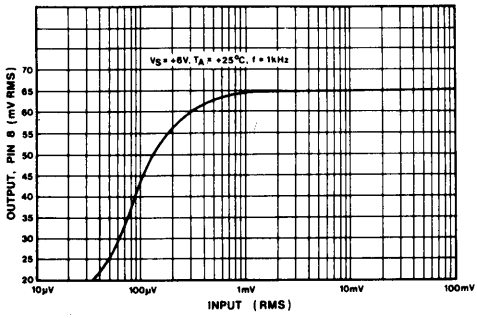


Fig. 6 Voltage gain (single ended input)

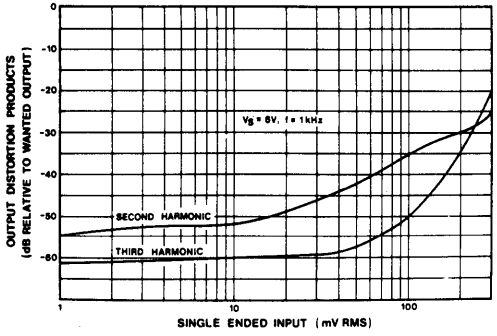


Fig. 7 Overload characteristics

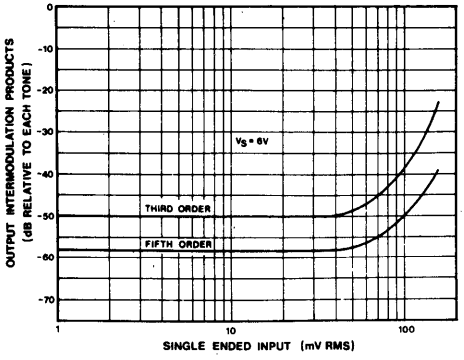


Fig. 8 Intermodulation distortions (1.55 and 1.85kHz tones)

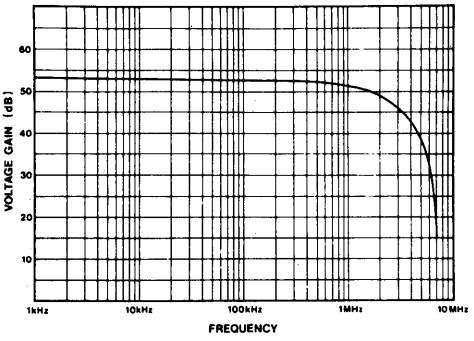


Fig. 9 Open loop frequency response

SL 6290C

TRANSMIT CIRCUIT

The SL6290 is a bipolar integrated circuit combining the functions of audio amplifier, voice operated gain adjusting device (VOGAD) and audio limiter; also included are an RF buffer and relay driver.

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 60dB range of input.

The output can be adjusted to provide varying degrees of clipping of the audio signal. This, when filtered to remove the edges, gives varying degrees of audio compression. The limiter has an open-collector output so that a present resistor can be used to set the maximum modulation required at the transmitter output.

The RF buffer is incorporated to provide isolation betwwen the synthesiser and RF power amplifier used in a typical complete transceiver.

The relay driver can be used as a receive transmit relay driver.

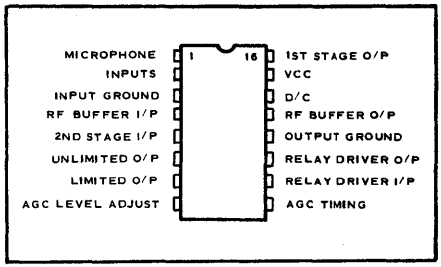


Fig. 1 Pin Connections (top view)

FEATURES

- Fast Attack
- Speech Compression
- Maximum Modulation Adjustment
- Constant Output Signal
- Relay Driver
- RF Buffer

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−30° to C + 85° C
Operating temperature	−30° to C + 70° C

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Prevention
- Speech Recording
- Level Setting Systems

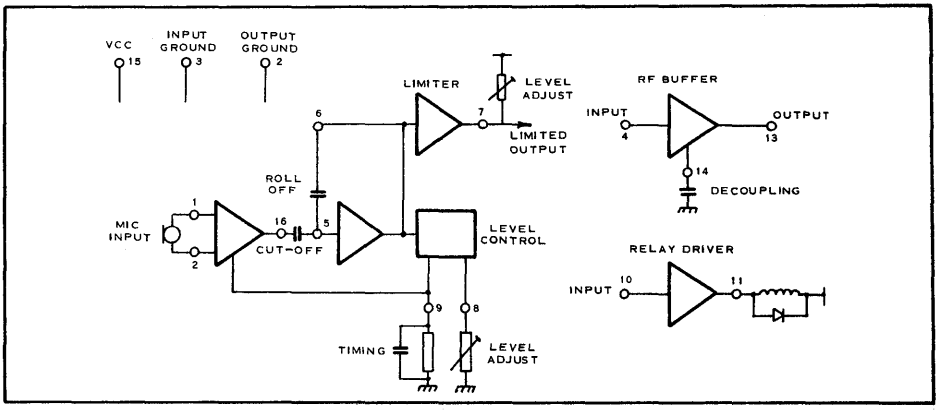


Fig. 2 SL6290 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc = +5V
Tamb = +25 C
Input frquency = 1kHz

Characteristic	Value			Units	Conditions
	Min	Typ.	Max.		
Current into pin 15		15	25	mA	5V on pin 15
Supply voltage pin 15	4.5	5	5.5	V	
Output pin 6		150		mV rms	2.2 pin 8 to earth 20mV rms signal I/P
Output pin 6		0		mV rms	Pin 8 connected to earth. 20mV rms signal I/P
AF amp voltage gain		54		dB	
Decay time		1.0		sec	See note 1
Attack time		20		ms	See note 2
THD		1.0		%	1mV I/P
Diff. input impedance		300		Ω	
Single ended I/P impedance		180		Ω	
AF amp O/P impedance		50		Ω	
Limiter O/P level		1.0		Vp-p	4.7k pin 7 to Vcc 20mV rms signal I/P
Limiter 0.5dB compression point		64		mV	4,7k pin 7 to Vcc
Pin 6 O/P change with temp		0.2		%/°C	-30°C to +70° C
Pin 7 O/P change with temp		0.12		%/°C	-30°C to +70°C
Buffer gain @ 27MHz		0		dB	500 Ω O/P load 50 ΩI/P
Reverse gain @ 27MHz		70		dB	500 Ω O/P 50 ΩI/P
Change of voltage gain from nominal with temp		±0.6		dB	-30°C to +70°C
Relay driver O/P current			50	mA	Pin 10 to 5V Vcc
Relay driver I/P current		1		mA	No external resistor on pin 10
Vsat relay O/P		1		V	Pin 11 sinking 50mA
Change of Vsat with temp		0.1		%/°C	-30°C to +70°C
Voltage on pin 11			20	V	

Note 1. Decay time is the time for the VOGAD output to return to within 10% of its original absolute level when the signal input voltage is switched down by 20dB.

Note 2. Attack time is the time for the VOGAD output to return to within 10% of its original absolute level when the

OPERATING NOTES

The microphone input stage is different and the accurate balance of this stage and the high common-mode rejection of the second stage gives an overall common mode rejection ratio of greater than 30dB.

Typically, the amplifier will handle differential and single-ended signals of up to 375mV peak to peak. When used in the unbalanced mode either pin 4 or pin 5 may be used as the input, the other being de-coupled to earth.

The LF cut-off of the amplifier is set by the coupling capacitor between pin 16 and pin 5 and also by the values of coupling capacitors to the input pins (pin 1 and pin 2). Coupling capacitors should be used if the input is not floating with respect to earth.

The HF cut-off is set by the capacitor between pin 5 and pin 6. In addition, the gain of the circuit may be reduced by putting a resistor between these pins. The HF cut-off capacitor should be adjusted in con-junction with any gain alteration in order to obtain the desired bandwidth.

The resistor and capacitor on pin 9 set the attack and decay rates of the VOGAD.

The values of external components shown in Fig. 3 give an attack time better than 20ms, a decay rate of 20dB/s and a 3dB bandwidth of approximately 300Hz to 3kHz.

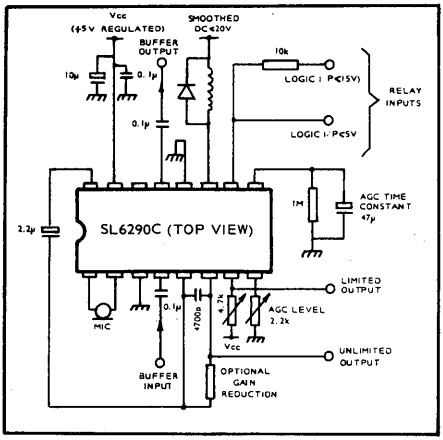


Fig. 3 SL6290 external connections

NOMINAL DC PIN VOLTAGES

Pin	Voltage (VDC)	Pin	Voltage (VDC)
1	1.6V	9	0V (no signal)
2	1.6V	10	0V (no input)
3	0V	11	5V
4	1.5V	12	0V
5	1.4V	13	1.7V
6	1.4V	14	4V
7	4.5V	15	5V
8	0.4V	16	2.5V

Table 1. Nominal DC pin voltages

SL6000 SERIES
COMMUNICATIONS CIRCUITS

SL6310C
SWITCHABLE AUDIO AMPLIFIER

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

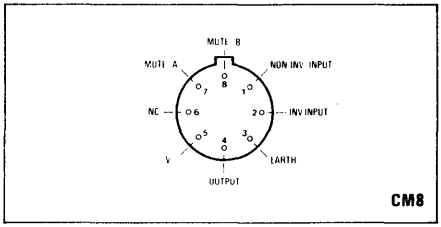


Fig. 1 Pin connections, SL6310C – CM

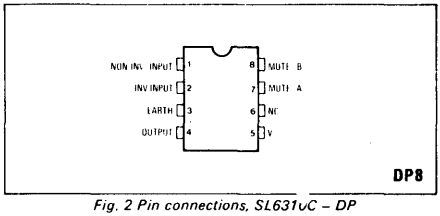


Fig. 2 Pin connections, SL631vC – DP

FEATURES

- Can be Muted with High or Low State Inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 13V
- Voltage Gain: 70dB
- Output into 8Ω on 9V Supply: 400mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 15V
Storage temperature: −55 C to +150 C
Chip temperature: +175 C
Dissipation (CM): 0.45W (85 C)
(DP): 0.50W (85 C)

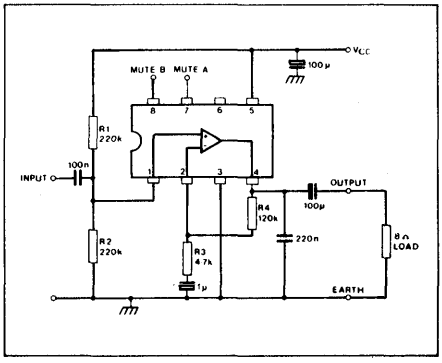


Fig. 3 SL6310C test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage Vcc: 4.5V to 13V
Ambient temperature: −30°C to +85°C
Mute facility: Pins 7 and 8 open circuit

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	Vcc = 9V
Supply current muted (A)		0.55	0.7	mA	Vcc = 9V, Pin 7 via 100k to earth
Supply current muted (B)		0.6	0.9	mA	Vcc = 9V, Pin 8 = Vcc
Input offset voltage		2	20	mV	Rs ≤ 10k
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	μA	
Voltage gain	40	70		dB	Vcc = 9V
Input voltage range	1.5	2.1		V	Vcc = 4.5V
	10	10.6		V	Vcc = 13V
CMRR	40	60		dB	Rs ≤ 10k
Output power	400	500		mW	Vcc = 9V, R_L = 8Ω
THD		0.4	3	%	P_{OUT} = 400mW, Vcc = 9V, Gain = 28dB

NOTE
1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage

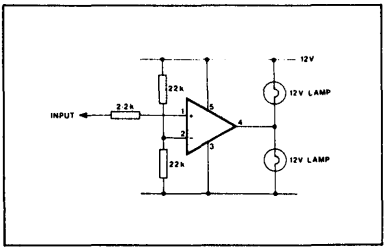


Fig. 4 SL6310C lamp driver

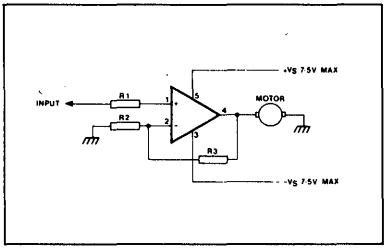


Fig. 5 SL6310C servo amplifier

OPERATING NOTES

Mute facility
The SL6310C has two mute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within one volt of Vcc (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310C is muted.

Mute control 'B', pin 8, is left open circuit or connected to a voltage less than 1 volt for normal operation: a voltage greater than 2.5V on pin 8 mutes the device. The input resistance at pin 8 is around 100kΩ and is suitable for interfacing with CMOS.

Only one mute control pin may be used at any time; the unused pin must be left open circuit.

Audio amplifier
As the SL6310C is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig. 3. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

The output and power supply decoupling capacitors have to carry currents of several hundred milliamps and should be rated accordingly.

Applications include hand-held radio equipment, hi-fi headphone amplifiers and line drivers.

Operational amplifier
It is impossible to list all their application possibilities in a single data sheet but the SL6310C offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig. 4) and servo amplifiers (Fig. 5).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring a high output current.

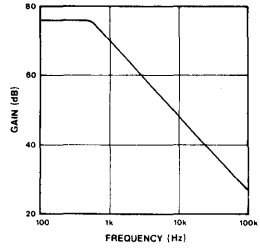


Fig. 6 Gain v frequency

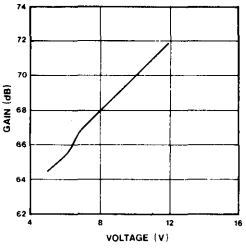


Fig. 7 Gain v. supply voltage

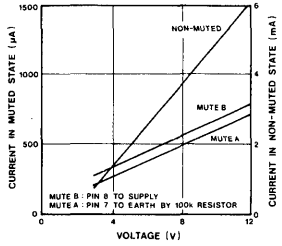


Fig. 8 Supply current v. supply voltage

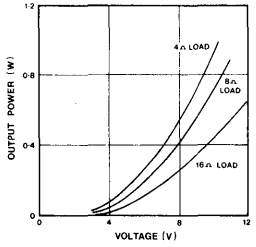


Fig. 9 Output power v. supply voltage at 5% (max) distortion

SL6440 A&C
HIGH LEVEL MIXER

The SL6440 is a high level mixer for use in Radio Communications and in applications requireing linear mixer.

The SL6440A is packaged in 16 lead ceramic DIL (DG) and the SL6440C in 16 lead plastic DIL DP)).

FEATURES

- + 30dBm Intercept Point
- Low Noise
- + 15dBm Compression Point (1dB)
- –55 o C to + 122 o C Temperature Range
- Programmable Performance
- Programmable Gain

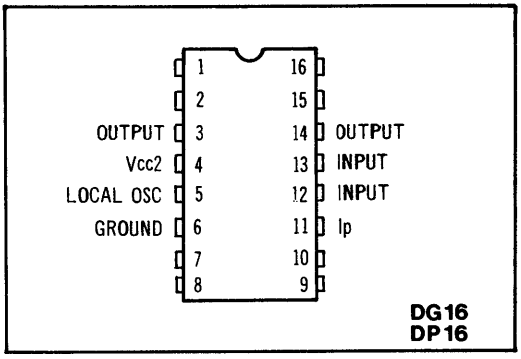


Fig. 1 Pin Connections

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Test circuit: Fig 2
Local oscillator input level 0dBm
Tamb = –55° C to +125° C (SL6440A)
–30° C to +85° C (SL6440C)
Vcc1 = 12V
Vcc2 = 10V
Ip = 25mA

ABSOLUTE MAXIMUM RATINGS

- Supply voltage, pins 3,4 and 14 15V
- Power dissipation (package limitation) 1200mW
- Derate above 25°C 8mW/° C
- Storage temperature range –65°C to + 150 °C
- Programme current 50mA

Characteristic	Value Min.	Value Typ.	Value Max.	Units	Conditions
Signal frequency 3dB point	100	150		MHz	
Oscillator frequency 3dB point	100	150		MHz	
Intercept point		+ 30		dBm	
Third order intermodulation distortion		– 60		dBm	Two 0dBm input
Second order intermodulation distortion		– 75		dB	Signals
1dBm compression point		15		dBm	Vcc1 = 15V
					Vcc2 = 12V
		12		dBm	Vcc1 = 12, Vcc2 10
Noise figure		11		dB	
Conversion gain		– 1		dB	50 Ω load fig. 2
Carrier leak to signal input	– 40			dB	Test circuit fig.11
Level of carrier at IF output		– 25		dBm	See applications information
Supply current		7		mA	Ip = 0
Supply current		60		mA	
Local oscillator input	100	250	500	mVrms	Ip = 35mA
Local oscillator input impedance		1.5		kΩ	
Signal input impedance		500		Ω	Single ended
		1000		Ω	Differential

PACKAGE THERMAL DATA

■ Chip to ambient	125 °C/W
■ Chip to case	40 °C/W
■ Time constant	1.9minutes
■ Max. chip temperature	170° C

CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the Ip pin (11). The total current programmed in the mixer and flowing into the output pins (3, 14), is twice the value programmed in on Pin 11.

The outputs pins are open collector outputs so that the conversion gain and output loads can be chosen for the specfic application.

The device has a separate supply (Vcc2) for the oscillator buffer on pin 4. Since the outputs are open collectors they should be returned to a supply Vcc1 through a load.

The choice of Vcc1 is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing unnecessarily. If the voltage on pins 3 and 14 is always greater than Vcc2 the outputs will not saturate, as the output frequency response will reduce near saturation.

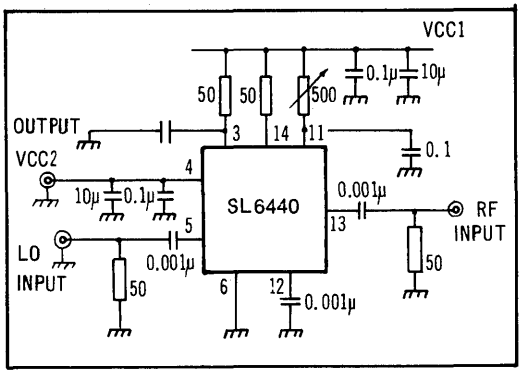


Fig. 2 Typical application and test circuit

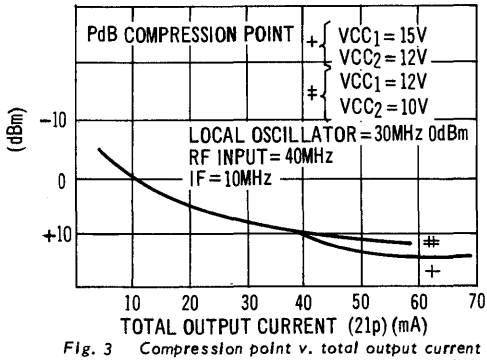


Fig. 3 Compression point v. total output current

Minimum V_{cc1} $(I_p \times RL) + V_s + V_{cc2}$

where I_p = programmed current
RL = DC load resistance
Vs = max signal swing at output

if the signal swing is not known:
minimum Vcc1 = 2(Ip x RL) +Vcc2

In this case the signal will be limiting at the input before the output saturates.

The current (Ip) programmed into pin 11 can be supplied via a resistor from Vcc 1 or from a current source.

The conversion gain is equal to

$$GdB = 20\text{Log}\frac{RL\ Ip}{56.6\ Ip + 0.0785}$$ for single-ended output

$$GdB\ 20\ \text{Log}\frac{2\ RL\ Ip}{56.6\ Ip + 0.0785}$$ for differential output

Device dissipation is calculated using the formula

mW diss = 2Ip Vo + Vp Ip + Vcc2 Diss
where Vo = voltage on pin 3 or pin 14
Vp = voltage on pin 11
Ip = programming current (mA)
Vcc2 Diss = dissipation obtained from graph (Fig.9)

As an example Fig. 10 shows typical dissipation assuming Vcc1 and Vo are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig. 4 shows the intermodulation performance against Ip. The curves are independent of Vcc1 and Vcc2 but if Vcc1 becomes too low the output signal swing cannot be accommodated, and if Vcc2 becomes too low the circuit will not provide enough drive to sink the programmed current.

Examples of performance at various supply voltages are shown below.

The SL6440 can be used with differential or single ended inputs and outputs. A balanced input will give better carrier leak. Fig. 5,6 and 7 show the performance with various input configurations. The high input impedance allows step-up transformers to be used if desired, whilst high output impedance allows a choice of output impedance and conversion gain.

Fig. 2 shows the simplest application circuit. The input and output are single ended and Ip is supplied from Vcc1 via a resistor. Increasing RL will increase the conversion gain, care being taken to choose a suitable value Vcc1.

Fig. 11 shows an application with balanced input from improved carrier leak, and balanced output for increased conversion gain. A lower Vcc1 giving lower device disssipation can be used with this arrangement.

Further Applications information is available.

(AN1007 and AN1009)

Decide on input configuration using local
llator data. If using transformer on input,
de on ratio from noise considerations.
Decide on output configuration and value of
'ersion gain required.
Decide on value of Ip and Vcc2 using inter–
ılation and compression point graphs.
Using values of conversion gain, Vcc2, load
lready chosen, decide on value of Vcc1.
Calculate device dissipation and decide
:her head sink is required from maximum opera–
temperature considerations.

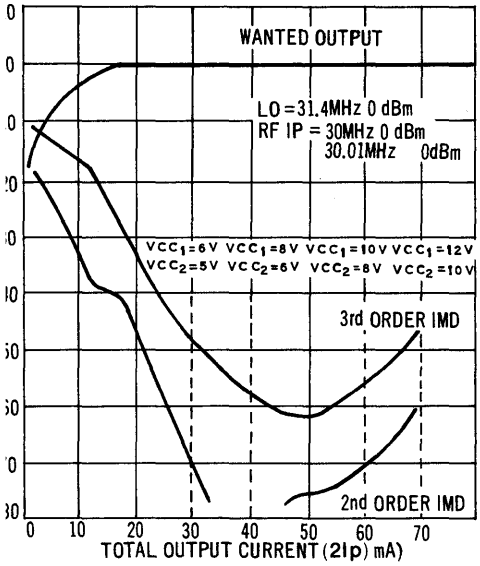


Fig.4 Intermodulation v. total output (average composite readings)

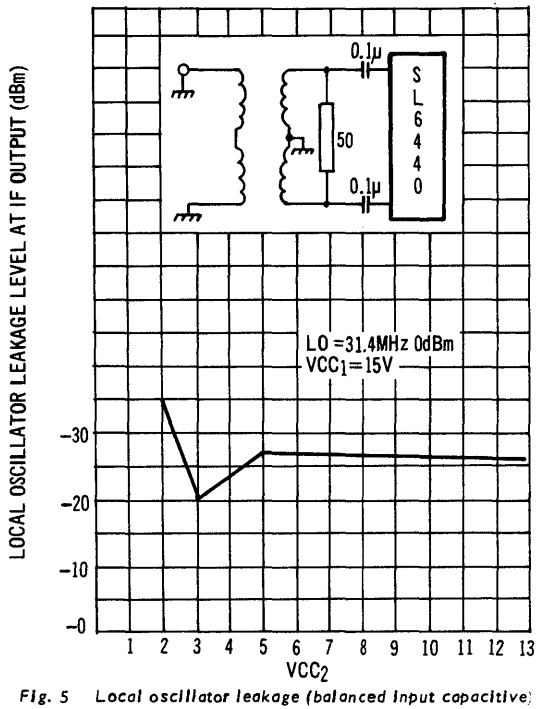


Fig. 5 Local oscillator leakage (balanced input capacitive)

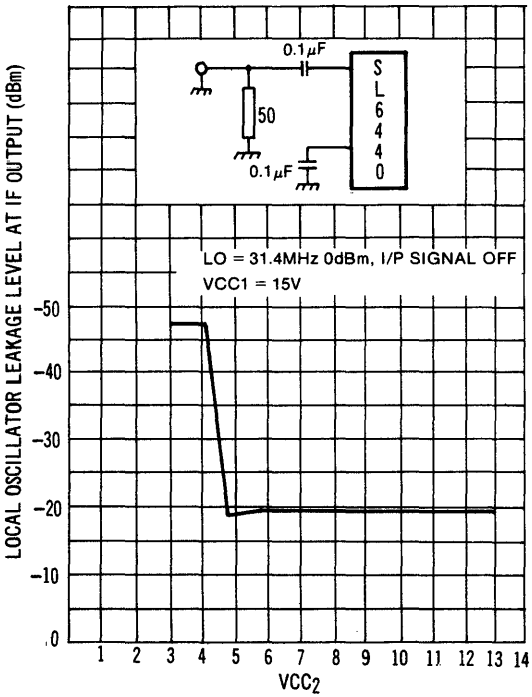


Fig. 6 Local oscillator leakage level at IF output (single ended input)

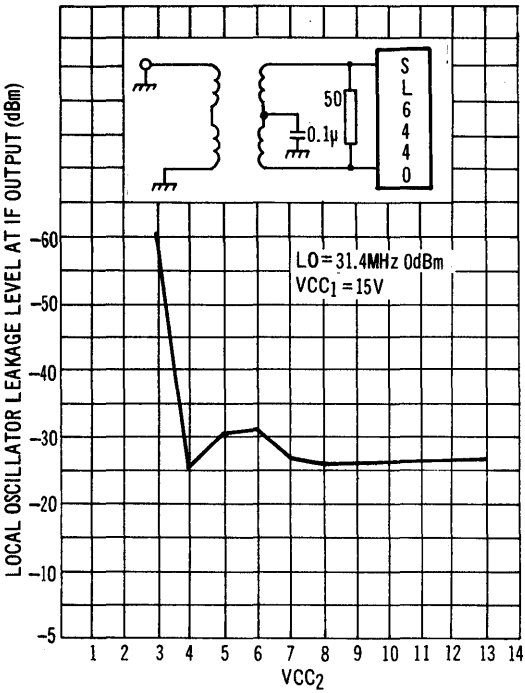


Fig. 7 Local oscillator leakage level at IF output (balanced input direct coupling)

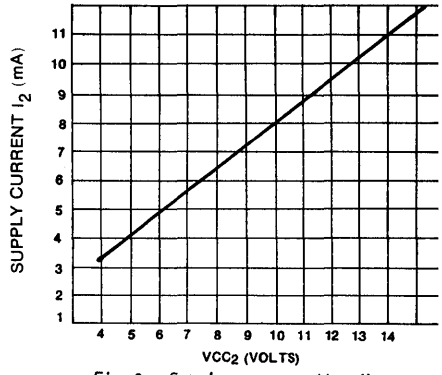


Fig. 9 Supply current v. Vcc2(Ip=0)

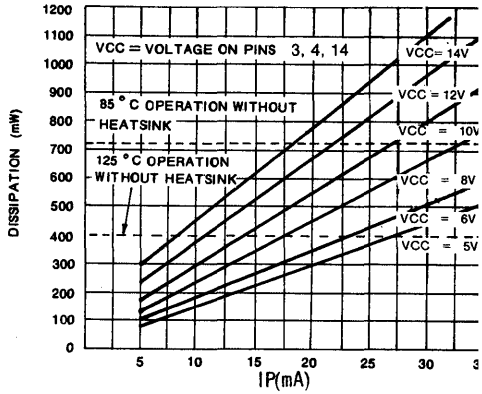


Fig. 10 Device dissipation v. Ip

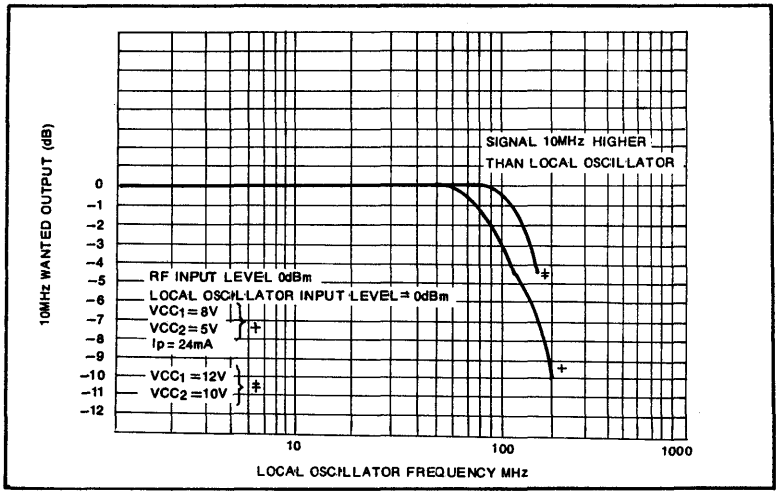


Fig. 8 Frequency response at constant output IF

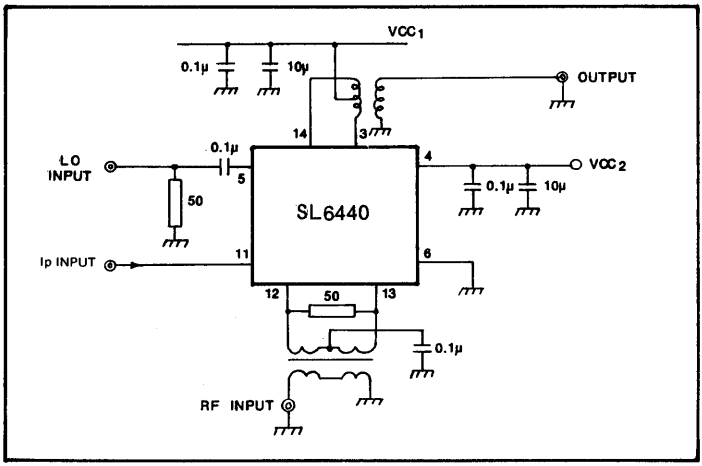


Fig. 11 Typical application circuit

PLESSEY
SEMICONDUCTORS
1641 Kaiser Avenue
Irvine, CA. 92714

SL6000 SERIES
COMMUNICATIONS CIRCUITS

SL6600C
LOW POWER IF/AF PLL CIRCUIT FOR NARROW BAND FM

The SL6600 is a single or double conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits the SL6600 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with a second IF frequency of less than 1MHz. Normally the SL6600 will be fed with a first IF signal of 10.7 or 21.4MHz; there is a crystal oscillator and mixer for conversion to the second IF amplifier, a PLL detector and squelch system.

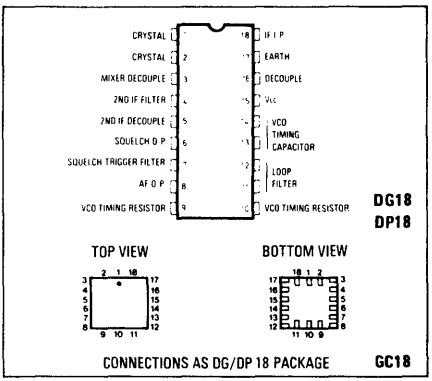


Fig. 1 Pin connections

FEATURES

- High Sensitivity: 5 μV minimum
- Low Power: 1.5mA typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 50dB S/N Ratio

APPLICATIONS

- Low Power NBFM Receivers

QUICK REFERENCE DATA

- Supply Voltage 7V ± 0.5V
- Input Dynamic Range 100dB min.

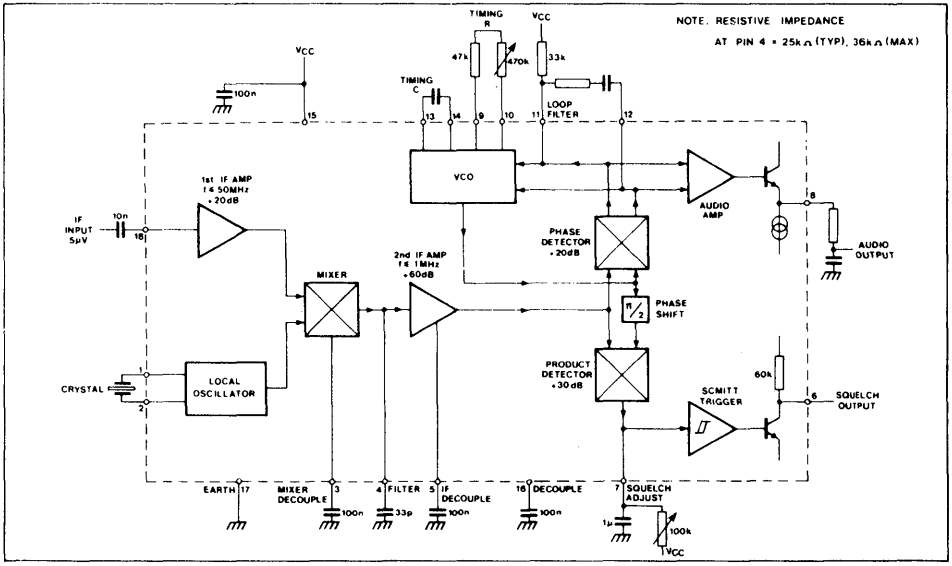


Fig. 2 SL6600 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} : 7V ±0.5V
Input signal frequency: 10.7MHz, frequency modulated with a 1 kHz tone with ±1.5kHz frequency deviation.
Ambient temperature: −30°C to +85°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		1.5	2.5	mA	
First IF input impedance		910		Ω	
Input dynamic range	100	120		dB	1dB change in AF output
Maximum input level	2			V rms	
Input sensitivity	5	3		µV rms	50 Ω source, S + N/N = 20dB
Audio output	20	50	80	mV rms	1mV rms input level
Audio THD		1.3	3	%	1mV rms input level
S + N/N	30	50		dB	1mV rms input level
AM rejection	30	40		dB	30% AM, 100µV rms Input
Squelch low level	0	0.2	0.5	V	20µV rms input
Squelch high level	V_{CC}−0.5	V_{CC}−0.1	V_{CC}	V	No input
Squelch hysteresis		2		dB	

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6600 can be operated either as a single conversion circuit with a maximum recommended input frequency of 800kHz or in a double conversion mode with a first IF of the input frequency (50 MHz max.) and a second IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IF's; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 25MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used.

When a single conversion circuit is required a 6.8k resistor should be connected in place of the crystal and a further 2.7k resistor connected between pin 1 and earth. The overall gain of the circuit will be reduced by 12dB with this technique.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz.

Phase Locked Loop.

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor according to the formula $\left(\frac{39}{f}\right)$pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine +10% frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 47k (recommended minimum value) increases the frequency by approx. 10%.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R_2 and capacitor C_1 must be calculated so that the natural loop frequency fn and damping factor ξ are suitable for the FM deviation and modulation bandwidth required. Values of 6.2kΩ and 2.2nF are recommended for ±5kHz maximum deviation and 3kHz audio bandwidth when the second IF frequency is 100kHz. These give fn = 20kHz, ξ = 0.707.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. This feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and Vcc to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10µF can be chosen to give the required characteristics.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7 kΩ and 4.7nF may be used.

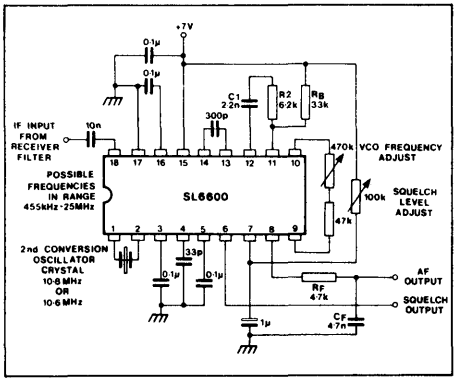
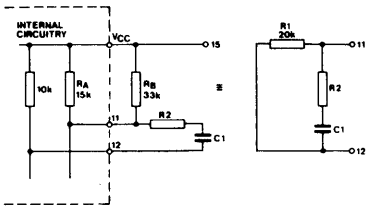


Fig.3 SL6600 application diagram (1stIF=10.7MHz, 2ndIF=100kHz



$K_o = 2.4f_o$ radians/volt-second
$K_D = 2.8$ volts/radian
f_o = 2nd IF frequency
f_n = natural loop frequency

From theory:

$$2\pi f_n = \left(\frac{K_o K_D}{\tau_1 + \tau_2}\right)^{\frac{1}{2}}$$

$$\text{Damping factor} = \xi = \tfrac{1}{2}\left(\frac{K_o K_D}{\tau_1 + \tau_2}\right)^{\frac{1}{2}}\left(\tau_2 + \frac{1}{K_o K_D}\right)$$

Fig. 4 Loop filter

TYPICAL CHARACTERISTICS

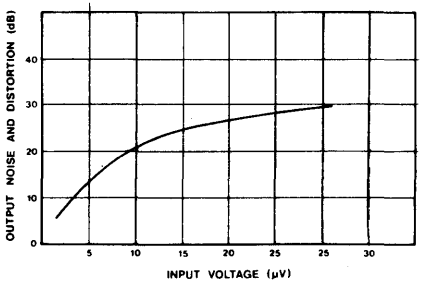


Fig. 5 Typical SINAD (Signal In/Noise & Distortion) Chacteristics

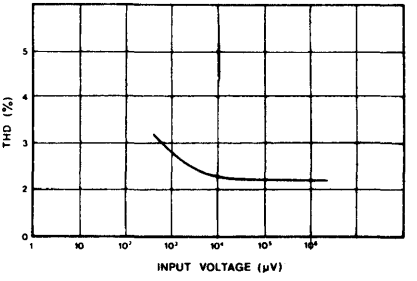


Fig. 6 Typical audio total harmonic distortion v. input signal voltage

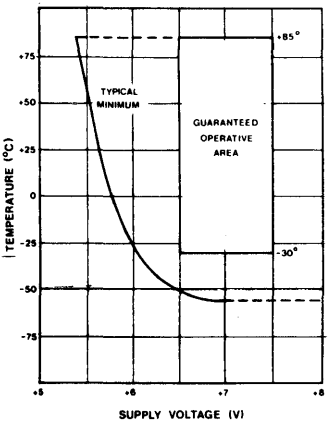


Fig. 7 Supply voltage v. temperature

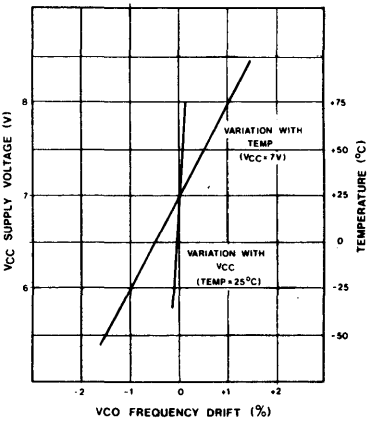


Fig. 8 Stability of VCO

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 9V
Storage temperature: −55°C to +150°C
Operating temperature: −55°C to +85°C

Plessey Semiconductors

SL6000 SERIES
COMMUNICATIONS CIRCUITS

SL6640/SL6650C
LOW POWER IF/AF CIRCUITS FOR NARROW BAND FM

The SL6640 and SL6650 independently perform the IF/AF function of a low power FM receiver. Each circuit is a complete IF strip and consists of a pre-amplifier, limiting amplifier, quadrature detector, carrier squelch, DC volume control and audio output stage. The SL6640 and SL6650 differ in that the SL6640 features a power audio output stage (typically 250mW into 8Ω) whilst the SL6650 has a level audio output which drives high impedance loads (open collector output). With the SL6640 the demodulator and audio amplifier are muted by the squelch output. The SL6650 squelch output does not internally mute the demodulator, which means that it can be used for tone decoding. If, on the SL6650, the squelch function is not required then, with some additional circuitry, (see Fig. 6) a signal strength meter can be incorporated.

APPLICATIONS

Mobile radio

Hand Held Radio

FEATURES

Low Power

Purpose Designed for narrow band

Carrier Squelch

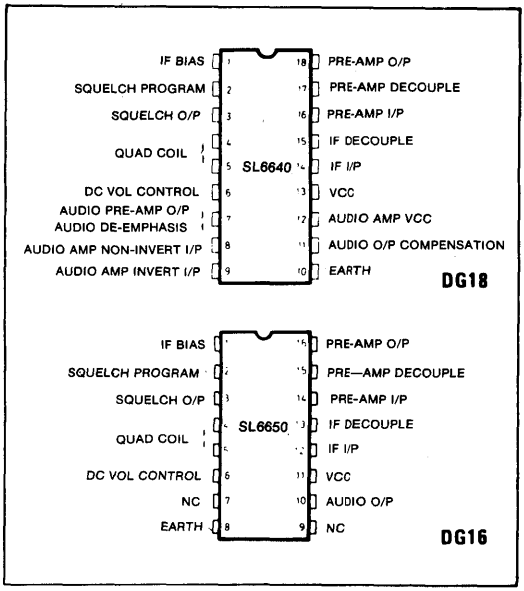


Fig. 1 Pin connections

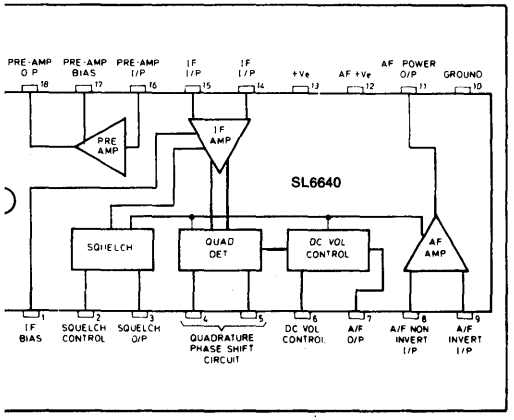


Fig. 2 SL6640 logic diagram

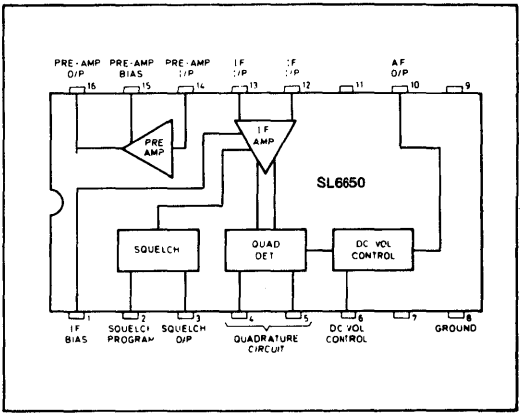


Fig. 3 SL6650 logic diagram

ELECTRICAL CHARACTERISTICS—SL6640

Test conditions (unless otherwise stated):
Supply voltage, V_{cc} = 6V
Ambient temperature, T_A = 22°C ± 2°C
IF = 10.7 MHz, Deviation = 5kHz (peak),
Modulating frequency = 1kHz

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4.5	6	12	V	
Supply current		3.5	6.0	mA	Muted
Supply current		10	13	mA	Unmuted
Pre-amp gain		46		dB	
Limiter gain		60		dB	
Combined 3dB bandwidth		25		MHz	
S/N ratio		50		dB	1mVrms input
Sensitivity	10			μV	20dB S/N
AM rejection		35		dB	1mVrms input 30% AM
Audio O/P power		250		mW	R_L = 8Ω
Distortion, THD			3	%	5%THD, 150mW O/P
Squelch range		45		dB	
Squelch law		2		μA/dB	
Squelch hysteresis		10		dB	Hysteresis resistor = 360kΩ
DC volume control range	50	70		dB	
DC volume control law		2		μA/dB	
Squelch O/P low level		1	1.5	V	100μVrms input
Squelch O/P high level	4.5	5		V	No input

ELECTRICAL CHARACTERISTICS—SL6650

As above except:

Supply current		6	9.5	mA	
Audio O/P level		25		mV RMS	1mVrms input, RL = 10 kΩ

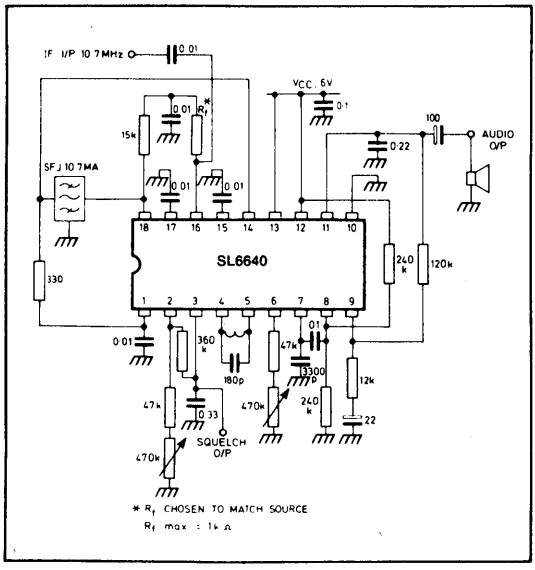


Fig. 4 SL6640 test circuit

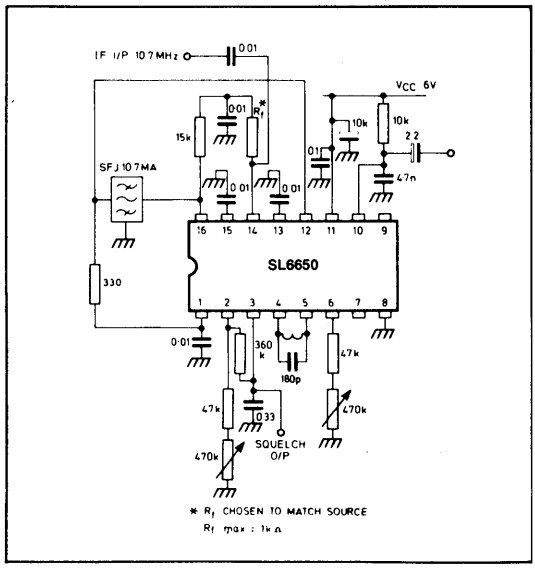


Fig. 5 SL6650 test circuit

²PLICATION NOTE

The detector characteristics depend upon the ıadrature circuitry used. The SL6640 and SL6650 ve been designed to permit the use of high-Q ıadrature circuits.

A quadrature circuit using a Q of approximately 0 can be made with an air cored coil of 25 turns SWG cotton covered wire on a neosid A7 former ıed by a trimmer.

J 10.7MA filters made by Murata (Distributed by doka, London).

3SOLUTE MAXIMUM RATINGS

ɔrage temperature range —55°C to +150°C
ɔerating temperature range —55°C to +85°C
pply voltage +14V

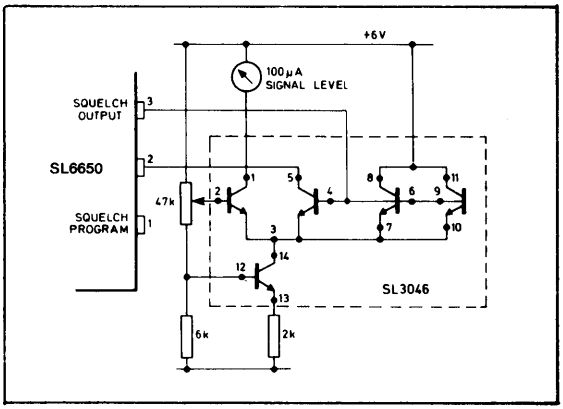


Fig. 6 Signal level meter application

SL6700C

IF AMPLIFIER AND AM DETECTOR

The SL6700C is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700 will be fed with a first IF signal of 10.7 or 21.4 MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable.

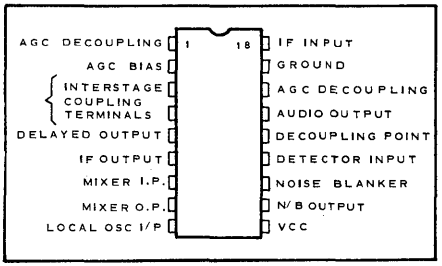


Fig. 1 Pin Connections

FEATURES

- High Sensetivity: 10 μV minimum
- Low Power: 8mA typied at 6v
- Linear Detector

APPLICATIONS

- Low Power AM Receivers

QUICK REFERENCE DATA

- Supply Voltage 4.5v
- Input Dynamic Range 100dB typ

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 7.5v
- Storage temperature:– –55 C to +125 C

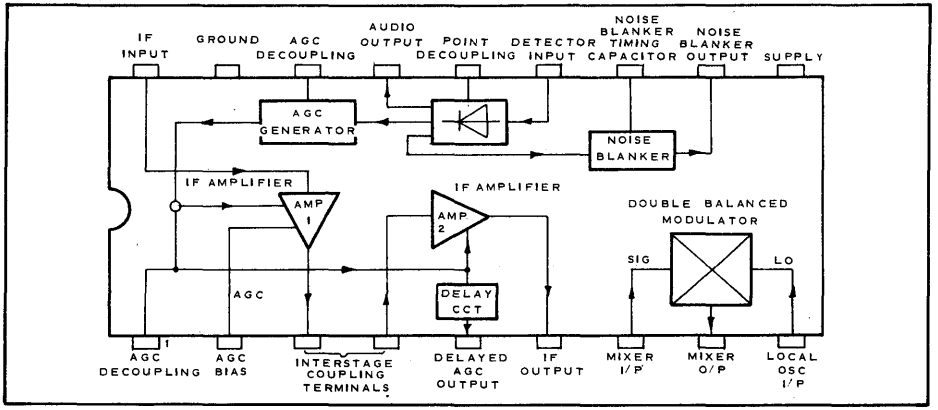


Fig. 2 SL6700 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage 4.5V
T amb −30° C to +85° C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Supply voltage	3		7	V	Optimum performance at 4.5V
Supply current		4.5	6	mA	
S/N ratio		40		dB	1mV I/P 80% mod @1kHz
TH distortion		1	5	%	1mV I/P 80% mod 1kHz
Sensitivity	10	5		μV	10dB S + N/N ratio, 30% mod 1kHz
Audio O/P level change		6		dB	10μV to 50mV I/P 80% mod 1kHz
AGC threshold		5		μV	
AGC range		80		dB	
AF O/P level		60		mV	
Delayed AGC threshold		10		mV rms	80% mod
Dynamic range		100		dB	Noise floor to overload
IF frequency response		50		MHz	3dB gain reduction
IF amplifier gain		50		dB	10.7MHz
Detector gain		46		dB	455kHz 80% AM 1kHz
Detector Z_{IN} Pin 13		4		kΩ	
IF amplifier Z_{IN} Pin 18		3		kΩ	
Noise blank level	2.7			V	Logic 1
			0.6	V	Logic 0
Noise blank duration		300		μs	C Pin 12 30nF
Mixer conversion gain		1.2R		kΩ	R is load resistor in kΩ
Mixer Z_{IN} (Signal)		3		kΩ	
Mixer Z_{IN} (L.O.)		5		kΩ	
Mixer L.O. injection	20	50	70	mV rms	fc = 10.245 MHz
Detector output voltage change	6	8		dB	1mV rms input, 1kHz modulation increased from 30% to 80%

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 300μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700C and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system. To keep the same sensitivity the mixer must be used as a linear amplifier by connecting a 20kΩ resistor between pin.9 and earth.

TYPICAL DC PIN VOLTAGES

(Supply 4.5V, Input 1 mV)

Pin	Voltage	Pin	Voltage
1	0.25V	10	4.5V
2	0.09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

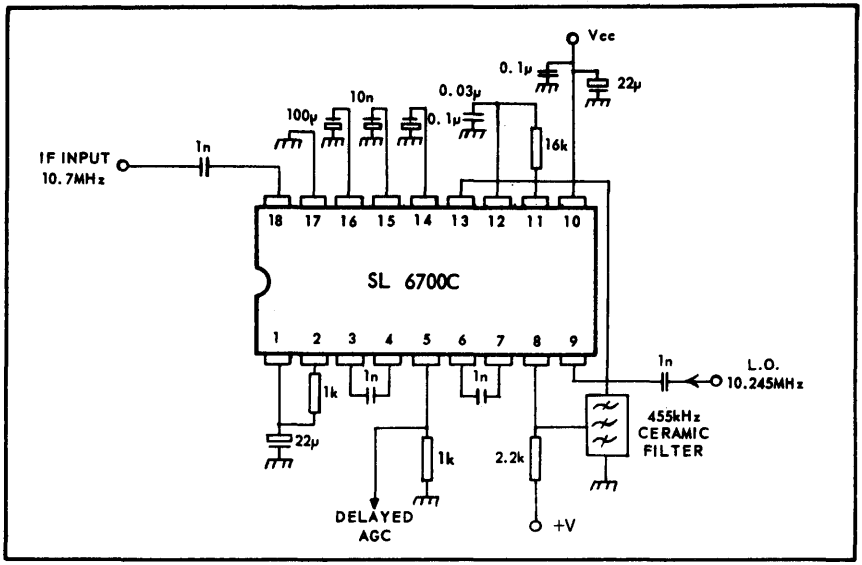


Fig. 3 SL6700 C AM double conversion receiver noise blanker

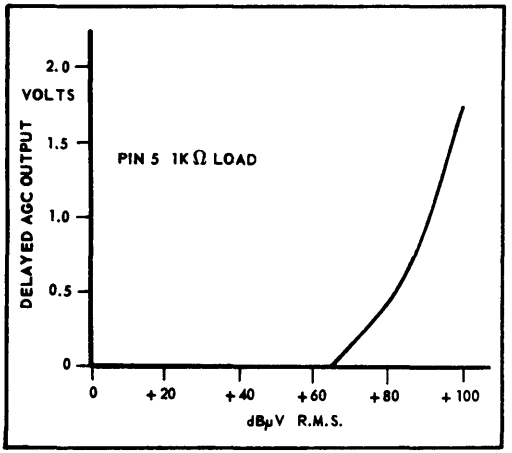


Fig. 4 Typied DAGC output variation with input signal (f= 10.7MHz, 30% modulation

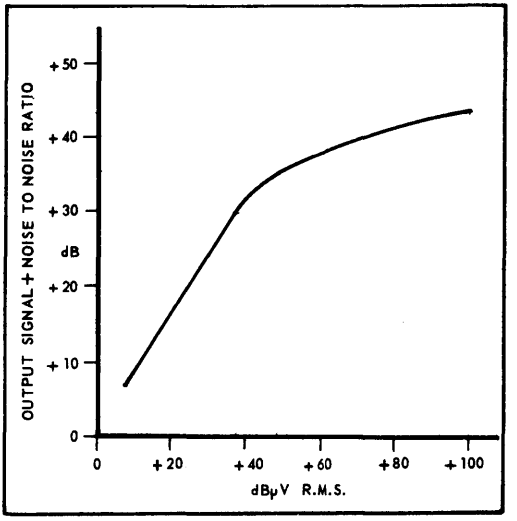


Fig 5 Typied Signal to Noise ratio $\left(\frac{S-N}{N}\right)$ *with input signal (f=10.7MHz, 30% modulation)*

PLESSEY
Semiconductors

SP9000 SERIES
DATA CONVERSION PRODUCTS

SP 9685
ULTRA FAST COMPARATOR

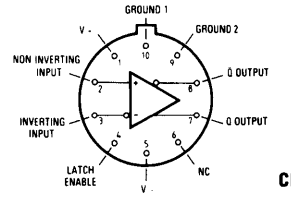
SP 9687
ULTRA FAST DUAL COMPARATOR

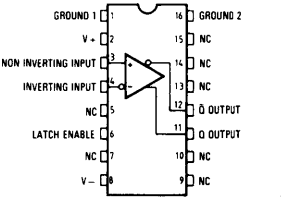
The SP 9685 is an ultra-fast comparator, and the SP 9687 is an ultra-fast dual comparator, both manufactured with a high performance bipolar process which makes possible very short propagation delays 2.2 nS typ ./ 2.7 nS typ. respectively. The circuits have differential inputs and complementary outputs fully compatible with ECL logic levels. The output currents capability are adequate for driving 50 ohm terminated transmission lines. The high resolution available makes the devices ideally suited to analogue-to-digital signal processing applications.

With the SP 9685 a latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used the latch enable may be connected to ground.

With the SP 9687 a latch function is provided to allow the comparator to operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If $\overline{LE}$ is high, and $\overline{LE}$ is low, the comparator function is in operation. When $\overline{LE}$ is driven low and $\overline{LE}$ high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, $\overline{LE}$ Must be connected to ground.

Both devices are compatible with the AM 685/AM 687 respectively but operate from conventional +5V and−5.2V rails.





On metal package, pin 5 is connected to case. On DIP pin 8 is connected to case

Fig. 1 Pin connections

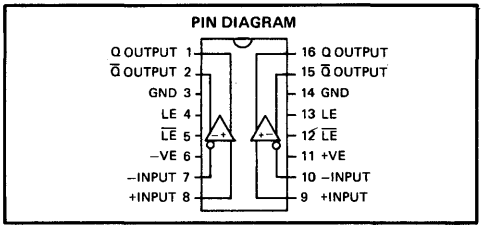
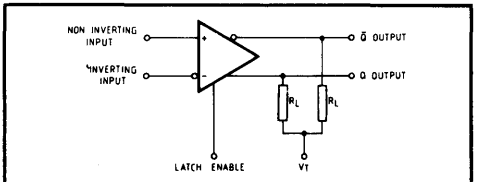


Fig. 1A



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200Ω connected to −2.0V or 200–2000Ω connected to −5.2V

SP 9685 is a dual without Latch enable.

Fig. 2 Functional diagram

FEATURES

- Propagation Delay 2.2 ns typ/2.7 ns typ respectively.
- Latch Set-up Time 1 ns max./0.5 ns typ
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM 685/687 but faster

QUICK REFERENCE DATA

- Supply voltages +5V, −5.2V
- Operating tempurature range −30°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	6V
Negative supply voltage	−6V
Output current	30mA
Input voltage	±5V
Differential input voltage	±5V
Power dissipation	500mW
Storage	−55° to 150°C
Lead temperature (soldering 60 sec)	300°

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = 25°C
V_{CC} = +5.0V ±.25V
V_{EE} = −5.2V ±.25V
R_L = 50 Ω

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Input offset voltage	Both	−5		+5	mV	Rs 100 ohms
Input bias current	Both		10	20	uA	
Input offset current	Both			5	uA	
Supply Currents Icc	SP 9685		19	23	mA	
IEE			23	34	mA	
	SP 9687		30		mA	
			54		mA	
Total Power Dissipation	SP 9685		210	300	mW	
	SP 9687		430		mW	Nominal Conditions
Min. Latch Set-up Time	SP 9685		0.5	1	ns	
	SP 9687		0.5		ns	
Input to Q Output Delay	SP 9685		2.2	3	ns	
	SP 9687		2.7	4	ns	
Input to $\overline{Q}$ Output Delay	SP 9685		2.2	3	ns	
	SP 9687		2.7	4	ns	100 mV pulse
Latch to Q delay	SP 9685		2.5	3	ns	10 mV Overdrive
	SP 9687		2.7	4	ns	
Latch to $\overline{Q}$ delay	SP 9685		2.5	3	ns	
	SP 9687		2.7	4	ns	
Min. latch pulse width	Both		2	3	ns	
Min. hold time	Both			1	ns	
Common Mode Range	Both	−2.5		+2.5	V	
Input Capacitance	Both		3		pF	
Input Resistance	Both	60			K ohms	
Output Logic Levels						
Output High	Both	−.96		−.81	V	At Nominal Supply
Output Low	Both	−1.85		−1.65	V	Voltages.
Common Mode Rejection Ratio	Both	80			dB	See Fig. 4
Supply Voltage Rejection Ratio	Both	60			dB	

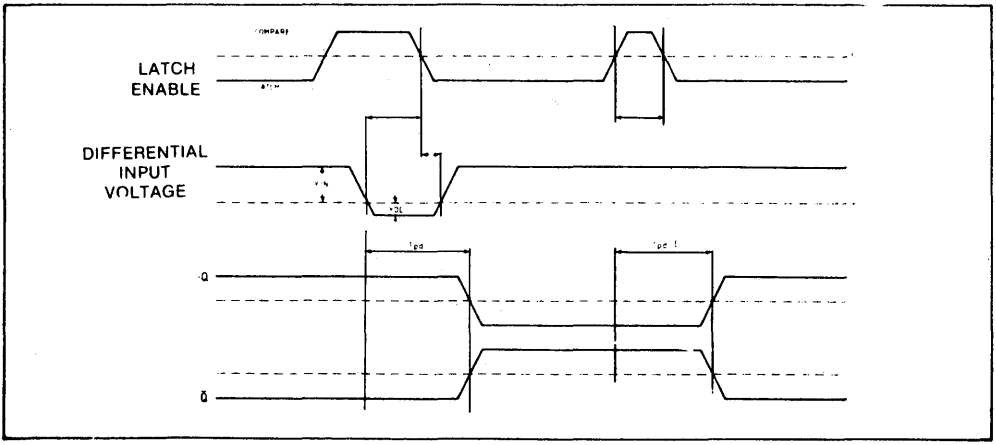


Fig. 3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse, switches the comparator over after a time tpd. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse with $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Definition of terms

Vos Input offset voltage – The potential difference required between the input terminals to obtain zero output potential difference.

Ios Input offset current – The difference between

the currents into the inputs when there is zero potential difference between the outputs.

I_B Input bias currents - The average of the two input currents. I_B is a chip design trade-off parameter; externally, it is desirable to have I_B as low as possible, while internally, circuit performance requirements demand higher I_B.

R_{IN} Input resistance - The resistance looking into either input with the other grounded.

C_{IN} Input capacitance - The capacitance looking into either input pin with the other grounded.

Switching terms (refer to Fig. 3)

t_{pd+} Input to output high delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} Input to output low delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ Latch enable to output high delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ Latch enable to output low delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transistion to the 50% point of an output HIGH to LOW transition.

t_s Minimum set-up time – The minimum time before the negative transition of the latch enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h The minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ Minimum latch enable pulse width – The minimum time that the latch enable signal must be HIGH in order to acquire and hold an input signal change.

V_{CM} Input voltage range – The range of input voltages for which the offset and propagation delay specifications are valid.

CMRR Common mode rejection ratio – The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Latched and unlatched gain

The gain of a high speed, high gain comparator is difficult to measure, because of input noise and the possibility of oscillations when in the linear region. For a full ECL output level swing, the unlatched input shift required is approximately 1mV. In the latched mode, the feedback action in effect enhances the gain and the limitation in the noise/oscillation level; under these conditions the usable resolution is 100μV, although this is only achieved by careful circuit design and layout.

Interconnection techniques

High speed components in general need special precautions in circuit board design to achieve optimum system performance. The SP 9685/SP9687, with around 50 dB gain at 200MHz, should be provided with a ground plane having a low inductance ground return. All lead lengths should be as short as possible, and RF decoupling capacitors should be mounted close to the supply pins. In most applications, it will be found to be necessary to solder the device directly into the circuit board. The output lines should be designed as microstrip transmission lines backed by the ground plane with a characteristic impedance between 50Ω and 150Ω. Terminations to −2V, or Thevenin equivalents, should be used.

Measurement of propagation and latch delays

A simple test circuit is shown in Figure 4. The operating sequence is:

1. Power up and apply input and latch signals. Input 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

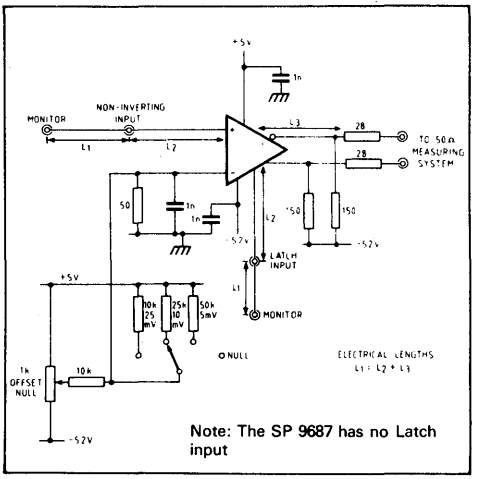


Fig. 4 SP9685/9687 test circuit

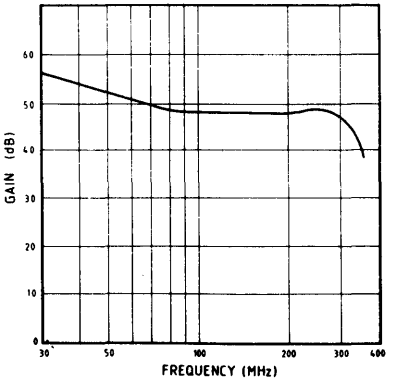


Fig. 5 Open loop gain as a function of frequency

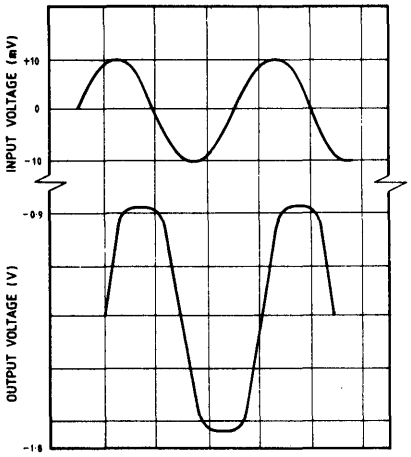


Fig. 6 Response to a 100MHz sine wave

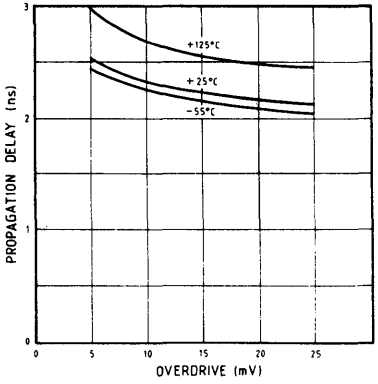


Fig. 7 Propagation delay, latch to output as a function of overdrive

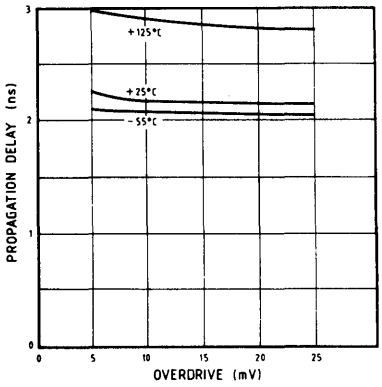


Fig. 8 Propagation delay, input to output as a function overdrive

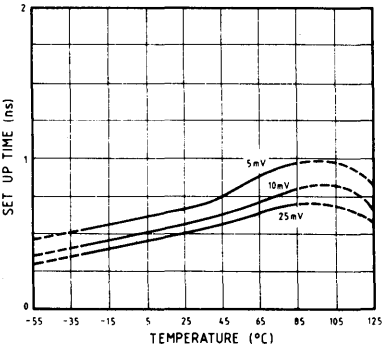


Fig. 9 Set-up time as a function of temperature

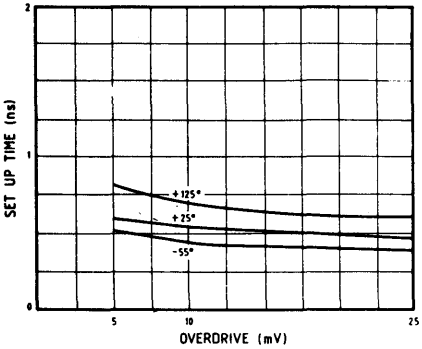


Fig. 10 Set-up time as a function of input overdrive

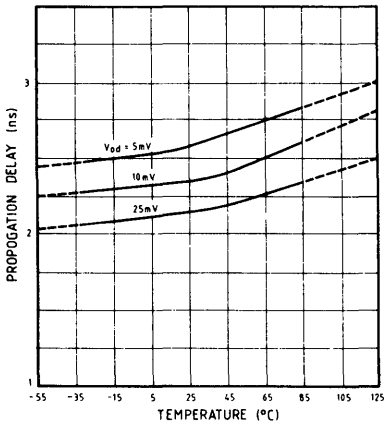


Fig. 11 Propagation delay, input to output as a function of temperature

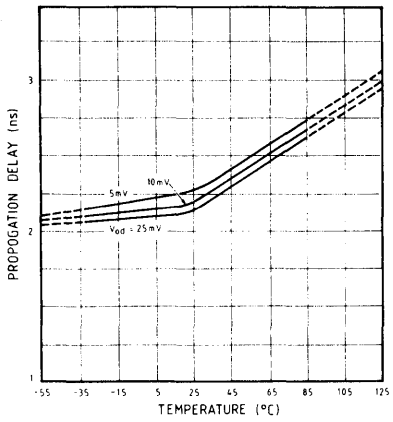


Fig. 12 Propagation delay, latch to output as a function of temperature

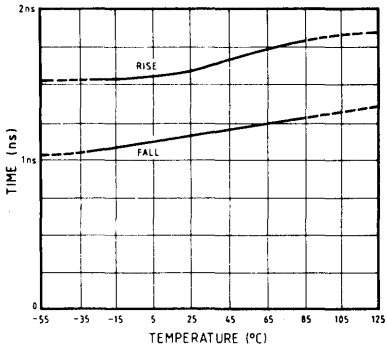


Fig. 13 Output rise and fall times as a function of temperature

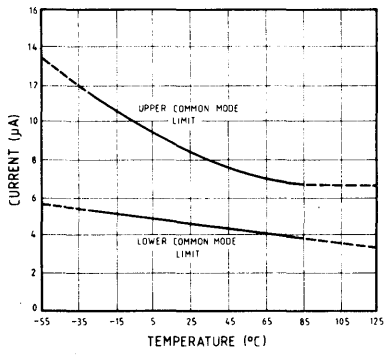


Fig. 14 Input bias currents as a function of temperature

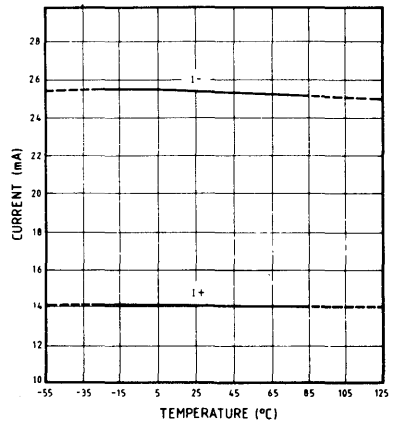


Fig. 15 Supply current as a function of temperature

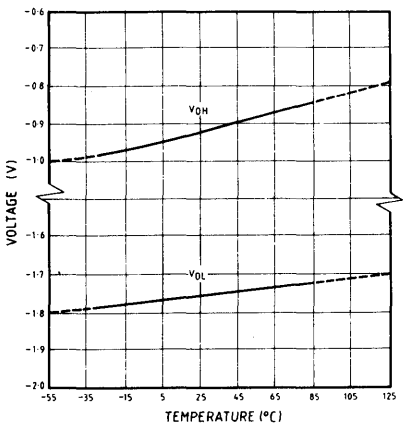


Fig. 16 Output levels as a function of temperature

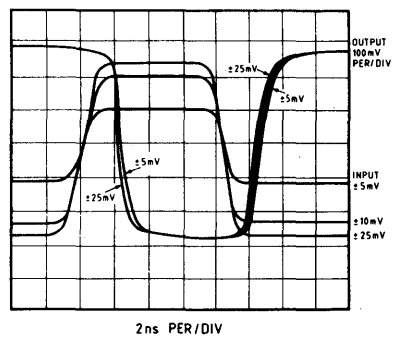


Fig. 17 Response to various input signal levels

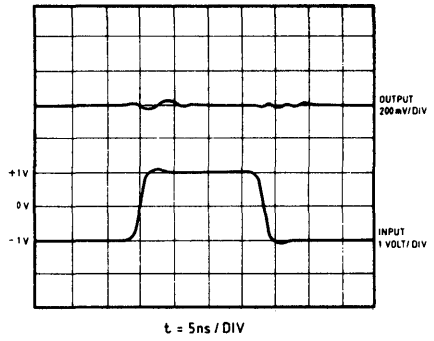


Fig. 18 Common mode pulse response

SP9750

HIGH SPEED COMPARATOR

The SP9750 is a high speed comparator with a latch circuit and other facilities intended for use in the construction of fast A–D converter systems. The speed capability of the device is compatible with conversion rates of up to 100 Mega-samples per second. Input and output logic levels are ECL compatible.

FEATURES

- Latch Set-up Time 2ns Max.
- Max. Input Offset Voltage 5mV
- Propagation Delay 3ns (Typ.)
- ECL Compatible
- Comparator Output Gating
- Wired OR Decoding for 4 Bits
- Current Output Settling to 0.2% in 8ns

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	–5.5V
Reference supply voltage	–8.5V
Reference current output	15 mA
Input voltage	±4V
Differential input voltage	±6V
Power dissipation	500 mW
Operating temperature range	–30°C to +85°C
Storage temperature range	–65°C to +150°C
Lead temperature (soldering 30 sec)	300°C

Logic input voltages to gate and latch V_{EE} to 0

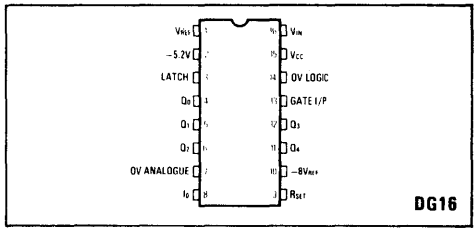


Fig. 1 Pin connections

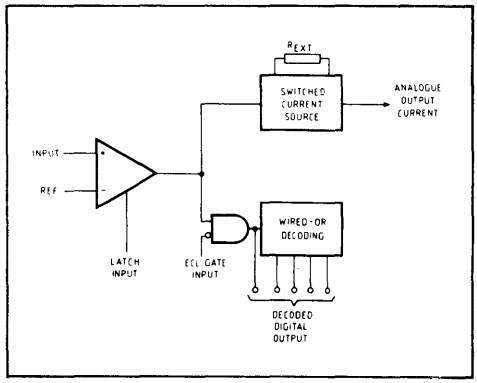
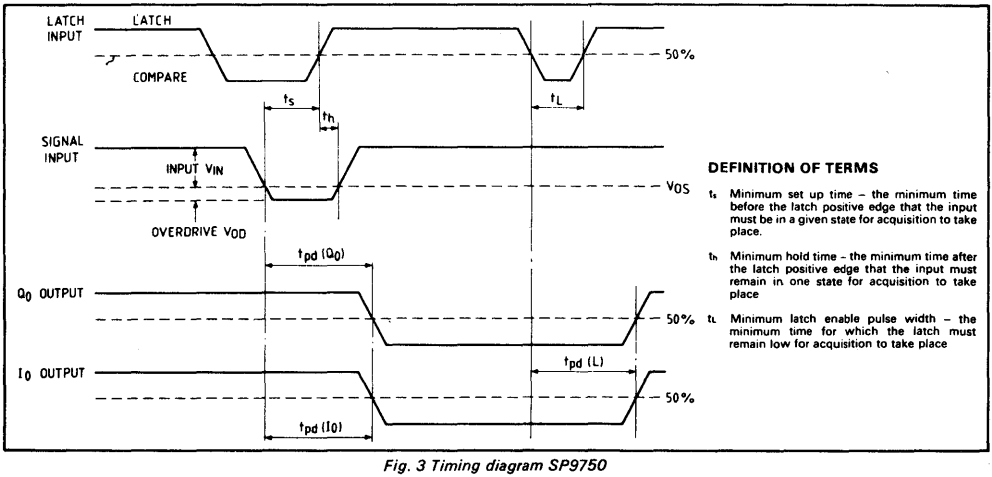


Fig. 2 Block diagram of SP9750



DEFINITION OF TERMS

t_s Minimum set up time – the minimum time before the latch positive edge that the input must be in a given state for acquisition to take place.

t_h Minimum hold time – the minimum time after the latch positive edge that the input must remain in one state for acquisition to take place

t_L Minimum latch enable pulse width – the minimum time for which the latch must remain low for acquisition to take place

Fig. 3 Timing diagram SP9750

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = +25°C
V_{CC} = +5V ±0.25V
V_{EE} = −5.2V ±0.25V
V_{REF} = −8V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−5		+5	mV	
Input bias current			25	µA	
Input offset current			5	µA	
Supply currents Vcc		16	20	mA	
V_{EE}		35	42	mA	
V_{REF}		14	18	mA	
Total power dissipation		390	470	mW	
Analogue O/P current 'on'		5		mA	See operating note 1
Analogue O/P current 'off'			5	µA	+5V on pin 8
Precision current stability		20		ppm/°C	Also depends on R_{EXT}
Min. latch set-up time (t_s)			2	ns	See operating note 2
Input to Q_o O/P delay (tpd (Q_o))		3	4.5	ns	V_{IN} = 100 mV, 25 mV over drive, 50Ω load
Input to I_o delay (tpd (I_o))		3	4.5	ns	on I_o to 0 volts (Note 3)
Delay gate input to Q_{1-4} high		1.5	2.5	ns	See operating note 4
Delay gate input to Q_{1-4} low		1.5	2.5	ns	
Latch to I_o (tpd (LI_o))					
between 50% points		3	4.5	ns	
to 1% settling		4	8	ns	See operating note 5
to 0.2% settling		8	12	ns	
Min. hold time t_h		1		ns	
Min. latch pulse width (t_L)		2		ns	
Common mode range	−2.5V		+2.5V	V	
Diff. mode range			5	V	
Node capacitance I_o		3.5		pf	
Node capacitance analogue input			3	pf	
Input resistance	60			KΩ	
Output logic levels					
Logic '1'	−.98		−0.78	V	Vcc = +5V, V_{EE} = −5.2V
Logic '0'	−1.85		−1.6	V	R_L = 220Ω to −2V

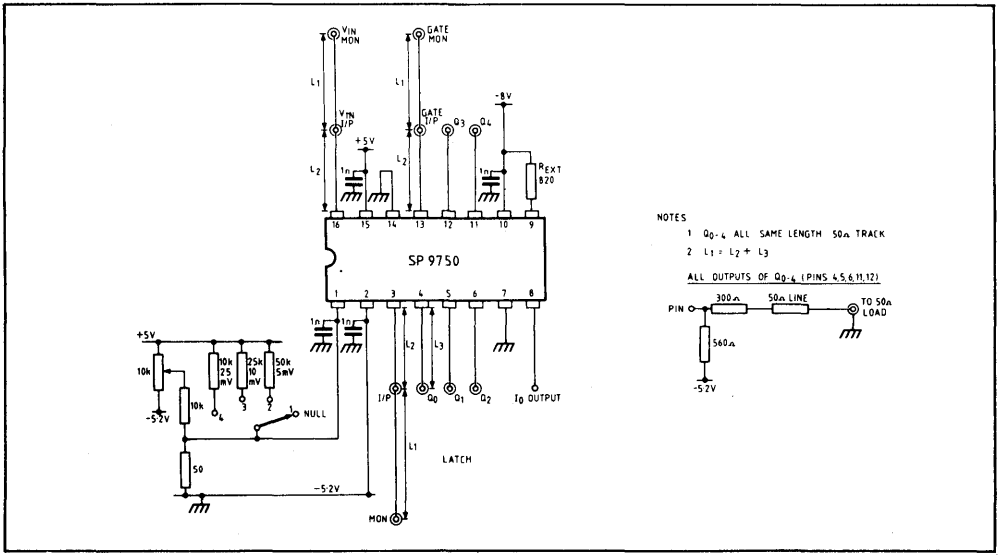


Fig. 4 Test circuit

GENERAL DESCRIPTION

The SP9750 is a fast comparator combined with a latch facility which allows the device to be operated in the sample and hold mode.

When the latch is 'low' the comparator is in the 'follow' mode, and when the latch is driven 'high' the output is locked in the existing state. The latch circuitry will therefore always produce a decision on the input state.

The comparator has a relatively low gain in the follow mode, which assists in achieving an extremely fast response. However, due to the positive feedback action of the latch function, the gain approaches infinity during the latch cycle, thereby ensuring high resolution.

In addition to the basic comparator, the following functions are provided on the chip to optimise the performance of high speed parallel-series-parallel A to D converter systems.

1. An ECL compatible gating function for simplified multi-comparator output logic.
2. Four emitter follower outputs from the gate to provide wired OR decoding for four bits.
3. A precision current source, set by an external resistor.
4. A high speed switch for the precision current to provide a fast and convenient reconstruction of the analogue input. Summing the currents in a multi-level comparator chain provides the D to A conversion directly for the construction of converters of the parallel-series-parallel type.

The philosophy adopted in the SP9750 makes possible the construction of ultra-fast, high accuracy parallel-series-parallel converters by integrating a significant portion of the system function on the same chip as the comparator. The result is not only to reduce considerably the total hardware count but to reduce the propagation delays where they are most critical, and eliminate redundant operations.

OPERATING NOTES

1. The analogue output current (Io) is set by means of an external setting resistor (R_{EXT}) and is equal to the reference voltage on Pin 9 (−8V nominal), divided by 2 x R_{EXT}. The accuracy of this reference voltage must be consistent with the conversion accuracy required. The output (Pin 8) compliance is −0.8V to +5.0 volts for correct operation.
2. This parameter is defined with +100 mV input and −10 mV overdrive, corrected to take account of the comparator offset, i.e. the switching threshold effectively is at OV on the input waveform. The relationship between setup time and overdrive is shown in Fig. 7c. The test circuit diagram, Fig. 4 indicates a method of performing this test.
3. Due to the relatively low gain of the comparator in the unlatched state, propagation measurements are defined with a 25 mV overdrive. The relationship between overdrive and delay is shown in Figs. 7a and 7b.
4. The gate input accepts an ECL drive. The outputs Q_1 to Q_4 are active when the gate input is at an ECL 'low' level, (−1.75V) and are switched by the internal circuitry. A 'high' gate input (− 0.9 V) switches the outputs to 'low', allowing the bussing of multiple devices onto the Q_1 – Q_4 rails.
5. Output settling times are measured at 10 mV overdrive conditions; larger overdrives produce shorter delays.
6. The test arrangement shown in Fig. 4 provides for a simple dynamic test of the SP9750 functions. When the switch is in position 1, the input offset voltage is nulled with the potentiometer, a condition detected by observing the output to be at the mid-point of its range (I_o or Q_o). The latch must be 'low' for this measurement. The offset voltage can be measured with a high impedance instrument. Positions 2, 3 and 4 provide increasing amounts of bias to the reference input corresponding to overdrives of 5mV, 10 mV, and 25 mV. For convenience of operation, the input analogue signal is referred to ground, and the reference input is set above ground, so that an input waveform which is positive going and referred to ground is all that is necessary. It should have an amplitude of (100 mV + overdrive voltage) and should have less than 5% overshoot. The risetime should be about 2 nS. Simple circuit modifications and a negative going signal would provide for inputs of opposite polarity. For accurate timing, the path length L_1 should be equal to L_2+L_3 properly terminated.

Static (DC) measurements can also be performed on the same test arrangement.

APPLICATIONS

Although the SP9750 was aimed at a particular system configuration it is sufficiently flexible to find application in a variety of conversion methods. In an all-parallel A–D converter, the SP9750 is capable of achieving sampling rates of up to 100 Megasamples per second. This technique is usable up to 5-bit accuracy. For higher bit accuracies, techniques such as the parallel-series method are required. Fig. 5 shows the schematic diagram of an A–D converter system capable of giving 8-bit accuracy at sampling rates of up to 30 Megasamples per second. The SP9750 is used in two 4-bit stages operating in the parallel-series-parallel mode. The analogue current output settling time from the first stage (an effective DAC facility) is dominated by the settling time of the one comparator which has the smallest overdrive. All other comparators have longer to settle, since the preceding sample and hold must be allowed to settle. For an 8-bit system, each comparator in the first 4-bit conversion has a weighting of 1/15 of full scale input. Therefore the settling band of interest for $\pm \frac{1}{2}$ L.S.B. is 2.9%. Typically the SP9750 settles to less than this, 1%, in four nanoseconds, illustrating the possibility of converter construction at higher speeds, or higher accuracies.

In order to achieve the optimum performance of this device, care must be taken to ensure that good layout practice is used, consistent with high frequency practice. A ground plane construction should be used and all leads should be designed to be microstrip transmission lines. The device should be soldered directly into the circuit board and the supplies decoupled with RF capacitors as close to each device as possible. In addition, to achieve the shortest possible settling time for the analogue current output, it is essential to keep the stray capacitance on Pin 9 (R_{SET}) to a minimum.

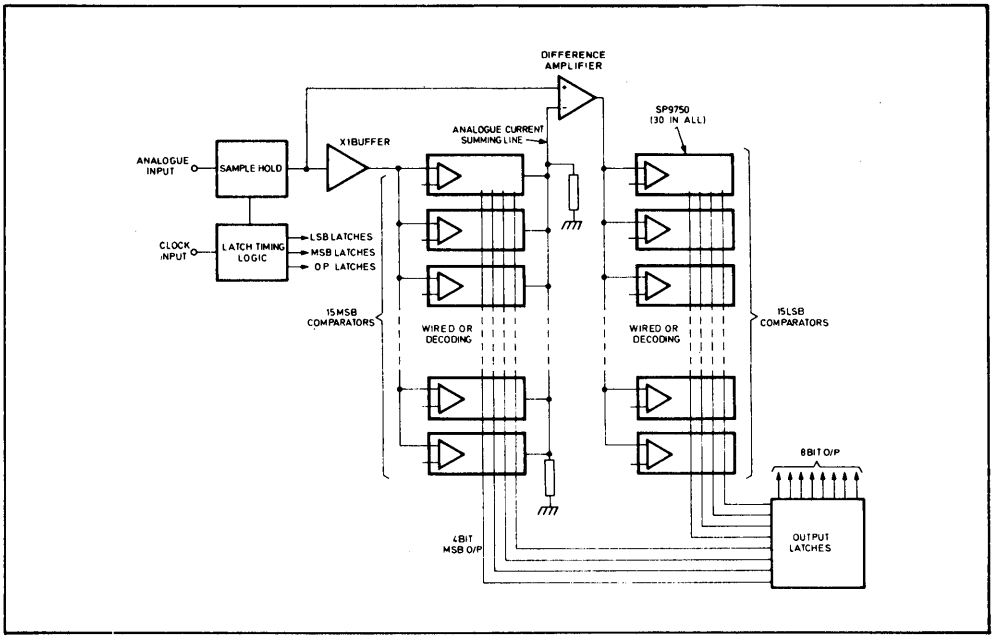


Fig. 5 Block diagram of a 4 x 4 bit parallel-series A/D converter

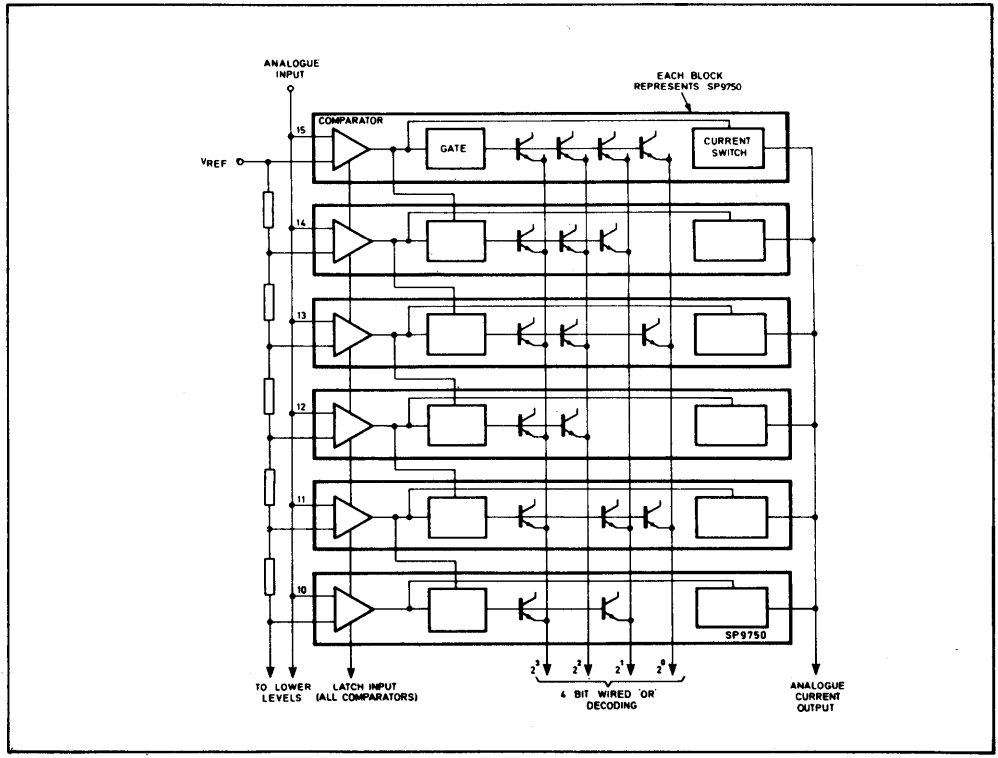


Fig. 6 Block diagram of 4-bit LSB stage showing top six levels

Fig. 7 Performance curves. Unless otherwise specified, standard conditions for all curves are $T_{AMB} = 25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.2V$, $V_{REF} = -8.0V$, I_O load $= 50\Omega$

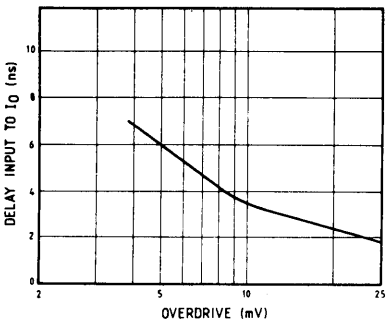


Fig. 7a input to 1_O output delay v. overdrive

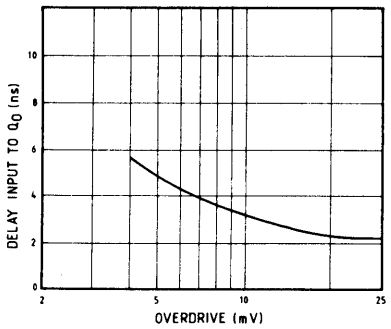


Fig. 7b Input to Q_O output delay v. overdrive

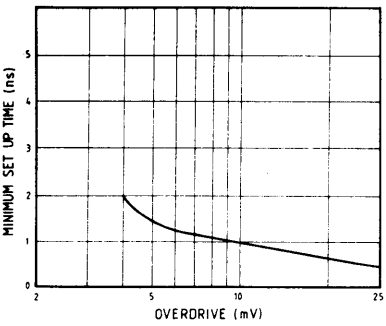


Fig. 7c T_S v. overdrive set-up time

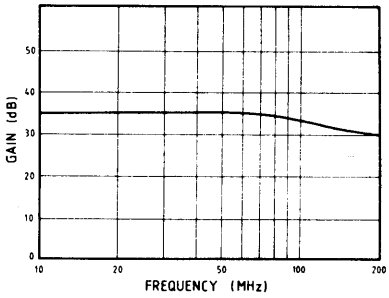


Fig. 7d Small signal gain v. frequency (to Q_O output). Latch input low.

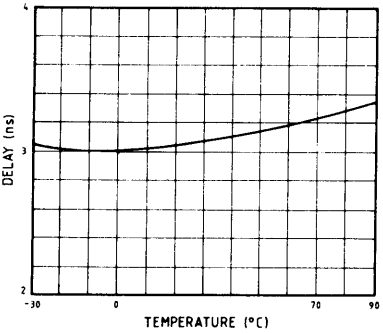


Fig. 7e Input to 1_O output delay as a function ot temperature

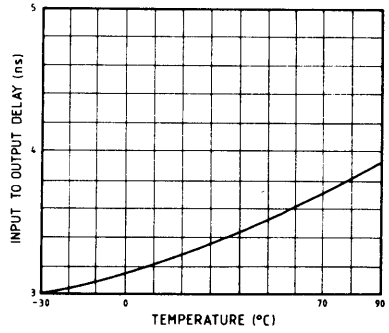


Fig. 7f Input to Q_O output delay as a function of temperature

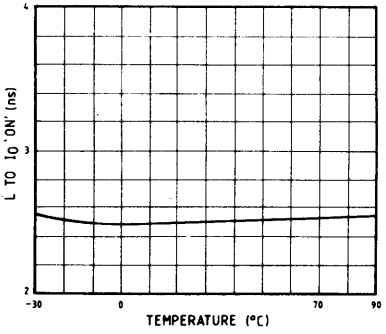


Fig. 7g Latch to I_O 'on' delay as a function of temperature

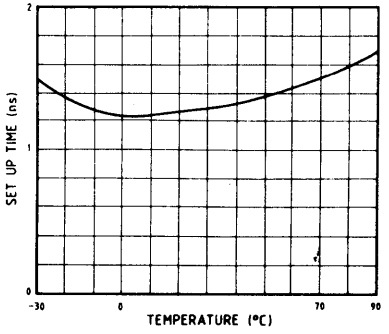


Fig. 7h Minimum set-up time as a function of temperature

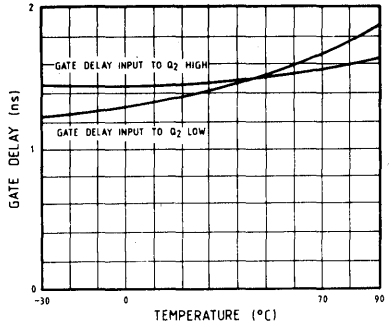


Fig. 7i Gate input to Q_1 – Q_4 delay variation with temperature

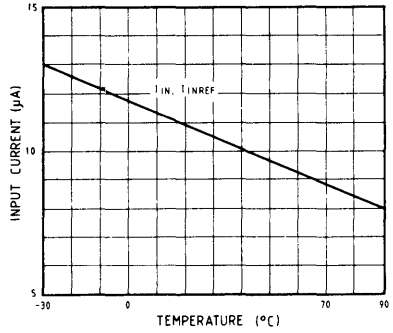


Fig. 7k Input current variation with temperature

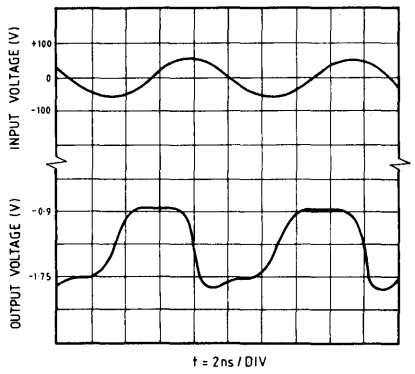


Fig. 7j Response to 100MHz sine wave

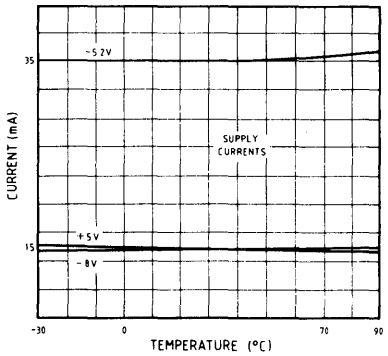
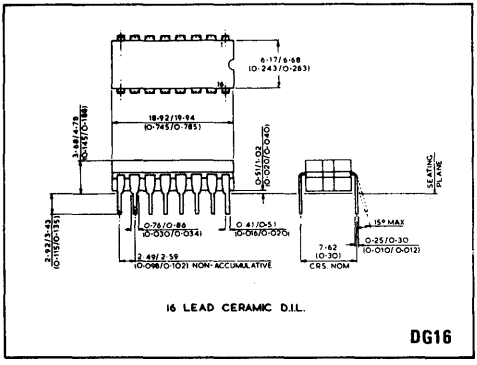


Fig. 7l Supply current variation with temperature

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



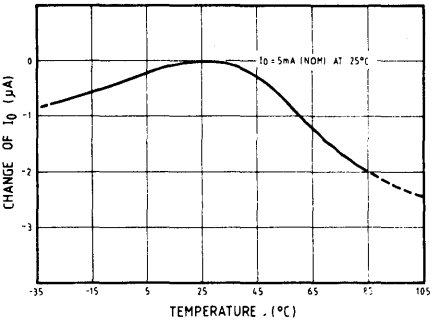


Fig. 7M Analogue output current variation with temperature

SP9752

TWO BIT EXPANDABLE A TO D CONVERTER

The SP9752 is a circuit block containing four comparators with associated decoding logic intended for use in the construction of A/D converter systems where the ultimate in speed performance is required.. Input and output logic levels are ECL compatible.

FEATURES

- Minimum set–up time 2 nS
- Maximum input offset 5 mV
- Latch to output delay 4 nS
- Maximum clock frequency 125 MHz
- Four comparators in 16–lead pack
- On–chip decoding with carry and $\overline{\text{carry}}$

GENERAL DESCRIPTION

Following the concept of the SP9750 and SP9685 high speed latched comparators, the SP9752 contains four comparator elements with master–slave latches in a configuration optimised for use in fast parallel, or combinatiob series–parallel A–D converters. Each comparator has a relatively low gain in the track mode, followed by a latch stage conferring essentially infinite gain in the hold mode to produce an unambiguous decision. On–chip decoding logic converts the master latch outputs into binary coded format, then slave latches hold the information through the clock period for maximum system flexibility. The provision of a complementary carry out (Co) eases the decode logic requirement. It is anticipated that most ystem designs using the SP9752 will be realised in ECL 10K logic for high speed operation with a minimum package count. Logic inputs to, and futputs from, the device are fully ECL compatible.

The basic comparator circuit is shown in Figure 3. Transistors Q1A, Q1B, Q2A, Q2B provide high input impedance, low offset modest gain in the track mode, but are switched off in hold when the cross–coupled pair Q5A, Q5B provide the latch function.

The slave latches are essentially simplified versions of the master latches. Master–slave action is determined be on–chip timing operations, and produces essentially glitch–free output conditions which are a pre–requisite of a successful multi–chip converter.

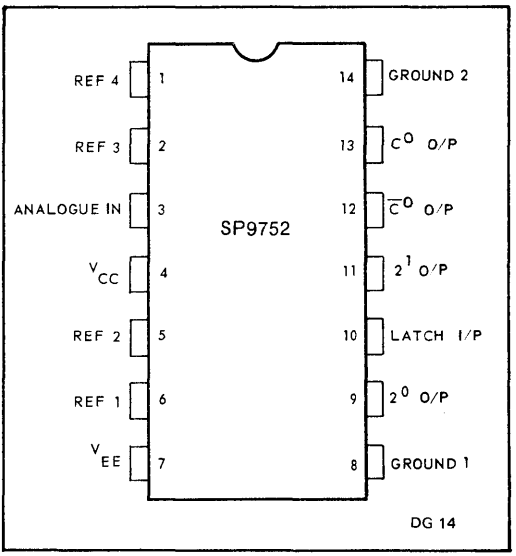


Fig. 1 Pin Connections.

DEFINTIONS

t_{pw} Minimum latch pulse width – the minimum time that the latch signal must be in the high (ECL definition) state for input acquisition to take place.

t_h Minimum hold time – the minimum time for which the input signal must maintain a particular level after the negative latch transistion for acquisition to take place.

t_s Minimum latch set–up time – the minimum time before the negative latch transistion that an input signal must be present for acquisition to take place.

t_{pd} Latch–to–output delay – the propagation delay measured from the 50% point of a latch transition to the 50%point of the corresponding output transition.

F_{CM} Maximum clock frequency – the maximum repetition rate of the latch command.

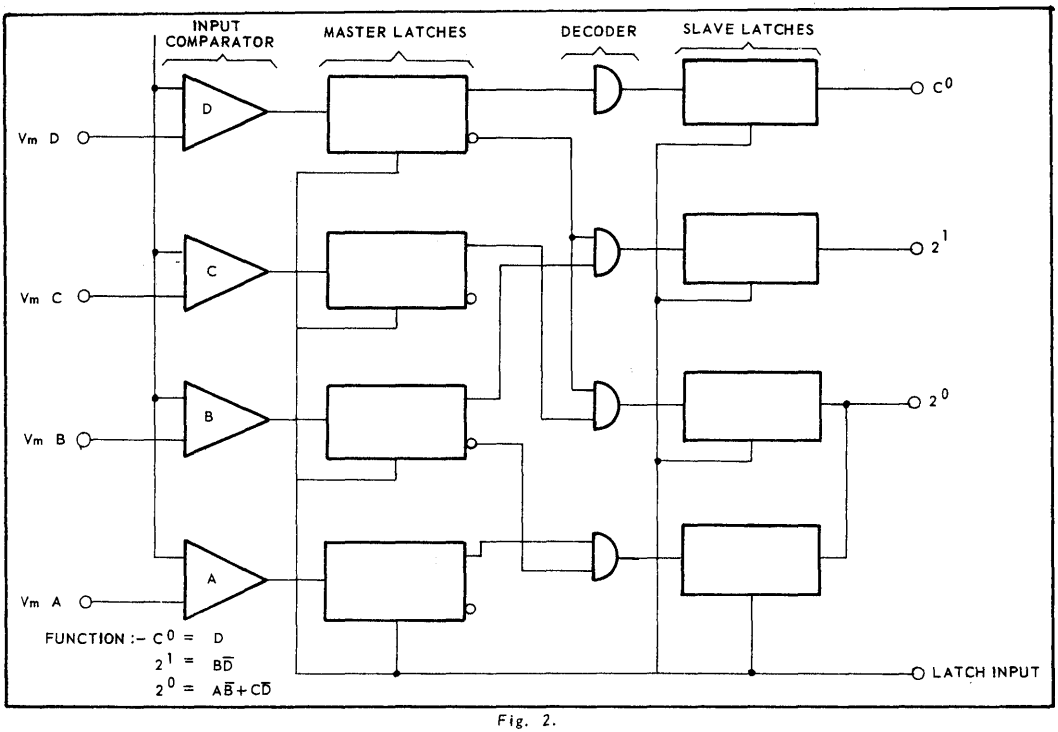

INPUT COMPARATOR
MASTER LATCHES
DECODER
SLAVE LATCHES
Vm D
Vm C
Vm B
Vm A
D
C
B
A
C0
21
20
LATCH INPUT
FUNCTION :- C0 = D
21 = BD̄
20 = AB̄+CD̄

Fig. 2.

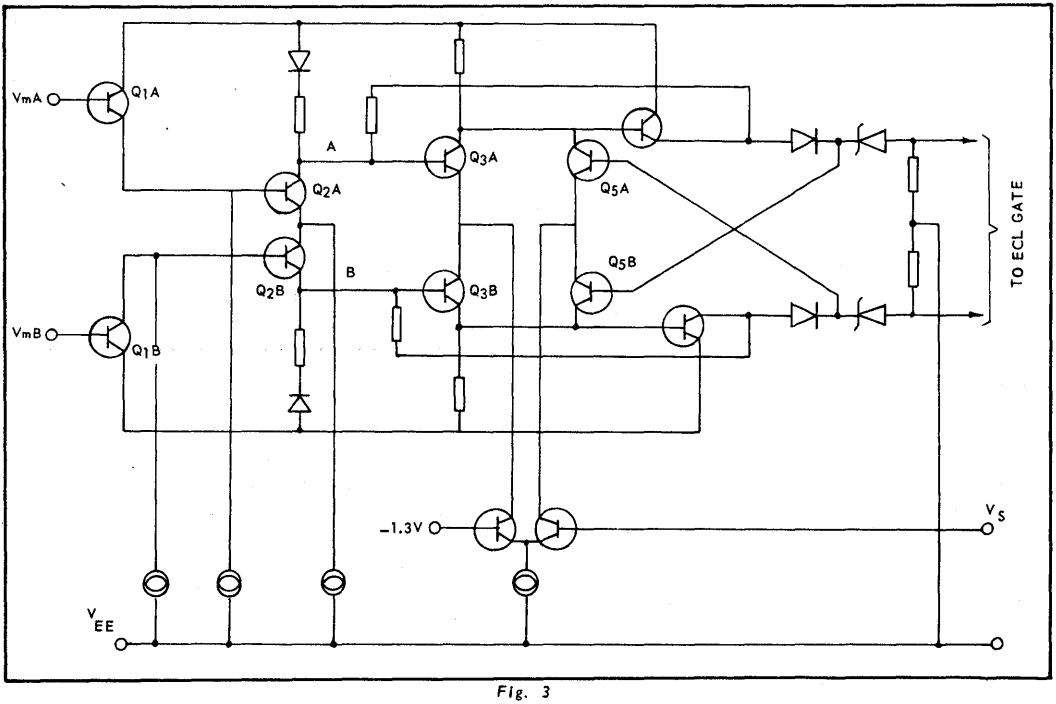

VmA
VmB
Q1A
Q1B
Q2A
Q2B
Q3A
Q3B
Q5A
Q5B
A
B
-1.3V
VS
VEE
TO ECL GATE

Fig. 3

ELECTRICAL CHARACTERISTICS

Test Conditions:–

T_{AMB} = 20°C

V_{CC} = 5.00V ±.25V

V_{EE} = –7.00 ±.25V

R_L = 50 ohm (equivalent)

Characteristic	Min	Typ	Max	Units	Comments
Input Offset Voltage	–5		+5	mV	R_{SOURCE} <100 Ω
Input Bias Current		14	40	µA	
Reference Input Current		4	10	µA	
Supply Current I_{CC}		41	60	mA	
Supply Current I_{ee}		76	90	mA	
Total Power Dissipation		750		mW	
Min. Latch Set–up Time			2	nS	
Latch to Output Delay		4		nS	Input o/d> 10mV
Min. Hold Time		4		nS	
Min. Latch Pulse Width		4		nS	
Max. Clock Frequency		125		MHz	
Input Capacitance		6.2		pF	
Latch Input Capacitance		2.6		pF	
Common Mode Range	–2.0		+2.0	V	
Output Logic Levels					
Output High	–.96		–.81	V	) Standard ECL
Output Low	–1.85		–1.65	V	)
Operating Temp. Range	–30°		+85°	°C	500 L.F.P.M. air flow

DYNAMIC TESTING

High speed testing of devices of this kind is necessarily a difficult undertaking and the suggested circuit shown in Figure 4 should be carefully constructed if accurate results are to be obtained. The test arrangement is designed to select a single comparator and to measure the response times from the latch to the outputs. Input to output delay are difficult to deal with due to the master/slave action; more relevant are the set–up and hold times. Operation is as follows:

1. Select the comparator to be tested by S3
2. Select position 1 on S2
3. Adjust for a middle state of the outputs using S1. The output should be randomly triggered by noise into alernate states.
4. Set up offset (2mV, 5mV or 10mV on S2 and measure the appropriate delays.
5. Repeat 1–4 on next comparator.

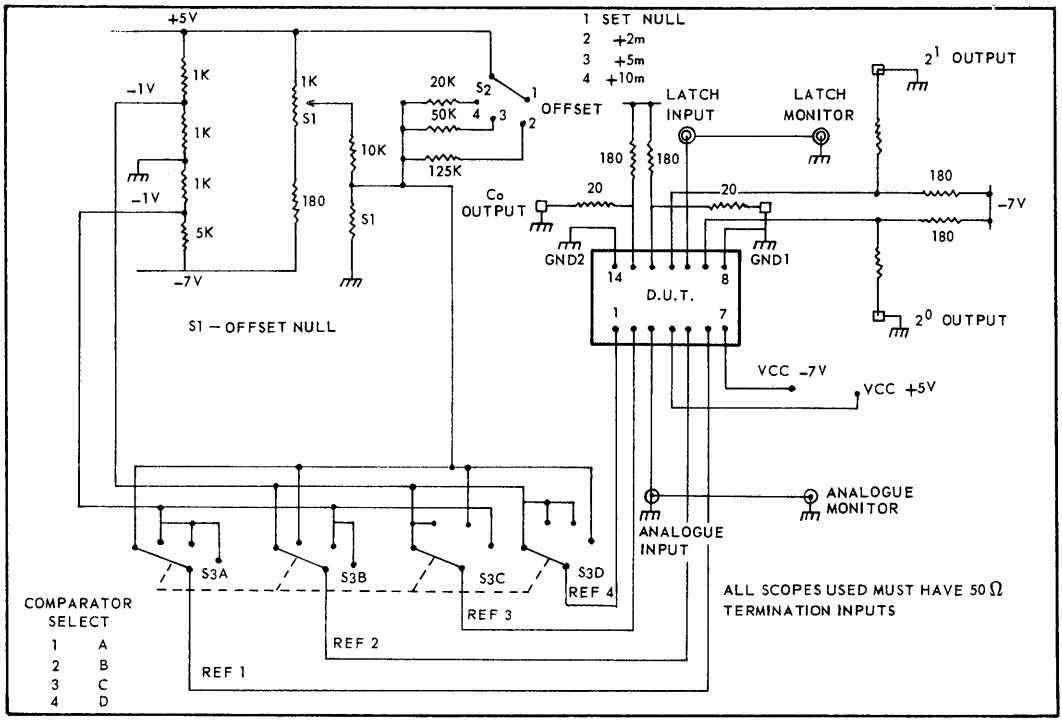


Fig. 4 Dynamic Test Box Wiring Diagram.

APPLICATIONS

5–bit ADC 125 MHz

A five–bit all–parallel ADC is shown in Figure 5. Operation at 125MHz is possible with no missing codes. Analogue and latch inputs are distributed along transmission lines designed to have matched propagation delays, to minimise latch aperture error. in many applications this avoids the need for a separate sample and hold function. The system input voltage range is ±1.5 volts at 50 ohms. Encoding is by ECL 10K logic, which is the prime speed limitation

The use of master/slave latching retimes the outputs which are available for the whole clock period.

This converter concept can be extended in principle to nine bits, but practical considerations limit the usefulness in all–parallel systems to six or seven bits, as, for example, seven bits require 32 SP9752's eight bits require 64, ect. In addition, latch and input signal distribution of sufficient accuracy becomes difficult, particularly in relation to aperture error.

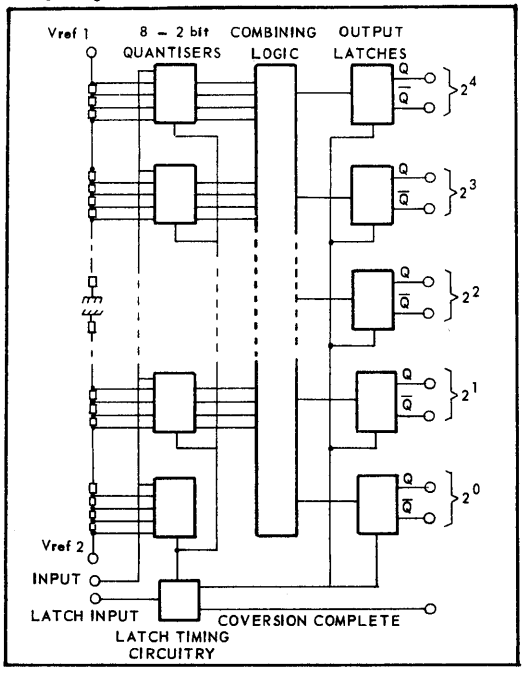


Fig. 5 Block Diagram of 5 bit A/D Converter.

SP9754

FOUR BIT EXPANDABLE A TO D CONVERTER

The SP9754 is a fast 4 bit A/D converter, expandable up to 8 bits without additional encoding circuitry.

It can convert at sample rates from DC to 110MHz, with analogue inputs up to Nyquist frequencies. All output levels are E.C.L. compatible.

The latch function to the device provides on–chip sampling which allows the converter to operate with out an external sample and hold. Data is clocked through the device in masterslave fashion, ensuring that all outputs are synchronous and valid for the complete clock period.

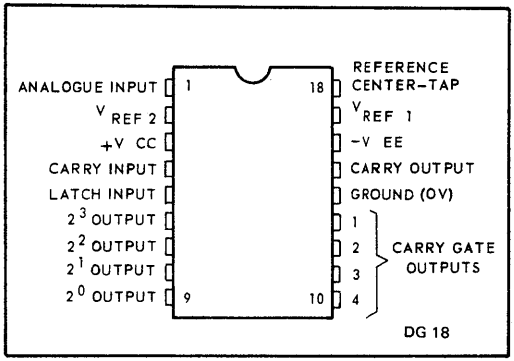


Fig. 1 Pin Connections

FEATURES

- No external components for 4–bit conversion.
- 110MHz conversion rate.
- On–chip encoding for expansion to 8 bits.
- No external sample and hold needed.
- On–chip resistor reference divider.
- Bit size 10–100mV.
- ECL compatible.

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	–7.5V
Operating temperature range	$-30^{o}C$ to $85^{o}C$
Storage temperature	$-55^{o}C$ to $+125^{o}C$
Lead temperature (soldering 60sec)	$300^{o}C$

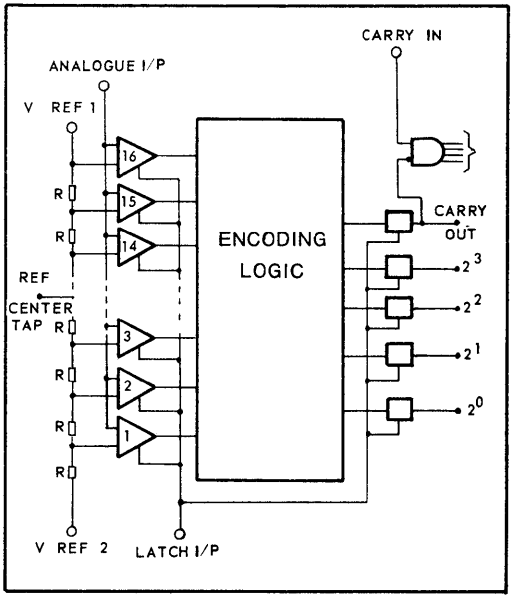


Fig. 2 Functional Diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):–

T_{AMB} = 25°C

V_{CC} = +5V

V_{EE} = –7V

R_L = 100 ohm to –2V

CHARACTERISTIC	SYMBOL	VALUE				CONDITIONS
		Min	Typ	Max	Units	
Analogue input current	I_B		30	100	µA	V_{IN} = 0V
Analogue input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	–2		+2	V	
Maximum input slewrate			1000		V/µsec	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I^+		55	65	mA	) See Fig. 11.
Negative supply current	I–		85	95	mA	)
Reference resistor chain			25		Ω	
Reference bit size		10		100	mV	
Comparator offset voltage	V_{os}	–5		+5	mV	
Total power dissipation	P_{DISS}		950	1100	mW	All outputs loaded
Output logic levels						
Logic high	V_{OH}	–0.930		–0.720	V	) for 100 ohm load
Logic Low	V_{OL}	–1.850		–1.620	V	) to –2V
Min. latch set–up time	t_S		1.5	2	nsec	10mV overdrive
Latch to output propagation delay						
Latch enable to output high	$t_{pd}+(E)$		6	8	nsec	
Latch enable to output low	$t_{pd}-(E)$		5	8	nsec	
Carry input to M.S.B. delay	t_{pd} (C)		3	5	nsec	
Max. sample rate	$F_{c\ max.}$	100	110		MHz	

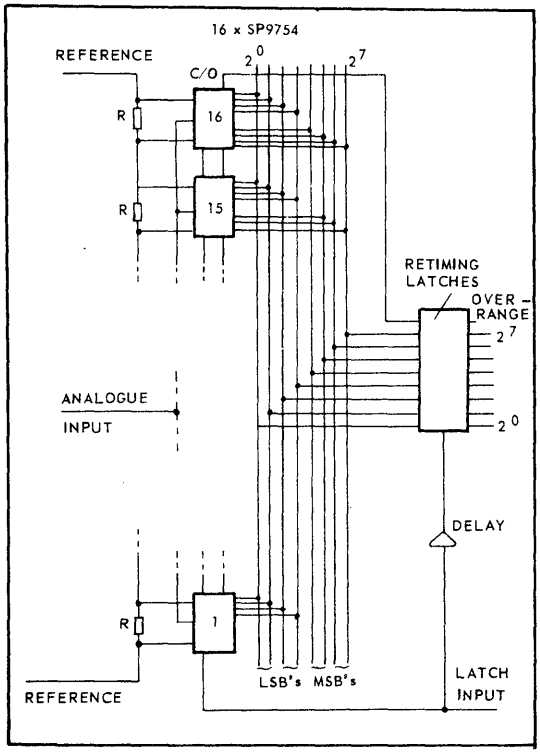


Fig. 3 8-bit All Parallel System

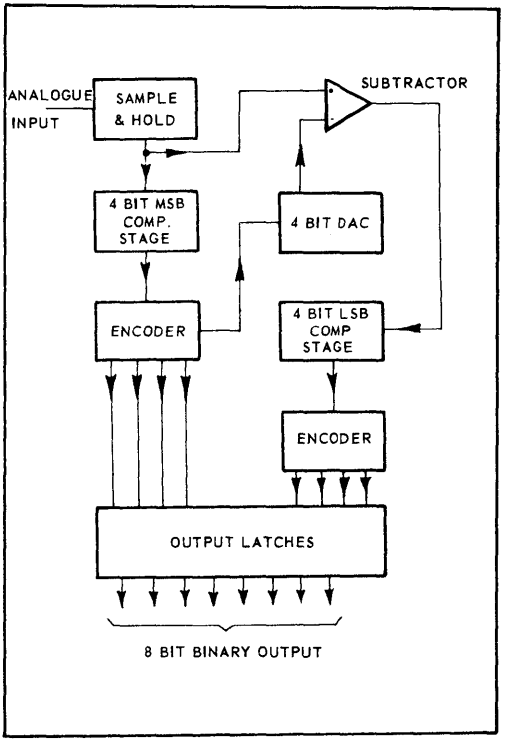


Fig. 4 Parallel Series Parallel System

PERFORMANCE CURVES

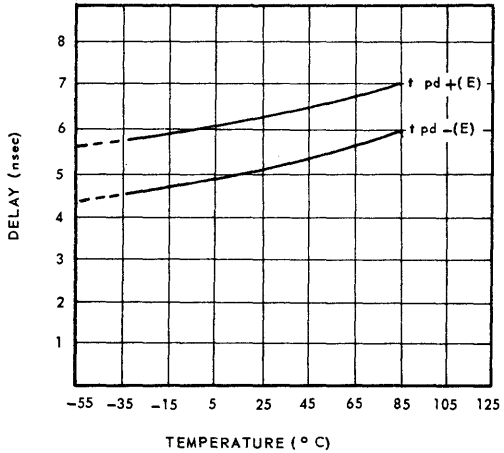


Fig. 5 Latch to Output Propagation Delay as a Function of Temperature

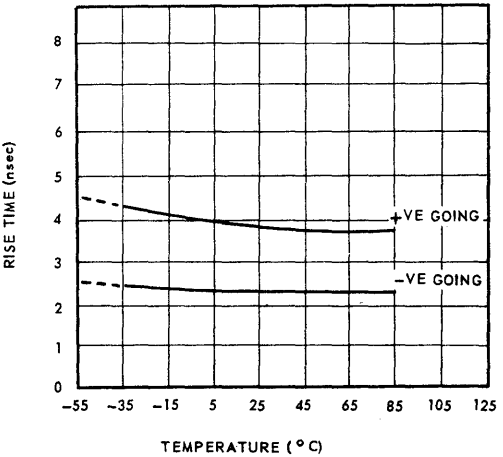


Fig. 6 Output Rise/Fall Times as a Function of Temperature

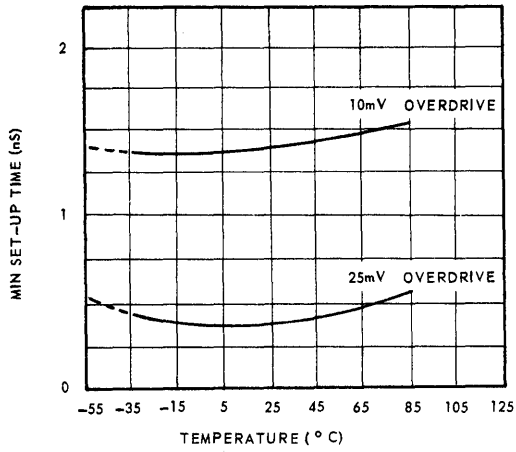


Fig. 7 Set–up Time as a Function of Temperature

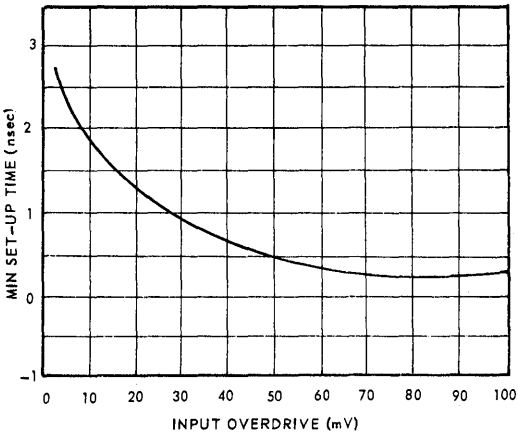


Fig. 8 Set–up Time as a Function of Overdrive

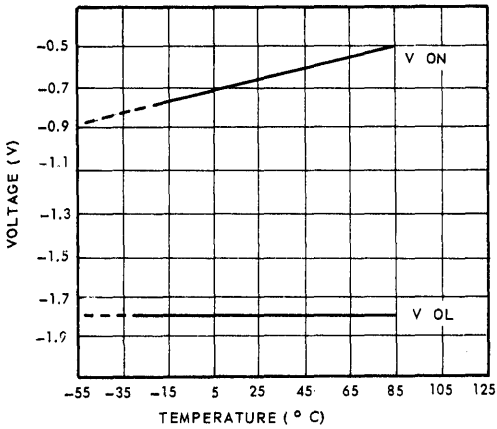


Fig. 9 Output Logic Levels as a Function of Temperature

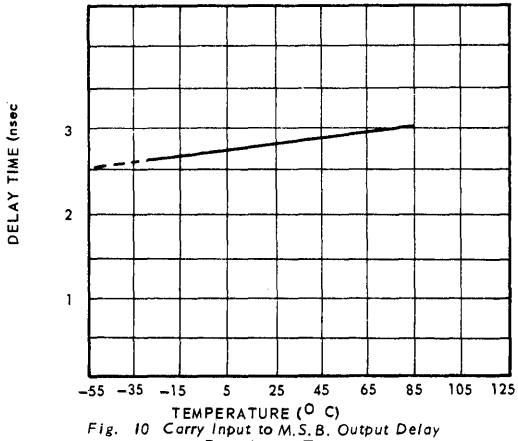


Fig. 10 Carry Input to M.S.B. Output Delay as a Function to Temperature

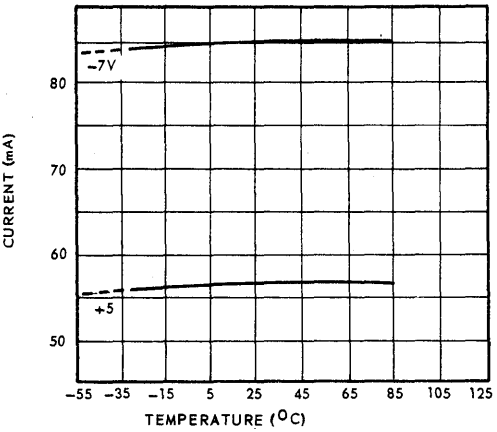


Fig. 11 Supply Current as a Function of Temperature

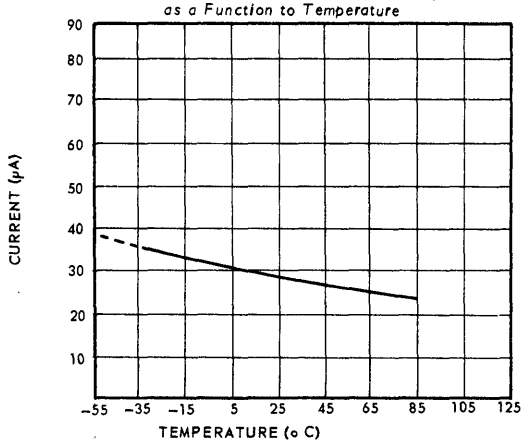


Fig. 12 Analogue Input Current as a Function of Temperature

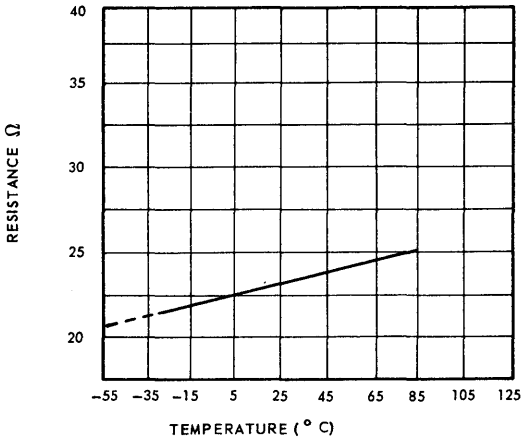


Fig. 13 Network Resistance as a Function of Temperature

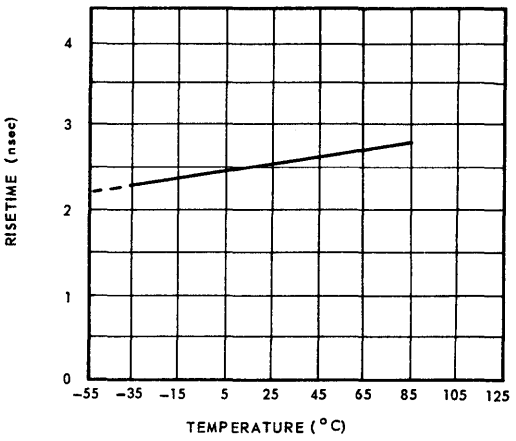


Fig. 14 M.S.B. Output Edge Speeds as a Function of Temperature

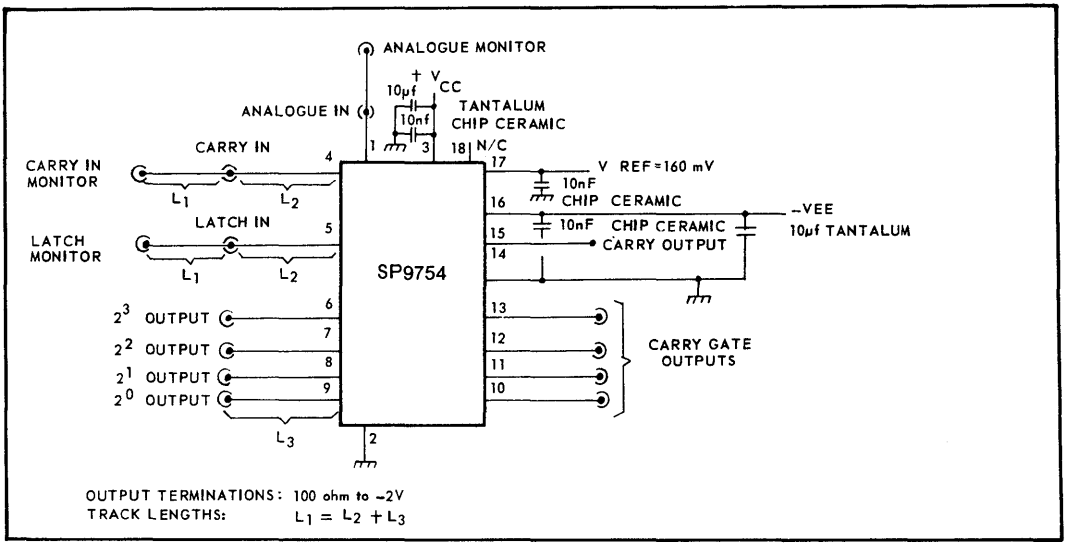


Fig. 15 Test and Applications Circuit for SP9754

SP9768
8-BIT DAC CONVERTER

The SP9768 8–bit D/A converter is capable of ɔnvertin a digital signal into an analogue volt–ɟe at a rate of over 100 megasamples per second lSPS). An inherently low glitch design is used ıd the complementary current outputs are suitable r direct transmission line drive. Included on the ıip are a high performance voltage reference and ference ampli fier.

EATURES

- 5 ns settling time
- 8 bits to ±½ L.S.B. Absolute and differential non–linearity.
- 100 MSPS update rate.
- Current output
- ECL standard inputs.
- Complementary outputs, 20 ma full scale.
- Reference tempco. typically 20 ppm/^{o}C
- DAC usable in multiplying mode to 40MHz
- 18–lead, 0.3" pitch package.

BSOLUTE MAXIMUM RATINGS

- Positive Supply Voltage +6v
- Negative Supply Voltage −6v
- Storage Temperature Range −55^{o} C to +125^{o} C
- Operating Temperature Range −55 ^{o} C to+125^{o}C

IRCUIT DESCRIPTION

The DAC has current outputs, with a nominal full ɜale for 20ma, corresponding to a 1 volt drop across 50ohm load, or ± 1 volt across 100ohms returned + 1 volt.
ɜe note 2.
The actual output current is determined by the on–ıip reference voltage and an off–chip current set–ng resistor. Output current, I_{OUT}, is given by:-

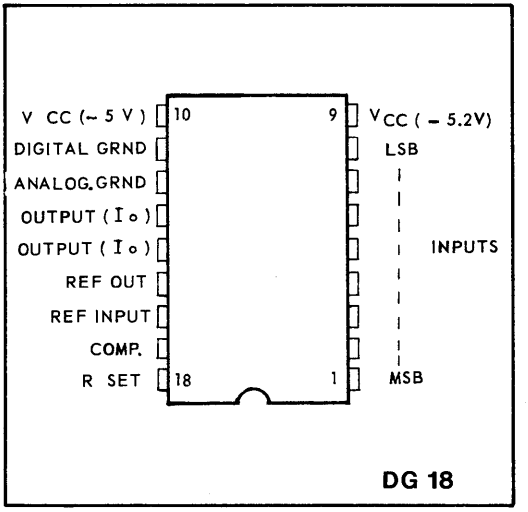


Fig. 1 Pin connections

$$I_{OUT} = 4 \times \frac{V_R}{REF_{SET}} \quad \text{at full scale}$$

A complementary I_{OUT} is also provided. The setting resistor R_{SET}, is typically 220 ohms, and should have a temperature coefficient similar to that of the output load resistor.

Where the load is an oscilloscope, with a 50 ohm nominal input, a good quality metal oxide resistor should be used for R_{SET}. It is important to real–ise that reflections present in 50 ohm load systems will often prove to ve a limiting factor in the mea–surement of settling time.

The reference voltage source is nominally 1.280 volts and is of a modified bandgap type, average temperature coefficient of 20 ppm/ o C over the range – 55 o C to 125 o C, corresponding to approx imately 1 L.S.B. change over this temperature range.

The reference supply is nominally on–chip stable; however, to reduce the possibility of instability or noise generation, pin 15 can be decoupled using a high quality ceramic chip capacitor. The current loop tech–nique has been used with a high performance loop

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)

Tamb 25 ^{o} C

V_{cc} + 5.00v ± 5%

V_{ee} − 5.20v ± 5%

R_L = 50 VL

R_{set} = 220 VL

		Min	Max
Input voltage	High	− .96	− .81
	Low	−1.85	−1.65

Characteristics	Value				Conditions
	Min	Typ	Max	Units	
Differential Non–Linearity			.2	%	
Absolute Non–Linearity			.2	%	
Resolution		8 .39		Bits %	
Settling time		5		nS	See note 1
Nominal bit size		78		µA	) R_{set} 220 Ω
		4		mV	R_L 50)
Positive output compliance		−3		volts	
Negative output compliance	1 − 0.7			volts volts	25 ^{o} C) − 85 ^{o} C) see note 2
Multiplying Bandwidth		40		MHz	Current mode note
Maximum Full Scale output		30		mA	
Minimum Full Scale Output		2		mA	
Reference voltage		1.28		volts	
Temp. coeff. of Reference voltage		20		ppm/ ^{o} C	
Zero output		60		µA	
Output Current Symmetry		100		µA	

amplifier. Current setting is by an external resistor as described above. Stabilisation of the loop amplifier is by a single capacitor from pin 17 to ground. Minimum value is 3900 pF, although a 10 nF chip ceramic is recommended.

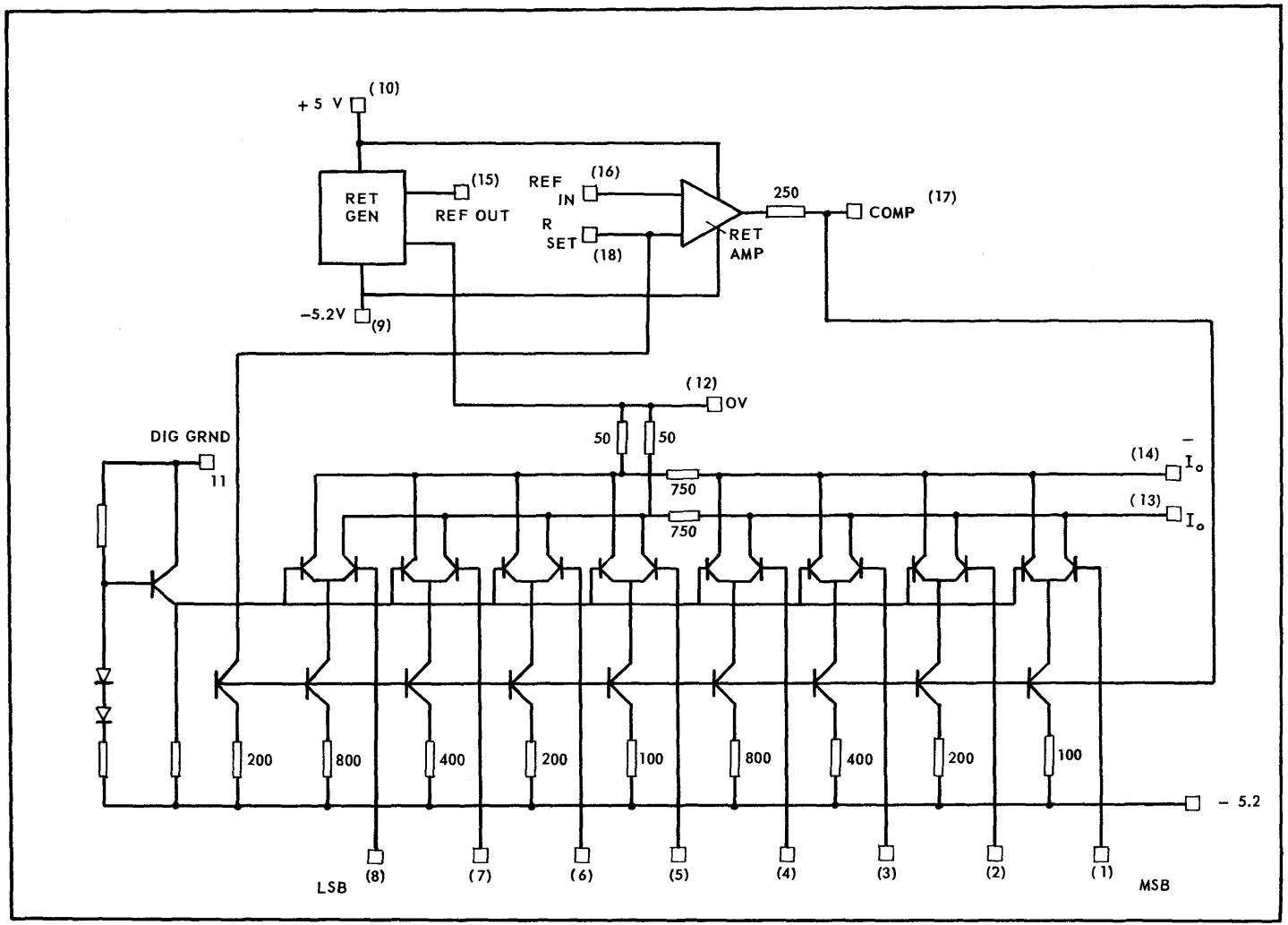


Fig. 2 Schematic 8-Bit DAC SP9768

OPERATING NOTES

1. Measurement of Settling Time

The settling time of the SP9768 is measured for a worst case transition of 0 to full scale.

Oscilloscopes. whether real time or sampling, do not have sufficiently low input VSWR or on–screen resolution for precise settling time measurements. A measurement technique has been designed, shown diagrammatically in Figure 3, in which the DAC can settle into a nearly ideal 50 ohm load, with minimal interconnection paths; this is also very closely related to the practical use of the device. Precision settling time measurements can be performed with a high speed comparator, conveniently a dual device, such as the SP9687, with a minimal delay time, in this case about 2 ns. Two references are set up to detect the DAC output settling within a window, conveniently defined as the settling to grounr of the output.

The lower comparator detects the DAC output coming within ½ LSB of the final settling point,while the upper device checks that there is less than ½ LSB of over shoot.

2. Output Compliance

Figure 5 shows the method of using the SP9768 with a load resistor not reffered to groud. This connection will be used most often when a larger output voltage than that permitted by the – 0.7 volt negative output voltage compliance specification is required. The output resistor can be referred to a positive supply in this case as long as R set and the analogue grad are also referred to this voltage. If I out is also connected to this reference then decoupling will be simplified.

3. Multiplication Modes

Multiplying operation of the DAC is available in two modes, either a voltage applied in place of the reference, or a current supplied via the current source pin. In the former case the 3 dB bandwidth is 250kHz, while in the latter, operational use exceeds 40 MHz. Suggested circuits are shown in Figures 5, 6 and 7.

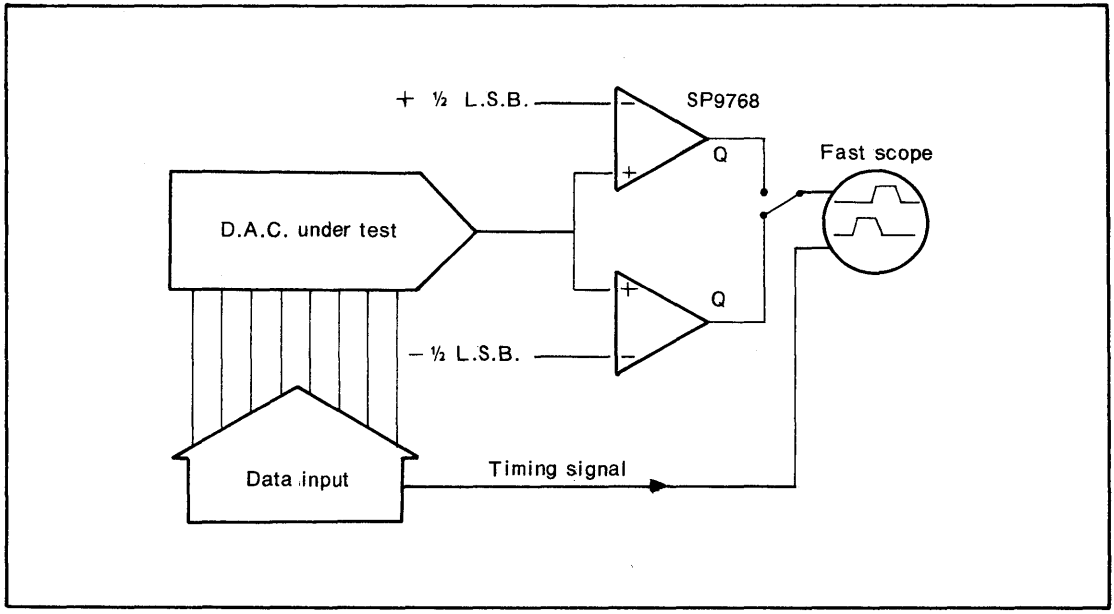


Fig. 3 Test Schematic (Settling Time)

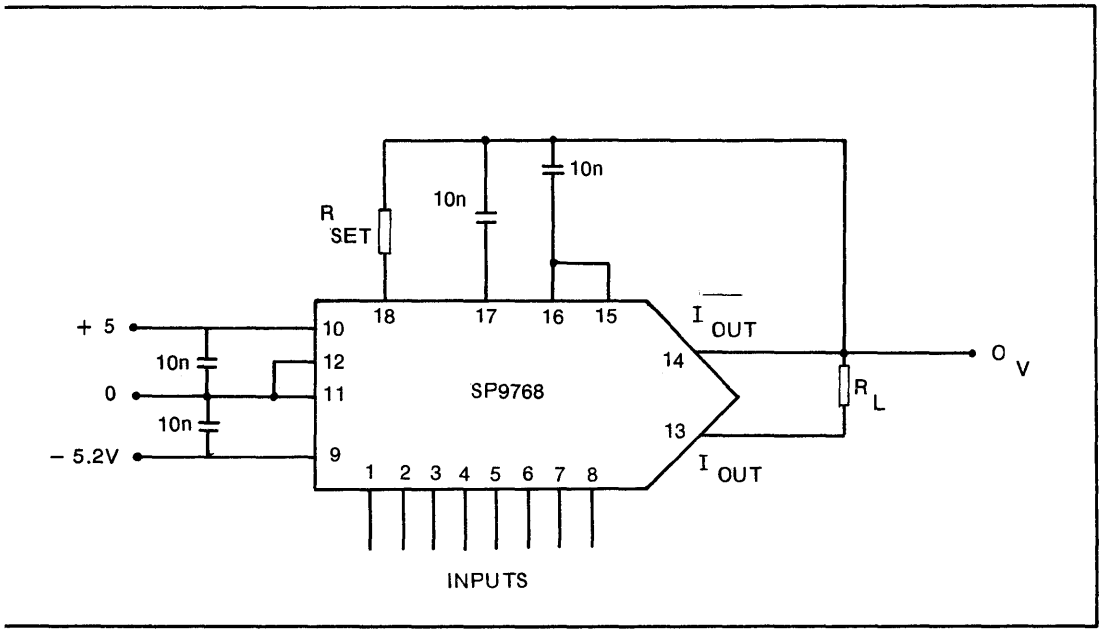


Fig. 4 Conventional DAC –VE output wrt ground

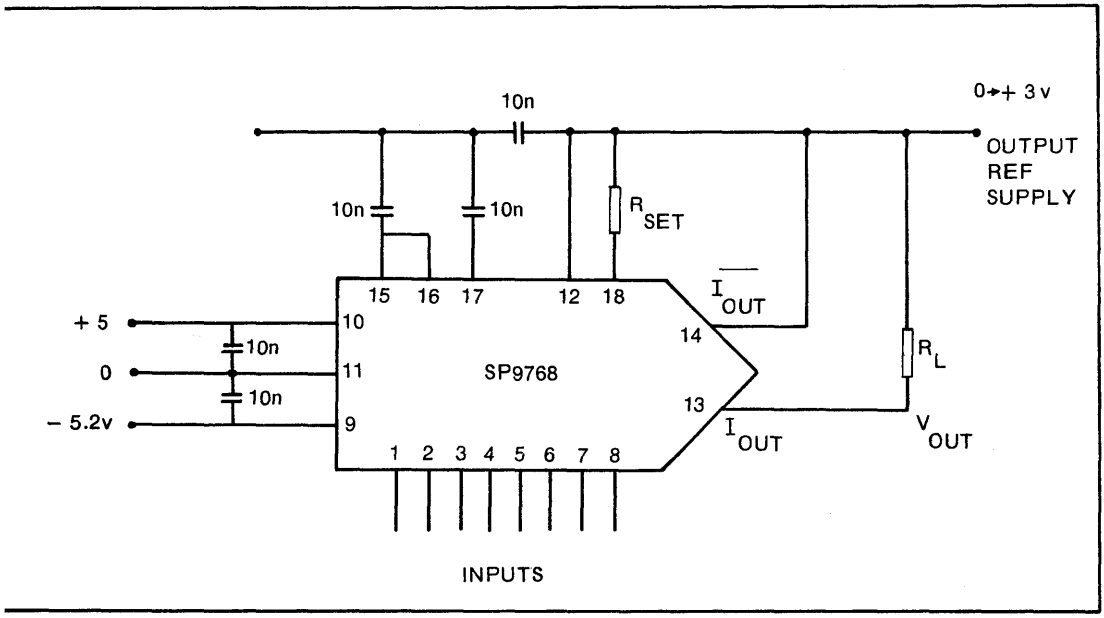


Fig. 5 Voltage output refered to +VE supply.

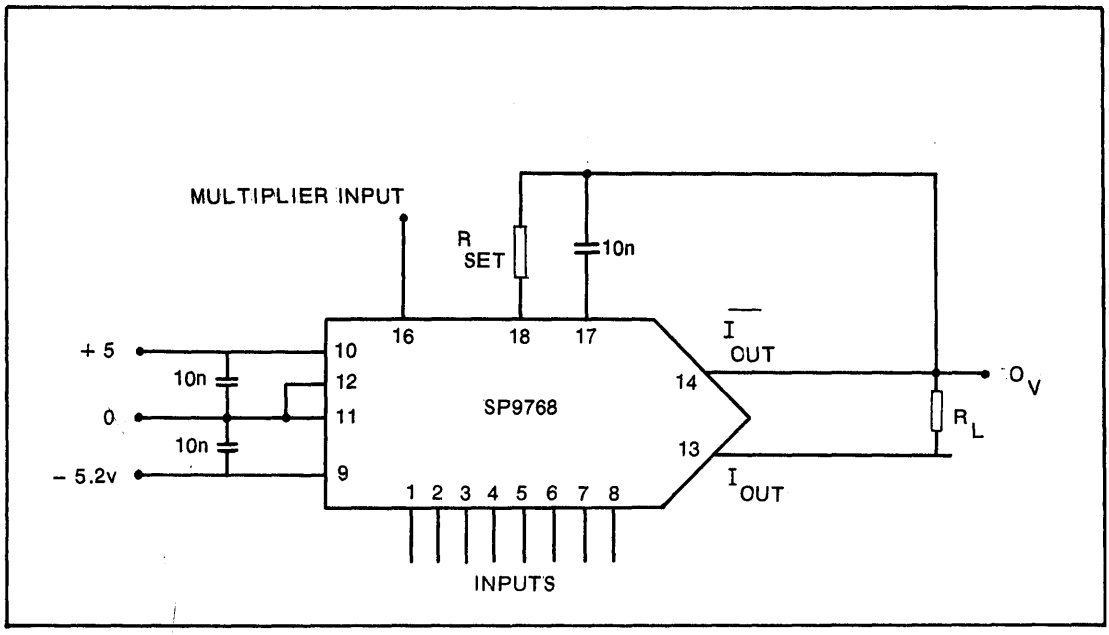


Fig. 6 Multiplying DAC (Voltage Mode)

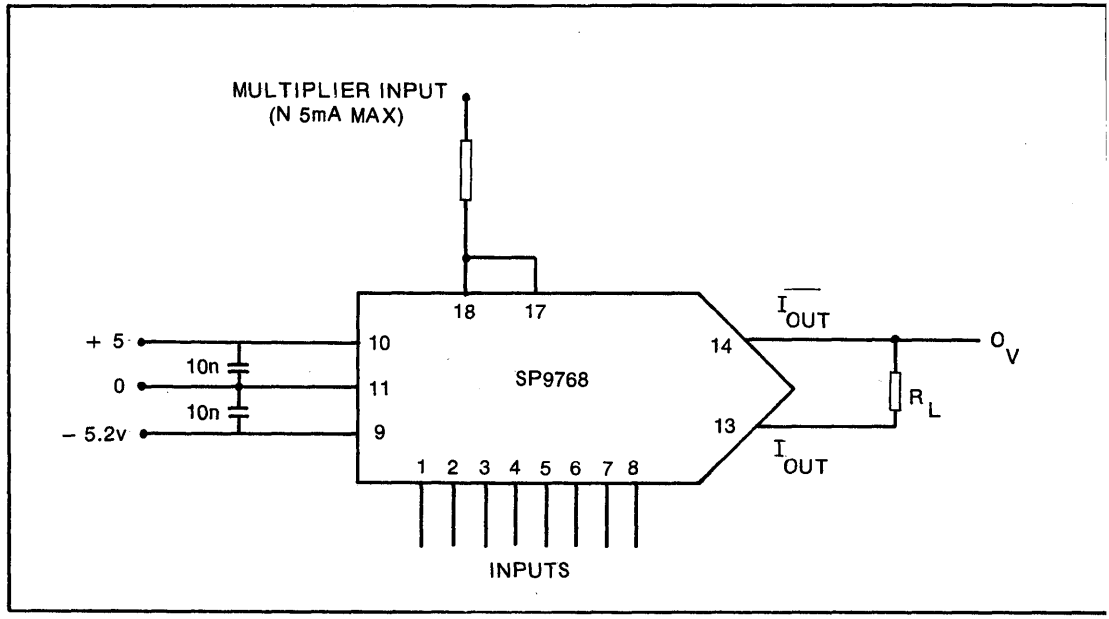


Fig. 7 Multiplying DAC (Current Mode)

SP9770

TEN BIT HIGH SPEED D TO A CONVERTER

ɜ Plessey SP9770 10-bit D/A converter is capable converting a digital signal into an analogue tage at a rate of over 75 mega-bits per sample 3PS). An inherently low glitch design is used and complmentary current outputs are suitable for ɜct transmission line drive. Included on the chip a high performance voltage reference and ɜrence amplifier.

ATURES

- 12 ns Settling time
- 10 bits to ±1/2 LSB absolute and differential non linearity
- 75 MBPS Update rate
- Current output
- ECL standard inputs
- Complementary outputs, 20 mA full scale
- Reference tempco. typically 35 ppm/^{o}C
- DAC usable in multiplying mode to 20MHz
- 24 lead, 0.6 pitch package

SOLUTE MAXIMUM RATINGS

ɨitive supply voltage	
ɟative supply voltage	
ɨitive supply voltage	+5.5V
ɟative supply voltage	—5.7V
ɜrating temperature range	—30 ^{o}C to 85 ^{o}C
rage temperature	—55 ^{o}C to 125 ^{o}C
ɹd temperature (soldering 60 sec)	300 ^{o}C

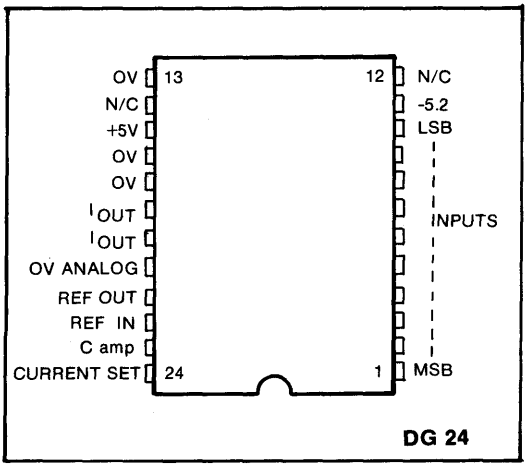


Fig. 1. SP9770 Pin Connections

OPERATING NOTES

The input of the device is shown in Fig. 1. External components are limited to the current setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full scale of 20 mA, corresponding with a 1 volt drop across a 50 ohm load.

The actual output current is determined by the on-chip reference voltage and an off-chip current setting resistor. Output current, I OUT, is given by

$$I_{OUT} = 4 \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. The setting resistor, R_{SET}, is typically 240 ohms, giving a full scale output current of 20.75 mA, and should have a temperature coefficient similar to that of the output load resistor.

The reference voltage source is nominally 1.260 volts and is of a modified bandgap type. Samples show average temperature coefficients of 35 ppm/^{o}C over the range —55 ^{o}C to 125 ^{o}C.

The reference supply is internally compensated; however, to reduce the possibility of instability or noise generation, pin 21 should be decoupled to pin 24 with a 10 nF ceramic chip

Parameter	Min.	Typ.	Max.	Units	Comments
DAC					
Output Current - Full Scale	2		30	ma	IOUT = V_{REF} x R_{SET}
Output Current - Zero		60		μA	
Inputs High	-.96		-.81	V	)Standard ECL
Low	-1.85		-1.65	V	)Compatible
Bit Size		19		μA	Current O/P
Bit Size		1		mV	Into 50 ohm loa
Settling Time - Full Scale		12		ns	To 1 LSB
Multiplying Bandwidth 3dB	20			MHz	Current mode
Resolution (		10		Bits	
(		0.098		%	
Differential Non-linearity			0.05	%	Lower grade
Absolute Non-linearity			0.05	%	available 0.1%
Output Compliance	-.5		+0.5	V	Note 1
Supply Voltage Vcc	+4.75	+5	+5.25	V	
Supply Voltage Vee	-5.45	-5.2	-4.95	V	

Note 1: Pin 17 should be connected to a reference voltage supply at the most positive compliance requir with the load returned similarly to this reference. Conveniently, the reference is ground, but this lim the output to negative voltage excursions only. The output compliance can be increased at t expense of linearity.

Note 2: All measurements are defined for +25 °C ambient temperature.

capacitor. The current loop technique (Reference 1) has been used with a high performance loop amplifier. The current is set by an external resistor as described above. Stabilisation of the loop amplifier is achieved by a single capacitor from pin 23 to ground. Minimum value is 3900 pF, although a 10 nF chip ceramic is recommended.

Multiplying operation of the DAC is avsailable to two modes, either a voltage applied in place of the reference, or a current supplied via the current source pin. In the former case the 3 dB bandwidth is 250 kHz, while in the latter, operational use exceeds 20 MHz. Suggested circuits are shown in Fig. 2.

Measurement of Settling Time

Oscilloscopes, whether real time or sampling do not have sufficiently low input VSWR or on-screen resolution for precise settling time measurments. A measurment technique has been devised, shown diagrammatically in Fig. 3, in which the DAC can settle into nearly ideal 50 ohm load, with minimal interconnection paths; this is also very closely related to the practical use of the device. Precision settling time measurements can be performed with a high speed comparator, conveniently a dual device, such as the SP9687, with a minimal delay time, in this case about 2 ns. Two references are set up to detect the DAC output settling within a window, conveniently defined the settling to ground of the output.

The lower comparator detects when the DA output has settled within 1/2 LSB of the final settli point, while the upper device when switched checks that there is no overshoot. In fact, t settling is very well behaved, and after correction f comparator delay, the results consistently show DAC settling time of 12 ns ±1 ns, defined from t 50% point of the DAC input switching waveform. N correction has been made for the excess loadi capacitance at the output mode, so these results a

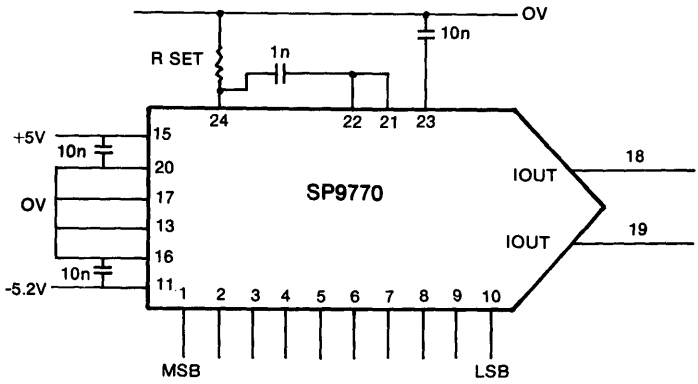


Fig. 2a. Conventional D/A operation using on-chip reference

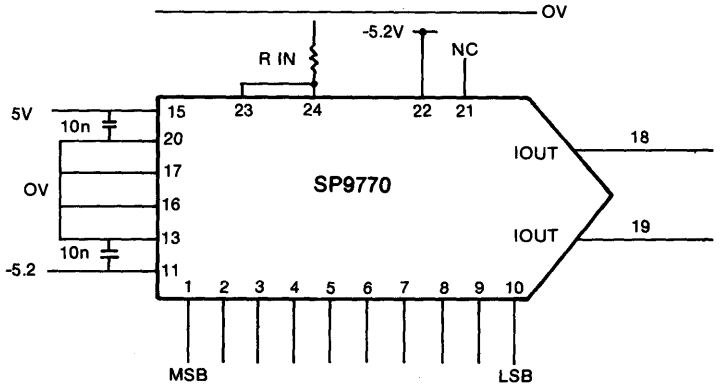


Fig. 2b. Multiplying Mode operation

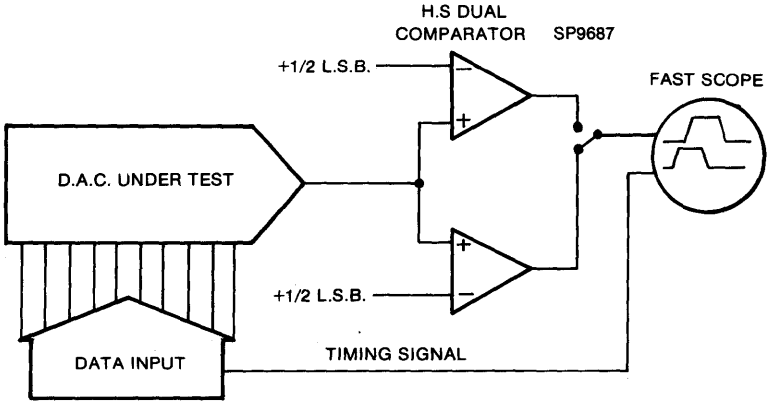
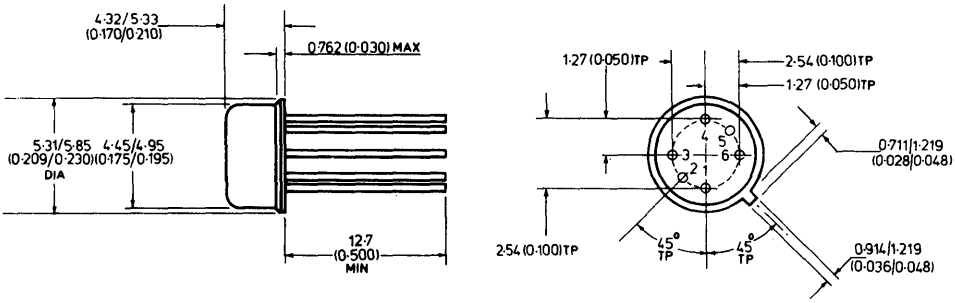


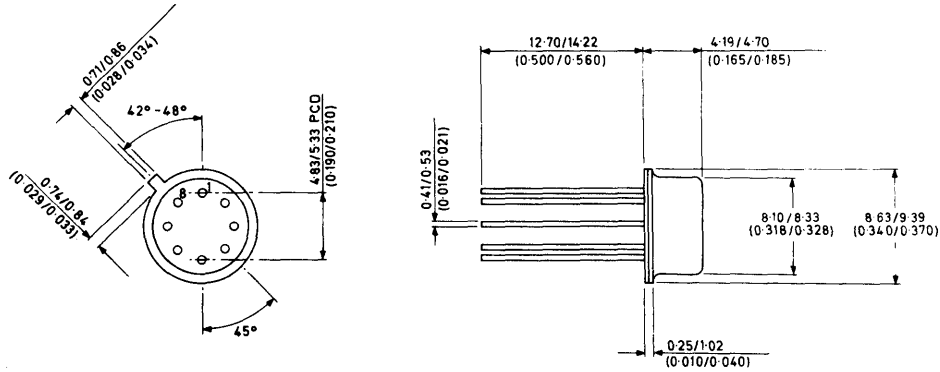
Fig. 3. Window detection of D.A.C. output settling

PACKAGES



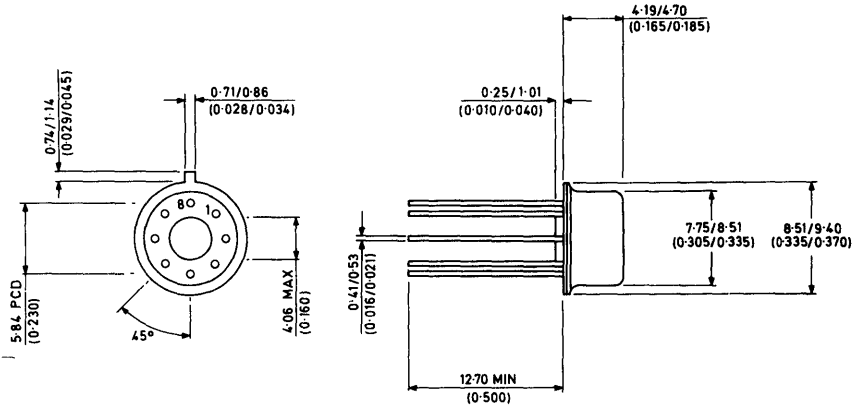
6 LEAD TO-71

CM6



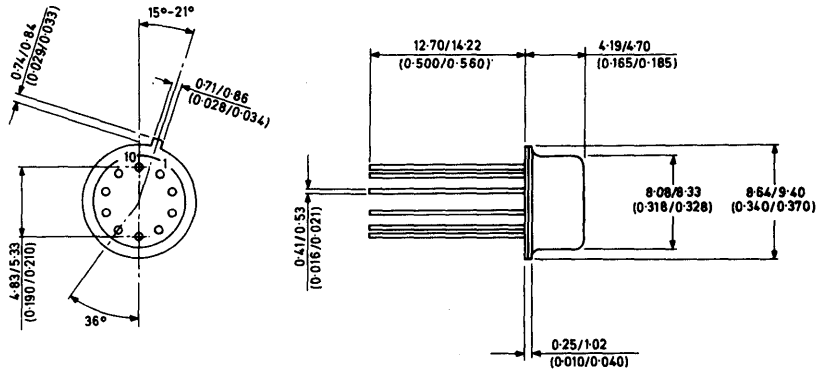
8 LEAD TO-5 (5·08mm PCD)

CM8



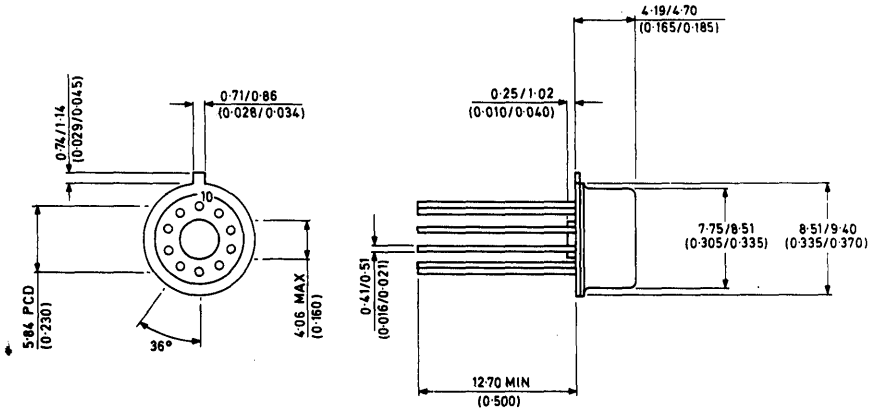
8 LEAD TO-5 (5·84mm PCD) WITH STANDOFF

CM8



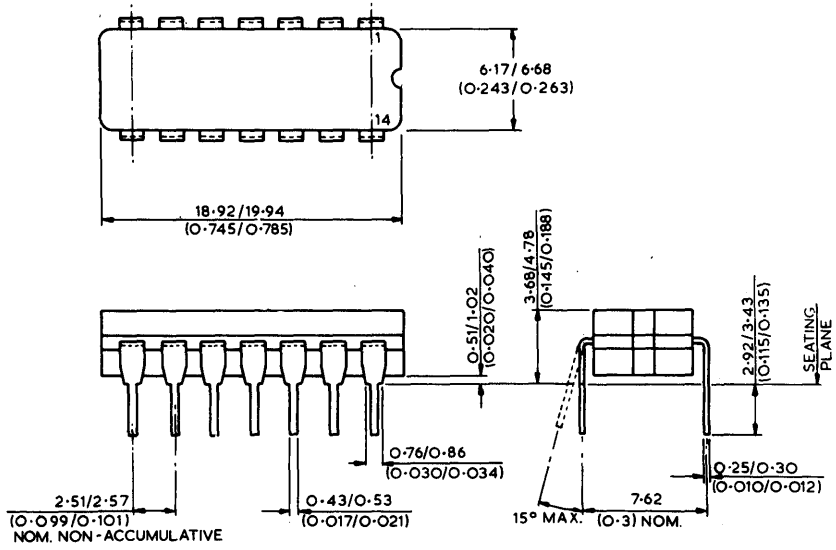
10 LEAD TO-5

CM10



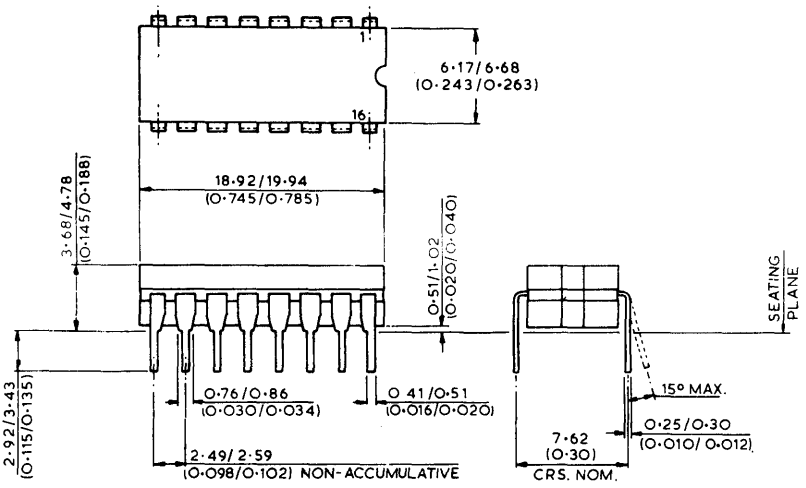
10 LEAD TO-100 (5·84 mm PCD) WITH STANDOFF

CM10



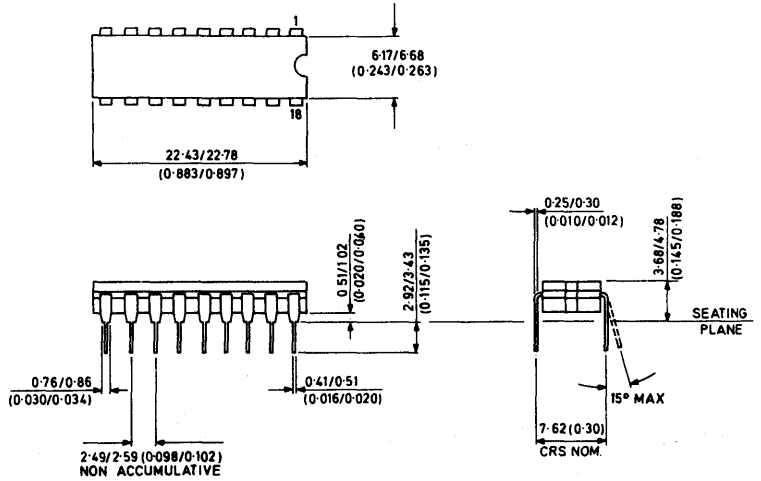
DG14

14 LEAD CERAMIC D.I.L.



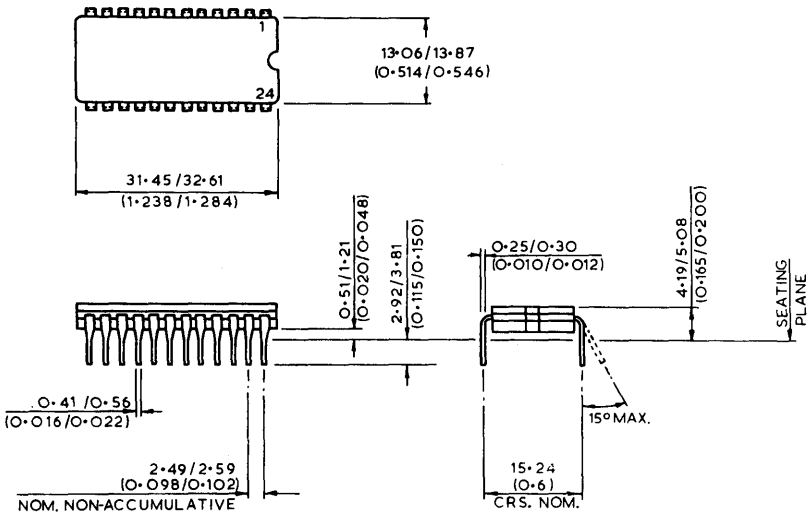
16 LEAD CERAMIC D.I.L.

DG16

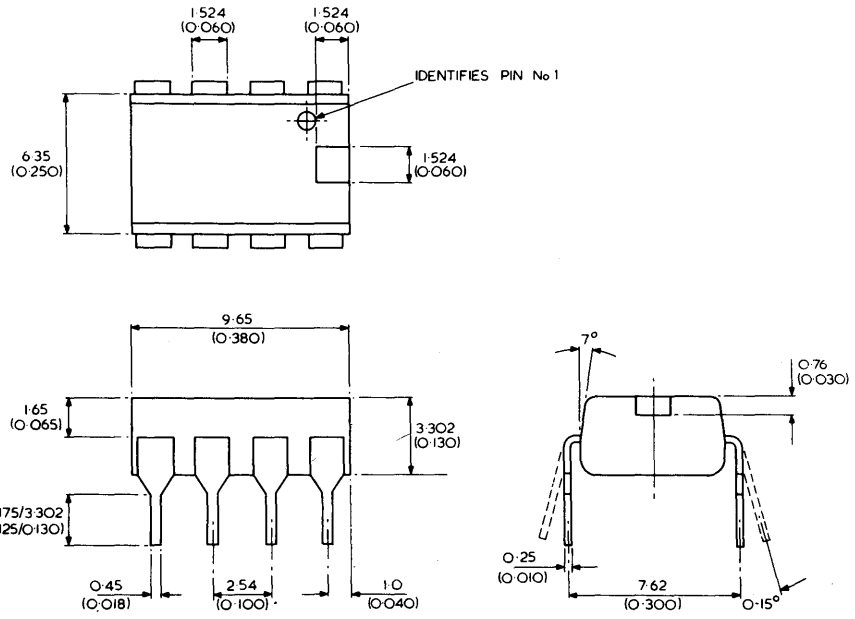


18 LEAD CERAMIC DIL

DG18



DG24 24 LEAD CERAMIC D.I.L.



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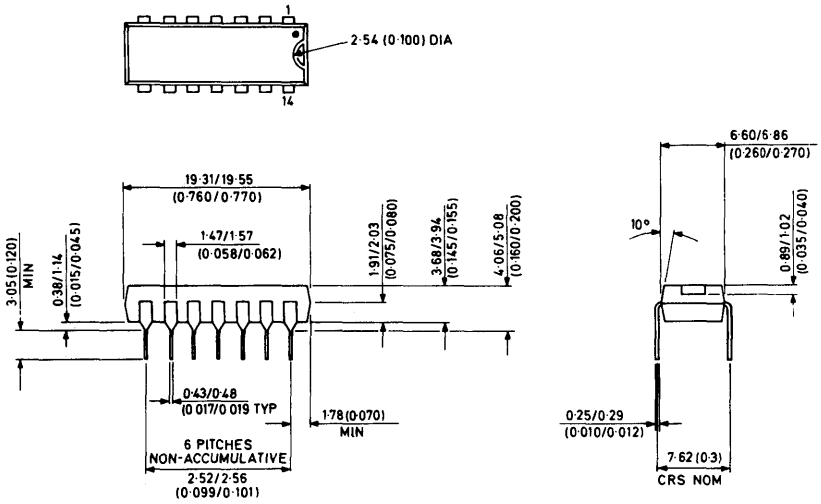
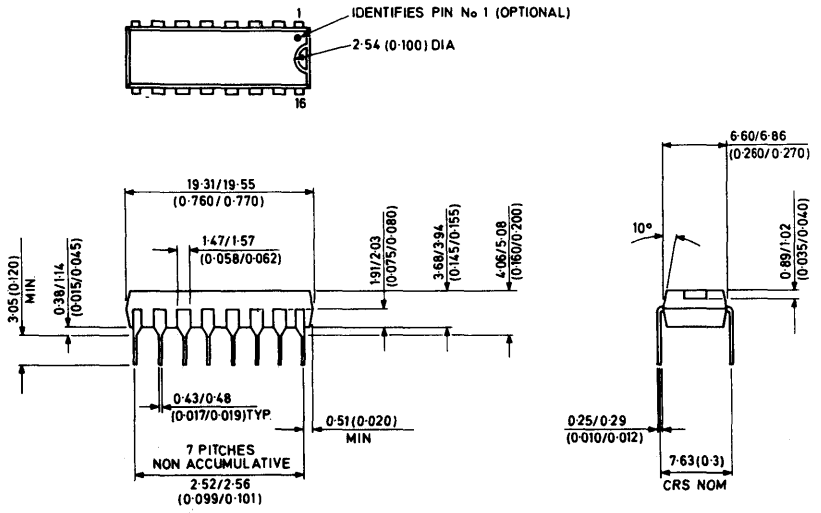


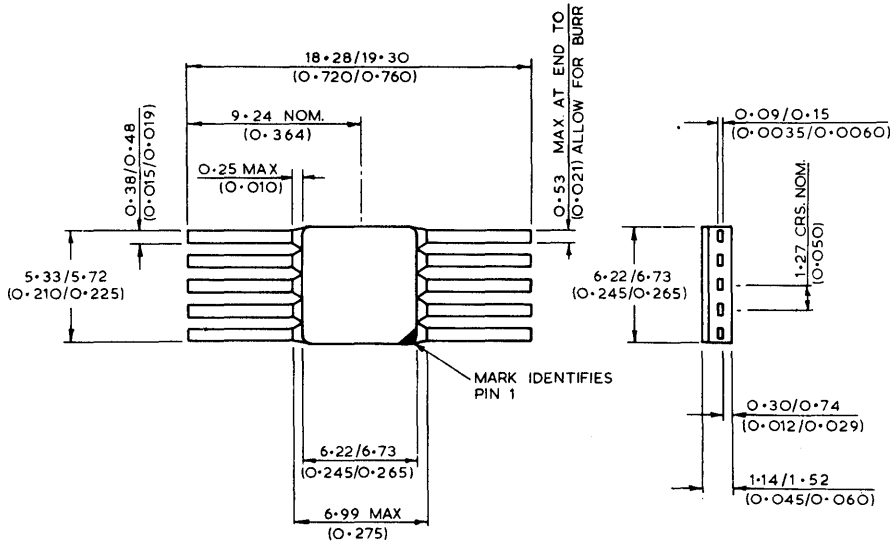
14 LEAD PLASTIC D.I.L.

DP14

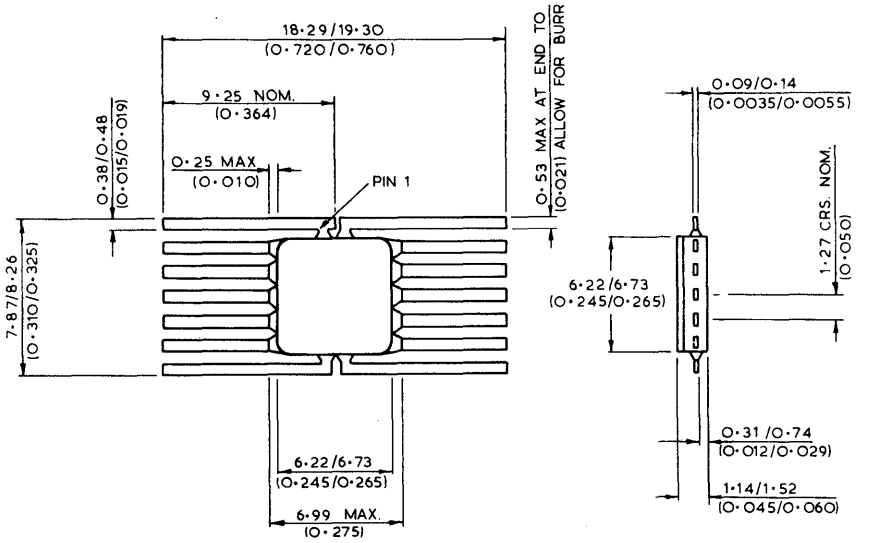


16 LEAD PLASTIC DIL

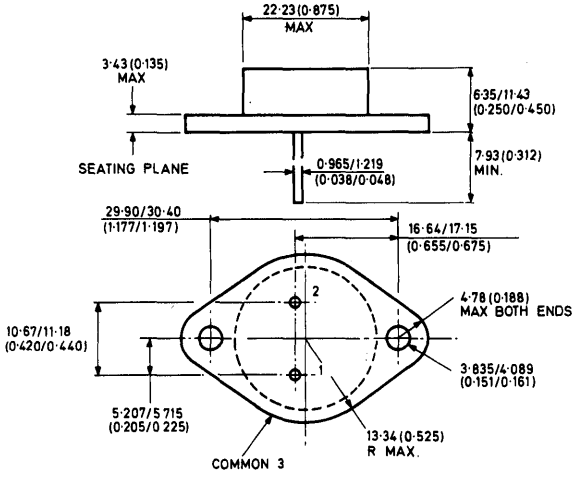
DP16



GM10 10 LEAD FLAT PACK



GM14 14 LEAD FLAT PACK



NOTE : CASE IS THIRD ELECTRICAL CONNECTION

TO-3

KM 3

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