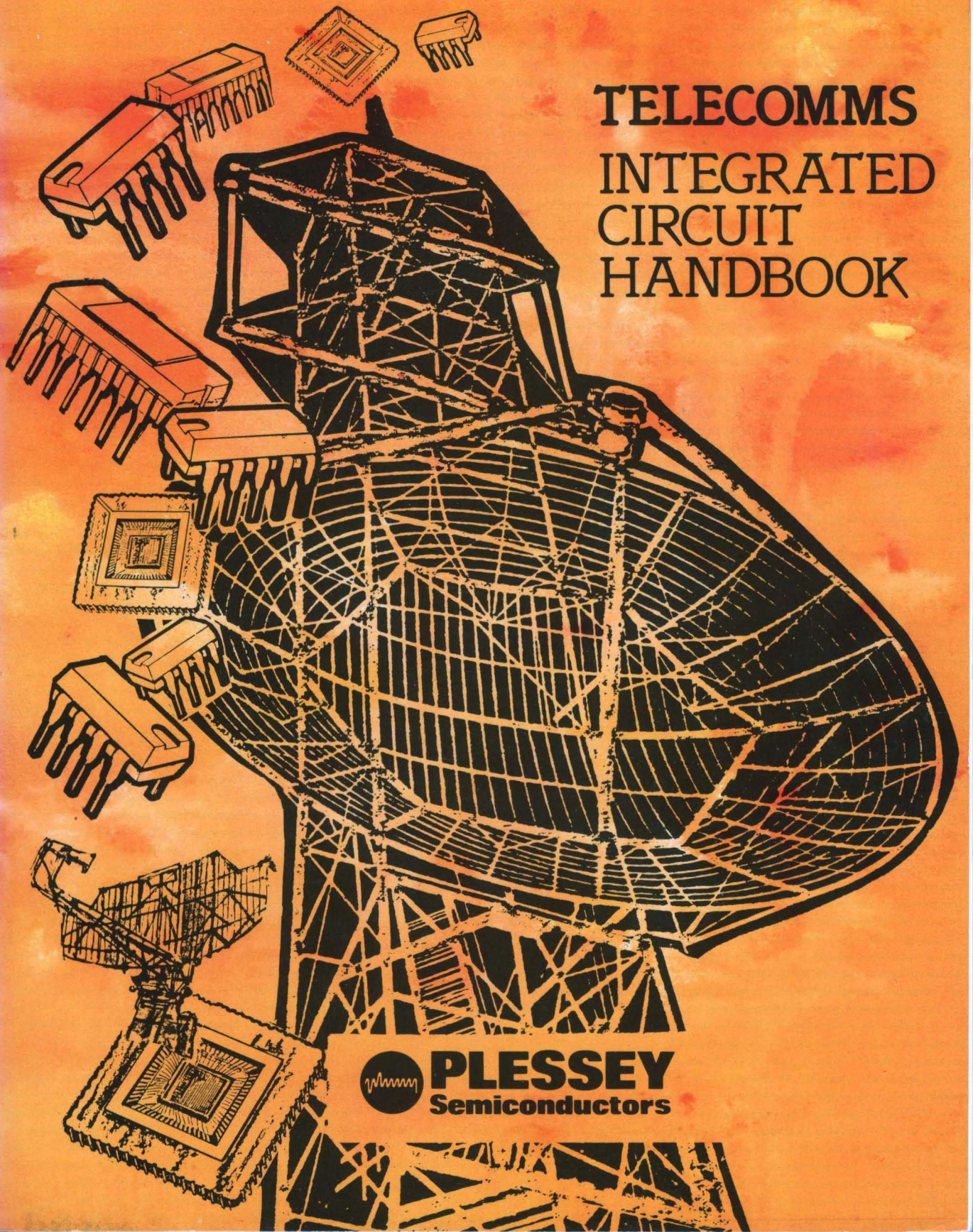
TELECOMMS
INTEGRATED CIRCUIT HANDBOOK



PLESSEY
Semiconductors

TELECOMS INTEGRATED CIRCUIT HANDBOOK

PLESSEY
Semiconductors

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EXP products are new designs designated 'Experimental' but which are, nevertheless, serious development projects. Details given may, therefore, change without notice and no undertaking is given or implied as to future availability. Please consult your local Plessey sales office for details of the current status

Selection guide

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The quality concept

In common with most semiconductor manufacturers, Plessey Semiconductors perform incoming piece parts check, in-line inspections and final electrical tests. However, quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes - followed by strict control and ongoing assessment to ensure that design requirements are still being met - that quality products will be produced.

In line with this philosophy, all designs conform to standard layout rules (evolved with performance and reliability in mind), all processes are thoroughly evaluated before introduction and all new piece part designs and suppliers are investigated before authorisation for production use.

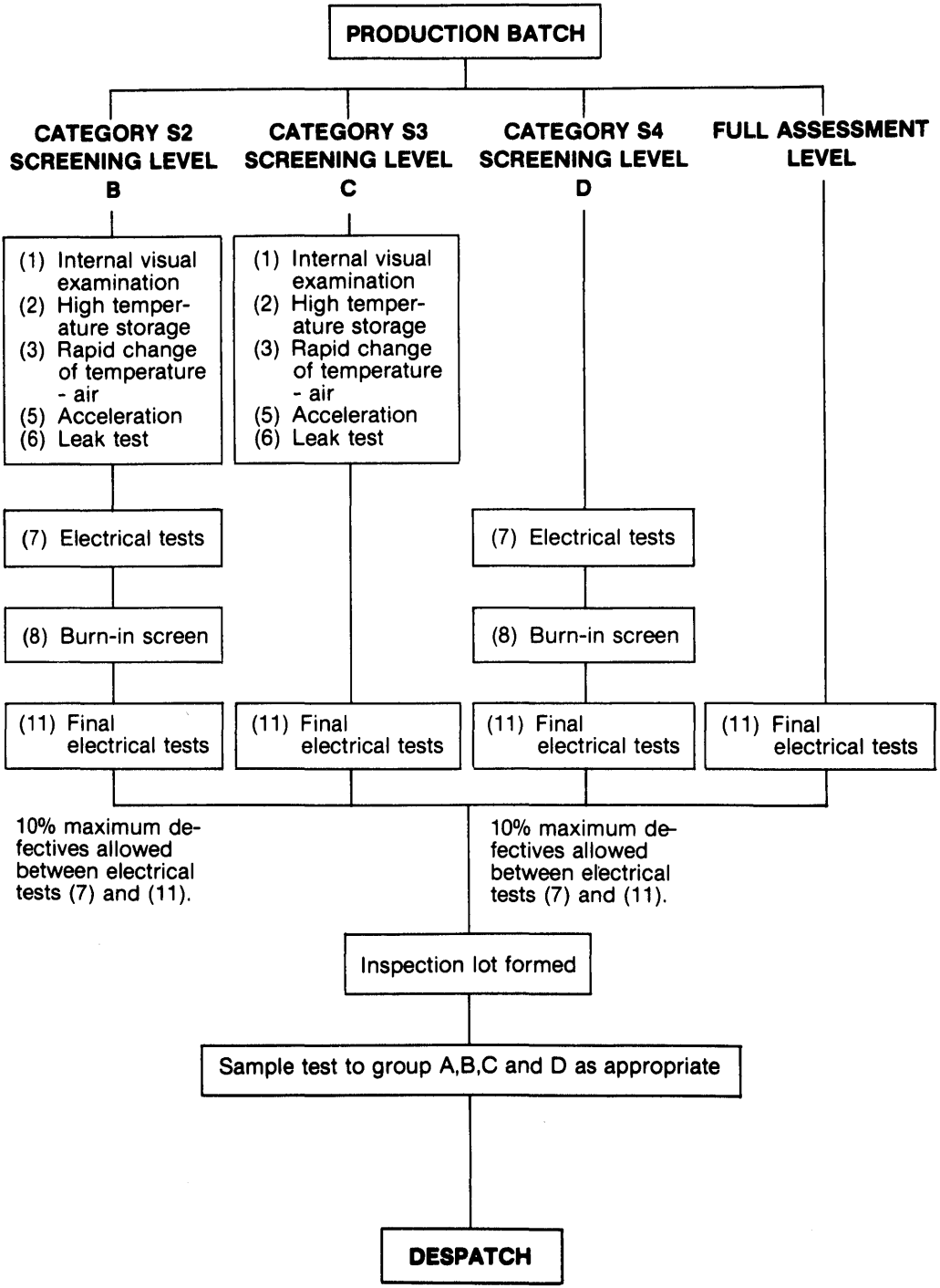
The same basic system of evaluation, appraisals and checks is used on all products up to and including device packing for shipment. It is only at this stage that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures for materials and processes for all types of customers advantages accrue to all users - the high reliability user gains the advantage of scale hence improving the confidence factor in the quality achieved whilst the large scale user gains the benefits associated with basic high reliability design concepts.

Plessey Semiconductors have the following factory approvals. **BS9300** and **BS9400** (BSI Approval No. 1053/M).
DEF-STAN 05-21 (Reg. No. 23H POD).

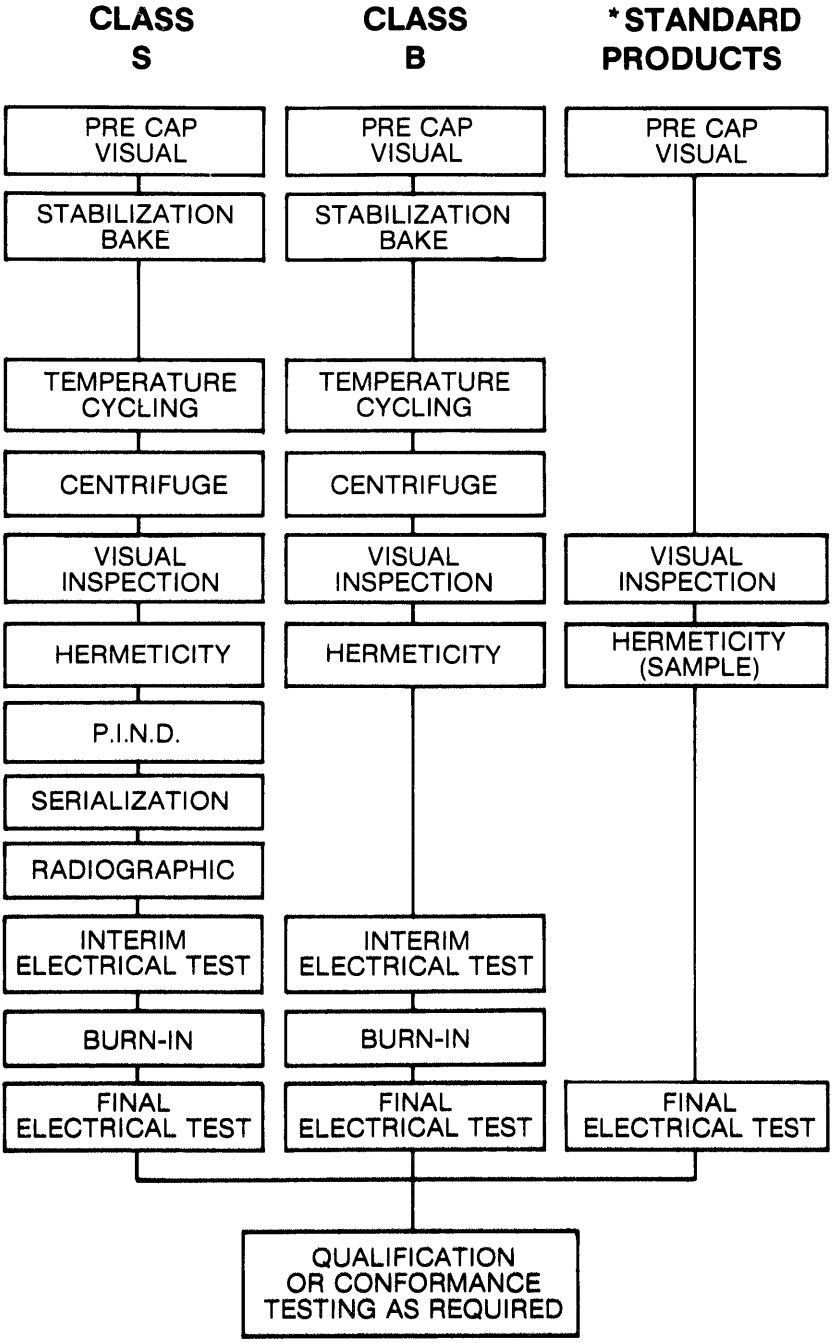
In addition a number of U.S., European and British customers manufacturing electronics for space have approved our facilities.

Screening to BS9400



Plessey Hi-Rel screening

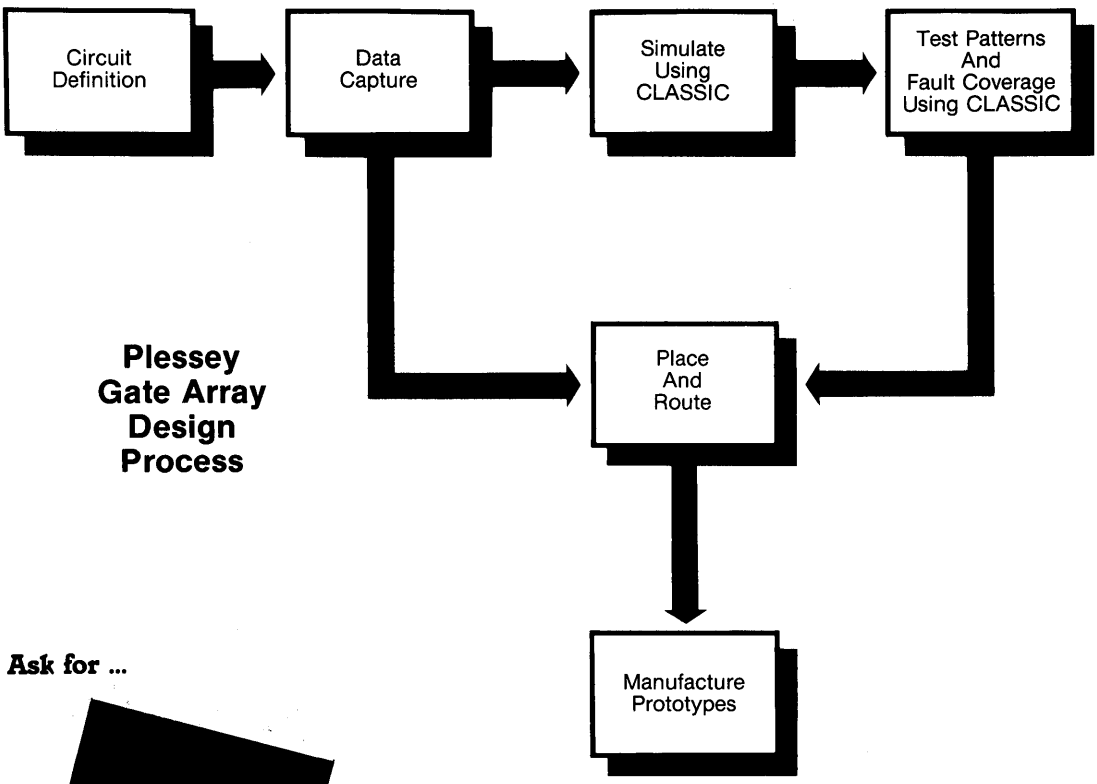
The following Screening Procedures are available from Plessey Semiconductors.



* Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

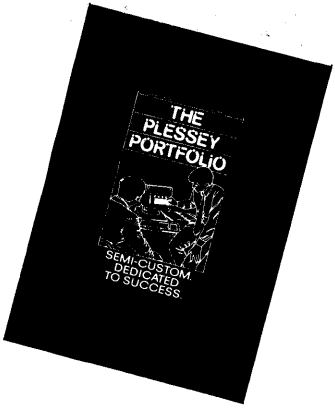
Semi-custom design

Plessey Semiconductors' advanced work in the Semi-Custom field enables us to offer our customers the opportunity to develop their own high performance circuits using our CLASSIC software. Among the many advantages are:
• CLASSIC is cost effective and user friendly • Prototypes in 6 weeks • Close coordination with customer throughout design and production process • State-of-the-art high performance produces • Up to 10044 gates available



Plessey Gate Array Design Process

Ask for ...



Microgate-C (Si-Gate CMOS)

CLA 2000 SERIES

- Double layer metallisation
- 5 micron channel length
- Product family:
  CLA 21XX 840 Gates
  CLA 23XX 1400 Gates
  CLA 25XX 2400 Gates
- 7ns max. prop delay (2 input NAND fanout of 2 with 2mm track 0-70° C 4.5-5.5V)
- 14MHz system clock rate
- 30MHz toggle rate
- Fully auto-routed

CLA 3000 SERIES

- Double layer metallisation
- 4 micron channel length
- Product family:
  CLA 31XX 840 Gates
  CLA 33XX 1440 Gates
  CLA35XX 2400 Gates
  CLA 37XX 4200 Gates
  CLA 39XX 6000 Gates
- 5ns max. prop delay
- 20MHz system clock rate
- 50MHz toggle rate
- Fully auto-routed

CLA 5000 SERIES

- Double layer metallisation
- 2 micron channel length
- Product family:
  CLA 51XX 640 Gates
  CLA 52XX 1232 Gates
  CLA 53XX 2016 Gates
  CLA 54XX 3060 Gates
  CLA 55XX 4408 Gates
  CLA 56XX 5984 Gates
  CLA 58XX 8064 Gates
  CLA 59XX 10044 Gates
- 2.5ns max. prop delay
- 40MHz system clock rate
- 100MHz toggle rate
- Fully auto-routed

Plessey Megacell™

Now there's a VLSI design system available that's perfect for solving your Application Specific Integrated Circuit (ASIC) problems. It's **PLESSEY MEGACELL** - a complete set of advanced computer-aided engineering and design tools coupled with an advanced CMOS process for implementing VLSI integrated circuits in the system design environment.

PLESSEY MEGACELL redefines semicustom integrated circuit design. It allows system engineers to design complex circuits with a high level of confidence of first time success in silicon - thanks to one of the best simulation facilities available in the world. This greatly reduces time to market, eliminating the many prototyping iterations that are all too common now in VLSI design.

PLESSEY MEGACELL is just about as close as you can get to achieving hand-crafted results short of full custom itself. System engineers can directly create their designs using the advanced layout and routing tools provided - without the aid of integrated circuit designers. So none of the system designers' application expertise is ever lost in transition, while chips of the smallest size and lowest production cost are regularly achieved.

Supporting the **PLESSEY MEGACELL** design capability is one of the most advanced CMOS processes available. It uses a 2-micron geometry capable of providing performance comparable with advanced Schottky TTL, with clock speeds to 40MHz and toggle rates of 100MHz achievable. And Plessey has established a 200,000 square foot dedicated processing facility to guarantee the manufacturing capacity required by even the most aggressive volume considerations.

PLESSEY MEGACELL is truly the gateway to the future - custom VLSI performance, with confidence of first time success and fast time to market. And it's going to stay that way - with Plessey's commitment to add future capabilities for high-speed ECL processes, 1 micron and submicron CMOS processes, and advanced analog capabilities.

Thermal design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$\theta_{ja} = \theta_{jc} + \theta_{ch} + \theta_{ha}$

where θ_{ja} is thermal resistance junction-to-ambient °C/W
θ_{jc} is thermal resistance junction-to-case °C/W
θ_{ch} is thermal resistance case-to-heatsink °C/W
θ_{ha} is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{ja})$
T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

A device is to be used at an ambient temperature of +50° C. θ_{ja} for the DG14 package with a chip of approximately 1mm sq is 107° C/W. Assuming the datasheet for the device gives P_D = 330mW and T_j max = 175° C.

$T_j = T_{amb} + P_D \theta_{ja}$
$= 50 + (0.33 \times 107)$
$= 85.31°C$ (typ.)

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Thermal design (cont'd)

Example 2

A device with T_{amb} max. = +175° C is to be used at an ambient temperature of +150° C. Again, θ_{ja} = 107° C/W, P_D = 330mW and T_j max. = +175° C.

$$T_j = 150 + (0.33 \times 107)$$
$$= +185.3° C \text{ (typ.)}$$

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{ja} is the sum of the individual thermal resistances; of these, θ_{jc} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{ca}, can be reduced.

If θ_{ca}, and therefore θ_{ja}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{ja} of 55° C/W for the DG14 package. Using this heatsink with the device operated as in Example 2 would result in a junction temperature given by:

$$T_j = 150 + (0.33 \times 55)$$
$$= 168° C$$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{jc} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{jc} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

Technial data

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MJ1410

8 BIT FORMAT CONVERTER

The MJ1410 is realised in N-channel MOS technology and operates from a single 5V supply. The circuit can be clocked from d.c. up to 2.5MHz and has 3-state output buffers capable of driving two LSTTL loads. All inputs are TTL compatible.

The MJ1410 performs the complementary functions of serial-to-parallel and parallel-to-serial data conversion on 8 bits of data. Both these conversions are achieved using the same time-position matrix, which has eight inputs and eight outputs.

An 8-bit parallel word clocked into the eight inputs appears as a serial 8-bit data stream on one of the eight outputs. Successive parallel words at the inputs appear as serial data streams on each of the eight outputs in turn.

Conversely, a serial 8-bit data stream on one of the eight inputs appears as an 8-bit parallel word on the eight outputs. Successive parallel words appearing at the eight outputs correspond to the serial data on each of the eight inputs in rotation.

The conversion can be 'programmed' to start in any register by setting the appropriate binary value on the counter pre-load inputs and applying a pulse to the Sync input. If the loading sequence produced by the counter is not required it can be disabled by connecting 'clock' to 'sync'. At each positive clock edge the register loaded will depend on the data on the counter inputs on the previous positive clock edge.

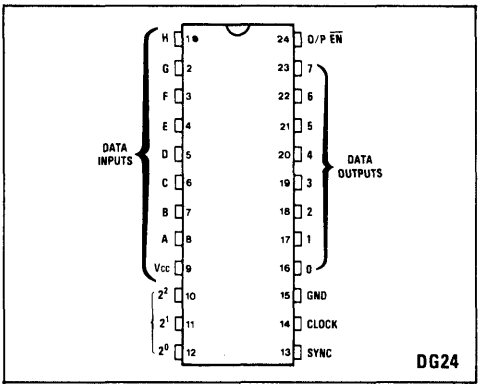

Fig.1 Pin connections

FEATURES

- Single 5V supply.
- Three-state outputs.
- All inputs TTL compatible.

FUNCTIONAL DESCRIPTION

Pin No.	Title	Function
1	H	Data i/p H
2	G	Data i/p G
3	F	Data i/p F
4	E	Data i/p E
5	D	Data i/p D
6	C	Data i/p C
7	B	Data i/p B
8	A	Data i/p A
	Data inputs	See Figs. 3 and 4
9	Vcc	Positive supply, 5V ± 5%
10	2^2	Counter preset i/p bit 2
11	2^1	Counter preset i/p bit 1
12	2^0	Counter preset i/p bit 0
		The counter is preset to the data on these i/ps on the 3rd positive clock edge following a negative edge on the 'sync' input.
13	SYNC	A negative edge on this i/p initiates the counter preset sequence which causes the conversion cycle to start in the register which corresponds to the binary value of the counter preset i/ps.
14	CLOCK	System clock
15	GND	Zero volts
16	0	Three state data o/p '0'
17	1	Three state data o/p '1'
18	2	Three state data o/p '2'
19	3	Three state data o/p '3'
20	4	Three state data o/p '4'
21	5	Three state data o/p '5'
22	6	Three state data o/p '6'
23	7	Three state data o/p '7'
	Data outputs	See Figs. 3 and 4
24	O/P $\overline{EN}$	A logic '1' on this i/p forces all the data outputs to a high impedance state.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{CC} = 5V, T_{amb} = 22°C ± 2°C, Test circuit: Fig. 6.
Supply voltage V_{CC} 5V ± 10%
Ambient operating temperature T_{amb} -10°C to +70°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level I/P voltage	V_{IL}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	-0.3		0.8	Volts	
High level I/P voltage	V_{IH}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	2.5		V_{CC}	Volts	
Low level I/P current/high level I/P current	I_{IN}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24		1	50	µA	
Low level O/P voltage	V_{OL}	16,17,18, 19,20,21, 22,23			0.5	Volts	I_{SYNC} = 1.6mA
High level O/P voltage	V_{OH}	16,17,18, 19,20,21, 22,23	2.5			Volts	I_{SOURCE} = 100uA
Low level O/P current sink capability	I_{OL}	16,17,18, 19,20,21, 22,23	-1.6			mA	
High level O/P current source capability	I_{OH}	16,17,18, 19,20,21, 22,23	100			µA	
OFF state O/P current	$I_{OFF\ L}$	16,17,18, 19,20,21, 22,23			40	µA	V_{OUT} = GND
	$I_{OFF\ H}$	16,17,18, 19,20,21, 22,23			-40	µA	V_{OUT} = V_{CC}
Power dissipation	P_{DISS}		90		500	mW	V_{CC} = 5.5V

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max.clock frequency	$F_{max.}$	2.4		10	MHz	
Min. clock frequency	$F_{min.}$	0			MHz	
Sync. pulse width (positive)	t_{SPP}	60			ns	Fig. 6
Sync. pulse width (negative)	t_{SPN}	100			ns	Fig. 6
Lead of sync. clocking edge on positive clock edge	t_{SL}	130			ns	Fig. 6
Set up time of counter inputs (2^0,2^1,2^2)	t_{SC}	70			ns	Fig. 6
Hold time of counter inputs	t_{HC}	60			ns	Fig. 6
Set up time of data inputs (A-H)	t_{SD}	80			ns	Fig. 6

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Hold time of data inputs	t_{HD}	85			ns	Fig. 6
Propagation delay, data out valid from output $\overline{\text{ENABLE}}$ low	t_{PDE}			100	ns	Fig. 6
Propagation delay, data out disabled from output $\overline{\text{ENABLE}}$ high	t_{PDD}			100	ns	Fig. 6
Propagation delay, clock to data out valid	t_{PCD}			200	ns	Fig. 6

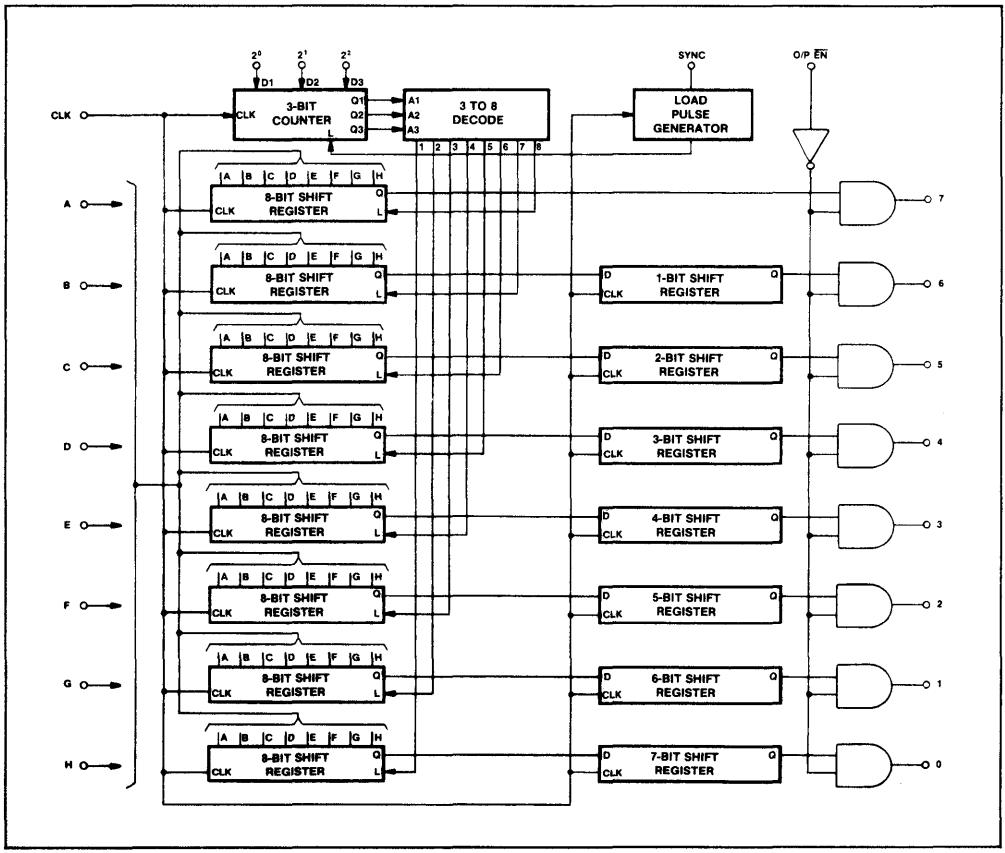

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin w.r.t. ground = 7V max.
Storage temperature = -55°C to +125°C

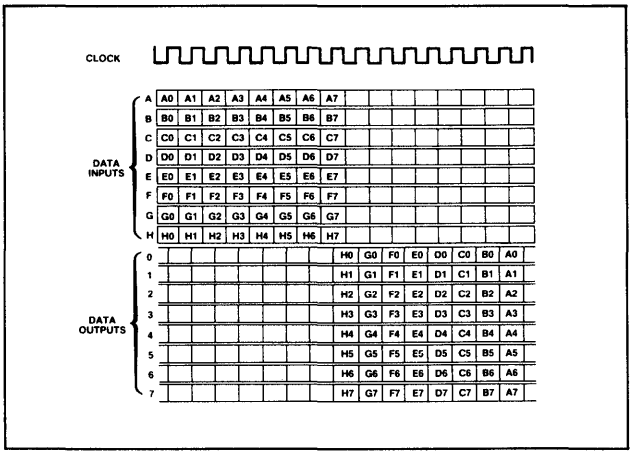

Fig.3 Data conversion

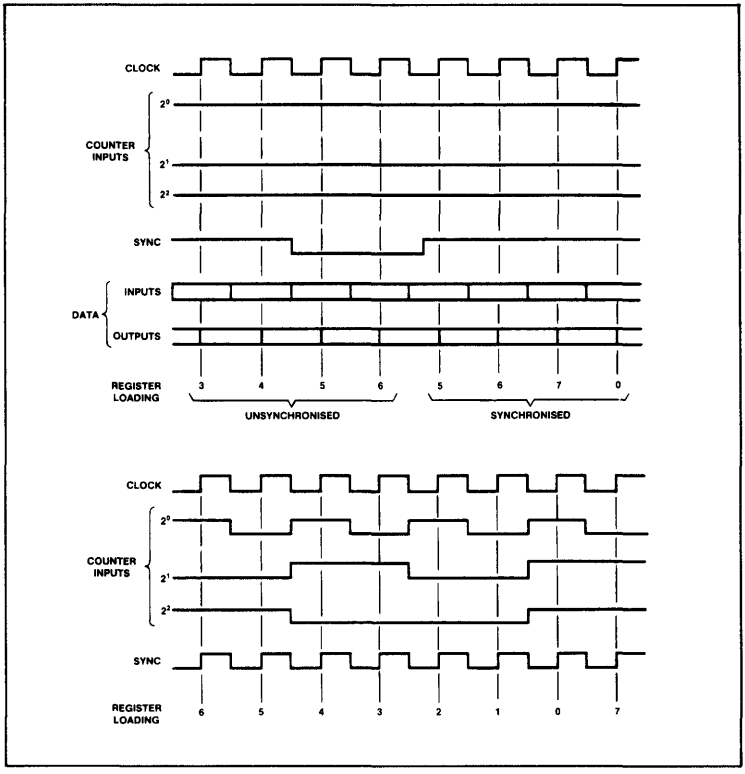

Fig.4 Input and output waveforms

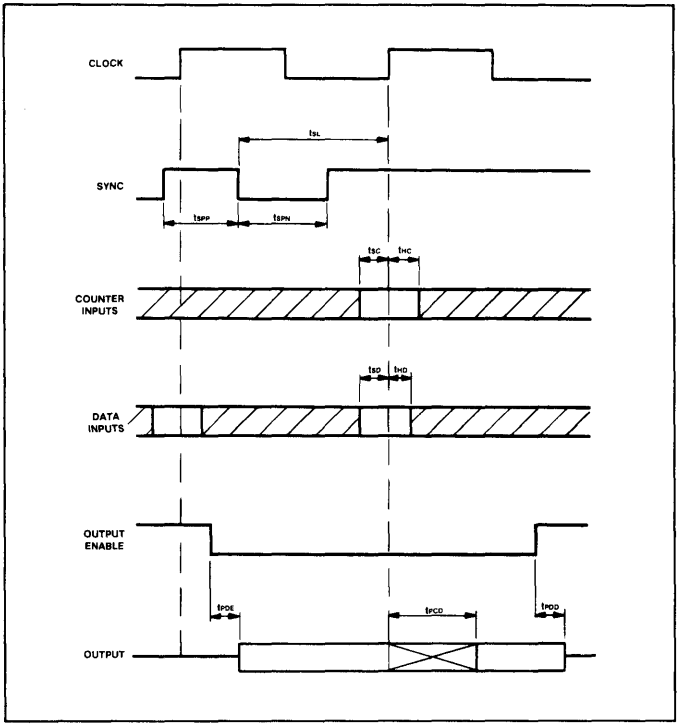

Fig.5 Timing details

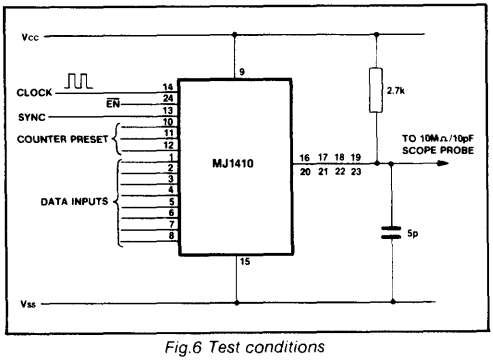

Fig.6 Test conditions

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2 MBIT PCM SIGNALLING CIRCUIT
MJ 1440
HDB3 ENCODER/DECODER

The 2.048 MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply, relevant inputs and outputs are TTL compatible.

The MJ1440 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeroes detection). In addition a loop back function is provided for terminal testing.

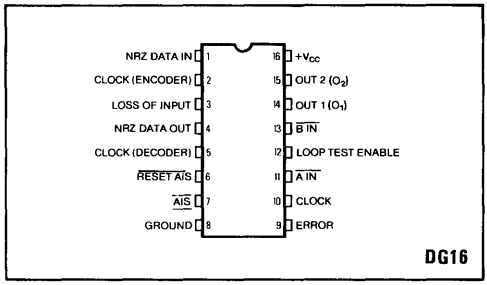

Fig. 1 Pin connections

FEATURES

- 5v ± 5% Supply −50mA Max
- HDB3 Encoding and Decoding to CCITT rec. G703.
- Asynchronous Operation.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal Generated from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector).
- Decode Data in NRZ Form.

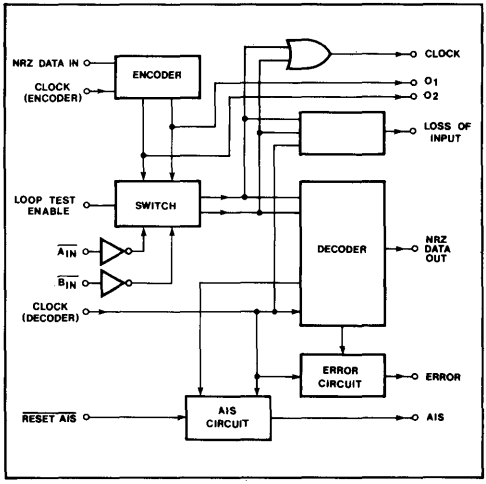

Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
40°C/Watt	120°C/Watt

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = 0°C$ to $+70°C$

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,5,6 10,11,12,13	-0.3		0.8	V	
Low level input current	I_{IL}				50	µA	$V_{IL} = 0V$
High level input voltage	V_{IH}		2.5		V_{cc}	V	
High level input current	I_{IH}				50	µA	$V_{IH} = 5V$
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 80µA
		3,4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	3,4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	50	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0			MHz	Figs.10, 15
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2			MHz	Figs.11, 15
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.10, 15. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.10, 15
tpd1A-tpd1B				20	ns	Figs.10, 15
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = Figs.13, 15
Setup time of NRZ data in to Clock (Encoder)	ts3	30			ns	Figs.8, 10, 15
Hold time of NRZ data in	th3	55			ns	Figs.10, 15
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.9, 13, 15
Propagation delay Clock (Decoder) to loss of input				150	ns	
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.12, 15
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.14, 15
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.9, 11, 15. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.9, 11, 15
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.9, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	100			ns	Figs.9, 14, 15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	200			ns	Figs.9, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2	0			ns	Figs.14, 15

NOTES
1. Encoded HDB3 outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4).

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1. NRZ Data in
Input data for encoding into ternary HDB3 form. The NRZ data is clocked by the negative edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1

3. Loss of input alarm
This output goes to logic '1' if eleven consecutive zeroes are detected in the incoming HDB3 data. The output is set to logic '0' on receipt of a '1'.

4. NRZ data out
Decoded data in NRZ form from ternary HDB3 input data (A_{in},B_{in}), data is clocked out by positive going edge of clock (Decoder).

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6, 7. Reset AIS, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}}$ = 1 periods.
Logic '1' on Reset AIS enables the internal decoded zero counter.

8. Ground
Zero volts

9. Error
A logic '1' indicates that a violation of the HDB3 coding has been received i.e. 3 '1's of the same polarity.

10. Clock
'OR' function of $\overline{A_{in}}$,$\overline{B_{in}}$ for clock regeneration when pin 12 = '0'. 'OR' function of O_1,O_2 when pin 12 = '1'.

11,13. $\overline{A}_{in}$,$\overline{B}_{in}$
Inputs representing the received ternary HDB3 PCM signal. $\overline{A_{in}}$ = '0' represents a positive going '1', $\overline{B_{in}}$ = '0' represents a negative going '1'. $\overline{A_{in}}$ and $\overline{B_{in}}$ are sampled by the positive going edge of the Clock (Decoder). $\overline{A_{in}}$ and $\overline{B_{in}}$ may be interchanged.

12. Loop test enable
Input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 12 = '1' O_1 is connected internally to A_{in}. O_2 is connected internally to B_{in}. Clock becomes the OR function $O_1 + O_2$. The delay from NRZ in to NRZ out is 6½ clock periods in the loop back condition.

14, 15. O_1, O_2
Outputs representing the ternary encoded data for line transmission O_1 = '1' representing a positive going '1', O_2 = '1' represents a negative going '1'. O_1 and O_2 may be interchanged.

16. V_{cc}
Positive supply, 5V ± 5%

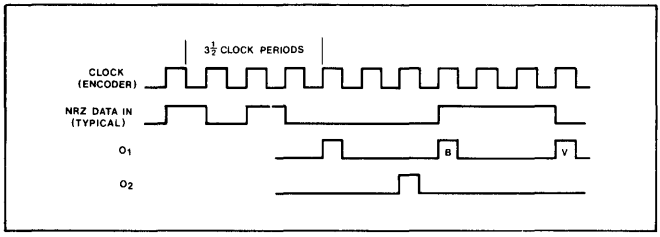

Fig. 3 Encode waveforms

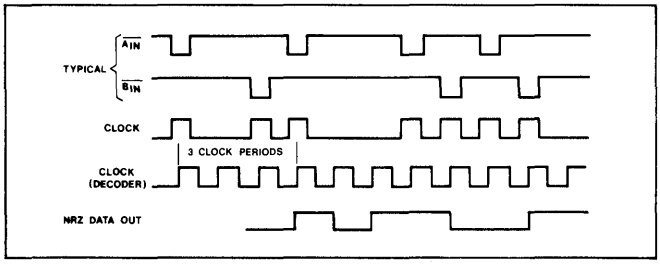

Fig. 4 Decode waveforms

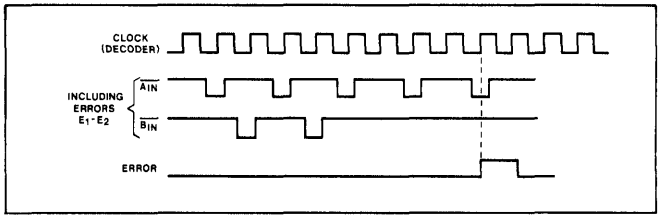

Fig. 5 HDB3 error output waveforms

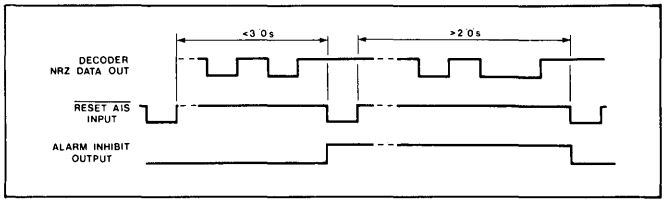

Fig. 6 AIS error and reset waveforms

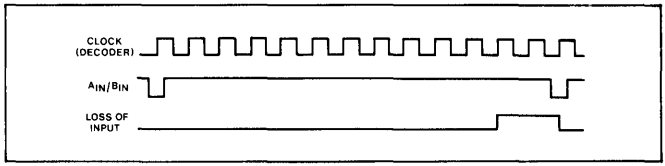

Fig. 7 Loss of input waveforms

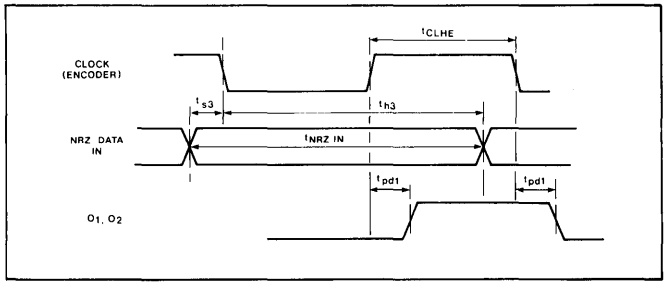

Fig. 8 Encoder timing relationship

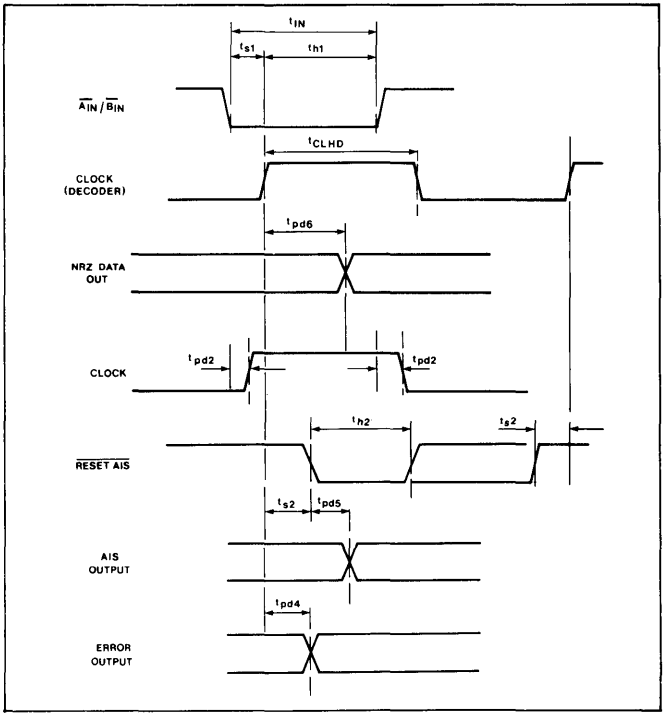

Fig. 9 Decoder timing relationship

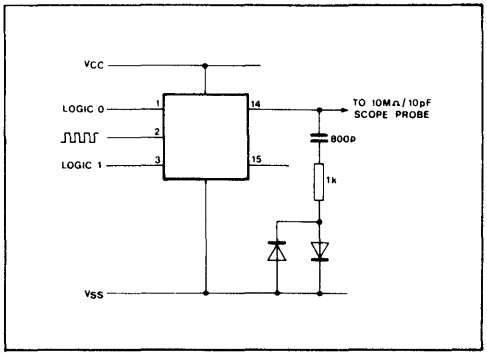

Fig. 10

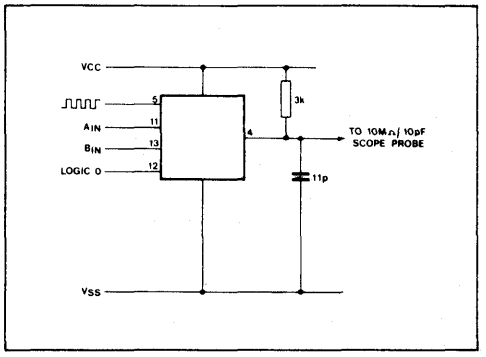

Fig. 11

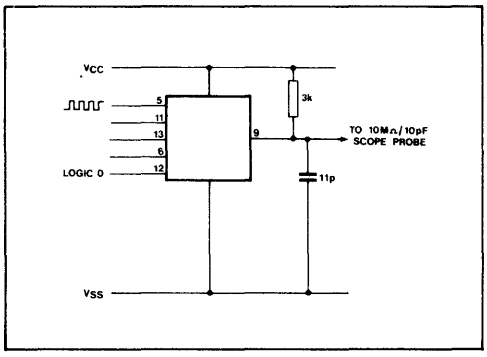

Fig. 12

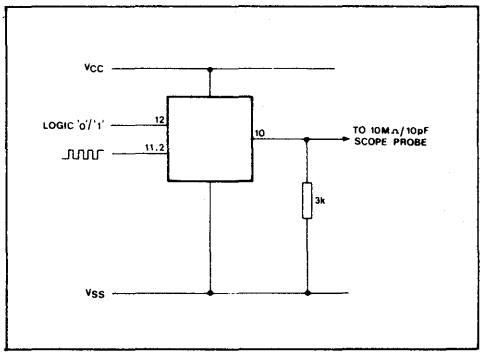

Fig. 13

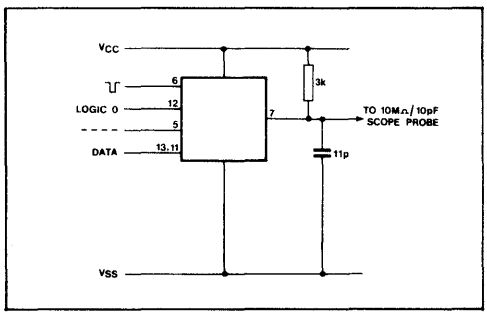

Fig. 14

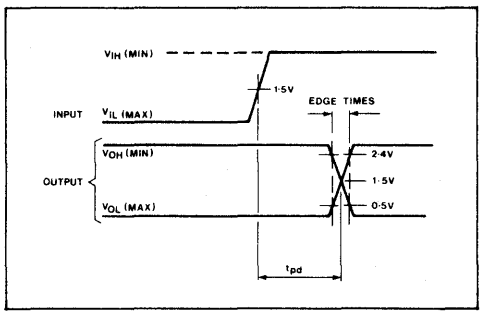

Fig. 15 *Test timing definitions*

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.
This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ 1444

PCM SYNCHRONISING WORD GENERATOR

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1444 generates the synchronising word in accordance with CCITT recommendations G732. The MJ1445 has been designed to detect this synchronising word when received at the remote end of the transmission system.

The synchronising word is injected onto the PCM data highway during time slot 0 in alternate frames. The spare time slot 0 data bits, bit 1 in every frame and bits 3 to 8 inclusive in alternate frames (i.e. those not containing the synchronising word) are available as parallel inputs and are output onto the PCM data highway.

The data output of the MJ1444 is 'open collector' and can be wire-OR'd directly onto the highway.

The device also provides a time slot 0 channel pulse 'TS0', time slot 0 non-sync. frame 'TS0 $\overline{SF}$', and time slot 16 'TS16' outputs.

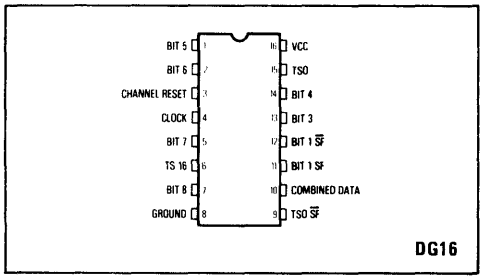

Fig.1 Pin connections

FEATURES

- 5V ± 5% Supply — 20mA Typical
- Fully Conforms to CCITT Recommendation G732
- Outputs Directly Onto PCM Data Highway
- Provides Both Time Slot 0 and Time Slot 16 Channel Pulses
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

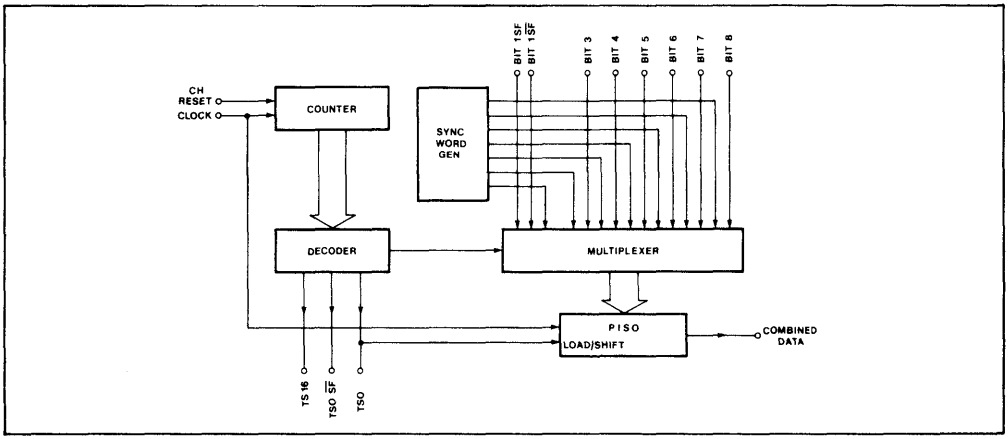

Fig.2 MJ1444 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient operating temperature -10°C to +70°C

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	1, 2, 3, 4, 5, 7, 11, 12, 13, 14.	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}		
Low level output voltage	V_{OL}	6, 9, 15			0.5	V	$I_{sink} = 2mA$
		10			0.7	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	6, 9, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{OH}	10			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max clock frequency	F_{max}	3			MHz	
Propagation delay, clock to TS0, TS0 $\overline{SF}$, TS16 and combined data outputs.	t_p	80		200	ns	See Figs.5 and 6
Set up time channel reset to clock	T_{S1}	100		450	ns	$f_{clock} = 2.048MHz$
Hold time of channel reset input	t_{H1}	20		400	ns	
Set up time of bit 1 (SF) to datum B	t_{S2}	100			ns	
Hold time of bit 1 (SF) wrt datum B	t_{H2}	300			ns	
Set up time of bit 1 ($\overline{SF}$) and data bits 3—8 to datum B	t_{S2}	100			ns	
Hold time of bit 1 ($\overline{SF}$) and data bits 3—8 wrt datum B	t_{H2}	300			ns	

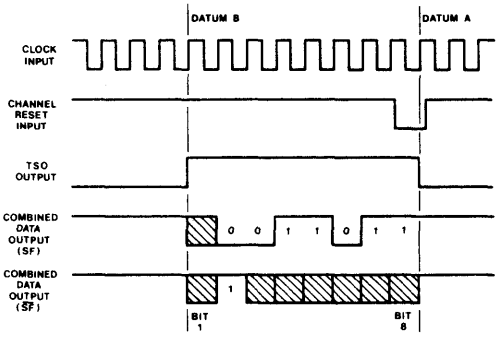

Fig.3 Data timing

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1, 2, 5, 7, 13, 14. Bits 3 to 8
Parallel data on these inputs is asynchronously loaded into bits 3 to 8 of the PISO shift register for transmission during Time slot 0 of non-sync. frames.

3. Channel Reset
A low going pulse at this input synchronises the MJ1444 with the other devices at the transmit end of the PCM link. It may be applied as a start pulse or repeated at the same instant in successive frames.

4. Clock
System clock input (2.048MHz for a 2 Mbit PCM system).

6. TS16
This output provides a positive pulse equivalent to 8 clock periods during time slot 16 of every 30 + 2 channel PCM frame.

8. GND
Zero volts.

9. TS0 $\overline{SF}$
This output provides a positive pulse equivalent to 8 clock periods during time slot 0 of non-sync. frames.

10. Combined data
This 'open collector' output injects the contents of the PISO shift register onto the PCM data highway during time slot 0 in successive frames. The contents of the PISO shift register are defined as follows:

	Bit 1	2	3	4	5	6	7	8
Sync. Frame	X	0	0	1	1	0	1	1
Non-sync. frame	X	1	X	X	X	X	X	X

X — indicates that these bits may be set according to the parallel data inputs.

11. Bit 1 SF
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of sync. frames.

12. Bit 1 $\overline{SF}$
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of non-sync. frames.

15. TS0
This output provides a positive pulse equivalent to 8 clock period during time slot 0 of every 30 channel PCM frame.

16. V_{CC}
Positive supply, 5V ±5%.

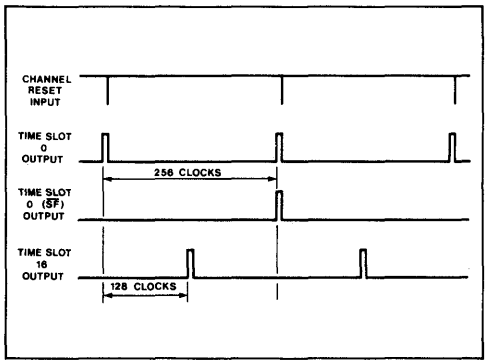

Fig.4 Sync. timing

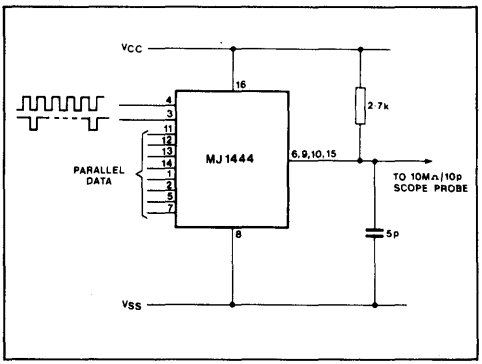

Fig.5 Test conditions (all outputs)

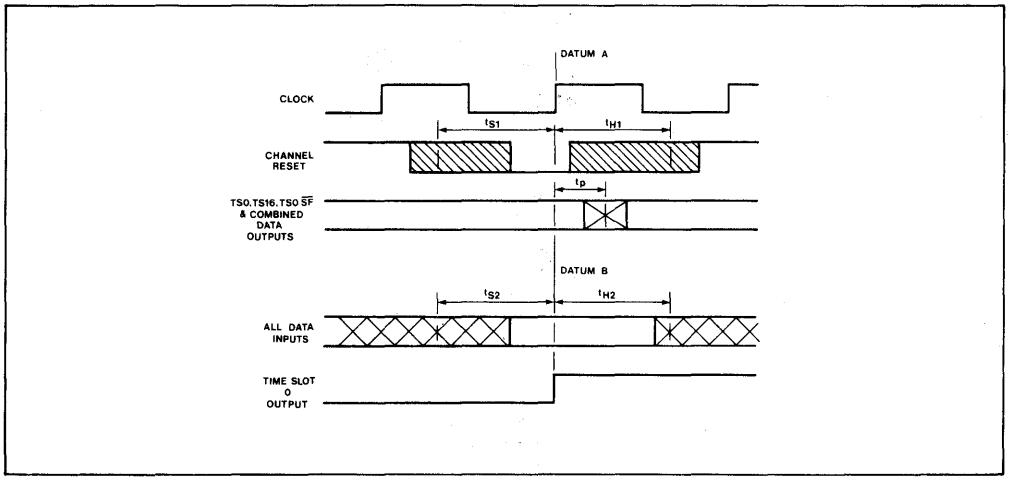

Fig.6 Timing definitions

PLESSEY
Semiconductors

PCM SYNCHRONISING WORD RECEIVER

MJ1445

2 MBIT PCM SIGNALLING CIRCUIT

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBii 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1445 establishes synchronisation by detecting the synchronising word when it is received at the remote end of the transmission system. The MJ1444 has been designed to generate this synchronisation word at the sending end of the system in accordance with CCITT recommendation G732.

Corruption of individual synchronisation words is signified by an 'Error' output, loss of synchronisation is indicated by a 'Sync Alarm' output and follows CCITT G732 in that loss of synchronism is assumed when 3 consecutive synchronisation words have been received with errors.

The 'Channel Reset' output goes low for the first period of the clock after time slot 0 in sync frames whenever the MJ1445 has established that the receiver terminal is in synchronisation in order that the rest of the receiver terminal may be reset.

The 'TSO' output is high for a period of 8 bits starting from the end of the first bit of the synchronising word. The spare data bits from the synchronising word are provided as parallel outputs.

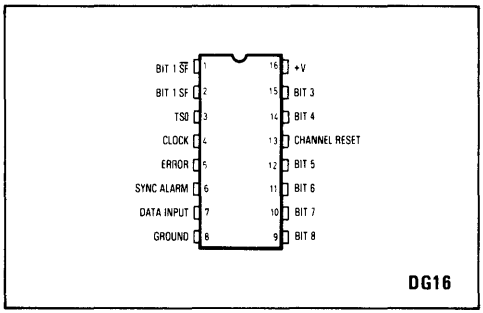

Fig.1 Pin connections

FEATURES

- 5V ±5% Supply - 20mA Typical.
- Conforms to CCITT Recommendation G732
- Synchronising Word Error Monitor
- Out of Sync. Alarm
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

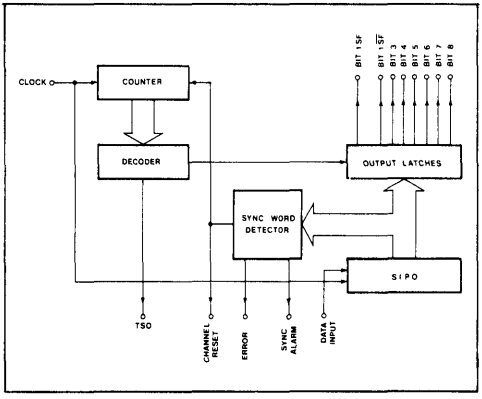

Fig.2 Block diagram MJ1445

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	4, 7	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	4, 7		1	50	μA	
High level input voltage	V_{IH}	4, 7	2.4		V_{CC}	V	
Low level output voltage	V_{OL}	1, 2, 3, 5, 6 9, 10, 11, 12 13, 14, 15			0.5	V	$I_{sink} = 2mA$
High level output voltage	V_{OH}		2.8				$I_{source} = 200\mu A$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock frequency	f_{max}	2.2			MHz	
Input delay of data input	$t_{d\ data}$	20		200	ns	$f_{clock} = 2.048MHz$
Propagation delay, clock to TS0 output	$t_{d\ TS0}$	40		200	ns	Fig.3
Propagation delay clock to error output, sync alarm and CH. Reset output high	t_d	50		400	ns	Fig.3
Propagation delay, clock to CH. Reset output low ($T - t_p$)	t_p	100		450	ns	Fig.3
Propagation delay clock to spare bits	$t_{d\ SB}$	50		300	ns	Fig.3

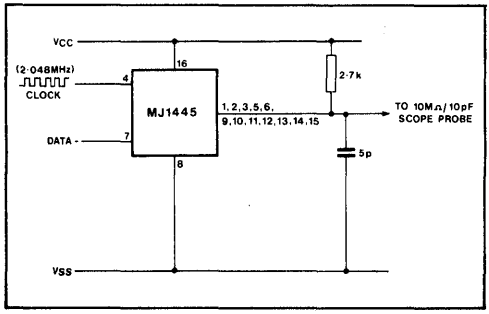

Fig.3 Test conditions, all outputs

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Bit 1 $\overline{SF}$
This output is set to the level of data bit 1 during time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

2. Bit 1 SF
This output is set to the level of data bit 1 during time slot 0 of sync frames. The data becomes true on the first falling edge of the clock during TS1.

3. TS0
This output provides a positive pulse of 8 clock periods in every frame starting from the end of the first bit of the synchronising word of the received data.

4. Clock
System clock input (2.048MHz for a 2MBit PCM system).

5.Error
This output goes high at the end of time slot 0 in the 2nd sync frame following the frame with sync word errors. If consecutive sync words occur with errors this output will remain high. If a sync alarm is generated this output will remain high until sync is regained.

6. Sync Alarm
This output goes high at the end of time slot 0 output in the 3rd consecutive sync frame containing sync word errors. It returns low at the end of TS0 output in the 3rd consecutive frame received correctly (sync and non sync).

7. Data Input
Serial data (2MBit/s) at this input is clocked through the SIPO shift register and examined by the sync word detector.

8. GND
Zero volts

9, 10, 11, 12, 14, 15. Bits 3 to 8
These parallel outputs are set to the level of the spare data bits (3 to 8) of time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

13. Channel reset
This output goes low for the first period of the clock after time slot 0 of the received data as long as synchronisation has been established. This pulse can be used to reset the rest of the receiver terminal.

16. V_{CC}
Positive supply $5V \pm 5\%$.

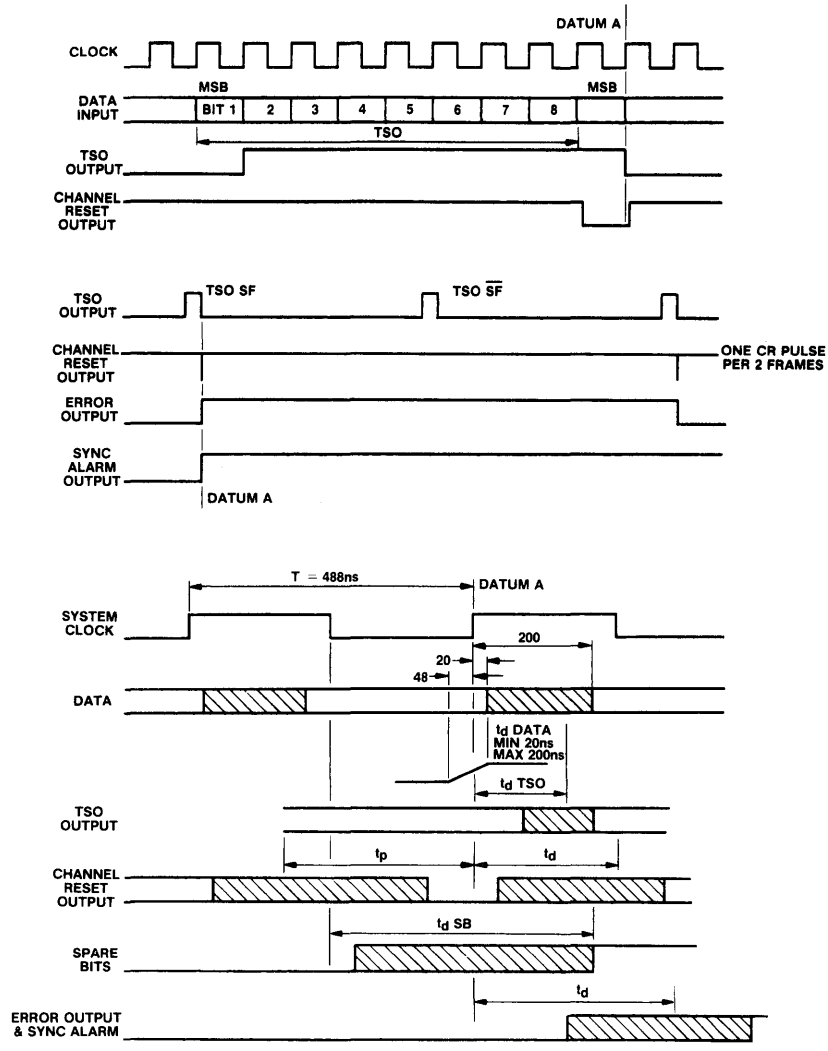

Fig.4 Timing diagram and output waveforms

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT
MJ1446
TIME SLOT 16 RECEIVER AND TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1446 has two modes of operation dependent on the state of the mode control input. With the mode control high the device is in the transmit mode and with the mode control low the device is in the receive mode.

In the transmit mode the device accepts 64k bits/sec signalling information in either binary or AMI format and outputs it at 2Mbits/sec on to the digital highway during time slot 16.

In the receive mode the device accepts 2Mbit/sec information from the digital highway, during time slot 16 and output is at 64kbits/sec in both binary and AMI format.

In both receive and transmit mode there is an AMI coded clock output, AMI output and $\overline{\text{AMI}}$ output which conforms to CCITT recommendation no G372 for a 64kbits/sec contradirectional interface. The alarm inhibit input causes the 8kHz timing signal to be removed from the AMI clock output.

The device is reset in both modes by a time slot 16 channel pulse and the alarm output provides an indication that the internal counter is operating correctly.

Also provided are 64kHz, 16kHz and 8kHz clock outputs.

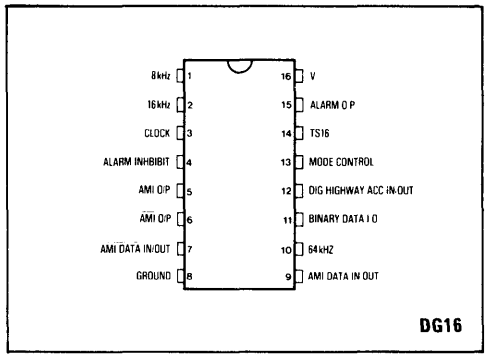

Fig.1 Pin connections

FEATURES

- 5V ±5% Supply — 20mA Typical
- Conforms to CCITT Recommendations
- Provides Both AMI and Binary Format Data Outputs
- Single Chip Receive or Transmit
- All Inputs and Outputs are TTL Compatible.

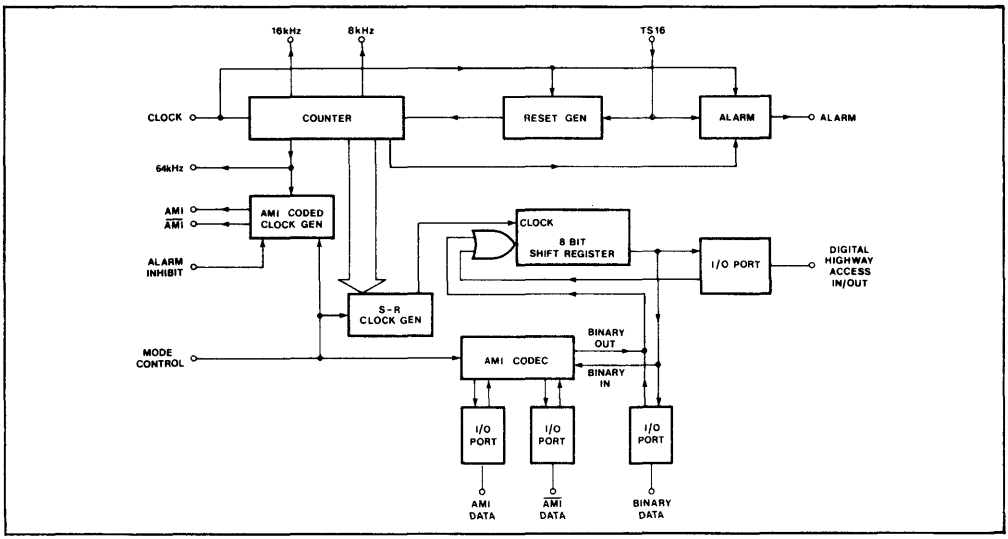

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	3, 4, 7, 9, 11, 12, 13, 14	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}	V	
Low level output	V_{OL}	1, 2, 5, 6, 7, 9, 10, 11, 15			0.5	V	$I_{sink} = 2mA$
		12			0.5	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	1, 2, 10, 5, 6, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{CH}	7, 9, 11, 12			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20		mA	$V_{CC} = 5.25V$

Dynamic Characteristics ($f_{clock} = 2.048MHz$)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propogation delay clock to data out to digital highway	t_p	20		200	ns	Fig.7
Propogation delay clock to 64kHz out	t_p	20		200	ns	Fig.7
Input delay, clock to digital highway access	$t_{d\,DATA}$	20		200	ns	
Input delay, clock to time slot 16	$t_{d\,TS16}$	80		200	ns	
Output delay 64kHz to 16kHz output	$t_{p\,16}$			70	ns	Fig.7
Output delay, 64kHz to 8kHz output	$t_{p\,8}$			170	ns	Fig.7
Output delay, 64kHz to binary data output (64kHz)	$t_{p\,BIN}$	20		450	ns	Fig.8
Output delay 64kHz to AMI, $\overline{AMI}$, AMI data & $\overline{AMI}$ data o/p's	$t_{p\,AMI}$	20		400	ns	Fig.8
Input delay, 64kHz to binary data in (64kHz)	$t_{d\,BIN}$			100	ns	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. 8kHz
8kHz square wave output.

2. 16kHz
16kHz square wave output.

3. Clock
System clock input (2.048MHz for a 2Mbit PCM system)

4. Alarm inhibit
A high level on this input inhibits the 8kHz timing signal on the AMI clock outputs.

5. AMI output
Alternative Mark Inversion coded 64kHz.

6. $\overline{AMI}$ output

7. $\overline{AMI}$ Data in/out
In the transmit mode 64kHz signalling data in AMI format is accepted at these inputs for output to PCM highway during time slot 16.

8. GND
Zero volts.

9. AMI Data in/out
In the receive mode data accepted from the PCM highway during time slot 16 appears on these outputs at 64kbits/sec in AMI format.

10. 64kHz
64kHz square wave output.

11. Binary data in/out
In the transmit mode 64k bit/sec signalling data in binary form is accepted at this input for output to the PCM data highway during time slot 16. In the receive mode data is accepted from the PCM highway during TS16 and appears at this output at 64k bits/sec in binary format.

12. Digital Highway access in/out
In the receive mode 2Mbit/sec signalling data is accepted at this input during time slot 16 from the PCM digital highway. In the transmit mode signalling data is output to the PCM digital highway during time slot 16 at 2Mbits/sec.

13. Mode control
A high level on this input causes the MJ1446 to operate in the transmit mode while a low level causes it to operate in the receive mode.

14. TS16
This input should be connected to time slot 16 channel pulse of the PCM system to synchronise the MJ1446 with the rest of the system.

15. Alarm output
A high level on this output indicates that the internal counter has stopped or is out of synchronisation with the time slot 16 channel pulse.

16 V_{CC}
Positive supply $5V \pm 5\%$.

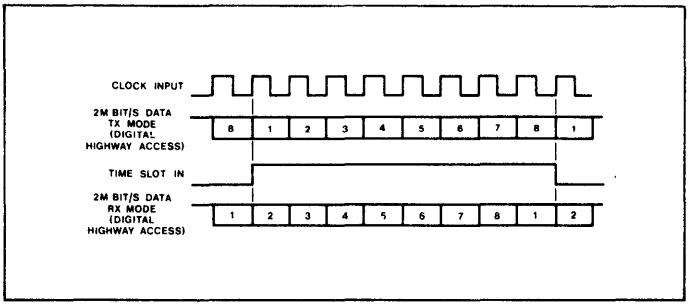

Fig.3 2MBit/s operation

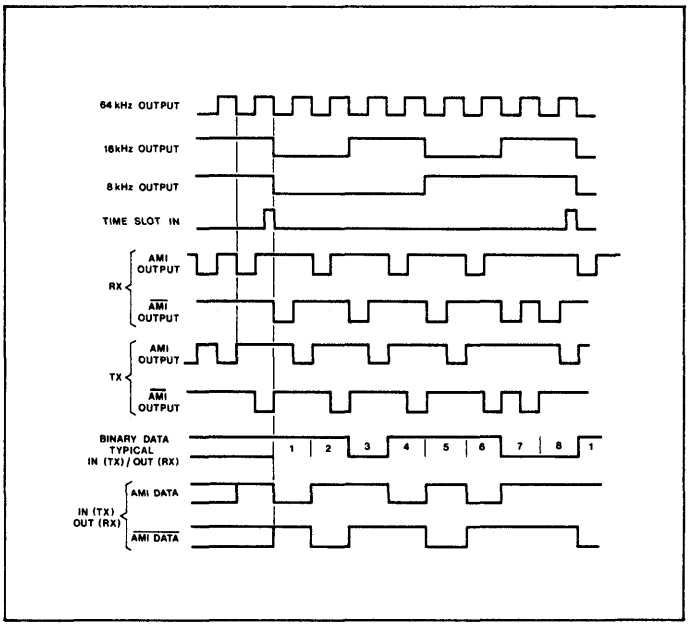

Fig.4 64kBit/s operation

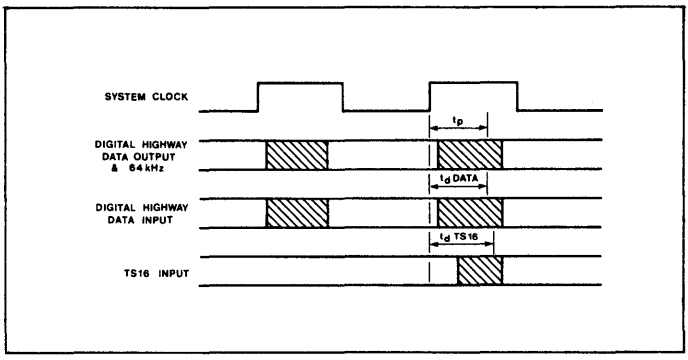

Fig.5 Timing diagram

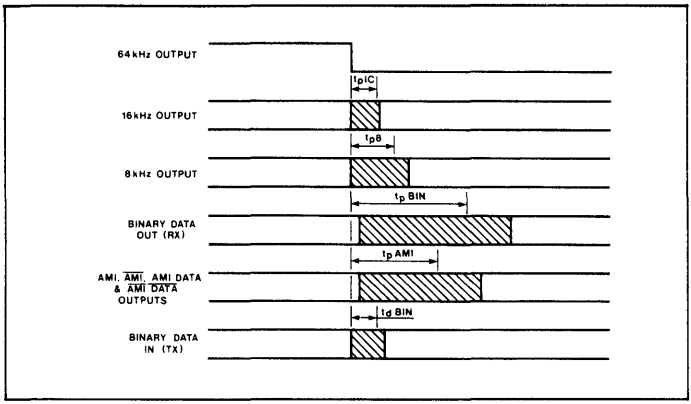

Fig.6 Timing diagram

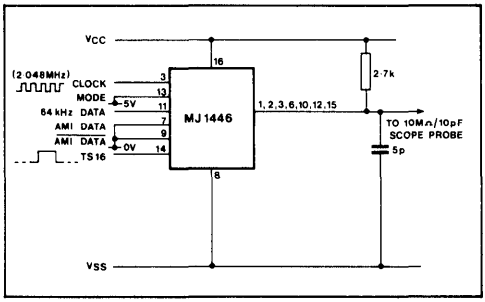

Fig.7 Test conditions (transmit mode)

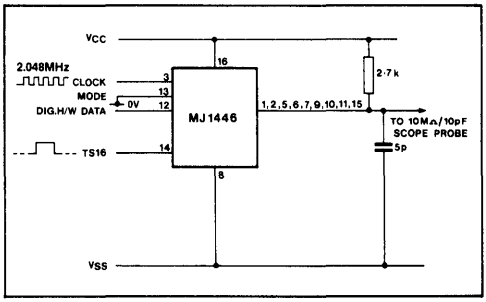

Fig.8 Test conditions (receive mode)

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ1471

HDB3 OR AMI ENCODER/DECODER

The MJ1471 is an encoder/decoder for pseudo-ternary transmission codes. The codes are true Alternate Mark Inversion (AMI) or AMI modified according to HDB3 rules (CCITT Orange Book Vol 111-2, Annex to Rec.G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding and all ones detection (AIS). In addition a loop test function is provided for terminal testing.

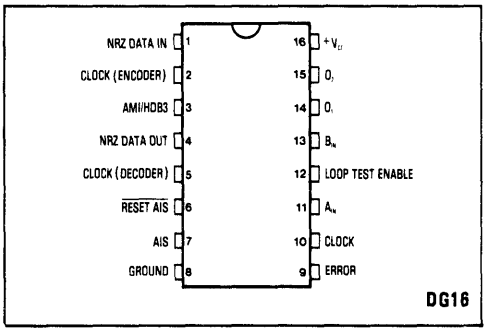

Fig.1 Pin connections

FUNCTIONS

- 5V ±5% Supply—40mA Max.
- AMI or HDB3 Operation—TTL Selectable
- Loop Back Facility
- 'All Ones' Error Monitor to Detect Loss of Synchronising Word (Time Slot Zero)
- Error Monitor of HDB3 Incoming Code
- Decoded Data in NRZ Form

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in
Input data for encoding into ternary form. The data is clocked by the negative-going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. AMI/HDB3
MJ1471 operates in HDB3 if pin 3 is at logic '1'. AMI if pin 3 is at logic '0'.

4. NRZ Data out
Decoded data from ternary inputs A_{in}, B_{in}.

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6, 7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}}$ = 1 periods.
Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground
Zero volts.

9. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been decoded i.e. 3 '1's of the same polarity.

10. Clock
OR function of A_{in}, B_{in} for clock regeneration when pin 12 = '0', OR function of O_1 O_2 when pin 12 = '1'.

11, 13. A_{in}, B_{in}
Inputs representing the received ternary PCM signal. A_{in} = '1' represents a positive going '1', B_{in} = '1' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the clock decoder. A_{in} and B_{in} may be interchanged.

12. Loop test enable
TTL input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous.
When pin 12 = '1' O_1 is connected internally to A_{in} and O_2 to B_{in}. Clock becomes the OR function of O_1 O_2. **N.B.** a decode clock has to be supplied. The delay from NRZ in to NRZ out is 7½ clock periods in loop back.

14, 15, O_1, O_2
Outputs representing the ternary encoded PCM AMI/HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length.

16. $+V_{CC}$
Positive 5V ±5% supply.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = 0°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}		-0.3		0.8	volts	
Low level input current	I_{IL}	1,2,3,5,6 10,11,12,13			50	µA	$V_{IL} = 0V$
High level input voltage	V_{IH}		2.5		V_{cc}	V	
High level input current	I_{IH}				50	µA	$V_{IH} = 5V$
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 800µA
		4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	40	mA	All inputs to 0v All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0			MHz	Figs.9, 14
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2			MHz	Figs.10, 14
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.8, 9, 14. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.9, 14
tpd1A-tpd1B				20	ns	Figs.9, 14
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = 1, Figs.9, 14
Setup time of NRZ data in to Clock (Encoder)	ts3	30			ns	Figs.7, 9, 14
Hold time of NRZ data in	th3	55			ns	Figs.7, 9, 14
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.12, 14
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.11, 14
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.13, 14
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.7, 10, 14. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.7, 10, 14
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.7, 10, 14
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	100			ns	Figs.7, 13, 14
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	200			ns	Figs.7, 13, 14
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2'	0			ns	Figs.13, 14

NOTES
1. The Encoded ternary outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4).

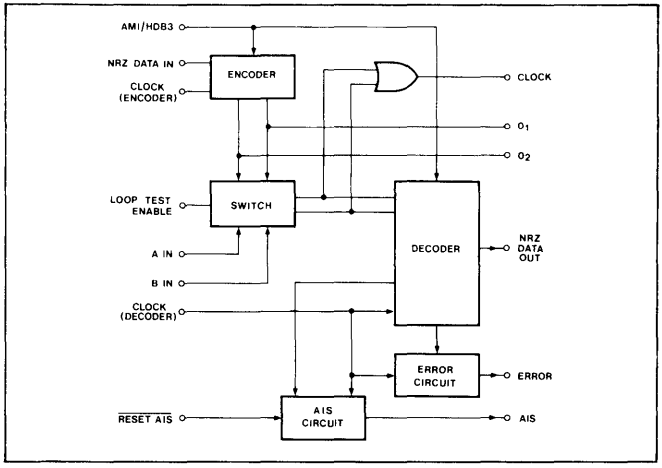

Fig. 2 MJ1471 Block diagram

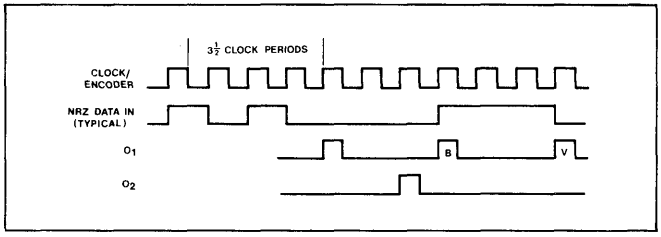

Fig. 3 Encode waveforms

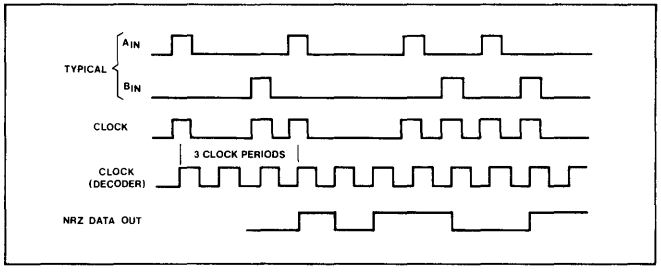

Fig. 4 Decode waveforms

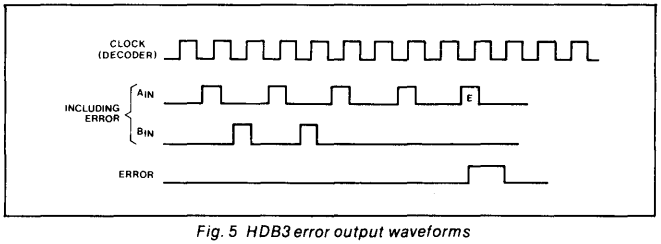

Fig. 5 HDB3 error output waveforms

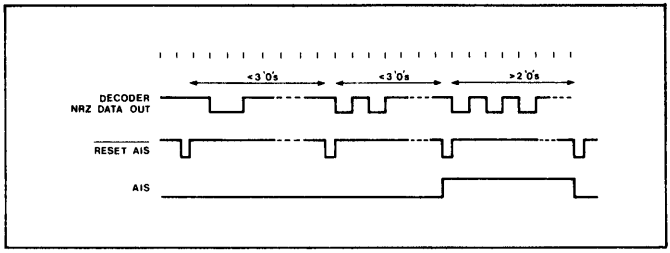

Fig.6 A/S error and reset waveforms

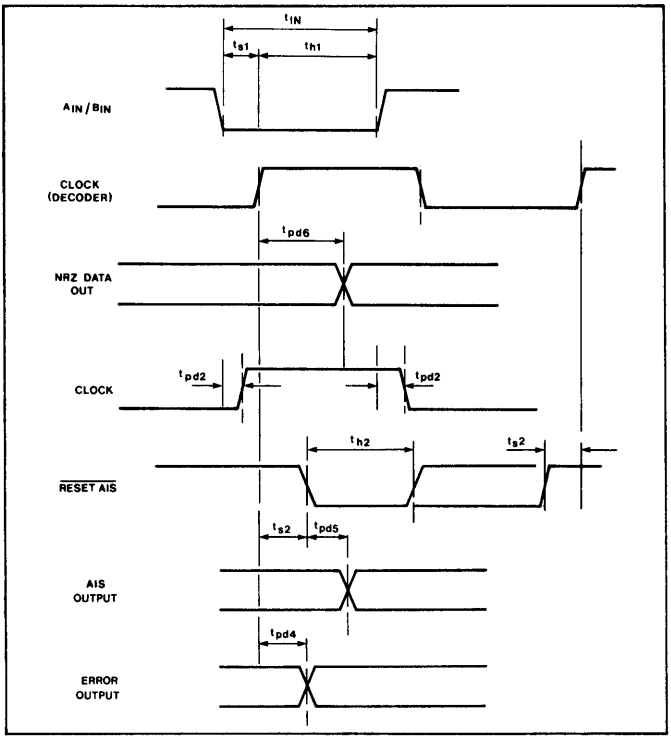

Fig. 7 Decoder timing relationship

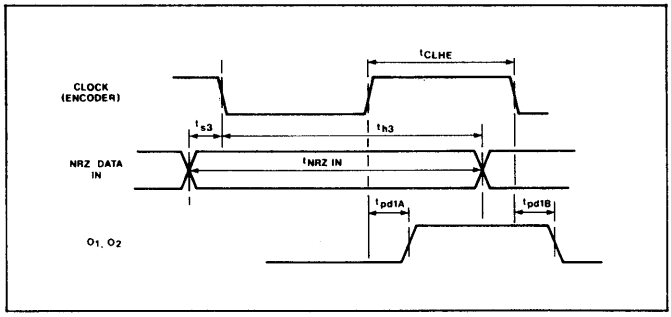

Fig. 8 Encoder timing relationship

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.

2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).

3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).

4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance:	Chip to Case	Chip to Amb.
	40°C/Watt	120°C/Watt

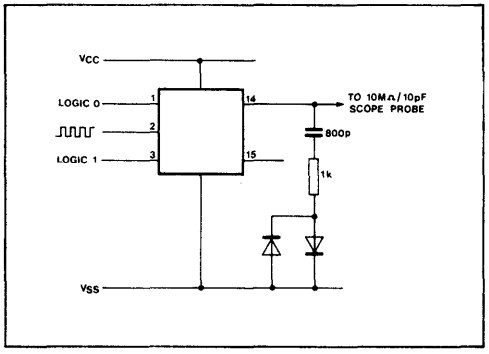

Fig. 9

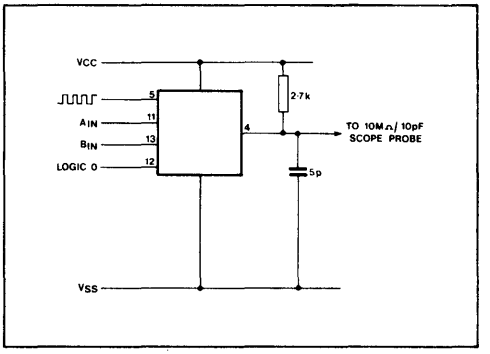

Fig. 10

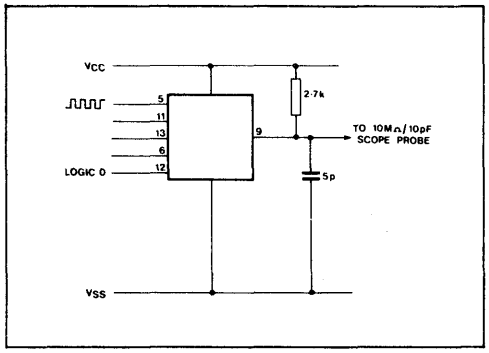

Fig. 11

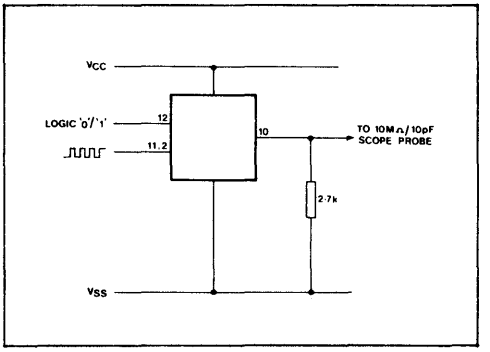

Fig. 12

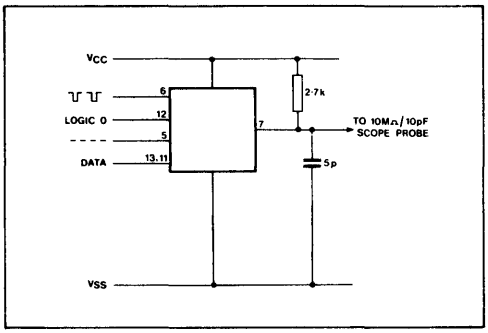

Fig. 13

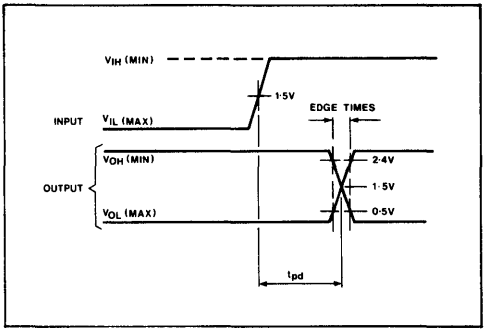

Fig. 14 Test timing definitions

PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MJ1472

PCM RECEIVING CIRCUIT

The MJ1471/1742/1473 circuits have been designed specifically for use in 30 channel PCM systems. All circuits conform to the appropriate CCITT recommendations. The range of circuits is realised in N-channel MOS technology. They all operate from a single 5V supply and all inputs and outputs are TTL compatible. Operating speed of 2.048MHz is guaranteed over 0°C to 70°C temperature range.

The MJ1472 block diagram is shown in Figure 2.

FEATURES

- Line Time Generation (From 9 Stage Clock Driven Counter)
- Line Timing, Frame Alignment
- Alarm Signals FAT + MIR, ATL, AW, EPAT
- Test Points TP1, TP2, TP3, MR
- Inputs and Outputs LSTTL Compatible

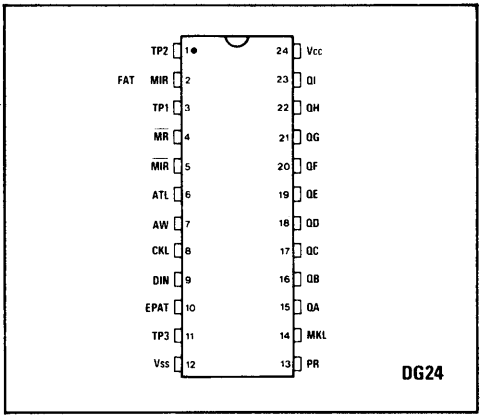

Fig.1 Pin connections (top view)

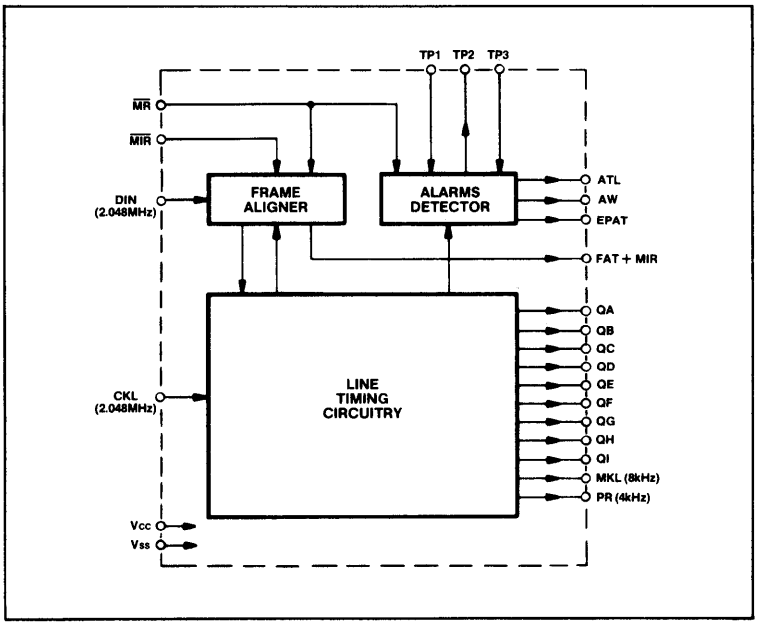

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0°C to +70°C
Package thermal resistance 60°C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	All inputs	2.7			V	I_{OH} -60μA
Low-level output voltage	V_{OL}	All inputs			0.5	V	I_{OL} = 0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25°C
High-level output current	I_{OH}	All outputs	-60			μA	V_{OH} = 2.7V
Low-level output current	I_{OL}	All outputs	0.8			mA	V_{OL} = 0.5V
Input capacitance	C_{IN}	All inputs			10	pF	1MHz 100mV
Supply current	I_{CC}			40	60	mA	V_{CC} = 5.25V

AC CHARACTERISTICS

Propagation delays	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Q_A to Q_I	t_{pd1}			50	ns	Fig 5 for loading Measure from CKL LE
MKL & PR	t_{pd2}			100	ns	As above
ATL & FAT + MIR	t_{pd3}			100	ns	As above
AW	t_{pd4}			300	ns	As above
EPAT	t_{pd5}			100	ns	Fig 5 for loading Measure from TP3 LE
TP2	t_{pd6}			150	ns	Fig 5 for loading Measure from TP1 TE
TP2	t_{pd7}			250	ns	Fig 5 for loading Measure from CKL LE
Required delay from DIN transition to CKE TE	t_1	50		430	ns	

FRAME ALIGNMENT

Frame alignment is described by the flow chart of Figure 3 where the A and B words are defined.

Position	1	2	3	4	5	6	7	8
Word A	X	0	0	1	1	0	1	1
Word B	X	1	X	X	X	X	X	X

Table 1

A(TA) represents the presence of word A in TSO of frame TA. B(TB) likewise represents the presence of word B in TSO of frame TB. $\overline{A}$(TA) and $\overline{B}$(TB) represent the absence of the words in TSO of the respective frame.

Frame alignment is assumed lost when 3 consecutive words A(TA) or B(TB) have been received with error. Frame alignment is recovered when the following sequence is detected in successive frames. Word A⟶ word B (TB) and finally A(TA). To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of an imitative frame alignment signal, the following procedure is followed. Should A(TA) be followed by absence of word B(TB) a new search for A is started a frame later.

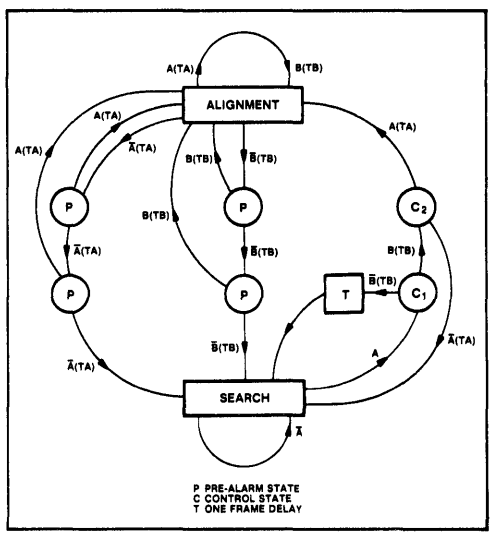

Fig.3 Frame alignment procedure

LINE TIMING

Nine stage clock (CKL) driven counter. All outputs (QA to QI) available externally.

MKL One bit positive pulse corresponding to 8th bit of TS15.

PR One bit positive pulse corresponding to position 8 of TS30 of frame A.

TRANSMISSION ALARM DETECTION

As already outlined in Fig.3. Three consecutive words A(TA) or B(TB) set an R-S flip-flop. This condition can also be forced by the external signal MIR.

MIR Input to R-S flip-flop.

FAT + MIR Output indication of state of R-S flip-flop.

ATL Output high when logic '1' is detected in position 3 of TS0, TB for two consecutive TB frames. Output low when logic '0' is detected in position 3 of TS0, TB. ATL output inhibited by the presence of output FAT + MIR.

AW Output high whenever $\overline{A}$(TA) is detected. Output is removed only when word $\overline{A}$(TA) is detected.

EPAT The output is high when for eight consecutive times at least 15 words A(TA) are detected in 512ms. EPAT alarm is removed (EPAT = 0) when less than 15 $\overline{A}$(TA) words are detected in (512 x 8)ms. The 512ms timer interval is obtained by an 11 bit binary counter clocked every double frame.

TEST POINTS

TP1, TP2, TP3 and Master Reset MR are test points.

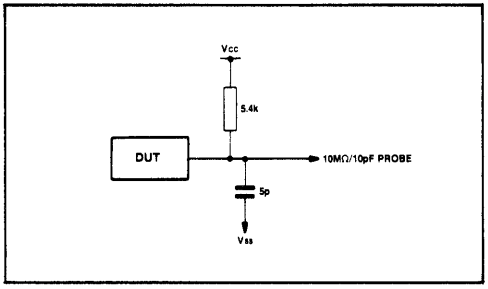

Fig.4 Propagation delay test circuit

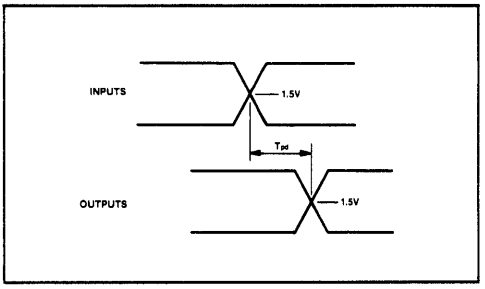

Fig.5 Waveforms for tpd

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MJ1473

PCM TRANSMITTER CIRCUIT

The MJ1400 Series of circuits have been specifically designed for use in 30 channel PCM systems.

The MJ1473 is designed to simplify the transmit section of a 30 channel, 2 MBit PCM link by converting NRZ PCM data to either AMI or HDB3 format after inserting a synchronising word in channel 0 (conforming to CCITT recommendations G.703 and G.732).

The data is output in pseudo-ternary form to facilitate driving the line interface via a transformer and AMI or HDB3 code may be remotely selected using bits 2 and 3 in channel 0 of the incoming data stream.

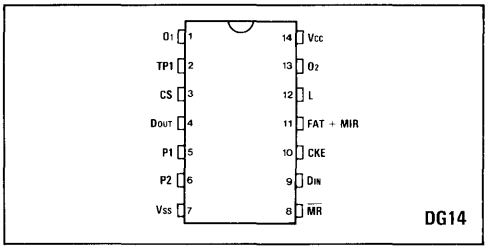

Fig.1 Pin connections - top view

FEATURES

- 5V - 30mA Power Requirements
- 0-70°C Operation
- Complies with Relevant CCITT Recommendations
- Control Signals Compatible with MJ1472,4
- NRZ, AMI or HDB3 Transmission Format
- Transmission Format Controlled Locally or Remotely Via TSO Data
- Fabricated in NMOS Technology
- Inputs and Outputs TTL Compatible

Bit	1	2	3	4	5	6	7	8
Channel 0 TS0.TA	X	0	0	1	1	0	1	1
Channel 0 TS0.TB	X	1	ATL	X	X	X	X	X

Table 1

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to Vss : 7V
Storage temperature : -55° C to +155° C

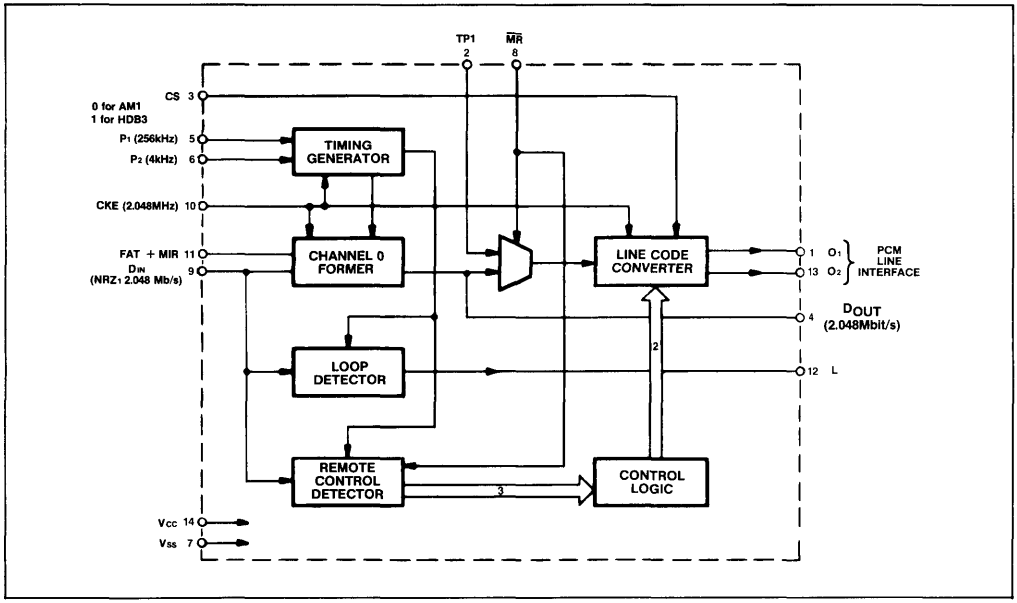

Fig.2 Block diagram of MJ1474

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0°C to +70°C
Package thermal resistance 95°C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	Outputs L & D_{OUT}	2.7			V	-60μA
Low-level output voltage	V_{OL}	Outputs L & D_{OUT}			0.5	V	0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25°C
High-level output current	I_{OH1}	Outputs L & D_{OUT}	60			μA	V_{OH} = 2.7V
High-level output current	I_{OH2}	Outputs O_1 & O_2	2			mA	V_{OH} = 2.8V
Low-level output current	I_{OL}	Outputs L & D_{OUT}	0.8			mA	V_{OH} = 0.5V
Input capacitance	C_{IN1}	All inputs except CKE			10	pF	1MHz 100mV
	C_{IN2}	Input CKE			20	pF	
Supply current	I_{CC}			30	45	mA	V_{CC} = 5.25V

AC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
O_1 & O_2	t_{pd1}			100	ns	Fig. 4 for loading; measure from CKE leading edge. See Fig. 5 for definition: total delay in t_{pd1} + 4 CKE periods.
L (Propagation delays)	t_{pd2}			200	ns	Fig. 3 for loading; measure from CKE trailing edge. See Fig. 5 for definition.
D_{OUT}	t_{pd3}			180	ns	Fig. 3 for loading; measure from CKE leading edge. See Fig. 5 for definition: total delay is t_{pd3} + 8 CKE periods.
Rise and fall times of O_1 & O_2	t_r/t_f			20	ns	Fig. 4 for loading. Measured between 0.5V and 2.4V points.
Required delay from D_{IN} P1.P2 transition to CKE TE	t_1	50		430	ns	
Required delay from FAT + MIR transition to CKE LE	t_2	50		430	ns	
Required delay from CS transition to CKE TE	t_3	50		430	ns	

CIRCUIT DESCRIPTION

The MJ1473 generates exchange timing by a synchronous 9-bit counter driven by exchange clock CKE and preset by P1,P2. The exchange clock also clocks data, D_{IN},through the channel 0 former and to D_{OUT} via an eight bit shift register. In the channel 0 former, data bits of channel 0 are modified as shown in Table 1.

An X in Table 1 indicates transparency through the circuit, bits 2 and 3 of the shift register are concerned with the loop command circuitry. When '01' is detected an internal latch is set and the loop condition on output L is registered.

D_{OUT} may also be routed through the HDB3/AMI Encoder. The CS control is logic '0' for AMI and logic '1' for HDB3. Encoded data is then output to O_1 and O_2 in a form suitable for driving the PCM interface.

The line code converter can also be controlled by the remote control commands present on bits 2 and 3 of the shift register. These commands are as follows:

1. The presence of '00' in the first frame yields AMI transmission except channel 0 and 1, which are transmitted in a code determined by CS.
   The presence of '00' in each consecutive frame yields unipolar transmission except in channel 0 and 1 as above. The polarity of unipolar transmission is constant for any number of consecutive '00' frames but will alternate with respect to the previous unipolar transmission provided there has been an intermediate frame where '00' was not detected.
2. The presence of '11' in any frame yields AMI transmission except for channel 0 and 1 which are transmitted in a code determined by CS.

ATL is forced to a '1' by the presence of the external signal FAT + MIR, or by the presence of one of the two remote control commands or by the loop comand.

An 'all ones' condition on the encoded data outputs (O_1 O_2) is forced in the presence of a '1' in position 4 of channel 0, when the loop condition is met.

For normal operation $\overline{MR}$ = TP1 = 1. The test point TP1 is provided as an input independent of the line code converter. In order to enable this input when $\overline{MR}$ = 0.

All inputs and outputs are compatible with LSTTL.

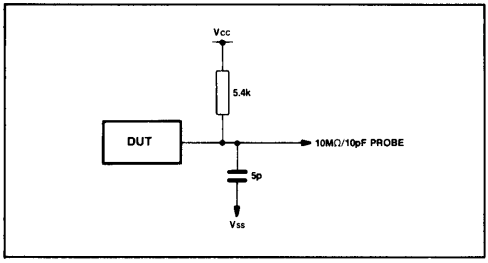

Fig.3 Propagation delay test circuits

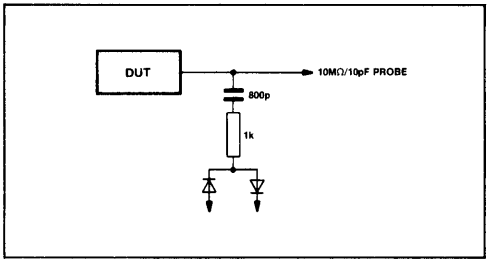

Fig.4

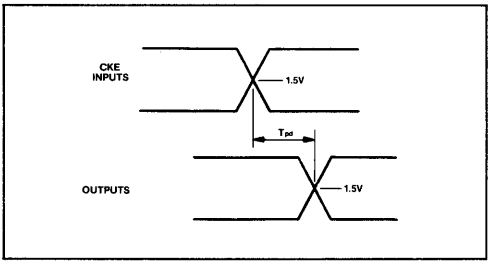

Fig.5 Waveforms for t_{pd}

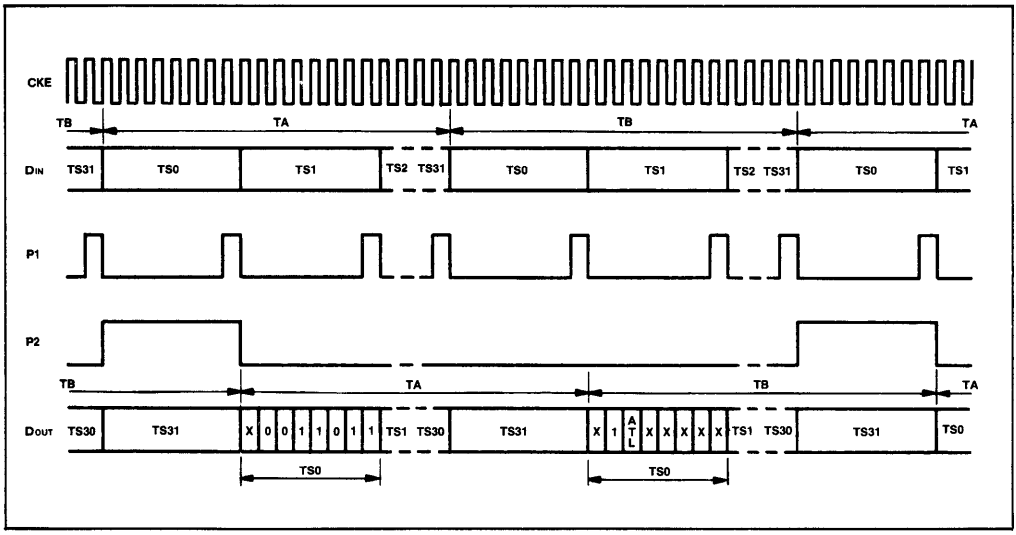

Fig.6 Timing diagram

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ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MJ1474

PCM ELASTIC STORE

The MJ1400 Series of circuits have been specifically designed for use in 30 channel PCM systems.

The MJ1474 retimes the received 30 (+2) channel PCM data stream to the exchange clock and also produces a 5-bit output which identifies the individual channels within the retimed data stream.

Slip is handled by control logic which causes a repetition (or jump) of channel 0 for two consecutive frames whenever the Store capacity is about to be exceeded.

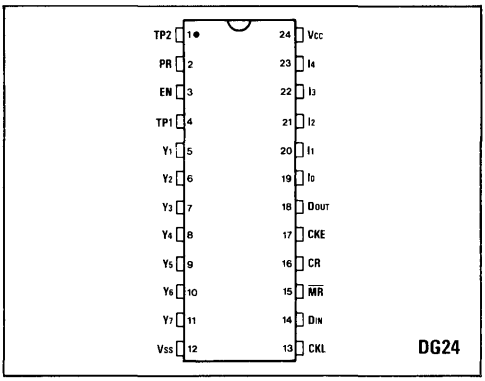

Fig.1 Pin connections - top view

FEATURES

- 5V - 50mA Power Requirements
- Performance Guaranteed Over 0-70°C Temperature Range
- Performs Slip/Alignment Function in 2.048 MBit PCM Systems
- Conforms to Relevant CCITT Recommendations
- Compatible with MJ1472, 3 Control Formats
- Fabricated in NMOS Technology
- Inputs and Outputs TTL Compatible

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to Vss : 7V

Storage temperature : -55° C to +155° C

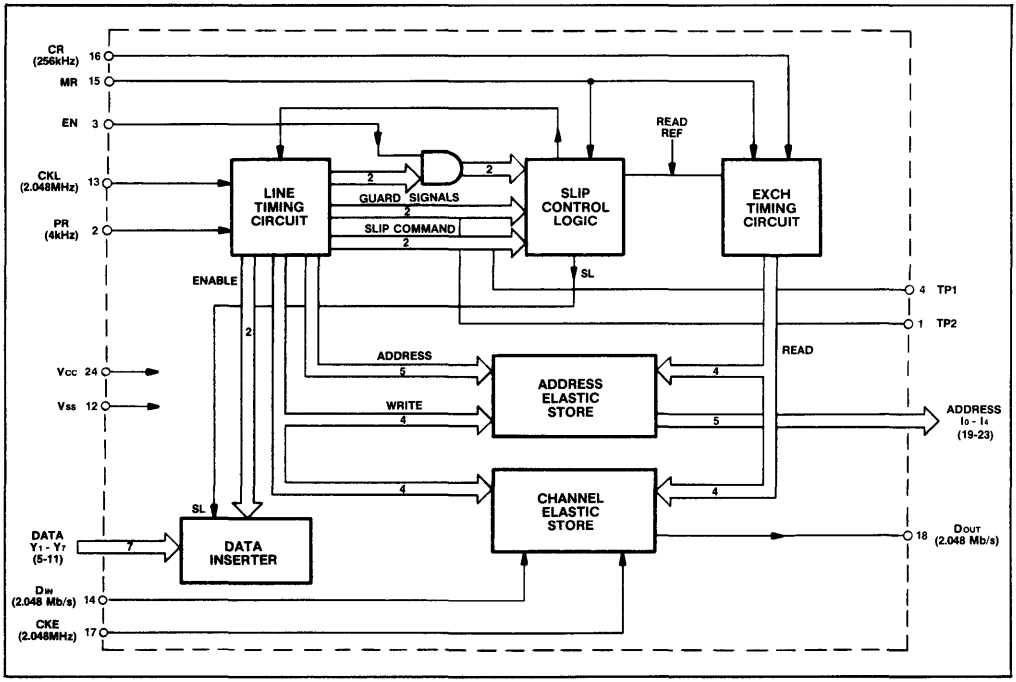

Fig. 2 Block diagram of MJ1473

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0° C to +70° C
Package thermal resistance 60° C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	All outputs	2.7			V	-60μA
Low-level output voltage	V_{OL}	All outputs except I_0 - I_4			0.5	V	0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25° C
Low-level output voltage	V_{OL1}	Outputs I_0 - I_4			0.4	V	3mA
High-level output current	I_{OH}	All outputs	60			μA	V_{OH} = 2.7V
Low-level output current	I_{OL0}	All outputs except I_0 - I_4	0.8			mA	V_{OH} = 0.5V
Low-level output current	I_{OL1}	Outputs I_0 - I_4	3.0			mA	V_{OL} = 0.4V
Input capacitance	C_{IN}	All inputs			10	pF	1MHz 100mV
Supply current	I_{CC}			50	80	mA	

AC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
D_{OUT}	t_{pd1}			100	ns	Fig. 4 for loading; measure from CKE leading edge. See Fig. 5 for definition.
TP1	t_{pd2}			150	ns	Fig. 3 for loading; measure from CR and CKL. See Fig. 5 for definition.
TP2	t_{pd3}			150	ns	Fig. 3 for loading; measure from CKL trailing edge. See Fig. 5 for definition.
I_0 - I_4	t_{pd4}			200	ns	Fig. 4 for loading: measure from CR trailing edge.
Propagation delays						
Required delay from D_{IN} transition to CKL leading edge	t_1	50		430	ns	
Required delay from FAT + MIR transition to CKL leading edge	t_2	50		430	ns	
Required delay from CS transition to CKL trailing edge	t_3	50		430	ns	

CIRCUIT DIAGRAM

The line timing circuit consists of a 9-bit counter clocked by CKL and preset by PR. Counter states are decoded to form slip commands for the slip control logic and enable signals for the data inserter. The counter also controls the switching logic that delivers the write signals for the two elastic stores, i.e. channel and address, and the guard signals for the slip control circuit.

The channel elastic store has the function of retiming the 32 channels from D_{IN}, clocked by CKL, to D_{OUT} clocked by the exchange clock CKE. The address elastic store has the function of retiming the address of the 32 channels from the line clock CKL to parallel I_0 to I_4 outputs clocked by the exchange clock CKE.

The elastic stores are controlled by a slip control logic, which compares guard signals and the read reference signal. The read reference is generated together with 4 read signals from a 2-bit counter, driven by CR, in the exchange timing circuit. When the store capacity is about to be exceeded the slip control logic becomes active. The effects are a repetition (or jump) of channel zero for the two consecutive frames. Full capacity is always recovered after a normal slip. The contents of all other channels are unchanged during a slip.

A slip may also be forced in the presence of signal EN. This effect is a repetition (or jump) of channel 0 and address 0 for one frame only.

The data inserter modifies channel 0 data out according to Table 1:

Position	1	2	3	4	5	6	7	8
Frame TA	X	X	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
Frame TB	X	1	Y_7	SL	X	X	X	X

Table 1 TSO format

Where SL is generated by the slip control logic Y_1 to Y_7 are external inputs and X indicates transparency through the circuit.

The circuit also has a master reset (MR) input for initialization of slip control and exchange timing circuits. TP1 and TP2 are also available as test points.

All inputs and outputs are compatible with LSTTL. Outputs I_0 - I_4 are capable of sinking 3mA at 0.4V.

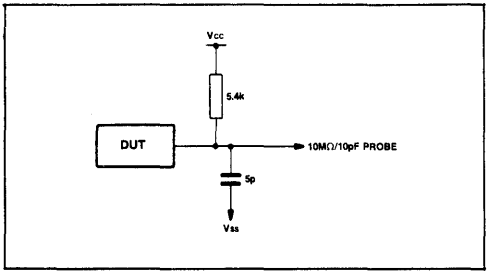

Fig.3

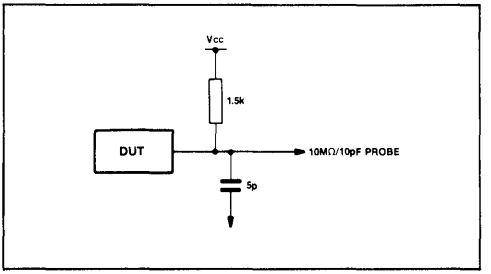

Fig.4

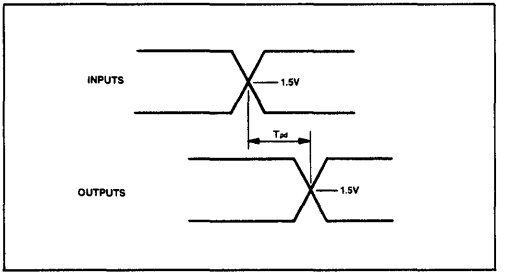

Fig.5 Waveforms for t_{pd}

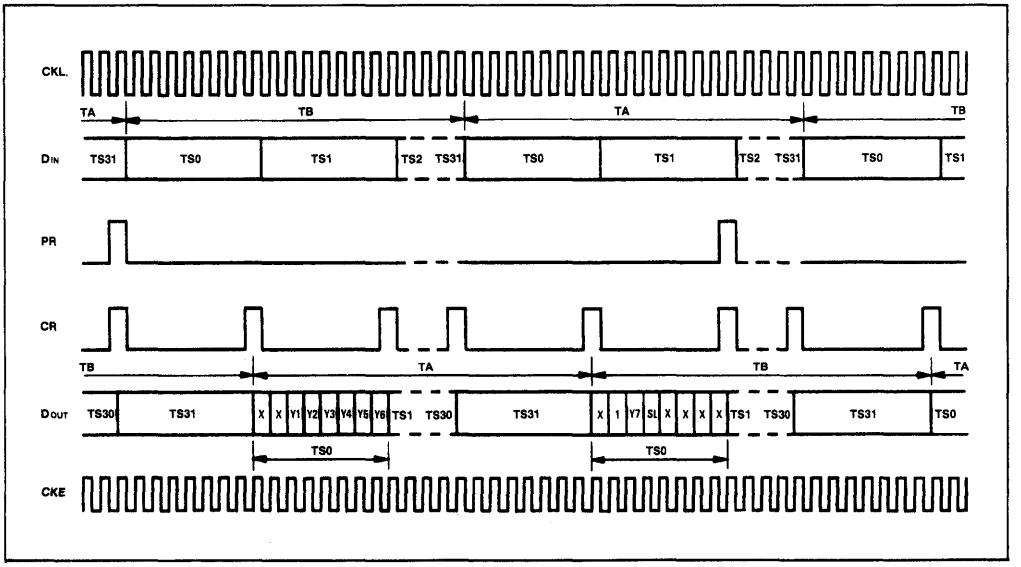

Fig.6 Timing diagram

PLESSEY
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PRELIMINARY INFORMATION

MS2002EXP

DIGITAL SWITCH MODULE (DSM)

The Plessey MS2002 is an n-channel MOS LSI integrated circuit providing digital switching for 256 channels in PCM systems. The device is unidirectional in operation and is capable of switching data from any incoming channel to any outgoing channel. Input data can be either serial or parallel. The DSM is designed to be easily expandable to provide a greater switching capacity.

FEATURES

- Single 5V Supply
- TTL Compatible
- Interfaces Directly with European Standard CCITT 32 Channel 2.048Mb/s Format
- 256 Input/256 Output Channels
- Inputs and Outputs can be either Serial or Parallel
- Open Drain Outputs Allow Easy Expansion
- Only One System Clock Required with One Frame Synchronisation Pulse

APPLICATION

- Circuit Switched PCM or Data Systems

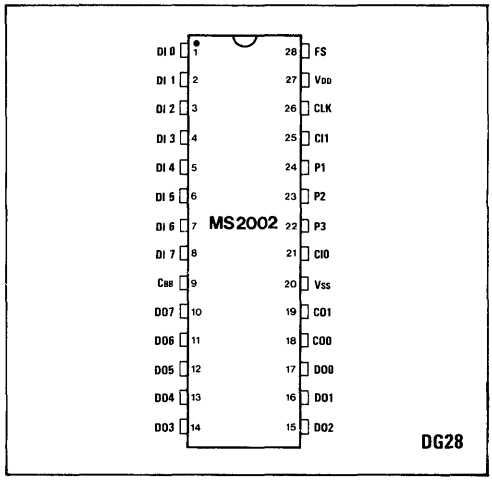


Fig.1 Pin connections - top view

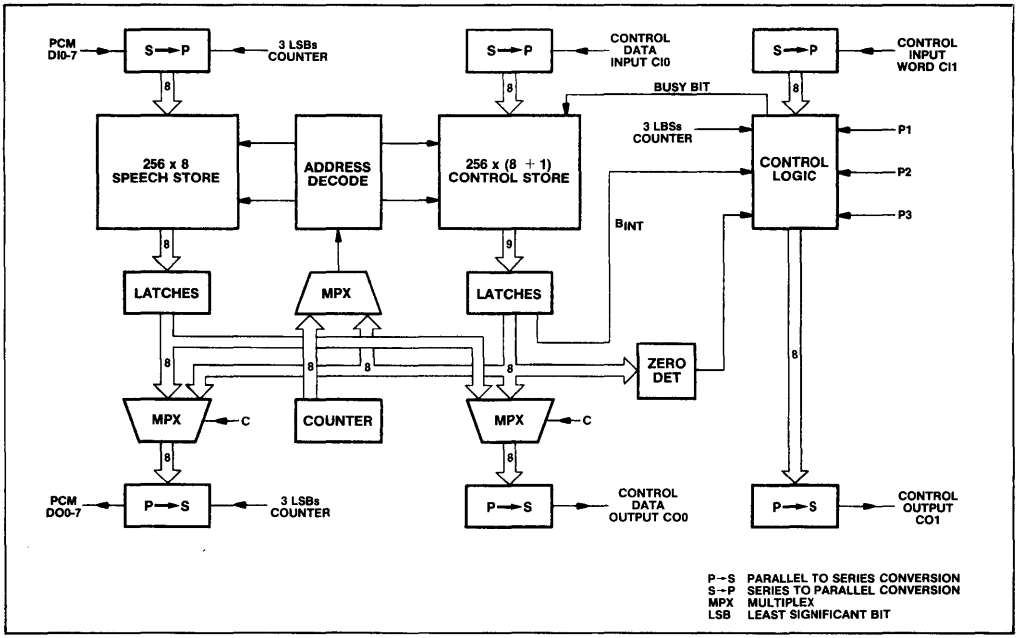


Fig.2 Block diagram of DSM

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	4.75	5	5.25	V	
High input voltage	V_{IH}	2.4		V_{DD}	V	
Low input voltage	V_{IL}	-0.5		0.8	V	
O/P pull up resistor	R_{PU}	950			Ω	+1 Schottky load
C_{BB} capacitor			1		nF	

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, T_{amb} = 25° C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		40		mA	
Input current	I_{IH}			50	μA	V_{IH} = 2.7V Logic
	I_{IL}			50	μA	V_{IL} = 0.4V inputs
Output voltage	V_{OH}	2.7			V	R_{PU} = 1kΩ Logic
	V_{OL}			0.5	V	R_{PU} = 1kΩ outputs
Input capacitance	C_i			5	pF	Logic inputs
Output capacitance	C_o			5	pF	Logic outputs

AC CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0° C to +70° C, V_{DD} = 5V ± 5%)

Characteristic	Symbol	Value		Units
		Min.	Max.	
System clock period	t_c	243	245	ns
System clock low period	t_{cl}	82		ns
System clock high period	t_{ch}	82		ns
Frame sync period	t_f	512	512	Clock periods
Frame sync set up time	t_{fss}	60		ns
Frame sync hold time	t_{fsh}	90		ns
Input data set up time	t_{ds}	60		ns
Input data hold time	t_{dh}	90		ns
Clock to output delay *	t_{cd}	5	150	ns

* Loaded with 7 similar outputs + 1 Schottky TTL input + 1kΩ pull up resistor to V_{DD} + 16pF.

PIN NAMES

DI0-7	Speech data input channels
DO0-7	Speech data output channels
CO0	Control data out
CO1	Control word out
CI0	Control data in
CI1	Control word in
P1-3	Programming pins
CLK	Clock
FS	Frame sync. pulse
V_{SS}	Negative supply (0V)
V_{DD}	Positive supply (5V)
C_{BB}	Substrate bias decoupling

ABSOLUTE MAXIMUM RATINGS

Supply voltage range (V_{DD})	-0.5V to +7V
Input voltage	-0.5V to +7V
Output voltage	-0.5V to +7V
Temperature: Storage	-65° C to +150° C
Operating	0° C to +70° C

NOTE
All voltages with respect to V_{SS}

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
DI0-DI7	1-8	**Speech Data Inputs** accept the 256 incoming speech channels at a 2.048Mb/s data rate and are latched on every alternate negative edge of the 4.096MHz system clock. The eight data bits of each channel may be arranged in serial format with each input line carrying 32 time multiplexed channels in standard CCITT PCM format. Frame and bit synchronisation is provided by the negative edge of FS as shown in Fig.4. The eight lines must be time slot synchronous with each other. Alternatively the speech data may be arranged in 8 bit parallel format, the eight input lines now operating as an eight bit wide bus carrying 256 consecutive channels. Channel 0 appears on the first negative edge of the clock after the FS negative transition as shown in Fig.4. The width of the frame sync. pulse FS is used to select the required format as shown in Table 2.
C_{BB}	9	**Substrate Bias Decoupling** for the -2.7V on-chip substrate bias generator is provided by a single capacitor between this pin and V_{SS}.
DO0-DO7	17-10	**Speech Data Outputs** carry the 256 switched outgoing speech channels at a 2.048Mb/s rate. As with the speech data inputs the data may be arranged in either serial or parallel format, the frame sync. pulse FS width designating the selected mode. The outgoing channels are delayed by 21 bit periods with respect to the incoming lines and are timed by the negative clock edges alternate to those used for input data. The timing relationships are shown in Fig.4. The speech data outputs use open drain drivers allowing wire OR-ing of up to 8 DSMs. The correspondence of the Speech and Control store data as seen at the Speech data outputs is shown in Fig.5(a).
CI0	21	**Control Data Input** allows updating of control memory contents (excluding B_{int}). Data format is 8 bit serial at a 2.048Mb/s rate. Thirty two words are received per frame, the frame sync. pulse designating the first bit (MSB) of the first word, as shown in Fig.4. Each Control Data word corresponds to a specific output channel and carries the number (in bit inverted format) of the input channel which is to be switched to that output. The format of the Control data input is shown in Fig.5(b). The numbering system for incoming channels is shown in Fig.5(a). The Control Data words are written to the appropriate locations in the control store determined by the current state of the Control Word CI1, received on pin 25, and the timeslot (0-31) in which the Control Data is received. The address construction is shown below (Outgoing Channel Address Construction). Table 1 shows those conditions under which a control store modification occurs.
CI1	25	**Control Word Input** accepts 8 bit serial data, word synchronised with the Control Data input CI0, thirty two Control Words being received per frame. Each Control Word corresponds to and controls the processing of the 8 bits of Control Data (CI0) received in the same timeslot on pin 21. The Control Word format is shown below. **CONTROL WORD FORMAT** (MSB) S3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$ W BEXT S2 S1 (LSB) (T = Φ) The outgoing speech channel address to which the present Control Data relates is determined by the combination of the present timeslot number (0-31 represented as a 5 bit number TS0-TS4) and the bits A0-A2 of the present Control Word as shown below. **OUTGOING CHANNEL ADDRESS CONSTRUCTION** (MSB) TS4 TS3 TS2 TS1 TS0 A2 A1 A0 (LSB) The remaining bits of the Control Word have the following functions: S1-S3 allows the message to be addressed to a specific DSM. These bits are compared with the status of the 3 Programming Pins P1-P3. W indicates whether the present operation is a control store write (W = 0) or a speech/control store read (W = 1) operation. B_{ext} is the external busy bit. If the operation is a control store write to this DSM then B_{ext} replaces the control store busy bit (B_{int}) for this channel, setting the channel to busy (B_{ext} = 0), or free (B_{ext} = 1) status. If the operation is a read then(B_{ext} = 1) data is to be read. The flow diagram of Fig.3 gives the precise interpretation of the control word.
CO0	18	**Control Data Output** allows interrogation of control or speech store contents. Data output is 8 bit serial with 32 words per frame. Each outgoing word corresponds to an incoming Control Data word but is delayed from it by 21 bit periods. The precise contents of each outgoing word are determined by the state of the related incoming Control Word CI1 as shown in the flow diagram of Fig.3. The Control Data Output uses an open drain driver allowing wire OR-ing of up to 8 DSMs.
CO1	19	**Control Word Out** is a reflection of the input Control Word delayed by 21 bit periods. The S1-S3 and B_{ext} bits may be modified depending on the internal state of the DSM, details are shown in Fig.3. The CO1 uses an open drain driver allowing wire OR-ing of up to 8 DSMs.

PIN DESCRIPTIONS

Symbol	Pin No.	Pin name and description
P1-P3	22-24	**Programming Pins** allow up to 8 DSMs to share a common control highway (CI0,CI1) and simplify the control structure when arrays of DSMs are used to construct larger switches. The Programming Pins should be hardwired to V_{SS} or V_{DD} to give each DSM a unique address. The state of the P1-P3 pins in combination with the S1-S3 and W bits (Control Word Format) of the control word determine how the control store is modified and also influence the contents of the outgoing CO0 and CO1 words. The complete control flow is shown in Fig.3. Table 1 summarises the effects on the control memory.
CLK	26	**Clock** input requires a 4.096MHz TTL level signal. All input signals are strobed in on alternate negative clock edges, the active edge being denoted by the position of the frame sync. signal FS, as shown in Fig.4.
FS	28	**Frame Sync.** provides a frame datum for the incoming data (both speech and control), marks the active edge of the system clock, and controls the speech input and output formats (serial or parallel) Fig.4 shows the timing relationship of the frame sync. signal to clock and data. The duration of the frame sync. low period determines the I/O format as shown in Table 2. Following a change in I/O mode the operation of the DSM is undefined for the remainder of that frame and the whole of the following frame.

W	S3 = P3	S2 = P2	S1 = P1	Action on Control Store
0	1	1	1	CI0→Control Store, BEXT→BINT
0	1	0	1	*FF→Control Store, 1→BINT
0	1	1	0	*FF→Control Store, 1→BINT
0	1	0	0	*FF→Control Store, 1→BINT
X	0	X	X	No action on Control Store
1	X	X	X	No action on Control Store

Table 1 Control Store modification

*Denotes hexadecimal notation.

Low period *	I/O format
1	SISO
2	SIPO
3	PISO
4	PIPO

Table 2 I/O format control

*Low period is shown in multiples of 4.096MHz system clock periods.

OPERATION

The DSM (block diagram is shown in Fig.2) is a 256 channel non-blocking digital switch capable of connecting all 256 incoming channels to all 256 outgoing channels in any desired order. Alternatively, selected input channels may be broadcast to any number of output channels. Each output channel may, however, receive from only one input channel at a time, i.e. conferencing facilities are not provided. Speech input to the device is via 8 lines (DI0-DI7) that can accept 8 bit data in either serial or parallel format at a 2.048Mb/s rate. Speech output is via a further 8 lines which may be set independently of the input lines to give out serial or parallel format data.

Call routings are held in an on-chip control memory in the form of a nine bit word for each outgoing speech channel, bit nine (B_{int}) indicating the busy status of the channel (0 = busy). In the case of a busy outgoing channel the remaining eight bits denote the number of the input channel to be connected to that outgoing channel. The numbering system for incoming channels is shown in Fig.5(a). If B_{int} indicates the channel is free then the remaining eight bits of the control word are used as the contents of the outgoing channel, hence allowing free choice of idle code. The contents of the control store can be modified, and speech or control store interrogated, via control messages received over the control interface CI0, CI1. Data generated by interrogation of either the control or speech memories appears on the two control output lines CO0, CO1.

SPEECH PATH DELAY CHARACTERISTICS

The switching function of the DSM is achieved by storing the incoming speech channels sequentially in the 256 x 8 speech memory (after conversion to parallel format) and then sending them to the output channels in the order specified by the control memory. The delay encountered by each channel consists of a fixed delay, determined by the format conversion circuitry and the memory read/write cycle time, and a variable delay determined by the time spent in memory waiting for the relevant outgoing timeslot. The delay is given by the relations:

$$\left.\begin{array}{l} D = 21 + (N - M) \text{ for } N \geqslant M \\ D = 277 + (N - M) \text{ for } N < M \end{array}\right\} \text{PIPO format}$$

$$\left.\begin{array}{l} D = 21 + (\text{INT}\frac{N}{8} - \text{INT}\ ) \times 8\ N \geqslant M) \\ D = 277 + (\text{INT}\frac{N}{8} - \text{INT}\ ) \times 8\ N < M \end{array}\right\} \text{SISO format}$$

where D = delay in bit periods (488ns)
M = incoming channel No. (as shown in Fig.5)
N = outgoing channel No.

CONSTRUCTION OF 512 CHANNEL SWITCH

Fig.6 demonstrates the use of the address facilities of the DSM control structure to build larger switches (512 channels in this case). The four devices share common control and speech highways, each device being assigned a unique address designated by the programming pins P1-P3. It should be noted that devices sharing a common output highway have been allocated a common value for P3. This allocation of addresses reduces the number of control messages required to set up or clear down calls as inspection of table 1 reveals; a message sent to one DSM setting or clearing a channel will automatically clear the same channel on any DSM which outputs to the same highway (has the same P3 value).

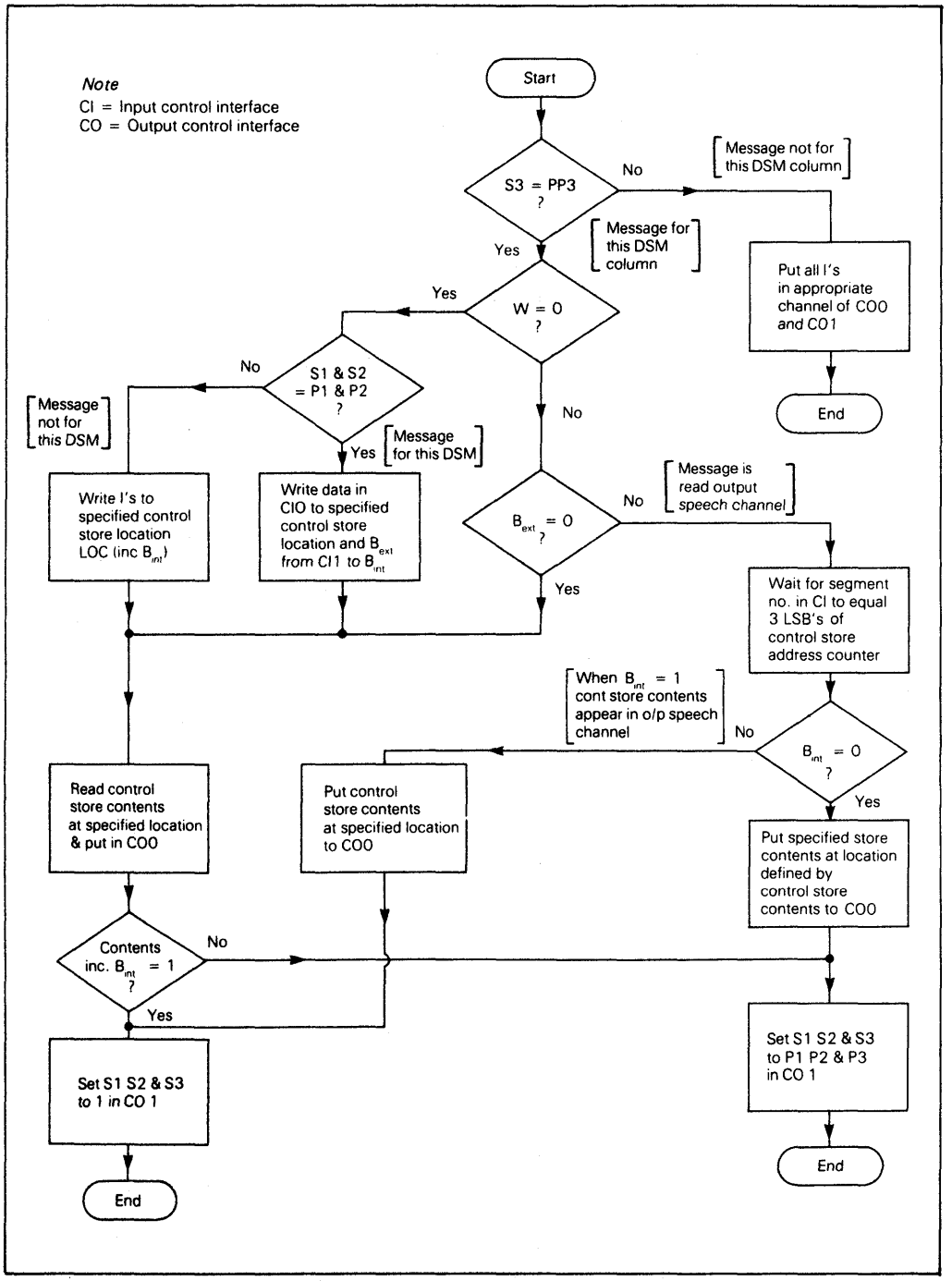
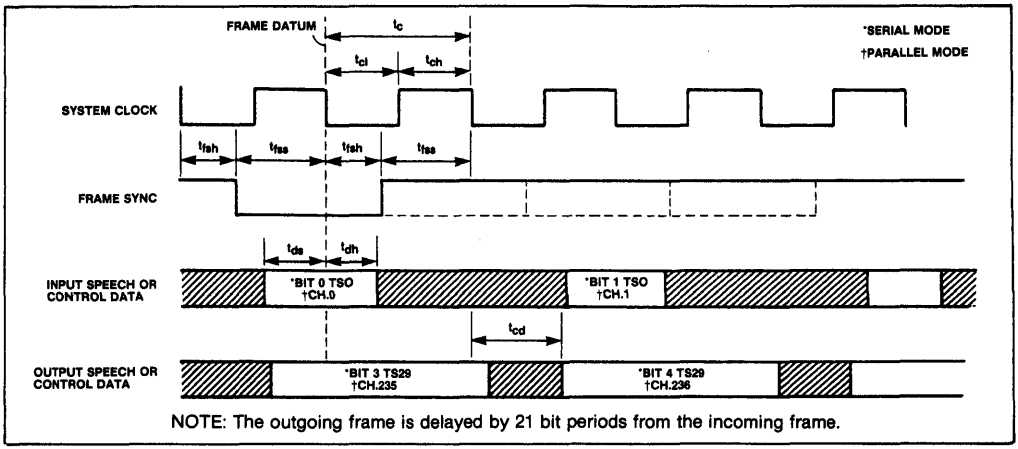


Fig.3 DSM control logic flowchart



NOTE: The outgoing frame is delayed by 21 bit periods from the incoming frame.

Fig.4 Clock, data, and frame sync timing relationships

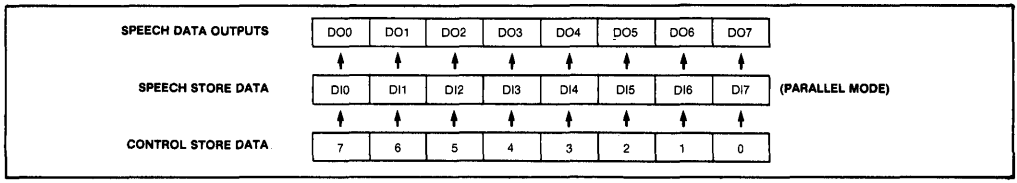


Fig.5(a) Correspondence of Speech and Control data

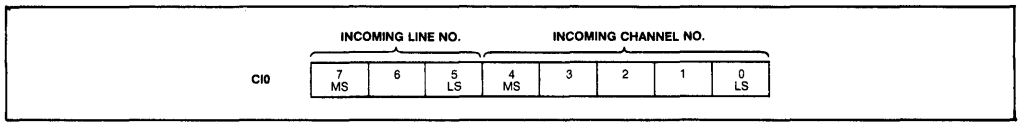


Fig.5(b) Format of Control data input

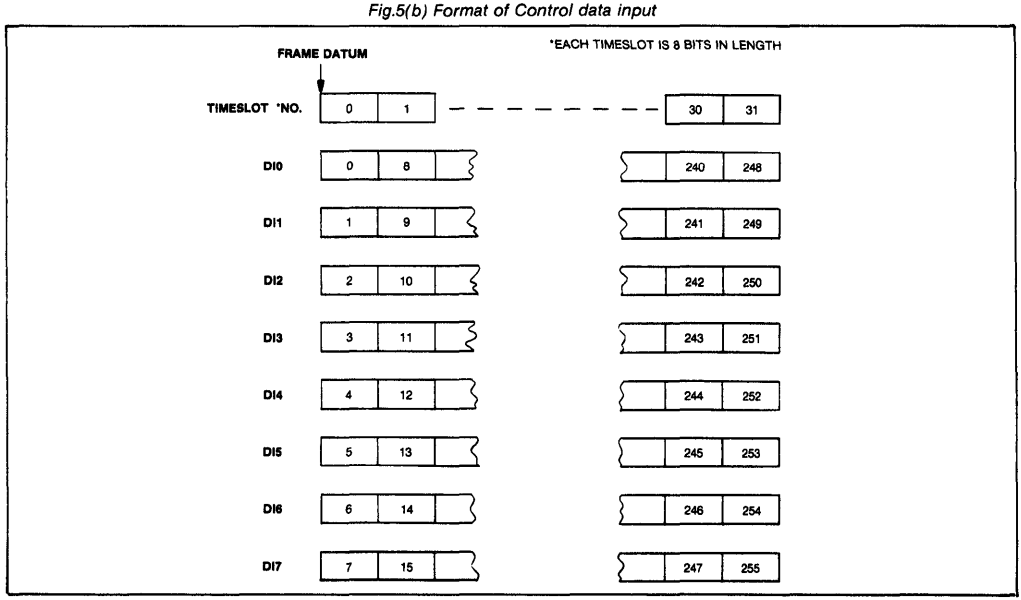


Fig.5(c) Channel numbering for incoming speech data (serial mode)

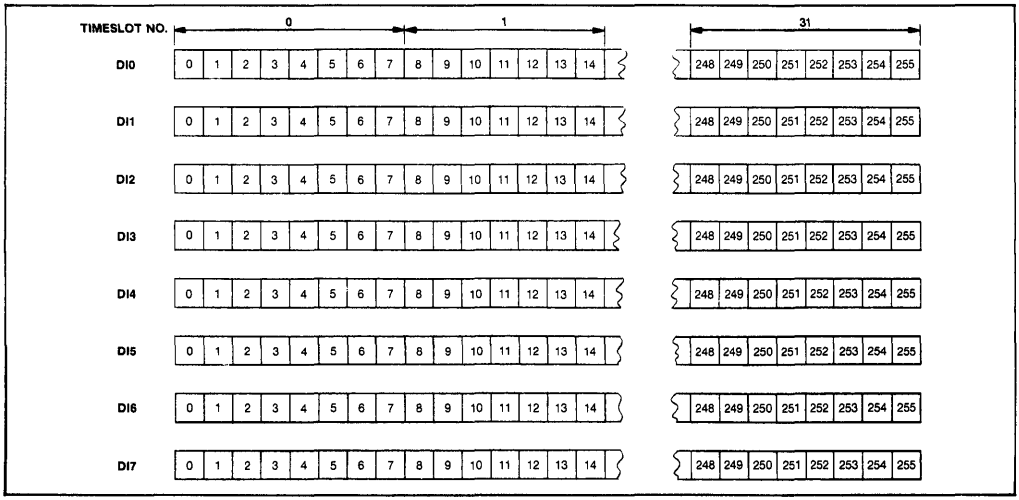


Fig.5(d) Channel numbering for incoming speech data (parallel mode).

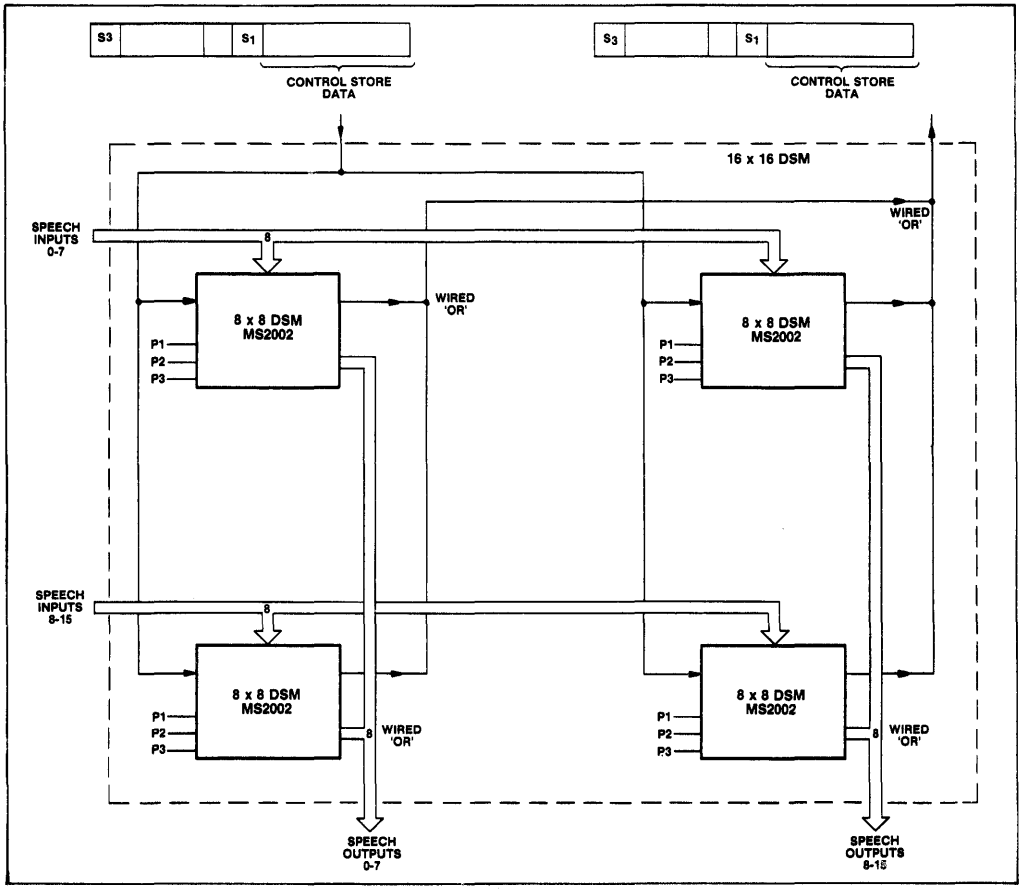


Fig.6 512 channel DSM made from four 8 x 8 DSMs

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MS2014

DIGITAL FILTER AND DETECTOR (FAD)

The MS2014 is a real time general purpose digital signal processor (DSP) which is easily programmed to perform digital filtering and level detection. The architecture of the FAD comprises a cascadable second order recursive filter and level detector using dedicated multipliers, adders and delay elements.

The data controlling the response of the MS2014 is stored in an external PROM or RAM and consists of a list of filter coefficients and comparison levels. This simple data format means that the user does not need an expensive development system at the design stage (in contrast to other DSP devices, which use microprocessor-based structures and require considerable software development effort to realise their function). The off-chip data memory allows for easy adaptive control, even when complicated algorithms are to be implemented.

The filter and detector have been designed to give maximum flexibility in use and can easily generate most of the functions required in tone detector, spectral analysis, adaptive filter and speech synthesis systems.

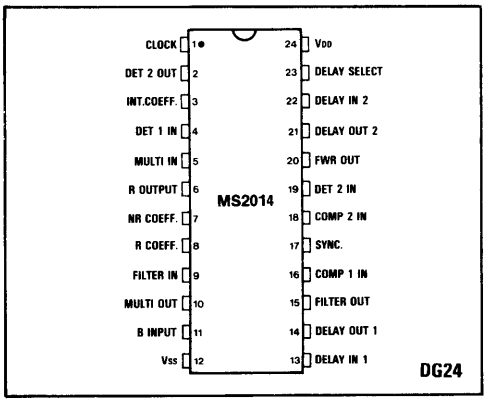

Fig.1 Pin connections - top view

FEATURES

- Linear 16-Bit Data
- 13-Bit Coefficient
- 2MHz Operating Clock Frequency
- Serial Operation
- 448 Bits of On-Chip Shift Register Data Storage for 8th Order Multiplex
- Nth Order Multiplexing (N≤8)
- TTL Compatible
- Single +5V Supply

APPLICATIONS

- Low Cost Digital Filtering
- Level Detection
- Spectral Analysis
- Tone Detectors (Multi-Frequency Receivers)
- Speech Synthesis and Analysis
- Data Modems
- Group Delay Equalisers (All-Pass Networks)

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD})	-0.5V to +7V
Input voltage	-0.5V to +7V
Maximum output voltage	+7V
Temperature: Storage	-65°C to 125°C
Operating	0°C to 70°C

NOTE
All voltages with respect to V_{SS}.

PIN NAMES

	Name	Function	I/O
1	Clock	Single phase clock input	I
2	Detect 2 Out	Output from detector 2	O
3	Int.Coeff	Integrator coefficients	I
4	DET 1 In	Detector 1 input	I
5	Mult In	Input to NR B multiplier	I
6	R Output	Output of recursive section	O
7	NR Coeff	Non-recursive (NR) coefficient input	I
8	R Coeff	Recursive coefficient input	I
9	Filter In	Data input to filter section	I
10	Mult Out	Output from B multiplier	O
11	B Input	Input from B multiplier	I
12	Vss	0V	
13	Delay In 1	Input from filter external delay	I
14	Delay Out 1	Output to filter external delay	O
15	Filter Out	Data output from filter section	O
16	Comp 1 In	Comparison level 1 input	I
17	Sync	Synchronisation pulse input	I
18	Comp 2 In	Comparison level 2 input	I
19	DET 2 In	Input for detector 2 via FWR	I
20	FWR Out	FWR output from Det 2 In data	O
21	Delay Out 2	Output from detectors 1 and 2, and connection to detector external delay	O
22	Delay In 2	Input from detector external delay	I
23	Delay Select	Internal/External delay selector	I
24	VDD	+5V supply	

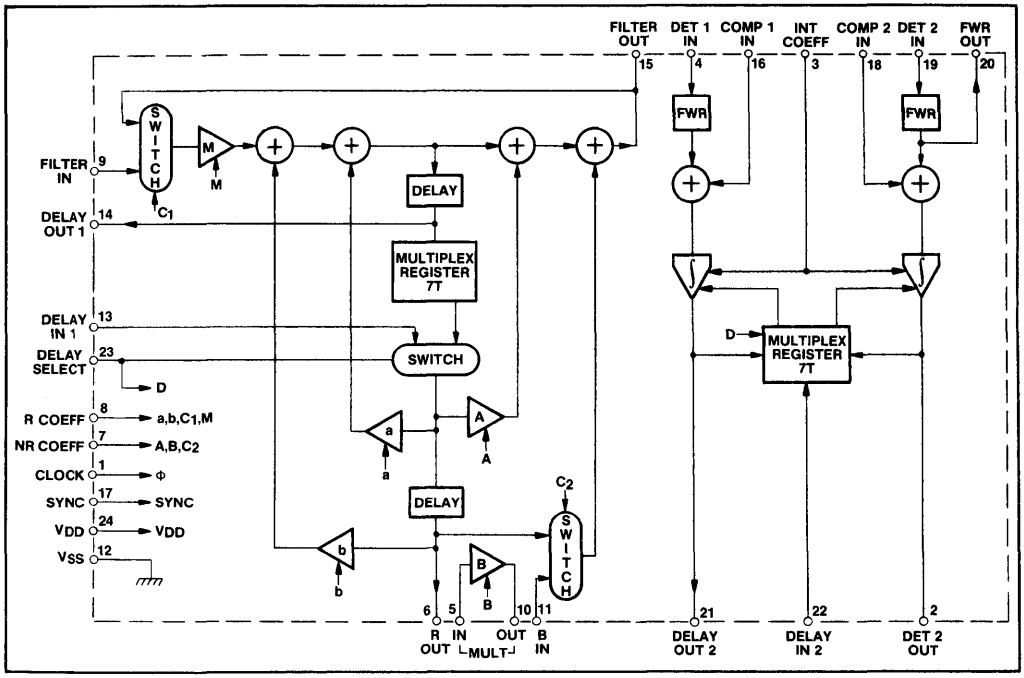

Fig.2 Block diagram

PERFORMANCE

A sample throughput of 64000 samples/s is guaranteed. Thus using a sampling period of 125μs (8000 samples/s) the following may be realised:

8 bi-quadratic 2nd-order recursive filter sections;
plus 16 full-wave rectification operations;
plus 16 1st-order leaky integrations;
plus 16 level comparisons.

Filters of more than 16th order are possible but will require a lower sampling rate or more than one MS2014.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Supply voltage	V_{DD}	4.75	5.25	V	
Input voltage (high state) except clock	V_{IH}	2.2	-	V	
Input voltage (low state) except clock	V_{IL}	-	0.7	V	
Input voltage (high state) clock	V_{IHC}	4.5	-	V	
Input voltage (low state) clock	V_{ILC}	-	0.5	V	
Clock rise and fall time	t_{cl}		30	ns	10% - 90% (Note 1)
Clock frequency	f_{cl}	0.5	2.048	MHz	
Operating temperature	T_{amb}	0	70	°C	

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V T_{amb} = 25° C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	I_{DD}		90	120	mA	
Output voltage, low	V_{OL}	-	-	0.5	V	I_{OL} = 0.4mA (Note 2)
Output voltage, high	V_{OH}	2.7	3.4	-	V	I_{OH} = -40μA (Note 2)
Input capacitance (except clock)	C_{in}		5	7	pF	
Input capacitance (clock)	C_{inc}		25		pF	
Input data set up time	t_{is}	50	-	-	ns	Fig.7
Input data hold time	t_{ih}	150	-	-	ns	Fig.7
Output data delay time	t_{os}	-	-	200	ns	Fig.7

NOTES
1. An operating clock frequency of 2.048MHz is guaranteed over the supply voltage range and the full operating temperature range.
2. The output stage is designed to drive a standard TTL LS gate (74LS series).

FUNCTIONAL DESCRIPTION

The Filter Section

The filter section provided in the MS2014 is a second order recursive type (see Fig.3). This structure was chosen because of its good coefficient sensitivity and predictable round-off, limit-cycle and overflow properties. Higher order filters are easily produced by cascading sections in a similar manner to analogue active filter design.

The transfer function of the section is given by:

$$H(z) = M \frac{[1 + Az^{-1} + Bz^{-2}]}{[1 - az^{-1} - bz^{-2}]} \quad \ldots (1)$$

The coefficients a and b define a pair of complex poles, whilst A and B define a pair of complex zeros. The Scaling Factor M is necessary because many filters have greater than unity gain, hence there is a danger of numeric overflow in the filter arithmetic. In the MS2014 this scaler multiplies by a factor of

$$M = (\tfrac{1}{2})^n \text{ where } 0 \leqslant n \leqslant 13$$

The multipliers in the MS2014 are serial/parallel types which require the coefficient data as a static parallel word. To minimise the number of pins on the device, this data is loaded serially and stored in a SIPO shift register. Each multiplier requires the coefficient data to be in 2s complement form with 12 bits for the fractional part of the number.

The range for the coefficients are:

$$\begin{aligned} 2 &> A \geqslant -2 \\ 2 &> a \geqslant -2 \\ 1 &\geqslant B \geqslant -1 \\ 1 &> b \geqslant -1 \end{aligned}$$

For the A,a coefficients there is an added bit ($a_S A_S$) to give the extra ± 1 range, which gives a total of 14 bits for the A,a coefficients and 13 bits for B,b.

The second-order filter is very easily multiplexed by increasing the delay function in steps of T (where T is the computation period*) and time-sharing the arithmetic elements. The limit on this process is the maximum clock rate of the MS2014. With a 32 bit computation cycle the clock rate f_{cl} is given by:

$$f_{cl} = 32 \times f_s \times Y$$

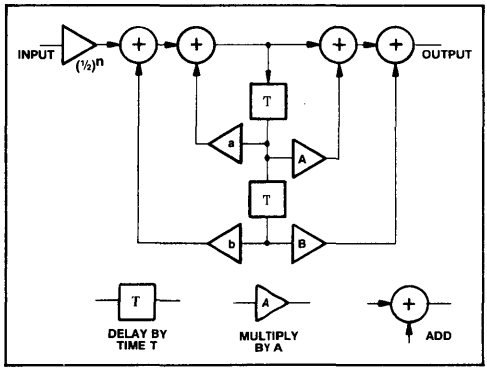

Fig.3 Basic 2nd order filter section

where Y is the number of times the filter is multiplexed and f_s is the sampling rate (the reciprocal of the sampling period T_s **). In telephony applications it is usual for f_s to be 8000 samples/s; hence at the maximum guaranteed clock rate of 2048kHz, Y must be less than or equal to 8.

By presenting an input sample during every 32-bit computation cycle, 8 separate second-order filters can be implemented. As the inputs can be independent of each other the filter is then said to be 'channel multiplexed'.

Filters of higher order can be built by feeding the output data emerging from one second-order section back to the input via an on-chip data selector, which is enabled by the control bit C_1; since the delay between the input and output of the filter section is 32 clock periods, the data arrives at the beginning of the next computation cycle. Thus by controlling the data selector two or more second-order filter sections can be cascaded. This arrangement allows any combination of filter and channel multiplexing to be achieved.

Higher orders of channel or filter multiplex require the connection of additional delay. For 8th-order multiplex, a delay of $7T$ (224 bits) is provided on chip; together with the inherent delay T (32 bits) of the computation cycle, this

*T = computation period = 32 x (1/2048k)s = 15.63µs i.e. 32 bits at 2048 kbit/s clock rate.

**T_S = sampling period = (1/8000)s = 125µs at a sampling rate of 8kHz i.e. 256 bits at 2048 kbit/s clock rate.

makes up the necessary $8T$ delay. Other orders of multiplex require the external connection of $(Y - 1) \times 32$ bits of delay.

The detector function is carried out by 'full wave rectifiers' followed by comparators and leaky integrators. By interconnecting these in different ways various absolute and relative level decisions can be made.

The 'Full Wave Rectifiers'

Data entering the 'full wave rectifiers' is inverted if the sign bit of the word is a '1' (i.e. negative). The 1LSB error generated by this is insignificant and does not materially affect operation of the detector.

The Integrators

The integrators in the MS2014 are unity gain variable-leak-factor types. Fig.4 shows the internal arrangement. The leak factor

$$1\text{-}2^{-(K + 1)}$$

controls the rise time of the integrator, the relationship is given in Table 1.

Level Detection

Both relative and absolute level detectors can be implemented in the MS2014. Fig.5 shows the arrangement for an absolute level detector. The sign bit of the data word emerging from the integrator is '1' if the mean level of the filter output is greater than the comparator input level.

Relative level detection can be achieved by using the arrangement of Fig.6. In most applications where relative level sensing is required, the filtering can be arranged such that $B = 1$ (i.e. the complex zeros are located on the unit circle in the z plane), this allows the B multiplier to be used for scaling the relative levels. In this application the B coefficient must be negative.

Leak factor	Rise time (0 to 90%)
1/2	3 Ts + T
3/4	8 Ts + T
7/8	17 Ts + T
15/16	35 Ts + T
31/32	72 Ts + T
63/64	146 Ts + T
127/128	293 Ts + T
255/256	588 Ts + T

Table 1 Integrator rise times

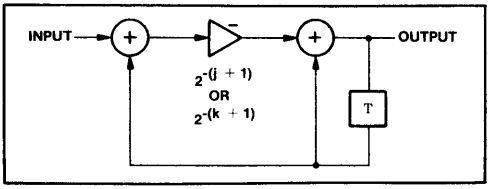

Fig.4 Leaky integrator

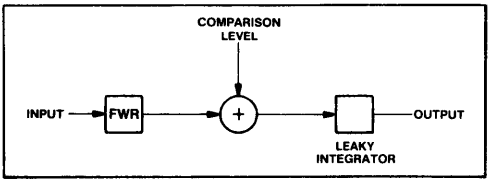

Fig.5 Simple level detector

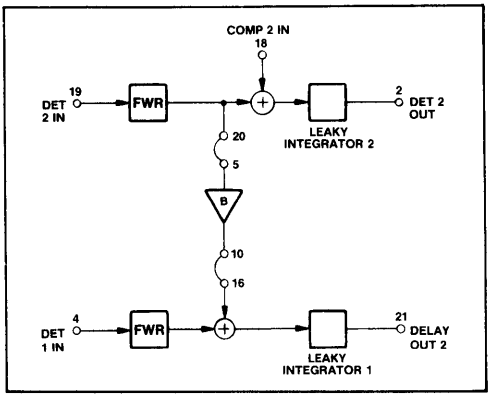

Fig.6 Relative level detection

FILTER DESIGN WITH THE MS2014

One of the commonest techniques for designing analogue filters is to factor the transfer function into blocks which can be realised by second order filter sections. Most designs of this type are done using tables which give coefficients for equations of the form:

$$H(s) = \frac{Cs^2 + Ds + K}{Es^2 + Fs + 1} \quad \ldots (2)$$

Since the MS2014 filter section is a general second-order structure, the same design technique can be employed. By using the Bilinear Transform:

$$s = \frac{2}{T}\frac{(1 - z^{-1})}{(1 + z^{-1})} \quad \ldots (3)$$

it is possible to design digital filters from analogue prototypes. By substituting equation (3) into (2) and re-arranging the result into the form of equation (1) the following relationships are derived:

$$A = \frac{2KT^2 - 8C}{4C + 2DT + T^2}$$

$$a = \frac{8E - 2T^2}{4E + 2FT + T^2}$$

$$M = \frac{4C + 2DT + KT^2}{4E + 2FT + T^2} \quad \ldots (4)$$

$$B = \frac{4C - 2DT + KT^2}{4C + 2DT + KT^2}$$

$$b = \frac{2FT - 4E - T^2}{4E + 2FT + T^2}$$

These five equations allow an analogue filter design to be transformed into digital form.

In addition to the four coefficients required by the filter section the data streams fed to the NR and R coefficient inputs include the four bits setting the Scaling Factor M (M_1 to M_4) and two selector control bits C_1 and C_2.

When $C_1 = 1$, data applied to FILTER IN (pin 9) goes to the filter section, when $C_1 = 0$ data emerging on FILTER OUT (pin 15) is fed back to the filter at the start of the next computation cycle.

When $C_2 = 0$ the B multiplier is by-passed by a direct connection, setting $B = 1$.

Table 2 shows the format of the serial data words for the NR and R coefficient inputs. The timing diagram (Fig.7) shows where this fits into the computation cycle. The synchronising pulse (SYNC) is coincident with the first clock pulse of the cycle and must be low before the rising edge of

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Clock Pulse Number
C_1	M_1	M_2	M_3	M_4	b Coeff. msb												lsb	a_S	a Coeff. (Recursive) msb													lsb	
X	X	X	X	C_2	B Coeff. msb												lsb	A_S	A Coeff. (Non-Recursive) msb													lsb	
0.125					0													0.73217773437														
1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	1	1	0	1	1	1	R
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NR

Table 2 Filter data format

the clock. The SYNC pulse is applied every *Y* clock pulses, where *Y* = CLOCK RATE/SAMPLING RATE.

Coefficient Conversion

After the coefficients have been obtained (from the Bilinear Transform or FAD Development Program) they must be assembled in the format given in Table 2. The FAD Development Program gives the multiplier coefficients in a ready-to-use binary string format, other techniques will give numerical values for the coefficients which must be converted into binary strings.

Coefficient Conversion Algorithm for '*A*'

The algorithm for converting *A* or *a* to binary is as follows:

Obtain $A = \frac{|A|}{2} \cdot 8191$

Convert *A* into a binary number (13 bits)

If *A* is positive INVERT THE MSB AND APPEND '0' AS NEW MSB.

If *A* is negative INVERT ALL BITS AND APPEND '1' AS NEW MSB, then ADD '1' LSB.

Conversion of '*B*' Coefficients

Obtain $B = B.4096$

Convert *B* into a binary number (12 bits)

If *B* is negative INVERT ALL BITS, ADD '1' LSB AND APPEND '1' AS NEW MSB.

If *B* is positive APPEND '0' AS NEW MSB.

In addition to the coefficient data streams one further input must be set up. DELAY SELECT (pin 23) is the control pin used to select the internal 7*T* delay. A '1' maintained on pin 23 selects the internal delay and a '0' the external option. The *B* multiplier is independent of the rest of the circuit and may be used for any purpose, although usually it will form part of either the filter or detect functions. In each case the appropriate connections must be made externally.

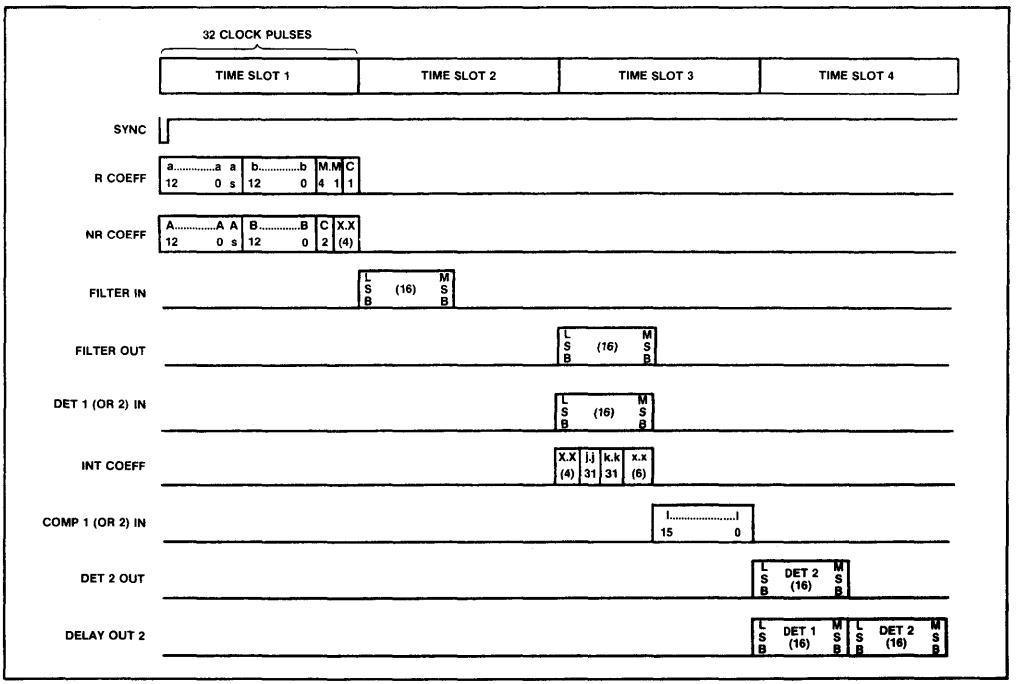

Fig.7 Timing diagram

Clock pulse number	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Integrator coefficients	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	K_1	K_2	K_3	J_1	J_2	J_3	X	X	X	X
Comparison level 1 or 2	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	P_8	P_9	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	P_{15}	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 3 Detector data format

Programming the Detector

Control data for the detect function is supplied by an external memory to the INT COEFF input (pin 3) and to the COMP 1 IN and COMP 2 IN inputs (pins 16 and 18) of the MS2014. The relative positions in time of the input sample data, detect function control data and output sample data are shown on the timing diagram (Fig.7).

Note that it is possible to economise on memory by strapping pin 3 either to pin 16 or to pin 18, since valid data for either combination of pins occurs at different times in the computation cycle. There are two integrator scaling factors in the INT COEFF data stream. The j_1, j_2, j_3 data bits determine the integrator coefficient for the data stream applied to DET 1 IN (pin 4) and the k_1, k_2, k_3 data bits for the DET 2 IN (pin 19) data stream; their definitions and clock pulse positions are given in Table 3.

In most applications, the comparison levels *l* and *m* applied to COMP 1 IN (pin 16) and COMP 2 IN (pin 18) will be negative quantities, and as they are coded in two's complement, each sign bit at clock pulse 32 will be a '1'. However,a positive quantity can be input by setting the sign bit to '0'. In this case, care must be taken to ensure that the addition of the DET data and the COMP data does not result in a number greater than unity and cause overflow, since no protection against overflow is provided in either detect function.

NOTE Round-off errors in the detector section may result in the integrator 'jamming' if the signal is below the 4 LSBs. Consequently, the available dynamic range is limited to the 12 MSBs.

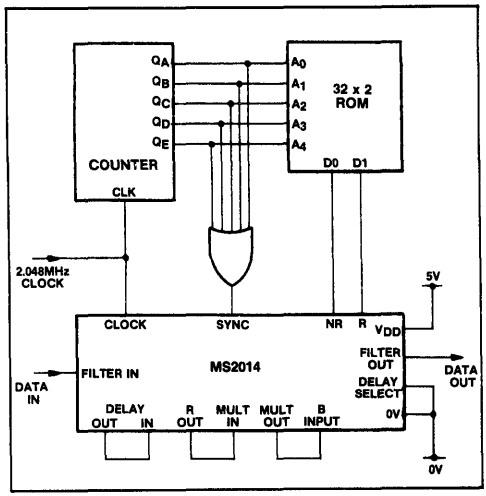

Fig.8 2nd order 32kHz bandwidth filter

TYPICAL APPLICATIONS CIRCUITS

A Second-Order High Sampling Rate Filter (Fig.8)

This is the simplest filter arrangement for the MS2014. No external delay is required so that DELAY 1 IN is connected to DELAY 1 OUT and DELAY SELECT is grounded.

A ÷32 counter generates the 5-bit wide address for the coefficient ROM. A 5-input OR gate on the address lines generates the SYNC pulse every 32 clock cycles so that at a 2.048MHz clock rate the sample rate is 64000 samples/second giving a maximum bandwidth of 32kHz.

If the desired *B* coefficient is not unity then ROUT (pin 16) must be connected to MULT IN (pin 5) and MULT OUT (pin 10) to *B* INPUT (pin 11).

A 16th Order Filter 8kHz Sample Rate Fig.9)

In this example DELAY SELECT (pin 23) is high so that the internal *7T* delay is switched in. Input data is applied during the first computation cycle (the one with the SYNC pulse in it) and coefficient data is loaded in the last computation cycle.

Channel Multiplexed Second Order Filter 8kHz Sampling

The hardware for this filter is identical to Fig.9. However, input data is provided during each computation cycle and each cycle contains a separate output. If the filter required for each channel is identical, then the coefficient memory need only be 32 x 2 bits.

Other Configurations

Sampling rates other than 64kHz and 8kHz can be achieved either by reducing the clock rate and/or by using external delays in place of the internal 0/*7T*. The use of external delay also allows different orders of multiplexing.

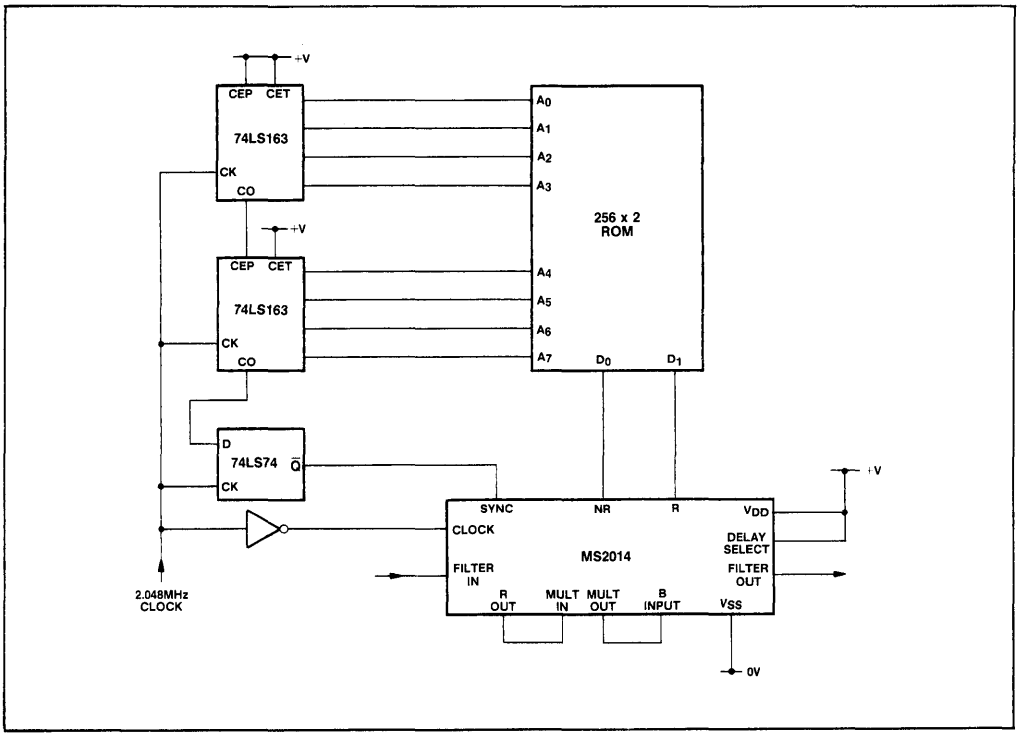

Fig.9 A 16th order 4kHz bandwidth filter

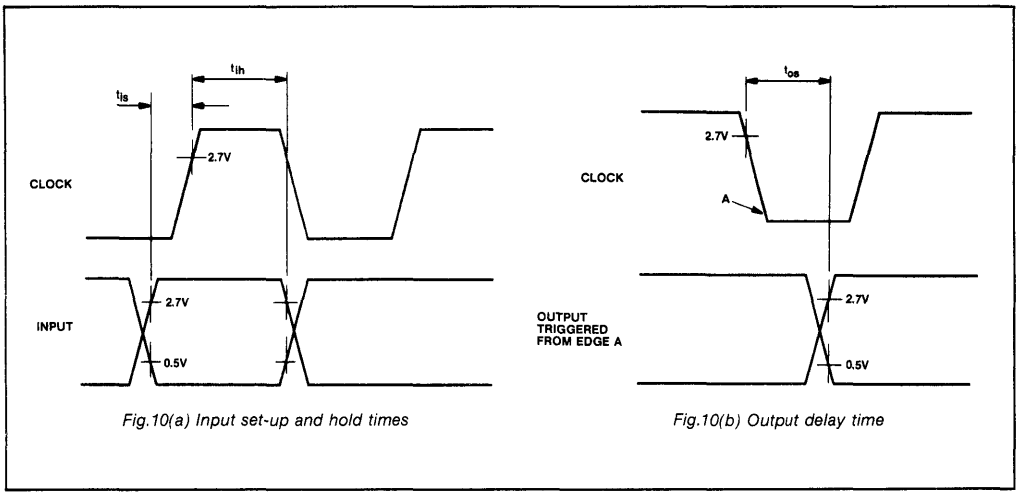

Fig.10(a) Input set-up and hold times

Fig.10(b) Output delay time

Fig.10 Input and output timing

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2MBIT PCM SIGNALLING CIRCUIT

MV1441

HDB3 ENCODER/DECODER/CLOCK REGENERATOR

The 2.048MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in CMOS and operate from a single 5 volt supply with relevant inputs and outputs TTL compatible.

The MV1441 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol.III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing. A clock recovery circuit is provided using a 16.384MHz crystal (12.352MHz for 1.544MHz operation), which may be shared between several separate devices.

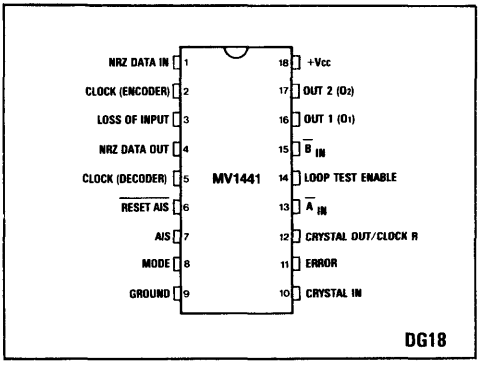

Fig.1 Pin connections - top view

FEATURES

- On-Chip Digital Clock Regenerator
- HDB3 Encoding and Decoding to CCITT rec. G703
- Asynchronous Operation
- Simultaneous Encoding and Decoding
- Clock Recovery Signal allows Off-Chip Clock Regeneration
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector)
- Decode Data in NRZ Form
- Low Power Operation
- 2.048MHz or 1.544MHz Operation

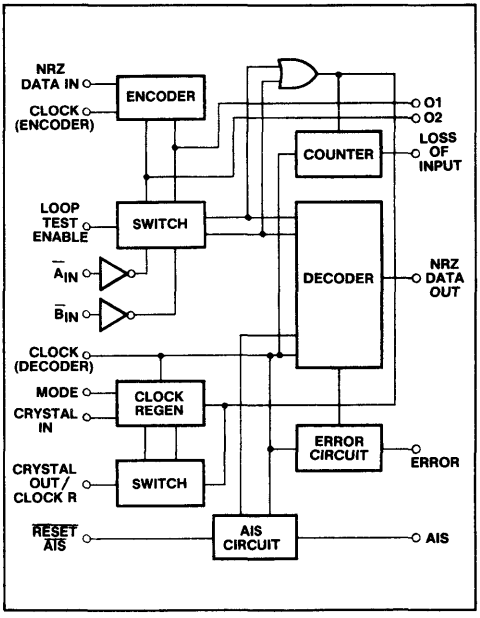

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	-0.5V to +7V
Inputs	Vcc +0.5V Gnd -0.3V
Outputs	Vcc, Gnd -0.3V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 5V ± 0.5V Ambient temperature T_{amb} = 0°C to +70°C

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	All inputs	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	V_{IL} = 0V
High level input voltage	V_{IH}		2.0		V_{CC}	V	
High level input current	I_{IH}				50	μA	V_{IH} = 5V
Low level output voltage	V_{OL}	All outputs			0.4	V	I_{sink} = 2.0mA
High level output voltage	V_{OH}		2.8			V	I_{source} = 2mA) both
			V_{CC}-0.75			V	I_{source} = 1mA) apply
Supply current	I_{CC}			2	4	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Max. Clock (Encoder) frequency	f_{maxenc}	4.0	10		MHz	Figs.10,15
Max. Clock (Decoder) frequency	f_{maxdec}	2.2	5		MHz	Figs.11,15
Propagation Delay Clock (Encoder) to O_1, O_2	$t_{pd1A/B}$			100	ns	Figs.8,10,15 See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.10,15
t_{pd1A} - t_{pd1B} difference				20	ns	Figs.10,15
Propagation Delay Clock (Encoder) to Clock Regenerate	t_{pd3}			150	ns	Loop test enable = '1', Figs.10,15
Setup time of NRZ data in to Clock (Encoder)	t_{s3}	75			ns	Figs.7,10,15
Hold time of NRZ data in	t_{h3}	55			ns	Figs.7,10,15
Propagation delay $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock Regenerate	t_{pd2}			150	ns	Loop test enable = '0' Figs.13,15
Propagation delay Clock (Decoder) to error	t_{pd4}			200	ns	Figs.12,15
Propagation delay $\overline{\text{Reset AIS}}$ falling edge to AIS output	t_{pd5}			200	ns	Loop test enable = '0', Figs.14,15
Propagation delay Clock (Decoder) to NRZ data out	t_{pd6}			150	ns	Figs.7,11,15 See Note 2
Setup time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock (Decoder)	t_{s1}	75			ns	Figs.7,11,15
Hold time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to Clock (Decoder)	t_{h1}	5			ns	Figs.7,11,15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	t_{h2}	30			ns	Figs.7,14,15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	t_{s2}	100			ns	Figs.7,14,15
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	t_{s2}	0			ns	Figs.14,15
Propagation Delay Clock (Decoder) to LIP				150	ns	

NOTES
1. The Encoded ternary outputs (O_1 , O_2) are delayed by 3.5 clock periods from NRZ Data In (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs ($\overline{A}_{IN}$, $\overline{B}_{IN}$) (Fig.4).

High Density Bipolar 3 (HDB3) is a pseudo-ternary signal in which the number of consecutive zeros that may occur is restricted to a maximum number of three. In any sequence of four consecutive binary zeros, the ultimate zero is substituted by a 'mark' (+ or -) of the same polarity as the previous mark, i.e. it violates AMI code (Alternate Mark Inversion) and is termed a 'violation'. To ensure parity between marks of opposite polarity, the first zero is substituted by an additional mark when there would otherwise be an even number of marks between 'violations'. Thus violations alternate in polarity.

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1. NRZ data in
Input data for encoding into ternary form. The data is clocked by the negative-going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. LIP
Loss of input circuit detects eleven consecutive zeros at the decoder input and then gives an output high. Any logic '1' at the input ($\overline{A}_{IN}$ or $\overline{B}_{IN}$ = '0') resets this count.

4. NRZ data out
Decoded binary data from pseudo-ternary inputs $\overline{A}_{IN}$, $\overline{B}_{IN}$

5. Clock (Decoder)
Clock for decoding data on $\overline{A}_{IN}$ and $\overline{B}_{IN}$, or O_1 and O_2 in loop test mode.

6,7. $\overline{\text{Reset AIS}}$, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS output to '0' provided 3 or more zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period, or sets AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period to indicate loss of time slot Zero. Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Mode
Mode at logic '1' selects internal crystal controlled clock regeneration and Mode at logic '0' selects external clock regeneration using, for example, a tuned circuit.

9. Ground
Zero volts.

10. Crystal In
Input to amplifier forming crystal oscillator when crystal is connected between pins 10 and 12. This pin may also be used as a 16.384MHz clock input if one oscillator is to be shared over several HDB3 encoders/decoders.

11. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been detected i.e. 3 '1's of the same polarity.

12. Clock R/Crystal Out
If pin 8 is at '0' pin 12 is Clock Regenerate, giving OR function of $\overline{A}_{IN}$, $\overline{B}_{IN}$ for clock regeneration when pin 14 = '0', OR function of O_1, O_2 when pin 14 = '1'. If pin 8 is at '1' then pin 12 becomes Crystal Out and forms oscillator with pin 10.

13,15. $\overline{A}_{IN}$, $\overline{B}_{IN}$
Inputs representing the received ternary PCM signal. $\overline{A}_{IN}$ = '0' represents a positive going '1', $\overline{B}_{IN}$ = '0' represents a negative going '1'. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ are sampled by the positive going edge of the clock decoder. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ may be interchanged.

14. Loop test enable
TTL input to select normal or loop back operation. Pin 14 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 14 = '1' O_1, is connected internally to A_{IN} and O_2 to B_{IN}. Clock R becomes the OR function of O_1, O_2. N.B. A decode clock has to be supplied, or regenerated. The delay from NRZ in (pin 1) to NRZ out (pin 4) is about 7½ clock periods in loop back.

16,17. O_1, O_2
Outputs representing the ternary encoded PCM HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length. Use suitable line drivers from these two outputs such that O_1 gives positive going pulse and O_2 gives negative going pulse.

18. $+V_{CC}$
Positive 5V ± 10% supply.

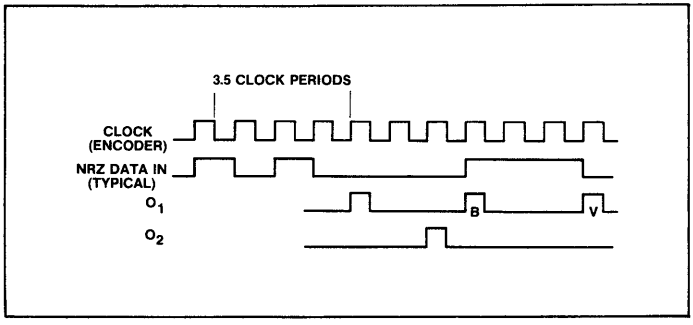

Fig.3 Encode waveforms

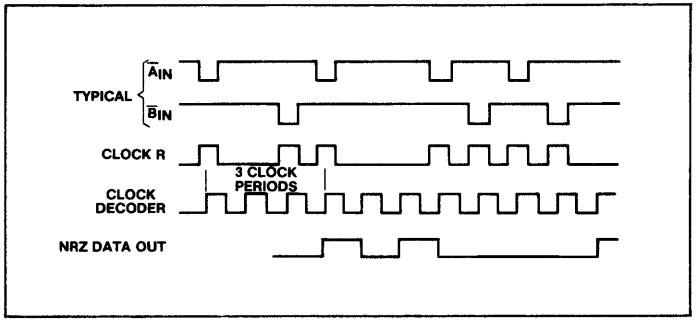

Fig.4 Decode waveforms

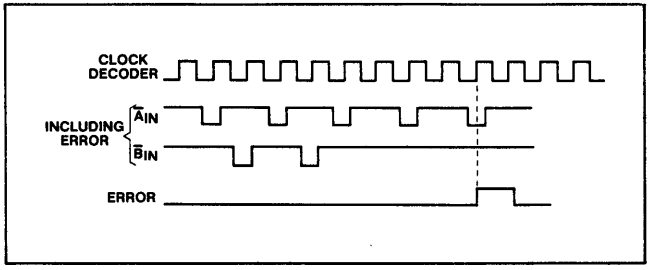

Fig.5 HDB3 error output waveforms

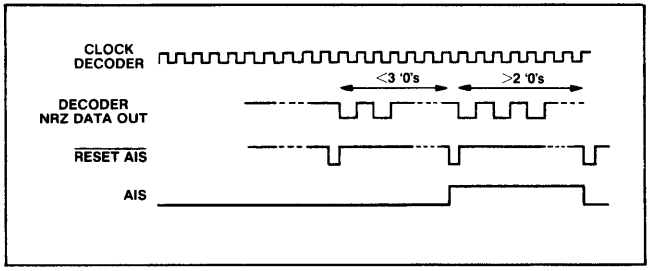

Fig.6 AIS error and Reset waveforms

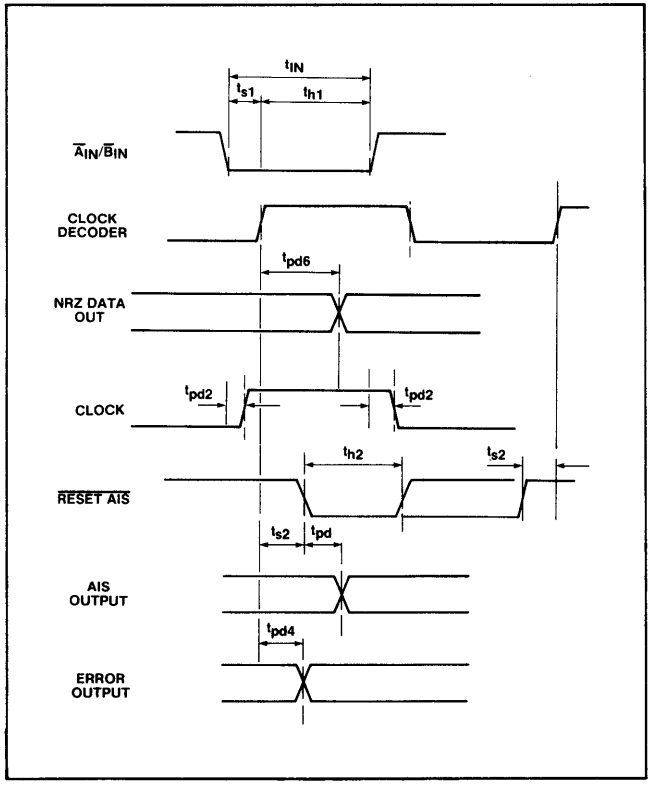

Fig.7 Decoder timing relationship

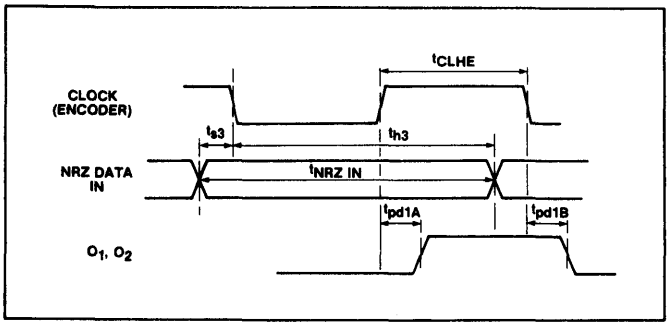

Fig.8 Encoder timing relationship

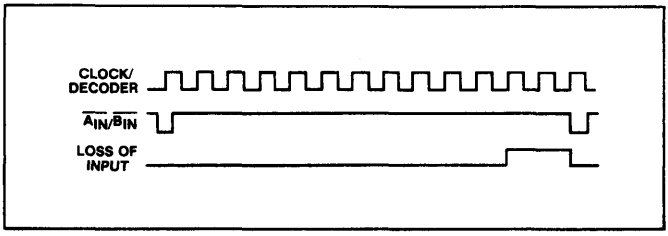

Fig.9 Loss of input waveforms

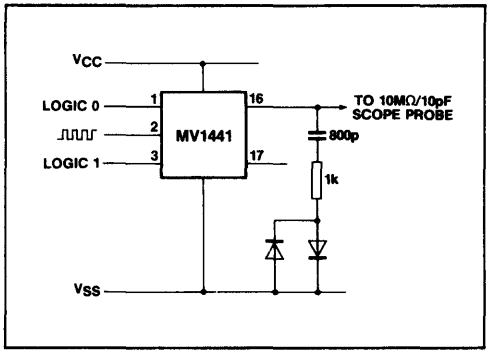

Fig.10

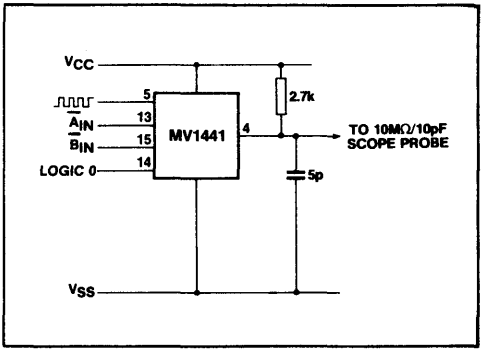

Fig.11

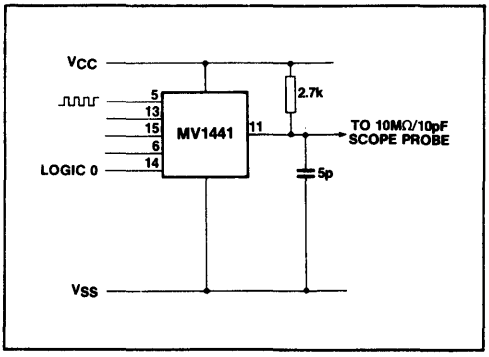

Fig.12

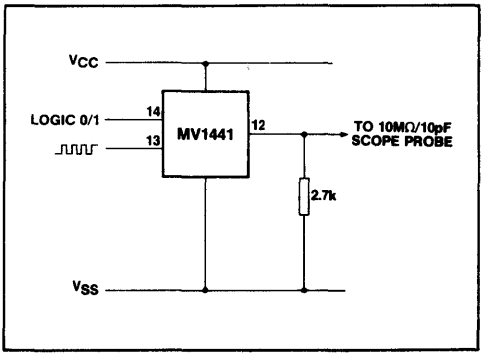

Fig.13

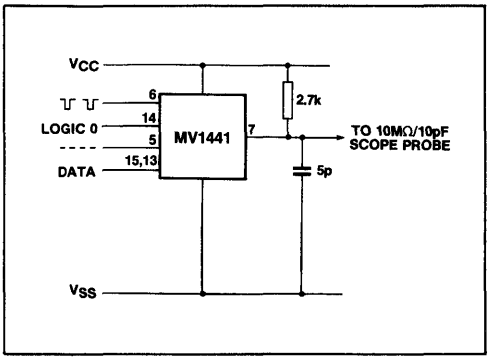

Fig.14

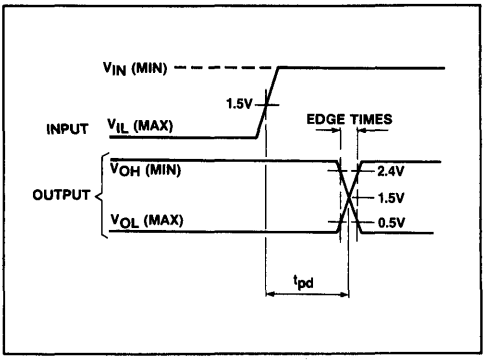

Fig.15 Test timing definitions

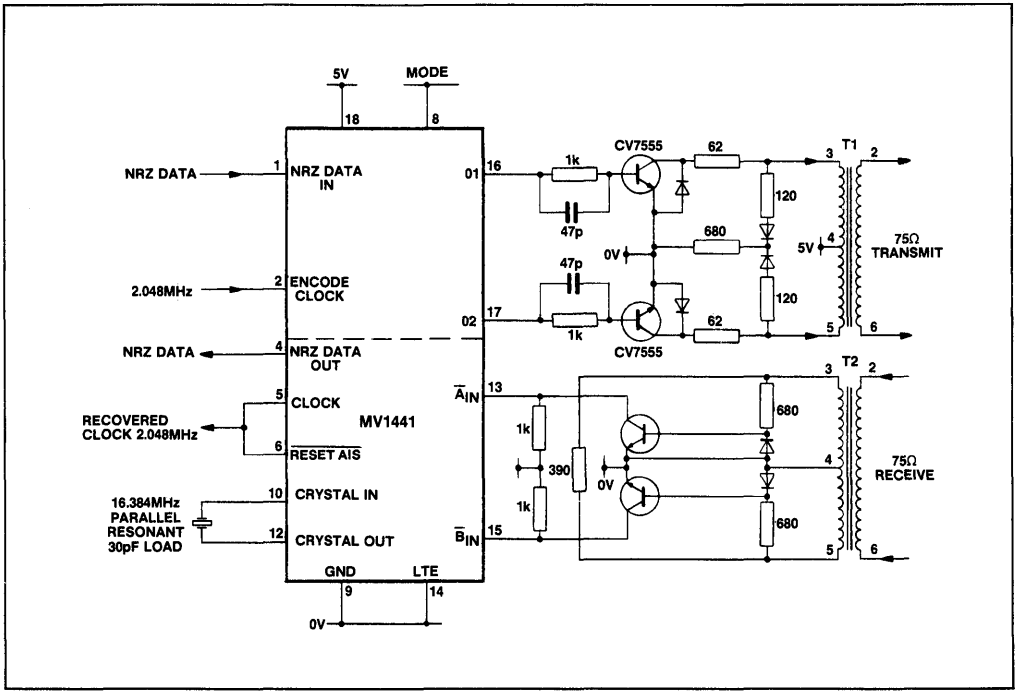

Fig.16 A typical application of the MV1441 with the interfacing to the transmission lines included

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8.5MBIT PCM SIGNALLING CIRCUIT

MV1448

HDB3 ENCODER/DECODER

This 8.544MBit PCM Signalling Circuit will perform the signalling and error detection functions for a 8.544MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuit is fabricated in CMOS and operates from a single 5V supply with TTL compatible inputs and outputs.

The MV1448 is an encoder/deocder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol. III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeros detection). In addition a loop back function is provided for terminal testing.

FEATURES

- HDB3 Encoding and Decoding to CCITT rec. G703
- Asynchronous Operation
- Simultaneous Encoding and Decoding
- Clock Recovery Signal Allows Clock Regeneration from Incoming HDB3 Data
- Loop Back Control
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector)
- Decoded Data in NRZ Form
- Low Power Operation
- 2.048MHz or 8.544MHz Operation

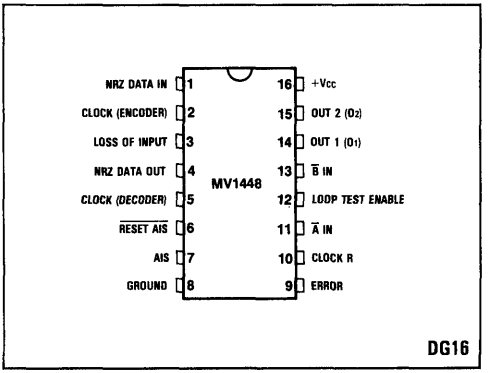


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	-0.5V to +7V
Inputs	Vcc +0.5V to GND -0.3V
Outputs	Vcc to GND -0.3V

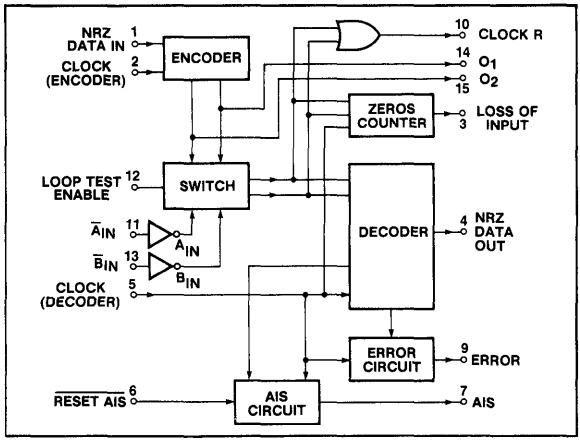


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 5V ± 0.5V Ambient temperature T_{amb} = 0°C to +70°C

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	All inputs	-0.3		0.8	V	
Low level input current	I_{IL}				50	μA	V_{IL} = 0V
High level input voltage	V_{IH}		2.0		V_{CC}	V	
High level input current	I_{IH}				50	μA	V_{IH} = 5V
Low level output voltage	V_{OL}	All outputs			0.4	V	Isink = 2.0mA
High level output voltage	V_{OH}		2.8			V	Isource = 2mA } both
			V_{CC}-0.75			V	Isource = 1mA } apply
Supply current	I_{CC}			2	4	mA	All inputs to 0V All outputs open circuit

Dynamic characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock (encoder) frequency	$Fmax_{enc}$	10			MHz	Figs. 10, 15
Max. clock (decoder) frequency	$Fmax_{dec}$	10			MHz	Figs. 11, 15
Propagation delay clock encoder to O_1, O_2	tpd1A/B		50		ns	Figs. 8, 10, 15 See Note 1
Rise and fall times O_1, O_2				20	ns	Figs. 10, 15
tpd1A - tpd1B difference				20	ns	Figs. 10, 15
Propagation delay clock to clock regenerate (clock R)	tpd3		50		ns	Loop test enable = '1', Figs. 10, 15
Setup time of NRZ data in to clock (encoder)	ts3		40		ns	Figs. 7, 10, 15
Hold time of NRZ data in	th3		40		ns	Figs. 7, 10, 15
Propagation delay $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock regenerate	tpd2		50		ns	Loop test enable = '0', Figs. 13, 15
Propagation delay clock (decoder) to error	tpd4		50		ns	Figs. 12, 15
Propagation delay $\overline{\text{Reset AIS}}$ falling edge to AIS output	tpd5		50		ns	Loop test enable = '0', Figs. 14, 15
Propagation delay clock (decoder) to NRZ data out	tpd6		50		ns	Figs. 7, 11, 15 See Note 2
Setup time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	ts1		40		ns	Figs. 7, 11, 15
Hold time of $\overline{A}_{IN}$, $\overline{B}_{IN}$ to clock (decoder)	th1		5		ns	Figs. 7, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	30			ns	Figs. 7, 14, 15
Setup time clock (decoder) to $\overline{\text{Reset AIS}}$	ts2		50		ns	Figs. 7, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = '1' to clock (decoder)	ts2	0			ns	Figs. 14, 15
Propagation delay clock (decoder) to LIP			50		ns	

High Density Bipolar 3 (HDB3) is a pseudo-ternary signal in which the number of consecutive zeros that may occur is restricted to a maximum number of three. In any sequence of four consecutive binary zeros, the ultimate zero is substituted by a 'mark' (+ or -) of the same polarity as the previous mark, i.e. it violates AMI code (Alternate Mark Inversion) and is termed a 'violation'. To ensure parity between marks of opposite polarity, the first zero is substituted by an additional mark when there would otherwise be an even number of marks between 'violations'. Thus violations alternate in polarity.

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in

Input data for encoding into ternary form. The data is clocked by the negative going edge of the Clock (Encoder).

2. Clock (Encoder)

Clock for encoding data on pin 1.

3. LIP

Loss if input circuit detects eleven consecutive zeros at the decoder input and then gives an output high. Any logic '1' at the input (A_{IN} or B_{IN} = '0') resets this count.

4. NRZ data out

Decoded binary data from pseudo-ternary inputs A_{IN} and B_{IN}.

5. Clock (Decoder)

Clock for decoding data on A_{IN} and B_{IN}, or O_1 and O_2 in loop test mode.

6,7. $\overline{\text{Reset AIS}}$, AIS

Logic '0' on Reset AIS resets a decoded zero counter and either resets AIS output to '0' provided 3 or more zeros have been decoded in the preceding Reset AIS = 1 period, or sets AIS to '1' if less than 3 zeros have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period to indicate loss of time slot zero. Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground

Zero volts.

9. Error

A logic '1' indicates that a violation of the HDB3 encoding law has been detected i.e. 3 '1's of the same polarity.

10. Clock R

OR function of $\overline{A}_{IN}$, $\overline{B}_{IN}$ for clock regeneration when pin 12 = '0', OR function of O_1, O_2 when pin 12 = '1'.

11,13. $\overline{A}_{IN}$, $\overline{B}_{IN}$

Inputs representing the received ternary PCM signal. $\overline{A}_{IN}$ = '0' represents a positive going '1', $\overline{B}_{IN}$ = '0' represents a negative going '1'. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ are sampled by the positive going edge of the clock decoder. $\overline{A}_{IN}$ and $\overline{B}_{IN}$ may be interchanged.

12. Loop test enable

TTL input to select normal or loop back operation. Pin 14 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 14 = '1' O_1, is connected internally to A_{IN} and O_2 to B_{IN}. Clock R becomes the OR function of O_1, O_2. N.B. A decode clock has to be supplied, or regenerated. The delay from NRZ in (pin 1) to NRZ out (pin 4) is about 6¾ clock periods in loop back.

14,15. O_1, O_2

Outputs representing the ternary encoded PCM HDB3 signal for line transmission. O_1 and O_2 are in Return to zero from and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length. Use suitable line drivers from these two outputs such that O_1 gives positive going pulse and O_2 gives negative going pulse.

16. $+V_{CC}$

Positive 5V ± 10% supply.

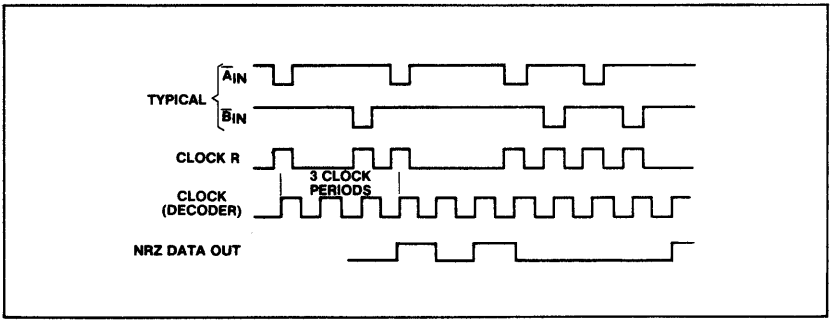


Fig. 3 Decode waveforms

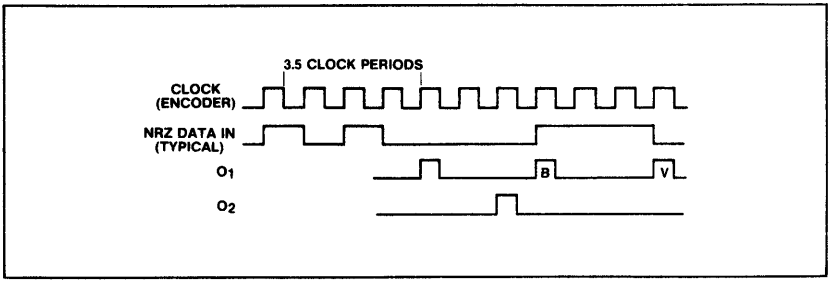


Fig.4 Encode waveforms

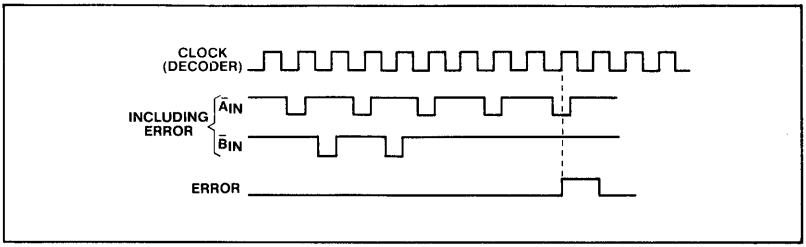


Fig.5 HDB3 error output waveforms

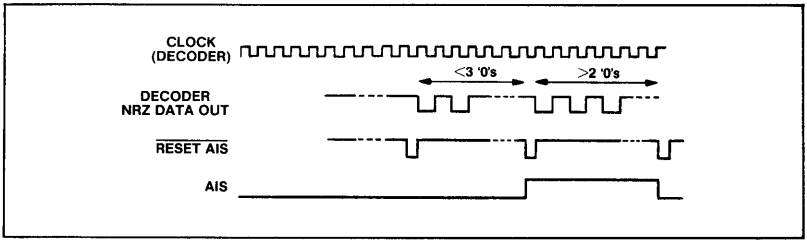


Fig.6 AIS error and Reset waveforms

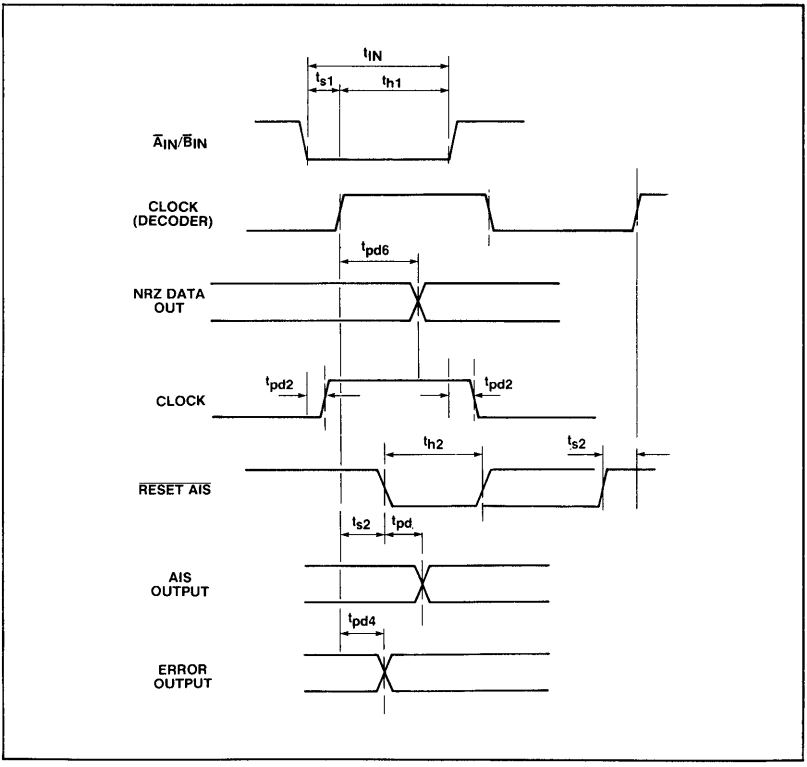


Fig.7 Decoder timing relationship

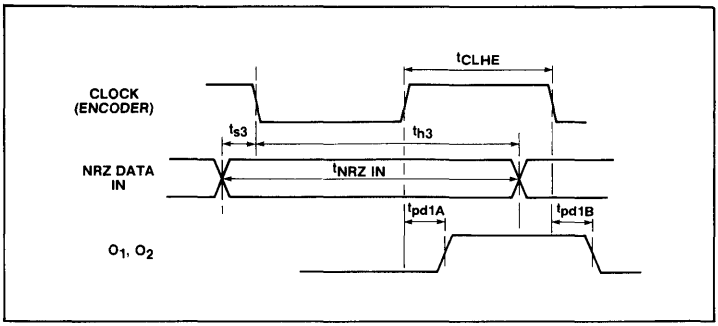


Fig.8 Encoder timing relationship

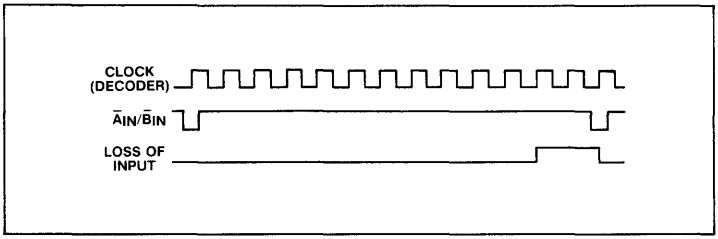


Fig.9 Loss of input waveforms

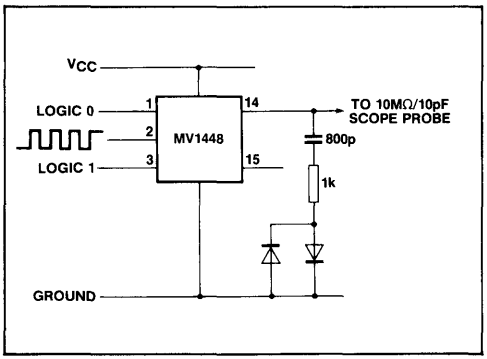


Fig.10

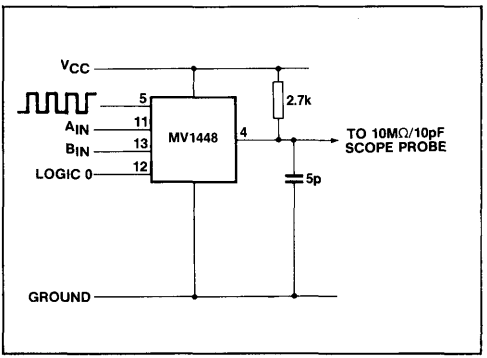


Fig.11

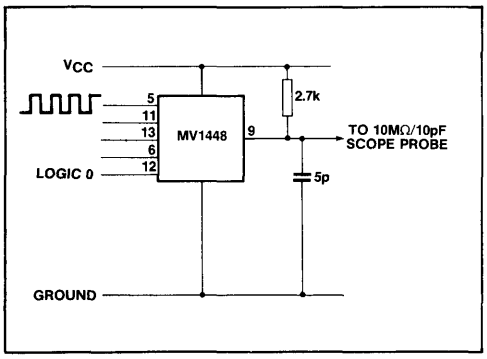


Fig.12

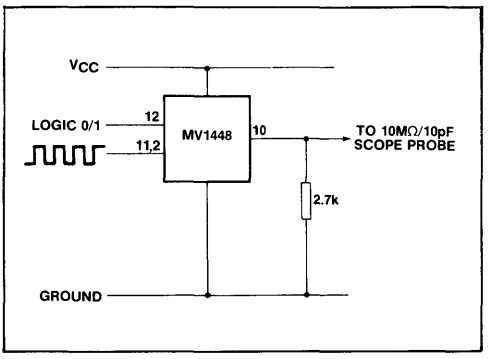


Fig.13

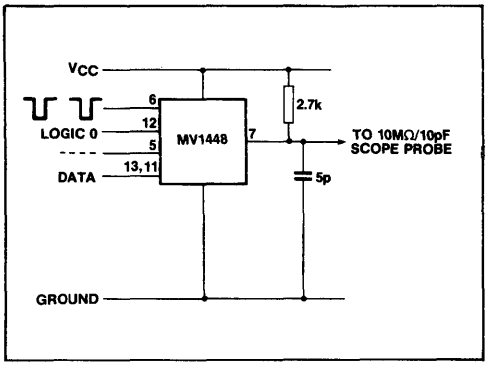


Fig.14

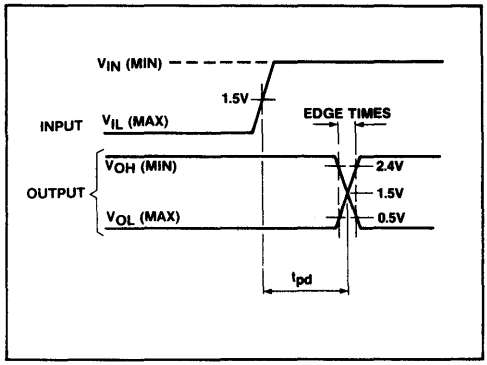


Fig.15 Test timing definitions

PLESSEY Semiconductors — CMOS

MV3506 A-LAW CODEC WITH FILTER
MV3507 μ-LAW CODEC WITH FILTER
MV3507A μ-LAW CODEC WITH FILTER AND A/B SIGNALLING

The MV3506 and MV3507 are silicon gate CMOS Companding Encoder/Decoder integrated circuits designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analogue to digital conversion circuits that conform to the desired transfer characteristic. The MV3506 provides the European A-Law companding and the MV3507 provides the North American μ-Law companding characteristic.

These circuits provide the interface between the analogue signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operates from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or asynchronous operation.

In 22-pin packages (0.400in centres) the MV3506/MV3507 are ideally suited for PCM applications: Exchange, PABX, Channel Bank or Digital Telephone as well as fibre optic and other non-telephone uses. A 28 pin version, the MV3507A, provides standard μ-Law A/B signalling capability.

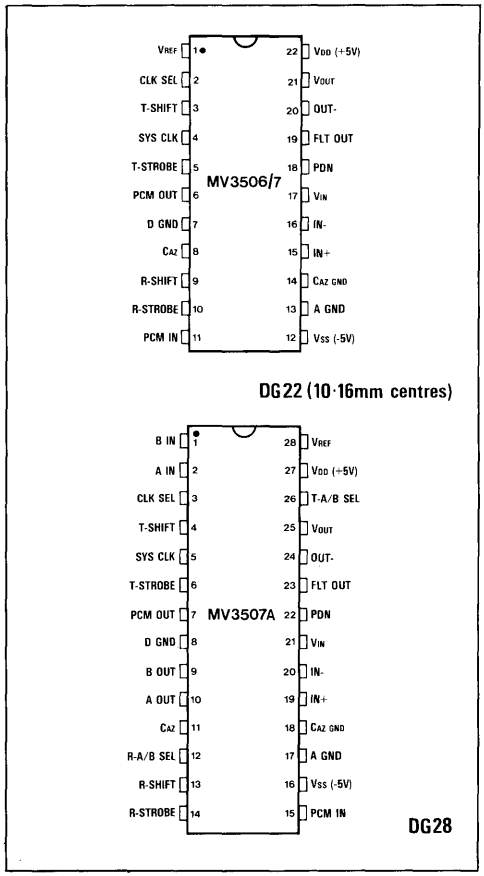


Fig.1 Pin connections - top view

FEATURES

- Independent Transmit and Receive Sections with 75dB Isolation
- Low power CMOS 80mW (Operating) 10mW (Standby)
- Stable Voltage Reference On-chip
- Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- Input Analogue Filter Eliminates Need for External Anti-aliasing Prefilter
- Input/Output Op. Amps for Programming Gain
- Output Op. Amp Provides ±3.1V Into a 1200 Ohms load or Can Be Switched Off for Reduced Power (70mW)
- Special Idle Channel Noise Reduction Circuitry
- Encoder has Dual-speed Auto-zero Loop for Fast Acquisition on Power-up
- Low Absolute Group Delay = 410μsec. at 1kHz

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{DD}: +6.0V
DC Supply Voltage V_{SS}: -6.0V
Operating Temperature: -40°C to +125°C
Storage Temperature: -65°C to +150°C
Power Dissipation at 25°C: 1000mW
Digital Input: V_{SS} -0.3≤V_{IN}≤V_{DD} -0.3
Analogue Input: V_{SS} -0.3≤V_{IN}≤V_{DD} -0.3

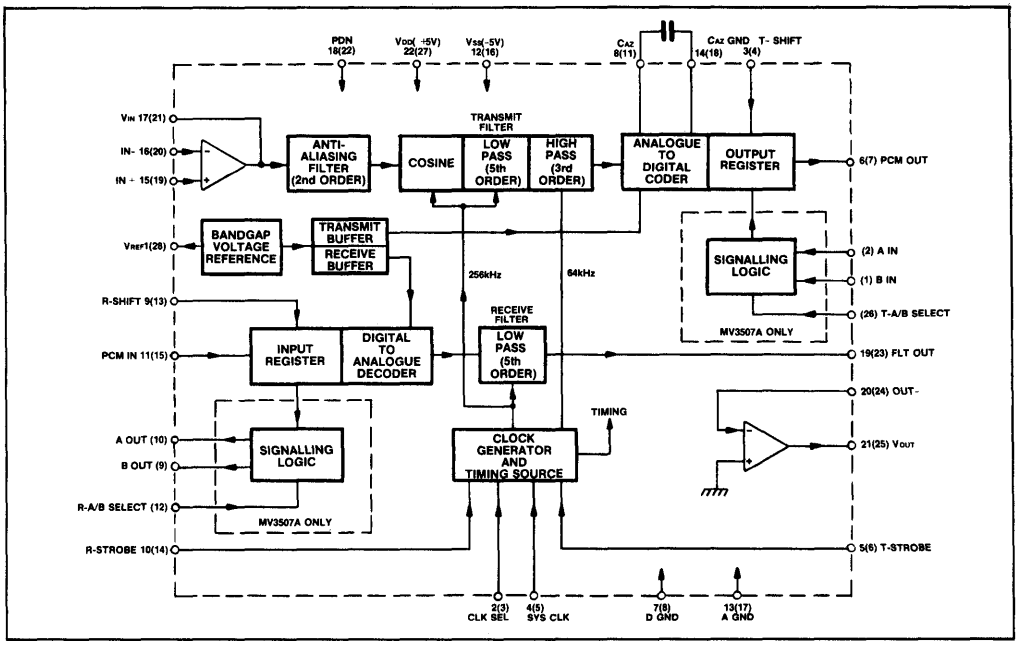


Fig.2 MV3506/MV3507/MV3507A block diagram. Pin numbers for the MV3507A are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to +70°C

Power Supply Requirements

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply	V_{DD}	4.75	5.0	5.25	V	
Negative supply	V_{SS}	-4.75	-5.0	-5.25	V	
Power dissipation (operating)	P_{OPR}		80	110	mW	V_{DD} = 5.0V, V_{SS} = -5.0V
Power dissipation (operating w/o output op. amp	P_{OPR}		70		mW	
Power dissipation (standby)	P_{STBY}		10	20	mW	

AC Characteristics (see Fig. 6)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
System clock duty cycle	D_{SYS}	40	50	60	%	At 1.544MHz or 2.048MHz
Shift clock frequency	f_{SC}	0.064		2.048	MHz	
Shift clock duty cycle	D_{SC}	40	50	60	%	
Shift clock rise time	t_{rc}			100	ns	
Shift clock fall time	t_{fc}			100	ns	
Strobe rise time	t_{rs}			100	ns	
Strobe fall time	t_{fs}			100	ns	
Shift clock to strobe (On) delay	t_{sc}	-100	0	200	ns	
Strobe width	t_{sw}	600ns		124.3μs		At 2.048MHz,700ns min at 1.544MHz
Shift clock to PCM out delay	t_{cd}		100	150	ns	
Shift clock to PCM in set-up time	t_{dc}	60			ns	
PCM output rise time C_L = 100pF	t_{rd}		50	100	ns	To 3V;510Ω to V_{DD}
PCM output fall time C_L = 100pF	t_{fd}		50	100	ns	To 0.4V;510Ω to V_{DD}
A/B select to strobe trailing edge	t_{dss}	100			ns	

DC Characteristics at V_{DD} = +5V, V_{SS} = -5V, V_{ref} = -3.075V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analogue input resistance	R_{INA}	100			kΩ	
Input capacitance	C_{IN}		7	15	pF	All logic and analogue inputs
Logic input low current (Shift clock, PCM IN, System clock)	I_{INL}			1	μA	V_{IL} = 0.8V
Logic input high current	I_{INH}			1	μA	V_{IH} = 2.0V
Logic input low current (Strobe, A/B Sel, A IN B IN, PDN)	I_{INL}			600	μA	V_{IL} = 0.8V
Logic input high current	I_{INH}			600	μA	V_{IH} = 2.0V
Logic input 'low' voltage	V_{IL}			0.8	V	
Logic input 'high' voltage	V_{IH}	2.0			V	
Logic output 'low' voltage (PCM out)	V_{OL}			0.4	V	510Ω pull-up to V_{DD} + 2 LS TTL
Logic output 'low' voltage (A/B out)	V_{OL}			0.4	V	I_{OL} = 1.6mA
Logic output 'high' voltage	V_{OH}	2.6			V	I_{OH} = 40μA
Output load resistance V_{OUT}	R_L	1200			Ω	C_L = 50pF max.

Transmission Delays

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Encoder			125		μs	From T_{STROBE} to the start of digital transmitting
Decoder		30	8T+25		μs	T = Period in μs of R_{SHIFT} CLOCK
Transmit section filter				182	μs	At 1kHz
Receive section filter				110	μs	At 1kHz

MV3506 Single-Chip A-Law Filter/Codec Linear Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Idle channel noise (weighted noise)	ICN_W		-85	-73	dBm0p	CCITT G.712 5.1
Idle channel noise (single frequency noise)	ICN_{SF}			-60	dBm0	CCITT G.712 5.2
Idle channel noise (receive section)	ICN_R			-78	dBm0p	CCITT G.712 5.3
Spurious out-of-band signals at the channel output				-30	dBm0	CCITT G.712 7.1
Intermodulation (2 tone method)	IMD_{2F}			-35	dBm0	CCITT G.712 8.1
Intermodulation (1 tone + power frequency)	IMD_{PF}			-49	dBm0	CCITT G.712 8.2
Spurious in-band signals at the channel output port				-40	dBm0	CCITT G.712 10
Inter-channel crosstalk $V_{IN-VOUT}$		75	80		dB	CCITT G.712 12
Max.coding analogue input level	$V_{IN}(max)$		±3.1		V_{0pk}	
Max.coding analogue output level	$V_{OUT}(max)$		±3.1		V_{0pk}	R_L = 1.2kΩ
Gain variation with temperature and power supply	ΔG		±0.25		dB	
Transmit gain repeatability			±0.1	±0.2	dB	
Receive gain repeatability			±0.1	±0.2	dB	
Zero transmission level point (decoder) (see Fig. 3)	$0TLP_R$		+5.8		dBm	V_{OUT} digital milliwatt response
Zero transmission level point (encoder)	$0TLP_T$		+5.8		dBm	V_{IN} to yield same as digital milliwatt response at decoder

MV350(7)A Single-Chip μ-Law Filter/Codec Linear Characteristics

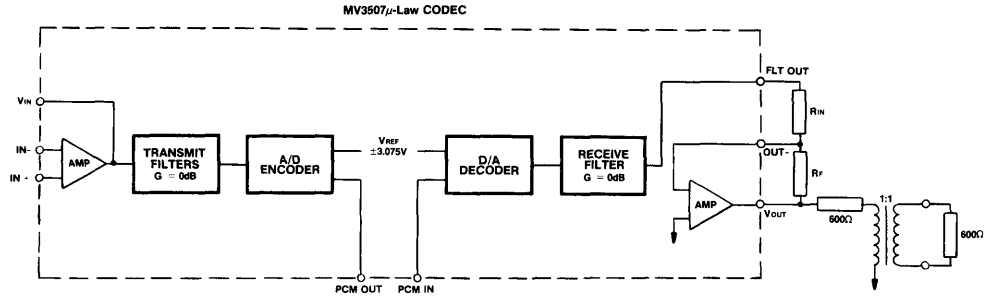
Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Idle channel noise (weighted noise)	ICN_W		5	17	dBrnc0	CCITT G.712 5.1
Idle channel noise (single frequency noise)	ICN_{SF}			-60	dBm0	CCITT G.712 5.2
Idle channel noise (receive section)	ICN_R			15	dBrnc0	CCITT G.712 5.3
Spurious out-of-band signals at the channel output				-28	dBm0	CCITT G.712 7.1
Intermodulation (2 tone method)	IMD_{2F}			-35	dBm0	CCITT G.712 8.1
Intermodulation (1 tone + power frequency)	IMD_{PF}			-49	dBm0	CCITT G.712 8.2
Spurious in-band signals at the channel output port				-40	dBm0	CCITT G.712 10
Inter-channel crosstalk V_{IN}-V_{OUT}		75	80		dB	CCITT G.712 12
Max.coding analogue input level	$V_{IN}(max)$		±3.1		V_{0pk}	
Max.coding analogue output level	$V_{OUT}(max)$		±3.1		V_{0pk}	R_L = 1.2kΩ
Gain variation with temperature and power supply	ΔG		±0.25		dB	
Transmit gain repeatability			±0.1	±0.2	dB	
Receive gain repeatability			±0.1	±0.2	dB	
Zero transmission level point (decoder) (see Fig. 3)	$0TLP_R$		+5.8		dBm	V_{OUT} Digital milliwatt response
Zero transmission level point (encoder)	$0TLP_T$		+5.8		dBm	V_{IN} to yield same as digital milliwatt response at decoder

PIN/FUNCTION DESCRIPTIONS

Name	Pin		Description
	MV3506/ MV3507	MV3507A	
SYS CLK	4	5	**System Clock** This pin is a TTL compatible input for either a 1.544MHz or a 2.048MHz clock that is divided down to provide the filter clocks. The status of CLK SEL pin must correspond to the provided clock frequency.
T-SHIFT	3	4	**Transmit Shift Clock** This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
R-SHIFT	9	13	**Receive Shift Clock** This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
T-STROBE	5	6	**Transmit Strobe** This TTL compatible pulse input (8kHz) is used for analogue sampling and for initiating the PCM output from the coder. It must be synchronised with the T-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
R-STROBE	10	14	**Receive Strobe** This TTL compatible pulse input (typ. 8kHz) initiates clocking of PCM input data into the decoder. It must be synchronised with the R-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
CLK SEL	2	3	**Clock Select** This pin selects the proper divide ratios to utilise either 1.544MHz or 2.048MHz as the system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz and to V_{SS} (-5V) for 1.544MHz operation. If this pin is connected to DGND, 256kHz may be used as the system clock.
PCM OUT	6	7	**PCM Output** This is a LS TTL compatible open-drain output. It is active only during transmission of PCM output for 8-bit periods of T-SHIFT clock signal following a positive edge on the T-STROBE input. Data is clocked out by the positive edge of the T-SHIFT clock into one 510Ω pull-up per system plus 2 LS TTL inputs.
PCM IN	11	15	**PCM Input** This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of T-SHIFT clock.

PIN/FUNCTION DESCRIPTIONS

Name	Pin		Description
	MV3506/ MV3507	MV3507A	
C_{AZ}	8	11	**Auto Zero Capacitor** A capacitor of 0.1μF ±20% should be connected between these pins for coder auto zero operation.
C_{AZ}GND	14	18	Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
V_{REF}	1	28	*Output of the internal* **Band-gap Reference Voltage** *(-3.075V) generator is* brought out to V_{REF} pin.
IN +	15	19	**Analogue input.** IN- and IN + are the inputs of a high input impedance op. amp and V_{IN} is the output of this op. amp. These three pins allow the user complete control over the input stage so that it can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain of as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel. channel.
IN-	16	20	
V_{IN}	17	21	
FLT OUT	19	23	**Filter Out** This is the output of the low pass filter which represents the recreated analogue signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 20kΩ.
OUT-	20	24	**Output and input of the uncommitted output amplifier stage.** Signal at the FLT OUT pin can be connected to this amplifier to realise a low output impedance with unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into 600Ω load. (See Fig. 3.) If OUT- is connected directly to V_{SS} the op. amp will be powered down, reducing power consumption by 12mW, typically.
V_{OUT}	21	25	
V_{DD}	22	27	**Power supply pins.** V_{DD} and V_{SS} are positive and negative supply pins, respectively (typ. +5V, -5V).
V_{SS}	12	16	
A GND	13	17	**Analogue and Digital Ground pins** are separate for minimising crosstalk and digital interference.
D GND	7	8	
PDN	18	22	**Power Down** This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
A IN		2	The **Transmit A/B select** input (T-A/B SEL) selects the **A signal** input in a positive transition and the **B signal** input on the negative transition. These inputs are TTL compatible. The A/B signalling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronised to the T-STROBE input in each device.
B IN		1	
T-A/B SEL		26	
A OUT		10	In the decoder the A/B signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which the **Receive A/B select (R-A/B SEL)** input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.
B OUT		9	
R-A/B SEL		12	



$$OTLP_{IN} = -\left[G - 20\log\left(\frac{V_{REF}}{1.58}\right)\right]$$

$$= -\left[0 - 20\log\left(\frac{3.075}{1.58}\right)\right]$$

= +5.8dBm at the V_{IN} terminal

$$OTLP_{OUT} = \left[G + 20\log\left(\frac{V_{REF}}{1.58}\right)\right]$$

$$= \left[0 + 20\log\left(\frac{3.075}{1.58}\right)\right]$$

= +5.8dBm at the FLT_{OUT} terminal

(Note: The 1.58V value is that value of reference voltage that would allow the peak value of +3.17dBm as the maximum coded value, resulting in a OTLP of 0dBm. For A-Law it would be 1.57V for +3.14dBm.)

Since the output buffer amplifier is designed to drive 1200Ω, a 600Ω resistor in series with the 600Ω load divides the available voltage in half resulting in a $OTLP_{OUT}$ to the load of -0.2dBm.

For a system where OTLP is chosen to be 0dBm the input op. amp. should be configured for 5.8dB gain and the output op. amp. for 0.2dB gain. R_{IN} should be ⩾20kΩ.

Fig.3 MV3507 and MV3507A μ-law Codec input/output reference signal levels

Power Down Logic

Powering down the Codec can be done in several ways. The most direct is to drive the PDN pin to a low level. Stopping both the transmit strobe and the receive strobe will also put the chip into the stand-by mode. The strobes can be held high, low or disconnected.

Voltage Reference Circuitry

A temperature compensated band-gap voltage generator (-3.075V) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimise crosstalk. This reference voltage is trimmed to within ±27mV during assembly to ensure a minimum gain error of ±0.2dB due to all causes.

FUNCTIONAL DESCRIPTION

Figure 2 shows the simplified block diagram of the MV3506/MV3507. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A band-gap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analogue signals first enter the chip at the uncommitted op. amp terminals. This op. amp allows gain trim to be used to set 0TLP in the system. From the V_{IN} pin the signal enters the 2nd Order analogue anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typ) at 256kHz and 44dB (typ) at 512kHz. From the cosine filter the signal enters a 5th Order low-pass filter clocked at 256kHz, followed by a 3rd Order high-pass filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are 26dB (typ) from 0 to 60Hz and 35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analogue-to-digital conversion process requires 9 1/2 clock cycles, or about 72μs. The 8 bit PCM date is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

Included in the circuitry of the MV3507 is 'All Zero' code suppression so that negative input signal values between decision values numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronisation by TI line clock recovery circuitry as there are never more than 15 consecutive zeroes.

An additional feature of the Codec is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of the chip is such that for 250ms the only code words generated were +0, -0, +1 or -1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation resetting the 250ms timer. This feature is a form of Idle Channel Noise 'Squelch' or 'Crosstalk Suppression'. It is of particular importance in the MV3506 A-Law version because the A-Law transfer characteristic has 'mid-riser' bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialised to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order low-pass filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalisation to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 20kΩ. When used in this fashion the low impedance output amp can be switched off for a considerable savings in power consumption. When it is required to drive a 600Ω load the output is configured as shown in Fig. 3 allowing gain trimming as well as impedance matching. With this configuration a transmission level of 0dBm can be delivered into the load with the +3.14dB or +3.17dB overload level being the maximum expected level.

Timing Requirements

The internal design of the Single-Chip Codec paid careful attention to the timing requirements of various systems. In North America, central office and channel bank designs follow the American Telephone and Telegraph Company's TI Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Nevertheless, in digital telephone designs, Codec's may be used in a non-multiplexed form with a data rate as low as 64kb/s. The MV3507 and MV3507A fulfil these requirements.

In Europe, telephone exchange and channel bank designs follow the CCITT carrier PCM format to multiplex 30 voice channels at a data rate of 2.048Mb/s. The MV3506 is designed for this market and will also handle PABX and digital telephone applications requiring the A-Law transfer characteristics.

The timing format chosen for the Plessey Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kb/s to 2.048Mb/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, the MV3506/MV3507 does not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+)edges of the strobe, forcing the PCM output in high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and transmit/receive shift clocks are synchronised to it. Figures 4 and 5 show the waveforms in typical multiplexed uses of the Codec.

System Clock

The basic timing of the Codec is provided by the system clock. This 2.048MHz or 1.544MHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. In most systems this clock will also be used as the shift clock to clock in and out the data. However, the shift clock can actually be any frequency between 64kHz and 2.048MHz as long as one of the two system clock frequencies is provided. Independent strobes and shift clocks allow asynchronous operation of transmit and receive.

Signalling In μ-Law Systems

The MV3506 and MV3507 are compact 22-pin devices to meet the two worldwide PCM standards. In μ-Law systems there can be a requirement for signalling information to be carried in the bit stream with the coded analogue data. This coding scheme is sometimes called 7 5/6 bit rather than 8 bit because of the LSB every 6th frame being replaced by a signalling bit. This is referred to as A/B Signalling and if a signalling frame carries the 'A' bit, then 6 frames later the LSB will carry the 'B' bit. To meet this requirement, the MV3507A is available in a 28-pin package, as 6 more pins are required for the inputs and outputs of the A/B signalling.

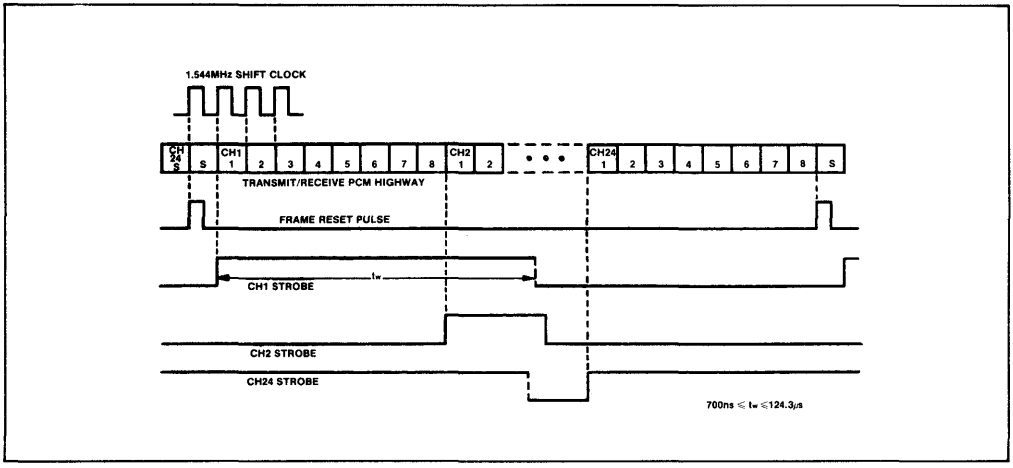


Fig.4 Waveforms in a 24 channel PCM system

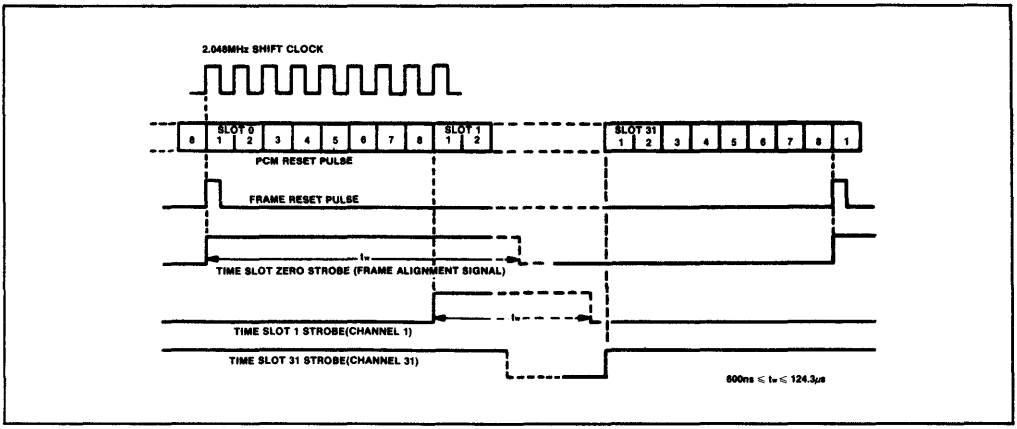
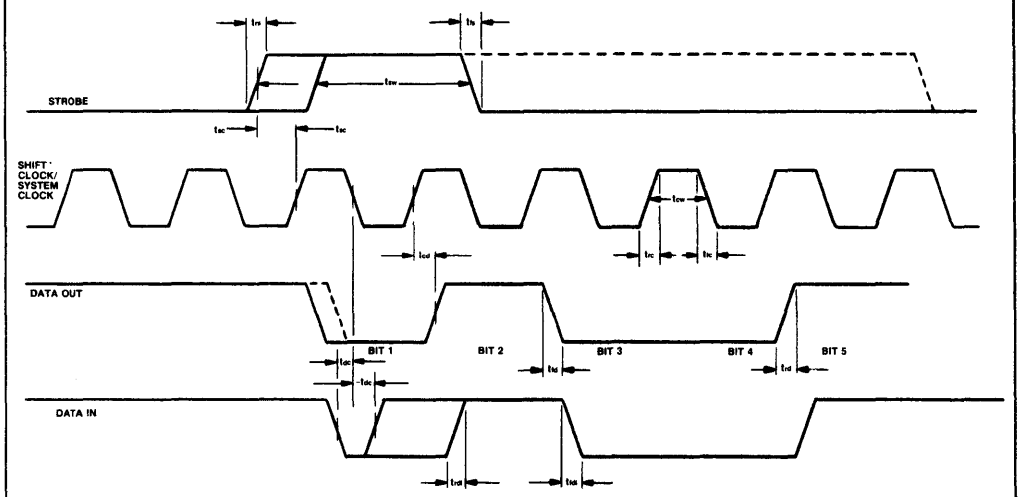


Fig.5 Waveforms in a 30 channel PCM system



*In this example the shift clock is the system clock (1.544 or 2.048MHz). In systems where the data shift rate is not the same the relationship of each to the strobe remains the same. The system clock and shift clock need not have coincident edges, but must relate to the strobe within the t_{sc}, timing requirements.
The effect of the strobe occurring after the shift clock is to shorten the first (sign) bit at the data output.
The length of the strobe is not critical. It must be at a logic state longer than one system clock cycle. Therefore, the minimum would be >488ns at 2.048 and the maximum <124.3μsec at 1.544MHz.

Fig.6 Waveform details

	Min.	Max.
t_{cw}	195nsec	9.38μsec
t_{rs}		100ns
t_{fs}		100ns
t_{sc}	-100ns	200ns**
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	600ns*	124.3μsec
t_{cd}	100ns	150ns
t_{dc}	60ns	
t_{rdi}		100ns
t_{fdi}		100ns

*At 2.048MHz, 700ns at 1.544MHz
**That is, the strobe can produce the shift clock by 200ns, or follow it by as much as 100ns.

Signalling Interface

In the AT&T TI carrier PCM format an A/B signalling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground, etc., depending on the application. Two signalling conditions (A and B) per channel, giving four possible signalling states per channel are repeated every 12 frames (1.5 milliseconds). The A signalling condition is sent in bit 8 of all 24 channels in frame 6. The B signalling conditions is sent in frame 12. In each frame, bit 193 (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The MV3507A in a 28-pin package is designed to simplify the signalling interface. For example, the A/B select input pins are transition sensitive. The Transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronises the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channel bank. The A and B signalling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore, A/B select input must go positive in the beginning of frame 5 and negative in the beginning of frame 11 (see Fig. 7).

The decoder uses a similar scheme for receiving the A and B signalling bits, with one difference. They are latched to the respective outputs in the same frame in which the A/B select input makes a transition. Therefore, the Receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

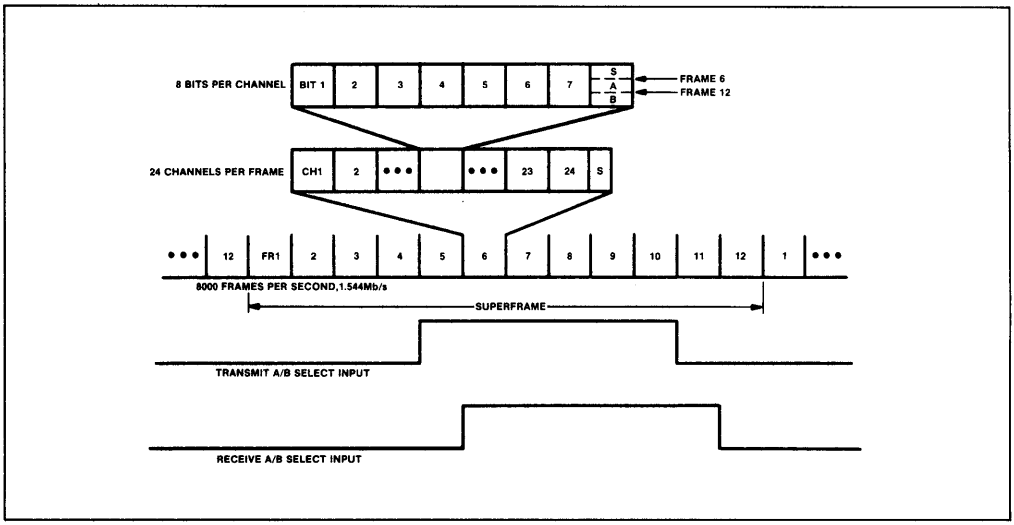


Fig.7 Signalling waveforms in a TI carrier system

In the TI carrier system, 24 voice channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mb/s. Within the channel bank the transmit and receive channels of a Codec can occupy the same time slot for a synchronous operation or they can be independent of each other for asynchronous operation. Asynchronous operation helps minimise switching delays through the system. Since the timing interface for the coder and decoder sections is independent of each other in the MV3507A, it can be operated in either manner.

In the CCITT carrier system 30 voice channels and 2 framing and signalling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mb/s.

The line supervision and control circuitry within each subscriber line interface can generate all the timing signals for the associated Codec under control of a central processor. Alternatively, a common circuitry within the channel bank can generate the timing signals for all channels. Generation of the timing signals for the MV3506 and MV3507A is straightforward because of the simplified timing requirements (see timing requirements for details). Figures 9 and 10 show design schemes for generating these timing signals in a common circuitry. Note that only three signals; a shift clock, a frame reset pulse (coincident with the S bit) and a superframe reset pulse (coincident with the S bit in Frame 1) are needed. These signals are generated by clock recovery circuitry in the channel bank. Since the Plessey Codec does not need channel strobes to be exactly 8-bit periods wide, extra decoding circuitry is not needed.

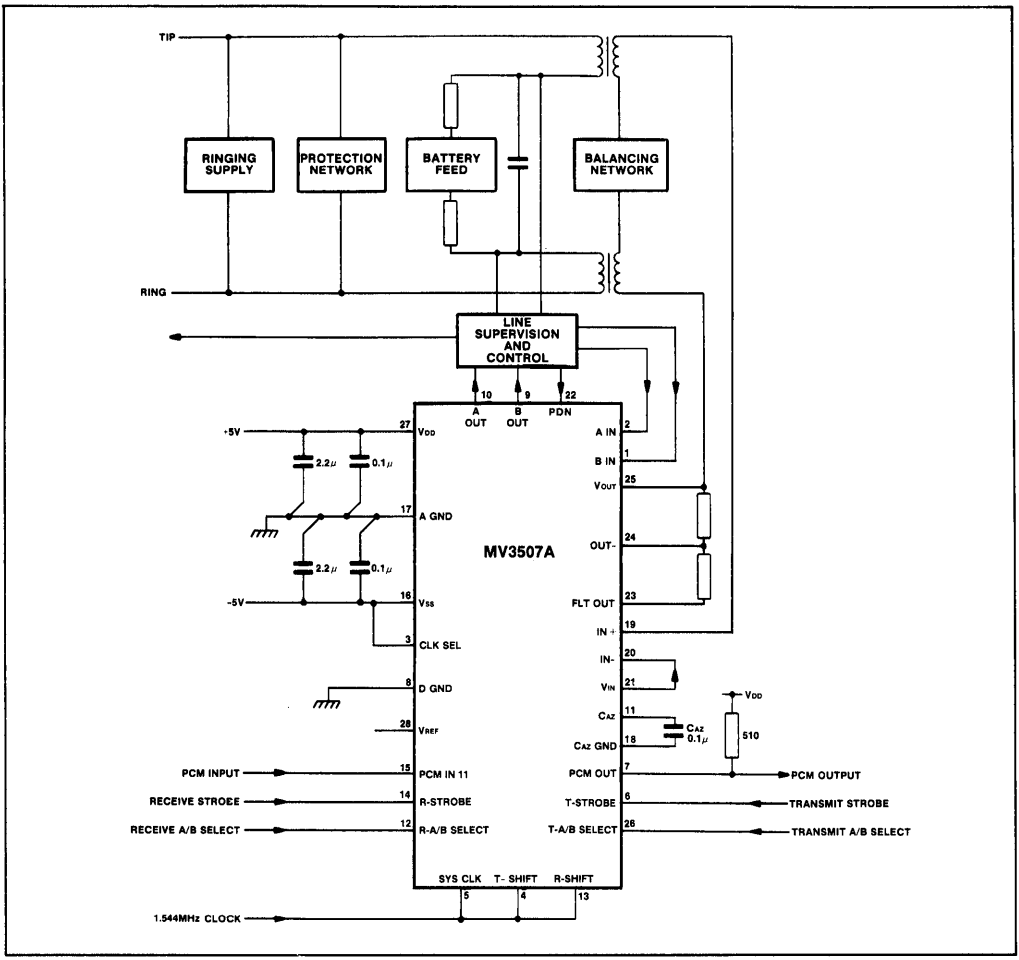


Fig.8 A subscriber line interface circuit

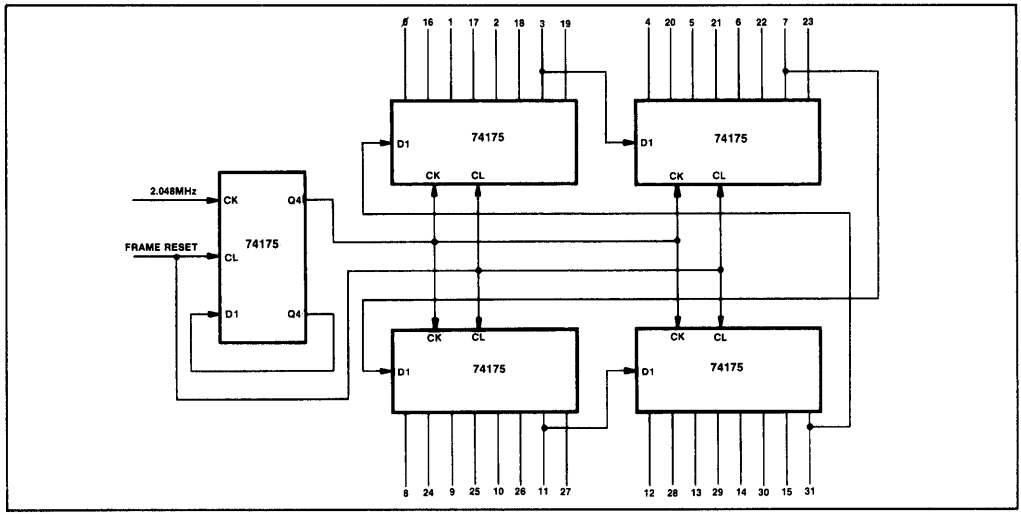


Fig.9 Generating timing signals in a CCITT carrier system (30 + 2 channels)

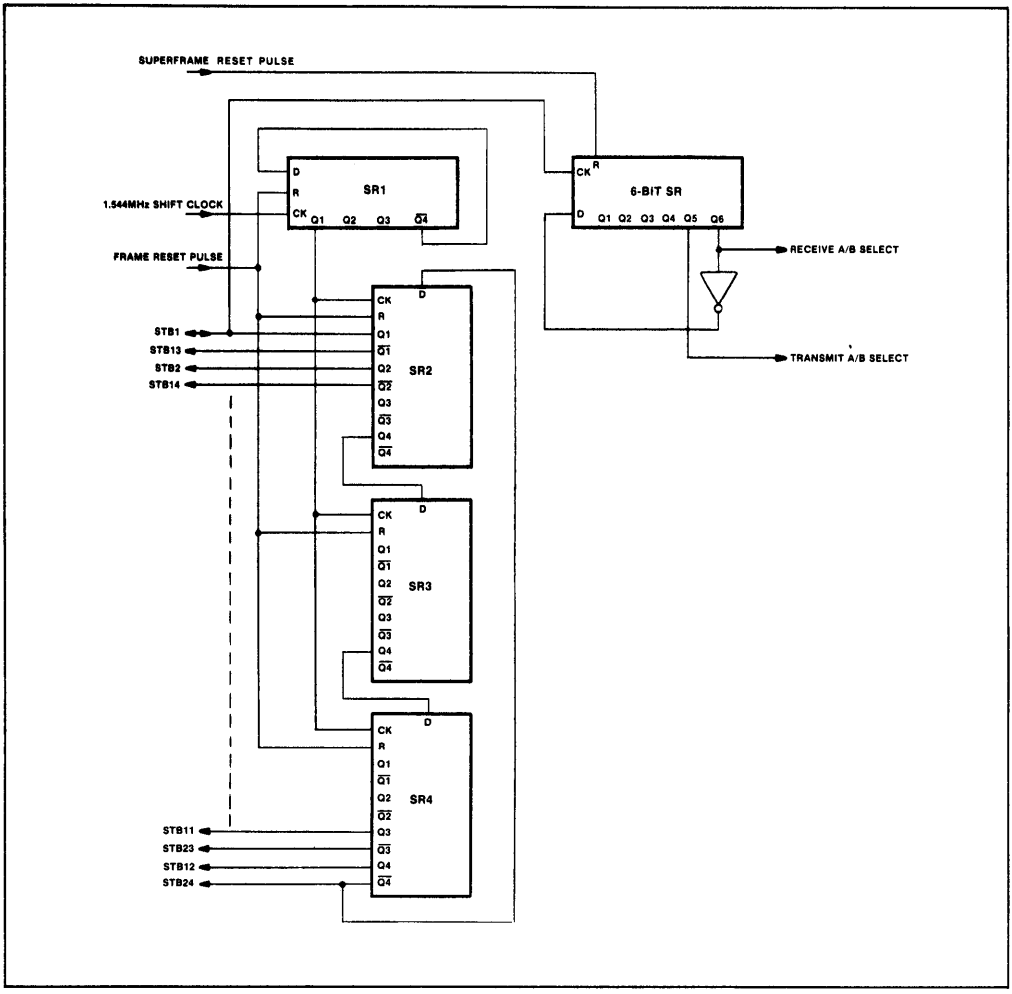


Fig.10 Generating timing signals in a TI carrier system

A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs of interface to the switch. Two pairs carry transmit and receive PCM voice date. One pair supplies an 8kHz synchronising clock signal and the remaining pair supplies power to the telephone. More sophisticated techniques minimise the number of wire pairs. The Plessey Single-Chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 11 shows a schematic for a typical digital telephone design.

Since asynchronous operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 2048kHz system clock and 64kHz shift clock from the 8kHz synchronising signal received from the switch. The synchronising signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output directly feeds into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

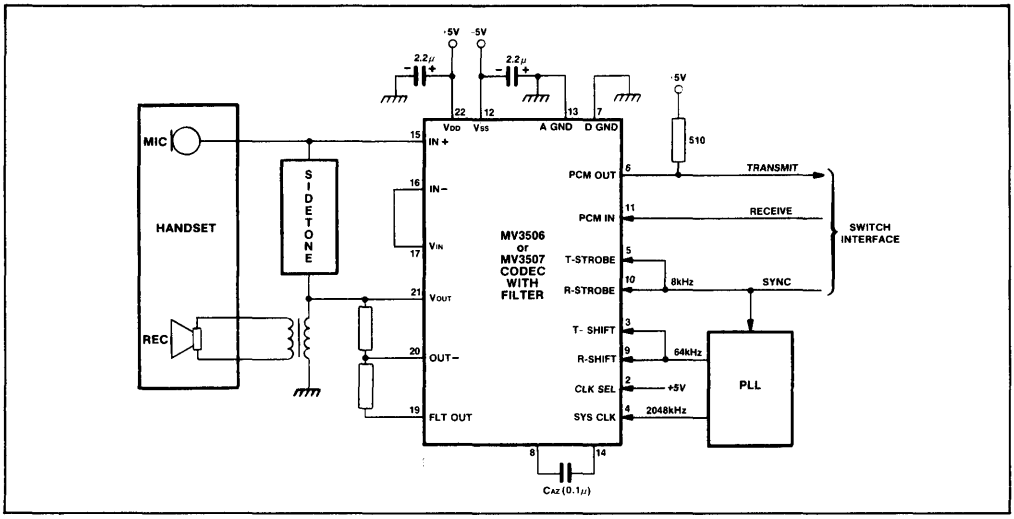


Fig.11 Voice processing in a digital telephone application

PLESSEY Semiconductors — CMOS

MV4320

KEYPAD PULSE DIALLER

The MV4320 series is fabricated using ISO-CMOS high density technology. The device is a pin-for-pin replacement for the DF320 Loop Disconnect Dialler and offers wider operating supply voltage range and lower power dissipation. The MV4320 accepts up to 20 digits from a standard 2 of 7 keypad and offers a REDIAL option activated by key #. The device provides dial pulsing and muting outputs and has a HOLD pin for interrupting a dialling sequence. Outpulsing mark/space ratio and dialling speed are pin selectable.

The MV4320 is available in Ceramic DIL (DG, -40° C to +85° C).

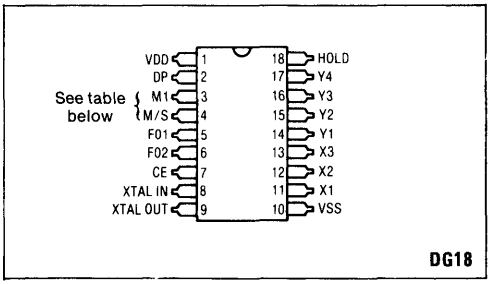


Fig.1 Pin connections (top view)

FEATURES

- Pin for Pin Replacement for the DF320
- 2.5V to 5.5V Supply Voltage Operating Range
- 375μW Dynamic Power Dissipation at 3V
- Uses Inexpensive 3.58 MHz Ceramic Resonator or Crystal
- Stores up to 20 Digits
- Selectable Outpulsing Mark/Space Ratio
- Selectable Dialling Speeds of 10, 16, 20 and 932 Hz
- Low Cost

APPLICATIONS

- Pushbutton Telephones
- Tone to Pulse Converters
- Mobile Telephone
- Repertory Dialers

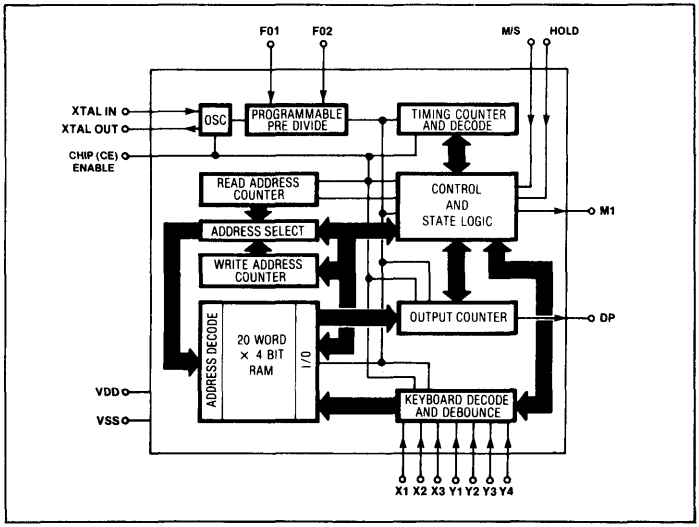


Fig.2 MV4320 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{DD} = 3.0V$; $T_{amb} = +25°C$; $f_{CLK} = 3.579545MHz$
All voltages wrt V_{SS}

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.5		5.5	V		
2		Standby Supply Current		I_{DDS}		1.0	10.0	μA	CE = V_{SS}	
3		Operating Supply Current		I_{DD}		125	200	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-12.0	μA	$V_{IN} = V_{SS}$	X_1,X_2,X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1,Y_2,Y_3,Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S,IDP,F01,
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	12.0	μA	$V_{IN} = V_{DD}$	F02,FD,HOLD
8		Logic '0' Level		V_{IL}			0.9	V	All inputs	
9		Logic '1' Level		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	$V_{OUT} = 2.3V$	DP, M1/M2
13			P-Channel Source	I_{OH}	-0.8	-2.0		mA	$V_{OUT} = 0.7V$	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{DD} = 3.0V$; $T_{amb} = +25°C$; $f_{CLK} = 3.579545MHz$
All voltages wrt V_{SS}

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
14	DYNAMIC	Output Rise Time	t_R		1.0		us	DP,M_1.
15		Output Fall Time	t_F		1.0		us	C_L = 50pF
16		Maximum Clock Frequency	t_{CLK}	3.58			MHz	3.579545 MHz Crystal
17		Mark to Space Ratio	M/S		2:1			Note 1
18					3:2			
19		Impulsing Rate = $\frac{1}{T}$			10		Hz	Note 1
20					16			
21					20			
22					932			
23		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE '1'
24		Input Capacitance	C_{in}		5.0		pF	Any Input

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

NOTES:
1. See Pin Function, Table 1.

OPERATING NOTES

The first key entered in any dialling sequence initiates the oscillator by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in figures 3 and 4. Figure 3 shows use of the circuits with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialler circuit. In this mode, the pulse occurring on M1 when CE is taken high, with no keypad input, can be used to initiate the bistable latching relay. Figure 4 shows the timing diagram for the CE internal control mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously.

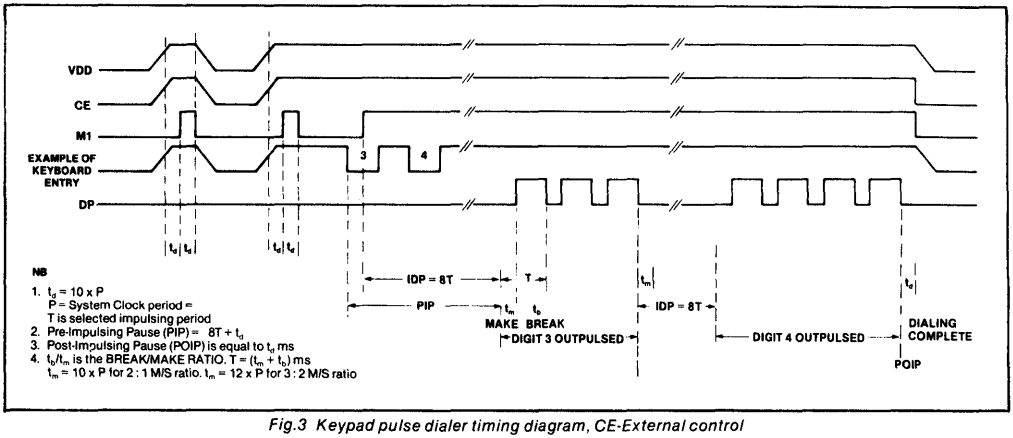


Fig.3 Keypad pulse dialer timing diagram, CE-External control

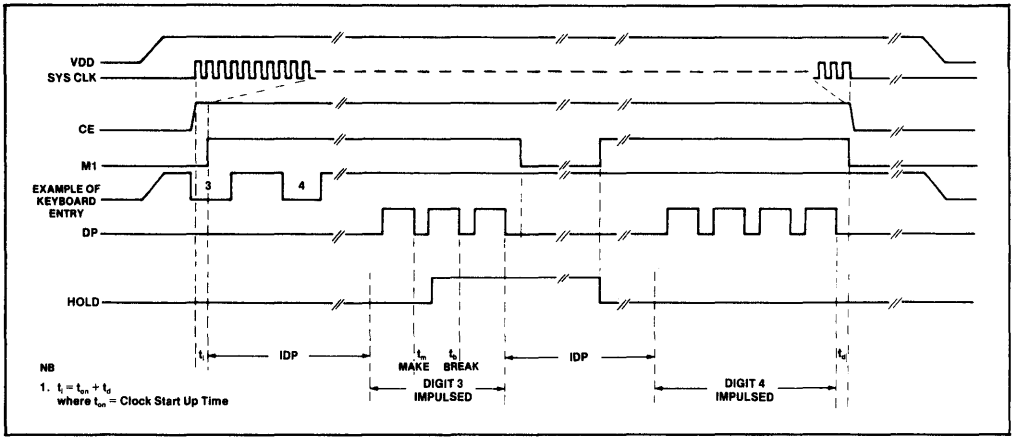


Fig.4 Keypad pulse dialer timing diagram, CE-Internal control

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN.	MAX.
V_{DD}-V_{SS}	-0.3V	10V
Voltage on any pin	V_{SS} -0.3V	V_{DD} +0.3V
Current at any pin		10mA
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C
Power Dissipation		1000mW

Derate 16mW/°C above 75°C. All leads soldered to PC board.

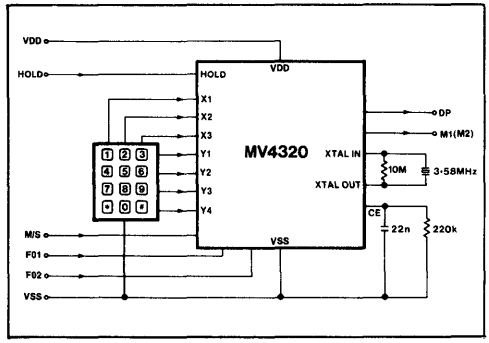


Fig.5 Application diagram

PIN FUNCTIONS

<table>
<tr><td>V_{DD}</td><td colspan="6">Positive voltage supply</td></tr>
<tr><td>DP</td><td colspan="6">Dial Pulsing Output Buffer</td></tr>
<tr><td>M1</td><td colspan="6">Mute Output (Off Normal) Buffer</td></tr>
<tr><td>M/S</td><td colspan="4">Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}.
Note: O/C = Open Circuit</td><td>O/C
V_{DD}</td><td>2:1
3:2</td></tr>
<tr><td>F01,F02</td><td colspan="6">Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}.
* Assumes f_{CLK} = 3.579545MHz.
<table>
<tr><th>F01</th><th>F02</th><th>Nominal Impulsing Rate</th><th>Actual* Impulsing Rate</th><th>System Clock frequency</th></tr>
<tr><td>O/C</td><td>O/C</td><td>10Hz</td><td>10.13Hz</td><td>303.9Hz</td></tr>
<tr><td>O/C</td><td>V_{DD}</td><td>20Hz</td><td>19.42Hz</td><td>582.6Hz</td></tr>
<tr><td>V_{DD}</td><td>O/C</td><td>932Hz</td><td>932.17Hz</td><td>27,965.1Hz</td></tr>
<tr><td>V_{DD}</td><td>V_{DD}</td><td>16Hz</td><td>15.54Hz</td><td>466.1Hz</td></tr>
</table></td></tr>
<tr><td>CE</td><td colspan="6">Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.</td></tr>
<tr><td>XTAL IN</td><td colspan="6">Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.</td></tr>
<tr><td>XTAL OUT</td><td colspan="6">Crystal Output Buffer to drive crystal.</td></tr>
<tr><td>V_{SS}</td><td colspan="6">System ground</td></tr>
<tr><td>X_1, X_2, X_3</td><td colspan="6">Column keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>Y_1, Y_2, Y_3, Y_4</td><td colspan="6">Row keyboard Inputs. On-chip pull-up transistors to V_{DD}.
Active LOW.</td></tr>
<tr><td>HOLD</td><td colspan="6">O/C — Normal Operation
V_{DD} — No impulsing. If activated during impulsing, hold occurs when the current digit is complete
Prevents further impulsing. On-chip pull-down transistor to V_{SS}.</td></tr>
</table>

PLESSEY Semiconductors — CMOS

MV4325

PROGRAMMABLE KEYPAD PULSE DIALLER

The MV4325 Keypad Pulse Dialler contains all the logic necessary to interface a 2 of 7 keypad and convert this key information to control and mute pulses simulating a telephone rotary dial. The MV4325 has programmable access pause capability to provide automatic interruption of dialling needed when accessing the toll network, WATS line or public network. The device is fabricated using Plessey Semiconductors' ISO-CMOS technology which enables the device to function down to 2.0V making it ideal for long loop operation.

The MV4325 will accept up to 20 digits and access pauses and will redial stored information at a later time by activation of # key. Device current in standby is less than 1μA at 1.0V.

The MV4325 is available in Ceramic DIL (DG, -40°C to +85°C).

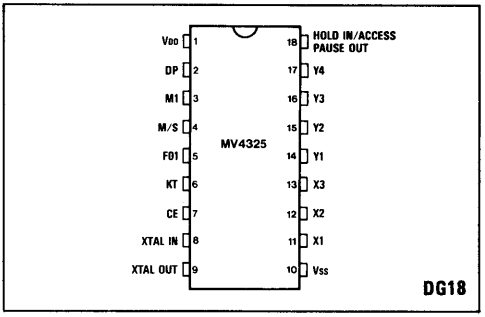


Fig.1 Pin connections (top view)

APPLICATIONS

- Pushbutton Telephones with Last Number Redial
- Repertory Dialers
- Tone to Pulse Converters

FEATURES

- Last Number Redial
- Multiple Access Pause Programming
- Any Valid Keypad Input or HOLD IN Causes Exit from Access Pause
- Oscillator Start Up Controlled from Keypad Input
- Oscillator Power Down whilst not Dialling
- 300 Hz Key Tone indicates Valid Key
- 2.0V to 7.0V Supply Voltage Operating Range
- Stores up to 20 Digits and Access Pauses
- Digit Memory Retained down to 1.0V at 1μA
- Selectable Mark/Space Ratio 66⅔ : 33⅓ or 60 : 40
- 10Hz Dialling Speed (932Hz Fast Test) :)

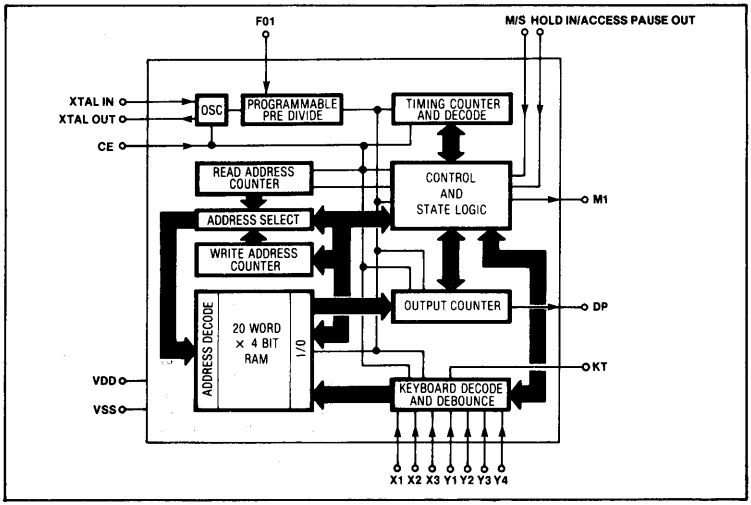


Fig.2 MV4325 function diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN	MAX		MIN	MAX
$V_{DD}-V_{SS}$	-0.3V	10V			
Voltage on any pin	V_{SS}-0.3V	V_{DD} + 0.3V			
Current at any pin		10mA			
Operating Temperature	-40°C	+85°C	Power Dissipation		1000mW
Storage Temperature	-65°C	+ 150°C			

* Derate 16mW/°C above 75°C. All leads soldered to PC board.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, f_{CLK} = 3.579545MHz; V_{DD} = +3.0V
All voltages wrt V_{SS}

		CHARACTERISTIC		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.0		7.0	V		
2		Standby Supply Current		I_{DDS}			1.0	μA	CE = M/S = F01 = HOLD IN = V_{SS}, V_{DD} = 1.0V	
3		Operating Supply Current		I_{DD}		100	150	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-12	μA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S, F01
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	8.0	μA	$V_{IN} = V_{DD}$	
8		Input Low Level Voltage		V_{IL}			0.9	V	All inputs	
9		Input High Level Voltage		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M_1, M_2, KT
13				I_{OL}	0.2	0.5		mA	V_{OUT} = 0.5V	
14			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	
15				I_{OH}	-0.2	-0.5		mA	V_{OUT} = 2.5V	
16	IN/OUTPUT	Input Low Level Voltage		V_{IL}			0.9	V		
17		Input High Level Voltage		V_{IH}	2.1			V		
18		Output Low Level Current		I_{OL}		15		μA	V_{OUT} = 0.5V	CE,
19		Output High Level Current		I_{OH}		-12		μA	V_{OUT} = 2.5V	HOLD IN/ACCESS
20		Input Force High Current (from V_{OL})		I_{FH}		55		μA	V_{IN} = 2.5V	PAUSE OUT
21		Input Force Low Current (from V_{OH})		I_{FL}		-70		μA	V_{IN} = 0.5V	

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = +25°C$; $f_{CLK} = 3.579545\,MHz$; $V_{DD} = +3.0V$

		CHARACTERISTIC	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
1	DYNAMIC	Output Rise Time	t_R		1.0		µs	DP, M_1
2		Output Fall Time	t_F		1.0		µs	C_L = 50pF
3		Maximum Clock Frequency	f_{CLK}	3.58			MHz	3.579545 MHz Crystal
4		Mark to Space Ratio	M/S		2:1			M/S = O/C (V_{SS})
5					3:2			M/S = V_{DD}
6		System Clock Frequency (Internal)			300		Hz	F01 = V_{SS}
7		Impulsing Rate = I/T			10		Hz	F01 = V_{SS}
8		Fast Test Impulsing Rate			14.9		Hz	F01 = V_{DD}
9		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE ↑ '1'
10		Input Capacitance	C_{in}		5.0		pF	Any Input

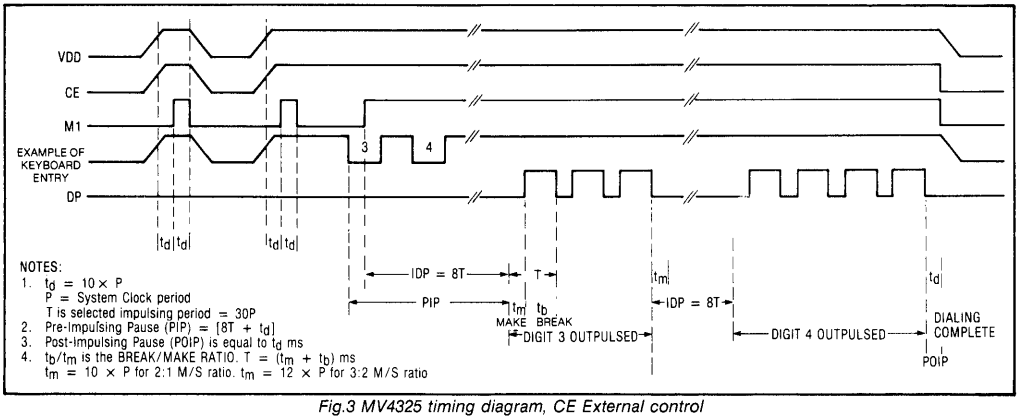


Fig.3 MV4325 timing diagram, CE External control

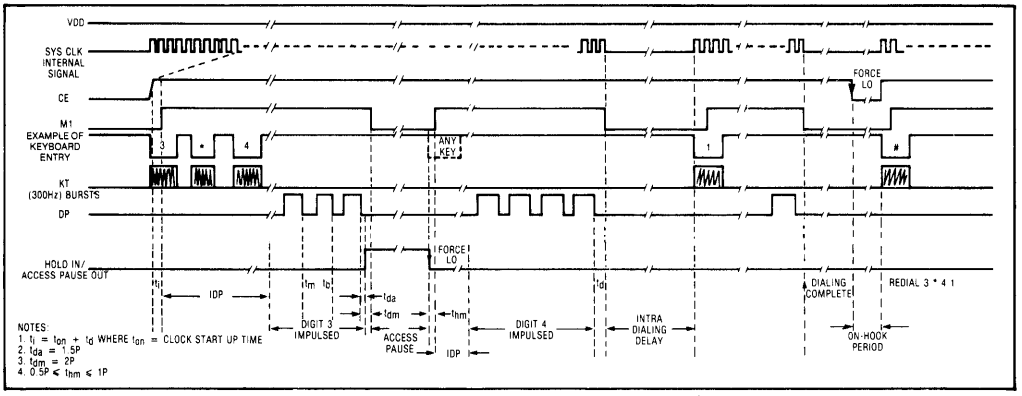


Fig.4 MV4325 timing diagram, CE Internal control

PIN FUNCTIONS

V_{DD}	Positive voltage supply				
DP	Dial Pulsing Output Buffer				
M1	Mute Output Buffer				
M/S	Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}. Note: O/C = Open Circuit			O/C	2:1
				V_{DD}	3:2
F01	Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}. * Assumes f_{CLK} = 3.579545MHz.	F01	Nominal Impulsing Rate	Actual* Inpulsing Rate	System Clock frequency
		O/C	10Hz	10.13Hz	303.9Hz
		V_{DD}	932Hz	932.17Hz	27,965.1Hz
CE	Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.				
XTAL IN	Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.				
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.				
V_{SS}	System ground				
X_1,X_2,X_3	Column keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
Y_1,Y_2,Y_3,Y_4	Row keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
HOLD IN/	INPUT/OUTPUT	O/C	Normal Operation		
ACCESS	INPUT	V_{DD}	No impulsing. If activated during impulsing, hold occurs when the current digit is complete.		
PAUSE OUT	OUTPUT	V_{DD}	Logic "1" level output indicates access pause condition.		
KT	300Hz	Square wave bursts indicate valid keypad input.			

No. of O/P Pulses	Digit	KEYPAD INPUT CODE Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0
ACCESS PAUSE		1	1	1	0	0	1	1

Table 1

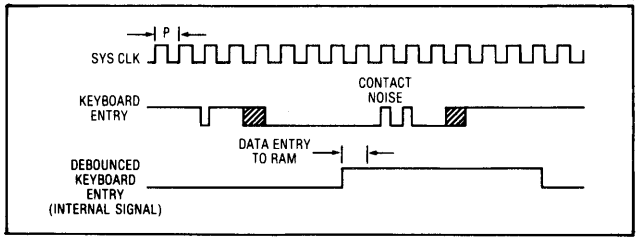


Fig.5 Keypad input debounce timing diagram

OPERATING NOTES

The MV4325 programmable keypad pulse dialer is optimized for use in key operated pulse dialling telephone sets and contains features which make it particularly suitable for applications where redial of last number dialled and repertory dial facilities are required.

Keypad information is accepted directly from a dual contact keypad having two single pole switches per key: one switch common to the column and one switch common to the row. The common row contacts are connected Y1 to Y4 and the common column contacts connected X1 to X3. The other side of each switch is connected to a common VSS line. The keypad code is shown in Table 1.

The MV4325 will accept up to 20 digits and access pauses, e.g. 18 digits plus 2 access pauses or alternately 19 digits plus 1 access pause. Prior to a keypad input being accepted contact bounce is eliminated by a circuit which ensures that any input which is valid for less than 10ms is rejected and any input valid for greater than 17ms is accepted as a valid key input. This circuit operates similarly on the trailing edge of a valid key input preventing multiple digit recognition in the presence of noise. Debounce operation is shown in Fig.5.

The first key entered in any dialling sequence initiates the oscillator on the MV4325 by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in Fig.3 and Fig.4. Fig.3 shows use of the MV4325 with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialer circuit. In this mode the pulse occurring on M1 when CE is taken high with no keypad input can be used to initiate the bistable latching relay.

Fig.4 shows the timing diagram of the MV4325 including access pause and redial mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously and dialling commences after recognition of the leading edge of the first valid key input. When an access pause is reached M1 goes low and Hold In/Access Pause Out goes high indicating the device is in an access pause. This output signal can be used to enable an external dial tone recognition circuit. Exit from the access pause is achieved by one of two methods. One method is by the next valid key operation. If a valid digit is entered, the digit will be entered in the next consecutive storage location in the digit memory. If the key # is activated, redialling of the number in memory will occur only if the device is in the redial mode. The alternative method to exit from an access pause is to pulse Hold In/Access Pause Out low, resetting the output latch associated with this input/output pin.

Fig.4 shows a pause in dialling between the completion of dialling digit 4 and keying digit 1. In this condition, the oscillator powers down to minimize power consumption and interfering signals, whilst CE remains high. On recognition of the next digit, the digit is entered in the next consecutive memory location and dialling resumes.

The end of a key entry sequence is indicated to the MV4325 by externally pulsing or clamping CE low. This causes the on-chip latch holding CE high to reset.

If the first key entered after a CE low period is #, redial of the last number dialled will occur. Access pause operation is as previously described. In the standby condition the MV4325 dissipates less than 1.0μW.

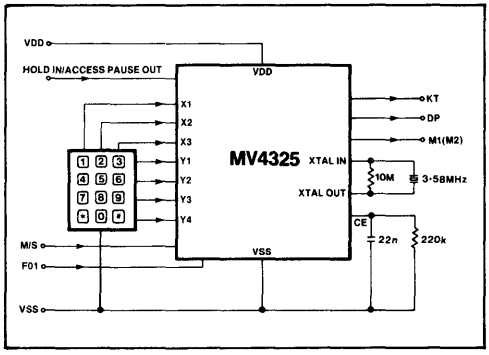


Fig.6 Application diagram

PLESSEY Semiconductors — ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV4330 MV4332

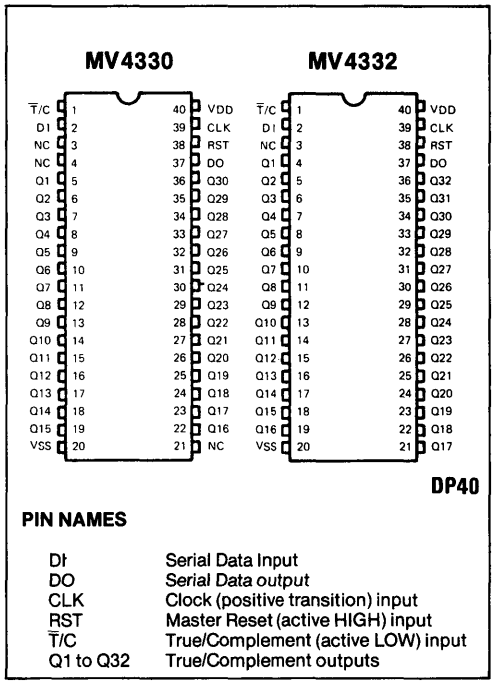
CMOS/LSI 30/32-BIT STATIC SHIFT REGISTERS WITH PARALLEL TRUE/COMPLEMENT OUTPUTS

The MV4330 and MV4332 are CMOS/LSI 30 and 32-bit static shift registers incorporating selectable true/complement outputs for each bit. These devices are well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. One of these devices can drive four 7-segment displays or two 14-segment alpha-numeric displays plus decimal points or two 16-segment alpha-numeric displays directly.

The devices are available in 40-pin plastic DIL (DP) package.

FEATURES

- Direct LCD Drive
- CMOS Low Power (1 μA)
- 3 to 18 Volt Operation
- On-Chip Wave-Shaping
- High Speed (Typ. 3 MHz) Shift Register



PIN NAMES

DI	Serial Data Input
DO	Serial Data output
CLK	Clock (positive transition) input
RST	Master Reset (active HIGH) input
T/C	True/Complement (active LOW) input
Q1 to Q32	True/Complement outputs

Fig.1 Pin connections (top view)

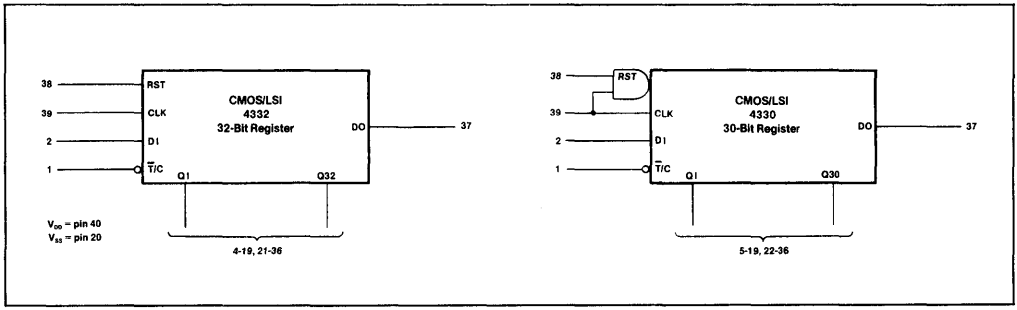


Fig.2 Block diagrams

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	VO Volts	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Quiescent Device Current		I_L			5	–	0.5	50	uA
					10	–	1	100	
Output Voltage	Low-Level	V_{OL}			5	–	0	0.01	V
					10	–	0	0.01	
	High-Level	V_{OH}			5	4.99	5	–	
					10	9.99	10	–	
Noise Immunity (Any Input)		V_{NL}		0.8	5	1.5	2.25	–	V
				1.0	10	3	4.5	–	
		V_{NH}		4.2	5	1.5	2.25	–	
				9.0	10	3	4.5	–	
Output Drive Current	D OUT	I_{DN}	N-Channel	0.5	5	0.8	1.7	–	mA
				0.5	10	1.0	3.0	–	
		I_{DP}	P-Channel	4.5	5	−0.35	−0.9	–	
				9.5	10	−0.8	−1.9	–	
	Q OUT	I_{DN}	N-Channel	0.5	10	50	250	–	uA
		I_{DP}	P-Channel	9.5	10	−50	−250	–	
Input Current		I_I				–	10	–	pA

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $C_L = 50pF$
All input rise and fall times = 20ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Propagation Delay Time	tPHL tPLH		10	–	300	–	ns
Transition Time	tTHL	D OUT (CL=50pF)	10	–	70	130	ns
	tTLH	Q OUT (CL=15pF)	10	–	300	–	ns
Maximum Clock Frequency	fCL		10	1.0	3.0	–	MHz
Minimum Clock Pulse Width	tWL tWH		10	–	200	–	ns
Minimum Reset Pulse Width	tWH(R)		10	–	200	–	ns
Input Capacitance	CI	Any Input		–	5	–	pF

Note 1.Voltages with respect to V_{SS}
Note 2.Typical temperature coefficient for all values = 0.3%/°C

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	LIMIT	UNIT
DC Supply Voltage	VDD	-0.5 to 18	V
Input Voltage	VIN	-0.5 to VDD+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Ts	-65 to 125	°C

OPERATING NOTES

The MV4330 and MV4332 accept a serial input DI which is shifted into the register on the positive transition of the clock (CLK) input. A feature of these devices is that the clock input and the true/complement control (T/C) input have wave-shaping circuits (Fig.3) to ensure fast edges on-chip regardless of the shape of the incoming signals.

The MV4330 also has the reset (RST) input gated with the clock input for synchronous reset on the positive transition of the clock. The MV4332 has asynchronous reset (RST) inputs which are active HIGH.

The parallel outputs of the shift registers are available in either true or complementary form dependent on the state of the true/complement control input. When input is logic-level LOW, the true form is available at all parallel outputs and when the input goes HIGH, the parallel outputs immediately revert to the complementary form of the data stored in each register. This action is independent of the clock input condition. A serial data (DO) output is provided for applications using longer shift registers, etc. This output is the true form of the last stage of the register.

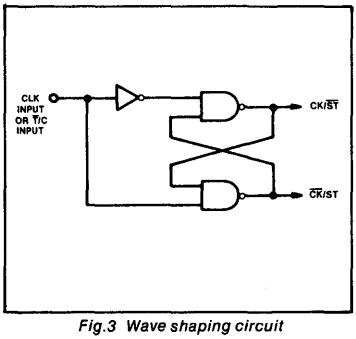


Fig.3 Wave shaping circuit

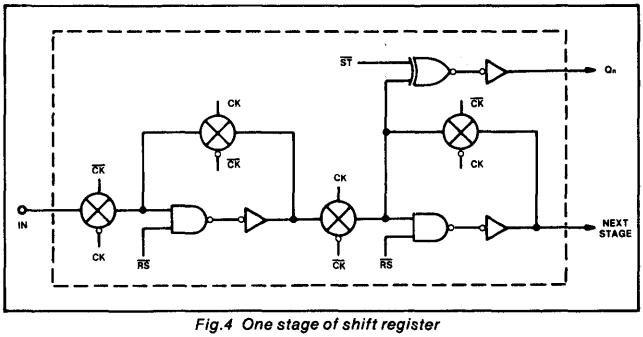


Fig.4 One stage of shift register

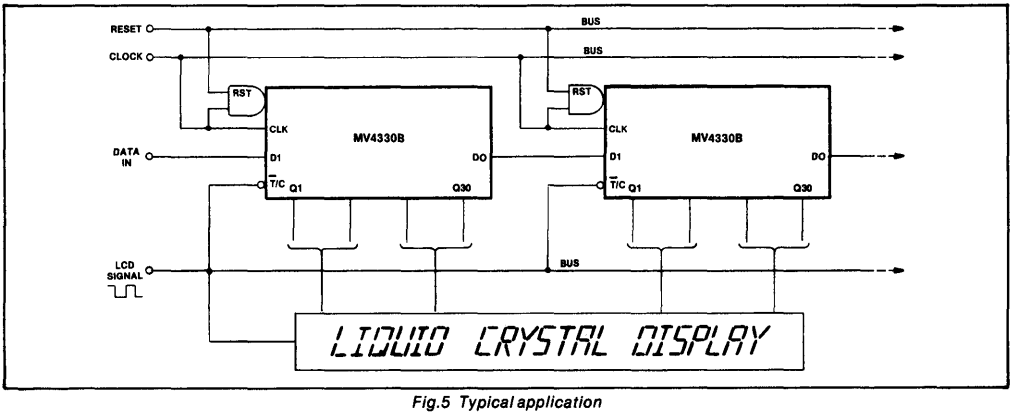


Fig.5 Typical application

PLESSEY Semiconductors — CMOS

MV5087

DTMF GENERATOR

The MV5087 is fabricated using Plessey Semiconductors' ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with either a standard 2-of-8, or single contact (form A), keyboard. The keyboard entries determine the correct division of the reference frequency by the row and column counters.

D-to-A conversion, using R-2R ladder networks, results in a staircase approximation of a sinewave with low total distortion.

Frequency and amplitude stability over operating voltage and temperature range are maintained within industry DTMF specifications.

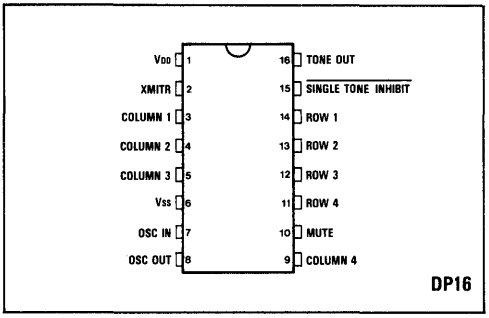


Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5087
- Low Standby Power
- Minimum External Parts Count
- 3.5V to 10V Operation
- 2-of-8 Keyboard or Calculator-Type Single Contact (Form A) Keyboard Input
- On-Chip Regulation of Output Tone
- Mute and Transmitter Drivers On-Chip
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point-of-Sale and Banking Terminals
- Process Control

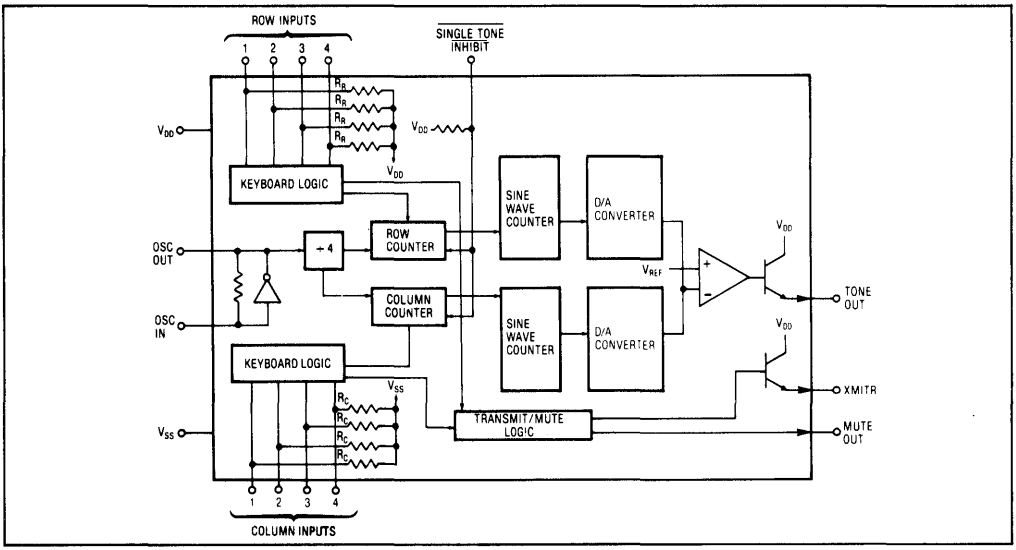


Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX		MIN.	MAX.
V_{DD}-V_{SS}	−0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} − 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	−40°C	+85°C			
Storage temperature	−65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3.5V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	3.5		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3.5V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3.5V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	SINGLE TONE INHIBIT	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
		INPUT RESISTANCE	R_{IN}		60		KΩ		
	ROW 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.9V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.3V_{DD}	V		
	COLUMN 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.1V_{DD}	V		
OUTPUTS	XMITR	SOURCE CURRENT	I_{OH}	-15	−25		mA	V_{DD} = 3.5V, V_{OH} = 2.5V	No Keyboard Entry
				-50	−100		mA	V_{DD} = 10V, V_{OH} = 8V	
		LEAKAGE CURRENT	I_{OZ}		0.1	10	uA	V_{DD} = 10V, V_{OH} = OV	Keyboard Entry
	MUTE	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3.5V, V_{OL} = 0.5V	No Keyboard Entry
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		SOURCE CURRENT	I_{OH}	-0.5			mA	V_{DD} = 3.5V, V_{OH} = 3.0V	Keyboard Entry
				-1.0			mA	V_{DD} = 10V, V_{OH} = 9.5V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3.5V to 10V

CHARACTERISTICS			SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	ROW TONE OUTPUT VOLTAGE		V_{OR}	320	400	500	mV_{RMS}	Single Tone R_L = 1KΩ
	COLUMN TONE OUTPUT VOLTAGE		V_{OC}	400	500	630	mV_{RMS}	
	EXTERNAL LOAD IMPEDANCE		R_L	700			Ω	V_{DD} = 3.5V
				330			Ω	V_{DD} = 10V
OUTPUT DISTORTION						−20	dB	Total out-of-band power relative to sum of row and column fundamental power
PRE EMPHASIS, High Band				1		3	dB	
Tone Output Rise Time			t_r		3	5	ms	

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	XMITR	Emitter output of a bipolar transistor whose collector is connected to V_{DD}. With no keyboard input this output remains at V_{DD} and a keyboard input changes the output to a high impedance state. The state of Single Tone Inhibit input has no effect on XMITR output.
3,4,5,9	Column 1-4	These inputs are held at V_{SS} by resistors Rc and sense a valid logic level (approx $1/2\ V_{DD}$) when tied to a Row input.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC In, OSC Out	On-chip inverter completes the oscillator when a 3,579545 MHz crystal is connected to these pins. OSC In is the invertor input and OSC Out is the output.
10	Mute	This CMOS Output switches to V_{SS} with no keyboard input and to V_{DD} with a keyboard input. This output is unaffected by the state of Single Tone Inhibit.
11,12,13,14	Row 1-4	These inputs are held at V_{DD} by resistors R_R and sense a valid logic level (Approx $1/2\ V_{DD}$) when tied to a column input.
15	$\overline{\text{Single Tone Inhibit}}$	This input has a pull-up resistor to V_{DD} and when left unconnected or tied to V_{DD}, single or dual tones may be generated. When V_{SS} is applied dual tones only are generated and no input combinations will cause generation of a single tone.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes, and regulates the output level of, the row and column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard, single contact (form A) keyboard and electronic input. Figures 3 and 4 show these input configurations, and Fig. 5 shows the internal structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed. Single tones are generated when more than one button is pushed in any row or column. No tones are generated when diagonally-positioned buttons are simultaneously pressed.

An electronic input to a single column generates that single column tone. Inputs to multiple columns generates no tone. An electronic input to a single row generates no tone and a single row tone may be generated only by activating 2 columns and the desired row.

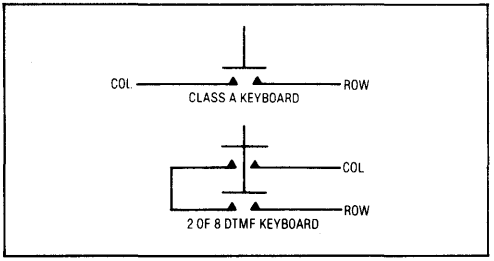


Fig.3 Keyboard configuration

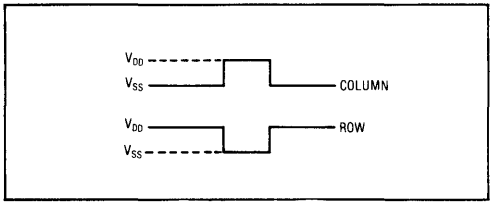


Fig.4 Electronic input

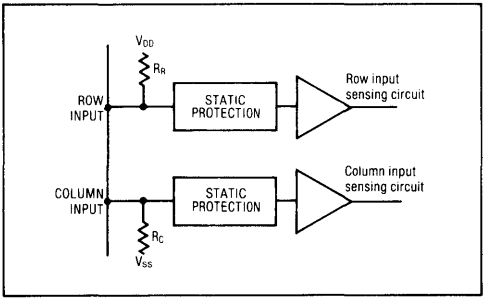


Fig.5 Row and column inputs

OUTPUT FREQUENCY

Table 1 shows the output frequency deviation from the standard DTMF frequencies when a 3.58MHz crystal is used as the reference.

The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6), resulting in a 'staircase' approximation to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	-0.32	
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

Table 1 Output frequency deviation

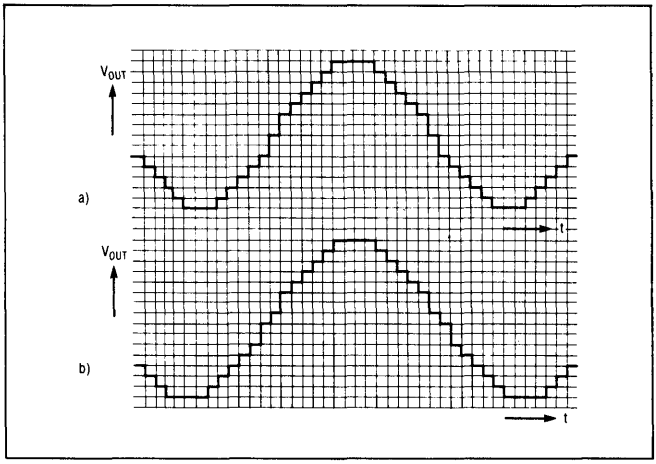


Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \text{----} V_{nf}^2}}{V_{fundamental}}\right)\%$$

Where V_{2f} -- V_{nf} are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \text{--} V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \text{---} V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
$V_{2R} - V_{nR}$ are the Fourier component amplitudes of the row frequencies
$V_{2C} - V_{nC}$ are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

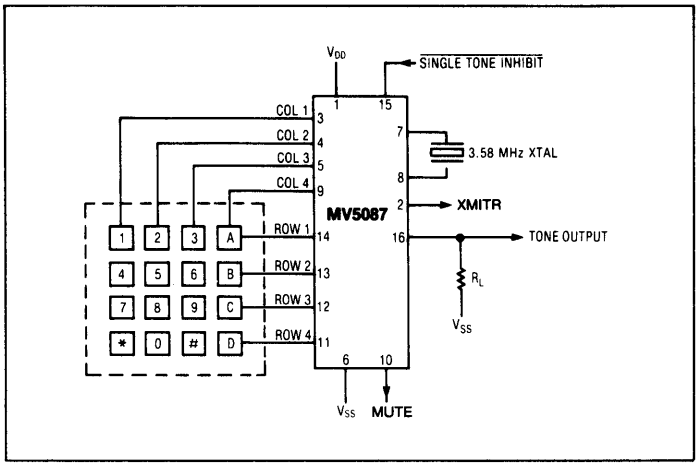


Fig.7 Connection diagram

PLESSEY
Semiconductors

CMOS

MV5089

DTMF GENERATOR

The MV5089 is fabricated using Plessey Semiconductors' ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with a standard 2-of-8 active-low keyboard and the keyboard entries determine the correct division of the reference frequency by the row and column counters. D-to-A conversion, using R-2R ladder networks, results in a 'staircase' approximation of a sinewave with low total distortion.

Frequency stability over operating voltage and temperature range are maintained within industry DTMF standards.

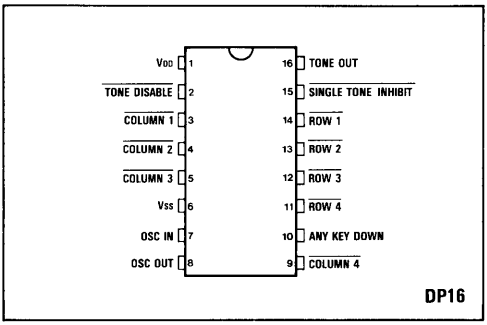


Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5089
- Low Standby Power
- Minimum External Parts Count
- 2.75V to 10V. Operation
- 2-of-8 Keyboard Input
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point of Sale and Banking Terminals
- Process Control

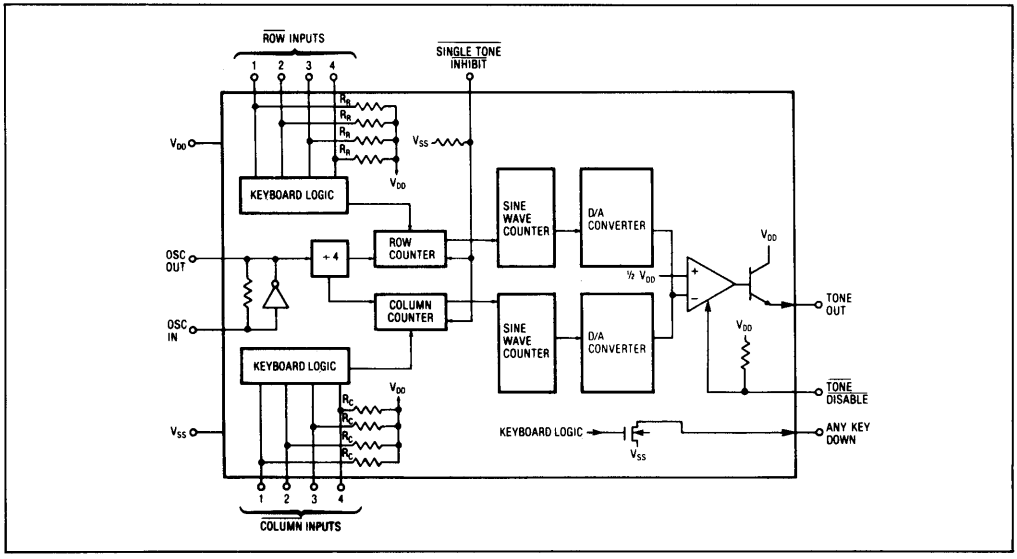


Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX		MIN.	MAX.
V_{DD}-V_{SS}	−0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} − 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	−40°C	+85°C			
Storage temperature	−65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	2.75		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	SINGLE TONE INHIBIT. TONE DISABLE	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
		INPUT RESISTANCE	R_{IN}		60		KΩ		
	ROW 1-4 COLUMN 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
OUTPUTS	ANY KEY DOWN	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3V, V_{OL} = 0.5V	
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		LEAKAGE CURRENT	I_{OZ}		1		uA	V_{DD} = 3V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	OUTPUT LEVEL, ROW	V_{OUT}	-10	−8	-7	dBm	V_{DD} = 3V. Single Tone. R_L = 100KΩ
PRE EMPHASIS, High Band			2.4	2.7	3.0	dB	
OUTPUT DISTORTION (Dual Tone)					−20	dB	Total out-of-band power relative to sum of row and column fundamental power
Tone Output Rise Time		t_r		3	5	ms	Time for waveform to reach 90% of magnitude of either frequency from initial key stroke

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	$\overline{\text{TONE DISABLE}}$	This input has an internal pull-up resistor to V_{DD}. When connected to V_{SS} no tones are generated by any key depression allowing the keyboard to be used for purposes other than DTMF signalling.
3,4,5,9	$\overline{\text{COLUMN 1-4}}$	These CMOS inputs are held at V_{DD} by an internal pull-up resistor and are activated by the application of V_{SS}.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC IN, OSC OUT	On-chip inverter completes the oscillator when a 3,58 MHz Crystal is connected to these pins. OSC IN is the inverter input and OSC OUT is the output.
10	Any Key Down	This is an NMOS transistor output which switches to V_{SS} while any key is depressed. Otherwise this output is high impedance. Switching is independent of Tone Disable and Single Tone Inhibit.
11,12,13,14	$\overline{\text{Row 1-4}}$	As $\overline{\text{Column 1-4}}$ inputs.
15	$\overline{\text{Single Tone Inhibit}}$	This input has a pull-down resistor to V_{SS}. When left unconnected or tied to V_{SS}, dual tones may be generated, but keyboard input combinations resulting in single tone generation are inhibited. When V_{DD} is applied single or dual tones may be generated.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes the Row and Column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard or with an electronic input. Figures 3 and 4 show these input configurations and Fig.5 shows the internal chip structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed.

With Single Tone Inhibit at V_{DD}, connection of V_{SS} to a single column causes the generation of that Column tone. Connection of V_{SS} to more than one Column will result in no Column tones being generated. Connection of V_{SS} to Rows only generates no tone - a Column must be connected to V_{SS}.

A single Row tone only may be generated by connecting 2 columns, and the desired row, to V_{SS}.

OUTPUT TONE LEVEL

The output tone level of the MV5089 is proportional to the applied DC supply voltage.

A regulated supply will normally be used which may be designed to provide stability over the temperature range.

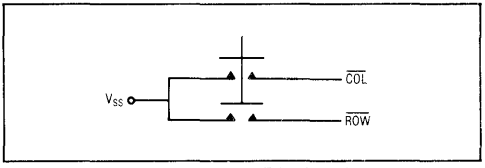


Fig.3 2 of 8 DTMF keyboard

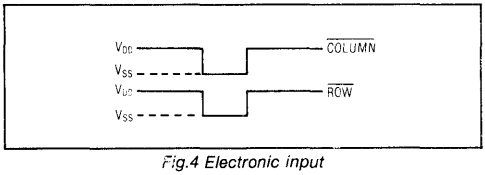


Fig.4 Electronic input

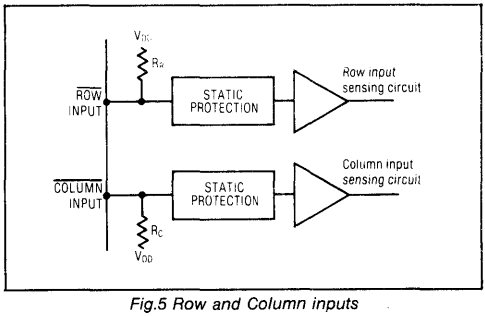


Fig.5 Row and Column inputs

OUTPUT FREQUENCY

Table 1 shows the output frequency deviation from the standard DTMF frequencies when a 3.58MHz crystal is used as the reference.

The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6) resulting in staircase approximations to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	−0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	−0.32	
	f_7	1477	1471.9	−0.35	
	f_8	1633	1645.0	+0.73	

Table 1 Output frequency deviation

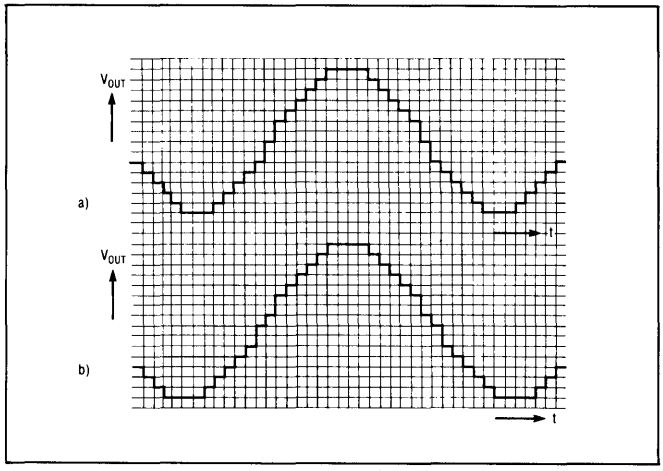


Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \cdots V_{nf}^2}}{V_{fundamental}}\right)\%$$

Where V_{2f} -- V_{nf} are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \cdots V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \cdots V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
V_{2R} -- V_{nR} are the Fourier component amplitudes of the row frequencies
V_{2C} -- V_{nC} are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

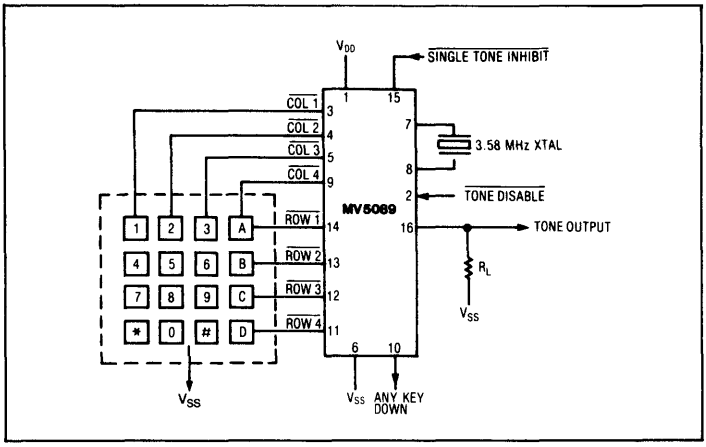


Fig.7 connection diagram

PLESSEY Semiconductors — PRELIMINARY INFORMATION CMOS

MV8804 EXP

8 x 4 BIDIRECTIONAL ANALOGUE SWITCH ARRAY

The MV8804 is a CMOS/LSI 8 x 4 Analogue Switch Array incorporating control memory (32 bits), decoder and digital logic level converters. The circuit has digitally-controlled analogue switches having very low 'ON' resistance and very low 'OFF' leakage current. The switches will operate with analogue signals at frequencies up to 40MHz and up to 13.0V peak-to-peak. A 'HIGH' on the Master Reset input switches all channels 'OFF' and clears the memory. The MV8804 is ideal for crosspoint switching applications.

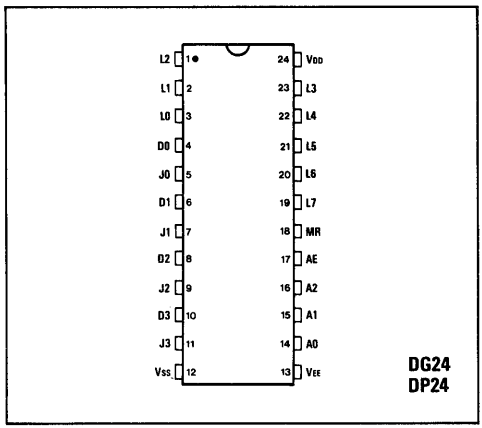


Fig.1 Pin connections - top view

FEATURES

- Microprocessor Compatible Control Inputs
- On-Chip Control Memory And Address Decoding
- Row Addressing
- Master Reset
- 32 Crosspoint Switches in 8 x 4 Array
- 5.0V to 13.0V Operation
- Low Crosstalk Between Switches
- Low On Resistance: 90Ω (typ.) At 10V
- Matched Switch Characteristics
- Switches Frequencies Up To 40MHz

APPLICATIONS

- PABX And Key Systems
- Data Acquisition Systems
- Test Equipment/Instrumentation
- Analogue/Digital Multiplexers

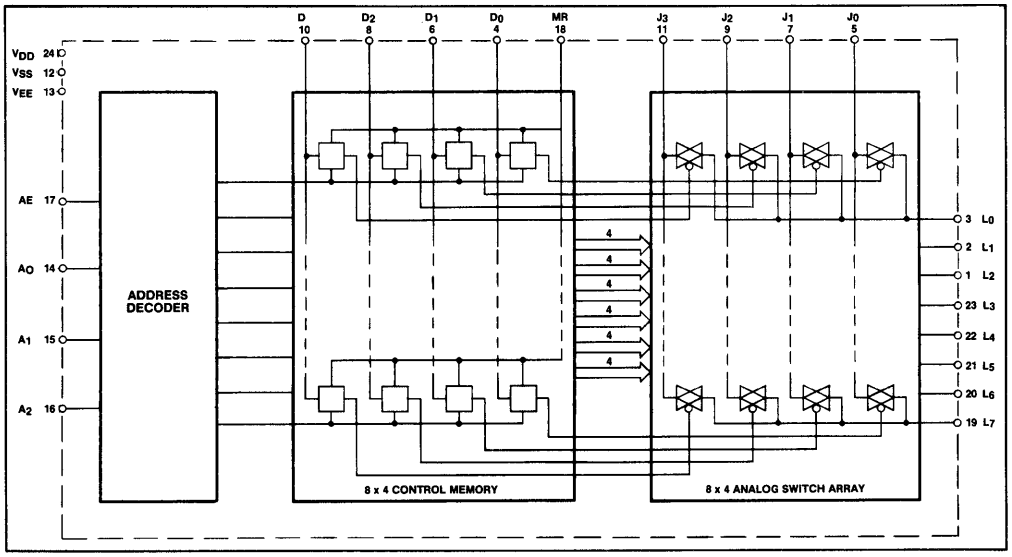


Fig.2 MV8804 functional block diagram

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

	Min.	Max.		Min.	Max.
V_{DD} - V_{SS}	-0.3V	16V	Storage temperature	-65°C	+125°C
V_{DD} - V_{EE}	-0.3V	16V	(DP package)		
V_{SS} - V_{EE}	-0.3V	16V	Power dissipation		1200mW*
Voltage on any logic pin	V_{SS} -0.3V	V_{DD} +0.3V	(DG package)		
Voltage on any line (V_L) or junctor (V_J)	V_{EE} -0.3V	V_{DD} +0.3V	Power dissipation		600mW**
Current at any logic pin		10mA	(DP package)		
Operating temperature (all packages)	-40°C	+85°C			
Storage temperature (DG package)	-65°C	+150°C			

* Derate 16mW/°C above 75°C. All leads soldered to PC board.

** Derate 6.3mW/°C above 25°C. All leads soldered to PC board.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = +25°C, V_{SS} - V_{EE} = 0V, V_{is} = 5V p-p, C_L = 50pF, R_L = 10kΩ, t_r = t_f = 20ns (input signal)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Sine wave response (distortion)			0.1		%	V_{DD} = 13V }
			0.2		%	V_{DD} = 10V } f_{in} = 1kHz
			1.0		%	V_{DD} = 5V }
Frequency response channel 'ON' (sine wave input)			40		MHz	V_C = V_{DD} = 10V, $\frac{V_o}{V_i}$ = -3dB
Feedthrough channel 'OFF'			-40		dB	V_{DD} = 10V, V_C = V_{EE}, R_L = 1kΩ, f_{in} = 1MHz
Crosstalk between any two channels			-40		dB	f_{in} = 1.0MHz } V_{DD} = 10V, Switch A
			-90		dB	f_{in} = 3.4kHz } 'ON',Switch B 'OFF'
Propagation delay Signal input to signal output	t_{PS}		10		ns	V_{DD} = 10V, Switch 'ON'
Turn 'ON' propagation delay	t_{PLH}		200		ns	V_{DD} = 10V
Data input to signal output	t_{PHL}		400		ns	V_{DD} = 5V
Address enable to signal output	t_{PAE}		300		ns	V_{DD} = 10V
			600		ns	V_{DD} = 5V
Minimum address enable (AE)	t_{AE}		90		ns	V_{DD} = 10V
Pulse width			225		ns	V_{DD} = 5V
Minimum set-up time						
Address to AE	t_s	0	50		ns	V_{DD} = 10V
		0	90		ns	V_{DD} = 5V
Data in to AE	t_s		50		ns	V_{DD} = 10V
			90		ns	V_{DD} = 5V
Minimum Hold Time	t_h		50		ns	V_{DD} = 10V
Address or data in to address enable			90		ns	V_{DD} = 5V
Memory reset time	t_{MR}		175		ns	V_{DD} = 10V, R_L = 1kΩ
Memory reset recovery time	T_{MRR}		150		ns	V_{DD} = 10V } R_L = 1kΩ
			250		ns	V_{DD} = 5V }

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{SS} = V_{EE} = 0V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range						
Digital	V_{DD} - V_{SS}	5	5	13	V	
Analogue	V_{DD} - V_{EE}	5	10	13	V	
Logic level converter	V_{SS} - V_{EE}	0	5	12	V	
On state resistance	R_{ON}		75	108	Ω	V_{DD} = 13V }
			90		Ω	V_{DD} = 10V } V_J = V_L = 0.6V
			240		Ω	V_{DD} = 5V }
Difference in On state	R_{ON}		20		Ω	V_{DD} = 13V
Resistance between any switches			30		Ω	V_{DD} = 10V
Off state leakage current (any line to any junctor)	I_{OFF}		±0.01	±500	nA	V_{DD} = 13V, selected crosspoint in Off state
Input logic '0' level	V_{IL}		4.5		V	V_{DD} = 10V } V_{is} = V_{DD} through 1kΩ
			2.25	1.5	V	V_{DD} = 5V }
Input logic '1' level	V_{IH}		5.5		V	V_{DD} = 10V } V_{is} = V_{DD} through 1kΩ
		3.5	2.75		V	V_{DD} = 5V }
Quiescent device current (per package)	I_Q		0.1	500	μA	V_{DD} = 13V
Maximum current through crosspoint switch	I_{MAX}		±8.0		mA	V_{DD} = 13V
Switch input capacitance	C_{is}		5		pF	V_{DD} = 10V, V_{in} = 0V
Switch output capacitance	C_{os}		20		pF	V_{DD} = 10V, V_{in} = 0V
Feedthrough capacitance	C_{ios}		0.2		pF	V_{DD} = 10V, V_{in} = 0V
Digital input capacitance	C_{in}		5		pF	V_{DD} = 10V, V_{in} = 0V

NOTES
1. Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing.
2. Vis is the analogue switch input voltage, Vin is digital input voltage.

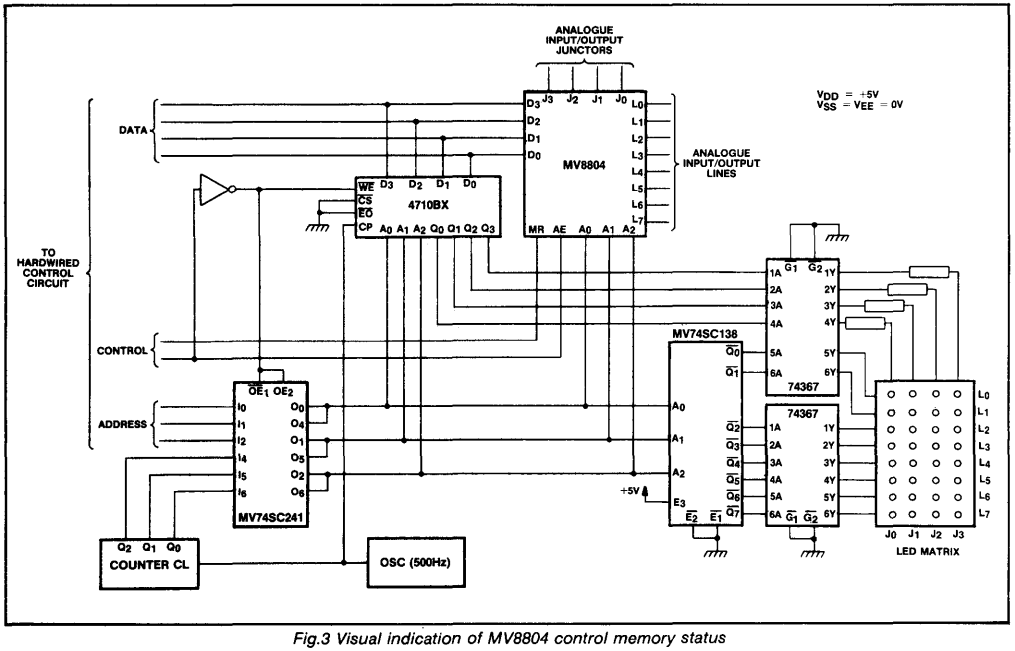


Fig.3 Visual indication of MV8804 control memory status

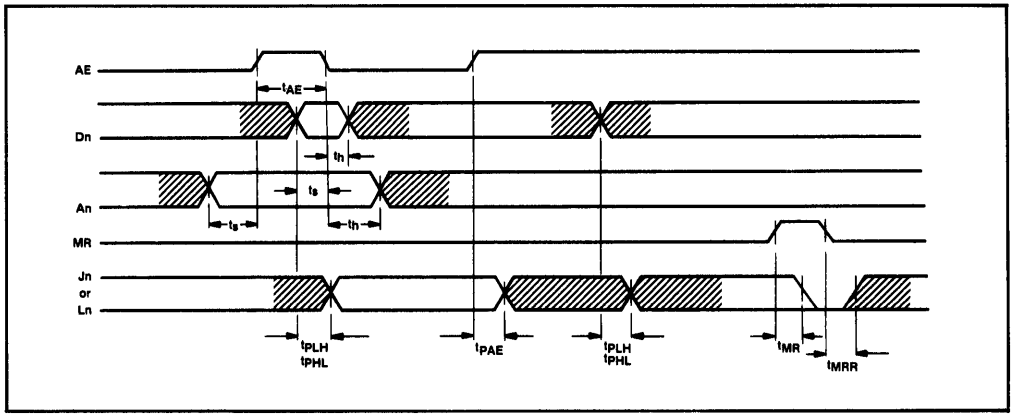


Fig.4 Timing waveforms

PIN DESCRIPTION

Pin	Name	Description
1	L_2	Analogue Switch Array Input/Output Line
2	L_1	Analogue Switch Array Input/Output Line
3	L_0	Analogue Switch Array Input/Output Line
4	D_0	Control Memory Data Line Input
5	J_0	Analogue Switch Array Input/Output Junctor
6	D_1	Control Memory Data Line Input
7	J_1	Analogue Switch Array Input/Output Junctor
8	D_2	Control Memory Data Line Input
9	J_2	Analogue Switch Array Input/Output Junctor
10	D_3	Control Memory Data Line Input
11	J_3	Analogue Switch Input/Output Junctor
12	V_{SS}	Negative Digital Power Supply
13	V_{EE}	Negative Analogue Power Supply
14	A_0	Control Memory Address Input
15	A_1	Control Memory Address Input
16	A_2	Control Memory Address Input
17	AE	Control Memory Address Enable Input (Strobe)
18	MR	Master Reset
19	L_7	Analogue Switch Array Input/Output Line
20	L_6	Analogue Switch Array Input/Output Line
21	L_5	Analogue Switch Array Input/Output Line
22	L_4	Analogue Switch Array Input/Output Line
23	L_3	Analogue Switch Array Input/Output Line
24	V_{DD}	Positive Analogue/Digital Power Supply

FUNCTIONAL DESCRIPTION

The analogue switch array is arranged in 8 rows and 4 columns. The row input/outputs are referred to as LINES (L0-L7) and the column input/outputs as JUNCTORS (J0-J3). The crosspoint analogue switches interconnect the lines and junctors when turned 'ON' and provide a high degree of isolation when turned 'OFF'. Interchannel crosstalk is minimal despite the high density of the analogue switch array.

The control memory of the MV8804 can be treated as an 8-word by 4-bit random access memory. The 8 words are selected by the ADDRESS (A0-A2) inputs through the on-chip address decoder. Data is presented to the memory via the 4 DATA inputs (D0-D3). This data is asynchronously written into the control memory whenever the ADDRESS ENABLE (AE) input is high. A high level written into a memory cell turns the corresponding crosspoint switch 'ON' while a low level causes the crosspoint to turn 'OFF'.

Only the crosspoint switches corresponding to the addressed memory word are affected when data is written into the memory. The remaining switches retain their previous states. By establishing appropriate patterns in the control memory, any combination of lines and junctors may be interconnected. A high level on the MASTER RESET (MR) input returns all memory locations to a low level and turns all crosspoint switches 'OFF', effectively isolating the lines from the junctors. The digital logic level converters allow the digital input levels to differ from limits of the analogue levels switched through the array. For example, with V_{DD} = 5V, V_{SS} = 0V and V_{EE} = -6V, the control inputs can be driven by a 5V system while the analogue voltages through the crosspoint switches can swing from +5V to -6V.

8 x 8 ANALOGUE/DIGITAL SWITCH

Two MV8804s configured as shown in Fig.7, implement an 8 x 8 analogue/digital switch. The switch capacity can be expanded to an M x N array of inputs/outputs. Expansion in the N dimension is as shown and connecting the lines (L0-L7) from the MV8804s in common.

LOGIC TRUTH TABLE

Memory reset	Address enable	Address			Addressed line	Input data to control memory				Junctors connected to addressed line			
	AE	A_2	A_1	A_0		D_3	D_2	D_1	0	J_3	J_2	J_1	J_0
H	X	X	X	X	All	X	X	X	X	All switches 'Off'			
L	L	X	X	X	None	X	X	X	X	No change of state			
L	H	L	L	L	L0	L	L	L	L	•	•	•	•
L	H	L	L	L	L0	L	L	L	H	•	•	•	+
L	H	L	L	L	L0	L	L	H	L	•	•	+	•
L	H	L	L	L	L0	L	L	H	H	•	•	+	+
L	H	L	L	L	L0	L	H	L	L	•	+	•	•
L	H	L	L	L	L0	L	H	L	H	•	+	•	+
L	H	L	L	L	L0	L	H	H	L	•	+	+	•
L	H	L	L	L	L0	L	H	H	H	•	+	+	+
L	H	L	L	L	L0	H	L	L	L	+	•	•	•
L	H	L	L	L	L0	H	L	L	H	+	•	•	+
L	H	L	L	L	L0	H	L	H	L	+	•	+	•
L	H	L	L	L	L0	H	L	H	H	+	•	+	+
L	H	L	L	L	L0	H	H	L	L	+	+	•	•
L	H	L	L	L	L0	H	H	L	H	+	+	•	+
L	H	L	L	L	L0	H	H	H	L	+	+	+	•
L	H	L	L	L	L0	H	H	H	H	+	+	+	+
L	H	L	L	H	L1	Each addressed line may have 16 different combinations of junctors connected to it by inputing data to the control memory as shown for LO.							
L	H	L	H	L	L2								
L	H	L	H	H	L3								
L	H	H	L	L	L4								
L	H	H	L	H	L5								
L	H	H	H	L	L6								
L	H	H	H	H	L7								

NOTES
L = Low Logic Level
H = High Logic Level
X = Don't Care Condition
+ = Indicates Connection Between Junctor and Addressed Line
• = Indicates No Connection Between Junctor and Addressed Line

Expansion in the N dimension is accomplished by replicating the circuit shown and connecting the MV8804 junctors (J0-J3) in common. The address and data control inputs of the MV8804s can be connected in common for any size and switch provided that the address enable (AE) inputs are driven individually, for example by an MV74SC601 programmable AND gate.

A particular signal path is connected by setting up the appropriate signals or the address and data lines and taking the corresponding address enable input high. The master reset (MR), when taken high, disconnects all signal paths.

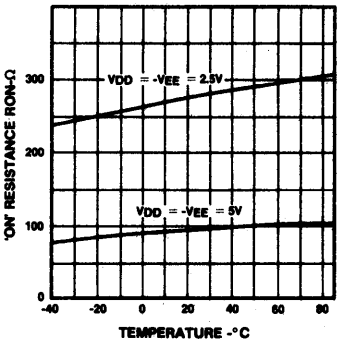


Fig.5 ON resistance vs temperature
Expanding MV8804s (input signal voltage = supply voltage/2)

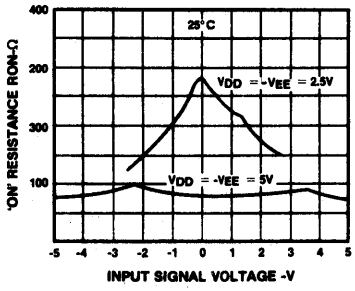


Fig.6 ON resistance vs input signal voltage

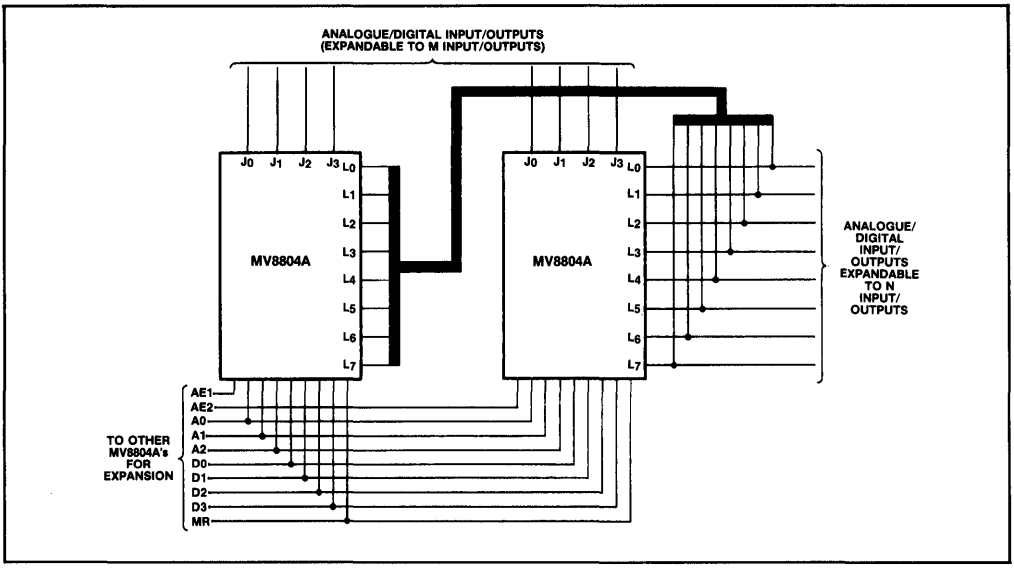


Fig.7 Expanding MV8804s

PLESSEY Semiconductors — CMOS

MV8860

DTMF DECODER

The MV8860 detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF filter (MV8865) and provides a 3-state buffered 4-bit binary output. The clock signals are derived from an on-chip oscillator requiring only a single resistor and low cost crystal as external components. The MV8860 is implemented in CMOS technology and incorporates an on-chip regulator, providing low power operation and power supply flexibility.

The MV8860 is available in Plastic DIL (DP) and Ceramic DIL (DG), both with an operating temperature range of −40°C to +85°C.

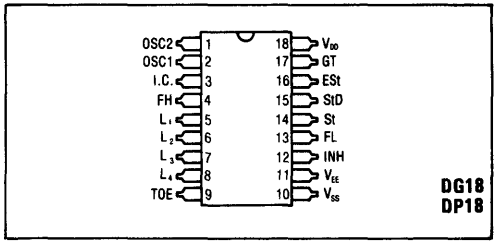


Fig.1 Pin connections (top view)

FEATURES

- 18 Pin DIL Package
- Central Office Quality Detection
- Excellent Voice Talk-Off
- Detect Times down to 20 ms
- Single Supply 5V, or 8 to 13 V Operation
- Latched 3-State Buffered Outputs
- Detects All 16 DTMF Combinations
- Uses Inexpensive 3.58 MHz Crystal
- Low Power CMOS Circuitry
- Adjustable Acquisition and Release Times
- Equivalent to MT8860X

APPLICATIONS

In DTMF Receivers For:

- End-to-end Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

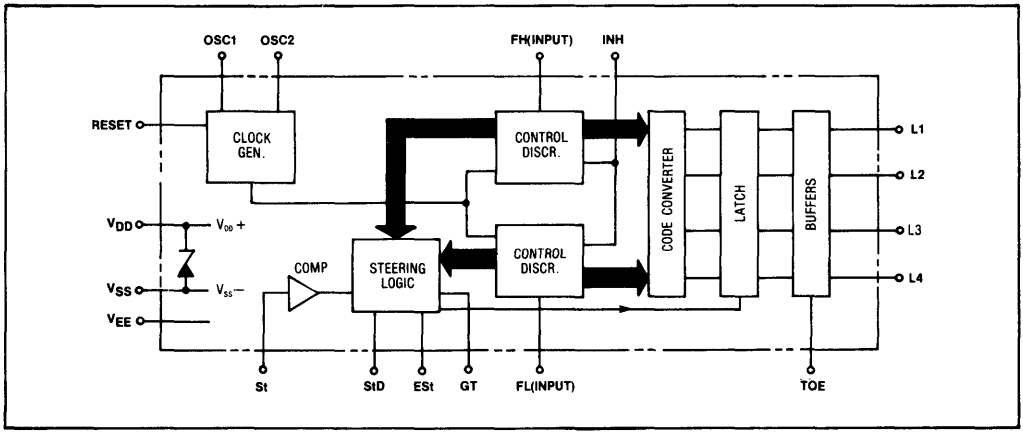


Fig.2 MV8860 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; f_c = 3.579545MHz
5 V operation: V_{DD} - V_{EE} = 5V, V_{SS} = V_{EE}, connections as Fig.5a
12 V operation: V_{DD} - V_{EE} = 12V, R_{SSEE} = 900Ω, connections as Fig.5b
Outputs not loaded
For input current parameters only, V_{IH} = V_{IHO} = V_{DD}, V_{IL} = V_{EE}, V_{ILO} = V_{SS}
All voltages referenced to V_{EE} unless otherwise noted.

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})		V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2					8		13	V	Connections Fig. 5b
3		Internal Logic Ground Voltage (V_{DD} - V_{SS})		V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4					6.0	6.5	7.5	V	Connections Fig. 5b
5		Operating Supply Current		I_{DD}		1.3	4	mA	5V
6						2.5	5	mA	12V V_{DD} - V_{SS} = 5.5V
7		Internal Logic Ground Pin Current		I_{SS}		5.5	6.7	mA	12V R_{SSEE} = 900Ω
8		Operating Power Consumption		P_O		6.5		mW	5V
9						66		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)		V_{IH}	3.5	4		V	5V
11					8.5	9		V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)		V_{IL}		1	1.5	V	5V
13						3	3.5	V	12V
14		High Level Input Voltage OSC1		V_{IHO}	3.5	4.5		V	5V
15					10.5	11		V	12V
16		Low Level Input Voltage OSC1		V_{ILO}		0.5	1.5	V	5V Ref V_{SS}
17						0.5	1.5	V	12V Ref V_{SS}
18		Steering Input Threshold Voltage		V_{TSt}	2.04	2.27	2.5	V	5V
19					5.4	6.0	6.6	V	12V
20		Pull Down Sink Current (INH)		I_{IHI}	10	25	75	μA	5V
21					10	190	400	μA	12V
22		Pull Up Source Current (TOE)		I_{ILT}	2	7	45	μA	5V
23					10	55	250	μA	12V
24		Input High Leakage Current		I_{IH}		0.1	1.5	μA	5V or 12V
25		Input Low Leakage Current		I_{IL}		0.1	1.5	μA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)		V_{OH}	4.9			V	5V
27					11.9			V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)		V_{OL}			0.1	V	5V
29							0.1	V	12V
30		High Level Output Voltage OSC2		V_{OHO}	4.9			V	5V
31					11.9			V	12V
32		Low Level Output Voltage OSC2		V_{OLO}			0.1	V	5V Ref V_{SS}
33							0.1	V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V V_{OH} = 4.5V
35					0.5	0.8		mA	12V V_{OH} = 11.5V
36			N Channel Sink	I_{OL}	0.8	1.2		mA	5V V_{OL} = 0.5V
37					1.0	1.6		mA	12V V_{OL} = 0.5V
38		Output Drive Current OSC2	P Channel Source	I_{OHO}	90	120		μA	5V V_{OH} = 4.5V
39					90	120		μA	12V V_{OH} = 11.5V
40			N Channel Sink	I_{OLO}	100	160		μA	5V V_{OL} = 0.5V
41					100	160		μA	12V V_{SS} = 0.5V
42		Tristate Output Current (High Impedance State)	L_1 - L_4 = H	I_{OZ}		0.035	1.5	μA	5V Appl V_{OL} = 0V
43			L_1 - L_4 = L			0.1	1.5	μA	5V Appl V_{OH} = 5V
44			L_1 - L_4 = H			0.1	1.5	μA	12V Appl V_{OL} = 0V
45			L_1 - L_4 = L			0.3	1.5	μA	12V Appl V_{OH} = 12V

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; V_{DD} = +5V; f_c = 3.579545MHz

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions
1	DETECTOR	Tone Frequency Deviation Accept		Δf_A			±2.5	% Nom.	
2		Tone Frequency Deviation Reject		Δf_R	±3.5			% Nom.	
3		Tone Present Detection Time		t_{DP}	6		10	ms	
4		Tone Absent Detection Time		t_{DA}	0.6	4	10	ms	
5		Guard Time (Adjustable)		$t_{GT(P\ or\ E)}$		20		ms	See Fig. 3
6		Time to Receive = (t_{DP} + t_{GTP})		t_{REC}	28	30	35	ms	Fig. 7a R = 300k Ω
7		Invalid Tone Duration (f_n of $t_{\overline{REC}}$)		$t_{\overline{REC}}$			20	ms	C = 0.1μF
8		Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}	30			ms	
9		Acceptable Drop Out (f_n of t_{ID})		t_{DO}			20	ms	
10	I/P	FL FH Input Transition Time		t_T			1.0	us	10% - 90% V_{DD}
11		Capacitance Any Input		C		5	7.5	pF	
12	OUTPUTS	Propogation Delay St to L_1 - L_4		t_{PL}		8	11	μs	V_{DD} 5V
13						8	11	μs	V_{DD} 12V
14		Propogation Delay St to StD		t_{PStD}		12	14	μs	V_{DD} 5V
15						12	14	μs	V_{DD} 12V
16		Propogation Delay TOE to L_1 - L_4	Enable	t_{PTE}		300		ns	V_{DD} 5V
17						200		ns	V_{DD} 12V
18			Disable	t_{PTD}		300		ns	V_{DD} 5V
19						200		ns	V_{DD} 12V
20	CLOCK	Crystal/Clock Frequency		f_c	3.5759	3.5795	3.5831	MHz	OSC 1 / OSC 2
21		Clock Input (OSC 1)	Rise Time	t_{LHCI}			110	ns	10% - 90% / Externally
22			Fall Time	t_{HLCI}			110	ns	V_{DD} = V_{SS} / Applied
23			Duty Cycle	DC_{CI}	40	50	60	%	/ Clock
24		Clock Output (OSC 2)	Capacitive Load	C_{LOC}			30	pF	With Clock Drive to OSC 1
25				C_{LOX}				nF	Sinusoidal Output With Crystal

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max	
V_{DD} - V_{EE}			16	V
V_{DD} - V_{SS} (Low Impedance Supply)			5.5	V
Voltage on any pin except OSC1 OSC2		V_{EE} −0.3	V_{DD} +0.3	V
Voltage OSC1 OSC2		V_{SS} −0.3	V_{DD} +0.3	V
Max current at any pin (except V_{DD} & V_{EE})			10	mA
Operating Temperature	DP/DG Package	−40	+85	°C
Storage Temperature	DG Package	−55	+175	°C
	DP Package	−55	+125	°C

		Max
Power Dissipation	DG Package*	1000mW
	DP Package**	450mW

* Derate 16mW/°C above 75°C
** Derate 6.3mW/°C above 25°C
All leads soldered to PC board.

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
DR	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
D	*	H	H	L	H	H
	#	H	H	H	L	L
	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

(a) Output coding

Detected Character	INH	ESt
None	Ø	L
X	L	H
DR	H	H
D	H	L

(b) Inhibit function

ESt	St	GT	StD*
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

(c) Steering

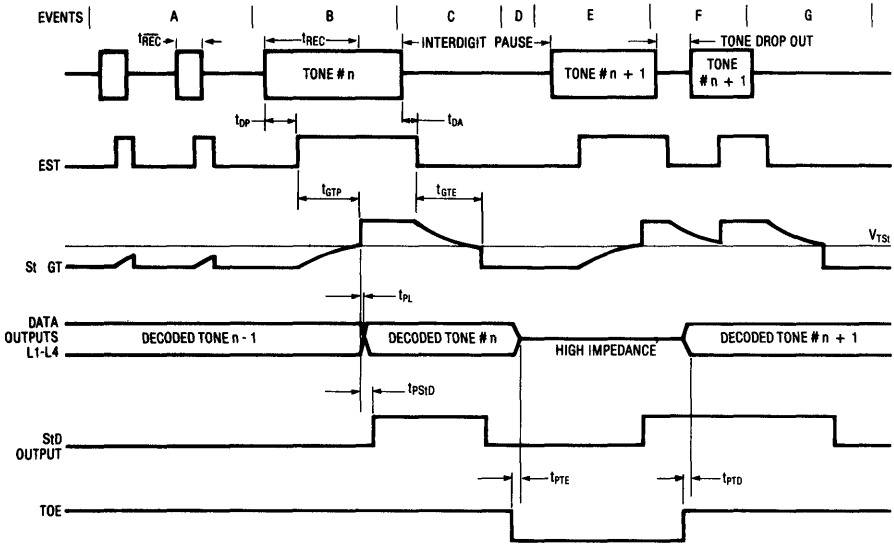
* DELAYED WRT St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH L = LOGIC LOW
Ø = "DON'T CARE" LOGIC HIGH OR LOW
Z = HIGH IMPEDANCE X = ANY CHARACTER

Table 1 Coding data



A) SHORT TONE BURSTS : DETECTED, TONE DURATION IS INVALID
B) TONE # n IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STAGE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n + 1 IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE # n + 1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n + 1 IS DETECTED AND VALIDATED.

Fig.3 Timing diagram

PIN FUNCTIONS

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5MΩ resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only (reset) Note 1	
4	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter	
5	L1	Data Outputs. 3 state buffered Provides 4 Bit binary word corresponding to the tone pair decoded, when enabled by TOE See Table 1 for state table	
6	L2		
7	L3		
8	L4		
9	TOE	3 state output enable input. Logic high on this input enables outputs L1-L4. Internal pull up	
10	V_{SS}	Internal logic ground. For V_{DD} - V_{EE} = 5V V_{SS} connected to V_{EE}. For V_{DD} - V_{EE} > 8V, V_{SS} connected via resistor to V_{EE} see Fig. 5	
11	V_{EE}	Negative power supply. External logic ground	
12	INH	Inhibit input. Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull down	
13	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter	
14	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage< V_{TSt} on this pin frees the device to accept a new tone pair. See Table 1c and Functional Description	
15	StD	Delayed Steering Output. Flags when a valid tone pair has been received. Presents logic high when output latch updated. When St voltage exceeds V_{TSt}. Returns to logic low when St voltage falls below V_{TSt}	
16	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low	
17	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Table 1c)	
18	V_{DD}	Positive power supply	

Note 1: Must be left open circuit.

OPERATING NOTES

The MV8860 is a CMOS Digital DTMF detector and decoder. Used in conjunction with a suitable DTMF filter (MV8865) it can detect and decode all 16 Standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MV8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sinewave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The high group and low group rectangular waves are applied to the MV8860s FH and FL inputs, respectively. The MV8865 DTMF filter provides these functions.

Within the MV8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Fig.2) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both high group and low group signals have been simultaneously detected, a flag ESt (Logic High), is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig.3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of 'tone absent' before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig.7a) is charged via resistor R from ESt which a DTMF tone pair is detected. After a period t_{GTP}, V_C exceeds the St input threshold voltage V_{TSt}, setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Table 1c) and timing diagram (Fig.3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L_1 to L_4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig.7a) falling below V_{TSt}.

Increasing the 'time to receive' (t_{REC}) tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig.7.

When L_1 to L_4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MV8860 may be operated from either a 5V or 8 to 13V supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig.5.

When using the MV8860 with the MV8865 DTMF filter it is only necessary to use the MV8865 crystal oscillator (see Fig.6). When using the higher supply voltage range the MV8865 OSC2 output should be capacitively coupled to the MV8860 OSC1 input as shown in Fig.6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

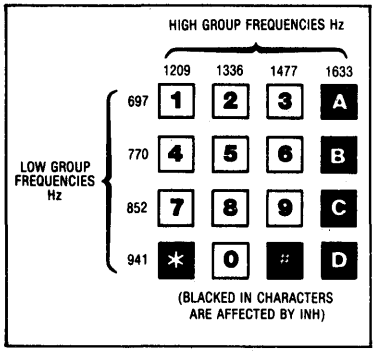


Fig.4 DTMF matrix, indicating character-tone pair correspondence

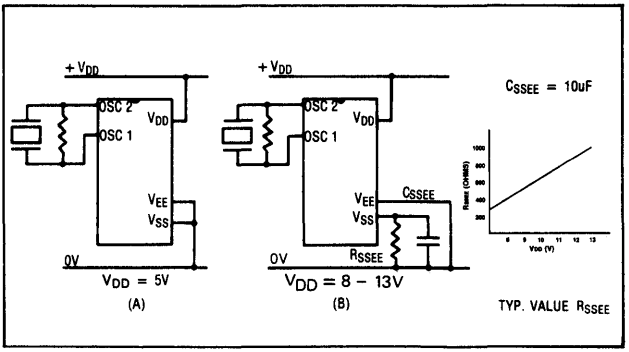
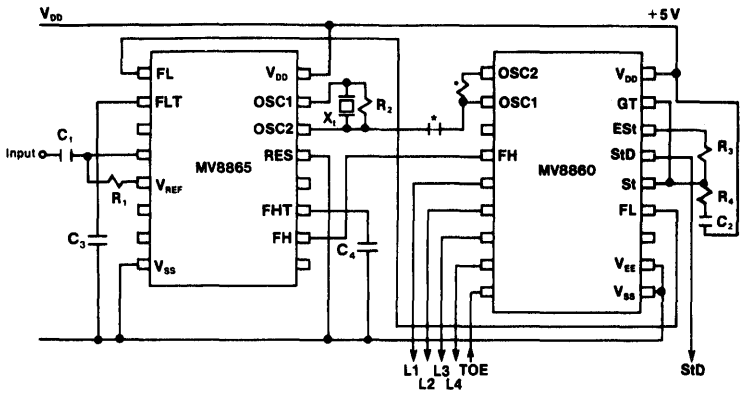


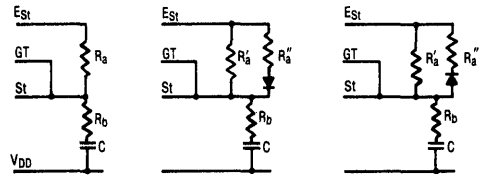
Fig.5 Power supply connection options



TYPICAL PERFORMANCE

DYNAMIC RANGE	30dB
TWIST	± 10dB
ACC. S/N RATIO	14dB
T_{REC}	30ms

Fig.6 Single-ended input receiver using the MV8865 (5 V operation)



$T_{GTP} = T_{GTE}$ (A)

$T_{GTP} < T_{GTE}$ (B)

$T_{GTP} > T_{GTE}$ (C)

$$T_{GTP} = C\,(R_a + R_b)\,\mathrm{Log_n}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{DD} - V_{TSt}}\right)$$

$$T_{GTE} = C\,(R_a + R_b)\,\mathrm{Log_n}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{TSt}}\right)$$

FOR V_{OHESt}, V_{OLESt} Symetric About $V_{TSt} = \frac{1}{2} V_{DD}$

WITH $R_b < 0.1\ R_a$ $\qquad R_b \geq V_{DD} - V_{EE}$ KΩ

$$R_b < 0.1\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$$

A) $T_{GTP} = T_{GTE} \triangleq 0.69\ R_a\ C\left(1 - \frac{R_b}{2\,R_a}\right)$

B) T_{GTP} } $\triangleq 0.69\ C\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$

C) T_{GTE} }

B) T_{GTE} }

C) T_{GTP} } $\triangleq 0.69\ R_a'\ C$

Fig.7 Guard time adjustment

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CMOS

MV8865

DTMF FILTER

The MV8865 contains both the high group and low group filtering and comparator functions required to implement a Dual Tone Multi Frequency tone receiver using a DTMF Digital Detector (i.e. MV8860/62/63). Switched capacitor techniques are used to implement the filters and the device is fabricated using Plessey Semiconductors' high density ISO/CMOS technology. The filter clocks are derived from an on-chip oscillator requiring only a low cost TV crystal as an external component. The MV8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

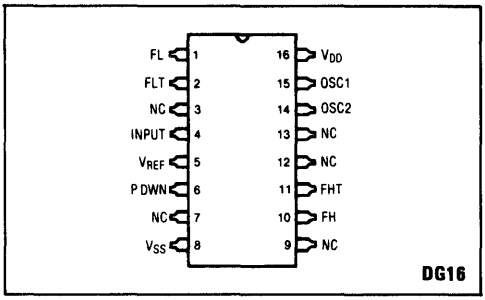

Fig.1 Pin connections (top view)

FEATURES

- Provides DTMF High and Low Group Filtering
- Hard Limiting on Filter Outputs
- 6 Pole Band Pass High and Low Group Filters
- 38 dB Intergroup Attenuation
- Dial Tone Suppression
- +5 to +12 V Single Supply Operation
- Logical Power Down
- Uses Inexpensive 3.58 MHz Crystal
- Wide Dynamic Range 30 dB
- Equivalent to MT8865X

APPLICATIONS

In DTMF Receivers for:

- End to End Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

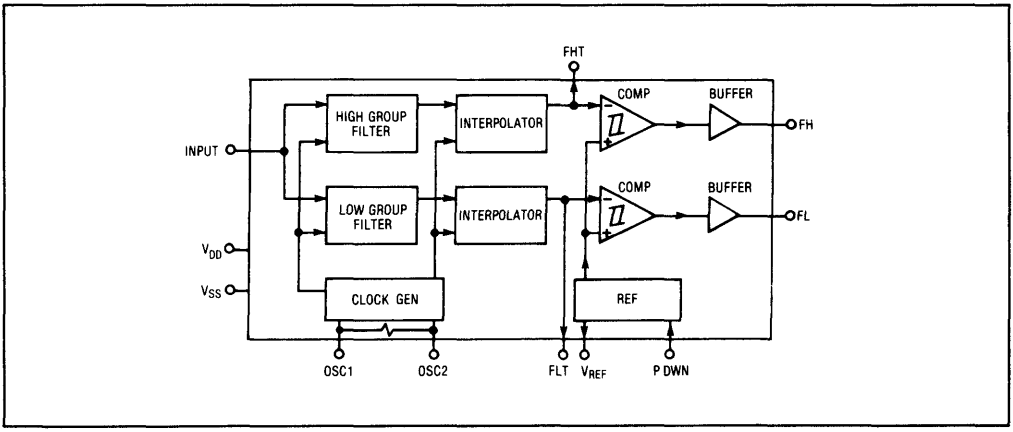

Fig.2 MV8865X functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; f_{CLK} = 3.579545 MHz
All voltages wrt V_{SS}

		Characteristic			Symbol	V_{DD} = 5V			V_{DD} = 12V			Unit	Test Conditions
						Min	Typ	Max	Min	Typ	Max		
1	SUPPLY	Operating Supply Voltage			V_{DD}	4.75					13	V	
2	SUPPLY	Operating Supply Current			I_{DD}		1.2	2.5		5	7.5	mA	PDWN = V_{SS}
3	SUPPLY	Standby Supply Current			I_{DDS}		100	150			400	µA	PDWN = V_{DD}
4	SUPPLY	Operating Power Consumption			P_O		6			60		mW	PDWN = V_{SS} Fig. 6(c)
5	SUPPLY	Standby Power Consumption			P_S		0.5			1.5		mW	PDWN = V_{DD} C = 15pF
6	INPUTS	Low Level Input Voltage		PDWN & OSC 1	V_{IL}			1.5			3.5	V	
7	INPUTS	High Level Input Voltage		PDWN & OSC 1	V_{IH}	3.5			8.5			V	
8	INPUTS	Pull Down Sink Current		PDWN	I_{IH}		3	6		12	24	µA	
9	INPUTS	Input Current		OSC 1	I_I		±2.5			±6		µA	
10	OUTPUTS	Low Level Output Voltage		FL, FH	V_{OL}			0.1			0.1	V	No load
11	OUTPUTS	High Level Output Voltage		OSC 2	V_{OH}	4.9			11.9			V	
12	OUTPUTS	Output Drive Current	N Channel Sink	FL, FH	I_{OL}	0.2			0.5			mA	V_{OL} = 0.4V (5V)
13	OUTPUTS			OSC 2		0.1			0.25			mA	V_{OL} = 1.2V (12V)
14	OUTPUTS		P Channel Source	FL, FH	I_{OH}	0.2			0.5			mA	V_{OH} = 4.6V (5V)
15	OUTPUTS			OSC 2		0.1			0.25			mA	V_{OH} = 10.8V (12V)

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max		Parameter		Max
V_{DD} - V_{SS}			15	V	Power Dissipation	DG package[1]	850mW
Voltage on any pin		V_{SS} − 0.3	V_{DD} + 0.3	V			
Max. current at any pin			10	mA	[1]Derate 16mW/°C above 75°C		
Operating Temperature		40°C	+85	°C			
Storage Temperature	DG package	−65°C	+150	°C			

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
t_{amb} = +25°C; f_c = 3.579545 MHz; V_{DD} = 4.75 V to 13 V

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions	
1		Dynamic Range			30		36	dB		
2		Valid Input Signal Levels					$V_{DD}/2$	V_{pp}		
3		(Each tone of composite signal)			27.9		883	mVrms	V_{DD} = 5V	
4					67.5		2120	mVrms	V_{DD} = 12V	
5		Input Impedance		Z_I	10			MΩ		
6		Low Group Sensitivity (1)			-28.85			dBm	V_{DD} = 5V	
7		Low Group Sensitivity (1)			-21.25			dBm	V_{DD} = 12V	
8	F	High Group Sensitivity (1)			-28.85			dBm	V_{DD} = 5V	
9	L	High Group Sensitivity (1)			-21.25			dBm	V_{DD} = 12V	
10	T	Intergroup	Low Group with	IR_{L1209}	34	45		dB	1209Hz	w.r.t.
11	E		High Tone	IR_{L1477}	36	40		dB	1477Hz	770Hz
12	R	Rejection	High Group with	IR_{H941}	38	45		dB	941Hz	w.r.t.
13			Low Tone	IR_{H770}	36	40		dB	770Hz	1336Hz
14		Dial Tone	Low Group	DR_{L440}		60		dB	440Hz	w.r.t
15				DR_{L350}		30		dB	350Hz	770Hz
16		Rejection	High Group	DR_{H440}		60		dB	440Hz	w.r.t.
17				DR_{H350}		50		dB	350Hz	1336Hz
18		FHT FLT Maximum Permissible Load		R_{LFT}	250			KΩ		
19				C_{LFT}			2000	pF		
20	L	Output Rise Time	FL, FH	t_{TLHO}		90	150	ns	10% to	
21	I M	Output Fall Time		t_{THLO}		60	100	ns	90% V_{DD}	
22		Crystal/Clock Freq.	OSC 1, OSC 2	f_c	3.5759	3.5795	3.5831	MHz		
23		Clock	Rise Time	t_{LHCI}			110	ns	10% to	Externally
24	C	Input	Fall Time	t_{HLCI}			110		90% V_{DD}	Applied
25	O	(OSC 1)	Duty Cycle	DC_{CI}	40	50	60	%		Clock
26	C K	Clock Output OSC 2	Capacitive Load	C_{LOC}			30	pF	Unbalanced load, see Operating Notes	
27		Capacitance Any Input		C_i		5	7.5	pF		

NOTES
1. The sensitivity characteristic specifies correct operation of the post-comparator outputs at minimum input signal levels. It is valid for each of the four DTMF tones in each passband.

PIN FUNCTIONS

DIP Pin	Name	Description	
1	FL	Low group limiter output.	
2	FLT	Test output. Monitors low group filter output. Decouple to V_{SS} with 680pF capacitor.	
3	NC	Not connected.	
4	INPUT	Tone signal input (single ended).	
5	V_{REF}	Internal reference, can be used to bias input via 2MΩ resistor.	
6	PDWN	Power down active high. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.	
7	NC	Not connected.	
8	V_{SS}	Negative (0V) power supply.	
9	NC	Not connected.	
10	FH	High group limiter output.	
11	FHT	Test output. Monitors high group filter output. Decouple to V_{SS} with 680pF capacitor.	
12	NC	Not connected.	
13	NC	Not connected.	
14	OSC 2	Clock Output.	3.58MHz crystal connected between these pins completes internal oscillator.
15	OSC 1	Clock Input.	
16	V_{DD}	Positive power supply.	

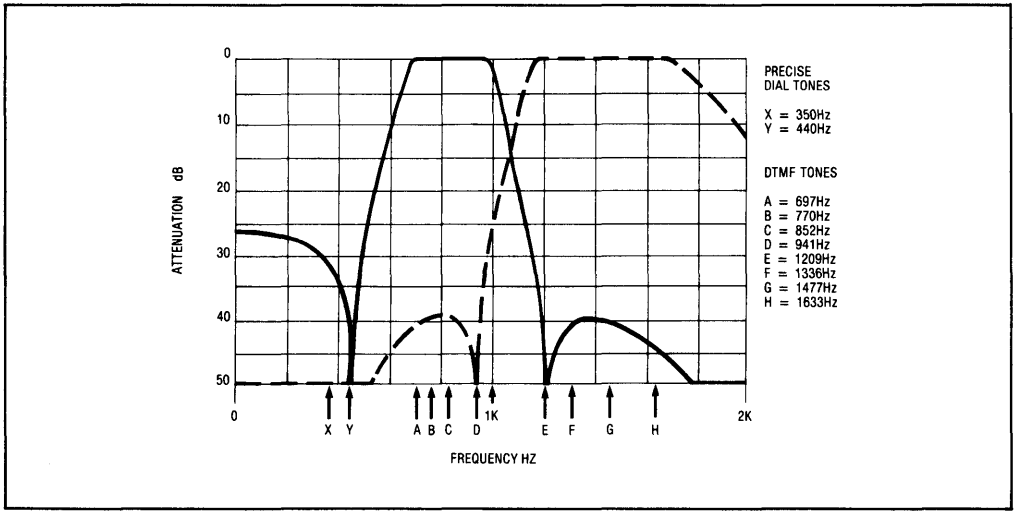

Fig.3 Typical filter characteristics

OPERATING NOTES

The MV8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves, to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of one of Plessey Semiconductors' range of DTMF Digital Decoders (MV8860/62/63), see Fig.4.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig.3) also incorporates a notch at 440 Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting.

The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MV8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig.4) or via a differential buffer to a telephone line (Fig.5). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input capacitively coupled, this is achieved by connecting the signal input to V_{REF} (Pin 5) via a 2 MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680 pF capacitors.

Unbalanced Loads

Presenting a high unbalanced capacitive load to the oscillator crystal can cause attenuation of the oscillator output signal and increased supply current (see Fig.6). Where the MV8865 oscillator is required to drive a high capacitive load such as a number of other MV8865/8860s it is desirable to connect a capacitor between OSC1 and Vss, the value of this capacitor being equal to the capacitive loading at OSC2.

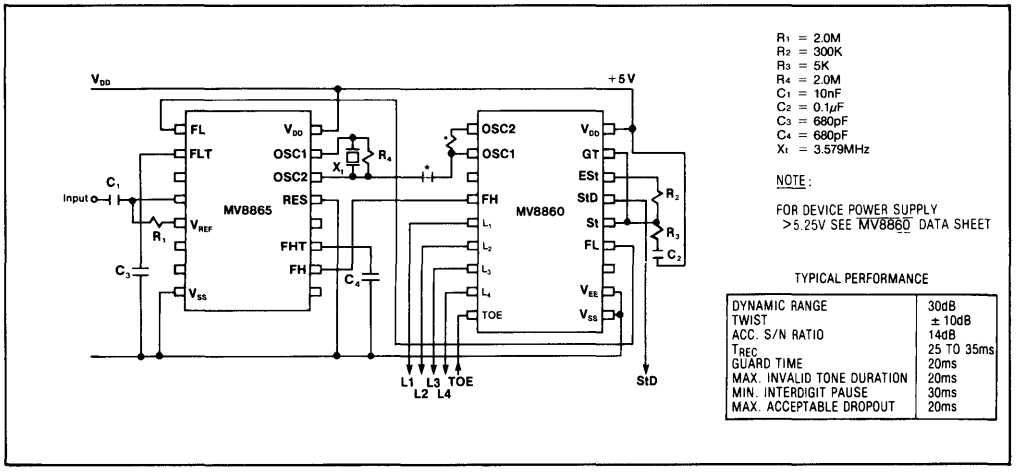

Fig.4 Single-ended input receiver using the MV8860 (5 V operation)

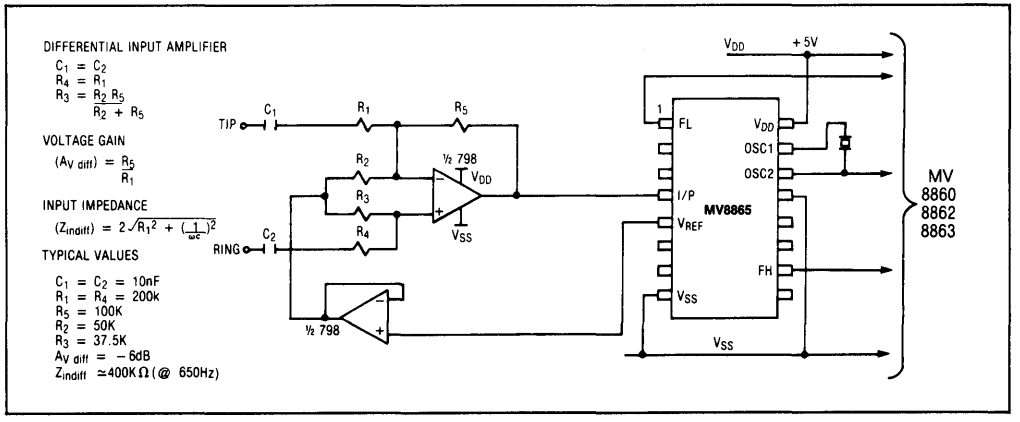

Fig.5 Connection to a telephone line

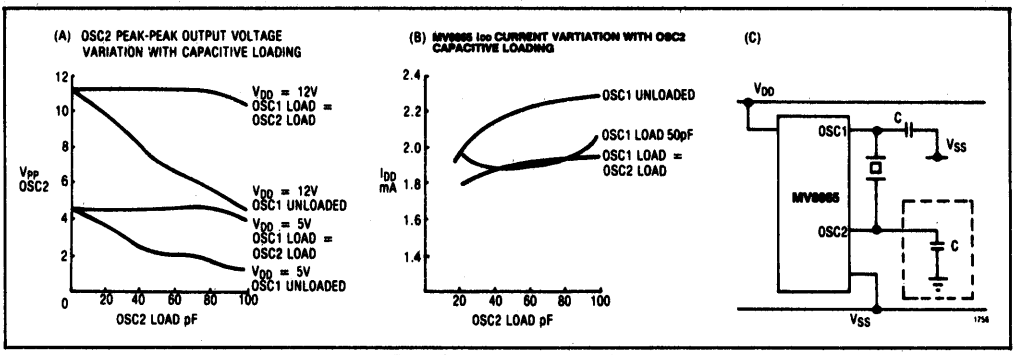

Fig.6 Crystal oscillator loading

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PRELIMINARY INFORMATION

MV8870EXP

DTMF RECEIVER

The MV8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated on Plessey Semiconductors' double-poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high- and low- group filters and dial-tone rejection; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimised by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

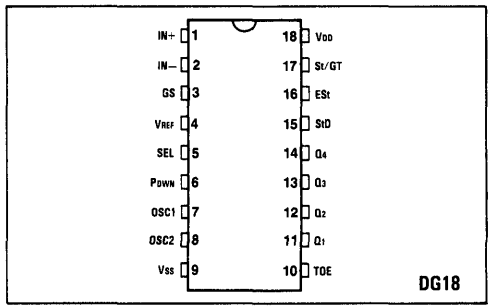


Fig.1 Pin connections (top view)

APPLICATIONS

- PABX
- Central Office
- Key Systems
- Mobile Radio
- Remote Control
- Remote Data Entry

FEATURES

- Full Receiver in Single 18-Pin Package
- Central Office Quality
- Lower Power Consumption
- Adjustable Acquisition and Release Times

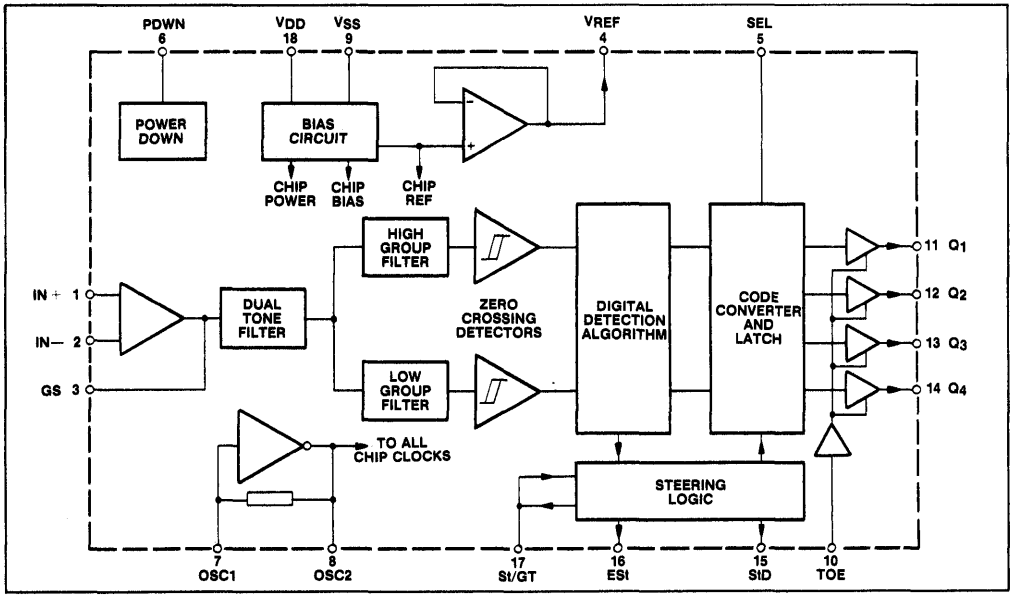


Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Parameter	Min.	Max.	Unit
Power supply voltage V_{DD} - V_{SS}		6	V
Voltage on any pin	V_{SS} -0.3	V_{DD} +0.3	V
Current at any pin		10	mA
Operating temperature	-40	+85	°C
Storage temperature	-65	+150	°C
Package power dissipation (Note 2)		1000	mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Derate above 75°C at 16mW/°C. All leads soldered to board.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25° C

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Operating supply voltage	V_{DD}	4.75		5.25	V	
Operating supply current	I_{DD}		3.0	7	mA	
Power consumption	P_O		15	35	mW	f = 3.579MHz
Low level input voltage	V_{IL}			1.5	V	
High level input voltage	V_{IH}	3.5			V	
Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
Pull up source current	I_{SO}		7.5	15.0	μA	TOE (Pin 10) = 0V
Input impedance (pins 1 & 2)	R_{IN}		10		MΩ	At 1kHz
Steering threshold voltage	V_{TSt}	2.2	2.35	2.5	V	
Low level output voltage	V_{OL}		0.03		V	No load
High level output voltage	V_{OH}		4.97		V	No load
Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4V
Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
Output voltage, pin 4	V_{REF}	2.4		2.7	V	No load
Output resistance, pin 4	R_{OR}		10		kΩ	

OPERATING CHARACTERISTICS, GAIN SETTING AMPLIFIER

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25° C

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input leakage current	I_{IN}		±100		nA	$V_{SS} < V_{IN} < V_{DD}$
Input resistance	R_{IN}		10		MΩ	
Input offset voltage	V_{OS}		±25		mV	
Power supply rejection	PSRR		60		dB	1kHz
Common mode rejection	CMRR		60		dB	V_{IN} = V_{REF} ±1.3V
DC open loop voltage gain	A_{VOL}		65		dB	
Open loop unity gain bandwidth	f_c		1.5		MHz	
Output voltage swing	V_O		4.5		V p-p	$R_L \geqslant$ 100kΩ to V_{SS}
Tolerable capacitive load (GS)	C_L		100		pF	
Tolerable resistive load (GS)	R_L		50		kΩ	
Common mode range	V_{cm}		3.0		V p-p	No load

AC CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25°C, f_{CLK} = 3.579545MHz, using test circuit of Fig.3.

Characteristic		Symbol	Value			Unit	Notes
			Min.	Typ.	Max.		
Valid input signal level (each tone of composite signal)	Min.				-29	dBm	1,2,3,5,6,9
					27.5	mVRMS	1,2,3,5,6,9
	Max.		+1			dBm	1,2,3,5,6,9
			883			mVRMS	
Twist accept limit	Positive			10		dB	2,3,6,9
	Negative			10		dB	2,3,5,9
Freq. deviation accept limit					±1.5% ±2Hz	Nom.	2,3,5,9
Freq. deviation reject limit			±3.5%			Nom.	2,3,5
Third tone tolerance				-16		dB	2,3,4,5,9,10
Noise tolerance				-12		dB	2,3,4,5,7,9,10
Dial tone tolerance				+18		dB	2,3,4,5,8,9,10
Tone present detection time		t_{DP}	5	11	14	ms	Refer to Fig.5
Tone absent detection time		t_{DA}	0.5	4	8.5	ms	
Tone duration accept		t_{REC}			40	ms	(User adjustable) Refer to 'Guard Time Adjustment'
Tone duration reject		t_{REC}	20			ms	
Interdigit pause accept		t_{ID}			40	ms	
Interdigit pause reject		t_{DO}	20			ms	
Propagation delay (St to Q)		t_{PQ}		8	11	µs	TOE = V_{DD}
Propagation delay (St to StD)		t_{PStD}		12		µs	
Output data set up (Q to StD)		t_{QStD}		3.4		µs	
Propagation delay (TOE to Q)	Enable	t_{PTE}		50	60	ns	R_L = 10kΩ
	Disable	t_{PTD}		300		ns	C_L = 50pF
Crystal/clock frequency		f_{CLK}	3.5759	3.5795	3.581	MHz	
Clock output (OSC2)	Capacitive load	C_{LO}			30	pF	

NOTES
1. dBm = decibels above or below a reference power of 1mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40ms. Tone pause = 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2Hz.
7. Bandwidth limited (0 to 3kHz) Gaussian Noise.
8. The precise dial tone frequencies are 350Hz and 440Hz ±2%.
9. For an error rate of better than 1 in 10,000.
10. Reference to lowest level frequency component in DTMF signal.

INPUT CONFIGURATION

The input arrangement of the MV8870 provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback register to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration the input pins are connected as shown in Fig.3 with the op-amp connected for unity gain and V_{REF} biasing the input at 1/2 V_{DD}. Fig.4 shows the differential configuration, which permits the adjustment of gain with the feedback resistor Rs.

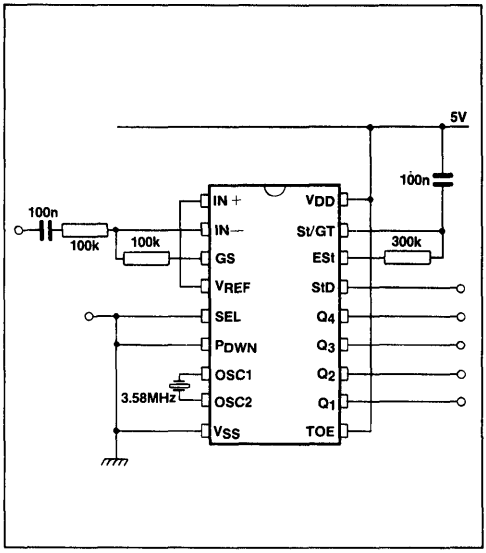


Fig.3 Single ended input configuration

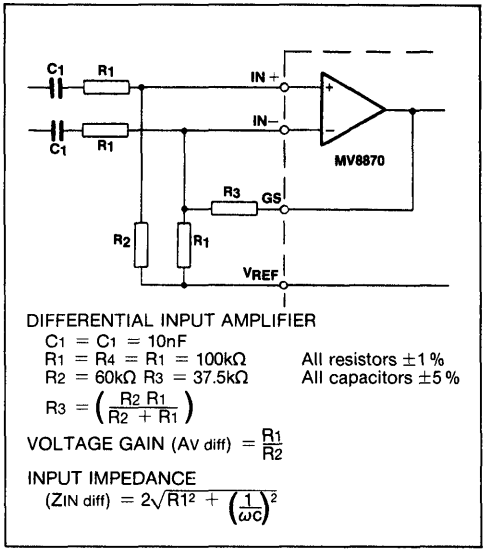
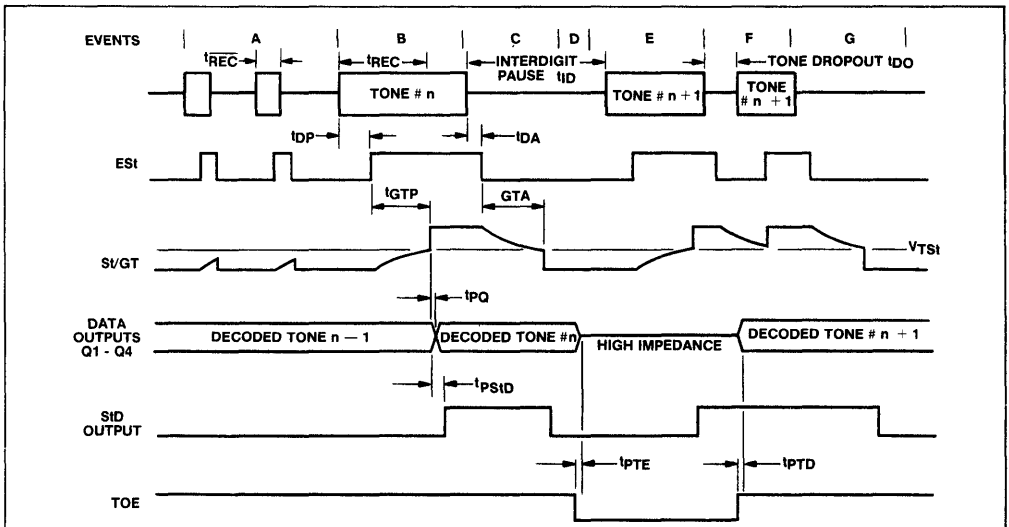


Fig.4 Differential input configuration



A. Short tone bursts detected; tone durations invalid. **B.** Tone #n detected; tone duration valid; decoded to outputs. **C.** End of tone #n detected and validated. **D.** 3-state outputs disabled (high impedance). **E.** Tone (#n + 1) detected; tone duration valid; decoded to outputs. **F.** 3-state outputs enabled; acceptable drop-out of tone (#n + 1) does not register at outputs. **G.** End of tone (#n + 1) detected and validated.

Fig.5 Timing diagram

PIN DESCRIPTIONS

Pin	Name	Description	
1	IN+	Non-inverting input	Connections to the front-end differential amplifier
2	IN−	Inverting input	
3	GS	Gain select. Gives access to output of front-end differential amplifier for connections of feedback resistor.	
4	V_{REF}	Reference voltage output, nominally $V_{DD/2}$. May be used to bias the inputs at mid-rail (see application diagram).	
5	SEL	Logic '1' or '0' selects one of two truth tables (see Table 1).	
6	P_{DWN}	Power down active high, internal pulldown resistor. A high level signal powers down and inhibits the oscillator.	
7	OSC1	Clock input	3.579545MHz crystal connected between these pins completes internal oscillator.
8	OSC2	Clock output	
9	V_{SS}	Negative power supply, normally connected to 0V.	
10	TOE	3-state output enable (input). Logic high enables the outputs Q1 - Q4. Internal pull-up.	
11	Q1	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1).	
12	Q2		
13	Q3		
14	Q4		
15	StD	Delayed steering output presents a logic high when a received tone-pair has been registered and the output high latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.	
16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognisable tone-pair (signal conditions). Any momentary loss of signal condition will cause ESt to return to a logic low.	
17	St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St (see Table 1).	
18	V_{DD}	Positive power supply.	

FUNCTIONAL DESCRIPTION

The MV8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tones of a received pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two sixth-order switched-capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low-group and high-group tones (see Fig.6).

The filter section also incorporates notches at 350Hz and 440Hz for exceptional dial-tone rejection. Each filter output is followed by a single-order switched capacitor section to smooth the signals prior to limiting.

Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The decoder uses digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small frequency deviations and variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to 'talk-off' and tolerance to the presence of interfering signals ('third tones') and noise. When the detector recognises the simultaneous presence of two valid tones (referred to as 'signal condition' in some industry specifications), it raises the 'Early Steering' flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

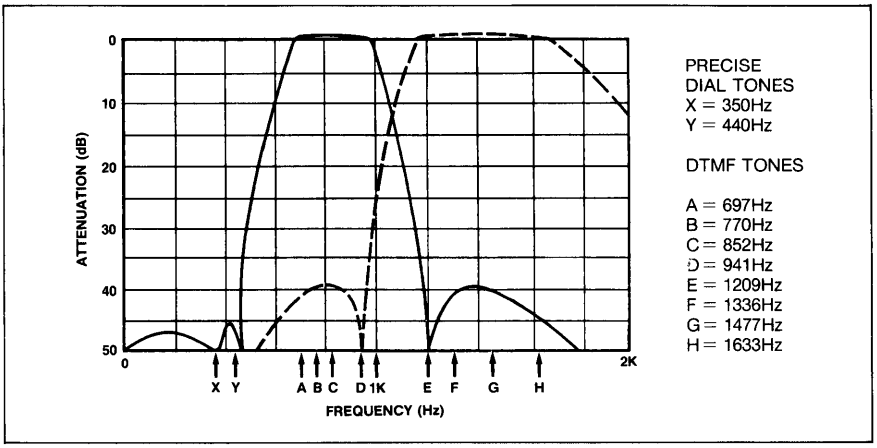


Fig.6 Typical filter characteristic

F_{LOW}	F_{HIGH}	KEY	TOE	SEL	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	L	0	0	0	1
697	1336	2	H	L	0	0	1	0
697	1477	3	H	L	0	0	1	1
770	1209	4	H	L	0	1	0	0
770	1336	5	H	L	0	1	0	1
770	1477	6	H	L	0	1	1	0
852	1209	7	H	L	0	1	1	1
852	1336	8	H	L	1	0	0	0
852	1477	9	H	L	1	0	0	1
941	1336	0	H	L	1	0	1	0
941	1209	*	H	L	1	0	1	1
941	1477	#	H	L	1	1	0	0
697	1633	A	H	L	1	1	0	1
770	1633	B	H	L	1	1	1	0
852	1633	C	H	L	1	1	1	1
941	1633	D	H	L	0	0	0	0
697	1209	1	H	H	0	0	0	1
697	1336	2	H	H	0	0	1	0
697	1477	3	H	H	0	0	1	1
770	1209	4	H	H	0	1	0	0
770	1336	5	H	H	0	1	0	1
770	1477	6	H	H	0	1	1	0
852	1209	7	H	H	0	1	1	1
852	1336	8	H	H	1	0	0	0
852	1477	9	H	H	1	0	0	1
941	1336	0	H	H	0	0	0	0
941	1209	*	H	H	1	0	1	0
941	1477	#	H	H	1	0	1	1
697	1633	A	H	H	1	1	0	0
770	1633	B	H	H	1	1	0	1
852	1633	C	H	H	1	1	1	0
941	1633	D	H	H	1	1	1	1
		ANY	L	ANY	Z	Z	Z	Z

L = Logic low, H = Logic high, Z = High impedance

Table 1 Functional decode table

STEERING CIRCUIT

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as 'character recognition condition'). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Fig.7) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point, the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the 'delayed steering' output flag, StD, goes high, signalling that a received tone pair has been registed. The contents of the output latch are made available on the 4-bit output bus by raising the 3-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions ('drop-out') too short to be considered a valid pulse. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

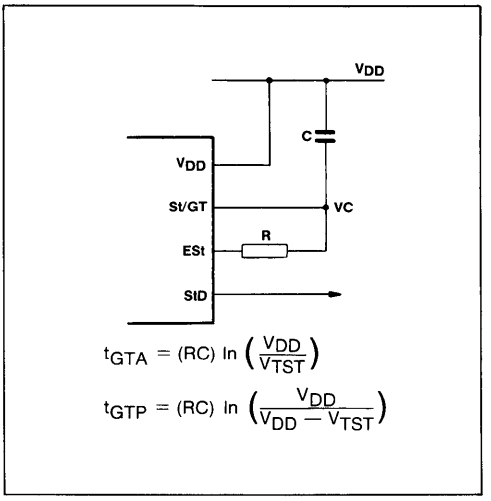


Fig.7 Basic steering circuit

Guard Time Adjustments

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Fig.7 is applicable. Component values are chosen according to the following formulae:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = T_{DA} + t_{GTA}$$

The value of t_{DP} is a parameter of the device (see AC Characteristics) and t_{REC} is the minimum signal duration to be recognised by the receiver. A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40ms would be 300kΩ.

Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specification which place both accept and reject limits on both tone duration and interdigital pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Fig.8.

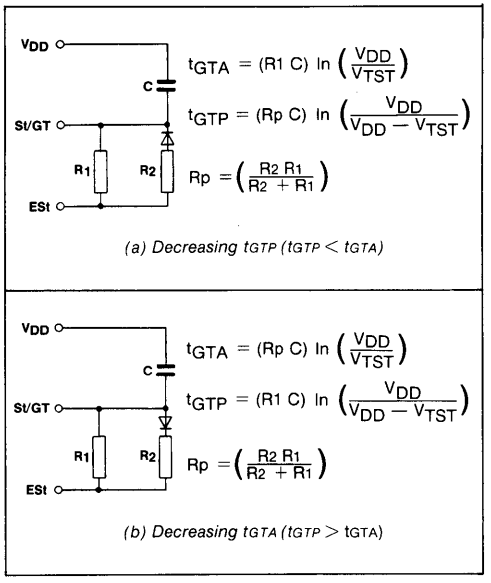


Fig.8 Guard time adjustment

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PRELIMINARY INFORMATION

MV9009 EXP

V21 MODEM TX/RX

The MV9009 is a single chip modulator/demodulator fabricated in silicon gate ISO-CMOS and designed for use in V21 modems. The device can be used alone, or in conjunction with the SL9009 Adaptive Cancellation Filter.

FEATURES

- 300 Baud V21 Operation
- Square or Sinewave Transmit Output Waveforms
- Baseband Shaping to Reduce Out-of-Band Modulation Products
- 2nd Order Digital PLL Receiver
- Lock Detect Output
- Off-Chip Post Detection Filter Enables Optimisation of Received Data Jitter
- Meets R20/SCVF Specification when used with SL9009

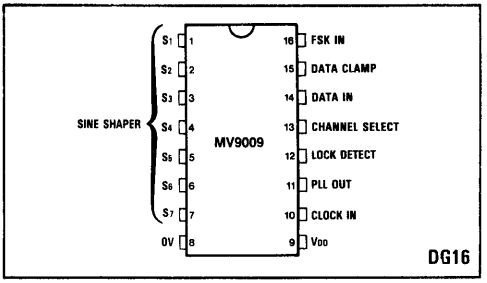


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Operating temperature	0° C to +70° C
Storage temperature	-65° C to +150° C
Supply voltage range	-0.3V to +7V
Input voltage range	-0.3V to V_{DD} +0.3V
Output voltage range	-0.3V to V_{DD} +0.3V

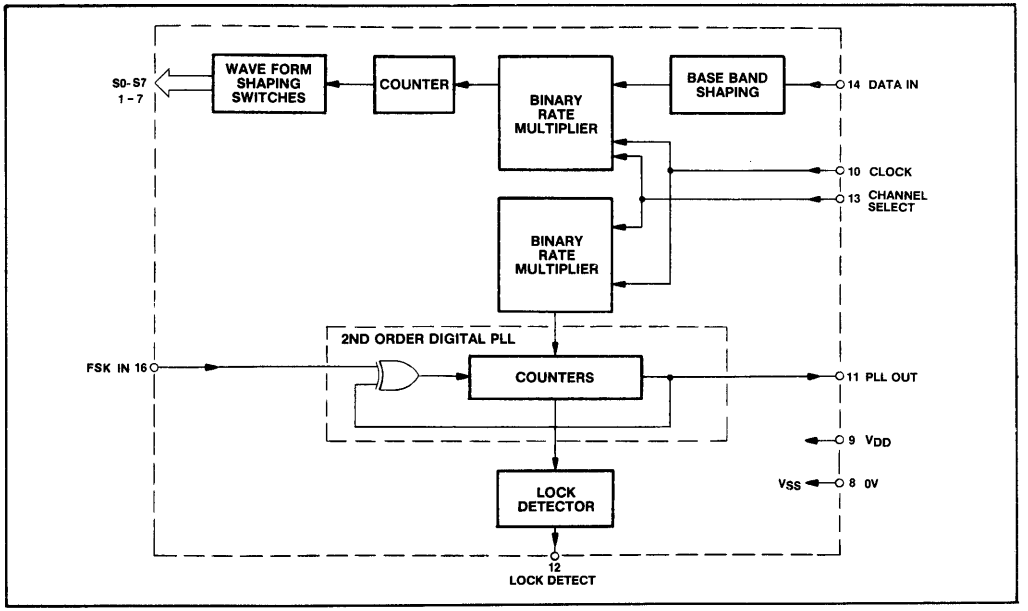


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C All potentials referred to pin 8

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply						
Voltage	9	4.5	5	5.5	V	For defined parametrics 0°C to +70°C
Current	9			2	mA	7.5MHz clock V_{DD} = 5.25V
	9			100	μA	Static
Clock input	10					
Input voltage high		3.3			V	V_{DD} = 4.75V
Input voltage low				1.58	V	V_{DD} = 5.25V
Input current				20	μA	V_{DD} = 5.25, V_{IN} = 5.5V
Other inputs	13,14,15,16					
Input voltage high		1.8			V	V_{DD} = 4.75V
Input voltage low				0.9	V	V_{DD} = 5.25V
Input current				20	μA	V_{DD} = 5.25V, V_{IN} = 5.5V
Hysteresis		30			mV	
Sine outputs (open drain)	1,2,3,4,5,6,7					
$R_{DS\ (ON)}$		20	32	47	Ω	V_{DD} = 4.75V
$\Delta R_{DS\ (ON)}$				10	Ω	I_{OL} = 5mA, V_{OL} = 0.5V
Lock detect	12					
Output voltage high		4.27			V	V_{DD} = 4.75, I_O = 4.75mA
Output voltage low				0.525	V	V_{DD} = 5.25V, I_O = 5.25mA
PLL out	11					
Output voltage high		4.995			V	I_O = 25μA, V_{DD} = 5V
Output voltage low				0.005	V	
Output s/c current				50	mA	V_{DD} = 5.25V

OPERATING NOTES

If it is desired to simplify the transmit filtering, the on-chip sine shaping circuit can be used. If this is not needed (for example when using the Reticon R5631 modem filter) then the square wave from pin 4 is used with a pull-up resistor.

The chip produces a sinewave output by scanning an array of 7 resistors as shown in Fig.3. The smallest resistor value should be chosen to be of the order Ron x 1000 ≃ 50kΩ.

Each resistor is successively connected to ground by N-channel MOS transistors within the chip then successively disconnected, as shown by Fig.4. Correct weighting of the resistors should give a sinewave output. If 1% matching of resistors is attained, the worst case distortion will be 2nd harmonic 47dB down on the fundamental. In Fig.4 a '0' indicates a closed switch, a '1' an open switch.

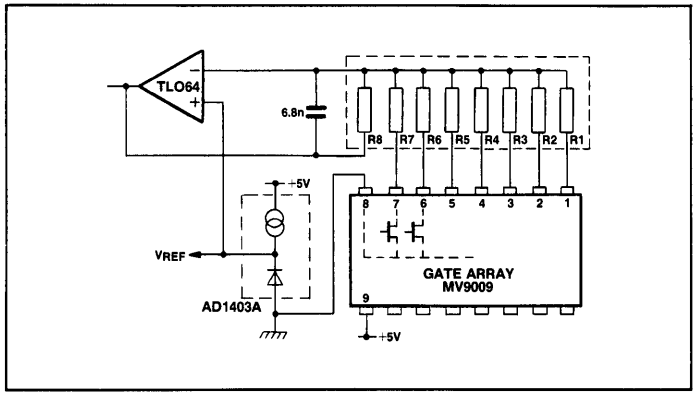
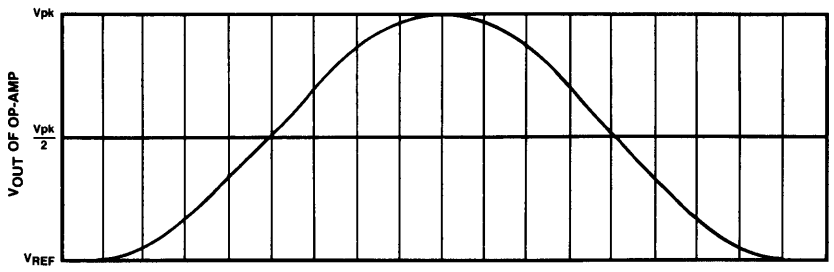


Fig.3 Output array scanning



$V_{ref} - V_{pk} = V_{ref}. R8/(R1 + R2 + R3 + R4 + R5 + R6 + R7)$

	PIN																	
LOB	7	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1
	6	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1
	5	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	4	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1
	3	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	2	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
MOB	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Phase	-90°								90°									270°	

Fig.4 16 step sinewave produced by scanning 7 resistors

OPERATING FREQUENCIES

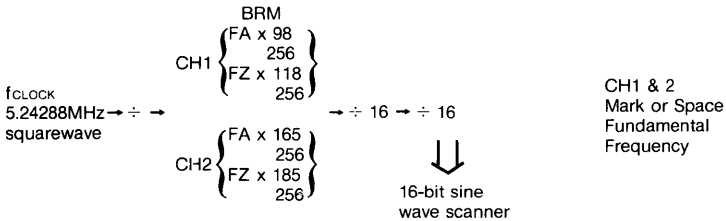
f_{CLOCK} = 5.24288MHz

Parameter	Conditions	Frequency (Hz)
CH1 Mark FZ	Pins 13,14 = 0V	1650
CH1 Space FA	Pin 13 = 0V Pin 14 = 5V	1850
CH2 Mark FZ	Pin 13 = 5V Pin 14 = 0V	980
CH2 Space FA	Pins 13,14 = 5V	1180
Receiver characteristics		
Centre frequency CH1		1080
Lock range CH1		398
Centre frequency CH2		1750
Lock range CH2		335

CIRCUIT DESCRIPTION

The MV9009 forms a digital transmitter and 2nd order PLL for modulation/demodulation of 300 Baud FSK signals. The chip transmits on one channel and receives on the other as defined by the truth Table 1.

The transmitter works by dividing a 5.24288MHz crystal clock as follows:



Baseband shaping is also provided for the data signal, to reduce out of band modulation products. This is performed digitally by taking 8 steps to change the Binary Rate Multiplier from FA to FZ.

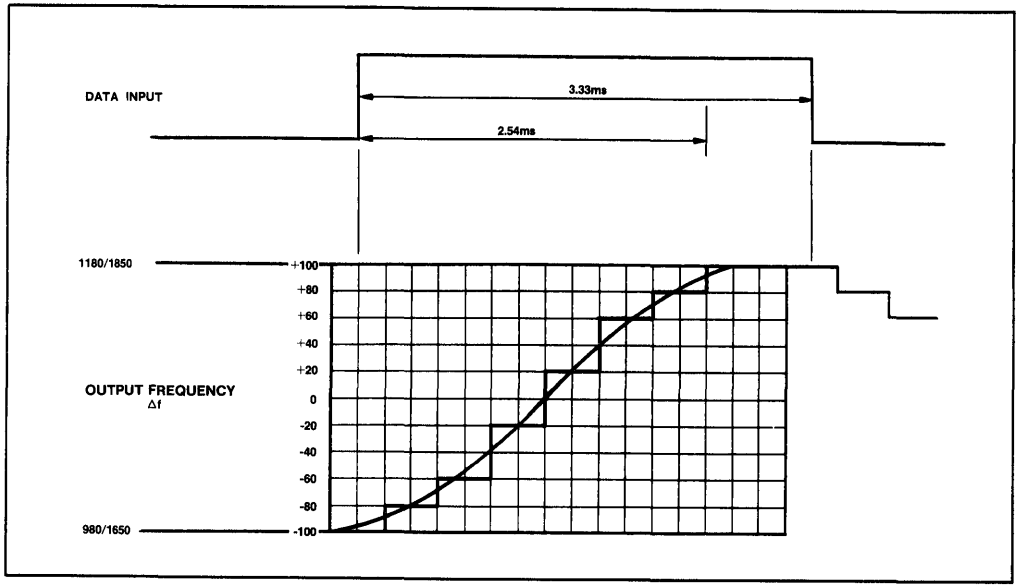


Fig.5

EXAMPLE

If the transmitter is operating at a continuous 980Hz output frequency and the data input goes to '1', the binary rate multiplier output is stepped from x 98/256 to x 118/256 as shown in Fig.5.

The receiver is a 2nd order digital phase locked loop, with an exclusive OR gate phase comparator. CMOS or TTL level FSK inputs are applied to the FSK input pin 16 and the demodulated signal appears at pin 11 as a twice carrier variable mark space ratio signal. A third order low pass post-detection filter and comparator are required in order to produce a data signal. The 2nd order PLL time constants have been optimised to give minimum jitter at 300 baud. Due to finite load times in the 12-bit counters a small amount of bias distortion (0.5 %) occurs in the demodulated signal, due to the loss of 1 or 2 least significant bits in the counters.

Fig.7 shows the block diagram for a complete modem also using the SL9009 Adaptive Cancellation Filter.

CHIP TRUTH TABLE

'1' = +5V '0' = 0V

Channel Select	Data IN	Data Clamp	FSK In	Transmitter Outputs	PLL Out	Lock Detect
Pin 13	14	15	16	1 to 7	11	12
0	0	0	980Hz 1180Hz	1650Hz	0 1	0
0	1	0	980Hz 1180Hz	1850Hz	0 1	0
1	0	0	1650Hz 1850Hz	980Hz	0 1	0
1	1	0	1650Hz 1850Hz	1180Hz	0 1	0
X	X	1	Valid input signal	S1-S4 0 S5-S7 OFF	PLL still demodulating	0
0	X	X	Inside Lock range	X	Undefined	1
1	X	X	Outside 970-1190Hz and 1640-1860Hz	X	Undefined	1
0	X	X	Outside Lock range	X	Undefined	Mainly 1
1	X	X	Outside	X	Undefined	Mainly 1

NOTE
The lock detector is mainly '1' when the input signal is outside the lock range. If a continuous signal is required a timer circuit is required to time out '0' intervals. Fig.6 shows a suggested circuit.

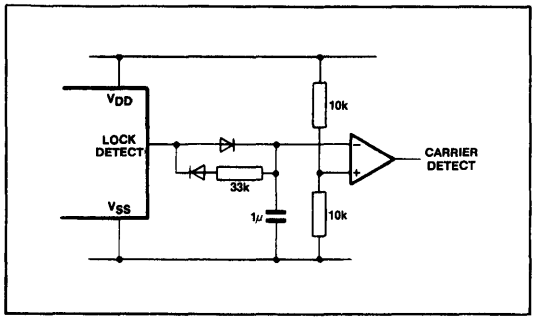


Fig.6

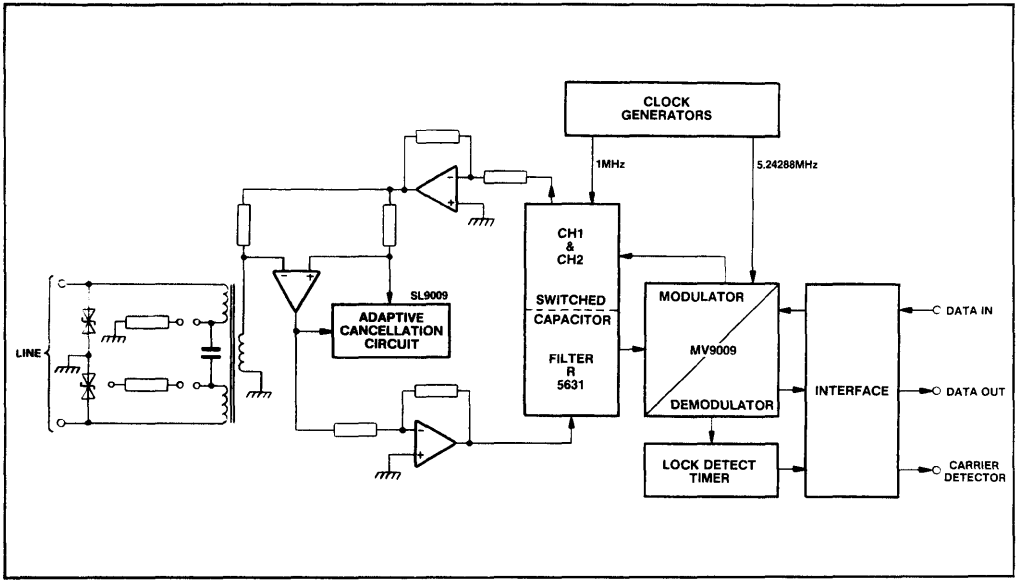


Fig.7 System block diagram

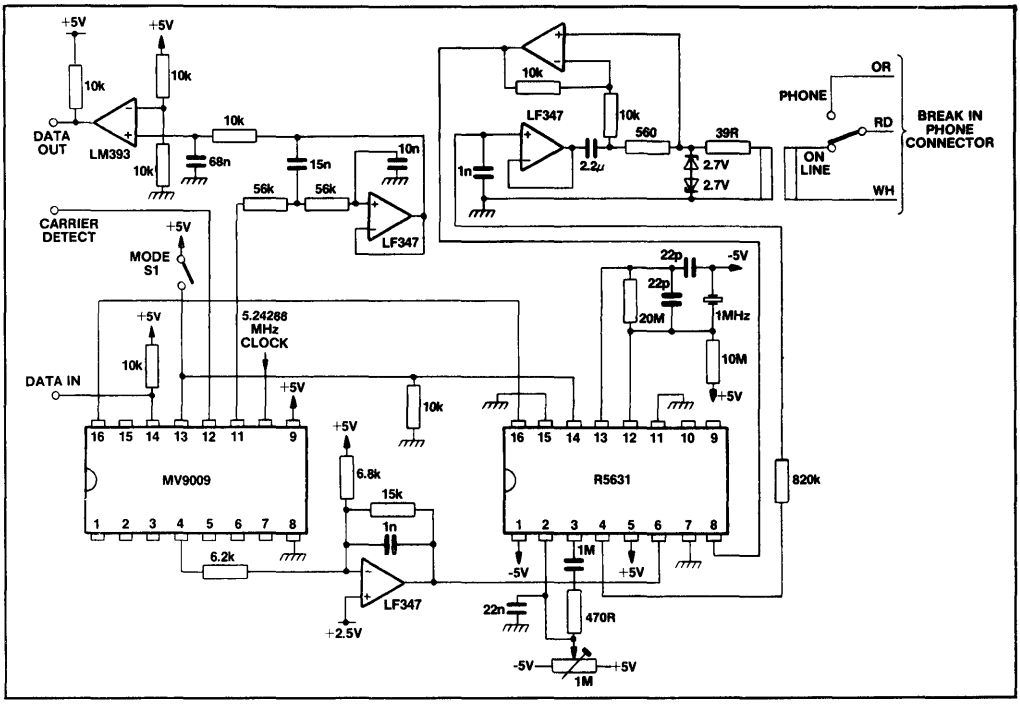


Fig.8 Basic V21 modem

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SL650B & C SL651B & C

MODULATOR/PHASE LOCKED LOOP CIRCUITS FOR MODEMS

The SL650/1 are versatile integrated circuits capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650 or SL651, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage –, current –, or resistance – programmable from zero to greater than 10,000.

An auxiliary amplifier with a voltage gain of, typically, 5000 is incorpated in the SL650 for use when it is required to interface to specified levels and impedances. The auxiliary amplifier features low bias current (typically 25nA), fast recovery from overload, and a short-circuit output current of ±7.5mA.

The auxiliary amplifier is omitted from the SL651.

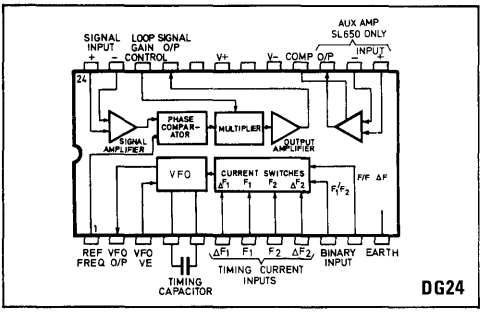

Fig.1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100:1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient:
  'B' Types 20 ppm/°C Max.
  'C' Types 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface
- Phase Comparator O/P Can Swing to Supply Voltages
- On-Chip Auxiliary Amplifier (SL650)

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	–55°C to +125°C

ELECTRICAL CHARACTERSTICS

Test conditions (unless otherwise stated)
Supply voltage ±6V
Temperature T_A +22°C ±2°C)

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current I_{CC}	17,19			3	mA	
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	17, 19		±20		ppm/%	
Voltage at timing current inputs	6, 7, 8, 9		±10		mV	See note 2
VFO output, 'low' state	2		0	0.2	V	
VFO output, 'high' state	2	+1.1	+1.3		V	$R_L \geqslant 10k\Omega$
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	10, 11			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	10, 11	+2.4			V	
Input current	10, 11		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	23, 24		±2		mV	V_{out} = 0V
Input bias current	23, 24		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	23, 24		100		kΩ	
Common mode I/P voltage range	23, 24	±4			V	
Differential I/P to limit (AC)	23, 24		1.0	10	mV rms	See note 4
Output current	21, 22	±1.0	±2.0	±5.0	mA	I_{22} = 250μA
Current gain (pin 22 to pin 21)	21, 22	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	21,23,24	±100	±250		mA/V	See note 5
Output voltage, linear range	21	±5	±5.5		V	
Output current	21			±2	μA	I_{22} = 0
Phase comparator I/P 'low'	1	−4		−0.2	V	
Phase comparator I/P 'high'	1	+1.9		+5.3	V	
Auxiliary amplifier (SL650 only)						
Differential I/P offset voltage	13, 14		±2		mV	V_{out} = 0V
Input bias current	13, 14		0.025	0.5	μA	V_{in} = 0V
Differential I/P resistance	13, 14	0.2	3		MΩ	
Common mode I/P voltage range	13, 14	±4			V	
Voltage gain (13–14) to 15	13,14,15	1000	5000		–	
Output voltage range	15	±4	±4.8		V	$R_L \geqslant 2k\Omega$
Output current limit	15	±4	±6.5	±12	mA	

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL650C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin 21) voltage-limits first.
5. For a control current input to pin 22 of 250μA The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high.'

ABSOLUTE MAXIMUM RATINGS

Supply voltages	± 7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

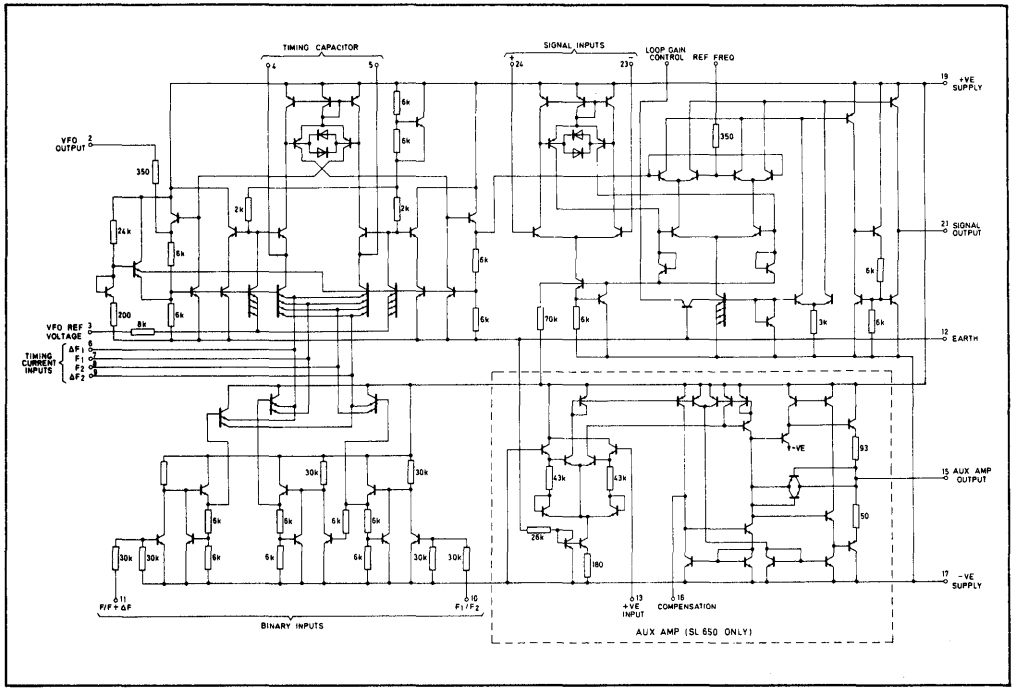

Fig. 2 Circuit diagram of SL650/SL651

OPERATING NOTES

Basic VFO Relationships

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 4 and 5, and directly proportional to the VFO timing current (see Fig.3). Four current switches, controlled by TTL-compatible logic inputs on pins 10 and 11 select a combination of external resistors (connected to pins 6, 7, 8 and 9) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to 0V however, then only the current switch associated with pin 7 is closed. the VFO timing current is then determined solely by the value of one resistor (R2 in Fig.3), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig.4 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR} \cdot \frac{V_R}{V_3}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 3), then

$$V_R = V_3$$

$$\text{and } f = \frac{1}{CR}$$

Pin 3 is normally connected to the chip negative supply; if, however, pin 3 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR} \cdot \frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 3

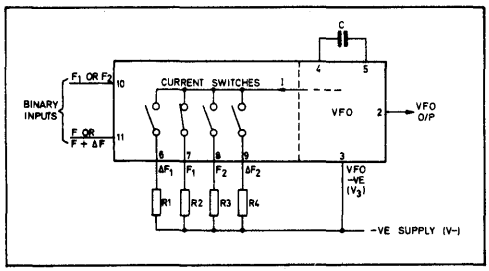

Fig. 3 VFO and binary interface

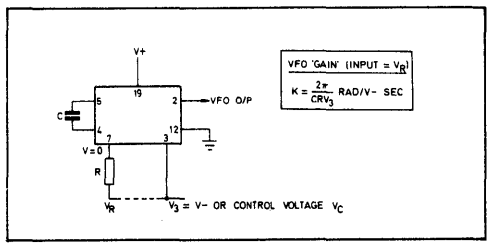

Fig. 4 VFO basic configuration

The timing current I should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig.3 the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 10	Pin 11	Timing Pins	VFO Frequency
LO	LO	7	$\frac{1}{CR_2}$
LO	HI	6 & 7	$\frac{1}{CR_2} + \frac{1}{CR_1}$
HI	LO	8	$\frac{1}{CR_3}$
HI	HI	8 & 9	$\frac{1}{CR_3} + \frac{1}{CR_4}$

Table 1 Binary interface relationships

Auxiliary amplifier

Internal compensation provides stability down to a closed loop gain of typically 20dB. A 30pF capacitor connected between pins 16 and 15 will give compensation down to a closed loop gain of unity. The output is short circuit protected but is not recommended for driving loads less than 2k

Phase Comparator

The phase comparator parameters are defined as follows (see Fig.5):

$$\text{Overall transconductance} = \frac{I_{21}}{V_{24} - V_{23}}$$

$$\text{Overall voltage gain} = \frac{V_{21}}{V_{24} - V_{23}}$$

The input amplifier will limit when the peak input ($V_{24} - V_{23}$) exceed ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

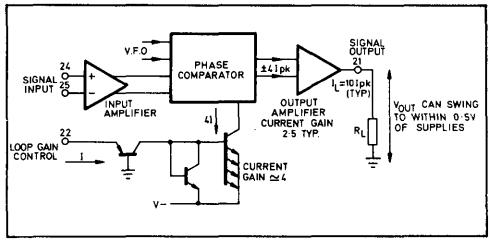

Fig. 5 Phase comparator

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SL652C

MODULATOR/PHASE LOCKED LOOP

The SL652C is a versatile integrated circuit capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using this device, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage – current – or resistance – programmable from zero to greater than 10,000.

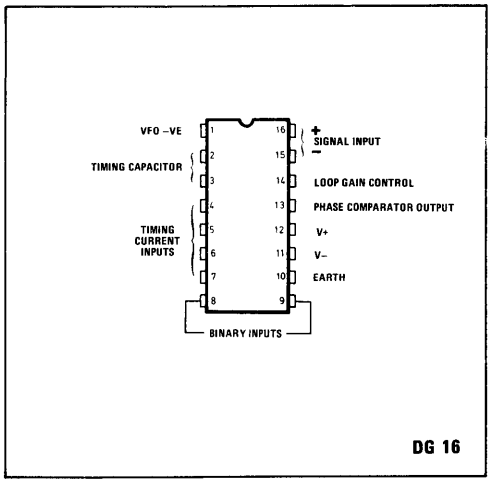

Fig. 1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100: 1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient: 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	0°C to +70°C
Supply Currents	1.5mA typ.

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators
- Stable Current-Controlled Oscillators

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±7.5V
Storage temperature	–55° to +175°C
Operating temperature	–55° to +125°C
Input voltages	Not greater than supplies

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage: ±6V
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	11, 12		±20		ppm/%	
Voltage at timing current inputs	4, 5, 6, 7		±10		mV	See note 2
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	8, 9			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	8, 9	+2.4			V	
Input current	8, 9		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	15, 16		±2		mV	V_{out} = 0V
Input bias current	15, 16		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	15, 16		100		kΩ	
Common mode I/P voltage range	15, 16	± 4			V	
Differential I/P to limit (AC)	15, 16		1.0	10	mV	See note 4
Output current	13, 14	±1.0	±2.0	±5.0	mA	I_{14} = 250μA
Current gain (pin 14 to pin 13)	13, 14	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	13, 15, 16	±100	±250		mA/V	See note 5
Output voltage, linear range	13	±5	±5.5		V	
Output current	13			±2	mA	I_{14} = 0

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL652C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin. 13) voltage-limits first.
5. For a control current input to pin. 14 of 250μA. The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

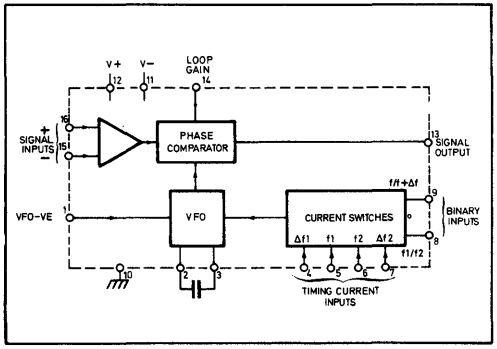

Fig. 2 SL652C block diagram

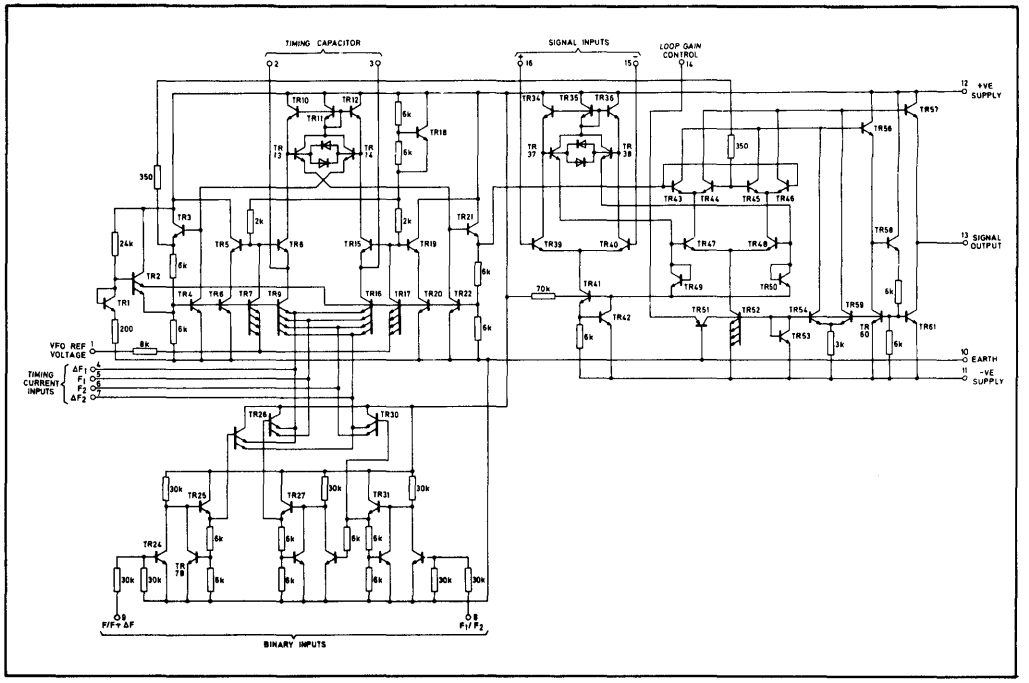

Fig. 3 Circuit diagram of SL652

OPERATING NOTES

Basic VFO Relationships

The oscillator output is normally taken from the phase comparator output by biasing the signal inputs a few hundred millivolts apart. If a direct oscillator output is required when the phase comparator is otherwise employed, it should be taken from pin 2 or 3 (which may affect oscillator stability). Alternatively, an SL651C can be used in place of the SL652C.

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 2 and 3, and directly proportional to the VFO timing current (see Fig.4). Four current switches, controlled by TTL-compatible logic inputs on pins 8 and 9 select a combination of external resistors (connected to pins 4, 5, 6 and 7) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to OV however, then only the current switch associated with pin 5 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig. 4), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig. 5 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR}\frac{V_R}{V_1}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 1) then

$$V_R = V_1$$

$$\text{and } f = \frac{1}{CR}$$

Pin 1 is normally connected to the chip negative supply; if, however, pin 1 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR}\frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 1.

The timing current should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig. 4, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 8	Pin 9	Timing Pins	VFO Frequency
LO	LO	5	$\frac{1}{CR_2}$
LO	HI	4 & 5	$\frac{1}{CR_2}+\frac{1}{CR_1}$
HI	LO	6	$\frac{1}{CR_3}$
HI	HI	6 & 7	$\frac{1}{CR_3}+\frac{1}{CR_4}$

Table 1 Binary interface relationships

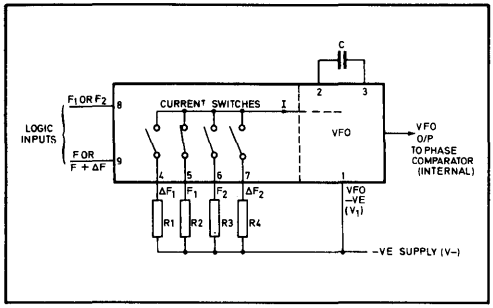

Fig. 4 VFO and binary interface

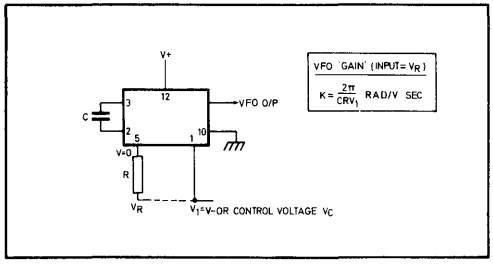

Fig. 5 VFO basic configuration

Phase Comparator

The phase comparator parameters are defined as follows (see Fig. 6):

$$\text{Overall transconductance} = \frac{I_{13}}{V_{16}-V_{15}}$$

$$\text{Overall voltage gain} = \frac{V_{13}}{V_{16}-V_{15}}$$

The input amplifier will limit when the peak input ($V_{16} - V_{15}$) exceeds ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

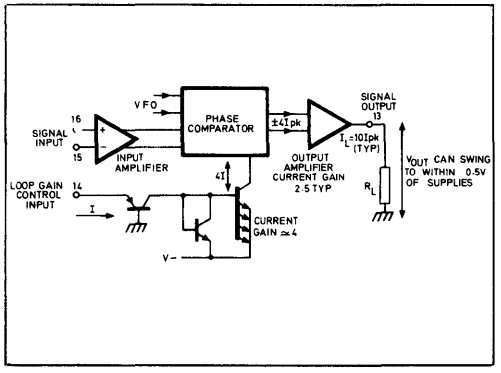

Fig 6. Phase comparator

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PRELIMINARY INFORMATION

SL8204

TELEPHONE TONE RINGER

The SL8204 is a telephone set tone ringer IC. It is packaged in an 8 pin DIL Minidip. The unit is designed for use as a telephone set bell replacement, or as an extension ringer. The SL8204 will drive a speaker in place of the existing bell, using power supplied from the telephone line.

Two audio oscillators are incorporated. The low frequency oscillator shifts the high frequency oscillator between 508 and 635Hz at a 10Hz rate. These frequencies are determined by external components which may be changed as desired. The IC has a built-in threshold circuit with hysteresis which prevents false triggering, eliminates rotary dial 'chirps', and provides positive switching operation.

The IC may also be used for other applications requiring an attention-getting sound. Output power from the built-in amplifier is nominally 35mW, and will produce a maximum 90dBA sound pressure-level from a properly baffled 2 inch speaker.

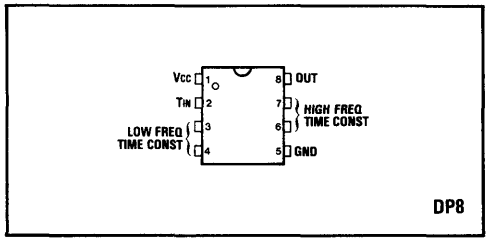


Fig.1 Pin connections - top view

FEATURES

- Low Current Drain
- Small Size (mini-DIP)
- Adjustable Frequency
- Threshold Circuit Prevents False Triggering and Rotary Dial 'Chirps'
- Built-In Hysteresis For Positive Enable
- Few External Components
- Up To 90dBA Sound Pressure Level

ABSOLUTE MAXIMUM RATINGS

Supply voltage	30V d.c.
Storage temperature range	-65°C to +150°C
Operating temperature range	-45°C to +65°C

APPLICATIONS

- Telephone Bell Replacement
- Extension Ringers

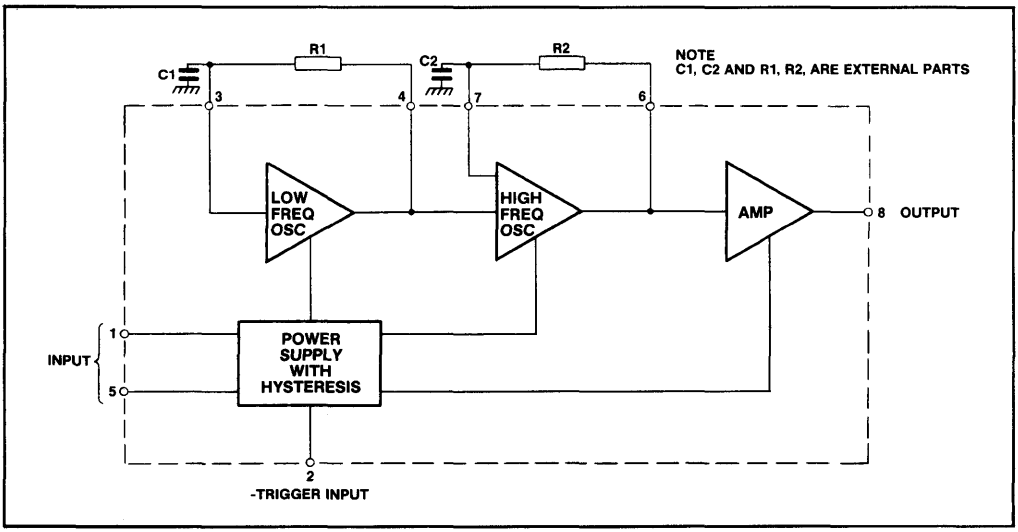


Fig.2 SL8204 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -45°C to +65°C

Characteristic	Value			Units	Conditions		
	Min.	Typ.	Max.				
Initiation supply voltage V_{SI}	17	19	21	V	See Fig.4		
Sustaining voltage V_{SUS}	9.7	11.5	13	V	See Fig.4		
Supply current I_{SI}	1.4	2.5	4.2	mA	No load. See Fig.4		
Supply current I_{SUS}	0.7	1.4	2.5	mA	See Fig.4		
K1, f_{H1} (constant) See Eq.1	1/1.681	1/1.515	1/1.380				
f_{H1} (frequency)	458	508	558	Hz	R_2 = 191k	C_2 = 6800pF	
K2, f_{H2} (constant) See Eq. 2	1.190	1.250	1.310				
f_{H2} (frequency)	545	635	731	Hz	R_2 = 191k	C_2 = 6800pF	
K3, f_L (constant) See Eq. 3	1/1.367	1/1.234	1/1.118				
f_L (frequency)	9	10	11	Hz	R_1 = 173k	C_1 = 0.47μF	
Operating voltage	-	-	29	V			
Output voltage high	18.0	19.0	20.0	V	V_{CC} = 21V Pin 6 = 6V	I(Pin 8) = -15mA Pin 7 = GND	
Output voltage low	0.5	0.9	1.3	V	V_{CC} = 21V Pin 6 = GND	I(Pin 8) = 15mA Pin 7 = 6V	
Trigger voltage V_T	8.5	9.5	10.5	V	V_{CC} = 15V See Note 1		
Trigger current I_T		20.0	1000	μA	See Notes 1 and 3		
Disable voltage V_D		0.4	0.8	V	T_{amb} = 25°C See Note 2		
Disable current	-40	-50		μA	T_{amb} = 25°C See Note 2		
I_{IN} (Pin 3)	-	-	500	nA	Pin 3 = 6V	Pin 4 = GND	
I_{IN} (Pin 7)	-	-	500	nA	Pin 7 = 6V	Pin 6 = GND	
I (Pin 4) Source V_{CC} = V_{SUS}	150	300	600	μA	Pin 3 = GND	Pin 4 = GND	
I (Pin 4) Sink V_{CC} = V_{SUS}	100	200	350	μA	Pin 3 = 6V	Pin 4 = 5V	
I (Pin 6) Source V_{CC} = V_{SUS}	80	175	350	μA	Pin 6 = GND	Pin 7 = GND	Pin 4 = GND
I (Pin 6) Source V_{CC} = V_{SUS}	125	250	500	μA	Pin 6 = GND	Pin 7 = GND	Pin 4 = 8V
I (Pin 6) Sink V_{CC} = V_{SUS}	70	125	250	μA	Pin 6 = 5V	Pin 7 = 6V	Pin 4 = GND
I (Pin 6) Sink V_{CC} = V_{SUS}	100	200	300	μA	Pin 6 = 5V	Pin 7 =6V	Pin 4 = 8V

NOTES
1. V_T and I_T are the conditions applied to Pin 2 to start oscillation for $V_{SUS} < V_{CC} < V_{SI}$
2. V_D and I_D are the conditions applied to Pin 2 to inhibit oscillation for $V_{SI} < V_{CC}$
3. Trigger Current must be limited externally

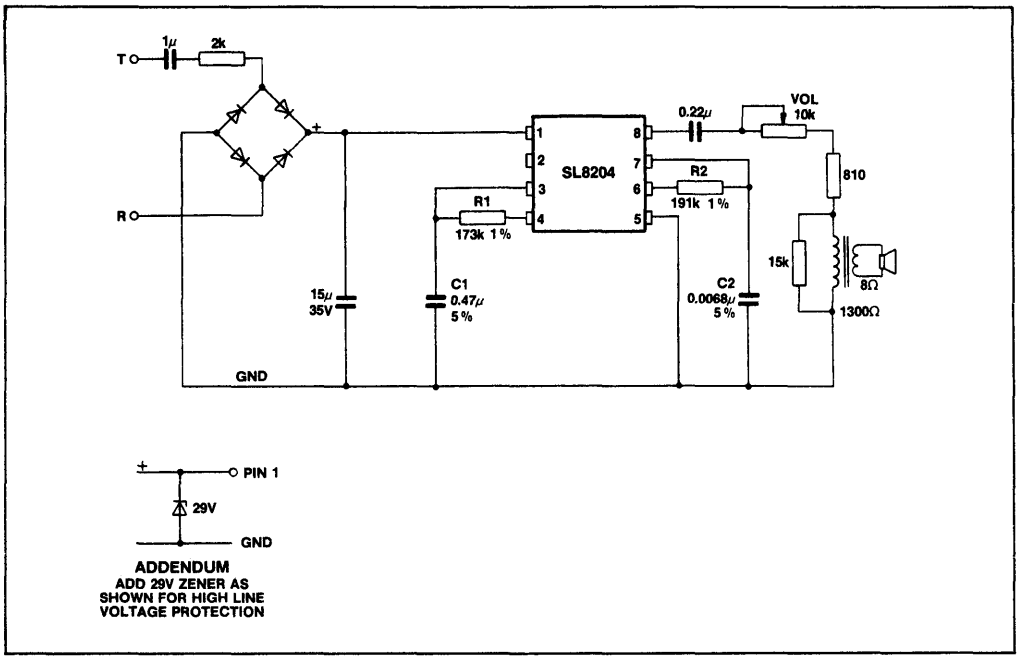


Fig.3 Circuit diagram - tone ringer

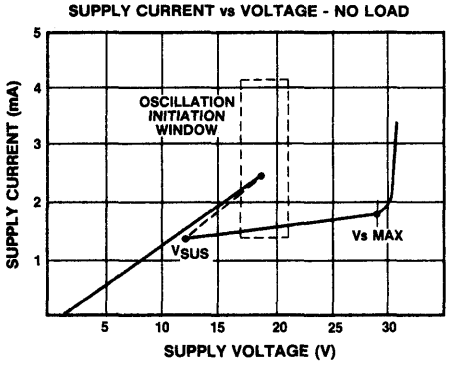


Fig.4 Tone ringer characteristics

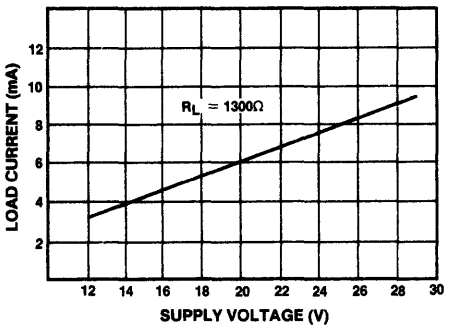


Fig.5 Typical RMS current

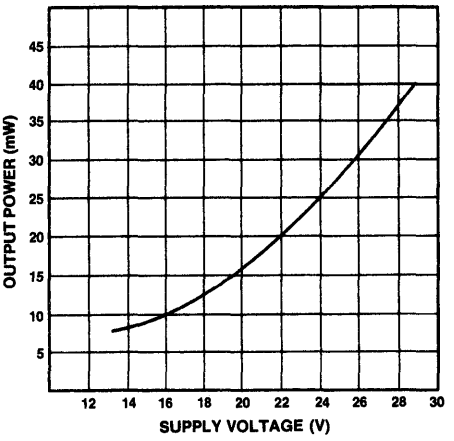


Fig.6 Typical power output

PLESSEY
Semiconductors

PRELIMINARY INFORMATION

SL9009EXP

ADAPTIVE CANCELLATION FILTER

The SL9009 is a bipolar integrated circuit designed for use in duplex modems on 600Ω telephone lines. It automatically optimises the duplexer such that the transmitted signal is cancelled at the input to the receiver.

- Automatically Simulates Impedance Characteristic of Line
- Independently Variable L,C,R Impedance Components
- Achieves Typical 40dB Rejection of Transmitted Signal
- Requires Only 2 External Op-Amps for Complete Adaptive Duplexer
- 16 Pin DIL Package
- ±4.5 to ±7V Supply Range

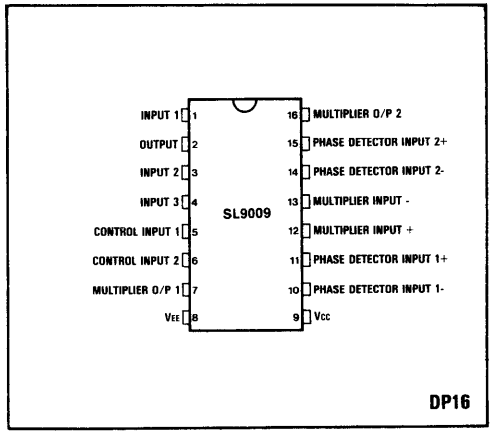


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	0°C to 70°C
Storage temperature range	-10°C to +125°C
Supply voltage range	±4.5V to ±10V
Input voltage range	
Pins 1,2,3,4,5,6,10,11,12,13,14,15	V- to V+
Output voltage range	
Pins 16,7	V- to V+
Input voltage range	
Pins 1,3 and 4 relative to Pin 2	±5V
Supply voltage range	
For specified parameters	±4.5V to ±7V

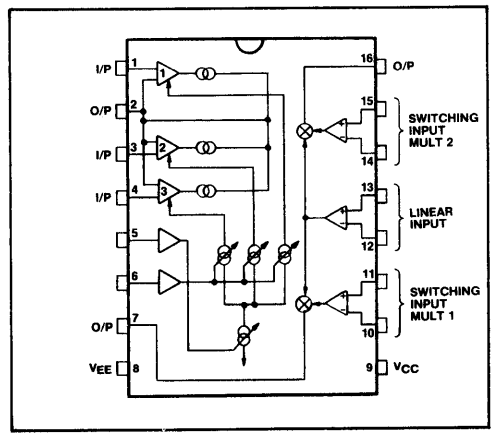


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
±4.5V to ±7V supply, 0° C to 70° C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply currents	0.8	1.3	2.0	mA	Pin 5 at V-, all other inputs and outputs at 0V
4-Quadrant multipliers					
Input offset voltage multiplier switching inputs			9	mV	Pins 14,15 and 10,11
Input offset voltage multiplier linear input			13	mV	Pins 12,13
Input bias current		0.1	0.7	μA	Pins 10 to 15
Input offset currents			±0.15	μA	Pins 10,11,12,13,14 and 15
Input common-mode range	V- +2.7		V + -2.7	V	Pins 10 to 15
Output offset current pin 7(16)			±1.2	μA	$V_{12} = V_{13} = 0V$ $V_{10} - V_{11}$ ($V_{14} - V_{15}$) = 200mV p-p sine wave
Transconductance $V_{12} - V_{13}$ to pin 7(16)	250	500	1000	μohm	$V_{10} - V_{11}$ ($V_{14} - V_{15}$) switched (±100mV)
Output voltage compliance	V- +2.5		V + -2	V	<0.2μA change in output current, pin 7 or 16
Transconductance cells					
Offset current pin 2			±12	μA	Cell under test set for gain = 4, other cells for gain 0, $V_2 = 0V$
Input impedance					Pin 2 = 0V
Pin 1	3		10	kΩ	
Pins 3 and 4	4		14	kΩ	
Operating voltage range					
Pins 1,2,3,4	V- +2.7		V +-2	V	
Gain range, each cell		0.05-10			
Input current range Pins 1,3,4	±10			μA	For <1 % non-linearity
Control inputs					
Input current I_5, I_6			0.12	μA	V_5, V_6 = +V
Control voltage input range Pin 5	V- +2.7		V- +6	V	Cell gain 0.05-10
Input range Pin 6	-2		+1.8	V	For cell 2 or 3 gain ≤2 x cell 1 gain, V + = -(V-)

PRINCIPLES OF OPERATION

The cancellation principle is to use the conductance cells to simulate the characteristics of the line, in a bridge circuit to separate out the received signal from the transmitted signal. The bridge output goes to two phase-sensitive detectors which detect the out-of-balance signal components in phase and in quadrature with the cancellation signal, derived from the transmit signal. These out-of-balance currents are integrated and fed back to the conductance cells, to adjust the effective resistance and capacitance or inductance until the bridge is balanced and the transmit signal is completely cancelled out. The current source characteristics are arranged to keep the loop stable for all normal line characteristics.

Description of Conductance Cell

Each conductance cell is effectively a variable-gain current amplifier with a gain approximately equal to

$$\frac{\text{CONTROL CURRENT}}{20\mu A}$$

The input roughly follows the output voltage, with an effective input series resistance of about 5kΩ. Therefore, with an impedance Z connected from the input to ground, the impedance seen at the output is approximately

$$(Z + 5k\Omega) \times \frac{20\mu A}{\text{CONTROL CURRENT}}$$

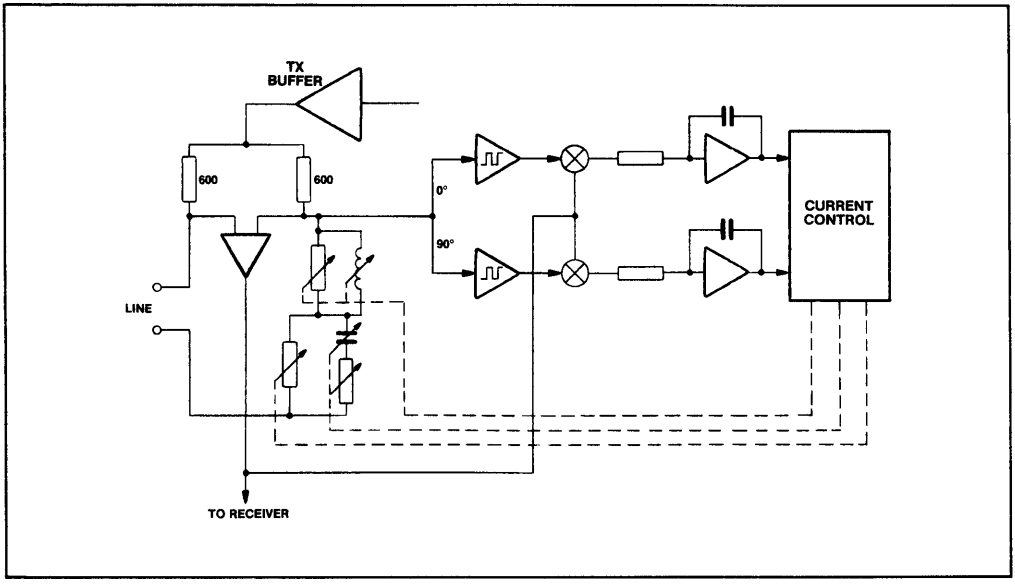


Fig.3 Simplified circuit illustrating cancellation principle

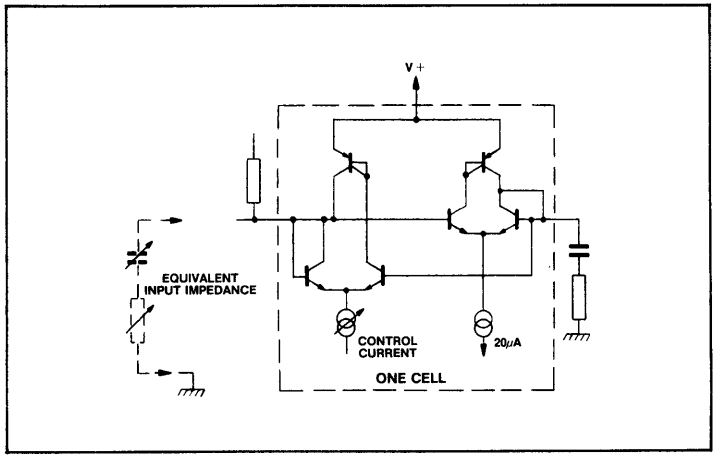


Fig.4 Conductance cell schematic

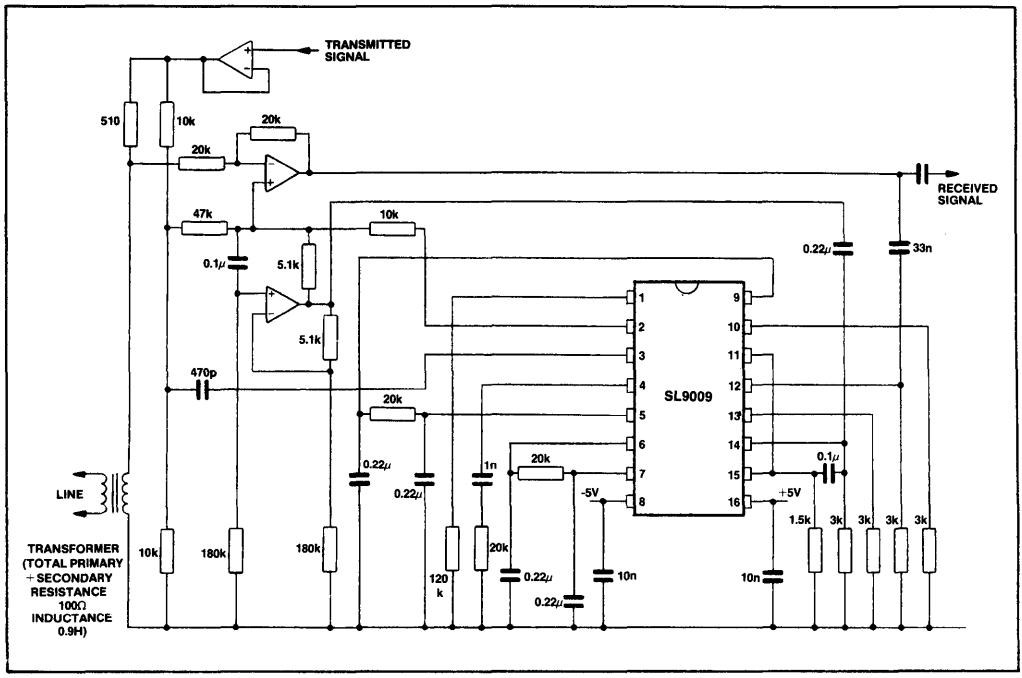


Fig.5 Typical line circuit for modem (900-3000Hz transmit frequency)

PLESSEY
Semiconductors

SP1404BW, D3702

HIGH VOLTAGE INTERFACE CIRCUIT

The SP1404 is a bipolar integrated circuit comprising five individual digital current amplifier circuits. Each circuit accepts a logic input from TTL, CMOS or a similar source and drives a high-current load at the output. The outputs are capable of withstanding high negative voltages in the 'off' state, making the SP1404 particularly suited to telecommunications applications.

The D3702 is a version of the SP1404BW in 14 pin plastic package approved to BT specification.

CIRCUIT DESCRIPTION (FIG.2)

The SP1404 operates as a power amplifier interfacing from a voltage-level sensitive input to a high-current output switch. The input threshold is TTL-compatible, with a low input current requirement enabling one standard TTL output to drive many interfaces. The low input current requirement also makes it possible to use series current-limiting resistors to protect the SP1404 inputs.

Each element of the device performs an inverting function, i.e. a low voltage level on the input causes a high current in the output. If the input is left open-circuit, the output will be off and the output current will be zero.

The isolation of the integrated circuit is biased to the more negative of the two earth points by diodes D1 and D2 so that differences of up to (V_{CC} - 1) volts can be tolerated between the 'noisy' exchange earth and the 'quiet' electronic earth.

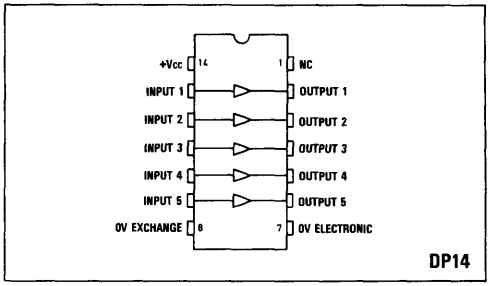


Fig. 1 Pin connections (viewed from underside)

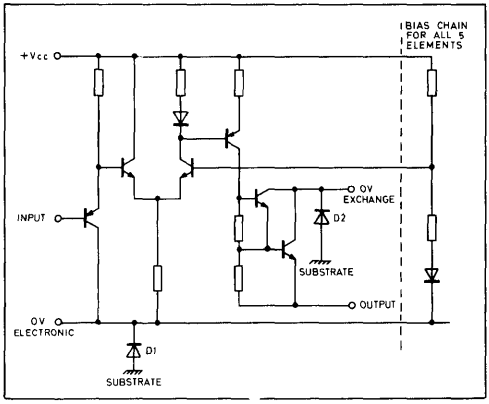


Fig. 2 Circuit diagram of one element

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
Temperature range = 0°C to +70°C
V_{CC} = +5V ± 0.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current		−20		μA	V_{in} = 0V
		−2		μA	V_{in} = V_{cc}
Output voltage			1.5	V	V_{in} = 0.8V, I_{out} = 50mA
Output current (Off state)			100	μA	V_{in} = 2V, V_{out} = -60V
Output current (On state)	50	80		mA	Vin = 0.8V
V_{CC} supply current		30		mA	V_{cc} = 5V, all inputs low
Total power dissipation		450		mW	V_{cc} = 5V, all inputs low all outputs I_{out} = 50mA

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Chip operating temperature	+150°C
Ambient temperature (I_{out} = 50mA)	+85°C
Load current	80mA
Voltage between output and 'noisy' earth	−65V
V_{CC} to output voltage	75V
V_{CC} to electronic earth	7V
Input voltage	V_{CC} + 1V

PLESSEY
Semiconductors

SP1450B(B) & SP1455B(B)

PCM SIGNAL MONITOR CIRCUITS

The SP1450 and SP1455 are bipolar integrated circuits designed to monitor errors in three-level digital signals modulated by a three-alphabet 4B3T code such as MS43. They can also indicate the failure of positive or negative pulses in the signal. The high frequency capability allows operation in PCM systems up to 34M bit/s (SP1450) and 140M bit/s (SP1455). Facilities are provided to adjust input thresholds independently on each polarity of input and the error output can be interfaced with low speed CMOS circuitry or high speed ECL.

The SP1450B(B) and SP1455B(B) are similar to the SP1450B and SP1455B but are screened to MIL-STD-883, Method 5004, Class B.

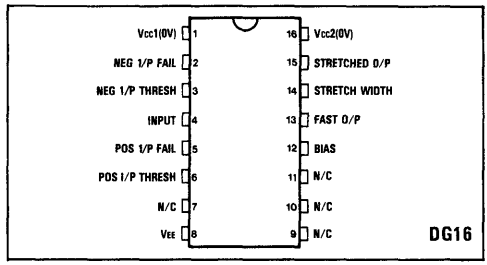


Fig.1 Pin connections (top view)

FEATURES

- Suitable for 34, 120 and 140M bit/s PCM
- Positive and Negative Input Signal Fail Outputs
- High Speed Error Output
- Low Speed 'Stretched' Output
- Low Power Consumption

APPLICATIONS

- PCM Telephone Transmission Terminal Equipment
- PCM Repeaters
- Error Checking Test Equipment

QUICK REFERENCE DATA

- Supply Voltage -4.4V to -5.25V
- Operating Temperature Range -10°C to +70°C
- Power Consumption 100mW typ
- Input Voltage Range ±450mV to ±1100mV (SP1450)
  ±450mV to ±600mV (SP1455)
- Thermal Resistance θj-a 100°C/W

ABSOLUTE MAXIMUM RATINGS

Supply voltage -8V
Reverse input current (pin 4) 5mA (continuous) 20mA (10us max)
Forward input current (pin 4) 20mA (10us max)
Storage temperature -55°C to +150°C
Operating temperature -10°C to +70°C
Junction temperature 150°C

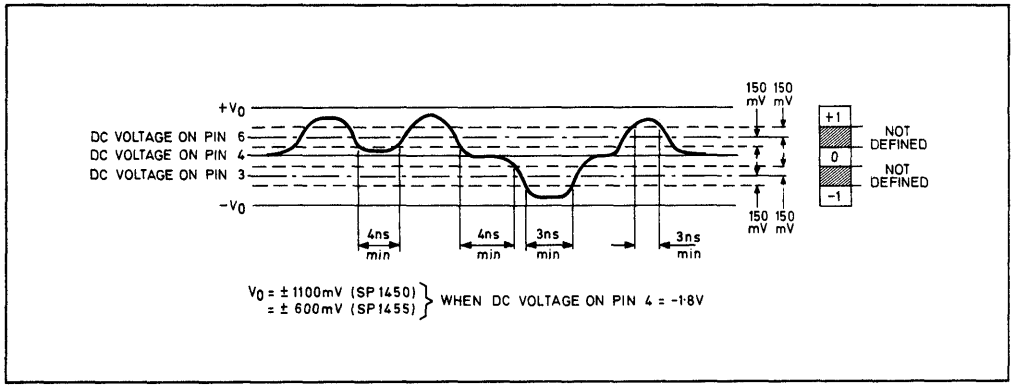


Fig.2 Input pulse wave form

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = Pins 1-16 = 0V
V_{EE} = Pin 8 = -5.0V
T_{amb} = +25°C
Input voltage range (pins 3,4,6) = -0.9V to -3.1V

DC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output low, current	2	0.9	1.2	1.9	mA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2.0V
Output low, current	2	0.7	—	—	mA	Pin 2 = OV Pin 3 = —1.95V Pin 4 = —2.0V
Output high, current	2	—	—	1	µA	Pin 2 = OV Pin 3 = —2.3V Pin 4 = —2.0V
Output high, current	2	—	—	0.4	mA	Pin 2 = OV Pin 3 = —2.05V Pin 4 = —2.0V
Output low, current	5	0.9	1.2	1.9	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.3V
Output low, current	5	0.7	—	—	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.05V
Output high, current	5	—	—	1	µA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.7V
Output high, current	5	—	—	0.4	mA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.95V
Output low, current	13	6.0	7.0	9.0	mA	Pin 13,15 = OV Pin 3 = —1.7V Pin 4 = —2.0V Pin 6 = —2.3V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V Six pos. or neg. pulses on pin 4
Output high, current	15	—	—	1	µA	
Output high, current	13	—	—	1	µA	Pin 13, 15 = OV Pin 3 = —2.3V Pin 4 = —2.0V Pin 6 = —1.7V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V
Output low, current	15	0.5	0.75	—	mA	
Current consumption	1,16	—	20	25	mA	(Pins 2,5,13,15 = OV (Pins 3,6 = —2.3V (Pin 4 = —2.0V (27 kΩ resistor between (Pin 14 and —5V (Pin 12 open
Input bias current	3	—	—	40	µA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2V
Input bias current	6	—	—	40	µA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —1.7V
Input bias current	4	—	—	80	µA	Pins 2,5 = OV Pins 3,6 = —2.3V Pin 4 = —2.0V

AC CHARACTERISTICS

Circuit reference: Fig.3
Input signal: Fig.2
T_{amb} = -10°C to +70°C
V_{EE} = -4.4V to -5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Input Frequency						
SP1450	13		—	25.5	M band/s	See note 1 below
SP1455	13		—	105	M band/s	See note 1 below
Stretched output pulse width	15	0.5	0.7	2	µS	c_1 = 390 pF R_1 = 27 kΩ using circuit of Fig. 7 (see note 2 below)
Error pulse width SP1455	13	4.25	—	5.25	nS	Input freq. 105 M band/s
Error pulse amplitude	13	300	—	—	mV	At max input frequency
Spurious pulse amplitude	13	—	—	50	mV	At max. input frequency

NOTE 1: These figures are the max.input symbol rates. For 4B3T codes, the effective bit rate is 4/3 x (input frequency).
NOTE 2: Resistor and capacitor values quoted are absolute values; temperature coefficients and tolerances have not been taken into account.

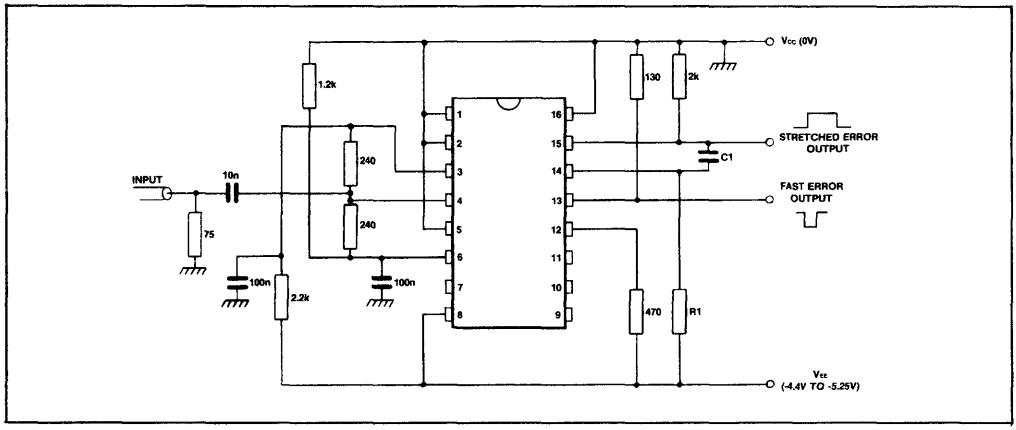


Fig.3 Functional test circuit

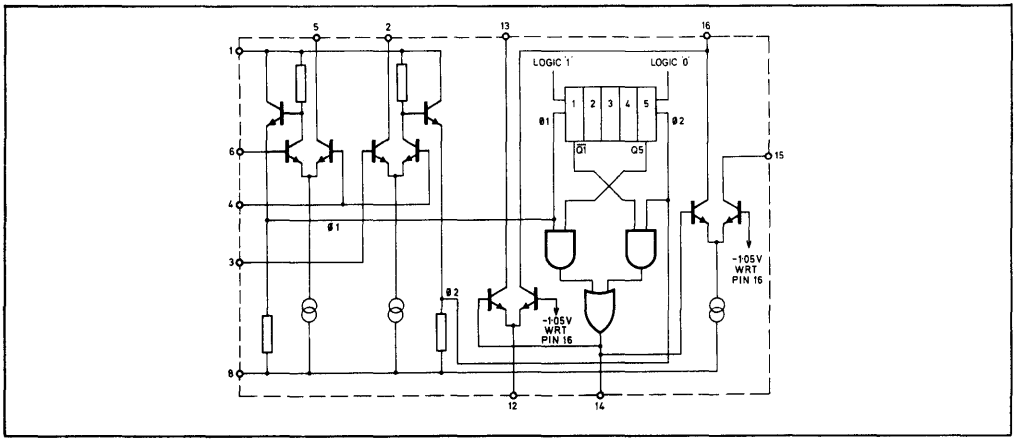


Fig.4 Circuit diagram of SP1450/SP1455

APPLICATIONS

The circuit shown in Fig.3 is designed to accept a three level (ternary) input signal as shown in Fig.2. The input is applied to pin 4 whilst fixed bias levels are maintained on pins 3 and 6. When a positive input pulse is applied at a level more positive than the bias on pin 6 the positive comparator output o 1 goes from '0' (V_{EE}) to '1' (V_{CC}). The 1-0 edge of this pulse clocks the five bit shift register one place to the right. Repeated operation will cause a pattern of logic '1's to be propagated along the shift register. When bit 5 is at logic '1' and the input is also positive an 'error' will occur at pins 13 and 15.

A negative input pulse at a level more negative than the voltage on bias pin 3 causes the negative comparator output o 2 to clock the shift register one place to the left. Repeated operation causes a pattern of logic '0's to be propagated along the shift register. When bit 1 is at logic '0' and the input is also negative an 'error' output will again occur at pins 13 and 15.

During normal operation the shift register can assume one of only six possible states as shown in Fig.5.

State	1	2	3	4	5
A	0	0	0	0	0
B	1	0	0	0	0
C	1	1	0	0	0
D	1	1	1	0	0
E	1	1	1	1	0
F	1	1	1	1	1

Fig.5 Shift register states

When power is initially connected other states may occur.

Two 'error' outputs are available. The fast output at pin 13 is negative going; the peak current is defined by a resistor connected between pin 12 and V_{EE} according to the formula:

$$I = \frac{3.3}{R} \text{ (e.g. 820 ohms; 4mA)}$$

A pullup resistor must then be connected between pin 13 and V_{CC} to give a suitable voltage swing. A suitable ECL interface is shown in Fig.6.

If, as in a repeater application, a fast output is not required, pin 12 should be left open and pin 13 connected to V_{CC} (pin 16).

A stretched output is available from pin 15 by connection of a capacitor between pins 14 and 15. A suitable circuit is shown in Fig.7.

Facilities are available at pins 2 and 5 to detect the absence of negative and positive going input signals. If these are not required pins 2 and 5 should be connected to V_{CC} (pin 1). A CMOS interface circuit is shown in Fig.8.

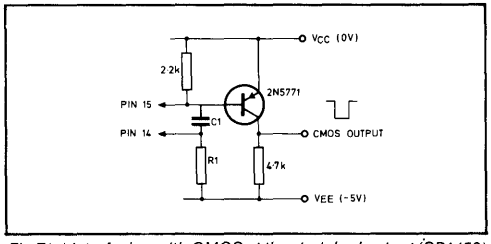


Fig.7(a) Interfacing with CMOS at the stretched output (SP1450)

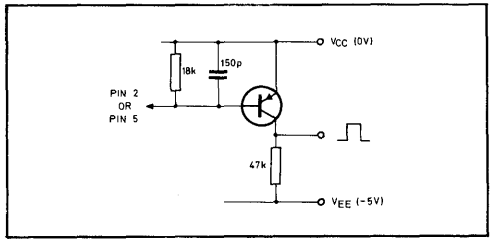


Fig.8 Interfacing with pulse fail output with CMOS

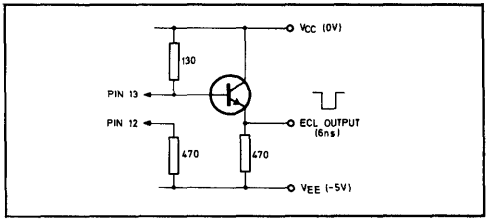


Fig.6 Interfacing with ECL at the output

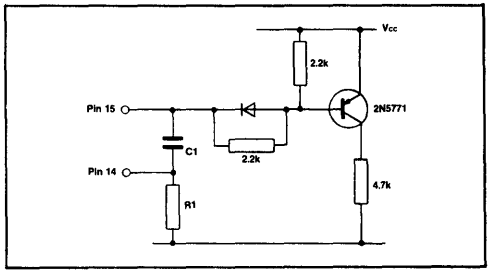
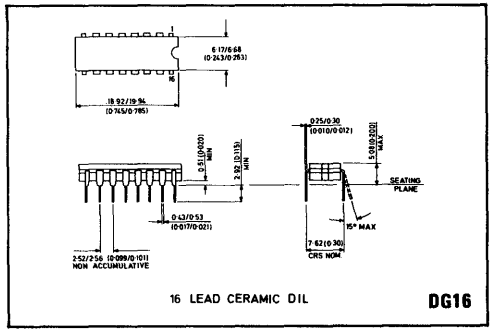
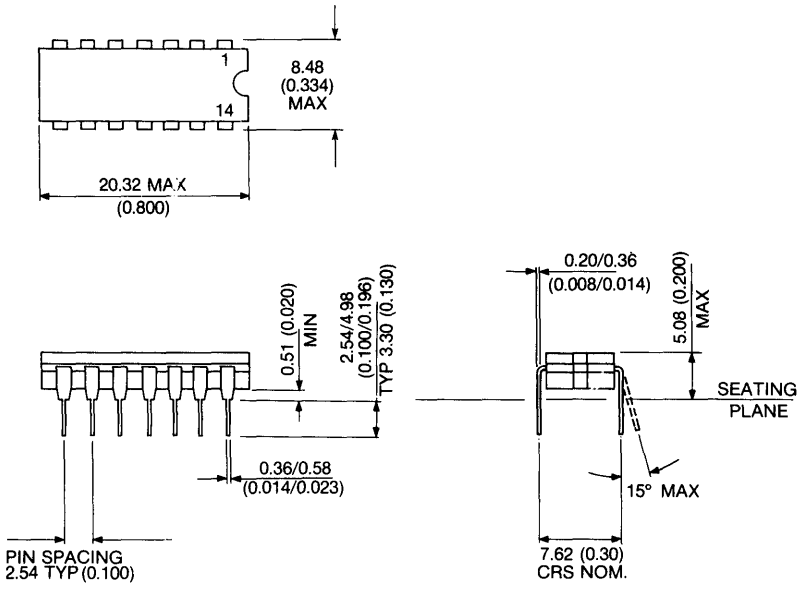


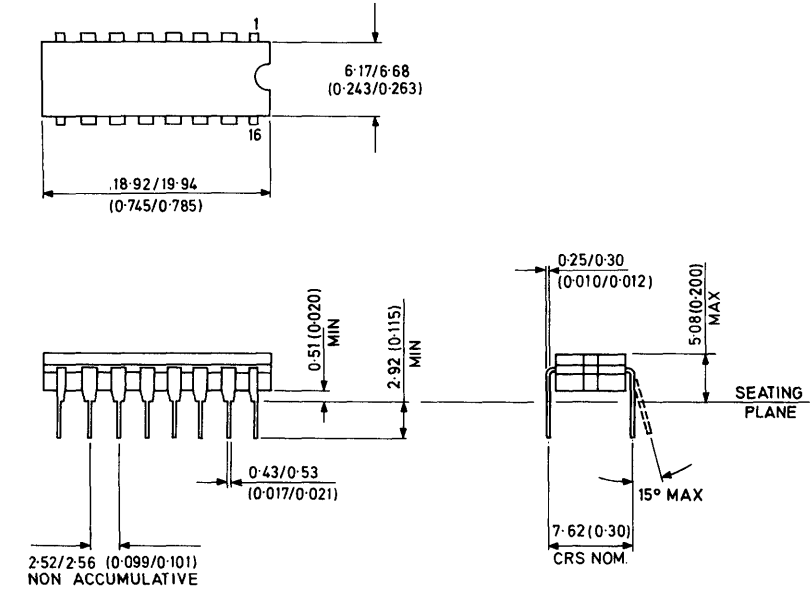
Fig.7(b) Interfacing with CMOS at the stretched output (SP1455)



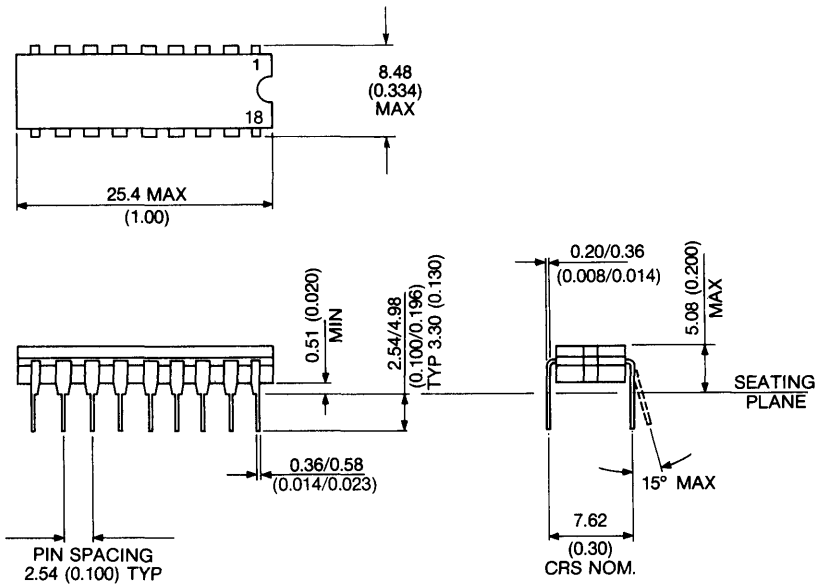
Package Outlines



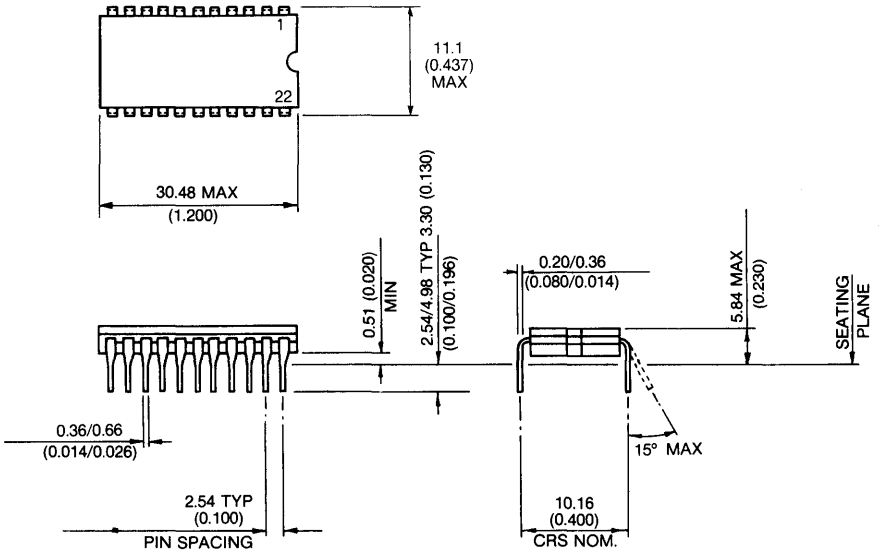
14 LEAD CERAMIC DIL
CERDIP - DG14



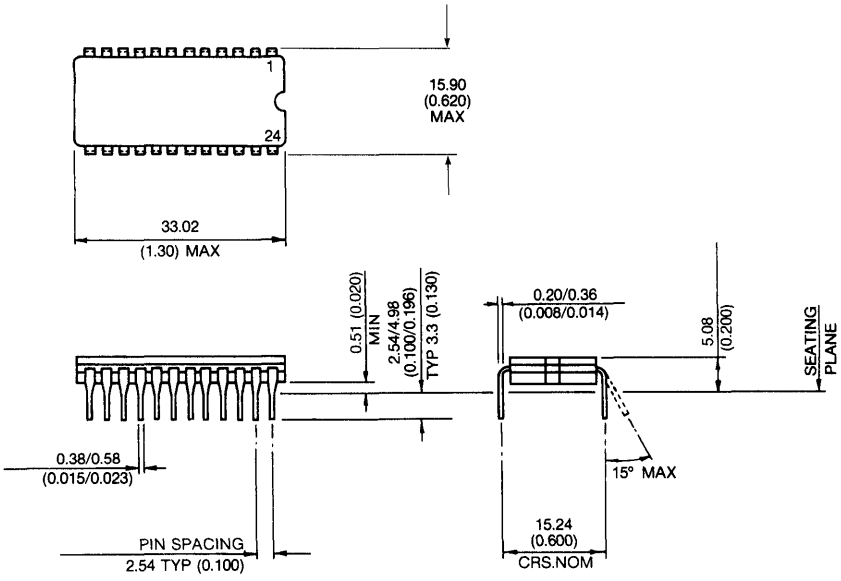
16 LEAD CERAMIC DIL
CERDIP-DG16



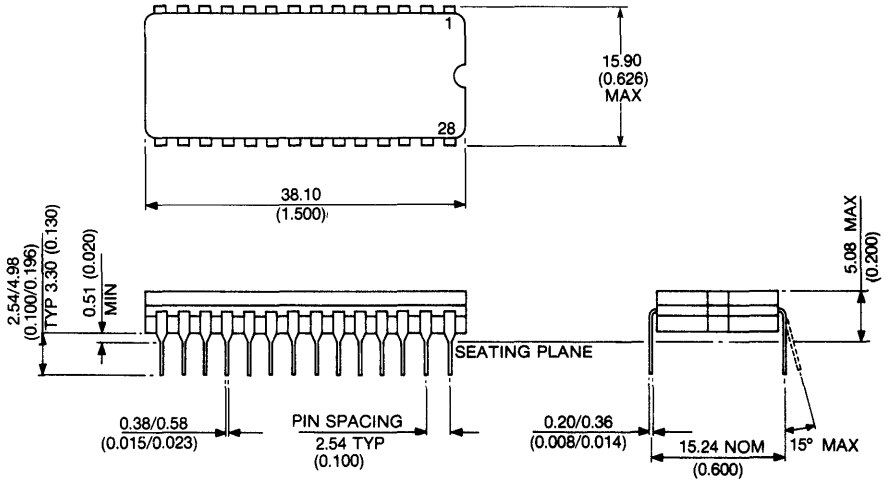
18 LEAD CERAMIC DIL
CERDIP - DG18



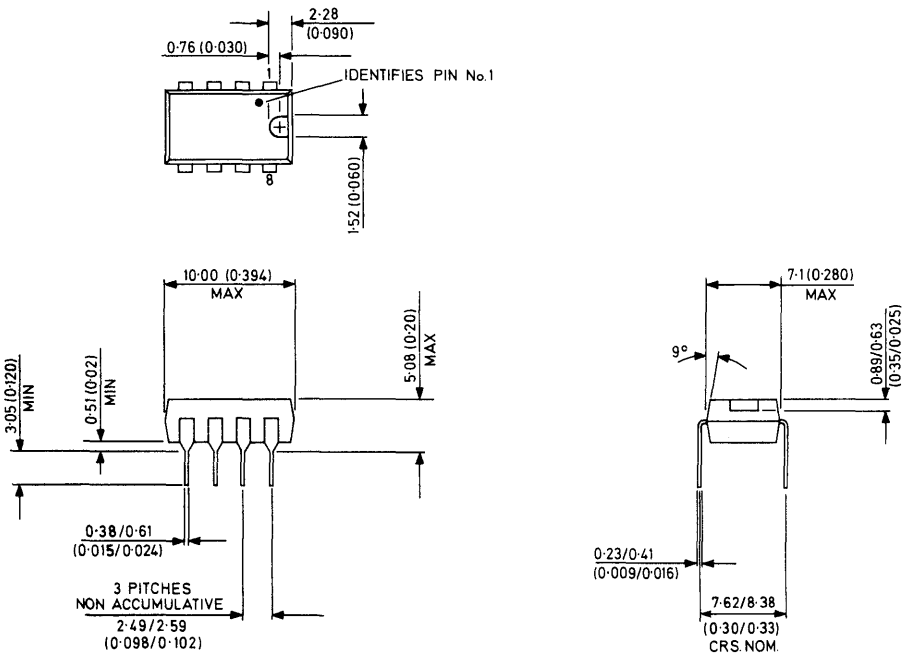
22 LEAD CERAMIC DIL
CERDIP - DG22



24 LEAD CERAMIC DIL
CERDIP - DG24



28 LEAD CERAMIC DIL - DG28



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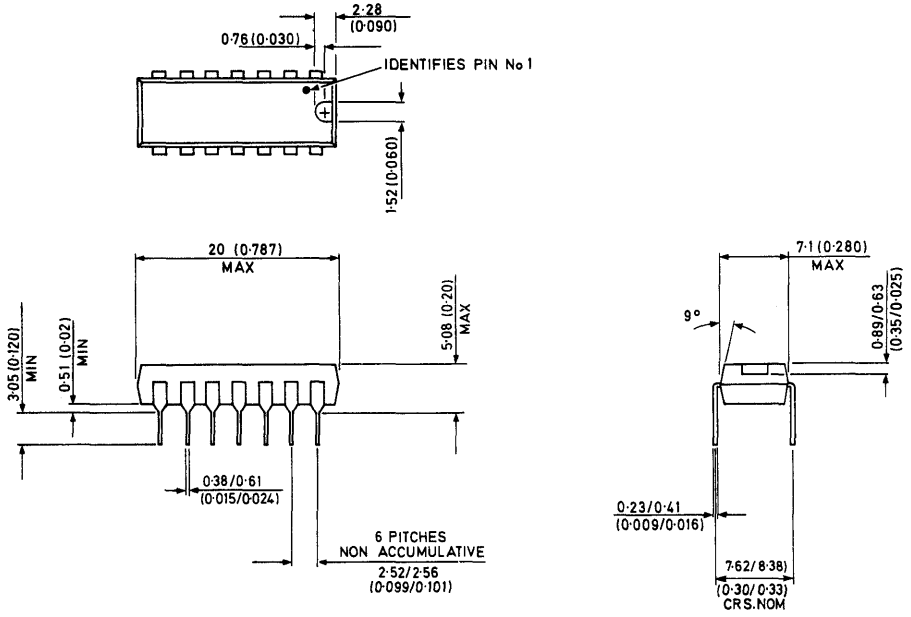

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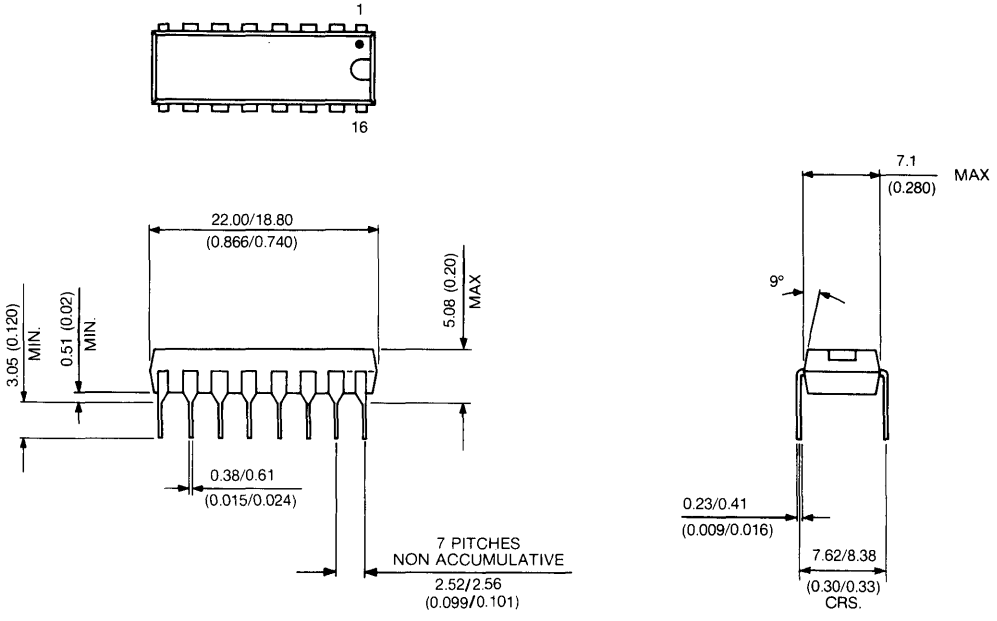

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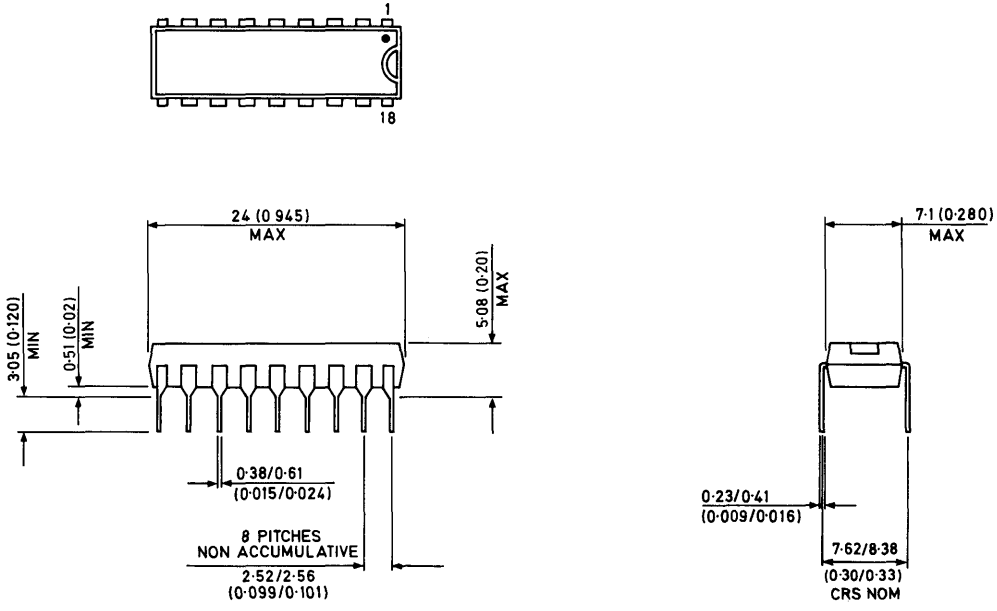

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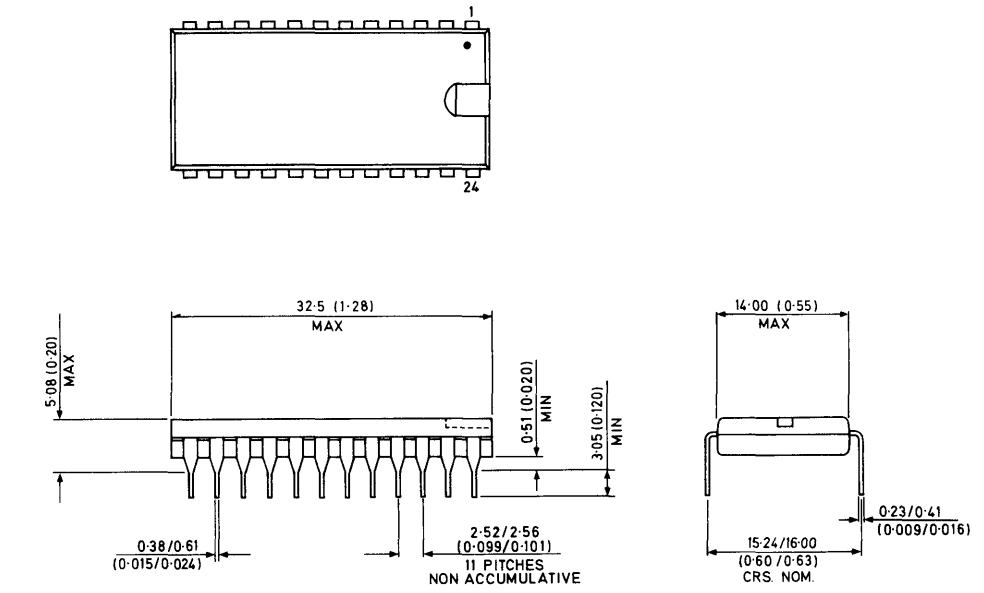
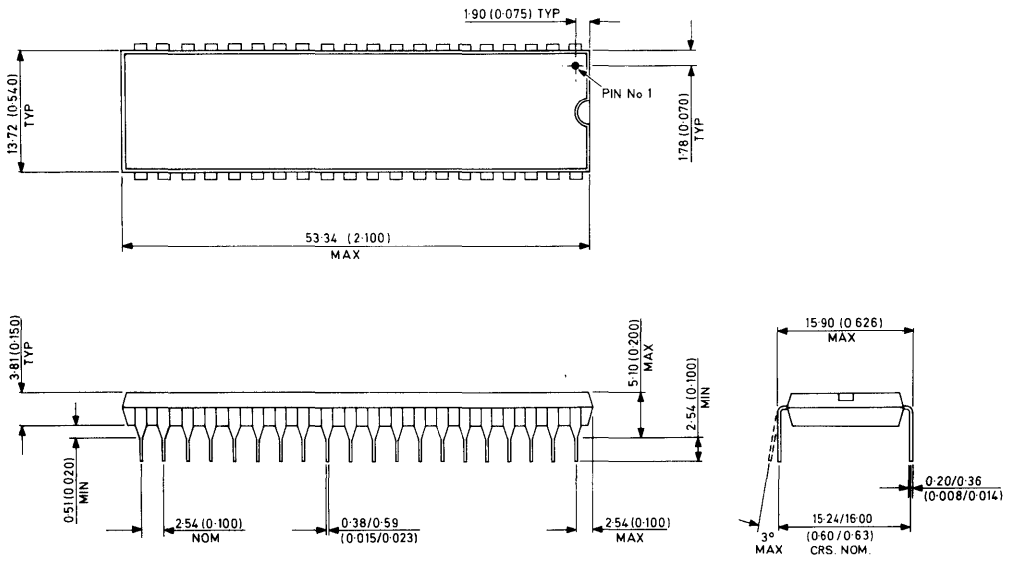


24 LEAD PLASTIC DIL - DP24



40 LEAD PLASTIC DIL - DP40

Ordering information

Plessey Semiconductor integrated circuits are allocated type numbers which take the following general form

WW XXXX Y/ZZ

where **WW** is a two-letter code identifying the product group and/or technology, **XXXX** is a three or four numeral code uniquely specifying the particular device, **Y** is a single letter which denotes the precise electrical or thermal specification for certain devices and **ZZ** is a two-letter code defining the package style. Digits **WW**, **XXXX** and **Y** must always be used when ordering; digits **ZZ** need only be used where a device is offered in more than one package style. For example, the **MV8863** is offered in **DG** (Ceramic dual-in-line) and **DP** (Plastic dual-in line) packages so the full ordering number for this device in ceramic DIL would be **MV8863/DG** and **MV8863/DP** for the plastic DIL version.

The Pro-Electron standard is used for package codes wherever possible. The two letters of this code have the following meanings:

FIRST LETTER (indicates general shape)

A Pin-Grid Array
C Cylindrical
D Dual-in-Line (DIL)
F Flat Pack (leads on two sides)
G Flat Pack (leads on four sides)
Q Quad-in-Line

M Miniature (for Small Outline)
L Leadless Chip Carrier — Not yet designated by Pro-Electron
H Leaded Chip Carrier

SECOND LETTER (indicates material)

C Metal-Ceramic (Metal Sealed)
G Glass-Ceramic (Glass Sealed)
M Metal
P Plastic
E Epoxy

Please Note:

Leadless Chip Carriers

LC Metal-Ceramic 3 Layer (Metal Sealed)
LG Glass-Sealed Ceramic
LE Epoxy-Sealed 1 Layer
LP Plastic

Note: The above information refers generally to Plessey Semiconductors integrated circuit products and does not necessarily apply to all the devices contained in this handbook.

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