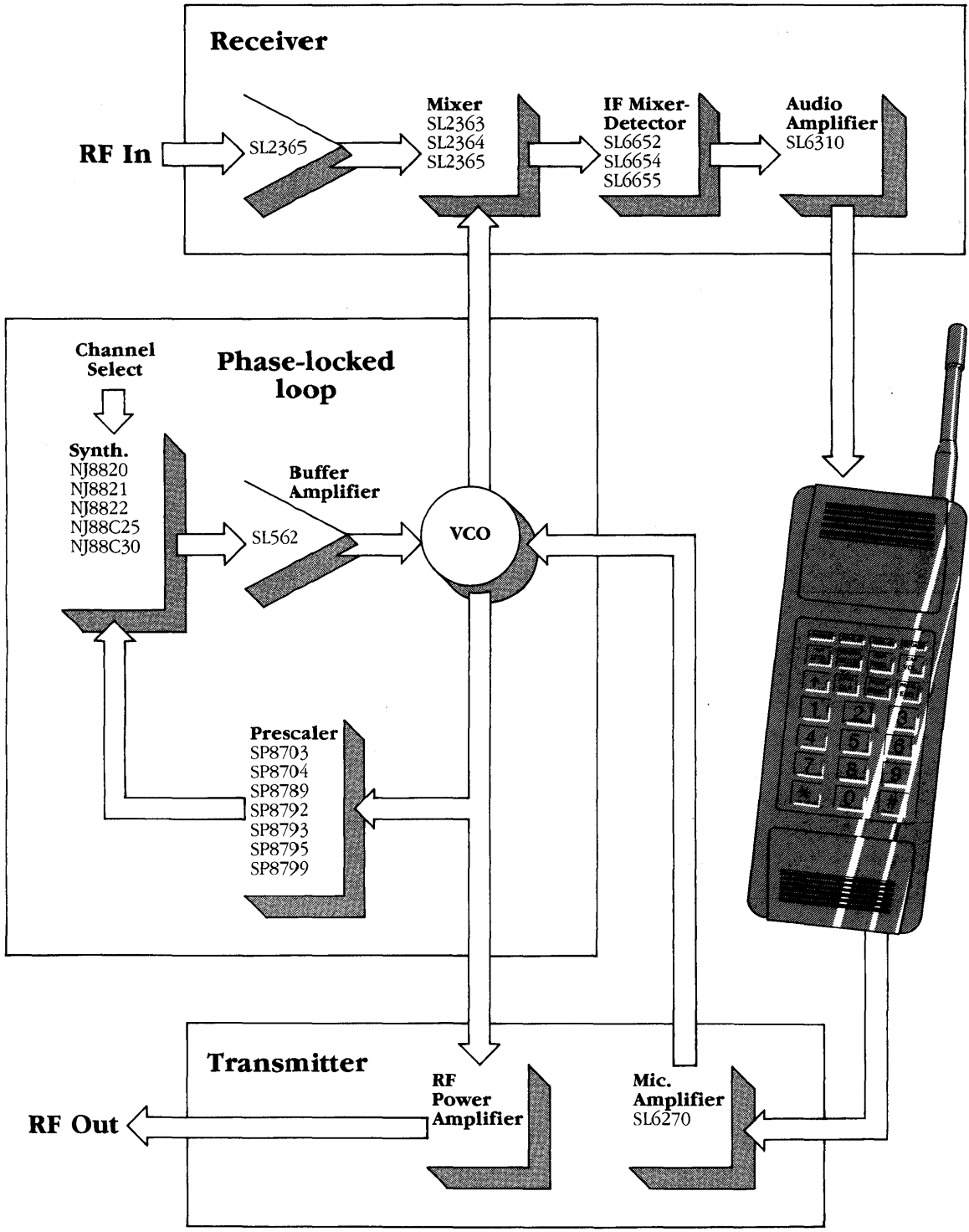
RADIO TELECOMS
IC Handbook

Plessey Semiconductors



Plessey products in a typical hand held radio.

RADIO TELECOMS
IC Handbook

PLESSEY
Semiconductors

Publication No. P.S.2123 March 1987

PWC 1864 3/87 30K

Contents

Foreword

Plessey Semiconductors has created a range of products specific to applications in the growing market for hand-held radio-telecommunications.

The features which identify ICs as being suitable for this market area are *supply current* and *frequency*. Since battery life is all-important in hand-held equipment, every effort is made by our IC designers to develop products which require the absolute minimum current. New ICs such as the SP8704 (a programmable two-modulus divider, which consumes only 10mA at 950MHz) exemplify this philosophy.

New frequency band allocations have now been made in the 450 and 900MHz regions for cordless telephones and cellular radios. Plessey's bipolar processes have been developed to operate at these and even higher frequencies for dividers, IF amplifiers and single chip synthesisers. The 2-Micron CMOS process is also capable of operating at high frequencies and the latest generation of CMOS synthesisers are included in this handbook.

Also making its debut is a range of new low power FM receivers. Suited for use in paging, the new ICs offer ideal solutions for Direct conversion or Superhet front ends.

All the relevant Plessey ICs can be supplied in surface mount miniature plastic and some in plastic quad packages in order to satisfy the requirement for small size in compact hand-held radio equipment.

Finally, the Quality Assurance Procedures that are applied to other Plessey Semiconductor products (from consumer electronics to Defence projects) are applied to Radio-Telecoms ICs with equal rigour. Performance and long term reliability are thereby guaranteed in what can be a demanding operating environment.

Product index - by application

Dividers

Ratio	Frequency (MHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
10/11	225	7	5.2 or 6.8 to 9.5	**SP8799**	81
20/21	225	7	5.2 or 6.8 to 9.5	**SP8789**	70
32/33	225	7	5.2 or 6.8 to 9.5	**SP8795**	77
40/41	225	7	5.2 or 6.8 to 9.5	**SP8793**	74
40/41	520	10.5	5.2	**SP8716**	67
64/65	950	10	3 to 5	**SP8704**	65
64/65	520	10.5	5.2	**SP8718**	67
80/81	225	7	5.2 or 6.8 to 9.5	**SP8792**	74
80/81	520	10.5	5.2	**SP8719**	67
128/129	950	10	3 to 5	**SP8704**	65
128/129	1000	30	5	**SP8703**	62

Synthesisers

Input Frequency (MHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
18	3.5	5	**NJ8820/1**	85-103
18	6.3	5	**NJ8822**	108
18		3 to 5	**NJ88C25**	113
125	4	5	**NJ88C31**	119
200	4	5	**NJ88C30**	114

Paging Receivers

Input Frequency (MHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
200	2.5	0.9 to 3.5	**SL6637**	27
100	1.0	0.9 to 7	**SL6655**	55

Product index - by application (contd.)

IF Amplifiers/Detectors

Input Frequency (MHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
100	1.5	2.5 to 7.5	**SL6652**[1]	36
100	1.5	2.5 to 7.5	**SL6653**[2]	44
100	1.5	2.5 to 7.5	**SL6654**[3]	49

1. With RSSI output and differential audio outputs. 2. Single audio output, no RSSI.
3. RSSI output, single audio output.

UHF Transistor Arrays

f_T (GHz)	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
5	4	2.0	**SL2363 & SL2364**[1]	18
5	4	2.0	**SL2365**[2]	20

1. 2 long-tailed pairs with tail transistors. 2. 2 long-tailed pairs with current mirrors.

Amplifiers

Function	Supply Current (mA)	Supply Voltage (V)	Type No.	Page
Audio	7.5	4.5 to 15	**SL6310**	24
Microphone	10	4.5 to 10	**SL6270**	21
Op-amp	20	±1.5 to ±10	**SL562**	15

Product index - by circuit type

Operational Amplifiers

Type No.	Supply Voltage (V)	Supply Current	Bandwidth	Maximum Offset Voltage (mV)	Gain (dB)	Page
SL562[1]	±1.5 to +10	20μA to 5mA	50kHz to 4MHz	5	95	15
SL6310	4.5 to 15V	7.5mA	100KHz	20	70	24

1. Noise figure 20nV/√Hz (Guaranteed).

Matched Transistors and Arrays

Type No.	LV_{CEO}(V) Min.	LV_{CEO}(V) Typ.	I_{CM}(mA)	Typ.Cut-off Frequency (GHz)	No. of Transistors	h_{FE} (I_C = 1mA) (Min.)	Page
SL2363[1]	6	9	12	5.0	6	20	15
SL2364[2]	6	9	12	5.0	6	20	15
SL2365[3]	6	9	12	5.0	8	20	18

1. TO-5 package (CM10). 2. DIL package (DC14, DP14). 3. Small outline plastic DIL package (MP14).

Radiocoms

Type No.	Function	Page
SL6270	Microphone amplifier with AGC	21
SL6652	FM IF and quadrature detector with RSSI and differential audio O/P	36
SL6653	FM IF and quadrature detector	44
SL6654	FM IF and quadrature detector with RSSI	49

Low Power Pagers

Type No.	Function	Page
SL6637	Direct conversion FSK receiver	27
SL6655	Superhet receiver consuming 1mA at 0.9V	55

Product index - by circuit type (contd.)

SP8000 Series Variable Modulus Dividers - Bipolar

Type No.	Function	Supply Current (Typ.) (mA)	Page
SP8703	1GHz ÷ 128/129	20	62
SP8704	950MHz ÷ 129/128/65/64	10	65
SP8716	520MHz ÷ 40/41	7	67
SP8718	520MHz ÷ 64/65	7	67
SP8719	520MHz ÷ 80/81	7	67
SP8789	225MHz ÷ 20/21	4	70
SP8792	225MHz ÷ 80/81	4	74
SP8793	225MHz ÷ 40/41	4	74
SP8795	225MHz ÷ 32/33	4	77
SP8799	225MHz ÷ 10/11	4	81

Radio Synthesisers

Type No.	Function	Page
NJ8820	CMOS control circuit with PROM interface	85
NJ8820/GG	Flatpack version of NJ8820	92
NJ8821	CMOS control circuit with microprocessor interface	98
NJ8821/GG	Flatpack version of NJ8821	103
NJ8822	CMOS control circuit with microprocessor serial interface	108
NJ88C25	CMOS control circuit with microprocessor serial interface operating down to 3V	113
NJ88C30	Single chip VHF synthesiser	114
NJ88C31	Single chip MF/VHF synthesiser	119

Product List

Semi-custom design

Only Plessey Semiconductors offers the system designer direct access to semi-custom design facilities from his own premises. Using Plessey proprietary licenced software, the customer can design his own CMOS gate array or cell-based PLESSEY MEGACELL™ systems in the easiest of ways and with the highest confidence of first-time success.

Faced with the need to get to market fast - for example, where product launch timescales have to be shortened to meet exhibition deadlines and competitors are in hot pursuit - gate arrays are often the first choice. Our deliveries can be very short, typically six weeks. Then, when your sales start to take off and you need to increase volume to match demand, your gate array can be very quickly converted to a silicon-efficient high-volume MEGACELL design.

This is because Plessey semi-custom software is not technology-dependent. Common design tools mean that a MEGACELL conversion can be rapidly committed to silicon, using a circuit description that contains the cells *you* have already specified.

Plessey Semiconductors semi-custom support group will offer guidance through all the stages of a design, advising you of the cost implications of varying complexities and package style configurations. Our design engineers will continue to support you on a 'one-to-one' level through our Design Review procedure.

After the circuit is jointly signed off, Plessey Semiconductors takes responsibility for the chip development and production test programmes. We normally supply ten fully-tested prototype circuits, guaranteeing performance to simulation.

A comprehensive 3-day training course is offered at your local Plessey Design Centre. The course gives personal tuition in all aspects of semi-custom design, including 'hands on' experience and the procedures are so straightforward that your engineers can be working on their own ASIC projects within those three days.

PLESSEY MEGACELL is a sophisticated ASIC design system, created by Plessey to make full use of both advanced semiconductor technology and the power of CAE *and* CAD. So, MEGACELL minimizes both design time and costs, and maximizes silicon usage, to give highly competitive product costs.

Unlike traditional cell-based methods, with MEGACELL the circuit designer can compile large cell structures such as memories, programmable logic array, and arithmetic logic units if his precise performance needs are not already met from the MEGACELL library.

Cell library

Four types of cell are available, allowing complete flexibility of design.

Microcells are SSI/MSI logic cells similar to those in current gate array and standard cell libraries;

Paracells provide user-definable memory and logic functions created from parameters set by the system designer;

Supracells are large fixed function cells which replicate - but more often improve upon - standard LSI functions;

Layout Cells or Macros, are more complex functions built up from Microcells.

The CLASSIC suite of design software has been developed by Plessey to specifications set by its own VLSI Design and Systems Engineers. They know what circuit designers need in a CAE/CAD system, and have made sure that the software can be used simply and easily by electronic design engineers. CLASSIC is very user-friendly, interfaces the major work stations, and can be addressed in plain language, and is extremely easy to learn.

Continuing development

Our on-going development programme includes design tools which will support emergent 1-micron bipolar and CMOS processes - together with Functional Modelling, Built-in Self-Test and Silicon Compilation.

The guiding principle throughout these developments remains, as it always has been - to make the transition from your initial thought to the finished silicon as simple as possible.

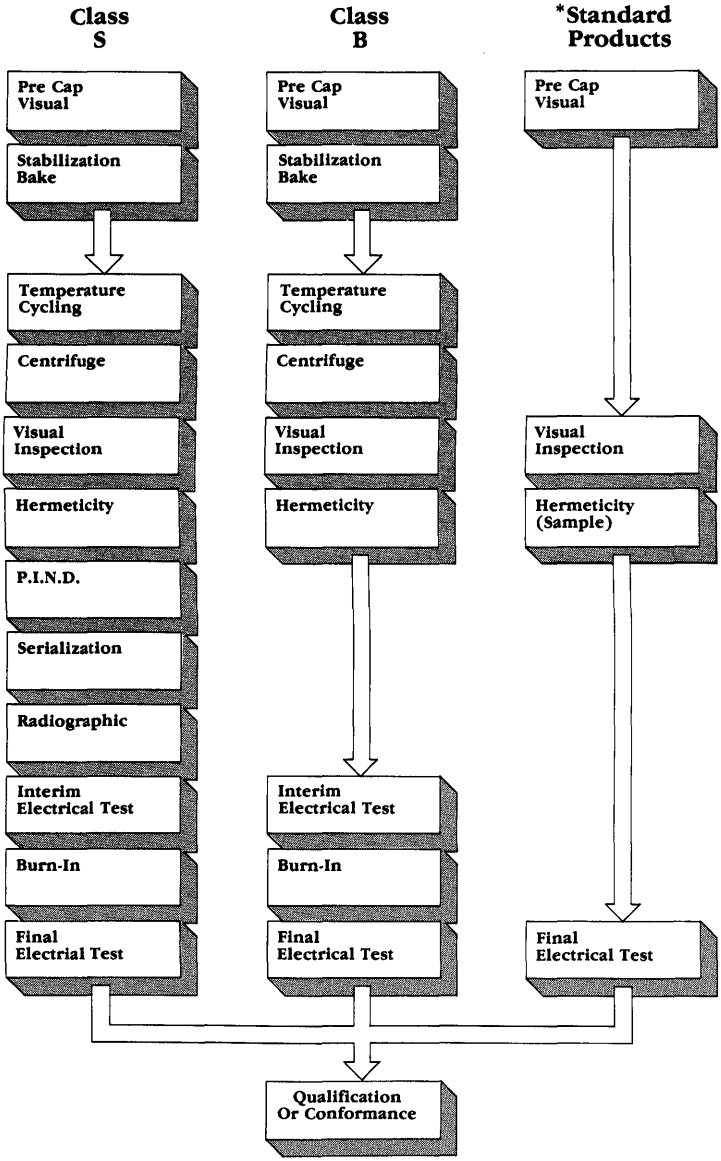
Microgate-C (SiGate CMOS) gate arrays

CLA 5000 SERIES	CLA 3000 SERIES
• Double layer metallisation • 2 micron channel length • Product family: CLA51XX 640 Gates CLA52XX 1232 Gates CLA53XX 2016 Gates CLA54XX 3060 Gates CLA55XX 4408 Gates CLA56XX 5984 Gates CLA57XX 7104 Gates CLA58XX 8064 Gates CLA59XX 10044 Gates • 1.2ns typ. prop delay • 40MHz system clock rate • 100MHz toggle rate • Fully auto-routed	• Double layer metallisation • 4 micron channel length • Product family: CLA31XX 840 Gates CLA33XX 1400 Gates CLA35XX 2400 Gates • 1.6ns typ. prop delay • 20MHz system clock rate • 40MHz toggle rate • Fully auto-routed

The Quality Concept

Screening

The following Screening Procedures are available from Plessey Semiconductors.



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes (followed by strict control and ongoing assessment) that quality products will be produced.

All designs conform to standard layout rules, all processes are thoroughly evaluated and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic procedures are used on all products up to and including device packing. It is only then that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures all users benefit; the high reliability user gains the advantage of scale hence improving the confidence factor in the quality achieved, whilst the volume user gains the benefits of basic high reliability design concepts.

Plessey Semiconductors have the following factory approvals:
BS9300 and **BS9400**
(BSI Approval No. 1053/M).
CECC50000 and **CECC90000**
(Reg. No. M/0020/CECC/UK-1053/M).
DEF-STAN 05-21
(DCL Reg. No. 1SB PO1).

Plessey Semiconductors conforms to **MIL-M-38510F** and is qualified to supply to **MIL-STD-883C**.

Technical Data

SL562

LOW NOISE PROGRAMMABLE OPERATIONAL AMPLIFIER

The SL562 is an advanced bipolar integrated circuit containing a single programmable operational amplifier. The amplifier can be programmed by current into a bias pin which determines the main characteristics of the amplifier's, supply current, frequency response and slew rate. With a suitable choice of bias current the SL562 can be used where low power and low noise characteristics are a necessity.

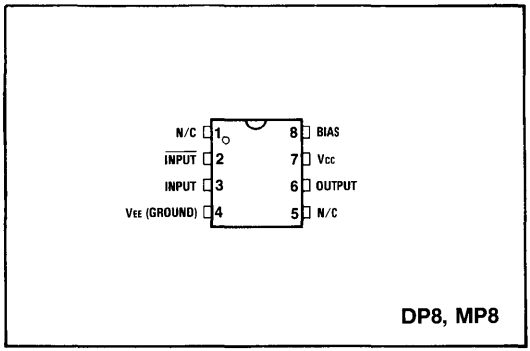


Fig.1 Pin connections - top view

FEATURES

- Low Noise Guaranteed (25nV/√Hz at 1kHz)
- Low Supply Current (40uA)
- Bias Conditions Adjustable to Optimise Performance
- Built In Short Circuit Protection
- Available In Small Outline

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers
- Frequency Synthesisers
- Hand Held Radio Applications

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±10V
- Supply Current ±40μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

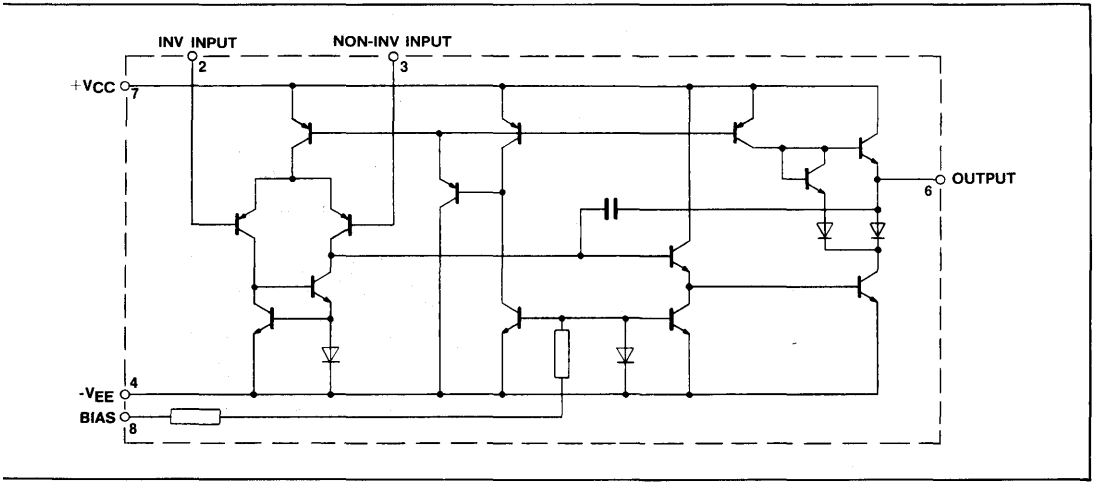


Fig.2 Circuit diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C
Operating mode A : Supply volts ±10V Bias set current 75μA
Operating mode B : Supply volts ±3.5V Bias set current 15μA
Operating mode C : Supply volts ±1.5V Bias set current 1μA

Characteristic	Operating mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	R_S = 10kΩ
Input offset current		20	190			150			49	nA	
Input bias current		250	800			350			95	nA	
Input resistance	0.1	0.6		0.2	0.5		0.3	2		MΩ	
Supply current	1000	1600	2200	50	200	1000	20	40	60	μA	
Large signal voltage gain	74	95		74	90		74	90		dB	R_L = 4kΩ(A) R_L = 100kΩ(B) R_L = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	R_S = 10kΩ
Common mode rejection ratio	70	110		70	85		70	82		dB	
Output voltage swing	8			1.5			0.7	0.8		±V	R_L = 4kΩ(A) R_L = 10kΩ(B) R_L = 4kΩ(C)
Supply voltage rejection ratio	74			85			85			dB	R_S = 10kΩ
Short circuit current	12		40				1	2.2		mA	T_{amb} = 0° C to +70° C
Gain bandwidth product		3.5			1			50		kHz MHz	Gain = 20dB
Slew rate		1.5			0.5			0.02		V/μs	Gain = 20dB
Input noise voltage		10	25		25	40		50	85	nV√Hz	fo = 1kHz
Input noise current		1.6			1.6			1.0		pA√Hz	f = 1kHz

OPERATING NOTES

Bias set current

The amplifier is programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02V/μs (I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{V_S - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

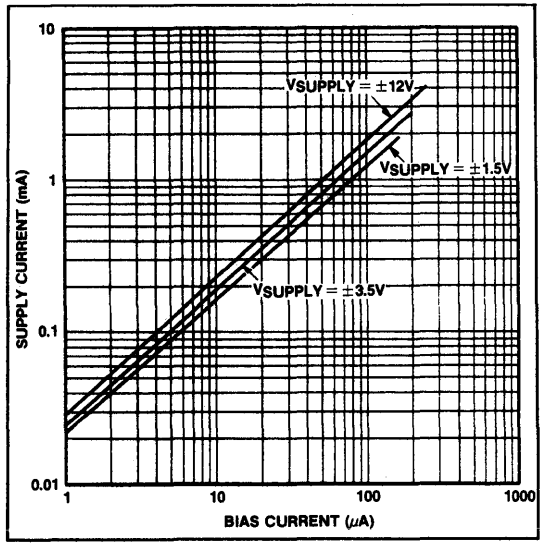


Fig.3 Supply current v. bias set current.

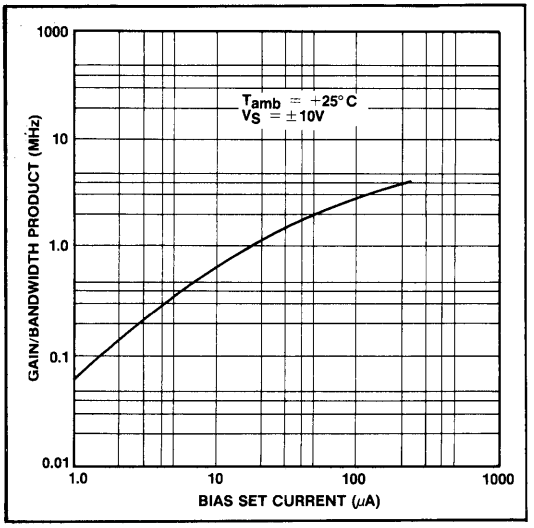


Fig.4 Gain bandwidth product v. ISET

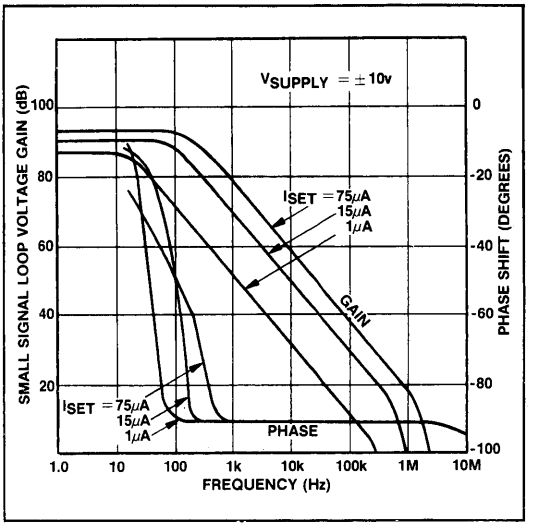


Fig. 5 Typical frequency response

APPLICATION EXAMPLE

The SL562 is especially suitable for use in loop filters for frequency synthesisers, the low noise and low power characteristics of the SL562 making it ideally suited for use with the Plessey low power frequency synthesiser circuits (NJ8820, SP87XX). All three integrated circuits are available in surface mounting packages, thus making a compact hybrid.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C
	Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

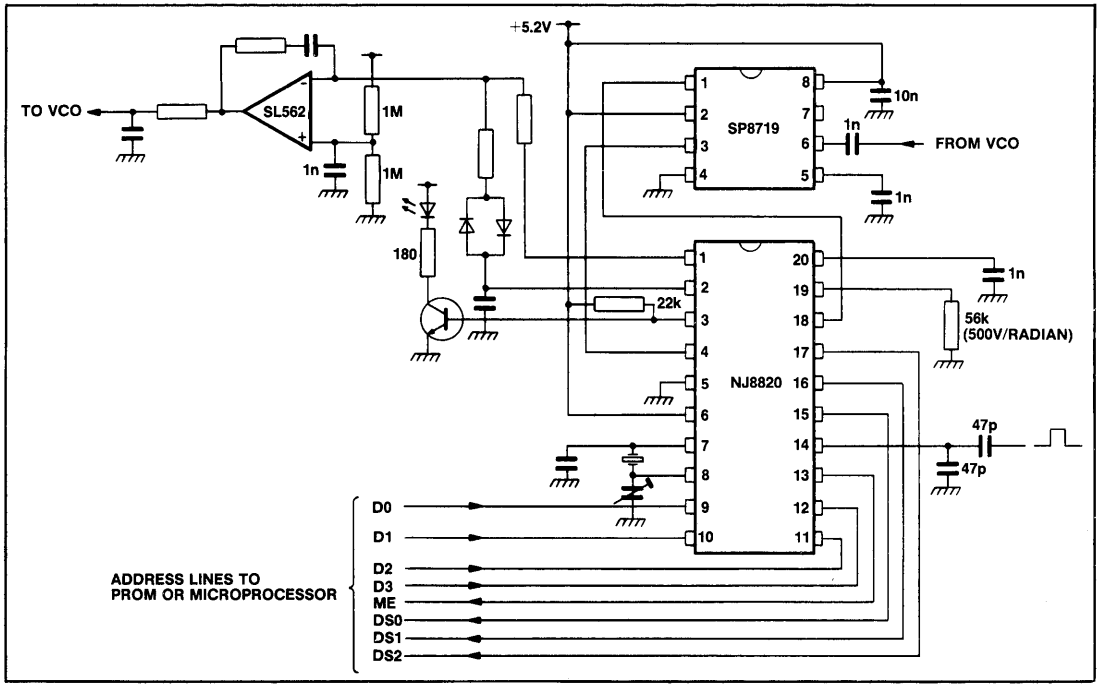


Fig.6 Application example.

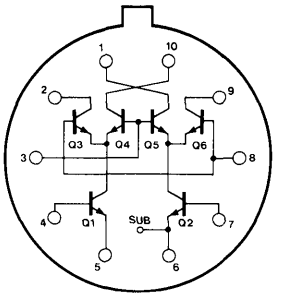
SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

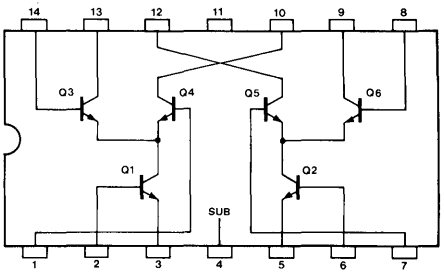
The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2363 is in a 10 lead TO5 encapsulation.

The SL2364 is in a 14 lead DIL plastic encapsulation and a high performance Dilmon encapsulation.



SL 2363C CM10



SL 2364C DC14 DP14

Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10μA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10μA
BV_{CIO}	16	40		V	I_C = 10μA
h_{FE}	20	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/°C	I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

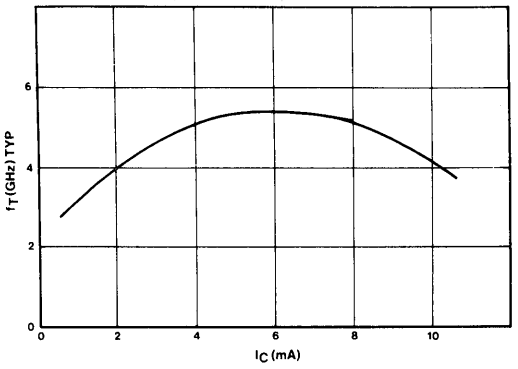


Fig. 2 Collector current

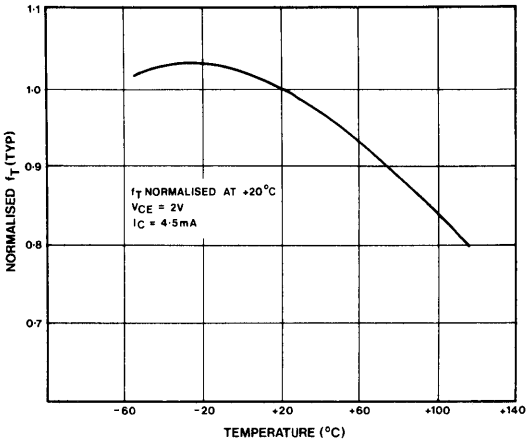


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature −55°C to +150°C
Maximum junction temperature +150°C
Package thermal resistance (°C/W):
Chip to case 65 (CM10)
Chip to ambient 225 (CM10) 175 (DP14)
V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

SL2365

VERY HIGH PERFORMANCE TRANSISTOR ARRAY

The SL2365 is an array of transistors internally connected to form a dual long-tail pair with current mirrors whose bases and collectors are connected internally. The ICs are manufactured on a very high speed bipolar process, which has a minimum usable f_T of 2.5GHz (typically 5GHz). The current mirror enables a well defined gain at low current levels to be achieved.

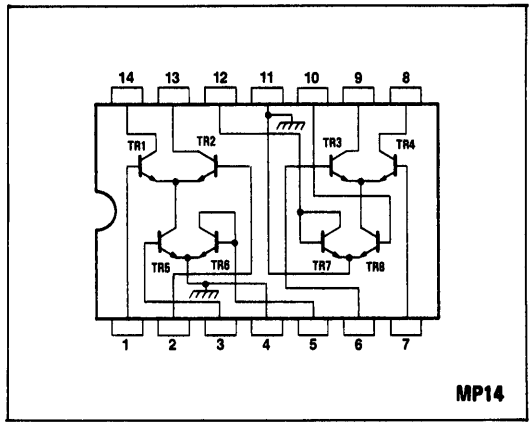


Fig.1 Pin connections - top view

FEATURES

- Complete Dual Long Tailed Pair in One Package
- Very High f_T - Typically 5GHz
- Well Defined Gain at Low Current Levels
- Available in Small Outline Package

ELECTRICAL CHARACTERISTICS

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{cbo}	10	20		V	$I_C = 10\mu A$
LV_{ceo}	6	9		V	$I_C = 5mA$
BV_{ebo}	2.5	5		V	$I_E = 10\mu A$
BV_{cio}	16	40		V	$I_C = 10\mu A$
H_{fe}	50	80			$I_C = 8mA$, $V_{ce} = 2V$
f_T	2.5	5		GHz	I_C (tail) $= 8mA$, $V_{ce} = 2V$
ΔV_{be}		2	5	mV	I_C (tail) $= 8mA$, $V_{ce} = 2V$
$\Delta V_{be}/T_{amb}$		-7		mV/°C	I_C (tail) $= 8mA$, $V_{ce} = 2V$
C_{CB}		0.5	0.8	pF	$V_{CB} = 0V$
C_{CI}		1.0	1.5	pF	$V_{CI} = 0V$

PLESSEY
Semiconductors

SL6270

GAIN CONTROLLED PREAMPLIFIER

The SL6270 is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 50dB range of input. The dynamic range, attack and decay times are controlled by external components.

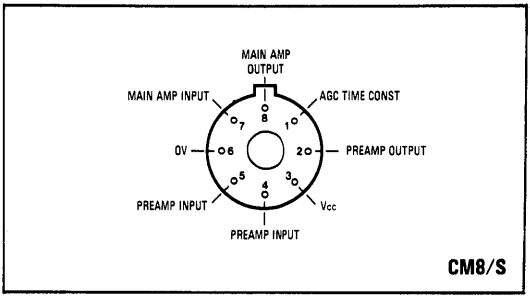


Fig.1 Pin connections, SL6270 - CM (bottom view)

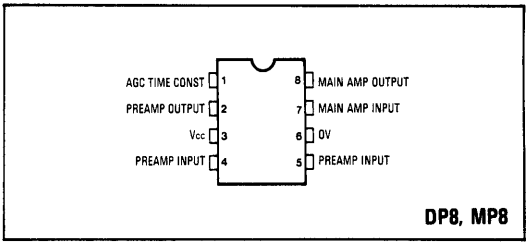


Fig.2 Pin connectons, SL6270 - DP (top view)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

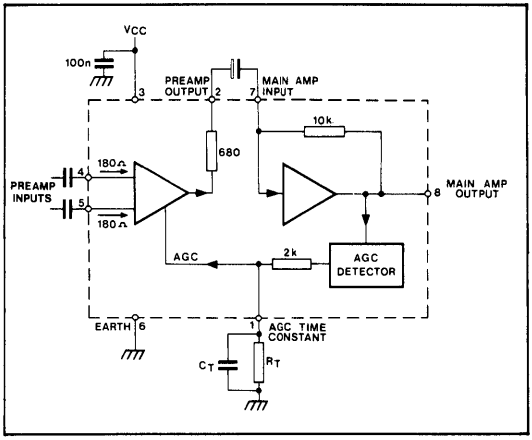
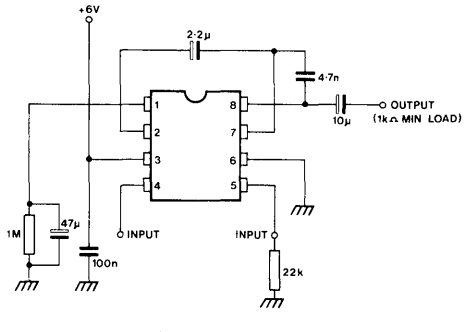


Fig.3 SL6270 block diagram

ELECTRICAL CHARACTERISTICS

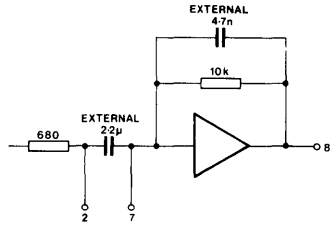
Test conditions (unless otherwise stated):
Supply voltage Vcc: 6V
Input signal frequency: 1kHz
Ambient temperature: −30°C to +85°C
Test circuit shown in Fig. 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential input impedance		300		Ω	
Voltage gain	40	52		dB	72μV rms input pin 4
Output level	55	90	140	mV rms	4mV rms input pin 4
THD		2	5	%	90mV rms input pin 4
Equivalent noise input voltage		1		μV	300Ω source, 400Hz to 25kHz bandwidth



N.B. If input not AC coupled the resistance between pins 4 and 5 must be less than 10 ohms.

Fig.4 SL6270 test and application circuit



$$\text{Voltage gain} = \frac{10k\Omega}{680\Omega}$$

Upper frequency response 10kΩ/4.7nF = 3kHz
Lower frequency response 680Ω/2.2μF = 300Hz

Fig.5 SL6270 frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270 may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270 is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a -3dB point at 300Hz, corresponding to 2.2μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270 has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and delay times

Normally the SL6270 is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig.4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

$$\text{Attack time} = 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

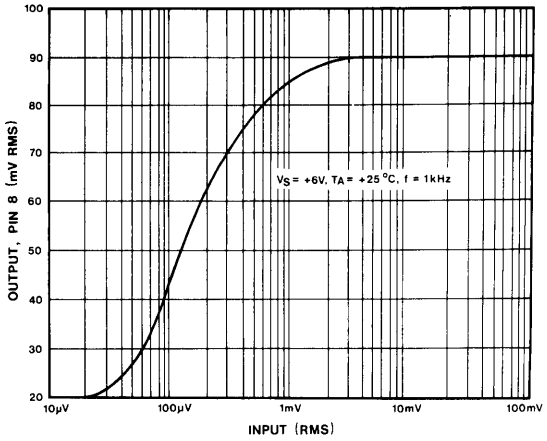


Fig. 6 Voltage gain (single ended input) (typical)

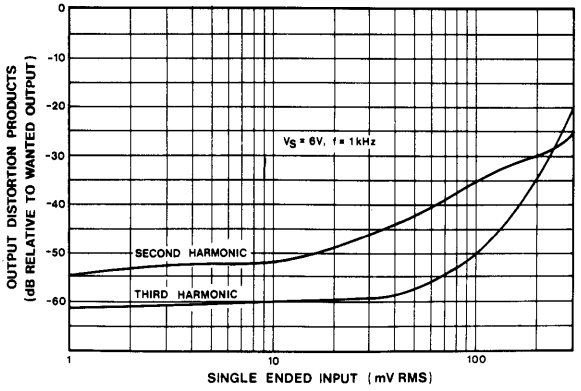


Fig. 7 Overload characteristics (typical)

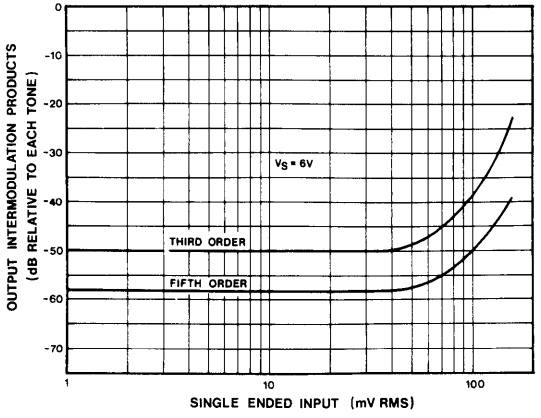


Fig. 8 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

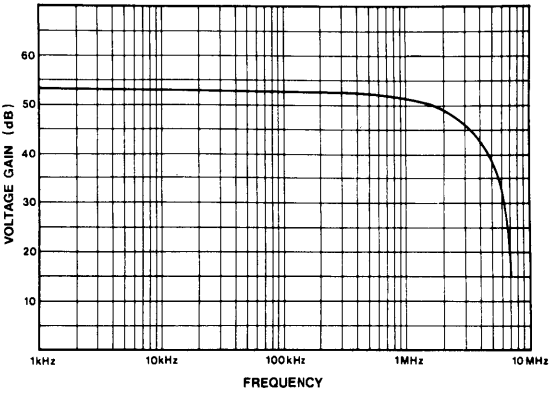


Fig. 9 Open loop frequency response (typical)

SL6310

SWITCHABLE AUDIO AMPLIFIER

The SL6310 is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

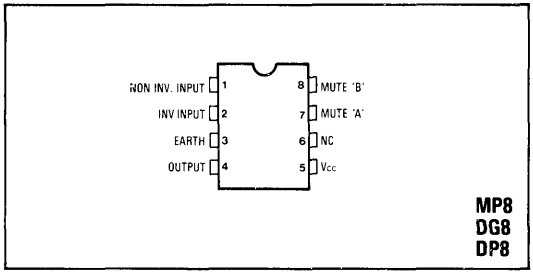


Fig.1 Pin connections SL6310 - (top view)

FEATURES

- Can be Muted with High or Low State Inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

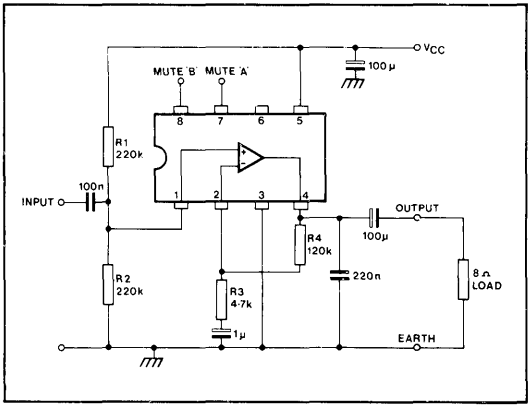


Fig.2 SL6310 test circuit

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 13.6V
- Voltage Gain: 70dB
- Output into 8Ω on 9V Supply: 400mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 15V
Storage temperature: −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage Vcc: 9V
Ambient temperature: −30°C to +85°C
Mute facility: Pins 7 and 8 open circuit frequency = 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current muted (A)		0.55	1	mA	Pin 7 via 100k to earth
Supply current muted (B)		0.6	0.9	mA	Pin 8 = Vcc
Input offset voltage		2	20	mV	Rs⩽10k
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	μA	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	Vcc = 4.5V
		10.6		V	Vcc = 13V
CMRR	40	60		dB	Rs⩽10k
Output power	400	500		mW	RL = 8Ω
THD		0.4	3	%	POUT = 400mW, Gain = 28dB

NOTE
1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage

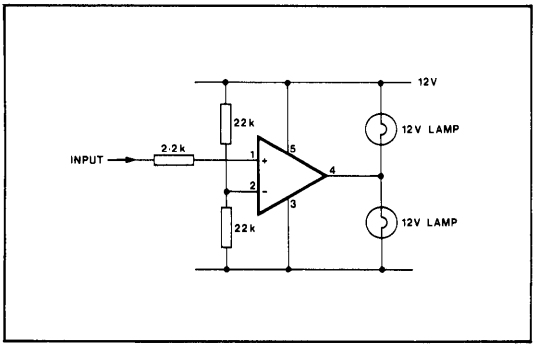


Fig.3 SL6310 lamp driver

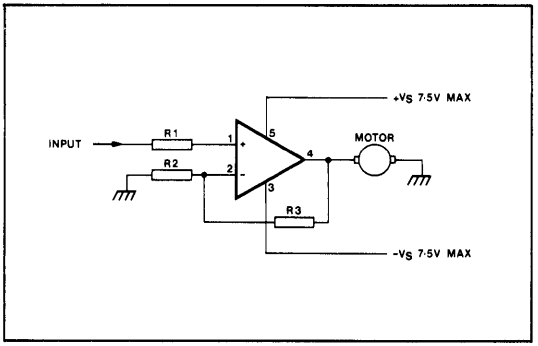


Fig.4 SL6310 servo amplifier

OPERATING NOTES

Mute facility

The SL6310 has twomute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within 0.65 volt of Vcc (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310 is muted.

Audio amplifier

As the SL6310 is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig.2. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

Operational amplifier

It is impossible to list all the application possibilities in a single data sheet but the SL6310 offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig.3) and servo amplifiers (Fig.4).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring high output current.

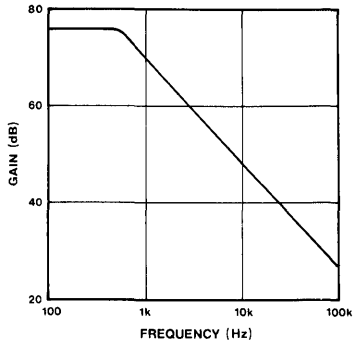


Fig.5 Gain v. frequency

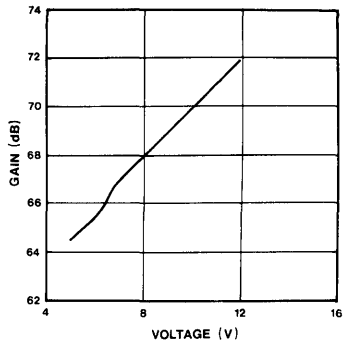


Fig.6 Gain v. supply voltage

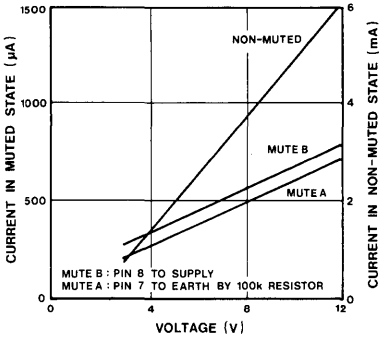


Fig.7 Supply current v. supply voltage

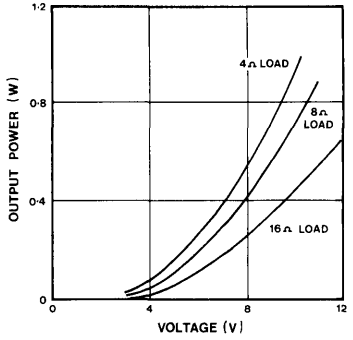


Fig.8 Output power v. supply voltage at 5% (max) distortion

SL6637

DIRECT CONVERSION FSK RECEIVER

The SL6637 is a lower power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capabilities of 'power down' for battery conservation and control of an external DC-DC converter if single cell operation is required. The device also comes equipped with high current beeper drive and low battery flag indicator.

FEATURES

- Very Low Power Operation - Typ. 4mW
- Single Cell Operation
- Complete Radio Receiver in One Package
- Operation Optimised at 200MHz
- 200nV Typical Sensitivity
- Operates at 1200 BPS

APPLICATIONS

- Low Power Radio Data Receiver
- Radio Paging
- Ultrasonic Direction Indication
- Security Systems

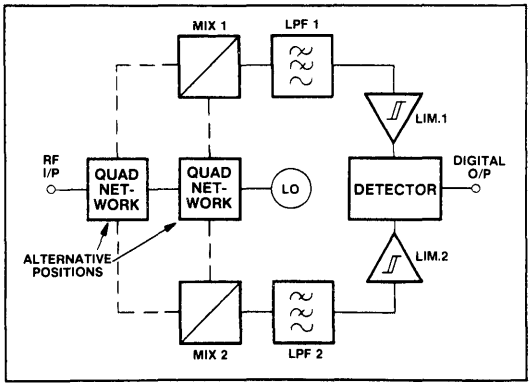
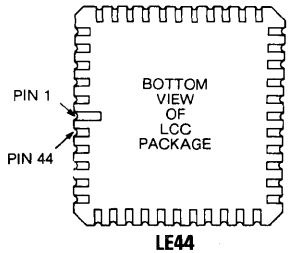


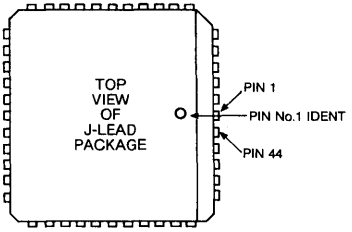
Fig.2 Block diagram

If the waveform at limiter '1' input leads the waveform at the limiter '2' input by 90°, output at the detector output will be a high level, and low at the Data Output.

If the waveform at limiter '1' input lags the waveform at the limiter '2' input by 90°, output at the detector output will be a low level and high at the Data Output.



LE44



HP44

PIN	FUNCTION	PIN	FUNCTION
1	Detector O/P	23	Mixer 1 O/P
2	BRF I/P	24	Power Down
3	BRF O/P Decoder I/P	25	Vcc2
4	LF Bias Decouple	26	Ground
5	Limiter '1' FB Decouple	27	Ground (Beep)
6	Limiter '1' I/P	28	Low Battery Control
7	Follower Filter O/P	29	Beep O/P
8	Follower Filter I/P	30	Beep Vcc1
9	Amplifier Filter O/P	31	Beep I/P
10	Amplifier Filter I/P	32	Mixer '2' RF I/P
11	Current Source Control (2)	33	Mixer '1' RF I/P
12	Current Source O/P (2)	34	Amplifier Filter I/P
13	Battery Flag	35	Amplifier Filter O/P
14	Osc.Current Source O/P(1)	36	Follower Filter I/P
15	Mixer '1' LO I/P	37	Follower Filter O/P
16	Mixer '2' LO I/P	38	RF Bias Decouple
17	Mixer Bias	39	RF Amplifier O/P
18	Inverter Control O/P	40	RF Ground
19	Reference O/P	41	RF I/P
20	Vcc1	42	Limiter '2' I/P
21	Inverter Control Threshold Adjust	43	Limiter '2' FB Decouple
22	Mixer 2 O/P	44	Decoder O/P

Fig.1 Pin connections

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency-converted to base band. The two paths are produced in phase quadrature (see Fig.2) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig.3. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig.3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency.

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states.

By applying the amplified outputs of the mixers to a phase discriminator, therefore, the digital data is reproduced.

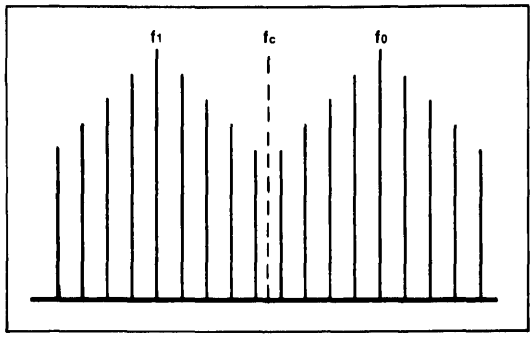


Fig.3 Spectrum diagram

ELECTRICAL CHARACTERISTICS (Use with test circuit Fig.4)

Test conditions: V_{CC1} = 1.3V V_{CC2} = 2.3V T_{amb} = -20°C to +60°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC1}	20	0.9		3.5	V	
Supply voltage V_{CC2}	25	1.8		3.5	V	
Supply current I_{CC1}	12,14,15, 16,17,20, 39	0.6	0.8	1.0	mA	Beep off Pin 11 unconnected
Supply current I_{CC2}	25	0.82	1.23	1.64	mA	
Powered-down I_{CC2}	25		7	15	µA	
RF amplifier						
Supply current (I_{RF})	39	400	500	650	µA	Pin 40 at 0V
Noise figure			5.5		dB	R_S = 50Ω
Oscillator						
Current source value (I_{OSC1})	14	200	250	350	µA	
Current source value (I_{OSC2})	12	220	270	370	µA	Pin 11 at 0V
Mixers						
Conversion gain		17	21	25	dB	10mV rms signal 10mV rms local oscillator
Input impedance	32,33		500		Ω	
Active filter	10,9					
Inverting amplifiers	34,35					
Input noise			20		nV/√Hz	
Open loop gain			40		dB	Tested as active filters
Input impedance			1		MΩ	using applications CCT
Output impedance			800		Ω	
Active filter	8,7					
Buffer amplifiers	36,37					
Gain			1		v/v	
Input impedance			20		kΩ	
Output impedance			1		kΩ	
Limiting amplifier						
Input impedance	6,42		50		kΩ	
Sensitivity	6,42		20	40	µV	Bit error of 1 in 30 5kHz deviation 500 bps

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Detector						
Output current	1		±5		μA	
Decoder						
Output mark-space ratio	44	7:9		9:7		40μV at limiter input
Output logic high	44	85			% V_{CC2}	
Output logic low	44			15	% V_{CC2}	
Battery economy	24					
Input current				1	μA	
Input logic high		1.5			V	Powered down
Input logic low				0.7	V	Powered up
Beeper driver						
Output saturation voltage	29			300	mV	I load = 50mA
Input current	31			1	μA	
Input logic high	31	1.5			V	Beep on
Input logic low	31			0.7	V	Beep off
Band-gap reference						
Output voltage	19	1.00	1.10	1.25	V	
Battery flag	13					
Output high level		85			% V_{CC2}	Battery high
Output low level				15	% V_{CC2}	Battery low
Flag trigger level		0.9		1.1	V	
Inverter control	18					
V_{CC2} voltage control level		2		2.4	V	Pin 21 unadjusted
Inverter output current			200		μA	Sourced from pin 18
Low battery control	28					
Input logic high		1.5			V	Removes beep drive if battery low
Input logic low				0.7	V	Connects beep drive
Input current				1	μA	

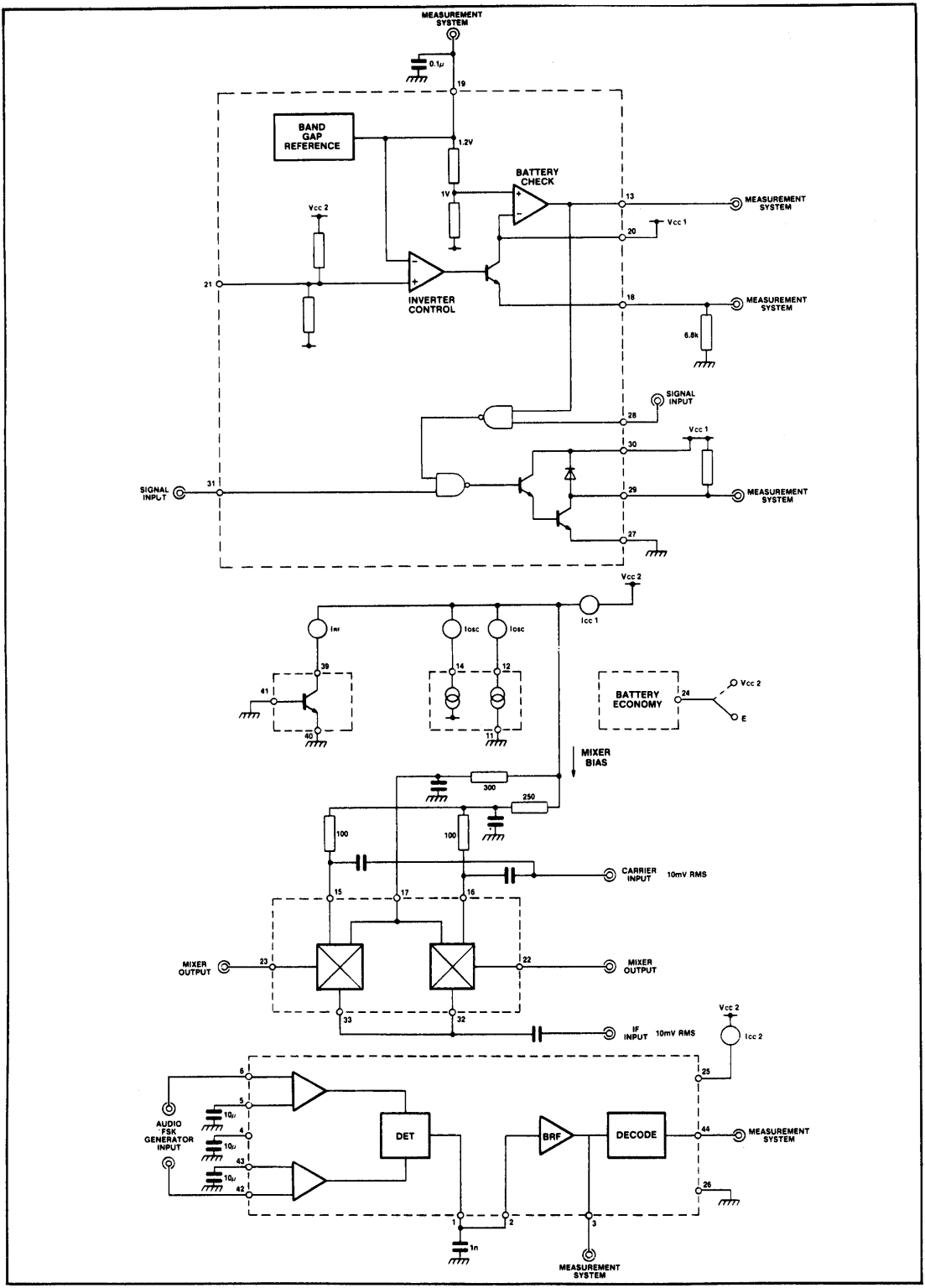


Fig.4 Test circuits

DETAILED DESCRIPTION

The schematic diagram of the SL6637 is shown in Fig.5. The various sub-sections will be described in more detail.

RF amplifier

The RF amplifier consists of a low noise transistor with a high f_t operating at a current of 500μA. It is arranged with a separate emitter connection to ensure stability, and to minimise noise introduction through common return impedances. The collector of this stage is uncommitted for maximum flexibility (transistor c, b, e on pins 39, 41 and 40 respectively) and is biased from a current mirror. The power-down circuitry removes bias from this stage in the standby condition. Typical parameters for this transistor are $\beta \simeq 100$, $rbb' \simeq 100\Omega$ and $f_t \simeq 1.2$GHz.

Mixers

The mixers are single balanced active mixers using a PNP current mirror as an active load. Inputs to the mixer are on pins 33 and 32 for the signal, and pins 15 and 16 for the LO. Pin 17 is the LO injection common point and may either be a common but 'live' point when the phase quadrature is used in the RF path or bypassed when quadrature LO drive to the mixers is employed. Emitter follower outputs on pins 23 and 22 ensure that mixer gain is unaffected by the load impedance. The mixers are also powered down on standby.

Local oscillator

A current source on pin 14 and a switchable current source on pin 12 are available for use in a local oscillator.

Inverting amplifiers

The inverting amplifiers have high gain (40dB open loop) and are for use in active low pass filters. The open loop gain is high and is not defined with any accuracy, as closed loop gain is defined by the external filter components.

Buffers

The buffer stages are x1 amplifiers for use in the active low pass filters.

Limiting amplifiers and detectors

These amplifiers provide the main gain block of the receiver system. An input of about 6μV provides limiting, and the inputs are to pins 6 and 42. Pins 4, 5 and 43 are bypass points for the amplifier bias points, while pin 1 is the digital output from the phase detector.

Bit rate filter

The bit rate filter provides a x1 buffer followed by a limiting amplifier. Its function is to act as a low pass filter to the modulation frequency, and may be configured as an active LPF if desired. It should however, be designed as a very high impedance active LPF as the drive from the detectors is at a high impedance. Alternatively, the connection of a small capacitor to ground from the input is generally adequate for most applications.

Beeper drive

The beeper drive stage accepts an input from an external source and provides a high current drive to the beeper. This current drive can be as high as 200mA, and the arrangement is such that the output waveform may be modified when the battery is near end of life. This modified waveform is generated externally (and applied to pin 28). The internal band gap reference is 1.2V and this is divided down to a suitable voltage.

Inverter control

This output is available (on pin 18) to control an external inverter. It is derived from the ratio of the internal reference to the V_{CC2} line, and moves in phase with changes in the V_{CC2} line.

Pin 21 allows the value of the inverted voltage supply to be adjusted.

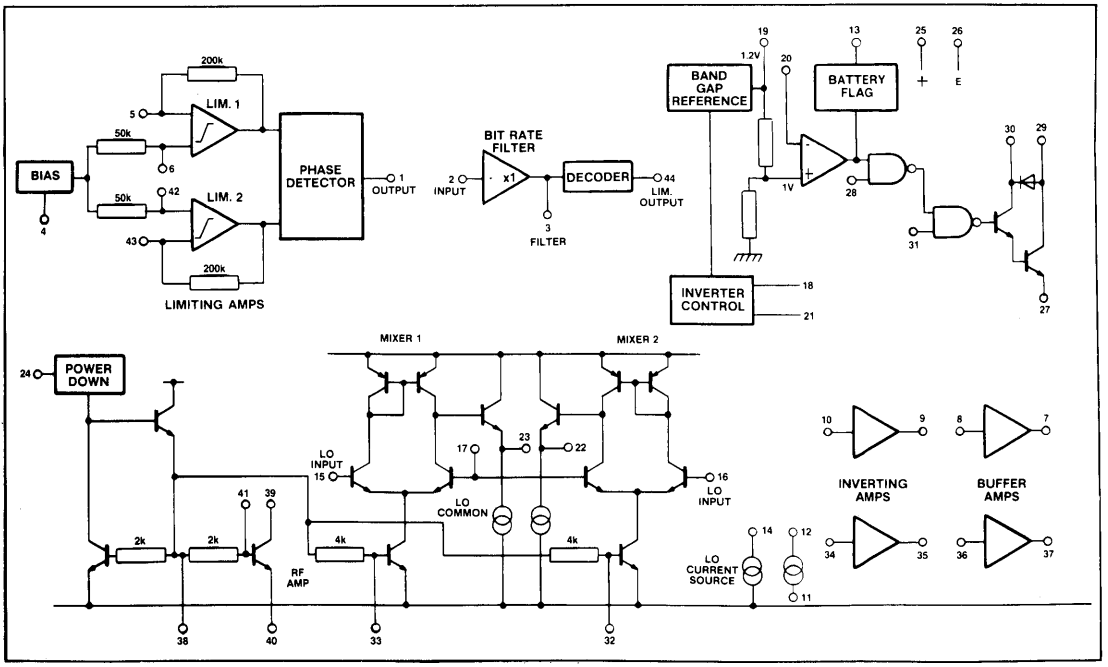


Fig.5 SL6637 schematic diagram

APPLICATIONS

The SL6637 is intended for applications at a low data rate and high deviation (e.g. 512 bits per sec. and ±4.5kHz deviation). Operation at a ratio of deviation to data rate of less than 6 is not recommended.

The choice of circuitry is dependent upon the system requirements. For example, operation from a single Leclanche or alkaline cell at a nominal 1.4V requires the use of an external inverter, while operation from a single 3 volt Lithium cell does not.

In the radio receiver application, a major decision is the positioning of the quadrature phase shift network. This network may be in the RF or the local oscillator paths, and each method has its advantages and disadvantages. Briefly, these are as follows:

1. **Local oscillator path.** This enables minimum RF loss to be attained. It requires a higher LO drive power to overcome the inevitable losses in the phasing network.
2. **RF signal path.** This method has the advantage that greater isolation may be achieved from the signal to the local oscillator - see Fig.6.

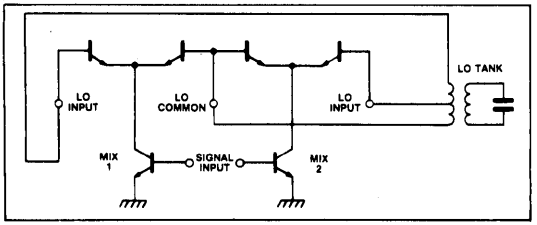


Fig.6 Local oscillator drive

The common mode rejection of the differential stages is used to its maximum advantage in this arrangement.

The form of the quadrature network is not critical. However, the use of an RC network as in Fig.7 has the disadvantage at VHF of being more subject to stray capacities than other methods.

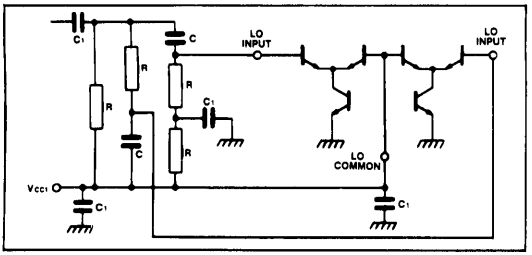


Fig.7 Quadrature LO drive

In the circuit of Fig.7, C_1 is a bypass capacitor, while $X_C = R$ at the operating frequency. Note that the resistances between the local oscillator inputs are equal to minimise DC offsets. The quadrature network can be achieved by coupled circuits (Fig.8) or a hybrid network (Fig.10).

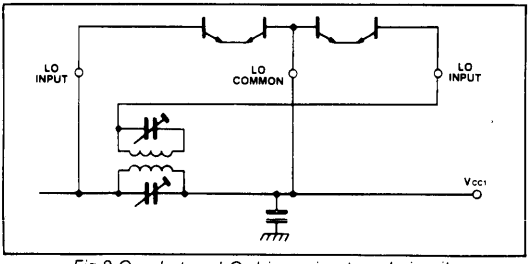


Fig.8 Quadrature LO drive using tuned circuits

In the method shown in Fig.8, the tuned circuits are adjusted to resonance, and are then detuned, one HF and the other LF, to achieve a 3dB drop in output from each one. This gives a +45° and -45° relative phase shift.

The quadrature hybrid network is well covered in the literature and is shown in Fig.9.

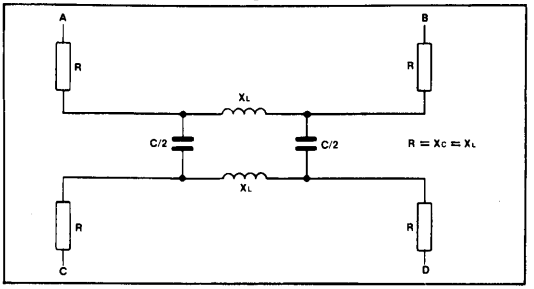


Fig.9 3dB quadrature coupler

The phase relationships are (A) input, (B) 90°, (C) 0° and (D) isolated. The circuit of Fig.10 may be used.

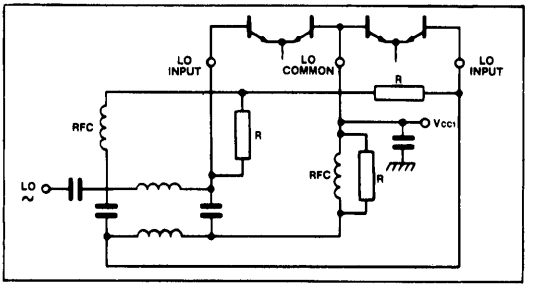


Fig.10

With a suitable local oscillator design some simplification occurs. In addition, it is possible to omit the resistors terminating the hybrid junction, although some mismatch then occurs.

Local oscillator

Because of the wide frequency range over which the SL6637 will operate, it is not possible to define which oscillator to use. Because of this, the oscillator provision is two uncommitted current sources which allows maximum flexibility. A typical overtone oscillator is shown in Fig.11.

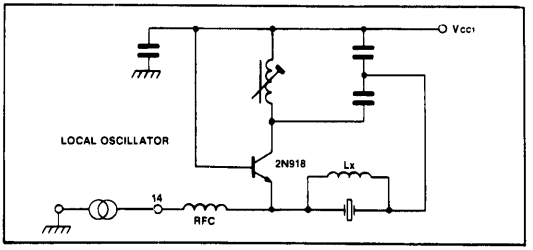


Fig.11 Typical overtone oscillator circuit

Lx is necessary with higher order overtone crystals to suppress oscillation at either the fundamental crystal frequency or as a form of Colpitts with no relation to the crystal frequency.

For lower frequencies, a simple oscillator may well be adequate as shown in Fig.12.

The choice of oscillator and quadrature network are dependent upon the application and no hard and fast rules can be formulated.

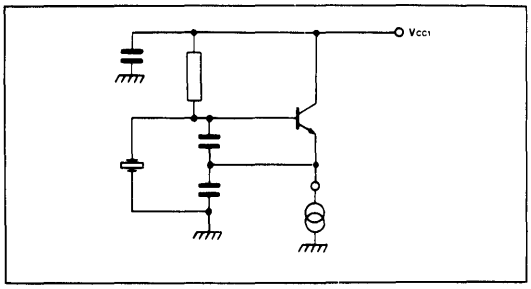


Fig.12 Fundamental LO circuit

Active filters

In any direct conversion receiver, the active filters provide the primary receiver selectively. The attenuation on the adjacent channel must be sufficient to prevent the limiting amplifiers from being driven into limiting by the unwanted signal; provided that this does not occur, then an adjacent channel signal has no effect.

The filter amplifiers consist of two stages for each channel, viz:

(a) An inverting amplifier with an open loop gain of about 40dB, and a gain-bandwidth product of 50kHz.

(b) A buffer stage with a x1 non-inverting gain.

Any of the standard variations of low pass filter can be used; however, design should ensure that differential group delay between the maximum possible error in mark and space frequencies is not excessive. The error in mark and space frequencies is caused by errors in the LO and received frequencies; an error in these frequencies leads to mark and space conditions producing different frequencies, and it is the differential group delay between these frequencies that must be minimised. This is especially important at data rates which are high in comparision with the deviation i.e. low values of modulation index m.

Bit rate filter

The bit rate filter consists of a x1 buffer amplifier and a limiting or 'decoder' stage. The buffer amplifier may be connected as an active filter: it should however be a group delay equalised ('linear phase') filter, and the input capacity should be minimised, as it is driven from a high impedance at the output of the detectors. It is perfectly satisfactory, however, to connect a 1000pF capacitor from the detector output to ground for bit rates up to 512 bits per second.

Beeper drive

This output has a high current drive capability, suitable for driving beepers in pagers, or as a relay driver in other applications (Fig.13).

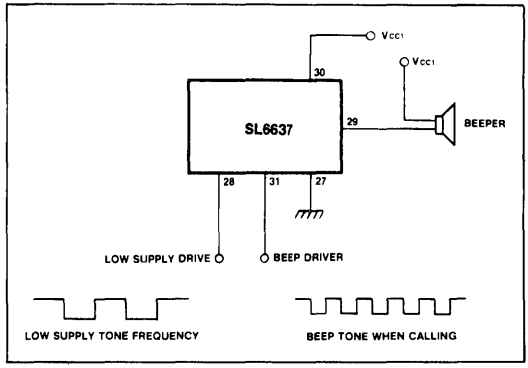


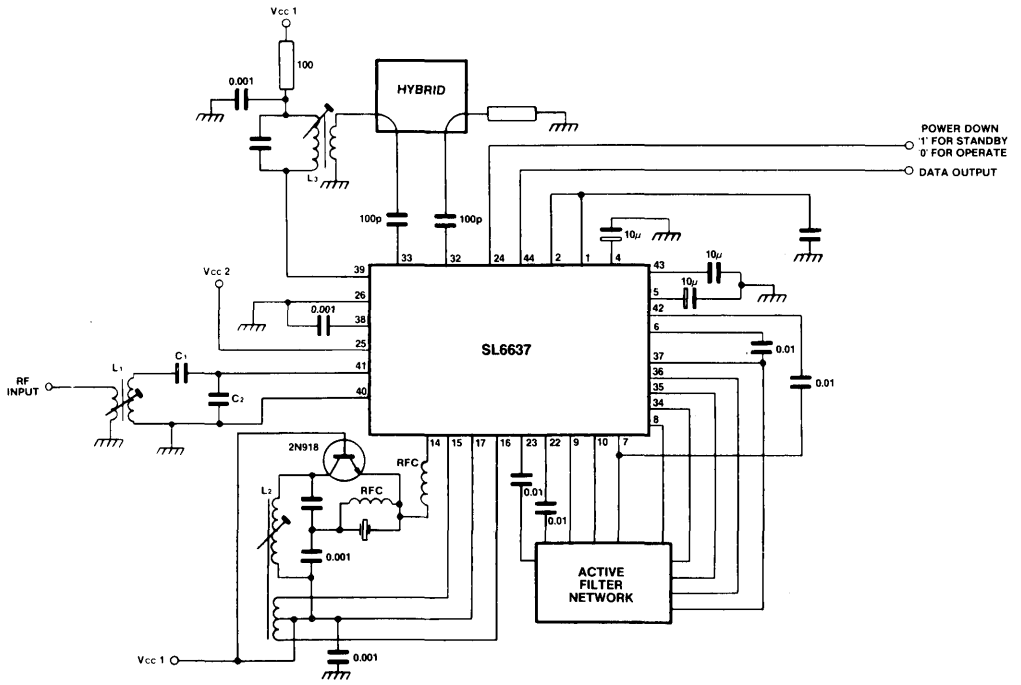
Fig.13 Beeper drive circuit

An internal diode connects pin 29 to pin 30 to protect the driver transistor when used with inductive loads.

The circuit allows for a modification of the beep output when the battery flag has operated. The low battery control pin 28 has no effect whilst the battery is high. When the battery is low pin 28 will override the beep input, a logic high will remove beep drive and a logic low will connect beep drive. Therefore wiring pin 28 high will stop the beeper when the battery is flat, while wiring a logic low on pin 28 will cause the beeper to ignore the battery flag. Putting a low frequency on pin 28 will modulate the beep tone giving a warbling effect when the battery is flat.

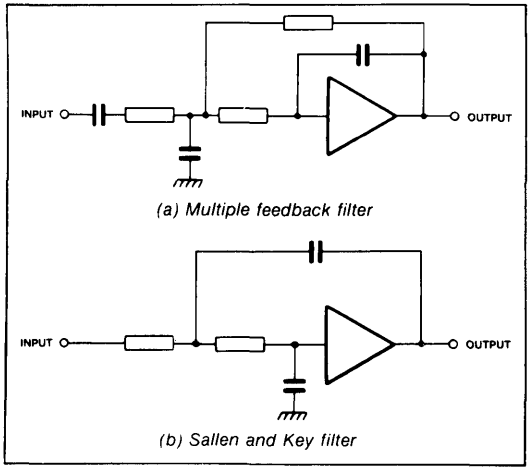
Typical application

Fig.14 shows a typical application as an FSK receiver for 512bps with a frequency deviation of ±4.5kHz. Typical sensitivity is of the order of 0.2μV for a 1 in 30 ber (bit error rate). The circuit as shown in Fig.13 uses a 9th overtone crystal and is usable to approximately 180MHz.



NOTES
Circuits L_1, C_1, C_2, L_2, L_3, resonate at the operating frequency. RFC1 suppresses oscillation at the crystal fundamental. RF level at pins 15 and 16 should be 10-20mV rms. For active filter network design, see Fig.15.

Fig.14 Typical application



(a) Multiple feedback filter

(b) Sallen and Key filter

Fig.15 Active filters. Component values may be determined from the standard books on active filter design.

The RF level at pins 15 and 16 can be increased which will increase the gain, but care must be taken with re-radiation from the input.

Operation at higher or lower frequencies is possible with appropriate external components.

USE OF SL6637 FROM ONE SUPPLY

For minimum power dissipation the SL6637 should be used with one cell (V_{CC1}) and an inverter (V_{CC2}). To operate from just one supply (Vc) certain precautions need to be taken.

Pin 25 will now be connected to Vc. Pins 12,14,39 can be returned to Vc through the same components as for two supply operation. Pins 15,16,17 are normally biased from V_{CC1} and cannot be connected directly to Vc. One diode volt drop down from the supply Vc is usually sufficient,see Fig.16.

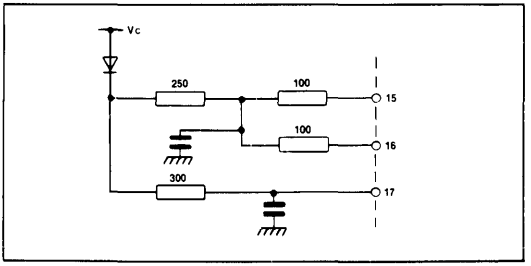


Fig.16

Pin 20 is usually connected to V_{CC1} when it is used to supply current to the inverter circuit and as an input to the battery check. For single voltage operation the inverter will not be required therefore pin 18 can be wired to Vc to disable the inverter. Pin 20 can still be used as a battery check by potting down the supply to pin 20, see Fig.17.

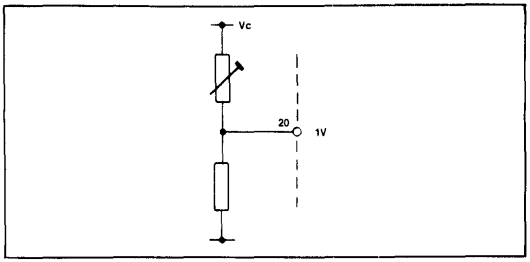


Fig.17

Pins 29,30 of the beeper driver are normally connected to V_{CC1}. These can be connected to Vc but the driver to the output transistor may then be excessive in any particular application. To reduce the drive a resistor may be included from pin 30 to Vc, see Fig.18.

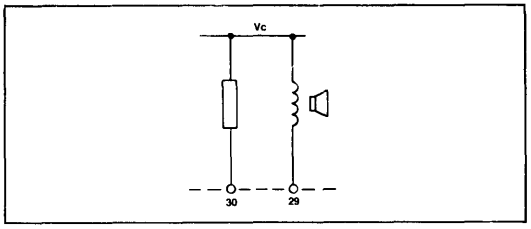


Fig.18

BATTERY ECONOMY

Function	Battery economised
RF amplifier	Yes
Osc current sources	Yes
Mixers	Yes
Active filters	Yes
Limiting amplifiers	No
Phase detector	Yes
Bit-rate filter	Yes
Decoder	Yes
Band-gap reference	No
Battery check/flag	No
Inverter control	No
Low battery control	No
Beeper driver	No

Functions that are economised above will have their bias removed during power-down. Functions that are not economised will not be affected during power-down.

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	5V max.
Current (Beep Output):	200mA max. (50% duty cycle max.)
(Any other pin):	5mA max.
Operating temperature:	-20°C to +85°C
Storage temperature:	-20°C to +85°C

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SL6652

LOW POWER IF/AF CIRCUIT FOR FM CELLULAR RADIO

The SL6652 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB

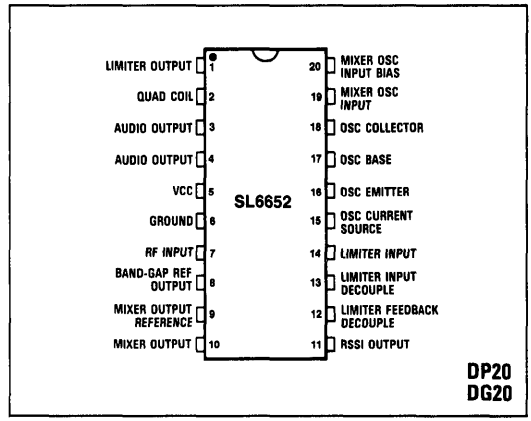

Fig.1 Pin connections (top view)

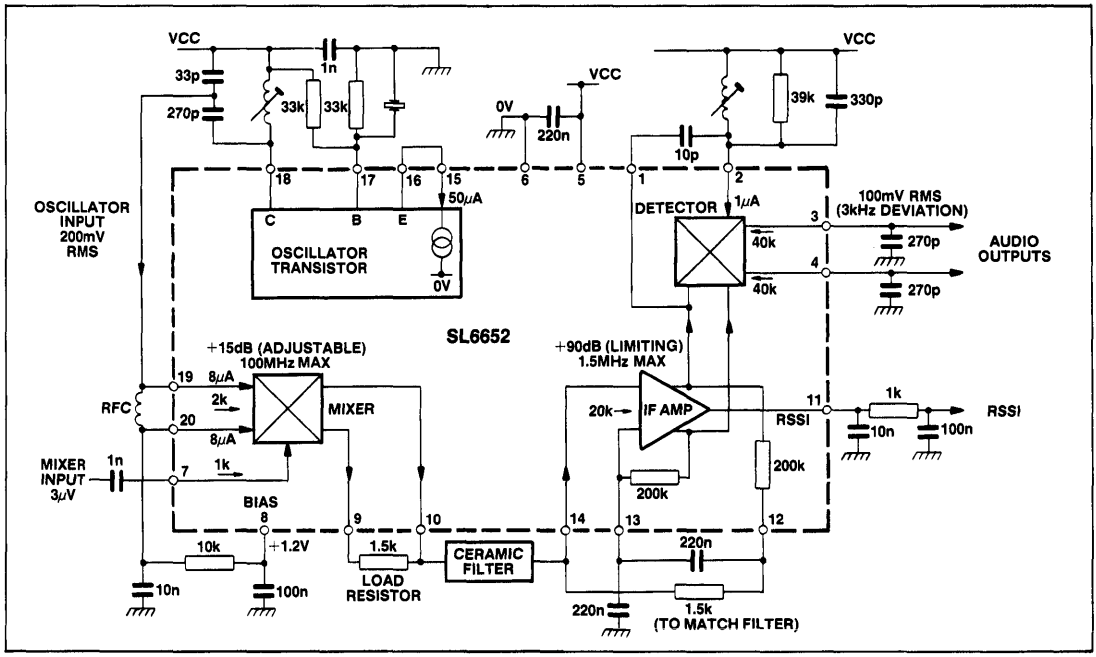

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30° C to +85° C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input <500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25° C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25° C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
RSSI Output(T_{amb} = +25° C)					
Output current			20	μA	No input pin 14
Output current	50		80	μA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

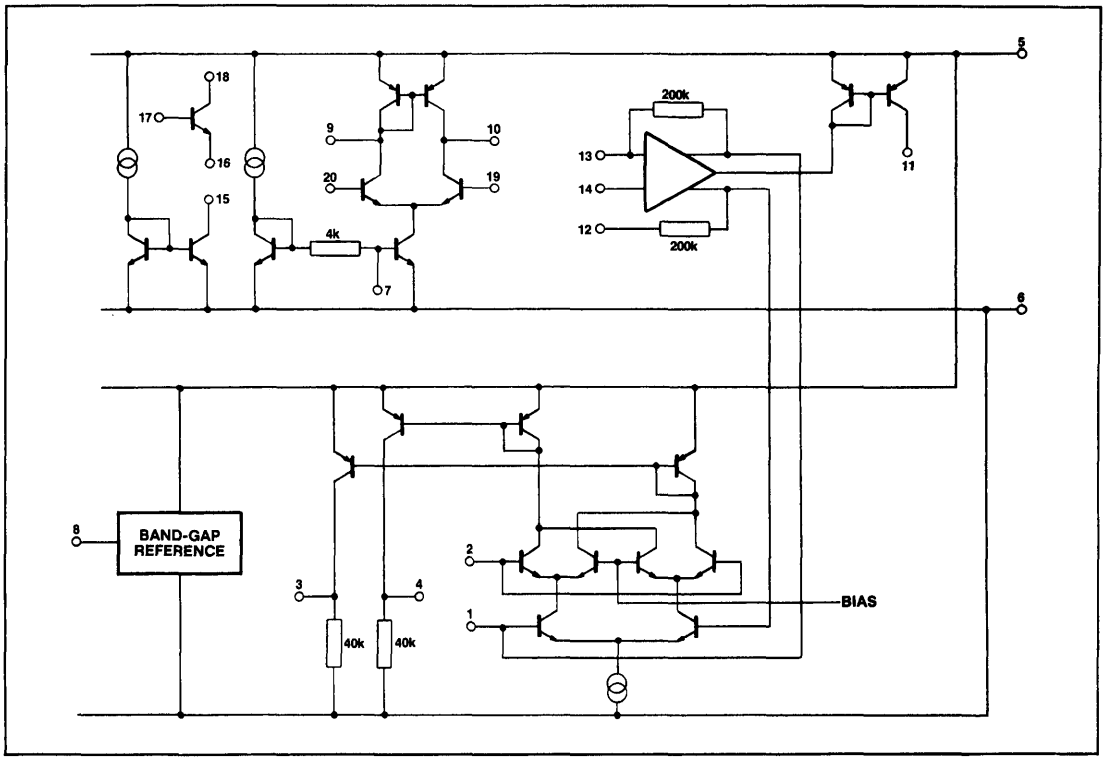

Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6652 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operting up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

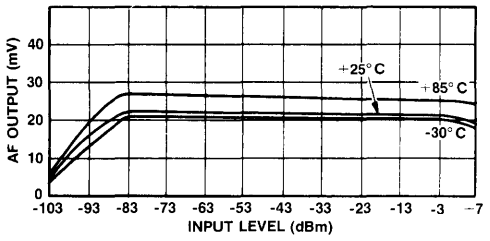

Fig.4 Audio output vs input and temperature at 2.5V

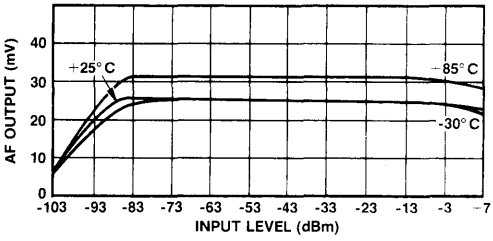

Fig.5 Audio output vs input and temperature at 5.0V

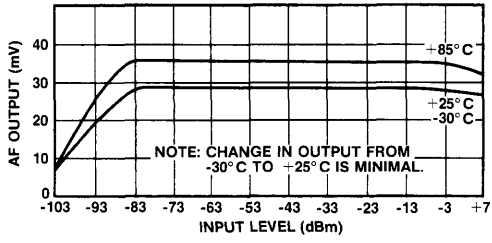

Fig.6 Audio output vs input and temperature at +7.5V

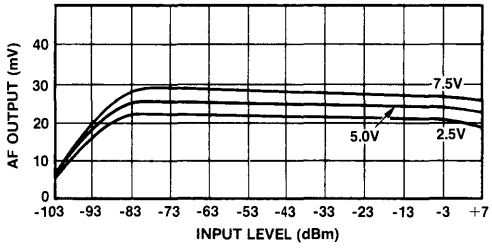

Fig.7 Audio output vs input and supply voltage at +25° C

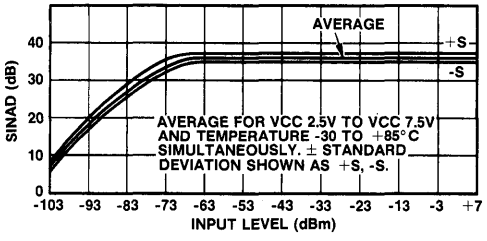

Fig.8 SINAD and input level

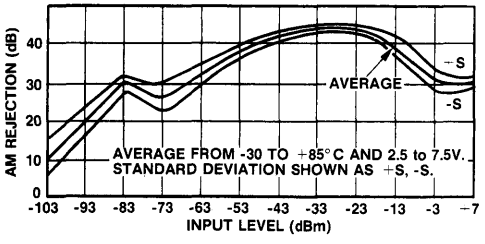

Fig.9 AM rejection and input level

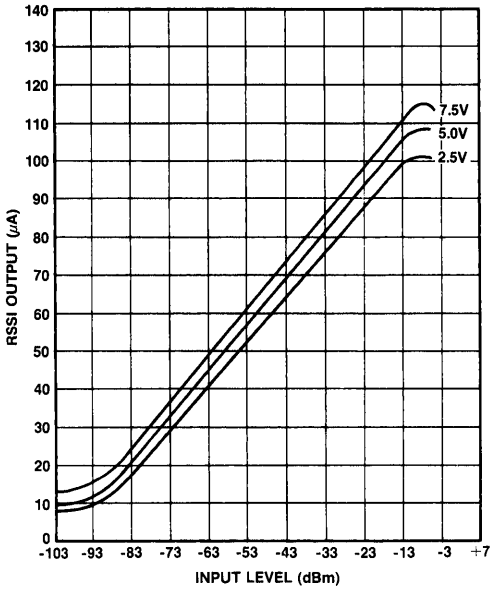

Fig.10 RSSI output vs input and supply voltage (T_{amb} = 20° C)

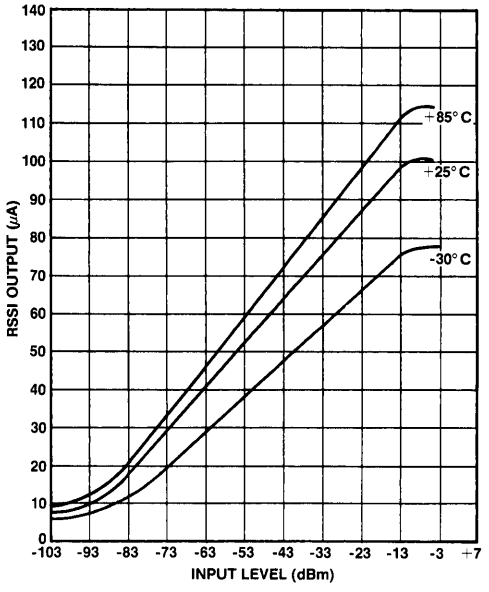

Fig.11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

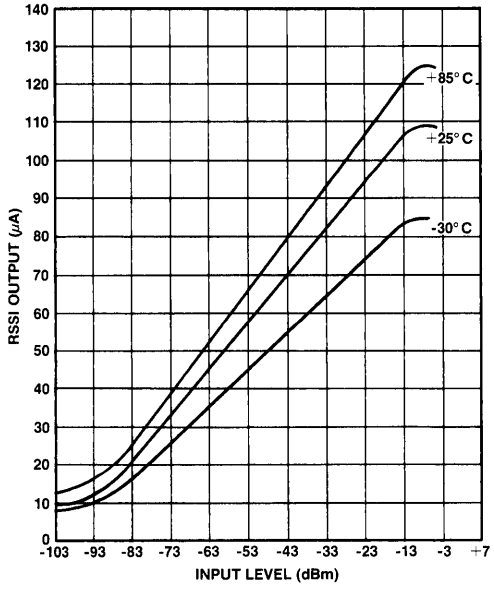

Fig.12 RSSI output vs input level and temperature (V_{CC} = 5V)

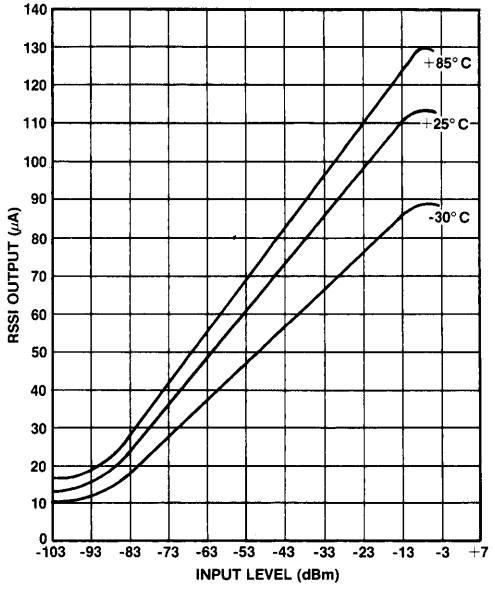

Fig.13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

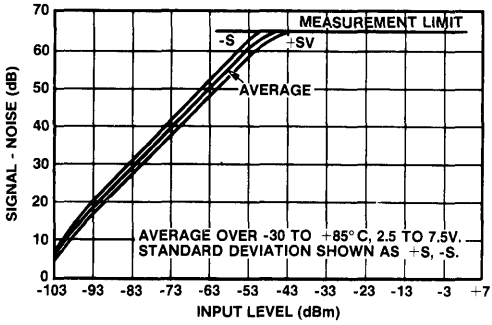

Fig.14 Signal + noise to noise ratio vs input level

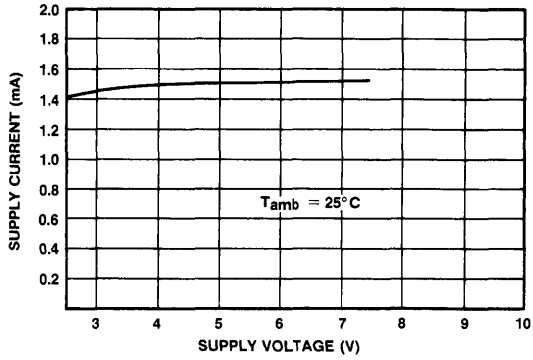

Fig.15 Supply current vs supply voltage

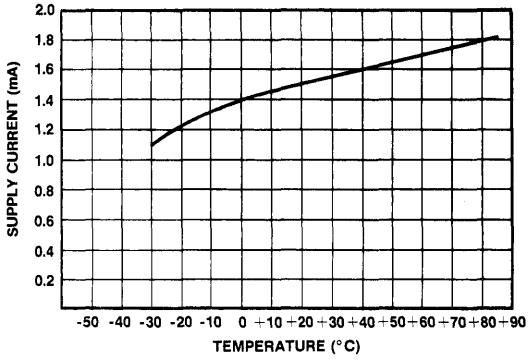

Fig.16 Supply current vs temperature (V_{CC} = 5V)

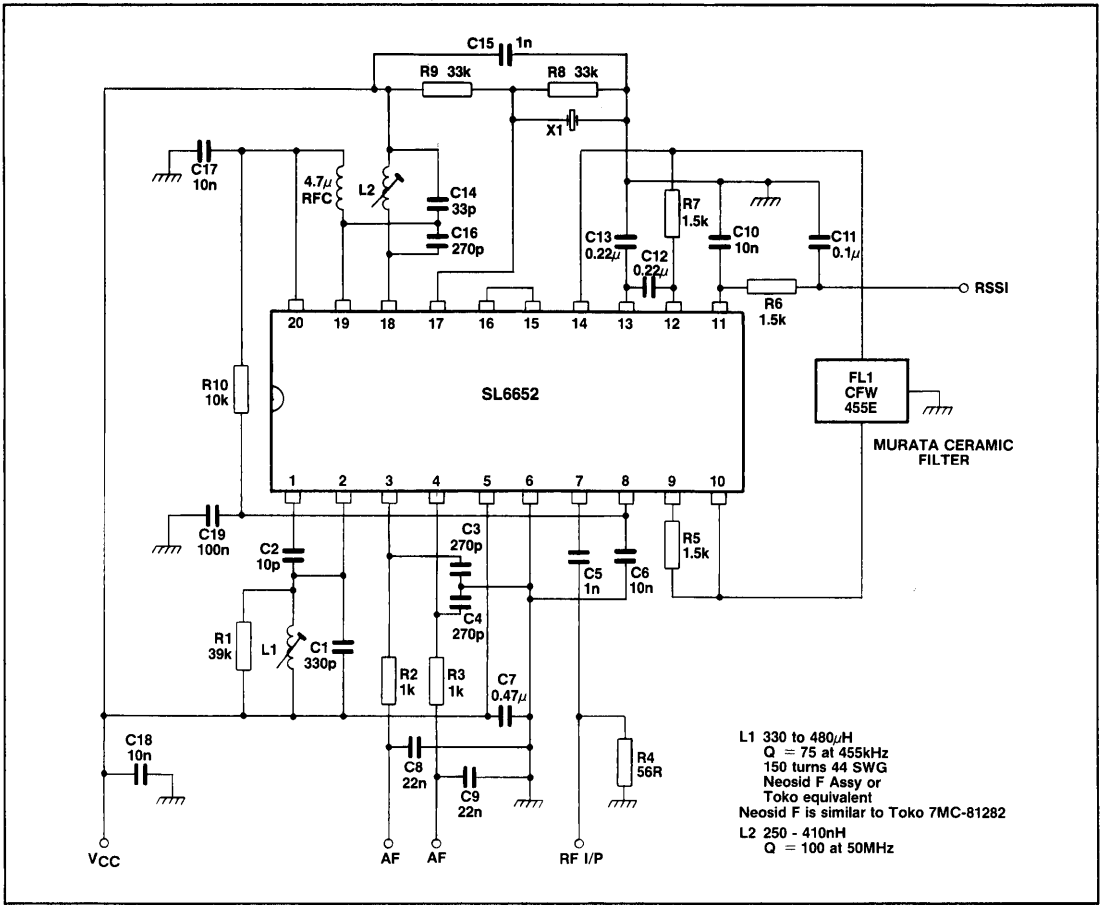

Fig.17 Circuit diagram of SL6652 demonstration board

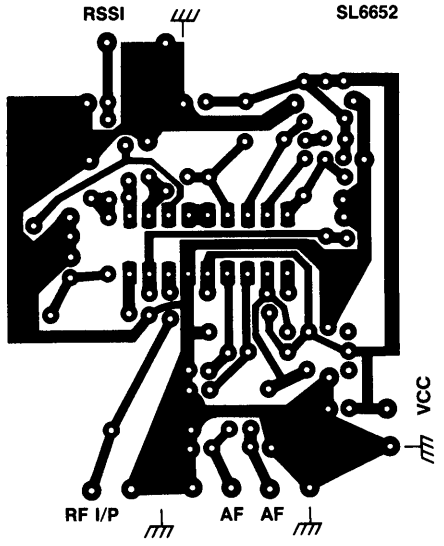

Fig.18 PCB mask of demonstration board (1:1)

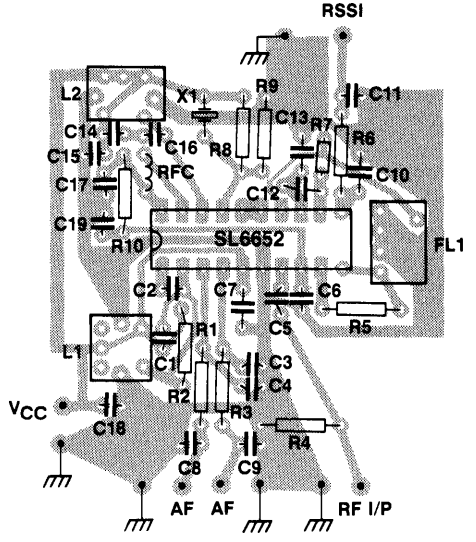

Fig.19 Component overlay of demonstration board (1:1)

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SL6653

LOW POWER IF/AF CIRCUIT FOR FM RECEIVERS

The SL6653 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V

The SL6653 affords maximum flexibility in design and use. It is supplied in a dual-in-line plastic package.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation

APPLICATIONS

- Mobile Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply voltage 2.5V to 7.5V
- Sensitivity 3μV

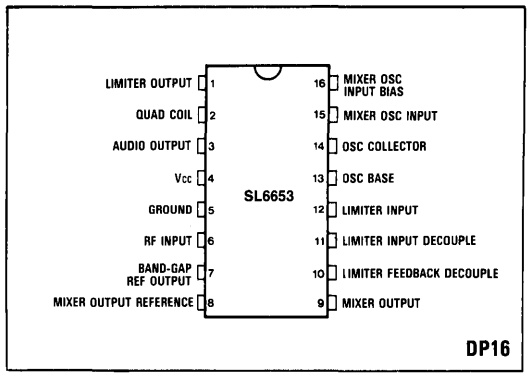


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

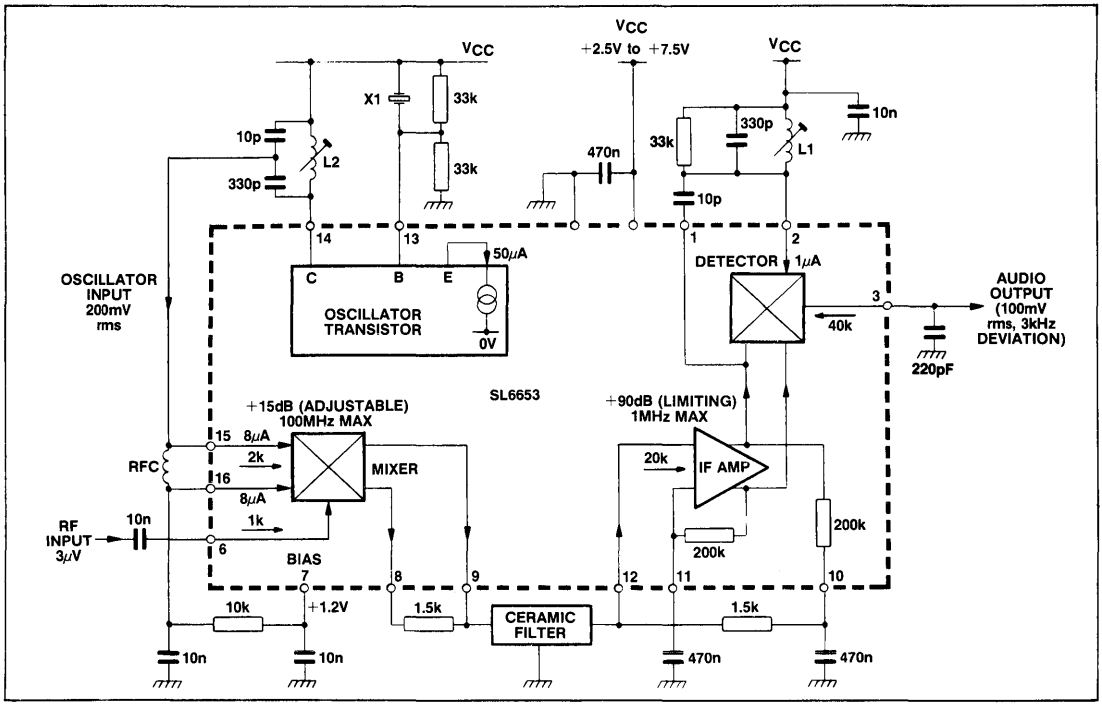


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30°C to +85°C, Mod.Freq. = 1kHz, Deviation = 2.5kHz, Quadrature Circuit Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		30		dB	RF input < 500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25°C
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25°C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	
Ultimate S/N ratio		60		dB	10mV into pin 12
THD		0.5	5	%	
Output impedance		40		kohm	

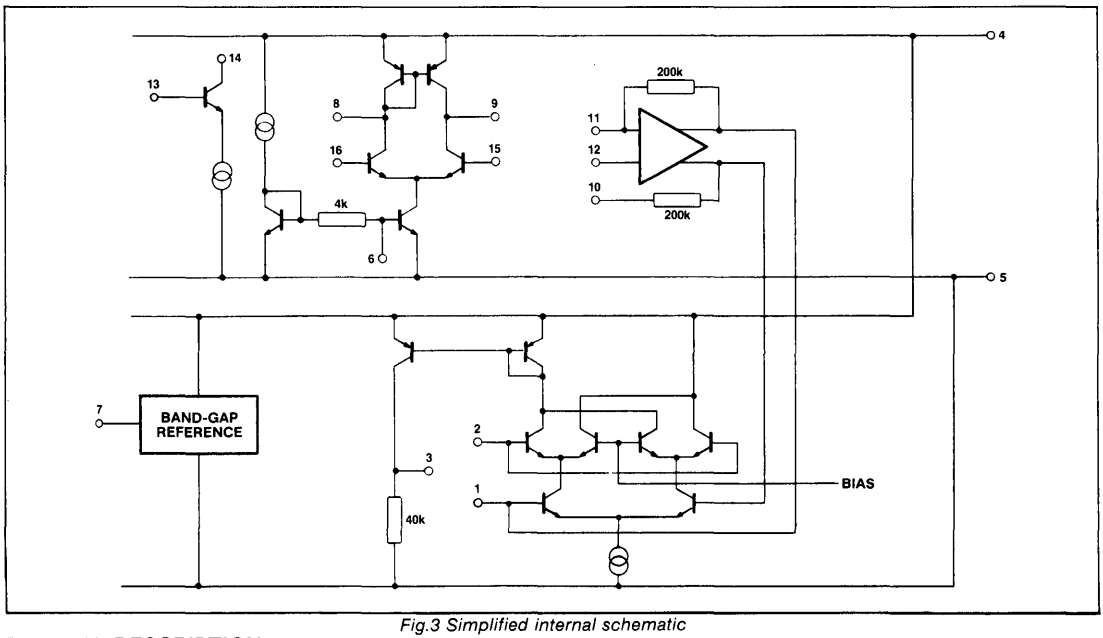


Fig.3 Simplified internal schematic

GENERAL DESCRIPTION

The SL6653 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- A transistor for use as an oscillator
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of a transistor and a current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

Supply voltage

The SL6653 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

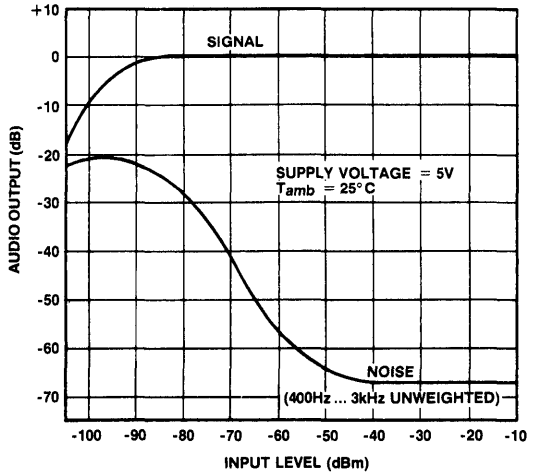


Fig.4 Audio and noise outputs vs input level

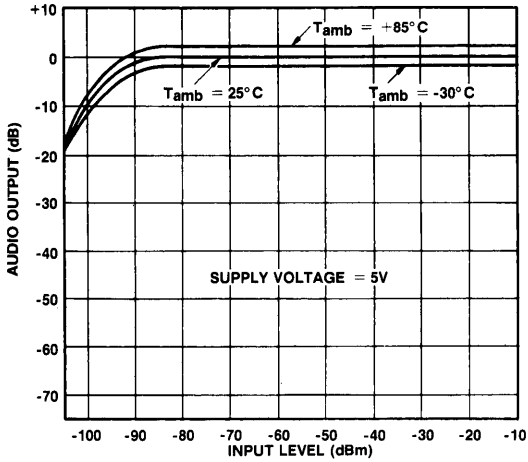


Fig.5 Audio output vs temperature

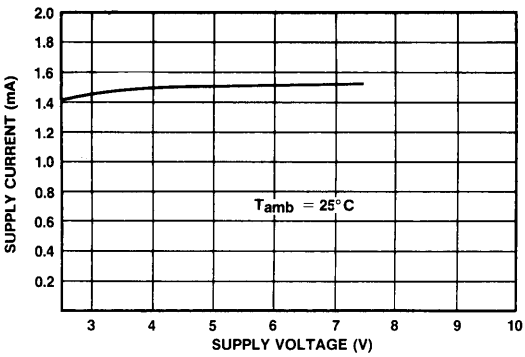


Fig.6 Supply current vs supply voltage

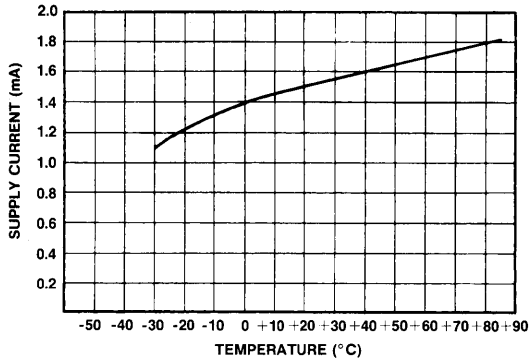


Fig.7 Supply current vs temperature

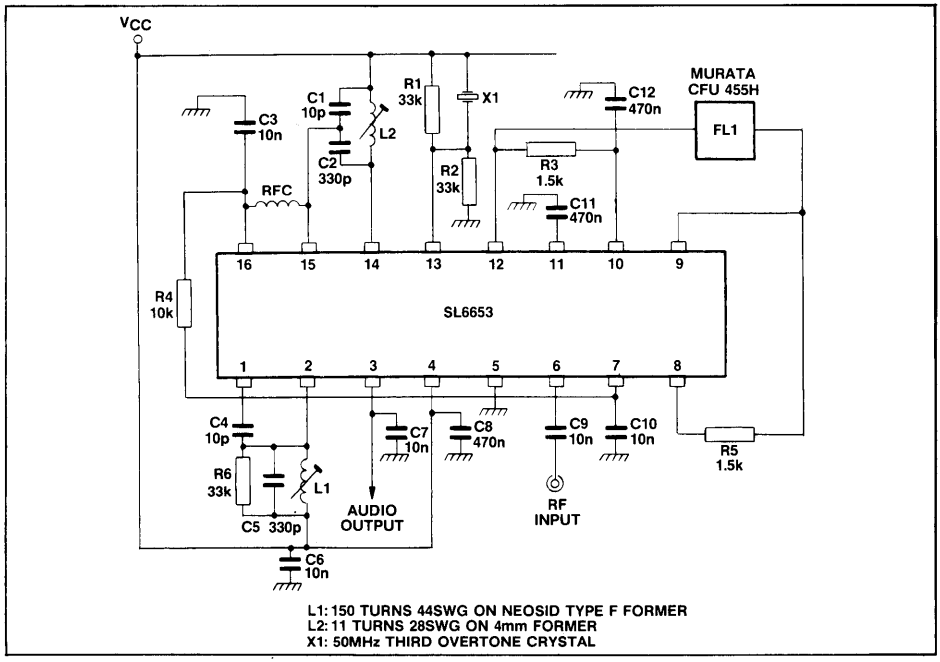


Fig.8 Circuit diagram of SL6653 demonstration board

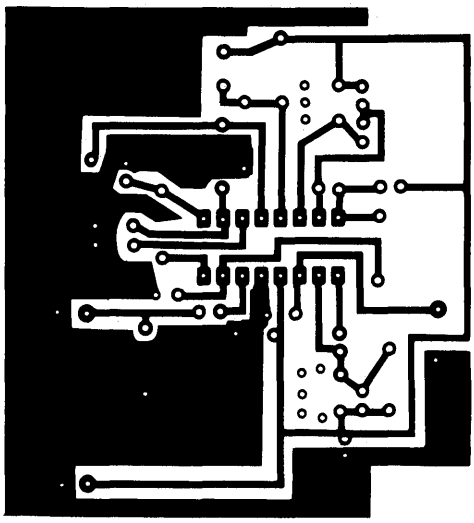


Fig.9 PCB mask of demonstration board (1:1)

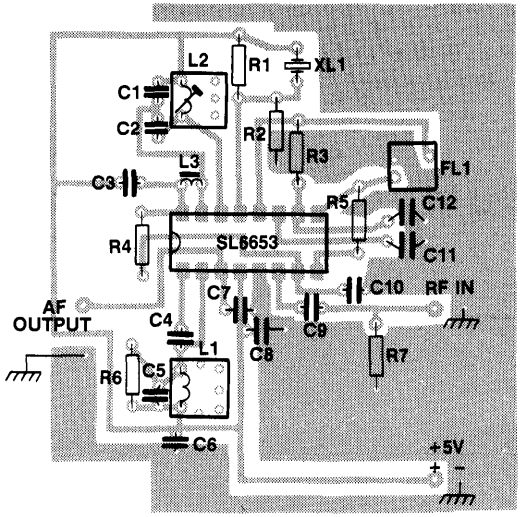


Fig.10 Component overlay of demonstration board (1:1)

SL6654

LOW POWER IF/AF CIRCUIT FOR FM CELLULAR RADIO

The SL6654 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

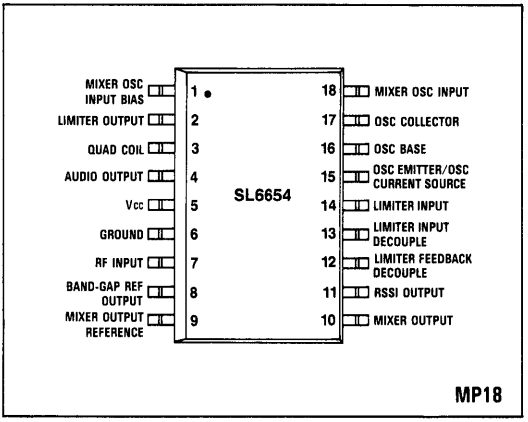


Fig.1 Pin connections (top view)

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB

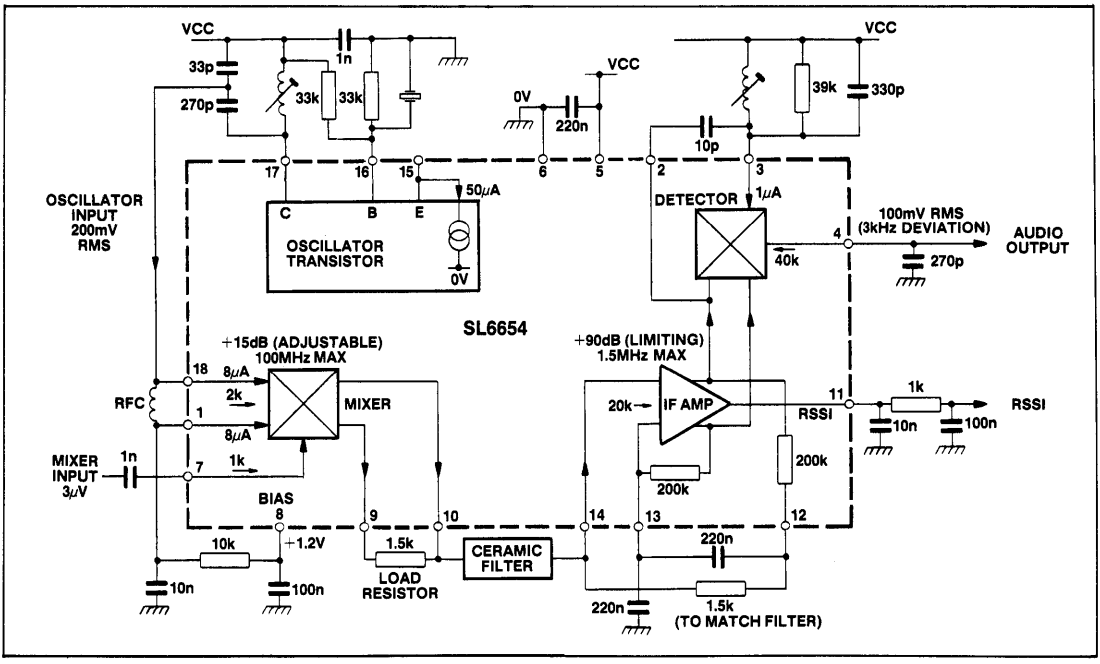


Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30° C to +85° C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input <500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25° C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25° C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
RSSI Output(T_{amb} = +25° C)					
Output current			20	μA	No input pin 14
Output current	50		80	μA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

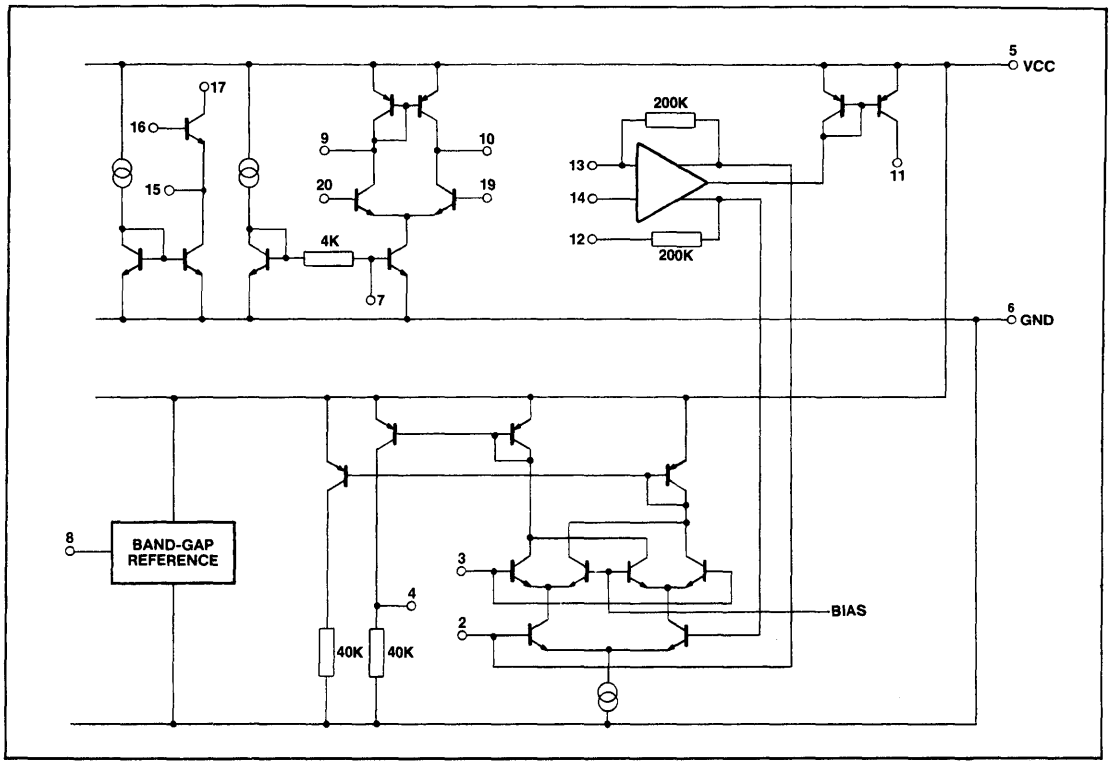


Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6654 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operting up to 1.5MHz
- A quadrature detector with AF output [redacted]
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor with a current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector providing audio output is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6654 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

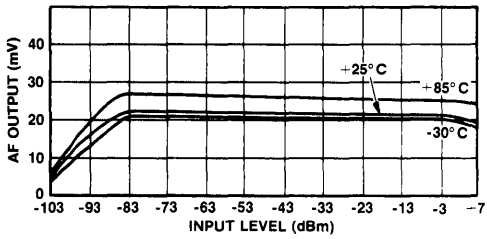


Fig.4 Audio output vs input and temperature at 2.5V

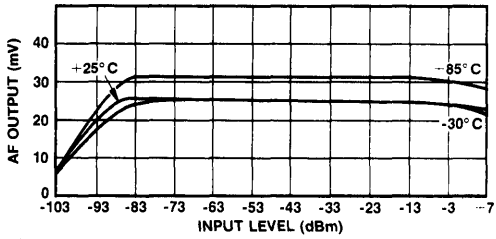


Fig.5 Audio output vs input and temperature at 5.0V

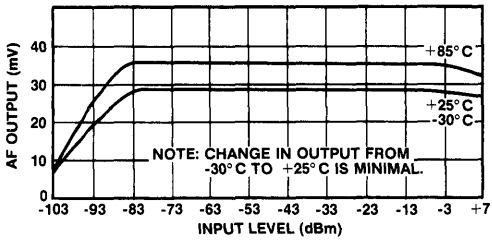


Fig.6 Audio output vs input and temperature at +7.5V

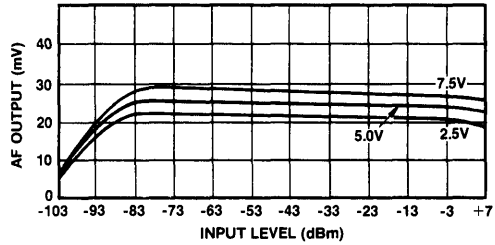


Fig.7 Audio output vs input and supply voltage at +25° C

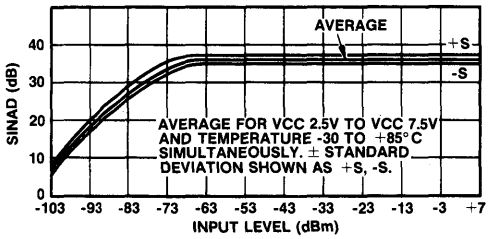


Fig.8 SINAD and input level

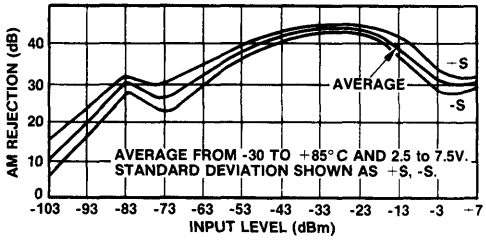


Fig.9 AM rejection and input level

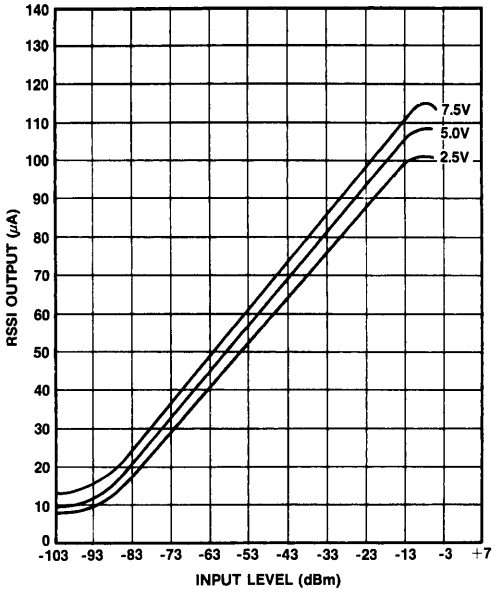


Fig.10 RSSI output vs input and supply voltage (T_{amb} = 20° C)

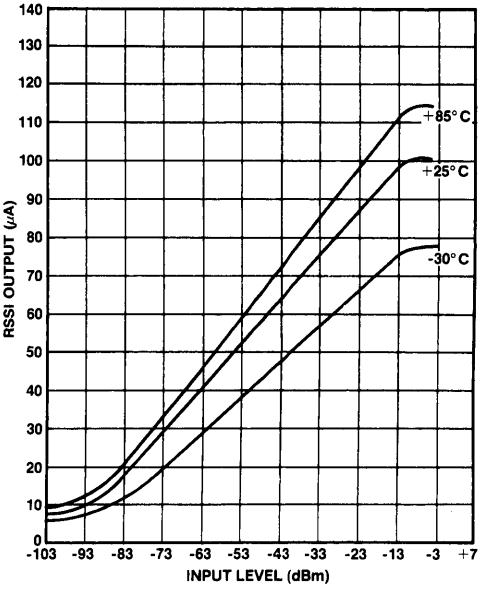


Fig.11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

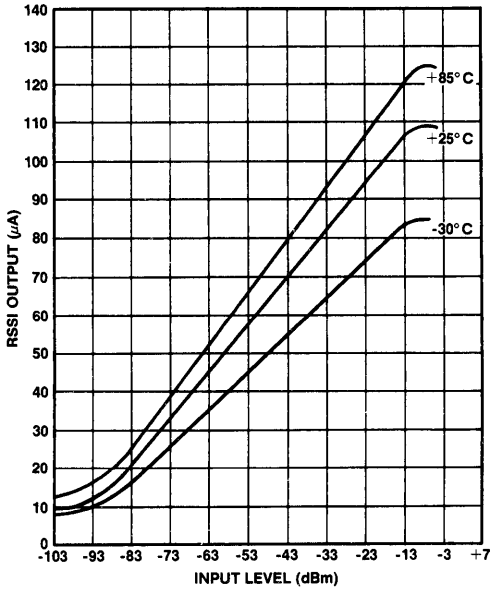


Fig.12 RSSI output vs input level and temperature (V_{CC} = 5V)

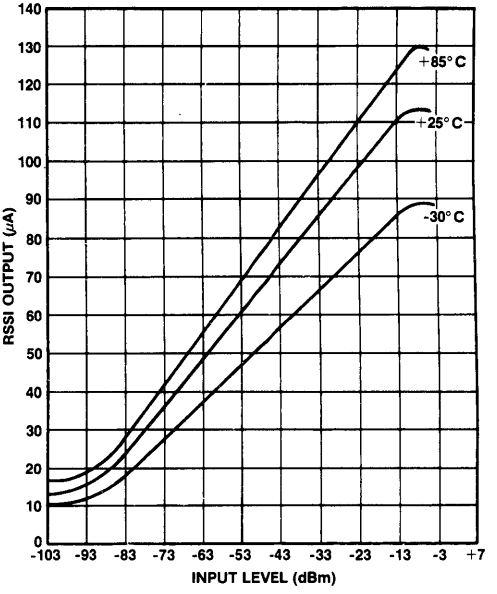


Fig.13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

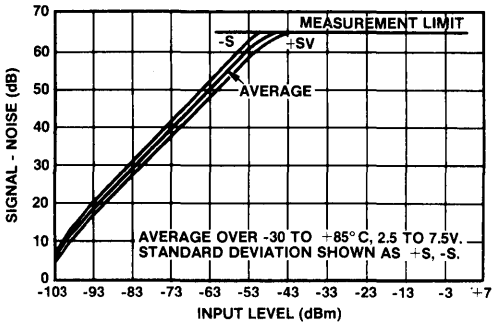


Fig.14 Signal + noise to noise ratio vs input level

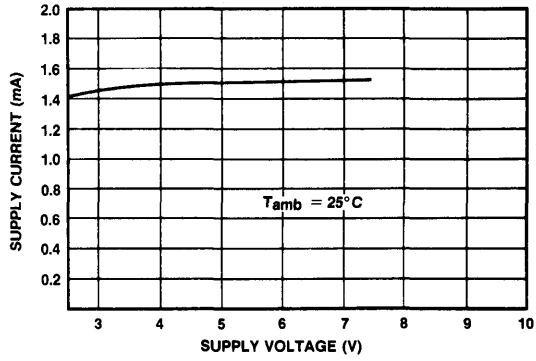


Fig.15 Supply current vs supply voltage

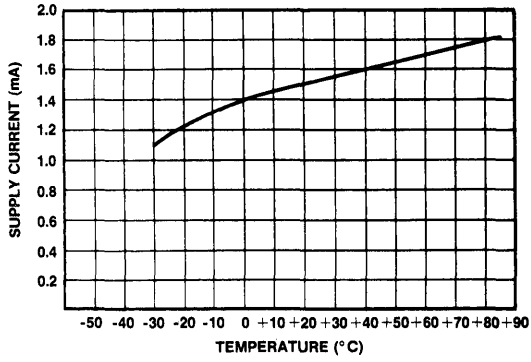


Fig.16 Supply current vs temperature (V_{CC} = 5V)

SL6655

ULTRA LOW POWER FM RADIO RECEIVER

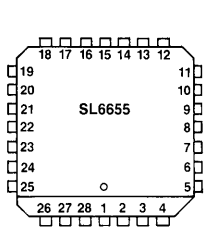
The SL6655 is a single conversion receiver complete with RF amp/mixer/oscillator/IF amplifier and detector. It features very low current consumption and operation from 0.9V to 8V supply. The device can be powered down to currents of 1μA and offers sensitivities of typically 250nV.

FEATURES

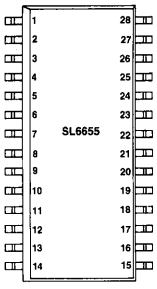
- Very Low Voltage Operation (0.9V)
- Very Low Current Consumption:
  - 1mA Powered Up (typ.)
  - 1μA Powered Down (typ.)
- Wide Supply Range 0.9V to 8V
- 250nV Sensitivity (12dB Sinad)
- Guaranteed 100MHz Operation
- Small Outline Package

APPLICATIONS

- Low Power Radio Receivers
- Radio Paging
- Cordless Telephones



HP28



MP28

Pin	Function	Pin	Function
1	N/C	15	RF Vcc +
2	Mixer output	16	LF Vcc +
3	Battery economy	17	Audio output
4	Oscillator current source & emitter	18	Audio output(Differential)
5	Oscillator base	19	Quad coil drive
6	Oscillator collector	20	Quad coil
7	Mixer osc input	21	N/C
8	Mixer osc I/P bias	22	2nd limiter F/B decouple
9	Mixer RF input	23	2nd limiter input
10	RF amp output	24	2nd limiter I/P decouple
11	Regulator output	25	1st limiter output
12	RF amp input	26	1st limiter I/P decouple
13	RF ground	27	1st limiter input
14	LF ground	28	1st limiter F/B decouple

Fig.1 Pin connections - top view

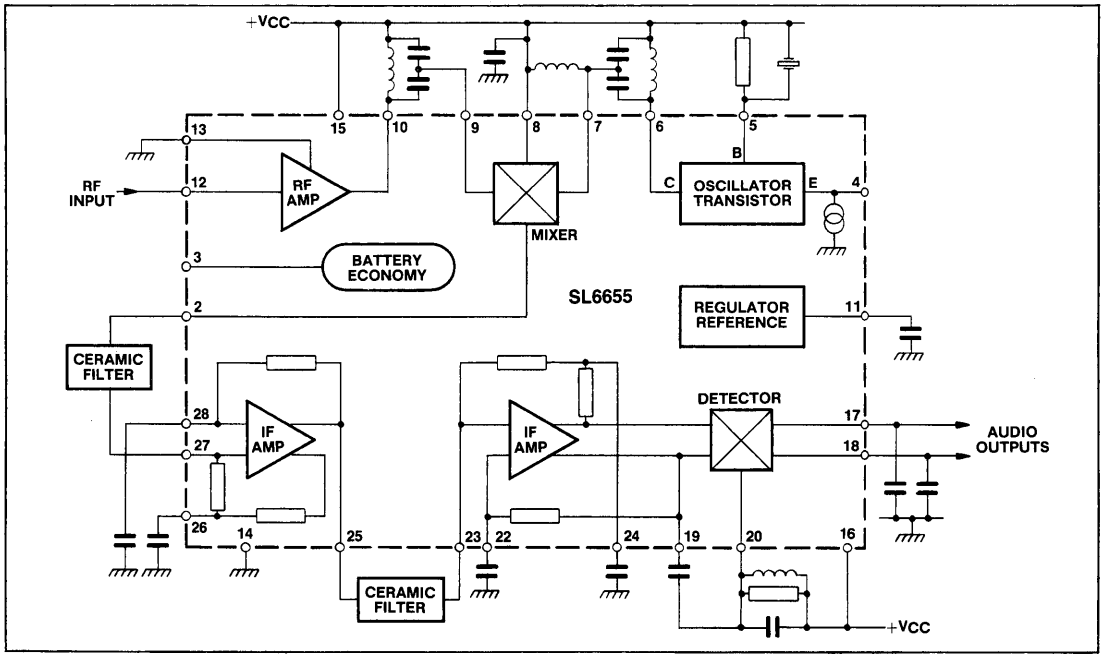


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, T_{amb} = 0° C to +50° C, V_{CC} = 1.3V

Characteristic	Pin Number	Value			Units	Conditions
		Min.	Typ.	Max.		
Overall						
Supply voltage		0.9		8	V	25° C
Supply voltage		1.0		8	V	-30° C to +85° C
Supply current						
Powered up			1.0	1.3	mA	Pin 3 High
Powered down			1.0		μA	Pin 3 Low
Battery economy response			0.5		ms	
Sensitivity			250		nV	12dB Sinad
AM rejection			37		dB	
RF amplifier						
Supply current			50		μA	
Noise figure			6		dB	
H_{FE}			100			
f_T			500		MHz	
Oscillator						
Supply current			50		μA	
H_{FE}			100			
f_T			500		MHz	
IF amplifier cascade						
Sensitivity	27		3		μV	12dB Sinad
Input impedance	27, 23		1.5		kΩ	
Output impedance	25		1.5		kΩ	
Gain			100		dB	
Upper cut-off frequency			1.5		MHz	
Detector						
Audio output level			7		mV(rms)	
Inter-output isolation			65		dB	
Output impedance			50		kΩ	
Mixer						
Conversion gain			6		dB	
Input impedance			4		kΩ	
Output impedance			1.5		kΩ	
Regulator						
Output level		0.9	0.95	1	V	
Output temperature coefficient			1.3		mV/° C	
Output current		6			mA	
Battery economy						
Input current			0.5		μA	
Input logic high		80			% V_{CC}	
Input logic low				20	% V_{CC}	

GENERAL DESCRIPTION

The RF amplifier is a diode biased input with a bias current of typically 50μA. The output is left open circuit so that the gain can be selected externally.

The RF input to the Mixer is diode biased with a bias current of typically 250μA. The oscillator input is differential, but would normally be driven single ended with the remaining input biased at V_{CC}.

The Mixer has a single output with resistance of 1.5kΩ. A single transistor is used for the oscillator which has its base and collector floating, and the emitter connected to a current source of 50μA nominal value.

The IF amplifiers have input impedances of 1.5kΩ and are thus ideally suited for use with 455kHz ceramic filters.

The detector is fed internally from the IF limiting amplifier and the quadrature input is fed externally using a capacitor and appropriate phase shift networks. A differential audio output is provided to feed a comparator for digital use. The regulated output is a supply independent and partially temperature compensated capable of sourcing 6mA.

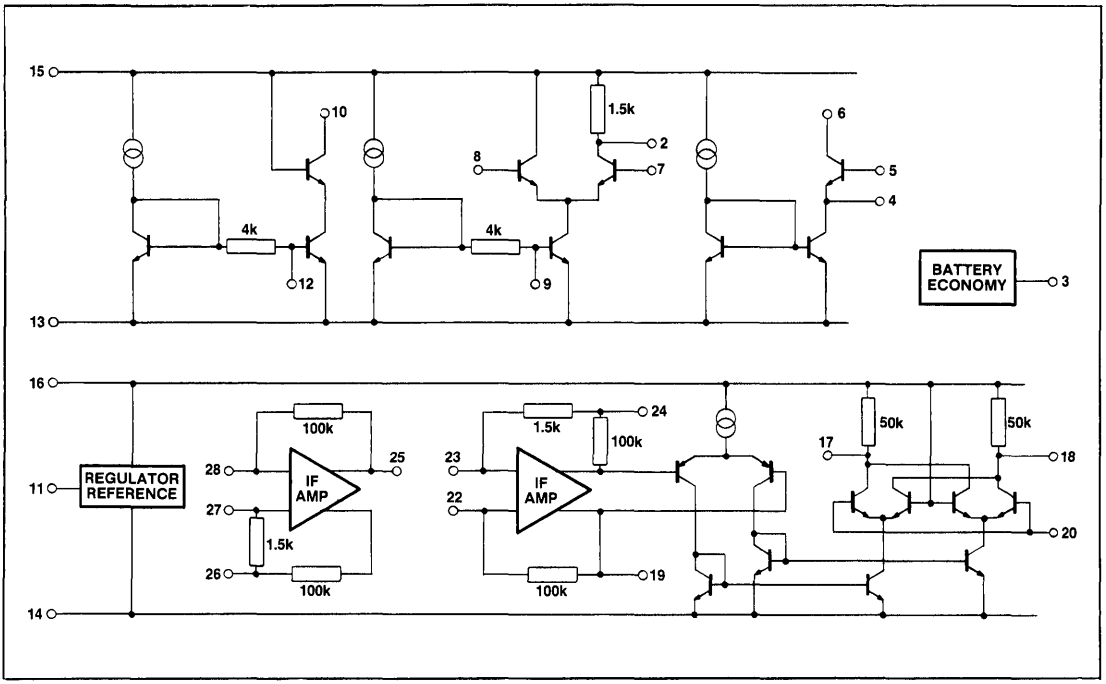


Fig.3 SL6655 internal schematic

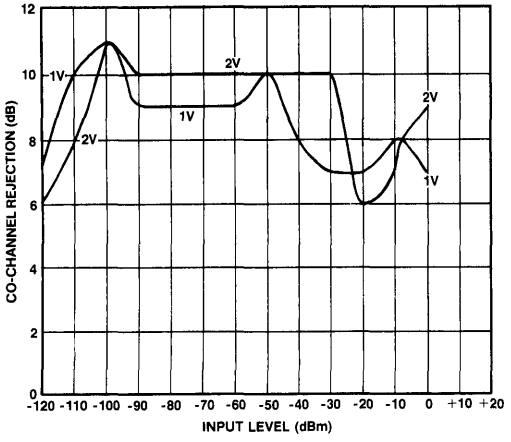


Fig.4 Input level vs co-channel rejection for V_{CC} = 1 & 2V at 25° C (unweighted measurements)

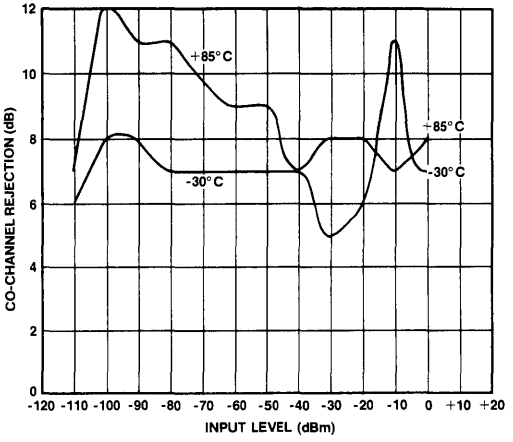


Fig.5 Co-channel rejection vs input level over temperature at V_{CC} = 1V (unweighted measurements)

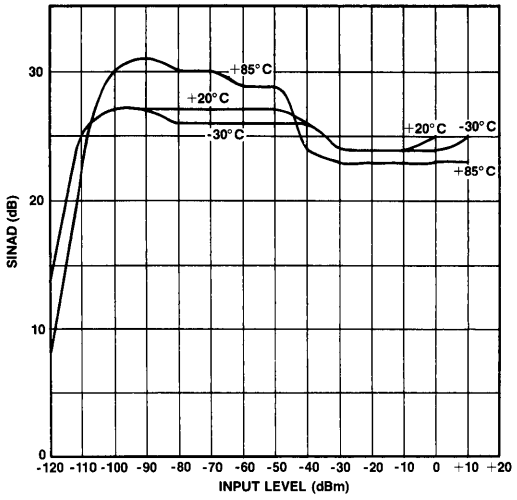


Fig.6 Sinad vs input level over temperature at Vcc = 1V (unweighted measurements)

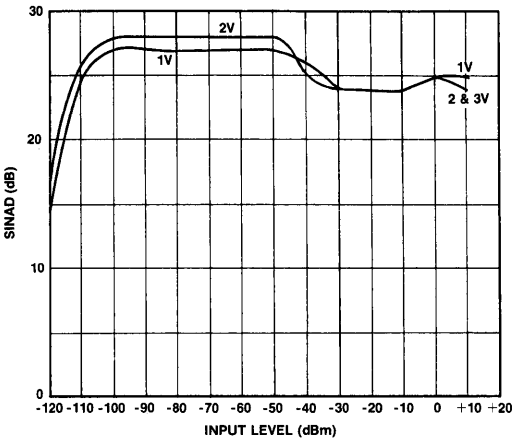


Fig.7 Sinad vs input level at Vcc = 1, 2 & 3V (unweighted measurements)

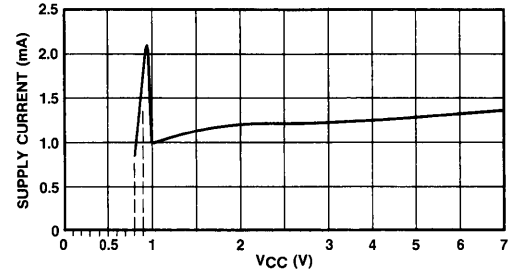


Fig.8 Supply current vs Vcc

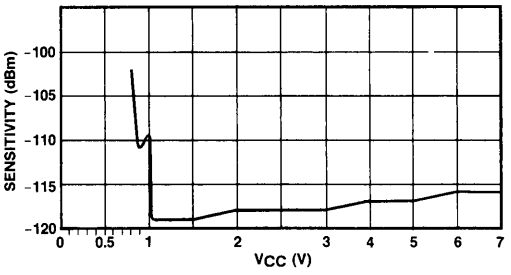


Fig.9 Sensitivity (dBm for 12dB sinad) vs Vcc

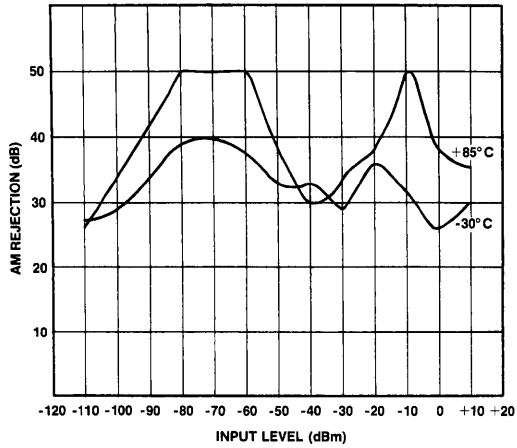


Fig.10 AM rejection vs input level over temperature at Vcc = 1V (unweighted measurements)

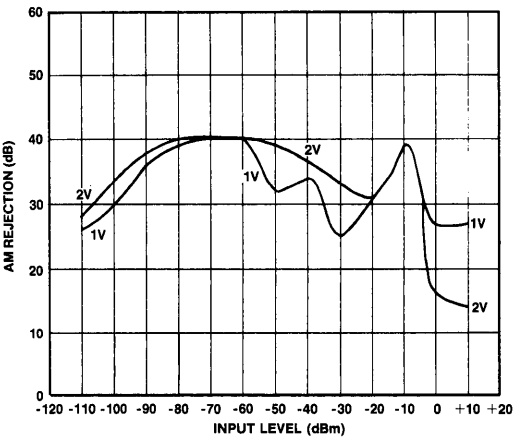


Fig.11 AM rejection vs input level at 20° C (unweighted measurements)

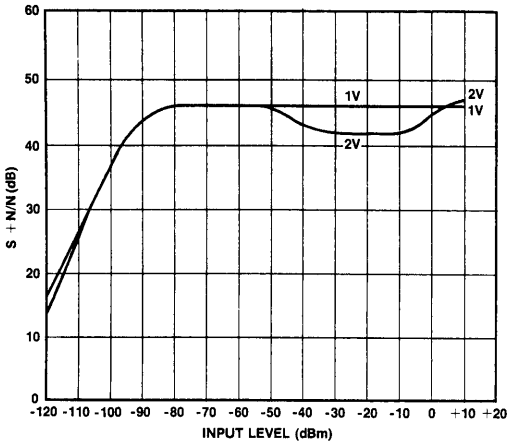


Fig.12 S + N/N vs input level (unweighted measurements)

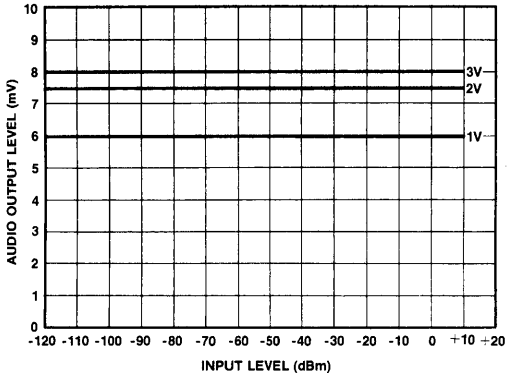


Fig.13 Audio output level vs input level (unweighted measurements)

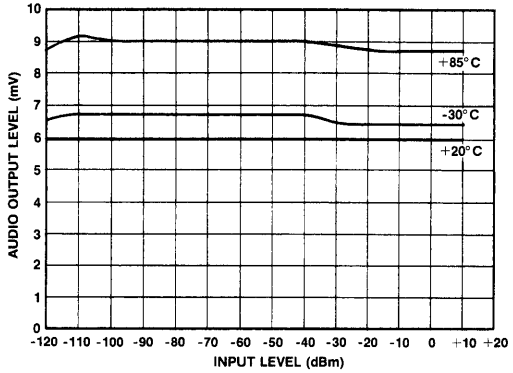
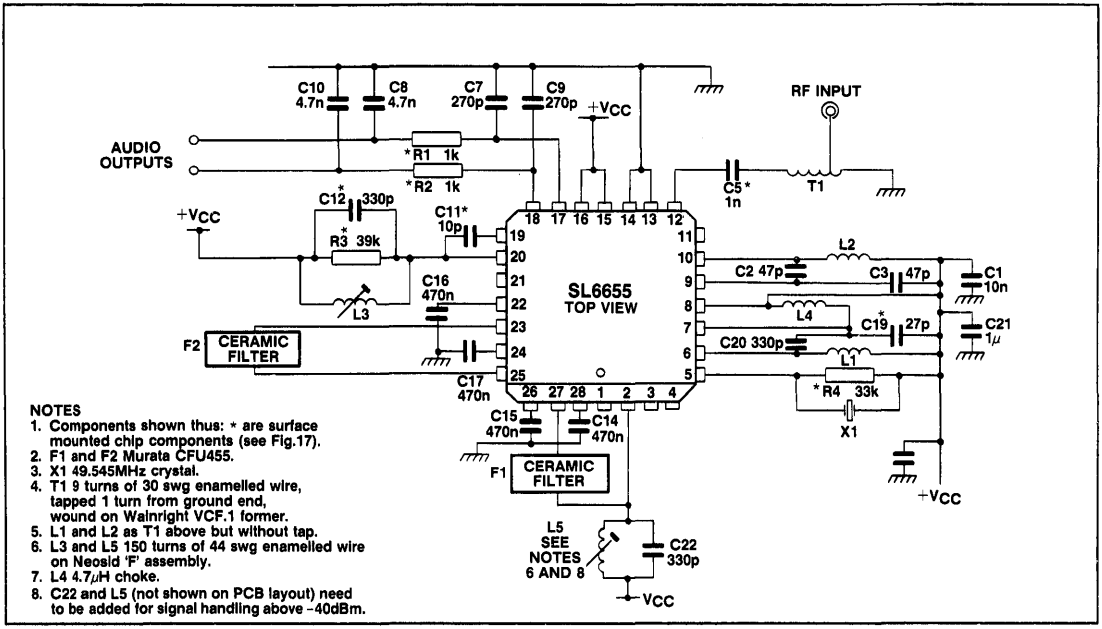


Fig.14 Audio output level vs input level over temperature at V_{CC} = 1V (unweighted measurements)



NOTES
1. Components shown thus: * are surface mounted chip components (see Fig.17).
2. F1 and F2 Murata CFU455.
3. X1 49.545MHz crystal.
4. T1 9 turns of 30 swg enamelled wire, tapped 1 turn from ground end, wound on Wainright VCF.1 former.
5. L1 and L2 as T1 above but without tap.
6. L3 and L5 150 turns of 44 swg enamelled wire on Neosid 'F' assembly.
7. L4 4.7µH choke.
8. C22 and L5 (not shown on PCB layout) need to be added for signal handling above -40dBm.

Fig.15 Circuit diagram of SL6655 demonstration board

PERFORMANCE OF SL6655 DEMONSTRATION BOARD

Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, T_{amb} = 0°C to +50°C, Vcc = 1.3V

Sensitivity	-119dBm for 12dB sinad at 1.3V -113dBm for 12dB sinad at 0.9V
Adjacent channel rejection	50dB at 1.3V 68dB at 0.9V
Co-channel rejection	10dB at 1.3V 9dB at 0.9V
RF amplifier 2nd order intercept **RF amplifier 3rd order intercept**	0dB -14dBm
Noise figure of RF amplifier	6dB

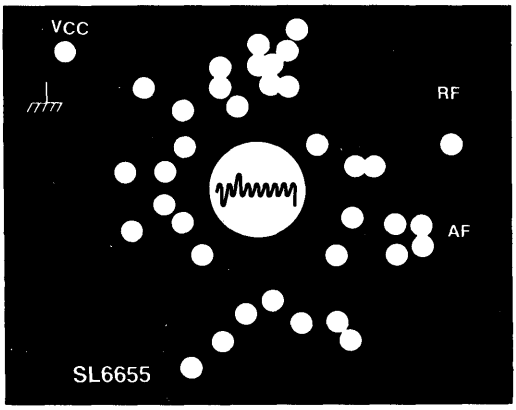


Fig.16 Ground plane of demonstration board (1:1)

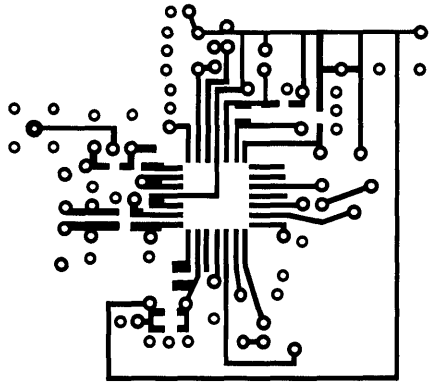


Fig.17 Track side of demonstration board (1:1)

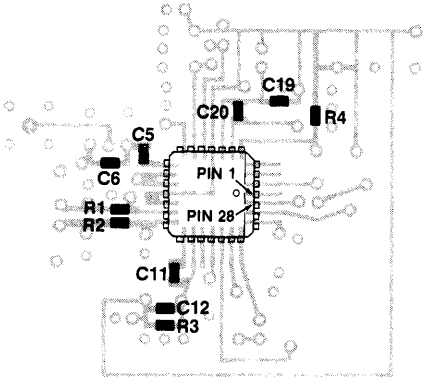


Fig.18 Surface mounted component overlay (track side) of demonstration board (1:1)

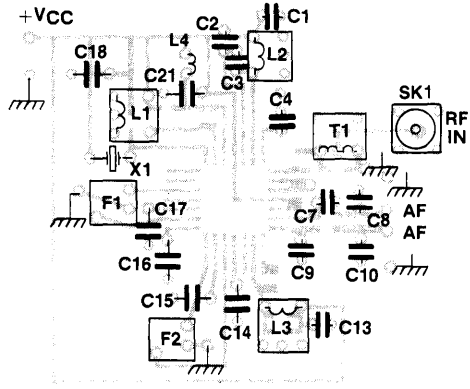


Fig.19 Component overlay (ground plane side) of demonstration board (1:1)

SP8703

1GHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8703 is a divide by 128/9 programmable divider with a maximum specified operating frequency of 1GHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The output stage is CMOS compatible only, the 0 to 1 output edge giving best loop delay performance.

A unique 'power-down' feature is included to minimise power consumption.

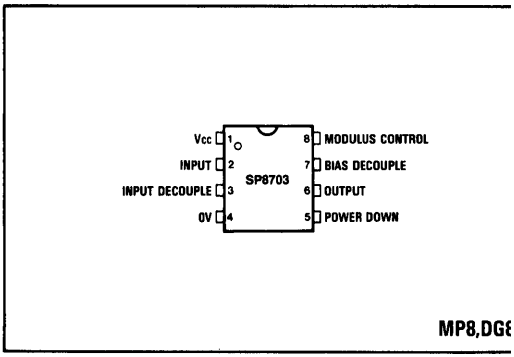


Fig.1 Pin connections - top view

FEATURES

- DC to 1GHz Operation
- -30° to +70°C Temperature Range
- Unique Power-Down Feature
- CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 30mA Typical

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 6V
- Storage Temperature Range: -30°C to +150°C
- Junction Temperature: +175°C
- Input Voltage: 2.5V p-p

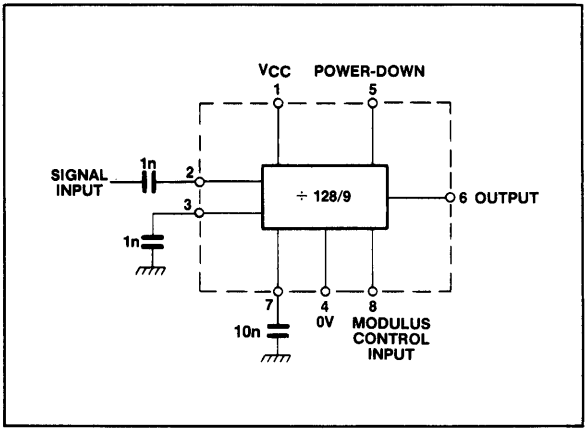


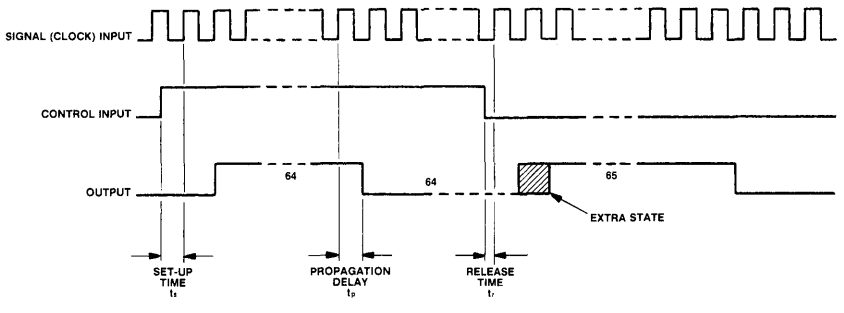
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +4.75V to 5.25V, T_{amb} = -30°C to +70°C

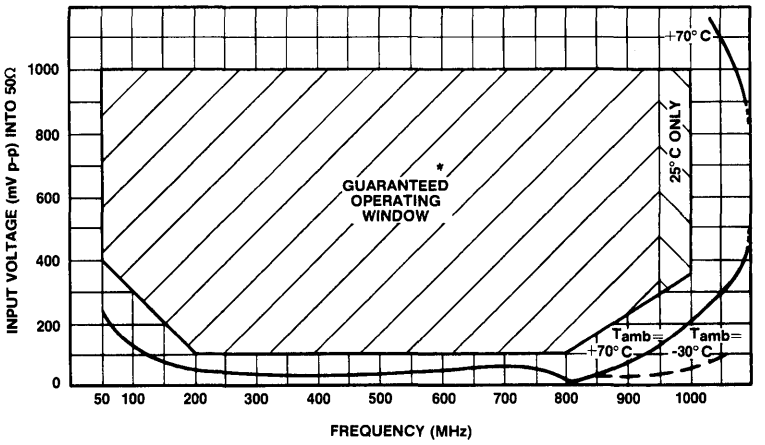
Characteristics	Value		Units	Conditions	Notes
	Min.	Max.			
Maximum frequency	1000		MHz	T_{amb} = 25°C	Note 1,2,4
Maximum frequency	950		MHz		Note 1,2,3
Minimum frequency (sinewave)		50	MHz		Note 1,2,3
Power supply current		40	mA	Power-up	Note 3
Power supply current		3	mA	Power-down	Note 3
Output high voltage	3.2	V_{CC}	V	IL = -0.2mA	Note 3
Output low voltage	0	1.7	V	IL = 0.2mA	Note 3
Control input high voltage	3.2	V_{CC}	V	Divide by 128	Note 3
Control input low voltage	0	1.7	V	Divide by 129	Note 3
Control input high current		50	μA	Input = V_{CC}	Note 3
Control input low current	-10		μA	Input = 0V	Note 3
Power-down high voltage	3.2	V_{CC}	V	Power-down	Note 3
Power-down low voltage	0	1.7	V	Power-up	Note 3
Power-down high current		10	μA	Input = V_{CC}	Note 3
Power-down low current	-2		μA	Input = 0V	Note 3
Clock to output delay		30	ns	CL = 10pF	Note 5
Set-up time		15	ns	CL = 10pF	Note 5
Release time		15	ns	CL = 10pF	Note 5

NOTES
1. See Fig.4 for guaranteed operating window.
2. See Fig.5 for input voltage measurement method.
3. Tested at 25°C and +70°C only.
4. Tested at 25°C only.
5. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷128 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷129 mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

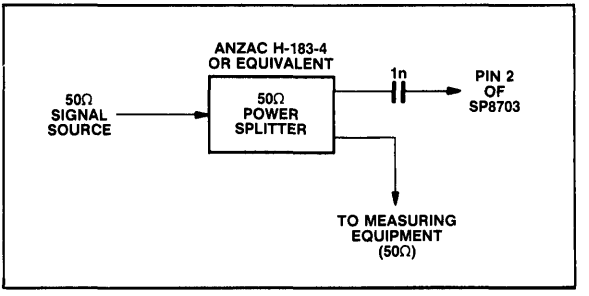


Fig.5 Input voltage measurement method

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/μs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.

SP8704

950MHz VERY LOW CURRENT TWO-MODULUS DIVIDER

The SP8704 is a switchable divide by 128/129, 64/65 programmable divider with a maximum specified operating frequency of 950MHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The SP8704 will operate from any supply from 3V to 5V and features full electrostatic discharge protection.

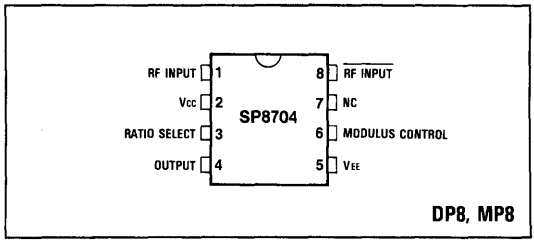


Fig.1 Pin connections - top view

FEATURES

- DC to 950MHz Operation
- -40°C to +85°C Temperature Range
- Operation from 3V to 5V Supply
- ESD Protection on all Pins

QUICK REFERENCE DATA

- Supply Voltage 3V to 5V
- Supply Current 10mA - Including Output Emitter Follower

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	7V
Storage temperature range:	30°C to +150°C
Junction temperature:	+175°C
Input voltage:	2.5V p-p

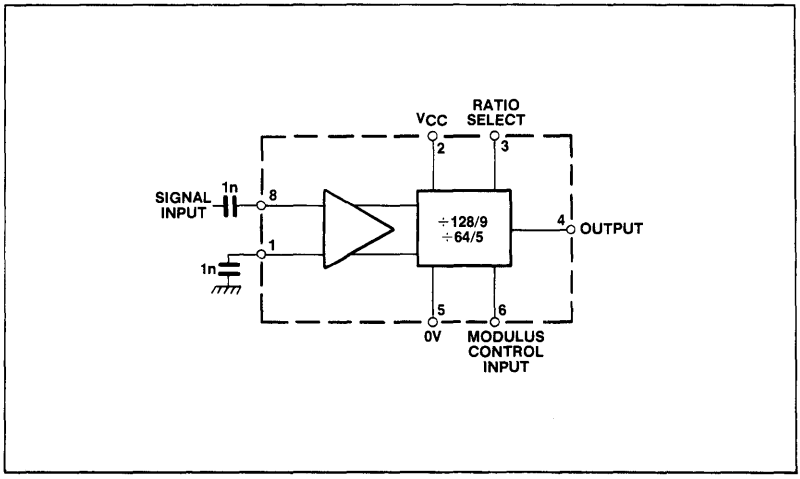


Fig.2 Functional diagram SP8704

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40°C to 85°C, V_{CC} = +2.75V to +5.5V

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current			10		mA	Including output emitter follower
Input sensitivity	10MHz			150	mV rms	Sinewave input into 50Ω
	80MHz			25		
	150MHz			15		
	850MHz			15		
	950MHz			50		
Input overload		300			mV rms	
Input impedance			50		Ω	
			2		pF	
Output			1		V pk-pk	Emitter follower output current source = 0.75mA
Ratio select (pin 3)	LO			1	V	128/129 selected
	HI *	V_{CC}			V	64/65 selected
Modulus control (pin 6)	LO	1			V	65 or 129 selected
	HI *			2	V	64 or 128 selected
Clock to output delay						
Set up time						
Release time						

*Or pin open circuit

TRUTH TABLE

Pin 3	Pin 6	Division ratio
L	L	129
L	H	128
H	L	65
H	H	64

SP8716/8/9

520MHz ULTRA LOW CURRENT TWO MODULUS DIVIDERS

SP8716 ÷ 40/41, SP8718 ÷ 64/65, SP8719 ÷ 80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -30°C to +70°C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the best loop delay performance.

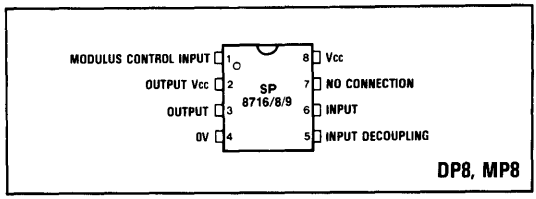


Fig.1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -40°C to +85°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.2V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage (Pin 2 or 8): 8V
- Storage Temperature Range: -40°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

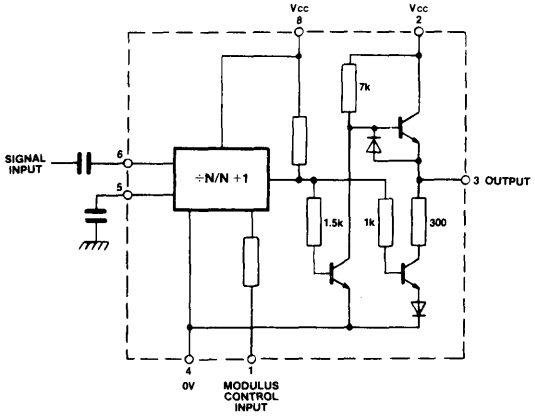


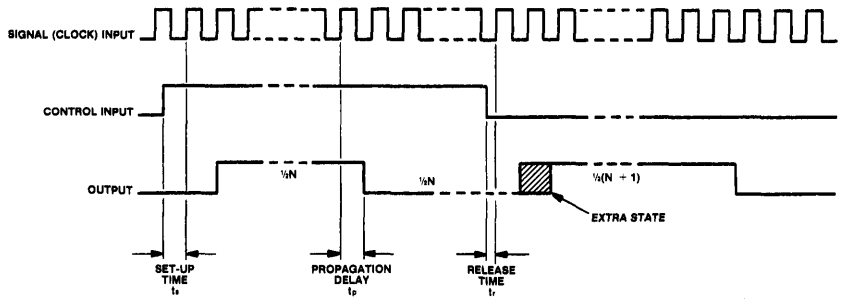
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = +4.95 to 5.45V, Temperature: T_{amb} = -40°C to +85°C

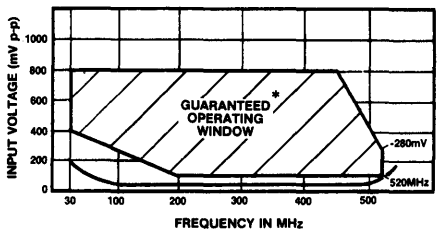
Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 100-280mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	C_L = 3pF; pins 2, 8 linked	1
Output high voltage	V_{OH}	(V_{CC} -1.2)		V	I_L = -0.2mA	1
Output low voltage	V_{OL}		1	V	I_L = 0.2mA	1
Control input high voltage	V_{INH}	3.3	8	V	÷N	1
Control input low voltage	V_{INL}	0	1.7	V	÷N + 1	1
Control input high current	I_{INH}		0.41	mA	V_{INH} = 8V	1
Control input low current	I_{INL}	-0.20		mA	V_{INL} = 0V	1
Clock to output delay	t_p		28	ns	C_L = 10pF	2
Set-up time	t_s	10		ns	C_L = 10pF	2
Release time	t_r	10		ns	C_L = 10pF	2

NOTES
1. Tested at 25°C only.
2. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷N mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷(N + 1) mode is obtained.

Fig.3 Timing diagram



*Tested as specified above.

Fig.4 Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

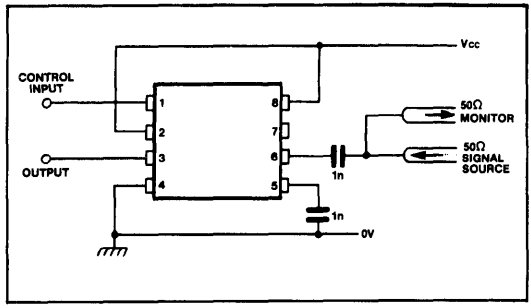


Fig.5 Toggle frequency test circuit

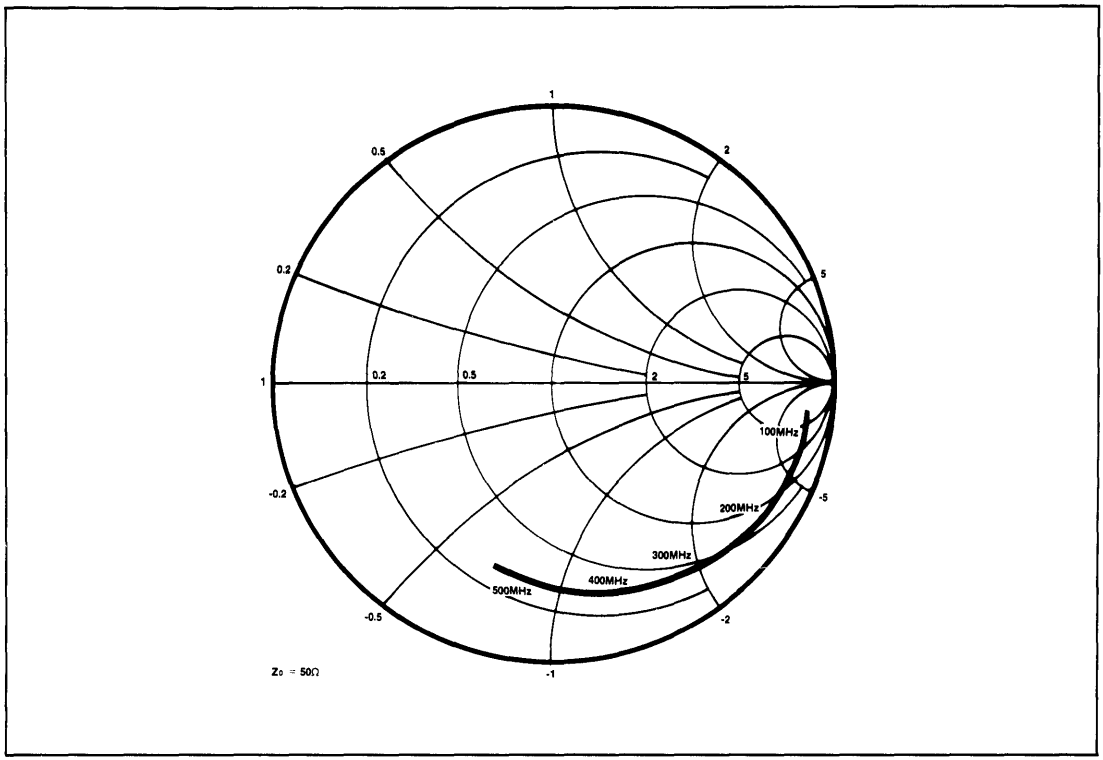


Fig.6 Typical input impedance

SP8789

225MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789 is a low power programmable ÷20/21 counter.It divides by 20, when the control input is in the high state and by 21 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

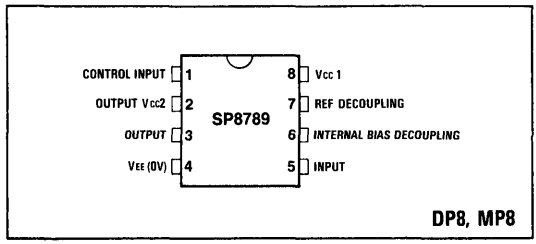


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
	13.5V Pin 8, Pin 7 decoupled
Storage temperature range:	-40°C to +85°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p
Vcc2:	Max. 10V

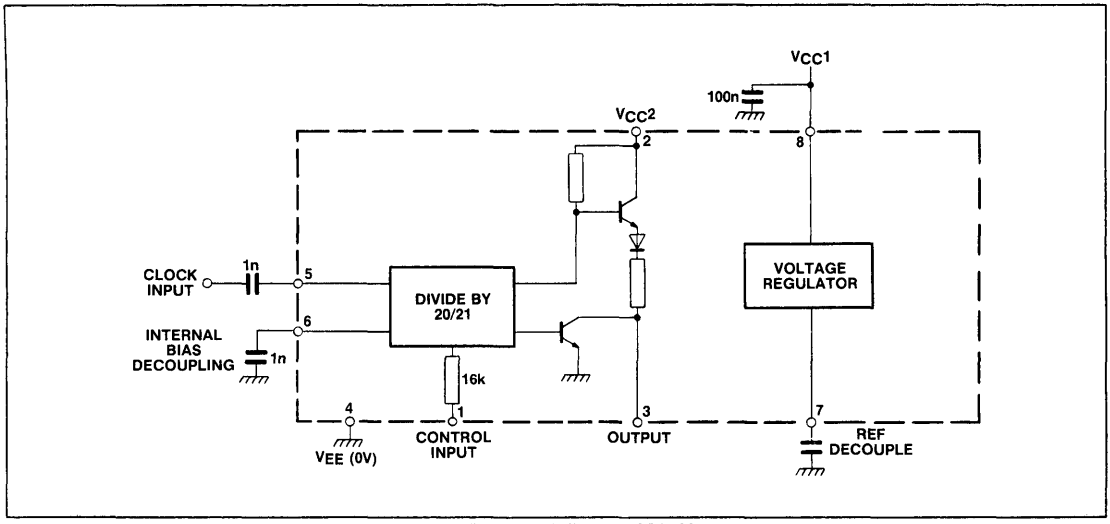


Fig.2 Functional diagram SP8789

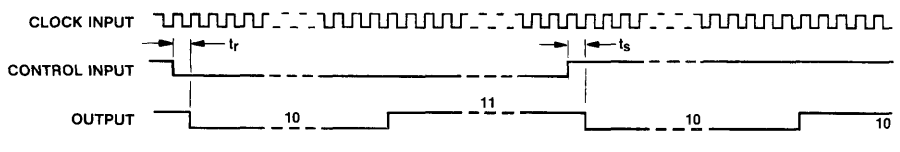
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.



TRUTH TABLE FOR CONTROL INPUTS

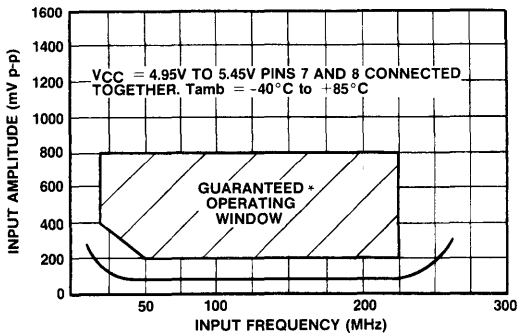
Control input	Division ratio
0	21
1	20

Fig.3 Timing diagram SP8789

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷20 mode is selected.

The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷21 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8789

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

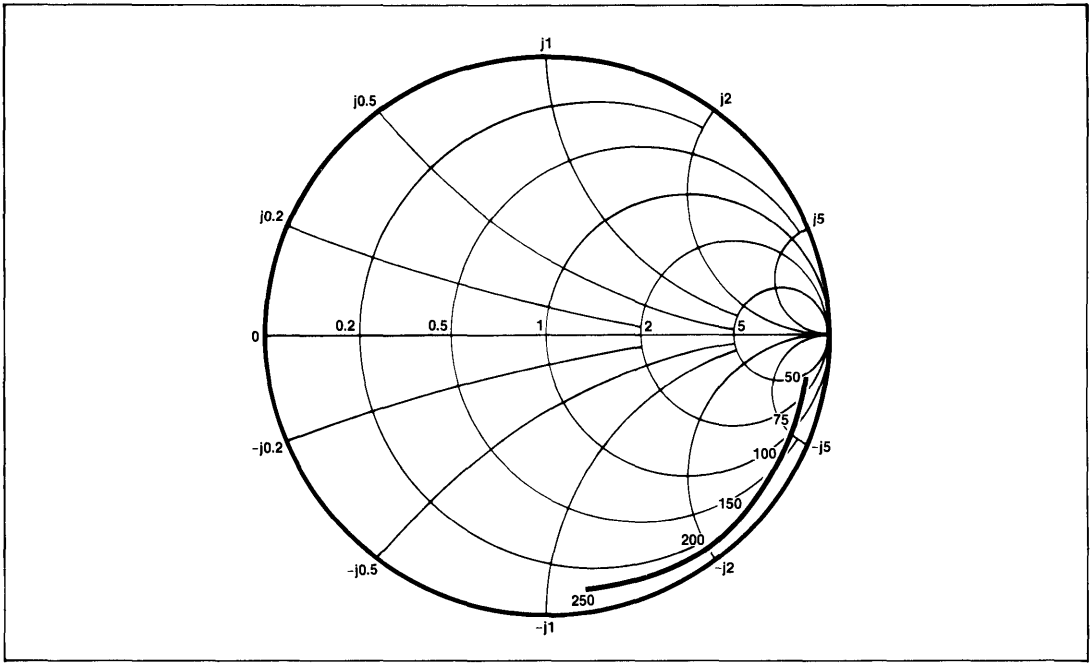


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

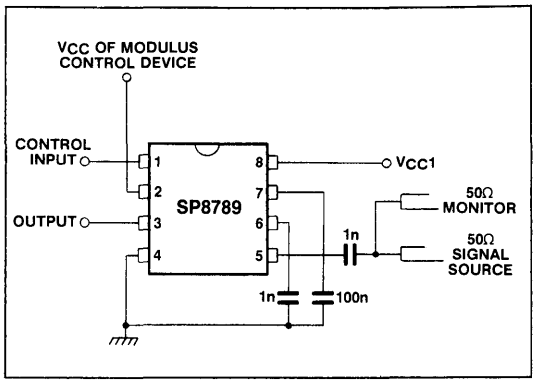


Fig.6 Toggle frequency test circuit

PLESSEY
Semiconductors

SP8792 225MHz ÷ 80/81
SP8793 225MHz ÷ 40/41

WITH ON-CHIP VOLTAGE REGULATOR

The SP8792 and SP8793 are low power programmable ÷80/81 and ÷40/41 counters, temperature range: -40° C to +85° C. They divide by 80(40) when control input is in the high state and by 81(41) when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

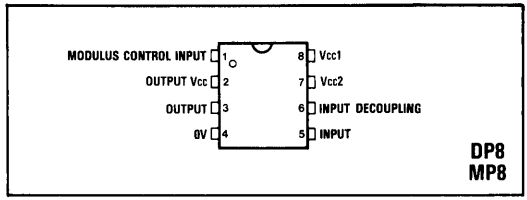


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage: +5.2V or 6.8V to 9.5V
- Power Consumption: 26mW

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-40°C to +85°C
Max. junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2 max	10V

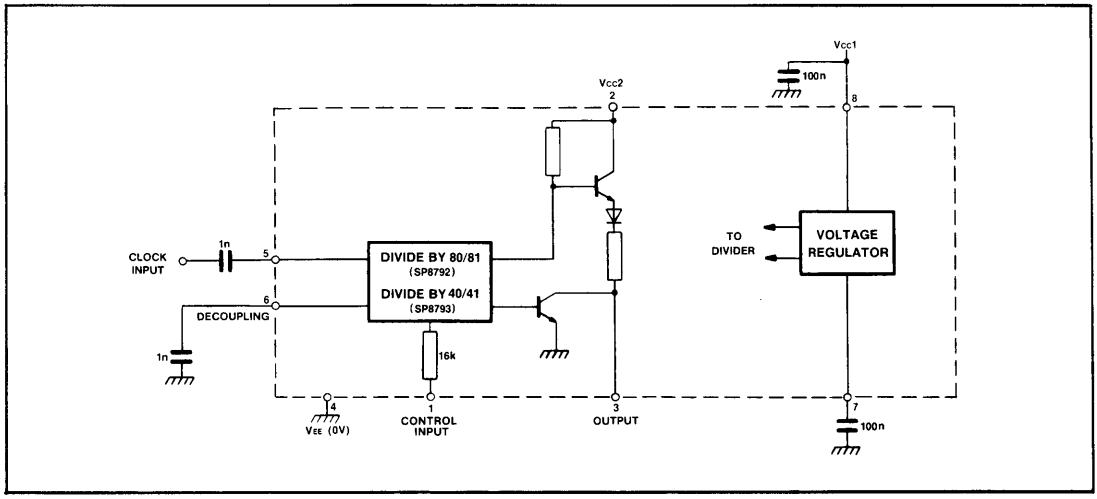


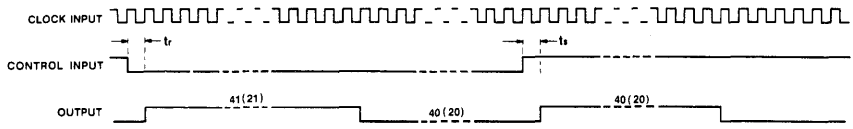
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V or 6.8-9.5V (See Operating Note 6) V_{EE} = 0V
Temperature: T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Input = 200-800mV p-p	Note 4
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input = 400mV p-p	Note 4
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC} = 4.95V I_{OH} = 100µA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 open or linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set up time	t_s	14		ns	25°C	Note 3
Release time	t_r	20		ns	25°C	Note 3
Clock to output propagation time	t_p		45	ns	25°C	Note 3

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

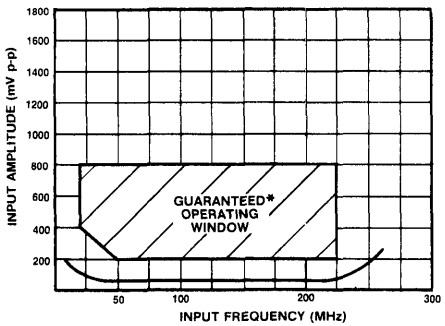


TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792	SP8793
0	81	41
1	80	40

Fig.3 Timing diagram SP8792/3

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure ÷80 or 40 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷81 or 41 mode is selected.



* Tested as specified above.

Fig.4 Input sensitivity SP8792/SP8793

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6, to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig. 5.
6. The internal regulator has its input connected to pin 8, while the internal reference voltage appears at pin 7 and should be decoupled. For use from a 5.2V supply, pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, pins 7 and 8 should be separately decoupled, and the supply voltage applied to pin 8.
7. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.

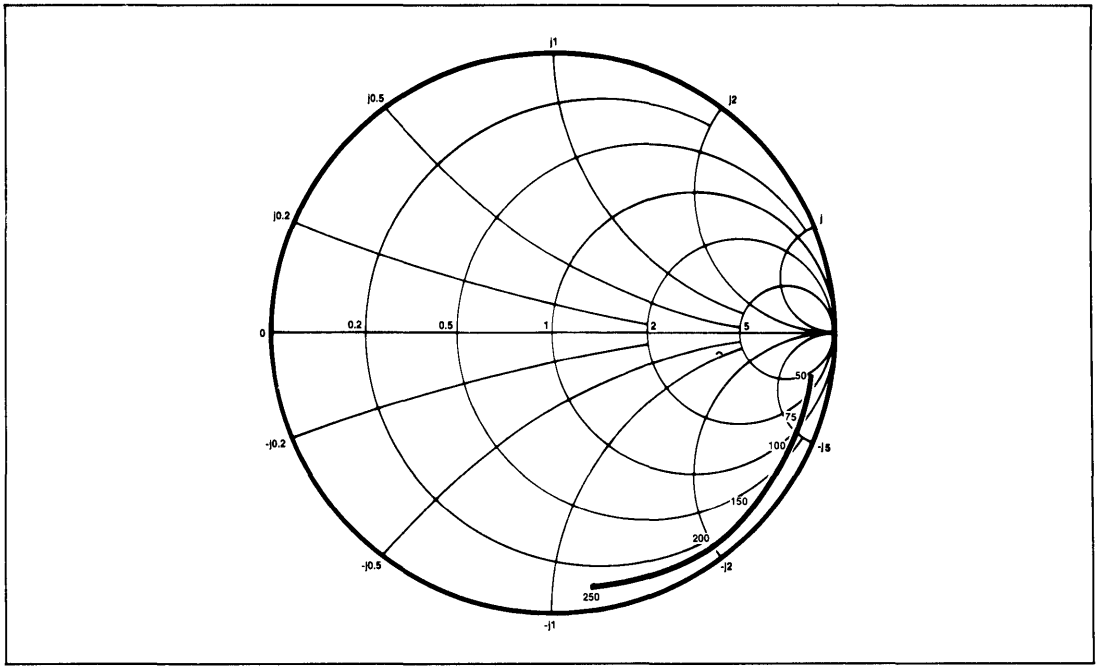


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

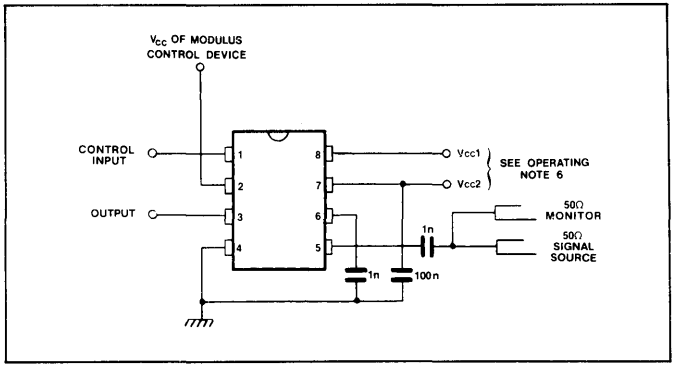


Fig.6 Toggle frequency test circuit

SP8795

225MHz ÷ 32/33 TWO MODULUS DIVIDER

The SP8795 is a low power programmable ÷32/33 counter.It divides by 32 when the control input is in the high state and by 33 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

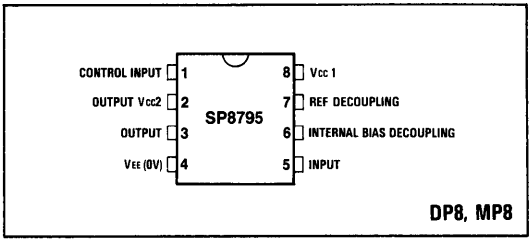


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
	13.5V Pin 8, Pin 7 decoupled
Storage temperature range:	-40°C to +85°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p
Vcc2:	Max. 10V

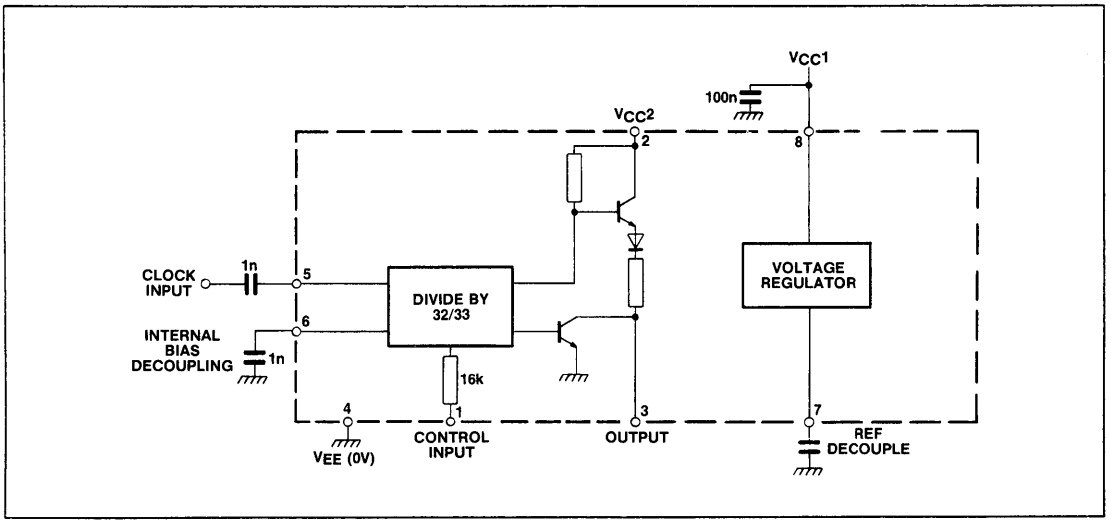


Fig.2 Functional diagram SP8795

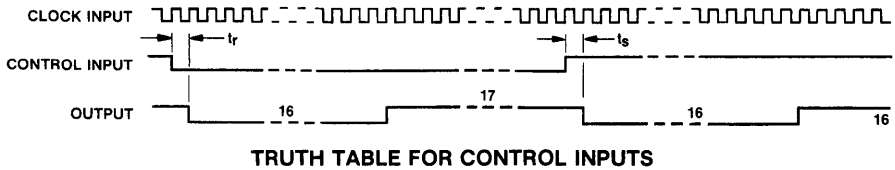
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.



TRUTH TABLE FOR CONTROL INPUTS

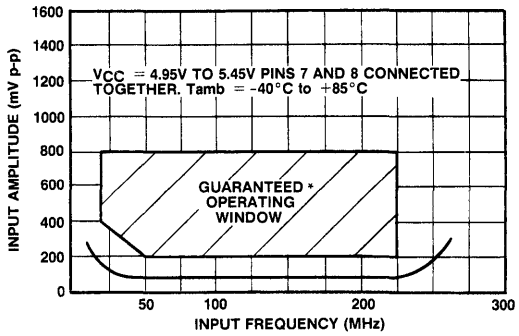
Control input	Division ratio
0	33
1	32

Fig.3 Timing diagram SP8795

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷32 mode is selected.

The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷33 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8795

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

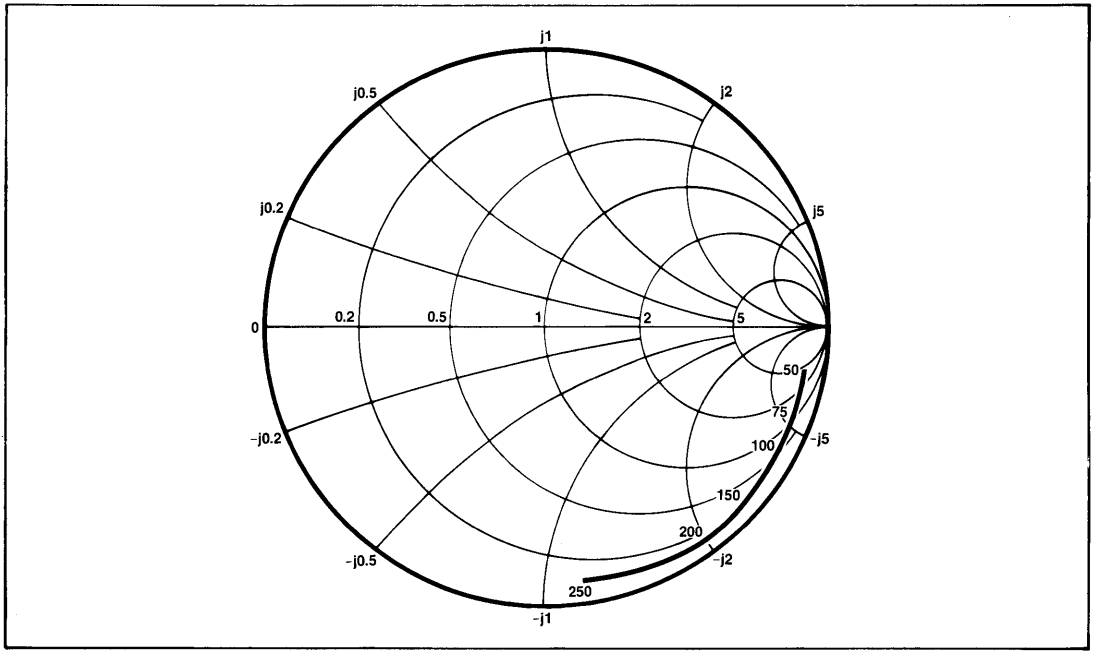


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

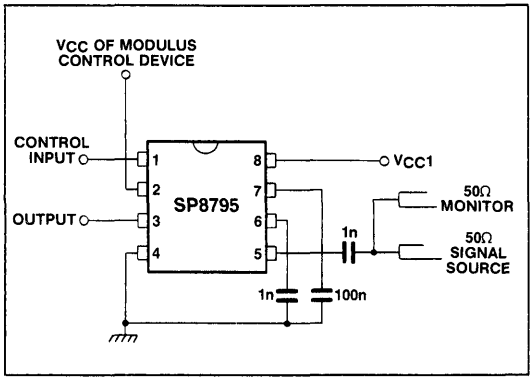


Fig.6 Toggle frequency test circuit

SP8799

225MHz ÷ 10/11 TWO MODULUS DIVIDER

The SP8799 is a low power programmable ÷10/11 counter.It divides by 10 when the control input is in the high state and by 11 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

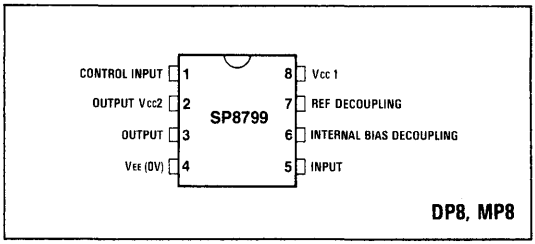


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply voltage: +5.2V or 6.8 to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	6.0V Pins 7 & 8 tied
	13.5V Pin 8, Pin 7 decoupled
Storage temperature range:	-40°C to +85°C
Max. junction temperature:	+175°C
Max. clock input voltage:	2.5V p-p
Vcc2:	Max. 10V

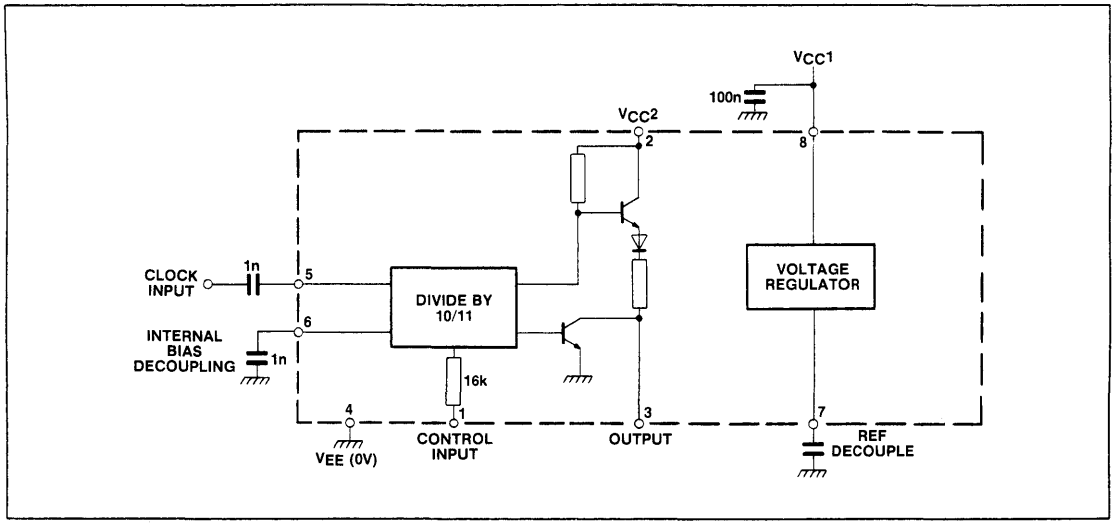


Fig.2 Functional diagram SP8799

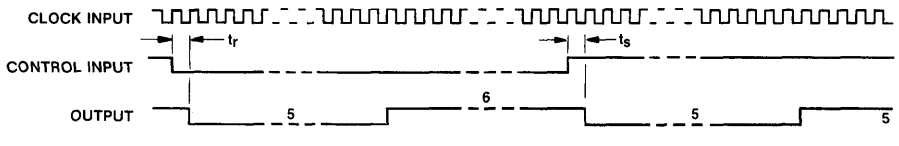
ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage: V_{CC} 1 & 2 = 5.2V ± 0.25V or 6.8V to 9.5V (see Operating Note 7);
V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked V_{CC} = 4.95V I_{OH} = 100μA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested only at 25°C.



TRUTH TABLE FOR CONTROL INPUTS

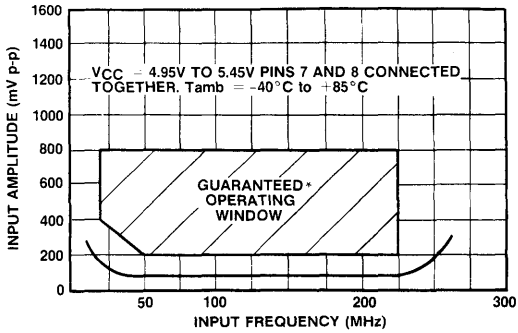
Control input	Division ratio
0	11
1	10

Fig.3 Timing diagram SP8799

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and next L→H clock pulse transition to ensure ÷10 mode is selected.

The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷11 mode is selected.



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity SP8799

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

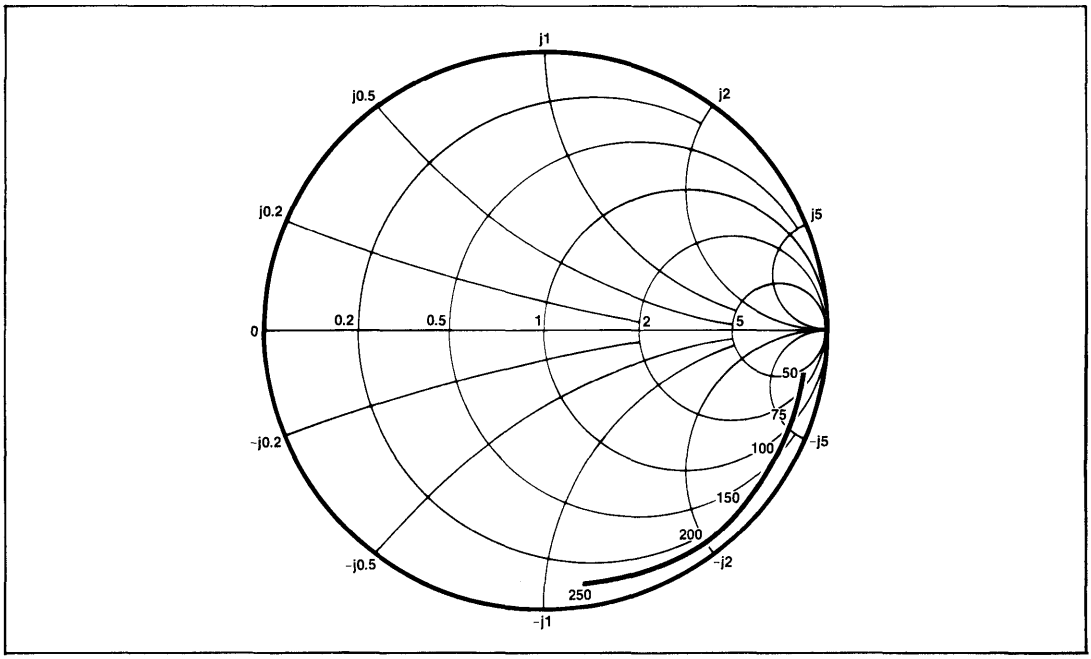


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

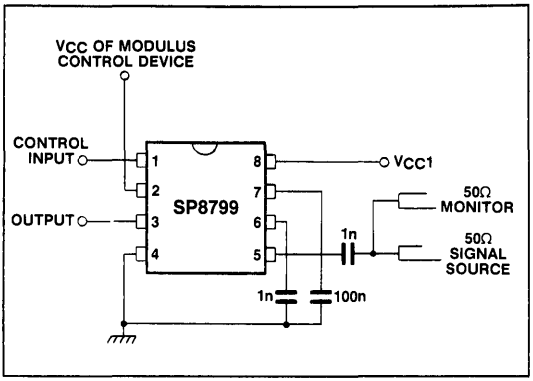


Fig.6 Toggle frequency test circuit

NJ8820

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820 is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

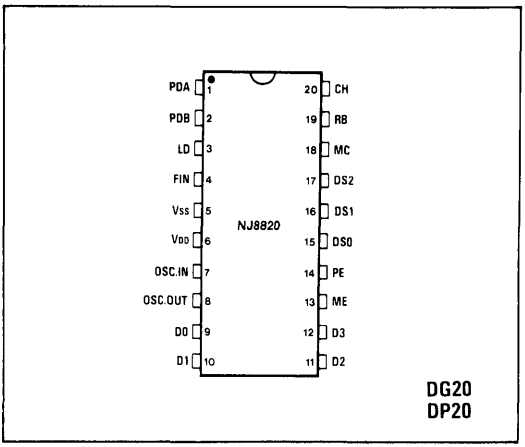


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

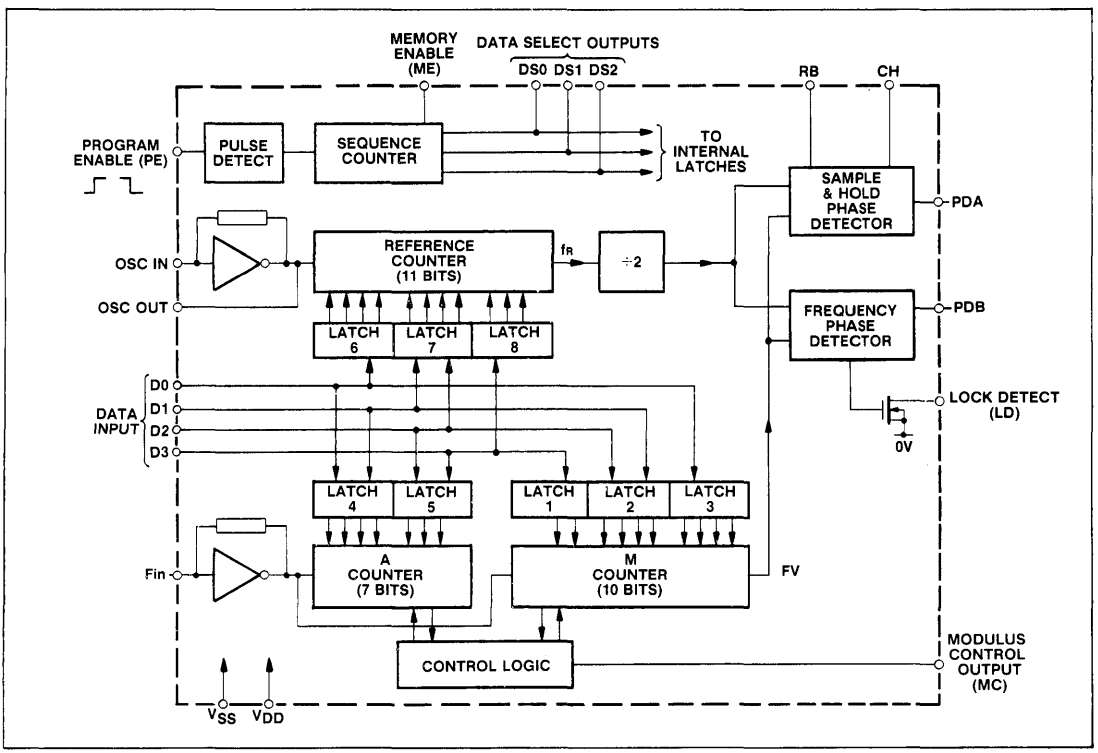


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V Temperature range -30°C to +70°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current		3.5	5	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1	mA	FOSC, FIN = 1.0MHz } square wave
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS} Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_w	5			μs	Pulse to V_{SS} or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs. 2. All counters have outputs directly synchronous with their respective clock rising edges. 3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds. 4. To ensure correct operation of power-on programming. 5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
13	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15,16,17	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M $\geqslant$A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 7V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature: -65° C to +150° C (DG Package)
Storage temperature: -55° C to +125° C (DP Package)

*Except on open drain outputs where this is 7V.

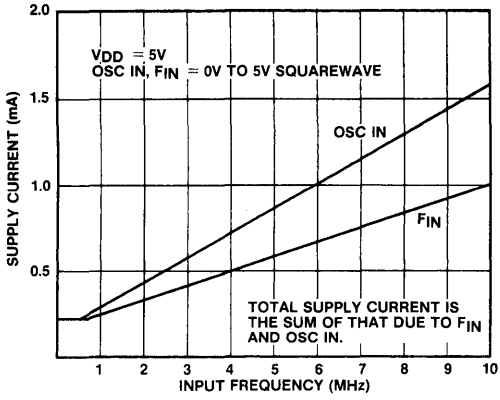


Fig.3 Typical supply current versus input frequency

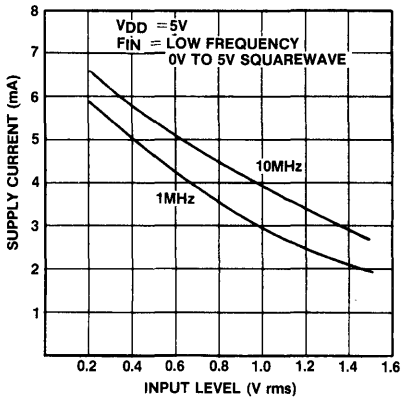


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Program information can be obtained from an external ROM or PROM under control of the NJ8820. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability as shown in Fig.5. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data map, data read cycle and timing diagram appears as Figs. 6 to 8. Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because the higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

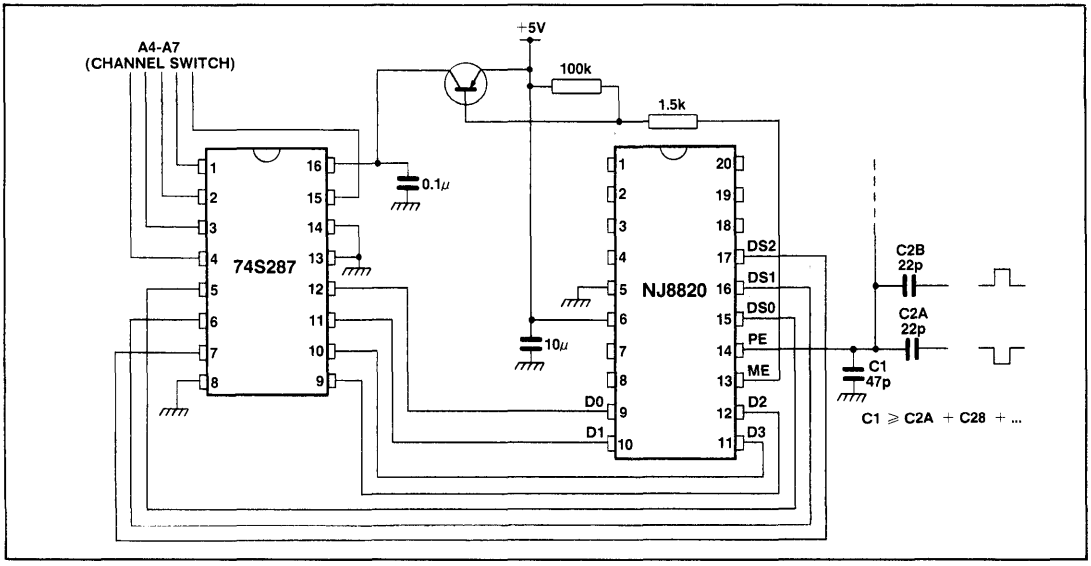


Fig.5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.6 Data map

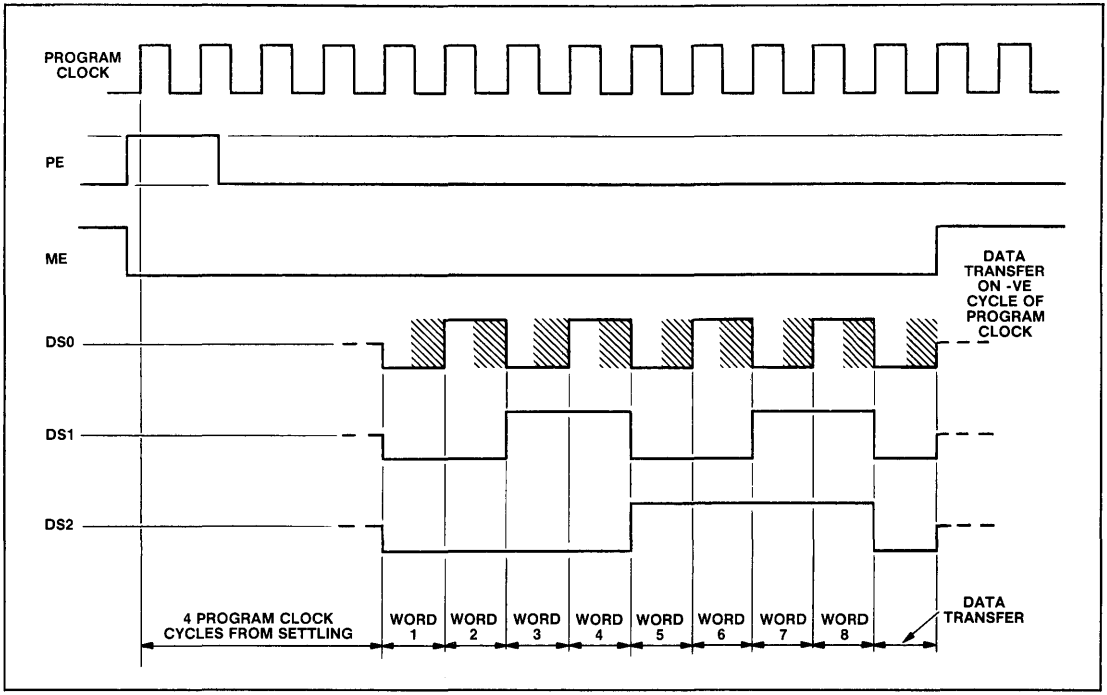


Fig.7 Data selection

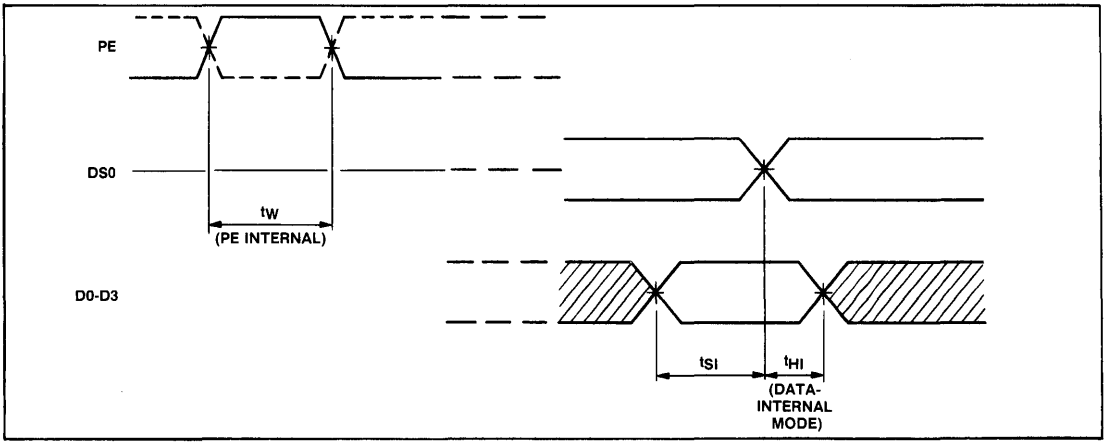


Fig.8 Timing diagram

PHASE COMPARATORS

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

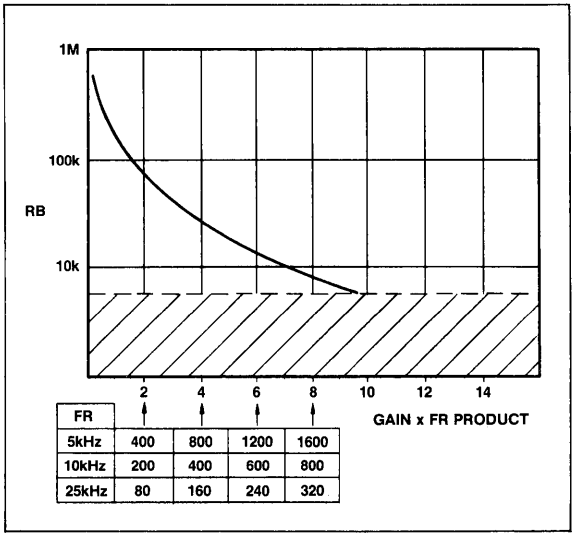
An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of gain frequency product by the desired frequency.

The output from these phase detectors should be combined and filtered to generate a single control voltage to drive the VCO as in Fig.8.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

APPLICATION EXAMPLE

An application example for a synthesiser for operation up to 520MHz is given in Fig.10. This gives up to 32 channels with a maximum supply current of 17mA, (typically 12mA) at 520MHz excluding the VCO. With careful construction the circuit is capable of providing sideband attenuation in excess of 90dB with lock-times of only a few milliseconds for a 1MHz frequency step.

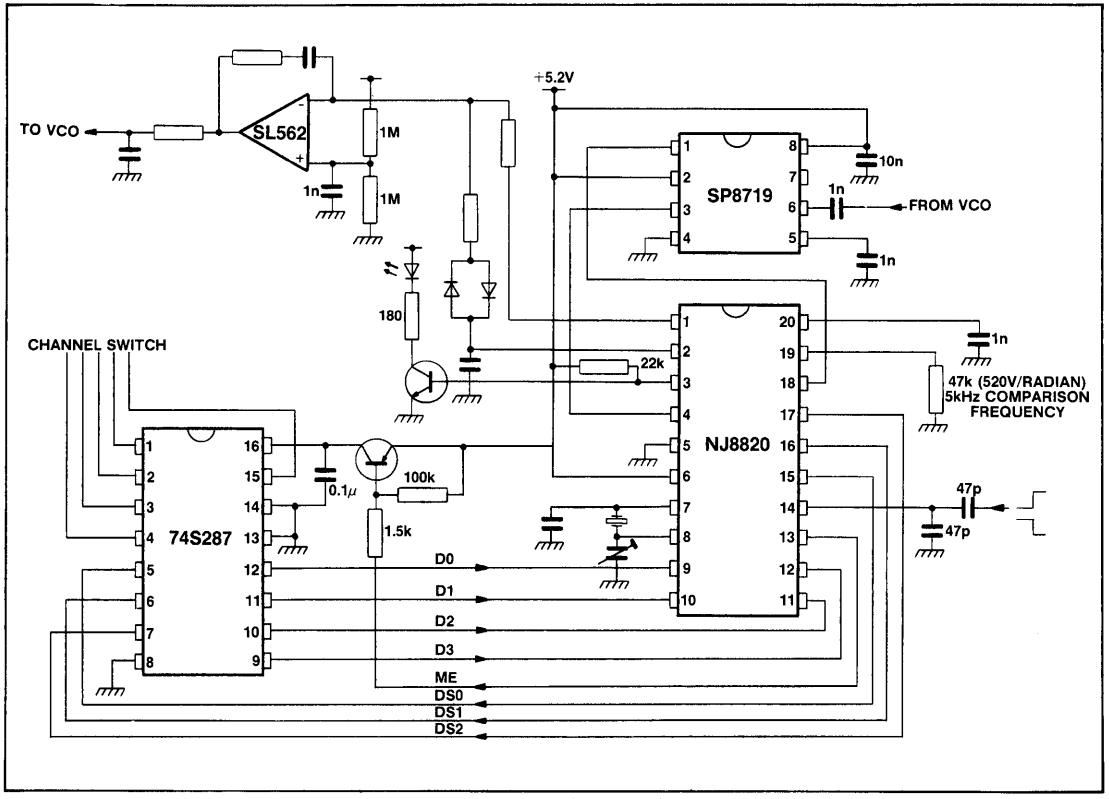


Fig.10 Application example

NJ8820GG

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820GG is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words in one of two modes. Data may be read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

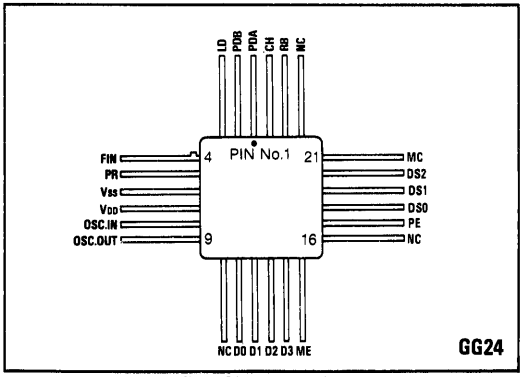


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency

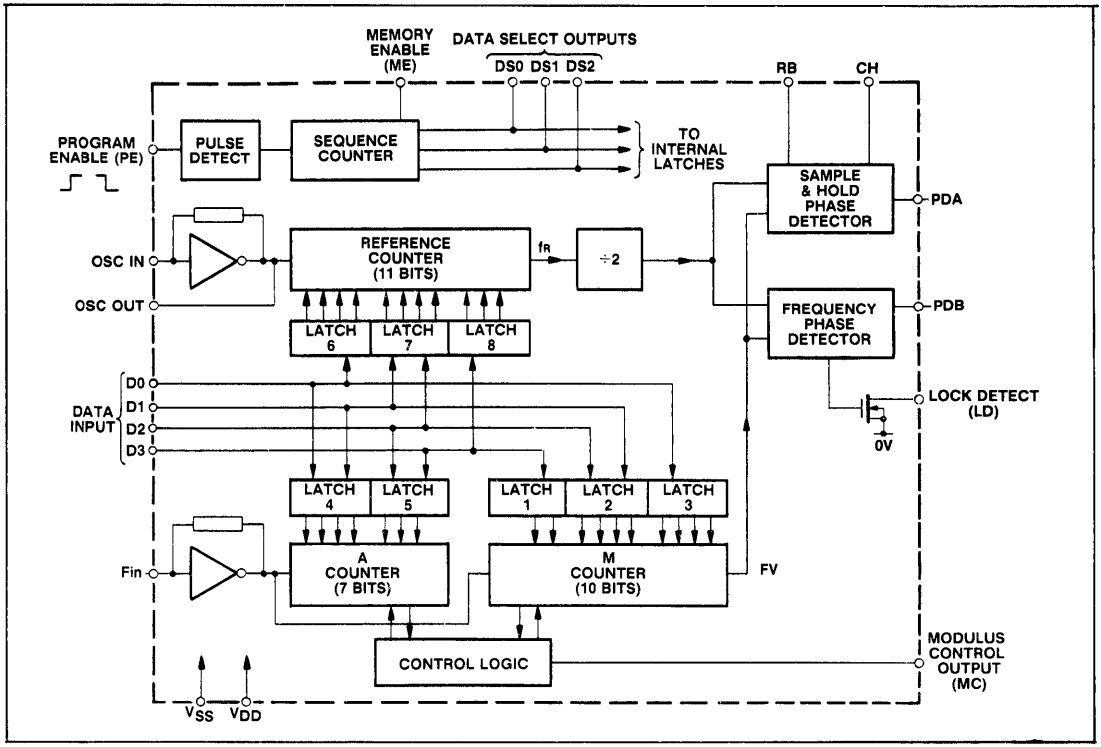


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V Temperature range -30° C to +70° C

DC Characteristics at V_{DD} = 5V

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current		3.5	5	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1	mA	FOSC, FIN = 1.0MHz } square wave
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally $V_{DD}/2$)

AC Characteristics

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS} Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_w	5			μs	Pulse to V_{SS} or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. To ensure correct operation of power-on programming.
5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	PR	This pin allows selection between programming modes. For internal control the pin should be left open circuit and should be grounded to allow external control.
6	V_{SS}	Negative supply (normally ground)
7	V_{DD}	Positive supply
8,9	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
15	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
17	PE	This pin has two functions. In internal mode a positive or negative pulse AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner. In external mode this pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
18,19,20	DS0-DS2	Internally generated three-state data select outputs which may be used to address external memory. In external mode these pins became inputs to control the addressing of data latches.
21	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ⩾A. Where every possible channel is required, the minimum division ratio should be N^2-N.
23	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
24	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 7V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature: -65°C to +150°C

*Except on open drain outputs where this is 7V.

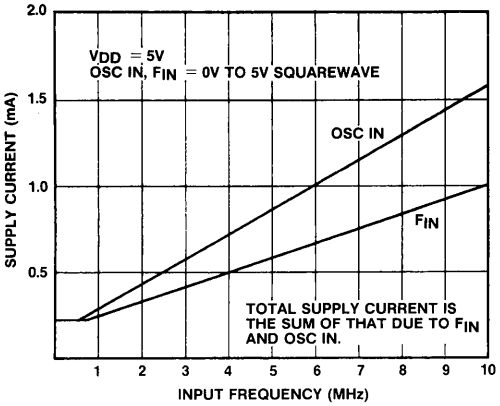


Fig.3 Typical supply current versus input frequency

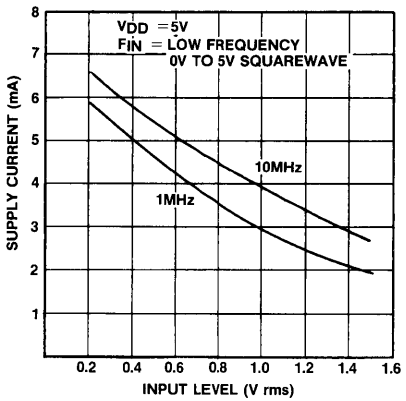


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING IN INTERNAL MODE

This mode of operation allows program information to be obtained from an external ROM or PROM under control of the NJ8820GG. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired.

Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because of higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

PROGRAMMING IN EXTERNAL MODE

The external mode of programming is selected by grounding the program pin, (PR). In this mode timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is as Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.8.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

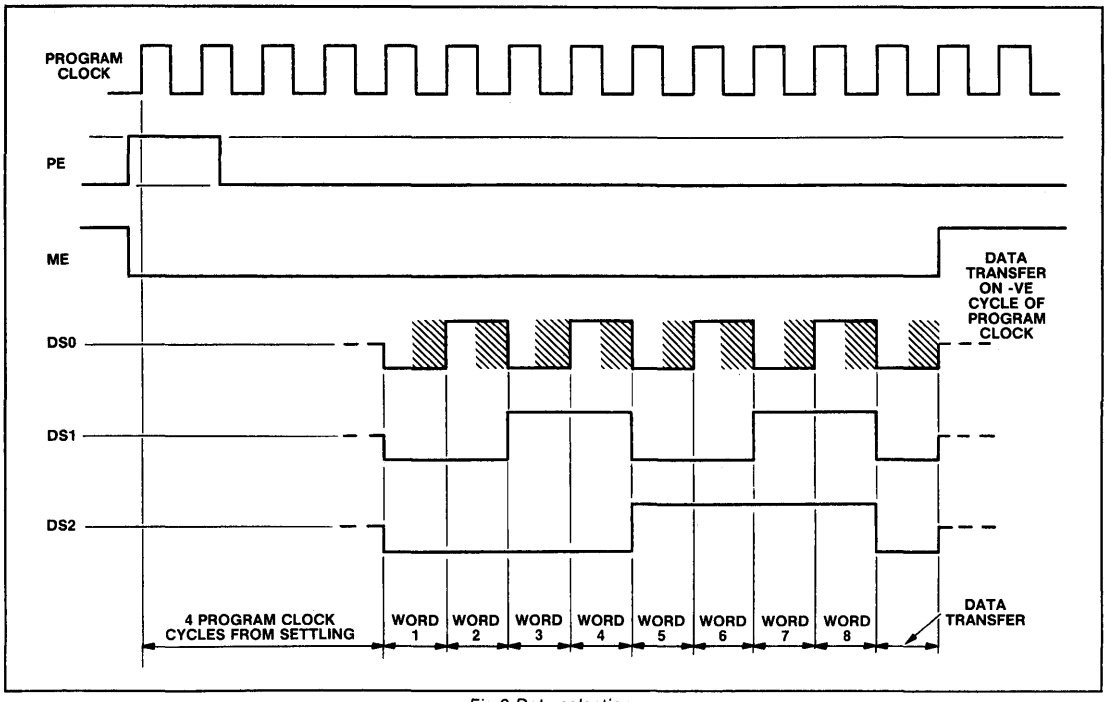


Fig.6 Data selection

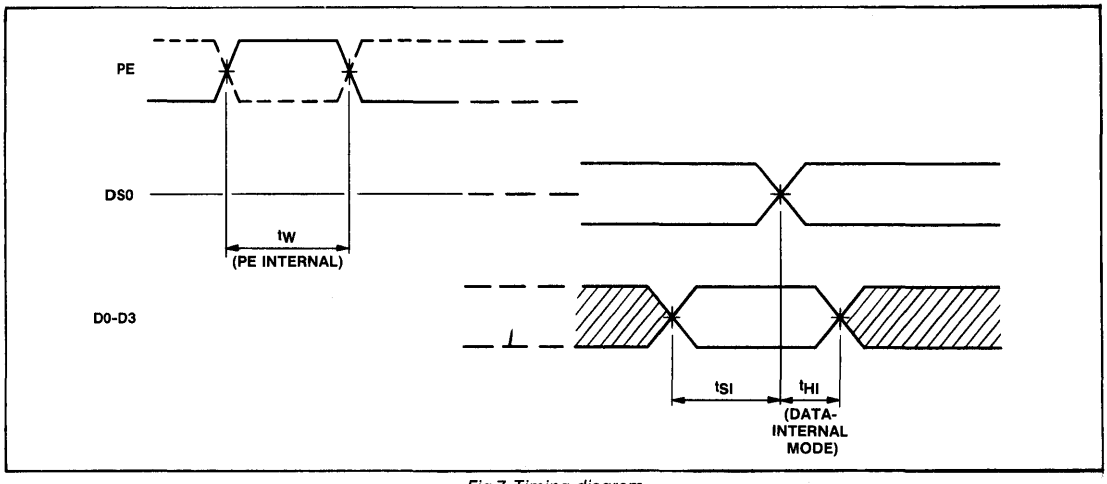


Fig.7 Timing diagram

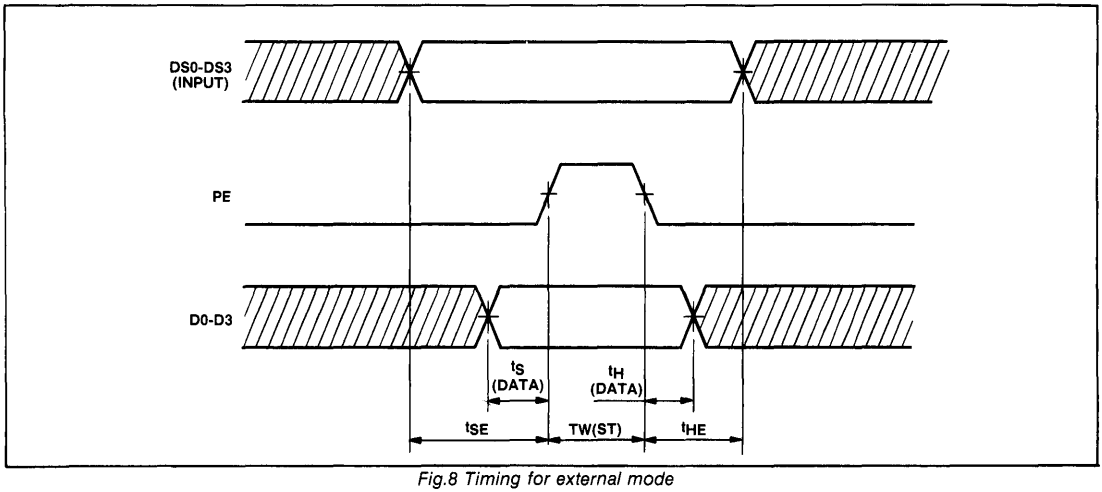


Fig.8 Timing for external mode

PHASE COMPARATORS

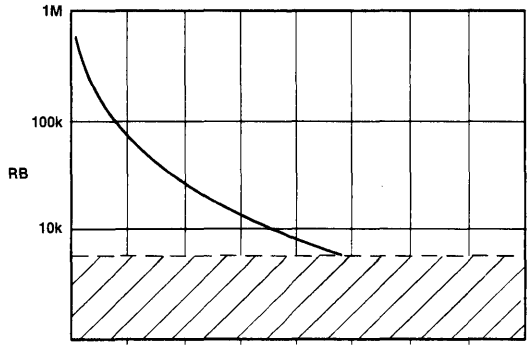
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-1/2})]}{2 \times \pi\ 50\text{x}10^{12} \times RB\text{x}FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

NJ8821

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE)

The NJ8821 is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

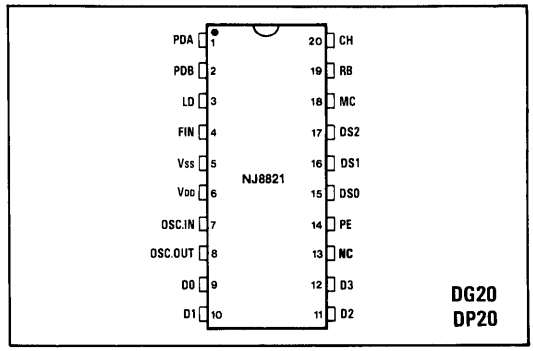


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency

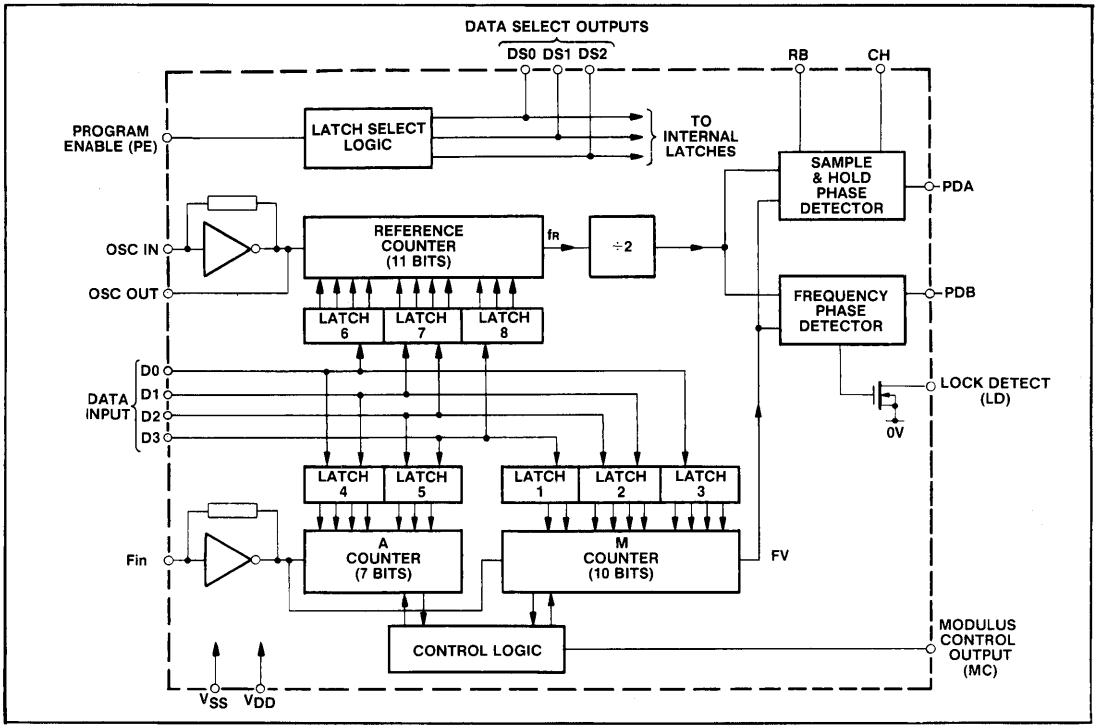


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range -30°C to +70°C for DP
Temperature range -40°C to +85°C for DG

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1	mA	FOSC, FIN = 1.0MHz } square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}.Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M $\geq$A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 7V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature: -65° C to +150° C (DG Package)
Storage temperature: -55° C to +125° C (DP Package)

*Except on open drain outputs where this is 7V.

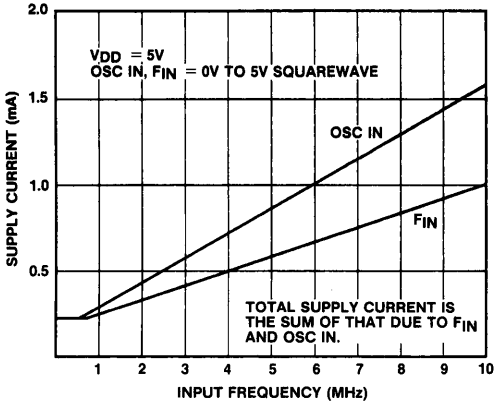


Fig.3 Typical supply current versus input frequency

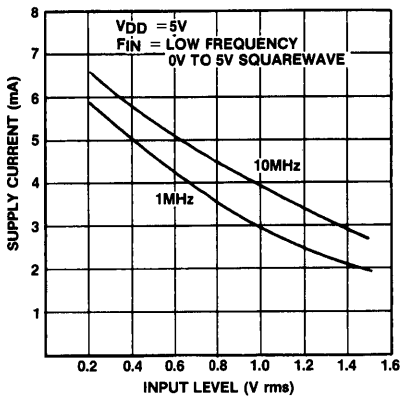


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

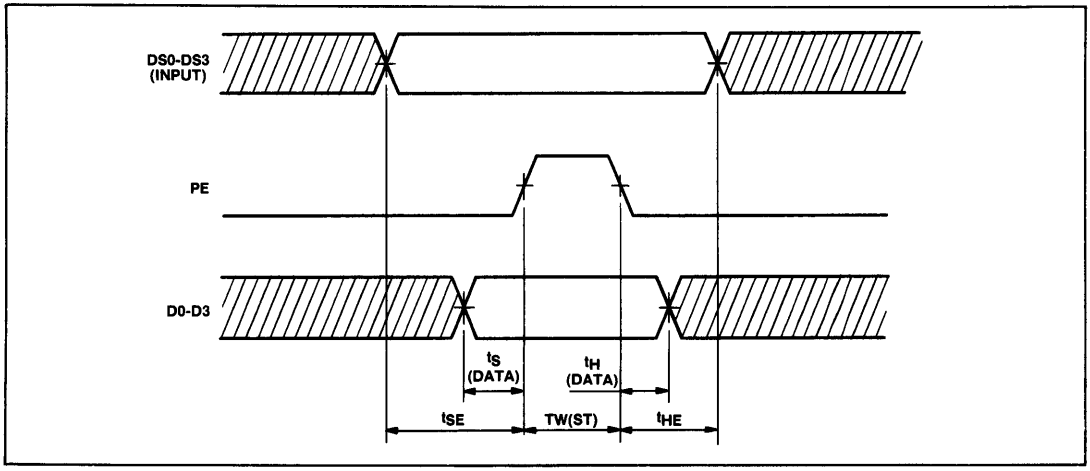


Fig.6 Timing diagram

PHASE COMPARATORS

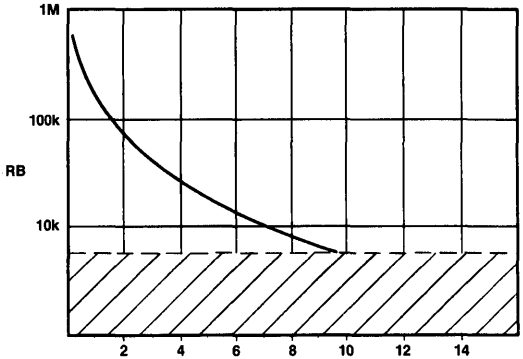
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-\frac{1}{2}})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

NJ8821GG

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE)

The NJ8821GG is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

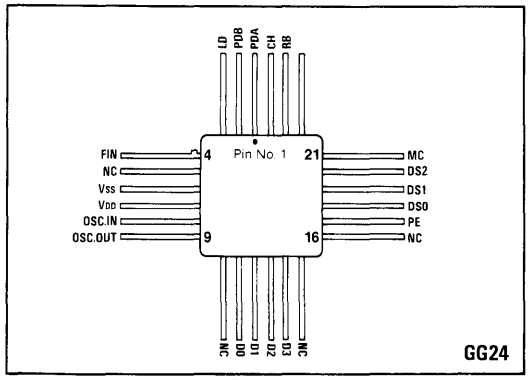


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- > 10MHz Input Frequency

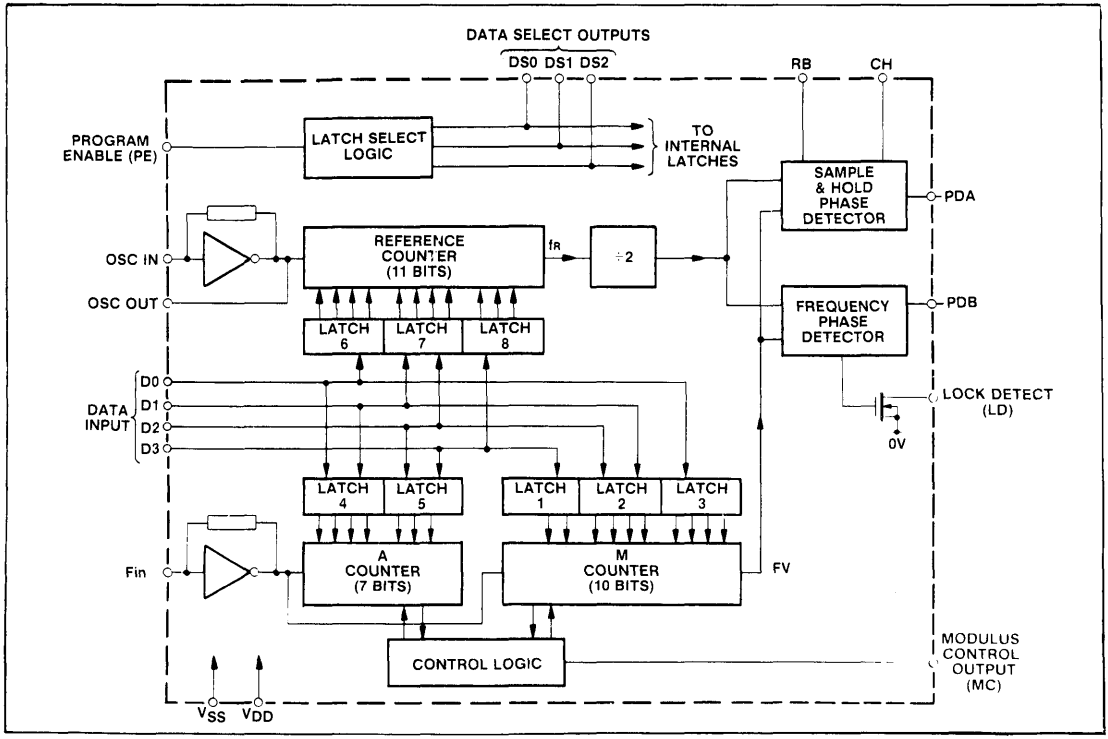


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range -30°C to +70°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1	mA	FOSC, FIN = 1.0MHz } square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}. Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
6	V_{SS}	Negative supply (normally ground)
7	V_{DD}	Positive supply
8,9	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12,13,14	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
17	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
18,19,20	DS0-DS2	Data-select inputs to control the addressing of data latches.
21	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N+1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M $\geqslant$A. Where every possible channel is required, the minimum division ratio should be N^2-N.
23	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
24	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 7V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature: -65° C to +150° C

*Except on open drain outputs where this is 7V.

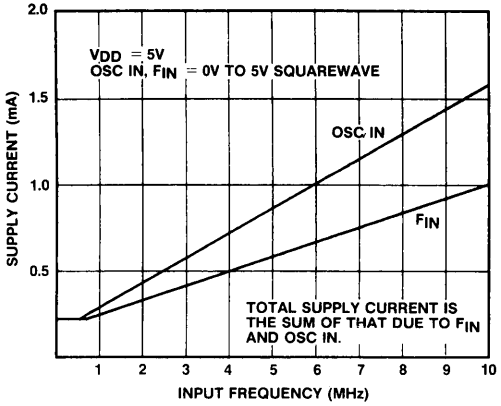


Fig.3 Typical supply current versus input frequency

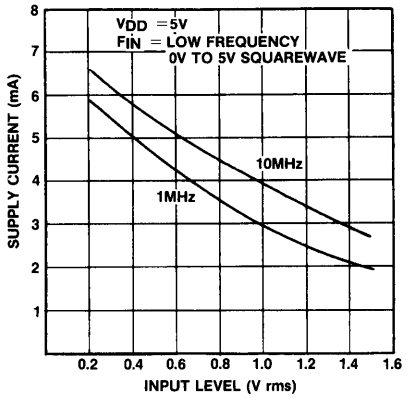


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

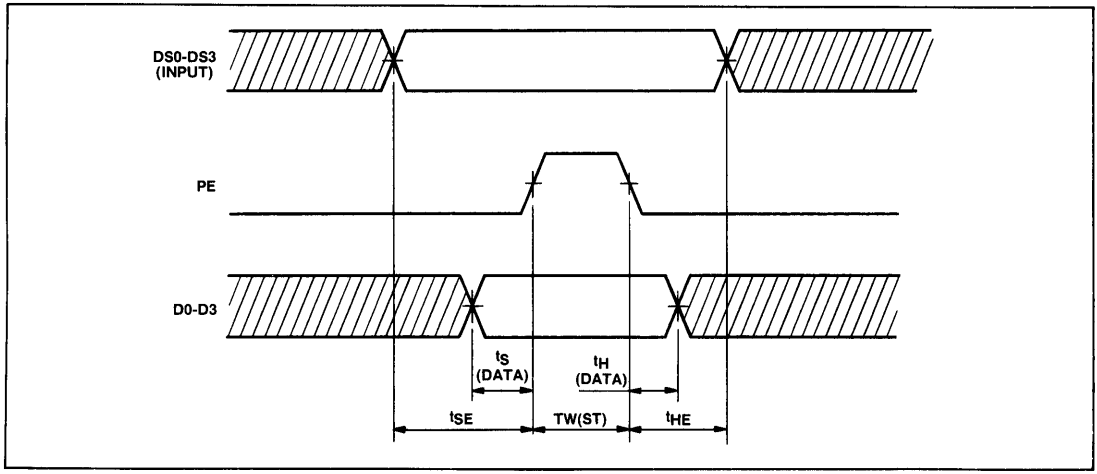


Fig.6 Timing diagram

PHASE COMPARATORS

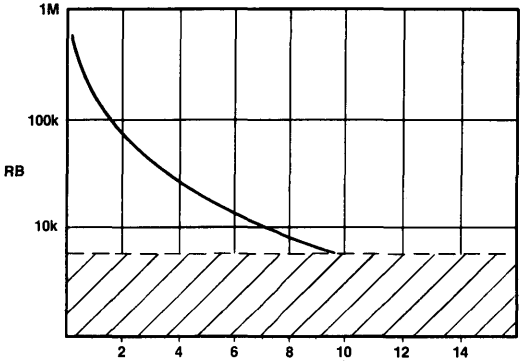
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

NJ8822

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ8822 is a synthesiser circuit fabricated with the 2-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessor. Although 28 bits of data are initially required to program all counters subsequent updating can be abbreviated to 17 bits when only the 'A' and 'M' counters require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8704 series to produce a universal binary coded synthesiser for up to 950MHz operation.

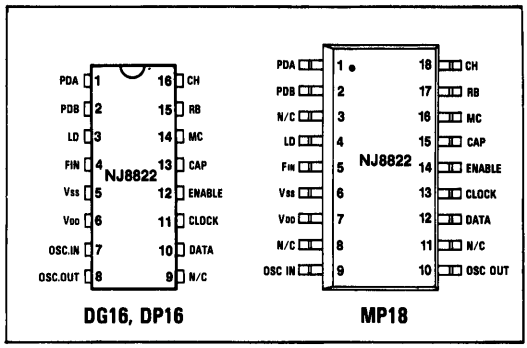


Fig.1 Pin connections - top view, not to scale

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >i10MHz Input Frequency

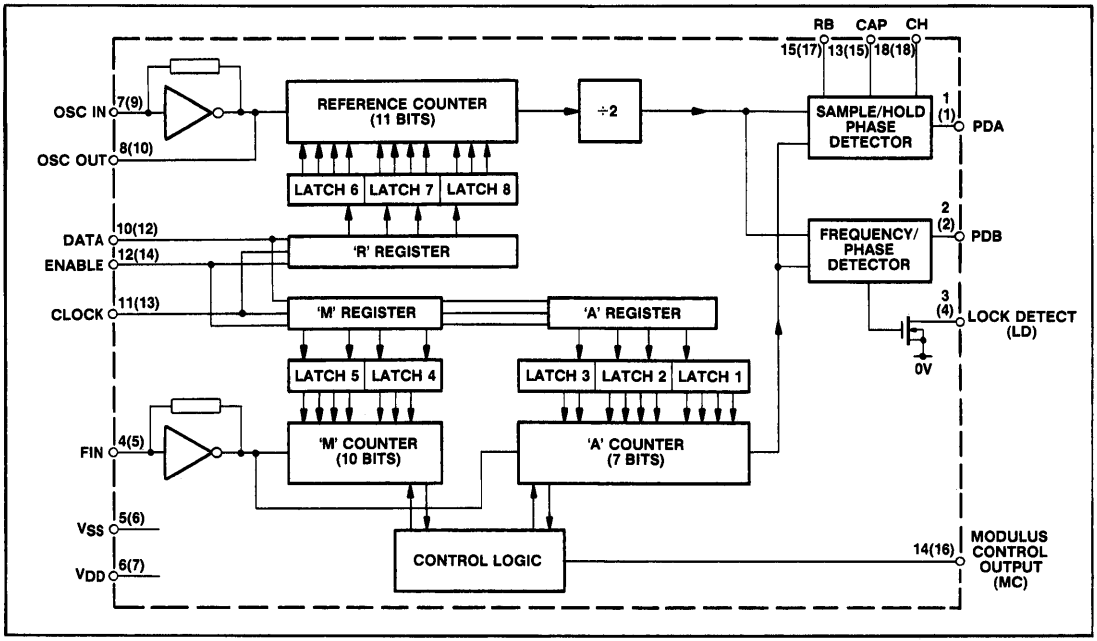


Fig.2 Block diagram. Pin numbers for MP package are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-Vss 5V ± 0.5V
Temperature range -30°C to +70°C for DP, MP : Temperature range -40°C to +85°C for DG

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		6.3	7	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1	mA	FOSC, FIN = 1MHz } square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB OUTPUT					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	18MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10			MHz	V_{DD} = 5V, Input squarewave V_{DD}-Vss, 25°C
Propagation delay, clock to modulus control		30	50	ns	Note 2
Programming Inputs					
Clock high time, t_{CH}	0.5			μs	All timing periods are referenced to the negative transition of the clock waveform
Clock low time, t_{CL}	0.5			μs	
Enable set-up time, t_{ES}	0.2		t_{CH}	μs	
Enable hold time, t_{EH}	0.2			μs	
Data set-up time, t_{DS}	0.2			μs	
Data hold time, t_{DH}	0.2			μs	
Clock rise and fall times	0.2			μs	
Positive going threshold, V_T+	3			V	TTL compatible
Negative going threshold, V_T-			2	V	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	
Hold capacitor, CH			1	nF	Note 3
Programming capacitor, CAP			1	nF	
Output resistance, PDA			5	kΩ	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. The finite output resistance of the internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time constant of 5 microseconds.
4. The inputs to the device should be at logic '0' when power is applied if latch up conditions are to be avoided. This includes the signal/osc. frequency inputs.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-Vss): -0.5V to 7V
Input voltage at any pin: *Vss -0.3V to V_{DD} +0.3V
Storage temperature: -65°C to +150°C (DG Package)
Storage temperature: -55°C to +125°C (DP and MP Packages)

*Except on open drain outputs where this is 7V.

PIN DESIGNATION

Pin No. DG,DP	Pin No. MP	Name	Description
1	1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. Voltage increases as FV (FV is the output from the 'M' counter) phase lead increases and decreases as FR (FR is the output from the reference counter) phase lead increases. Output is linear over only a narrow phase window determined by gain (programmed by RB). In a type 2 loop, this pin is at (V_{DD} - V_{SS})/2 when the system is in lock.
-	3	N/C	Not connected.
2	2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses. FV < FR or FR leading: negative pulses. FV = FR and phase error within PDA window: high impedance.
3	4	LD	An open drain lock detect output at low level when phase error is within PDA window (in lock); high impedance at all other times.
4	5	FIN	The input to the main counters. It is normally driven from a prescaler which may be AC coupled or, when a full logic swing is available, may be DC coupled.
5	6	V_{SS}	Negative supply (ground).
6	7	V_{DD}	Positive supply (normally 5V).
-	8	N/C	Not connected.
7,8	9,10	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. The addition of a 220 ohm resistor between Pin 8 and the crystal will improve stability. An external reference signal may alternatively be applied to OSC.IN. This may be a low-level signal, AC coupled, or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6 to 4094 in steps of 2, with the division ratio being twice that programmed.
9	-	N/C	Not connected.
10	12	DATA	Information on this input is transferred to the internal latches during the appropriate data read time slot. Data is high for a '1' and low for a '0'. There are three data words which control the NJ8822, MSB is first in the order, 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).
11	13	CLK	Data is clocked in on the negative transition of the clock waveform. If less than 28 negative clock transitions have been received when the enable line goes low (i.e. only 'M' and 'A' will have been clocked in) then the 'R' counter latch will remain unchanged and only 'M' and 'A' will be transferred from the input shift register to the counter latches. This will protect the 'R' counter from being corrupted by any glitches on the clock line after only 'M' and 'A' have been loaded. If 28 negative transitions have been counted then the 'R' counter will be loaded with the new data.
12	14	ENABLE	When the enable is low the data and clock inputs are disabled internally. As soon as the enable is high the data and clock input are enabled and data may be clocked into the device. The data is transferred from the input shift register to the counter latches on the negative transition of the enable input and both inputs to the phase detector are synchronised to each other. Enable transitions only allowed when CLK is high.
13	15	CAP	This pin allows an external capacitor to be put in parallel with the ramp capacitor, and allows further programming of the device. (This capacitor is connected from CAP to V_{SS}).
14	16	MC	Output for controlling an external dual modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N + A where N and N + 1 represent the dual modulus prescaler values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷ 128/129. The programming range of the 'M' counter is 3-1023 and for correct program operation M ⩾ A. Where every possible channel is required, the minimum division ratio should be N^2 - N.
15	17	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
16	18	CH	An external hold capacitor should be connected between this pin and V_{SS}.

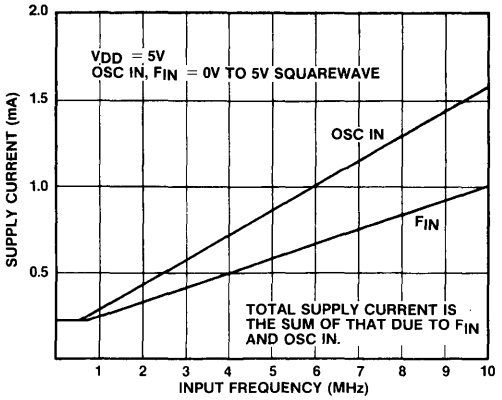


Fig.3 Typical supply current v. input frequency

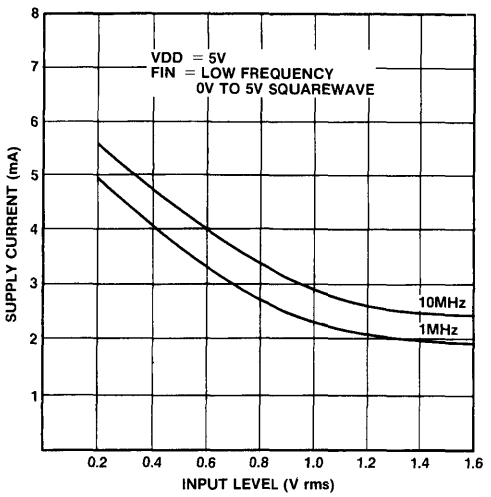


Fig.4 Typical supply current v. input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in the three latches.

Taking the enable pin high will transfer the data from the pin into the registers, 'R', 'A', 'M'.

Taking the enable pin low will transfer the data from the register to the latches and into the counter (on the negative enable edge). The three data words are input into the register, in order 'A' - (7 bits), 'M' - (10 bits), 'R' - (11 bits).

If less than 28 negative clock transitions have been received when the enable goes low then only the 'A' - (7 bits), 'M' - (10 bits) will be transferred to the latches and the 'R' - (11 bits) latch will remain unchanged.

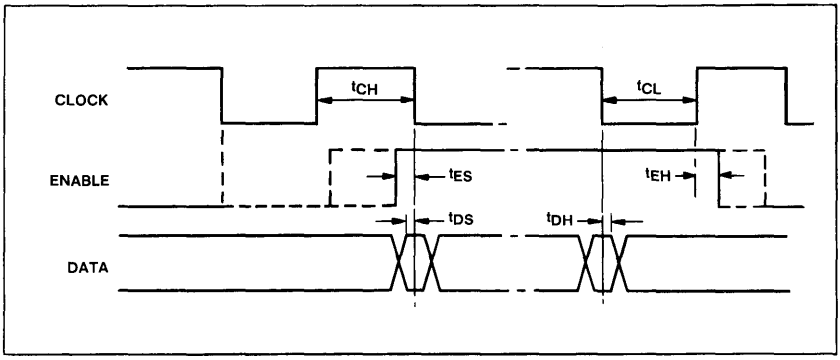


Fig.5 Timing diagram showing timing periods required for correct operation

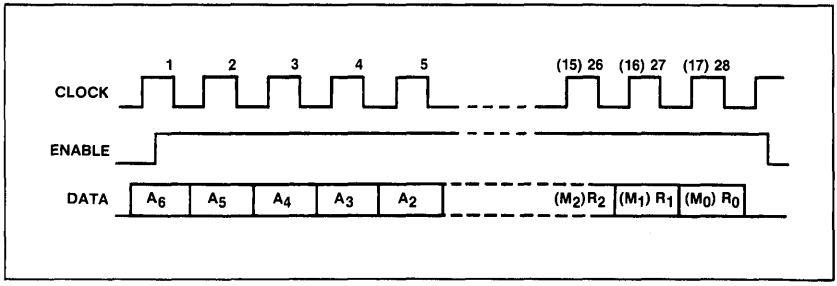


Fig.6 Timing diagram showing programming details

PHASE COMPARATORS

Noise output from a synthesiser loop is related to loop gain $K_\Phi K_{V/P}$, where K_Φ is phase detector constant (volts/rad), K_V is the VCO constant (rad-secs/volt) and P is the overall loop division ratio. When P is large and the loop gain is low, noise may be reduced by employing a phase comparator with a high gain. The sample and hold phase detector within the NJ8822 has both a high gain and uses a double sampling technique to reduce spurious ouputs to a low level.

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels.

This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error.

The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB and a capacitor, CAP.

An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2\pi\,[CAP + 50\times10^{-12}] \times RB \times FR}$$

The value of RB and CAP should be chosen to give the required gain at the reference frequency used. Fig.8 shows that to achieve a gain of 380V per radian at 10kHz requires RB to be approximately 39kΩ, CAP is zero. A hold capacitor (CH) of non-critical value which might be typically 470pF is connected from CH to V_{SS}. A smaller value is sufficient if the sideband performance required is not high.

The output from the sample/phase detector should be combined with that of the coarse phase/frequency detector and filtered to generate a single control voltage to drive the VCO.

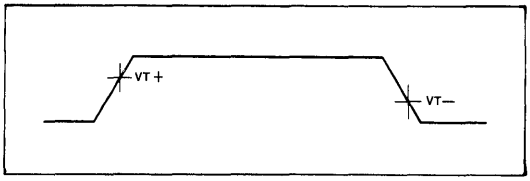


Fig.7 Timing diagram showing voltage thresholds

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.

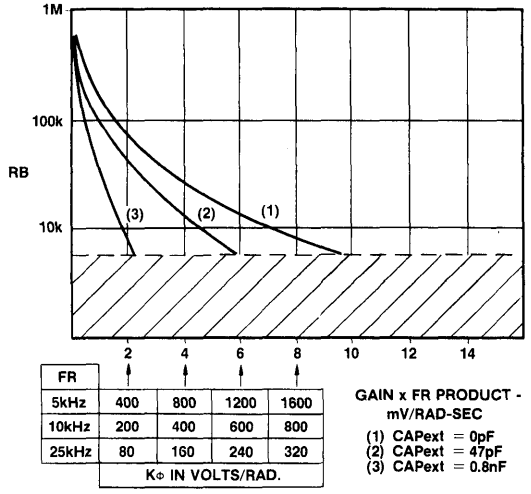


Fig.8 RB v. gain and reference frequency

NJ88C25

FREQUENCY SYNTHESISER (MICROPROCESSOR SERIAL INTERFACE)

The NJ88C25 is a synthesiser circuit fabricated with the 2 micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference counter, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter, latched and buffered BAND 0 and BAND 1 outputs and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented serially under external control from a suitable microprocessr. Although 30 bits of data are initially required to program all counters subsequent updating can be abbreviated to 19 bits when only the 'A', 'M' and 'B' registers require changing.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 or SP8704 series to produce a universal binary coded synthesiser for up to 950MHz operation.

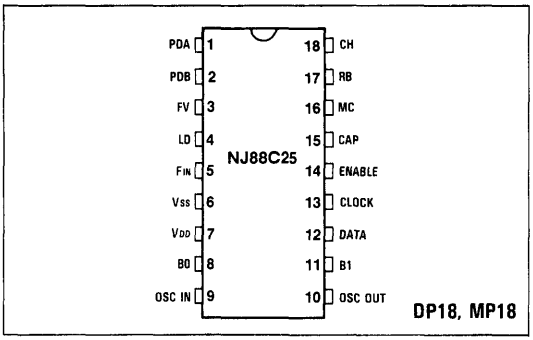


Fig.1 Pin connections - top view

FEATURES

- 3.0V to 5.0V Supply Range
- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Serial Input with Fast Update Feature
- >10MHz Input Frequency

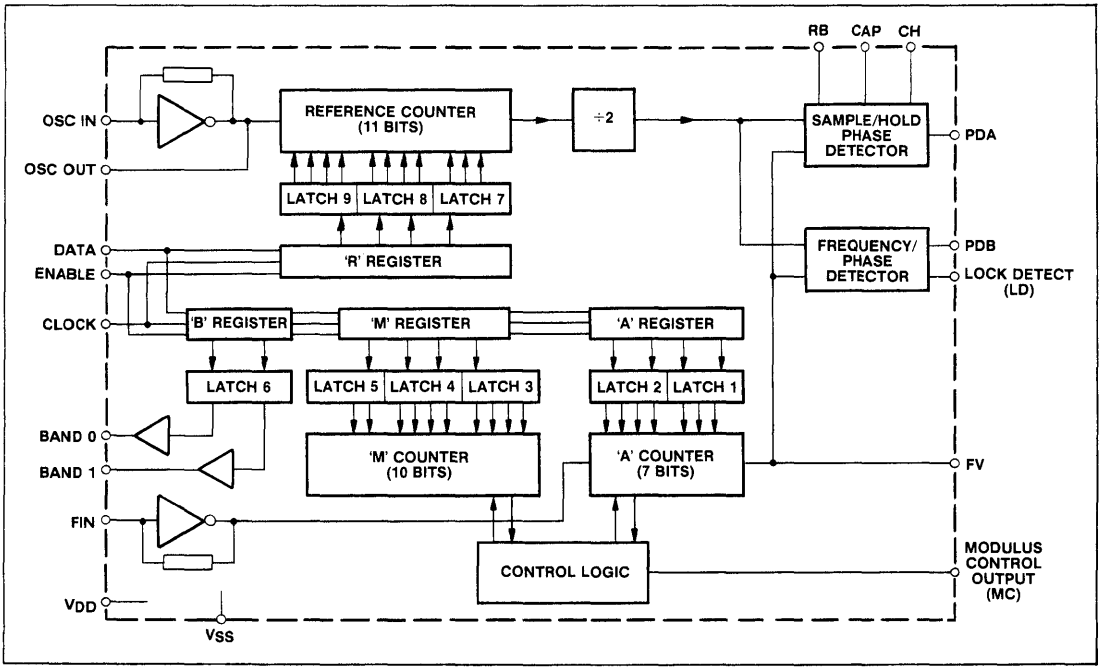


Fig.2 Block diagram

NJ88C30

VHF SYNTHESISER

The NJ88C30 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the Plessey high performance small geometry CMOS. The circuit contains a reference oscillator and divider, a two modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

FEATURES

- Low Power CMOS
- Easy to Use
- Low Cost
- Single Chip Synthesiser to VHF
- Lock Detect Output

APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonobuoys

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3V to +6V
Voltage on any pin	-0.3V to V_{DD} +0.3V
Operating temperature	-30°C to +70°C
Storage temperature	-55°C to +125°C

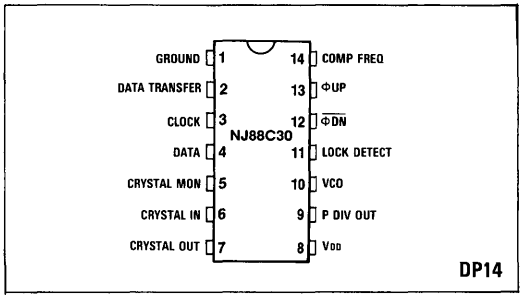


Fig.1 Pin connections (Dual In Line packages) - top view

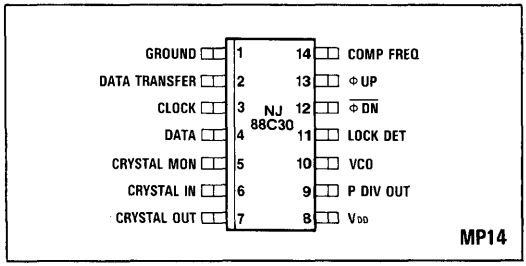


Fig.2 Pin connections (Small Outline Plastic DIL package) - top view

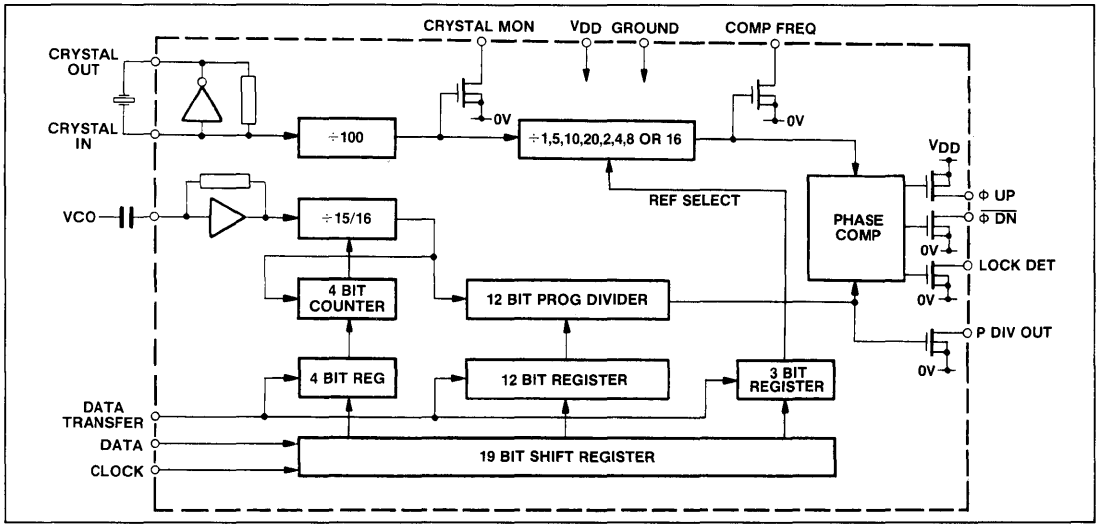
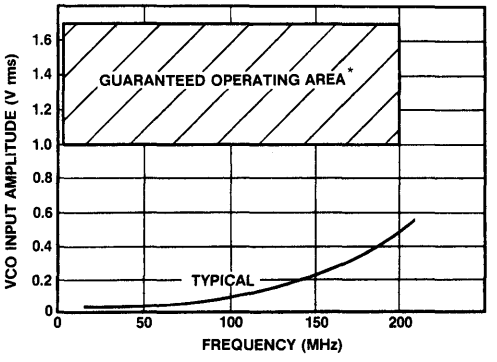


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 5V ± 0.5V

Characteristic	Pin MP14	Pin DG14 DP14	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply							
Supply current	8	4		4	7	mA	1V rms VCO input at 200MHz and f_{XTAL} = 10MHz
Crystal oscillator							
Frequency	6,7	2,3		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	2	1			V rms	AC coupled
High level	6	2	V_{DD}1			V	DC coupled
Low level	6	2			1	V	DC coupled
VCO input							
VCO input sensitivity	10	6	1			V rms	At 200MHz, see Fig.4
Slew rate VCO input	10	6	4			V/μs	
VCO input impedance	10	6		5pF//10kΩ			
DATA, DATA TRANSFER, CLOCK inputs							
High level	2,3,4	12,13,14	V_{DD}1			V	
Low level	2,3,4	12,13,14			1	V	
Rise, fall time	2,3	12,13			200	ns	
Data set up time	3,4	13,14	200			ns	See Fig.5
Clock frequency	3	13			2	MHz	
Transfer pulse width	2	12	500			ns	
Crystal monitor output							
Current sink	5	1	0.8			mA	V_{OUT} = 0.5V
Comp freq, LOCK DET, P DIV							
Current sink	9,11,14	5,7,10	1.6			mA	V_{OUT} = 0.5V
Φ UP/$\overline{\Phi}$ DN							
Current sink	12	8	0.8			mA	V_{OUT} = 0.5V
Current source	13	9	0.8			mA	V_{OUT} = V_{DD} - 0.5V



*Tested as specified in table of Electrical Characteristics

Fig.4 Input sensitivity

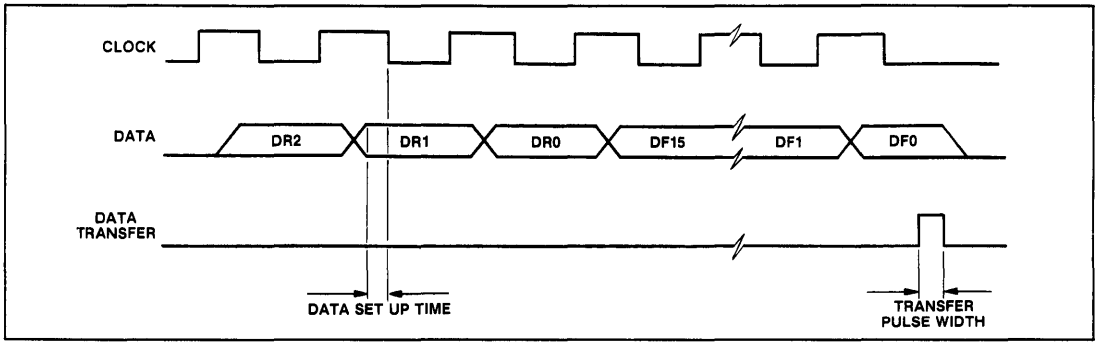


Fig.5 Input data timing diagram

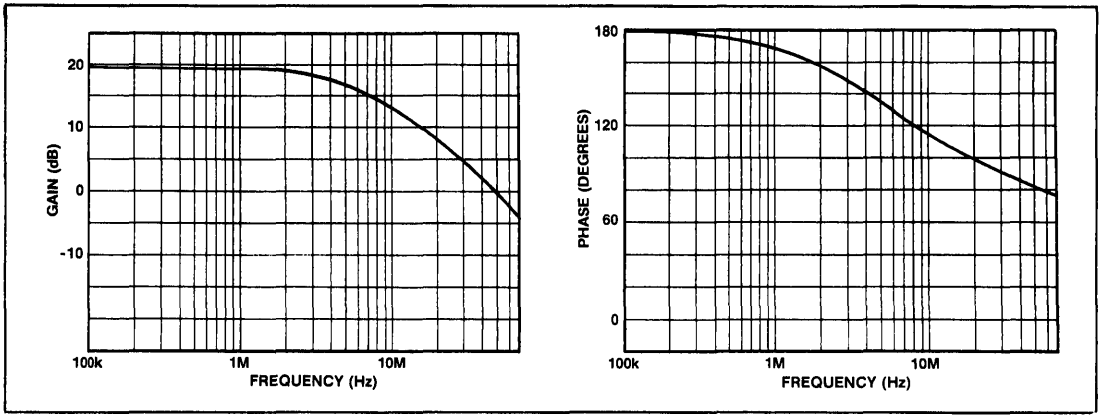


Fig.6 Gain phase characteristics of reference oscillator inverter

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The reference oscillator consists of a Pierce type oscillator intended for use with parallel resonant fundamental crystals. Typical gain and phase characteristics for the oscillator inverter are shown in Fig.6. An external reference oscillator may be used by either capacitively coupling a 1V rms sinewave into the CRYSTAL IN pin or if CMOS logic levels are available by connecting directly to CRYSTAL IN pin.

The reference oscillator drives a divider to produce a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies if a 10MHz crystal is used are shown in Fig.7.

DR2	DR1	DR0	Division Ratio	Comparison Frequency for 10MHz Ref. Osc.
0	0	0	1600	6.25kHz
0	0	1	800	12.5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Fig.7 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 1.

Programmable Divider

The programmable divider consits of a ÷15/16 two modulus prescaler with a 4-bit control register followed by a 12-bit programmable divider. A 1V rms sinewave should be capacitively coupled from the VCO to the divider input VCO pin.

The overall division ratio is selected by a single 16-bit word (DF 15 to 0) loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

Phase Comparator

The phase comparator consists of a digital type phase comparator with open drain Φ UP and $\overline{\Phi}$ DN outputs and an open drain lock detect output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.8. The duty cycle of Φ UP and $\overline{\Phi}$ DN versus phase difference are shown in Fig.9. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π the phase comparator outputs repeat with a 2π period.

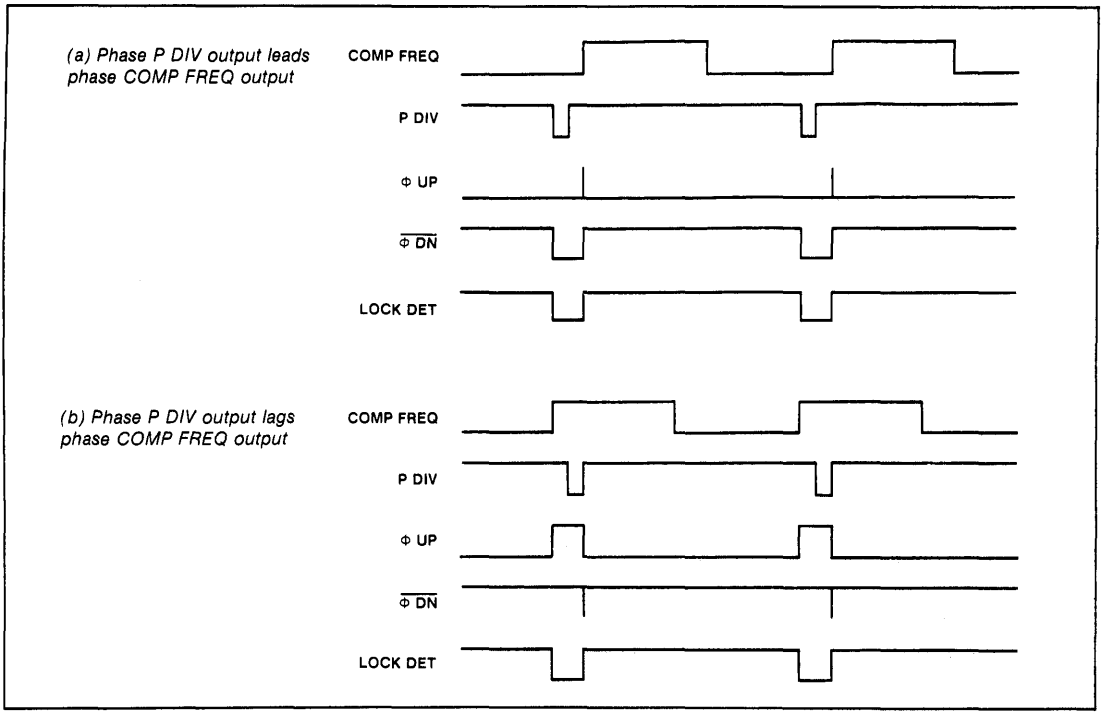


Fig.8 Phase comparator waveforms

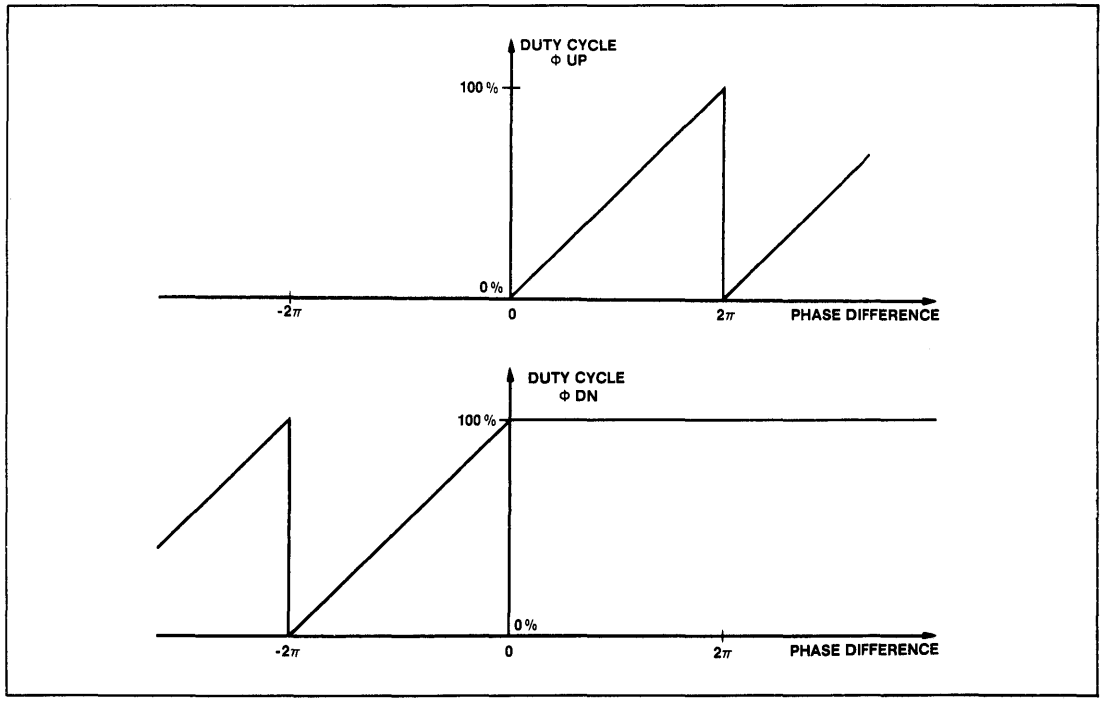


Fig.9 Phase comparator output characteristics

Once the phase difference exceeds 2π the comparator will gain or slip one cycle and then try to lock to the new zero phase difference. Note very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output.

Data Input and Control Register

To control the synthesiser a simple three line serial input is used with Data, Clock and Data Transfer signals. The data consists of 19 bits, the first three DR2, DR1, DR0 control the reference divider, the next sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the Data Transfer pulse it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig.10. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig.10 is required. Pulses from the phase comparator are filtered by R_1, R_2 and C_1. Their values can be determined, given a required natural loop bandwidth ω_n and damping factor δ, by the following equations:

$$R_1C_1 = \frac{K}{\omega_n^2}, \quad R_2C_1 = \frac{2\delta}{\omega_n} \text{ and } K = \frac{K_0 V_{CC}}{4\pi N}$$

where

ω - natural loop bandwidth (rad/s)
δ - damping factor
K_0 - VCO gain factor (rad/Vs)
V_{CC} - charge pump supply voltage (V)
N - division ratio = f_{OUT}/f_{COMP}

The values in Fig. 10 were calculated for:

ω_n = 3000 rad/s
δ = 0.707
K_0 = 18 Mrad/Vs
V_{CC} = 5V
f_{OUT} = 100MHz
f_{COMP} = 50kHz

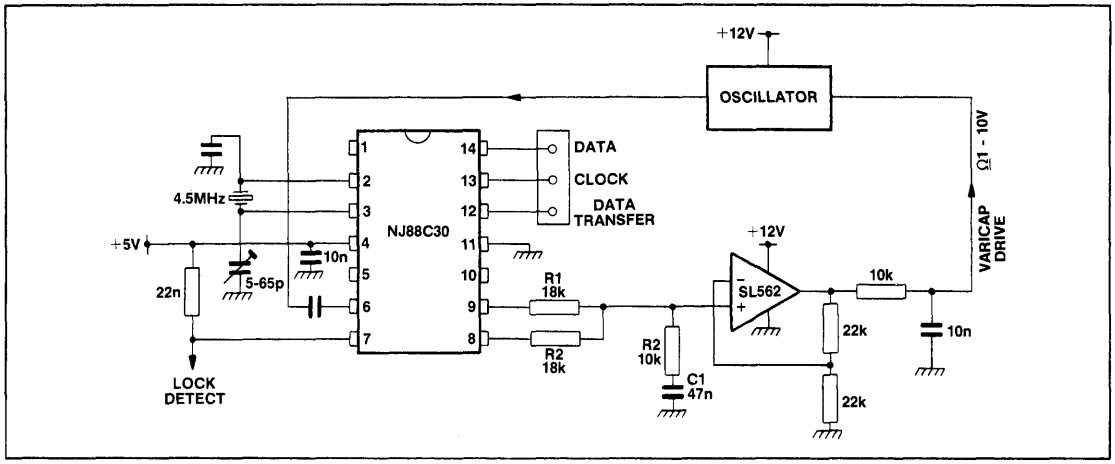


Fig.10 Typical application for DP14 device

Example of Programming

For a channel spacing (comparison frequency) of 5kHz when using a crystal oscillator of 10MHz the reference divider ratio will need to be 2000 (see Fig.7). This is programmed as binary 100 in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200 \times 10^6}{5 \times 10^3} = 40 \times 10^3 \text{ which is 9C40 Hex.}$$

The complete program word would then be:

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
Hex	4			9				C				4				0			

Using the same crystal and 5kHz channel spacing the minimum VCO frequency programmable would be 1.2MHz with the division ratio of 240 (= F0 Hex). The program word would then be:

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Hex	4			0				0				F				0			

NJ88C31

MF/VHF SYNTHESISER

The NJ88C31 contains all the logic needed for an MF/VHF PLL synthesiser and is fabricated on Plessey high performance small geometry CMOS. The circuit contains a reference oscillator and divider, a two modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic, and a 4.5MHz μP clock drive output.

FEATURES

- Low Power CMOS
- Easy To Use
- Low Cost
- Single Chip Synthesiser
- Lock Detect Output
- 4.5MHzμP Clock Output
- MF Band Prescaler Bypass Function
- Front End Disable for Very Low Power Standby
- Band Output to Switch Radio Between MF and VHF

APPLICATIONS

- AM/FM Radios
- Car Radios

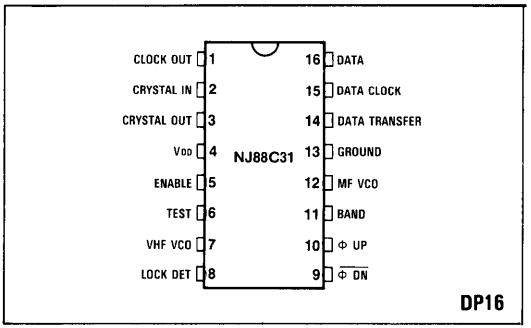


Fig.1 Pin connections (plastic DIL - top view)

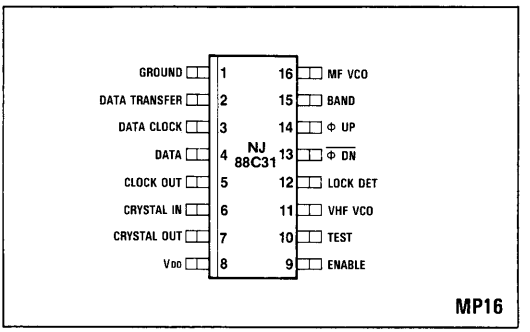


Fig.2 Pin connections (plastic Small Outline DIL - top view)

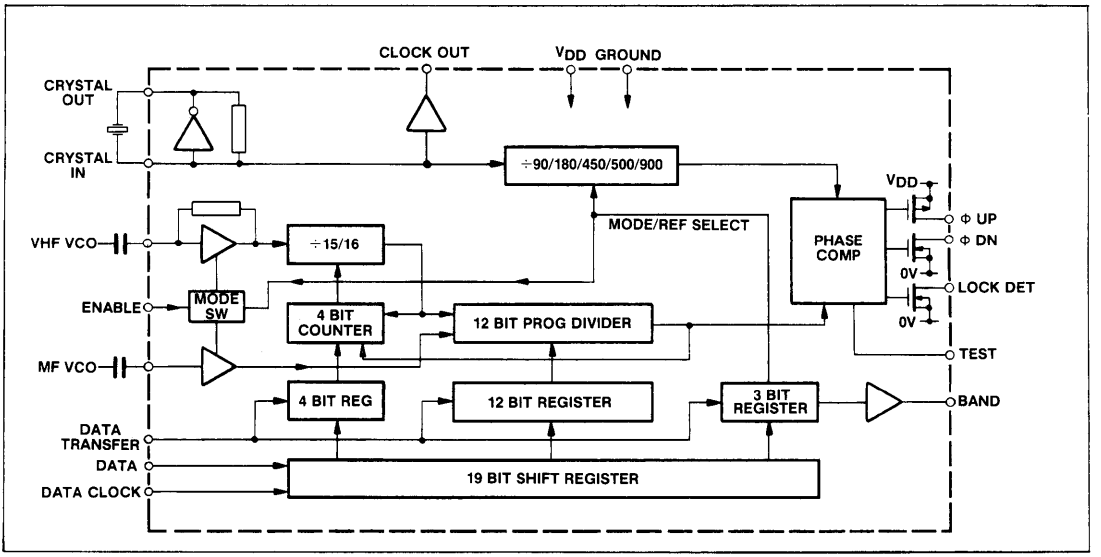


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -40 to +85°C, V_{DD} = 5V ± 0.5V

ABSOLUTE MAXIMUM RATINGS

V_{DD}	-0.3V to +6V
Voltage on any pin	-0.3V to V_{DD} +0.3V
Operating temperature	-40°C to +85°C
Storage temperature	-55°C to +125°C

Characteristic	Pin MP16	Pin DP16	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply							
Supply current	8	4		4	7	mA	1V rms VHF VCO input at 120MHz and f_{XTAL} = 4.5MHz
Supply current (Standby mode)					2	mA	f_{XTAL} = 4.5MHz, Enable low
Crystal oscillator							
Frequency	6,7	2,3		4.5	15	MHz	Parallel resonant, fundamental crystal
External input level	6	2	1			V rms	AC coupled
High level	6	2	V_{DD}-1			V	DC coupled
Low level	6	2			1	V	DC coupled
VCO inputs							
VHF VCO input sensitivity	13	7	0.3			V rms	At 50 to 125MHz, see Fig.4
MF VCO input sensitivity	16	12	0.3			V rms	At 0.1 to 2.5MHz
VCO input impedance	13,16	7,12		5pF/10kΩ			
DATA, DATA TRANSFER, DATA CLOCK, TEST and ENABLE inputs							
High level	2,3,4 9,10	5,6, 14,15,16	V_{DD}-1			V	
Low level	2,3,4, 9,10	5,6, 14,15,16			1	V	
Rise, fall time	2,3	14,15			200	ns	
Data set up time	3,4	15,16	200			ns	See Fig.5
Clock frequency	3	15			2	MHz	
Transfer pulse width	2	14	500			ns	
CLOCK OUT, BAND							
Current sink	5,15	1,11	0.8			mA	V_{OUT} = 0.5V
Current source	5,15	1,11	0.8			mA	V_{OUT} = V_{DD} -0.5V
LOCK DET							
Current sink	12	8	1.6			mA	V_{OUT} = 0.5V
Φ UP/$\overline{\Phi}$ DN, BAND							
Current sink	13	9	0.8			mA	V_{OUT} = 0.5V
Current source	14	10	0.8			mA	V_{OUT} = V_{DD} -0.5V

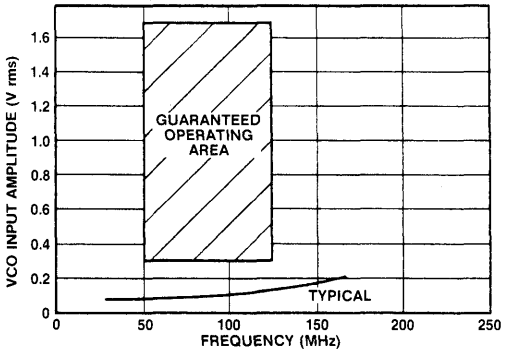


Fig.4 Input sensitivity of VHF VCO

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The reference oscillator consists of a Pierce type oscillator intended for use with parallel resonant fundamental crystals. Typical gain and phase characteristics for the oscillator inverter are shown in Fig.6. An external reference oscillator may be used by either capacitively coupling a 1V rms sinewave into the CRYSTAL IN pin or if CMOS logic levels are available by connecting directly to the CRYSTAL IN pin.

The reference oscillator drives a divider to produce a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies if a 4.5MHz crystal is used are shown in Fig.7.

There is a 4.5MHz μP clock drive output available on the CRYSTAL OUT pin.

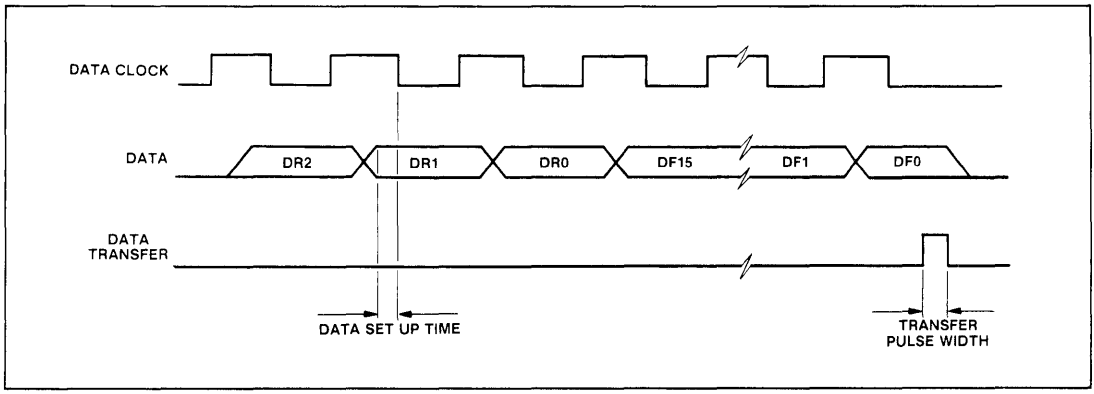


Fig.5 Input data timing diagram

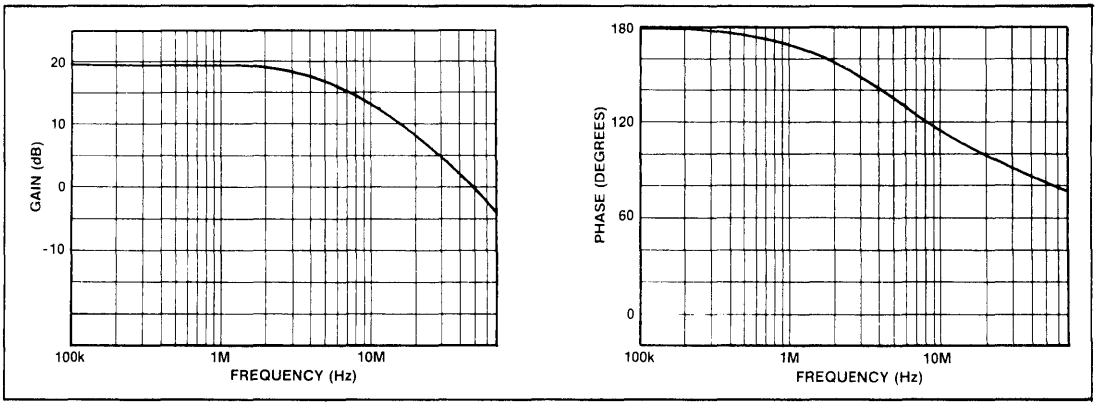


Fig.6 Gain phase characteristics of reference oscillator inverter

BAND Output

The programming bit DR2 is brought out as a BAND output, '1' for MF band and '0' for VHF.

DR2	DR1	DR0	Division Ratio	Comparison Frequency 4.5MHz XTAL	BAND
0	0	0	90	50kHz	VHF
0	0	1	180	25kHz	
0	1	0	450	10kHz	
1	0	0	450	10kHz	MF
1	0	1	500	9kHz	
1	1	0	900	5kHz	

Fig.7 Reference divider division ratios

Programmable Divider

The programmable divider consists of a 12-bit divider preceded on FM by a divide by 15/16 two modulus divider. The F/M input is fed through an amplifier to provide adequate sensitivity.

TEST Input

When the TEST pin is taken to a logic 1, the Φ UP pin is connected to the output of the reference chain divider (COMP FREQ) and the $\overline{\Phi \text{ DN}}$ pin is connected to the output of the 12-bit programmable signal chain divider (PROG DIV); this mode is normally only used in factory testing.

Phase Comparator

The digital phase comparator has three open drain outputs; Φ UP and $\overline{\Phi \text{ DN}}$ drive the charge pump and LOCK DETECT may be integrated to generate a MUTE signal. Waveforms for all these outputs are shown in Fig.8. The duty cycle of Φ UP and $\overline{\Phi \text{ DN}}$ versus phase difference are shown in Fig.9. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π the phase comparator outputs repeat with a 2π period. Once the phase difference exceeds 2π the comparator will gain or slip one cycle and then try to lock to the new zero phase difference. Note very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output.

ENABLE Input

When ENABLE is taken to logic '0' both VCO input buffers and the prescaler are switched off to save power. The crystal oscillator, CLOCK OUT and control registers continue working normally, such that when ENABLE is taken to a '1' the device will retune the last programmed frequency.

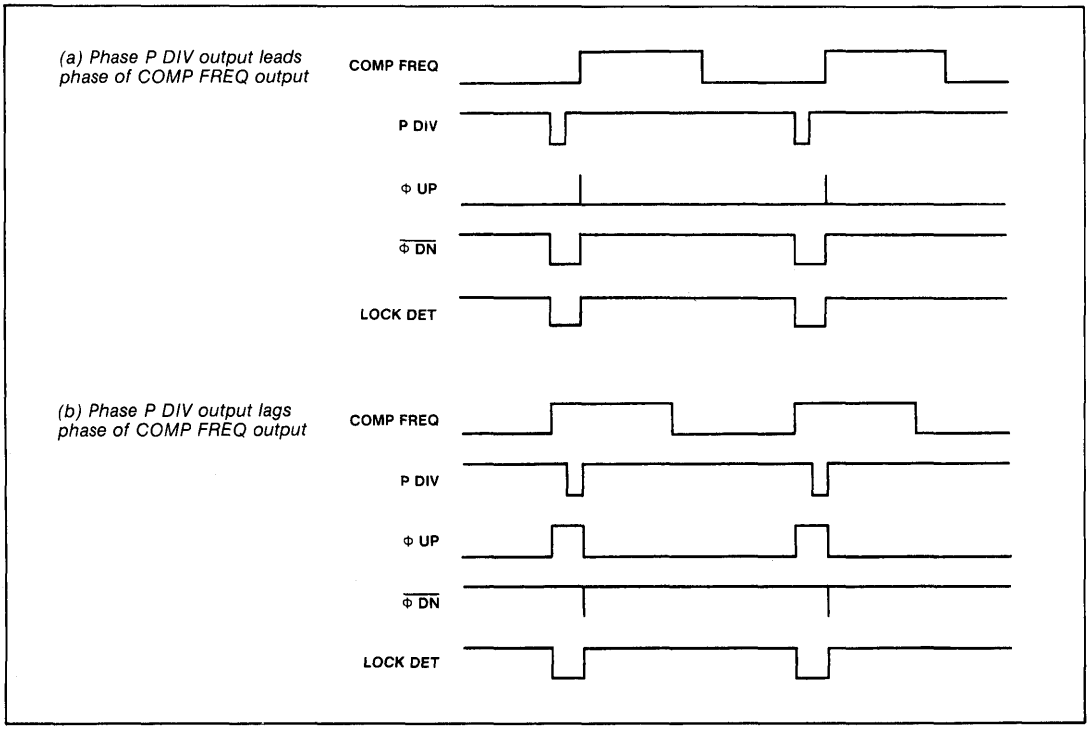


Fig.8 Phase comparator waveforms

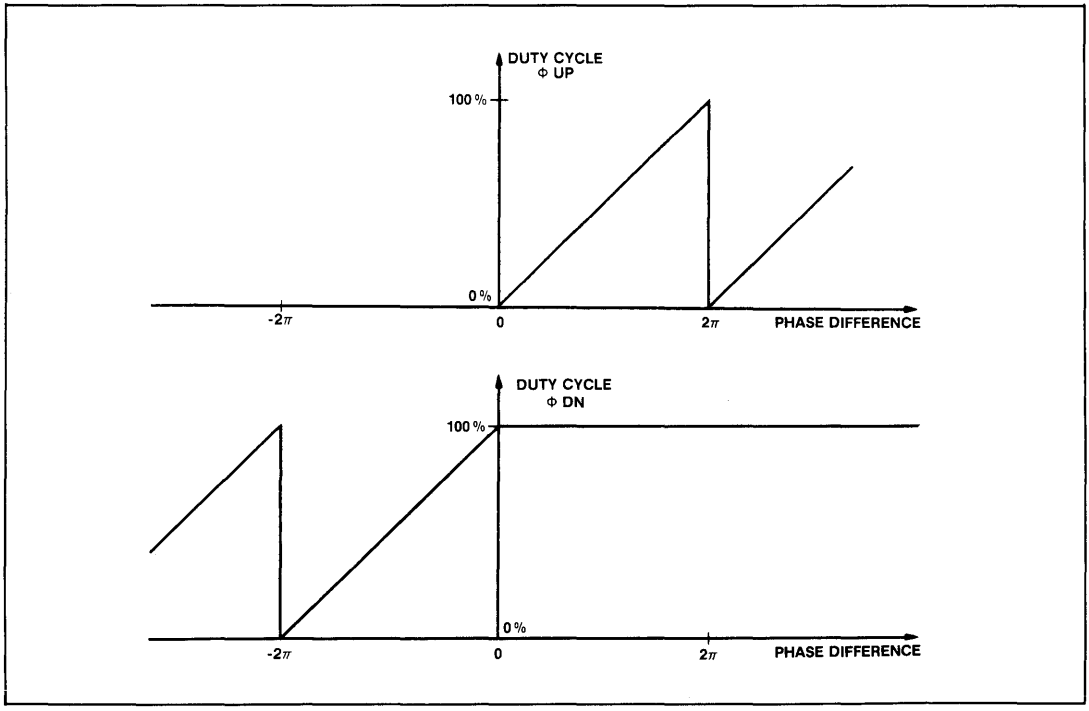


Fig.9 Phase comparator output characteristics

Data Input and Control Register

To control the synthesiser a simple three line serial input is used with Data, Clock and Data Transfer signals. The data consists of 19 bits, the first three DR2, DR1, DR0 control the reference divider, the next sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the Data Transfer pulse it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data. See Fig.5.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig.10. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig.10 is required.Pulses from the phase comparator are filtered by R_1, R_2, and C_1. Their values can be determined, given a required natural loop bandwidth ω_n and damping factor δ, by the following equations:

$$R_1C_1 = \frac{K}{\omega_n^2}, R_2C_1 = \frac{2\delta}{\omega_n} \text{ and } K = \frac{K_0 \times V_{CC} \times G}{4\pi N}$$

where

ω - natural loop bandwidth (rad/s)
δ - damping factor
K_0 - VCO gain factor (rad/Vs)
V_{CC} - charge pump supply voltage (V)
N - division ratio = f_{OUT}/f_{COMP}
G - Gain of amplifier

The values in Fig.10 were calculated for:

ω = 3000 rad/s
δ = 0.707
K_0 = 18 Mrad/Vs
V_{CC} = 5V
f_{OUT} = 100MHz
f_{COMP} = 25kHz
G = 2

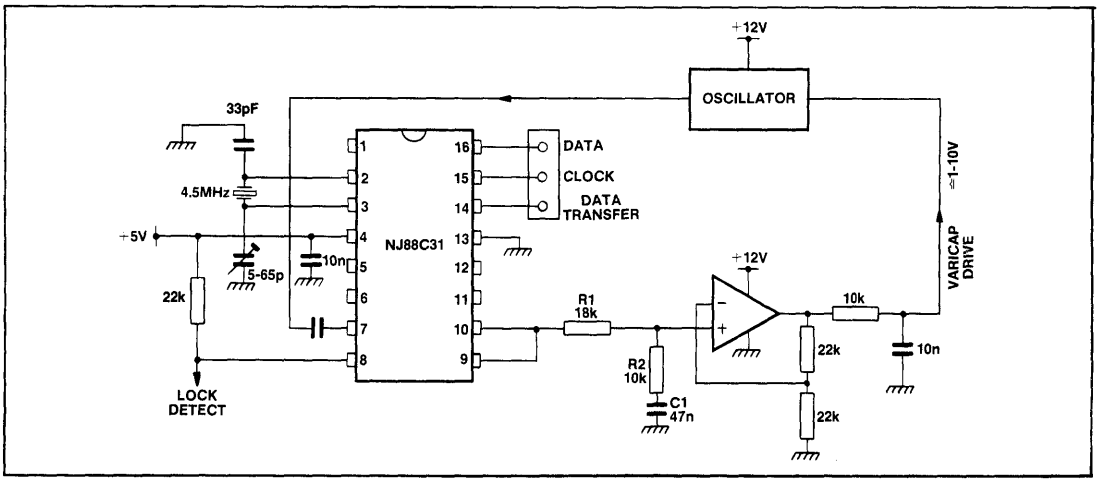


Fig.10 Typical application for DP16 device

Example of Programming

VHF section

For a channel spacing (comparison frequency) of 10kHz when using a crystal oscillator of 4.5MHz, the reference divider ratio will need to be 450 (see Fig.7). This is programmed as binary 010 in the most significant three bits of the 19 bit data word (MSB programmed first).

To obtain a VCO frequency of 125MHz the programmable divider ratio would be:

$$\frac{125 \times 10^6}{10 \times 10^3} = 12500 = 30D4 \text{ Hex.}$$

The programming word would be:

	DR			DF															
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	0	1	0	0	0	1	1	0	0	0	0	1	1	0	1	0	1	0	0
Hex	2			3				0				D				4			

MF section

The four least significant bits of DF are not used in programming the programmable divider ratio, but nevertheless a total of 19 bits must be supplied.

For a channel spacing of 5kHz when using a crystal oscillator of 4.5MHz, the reference divider ratio will be 900 (see Fig.7). This is programmed as 110 in the most significant bits of the 19 bit word (MSB is programmed first).

To obtain a frequency of 2.5MHz the programmable divider ratio would need to be 500. The value programmed into the DP register must be the desired ratio minus one, i.e. in this case 499 which is 1F3 Hex.

The programming word would be:

	DR			DF															
Bit No.	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	1	0	0	0	0	1	1	1	1	1	0	0	1	1	X	X	X	X
Hex	6			1				F				3				DON'T CARE			

Application Notes

SL2365 Applications

The SL2365 is an array of transistors configured to form a dual long-tailed pair with tail transistors which are current mirrored to similar transistors whose bases and collectors are connected internally.

The ICs are manufactured on a very high speed bipolar process which has a typical f_T of 5GHz. The device is available in a surface mounted DIL package (MP14), the pin connections of which are shown below.

Various applications are described including a 900MHz amplifier, a frequency doubler, a frequency tripler and a single balanced mixer.

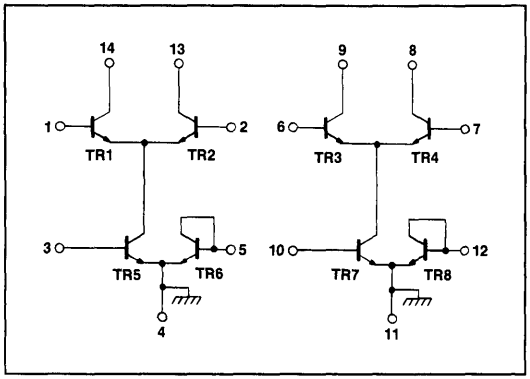


Fig.1 SL2365 schematic diagram

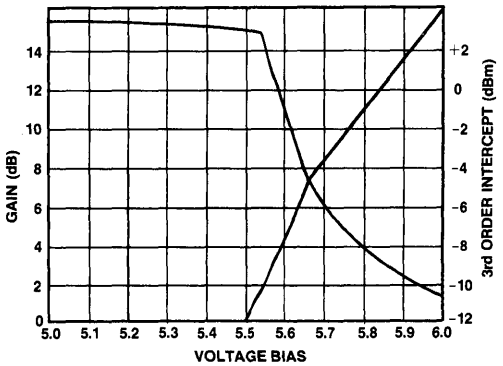


Fig.3 3rd order intercept at gain of 12.5dB (using current mirror at 4mA) = -7dBm

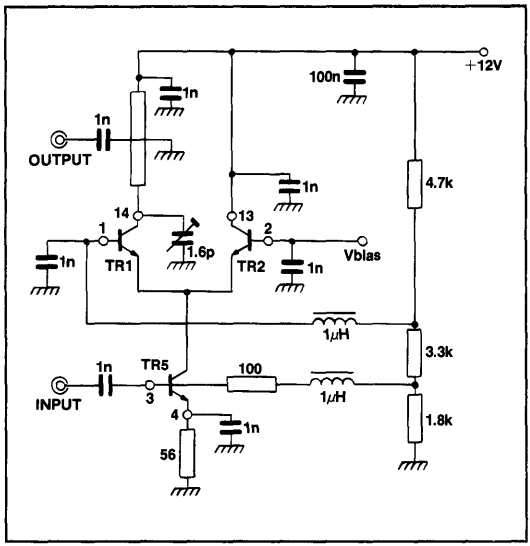


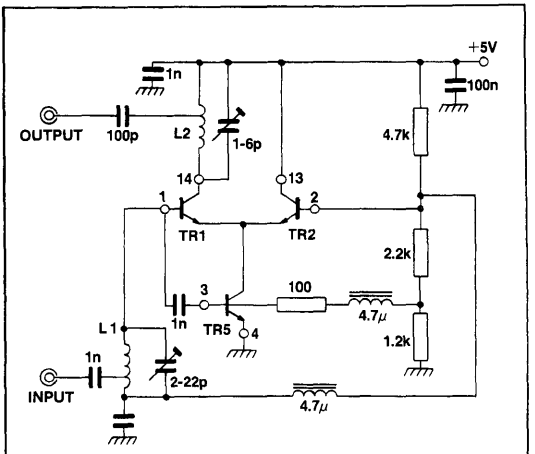
Fig.2

A 900MHz GAIN CONTROLLED AMPLIFIER

In Fig.2, the collector load of TR1 is a transformer composed of a 14mm length of 75Ω stripline resonated with a 1-6pF variable capacitor. The secondary of the transformer is a small loop of stiff wire grounded at one end and located a few mm above the stripline. The gain and 3rd order intercept versus V bias is shown in Fig.3. The noise figure at full gain is 9dB.

A 150-300MHz FREQUENCY DOUBLER

The frequency doubler, Fig.4, has a gain of +1dB for a -20dB input and input frequency rejection of 18dB.

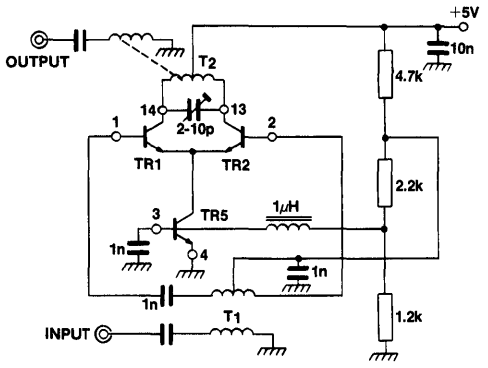


NOTES
L_1 = 4 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from ground end
L_2 = 3 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from 5V rail end

Fig.4

A 100-300MHz FREQUENCY TRIPLER

Fig.5 shows a 100-300MHz frequency tripler with a gain of -40dB, input frequency rejection of 30dB and second harmonic rejection of 28dB.

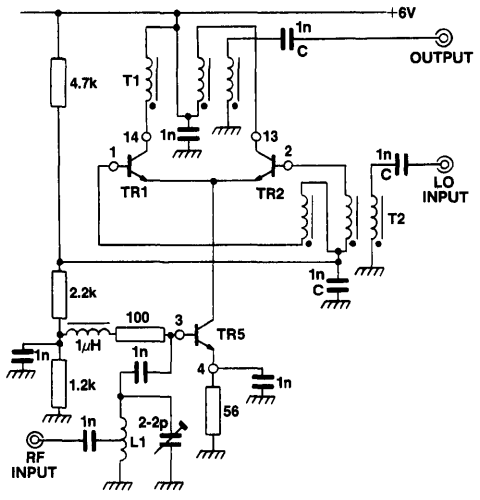


NOTES
T_1 Primary = 4 turns 36 swg enamelled wire wound on ferrite core
T_1 Secondary = 4 turns 36 swg enamelled wire wound on LF ferrite core (twisted pair)
T_2 Primary = 2 turns 20 swg tinned wire 5mm diameter
T_2 Secondary = 4 turns 20 swg tinned wire 5mm diameter, positioned axially relative to T_2 Primary

Fig.5

A SINGLE BALANCED MIXER

The mixer of Fig.6 has a gain of 13dB, 3rd order intercept = -13dBm, -10dBm (using 2mA in current mirror) and noise figure = 10dB.



NOTES
L_1 = 4 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from ground end
T_1 and T_2 = 4 turns of trifilar wound 36 swg enamelled wire wound on LF ferrite core

Fig.6

Radio Synthesiser Circuits
Loop Filter Design

LOOP BANDWIDTH

An important choice in the design of the Phase Locked Loop is the Loop Bandwidth. This determines parameters such as lock up time, noise and modulation capability, and generally is made as wide as possible in single loop synthesisers. There are conflicting requirements however, and single loop synthesisers are not always practicable - Refs. 1, 2.

The NJ8820 series use two phase detectors, a digital 'steering' detector and an analog high gain linear detector. This latter detector is a sample-and-hold type in which an internal 50pF capacitor is discharged at a constant current. This current is set by the gain programming resistor *RB*, and the voltage on the capacitor is sampled at the reference frequency. Thus the gain of the detector is fixed by the time available for the capacitor to be discharged. If the discharge current was constant, the phase detector would have a gain directly proportional to frequency and current, but the departure from constant current gives a correcting factor, and the gain is thus:

$$K\Phi = 10\,\frac{[V_{SUPPLY} - 0.7 - 89\,(RB)^{-\frac{1}{2}}]}{[2\pi \times (50 \times 10^{12} + CAP) \times RB \times FR]} \quad ...(1)$$

where *RB* is the gain programming resistor and *FR* is the phase comparison frequency. The value of *CAP* is 0 for the NJ8820/1 and is fixed externally in the NJ8822.

The analog phase comparator has a very high gain and so can only operate over a narrow phase range. This phase window is given by:

$$\Delta\Phi = 4.5/K\Phi \text{ radian}$$

where $K\Phi$ is the phase detector constant (volts/radian).

When the analog phase detector is outside this range, the digital detector operates to provide steering. Inside the analog detector phase range, the digital output is in its 'Tri-State' high impedance condition.

When the loop filter consists of an integrator of the form of Fig.1 the digital output produces a voltage ramp given by:

$$-2.5\,\frac{R_3}{R_1} - \frac{2.5}{R1C} \text{ volts/sec} \quad ...(2)$$

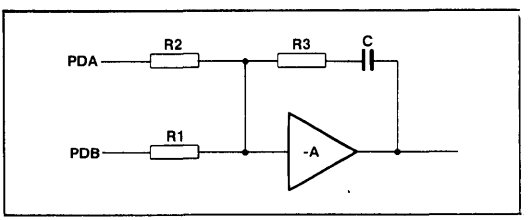


Fig.1 Augmenting integrator for loop filter

The figure of 2.5 is derived as follows:

A 2nd order loop has infinite DC gain and thus the analog phase detector output sits at a potential very close to the half supply voltage point. It is thus at 2.5V, and the maximum change in Vin is therefore 2.5V, and this input will appear whenever the digital phase detector operates.

This ramp results in a frequency sweep of approximately

$$2.5K_V \left(\frac{R_3}{R_1} + \frac{1}{R_1C_1}\right) \text{rads/sec}^2 \quad ...(3)$$

Thus for a frequency step of $\Delta\omega$, the loop will slew to the new frequency in

$$\frac{\Delta\omega}{\frac{2.5K_V}{R_1}\left(R_3 + \frac{1}{C}\right)} \quad ...(4)$$

where K_V is the VCO constant in rads/volts-sec.

Although the loop will lock eventually without the digital steering, the time taken is much longer. The time to attain frequency lock is given approximately by:

$$\frac{\Delta\omega R_2}{2.5K_V\left(R_3 + \frac{1}{C_1}\right)} \quad ...(5)$$

This is derived from the slew rate at the output of the integration without the digital loop connected. Independent control of lock up time and loop bandwidth is therefore available by correct choice of R_1.

The 2nd order analog loop has a bandwidth and damping factor given by:

$$\omega_n = \sqrt{\frac{K\Phi K_V}{NR_2C}} \quad ...(6)$$

$$D = \frac{R_3C}{2} \cdot \omega_n \quad ...(7)$$

If the loop is slewed at too high a rate by the digital output, then a longer lock up time may result because of overshoot; in extreme cases, the loop will become unstable, because the VCO frequency will sweep too quickly.

$$CR_2 = \frac{2\pi\, K\Phi K_V}{\omega_n^2 N} \quad ...(8)$$

$$\frac{R_2}{R_3} = \frac{\pi\, K\Phi K_V}{DN\omega_n} \quad ...(9)$$

$$R_1 \geqslant 5R_2\,\frac{2D}{\omega_n} + 1 \quad ...(10)$$

where ω_n = loop bandwidth in rads/sec
$K\Phi$ = analog phase detector gain in volts/rad
K_V = VCO sensitivity in Hz/volt
D = loop damping factor
N = divide ratio

The minimum value of R_1 can be determined as follows. The noise bandwidth, B_n, of a second order loop is:

$$B_n = \frac{K\Phi K_V\left(\frac{R_3}{R_2} + \frac{1}{R_3C}\right)}{4} \text{ Hz} \quad ...(11)$$

and the maximum sweep rate is

$$\frac{d\Delta\omega}{dt} = \frac{1}{2R_3C}\left(4B_n - \frac{1}{R_3C}\right) (B_n \text{ in radians}) \quad ...(12)$$

Thus the maximum voltage sweep is

$$\frac{dV}{dt} = \frac{1}{2K_V R_3C}\left(4B_n - \frac{1}{R_3C}\right) \quad ...(13)$$

which simplifies to

$$\frac{dV}{dt} = \frac{K\Phi}{2R_2C} \quad ...(14)$$

The integrator gives an output (assuming $R_2 >> R_1$)

$$V = 2.5\left(\frac{R_3}{R_1} + \frac{1}{R_1C}\right) \text{ volts/sec} \quad ...(15)$$

$$\text{therefore } 2.5\left(\frac{R3}{R1} + \frac{1}{R1C}\right) \leqslant \frac{K\Phi}{2R2C} \quad ...(16)$$

$$R3 = \frac{2D}{\omega_n D} \quad \text{and by substitution,}$$

$$R1 \geqslant \frac{5R2}{K\Phi}\left(\frac{2D}{\omega_n} + 1\right) \quad ...(17)$$

For $D > 0.5 < 1.0$
and $\omega_n > 10$ rads/sec
Then the approximation

$$R1 \geqslant \frac{5R2}{K\Phi} \quad ...(18)$$

is correct.

It is advisable to use a larger value than this: it is suggested that

$$R1 \text{ min} = \frac{6R2}{K\Phi} \quad ...(19)$$

The minimum usable values of $K\Phi$ occur at higher reference frequencies, where a wider loop bandwidth can be used. Wide loop bandwidths are good for reduction of VCO noise and freedom from microphony, while narrow loops minimise the effects of reference frequency noise.

The NJ8820 analog phase detector has an internal noise level of about 1 microvolt/$\sqrt{}$Hz at a frequency of 100Hz. This falls within increasing frequency, and decreasing phase detector gain.

VCO Noise

Phase noise of the VCO inside the loop bandwidth will be reduced by the loop, while outside the loop bandwidth it will be unaltered. The phase noise of the reference oscillator will add to the VCO noise at frequencies inside the loop bandwidth and this effect also influences the choice of loop bandwidth. For example, a loop with a 5kHz loop bandwidth operating at 900MHz with a reasonable 5MHz crystal oscillator noise floor (-125dBc/Hz at 1kHz oscillator) would have a noise power of some -80dBc/Hz at 1kHz offset at final frequency. For a further discussion of phase noise and other compromises see Ref. 2.

Where a high phase detector gain is used with a noisy oscillator, or with a high value of K_V, it may well happen that the analog phase detector is driven outside the phase window. This will lead to the digital output becoming active, and instability is likely to result.

Modulation Techniques

Modulation of the PLL may take place inside or outside the loops bandwidth. Modulation outside the loop bandwidth requires the loop bandwidth to be less than the lowest modulating frequency, and the amount of modulation will vary over the frequency range as K_V, the VCO constant varies.

Various techniques may be used to minimise the variation in modulation sensitivity, and probably the easiest in the use of a separate modulation diode. The variation in capacitance is very small for normal NBFM variations and thus the deviation may well remain sensibly constant over a wide range, e.g. +0.75kHz for 5kHz nominal deviation over an 18MHz range at VHF.

Modulation outside the loop bandwidth leads to a signal appearing at the phase detector output corresponding to the phase error between reference frequency and the divided VCO. Should this phase error be such as to lead to the phase detector being driven outside its phase window, then problems may occur, with reference frequency sidebands appearing and possibly even unlocking of the loop.

Avoidance of this condition may be achieved by limiting the phase deviation at the detector such that detector is operating within its linear range. For devices with programmable phase detector gain, such as NJ8820 series, this may be achieved by using a low gain and high deviation ratio.

Modulation index, m, is given by:

$$m = \frac{\text{frequency deviation}}{\text{modulating frequency}} \quad ...(20)$$

For a modulation index of 1 at the VCO, the phase variation is 1 radian. Thus an NBFM transmitter with a deviation of 2.5kHz and modulation frequency of 500Hz has a phase deviation of 5 radians.

In a 25kHz channelled system at 30MHz, the deviation at the detector would be 5/1200 rads or 0.24 degrees. Attempting to operate the NJ8820 at 800 volts/rad would give problems because of limiting in the analog phase detector.

Modulation inside the loop bandwidth avoids this problem, but care must be taken to ensure that the reference frequency sidebands do not become appreciable. In addition, the wideband noise of the phase detector and loop filter can cause problems when K_V, the oscillator constant in MHz/volt, is high.

Modulation of the reference oscillator is another possible technique of modulating inside the loop bandwidth. However, all modulation inside the loop bandwidth produces phase rather than frequency modulation and there are, in addition, limits on the frequency deviation and modulation frequency that can be accepted without the loop becoming unlocked. Generally, the modulation frequency must be much less than the loop bandwidth. Gardner (Ref.4) has derived the equation:

$$\Delta\omega = \frac{\omega_n^2}{\omega_m} \quad ...(21)$$

where $\Delta\omega$ = frequency deviation
ω_n = loop natural frequency (bandwidth)
ω_m = modulating frequency

This equation is only valid for $\omega_m << \omega_n$

In general, modulation outside the loop bandwidth is used, because the required bandwidth is greater than the reference frequency. The loop bandwidth is usually 1/5 and 1/10 of the lower modulating frequency.

Note that modulation applied such that

$$\frac{\Delta\omega}{dt} \geqslant \frac{K\Phi K_V}{R2C} \quad ...(22)$$

will cause the loop to unlock.

In addition, modulation such that the analog phase detector limits is not advisable. This will occur when

$$\Delta\Phi \geqslant 4.5N/K\Phi \text{ rads} \quad ...(23)$$

$\Delta\Phi$ is equivalent to m, the modulation index: when $m = 1$, $\Delta\Phi = 1$ radian.

Thus, a synthesiser operating at 145MHz with a 25kHz comparison frequency and a modulation index of 30 for the lowest modulating frequencies would need $K\Phi$ to be less than 870 volts/rad. Operation at lower frequencies are used. However, large amounts of LF phase noise can have appreciable phase deviations and thus low noise oscillators should be used.

Noise from the amplifier used in the loop filter should be minimised: the use of a low noise amplifier such as a Plessey SL562 is suggested. Filtering after the amplifier, such as in Fig.2, is advisable to minimise the noise modulation of the VCO, but care should be taken to ensure that the added phase shift does not cause the loop to become unstable.

Loop Stability

Calculation of loop stability may be carried out in a number of ways. It has been claimed (Ref.4) that a true 2nd order PLL does not exist because of strays. In addition, an extra section (at least) of RC filtering is generally required to minimise the effects of noise in the operational amplifier. Various computer programs exist in which such analysis can be undertaken, but it is possible to evaluate loop stability in a relatively easy manner using a programmable calculator.

For a 2nd order loop such as Fig.2, it may be shown that the transfer function is

$$\frac{AoK\Phi Kv}{N\omega} \cdot \frac{j\,\omega T2 + 1}{j\,(1-\omega^2 E) - \omega\,(F - \omega^2 D)} \qquad ...(24)$$

where $D = T3To\,(T1 + T2)$

$E = T3\,(Ao\,T1 + To + T1 + T2) + To\,(T1 + T2)$

$F = Ao\,T1 + To + T1 + T2 + T3$

and Ao, $K\Phi$, Kv, N, ω, have the previously assigned definitions.

Ao = open loop amplifier gain
To = $1/fo$, amplifier open loop 3dB bandwidth
$T1$ = $R2C1$
$T2$ = $R3C1$
$T3$ = $R4C2$

The finite modulation bandwidth of the VCO is ignored in this analysis.

Evaluating the equation (24) in terms of gain and angle ($rL\theta$) at various frequencies allows the stability to be evaluated. An example of a frequency synthesiser design is given in the following section, where Table 1 lists a suitable program for Hewlett Packard Calculators using Reverse Polish Notation.

Frequency Synthesiser Design

A frequency synthesiser is required for a transmitter covering 144-148MHz. the supply voltage for the synthesiser is 10 volts, pre-emphasised frequency modulation is required with an upper limit of 3kHz, adjacent channel noise is required to be -70dB at 12.5kHz channel spacing and a 'lock-up' time of 25ms is required.

12.5kHz channel spacing systems use an IF bandwidth of 7.5kHz, which gives approximately 39dB more noise than a 1Hz bandwidth. Thus the VCO for this synthesiser must have a phase noise characteristic of -109dBc/Hz at 12.5kHz (see Ref.1) and from Refs. 2 and 3 this may be shown to be practical with a single loop synthesiser using a narrow bandwidth.

The choice of prescaler should be made from a consideration of programming - see the relevant data sheet.

The lowest modulation frequency is 300Hz and the transmitter will attenuate components below this frequency at 12dB/octave or more. Standard pre-emphasis rises at 6dB/octave from 300Hz to 2700Hz: thus the deviation at 300Hz is approximately 18dB down on that at 2.7kHz and at 50Hz will be about -45dB. With a deviation at 2.7kHz of 2.5kHz, the deviation at 50Hz will be about 15Hz.

At 144MHz, the divide ratio is 145000/12.5 = 11600. Thus the 15Hz deviation it caused by the 50Hz modulation becomes

$$15/50 \times 1/11600$$

radians at the phase detector, which is negligible. Thus the analog phase detetor will operate inside its window at low frequencies. Even at 300Hz where the modulation index is 8.33, the phase deviation at the phase detector is only 0.041 degrees.

Since a 10V supply is available, a VCO control line swing of 8 volts may be assumed. Allowing overlap, the VCO will cover 143-149MHz, giving Kv (the VCO constant) as 0.75MHz/volt. This gives a residual deviation caused by the phase detector noise of about 0.75Hz.

A loop bandwidth of 50Hz is well below the lowest modulating frequency and values may be readily calculated. $K\Phi$, the phase detector gain, is an independent variable; a reasonable mid-range value of 320 volts/rad gives a phase window of 0.89 degrees.

From these constants, values of $R1$, $R2$, $R3$ and C in Fig.1 may be calculated.

$$CR2 = \frac{2\pi\,K\Phi Kv}{\omega_n{}^2 N} \qquad ...(25)$$

$$\frac{R2}{R3} = \frac{\pi K\Phi Kv}{DN\,\omega_n} \qquad ...(26)$$

$$R1\ \text{min} = \frac{6R2}{K\Phi} \qquad ...(27)$$

Thus, at the mid-band frequency of 146MHz, where N = 11680:

$$CR2 = \frac{2\pi \times 320 \times 0.75 \times 10^6}{(2\pi \times 50)^2 \times 11680} = 1.3 \qquad ...(28)$$

$$\frac{R2}{R3} = \frac{\pi \times 320 \times 0.75 \times 10^6}{0.7 \times 11680 \times 2\pi \times 50} = 293 \qquad ...(29)$$

$$R1 \geqslant \frac{5R2}{K\Phi}\left(\frac{2D}{\omega_n}\right) + 1 \qquad ...(30)$$

The use of high values of resistance leads to greater noise generation in the loop filter because of KTB noise, while low values lead to larger current swings, which can give slew rate limiting in the op-amp. If $R3$ is set to 2200Ω, thus preventing slew rate limiting,

$R2 = 664k\Omega$ (use $680k\Omega$)
$C1 = 1.9\mu F$ (use $2.2\mu F$)

From these standard values

$$\omega_n = \sqrt{\frac{K\Phi Kv}{NCR2}} = 46.7Hz \qquad ...(31)$$

$$\text{and } D = \frac{R3C}{2} \cdot \omega_n = 0.71$$

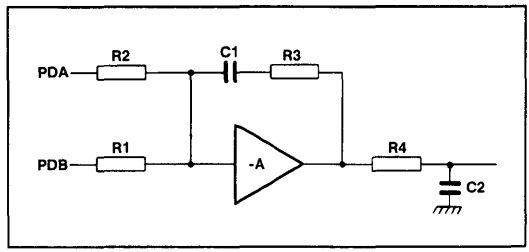


Fig.2 Augmenting integrator amplifier with filtering

$$R1 \text{ min} = \left(\frac{5 \times 680k\Omega}{320}\right)\left(\frac{2 \times 0.71}{2\pi \times 46.7} + 1\right) = 10.7k\Omega \quad ...(32)$$

(use 12kΩ or 15kΩ).

A further section of filtering may be added as in Fig.2, and the cut-off frequency may be arbitrarily set at 500Hz. Again, a reasonable compromise is required on *CR* values for the same reasons. The added filter section reduces noise from the op-amp and resistors, and so is a useful addition.

Let $R = 10k\Omega$ and $C = 0.33\mu F$

Using the program in Table 1, the stability may be calculated. (Assume a Plessey SL562 op-amp, where *fo*, the open loop 3dB frequency is 250Hz and *Ao*, the open loop gain = 30000).

$T0 = 1/fo = 4 \times 10^{-3}$
$T1 = R2C1 = 1.496$
$T2 = R3C1 = 4.84 \times 10^{-3}$
$T3 = R4C2 = 330 \times 10^{-6}$
$N = 11680$
$K\Phi = 320$
$Kv = 0.75$MHz/volt (4.7×10^6 rads/volt)

The results of the program are:

Frequency (Hz)	Loop Gain	Phase Margin (Degrees)
1	2200	-178
10	23	-164
50	1.59	-119
100	0.69	-128

From this analysis, it may be seen that the loop is stable. Increasing the time constant of *T3* is thus practicable from a loop stability point of view.

The lock up time *t* may be calculated from

$$\frac{\Delta\omega}{2.5Kv}\left(\frac{1}{R1R3} + CR1\right) \quad ...(33)$$

so for a 600kHz change,
$t = 8.5$ms to achieve frequency lock.
as opposed to 476ms without the digital steering (see equation (5)).

Note that these lock up times assume that the major factors affecting loop bandwidth are the values of the time constant *R2C*. In practice, this simplification is not completely justified, and, for example, increasing the value of *C2R4* to give *T3* = 5ms would increase lock up time while having little effect on loop stability.

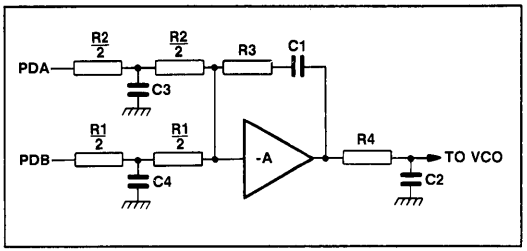


Fig.3 Loop filter with input sections

In cases where the operational amplifier 'locks up' because of overdrive, the circuit of Fig.3 may be used, often with success. The time constants *C3R2/2* should be about *10/fn* where *fn* is the loop bandwidth. It should be noted that the capacitor *C1 must* be of the non-polarised variety, as the voltage across it can reverse. Similarly, the external capacitor provided in the phase detector of the NJ8820 should be a low leakage type, such as polystyrene: ceramic capacitors are not generally good enough.

Bypassing the gain setting resistor of the NJ8820 series with a large capacitor may reduce noise derived from this resistor.

Loop Stability Program for HP Calculators

Enter

STO0	T0
STO1	T1
STO2	T2
STO3	T3
STO4	Ao
STO5	KΦ
STO6	Kv
STO7	N

(*T0* = 1/*fo*, the 3dB point of the op amp 'open loop' bandwidth, *T1* = *R2C1*, *T2* = *R3C*, *T3* = *R4C2*, *Ao* = open loop gain, *KΦ* = phase detector gain in volts/rad for the analog phase detector, *Kv* = VCO constant in rads/volt-sec, *N* = divide ratio).

Line	Function	Line	Function	Line	Function
001	hLBLA		+		RCL0
	Enter		RCL0		(g)x²
	2		x	075	+
	x	040	STO0		(h)1/x
005	(h)π		RCL4		RCL1
	x		RCL1		x
	STO8		x		STO1
	RCL1		RCL0	080	RCL8
	RCL2		+	081	RCL2
010	+	046	RCL1		x
	RCL0		+		RCL0
	x		RCL2		x
	RCL3		+	085	RCL9
	x	050	RCL3		-
015	RCL8		x		RCL1
	(g)x²		RCL0		x
	x		+		STO2
	STO9		RCL8	090	RCL8
	RCL4	055	(g)x²		RCL2
020	RCL1		x		x
	x		CHS		RCL9
	RCL0		1		x
	+		+	095	RCL0
	RCL1	060	STO0		+
025	+		RCL4		CHS
	RCL2		RCL5		RCL1
	+		x		x
	RCL3		RCL6	100	STO3
	+	065	x		Enter
030	RCL9		RCL7		RCL2
	-		"		(g)P
	RCL8		RCL8		(h)PSE
	x		"	105	(h)PSE
	STO9	070	STO1		(g)R
035	RCL1		RCL9		(h)RTN
	RCL2		(g)x²		

Table 1 Loop stability program

To use, enter the frequency in Hz, and press R/S. The display will show the loop gain, flash twice and display the phase margin in degrees.

Note that HP calculators provide angular information up to ±180 degrees only. Thus a change from -179 degrees to -181 degrees would show as -179 to +179 degrees.

Multimodulus Division

Phase Locked Loop Frequency Synthesisers of the form shown in Fig.4 suffer from the problems inherent in producing fully programmable dividers required to operate at appreciable frequencies while not consuming excessive power. Although advances in small geometry integrated circuit technology make any figures obsolete, guaranteed operation above about 50MHz requires relatively high power.

The use of fixed prescaling, as in Fig.5, is widely used, but for a division ratio of N in the prescaler and a channel spacing of f kHz, the phase comparison frequency of Fig.4 has been reduced by the factor f/N. This lower frequency necessitates a lower bandwidth in the phase locked loop, and thus a greater susceptibility to microphonics etc., and, generally speaking, a longer lock up time.

The alternatives to fixed division are mixing, as in Fig.6 or 'multimodulus division' ('pulse swallowing') as in Fig.7. The use of mixers requires great care in the choice of frequencies if spurious products are not to be a problem and although widely used, is certainly more complicated than multimodulus division in terms of its physical realisation, requirements for 'adjust-on-test' parts, and its susceptibility to layout problems.

The multimodulus divider system is shown in Fig.7. It is built up from a number of blocks:

1. A two-modulus divider which will divide by one of two numbers N or $N + 1$ (e.g., 10/11, 64/65 etc.).

2. An A counter which is programmable and the output of which controls the modulus of the divider.

3. An M counter which is programmable, is clocked in parallel with the A counter, and the output of which resets both itself and the A counter.

The counters may count 'down' to zero from the programmed input, or count 'up' from zero.

The principle of operation is as follows:

The A counter is programmed to a smaller number than the M counter and assuming the counters to be empty, the system starts with the divider $(N/N + 1)$ dividing by $N + 1$. This continues until the A counter reaches its programmed value, whereupon the divider divides by N until the M counter is full. As the M counter has received A pulses, this counter overflows after (M - A) pulses, corresponding to $N(M - A)$ input pulses to the divider. Thus the total division ratio P is given by:

$$P = (N + 1)A + N(M - A)$$
$$= NM + A$$

Obviously, A must be equal to or less than M for the system to work, while for every possible channel to be available, the minimum total divide ratio is $N(N - 1)$ while the maximum total divide ratio is $M(N + 1)$. A_{max} should be equal to or greater than N.

Although deceptively simple in theory, there are a few points which require consideration in the design of such a divider system. Of these probably the most important is Loop Delay.

Consider the counter chain at the instant that the $(N + 1)$th pulse appears at the two modulus divider input. After some time $tp1$ the output produces a pulse, which clocks the A and M counters. Assume that the A counter is filled by the pulse, and so after a time $tp2$ (determined by the propagation delay of the A counter) an output is produced to set the dual modulus divider ratio to N. After a set-up time ts, the dual modulus divider will divide by N. But if $tp1 + tp2 + ts$ is greater than N cycles of input frequency, the divider will not be set to divide by N until after N pulses have appeared, and the system will fail. Thus

$$\frac{N}{fin} > \text{total loop delay}$$

Design in this region is critical: worst case tolerances *MUST* be used if the reproducibility and reliability of the design under temperature and voltage extremes is not to be compromised.

The value of N must also be large enough that the output frequency from the divider does not exceed the maximum input frequency of the following circuitry. In single chip MOS controllers, this may well be as high as 50MHz under some conditions, but under others, such as high temperature and low voltage, much lower. Generally, however, the limitation on such circuits is the loop delay rather than input frequency.

The loop delay is affected by the edge of the waveform on which the divider and the A and M counters trigger. If the edges are opposite then the loop delay may be increased by large amount, and if in these circumstances, the use of an inverter at the output of the divider is justified.

The minimum value of N is therefore settled by these constraints, but the actual choice of N may be determined by the ease of programming. This may be seen by considering a synthesiser with a 25kHz phase comparison frequency and 25kHz channelling, using a 40/41 divider.

At 156MHz:

$$P = \frac{156}{0.025} = 6240$$

therefore $NM + A = 6240$
therefore $40M + 0 = 6240$ ($A = 0$ for the lowest channel)
therefore $M = 156$

In general, where

$$fN = 1 \text{ or } 10 \text{ or } 100$$

$$M = f, \frac{f}{10}, \frac{f}{100} \text{ etc.}$$

and similarly for binary divide ratios.

The choice of prescaler is therefore fixed by

1. Total allowable loop delay.

$$\frac{N}{fin} > \text{controller delays}$$

2. Output frequency within the controller input frequency band.

3. Programming ease.

REFERENCE FREQUENCY DIVISION RATIO (R)

The value of R is set by the input frequency and the phase comparison frequency. Higher input frequencies require greater power and offer lower stability, while lower frequencies (below 4MHz) generally require larger physical crystal case sizes. Normally, a frequency between 4 and 10.7MHz is used, especially as in double conversion equipments commonality of oscillators may be possible.
e.g. for a 2.5kHz comparison frequency and 10.245MHz 2nd local oscillator frequency,

$$R = \frac{10.245 \times 10^6}{2.5 \times 10^3} = 4098$$

Note that R is *always* an even number.

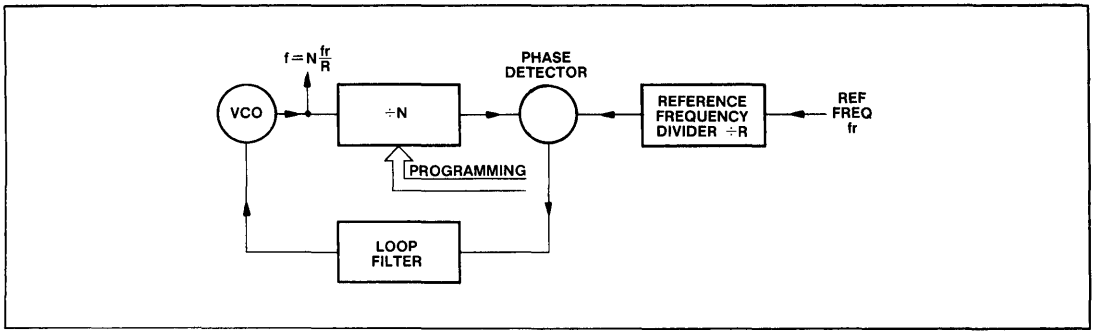


Fig.4 Direct division

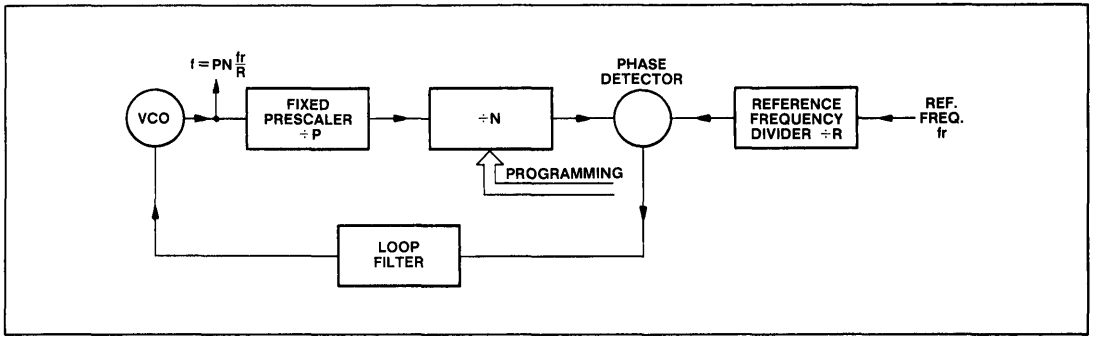


Fig.5 Fixed prescaling

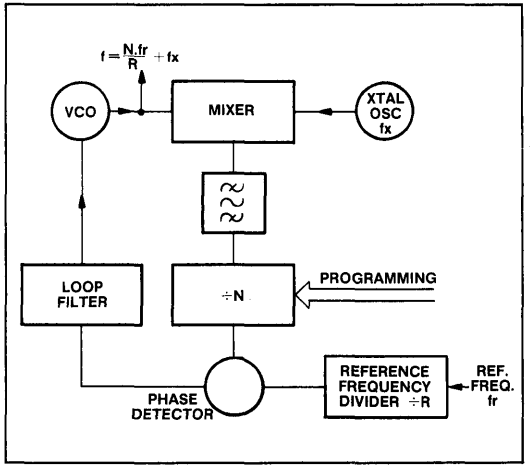


Fig.6 Mixing in the loop

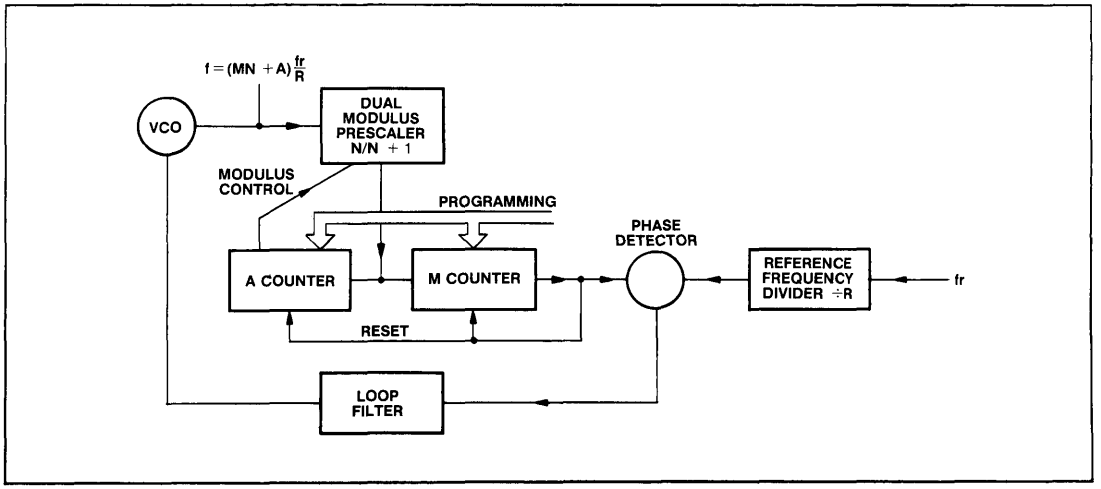


Fig.7 Dual modulus prescaling

Programming the NJ8820 and NJ8821

The NJ8820, NJ8820HG and NJ8821 are versatile high performance CMOS frequency synthesiser controllers. The differences between devices lies in hardware programming methods.

The basic system of a single loop frequency synthesiser is shown in Fig.8, where a 2-modulus prescaler is used to divide the VCO frequency down to a suitable range for use in the CMOS device. The NJ8820/1 is programmed by 8 of 4 bit words on the data inputs: the addresses for these words may be obtained internally or externally and appear on the Data Select inputs/outputs. To program any frequency, it is necessary to program the *A* counter, the *M* counter and the reference or *R* counter: these counters are respectively, 7, 10, and 11 bits long.

ADDRESSING

Addressing is by one of three modes: These are:

A. Self Programming Internal Mode

Here the reference oscillator (either an internal crystal oscillator or from an external source) signal is divided in the reference counter by 64 and a DATA READ cycle commences every 1024/fosc seconds.

In this DATA READ cycle, the MEMORY ENABLE pin is pulled low, and the DATA SELECT outputs DS0, 1 and 2 count in binary from 0 to 7. This provides addresses for the DATA on D0, 1, 2 and 3, the data being transferred to internal latches on the trailing edge of the DATA SELECT pulses -see Fig.9. Note that the Program Clock is internally derived and is at a frequency of fosc/64. The PE (Program enable) pin is grounded, and the cycle continuously repeats. This mode is not recommended, as noise may be picked up by the phase locked loop.

B. Single Shot Internal Mode

In this mode, the PE pin is provided with a pulse input. This pulse initiates a data read cycle as outlined above, and at the end of the cycle, the ME (Memory Enable - NJ8820 and NJ8820HG only) pin goes high and thus system power consumption is minimised. 'Power-on' initiation is used, in which the application of power to the device is sensed and a programming cycle initiated. In order to avoid corruption of the data, a delay of 53248 cycles of reference oscillator frequency is provided before the programming cycle occurs. This delay is approximately 5ms for a 10MHz reference frequency.

C. External Mode

The address is presented to DS0, 1 and 2, and a pulse is applied to the PE pin to transfer data to the internal latches. The data is transferred from the latches to the counters simultaneously with the transfer of data into Latch 1: thus this word should be the last one entered.

WORD VALUES

For any particular set of conditions, viz operating frequency, prescaler ratio, comparison frequency and input frequency from the reference oscillator, a unique set of programming words exist.

Reference Divider

This divider produces the comparison frequency required by the synthesiser. It is programmable from 6 to 4094 in steps of 2. The division ratio is twice the programmed number. Therefore, if for example a 10MHz crystal is used, and a 12.5kHz reference required, this counter would be programmed to give a ratio of 100000/12.5 = 800. The actual programming would then be 400, which would be entered in binary according to the data map, Table 3.

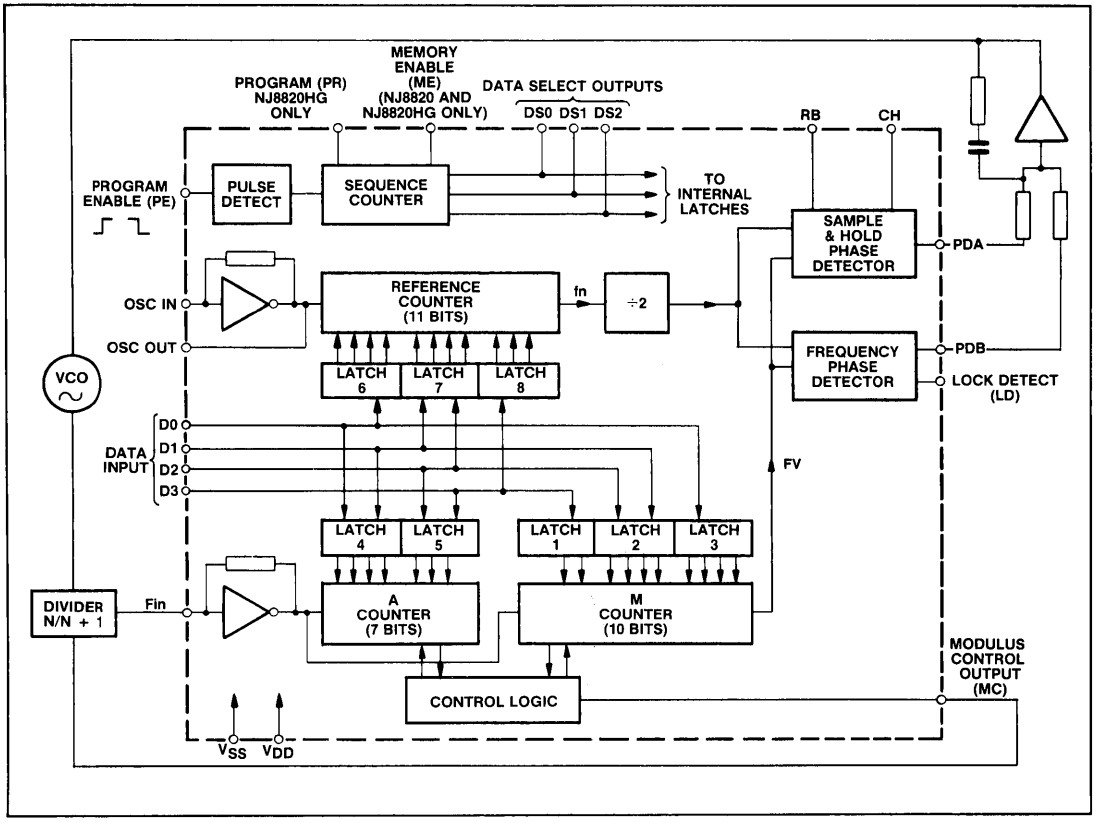


Fig.8 The phase lock loop

A and N Dividers

The *A* counter is a 7-bit counter and the *M* counter is a 10-bit counter. The programming calculations are as follows:

1. The *A* counter should contain *x* bits such that $2^x = M$.

2. If more bits are included in the *A* counter, these should be programmed to zero.

e.g. $M = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The *M* and *A* counters are treated as being combined so that the MSB of the *M* counter is the MSB of the total and LSB of the *A* counter is the LSB of the total.

e.g. A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
P = f/fref and fref = channel spacing = 25kHz
$Pmin = 430/0.025 = 17200$
$Pmax = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

$$\text{maximum allowable loop delay} = \frac{64}{440 \times 106} = 145\text{ns}$$

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
$Pmin$ from above is 17200

Therefore $17200 = 64M + A$
And $M \geqslant A$
Let $A = 0$ Then $Mmin = \frac{17200}{64} = 268.75$

$= 268$
and $Mmax = \frac{17600}{64} = 275.0$

Thus the *M* counter must be programmable from 268 to 275 as required: the *M* counter must have at least 9 bits.
For a frequency of 433.975MHz

$P = 433.97/0.025 = 17359$

$$\text{therefore} \quad M = \frac{17359}{64} = 271.2343$$

The *A* counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the *A* counter is programmed to 15 and the *M* counter to 271. The output frequency can bow be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

Repeated calculations for memory programming may be easily evaluated using a programmable calculator. The program listed in Table 2 is suitable for most Hewlett Packard calculators.

Line	Function	Display
001	hLBLA	25 13 11
002	ENTER	31
003	RCL0	24 0
004	-	71
005	STO2	23 2
006	RCL1	24 1
007	-	71
008	STO3	23 3
009	hFRAC	25 33
010	ENTER	31
011	RCL1	24 1
012	X	61
013	STO4	23 4
014	RCL3	24 3
015	ENTER	31
016	RCL3	24 3
017	hFRAC	25 33
018	-	41
019	STO3	23 3
020	hPSE	25 74
021	hPSE	25 74
022	RCL4	25 4
023	hRTN	25 12

Table 2 Calculator program for values of M and A

To use the program, enter the comparison frequency in STO0, and the dual-modulus prescaler ratio in STO1 (this is the value of N in an $N/N + 1$ divider).

Enter the frequency to be synthesised in Hz and press the R/S button. The calculator will flash twice and display the decimal value of M: pressing R/S again will display the value for the A counter. The M counter value is in STO3: the A counter value is in STO4.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Table 3 Data map

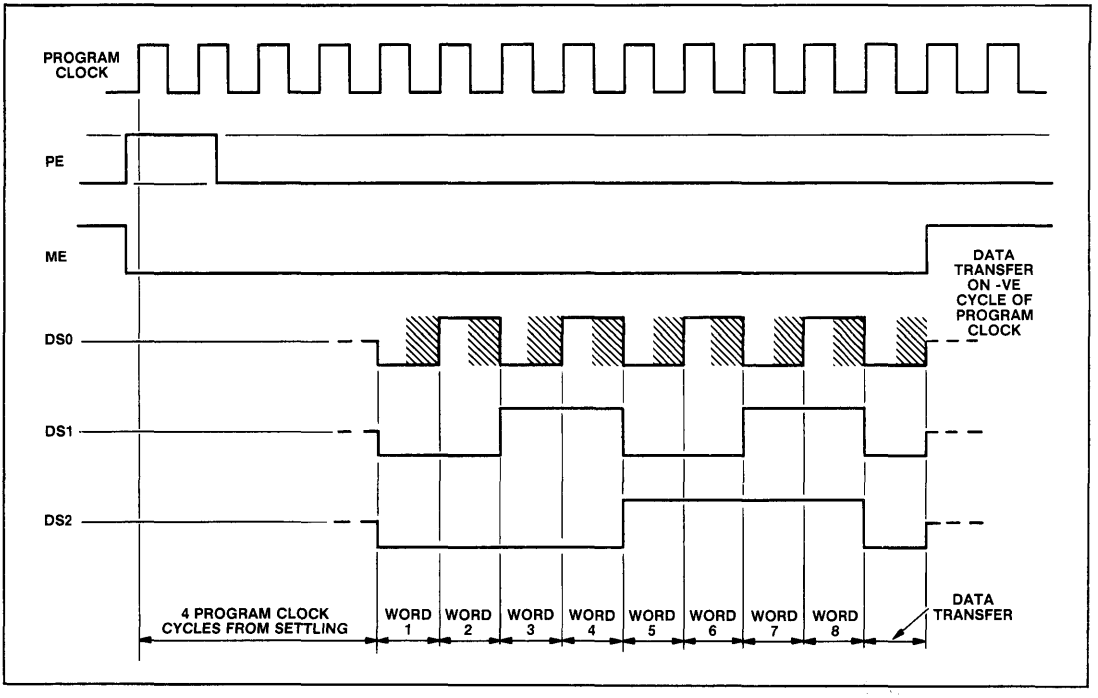


Fig.9 Data selection

NJ8820/1 SYNTHESISER DESIGN SUMMARY

1. Choose a suitable prescaler

- Check that input frequency range is suitable.
- $\frac{fin}{N} < 10.7\text{MHz}$
- $\frac{N}{fin} > 50\text{ns} + tr + tp$

  (tr is 'set-up' or 'release' time - whichever is longer; tp is propagation delay).
- Minimum division ratio is $N^2 - N$.

2. Choose the crystal frequency and value of R

- The phase comparison frequency should be as high as possible - usually the channel spacing.
- Higher crystal frequencies use more current and are less stable, but frequencies below 4MHz need larger case styles.
- R *must* be an even number.

3. Set values for A and M

- A is between 0 and 127.
- A is always equal to or less than M.
- Total division ratio is $NM + A$.
- M is between 3 and 1023.

4. Set loop values

- Choose the loop bandwidth ω_n rads/sec - normally less than $\frac{fx \,.\, 2\pi}{10R}$ (fx = crystal frequency)
- Choose the Damping Factor D - normally 0.7.
- Choose phase comparator gain such that at the lowest modulation frequency the phase deviation

$$\frac{\text{Modulation index}}{(MN + A)} < \frac{4.5}{K\Phi}\text{ rads}$$

5. Calculate the values:

- $CR2 = \frac{2\pi K\Phi K_V}{\omega_n^2 \,.\, (NM + A)}$

  ($K\Phi$ in volts/rad)
  (K_V in rads/volt-sec)
  (ω_n in rads/sec)
- $\frac{R2}{R3} = \frac{\pi K\Phi K_V}{D(NM + A)\ \omega_n}$
- $R1 > \frac{6R2}{K\Phi}$
- $\frac{1}{R4C2} \geqslant \frac{10\ \omega_n}{2\pi}$

6. Check the time to reach a new frequency

- $t = \frac{\Delta\omega}{2.5K_V}\left(\frac{1}{R1R3} + CR1\right)$

  ($\Delta\omega$ is the frequency step in rads/sec).

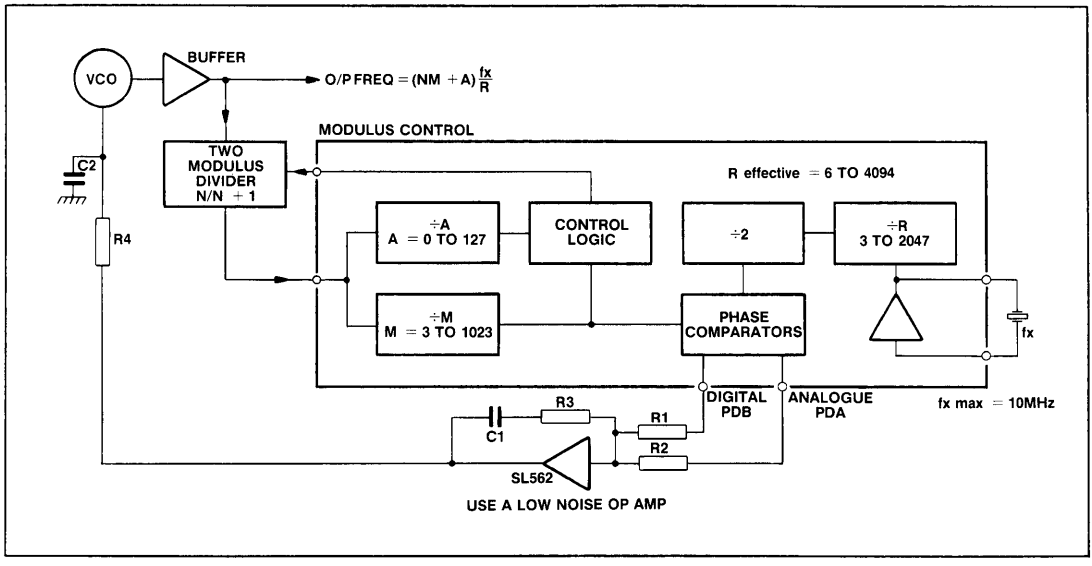


Fig.10 PLL using NJ8820/1

7. Check the loop stability using Bode or Nyquist plots - or use the calculator program listed in Table 1. (Page 4).

8. Derive the program numbers for the *A* and *M* counters - or use the calculator program listed in Table 2. (Page 9).

9. An example

A synthesiser is to operate from 430 to 440MHz in 25kHz steps (the channel spacing is 25kHz):

- **Choose the divider** The SP8718 is one choice. Since it divides by 64/65 then $N = 64$.
- **Choose the reference frequency** 25kHz is the channel spacing and is the best choice in this case.
- **Choose the crystal frequency** 2.5MHz is one possibility. The value of *R* can now be calculated:

  Crystal frequency = Reference frequency x *R* x 2
  So $R = 50$
- **Calculate the division ratio** (the ratio between the VCO output frequency and reference frequency)
  This is 17200 to 17600 in steps of 1.
- **Calculate values for A and M** The division ratio $NM + A$ is 17200 to 17600.

  So for the **minimum** frequency: $64M + A = 17200$
  If $A = 0$, $M = 268.75$
  This is not possible (it must be an integer) so this must be **decreased** to make $Mmin = 268$.
- **Draw up a table** for the required values of *A* and *M*

  Division ratio $(P) = NM + A$
  $= 64M + A$

  or use the calculator program listed in Table 2.

M	A	Division ratio	Output frequency (MHz)
268	48	17200	430.000
..	49	17201	430.025
..	50	17202	430.050
..	..	..	..
..	..	..	..
..	..	..	..
268	63	17215	430.375
269	0	17216	430.400
..	..	..	..
..	..	..	..
..	..	..	..
..	..	..	..
274	63	17599	439.975
275	0	17600	440.000

Table 4 Decimal values of A and M

These figures are acceptable:

$$N \geqslant A$$
$$P > M^2 - M$$

The values of *M*, *A* and *R* must be fed into the NJ8820/1 for each value of frequency required. (In this example the value of *R* is constant). The values must first be converted into BINARY format as shown in Table 5.

M (decimal	M (10 bit binary)									
	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
268	0	1	0	0	0	0	1	1	0	0
268										
268										
..										
..										
..										
..										
..										
..										
..										
274	0	1	0	0	0	1	0	0	1	0
275	0	1	0	0	0	1	0	0	1	1

Table 5a Binary values for M

A (decimal)	A (7 bit binary)						
	A6	A5	A4	A3	A2	A1	A0
48	0	1	1	0	0	0	0
49	0	1	1	0	0	0	1
50	0	1	1	0	0	1	0
..							
..							
..							
..							
..							
..							
..							
..							
63	0	1	1	1	1	1	1
0	1	0	0	0	0	0	0

Table 5b Binary values for A

R (decimal)	R (11 bit binary)										
	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
50	0	0	0	0	0	1	1	0	0	1	0
50											
50											
..											
..											
..											
..											
..											
..											
..											
..											
50											
50											

Table 5c Binary values for R

In each case the LSB is identified by the heading *M*0, *A*0 or *R*0.

The NJ8820 and NJ8821 require 32 bits of data to be transferred for each value of frequency. These 32 bits are composed of the 28 bits above (10 + 7 + 11) plus 4 redundant bits. The method of transferring this data is different for the two device types.

NJ8820 - data obtained from a PROM

NJ8821 - data obtained from a Microprocessor.

USING THE NJ8820

The NJ8820 operates with an external 4 bit wide PROM. Information is transferred automatically from the PROM to the NJ8820 when the *PE* pin is activated. A 1024 bit PROM (256 x 4) will store 32 channels because each channel requires the transfer of 8 words (32 bits) of data. A 256 x 4 PROM has 8 address lines (*A*0 to *A*7) of which the NJ8820 can address 3 (*A*0 to A2, connected to *DS*0 to *DS*2). The remaining 5 address lines allow the unique identification of the channel required (32 channels in this case) as shown in Table 6, so for each channel number there are 8 words, each of four bits. The composition of these words is as shown in Table 7. The '-' symbol indicates that this is not read - normally the 8 bit value is 0.

The value of the bits *D*3, *M*1, etc. can be either 0 or 1 and can be found from the tables in the previous section. For example, when $M = 268$ then $M1 = 0, M0 = 0$ and WORD 1 is 0000.

USING THE NJ8821 IN A PARALLEL MODE

The NJ8821 operates with an asynchronous stream of data supplied from a microprocessor. When used in a 4-bit parallel mode it requires the transfer of 8 words (32 bits) of data. Word numbers 1 to 3 control the '*M*' counter, 4 and 5 the '*A*' counter, 6 to 8 the '*R*' counter. It is not necessary to transfer all the words every time; WORD 1 indicates to the NJ8821 that the data should be transferred from all latches to counters and so WORD 1 must always be sent last. There are 8 data connections between the microprocessor and NJ8821:

- *DS*0, *DS*1 and *DS*2 to select the correct word
- *D*0, *D*1, *D*2 and *D*3 are the input data for *A*, *M* and *R* counters
- *PE* is the strobe

To enter channel information follow the sequence listed below:

1. Ensure the *PE* (strobe) is 0.
2. Select any word (except word 1)...(*DS*0 to *DS*2) and the relevant input data (*D*0 to *D*3).
3. Wait for 1 microsecond or more.
4. Pulse the strobe (to 1) for 2 microseconds or more and return to 0.
5. Wait for 1 microsecond or more.
6. Repeat (2) to (5) as required.
7. Repeat (2) to (5) for word 1.

The composition of the data words is identical to that for the NJ8820.

USING THE NJ8821 IN A SERIAL MODE

When used in a serial mode (using a single external shift register) the NJ8821 requires the transfer of 8 words, each of 7 bits (56 bits) of data to program the *A*, *M* and *R* counters but only 5 words (35 bits) subsequently to reprogram the *A* and *M* counters. There are thus only 3 data inputs from the microprocessor: DATA, CLOCK and STROBE, as shown in Fig.11.

	ADDRESS LINES								
	A7	A6	A5	A4	A3	A2	A1	A0	
CHANNEL NUMBER 0					0	0	0	0	word 1
					0	0	0	1	word 2
					0	0	1	0	word 3
					0				..
					0				..
					0	1	1	1	word 8
CHANNEL NUMBER 1	0	0	0	0	1	0	0	0	word 1
					1	0	0	1	word 2
					1	0	1	0	word 3
					1				..
					1				..
					1	1	1	1	word 8

Table 6 Channel identification

ADDRESS LINES					DATA LINES				WORD
-	-	A2	A1	A0	D3	D2	D1	D0	
		0	0	0	M1	M0	-	-	1
		0	0	1	M5	M4	M3	M2	2
		0	1	0	M9	M8	M7	M6	3
		0	1	1	A3	A2	A1	A0	4
		1	0	0	-	A6	A5	A4	5
		1	0	1	R3	R2	R1	R0	6
		1	1	0	R7	R6	R5	R4	7
		1	1	1	-	R10	R9	R8	8

Table 7 Channel number composition

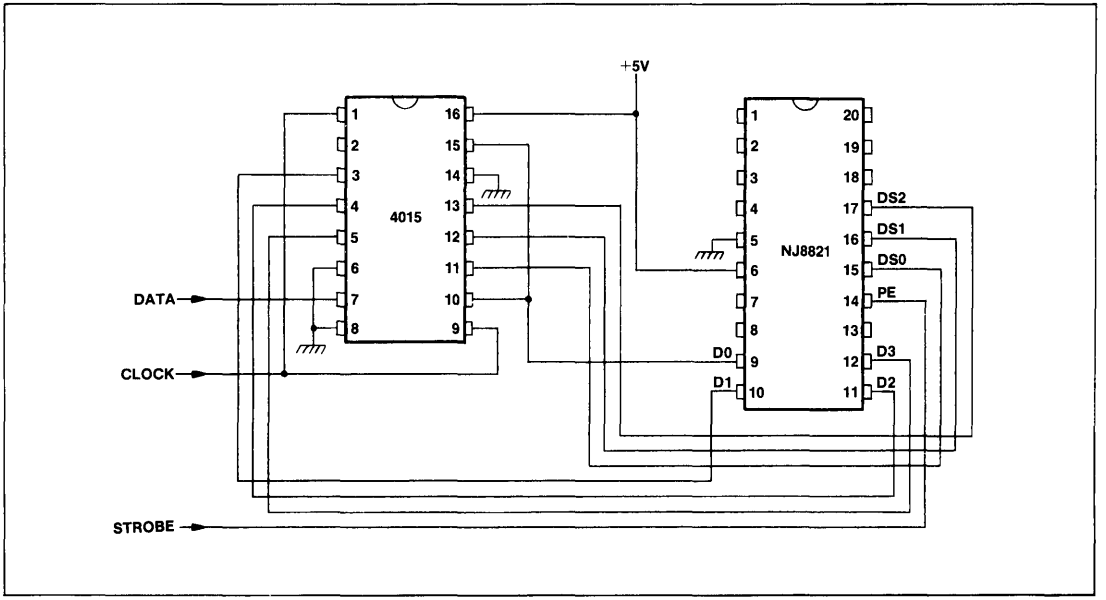


Fig.11 NJ8821 serial mode connections

The composition and entry sequence of the data words is identical to that of the NJ8820 except that the data is transmitted serially.

Once again, there is no need to transfer all the words every time provided that WORD 1 is always sent last.

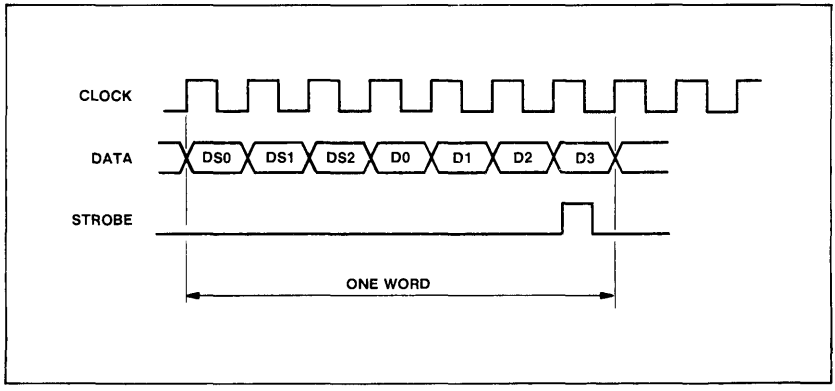


Fig.12 Serial data timing

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1. "Design Compromise in Single Loop Frequency Synthesisers" P.E. Chadwick, RF Design Expo, Anaheim, Ca. Jan 1985
2. Frequency Synthesisers, Theory and Design, V. Manassewitsch, Wiley, 1980, ISBN 0-471-07917-0
3. Digital PLL Frequency Synthesisers, U.L. Rohde, Prentice Hall, 1983, ISBN 0-13-214239-2
4. Phaselock Techniques, F.M. Gardner, Wiley 1979, ISBN 0-471-04294-3

A Serially Programmable VHF Frequency Synthesiser

This demonstration circuit uses three Plessey Devices - the NJ8822 single chip synthesiser, the SP8793 dual-modulus prescaler and the SL562 low noise op-amp in the configuration shown in Fig.1. The NJ8822 is programmed using a 'universal' programmer, the of which is shown in Fig.2.

The VCO is a JFET oscillator using a transmission line as the resonator. This VCO is modulated by applying the audio signal to the cathode of a reversed biased PIN diode as shown in the circuit diagram. The loop filter uses the SL562 which with the values shown has a loop bandwidth of 60Hz and a damping factor of 0.6. This filter is followed by a low pass pole at 3.7kHz to attenuate the 12.5kHz reference sidebands. The lock up time for a 1MHz change in frequency is 80ms (determined empirically). The output frequency range is 144-146MHz and the level is +3dBm into 50Ω.

The output spectra at 12.5kHz reference frequency is shown in Fig.3, and Fig.4 is a graph of modulating frequency against percentage distortion at several values of deviation. The circuit performs normally at a supply voltage of 5V ± 0.5V and within a temperature range of -30°C to +70°C. The only observable effect of varying the temperature was a frequency drift of 3kHz between the temperature extremes due to the uncompensated reference oscillator.

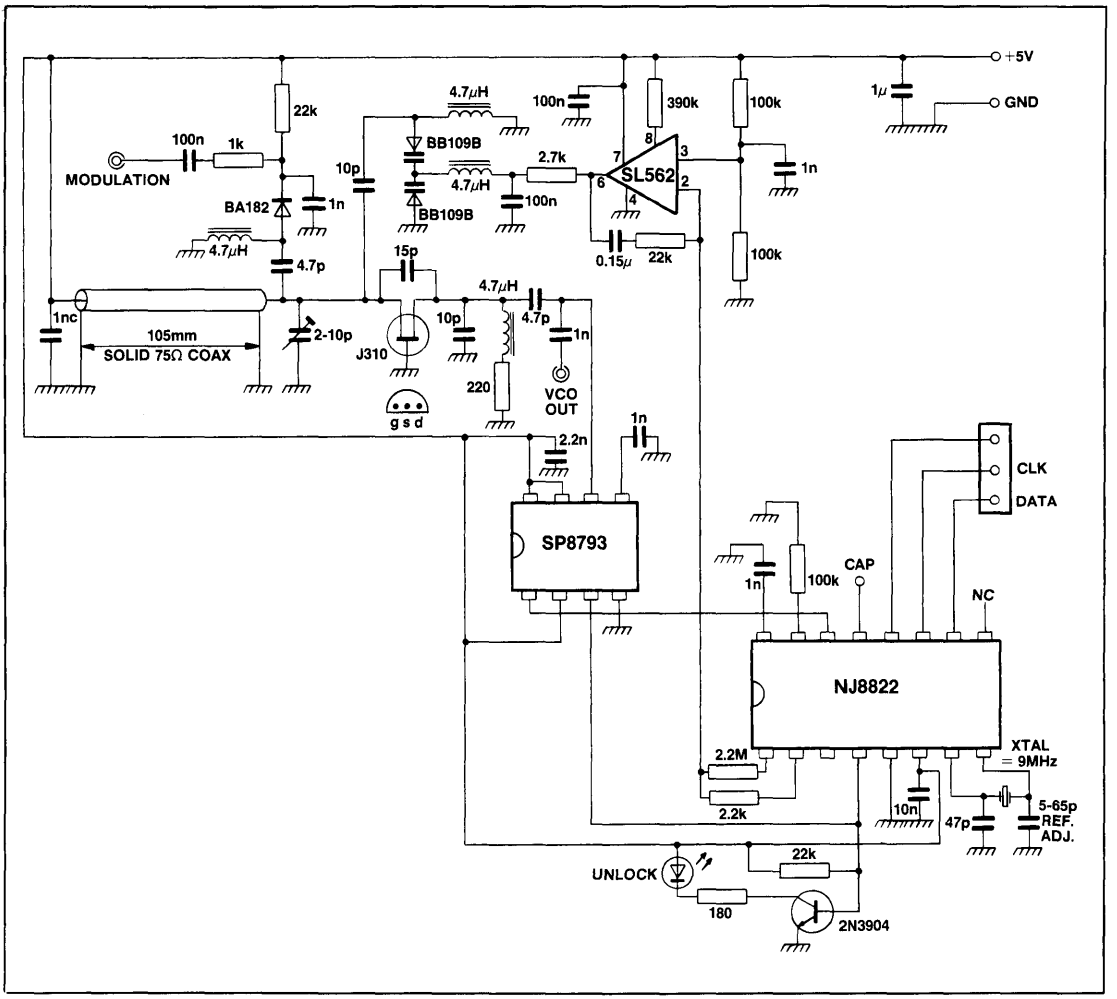


Fig.1 NJ8822 serially programmable VHF synthesiser

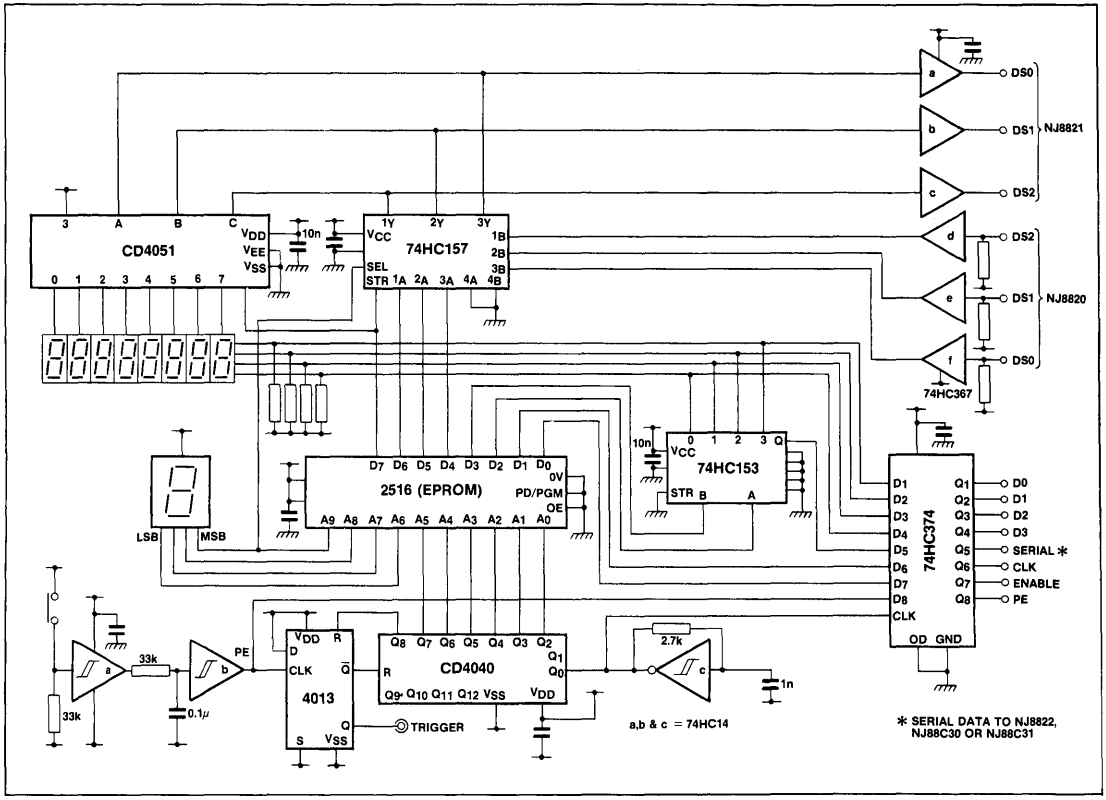
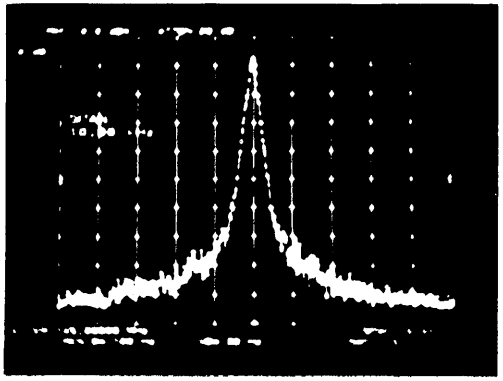
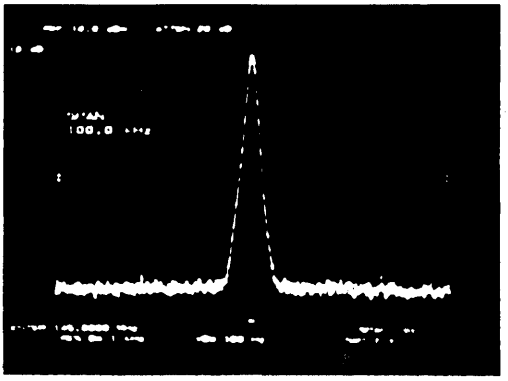


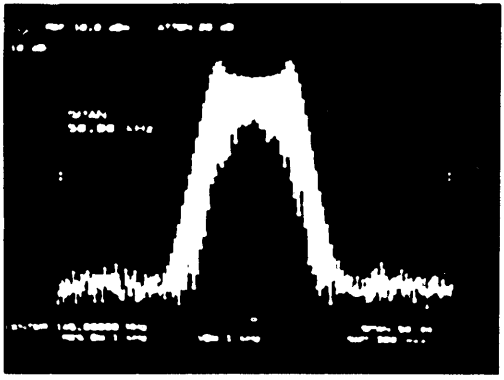
Fig.2 Universal programmer for NJ8820/21/22 & NJ88C30/31



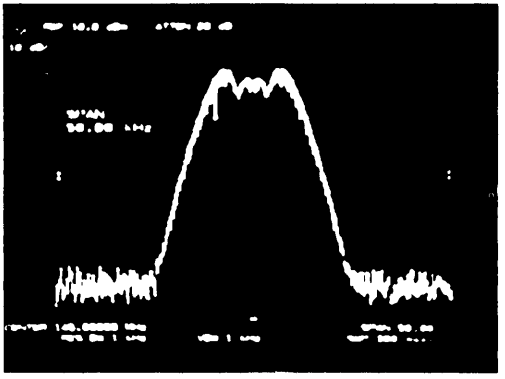
(a) Unmodulated 10kHz span



(b) Unmodulated 100kHz span



(c) Modulated 400Hz 5kHz deviation 50kHz span



(d) Modulated 1kHz 5kHz deviation 50kHz span

Fig.3 NJ8822 frequency synthesiser spectral performance

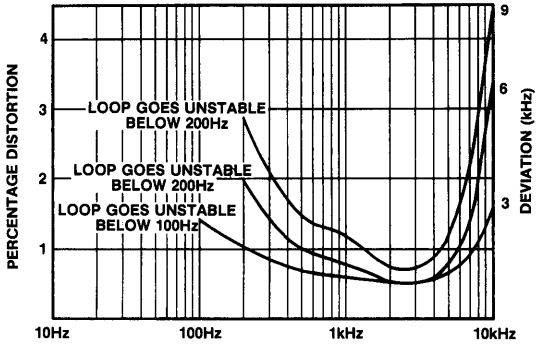


Fig.4 Graph of distortion against modulating frequency at various deviations for the NJ8822 VHF frequency synthesiser

Phase Noise Intermodulation and Dynamic Range

The radio receiver operates in a non-benign environment. It needs to pick out a very weak wanted signal from a background of noise at the same time as it rejects a large number of much stronger unwanted signals. These may be present either fortuitously, as in the case of the overcrowded radio spectrum, or because of deliberate action, as in the case of Electronic Warfare. In either case, the use of suitable devices may considerably influence the job of the equipment designer.

Dynamic range is a 'catch all' term, applied to limitations of intermodulation or phase noise: it has many definitions depending upon the application. Firstly, however, it is advisable to define those terms which limit the dynamic range of a receiver.

INTERMODULATION

This is described as the *'result of a non linear transfer characteristic'*. The mathematics have been exhaustively treated, and Ref.1 is recommended to those interested.

The effects of intermodulation are similar to those produced by mixing and harmonic production, insofar as the application of two signals of frequencies f_1 and f_2 produce outputs of $2f_2 - f_1$, $2f_1 - f_2$, $2f_1$, $2f_2$ etc. The levels of these signals are dependent upon the actual transfer function of the device and thus vary with device type. For example, a truly square law device, such as a perfect FET, produces no third order products ($2f_2 - f_1$, $2f_1 - f_2$). Intermodulation products are additional to the harmonics $2f_1$, $2f_2$, $3f_1$, $3f_2$ etc. Fig.1 shows intermodulation products diagrammatically.

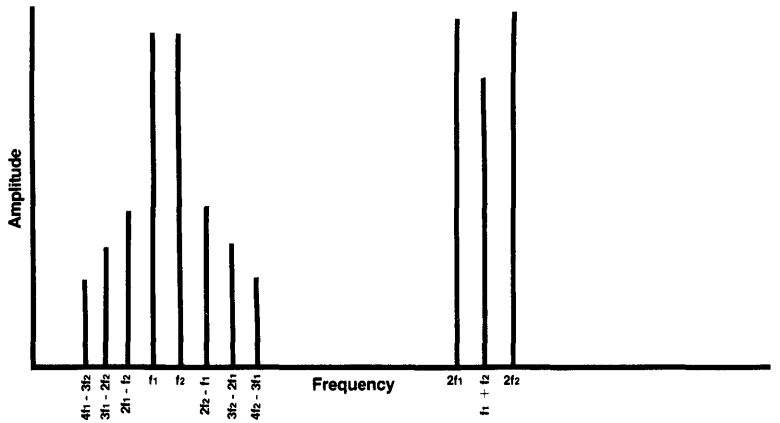


Fig.1 Intermodulation products

The effects of intermodulation are to produce unwanted signals, and these degrade the effective signal to noise ratio of the wanted signal. Consider firstly the discrete case of a weak wanted signal on 7.010MHz and two large unwanted signals on 7.020 and 7.030MHz. A third order product (2 x 7.02 - 7.03) falls on the wanted signal, and may completely drown it out. Fig.2 shows the total HF spectrum from 1.5 to 41.5MHz and Fig.3 shows the integrated power at the front end of a receiver tuned to 7MHz. It may be seen that just as white light is made up from all the colours of the spectrum, so the total power produced by so many signals approximates to a large wide band noise signal. Now, it has already been shown that two signals, f_1 and f_2, produce third order intermodulation products of $2f_1 - f_2$ and $2f_2 - f_1$. The signals will produce third order products somewhat greater in number, viz: $2f_1 - f_2$, $2f_1 - f_3$, $2f_2 - f_1$, $2f_2 - f_3$, $2f_3 - f_1$ and $2f_3 - f_2$. An increase in the number of input signals will multiply greatly the effects of intermodulation, and will manifest as a rise in the noise floor of the receiver.

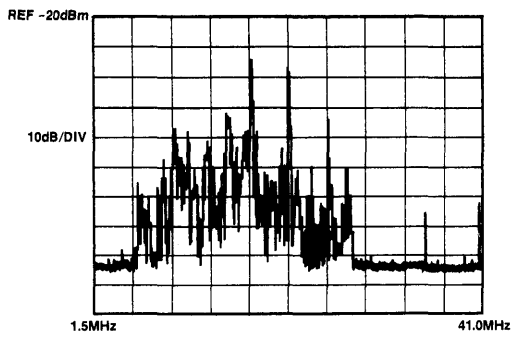


Fig.2

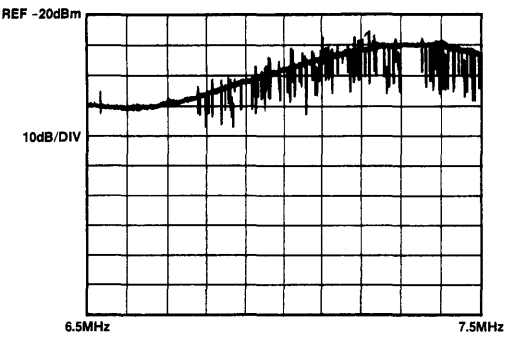


Fig.3

The amplitude relationships of the third order intermodulation products and the fundamental tones may be derived from Ref.1, where it is shown that the intermodulation product amplitude is proportional to the cube of the input signal level. Thus an increase of 3dB in input level will produce an increase of 9dB in the levels of the intermodulation products. Fig.4 shows this in graphic form, and the point where the graphs of fundamental power and intermodulation power cross is the *Third Order Intercept Point*.

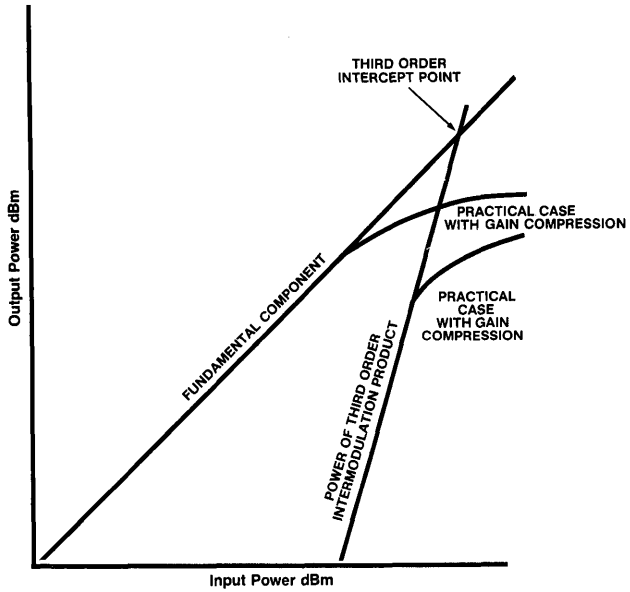


Fig.4 3rd order intercept

The third order intercept point is, however, a purely theoretical concept. This is because the worst possible intermodulation ratio is 13dB (Ref.2), so that in fact the two graphs never cross. In addition, the finite output power capability of the device leads to *Gain Compression*.

Thus, it is apparent that the intermodulation produced noise floor in a receiver is related to the intercept point. Figs.5, 6 and 7 show the noise floor produced by various intercept points, in a receiver fed from an antenna - a realistic test! Fig.5 shows that a large number of signals are below the noise floor and are thus lost; this represents a 0dBm intercept point. Fig.7 shows a +20dBm intercept noise floor, and it is obvious that many more signals may be received.

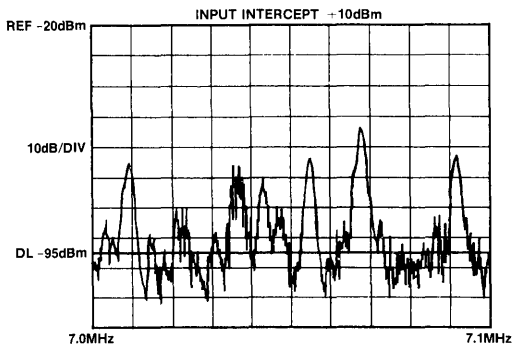


Fig.6

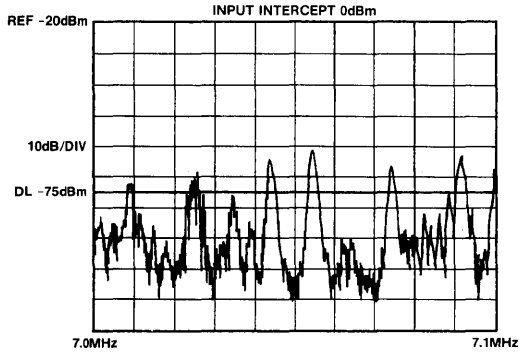


Fig.5

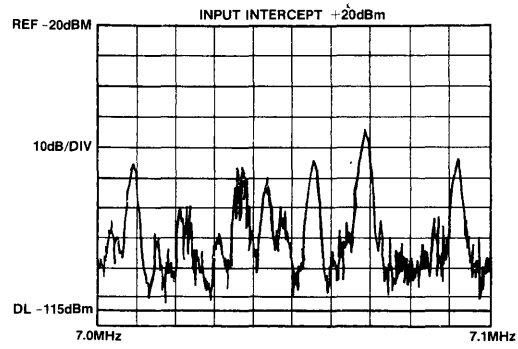


Fig.7

Because of the rate at which intermodulation products increase with input level (3dB on the intermodulation products for 1dB on the fundamental), the addition of an attenuator at the front end can improve the signal to noise ratio, as an increase in attenuation of 3dB will reduce the wanted signal by 3dB, but the intermodulation will decrease by 9dB. However, it is a fair comment that aerial attenuators are an admission of defeat, as suitable design does not require them!

The concept of dynamic range is often used when discussing intermodulation. Fig.8 shows total receiver dynamic range, which is defined as the spurious Free Dynamic Range. Obviously an intermodulation product lying below the receiver noise floor may be ignored. Thus the usable dynamic range is that input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. In fact

$$DR = \frac{2}{3}(I_3 - NF) \quad \ldots (1)$$

Where *DR* is the dynamic range in dB
I_3 is the intermodulation input intercept point in dBm
NF is the noise floor in dBm.

Note that in any particular receiver, the noise floor is related to the bandwidth; dynamic range is similarly so related.

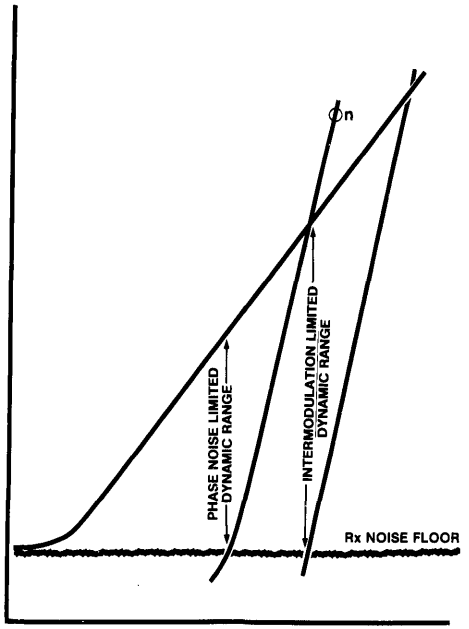


Fig.8

HF receivers will often require input intercept points of +20dBm or more. The usable noise factor of HF receivers is normally 10-12dB: exceptionally 7 or 8dB may be required when small whip antennas are used. An SSB bandwidth would have a dynamic range from (1) of 105.3dB. The same receiver with a 100Hz CW bandwidth would have a dynamic range of 114.6dB and thus dynamic range is quite often a confusing and imprecise term.

Appendix A defines a quantitive method of Intermodulation Noise Floor assessment, developed later than the data in Figs.5 to 7.

VHF receivers require noise figures of 1 or 2dB for most critical applications, and where co-sited transmitters are concerned, signals at 0dBm or more are not uncommon. However, such signals are usually separated by at least 5 % in frequency and filters can be provided. Close-in signals at levels of -20dBm are not uncommon, and dynamic ranges in SSB bandwidths of about 98dB are required.

The achievement of high input intercept points and low noise factors is not necessarily easy. The usual superhet architecture follows the mixer with some sort of filter, frequently a crystal filter, and the performance of this filter may well limit the performance. Crystal filters are not the linear reciprocal two-part networks that theory suggests, being neither linear nor reciprocal. It has been suggested that the IMD is produced by ferrite cored transformers, but experiments have shown that ladder filters with no transformers suffer similarly. Thus, although ferrite cored transformers can contribute, other mechanisms dominate in these components. The most probable is the failure of the piezo-electric material to follow Hooke's Law at high input levels, and possibly the use of crystal cuts other than AT could help insofar as the relative mechanical crystal distortion is reduced. The use of SAW filters is attractive, since they are not bulk wave devices and do not suffer to such an extent from IMD; however, it is necessary to use a resonant SAW filter to achieve the necessary bandwidths and low insertion losses.

The design of active components such as amplifiers is relatively straightforward. Amplifiers of low noise and high dynamic range are fairly easy to produce, especially with transformer feedback, although where high reverse isolation is required, care must be taken. Mixers are however, another matter.

Probably the most popular mixer is the diode ring (Fig.9). Although popular, this mixer does have some drawbacks, which have been well documented. These are:

Insertion loss (normally about 7dB)
High LO drive power (up to +27dBm)
Termination sensitive (needs a wideband 50Ω)
Poor interport isolation (40dB)

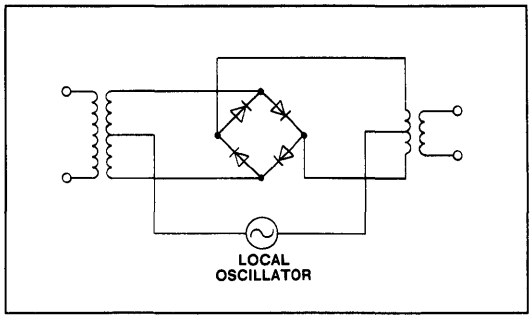


Fig.9 Diode ring

The insertion loss is a parameter which may be classed merely as annoying, although it does limit the overall noise figure of the receiving system. The high LO drive power means a large amount of DC is required, affecting power budgets in a disastrous way, while termination sensitivity may mean the full potential of the mixer cannot be realised.

For the diode ring to perform adequately, a good termination 'from DC to daylight' is required - definitely at the image frequency (LO ± sig. freq.) - and preferably at the harmonics as well. Finally, interport isolation of 40dB with a +27dBm LO still leaves -13dBm of LO radiation to be filtered or otherwise suppressed before reaching the antenna.

A further problem with the simple diode ring of this form is that the 'OFF' diodes are only off by the forward voltage drop of the ON diodes. Thus the application of an input which exceeds this OFF voltage leads to the diodes trying to turn ON, giving gain compression and reduced IMD performance.

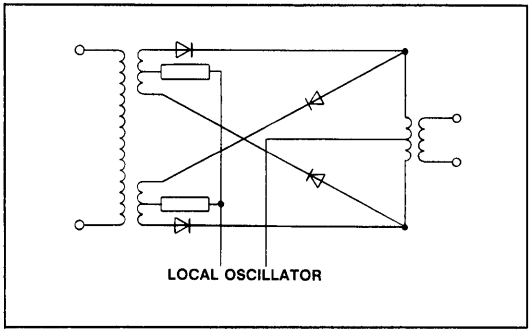


Fig.10 Resistive loaded high intercept point mixer

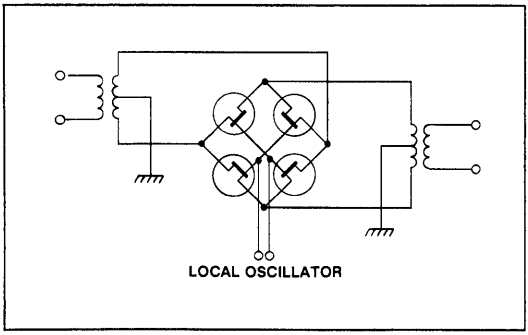


Fig.11 Quad MOSFET commutative mixer

Fig.10 shows a variation of this in which series resistors are added. The current flow through these resistors increases the reverse bias on the OFF diodes which gives a higher gain compression point: such a mixer can give +36dBm intercept points with a +30dBm of LO drive. Nevertheless, as is common to all commutative mixers, the intermodulation performance is related to the termination, and the LO radiation from the input port is relatively high.

Variations of this form of mixer include the Rafuse Quad MOSFET mixer of Fig.11, which suffers with many of the same problems. Fig.12 shows a dual VMOS mixer capable of good performance, but requiring a large amount of DC power and with limited isolation of the LO injection.

Many advantages accrue to the choice of the transistor tree type of approach (Fig.13). Here the input signal produces a current in the collectors of the lower transistors and this current is commutated by the upper set of switching transistors. Because the current is to a first order approximation independent of collector voltage, the transistor tree does not exhibit the sensitivity to load impedance that the diode ring does, and indeed, by the use of suitable load impedances, gain may be achieved. The non-linearity of the voltage to current conversion in the base emitter junctions of the bottom transistors is the major cause of intermodulation, but by using suitably large transistors and emitter degeneration, very high performances (+32dBm input intercept) can be achieved. The Plessey SL6440 has been described (Refs.3, 4, 5) and uses these techniques to achieve a high standard of performance (see Fig.16).

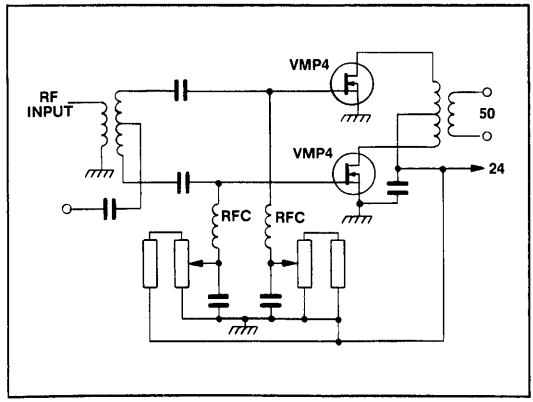


Fig.12 VMOS mixer

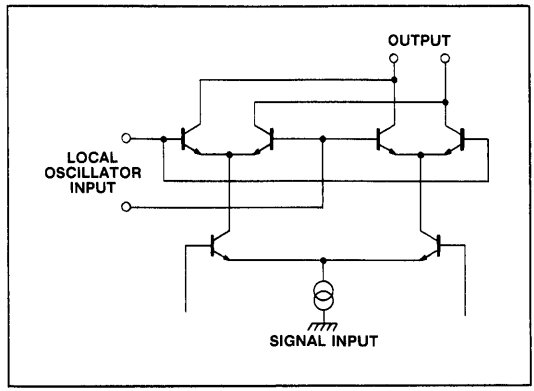


Fig.13 The transistor tree

PHASE NOISE

The mixing process for the superhet receiver is shown in Fig.14, where an incoming signal mixes with the local oscillator to produce the intermediate frequency. Fig.15 shows the effect of noise modulation on the LO, where the noise sidebands of the LO mix with a strong, off channel signal to produce the IF. This means that the phase noise performance of the LO affects the capability of the receiver to reject off channel signals, and thus the receiver selectivity is not necessarily defined by the signal path filters. This phenomena is referred to as *Reciprocal Mixing*, and has tended to become more prominent with the increased use of frequency synthesisers in equipments.

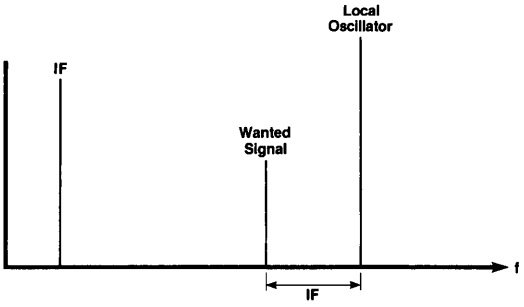


Fig.14 Superhet mixing

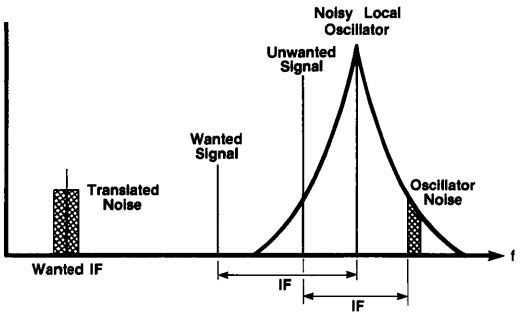


Fig.15 Reciprocal mixing

The performance level requirements of receivers is dependent upon the application. Some European mobile radio specifications call for 70dB of adjacent channel rejection, equating to some -122dBc/Hz, while an HF receiver requiring 60dB rejection in the adjacent sideband needs -94dBc/Hz at a 500Hz offset. The use of extremely high performance filters in the receiver can be completely negated if the phase noise is poor. For example, a receiver using a KVG XF9B filter with a rejection in the unwanted sideband of 80dB at 1.2kHz, would require a local oscillator with -114dBc/Hz phase noise at 1.2kHz if the filter performance was not to be degraded.

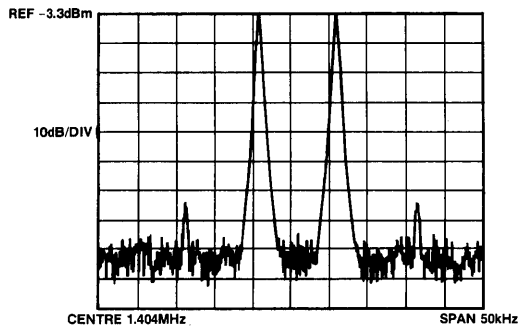


Fig.16 SL6440 intermodulation performance

To put these levels in perspective, relatively few signals generators are adequate to the task of being the LO in such a system. For example, 'Industry Standards' like the HP8640B are not specified to be good enough: neither are the HP8642, Marconi 2017/2018, or Racal 9082, all of which are modern, high performance signal generators.

All this suggests that it is very easy to over-specify a receiver in terms of selectivity, and simple synthesisers are not necessarily ideal in all situations.

The ability of the receiver to receive weak wanted signals in the presence of strong unwanted signals is therefore determined not only by the intermodulation capabilities of the receiver, but by phase noise and filter selectivity.

The usual approach to high performance synthesis has used multiple loops for good close-in performance. Notable exceptions are those equipments using fractional N techniques with a single loop. Nevertheless, such equipments not generally specified as highly as multi-loop synthesisers. A vital part of the synthesiser is still the low noise VCO, for which many approaches are possible. This VCO performance should not be degraded by the addition of the synthesiser: careful choice of technologies is therefore essential. For example, Gallium Arsenide dividers are much worse in phase noise production than silicon, and amongst the silicon technologies, TTL is better than ECL.

From equation (1)

$$DR = \frac{2}{3}(I_{p3} - NF) \text{ dB}$$

where I_{p3} = input intercept point dBm
NF = noise floor dBm

The phase noise governed dynamic range is given by

$$DR_{\Phi} = P_n + 10 \log_{10} B \; Db \qquad (2)$$

Where P_n is the phase noise spectral density in dBc/Hz at any offset and B is the IF bandwidth in Hz.

(N.B. This is not quite correct if B is large enough such that noise floor is not effectively flat inside the IF bandwidth).

Ideally the ratio

$$\frac{DR_{IM}}{DR_{\Phi}}$$

should be 1 in a well designed receiver - i.e. the dynamic range limited by phase noise is equal to the dynamic range limited by intermodulation.

Certain aspects of low noise synthesiser design have been touched upon and Ref.6 provides further information.

The performance of a receiver in terms of its capabilities to handle input signals widely ranging in input level is dependent upon the receiver capability in terms of intermodulation and phase noise. Neglect of either of these parameters leads to performance degradation, and it has been shown that specifications are not only often difficult to meet, but sometimes contradictory in their requirements.

This paper was first presented at the RF Technology Expo, Anaheim, Jan 1986.

P.E. Chadwick

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ANNEXE A

Intermodulation is caused by odd order curvature in the transfer characteristic of a device. If two signals f_1 and f_2 are applied to a device with third order term in its transfer characteristic, the products are given by:

$(\text{Cos}f_1 + \text{Cos}f_2)^3 = \text{Cos}^3f_1 + 3\text{Cos}^2f_1\,\text{Cos}f_2 + 3\text{Cos}f^2f_2\,\text{Cos}f_1 + \text{Cos}^3f_2$

from the trig identities Cos^3A, Cos^2A and CosACosB, this is

$\frac{1}{4}\text{Cos}^3f_1 + \frac{3}{4}\text{Cos}f_1 + \frac{3}{2}\text{Cos}^2f_1\text{Cos}f_2 + \frac{3}{2}\text{Cos}f_1\text{Cos}^2f_2 + \frac{3}{4}\text{Cos}f_2 + \frac{1}{4}\text{Cos}^3f_2 + \frac{3}{4}\text{Cos}f_2$

(where $f_1 = A$ and $f_2 = B$). Neglecting coefficients, the terms $\text{Cos}^2f_1\,\text{Cos}f_2$ and $\text{Cos}f_1\,\text{Cos}^2f_2$ are equal to

$\text{Cos}(2f_1 + f_2) + \text{Cos}(2f_1 - f_2)$ and
$\text{Cos}(2f_2 + f_1) + \text{Cos}(2f_2 - f_1)$

By inspection, it may be seen that frequencies of f_1, f_2, $3f_1$,$3f_2$, $(2f_1 \pm f_2)$ and $(2f_2 \pm f_1)$ are present in the output. Of these, only $2f_2 - f_1$, and $2f_1 - f_2$ are close to wanted frequencies f_1 and f_2.
The application of three signals f_1, f_2 and f_3, produces a similar answer, in that the resulting products are:

$3f_1$, $3f_2$, $3f_3$, $f_1 + f_2 + f_3$, $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$, $f_1 - f_2 - f_3$, $f_2 - f_1 + f_3$, $f_2 - f_1 - f_3$, $-f_1 - f_2 - f_3$, $-f_1 - f_2 + f_3$

in addition to the products

$2f_1 \pm f_2$, $2f_2 \pm f_1$, $2f_2 \pm f_3$, $2f_3 \pm f_2$, $2f_1 \pm f_3$, $2f_3 \pm f_1$

if a greater number of signals are applied such that the input may be represented by:

$\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n$

The result from third order curvature can be calculated from:

$(\text{Cos}f_1 + \text{Cos}f_2 + \text{Cos}f_3 + \text{Cos}f_4 \ldots \text{Cos}f_n)^3$

This expansion produces terms of

$\text{Cos}(f_1 \pm f_2 \pm f_3)$, $\text{Cos}(f_1 \pm f_2 \pm f_4)$, $\text{Cos}(f_1 \pm f_2 \pm f_n)$ etc from which it can be seen that the total number of products is:

$$\frac{n!}{3!(n-3)!} = 4 \times \tfrac{1}{6}n\,(n-1)(n-2)$$

(The factor of 4 appears because each term has four possible sign configuratons i.e. $\text{Cos}(f_1 + f_2 + f_3)$, $\text{Cos}(f_1 + f_2 - f_3)$ etc). This agrees with Ref A1.
By a similar reasoning, n signals produce:

$2n(n-1)$ produces of the form $(2f_1 \pm f_2)$ $(2f_2 \pm f_1)$ etc and n 3rd harmonics.

Thus the total number of intermodulation produces produced by third order distortion is:

$$n + 2n(n-) + \tfrac{2}{3}n\,(n-1)(n-2) \qquad (1)$$

Reduction of the input bandwidth of the receiver modifies this. Consider, for example, a receiver with sub-octave filters, rather than the 'wide-open' situation analysed above. In this case, the third harmonics produced by any input signals will not fall within the tune band, as will some of the products such as $f_1 + f_2 + f_3$, $f_1 - f_2 - f_3$, etc. In this case, the total number of intermoduation products is reduced. There are only three possible sets of products of the form f_1 $f_1 \pm f_2 \pm f_3$, i.e. $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$ and $f_3 - f_1 - f_2$ which can give products within the band. Note that for products to be considered, they must have an effective input frequency at the receiver mixer equivalent to an on-tune desired signal. In addition, products of the form $2f_1 + f_2$, $2f_2 + f_1$ etc are again out of band. Thus half of the $2n\,(n-1)$ products of this class are not able to cause problems and the total number of products to be considered is now:

$$n\,(n-1) + \tfrac{1}{2}n\,(n-1)(n-2) \qquad (2)$$

This result does not agree with Barrs (Ref A2) who uses the results in (1). The results in (2) are an absolute worst case, insofar as a number of the intermodulation products are out of band.

(For the purposes of this analysis, IMD in a mixer is assumed to produce an 'on tune' signal. Thus not all the possible intermodulation frequencies appearing in a half octave bandwidth will be able to interfere).

The same arguments apply to narrower front end bandwidths. However, the narrower the front end bandwidth, the higher is the probability that the distribution of signals will produce IMD products outside the band. For example, a receiver with ±2.5% front end bandwidth tuned to 10MHz will accept signals in a band from 9.75 to 10.25MHz. Signals capable of producing a product of the form $2f_1 - f_2$ must have one of the signals (f_1 or f_2) in the band 9.875 - 10.25 for a product to appear on tune. Thus the two signal apparent bandwidth is less than would be expected. Similar constraints apply to the $f_1 + f_2 - f_3$ product.

Similar arguments apply to other orders of curvature. Second order curvature, for example, will not produce any products in band for input bandwidths of less than 2:1 in frequency ratio.

The actual levels of intermodulation produced can be predicted from reference A1. In practice, the situation is that the input signals to a receiver are rarely all of equal unvarying amplitude and assumptions are made from the input intercept points and the input signal density.

If a series of amplitude cells are established for given frequency ranges, such as that in Table 1, then a prediction of the number of intermodulation products for any given number of input signals and amplitudes may be obtained, either from equation (1) or (2) (as applicable) or from Ref A1 (for higher orders). Where the input bandwidth of the receiver is deliberately minimised, the maximum cell size in the frequency domain should be equal to the input bandwidth.

The total input power in each cell is

$nPav$

where n is the number of signals and Pav is the average power of each signal.

A worst case situation is to assume that all signals in the cell are equal to the cell upper power limit boundary, e.g. if the cell amplitude range is from -40 to -30dBm, then an assumption that all signals in this cell are at -30dBm is a worst case.

If, however, it is assumed that signals will have a Gaussian distribution of input levels within a cell, then the total input power becomes:

$$Pt = 0.55nP$$

where Pt is the total power
n is the number of signals
P is the power level at the upper boundary of the cell

Because the total IMD power is the sum of all the IMD powers, the average input power is

$$Pav = \frac{0.55nP}{n}$$

The IMD power produced by third order curvature is:

$$10 \log_{10} [\tfrac{1}{3}n(2n^2 + 1)] \text{ Antilog } \tfrac{1}{10}[Pav - 3(I_3 - Pav)]dBm$$

where P_{IM} is the total power of the intermodulation products
I_3 is the third order input intercept point

Because the coefficients of the amplitudes of the intermodulation products are (depending on product)

$$a^3, a^2b, ab^2, abc, b^3$$

where a, b and c are approximately equal, the use of a^3 as the general coefficient is justified.

From equations (1) or (2) and (3), the total IMD power and number of products may be calculated. As 'n' increase in number, the number of products will mean that the resultant IMD tends more to a noise floor increase in the receiver, thus reducing the effective sensitivity.

The amount of this degradation is such that the noise floor is:

$$\frac{\frac{2}{3}(0.55nP)^3}{I_3} \times \frac{I_3}{(f_{max} - f_{min})} \times \Delta f$$

where $(f_{max} - f_{min})$ is the bandwidth prior to the first intermodulating stage. Δf is signal bandwidth in a linear system. The Gaussian Factor of 0.55 is somewhat arbitrary, since errors in this assumption are cubed.

The intermodulation Limited Dynamic Range is

$$\tfrac{2}{3}(I_3 + 174 - 10 \log_{10} \Delta f - NF)$$

where NF is the Noise Figure in dB.

The effects of Reciprocal Mixing are similar, except that signals may be taken one at a time. The performance is affected by the frequency separation between an 'off-tune' interfering signal and an 'on-tune' wanted signal unless the separation is such that the oscillator noise floor has been reached. Here again, reduction of front end bandwidth reduces the number of signals.

Generally speaking, the effects of reciprocal mixing are limited to close in effects - say within $\pm$50kHz, unless very poor synthesisers are used.

The response at some separation f_0 from the tune frequency is: $(L - 10 \log_{10} 10\Delta f)$dB where L is phase noise spectral density in dBc/Hz and Δf is the IF bandwidth.

This assumes that the spectral density does not change within the receiver bandwidth: Ref A1 shows this to be generally applicable for narrow bandwidths.

The intermodulation free dynamic range is defined as:

$$\tfrac{2}{3}[I_3 - \text{noise floor}] = \tfrac{2}{3}[I_3 + 174 - 10 \log_{10} \Delta f - NF]dB$$

where I_3 is the input 3rd order intercept point in dBm
NF is the noise figure in dB
Δf is the IF bandwidth in Hz

It has been claimed (Ref A3) that there is 6dB rejection of phase noise in diode commutative mixers. Thus the relationship between IMD and phase noise can be expressed as:

IMD dynamic range = phase noise dynamic range +6dB = (L - 10 $\log_{10}$ Δf) + 6dB

Thus at any offset, it is important to ensure that the two dynamic ranges are approximately equal if performance is not be be compromised.

A receiver for example with an input intercept point of +20dBm and input signals of -30dBm will produce an IMD product at -130dBm which, for an HF receiver with a noise factor of 8dB, will be just above the noise floor, in an SSB bandwidth. The noise floor of the LO will need to be such that the noise is at -133dBm if degradation is not to occur, and this will be produced by a noise floor of -137dBc/Hz in the synthesiser at the frequency separation of the signals in question. Thus the high intermodulation performance may well be compromised by poor phase noise.

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Design Compromises in Single Loop Frequency Synthesisers

The single loop frequency synthesiser is justly popular as an approach to frequency synthesis. It has the merit of simplicity, and because of this, low cost, especially as a large amount of the circuitry is easily produced in monolithic integrated circuit form.

Certain performance parameters of the synthesiser are defined by the equipment performance. For example, a marine VHF radio frequency synthesiser has requirements for phase noise and discrete spurious outputs defined by the adjacent channel specification, and the phase noise performance may well need to be several dB better than would at first be expected. If the adjacent channel rejection is 70dB for example, then a single sideband phase noise level in the receiver bandwidth must be more than 70dB, see Fig.1. In fact, the translated noise level should be reduced by an amount dependent upon the performance of other areas of the equipment and these specification levels are typically determined by the system architect. Frequently, however, during design of a project, some modifications in architecture become apparent, but an understanding of practical limitations is vital at an early stage if delay and consequent expense is to be avoided. For further details on the effects of phase noise on receiver performance, see Ref.1.

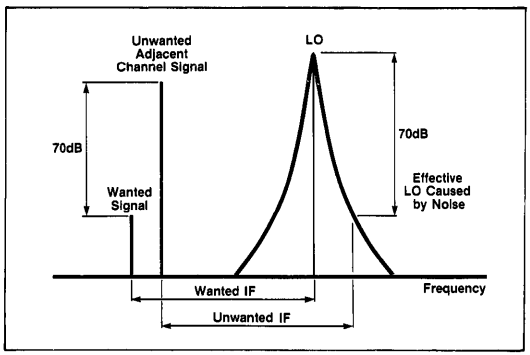

Fig.1 Phase noise and adjacent channel rejection

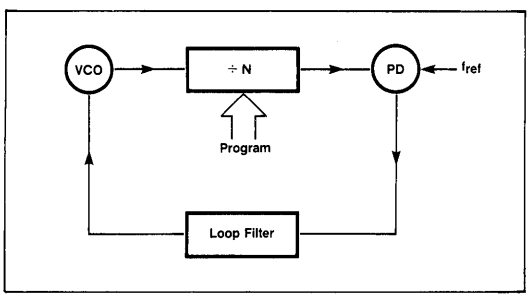

Fig.2 Simple PLL

DIVIDERS

Single loop synthesisers using direct division as in Fig.2 suffer from certain limitations. Fully programmable dividers are not generally available for frequencies above about 50MHz without high power consumptions, and even CMOS dividers currently available are limited in applications at low (5V) supply voltages and extreme temperatures. Newer devices are appearing, however, and experimental 250MHz operation has been observed.

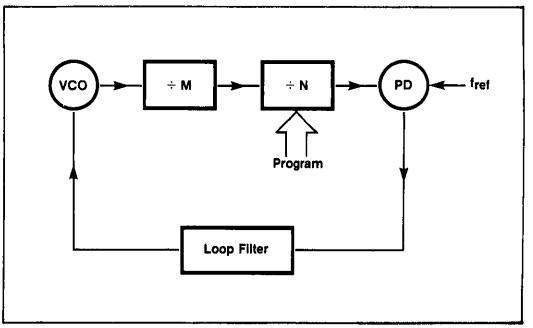

Fig.3 Use of a fixed prescaler

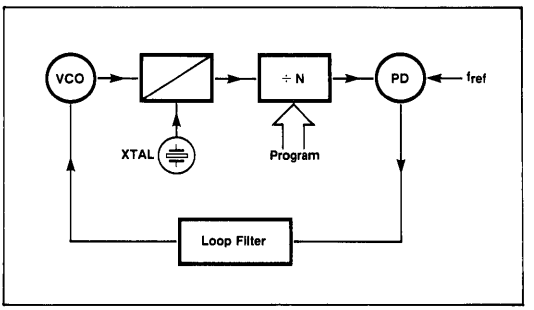

Fig.4 Mixing in the loop

Early synthesisers used fixed prescalers to divide the VCO down to a suitable frequency for the programmable counter as in Fig.3, or used mixing techniques as in Fig.4. Indeed, a large number of CB radios use the mixing technique, but this system can suffer from spurious products unless carefully designed in choice of frequencies, input levels and particular mixers used, see Refs. 2,3,4 and 5. In addition, the large variation in subsequent division ratio may give problems with loop dynamic performance.

A major area of conflict lies in the choice of reference frequency. In synthesisers such as Fig.3, the output frequency step size is *M* times, the reference frequency, where *M* is the prescale ratio. In a system where every channel is used, the problem is then that the reference frequency has to be decreased by a factor of *M*, and as a result, the bandwidth of the feedback loop must decrease. The bandwidth and damping factor of the loop filter are vitally important parameters in determining such loop characteristics as lock up time as well as the phase noise characteristics. (The effects of loop bandwidth on phase noise will be discussed later.) In general, the widest possible loop bandwidth is required to minimise lock up time and to confer the greatest immunity to shock and vibration. However, the loop bandwidth cannot be greater than the reference frequency and so the use of a fixed prescaler is obviously somewhat limited. The alternative is the widely used 'Two Modulus' or 'Pulse Swallowing' prescaler system, illustrated in Fig.5. In this method, the prescaler is able to divide by two integers *N* and *N* + 1. The two counters *A* and

M are programmable and are clocked in parallel, the divider being set initially to the $N + 1$ ratio. When the A counter is full, the divider is set to divide by N until the M counter is full, giving a total division ratio of $MN + A$. This system is limited to a minimum division ratio of $N^2 - N$ if every value of N is to be achieved (no 'skipped' channels) and the M counter must always be programmed to a bigger number than the A counter. Within these limitations, however, a fully programmable divider is achieved and so f_{ref} can now equal the channel spacing.

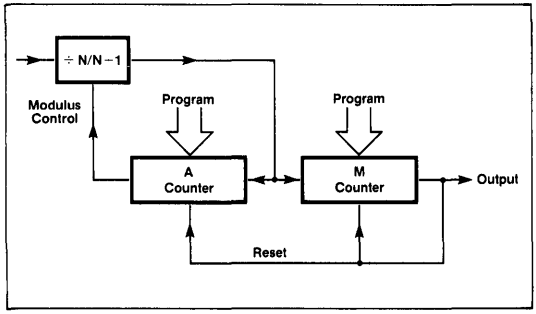

Fig.5 Two modulus divider

Another and more subtle limitation is in the delay times of the various components within the loop. When the circuit (Fig.5) has counted down so that the M counter has been filled, the whole system is reset, and quite obviously, must achieve this in a time equal to $N + 1$ cycles of the input frequency e.g. in a ÷64/65 prescaler, at 1GHz, the reset of the M and A counters must be achieved in 65 cycles or in this case, 65ns. This means that the propagation delays plus set up/release times plus reset delays must not exceed 65ns and it is this area where trouble can often be expected, especially at temperature extremes. Although a 1GHz synthesiser with a 64/65 divider only sees an input frequency of 15MHz for 1GHz input, the set up/release time and delays may well easily reach 85-90ns and the system will thus fail.

If the propagation through the divider $= t_d$
the set up time $= t_s$
the release time $= t_r$
the propagation delay through the A and M counters $= t_c$

then

$$f_{max} = \frac{N}{(t_d + t_s + t_c)} \text{ or } \frac{N}{(t_d + t_r + t_c)}$$

whichever is least.

One of the areas in which an increase in loop delay time can inadvertently occur is if the A and M counters trigger from a different edge to the dual modulus prescaler. This can cause a major diminution in available loop delay, as can an attempt to physically separate the divider and control circuits. Other deleterious affects have been noted, such as radiation of the divider output to the VCO, producing high frequency sidebands, so practical synthesisers are best produced with little physical spacing between divider and control circuit.

The control circuit is a practical device in a number of technologies, although modern devices exclusively use CMOS to minimise power consumption. Prescalers are still mainly exemplified by bipolar technology, advances in which have seen major reductions in power consumptions in recent years - for example from 65mA at 5V for a divide by 10/11 operating at 250MHz in 1976 to 4mA at 5V for a divide by 40/41 operating at 225MHz today. Some equipments still build up the A and M counters from discrete ICs and then add phase detectors, reset circuitry and so on, but such equipments are by now obsolete in design and extremely expensive to manufacture. Nevertheless, the lessons of tolerancing delays necessary in such designs should not be forgotten just because the majority of circuitry is now hidden inside a block of silicon.

The choice of prescaler ratio is governed by a number of factors. Discussed so far have been minimum ratio and loop delay. However, the output frequency of the divider must be low enough for the A and M counters to function. Summarising

1. $f_{in} \leqslant N f_{max\ control}$
   where N is the divider ratio
   $f_{max\ control}$ is control circuit maximum operating frequency.
2. $f_{min} \leqslant \dfrac{N}{\text{total loop delay}}$
3. $P_{min} = N^2 - N$
   where P_{min} is the minimum divide ratio.
   N is the dual modulus divider ratio.

Various values for N exist in proprietary devices. These range from 3/4 to 128/129: binary values (32/33, 64/65, 128/129) are popular for ease of programming from ROMs and microprocessors, while decimal and BCD are used for thumbwheel switch programming.

Programming is a straightforward exercise for binary division and the following method is recommended.

1. The A counter should contain x bits such that
   $$2^x = N$$
2. If more bits are included in the A counter, these should be programmed to zero.

e.g.
$N = 64 = 6$ bits
$A = 10$ bits
then the 4 MSB are programmed to zero.

3. The M and A counters are treated as being combined so that the MSB of the M counter is the MSB of the total and LSB of the A counter is the LSB of the total.

e.g.
A synthesiser operating from 430-440MHz in 25kHz steps uses a 64/65 divider, and the control circuit uses binary counters.
$P = f/f_{ref}$ and f_{ref} = channel spacing $= 25$kHz
$P_{min} = 430/0.025 = 17200$
$P_{max} = 440/0.025 = 17600$

Minimum possible divide ratio is $N^2 - N = 4032$
where N is two modulus divider ratio

Maximum allowable loop delay $= \dfrac{64}{440 \times 106} = 145$ns

Total divide ratio, P, is given by
$P = NM + A$
$N = 64$, as a 64/65 divider is used
P_{min} from above is 17200
Therefore $17200 = 64M + A$
And $M \geqslant A$

Let $A = 0$ Then $M_{min} = \dfrac{17200}{64} = 268.75$

$= 268$

and $M_{max} = \dfrac{17600}{64} = 275.0$

Thus the M counter must be programmable from 268 to 275 as required: the M counter must have at least 9 bits.

For a frequency of 433.975MHz

$$P = 433.97/0.025 = 17359$$

therefore $$M = \frac{17359}{64} = 271.2343$$

The *A* counter is programmed for the remainder i.e.

$$0.2343 \times 64 = 15$$

From this, the *A* counter is programmed to 15 and the *N* counter to 271. The output frequency can now be checked.

$P = NM + A$
$= 271 \times 64 + 15 = 17359$
and this is the required divider ratio.

The two modulus prescaler is therefore able to offer the advantages of producing a programmable divider operating at a very high frequency, but consuming a fraction of the power of such a divider. This enables the reference frequency to equal the channel spacing, thus allowing maximisation of loop bandwidth with its concomitant faster lock up time. It is limited by total loop delay, maximum operating frequencies of dividers and counters, and in minimum count values, but is nevertheless a powerful tool for the synthesiser designer.

The limitation on the value of P_{min}, the minimum ratio can be avoided by the use of three and four modulus dividers. The use of a four modulus counter allows a very wide frequency range to be covered with one device, but at the expense of a much higher power dissipation. Typical of such devices are the Plessey SP8901 and SP8906. Power consumptions for 2-modulus dividers typically range from 4mA at 200MHz (Plessey SP8792/3) through 11mA at 520MHz (Plessey SP8716/8/9) to 25mA at 1GHz (Plessey SP8703).

LOOP BANDWIDTH AND PHASE NOISE

As stated earlier, phase noise is a very important parameter in frequency synthesisers. Too many early synthesisers suffered from phase noise problems which manifested themselves as poor equipment performance in such areas as multiple signal selectivity and ultimate signal to noise ratio. The performance of the synthesiser may be degraded or improved by changing the loop bandwidth, depending upon the characteristics and parameters involved.

The general characteristics of a phase locked loop (PLL) are that for signals injected into the loop it acts as a low pass filter for signals inside the loop bandwidth, and as a high pass filter for signals outside the loop bandwidth. To analyse the performance, consider modulation of the VCO at very low frequencies. The output of the phase detector will be a low frequency signal of phase such as to attempt to remove the modulation imposed on the VCO. As the modulation frequency increases, the error component of the phase detector output is not passed by the loop filter, and so the modulation is not removed by the loop. Note that the modulation is phase modulation (PM) up to the filter break point, and frequency modulation (FM) thereafter. In the 'in-between' range, some interesting distortion effects can occur, especially when excessive group delay exists in the loop filter.

The relationship of loop filter bandwidth to phase noise is now apparent. Phase noise from the oscillator corresponding to frequencies below the filter bandwidth will be removed by the loop, while phase noise components outside the loop bandwidth will be unaffected by the loop. Under these circumstances then, the VCO output spectrum will be cleaned up by the loop. However, for frequencies inside the loop bandwidth, other factors enter. Variations in the reference frequency cause variations in output frequency from the synthesiser, and phase noise components at the reference frequency are purely the frequency domain transforms of time domain frequency instability (Refs. 6,7 and 8). These phase noise effects are multiplied in the loop by the divider ratio. An example (admittedly using gross instability for demonstration) is shown.

If the 430MHz synthesiser has an instability of +1Hz in the 25kHz reference frequency, this is multiplied by *P*.

i.e. for operation at 433MHz
$P = 433/0.025 = 17320$

Therefore IF +1Hz at 25kHz gives +17.32kHz at final frequency.

Phase noise at the reference frequency is derived from two sources:

(a) the system standard oscillator
(b) the reference chain divider

Oscillators for standards are available with very low phase noise characteristics, and -130 to -170dBc/Hz at 1kHz offset covers the usual range. This phase noise is modified by the reference divider and multiplied by the division ratio as explained above. Of course, phase noise at any offset is reduced by division until the phase noise floor of the divider is reached. Little has been published on the causes of phase noise in dividers, although various measurements have been made (Ref. 9). It has been suggested that TTL and CMOS dividers are better than ECL and CMOS is better at low (10-20Hz) offsets. At a 1kHz offset, ECL levels of about -155 to -165dBc/Hz appear usual. The explanations for the occurence of phase noise is intuitively regarded as being jitter in the transition point of the signal: on this basis, one would not expect CMOS to be so good as TTL insofar as the rise and fall times will be somewhat slower. Regrettably, the difficulty and cost of making meaningful measurements is an inhibiting factor: data on the phase noise performance of Gallium Arsenide dividers would be of considerable interest, especially at small frequency offsets.

From the above discussion, a phase noise floor of some -150dBc/Hz can be expected at the end of the reference frequency divider chain if a good frequency standard is used, while a low cost one may well be at about -130dBc/Hz. In our 430MHz synthesiser, a degradation at 1kHz (if the loop is wide enough) of some 84dB will be seen, so inside the loop bandwidth, the noise performance will be limited to -130 + 84 = -46dBc/Hz. At lower offset frequencies, the phase noise of dividers and frequency standards is worse, so the phase noise performance is now being defined by the loop, rather than the VCO. These are worst case figures, but the ultimate signal to noise ratio of an FM receiver can clearly be seen to be easily limited at UHF by multiplied phase noise. Fortunately, the noise enhancement by the loop is such that pre-emphasis of the modulation provides major improvements in signal to noise ratio.

Nevertheless, it is obvious that the choice of loop bandwidth is compromised by the ultimate signal to noise level required by the system and that such factors as reference oscillator noise level and divider noise cannot be totally disregarded. Operation in the usual cellular radio bands at 800 or 900MHz makes the situation some 6dB worse than that analysed above and the use of a psophometric audio weighting in the equipment is advisable. Sub audible tones may well need fairly high deviation if signal to noise performance is not to be severely limited on them, although modern decoders will work with a negative signal to noise ratio (Ref.10).

In the single loop synthesiser, the phase noise in adjacent channels, which determines the adjacent channel performance, is, to a first order, unaffected by the loop and its parameters. Second order effects such as noise modulation

by such loop components as high value resistors and operational amplifiers may be negated by the use of a passive low pass filter prior to the VCO. Phase noise in the oscillator is discussed below.

Even where the effects of multiplied phase noise may be ignored, such as where the reference divider chain noise is sufficiently low, certain other problems occur in the loop filter design. Many of these are associated with the phase detector employed, which in many areas has been a digital phase/frequency detector. Various types of detector have been used over the years, from an OR gate producing a variable mark space ratio to the well known 2 D type detector. The first of these used integration of the variable mark-space ratio to produce the required output, while the latter (Fig.6) produces minimal width pulses on both Φu and ΦD when in the zero phase error condition. Unfortunately, the zero phase error state exists for a degree of phase error dependent upon the propagation of the gates and a phase error/output voltage characteristic such as Fig.7 is achieved. The performance in the central flat portion of the characteristic means that the loop gain falls to zero when the phase error reaches some small but finite value, and this leads to an increase in the low frequency phase noise of the loop. This phenomenon is of course related to the reference frequency of the loop, being worse at high comparison frequencies.

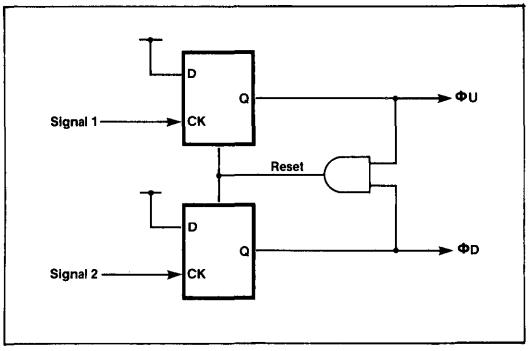

Fig.6 Dual D type phase discriminator

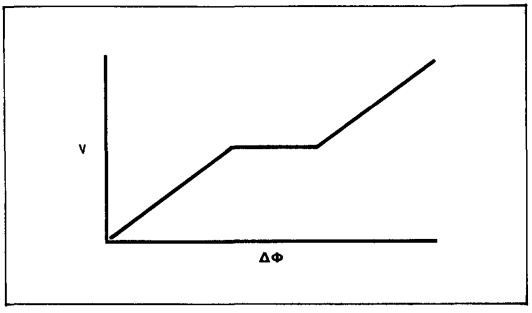

Fig.7 Transfer characteristic of phase discriminator with a charge pump

Although a number of approaches have been made to minimise this problem, including the provision of a leakage path across the VCO control line (Ref. 16), the better approach is to use a linear phase detector of high gain to 'fill in' the gap in the response. An additional benefit of this method is that if the digital phase detector has a 'tri-state' output for the area in which the dead zone occurs and the linear phase detector operates, then the phase detector output at comparison frequency is reduced, allowing either a wider loop bandwidth for the same comparison frequency sideband rejection, or increased rejection, or to some extent, both. The analog phase detector may easily be given a very high gain and narrow range of operation - say a 2 degree range with a gain of 600 volts/radians, but only a limited lock range. It is however, essential to ensure that saturation of this detector, and indeed of the loop filter/amplifier is minimised, as under channel change conditions, the control line and thus the filter amplifiers can be driven hard into saturation. A long recovery time here may well make a mockery of any lock up time calculations. It is this approach which has been adopted in the NJ8820 series of CMOS control circuits from Plessey with a large degree of success.

The choice of loop bandwidth is also governed by the time to change channel, and here again, compromise is often necessary. For example, a lock up time of 1ms and a loop bandwidth of 100Hz are apparently mutually incompatible. By using the two detector approach outlined above however, the loop bandwidth for the digital detector may be made much wider than the analogue detector, thus providing a form of adaptive filtering. The basic loop equation for a type 2 2nd order loop is

$$\omega_n = \sqrt{\frac{K_0 K_v}{N t_1}}$$

where ω_n = loop natural frequency, K_v = VCO gain in Rad/S-v, K_0 = phase detector gain in volts/rad, N = division ratio and t_1 = integrator time constant, shows the dependence of ω_n, the loop natural frequency on N. It should be noted the 3dB bandwidth of the loop and the natural frequency ω_n, are not identical - except for a damping factor, $D = 3.02$.

It was stated earlier that noise caused by the phase detector and loop filter is easily filtered to avoid noise in adjacent channels and the use of low-noise components in loop filters (NOT a 741!) is advisable. Where possible, time constants should use large capacitors and small resistors to minimise KTBR noise. 1/f noise can be a problem with operational amplifiers, and where loop bandwidth is high, slew rate is important if the dynamic loop bandwidth is to beary any relationship to the small signal case.

To summarise, the choice of loop bandwidth affects close in phase noise and lock up time. Phase noise is produced by dividers, phase detectors and filters, and when multiplication ratios are high, the reference frequency phase noise can be dominant when multiplied. To minimise this effect, the loop bandwidth can be narrowed, since noise outside the loop bandwidth is determined soley by the VCO. Typical divider phase noises of -150 or -160dBc/Hz can be expected, so low cost reference oscillators can dominate the noise performance.

VOLTAGE CONTROLLED OSCILLATORS

Many engineers consider VCO design to be a black art, and although some art is occasionally involved, VCOs are amenable to analysis.

In the single loop synthesiser, the phase noise performance outside the loop bandwidth is dominated by the VCO, with the noise generation by passive components in the loop filter generally being of lesser importance.

Scherer, Leeson (Ref.12) and Robins (Ref.13) have analysed oscillator phase noise performance and Scherer (Ref.14) has demonstrated the applicability of Leeson's equations and uses the equation

$$L_{(f)} = \tfrac{1}{8} \left[\frac{FkT}{P_s}\right] \frac{(fo)^2}{(f)} \left[\frac{1}{Q} + \frac{P_o}{\tfrac{1}{2}CV^2 2\pi f.}\right]^2 \quad \text{Eq. 1}$$

where $L_{(f)}$ is the SSB phase noise at an offset F
F is the Noise Figure of the amplifier in the oscillator
k is Boltzmann's Constant
T is the Temperature
P_s is the available signal power
f_o is operating frequency
f is the offset at which the power is to be calculated
Q is working Q of the tuned circuit
C is tank capacity
V is tank current peak voltage
P_o is rf output power

By inspection of Eq. 1, it may be seen that the phase noise is proportional to Q^{-2} and also to (frequency offset)$^{-2}$. This means that for each octave decrease in the offset frequency, the noise power will increase by 4 times or at 6dB/octave. As the frequency offset decreases $1/f$ or flicker noise becomes important: this 'break' frequency can be as high as 50MHz with GaAs devices. From Eq. 1, it may be determined that a low phase noise oscillator will have a large voltage swing, a high working Q and provide little output power to the load. There is of course a limit as to the level of power required, as the noise of any subsequent buffer amplifiers will degrade the oscillator.

A major compromise in the design of equipment is the choice of VCO frequency. If, for example, a 800MHz cellular radio type of receiver is considered, some fairly straightforward calculations will serve to act as a guide. Starting with the receiver parameters, we will assume that a 70dB rejection of a signal two channels (60kHz) away is required. A numbr of receiver sub system parameters are involved.

(a) Synthesiser phase noise
(b) IF filter performance
(c) Co-channel rejection ratio
(d) Gain compression of stages before the main IF selectivity.

Of these parameters, (c) is the least obvious in its applicability. Ref.1 showed how oscillator noise was mixed onto a wanted signal by a strong unwanted signal. The degradation of a wanted signal by this noise obviously depends upon the relative levels of signal and noise, and because the noise is on the same frequency, the Co-channel rejection. Typically, this means that a noise level within the IF passband of some 8dB less than the signal is required. Thus for the 70dB rejection, oscillator noise at -78dB is required, and 80dB would thus be the design aim.

Conversion of this level to dBc/Hz is not straightforward because of the non linear slope of the phase noise. However, for narrow bandwidths at large offsets, little error is obtained by approximating the phase noise slope to a straight line. This may be illustrated as follows:

From Eq. 1, the power spectrum at an offset beyond the flicker noise knee is given by:

$$P_o = Kf^{-2}$$

where P is the noise power
K is a constant
f is the offset

For a frequency band bounded by f_{lower} and f_{upper}, the noise power is:

$$P_t = \int_{f_L}^{f_U} Kf^{-2}\,df = \left[-Kf^{-1}\right]_{f_L}^{f_U}$$

$$= K(f_L^{-1} - f_U^{-1})$$

Therefore

$$K = \frac{P_t}{(f_L^{-1} - f_U^{-1})}$$

P_t has been defined as the phase noise in the band $= -80$dB therefore

$$K = \left[\frac{10^{-8}}{\frac{1}{53.5 \times 10^3} - \frac{1}{67.5 \times 10^3}}\right] = 2.58 \times 10^{-3}$$

To find the phase noise in a 1Hz bandwidth at an offset f

$$P = Kf^{-2}$$

so at 53.5kHz

$$P = \frac{2.58 \times 10^{-3}}{(53.5 \times 10^3)^2} = 0.901 \times 10^{-15}$$

$$= -120.5\text{dBc/Hz}$$

At 60kHz

$$P = -121.4\text{dBc/Hz}$$

and at 67.5kHz

$$P = -122.5\text{dBc/Hz}$$

If the 'break point' for $1/f$ noise is above 60kHz, then the spectral density is determined by noise rising at f^{-3}. Similar procedures are followed:

$$P_o = K'f^{-3}$$

$$P_t = \int_{f_L}^{f_U} K'f^{-3}\,df = -K'\left[\frac{f^{-2}}{2}\right]_{f_L}^{f_U}$$

$$= \frac{-K'}{2}(f_U^{-2} - f_L^{-2})$$

$$= \frac{K'}{2}(f_L^{-2} - f_U^{-2})$$

Using similar figures, the performance required is:

53.5kHz	-120.0dBc/Hz
60.0kHz	-121.5dBc/Hz
67.5kHz	-123.0dBc/Hz

The error by assuming a linear relationship is given by:

IF bandwidth = 15kHz
therefore noise power is $10 \log_{10} 15 \times 10^3$dB greater than in a 1Hz bandwidth
which is 41.8dB
therefore if the noise power is 80dB down on the signal, total carrier to noise power ratio is -121.8dBc/Hz at 60kHz.

This in fact gives a requirement some 0.4dB higher than previously calculated and in 120dB is obviously negligible.

Having decided upon the level of allowable oscillator noise, it is now possible to calculate the best methods of achieving this level. Using Scherer's figures from Ref.13 for a 400MHz oscillator which will be doubled, using parameters of:

$Q = 200$
$C = 23$pF
$V = 10$V pk
$\frac{FKT}{P^5} = \left[\frac{6\text{nV}}{1\text{V}}\right]^2$ where 6nV is the noise voltage and 1V is the input before limiting.

The noise power P at a 30kHz offset is, from Eq. 1, -135dBc/Hz.

So far flicker noise has been ignored. Flicker noise is a low frequency phenomonen which causes problems by intermodulation with the carrier frequency to produce noise sidebands. The 'break point' at which flicker noise becomes dominant varies but a UHF VCO of the type under consideration would probably have a break point at about 50-150kHz offset from the carrier. Eq. 1 needs some

modification to include this factor and a multiplicand of

$$\frac{(1 + f_e)}{f}$$

may be used, where f_e is the 1/f noise corner frequency.

The previously calculated noise will now be degraded by about 8dB under these conditions, (assuming f_e = 150kHz) and will now be -127dBc/Hz. This is about 5dB inside the previously calculated requirement. Note that calculations have been made on the basis of a 30kHz offset to allow for doubling the oscillator frequency.

Considering an oscillator with a fundamental frequency of 800MHz, a number of problems appear. Ignoring for the time being the increased noise figure of the device, the available Q of components is considerably less - for example high quality chip capacitors can offer Q's of about 200, leading to working Q of about 100. Calculating noise levels for a 60kHz offset with all other parameters constant except tank capacity which is 12pF (half the 400MHz oscillator) the noise at 60kHz is -105dBc/Hz or about 17dB outside the requirement. Obviously, these figures are no more than a guide, but the suggestion is that the doubled 400MHz oscillator will meet requirements, while the 800MHz oscillator will not (see Fig.8).

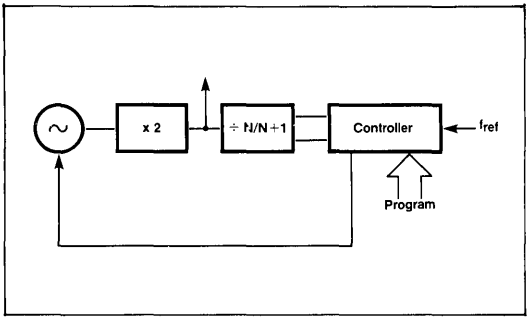

Fig.8 Use of a lower frequency oscillator for improved phase noise

Flicker noise can be reduced by the inclusion of local DC negative feedback, such as an unbypassed emitter resistor, but a major requirement is to choose a suitable device. In general a low phase noise oscillator will run at high power, using a device with both low flicker noise and low high frequency noise, and with high gain and minimum damping on the tuned circuit. In fact, in many applications, the thermionic tube is attractive! Q should be as high as possible, and where VCOs are concerned, the MHz/V should be minimised. This is because of the effects of noise - at 10MHz/V, 1 microvolt of noise will produce 10Hz of FM deviation.

Where relatively wide frequency ranges are concerned, the variation in loop bandwidth may cause problems.

$$\omega_n = \sqrt{\frac{K_o K_v}{N t_1}}$$

where ω_n = natural loop frequency
K_o = VCO constant
K_v = phase detector constant
N = divider ratio
t_1 = integrator time constant

ω_n varies with N, and where desirable to maintain equal lock up times and loop bandwidth, K_v may be designed to vary with N. Several methods exist, but the use of a transmission line VCO can prove useful, as the effective inductance increases with frequency. The use of a suitable length of transmission line can provide an oscillator tuneable from 130 to 190MHz with a coarse tuning trimmer, and electrically tuneable over 6MHz at the bottom of the band to 8.75MHz at the top, thus maintaining ω_n sensibly constant. The use of PIN diodes to switch capacitors is possible, although care must be taken not to degrade Q e.g. a 10pF capacitor at 150MHz has X_c = 106Ω. A PIN diode with an ON resistance of 0.5Ω will give Q_{MAX} = 212, assuming a perfect capacitor, and as considered earlier, this can have disastrous effects on phase noise performance.

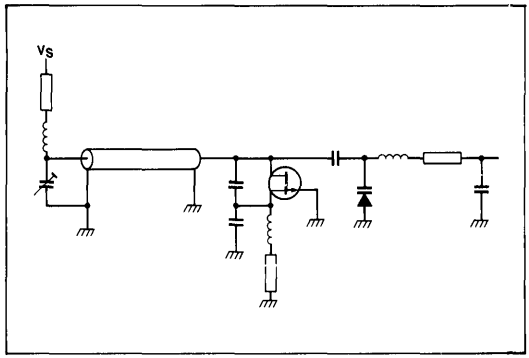

Fig.9 Transmission line VCO using the line as an impedance inverter

An initially attractive method of realising the transmission line VCO is shown in Fig.9, where a length of line is used as a reactance inverter, changing the capacity into an inductance. The use of a Smith Chart will, however, show that the resulting inductance will have a low reactance unless the terminating capacitor is large and the line relatively long (greater than ⅛ wavelength). This leads to a low Q circuit as the resistance of the line is constant, and measurements made using a 16cm rigid coax 75Ω line with a loss of 4dB/100ft at 150MHz gave a Q of less than 100. This line was terminated with an air spaced trimmer. The same line as a shortened capacitively loaded resonator as in Fig.10 had a Q of over 250.

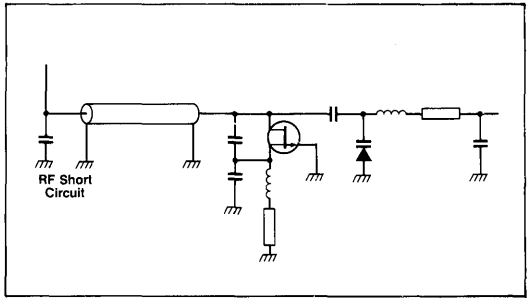

Fig.10 Transmission line VCO using a shortened λ/4 line capacitively loaded

SUMMARY

The compromises in the synthesiser design are now apparent: a narrow bandwidth is required to minimise multiplied reference noise, but a wide bandwidth is needed to minimise lock up time. A high oscillator frequency may be required to avoid spurious outputs and multiplier chains, while a low frequency and multiplier chain give the best performance on system phase noise and possibly power consumption. The classical way to minimise these problems is the two loop synthesiser, but cost is a determining factor effecting the compromise finally reached. Power consumption is always a problem and unfortunately is more demanding at high frequencies while increasing channel occupancy will lead to ever tighter performance requirements in terms of phase noise and switching time.

Modern integrated circuits help the designer by providing better phase detectors and faster lower power dividers. Nevertheless, the single loop synthesiser has been shown to involve a number of compromises in its design, and in some cases, these compromises may limit the final equipment performance level. The single loop synthesiser is very useful, but is not universally applicable.

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SL6637 Direct Conversion Receiver Applications

The SL6637 is a lower power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capabilities of 'power down' for battery conservation and control of an external DC-DC converter if single cell operation is required. The device also comes equipped with high current beeper drive and low battery flag indicator.

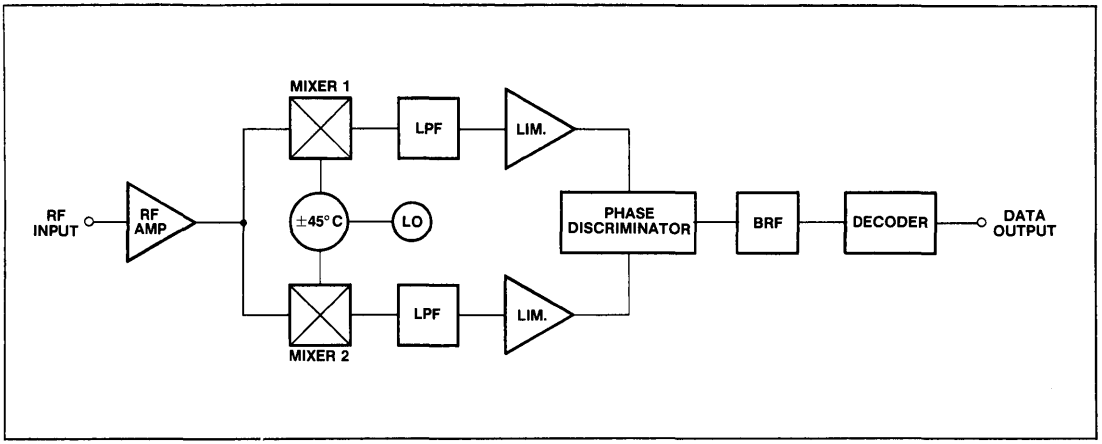


Fig.1 Block diagram of SL6637

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency-converted to base band. The two paths are produced in phase quadrature (see Fig.1) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig.2. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig.2 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency.

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states.

By applying the amplified outputs of the mixers to a phase discriminator, therefore, the digital data is reproduced.

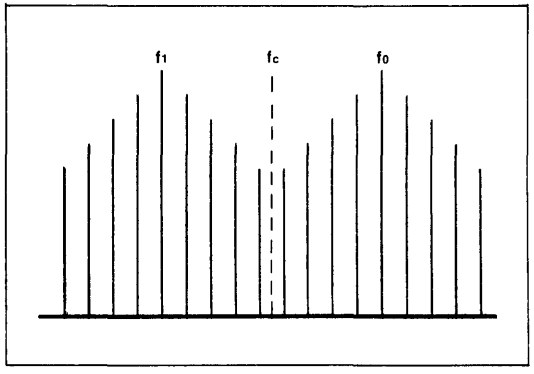


Fig.2 Spectrum diagram

If the waveform at limiter '1' input leads the waveform at the limiter '2' input by 90°, output at the detector output will be a high level, and low at the Data Output.

If the waveform at limiter '1' input lags the waveform at the limiter '2' input by 90° C, output at the detector output will be a low level and high at the Data Output.

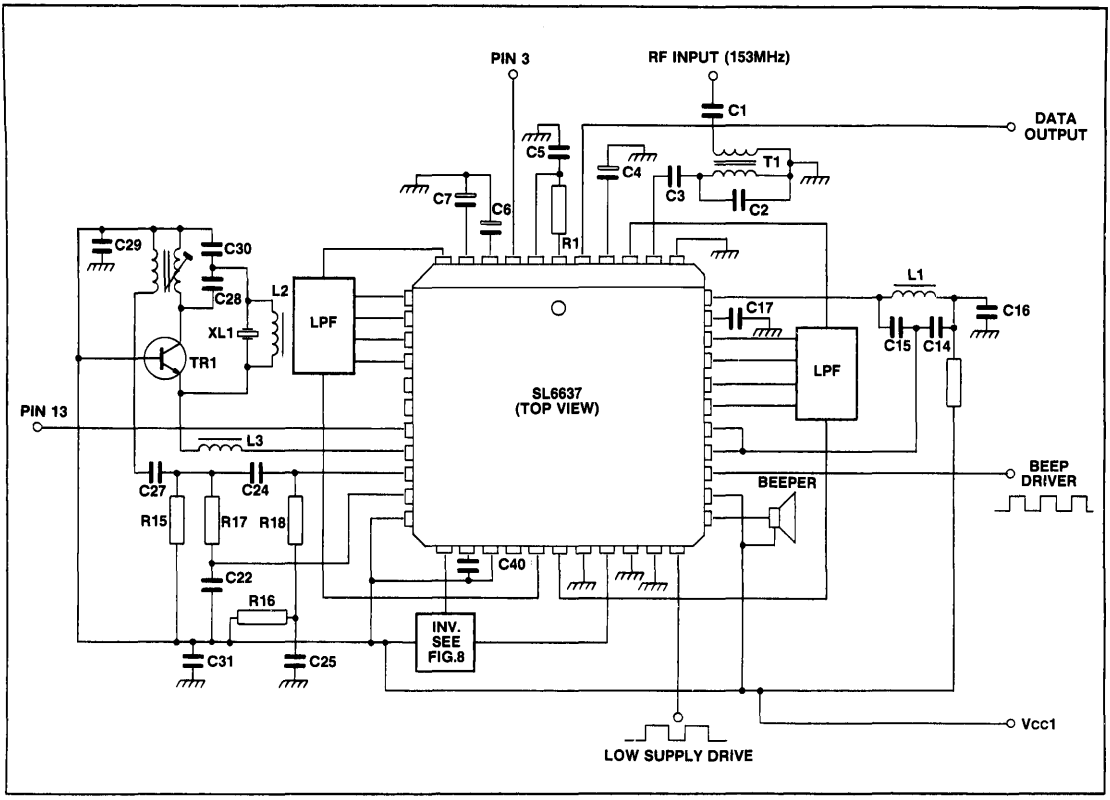


Fig.3 SL6637 applications circuit

R1	220k	C1	1n	C26	22n	L1 3 turns of 0.46 dia.
R2	15k	C2	3.9p	C27	1n	enamelled wire on 3.5mm
R3	100	C3	1n	C28	15p	dia. form (available from
R4	39k	C4	10µ	C29	1n	Wainwright Instruments,
R5	22k	C5	1n	C30	22p	type VCF-1)
R6	2.7k	C6	10µ	C31	1n	
R7	180k	C7	10µ	C32	10µ	L2 220nH choke
R8	22k	C8	8.2n (5%)	C33	47µ	
R9	15k	C9	2.2n (5%)	C34	10n (5%)	L3 10µH choke
R10	100k	C10	2.2n	C35	8.2n (5%)	
R11	6.8k	C11	1n//180p (5%)	C36	22n	L4 10µH choke
R12	27k	C12	2.2n	C37	180 (5%)	
R13	10k	C13	2.2n (5%)	C38	1n//180p (5%)	T1 as L1 but with a con-
R14	12k	C14	27p	C39	470p (5%)	centric winding of 3 turns
R15	100	C15	8.2p	C40	1µ	
R16	100	C16	1.2n	C41	10n	T2 as L1 but with an
R17	100	C17	1.2n			axial winding of 4 turns
R18	100	C18	100	TR1	BFY90	
R19	6.8k//100k	C19	470 (5%)	TR2	2N3906	T3 30 turns of 36 swg
R20	22k	C20	180 (5%)	TR3	2N3904	enamelled wire wound
R21	15k//180k	C21	10n (5%)			on a SE1 MM428P ferrite
R22	2.7k	C22	8.2p	D1	1N4148	ring
R23	22k	C23	1n	D2	1N4148	
R24	39k	C24	8.2p			XL1 153MHz 7th/9th
R25	15k	C25	1n	IC1	SL6637	overtone xtal

Table 1 Component values for Fig.3

CIRCUIT DESCRIPTION See Figs.1 and 3

The RF input, which is an FSK signal, is applied to the RF amplifier, and from the output of this stage to the mixers. The local oscillator inputs of these mixers are driven in phase quadrature from the crystal controlled oscillator, phase shift being produced by a resistor-capacitor network. The frequency of the local oscillator is equal to the nominal carrier frequency, and the mixer outputs at baseband are filtered in the active filters, which provide selectivity. In theory, a receiver using 'zero IF' has infinite adjacent channel rejection. The AF outputs of the LPF's are in turn fed to the inputs of two limiting amplifiers which provide most of the receiver gain, and the outputs of which feed the detector. This consists of a number of phase detectors arranged to provide phase comparison on four pairs of signal edges, thus maximising sensitivity. The detected output is now filtered in the Bit Rate Filter, and applied to a further limiter, providing the received data at the output.

The RF Amplifier

This is a single NPN transistor whose bias is provided internally and whose terminals are available on pins 39, 40 and 41.

There is a collector tuned load and tuned transformer T1 is included at the input to simulate an antenna.

A set of s-parameters is included (see Fig.15) to facilitate the optimum design of input and output networks for the RF amplifier.

The Mixers and Quadrature Network

The two mixers are fed with local oscillator energy via an RC network which provides 90° phase shift between the two LO inputs on pins 15 and 16. The signal inputs are on pins 33 and 32 respectively and the mixer outputs are on pins 23 and 22.

It is also possible to include the quadrature network in the RF signal path in which case pins 15 and 16 are fed directly from the LO.

A plot of S_{11} measurements is included to enable optimum matching of the quadrature network to pins 15 and 16 (see Fig.16).

The RC network employed in this application is shown in Fig.4.

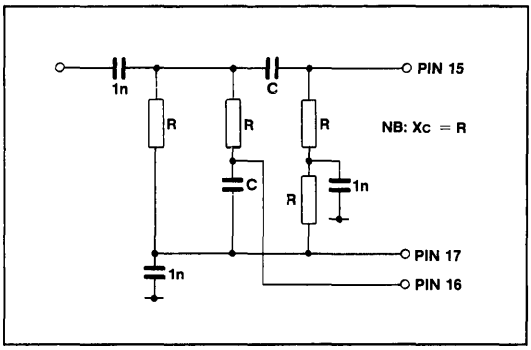


Fig.4

The Local Oscillator

The circuit employed in this application uses a BFY90 transistor and a 7th or 9th overtone crystal and is illustrated in Fig.5. The 220nH inductor L2 in parallel with the crystal suppresses oscillation at the crystal fundamental.

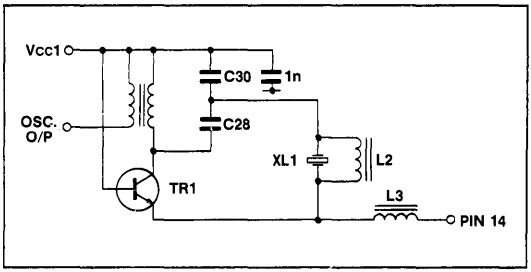


Fig.5

The Active Filters

These are 4-pole low-pass filters utilising the high gain inverting amplifier and the unity gain emitter follower available on the device. These amplifiers are configured as a multiple feedback LP filter and a Salen and Key LP filter respectively. There are two passive RC networks which provide a further two poles.

The following equations may be used to design the filters.

MFB low pass filter (Fig.6(a))

1. Select C_1 and C_2 such that $C_2 = 10/fc\ \mu F$ and $C_1 =$ or $C_{2/2}$ $(K + 1)$ where K is the required gain.

2. Resistance values are found by:

$$R_2 = \frac{2(K+1)}{\left[\sqrt{2C_2} + \sqrt{2C_2^2 - 4C_1C_2(K+1)}\right]\omega_c}$$

$$R_1 = R_2/K$$

$$R_3 = \frac{1}{C_1C_2\omega_c^2R_2}$$

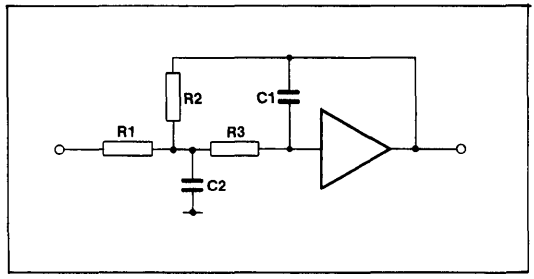


Fig.6(a)

Salen & Key low pass filter (Fig.6(b))

1. Select $C_2 = 10/fc\ \mu F$ and $C_1 = C_{2/2}$.

2. Resistance values are found by:

$$R_1 = \frac{2}{\left[\sqrt{2C_2} + \sqrt{2C_2^2 - 8C_1C_2}\right]\omega_c}$$

$$R_2 = \frac{1}{C_1C_2R_1\omega_c^2}$$

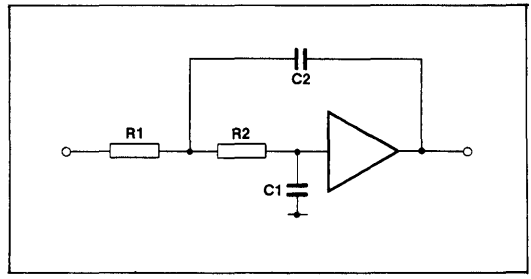


Fig.6(b)

RC single pole filter (Fig.6(c))

$C = 10/fc\ \mu F$

$R = 1/\omega_c C$

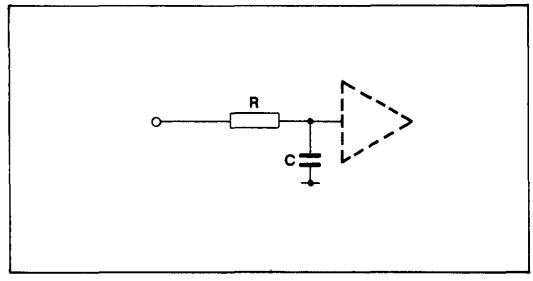


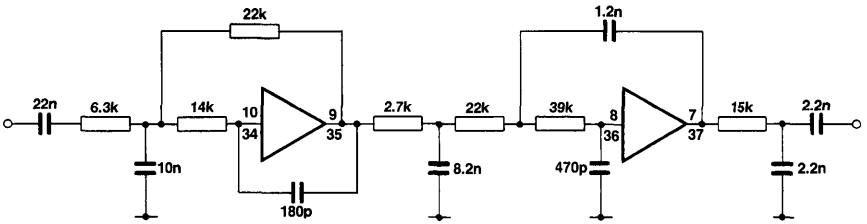
Fig.6(c)

NB. These equations are for 2nd order Butterworth LP filters.

The actual component values used in this application and a plot of the frequency response are illustrated in Fig.7.

The filters provide an adjacent channel rejection of 70dB at 25kHz separation with a 250Hz square wave modulated signal at 4.5kHz deviation.

It is possible to obtain similar performance at 12.5kHz separation with 2kHz deviation if all capacitance values shown above are doubled.



NB: ALL CAPACITOR VALUES ARE ±5% EXCEPT COUPLING CAPACITORS

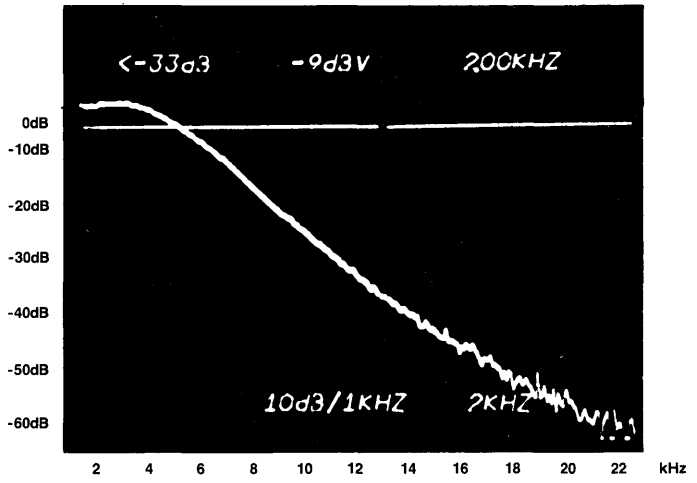


Fig.7 Active filter component values and frequency response for SL6637 DC pager

Limiting Amplifiers and Phase Discriminator

The limiting amplifiers limit with inputs of about 6μV on pins 6 and 42. Pins 4,5 and 43 are bypassed to ground by 10μF capacitors.

The outputs of the limiting amplifiers go directly to the phase discriminator and are not accessible externally. The discriminator output is at pin 1.

Bit-Rate Filter and Decoder

This is a unity gain buffer followed by a limiting amplifier. The buffer may be configured as an active filter if desired; however, the connection of a 1nF capacitor from pin 2 to ground is adequate as a LPF to the modulation frequency.

A 220kΩ resistor is connected between pin 1 and pin 2 to suppress feedback. The data output is available at pin 44.

Inverter Circuit

This inverter is used to provide Vcc2 which is 2.3V from a single supply Vcc1 which is 1.3V.

The inverter control output on pin 18 is derived from the ratio of the internal reference to the Vcc2 line and moves in phase with changes in the Vcc2 line. Pin 21 allows the value of Vcc2 to be adjusted.

Pin 13 is a battery flag which is activated when Vcc1 falls below about 1V. The inverter circuit is shown in Fig.8.

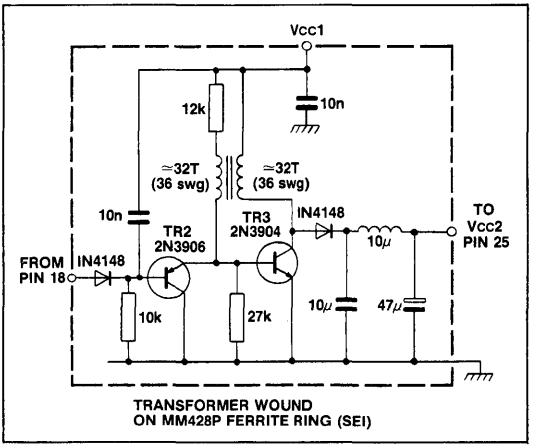


Fig.8 Inverter circuit for SL6637 pager

Beeper Drive

This stage accepts an input from an external source and provides a high current drive to the beeper. This current drive can be as high as 200mA and the arrangement is such that the output waveform may be modified when the battery is low. This modified waveform is generated externally and applied to pin 28. When the battery is low pin 28 will override the beep input on pin 31. A logic high will remove beep drive and a logic low will connect beep drive.

The internal band-vap reference is 1.2V and this is divided down to a suitable voltage.

An internal diode connects pin 29 to pin 30 to protect the driver transistor when used with inductive loads.

Battery Economy

The following functions will have their bias removed during power down (high on pin 24):

RF amplifier
Oscillator current sources
Mixers
Active filters
Phase discriminator
Bit-rate filter and decoder

RECEIVER PERFORMANCE

The performance of the pager circuit is measured using a quasi bit-error detector which is illustrated schematically in Fig.9. Errors on the +ve or -ve half cycles of the recovered data (depending on the setting of SW1) are examined.

A reading of 8Hz on the frequency counter corresponds to a bit-error rate (b.e.r.) of 1 in 30. The sensitivity at a b.e.r. of 1 in 30 with a square wave modulated signal and a deviation of 4.5kHz is 200nV.

Graphs of b.e.r./input level and errors/sec./input level for various offsets from nominal LO frequency are shown in Figs. 10 and 11.

Adjacent channel rejection = 70dB (for 6dB degradation at 25kHz separation)
Co-channel rejection = 1dB (wanted signal 6dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 0dB (wanted signal 12dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 0dB (wanted signal 20dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 1dB (wanted signal 30dB above level for 1 in 30 b.e.r.)
3rd order input intercept = -6.5dBm

The above measurements are all made using a wanted signal of 153MHz modulated by a 250Hz square wave at a deviation of ±4.5kHz

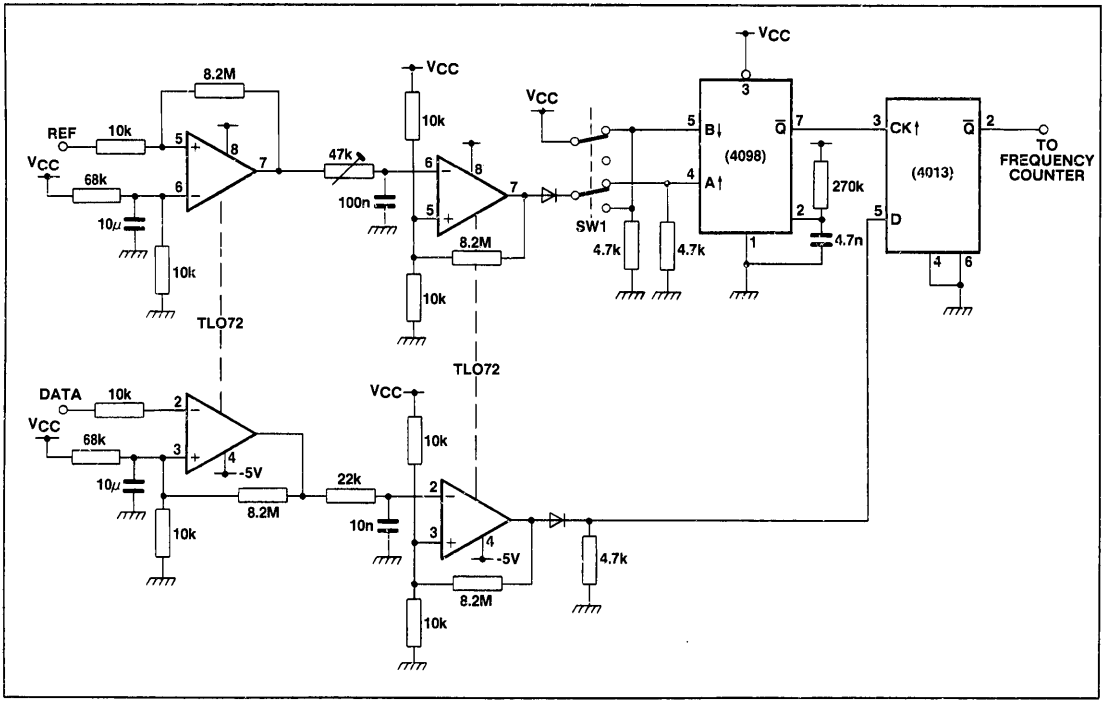


Fig.9 Simple circuit for quasi bit-error detector

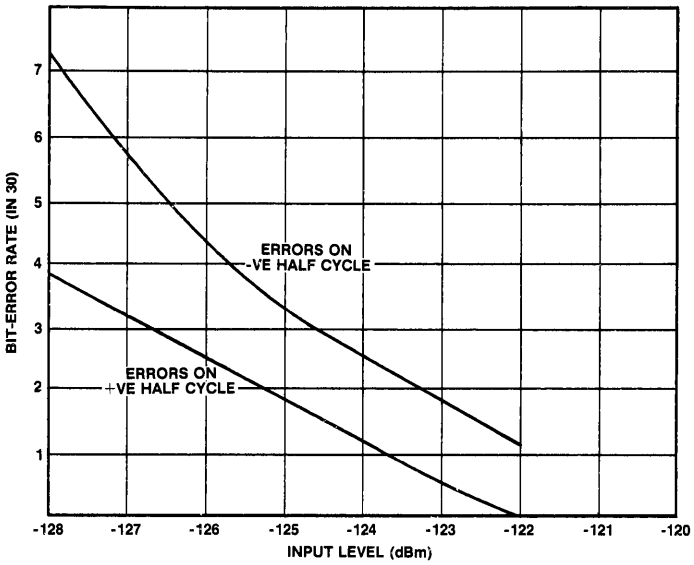


Fig.10 Bit-error rate/input level for SL6637 DC pager

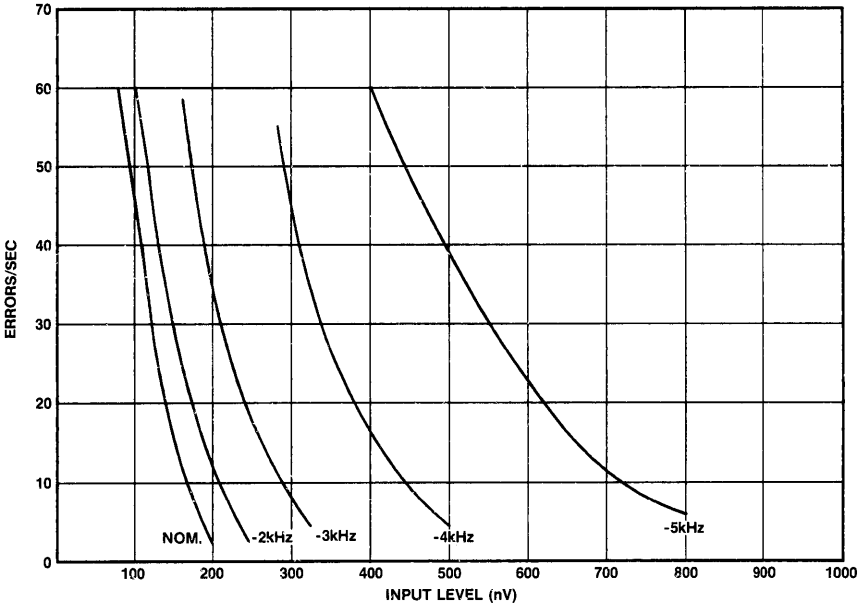


Fig.11 Errors/Sec./input level for various offsets from LO frequency

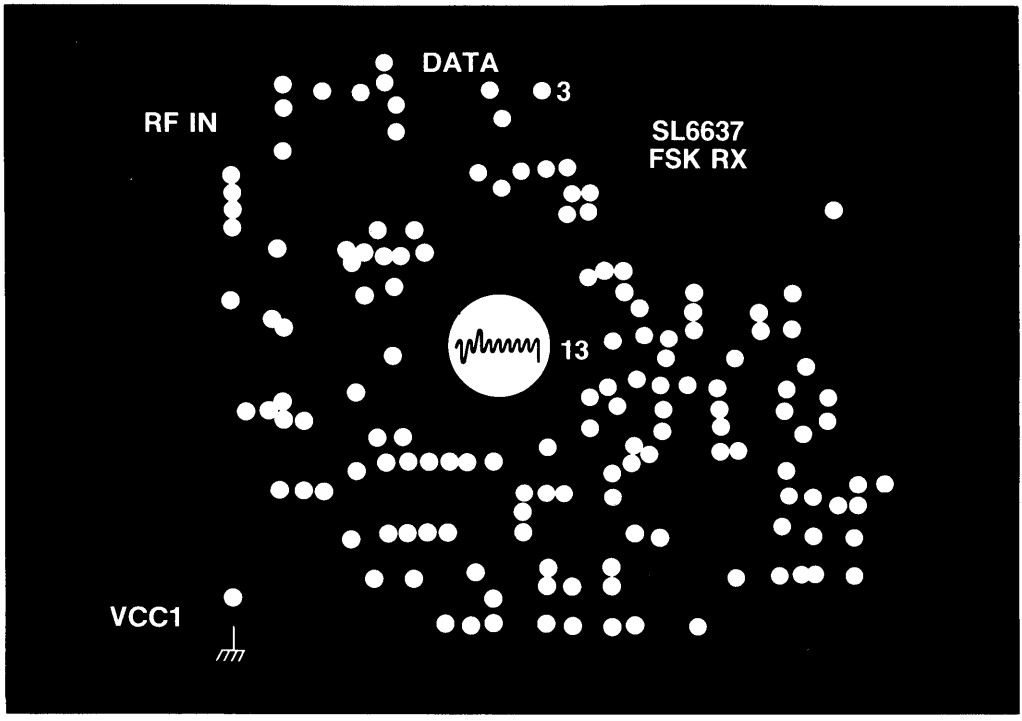


Fig.12 SL6637 demonstration board - ground plane

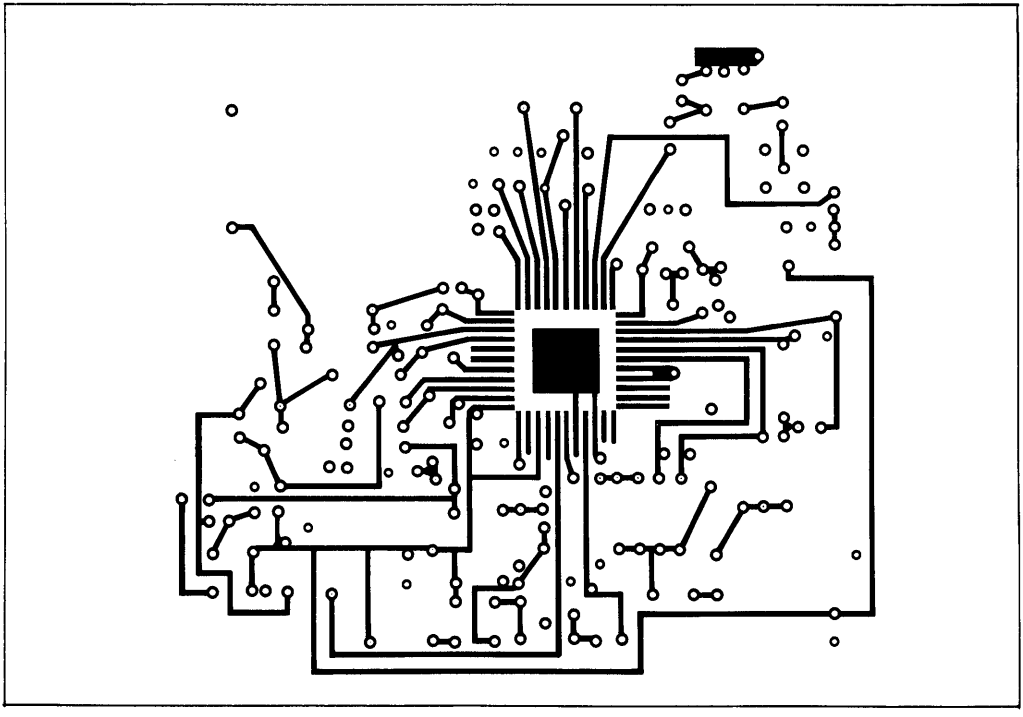


Fig.13 SL6637 demonstration board - track side

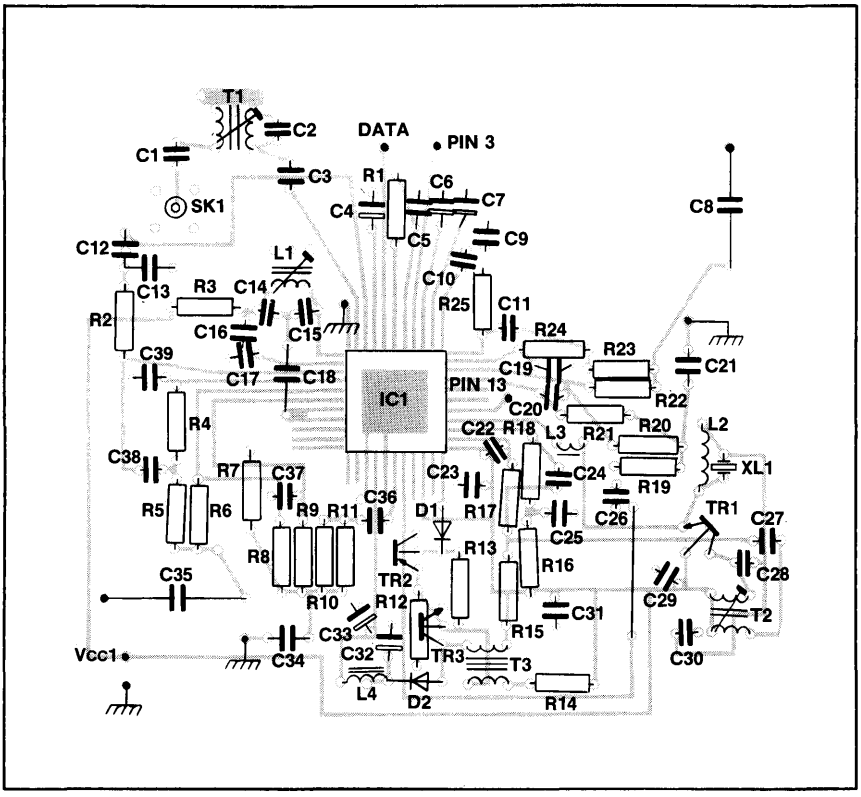


Fig.14 SL6637 demonstration board component layout

NOTE: C40 is connected between pin 19 and Vcc1, C41 is connected between the base of TR2 and Vcc1

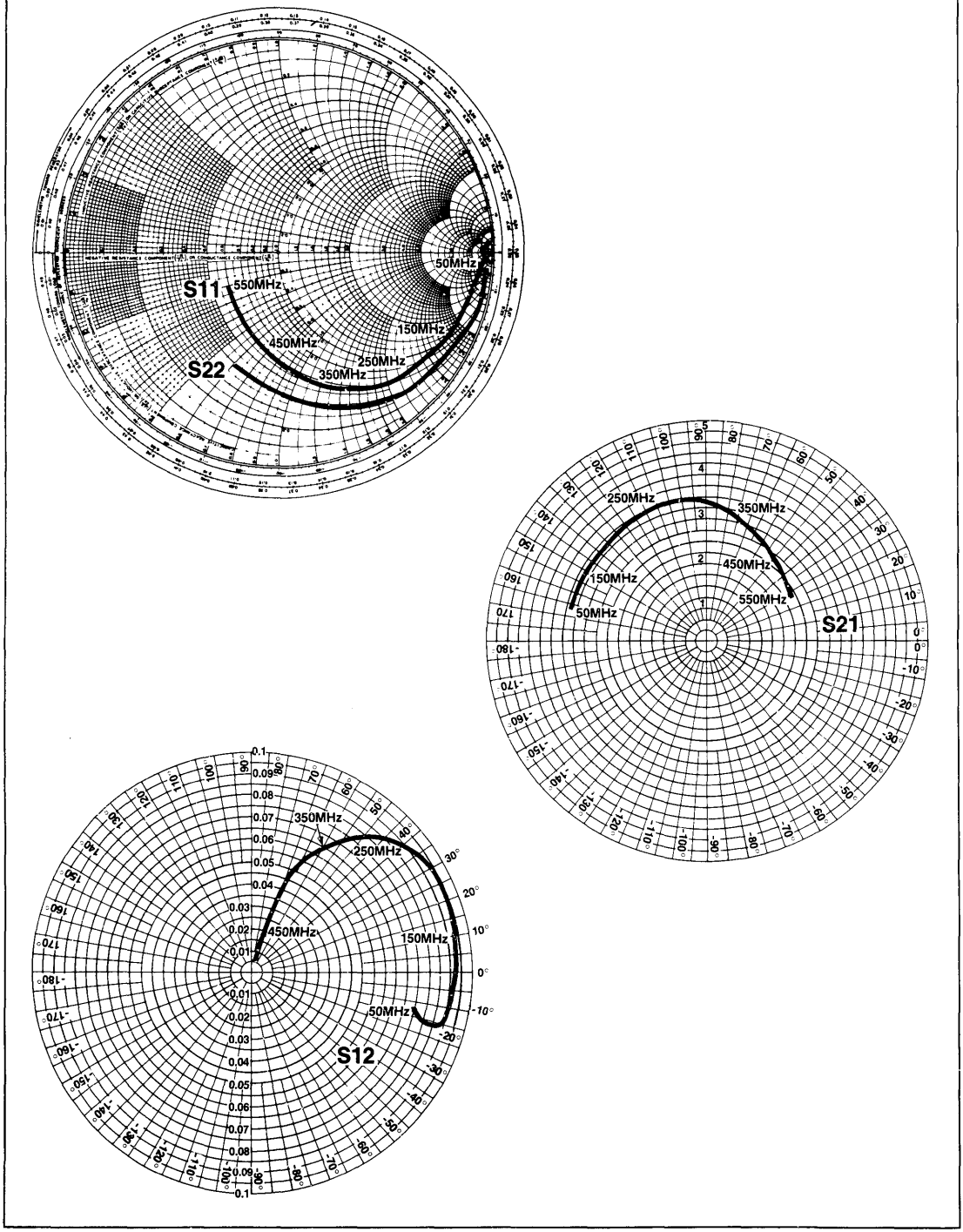


Fig.15 'S' parameters for the RF amplifier of the SL6637

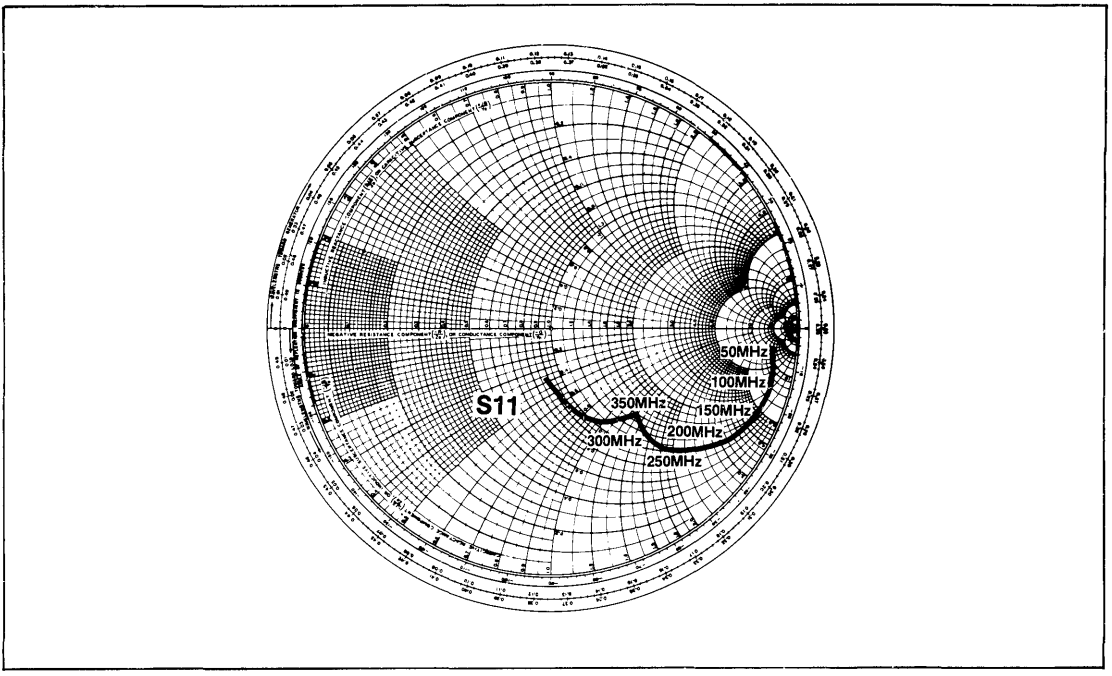


Fig.16 S_{11} for the mixer of the SL6637

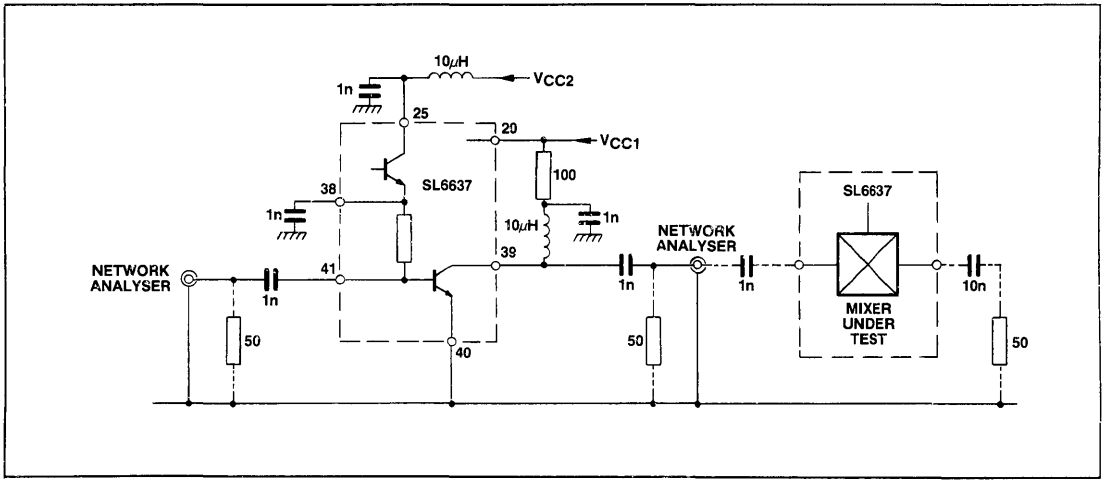


Fig.17 S-parameter test fixture

The care and feeding of High Speed Dividers

Circuit design and layout for high speed dividers operating at frequencies up to 2GHz owe much more to analog RF design techniques than normal digital ones and the limitations on flexibility and component choice inherent in UHF RF design are of paramount importance in successful designs.

PRACTICAL DESIGN CONSIDERATIONS

High speed divider applications require the printed circuit boards to be mechanically designed with two considerations in mind:

(1) Electrical performance
(2) Mechanical and thermal performance.

These two considerations are inter-related; for example, the use of 1/16 inch thick fibreglass PC board may be desirable mechanically, but a 50Ω stripline on this thickness of board is about 5/32 inch wide, and is thus too wide to pass between the pins of an IC.

Most of the heat conducted from a dual-in-line IC package is removed from the bottom of the package. Less than 10% is conducted out by the leads, and because of the cavity between the chip and lid, relatively little through the top of the package.

For this reason, the use of a double-layer PC board layout is recommended, with a ground plane top surface. Where 1/32 inch thick material is used, a top surface ground plane will add substantially to the heat dissipation capabilities of the board.

For use at very high frequencies, consideration must be given to the type of component used. Carbon composition resistors are more nearly resistive at high frequencies than either carbon or metal film types, and are available in very small sizes. Bypass capacitors need to be chosen carefully if they are to act as low impedances, as series inductance leads to an increasing impedance with frequency above the series resonant frequency of the device. As a guide, a 1000pF disc ceramic capacitor with 1/4 inch leads will be self resonant at about 75MHz, and will appear as an inductive impedance of about 22Ω at 800MHz. The use of chip capacitors is recommended above 500MHz, although leaded monolithic ceramic capacitors with suitably short leads are often acceptable.

The use of a ground plane for RF decoupling purposes is often recommended, and can be helpful. However, the danger is that the ground current paths in the plane are not defined very well, and because of this lack of definition, the ground plane can cause unsatisfactory operation. Probably the best method is to return all the bypass capacitors to a single point (as in Fig.1) and return this point to the ground plane.

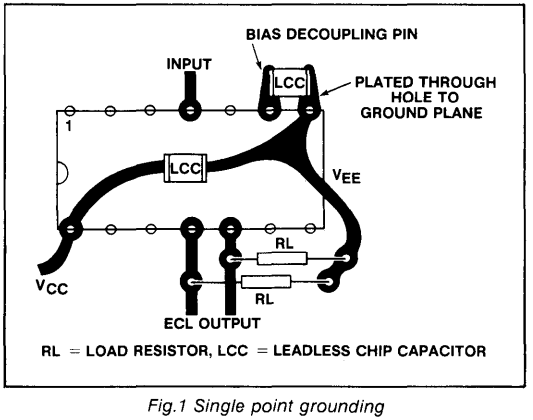


Fig.1 Single point grounding

Also note that in Fig.1 the output load resistors have their grounded ends connected together and a common return used. Because the currents in the resistors are in antiphase, cancellation of the inductive effects taken place, and the path followed by the relatively large output currents is controlled. Defining the ground current path is more important in applications like frequency synthesis, where a relatively large part of the system may be on one PCB.

It is well known that the effect of mismatching a transmission line is to cause variations in the voltage along the line. Standard practice at Plessey Semiconductors has been to use a 5:1 attenuator manufactured from 'microdot' resistors as an attenuator feeding a 50Ω sampling oscilloscope or a power meter. Although a high VSWR will exist on the line from the generator to the test fixture, the theory is that the line from the power meter to the attenuator will be a matched line, and so the power measured is 14dB lower than the power at the device input pin. This method has been proved very successful, even if simple, and offers some advantages over the use of hybrids or directional couplers.

The use of a matched 50Ω system can help, and using microstrip techniques, a track with a defined impedance is reasonably practical. The impedance of a microstrip line is given by:

$$Z_O = 377\ (L/w)\ (1/\varepsilon_r)$$

Where L = dielectric thickness, w = width of track and ε_r is the relative permeability of the board material.

Some correction factors have to be applied, and typically, on 1/16 inch glass fibre epoxy board, the following sizes provide a guide to track width

100Ω - 1mm
75Ω - 2mm
50Ω - 4mm

These impedances rely on the ground plane on the obverse of the board being complete, and where boards are wave soldered, it may be necessary to make arrangements to prevent blistering.

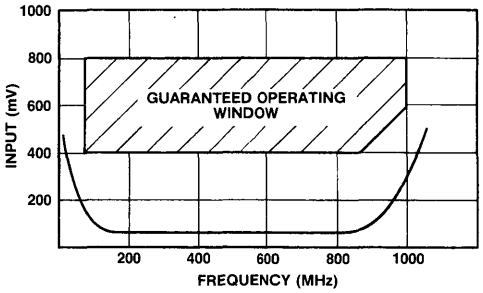


Fig.2 Example of input sensitivity curves

The input level of a divider should be maintained within the guaranteed operating window shown on its data sheet (Fig.2). Excessive input can vary in its effects, from causing permanent damage to miscounting, especially when cold. Running the device at too low a level can cause problems, even though the level is within the 'typical' performance line of the device. An ECL output signal on pin 6 of the device in

Fig.3 can couple 60mV of signal to the input shown on Fig.2 at 500MHz. Such a level of coupling can lead to divider jitter if the input signal is low, and it becomes very necessary to keep the inputs and outputs well separated at the higher frequencies. This includes ECL lines to modulus control pins on two modulus dividers.

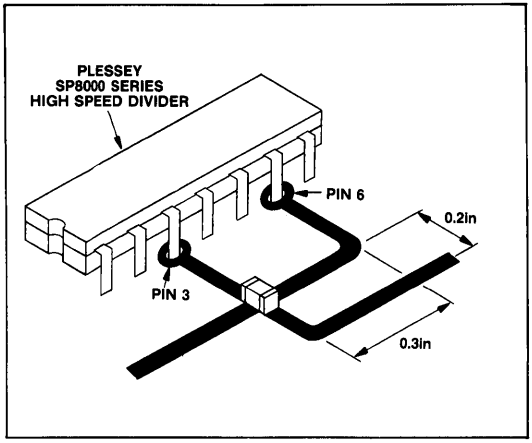


Fig.3 Coupling between parallel tracks

Most dividers are edge triggered, and although they are specified over a frequency range with sine wave input, they will operate to lower frequencies provided a suitably high slew rate is provided on the input signal. This is generally of the order of 100 to 200 volts/microsecond. This should be achieved by shaping of the input signal, for example by limiting, rather than by overdriving the device.

The outputs of devices may be of the following forms:

(1) ECL
(2) Open collector TTL
(3) TTL
(4) CMOS

Of these, the ECL output is well defined; some devices require external load resistors and the data sheet should be consulted. Where these external resistors are required, suitable interconnection techniques should be used between them and the device; the resistors should be carefully chosen for their non-inductive properties when output frequencies are very high. Where an ECL output divider drives another divider it is best to AC couple, since few dividers are strictly ECL-compatible on their inputs.

Open collector TTL outputs are relatively slow. Although the negative edge is limited in speed by the turn-on time of the output transistor, the rising edge is limited by the external load resistor and capacitance to ground. In practice this means that short narrow tracks are required to the following device, and a minimum 'fan-in' load provided. In addition, open collector TTL should not be used above about 10MHz output frequency.

True TTL outputs are not so limited, because of the active pull-up. Nevertheless, the use of such outputs at frequencies above about 25-30MHz is not recommended, especially into capactive loads. Loads of more than 30pF should not be driven faster than about 15MHz. Note that the current drawn by true TTL outputs increases with increasing load capacitance.

CMOS outputs are, on the face of it, TTL-compatible. However, investigation will show that the outputs are not guaranteed to meet TTL levels at TTL currents and it is not recommended that CMOS output devices be used to directly drive TTL. Where an interface of this sort is required, an active transistor interface should be used.

Fig.4 shows a circuit for an ECL-TTL interface, using a line receiver. Simple circuits using one or two transistors cannot be guaranteed to work over all the tolerances of ECL output voltages and temperature ranges.

Interfacing to dividers is not difficult if a few simple rules are obeyed. These are:

(1) Observe the input requirements - guaranteed input operating area, and slew rate.
(2) Do not use open collector outputs above 10MHz.
(3) Do not use CMOS outputs to drive TTL.
(4) Use a sensible layout with good components, and sensible values - 0.1 microfarad ceramic capacitors are NOT bypasses at 1.5GHz.

Treating dividers as RF linear devices is probably the best way to ensure successful applications at high frequencies. There is no magic in HF design, only intelligent layout and sensible component choice.

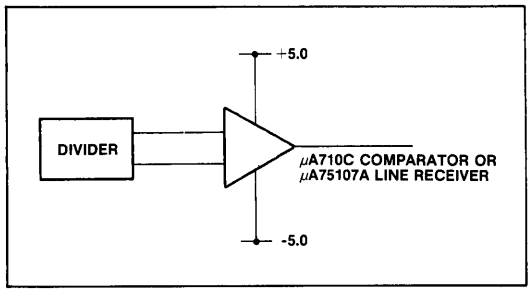


Fig.4 ECL/TTL interface

Impedance Matching

The use of microstrip techniques has been mentioned already. However, in itself this will not produce a matched network and various possibilities exist to improve the matching at the input of a device. These include Tchebycheff impedance transforming networks, narrow band 'L' matching networks, and at high enough frequencies, the use of transmission lines. Wideband matching is often difficult, and attempts should be made to use networks that have the lowest possible working Q. This is for two reasons: firstly a high Q network will not only be narrow band, but will have the capability of increasing the losses, and secondly, a low Q network is generally more tolerant of component variations.

The greater losses in high Q circuits occur because of the greater circulating current: the loss power is I^2R, so that if the Q is doubled with all else constant, the power loss is increased by 4 times.

The easiest method of determining matching components is by means of the Smith Chart.

THE SMITH CHART

The input impedance of SP8000-series high speed dividers varies as a function of frequency and is therefore specified on the datasheets by means of Smith Charts. The following information is included in this handbook as a guide to their interpretation and use.

Construction of the chart

The chart is constructed with two sets of circles, one set comprising circles of CONSTANT RESISTANCE (Fig. 5) and the other circles of CONSTANT REACTANCE (Fig. 6). The values on these circles are normalised to the characteristic impedances of the system by dividing the actual value of resistance or reactance by the characteristic impedance e.g. in a 50Ω system, a resistance of 100Ω is normalised to a value of 2.0.

By combining Figs. 5 and 6 to form Fig. 7, a chart is produced in which any normalised impedance has a unique position on the chart, and the variation of this impedance with frequency or other parameters may be plotted.

A further series of circles may be plotted on the chart: these are circles of constant VSWR, and represent the degree of mismatch in a system. The VSWR is the ratio of the device impedance to the characteristic impedance, and is always expressed as a ratio greater than 1: thus a 25Ω device in a 50Ω system gives rise to a 2:1 VSWR. These circles of constant VSWR have been added in Fig. 7.

Any point can be represented on the Smith Chart: for example an impedance of 150-j75Ω can be represented by a normalised impedance (in a 50 Ω system) of 3-j1.5 and this point is plotted in Fig. 7 as point A.

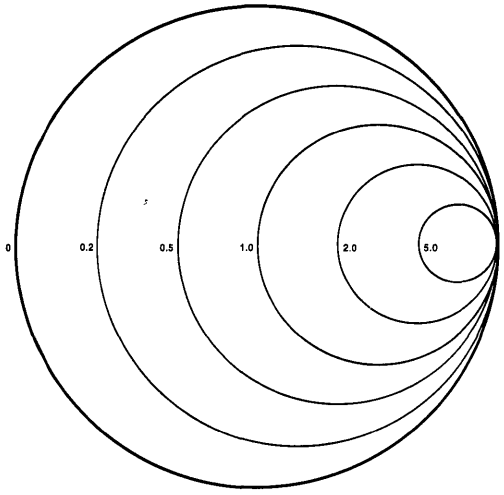


Fig.5 Constant resistance circles

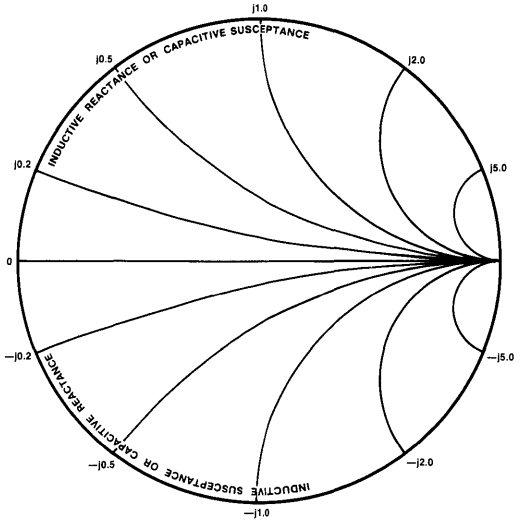


Fig.6 Constant reactance circles

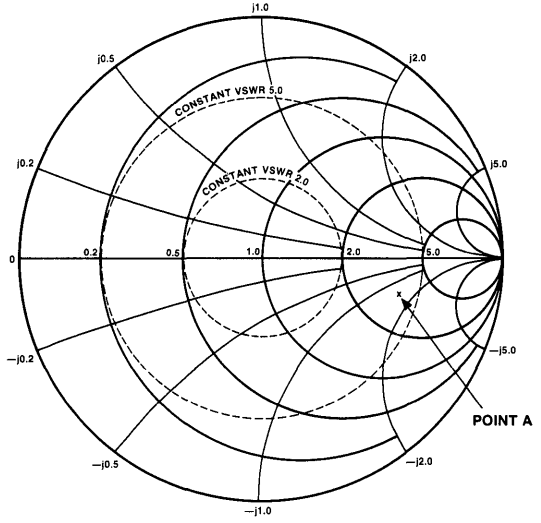


Fig.7 The complete chart

Network calculations

The main application for Smith Charts with integrated circuits is in the design of matching networks. Although these can be calculated by use of the series to parallel (and vice-versa) transforms, followed by the application of Kirchoff's Laws, the method can be laborious. Although the Smith Chart as a graphical method cannot necessarily compete in terms of overall accuracy, it is nevertheless more than adequate for the majority of problems, especially when the errors inherent in practical components are taken into account.

Any impedance can be represented at a fixed frequency by a shunt conductance and susceptance (impedances as series reactance and resistance in this context). By transferring a point on the Smith Chart to a point at the same diameter but 180° away, this transformation is automatically made (see Fig. 8) where A and B are the series and parallel equivalents.

It is often easier to change a series RC network to its equivalent parallel network for calculation purposes. This is because as a parallel network of admittances, a shunt admittance can be directly added, rather than the tortuous calculations necessary if the series form is used. Similar arguments apply to parallel networks, so in general it is best to deal with admittances for shunt components and reactances for series components.

Admittances and impedances can be easily added on the Smith Chart (see Fig. 9). Where a series inductance is to be added to an admittance (i.e. parallel R and C), the admittance should be turned into a series impedance by the method outlined above and in Fig. 8. The series inductance can then be added as in Fig. 9 (see also Fig. 10).

Point A is the starting admittance consisting of a shunt capacitance and resistance. The equivalent capacitive impedance is shown at point B. The addition of a series inductor moves the impedance to point C. The value of this inductor is defined by the length of the arc BC, and in Fig. 10 is $-j0.5$ to $j0.43$ i.e. a total of $j0.93$. This reactance must of course be denormalised before evaluation. Point C represents an inductive impedance which is equivalent to the admittance shown at Point D. The addition of shunt reactance moves the input admittance to the centre of the chart, and has a value of $-j2.0$. Point D should be chosen such that it lies on unity impedance/conductance circle: thus a locus of points for point C exists.

This procedure allows for design of the matching at any one frequency. Wide band matching is more difficult and other techniques are needed. Of these, one of the most powerful is to absorb the reactance into a low pass filter form of ladder network: if the values are suitably chosen, the resulting input impedance is dependent upon the reflection coefficient of the filter.

At frequencies above about 400MHz, it becomes practical to use sections of transmission line to provide the necessary reactances, and reference to one of the standard works on the subject is recommended.

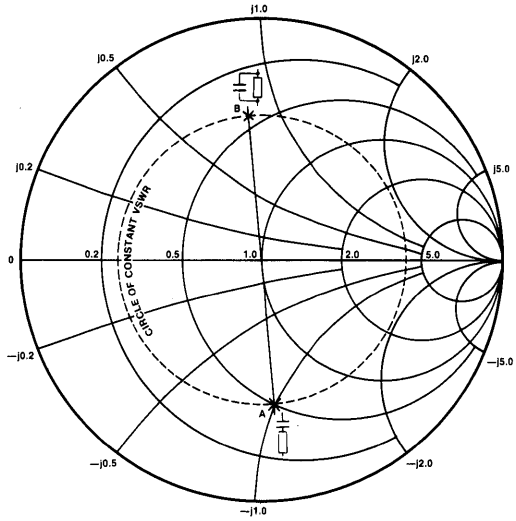


Fig.8 Series reactance to parallel admittance conversion

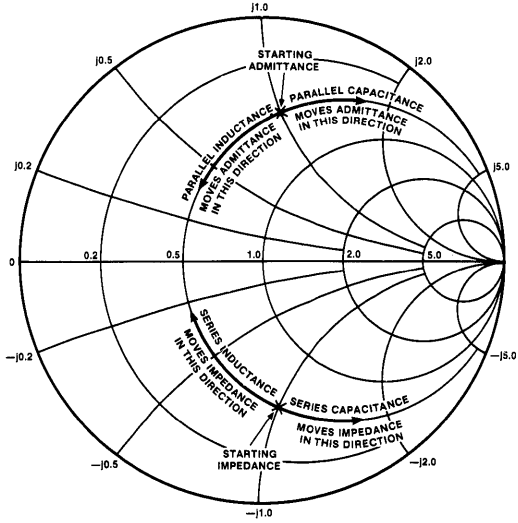


Fig.9 Effects of series and shunt reactance

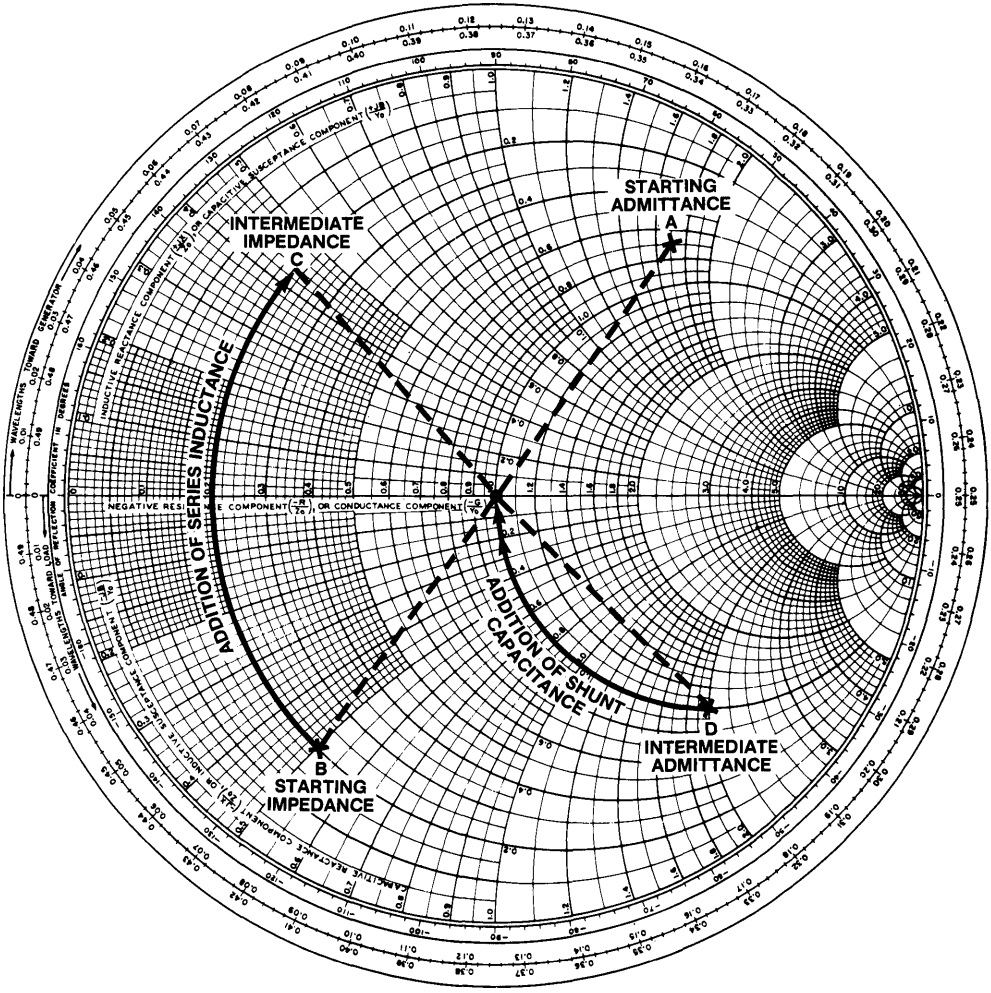


Fig.10 Matching design using the Smith Chart

PHASE NOISE AND DIVIDERS

Phase noise is becoming increasingly important in systems and it is necessary to minimise its effects. First, however, phase noise must be defined.

A spectrally pure signal of a given frequency would appear on a perfect spectrum analyser display as a single straight line as in Fig.11. If the signal is frequency modulated with a discrete modulation frequency, the result will be a comb of frequencies as in Fig.12, while modulation with noise will produce an output spectrum as in Fig.13. Note that the noise density decreases as the offset from the carrier increases. This effect is the result of the effectively lower modulation index *m*. In the case of a Voltage Controlled Oscillator modulated by white noise, a similar effect will be seen, because for a given deviation *f*, the modulation index *m*, (= 1/*fmod*) is greater for lower frequencies than for higher frequencies. Thus the number of sidebands is greater for lower frequencies, and the noise spectral density increases as the carrier is approached.

The causes of phase noise in dividers are not well understood, but the effects of internal noise on the switching point of the various flip-flops cannot be ignored. The 1/*f* noise will obviously inter-relate to the phase noise if this is so, and it is interesting to note that various measurements of Gallium Arsenide dividers suggest performances 20 to 30dB worse than for ECL dividers. Rohde (ref. 4) suggests that TTL and CMOS are much better than ECL, although little work has been published in this field, possibly because of the measurement difficulties.

The non-saturating nature of ECL, the fact that the transistors are designed and processed for high speed rather than low noise, and the smaller signal swings than TTL or CMOS, lead intuitively to the conclusion that ECL should be worse than either of these other two logic families. This appears to be the case, while the high 1/*f* noise knee of Gallium Arsenide devices leads to the high relatively close in phase noise.

Devices with slow output edges, such as open collector TTL output stages may also be expected to be worse, which is again born out in practice.

Minimisation of phase noise requires the use of well-filtered supplies, correct input levels and minimisation of noise in level changing circuitry.

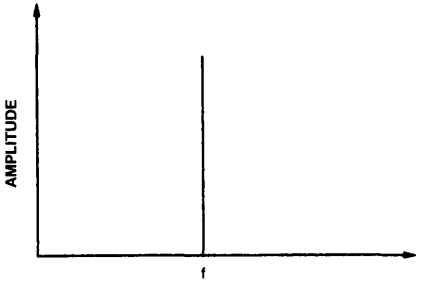


Fig.11 Spectrally pure signal

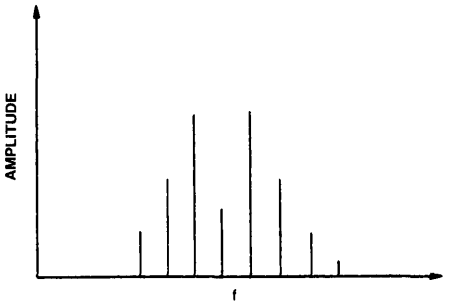


Fig.12 Spectrally pure signal, frequency modulated with single tone

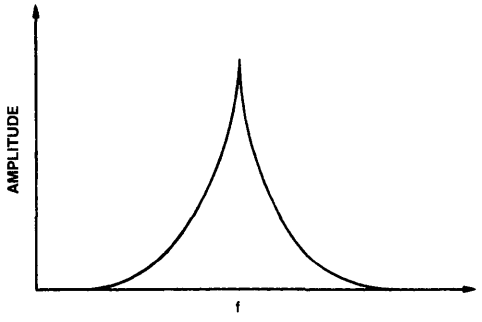


Fig.13 Spectrally pure signal, frequency modulated by noise

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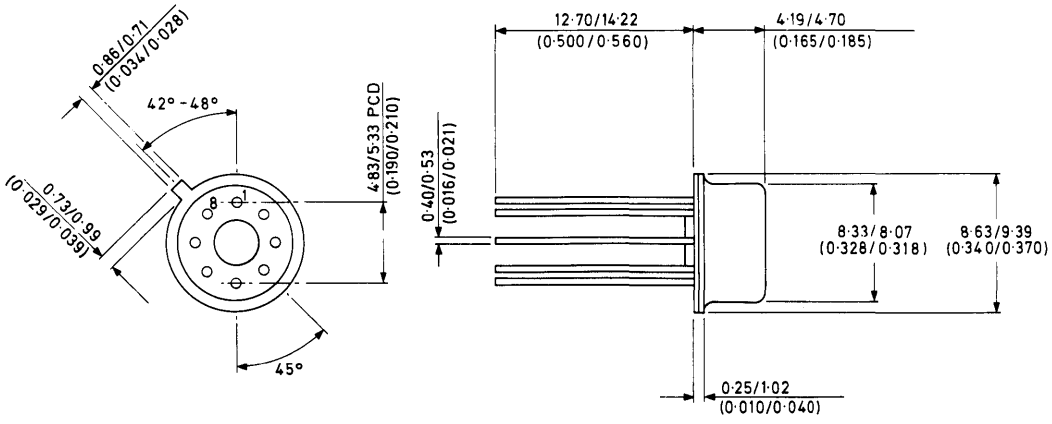
4. Digital PLL Frequency Synthesis Theory and Design V.L. Rohde, Prentice Hall 1983 ISBN 0-13-214239-2.

Package Outlines



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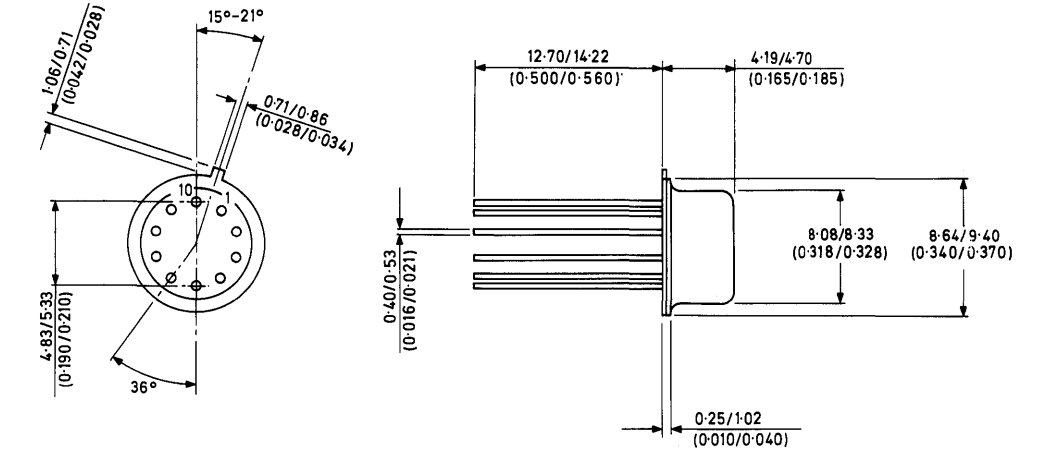

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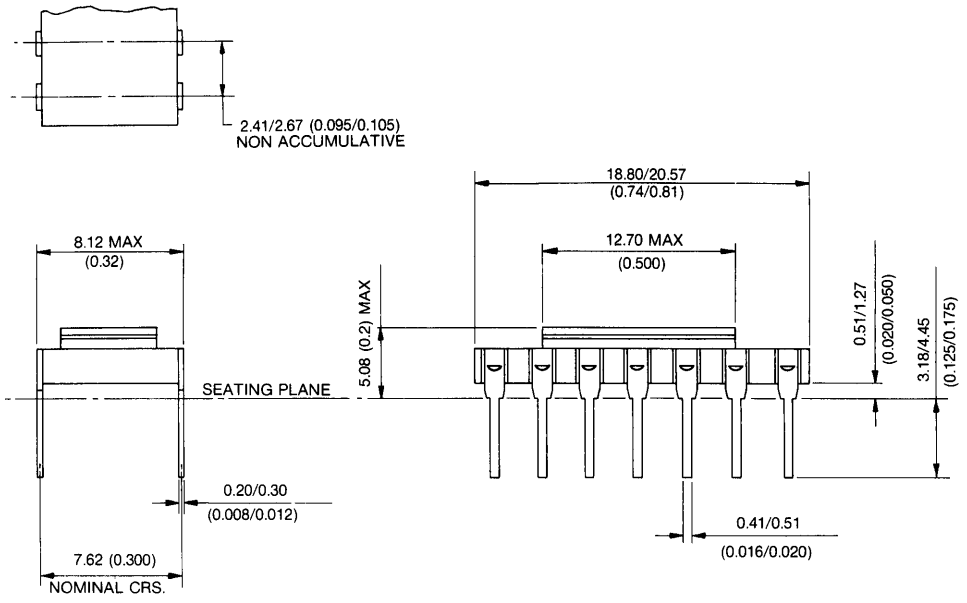

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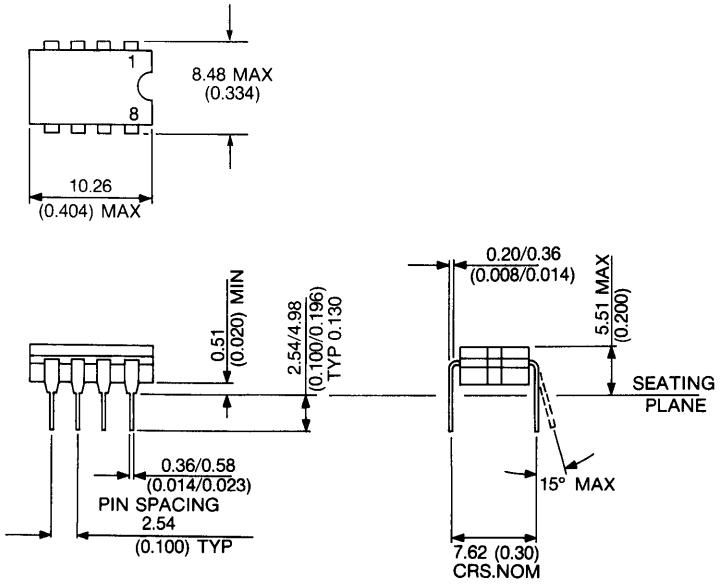

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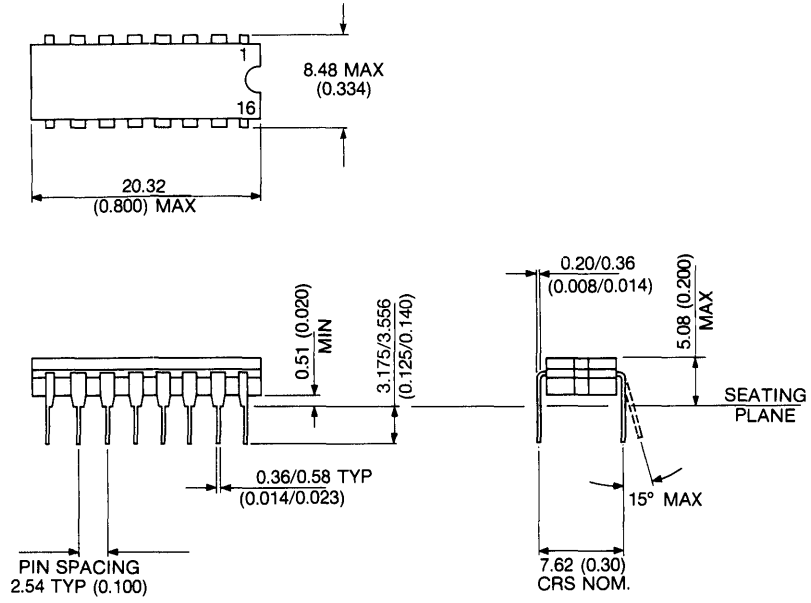
CERDIP - DG8



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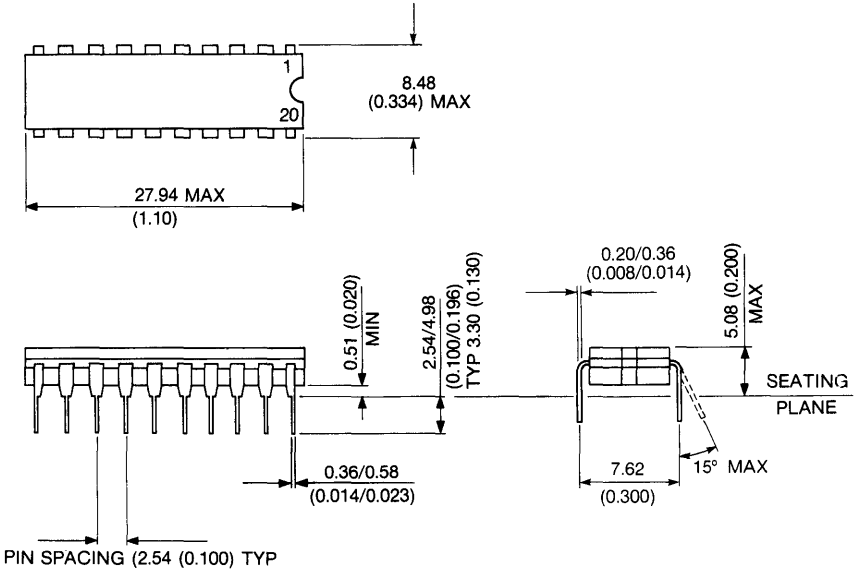

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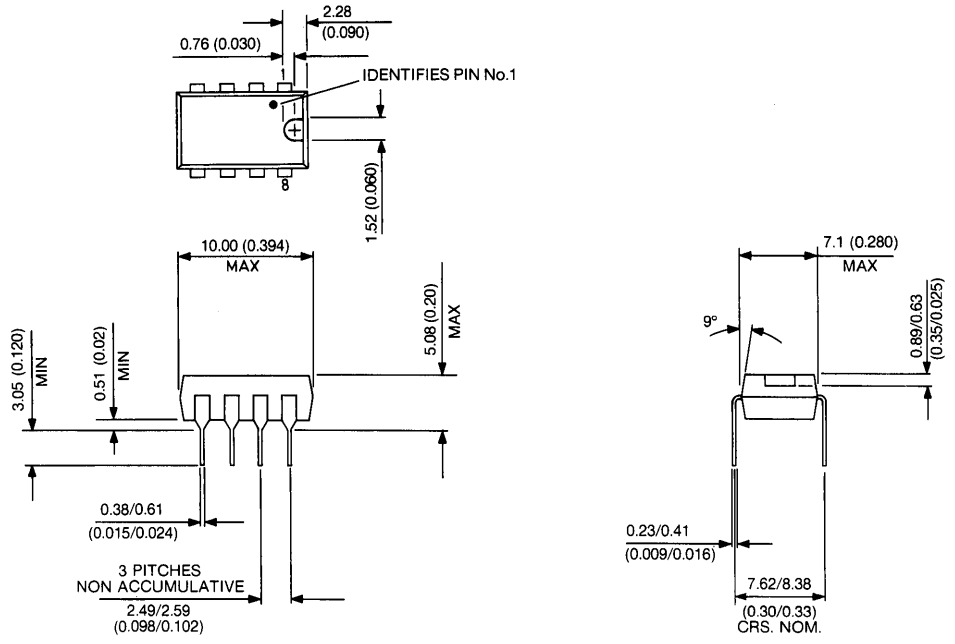

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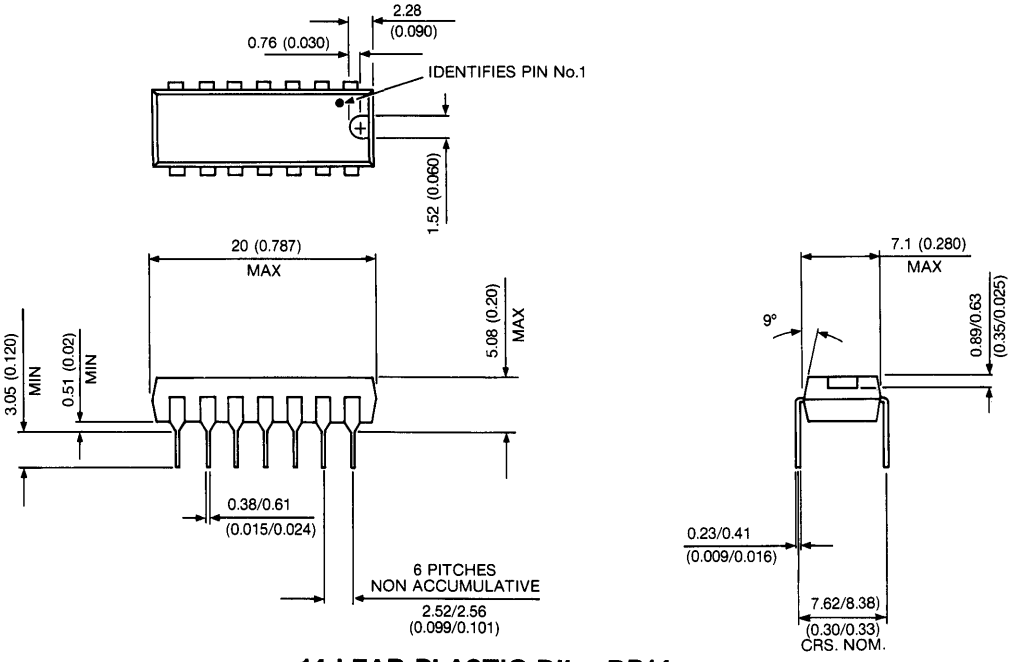

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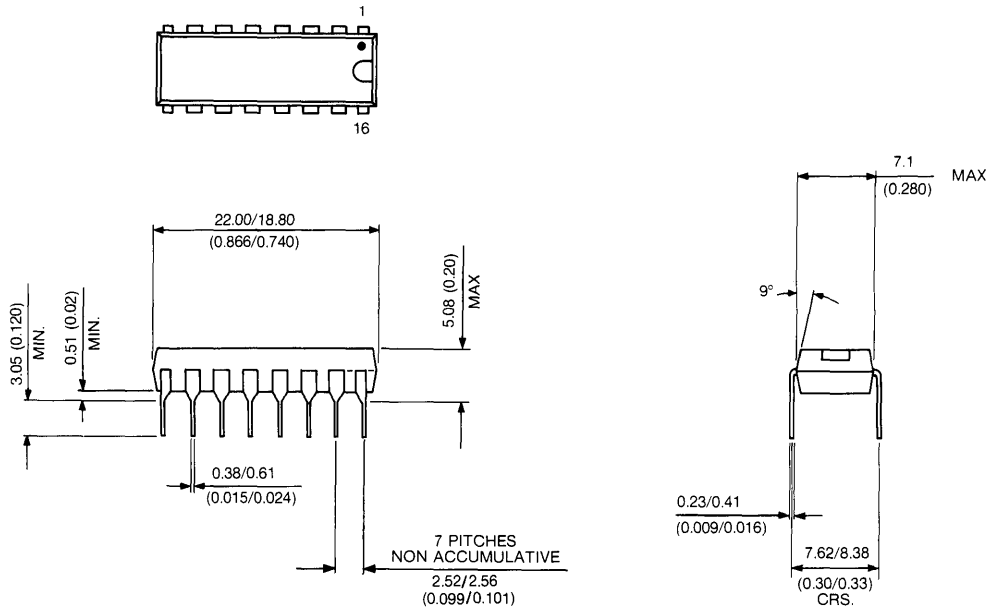

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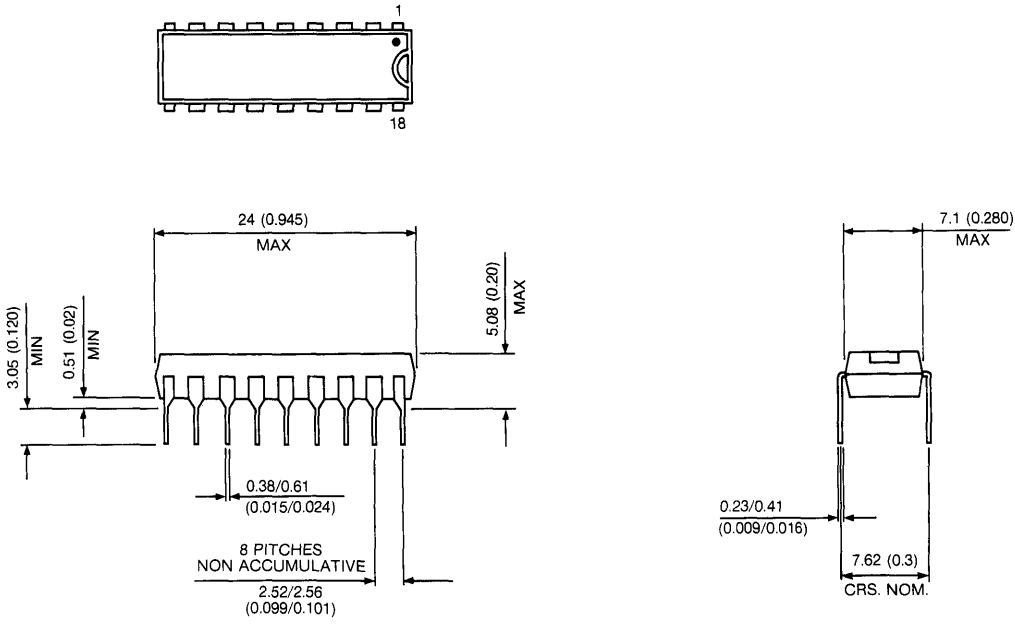

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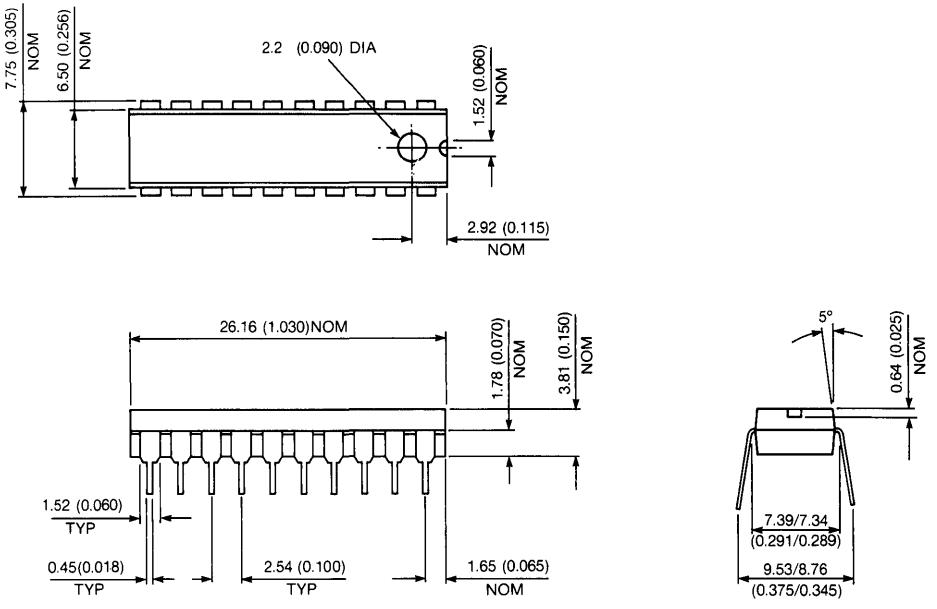

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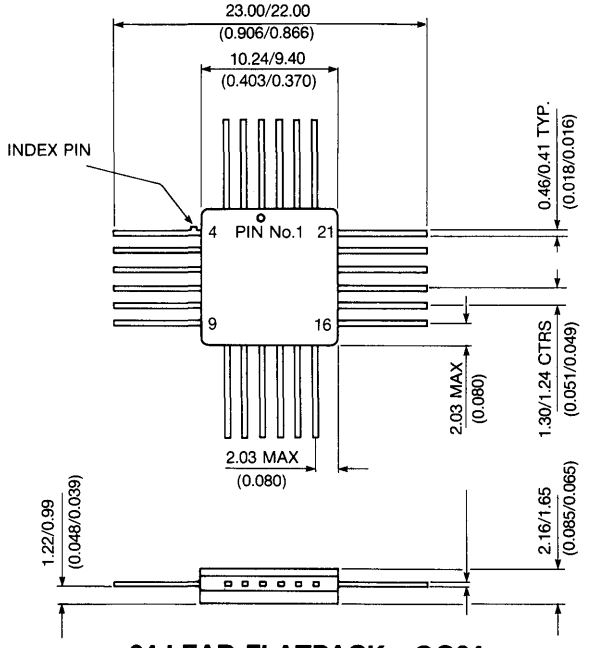

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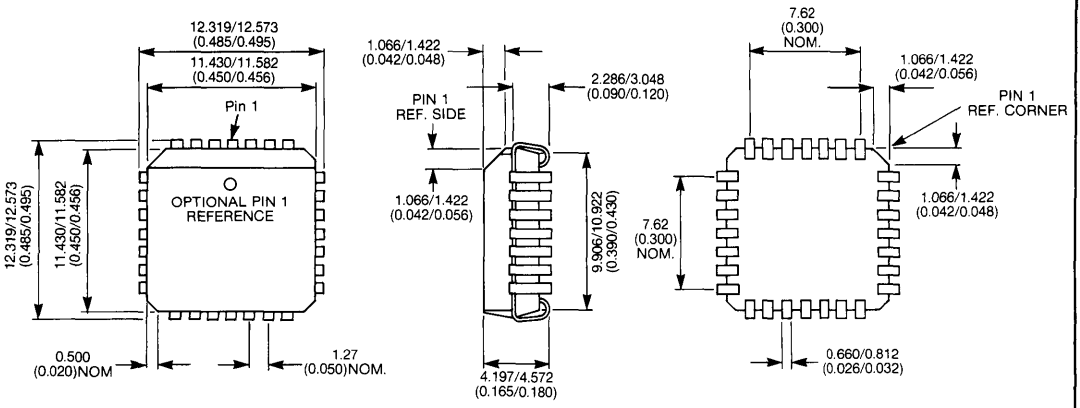

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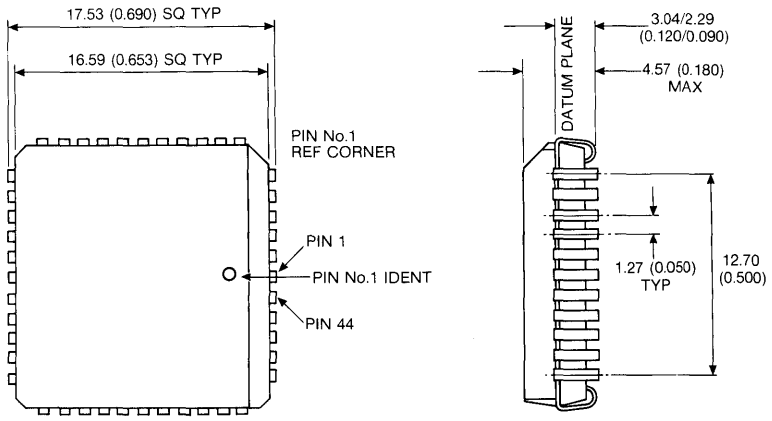

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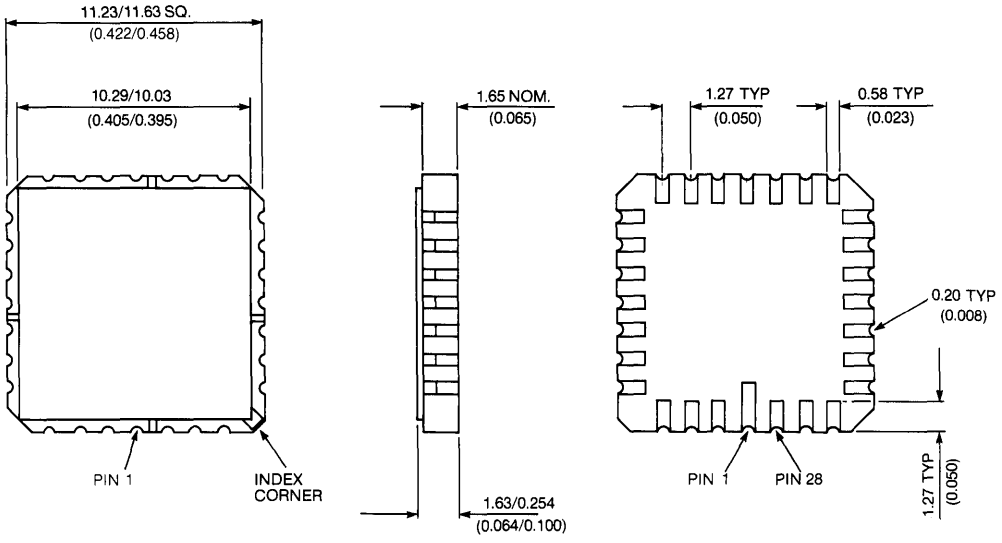

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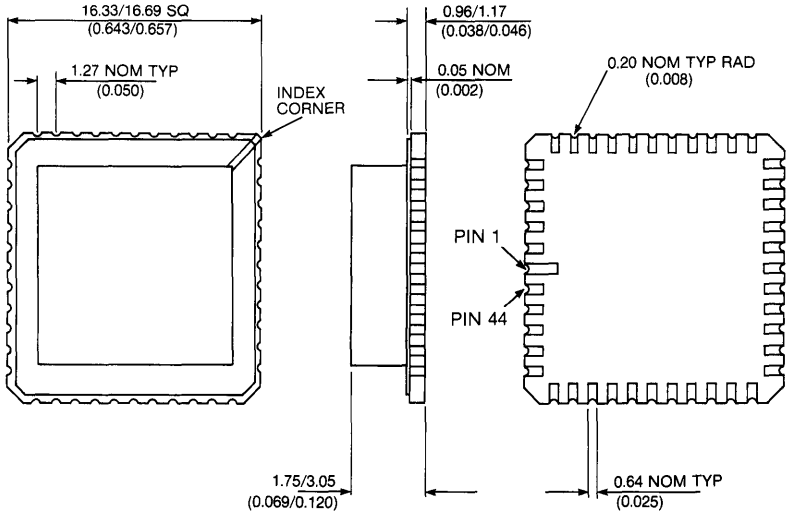

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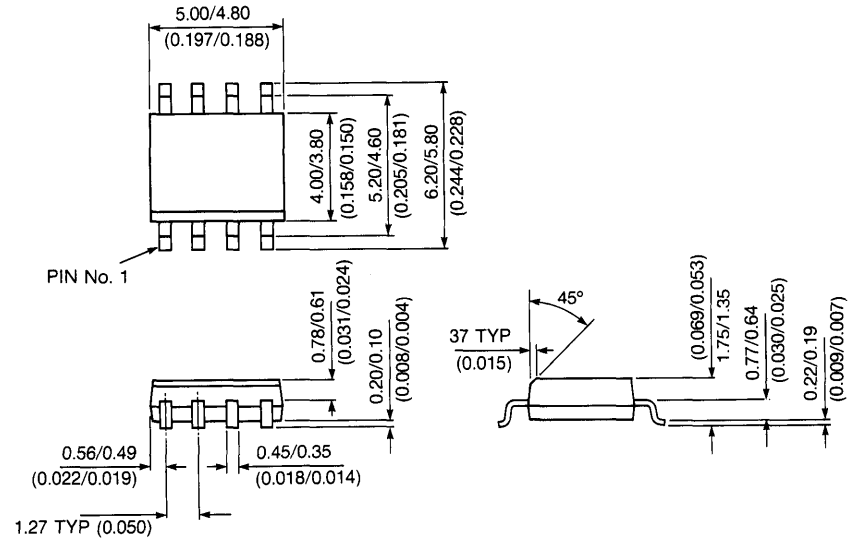

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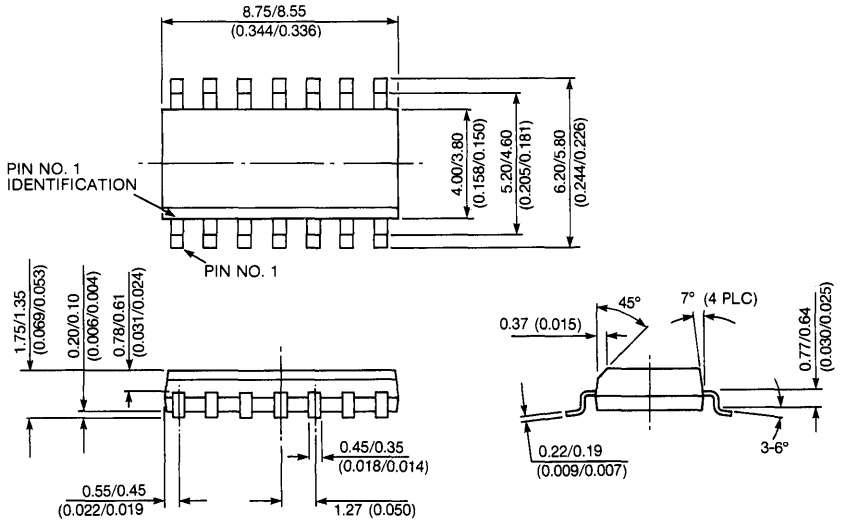

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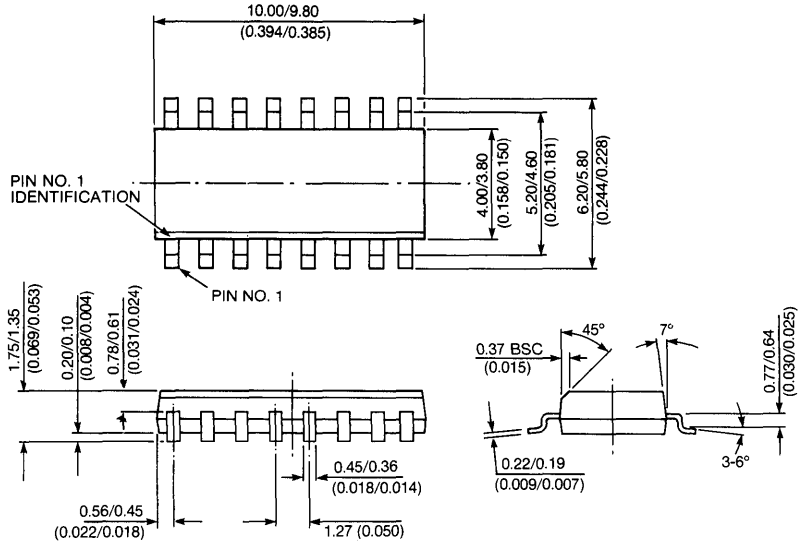

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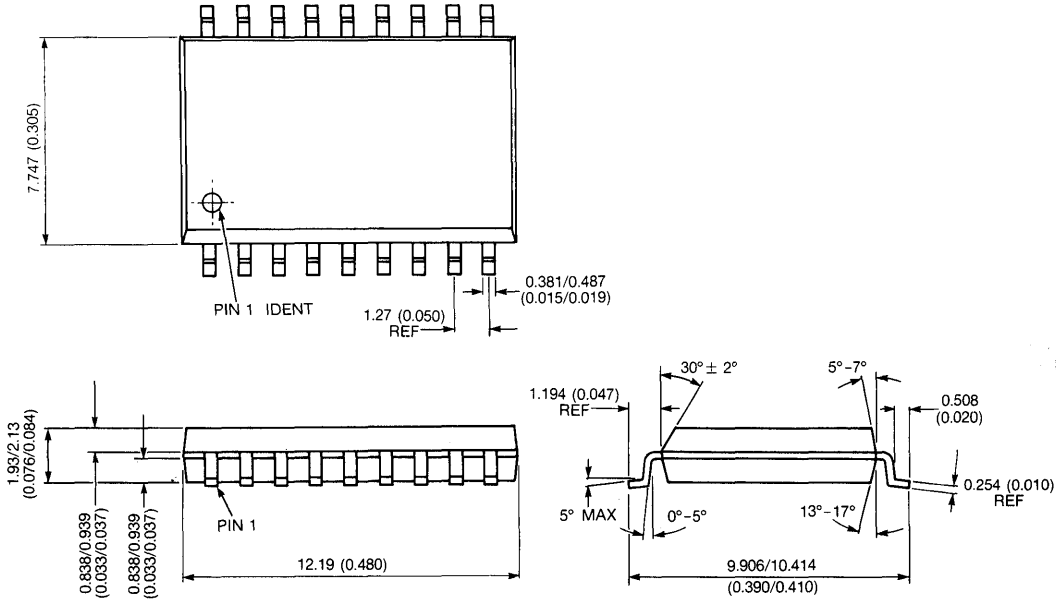

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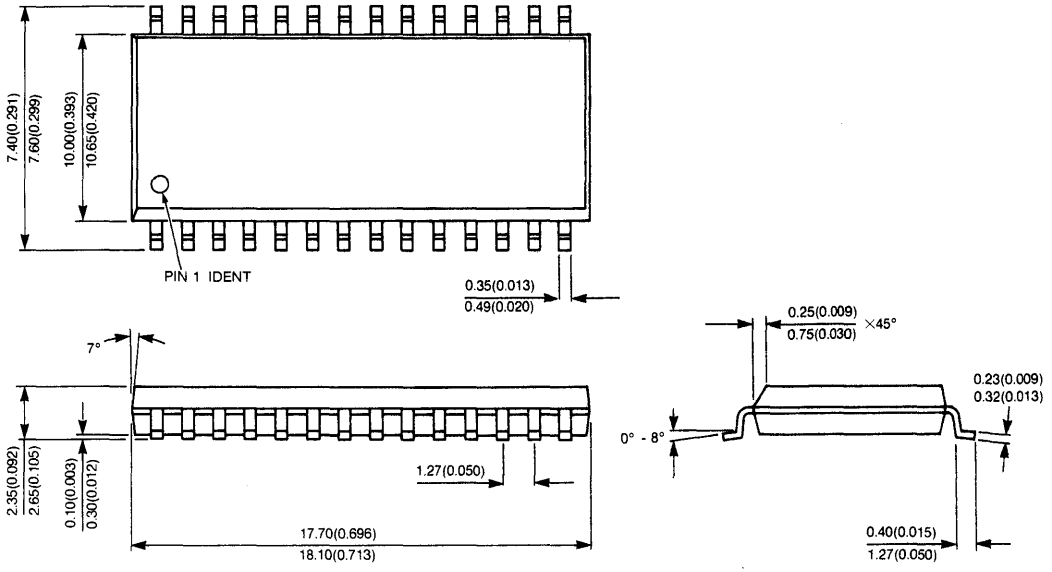

28 LEAD SMALL OUTLINE PLASTIC DIL - MP28

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	Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878/787848 Tx: 847571.
	Gothic Crellon Ltd., P.O.Box 301, Trafalgar House, 28 Paradise Circus, Queensway, Birmingham B1 2BL. Tel: 021 6436365 Tx: 338731.
	Quarndon Electronics Ltd., Slack Lane, Derby DE3 3ED. Tel: 0332 32651 Tx: 37163.
	Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street, Yiewsley, West Drayton, Middlesex UB7 7XB. Tel: 0895 445522 Tx: 21958.
	Unitel Limited, Unitel House, Fishers Green Road, Stevenage, Herts. SG1 2PT. Tel: 0438 312393 (Direct Sales) 0438 314393 (General) Tx: 825637, 826080 Fax: 0438 318711.
WEST GERMANY	**AS Electronic Vertriebs-GmbH**, Elisabethenstrasse 35, 6380 Bad Homburg. Tel: 06172/2 90 28-29 Tx: 410868.
	Astronic GmhH, Winzererstrasse 47D, 8000 Munchen 40. Tel: 089/309031 Tx: 5216187.
	Micronetics GmbH, Weil der Stadter Str. 45, 7253 Renningen 1. Tel: 07159/6019 Tx: 724708.
	Nordelektronik GmbH, Carl-Zeiss-Str. 6, 2085 Quickborn. Tel: 04106/72072 Tx: 214299.

North American sales offices

NATIONAL SALES	9 Parker, Irvine, CA 92718. Tel: (714) 472-0303 Twx: (910) 595-1930 Telex: 701464 Fax: (714) 770-0627.
EASTERN REGION	1767-42 Veterans Memorial Hwy., Central Islip, NY 11722. Tel: (516) 582-8070 Tlx: 705922 Fax: 516-582-8344.
CHESAPEAKE REGION	9001 I Greentree Commons, Marlton, New Jersey 08053. Tel: (609) 596 2030 Tlx: 62953899 Fax: 609-596-1635.
NEW ENGLAND REGION	132 Central St., 216 Foxboro, MA 02035. Tel: (617) 543-3855 Tlx: 316805 Fax: 305-260-6587.
WESTERN REGION	4633 Old Ironsides Dr. 250, Santa Clara, CA 95054. Tel: (408) 986-8911 Twx: 62217370 Fax: 408-970-0263.
SOUTHEAST REGION	9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930 Twx: 510-600-3635 Fax: 214-680-9753.
NORTH CENTRAL REGION	1919 South Highland 120C, Lombard, IL 60148. Tel: (312) 953-1484 Tlx: 705186 Fax: 312-953-0633.
OHIO VALLEY REGION	1717 E. 116th Street, Ste. 210, Carmel, IN 46032. Tel: (317) 843-0561 Twx: 810-332-1517 Fax: 317-844-4753.
SOUTHWEST REGION	9 Parker, Irvine, CA 92718. Tel: (714) 472-0303.
DISTRIBUTION SALES	9 Parker, Irvine, CA 92718. Tel: (714) 472-0303 Twx: (910) 595-1930 Telex: 701464 Fax: (714) 770-0627.

North American representatives

ALABAMA	**Electronic Marketing Associates, Inc. (EMA),** 1200 Jordan Lane, Suite 4, Jordan Center, Huntsville, AL 35805. Tel: (205) 536-3044 Twx: 910-997-0551.
ARIZONA	**Chaparral Electronics,** 2024 N. 7th Street 200, Phoenix, AZ 85006. Tel: (602) 252-0897 Tlx: 667413.
CALIFORNIA	**Cerco,** 5230 Carrol Canyon Rd. 214, San Diego, CA 92121. Tel: (619) 450-1754 Twx: 910-335-1220.
	Pinnacle Sales Corp., 275 Saratoga Ave., Suite 200, Santa Clara, CA 95050. Tel: (408) 249-7400 Tlx: 910-338-2081 Fax: 408-249-5129.
	Select Electronics, 14480 Alondra Blvd., Suite A, La Mirada, CA 90638. Tel: (714) 739-8891 Twx: 910-596-2818 Fax: 714-739-1604.
COLORADO	**Peak Sales,** 329 N. Circle Drive, Colorado Springs, CO 80909. Tel: (303) 630-0488.
CONNECTICUT	**Scientific Components,** 1185 S. Main St., Cheshire, CT 06410. Tel: (203) 272-2963 Twx: 710-455-2078 Fax: 203-271-3048.
FLORIDA	**Lawrence Associates,** 711 Turnbull Av., Altamonte Springs, FL 32701. Tel: (305) 339-3855.
	Lawrence Associates, 5021 N. Dixie Highway, Boca Raton, FL 33431. Tel: (305) 368-7373 Twx: 510-953-7602 Fax: 305-394-5442.
	Lawrence Associates, 1605 S. Missouri Ave., Clearwater, FL 33516. Tel: (813) 584-8110 Fax: 813-584-5865.
GEORGIA	**Electronic Marketing Associates, Inc. (EMA),** 6695 Peachtree Industrial Blvd., Suite 101, Atlanta, GA 30360. Tel: (404) 448-1215 Twx: 810-766-0483.
INDIANA	**Corrao Marsh, Inc.,** 6211 Stoney Creek Drive, Fort Wayne, IN 46825. Tel: (219) 482-2725 Twx: 910-333-8892 Fax: 219-484-7491.
	Corrao Marsh, Inc., 3117 West U.S. 40, Greenfield, IN 46140. Tel: (317) 462-4446.
ILLINOIS	**Micro Sales, Inc.,** 54 West Seegars Road, Arlington Heights, IL 60006. Tel: (312) 956-1000 Twx: 510-600-0756.
IOWA	**Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666 Twx: 910-525-1370 Fax: 319-377-2273.
KANSAS	**Lorenz Sales, Inc.,** 8020 Santa Fe Dr., Suite G-2, Overland Park, KS 66204. Tel: (913) 649-5556 Fax: 913-649-5944.
MARYLAND	**Walker-Houck,** 10706 Reisters Town Rd., Suite D, Owings Mills, MA 21117. Tel: (301) 356-9500 Tlx: 757850 Fax: 301-356-9503.
MASSACHUSETTS	**Stone Components,** 2 Pierce Street, Framingham, MA 01701. Tel: (617) 875-3266 Twx: 310-374-6662 Fax: 617-875-0537.
MICHIGAN	**Fred Gehrke & Associates,** 29551 Greenfield Rd., Suite 206, Southfield, MI 48076. Tel: (313) 559-5363.
MINNESOTA	**Electronics Sales Agency,** 8053 Bloomington Freeway, Bloomington, MN 55420. Tel: (612) 884-8291 Fax: 612-884-8294.

MISSOURI **Lorenz Sales, Inc.,** Del Crest Plaza Bldg. Suite 208, 8420 Delmar Blvd., University City, MO 63124. Tel: (314) 997-4558 Fax: 314-997-5829.

NEBRASKA **Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660.

NEW JERSEY **Metro Logic,** 280 Midland Ave., Bldg N-1, Saddle Brook, NJ 07662. Tel: (201) 797-8844 Tlx: 135-095-CBO Ft Lee Fax: 201-797-8418.

Tai Corporation, 12S Black Horse Pike, Bellmawr NJ 08031. Tel: (609) 933-2600 Fax: (609) 933-3329.

NEW YORK **L-Mar Associates, Inc.,** 4515 Culver Road, Rochester, NY 14622. Tel: (716) 323-1000 Twx: 62759452 Fax: 716-323-1541.

NORTH CAROLINA **Electronic Marketing Associates, Inc. (EMA),** 92225 Honeycutt Creek Road, Raleigh, NC 27609. Tel: (919) 847-8880 Twx: 510-928-0594.

SOUTH CAROLINA **Electronic Marketing Associates, Inc. (EMA),** 210 W. Stone Ave., Greenville, SC 29609. Tel: (803) 233-4637 Twx: 810-281-225.

OHIO **Stegman Blaine Marketing,** 8444 Winton Road, Cincinnati, OH 45231. Tel: (513) 729-1969 EZ-LINK 62889845.

Stegman Blaine Marketing, 340 North Dixie Drive, Ste. 3, Vandalia, OH 45377. Tel: (513) 890-7975 EZ-LINK 62902094.

Stegman Blaine Marketing, 19701 S. Miles Road, Room 25A, Warrensville, OH 44128. Tel: (216) 475-1515.

OKLAHOMA **Bonser-Philhower Sales (B-P Sales),** 4614 S. Knoxville Ave., Tulsa, OK 74135. Tel: (914) 744-9964 Twx: 510-600-5274 Fax: 918-749-0497 EZ-LINK 62907438.

OREGON **Crown Electronic Sales, Inc.,** 17020 S.W. Upper Boones Ferry Rd., Suite 202, Portland, OR 97223. Tel: (503) 620-8320 Fax: 503-639-4023.

TEXAS **Bonser-Philhower Sales (B-P Sales),** 689 West Renner Road, C., Richardson TX 75080. Tel: (214) 234-8438 Twx: 910-867-4752 Fax: 214-437-0897 EZ-LINK 62801325.

Bonser-Philhower Sales (B-P Sales), 8200 Mopac Expressway, 120, Austin, TX 78759. Tel: (512) 346-9186 Twx: 910-997-8141. Fax: 512-346-2393. EZ-LINK 62689720.

Bonser-Philhower Sales (B-P Sales), 11321 Richmond, Ste., 100A, Houston, TX 77082. Tel: (713) 531-4144 Twx: 910-350-3451 EZ-LINK 62814523.

UTAH **West High Tech,** 369 East 900 South, Salt Lake City, UT 84111. Tel: (801) 466-5739.

Peak Sales, 8780 S. 1275 East, Sandy, UT 84070. Tel: (801) 566-5000.

WASHINGTON **Crown Electronic Sales, Inc.,** 14400 Bel-Red Rd., 108, Bellevue, WA 98007. Tel: (206) 643-8100 Fax: 206-747-6861.

WISCONSIN **Micro Sales, Inc.,** N8 W12920 Leon Road, Suite 115, Menomonee Falls, WI 53051. Tel: (414) 251-0151 Twx: 510-500-0756.

CANADA EASTERN **Eli Manis, Inc.,** P.O.Box 605, Cote St. Luc., Montreal, Quebec H4V 2Z2. Tel: (514) 484-2923 Tlx: 05-25134 MTL.

Eli Manis Shipping Address: 7370 Cote St. Luc Road, Montreal, Quebec H4W 1P9.

North American distributors

ALABAMA **Pioneer/Technologies,** 4825 University Square, Huntsville, AL 35805. Tel: (205) 837-9300 Twx: 810-726-2197

Hammond, 4411 B Evangel Circle, Huntsville, AL 35816. Tel: (205) 830-4764.

ARIZONA **Insight Electronics,** 1525 W. University 105, Tempe, AZ 85282. Tel: (602) 829-1800 Twx: 510-601-1618.

CALIFORNIA **Added Value Electronics,** 1582 Parkway Unit G, Tustin, CA 92680. Tel: (714) 259-8258 Fax: 714-544-2302.

Cypress Electronics, 2175 Martin Ave., Santa Clara, CA 95050. Tel: (408) 980 2500 Fax: 408-986-9584.

Cypress Electronics, 6230 Descanso Ave., Buena Park, CA 90620. Tel: (714) 521-5230 Twx: 5215716 Fax: 714-521-5716.

Insight Electronics, 6885 Flanders Dr., Unit G, San Diego, CA 92121. Tel: (619) 587-0471 Twx: 183035 Fax: 619-587-1380.

Insight Electronics, 1525 W. University Dr., Suite 105, Tempe AZ 85282. Tel: (602) 829-1800 Twx: 510-601-1618.

Insight Electronics, 3505 Cadillac Ave. Unit E-1, Costa Mesa CA 92626. Tel: (714) 556-6890 Twx: 62354990 Fax: 714 556-6897.

Nepenthe, 2471 East Bayshore 520, Palo Alto, CA 94303. Tel: (415) 856-9332 Twx: 910-373-2060.

NORTH CAROLINA **Hammond,** 2923 Pacific Ave., Greensboro, NC 27406. Tel: (919) 275-6391 Twx: 62894645.

Pioneer/Technologies, 9801A South Pine Blvd., Charlotte, NC 28210. Tel: (704) 527-8188 Twx: 810-621-0366.

COLORADO **Cypress Electronics,** 12441 West 48th Ave., Wheatridge, CO 80033. Tel: (303) 431-2622 Fax: 303-431-7191.

CONNECTICUT	**Pioneer/Standard,** 112 Main Street, Norwalk, CT 06851. Tel: (203) 853-1515 Twx: 710 468
FLORIDA	**Hammond,** 6600 N.W. 21st Ave., Ft. Lauderdale, FLA 33309. Tel: (305) 973-7103 Twx: 510-956-9401.
	Hammond, 1230 West Central Blvd., Orlando, FLA 32802. Tel: (305) 849-6060 Twx: 810-850-4121.
	Pioneer/Technologies, 674 South Military Trail, Deerfield Beach, FL 33442. Tel: (305) 428-8877 Twx: 510-995-9653.
	Pioneer/Technologies, 337 South Northlake Blvd., Suite 1000, Altamonte Springs, FLA 32701. Tel: (305) 834-9090 Twx: 810-853-0284.
GEORGIA	**Hammond,** 6000 Dawson Blvd., H. Norcross, GA 30093. Tel: (404) 449-1996.
	Pioneer/Technologies, 3100 F Northwoods Pl., Norcross, GA 30071. Tel: (404) 448-1711 Twx: 810-766-4515.
INDIANA	**Pioneer/Standard,** 6408 Castleplace Dr., Indianapolis, IN 46250. Tel: (317) 849-7300 Twx: 810-260-1794.
ILLINOIS	**Pioneer/Standard,** 1551 Carmen Drive, Elk Grove Vlge., IL 60007. Tel: (312) 437-9680 Twx: 910-222-1834.
KANSAS	**Pioneer,** 10551 Lackman Rd., Lenexa, KS 66215. Tel: (913) 492-0500 Twx: 510-601-6411.
MASSACHUSETTS	**Emtel Electronics,** 375 Vanderbilt Ave., Norwood, MA 02062. Tel: (617) 769-9500.
	Pioneer/Standard, 44 Hartwell Avenue, Lexington, MA 02173. Tel: (617) 861-9200 Twx: 710-326-6617.
MARYLAND	**Pioneer Tech. Group. Inc.,** 9100 Gaither Rd., Gaithersbury, MD 20877. Tel: (301) 921-0660 Twx: 710-828-0545.
MICHIGAN	**Pioneer/Standard,** 13485 Stamford, Livonia, MI 48150. Tel: (313) 525-1800 Twx: 810-242-3271.
	Pioneer, 4505 Broadmoor Ave., S.E., Grand Rapids, MI 49508. Tel: (616) 698-1800 Twx: 510-600-8456.
MINNESOTA	**Pioneer/Standard,** 10203 Bren Road East, Minnetonka, MN 55243. Tel: (612) 925-5444 Twx: 910-576-2738.
NEW JERSEY	**Pioneer/Standard,** 45 Rte. 46 Pinebrook, NJ 07058. Tel: (201) 575-3510 Twx: 710-734-4382.
NEW YORK	**General Components, Inc.,** 245 D Clifton Ave., W. Berlin, NY 08091. Tel: (609) 768-6767 Twx: 910-333-3057.
	Mast, 215 Marcus Bld., Hauppaugh, NY 11788. Tel: (516) 273-4422 Twx: 510 227 6622.
	Pioneer/Standard, 60 Crosswalks Park West, Woodbury, NY 11797 Tel: (516) 921-8700 Twx: 510-221-2184.
	Pioneer/Standard, 840 Fairport Park, Fairport Park, NY 14450. Tel: (716) 381-7070 Twx: 510-253-7001.
	Pioneer/Standard, 1806 Vestal Parkway East, Vestal, NY 13850. Tel: (607) 748-8211 Twx: 510-252-0893.
OHIO	**Pioneer/Standard,** 4800 East 131st St., Cleveland, OH 44105. Tel: (216) 587-3600 Twx: 810-421-0011.
	Pioneer, 4433 Interpoint Bl., Dayton, OH 45424. Tel: (513) 236-9900 Twx: 810 459 1622.
PENNSYLVANIA	**Pioneer/Technologies,** 261 Gibraltar Rd., Horsham, PA 19044. Tel: (215) 674-4000 Twx: 510-665-6778.
	Pioneer/Standard, 259 Kappa Drive, Pittsburg, PA 15238. Tel: (412) 782-2300 Twx: 710-795-3122
TEXAS	**Pioneer/Standard,** 9901 Burnet Road, Austin, TX 78758. Tel: (512) 835-4000 Twx: 910-874-1323
	Pioneer/Standard, 13710 Omega Road, Dallas, TX 75244. Tel: (214) 386-7300 Twx: 910-860-5563.
	Pioneer/Standard, 5853 Point West Drive, Houston, TX 77036. Tel: (713) 988-5555 Twx: 910-881-1606.
CANADA EASTERN	**Semad,** 9045 Cote De Liesse 101, Dorval, Quebec H9P 2M9. Tel: (514) 636-4614 Twx: 05821861.
	Semad, 1827 Woodward Dr., Suite 303, Ottawa, Ontario K2C 0R3. Tel: (613) 727-8325. Twx: 0533943.
CANADA WESTERN	**Semad,** 75 Glendeer Dr. E 210, Calgary, Alberta T2H 2S8. Tel: (403) 252-5664 Twx: 03824775.
	RAE, 3455 Gardner Ct., Burnaby, BC V5G 4J7. Tel: (604) 291-8866. Twx: 04356533.
	Semad, 3700 Gilmore 210, Burnaby, BC V5G 4M1. Tel: (604) 438-2515. Twx: 04356625.
	Semad, 85 Spy Court, Markham, Ontario, L3R 4Z4. Tel: (416) 475-3922 Twx: 06966600.