Raytheon

Linear Integrated Circuits

1989

Linear 1989

Raytheon

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ALPHANUMERIC INDEX

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AD558		DAC-4888
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AD581		REF-01
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AD707		RC4077
AD708		RC4277
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AD767		DAC-4881
AM686		RC4805
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CA124	LM124	
CA324	LM324	
CA139	LM139	
CA339	LM339	
CA741	RC741	
CS3842		RC4190
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CMP-05		RC4805
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DAC-10	DAC-10	
DAC-80		DAC-4881
DAC-100		DAC-10
DAC-312	DAC-6012	
DAC0800	DAC-08	
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DAC0830		DAC-4888
DAC-888		DAC-4888
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INDUSTRY TYPE	RAYTHEON DIRECT REPLACEMENT	RAYTHEON FUNCTIONAL REPLACEMENT
ICL7660		RC4391
ICL7680		RC4190
ICL8013		RC4200
LF155	LF155	
LF156	LF156	
LF157	LF157	
LH2101	LH2101	
LH2108	LH2108	
LH2111	LH2111	
LM101	LM101	
LM111	LM111	
LM108	LM108	
LM124	LM124	
LM148	LM148	
LM324	LM324	
LM331		RC4152
LM348	LM348	
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LM607		RC4077
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General Cross References (Continued)

INDUSTRY TYPE	RAYTHEON DIRECT REPLACEMENT	RAYTHEON FUNCTIONAL REPLACEMENT
MC4741	RC4741	
MPREF01	REF-01	
MPREF02	REF-02	
MPOP07	OP-07	
MPOP27	OP-27	
MPOP37	OP-37	
MP108	LM108	
MP155	LM155	
MP156	LM156	
MP157	LM157	
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OP-200		RC4207, RC4277
OP-207		RC4207
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OP-270		RC4227
PM-108	LM108	
PM-139	LM139	
PM-148	LM148	
PM-155	LM155	
PM-156	LM156	
PM-157	LM157	
PM-339	LM339	
PM-348	LM348	
PM-741	RC741	
PM-747	RC747	
RC4136	RC4136	
RC4151	RC4151	
RC4152	RC4152	
RC4558	RC4558	
RC4559	RC4559	
REF-01	REF-01	
REF-02	REF-02	
REF-05		REF-02
REF-10		REF-01
SE5534		RC5534
SG101	LM101	
SG124	LM124	
SG741	RC741	
SI-9100		RC4292
SSM-2134		RC5534
TA7504	RC741	
TA75339	LM339	
TL494		RC4190
TL496		RC4190
TL497		RC4190
TL510		RC4805
TSC9400		RC4151
TSC9401		RC4151
TSC9402		RC4151
UC1842		RC4292
VFC-32		RC4153
XR-2207	XR-2207	
XR-2208		RC4200
XR-2211	XR-2211	
XR-3403	RC3403	
XR-4136	RC4136	
XR-4194	RC4194	
XR-4195	RC4195	
XR-5532	RC5532	
XR-5534	RC5534	
µA101	LM101	
µA108	LM108	
µA111	LM111	
µA124	LM124	
µA139	LM139	
µA148	LM148	
µA324	LM324	
µA339	LM339	
µA348	LM348	
µA741	RC741	
µA747	RC747	

Precision Operational Amplifier Cross Reference

ANALOG DEV.	RAYTHEON	PACKAGE
AD OP-07AH	*OP-07AT	TO-99
AD OP-07AH/883	*OP-07AT/883B	TO-99
AD OP-07CN	*OP-07CN	PLASTIC
AD OP-07CR	*OP-07CM	SO-8
AD OP-07Q/883	*OP-07D/883B	CERAMIC
AD OP-07DN	*OP-07DN	PLASTIC
AD OP-07EN	*OP-07EN	PLASTIC
AD OP-07H	*OP-07T	TO-99
AD OP-07H/883	*OP-07T/883B	TO-99
AD OP-07Q	*OP-07D	CERAMIC
AD OP-07AQ	*OP-07AD	CERAMIC
AD OP-07AQ/883B	*OP-07AD/883B	CERAMIC
AD OP-27AH	OP-27AT	TO-99
AD OP-27AH/883	OP-27AT/883B	TO-99
AD OP-27AQ	OP-27AD	CERAMIC
AD OP-27AQ/883	OP-27AD/883B	CERAMIC
AD OP-27BH	OP-27BT	TO-99
AD OP-27BH/883	OP-27BT/883B	TO-99
AD OP-27BQ	OP-27BD	CERAMIC
AD OP-27BQ/883	OP-27BD/883B	CERAMIC
AD OP-27CH	OP-27CT	TO-99
AD OP-27CH/883	OP-27CT/883B	TO-99
AD OP-27CQ	OP-27CD	CERAMIC
AD OP-27CQ/883	OP-27CD/883B	CERAMIC
AD OP-27EN	OP-27EN	PLASTIC
AD OP-27FN	OP-27FN	PLASTIC
AD OP-27GN	OP-27GN	PLASTIC
AD OP-37AE	OP-37AL	LCC
AD OP-37AE/883	OP-37AL/883B	LCC
AD OP-37AH	OP-37AT	TO-99
AD OP-37AH/883	OP-37AT/883B	TO-99
AD OP-37AQ	OP-37AD	CERAMIC
AD OP-37AQ/883	OP-37AD/883B	CERAMIC
AD OP-37BH	OP-37BT	TO-99
AD OP-37BH/883	OP-37BT/883B	TO-99
AD OP-37BQ	OP-37BD	CERAMIC
AD OP-37BQ/883	OP-37BD/883B	CERAMIC
AD OP-37CH	OP-37CT	TO-99
AD OP-37CH/883	OP-37CT/883B	TO-99
AD OP-37CQ	OP-37CD	CERAMIC
AD OP-37CQ/883	OP-37CD/883B	CERAMIC
AD OP-37EN	OP-37EN	PLASTIC
AD OP-37FN	OP-37FN	PLASTIC
AD OP-37GN	OP-37GN	PLASTIC
AD707AQ	*RC4077FD	CERAMIC
AD707CH	*RM4077AT	TO-99
AD707CH/883	*RM4077AT/883B	TO-99
AD707CQ	*RM4077AD	CERAMIC
AD707CQ/883	*RM4077AD/883B	CERAMIC
AD707JN	*RC4077FN	PLASTIC
AD707JR	*RC4077FM	SO-8
AD707KN	*RC4077EN	PLASTIC
AD707KR	*RC4077EM	SO-8
AD707SH	*RC4077AT	TO-99
AD707SH/883B	*RC4077AT/883B	TO-99
AD707SQ	*RC4077AD	CERAMIC
AD707SQ/883	*RC4077AD/883B	CERAMIC
AD707TH	*RC4077AT	TO-99
AD707TH/883B	*RC4077AT/883B	TO-99
AD707TQ	*RC4077AD	CERAMIC
AD707TQ/883	*RC4077AD/883B	CERAMIC

BURR BROWN	RAYTHEON	PACKAGE
OPA27AJ/883	*OP-27AT/883B	TO-99
OPA27BJ/883	*OP-27BT/883B	TO-99
OPA27CJ	*OP-27CT/883B	TO-99
OPA27AJ	*OP-27AT	TO-99
OPA27AZ	*OP-27AD	CERAMIC
OPA27BJ	*OP-27BT	TO-99
OPA27BZ	*OP-27BD	CERAMIC
OPA27CJ	*OP-27CT	TO-99
OPA27CZ	*OP-27CD	CERAMIC
OPA27EP	*OP-27EN	PLASTIC
OPA27FP	*OP-27FN	PLASTIC
OPA27GP	*OP-27GN	PLASTIC
OPA27GU	*OP-27GM	SO-8
OPA27GZ	*OP-27GD	CERAMIC
OPA27AZ/883	*OP-27AD/883B	CERAMIC
OPA27BZ/883	*OP-27BD/883B	CERAMIC
OPA27CZ/883	*OP-27CD/883B	CERAMIC
OPA37AJ	*OP-37AT	TO-99
OPA37AJ/883	*OP-37AT/883B	TO-99
OPA37AZ	*OP-37AD	CERAMIC
OPA37AZ/883	*OP-37AD/883B	CERAMIC
OPA37BJ	*OP-37BT	TO-99
OPA37BJ/883	*OP-37BT/883B	TO-99
OPA37BZ	*OP-37BD	CERAMIC
OPA37BZ/883	*OP37-BD/883B	CERAMIC
OPA37CJ	*OP-37CT	TO-99
OPA37CJ/883	*OP-37CT/883B	TO-99
OPA37CJ/883	*OP-37CD/883B	CERAMIC
OPA37CZ	*OP-37CD	CERAMIC
OPA37EP	*OP-37EN	PLASTIC
OPA37FP	*OP-37FN	PLASTIC
OPA37GP	*OP-37GN	PLASTIC
OPA37GU	*OP-27GM	SO-8

* Denotes functionally equivalent types.

Precision Operational Amplifier Cross Reference (Continued)

LTC	RAYTHEON	PACKAGE
OP-07AH	OP-07AT	TO-99
OP-07AH/883B	OP-07AT/883B	TO-99
OP-07AJ8	OP-07AD	CERAMIC
OP-07AJ8/883B	OP-07AD/883B	CERAMIC
OP-07CN8	OP-07CN	PLASTIC
OP-07CS8	OP-07CM	SO-8
OP-07EN8	OP-07EN	PLASTIC
OP-07H	OP-07T	TO-99
OP-07H/883B	OP-07T/883B	TO-99
OP-07J8	OP-07D	CERAMIC
OP-07J8/883B	OP-07D/883B	CERAMIC
OP-27AH	OP-27AT	TO-99
OP-27AH/883B	OP-27AT/883B	TO-99
OP-27AJ8	OP-27AD	CERAMIC
OP-27AJ8/883B	OP-27AD/883B	CERAMIC
OP-27CH	OP-27CT	TO-99
OP-27CH/883B	OP-27CT/883B	TO-99
OP-27CJ8	OP-27CD	CERAMIC
OP-27CJ8/883B	OP-27CD/883B	CERAMIC
OP-27EN8	OP-27EN	PLASTIC
OP-27GN8	OP-27GN	PLASTIC
OP-37AH	OP-37AT	TO-99
OP-37AH/883B	OP-37AT/883B	TO-99
OP-37AJ8	OP-37AD	CERAMIC
OP-37AJ8/883B	OP-37AD/883B	CERAMIC
OP-37CH	OP-37CT	TO-99
OP-37CH/883B	OP-37CT/883B	TO-99
OP-37CJ8	OP-37CD	CERAMIC
OP-37CJ8/883B	OP-37CD/883B	CERAMIC
OP-37EN8	OP-37EN	PLASTIC
OP-37GN8	OP-37GN	PLASTIC

LTC	RAYTHEON	PACKAGE
LM108AH	LM108AT	TO-99
LM108AH/883B	LM108AT/883B	TO-99
LM108AJ8/883B	LM108AD/883B	CERAMIC
LM108H	LM108T	TO-99
LM108H/883B	LM108T/883B	TO-99
LM108J8/883B	LM108D/883B	CERAMIC
LT1001ACH	LT-1001ACT	TO-99
LT1001ACN8	LT-1001ACN	PLASTIC
LT1001AMH/883B	LT-1001AMT/883B	TO-99
LT1001AMJ8	LT-1001AMD	CERAMIC
LT1001AMJ8/883	LT-1001AMD/883B	CERAMIC
LT1001CH	LT-1001CT	TO-99
LT1001CN8	LT-1001CN	PLASTIC
LT1001CS8	LT-1001CM	SO-8
LT1001MH	LT-1001MT	TO-99
LT1001MH/883B	LT-1001MT/883B	TO-99
LT1001MJ8	LT-1001MD	CERAMIC
LT1001MJ8/883B	LT-1001MD/883B	CERAMIC
OP-227EN	*RC4227FN	PLASTIC
OP-227GN	*RC4227GN	PLASTIC
OP-227AJ	*RM4227BD	CERAMIC
OP-227AJ/883B	*RM4227BD/883B	CERAMIC

*Denotes functionally equivalent types.
NOTE: LTC OP-227 contains two die in a 14-pin package.
Raytheon's 4227 is a monolithic IC in an 8-pin package.

Precision Operational Amplifier Cross Reference (Continued)

PMI	RAYTHEON	PACKAGE
OP07AJ	OP-07AT	TO-99
OP07AJ/883	OP-07AT/883B	TO-99
OP07AZ	OP-07AD	CERAMIC
OP07AZ/883	OP-07AD/883B	CERAMIC
OP07CP	OP-07CN	PLASTIC
OP07CS	OP-07CM	SO-8
OP07DP	OP-07DN	PLASTIC
OP07DS	OP-07DM	SO-8
OP07EP	OP-07EN	PLASTIC
OP07J	OP-07T	TO-99
OP07J/883	OP-07T/883B	TO-99
OP07RC/883	OP-07L/883B	LCC
OP07Z	OP-07D	CERAMIC
OP07Z/883	OP-07D/883B	CERAMIC
OP27AJ	OP-27AT	TO-99
OP27AJ/883	OP-27AT/883B	TO-99
OP27AZ	OP-27AD	CERAMIC
OP27AZ/883	OP-27AD/883B	CERAMIC
OP27BJ	OP-27BT	TO-99
OP27BJ/883	OP-27BT/883B	TO-99
OP27BRC/883	OP-27BL/883B	LCC
OP27BZ	OP-27BD	CERAMIC
OP27BZ/883	OP-27BD/883B	CERAMIC
OP27CJ	OP-27CT	TO-99
OP27CJ/883	OP-27CT/883B	TO-99
OP27CZ	OP-27CD	CERAMIC
OP27CZ/883	OP-27CD/883B	CERAMIC
OP27EP	OP-27EN	PLASTIC
OP27FP	OP-27FN	PLASTIC
OP27FS	OP-27FM	SO-8
OP27GS	OP-27GM	SO-8
OP27GP	OP-27GN	PLASTIC
OP37AJ	OP-37AT	TO-99
OP37AJ/883	OP-37AT/883B	TO-99
OP37AZ	OP-37AD	CERAMIC
OP37AZ/883	OP-37AD/883B	CERAMIC
OP37BJ	OP-37BT	TO-99
OP37BJ/883	OP-37BT/883B	TO-99
OP37BRC/883	OP-37BL/883B	LCC
OP37BZ	OP-37BD	CERAMIC
OP37BZ/883	OP-37BD/883B	CERAMIC
OP37CJ	OP-37CT	TO-99
OP37CJ/883	OP-37CT/883B	TO-99
OP37CZ	OP-37CD	CERAMIC
OP37CZ/883	OP-37CD/883B	CERAMIC
OP37EP	OP-37EN	PLASTIC
OP37FP	OP-37FN	PLASTIC

PMI	RAYTHEON	PACKAGE
OP77AJ	OP-77AT	TO-99
OP77AJ/883	OP-77AT/883B	TO-99
OP77AZ	OP-77AD	CERAMIC
OP77AZ/883	OP-77AD/883B	CERAMIC
OP77BJ	OP-77BT	TO-99
OP77BJ/883	OP-77BT/883B	TO-99
OP77BRC/883	OP-77BL/883B	LCC
OP77BZ	OP-77BD	CERAMIC
OP77BZ/883	OP-77BD/883B	CERAMIC
OP77EP	OP-77EN	PLASTIC
OP77FP	OP-77FN	PLASTIC
OP77FS	OP-77FM	SO-8
OP77GP	OP-77GN	PLASTIC
OP77GS	OP-77GM	SO-8
PM108AZ	LM108AD	CERAMIC
PM108AZ/883	LM108AD/883B	CERAMIC
PM108AJ	LM108AT	TO-99
PM108AJ/883	LM108AT/883B	TO-99
PM108ARC	LM108AL	LCC
PM108ARC/883	LM108AL/883B	LCC
PM108DZ	LM108D	CERAMIC
PM108DZ/883	LM108D/883B	CERAMIC
PM108J	LM108T	TO-99
PM108J/883	LM108T/883B	TO-99
PM2108AQ	LH2108AD	CERAMIC
PM2108AQ/883	LH2108AD/883B	CERAMIC
PM2108Q	LH2108D	CERAMIC
PM2108Q/883	LH2108D/883B	CERAMIC
OP207AY/883	*RM4207BD/883B	CERAMIC
OP207AY	*RM4207BD	CERAMIC
OP227AY	*RM4227BD	CERAMIC
OP227AY/883	*RM4227BD/883B	CERAMIC
OP227BY/883	*RM4227BD/883B	CERAMIC
OP227GY	*RC4227GN	PLASTIC

* Denotes functionally equivalent types.
NOTE: PMI"s OP207/227 contains two die in a 14-pin package.
Raytheon's 4207/4227 is a monolithic IC in an 8-pin package.

General Purpose Operational Amplifier Cross Reference

Raytheon	PMI	FSC	AMD	Motorola	National	RCA	Signetics	T.I.
LH2101A			LH2101A		LH2101A		LH2101A	
LH2111			LH2111		LH2111			
LM101A		µA101A	LM101A	LM101A	LM101A	CA101A	LM101A	
LM111		µA111	LM111	LM111	LM111	CA111	LM111	
LM124		µA124	LM124	LM124	LM124	CA124	LM124	LM124
LM139	PM139	µA139	LM139	LM139	LM139	CA139	LM139	LM139
LM148	PM148	µA148	LM148		LM148		LM148	
LM301A		µA301A	LM301A	LM301A	LM301A	CA301A	LM301A	LM301A
LM324		µA324	LM324	LM324	LM324	CA324	LM324	LM324
LM339	PM339	µA339	LM339	LM339	LM339	CA339	LM339	LM339
LM348		µA348	LM348		LM348		LM348	LM348
LM2900		µA2900			LM2900			
LM3900		µA3900			LM3900			LM3900
RC3403A		µA3403		MC3403				MC3403
RC4136	OP-09	µA4136						RC4136
RC4156		µA148*		MC4741	LM348*			LM348*
RC4157		µA148/ 348*		MC4741*	LM348*			LM348*
RC4558		µA4558		MC4558				RC4558
RC4559		µA4558*		MC4558*				RC4559
RC4741N				MC3-4741-5				
RM4741D				MC1-4741-2				
RC5532							NE5532	NE5532
RC5532A							NE5532A	NE5532A
RC5534							NE5534	NE5534
RC5534A							NE5534A	NE5534A
RC741	OP-02	µA741		MC1741	LM741	CA741	CA741	
RC747	OP-04	µA747		MC1747	LM747	CA747	CA747	
RC747S	OP-04	µA747			LM747			

*Functional Equivalent

Data Conversion Cross Reference

Raythen	PMI	AMD	Motorola	NSC	Devices	Analog Power	Micro-Datel
DAC-08AD	DAC-08AQ	AMDAC-08AQ	MC1408L8	DAC-08AQ	AD-1508-9D	MP-7523*	DAC-IC8BC*
DAC-08D	DAC-08Q	AMDAC-08Q		DAC-08Q	AD-1508-9D	MP-7523*	DAC-IC8BC*
DAC-08ED	DAC-08EQ	AMDAC-08EQ		DAC-08EQ	AD-1408-8D	MP-7523*	DAC-IC8UP*
DAC-08EN	DAC-08EP	AMDAC-08EN		DAC-08EP			DAC-IC8UP*
DAC-08CN	DAC-08CP	AMDAC-08CN	MC1408P6	DAC-08CP			DAC-IC8UP*
DAC-10BD	DAC-10BX			DAC-1020 LD*	AD7520/30/33*	MP-7520/30/33*	DAC- HF10BMM*
DAC-10CD	DAC-10CX			DAC-1021/22LD8*	AD7520/30/33*	MP-7520/30/33*	DAC- HF10BMM*
DAC-10FD	DAC-10FX			DAC-1020 LCN*	AD7520/30/33*	MP-7520 30/33*	DAC- HF10BMC*
DAC-10GD	DAC-10GX			DAC-1021/22LCN*	AD7520/30/33*	MP-7520/30/33*	DAC-HF10BMC*
DAC- 6012AMD		AM6012ADM		DAC-1220 LD*	AD6012ADM	MP-7531/41*	DAC-HF12BMM*
DAC- 6012MD	DAC-312 BR*	AM6012DM		DAC-1221/22LD*	AD6012DM	MP-7531/41*	DAC- HF12BMM*
DAC- 6012ACN		AM6012ADC		DAC-1220 LCN*	AD6012ADC	MP-7531/41*	DAC- HF12BMC*
DAC- 6012CN	DAC-312FR*	AM6012DC		DAC-1221/22LCN*	AD6012DC	MP-7531/41*	DAC- HF12BMC*
DAC-8565DS*				MC3412L	DAC-1208 AD-I*	AD565JD/BIN	
DAC-8565JS*				MC3412L	DAC-1280 HCD-I*	AD565JD/BIN	
DAC-8565SS*					DAC-1280 HCD-I*	AD565SD/BIN	

*Functional Equivalent

Special Functions Cross Reference

Raytheon	Teledyne	Analog Devices	EXAR	Motorola	Datel	Burr Brown
RC4151	4780*	AD451*	XR4151		VFQ-1C*	VFC-32KF*
RC4152	4781*	AD452*	XR4151*		VFQ-2C*	VFC-42BP*
RC4153	4782*	AD537*			VFQ-3C*	VFC-52BP*
RC4200/A		AD539*		MC1494*		4202K* & 4205K*
XR2207			XR2207			
XR2211			XR2211			
RC4444				MC3416		

*Functional Equivalent

Voltage Regulator and Voltage Reference Cross Reference

Raytheon	EXAR	Maxim	T.I.	Analog Devices	Motorola	NSC
REF-01	REF-01		MP-5501	AD581*	MC1504AU10*	LH0070-0*
REF-01A	REF-01A		MP-5501A	AD581*		LH0070-1*
REF-01C	REF-01C		MP-5501C	AD581*	MC1404U10*	LH0070-2*
REF-01D	REF-01D		MP-5501D	AD581*	MC1404U10*	
REF-01E	REF-01E		MP-5501E	AD581*		
REF-01H	REF-01H		MP-5501H	AD581*	MC1404AU10*	
REF-02	REF-02		MP-5502		MC1504AU5*	LM136-5.0*
REF-02A	REF-02A		MP-5502A			LM136A-5.0*
REF-02C	REF-02C		MP-5502C		MC1404U5*	LM336-5.0*
REF-02D	REF-02D		MP-5502D		MC1404U5*	LM336-5.0*
REF-02E	REF-02E		MP-5502E			LM336A-5.0*
REF-02H	REF-02H		MP-5502H		MC1404AU5*	
RC4190		MAX630*				
RC4193		MAX630*				
RC4391		MAX634*				
RC4194	XR4194CN					
RC4195	XR4195CP				MC1468/ MC1568*	LM325/326*

*Functional Equivalent

SECTION 2
PRODUCT SELECTION GUIDE

Precision Operational Amplifiers

Input Offset Voltage Selection Table by Package Type
(+25°C limits, in microvolts)

Part Type	Plastic Dip (N)	SOIC (M)	Ceramic Dip (D)	Leadless Chip Carrier (L)	Metal Can TO-99 (T)
RC4077	±10	±25	±10	±10	±10
RC4097	±15	±25	±15		±15
RC4207*	±75		±75		
RC4227*	±75		±75		
RC4277*	±30		±30		
OP-07	±75	±75	±25	±25	±25
OP-27	±25	±25	±25	±25	±25
OP-37	±25	±25	±25	±25	±25
OP-47	±25	±25	±25	±25	±25
OP-77	±25	±60	±25	±25	±25
LT1001	±25	±25	±15	±15	±15
LT-1012	±50				±35
LM108			±500	±500	±500
LH2108*			±500	±500	±500

* Dual

Precision Operational Amplifiers

Type	Description	Electrical Characteristics (min/max except *)						
		V_{os} (μV)	TCV_{os} (μV/°C)	I_{os} (nA)	I_B (nA)	CMRR (dB)	Gain (V/μV)	I_{sy} (mA
RC4077A	Ultra Low V_{os}	10	0.3	1.5	±2.0	120	5	1.67
RC4077E		25	0.3	1.5	±2.0	120	5	1.67
RC4077F		60	0.6	2.8	±2.8	116	2	1.67
RM4077A		10	0.3	1.5	±1.5	120	5	1.67
RC4097A	Low I_B,	15	0.3	0.1	±0.1	120	1.0	0.6
RC4097E	Low Power	25	0.6	0.1	±0.1	120	1.0	0.6
RC4097F		60	1.2	0.15	±0.15	110	0.6	0.6
RV4097E		25	0.6	0.1	±0.1	120	1.0	0.6
RV4097F		60	1.2	0.15	±0.15	110	0.6	0.6
RM4097A		15	0.3	0.1	±0.1	120	1.0	0.6
RC4207F	Dual Low Noise	75	1.3	5	±5	100	0.4	6.67
RC4207G		150	0.7*	10	±10	94	0.25	8.0
RM4207B		75	1.3	5	±5	100	0.4	6.67
RC4227F	Dual Low Noise	75	1.3	10	±15	104	0.5	6.67
RC4227G		150	0.4*	15	±25	100	0.4	8.0
RM4227B		75	1.3	10	±15	104	0.5	6.67
RC4277E	Dual Low V_{os}	30	0.3	0.3	±3.0	120	5.0	5.5
RC4277F		75	1.0	5.0	±5.0	110	2.5	5.5
RV4277E		30	0.3	3.0	±3.0	120	5.0	5.5
RV4277F		75	1.0	5.0	±5.0	110	2.5	5.5
RM427A		30	0.3	3.0	±3.0	120	5.0	5.5
LH2108A	Low Noise	500	5.0	0.2	±2.0	96	.04	0.4
LH2108		2000	15	0.2	±2.0	85	.025	0.4
LM108A		500	5.0	0.2	±2.0	96	.04	0.4
LM108		2000	15	0.2	±2.0	85	.025	0.4
LT1001AM	Ultra Low V_{os}	15	0.6	2.0	±2.0	114	0.45	2.5
LT1001AC		25	0.6	2.0	±2.0	114	0.45	2.5
LT1001C		60	1.0	3.8	±4.0	110	0.4	2.67
LT1001M		60	1.0	3.8	±4.0	110	0.4	2.67
LT1012C	Low I_B,	50	1.5	0.15	±0.15	110	0.2	0.6
LT1012M	Low Power	35	1.5	0.1	±0.1	114	0.3	0.6
OP-07A	Low V_{os}	25	0.6	2.0	±2.0	110	0.3	4.0
OP-07		75	1.3	2.8	±3.0	110	0.2	4.0
OP-07E		75	1.3	3.8	±4.0	106	0.2	4.0
OP-07C		150	1.8	6.0	±7.0	100	0.12	5.0
OP-07D		150	2.5	6.0	±12	94	0.12	5.0
OP-27A	Ultra-Low Noise	25	0.6	35	±40	114	1.0	4.67
OP-27B		60	1.3	50	±55	106	1.0	4.67
OP-27C		100	1.8	75	±80	100	0.7	5.67
OP-27E		25	0.6	35	±40	114	1.0	4.67
OP-27F		60	1.3	50	±55	106	1.0	4.67
OP-27G		100	1.8	75	±80	100	0.7	5.67
OP-37A	Decompensated	25	0.6	35	±40	114	1.0	4.67
OP-37B	(AC Stable With	60	1.3	50	±55	106	1.0	4.67
OP-37C	$AV_{CL} \geq 5$)	100	1.8	75	±80	100	0.7	5.67
OP-37E		25	0.6	35	±40	114	1.0	4.67
OP-37F		60	1.3	50	±55	106	1.0	4.67
OP-37G		100	1.8	75	±80	100	0.7	5.67
OP-47A	Decompensated	25	0.6	35	±40	114	1.0	4.67
OP-47B	(AC Stable With	60	1.3	50	±55	106	1.0	4.67
OP-47C	$AV_{CL} \geq 400$)	100	1.8	75	±80	100	0.7	5.67
OP-47E		25	0.6	35	±40	114	1.0	4.67
OP-47F		60	1.3	50	±55	106	1.0	4.67
OP-47G		100	1.8	75	±80	100	0.7	5.67
OP-77A	Low V_{os}	25	0.3	1.5	±2.0	120	5.0	2.0
OP-77B		60	0.6	2.8	±2.8	116	2.0	2.0
OP-77E		25	0.3	1.5	±2.0	120	5.0	2.0
OP-77F		60	0.6	2.8	±2.8	116	2.0	2.0
OP-77G		100	1.2	2.8	±2.8	116	2.0	2.0

Slew (V/μS)	GBW* (mHz)	Noise** (nV/√Hz)	Packages M SOIC	D CDIP	N PDIP	T TO-99	L LCC	Temperature Range -55° to +125°	-25° to +85°	0°to +70°	Mil-Std 883/B Availability
0.3	0.8	18			X				X		
0.3	0.8	18	X	X	X	X			X	X	
0.3	0.8	20	X	X	X	X			X	X	
0.3	0.8	18		X		X	X	X			X
0.3	0.8	30			X					X	
0.3	0.8	30	X		X					X	
0.3	0.8	30	X		X					X	
0.3	0.8	30		X		X			X		
0.3	0.8	30		X		X			X		
0.3	0.8	30		X		X		X			X
0.3	1.5	10.3*		X	X					X	
0.3	1.5	10.3*		X	X					X	
0.3	1.5	10.3*		X				X			X
2.7	8.0	3.8*		X	X					X	
2.7	8.0	3.8*		X	X					X	
2.7	8.0	3.8*		X				X			X
0.3	1.5	10.3*			X					X	
0.3	1.5	10.3*			X					X	
0.3	1.5	10.3*		X					X		
0.3	1.5	10.3*		X					X		
0.3	1.5	10.3*		X				X			X
0.3	1.0	30		X				X			X
0.3	1.0	30		X				X			X
0.3	1.0	30		X		X	X	X			X
0.3	1.0	30				X	X	X			X
0.3	0.8	18		X		X	X	X			X
0.3	0.8	18	X	X	X	X					
0.3	0.8	18	X	X	X	X					
0.3	0.8	18		X		X					
0.3	0.8	30			X	X				X	
0.3	0.8	30				X		X			X
0.3	0.5	18		X		X	X	X			X
0.3	0.5	18		X		X	X	X			X
0.3	0.5	18	X	X	X	X				X	
0.3	0.5	20	X	X	X	X				X	
0.3	0.5	20	X	X	X	X				X	
2.8	8.0	5.5		X		X	X	X			X
2.8	8.0	5.5		X		X	X	X			X
2.8	8.0	8.0		X		X	X	X			X
2.8	8.0	5.5	X	X	X	X			X	X	
2.8	8.0	5.5	X	X	X	X			X	X	
2.8	8.0	8.0	X	X	X	X			X	X	
17	63	5.5		X		X	X	X			X
17	63	5.5		X		X	X	X			X
17	63	8.0		X		X	X	X			X
17	63	5.5	X	X	X	X			X		
17	63	5.5	X	X	X	X			X		
17	63	8.0	X	X	X	X			X		
50	70	5.5		X		X	X	X			X
50	70	5.5		X		X	X	X		X	X
50	70	8.0		X		X	X	X		X	X
50	70	5.5	X	X	X	X			X		
50	70	5.5	X	X	X	X			X	X	
50	70	8.0	X	X	X	X			X	X	
0.3	0.6	18		X		X	X	X			X
0.3	0.6	18		X		X	X	X			X
0.3	0.6	18		X	X	X			X		
0.3	0.6	20	X	X	X	X			X		
0.3	0.6	20	X		X					X	

**10 Hz

Audio and General Purpose Operational Amplifiers

Single Operational Amplifiers

Type	Description	Maximum Input Specifications @ 25°C			Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[2] Range	Available Packages				
		Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)				D	L	M	N	T
LM101A	General Purpose with Improved	2.0	10	75	1.0	0.5	M	X				X
LM301A	Input Characteristics	7.5	50	250	1.0	0.5	C				X	
RC741	General Purpose, Internal Comp	6.0	200	500	1.0	0.5	C	X			X	X
RC5534	High Performance, Low Noise	4.0	300	1500	10	13	C				X	
RM5534		2.0	200	800	10	13	M	X				X
RC5534A[3]		4.0	300	1500	10	13	C				X	
RM5534A[3]		2.0	200	800	10	13	M	X				X
LF156	JFET Input						M	X	X			X

Notes:
1. Gain bandwidth product for 5534/A series and closed loop bandwidth for OP series.
2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
3. RM/RC5534A guarantees maximum input noise specification.

Dual Operational Amplifiers

Type	Description	Maximum Input Specifications @ 25°C			Typ[1] Unity Gain BW (MHz)	Typ. Slew Rate (V/μS)	Temp[2] Range	Available Packages				
		Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)				D	L	M	N	T
LH2101A	High Performance	2	10	75		10		X				
RC747	Dual 741	6	200	500	1	0.5	C				X	
RM747		5	200	500	1	0.5	M	X				X
RC4558	Wideband 741	6	200	500	3	1	C			X	X	
RM4558		5	200	500	3	1	M	X				X
RC4559	High Performance	6	100	250	4 (3)	2 (1,5)	C			X	X	
RM4559		5	100	250	4 (3)	2 (1,5)	M	X				X
RC5532	High Performance, Low Noise	4	150	800	10	8	C				X	
RM5532		2	100	400	10	8	M	X				X
RC5532A[3]		4	150	800	10	8	C				X	
RM5532A[3]		2	100	400	10	8	M	X				X

Notes:
1. Gain bandwidth product for 5532A series.
2. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
3. RM/RC5532A guarantees maximum input noise specification.
( ) Denotes guaranteed specifications.

Package Codes:
D = Ceramic DIP
L = Leadless Chip Carrier
M = Plastic SOIC
N = Plastic DIP
T = Metal Can (TO-99)

Audio and General Purpose Operational Amplifiers

Quad Operational Amplifiers

Type	Description	Maximum Input Specifications @ 25°C			Typ Unity Gain BW	Typ. Slew Rate	Temp[1]	Available Packages				
		Offset Voltage (mV)	Offset Current (nA)	Bias Current (nA)	(MHz)	(V/μS)	Range	D	L	M	N	T
RM4741	741 General Purpose	3	30	200	3.5	1.6	M	X				
RC4741		5	50	300	3.5	1.6	C				X	
LM124	Single Supply	5	30	150	1	—	M	X				
LM148	Low Power 741	5	25	100	1	0.5	M	X				
LM324	Single Supply	7	50	250	1	—	C				X	
LM348	Low Power 741	6	50	200	1	0.5	C				X	
LM3900	Current Mode, Single Supply	—	—	200	2.5	+.5/-20	C				X	
RC3403A	Ground Sensing	6	50	500	1	1.2	C				X	
RC4136	741 General Purpose	6	200	500	3	1	C			X	X	
RM4136		4	150	400	3	1.5	M	X				
RC4156	High Performance	5	50	300	3.5 (2.8)	1.6 (1.3)	C			X	X	
RM4156		3	30	200	3.5 (2.8)	1.6 (1.3)	M	X				
RC4157	High Speed, Decompensated	5	50	300	19 (15)	8 (6.5)	C				X	
RM4157		3	30	200	19 (15)	8 (6.5)	M	X				

Notes:
1. Operating Temperature Range: M = -55°C to +125°C; C = 0°C to +70°C.
( ) Denotes guaranteed specification.

Comparators

Type	Description	Maximum Input Specifications @ 25°C			Voltage Gain (V/mV Typ)	Max Sat. Voltage	Output Leakage Current (nA Typ)	Available Packages				
		Offset Voltage (mV)	Bias Current (nA)	Offset Current (nA)				D	L	M	N	T
LH2111	Dual Precision Voltage	3.0	10	100	200	1.5V	0.2	X				
LM111	Low Input Current	3.0	10	100	200	1.5V	0.2	X	X			X
LM139	Quad Single Supply	5.0	100	25	200	0.40	0.1	X				
LM339	Quad Single Supply	5.0	250	50	200	0.40	0.1			X	X	
LP165	Programmable	3.0	50	20	500	0.40	2	X			X	
RC4805	Precision High Speed	0.6	1800	20	15	0.40	—				X	
RM4805		0.6	1800	150	20	0.40	—	X				X
RM4805A		0.25	1200	80	20	0.40	—	X				X
RC4805E		0.25	1200	80	20	0.40	—				X	

Voltage References

Device	Nominal Voltage Out	Typical Tempco (ppm/°C)	Temp. Range	Typical ΔV_{OUT} Over Temp. (%)	Typical Line Reg. (%/Volt)	Typical Load Reg. (%/mA)	Typical Load Current (mA)	Input Voltage Range (Voltage)
REF-01A	10.00	3.0	Mil	.06	.006	.005	15	12 to 40
REF-01	10.00	10.0	Mil	.18	.006	.006	15	12 to 40
REF-01C	10.00	20.0	Comm	.14	.009	.006	15	12 to 40
REF-01D	10.00	70.0	Comm	.49	.012	.009	15	12 to 40
REF-01E	10.00	3.0	Comm	.02	.006	.005	15	12 to 40
REF-01H	10.00	10.0	Comm	.07	.006	.006	15	12 to 40
REF-02A	5.00	3.0	Mil	.06	.006	.005	15	7 to 40
REF-02	5.00	10.0	Mil	.18	.006	.006	15	7 to 40
REF-02C	5.00	20.0	Comm	.14	.009	.006	15	7 to 40
REF-02D	5.00	70.0	Comm	.49	.012	.009	15	7 to 40
REF-02E	5.00	3.0	Comm	.02	.006	.005	15	7 to 40
REF-02H	5.00	10.0	Comm	.07	.006	.006	15	7 to 40

Other Standard Linear Products

D/A Converters
DAC-08, 8-Bit Current Output
DAC-10, 10-Bit Current Output
DAC-4881, 12-Bit Complete
DAC-4888, 8-Bit Complete
DAC-8565, 12-Bit with Reference

V/F Converters
RC4151, Basic 100 kHz
RC4152, Low-Drift 100 kHz
RC4153, Precision 250 kHz

Voltage Regulators
RC4190, Low Power Switcher
RC4191/92/93, Low Power Switcher
RC4194, Dual Tracking Linear
RC4195, Dual Tracking Linear
RC4292, Negative Input
RC4391, Inverting Switcher

Ground Fault Interrupters
LM1851, Industry Alternate Source
RC4143/4144, Standard GFI
RC4145, Low Power GFI

Special Functions
RC4200, Analog Multiplier
RC4444, Cross-Point Array
RC4447, Pin-Diode Driver
RM3182, ARINC Bus Driver
XR-2207, Voltage-Controlled Oscillator
XR-2211, FSK Demodulator

SECTION 3
QUALITY & RELIABILITY

Quality is the measure of a device's conformance to its specifications, and reliability is the measure of the device's performance over time. The approach to maintaining and improving them must be systematic, because every phase of the manufacturing process has an impact on the final product.

Reliability Concepts

Reliability is a measure of the life expectancy of a device, or to state it another way, the length of trouble-free performance that it can offer. There are various parameters of reliability, and these can be summarized by the curve shown in Figure 1.

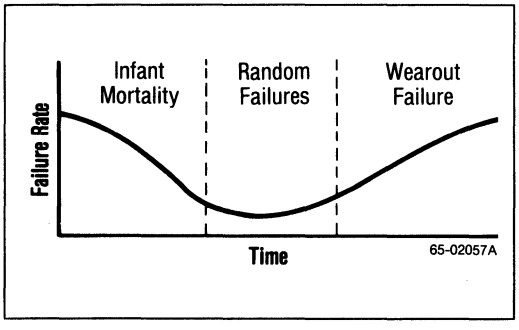


Figure 1. Failure vs. Time

As a device is manufactured, there are numerous random potential failure mechanisms built in. These potential failure mechanisms usually exhibit themselves under a relatively moderate stress level, and hence occur early in the life span of the device. This period is termed Infant Mortality. The period of early failures can be reduced through good manufacturing control and screening methods. The screening techniques detailed are typical of the types of stress tests to which a product lot is subjected in order to detect the failure modes and to eliminate the suspect devices from the production lot. The tests described in Tables 1, 2, 3, and 4 are designed to screen out infant mortality defects which normally arise from manufacturing processes.

The period of Random Failure represents the time when an occasional random failure mechanism can cause a device to fail. This period usually represents a long time with a very low device failure rate and is the major time frame of customer interest. The Wearout Failure period is the final period where the device literally wears out due to physical phenomenon that existed at the time of manufacture.

The infant mortality and random failures periods can be described through a series of mathematical equations and probability calculations. The probability of having a failure at a specific point in time can be expressed by the equation:

$$P_o = e^{-xt}$$

where:

x = the failure rate (failures per unit time)
t = time

During the infant mortality period, "x" is changing rapidly and does not become stable under the random failure period. The failure rate "x" is usually expressed in % failures per 1000 hours and is sometimes expressed as a mean time between failures (MTBF) through the expression:

$$MTBF = \frac{1}{\text{Failure Rate}}$$

Since the data for the failure rate calculations is derived from a sample of devices from a production lot, a confidence level number is usually stated for the failure rate. A 60% confidence level (CL) has become a common number. The confidence level is demonstrated by the distribution curve shown in Figure 2.

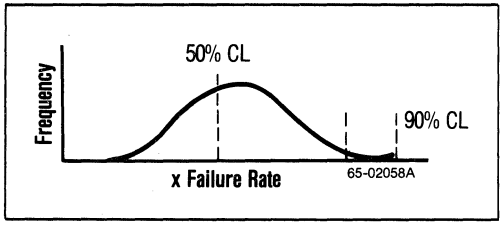


Figure 2. Frequency vs. Failure Rate

The failure rate "x" is calculated by using a Chi square (χ^2) distribution through the equation:

$$\chi = \frac{\chi^2(x.\ 2r+2)}{2nt}$$

where:

x = 100-%CL/100
r = number of rejects
n = total number of devices
t = time

The number of failures over a period of time (x) is critical in determining an accurate failure rate number. If only device failures at room or operating temperatures were counted, it would take a large number of failures over a long period of time to gather sufficient data. Therefore, accelerated test methods using elevated temperatures are used. Temperature will accelerate the failures in a device and the increase can be expressed in a form of the Arrhenius equation which states that the reaction rate increases exponentially with temperature.

$$R = R_o\, e^{\frac{-E}{kT}}$$

where:

R = reaction rate as a function of time and temperature
R_o = constant related to temperature
T = Kelvin temperature
E = activation energy (electron volts)

When this equation is plotted, as shown in Figures 3 and 4, it can be used to determine the failure rate at temperatures other than the test temperature of the device.

Reliability Program

The quality and reliability activity at Raytheon is a thorough and continuous activity. It starts with the initial design concepts and carries through to the finished product.

Reliability Engineering, working with the Design or Product Engineer, monitors the new device design or process through all stages of development and remains the full and final authority over the qualification status of all products. A facility will never ship a product to the customer

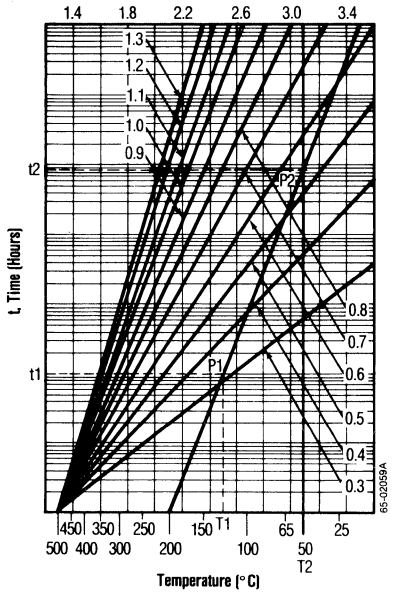


Figure 3. Normalized Time-Temperature Regressions for Various Activation Energy Values (1000/°K)

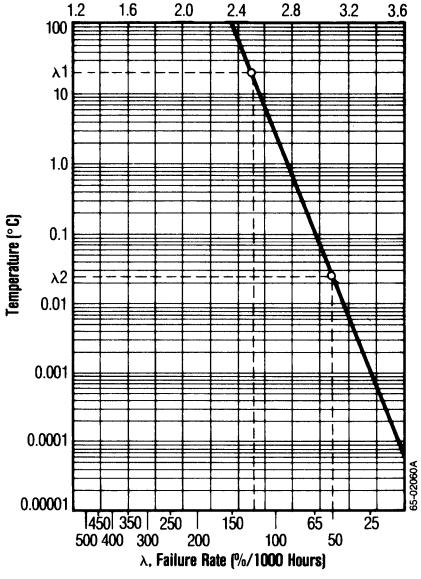


Figure 4. Failure Rate (1000/°K)

until it has been fully documented, released to manufacturing and formally approved by the Reliability Department.

Raytheon has established several RA Qualification plans which are used to approve a new device, process or manufacturing facility. Two of these plans are shown in Tables 5 and 6 for hermetic package devices and plastic package devices.

The Reliability Department continually monitors all product lines through product sampling, the Plastic Process Monitor and the QCI testing of JAN and other Hi-Rel products to evaluate failure modes and failure rates. The results from these tests are reviewed with Product and Production Engineering and any necessary corrective actions are taken.

Table I. Group A Electrical Tests for Class B Devices.[1]

Subgroups[2] Quality/Accept No. = 116/0 [3][4]
Subgroup 1 Static tests at 25°C
Subgroup 2 Static tests at maximum rated operating temperature
Subgroup 3 Static tests at minimum rated operating temperature
Subgroup 4 Dynamic tests at 25°C
Subgroup 5 Dynamic tests at maximum rated operating temperature
Subgroup 6 Dynamic tests at minimum rated operating temperature
Subgroup 7 Functional tests at 25°C
Subgroup 8A Functional tests at maximum rated operating temperatures
Subgroup 8B Functional tests at minimum rated operating temperatures
Subgroup 9 Switching tests at 25°C
Subgroup 10 Switching tests at maximum rated operating temperature
Subgroup 11 Switching tests at minimum rated operating temperature

(1) The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

(2) The applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in Table I.), or sets of subgroups.

(3) The sample plan (quantity and accept number) for each test shall be 116/0.

(4) If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

Table 2 Group B Tests for Class B [1][2]

Test	Mil-Std-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 2[3] a. Resistance to solvents	2015		4(0)
Subgroup 3 a. Solderability[4]	2022 or 2003	Soldering temperature of 245 ±5°C	10
Subgroup 4 a. Internal visual and mechanical	2014		1 device (no failures)
Subgroup 5 a. Bond strength[5] 1. Thermocompression 2. Ultrasonic or wedge 3. Flip-chip 4. Beam Lead	2011	 1. Test condition C or D 2. Test condition C or D 3. Test condition F 4. Test condition H	

(1) Post burn-in electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.

(2) Subgroups 1, 6, 7, and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.

(3) Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.

(4) All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

(5) Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum n umber of 4 devices, and for condition F or H is the number of dice (not bonds) (see Method 2011).

Table 3. Group C (Die-Related Tests — For Class B only)

Test		Mil-Std-883	Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 1 a. Steady-state life test b. End-point electrical parameters	1005	Test condition to be specified (1,000 hours at 125°C) As specified in the applicable device specification	5

Table 4. Group D (Package Related Tests)

Test	Mil-Std-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 1 (1)			
a. Physical dimensions	2016		15
Subgroup 2 (1)			
a. Lead integrity (2)	2004	Test condition B_2 (lead fatigue)	15
b. Seal (3)			
1. Fine	1014	As applicable	
2. Gross			
Subgroup 3 (4)			
a. Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	15
b. Temperature cycling	1010	Test condition C, 100 cycles minimum	
c. Moisture resistance (5)	1004		
d. Seal	1014	As applicable	
1. Fine			
2. Gross			
e. Visual examination		In accordance with visual criteria of Method 1004 and 1010	
f. End-point electrical parameters (6)		As specified in the applicable device specification	
Subgroup 4 (4)			
a. Mechanical shock	2002	Test condition B minimum	15
b. Vibration, variable frequency	2007	Test condition A minimum	
c. Constant acceleration	2001	Test condition E minimum (see 3), Y_1 orientation only	
d. Seal	1014	As applicable	
1. Fine			
2. Gross			
e. Visual examination	(note 7)		
f. End-point electrical parameters		As specified in the applicable device specification	
Subgroup 5 (1)			
a. Salt atmosphere (5)	1009	Test condition A minimum	15
b. Seal	1014	As applicable	
1. Fine			
2. Gross			
c. Visual examination		In accordance with visual criteria of Method 1009	

Table 4. Group D (Package Related Tests) (Continued)

Test	Mil-Std-883		Quantity/ (Accept No.) or LTPD
	Method	Condition	
Subgroup 6 [1`] a. Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3(0) or 5(1) (note 8)
Subgroup 7 [1] a. Adhesion of lead finish [,9,10]	2025		15
Subgroup 8 a. Lid torque [1]	2024		5(0)

(1) Electrical reject devices from that same inspection lot may be used for samples.

(2) For leadless chip carrier packaged only, use test condition D. For leaded chip carrier packages, use condition B1. For pin grid array and other rigid leads use Method 2038.

(3) Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

(4) Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

(5) Lead bend stress initial conditioning is not required for leadless chip carrier packages.

(6) End-point electrical parameters are performed after moisture resistance and prior to seal test.

(7) Visual examination shall be in accordance with Method 1010 or 1011.

(8) Test three devices; if one fails, test two additional devices with no failures. At the manufacturers option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot.

(9) The adhesion of lead finish test shall not apply fo leadless chip carrier packages.

(10) LTPD based on number of leads.

Table 5. Qual Plan for Hermetic Packages Devices [1][2][3]

Test	Conditions Per Mil-Std-883	Quantity	Accept No.
Group B			
Subgroup 3		15	0
Solderability	245 ±5°C		
Subgroup 4		1	0
Internal Visual			
Subgroup 5		15	0
Bond Strength	Condition C and record bond pull strength		
Subgroup 7		77	1
F&G Leak			
Group C			
Subgroup 1		77	1
Operational Life (168, 250, 500, 1000, 2000)	168-hour point will be used to screen out the infant mortality failure. The sample size after the 168-hour point will be 77.		
Electrical Test (25°C dc) (2 date codes, 77 samples each)			
Subgroup 2		25	1
Temperature Cycle	Condition B, 15 cycles		
Constant Acceleration	Condition C, 100 cycles		
Moisture Resistance	10 Day		
F&G Leak			
Visual			
Electrical Test 25°C			
Group D			
Subgroup 2		25	1
Lead Integrity	Condition B_2		
F&G Leak			
Lid Torque			
Subgroup 4		25	1
Mechanical Shock	Condition B		
Vibration	Condition A		
Constant Acceleration	Condition B Min.		
F&G Leak			
Visual Examination			
Electrical Test 25°C			

(1) The above group B, C, D are run completely, if the product (package and die) has no history.

(2) If the package is pre-qualified, then only Group C, Subgroups 1 and 2, and Group D, Subgroup 4 are conducted.

(3) If the product is not JAN or 883 compliant, then 168-hour pre-burn in is not performed to screen out infant mortality prior to Group C test.

Table 6. Qualification Plan for Plastic Package Devices

Test	Test Conditions	Purpose of Test	Sample Size	Accept No.
Operating Life	Temperature 125°C Time 2000 hrs. Electrical Test at 168 hrs., 500 hrs., 1000 hrs., 2000 hrs. Bias — per spec requirements	Accelerated Life	100	1
	NOTE: Samples from this test will continue for 2000 and 3000 hrs. evaluation.			
Steam Pressure	Pressure 15 lbs. Temperature 120°C Time 96 hrs. Electrical Test at 48 hrs., (no metal deterioration), 96 hrs., 144 hrs., 250 hrs., 500 hrs.	Package integrity and moisture resistance	55	1
	NOTE: Bake and retest electrical rejects for engineering evaluation and data.			
85°C/85% RH	Temperature 85°C Humidity 85% Time 250 hrs. (no metal deterioration) Electrical Test at 160 hrs., 250 hrs., 500 hrs., 1000 hrs., 2000 hrs.	Accelerated life corrosion resistance	100	1
	NOTE: Bake and retest electrical rejects for engineering evaluation and data.			
Storage Life	Temperature 150°C Time 144 hrs. Bias — None Electrical Test at 144 hrs., 500 hrs.	Determine the effect of high temperature storage	32	0
Temperature Cycle	Temperature -55°C to +85°C No. Cycles 100 Electrical Test 25°C, 70°C	Determine the resistance to high and low temperatures	32	0
Moisture (10 Day)	Temperature -10°C to +65°C Humidify 90% RH Time 240 hrs. Electrical Test at 240 hrs. Visual Inspection of Leads	Package integrity to moisture, lead corrosion, etc.	32	0
Solderability	Per 883, Method 2003	To determine the solderability of the lead finish	15	0
Lead Fatigue	Per 883, Method 2004 Condition B	To determine the physical resistance to lead bending fatigue	15	0
External Visual	10-30X Magnification	To evaluate pnysical construction and processing results to package and lead frame	15	0

*2 date codes of 50 each

Lab Facilities

Raytheon maintains a fully equipped laboratory to conduct its reliability, failure analysis, and environmental testing. The typical types of tests that are performed by this facility include:

- QCI Groups A, B, C and D environment re quirements
- Destructive Physical Aanalysis
- SEM Analysis
- Microprobe Analysis
- X-ray Dispersion Analysis
- Biased 85/85 and Steam Pressure Pot (PCT)
- Highly Accelerated Stress Testing (HAST)
- Reliability Analysis
- Electrical DC and Functional Testing

Plastic Package Device Monitor

Raytheon is a major supplier of standard and ASIC products in plastic packages. The linear devices are available in a variety of plastic packages such as DIPs, SOICs, and LCCs. Significant investments have been made in both the technology and manufacture of high-reliability, low-stress plastic encapsulated packages.

In addition to quality control check point inspection at every assembly step, reliability process monitoring (see Table 7) is performed.

The autoclave (steam pressure) test determines the package's moisture resistance in the shortest possible time, allowing immediate corrective action where necessary, thus ensuring the long-term reliability of the products.

All products are100% electrically tested and visually screened followed by sample testing for electrical, visual and mechanical defects to determine the outgoing PPM defect rate. With a quality goal of 200 ppm or less, Raytheon's devices have failure rates well below the industry standards.

Table 7. Typical Plastic Process Monitor Tests

Test	Purpose of Test
Autoclave (steam pressure)	To evaluate the resistance of moisture penetration of the package and the effects of moisture on the chip under accelerated conditions of 15 pounds of steam pressure at 120°C.
Biased 85°C/85% RH	To evaluate the operational life and resistance to moisture penetration of the chip and the plastic package under the accelerated conditions of 85°C and 85% relative humidity.
Operating Life	To evaluate the operational field life of the device under accelerated conditions of 125°C.
Resistance to Solvents	To determine that the brand markings will not become illegible on the package parts when subjected to the solvents and test per Mil-Std-883C, Method 2015.
Solderability	Per Method 2004 of Mil-Std-883.
External Visual	To determine the physical construction and processing results to the package and lead frame at 30X magnification.
Lead Fatigue	To determine the physical resistance to lead bending fatigue per Condition B, Method 2004, of Mil-Std-883.
Thermal Shock	To determine that the device can survive exposure to rapid changes in temperature from -55°C to +125°C per Condition B of Method 1011 of Mil-Std-883.

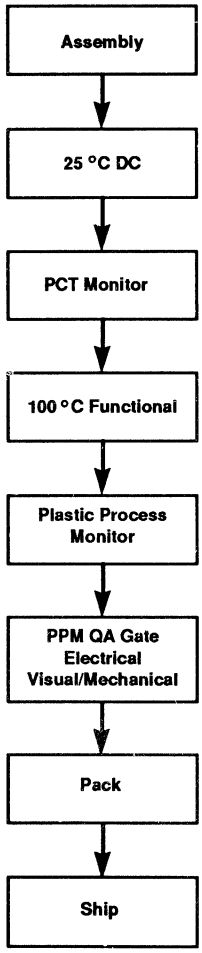


Figure 5. Linear Plastic Flow Chart

Major Programs

Raytheon is involved in major programs which require and support a high level of quality and reliability expertise in the design, manufacture and control of our products.

The commercial programs address such market segments as computers and automotive.

These markets are a driving force within Raytheon's commercial product quality and reliability controls.

The most significant military program is JAN 38510 which requires a Defense Electronics Supply Center (DESC) certification of our fabrication and manufacturing lines. The JAN military specifications and Mil-I-45208 form the foundation of our QA system, thereby benefitting all products — JAN, 883 compliant,Source Control Drawings (SCD), and commercial.

Additional key military oriented programs include Raytheon's 883 compliant, DESC Standard Military Drawings (SMD) and SCDs.

An extensive statistical process control program has been initiated which includes wafer fabrication processing, quality assurance monitors, assembly monitors, environmental screening and electrical testing.

Internal Audit Program

Raytheon has an internal audit program which requires the auditing of all product processing and control systems. This audit verifies conformance to manufacturing and quality procedures identifying areas needing improvement and enhancement.

Process Monitors

Extensive process monitors in fab, assembly and electrical test are a critical part of Raytheon's quality program.

Product Improvement Program (PPM)

The product improvement committee oversees and documents status of the Product Improvement Program.

Raytheon's acceptance goal is zero defects. In order to meet this goal, the product improve-

ment program evaluates visual, mechanical and electrical properties, and takes the necessary corrective action to reduce the defect density of the outgoing product.

Reliability Monitor

The Reliability Monitor Program monitors, on a continuing basis, the reliability of all IC products in hermetic and plastic packages. (For plastic package reliability monitor refer to Table 7.) This program requires that periodically several different part types from each microcircuit technology group as detailed in Appendix E of Mil-M-38510 be evaluated to the Mil-Std-883 Test Method 5005 Groups A, B, C and D test requirements. The data generated from this program provides a basic library of reliability information on many product types and can be used to provide Quality Conformance Inspection (QCI) data to meet a customers specific group test data requirements.

Military Programs

JAN-MIL-M-38510

Raytheon's foremost commitment is to the JAN MIL-M-38510 program which is administered by the Defense Electronics Supply Center (DESC) and the Defense Logistics Agency (DLA) of the Department of Defense. We maintain DESC certified wafer fabrication, assembly and test facilities which allow us to provide an extensive number of JAN QPL device types.

The JAN 38510 program is designed to provide a consistently high reliability hermetic product manufactured to a standard process flow and quality/reliability program as defined in Mil-M-38510, Mil-Std-976 and Mil-Std-883 and the resulting baselines.

A JAN device is identified and branded with a unique part number as shown in Figure 7 and Table 8. The device is also branded with our manufacturers designating symbol (CRP or RP), logo (RAY or R), the sealing cycle date code, country of origin, a two-digit fab quarter code (indicating year and quarter in which die fabrication was completed) and the applicable electrostatic discharge sensitivity identifier.

A current listing of Raytheon's JAN 38510 QPL devices may be obtained by contacting the nearest Raytheon Field Sales Office.

883 Compliant

The 883 compliant program offers hermetic products assembled and tested to the requirements of paragraph 1.2.1 of Mil-Std-883 for class B devices. With Raytheon as the qualifying activity and off-shore assembly permissible these devices are as close as one can get to JAN 38510 reliability using a standard process flow (see Figure 6).

Raytheon's 883 compliant program is complemented by our active participation in DESC's Standard Military Drawing (SMD) program.

A current listing of our 883 compliant devices which includes those DESC SMDs for which Raytheon is an approved source of supply may be obtained by contacting the nearest Raytheon Field Sale Office.

Lead Finish

Raytheon offers three lead finishes — solder dipped, gold and matte tin plate (non-JAN only). The preferred and recommended lead finish is solder which is tin plated prior to dipping. The gold finish is applied over nickel plate.

Raytheon is offering a solder lead finish that will meet the solderability requirements of MIL-M-38510, WS6536E and DOD-STD-2000. Our customers must state in either their purchase order or SCD which solderability specification is applicable.

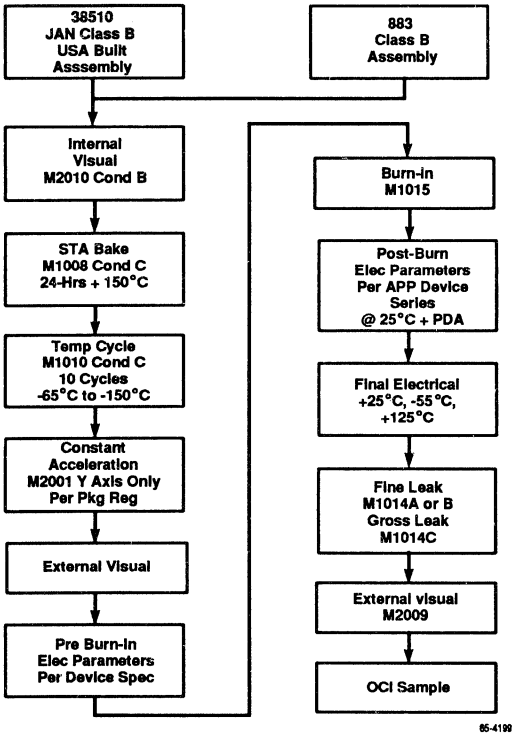


Figure 6. Screening for JAN and 883 Compliant Devices

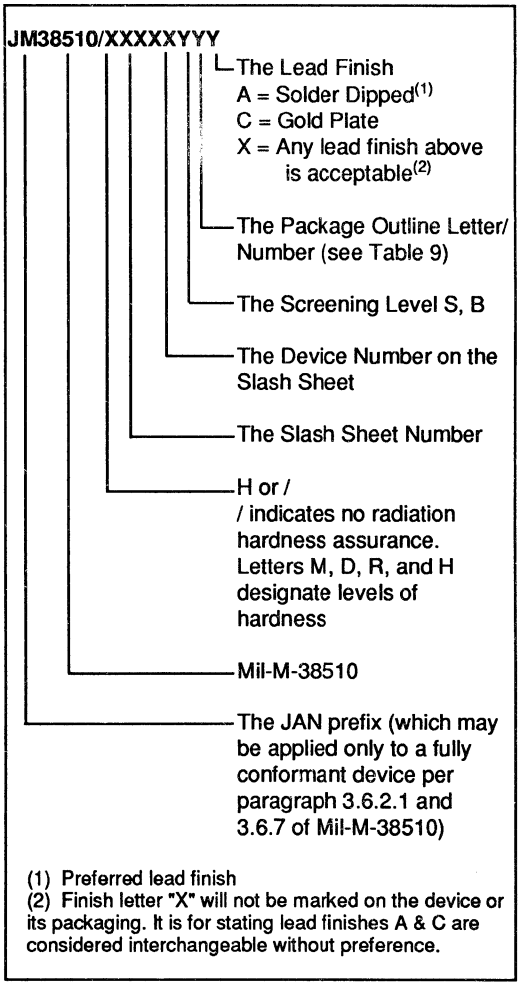


Figure 7. Mil-M-38510 Part Marking

Table 8. JAN Package Codes

38510 Outline Letter/ Number	38510 Type Designation	Description
A	F-1	14-lead, 1/4 x 1/4 Cerpak
B	F-3	14-lead, 3/16 x 1/4 Cerpak
C	D-1	14-lead, 1/4 x 3/4 Cerdip
D*	F-2	14-lead, 1/4 x 3/8 Cerpak
E	D-2	16-lead, 1/4 x 7/8 Cerdip
F	F-5	16-lead, 1/4 x 7/8 Cerpak
G	A-1	8-lead, TO-99 can
H	F-4	10-lead, 1/4 x 1/4 Cerpak
I	A-2	10-lead, TO-100 can
J	D-3	24-lead, 1/2 x 1-1/4 Cerdip
K	F-6	24-lead, 3/8 x 5/8 Flatpak
L	D-9	24-lead, 1/4 x 1-1/4 Cerdip
M*	A-3	12-lead, TO-101 can
P	D-4	8-lead, 1/4 x 3/8 Cerdip
Q	D-5	40-lead, 2 x 5/8 DIP
R	D-8	20-lead, 1/4 x 1-1/16 Sidebraze DIP
S	F-9	20-lead, 1/4 x 1/2 Cerpak
V	D-6	18-lead, 1/4 x 5/16 Cerdip
W*	D-7	22-lead, 3/8 x 5/16 DIP
2	C-2	20-terminal, 3/8 x 3/8 Chip carrier
3	C-4	28-terminal, 1/2 x 1/2 Chip carrier

*Consult your nearest Field Sales Office

SECTION 4

OPERATIONAL AMPLIFIERS

DEFINITIONS

Average Input Bias Current Drift (TC_{IB})
The ratio of change in input bias current to a change in ambient temperature, expressed in nanoamps per degree C (nA/° C).

$$TC_{IB} = \frac{I_B @ T_{(1)} - I_B @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Average Input Offset Current Drift (TC_{IOS})
The ratio of change in input offset current to a change in ambient temperature, expressed in nanoamps per degree C (nA/° C).

$$TC_{IOS} = \frac{I_{OS} @ T_{(1)} - I_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Average Input Offset Voltage Drift (TC_{VOS})
The ratio of change in input offset voltage to a change in ambient temperature, expressed in microvolts per degree C (μV/° C).

$$TC_{VOS} = \frac{V_{OS} @ T_{(1)} - V_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Channel Separation
The ratio of output voltage of an amplifier to the output voltage of an adjacent amplifier whose gain is 100, and whose inputs are grounded, expressed in decibels (dB). Channel separation is measured at the outputs of adjacent amplifiers:

$$\text{Channel Separation} = 20LOG_{10}\left(\frac{100V_{O(1)}}{V_{O(2)}}\right)$$

Where $V_{O(1)}$ and $V_{O(2)}$ are the independent and dependent amplifier output voltages.

Common Mode Rejection Ratio (CMRR)
The ratio of change of input common mode voltage (both inputs swing together over a specified voltage range) to a change in input offset voltage, expressed in decibels (dB).

$$CMRR = 20LOG_{10}\left(\frac{V_{IN(1)} - V_{IN(2)}}{V_{OS} @ V_{IN(1)} - V_{OS} @ V_{IN(2)}}\right)$$

Where $V_{IN(1)}$ and $V_{IN(2)}$ are the upper and lower limits of the input common mode voltage range.

Distortion (THD)
The large signal harmonic distortion between input and output under closed loop conditions, expressed in percent at a specified frequency.

Gain Bandwidth Product (GBW)
The frequency at which the open loop gain equals unity, expressed in Hertz (Hz).

DEFINITIONS (Continued)

Input Bias Current (I_B)
The average of the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Noise Current
The peak-to-peak noise current within a specified frequency band, expressed in nanoamps or picoamps (nA or pA).

Input Noise Current Density (I_N)
The rms noise current in a 1 Hertz band centered on a specified frequency, expressed in picoamps per root Hertz ($pA/\sqrt{Hz}$).

Input Noise Voltage
The peak-to-peak noise voltage within a specified frequency band, expressed in nanovolts or microvolts (nV or μV).

Input Noise Voltage Density (e_n)
The rms noise voltage in a 1 Hertz band centered on a specified frequency, expressed in nanovolts per root Hertz ($nV/\sqrt{Hz}$).

Input Offset Current (I_{OS})
The difference between the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Offset Voltage (V_{OS})
The voltage that must be applied between the two inputs to obtain an output voltage in the center of the output swing range, expressed in millivolts or microvolts (mV or μV).

Input Resistance (Common Mode)
The ratio of input voltage change to the resulting change in input bias current, expressed in megaohms or gigaohms (MΩ or GΩ).

$$\text{Common mode } R_{IN} = \frac{V_{(1)} - V_{(2)}}{I_B @ V_{(1)} - I_B @ V_{(2)}}$$

Where $V_{(1)}$ and $V_{(2)}$ are the upper and lower limits of the input voltage range.

Input Resistance (Differential Mode)
The ratio of small signal change in input offset voltage to a change in input current at either input terminal with the other grounded, expressed in megaohms (MΩ).

Input Voltage Range
The range of voltages at the inputs over which the amplifier operates within its common mode rejection ratio specification, expressed in volts (V).

Large Signal Voltage Gain (A_V)
The ratio of a specified output voltage change to the change in input offset voltage required to effect the change under open loop conditions, expressed in volts per millivolt (V/mV).

$$A_V = \frac{V_{O(1)} - V_{O(2)}}{V_{OS(1)} - V_{OS(2)}}$$

Where $V_{O(1)}$ and $V_{O(2)}$ are the specified upper and lower voltage limits for the change at the output.

Long Term Input Offset Voltage Stability
The averaged trend line of V_{OS} vs. time over extended periods after the first 30 days of operation, expressed in microvolts per month ($\mu V/Mo$).

Offset Adjustment Range
The change in V_{OS} that can be produced using the specified external offset adjustment circuit, expressed in millivolts (mV).

Open Loop Output Resistance (R_O)
The resistance seen looking into the output with the output at the center of its swing, under small signal conditions, expressed in ohms (Ω).

Output Sink Current
The current flowing into the output for a specified set of input and output conditions, measured in milliamps (mA).

DEFINITIONS (Continued)

Output Source Current
The current flowing out of the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Voltage Swing
The peak output change, referred to ground, that can be obtained for a specified load resistance, expressed in volts (V).

Overshoot
The positive or negative going excursion that exceeds the final settled condition at the output of a closed loop unity gain amplifier, expressed as a percentage of the output step.

Phase Margin
The difference between the amplifier phase shift and 180° at the frequency where the open loop gain equals unity, expressed in degrees.

$$\text{Phase margin} = 180° - \phi$$

Where ϕ equals the input-output phase shift at $A_V = 1$.

Power Bandwidth
The maximum frequency at which a specified peak voltage sine wave may be obtained, measured in Hertz (Hz).

Power Consumption
The DC power required to operate the amplifier with the output at the center of its swing and zero load current, expressed in milliwatts (mW).

Power Supply Rejection Ratio (PSRR)
The ratio of change of supply voltage to a change in input offset voltage, expressed in decibels (dB).

$$PSRR = 20LOG_{10}\left(\frac{V_{S(1)} - V_{S(2)}}{V_{OS} @ V_{S(1)} - V_{OS} @ V_{S(2)}}\right)$$

Where $V_{S(1)}$ and $V_{S(2)}$ are the upper and lower limits of the specified change of supply voltage.

Rise Time
The time required for an output voltage step to change from 10% to 90% of its final value, expressed in nanoseconds (nS).

Short Circuit Current
The maximum output current available from the amplifier with the output shorted to ground, expressed in milliamps (mA).

Slew Rate
The average rate of change of output voltage under large signal overdriven conditions, expressed in volts per microsecond (V/μS).

Supply Current (I_S)
The current required from the power supply to operate the amplifier under quiescent no load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which the amplifier will operate, expressed in volts (V).

Unity Gain Bandwidth
The frequency at which the small signal voltage gain is 3dB below unity when operated as a closed loop unity gain follower, expressed in Hertz (Hz).

RC4077 Series Precision Operational Amplifiers

Features

- Ultra-low V_{os} — 10 μV max
- Ultra low V_{os} drift – 0.1 μV/°C max (B grade only)
- Outstanding gain linearity
- High gain — 5000 V/mV min
- High CMRR — 120 dB min
- High PSRR – 110 dB min
- Low noise — 0.3 μV_{p-p} (0.1 to 10 Hz)
- Low input bias current — 2.0 nA max
- Low power consumption — 50 mW max
- Replaces OP-07, OP-77, 725, 108, 741 types

Description

The RC4077 is an advanced, ultra-high performance precision bipolar operational amplifier.

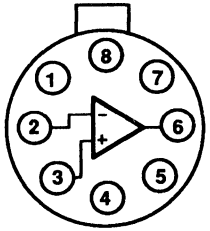
Its high precision performance results from two innovative and unconventional manufacturing steps, plus careful circuit layout and design. Thin-film resistor technology and a novel method of digital offset nulling are the key steps. A low ±10 μV offset voltage is delivered via a patented, proprietary V_{os} nulling adjustment. Devices retain this low offset through the stability and accuracy of Si-Cr thin-film resistors.For applications needing the lowest input offset voltage drift with temperature (TC V_{os}), the "B" grade has a worst-case specification of just 0.1 μV/°C.

Designed to upgrade OP-07 and other low-I_B bipolar precision types, the RC4077 has a well-balanced, mutually supporting set of input specifications. Low V_{os}, low I_B, and high open-loop gain combine to raise the performance level of many instrumentation, low-level signal conditioning, and data conversion applications. PSRR, CMRR, drift, and noise levels also support high precision operation.

The RC4077 is available in LCC, SO-8 (small outline), TO-99 can, plastic mini-DIP and ceramic mini-DIP packages, and can be ordered with Mil-Std-883 Level B processing.

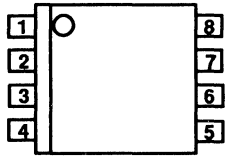
Connection Information

8-Lead TO-99 Metal Can
(Top View)



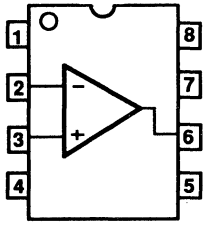
65-03205A

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

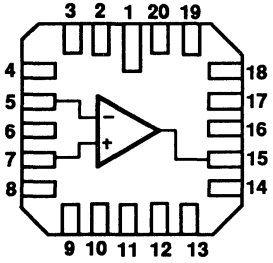
8-Lead Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

20-Pad LCC
(Top View)



65-02657A

Pin	Function
2	V_{OS} Trim
5	-Input
7	+Input
10	$-V_S$
15	Output
17	$+V_S$
20	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
RC4077AN	N	0°C to +70°C
RC4077EN	N	0°C to +70°C
RC4077FN	N	0°C to +70°C
RC4077EM	M	0°C to +70°C
RC4077FM	M	0°C to +70°C
RV4077ET	T	-25°C to +85°C
RV4077FT	T	-25°C to +85°C
RV4077ED	D	-25°C to +85°C
RV4077FD	D	-25°C to +85°C
RM4077AT	T	-55°C to +125°C
RM4077AT/883B	T	-55°C to +125°C
RM4077AD	D	-55°C to +125°C
RM4077AD/883B	D	-55°C to +125°C
RM4077AL/883B	L	-55°C to +125°C
RM4077BT	T	-55°C to +125°C
RM4077BT/883B	T	-55°C to +125°C
RM4077BD	D	-55°C to +125°C
RM4077BD/883B	D	-55°C to +125°C
RM4077BL/883B	L	-55°C to +125°C

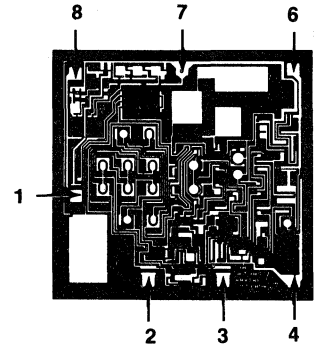
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4077A ..... -55°C to +125°C
RV4077A,E,F (Hermetic) ..... -25°C to +85°C
RC4077A,E,F (Plastic) ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8, 10 sec) ..... +260°C
(DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



Die Size: 75 x 78 mils
Min Pad Dimensions: 4 x 4 mils
65-03218A

Thermal Characteristics

	20-Pad LCC	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Small Outline	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	175°C	125°C	125°C
Max. P_D T_A <50°C	925 mW	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	37°C/W	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	105°C/W	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	7.0 mW/°C	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4077A/B/E			4077F			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]	RC/RM4077A RM4077B RC4077E		4.0 7.0 15	10 15 25		20	60	µV
Long Term V_{OS} Stability[1]			0.2			0.4		µV/Mo
Input Offset Current			0.1	1.5		0.1	2.8	nA
Input Bias Current			±0.3	±2.0		±1.0	±2.8	nA
Input Noise Voltage[5]	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.65	μV_{p-p}
Input Noise Voltage Density[5]	F_O = 10 Hz		10.3	18		10.3	20	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10	13		10	13.5	
	F_O = 1000 Hz		9.6	11		9.6	11.5	
Input Noise Current[5]	0.1 Hz to 10 Hz		14	30		14	35	pA_{p-p}
Input Noise Current Density[5]	F_O = 10 Hz		0.32	0.8		0.32	0.9	$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14	0.23		0.14	0.27	
	F_O = 1000 Hz		0.12	0.17		0.12	0.18	
Input Resistance (Diff Mode)[2]		30	80		20	60		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range[4]		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	120	140		116	130		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±8.0V	110	125		110	125		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	5000	12,000		2000	8000		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±13	±13.5		±13	±13.5		V
	$R_L \geq 2$ kΩ	±12.5	±13		±12.5	±13		
	$R_L \geq 1$ kΩ	±12	±12.5		±12	±12.5		
Slew Rate	$R_L \geq 2$ kΩ	0.1	0.3		0.1	0.3		V/µS
Closed Loop Bandwidth[2]	A_{VCL} = +1.0	0.4	0.8		0.4	0.8		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		35	50		35	50	mW
	V_S = ±3.0V, R_L = ∞		3.5	4.5		3.5	4.5	mW

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The RC/RM4077A/RM4077B grades are tested fully warmed up.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
5. Sample tested.

Electrical Characteristics (V_S = ±15V, -25°C ≤ T_A ≤ +85°C for hermetic packages, 0°C ≤ T_A ≤ +70°C for plastic packages unless otherwise noted)

Parameters	Test Conditions	4077A/E			4077F			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	RC4077A		7.0	24				µV
	RC4077EN,EM		10	40				
	RC4077FN,FM					25	90	
	RV4077ET,ED		10	45				
	RV4077FT,FD					30	100	
Average Input Offset Voltage Drift[1]	RC4077A/E		0.1	0.3		0.2	0.6	µV/°C
Input Offset Current			0.8	2.2		1.0	4.5	nA
Average Input Offset Current Drift[2]			±5.0	±40		±5.0	±85	pA/°C
Input Bias Current			±2.4	±4.0		±2.4	±6.0	nA
Average Input Bias Current Drift[2]			±8.0	±40		±15	±60	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	120	130		110	120		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	110	115		106	115		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	2000	6000		1000	4000		V/mV
Maximum Output Voltage Swing	$R_L \geq 2$ kΩ	±12	±13		±12	±13		V
Power Consumption	$R_L = \infty$		40	60		40	60	mW

Notes:
1. 100% tested for Grade A/E, sample tested for Grade F.
2. Sample tested.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	RM4077A/B			Units
		Min	Typ	Max	
Input Offset Voltage	RM4077A RM4077B		20 10	40 25	µV
Average Input Offset Voltage Drift[1]	RM4077A RM4077B		0.1 0.05	0.3 0.1	µV/°C
Input Offset Current			0.8	2.2	nA
Average Input Offset Current Drift[2]			±0.5	±25	pA/°C
Input Bias Current			±2.4	±4.0	nA
Average Input Bias Current Drift[2]			±0.8	±25	pA/°C
Input Voltage Range		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	120	130		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	110	115		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	2000	6000		V/mV
Maximum Output Voltage Swing	$R_L \geq 2$ kΩ	±12	±13		V
Power Consumption	$R_L = \infty$		40	60	mW

Notes:
1. 100% tested for Grade A/E/B, sample tested for Grade F.
2. Sample tested.

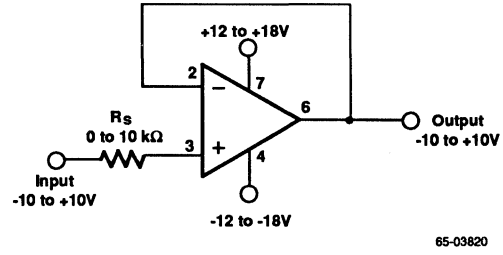
Offset Voltage Adjustment

The input offset voltage of the RC4077, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10K or 20K potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) µV/°C, e.g., if V_{OS} is adjusted to 300 µV, the change in drift will be 1 µV/°C. The adjustment range with a 10K or 20K potentiometer is approximately 4.0 mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example on the next page has an approximate null range of ±100 µV.

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

RC4077 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The RC4077 can also be used in 741 applications provided that the nulling circuitry is removed.

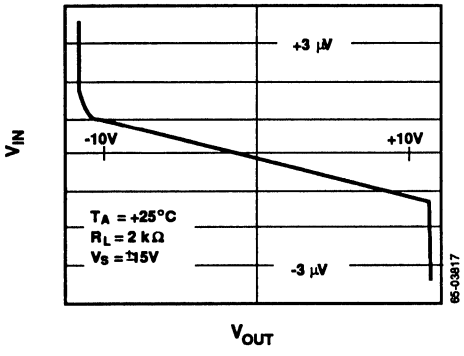
The voltage follower is an ideal example illustrating the overall excellence of the RC4077. The contributing error terms are due to offset voltage, input bias current, voltage gain, common-mode and power-supply rejections. Worst-case summation of guaranteed specifications is tabulated below.



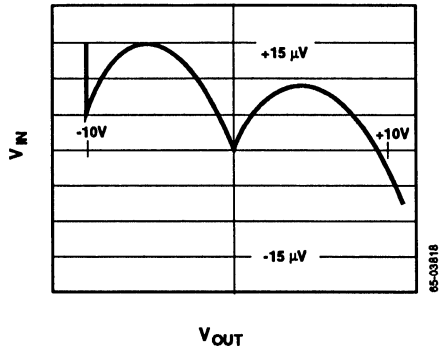
Large Signal Voltage Follower With 0.00063% Worst-Case Accuracy Error

Output Accuracy

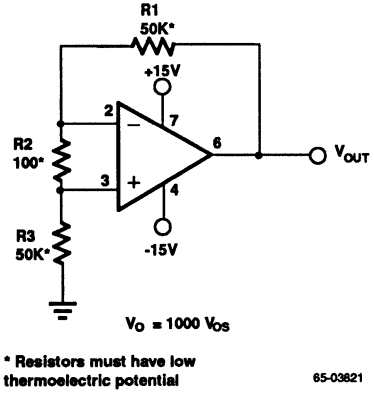
Error	RM4077A 25°C Max (µV)	RV4077F 25°C Max (µV)	RM4077A -55 to +125°C Max (µV)	RV4077F -25 to +85°C Max (µV)
Offset Voltage	10	60	40	100
Bias Current	15	28	40	60
CMRR	20	32	20	60
PSRR	18	18	18	30
Voltage Gain	7	8	8	20
Worst Case Sum	70	146	126	270
Percent of Full Scale (= 20V)	.00035%	.00073%	.00063%	.0013%



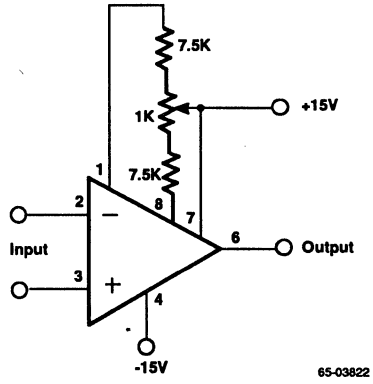
RC4077 Open-Loop Gain Linearity



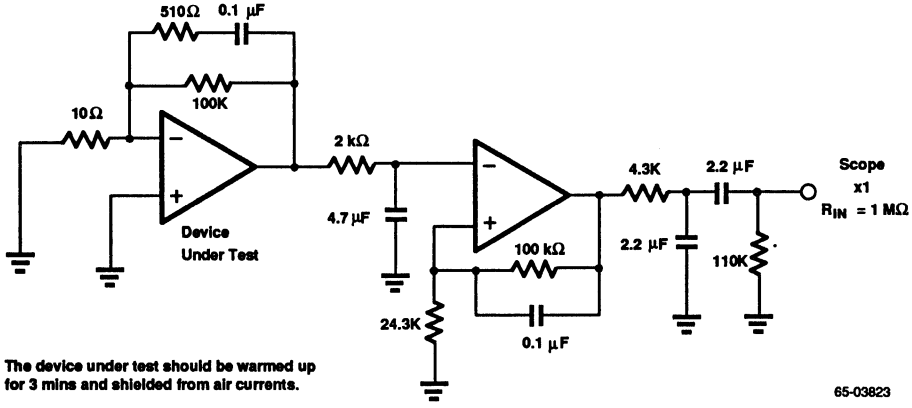
Typical Precision Op Amp Gain Linearity



Test Circuit for Offset Voltage and Its Drift With Temperature

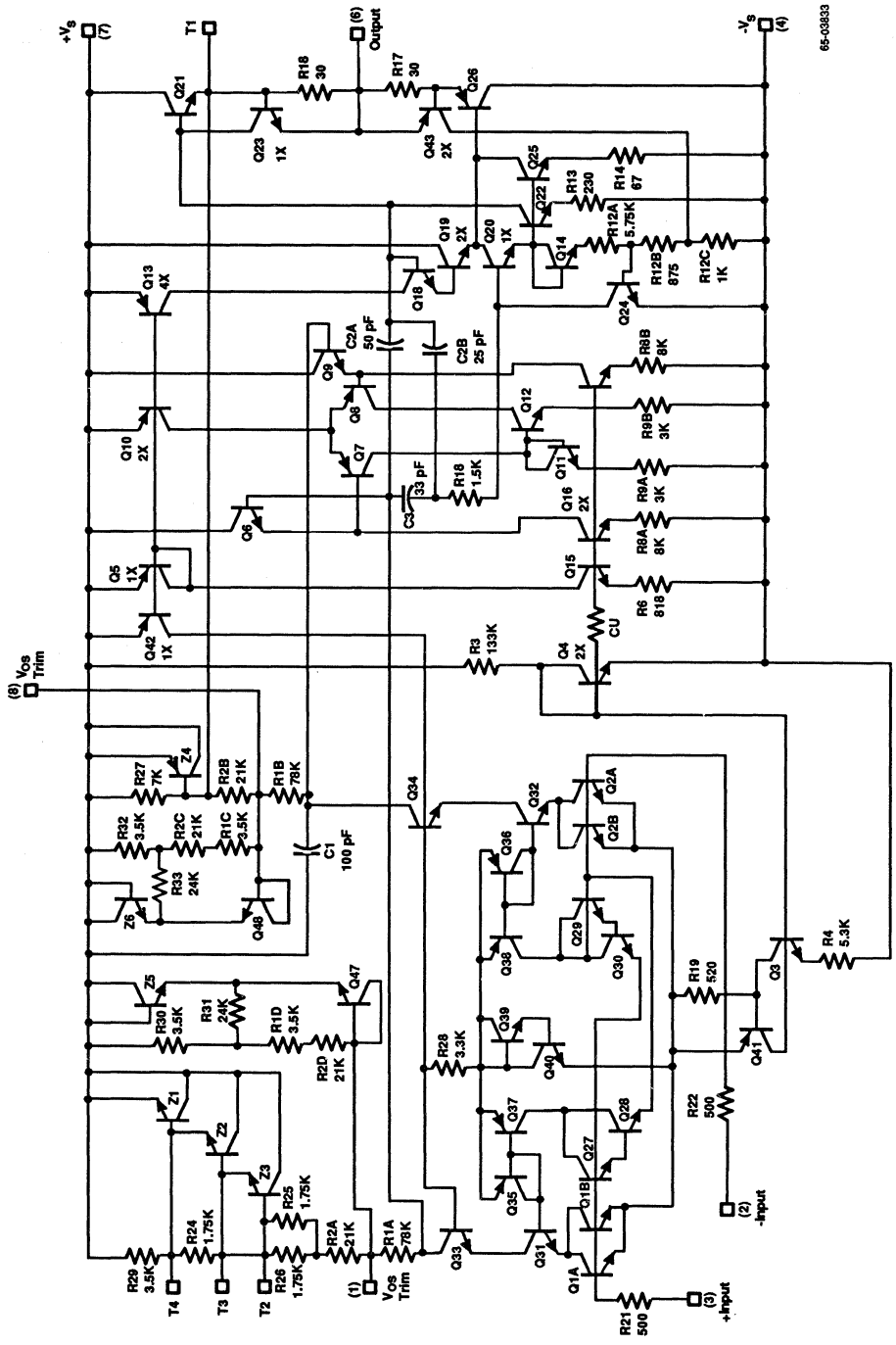


Improved Sensitivity Adjustment



0.1 Hz to 10 Hz Noise Test Circuit (peak-to-peak noise measured in 10 -sec intervals)

Schematic Diagram



RC4207 Precision Monolithic Dual Operational Amplifier

Features

- Low noise 0.1 Hz to 10 Hz — 0.35 μV_{p-p}
- Ultra-low V_{OS} — 75 μV max
- Ultra-low V_{OS} drift — 1.3 μV/°C max
- Long term stability — 0.2 μV/Mo
- Dual precision in 8-pin format
- Fits 4558, 1558 sockets
- Industry standard pinout
- Low input and offset current — ±5 nA max
- High gain — 400 V/mV min

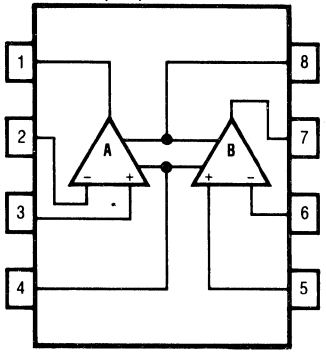
Description

Designed for low level signal conditioning and instrumentation applications, the 4207 is a precision dual amplifier combining excellent dc input specifications with low input noise characteristics. Ultra low offset voltage, low drift, high CMRR, and low input bias currents serve to reduce input related errors to less than 0.01% in a typical high gain instrumentation amplifier system (Av = 1000). The 4207 contains two separate amplifiers with a high degree of isolation between them; each is complete, requiring no external compensation capacitors or offset nulling potentiometers. The inherent V_{OS} is typically less than 150 μV, resulting in superior temperature drift, and this low initial offset is further reduced by "Zener-zap" nulling when the wafers are tested.

Advanced thin film and nitride dielectric processing allows the 4207 to achieve its high performance and small size (the 4207 is offered in 8-lead DIPs). The 4207 fits the industry standard 8-lead op amp pin-out.

Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Output A
2	Input A Inverting
3	Input A Non-Inverting
4	$-V_S$
5	Input B Non-Inverting
6	Input B Inverting
7	Output B
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC4207FN	N	0°C to +70°C
RC4207GN	N	0°C to +70°C
RV4207FD	D	-25°C to +85°C
RV4207GD	D	-25°C to +85°C
RM4207BD	D	-55°C to +125°C
RM4207BD/883B*	D	-55°C to +125°C

*Mil-Std-883, Level B processing
D = 8-lead ceramic DIP
N = 8-lead plastic DIP
Contact your sales representative for other package/ temperature range combinations.

Absolute Maximum Ratings

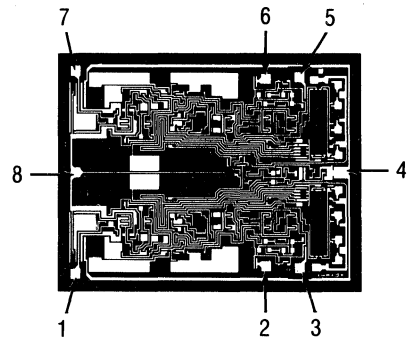
Supply Voltage ..... ±18V
Input Voltage* ..... ±18V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4207B ..... -55°C to +125°C
RC4207F/G ..... 0°C to +70°C
RV4207F/G ..... -25°C to +85°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

*For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead Plastic DIP
Max. Junction Temp.	175°C	125°C
Max. P_D T_A < 50°C	833 mW	468 mW
Therm. Res. θ_{JC}	45°C/W	—

Mask Pattern



65-02688A

Die Size: 115 × 90 mils
Min. Pad Dimensions: 4 × 4 mils

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	4207B			Units
		Min	Typ	Max	
Input Offset Voltage[1]			50	200	μV
Average Input Offset Voltage Drift[2]			0.3	1.3	μV/°C
Input Offset Current			±6.0	±15	nA
Average Input Offset Current Drift			8.0		pA/°C
Input Bias Current			±6.0	±15	nA
Average Input Bias Current Drift			13		pA/°C
Input Voltage Range		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	94	120		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	94	115		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_O = ±10V	200	400		V/mV
Maximum Output Voltage Swing	R_L > 2.0kΩ	±11	±12.6		V
Power Consumption	R_L = ∞		150	240	mW

Notes: 1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Electrical Characteristics (V_S = ±15V, -25°C to +85°C for hermetic packages, 0°C ≤ T_A ≤ +70°C for plastic packages unless otherwise noted)

Parameters	Test Conditions	4207F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			45	150		85	250	μV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.7		μV/°C
Input Offset Current			±2.0	±10		±1.6	±15	nA
Average Input Offset Current Drift			8.0			12		pA/°C
Input Bias Current			±2.0	±10		±3.0	±15	nA
Average Input Bias Current Drift			13			18		pA/°C
Input Voltage Range		±10	±13.5		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	94	120		92	106		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	94	115		92	100		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_O = ±10V	200	450		75	400		V/mV
Maximum Output Voltage Swing	R_L > 2.0kΩ	±11	±12.6		±11	±12.6		V
Power Consumption	R_L = ∞		150	240		150	240	mW

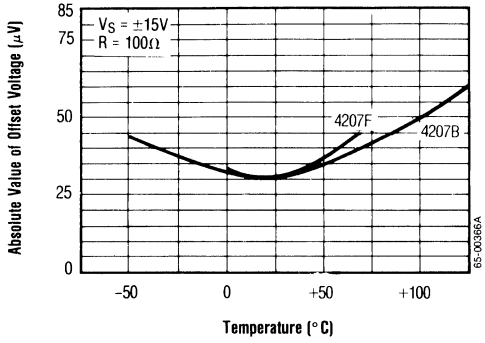
Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4207B/F			4207G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			30	75		60	150	μV
Long Term V_{OS} Stability[1]			0.2			0.5		μV/Mo
Input Offset Current			±0.5	±5		±2	±10	nA
Input Bias Current			±0.5	±5		±2	±10	nA
Input Noise Voltage	0.1Hz to 10Hz		0.35			0.35		μV_{p-p}
Input Noise Voltage Density	f_0 = 10Hz		10.3			10.3		$\frac{nV}{\sqrt{Hz}}$
	f_0 = 100Hz		10			10		
	f_0 = 1000Hz		9.6			9.6		
Input Noise Current	0.1Hz to 10Hz		14			14		pA_{p-p}
Input Noise Current Density	f_0 = 10Hz		0.32			0.32		$\frac{pA}{\sqrt{Hz}}$
	f_0 = 100Hz		0.14			0.14		
	f_0 = 1000Hz		0.12			0.12		
Input Resistance (Diff. Mode)			60			31		MΩ
Input Resistance (Com. Mode)			200			120		GΩ
Input Voltage Range[4]		±11	±14		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	100	126		94	110		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	100	110		94	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	400	600		250	400		V/mV
	V_O = ±1.0V, R_L = 1kΩ, V_S = ±4.0V	200	400		100	200		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slewing Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		V/μS
Closed Loop Bandwidth	A_{VCL} = +1.0		1.5			1.5		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		150	200		160	240	mW
	V_S = ±4.0V, R_L = ∞		35	50		48	64	
Crosstalk		126	155		126	155		dB

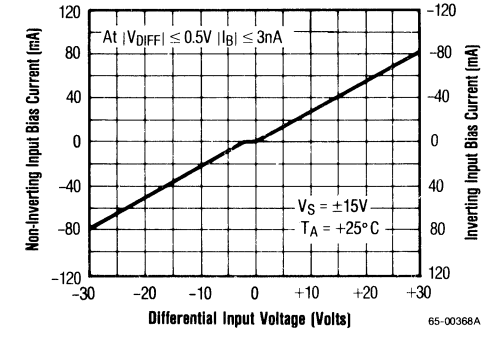
Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Typical Performance Characteristics

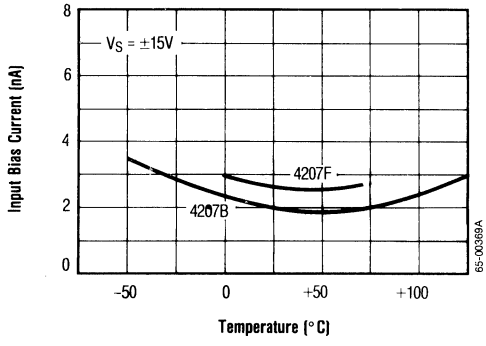
Offset Voltage vs. Temperature



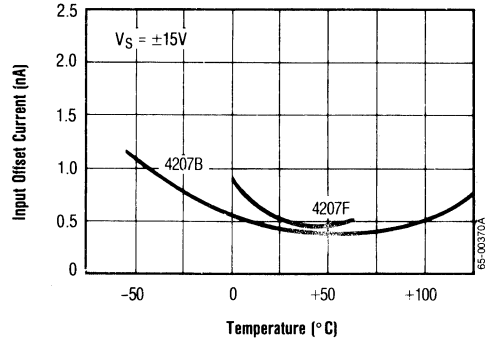
Input Bias Current vs. Differential Input Voltage



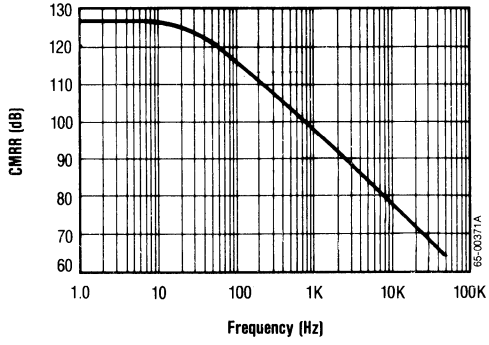
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature

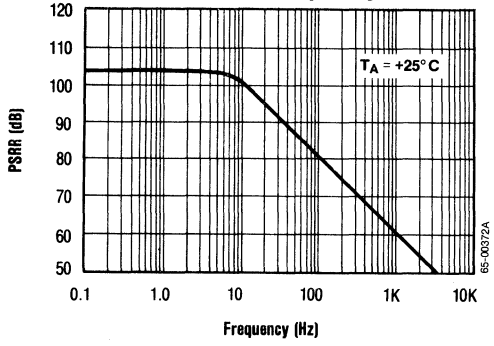


CMRR vs. Frequency

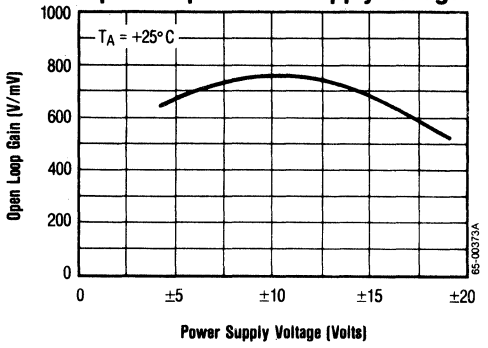


Typical Performance Characteristics (Continued)

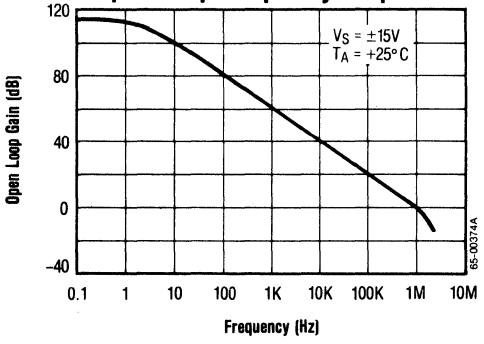
PSRR vs. Frequency



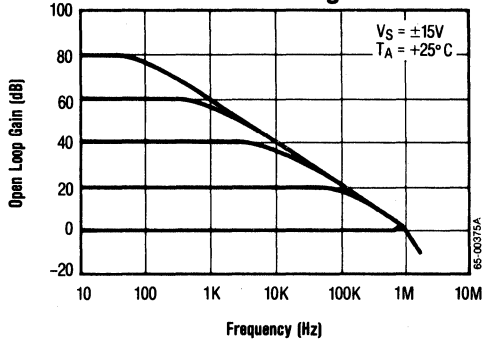
Open Loop Gain vs. Supply Voltage



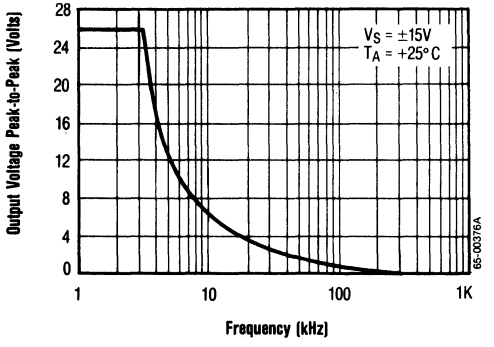
Open Loop Frequency Response



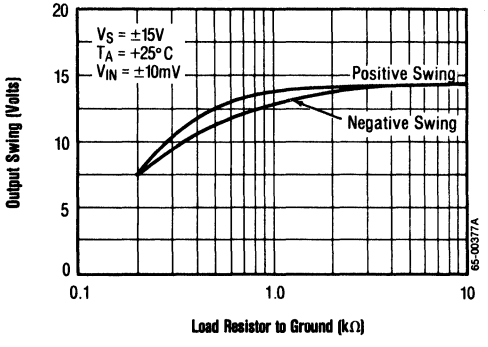
Closed Loop Response for Various Gain Configurations



Maximum Undistorted Output vs. Frequency

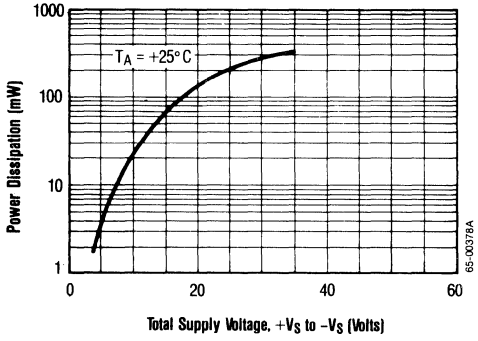


Output Voltage vs. Load Resistance

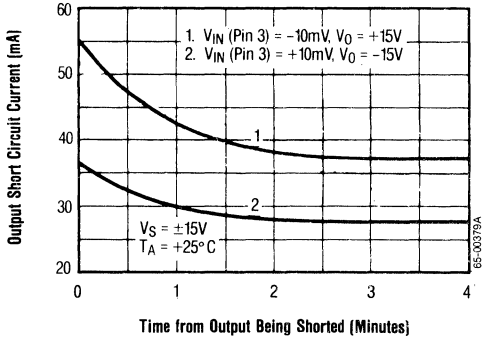


Typical Performance Characteristics (Continued)

Power Consumption vs. Supply Voltage

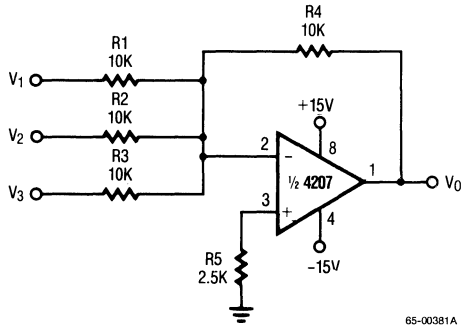


Output Short Circuit Current vs. Time

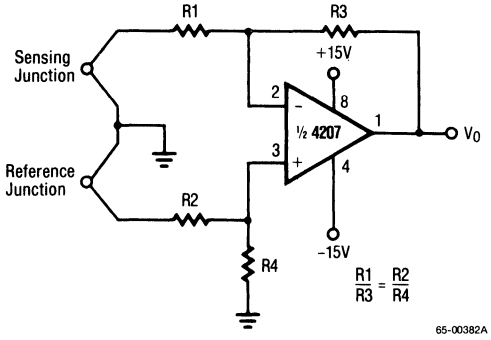


Typical Applications

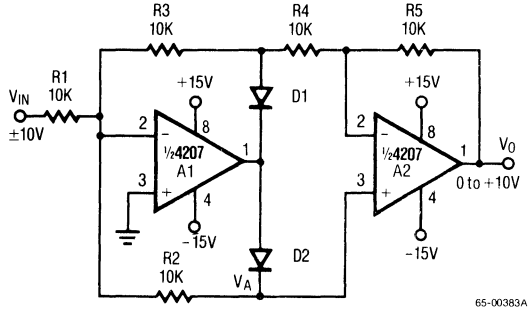
Adjustment-Free Precision Summing Amplifier



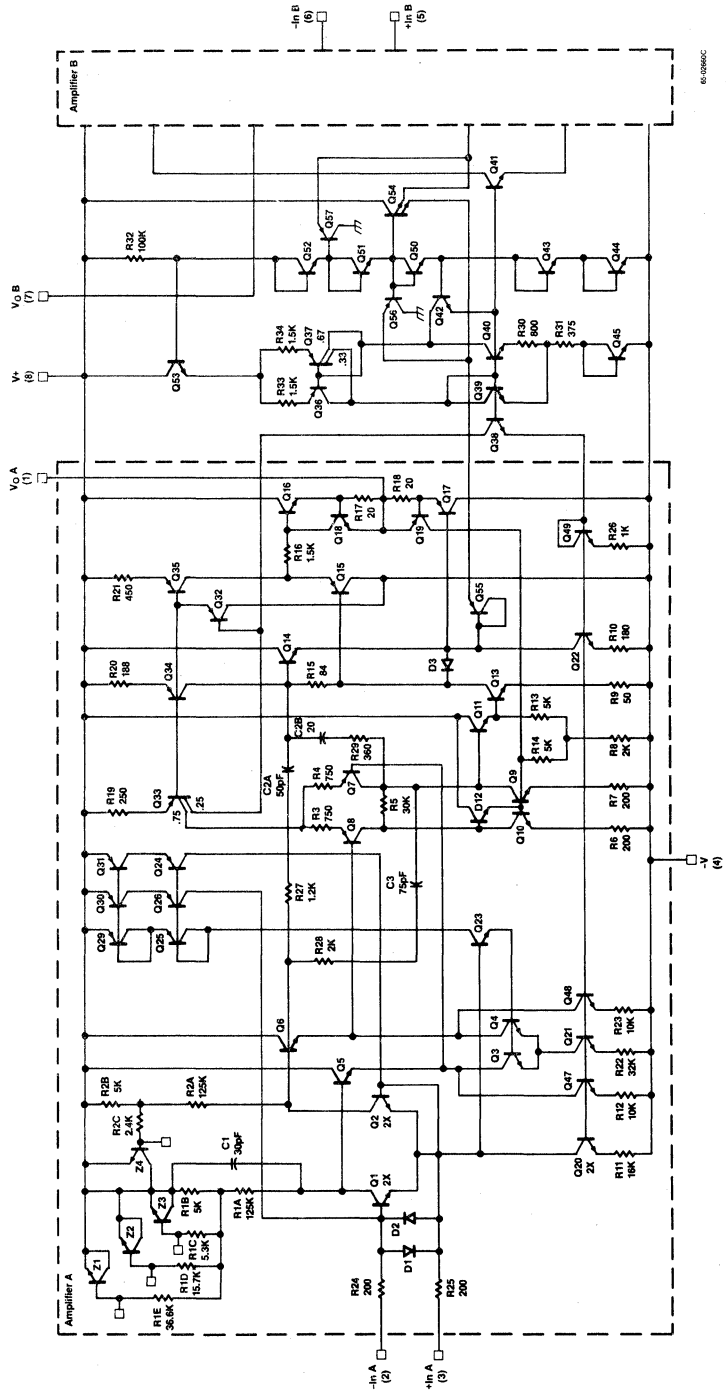
High Stability Thermocouple Amplifier



Precision Absolute Value Circuit



Schematic Diagram



RC4227 Precision Monolithic Dual Operational Amplifier

Features

- Very low noise
  Spectral noise density — 3.0 nV/√Hz
  1/f noise corner frequency — 2.7 Hz
- Very low V_{os} drift
  0.2 µV/Mo; 0.2 µV/°C
- High gain — 500 V/mV
- High output drive capability — ±10V into 1K load
- High slew rate — 2.7 V/µS typ
- Wide gain bandwidth product — 8 MHz typ
- High common mode rejection ratio — 104 dB
- Low input offset voltage — 75 µV
- Low frequency noise — 0.08 μV_{p-p} 0.1 Hz to 10 Hz typ
- Low input offset current — 2.5 nA typ
- Standard dual 8-lead pinout

Description

The 4227, a dual version of the OP-27, is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70°) in a unity gain configuration. Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 75 µV max. Input bias current cancellation techniques are used to obtain ±55 nA max. input bias currents.

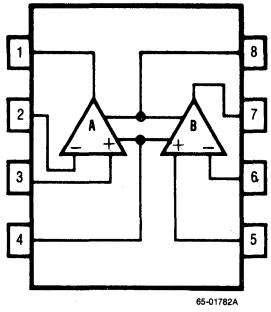
In addition to providing superior performance for audio frequency range applications, the 4227 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120 dB. A phase margin of 70° at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000 pF.[1] The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The performance of the 4227 is achieved through the usage of precision amplkifier design techniques coupled with a process that combines nitride transistors and capacitors with precision thin-film resistors. The die size savings of nitride capacitors and thin film resistors allow the 4227 to be offered in an 8-pin minidip package and fit the industry standard dual op amp pinout.

[1]By decoupling the load capacitance with a series resistor of 50 or more, load capacitances larger than 2000 pF can be accommodated.

Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Output A
2	Input A Inverting
3	Input A Non-Inverting
4	$-V_S$
5	Input B Non-Inverting
6	Input B Inverting
7	Output B
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC4227FN	N	0°C to +70°C
RC4227GN	N	0°C to +70°C
RV4227FD	D	-25°C to +85°C
RV4227GD	D	-25°C to +85°C
RM4227BD	D	-55°C to +125°C
RM4227BD/883B*	D	-55°C to +125°C

*Mil-Std-883, Level B processing
D = 8-lead ceramic DIP
N = 8-lead plastic DIP
Contact your sales representative for other package/ temperature range combinations.

Absolute Maximum Ratings

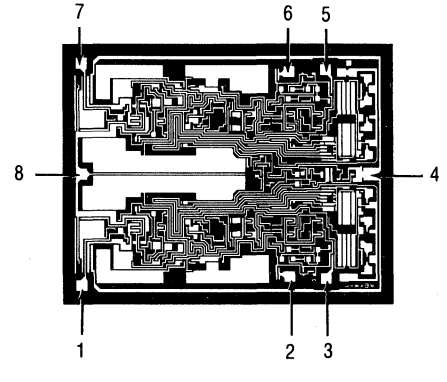
Supply Voltage ..... ±18V
Input Voltage* ..... ±18V
Differential Input Voltage 0.7V
Internal Power Dissipation** ..... 658 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4227B ..... -55°C to +125°C
RV4227F/G ..... -25°C to +85°C
RC4227F/G ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

*For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead Plastic DIP
Max. Junction Temp.	175°C	125°C
Max. P_D $T_A < 50°C$	833 mW	468 mW
Therm. Res. θ_{JC}	45°C/W	—

Mask Pattern



Die Size: 115 × 90 mils
Min. Pad Dimensions: 4 × 4 mils

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4227B/F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			20	75		30	150	μV
Long Term Input Offset Voltage Stability[1]			0.3			0.4		μV/Mo
Input Offset Current			±2.5	±10		±5	±15	nA
Input Bias Current			±5	±15		±7.5	±25	nA
Input Noise Voltage	0.1Hz to 10Hz		0.08			0.08		μV_{p-p}
Input Noise Voltage Density	f_0 = 10Hz		3.8			3.8		$\frac{nV}{\sqrt{Hz}}$
	f_0 = 30Hz		3.3			3.3		
	f_0 = 1000Hz		3.2			3.2		
Input Noise Current Density	f_0 = 10Hz		1.7			1.7		$\frac{pA}{\sqrt{Hz}}$
	f_0 = 30Hz		1.0			1.0		
	f_0 = 1000Hz		0.4			0.4		
Input Resistance (Diff. Mode)			5.0			4.0		MΩ
Input Resistance (Com. Mode)			2.5			2.0		GΩ
Input Voltage Range[2]		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	104	123		100	120		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±16.5V	104	120		100	118		dB
Large Signal Voltage Gain	$R_L \geq 2.0k\Omega$, V_0 = ±10V	500	1000		400	800		V/mV
	$R_L \geq 1.0k\Omega$, V_0 = ±10V	400	800		300	600		
	V_0 = ±1.0V, V_S = ±4.0V $R_L \geq 1.0k\Omega$	250	500		200	400		
Output Voltage Swing	$R_L \geq 2.0k\Omega$	±12	±13.8		±12	±13.8		V
	$R_L \geq 1k\Omega$	±11	±12		±11	±12		
Slew Rate	$R_L \geq 2.0k\Omega$	1.5	2.7		1.5	2.7		V/μS
Gain Bandwidth Product		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_0 = 0, I_0 = 0		70			70		Ω
Power Consumption	R_L = ∞		160	200		180	240	mW
Crosstalk		126	155		126	155		dB

Notes: 1. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately .5 seconds after application of power.
Caution: The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	4227B			Units
		Min	Typ	Max	
Input Offset Voltage[1]			50	200	μV
Average Input Offset Voltage Drift[2]			0.3	1.3	μV/°C
Input Offset Current			±10	±35	nA
Input Bias Current			±15	±45	nA
Input Voltage Range		±10	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	119		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	100	114		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_O = ±10V	350	650		V/mV
Output Voltage Swing	R_L > 2.0kΩ	±11	±13.2		V
Power Consumption	R_L = ∞		200	280	mW

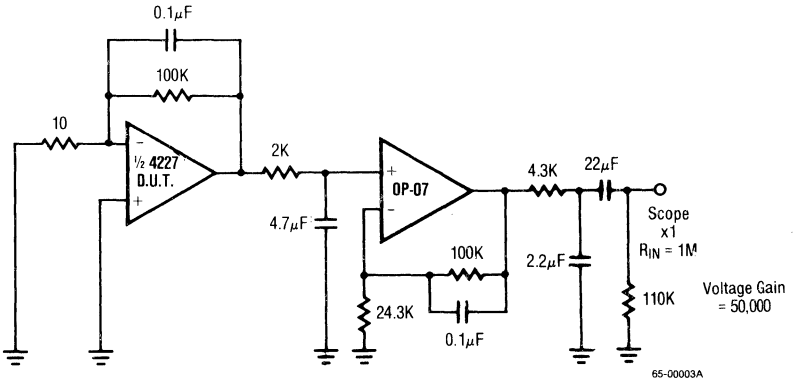
Notes: 1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

Electrical Characteristics (V_S = ±15V, -25°C to +85°C for hermetic packages, 0°C ≤ T_A ≤ +70°C for plastic packages unless otherwise noted)

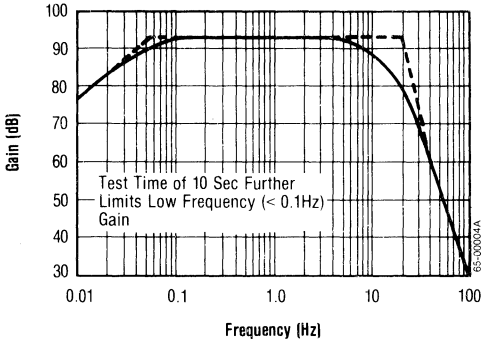
Parameters	Test Conditions	4227F			4227G			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			40	150		85	250	μV
Average Input Offset Voltage Drift[2]			0.3	1.3		0.4		μV/°C
Input Offset Current			±8	±15		±10	±35	nA
Input Bias Current			±10	±30		±15	±45	nA
Input Voltage Range		±10	±11.8		±10	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	100	121		92	118		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	100	116		92	114		dB
Large Signal Voltage Gain	R_L > 2.0kΩ, V_O = ±10V	350	700		250	500		V/mV
Output Voltage Swing	R_L > 2.0kΩ	±11	±13.5		±11	±13.5		V
Power Consumption	R_L = ∞		180	240		200	280	mW

Typical Performance Characteristics

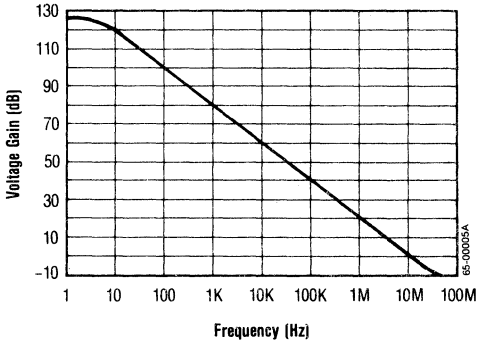
0.1Hz to 10Hz Noise Test Circuit (1/2 Shown)



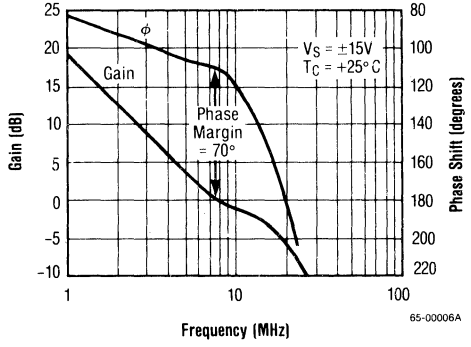
0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response



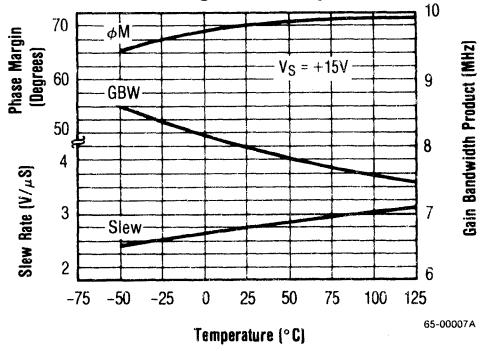
Open Loop Gain vs. Frequency



Gain, Phase Shift vs. Frequency

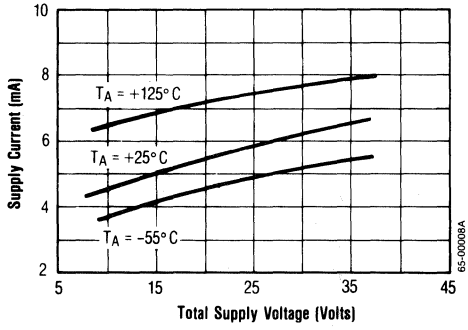


Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature

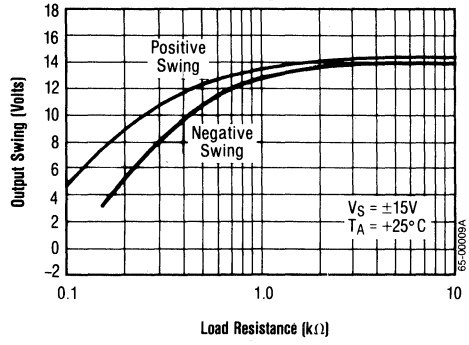


Typical Performance Characteristics (Continued)

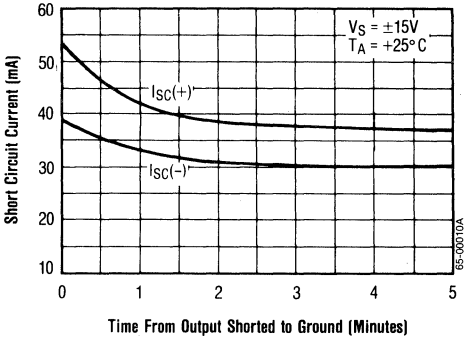
Supply Current vs. Supply Voltage



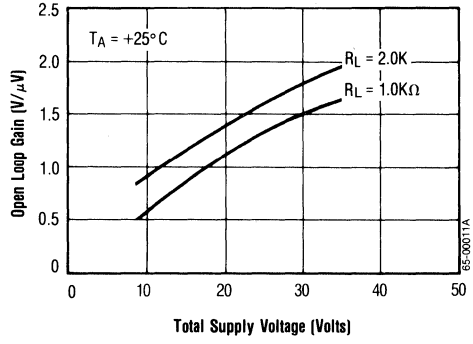
Maximum Output Swing vs. Resistive Load



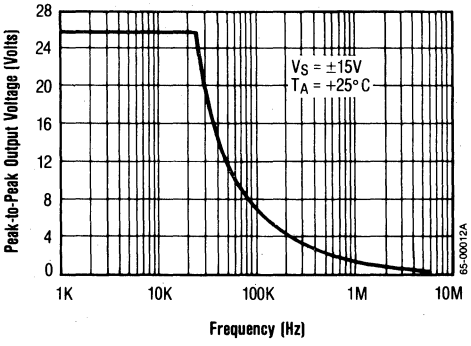
Short Circuit Current vs. Time



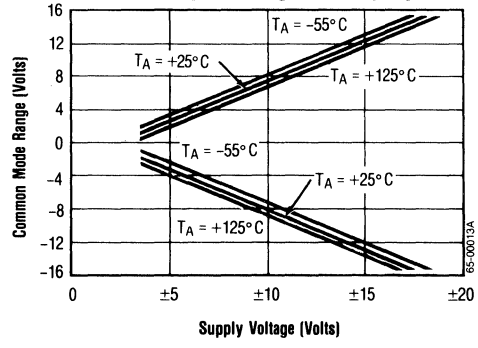
Open Loop Voltage Gain vs. Supply Voltage



Maximum Undistorted Output vs. Frequency

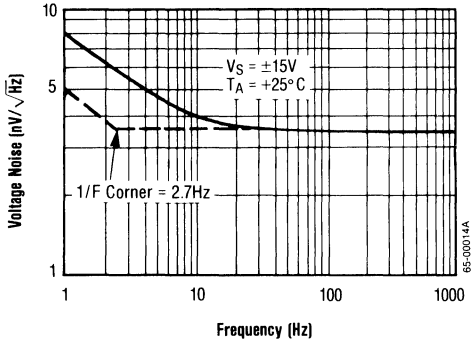


Common Mode Input Range vs. Supply Voltage

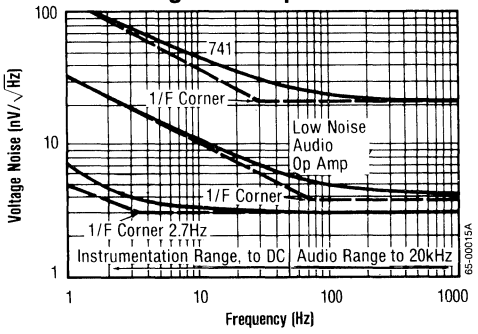


Typical Performance Characteristics (Continued)

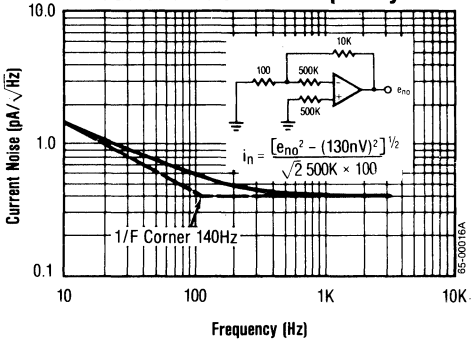
4227 Voltage Noise vs. Frequency



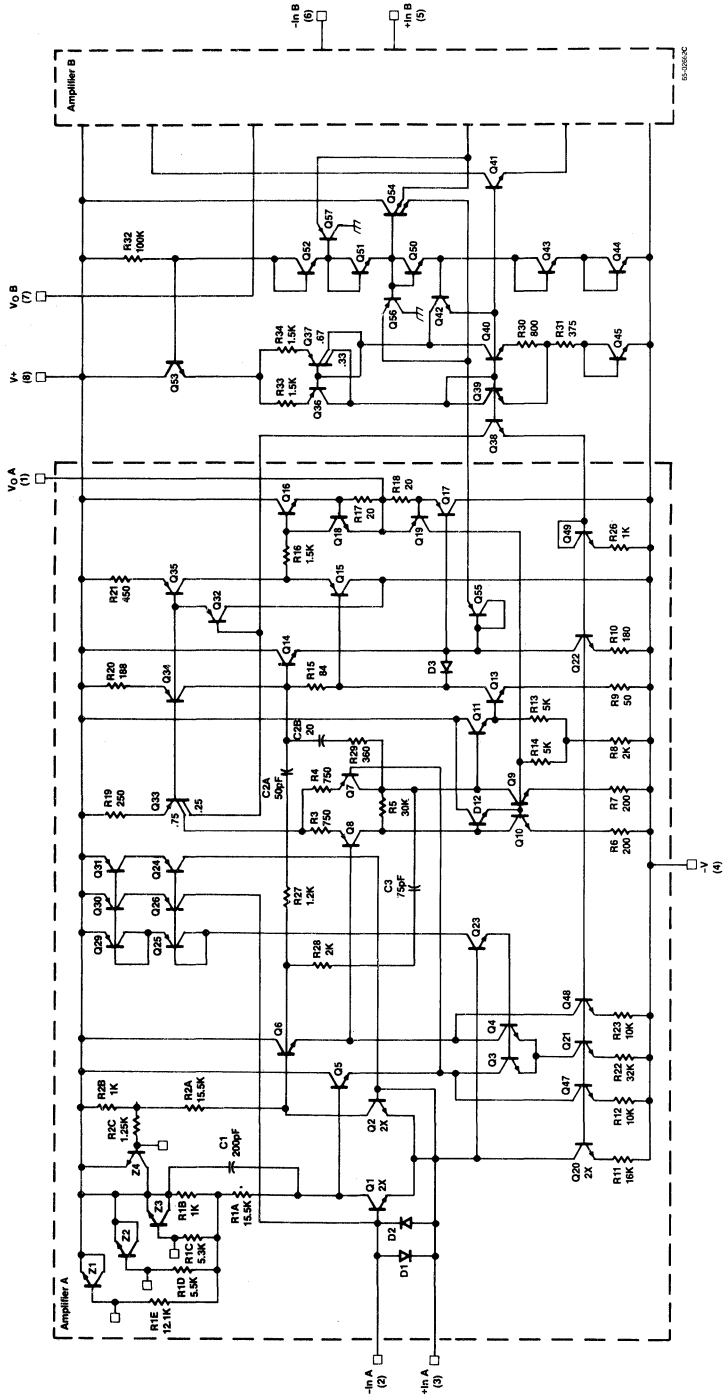
A Comparison of Op Amp Voltage Noise Spectrums



Current Noise vs. Frequency



Schematic Diagram



RC4277 Dual Precision Operational Amplifiers

Features

- High dc precision
- Very low V_{OS} — 30 μV max
- Very low V_{OS} drift — 0.3 μV/°C max
- High open-loop gain — 5M min
- High CMRR — 120 dB min
- High PSRR — 110 db min
- Low noise — 0.35 μV_{p-p} (0.1 to 10 Hz)
- Low bias current — 4.0 nA max
- Low power consumption — 120 mW max

Description

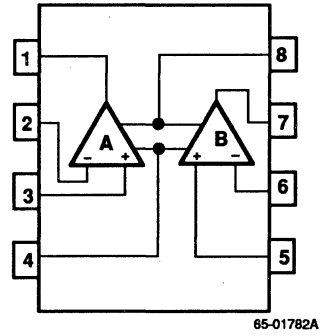
The RC4277 provides the highest precision available in a dual bipolar operational amplifier. A monolithic dual version of the RC4077, the RC4277 is designed to replace OP-207, LT1002, OP-07 and OP-77 type amplifiers in applications requiring high PC board layout density. The RC4277 has a well-balanced, mutually supporting set of input specifications. Low V_{OS}, low I_B, high open-loop gain, and excellent matching characteristics combine to raise the performance level of many instrumentation, low-level signal conditioning, and data conversion applications. PSRR, CMRR, V_{OS} drift, and noise levels also support high precision operation.

The high performance of the RC4277 results from two innovative and unconventional manufacturing steps, plus careful circuit layout and design. The key steps are SiCr thin-film resistor deposition and post-package trimming of the input offset voltage characteristic. The low ±30 μV max V_{OS} specification is maintained in high-volume production by way of the post-package trim procedure, where internal resistors are trimmed through the device input leads at the final test operation. Devices retain this low offset through the stability and accuracy of the trimmed thin-film resistors.

The RC4277 is available in 8-lead plastic and ceramic DIPs, and can be ordered with Mil-Std-883 Level B processing.

Connection Information

8-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	Output A
2	-Input A
3	+Input A
4	$-V_S$
5	+Input B
6	-Input B
7	Output B
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
RC4277EN	N	0°C to +70°C
RC4277FN	N	0°C to +70°C
RV4277ED	D	-25°C to +85°C
RV4277FD	D	-25°C to +85°C
RM4277AD	D	-55°C to +125°C
RM4277AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

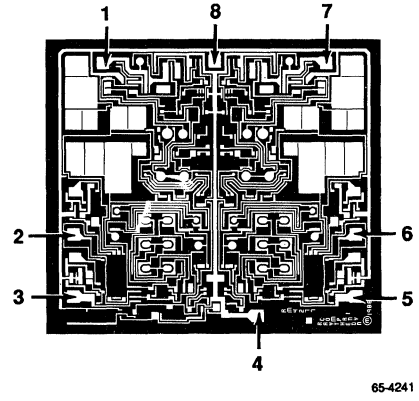
Supply Voltage ..... ±18V
Input Voltage* ..... ±18V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4277 ..... -55°C to +125°C
RV4277 ..... -25°C to +85°C
RC4277 ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

*For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
**Observe maximum power dissipation vs. ambient temperature in the table of Thermal Characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	833 mW	468 mW
Therm. Res θ_{JC}	45°C/W	—
Therm. Res. θ_{JA}	150°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	6.25 mW/°C

Mask Pattern



Die Size: mils
Min Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RC4277A/E			RC4277F			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			12	30		30	75	µV
Long Term V_{OS} Stability[1]			0.3			0.3		µV/Mo
Input Offset Current			0.5	3.0		0.5	5.0	nA
Input Bias Current			±0.5	±3.0		±0.5	±5.0	nA
Input Noise Voltage	0.1 Hz to 10 Hz		0.35			0.35		μV_{p-p}
Input Noise Voltage Density	F_O = 10 Hz		10.3			10.3		$nV/\sqrt{Hz}$
	F_O = 100 Hz		10			10		
	F_O = 1000 Hz		9.6			9.6		
Input Noise Current	0.1 Hz to 10 Hz		14			14		pA_{p-p}
Input Noise Current Density	F_O = 10 Hz		0.32			0.32		$nV/\sqrt{Hz}$
	F_O = 100 Hz		0.14			0.14		
	F_O = 1000 Hz		0.12			0.12		
Input Voltage Range[4]		±11	±14		±11	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	120	132		110	126		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	120	132		110	126		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	5000	7000		2500	5000		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12.5	±13		±12.5	±13		V
	$R_L \geq 2$ kΩ	±12	±12.8		±12	±12.8		
	$R_L \geq 1$ kΩ	±11	±12		±11	±12		
Slewing Rate	$R_L \geq 2$ kΩ	0.1	0.3		0.1	0.3		V/µS
Closed Loop Bandwidth	A_{VCL} = +1.0		1.5			1.5		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = 15V, R_L = ∞		140	165		140	165	mW
Crosstalk		126	155		126	155		dB

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µ.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after applica tion of power.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

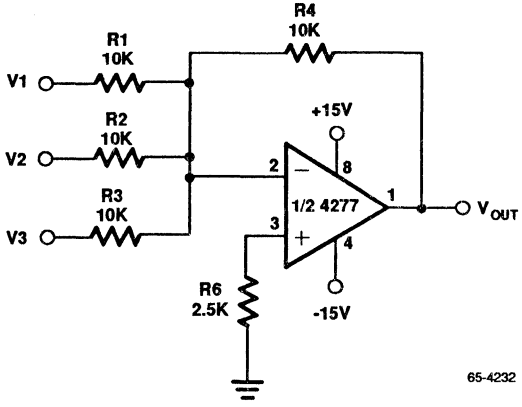
Parameters	Test Conditions	4277A Min	4277A Typ	4277A Max	Units
Input Offset Voltage[1]			25	60	µV
Average Input Offset Voltage Drift[2]			0.1	0.3	µV/°C
Input Offset Current			1.5	5.0	nA
Average Input Offset Current Drift			5.0	20	pA/°C
Input Bias Current			±1.5	±5.0	nA
Average Input Bias Current Drift			5.0	20	pA/°C
Input Voltage range		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	120	128		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5 V	120	128		dB
Large Signal Voltage Gain	R_L > 2 kΩ, V_O = ±10V	3000	5000		V/mV
Maximum Output Voltage Swing	R_L > 2 kΩ	±11	±12.6		V
Power Consumption	R_L = ∞		150	200	mW

Notes:
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.

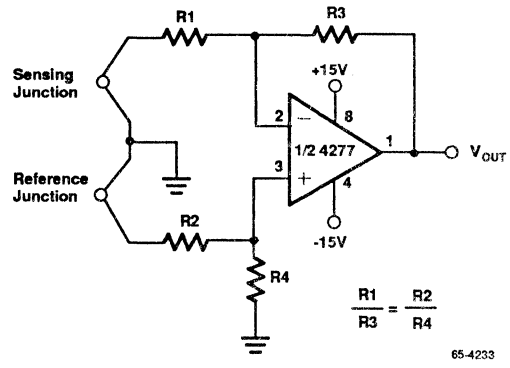
Electrical Characteristics (V_S = ±15V, -25°C to +85°C for hermetic packages, 0°C ≤ T_A ≤ +70°C for plastic packages unless otherwise noted)

Parameters	Test Conditions	4277E Min	4277E Typ	4277E Max	4277F Min	4277F Typ	4277F Max	Units
Input Offset Voltage	0°C ≤ T_A ≤ +70°C -25°C ≤ T_A ≤ +85°C		20 20	44 48		50 50	120 135	µV µV
Average Input Offset Voltage Drift[2]			0.1	0.3		0.3	1.0	µV/°C
Input Offset Current			1.5	5.0		1.5	5.0	nA
Input Bias Current			±1.5	±5.0		±1.5	±5.0	nA
Input Voltage Range		±10	±13.5		±10	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	120			110	124		dB
Power Supply Rejection Ratio	V_S = ±4V to ±16.5V	120			110	124		dB
Large Signal Voltage Gain	R_L > 2 kΩ, V_O = ±10V	3000	5000		1500	4000		V/mV
Maximum Output Voltage Swing	R_L > 2 kΩ	±11	±12.6		±11	±12.6		V
Power Consumption	R_L = ∞		150	200		150	200	mW

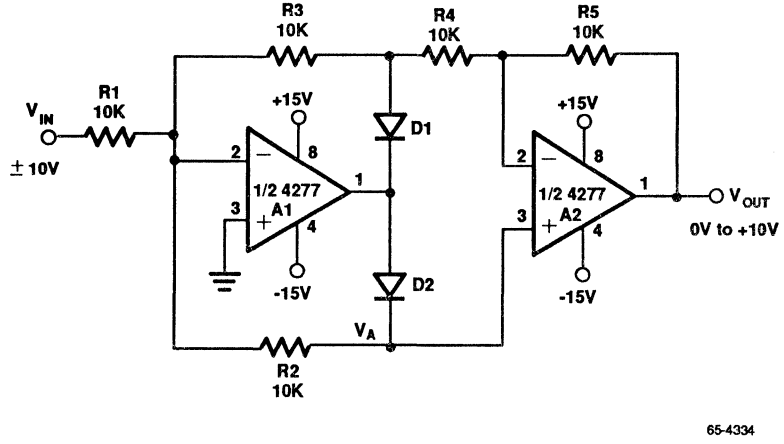
Typical Applications



Adjustment-Free Precision Summary Amplifier

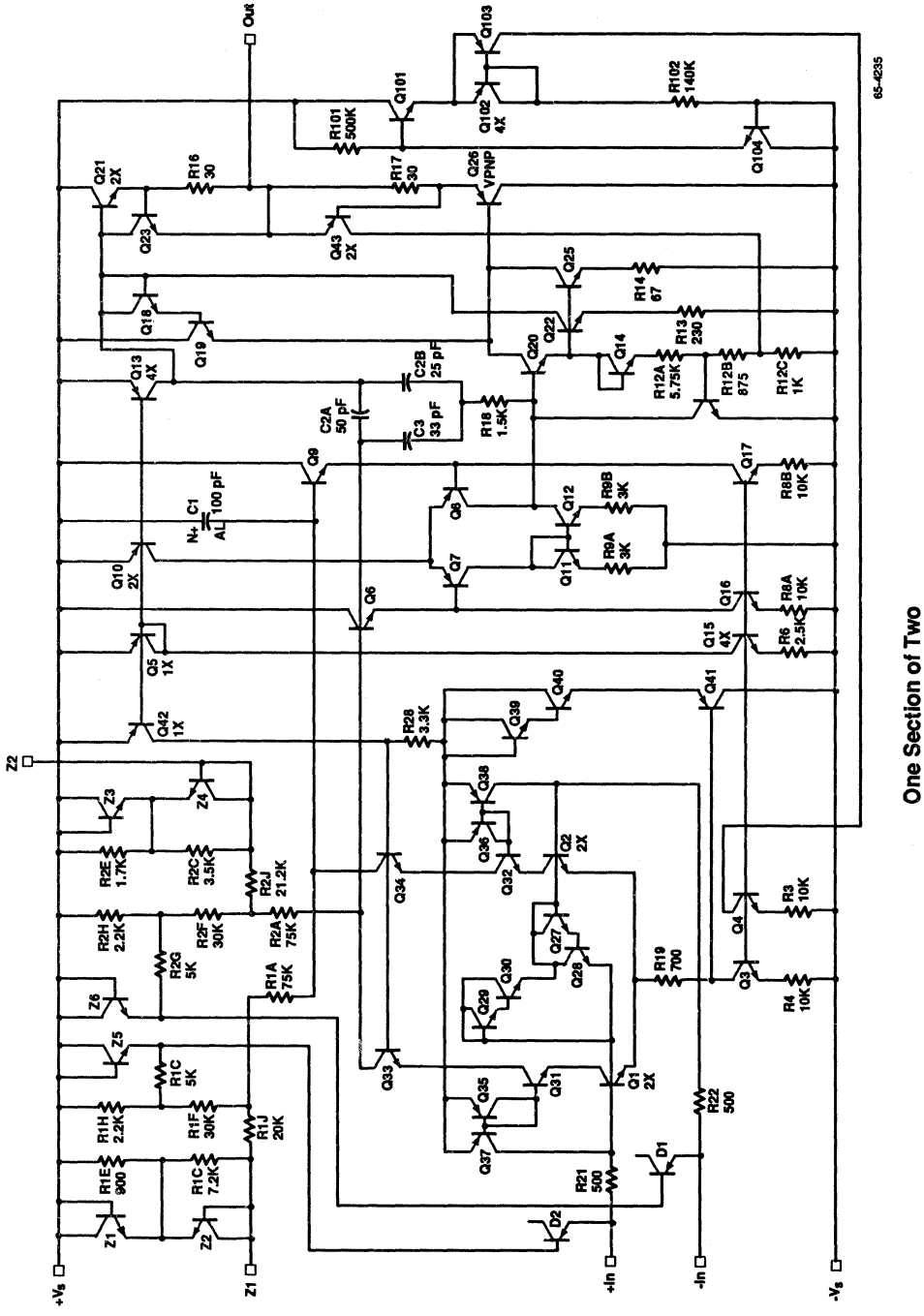


High Stability Thermocouple Amplifier



Precision Absolute Value Circuit

Schematic Diagram



LM108A/LH2108A Precision Operational Amplifiers

Features

- Low input bias current — 2nA
- Low input offset current — 200pA
- Low input offset voltage — 500μV
- Low input offset drift — 5μV/°C
- Wide supply range — ±3V to ±20V
- Low supply current — 0.6mA
- High PSRR — 96dB
- High CMRR — 96dB
- Mil-Std-883B available

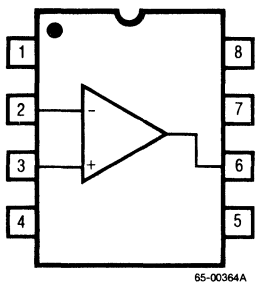
Description

These operational amplifiers feature low input bias current combined with the advantages of bipolar transistor construction; input offset voltages and currents are kept low over a wide range of temperature and supply voltage. Raytheon's superbeta bipolar manufacturing process includes extra treatment at epitaxial growth to ensure low input voltage noise.

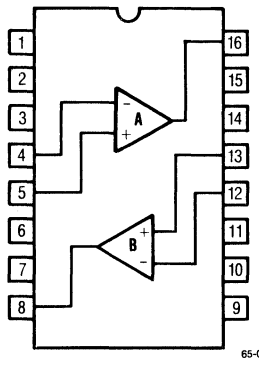
The LH2108 consists of two LM108 ICs in one 16-lead DIP. The "A" versions meet tighter electrical specifications than the plain versions. All types are available with 883B military screening.

Connection Information (Top Views)

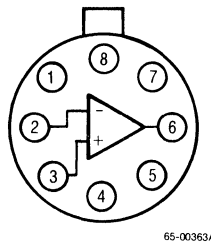
8-Lead DIP



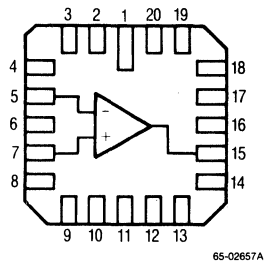
16-Lead DIP



TO-99 Can



20-Pad LCC



Pin	Function
1	Comp
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	Comp

Pin	Function
1	$+V_S$ (A)
2	Comp (A)
3	Comp (A)
4	-Input (A)
5	+Input (A)
6	$-V_S$
7	NC
8	Output (B)

Pin	Function
9	$+V_S$ (B)
10	Comp (B)
11	Comp (B)
12	-Input (B)
13	+Input (B)
14	NC
15	NC
16	Output (A)

Pin	Function
1	Comp
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	Comp

Pin	Function	Pin	Function
1	NC	11	NC
2	Comp	12	NC
3	NC	13	NC
4	NC	14	NC
5	-Input	15	Output
6	NC	16	NC
7	+Input	17	$+V_S$
8	NC	18	NC
9	NC	19	NC
10	$-V_S$	20	Comp

Ordering Information

Part Number	Package	Operating Temperature Range
LM108L	L	-55°C to +125°C
LM108AL	L	-55°C to +125°C
LM108D	D	-55°C to +125°C
LM108AD	D	-55°C to +125°C
LM108T	T	-55°C to +125°C
LM108AT	T	-55°C to +125°C
LH2108D	D	-55°C to +125°C
LH2108AD/883B	D	-55°C to +125°C

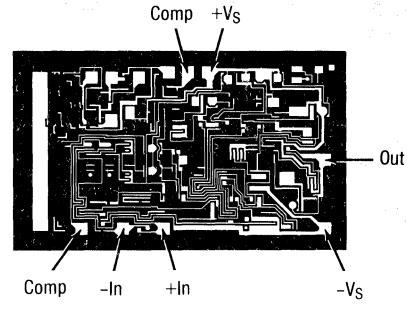
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 16 lead ceramic DIP (LH2108)
D = 8-lead ceramic DIP (LM108)
T = 8-lead metal can TO-99
L = 20-pad leadless chip carrier
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Current* ..... ±10 mA
Input Voltage** ..... ±15V
Output Short Circuit ..... Continuous
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (60 sec) ..... +300°C

*The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
**For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Mask Pattern



65-02659A

Die Size: 104 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead TO-99 Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP	20-Lead LCC
Max. Junction Temp.	175°C	175°C	175°C	175°C
Max. P_D T_A <50°C	658 mW	833 mW	1042 mW	925 mW
Therm. Res θ_{JC}	50°C/W	45°C/W	60°C/W	37°C/W
Therm. Res. θ_{JA}	190°C/W	150°C/W	120°C/W	105°C/W
For T_A >50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C	7.0 mW/°C

Electrical Characteristics ($\pm 5V \leq V_S \leq \pm 20V$ and $T_A = +25°C$ unless otherwise noted

Parameters	Test Conditions	LM108A/LH2108A			LM108/LH2108			Units
		Min	Typ	Max	Min	Tp	Max	
Input Offset Voltage			0.3	0.5		0.7	2.0	mV
Input Offset Current			0.05	0.2		0.05	0.2	nA
Input Bias Current			0.8	2.0		0.8	2.0	nA
Input Resistance[1]		30	70		30	70		MΩ
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	80	300		50	300		V/mV
Supply Current	Each Amplifier		0.3	0.6		0.3	0.6	mA

Electrical Characteristics ($\pm 5V \leq V_S \leq \pm 20V$; $-55°C \leq T_A \leq +125°C$ unless otherwise noted)

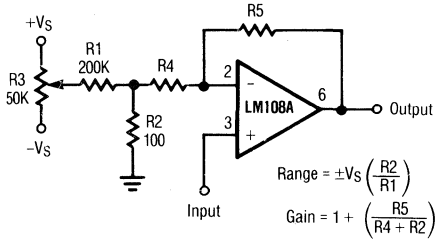
Parameters	Test Conditions	LM108A/LH2108A			LM108/LH2108			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.4	1.0		1.0	3.0	mV
Average Input Offset Voltage Drift[2]			1.0	5.0		3.0	1.5	µV/°C
Input Offset Current			0.1	0.4		0.1	0.4	nA
Average Input Offset Current Drift[2]			0.5	2.5		0.5	2.5	pA/°C
Input Bias Current			1.0	3.0		1.0	3.0	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_O = \pm 10V$, $R_L \geq 10\ k\Omega$	40	200		25	200		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$ $V_S = \pm 20V$	±16	±18		±16	±18		V
Input Voltage Range	$V_S = \pm 15V$	±13.5			±13.5			V
Common Mode Rejection Ratio	$V_{CM} = \pm 13.5$ $V_S = \pm 15V$	96	110		85	100		dB
Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 20V$	96	110		80	96		dB
Supply Current	Each Amplifier			0.6			0.6	mA

Notes: 1. Guaranteed by input bias current specification.
2. Sample tested

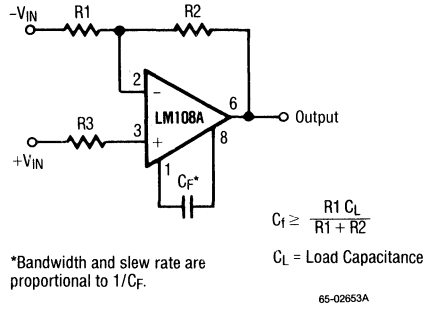
Typical Applications

The LM108 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to achieve the LM108A's rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifier's output or ground.

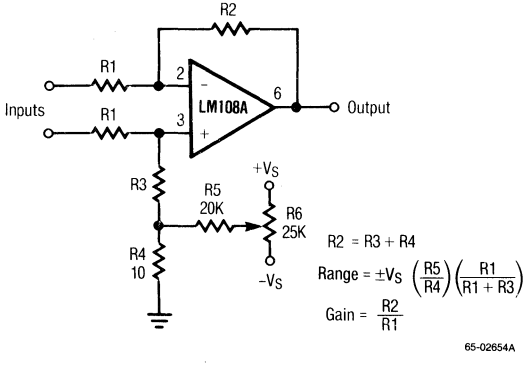
Offset Adjustment for Non-Inverting Amplifiers



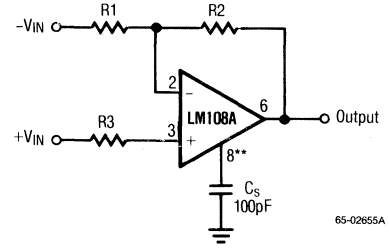
Standard Compensation Circuit



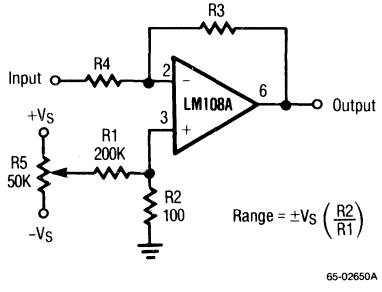
Offset Adjustment for Differential Amplifiers



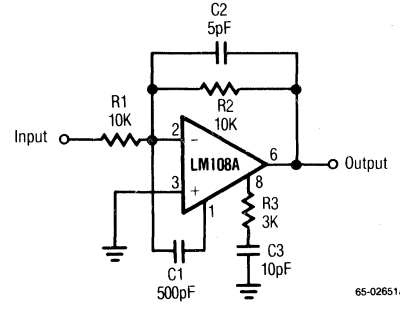
Alternate* Frequency Compensation



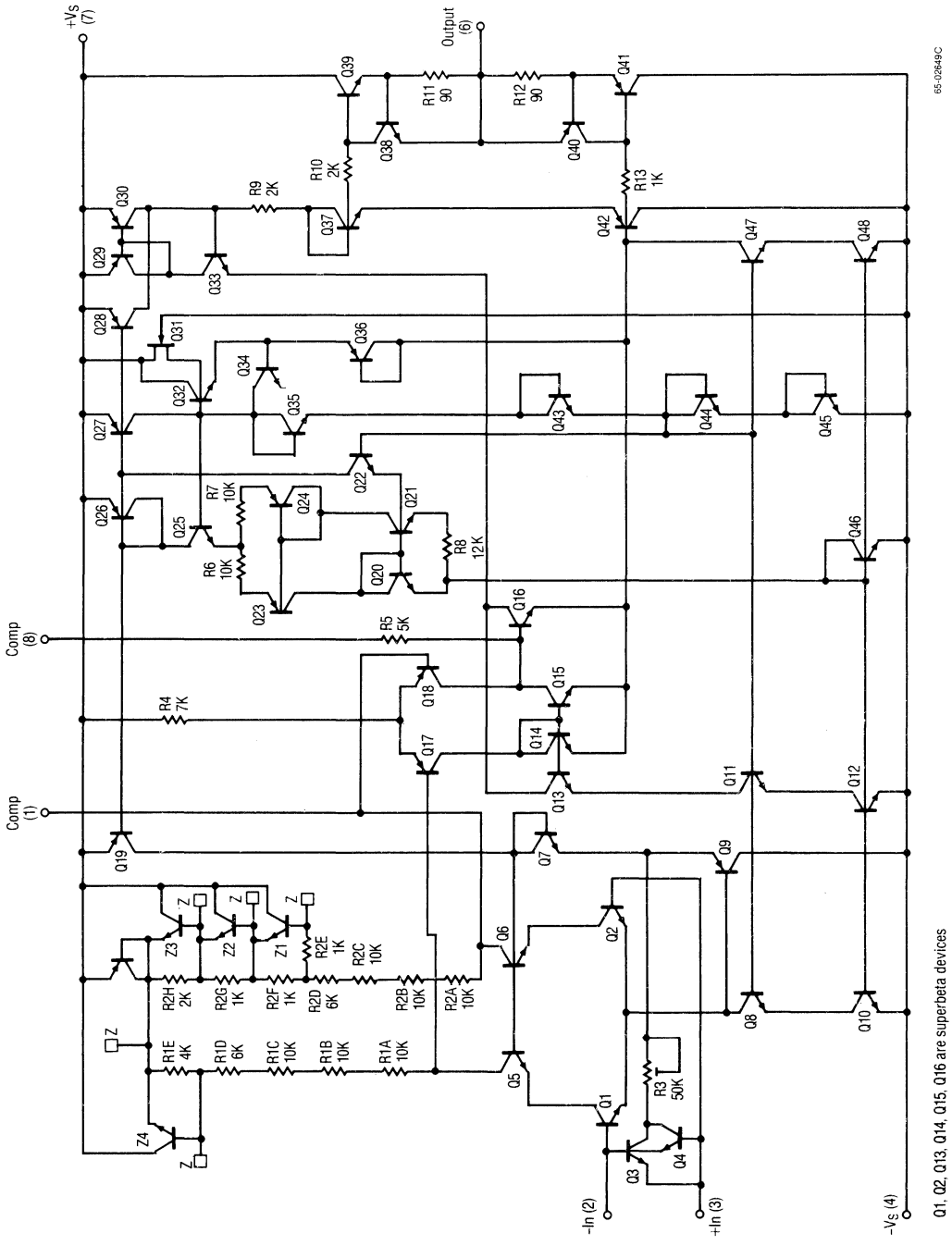
Offset Adjustment for Inverting Amplifiers



Feedforward Compensation



Schematic Diagram



LT-1001 Series Precision Operational Amplifiers

Features

- Ultra-low V_{OS} — 15 µV max
- Ultra-low V_{OS} drift — 0.6 µV/°C max
- Low input bias current — 2 nA max
- High CMRR — 114 dB min
- High PSRR — 110 dB min
- Low noise — 0.3 μV_{p-p} (0.1 to 10 Hz)
- Low power dissipation — 75 mW max
- High gain linearity
- LCC, SO-8, DIP and can packages

Description

Designed for low level signal conditioning, instrumentation, and data conversion applications, the LT-1001 is a precision amplifier combining excellent dc input specifications with low input voltage noise. Advanced circuit design, wafer processing, and test methods all contribute to these well-balanced, mutually supporting input characteristics.

The circuit design uses special low-noise transistor geometries and careful thermal layout to achieve exceptionally low noise and linear gain characteristics. A patented, proprietary test method which includes digital V_{OS} nulling after packaging as well as at wafer test tightens the distribution of this parameter such that the highest grade, the LT-1001AM, is specified at ±15 µV maximum. This low V_{OS}, along with extra-low power dissipation (which reduces warm-up drift), set the LT-1001 apart from similar precision op amp types.

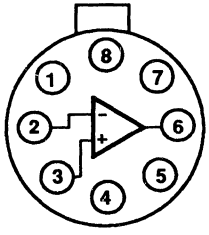
Ordering Information

Part Number	Package	Operating Temperature Range
LT-1001ACN	N	0°C to +70°C
LT-1001CN	N	0°C to +70°C
LT-1001ACM	M	0°C to +70°C
LT-1001CM	M	0°C to +70°C
LT-1001MT	T	-55°C to +125°C
LT-1001AMT/883B	T	-55°C to +125°C
LT-1001MD	D	-55°C to +125°C
LT-1001AMD/883B	D	-55°C to +125°C
LT-1001ML	L	-55°C to +125°C
LT-1001AML/883B	L	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

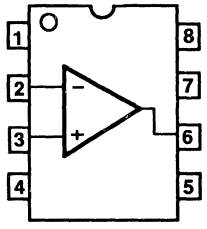
Connection Information

8-Lead TO-99 Metal Can
(Top View)



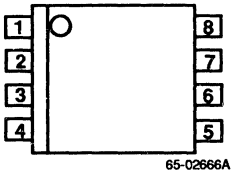
65-03205A

8-Lead Dual In-Line Package
(Top View)



65-03206A

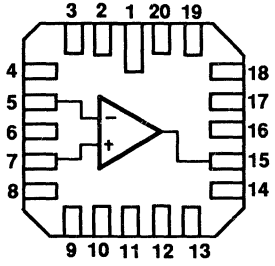
8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

20-Pad LCC
(Top View)



65-02657A

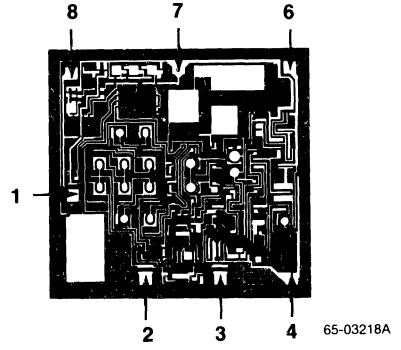
Pin	Function
2	V_{OS} Trim
5	-Input
7	+Input
10	$-V_S$
15	Output
17	$+V_S$
20	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
M Suffix ..... -55°C to +125°C
C Suffix ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8; 10 sec) ..... +260°C
Lead Soldering Temperature
(DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



65-03218A

Die Size: 75 x 78 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	20-Pad LCC	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Small Outline	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	175°C	125°C	125°C
Max. P_D T_A <50°C	925 mW	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	37°C/W	45°C/W	50°C/W	–	–
Therm. Res.θ_{JA}	105°C/W	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	7.0 mW/°C	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	LT-1001A			LT-1001M/C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]	LT-1001AM/883B		7.0	15		18	60	μV
	LT-1001AC		10	25				
Long Term Input Offset Voltage Stability[3,4]			0.2	1.0		0.2	1.5	μV/Mo
Input Offset Current			0.3	2.0		0.4	3.8	nA
Input Bias Current			±0.5	±2.0		±1.0	±4.0	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2,5]	f_O = 10 Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100 Hz		10	13		10	13	
	f_O = 1000 Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1 Hz to 10 Hz		14	30		14	30	pA_{p-p}
Input Noise Current Density[5]	f_O = 10 Hz		0.32	0.8		0.32	0.8	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100 Hz		0.14	0.23		0.14	0.23	
	f_O = 1000 Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	100		15	80		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	114	126		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	110	123		106	123		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±12V	450	2000		400	2000		V/mV
	$R_L \geq 1$ kΩ, V_O = ±10V	300	1000		250	1000		
Output Voltage Swing	$R_L \geq 2$ kΩ	±13	±14		±13	±14		V
	$R_L \geq 1$ kΩ	±12	±13.5		±12	±13.5		
Slew Rate	$R_L \geq 2$ kΩ	0.1	**0.3**		0.1	**0.3**		V/μS
Unity Gain Bandwidth	A_{VCL} = +1.0	0.4	0.8		0.4	0.8		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		50	75		50	80	mW
	V_S = ±3V, R_L = ∞		4.0	6.0		4.0	8.0	
Offset Adjustment Range	R_P = 20 kΩ		±4.0			±4.0		mV

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. LT1001AM/883B and LT-1001AC grades in hermetic packages are measured after the device is fully warmed up.
2. This parameter is tested on a sample basis only.
3. This parameter is guaranteed by design.
4. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV.
5. 10 Hz input noise voltage density is sample tested on every lot. Devices 100% tested at 10 Hz are available on request.

Electrical Characteristics ($V_S = \pm 15V$ and $-55°C \leq T_A \leq +125°C$ unless otherwise noted)

Parameters	Test Conditions	LT-1001AM/883B			LT-1001M			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			25	60		45	160	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.2	0.6		0.3	1.0	μV/°C
With External Trim[3]	$R_P = 20\ k\Omega$		0.2	0.6		0.3	1.0	
Input Offset Current			0.8	4.0		1.2	7.6	nA
Average Input Offset Current Drift[2]			5.0	25		8.0	50	pA/°C
Input Bias Current			±1.0	±4.0		±1.5	±8.0	nA
Average Input Bias Current Drift[2]			8.0	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	110	123		106	123		dB
Power Supply Rejection Ratio	$V_S = \pm 3.0V$ to $\pm 18V$	104	117		100	117		dB
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_O = \pm 10V$	300	600		200	600		V/mV
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12.5	±13		±12	±13		V
Power Consumption	$R_L = \infty$		60	90		60	100	mW

See notes on page 3.

Electrical Characteristics ($V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$ unless otherwise noted)

Parameters	Test Conditions	LT-1001AC			LT-1001C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	60		30	110	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.2	0.6		0.3	1.0	μV/°C
With External Trim[3]	$R_P = 20\ k\Omega$		0.2	0.6		0.3	1.0	
Input Offset Current			0.5	3.5		1.6	8.0	nA
Average Input Offset Current Drift[2]			8.0	35		12	50	pA/°C
Input Bias Current			±0.7	±3.5		±1.0	±5.5	nA
Average Input Bias Current Drift[2]			13	35		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	110	123		106	120		dB
Power Supply Rejection Ratio	$V_S = \pm 3.0V$ to $\pm 18V$	106	120		103	120		dB
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_O = \pm 10V$	300	600		250	600		V/mV
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12.5	±13.5		±12.5	±13.5		V
Power Consumption	$R_L = \infty$		60	85		60	90	mW

See notes on page 3.

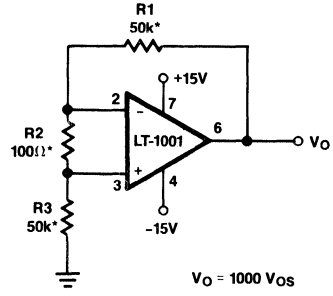
Applications Information

The LT-1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT-1001 can also be used in 741 applications provided that the nulling circuitry is removed.

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Input bias currents may flow either into or out of the input terminals, depending on the value of I_{OS}.

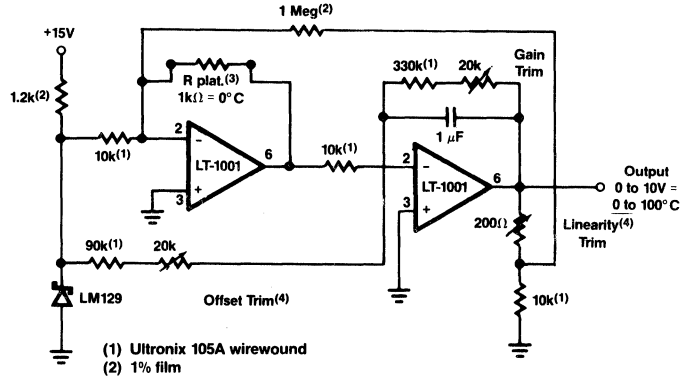
Typical Applications



65-03787A

*Resistors must have low thermoelectric potential.

Test Circuit for Offset Voltage and Its Drift With Temperature



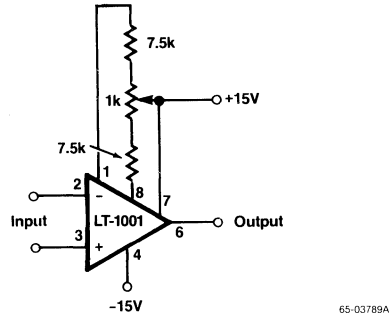
(1) Ultronix 105A wirewound
(2) 1% film
(3) Platinum RTD 118MF (Rosemount, Inc.)
(4) Trim sequence:
trim offset (0°C = 1000.0Ω),
trim linearity (35°C = 1138.7Ω),
trim gain (100°C = 1392.6Ω).
Repeat until all three points are fixed with ±0.025°C.

65-03788A

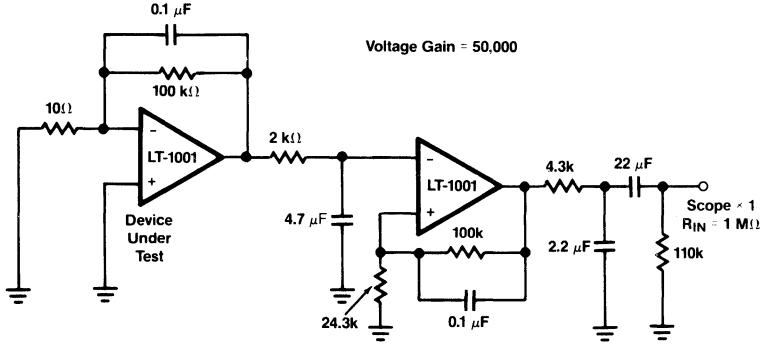
Linearized Platinum Resistance Thermometer With ±0.025°C Accuracy Over 0 to 100°C

Offset Voltage Adjustment

The input offset voltage of the LT-1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 300 μV, the change in drift will be 1 μV/°C. The adjustment range with a 10k or 20k pot is approximately 4.0 mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of ±100 μV.



Improved Sensitivity Adjustment

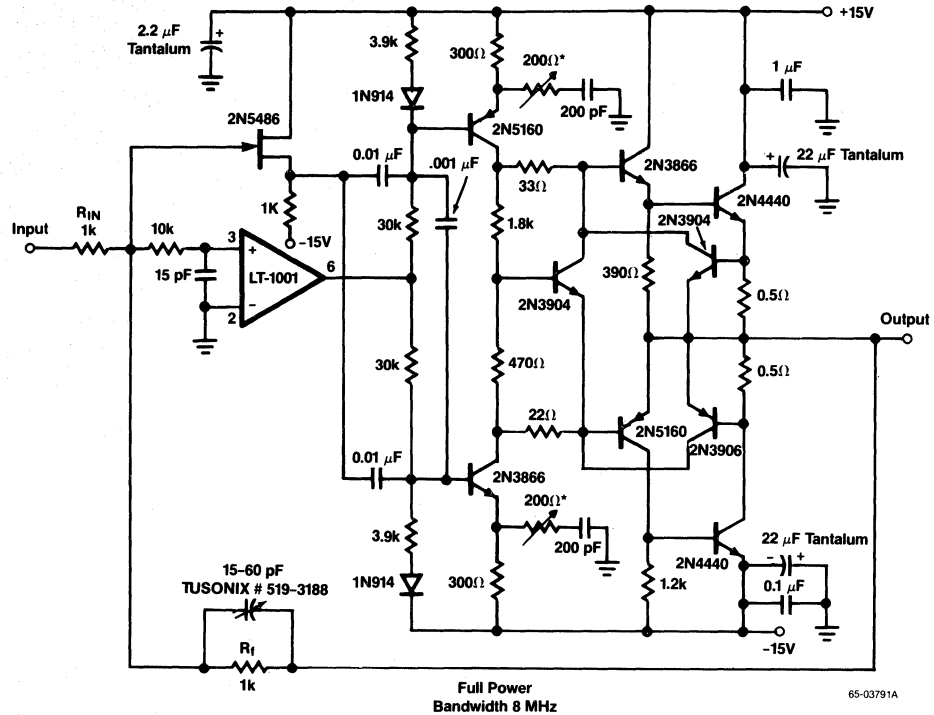


(1) Peak-to-peak noise is measured in a 10-second interval
(2) The device under test should be warmed up for 3 minutes and shielded from air currents.

65-03790A

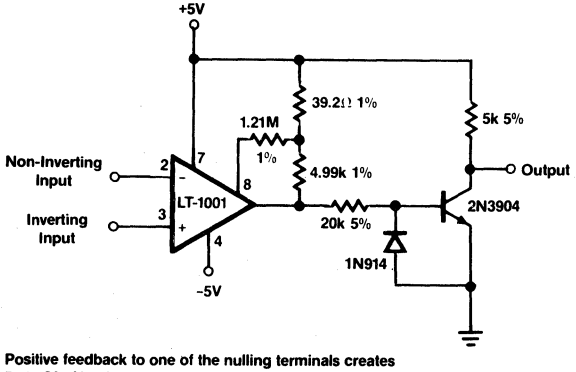
0.1 Hz to 10 Hz Noise Test Circuit

Typical Applications (Continued)



*Adjust for best squarewave at output.

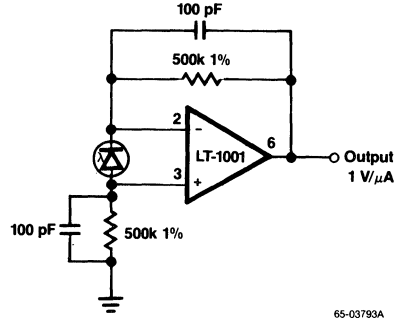
DC Stabilized — 1000 V/μS Op Amp



Positive feedback to one of the nulling terminals creates 5μ to 20 μV of hysteresis. Input offset voltage is typically changed by less than 5 μV due to the feedback.

65-03792A

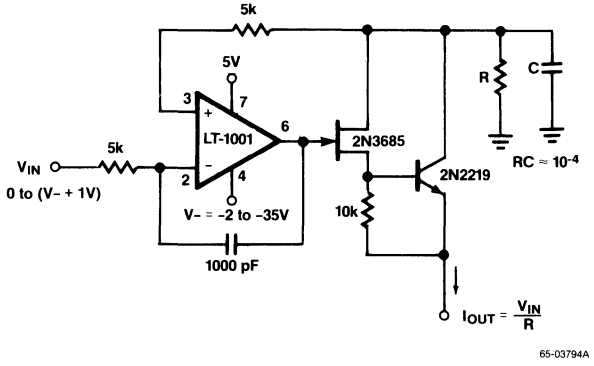
Microvolt Comparator With TTL Output



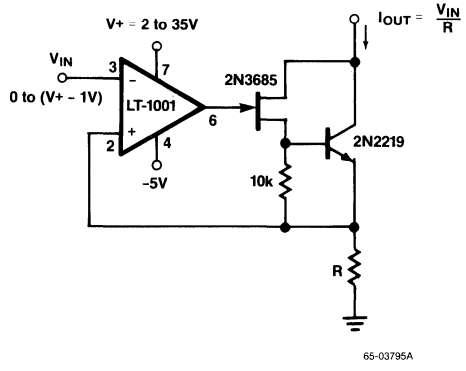
65-03793A

Photodiode Amplifier

Typical Applications (Continued)

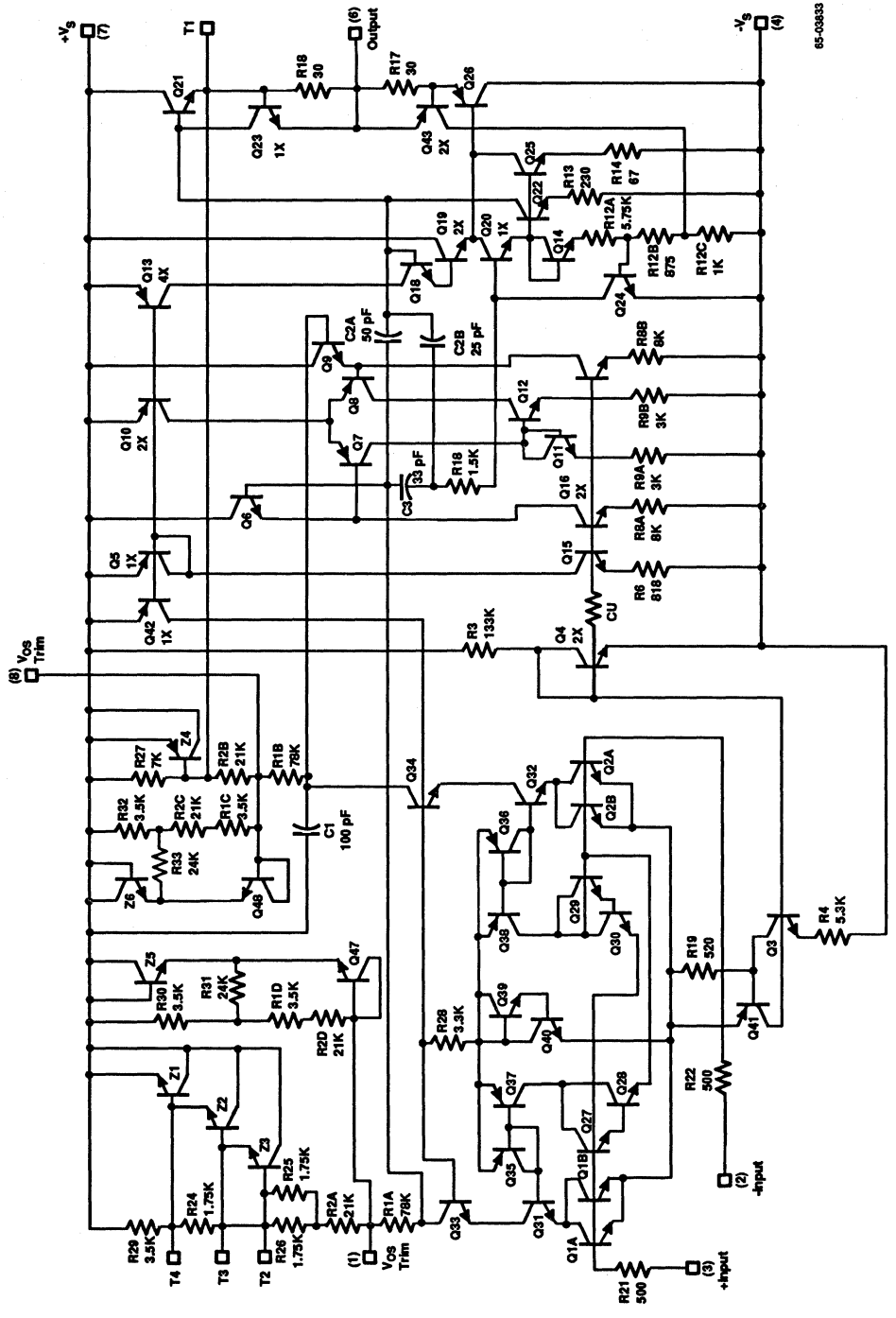


Precision Current Source



Precision Current Sink

Schematic Diagram



LT-1012 Low-Power Precision Operational Amplifiers

Features

- Low input bias current
  +25°C, 100 pA max
  -55°C to +125°C, 600 pA max
- Low input offset voltage — 35μV max
- Low V_{OS} drift — 1.5 μV/°C max
- Low supply current — 600 μA max
- High gain — 300 V/mV min
- High CMRR — 114 dB min
- High PSRR — 114 dB min
- Low noise — 0.5 μV_{p-p} (0.1 to 10 Hz)

Description

The LT-1012 is an instrumentation-type operational amplifier that combines the low input bias currents of a FET-type op amp with the low noise and low input offset voltage drift of a precision bipolar op amp. For a similar device with yet tighter specifications, refer to the RC4097 Data Sheet. The LT-1012 can improve the performance of a wide range of precision operational amplifier applications, including reference circuits, thermocouple amplifiers, charge integrators, sample-and-hold circuits, data conversion circuits, log amplifiers, and differential instrumentation amplifiers.

The superior performance of the LT-1012 is a result of advanced design and processing techniques, including post-package trimming of the input offset voltage, and superbeta processing of the input transistors. Picoampere input bias currents are maintained over the full military temperature range through the use of bias current cancellation techniques in the design of the input stage. The entire spectrum of input parameters, such as CMRR and PSRR, are specified very tightly so as to support the low I_B and low V_{OS} in maintaining overall system accuracy.

The LT-1012 is a direct replacement for industry-standard LT-1012 types except for lacking the over-compensation function at pin 5 (the LT-1012 is internally compensated for unity-gain stability).

The LT-1012 is available in plastic DIPs or TO-99 metal cans. The devices are specified over both commercial and military temperature ranges, and can be ordered with Mil-Std-883 processing.

Ordering Information

Part Number	Package	Operating Temperature Range
LT-1012CT	T	0°C to +70°C
LT-1012CN	N	0°C to +70°C
LT-1012MT	T	-55°C to +125°C
LT-1012MT/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage ..... ±0.7V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
M Suffix ..... -55°C to +125°C
C Suffix ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

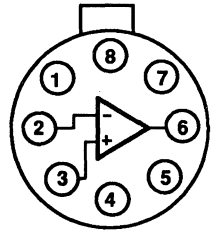
*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Thermal Characteristics

	8-Lead TO-99 Metal Can	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	658 mW	468 mW
Therm. Res θ_{JC}	507°C/W	—
Therm. Res. θ_{JA}	190°C/W	160°C/W
For T_A <50°C Derate at	5.26 mW/°C	6.25 mW/°C

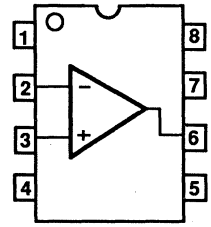
Connection Information

8-Lead TO-99 Metal Can (Top View)



65-03205A

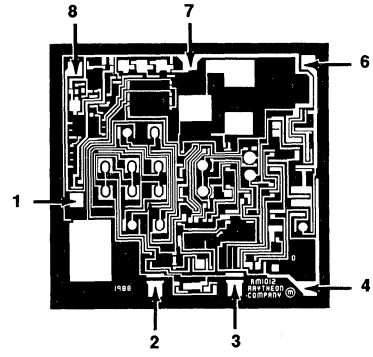
8-Lead Dual In-Line Package (Top View)



65-03206A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Mask Pattern



Die Size: 75 x 78 mils
Min. Pad Dimensions: 4 x 4 mils

65-4238

Electrical Characteristics (V_S = ±15V and T_A = +25°C, unless otherwise noted)

Parameters	Test Conditions	LT-1012M Min	LT-1012M Typ	LT-1012M Max	LT-1012C Min	LT-1012C Typ	LT-1012C Max	Units
Input Offset Voltage[1]			7.0	35		10	50	µV
	See Note 2		20	90		25	120	
Long Term Input Offset Voltage Stability[4,5]			0.2			0.2		µV/Mo
Input Offset Current			20	100		20	150	pA
	See Note 2		30	150		30	200	
Input Bias Current			±20	±100		±20	±150	pA
	See Note 2		±30	±150		±30	±200	
Input Noise Voltage[3]	0.1 Hz to 10 Hz		0.5			0.5		μV_{p-p}
Input Noise Voltage Density[3,6]	F_O = 10 Hz		17	30		17	30	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		14	22		14	22	
Input Noise Current[3]	0.1 Hz to 10 Hz		20			20		$fA/\sqrt{Hz}$
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	114	130		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	114	130		110	126		dB
Large Signal Voltage Gain	$R_L \geq 10\ k\Omega$, V_O = ±12V	300	2000		200	1500		V/mV
	$R_L \geq 2\ k\Omega$, V_O = ±10V	200	1000		120	1200		
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±13	±14		±13	±14		V
Slew Rate	$R_L \geq 2\ k\Omega$	0.1	0.3		0.1	0.3		V/µS
Unity Gain Bandwidth	A_{VCL} = +1.0	0.4	0.8		0.4	0.8		MHz
Supply Current	See Note 2		400	600		400	600	µA

Notes:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. LT-1012M grade is measured after the device is fully warmed up.
2. These specifications apply for $\pm 2.5V \leq V_S \leq \pm 20V$ and $-13V \leq V_{CM} \leq +13V$ (at V_S = ±15V).
3. This parameter is tested on a sample basis only.
4. This parameter is guaranteed by design.
5. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
6. 10 Hz input noise voltage density is sample tested on every lot. Devices 100% tested at 10 Hz are available on request.

Electrical Characteristics (V_S = ±15V, 0°C ≤ T_A ≤ +70°C for LT-1012C and -55°C ≤ T_A ≤ +125°C for LT-1012M unless otherwise noted)

Parameters	Test Conditions	LT-1012M Min	LT-1012M Typ	LT-1012M Max	LT-1012C Min	LT-1012C Typ	LT-1012C Max	Units
Input Offset Voltage[1]			30	180		20	120	µV
	See Note 2		40	250		30	200	
Average Input Offset Voltage Drift			0.2	1.5		0.2	1.5	µV/°C
Input Offset Current			30	250		20	230	pA
	See Note 2		70	350		40	300	
Average Input Offset Current Drift[3]			0.3	2.5		0.3	2.5	pA/°C
Input Bias Current			±80	±600		±35	±230	pA
	See Note 2		±150	±800		±50	±300	
Average Input Bias Current Drift[3]			0.6	6.0		0.3	2.5	pA/°C
Input Voltage Range		±13			±13			V
Common Mode Rejection Ratio	V_{CM} = ±13V	108	126		108	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	108	126		108	126		dB
Large Signal Voltage Gain	R_L ≥ 10 kΩ, V_{OUT} = ±12V	150	1000		150	1500		V/mV
	R_L ≥ 2 kΩ, V_{OUT} = ±10V	100	600		100	800		
Output Voltage Swing	R_L ≥ 10 kΩ	±13	±14		±13	±14		V
Supply Current	R_L = ∞		450	800		450	800	µA

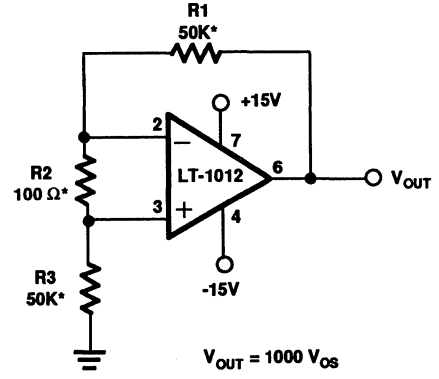
Notes:
1. Input offset voltage measurements are performed by automatic test equipment approximately 0.5 seconds after the application of power. The LT-1012M grade is tested fully warmed up.
2. These specifications apply for ±3V ≤ V_S ≤ ±20V and -13V ≤ V_{CM} ≤ 13V (at V_S = ±15V).
3. This parameter is tested on a sample basis only.

Applications Information

The LT-1012 units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT-1012 can also be used in 741 applications provided that the nulling circuitry is removed.

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

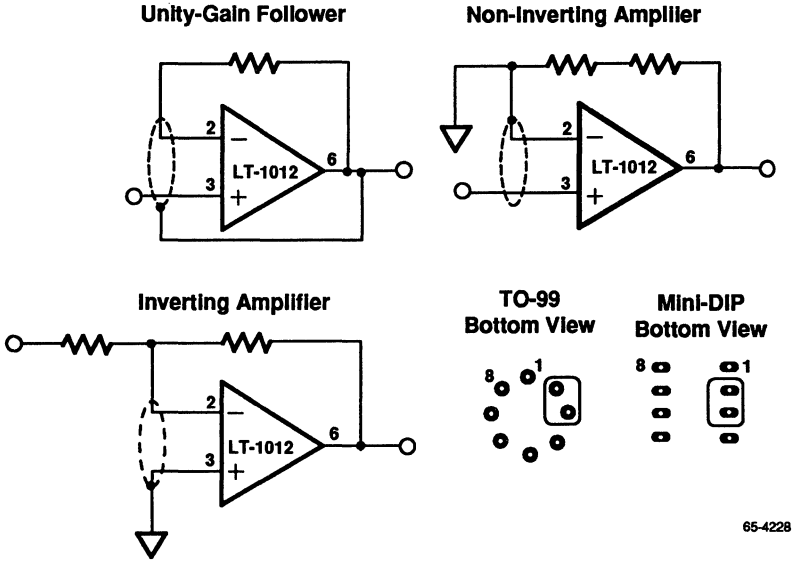
Input bias currents may flow either into or out of the input terminals, depending on the value of I_{OS}. In high-source impedance applications, the pc board layout includes guard rings and must be well cleaned of solder flux. Teflon sockets may aid in keeping leakage currents low.



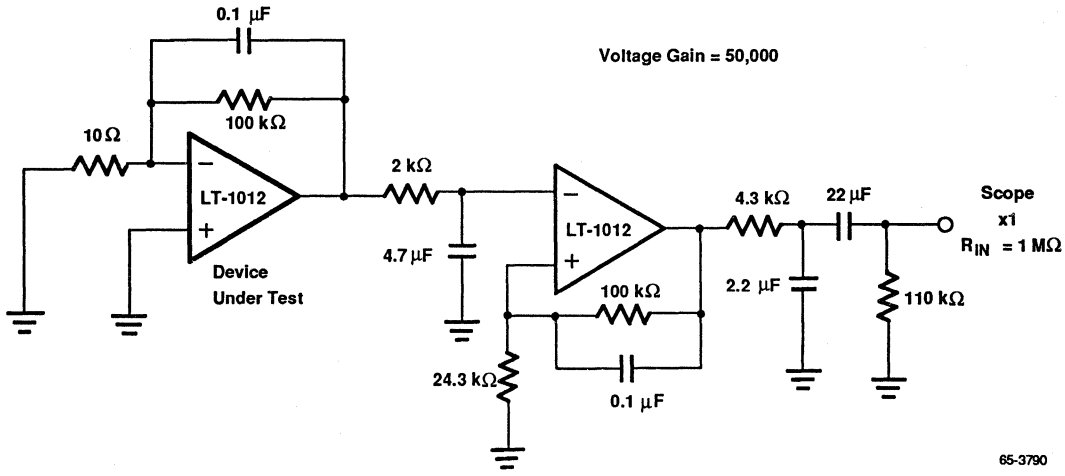
* Resistors must have low thermoelectric potential.

65-3787

Test Circuit for Offset Voltage and Its Drift With Temperature



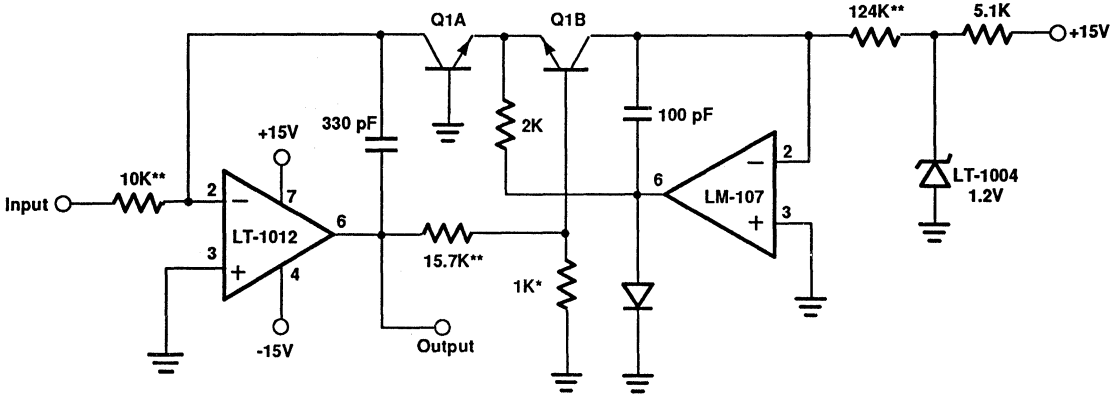
Guard Ring Layout and Connections



1. Peak-to-peak noise is measued in a 10-second interval.
2. The device under test should be warmed up for 3 minutes and shielded from air currents.

0.1 Hz to 10 Hz Noise Test Circuit

Typical Applications



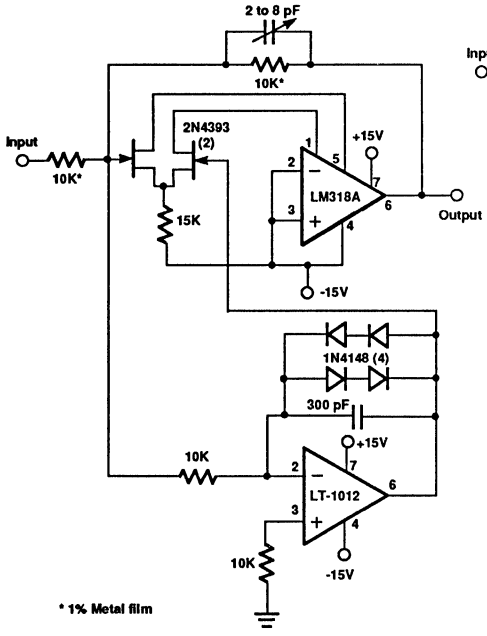
* Tel. labs, type Q81
** 1% Film resistor
Q1 = 2N2979

Low bias current and offset voltage of the LT-1012 allow 4.5 decades of voltage input logging.

65-4230

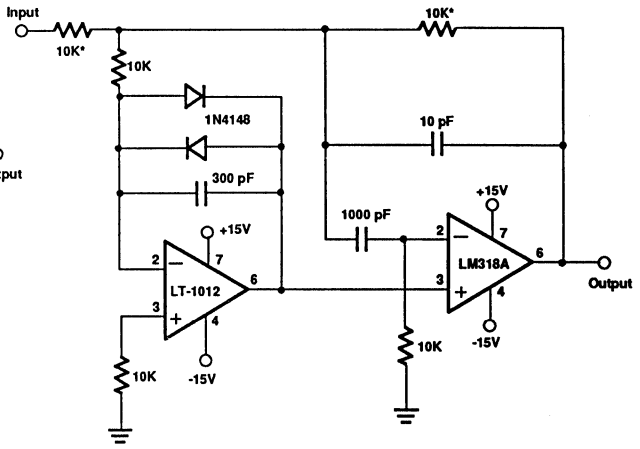
Logarithmic Amplifier

Typical Applications (Continued)



* 1% Metal film

Slew rate @ 100V/μS
Settling = 5 μS to 0.1%/10V step
Offset voltage = 30 μV
Bias current = 30 pA



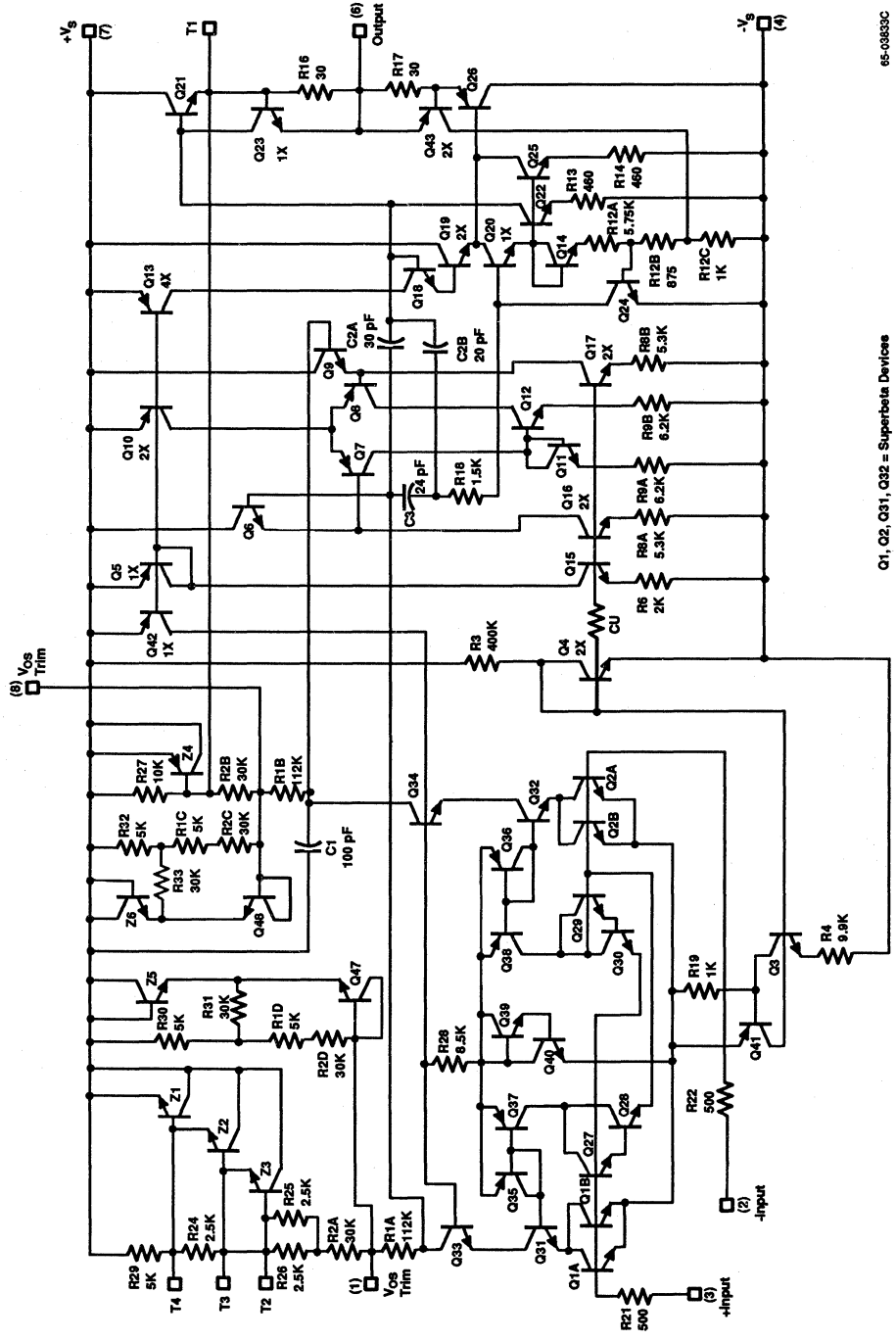
* 1% Metal film

Full power bandwith = 2 MHz
Slew rate = 50V/ μS
Settling (10V step) = 12 μS to 0.01%
Bias current dc = 30 pA
Offset drift = 0.3 μV/°C
Offset voltage = 30 μV

Fast Precision Inverters

65-4231

Schematic Diagram



OP-07 Series Instrumentation Grade Operational Amplifier

Features

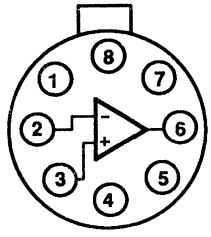
- Low noise 0.1 Hz to 10 Hz — 0.35 μV_{p-p}
- Ultra-low V_{OS} — 10 μV
- Ultra-low V_{OS} drift — 0.2 $\mu V/^{\circ}C$
- Fits 725, 108A, 741, and AD510 sockets
- Long term stability — 0.2 μV/Month
- Low input bias current — ±1 nA
- High CMRR — 126 dB
- Wide input voltage range — ±14V
- Wide supply voltage range — ±3V to ±22V

Description

The OP-07 amplifier series is designed for precision low level signal conditioning where ultra low V_{OS} and TCV_{OS} are required along with very low bias currents. Internal compensation eliminates the need for external components. Novel circuit design and tight process controls are used to obtain very low values of V_{OS}. V_{OS} is further reduced by a computer controlled digital nulling techniques at test. Low frequency noise is minimized. Internal biasing techniques reduce external bias and offset currents to values in the order of ±1 nA over the military temperature range. OP-07s are direct replacements for the 108A, 714, 725 and 5507. They can replace chopper stabilized amplifiers in many applications.

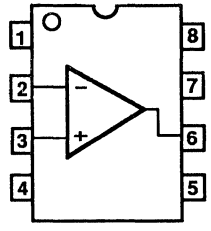
Connection Information

8-Lead TO-99 Metal Can
(Top View)



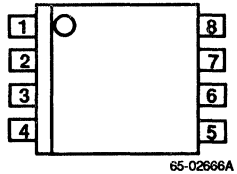
65-03205A

8-Lead Dual In-Line Package
(Top View)



65-03206A

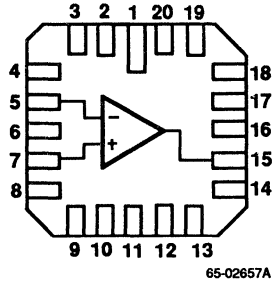
8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

20-Pad LCC
(Top View)



65-02657A

Pin	Function
2	V_{OS} Trim
5	-Input
7	+Input
10	$-V_S$
15	Output
17	$+V_S$
20	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
OP-07CT	T	0°C to +70°C
OP-07DT	T	0°C to +70°C
OP-07ET	T	0°C to +70°C
OP-07CD	D	0°C to +70°C
OP-07DD	D	0°C to +70°C
OP-07ED	D	0°C to +70°C
OP-07CN	N	0°C to +70°C
OP-07DN	N	0°C to +70°C
OP-07EN	N	0°C to +70°C
OP-07CM	M	0°C to +70°C
OP-07DM	M	0°C to +70°C
OP-07EM	M	0°C to +70°C
OP-07T	T	-55°C to +125°C
OP-07T/883B	T	-55°C to +125°C
OP-07AT	T	-55°C to +125°C
OP-07AT/883B	T	-55°C to +125°C
OP-07D	D	-55°C to +125°C
OP-07D/883B	D	-55°C to +125°C
OP-07AD	D	-55°C to +125°C
OP-07AD/883B	D	-55°C to +125°C
OP-07L	L	-55°C to +125°C
OP-07L/883B	L	-55°C to +125°C
OP-07AL	L	-55°C to +125°C
OP-07AL/883B	L	-55°C to +125°C

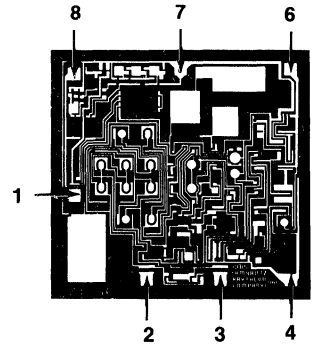
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
OP-07A ..... -55°C to +125°C
OP-07E/C/D ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8; 10 sec) ..... +260°C
(DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



Die Size: 75 x 78 mils
Min . Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	20-Pad LCC	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Small Outline	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	175°C	125°C	125°C
Max. P_D T_A <50°C	925 mW	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	37°C/W	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	105°C/W	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	7.0 mW/°C	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			10	25		30	75	μV
Long Term Input Offset Voltage Stability[3] [4]			0.2	1.0		0.2	1.0	μV/Mo
Input Offset Current			0.3	2.0		0.4	2.8	nA
Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100Hz		10	13		10	13	
	f_O = 1000Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		14	30	pA_{p-p}
Input Noise Current Density[2]	f_O = 10Hz		0.32	0.80		0.32	0.80	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100Hz		0.14	0.23		0.14	0.23	
	f_O = 1000Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	80		20	60		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	300	500		200	500		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500k\Omega$, V_O = ±0.5V, V_S = ±3V	150	500		150	500		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12.5	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±12	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12		±10.5	±12		
Slew Rate	$R_L \geq 2k\Omega$	0.1	0.3		0.1	0.3		V/μS
Unity Gain Bandwidth	A_{VCL} = +1.0		0.8			0.8		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V		75	120		75	120	mW
	V_S = ±3V		4.0	6.0		4.0	6.0	
Offset Adjustment Range	R_P = 20kΩ		±4.0			±4.0		mV

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. OP-07A is tested fully warmed up.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.
4. Long Term Input Offset Voltage Stability refers to the average trend line of V_{os} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{os} during the first 30 operating days are typically 2.5 μV.

Electrical Characteristics (Continued)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	75		60	150		60	150	μV
Long Term Input Offset Voltage Stability[3,4]			0.3	1.5		0.4	2.0		0.5	3.0	$\mu V/Mo$
Input Offset Current			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage[2]	0.1Hz to 10Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
Input Noise Voltage Density[2]	f_O = 10Hz		10.3	18		10.5	20		10.5	20	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100Hz		10	13		10.2	13.5		10.2	13.5	
	f_O = 1000Hz		9.6	11		9.8	11.5		9.8	11.5	
Input Noise Current[2]	0.1Hz to 10Hz		14	30		15	35		15	35	pA_{p-p}
Input Noise Current Density[2]	f_O = 10Hz		0.32	0.8		0.35	0.9		0.35	0.9	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100Hz		0.14	0.23		0.15	0.27		0.15	0.27	
	f_O = 1000Hz		0.12	0.17		0.13	0.18		0.13	0.18	
Input Resistance (Diff. Mode)[3]		15	50		8.0	33		7.0	31		MΩ
Input Resistance (Com. Mode)			160			120			120		GΩ
Input Voltage Range		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	200	500		120	400		120	400		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500\Omega$, V_O = ±0.5V, V_S = ±3.0V	150	500		100	400			400		
Output Voltage Swing	$R_L \geq 10k\Omega$	±12.5	±13		±12	±13		±12	±13		V
	$R_L \geq 2k\Omega$	±12	±12.8		±11.5	±12.8		±11.5	±12.8		
	$R_L \geq 1k\Omega$	±10.5	±12			±12					
Slew Rate	$R_L \geq 2k\Omega$	0.1	**0.3**		0.1	**0.3**		0.1	**0.3**		$V/\mu S$
Unity Gain Bandwidth	A_{VCL} = +1.0		**0.8**			**0.8**			**0.8**		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60			60		Ω
Power Consumption	V_S = ±15V		75	120		80	150		80	150	mW
	V_S = ±3.0V		4.0	6.0		4.0	8.0		4.0	8.0	
Offset Adjustment Range	R_p =20kΩ		±4.0			±4.0			±4.0		mV

See footnotes on page 3.

Electrical Characteristics (Continued)

(V_S = ±15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			25	60		60	200	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.2	0.6		0.3	1.3	μV/°C
With External Trim[3]	R_p = 20kΩ		0.2	0.6		0.3	1.3	
Input Offset Current			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift[2]			5.0	25		8.0	50	pA/°C
Input Bias Current			±1.0	±4.0		±2.0	±6.0	nA
Average Input Bias Current Drift[2]			8.0	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	94	106		94	106		dB
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_O = ±10V	200	400		150	400		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±12	±12.6		±12	±12.6		V

Notes: 1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.

Electrical Characteristics (Continued)

(V_S = ±15V and 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			45	130		85	250		85	250	μV
Average Input Offset Voltage Drift Without External Trim[2]			0.3	1.3		0.5	1.8		0.7	2.5	μV/°C
With External Trim[3]	R_P = 20kΩ		0.3	1.3		0.4	1.6		0.7	2.5	μV/°C
Input Offset Current			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift[2]			8.0	35		12	50		12	50	pA/°C
Input Bias Current			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift[2]			13	35		18	50		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	90	104		86	100		86	100		dB
Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	180	450		100	400		100	400		V/mV
Output Voltage Swing	R_L = 2kΩ	±12	±12.6		±11	±12.6		±11	±12.6		V

Notes: 1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.

Digital Nulling Technique

The digital nulling technique involves the zener diode nulling network of Figure 1. The zener diodes have relatively high breakdown voltages and never operate in the zener mode. The purpose of the zeners is to short out resistors R1, 2R1, 4R1, or 8R1 by forcing a high reverse current through the diode to metalize the junction. The input offset voltage can be adjusted by varying the collector resistor ratio. If the difference in the two collector resistors (R_C) is a small increment ΔR_C, V_{OS} can be written as:

$$V_{OS} = V_T \ln \frac{R_C + \Delta R_C}{R_C} = V_T \ln\ 1 + \frac{\Delta R_C}{R_C}$$

for $\Delta R_C/R_C \ll 1.0$ $\ln(1+\Delta R_C/R_C) \approx \Delta R_C/R_C$, thus:

$$V_{OS} \approx V_T \frac{\Delta R_C}{R_C}$$

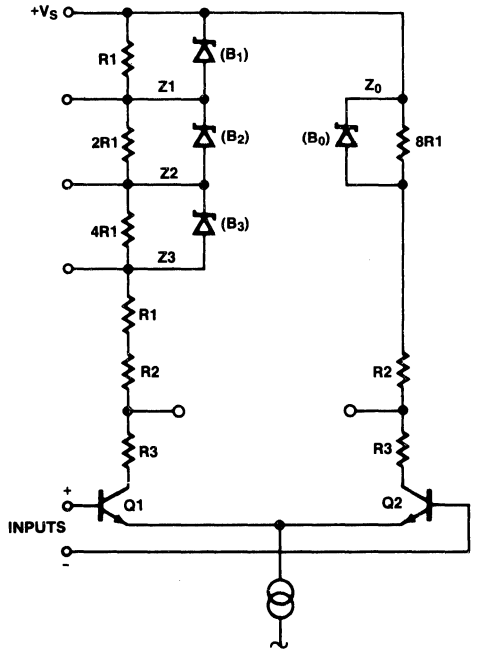
For Figure 1 R2 + R3 ≫ 8R1, thus

$$V_{OS} \approx -V_T \frac{R_1}{8R1 + R2 + R3} (7 - B_3B_2B_1) \quad (B_0 = 1)$$

or:

$$V_{OS} \approx V_T \frac{R1}{R2 + R3} \quad (1 + B_3B_2B_1) \quad (B_0 = 0)$$

where $B_3B_2B_1$ is a binary number which corresponds to the state of zener diodes Z1, Z2 and Z3 as per Figure 1.



65-00365A

Figure 1. Digital Nulling Network

$$\Delta V_{OS}(25°C) \approx \frac{-2.6mV\ (7 - B_3B_2B_1)R1}{8R1 + R2 + R3} \quad (B_0 = 1.0)$$

$B_n = 1.0$ for Z_n unshorted.

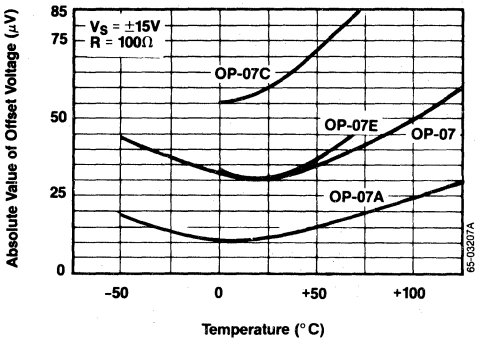
$B_n = 0$ for Z_n shorted.

$B_1B_2B_3$ = Binary number with values from 0 to 7.

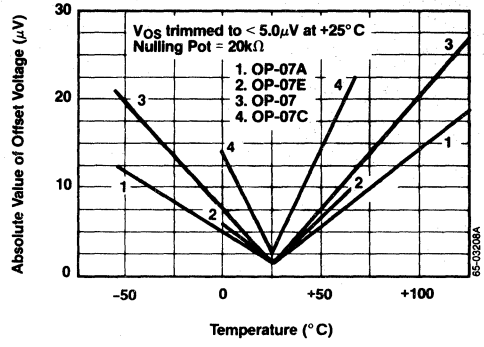
$$\Delta V_{OS}(25°C) \approx \frac{2.6mV\ (1 + B_3B_2B_1)R1}{R2 + R3} \quad (B_0 = 0)$$

Typical Performance Characteristics

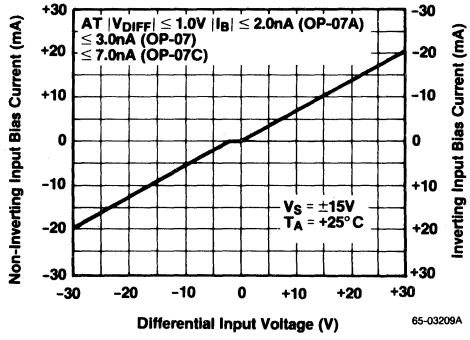
Untrimmed Offset Voltage vs. Temperature



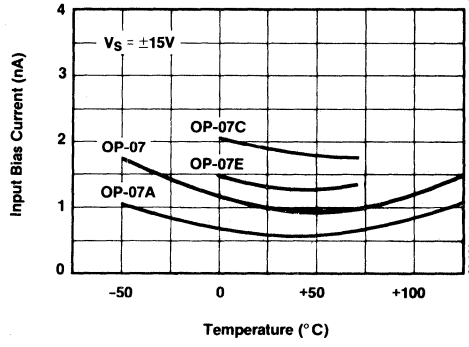
Trimmed Offset Voltage vs. Temperature



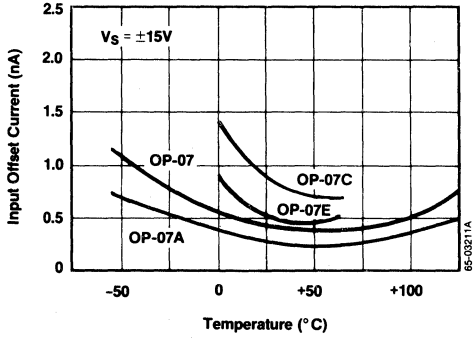
Input Bias Current vs. Differential Input Voltage



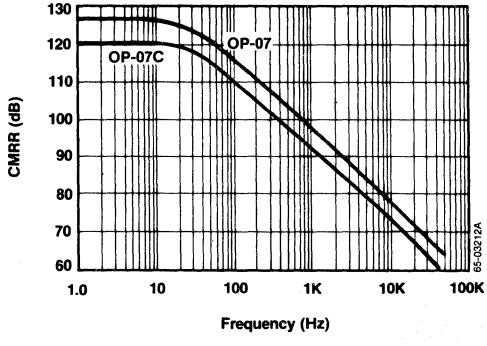
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature

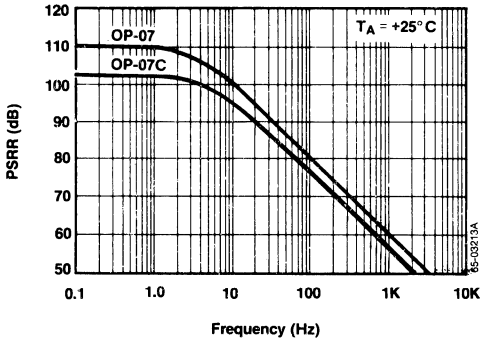


CMRR vs. Frequency

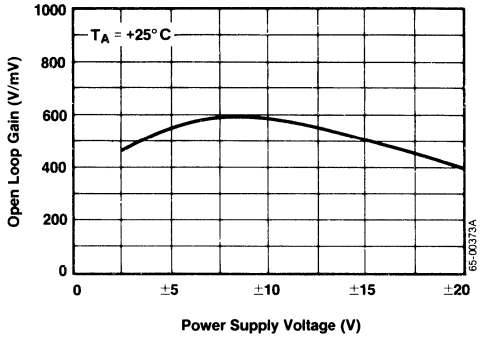


Typical Performance Characteristics (Continued)

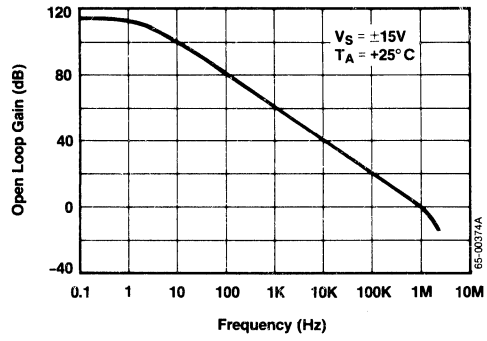
PSRR vs. Frequency



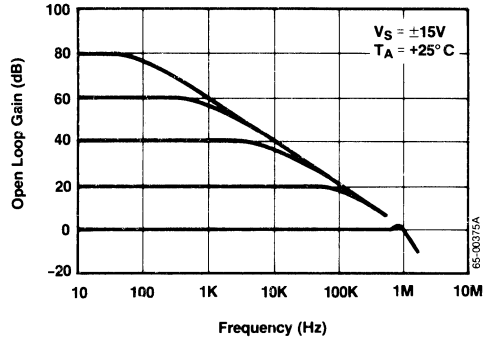
Open Loop Gain vs. Supply Voltage



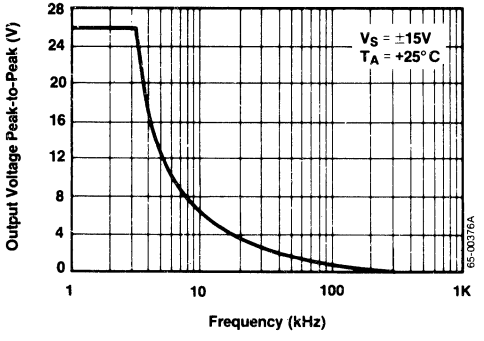
Open Loop Frequency Response



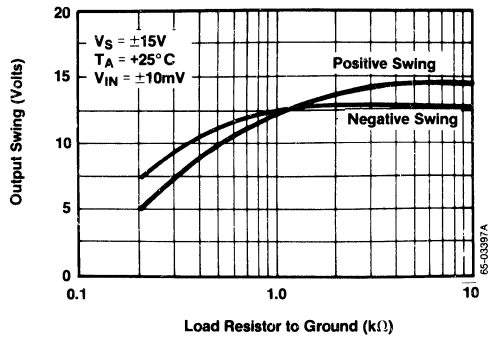
Closed Loop Response for Various Gain Configurations



Maximum Undistorted Output vs. Frequency

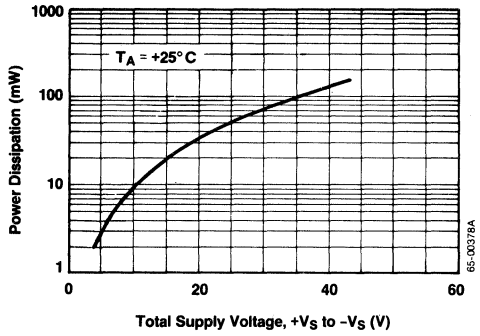


Output Voltage vs. Load Resistance

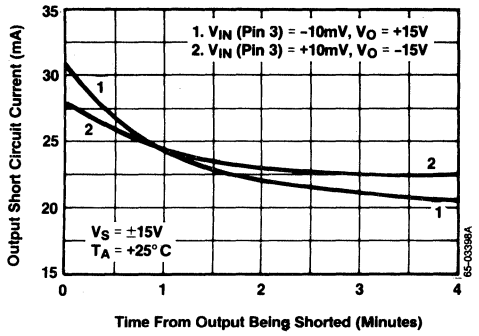


Typical Performance Characteristics (Continued)

Power Consumption vs. Supply Voltage

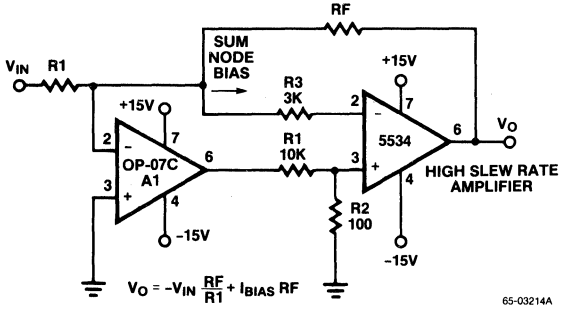


Output Short Circuit Current vs. Time

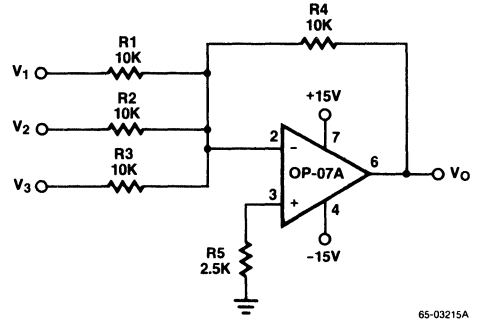


Typical Applications

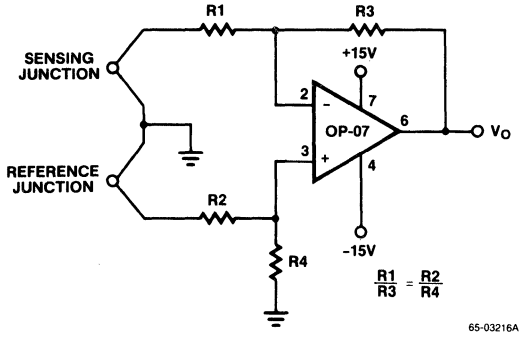
High Speed, Low V_{OS} Composite Amplifier*



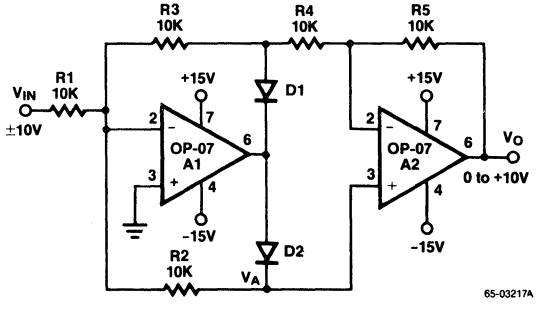
Adjustment-Free Precision Summing Amplifier*



High Stability Thermocouple Amplifier*

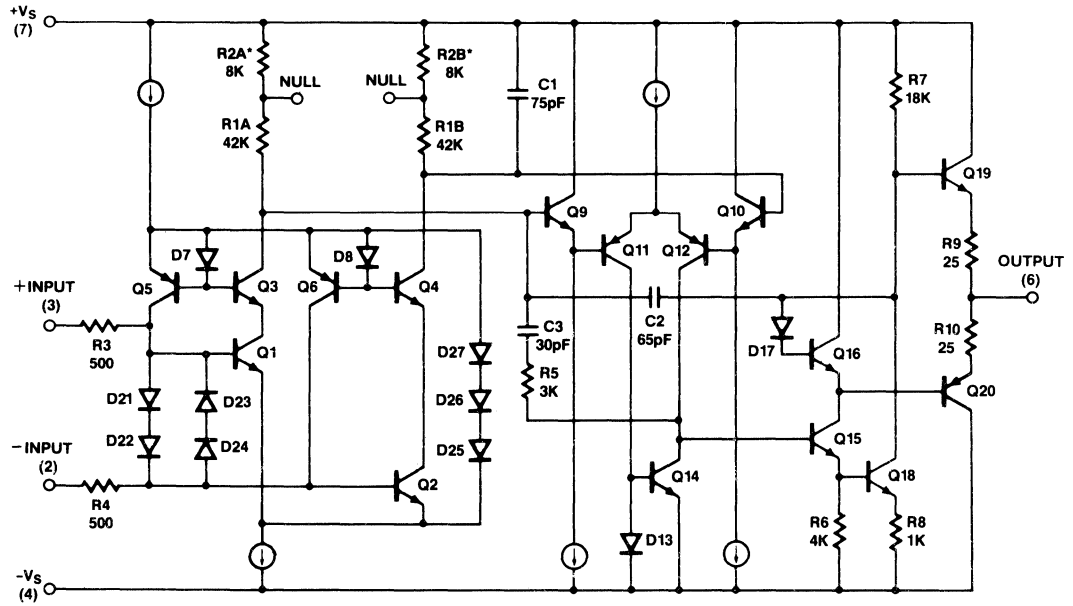


Precision Absolute Value Circuit*



*Pin outs shown for metal can packages

Schematic Diagram



*R2A and R2B are electronically adjusted during factory test for minimum V_{OS}.

65-00362B

OP-27 Low Noise Operational Amplifier

Features

- Very low noise
  Spectral noise density — 3.0 nV/ Hz
  1/f noise corner frequency — 2.7 Hz
- Very low V_{os} drift
  0.2 µV/Mo
  0.2 µV/°C
- High gain — 1.8 x 106 V/V
- High output drive capability — ±12V into 600 load
- High slew rate —2.8 V/µS
- Wide gain bandwidth product — 8 MHz
- Good common mode rejection ratio — 126 dB
- Low input offset voltage — 10 µV
- Minimum low frequency noise — 0.08 μV_{p-p}
  0.1 Hz to 10 Hz
- Low input bias and offset currents — 10 nA

Description

The OP-27 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. These features are all available in a device which is internally compensated for excellent phase margin (70°) in a unity gain configuration.

Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 25 µV. Input bias current cancellation techniques are used to obtain 10 nA input bias currents.

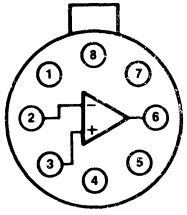
The OP-27 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120 dB. A phase margin of 70° at unity gain guards against peaking (and ringing) in low gain feedback circuits. Stable operation can be obtained with capacitive loads up to 2000 pF*. Input offset voltage can be externally trimmed without affecting input offset voltage drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metal at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The OP-27 is available in LCC, SO-8 (small-outline), TO-99 can, plastic mini-DIP and ceramic mini-DIP packages, and can be ordered with Mil-Std-883 Level B processing.

*By decoupling the load capacitance with a series resistor of 50 or more, load capacitances larger than 2000 pF can be accommodated.

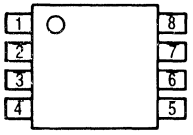
Connection Information

8-Lead TO-99 Metal Can
(Top View)



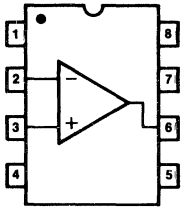
65-03205A

8-Lead Plastic Dual In-Line SO
(Top View)



65-02666A

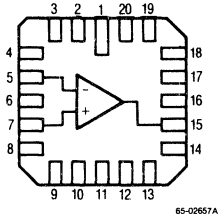
8-Lead Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

20-Pad LCC



65-02657A

Pin	Function
2	V_{OS} Trim
5	-Input
7	+Input
10	$-V_S$
15	Output
17	$+V_S$
20	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
OP-27EN	N	0°C to +70°C
OP-27FN	N	0°C to +70°C
OP-27GN	N	0°C to +70°C
OP-27EM	M	0°C to +70°C
OP-27FM	M	0°C to +70°C
OP-27GM	M	0°C to +70°C
OP-27ED	D	-25°C to +85°C
OP-27FD	D	-25°C to +85°C
OP-27GD	D	-25°C to +85°C
OP-27ET	T	-25°C to +85°C
OP-27FT	T	-25°C to +85°C
OP-27GT	T	-25°C to +85°C
OP-27AD	D	-55°C to +125°C
OP-27AD/883	D	-55°C to +125°C
OP-27BD	D	-55°C to +125°C
OP-27BD/883	D	-55°C to +125°C
OP-27CD	D	-55°C to +125°C
OP-27CD/883	D	-55°C to +125°C
OP-27AT	T	-55°C to +125°C
OP-27AT/883	T	-55°C to +125°C
OP-27BT	T	-55°C to +125°C
OP-27BT/883	T	-55°C to +125°C
OP-27CT	T	-55°C to +125°C
OP-27CT/883	T	-55°C to +125°C
OP-27AL/883	L	-55°C to +125°C
OP-27BL/883	L	-55°C to +125°C

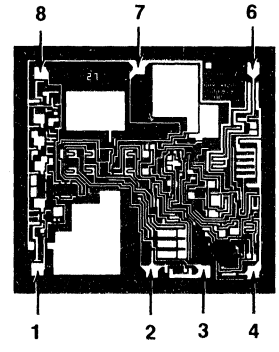
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation** ..... 658 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-27A/B/C ..... -55°C to +125°C
OP-27E/F/G (Hermetic) ..... -25°C to +85°C
OP-27E/F/G (Plastic) ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8, 10 sec) ..... +260°C
(DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



65-01540A

Die Size: 75 × 80 mils
Min. Pad Dimensions: 4 × 4 mils

Thermal Characteristics

	8-Lead Small Outline	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	20-Pad LCC	8-Lead Plastic DIP
Max. Junction Temp.	125°C	175°C	175°C	175°C	125°C
Max. P_D T_A <50°C	300 mW	833 mW	658 mW	925 mW	468 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W	37°C/W	—
Therm. Res. θ_{JA}	240°C/W	150°C/W	190°C/W	105°C/W	160°C/W
For T_A >50°C Derate at	4.17 mW/°C	8.33 mW/°C	5.26 mW/°C	7.0 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-27A/E			OP-27B/F			OP-27C/G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			10	25		20	60		30	100	µV
Long Term Input Offset Voltage Stability[1,4]			0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current			7.0	35		9.0	50		12	75	nA
Input Bias Current			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.08	0.18		0.08	0.18		0.09	0.25	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		3.5	5.5		3.5	5.5		3.8	8.0	nV/Hz
	F_O = 30 Hz		3.1	4.5		3.1	4.5		3.3	5.6	
	F_O = 1000 Hz		3.0	3.8		3.0	3.8		3.2	4.5	
Input Noise Current Density[2]	F_O = 10 Hz		1.7	4.0		1.7	4.0		1.7		pA/Hz
	F_O = 30 Hz		1.0	2.3		1.0	2.3		1.0		
	F_O = 1000 Hz		0.4	0.6		0.4	0.6		0.4	0.6	
Input Resistance (Diff. Mode)[4]		1.5	6.0		1.2	5.0		0.8	4.0		M
Input Resistance (Com. Mode)			3.0			2.5			2.0		G
Input Voltage Range[3]		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	V_S ±4V to ±18V	100	120		120	120		94	118		dB
Large Signal Voltage Gain	$R_L \geq 2$ k, V_O = ±10V	1000	1800		1000	1800		700	1500		V/mV
	$R_L \geq 1$ kΩ, V_O = ±10V	800	1500		800	1500			1500		
	V_O = ±1V, V_S = ±4V[4]	250	700		250	700		200	500		
Output Voltage Swing	$R_L \geq 2$ k,	±12	±13.8		±12	±13.8		±11.5	±13.5		V
	$R_L \geq 600$,	±11	±12		±11	±12		±11	±12		
Slew Rate[4]	$R_L \geq 2$ k,	1.7	2.8		1.7	2.8		1.7	2.8		V/µS
Gain Bandwidth Product[4]		5.0	8.0		5.0	8.0		5.0	8.0		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		70			70			70		Ω
Power Consumption			90	140		90	140		100	170	mW
Offset Adjustment Range	R_p = 10 k		±4.0			±4.0			±4.0		mV

Notes:

1. Long Term Input Offset Voltage Supply refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. This parameter is tested on a sample basis only.
3. Caution: The Common Mode Input Range is a function of supply voltage. See Typical Performance Curves. Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed but not tested.
5. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-27A			OP-27B			OP-27C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	60		50	200		70	300	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			15	50		22	85		30	135	nA
Input Bias Current			±20	±60		±28	±95		±35	±150	nA
Input Voltage Range		±10.3	±11.5		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	V_S ±4.5V to ±18V	96	116		94	114		86	110		dB
Large Signal Voltage Gain	R_L ≥ 2 k , V_O = ±10V	600	1200		500	1000		300	800		V/mV
Output Voltage Swing	R_L ≥2 k	±11.5	±13.5		±11	±13.2		±10.5	±13		V

Electrical Characteristics (V_S = ±15V, -25°C ≤ T_A ≤ +85°C for hermetic package types, 0°C ≤ T_A ≤ +70°C for plastic packages unless otherwise noted)

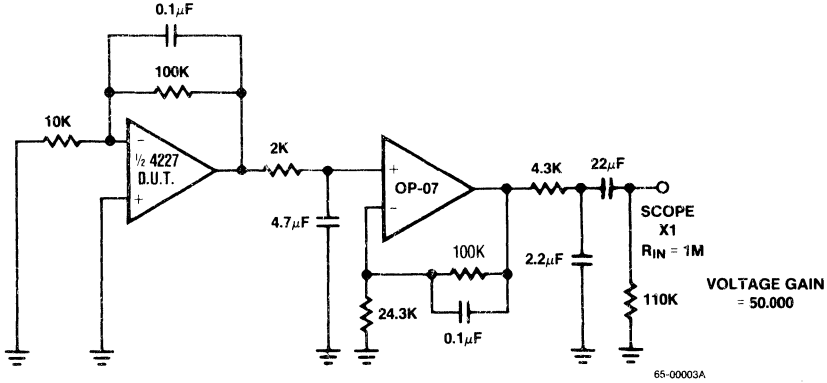
Parameters	Test Conditions	OP-27E			OP-27F			OP-27G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	50		40	140		55	220	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			10	50		14	85		20	135	nA
Input Bias Current			±10	±40		±12	±55		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		102	121		96	118		dB
Power Supply Rejection Ratio	V_S ±4.5V to ±18V	97	118		96	116		90	114		dB
Large Signal Voltage Gain	R_L ≥ 2 k , V_O = ±10V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	R_L ≥2 k	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

Notes:

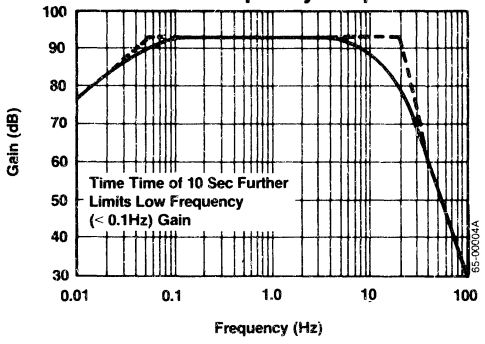
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed unnulled or when nulled with R_P = 8.0 k to 20 k .

Typical Performance Characteristics

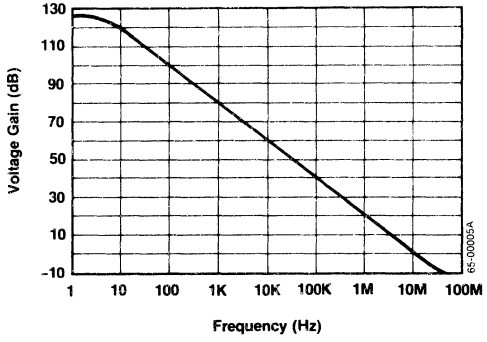
0.1Hz to 10Hz Noise Test Circuit



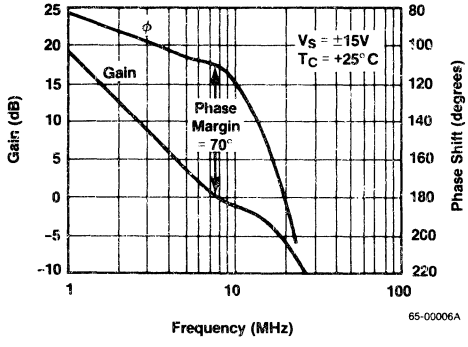
0.1Hz to 10Hz Peak-to-Peak Noise Tester Frequency Response



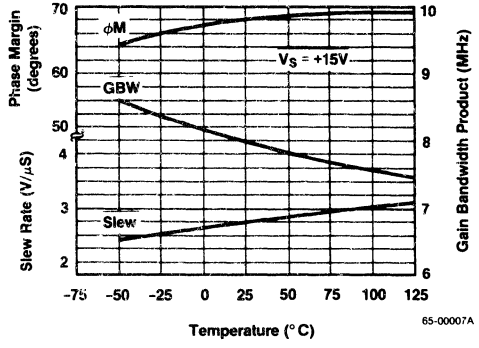
Open Loop Gain vs. Frequency



Gain, Phase Shift vs. Frequency

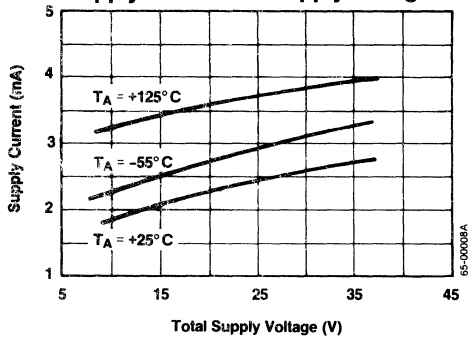


Slew Rate, Gain Bandwidth Product, Phase Margin vs. Temperature

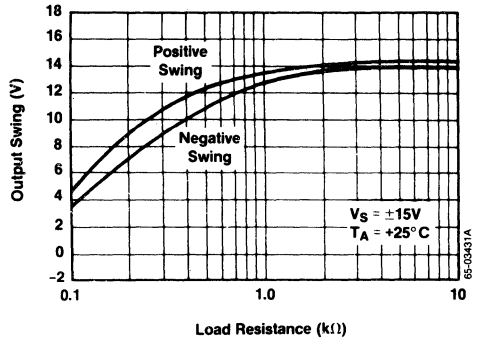


Typical Performance Characteristics (Continued)

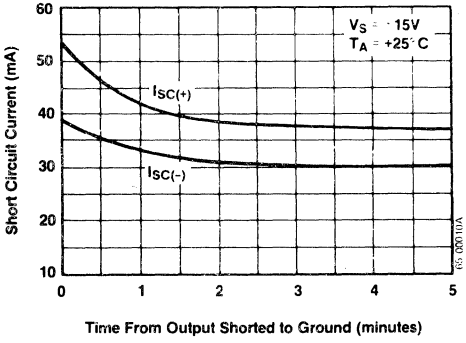
Supply Current vs. Supply Voltage



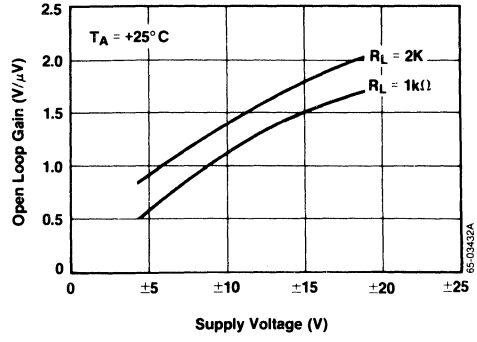
Maximum Output Swing vs. Resistive Load



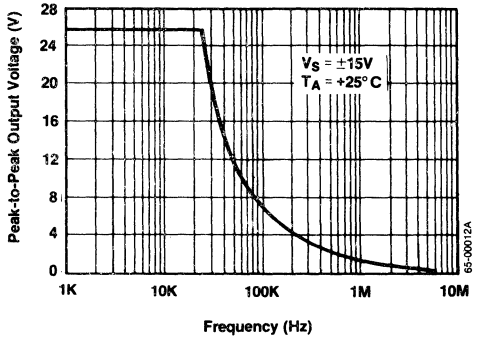
Short Circuit Current vs. Time



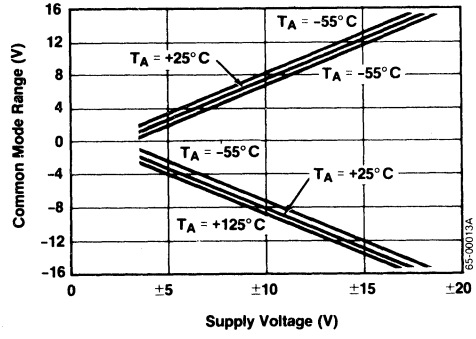
Open Loop Voltage Gain vs. Supply Voltage



Maximum Undistorted Output vs. Frequency

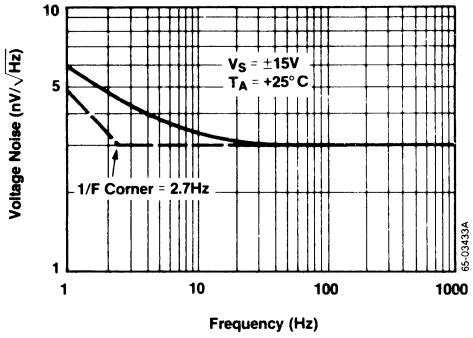


Common Mode Input Range vs. Supply Voltage

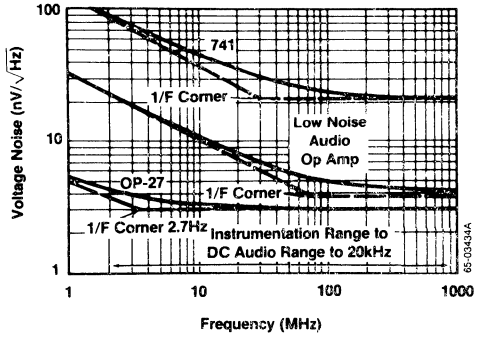


Typical Performance Characteristics (Continued)

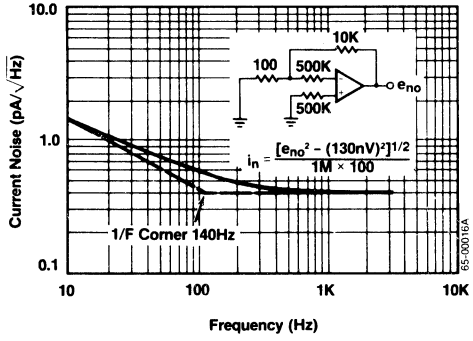
OP-27 Voltage Noise vs. Frequency



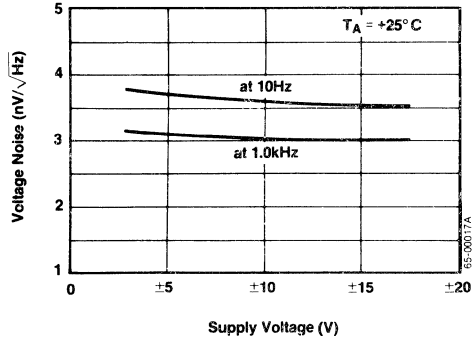
A Comparison of Op Amp Voltage Noise Spectrums



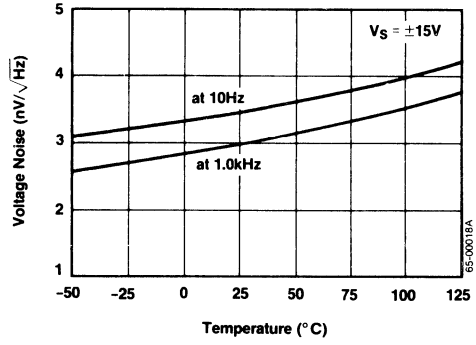
Current Noise vs. Frequency



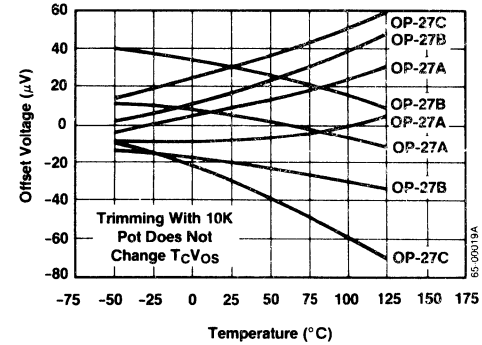
Voltage Noise vs. Supply Voltage



Voltage Noise vs. Temperature

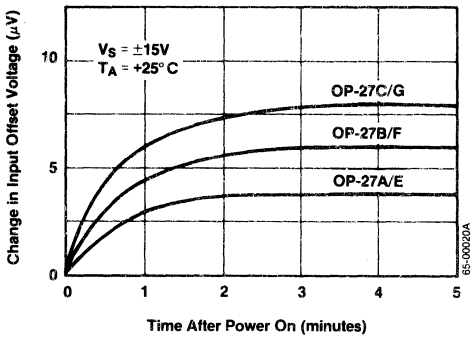


Offset Voltage Drift of Representative Units

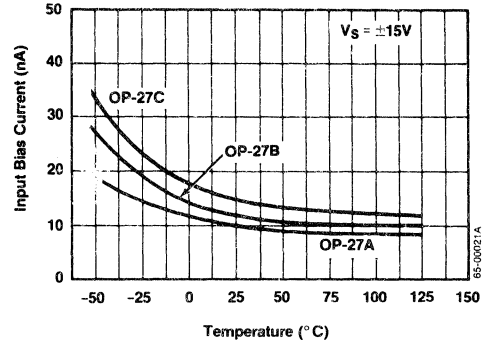


Typical Performance Characteristics (Continued)

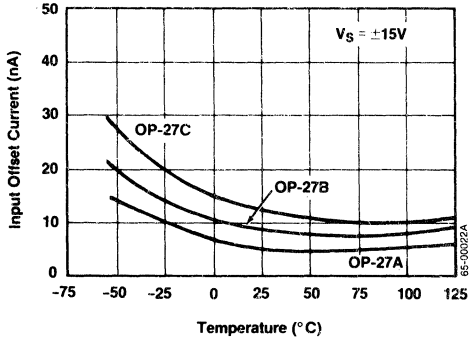
Warm-Up Drift



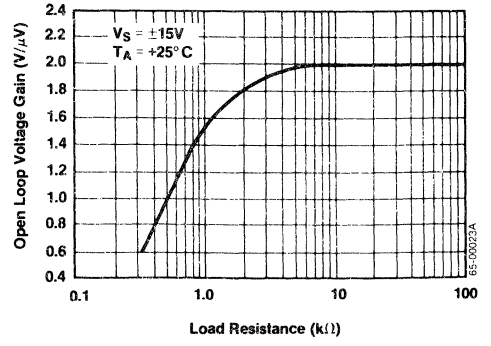
Input Bias Current vs. Temperature



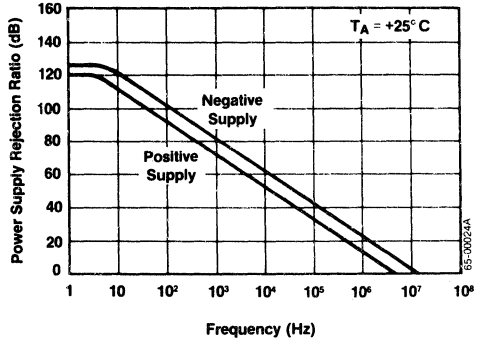
Input Offset Current vs. Temperature



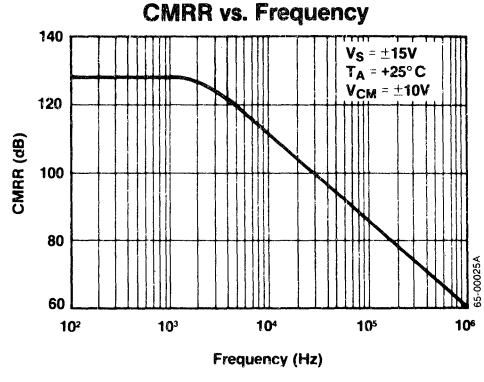
Open Loop Voltage Gain vs. Load Resistance



PSRR vs. Frequency

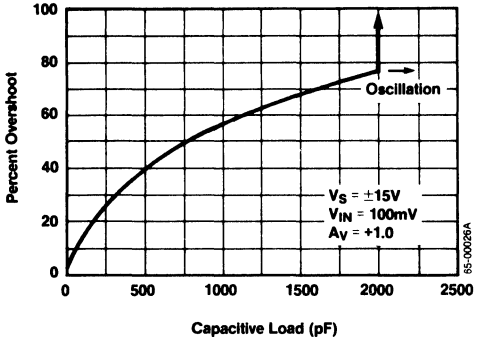


CMRR vs. Frequency

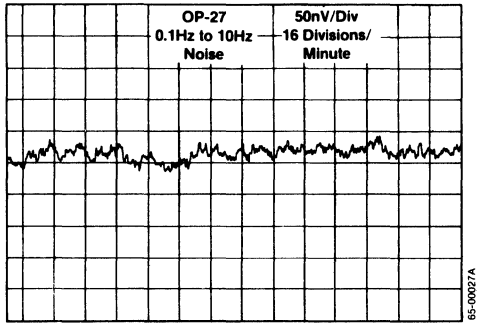


Typical Performance Characteristics (Continued)

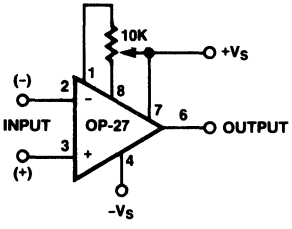
Small Signal Overshoot vs. Capacitive Load



OP-27 0.1Hz to 10Hz Peak-to-Peak Noise
Vertical Scale 50nV/Division
Recorder Speed 16 Divisions/Min

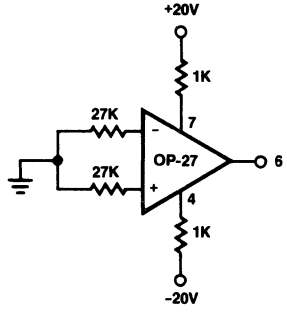


Offset Nulling Circuit



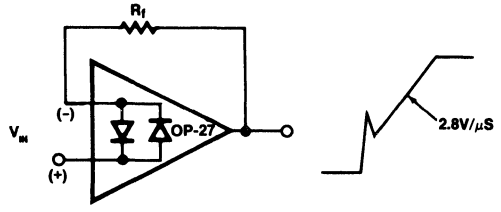
65-00029A

Burn-In Circuit



65-00028A

Large Signal Transient Response



When $R_f \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($\geq$ 1.0V), the output waveform will look as shown.

65-00030A

Typical Applications

RIAA Phono Preamplifier (Figure 1)

The new moving coil magnetic phono cartridges have sensitivities that are an order of magnitude lower than the sensitivity of a typical moving magnet cartridge (0.1 mV per CM/S versus 1.0 mV per CM/S). This places a greater burden on the preamplifier to achieve more gain and less noise. The OP-27 is ideally suited for this task. The object in designing an RIAA phono preamp is to achieve the RIAA gain-frequency response curve while contributing as little noise as possible to avoid masking the very small signal generated by the cartridge. The circuit shown is adjusted to match a 40 dB RIAA curve as shown in Figure 2. Note that by convention the RIAA gain is specified at 1 kHz. With the "break points" of the curves specified at 50,500 and 2.1 kHz respectively the entire curve is fixed by the specified gain at 1kHz.

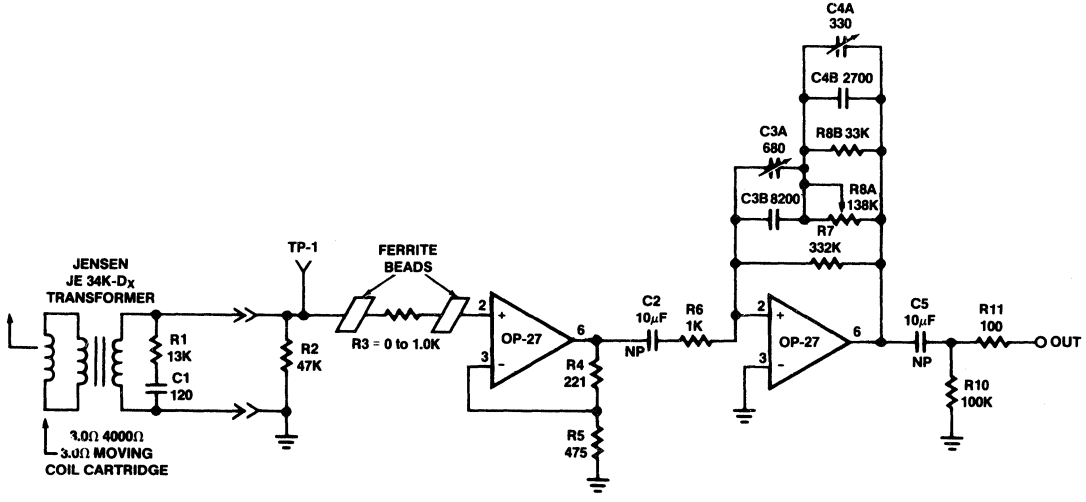
The circuit is designed to operate with a 3/4000Ω step-up transformer to present the optimum source impedance to the amplifier for best noise figure. The optimum source impedance is obtained as the ratio of the spectral noise voltage en to the spectral noise current i_n (when e_n has dimensions of nV/ Hz and i_n has dimensions of pA/√Hz and the ratio has dimensions of kΩ). The circuit is designed to be tested and adjusted independent of the transformer, for this purpose introduce a very low level signal 1 mV at test point TP-1. The first stage is a wideband stage which provides a small amount of gain (1 + R4/R5) approximately equal to 10 dB. Low value feedback resistors must be used to prevent additional noise due to the spectral current noise or excessive Johnson noise. The gain of the first stage reduces the noise contribuition of the second stage. The RIAA transfer curve poles and zeros are due entirely to the feedback network of the second stage.

The poles and zeros of the RIAA feedback network are sufficiently separated in frequency that they may be estimated with the following equations:

$$f_1(50\text{Hz}) \approx \frac{1}{2\pi R7C3}$$

$$f_2(500\text{Hz}) \approx \frac{1}{2\pi R8C3}$$

$$f_3(2100\text{Hz}) \approx \frac{1}{2\pi R8C2}$$



To test, disconnect transformer and inject signal at TP-1.

Figure 1. RIAA Phono Preamplifier

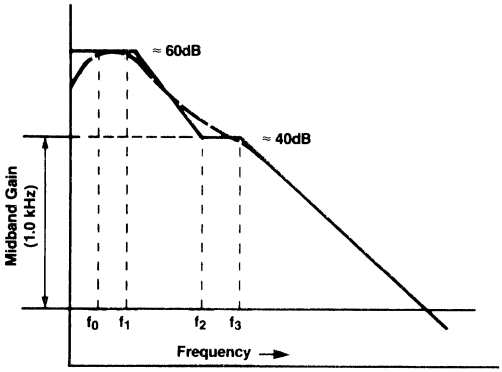


Figure 2. RIAA Phone Playback Equalization Curve

These equations are only approximations. Final tuning is performed with the adjustable capacitors and potentiometers. The following sequence can be used to adjust for the RIAA response after injecting a low level signal into TP-1 (transformer disconnected).

1. At 100 Hz adjust C3A for an output level 6 dB lower than the low frequency output.
2. At 1000 Hz adjust R8A for an output level 20 dB lower than the low frequency output.
3. At 21 kHz adjust C4A for an output 40 dB less than the low frequency output.

Low Impedance Microphone Preamp (Figure 3)

In this preamp the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-27 for best noise performance. The optimum source impedance can be calculated as the ratio of en/in which for the OP-27 is approximately 7000Ω. Fortunately the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value and the source impedance at the output of this transformer, approximately 15 kΩ, still provides near optimum noise performance. (A high quality audio transformer with a step-up ratio of 6.7 to one is not available.) The voltage gain of the amplifier, not including the transformer step-up, is unity up to about 1.5 Hz. It may be desirable to reduce the size of this capacitor to minimize burst noise even though the OP-27 has a 1/f noise corner below 3 Hz. C2 rolls off the high frequency response at 90 kHz giving a noise power bandwidth of 140 kHz.

Instrumentation

The OP-27 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-27 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that it is dominated almost entirely by the resistor Johnson noise.

The three op amp instrumentation amplifier of Figure 8 avoids the low input impedance characteristics of difference amplifiers at the expense of two more operational amplifiers and a slight degradation in noise performance. The noise increases because two amplifiers are contributing to the input voltage spectral noise instead of one. Thus the noise contribution, exclusive of resistor Johnson noise, increases by slightly more than the $\sqrt{2}$. The spectral noise voltage increases from approximately 3 nV/$\sqrt{Hz}$ to approximately 4.9 nV/$\sqrt{Hz}$, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 40 for an overall gain of 1000. R7 is trimmed to optimize the common mode rejection ratio (CMRR) with frequency. With balanced source resistors a CMRR of 100 dB is achieved. With a 1 kΩ source impedance imbalance CMRR is degraded to 80 dB at 5 kHz due to the finite (3 GΩ) input impedance.

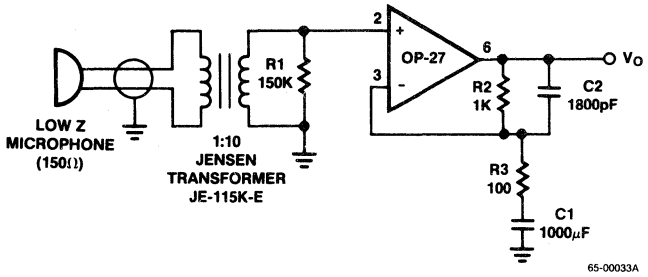


Figure 3. Low Impedance Microphone Preamplifier

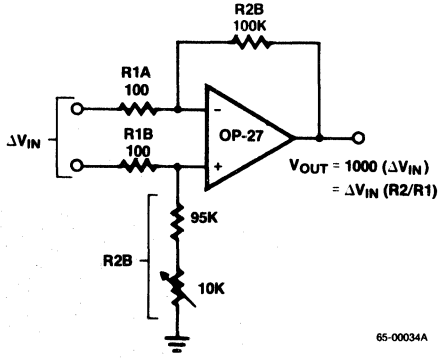
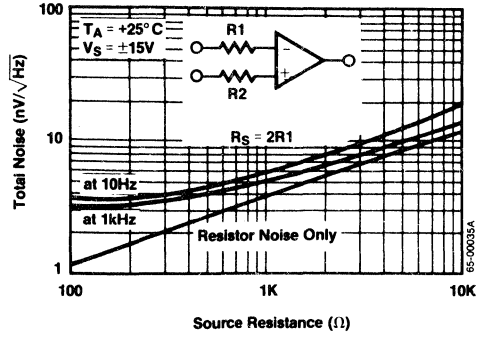


Figure 4. A Single Op Amp IC Difference Amplifier Using an OP-27. The Difference Amplifier is Connected for a Gain of 1000.



Voltage noise vs. source resistance for the difference amplifier. Noise performance shown is for $V_S = \pm 15V$, $T_A = +25°C$, and $R_S = R1 + R2$.

Figure 5. Total Noise vs. Source Resistance

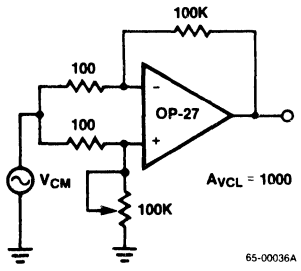


Figure 6. Common Mode Rejection Ratio Test Circuit

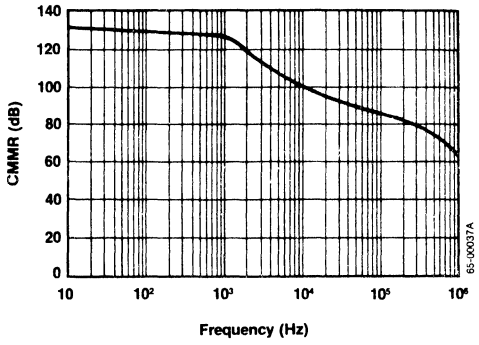
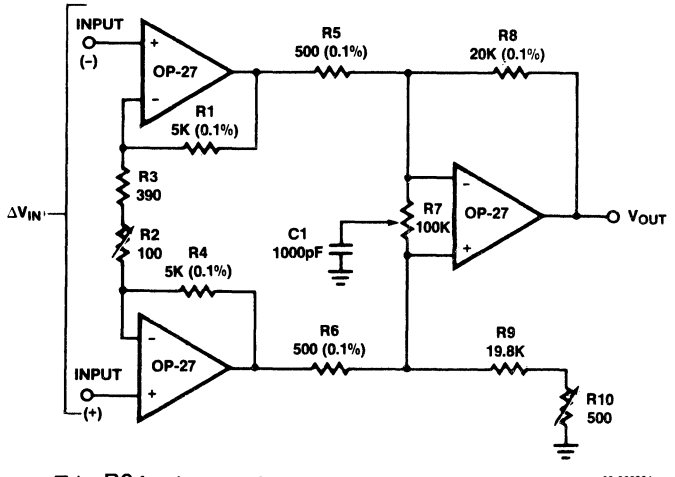


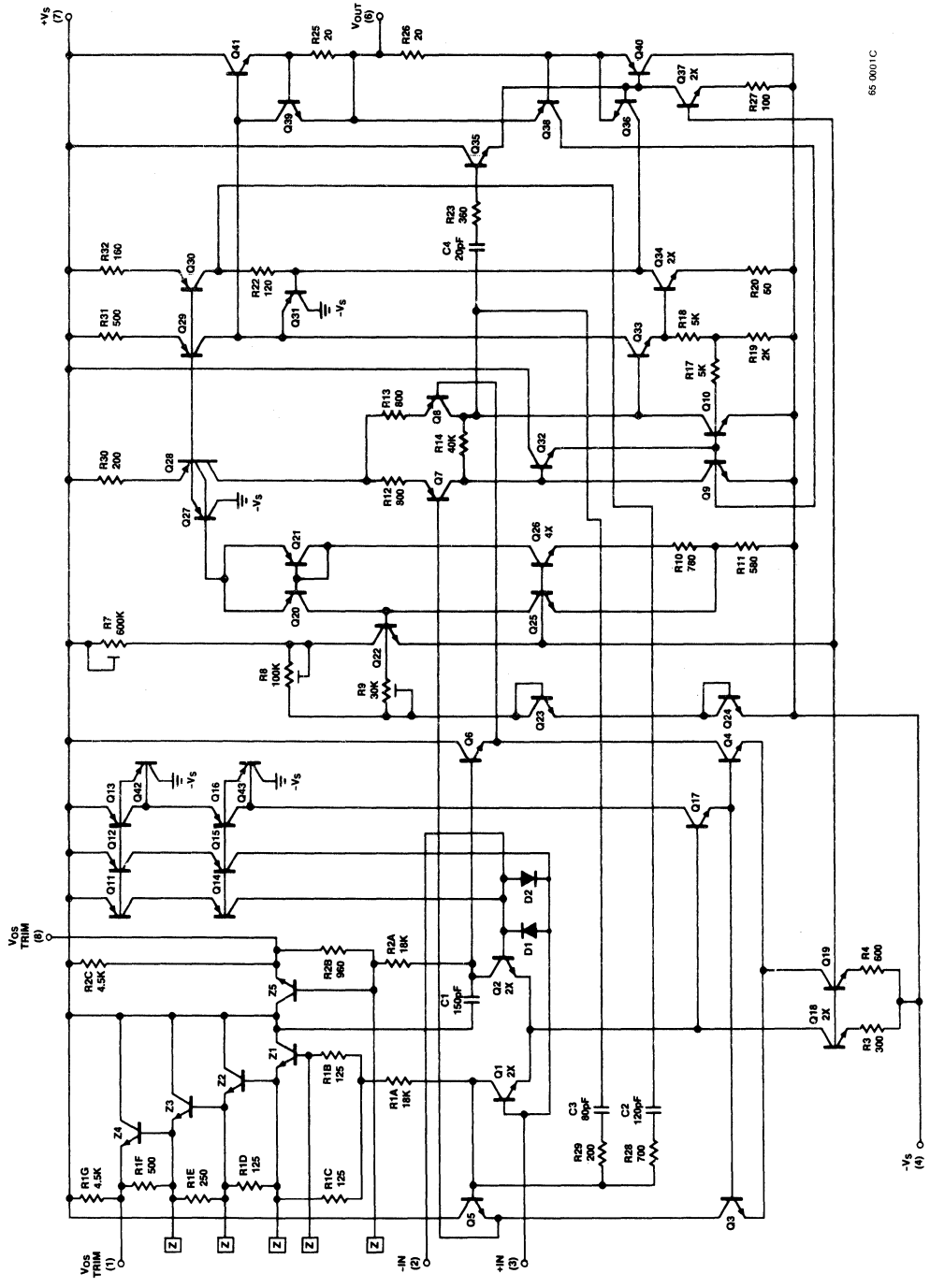
Figure 7. Common Mode Rejection Ratio vs. Frequency for the Circuit of Figure 4



Trim R2 for A_{VCL} = 1000
Trim R10 for DC CMRR
Trim R7 for Minimum V_{OUT} at V_{CM} = $20V_{p-p}$ 10kHz

Figure 8. Three Op Amp IC Instrumentation Amplifier

Schematic Diagram



OP-37 Low Noise Operational Amplifier

Features

- Very low noise
  Spectral noise density — 3.0 nV/$\sqrt{Hz}$
  1/f noise corner frequency — 2.7 Hz
- Very low V_{os} drift
  0.2 μV/Month
  0.2 μV/°C
- High gain — 1.8 Million
- High output drive capability —±12V into 600Ω load
- High slew rate —17 V/μS
- High gain bandwidth product — 63 MHz
- Good common mode rejection ratio — 126 dB
- Low input offset voltage — 10 μV
- Minimum low frequency noise — 0.08 μV_{p-p} (0.1 Hz to 10 Hz)
- Low input bias and offset currents — 10 nA
- Compensated for ac stability with $A_{VCL} \geq 5$

Description

The OP-37 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents.. The OP-37 is a decompensated version of the OP-27 and is ac stable in gain configurations equal to five and higher.

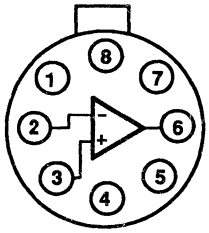
Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 25 μV. Input bias current cancellation techniques are used to obtain 10 nA input bias currents.

The OP-37 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120 dB. Input offset voltage can be externally trimmed without affecting input offset voltatge drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The OP-37 is available in LCC, SO-8 (small-outline), TO-99 can, plastic mini-DIP and ceramic mini-DIP packages, and can be ordered with Mil-Std-883 Level B processing.

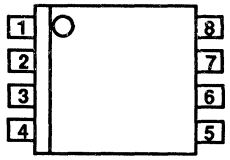
Connection Information

8-Lead TO-99 Metal Can
(Top View)



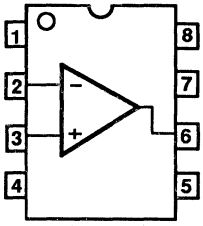
65-03205A

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

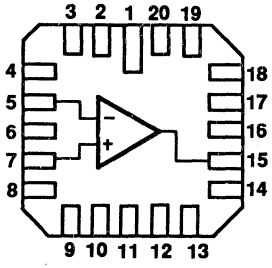
8-Lead Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{os} Trim
2	-Input
3	+Input
4	$-V_s$
5	NC
6	Output
7	$+V_s$
8	V_{os} Trim

20-Pad LCC
(Top View)



65-02657A

Pin	Function
2	V_{os} Trim
5	-Input
7	+Input
10	$-V_s$
15	Output
17	$+V_s$
20	V_{os} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
OP-37EN	N	0°C to +70°C
OP-37FN	N	0°C to +70°C
OP-37GN	N	0°C to +70°C
OP-37EM	M	0°C to +70°C
OP-37FM	M	0°C to +70°C
OP-37GM	M	0°C to +70°C
OP-37ED	D	-25°C to +85°C
OP-37FD	D	-25°C to +85°C
OP-37GD	D	-25°C to +85°C
OP-37ET	T	-25°C to +85°C
OP-37FT	T	-25°C to +85°C
OP-37GT	T	-25°C to +85°C
OP-37AD	D	-55°C to +125°C
OP-37AD/883B	D	-55°C to +125°C
OP-37BD	D	-55°C to +125°C
OP-37BD/883B	D	-55°C to +125°C
OP-37CD	D	-55°C to +125°C
OP-37CD/883B	D	-55°C to +125°C
OP-37AT	T	-55°C to +125°C
OP-37AT/883B	T	-55°C to +125°C
OP-37BT	T	-55°C to +125°C
OP-37BT/883B	T	-55°C to +125°C
OP-37CT	T	-55°C to +125°C
OP-37CT/883B	T	-55°C to +125°C
OP-37AL/883B	L	-55°C to +125°C
OP-37BL/883B	L	-55°C to +125°C

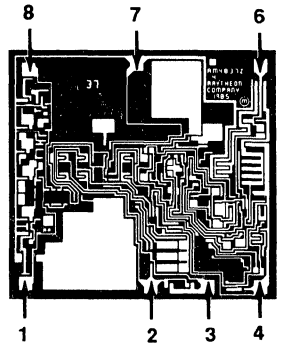
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation** ..... 658 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP-37A/B/C ..... -55°C to +125°C
OP-37E/F/G (Hermetic) ..... -25°C to +85°C
OP-37E/F/G (Plastic) ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8, 10 sec) ..... +260°C
(DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



Die Size: 75 x 80 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Small Outline	8-Lead Ceramic DIP	TO-99 8-Lead Metal Can	20-Pad LCC	8-Lead Plastic DIP
Max. Junction Temp.	125°C	175°C	175°C	175°C	125°C
Max. P_D T_A <50°C	300 mW	833 mW	658 mW	925 mW	468 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W	37°C/W	—
Therm. Res. θ_{JA}	240°C/W	150°C/W	190°C/W	105°C/W	160°C/W
For T_A >50°C Derate at	4.17 mW/°C	8.33 mW/°C	5.26 mW/°C	7.0 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-37A/E			OP-37B/F			OP-37C/G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			10	25		20	60		30	100	µV
Long Term Input Offset Voltage Stability[1,2]			0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current			7.0	35		9.0	50		12	75	nA
Input Bias Current			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.08	0.18		0.08	0.18		0.09	0.25	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		3.5	5.5		3.5	5.5		3.8	8.0	$\frac{nV}{\sqrt{Hz}}$
	F_O = 30 Hz		3.1	4.5		3.1	4.5		3.3	5.6	
	F_O = 1000 Hz		3.0	3.8		3.0	3.8		3.2	4.5	
Input Noise Current Density[2]	F_O = 10 Hz		1.7	4.0		1.7	4.0		1.7		$\frac{pA}{\sqrt{Hz}}$
	F_O = 30 Hz		1.0	2.3		1.0	2.3		1.0		
	F_O = 1000 Hz		0.4	0.6		0.4	0.6		0.4	0.6	
Input Resistance (Diff. Mode)[4]		1.5	6.0		1.2	5.0		0.8	4.0		MΩ
Input Resistance (Com. Mode)			3.0			2.5			2.0		GΩ
Input Voltage Range[3]		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	V_S ±4V to ±18V	100	120		100	120		94	118		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	1000	1800		1000	1800		700	1500		V/mV
	$R_L \geq 1$ kΩ, V_O = ±10V	800	1500		800	1500			1500		
	V_O = ±1V, V_S = ±4V[4]	250	700		250	700		200	500		
Output Voltage Swing	$R_L \geq 2$ kΩ	±12	±13.8		±12	±13.8		±11.5	±13.5		V
	$R_L \geq$600Ω	±11	±12		±11	±12		±11	±12		
Slew Rate[4]	$R_L \geq 2$ kΩ	11	17		11	17		11	17		V/µS
Gain Bandwidth Product[4]	F_O = 10 kHz	45	63		45	63		45	63		MHz
	F_O = 1 MHz		40			40			40		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		70			70			70		Ω
Power Consumption			90	140		90	140		100	170	mW
Offset Adjustment Range	R_p = 10 kΩ		±4.0			±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Supply refers to the average trend line of V_{os} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{os} during the first 30 operating days are typically 2.5 µV.
2. This parameter is tested on a sample basis only.
3. Caution: The Common Mode Input Range is a function of supply voltage. See Typical Performance Curves. Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed but not tested.
5. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-37A			OP-37B			OP-37C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	60		50	200		70	300	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			15	50		22	85		30	135	nA
Input Bias Current			±20	±60		±28	±95		±35	±150	nA
Input Voltage Range		±10.3	±11.5		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	V_S ±4.5V to ±18V	96	116		94	114		86	110		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V	600	1200		500	1000		300	800		V/mV
Output Voltage Swing	R_L ≥2 kΩ	±11.5	±13.5		±11	±13.2		±10.5	±13		V

Electrical Characteristics (V_S = ±15V, -25°C ≤ T_A ≤ +85°C for hermetic package types, 0°C ≤ T_A ≤ +70°C for plastic package types unless otherwise noted)

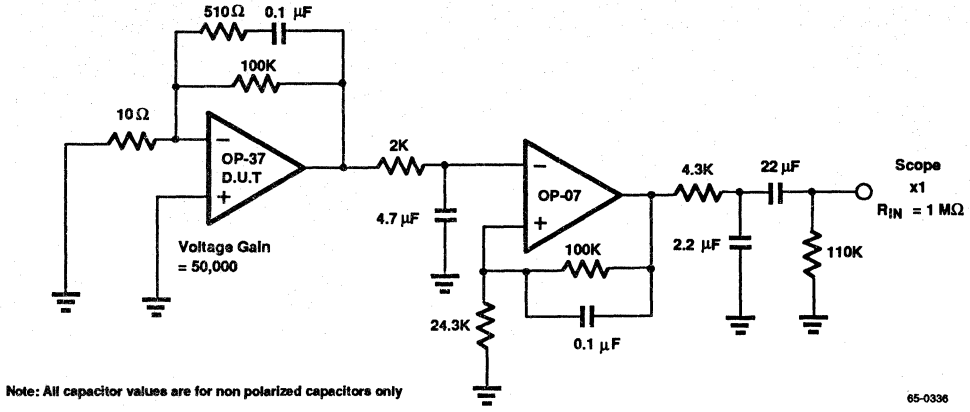
Parameters	Test Conditions	OP-37E			OP-37F			OP-37G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	50		40	140		55	220	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			10	50		14	85		20	135	nA
Input Bias Current			±14	±60		±18	±95		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		102	121		96	118		dB
Power Supply Rejection Ratio	V_S ±4.5V to ±18V	97	118		96	116		90	114		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	R_L ≥2 kΩ	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed unnulled or when nulled with R_P = 8.0 kΩ to 20 kΩ.

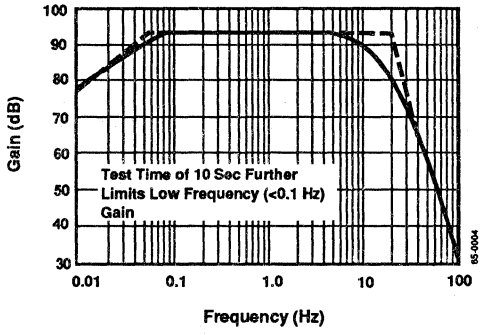
Typical Performance Characteristics

0.1 Hz to 10 Hz Noise Test Circuit

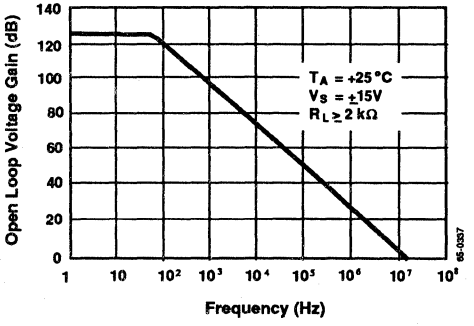


Note: All capacitor values are for non polarized capacitors only

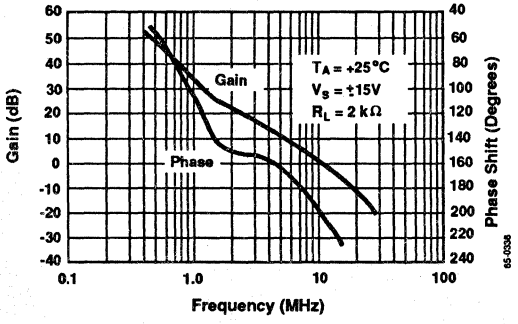
0.1 Hz to 10 Hz Peak-to-Peak Noise Tester Frequency Response



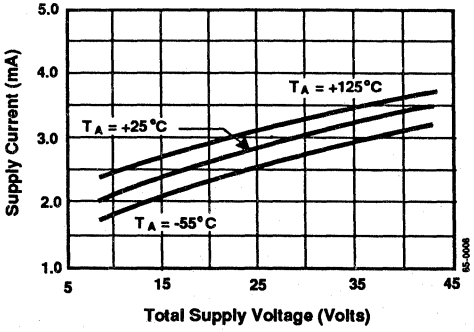
Open Loop Gain vs. Frequency



Gain, Phase Shift vs. Frequency

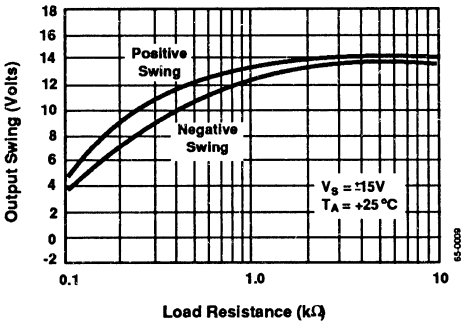


Supply Current vs. Supply Voltage

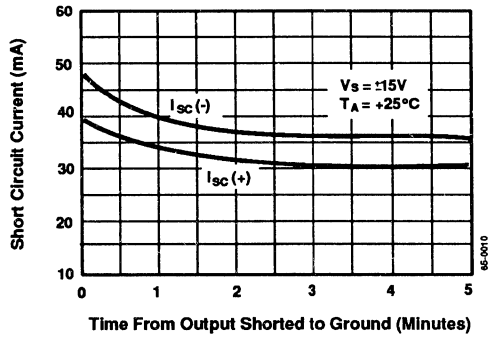


Typical Performance Characteristics (Continued)

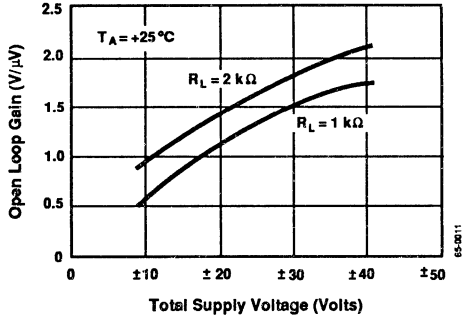
Maximum Output Swing vs. Resistive Load



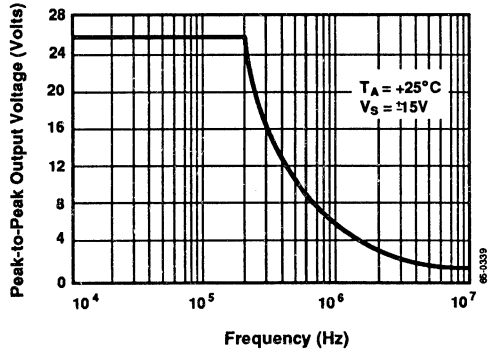
Short Circuit Current vs. Time



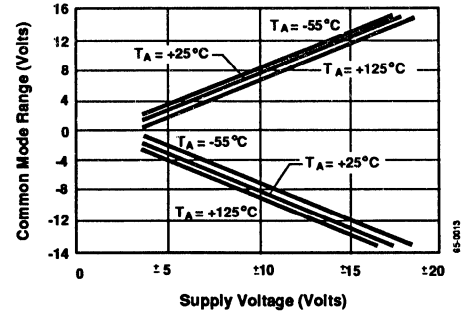
Open Loop Voltage Gain vs. Supply Voltage



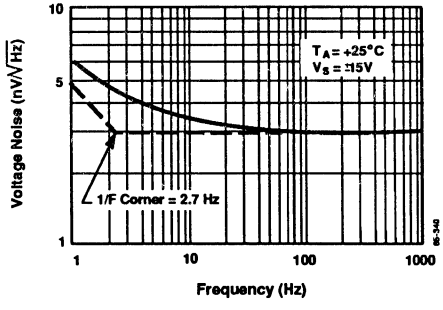
Maximum Undistorted Output vs. Frequency



Common Mode Input Range vs. Supply Voltage

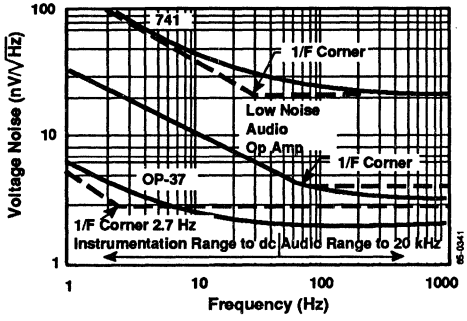


OP-37 Voltage Noise vs. Frequency

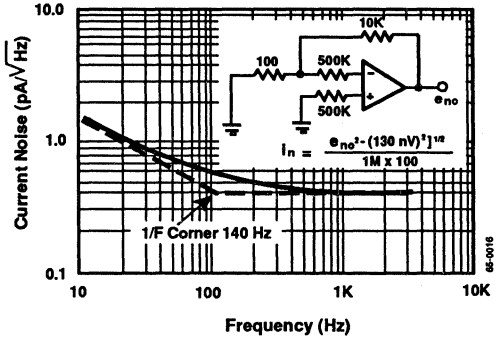


Typical Performance Characteristics (Continued)

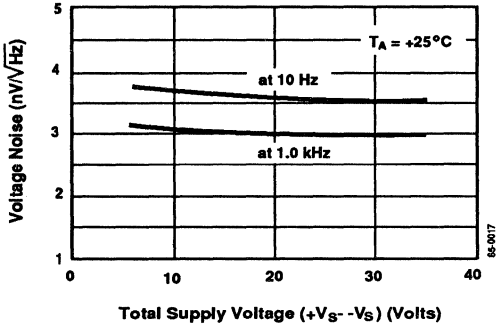
A Comparison of Op Amp Voltage Noise Spectrums



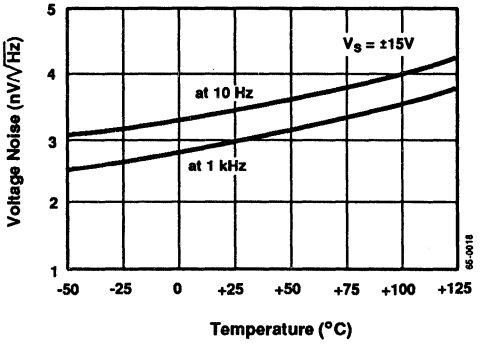
Current Noise vs. Frequency



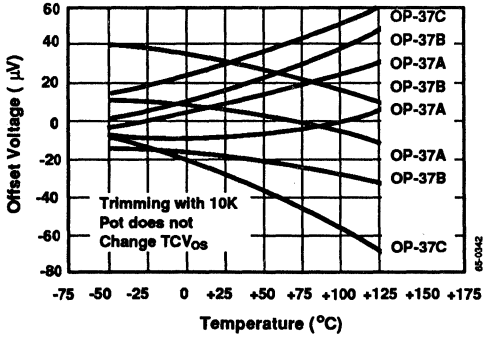
Voltage Noise vs. Supply Voltage



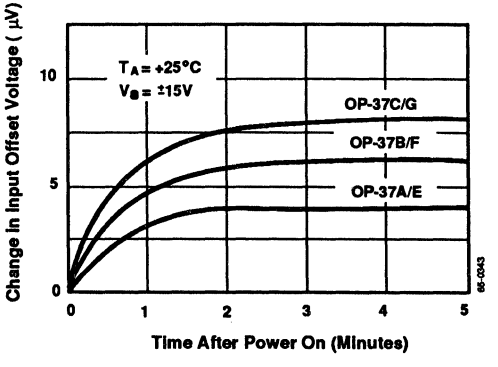
Voltage Noise vs. Temperature



Offset Voltage Drift of Representative Units

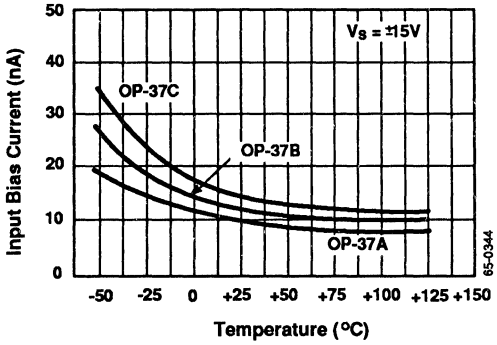


Warm-Up Drift

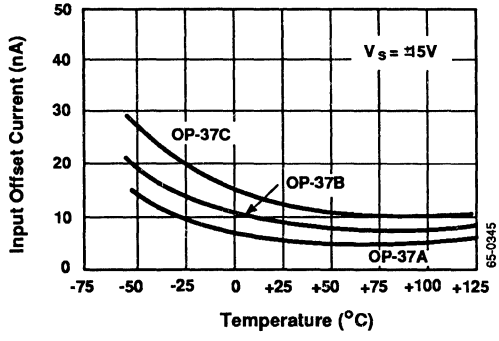


Typical Performance Characteristics (Continued)

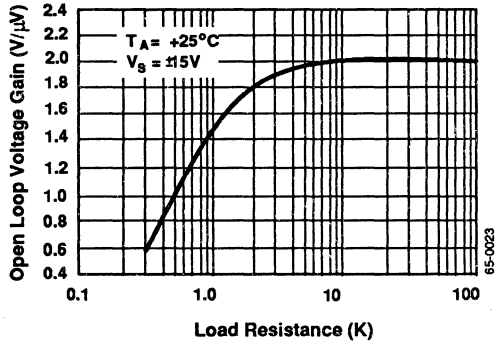
Input Bias Current vs. Temperature



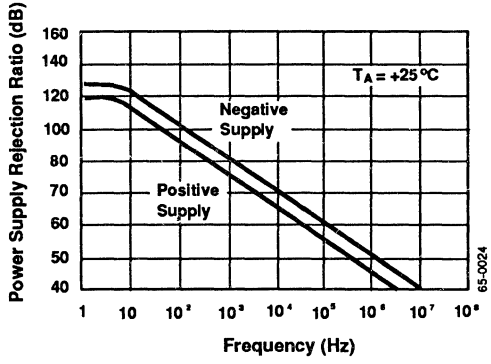
Input Offset Current vs. Temperature



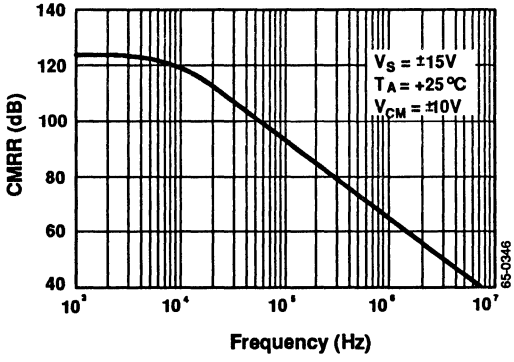
Open Loop Voltage Gain vs. Load Resistance



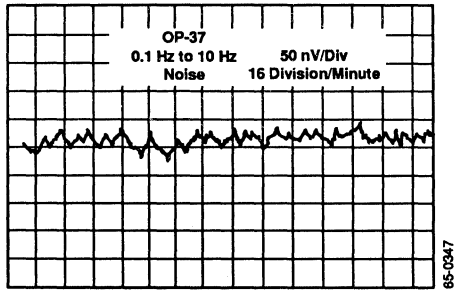
PSRR vs. Frequency



CMRR vs. Frequency

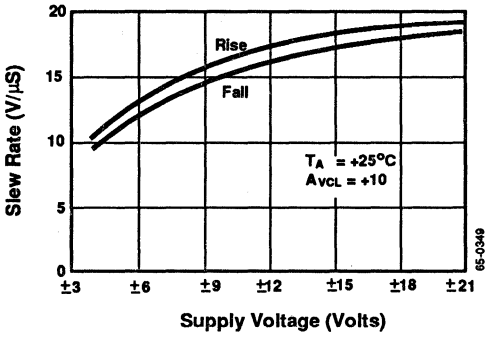


OP-37 0.1 Hz to 10 Hz Peak-to-Peak Noise Vertical Scale 50 nV/Division Recorder Speed 8 Divisions/Minute

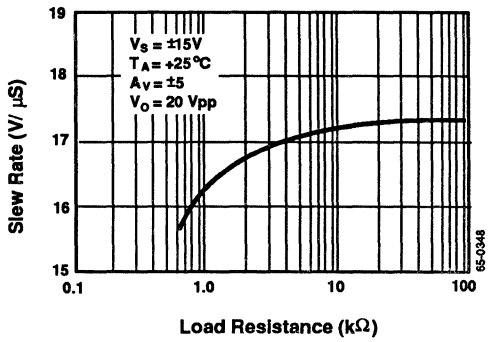


Typical Performance Characteristics (Continued)

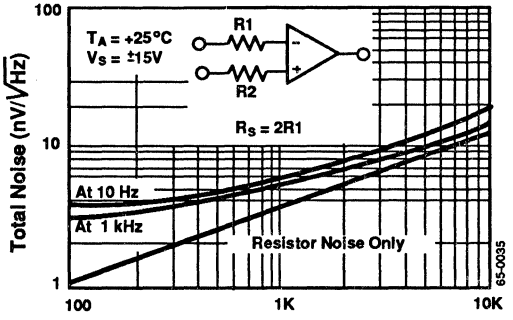
Slew Rate vs. Supply Voltage



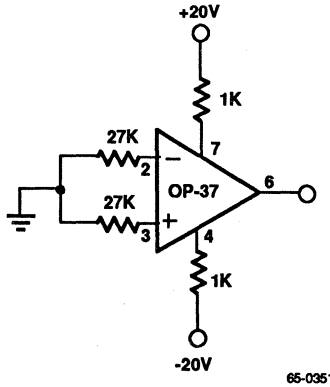
Slew Rate vs. Load



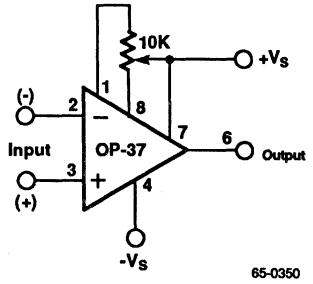
Total Noise vs. Source Resistance



Burn-In Circuit



Offset Nulling Circuit



Typical Applications

Low Impedance Microphone Preamp (Figure 1)

In this preamp the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-37 for best noise performance. The optimum source impedance can be calculated as the ratio of en/in which for the OP-37 is approximately 7000Ω. Fortunately the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value. The source impedance at the output of this transformer of 15 kΩ still provides near optimum noise performance. (A high quality audio transformer with a step-up ratio of 6.7 to one is not available.) C1 rolls off the high frequency response at 90 kHz giving a noise power bandwidth of 140 kHz.

Instrumentation

The OP-37 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-37 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that it is dominated almost entirely by the resistor Johnson noise.

The three op amp instrumentation amplifier of Figure 4 avoids the low in put impedance characteristics of difference amplifiers at the expense of two more operational amplifiers and a slight degradation in noise performance. The noise increases because two amplifiers are contributing to the input voltage spectral noise instead of one. Thus, the noise contribution, exclusive of resistor Johnson noise, increases by slightly more than the $\sqrt{2}$. The spectral noise voltage increases from approximately 3 nV/$\sqrt{Hz}$ to approximately 4.9 nV/$\sqrt{Hz}$, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 40 for an overall gain of 1000. R7 is trimmed to optimize the common mode rejection ratio (CMRR) with frequency . With balanced source resistors a CMRR of 100 dB is achieved. With a 1 kΩ source impedance imbalance CMRR is degraded to 80 dB at 5 kHz due to the finite (3 GΩ) input impedance.

DAC Current to Voltage Converter

Many high speed voltage output D/A conversion applications require a high speed op amp to convert a standard current output DAC (such as a DAC-08 or DAC-10) to voltage output. The OP-37 is ideal for this because it has the speed and settling time for fast data conversion, but still has excellent dc specifications to ensure high accuracy .

The 360Ω resistor is required to increase the effective gain of the OP-37 to meet the minimum gain requirement for stability. The high speed of the OP-37 allows a conversion time of 1 μS to 1/2 LSB in this circuit. In addition, the low V_{OS} and V_{OS} drift of the OP-37 complements the high accuracy of the DAC-10, and the high output drive capability allows connection to demanding loads.

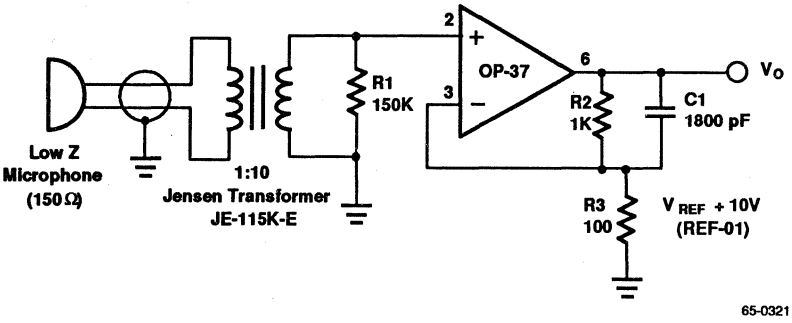


Figure 1. Low Impedance Microphone Preamplifier

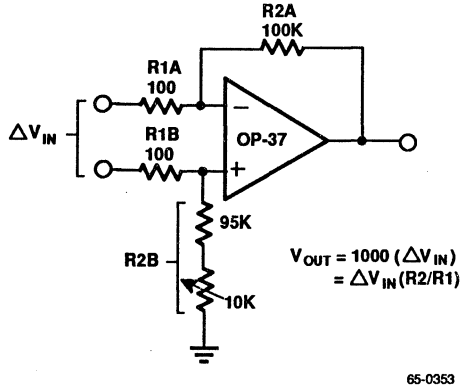


Figure 2. A Single Op Amp IC Difference Amplifier Using an OP-37. The Difference Amplifier is Connected for a Gain of 1000.

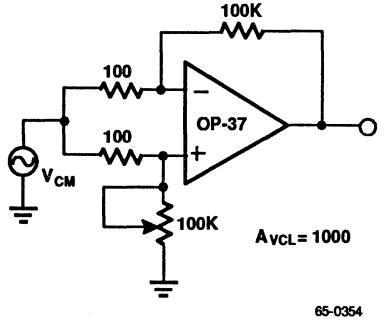


Figure 3. Common Mode Rejection Ratio Test Circuit

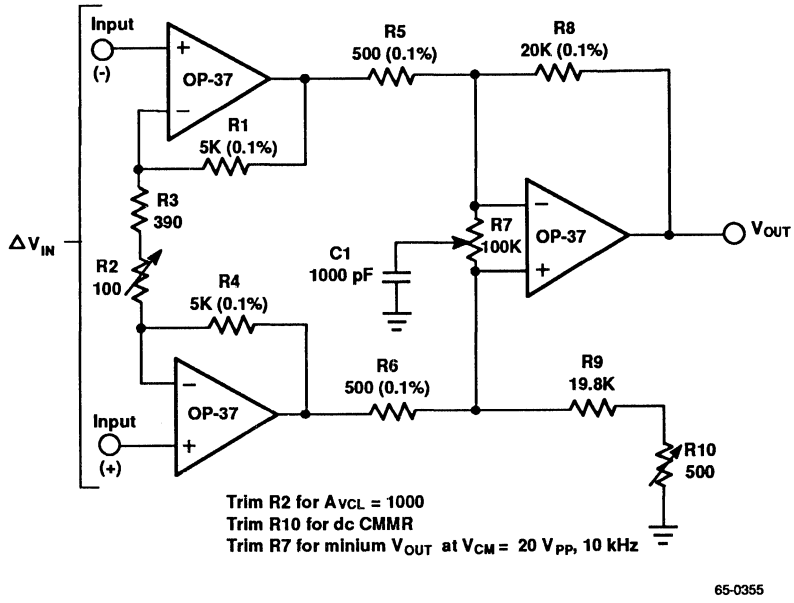


Figure 4. Three Op Amp IC Instrumentation Amplifier

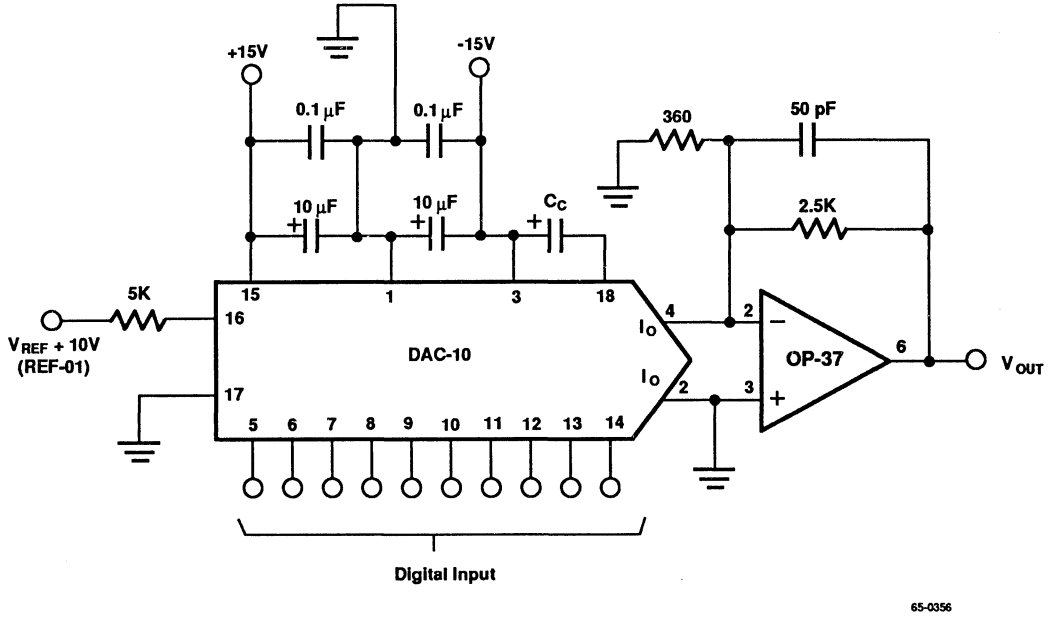
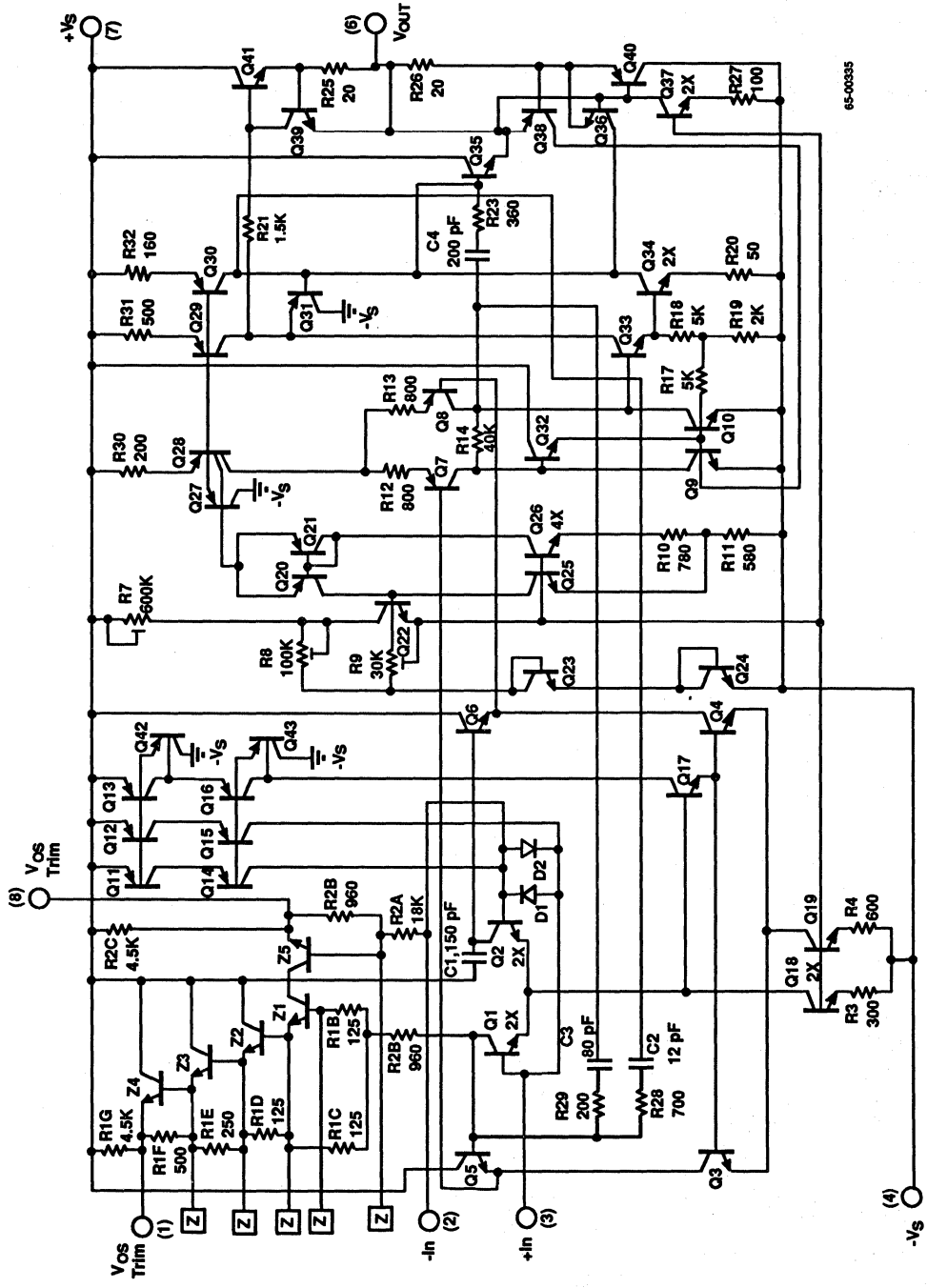


Figure 5. D/A Converter Application

Schematic Diagram



OP-47 Low Noise, High Slew Rate Operational Amplifier

Features

- Very low noise
  - Spectral noise density – 3.0 nV/$\sqrt{Hz}$
  - 1/f noise corner frequency – 2.7 Hz
- Very low V_{os} drift
  - 0.2 μV/Month
  - 0.2 μV/°C
- High gain – 1.8 million
- High output drive capability – ±12V into 600Ω load
- High slew rate – 50 V/μS
- High gain bandwidth product – 63 MHz
- Good common mode rejection ratio –126 dB
- Low input offset voltage – 10 μV
- Minimum low frequency noise –.08 μVp-p (0.1 Hz to 10 Hz)
- Low input bias and offset currents –10 nA
- Compensated for ac stability with AVCL ≥400

Description

The OP-47 is designed for instrumentation grade signal conditioning where low noise (both spectral density and burst), wide bandwidth, and high slew rate are required along with low input offset voltage, low input offset temperature coefficient, and low input bias currents. The OP-47 is a decompensated version of the OP-27 and is ac stable in closed-loop gain configurations greater than or equal to 400.

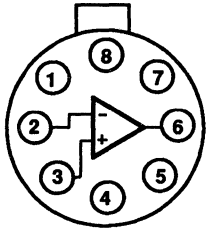
Digital nulling techniques performed at wafer sort make it feasible to guarantee temperature stable input offset voltages as low as 25 μV. Input bias current cancellation techniques are used to obtain 10 nA input bias currents.

The OP-47 design uniquely addresses the needs of the instrumentation designer. Power supply rejection and common mode rejection are both in excess of 120 dB. Input offset voltage can be externally trimmed without affecting input offset voltage drift with temperature or time. The drift performance is, in fact, so good that the system designer must be cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals are enough to degrade its performance. For this reason it is also important to keep both input terminals at the same relative temperature.

The OP-47 is available in LCC, SO-8 (small-outline), TO-99 can, plastic mini-DIP and ceramic mini-DIP packages, and can be ordered with Mil-Std-883 Level B processing.

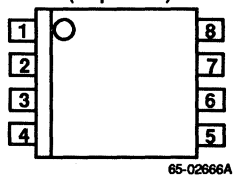
Connection Information

8-Lead TO-99 Metal Can
(Top View)



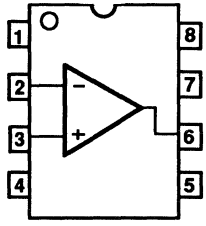
65-03205A

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

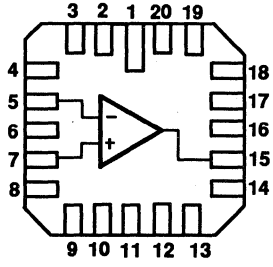
8-Lead Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

20-Pad LCC
(Top View)



65-02657A

Pin	Function
2	V_{OS} Trim
5	-Input
7	+Input
10	$-V_S$
15	Output
17	$+V_S$
20	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
OP-47EN	N	0°C to +70°C
OP-47FN	N	0°C to +70°C
OP-47GN	N	0°C to +70°C
OP-47EM	M	0°C to +70°C
OP-47FM	M	0°C to +70°C
OP-47GM	M	0°C to +70°C
OP-47ED	D	-25°C to +85°C
OP-47FD	D	-25°C to +85°C
OP-47GD	D	-25°C to +85°C
OP-47ET	T	-25°C to +85°C
OP-47FT	T	-25°C to +85°C
OP-47GT	T	-25°C to +85°C
OP-47AD	D	-55°C to +125°C
OP-47AD/883B	D	-55°C to +125°C
OP-47BD	D	-55°C to +125°C
OP-47BD/883B	D	-55°C to +125°C
OP-47CD	D	-55°C to +125°C
OP-47CD/883B	D	-55°C to +125°C
OP-47AT	T	-55°C to +125°C
OP-47AT/883B	T	-55°C to +125°C
OP-47BT	T	-55°C to +125°C
OP-47BT/883B	T	-55°C to +125°C
OP-47CT	T	-55°C to +125°C
OP-47CT/883B	T	-55°C to +125°C
OP-47AL/883B	L	-55°C to +125°C
OP-47BL/883B	L	-55°C to +125°C

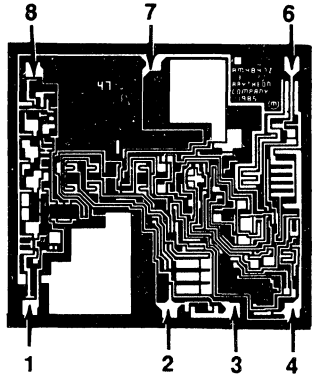
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 0.7V
Internal Power Dissipation** ..... 658 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
  Range ..... -65°C to +150°C
Operating Temperature Range
  OP-47A/B/C ..... -55°C to +125°C
  OP-47E/F/G (Hermetic) ..... -25°C to +85°C
  OP-47E/F/G (Plastic) ..... 0°C to +70°C
Lead Soldering Temperature
  (SO-8, 10 sec) ..... +260°C
  (DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



Die Size: 75 x 80 mils
Min Pad Dimensions: 4 x 4 mils
65-01681A

Thermal Characteristics

	8-Lead Small Outline	8-Lead Ceramic DIP	TO-99 8-Lead Metal Can	20-Pad LCC	8-Lead Plastic DIP
Max. Junction Temp.	125°C	175°C	175°C	175°C	125°C
Max. P_D T_A <50°C	300 mW	833 mW	658 mW	925 mW	468 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W	37°C/W	—
Therm. Res. θ_{JA}	240°C/W	150°C/W	190°C/W	105°C/W	160°C/W
For T_A >50°C Derate at	4.17 mW/°C	8.33 mW/°C	5.26 mW/°C	7.0 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-47A/E			OP-47B/F			OP-47C/G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[5]			10	25		20	60		30	100	µV
Long Term Input Offset Voltage Stability[1,4]			0.2	1.0		0.3	1.5		0.4	2.0	µV/Mo
Input Offset Current			7.0	35		9.0	50		12	75	nA
Input Bias Current			±10	±40		±12	±55		±15	±80	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.08	0.18		0.08	0.18		0.09	0.25	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		3.5	5.5		3.5	5.5		3.8	8.0	$\frac{nV}{\sqrt{Hz}}$
	F_O = 30 Hz		3.1	4.5		3.1	4.5		3.3	5.6	
	F_O = 1000 Hz		3.0	3.8		3.0	3.8		3.2	4.5	
Input Noise Current Density[2]	F_O = 10 Hz		1.7	4.0		1.7	4.0		1.7		$\frac{pA}{\sqrt{Hz}}$
	F_O = 30 Hz		1.0	2.3		1.0	2.3		1.0		
	F_O = 1000 Hz		0.4	0.6		0.4	0.6		0.4	0.6	
Input Resistance (Diff. Mode)[4]		1.5	6.0		1.2	5.0		0.8	4.0		MΩ
Input Resistance (Com. Mode)			3.0			2.5			2.0		GΩ
Input Voltage Range[3]		±11	±12.3		±11	±12.3		±11	±12.3		V
Common Mode Rejection Ratio	V_{CM} = ±11V	114	126		106	123		100	120		dB
Power Supply Rejection Ratio	V_S ±4V to ±18V	100	120		100	120		94	118		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V	1000	1800		1000	1800		700	1500		V/mV
	R_L ≥ 1 kΩ, V_O = ±10V	800	1500		800	1500			1500		
	V_O = ±1V, V_S = ±4V[4]	250	700		250	700		200	500		
Output Voltage Swing	R_L ≥ 2 kΩ	±12	±13.8		±12	±13.8		±11.5	±13.5		V
	R_L ≥600Ω	±11	±12		±11	±12		±11	±12		
Slew Rate[4]	R_L ≥ 2 kΩ	35	50		35	50		35	50		V/µS
Gain Bandwidth Product[4]	F_O = 10 kHz F_O = 1 MHz	45	70 45		45	70 45		45	70 45		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		70			70			70		Ω
Power Consumption			90	140		90	140		100	170	mW
Offset Adjustment Range	R_P = 10 kΩ		±4.0			±4.0			±4.0		mV

Notes:
1. Long Term Input Offset Voltage Supply refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. This parameter is tested on a sample basis only.
3. Caution: The Common Mode Input Range is a function of supply voltage. See Typical Performance Curves. Also, the input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
4. Parameter is guaranteed but not tested.
5. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	OP-47A			OP-47B			OP-47C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	60		50	200		70	300	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			15	50		22	85		30	135	nA
Input Bias Current			±20	±60		±28	±95		±35	±150	nA
Input Voltage Range		±10.3	±11.5		±10.3	±11.5		±10.2	±11.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	108	122		100	119		94	116		dB
Power Supply Rejection Ratio	V_S ±4.5V to ±18V	96	116		94	114		86	110		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V	600	1200		500	1000		300	800		V/mV
Output Voltage Swing	R_L ≥2 kΩ	±11.5	±13.5		±11	±13.2		±10.5	±13		V

Electrical Characteristics (V_S = ±15V, -25°C ≤T_A ≤ +85°C for hermetic package types, 0°C ≤ T_A ≤ +70°C for plastic package types unless otherwise noted)

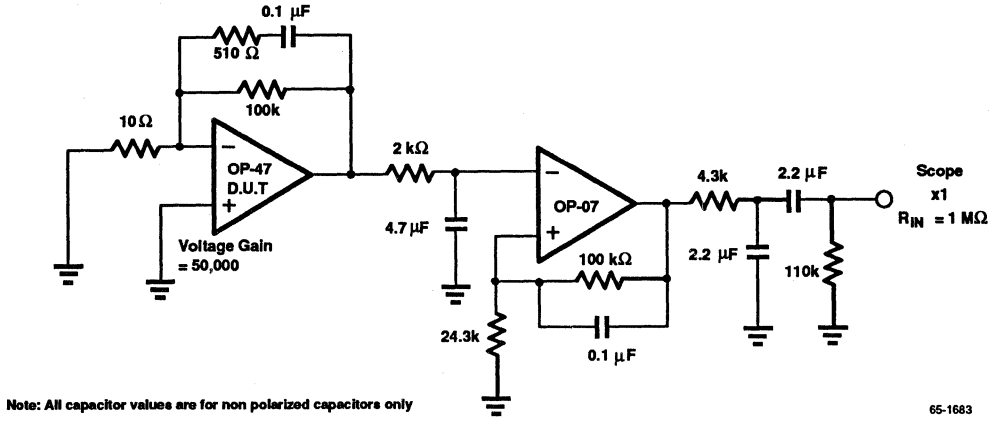
Parameters	Test Conditions	OP-47E			OP-47F			OP-47G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	50		40	140		55	220	µV
Average Input Offset Voltage Drift[2]			0.2	0.6		0.3	1.3		0.4	1.8	µV/°C
Input Offset Current			10	50		14	85		20	135	nA
Input Bias Current			±14	±60		±18	±95		±25	±150	nA
Input Voltage Range		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
Common Mode Rejection Ratio	V_{CM} = ±10V	110	124		102	121		96	118		dB
Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	97	118		96	116		90	114		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V	750	1500		700	1300		450	1000		V/mV
Output Voltage Swing	R_L ≥2 kΩ	±11.7	±13.6		±11.4	±13.5		±11	±13.3		V

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. $T_C V_{OS}$ performance is guaranteed unnulled or when nulled with R_P = 8.0 kΩ to 20 kΩ.

Typical Performance Characteristics

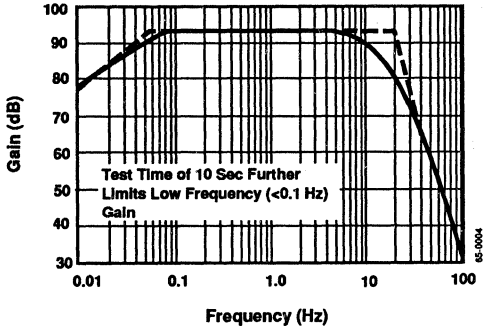
0.1 Hz to 10 Hz Noise Test Circuit



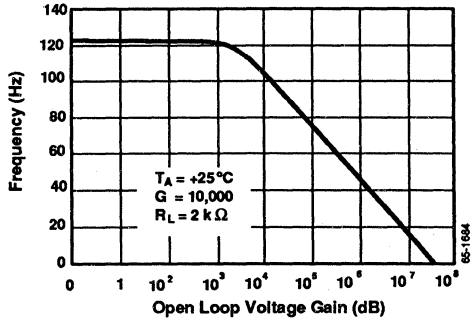
Note: All capacitor values are for non polarized capacitors only

65-1683

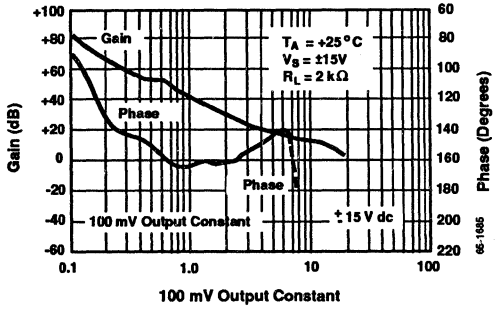
0.1 Hz to 10 Hz Peak-to-Peak Noise Tester Frequency Response



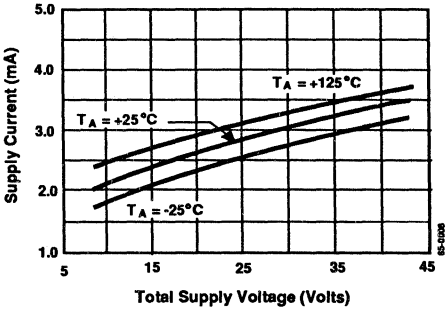
Open Loop Gain vs. Frequency



Gain and Phase Shift vs. Frequency

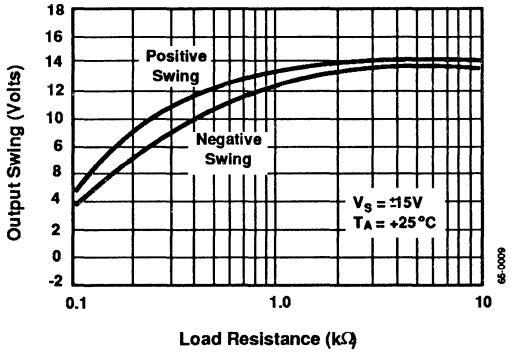


Supply Current vs. Supply Voltage

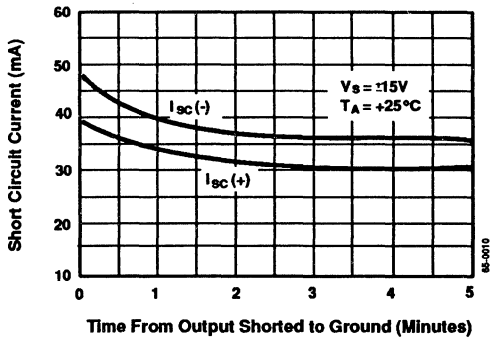


Typical Performance Characteristics (Continued)

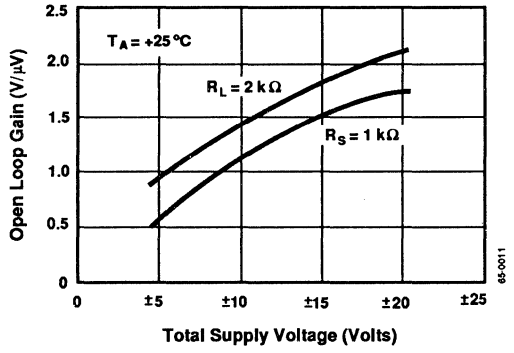
Maximum Output Swing vs. Resistive Load



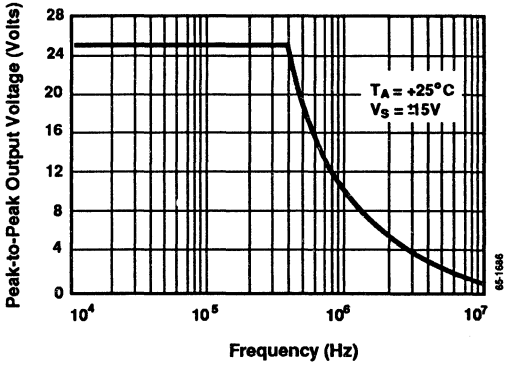
Short Circuit Current vs. Time



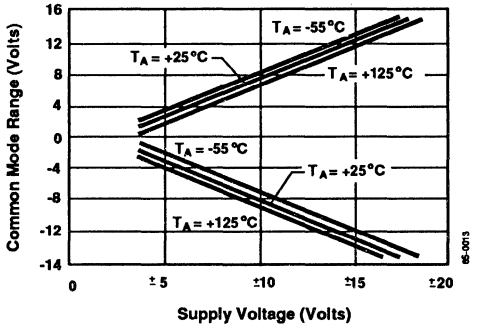
Open Loop Voltage Gain vs. Supply Voltage



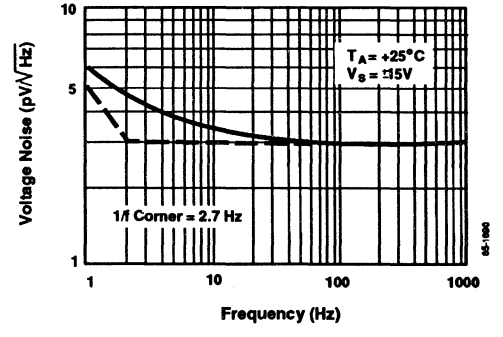
Maximum Undistorted Output vs. Frequency



Common Mode Input Range vs. Supply Voltage

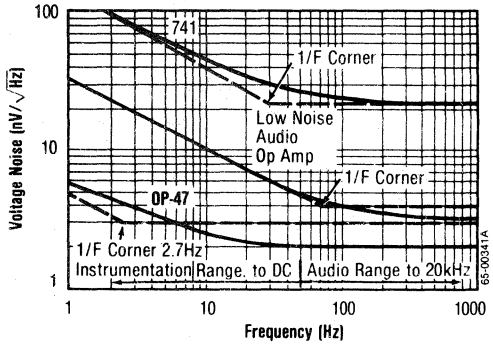


OP-47 Voltage Noise vs. Frequency

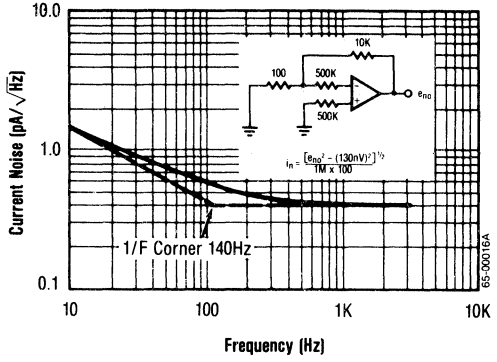


Typical Performance Characteristics (Continued)

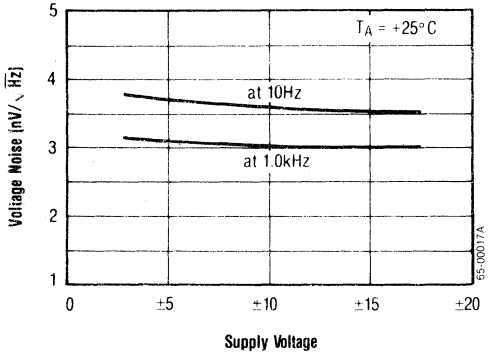
A Comparison of Op Amp Voltage Noise Spectrums



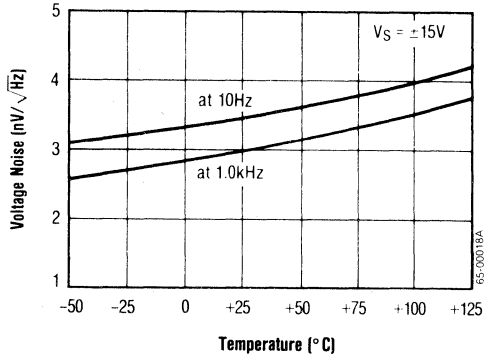
Current Noise vs. Frequency



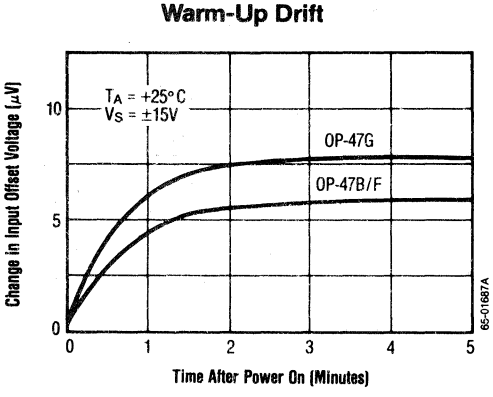
Voltage Noise vs. Supply Voltage



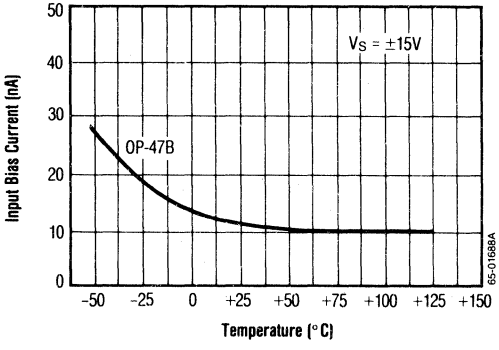
Voltage Noise vs. Temperature



Warm-Up Drift

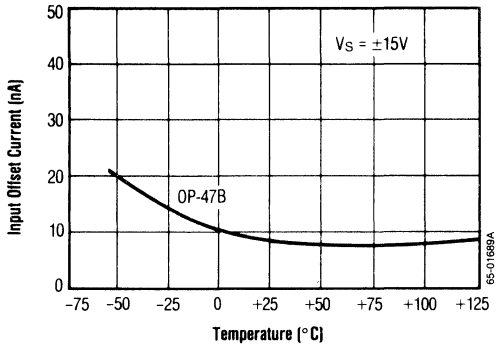


Input Bias Current vs. Temperature

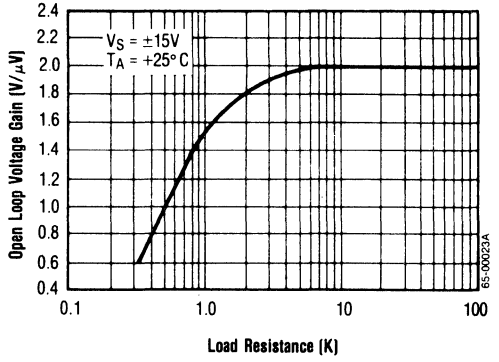


Typical Performance Characteristics (Continued)

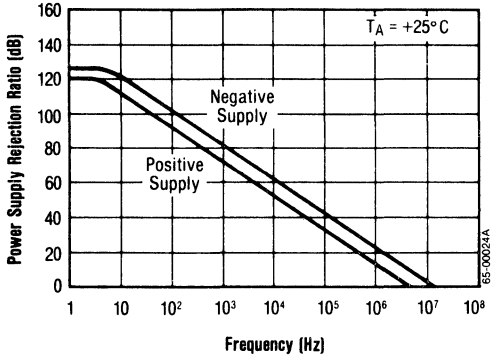
Input Offset Current vs. Temperature



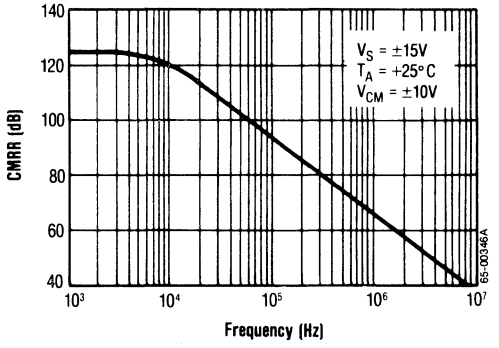
Open Loop Voltage Gain vs. Load Resistance



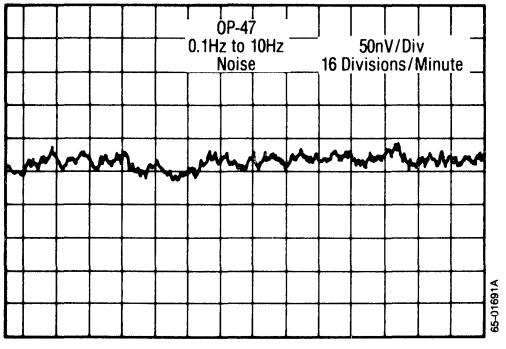
PSRR vs. Frequency



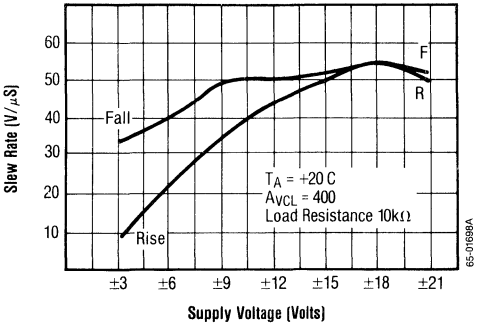
CMRR vs. Frequency



OP-47 0.1Hz to 10Hz Peak-to-Peak Noise Vertical Scale 50nV/Division Recorder Speed 8 Divisions/Min

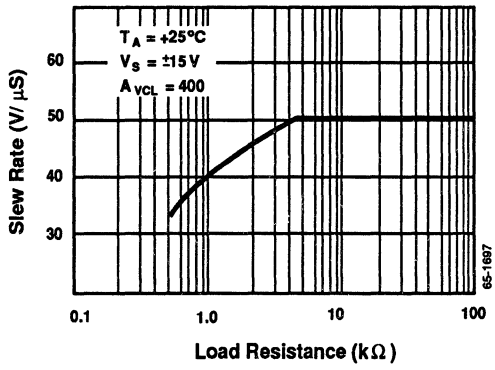


Supply Voltage vs. Slew Rate

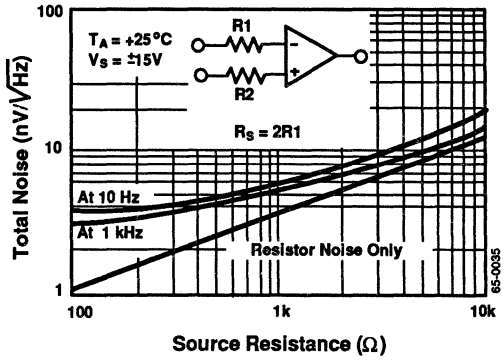


Typical Performance Characteristics (Continued)

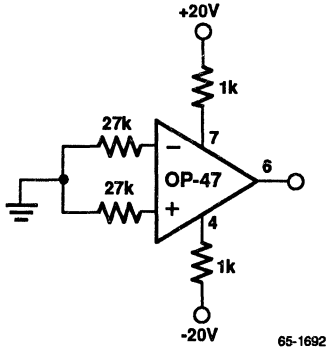
Load Resistance vs. Slew Rate



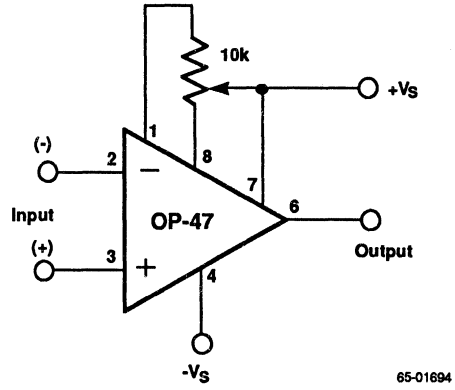
Total Noise vs. Source Resistance



Burn-In Circuit



Offset Nulling Circuit



Typical Applications

Low Impedance Microphone Preamp (Figure 1)

In this preamp the transformer converts the low microphone impedance up to a value that is close to the optimum source impedance required by the OP-47 for best noise performance. The optimum source impedance can be calculated as the ratio of e_n/i_n which for the OP-47 is approximately 7000Ω. Fortunately the noise performance does not degrade appreciably until the source impedance is four or five times this optimum value.The source impedance at the output of this transformer, of 15 kΩ, still provides near optimum noise performance. (A high quality audio transformer with a step-up ratio of 6.7 to one is not available.) . C1 rolls off the high frequency response at 90 kHz giving a noise power bandwidth of 140 kHz.

Instrumentation

The OP-47 is particularly adaptable to instrumentation applications. When wired into a single op amp difference amplifier configuration, the OP-47 exhibits outstanding common mode rejection ratio. The spot voltage noise is so low that it is dominated almost entirely by the resistor Johnson noise.

The three op amp instrumentation amplifier of Figure 2. avoids the low input impedance characteristics of difference amplifiers .The noise increases because two amplifiers are contributing to the input voltage spectral noise. The noise contribution, exclusive of resistor Johnson noise, increases by slightly more than the $\sqrt{2}$. The spectral noise voltage increases from approximately 3 nV/$\sqrt{Hz}$ to approximately 4.9 nV/$\sqrt{Hz}$, with the third amplifier contributing about 10% of the noise. The gain of the input amplifier is set at 25 and the second stage at 400 for an overall gain of 1000. R7 is trimmed to optimize the common mode rejection ratio (CMRR) with frequency. With balanced source resistors a CMRR of 100 dB is achieved. With a 1 kΩ source impedance imbalance CMRR is degraded to 80 dB at 5 kHz due to the finite (3 GΩ) input impedance.

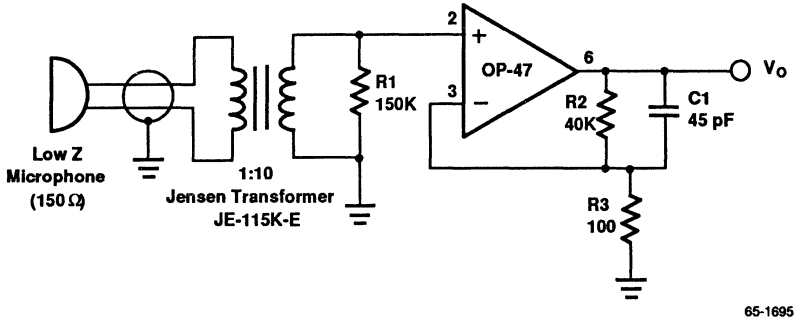


Figure 1. Low Impedance Microphone Preamplifier

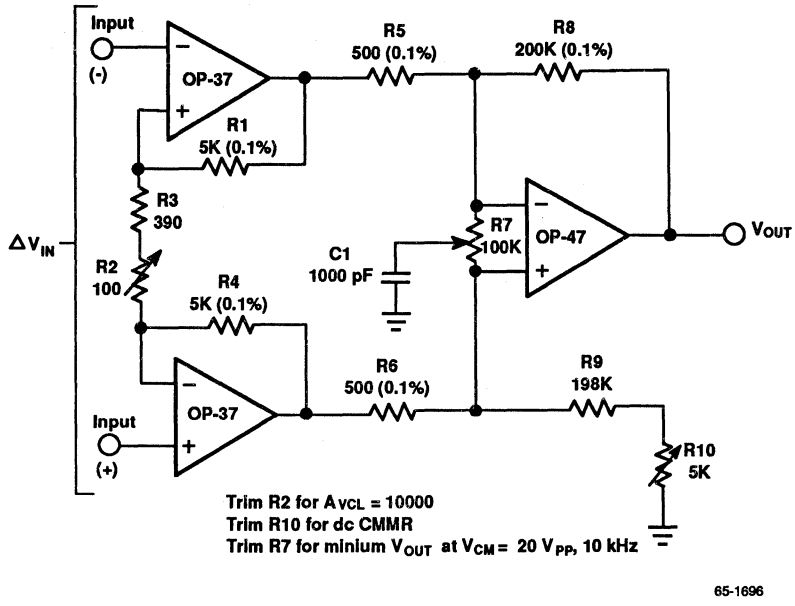
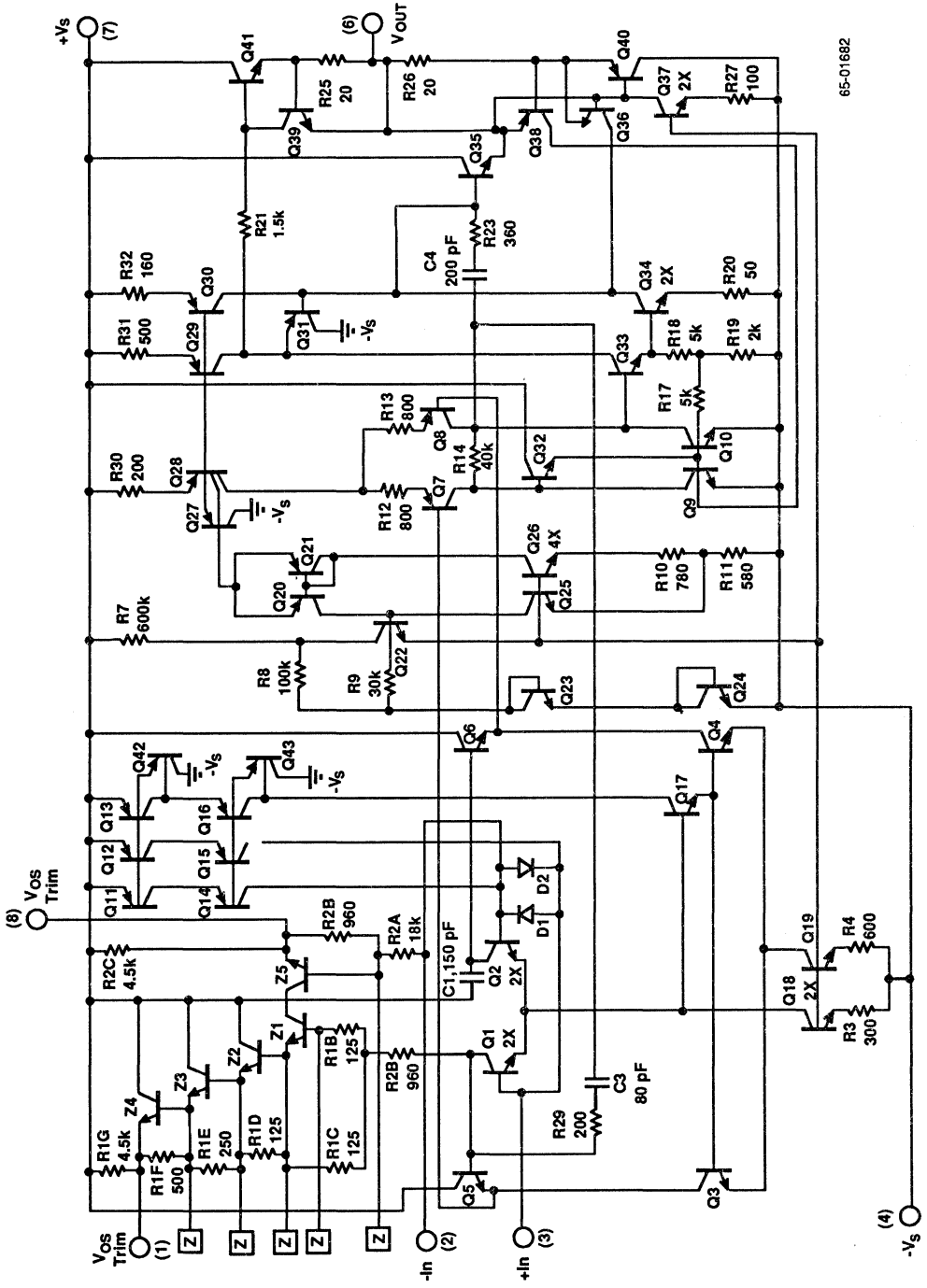


Figure 2. Three Op Amp IC Instrumentation Amplifier

Schematic Diagram



OP-77 Series Precision Operational Amplifiers

Features

- Ultra high gain – 5000 V/mV min
- Outstanding gain linearity
- Ultra low V_{os} drift – 0.3 μV/°C max
- Low V_{os} – 25 μV max
- Low noise – 0.3 μV_{p-p} (0.1 to 10 Hz)
- Low power consumption – 35 mW
- Low input offset current – 1.5 nA max
- High CMRR – 120 dB min
- High PSRR – 110 dB min
- Replaces OP-07, 108, 725, 741 types
- Wide range of package types

Description

Designed to upgrade OP-07 and other similar precision op amps, the OP-77 offers ultra high performance in applications requiring high gain, superior gain-linearity, and extremely low TCV_{os}. The OP-77's outstanding gain-linearity, which eliminates incorrectable system nonlinearities common in previous precision op amps, is achieved by an exceptional open-loop gain of more than 10 million maintained over ±10V output range. The excellent TCV_{os} of 0.3 μV/°C maximum, plus an extremely low power consumption of 35 mW (which reduces warm-up drift) significantly increases system accuracy over temperature. These characteristics, along with low V_{os}, low I_{os}, high CMRR, high PSRR, and low input noise levels, combine to raise the performance level of many high-resolution instrumentation and data conversion systems.

Advanced circuit design and wafer processing are Raytheon's added advantages in quality and reliability. A patented, proprietary V_{os} trimming method after packaging significantly enhances yield and availability of top grade (A/E) devices.

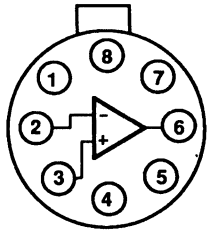
Ordering Information

Part Number	Package	Operating Temperature Range
OP-77EN	N	0°C to +70°C
OP-77FN	N	0°C to +70°C
OP-77GN	N	0°C to +70°C
OP-77FM	M	0°C to +70°C
OP-77GM	M	0°C to +70°C
OP-77ET	T	-25°C to +85°C
OP-77FT	T	-25°C to +85°C
OP-77ED	D	-25°C to +85°C
OP-77FD	D	-25°C to +85°C
OP-77AT	T	-55°C to +125°C
OP-77AT/883B*	T	-55°C to +125°C
OP-77BT	T	-55°C to +125°C
OP-77BT/883B*	T	-55°C to +125°C
OP-77AD	D	-55°C to +125°C
OP-77AD/883B*	D	-55°C to +125°C
OP-77BD	D	-55°C to +125°C
OP-77BD/883B*	D	-55°C to +125°C
OP-77AL/883B*	L	-55°C to +125°C
OP-77BL/883B*	L	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

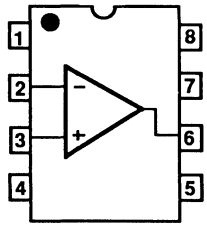
Connection Information

8-Lead TO-99 Metal Can
(Top View)



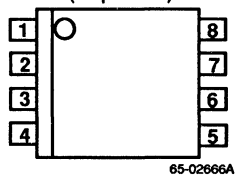
65-03205A

8-Lead Dual In-Line Package
(Top View)



65-03206A

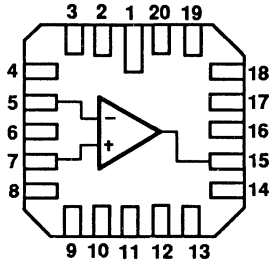
8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

Pin	Function
1	V_{os} Trim
2	-Input
3	+Input
4	$-V_s$(Case)
5	NC
6	Output
7	$+V_s$
8	V_{os} Trim

20-Pad LCC
(Top View)



65-02657A

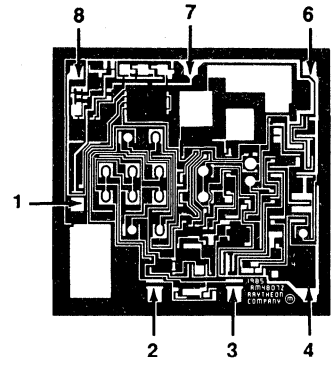
2	V_{os} Trim
5	-Input
7	+Input
10	$-V_s$
15	Output
17	$+V_s$
20	V_{os} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
OP77A,B ..... -55°C to +125°C
OP77E,F,G (Hermetic) ..... -25°C to +85°C
OP77E,F,G (Plastic) ..... 0°C to +70°C
Lead Soldering Temperature
TO-99, DIP, LCC (60 sec) ..... +300°C
SO-8 (10 sec) ..... +260°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



65-4020

Die Size: 75 x 78 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	20-Pad LCC	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic SO	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	175°C	125°C	125°C
Max. P_D T_A <50°C	925 mW	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	37°C/W	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	105°C/W	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	7.0 mW/°C	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-77A			OP-77B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			±10	±25		±20	±60	µV
Long Term V_{OS} Stability[1]			0.2			0.2		µV/Mo
Input Offset Current			±0.3	±1.5		±0.3	±2.8	nA
Input Bias Current			±1.2	±2.0		±1.2	±2.8	nA
Input Noise Voltage[5]	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.65	μV_{p-p}
Input Noise Voltage Density[5]	F_O = 10 Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10	13		10	13	
	F_O = 1000 Hz		9.6	11		9.6	11	
Input Noise Current[5]	0.1 Hz to 10 Hz		14	30		14	35	pA_{p-p}
Input Noise Current Density[5]	F_O = 10 Hz		0.32	0.8		0.32	0.8	$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14	0.23		0.14	0.23	
	F_O = 1000 Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[2]		26	45		18.5	45		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range[4]		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±11V	120	140		116	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±8V	110	120		110	120		dB
Large Signal Voltage Gain	R_L ≥2 kΩ, V_O = ±10V	5000	12000		2000	8000		V/mV
Output Voltage Swing	R_L ≥10 kΩ,	±13	±13.5		±13	±13.5		V
	R_L ≥2 kΩ,	±12.5	±13		±12.5	±13		
	R_L ≥1 kΩ,	±12	±12.5		±12	±12.5		
Slew Rate[2]	R_L ≥2 kΩ,	0.1	0.2		0.1	0.2		V/µS
Closed Loop Bandwidth[2]	A_{VCL} = +1.0	0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		35	60		35	60	mW
	V_S = ±3V, R_L = ∞		2.0	4.5		2.0	4.5	
Offset Adjustment Range	R_P = 20 kΩ		±3.5			±3.5		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The OP-77A/E grades in T, D, and L packages are tested fully warmed up.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
5. Sample tested.

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-77E			OP-77F			OP-77G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]			±10	±25		±20	±60		±50	±100	µV
Long Term Input Offset Voltage Stability[1]			0.3			0.4			0.4		µV/Mo
Input Offset Current			±0.3	±1.5		±0.3	±2.8		±0.3	±2.8	nA
Input Bias Current			±1.2	±2.0		±1.2	±2.8		±1.2	±2.8	nA
Input Noise Voltage[5]	0.1 Hz to 10 Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
Input Noise Voltage Density[5]	F_O = 10 Hz		10.3	18		10.5	20		10.5	20	nV/√Hz
	F_O = 100 Hz		10	13		10.2	13.5		10.2	13.5	
	F_O = 1000 Hz		9.6	11		9.8	11.5		9.8	11.5	
Input Noise Current[5]	0.1 Hz to 10 Hz		14	30		15	35		15	35	pA_{p-p}
Input Noise Current Density[5]	F_O = 10 Hz		0.32	0.8		0.35	0.9		0.35	0.9	pA/√Hz
	F_O = 100 Hz		0.14	0.23		0.15	0.27		0.15	0.27	
	F_O = 1000 Hz		0.12	0.17		0.13	0.18		0.13	0.18	
Input Resistance (Diff. Mode)[2]		26	45		18.5	45		18.5	45		MΩ
Input Resistance (Com. Mode)			200			200			200		GΩ
Input Voltage Range[4]		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	120	140		116	140		116	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	110	123		110	123		110	123		dB
Large Signal Voltage Gain	R_L ≥2 kΩ, V_O = ±10V	5000	12000		2000	6000		2000	6000		V/mV
Output Voltage Swing	R_L ≥10 kΩ	±13	±13.5		±13	±13.5		±13	±13.5		V
	R_L ≥2 kΩ	±12.5	±13		±12.5	±13		±12.5	±13		
	R_L ≥1 kΩ	±12	±12.5		±12	±12.5		±12	±12.5		
Slew Rate[2]	R_L ≥2 kΩ	0.1	0.2		0.1	0.2		0.1	0.2		V/µS
Closed-Loop Bandwidth[2]	A_{VCL} = +1.0	0.4	0.6		0.4	0.6		0.4	0.6		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		35	60		35	60		35	60	mW
	V_S = ±3V, R_L = ∞		2.0	4.5		2.0	4.5		2.0	4.5	
Offset Adjustment Range	R_P = 20 kΩ		±3.5			±3.5			±3.5		mV

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The OP-77A/E grades on T, D, and L packages are tested fully warmed up.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
5. Sample tested.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

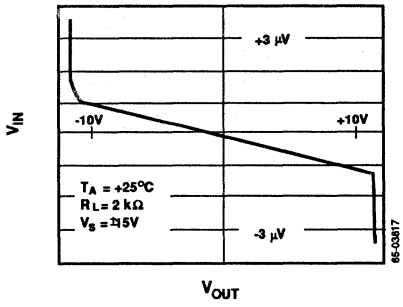
Parameters	Test Conditions	OP-77A			OP-77B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			±25	±60		±45	±120	µV
Average Input Offset Voltage Drift[1]			0.1	0.3		0.2	0.6	µV/°C
Input Offset Current			±0.8	±2.2		±1.0	±4.5	nA
Average Input Offset Current Drift[2]			±5.0	±25		±5.0	±50	pA/°C
Input Bias Current			±2.4	±4.0		±2.4	±6.0	nA
Average Input Bias Current Drift[2]			±8.0	±25		±15	±35	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM}= ±10V	120	140		110	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±8V	110	120		106	120		dB
Large Signal Voltage Gain	R_L ≥2 kΩ, V_O = ±10V	2000	6000		1000	4000		V/mV
Maximum Output Voltage Swing	R_L ≥2 kΩ,	±12	±13		±12	±13		V
Power Consumption	R_L = ∞		40	75		40	75	mW

Electrical Characteristics

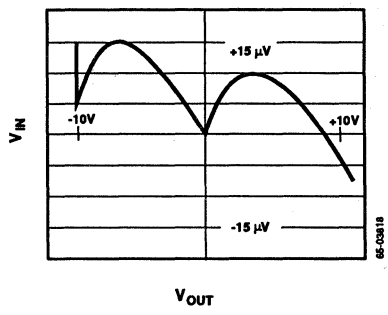
(V_S = ±15V; -25°C ≤ T_A ≤ +85°C for T, D, and L packages; 0°C ≤ T_A ≤ +70°C for N and M packages unless otherwise noted)

Parameters	Test Conditions	OP-77E			OP-77F			OP-77G			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			±10	±45		±20	±100		±80	±100	µV
Average Input Offset Voltage Drift			0.1	0.3		0.2	0.6		0.3	1.2	µV/°C
Input Offset Current			±0.5	±2.2		±0.5	±4.5		±0.5	±4.5	nA
Average Input Offset Current Drift[2]			±1.5	±40		±1.5	±85		±1.5	±85	pA/°C
Input Bias Current			±2.4	±4.0		±2.4	±6.0		±2.4	±6.0	nA
Average Input Bias Current Drift[2]			±8	±40		±15	±60		±15	±60	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM}= ±13V	120	140		110	140		110	140		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	110	120		106	120		106	120		dB
Large Signal Voltage Gain	R_L ≥2 kΩ, V_O = ±10V	2000	6000		1000	4000		1000	4000		V/mV
Output Voltage Swing	R_L ≥2 kΩ	±12	±13		±12	±13		±12	±13		V
Power Consumption	R_L = ∞		40	75		40	75		40	75	mW

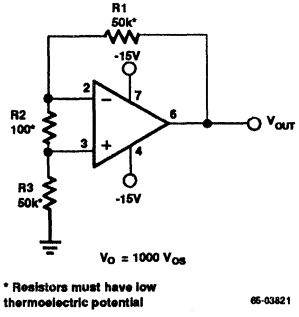
Notes:
1. 100% tested for Grade A on T, and L packages.
2. Sample tested.



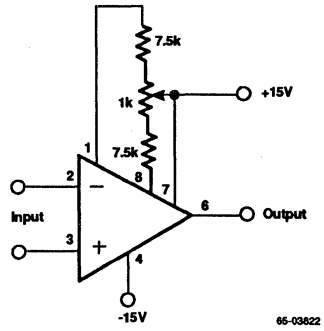
OP-77 Improved Open-Loop Gain Linearity



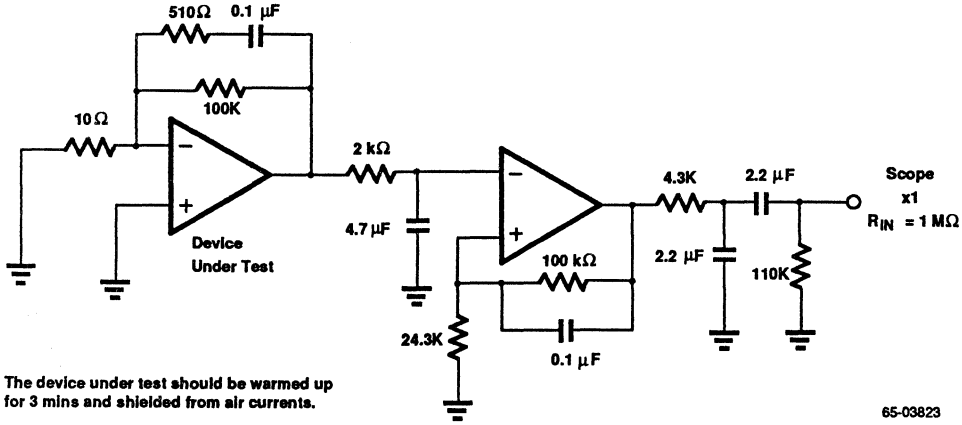
Typical Precision Op Amp Gain Linearity



Test Circuit for Offset Voltage and Its Drift With Temperature

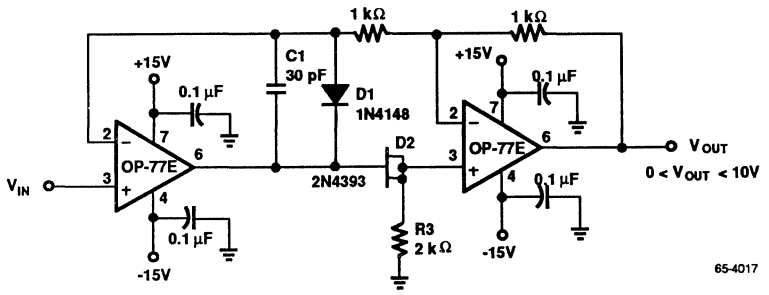


Improved Sensitivity V_{OS} Adjustment



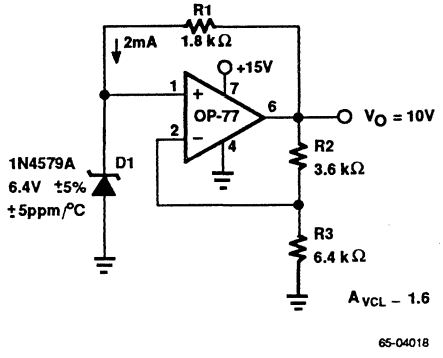
0.1 Hz to 10 Hz Noise Test Circuit
(peak to peak noise measured in 10 sec interval)

Typical Applications



The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP-77E CMRR of 1 µV/V assures errors of less than 2 ppm.

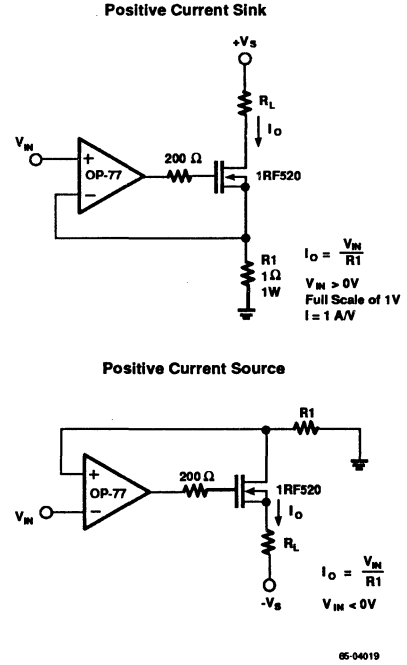
Precision Absolute Value Amplifier



This simple bootstrapped voltage reference provides a precise 10V virtually independent of changes in power supply voltage, ambient temperature and output loading. Correct zener operating current of exactly 2 mA is maintained by R1, a selected 5 ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5 ppm/°C temperature coefficient of D1, 1 ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

V_{OS} errors, amplified by 1.6 (A_{VCL}), appear at the output and can be significant with most monolithic amplifiers. For example: an ordinary amplifier with TCV_{OS} of 5 µV/°C contributes 0.8 ppm/°C of output error while the OP-77, with TCV_{OS} of 0.3 µV/°C, contributes but 0.05 ppm/°C of output error, thus effectively eliminating TCV_{OS} as an error consideration.

High Stability Voltage Reference

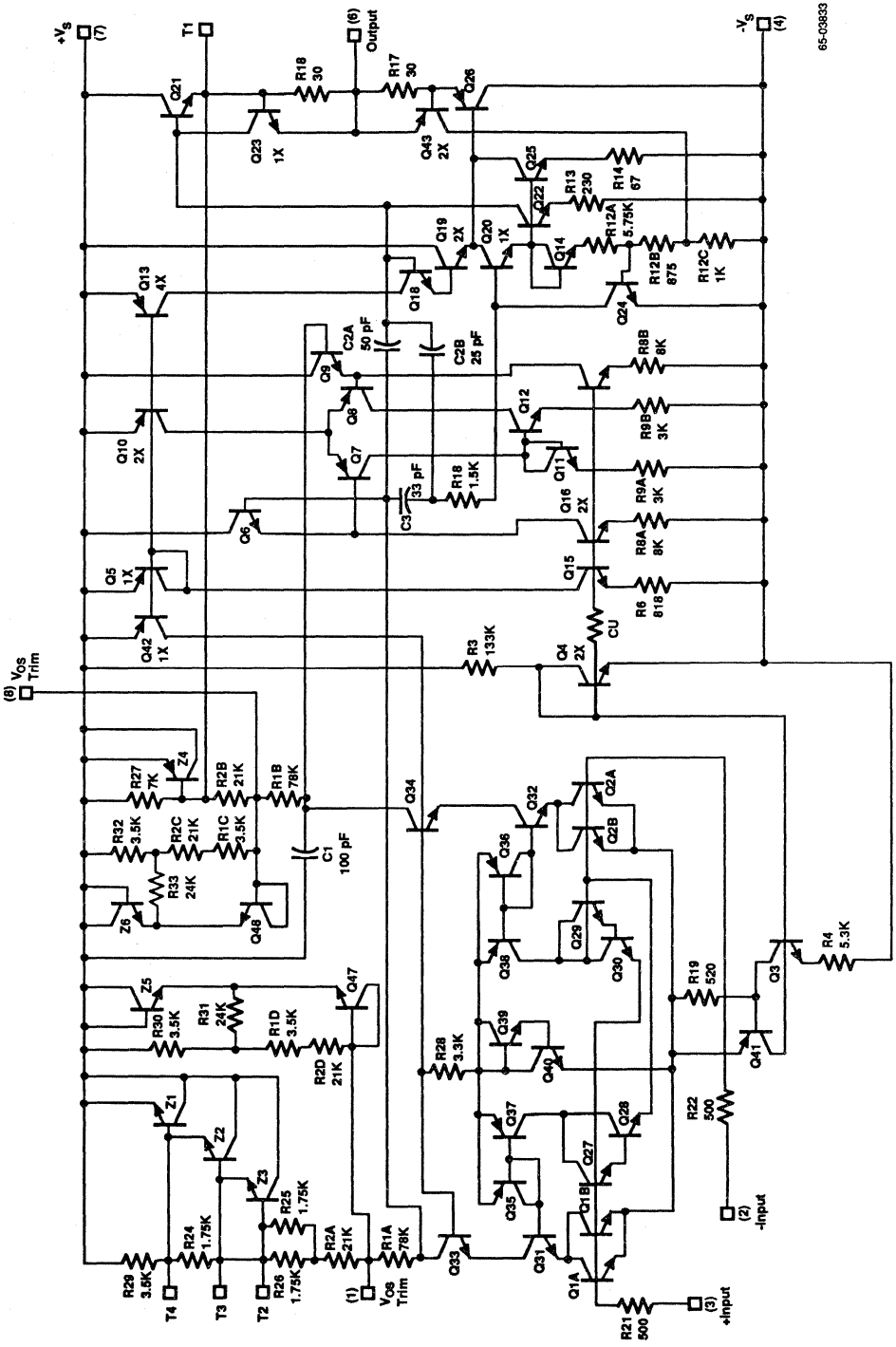


These simple high current sinks require that the load float between the power supply and the sink.

In these circuits, OP-77's high gain, high CMRR, and low TCV_{OS} assure high accuracy.

Precision Current Sinks

Simplified Schematic Diagram



RC4097 Series Low-Power, High Precision Operational Amplifiers

Features

- Low input offset voltage — 15 μV max
- Low V_{OS} drift — 0.3 μV/°C max
- Low input bias current —
  +25°C, 100 pA max
  -55°C to +125°C, 600 pA max
- High gain — 1000 V/mV min
- High CMRR — 120 dB min
- High PSRR 114 dB min
- Low supply current — 600 μA max
- Low noise — 0.5 μV_{p-p} (0.1 to 10 Hz)
- Replaces OP-97, LT1012

Description

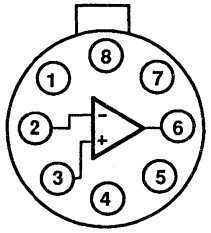
The RC4097 is a micropower device that can be used to improve the performance of a wide range of precision operational amplifier applications. Essentially, a low-power idling current, low I_B version of the popular OP-07 industry type, the RC4097 can replace FET-input op amps in circuits requiring low input bias currents while realizing significant improvements in voltage noise, V_{OS}, and V_{OS} drift. The other input specifications, such as CMRR and PSRR, support the high level of precision performance, allowing upgrading of many instrumentation, low-level signal conditioning, sample-and-hold, and data conversion applications.

The superb performance of the RC4097 is a result of advanced design and processing techniques, including post-package trimming of the input offset voltage, and superbeta processing of the input transistors. Picoampere input bias currents are maintained over the full military temperature range through the use of bias cancellation techniques in the design of the input stage. The RC4097 offers lower V_{OS} drift, lower V_{OS}, higher open-loop gain , and better CMRR than industry-standard OP-97 or LT1012 types.

The RC4097 is available in 8-lead plastic or ceramic DIPs, TO-99 metal cans, and plastic small outline packages. Military, industrial, and commercial temperature ranges can be selected, and Mil-Std-883B processing is available.

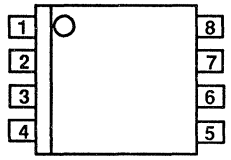
Connection Information

8-Lead TO-99 Metal Can
(Top View)



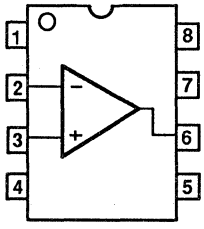
65-03205A

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

8-Lead Dual In-Line Package
(Top View)



65-03206A

Pin	Function
1	V_{os} Trim
2	-Input
3	+Input
4	$-V_s$
5	NC
6	Output
7	$+V_s$
8	V_{os} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
RC4097AN	N	0°C to +70°C
RC4097EN	N	0°C to +70°C
RC4097FN	N	0°C to +70°C
RC4097EM	M	0°C to +70°C
RC4097FM	M	0°C to +70°C
RV4097ET	T	-25°C to +85°C
RV4097FT	T	-25°C to +85°C
RV4097ED	D	-25°C to +85°C
RV4097FD	D	-25°C to +85°C
RM4097AT	T	-55°C to +125°C
RM4097AT/883B	T	-55°C to +125°C
RM4097AD	D	-55°C to +125°C
RM4097AD/883B	D	-55°C to +125°C

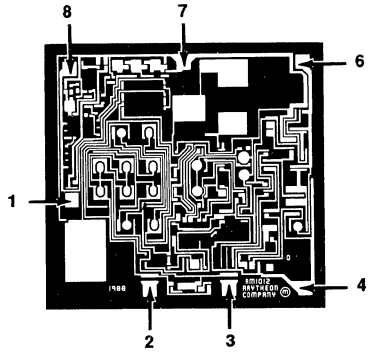
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4097A ..... -55°C to +125°C
RV4097E,F (Hermetic) ..... -25°C to +85°C
RC4097A,E,F (Plastic) ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8, 10 sec) ..... +260°C
(DIP, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



65-4238

Die Size: 75 x 78 mils
Min Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Small Outline	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	125°C	125°C
Max. P_D T_A <50°C	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4097A/E			4097F			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[3]	RC/RM4097A RC4097E		±7.0 ±15	±15 ±25		±20	±60	µV
Long Term V_{OS} Stability[1]			0.2			0.4		µV/Mo
Input Offset Current			30	100		30	150	pA
Input Bias Current			±30	±100		±30	±150	pA
Input Noise Voltage[5]	0.1 Hz to 10 Hz		0.5			0.5		μV_{p-p}
Input Noise Voltage Density[5]	F_O = 10 Hz		17	30		17	30	$\frac{nV}{\sqrt{Hz}}$
	F_O = 1000 Hz		14	22		14	22	
Input Noise Current Density[5]	F_O = 10 Hz		20			20		$fA/\sqrt{Hz}$
Input Resistance (Diff Mode)[2]		30			30			MΩ
Input Voltage Range[4]		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	120	140		110	130		dB
Power Supply Rejection Ratio	V_S = ±2.5V to ±20V	114	128		110	128		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	1000	2500		600	2500		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±13	±13.5		±13	±13.5		V
Slew Rate		0.1	0.3		0.1	0.3		V/µS
Closed Loop Bandwidth[2]	A_{VCL} = +1.0	0.4	0.8		0.4	0.8		MHz
Power Consumption	V_S = ±15V, R_L = ∞		12	18		12	18	mW
Supply Voltage Range	Operating	±2.5		±20	±2.5		±20	V

Notes:
1. Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 µV.
2. Guaranteed by design.
3. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. The RC/RM4097A grades are tested fully warmed up.
4. The input protection diodes do not allow the device to be removed or inserted into the circuit without first removing power.
5. Sample tested.

Electrical Characteristics (V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	4097A/E			4097F			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	RC4097A RC4097E/F		10 20	30 55		 35	 115	µV
Average Input Offset Voltage Drift[1]	RC4097A RC4097E/F		0.1 0.2	0.3 0.6		04 0.4	1.2 1.2	µV/°C
Input Offset Current			60	250		80	500	pA
Average Input Offset Current Drift[2]			0.6	7.8		1.1	15	pA/°C
Input Bias Current			±60	±250		±80	±500	pA
Average Input Bias Current Drift[2]			0.6	7.8		2.8	15	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	114	128		108	126		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±20V	108	126		108	126		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_O = ±10V	600	1500		400	1200		V/mV
Maximum Output Voltage Swing	R_L ≥ 10 kΩ	±12	±13		±12	±13		V
Power Consumption	R_L = ∞		14	24		14	24	mW
Supply Voltage Range	Operating	±3		±20	±3		±20	V

Notes:
1. 100% tested for A Grade .
2. Sample tested.

Electrical Characteristics ($V_S = \pm 15V, -25°C \leq T_A \leq +85°C$ unless otherwise noted)

Parameters	Test Conditions	4097E			4097F			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			25	60		40	130	µV
Average Input Offset Voltage Drift[1]			0.2	0.6		0.4	1.2	µV/°C
Input Offset Current			100	600		200	750	pA
Average Input Offset Current Drift[2]			1.1	11.7		2.8	15	pA/°C
Input Bias Current			±100	±600		±200	±750	pA
Average Input Bias Current Drift[2]			1.1	11.7		2.8	15	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	114	128		108	126		dB
Power Supply Rejection Ratio	$V_S = \pm 3.0V$ to $\pm 20V$	108	126		108	126		dB
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_O = \pm 10V$	600	1500		400	1200		V/mV
Maximum Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±13		±12	±13		V
Power Consumption	$R_L = \infty$		14	24		14	24	mW
Supply Voltage Range	Operating	±3		±20	±3		±20	V

Notes:
1. 100% tested for A Grade.
2. Sample tested.

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	RM4097A			Units
		Min	Typ	Max	
Input Offset Voltage			20	45	µV
Average Input Offset Voltage Drift[1]			0.1	0.3	µV/°C
Input Offset Current			100	600	pA
Average Input Offset Current Drift[2]			0.7	7.0	pA/°C
Input Bias Current			±100	±600	pA
Average Input Bias Current Drift[2]			0.7	7.0	pA/°C
Input Voltage Range		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±10V	114	130		dB
Power Supply Rejection Ratio	V_S = ±4.0V to ±20V	108	126		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	600	1200		V/mV
Maximum Output Voltage Swing	$R_L \geq 10$ kΩ	±13	±13.5		V
Power Consumption	$R_L = \infty$		15	24	mW
Supply Voltage Range		±3.0		±20	V

Notes:
1. 100% tested for A Grade.
2. Sample tested.

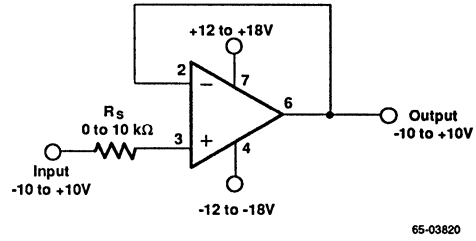
Offset Voltage Adjustment

The input offset voltage of the RC4097, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of V_{os} is necessary, nulling with a 10K or 20K potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{os}/300) μV/°C, e.g., if V_{os} is adjusted to 300 μV, the change in drift will be 1 μV/°C. The adjustment range with a 10K or 20K potentiometer is approximately 4.0 mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example on page 9 has an approximate null range of ±100 μV.

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

RC4097 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The RC4097 can also be used in 741 applications provided that the nulling circuitry is removed.

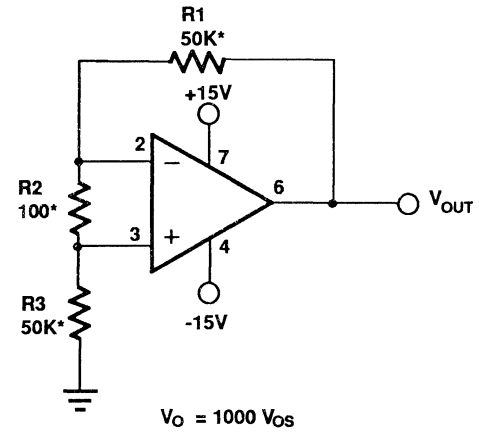
The voltage follower is an ideal example illustrating the overall excellence of the RC4097. The contributing error terms are due to offset voltage, input bias current, voltage gain, common-mode and power-supply rejections. Worst-case summation of guaranteed specifications is tabulated below.



Large Signal Voltage Follower With 0.00065% Worst-Case Accuracy Error

Output Accuracy

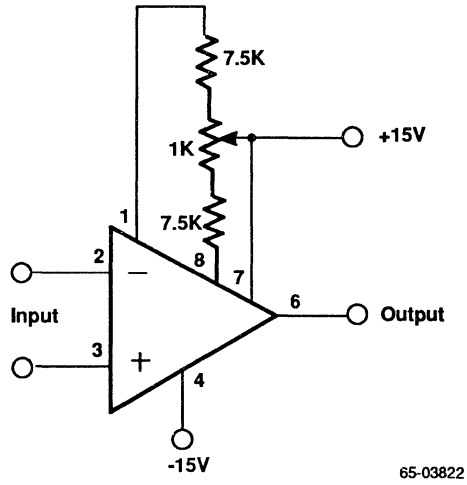
Error	RM4097A 25°C Max (μV)	RM4097A -55 to +125°C Max (μV)	RC4097A 0°C to +70°C Max (μV)
Offset Voltage	15	45	30
Bias Current	1.0	6	2.5
CMRR	20	40	40
PSRR	12	24	24
Voltage Gain	20	33	33
Worst Case Sum	68	148	129.5
Percent of Full Scale (= 20V)	.00034%	.00074%	.00065%



* Resistors must have low thermoelectric potential

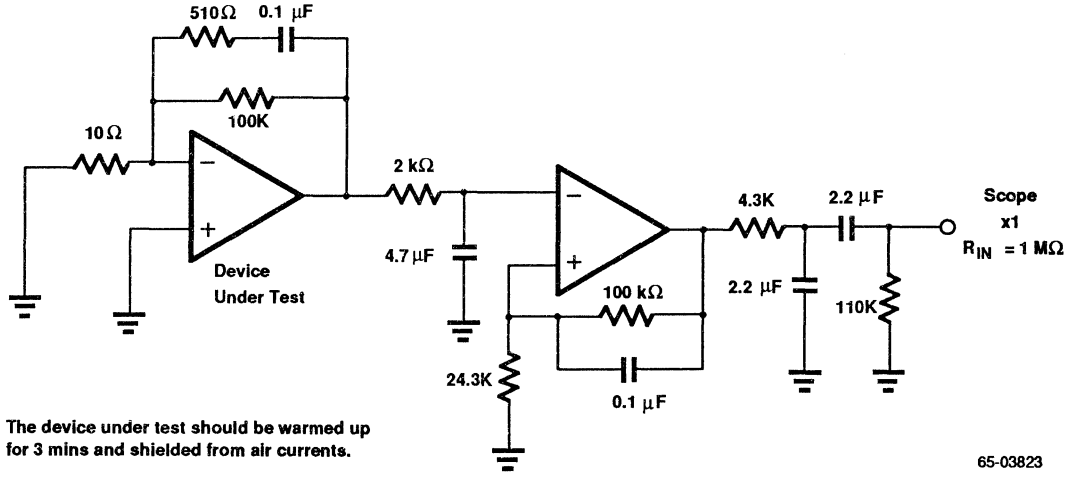
65-03821

Test Circuit for Offset Voltage and Its Drift With Temperature



65-03822

Improved Sensitivity V_{OS} Adjustment

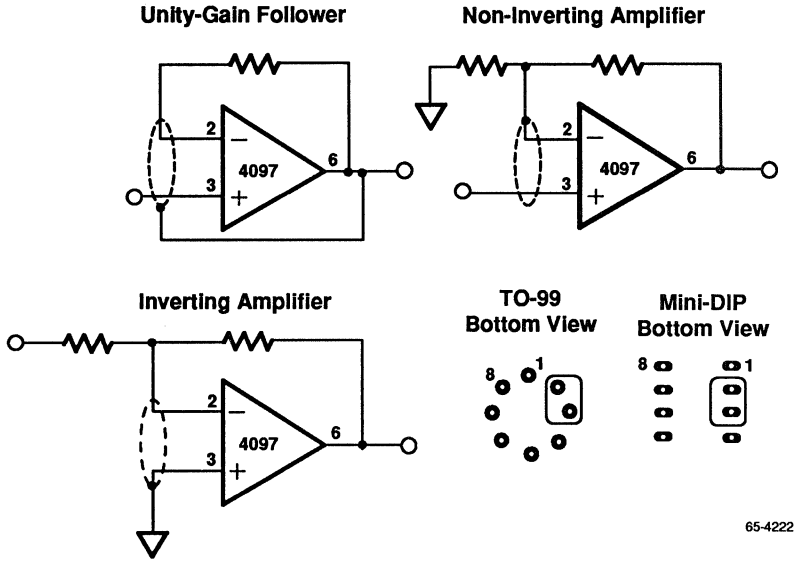


The device under test should be warmed up for 3 mins and shielded from air currents.

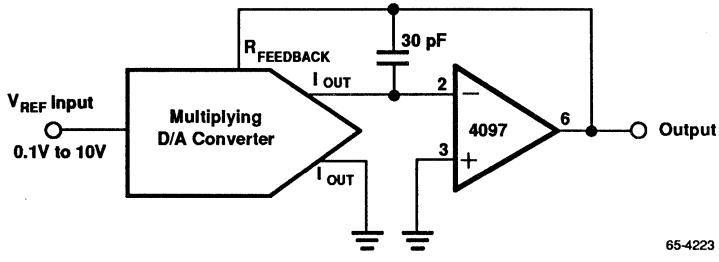
65-03823

0.1 Hz to 10 Hz Noise Test Circuit (peak-to-peak noise measured in 10-sec intervals)

Typical Applications

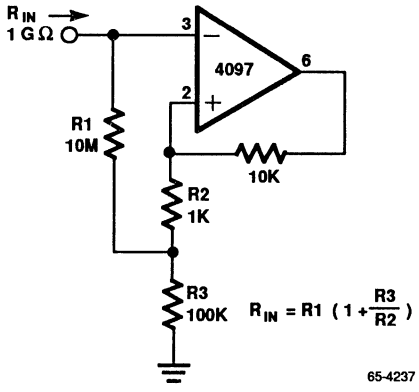


Guard Ring Layout and Connections

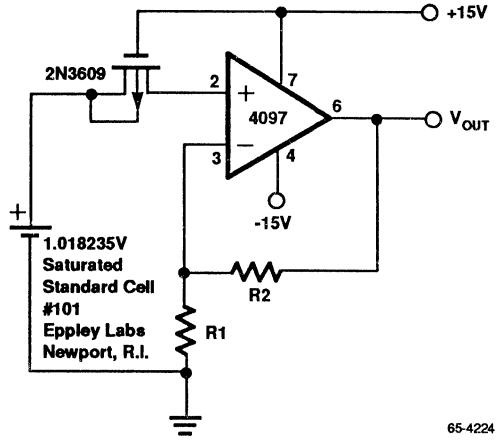


Wide Dynamic Range Multiplying DAC

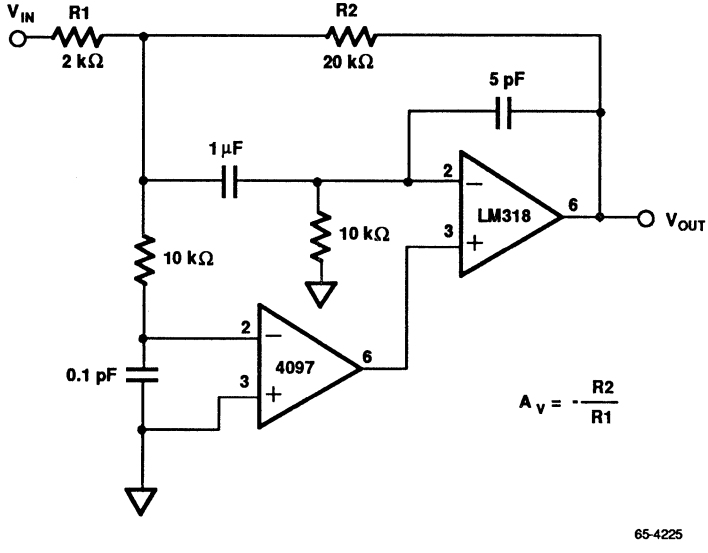
Typical Applications (Continued)



Resistor Multiplier

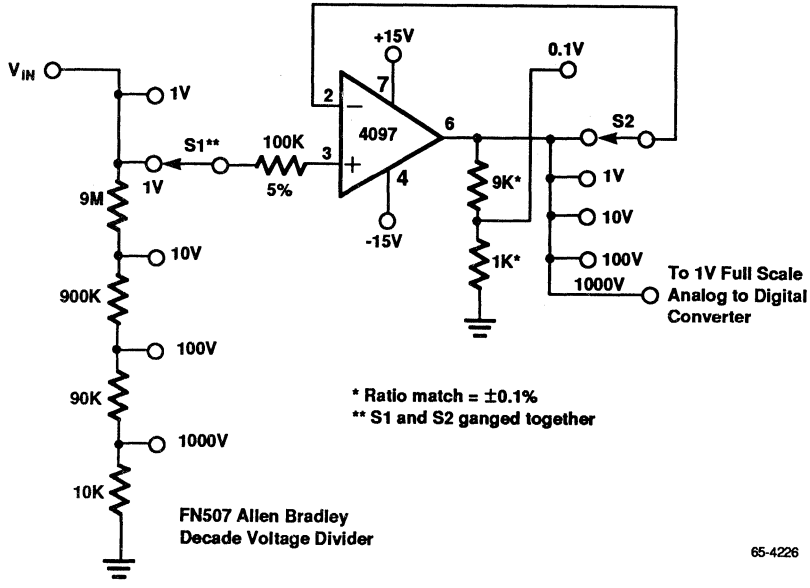


Long-Life Standard Cell Amplifier

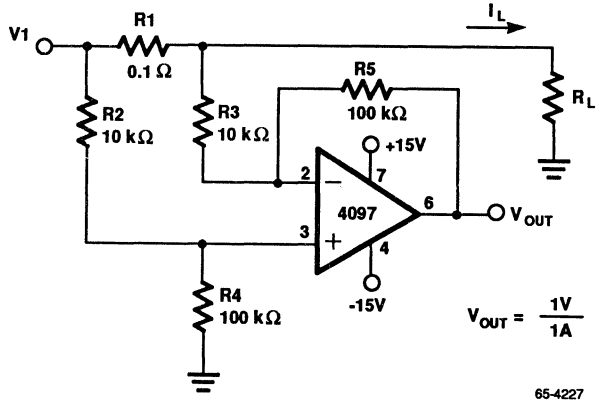


Composite High-Speed, Precision Amplifier

Typical Applications (Continued)

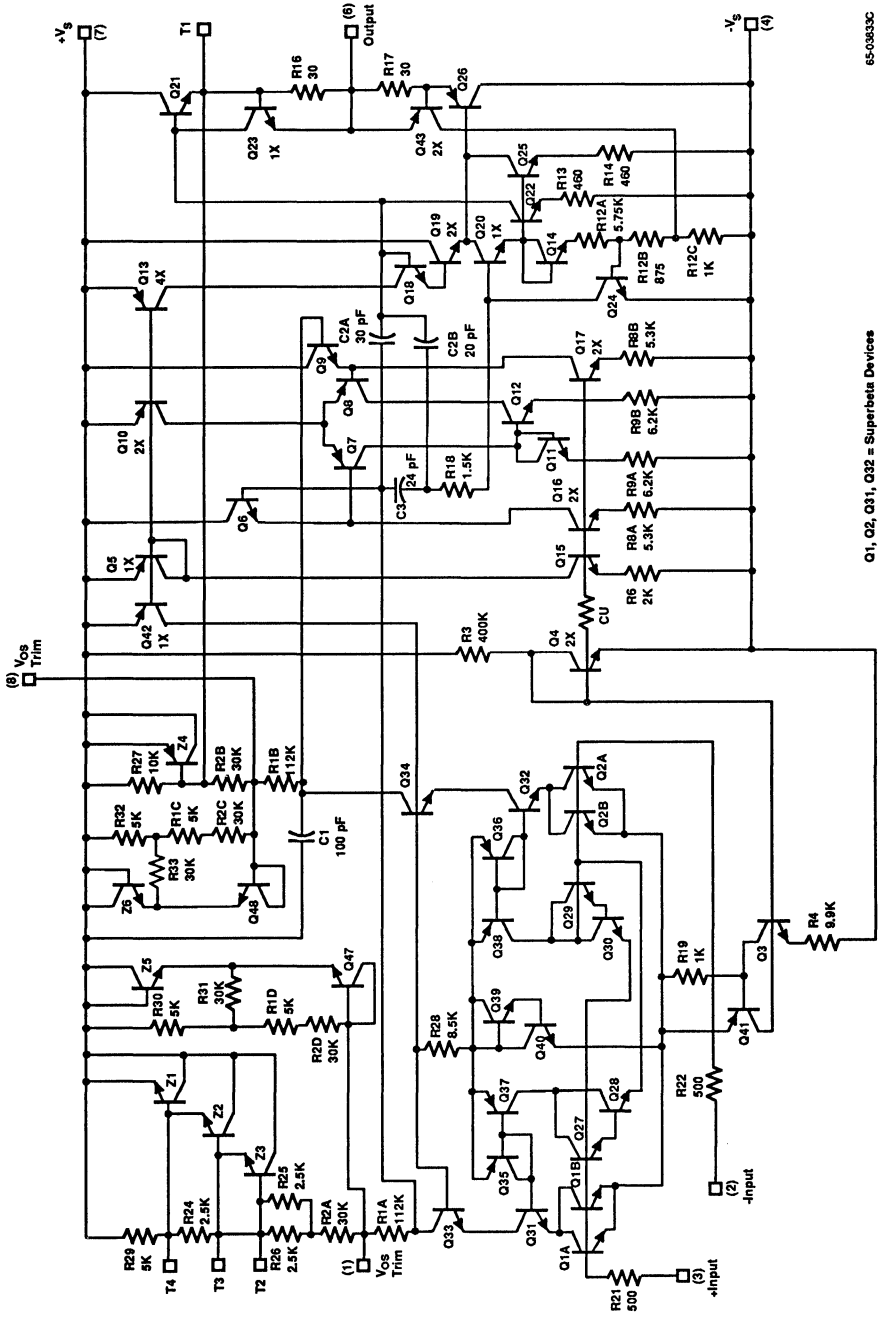


Input Amplifier for 4-1/2 Digit Voltmeter



Precision Current Monitor

Schematic Diagram



RC741 General Purpose Operational Amplifier

Features

- Supply voltages
  RC/RV741 — ±18V
  RM741 — ±22V
- Offset voltage null capability
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption

Description

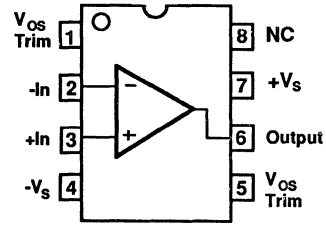
The RC741 integrated circuit is a high-performance, high-gain, internally compensated monolithic operational amplifier fabricated on a single silicon chip using an advanced epitaxial process.

High common-mode voltage range and absence of latch-up tendencies make the RC741 ideal for use as a voltage follower. High gain and wide ranges of operating voltages provide superior performance in integrator, summing amplifier and general feedback applications.

The RC741 is pin compatible with the RM709, LM101A and the LM107. The military version, RM741 operates over a temperature range from -55°C to +125°C. The commercial version, RC741, operates from 0°C to +70°C. The industrial version, RV741, operates from -25°C to +85°C.

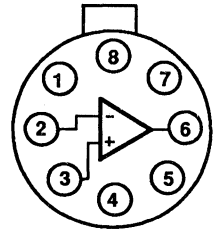
Connection Information

8-Lead
Dual In-Line Package
(Top View)



65-0939

8-Lead
TO-99 Metal Can
(Top View)



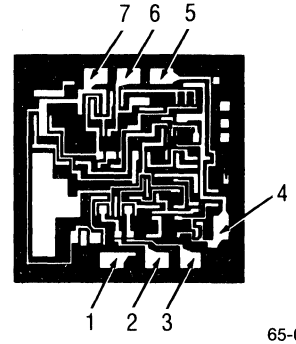
65-03205A

Ordering Information

Part Number	Package	Operating Temperature Range
RC741N	N	0°C to +70°C
RV741D	D	-25° C to +85°C
RV741T	T	-25° C to +85°C
RV741N	N	-25° C to +85°C
RM741D	D	-55°C to +125°C
RM741D/883B	D	-55°C to +125°C
RM741T	T	-55°C to +125°C
RM741T/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can TO-99
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Mask Pattern



65-01178A

Die Size: 55 x 55 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage
- RC/RV741 ..... ±18V
- RM741 ..... ±22V

Differential Input Voltage 30V
Input Voltage* ..... ±15V
Output Short Circuit Duration** ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- RM741 ..... -55°C to +125°C
- RV741 ..... -25°C to +85°C
- RC741 ..... 0°C to +70°C

Lead Soldering Temperature
- (60 sec) ..... +300°C

*For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
** Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RM741.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D T_A <50°C	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25° C unless otherwise noted)

Parameters	Test Conditions	RM741			RC/RV741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance (Differential Mode)		0.3	2.0		0.3	2.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	200		20	200		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	90		76	30		dB
Power Consumption			50	85		50	85	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.3			0.3		μS
Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Slew Rate	$R_L \geq 2k\Omega$		0.5			0.5		V/μS

Note: 1. Offset voltage is nulled by connecting a 10kΩ potentiometer across the balance pins and connecting the wiper pin to $-V_S$.

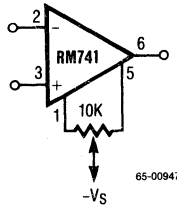
Electrical Characteristics

($-55°C \le T_A \le +125°C$ for RM741; $0°C \le T_A \le +70°C$ for RC741; $-25°C \le T_A \le +85°C$ for RV741)

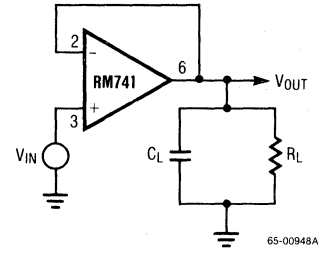
Parameters	Test Conditions	RM741			RC/RV741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_L \ge 10k\Omega$			6.0			7.5	mV
Input Offset Current				200			300	nA
Input Bias Current				1500			800	nA
Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_{OUT} = \pm 10V$	25			15			V/mV
Output Voltage Swing	$R_L \ge 10k\Omega$	±12			±12			V
	$R_L \ge 2k\Omega$	±10			±10			V
Common Mode Rejection Ratio	$R_S \le 10k\Omega$	70			70			dB
Supply Voltage Rejection Ratio	$R_S \le 10k\Omega$	76				94		dB
Supply Current	+125°C			2.5				mA
	-55°C			3.3				
Power Consumption	+125°C			75				mW
	-55°C			100				

Typical Performance Characteristics

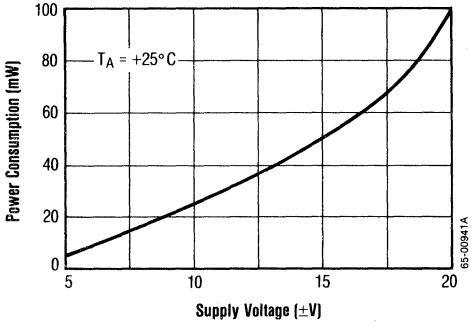
Voltage Offset Null Circuit



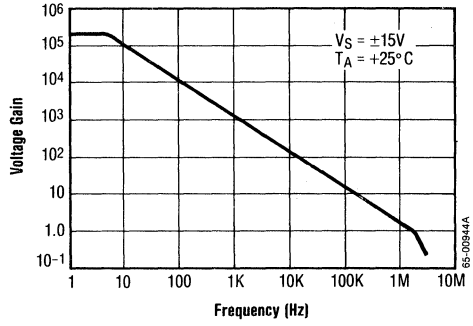
Transient Response Test Circuit



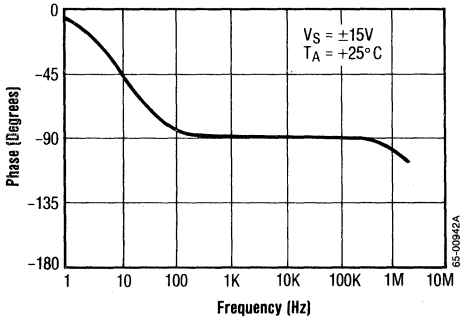
Power Consumption as a Function of Supply Voltage



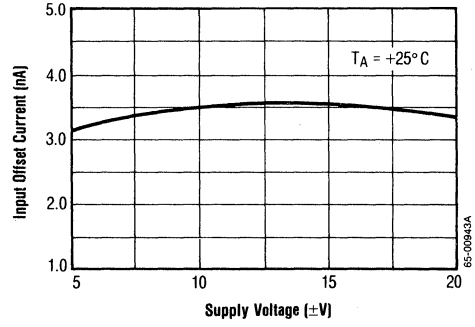
Open Loop Voltage Gain as a Function of Frequency



Open Loop Phase Response as a Function of Frequency

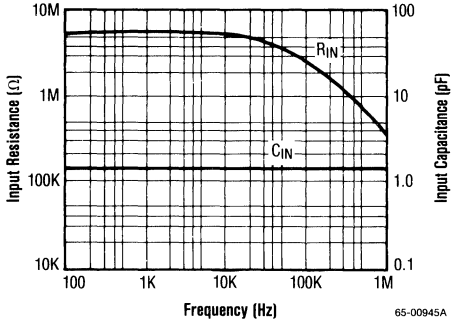


Input Offset Current as a Function of Supply Voltage

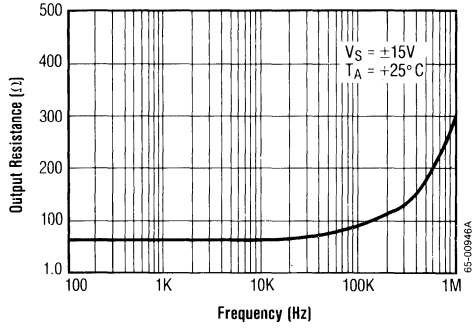


Typical Performance Characteristics (Continued)

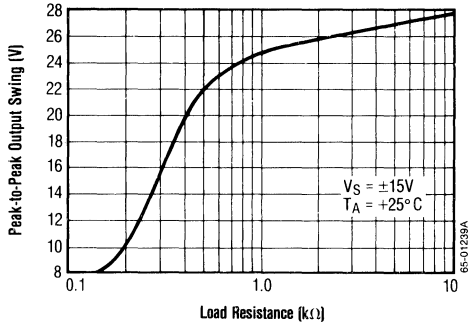
Input Resistance and Input Capacitance as a Function of Frequency



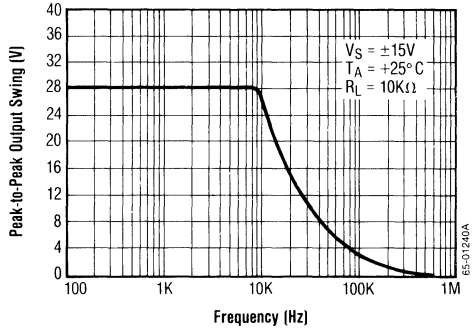
Output Resistance as a Function of Frequency



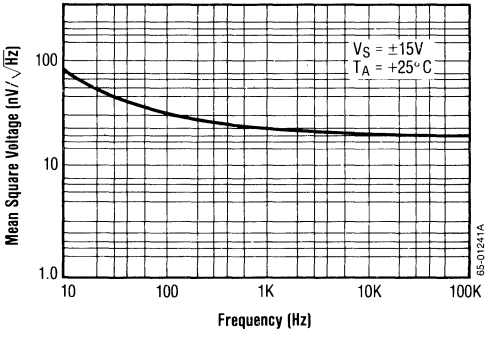
Output Voltage Swing as a Function of Load Resistance



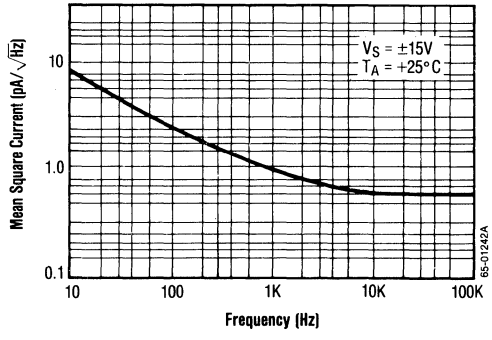
Output Voltage Swing as a Function of Frequency



Input Noise Voltage as a Function of Frequency

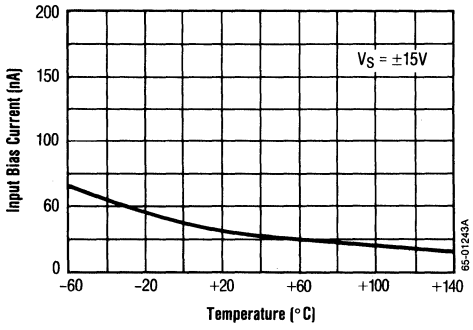


Input Noise Current as a Function of Frequency

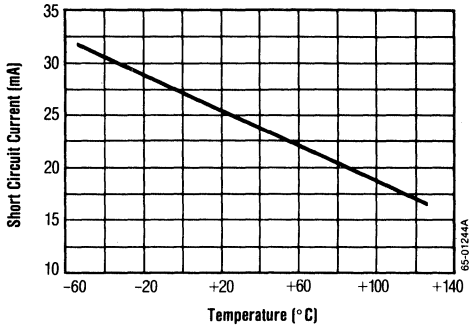


Typical Performance Characteristics (Continued)

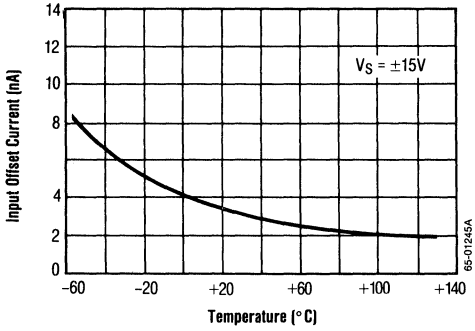
Input Bias Current as a Function of Ambient Temperature



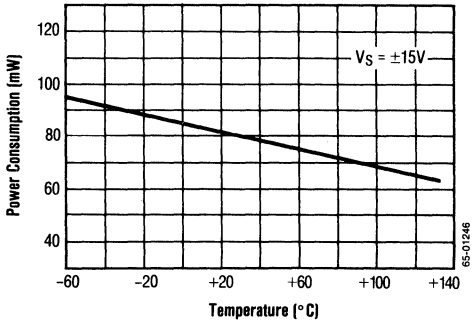
Output Short Circuit Current as a Function of Ambient Temperature



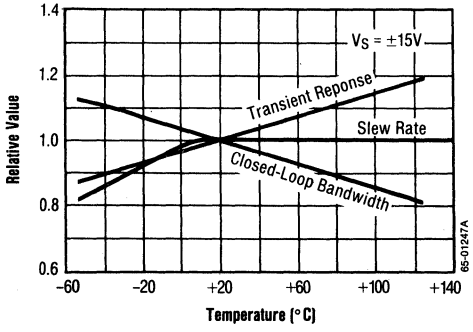
Input Offset Current as a Function of Ambient Temperature



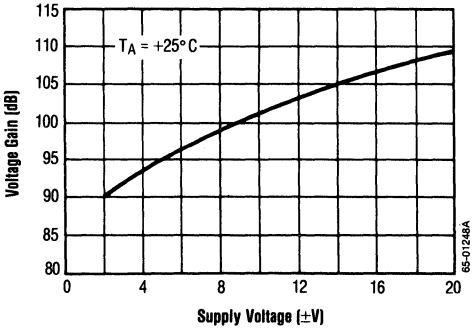
Power Consumption as a Function of Ambient Temperature



Frequency Characteristics as a Function of Ambient Temperature

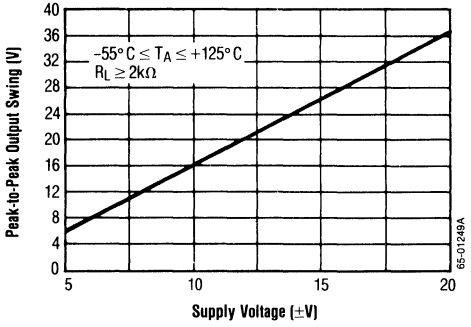


Open Loop Voltage Gain as a Function of Supply Voltage

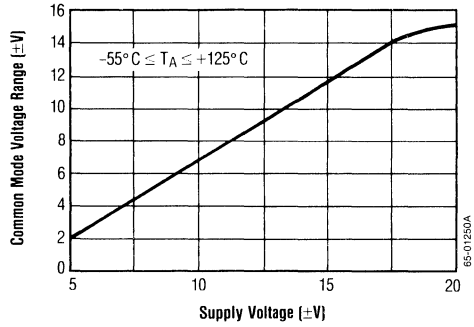


Typical Performance Characteristics (Continued)

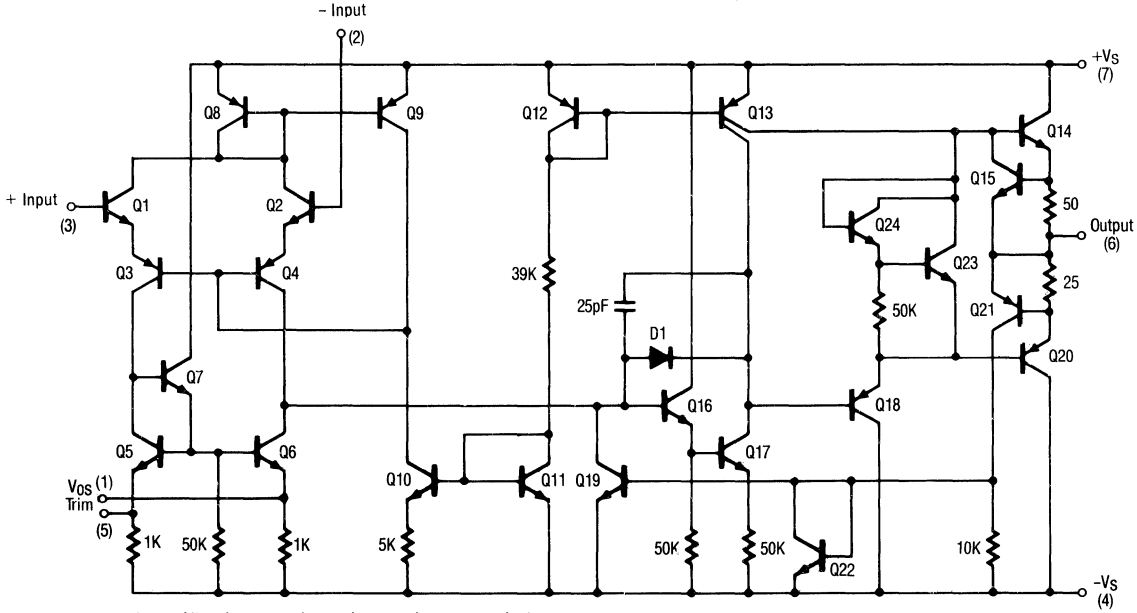
Output Voltage Swing as a Function of Supply Voltage



Input Common Mode Voltage Range as a Function of Supply Voltage



Schematic Diagram



Note: All resistance and capacitance values are nominal.

65-00940B

RC747 General Purpose Operational Amplifier

Features

- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Description

The RC/RM747 integrated circuits are high gain, operational amplifiers internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

The military version, RM747, operates over a temperature range from -55°C to +125°C. The commercial version, RC747, operates from 0°C to +70°C.

Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in all single 741 operational amplifier applications providing high packaging density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

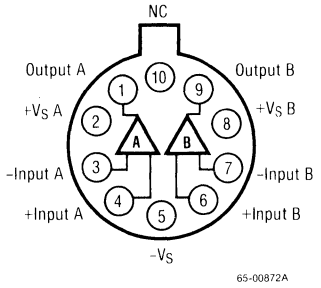
Ordering Information

Part Number	Package	Operating Temperature Range
RC747N	N	0°C to +70°C
RC747T	T	0°C to +70°C
RM747D	D	-55°C to +125°C
RM747D/883B*	D	-55°C to +125°C
RM747T	T	-55°C to +125°C
RM747T/883B*	T	-55°C to +125°C

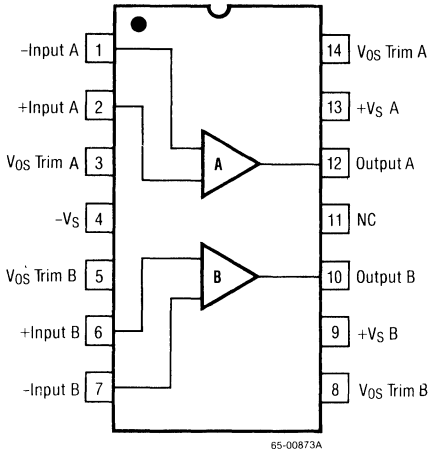
Notes:
*/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
T = 10-lead metal can TO-99
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

10-Lead TO-100 Metal Can
(Top View)



14-Lead Dual In-Line Package
(Top View)



$+V_S$ A is internally connected to $+V_S$ B for the 747S

Absolute Maximum Ratings

Supply Voltage
- RM747 ..... ±22V
- RC747 ..... ±18V

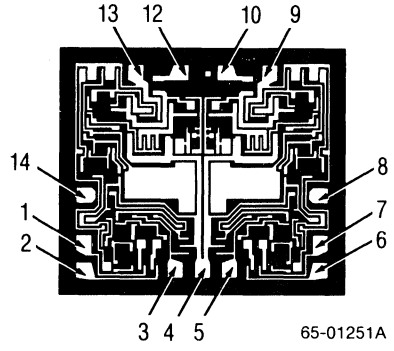
Differential Input Voltage 30V
Input Voltage* ..... ±15V
Output Short-Circuit Duration** ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- RM747 ..... -55°C to +125°C
- RC747 ..... 0°C to +70°C

Lead Soldering Temperature
- (60 sec) ..... +300°C

*For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
**Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RC747.

Mask Pattern



Die Size: 62 x 72 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP	10-Lead TO-100 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D T_A <50°C	468 mW	1042 mW	658 mW
Therm. Res θ_{JC}	—	60°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

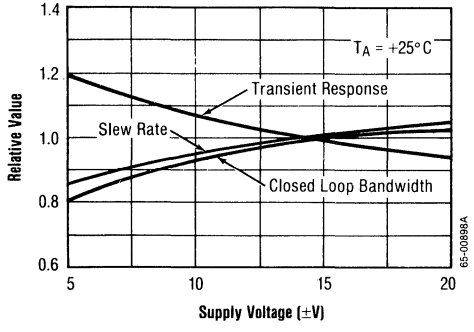
Parameters	Test Conditions	RM747 Min	RM747 Typ	RM747 Max	RC747 Min	RC747 Typ	RC747 Max	Units
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance (Diff. Mode)		0.3	2.0		0.3	2.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	80	90		70	90		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ	76	90		76	90		dB
Power Consumption			100	170		100	170	mW
Transient Response								
Rise Time	V_{IN} = 20 mV, R_L = 2 kΩ		0.3			0.3		µS
Overshoot	$C_L \leq 100$ pF		5.0			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5			0.5		V/µS
Channel Separation	f = 1 kHz		98			98		dB

Electrical Characteristics ($-55°C \le T_A \le +125°C$ for RM747; $0°C \le T_A \le +70°C$ for RC747)

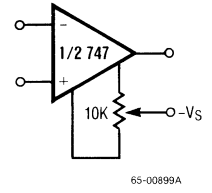
Parameters	Test Conditions	RM747 Min	RM747 Typ	RM747 Max	RC747 Min	RC747 Typ	RC747 Max	Units
Input Offset Voltage	$R_S \le 10\ k\Omega$			6.0			7.5	mV
Input Offset Current	$T_A = +125°C$, $T_A = +70°C$			200			300	nA
	$T_A = -55°C$ $T_A = 0°C$			500			300	nA
Input Bias Current	$T_A = +125°C$, $T_A = +70°C$			500			800	nA
	$T_A = -55°C$, $T_A = 0°C$			1500			800	nA
Large Signal Voltage Gain	$R_L \ge 2\ k\Omega$, $V_{OUT} = \pm 10V$	25			25			V/mV
Output Voltage Swing	$R_L \ge 10K$	±12			±10			V
	$R_L \ge 2\ k\Omega$	±10						V
Common Mode Rejection Ratio	$R_S \le 10\ k\Omega$	70			70			dB
Power Supply Rejection Ratio	$R_S = \le 10\ k\Omega$	76		150	76		150	dB
Power Consumption	$T_A = +125°C$			150			150	mW
	$T_A = -55°C$			200			200	mW
Input Voltage Range		±12			±12			V

Typical Performance Characteristics

Frequency Characteristics as a Function of Ambient Temperature

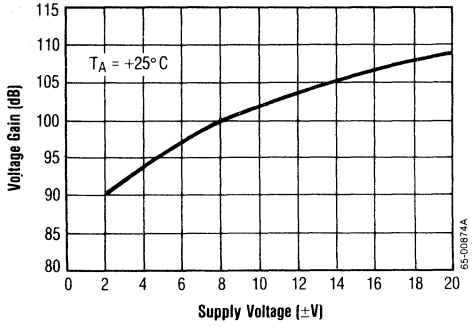


Voltage Offset Null Circuit

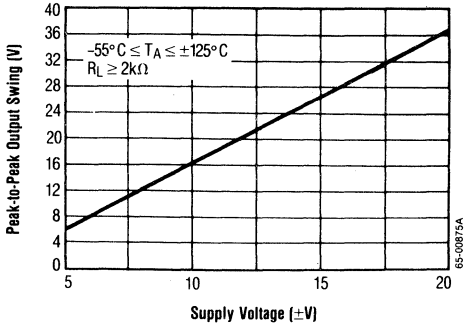


Typical Performance Characteristics (Continued)

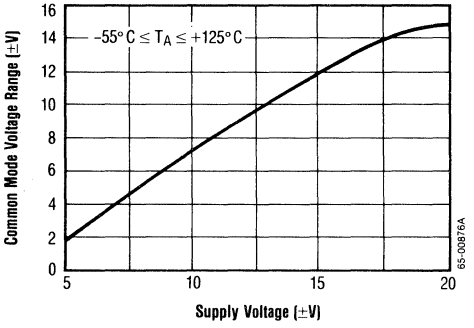
Open Loop Voltage Gain as a Function of Supply Voltage



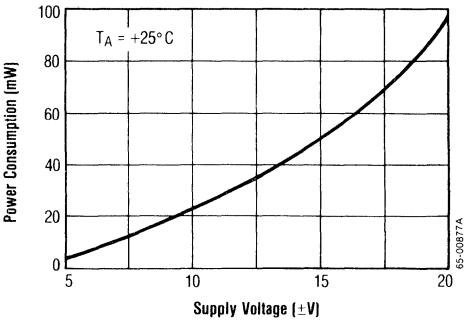
Output Voltage Swing as a Function of Supply Voltage



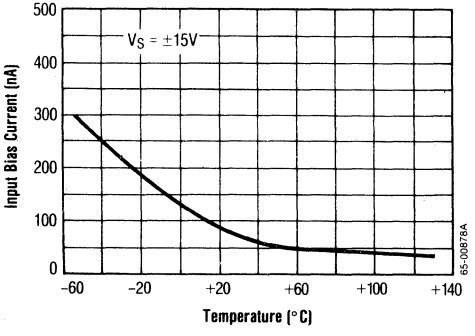
Input Common Mode Voltage Range as a Function of Supply Voltage



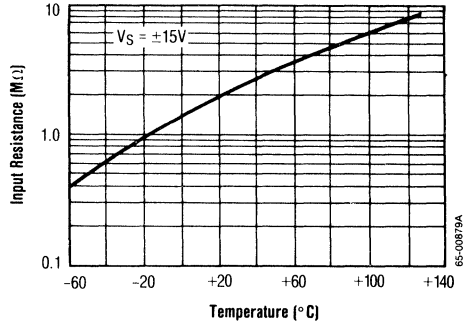
Power Consumption as a Function of Supply Voltage



Input Bias Current as a Function of Ambient Temperature

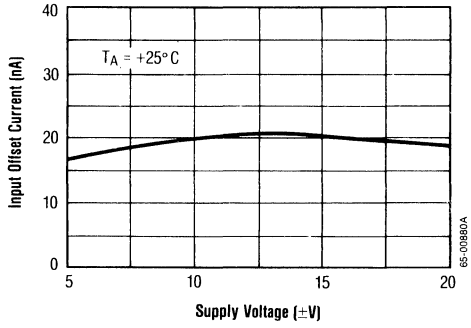


Input Resistance as a Function of Ambient Temperature

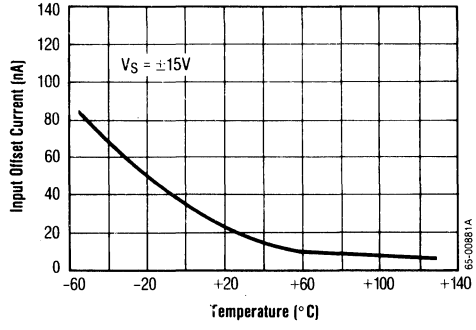


Typical Performance Characteristics (Continued)

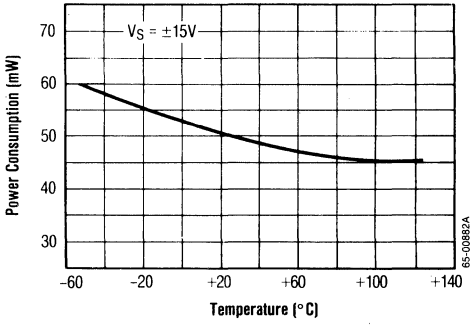
Input Offset Current as a Function of Supply Voltage



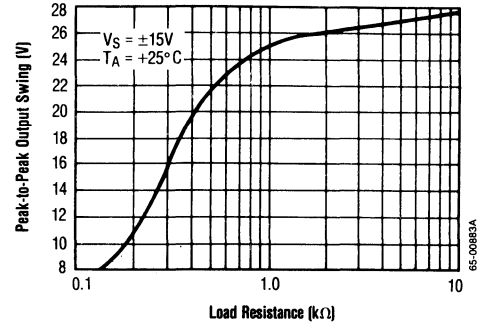
Input Offset Current as a Function of Ambient Temperature



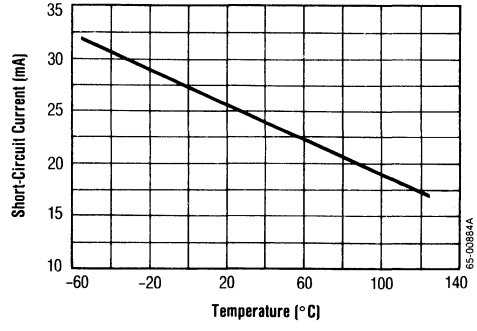
Power Consumption as a Function of Ambient Temperature



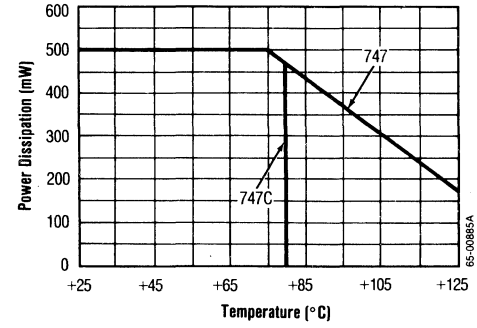
Output Voltage Swing as a Function of Load Resistance



Output Short Circuit Current as a Function of Ambient Temperature

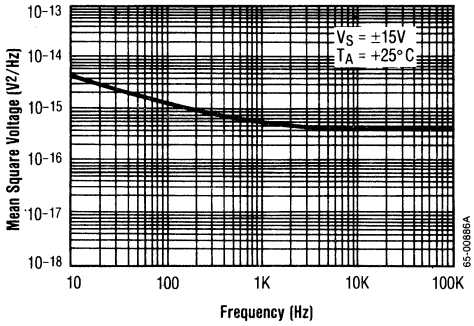


Absolute Maximum Power Dissipation as a Function of Ambient Temperature

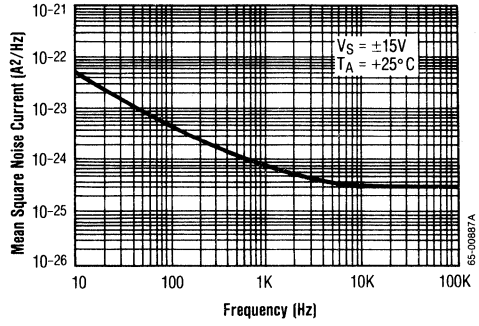


Typical Performance Characteristics (Continued)

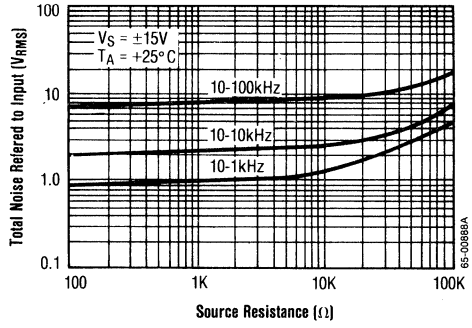
Input Noise Voltage as a Function of Frequency



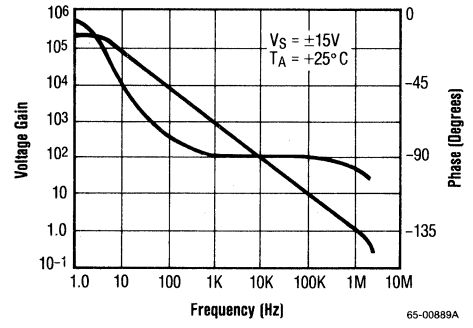
Input Noise Current as a Function of Frequency



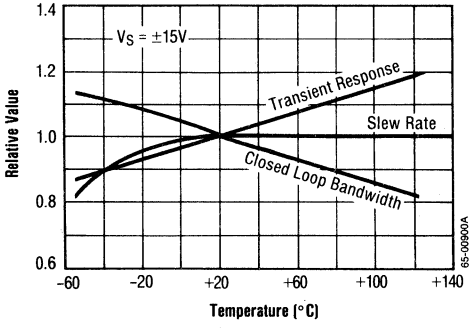
Broadband Noise for Various Bandwidths



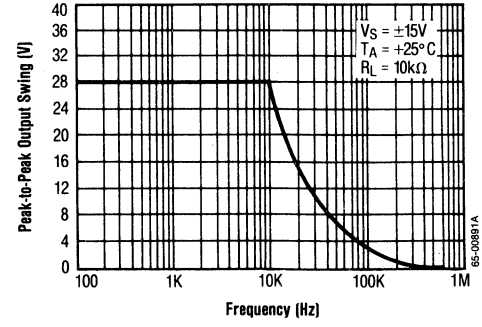
Open Loop Voltage Gain as a Function of Frequency



Frequency Characteristics as a Function of Ambient Temperature

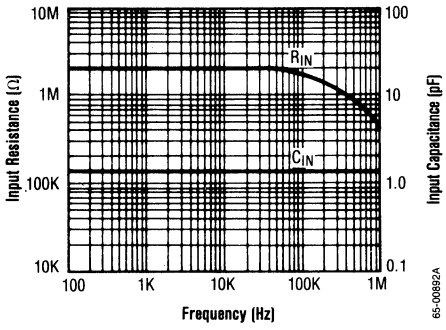


Output Voltage Swing as a Function of Frequency

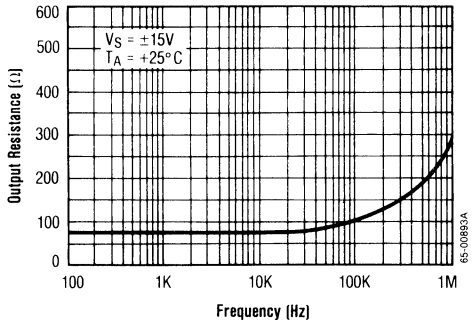


Typical Performance Characteristics (Continued)

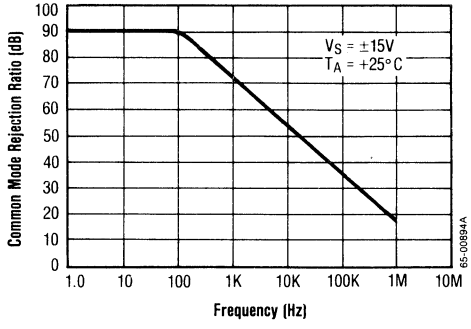
Input Resistance and Input Capacitance as a Function of Frequency



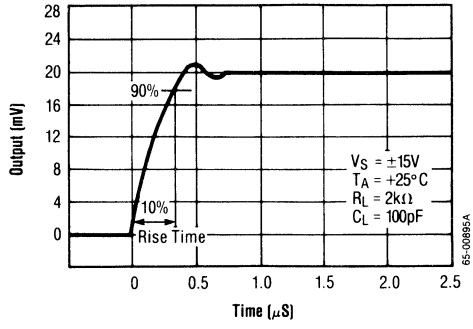
Output Resistance as a Function of Frequency



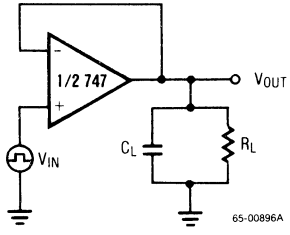
Common Mode Rejection Ratio as a Function of Frequency



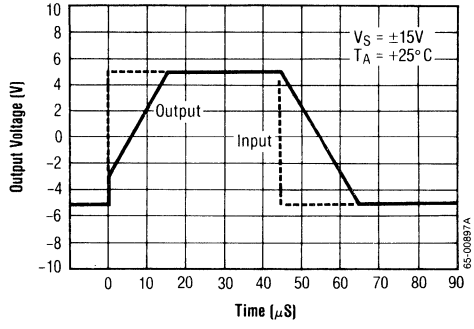
Transient Response



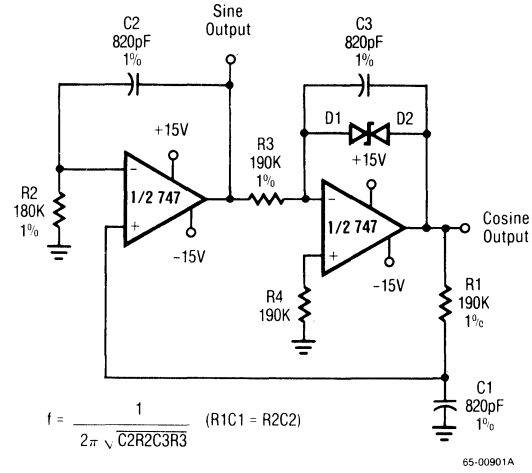
Transient Response Test Circuit



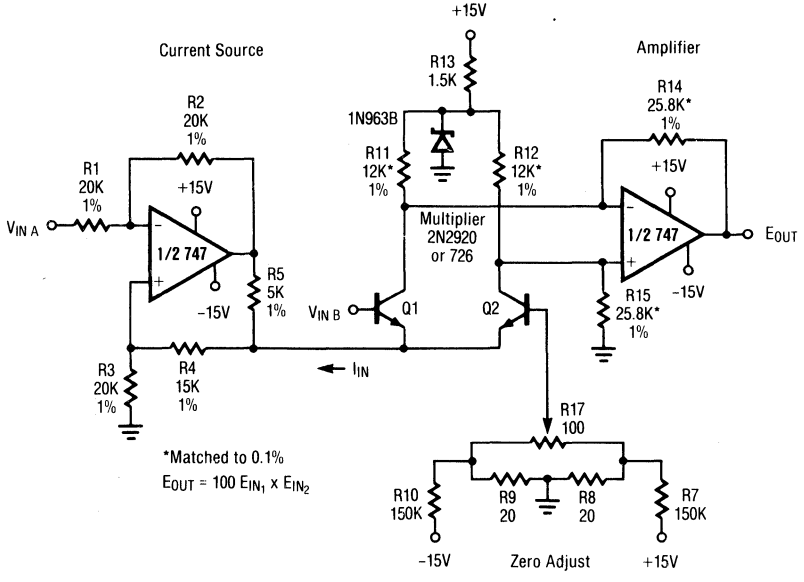
Voltage Follower Large Signal Pulse Response



Typical Applications

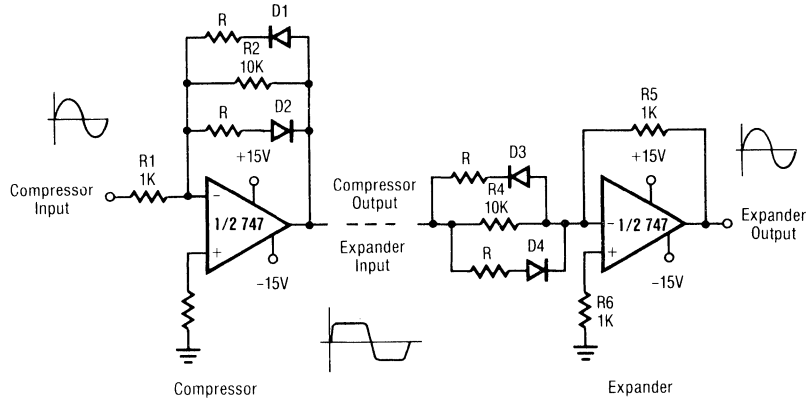


Quadrature Oscillator



Analog Multiplier

Typical Applications (Continued)

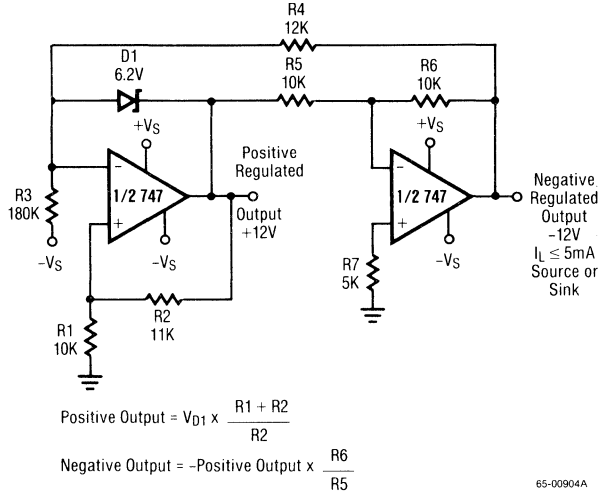


Maximum compression expansion ratio = R1/R (10KΩ > R ≥ 0)

65-00903A

Note: Diodes D1 through D4 are matched FD6666 or equivalent

Compressor/Expander Amplifiers



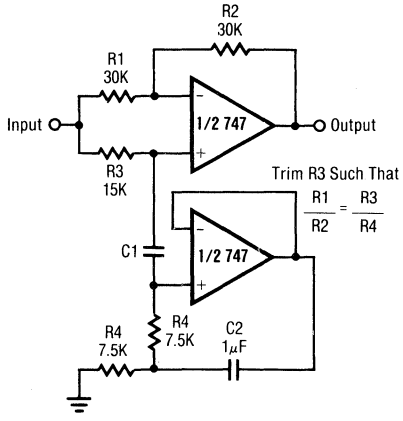
$$\text{Positive Output} = V_{D1} \times \frac{R1 + R2}{R2}$$

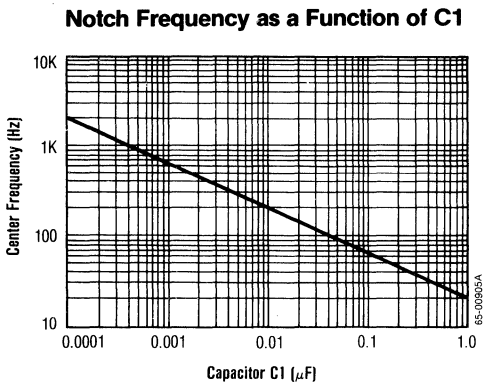
$$\text{Negative Output} = -\text{Positive Output} \times \frac{R6}{R5}$$

65-00904A

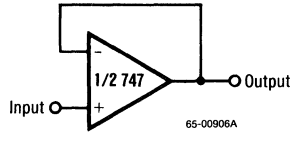
Tracking Positive and Negative Voltage References

Typical Applications (Continued)



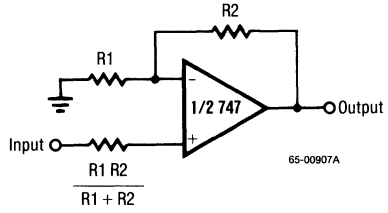


Notch Filter Using the 747 as a Gyrator



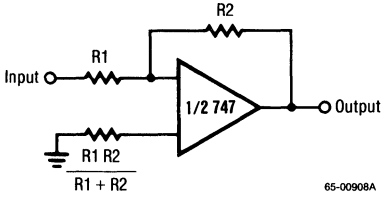
R_{IN} = 400MΩ
C_{IN} = 1pF
R_{OUT} << 1Ω
BW = 1MHz

Unity Gain Voltage Follower



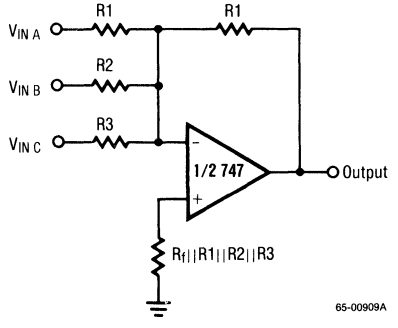
Gain	R1	R2	B.W.	R_{IN}
10	1kΩ	9kΩ	100kHz	400MΩ
100	100Ω	9.9kΩ	10kHz	280MΩ
1000	100Ω	99.9kΩ	1kHz	80MΩ

Non-Inverting Amplifier



Gain	R1	R2	B.W.	R_{IN}
1	10kΩ	10kΩ	1MHz	10kΩ
10	1kΩ	10kΩ	100kHz	1kΩ
100	1kΩ	100kΩ	10kHz	1kΩ
1000	100Ω	100kΩ	1kHz	100Ω

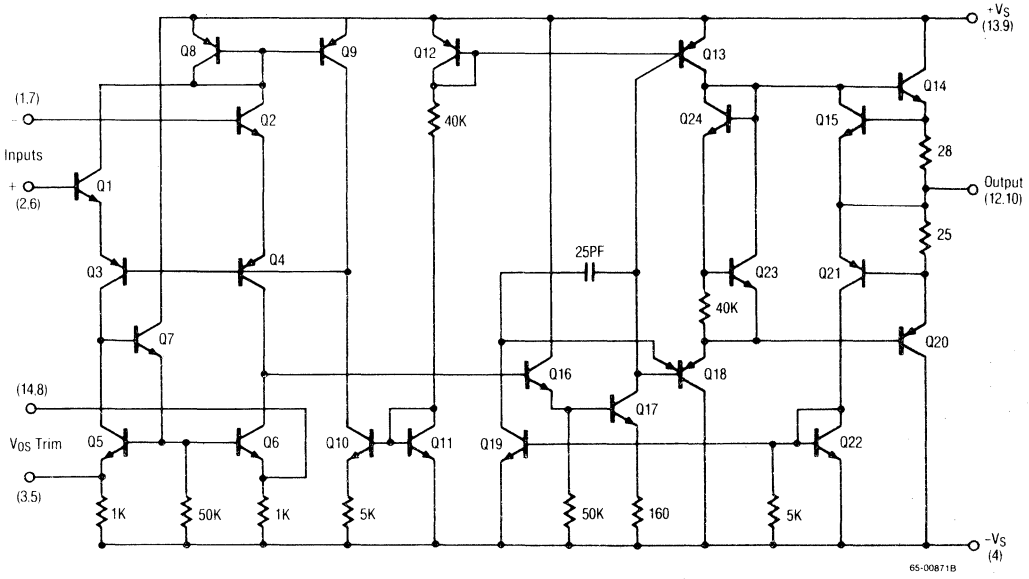
Inverting Amplifier



$$-V_O = V_{IN\,A}\left(\frac{R_f}{R1}\right) - V_{IN\,B}\left(\frac{R_f}{R2}\right) - V_{IN\,C}\left(\frac{R_f}{R3}\right)$$

Weighted Averaging Amplifier

Schematic Diagram (1/2 Shown)



RC3403A Ground Sensing Quad Operational Amplifier

Features

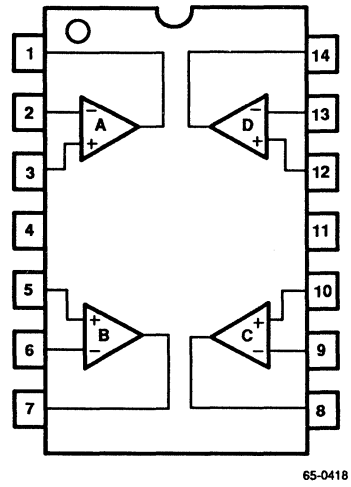
- Class AB output stage — no crossover distortion
- Output voltage swings to ground in single supply operation
- High slew rate — 1.2 V/μS
- Single or split supply operation
- Wide supply operation — +2.5V to +36V or ±1.25V to ±18V
- Pin compatible with LM324 and MC3403
- Low power consumption — 0.8 mA/amplifier
- Common mode range includes ground

Description

The RC3403A is a high performance ground sensing quad operational amplifiers featuring improved dc specifications equal to or better than the standard 741 type general purpose op amp. The ground sensing differential input stage of this op amp provides increased slew rate compared to 741 types.

Connection Information

14-Lead Dual In-Line Package
(Top View)



Pin	Function	Pin	Function
1	Output (A)	8	Output (C)
2	-Input (A)	9	-Input (C)
3	+Input (A)	10	+Input (C)
4	$+V_S$	11	$-V_S$ (Gnd)
5	+Input (B)	12	+Input (D)
6	-Input (B)	13	-Input (D)
7	Output (B)	14	Output (D)

Ordering Information

Part Number	Package	Operating Temperature Range
RC3403AN	N	0°C to +70°C

Notes:
N = 14-lead plastic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

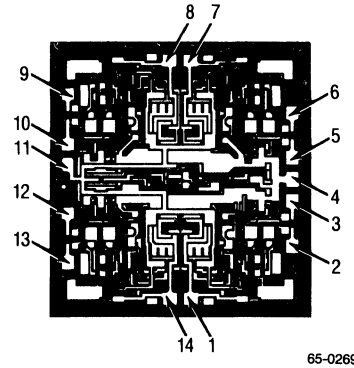
Absolute Maximum Ratings

Supply Voltage ..... +36V or ±18V
Input Voltage ..... -0.3 to +36V
Differential Input Voltage 36V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Thermal Characteristics

	14-Lead Plastic DIP
Max. Junction Temp.	125°C
Max. P_D T_A <50°C	468mW
Therm. Res θ_{JC}	—
Therm. Res. θ_{JA}	160°C/W
For T_A >50°C Derate at	6.25 mW/°C

Mask Pattern



Die Size: 81 x 85 mils
Min. Pad Dimensions: 4 x 4 mils

Low Voltage Electrical Characteristics ($+V_S$ = +5V, $-V_S$ = GND, and T_A = +25° C)

Parameters	Test Conditions	RC3403A			Units
		Min	Typ	Max	
Input Offset Voltage			2.0	10	mV
Input Bias Current			-150	-500	nA
Input Offset Current			30	50	nA
Supply Current	$R_L = \infty$ All Amplifiers		2.5	5.0	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	20	200		V/mV
Output Voltage Swing[1]	$R_L \geq 10k\Omega$	3.5			V_{p-p}
Channel Separation	1kHz ≤ F ≤ 200kHz (Input Referred)		120		dB
Power Supply Rejection Ratio		76			dB

Note: 1. Output will swing to ground.

Electrical Characteristics ($+V_S$ = ±15V over the specified operating temperature range)

Parameters	Test Conditions	RC3403A			Units
		Min	Typ	Max	
Input Offset Voltage				10	mV
Input Bias Current				-800	nA
Input Offset Current				200	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			V

Electrical Characteristics ($+V_S = \pm 15V$, $T_A = +25°C$)

Parameters	Test Conditions	RC3403A			Units
		Min	Typ	Max	
Input Offset Voltage			2.0	6.0*	mV
Input Bias Current			-150	-500	nA
Input Offset Current		±30	±50	nA	
Input Voltage Range		0		$+V_S$ -2	V
Supply Current	$R_L = \infty$ On All Op Amps		3.0	5.0*	mA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$	25*	100		V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±13	±14		V
Common Mode Rejection Ratio	DC	70	90		dB
Channel Separation	±1kHz to 20kHz		120		dB
Output Source Current	$V_{IN+} = 1V$, $V_{IN-} = 0V$	20	40		mA
Output Sink Current		10	20		mA
Unity Gain Bandwidth			1.0		MHz
Slew Rate	$A_V = 1$, $-10 \leq V_I < +10$		1.2*		V/μS
Distortion (Crossover)	f = 20kHz, $V_O = 10V_{p-p}$		1.0		%
Power Bandwidth	$V_O = 10V_{p-p}$		40		kHz
Power Supply Rejection Ratio		80	94		dB

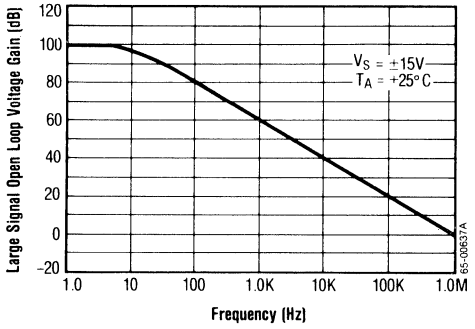
*Significantly improved performance.

Electrical Characteristics Comparison RC3403A, MC3403, LM324

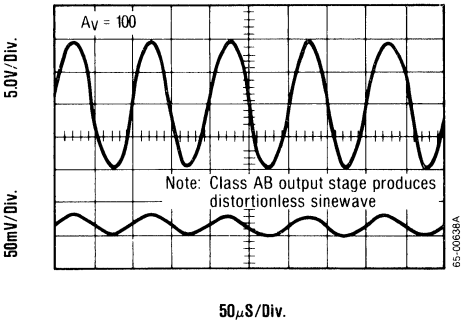
Max Ratings	RC3403A			MC3403			LM324			Units
Supply Voltage	+36 or ±18			+36 or ±18			+32 or ±16			V
Differential Input Voltage	36			36			32			V
Input Voltage	36			36			32			V
Electrical Characteristics	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Test Conditions		±15			±15			+5.0		V
Input Offset Voltage		2.0	6.0		2.0	8.0		2.0	7.0	mV
Input Offset Current		±30	±50		±30	±50		±5.0	±50	nA
Input Bias Current		150	500		200	500		45	500	nA
Input Voltage Range	0		$+V_S$ -2				0		$+V_S$ -1.5	V
Supply Current		3.0	5.0		2.8	7.0		0.8	2.0	mA
Large Signal Voltage Gain	25	100		20	200			100		V/mV
Output Voltage Swing	±13	±14		±1.0	±13				$+V_S$ -1.5	V
Common Mode Rejection Ratio	70	90		70	90			85		dB
Power Supply Rejection Ratio	80	94		76	90			100		dB
Unity Gain Bandwidth		1.0			1.0			1.0		MHz
Slew Rate		1.2			0.6			0.4		V/μS
Output Sink Current	10	20						20		mA
Output Source Current	20	40					20	40		mA
Channel Separation		120			120			120		dB
Distortion (Crossover)		1.0			1.0					%

Typical Performance Characteristics

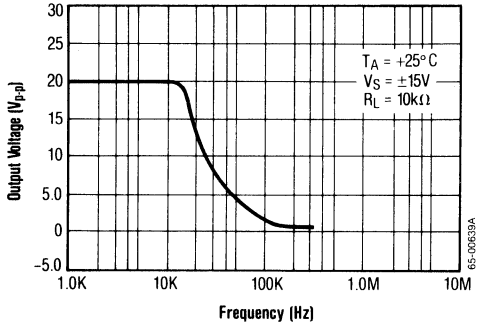
Large Signal Open Loop Voltage Gain as a Function of Frequency



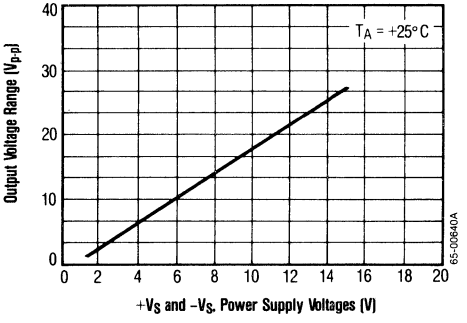
Sinewave Response



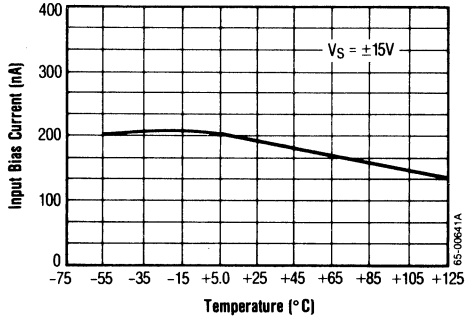
Output Voltage as a Function of Frequency



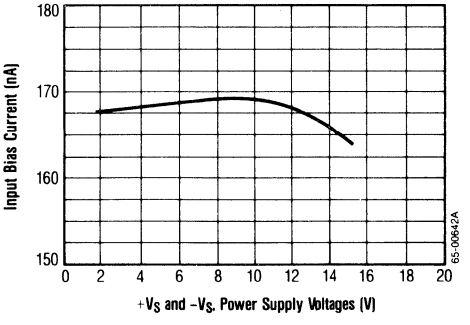
Output Swing as a Function of Supply Voltage



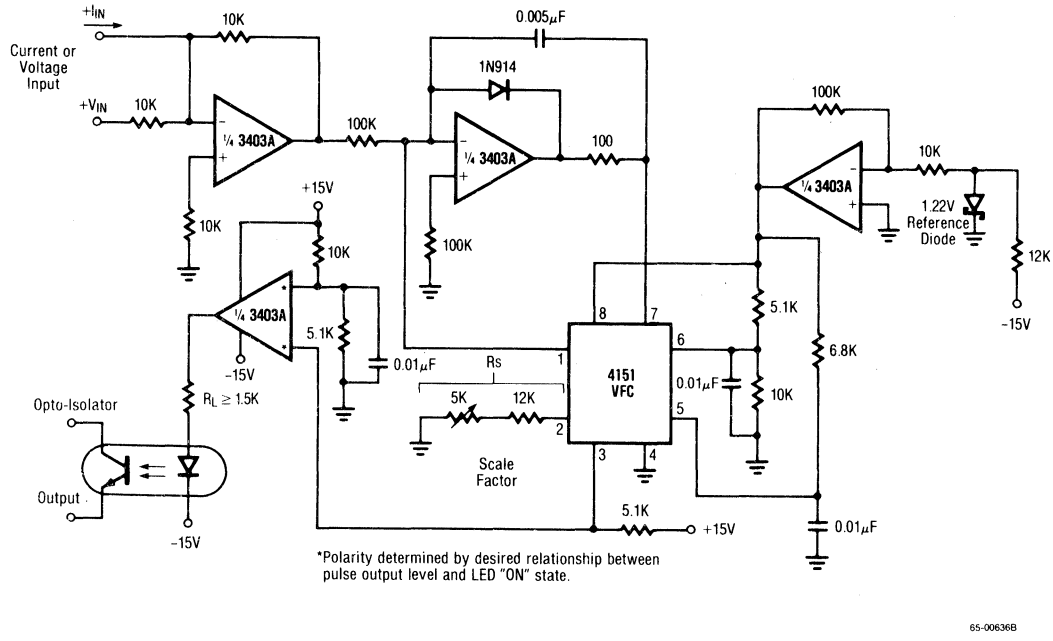
Input Bias Current as a Function of Temperature



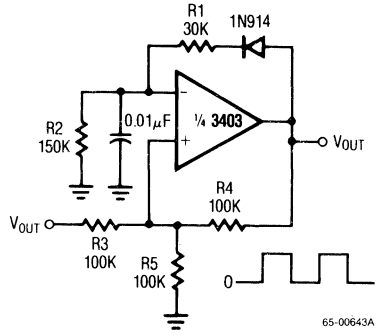
Input Bias Current as a Function of Supply Voltage



Typical Applications

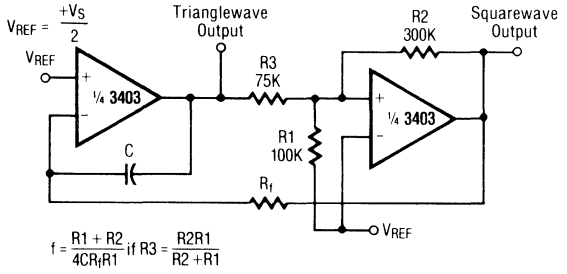


Precision Voltage-to-Frequency Converter With Isolated Output

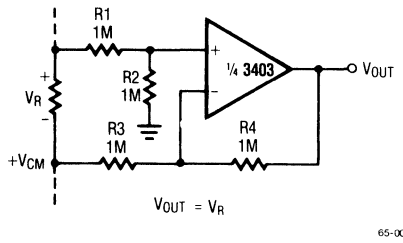


Pulse Generator

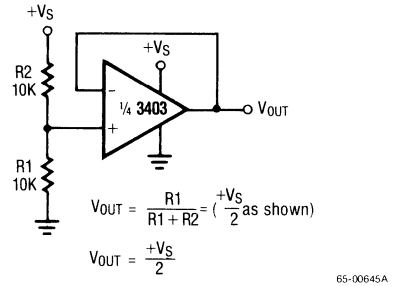
Typical Applications (Continued)



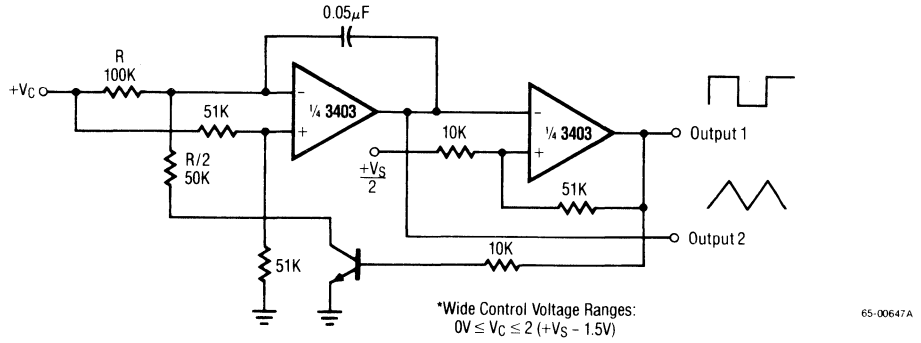
Function Generator



Ground Referencing a Differential Input Signal

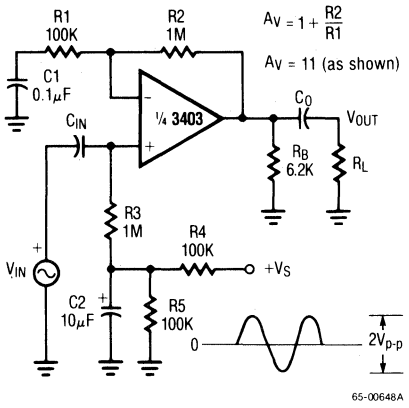


Voltage Reference

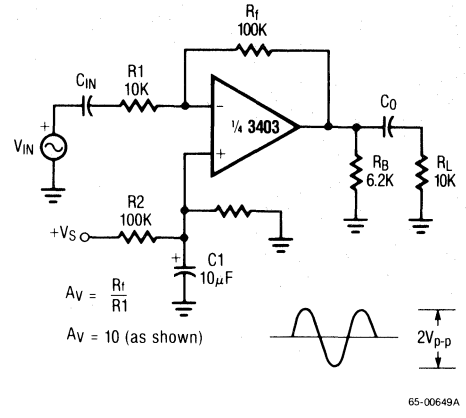


Voltage Controlled Oscillator

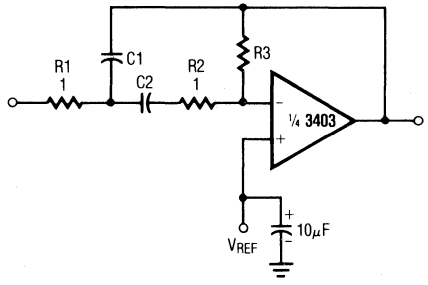
Typical Applications (Continued)



AC Coupled Non-Inverting Amplifier



AC Coupled Inverting Amplifier



fo ≙ Center Frequency
BW ≙ Bandwidth
R in kΩ
C in μF

$Q = \frac{fo}{BW} < 10$

$C1 = C2 = \frac{Q}{3}$

$R1 = R2 = 1$
$R3 = 9Q^2 - 1$ } Use scaling factors in these expressions.

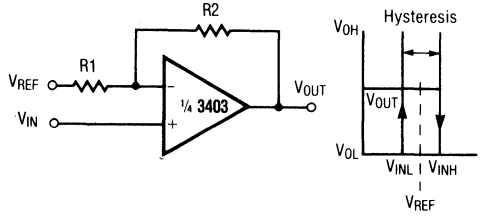
If source impedance is high or varies, filter may be preceeded with voltage follower buffer to stabilize filter parameters.

Design Example:
given: Q = 5, fo = 1kHz
Let R1 = R2 = 10kΩ
then R3 = 9(5)² - 10
R3 = 215kΩ

$C = \frac{5}{3} = 1.6nF$

65-00650A

Multiple Feedback Bandpass Filter



$V_{INL} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$

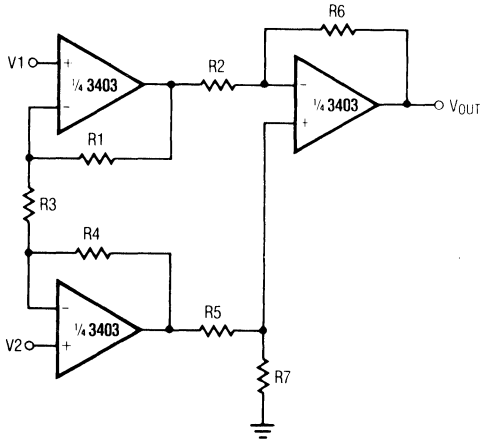
$V_{INH} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$

$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

65-00653A

Comparator With Hysteresis

Typical Applications (Continued)



$V_{OUT} = C(1 + a + b)(V2 - V1)$

$\frac{R2}{R5} = \frac{R6}{R7}$ for best CMRR

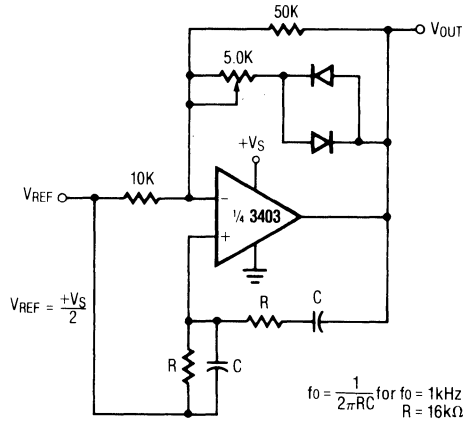
$R1 = R4$

$R2 = R5$

$Gain = \frac{R6}{R2}(1 + \frac{2R1}{R3}) = C(1 + a + b)$

65-00652A

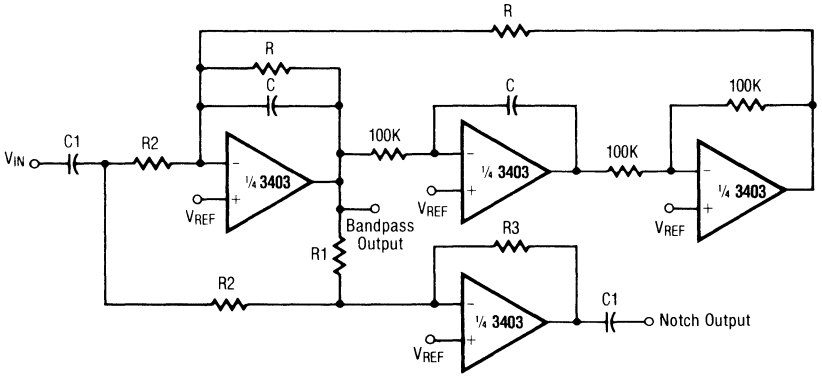
High Impedance Differential Amplifier



$f_o = \frac{1}{2\pi RC}$ for f_o = 1kHz
R = 16kΩ
C = 0.01μF

65-00651A

Wein Bridge Oscillator



$Q = \frac{f_o}{BW}$

Where
T_{BP} = Center Frequency Gain
T_N = Bandpass Notch Gain

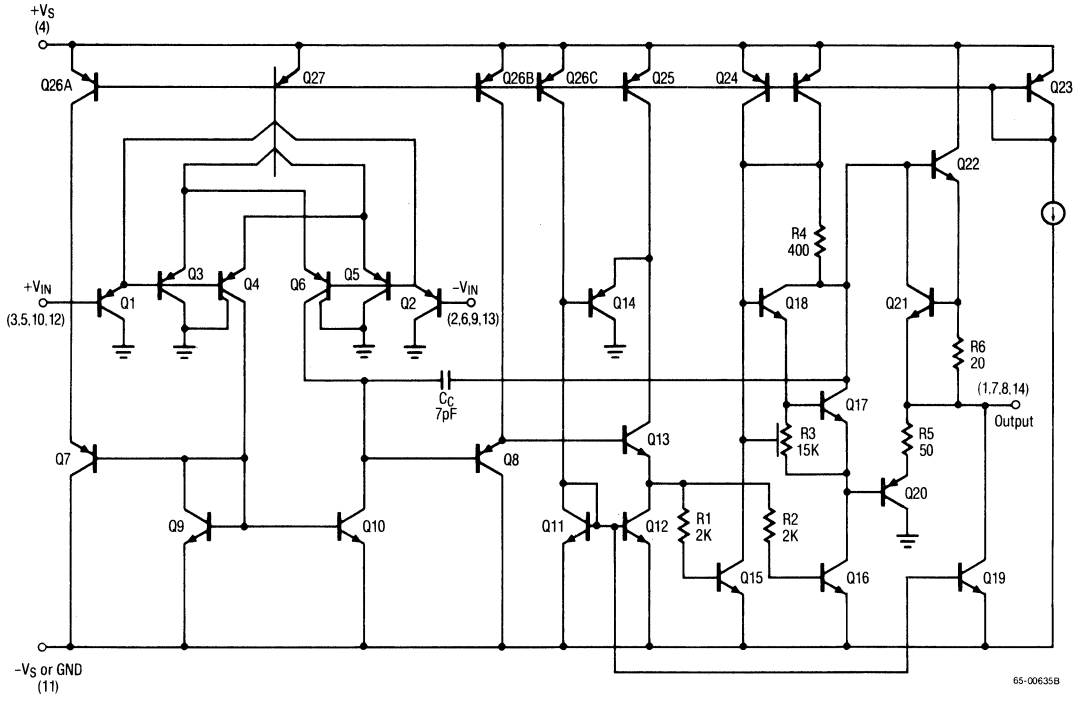
$f_o = \frac{1}{2\pi RC}$
$R1 = QR$
$R2 = \frac{R1}{T_{BP}}$
$R3 = T_N R2$
$C1 = 10C$

Example:
f_o = 1000Hz
BW = 100Hz
T_{BP} = 1
T_N = 1
R = 160kΩ
R1 = 1.6MΩ
R2 = 1.6MΩ
R3 = 1.6MΩ
C = 0.001μF

65-00654A

Bi-Quad Filter

Schematic Diagram (1/4 Shown)



RC4136 General Performance Quad 741 Operational Amplifier

Features

- Unity gain bandwidth — 3 MHz
- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Description

The 4136 is made up of four 741 type independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

This amplifier meets or exceeds all specifications for 741 type amplifiers. Excellent channel separation allows the use of the 4136 quad amplifier in all 741 operational amplifier applications providing the highest possible packaging density.

The specially designed low noise input transistors allow the 4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

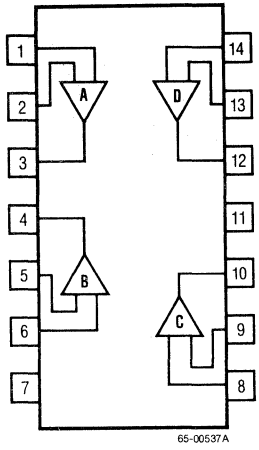
Ordering Information

Part Number	Package	Operating Temperature Range
RC4136N	N	0°C to +70°C
RC4136M	M	0°C to +70°C
RV4136N	N	-25° C to +85°C
RV4136D	D	-25° C to +85°C
RM4136D	D	-55°C to +125°C
RM4136D/883B*	D	-55°C to +125°C

Notes:
*/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

14-Lead
Dual In-Line Package
(Top View)



Pin	Function
1	-Input (A)
2	+Input (A)
3	Output (A)
4	Output (B)
5	+Input (B)
6	-Input (B)
7	$-V_S$
8	-Input (C)
9	+Input (C)
10	Output (C)
11	$+V_S$
12	Output (D)
13	+Input (D)
14	-Input (D)

Absolute Maximum Ratings

Supply Voltage
- RM4136 ..... ±22V
- RC4136, RV4136 ..... ±18V

Input Voltage* ..... ±30V
Differential Input Voltage 30V
Output Short Circuit Duration** ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- RM4136 ..... -55°C to +125°C
- RV4136 ..... -25°C to +85°C
- RC4136 ..... 0°C to +70°C

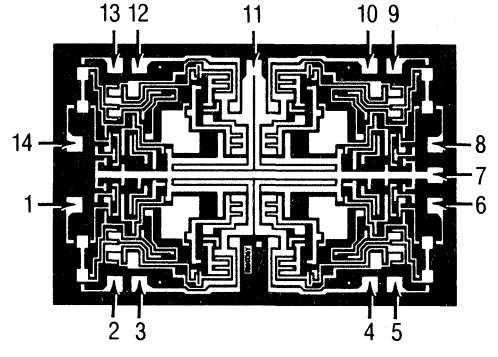
Lead Soldering Temperature
- (DIP, 60 sec) ..... +300°C
- (SO-14, 10 sec) ..... +260°C

*For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
**Short circuit may be to ground, typically 45 mA.

Thermal Characteristics

	14-Lead Small Outline	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	125°C	175°C
Max. P_D T_A <50°C	300 mW	468 mW	1042 mW
Therm. Res θ_{JC}	—	—	50°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW per °C	6.25 mW per °C	8.33 mW/ per °C

Mask Pattern



Die Size: 99 x 64 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = ±15V and T_A = +25°C, unless otherwise noted)

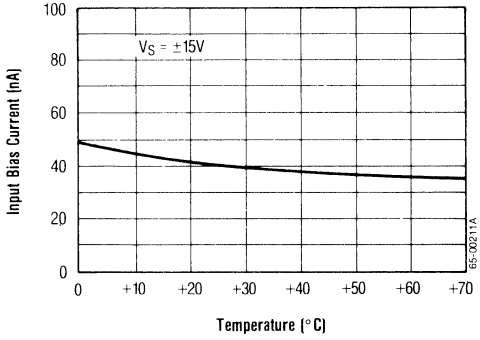
Parameters	Test Conditions	RM4136			RC/RV4136			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	5.0		0.5	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		
Input Voltage Range		±12	±14		±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	R_L = ∞, All Outputs		210	340		210	340	mW
Transient Response Rise Time	V_{IN} = 20mV, R_L = 2kΩ		0.13			0.13		μS
Overshoot	$C_L \leq 100pF$		5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate	$R_L \geq 2k\Omega$		1.5			1.0		V/μS
Channel Separation	f = 1.0kHz, R_S = 1kΩ		90			90		dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C for RM4136; 0°C ≤ T_A ≤ +70°C for RC4136; -25°C ≤ T_A ≤ +85°C for RV4136, V_S = ±15V								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current RM/RC4136				500			300	nA
RV4136							500	
Input Bias Current RM/RC4136				1500			800	nA
RV4136							1500	
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption			240	400		240	400	mW

Electrical Characteristics Comparison (V_S = ±15V and T_A +25°C unless otherwise noted)

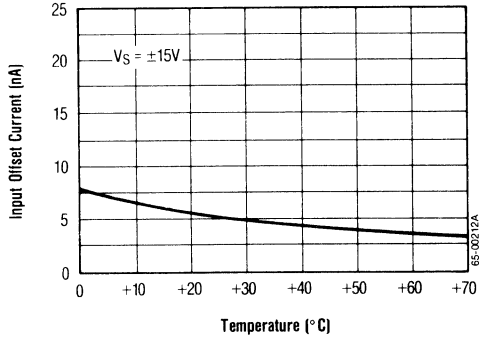
Parameter	RC4136 (Typ)	RC741 (Typ)	LM324 (Typ)	Units
Input Offset Voltage	0.5	2.0	2.0	mV
Input Offset Current	5.0	10	5.0	nA
Input Bias Current	40	80	55	nA
Input Resistance	5.0	2.0		MΩ
Large Signal Voltage Gain (R_L = 2kΩ)	300	200	100	V/mV
Output Voltage Swing (R_L = 2kΩ)	±13V	±13V	$\lvert+V_S - 1.2V\rvert$ to $-V_S$	V
Input Voltage Range	±14V	±13V	$\lvert+V_S - 1.5V\rvert$ to $-V_S$	V
Common Mode Rejection Ratio	100	90	85	dB
Power Supply Rejection Ratio	100	90	100	dB
Transient Response Rise Time	0.13	0.3		μS
Overshoot	5.0	5.0		%
Unity Gain Bandwidth	3.0	0.8	0.8	MHz
Slew Rate	1.0	0.5	0.5	V/μS
Input Noise Voltage Density (f = 1kHz)	10	22.5		$nV/\sqrt{Hz}$
Short Circuit Current	±45	±25		mA

Typical Performance Characteristics

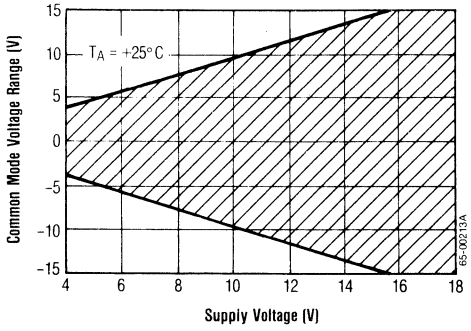
Input Bias Current as a Function of Ambient Temperature



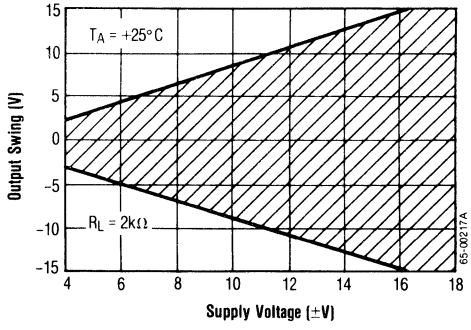
Input Offset Current as a Function of Ambient Temperature



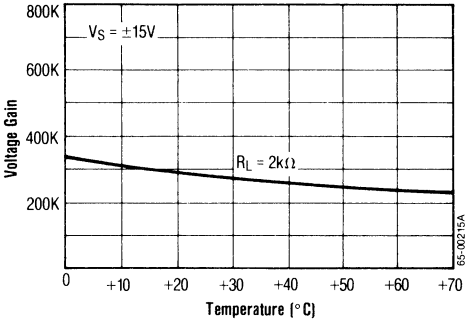
Common Mode Range as a Function of Supply Voltage



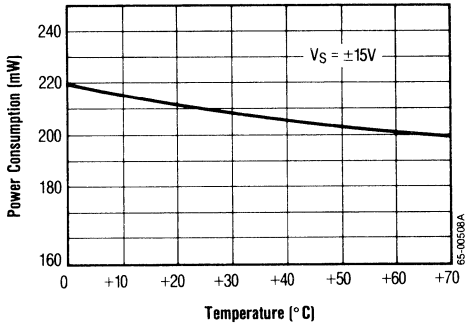
Typical Output Voltage as a Function of Supply Voltage



Open Loop Gain as a Function of Temperature

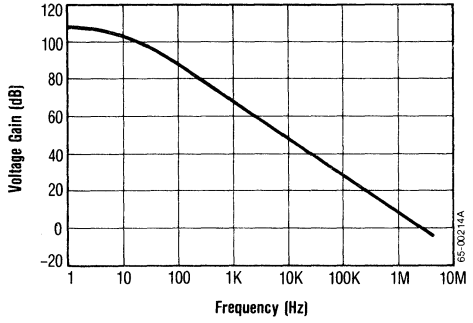


Power Consumption as a Function of Ambient Temperature

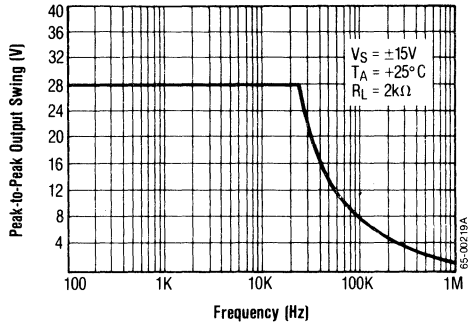


Typical Performance Characteristics (Continued)

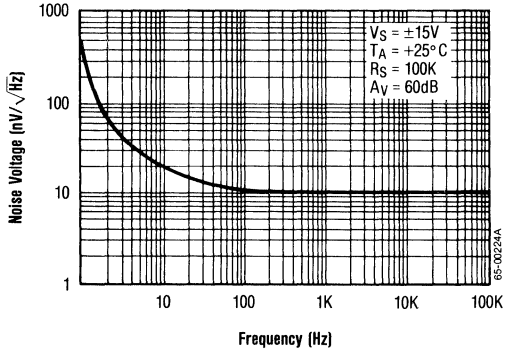
Open Loop Voltage Gain as a Function of Frequency



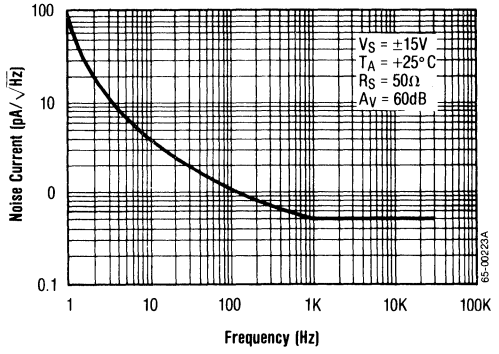
Output Voltage Swing as a Function of Frequency



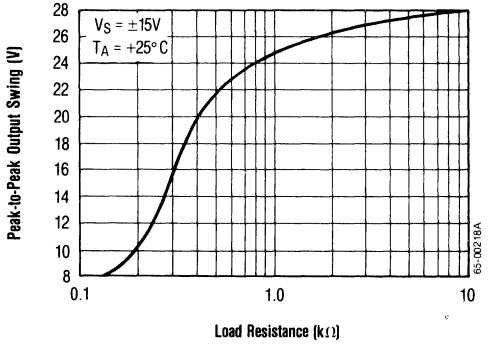
Input Noise Voltage as a Function of Frequency



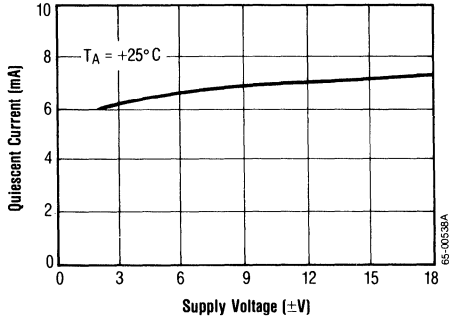
Input Noise Current as a Function of Frequency



Output Voltage Swing as a Function of Load Resistance

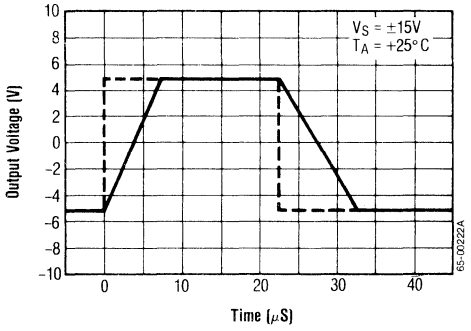


Quiescent Current as a Function of Supply Voltage

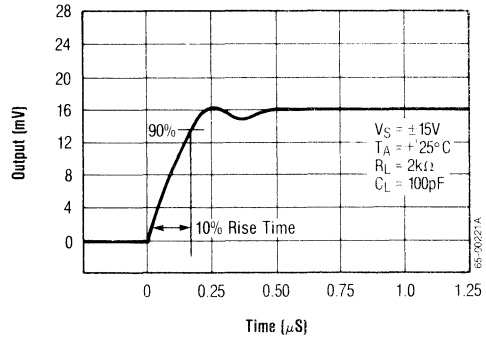


Typical Performance Characteristics (Continued)

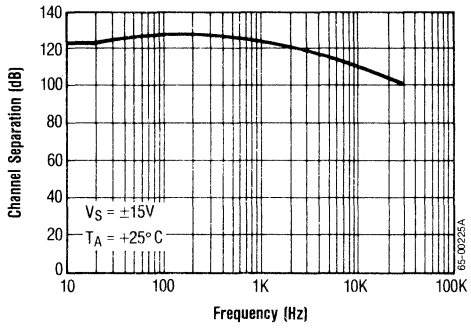
Voltage Follower Large Signal Pulse Response



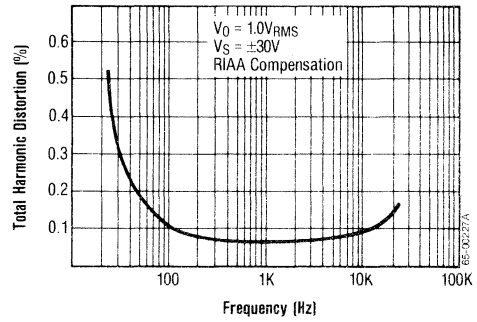
Transient Response



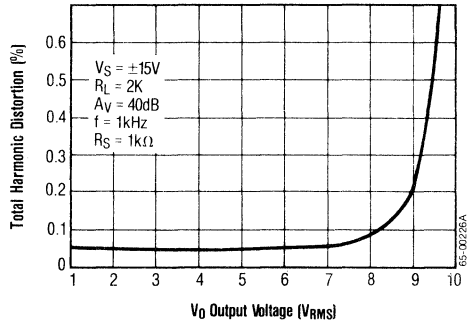
Channel Separation



Distortion vs. Frequency



Total Harmonic Distortion vs. Output Voltage

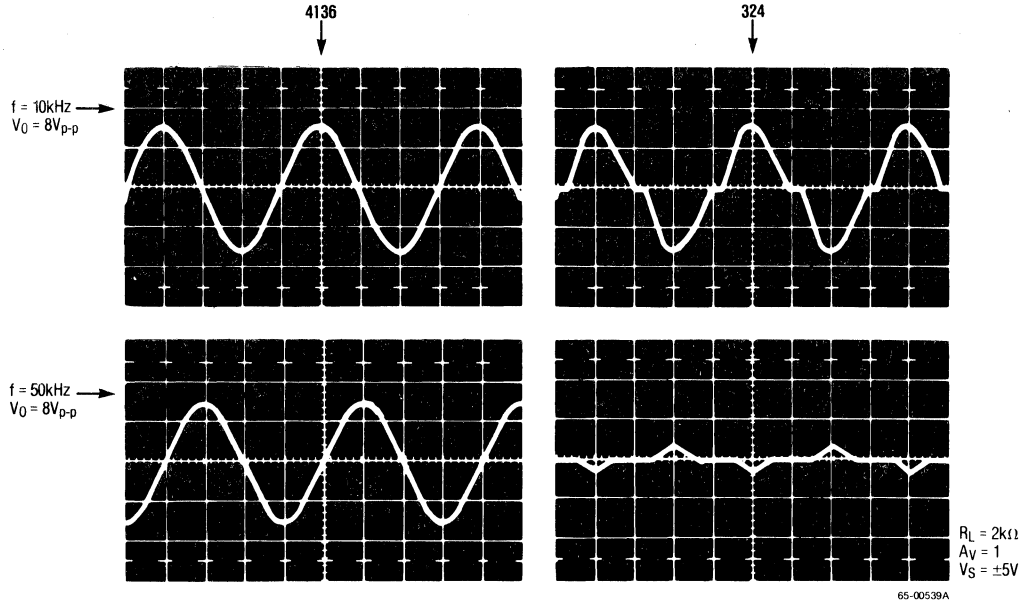


4136 Versus 741

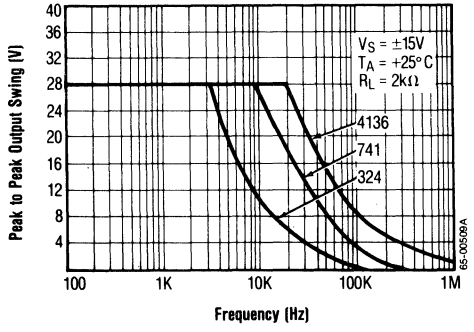
Although the 324 is an excellent device for single-supply applications where ground sensing is important, it is a poor substitute for four 741s in split supply circuits.

The simplified input circuit of the 4136 exhibits much lower noise than that of the 324 and exhibits no crossover distortion as compared with the 324 (see illustration). The 324 shows serious crossover distortion and pulse delay in attempting to handle a large signal input pulse.

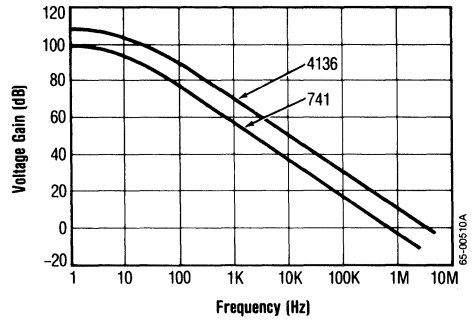
Comparative Crossover Distortion



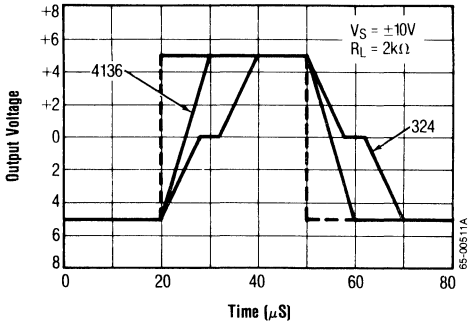
Output Voltage Swing as a Function of Frequency



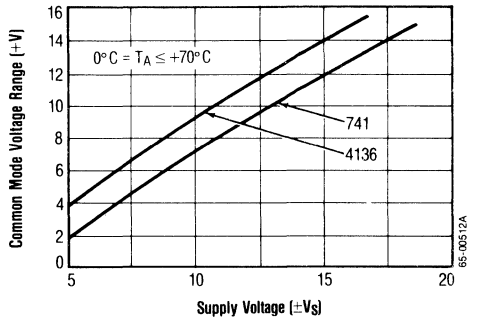
Open Loop Voltage Gain as a Function of Frequency



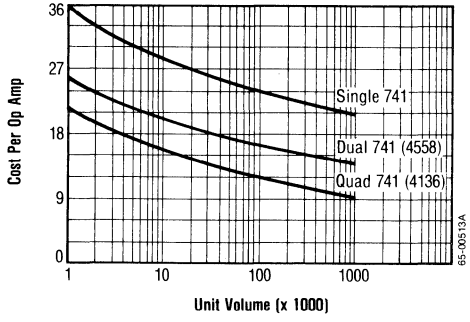
Voltage Follower Large Signal Pulse Response



Input Common Mode Voltage Range as a Function of Supply Voltage

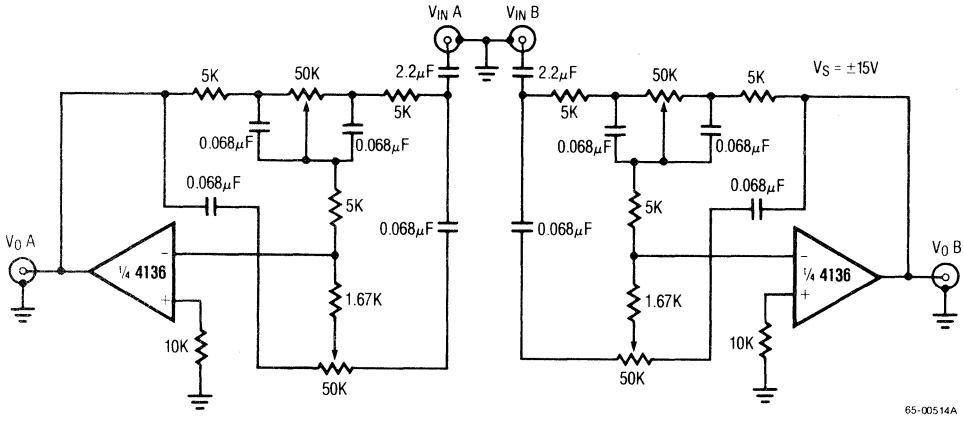


Unit Cost Comparisons

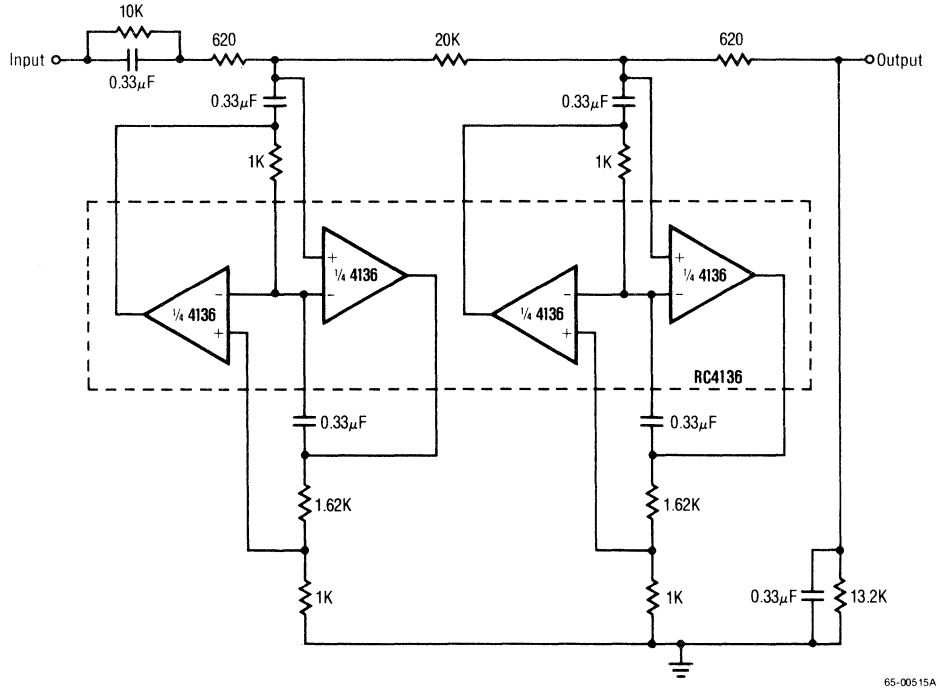


Typical Applications

Stereo Tone Control

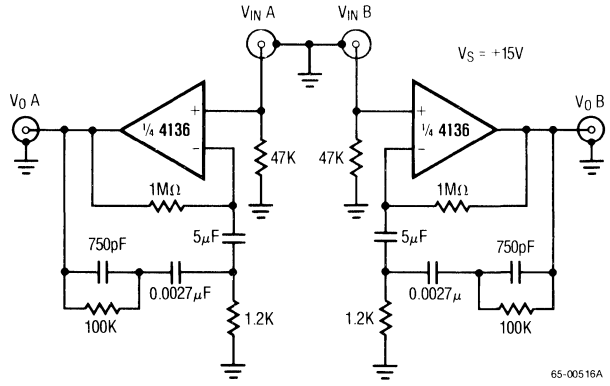


400 Hz Lowpass Butterworth Active Filter

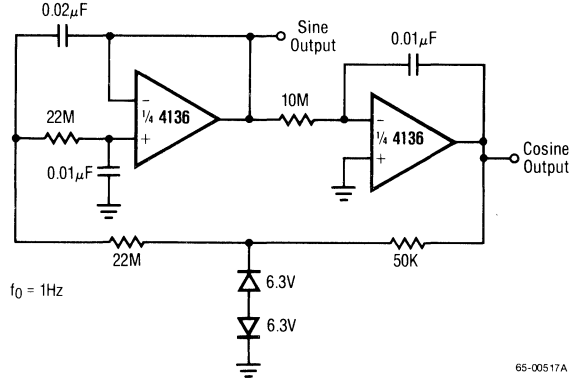


Typical Applications (Continued)

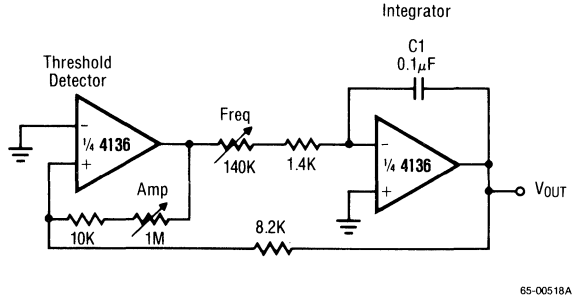
RIAA Preamplifier



Low Frequency Sine Wave Generator With Quadrature Output

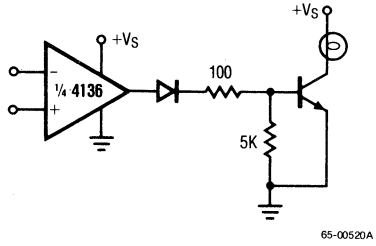


Triangular-Wave Generator

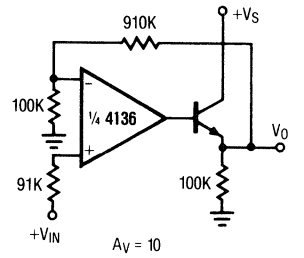


Typical Applications (Continued)

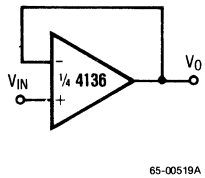
Lamp Driver



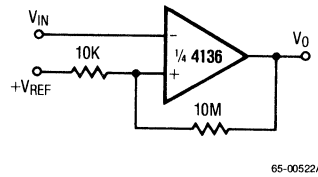
Power Amplifier



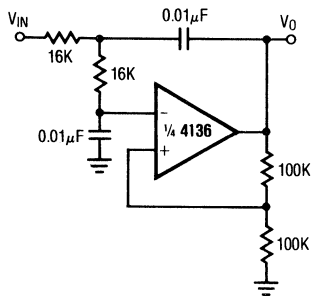
Voltage Follower



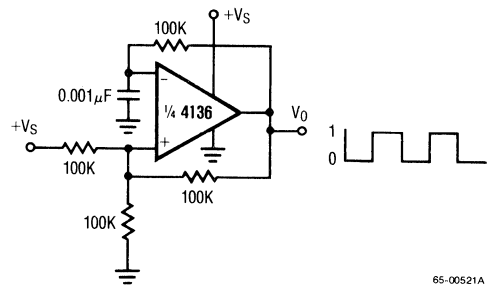
Comparator With Hysteresis



DC Coupled 1 kHz Lowpass Active Filter

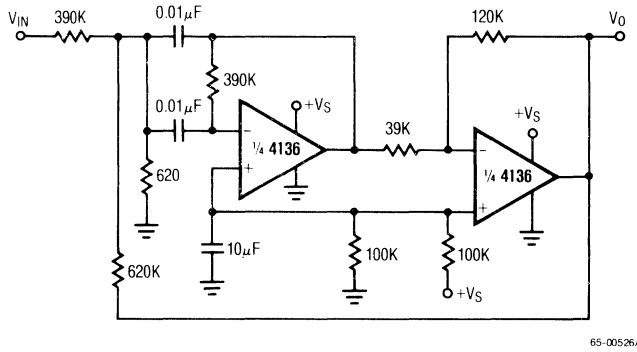


Squarewave Oscillator



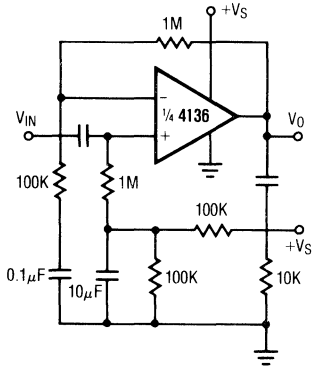
Typical Applications (Continued)

1 kHz Bandpass Active Filter



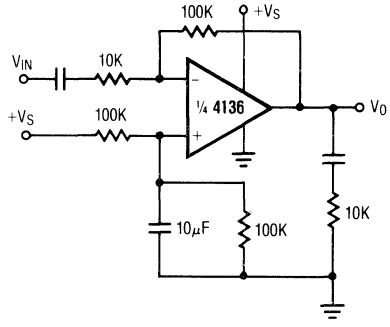
65-00526A

AC Coupled Non-Inverting Amplifier



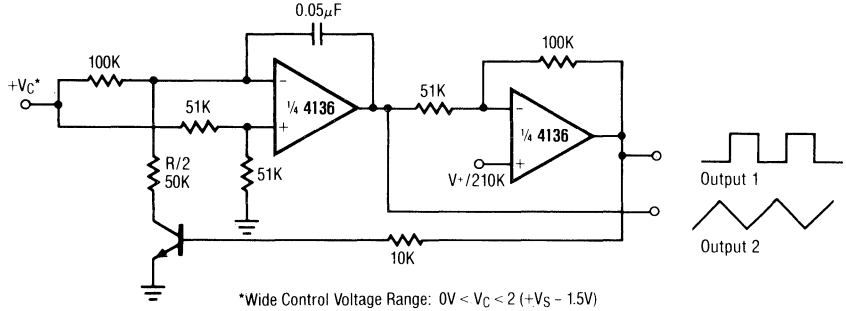
65-00524A

AC Coupled Inverting Amplifier



65-00525A

Voltage Controlled Oscillator (VCO)

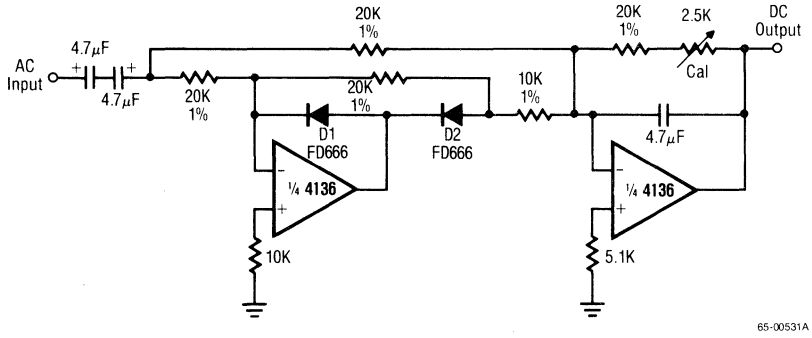


*Wide Control Voltage Range: $0V < V_C < 2 (+V_S - 1.5V)$

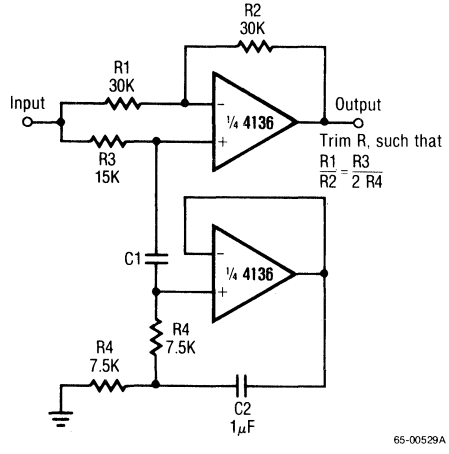
65-00528A

Typical Applications (Continued)

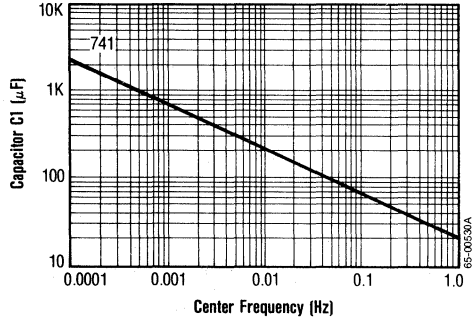
Full-Wave Rectifier and Averaging Filter



Notch Filter Using the 4136 as a Gyrator

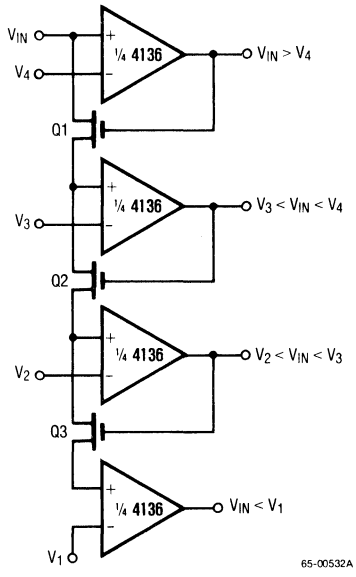


Notch Frequency as a Function of C1

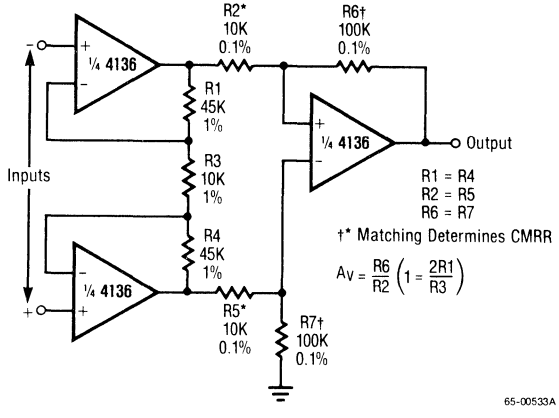


Typical Applications (Continued)

Multiple Aperture Window Discriminator

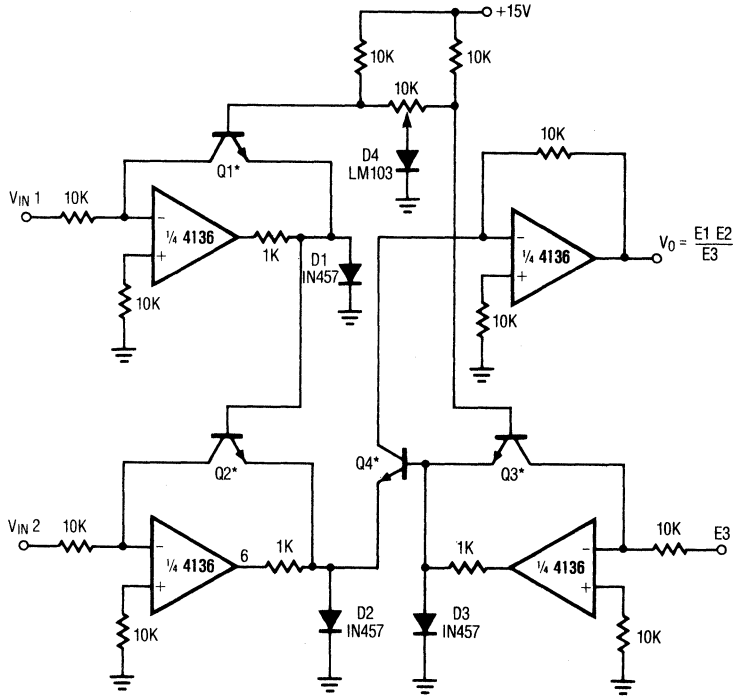


Differential Input Instrumentation Amplifier With High Common Mode Rejection



Typical Applications (Continued)

Analog Multiplier/Divider

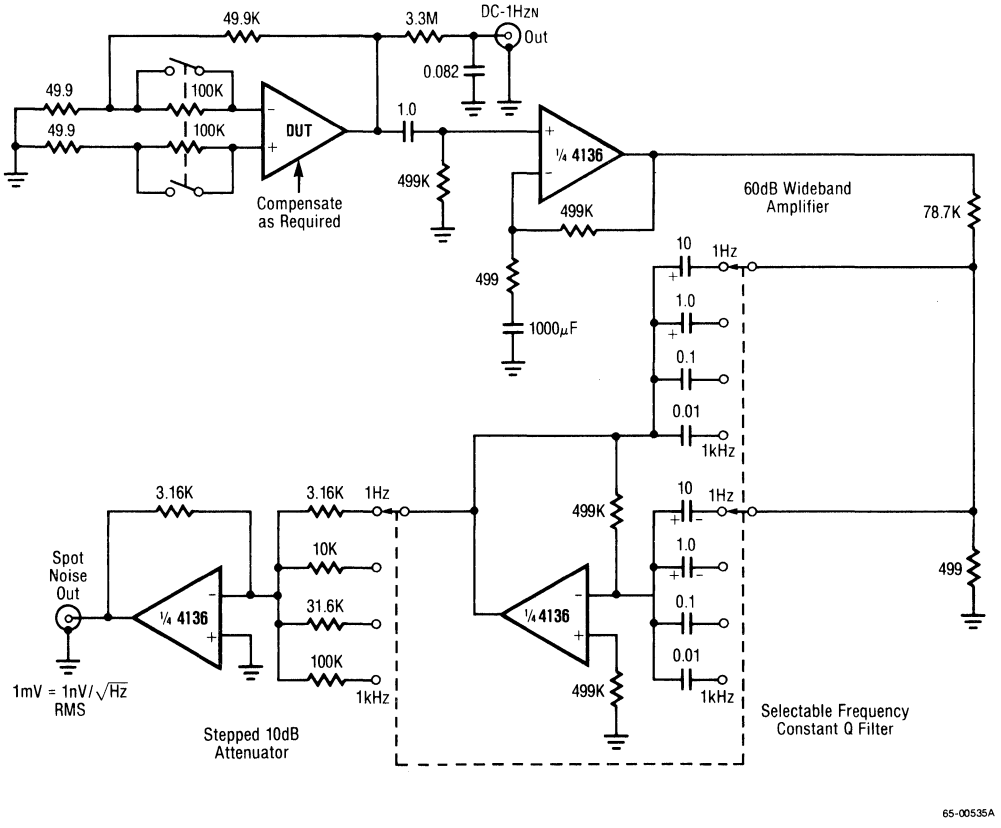


*Matched Transistors

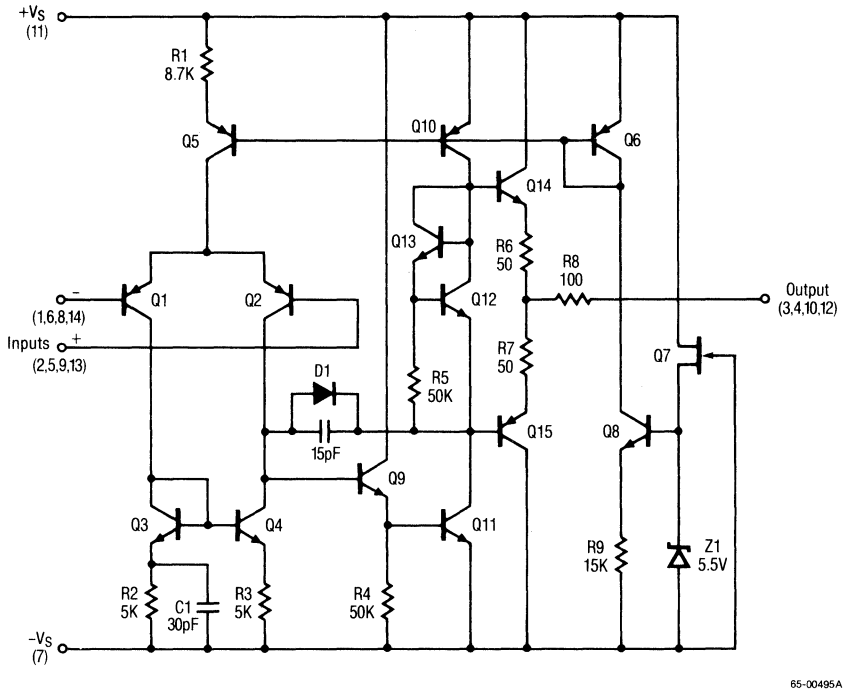
65-00534A

Typical Applications (Continued)

Spot Noise Measurement Test Circuit



Schematic Diagram



RC4156/RC4157 High Performance Quad Operational Amplifier

Features

- Unity gain bandwidth — 2.8 MHz minimum (4156); 15 MHz minimum (4157)
- High slew rate — 1.3 V/μS minimum (4156); 6.5V/μS (4157)
- Low noise voltage — 1.4 μV typical; 2.0 μV_{RMS} guaranteed
- Indefinite short circuit protection
- No crossover distortion

Description

The 4156 and 4157 are monolithic integrated circuits, consisting of four independent high performance operational amplifiers constructed with an advanced epitaxial process.

These amplifiers feature guaranteed ac performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and guaranteed low noise, making this device the optimum choice for audio, active filter and instrumentation applications. The 4157 is a decompensated version of the 4156 and is ac stable in gain configurations of -5 or greater.

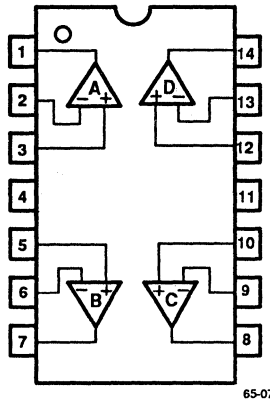
Ordering Information

Part Number	Package	Operating Temperature Range
RC4156N	N	0°C to +70°C
RC4156M	M	0°C to +70°C
RC4157N	N	0°C to +70°C
RM4156D	D	-55°C to +125°C
RM4156D/883B*	D	-55°C to +125°C
RM4157D	D	-55°C to +125°C
RM4157D/883B*	D	-55°C to +125°C

Notes:
*/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

14-Lead Dual In-Line Package
(Top View)



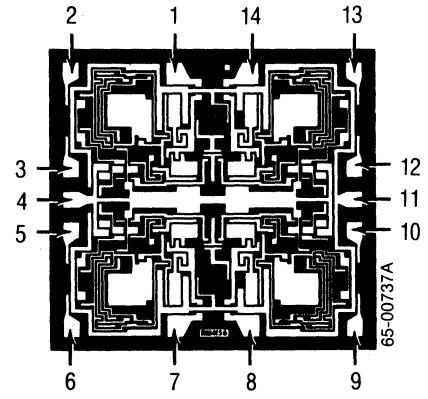
Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$+V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	Output (C)
9	-Input (C)
10	+Input (C)
11	$-V_S$
12	+Input (D)
13	-Input (D)
14	Output (D)

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Voltage 30V
Input Voltage* ..... ±15V
Output Short Circuit Duration ** ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4156/4157 ..... -55°C to +125°C
RC4156/4157 ..... 0°C to +70°C
Lead Soldering Temperature
(DIP; 60 sec) ..... +300°C
(SO-14; 10 sec) ..... +260°C

*For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
**Short circuit to ground on one amplifier only.

Mask Pattern



Die Size: 80 x 84 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	14-Lead Plastic SO-14	14 Lead Plastic DIP	14 Lead Ceramic DIP
Max. Junction Temp.	125°C	125°C	175°C
Max. P_D T_A <50°C	300mW	468mW	1042mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics

(-55°C ≤ T_A ≤ +125°C for RM4156, 0°C ≤ T_A ≤ +70°C for RC4156, V_S = ±15V)

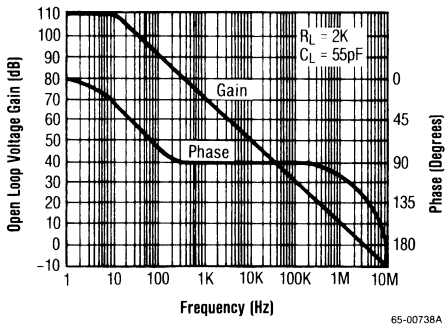
Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 10 kΩ			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				320			400	nA
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±10			±10			V
Supply Current			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		µV/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

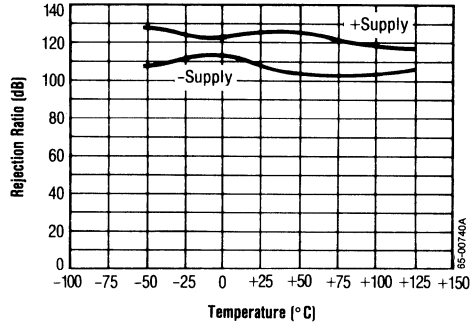
Parameters	Test Conditions	RM4156/4157			RC4156/4157			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ $R_L \geq 2$ kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ	80			80			dB
Supply Current (All Amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response (4156)								
Rise Time			60			60		nS
Overshoot			25			25		%
Slew Rate		1.3	1.6		1.3	1.6		V/μS
Unity Gain Bandwidth (4156)		2.8	3.5		2.8	3.5		MHz
Phase Margin (4156)	R_L = 2 kΩ, C_L = 50 pF		50			50		%
Transient Response (4157)	A_V = -5							
Rise Time			50			50		nS
Overshoot			25			25		%
Slew Rate		6.5	8.0		6.5	8.0		V/μS
Unity Gain Bandwidth (4157)	A_V = -5	15	19		15	19		MHz
Phase Margin (4157)	A_V = -5, R_L = 2 kΩ, C_L = 50 pF		50			50		%
Power Bandwidth	$V_O = 20V_{P-P}$	20	25		20	25		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	f = 20 Hz to 20 kHz		15			15		pA_{RMS}
Channel Separation			108			108		dB

Typical Performance Characteristics

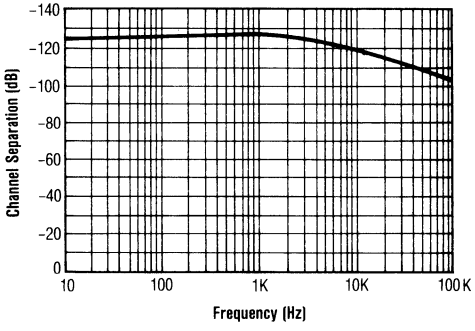
Open Loop Frequency Response

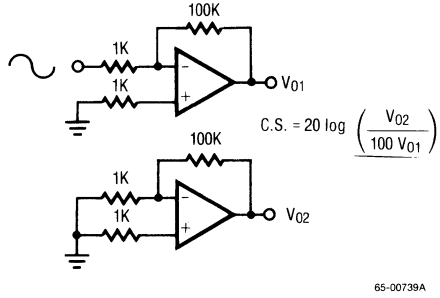


Power Supply Rejection Ratio vs. Temperature

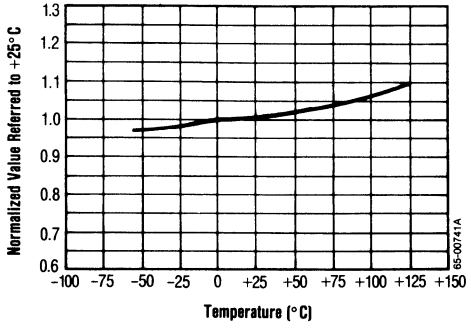


Channel Separation vs. Frequency

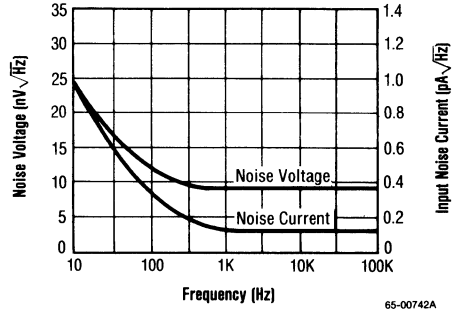




Transient Response vs. Temperature

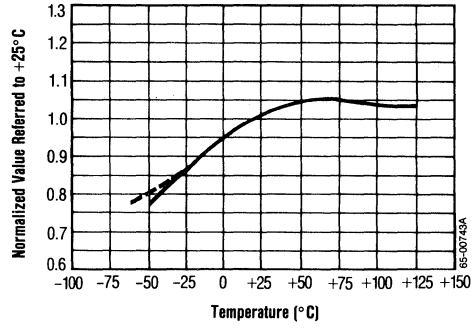


Input Noise vs. Frequency

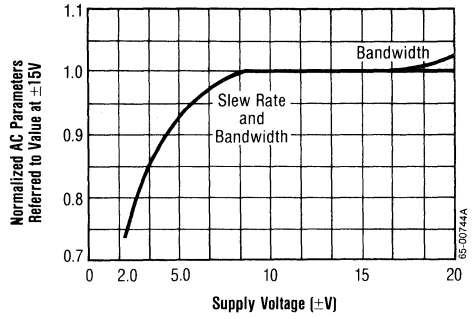


Typical Performance Characteristics (Continued)

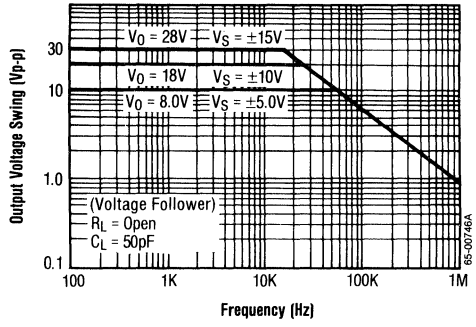
Normalized AC Parameters vs. Temperature



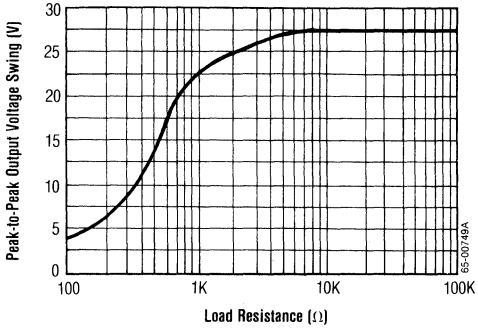
Slew Rate vs. Supply Voltage



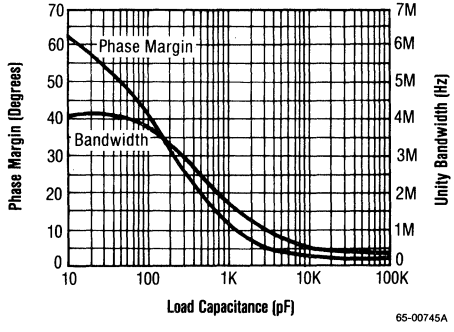
Output Voltage Swing vs. Frequency



Output Voltage Swing vs. Load Resistance

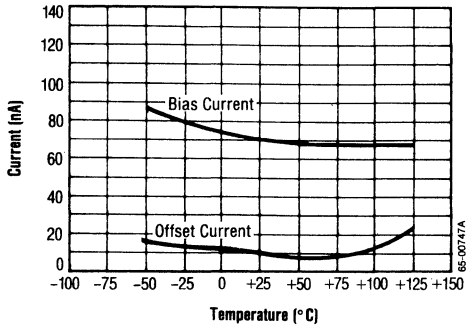


Small Signal Bandwidth and Phase Margin vs. Load Capacitance

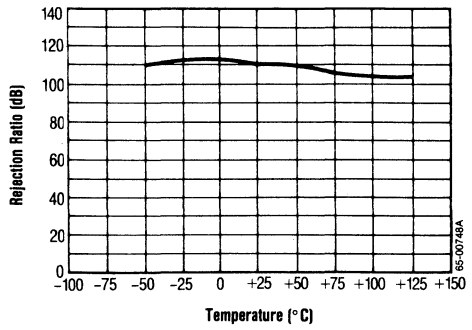


Typical Performance Characteristics (Continued)

Input Current vs. Temperature



Common Mode Rejection Ratio vs. Temperature



Applications

The 4156 and 4157 quad operational amplifiers can be used in almost any 741 application and will provide superior performance. The higher unity gain bandwidth and slew rate make it ideal for applications requiring good frequency response, such as active filter circuits, oscillators and audio amplifiers.

The following applications have been selected to illustrate the advantages of using the Raytheon 4156 and 4157 quad operational amplifiers.

Triangle and Square Wave Generator

The circuit of Figure 1 uses a positive feedback loop closed around a combined comparator and integrator. When power is applied the output of the comparator will switch to one of two states, to the maximum positive or maximum negative voltage. This applies a peak input signal to the integrator, and the integrator output will ramp either down or up, opposite of the input signal. When the integrator output (which is connected to the comparator input) reaches a threshold set by R1 and R2, the comparator will switch to the opposite polarity. This cycle will repeat endlessly, the integrator charging positive then negative, and the comparator switching in a square wave fashion.

Amplitude of V_2 is adjusted by varying R1. For best operation, it is recommended that R1 and V_R be set to obtain a triangle wave at V_2 with ±12V amplitude. This will then allow A3 and A4 to be used for independent adjustment of output-offset and amplitude over a wide range.

The triangle wave frequency is set by C0, R0, and the maximum output voltages of the comparator. A more symmetrical waveform can be generated by adding a back-to-back zener diode pair as shown in Figure 2.

An asymmetric triangle wave is needed in some applications. Adding diodes as shown by the dashed lines is a way to vary the positive and negative slopes independently.

Frequency range can be very wide and the circuit will function very well up to about 10 kHz. Transition time for the squave wave at V_1 is less than 21 µS when using the 4156.

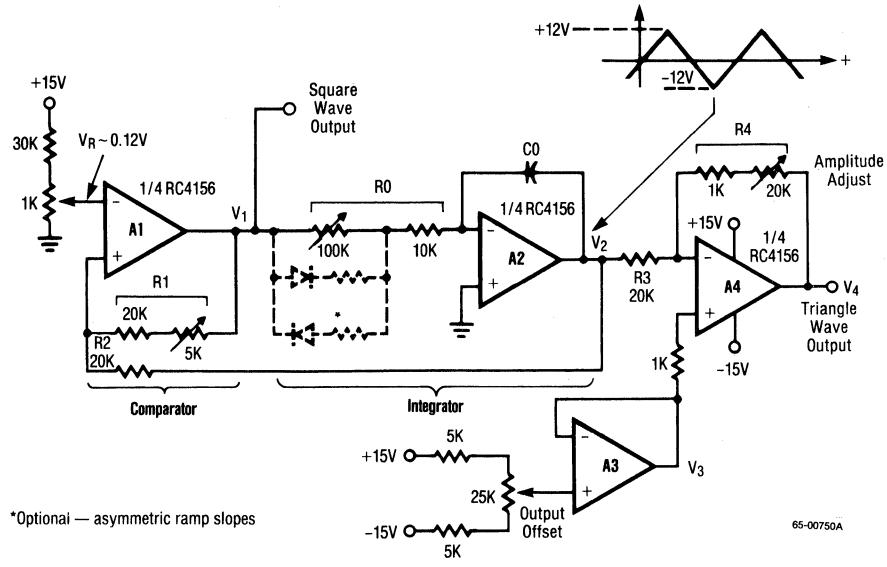


Figure 1. Triangle and Square Wave Generator

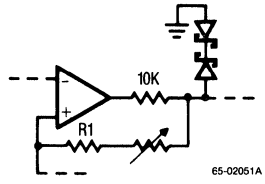
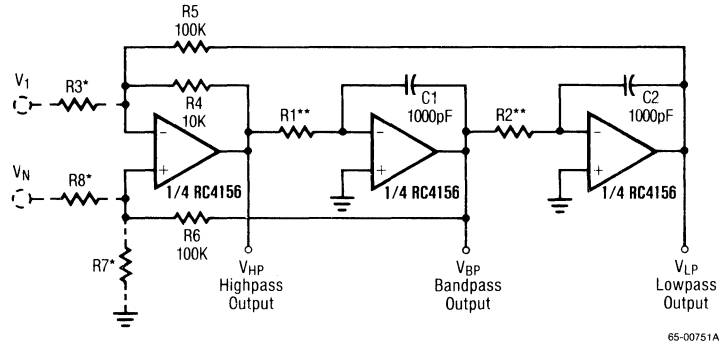


Figure 2. Triangle Generator — Symmetrical Output Option

Active Filters

The introduction of low-cost quad op amps has had a strong impact on active filter design. The complex multiple-feedback, single op amp filter circuits have been rendered obsolete for most applications. State-variable active-filter circuits using three to four op amps per section offer many advantages over the single op amp circuits. They are relatively insensitive to the passive-component tolerances and variations. The Q, gain, and natural frequency can be independently adjusted. Hybrid construction is very practical because resistor and capacitor values are relatively low and the filter parameters are determined by resistance ratios rather than by single resistors. A generalized circuit diagram of the 2-pole state-variable active filter is shown in Figure 3. The particular input connections and component-values can be calculated for specific applications. An important feature of the state-variable filter is that it can be inverting or non-inverting and can simultaneously provide three outputs: lowpass, bandpass, and highpass. A notch filter can be realized by adding one summing op amp.

The Raytheon 4156 was designed and characterized for use in active filter circuits. Frequency response is fully specified with minimum values for unity-gain bandwidth, slew-rate, and full-power response. Maximum noise is specified.



*Input connections are chosen for inverting or non-inverting response. Values of R3, R7, R8 determine gain and Q.
**Values of R1 and R2 determine natural frequency.

Figure 3. Generalized State-Variable Configuration for Active Filter

Output swing is excellent with no distortion or clipping. The Raytheon 4156 provides full, undistorted response up to 20 kHz and is ideal for use in high-performance audio and telecommunication equipment.

In the state-variable filter circuit, one amplifier performs a summing function and the other two act as integrators. The choice of passive component values is arbitrary, but must be consistent with the amplifier operating range and input signal characteristics. The values shown for C1, C2, R4, R5 and R6 are arbitrary. Pre-selecting their values will simplify the filter tuning procedures, but other values can be used if necessary.

The generalized transfer function for the state-variable active filter is:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$$

Filter response is conventionally described in terms of a natural frequency ω_0 in radians/sec, and Q, the quality of the complex pole pair. The filter parameters ω_0 and Q relate to the coefficients in T(s) as:

$$\omega_0 = \sqrt{b_0} \text{ and } Q = \frac{\omega_0}{b_0}$$

The input configuration determines the polarity (inverting or non-inverting), and the output selection determines the type of filter response (lowpass, bandpass, or highpass).

Notch and all-pass configurations can be implemented by adding another summing amplifier.

Bandpass filters are of particular importance in audio and telecommunication equipment. A design approach to bandpass filters will be shown as an example of the state-variable configuration.

Design Example — Bandpass Filter

In this example, the input signal is applied through R3 to the inverting input of the summing amplifier and the output is taken from the first integrator (V_{BP}). The summing amplifier will maintain equal voltage at the inverting and non-inverting inputs (see equation on next page).

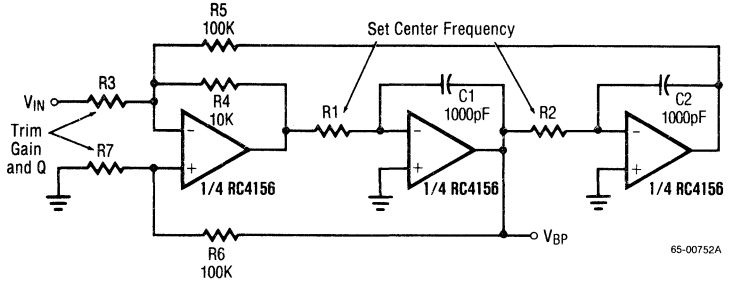


Figure 4. Bandpass Active Filter

$$\frac{\frac{R3R5}{R3+R5}}{R4+\frac{R3R5}{R3+R5}}V_{HP}(s)+\frac{\frac{R3R4}{R3+R4}}{R5+\frac{R3R4}{R3+R4}}V_{LP}(s)+\frac{\frac{R4R5}{R4+R5}}{R3+\frac{R4R5}{R4+R5}}V_{IN}(s)=\frac{R7}{R6+R7}V_{BP}(s)$$

These equations can be combined to obtain the transfer function:

$$V_{BP}(s)=-\frac{1}{R1C1S}V_{HP}(s) \text{ and } V_{LP}(s)=-\frac{1}{R2C2S}V_{BP}(s)$$

$$\frac{V_{BP}(s)}{V_{IN}(s)}=\frac{\frac{R4}{R3}\frac{1}{R1C1}s}{s^2+\frac{R7}{R6+R7}\left(1+\frac{R4}{R5}+\frac{R4}{R3}\right)\left(\frac{1}{R1C1}\right)s+\frac{R4}{R5}\frac{1}{R1C1R2C2}}$$

Defining 1/R1C1 as ω_1, 1/R2C2 as ω_2, and substituting in the assigned values for R4, R5, and R6, then the transfer function simplifies to:

$$\frac{V_{BP}(s)}{V_{IN}(s)}=\frac{\frac{10^4}{R3}\omega_1 s}{s^2+\left[\frac{1.1+\frac{10^4}{R3}}{1+\frac{10^5}{R7}}\right]\omega_1 s+\frac{0.1}{\omega_1\omega_2}}$$

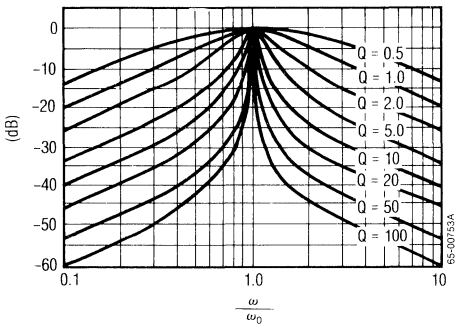
This is now in a convenient form to look at the center-frequency ω_0 and filter Q.

$$\omega_0=\sqrt{0.1\omega_1\omega_2}$$

$$=10^{-9}\sqrt{0.1R1R2}$$

$$\text{and } Q=\left[\frac{1+\frac{10^5}{R7}}{1.1+\frac{10^4}{R3}}\right]\omega_0$$

The frequency response for various values of Q are shown in Figure 5.



$$\frac{V_{BP}}{V_{IN}} = \frac{\frac{\omega}{\omega_0}\,\frac{1}{Q}}{\sqrt{\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right]^2+\left(\frac{1}{Q}\,\frac{\omega}{\omega_0}\right)^2}}$$

Figure 5. Bandpass Transfer Characteristics Normalized for Unity Gain and Frequency

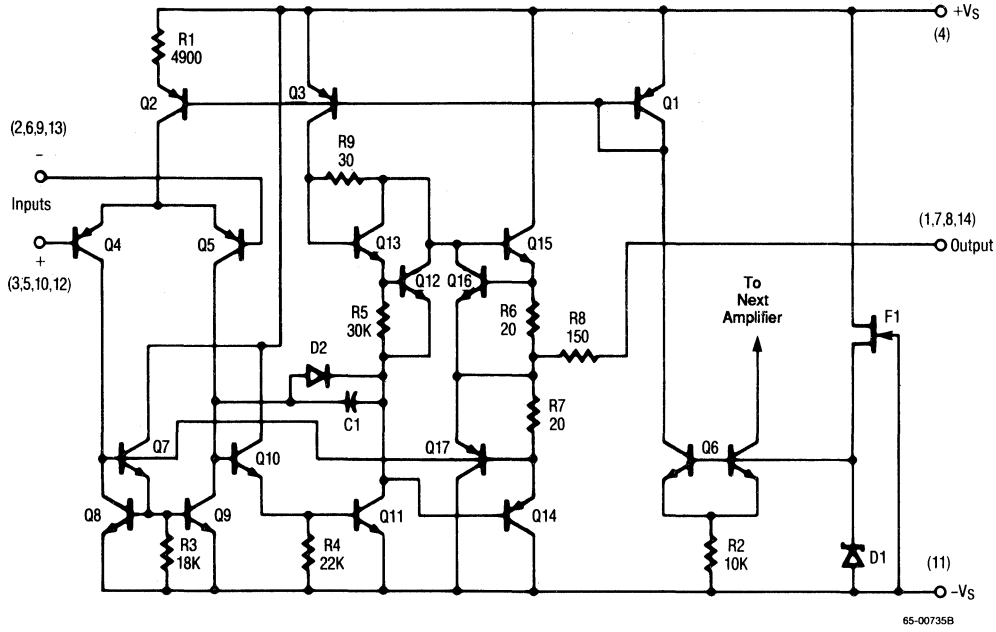
These equations suggest a tuning sequence where ω is first trimmed via R1 or R2, then Q is trimmed by varying R7 and/or R3. An important advantage of the state-variable bandpass filter is that Q can be varied without affecting center frequency ω_0.

This analysis has assumed ideal op amps operating within their linear range, which is a valid design approach for a reasonable range of ω_0 and Q. At extremes of ω_0 and at high values of Q, the op amp parameters become significant. A rigorous analysis is very complex, but some factors are particularly important in designing active filters.

1. The passive component values should be chosen such that all op amps are operating within their linear region for the anticipated range of input signals. Slew rate, output current rating, and common-mode input range must be considered. For the integrators, the current through the feedback capacitor (I = C dV/dt) should be included in the output current computations.
2. From the equation for Q, it should seem that infinite Q could be obtained by making R7 zero. But as R7 is made small, the Q becomes limited by the op amp gain at the frequency of interest. The effective closed-loop gain is being increased directly as R7 is made smaller, and the ratio of open-loop gain to closed-loop gain is becoming less. The gain and phase error of the filter at high Q is very dependent on the op amp open-loop gain at ω_0.
3. The attenuation at extremes of frequency is limited by the op amp gain and unity-gain bandwidth. For integrators, the finite open-loop op amp gain limits the accuracy at the low-end. The open-loop roll-off of gain limits the filter attenuation at high frequency.

The Raytheon 4156 quad operational amplifier has much better frequency response than a conventional 741 circuit and is ideal for active filter use. Natural frequencies of up to 10 kHz are readily achieved and up to 20 kHz is practical for some configurations. Q can range up to 50 with very good accuracy and up to 500 with reasonable response. The extra gain of the 4156 at high frequencies gives the Raytheon quad op amp an extra margin of performance in active-filter circuits.

Schematic Diagram (1/4 Shown)



RC4558 High-Gain Dual Operational Amplifier

Features

- 2.5 MHz unity gain bandwidth guaranteed
- Supply voltage ±22V for RM4558 and ±15V for RC4558
- Short-circuit protection
- No frequency compensation required
- No latch-up
- Large common-mode and differential voltage ranges
- Low power consumption
- Parameter tracking over temperature range
- Gain and phase match between amplifiers

Description

The 4558 integrated circuit is a dual high-gain operational amplifier internally compensated and constructed on a single silicon IC using an advanced epitaxial process.

Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in single 741 operational amplifier applications providing density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

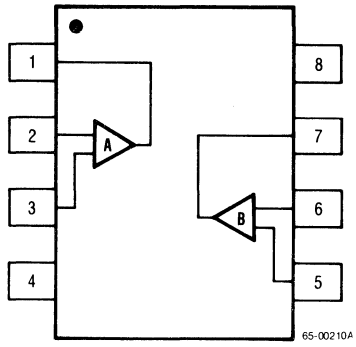
Ordering Information

Part Number	Package	Operating Temperature Range
RC4558M	M	0°C to +70°C
RC4558N	N	0°C to +70°C
RV4558D	D	-25°C to +85°C
RV4558N	N	-25°C to +85°C
RM4558D	D	-55°C to +125°C
RM4558D/883B	D	-55°C to +125°C
RM4558T	T	-55°C to +125°C
RM4558T/883B	T	-55°C to +125°C

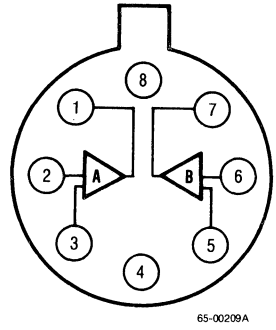
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

8-Lead
Dual In-Line Package
(Top View)



8-Lead
Metal Can TO-99
(Top View)



Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$-V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage
- RM4558 ..... ±22V
- RC4558 ..... ±18V

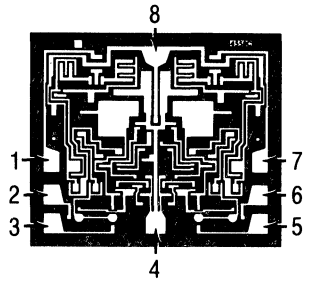
Input Voltage* ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration* ..... Indefinite
Operating Temperature Range
- RM4558 ..... -55°C to +125°C
- RV4558 ..... -25°C to +85°C
- RC4558 ..... 0°C to +70°C

Lead Soldering Temperature
- (SO-8; 10 sec) ..... +260°C

Lead Soldering Temperature
- (DIP, TO-99; 60 sec) ..... +300°C

*For supply voltages less than -15V, the absolute maximum input voltage is equal to the supply voltage.
**Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Mask Pattern



Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Small Outline Plastic SO-8	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	+125°C	+125°C	+175°C	+175°C
Max. P_D T_A <50°C	300 mW	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	240°C/W	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	4.1 mW/°C	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Matching Characterisitics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

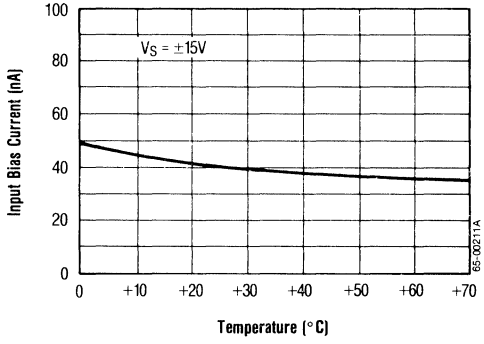
Parameter	Conditions	RC4558 Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current	$R_L \geq 2$ kΩ	±15	nA
Input Offset Current	$R_L \geq 2$ kΩ	±7.5	nA

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise specified)

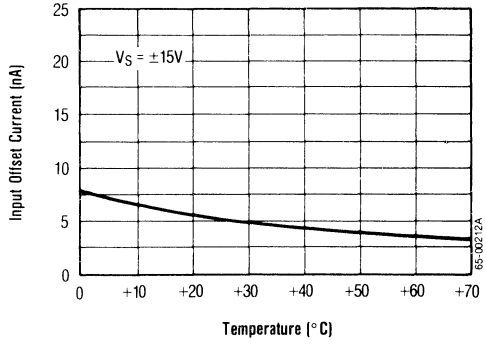
Parameters	Test Conditions	RM4558			RV/RC4558			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	200		5.0	200	nA
Input Bias Current			40	500		40	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	76	100		76	100		dB
Power Consumption	$R_L = \infty$		100	170		100	170	mW
Transient Response Rise Time	V_{IN} = 20mV R_L = 2kΩ		0.3			0.3		μS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate	$R_L \geq 2k\Omega$		0.8			0.8		V/μS
Channel Separation	f = 10kHz, R_S = 1kΩ		90			90		dB
Unity Gain Bandwidth (Gain = 1)		2.5	3.0		2.0	3.0		MHz
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for RM4558; $0°C \leq T_A \leq +70°C$ for RC4558; $-25°C \leq T_A \leq +85°C$ for RV4558								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current RC4558 RV4558				 500 500			 300 500	 nA nA
Input Bias Current RC4558 RV4558				 1500 1500			 800 1500	 nA nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Power Consumption	$R_L = \infty$		120	200		120	200	mW

Typical Performance Characteristics

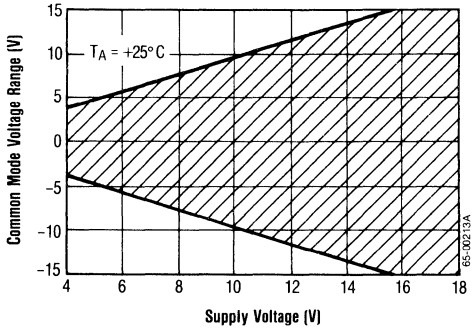
Input Bias Current as a Function of Ambient Temperature



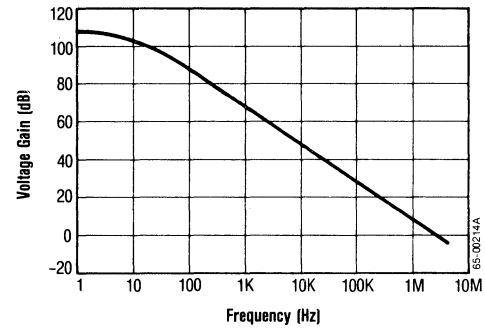
Input Offset Current as a Function of Ambient Temperature



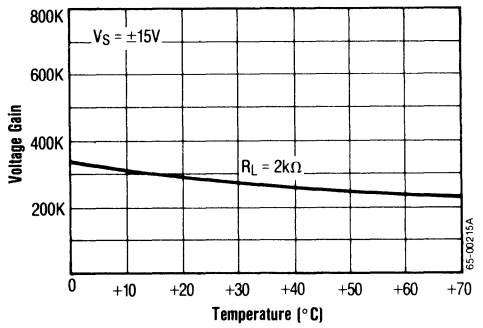
Common Mode Range as a Function of Supply Voltage



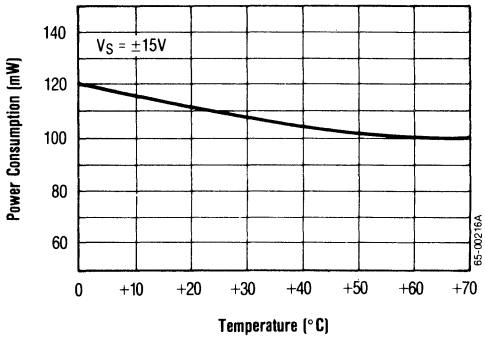
Open Loop Voltage Gain as a Function of Frequency



Open Loop Gain as a Function of Temperature

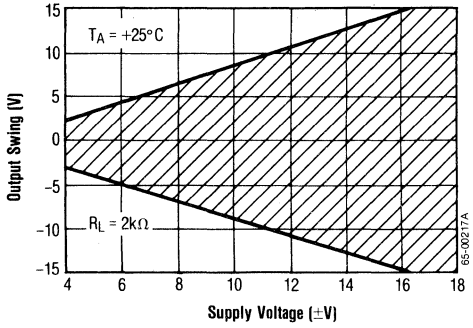


Power Consumption as a Function of Ambient Temperature

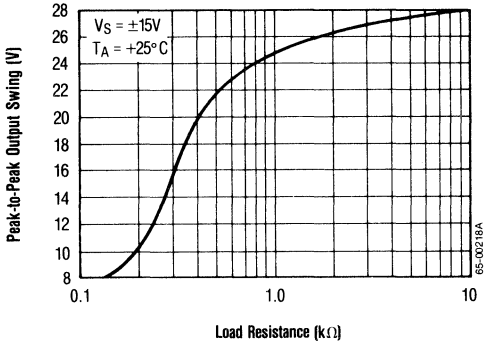


Typical Performance Characteristics (Continued)

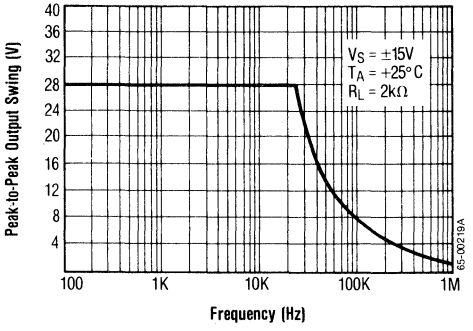
Typical Output Voltage as a Function of Supply Voltage



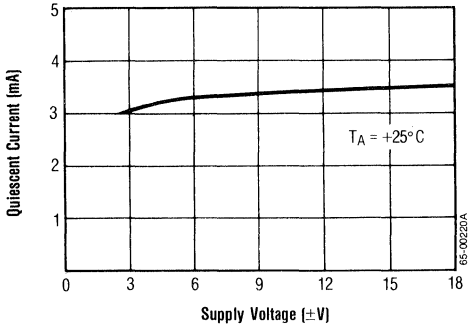
Output Voltage Swing as a Function of Load Resistance



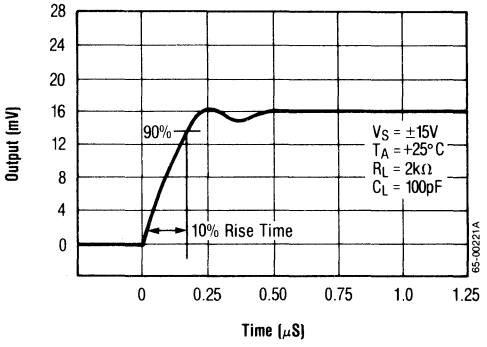
Output Voltage Swing as a Function of Frequency



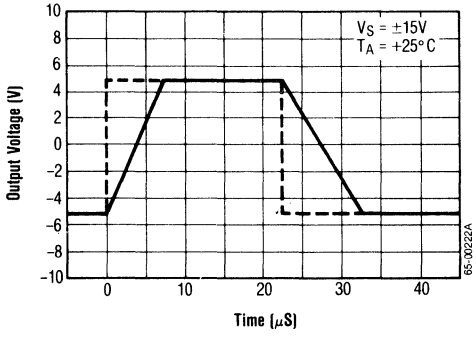
Quiescent Current as a Function of Supply Voltage



Transient Response

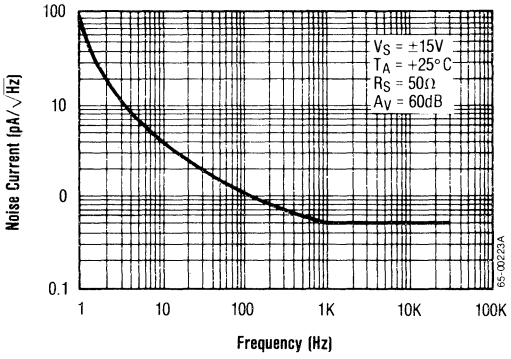


Voltage Follower Large Signal Pulse Response

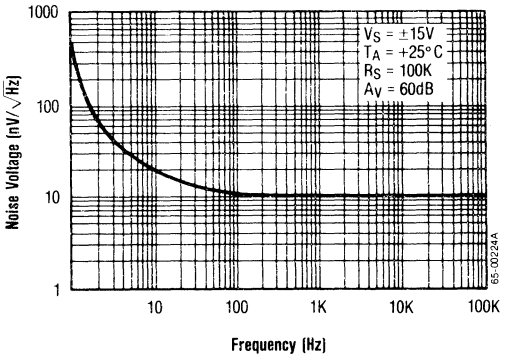


Typical Performance Characteristics (Continued)

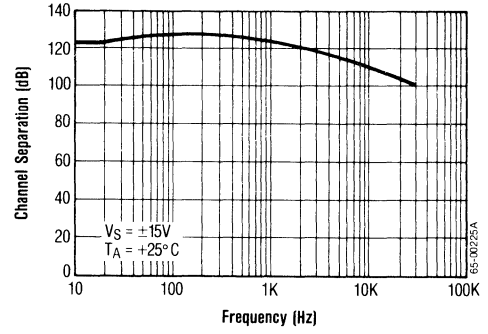
Input Noise Current as a Function of Frequency



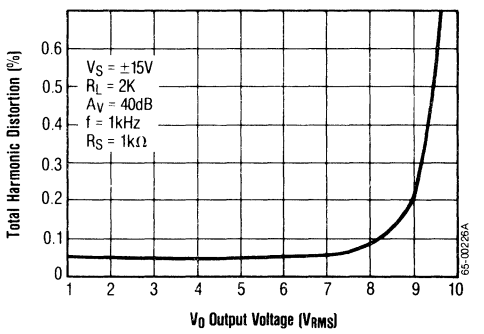
Input Noise Voltage as a Function of Frequency



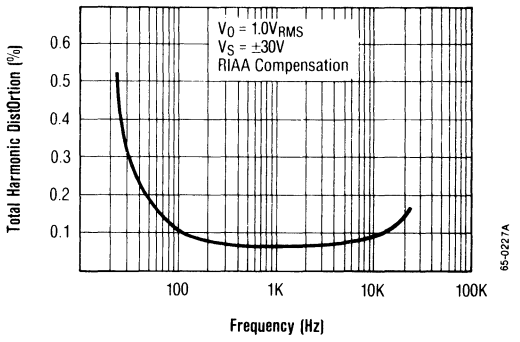
Channel Separation



Total Harmonic Distortion vs. Output Voltage

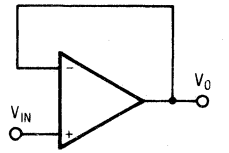


Distortion vs. Frequency



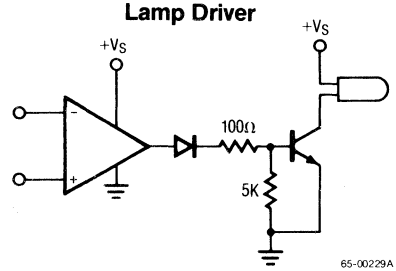
Typical Applications

Voltage Follower



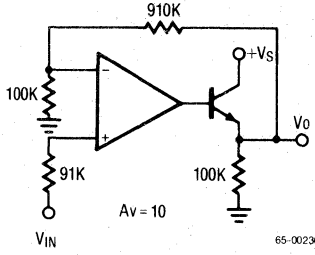
65-00228A

Lamp Driver



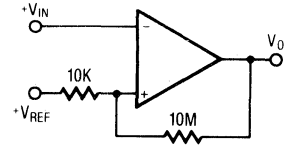
65-00229A

Power Amplifier



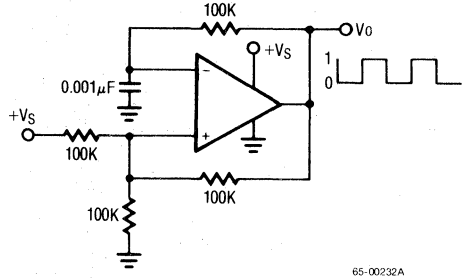
65-00230A

Comparator With Hysteresis



65-00231A

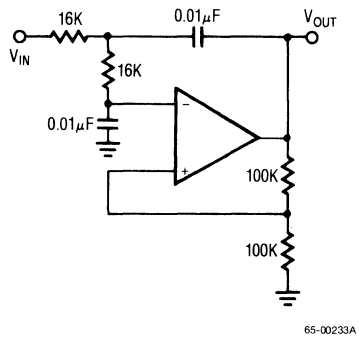
Squarewave Oscillator



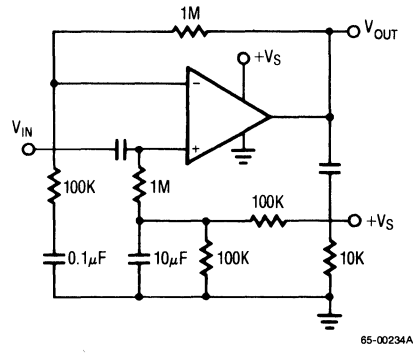
65-00232A

Typical Applications (Continued)

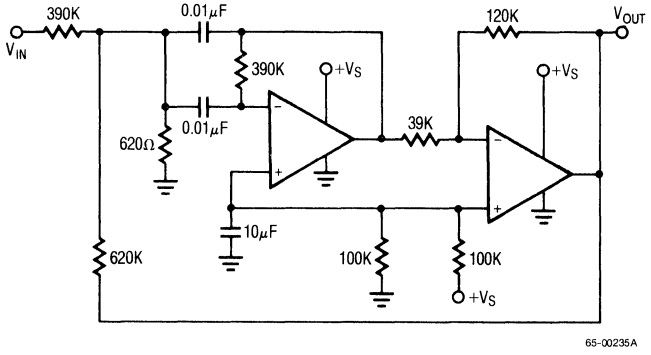
DC Coupled 1kHz Low-Pass Active Filter



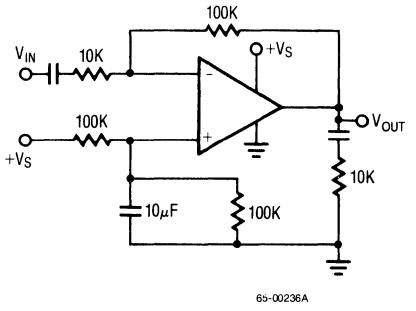
AC Coupled Non-Inverting Amplifier



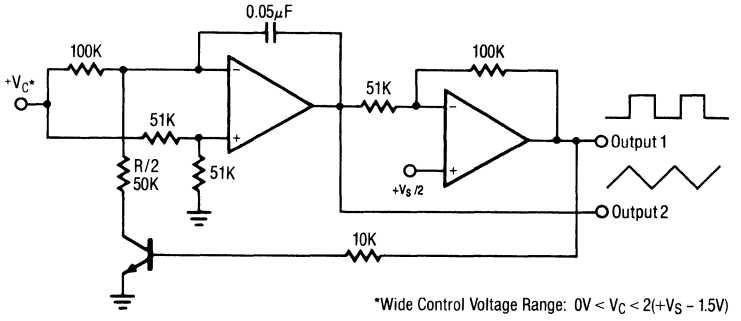
1kHz Bandpass Active Filter



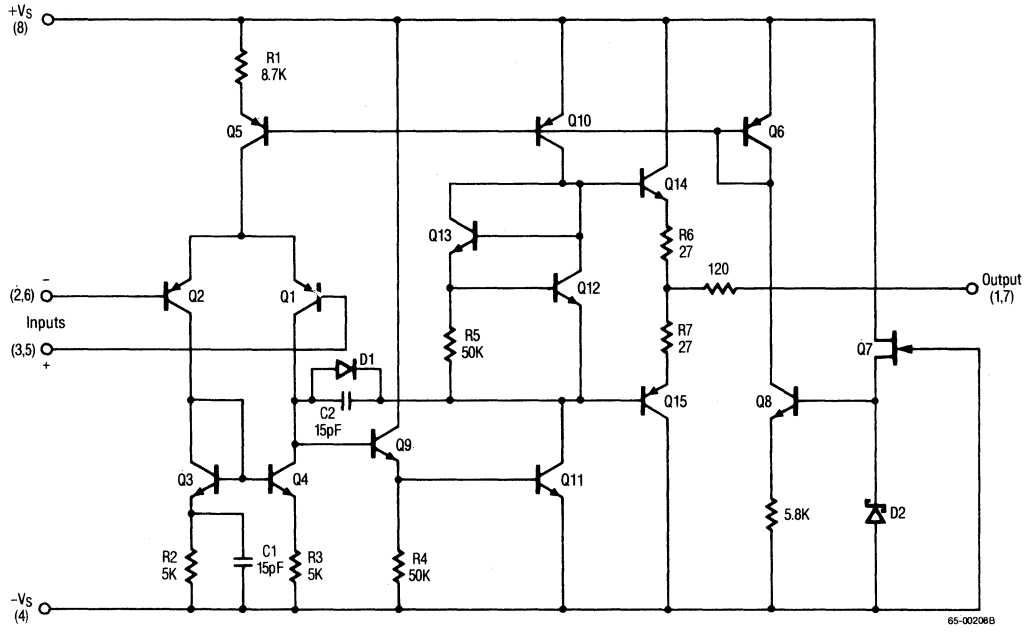
AC Coupled Inverting Amplifier



Voltage Controlled Oscillator (VCO)



Schematic Diagram (1/2 Shown)



RC4559 High-Gain Dual Operational Amplifier

Features

- Unity gain bandwidth — 4.0 MHz typical, 3.0 MHz guaranteed
- Slew rate — 2.0 V/μS typical, 1.5 V/μS guaranteed
- Low noise voltage — 1.4 μV_{RMS} typical, 2.0 μV_{RMS} guaranteed
- Supply voltage — ±22V for RM4559 and ±18V for RC4559
- No frequency compensation required
- No latch up
- Large common mode and differential voltage ranges
- Low power consumption
- Parametric tracking over temperature range
- Gain and phase match between amplifiers

Description

The 4559 integrated circuit is a high performance dual operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process.

These amplifiers feature guaranteed ac performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the 4559 to be used in low-noise signal processing applications such as audio preamplifiers and signal conditioners.

The 4559 also has more output drive capability than 741-type amplifiers and can be used to drive a 600Ω load.

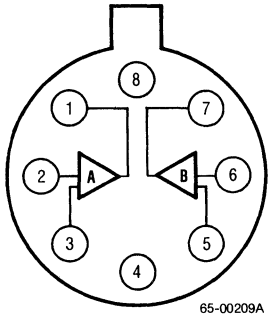
Ordering Information

Part Number	Package	Operating Temperature Range
RC4559M	M	0°C to +70°C
RC4559N	N	0°C to +70°C
RV4559D	D	-25°C to +85°C
RV4559N	N	-25°C to +85°C
RM4559D	D	-55°C to +125°C
RM4559D/883B	D	-55°C to +125°C
RM4559T	T	-55°C to +125°C
RM4559T/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

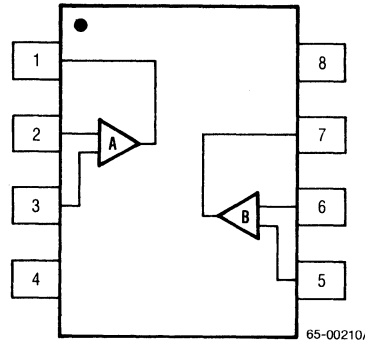
Connection Information

8-Lead Metal Can TO-99
(Top View)



65-00209A

8-Lead Dual In-Line Package
(Top View)



65-00210A

Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (A)
4	$-V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage
- RM4559 ..... ±22V
- RC/RV4559 ..... ±18V

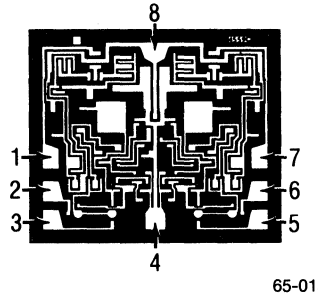
Input Voltage* ..... ±15V
Differential Input Voltage 30V
Output Short Circuit Duration* ..... Indefinite
Operating Temperature Range
- RM4559 ..... -55°C to +125°C
- RV4559 ..... -25°C to +85°C
- RC4559 ..... 0°C to +70°C

Lead Soldering Temperature
- (SO-8; 10 sec) ..... +260°C

Lead Soldering Temperature
- (DIP, TO-99; 60 sec) ..... +300°C

*For supply voltages less than -15V, the absolute maximum input voltage is equal to the supply voltage.
**Short circuit may be to ground on one amp only. Rating applies to +75°C ambient temperature.

Mask Pattern



65-01537A

Die Size: 52 x 61 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Small Outline Plastic SO-8	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	125°C	175°C	175°C
Max. P_D T_A <50°C	300 mW	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	240°C/W	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	4.1 mW/°C	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Matching Characteristics

(V_S = ±15V, T_A = +25°C unless otherwise specified)

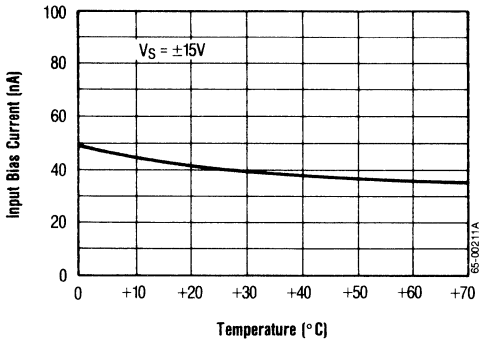
Parameter	Conditions	RC4559 Typ	Units
Voltage Gain	$R_L \geq 2$ kΩ	±1.0	dB
Input Bias Current		±15	nA
Input Offset Current		±7.5	nA

Electrical Characteristics ($V_S = \pm 15V$ and $T_A = +25°C$ unless otherwise specified)

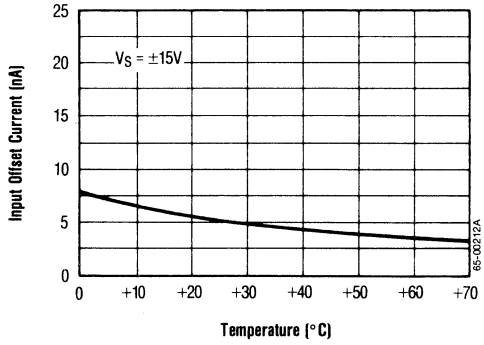
Parameters	Test Conditions	RM4559			RV/RC4559			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offest Current			5.0	100		5.0	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance (Differential Mode)		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	50	300		20	300		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
	$R_L \geq 600\Omega$	±9.5	±10		±9.5	±10		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		80	100		dB
Power Supply Rejection Ratio	$R_S \leq 10k\Omega$	82	100		82	100		dB
Supply Current	$R_L = \infty$		3.3	5.6		3.3	5.6	mA
Transient Response Rise Time	$V_{IN} = 20mV$ $R_L = 2k\Omega$		80			80		nS
Overshoot	$C_L \leq 100pF$		35			35		%
Slew Rate		1.5	2.0		1.5	2.0		V/μS
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Power Bandwidth	$V_O = 20V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage	f = 20Hz to 20kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	f = 20Hz to 20kHz		25			25		pA_{RMS}
Channel Separation	Gain = 100, f = 10kHz $R_S = 1k\Omega$		90			90		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for RM4559; $0°C \leq T_A \leq +70°C$ for RC4559; $-25°C \leq T_A \leq +85°C$ for RV4559								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			500	nA
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25			15			V/mV
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Supply Current	$R_L = \infty$		4.0	6.6		4.0	6.6	mA

Typical Performance Characteristics

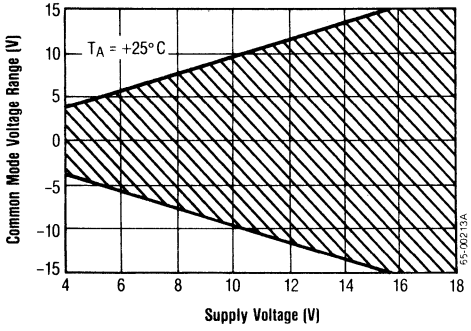
Input Bias Current as a Function of Ambient Temperature



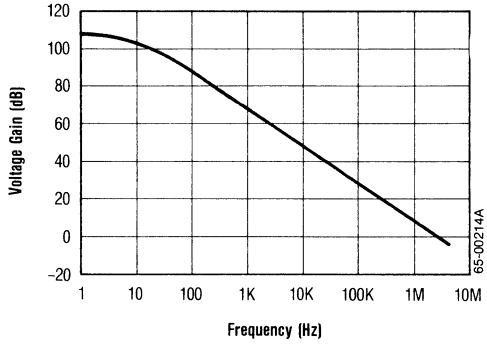
Input Offset Current as a Function of Ambient Temperature



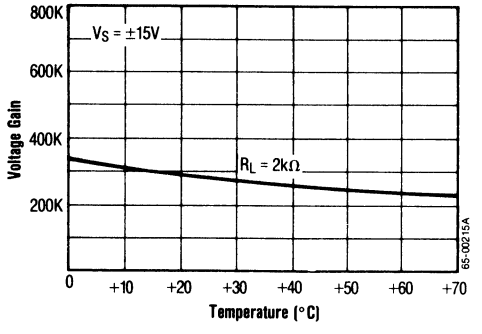
Common Mode Range as a Function of Supply Voltage



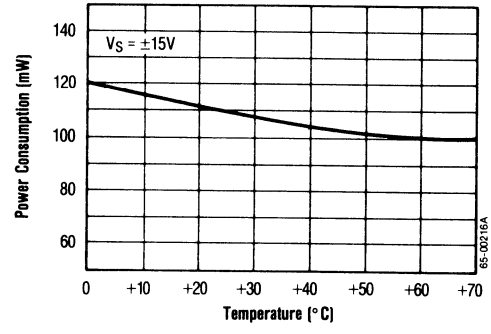
Open Loop Voltage Gain as a Function of Frequency



Open Loop Gain as a Function of Temperature

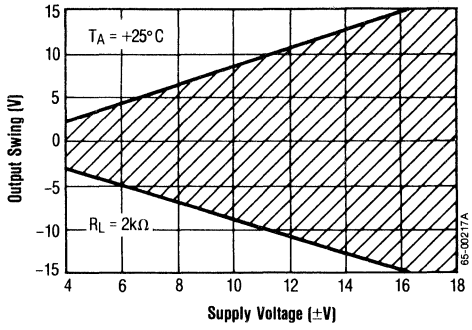


Power Consumption as a Function of Ambient Temperature

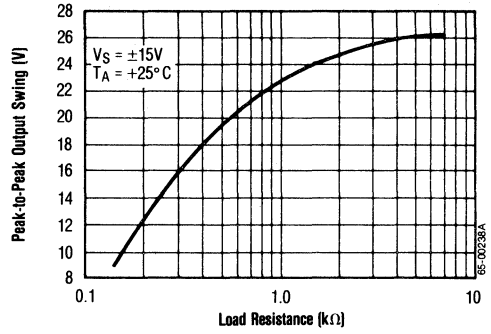


Typical Performance Characteristics (Continued)

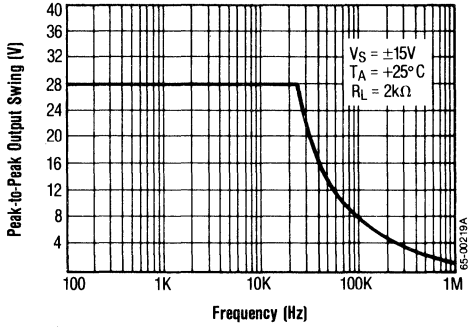
Typical Output Voltage as a Function of Supply Voltage



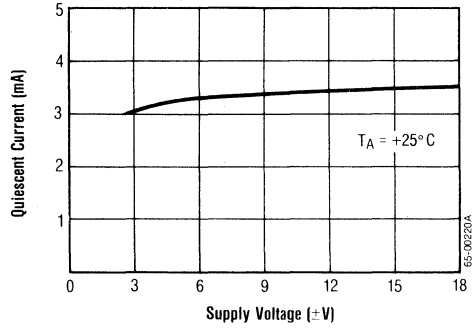
Output Voltage Swing as a Function of Load Resistance



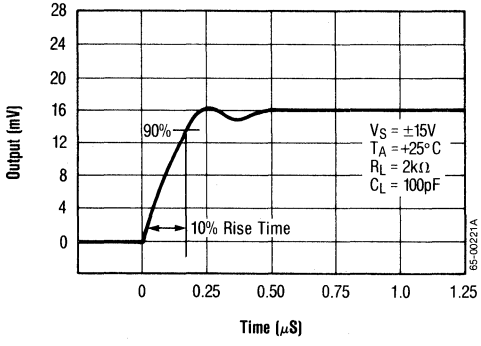
Output Voltage Swing as a Function of Frequency



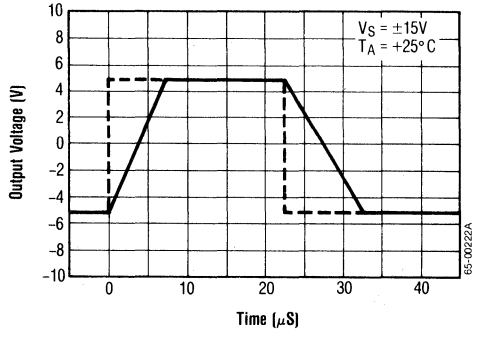
Quiescent Current as a Function of Supply Voltage



Transient Response

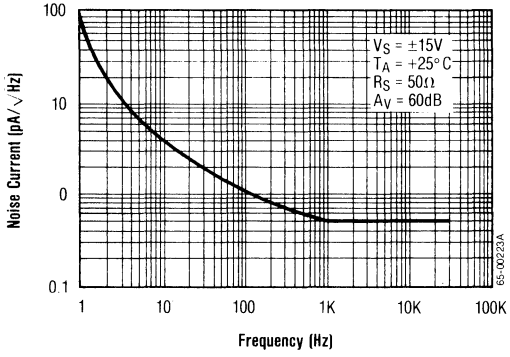


Voltage Follower Large Signal Pulse Response

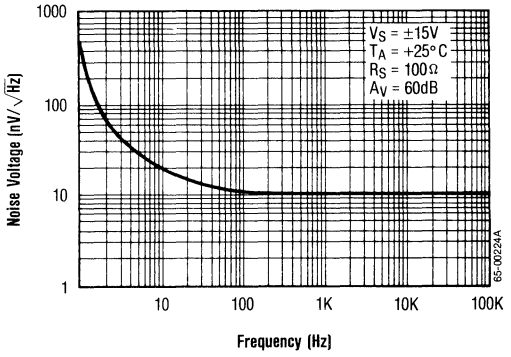


Typical Performance Characteristics (Continued)

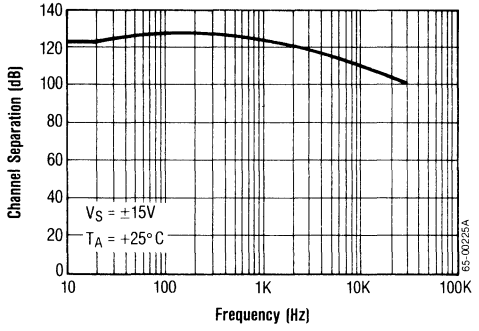
Input Noise Current as a Function of Frequency



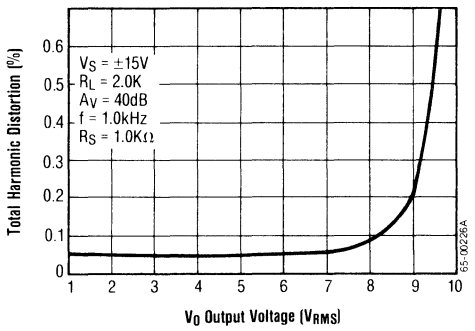
Input Noise Voltage as a Function of Frequency



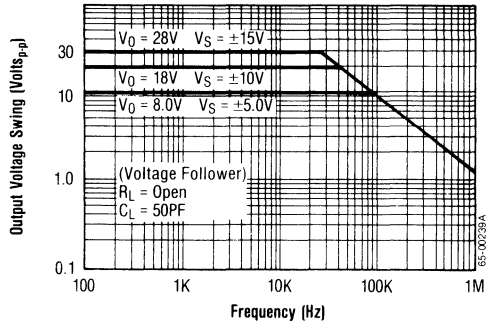
Channel Separation



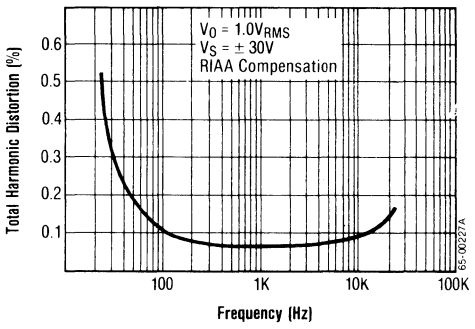
Total Harmonic Distortion vs. Output Voltage



Output Voltage Swing vs. Frequency

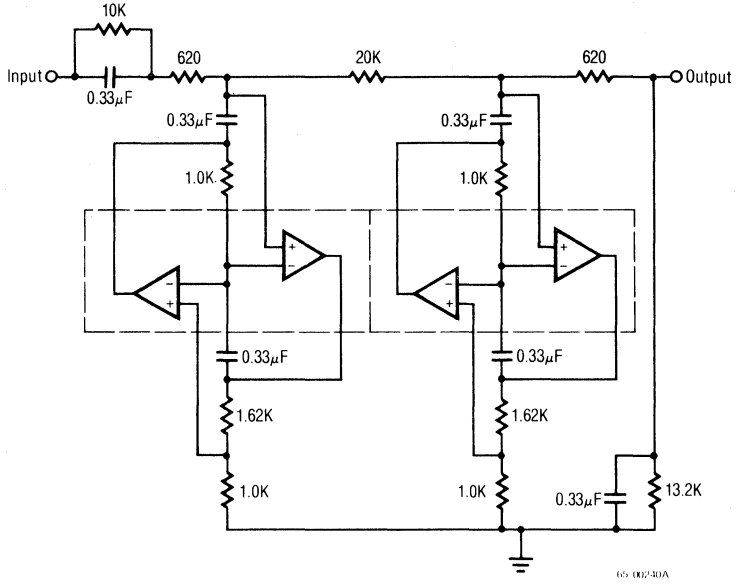


Distortion vs. Frequency

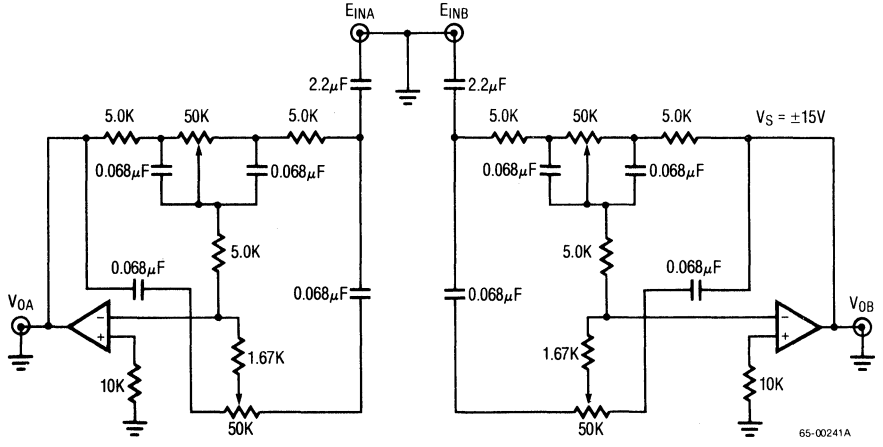


Typical Applications

400Hz Lowpass Butterworth Active Filter

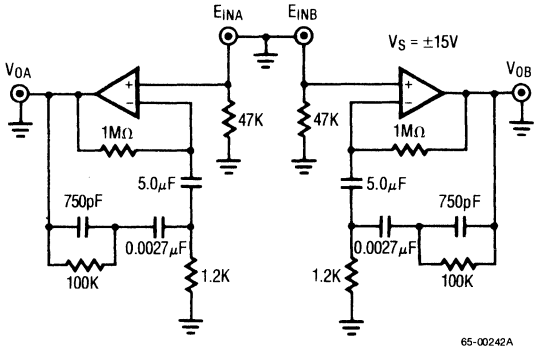


Stereo Tone Control

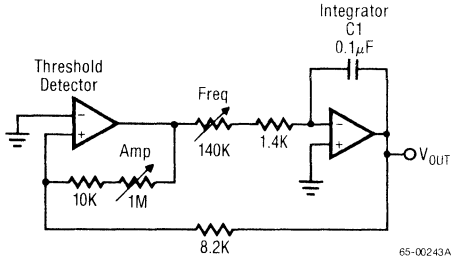


Typical Applications (Continued)

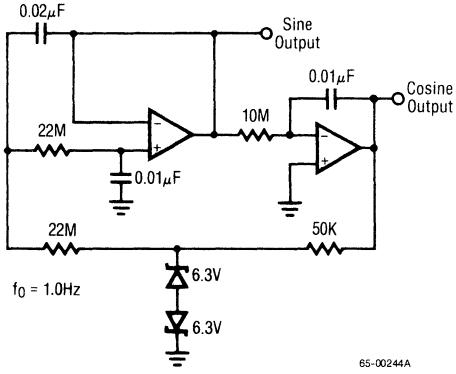
RIAA Preamplifier



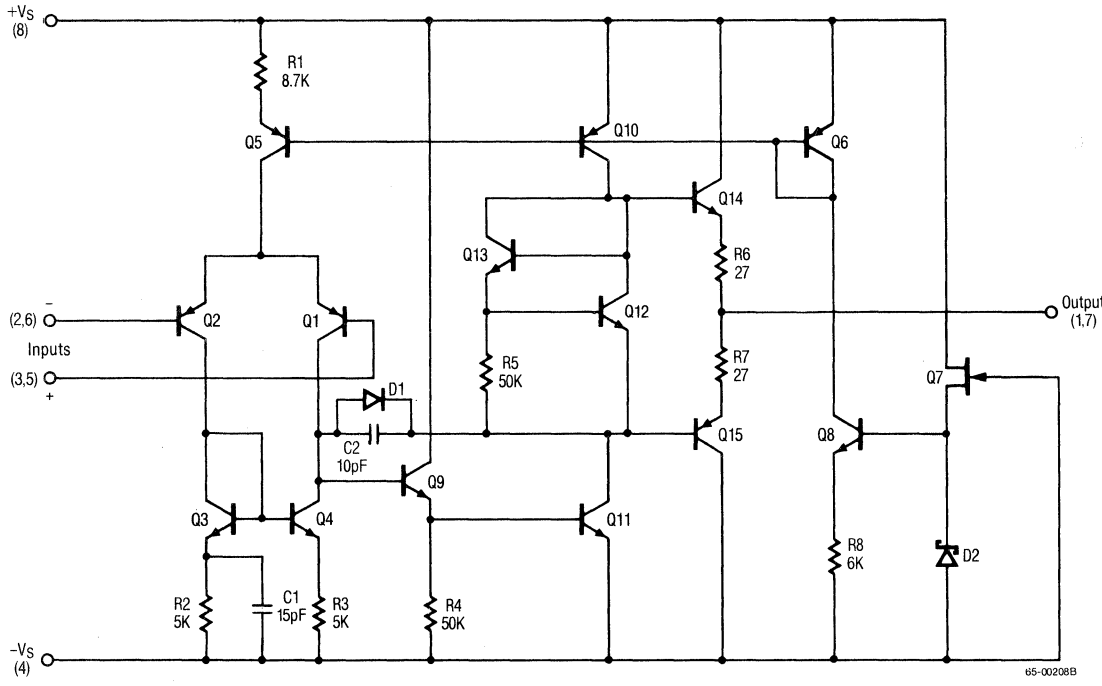
Triangular-Wave Generator



Low Frequency Sine Wave Generator With Quadrature Output



Schematic Diagram



RC4741 General Purpose Operational Amplifier

Features

- Unity gain bandwidth — 3.5 MHz (typ)
- High slew rate — 1.6 V/μS (typ)
- Low noise voltage — 9 nV/√Hz (typ)
- Input offset voltage — 0.5 mV (typ)
- Input bias current — 60 nA (typ)
- Indefinite short circuit protection
- No crossover distortion
- Internal compensation
- Wide power supply range — ±2V to ±20V

Applications

- Universal active filters
- Audio amplifiers
- Battery powered equipment
- D3 communications filters

Description

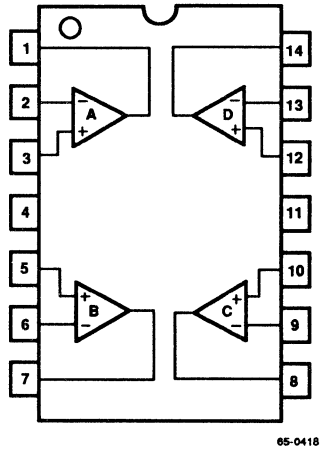
The RC4741 is a monolithic integrated circuit, consisting of four independent operational amplifiers constructed with the planar epitaxial process.

These amplifiers feature ac and dc performance which exceed that of the 741 type amplifiers. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

A wide range of supply voltages (±2V to ±20V) can be used to power the RC4741, making it compatible with almost any system including battery powered equipment.

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-0418

Pin	Function	Pin	Function
1	Output (A)	8	Output (C)
2	-Input (A)	9	-Input (C)
3	+Input (A)	10	+Input (C)
4	$+V_S$	11	Ground
5	+Input (B)	12	+Input (D)
6	-Input (B)	13	-Input (D)
7	Output (B)	14	Output (D)

Ordering Information

Part Number	Package	Operating Temperature Range
RC4741M	M	0°C to +70°C
RC4741N	N	0°C to +70°C
RM4741D	D	-55°C to +125°C
RM4741D/883B*	D	-55°C to +125°C

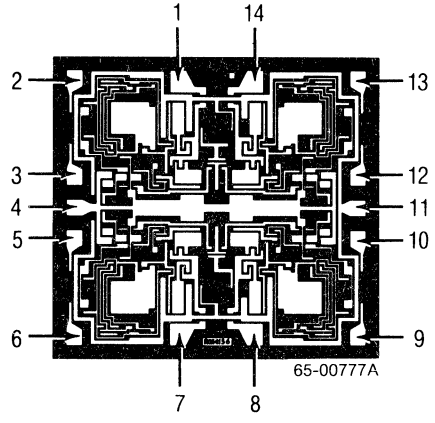
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead small outline
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±20V
Differential Input Voltage 30V
Input Voltage* ..... ±15V
Output Short Circuit Duration** ..... Indefinite
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range
RM4741 ..... -55°C to +125°C
RC4741 ..... 0°C to +70°C
Lead Soldering Temperature
(DIP, 60 sec) ..... +300°C
(SO-14, 10 sec) ..... +260°C

*For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
**Short circuit to ground on one amplifier only.

Mask Pattern



Die Size: 80 x 84 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	14-Lead Small Outline SOIC	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	125°C	175°C
Max. P_D T_A <50°C	300 mW	468 mW	1042 mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25° C unless otherwise specified)

Parameters	Test Conditions	RM4741 Min	RM4741 Typ	RM4741 Max	RC4741 Min	RC4741 Typ	RC4741 Max	Units
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT} ±10V	50	100		25	50		V/mV
Input Voltage Range		±12			±12			V
Output Resistance			300			300		Ω
Output Current	V_{OUT} ±10V	±5	±15		±5	±15		mA
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$ ΔV = ±5V	80			80			dB
Supply Current (All Amplifiers)			4.5	5.0		5.0	7.0	mA
Transient Response Rise Time			75			75		nS
Overshoot			25			25		%
Slew Rate			1.6			1.6		V/μS
Unity Gain Bandwidth			3.5			3.5		MHz
Power Bandwidth	V_O = 20Vp-p R_L = 2k		25			25		kHz
Input Noise Voltage Density	f = 1kHz		9.0			9.0		nV/√Hz
Channel Separation			108			108		dB

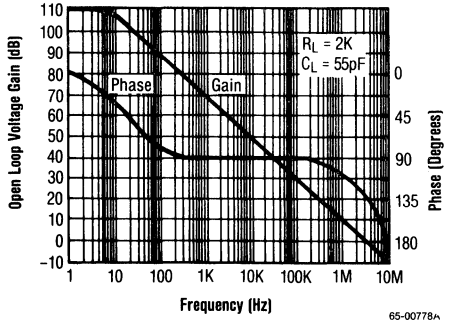
Electrical Characteristics

(VS = ±15V and -55°C ≤T_A ≤ +125°C for RM4741, 0°C ≤ T_A ≤ +70°C for RC4741)

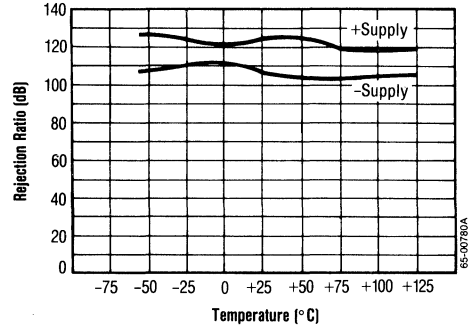
Parameters	Test Conditions	RM4741			RC4741			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	R_S ≤ 10kΩ		4.0	5.0		5.0	6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	R_L ≥ 2kΩ V_{OUT} ±10V	25			15			V/mV
Output Voltage Swing	R_L ≥ 10kΩ	±12	±13.7		±12	±13.7		V
	R_L ≥ 2kΩ	±10	±12.5		±10	±12.5		V
Supply Current (All Amplifiers)			10			10		mA
Average Input Offset Voltage Drift			5.0			5.0		μV/°C
Common Mode Rejection Ratio	R_S ≤ 10kΩ ΔV ±5.0V	74			74			dB
Power Supply Rejection Ratio	R_S ≤ 10kΩ ΔV ±5.0V	80			80			dB

Typical Performance Characteristics

Open Loop Frequency Response

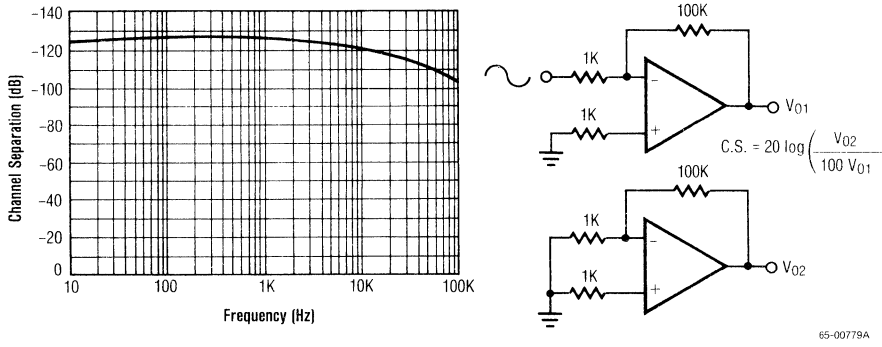


Power Supply Rejection Ratio vs. Temperature

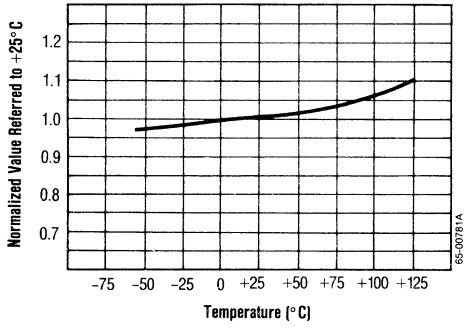


Typical Performance Characteristics (Continued)

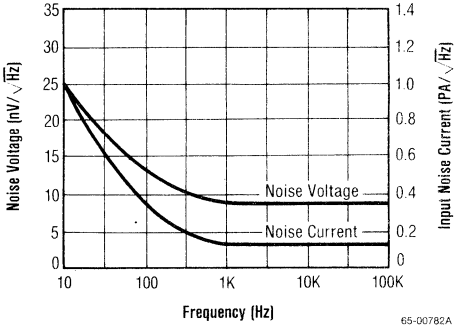
Channel Separation vs. Frequency



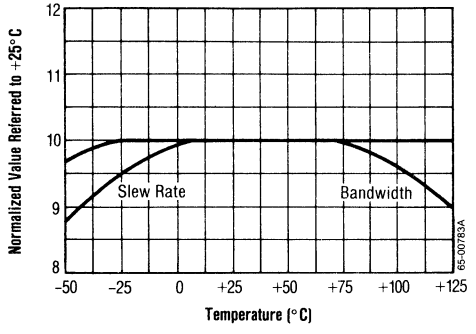
Transient Response vs. Temperature



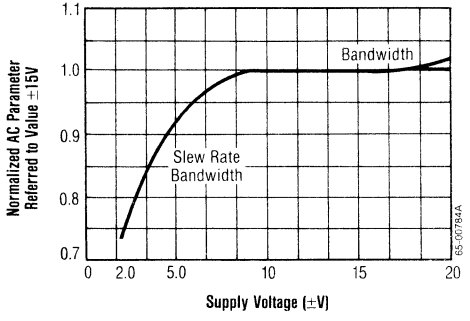
Input Noise vs. Frequency



Normalized AC Parameters vs. Temperature

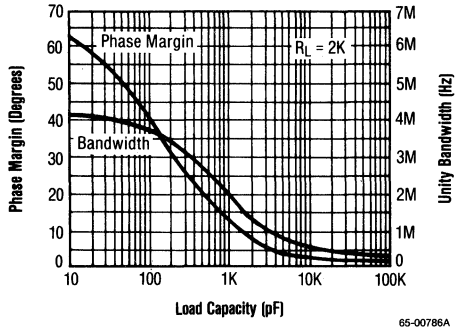


Slew Rate vs. Supply Voltage

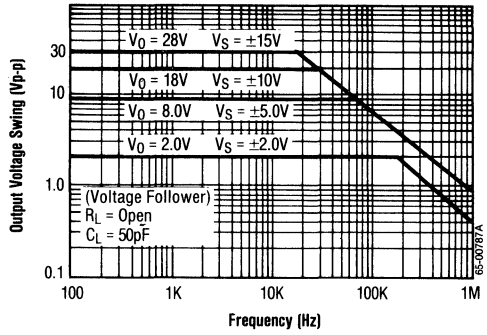


Typical Performance Characteristics (Continued)

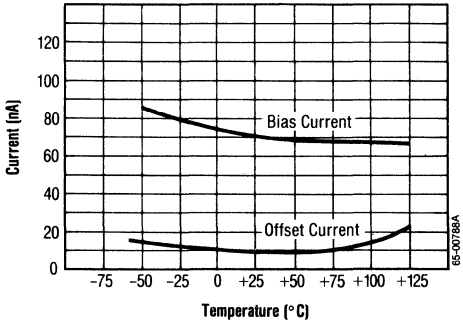
Small Signal Bandwidth and Phase Margin vs. Load Capacitance



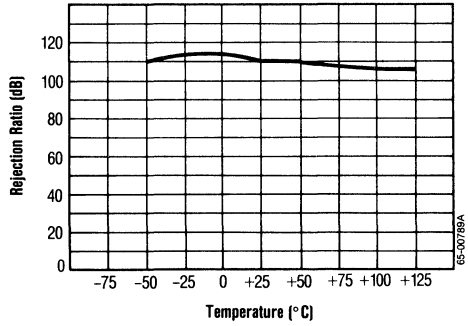
Output Voltage Swing vs. Frequency



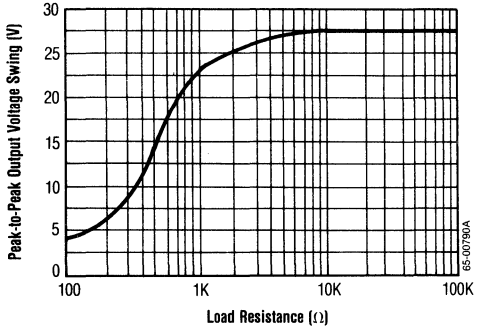
Input Currents vs. Temperature



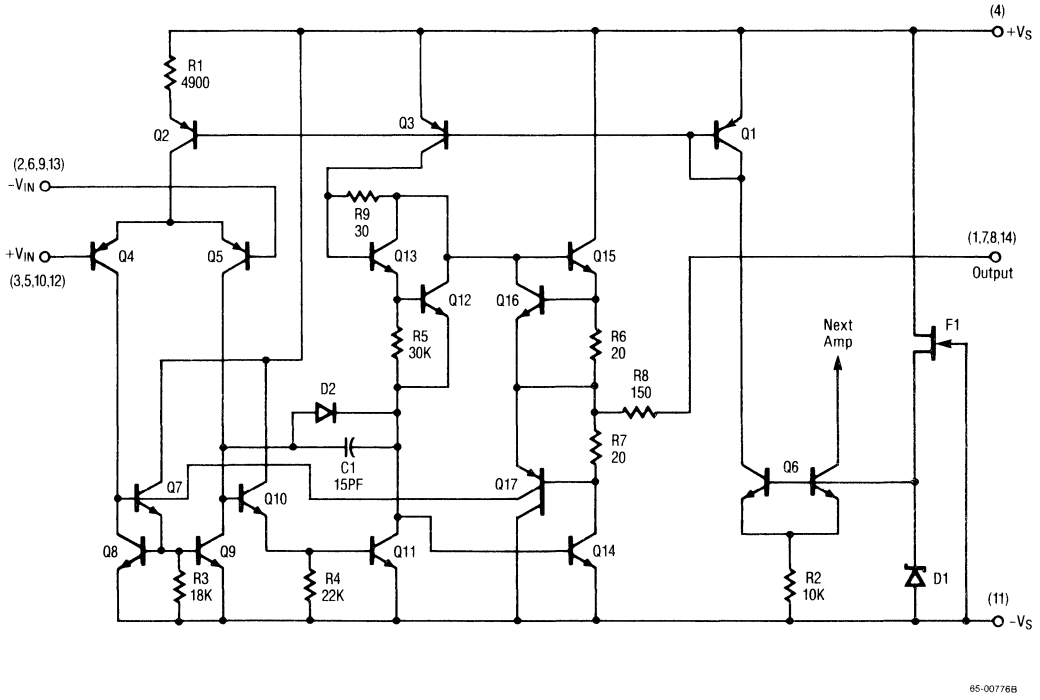
Common Mode Rejection Ratio vs. Temperature



Maximum Output Voltage Swing vs. Load Resistance



Schematic Diagram (1/4 Shown)



RC5532/5532A High Performance Dual Low Noise Operational Amplifier

Features

- Small signal bandwidth — 10 MHz
- Output drive capability — 600Ω, 10 V_{RMS}
- Input noise voltage — 5 nV/√Hz
- DC voltage gain — 50,000
- AC voltage gain — 2200 at 10 kHz
- Power bandwidth — 140 kHz
- Slew rate — 8 V/μS
- Large supply voltage range — ±3V to ±20V

Description

The 5532 is a high performance, dual low noise operational amplifier. Compared to the standard dual operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability, and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation, and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise specifications.

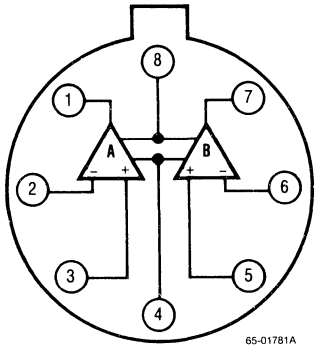
Ordering Information

Part Number	Package	Operating Temperature Range
RC5532N	N	0°C to +70°C
RC5532AN	N	0°C to +70°C
RM5532D	D	-55°C to +125°C
RM5532D/883B*	D	-55°C to +125°C
RM5532AD	D	-55°C to +125°C
RM5532AD/883B*	D	-55°C to +125°C
RM5532T	T	-55°C to +125°C
RM5532T/883B*	T	-55°C to +125°C
RM5532AT	T	-55°C to +125°C
RM5532AT/883B*	T	-55°C to +125°C

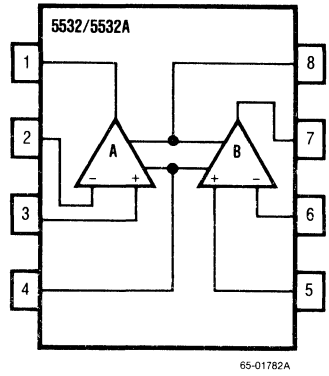
Notes:
*/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can TO-99
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

8-Lead TO-99 Package
(Top View)

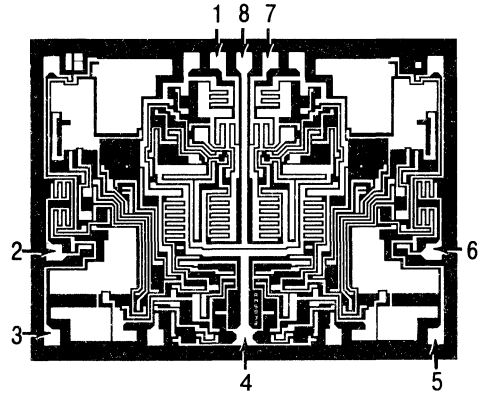


8-Lead Dual In-Line Package
(Top View)



Pin	Function
1	Output (A)
2	-Input (A)
3	+Input (B)
4	$-V_S$
5	+Input (B)
6	-Input (B)
7	Output (B)
8	$+V_S$

Mask Pattern



Die Size: 78 x 104 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage ..... ±V Supply
Differential Input Voltage 0.5V
Operating Temperature Range
RM5532 ..... -55°C to +125°C
RC5532 ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(10 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	125°C	175°C	175°C
Max. P_D T_A <50°C	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

DC Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	RM5532/5532A			RC5532/5532A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			0.5	2.0		0.5	4.0	mV
	Over Temperature			3.0			5.0	mV
Input Offset Current				100		10	150	nA
	Over Temperature			200			200	nA
Input Bias Current			200	400		200	800	nA
	Over Temperature			700			1000	nA
Supply Current			6.0	11		6.0	16	mA
	Over Temperature			13			22	mA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio		80	100		70	100		dB
Power Supply Rejection Ratio		86	100		80	100		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	50			25	100		V/mV
	Over Temperature	25			15	50		V/mV
	$R_L \geq 600\Omega$, V_O = ±10V	40			15	50		V/mV
	Over Temperature	20			10			V/mV
Output Voltage Swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
	R_L = 600Ω, V_S = ±18V	±15	±16		±15	±16		V
	$R_L \geq 2k\Omega$	±12	±13					V
Input Resistance (Diff. Mode)			300			300		kΩ
Short Circuit Current			38			38		mA

Notes:
1. Diodes protect the inputs agains over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For RC5532/RC5532A: T_{MIN} = 0°C, T_{MAX} = +70°C
3. For RM5532/RM5532A: T_{MIN} = -55°C, T_{MAX} = +125°C

Electrical Characteristics (V_S = +15V and T_A = +25°C)

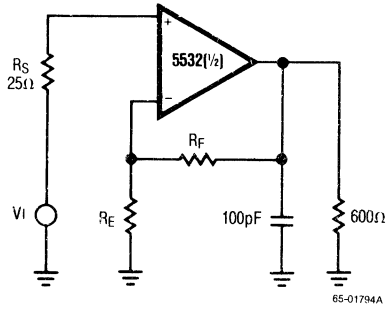
Parameters	Test Conditions	RC/RM5532			RC/RM5532A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Noise Voltage Density	f_o = 30 Hz f_o = 1 kHz		8.0 5.0			8.0 5.0	12 6.0	nV/√Hz
Input Noise Current Density	f_o = 30 Hz f_o - 1 kHz		2.7 0.7			2.7 0.7		pA/√Hz
Channel Separation	f = 1 kHz, R_S = 5 kΩ		110			110		dB

AC Electrical Characteristics (V_S = ±15V and T_A = +25°C)

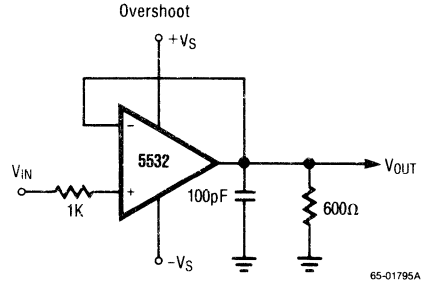
Parameters	Test Conditions	RC/RM5532/5532A Min	Typ	Max	Units
Output Resistance	A_V = 30 dB Closed Loop, f = 10 kHz, R_L = 600Ω		0.3		Ω
Overshoot	Unity Gain, V_{IN} = 100 mV_{P-P} C_L = 100 pF, R_L = 600Ω		10		%
Gain	f = 10 kHz		2.2		V/mV
Gain Bandwidth Product	C_L = 100 pF, R_L = 600Ω		10		MHz
Slew Rate			8.0		V/μS
Power Bandwidth	V_{OUT} = ±10V		140		kHz
	V_{OUT} = ±14V, R_L = 600Ω, V_{CC} = ±18V		100		kHz

Test Circuits

Closed Loop Frequency Response

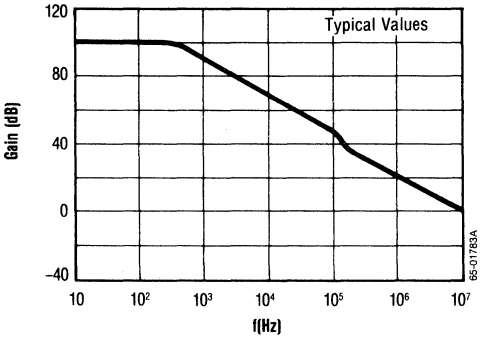


Voltage Follower

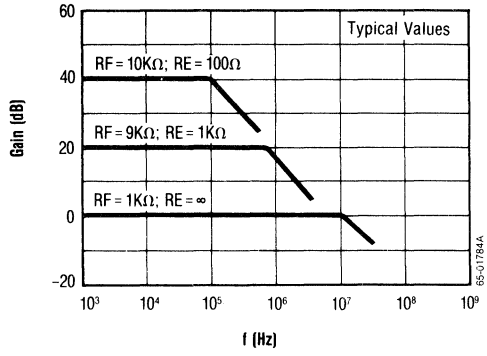


Typical Performance Characteristics

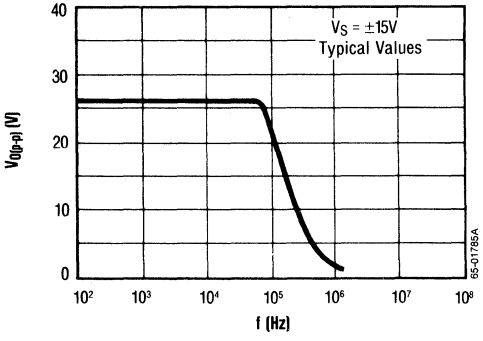
Open Loop Frequency Response



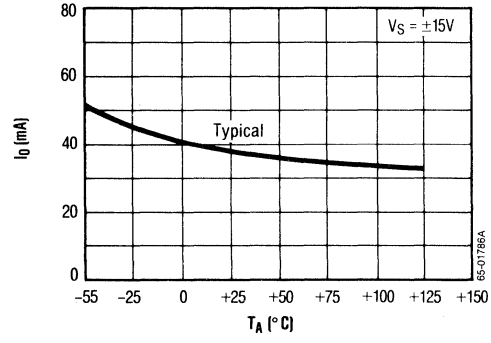
Closed Loop Frequency Response



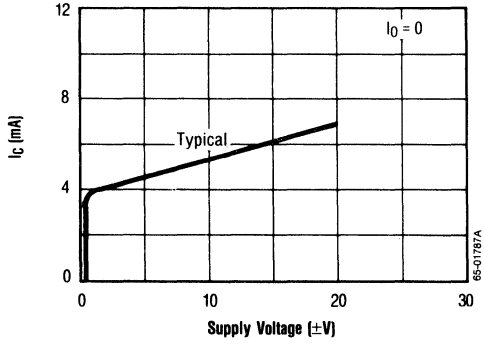
Large Signal Frequency Response



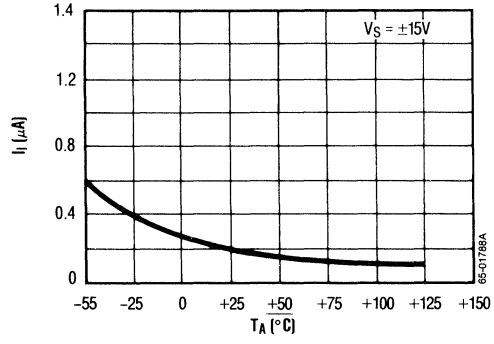
Output Short Circuit Current



Supply Current

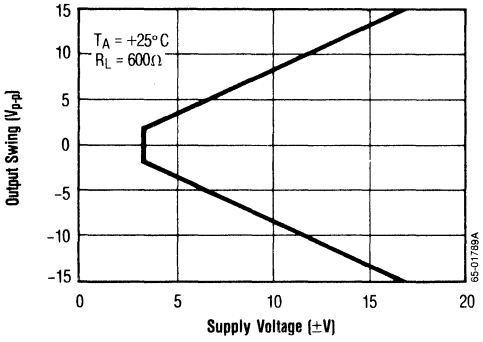


Input Bias Current

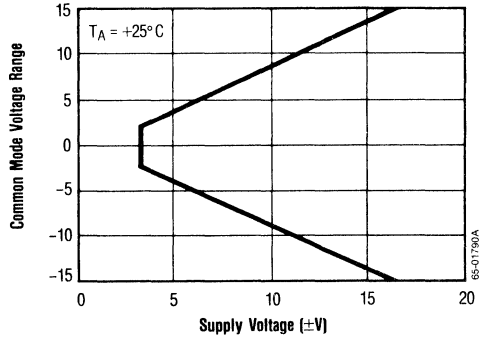


Typical Performance Characteristics (Continued)

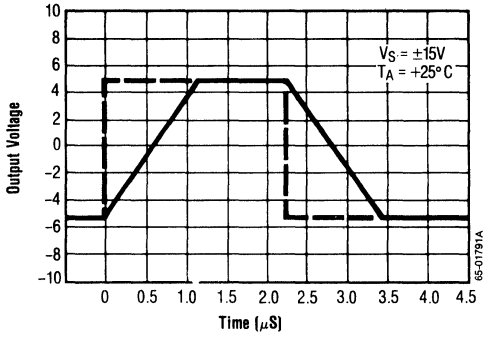
Typical Output Voltage as a Function of Supply Voltage



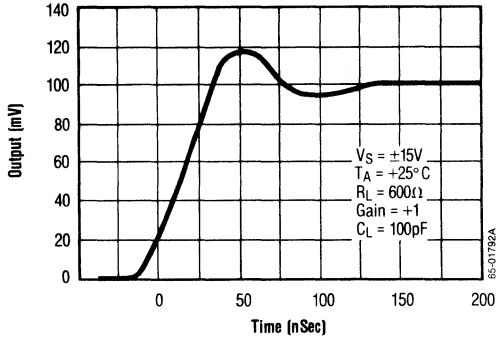
Common Mode Range as a Function of Supply Voltage



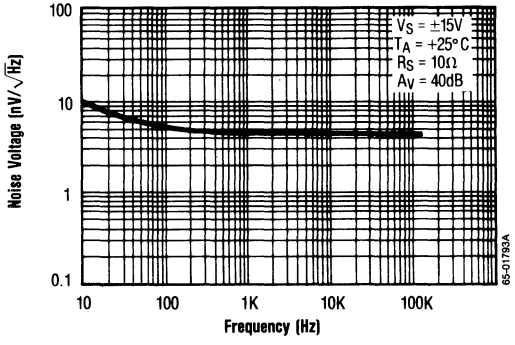
Voltage Follower Large Signal Pulse Response



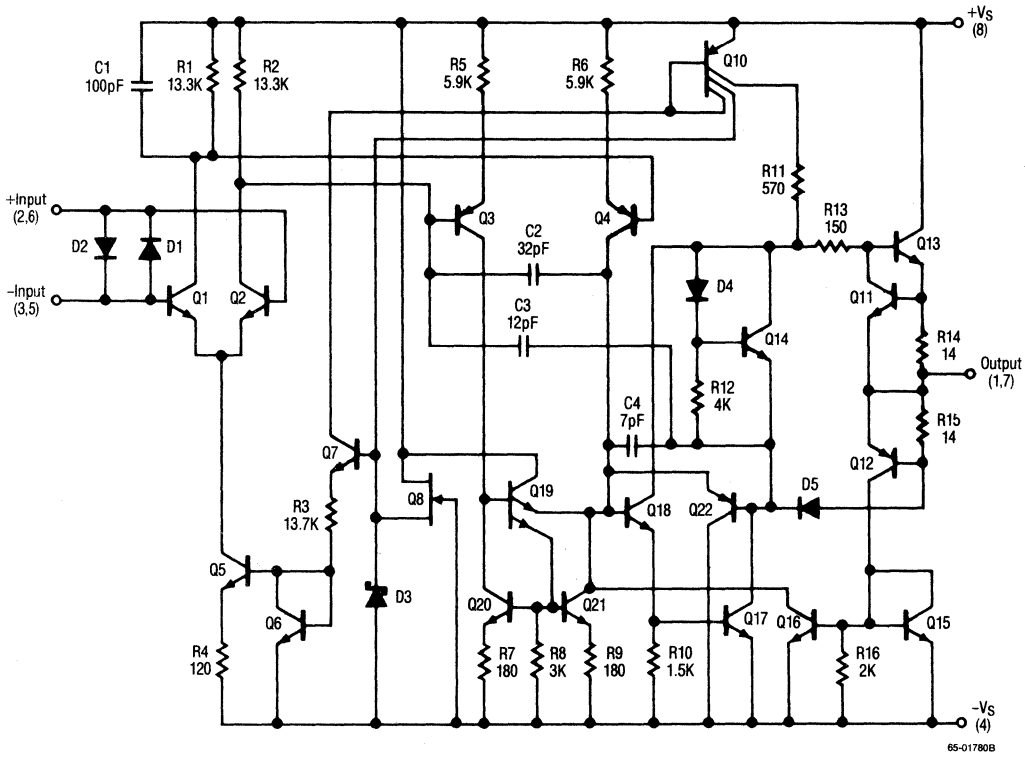
Transient Response



Input Noise Voltage Density



Schematic Diagram (1/2 Shown for 5532)



RC5534/5534A High Performance Low Noise Operational Amplifier

Features

- Small signal bandwidth — 10 MHz
- Output drive capability — 600Ω, 10 V_{RMS} at V_S = ±18V
- Input noise voltage — 4 nV/√Hz
- DC voltage gain — 100,000
- AC voltage gain — 6000 at 10 kHz
- Power bandwidth — 200 kHz
- Slew rate — 13 V/μS
- Large supply voltage range — ±3V to ±20V

Description

The 5534 is a high performance, low noise operational amplifier. Ths amplifier features popular pin-out, superior noise performance, and high output drive capability.

This amplifier also features guaranteed noise performance with substantially higher gain-bandwidth product, power bandwidth, and slew rate which far exceeds that of the 741 type amplifiers. The 5534 is internally compensated for a gain of three or higher and may be externally compensated for optimizing specific performance requirements of various applications such as unity-gain voltage followers, drivers for capacitive loads or fast settling.

The specially designed low noise input transistors allow the 5534 to be used in very low noise signal processing applications such as audio preamplifiers and servo error amplifiers

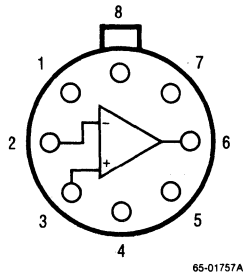
Ordering Information

Part Number	Package	Operating Temperature Range
RC5534N	N	0°C to +70°C
RC5534AN	N	0°C to +70°C
RM5534D	D	-55°C to +125°C
RM5534D/883B*	D	-55°C to +125°C
RM5534AD	D	-55°C to +125°C
RM5534AD/883B*	D	-55°C to +125°C
RM5534T	T	-55°C to +125°C
RM5534T/883B*	T	-55°C to +125°C
RM5534AT	T	-55°C to +125°C
RM5534AT/883B*	T	-55°C to +125°C

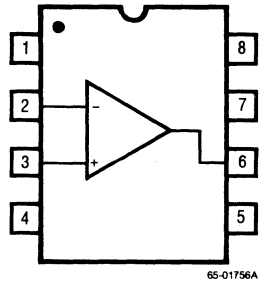
Notes:
*/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can TO-99
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

8-Lead TO-99 Package
(Top View)

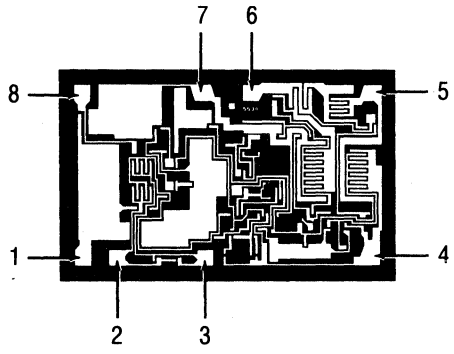


8-Lead Dual In-Line Package
(Top View)



Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	Compensation
6	Output
7	$+V_S$
8	V_{OS} Trim/ Compensation

Mask Pattern



Die Size: 83 x 51 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Differential Input Voltage 0.5V
Input Voltage ..... ±V Supply
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM5534/A ..... -55°C to +125°C
RC5534/A ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C
Output Short Circuit Duration* ..... +300°C

*Short circuit may be to ground only. Rating applies to +125°C case temperature or -175°C ambient temperature.

Thermal Characteristics

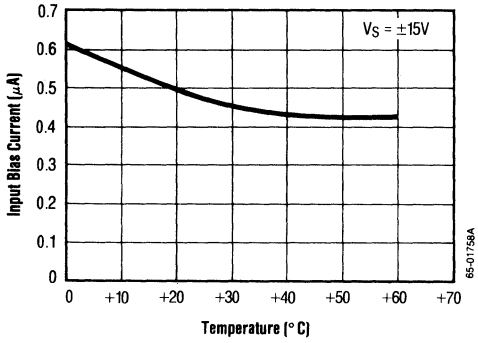
	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can
Max. Junction Temp.	+125°C	+175°C	+175°C
Max. P_D T_A <50°C	468 mW	833 mW	658 mW
Therm. Res θ_{JC}	—	45°C/W	50°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W	190°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	5.26 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

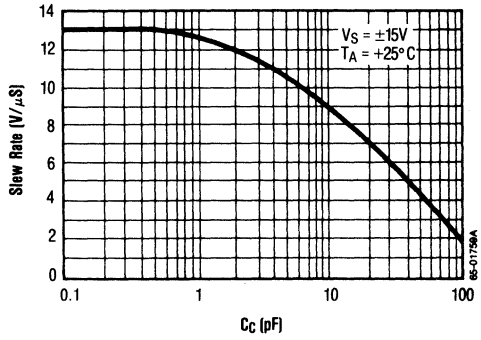
Parameters	Test Conditions	RM5534/A Min	RM5534/A Typ	RM5534/A Max	RC5534/A Min	RC5534/A Typ	RC5534/A Max	Units
Input Offset Voltage	$R_S \le 1k\Omega$		0.5	2.0		0.5	4.0	mV
Input Offset Current			10	200		20	300	nA
Input Bias Current			400	800		500	1500	nA
Input Resistance (Diff.Mode)			100			100		kΩ
Large Signal Voltage Gain	$R_L \ge 600\Omega$, V_{OUT} = ±10V	50	100		25	100		V/mV
Output Voltage Swing	$R_L \ge 600\Omega$	±12	±13		±12	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \le 1k\Omega$	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \le 1k\Omega$	86	100		86	100		dB
Supply Current	$R_L = \infty$		4.0	6.5		4.0	8.0	mA
Transient Response Rise Time	V_{IN} = 50 mV, R_L = 600Ω, C_L = 100 pF, C_C = 22 pF		35			35		nS
Overshoot			17			17		%
Slew Rate	C_C = 0		13			13		V/μS
Gain Bandwidth Product	C_C = 22 pF, C_L = 100 pF		10			10		MHz
Power Bandwidth	$V_O = 20V_{P-P}$, Cc = 0		200			200		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.0			1.0		μV_{RMS}
Input Noise Current	f = 20 Hz to 20 kHz		25			25		pA_{RMS}
Supply Current	V_S = ±15V, $R_L = \infty$			9.0			14	mA
Channel Separation	f = 1 kHz, R_S = 5 kΩ		110			110		dB
			5534A			**5534**		
Input Noise Voltage Density	f_O = 30 Hz		5.5	7.0		7.0		$\frac{nV}{\sqrt{Hz}}$
	f_O = 1 kHz		3.5	4.5		4.0		
Input Noise Current Density	f_O = 30 Hz		1.5			2.5		$\frac{pA}{\sqrt{Hz}}$
	f_O = 1 kHz		0.4			0.6		
Broadband Noise Figure	f = 10 Hz - 20 kHz, R_S = 5 kΩ		0.9					dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C for RM; 0°C ≤ +70°C for RC, V_S = ±15V								
			RM5534/A			**RC5534/A**		
Input Offset Voltage	$R_S \le 1$ kΩ			3.0			5.0	mV
Input Offset Current				500			400	nA
Input Bias Current				1500			2000	nA
Large Signal Voltage Gain	$R_L \ge 600\Omega$, V_{OUT} = ±10V	25			15			V/mV
Output Voltage Swing	$R_L \ge 600\Omega$	±10			±10			V

Typical Performance Characteristics

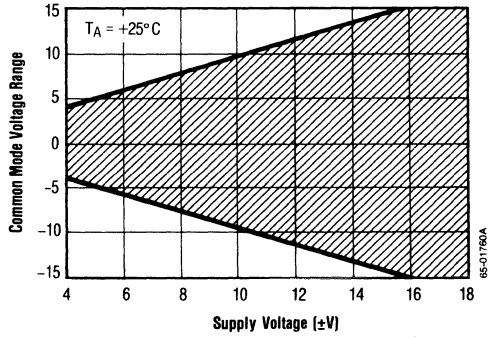
Input Bias Current vs. Temperature



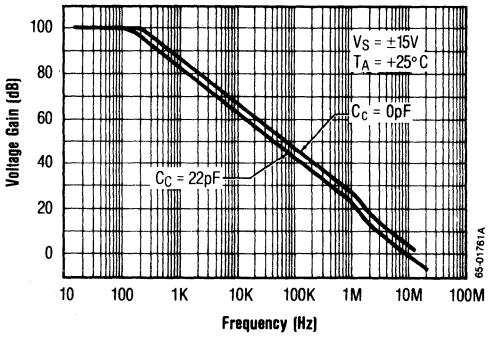
Slew Rate vs. Compensation Capacitor



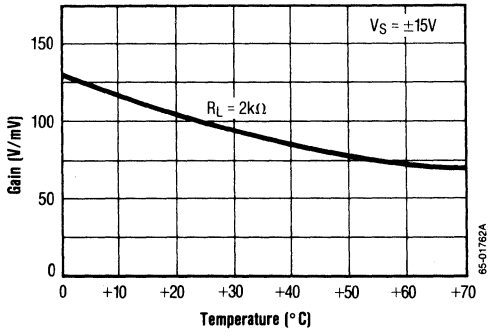
Common Mode Range as a Function of Supply Voltage



Open Loop Gain vs. Frequency

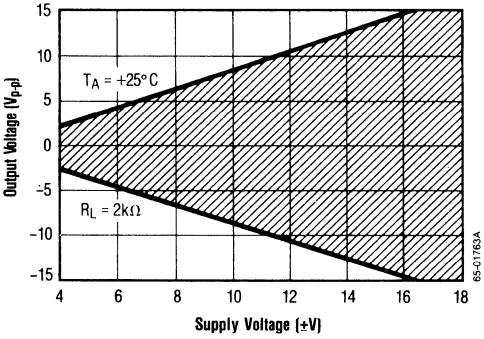


Open Loop Gain vs. Temperature

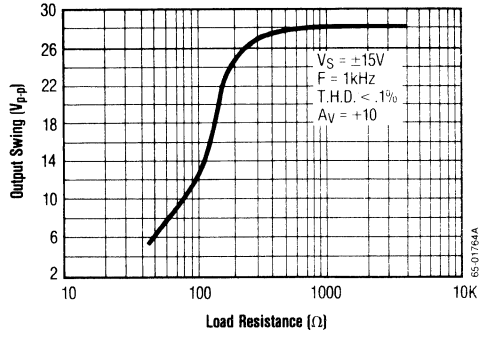


Typical Performance Characteristics (Continued)

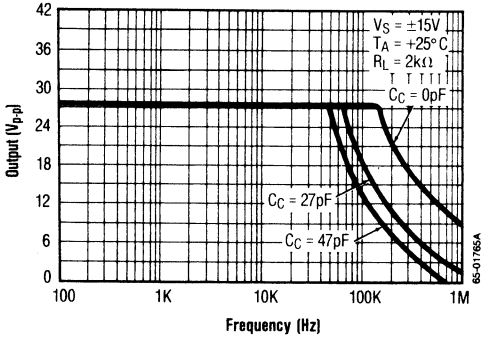
Typical Output Voltage as a Function of Supply Voltage



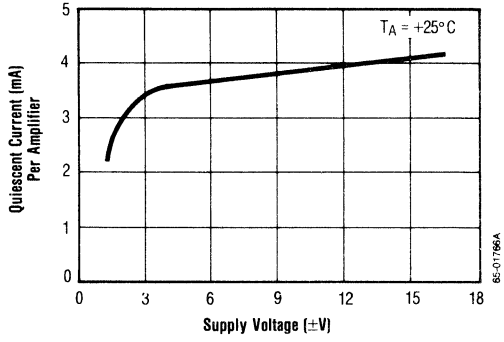
Output Voltage vs. Load Resistance



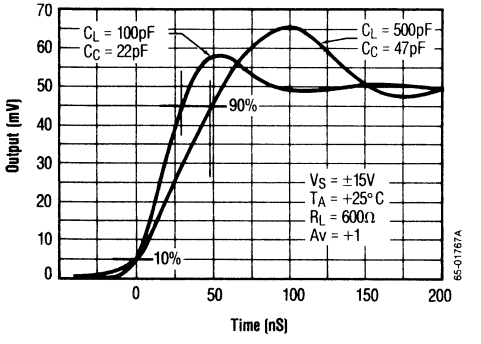
Output Voltage vs. Frequency



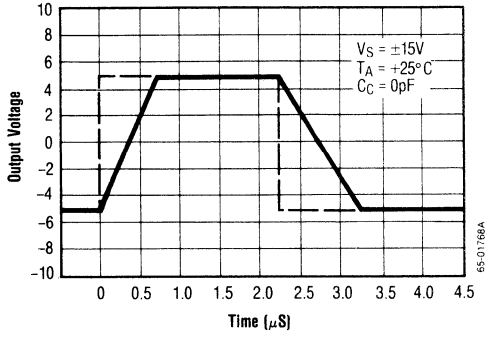
Quiescent Current as a Function of Supply Voltage



Transient Response

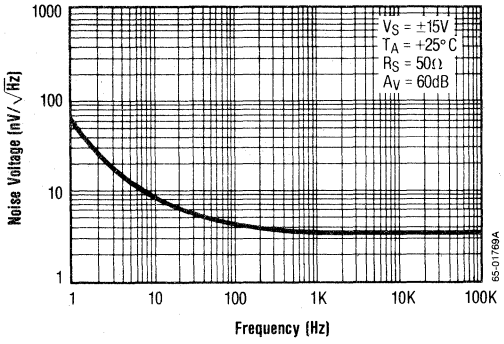


Voltage Follower Large Signal Pulse Response

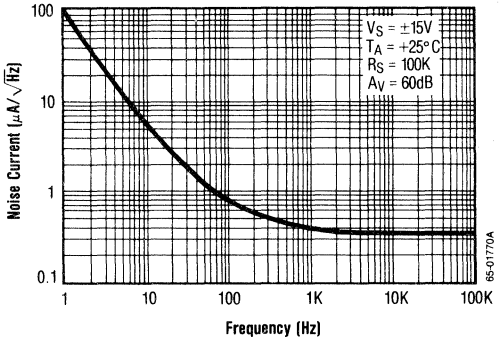


Typical Performance Characteristics (Continued)

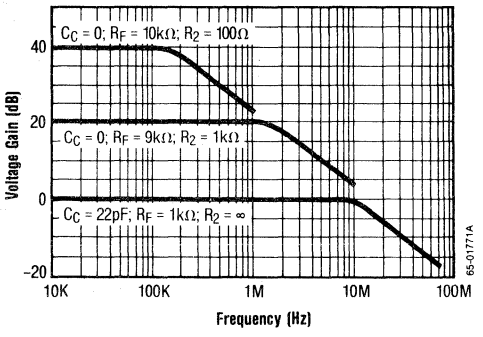
Input Noise Voltage as a Function of Frequency



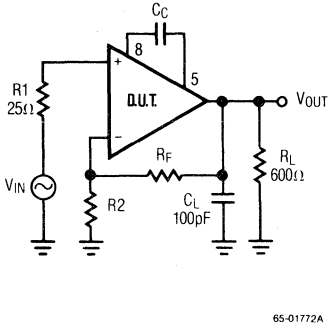
Input Noise Current as a Function of Frequency



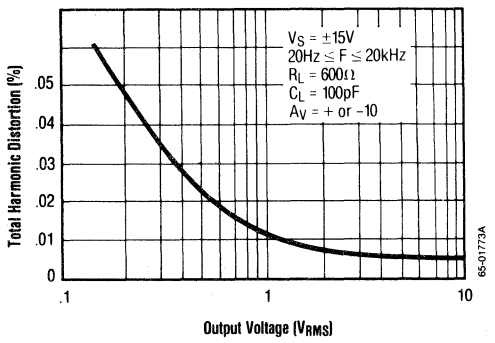
Closed Loop Frequency Response



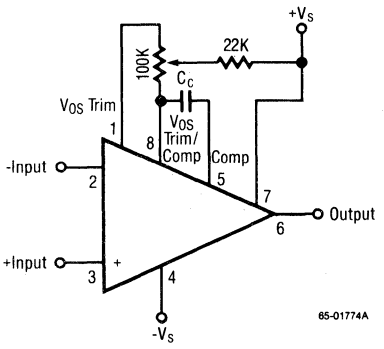
Test Circuit



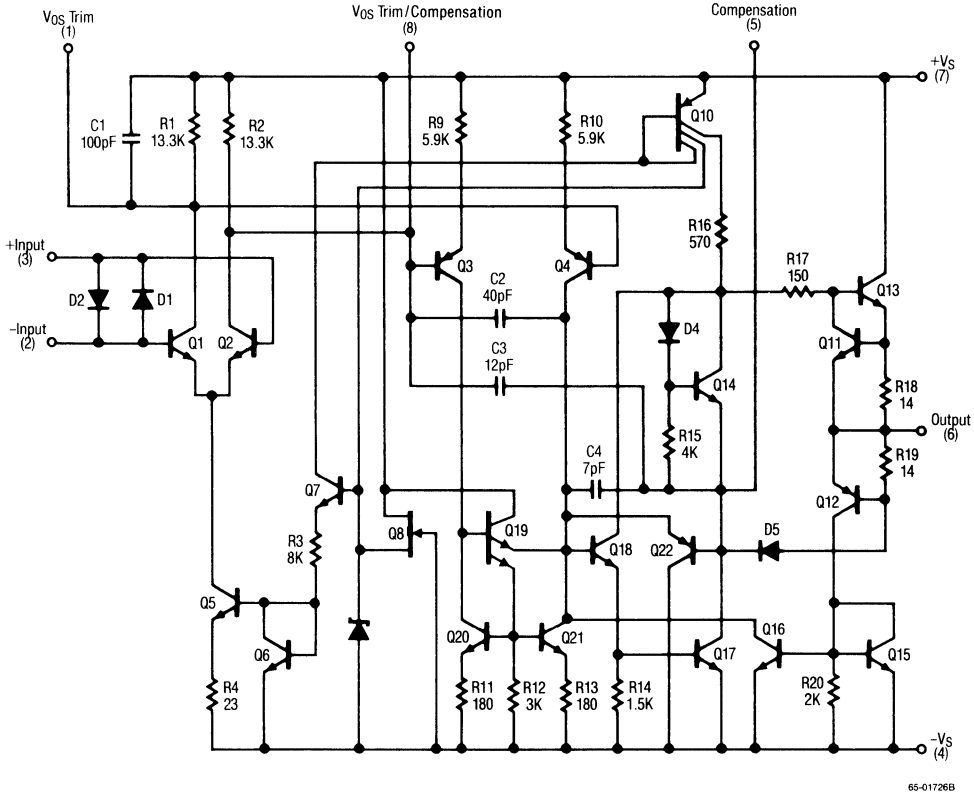
Total Harmonic Distortion vs. Output Voltage



Offset Voltage Adjust Circuit



Schematic Diagram



LF155/156/157 JFET-Input Operational Amplifiers

Features

All Devices

- Low input offset voltage — 0.3 mV
- High common mode rejection ratio — 100 dB
- Low input bias current — 30 pA
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Low input offset voltage drift — 3.0 µV/°C

LF155 Only

- Low supply current — 2.5 mA

LF156 Only

- High slew rate — 13 V/µS
- Wide gain bandwidth — 8 MHz
- Fast settling time to 0.01% — 4 µS

LF 157 Only

- High slew rate — 60 V/µS
- Wide bandwidth decompensated (A_{VCL} = 5 min) — 28 MHz
- Fast settling time — 4 µS

Description

The LF156 series of JFET-input operational amplifiers feature low input bias currents and high slew rate. They are direct replacements for the industry standard LF155/156/157 types (except that pin 8 is used for internal post-package V_{OS} trimming, so pin 8 cannot be used for PC board trace routing). Only military temperature range devices are available.

The LF155 is a general-purpose device having lower internal power dissipation than the other two versions, and a slew rate of 5 V/µS.

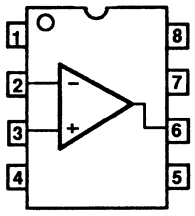
The LF156 has higher internal stage currents than the LF155, giving it a slew rate of 12 V/µS. The LF156, like the LF155, is compensated for ac stability in unity-gain applications.

The LF157 decompensated version is the fastest member of the series, with a 45 V/µS slew rate. The LF157 requires a minimum closed-loop gain configuration of +5 for ac stability.

Two accuracy grades are offered for each version; the "A" versions have tighter V_{OS}, I_B, and I_{OS} specifications. All types are offered in hermetic DIP, TO-99 can, and LCC packages, and can be ordered with Mil-Std-883, Level B processing.

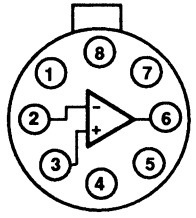
Connection Information

8-Lead
Dual In-Line Package
(Top View)



65-03206A

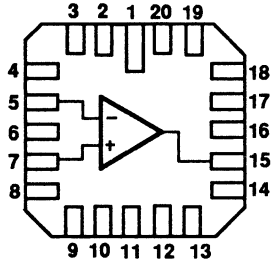
8-Lead
TO-99 Metal Can
(Top View)



65-03205A

Pin	Function
1	Bal
2	-In
3	+In
4	$-V_S$
5	Bal
6	Out
7	$+V_S$
8	Int. Trim*

20-Pad LCC
(Top View)



65-02657A

Pin	Function	Pin	Function
1	NC	11	NC
2	Bal	12	Bal
3	NC	13	NC
4	NC	14	NC
5	-In	15	Out
6	NC	16	NC
7	+In	17	$+V_S$
8	NC	18	NC
9	NC	19	NC
10	$-V_S$	20	Int. Trim*

*This pin has no user function, but is connected to an internal trim network.

Ordering Information

Part Number	Package	Operating Temperature Range
LF155AD	D	-55°C to +125°C
LF156AD	D	-55°C to +125°C
LF157AD	D	-55°C to +125°C
LF155D	D	-55°C to +125°C
LF156D	D	-55°C to +125°C
LF157D	D	-55°C to +125°C
LF155AT	T	-55°C to +125°C
LF156AT	T	-55°C to +125°C
LF157AT	T	-55°C to +125°C
LF155AL	L	-55°C to +125°C
LF156AL	L	-55°C to +125°C
LF157AL	L	-55°C to +125°C

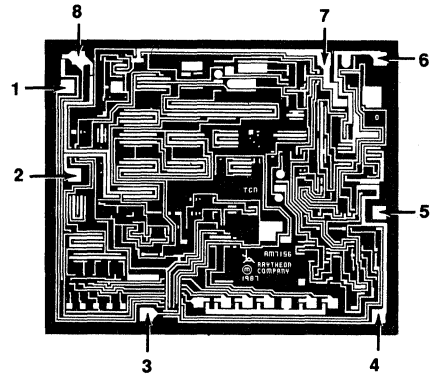
Notes:
Add /883B suffix to basic part number to specify Mil-Std-883, Level B processing.
L = 20-pad leadless chip carrier
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Differential Input Voltage Range ..... ±40V
Input Voltage Range* ..... ±20V
Output Short Circuit ..... Continuous
Operating Temperature
Range ..... -55°C to +125°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 sec) ..... +300°C

*For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.

Mask Pattern



Die Size: 87 x 105 mils 65-4240
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

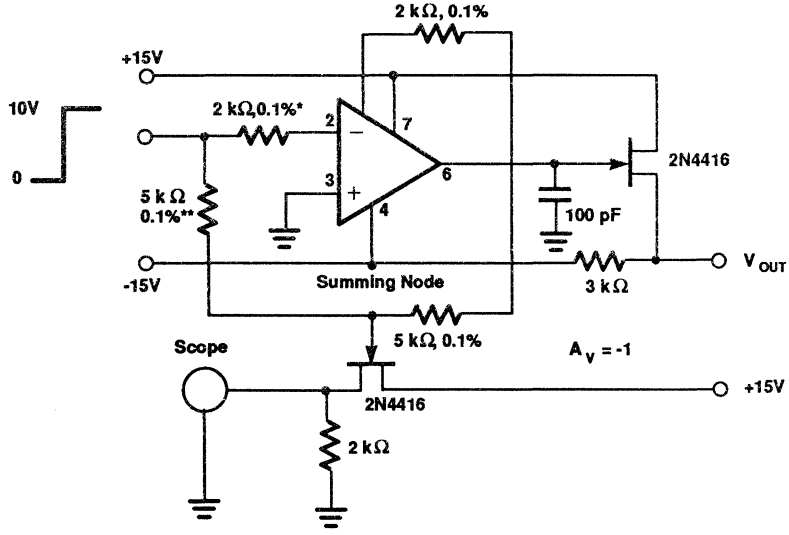
	8-Lead TO-99 Metal Can	8-Lead Ceramic DIP	20-Lead LCC Package
Max. Junction Temp.	175°C	175°C	175°C
Max. P_D T_A <50°C	658 mW	833 mW	925 mW
Therm. Res θ_{JC}	50°C/W	45°C/W	37°C/W
Therm. Res. θ_{JA}	190°C/W	150°C/W	105°C/W
For T_A >50°C Derate at	5.26 mW/°C	8.33 mW/°C	7.0 mW/°C

Electrical Characteristics ($\pm 15V \le V_S \le \pm 20V$, $T_A = +25°C$, unless otherwise noted)

Parameters	Test Conditions	LF155A/ 156A/157A Min	LF155A/ 156A/157A Typ	LF155A/ 156A/157A Max	LF155/ 156/157 Min	LF155/ 156/157 Typ	LF155/ 156/157 Max	Units
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$		0.3	2.0		0.4	5.0	mV
V_{OS} Adjustment Range		8.0			8.0			mV
Input Offset Current	$V_{CM} = 0V$, $T_J = +25°C$		3	10		6	20	pA
Input Bias Current	$V_{CM} = 0V$, $T_J = +25°C$		30	50		30	100	pA
Input Resistance			10^{12}			10^{12}		Ω
Large-Signal Voltage Gain	$V_S = \pm 15V$, $R_L \ge 2\ k\Omega$, $V_O = \pm 10V$	50	200		50	200		V/mV
Output Voltage Swing	$R_L = 10\ k\Omega$, $V_S = \pm 15V$ $R_L = 2\ k\Omega$, $V_S = \pm 15V$	±12 ±10	±13.5 ±13.2		±12 ±10	±13.5 ±13.2		V V
Supply Current	$V_S = \pm 15V$ LF155 LF156/157		3.0 4.0	4.0 7.0		3.0 4.0	4.0 7.0	 mA mA
Slew Rate	$A_{VCL} = +1$, $V_S = \pm 15V$, LF155 $A_{VCL} = +1$, $V_S = \pm 15V$, LF156 $A_{VCL} = +5$, $V_S = \pm 15V$, LF157	3.0 10 40	6.0 13 60		2.0 7.5 30	6.0 13 60		V/µS V/µS V/µS
Gain Bandwidth Product	$A_{VCL} = +1$, $V_S = \pm 15V$, LF155 $A_{VCL} = +1$, $V_S = \pm 15V$, LF156 $A_{VCL} = +5$, $V_S = \pm 15V$, LF157		6.0 8.0 30			5.7 7.6 28		MHz MHz MHz
Settling Time	To 0.01%, LF155 To 0.01%, LF156 To 0.01%, LF157		4.5 3.8 3.8			4.5 3.8 3.8		µS µS µS
Input Voltage Range	$V_S = \pm 15V$	±10.5	+15.1 -12.0		±10.5	+15.1 -12.0		V
Common Mode Rejection Ratio	$V_{CM} = \pm 10.5$	85	100		85	100		dB
Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$	85	100		85	100		dB
Input Noise Voltage Density	$R_S = 100\Omega$, $V_S = \pm 15V$ $F_O = 100$ Hz, LF155 $F_O = 1000$ Hz		25 20			25 20		 nV/√Hz nV/√Hz
	$V_S = \pm 15V$ $F_O = 100$ Hz, LF156/157 $F_O = 1000$ Hz		15 12			15 12		 nV/√Hz nV/√Hz
Input Noise Current Density	$V_S = \pm 15V$ $F_O = 100$ Hz $F_O = 1000$ Hz		0.01 0.01			0.01 0.01		 pA/√Hz pA/√Hz
Input Capacitance			3			3		pF

Electrical Characteristics ($\pm 15V \le V_S \le \pm 20V$, $-55°C \le T_A \le +125°C$, unless otherwise noted)

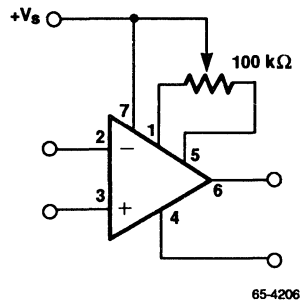
Parameters	Test Conditions	LF155A/ 156A/157A Min	Typ	Max	LF155/ 156/157 Min	Typ	Max	Units
Input Offset Voltage	$R_S = 50\Omega$, $V_{CM} = 0V$		0.5	2.5		1.0	7.0	mV
Average Input Offset Voltage Drift	Without external trim, $R_S = 50\Omega$ With external trim, $R_S = 50\Omega$		3.0 2.0	5.0		5.0 3.0		µV/°C µV/°C
Input Offset Current	$T_J = +125°C$, $V_{CM} = 0V$		0.6	10		0.8	20	nA
Input Bias Current	$T_J = +125°C$, $V_{CM} = 0V$		10	25		10	50	nA
Input Voltage Range	$V_S = \pm 15V$	±10.4	+15.1 -12.0		±10.4	+15.1 -12.0		V
Common Mode Rejection Ratio	$V_S = \pm 15V$, $V_{CM} = \pm 10.4V$	85	100		85	100		dB
Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 20V$	85	100		85	100		dB
Large Signal Voltage Gain	$V_S = \pm 15V$, $R_L \ge 2k\Omega$, $V_O = \pm 10V$	25	200		25	150		V/mV
Output Voltage Swing	$R_L \ge 10\ k\Omega$, $V_S = \pm 15V$ $R_L \ge 2\ k\Omega$, $V_S = \pm 15V$	±12 ±10	±13.5 ±13.0		±12 ±10	±13.5 ±13.0		V V



* 400Ω ±0.1% for LM157A
** 1 kΩ ±0.1% for LM157A

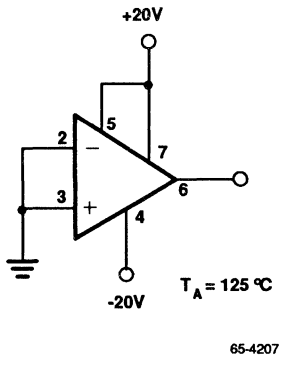
65-4205

Settling -Time Test Circuit



Note: For potentiometers with a temperature coeficient < 100 ppm/ °C, the added TCV_{OS} with nulling is ≈ 0.5 µV/°C /mV of adjustment

Input Offset Voltage Nulling



Burn-In Circuit

Applications Information

Input Voltage Considerations

The LF155/156/157 JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than $-V_S$ can result in a destroyed unit.

If both inputs exceed the negative common mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common mode voltage range.

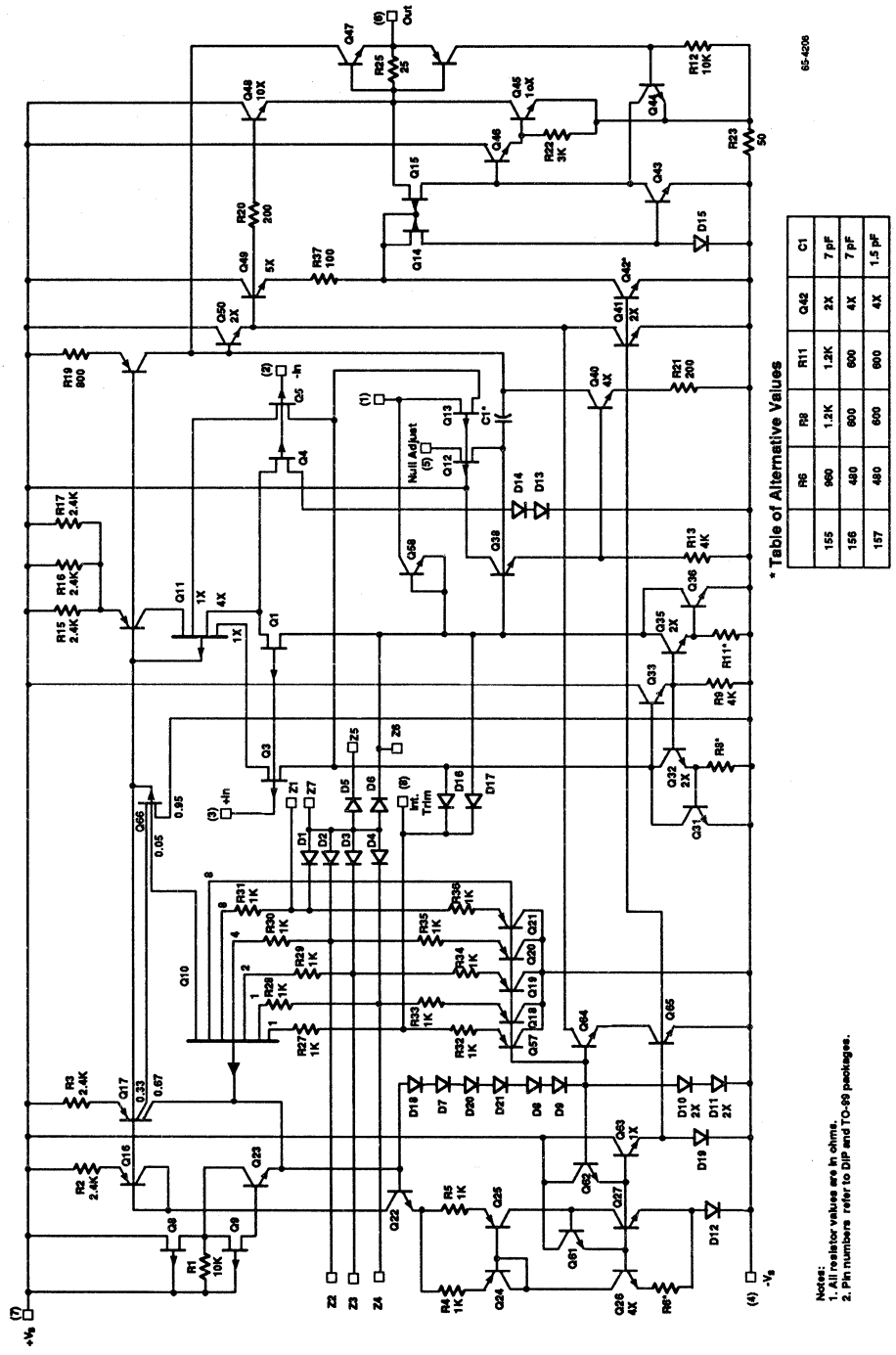
Exceeding the positive common mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

Dynamic Operation Considerations

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input. This minimizes "pick-up" and increases the frequency of the feedback pole by minimizing the capacitance from input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device to ac ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3 dB frequency of the closed-loop gain. Consequently, the pole has negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency, a lead capacitor should be placed from the output to the inverting input of the op amp. The capacitor value should be such that the RC time constant of the capacitor and feedback resistor is greater than, or equal to, the original feedback-pole time constant.

Schematic Diagram



	R6	R8	R11	Q42	C1
155	960	1.2K	1.2K	2X	7 pF
156	480	600	600	4X	7 pF
157	480	600	600	4X	1.5 pF

LM101A/ LH2101A General Purpose Operational Amplifier

Features

- Offset voltage 3.0 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Offsets guaranteed over entire common mode range and supply voltage range
- Frequency compensated 30 pF
- Supply voltage ±5.0V to ±20V

Description

The LM101A/LH2101A is a general purpose high performance operational amplifiers fabricated monolithically on a silicon chip by an advanced epitaxial process. The LH2101A consists of two LM101A ICs in one 16-lead DIP. The units may be fully compensated with the addition of a 30 pF capacitor stabilizing the circuit for all feedback configurations including capacitive loads.

The device may be operated as a comparator with a differential input as high as ±30V. Used as a comparator the output can be clamped at any desired level to make it compatible with logic circuits.

The LM101A and LH2101A operate over the full military temperature range from -55°C to +125°C.

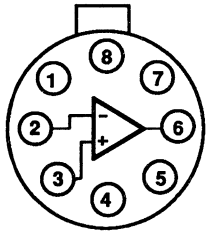
Ordering Information

Part Number	Package	Operating Temperature Range
LM101AD	D	-55°C to +125°C
LM101AD/883B	D	-55°C to +125°C
LM101AT	T	-55°C to +125°C
LM101AT/883B	T	-55°C to +125°C
LH2101D	D	-55°C to +125°C
LH2101D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 8-lead ceramic DIP (LM101 types)
D = 16-lead ceramic DIP (LH2101 types)
T = 8-lead metal can TO-99
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

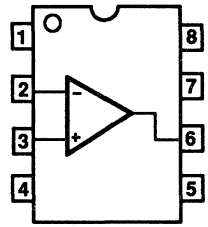
Connection Information

8-Lead TO-99 Metal Can
(Top View)



65-03205A

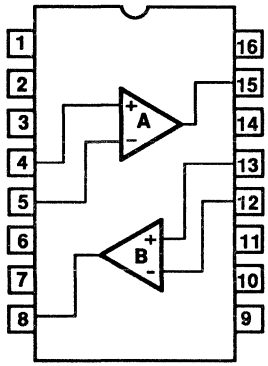
8-Lead Dual In-Line Package
(Top View)



65-0103

Pin	Function
1	Comp/V_{os} Trim
2	-Input
3	+Input
4	$-V_s$
5	V_{os} Trim
6	Output
7	$+V_s$
8	Comp

16-Lead Dual In-Line Package (Top View)



65-02658

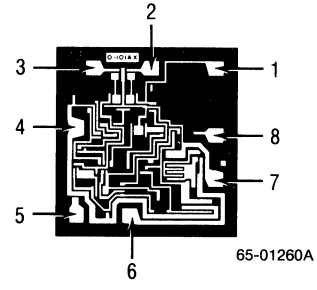
Pin	Function	Pin	Function
1	$+V_s$ (A)	9	$+V_s$ (B)
2	Comp (A)	10	Comp (B)
3	Comp (A)	11	Comp (B)
4	-Input (A)	12	-Input (B)
5	+Input (A)	13	+Input (B)
6	$-V_s$	14	Bal (A)
7	Bal (B)	15	NC
8	Output (B)	16	Output (A)

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Differential Input Voltage 30V
Input Voltage* ..... ±15V
Output Short-Circuit Duration** ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
LM101A, LH2101A ..... -55°C to +125°C
Lead Soldering Temperature
(60 sec) ..... +300°C

*For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Mask Pattern



Pin numbers are for 8-lead devices

Die Size: 55 x 55 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	16-Lead Ceramic DIP
Max. Junction Temp.	+175°C	+175°C	+175°C
Max. P_D T_A <50°C	833 mW	658 mW	1042 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	60°C/W
Therm. Res. θ_{JA}	150°C/W	190°C/W	120°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	8.33 mW/°C

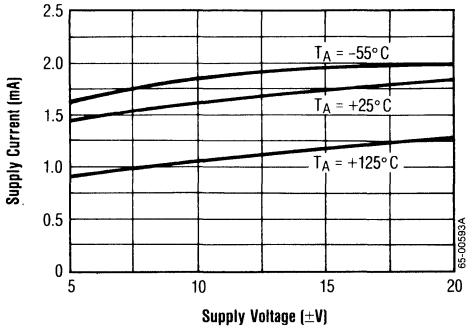
Electrical Characteristics

(C = 30 pF; ±5.0V ≤V_S ≤ ±20V; -55°C ≤ T_A ≤ +125°C unless otherwise specified)

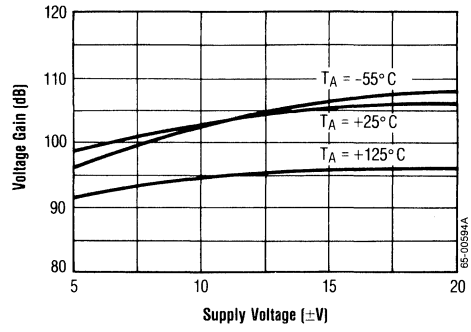
Parameters	Test Conditions	LM101A/LH2101A Min	Typ	Max	Units
Input Offset Voltage	T_A = +25°C, R_S ≤ 50 kΩ		0.7	2.0	mV
Input Offset Current	T_A = +25°C		1.5	10	nA
Input Bias Current	T_A = +25°C		30	75	nA
Input Resistance	T_A = +25°C	1.5	4.0		MΩ
Supply Current	T_A = +25°C (Note 2)		1.8	3.0	mA
Large Signal Voltage Gain	T_A = +25°C, V_S = ±15V V_{OUT} = ±10V, R_L ≥ 2 kΩ	50	160		V/mV
Input Offset Voltage	R_S ≤ 50 kΩ			3.0	mV
Average Input Offset Voltage Drift			3.0	15	µV/°C
Input Offset Current				20	nA
Average Input Offset Current Drift	+25°C ≤T_A ≤ +125°C		0.01	0.1	
	-55°C ≤ T_A ≤ +25°C		0.02	0.2	nA/°C
Input Bias Current				100	nA
Supply Current	T_A = +125°C, V_S = ±20V		1.2	2.5	mA
Large SignalVoltage Gain	V_S = ±15V V_{OUT} = ±10V, R_L ≥ 2 kΩ	25			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±14		V
	R_L ≥ 2 kΩ	±10	±13		
Input Voltage Range	V_S = ±20V	±15			V
Common Mode Rejection Ratio	R_S ≤ 50 kΩ	80	96		dB
Power Supply Rejection Ratio	R_S ≤ 50 kΩ	80	96		dB

Typical Performance Characteristics

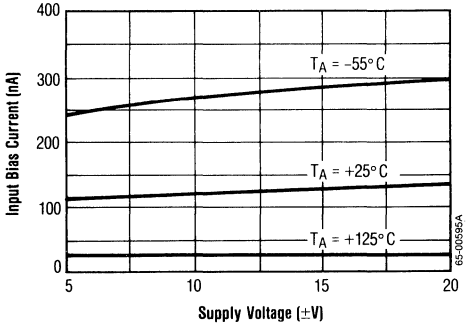
Supply Current



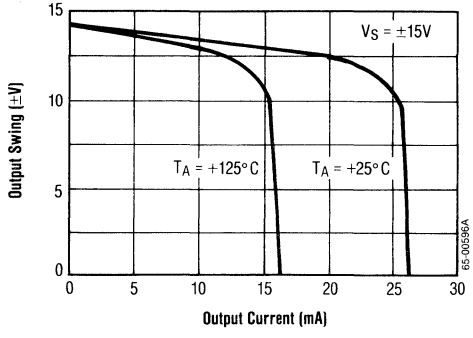
Voltage Gain



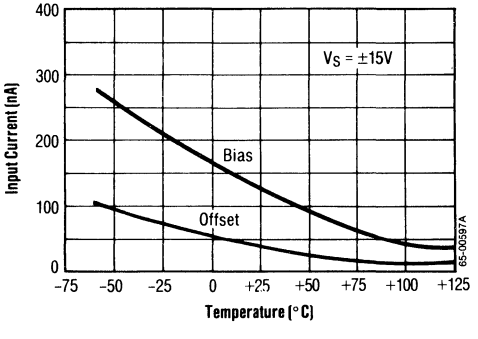
Input Bias Current



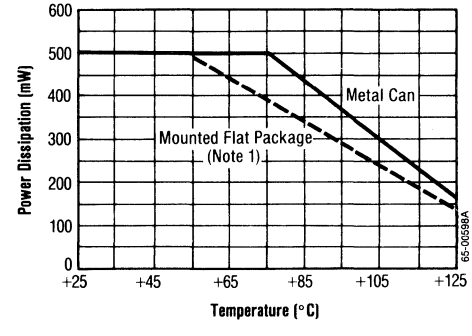
Current Limiting



Input Current

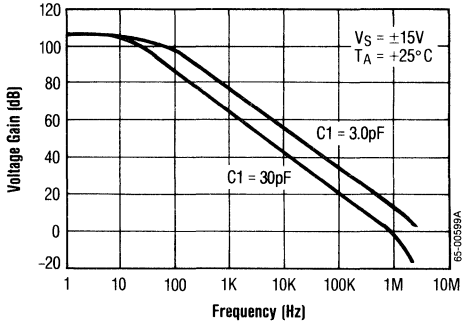


Maximum Power Dissipation

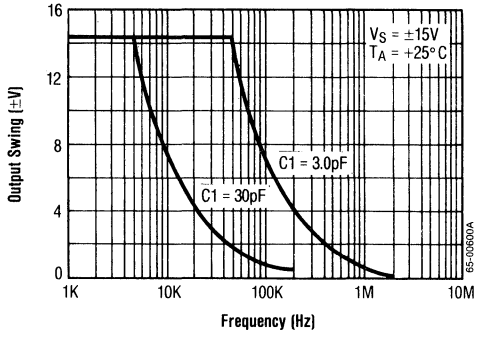


Typical Performance Characteristics (Continued)

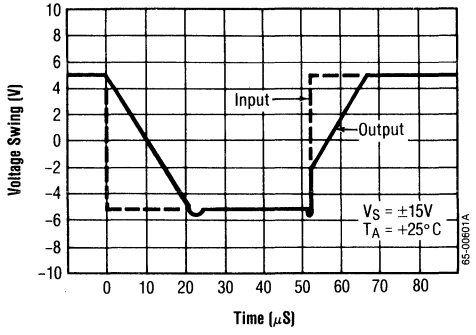
Open Loop Frequency Response



Large Signal Frequency Response

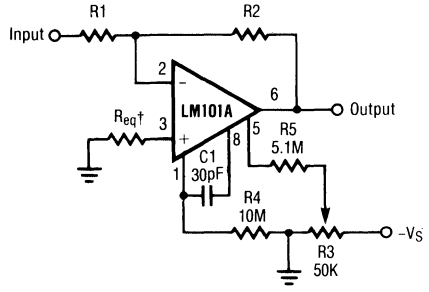


Voltage Follower Pulse Response



Typical Applications

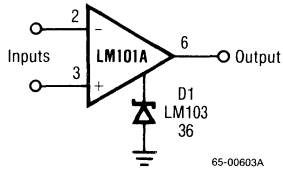
Inverting Amplifier With Balancing Circuit



†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

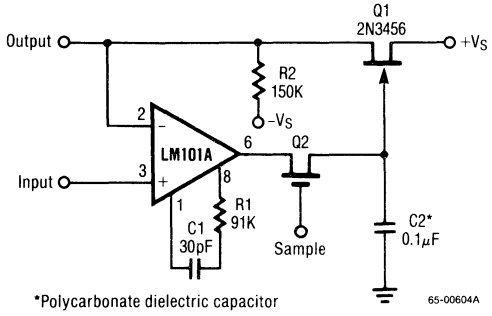
65-00602A

Voltage Comparator for Driving DTL or TTL Integrated Circuits



65-00603A

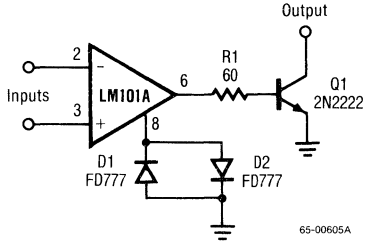
Low Drift Sample and Hold



*Polycarbonate dielectric capacitor

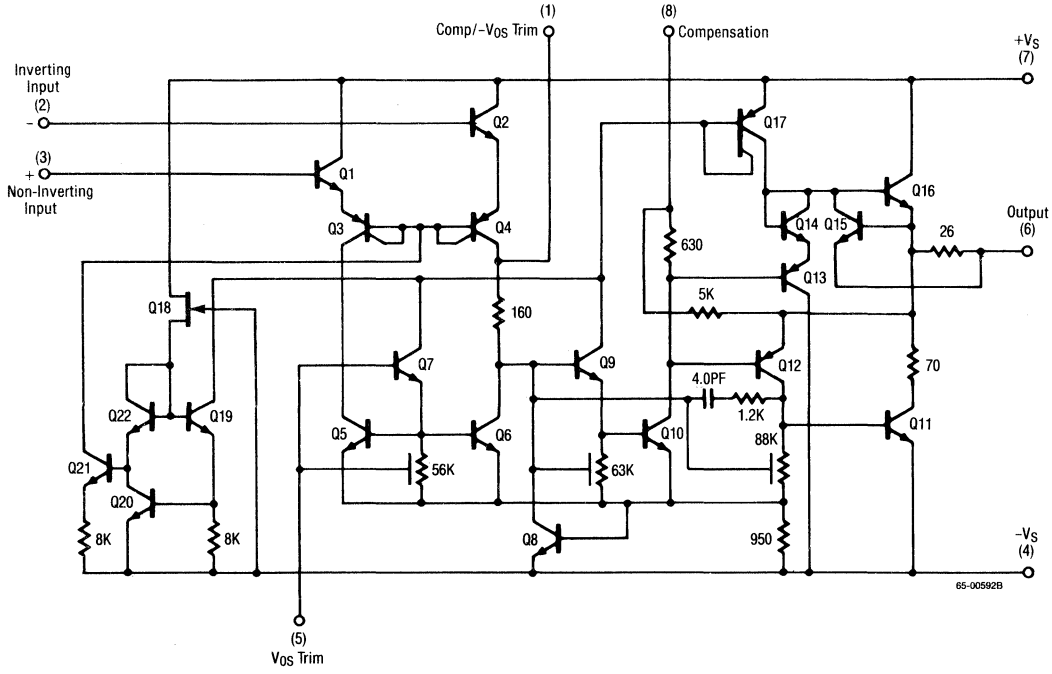
65-00604A

Voltage Comparator for Driving RTL Logic or High Current Driver



65-00605A

Schematic Diagram



LM124/324 Single-Supply Quad Operational Amplifiers

Features

- Large dc voltage gain — 100 dB
- Compatible with all forms of logic
- Temperature compensated
- Wide bandwidth at unity gain frequency — 1 MHz
- Large output voltage swing — 0V to $+V_S$ -1.5V
- Input common mode voltage range includes ground

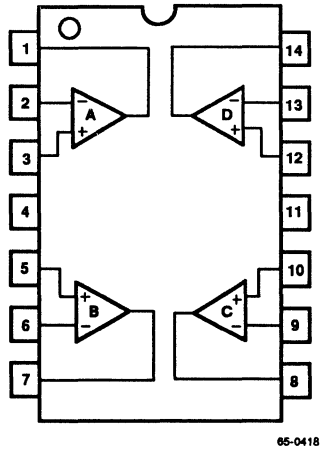
Description

Each of the devices in this series consists of four independent high-gain operational amplifiers that are designed for single-supply operation. Operation from split power supplies is also possible and the low power supply drain is independent of the magnitude of the power supply voltage.

Used with a dual supply, the circuit will operate over a wide range of supply voltages. However, a large amount of crossover distortion may occur with loads to ground. An external current-sinking resistor to $-V_S$ will reduce crossover distortion. There is no crossover distortion problem in single-supply operation if the load is direct-coupled to ground.

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-0418

Pin	Function	Pin	Function
1	Output (A)	8	Output (C)
2	-Input (A)	9	-Input (C)
3	+Input (A)	10	+Input (C)
4	$+V_S$	11	Ground
5	+Input (B)	12	+Input (D)
6	-Input (B)	13	-Input (D)
7	Output (B)	14	Output (D)

Ordering Information

Part Number	Package	Operating Temperature Range
LM324M	M	0°C to +70°C
LM324N	N	0°C to +70°C
LM124D	D	-55°C to +125°C
LM124D/883B*	D	-55°C to +125°C

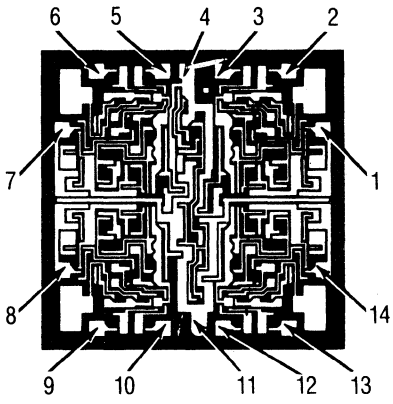
Notes:
*/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
M = 14-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage, $+V_S$ ..... +32V or ±16V
Differential Input Voltage 32V
Input Voltage ..... -0.3V to +32V
Output Short Circuit to Ground(1)
(One Amplifier) + $V_S \leq 15V$ and
$T_A = +25°C$ ..... Continuous
Input Current ($V_{IN} < -0.3V$)(2) ..... 50 mA
Operating Temperature Range
LM124 ..... -55°C to +125°C
LM324 ..... 0°C to +70°C

See Notes on next page.

Mask Pattern



Die Size: 78 x 80 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	14-Lead Small Outline SOIC	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	125°C	175°C
Max. P_D T_A <50°C	300 mW	468 mW	1042 mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

Electrical Characteristics ($+V_S = +5.0V$[3])

Parameters	Test Conditions	LM124 Min	LM124 Typ	LM124 Max	LM324 Min	LM324 Typ	LM324 Max	Units
Input Offset Voltage[4]	$T_A = +25°C$		±2.0	±5.0		±2.0	±7.0	mV
Input Bias Current[5]	$T_A = +25°C$		45	150		45	250	nA
Input Offset Current	$T_A = +25°C$		±3.0	±30		±5.0	±50	nA
Input Voltage Range[6]	$+V_S = +30V$, $T_A = +25°C$	0	$+V_S$ -1.5	0		$+V_S$ -1.5		V
Supply Current	$R_L = \infty$, $+V_S = 30V$		1.5	3.0		1.5	3.0	mA
	$R_L = \infty$ on all op amps		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	$+V_S = 15V$ (for large V_O swing) $R_L \geq 2\ k\Omega$, $T_A = +25°C$	50	100		25	100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = +25°C$	0		$+V_S$ -1.5	0		$+V_S$ -1.5	V
Common Mode Rejection Ratio	$T_A = +25°C$	70	85		65	70		dB
Power Supply Rejection Ratio	$T_A = +25°C$	65	100		65	100		dB
Channel Separation[7]	f = 1 kHz to 20 kHz $T_A = +25°C$ (input referred)		-120`			-120		dB
Output Current								
Source	$V_{IN+} = 1V$, $V_{IN-} = 0V$, $+V_S = 15V$, $T_A = +25°C$	20	40		20	40		mA
Sink	$V_{IN-} = 1V$, $V_{IN+} = 0V$, $+V_S = 15V$, $T_A = +25°C$	10	20		10	20		mA
	$V_{IN-} = 1V$, $V_{IN+} = 0V$, $T_A = +25°C$, $V_O = 200\ mV$	12	50		12	50		µA

Notes:
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns to a value greater than -0.3V.
3. These specifications apply for $+V_S = +5V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. Specifications are limited to $-25°C \leq T_A \leq +85°C$; the LM324 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
4. $V_O \cong 1.4V$, $R_S = 0\Omega$ with $+V_S$ from 5V to 30V; and over the full common mode range (0V to $+V_S$ -1.5V).
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
6. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage.
7. Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Electrical Characteristics ($+V_S = +5.0V$[3])

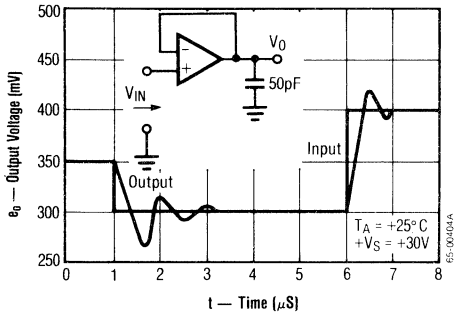
Parameters	Test Conditions	LM124			LM324			Units
		Min	Typ	Max	Min	Typ	Max	
Short Circuit Current[1]	$T_A = +25°C$		40	60		40	60	mA
Input Offset Voltage [4]				±7.0			±9.0	mV
Input Offset Voltage Drift	$R_S = 0\Omega$		7.0			7.0		µV/°C
Input Offset Current				±100			±150	nA
Input Offset Current Drift			10			10		pA/°C
Input Bias Current			40	300		40	500	nA
Input Voltage Range[6]	$+V_S = +30V$	0		$+V_S$ 2.0	0		$+V_S$ -2.0	V
Large Signal Voltage Gain	$+V_S = +15V$ (For Large V_O Swing) $R_L \geq 2.0\ k\Omega$	25			15			V/mV
Output Voltage Swing								
V_{OH}	$+V_S = +30V$, $R_L\ \Omega$	26			26			V
V_{OH}	$R_L \geq 10\ k\Omega$	27	28		27	28		V
V_{OL}	$+V_S = +5.0V$, $R_L = 10\ k\Omega$		5.0	20		5.0	20	mV
Output Current								
Source	$V_{IN+} = +1.0V$, $V_{IN-} = 0V$, $+V_S = +15V$	10	20		10	20		mA
Sink	$V_{IN-} = +1.0V$, $V_{IN+} = 0V$, $+V_S = +15V$	5.0	8.0		5.0	8.0		mA
Differential Input Voltage[6]				$+V_S$			$+V_S$	V

Notes:

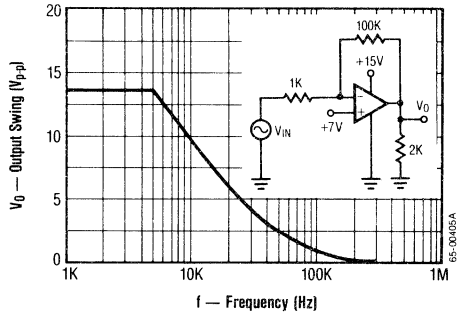
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of $+V_S$. At values of supply voltage in excess of $+V_S$, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns to a value greater than -0.3V.
3. These specifications apply for $+V_S = +5V$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. The LM324 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
4. $V_O = 1.4V$, $R_S = 0\Omega$ with $+V_S$ from 5V to 30V; and over the full common mode range (0V to $+V_S$ -1.5V).
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
6. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +32V without damage.
7. Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Typical Performance Characteristics

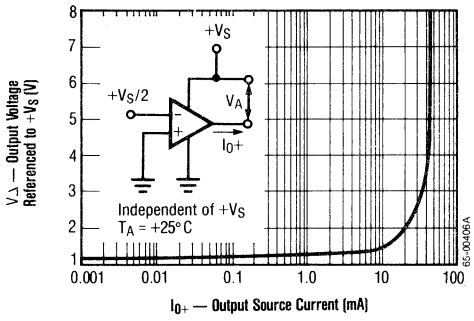
Voltage Follower Pulse Response (Small Signal)



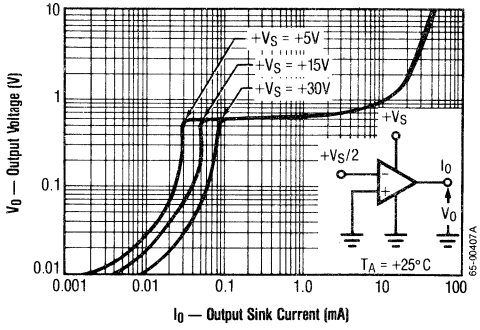
Large Signal Frequency Response



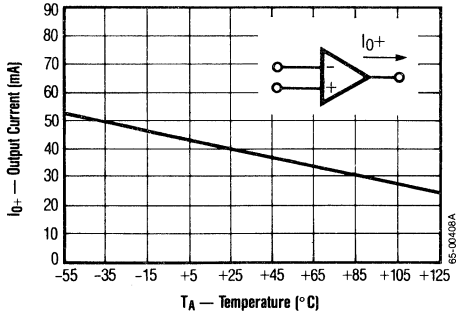
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

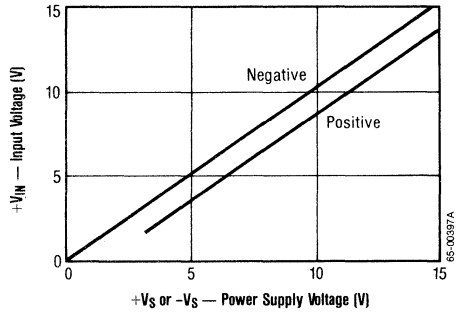


Current Limiting

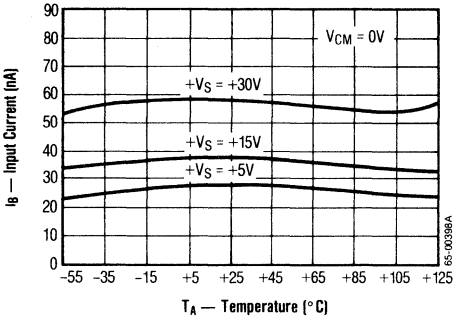


Typical Performance Characteristics (Continued)

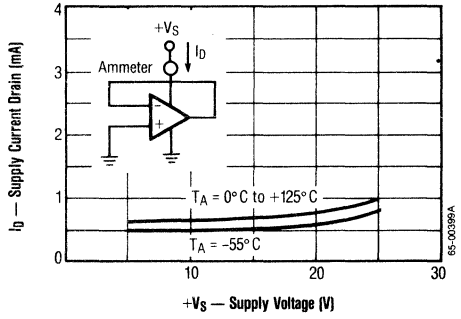
Input Voltage Range



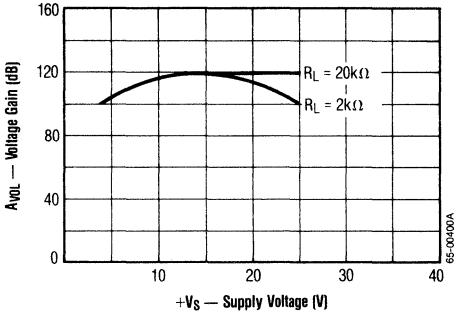
Input Current



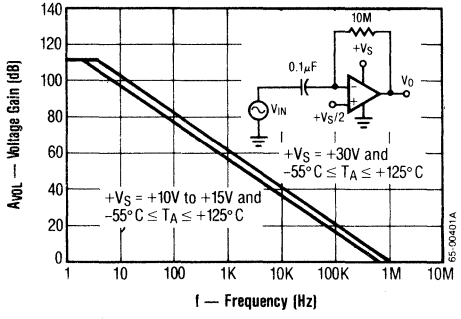
Supply Current



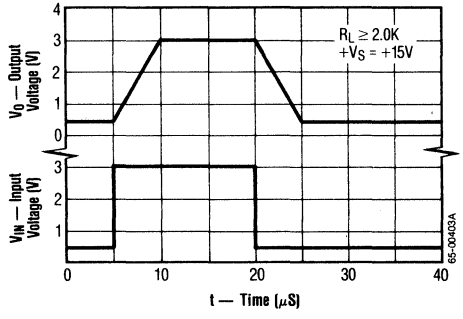
Voltage Gain



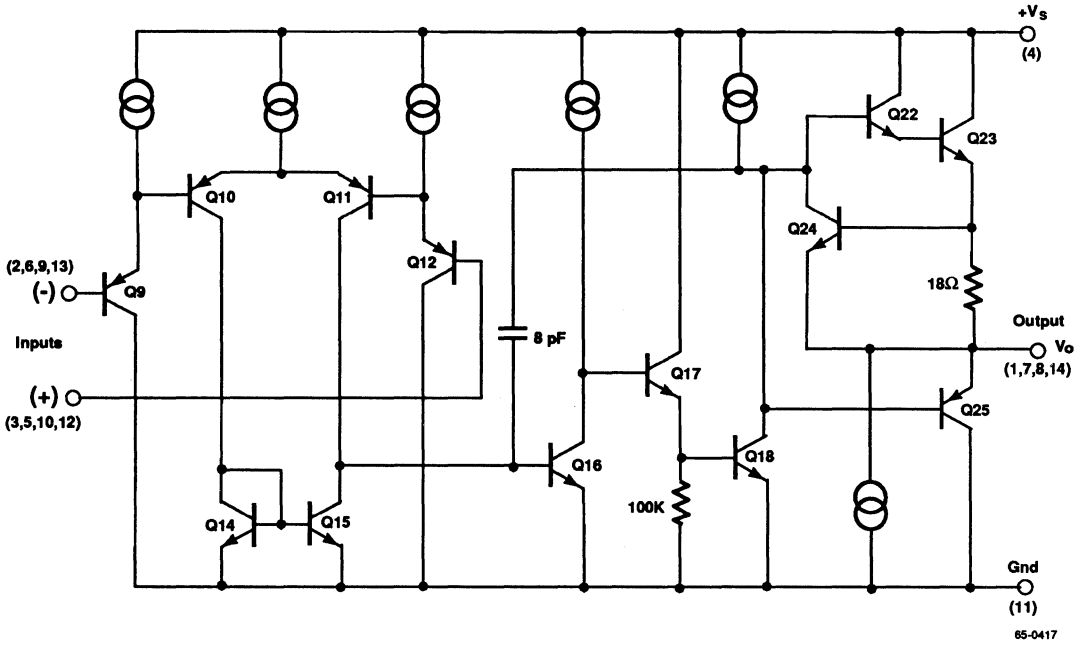
Open Loop Frequency Response



Voltage Follower Pulse Response



Schematic Diagram



LM148/348 Low Power Quad 741 Operational Amplifier

Features

- 741 op amp operating characteristics
- Low supply current drain — 0.6 mA/amplifier
- Class AB output stage — no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage — 1.0 mV
- Low input offset current — 4.0 nA
- Low input bias current — 30 nA
- Gain bandwidth product — LM148 (unity gain) 1.0 MHz
- High degree of isolation between amplifiers — 120 dB
- Overload protection for inputs and outputs

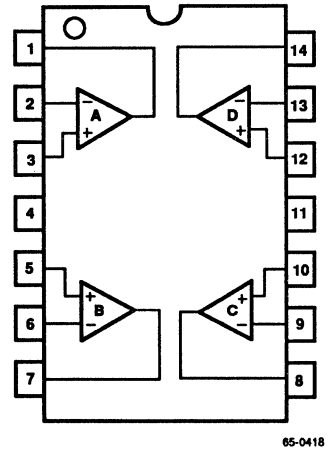
Description

The LM148 series is a true quad 741. It consists of four independent high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias currents which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-0418

Pin	Function	Pin	Function
1	Output (A)	8	Output (C)
2	-Input (A)	9	-Input (C)
3	+Input (A)	10	+Input (C)
4	$+V_S$	11	$-V_S$
5	+Input (B)	12	+Input (D)
6	-Input (B)	13	-Input (D)
7	Output (B)	14	Output (D)

Ordering Information

Part Number	Package	Operating Temperature Range
LM348N	N	0°C to +70°C
LM148D	D	-55°C to +125°C
LM148D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage
- LM148 ..... ±22V
- LM348 ..... ±18V

Differential Input Voltage
- LM148 ..... 22V
- LM348 ..... 36V

Input Voltage
- LM148 ..... ±22V
- LM348 ..... ±18V

Output Short Circuit Duration* ..... Indefinite

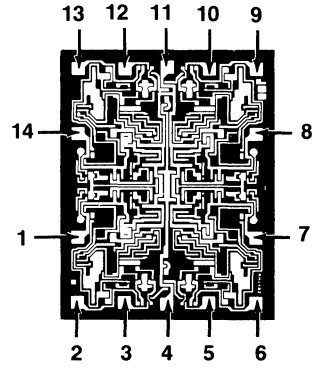
Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- LM148 ..... -55°C to +125°C
- LM348 ..... 0°C to +70°C

Lead Soldering Temperature (60 sec) ..... +300°C

*For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage. Short circuit to ground on one amplifier only.

Mask Pattern



65-03697A

Die Size: 84 x 67 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

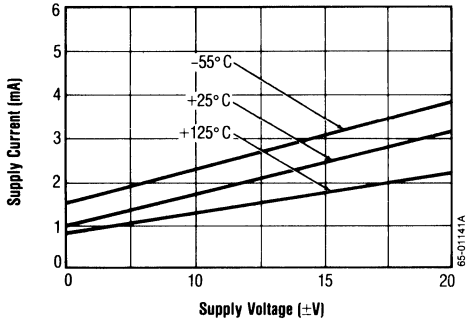
	14-Lead Plasticc DIP	14-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A <50°C	468 mW	1042 mW
Therm. Res θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A >50°C Derate at	6.25 mW per °C	8.38 mW per °C

Electrical Characteristics (V_S = ±15V and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise specified)

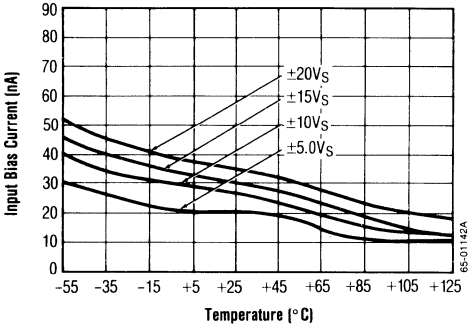
Parameters	Test Conditions	LM148			LM348			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = +25°C, R_S ≤10 kΩ		1.0	5.0		1.0	6.0	mV
Input Offset Current	T_A = +25°C		4.0	25		4.0	50	nA
Input Bias Current	T_A = +25°C		30	100		30	200	nA
Input Resistance (Differential Mode)	T_A = +25°C	0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	T_A = +25°C, V_S = ±15V		2.4	3.6		2.4	4.5	mA
Large Signal Voltage Gain	T_A = +25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \ge$ 2 kΩ	50	160		25	160		V/mV
Channel Separation	T_A = +25°C, f = 1 Hz to 20 kHz		120			120		dB
Unity Gain Bandwidth	T_A = +25°C		1.0			1.0		MHz
Phase Margin	T_A = +25°C		60			60		Degrees
Slew Rate	T_A = +25°C		0.5			0.5		V/μS
Short Circuit Current	T_A = +25°C		25			25		mA
Input Offset Voltage	$R_S \le$ 10 kΩ			6.0			7.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L >2 kΩ	25			15			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		±12	±13		V
	R_L = 2 kΩ	±10	±12		±10	±12		V
Input Voltage Range	V_S = ±15V	±12			±12			V
Common Mode Rejection Ratio	$R_S \le$ 10 kΩ	70	90		70	90		dB
Power Supply Rejection Ratio	$R_S \le$ 10 kΩ	77	96		77	96		dB

Typical Performance Characteristics

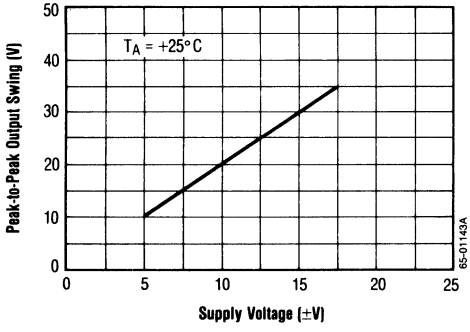
Supply Current vs. Supply Voltage



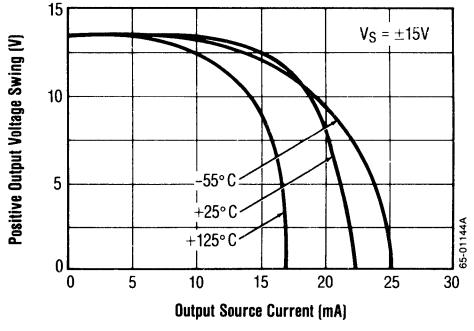
Input Bias Current vs. Temperature



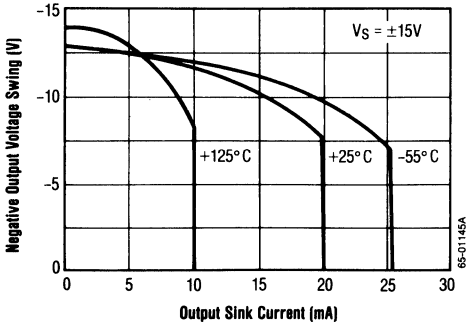
Voltage Swing vs. Supply Voltage



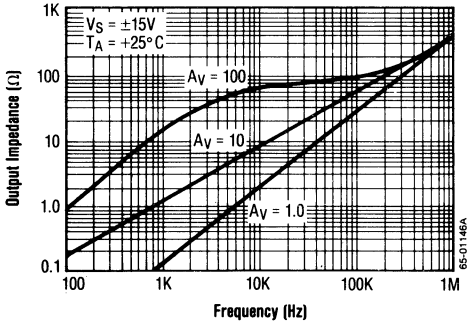
Positive Current Limit



Negative Current Limit

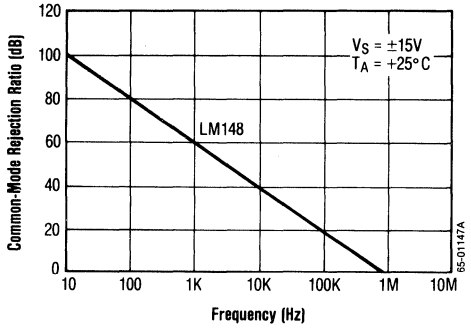


Output Impedance vs. Frequency

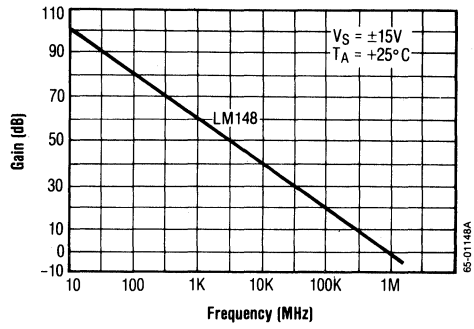


Typical Performance Characteristics (Continued)

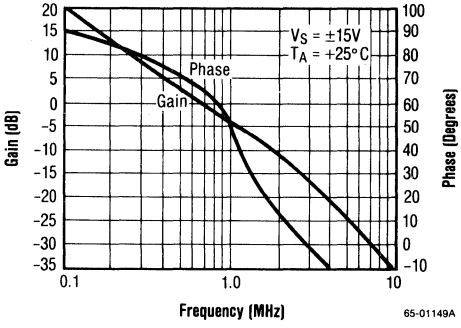
Common Mode Rejection Ratio vs. Frequency



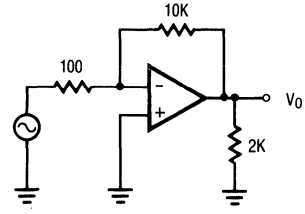
Open Loop Frequency Response



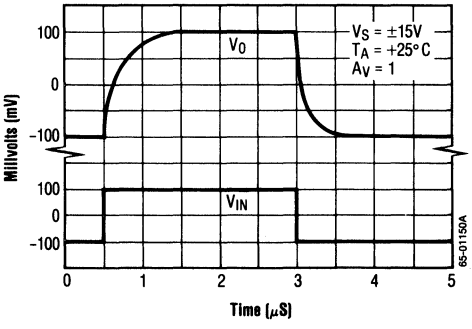
Phase Margin vs. Frequency



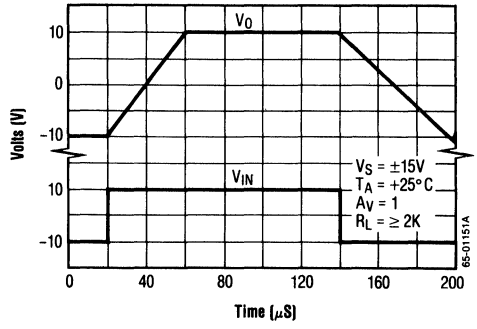
Test Circuit



Small Signal Pulse Response

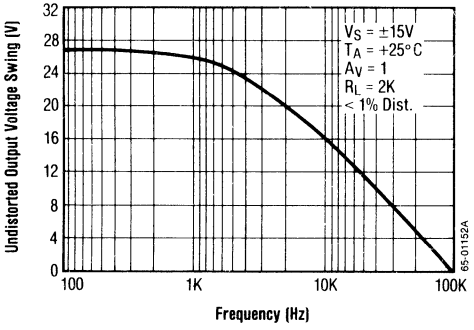


Large Signal Pulse Response

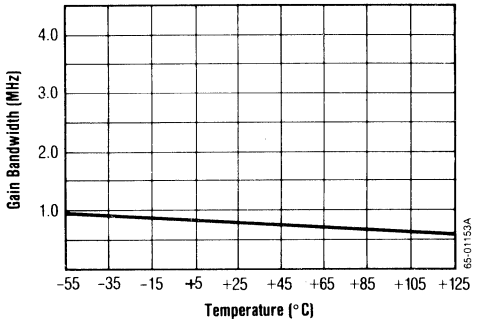


Typical Performance Characteristics (Continued)

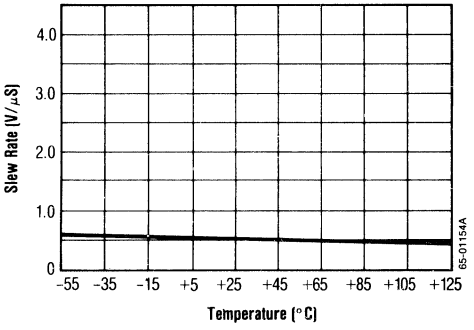
Undistorted Output Voltage Swing vs. Frequency



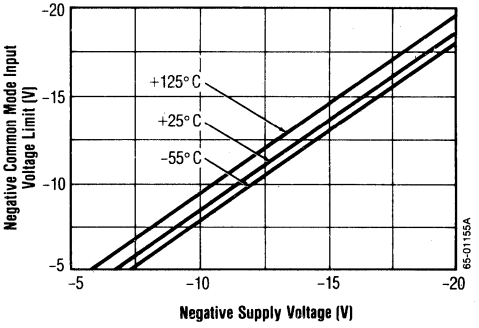
Gain Bandwidth vs. Temperature



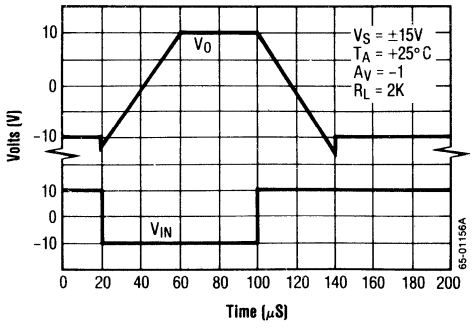
Slew Rate vs. Temperature



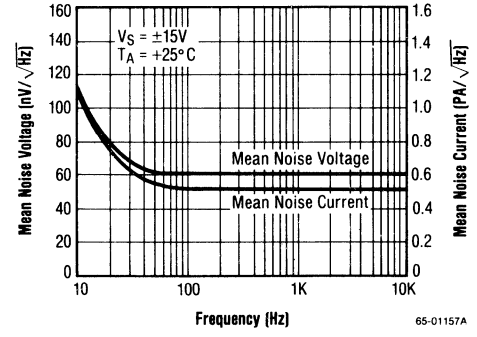
Negative Common Mode Input Voltage Limit



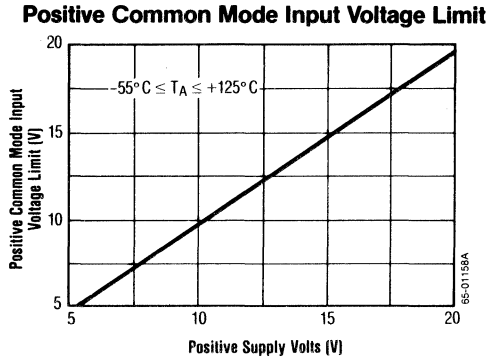
Inverting Large Signal Pulse Response



Input Noise Voltage and Noise Current



Typical Performance Characteristics (Continued)



Typical Simulation

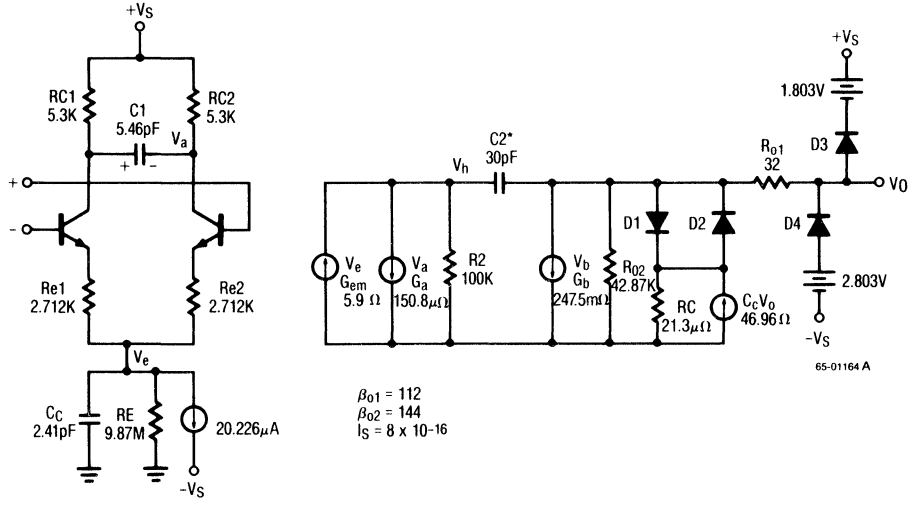


Figure 1. LM148 Macromodel for Computer Simulation

Typical Applications

The 148 series are low power quad operational amplifiers that exhibit performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

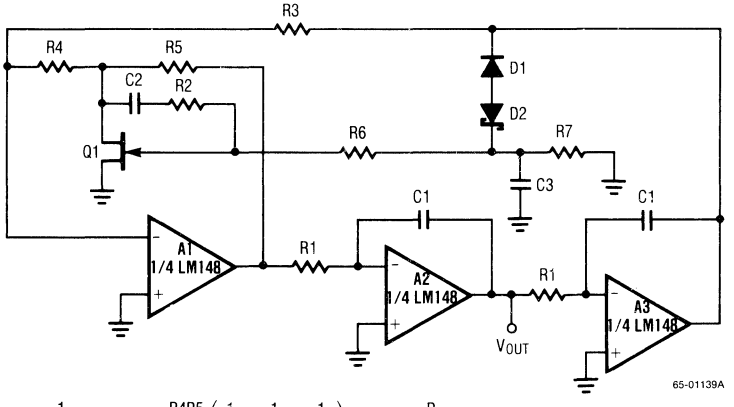
The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs are within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

When capacitive loading becomes much greater than 100pF, a resistor should be placed between the output and feedback connection in order to reduce phase shift.

The 148 series is short circuit protected to either ground or the supplies continuously when only one of the four amplifiers are shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability and to minimize pickup, feedback resistors should be placed close to the input to maximize the feedback pole frequency (a function of input to ground capacitance). A good rule of thumb is that the feedback pole frequency should be 6 times the operating -3.0dB frequency. If less, a lead capacitor should be placed between the output and input.

Typical Applications

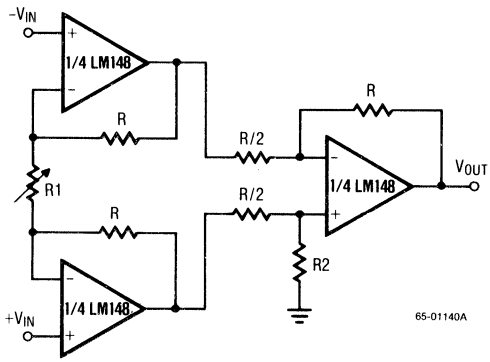


$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\ r_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

f_{MAX} = 5.0kHz, THD ≤ 0.03%
R1 = 100K pot., C1 = 0.0047μF, C2 = 0.01μF, C3 = 0.1μF, R2 = R6 = R7 = 1M, R3 = 5.1K, R4 = 12Ω, R5 = 240Ω, Q1 = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

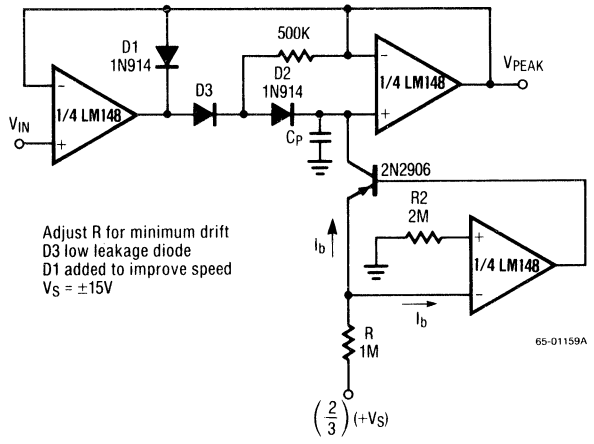
Figure 2. One Decade Low Distortion Sinewave Generator

Typical Applications (Continued)



$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right)$, $-V_S - 3V \leq V_{IN\ CM} \leq +V_S - 3V$,
$V_S = \pm 15V$
R = R2, trim R2 to boost CMRR

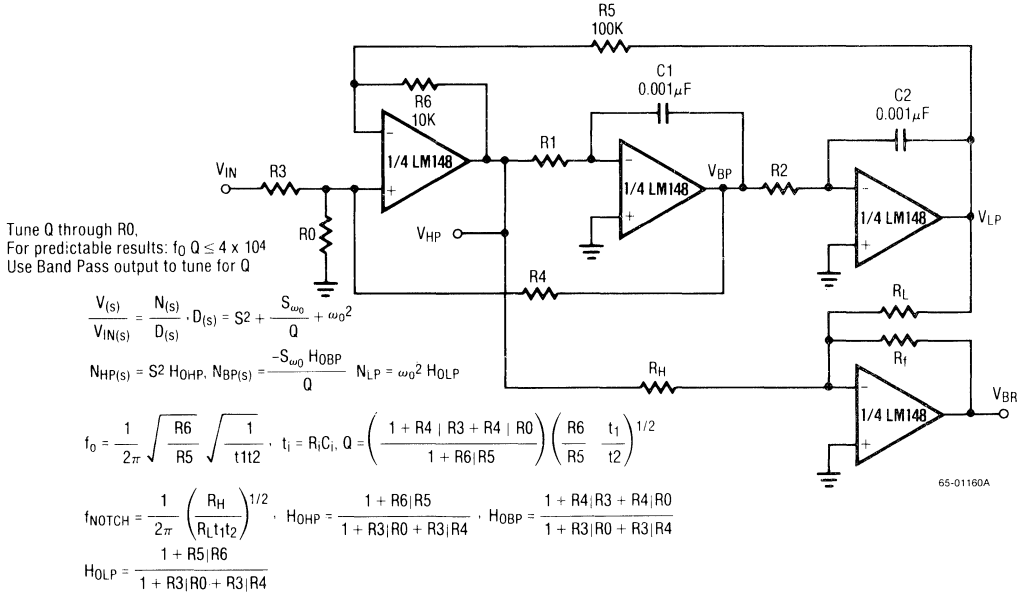
Figure 3. Low Cost Instrumentation Amplifier



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

Figure 4. Low Voltage Peak Detector With Bias Current Compensation

Typical Applications (Continued)



Tune Q through R0.
For predictable results: $f_0\ Q \leq 4 \times 10^4$
Use Band Pass output to tune for Q

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N_{(s)}}{D_{(s)}},\ D_{(s)} = S^2 + \frac{S_{\omega_0}}{Q} + \omega_0^2$$

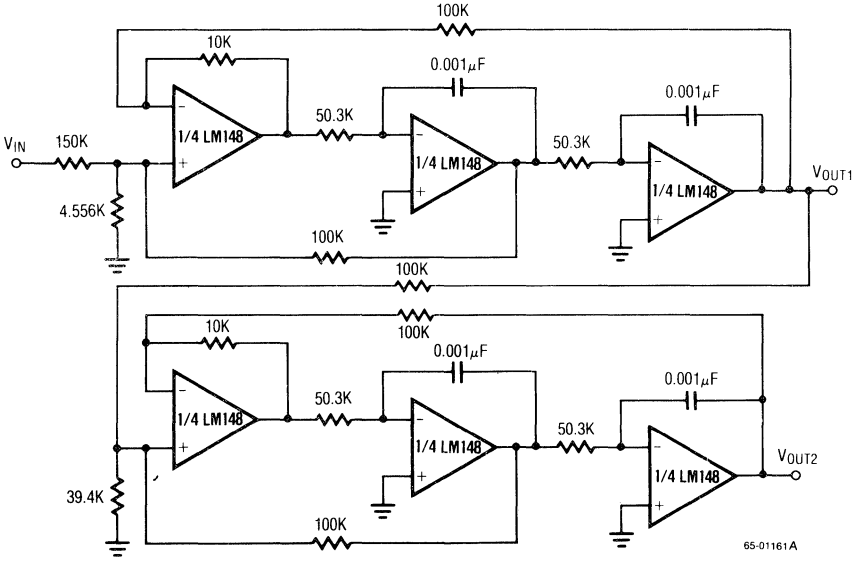
$$N_{HP(s)} = S^2\ H_{OHP},\ N_{BP(s)} = \frac{-S_{\omega_0}\ H_{OBP}}{Q}\quad N_{LP} = \omega_0^2\ H_{OLP}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4\,|\,R3 + R4\,|\,R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\ \frac{t_1}{t2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_Lt_1t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

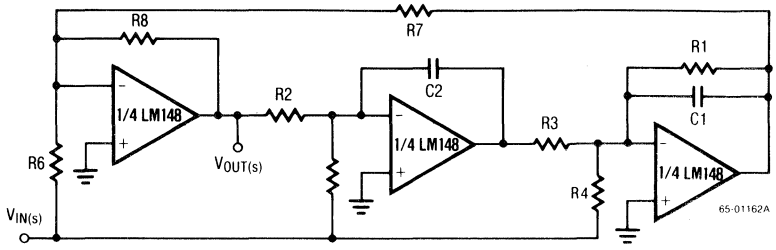
Figure 5. Universal State-Space Filter



Use general equations, and tune each section separately
$Q_{1st\ Section} = 0.541$, $Q_{2nd\ Section} = 1.306$
The response should have 0dB peaking

Figure 6. 1 kHz 4-Pole Butterworth Filter

Typical Applications (Continued)



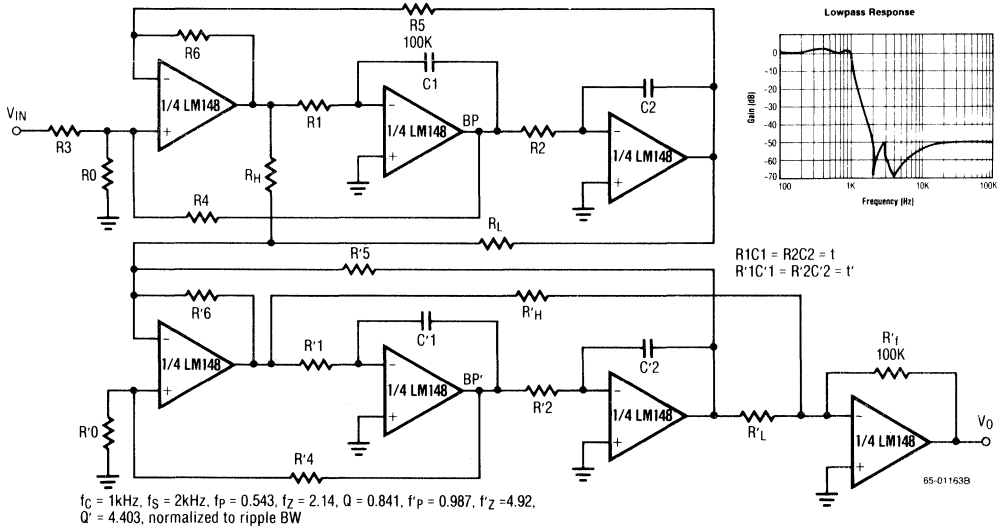
$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}},\ f_0 = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}},\ f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3kHz, Q = 5, R1 = 270K, R2 = R3 =20K, R4 = 27K, R5 = 20K, R6 = R8 = 10K, R7 = 100K, C1 = C2 = 0.001μF

Better noise performance than the state-space approach

Figure 7. 3 Amplifier Bi-Quad Notch Filter



f_C = 1kHz, f_S = 2kHz, f_P = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z =4.92, Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t},\ f_Z = \frac{1}{2\pi} \cdot \sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \frac{1 + R4|R3 + R4|R0}{1 + R6|R5} \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R'5}}\ \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

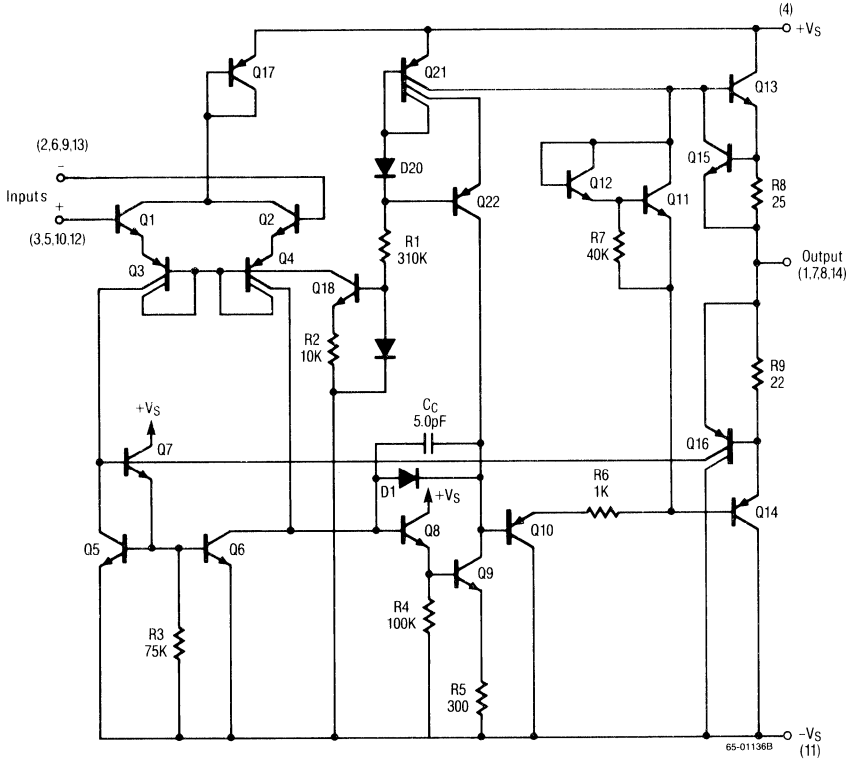
Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6K, R3 = R4 = R5 = 100K, R6 = 10K, R0 = 107.8K, R_L = 100K, R_H =155.1K,
R'1 = R'2 = 50.9K, R'4 = R'5 = 100K, R'6 = 10K, R'0 = 5.78K, R'_L = 100K, R'_H = 248.12K, R'_f = 100K.

All capacitors are 0.001μF

Figure 8. 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)

Schematic Diagram (1/4 Shown)



LM2900/3900 Current Mode Single Supply Quad Operational Amplifier

Features

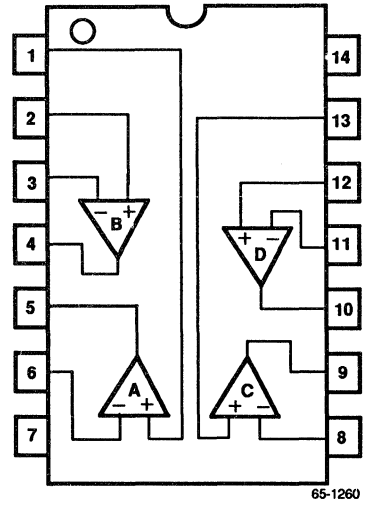
- Wide single supply voltage range — 4.0V to 36V
- Supply current drain independent of supply voltage
- Low input biasing current — 30 nA
- High open-loop gain — 70 dB
- Wide bandwidth — 2.5 MHz (unity gain)
- Larger gain-bandwidth product in non-inverting mode (A_V = 100 at f = 1.0 MHz)
- Large output voltage swing (V_S -1.0) V_{P-P}
- Internally frequency compensated for unity gain
- Output short-circuit protection

Description

The LM2900 and LM3900 consist of four independent, dual input, internally compensated amplifiers designed specifically to operate off a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: AC amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

Connection Information

14-Lead Dual In-Line Package
(Top View)



65-1260

Pin	Function	Pin	Function
1	+Input (A)	8	-Input (C)
2	+Input (B)	9	Output (C)
3	-Input (B)	10	Output (D)
4	Output (B)	11	-Input (D)
5	Output (A)	12	+Input (D)
6	-Input (A)	13	+Input (C)
7	Ground	14	$+V_S$

Ordering Information

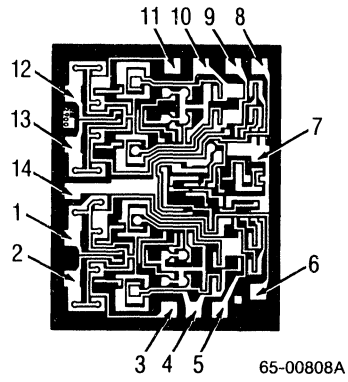
Part Number	Package	Operating Temperature Range
LM3900N	N	0°C to +70°C
LM2900N	N	-25°C to +85°C

Notes:
N = 14-lead plastic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage
LM2900 ..... +36V
LM3900 ..... +32V
Supply Voltage ..... ±18V
Input Currents, I_{IN+} or I_{IN-} ..... 20 mA
Output Short Circuit Duration ..... Continuous
One Amplifier, T_A = +25°C
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
LM2900 ..... -25°C to +85°C
LM3900 ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Mask Pattern



Die Size: 56 x 70 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	14-Lead Plastic DIP
Max. Junc. Temp.	+125°C
Max. P_D T_A < 50°C	468 mW
Therm. Res. θ_{JC}	—
Therm. Res. θ_{JA}	160°C/W
For T_A > 50°C Derate at	6.25 mW/°C

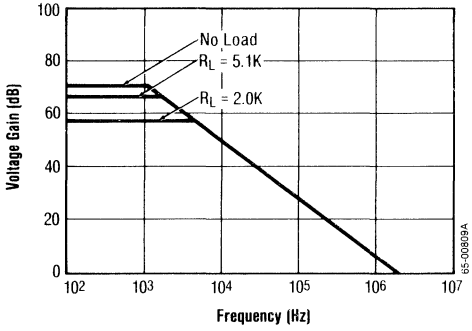
Electrical Characteristics (V_S = +15V and T_A = +25° C unless otherwise noted)

Parameter	Test Conditions	LM2900/3900 Min	Typ	Max	Units
Large Signal Voltage Gain	f = 100Hz	1200	2800		V/V
Input Resistance (Differential Mode)	Inverting Input		1.0		MΩ
Output Resistance			8.0		kΩ
Unity Gain Bandwidth[1]	Inverting Input		2.5		MHz
Input Bias Current	Inverting Input		30	200	nA
Slew Rate	Positive Output Swing		0.5		V/μS
	Negative Output Swing		20		
Supply Current	R_L = ∞ On All Amplifiers		6.2	10	mA
Output Voltage Swing V_{OUT} High	R_L = 2k I_{IN-} = 0, I_{IN+} = 0	13.5	14.2		V
V_{OUT} Low	I_{IN-} = 10μA, I_{IN+} = 0		0.09	0.2	V
Output Current	Source	6.0	18		mA
	Sink[2]	0.5	1.3		
Power Supply Rejection Ratio	f = 100Hz		70		dB
Mirror Gain[3]	I_{IN+} = 200μA	0.90	1.0	1.1	μA/μA
Mirror Current[4]			10	500	μA
Negative Input Current[5]			1.0		mA

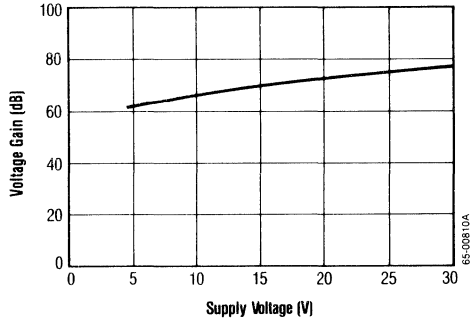
Notes:
1. When used as a "non-inverting amplifier", the gain-bandwidth product is not limited to 2.5MHz. The isolation provided by the "current mirror" allows a constant unity voltage gain feedback for the main inverting amplifier. This means that large values of gain can be achieved at high frequencies and the dominant limit is due to the slew rate of the amplifier. For example: a voltage gain of 100 is easily obtained at 1MHz and an output voltage swing of 160mV_{p-p} can be achieved prior to slew rate limiting. This operational mode is useful for signal frequencies in the 50kHz to 1MHz range as would be encountered in IF or carrier frequency applications.
2. The output current sink capability can be increased for large signal conditions by overdriving the inverting input.
3. This spec indicates the current gain of the current mirror which is used as the non-inverting input.
4. Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror-current (non-inverting input current) of approximately 10μA. This is therefore a typical design center for many of the application circuits.
5. Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately -0.3V. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1.0mA. Negative input currents in excess of 4.0mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven, negative smaller maximum currents are allowed. Common mode current biasing can be used to prevent negative input voltages; for example, see the "Differentiator Circuit" in the applications section.

Typical Performance Characteristics

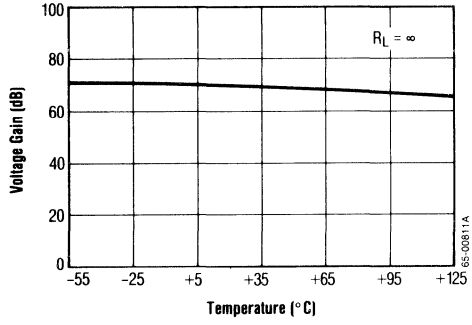
Open Loop Gain



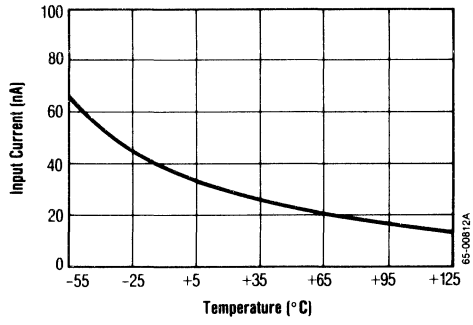
Voltage Gain vs. Supply Voltage



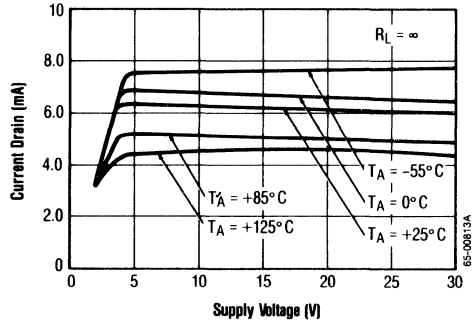
Voltage Gain vs. Temperature



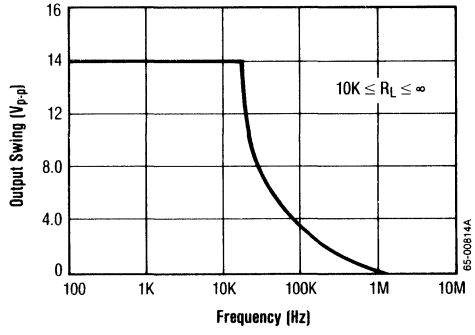
Input Current vs. Temperature



Supply Current

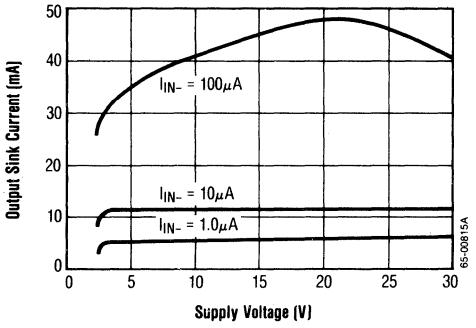


Large Signal Frequency Response

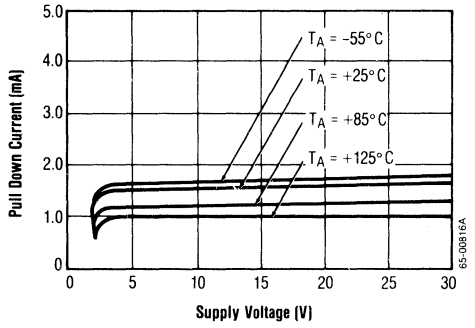


Typical Performance Characteristics (Continued)

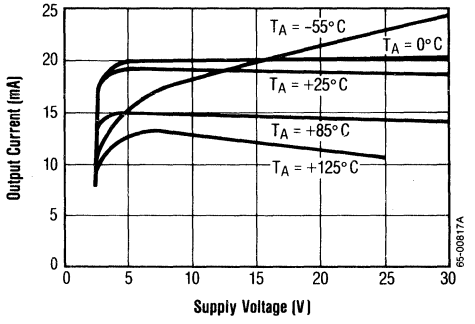
Output Sink Current vs. Supply Voltage



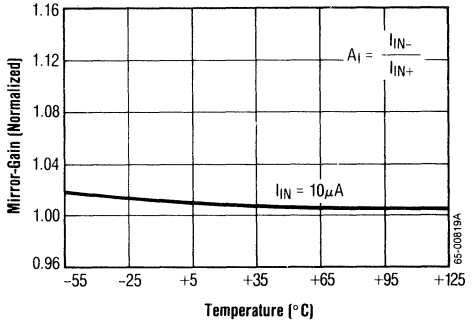
Output Class A Bias Current



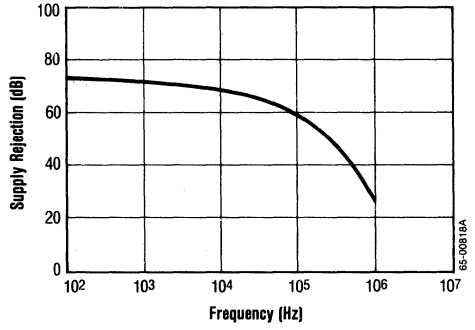
Output Source Current



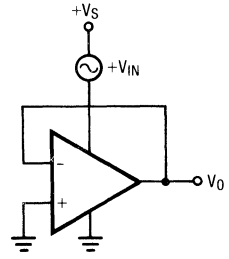
Mirror Gain vs. Temperature



Supply Rejection vs. Frequency

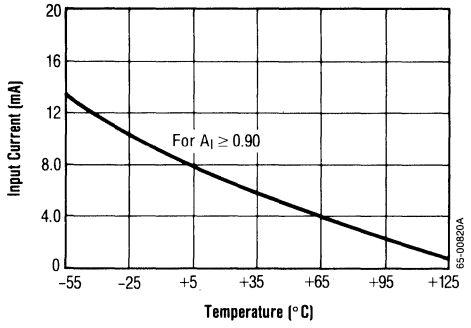


Test Circuit for Supply Rejection



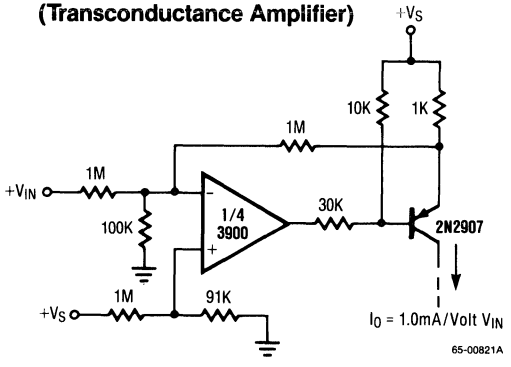
Typical Performance Characteristics (Continued)

Maximum Mirror Current

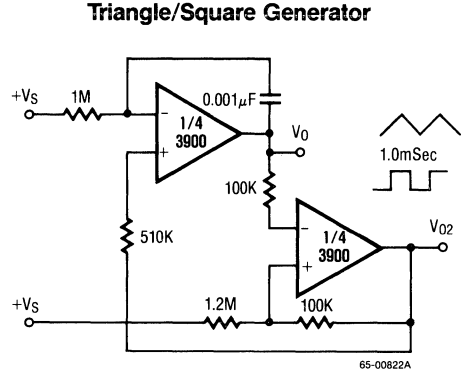


3900 Typical Applications (V_S = +15V)

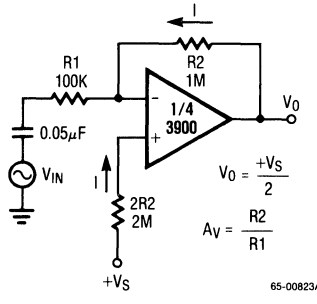
Voltage-Controlled Current Source (Transconductance Amplifier)



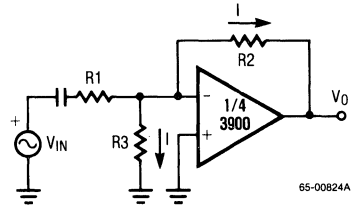
Triangle/Square Generator



Inverting Amplifier



V_{BE} Biasing



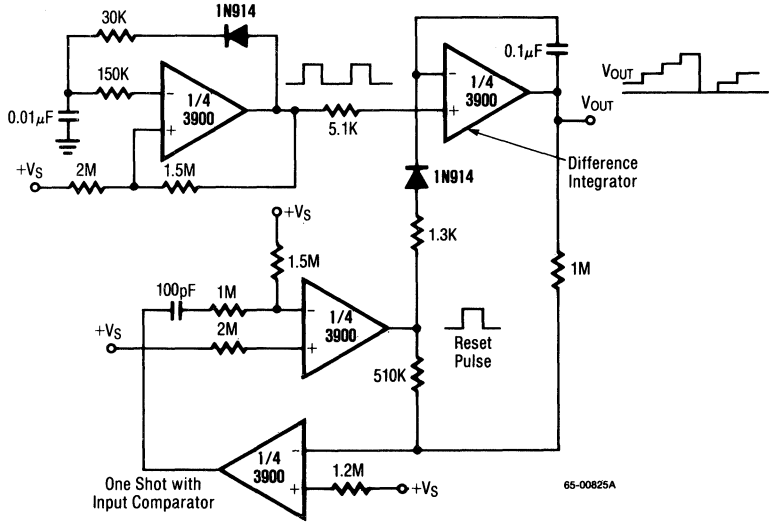
$V_{BE} = 0.5V$

$V_O = V_{BE}\left(1 + \frac{R2}{R3}\right)$

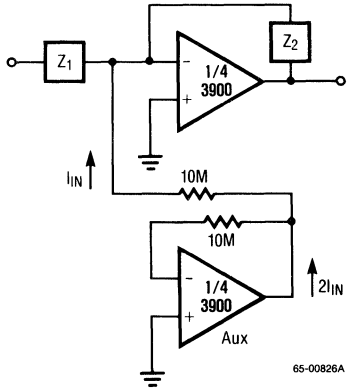
$A_V = \frac{-R2}{R1}$

3900 Typical Applications (Continued)

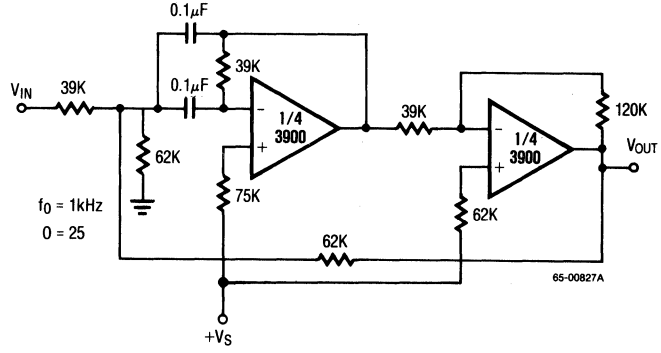
Free-Running Staircase Generator/Pulse Counter



Supplying I_{IN} With Auxiliary Amplifier (to Allow High Z Feedback Networks)

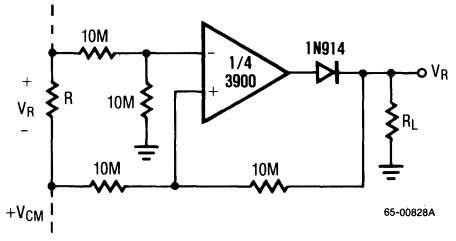


Bandpass Active Filter

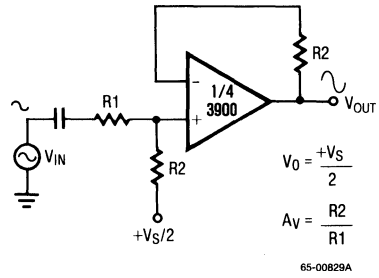


3900 Typical Applications (Continued)

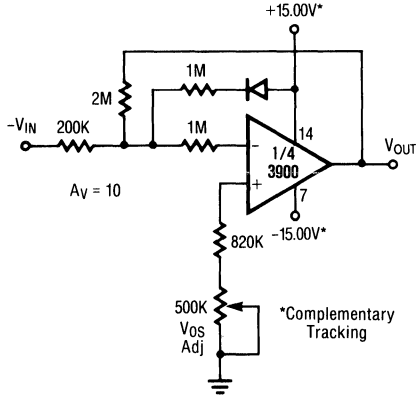
Ground Referencing a Differential Input Signal

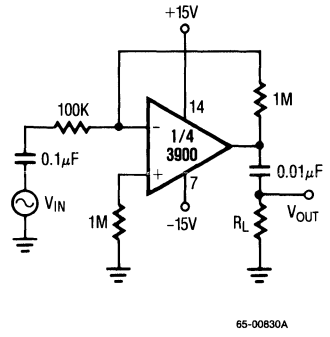


Non-Inverting Amplifier

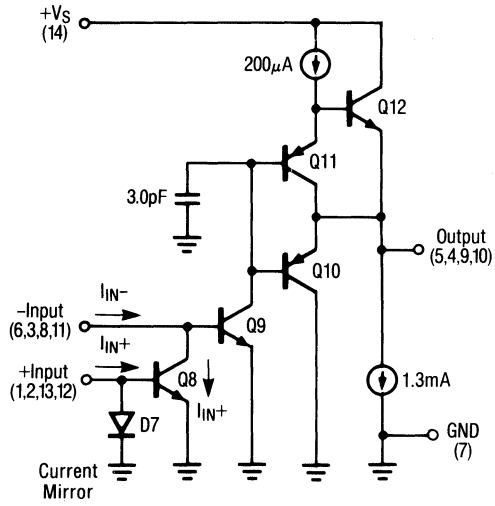


Split Supply ($+V_S$ = +15V and $-V_S$ = -15V)





Schematic Diagram



65-00807A

SECTION 5

COMPARATORS

DEFINITIONS

Average Input Offset Voltage Drift (TC_{VOS})
The ratio of change in input offset voltage to a change in ambient temperature, expressed in microvolts per degree C ($\mu V/^\circ C$).

$$TC_{VOS} = \frac{V_{OS} @ T_{(1)} - V_{OS} @ T_{(2)}}{T_{(1)} - T_{(2)}}$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Common Mode Rejection Ratio (CMRR)
The ratio of change of input common mode voltage (both inputs swing together over a specified voltage range) to a change in input offset voltage, expressed in decibels (dB).

$$CMRR = 20LOG_{10}\left(\frac{V_{IN(1)} - V_{IN(2)}}{V_{OS} @ V_{IN(1)} - V_{OS} @ V_{IN(2)}}\right)$$

Where $V_{IN(1)}$ and $V_{IN(2)}$ are the upper and lower limits of the input common mode voltage range.

Input Bias Current (I_B)
The average of the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Offset Current (I_{OS})
The difference between the two input currents with the output voltage at the center of its swing with no load, expressed in nanoamps (nA).

Input Offset Voltage (V_{OS})
The voltage that must be applied between the two inputs to obtain an output voltage in the center of the output swing range, expressed in millivolts or microvolts (mV or μV).

Input Voltage Range
The range of voltages at the inputs over which the comparator operates within its common mode rejection ratio specification, expressed in volts (V).

Large Signal Voltage Gain (A_V)
The ratio of a specified output voltage change to the change in input offset voltage required to effect the change under open loop conditions, expressed in volts per millivolt (V/mV).

$$A_V = \frac{V_{O(1)} - V_{O(2)}}{V_{OS(1)} - V_{OS(2)}}$$

Where $V_{O(1)}$ and $V_{O(2)}$ are the specified upper and lower voltage limits for the change at the output.

Output Leakage Current
For open collector output types; the collector to emitter leakage current of the output transistor with the output in an off condition and a specified voltage applied, expressed in microamps (μA).

DEFINITIONS (Continued)

Output Sink Current
The current flowing into the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Source Current
The current flowing out of the output for a specified set of input and output conditions, measured in milliamps (mA).

Output Voltage Swing
The peak output change, referred to ground, that can be obtained for a specified load resistance, expressed in volts (V).

Power Consumption
The DC power required to operate the comparator with the output at the center of its swing and zero load current, expressed in milliwatts (mW).

Power Supply Rejection Ratio (PSRR)
The ratio of change of supply voltage to a change in input offset voltage, expressed in decibels (dB).

$$PSRR = 20LOG_{10}\left(\frac{V_{S(1)} - V_{S(2)}}{V_{OS} @ V_{S(1)} - V_{OS} @ V_{S(2)}}\right)$$

Where $V_{S(10}$ and $V_{S(2)}$ are the upper and lower limits of the specified change of supply voltage.

Propagation Delay
The time delay between a step input to a resulting change at the output, from the 50% point of the input step to the 50% point of the output swing, measured in nanoseconds (nS).

Saturation Voltage (V_{SAT})
Voltage at the output when sinking a specified amount of current into the output, expressed in volts (V).

Supply Current (I_S)
The current required from the power supply to operate the comparator under quiescent no load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which the comparator will operate, expressed in volts (V).

RC4805 Precision High Speed Latching Comparator

Features

- 22 nS propagation delay
- Low offset voltage — 100 µA
- Low offset current — 15 nA
- TTL compatible latch
- TTL output

Description

The RC4805 is an ideal comparator for high speed, high precision applications. The input errors are factory trimmed to less than 1/10 LSB of a 12-bit, 10V system. The latch function allows the system designer additional flexibility. When the latch input is a TTL low, the comparator functions normally. When the input is raised to a TTL high, the comparator output is latched in its current state.

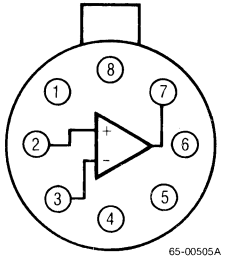
The RC4805 is ideal for ultra precise, very fast system designs. Typical applications include successive approximation A/D converters of 12 or more bits, zero crossing detectors, high speed sampling, or window detectors.

The RC4805 high speed comparator is functionally equivalent to the popular comparators HA-4950, AM686, SE527, CMP-05 and µA760. Propagation delay is 35 nS with a 1/2 LSB overdrive in a 12-bit, 10V system.

The RC4805 specifications and design have been upgraded since the last printing of this data sheet.

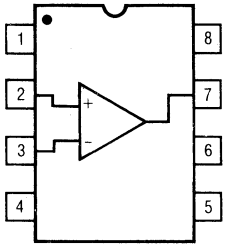
Connection Information

8-Lead
TO-99 Metal Can
(Top View)



65-00505A

8-Lead
Dual In-Line Package
(Top View)



65-00506A

Pin	Function
1	Ground
2	+ Input
3	-Input
4	$-V_S$
5	NC
6	Latch Enable
7	V_{OUT}
8	$+V_S$

Absolute Maximum Ratings

Supply Voltage ..... +5.5V/-16.5V
Differential Input Voltage 3V
Internal Power Dissipation* ..... 500 mW
Input Voltage ..... ±4V
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4805 ..... -55°C to +125°C
RC4805 ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

*See table of Thermal Characteristics for maximum ambient temperature derating factor.

Thermal Characteristics

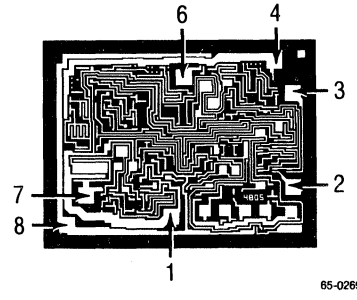
	8- Lead Ceramic DIP	8- Lead TO-99 Metal Can	8- Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	125°C
Max. P_D T_A <50°C	833mW	658mW	468mW
Therm. Res θ_{JC}	45°C/W	50°C/W	—
Therm. Res. θ_{JA}	150°C/W	190°C/W	160°C/W
For T_A >50°C Derate at	8.33mW per °C	5.26mW per °C	6.25 mW per °C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4805EN	N	0°C to +70°C
RC4805N	N	0°C to +70°C
RM4805D	D	-55°C to +125°C
RM4805D/883B	D	-55°C to +125°C
RM4805AD	D	-55°C to +125°C
RM4805AD/883B	D	-55°C to +125°C
RM4805T	T	-55°C to +125°C
RM4805T/883B	T	-55°C to +125°C
RM4805AT	T	-55°C to +125°C
RM4805AT/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Mask Pattern



Die Size: 51 x 67 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = ±5V, T_A = +25°C, Latch Enable = 0V unless otherwise noted)

Parameters	Test Conditions	RC4805E/ RM4805A			RC4805/ RM4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 50\Omega$		100	250		250	600	µV
Input Offset Current			10	80		25	150	nA
Input Bias Current			0.7	1.2		0.9	1.8	µA
Large Signal Voltage Gain		15	50		10	40		V/mV
Output Voltage Swing	V_{IN} > 10 mV, I_O = 200 µA	2.4	2.7		2.4	2.7		V
	V_{IN} < -10 mV, I_{SINK} = 8 mA		0.3	0.4		0.3	0.4	V
Input Voltage Range		±2.2	±2.7		±2.0	±2.7		V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, V_{CM} = Min Input Voltage Range	86			84			dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $+V_S$ = +5V, $-5.25V \leq -V_S \leq -4.75V$ and $-V_S$ = -5V, $+4.75V \leq +V_S \leq +5.25V$	86			84			dB
	$R_S \leq 50\Omega$ $+V_S$ = +5V, $-5V \leq -V_S \leq -15V$	86			84			dB
Supply Current (Positive)	$V_O \leq 0.4V$		11	16		13	18	mA
Supply Current (Negative)	$V_O \leq 0.4V$		12	16		13	18	mA
Power Consumption	$V_O \leq 0.4V$		115	160		130	180	mW
Propagation Delay*	100 mV Step, V_{OD} = 5 mV		22	35		22	35	nS
	100 mV Step, V_{OD} = 1.2 mV		35			35		nS
Latch Enable Time	V_{OD} = 5 mV		16			16		nS
Disable Time	V_{OD} = 5 mV		22			22		nS
Latch High Voltage		2.0			2.0			V
Low Voltage				0.8			0.8	V
Latch High Current	V_{LH} = 3.0V			40			75	µA
Low Current	V_{LL} = 0.8V			10			20	µA

*Minimize lead lengths by soldering directly to PC board. The use of sockets may cause oscillations from stray capacitive coupling.

Electrical Characteristics

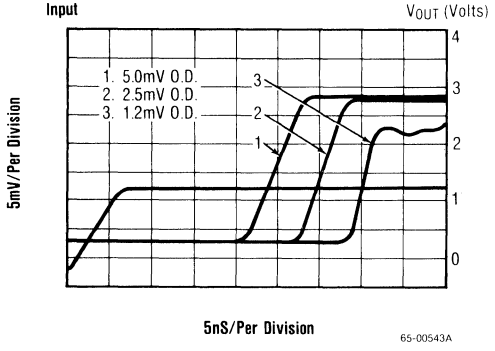
(V_S = ±5V, RM = -55°C ≤ TA ≤ +125°C; RC = 0°C ≤ T_A ≤ +70°C, Latch Enable = 0V unless otherwise noted)

Parameters	Test Conditions	RC4805E/ RM4805A			RC4805/ RM4805			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$R_S \leq 50\Omega$		0.25	0.80		0.50	1.5	mV
Average Input Offset Voltage Drift	(Note 1)		1.5	5.0		2.5	7.5	µV/°C
Input Offset Current				200			400	nA
Input Bias Current				2.5			3.8	µA
Large Signal Voltage Gain			15			10		V/mV
Output Voltage Swing	V_{IN} > 10 mV, I_O = 200 µA	2.2	2.5		2.2			V
	V_{IN} < -10 mV, I_{SINK} = 6.4 mA		0.3	0.45		0.3	0.45	V
Input Voltage Range		±2.0			±2.0			V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, V_{CM} = ±2V Input Voltage Range	85			80			dB
Power Supply Rejection Ratio	$R_S \leq 50\Omega$, $+V_S$ = +5V, -5.25V ≤ $-V_S$ ≤ -4.75V and $-V_S$ = -5V, +4.75V ≤ $+V_S$ ≤ +5.25V	75			72			dB
Supply Current (Positive)	$V_O \leq 0.4V$		13	18		15	20	mA
Supply Current (Negative)	$V_O \leq 0.4V$		15	20		15	20	mA
Power Consumption	$V_O \leq 0.4V$		140	190		150	200	mW
Propagation Delay[1]	100 mV Step, V_{OD} = 5 mV		30	50		35	55	nS
	100 mV Step, V_{DD} = 1.2 mV		50			50		nS

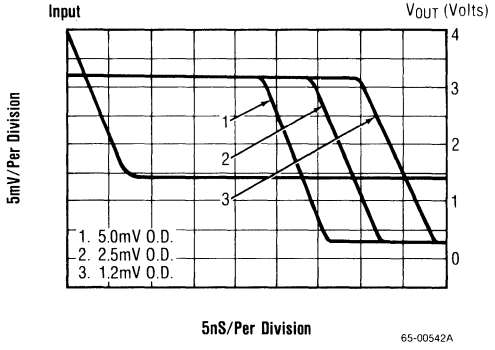
Notes:
1. Guaranteed but not tested.

Typical Performance Characteristics

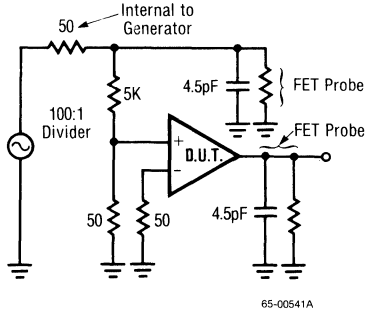
4805 Response Time Rising Edge



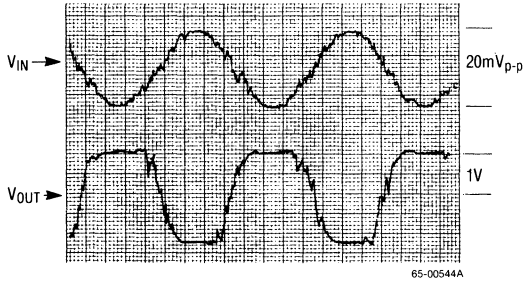
4805 Response Time Falling Edge



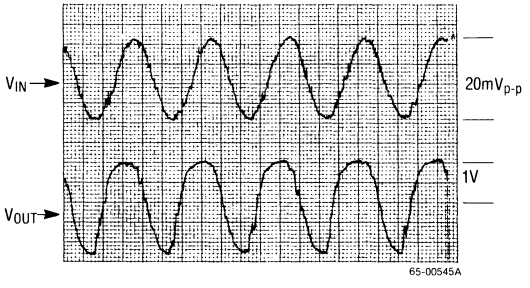
Response Photography Test Setup



Response to 25MHz Sine Wave

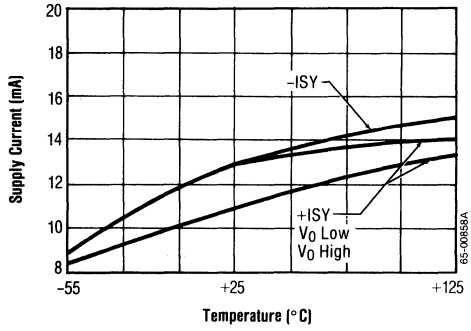


Response to 50MHz Sine Wave

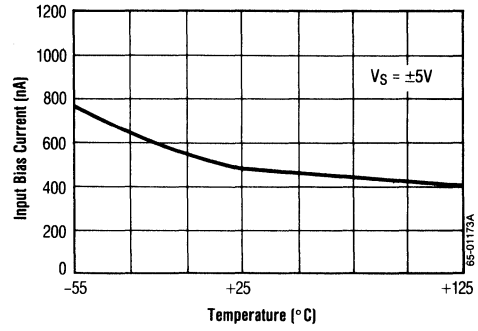


Typical Performance Characteristics (Continued)

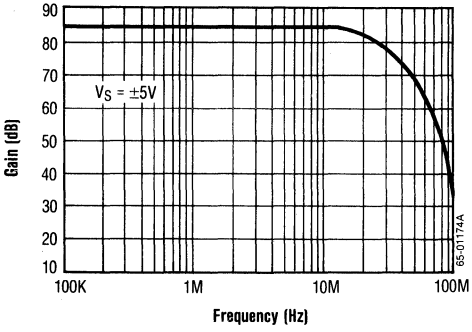
Supply Current vs. Temperature



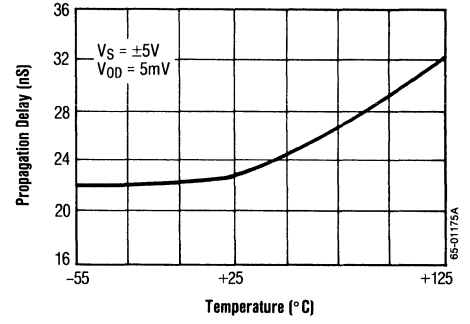
Input Bias Current vs. Temperature



Gain vs. Frequency



Propagation Delay vs. Temperature



Applications Information

Optimal performance of the 4805 in high speed applications circuits requires that careful layout and circuit design techniques are used. The use of good power supply bypass capacitors, minimum lead lengths, and a good ground plane are essential.

Bypass Capacitors

Tantalum electrolytics connected close to the power suppiy leads are usually sufficient; sometimes a smaller ceramic capacitor in parallel with the tantalum may improve high frequency response even further. Typical values would be 10μF in parallel with 0.01μF.

Minimize Lead Lengths

Short input leads are essential to eliminate stray capacitance that might otherwise induce oscillations. **Avoid the use of sockets;** solder the IC directly to the PC board. When laying out a PC board, position the signal source as close to the comparator inputs as is physically possible. Avoid stray capacitance from the inputs to ground, and route the output away from the inputs. Best response times will occur when the source impedance driving the inputs is kept low (<1kΩ). Avoid driving heavy capacitive loads with the output (example: coaxial cable, which has a parasitic capacitance of 50pF per foot).

Ground Plane

A ground plane reduces the parasitic inductance of PC traces. Current flow through the PC trace is mirrored by a return current flow that passes through the ground plane adjacent to the PC trace. This sets up a magnetic field that cancels the magnetic field in the PC trace, thus reducing parasitic inductance.

Use the component side of the board for the ground plane. Cover that side as completely as is practical, especially under traces carrying high frequency signals. Mount HF components close to the board.

Latch Enable

The effective gain at low levels of input overdrive can be increased by applying a carefully timed positive going step to the latch enable input. This technique is especially useful in successive approximation A/D converters, where the exact time of comparison is well defined. After the SAR changes the DAC output, a delayed pulse applied to pin 6 will increase the effective gain from about 5V/mV to 20V/mV, and therefore speeds up the response time for low levels input signals. In a 12-bit ±10V A/D system, the propagation delay for 1 LSB will decrease about 30%. Figure 1 shows the waveforms for this technique, and Figure 2 shows a one-shot time delay circuit using a TTL IC that can be used to create the pulse.

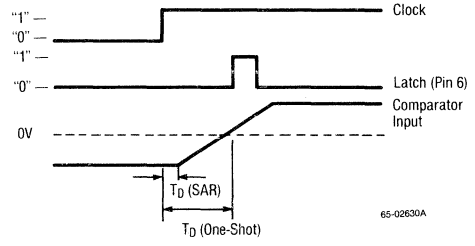


Figure 1. Gain Boost Waveforms

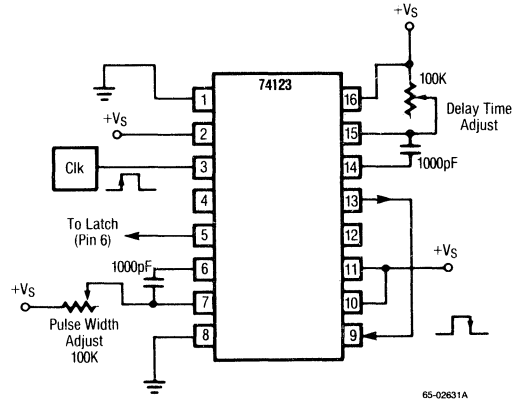
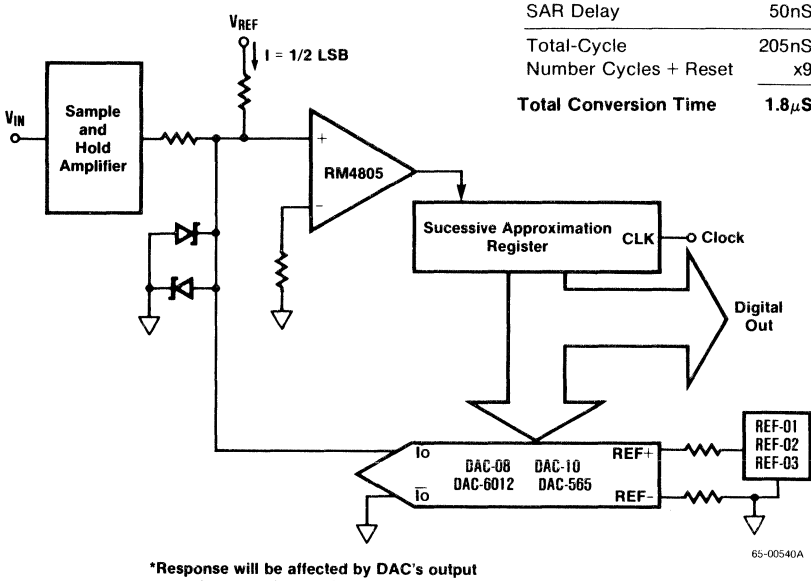


Figure 2. Delayed Pulse Circuit

Typical Applications

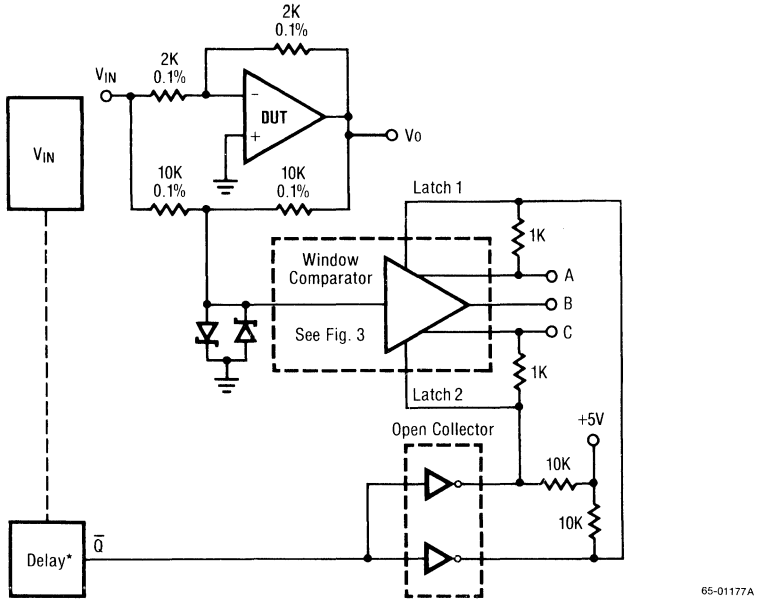
	Conversion Time		
	8-Bit	10-Bit	12-Bit
RM4805 Response	20nS	22nS	50nS
DAC Settling*	135nS	135nS	500nS
SAR Delay	50nS	50nS	50nS
Total-Cycle	205nS	207nS	600nS
Number Cycles + Reset	x9	x11	x13
Total Conversion Time	**1.8μS**	**2.3μS**	**7.8μS**



*Response will be affected by DAC's output capacitance and equivalent resistance.

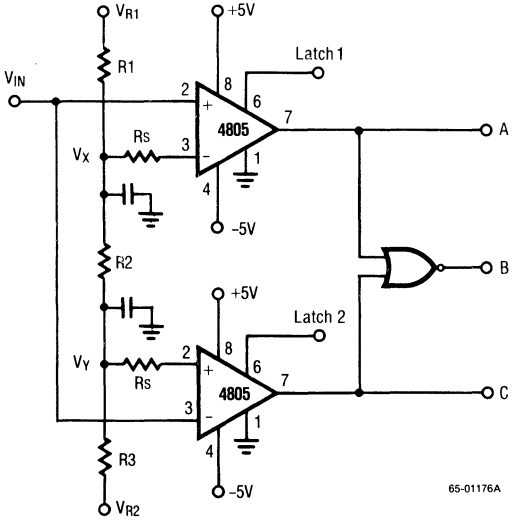
Figure 3. Successive Approximation 8, 10, or 12-bit Resolution

Typical Applications (Continued)



*Delay should equal the settling time specification minus 30nS minus appropriate guard band

Figure 4. Op Amp Settling Time Tester



The settling time tester uses the precision latching window comparator to automate op amp settling time testing. If the DUT is not settled by the end of the time delay, the A output is latched low.

V_{IN} (V_X > V_Y)*	A	B	C
V_{IN} > V_X	1	0	0
V_X > V_{IN} > V_Y	0	1	0
V_Y > V_{IN}	0	0	1

*Both latches low

Figure 5. Precision Latching Window Comparator (Detail)

Fast Latching ECL to TTL Line Translator, Up to 50MHz

The high speed differential input and the latched TTL output makes the RC4805 ideally suited for use as an ECL to TTL translator. Existing logic supplies of -5.2V and +5.0V are compatible with the RC4805 power supply requirements. With a TTL compatible latch input the RC4805 can be latched from the TTL subsystem or from the ECL subsystem, by using another RC4805 on the latch signal.

In ECL systems the termination resistors and pull-down resistors can be combined in a network as shown in Figure 6, a typical ECL to TTL translator. The configuration shown in Figure 8 has a common mode range of ±2.0V. But either input can swing as low as -5.0V below the input, providing one input stays in the ±2.0V common mode range. By using a -15V supply on the RC4805 the common mode range is extended to -8.0V, +2.0V as shown in Figure 7. The only caution is that the differential mode voltage must not exceed +5.0V.

Not all ECL families have the same logic levels, the same logic level V_S supply voltage, or the same temperature characteristics. By using the same logic type as a reference, a single-end ECL to TTL translator can be made to track changes in logic levels. A typical circuit is shown in Figure 8.

In system design one subsystem may in one configuration be driven with ECL line drivers, but in another configuration the same subsystem may be driven from a TTL gate.

High gain, low input bias current and ±2.0V common mode range on the RC4805 allow the easy design of an adaptive ECL-TTL to TTL translator. The ECL interface is the same as shown in Figure 6. By adding pull-up resistors and a bypassed level shifting resistor to the TTL outputs (see Figure 9), the same subsystem line receiver can interface with ECL or TTL with no hardware change in the receiver.

In summary, the RC4805 is a very flexible system element that allows the system designer to interface ECL to TTL in a number of easy to use configurations. The RC4805 can also be used in an adaptive ECL-TTL to TTL interface.

Typical Examples

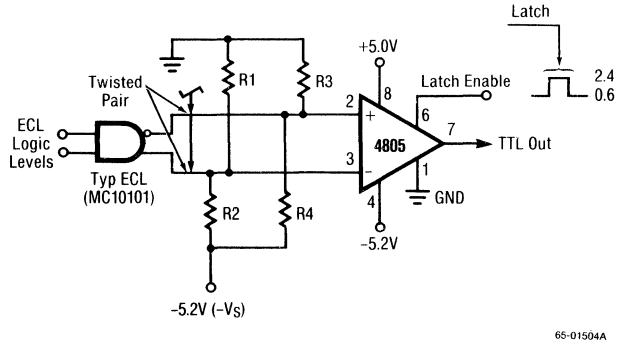
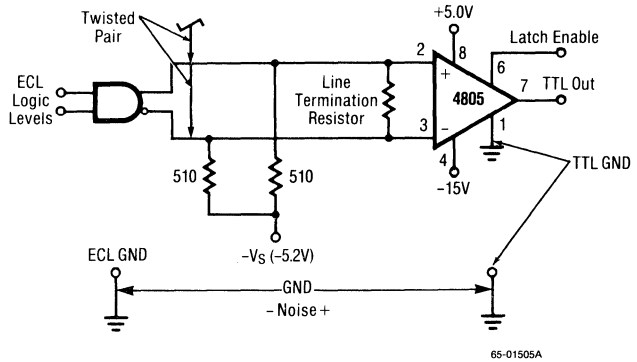


Figure 6. Typical ECL to TTL Translator

Typical Examples (Continued)



Notes:

1. Common mode range of 4805 is -8.0V to +2.0V.
2. The 4805 can stand -3.0V, +5.0V of GND noise from the ECL GND to the TTL GND.

Figure 7. ECL to TTL Translator With Extended Common Mode Range

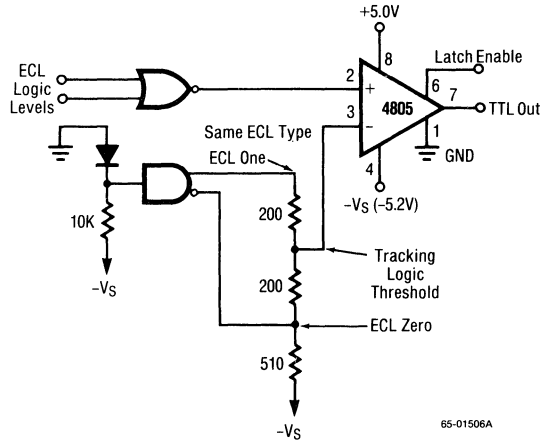


Figure 8. Single-Ended ECL to TTL Translator With Tracking ECL Reference

Typical Examples (Continued)

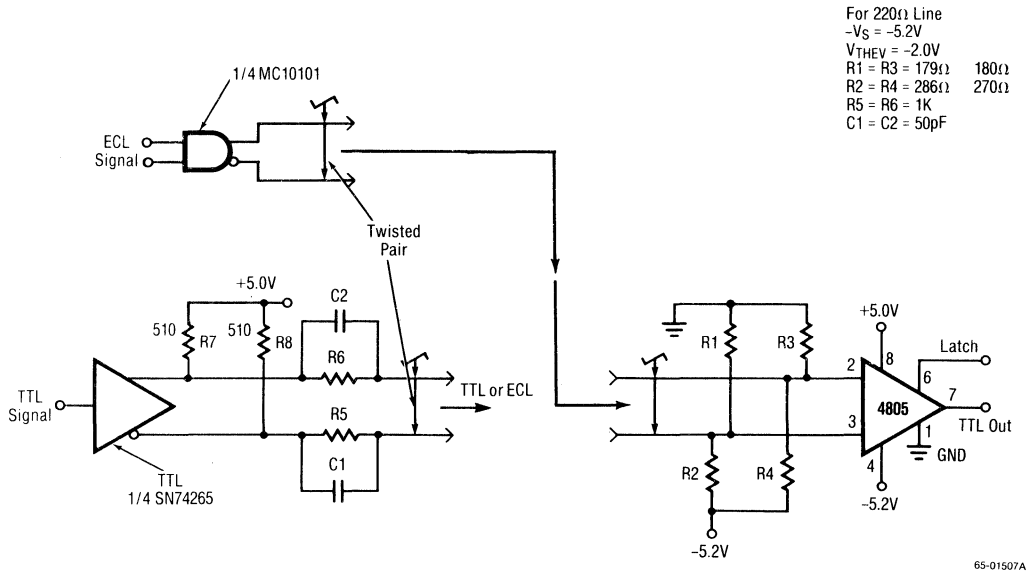
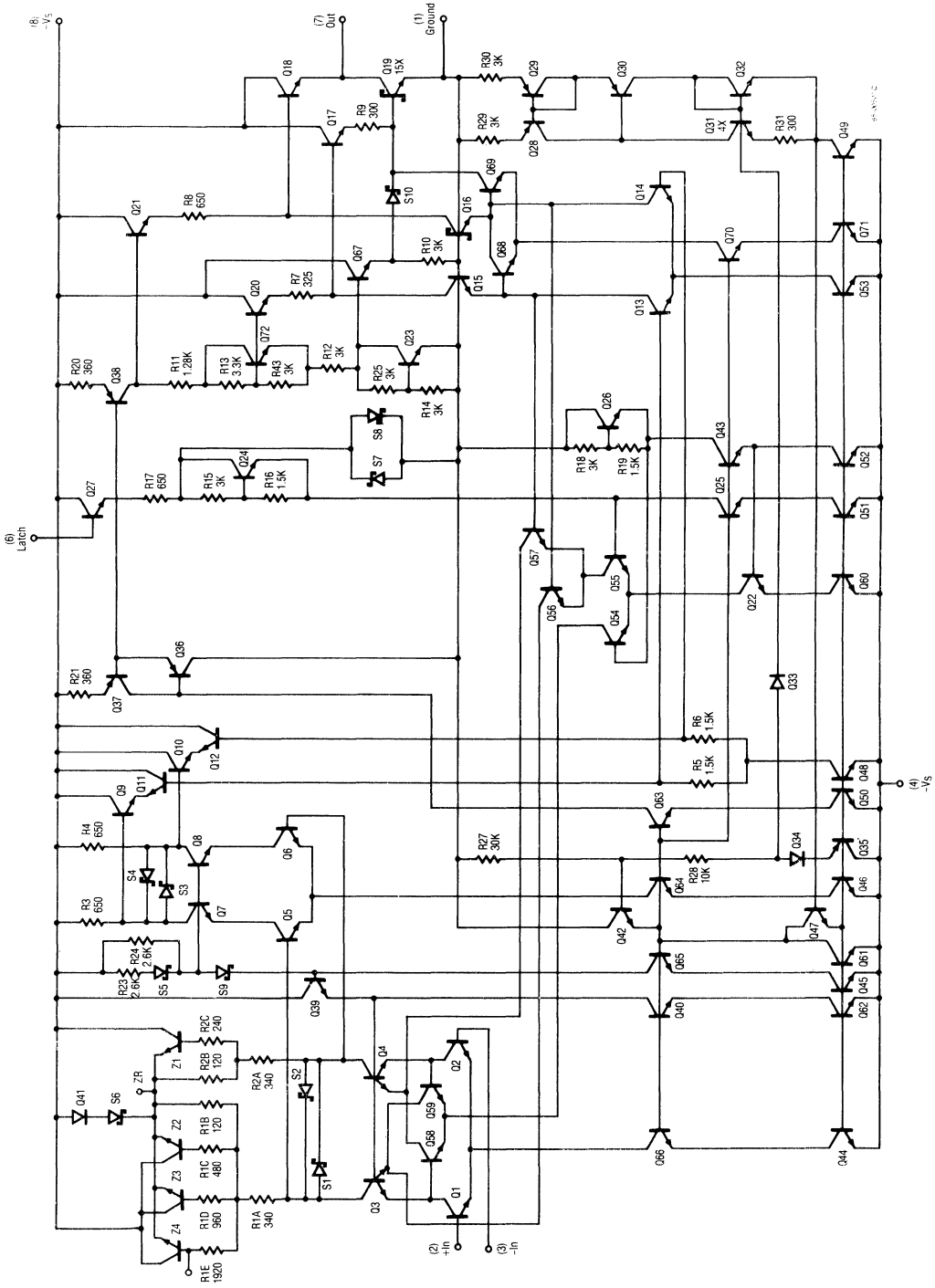


Figure 9. Adaptive ECL-TTL to TTL Translator

Schematic Diagram



LM111/LH2111 Voltage Comparators

Features

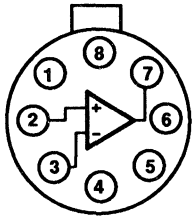
- Low input offset current — 10 nA max
- Low input bias current — 100 nA max.
- Operates from a single +5V supply
- Response time — 200 nS

Description

These low-input current voltage comparators are designed to operate over a wide range of supply voltages, including ±15V and single +5V supplies. Their outputs are compatible with DTL, RTL, TTL, and MOS devices, and can be connected in "wire-OR" configuration. The LH2111 consists of two LM111 ICs packaged in one 16-lead DIP. Both the LM111 and LH2111 are available with Mil-Std-883B screening.

Connection Information

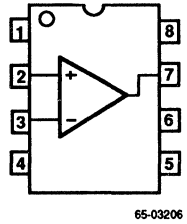
8-Lead TO-99 Metal Can
(Top View)



65-03205

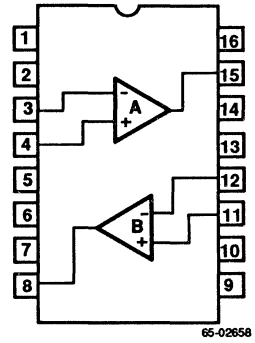
Pin	Function
1	Ground
2	+Input
3	-Input
4	$-V_S$
5	Balance
6	Balance/Strobe
7	Output
8	$+V_S$

8-Lead Dual In-Line Package
(Top View)



65-03206

16-Lead Ceramic DIP



65-02658

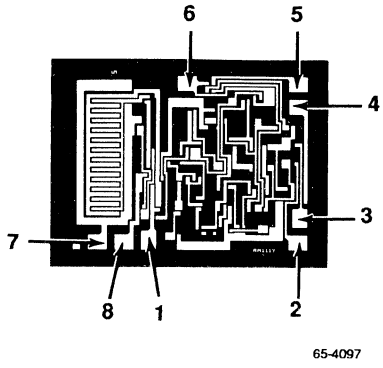
Pin	Function
1	$+V_S$ (A)
2	Ground (A)
3	+Input (A)
4	-Input (A)
5	$-V_S$
6	Balance (B)
7	Bal/Strobe (B)
8	Output (B)
9	$+V_S$ (B)
10	Ground (B)
11	+Input (B)
12	-Input (B)
13	Balance (A)
14	Bal/Strobe (A)
15	Output (A)
16	NC

Ordering Information

Part Number	Package	Operating Temperature Range
LM111T	T	-55°C to +125°C
LM111T/883B	T	-55°C to +125°C
LM111D	D	-55°C to +125°C
LM111D/883B	D	-55°C to +125°C
LH2111D	D	-55°C to +125°C
LH2111D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D = 8- lead ceramic DIP (LM111)
D = 16-lead ceramic DIP (LH2111)
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Mask Pattern



Die Size: 53 mils x 69 mils
Min. Pad Dimensions: 4 mils x 4 mils

Absolute Maximum Ratings

Supply Voltage 36V
Output to $-V_S$ 50V
Ground to $-V_S$ 30V
Differential Input Voltage 30V
Input Voltage* ..... ±15V
Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... 10 Sec
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +125°C
Voltage at Strobe Pin ..... $+V_S$ -5V
Lead Soldering Temperature (60 sec) ..... +300°C

*For supply voltages other than ±15V, the maximum input is equal to the supply voltage.
**Observe package thermal characteristics.

Thermal Characteristics

	8-Lead TO-99 Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP
Max. Junction Temp.	175°C	175°C	175°C
Max. P_D T_A <50°C	658 mW	833 mW	1042 mW
Therm. Res θ_{JC}	50°C/W	45°C/W	60°C/W
Therm. Res. θ_{JA}	190°C/W	150°C/W	120°C/W
For T_A >50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C

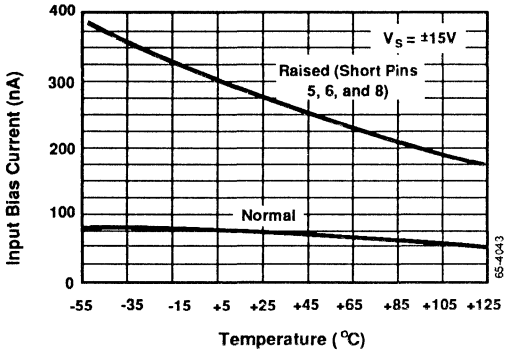
Electrical Characteristics (V_S = ±15V[1] and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Offset Voltage[2]	T_A = +25°C, R_S ≤ 50 kΩ		0.7	3.0	mV
Input Offset Current[2]	T_A = +25°C		4.0	10	nA
Input Bias Current	T_A = +25°C		60	100	nA
Large Signal Voltage Gain	T_A = +25°C	40	200		V/mV
Response Time	T_A = +25°C, 100 mV step, 5mV overdrive		200		nS
Output Voltage Low (V_{OL})	V_{IN} ≤ 5 mV, I_L = 50 mA, T_A = +25°C		0.75	1.5	V
Strobe on Current	T_A = +25°C		3.0		mA
Output Leakage Current	V_{IN} ≥ 5 mV, V_{OUT} = 35V, T_A = +25°C, I_{STROBE} = 3 mA		0.2	10	nA
Input Offset Voltage[2]	R_S ≤ 50 kΩ		1.5	4.0	mV
Input Offset Current[2]			5.0	20	nA
Input Bias Current			100	150	nA
Input Voltage Range	Pin 7 pull up may go to +5V	-14.5		13.0	V
Output Voltage Low (V_{OL})	+V_S = 4.5V, -V_S = 0V, V_{IN} ≤ -6 mV, I_{OUT} = 8.0 mA		0.23	0.4	V V
Output Leakage Current	V_{IN} ≥ 5 mV, V_{OUT} = 35V		100	500	nA
Positive Supply Current	T_A = +25°C, each amplifier		5.1	6.0	mA
Negative Supply Current	T_A = +25°C, each amplifier		4.1	5.0	mA

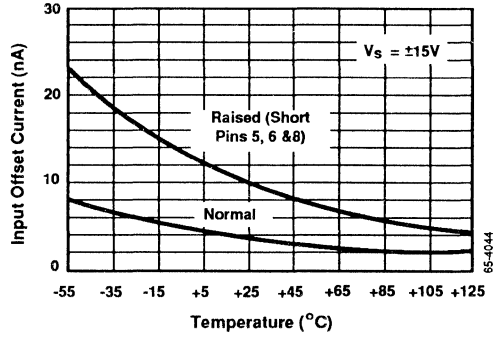
Notes:
1. V_{OS}, I_{OS}, and I_B specifications apply for V_S = +5V to V_S = ±15V.
2. V_{OS} and I_{OS} are maximum values required to drive the output to within 1V of either supply with a 1 mA load.
3. Do not short circuit the strobe pin to ground — drive it instead with a 3 to 5 mA current.
4. If the strobe and balance pins are unused, short them together for maximum ac stability.

Typical Performance Characteristics

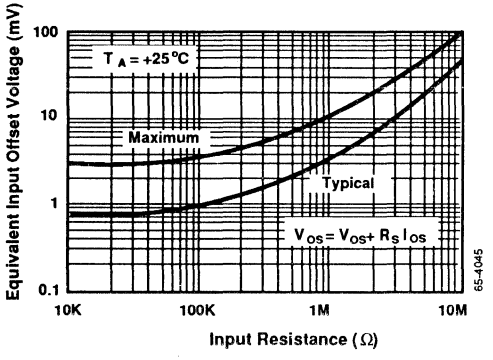
Input Bias Current



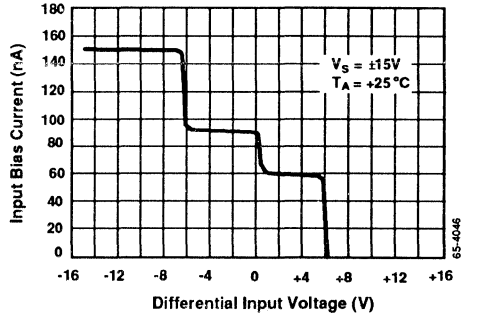
Input Offset Current



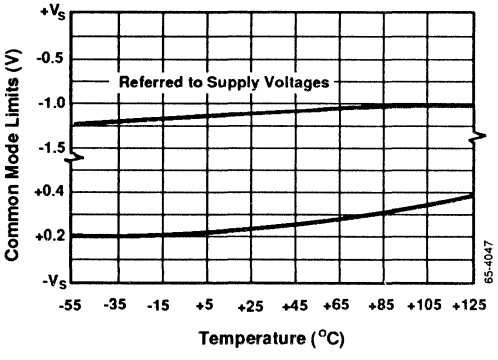
Offset Error



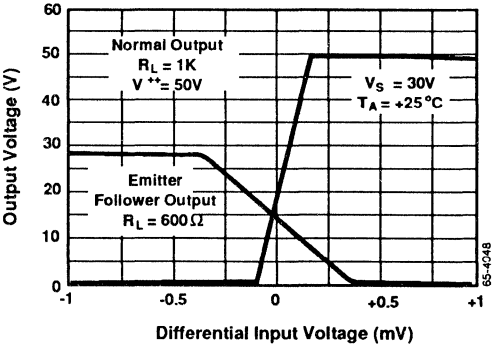
Input Characteristics



Common Mode Limits

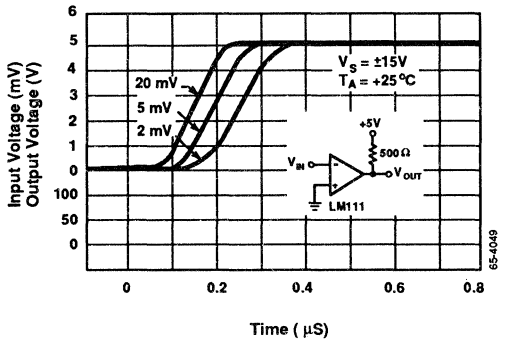


Transfer Function

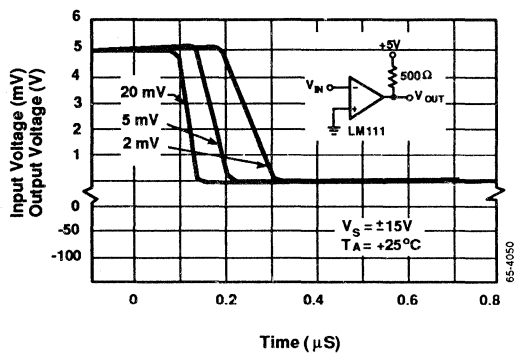


Typical Performance Characteristics (Continued)

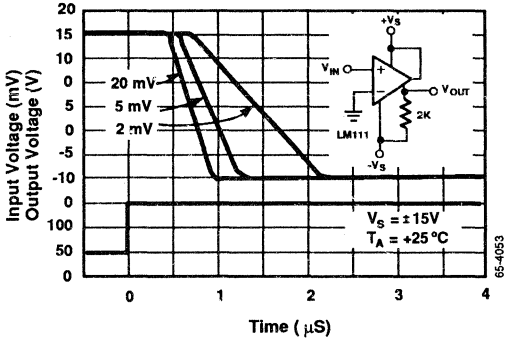
Response Time for Various Input Overdrives



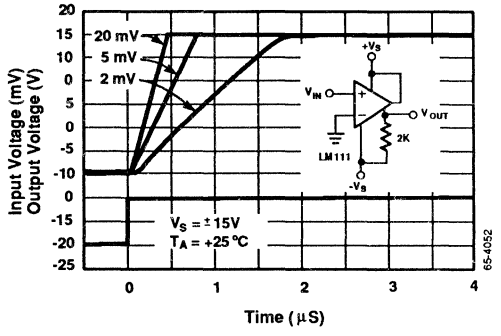
Response Time for Various Input Overdrives



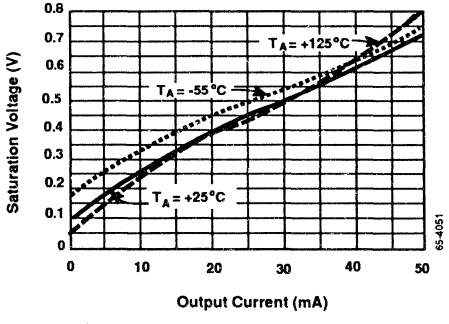
Response Time for Various Input Overdrives



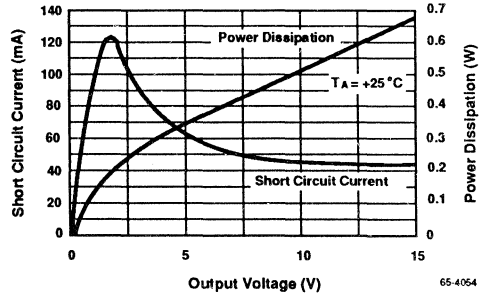
Response Time for Various Input Overdrives



Output Saturation Voltage

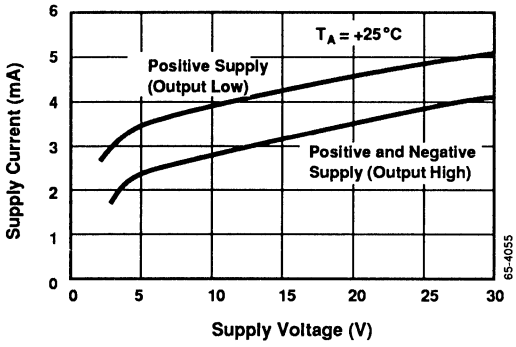


Output Limiting Characteristics

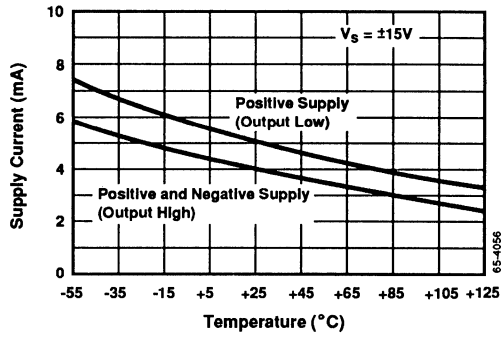


Typical Performance Characteristics (Continued)

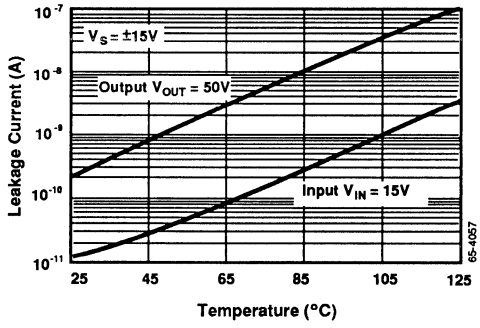
Supply Current



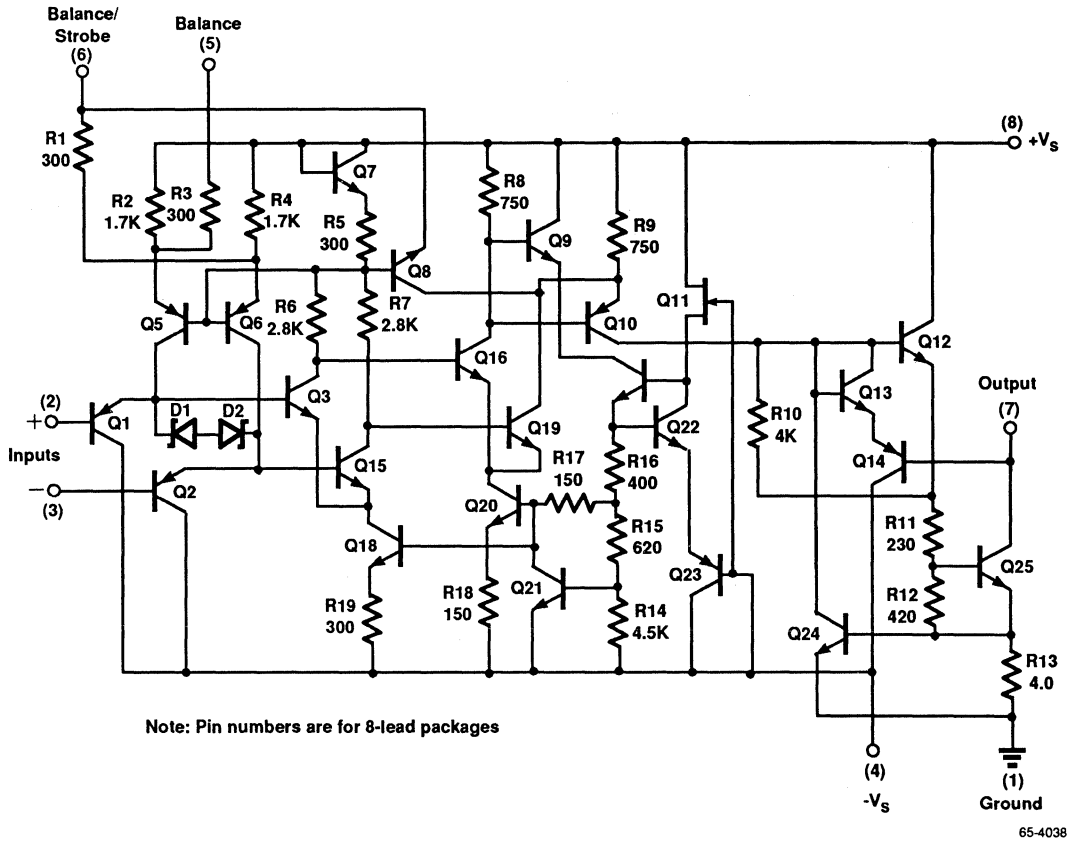
Supply Current



Leakage Currents



Schematic Diagram



LM139/139A, 339/339A, Single-Supply Quad Comparators

Features

- Input common mode voltage range includes ground
- Wide single supply voltage range — 2V to 36V
- Output compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Very low supply current drain (0.8 mA) independent of supply voltage

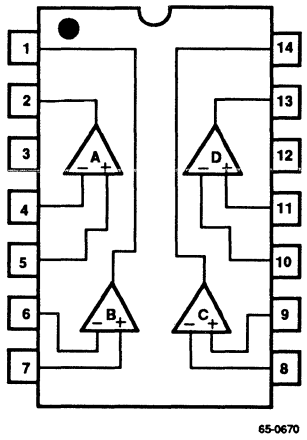
Description

These devices offer higher frequency operation and faster switching than can be had from internally compensated quad op amps. Intended for single-supply applications, the Darlington PNP input stage allows them to compare voltages that include ground. The two-stage common-emitter output circuit provides gain and output sink capacity of 3.2 mA at an output level of 400 mV. The output collector is left open, permitting the designer to drive devices in the range of 2V to 36V.

They are intended for applications not needing response time less than 1 μS, but demanding excellent op amp input parameters of offset voltage, current, and bias current, to ensure accurate comparison with a reference voltage.

Connection Information

14-Lead Dual In-Line Package (Top View)



65-0670

Pin	Function	Pin	Function
1	Output B	8	-Input C
2	Output A	9	+Input C
3	$+V_S$	10	-Input D
4	-Input A	11	+Input D
5	+Input A	12	Ground
6	-Input B	13	Output D
7	+Input B	14	Output C

Absolute Maximum Ratings

Supply Voltage, $+V_S$ ..... +36V or ±18V
Differential Input Voltage 36V
Input Voltage Range ..... -0.3 to +36V(2)
Output Short Circuit to Ground(1) ..... Continuous
Input Current (V_{IN} < -0.3V)(2) ..... 50 mA
Operating Temperature Range
LM139 ..... -55°C to +125°C
LM339 ..... 0°C to +70°C
StorageTemperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(SO-14; 10 sec) ..... +260°C
Lead Soldering Temperature
(DIP; 60 sec) ..... +300°C

See Notes on page 5-27

Ordering Information

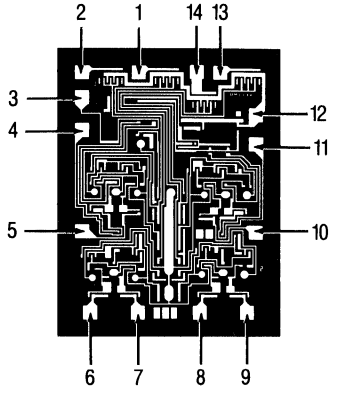
Part Number	Package	Operating Temperature Range
LM339M	M	0°C to +70°C
LM339N	N	0°C to +70°C
LM339AM	M	0°C to +70°C
LM339AN	N	0°C to +70°C
LM139D	D	-55°C to +125°C
LM139D/883B	D	-55°C to +125°C
LM139AD	D	-55°C to +125°C
LM139AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14 lead ceramic DIP
M = 14-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Thermal Characteristics

	14-lead Plastic SO	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	125°C	175°C
Max. P_D T_A <50°C	300 mW	468 mW	1042 mW
Therm. Res θ_{JC}	—	—	60°C/W
Therm. Res. θ_{JA}	200°C/W	160°C/W	120°C/W
For T_A >50°C Derate at	5.0 mW per °C	6.25 mW per °C	8.38 mW per °C

Mask Pattern



Die Size: 59 x 77 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics ($+V_S = +5V$[3])

Parameters	Test Conditions	LM139A Min	LM139A Typ	LM139A Max	LM339A Min	LM339A Typ	LM339A Max	Units
Input Offset Voltage	$T_A = +25°C$ [8]		±1.0	±2.0		±1.0	±2.0	mV
Input Bias Current	Output in Linear Range $T_A = +25°C$ [4], $V_{CM} = 0V$		25	100		25	250	nA
Input Offset Current	$T_A = +25°C$, $V_{CM} = 0V$		±3.0	±25		±5.0	±50	nA
Input Voltage Range	$T_A = +25°C$ [5], $V_S = 30V$	0		$+V_S$ -1.5	0		$+V_S$ -1.5	V
Supply Current	$R_L = \infty$ on all comparators, $T_A = +25°C$		0.8	2.5		0.8	2.5	mA
Large Signal Voltage Gain	$R_L = \infty$, $+V_S = 30V$, $R_L \geq 15\ k\Omega$, $+V_S = +5V$ (to support large V_O swing), $T_A = +25°C$	50	200		50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1\ k\Omega$, $T_A = +25°C$		300			300		nS
Response Time	$V_{RL} = 5V$, $R_L = 5.1\ k\Omega$, $T_A = +25°C$ [6]		1.3			1.3		µS
Output Sink Current	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $V_O \leq 1.5V$, $T_A = +25°C$	6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = +25°C$		250	400		250	400	mV
Output Leakage Current	$V_{IN+} \geq 1V$, $V_{IN-} = 0$, $V_O = 5V$, $T_A = +25°C$		0.1			0.2		µA
Input Offset Voltage	Note 8			±4.0			±4.0	mV
Input Offset Current	$V_{CM} = 0V$			±100			±150	nA
Input Bias Current	$V_{CM} = 0V$			300			400	nA
Input Voltage Range	$+V_S = 30V$	0		$+V_S$ -2.0	0		$+V_S$ -2.0	V
Saturation Voltage	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $I_{SINK} \leq 4\ mA$			700			700	mV
Output Leakage Current	$V_{IN+} \geq 1V$, $V_{IN-} = 0$, $V_O = 30V$			1.0			1.0	µA
Differential Input Voltage [10]	Keep all V_{IN}s ≥ 0V (or $-V_S$, if used) [7]			36			36	V

See Notes on page 5-27

Electrical Characteristics ($+V_S = +5V$[3])

Parameters	Test Conditions	LM139 Min	LM139 Typ	LM139 Max	LM339 Min	LM339 Typ	LM339 Max	Units
Input Offset Voltage	$T_A = +25°C$ [8]		±2.0	±5.0		±2.0	±5.0	mV
Input Bias Current	Output in Linear Range $T_A = +25°C$ [4], $V_{CM} = 0V$		25	100		25	250	nA
Input Offset Current	$T_A = +25°C$, $V_{CM} = 0V$		±3.0	±25		±5.0	±50	nA
Input Voltage Range	$T_A = +25°C$ [5], $+V_S = 30V$	0		$+V_S$ -1.5	0		$+V_S$ -1.5	V
Supply Current	$R_L = \infty$ on all comparators, $T_A = +25°C$		0.8	2.5		0.8	2.5	mA
Large Signal Voltage Gain	$R_L = \infty$, $+V_S = 30V$, $R_L \geq 15\ k\Omega$, $+V_S = +5V$ (to support large V_O swing), $T_A = +25°C$	50	200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1\ k\Omega$, $T_A = +25°C$		300			300		nS
Response Time	$V_{RL} = 5V$, $R_L = 5.1\ k\Omega$, $T_A = +25°C$ [6]		1.3			1.3		µS
Output Sink Current	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $V_O \leq 1.5V$, $T_A = +25°C$	6.0	16		6.0	16		mA
Output Voltage V_{OL}	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = +25°C$		250	400		250	400	mV
Output Leakage Current	$V_{IN+} \geq 1V$, $V_{IN-} = 0$, $V_O = 5V$, $T_A = +25°C$		0.1			0.1		µA
Input Offset Voltage	Note 8			±9.0			±9.0	mV
Input Offset Current				±100			±150	nA
Input Bias Current	$V_{CM} = 0V$			300			400	nA
Input Voltage Range	$V_{CM} = 30V$	0		$+V_S$ -2.0	0		$+V_S$ -2.0	V
Output Voltage V_{OL}	$V_{IN-} \geq 1V$, $V_{IN+} = 0$, $I_{SINK} \leq 4\ mA$			700			700	mV
Output Leakage Current	$V_{IN+} \geq 1V$, $V_{IN-} = 0$, $V_O = 30V$			1.0			1.0	µA
Differential Input Voltage [10]	Keep all V_{IN}s ≥ 0V (or $-V_S$, if used) [7]			36			36	V

See Notes on page 5-27

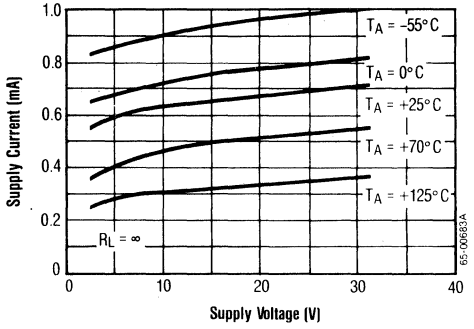
Electrical Characteristics (Continued)

Notes:

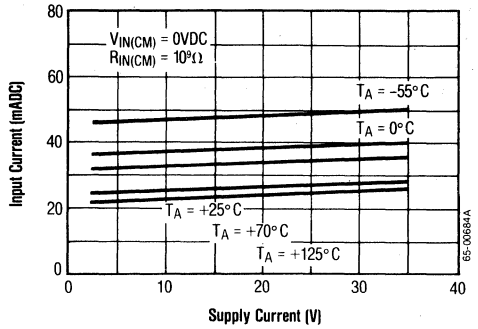
1. Short circuits from the output to $+V_S$ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of $+V_S$.
2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the $+V_S$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output sates will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.
3. These specifications apply for $+V_S$ = 5V and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. The LM339 temperature specifications are limited to $0°C \leq T_A \leq +70°C$.
4. The direction of the input current is out of the IC due to the PNP input state. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
5. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is $+V_S$ -1.5V, but either or both inputs can go to +30V without damage.
6. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 nS can be obtained. See Typical Performance Characteristics section.
7. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. the low input voltage state must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
8. At output switch point, V_O = 1.4V, RS = 0Ω with $+V_S$ from 5V to 30V; and over the full input common mode range (V_O to $+V_S$ -1.5V).
9. For input signals that exceed $+V_S$, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.
10. Guaranteed by design.

Typical Performance Characteristics

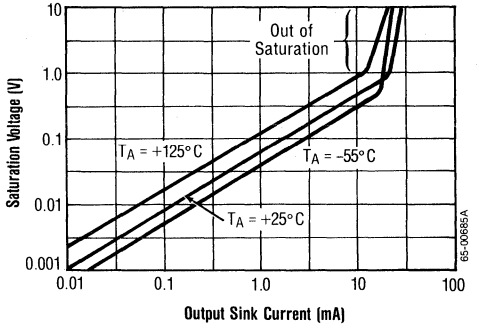
Supply Current



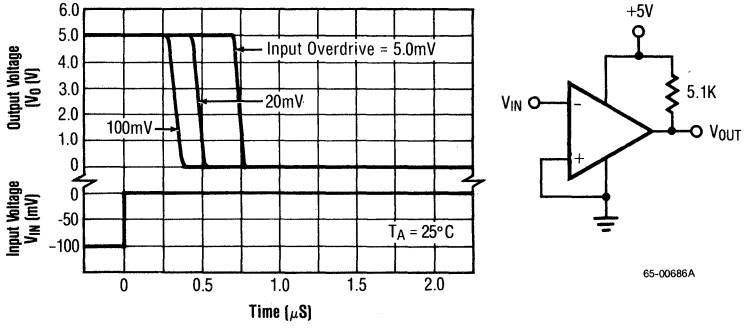
Input Current



Output Saturation Voltage

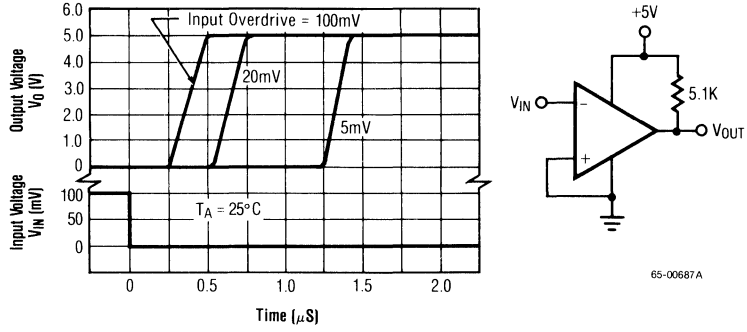


Response Time for Various Input Overdrives Negative Transition

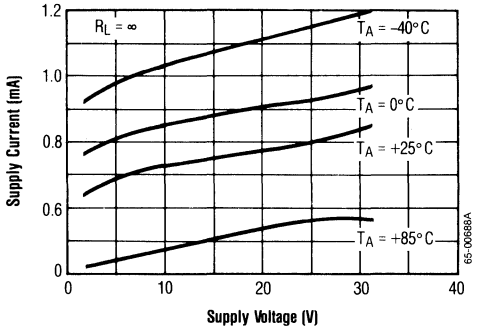


Typical Performance Characteristics (Continued)

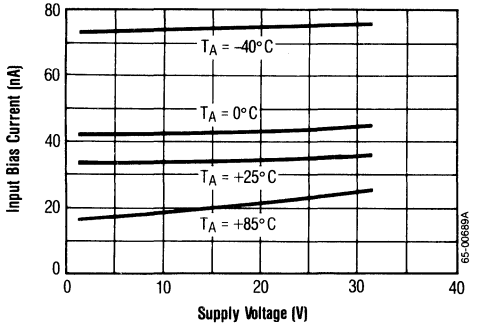
Response Time for Various Input Overdrive Positive Transition



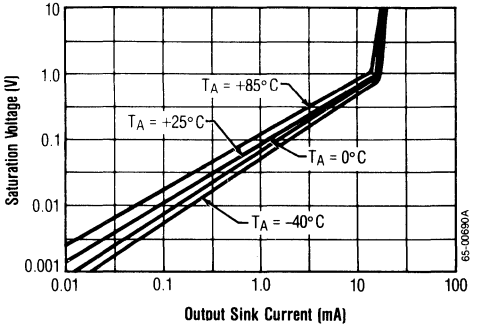
Supply Current



Input Current

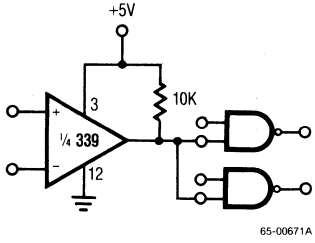


Output Saturation Voltage

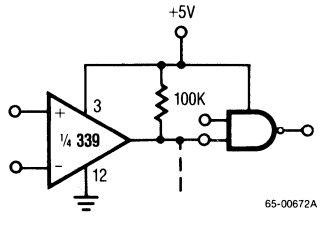


Typical Applications — Single Supply ($+V_S = +15V$)

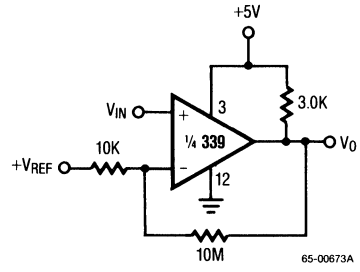
Driving TTL



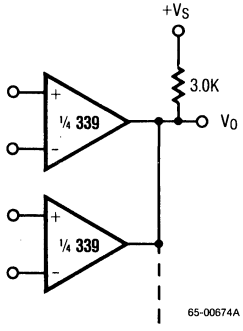
Driving CMOS



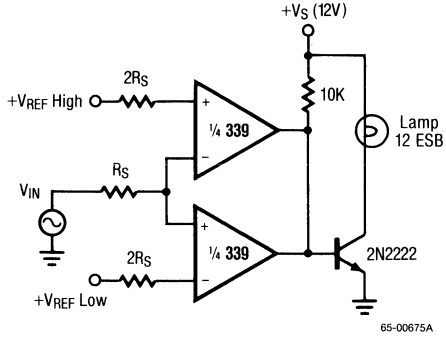
Comparator With Hysteresis



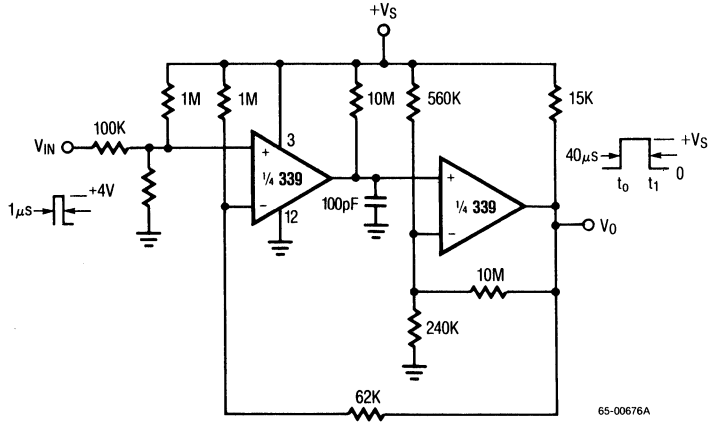
ORing the Output



Limit Comparator

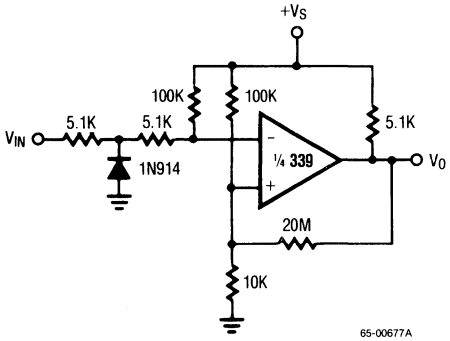


One-Shot Multivibrator With Input Lock Out

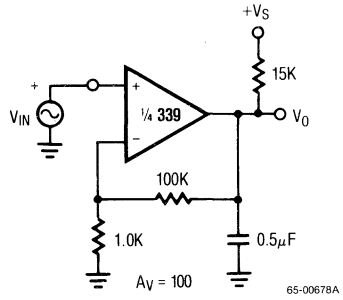


Typical Applications — Single Supply (Continued)

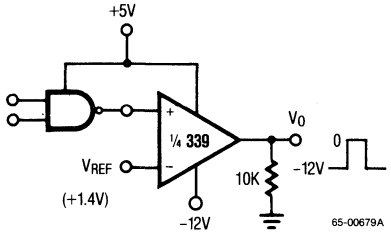
Zero Crossing Detector (Single Power Supply)



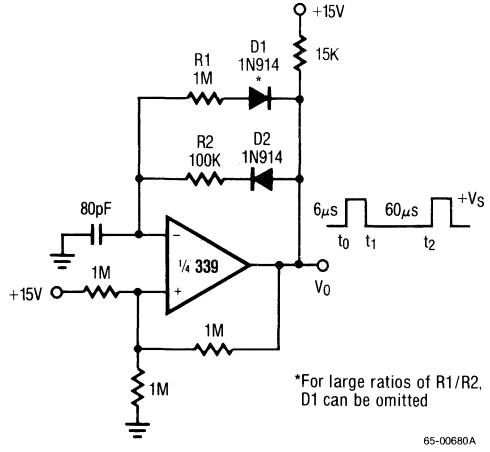
Low Frequency Op Amp



TTL to MOS Logic Converter

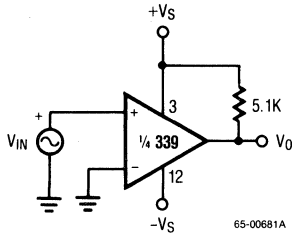


Pulse Generator

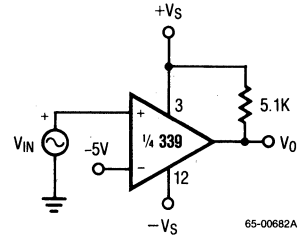


Typical Applications — Single Supply ($+V_S$ = +15V and $-V_S$ = -15V)

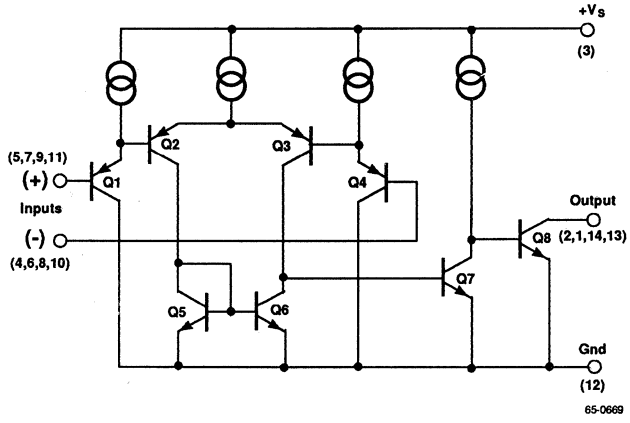
Zero Crossing Detector



Comparator With a Negative Reference



Schematic Diagram (1/4 Shown)



LP165/365 Micropower Programmable Quad Comparator

Features

- Single programming resistor tailors power, input currents, speed, and output current characteristics
- Uncommitted emitters allow logic interface flexibility
- Wide supply voltage range or dual supplies (4V to 36V, or ±2V to ±18V)
- Input common mode range includes ground in single supply applications
- Low power consumption (10μW per comparator at V_S = 5V, I_{SET} = 0.5μA)

Description

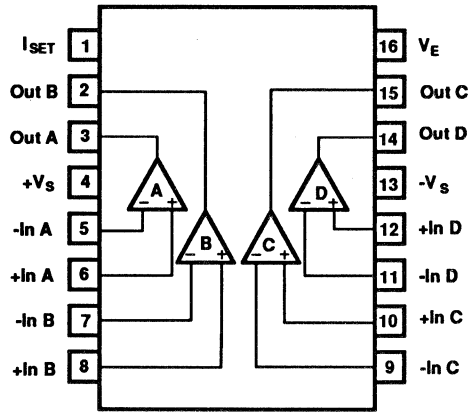
The LP165/365 consists of four independent voltage comparators constructed monolithically using a bipolar transistor fabrication process. These comparators are functionally similar to the 139 series of comparators, but feature programmability and an uncommitted output emitter connection. Programmability gives the user ability to adjust supply current drain and so control power dissipation. At higher values of programming (I_{SET}) current the supply current will increase, response time and output drive capability will improve, and input bias currents will increase. At lower values of I_{SET} supply current and power dissipation will decrease, the response time slows, and input bias currents improve. The uncommitted output emitter connection allows flexibility to interface with various logic families, such as TTL, DTL, CMOS, NMOS, and PMOS.

These comparators can be operated from a single or split power supply; the inputs have a common mode range that includes the negative supply voltage (ground in single supply applications).

Applications include battery-powered circuits, threshold detectors, zero crossing detectors, multivibrators, VCOs, and digital interface circuits.

Connection Information

16-Lead DIP (Top View)



65-2191

Pin	Function
1	Set Current
2	Output B
3	Output A
4	$+V_S$
5	-Input A
6	+Input A
7	-Input B
8	+Input B
9	-Input C
10	+Input D
11	-Input D
12	+Input D
13	$-V_S$
14	Output D
15	Output C
16	Emitter Common

Absolute Maximum Ratings

Supply Voltage ..... 36V or ±18V
Differential Input Voltage 36V
Input Voltage ..... -0.3V to +36V (single supply)*
Output Short Circuit
Duration to V_E ..... Indefinite**
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
LP165 ..... -55°C to +125°C
LP365/LP365A ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

*The input voltage is not allowed to go 0.3V above $+V_S$ or -0.3V below $-V_S$ as this will turn on a parasitic transistor causing large currents to flow through the device.
**Short circuits from the output to $+V_S$ may cause excessive heating and eventual destruction. The current in the output leads and the V_E lead should not be allowed to exceed 30 mA. The output should not be shorted to $-V_S$ if $V_E \geq (-V_S) + 7V$.

Ordering Information

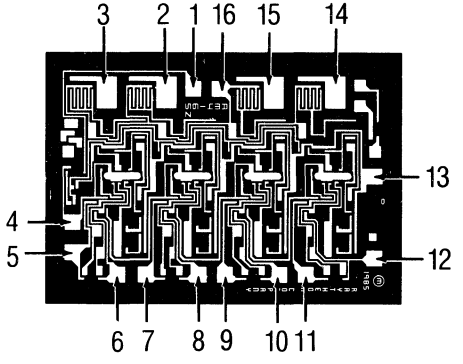
Part Number	Package	Operating Temperature Range
LP365N	N	0°C to +70°C
LP365AN	N	0°C to +70°C
LP165D	D	-55°C to +125°C
LP165D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 16-lead plastic DIP
D = 16-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Thermal Characteristics

	16 Lead Plastic DIP	16 Lead CeramicDIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A <50°C	555mW	1042mW
Therm. Res θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	135°C/W	120°C/W
For T_A >50°C Derate at	7.41 mW/°C	8.33 mW/°C

Mask Pattern



Die Size: 60 x 86 mils
Min. Pad Dimensions: 4 x 4 mils
65-02218A

Electrical Characteristics (V_S = +5V, I_{SET} = 10 µA, and T_A = +25°C)

Parameters	Test Conditions	LP165/LP365A			LP365			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{CM} = 0V, R_S = 100Ω		1	3		2	6	mV
Input Offset Current	V_{CM} = 0V		2	20		4	25	nA
Input Bias Current	V_{CM} = 0V		10	50		15	75	nA
Large Signal Voltage Gain	V_O = 1 to 4V, R_L = 100 kΩ	50	500		25	500		V/mV
Input Voltage Range		0		3	0		3	V
Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3V	75	85		75	85		dB
Power Supply Rejection Ratio	±2.5 ≤ V_S ≤ +3.5V	65	75		65	75		dB
Supply Current	Output High, Open Load		230	250		230	275	µA
Output Voltage High	V_C = 5V, V_E = 0, R_L = 100 kΩ	4.9			4.9			V
Output Voltage Low	V_E = 0, I_{SINK} = 0.8mA	0.4			0.4			V
Output Leakage Current	V_C = 5V, V_E = 0V		2	50		2	100	nA
Output Sink Current	V_E = 0V, V_O = 0.4V	1.2	2.4		0.8	2		mA
Response Time	V_{CC} = 5V, V_E = 0V, R_L = 5kΩ C_L = 10pF, 100mV Step With 5mV Overdrive		4			4		µS

Electrical Characteristics (-55°C ≤ T_A ≤ +125°C for the LP165; 0°C ≤ T_A ≤ +70°C for the LP365/365A; V_S = +5V, I_{SET} = 10 µA over operating temperature range)

Parameters	Test Conditions	LP165/LP365A			LP365			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{CM} = 0V, R_S = 100Ω		1	6		3	9	mV
Input Offset Current	V_{CM} = 0V		2	50		4	75	nA
Input Bias Current	V_{CM} = 0V		10	125		15	200	nA
Large Signal Voltage Gain	V_O = 1 to 4V, R_L = 100 kΩ	50	500		25	500		V/mV
Input Voltage Range		0		3	0		3	V
Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3V	70	85		70	80		dB
Power Supply Rejection Ratio	±2.5 ≤ V_S ≤ +3.5V	65	75		65	70		dB
Supply Current	Output High, Open Load		230	300		230	300	µA
Output Voltage High	V_C = 5V, V_E = 0, R_L = 100 kΩ		4.9	4.5		4.9	4.5	V
Output Voltage Low	V_E = 0, I_{SINK} = 0.4mA		0.2	0.4		0.2	0.4	V
Output Leakage Current	V_C = 5V, V_E = 0V		30	5000		30	5000	nA
Output Sink Current	V_E = 0V, V_O = 0.4V	0.6	2.4		0.4	2		mA

Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 100\ \mu A$, and $T_A = +25°C$)

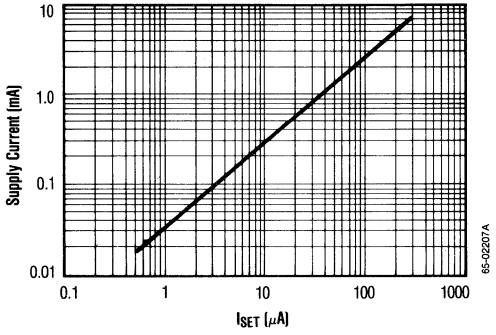
Parameters	Test Conditions	LP165/LP365A			LP365			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100\Omega$		1	3		2	6	mV
Input Offset Current	$V_{CM} = 0V$		5	50		10	90	nA
Input Bias Current	$V_{CM} = 0V$		60	200		80	300	nA
Large Signal Voltage Gain	$V_O = 1$ to 4V, $R_L = 15\ k\Omega$	100	500		100	500		V/mV
Input Voltage Range		-15		+13	-15		+13	V
Common Mode Rejection Ratio	$-15V \le V_{CM} \le +13V$	75	85		75	85		dB
Power Supply Rejection Ratio	$\pm 10V \le V_S \le \pm 15V$	70	85		70	85		dB
Supply Current	$R_L = \infty$, Output High		2.8	3.0		2.8	3.5	mA
Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100\ k\Omega$	4.9	4.95		4.9	4.95		V
Output Voltage Low	$V_E = 0$		0.2	0.4		0.2	0.4	V
Output Leakage Current	$V_C = 15V$, $V_E = -15V$		5	50		5	50	nA
Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	8	10		6	7.5		mA
Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5\ k\Omega$ $C_L = 10pF$, 100mV Step With 5mV Overdrive		1			1		μS

Electrical Characteristics (-55°C ≤ T_A ≤ +125°C for the LP165; 0°C ≤ T_A ≤ +70°C for the LP365/365A; $V_S = \pm 15V$, $I_{SET} = 100\ \mu A$)

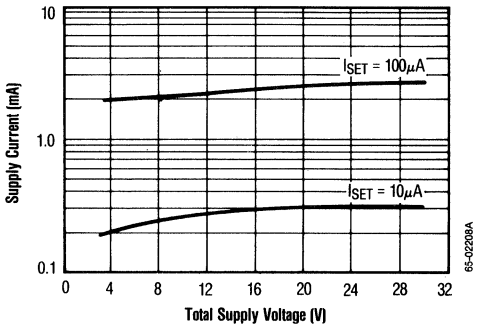
Parameters	Test Conditions	LP165/LP365A			LP365			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100\Omega$		1	6		3	9	mV
Input Offset Current	$V_{CM} = 0V$		5	100		10	200	nA
Input Bias Current	$V_{CM} = 0V$		60	500		60	500	nA
Large Signal Voltage Gain	$V_O = 1$ to 4V, $R_L = 15\ k\Omega$	100	500		100	500		V/mV
Input Voltage Range		-15		+13	-15		+13	V
Common Mode Rejection Ratio	$-15 \le V_{CM} \le +13V$	70	85		70	85		dB
Power Supply Rejection Ratio	$\pm 10V \le V_S \le +15V$	70	80		70	75		dB
Supply Current	$R_L = \infty$, Output High		2.8	3.3		2.8	3.7	mA
Output Voltage High	$V_C = 5V$, $V_E = 0$, $R_L = 100\ k\Omega$	4.5	4.95		4.5	4.95		V
Output Voltage Low	$V_E = 0$		0.2	0.4		0.2	0.4	V
Output Leakage Current	$V_C = 15V$, $V_E = -15V$		30	5000		30	5000	nA
Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	5.5	7		4	5		mA

Typical Performance Characteristics

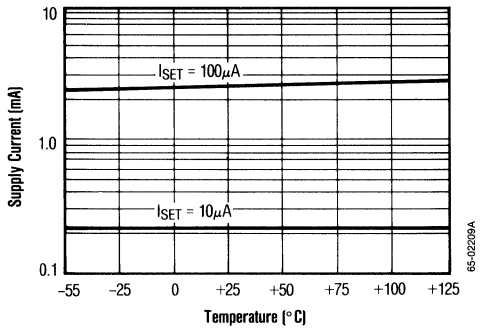
Supply Current vs. I_{SET}



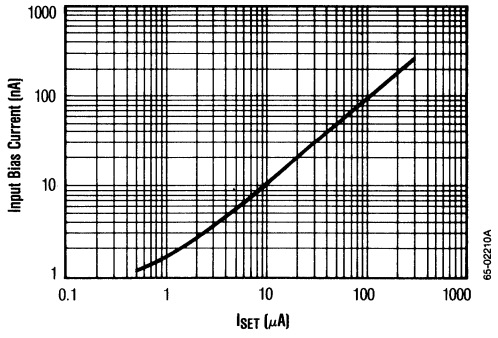
Supply Current vs. Supply Voltage



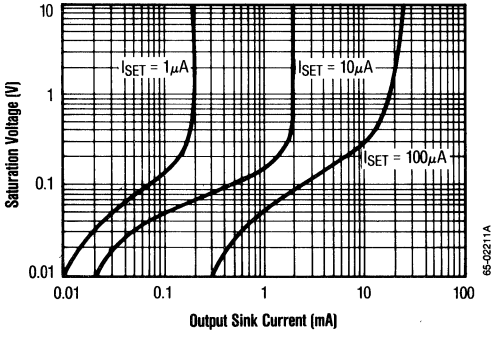
Supply Current vs. Temperature



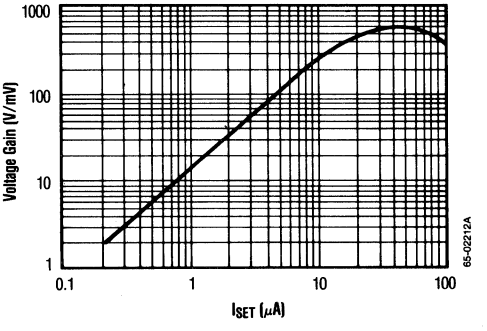
Input Bias Current vs. I_{SET}



Output Saturation Voltage

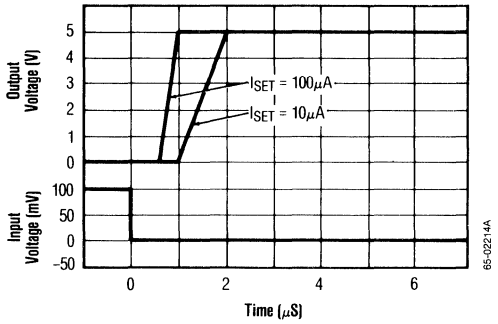


Voltage Gain vs. I_{SET}

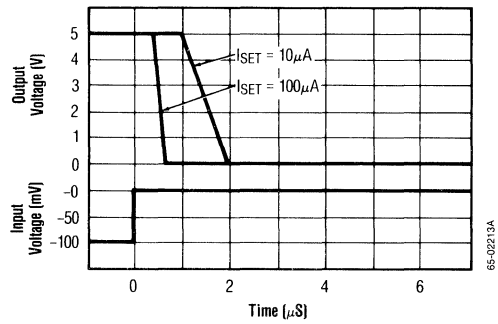


Typical Performance Characteristics (Continued)

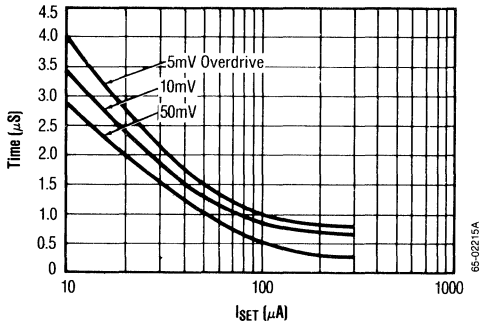
LP165/365 Response Time Negative Transition
T_A = +25°C, ±5V, 5mV Overdrive



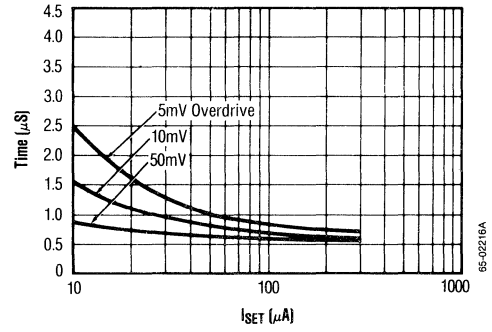
LP165/365 Response Time Positive Transition
T_A = +25°C, ±5V, 5mV Overdrive



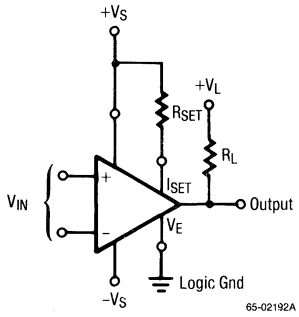
Response Time Negative Transition



Response Time Positive Transition



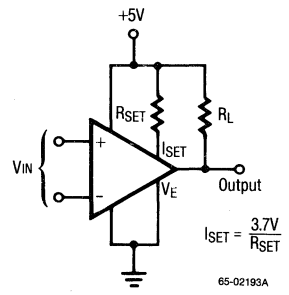
Typical Applications



$$I_{SET} = \frac{(+V_S) - (-V_S) - 1.3V}{R_{SET}}$$

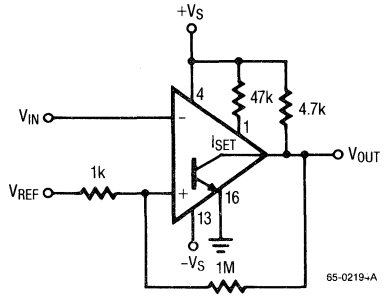
$$I_{supply} \approx 22 \times I_{SET}$$

Split Supply With Logic Output



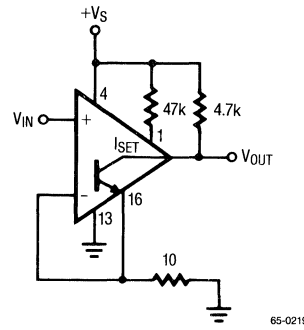
$$I_{SET} = \frac{3.7V}{R_{SET}}$$

TTL Supply — TTL Output



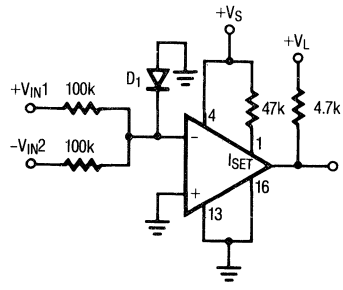
It is a good practice to add a few millivolts of positive feedback to prevent oscillation when the input voltage is near the threshold.

Ordinary Hysteresis



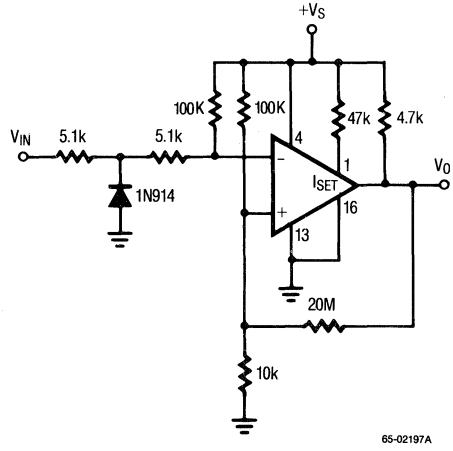
Positive feedback from the emitter can also prevent oscillations when V_{IN} is near the threshold. Can only be used with one section of four.

Hysteresis From Emitter



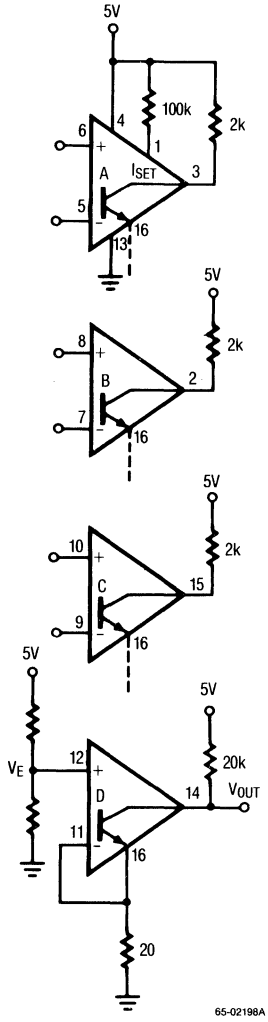
D_1 = Small signal Schottky or low V_D equivalent

Opposite Polarity Magnitude Comparator (Single Supply)



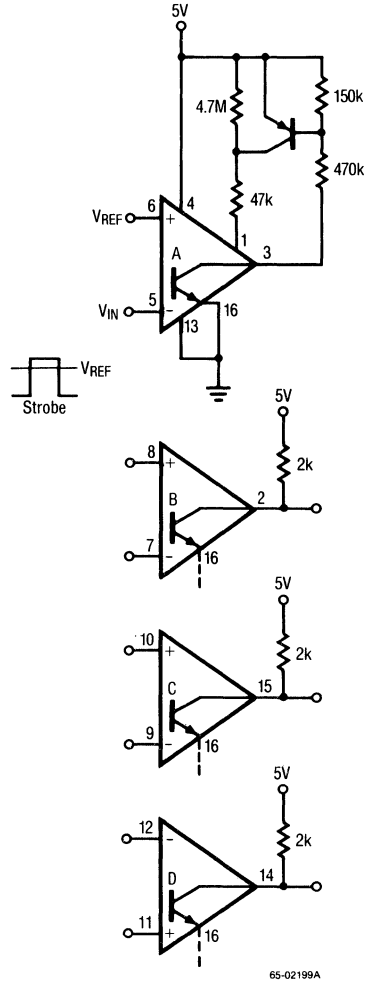
Zero Crossing Detector (Single Supply)

Typical Applications (Continued)



If you choose V_E = 25mV, 75mV, or 125mV, then V_{OUT} will fall if 1/3, 2/3 or all of the other three outputs are low.

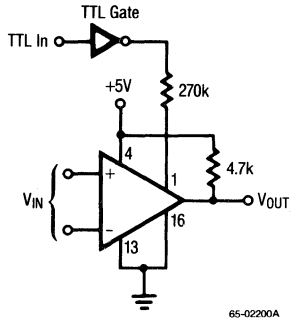
Voting Comparator



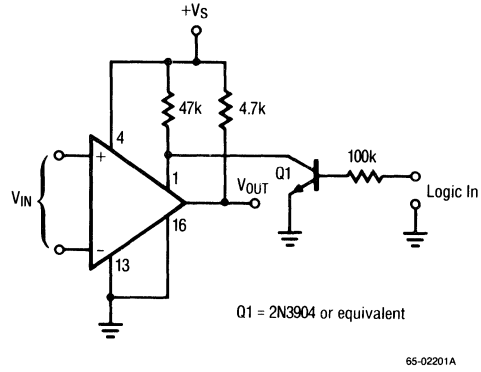
Comparators B, C, and D do not respond until activated by the signal applied to comparator A.

Level Sensitive Strobe

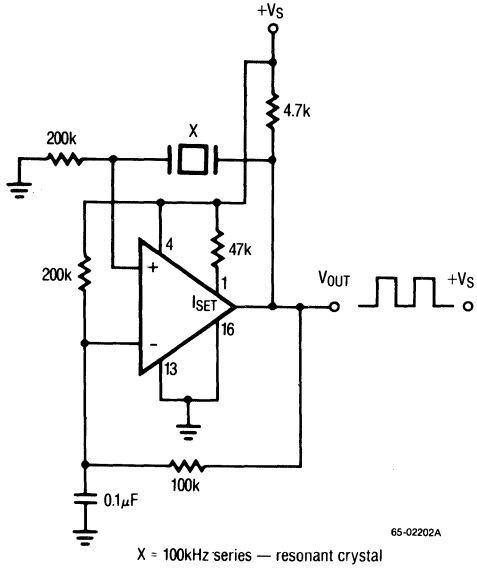
Typical Applications (Continued)



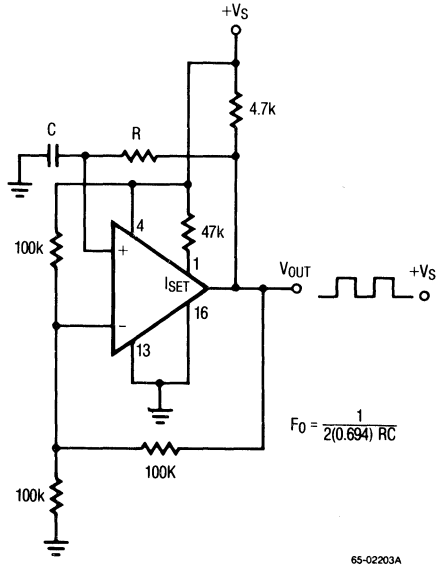
Chip Disable (TTL)



Chip Disable (Transistor)

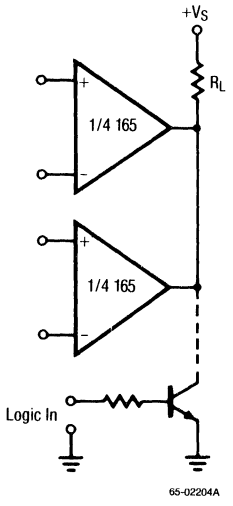


Crystal Controlled Oscillator (Single Supply)

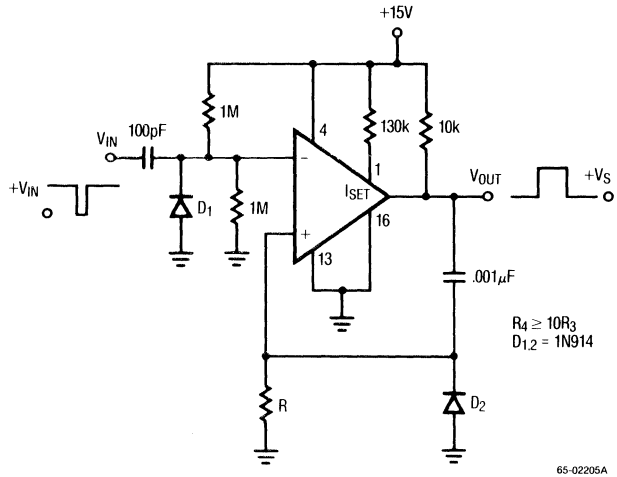


Squarewave Oscillator

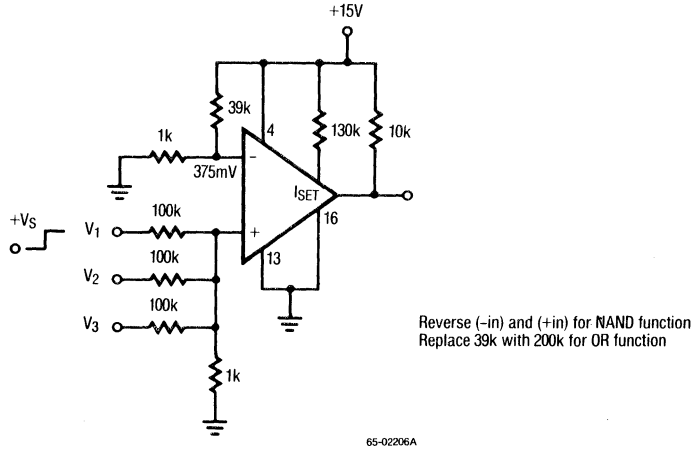
Typical Applications (Continued)



Wired-OR Outputs

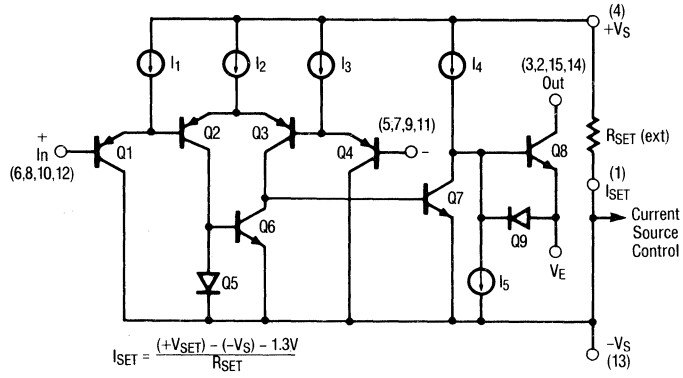


One Shot Multivibrator



3 Input AND Gate

Simplified Schematic Diagram



SECTION 6

DIGITAL-TO-ANALOG CONVERTERS

DEFINITIONS

Differential Nonlinearity (DNL)
The incremental error from an ideal 1 LSB analog output change when the input is changed 1 LSB; guaranteed monotonicity requires the differential nonlinearity error to be less than 1 LSB. Differential nonlinearity is expressed as a percentage of the full scale output.

Full Scale Current (I_{FS})
The maximum current that can be obtained from the output, for a specified reference current, measured in milliamps (mA). A typical binary D/A produces its full scale output with all ones applied at the input.

Full Scale Symmetry
The difference between the full scale output values of the two outputs of a complementary output D/A, expressed in microamps (μA).

Gain Temperature Coefficient
The variation of full scale current measured over a specified temperature range, expressed in parts per million per degree C (ppm/° C).

$$\text{Gain TC} = \left(\frac{I_{FS} @ T_{(1)} - I_{FS} @ T_{(2)}}{T_{(1)} - T_{(2)}}\right)\left(\frac{10^6}{I_{FS}}\right)$$

Where $T_{(1)}$ and $T_{(2)}$ are the upper and lower limits of the specified temperature range.

Least Significant Bit (LSB)
The digital input line which has the smallest effect on the analog output. LSB can also refer to the measure of the analog output change when the input code is incremented; in that case, the ideal value of 1 LSB is calculated as:

$$1 \text{ LSB} = \left(\frac{1}{2^N}\right)(\text{Full Scale Range}) \text{ in V or mA}$$

where N is the resolution of the converter.

Logic Input Current
The input current into the logic switch at a specified applied voltage, expressed in microamps (μA).

Logic Input Levels
The range of voltages within which the logic trip level is guaranteed to be expressed in volts (V).

Monotonicity
For any one LSB increase in input code the D/A output either increases or remains constant.

Nonlinearity
The difference between the actual analog output and an imaginary straight line drawn between the measured zero scale and full scale readings, for any code combination. Nonlinearity is expressed as a percentage of the full scale output.

DEFINITIONS (Continued)

Output Capacitance
The value of the internal parasitic capacitances, modeled as a single capacitor from the output to ground, expressed in picofarads (pF).

Output Voltage Compliance
The range of voltages over which the output can be driven while maintaining nonlinearity specifications, measured in volts (V).

Power Consumption
The DC power required to operate the D/A converter with a specified reference current, expressed in milliwatts (mW).

Power Supply Sensitivity
The ratio of change in the full scale output to a change in supply voltage, measured in percent of full scale per percent change in supply voltage (%ΔFS/%ΔV).

Propagation Delay
The time delay between a step input to all inputs and a change in the output, from the 50% point of TTL input swing to the 50% point of the final output value. Propagation delay is expressed in nanoseconds (nS).

Reference Bias Current
The input current to the reference amplifier which subtracts from the reference current, expressed in microamps (μA).

Reference Current Range
The range of currents into the reference terminal over which the D/A converter is guaranteed to meet the resolution specification, measured in milliamps (mA).

Reference Input Slew Rate
The average rate of change of the output current for a step change at the reference input, expressed in milliamps per microsecond (mA/μS).

Resolution
The number of inputs or bits. The number of discrete steps or states at the output is equal to 2^N, where N is the resolution of the converter.

Settling Time
The time delay between a 50% of TTL level change at all logic inputs to the point where the output settles within a specified error band of its final value, for either full scale to zero scale or zero scale to full scale changes. Settling time is measured in nanoseconds or microseconds (nS or μS).

Supply Current
The current required from the power supply to operate the D/A converter under specified supply voltage and reference current conditions, expressed in milliamps (mA).

Supply Voltage
The range of power supply voltages over which the D/A converter is guaranteed to meet the resolution specification, expressed in volts (V).

Zero Scale Current
The leakage current flowing into the D/A converter output with all logic inputs off and the output at a specified voltage, expressed in microamps (μA).

DAC-08 8-Bit High Speed Multiplying D/A Converter

Features

- Fast settling output current — 85nS
- Full scale current prematched to ±1.0 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% max. over temperature range
- High output impedance and compliance — -10V to +18V
- Differential current outputs
- Wide range multiplying capability — 1.0MHz bandwidth
- Low FS current drift — ±10ppm/°C
- Wide power supply range — ±4.5V to ±18V
- Low power consumption — 33mW @ ±5.0V
- Low cost

Description

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85nS settling times with very low "glitch" and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications.

Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

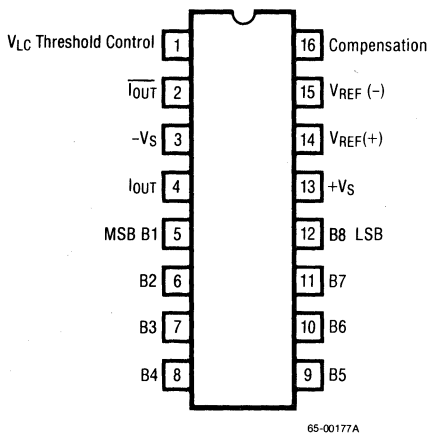
High voltage compliance dual complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 33mW power consumption attainable at ±5.0V supplies.

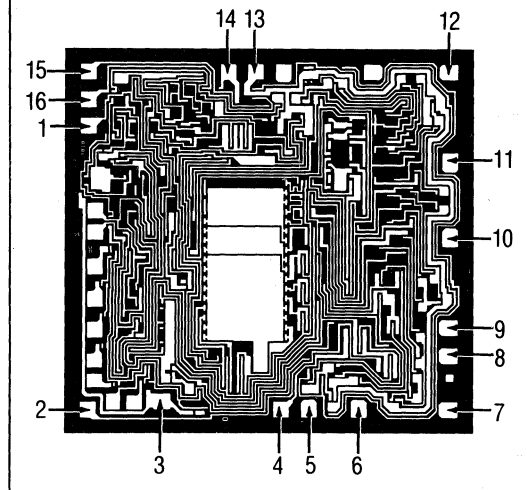
The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1.0μS A/D converters, servo-motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high speed modems and other applications where low cost, high speed and complete input/output versatility are required.

Connection Information

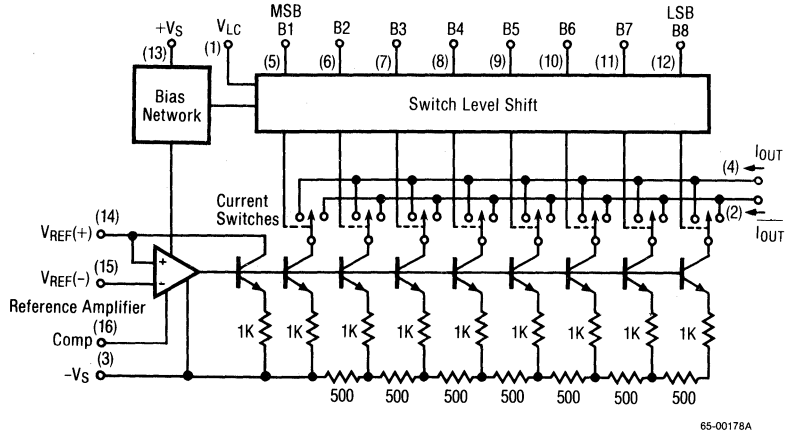


Mask Pattern



Die Size: 94 x 100 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram



Ordering Information

Part Number	Package	Operating Temperature Range	Non-linearity
DAC-08HN	N	0°C to +70°C	±0.1%
DAC-08EN	N	0°C to +70°C	±0.19%
DAC-08CN	N	0°C to +70°C	±0.39%
DAC-08AD	D	-55°C to +125°C	±0.1%
DAC-08D	D	-55°C to +125°C	±0.19%
DAC-08D/883B	D	-55°C to +125°C	±0.19%
DAC-08AD/883B	D	-55°C to +125°C	±0.1%

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N= 16-lead plastic DIP
D =16-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Thermal Characteristics

	16-Lead Ceramic DIP	16-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	1042 mW	555 mW
Therm. Res θ_{JC}	60°C/W	—
Therm. Res. θ_{JA}	120°C/W	135°C/W
For T_A >50°C	8.38 mW	7.41 mW
Derate at	per °C	per °C

Absolute Maximum Ratings

(T_A = +25°C unless otherwise noted)

Supply Voltage (between $+V_S$ and $-V_S$ 36V
Logic Inputs ..... $-V_S$ to $-V_S$ plus 36V
V_{LC} ..... $-V_S$ to $+V_S$
Analog Current Outputs ..... 4 mA
Reference Inputs (V_{14} to V_{15}) ..... $-V_S$ to $+V_S$
Reference Input Differential
Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) ..... 5.0 mA
Operating Temperature Range
DAC-08AD, D ..... -55°C to +125°C
DAC-08HN, EN, CN ..... 0°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Electrical Characteristics (V_S = ±15V, I_{REF} = 2.0mA, T_A = -55°C to +125°C for DAC-08 and DAC-08A; T_A = 0°C to +70°C for DAC-08C, DAC-08E and DAC-08H unless other specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.)

Parameters	Test Conditions	DAC-08A/-08H			DAC-08			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			±0.1			±0.19	%FS
Settling Time	To +½LSB, All Bits Switched ON or OFF T_A = +25°C (See Note)		85	135		85	150	nS
Propagation Delay Each Bit	T_A = +25°C (See Note)		35	60		35	60	nS
All Bits Switched			35	60		35	60	nS
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < ½LSB R_{OUT} > 20MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Scale Summetry	I_{FS4}-I_{FS2}		±0.5	±4.0		±1.0	±8.0	μA
Zero Scale Current			0.1	1.0		0.2	2.0	μA
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5.000kΩ	V_{REF} = +25V, $-V_S$ = -12V	4.2			4.2			mA
Logic Input Levels Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			V
Logic Input Current Logic "0"	V_{LC} = 0V V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	μA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	μA
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range (See Note)	V_S = ±15V	-10		+13.5	-10		+13.5	V
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	μA
Reference Input Slew Rate (See Note)		4.0	8.0		4.0	8.0		mA/μS

Note: Guaranteed by Design

Electrical Characteristics (Continued)

Parameters	Test Conditions	DAC-08A/-08H			DAC-08			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Sensitivity Positive	$+V_S$ = 4.5V to 18V $-V_S$ = -4.5V to -18V I_{REF} = 1.0mA		±0.0003	±0.01		±0.0003	±0.01	$\frac{\%\Delta FS/}{\%\Delta V}$
Negative			±0.002	±0.01		±0.002	±0.01	%/%
Power Supply Current Positive	V_S = ±5.0V, I_{REF} = 1.0mA		2.3	3.8		2.3	3.8	mA
Negative			-4.3	-5.8		-4.3	-5.8	mA
Positive	V_S = +5.0V, -15V, I_{REF} = 2.0mA		2.4	3.8		2.4	3.8	mA
Negative			-6.4	-7.8		-6.4	-7.8	mA
Positive	V_S = ±15V, I_{REF} = 2.0mA		2.5	3.8		2.5	3.8	mA
Negative			-6.5	-7.8		-6.5	-7.8	mA
Power Consumption	V_S = ±5.0V, I_{REF} = 1.0mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0mA		108	136		108	136	mW
	V_S = ±15V, I_{REF} = 2.0mA		135	174		135	174	mW

Parameters	Test Conditions	DAC-08E			DAC-08C			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Nonlinearity	Full Temperature Range			+0.19			+0.39	%FS
Settling Time	To +½LSB, All Bits Switched ON or OFF T_A = +25°C (See Note)		85	150		85	150	nS
Propagation Delay Each Bit	T_A = +25°C		35	60		35	60	nS
All Bits Switched	(See Note)		35	60		35	60	nS
Full Scale Tempco			±10	±50		±10	±80	ppm/°C
Output Voltage Compliance	Full Scale Current Change < ½LSB R_{OUT} > 20MΩ Typical	-10		+18	-10		+18	V
Full Scale Current	V_{REF} = 10.000V R_{14}, R_{15} = 5.000kΩ T_A = +25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Summetry	I_{FS4}-I_{FS2}		±1.0	±8.0		±2.0	±16.0	μA

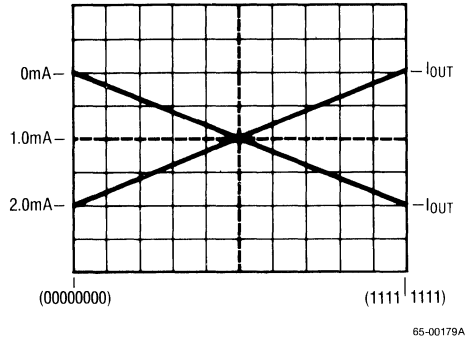
Electrical Characteristics (Continued)

Parameters	Test Conditions	DAC-08E			DAC-08C			Units
		Min	Typ	Max	Min	Typ	Max	
Zero Scale Current			0.2	2.0		0.2	4.0	μA
Output Current Range	V_{REF} = +15V, $-V_S$ = -10V	2.1			2.1			mA
R_{14}, R_{15} = 5.000kΩ	V_{REF} = +25V, $-V_S$ = -12V	4.2			4.2			mA
Logic Input Levels								
Logic "0"	V_{LC} = 0V			0.8			0.8	V
Logic "1"		2.0			2.0			V
Logic Input Current	V_{LC} = 0V							
Logic "0"	V_{IN} = -10V to +0.8V		-2.0	-10		-2.0	-10	μA
Logic "1"	V_{IN} = 2.0V to 18V		0.002	10		0.002	10	μA
Logic Input Swing	$-V_S$ = -15V	-10		+18	-10		+18	V
Logic Threshold Range (See Note)	V_S = ±15V	-10		+13.5	-10		+13.5	V
Reference Bias Current			-1.0	-3.0		-1.0	-3.0	μA
Reference Input Slew Rate (See Note)		4.0	8.0		4.0	8.0		mA/μS
Power Supply Sensitivity	$+V_S$ = 4.5V to 18V							
Positive	$-V_S$ = -4.5V to -18V		±0.0003	±0.01		±0.0003	±0.01	%ΔFS/%ΔV
Negative	I_{REF} = 1.0mA		±0.002	±0.01		±0.002	±0.01	
Power Supply Current								
Positive	V_S = ±5.0V,		2.3	3.8		2.3	3.8	mA
Negative	I_{REF} = 1.0mA		-4.3	-5.8		-4.3	-5.8	mA
Positive	V_S = +5.0V, -15V,		2.4	3.8		2.4	3.8	mA
Negative	I_{REF} = 2.0mA		-6.4	-7.8		-6.4	-7.8	mA
Positive	V_S = ±15V,		2.5	3.8		2.5	3.8	mA
Negative	I_{REF} = 2.0mA		-6.5	-7.8		-6.5	-7.8	mA
Power Consumption	V_S = ±5.0V, I_{REF} = 1.0mA		33	48		33	48	mW
	V_S = +5.0V, -15V, I_{REF} = 2.0mA		103	136		103	136	mW
	V_S = ±15V, I_{REF} = 2.0mA		135	174		135	174	mW

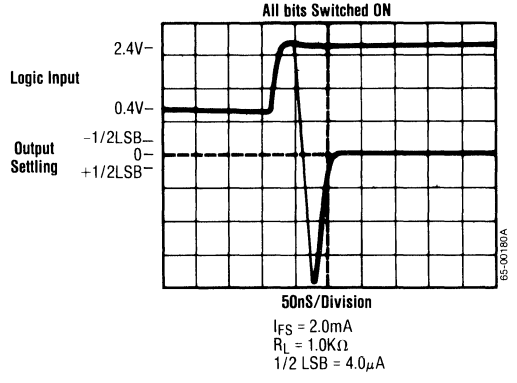
Note: Guaranteed by design

Typical Performance Characteristics

True and Complementary Output Operation

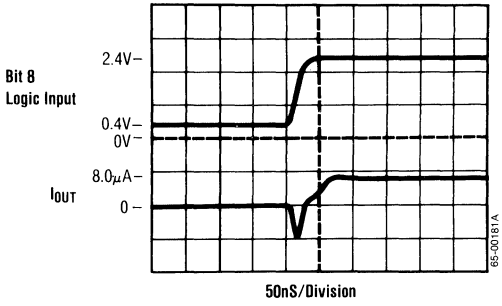


Full Scale Settling Time

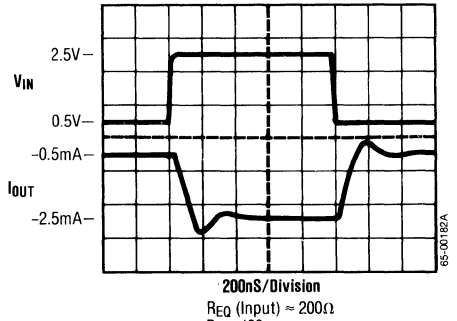


I_{FS} = 2.0mA
R_L = 1.0KΩ
1/2 LSB = 4.0μA

LSB Switching

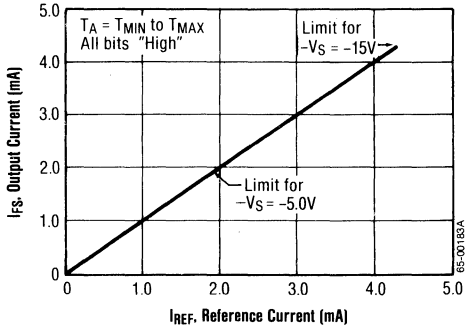


Fast Pulsed Reference Operation



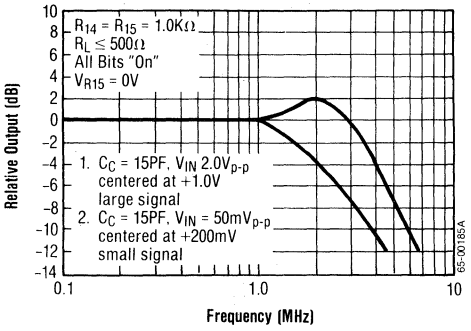
R_{EQ} (Input) ≈ 200Ω
R_L = 100Ω
C_C = 0
R_{IN} = 5.0K
$+V_{IN}$ = 10V

Full Scale Current vs. Reference Current

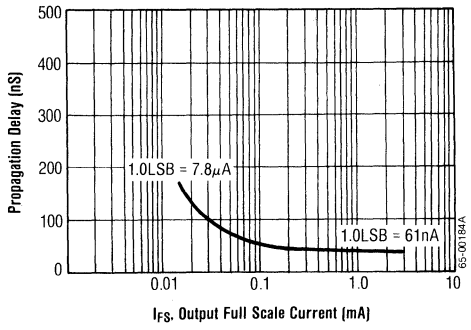


Typical Performance Characteristics (Continued)

Reference Input Frequency Response



LSB Propagation Delay vs. I_{FS}



Applications Information

Reference Amplifier Setup

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common mode range of the reference amplifier is given by: V_{CM-} = $-V_S$ plus (I_{REF} x 1kΩ) plus 2.5V. The positive common mode range is $+V_S$ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to $-V_S$. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

Multiplying Operation

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4.0mA to 4.0μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to $-V_S$. The value of this capacitor depends on the impedance presented to pin 14; for R_{14} values of 1.0, 2.5, and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R_{14} = 1.0kΩ and C_C = 15pF, the reference amplifier slews at 4.0mA/μS enabling a transition from I_{REF} = 0 to I_{REF} = 2.0mA in 500nS.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff (I_{REF} = 0) condition. Full scale transition (0 to 2.0mA) occurs in 120nS when the equivalent impedance at pin 14 is 200Ω and C_C = 0. This yields a reference slew rate of 16mA/μS which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC-08 design incorporates a unique logic input circuit which enbles direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2.0μA logic input current and completely adjustable logic threshold voltage. For $-V_S$ = -15V, the logic inputs may swing between -10V and +18V. This enables direct interface with +5V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: $-V_S$ plus (I_{REF} x 1.0kΩ) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4V above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL an I_{REF} = 1.0mA is recommended. For general setup of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1.0kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above $-V_S$ and is independent of the positive supply. Negative compliance is given by $-V_S$ plus (I_{REF} x 1.0kΩ) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection, and other balanced applications such as driving center-tapping coils and transformers.

Power Supplies

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5.0V or less, $I_{REF} \leq$ 1.0mA is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required. However, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows: $P_d = (I+)\ (+V_S) + (I-)\ (-V_S) + (2\ I_{REF})\ (-V_S)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power bypass capacitors.

Temperature Performance

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at -55°C; at +125°C an increase of about 15% is typical.

Typical Applications

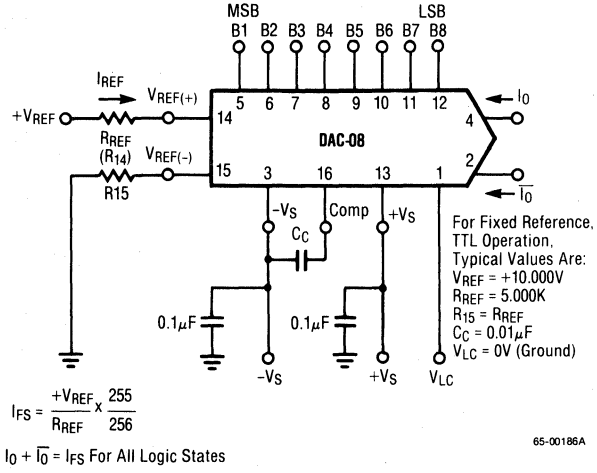


Figure 1. Basic Positive Reference Operation

Typical Applications (Continued)

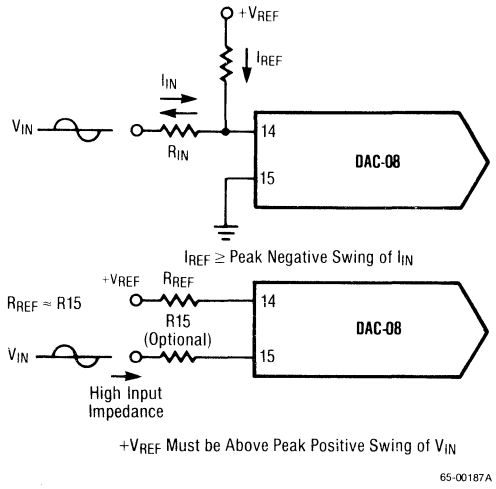


Figure 2. Accommodating Bipolar References

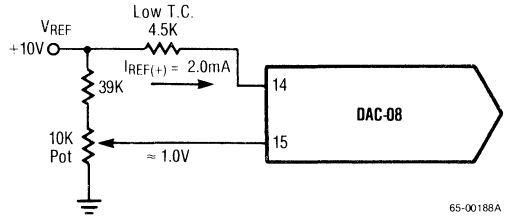
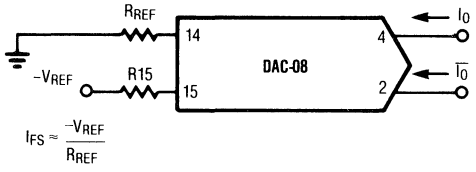


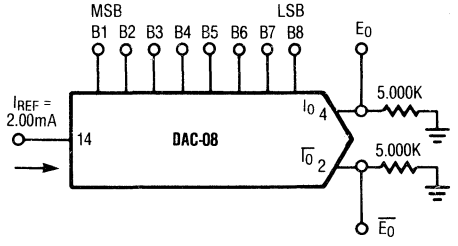
Figure 3. Recommended Full Scale Adjustment Circuit



Note: R_{REF} sets I_{FS}: R15 is for bias current cancellation.

65-00189A

Figure 4. Basic Negative Reference Operation

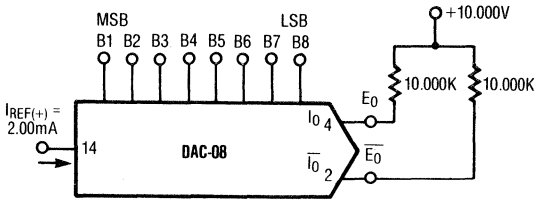


Scale	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

65-00190A

Figure 5. Basic Unipolar Negative Operation

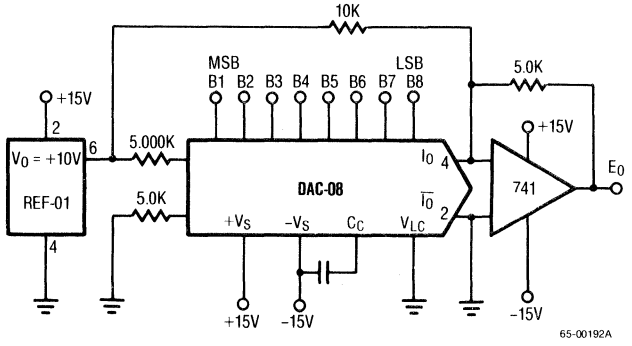
Typical Applications (Continued)



Scale	B1 B2 B3 B4 B5 B6 B7 B8	E_0	$\overline{E_0}$
Pos Full Scale	1 1 1 1 1 1 1 1	-9.920	+10.000
Pos Full Scale -LSB	1 1 1 1 1 1 1 0	-9.840	+9.920
Zero Scale +LSB	1 0 0 0 0 0 0 1	-0.080	+0.160
Zero Scale	1 0 0 0 0 0 0 0	0.000	+0.080
Zero Scale -LSB	0 1 1 1 1 1 1 1	+0.080	0.000
Neg Full Scale +LSB	0 0 0 0 0 0 0 1	+9.920	-9.840
Neg Full Scale	0 0 0 0 0 0 0 0	+10.000	-9.920

65-00191A

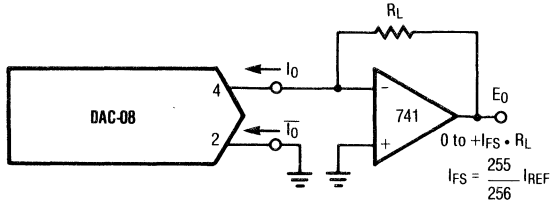
Figure 6. Basic Bipolar Output Operation



65-00192A

Scale	B1 B2 B3 B4 B5 B6 B7 B8	E_0
Pos Full Scale	1 1 1 1 1 1 1 1	+4.960
Zero Scale	1 0 0 0 0 0 0 0	0.00
Neg Full Scale +1 LSB	0 0 0 0 0 0 0 1	-4.960
Neg Full Scale	0 0 0 0 0 0 0 0	-5.000

Figure 7. Offset Binary Operation

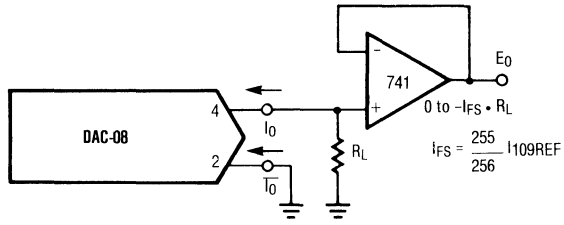


For complementary output (operation as a negative logic DAC), connect inverting input of Op-Amp to I_0 (pin 2); connect I_0 (pin 4) to ground.

65-00193A

Figure 8. Positive Low Impedance Output Operation

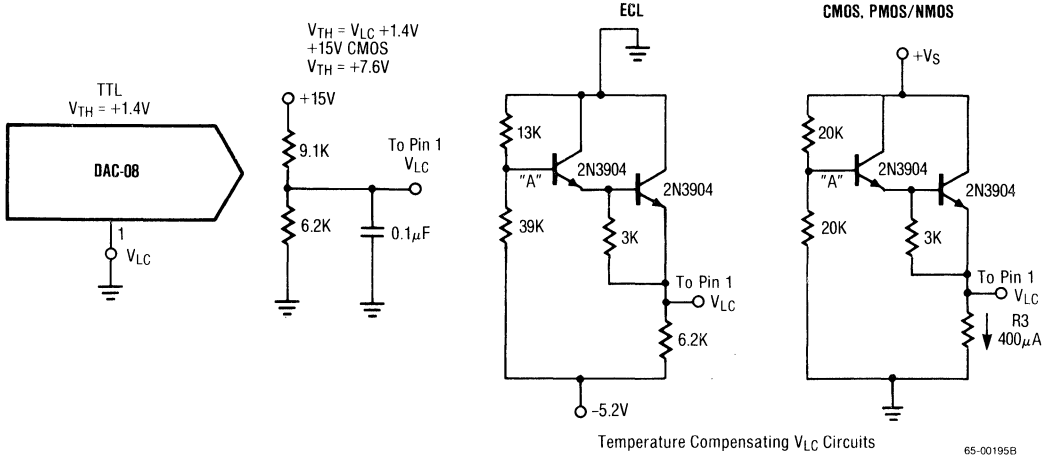
Typical Applications (Continued)



For complementary output (operation as a negative logic DAC), connect non-inverting input of Op-Amp to I_O (pin 2); connect I_O (pin 4) to ground.

65-00194A

Figure 9. Negative Low Impedance Output Operation



Temperature Compensating V_{LC} Circuits

65-00195B

Figure 10. Interfacing With Various Logic Families

Settling Time

The DAC-08 is capable of extremely fast settling times, typically 85nS at I_{REF} = 2.0mA. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35nS for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35nS, with each progressively larger bit taking successively longer. The MSB settles in 85nS, thus determining the overall settling time of 85nS. Settling to 6-bit accuracy requires about 65 to 70nS. The output capacitance of the DAC-08 including the package is approximately 15pF; therefore the output RC time constant dominates settling time if R_L > 500Ω.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4.0μA, therefore a 1.0kΩ load is needed to provided adequate drive for most oscilloscopes. The settling time fixture uses a cascode design to permit driving a 1.0kΩ load with less than 5.0pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value, and thus settling times may be observed at lower values of I_{REF}.

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic state; 0.1μF capacitors at the supply pins provide full transient protection.

Typical Applications (Continued)

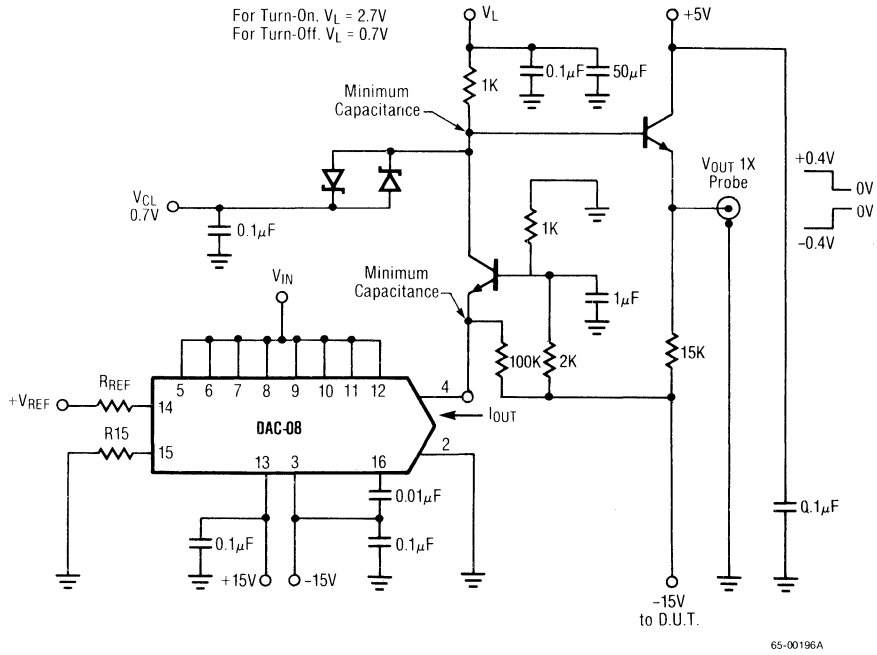


Figure 11. Settling Time Test Fixture

DAC-10
10-Bit High Speed Multiplying D/A Converter

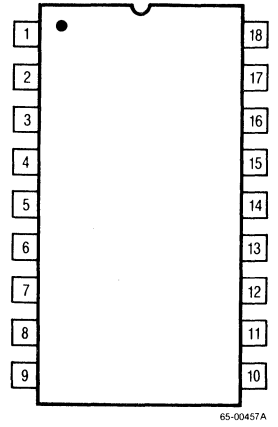
Features
- Nonlinearity to 0.05% max over temperature range
- Low full scale drift — 10ppm/°C
- Wide range multiplying capability — 1.0MHz bandwidth
- Wide power supply range — +5.0V/-7.5V to ±18V
- Two quadrant multiplying
- High output compliance
- High speed — 85nS

Applications
- A/D converters
- Servo controls
- Waveform generators
- Programmable power supplies
- High Speed Modems

Description
The DAC-10 is a high speed, 10-bit, monolithic, multiplying Digital-to-Analog Converter. Settling times of 85nS are achieved with low power consumption and minimal output glitches. Full scale (10-bit) accuracy is achieved. The DAC-10 can be operated from almost any logic level input due to its adjustable (V_{LC}) threshold. Monotonicity is guaranteed to 10 bits and nonlinearities of ±0.05% are guaranteed over the full operating temperature range. Power consumption can be reduced to 85mW by lowering supply voltages to +5.0V to -7.5V. Operation at supply voltages up to ±18V does not appreciably affect device performance. Zener-Zap trimming is performed at wafer probe to optimize the converter's accuracy.

Connection Information

18-Lead
Hermetic Dual In-Line
(Top View)



Pin	Function
1	V_{LC} Trim
2	$\overline{I_O}$
3	$-V_S$
4	I_O
5	MSB B1
6	B2
7	B3
8	B4
9	B5
10	B6
11	B7
12	B8
13	B9
14	B10 LSB
15	$+V_S$
16	$V_{REF(+)}$
17	$V_{REF(-)}$
18	Comp

Absolute Maximum Ratings

Operating Temperature Range
- DAC-10BD, CD ..... -55°C to +125°C
- DAC-10FD, GD ..... 0°C to +70°C

Storage Temperature Range ..... -65°C to +150°C

Lead Soldering Temperature (60 Sec) ..... +300°C

Supply Voltage ($+V_S$ to $-V_S$) ..... +36V

Logic Inputs ..... $-V_S$ to $-V_S$ plus 36V

V_{LC} ..... $-V_S$ to $+V_S$

Analog Current Outputs ..... $-V_S$ to $+V_S$

Reference Inputs (V_{16} to V_{17}) ..... $-V_S$ to $+V_S$

Reference Input Differential Voltage (V_{16} to V_{17}) ..... ±18V

Reference Input Current (I_{16}) 2.5mA

Ordering Information

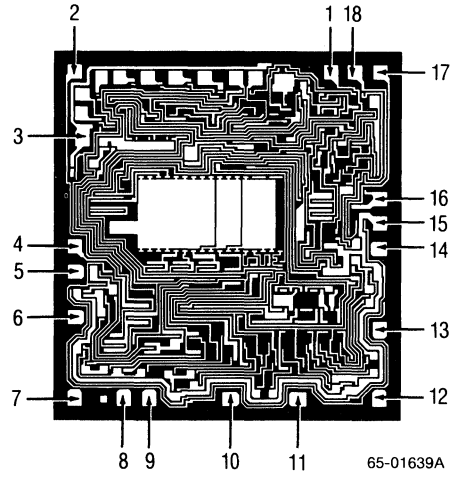
Part Number	Package	Operating Temperature Range	Non-linearity
DAC-10FD	D	0°C to +70°C	±0.05%
DAC-10GD	D	0°C to +70°C	±0.01%
DAC-10BD	D	-55°C to +125°C	±0.05%
DAC-08BD/883B	D	-55°C to +125°C	±0.05%
DAC-08CD	D	-55°C to +125°C	±0.05%
DAC-08CD/883B	D	-55°C to +125°C	±0.05%

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D =18-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Thermal Characteristics

	18-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	1042 mW
Therm. Res θ_{JC}	60°C/W
Therm. Res. θJA	120°C/W
For T_A >50°C Derate at	8.38 mW/°C

Mask Pattern



Die Size: 94 x 100 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics ($V_S = \pm 15V$; $I_{REF} = 2.0mA$, $-55°C \leq T_A \leq +125°C$ for DAC-10B, DAC-10C, $0°C \leq T_A \leq +70°C$ for DAC-10F, DAC-10G. Output characteristics apply to both I_O and $\overline{I_O}$ unless otherwise specified.)

Parameters	Test Conditions	DAC-10B/F			DAC-10C/G			Units
		Min	Typ	Max	Min	Typ	Max	
Monotonicity		10			10			Bits
Nonlinearity			.029	.049		.058	.098	% FS
Differential Nonlinearity			.029	.098		.068		% FS
Output Voltage Compliance	Full Scale Current Change < 1 LSB		-5.5 +10			-5.5 +10		V
Gain Temperature Coefficient	See Note		±10	±25		±10	±50	ppm/°C
Full Scale Current	$V_{REF} = 10.000V$ $R_{16} = R_{17} = 5.000k\Omega$	3.968	3.996	4.024	3.936	3.996	4.056	mA
Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$		0.1	4.0		1.0	4.0	μA
Zero Scale Current			0.01	0.5		0.01	0.5	μA
Reference Input Slew Rate	$R_{EQ} = 200\Omega$, $C_C = 0$		6.0			6.0		mA/μS
Power Supply Sensitivity Positive	$+4.5V \leq +V_S \leq +18V$		0.001	0.01		0.001	0.01	$\%\Delta_{FS}/$
Negative	$-18V \leq -V_S \leq -10V$		0.0012	0.01		0.0012	0.01	$\%\Delta V$
Supply Current Positive	$V_S = \pm 15V$		2.3	4.0		2.3	4.0	mA
Negative	$I_{REF} = 2.0mA$		9.0	15		9.0	15	
Positive	$V_S = +5.0V/-7.5V$;		1.8	4.0		1.8	4.0	
Negative	$I_{REF} = 1.0mA$		5.9	9.0		5.9	9.0	
Power Consumption	$V_S = \pm 15V$ $I_{REF} = 2.0mA$		231	276		231	276	mW
	$V_S = +5.0V/-7.5V$; $I_{REF} = 1.0mA$		85	107		85	107	
Logic Input Levels Low	$V_{LC} = 0$			0.8			0.8	V
High		2.0			2.0			
Logic Input Currents Low	$V_{LC} = 0$; $-5.0V \leq V_{IN} \leq +0.8V$	-10	-5.0		-10	-5.0		μA
High	$+2.0V \leq V_{IN} \leq +18V$		0.001	10		0.001	10	

Note: Guaranteed by Design.

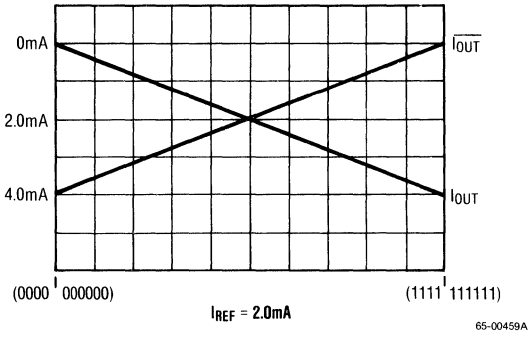
Electrical Characteristics ($V_S = \pm 15V$; $I_{REF} = 2.0mA$; $T_A = +25°C$, unless otherwise noted. Output characteristics apply to both I_O and $\overline{I_O}$.)

Parameters	Test Conditions	DAC-10B/C/F			DAC-10G			Units
		Min	Typ	Max	Min	Typ	Max	
Monotonicity		10			10			Bits
Nonlinearity			.029	.049		.058	.098	% FS
Differential Nonlinearity			.029	.098		.068		% FS
Output Voltage Compliance	Full Scale Current Change < 1 LSB	-5.0	-6/+18	+10	-5.0	-6/+15	+10	V
Full Scale Current	$V_{REF} = 10.000V$, $R_{16} = R_{17} = 5.000k\Omega$	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full Scale Symmetry	$I_{FS} - \overline{I_{FS}}$		0.1	4.0		0.1	4.0	μA
Zero Scale Current			0.01	0.5		0.01	0.5	μA
Settling Time	All Bits Switched ON or OFF Settle to 0.05% of FS See Note		85	135		85	150	nS
Output Capacitance			18			18		pF
Propagation Delay	$R_L = 5.0k\Omega$		50			50		nS

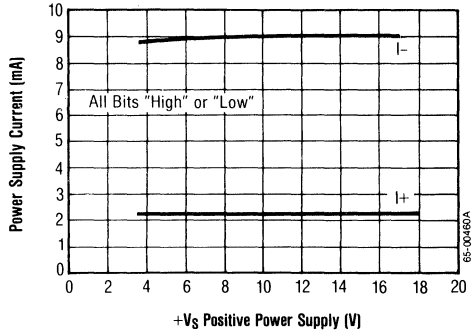
Note: Guaranteed by Design

Typical Performance Characteristics

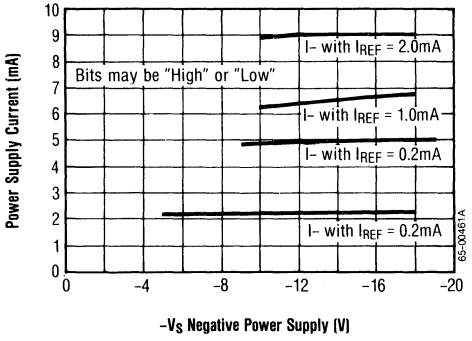
True and Complementary Output Operations



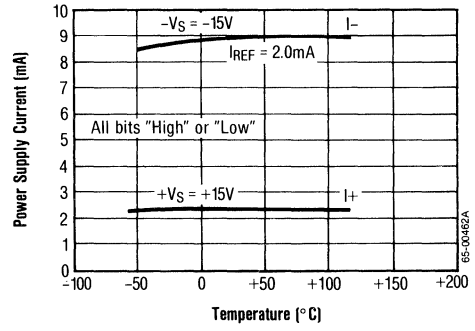
Power Supply Current vs. $+V_S$



Power Supply Current vs. $-V_S$



Power Supply Current vs. Temperature



Propagation and Settling Time

Propagation delays from logic input to analog outputs are typically less than 35nS. Settling times and propagation delays are relatively insensitive to logic input amplitude, power supply voltage or reference current. However, larger reference currents allow for the use of smaller output resistors. This reduces the degradation of speed that occurs due to the DACs output capacitance.

The settling time circuit (Figure 1) yields the optimal settling time that can achieved (85nS). However, in real applications the settling time will be somewhat degraded from ideal. The following applications indicate circuits and settling times for commonly used applications.

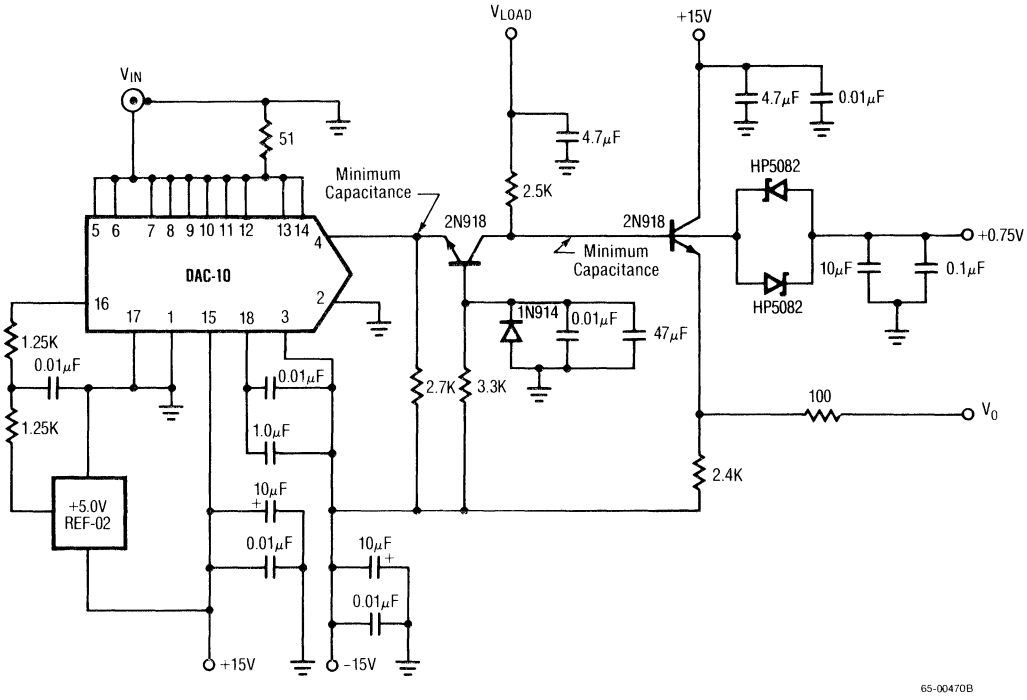


Figure 1. Settling Time Test Fixture

Applications

Output Currents

The analog output currents consist of both true and complemented output sink currents. The sum of the true and complemented currents is always equal to the full scale output current. Full scale output current (I_{FS}) is related to the input reference current by the equation:

$$I_{FS} = 1023/1024 \times 2I_{REF}$$

Input coding of either positive true binary or complementary binary is allowed. The difference of the two output currents is a linear function of the binary input. This feature results in some useful DAC applications where differential outputs are desired, such as differential line driving or digital offset nulling of op amps.

Input Reference

The output current of the DAC-10 is the product of the binary input and the input reference current. The output current is twice the input reference current, defined by the equation:

$$I_O = D/1024 \times 2I_{REF}$$

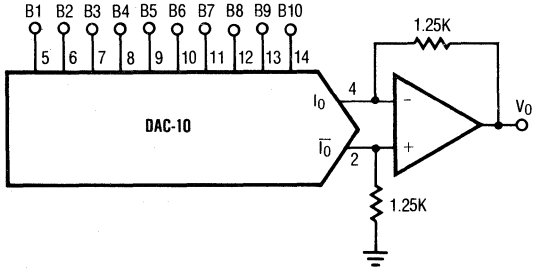
Where I_{REF} is the input reference current into pin 16 and D represents the value of the binary input.

The voltage reference may either be postive or negative. A positive reference is used to force current into pin 16 through bias resistor R16. A negative reference is used to force the voltage at pin 17 negative. The high gain reference amplifier will cause pin 16 to follow pin 17 and again force current into pin 16. The bias resistor is always the resistor in series with pin 16 even when a negative reference is used. Either pin 16 or pin 17 may be offset to accommodate bipolar references.

Noise from the reference supply is reflected into the output. Since the noise output of a reference is directly proportional to bandwidth, the bandwidth must be restricted. A center tapped bias resistor serves as a simple one pole roll-off filter to minimize the effects of wideband noise. A +5V regulated voltage is recommended, with the bias resistor to pin 16 split into two equal resistors having the junction bypassed to ground with a 0.25μF capacitor. A typical +5V bandgap reference (REF-02) puts out a wideband noise voltage of 1 to 2mV_{p-p} at the full 10MHz bandwidth. For a multiplying DAC this voltage is transmitted directly to the output such that, for a +5V output system (LSB = 5.0mV) this amount of noise is significant. The simple filter suggested here restricts the noise bandwidth to 1/4RC. For a bias resistor of 1.25kΩ and a bypass capacitor of 0.25μF the noise bandwidth can be reduced to 800Hz and the noise voltage reduced to approximately 80μV_{p-p}, a significant reduction. The +5V TTL supply should **never** be used for a DAC reference.

High Speed Multiplying Applications

For high speed multiplying applications the transient behavior of the input reference amplifier deserves special consideration. The reference amplifier is compensated with a capacitor from pin 18 to the negative supply. The size of this



	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	V_O
Pos Full Scale	1 1 1 1 1 1 1 1 1 1	+4.995
Pos Full Scale -LSB	1 1 1 1 1 1 1 1 1 0	+4.985
(+) Zero Scale	1 0 0 0 0 0 0 0 0 0	+0.005
(-) Zero Scale	0 1 1 1 1 1 1 1 1 1	-0.005
Neg Full Scale +LSB	0 0 0 0 0 0 0 0 0 1	-4.985
Neg Full Scale	0 0 0 0 0 0 0 0 0 0	-4.995

65-00463A

Figure 2. Bipolar Operation

capacitor is a function of the equivalent driving impedance to pin 16. The larger the driving impedance, the larger the capacitor that is required to maintain an adequate phase margin. Although exact mathematical models of the compensated reference amplifier are somewhat involved, it has been established empirically that the compensating capacitor should never be smaller than 15pF per kΩ of driving impedance.

Finally, for a driving point impedance less than 800Ω the compensating capacitor is no longer required. The Pulsed Reference Operation panel shows how to compute driving point impedance R_{EQ}. In general the smaller R_{EQ} the faster the response. The output current will slew at 6.0mA per μS when no compensation capacitor is required.

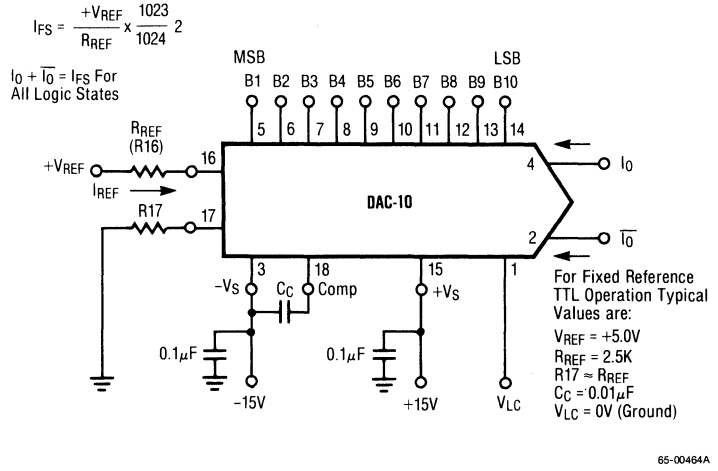


Figure 3. Positive Reference Operation

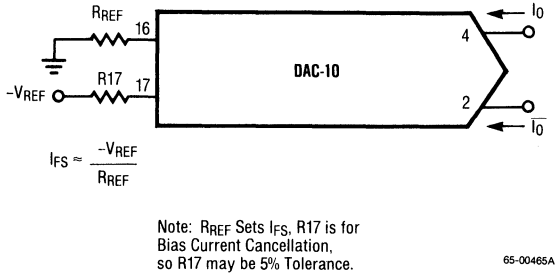


Figure 4. Negative Reference Operation

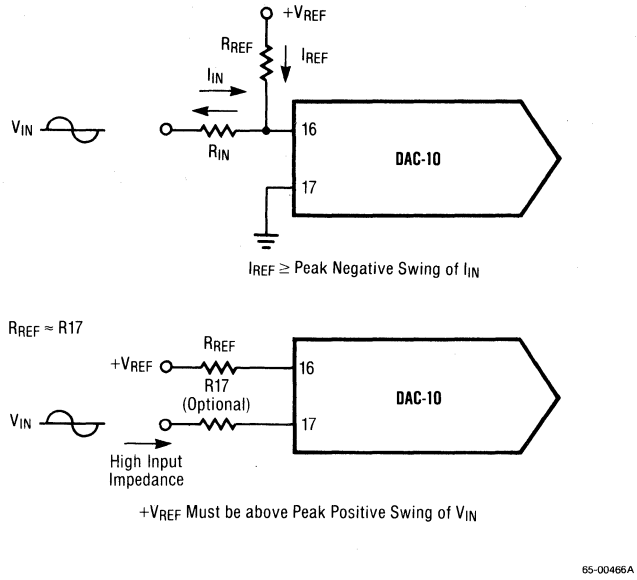


Figure 5. Providing Offsets to Accommodate Bipolar References

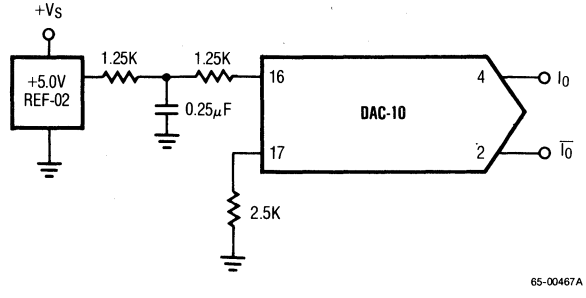


Figure 6. Input Reference Noise Limiting Filter

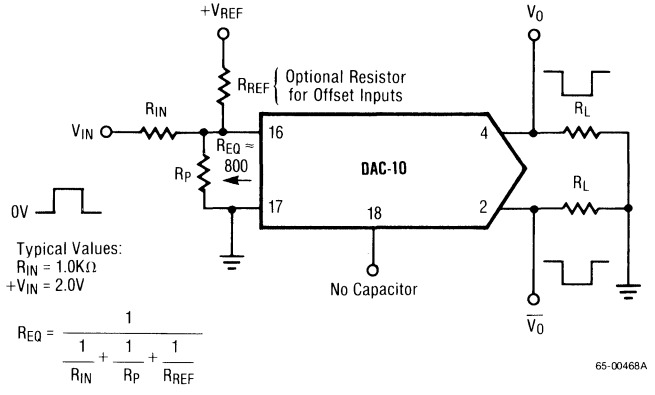


Figure 7. Pulsed Reference Operation

Analog-to-Digital Conversion

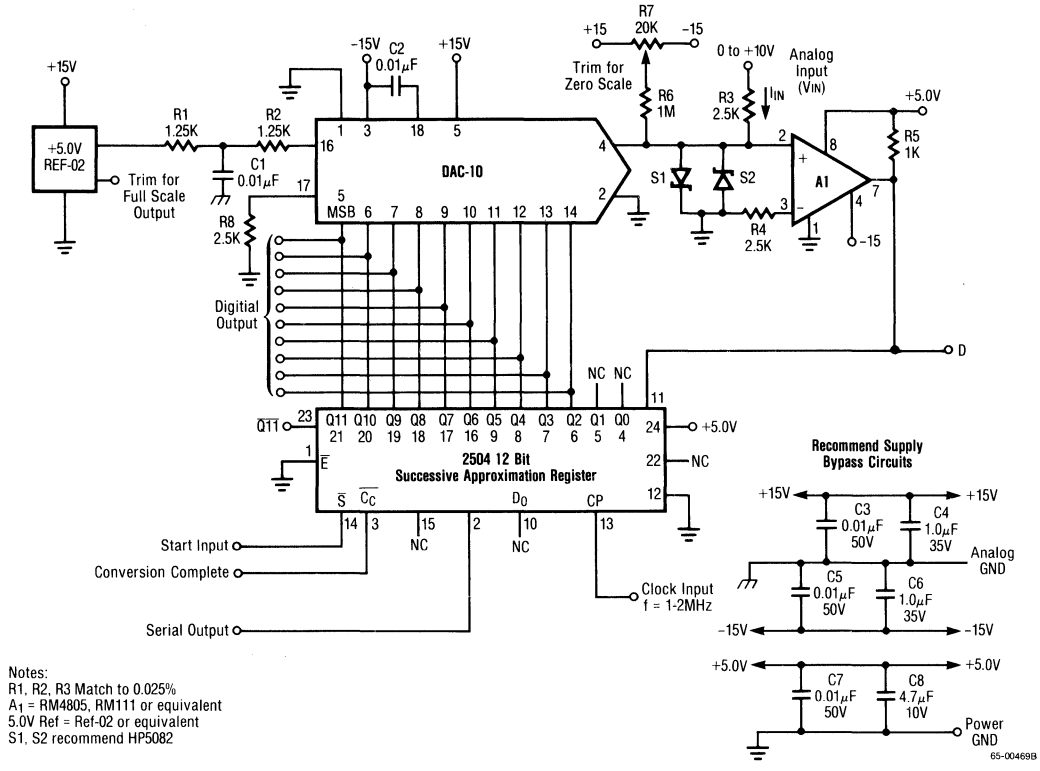
Successive approximation is a logical method of measuring an analog quantity using binary weighted approximation. For example, to measure an unknown weight using a balance scale, the weight is placed on one side of the balance and counterweights are placed on the other side until the scale is balanced. The number of "trials" is made equal to the number of counterweights by starting with the heaviest counterweight first, and either retaining it or rejecting it based on a comparison with the unknown weight. This process is repeated for each weight from heaviest to lightest until all weights have been tried.

By interfacing the DAC-10 with a commercially available successive approximation register (SAR) such as the DM2504 (Figure 8), an analog-to-digital converter (ADC) can be built. The DM2504 register operates as follows.

The register is reset by holding the $\overline{S}$ (Start) input low during a clock (CP) low-to-high transition. After $\overline{S}$ is brought back high, the MSB output (Q11) will be set low and all the remaining register outputs (Q10 - Q12) will be set high, providing a trial binary number for the DAC. This binary number (0111111111) causes the DAC to generate an output current (I_O) which is one half of the full scale output.

I_O is constantly being compared to a current I_{IN}. I_{IN} is generated by the analog input voltage ($I_{IN} = V_{IN}/R_3$). If the first trial number generates an I_O greater than I_{IN}, then the comparator sends a logical zero signal to the SAR. On the next clock low-to-high transition the logical zero is latched into the MSB (Q11) output of the SAR. If the first trial number generates an I_O less than I_{IN}, then the comparator output will be high, and a logical one will be latched into the MSB output. This is a decision making process where the circuit determines, bit by bit, whether the code present on the SAR digital outputs is proportional to the input voltage. After the MSB is latched, the circuit will go through the same decision making process for the next most significant bit, deciding whether it should be latched high or low. The process is repeated successively for each bit until the least significant bit is latched. At this time control logic in the SAR will stop the conversion and signal completion by bringing the QCC output low. The circuit will then stay in its latched output state until conversion is again initiated by the start input.

Since a bit is decided for each clock low to high transition the maximum time needed for a complete conversion will be equal to twelve clock cycles. As each bit is generated it is also latched into the D_O output so that D_O can be used as a serial output. The last two bits will be invalid data because this system uses a 12 bit SAR and a 10 bit DAC.



Notes:
R1, R2, R3 Match to 0.025%
A_1 = RM4805, RM111 or equivalent
5.0V Ref = Ref-02 or equivalent
S1, S2 recommend HP5082

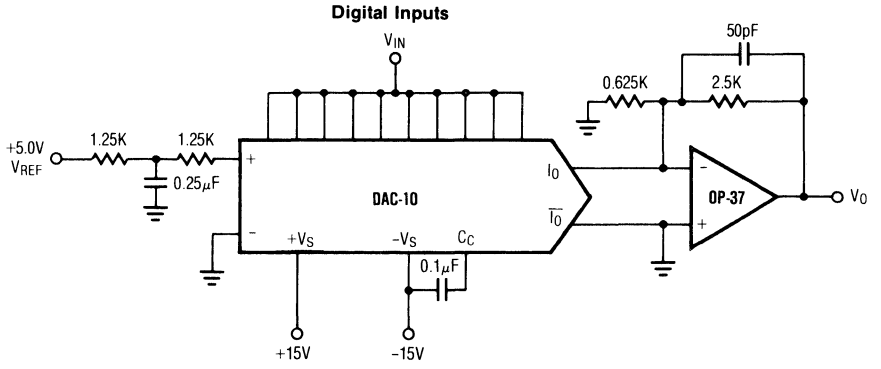
Figure 8. 10-Bit Successive Approximation A/D Converter

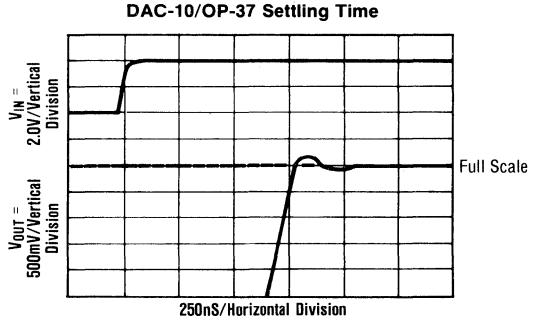
Output Voltage Compliance

The DAC-10 will operate over a wide range of supply voltages. However, the minimum negative output voltage is a direct function of the full scale output current and the negative supply voltage. Output voltage compliance range is the maximum voltage change from which the $\overline{I_O}$ and I_O can sink current. The minimum negative output voltage (V_S-) can be computed by the equation:

$$V_{OC}- \geq (-V_S) + 0.5I_{FS} + 2.6V$$

where V_{OC}- is in volts and full scale current I_{FS} is in milliamps. For instance V_{OC}- will be equal to -10.4V when $-V_S$ = -15V and I_{FS} = 4mA. V_{OC} (positive or negative) does not vary significantly over temperature. The maximum positive output voltage (V_{OC}+) has no theoretical limitations except for device breakdown phenomena. For $-V_S$ = -15V, I_{FS} = 4mA, V_{OC} is ±10V. The full scale current will typically change less than 1 LSB over this output range.





OP-37	F.S. Settling Time (0V to 10V)
0.05% FS	1080nS
0.1% FS	1000nS
0.2% FS	920nS

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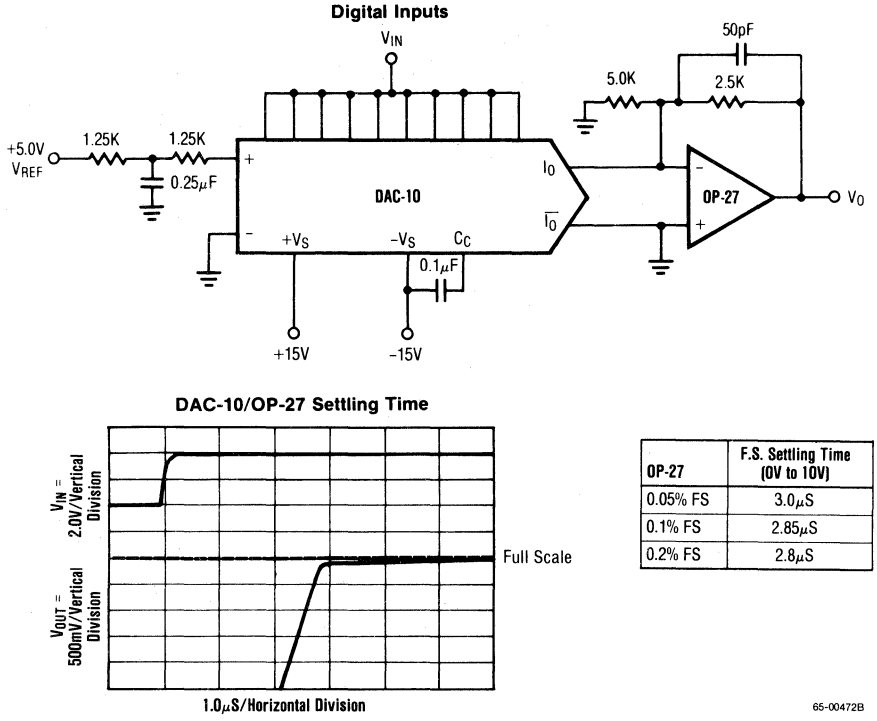
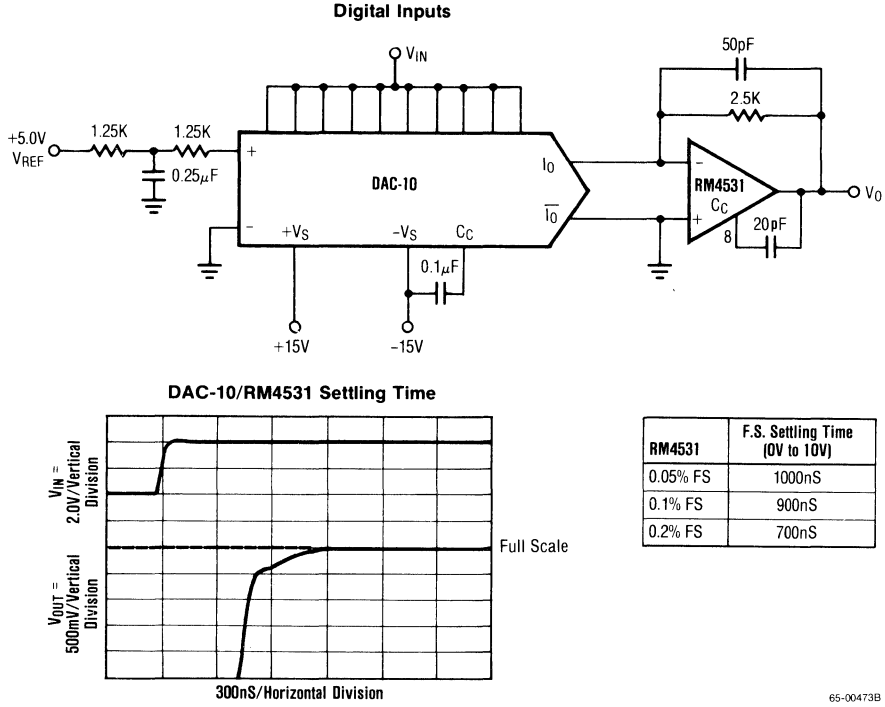
Figure 9. Settling Time Using OP-37



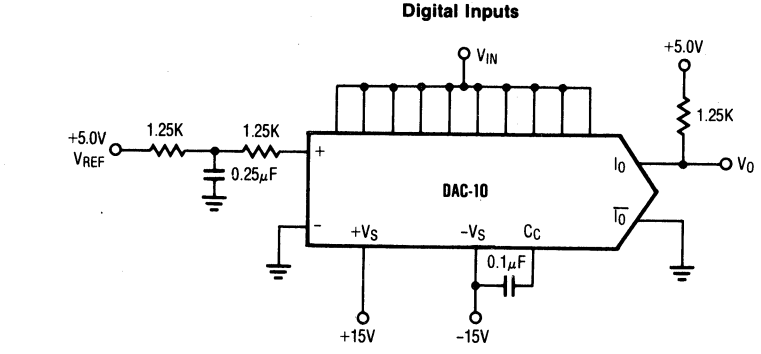
OP-27	F.S. Settling Time (0V to 10V)
0.05% FS	3.0μS
0.1% FS	2.85μS
0.2% FS	2.8μS

Figure 10. Settling Time Using OP-27

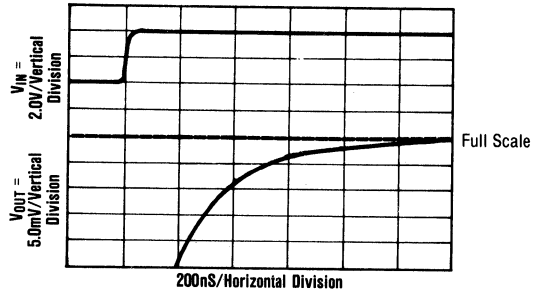


RM4531	F.S. Settling Time (0V to 10V)
0.05% FS	1000nS
0.1% FS	900nS
0.2% FS	700nS

Figure 11. Settling Time Using RM4531



DAC-10 with 1.25KΩ Resistive Output Settling Time



1.25KΩ Resistor	F.S. Settling Time (5.0V to 5.0mV)
0.05% FS	450nS
0.1% FS	320nS
0.2% FS	240nS

65-00474B

Figure 11. Settling Time Using 1.25kΩ Resistor Output

Logic Inputs

By programming the V_{LC} pin the DAC-10 can be made to interface with most logic families. The logic threshold voltage is approximately +1.4V above V_{LC}. Thus when V_{LC} = 0 the DAC-10 will interface with TTL logic; for other logic families V_{LC} must be programmed accordingly. Note that V_{LC} must be obtained from a low impedance source. Low impedance can be provided by a 0.1μF capacitor bypass (see Figure 12).

Output Glitches

The DAC-10 is designed for minimal output glitches. However, a further reduction of output glitches is possible, at a slight sacrifice in settling time, by installing small capacitors at the $I_O/\overline{I_O}$ outputs.

Full Scale Adjustment

Full scale trimming is sometimes required to compensate for resistor or voltage reference tolerances. If a potentiometer is used in series with pin 16 the performance of the DAC may be degraded by the temperature coefficient of the potentiometer. A preferred method of trimming is to use the potentiometer as a voltage divider to bias pin 17. With this method the temperature coefficient of the potentiometer has little effect on the circuit since I_{REF} expands on the tracking of the two resistor halves rather than the absolute value (see Figure 13).

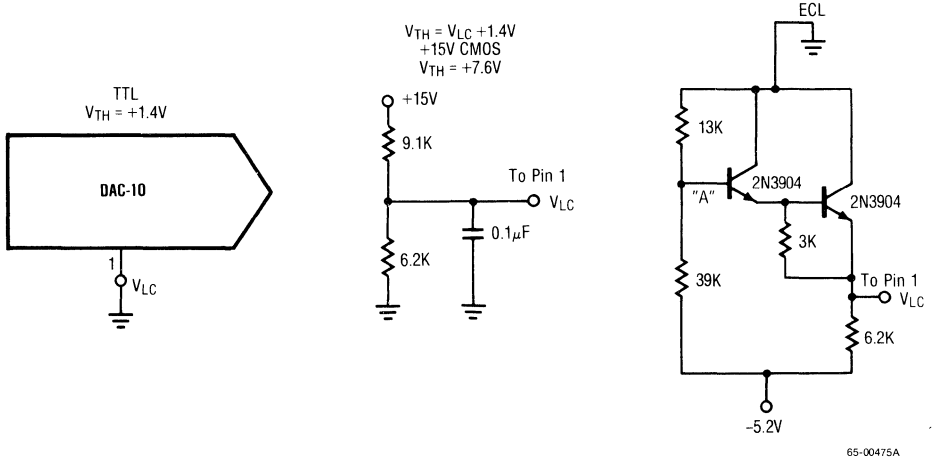


Figure 12. Interfacing With Various Logic Families

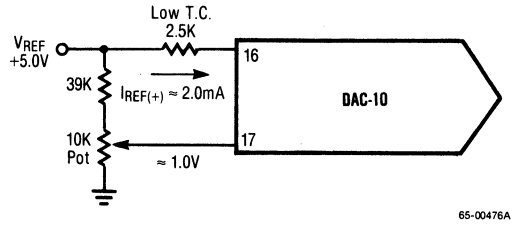
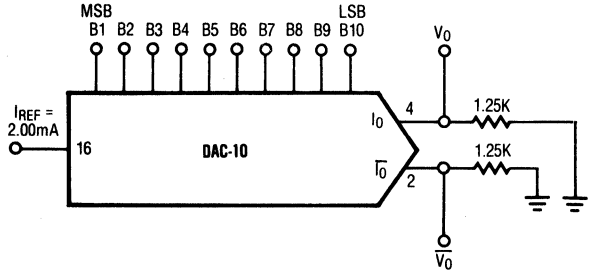


Figure 13. Recommended Full Scale Adjustment Circuit

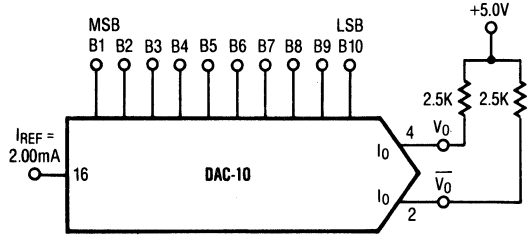
Basic Operation

Resistive terminations can be used to demonstrate basic operation of the DAC-10.



	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	I_0mA	$\overline{I_0mA}$	V_0	$\overline{V_0}$
Full Scale	1 1 1 1 1 1 1 1 1 1	3.996	0.000	-4.995	-0.000
Half Scale +LSB	1 0 0 0 0 0 0 0 0 1	2.004	1.992	-2.505	-2.490
Half Scale	1 0 0 0 0 0 0 0 0 0	2.000	1.996	-2.500	-2.495
Half Scale -LSB	0 1 1 1 1 1 1 1 1 1	1.996	2.000	-2.495	-2.500
Zero Scale +LSB	0 0 0 0 0 0 0 0 0 1	0.004	3.992	-0.005	-4.990
Zero Scale	0 0 0 0 0 0 0 0 0 0	0.000	3.996	-0.000	-4.995

Figure 14. Basic Unipolar Negative Operation

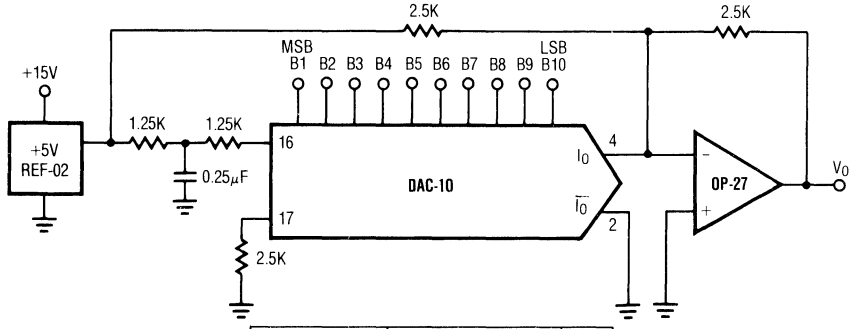


	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	V_0	$\overline{V_0}$
Pos Full Scale	1 1 1 1 1 1 1 1 1 1	-4.990	+5.000
Pos Full Scale -LSB	1 1 1 1 1 1 1 1 1 0	-4.980	+4.990
Zero Scale +LSB	1 0 0 0 0 0 0 0 0 1	-0.010	+0.020
Zero Scale	1 0 0 0 0 0 0 0 0 0	0.000	+0.010
Zero Scale -LSB	0 1 1 1 1 1 1 1 1 1	+0.010	0.000
Neg Full Scale +LSB	0 0 0 0 0 0 0 0 0 1	+4.990	-4.980
Neg Full Scale	0 0 0 0 0 0 0 0 0 0	+5.000	-4.990

Figure 15. Basic Bipolar Output Operation

Offset Binary Operation

By feeding the inverting terminal of the output op amp a current equal to I_{REF} offset binary operation may be implemented.

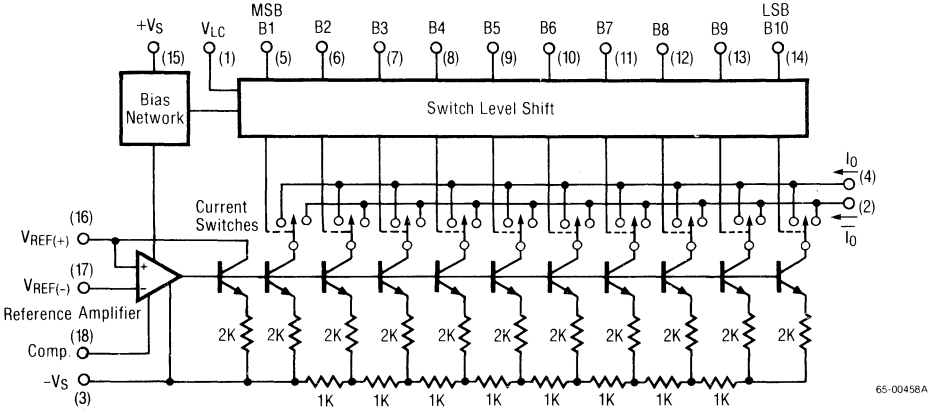


	B1 B2 B3 B4 B5 B6 B7 B8 B9 B10	V_O
Pos Full Scale	1 1 1 1 1 1 1 1 1 1	+4.990
Zero Scale	1 0 0 0 0 0 0 0 0 0	0.000
Neg Full Scale +1 LSB	0 0 0 0 0 0 0 0 0 1	-4.990
Neg Full Scale	0 0 0 0 0 0 0 0 0 0	-5.000

65-00479A

Figure 16. Offset Binary Operation

Simplified Schematic Diagram



65-00458A

DAC-4881 High Performance Microprocessor Compatible Complete 12-Bit D/A Converter

Features

- Complete —
  - High speed op amp for voltage output
  - Precision trimmed thin film resistors
  - Voltage reference — buried zener, 10 ppm/°C typical
  - Input latches for microprocessor compatibility
  - Internal ac compensation
- Accurate —
  - Nonlinearity — less than 1/4 LSB
  - Differential Nonlinearity — less than 1/2 LSB
  - Monotonicity guaranteed over temperature range
- High speed —
  - Settling time — 250 nS (current output)
  - Settling time — 2 μS (voltage output)
- Versatile —
  - High compliance, complementary current outputs
  - Input codes — binary, complementary binary, offset binary, complementary offset binary
  - Voltage output ranges — 0 to +10V, 0 to +5V, ±2.5V, ±5V, ±10V
  - Direct interface to major logic families
  - Direct interface to 8- and 16-bit busses
  - Operates with ±12V to ±15V supplies
  - Low power dissipation — 350 mW
- Monolithic
- Metal/ceramic package
- 883B processing available

Description

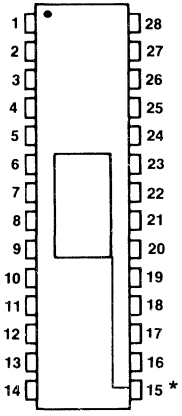
Raytheon's DAC-4881 is a "complete" 12-bit digital-to-analog converter. All of the functions needed for a D/A conversion system have been included on a single chip: a precision 12-bit D/A converter (laser trimmed to better than 0.006% nonlinearity), a buried Zener voltage reference (10 ppm/ °C drift), a high speed, high accuracy current-to-voltage conversion amplifier (2 μS settling time, 200 μV offset error), laser trimmed temperature tracking application resistors, and microprocessor interface latches (50 nS logic time).

The heart of the device is a 12-bit interdigitized laser trimmed resistor ladder network. The DAC is supported by a low noise Kelvin anode buried Zener 10V voltage reference, by a high speed interface amplifier which uses slew enhancement to increase speed without degrading accuracy, and by a switch and latch circuit (single buffered, not double buffered, to improve data throughput rates) which are integrated as a cell to improve microprocessor interface time while simultaneously improving the die size. This high level of integration and performance makes the DAC-4881 an ideal choice for microprocessor interface applications as well as 12-bit high performance applications. For an IC suitable for 8-bit applications, please refer to the DAC-4888 data sheet.

The DAC-4881 is available in three performance grades. The DAC-4881B is specified over the -55° C to +125° C temperature range while the F and D grades are specified over the 0° C to +70° C temperature ranges. All three grades are packaged in a 28-lead side brazed hermetic DIP.

Connection Information

28-Lead Ceramic Side-Brazed Dual In-Line Package
(Top View)



Note: Package lid ac grounded to $-V_S$ 65-01730A

Pin	Function
1	$\overline{CS}$
2	$\overline{ADH}$
3	Bit 1 (MSB)
4–13	Input Bits
14	Bit 12 (LSB)
15	$-V_S$
16	V_{OUT}
17	Ref In
18	Bip Off
19	10V Span
20	20V Span
21	Sum Node
22	$\overline{I_O}$
23	I_O
24	Gnd
25	$+V_S$
26	Gain Adj
27	Ref Out
28	$\overline{ADL}$

Ordering Information

Part Number	Package	Operating Temperature Range
DAC-4881FS	S	0°C to +70°C
DAC-4881DS	S	0°C to +70°C
DAC-4881BS	S	-55°C to +125°C
DAC-4881BS/883B	S	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
S =28-lead ceramic sidebrazed DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

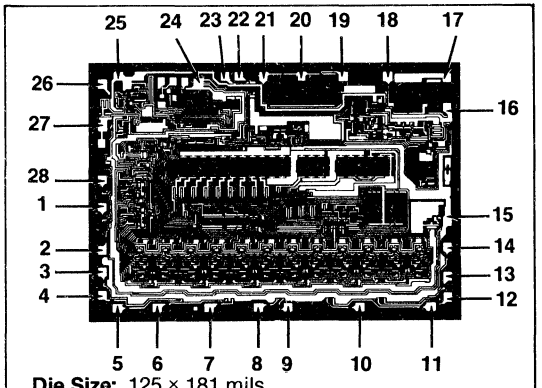
Absolute Maximum Ratings

Supply Voltage ..... ±16.5V
Logic Input Voltages ..... -5V to $-V_S$ +33V
I_O and $\overline{I_O}$ Voltages ..... -5V to +12V
Reference Input Voltage ..... $-V_S$ to $+V_S$
Reference Input Current ..... 2 mA
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (60 Sec) ..... +300°C

Thermal Characteristics

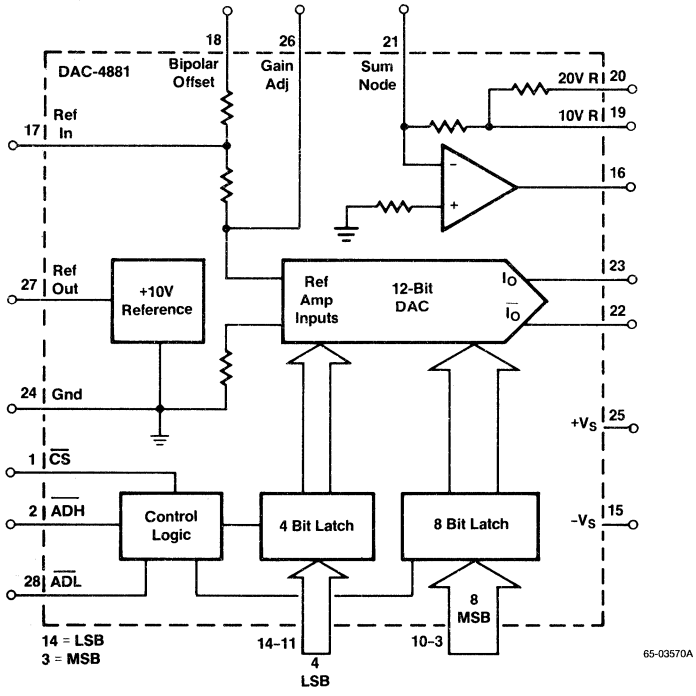
	28-Lead Sidebrazed DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	2000 mW
Therm. Res θ_{JC}	15°C/W
Therm. Res. θ_{JA}	60°C/W
For T_A >50°C Derate at	17 mW/°C

Mask Pattern



Die Size: 125 × 181 mils
Min. Pad Dimensions: 4 × 4 mils
65-03536A

Functional Block Diagram



Electrical Characteristics ($+V_S$ = +15V; $-V_S$ = −15V; and T_A = +25°C unless otherwise noted)

Parameters	4881B/F Min	4881B/F Typ	4881B/F Max	4881D Min	4881D Typ	4881D Max	Units
Resolution Full Temperature	12			12			Bits
Monotonicity Full Temperature	12			12			Bits
Linearity Error		1/4	1/2		1/3	3/4	LSB
Differential Linearity Error		1/4	3/4		1/2	3/4	LSB
Unipolar Gain Error (ext. ref.)[2]		0.05	0.1		0.1	0.4	% of FS
Offset Error Unipolar 10V Range (V_{ZS})		0.003	0.025		0.003	0.15	% of FSR
Bipolar (V_{FS+} + V_{FS-})/2			0.15			0.4	% of FSR
Reference Output	9.950	10.000	10.050	9.900	10.000	10.100	V
Load Regulation — 4.0 mA		0.01	0.05		0.01	0.2	%/mA
Line Regulation — V_S ±10%			0.01			0.1	%/V
Noise[1] (0.1 Hz to 1 MHz)		0.7	1.5		0.7	1.5	mV_{p-p}
Referefnce Input Impedance	8	10	12		10		kΩ
Voltage Output Ranges	0V to +10V, 0V to +5V, ±10V, ±5V, ±2.5V						
External Current	±5			±5			mA
Short Circuit Current to Gnd		45	100		45	100	mA
Current Output Full Scale (ext. ref.)	3.2	4.0	4.8	3.2	4.0	4.8	mA
Zero Scale			250			250	nA
Impedance in Parallel with 15 pF	2.0	7.0		2.0	7.0		MΩ
Compliance	−1.5		+10	−1.5		+10	V
Full Scale Symmetry (10V and 20V FSR)		0.005	0.1				% of FS
Voltage Settling Time[1] 10V Change to .01% of FSR		1.8	2.5		1.8	2.5	μS
20V Change to .01% of FSR		3.0	5.0		3.0	5.0	μS
1 LSB Change to .01% of FSR		1.3			1.3		μS
Slew Rate		20			20		V/μS
Current Settling, FS Transition		250			250		nS
Power Supply Sensitivity (ext. ref.) +15V ±10%			0.002			0.002	% Δ FS
−15V ±10%			0.01			0.01	% Δ V

Notes:
1. Guaranteed by design; not tested.
2. Trimmable to zero.

Electrical Characteristics (Continued)

($+V_S$ = +15V; $-V_S$ = -15V; and T_A = +25°C unless otherwise noted)

Parameters	4881B/F			4881D			Units
	Min	Typ	Max	Min	Typ	Max	
Power Supply Current							
+ISY		8	13		8	13	mA
-ISY		14	19		14	19	mA
Logic Levels[3]	0.8		2.0	0.8		2.0	V
Logic Currents[3]							
Data Hi = 5.5V		0.03	1.0		0.03	1.0	μA
Data Lo = -0.5V		1.5	80		1.5	80	μA
cbits Hi = 5.5V		250	500		250	500	μA
cbits Lo = -0.5V		30	100		30	100	μA
Logic Times[1 3]							
Data Setup	100	30		100	30		nS
Data Hold	100	30		100	30		nS
Propagation Delay[3]							
Data to V_{OUT} 10V Unipolar		0.25			0.25		μS
Data to I_{OUT}		50			50		nS
cbits to V_{OUT}		0.30			0.30		μS
cbits to I_{OUT}		80			80		nS
Minimum Write Pulse[1 3]	100	60		100	60		nS
Total Gain Drift — Internal Ref.[2]		10	30		15		ppm/°C
Total Gain Drift — External Ref.[2]		2	30		2		ppm/°C
Offset Drift							
Unipolar		1.0			1.0		ppm of
Bipolar		3.0			3.0		FSR/°C
Reference Drift		10	30		25		ppm/°C

Notes:
1. Guaranteed by design.
2. FSR equals 0-10V; not specified for current output.
3. Over operating temperature range.

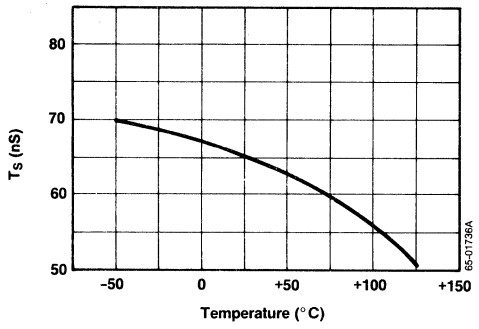
Electrical Characteristics (Continued)

($+V_S$ = +15V; $-V_S$ = -15V; -55°C ≤ T_A ≤ +125°C for B suffix; and 0°C ≤ T_A ≤ +70°C for F/D suffix)

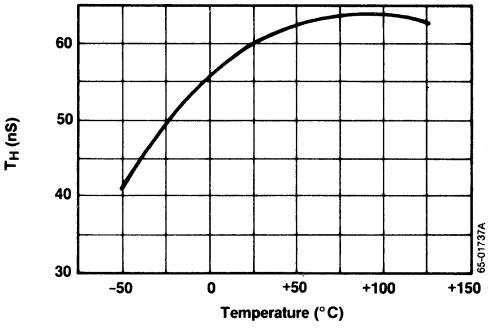
	4881B/F			4881D			
Parameters	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Monotonicity	12			12			Bits
Linearity Error		1/3	2/3		1/2	1.0	LSB
Reference Load Regulation — 4.0 mA		0.01	0.10		0.01	0.2	%/mA
Line Regulation — V_S ±10%		0.001	0.04			0.2	%/V
Current Output Zero Scale		60	500		60	500	nA
Full Scale Symmetry		0.01	0.3		0.01	0.3	% of FS
Voltage Output External Current	±5.0			±5.0			mA
Power Supply Sensitivity (ext. ref.) +15V ±10%			0.01			0.01	%ΔFS
-15V ±10%			0.01			0.01	%ΔV
Slew Rate		20			20		V/μS
Power Supply Current +ISY		10	15		10	15	mA
-ISY		18	22		18	22	mA

Typical Performance Characteristics

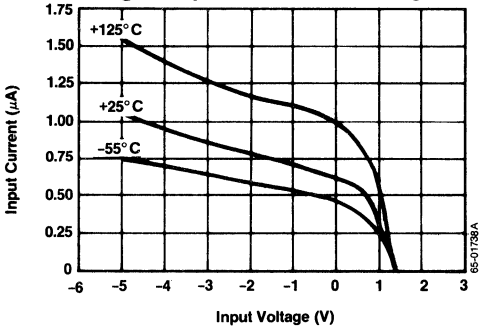
Data Set-Up Time vs. Temperature



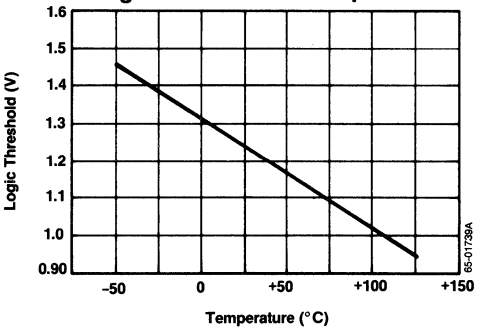
Data Hold Time vs. Temperature



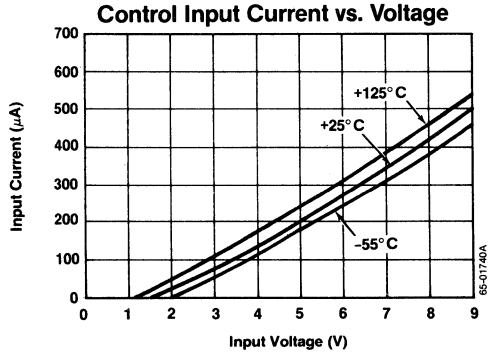
Digital Input Current vs. Voltage



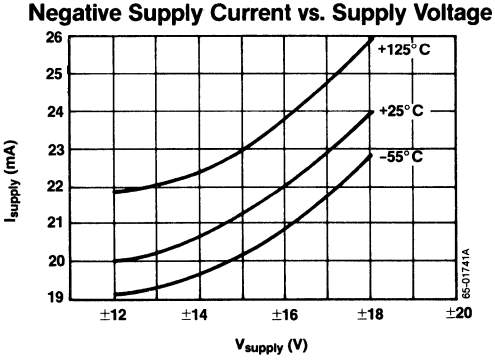
Logic Threshold vs. Temperature



Control Input Current vs. Voltage

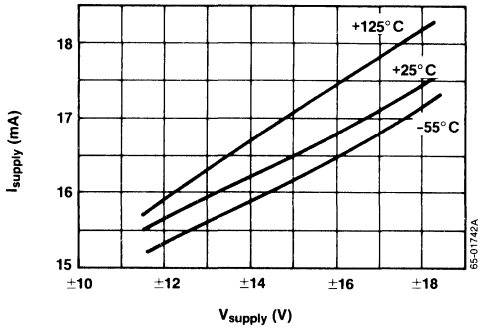


Negative Supply Current vs. Supply Voltage

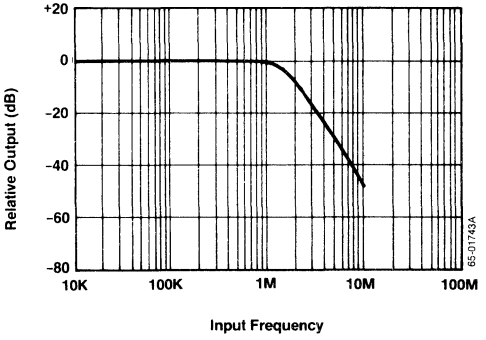


Typical Performance Characteristics (Continued)

Positive Supply Current vs. Supply Voltage



Reference Input Multiplying Frequency Response (V_S 100 mV_{p-p})



Digital Input

The interface latches are arranged in two sections: an 8-bit latch for bits 1 through 8, enabled by $\overline{ADH}$, and a 4-bit latch for bits 9 through 12, enabled by $\overline{ADL}$. This 8-bit-4-bit division allows easy interface to an 8-bit microcomputer data bus using the connection shown in Figure 1.

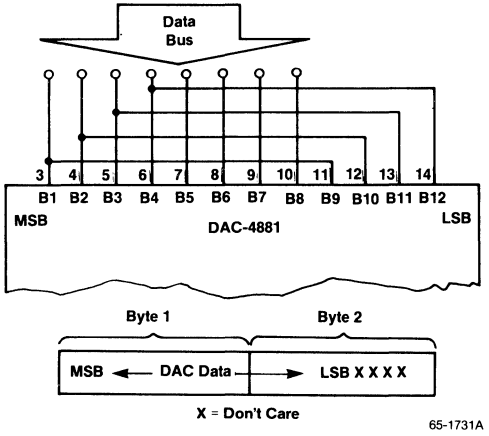
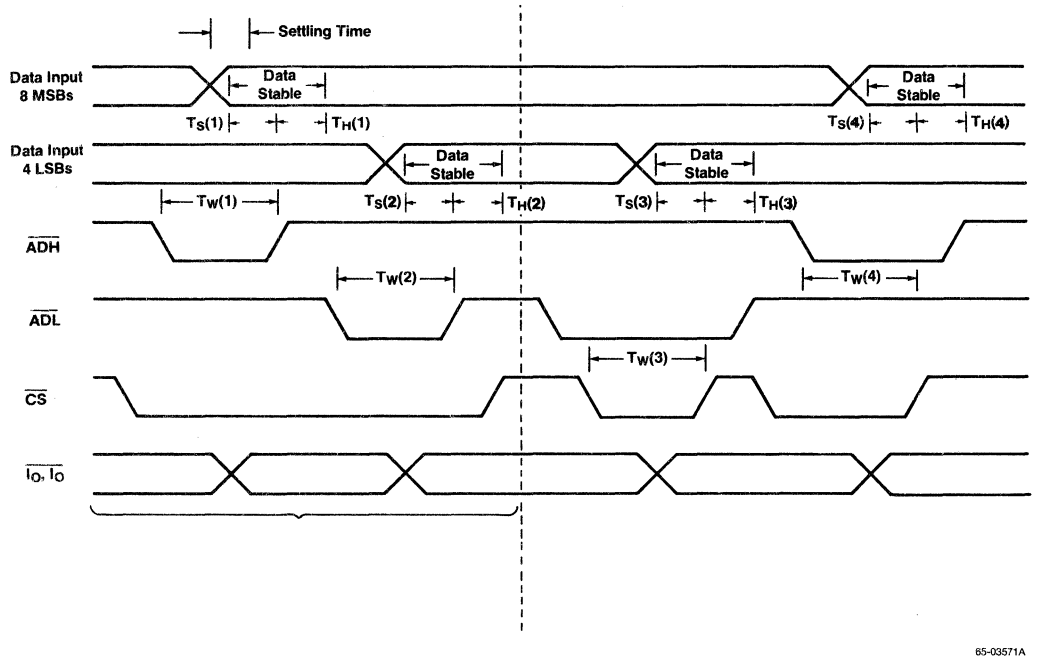


Figure 1. Typical 8-Bit Data Bus Connection — Left Justified Format

TTL, PMOS or CMOS logic levels from the data bus drive the DAC inputs; the logic threshold is typically +1.4V. The voltage level at the inputs can be high going positive, even somewhat higher than the + supply voltage, but can go negative only to about -5V.

Figure 2 shows a timing diagram for a typical 8-bit data bus interface. The DAC-4881 appears to the microprocessor as two locations in memory; the first location for the 8 MSBs and the second location for the 4 LSBs. The addresses for these two locations can be selected by checking the processor's memory map for unused spaces, or by using ROM space (ROMs will only be enabled by read instruction, while the DAC-4881 will only respond to a write). Address decoding can be realized by hard wired logic gates designed to respond with a low output or by using a digital comparator IC such as a DM8131. If the processor used has double byte write instructions with an automatic address incrementation then the system can be simplified, putting the two addresses consecutively and storing the data to be written in a two byte stack.

The sequence in the timing diagram (Figure 2) is as follows: first, the R/W line from the processor, which is tied to the $\overline{CS}$ control input, goes low to start a write to the DAC-4881. Then the address code for the 8 MSBs is sent out on the address bus, is decoded by logic, bringing $\overline{ADH}$ low. The 8 MSB latches are now enabled and the data present on the data bus will change the DAC output. When the $\overline{ADH}$ line goes high again the MSB data is latched in. This sequence of write, address, data is repeated for the 4 LSB latches, and then the $\overline{CS}$ input goes high, ensuring that the data will stay latched in.



Typical 8-bit data bus operation:
1. Select chip with $\overline{CS}$
2. Write eight most significant bits with $\overline{ADH}$
3. Write four least significant bits with $\overline{ADL}$
4. Latch data in with $\overline{CS}$

T_W = Data write time*
T_S = Data set-up time*
T_H = Data hold time*

*See Electrical Characteristics for specifications

Figure 2. Timing Diagram

Control Inputs

Figure 3 shows a truth table for the three control inputs. Note that minimum durations for these signals are required for proper operation (see the table of Electrical Characteristics for specifications of T_W, T_S, and T_H). T_W is the minimum low state pulse width to guarantee enabling the latch. The data (bit) inputs must also stay in a known state for a minimum amount of time, both before and after the control signal goes high again. The time before the control input goes high is T_S, the data set-up time, and the time after is T_H, the data hold time. This timing is generally created through wait statements in the computer program, or with a one shot if necessary.

The specifications for logic current into the control inputs seem to imply that the logic driving the inputs must have a high output current capability, but note that the logic high is specified at 5.5V, while the logic threshold is down at 1.4V. The actual requirement is for the logic to supply 15 μA at 2V, which is within the capability of CMOS and PMOS.

If all the control bits are wired to ground then the DAC-4881 will function just like a conventional D/A converter; that is, any data input will immediately flow through to the output.

$\overline{CS}$	$\overline{ADH}$	$\overline{ADL}$	Result
1	X	X	All inputs disabled — output latched
0	0	0	All inputs active
0	0	1	8 MSBs active — others latched
0	1	0	4 LSBs active — others latched
0	1	1	All inputs disabled — output latched

X = don't care

Figure 3. Control Input Truth Table

Analog Output

The heart of the DAC-4881 is a binary weighted current source DAC. Refer to the Functional Block Diagram.

The reference amplifier forces the reference amplifier input (pin 26, Gain Adjust) to virtual ground (0V). When the +10V reference voltage is connected to pin 17 the entire 10V is applied across the 10kΩ reference resistor. The resultant 1 mA current (10V/10K = 1 mA) flows into the ref amp input where it is mirrored and scaled by the binary weighted current sources. The scaling of these current sources is such that the full scale output current is four times the input current; for a 1 mA reference the full scale output will be -4 mA. (Actually, because the code combination starts at all zeros for 0 output full scale is 4 mA +1 LSB, which is -3.99902 mA. For a similar reason with 3 decimal digits one can only count up to 999, not to 1000.)

Two outputs are provided, I_O and $\overline{I_O}$. The logic inputs can be complemented (the sense of 1 and 0 reversed) by taking the output from $\overline{I_O}$ instead of I_O. For all zeros at the bit inputs $\overline{I_O}$ will be at full scale, -3.99902 mA. If either output is unused it should be grounded, and not left unconnected.

An option for bipolar output (both positive and negative output currents over the input code range — normally both output currents are negative — current flowing into the DAC) is provided with the bipolar offset resistor between pins 17 and 18. For example, what if I_O is connected to pin 18, and I_O is also monitored with a current meter to ground? The reference voltage connected to pin 17 will be applied across the bipolar offset resistor, because pin 18 is wired to ground through the current meter. This creates a 2 mA offset current (10V/5K = 2 mA) which adds to the normal output current. So, for all zeros at the inputs the output will be +2 mA. For all ones at the inputs the output will be at -2 mA +1 LSB (-3.99902 mA +2 mA = -1.99902).

The op amp is provided as a current to voltage converter, i.e., it changes the -4 mA output current into a selectable output voltage. When the output current is connected to the sum node, all of the current will flow into the sum node, and, having nowhere else to go, will flow through the 2.5K span resistors and into the op amp output. Feedback holds the sum node at virtual ground (0V); the IR drop across the span resistor adds to the 0V virtual ground to produce a proportional output voltage at the op amp output.

For example, if pin 19 is wired to pin 16, no offset resistor used, and full scale current of -4 mA is flowing into I_o, then 4 mA will flow out of the op amp output, through the 2.5K resistor, and into I_o. 4 mA x 2.5K = 10V, so V_{OUT} will equal +10V. Figure 4 shows a table of all the possible combinations of offset and output ranges.

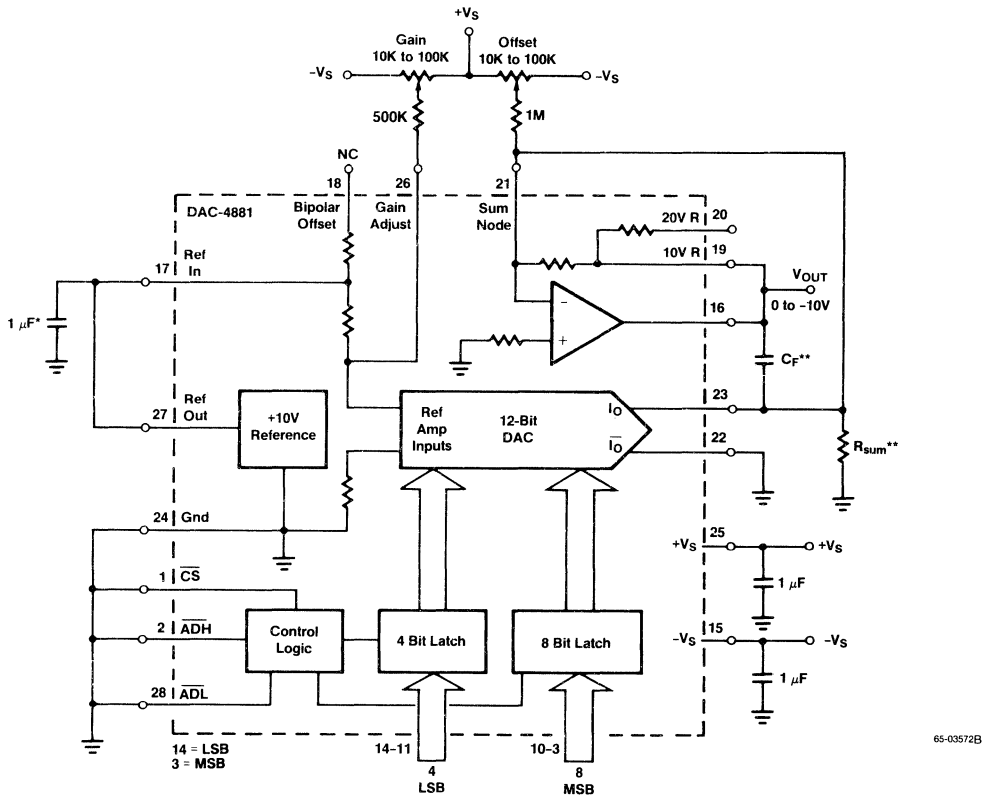
Output Range (zeros to ones)	Pin Connections (always connect 17 to 27)
0V to +5V	20 to 21, 16 to 19, 21 to 23, 22 to Gnd
+5V to 0V	20 to 21, 16 to 19, 21 to 22, 23 to Gnd
0V to +10V	16 to 19, 21 to 23, 22 to Gnd
+10V to 0V	16 to 19, 21 to 22, 23 to Gnd
-2.5V to +2.5V	16 to 19, 18 and 20 to 21, 21 to 23, 22 to Gnd
+2.5V to -2.5V	16 to 19, 18 and 20 to 21, 21 to 22, 23 to Gnd
-5V to +5V	16 to 19, 18 to 21, 21 to 23, 22 to Gnd
+5V to -5V	16 to 19, 18 to 21, 21 to 22, 23 to Gnd
-10V to +10V	16 to 20, 18 to 21, 21 to 23, 22 to Gnd
+10V to -10V	16 to 20, 18 to 21, 21 to 22, 23 to Gnd

Figure 4. Connections for Various Output Formats

Some improvement of settling time can be made with the addition of R_{SUM} and C_F in Figures 6 and 7. Figure 5 gives a table of values for the various output combinations. C_F can also be added in applications where speed is not critical but output noise is. Larger values of C_F will overcompensate the amplifier, slowing it down, but simultaneously integrating out high frequency noise. Noise can also be reduced by adding a large capacitor from the reference output to ground.

Output Range	CF	R_{sum}
0V to +5V	15 pF	10K
0V to +10V	5 pF	2.5K
±2.5V	15 pF	3.3K
±5V	0 pF	∞
±10V	0 pF	∞

Figure 5. Component Values for Improved Settling Time



Calibration Procedure:

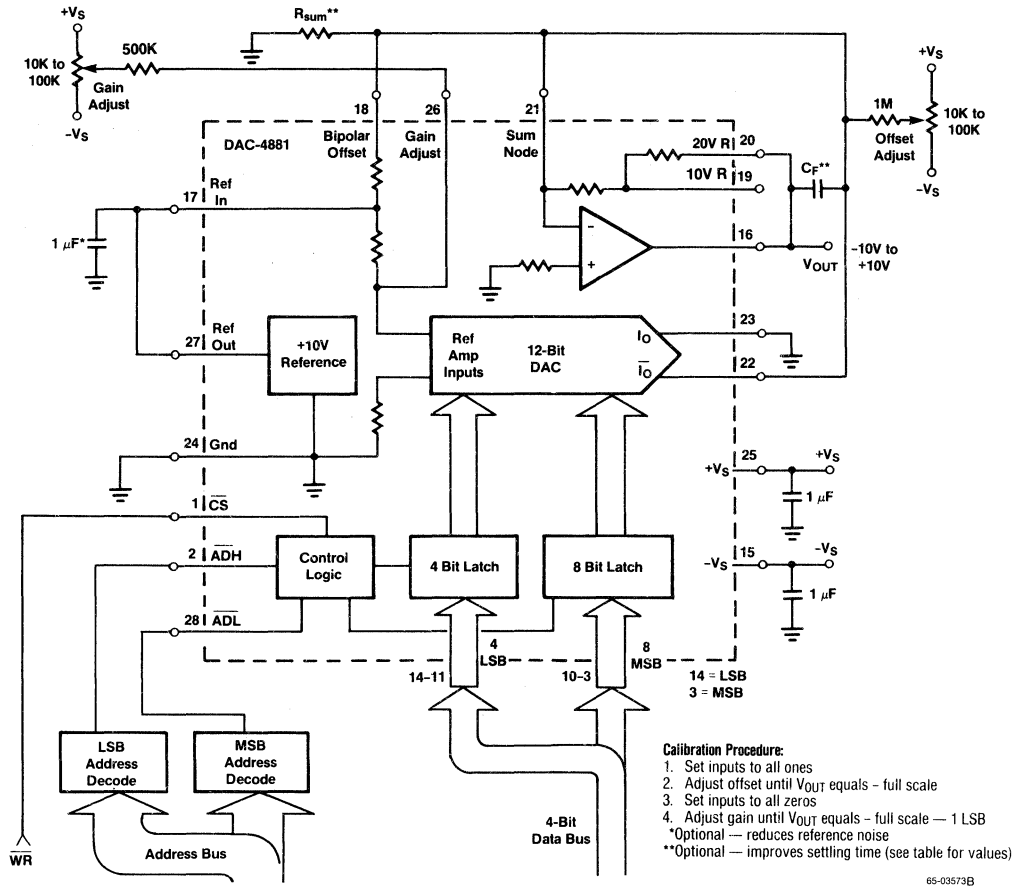
1. Set inputs to all zeros
2. Adjust offset until V_{OUT} equals 0V
3. Set inputs to all ones
4. Adjust gain until V_{OUT} equals correct full scale value

*Optional — reduces reference noise

**Optional — improves settling time (see table for values)

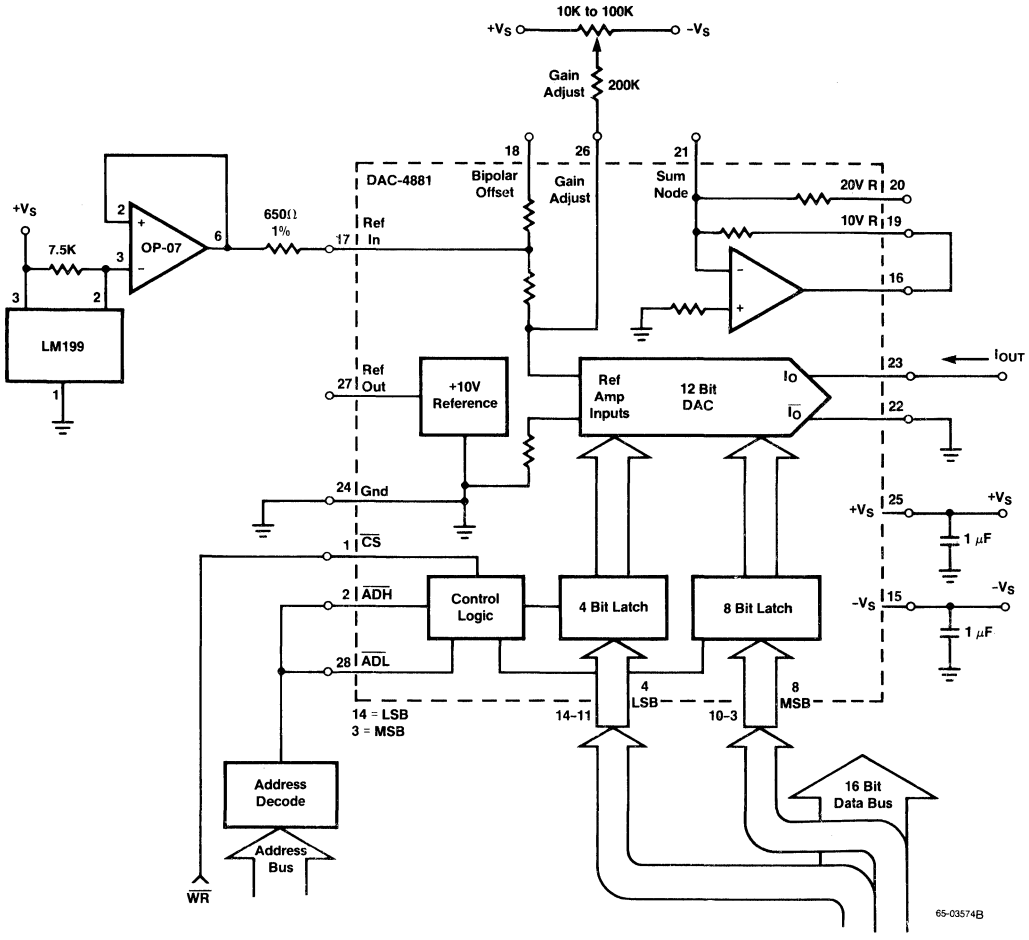
Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Straight Binary; Unipolar with True Input Code, True Zero Output	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.0001	3.998	0.0024
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary Binary; Unipolar with Complementary Input Code, True Zero Output	Positive Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
	Positive Full Scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
	Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

Figure 6. Stand-Alone, 0 to -10V, 12-Bit Straight Binary With Gain and Offset Adjust Connections



Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Offset Binary; True Zero Output	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	2.000	1.999
	- LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000
2's Complement; True Zero Output MSB Complemented (Need Inverter at B1)	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0000
	- LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000

Figure 7. Microprocessor Interface, 8-Bit Data Bus, =10V to -10V Output With Complementary Binary Input (All Zeros Equal - Full Scale)

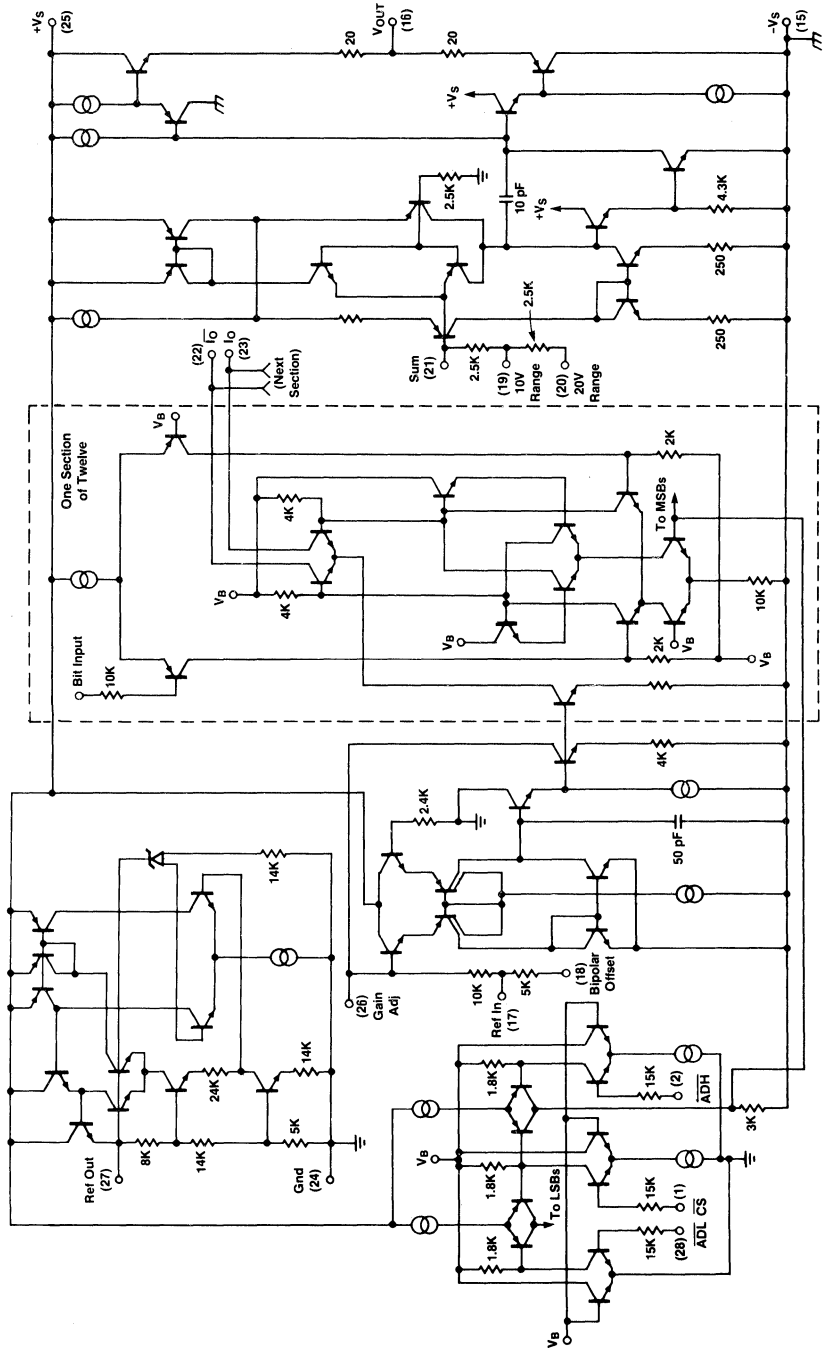


Calibration Procedure:
Zero scale error is entirely leakage current — no adjustment necessary
1. Set inputs to all ones
2. Adjust gain until I_O equals correct full scale value

65-03574B

Figure 8. Microprocessor Interface, 16-Bit Data Bus, 0 to -4 mA Output With Straight Binary Input and External Reference

Simplified Schematic Diagram



DAC-4888 8-Bit D/A Converter With Microprocessor Interface Latches

Features

- Complete —
  High speed op amp for voltage output
  Tracking thin film resistors
  Voltage reference - bandgap, 25ppm/°C
  Input latches for microprocessor compatibility
  Internal AC compensation
- Accurate —
  Nonlinearity - ±1/4LSB max. over temperature range
  Monotonic - differential nonlinearity ±1/3 LSB max. over temperature range
- High speed —
  Settling time - 150nS (current output)
  Settling time - 1.4μS (voltage output)
- Versatile —
  High compliance, complementary current outputs
  Input codes - binary, complementary binary, offset binary, complementary offset binary
  Voltage output ranges - 0 to +10V, 0 to +5V, ±2.5V, ±5V, ±10V
  Direct interface to major logic families
  Direct interface to 4- and 8-bit busses
  Operates with ±12V to ±15V supplies
  Low power dissipation - 330mW
- Monolithic
- Ceramic package
- 883B processing available

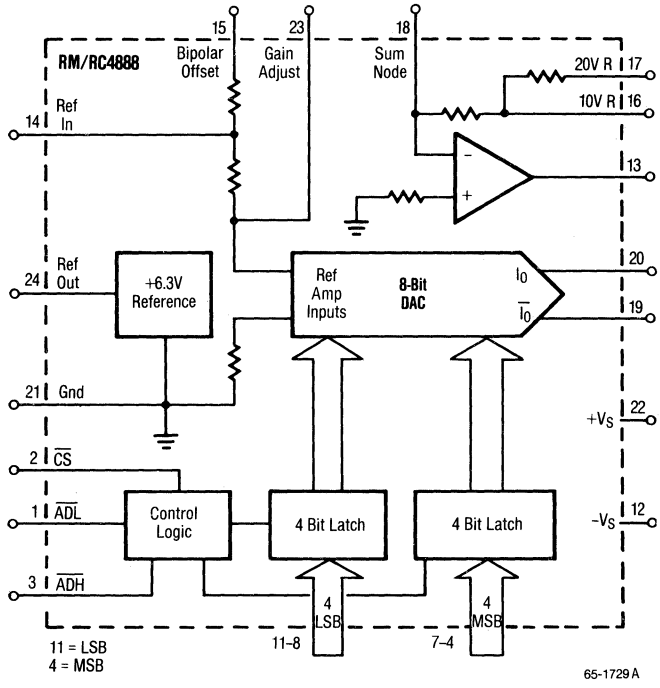
Description

Raytheon's DAC-4888 is a "complete" 8-bit digital-to-analog converter. All of the functions needed to build a D/A conversion system have been integrated on a single monolithic chip: a precision 8-bit current output D/A converter, a bandgap voltage reference (±25ppm/°C drift), a high speed, high accuracy current-to-voltage conversion amplifier (1.4μS settling time, 200μV offset error), temperature tracking thin film application resistors, and microprocessor interface latches (50nS logic time).

The DAC is supported by a bandgap reference derived from the REF-01 Series Voltage Reference, by a high speed interface amplifier which uses slew enhancement to increase speed without degrading accuracy, and by a switch and latch circuit (single buffered, not double buffered, to improve data throughput rates) which are integrated as a cell to improve microprocessor interface time while simultaneously improving the die size. This high level of integration and performance makes the DAC-4888 an ideal choice for microprocessor interface applications as well as 8-bit high performance applications.

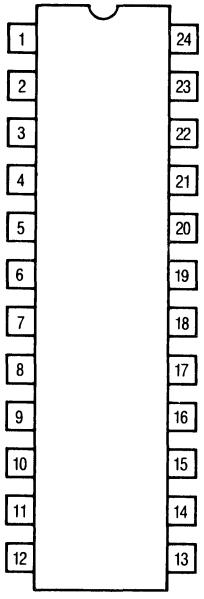
The DAC-4888 is available in three performance grades: the "F" and "D" grades are specified over the commercial (0 to +70°C) temperature range, and the "B" grade is specified from -55°C to +125°C. All types are packaged in a 24-pin 300-mil wide DIP.

Functional Block Diagram



Connection Information

24-Pin Ceramic Dual In-Line Package
(Top View)



65-02255A

Pin	Function
1	$\overline{ADL}$
2	$\overline{CS}$
3	$\overline{ADH}$
4	DB7 (MSB)
5–10	Input Bits
11	DB0 (LSB)
12	$-V_S$
13	V_{OUT}
14	Ref In
15	Bip Off
16	10V Span
17	20V Span
18	Sum Node
19	$\overline{I_O}$
20	I_O
21	Gnd
22	$+V_S$
23	Gain Adj
24	Ref Out

Ordering Information

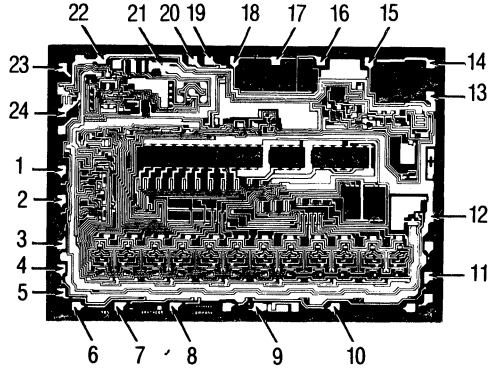
Part Number	Package	Operating Temperature Range
DAC-4888FD	D	0°C to +70°C
DAC-4888DD	D	0°C to +70°C
DAC-4888BD	D	-55°C to +125°C
DAC-4888BD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
D =24-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Supply Voltage ..... ±18V
Logic Input Voltages ..... -5V to $-V_S$ +36V
I_O and $\overline{I_O}$ Voltages ..... -5V to +12V
Reference Input Voltage ..... $-V_S$ to $+V_S$
Reference Input Current ..... 2 mA
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (60 Sec) ..... +300°C

Mask Pattern



65-02277A

Note: Pin numbers are for 24-pin DIP

Die Size: 125 x 181 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	24-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	1666 mW
Therm. Res θ_{JC}	20°C/W
Therm. Res. θ_{JA}	75°C/W
For T_A >50°C Derate at	13.3 mW/°C

Electrical Characteristics ($+V_S$ = +15V; $-V_S$ = -15V; and T_A = +25°C unless otherwise noted)

Parameters	DAC-4888B/F			DAC-4888D			Units
	Min	Typ	Max	Min	Typ	Max	
Resolution Full Temperature	8			8			Bits
Monotonicity Full Temperature	8			8			Bits
Linearity Error		1/10	1/4		1/10	1/3	LSB
Differential Linearity Error		1/8	1/3		1/8	1/2	LSB
Gain Error (Ext. Ref.)[3]		0.5	2.0		0.7	3.0	% of FS
Offset Error							
Unipolar 10V Range		0.05	0.1		0.1	0.2	% of FSR
Bipolar ($V_{FS+} + V_{FS-}$) ÷ 2		0.1	0.5		0.2	2.0	% of FSR
Reference Output	6.20	6.35	6.50	6.10	6.35	6.70	V
Load Regulation — 9.0mA			0.05			0.1	%/mA
Line Regulation — V_S +10%			0.02			0.1	%/V
Noise[1] (0.1Hz to 1MHz)		2.0	3.0		2.0		mV_{p-p}
Reference Input Impedance	5.0	6.3	7.5		6.3		kΩ
Voltage Output Ranges	0 to +10, 0 to +5, ±10, ±5, ±2.5						V
External Current	±5.0			±5.0			mA
Short Circuit Current (to GND)		45	100		45	100	mA
Noise[1] (0.1 to 1MHz)		3.0	4.5		3.0		mV_{p-p}
Current Output Full Scale (Ext. Ref.)	3.2	4.0	4.8	3.2	4.0	4.8	mA
Zero Scale		30	200		30	200	nA
Impedance in Parallel with 15pF	1.5	6.0		1.5	6.0		MΩ
Compliance	-1.5		+10	-1.5		+10	V
Full Scale Symmetry		0.001	0.1		0.001	0.2	% of FS
Voltage Settling Time[1]							
10V Change to .2% FS		1.4	2.5		1.4	2.5	μS
20V Change to .2% FS[1]		2.5	5.0		2.5	5.0	μS
Slew Rate		20			20		V/μS
Current Settling, FS Transition[1,2]		150	500		150	500	nS
Power Supply Sensitivity							
+15V ±10%			0.002			0.002	%ΔFS
-15V ±10%			0.01			0.01	%ΔV

Notes:
1. Guaranteed by design.
2. To 0.2% FS.
3. Trimmable to zero.

Electrical Characteristics (Continued)

($+V_S$ = +15V; $-V_S$ = −15V; and T_A = +25°C unless otherwise noted)

Parameters	DAC-4888B/F			DAC-4888D			Units
	Min	Typ	Max	Min	Typ	Max	
Power Supply Current							
+ISY		8	12		8	12	mA
-ISY		14	18		14	18	mA
Logic Input Bits Low			0.8			0.8	V
Logic Input Bits High	2.0			2.0			V
Logic Currents[5]							
Data Hi = 5.5V		0.03	1.0		0.03	1.0	μA
Data Lo = −0.5V		1.5	80		1.5	80	μA
Address control bits Hi = 5.5V		250	500		250	500	μA
Address control bits Lo = −0.5V		30	100		30	100	μA
Logic Times[1,5]							
Data Set-Up	100	50		100	50		nS
Data Hold	100	50		100	50		nS
Propagation Delay[5]							
Data to V_{OUT} 10V Unipolar		0.25			0.25		μS
Data to I_{OUT}		60			60		nS
Address control bits to V_{OUT}		0.3			0.3		μS
Address control bits to I_{OUT}		75			75		nS
Minimum Write Pulse[1,5]	100	60		100	60		nS
Total Gain Drift — Internal Reference[4,5]		20	70		30		ppm/°C
Total Gain Drift — External Reference[4,5]		15	70		20		ppm/°C
Offset Drift							
Unipolar[1,4,5]		1.0			1.0		ppm of FSR/°C
Bipolar[1,3,5]		3.0			3.0		ppm of FSR/°C
Reference Drift[5]		25	70		40		ppm/°C
Linearity Drift[1,2,5]		1	10		1.5		ppm/°C
Differential Linearity Drift[1,2,5]		1	10		1.5		ppm/°C

Notes:
1. Guaranteed by design.
2. For all DAC codes. FSR equals any voltage range.
3. FSR equals ±10V; not specified for current output.
4. FSR equals 0–10V; not specified for current output.
5. Over temperature.

Electrical Characteristics (Continued)

($+V_S$ = +15V; $-V_S$ = -15V; -55°C ≤ T_A ≤ +125°C for B; and 0°C ≤ T_A ≤ +70°C for F/D)

Parameters	DAC-4888B/F			DAC-4888D			Units
	Min	Typ	Max	Min	Typ	Max	
Monotonicity	8.0			8.0			Bits
Linearity Error		1/10	1/3		1/8	1/2	LSB
Reference							
Load Regulation — 9.0mA		0.01	0.10		0.01	0.2	%/mA
Line Regulation — V_S ±10%		0.001	0.04			0.2	%/V
Current Output Zero Scale		60	500		60	500	nA
Full Scale Symmetry		0.01	0.3		0.01	0.3	% of FS
Voltage Output							
External Current	±5.0			±5.0			mA
Power Supply Sensitivity							
+15V ±10%		0.0002	0.01		0.0002	0.01	%ΔFS
-15V ±10%		0.0005	0.01		0.0005	0.01	%ΔV
Slew Rate		20			20		V/μS
Power Supply Current							
+ISY		10	15		10	15	mA
-ISY		18	22		18	22	mA

Digital Input

The interface latches are arranged in two sections: a 4-bit latch for bits 1 through 4 enabled by $\overline{ADH}$, and a 4-bit latch for bits 5 through 8 enabled by $\overline{ADL}$. This 4-bit-4-bit division allows easy interface to a 4-bit microcomputer data bus using the connection shown in Figure 1.

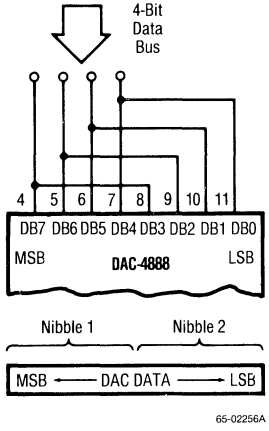


Figure 1. Typical 4-Bit Data Bus Connection

TTL, PMOS or CMOS logic levels from the data bus drive the DAC inputs; the logic threshold is typically +1.4V. Digital input voltage levels can be more positive than the + supply voltage, and also negative to as much as 5V below ground.

Figure 2 shows a timing diagram for typical 4-bit and 8-bit interfaces. The DAC-4888 appears to the microprocessor as two locations in memory; the first location stores nibble 1 and the second nibble 2. The addresses for these two locations can be selected by checking the processor's memory map for unused locations. For 8-bit microprocessors the instruction can be written as a single byte to a single memory address. Address decoding can be realized through hard-wired logic gates designed to respond with a low output to the correct address code ($\overline{AD}$ = A · B · C · D · E · F · G · H) or by using a digital comparator IC such as a DM8131.

For a 4-bit processor the first sequence in the timing diagram goes as follows: first, the R/$\overline{W}$ line from the processor, which is tied to the $\overline{CS}$ control input, goes low to start a write to the DAC-4888. Then the address code for the 4 MSB is sent out on the address bus and decoded, bringing $\overline{ADH}$ low. The 4 MSB latches are now enabled and the data present on the data bus will alter the DAC output. When the $\overline{ADH}$ line goes high again the MSB data is latched in, freezing the DAC output. This sequence of write, address, data is repeated for the 4LSB latches, and then the $\overline{CS}$ input goes high, ensuring that the data will stay latched in.

The sequence is the same for an 8-bit microprocessor, except that the write operation will combine $\overline{ADH}$ and $\overline{ADL}$ since all the DAC inputs are simultaneously presented with valid data.

Control Inputs

Figure 3 shows a truth table for the three control inputs. Note that minimum durations for these signals are required for proper operation (see the table of Electrical Characteristics for specifications of T_W, T_S, and T_H). T_W is the minimum low state pulse width to guarantee enabling the latch. The data (bit) inputs must also stay in a known state for a minimum amount of time, both before and after the control signal goes high again. The time before the control input goes high is T_S, the data set-up time, and the time after is T_H, the data hold time. This timing is generally created through wait statements in the computer program, or with a one shot if necessary.

The specifications for logic current into the control inputs seem to imply that the logic driving the inputs must have a high output current capability, but note that the logic high is specified at 5.5V, while the logic threshold is down at 1.4V. The actual requirement is for the logic to supply 15μA at 2V, which is within the capability of CMOS and PMOS.

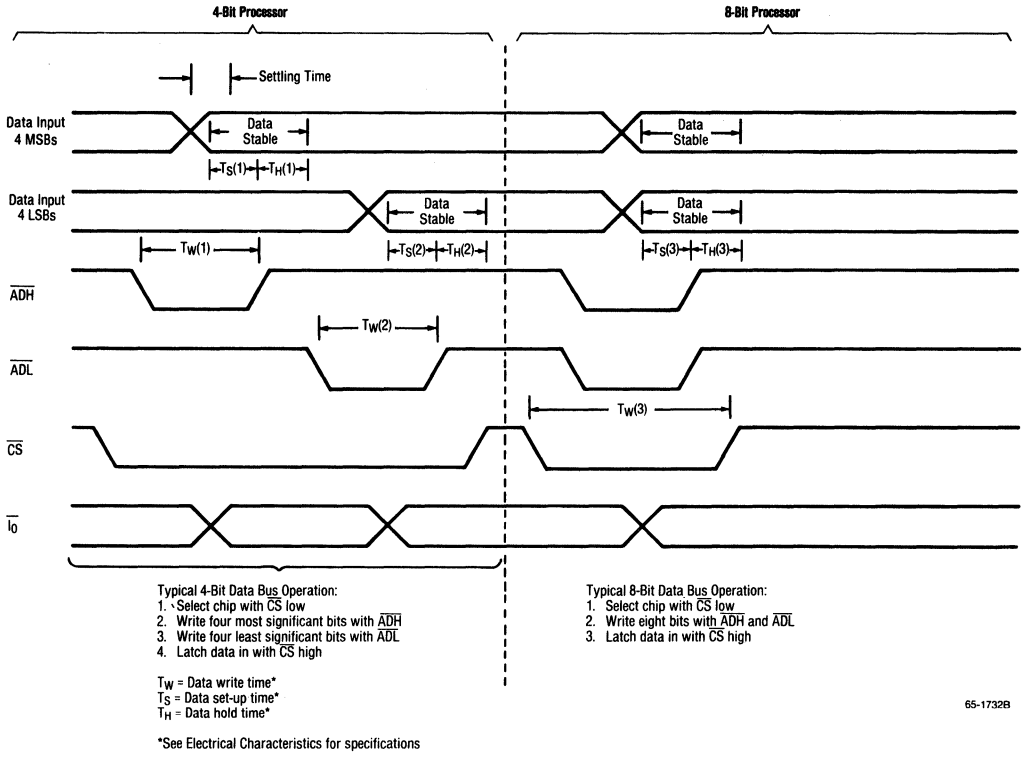


Figure 2. Timing Diagram

If all the control bits are wired to ground then the DAC-4888 will function just like a conventional D/A converter; that is, any data input will immediately flow through to the output.

$\overline{CS}$	$\overline{ADH}$	$\overline{ADL}$	Result
1	X	X	All inputs disabled - output latched
0	0	0	All inputs active
0	0	1	4 MSBs active - others latched
0	1	0	4 LSBs active - others latched
0	1	1	All inputs disabled - output latched

X = don't care

Figure 3. Control Input Truth Table

Analog Output

The heart of the DAC-4888 is a binary weighted current source DAC. Refer to the Functional Block Diagram.

The reference amplifier forces the reference amplifier input (pin 23, Gain Adjust) to virtual ground (0V). When the +6.3V reference voltage is connected to pin 14 the entire 6.3V is applied across the 6.3kΩ reference resistor. The resultant 1mA current (6.3V/6.3K = 1mA) flows into the ref amp input where it is mirrored and scaled by the binary weighted current sources. The scaling of these current sources is such that the full scale output current is four times the input current; for a 1mA reference the full scale output will be -4mA. (Actually, because the code combination starts at all bits zero for 0 current output, the full scale current is -4mA +LSB, which is -3.98438mA. For a similar reason with 3 decimal digits one can only count up to 999, not to 1000.)

Two outputs are provided, I_O and $\overline{I_O}$. The logic inputs can be complemented (the sense of 1

and 0 reversed) by taking the output from $\overline{I_O}$ instead of I_O. For all zeros at the bit inputs $\overline{I_O}$ will be at full scale, -3.98438mA. If either output is unused it should be grounded, and not left unconnected.

An option for bipolar output (both positive and negative output currents over the input code range — normally both output currents are negative — current flowing into the DAC) is provided with the bipolar offset resistor between pins 14 and 15. For example, what if I_O is connected to pin 15, and I_O is also monitored with a current meter to ground? The reference voltage connected to pin 14 will be applied across the bipolar offset resistor, because pin 15 is wired to ground through the current meter. This creates a 2mA offset current (6.3V/3.15K = 2mA) which adds to the normal output current. So, for all zeros at the inputs the output will be +2mA. For all ones at the inputs the output will be at -2mA +1LSB (-3.98438mA +2mA = -1.98438mA).

The op amp is provided as a current to voltage converter, i.e., it changes the -4mA output current into a selectable output voltage. When the output current is connected to the sum node (pin 20 to pin 18), all of the current will flow into the sum node, and having nowhere else to go, will flow through the 2.5K span resistors and into the op amp output. Feedback holds the sum node at virtual ground (0V); the IR drop across the span resistor adds to the 0V virtual ground to produce a proportional output voltage at the op amp output.

For example, if pin 16 is wired to pin 13, no offset resistor used, and full scale current of ≈ -4mA is flowing into I_O, then 4mA will flow out of the op amp output, through the 2.5K resistor, and into I_O. 4mA x 2.5K = 10V, so V_{OUT} will equal approximately +10V. Figure 4 shows a table of all the possible combinations of offset and output ranges.

Output Range (zeros to ones)	Pin Connections (always connect 14 to 24 for internal ref)
0 → +5V	17 to 18, 13 to 16, 18 to 20, 19 to Gnd
+5V → 0	17 to 18, 13 to 16, 18 to 19, 20 to Gnd
0 → +10V	13 to 16, 18 to 20, 19 to Gnd
+10V → 0	13 to 16, 18 to 19, 20 to Gnd
-2.5V → +2.5V	13 to 16, 15 and 17 to 18, 18 to 20, 19 to Gnd
+2.5V → -2.5V	13 to 16, 15 and 17 to 18, 18 to 19, 20 to Gnd
-5V → +5V	13 to 16, 15 to 18, 18 to 20, 19 to Gnd
+5V → -5V	13 to 16, 15 to 18, 18 to 19, 20 to Gnd
-10V → +10V	13 to 17, 15 to 18, 18 to 20, 19 to Gnd
+10V → -10V	13 to 17, 15 to 18, 18 to 19, 20 to Gnd

Figure 4. Connections for Various Output Formats

Some improvement of settling time can be made with the addition of R_{sum} and C_F in Figures 7 and 8. Figure 5 gives a table of values for the various output ranges. C_F can also be added in applications where speed is not critical but output noise is. Larger values of C_F will overcompensate the amplifier, slowing it down, but simultaneously integrating out high frequency noise. For most applications the noise produced by the reference will be well within acceptable limits; however, for noise sensitive applications it can be reduced by adding a 1.0μF capacitor from the reference output to ground (see Figure 6). A graph of noise performance with and without this capacitor is given in the section on Typical Performance Characteristics.

Output Range	C_F	R_{sum}
0V to +5V	15pF	10K
0V to +10V	5pF	2.5K
±2.5V	15pF	3.3K
+5V	0pF	∞
±10V	0pF	∞

Figure 5. Component Values for Improved Settling Time

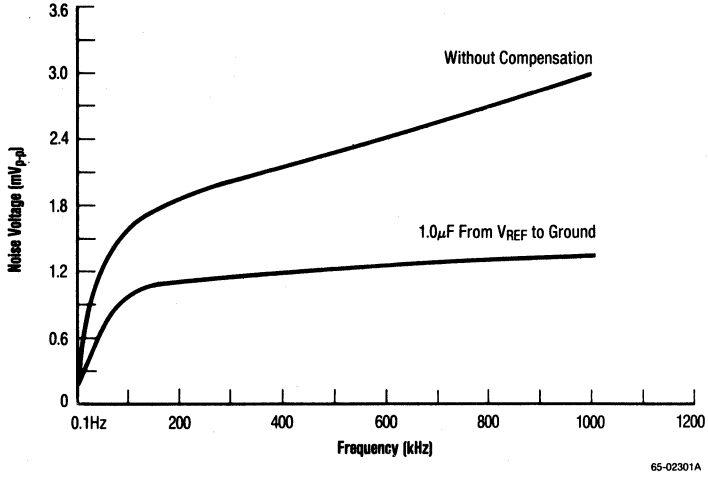
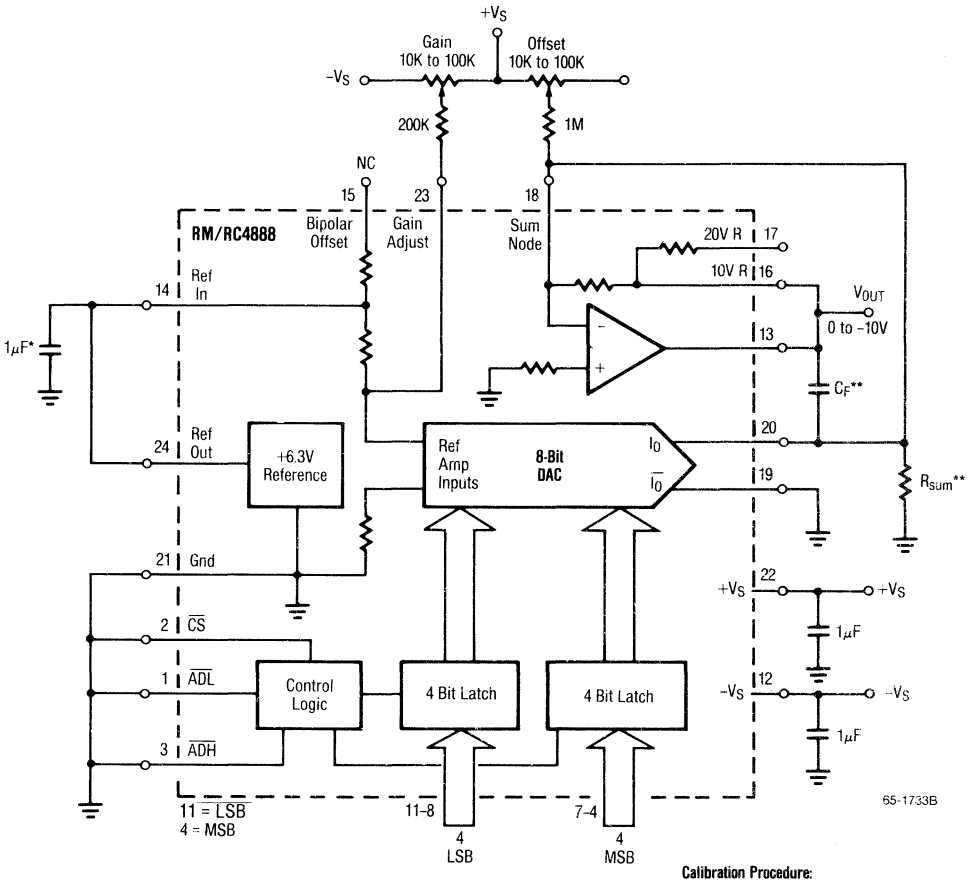


Figure 6. 4888 Broadband Noise

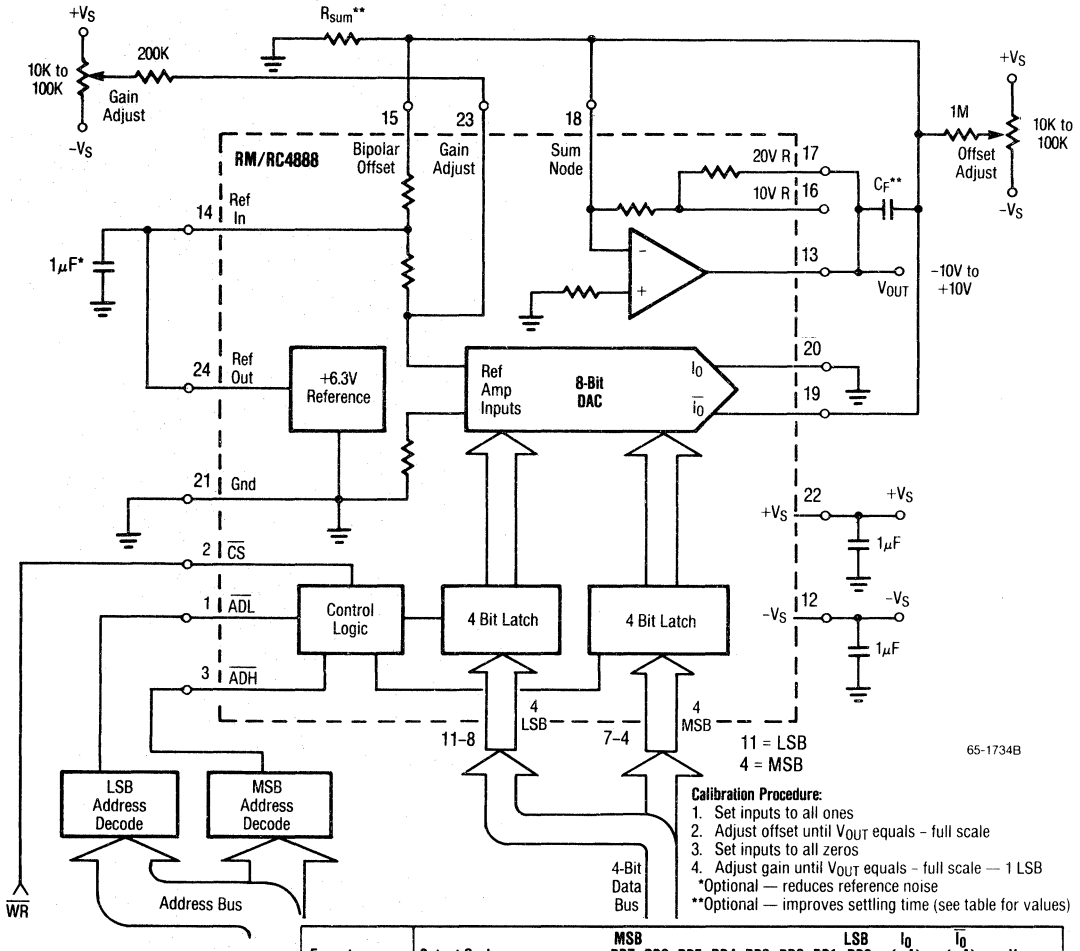


Calibration Procedure:
1. Set inputs to all zeros
2. Adjust offset until V_{OUT} equals 0V
3. Set inputs to all ones
4. Adjust gain until V_{OUT} equals correct full scale value

*Optional — reduces reference noise
**Optional — improves settling time (see table for values)

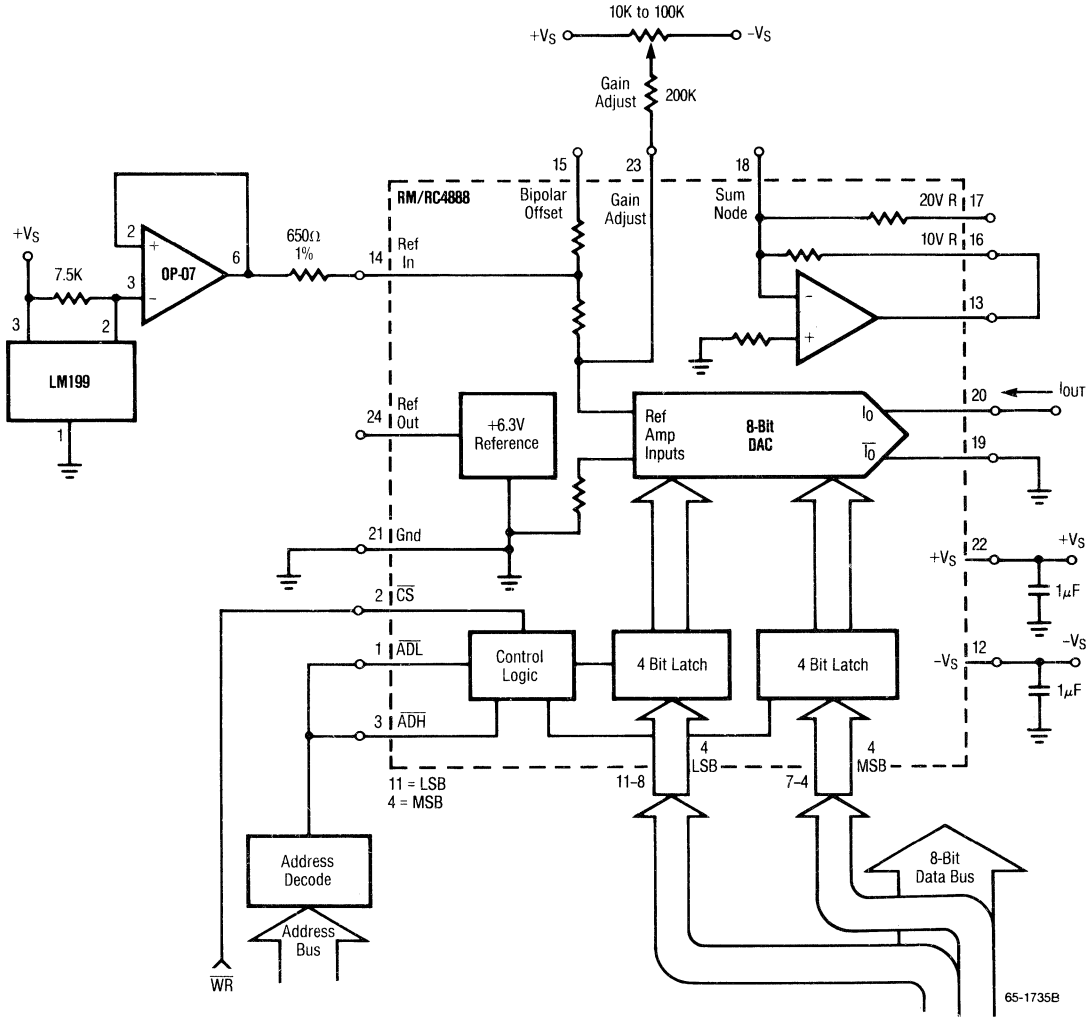
Format	Output Scale	MSB DB7	DB6	DB5	DB4	DB3	DB2	DB1	LSB DB0	I_O (mA)	$\overline{I_O}$ (mA)	V_{OUT}
Straight Binary: Unipolar With True Input Code. True Zero Output	Positive Full Scale	1	1	1	1	1	1	1	1	3.999	0.000	9.9609
	Positive Full Scale - LSB	1	1	1	1	1	1	1	0	3.984	0.001	9.9219
	LSB	0	0	0	0	0	0	0	1	0.0001	3.984	0.0391
	Zero Scale	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary Binary: Unipolar With Complementary Input Code. True Zero Output	Positive Full Scale	0	0	0	0	0	0	0	0	0.000	3.999	9.9609
	Positive Full Scale - LSB	0	0	0	0	0	0	0	1	0.001	3.984	9.9219
	LSB	1	1	1	1	1	1	1	0	3.984	0.001	0.0391
	Zero Scale	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

Figure 7. Stand-Alone, 0 to +10V, 8-Bit Straight Binary With Gain and Offset Adjust Connections



Format	Output Scale	MSB DB7	DB6	DB5	DB4	DB3	DB2	DB1	LSB DB0	IO (mA)	$\overline{I_O}$ (mA)	VOUT
Offset Binary: True Zero Output	Positive Full Scale	1	1	1	1	1	1	1	1	3.999	0.000	9.9219
	Positive Full Scale - LSB	1	1	1	1	1	1	1	0	3.984	0.001	9.8438
	+LSB	1	0	0	0	0	0	0	1	2.001	1.992	0.0781
	Zero Scale	1	0	0	0	0	0	0	0	0.000	2.000	1.999
	-LSB	0	1	1	1	1	1	1	1	1.999	2.000	-0.0781
	Negative Full Scale - LSB	0	0	0	0	0	0	0	1	0.001	3.984	-9.9219
	Negative Full Scale	0	0	0	0	0	0	0	0	0.000	3.999	-10.000
2's Complement: True Zero Output MSB Complemented (Need Inverter at DB7)	Positive Full Scale	0	1	1	1	1	1	1	1	3.999	0.000	9.9219
	Positive Full Scale - LSB	0	1	1	1	1	1	1	0	3.984	0.001	9.8438
	+LSB	0	0	0	0	0	0	0	1	2.001	1.992	0.0781
	Zero Scale	0	0	0	0	0	0	0	0	2.000	1.999	0.0000
	-LSB	1	1	1	1	1	1	1	1	1.999	2.000	-0.0781
	Negative Full Scale - LSB	1	0	0	0	0	0	0	1	0.001	3.984	-9.9219
	Negative Full Scale	1	0	0	0	0	0	0	0	0.000	3.999	-10.000

Figure 8. Microprocessor Interface, 4-Bit Data Bus, +10V to -10V Output With Complementary Binary Input (All Zeros Equal — Full Scale)

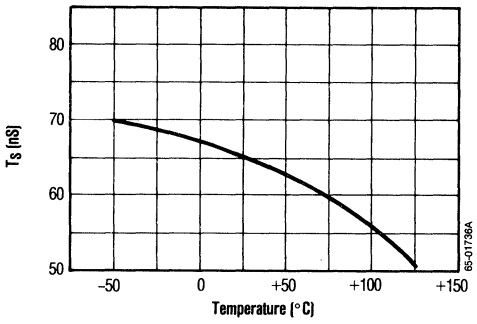


Calibration Procedure:
Zero scale error is entirely leakage current — no adjustment necessary
1. Set inputs to all ones
2. Adjust gain until I_O equals correct full scale value

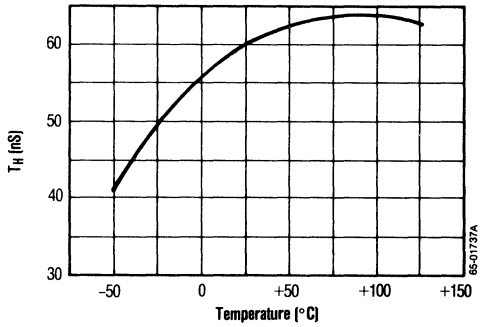
Figure 9. Microprocessor Interface, 8-Bit Data Bus, 0 to -4mA Output With Straight Binary Input and External Reference

Typical Performance Characteristics

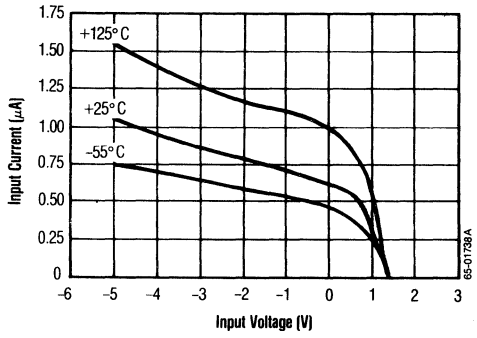
Data Set-Up Time vs. Temperature



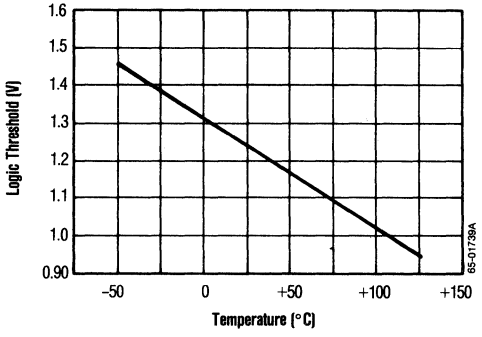
Data Hold Time vs. Temperature



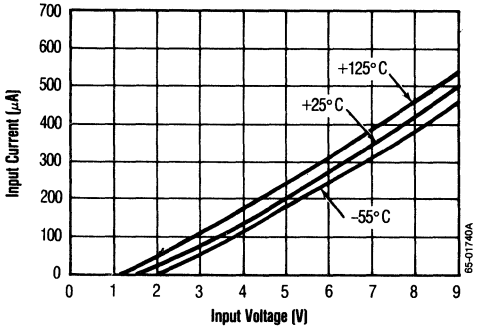
Digital Input Current vs. Voltage



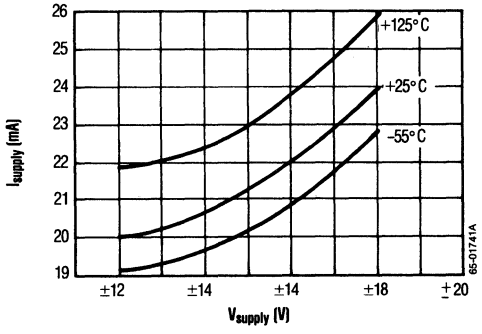
Logic Threshold vs. Temperature



Control Input Current vs. Voltage

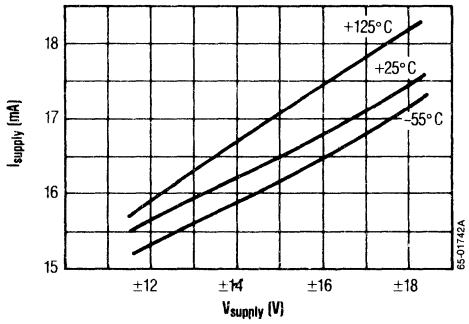


Negative Supply Current vs. Supply Voltage

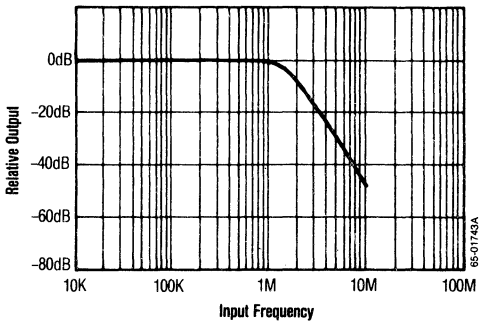


Typical Performance Characteristics (Continued)

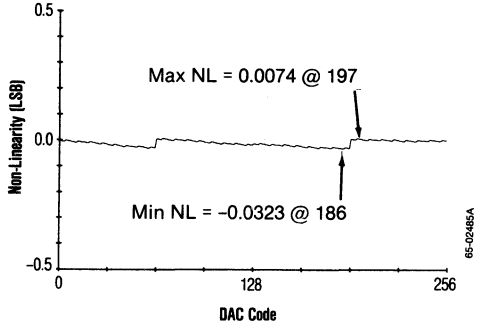
Positive Supply Current vs. Supply Voltage

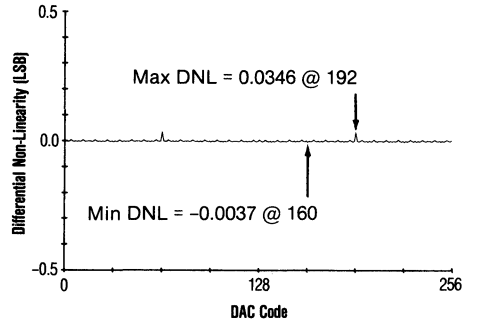


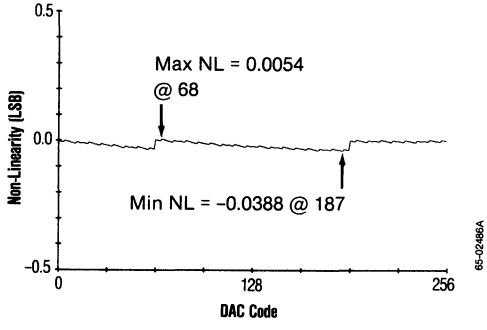
Reference Input Multiplying Frequency Response (V_S 100mV_{p-p})

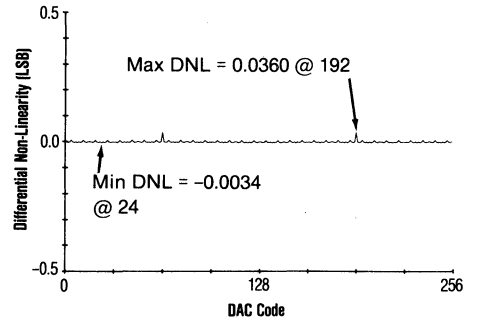


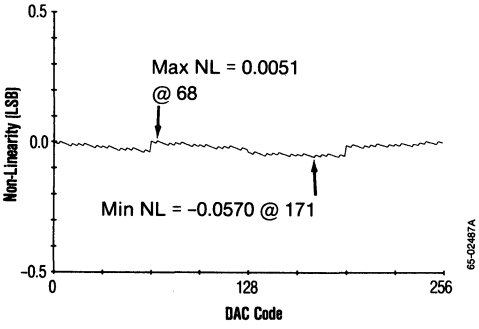
DAC Accuracy Over Full Temperature Range

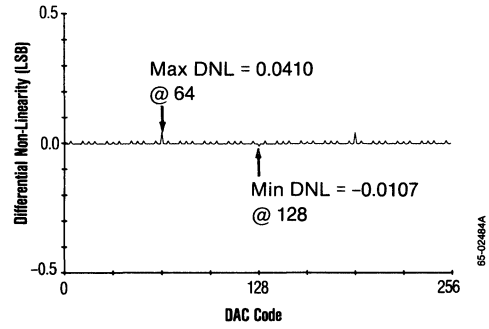








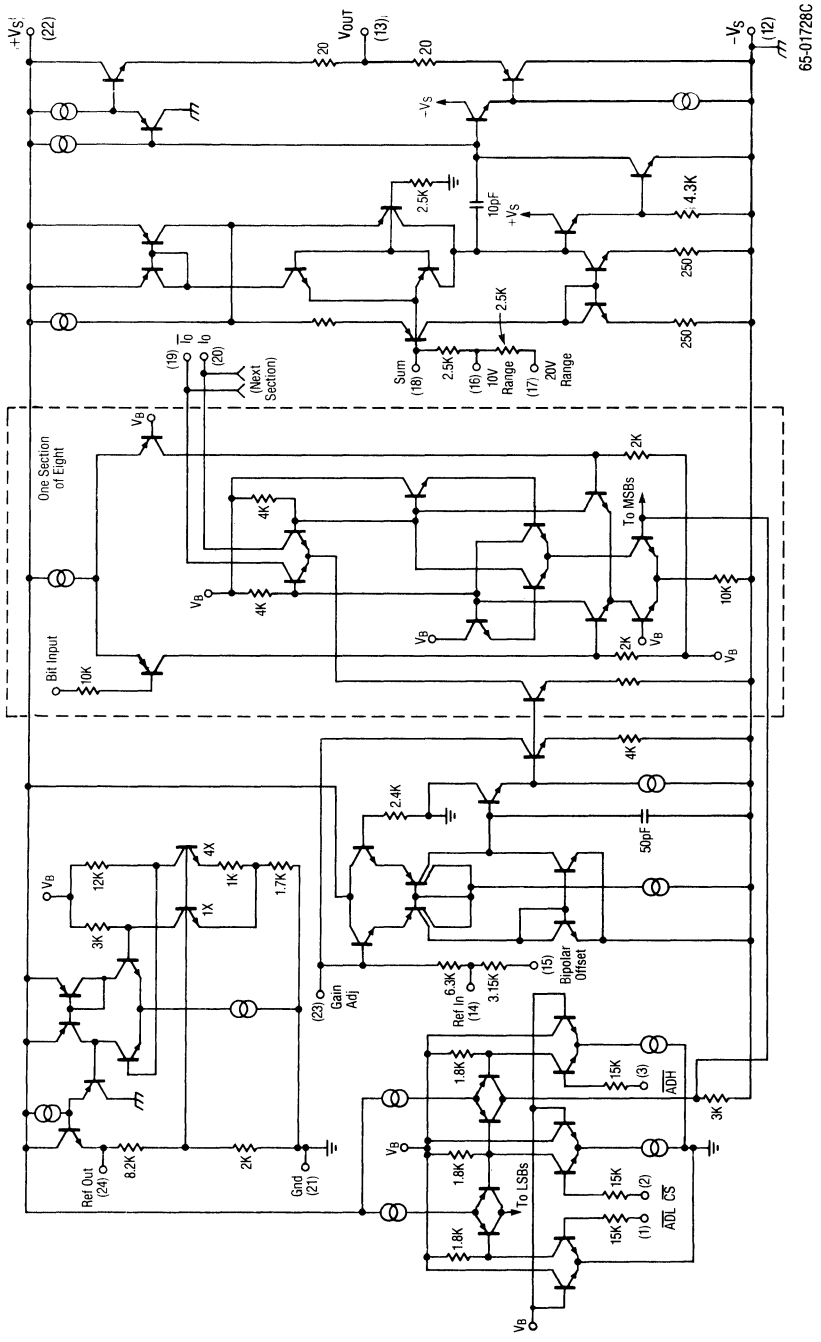




DAC-4888 Linearity Plots

> Internal Reference
> 10V Unipolar Mode
> +V = +15V, -V = -15V
> Typical Sample

Simplified Schematic Diagram



DAC-6012 12-Bit High Speed Multiplying D/A Converter

Features

- Differential nonlinearity — 0.012% (13 bits)
- Guaranteed monotonicity to 12 bits over temperature
- Relative accuracy — 0.05% all grades
- Fast settling time — 250nS to ±0.5 LSB
- Full scale output current — 4mA
- Complementary current outputs
- Output compliance — -5V to +10V
- Full scale tempco — ±10ppm/°C
- Power consumption — 230mW
- Direct interface to all major logic families
- Standard processing without resistor trimming

Description

The Raytheon DAC-6012 series of monolithic Multiplying Digital-to-Analog Converters guarantee differential nonlinearity to better than ±0.5 LSB (0.012%) for the 6012A and ±1 LSB (0.025%) for the 6012 over the full military and commercial temperature ranges. In addition to the excellent differential nonlinearity specifications, the 6012 series also include many features that previously were found in expensive hybrid modules or required full use of monolithic thim film laser or zener zap trimming techniques.

The Raytheon DAC-6012 incorporates a segmented design technique which reduces the requirement for high accuracy resistor ladder networks as an integral part of the DAC. The DAC-6012 design is structured with a 3-bit segment decoder, 5-bit master R-2R ladder DAC and 4-bit Slave DAC. This circuit configuration actually contains less ladder resistors than the traditional R-2R ladder approach as well as effectively improving the accuracy of the ladder resistors by a factor of 8.

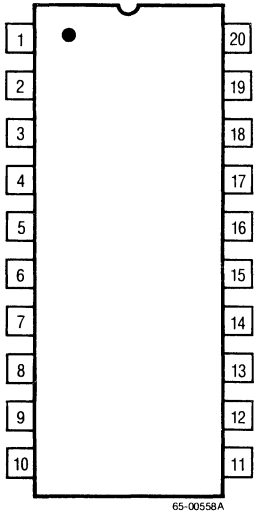
The performance of the DAC-6012 is virtually independent of supply voltage variations due to the inherent nature of its design and processing. As an example, the DAC-6012 may be operated at any voltage from +4/-10V to ±18V with minimal effect on the full scale current, DNL, relative accuracy and settling time. The 5MΩ output impedance and -5V to +10V compliance range make the DAC-6012 ideal for high speed applications where output load resistors can be used in place of an output interface amplifier.

The complementary current outputs of the DAC-6012 are useful in symmetrical offset DAC applications and A/D converters requiring constant current loads to ensure significant reduction of switching transients.

In conjunction with the REF-01 and REF-02 voltage references, and the RC4805 fast precision voltage comparator, the DAC-6012 can be used as the main building block in a wide variety of data conversion applications.

Connection Information

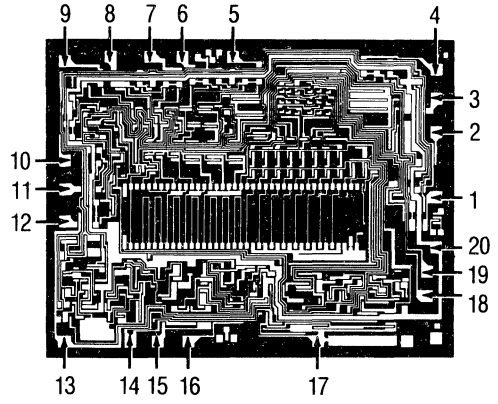
20-Lead Ceramic Dual In-Line
(Top View)



65-00558A

Pin	Function
1	MSB B1
2	B2
3	B3
4	B4
5	B5
6	B6
7	B7
8	B8
9	B9
10	B10
11	B11
12	B12 LSB
13	V_{LC}/A_{GND}
14	$V_{REF}(+)$
15	$V_{REF}(-)$
16	Comp
17	$-V_S$
18	I_O
19	$\overline{I_O}$
20	$+V_S$

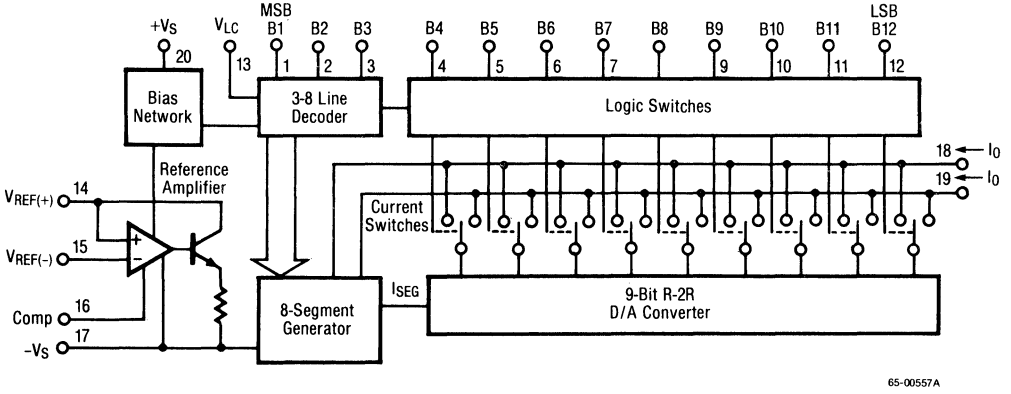
Mask Pattern



65-02064A

Die Size: 104 x 133 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram



65-00557A

Absolute Maximum Ratings

Power Supply Voltage .....±18V
Logic Inputs.....-5V to +18V
Analog Current Outputs .....-8V to +12V
Reference Inputs V_{14},V_{15}.....$-V_S$ to $+V_S$
Reference Input Differential
Voltage (V_{14}, V_{15}).....±18V
Reference Input Current (I_{14}) .....1.25 mA
Operating Temperature Range
DAC-6012AMD, MD .....-55°C to +125°C
DAC-6012ACN, CN .....0°C to +70°C
Storage Temperature
Range .....-65°C to +150°C
Lead Soldering Temperature
(60 Sec) .....+300°C

Thermal Characteristics

	20-Lead Plastic DIP	20-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A <50°C	1000 mW	1042 mW
Therm. Res θ_{JC}	35°C/W	60°C/W
Therm. Res. θ_{JA}	75°C/W	120°C/W
For T_A >50°C Derate at	13.33 mW/°C	8.38 mW/°C

Ordering Information

Part Number	Package	Operating Temperature Range
DAC-6012ACN	N	0°C to +70°C
DAC-6012CN	N	0°C to +70°C
DAC-6012AMD	D	-55°C to +125°C
DAC-6012MD	D	-55°C to +125°C
DAC-6012AMD/883B	D	-55°C to +125°C
DAC-6012MD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 20-lead plastic DIP
D = 20-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Electrical Characteristics

(V_S = ±15V, I_{REF} = 1.0mA, over the operating temperature range unless otherwise specified)

Parameters	Test Conditions	DAC-6012A			DAC-6012			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Differential Nonlinearity	Deviation From Ideal Step Size			±0.012			±0.025	%FS
		13			12			Bits
Nonlinarity	Deviation From Ideal Straight Line			±0.05			±0.05	%FS
Full Scale Current	V_{REF} = 10.000V $R_{14} = R_{15}$ = 10.000kΩ T_A = +25°C	3.967	3.999	4.031	3.935	3.999	4.063	mA
Full Scale Tempco[1]			±5.0	±20		±10	±40	ppm/°C
			±0.0005	±0.002		±0.001	±0.004	%FS/°C
Output Voltage Compliance	D.N.L. Specification Guaranteed Over Compliance Range R_{OUT} > 10MΩ Typ.	-5.0		+10	-5.0		+10	V
Full Scale Symmetry	$I_{FS} - I_{FS}$		±0.2	±1.0		±0.4	±2.0	μA
Zero Scale Current				0.2			0.2	μA
Settling Time[1]	To ±1/2 LSB, All Bits ON or OFF, T_A = +25°C		250	500		250	500	nS
Propagation Delay — All Bits[1]	50% to 50%		25	50		25	50	nS
Output Capacitance			20			20		pF
Logic Input Levels Logic "0"				0.8			0.8	V
Logic "1"		2.0			2.0			
Logic Input Current	V_{IN} -5.0V to +18V			40			40	μA
Logic Input Swing	V_S = -15V	-5.0		+18	-5.0		+18	V
Reference Current Range		0.2	1.0	1.1	0.2	1.0	1.1	mA
Reference Bias Current		0	-0.5	-2.0	0	-0.5	-2.0	μA
Reference Input Slew Rate[1]	$R_{14(eq)}$ = 800Ω C_C = 0pF	4.0	8.0		4.0	8.0		mA/μS
Power Supply Sensitjvity Positive	V_S = +13.5V to +16.5V, V_S = -15V		±0.0005	±0.001		±0.0005	±0.001	%FS/%
Negative	V_S = -13.5V to -16.5V, V_S = +15V		±0.00025	±0.001		±0.00025	±0.001	

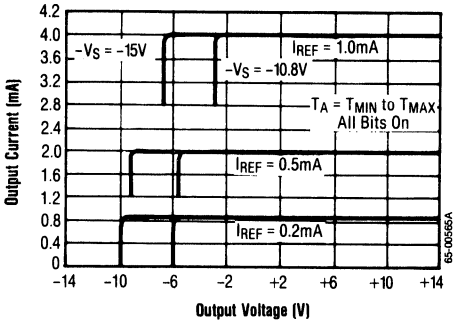
Note: 1. Guaranteed by design.

Electrical Characteristics (Continued)

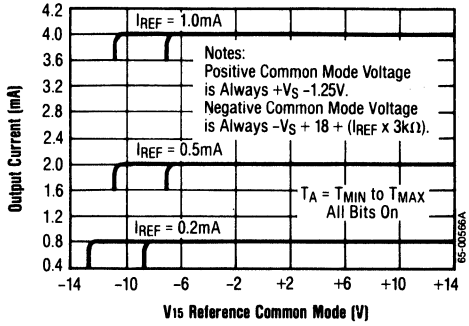
Parameters	Test Conditions	DAC-6012A			DAC-6012			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Range								
Positive	V_{OUT} = 0V	4.5		18	4.5		18	V
Negative		-18		-10.8	-18		-10.8	
Power Supply Current								
Positive	V_S = +5.0V, V_S = -15V		5.7	8.5		5.7	8.5	mA
Negative			-13.7	-18		-13.7	-18	
Positive	V_S = +15V, V_S = -15V		5.7	8.5		5.7	8.5	
Negative			-13.7	-18		-13.7	-18	
Power Dissipation	V_S = +5.0V, V_S = -15V		234	312		234	312	mW
	V_S = +15V, V_S = -15V		291	397		291	397	

Typical Performance Characteristics

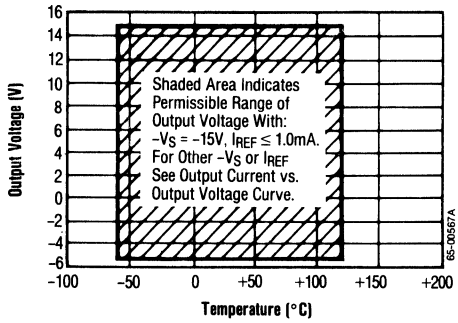
Output Current vs. Output Voltage (Output Voltage Compliance)



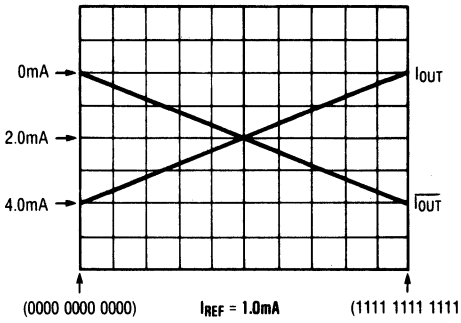
Reference Amplifier Common Mode Range



Output Compliance vs. Temperature



True and Complementary Output Operation



Segmented Design Information

To achieve the linearity necessary to manufacture a 12-bit DAC, previously designed 12-bit DACs have required the use of high precision trimmed thin film resistors arranged in an R-2R ladder configuration (Figure 1). The DAC-6012 deviates from the traditional design by using a segment decoder controlled by bit 1 (MSB) through bit 3. Bits 4 through bit 12 (LSB) control a 9-bit master/slave DAC similar in design to the type used in the DAC-08 and DAC-10 8-bit and 10-bit DACs. The 3-bit segment decoder consists of 8 equal current sources of 0.5 I_{REF} each, and a priority decoder which determines, through the 3-bit code, which one and only one of 8 current sources provide the reference current to the 9-bit DAC and which of the other 7 feed either the I_O or $\overline{I_O}$ ports (Figure 2).

As an example, when bit 1 through bit 3 are 000, the I_A current source is used as the reference current for the 9-bit DAC, I_B through I_H go to the $\overline{I_O}$ port. The outputs of the 9-bit DAC go to either I_O or $\overline{I_O}$ depending on the code at bits 4 through 12. A major segment decoder transition occurs when the code changes from (MSB) 000111111111 (LSB) to 001000000000.

At the transition the I_A current source switches from the 9-bit DAC to the I_O port and the I_B current source switches from $\overline{I_O}$ to become the reference current for the 9-bit DAC, which has just changed from its full scale current (I_A -1 LSB) to its zero scale current at the I_O port. As the input code is increased toward 4095_{10}, the output of each segment current source is switched from $\overline{I_O}$ to become the reference current for the 9-bit DAC, and is then switched to I_O.

Monotonicity is guaranteed using this technique since the current source that was used as the 9-bit DAC reference current is then added directly to the I_O port when the 9-bit DAC changes from its full scale to its zero scale current.

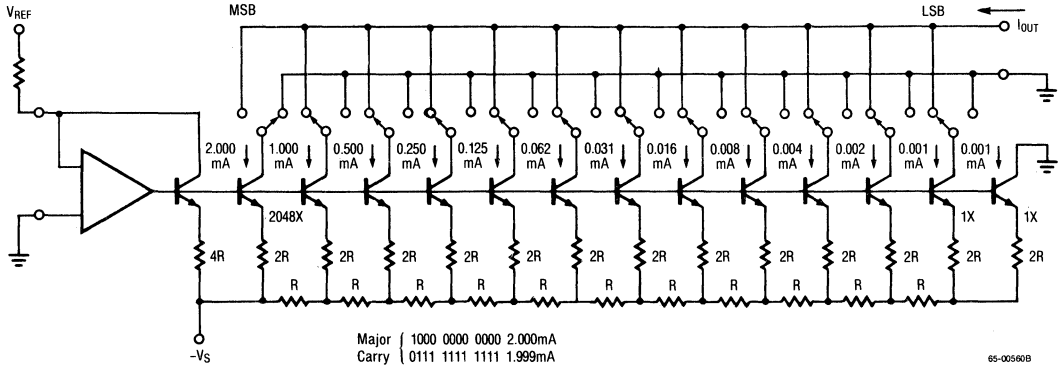


Figure 1. Traditional R-2R D/A Converter

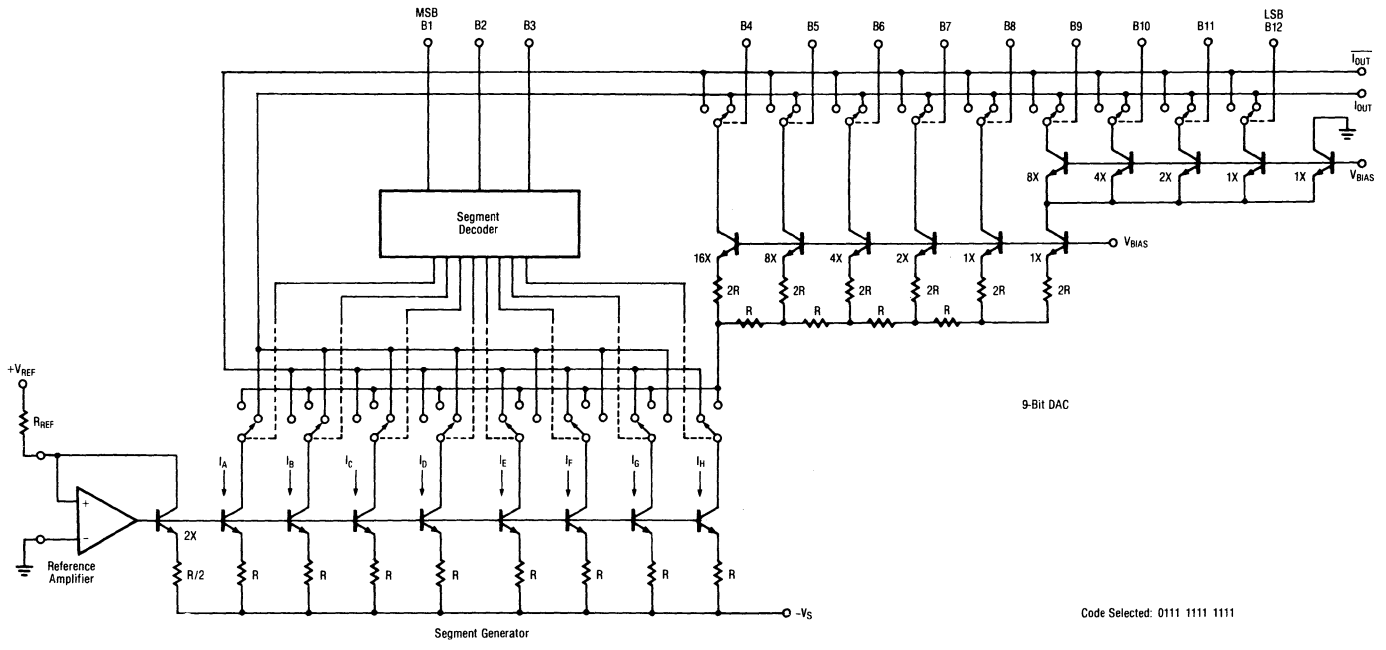


Figure 2. 3-Bit Segment Decoded 12-Bit DAC

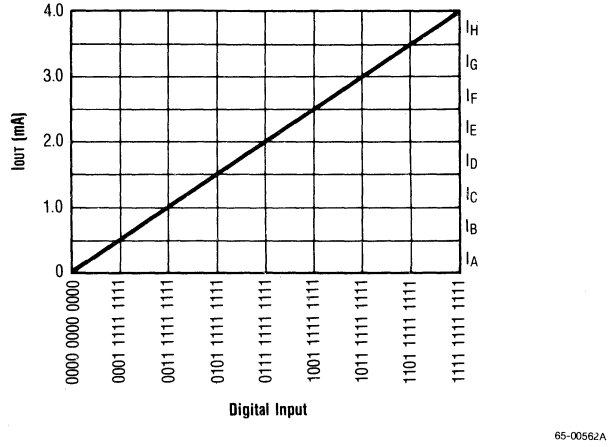


Figure 3. I_O vs. Code for DAC-6012

Recommended Basic Connections

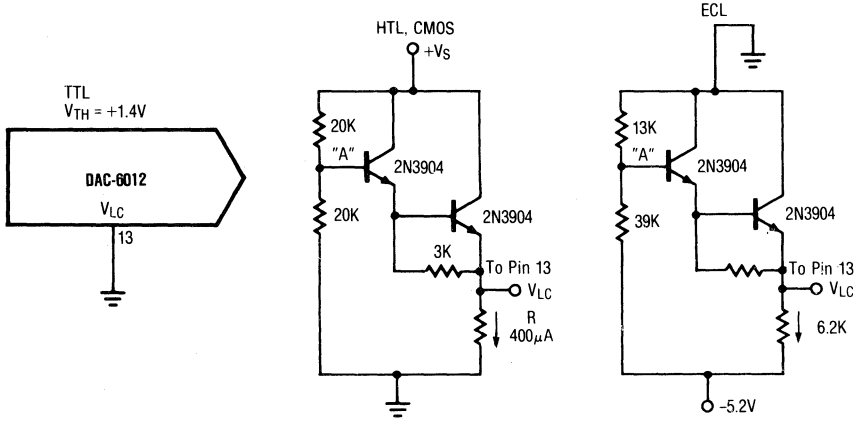
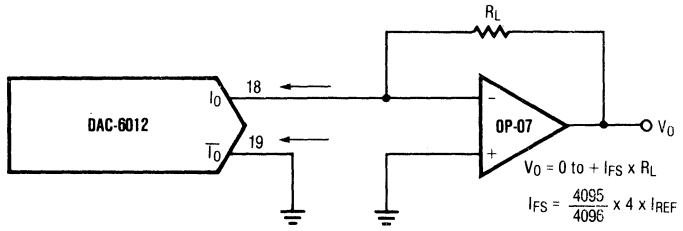


Figure 4. Interfacing With Various Logic Families

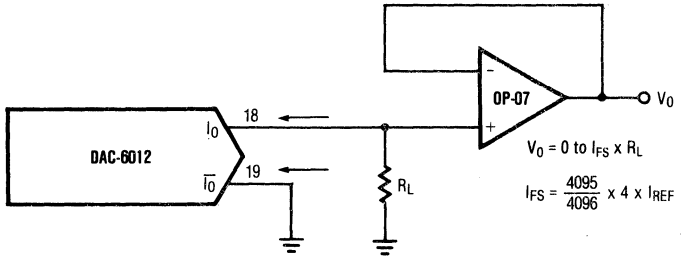
Recommended Basic Connections (Continued)



For Complementary Output (Operation as a Negative Logic DAC), Connect Inverting Input of Op Amp to $\overline{I_O}$ (Pin 19); Connect I_O (Pin 18) to Ground.

65-00569A

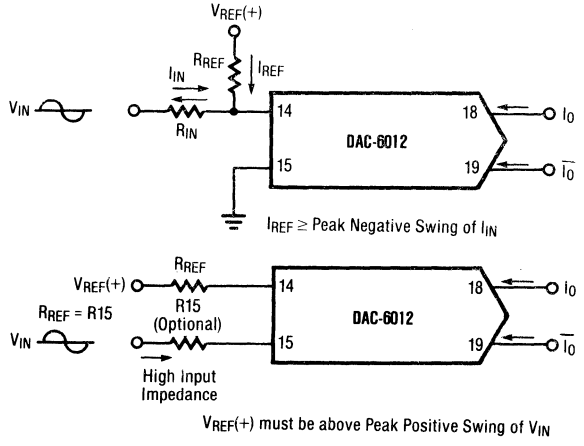
Figure 5. Negative Low Impedance Output Operations



For Complementary Output (Operation as a Negative Logic DAC), Connect Inverting Input of Op Amp to $\overline{I_O}$ (Pin 19); Connect I_O (Pin 18) to Ground.

65-00570A

Figure 6. Positive Low Impedance Output Operations



65-00571A

Figure 7. Accommodating Bipolar References

Recommended Basic Connections (Continued)

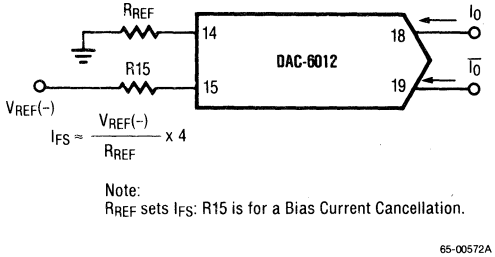


Figure 8. Basic Negative Reference Operation

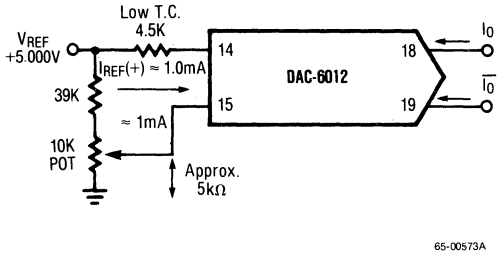


Figure 9. Recommended Full Scale Adjustment Circuit

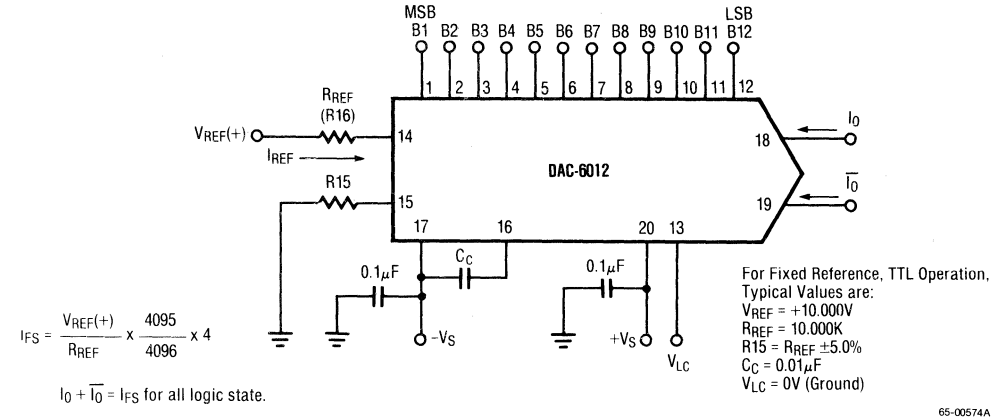


Figure 10. Basic Positive Reference Operation

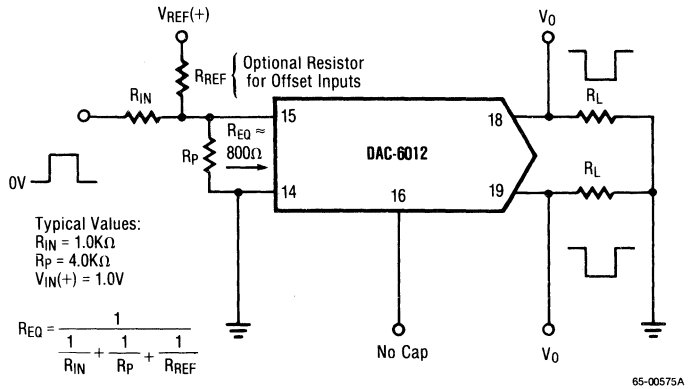
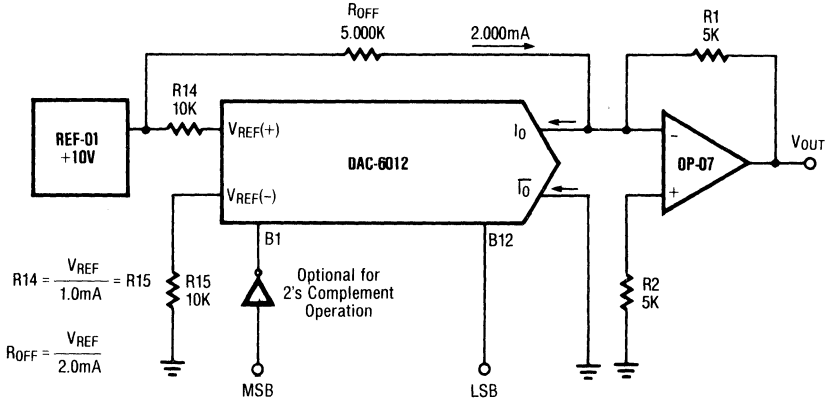


Figure 11. Pulsed Reference Operation

Recommended Basic Connections (Continued)



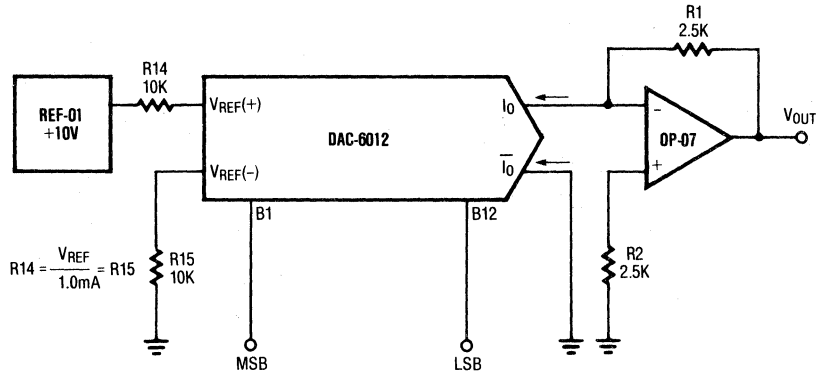
Note: Code may be Complemented by Reversing I_O and $\overline{I_O}$.

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Offset Binary; True Zero Output.	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0000
	- LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951
	Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000
2's Complement; True Zero Output MSB Complemented (need Inverter at B1).	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951
	Positive Full Scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902
	+ LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0000
	- LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049
	Negative Full Scale + LSB	1	0	0	0	0	0	0	0	0	0	0	0	0.001	3.998	-9.9951
	Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000

65-00576B

Figure 12. Bipolar Offset (True Zero)

Recommended Basic Connections (Continued)



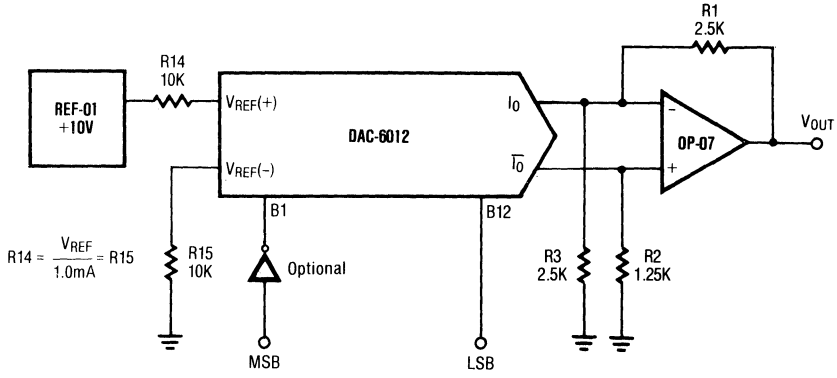
Note: Code may be Complemented by Reversing I_O and $\overline{I_O}$.

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Straight Binary; Unipolar with True Input Code, True Zero Output.	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.0001	3.998	0.0024
	Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary Binary; Unipolar with Complementary Input Code, True Zero Output.	Positive Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
	Positive Full Scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
	Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

65-00577B

Figure 13. Basic Unipolar Operation

Recommended Basic Connections (Continued)



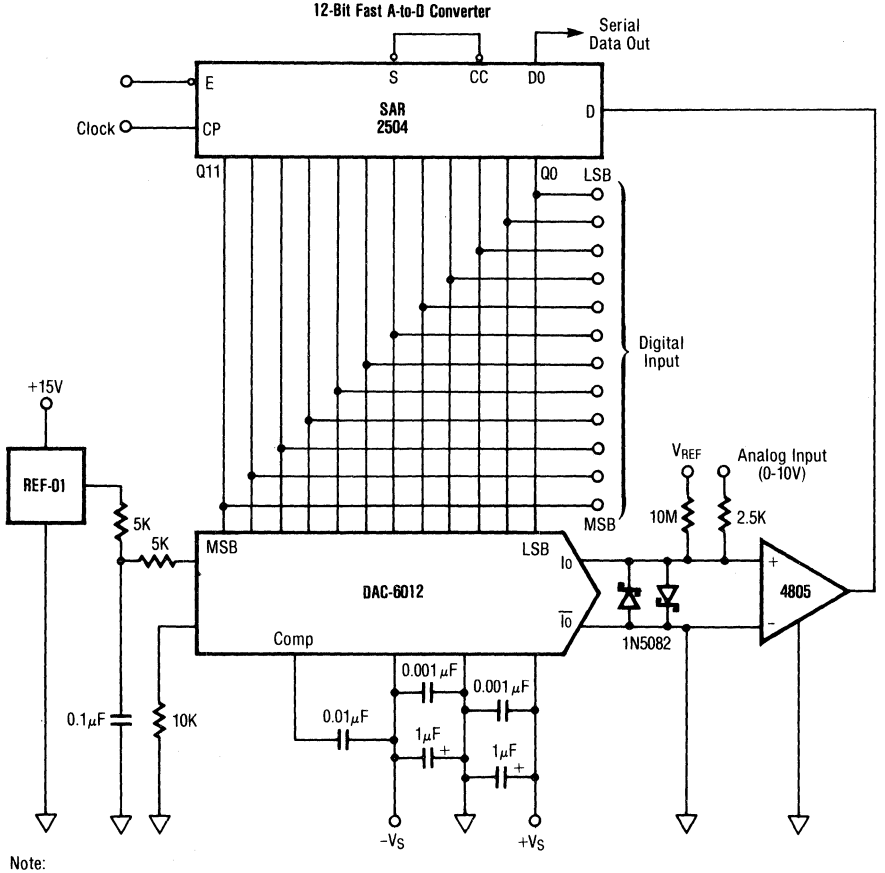
Note: Code may be Complemented by Reversing I_O and $\overline{I_O}$.

Code Format	Output Scale	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_O(mA)	$\overline{I_O}$(mA)	V_{OUT}
Straight Offset Binary; Symmetrical about Zero, No True Zero Output.	Positive Full Scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero Scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative Full Scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
	Negative Full Scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976
1's Complement; Symmetrical about Zero, No True Zero Output MSB Complemented (need Inverter at B1).	Positive Full Scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive Full Scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero Scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero Scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative Full Scale — LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
	Negative Full Scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976

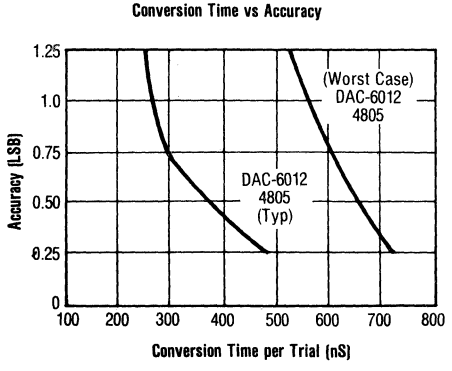
65-00578B

Figure 14. Symmetrical Offset Operation

Recommended Basic Connections (Continued)



Note:
Device(s) connected to analog input must be capable of sourcing 4.0mA a buffer may be required



Conversion Time (nS)	Typ	Worst Case
SAR	33nS	55nS
4805	92nS	125nS
Total	375nS	680nS
x 13	4.9μS	8.8μS

65-00579B

Figure 15. Fast 12-Bit Analog-to-Digital Converter Application

Design and Applications Information

Logic Input

The DAC-6012 uses a unique logic input circuit which allows the user to interface the 6012 with all major logic families. Inputs from -5.0V to +10V may be used when using ±15V supplies. The internal logic threshold is 1.3V nominal and must be adjusted for logic families other than TTL and 5V CMOS by using the circuits in Figure 4. The logic threshold may be adjusted over a wide range using the relationship $V_{TH} = V_{LC} + 1.3V$. Care must be taken when connecting the V_{LC} pin since it typically sinks 3mA. When interfacing with ECL a reference current less than 1mA is recommended since internal voltage compliance problems may exist using negative logic threshold voltages greater than -5V with a -15V supply.

Power Supplies

The DAC-6012 operates over a supply range of +5.0V, -10V to ±18V when using an I_{REF} = 1.0mA. Below -10V voltage headroom limitations inside the DAC-6012 will reduce output compliance to near 0V. Operation below -8V will seriously degrade the overall linearity of the DAC-6012. The positive supply voltage is not critical, and voltage between +4.0V and +18V can be used since most of the circuitry is used to bias the internal logical inputs.

Reference Current and Amplifier

The full scale output current (I_{FS}) at the I_O port is in direct proportion to the reference current into pin 14. The relationship is given as I_{FS} = 4095/4096 I_{REF} x 4 x 4095/4096. When I_{REF} = 1.000mA, I_{FS} = 3.999mA. I_{REF} can be varied over a wide range from 1.0μA to 1.1mA for multiplying digital-to-analog converter applications.

For high accuracy, DC reference application circuits require a high quality voltage reference such as the +10V REF-01 or +5.0V REF-02. A stable output current free from excess noise, supply voltage glitches and temperature variations is possible when using a high quality voltage reference and a low TC high accuracy source resistor. If the reference has a 100ppm/°C TC then the output of the DAC will have a similar TC due to the reference alone. Standard 3 terminal voltage regulators used for regulating logic or op amp supply voltage are normally not accurate enough to be used as a reference for 12-bit DAC applications, and therefore are not recommended.

The close relationship between I_{FS} and I_{REF} (±0.8% max error) will, in many applications, not require adjustment of the source or output scaling resistors. If adjustment is necessary, keep in mind the TC of many potentiometers is poorer than fixed resistors. When using DC references it is recommended to split the source resistor in two and bypass with a 0.01μF capacitor from the junction of the two resistors to analog ground. A resistor connected to analog ground from pin 15 should have an ohmic value similar to the total reference resistor so that reference amplifier input bias current effects can be cancelled.

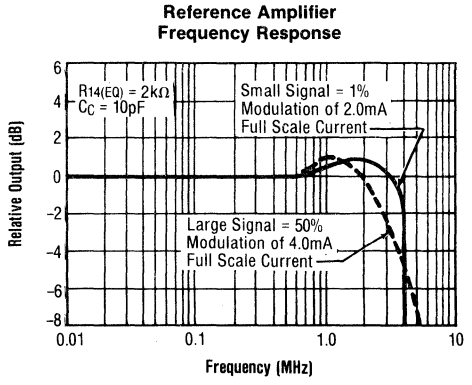
A negative reference voltage may be used as shown in Figure 8. Care must be taken to not exceed the negative common mode voltage of the reference amplifier. This voltage is given by $V_{CM} - = -|-V_S| + 1.8V + (I_{REF} \times 3k\Omega)$.

The reference amplifier must be compensated with a 0.01μF capacitor from pin 16 to pin 17 when using a DC reference. For AC reference applications refer to Figure 16. The value for C_C will depend on the value of the unbypassed source resistor at pin 14. For pulsed reference operation, minimum value source resistors should be used. Compensation is not required for source resistors less than 800Ω, resulting in a fast slew rate and wide bandwidth for the reference amplifier.

For AC reference applications, a minimum value compensation capacitor (C_C) is normally used. The value of this capacitor depends on the equivalent resistance at pin 14. The values to maximize bandwidth without oscillation are as follows:

Minimum Size Compensation Capacitor (I_{FS} = 4.0mA, I_{REF} =1.0mA)

$R_{14(EQ)}$ (kΩ)	C_C (pF)
10	50
5.0	25
2.0	10
1.0	5.0
0.5	0



Note: A 0.01μF capacitor is recommended for fixed reference operation.

65-00563A

Figure 16. Reference Amplifier Compensation

Analog Output Currents

The true (I_O) and complemented ($\overline{I_O}$) outputs both sink current. The sum of I_O and $\overline{I_O}$ equals I_{FS} for all codes. Complementary outputs are useful for driving balanced cables, CRT deflection coils and center tapped transformers. The current at I_O will increase when "1" (true) is applied at any logic input and decrease when "0" (false) is applied to any logic input. Conversely the $\overline{I_O}$ current decreases when a "1" is applied and increases when a "0" is applied.

The output compliance voltage of the DAC-6012 is between +10V to +25V above the $-V_S$ voltage and as such is useful in applications requiring fast current to voltage conversion since load resistors are used in place of an output amplifier.

If either output is unused it should be grounded. It cannot be left unconnected.

Settling Time

Typical full scale settling time to within +0.5 LSB for the DAC-6012 is 250nS using an I_{REF} between 0.5mA and 1.0mA. The full potential of the DAC-6012 is realized only through careful PC board design. Special care must be taken to separate the analog ground from the digital and power supply grounds. Connect the grounds together at one point near the power supply ground. Logic traces must be kept short and supply bypassing near the DAC-6012 must be generous using a minimum of 1.0μF and 0.01μF in parallel.

If output load resistors are used a pole will be created by the 20pF output capacitance of the DAC-6012 and the load resistor. To prevent degradation of the settling time the load resistor must be kept to less than 500Ω.

Measurement of the settling time requires the ability to resolve less than ±0.5μA. The schematic in Figure 17 and a fast, high resolution oscilloscope (250MHz at 2mV/Div.) are capable of measuring settling times to less than ±0.5 LSB at 12 bits (±0.01%).

The MSB of the DAC-6012 determines the overall settling time of 250nS. If the 6012 is operated as a 10-bit DAC by grounding the MSB and LSB pins, settling times of typically 90nS to 130nS can be achieved.

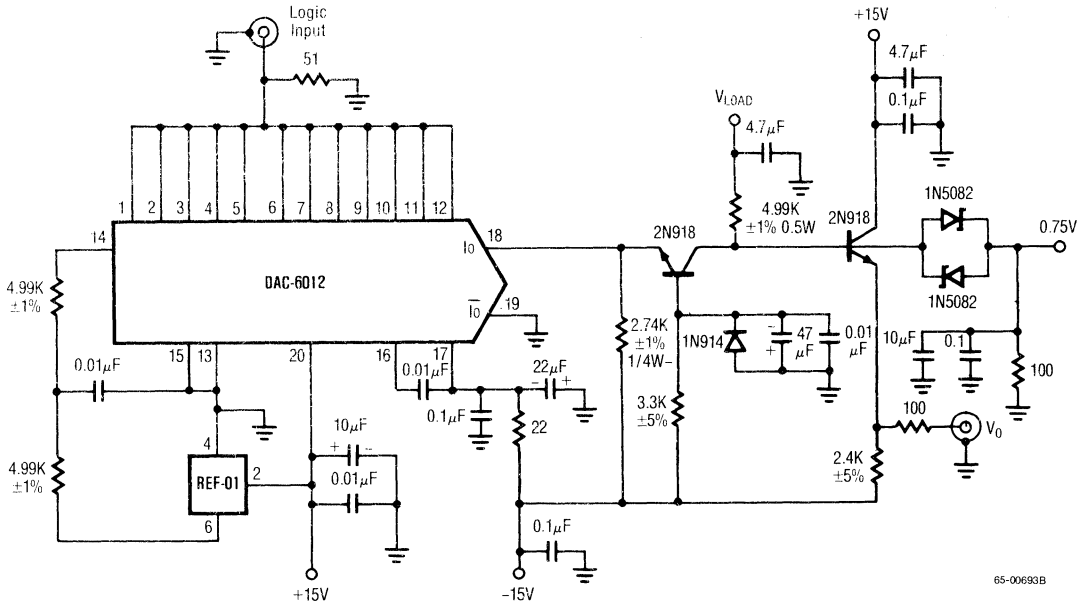


Figure 17. Settling Time Measurement Circuit

Settling Time Measurement

The settling time measurement circuit (Figure 17) must be constructed using the same techniques used for RF circuits. All component leads must be kept short and a very generous ground plane used. Coaxial connectors should be used for the digital input signal as well as the output. 1X probes to monitor the input and output should be used in conjunction with a high speed (>100MHz) oscilloscope with a vertical resolution to at least 2mV/Div. A ±0.5 LSB change at the output of the DAC-6012 will result in a ±2.5mV change at V_O.

A. Set-up procedure — Low to high settling time measurement.
   1. Adjust the DAC-6012 digital inputs to 2V.
   2. Adjust V_{LOAD} so that V_O = 0mV ±10mV. (V_{LOAD} will be about +47V)
   3. Adjust the pulse generator (<10nS rise time) for a 500kHz square wave.
   4. Adjust pulse generator output amplitude so the logic 0 = 0.8V and logic 1 = 2.4V.
   5. Set scope for 100nS/Div. and 2.0mV/Div. and measure time for V_O to fall within ±2.5mV of the final value after the digital inputs change from 0.8V to 2.4V.

B. Set-up procedure — High to low settling time measurement.
   1. Adjust the DAC-6012 digital inputs to 0V.
   2. Adjust V_{LOAD} so that V_O = 0mV ±10mV (V_{LOAD} will abe about +27V).
   3. Repeat steps 3 to 4 above.
   4. Set scope for 100nS/Div. and 2.0mV/Div. and measure time for V_O to fall within ±2.5mV of final value after the digital inputs change from 2.4V to 0.8V.

Temperature Considerations

The DAC-6012 is fully specified for DNL, nonlinearity, and other major DC parameters over temperature. The temperature coefficient (TC) of the full scale output current (I_{FS}) is typically ±8.0ppm/°C drift over the full military temperature range. In most cases, parameters external to the DAC-6012 will contribute most of the errors due to temperature variations. The temperature coefficient (TC) of the reference voltage will cause a directly proportional TC at the output of the DAC-6012. Other factors which enter into the temperature error budget are the TC of the reference (R14) and output scaling resistors. Ideally it should be sufficient that the two resistors track each other so that the TC errors will cancel. Unfortunately the reference resistor power dissipation is constant (assuming a constant reference voltage), therefore, always at a constant temperature rise above the ambient temperature. The output scaling resistor has a power dissipation proportional to the square of the output voltage. For a 0V output in a 10V full scale output system the scaling resistor dissipates 0mW, but at full scale current the resistor (2.5kΩ) is dissipating 40mW. If the TC of the "matched" source and scaling resistors is high enough it can cause a substantial artificial error in the relative accuracy.

DAC-8565 Complete High Speed 12-Bit Monolithic D/A Converter

Features

- Nonlinearity 1/2 LSB — 0.012%
- Differential nonlinearity — 0.012% (13 bits)
- Settles to 1/2 LSB in 300nS
- On-chip buried zener voltage reference
- Linearity guaranteed over temperature
- Low power — 225mW including reference
- Direct interface to all major logic families
- Includes trimmed application resistors

Highlights

- The DAC-8565 is a monolithic 12-Bit DAC that has on-board a self-contained voltage reference plus application resistors.
- The device incorporates interdigitizing of the elements forming the currents of the 3 MSBs of the DAC. Interdigitizing minimizes the effects of thin film sputtering, thermal, and diffusion gradients in the most critical portions of the design. Excellent linearity distributions are achieved prior to trimming, thus ensuring optimal stability of nonlinearity over temperature, as well as ensuring stability versus time.
- The thin film resistors have a trim tab which is distant from the main body of the resistor. This resistor geometry ensures near perfect nonlinearity after trim, and this geometry also reduces damage due to laser trimming.
- The internal reference is laser trimmed to 10 Volts with a ±1.0% maximum error. The reference voltage is available externally and can supply 2mA beyond that required for the reference and bipolar offset resistors.
- The DAC-8565 contains SiCr thin film application resistors which can be used with either an external op amp, creating a precision voltage output DAC, or as input resistors for a successive approximation A/D converter. The resistors are inherently matched and are laser trimmed to guarantee minimum full scale and bipolar offset errors.
- The DAC-8565S grade guarantees linearity and monotonicity over the -55°C to +125°C range and is available fully processed to MIL-STD-883, Level B.

Description

The DAC-8565 is a fast 12-bit digital-to-analog converter. Inside the 24 pin DIP package are all of the circuit functions required for a complete DAC: a stable zener voltage reference, a reference amplifier and resistors, twelve laser trimmed binary weighted current sources, twelve high speed precision current steering switches, and laser trimmed span and bipolar offset application resistors.

The high performance and flexibility of the DAC-8565 are achieved through circuit design and layout, SiCr thin film resistor processing, and interactive computer-controlled laser trimming. The DAC-8565 settles to 1/2 LSB in 300nS typically, with a maximum settling time of 400nS. Accuracy is specified at a **maximum** of 1/2 LSB for all grades.

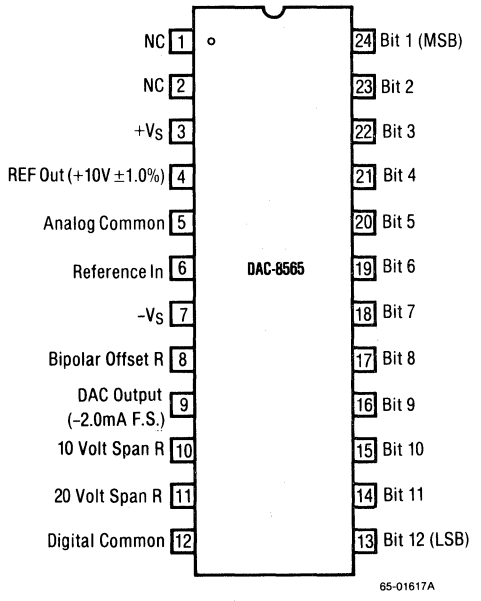
High speed and accuracy coupled with inherent high output impedance make the DAC-8565 the ideal DAC for high speed display drivers, high speed control systems, and in conjunction with the RC4805 high speed latching comparator in anlaog-to-digital converters.

The zener voltage reference is laser trimmed to optimize both temperature drift and absolute output voltage. Typical reference drift is better than 15 ppm/°C (S and J grade).

The DAC-8565 is available in three performance grades. The DAC-8565JS and DS grades are specified over 0°C to +70°C, while the SS grade is specified over the -55°C to +125°C temperature range.

Connection Information

24-Lead Sidebrazed DIP
(Top View)



Ordering Information

Part Number	Package	Operating Temperature Range
DAC-8565DS	S	0°C to +70°C
DAC-8565JS	S	0°C to +70°C
DAC-8565SS	S	-55°C to +125°C
DAC-8565SS/883B	S	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
S = 24-lead small outline DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

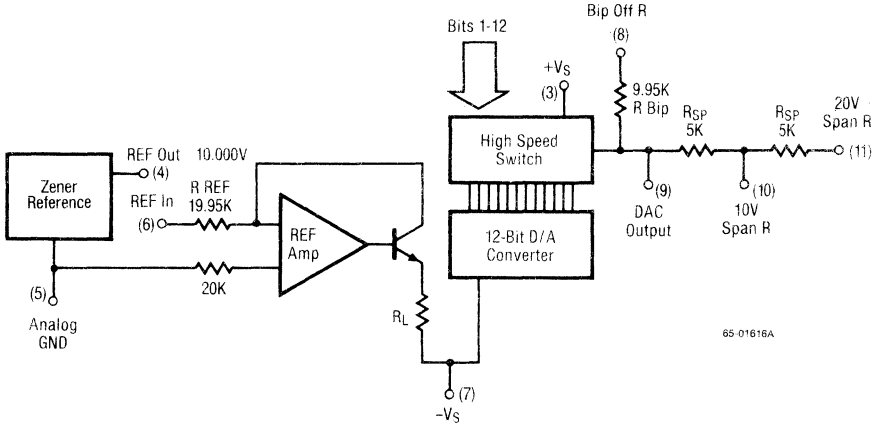
Absolute Maximum Ratings

Supply Voltages ..... ±18V
Logic Inputs ..... -1V to +18V
Analog Common to Digital Common ..... ±1V
Voltage on DAC Output (Pin 9) ..... -3V to +18V
Reference Input to Analog Common ..... ±12V
Bipolar Offset to Analog Common ..... ±12V
10V Span R to Analog Common ..... ±12V
20V Span R to Analog Common ..... ±24V
Ref Out ..... Indefinite Short to Either Common, Momentary Short to $+V_S$
Lead Soldering Temperature (60 Sec) ..... +300°C

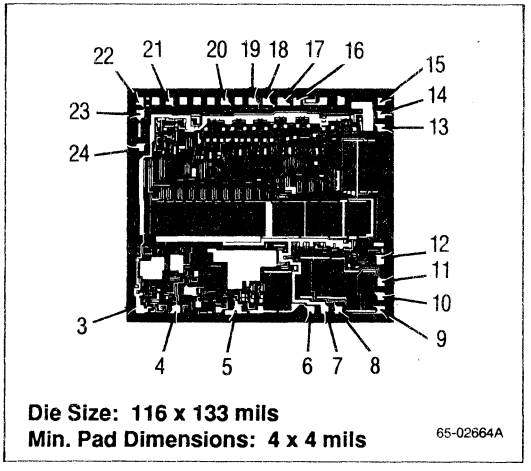
Thermal Characteristics

	24-Lead Sidebrazed DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	1042 mW
Therm. Res θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A >50°C Derate at	8.38 mW/°C

Functional Block Diagram



Mask Pattern



Electrical Characteristics (T_A = +25°C, $+V_S$ = +15V, $-V_S$ = -15V, unless otherwise noted)

Parameters	Test Conditions	DAC-8565S/J			DAC-8565D			Units
		Min	Typ	Max	Min	Typ	Max	
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Nonlinearity			±.006	±.012		±.006	±.012	%FS
Differential Nonlinearity	Deviation From Ideal Step Size		±.007	±.018		±.007	±.018	%FS
Full Scale Current	Unipolar (all bits on) Internal Reference (full temperature)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
	Bipolar (Figure 2 R_2 = 50Ω fixed) All Bits On or Off (full temperature)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	
Output Resistance		1.0	10		1.0	10		MΩ
Output Voltage Compliance	R_O > 1.0MΩ (full temperature)	-1.5		+10	-1.5		+10	V
Output Capacitance			25			25		pF
Offset Unipolar Zero Scale			0.001	0.005		0.002	0.01	%FS
Bipolar	(Figure 2 R_2 = 50Ω Fixed)		0.05	0.15		0.10	0.30	
Settling Time to 1/2 LSB (guaranteed by design)	All Bits On to Off or Off to On		300	400		300	400	nS
Full Scale Transition Rise Time	10% to 90% Plus Propagation Delay		30			30		nS
Fall Time	90% to 10% Plus Propagation Delay		30			30		
Logic Input Levels Logic "0"	(Full temperature)			0.8			0.8	V
Logic "1"	(Full temperature)	2.0			2.0			
Logic Input Current	V_{IN} = 0V to 18V (Full temperature)			80			80	μA
Reference Input Current	V_{REF} = 10.000V	0.4	0.5	0.6	0.4	0.5	0.6	mA
Input Resistance		15	20	25	15	20	25	kΩ
Supply Range	(Full temperature)	±13.5	±15	±16.5	±13.5	±15	±16.5	V
Supply Current	$+V_S$ = +13.5 to +16.5		3.0	5.0		3.0	5.0	mA
	$-V_S$ = -13.5 to -16.5		-10	-18		-10	-18	
Power Consumption			195	345		195	345	mW

Electrical Characteristics (Continued)

Parameters	Test Conditions	DAC-8565S/J			DAC-8565D			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Sensitivity	$+V_S$ = +15V, ±10%		.0003	.001		.0007	.002	%FS
	$-V_S$ = -15V, ±10%		.0015	.0025		.002	.0035	
Reference Output Voltage	External Current = 1mA	9.9	10	10.1	9.7	10	10.3	V
Reference Output Current	(Available for External Loads)	1.0	2.0		1.0	2.0		mA
External Adjustment Gain Error With Fixed 50Ω Resistor for R2	Figure 1		±0.1	±0.25		±0.1	±0.50	%FS
Bipolar Zero Error With Fixed 50Ω Resistor for R1	Figure 2		±0.05	±0.15		±0.05	±0.3	%FS
Gain Adjustment Range	Figure 1	±0.25			±0.50			%FS
Bipolar Zero Adjustment Range	Figure 2	±0.15			±0.3			%FS
Programmable Output Range	(See Figs. 1, 2, 3 & 4)	0		5.0	0		5.0	V
		-2.5		+2.5	-2.5		+2.5	
		0		10	0		10	
		-5.0		+5.0	-5.0		+5.0	
		-10		+10	-10		+10	
Wideband Reference Noise	0.1 to 1MHz		1.0			1.0		mV
DAC-8565S = -55°C to +125°C, DAC-8465J/D = 0°C to +70°C (unless otherwise noted)								
Resolution		12	12	12	12	12	12	Bits
Monotonicity		12	12	12	12	12	12	Bits
Nonlinearity			±.012	±.018		±.012	±.018	%FS
Differential Nonlinearity	Deviation From Ideal Step Size	Monotonicity Guaranteed						
Temperature Coefficients Unipolar Zero			1.0	2.0		1.0		
Bipolar Zero			5.0	10		10		
Differential Nonlinearity			2.0			2.0		ppm/°C
Gain With Internal Reference	Full Scale		15	30		30		
Gain With External Reference			5.0			5.0		
Supply Current	$+V_S$ = +13.5 to +16.5V		4.0	7.0		4.0	7.0	mA
	$-V_S$ = -13.5 to -16.5V		-12	-18		-12	-18	

Connecting the DAC-8565 for Buffered Voltage Output

The standard current to voltage conversion connections using an operational amplifier are shown in Figure 1. If a low offset voltage operational amplifier (OP-07, OP-27, OP-37) is used, excellent performance can be obtained in most applications without trimming. If a fixed 50Ω resistor is substituted for the 100Ω trimmer of Figure 1, unipolar zero will be typically much less than ±1/2 LSB and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer (R1) of Figure 2 will give a bipolar zero error typically within ±2.0 LSB.

The configuration of Figure 1 will provide a unipolar 0V to +10V output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

Unipolar Configurations

Step 1 — Gain Adjust
Turn all bits on and adjust 100Ω gain trimmer R1 until the output is +9.9976 (full scale should be adjusted to 1 LSB less than +10.000V). If a +10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

In most cases a zero trim is not needed, due to the extremely low zero scale output current. Pin 8 should be connected to pin 9 for unipolar operation.

Bipolar Configurations

These configurations will yield ±5.0V, ±10V, or ±2.5V, with positive full scale occurring with all bits on (all 1's).

Step 1 — Offset Adjust
Turn off all bits. Adjust 100Ω trimmer R1 to give -5.000, -10.000, or -2.500V, depending upon the full scale range selected.

Step 2 — Gain Adjust
Turn on all bits and adjust trimmer R2 to give a reading of +4.9976, +9.9951, or +2.4988V depending upon the range.

If a precision op amp such as the OP-07, OP-27, or OP-37 is used no separate trimming of the operational amplifier is required or recommended.

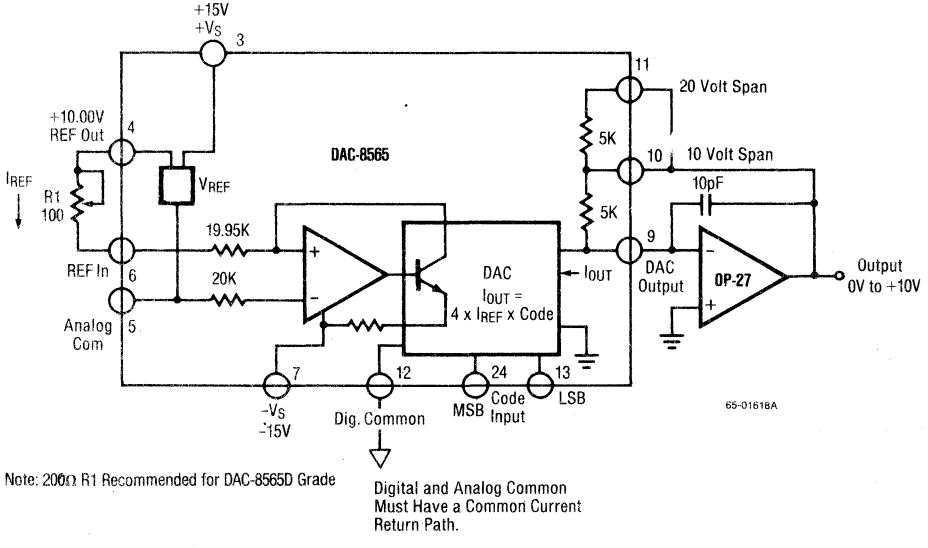
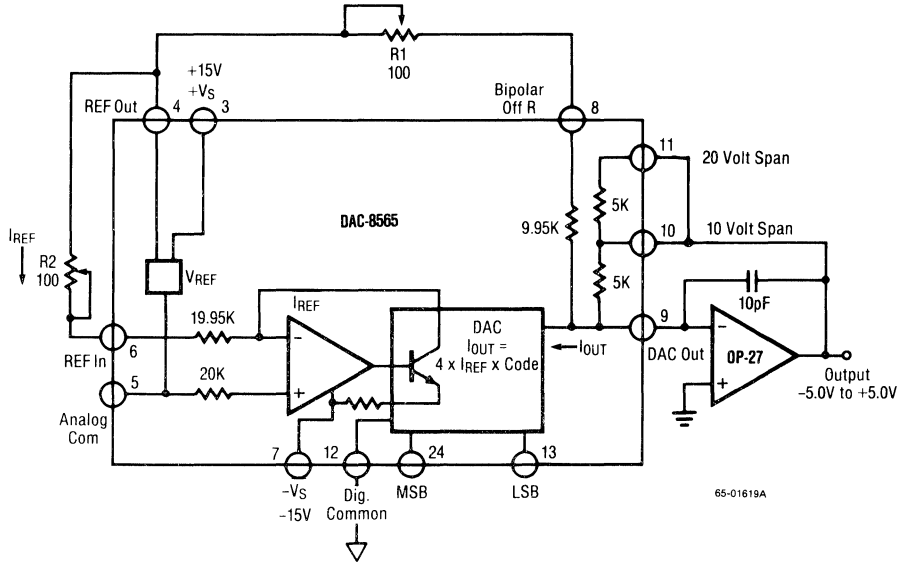


Figure 1. 0V to +10V Unipolar Voltage Output



Note: 200Ω R1 and R2 Pots are Recommended for DAC-8565D Grade

Figure 2. ±5.0V Bipolar Voltage Output

0V to +5.0V Range

A 0V to +5V output can be achieved by modifying the configuration of Figure 1. Tie pin 11 to pin 9 rather than to pin 10 and adjust full scale to +4.9988V.

Internal/External Reference Use

The DAC-8565 has an internal bandgap voltage reference which is trimmed for both temperature coefficient and absolute accuracy. The reference is buffered with an internal operational amplifier and is capable of driving a minimum of 5.0mA in addition to the 0.5mA into REF_{IN} and 1.0mA into Bipolar Offset for the DAC. The reference is typically trimmed to ±0.2% but specified to 1.0% (J, S grades) max error. Testing and specifying of absolute unipolar and bipolar full scale is done using the internal reference. For noise performance of the reference see Figure 6.

Digital Input Considerations

The DAC-8565 uses a positive true straight binary code for unipolar outputs (all 1's give full scale output) and an offset binary code for bipolar output ranges. In the bipolar mode, all 0's give -F.S., with only the MSB on give 0.00V, and with all 1's, +F.S. is achieved.

The threshold of the digital input circuitry is set at +1.4V independent of supply voltage. The bit lines are compatible with TTL, DTL, CMOS, and unbuffered CMOS.

Application of Analog and Digital Commons

The DAC-8565 separates analog and digital grounds to optimize accuracy and noise. 200mV difference between the two grounds can be tolerated without degradation in performance.

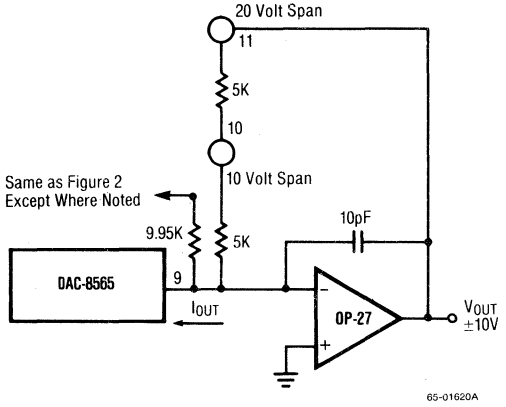


Figure 3. ±10V Bipolar Voltage Output

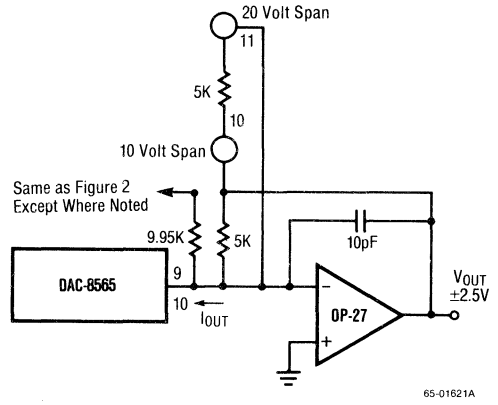


Figure 4. ±2.5V Bipolar Voltage Output

Output Voltage Compliance

The DAC-8565 has a minimum output voltage compliance range of -1.5V to +10V and is independent of both the positive and negative supply voltages. The output can be modeled as a 25pF capacitance shunted by a 10MΩ resistance across the output current source to ground. This is a dramatic improvement over competitive DAC-8565 designs which have an 8kΩ output impedance. The DAC-8565's output current varies insignificantly as a function of output voltage, allowing direct conversion to voltage by an external resistor in many applications.

More significantly, the errors introduced by the input errors of the external output operational amplifier are not magnified by a low output impedance. The output system error from the op amp is equal to:

$$(V_{ERR} \text{ in op amp}) \left(\frac{R_{SPAN} + R_{IN}}{R_{IN}} \right)$$

and defaults to only the inherent input errors of the op amp.

Settling Time

The internally compensated reference amplifier and differential bit switch are optimized for fast settling operation. Worst case settling time occurs when all bits are switched and is specified as 400nS maximum. Note: The settling time specification is for the output current, not for a voltage. When using an external op amp as a current to voltage converter, the settling time will usually be dominated by the speed performance of the operational amplifier. When using the DAC in a successive approximation A/D application, care in the selection of the comparator is critical in determining accuracy and speed. Raytheon recommends the use of the RM4805 comparator to optimize A/D performance. Please refer to the 4805 application notes for further details on speed and accuracy characteristics of successive approximation A/D converters.

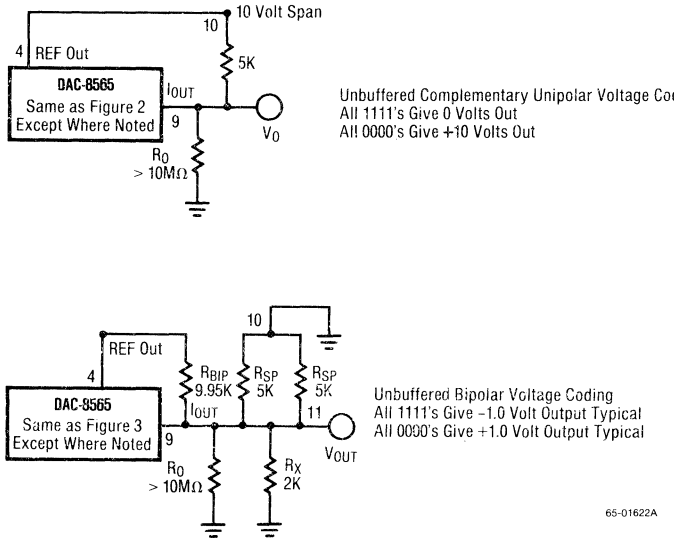
Direct Unbuffered Voltage Output for Cable Driving

The high output impedance and compliance range allow for direct current to voltage conversion using the bipolar and span resistors. The

circuit configurations of Figure 5 yield complementary unipolar coding (+10V to 0V) as well as ±1.0V bipolar coding. The 10MΩ output impedance of the DAC-8565 allows for direct current to voltage conversion without any degradation of linearity performance.

12-Bit Analog-to-Digital Converter

Figure 7 shows an application of the DAC-8565 coupled with the 4805 comparator to make a successive approximation 12-bit analog-to-digital converter. The SAR selected is the AM2504. Latched output capability is provided by the 25LS374. Conversion time with the 1K summing mode resistance should be set by the clock at 13μS.



Note: R_{SPANS} can vary by ±20% max

Figure 5. Unbuffered Voltage Output Configurations

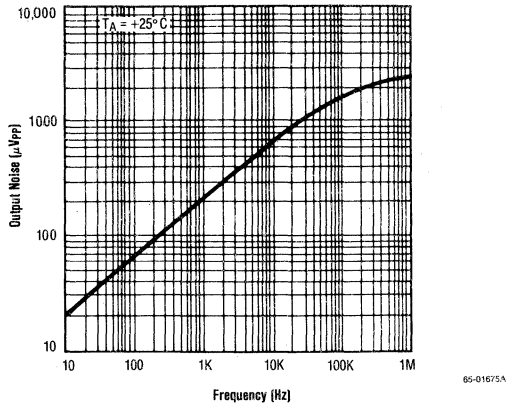


Figure 6. Output Wideband Noise vs Bandwidth (0.1Hz to Frequency Indicated)

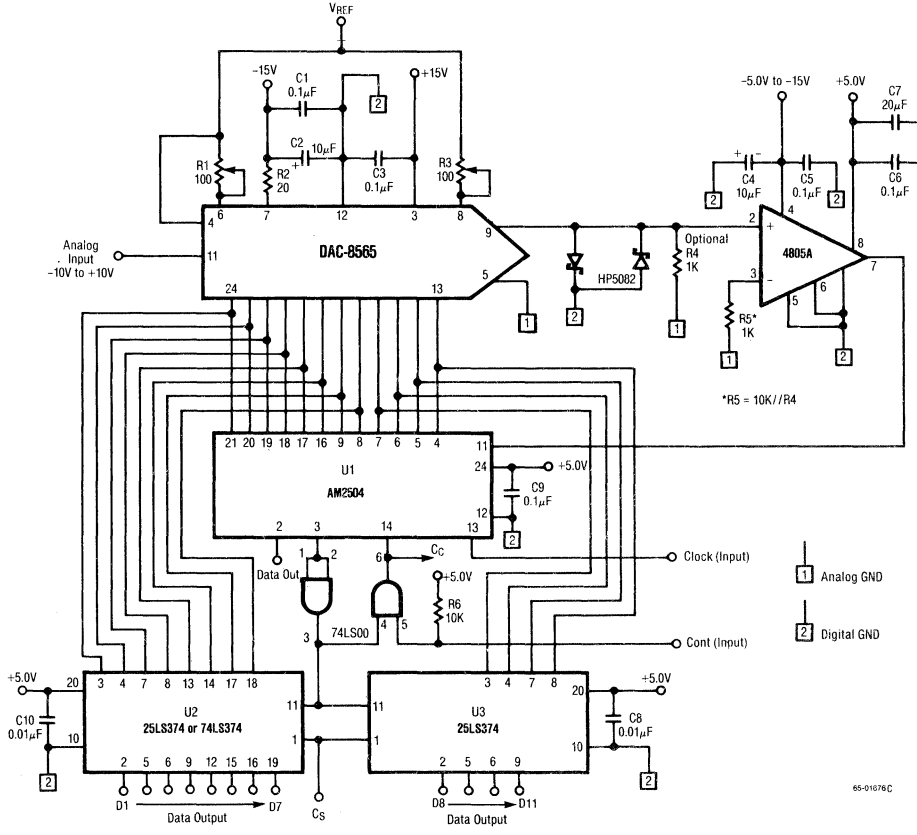


Figure 7. 12-Bit Analog-to-Digital Converter

SECTION 7
V/F CONVERTERS

DEFINITIONS

Compliance
The measure of the output impedance of a switched current source, given as a maximum current for a specified voltage change, in microamps (μA).

Full Scale Frequency
A voltage-to-frequency converter can operate up to the guaranteed full scale frequency without violating any of the performance specs for this frequency range. Full scale frequency is expressed in Hertz (Hz).

Nonlinearity Error
On a plot of input voltage versus output frequency, a straight line is drawn from the origin to the full scale point which is defined by the intersection of the maximum input voltage and maximum output frequency.

The actual plot of output frequency versus input voltage should not deviate from this straight line by more than increment $\Delta F_{O(MAX)}$. Nonlinearity is defined here as $(\Delta F_O/\Delta F_S) \times 100\%$ where F_S is the maximum frequency for the range in question. For instance, when specifying nonlinearity error for the 0.1Hz to 10kHz range, then F_S = 10kHz. When specifying nonlinearity error for a frequency-to-voltage converter, nonlinearity error is defined as $(\Delta V/V_{FS}) \times 100\%$.

Leakage Current
The current that flows into the open collector output transistor when the logic output transistor is in the "off" state, as a result of the application of the maximum supply voltage to the output. Leakage current is measured in microamps (μA).

Reference Current (4153)
The current flowing into pin 5 as a result of applying a reference voltage of exactly 7.3V, measured in milliamps (mA).

Reference Voltage (V_{REF})
The voltage output of the internal reference as measured from pin 3 to the common terminal (pin 2) of the 4153 — cannot be directly measured for the 4151 and 4152. V_{REF} is expressed in volts (V).

Scale Factor
Scale factor K is the ratio of F_O/V_{IN}.

Scale Factor Tolerance (4153)
Scale factor tolerance is defined for V_{REF}, R_{IN}, and C_O equal to 7.3V, 20,000Ω and 3500pF, respectively. The scale factor tolerance is the amount a measured value of K deviates from the computed value.

RC4151, 4152 Voltage-to-Frequency Converters

Features

- Single supply operation
- Pulse output DTL/TTL/CMOS compatible
- Programmable scale factor (K)
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- V-F or F-V conversion
- Voltage or current input
- Wide dynamic range

Applications

- Precision voltage-to-frequency converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converters
- Long-term analog integrators
- Signal conversion —
  Current-to-Frequency
  Temperature-to-Frequency
  Pressure-to-Frequency
  Capacitance-to-Frequency
  Frequency-to-Current
- Signal isolation —
  VFC — opto-isolation — FVC
  ADC with opto-isolation
- Signal Encoding —
  FSK modulation/demodulation
  Pulse-width modulation
- Frequency scaling
- DC motor speed control

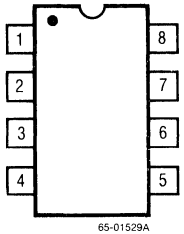
Description

The 4151 and 4152 are monolithic circuits containing all of the active components needed to build a complete voltage-to-frequency converter. Circuits that convert a DC voltage to a pulse train (VFC) can be built by adding a few resistors and capacitors to the internal comparator, one-shot, voltage reference, and switched current source. Frequency-to-voltage converters (FVCs) and many other signal conditioning circuits are also easily created using these converters.

Raytheon was the first company to introduce a monolithic VFC. The low cost 4151 was followed by the 4152, a pin compatible replacement offering guaranteed temperature and accuracy specifications. Both converters are available in a standard 8-pin plastic DIP.

Connection Information

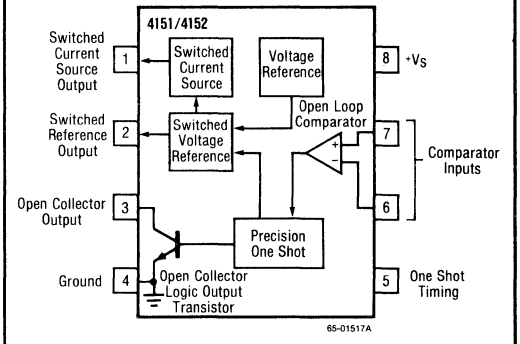
8-Lead Plastic DIP



65-01529A

Pin	Function
1	Switched Current Source Output (I_O)
2	Switched Voltage Reference (R_S)
3	Logic Output (Open Collector) (F_O)
4	Ground (GND)
5	One-Shot R, C Timing (C_O)
6	Threshold (V_{TH})
7	Input Voltage (V_{IN})
8	$+V_S$

Functional Block Diagram



65-01517A

Absolute Maximum Ratings

Supply Voltage ..... +22V
Internal Power Dissipation ..... 500 mW
Input Voltage ..... -0.2V to $+V_S$
Output Sink Current
(Frequency Output) ..... 20 mA
Output Short Circuit to Ground ..... Continuous
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range ..... 0°C to +70°C

Ordering Information

Part Number	Package	Operating Temperature Range
RC4151N	N	0°C to +70°C
RC4152N	N	0°C to +70°C

Notes:
N = 8- lead plastic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Thermal Characteristics

	8-Lead Plastic DIP
Max. Junction Temp.	125°C
Max. P_D T_A <50°C	468 mW
Therm. Res θ_{JC}	—
Therm. Res. θ_{JA}	160°C/W
For T_A >50°C Derate at	6.25 mW/°C

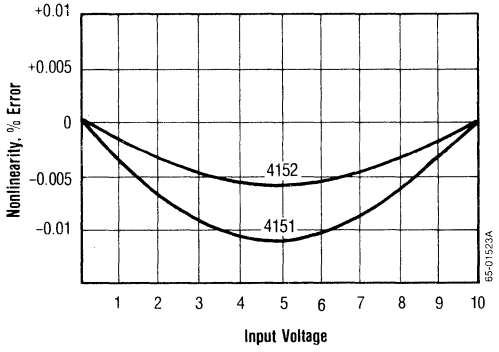
Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	4151			4152			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Requirements (Pin 8)								
Supply Current	V_S = +15V		4.5	7.5		2.5	6.0	mA
Supply Voltage		+8.0	+15	+22	+7.0	+15	+18	V
Input Comparator (Pins 6 and 7)								
V_{OS}			±2.0	±10		±2.0	±10	mV
Input Bias Current			-100	-300		-50	-300	nA
Input Offset Current			±50	±100		±30	±100	nA
Input Voltage Range		0	V_S-2	V_S-3	0	V_S-2	V_S-3	V
One Shot (Pin 5)								
Threshold Voltage		0.63	0.67	0.70	0.65	0.67	0.69	XV_S
Input Bias Current			-100	-500		-50	-500	nA
Saturation Voltage	I = 2.2mA		0.15	0.5		0.1	0.5	V
Drift of Timing vs. Temperature[2]	T = 75μS 0°C to +70°C		±35			±30	±50	ppm/°C
Drift of Timing vs. Supply			±150			±100		ppm/V
Switched Current Source[1] (Pin 1) Output Current	4151-R_S = 14.0K/ 4152-R_S = 16.7K		+138			+138		μA
Drift vs. Temperature[2]	0°C to +70°C		±75			±50	±100	ppm/°C
Drift vs. Supply Voltage			0.15			0.10		%/V
Leakage Current	Off State		1.0	50		1.0	50	nA
Compliance	Pin 1 = 0V to +10V	1.0	2.5		1.0	2.5		μA
Reference Voltage (Pin 2)								
V_{REF}		1.7	1.9	2.08	2.0	2.25	2.5	V
Drift vs. Temperature[2]	0°C to +70°C		±50			±50	±100	ppm/°C
Logic Output (Pin 3)								
Saturation Voltage	I_{SINK} = 3.0mA		0.1	0.5		0.1	0.5	V
Saturation Voltage	I_{SINK} = 10mA		0.8			0.8		V
Leakage Current	Off State		0.2	1.0		0.1	1.0	μA
Nonlinearity % Error Voltage Sourced Circuit of Figure 3	1.0Hz to 10kHz		0.013			0.007	0.05	%
Temperature Drift Voltage[2] Sourced Circuit of Figure 3	0°C to +70°C F_0 = 10kHz		±100			±75	±150	ppm/°C

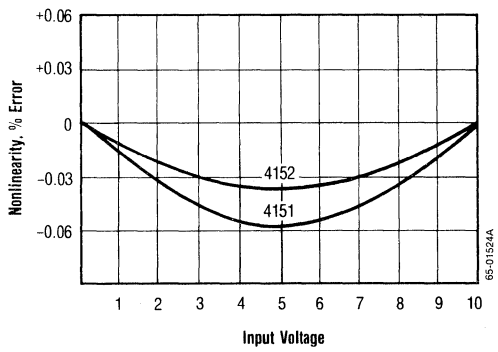
Notes:
1. Temperature coefficient of output current source (pin 1 output) exclusive of reference voltage drift.
2. Guaranteed but not tested.

Typical Performance Characteristics

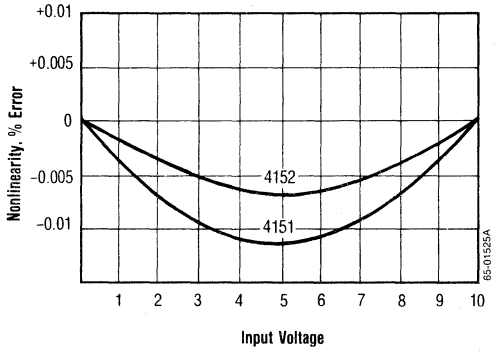
10kHz Current-Sourced VFC Nonlinearity



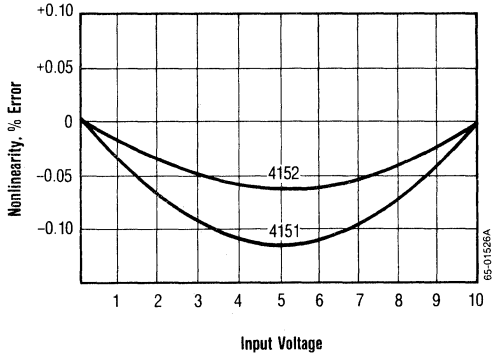
100kHz Current-Sourced VFC Nonlinearity



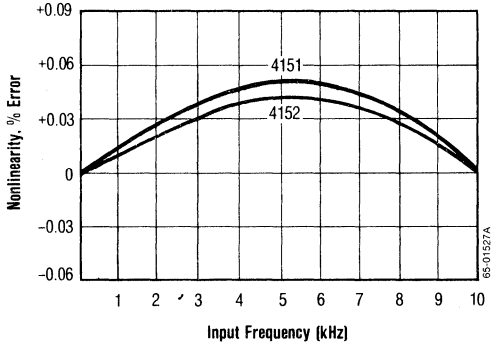
10kHz Voltage-Sourced VFC Nonlinearity



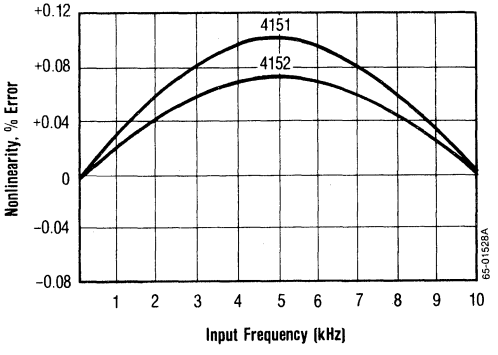
100kHz Voltage-Sourced VFC Nonlinearity



10kHz Precision FVC Nonlinearity



100kHz Precision FVC Nonlinearity



Principles of Operation

The 4151 and the 4152 contain the following components: an open loop comparator, a precision one-shot timer, a switched voltage reference, a switched current source, and an open collector logic output transistor. These functional blocks are internally interconnected in a special way. By adding some external resistors and capacitors, a designer can create a complete voltage-to-frequency converter.

The comparator's output controls the one-shot (monostable timer). The one-shot in turn controls the switched current source, the switched reference, and the open collector output transistor. The block diagram shows the components and their interconnection.

To detail, if the voltage at pin 7 is greater than the voltage at pin 6, the comparator switches and triggers the one-shot. When the one-shot is triggered, two things happen. First, the one-shot begins its timing period. Second, the one-shot's output turns on the switched current source, the switched voltage reference, and the open collector output transistor.

The one-shot creates its timing period much like the popular 555 timer does, by charging a capacitor from a resistor tied to $+V_S$. The one-shot senses the voltage on the capacitor (pin 5) and ends the timing period when the voltage reaches 2/3 of the supply voltage. At the end of the timing period the capacitor is discharged by a transistor similar to the open collector output transistor.

Meanwhile, during the timing period of the one-shot, the switched current source, the switched reference, and the open collector output transistor all will be switched on. The switched current source (pin 1) will deliver a current proportional to both the reference voltage and an external resistor, R_S. The switched reference (pin 2) will supply an output voltage equal to the internal reference voltage (4151 = 1.9V, 4152 = 2.25V). The open collector output transistor will be turned on, forcing the logic output (pin 3) to a low state. At the end of the timing period all of these outputs will turn off. The switched voltage reference has produced an off-on-off voltage pulse, the switched current source has emitted a quanta of charge, and the open collector output has transmitted a logic pulse.

To summarize, the purpose of the circuit is to produce a current pulse, well-defined in amplitude and duration, and to simultaneously produce an output pulse which is compatible with most logic families. The circuit's outputs show a pulse waveform in response to a voltage difference between the comparator's inputs.

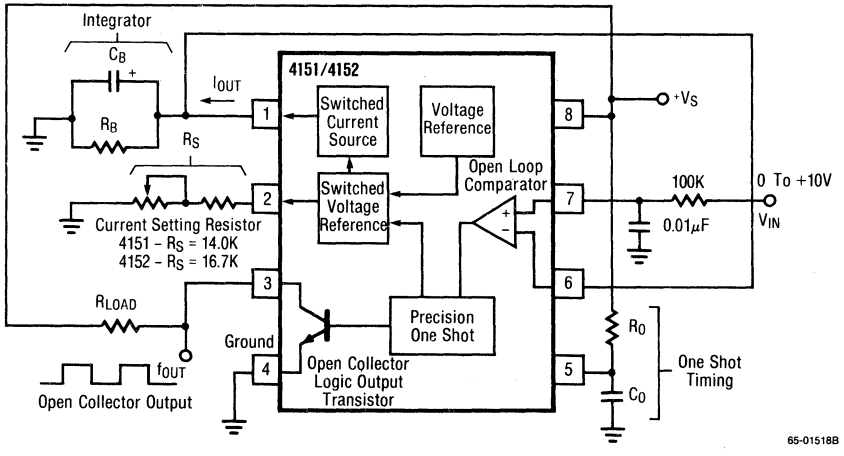


Figure 1. Single Supply VFC

Applications

Single Supply VFC

The stand-alone voltage-to-frequency converter is one of the simplest applications for the 4151 or 4152. This application uses only passive external components to create the least expensive VFC circuit.

The positive input voltage V_{IN} is applied to the input comparator through a low pass filter. The one-shot will fire repetitively and the switched current source will pump out current pulses of amplitude V_{REF}/R_S and duration 1.1 R_OC_O into the integrator. Because the integrator is tied back to the inverting comparator input, a feedback loop is created. The pulse repetition rate will increase until the average voltage on the integrator is equal to the DC input voltage at pin 7. The average voltage at pin 6 is proportional to the output frequency because the amount of charge in each current pulse is precisely controlled.

Because the one-shot firing frequency is the same as the open collector output frequency, the output frequency is directly proportional to V_{IN}.

The external passive components set the scale factor. For best linearity, R_S should be limited to a range of 12kΩ to 20kΩ.

The reference voltage is nominally 1.9V for the 4151 and 2.25V for the 4152. Recommended values for different operating frequencies are shown in the table below.

Operating Range	R_O	C_O	R_B	C_B
DC to 1.0kHz	6.8kΩ	0.1μF	100kΩ	10μF
DC to 10kHz	6.8kΩ	0.01μF	100kΩ	1.0μF
DC to 100kHz	6.8kΩ	0.001μF	100kΩ	0.1μF

The single supply VFC is recommended for uses where the dynamic range of the input is limited, and the input does not reach 0V. With 10kHz values, nonlinearity will be less than 1.0% for a 10mV to 10V input range, and response tme will be about 135mS.

Precision Current-Sourced VFC

This circuit operates similarly to the single supply VFC, except that the passive R-C integrator has been replaced by an active op amp integrator. This increases the dynamic range down to 0V, improves the response time, and eliminates the nonlinearity error introduced by the limited compliance of the switched current source output.

The integrator algebraically sums the positive current pulses from the switched current source with the current V_{IN}/R_B. To operate correctly, the input voltage must be negative, so that when the circuit is balanced, the two currents cancel.

$$T = \frac{1}{F_{OUT}}$$

$$\frac{|V_{IN}|}{R_B} = I_{OUT}\left[\frac{T_P}{T}\right] \text{ where } T_P = 1.1\ R_OC_O$$

$$I_{OUT} = \frac{V_{REF}}{R_S}$$

By rearranging and substituting,

$$F_{OUT} = \left[\frac{R_S}{1.1\ R_OC_OR_B}\right]\left[\frac{V_{IN}}{V_{REF}}\right]$$

Recommended component values for different operating frequencies are shown in the table below.

Range		Scale Factor	R_O	C_O	C_I	R_B
Input V_{IN}	Output F_O					
0 to -10V	0 to 1.0kHz	0.1kHz/V	6.8kΩ	0.1μF	0.05μF	100kΩ
0 to -10V	0 to 10kHz	1.0kHz/V	6.8kΩ	0.01μF	0.005μF	100kΩ
0 to -10V	0 to 100kHz	10kHz/V	6.8kΩ	1000pF	500pF	100kΩ

The graphs shown under Typical Performance Characteristics show nonlinearity versus input voltage for the precision current-sourced VFC. The 4152s improved circuitry reduces nonlinearity error when compared to the 4151. The best linearity is achieved by using an op amp having greater than 1.0V/μS slew rate, but any op amp can be used.

Precision Voltage-Sourced VFC

This circuit is identical to the current-sourced VFC, except that the current pulses into the integrator are derived directly from the switched voltage reference. This improves temperature drift at the expense of high frequency linearity.

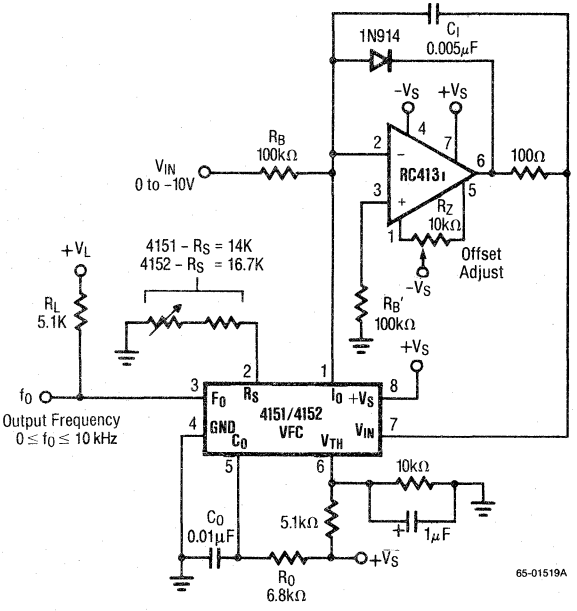


Figure 2. Precision Current — Sourced VFC

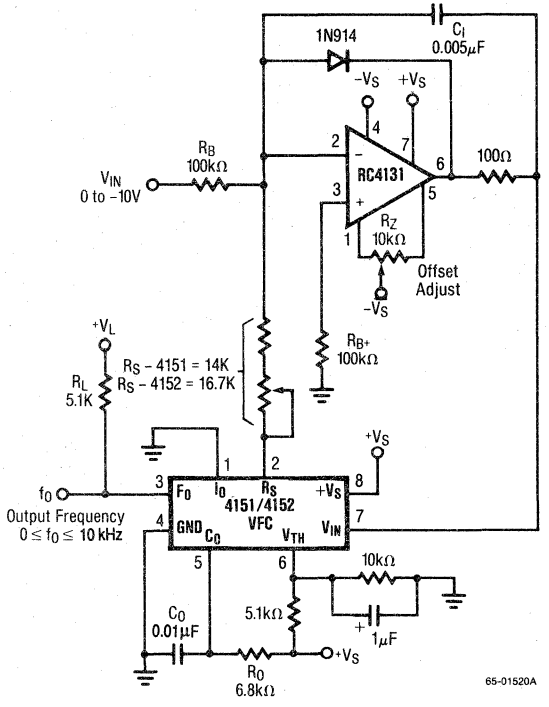


Figure 3. Precision Voltage — Sourced VFC

The switched current source (pin 1) output has been tied to ground, and R_S has been put in series between the switched voltage reference (pin 2) and the summing node of the op amp. This eliminates temperature drift associated with the switched current source. The graphs under the Typical Performance Characteristics show that the nonlinearity error is worse at high frequency, when compared with the current-sourced circuit.

Single Supply FVC

A frequency-to-voltage converter performs the exact opposite of the VFCs function; it converts an input pulse train into an average output voltage. Incoming pulses trigger the input comparator and fire the one-shot. The one-shot then dumps a charge into the output integrator. The voltage on the integrator becomes a varying DC voltage proportional to the frequency of the input signal. Figure 4 shows a complete single supply FVC.

The input waveform must have fast slewing edges, and the differentiated input signal must be less than the timing period of the one-shot, $1.1\ R_OC_O$. A differentiator and divider are used to shape and bias the trigger input; a negative going pulse at pin 6 will cause the comparator to fire the one-shot. The input pulse amplitude must be large enough to trip the comparator, but not so large as to exceed the ICs input voltage ratings.

The output voltage is directly proportional to the input frequency:

$$V_O = \left[\frac{1.1\ R_OC_O\ R_B\ V_{REF}}{R_S}\right] f_{IN}\ (Hz)$$

Output ripple can be minimized by increasing C_B, but this will limit the response time. Recommended values for various operating ranges are shown in the table below.

Input Operating Range	C_{IN}	R_O	C_O	R_B	C_B	Ripple
0 to 1.0kHz	0.02μF	6.8kΩ	0.1μF	100kΩ	100μF	1.0mV
0 to 10kHz	0.002μF	6.8kΩ	0.01μF	100kΩ	10μF	1.0mV
0 to 100kHz	200pF	6.8kΩ	0.001μF	100kΩ	1.0μF	1.0mV

Precision FVC

Linearity. offset, and response time can be improved by adding one or more op amps to form an active lowpass filter at the output. A circuit using a single pole active integrator is shown in Figure 5.

The positive output current pulses are averaged by the inverting integrator, causing the output voltage to be negative. Response time can be further improved by adding a double pole filter to replace the single pole filter. Refer to the graphs under Typical Performance Characteristics that show nonlinearity error versus input frequency for the precision FVC circuit.

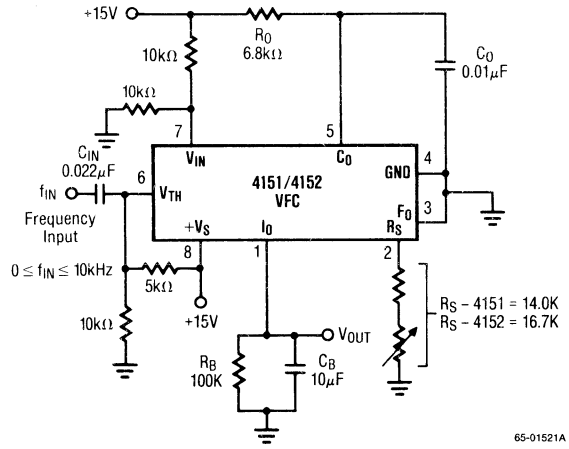


Figure 4. Single Supply FVC

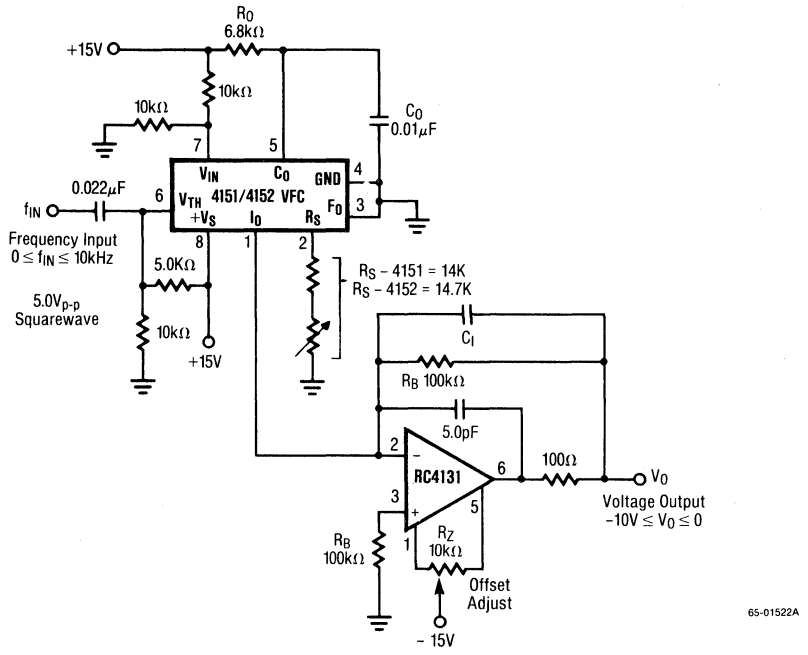
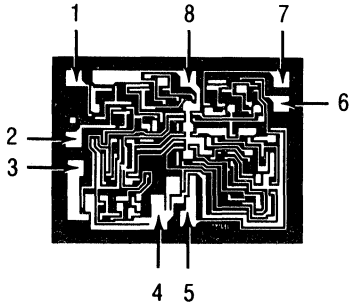


Figure 5. Precision FVC

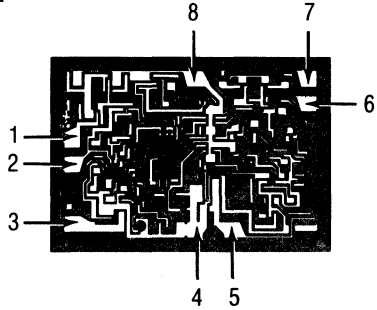
Mask Pattern

4151



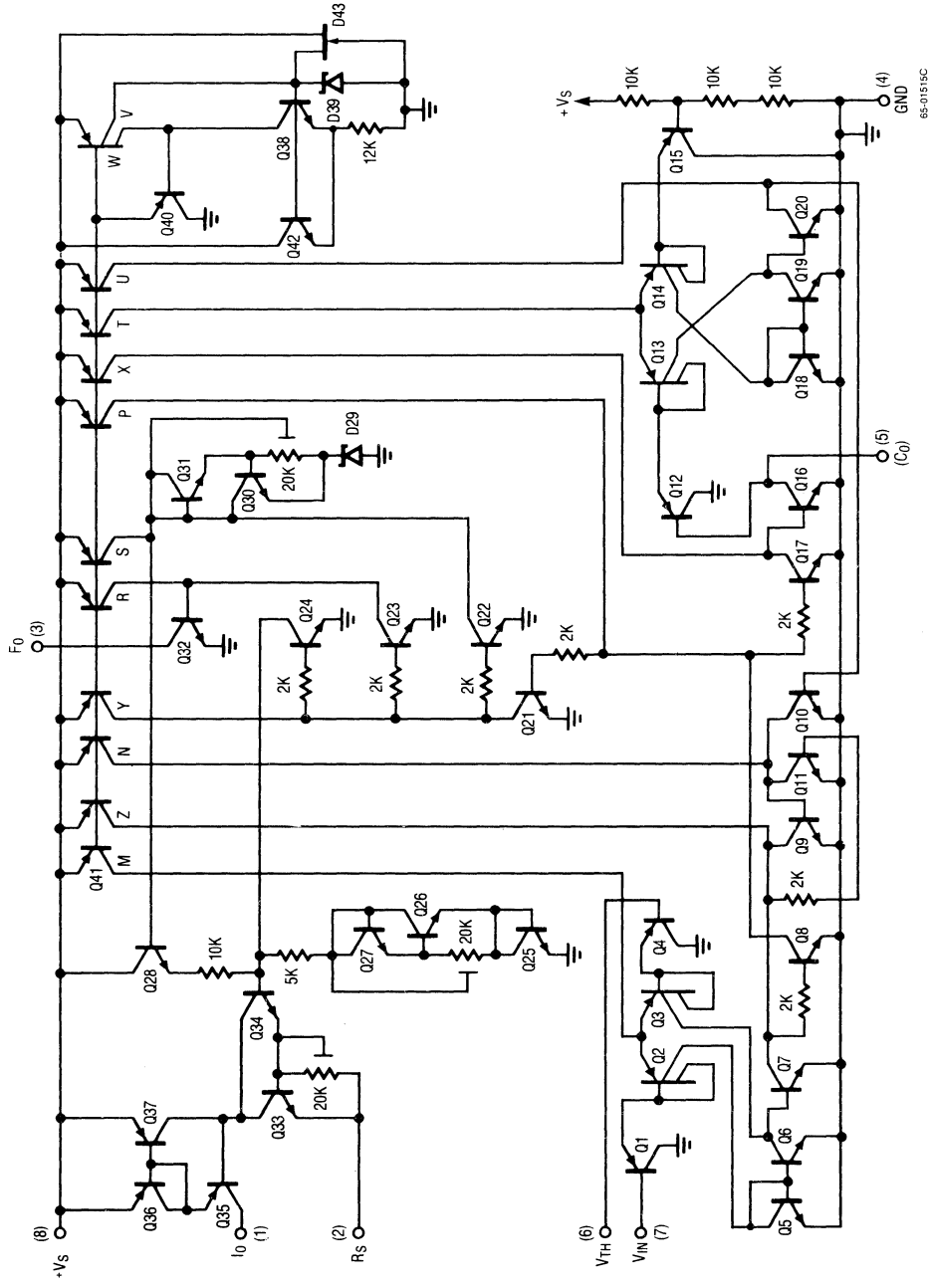
Die Size: 45 x 61 mils
Min. Pad Dimension: 4 x 4 mils

4152

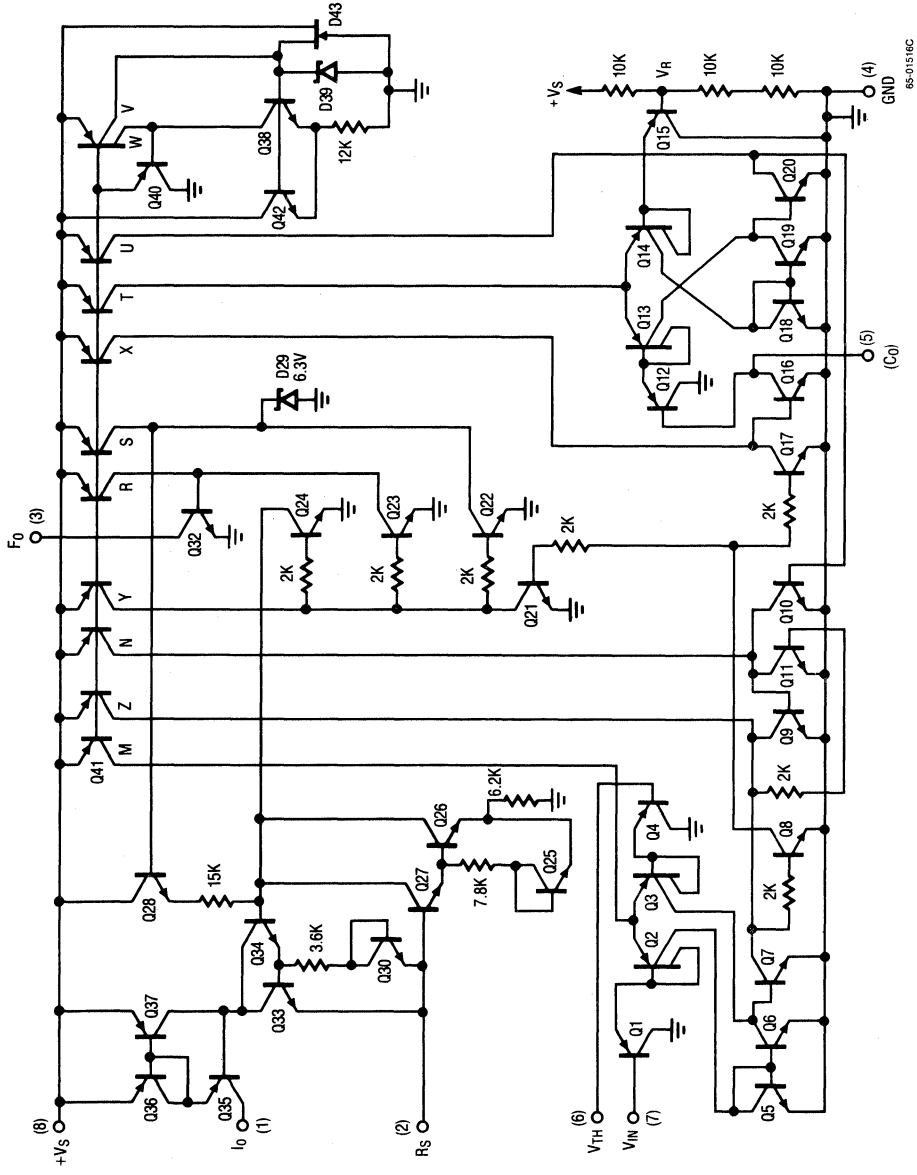


Die Size: 47 x 68 mils
Min. Pad Dimension: 4 x 4 mils

Schematic Diagram — 4151



Schematic Diagram — 4152



RC4153 Voltage-to-Frequency Converter

Features

- 0.1Hz to 250kHz dynamic range
- 0.01% F.S. maximum nonlinearity error — 0.1Hz to 10kHz
- 50ppm/°C maximum gain temperature coefficient (external reference)
- Few external components required

Applications

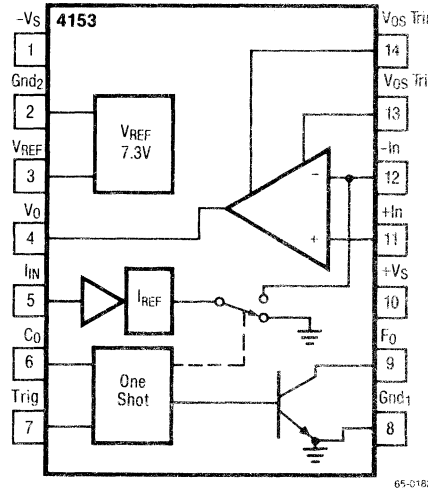
- Precision voltage-to-frequency converters
- Serial transmission of analog information
- Pulse width modulators
- Frequency-to-voltage converters
- A/D converters and long term integrators
- Signal isolation
- FSK modulation/demodulation
- Frequency scaling
- Motor speed controls
- Phase lock loop stabilization

Description

The 4153 sets a new standard for ease of application and high frequency performance in monolithic voltage-to-frequency converters. This voltage-to-frequency requires only four passive external components for precision operation, making it ideal for many low cost applications such as A/D conversion, frequency-to-voltage conversion, and serial data transmission. The improved linearity at high frequency makes it comparable to many dual slope A/D converters both in conversion time and accuracy, while retaining the benefits of voltage-to-frequency conversion, i.e., serial output, cost and size. The speed, accuracy, and temperature performance of the 4153 is achieved by incorporating high speed ECL logic, a high gain, wide bandwidth op amp, and a buried zener reference on a single monolithic chip.

4153 Functional Block Diagram

14 Lead
Dual In-Line Package
(Top View)



Pin	Function	Pin	Function
1	$-V_S$	8	Circuit Gnd
2	REF Gnd	9	Frequency Output (Open Collector)
3	V_{REF} Output	10	$+V_S$
4	V_{OUT} (Op Amp)	11	(+) Op Amp Input
5	I_{IN} (REF Input)	12	(-) Op Amp Input
6	C_O (Pulse Width)	13	V_{OS} Trim
7	Trigger Input	14	V_{OS} Trim

Ordering Information

Part Number	Package	Operating Temperature Range
RC4153D	D	0°C to +70°C
RM4153D	D	-55°C to +125°C

Notes:
D = 14- lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

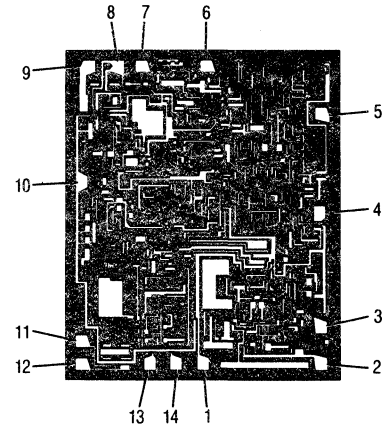
Absolute Maximum Ratings

Supply Voltage ..... ±18V
Internal Power Dissipation ..... 500 mW
Input Voltage Range ..... $-V_S$ to $+V_S$
Output Sink Current (Freq. Output) ..... 20 mA
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RM4153 ..... -55°C to +125°C
RC4153 ..... 0°C to +70°C

Thermal Characteristics

	14-Lead Ceramic DIP
Max. Junction Temp.	175°C
Max. P_D T_A <50°C	1042 mW
Therm. Res θ_{JC}	60°C/W
Therm. Res. θ_{JA}	120°C/W
For T_A >50°C Derate at	8.33 mW/°C

Mask Pattern



Die Size: 90 x 108 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Min	Typ	Max	Units
Power Supply Requirements				
Supply Voltage	±12	±15	±18	V
Supply Current (I_O = 0, Pos)		+4.2	+7.5	mA
(I_O = 0, Neg)		-7	-10	
Full Scale Frequency	250	500		kHz
Transfer Characteristics				
Nonlinearity Error Voltage-to-Frequency[1]				
0.1 Hz ≤ F_{OUT} ≤ 10 kHz		0.002	0.01	%FS
0.1 Hz ≤ F_{OUT} ≤ 100 kHz		0.025	0.05	%FS
5.0 Hz ≤ F_{OUT} ≤ 250 kHz		0.06	0.1	%FS
Nonlinearity Error Frequency-to-Voltage[1]				
0.1 Hz ≤ F_{IN} ≤ 10 kHz		0.002	0.01	%FS
0.1 Hz ≤ F_{IN} ≤ 100 kHz		0.05	0.1	%FS
5.0 Hz ≤ F_{IN} ≤ 250 kHz		0.07	0.12	%FS
Scale Factor Tolerance, F = 10 kHz $K = \frac{1}{2V_{REF} R_{IN} C_O}$		±0.5		%
Change of Scale Factor With Supply		0.008		%/V
Reference Voltage (V_{REF})		7.3		V
Temperature Stability [1,2,3]				
Scale Factor 10 kHz Nominal		±75	±150	ppm/°C
Reference Voltage		±50	±100	ppm/°C
Scale Factor (External Ref) 10 kHz FS		±25	±50	ppm/°C
Scale Factor (External Ref) 100 kHz FS		±50	±100	ppm/°C
Scale Factor (External Ref) 250 kHz FS		±100	±150	ppm/°C

Notes:
1. Guaranteed but not tested.
2. V_{REF} Range 6.6V ≤ VR ≤ 8.0V.
3. Over the specified operating temperature range

Electrical Characteristics (Continued)

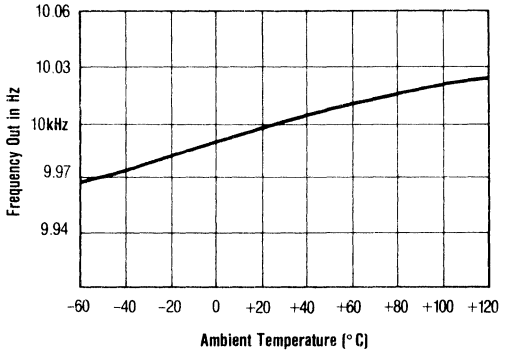
Parameters	Min	Typ	Max	Units
Op Amp				
Open Loop Output Resistance		230		Ω
Short Circuit Current		25		mA
Gain Bandwidth Product[1]	2.5	3.0		MHz
Slew Rate	0.5	2.0		V/μS
Output Voltage Swing ($R_L \geq 2K$)	0 to +10	-0.5 to +14.3		V
Input Bias Current		70	400	nA
Input Offset Voltage (Adjustable to 0)		0.5	5.0	mV
Input Offset Current		30	60	nA
Input Resistance (Differential Mode)		1.0		MΩ
Common Mode Rejection Ratio	75	100		dB
Power Supply Rejection Ratio	70	106		dB
Large Signal Voltage Gain	25	350		V/mV
Switched Current Source				
Reference Current (Ext Ref)		1.0		mA
Digital Input (Frequency-to-Voltage, Pin 7)				
Logic "0"			0.5	V
Logic "1"	2.0			V
Trigger Current		-50		μA
Logic Output (Open Collector)				
Saturation Voltage (Pin 9)				
I_{SINK} = 4 mA		0.15	0.4	V
I_{SINK} = 10 mA		0.4	1.0	V
Leakage Current (Off State)		150		nA

Notes:

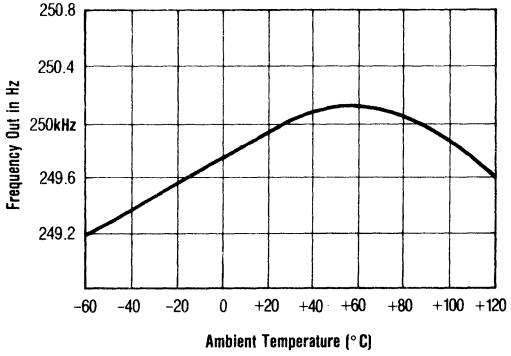
1. Guaranteed but not tested.

Typical Performance Characteristics

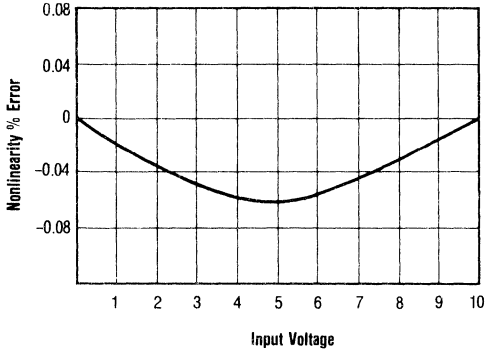
4153 10kHz Full Scale Temperature Drift



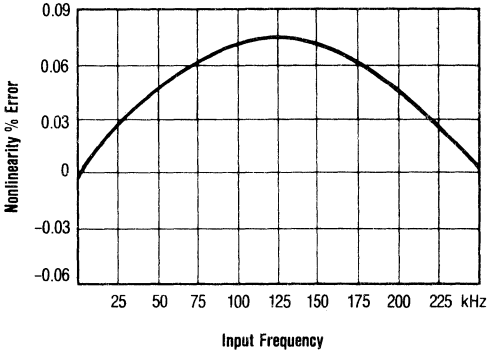
4153 250kHz Full Scale Temperature Drift



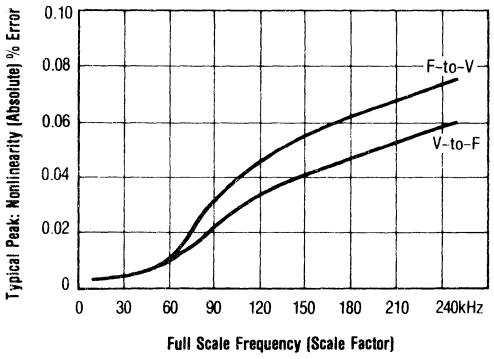
4153 250kHz Frequency-to-Voltage Nonlinearity



4153 250kHz Voltage-to-Frequency Nonlinearity

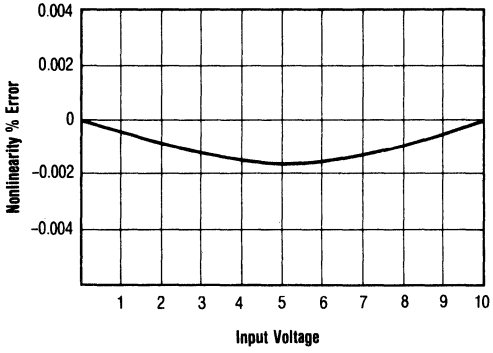


4153 Scale Factor vs. Typical Peak Linearity

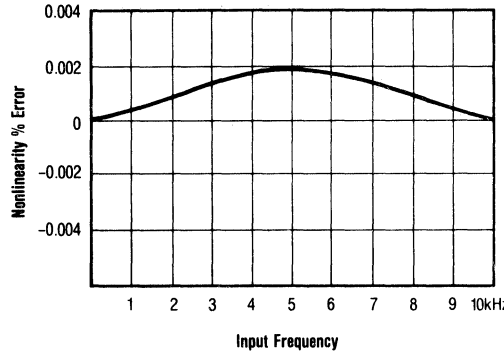


Typical Performance Characteristics (Continued)

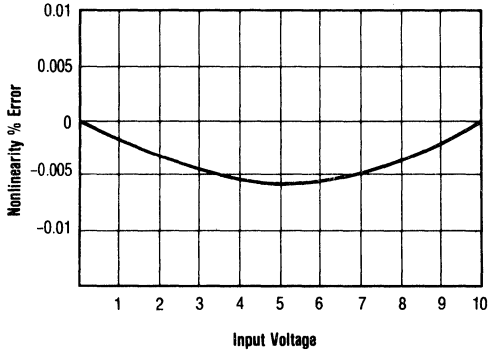
4153 10kHz Voltage-to-Frequency Nonlinearity



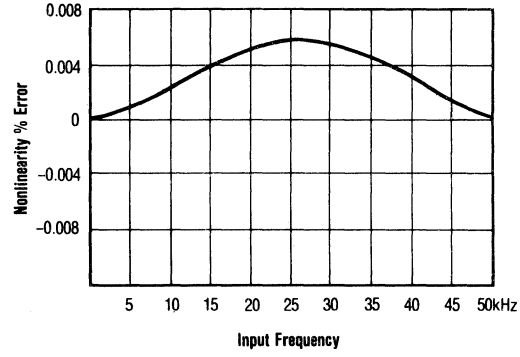
4153 10kHz Frequency-to-Voltage Nonlinearity



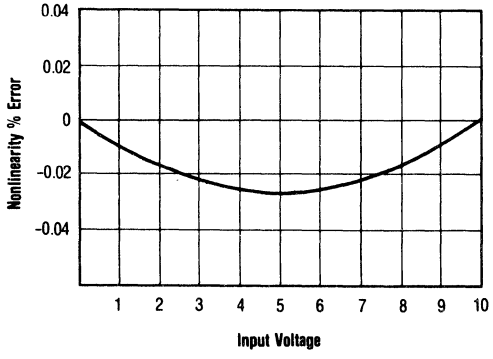
4153 50kHz Voltage-to-Frequency Nonlinearity



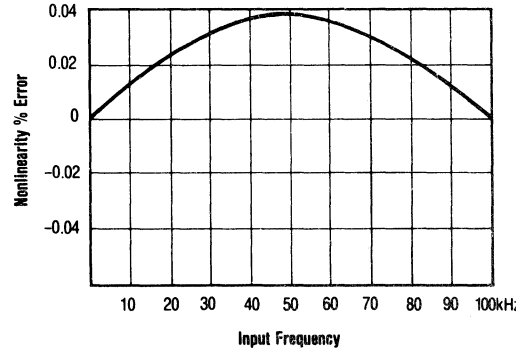
4153 50kHz Frequency-to-Voltage Nonlinearity



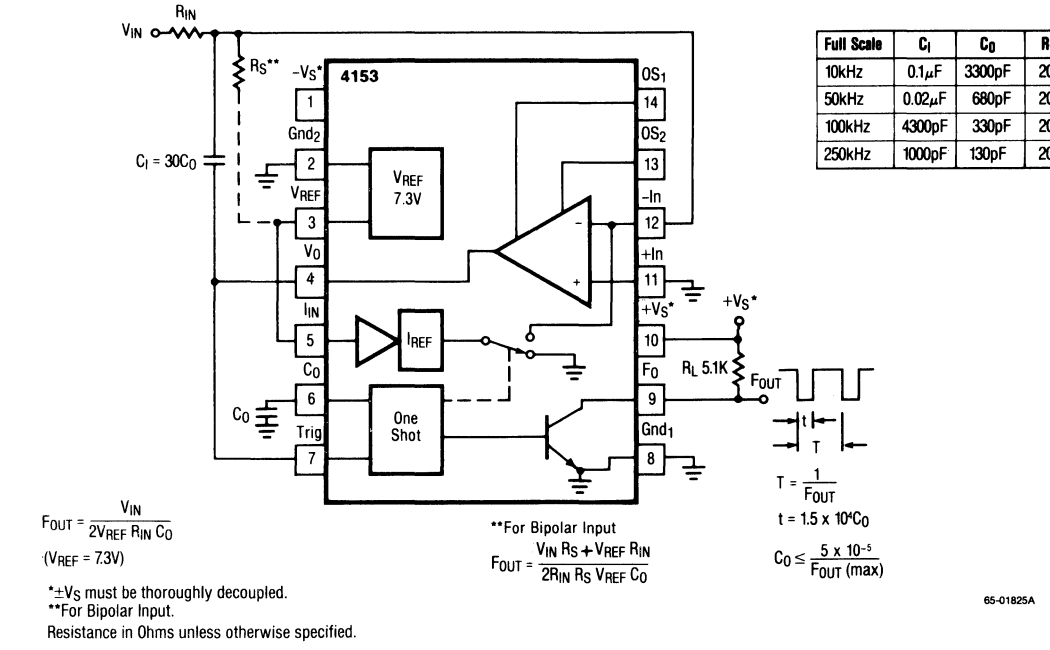
4153 100kHz Voltage-to-Frequency Nonlinearity



4153 100kHz Frequency-to-Voltage Nonlinearity



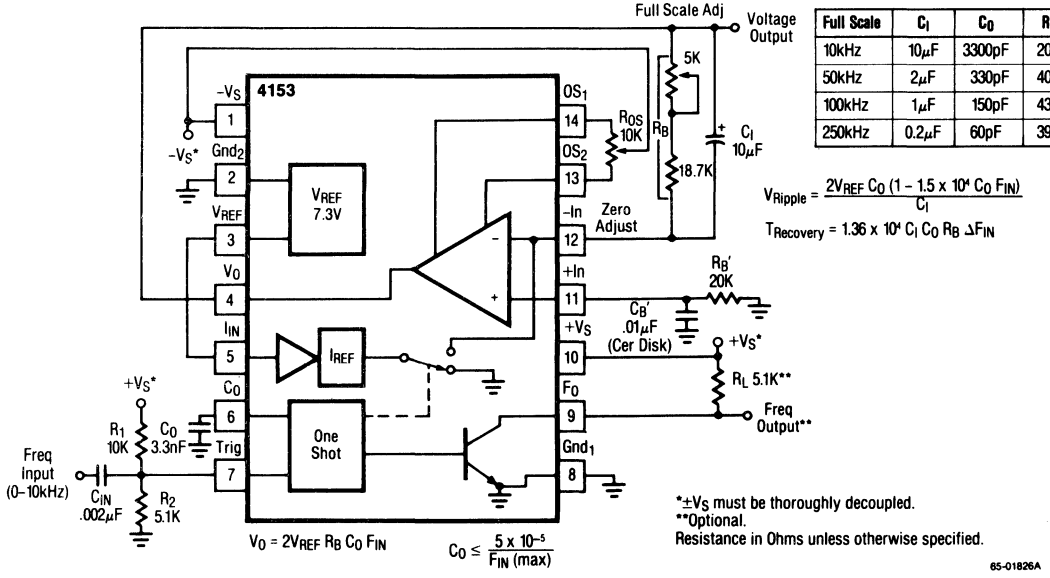
Typical Application Circuits



Full Scale	CI	CO	RIN
10kHz	0.1μF	3300pF	20K
50kHz	0.02μF	680pF	20K
100kHz	4300pF	330pF	20K
250kHz	1000pF	130pF	20K

*±VS must be thoroughly decoupled.
**For Bipolar Input.
Resistance in Ohms unless otherwise specified.

Figure 1. Voltage-to-Frequency Converter Minimum Circuit

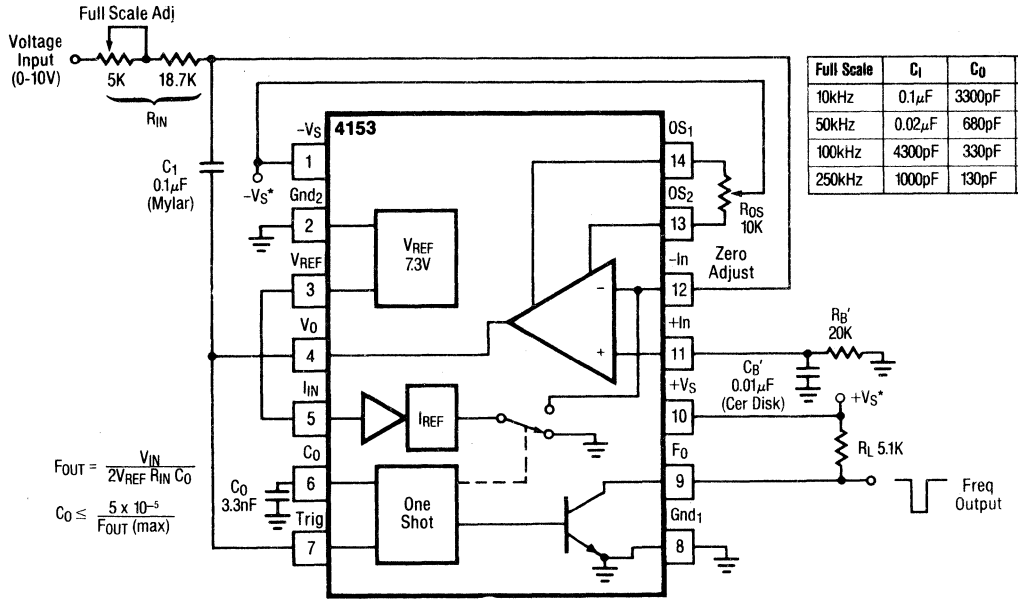


Full Scale	CI	CO	RB
10kHz	10μF	3300pF	20K
50kHz	2μF	330pF	40K
100kHz	1μF	150pF	43K
250kHz	0.2μF	60pF	39K

*±VS must be thoroughly decoupled.
**Optional.
Resistance in Ohms unless otherwise specified.

Figure 2. Frequency-to-Voltage Converter — V_O (Volts) = F_{IN} (kHz) — 100kHz Max

Typical Application Circuits (Continued)



Full Scale	C_I	C_O	R_{IN}
10kHz	0.1μF	3300pF	20K
50kHz	0.02μF	680pF	20K
100kHz	4300pF	330pF	20K
250kHz	1000pF	130pF	20K

Figure 3. Voltage-to-Frequency Converter With Offset and Gain Adjusts

Principles of Operation

The 4153 consists of several functional blocks which provide either voltage-to-frequency or frequency-to-voltage conversion, depending on how they are connected. The operation is best understood by examining the block diagram as it is powered in a voltage-to-frequency mode.

When power is first applied, all capacitors are discharged. The input current, V_{IN}/R_{IN}, causes C_{IN} to charge, and point **C** will try to ramp down. The trigger threshold of the one-shot is approximately +1.3V, and if the integrator output is less than +1.3V, the one-shot will fire and pulse the open collector output **E** and the switched current source **A** (see Figures 4 and 5). Because the point **C** is less than +1.3V, the one-shot fires, and the switched current source delivers a negative current pulse to the integrator. This causes C_{IN} to charge in the opposite direction, and point **C** will ramp up until the end of the one-shot pulse. At that time, the positive current V_{IN}/R_{IN} will again make point **C** ramp down until the trigger threshold is reached.

When power is applied, the one-shot will continuously fire until the integrator output exceeds the trigger threshold. Once this is reached, the one-shot will fire as needed to keep the integrator output above the trigger threshold. If V_{IN} is increased, the slope of the downward ramp increases, and the one-shot will fire more often in order to keep the integrator output high. Since the one-shot firing frequency is the same as the open collector output frequency, any increase in V_{IN} will cause an increase in F_{OUT}. This relationship is very linear because the amount of charge in each I_{OUT} pulse is carefully defined, both in magnitude and duration. The duration of the pulse is set by the timing capacitor C_O (point **D**). This feedback system is called a charge balanced loop.

The scale factor (the number of pulses per second for a specified V_{IN}) is adjusted by changing either R_{IN} and therefore I_{IN}, or by changing the amount of charge in each I_O pulse. Since the magnitude of I_O is fixed at 1 milliamp,

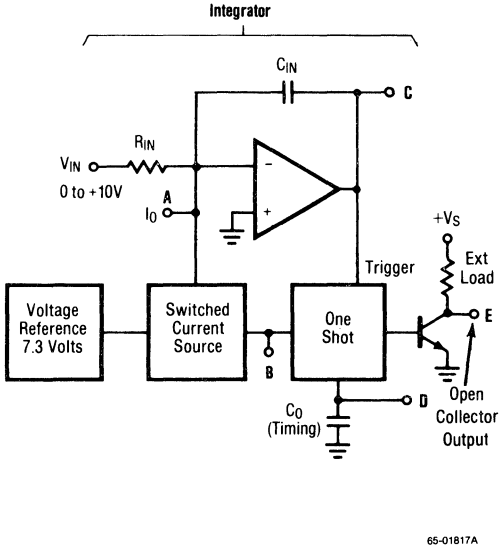


Figure 4. VFC Block Diagram

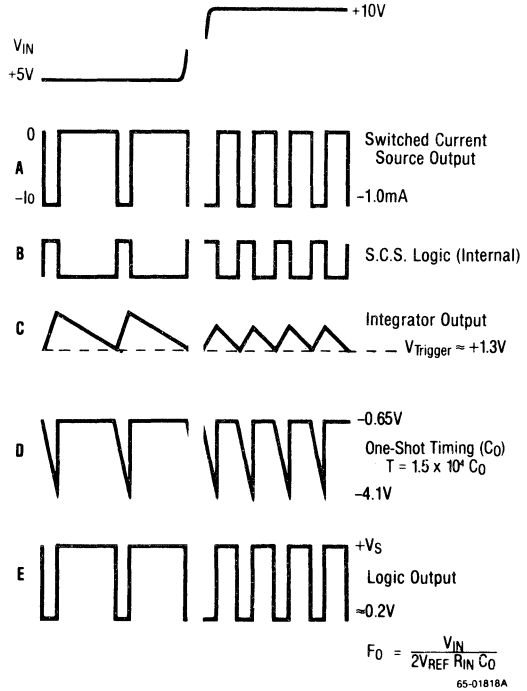


Figure 5. 4153 Voltage-to-Frequency Timing Waveforms

the way to change the amount of charge is by adjusting the one-shot duration set by C_O. (I_O may be adjusted by changing V_{REF}.) The accuracy of the relationship between V_{IN} and F_{OUT} is affected by three major sources of error: temperature drift, nonlinearity, and offset.

The total temperature drift is the sum of the individual drift of the components that make up the system. The greatest source of drift in a typical application is in the timing capacitor, C_O. Low temperature coefficient capacitors, such as silver mica and polystyrene, should be measured for drift, using a capacitance meter. Experimentation has shown that the lowest tempco's are achieved by wiring a parallel capacitor composed of 70% silver mica and 30% polystyrene.

The reference on the chip can be replaced by an external reference with much tighter drift specifications, such as an LM199. The 199s 6.9V output is close to the 4153s 7.3V output, and has less than 10 ppm/° C drift.

Nonlinearity is primarily caused by changes in the precise amount of charge in each I_{OUT} pulse. As frequency increases, internal stray capacitances and switching problems change the width and amplitude of the I_{OUT} pulses, causing a nonlinear relationship between V_{IN} and F_{OUT}. For this reason, the scale factor you choose should be below 1kHz/V or as low as the acquisition time of your system will allow.

Nonlinearity is also affected by the ratio of C_I to C_O. Less error can be achieved by increasing the value of C_I, but this affects response time and temperature drift. Optimum values for C_I and C_O are shown in the tables in Figures 1, 2, and 3. These values represent the best compromise of nonlinearity and temperature drift. Polypropylene, mylar or polystyrene capacitors should be used for C_I.

The accuracy at low input voltages is limited by the offset and V_{OS} drift of the op amp. To improve this condition, an offset adjust is provided.
Once your system is running, it may be calibrated as follows: apply a measured full scale input voltage and adjust R_{IN} until the scale factor is correct. For precise applications, trimming by soldering metal film resistors in parallel is recommended instead of trimpots, which have bad tempco's and are easily taken out of adjustment by mechanical shock. After the scale factor is calibrated, apply a known small input voltage (approximately 10mV) and adjust the op amp offset until the output frequency equals the input multiplied by the scale factor.

The output **E** consists of a series of negative going pulses with a pulse width equal to the one-shot time. The open collector pull up resistor may be connected to a different supply (such as 5V for TTL) as long as it does not exceed the value of $+V_S$ applied to pin 10. The load current should be kept below 10mA in order to minimize strain on the device. Pins 2 and 8 must be grounded in all applications, even if the open collector transistor is not used.

Figure 6 shows the complete circuit for a precision frequency-to-voltage converter. This circuit converts an input frequency to a proportional voltage by integrating the switched current source output. As the input frequency increases, the number of I_{OUT} pulses delivered to the integrator increases, thus increasing the average output voltage. Depending on the time constant of the integrator, there will be some ripple on the output. The output may be further filtered, but this will reduce the response time. A second order filter will decrease ripple and improve response time.

The output waveform must meet three conditions for proper frequency-to-voltage operation. First, it must have sufficient amplitude and offset to swing above and below the 1.3V trigger threshold. (See Figure 6 for an example of AC coupling and offset bias.) Second, it must be a fast slewing waveform having a quick rise time. A comparator may be used to square it up. Finally, the input pulse width must not exceed the one-shot time, in order to avoid retriggering the one-shot (AC couple the input).

Capacitive coupling between the trigger input and the timing capacitor pin may occur if the input waveform is a squarewave or the input has a short period. This can cause gross nonlinearity due to changes in the one-shot timing waveform (see Figure 7). This problem can be avoided by keeping the value of C_O small, and thereby keeping the timing period less than the input waveform period.

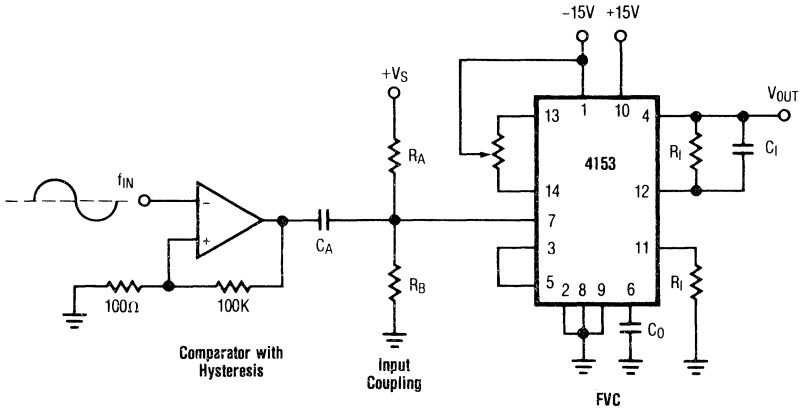


Figure 6. FVC Input Conditioning

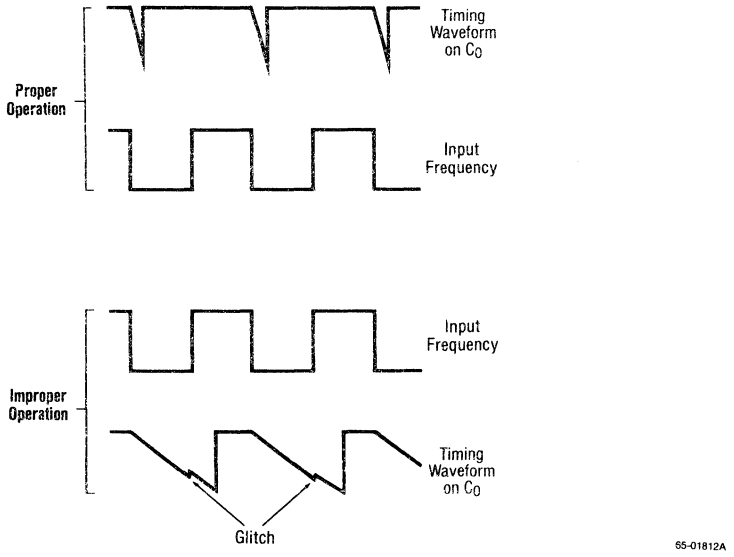


Figure 7. FVC Timing Waveform

Detailed Circuit Operation

The circuit consists of a buried zener reference (breakdown occurs below the surface of the die, reducing noise and contamination), a high speed one-shot, a high speed switched precision voltage-to-current converter, and an open collector output transistor.

Figure 8 shows a block diagram of the high speed one-shot and Figure 9 shows the monolithic implementation. A trigger pulse sets the R-S latch, which lets C_O charge from I_T. When the voltage on C_O exceeds V_{TH}, the comparator resets the latch and discharges C_O. Looking at the detailed schematic, a positive trigger voltage turns on Q5, turns off Q4, and turns on Q3. Q3 provides more drive to Q5 keeping it on and latching the base of Q11 low. This turns on the switched current source and turns off Q1, allowing C_O to charge in a negative direction. When the voltage on C_O exceeds V_{TH}, Q13's collector pulls Q3's base down, resetting the latch, turning off the switched current source and discharging C_O through Q1. Note that all of the transistors in the signal path are NPNs and that the voltage swings are minimized ECL fashion to reduce delays. Minimum delay means minimum drift of the resultant VFC scale factor at high frequency.

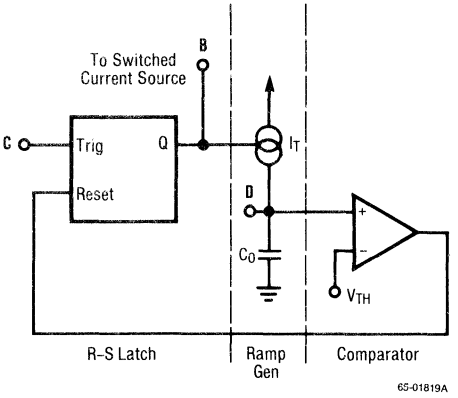


Figure 8. One-Shot Block Diagram

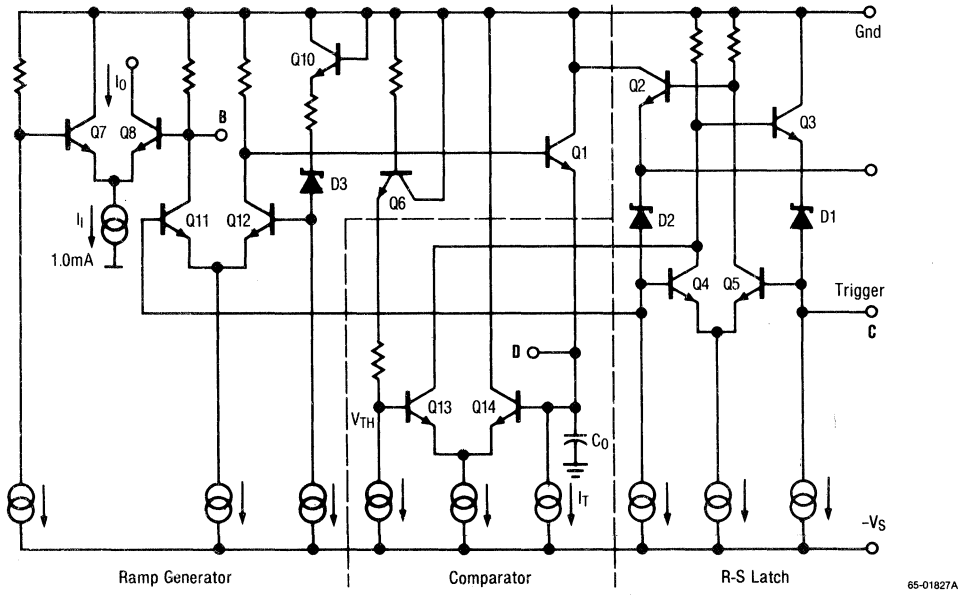


Figure 9. One-Shot Detail

The switched current source is shown as a block diagram in Figure 10 and detailed in Figure 11. The summing node (+ input of op amp) is held at 0V by the amplifier feedback, causing V_{REF} to be applied across R60. This current (V_{REF}/R60), minus the small amplifier bias current, flows through Q35. Q35 develops a V_{BE} dependent on that current. This V_{BE} is developed across Q36. Since Q35 and Q36 are equal in area, their currents are equal. This mirrored current is switched by the one-shot output.

The detail schematic shows the amplifier and load (Q21 through Q34), the mirror transistors (Q35, Q36) and the differential switching transistors (Q7, Q8). The amplifier uses a complementary paraphase input composed of Q21 through Q26 with a current mirror formed by Q27 through Q30, which converts from differential to single ended output. Level shift diodes Q32 and Q34 and emitter follower Q31 bootstrap the emitters of the mirror devices Q29 and Q30 to increase gain and lower input offsets, which would otherwise be caused by unbalanced collector voltages on Q23 and Q26. Matching emitter currents in Q35 and Q36 are assured by degeneration resistors R3 and R4. The differential switch allows the current source to remain active continuously, shunting to ground in the off state. This helps stabilize the output, and again, NPNs reduce switching time, timing errors, and most important, drift of timing errors over temperature.

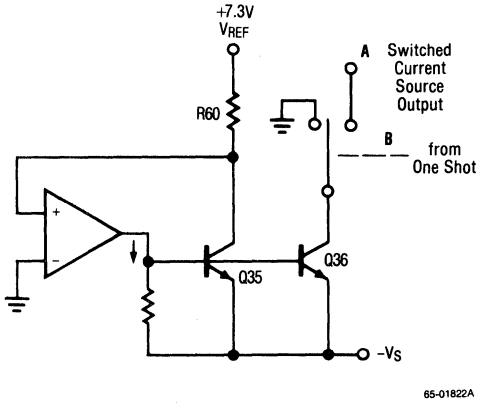


Figure 10. Switched Current Source Simplified Diagram

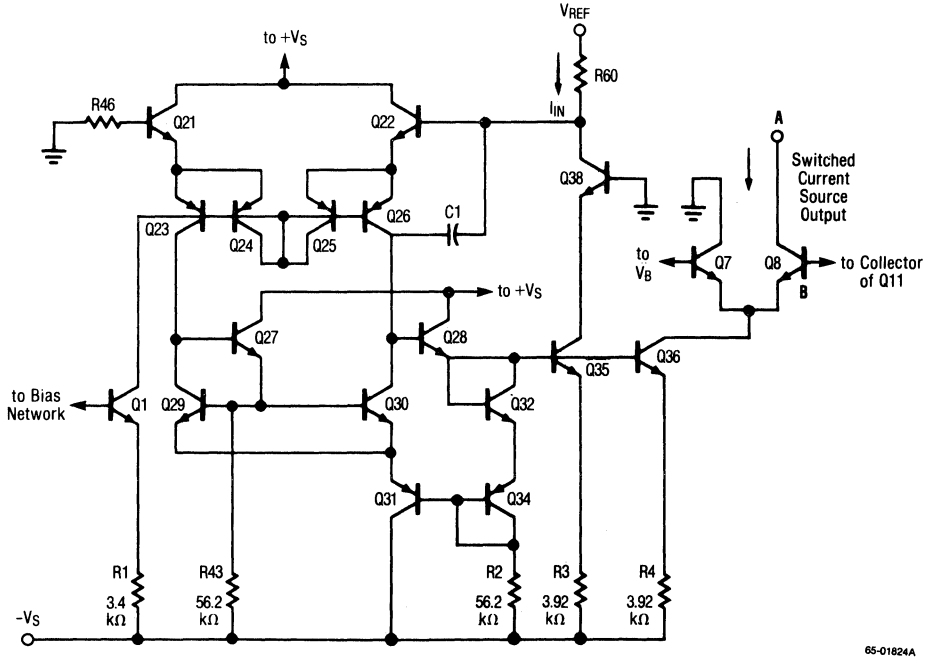


Figure 11. Switched Current Source (Detail)

SECTION 8

VOLTAGE REFERENCES

DEFINITIONS

Line Regulation
The ratio of change in output voltage to the change in supply (line) voltage effecting it, expressed as a percentage of the output voltage per volt change in supply voltage (%/V).

Load Regulation
The ratio of change in output voltage to the change in load (output) current effecting it, measured in percent of output voltage per milliamp change in load current (%/mA).

Output Voltage Noise
Output voltage noise is the broadband noise over a specified range of frequencies, measured in microvolts peak-to-peak (μV_{p-p}).

Short Circuit Current
The maximum output current available from the regulator with the output shorted to ground, expressed in milliamps (mA).

Sink Current
The amount of current that can be forced into the output with the reference still within ±3% regulation, expressed in milliamps (mA).

Supply Current (I_S)
The current required from the power supply to operate the regulator under quiescent no-load conditions, expressed in milliamps (mA).

Supply Voltage (V_S)
The range of power supply voltages over which the regulator will operate, expressed in volts (V).

Temperature Coefficient (T_C)
The change in the output voltage over specified temperature range in parts per million per °C (ppm/°C).

REF-01 +10V Precision Voltage References

Features

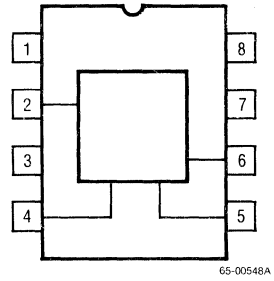
- +10V output — ±0.3%
- Adjustable — ±3%
- Excellent temperature stability — 3 ppm/°C
- Low noise — 20 μV_{p-p}
- Wide input voltage range — +12V to +40V
- No external components
- Short circuit proof
- Low power consumption — 15 mW

Description

The REF-01 Precision Voltage Reference contains a bandgap reference using thin film resistors, a step-up amplifier, short circuit protection, and a zener trim network. The REF-01's +10V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient.

Connection Information

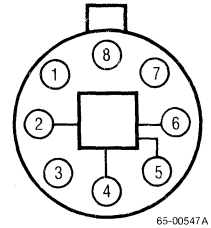
8-Lead Dual In-Line Package
(Top View)



65-00548A

Pin	Function
1	NC
2	$+V_S$
3	NC
4	Ground
5	Adjust
6	Output
7	NC
8	NC

8-Lead TO-99 Metal Can
(Top View)



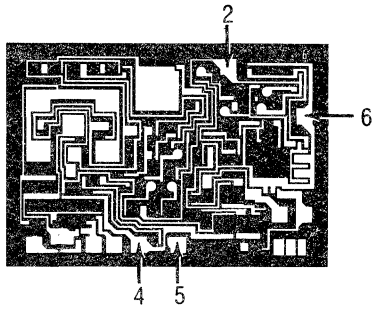
65-00547A

Ordering Information

Part Number	Package	Operating Temperature Range
REF-01CD	D	0°C to +70°C
REF-01DD	D	0°C to +70°C
REF-01ED	D	0°C to +70°C
REF-01HD	D	0°C to +70°C
REF-01CN	N	0°C to +70°C
REF-01DN	N	0°C to +70°C
REF-01EN	N	0°C to +70°C
REF-01HN	N	0°C to +70°C
REF-01CT	T	0°C to +70°C
REF-01DT	T	0°C to +70°C
REF-01ET	T	0°C to +70°C
REF-01HT	T	0°C to +70°C
REF-01AD	D	-55°C to +125°C
REF-01AD/883B	D	-55°C to +125°C
REF-01D	D	-55°C to +125°C
REF-01D/883B	D	-55°C to +125°C
REF-01AT	T	-55°C to +125°C
REF-01AT/883B	T	-55°C to +125°C
REF-01T	T	-55°C to +125°C
REF-01T/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Mask Pattern



Die Size: 55 x 79 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage
- REF-01A, E, H Grades ..... +40V
- REF-01C, D Grades ..... +30V

Internal Power Dissipation ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
- Range ..... -65°C to +150°C

Operating Temperature Range
- REF-01A, -01 ..... -55°C to +125°C
- REF-01E,H,C,D ..... 0°C to +70°C

Lead Soldering Temperature
- (60 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+175°C	+125°C
Max. P_D T_A <50°C	833 mW	658 mW	468 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	—
Therm. Res. θ_{JA}	150°C/W	190°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-01A/E			REF-01/H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	R_P = 10kΩ	±3.0	±3.3		±3.0	±3.3		%
Output Voltage Noise[1]	0.1Hz to 10Hz		20	30		20	30	μV_{p-p}
Supply Voltage		12		40	12		40	V
Line Regulation[2]	V_S = +13V to +33V		0.006	0.010		0.006	0.010	%/V
Load Regulation[2]	I_L = 0mA to 10mA		0.005	0.008		0.006	0.010	%/mA
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.4		1.0	1.4	mA
Load Current		10	21		10	21		mA
Sink Current		-0.3	-0.5		-0.3	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA

Electrical Characteristics (V_S = +15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	REF-01A			REF-01			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3] [4]	Over Temp. Range		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +13V to +33V		0.009	0.015		0.009	0.015	%/V
Load Regulation[2]	I_O = 0mA to 8mA		0.007	0.012		0.007	0.012	%/mA

Notes: 1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{10V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{180°C}$

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-01C			REF-01D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	9.90	10.00	10.10	9.850	10.00	10.150	V
Output Adjustment Range	R_P = 10kΩ	±2.7	±3.3		±2.0	±3.3		%
Output Voltage Noise[1]	0.1Hz to 10Hz		25	35		25		μV_{p-p}
Supply Voltage		12		30	12		30	V
Line Regulation[2]	V_S = +13V to +33V		0.009	0.015		0.012	0.04	%/V
Load Regulation[2]	I_L = 0mA to 8mA		0.006	0.015				%/mA
	I_L = 0mA to 4mA		0.006	0.015		0.009	0.04	
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.6		1.0	2.0	mA
Load Current		8.0	21		8.0	21		mA
Sink Current		-0.2	-0.5		-0.2	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA

Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C, and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-01E			REF-01H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3] [4]	Over Temp. Range		0.02	0.06		0.07	0.17	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +13V to +33V		0.007	0.012		0.007	0.012	%/V
Load Regulation[2]	I_L = 0mA to 8mA		0.006	0.010		0.007	0.012	%/mA

Notes: 1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{10V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$

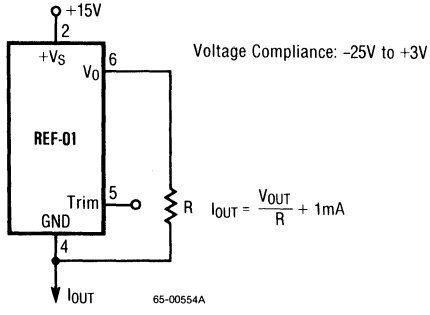
Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C, and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-01C			REF-01D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3] [4]	Over Temp. Range		0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		20	65		70	250	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +13V to +30V		0.011	0.018		0.020	0.025	%/V
Load Regulation[2]	I_O = 0mA to 5mA		0.008	0.018		0.020	0.025	%/mA

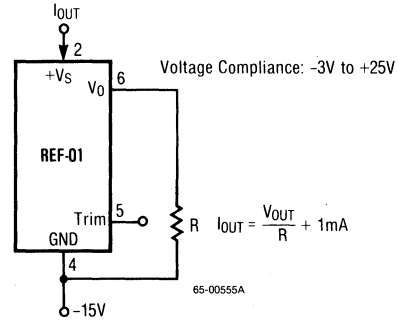
Notes:
1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{10V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$

Typical Applications

Current Source

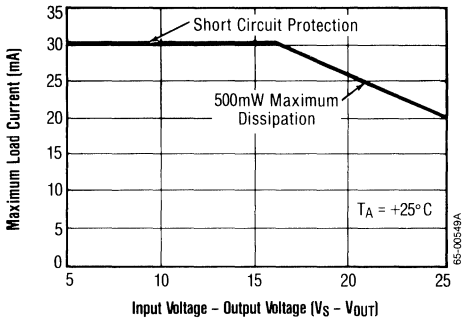


Current Sink

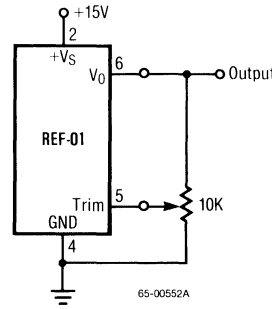


Typical Performance Characteristics

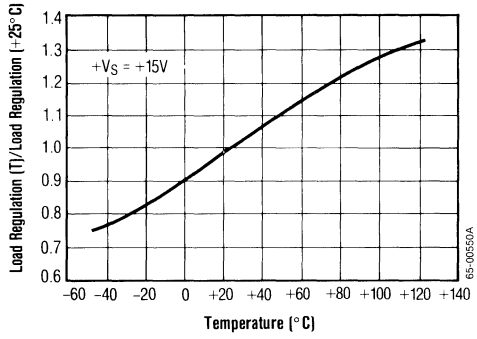
Maximum Load Current vs. Differential Input Voltage



Output Adjustment

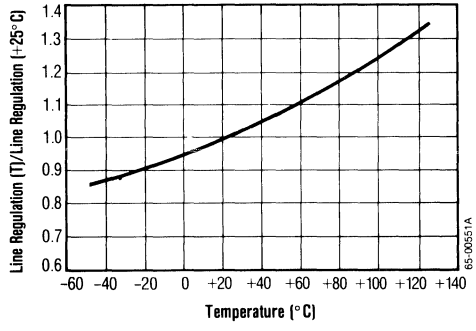


Normalized Load Regulation (ΔIL = 10mA) vs. Temperature

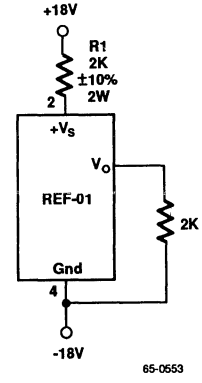


The REF-01 trim terminal can be used to adjust the output voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V or to 10.240V for binary operation. Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

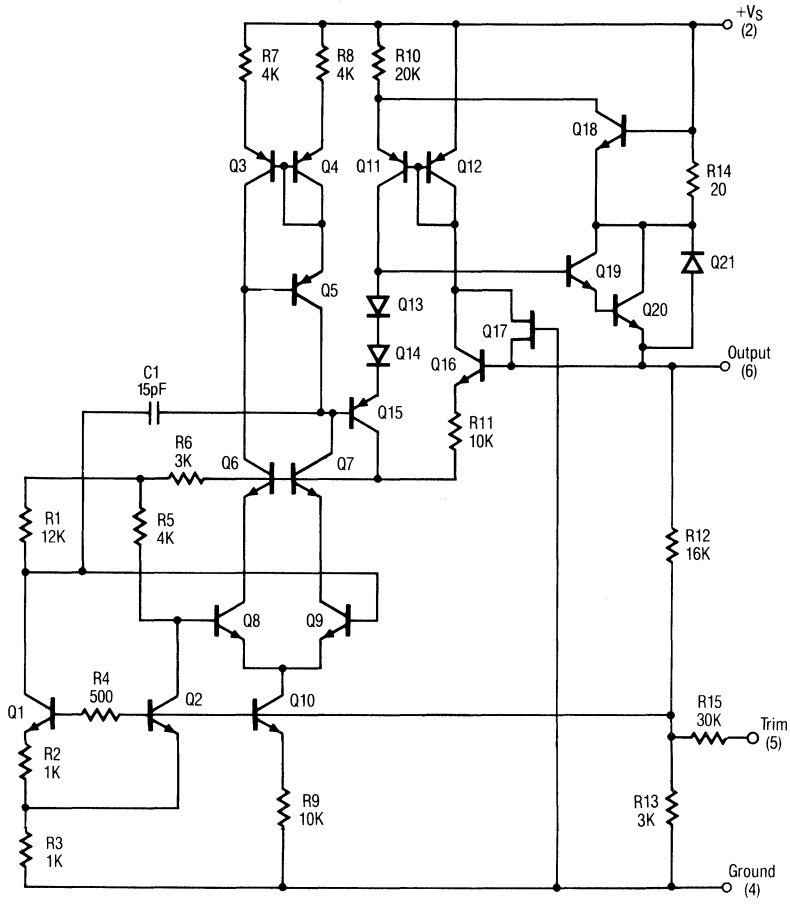
Normalized Line Regulation vs. Temperature



Burn-In Circuit



Simplified Schematic Diagram



REF-02 +5V Precision Voltage References

Features

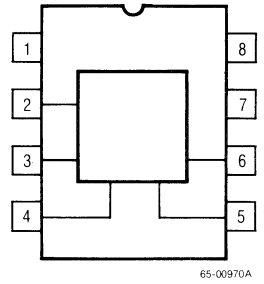
- +5V output — ±0.3%
- Adjustable — ±3%
- Excellent temperature stability — 3 ppm/°C
- Low noise — 10 μV_{p-p}
- Wide input voltage range — +7V to +40V
- No external components
- Short circuit proof
- Low power consumption — 10 mW

Description

The REF-02 Precision Voltage Reference contains a bandgap reference using thin-film resistors, a step-up amplifier, short circuit protection, and a zener trim network. The REF-02's +5V output shows excellent stability for large changes of temperature, load current, and input voltage. An adjust pin is provided that can change the output voltage by at least 3% with little effect on temperature coefficient. A tempco pin also provides a voltage that varies linearly with temperature, typically from +470 mV to +830 mV over the military temperature range.

Connection Information

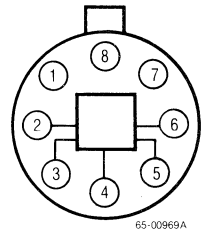
8-Lead Dual In-Line Package
(Top View)



65-00970A

Pin	Function
1	NC
2	$+V_S$
3	Tempco
4	Ground
5	Adjust
6	Output
7	NC
8	NC

8-Lead TO-99 Metal Can
(Top View)



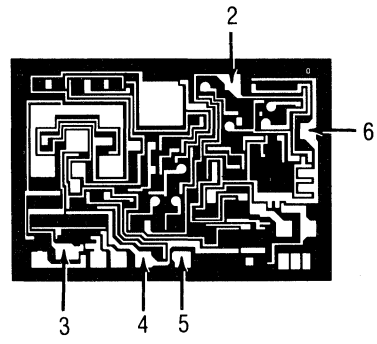
65-00969A

Ordering Information

Part Number	Package	Operating Temperature Range
REF-02CD	D	0°C to +70°C
REF-02DD	D	0°C to +70°C
REF-02ED	D	0°C to +70°C
REF-02HD	D	0°C to +70°C
REF-02CN	N	0°C to +70°C
REF-02DN	N	0°C to +70°C
REF-02EN	N	0°C to +70°C
REF-02HN	N	0°C to +70°C
REF-02CT	T	0°C to +70°C
REF-02DT	T	0°C to +70°C
REF-02ET	T	0°C to +70°C
REF-02HT	T	0°C to +70°C
REF-02AD	D	-55°C to +125°C
REF-02AD/883B	D	-55°C to +125°C
REF-02D	D	-55°C to +125°C
REF-02D/883B	D	-55°C to +125°C
REF-02AT	T	-55°C to +125°C
REF-02AT/883B	T	-55°C to +125°C
REF-02T	T	-55°C to +125°C
REF-02T/883B	T	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
T = 8-lead metal can (TO-99)
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Mask Pattern



Die Size: 79 x 55 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage
REF-02A, E, H Grades ..... +40V
REF-02C, D Grades ..... +30V
Internal Power Dissipation ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
REF-02A, -01 ..... -55°C to +125°C
REF-02E,H,C,D ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+175°C	+125°C
Max. P_D T_A <50°C	833 mW	658 mW	468 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	—
Therm. Res. θ_{JA}	150°C/W	190°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-02A/E			REF-02/H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	R_P = 10kΩ	±3.0	±6.0		±3.0	±6.0		%
Output Voltage Noise[1]	0.1Hz to 10Hz		10	15		10	15	μV_{p-p}
Supply Voltage		7		40	7		40	V
Line Regulation[2]	V_S = +8V to +33V		0.006	0.010		0.006	0.010	%/V
Load Regulation[2]	I_L = 0mA to 10mA		0.005	0.010		0.006	0.010	%/mA
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.4		1.0	1.4	mA
Load Current		10	21		10	21		mA
Sink Current		-0.3	-0.5		-0.3	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA
Tempco Voltage Output[6]			630			630		mV

Electrical Characteristics (V_S = +15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	REF-02A			REF-02			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.06	0.15		0.18	0.45	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.009	0.015		0.009	0.015	%/V
Load Regulation[2]	I_O = 0mA to 8mA		0.007	0.012		0.007	0.012	%/mA
Tempco Voltage Output Temperature Coefficient[6]			2.1			2.1		mV/°C

Notes: 1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{5V}$ x 100%
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +5V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{180°C}$
6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

Electrical Characteristics (V_S = +15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	REF-02C			REF-02D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	I_L = 0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	R_P = 10kΩ	±2.7	±6.0		±2.0	±6.0		%
Output Voltage Noise[1]	0.1Hz to 10Hz		12	18		12		μV_{p-p}
Supply Voltage		7.0		30	7.0		30	V
Line Regulation[2]	V_S = +8V to +33V		0.009	0.015		0.012	0.04	%/V
Load Regulation[2]	I_L = 0mA to 8mA I_L = 0mA to 4mA		0.006	0.015		0.009	0.04	%/mA
Turn-on Settling Time	To ±0.1% of Final Value		5.0			5.0		μS
Supply Current	No Load		1.0	1.6		1.0	2.0	mA
Load Current		8.0	21		8.0	21		mA
Sink Current		-0.2	-0.5		-0.2	-0.5		mA
Short Circuit Current	V_O = 0		30			30		mA
Tempco Voltage Output[6]			630			630		mV

Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-02E			REF-02H			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3] [4]	Over Temp. Range		0.02	0.06		0.07	0.17	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		3.0	8.5		10	25	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.007	0.012		0.007	0.012	%/V
Load Regulation[2]	I_L = 0mA to 8mA		0.006	0.010		0.007	0.012	%/mA
Tempco Voltage Output Temperature Coefficient[6]			2.1			2.1		mV/°C

Notes: 1. Guaranteed by design.

2. Line and load regulation specifications include the effects of self heating.

3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{5V}$ x 100%

4. Output voltage change with temperature specification applies untrimmed, or trimmed to +10V.

5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$

6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

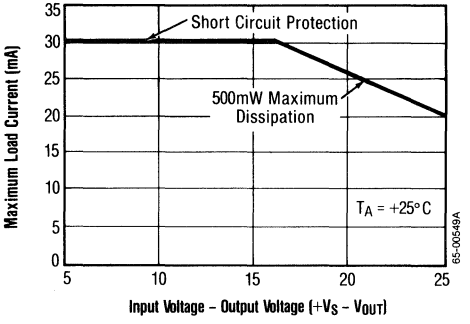
Electrical Characteristics (V_S = +15V, 0°C ≤ T_A ≤ +70°C and I_O = 0 unless otherwise noted)

Parameters	Test Conditions	REF-02C			REF-02D			Units
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Change With Temperature[3,4]	Over Temp. Range		0.14	0.45		0.49	1.7	%
Output Voltage Temperature Coefficient[5]	Over Temp. Range		20	65		70	250	ppm/°C
Change in V_{OUT} Temperature Coefficient With Output Adjustment	R_P = 10kΩ		0.7			0.7		ppm/%
Line Regulation[2]	V_S = +8V to +33V		0.011	0.018		0.020	0.025	%/V
Load Regulation[2]	I_O = 0mA to 5mA		0.008	0.018		0.020	0.025	%/mA
Tempco Voltage Output Temperature Coefficient[6]			2.1			2.1		mV/°C

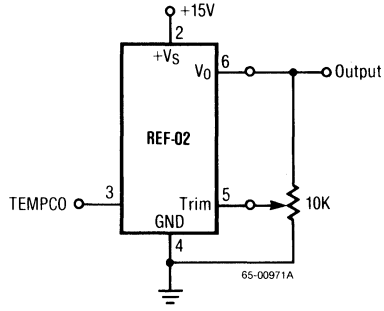
Notes:
1. Guaranteed by design.
2. Line and load regulation specifications include the effects of self heating.
3. Output voltage change with temperature = $\frac{V_{MAX} - V_{MIN}}{5V} \times 100\%$
4. Output voltage change with temperature specification applies untrimmed, or trimmed to +5V.
5. Output voltage temperature coefficient = $\frac{\text{Output voltage change with temperature}}{70°C}$
6. Limit current in or out of pin 3 to 50nA and limit capacitance on pin 3 to 30pF.

Typical Performance Characteristics

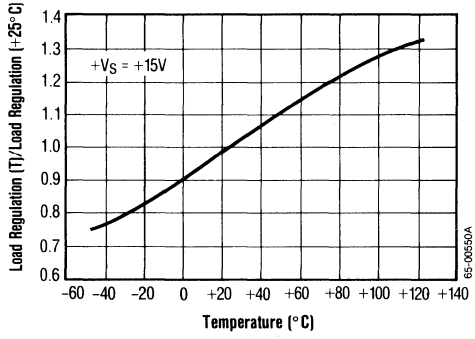
Maximum Load Current vs. Differential Input Voltage



Output Adjustment

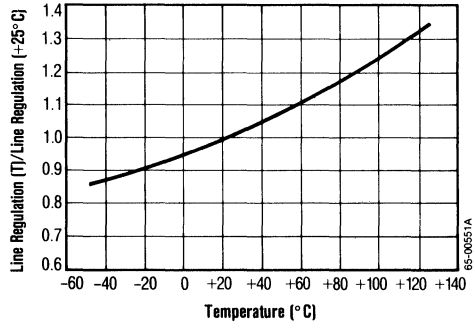


Normalized Load Regulation (ΔIL = 10mA) vs. Temperature

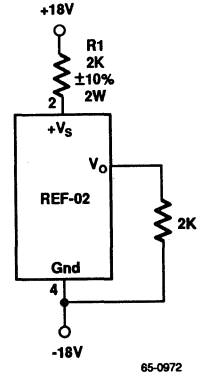


The REF-02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary operation. Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

Normalized Line Regulation vs. Temperature



Burn-In Circuit



Typical Applications

Figure 3 shows how the REF-02 can be connected with an OP-07 to create an electronic thermometer. The circuit uses the +5V reference output and the op amp to level shift and amplify the 2.1mV/°C Tempco output into a voltage signal dependent on the ambient temperature. Different scaling can be obtained by selecting appropriate resistors from the table in Figure 3, giving output slopes calibrated in degrees Celsius or degrees Fahrenheit.

To calibrate, first measure the voltage on the Tempco pin (V_{TEMPCO}) and the ambient room temperature (T_A in °C). Put those values into the following equation:

$$X = \frac{V_{TEMPCO} \text{ (in millivolts)}}{(S)\ (T_A + 273)}$$

Where S = Scale factor for your circuit selected from the table in Figure 3 (in millivolts).

Then turn the circuit power off, short V_{OUT} (pin 6) of the REF-02 to ground, and while applying exactly 100.00mV to the op amp output, adjust R_{B2} so that V_B = (x) (100mV). Now remove the short and the 100mV source, reapply circuit power and adjust R_P so that the op amp output voltage equals (T_A) (S). The system is now exactly calibrated.

For remote sensor applications a 1.5kΩ resistor (R_S) must be connected in series with the Tempco pin to isolate it from cable capacitances. Low temperature coefficient metal film resistors must be used for R_A, R_B and R_C.

Better grades of REF-02 will provide greater accuracy over a wider range of temperatures. To decrease op amp input errors, use an OP-27 instead of an OP-07. A system using a REF-02A and an OP-07C will provide a typical accuracy of ±0.5% over the military temperature range.

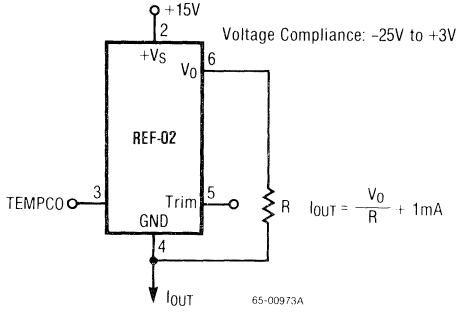


Figure 1. Current Source

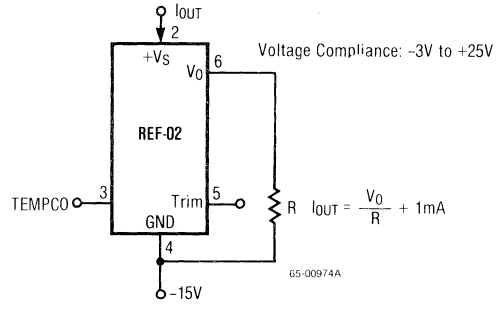
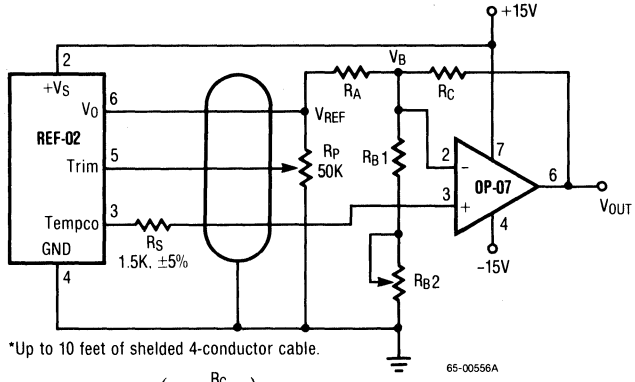


Figure 2. Current Sink



$$TCV_{OUT} = (2.1mV/°C)\left(1 + \frac{R_C}{R_A \,||\, R_B}\right)$$

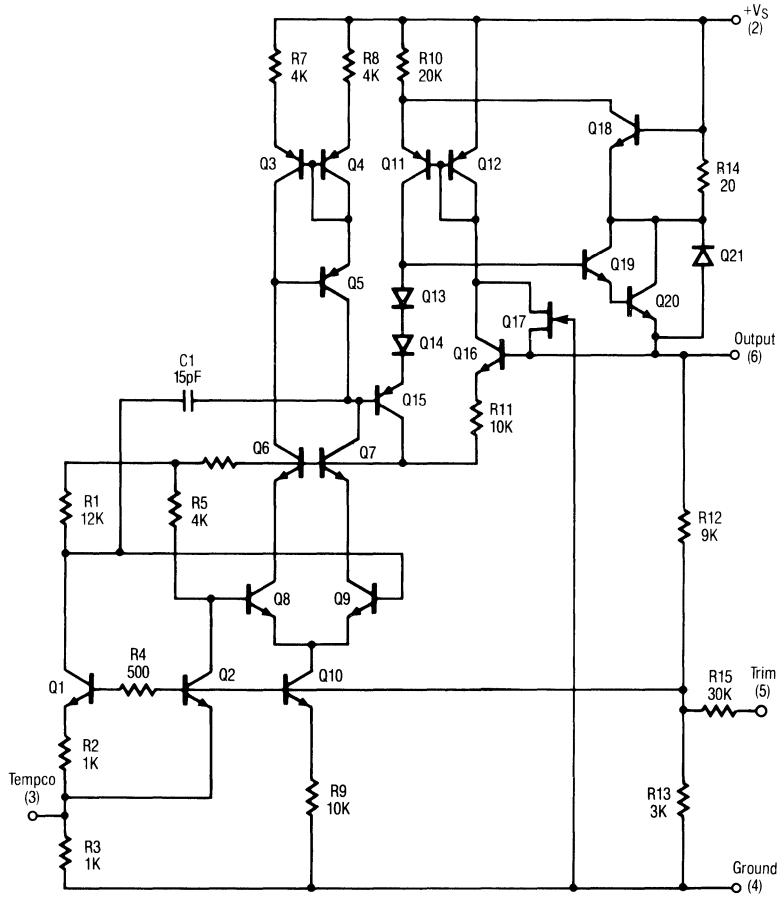
$$V_O = \left(H\,\frac{R_C}{R_A \,||\, R_B}\right)V_{Tempco} - \left(\frac{R_C}{R_A}\right)(V_O)$$

Resistor Values

TCVOUT Slope(s)	10mV/°C	100mV/°C	10mV/°F
Temperature Range	-55°C to +125°C	-55°C to +125°C	-65°F to +257°F
Output Voltage Range	-0.55V to +1.25V	-5.5V to +12.5V	-0.67V to +2.57V
Zero Scale	0V at 0°C	0V at 0°C	0V at 0°F
R_A (±1% Resistor)	9.09KΩ	15KΩ	8.25KΩ
R_{B1} (±1% Resistor)	1.5KΩ	1.82KΩ	1.0KΩ
R_{B2} (Potentiometer)	200Ω	500Ω	200Ω
R_C (±1% Resistor)	5.11KΩ	84.5KΩ	7.5KΩ

Figure 3. Precision Electronic Thermometer

Simplified Schematic Diagram



65-00968B

SECTION 9
VOLTAGE REGULATORS

RC4190 Micropower Switching Regulators

Features

- High efficiency — 85% typical
- Low quiescent current — 215 µA
- Adjustable output — 1.3V to 30V
- High switch current — 150 mA
- Bandgap reference — 1.31V
- Accurate oscillator frequency — ±10%
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- 8-lead packages including small outline (SO-8)

Description

The RC4190 monolithic IC is a low power switch mode regulator intended for miniature power supply applications. This DC-to-DC converter IC provides all of the active functions needed to create supplies for micropower circuits (load power up to 400 mW, or up to 10W with an external power transistor). Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

Application areas include on-card circuits where a non-standard voltage supply is needed, or in battery operated instruments where a 4190 can be used to extend battery lifetime.

These regulators can achieve up to 80% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 µA.

The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the 4190 adaptable to a wide range of miniature power supply applications.

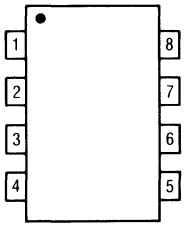
The 4190 is most suited for single ended step-up circuits because the internal switch transistor is referenced to ground. It is complemented by another Raytheon micropower switching regulator, the 4391, which is dedicated to step-down and negative output (inverting) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the 4391 data sheet for step-down and inverting applications.

With some optional external components the application circuit can be designed to signal a display when the battery has decayed below a predetermined level, or designed to signal a display at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other unique circuits.

The 4190 micropower switching regulator consists of two devices, each with slightly different specifications. The RM4190 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The RC4190 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical. Each type is available in plastic and ceramic DIPs, or SO-8 packages.

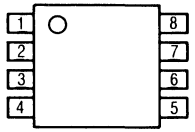
Connection Information

8-Lead DIP (Top View)



65-00070A

Small Outline SO-8 (Top View)



65-02666A

Pin	Function
1	Low Battery (Set) Resistor (LBR)
2	Timing Capacitor (C_X)
3	Ground
4	External Inductor (L_X)
5	+Supply Voltage (+V_S)
6	Reference Set Current (I_C)
7	Feedback Voltage (V_{FB})
8	Low Battery Detector Output (LBD)

Absolute Maximum Ratings

Supply Voltage (Without External Transistor)
- RM4190 ..... +30V
- RC4190 ..... +24V

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- RM4190 ..... -55°C to +125°C
- RC4190 ..... 0°C to +70°C

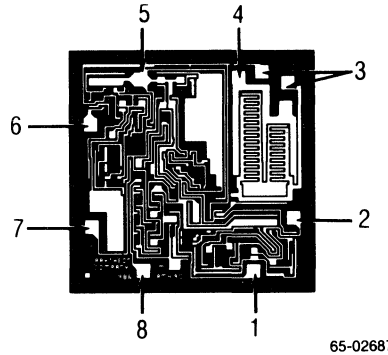
Switch Current ..... 375 mA Peak

Ordering Information

Part Number	Package	Operating Temperature Range
RC4190M	M	0°C to +70°C
RC4190N	N	0°C to +70°C
RM4190D	D	-55°C to +125°C
RM4190D/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Mask Pattern



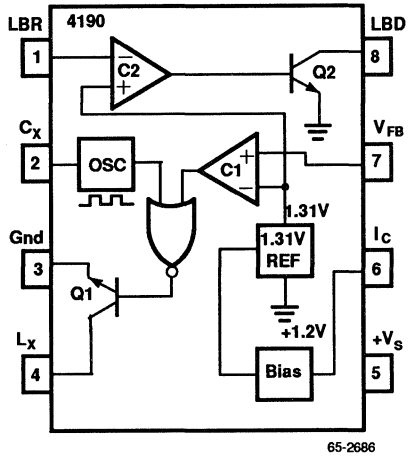
65-02687A

Die Size: 66 x 67 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	Small Outline SO-8
Max. Junction Temp.	+125°C	+175°C	+125°C
Max. P_D T_A <50°C	468 mW	833 mW	240 mW
Therm. Res θ_{JC}	—	45°C/W	—
Therm. Res. θ_{JA}	160°C/W	150°C/W	240°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	4.17 mW/°C

Functional Block Diagram



Electrical Characteristics

(+V_S = +6.0V, I_C = 5.0 μA unless otherwise noted, over the full operating temperature range)

Parameters	Symbol	Conditions	RM4190			RC4190			Units
			Min	Typ	Max	Min	Typ	Max	
Supply Voltage	$+V_S$		2.6		30	2.6		24	V
Reference Voltage (Internal)	V_{REF}		1.25	1.31	1.37	1.20	1.31	1.42	V
Supply Current	I_S	Measure at Pin 5 I_4 = 0		235	350		235	350	μA
Line Regulation		0.5 V_O < V_S < V_O		0.2	0.5		0.5	1.0	% V_O
Load Regulation	L_I	V_S = +0.5 V_O, P_L = 150 mW		0.5	1.0		0.5	1.0	% V_O
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	μA
Switch Leakage Current	I_{CO}	V_4 = 24V			30			30	μA
Supply Current (Disabled)	I_{SO}	$V_C \leq$ 200 mV			30			30	μA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1200		500	1200		μA
Oscillator Frequency Temperature Drift				±200			±200		ppm/ °C

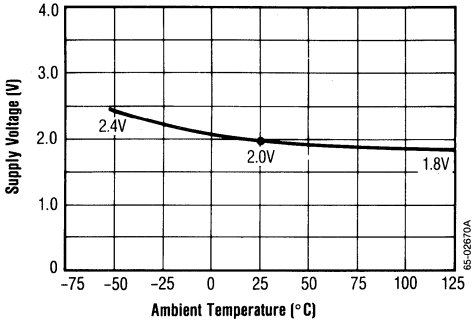
Electrical Characteristics ($+V_S$ = +6.0V, I_C = 5.0 μA, and T_A = +25°C unless otherwise noted)

Parameters	Symbol	Conditions	RM4190			RC4190			Units
			Min	Typ	Max	Min	Typ	Max	
Supply Voltage	$+V_S$		2.2		30	2.2		24	V
Reference Voltage (Internal)	V_{REF}		1.29	1.31	1.33	1.24	1.31	1.38	V
Switch Current	I_{SW}	V_4 = 400 mV	100	200		100	200		mA
Supply Current	I_S	Measure at Pin 5 I_4 = 0		215	300		215	300	μA
Efficiency	ef			85			85		%
Line Regulation		0.5 V_O < V_S < V_O		0.04	0.2		0.04	0.5	% V_O
Load Regulation	L_I	V_S = +0.5 V_O, P_L = 150 mW		0.2	0.5		0.2	0.5	% V_O
Operating Frequency Range[1]	F_O		0.1	25	75	0.1	25	75	kHz
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	μA
Switch Leakage Current	I_{CO}	V_4 = 24V		0.01	5.0		0.01	5.0	μA
Supply Current (Disabled)	I_{SO}	$V_C \leq$ 200 mV		0.1	5.0		0.1	5.0	μA
Low Battery Bias Current	I_1	V_1 = 1.2V		0.7			0.7		μA
Capacitor Charging Current	I_{CX}			8.6			8.6		μA
Oscillator Frequency Tolerance				±10			±10		%
Capacitor Threshold Voltage +	$+V_{THX}$			1.4			1.4		V
Capacitor Threshold Voltage -	$-V_{THX}$			0.5			0.5		V
Feedback Input Current	I_{FB}	V_7 = 1.3V		0.1			0.1		μA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1500		500	1500		μA

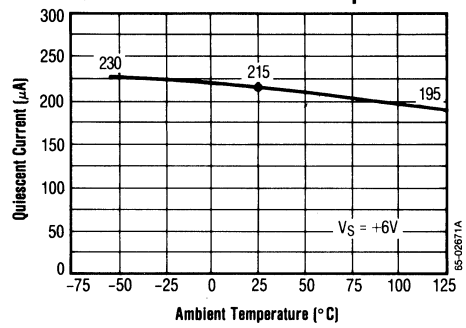
Note 1. Guaranteed by design.

Typical Performance Characteristics

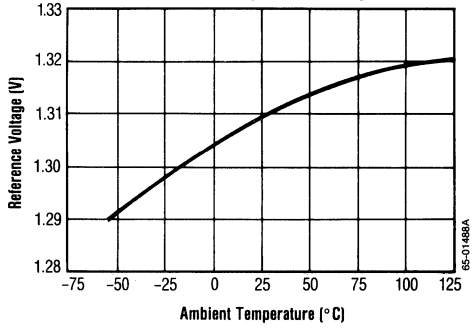
Minimum Supply Voltage vs. Temperature



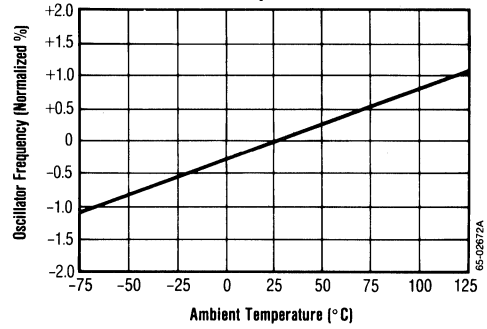
Quiescent Current vs. Temperature



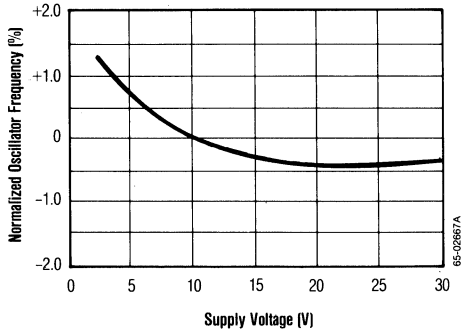
Reference Voltage vs. Temperature



Oscillator Frequency vs. Temperature



Oscillator Frequency vs. Supply Voltage



Principles of Operation

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up dc-to-dc converter (Figure 1).

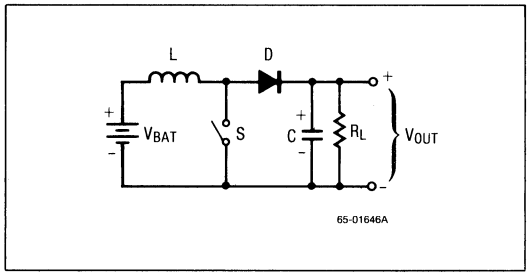


Figure 1. Simple Step-Up DC-to-DC Converter ($V_{OUT} > V_{BAT}$)

When switch S is closed the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{PEAK} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant dc voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete 4190 regulator a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in Figure 2. The ideal switch in the dc-to-dc converter diagram is replaced by an open collector NPN transistor Q1. C1 functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the 4190 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

At this point the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple dc-to-dc converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter this feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 3). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle, thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

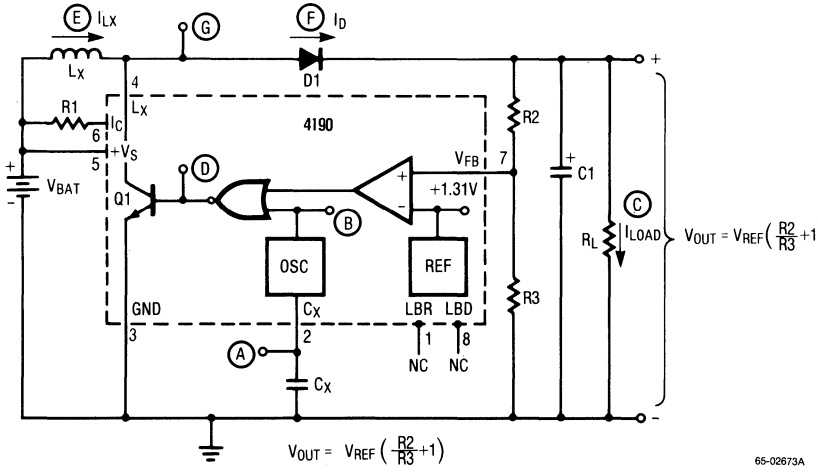


Figure 2. Minimum Step-Up Application

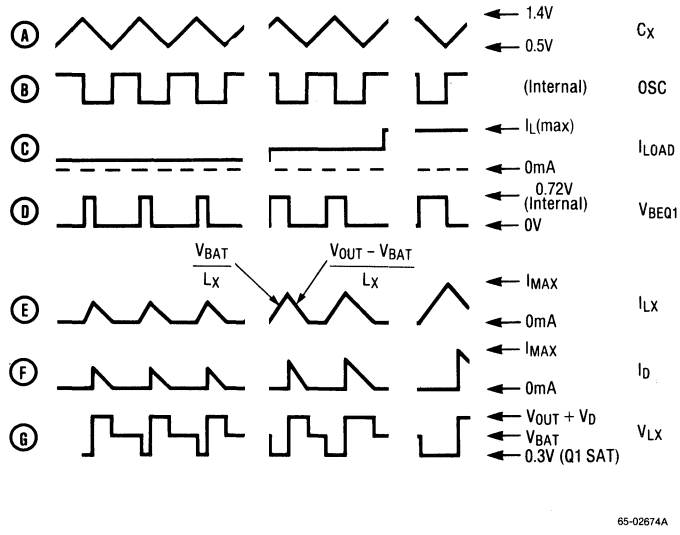


Figure 3. Step-Up Regulator Waveforms

The inductor value and oscillator frequency must be carefully tailored to the battery voltage, output current, and ripple requirements of the application (see Design Equations, page 10). If the inductor value is too high or the oscillator frequency is too high then the inductor current will never reach a value high enough to meet the load current drain and the output voltage will collapse. If the inductor value is too low or the oscillator frequency too low then the inductor current will build up too high, causing excessive output voltage ripple, or possibly over stressing the switch transistor, or possibly saturating the inductor.

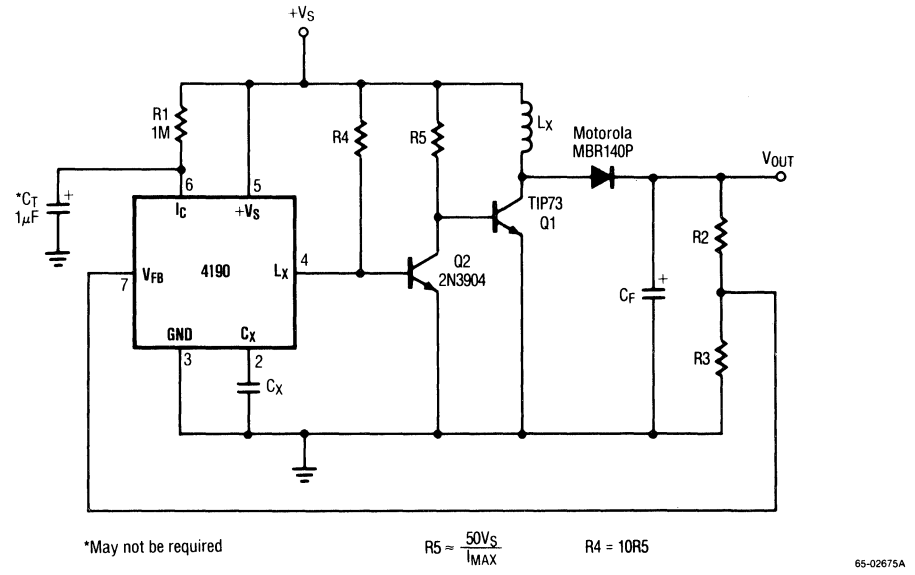


Figure 4. High Power Step-Up Application (up to 10W)

Simple Step-Down Converter

Figure 5 shows a simple step-down dc-to-dc converter with no feedback or control.

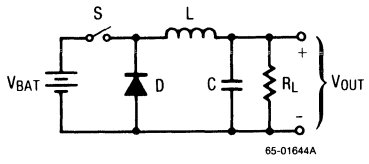


Figure 5. Simple Step-Down DC-to-DC Converter ($V_O \leq V_{BAT}$)

When S is closed the battery voltage minus the output voltage is applied across the inductor. All of the inductor current will flow into the load until the inductor current exceeds the load current. The excess current will then charge the capacitor and the output voltage will rise. When S is opened the voltage applied across the inductor will be reduced to V_{OUT} plus V_{DIODE}, and the inductor will discharge into the load. As in the step-up case, the average inductor current equals the load current. The maximum inductor current I_{MAX} will equal $(V_{BAT} - V_{OUT})/L_X$ times the maximum on time of the switch transistor. Current flows to the load during both half cycles of the oscillator.

Complete Step-Down Regulator

Most step-down applications are better served by the 4391 step-down and inverting switching regulator (refer to the 4391 data sheet). However, there is a range of load power for which the 4190 has an advantage over the 4391 in step-down applications. From approximately 500mW to 2W of load power, the 4190 step-down circuit of Figure 6 offers a lower component count and simpler circuit than the comparable 4391 circuit, particularly when stepping down a voltage greater than 30V.

Since the switch transistor in the 4190 is in parallel with the load a method must be used to convert it to a series connection. The circuit of Figure 7 accomplishes this. The 2N2907 replaces S of Figure 6, and R6 and R7 are added to provide the base drive to the 2N2907 in the correct polarity to operate the circuit properly.

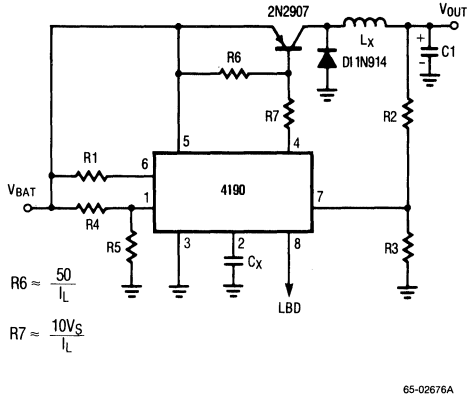


Figure 6. Complete Step-Down Regulator

Greater Than 30V Application

Adding a zener diode in series with the base of the 2N2907 allows the battery voltage to increase by the value of the zener, with only a slight decrease in efficiency. As an example, if a 24V zener is used, the maximum battery voltage can go to 48V* when using a 4190. Refer to Figure 7.

Note, however, that the addition of the zener diode will not alter the maximum change of supply. With a 24V zener the circuit will stop operating when the battery voltage drops below 24V + 2.2V = 26.2V.

*Maximum battery voltage is 54V when using RM4190 (30V + 24V).

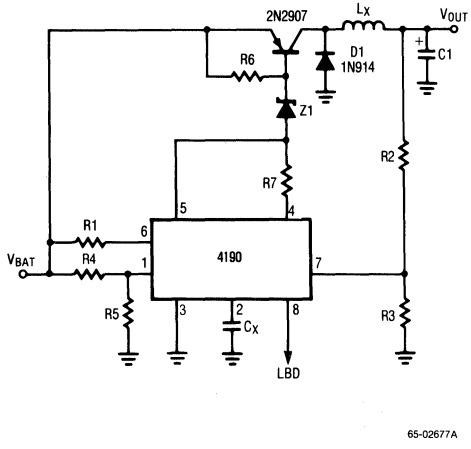


Figure 7. Stepping Down An Input Voltage Greater Than 30V

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±20% as a maximum change from the nominal oscillator frequency.

The worst-case conditions for calculating ability to supply load current are found at the minimum supply voltage; use $+V_S$ (min) to calculate the inductor value. Worst-case conditions for ripple are at $+V_S$ (max).

The value of the timing capacitor is set according to the following equation:

$$f_O\ (Hz) = \frac{2.4 \times 10^{-6}}{C_X}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 4. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Find a value for the start-up resistor R1:

$$R1 = \frac{V_S - 1.2V}{5\ \mu A}$$

Find a value for the feedback resistors R2 and R3:

$$R2 = \frac{V_{OUT} - 1.31V}{I_A}$$

$$R3 = \frac{1.31V}{I_A}$$

Where I_A is the feedback divider current (recommended value is between 50 µA and 100 µA).

Step-Up Design Procedure

1. Select an operating frequency and timing capacitor as shown above (10 kHz to 40 kHz is typical).
2. Find the maximum on time (add 5 µS for the turn-off base recombination delay of Q1):

$$T_{ON} = \frac{1}{2f_O} + 5\ \mu S$$

3. Calculate the peak inductor current I_{MAX} (if this value is greater than 375 mA, then an external power transistor must be used in place of Q1):

$$I_{MAX} = \left(\frac{V_{OUT} + V_D - V_S}{(f_O)\ T_{ON}\ [V_S - V_{SW}]}\right)\ 2I_L$$

where:
V_S = supply voltage
V_D = diode forward voltage
I_L = dc load current
V_{SW} = saturation voltage of Q1 (typ 0.5V)

4. Find an inductance value for L_X:

$$L_X\ (Henries) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right) T_{ON}$$

The inductor chosen must exhibit approximately this value at a current level equal to I_{MAX}.

5. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{T_{ON}\left(\frac{V_S\ I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

where V_R = ripple voltage (peak)

Step-Down Design Procedure

1. Select an operating frequency.
2. Determine the maximum on time (T_{ON}) as in the step-up design procedure.
3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(f_O)\ (T_{ON})\left(\frac{V_S - V_{OUT}}{V_{OUT} - V_D} + 1\right)}$$

4. Calculate L_X:

$$L_X = \left(\frac{V_S - V_{OUT}}{I_{MAX}}\right) T_{ON}$$

5. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{T_{ON}\left(\frac{[V_S - V_{OUT}]\, I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

Alternate Design Procedure

The design equations above will not work for certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, use the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example the inductor current will be continuous and the alternate procedure will be necessary.

1. Select an operating frequency (a value between 10 kHz and 40 kHz is typical).
2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.
3. Adjust the inductor value down until the desired output voltage is achieved, then go a little lower (approximately 20%) to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripple, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents [eff = $(V_{OUT})(I_{OUT})/(+V_S)(I_{SY})$ x 100%].
5. If the efficiency is poor, go back to (1) and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread boarding prototypes. Care must be taken to choose a permeable enough core to handle the magnetic flux produced at I_{MAX}; if the core saturates then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. An isolated ac current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 8). This level is determined by the +1.31V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

Where V_{TH} = Threshold Voltage for Detection

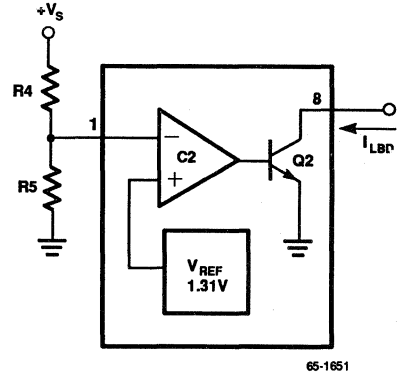


Figure 8. Low Battery Detector

When the battery voltage drops below this threshold Q2 will turn on and sink over 1500 μA typically. The low battery detector circuitry may also be used for other, less conventional applications (see Figures 14 and 15).

Bias Current Shutdown

The control current for the reference is an externally set by a resistor from the I_C pin to the battery. This current can vary from 1.0 μA to 50 μA without affecting the operation of the IC. Interrupting this current will disable the entire circuit, causing the output voltage to go to 0V for step-down applications, and reducing the supply current to less than 1.0 μA.

Automatic shutdown of the 4190 can be achieved using the circuit of Figure 9.

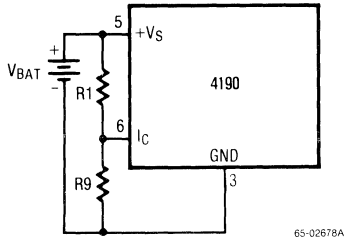


Figure 9. Simple Automatic Shutdown

A resistor is placed from the I_C pin to ground, creating a voltage divider. When the voltage at the I_C pin is less than 1.2V, the 4190 will begin to turn off. This scheme should only be used in limited temperature range applications since the "turn off" voltage at the I_C pin has a temperature coefficient of -4.0 mV/°C. At 25°C, typically 250 nA is the minimum current required by the I_C pin to sustain operation. A 5.0 μA voltage divider works well taking into account the sustaining current of 250 nA and a threshold voltage of 0.4V at turn off. As an example, if 3.0V is to be the turn off voltage, then R9 = 1.1/4.75 μA and R1 - (3.0 - 1.1) 5.0 μA or about 240 kΩ and 390 kΩ respectively. The tempco at the top of the divider will be -4.0 mV (R1 + R9)/R9 or -10.5 mV/°C, an acceptable number for many applications.

Another method of automatic shutdown without temperature limitations is the use of a zener diode in series with the I_C pin and set resistor. When the battery voltage falls below V_Z + 1.2V the circuit will start to shut down. With this connection and the low battery detector, the application can be designed to signal a display when the battery voltage has dropped to the first programmed level, then shut itself off as the battery reaches the zener threshold.

The set current can also be turned off by forcing the I_C pin to 0.2V or less using an external transistor or mechanical switch. An example of this is shown in Figure 10.

In this circuit an external control voltage is used to determine the operating state of the 4190. If the control voltage V_C is a logic 1 at the input of the 4021 (CMOS Triple NOR Gate), the voltage at the I_C pin will be less than 0.5V forcing the 4190 off (<0.1 μA I_{CC}). both the 2N3904 and 2N2907 will be off insuring long shelf for the battery since less than 1.0 μA is drawn by the circuit.

When V_C goes to a logic 0, 2.0 μA is forced into the I_C pin through the 2.2 MΩ resistor and the NOR gate, and at the same time the 2N3904 and 2N2907 turn on, connecting the battery to the load.

As long as V_C remains low the circuit will regulate the output to 5.0V. This type of circuit is used to back up the main supply voltage when line interruptions occur, a particularly useful feature when using volatile memory systems.

Typical Step-Up Application

Figure 11 shows a common application: a circuit to extend the lifetime of a 9.0V battery. The regulator remains in its quiescent state (drawing only 215 μA) until the battery voltage decays below 7.5V, at which time it will start to switch and regulate the output at 7.0V until the battery falls below 2.2V.

If this circuit operates at tis typical efficiency of 80%, with an output current of 10 mA, at 5.0V battery voltage, then the average input current will be $I_{IN} = (V_{OUT} \times I_L) \div (V_{BAT}) \times e_f)$ or 7.0V x 10 mA) ÷ (5.0V x 0.8) = 17.5 mA.

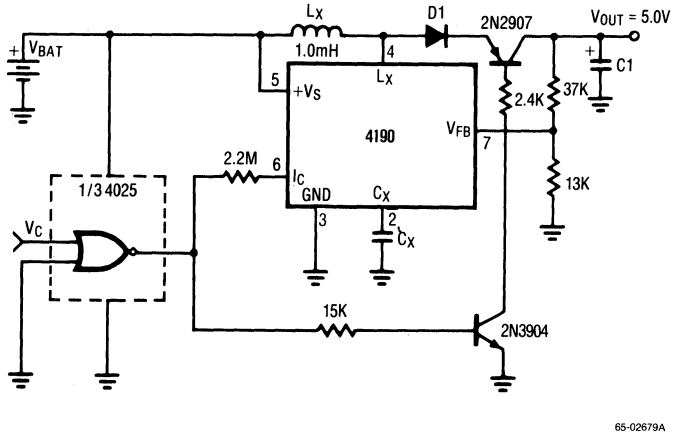


Figure 10. Battery Back-Up Circuit

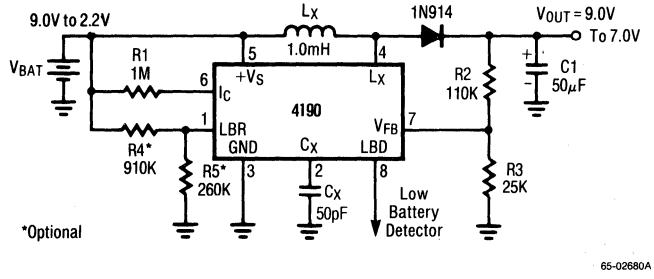


Figure 11. Typical Application: 9.0V Battery Life Extender

Bootstrapped Operation

In step-up applications, power to the 4190 can be derived from the output voltage by connecting the $+V_S$ pin and the top of R1 to the output voltage (Figure 12).

One requirement is that the battery voltage must be greater than 3.0V when the circuit is energized or else there will not be enough voltage at pin 5 to start up the IC. The big advantage of this circuit is the ability to operate down to a discharged battery voltage of 1.0V.

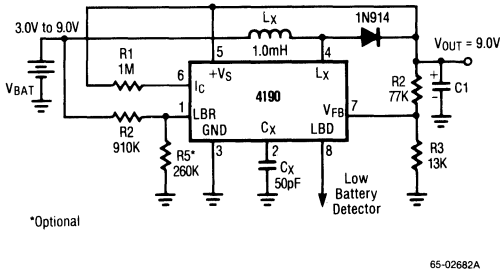


Figure 12. Bootstrapped Operation

Buck-Boost Application

A disadvantage of the standard step-up and step-down circuits is the limitation of the input voltage range; for a step-up circuit, the battery voltage must always be less than the programmed output voltage, and for a step-down circuit, the battery voltage must always be greater than the output voltage. The following circuit eliminates this disadvantage, allowing a battery voltage above the programmed output voltage to decay to well below the output voltage (see Figure 13).

The circuit operation is similar to the step-up circuit operation, except that both terminals of the inductor are connected to switch transistors. This switching method allows the inductor to be disconnected from the battery during the time the inductor is being discharged. A new discharge path is provided by D1, allowing the inductor to be referenced to ground and independent of the battery voltage. The efficiency of this circuit will be reduced to 55–60% by losses in the extra switch transistor and diode. Efficiency can be improved by choosing transistors with low saturation voltages and by using power Schottky diodes such as Motorola's MBR030.

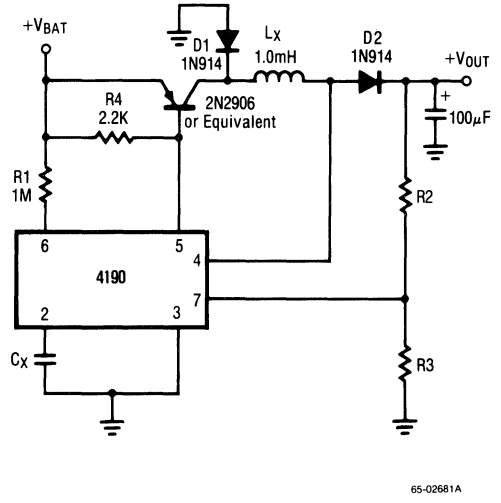


Figure 13. Buck Boost Circuit (V_{BAT} > or < V_{OUT})

Voltage Dependent Oscillator

The 4190's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the load current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This tradeoff between load current capability and output ripple can be improved with the circuit connection shown in Figure 14. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-programmed threshold is reached.

The threshold is programmed exactly as the normal low battery detector connection:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

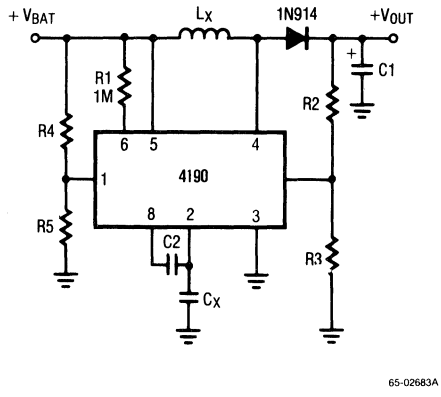


Figure 14. Step-Up Regulator With Voltage-Dependent Oscillator

When the battery voltage reaches this threshold the comparator will turn on the open collector transistor at pin 8, effectively putting C2 in parallel with C_X. This added capacitance will reduce the oscillator frequency according to the following equation:

$$F_O \approx \frac{2.4 \times 10^{-6}}{C_X + C2}$$

Where C is in pF and F_O is in Hz.

Component values for a typical application might be R2 = 330 kΩ, R5 = 150 kΩ, C_X = 100 pF, and C2 = 100 pF. These values would set the threshold voltage at 4.1V and change the operating frequency from 48 kHz to 24 kHz. Note that this technique may be used for step-up, step-down, or inverting applications.

Compensation

When large values (> 50 kΩ) are used for the voltage setting resistors, R2 and R3 of Figure 2, stray capacitance at the V_{FB} input can add a lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100 pF to 10 nF in parallel with R2 in Figure 2.

Short Circuit Protection

One disadvantage of the simple application circuits is their lack of short circuit protection, especially for the step-up circuit, which has a very low resistance path for current flow from the input to the output. A current limiting circuit which senses the output voltage and shuts down the 4190 if the output voltage drops too low can be built using the low battery detector circuitry. The low battery detector is connected to sense the output voltage and will shut off the oscillator by forcing pin 2 low if the output voltage drops. Figure 15 shows a schematic of a step-down regulator with this connection.

R3 and R4 set the output voltage, as in the circuit of Figure 2. Choose resistor values so R5 = R3 and R4 = R2, and make R8 25 to 35 times higher than R3. When the output is shorted, the open collector transistor at pin 8 will force pin 2 low and shut off the oscillator and therefore shut off the external switch transistor. The regulator will then remain in a low current off condition until power is removed and reapplied. C2 provides momentary current to ensure proper start up. This scheme will not work with the simple step-up regulator, but will work with the boost-buck converter, providing short circuit protection in both step-up and step-down modes.

4190/4391 ± Power Supply

A positive and negative dual tracking power supply using a step-up 4190 and an inverting 4391 is shown in Figure 16. The inductor and capacitor values were chosen to achieve the highest practical output currents from a +12V battery, as it decays, while keeping the output voltage ripple under 100mV$_{pp}$ at ±15V output.

The circuit may be adapted to other voltages and currents, but note that the 4190 is step-up, so V_{OUT} must be greater than V_{BAT}.

The output voltages may both be trimmed by adjusting a single resistor value (R3 or R4), because the reference for the negative output is derived from +V_{OUT}. This connection also allows the output voltages to track each other with changes in temperature and line voltage.

The timing capacitors are set up exactly as in the voltage dependent oscillator application of Figure 16. The values of R2, R5, C6, and C4 that are given were chosen to optimize for the +12V battery conditions, setting the threshold for oscillator frequency change at V_{BAT} = +8.5V.

As given, this power supply is capable of delivering +45 mA and -15 mA with regulation, until the battery decays below 5.0V.

For information on adjusting the 4391 to meet a specific application refer to the Raytheon 4391 data sheet.

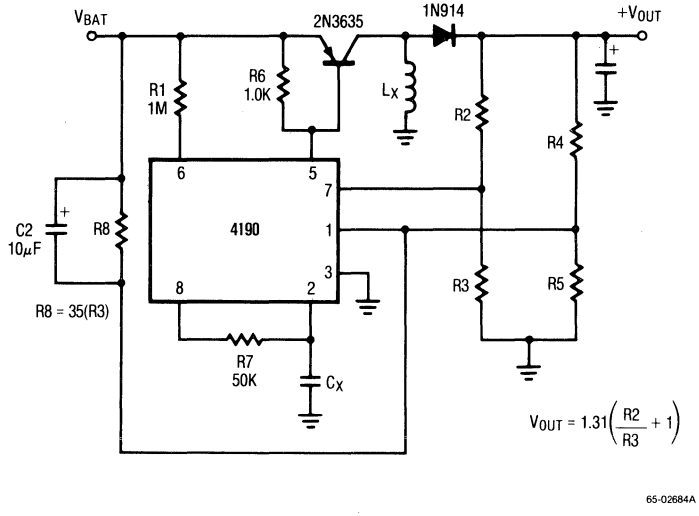


Figure 15. Step-Down Regulator With Short Circuit Protection

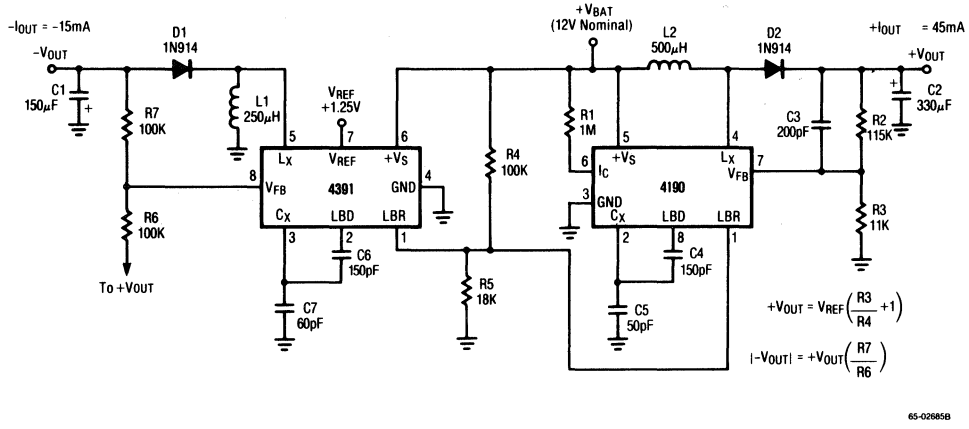


Figure 16. RC4190/4391 Power Supply (±15V With Values Given)

Negative Input, Negative Output Step-Up Regulator

In the circuit of Figure 17, a bootstrap arrangement of supply and ground pins helps generate an output voltage more negative than the input voltage. On power-up, the output filter capacitor (C_F) will charge through D2 and L_X. When the voltage goes below -2.4V, the 4190 begins switching and charging C_F. The output will regulate at a value equal to the reference voltage (1.31V) plus the zener voltage of D1. RZ sets the value of zener current, stabilized at 1.31V/R2.

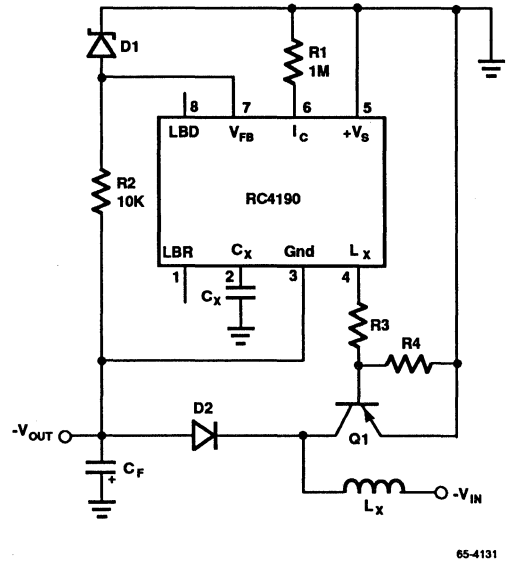
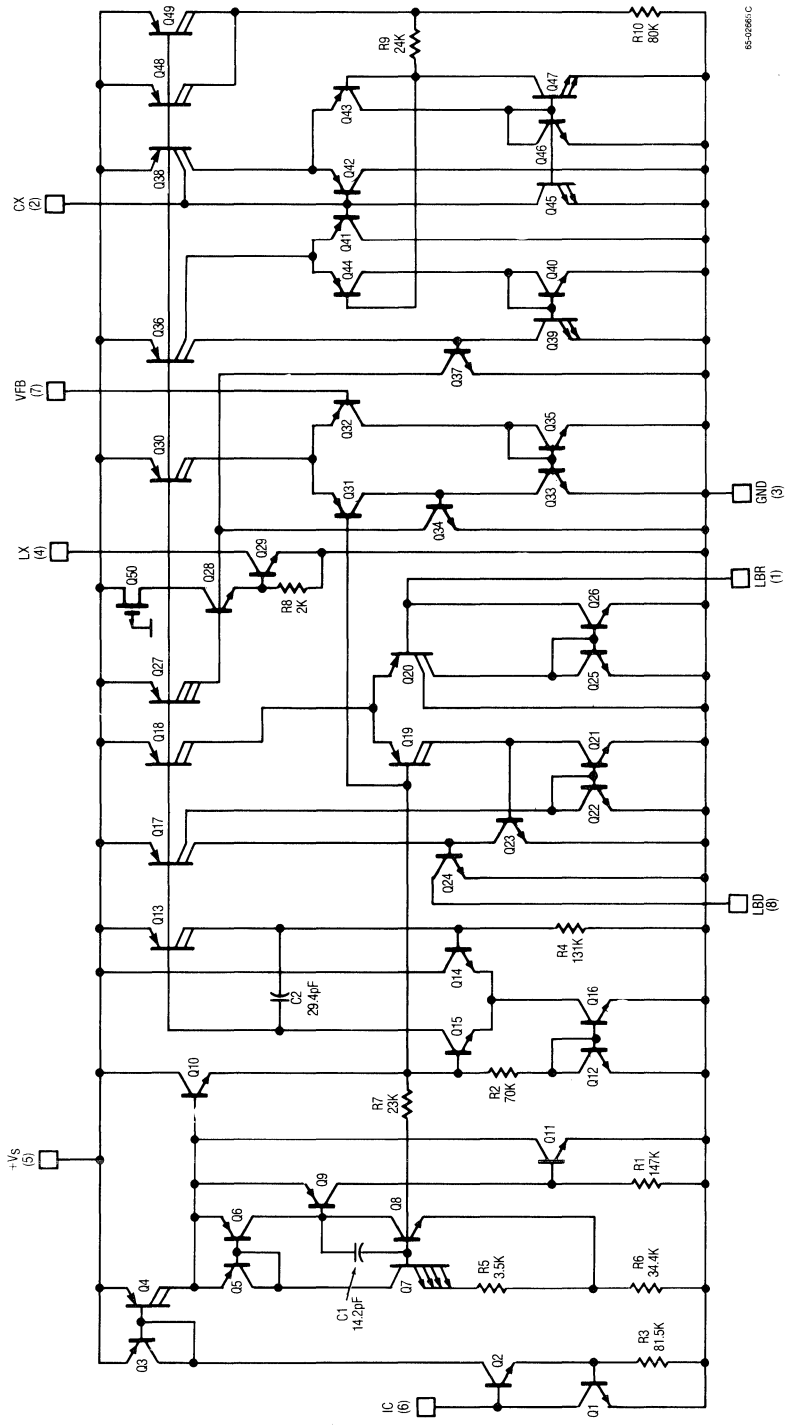
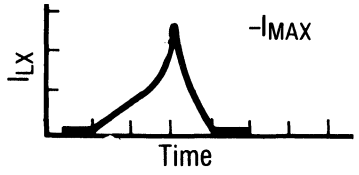
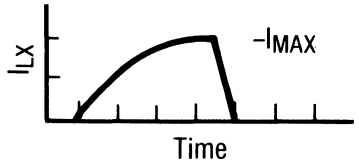
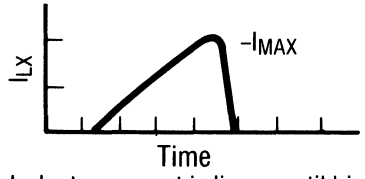


Figure 17. Negative Input, Negative Output Step-Up Regulator

Schematic Diagram



Troubleshooting Chart

Symptom	Possible Problems
Draws excessive supply current on start-up.	Battery not "stiff" — inadequate supply bypass capacitor. Inductance value too low. Operating frequency too low.
Output voltage is low.	Inductance value too high for F_O or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
Lx pin appears noisy — scope will not synchronize.	Normal operating condition.
 Inductor current shows nonlinear waveform.	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
 Inductor current shows nonlinear waveform.	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
 Inductor current is linear until high current is reached.	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating. Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high SAT). High series resistance. Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback capacitor from V_{OUT} to pin 7 (100 to 1000pF).

Background Information

During the past several years there have been various switching regulator ICs introduced by many manufacturers, all of which attended to the same market, namely controllers for use in power supplies delivering greater than 10W of DC power. Raytheon felt there was another area which could use a switching regulator to even more advantage the area of battery powered equipment. Battery powered systems have problems peculiar unto themselves: changes in supply voltage, space considerations, battery life and usually cost. The 4190 was designed with each of these in mind.

The 4190 was partitioned to work in an eight pin package, making it smaller than other controllers which go into 14 and 16 pin packages.

Battery powered applications require the load as seen by the battery to be as small as possible to extend battery life. To this end, the quiescent current of the 4190 is 15 to 100 times less than controllers designed for nonbattery applications. At the same time the switch transistor can sink 200mA at 0.4V, comparable to or better than higher powered controllers. As an example, the 4190 configured in the step-up mode can supply 5.0V at 40mA output with an input of 3.0V.

Cost is usually a primary consideration in battery powered systems. The 4190, guaranteed to work down to 2.2V, can save the designer and end user money as well because battery costs decrease as the number of cells needed goes down.

RC4191/4192/4193 Micropower Switching Regulators

Features

- High efficiency — 80% typical
- Low quiescent current — 215 μA
- Adjustable output — 2.2V to 30V
- High switch current — 150 mA
- Bandgap reference — 1.31V
- Remote shutdown capability
- Low battery detection circuitry
- Low component count
- Small 8-lead package

Description

Not recommended for new designs. Refer to RC4190 Data Sheet. The RC4193 series of monolithic ICs are low power switch mode regulators intended for miniature power supply applications. These dc-to-dc converter ICs provide all of the active functions needed to create supplies for micropower circuits (load power up to 400 mW, or up to 10W with external power transistor). Contained internally are an oscillator, switch, reference, comparator, and logic, plus a discharged battery detection circuit.

Application areas include on-card circuits where a non-standard voltage supply is needed, or in battery operated instruments where a 4193 can be used to extend battery lifetime.

These regulators can achieve up to 80% efficiency in most applications while operating over a wide supply voltage range, 2.2V to 30V, at a very low quiescent current drain of 215 μA.

The standard application circuit requires just seven external components for step-up operation: an inductor, a steering diode, three resistors, a low value timing capacitor, and an electrolytic filter capacitor. The combination of simple application circuit, low supply current, and small package make the 4193 adaptable to a wide range of miniature power supply applications.

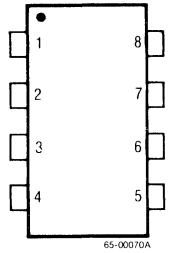
The 4193 is most suited for single ended step-up circuits because the internal switch transistor is referenced to ground. It is complemented by Raytheon's other micropower switching regulator, the 4391, which is dedicated to step-down and negative output (inverting) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the 4391 data sheet for step-down and inverting applications.

The 4191/92/93 series of micropower switching regulators consists of three devices, each with slightly different specifications. The 4191 has a 1.5% maximum output voltage tolerance, 0.2% maximum line regulation, and operation to 30V. The 4192 has a 3.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 30V. The 4193 has a 5.0% maximum output voltage tolerance, 0.5% maximum line regulation, and operation to 24V. Other specifications are identical for the 4191, 4192 and 4193. Each type is available in commercial, industrial, and military temperature ranges, and in plastic and ceramic DIPs.

With some optional external components the application can be designed to signal a display when the battery has decayed below a predetermined level, or designed to signal a display at one level and then shut itself off after the battery decays to a second level. See the applications section for these and other unique circuits.

Connection Information

8-Lead
Dual In-Line Package
(Top View)



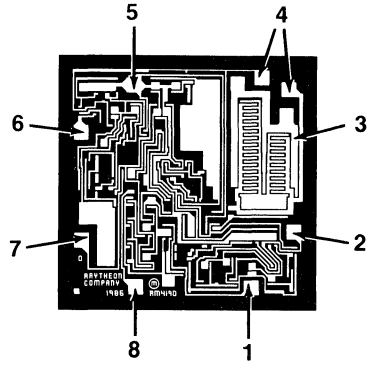
Pin	Function
1	Low Battery (Set) Resistor (LBR)
2	Timing Capacitor (C_X)
3	External Inductor (L_X)
4	Ground
5	+Supply Voltage ($+V_S$)
6	Reference Set Current (I_C)
7	Feedback Voltage (V_{FB})
8	Low Battery Detector Output (LBD)

Ordering Information

Part Number	Package	Operating Temperature Range
RC4191N	N	0°C to +70°C
RC4192N	N	0°C to +70°C
RC4193N	N	0°C to +70°C
RV4191N	N	-25°C to +85°C
RV4192N	N	-25°C to +85°C
RV4193N	N	-25°C to +85°C
RM4191D	D	-55°C to +125°C
RM4192D	D	-55°C to +125°C
RM4193D	D	-55°C to +125°C
RM4191D/883B	D	-55°C to +125°C
RM4192D/883B	D	-55°C to +125°C
RM4193D/883B	D	-55°C to +125°C

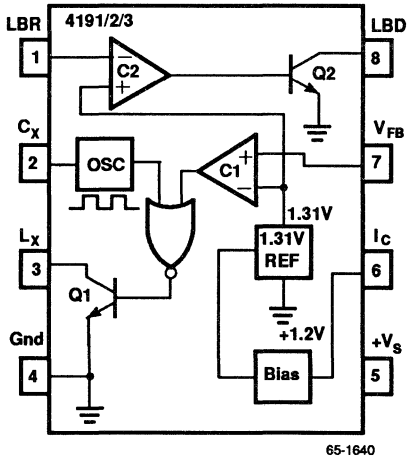
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Mask Pattern



Die Size: 66 x 67 mils
Min. Pad Dimensions: 4 x 4 mils 65-01482A

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (Without External Series Pass Transistor
- 4191, 4192 ..... +30V
- 4193 ..... +24V

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- RM4191/2/3 ..... -55°C to +125°C
- RV4191/2/3 ..... -25°C to +85°C
- RC4191/2/3 ..... 0°C to +70°C

Switch Current ..... 375 mA Peak

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	833mW
Therm. Res. θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Electrical Characteristics (V_S = +6.0V, I_C = 5.0 μA, and T_A = +25°C unless otherwise noted)

Parameters	Symbol	Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Supply Voltage	$+V_S$		2.2		30	2.2		30	2.2		24	V
Reference Voltage (Internal)	V_{REF}		1.29	1.31	1.33	1.27	1.31	1.35	1.24	1.31	1.38	V
Switch Current	I_{SW}	V_3 = 400mV	100	200		100	200		100	200		mA
Supply Current	I_S	Measure at Pin 5 $I_3 = 0$		215	300		215	300		215	300	μA
Efficiency	ef			85			85			85		%
Line Regulation		$0.5\ V_O < V_S < V_O$		0.04	0.2		0.04	0.5		0.04	0.5	% V_O
Load Regulation	L_I	V_S = +0.5 V_O, P_L = 150mW		0.2	0.5		0.2	0.5		0.2	0.5	% V_O
Operating Frequency Range[1]	F_O		0.1	25	75	0.1	25	75	0.1	25	75	kHz
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	μA
Switch Leakage Current	I_{CO}	V_3 = 24V		0.01	5.0		0.01	5.0		0.01	5.0	μA
Supply Current (Disabled)	I_{SO}	$V_C \leq 200$ mV		0.1	5.0		0.1	5.0		0.1	5.0	μA
Low Battery Bias Current	I_1	V_1 = 1.2V		0.7			0.7			0.7		μA
Capacitor Charging Current	I_{CX}			8.6			8.6			8.6		μA
Oscillator Frequency Tolerance				±10						±10		%

Note 1: Guaranteed by design.

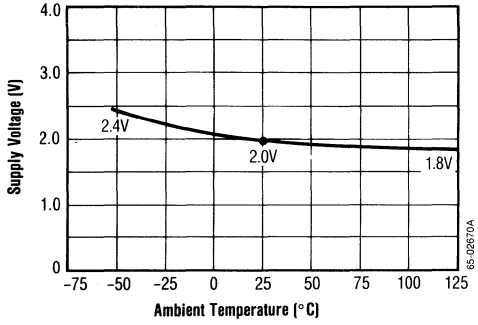
Electrical Characteristics (Continued)

(V_S = +6.0V, I_C = 5.0 μA, and T_A = +25°C unless otherwise noted)

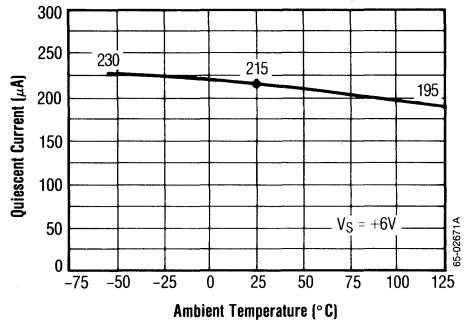
Parameters	Symbol	Conditions	4191			4192			4193			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Capacitor Threshold Voltage +	$+V_{THX}$			1.4			1.4			1.4		V
Capacitor Threshold Voltage -	$-V_{THX}$			0.5			0.5			0.5		V
Feedback Input Current	I_{FB}	V_7 = 1.3V		0.1			0.1			0.1		μA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1500		500	1500		500	1500		μA
($+V_S$ = 6.0V, I_C = 5.0 μA, unless otherwise noted, over the full operating temperature range)												
Supply Voltage	$+V_S$		2.6		30	2.6		30	2.6		24	V
Reference Voltage (Internal)	V_{REF}		1.25	1.31	1.37	1.23	1.31	1.39	1.20	1.31	1.42	V
Supply Current	I_S	Measure at Pin 5 I_3 = 0		225	350		225	350		225	350	μA
Line Regulation		0.5 V_O < $+V_S$ < V_O		0.2	0.5		0.5	1.0		0.5	1.0	% V_O
Load Regulation	L_I	$+V_S$ = 0.5 V_O, P_L = 150 mW		0.5	1.0		0.5	1.0		0.5	1.0	% V_O
Reference Set Current	I_C		1.0	5.0	50	1.0	5.0	50	1.0	5.0	50	μA
Switch Leakage Current	I_{CO}	V_3 = 24V			30			30			30	μA
Supply Current (Disabled)	I_{SO}	V_C < 200 mV			30			30			30	μA
Low Battery Output Current	I_{LBD}	V_8 = 0.4V, V_1 = 1.1V	500	1200		500	1200		500	1200		μA
Oscillator Frequency Temperature Drift				±200			±200			±200		ppm/°C

Typical Performance Characteristics

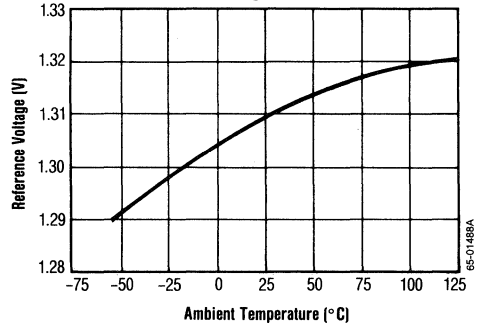
Minimum Supply Voltage vs. Temperature



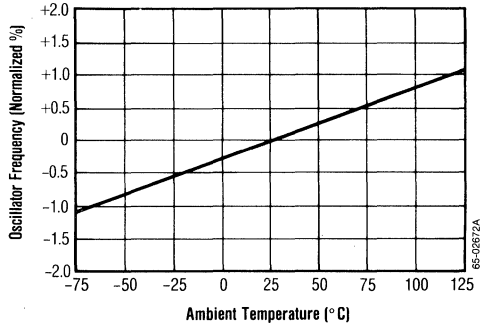
Quiescent Current vs. Temperature



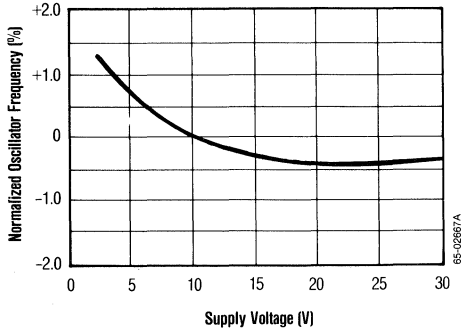
Reference Voltage vs. Temperature



Oscillator Frequency vs. Temperature



Oscillator Frequency vs. Supply Voltage



Principles of Operation

Simple Step-Up Converter

The most common application, the step-up regulator, is derived from a simple step-up DC-to-DC converter (Figure 1).

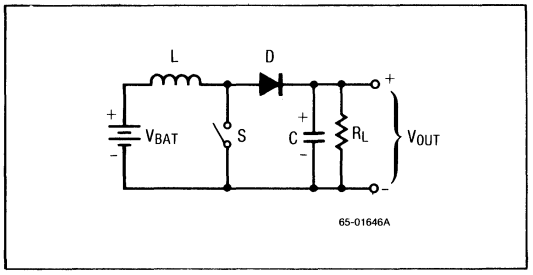


Figure 1. Simple Step-Up DC-to-DC Converter ($V_{OUT} > V_{BAT}$)

When switch S is closed the battery voltage is applied across the inductor L. Charging current flows through the inductor, building up a magnetic field, increasing as the switch is held closed. While the switch is closed, the diode D is reverse biased (open circuit) and current is supplied to the load by the capacitor C. Until the switch is opened the inductor current will increase linearly to a maximum value determined by the battery voltage, inductor value, and the amount of time the switch is held closed ($I_{PEAK} = V_{BAT}/L \times T_{ON}$). When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a discharge current which flows through the inductor in the same direction as the charging current. Because there is no path for current to flow through the switch, the current must flow through the diode to supply the load and charge the output capacitor.

If the switch is opened and closed repeatedly, at a rate much greater than the time constant of the output RC, then a constant DC voltage will be produced at the output.

An output voltage higher than the input voltage is possible because of the high voltage produced by a rapid change of current in the inductor. When the switch is opened the inductor voltage will instantly rise high enough to forward bias the diode, to $V_{OUT} + V_D$.

In the complete 4193 regulator a feedback control system adjusts the on time of the switch, controlling the level of inductor current, so that the average inductor discharge current equals the load current, thus regulating the output voltage.

Complete Step-Up Regulator

A complete schematic of the minimum step-up application is shown in Figure 2. The ideal switch in the DC-to-DC converter diagram is replaced by an open collector NPN transistor Q1. C1 functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the current in R1 supplies bias current to pin 6 (I_C). This current is stabilized by a unity gain current source amplifier and then used as bias current for the 1.31V bandgap reference. A very stable bias current generated by the bandgap is mirrored and used to bias the remainder of the chip. At the same time the 4193 is starting up, current will flow through the inductor and the diode to charge the output capacitor to $V_{BAT} - V_D$.

At this point the feedback (pin 7) senses that the output voltage is too low, by comparing a division of the output voltage (set by the ratio of R2 to R3) to the +1.31V reference. If the output voltage is too low then the comparator output changes to a logical zero. The NOR gate then effectively ANDs the oscillator square wave with the comparator signal; if the comparator output is zero AND the oscillator output is low, then the NOR gate output is high and the switch transistor will be forced on. When the oscillator goes high again the NOR gate output goes low and the switch transistor will turn off. This turning on and off of the switch transistor performs the same function that opening and closing the switch in the simple DC-to-DC converter does; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time.

The comparator will continue to allow the oscillator to turn the switch on and off until enough charge has been delivered to the capacitor to raise the feedback voltage above 1.31V.

Thereafter this feedback system will vary the duration of the on time in response to changes in load current or battery voltage (see Figure 3). If the load current increases (waveform C), then the transistor will remain on (waveform D) for a longer portion of the oscillator cycle, thus allowing the inductor current (waveform E) to build up to a higher peak value. The duty cycle of the switch transistor varies in response to changes in load and line.

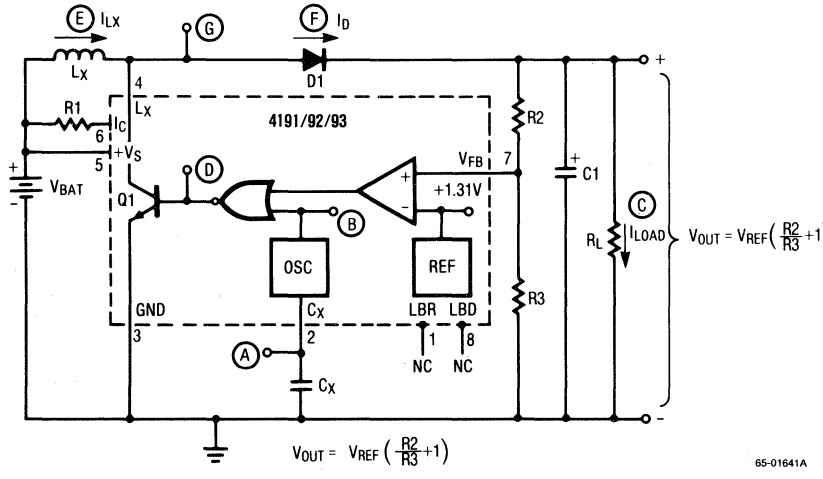


Figure 2. Minimum Step-Up Application

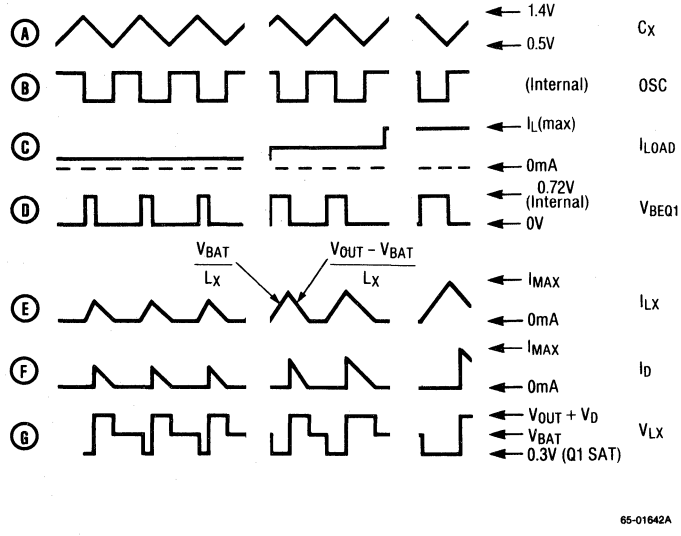


Figure 3. Step-Up Regulator Waveforms

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±20% as a maximum change from the nominal oscillator frequency.

The value of the timing capacitor is set according to the following equation:

$$f_O\ (Hz) = \frac{2.4 \times 10^{-6}}{C_X}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 3. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Find a value for the start-up resistor R1:

$$R1 = \frac{V_S - 1.2V}{5\mu A}$$

Find a value for the feedback resistors R2 and R3:

$$R2 = \frac{V_{OUT} - 1.31V}{I_A}$$

$$R3 = \frac{1.31V}{I_A}$$

Where I_A is the feedback divider current (recommended value is between 50μA and 100μA).

Step-Up Design Procedure

1. Select an operating frequency and timing capacitor as shown above (10kHz to 40kHz is typical).
2. Find the maximum on time (add 5μS for the turn-off base recombination delay of Q1):

$$T_{ON} = \frac{1}{2f_O} + 5\mu S$$

3. Calculate the peak inductor current I_{MAX} (if this value is greater than 375mA, then an external power transistor must be used in place of Q1):

$$I_{MAX} = \left(\frac{V_{OUT} + V_D - V_S}{(f_O)\ T_{ON}\ [V_S - V_{SW}]}\right) 2I_L$$

Where:

V_S = Supply Voltage
V_D = Diode Forward Voltage
I_L = DC Load Current
V_{SW} = Saturation Voltage of Q1 (typically 0.5V)

4. Find an inductance value for L_X:

$$L_X\ (Henries) = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right) T_{ON}$$

The inductor chosen must exhibit approximately this value at a current level equal to I_{MAX}.

5. Calculate a value for the output filter capacitor:

$$C_F(\mu F) = \frac{T_{ON}\left(\frac{V_S\ I_{MAX}}{V_{OUT}}\right) + I_L}{V_R}$$

Where V_R = Ripple Voltage (peak)

Step-Down Design Procedure

1. Select an operating frequency.
2. Determine the maximum on time (T_{ON}) as in the step-up design procedure.
3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(f_O)\ (T_{ON})\left(\frac{V_S - V_{OUT}}{V_{OUT} - V_D} + 1\right)}$$

4. Calculate L_X:

$$L_X = \left(\frac{V_S - V_{OUT}}{I_{MAX}}\right) T_{ON}$$

5. Calculate a value for the output filter capacitor:

$$C_{F(\mu F)} = \frac{T_{ON}\left(\frac{[V_S - V_{OUT}]\, I_{MAX}}{V_{OUT}} + I_L\right)}{V_R}$$

Alternate Design Procedure

The design equations above will not work for certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, use the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example the inductor current will be continuous and the alternate procedure will be necessary.

1. Select an operating frequency (a value between 10kHz and 40kHz is typical).
2. Build the circuit and apply the worst case conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.
3. Adjust the inductor value down until the desired output voltage is achieved, then go a little lower (approximately 20%) to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripple, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents (eff = $(V_{OUT})(I_{OUT})/(+V_S)(I_{SY})$ x 100%).
5. If the efficiency is poor, go back to (1) and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread boarding prototypes. Care must be taken to choose a permeable enough core to handle the magnetic flux produced at I_{MAX}; if the core saturates then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 8). This level is determined by the +1.31V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R5} + 1\right)$$

Where V_{TH} = Threshold Voltage for Detection

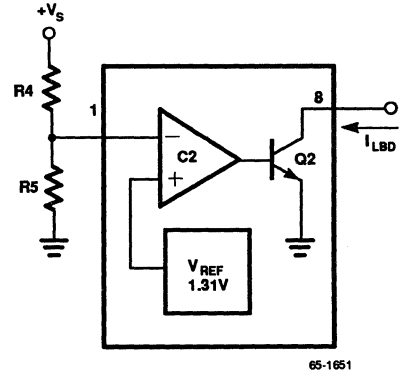
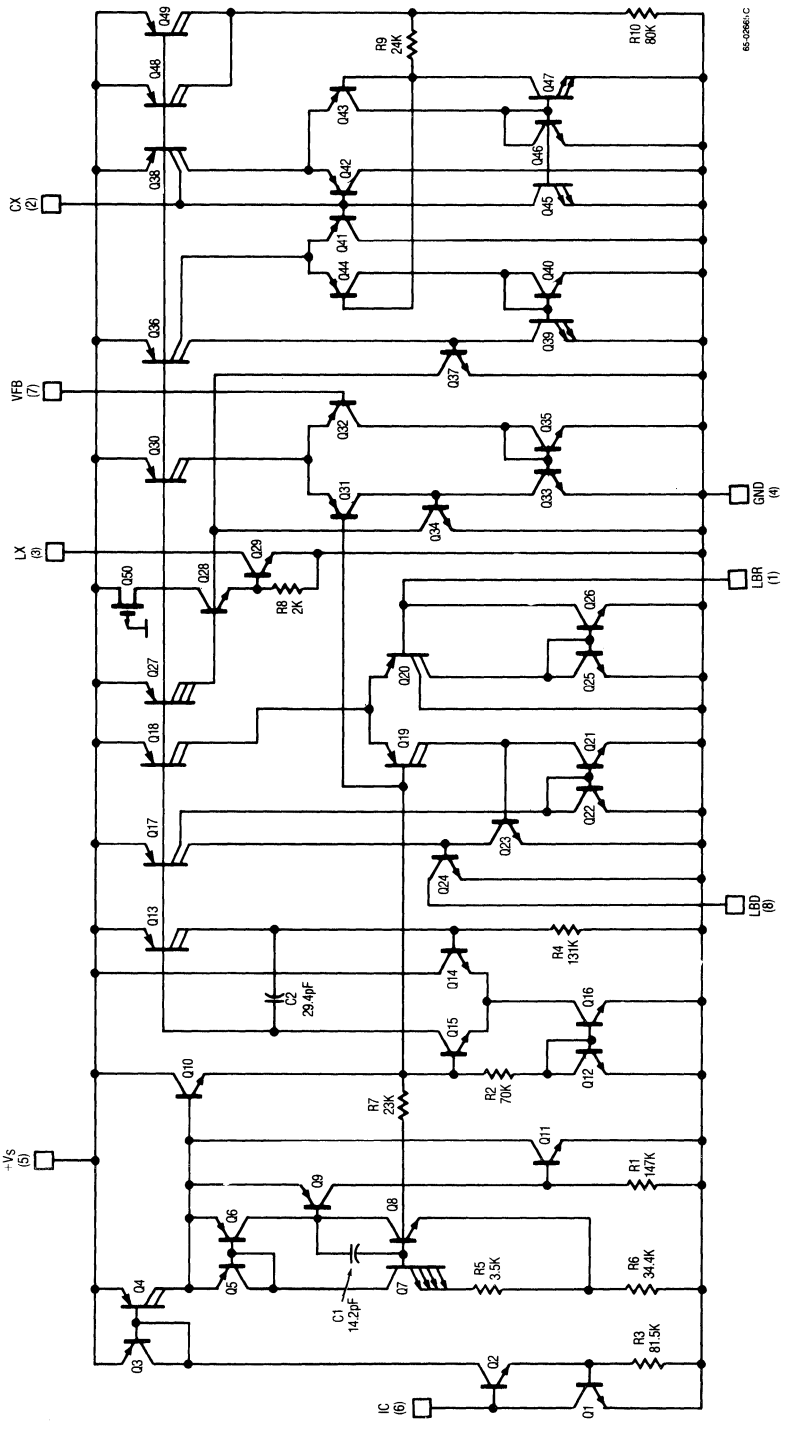


Figure 8. Low Battery Detector

Schematic Diagram



RC4292 Negative Switch Mode Power SupplyController

Features

- Converts a negative voltage into positive and/or negative voltages
- Wide application voltage range: -20V minimum, -120V maximum
- High efficiency: 70% typical
- Adjustable output voltage
- Accurate oscillator frequency: ±10%
- Wide frequency range: 20 kHz to 100 kHz
- Bandgap voltage reference; 50 ppm/°C
- Good line regulation: 0.1%/V
- PWM feedback circuitry
- Short circuit protection
- Soft start
- 8-lead mini DIP
- Load power up to 10W
- Undervoltage lockout

Applications

- Small power supplies
- Local on-card regulators
- Telephone peripheral equipment
- Converts -48V off-hook voltage
- Battery operated equipment

Description

The RC4292 is a monolithic IC containing all the high level functional blocks required to build small power supplies. Although designed specifically for converting -48V off-hook telephone power at PBX and branch office exchanges, this IC is versatile and can be used for a variety of DC-to-DC converter applications, such as on-card regulators and battery operated equipment. The RC4292 controller IC interfaces with a transistor which serves as the power switch. A 350 mA output current drives this power switch transistor, which in turn controls the current in primary of a transformer. Passive components are used to steer and filter the transformer current, set the output voltage, set the level of current limiting, and determine the free-running oscillator frequency.

Contained internally are seven major circuit functions: temperature stabilized voltage reference, error amplifier, temperature stabilized oscillator, current comparator, PWM control flip-flop and logic, shunt regulator, and an output driver to interface with the external transistor. The combination of these elements with a simple application circuit yields a compact and efficient power supply. The high efficiency, low quiescent current, small size, and wide input voltage range of the 4292 make it ideal for telephone peripherals and also many other negative input switch mode regulator applications.

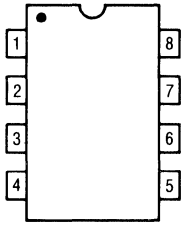
Ordering Information

Part Number	Package	Operating Temperature Range
RC4292N	N	0°C to +70°C
RM4292D	D	-55°C to +125°C

Notes:
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

8-Lead Dual In-Line Package
(Top View)



65-00070A

Pin	Function
1	CX — Timing Capacitor
2	-VFB — Error Amp Input
3	+VFB — Error Amp Input
4	V_{REF} — Reference Voltage
5	$-V_S$ — Negative Shunt
6	V_{DRIVE} — Output
7	I_{FB} — Current Limit Feedback
8	GND — Ground

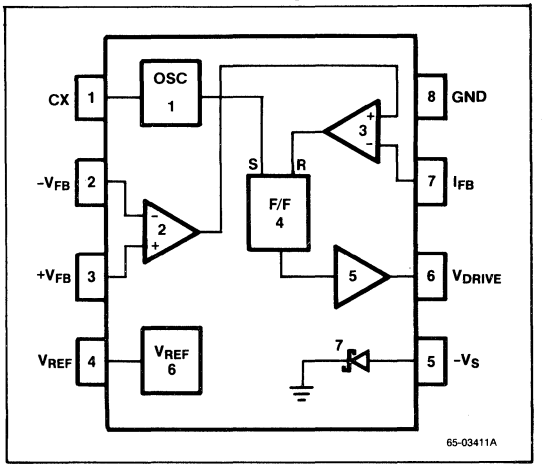
Absolute Maximum Ratings

Internal Power Dissipation ..... 750 mW
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(60 Sec) ..... +300°C
Output Drive Current ..... 750 mA
Shunt Current ..... 20 mA
V_{DRIVE} Voltage ..... -17V to +1.0V

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	+125°C	+175°C
Max. P_D T_A < 50°C	468mW	833mW
Therm. Res. θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C

Functional Block Diagram



65-03411A

Description of Functional Blocks

① **Oscillator** — The oscillator generates a time base for the V_{DRIVE} pulse. The frequency of oscillation is set by a low-value external capacitor connected between C_X and ground.

② **Error Amplifier** — Here the feedback signals $+V_{FB}$ and $-V_{FB}$ are compared, and the error amplifier output generates an error signal proportional to the input difference.

③ **Current Comparator** — This circuit compares the output of the error amplifier to a signal proportional to the current in the primary of the transformer (derived via a low value resistor in series with the transformer). If the I_{FB} signal is greater than the error signal, the control F/F is reset and the external power transistor will turn off.

④ **Control F/F** — The control F/F ensures that the external power transistor receives only one pulse for each oscillator cycle.

⑤ **Output Driver** — This circuit amplifies the control F/F output and provides a fast switching signal to drive the gate of an external power MOSFET or BJT.

⑥ **Voltage Reference** — Generates a voltage reference (-5.0V) for the voltage feedback and also generates internal bias currents.

⑦ **Shunt Regulator** — The shunt regulator acts like a zener diode to clamp the voltage across the 4292, thus regulating the supply voltage applied to the 4292 to within safe limits.

Electrical Characteristics (V_S = -30V, R3 = 5kΩ, T_A = +25°C unless otherwise specified)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Section						
Output Voltage	V_{REF}	I_{REF} = 0mA	-4.850	-5.000	-5.150	Volts
Line Regulation	V_{RLINE}	V_S = -30V to -60V		0.15	0.2	% V_{OUT}
Load Regulation	V_{RLOAD}	I_{REF} = ±200μA		0.2	0.4	% V_{OUT}
Temperature Coefficient	TC_{VREF}			50		ppm/°C
Short Circuit Current	I_{REF} Short				-2.0	mA
Output Voltage	V_R	$R_{L(REF)}$ = 15kΩ	-4.800	-5.000	-5.200	Volts
Shunt Regulator Section						
Output Voltage	V_{SH}	At Pin 5	-13.5	-15.0	-16.5	Volts
Line Regulation	V_{LINE}	V_S = -30V to -60V	-1000	200	+1000	mV
Start-Up Voltage		R3 = 0Ω at Pin 5 I_{SH} = 4.0mA max.		-15.0	-16.5	Volts
Load Regulation	V_{LOAD}	I_C = 4mA to 20mA	-1.0	0.5	1.0	Volts
Oscillator Section						
Frequency Range	FO	C_X = 43pF for max C_X = 243pF for min	20		120	KHz
Frequency Accuracy		C_X = 43pF		10		%
Frequency Tempco	T_{CFO}	C_X = 43pF		5		% FO
Feedback Section						
Gain to Current Comparator	AV		6.0	8.0	10.0	V/V
Offset Voltage to Comparator				±30		mV
Input Bias Current				200		nA
Gain Amplifier						
Input Offset Current	V_{OS} Gain Amp			60		nA
Input Bias Current				500		nA
CMRR		V_{IN} = 0V to -5.5V		60		dB
Output Section						
V_{DRIVE} High	V_{DH}	Referred to Pin 8 I_L = 1mA			-1.8	Volts
V_{DRIVE} Low	V_{DL}	Referred to Pin 5 I_L = 1mA			2.0	Volts
V_D Sink Current	I_{SINK}		300	400		mA
V_D Source Current	I_{SOURCE}		300	400		mA

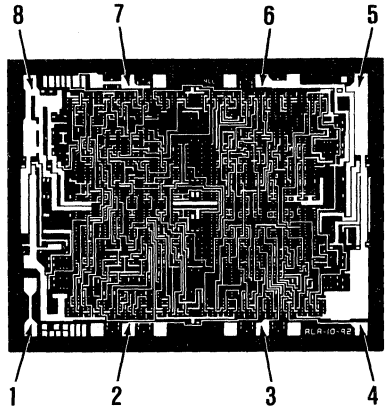
Electrical Characteristics (Continued)

(V_S = -30V, R3 = 5kΩ over full operating temperature range unless otherwise specified)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Section						
Output Voltage	V_{REF}	I_{REF} = 0mA	-4.800	-5.000	-5.200	Volts
Line Regulation	V_{LINE}	V_S = -30V to -60V			0.5	% V_{OUT}
Load Regulation	V_{LOAD}	I_{REF} = ±200μA			1.0	% V_{OUT}
Short Circuit Current	I_{SHORT}				-2.0	mA
Shunt Regulator Section						
Output Voltage	V_{OUT}	At Pin 3	-12.0	-15.0	-18.0	Volts
Line Regulation	V_{LINE}	V_S = -30V to -60V	-1500	±300	+1500	mV
Load Regulation	V_{LOAD}	I_C = 4mA to 20mA	-1.5	+0.7	+1.5	Volts
Oscillator Section						
Frequency Range	FO	CX_1 = 43pF CX_2 = 243pF	20		120	kHz
Feedback Section						
Gain to Current Comparator	AV		6.0	8.0	10.0	V/V
Output Section						
V_{DRIVE} High	V_{DH}	Referred to Pin 8 I_L = 1mA			-2.0	Volts
V_{DRIVE} Low	V_{DL}	Referred to Pin 5 I_L = 1mA			3.6	Volts
Sink Current	I_{SINK}		250	400		mA
Source Current	I_{SOURCE}		250	400		mA

A note on terminology: to minimize possible confusion in discussing a circuit which is designed "upside-down" with respect to standard positive-input switching regulators, the terms "greater" and "lesser" and "minimum" and "maximum" will refer to the magnitude or absolute value of a parameter and not to its polarity. Negative currents and voltages will still be referred to as negative, however, as in "-150μA" etc.

Mask Pattern

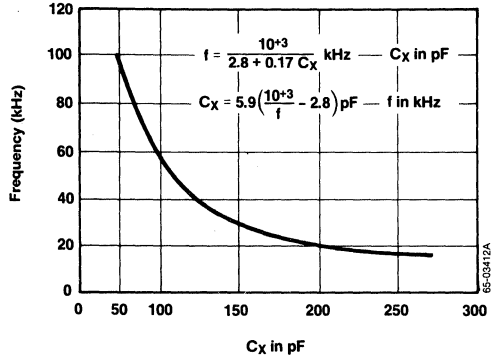


65-03430A

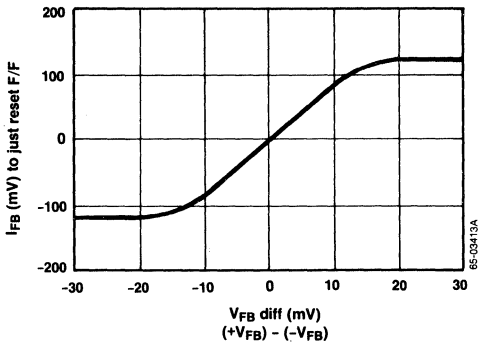
Die Size: 95 mils × 123 mils
Min. Pad Dimensions: 4 mils × 4 mils

Typical Performance Characteristics

Oscillator Frequency vs. C_X

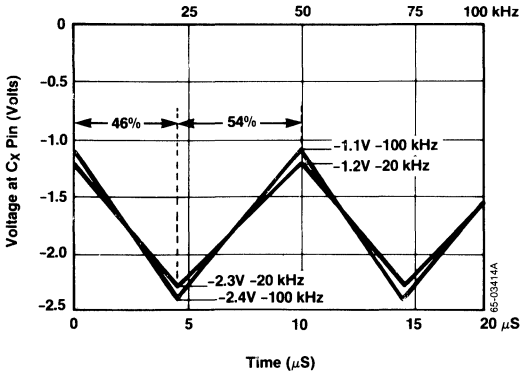


V_{FB} vs. I_{FB}

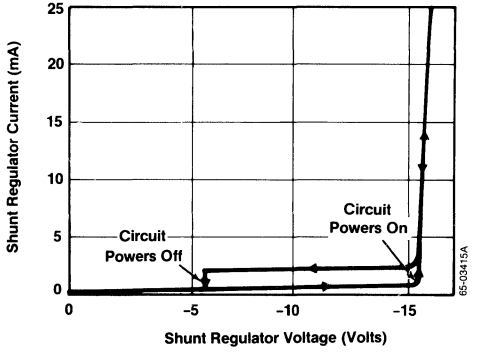


Typical Performance Characteristics (Continued)

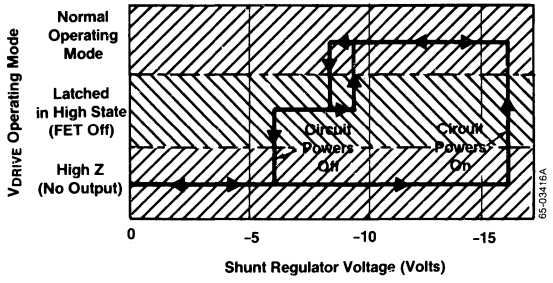
Typical Oscillator Waveform



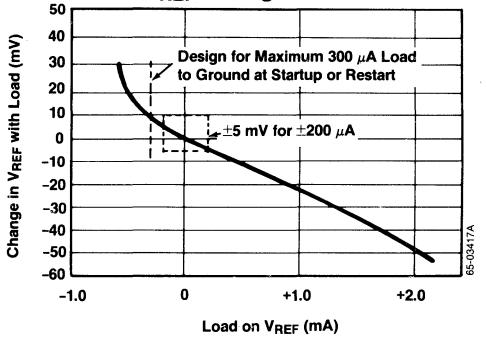
Shunt Regulator Current vs. Voltage



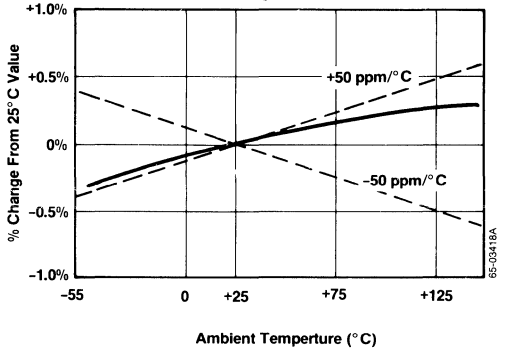
V_{DRIVE} Mode vs. Shunt Voltage



V_{REF} Change vs. Load

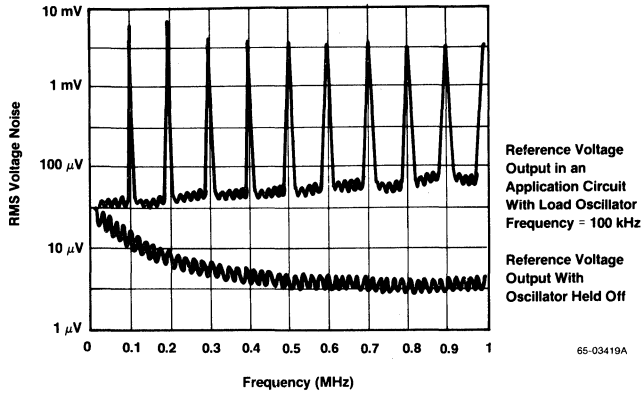


Typical Reference Voltage Change vs. Temperature

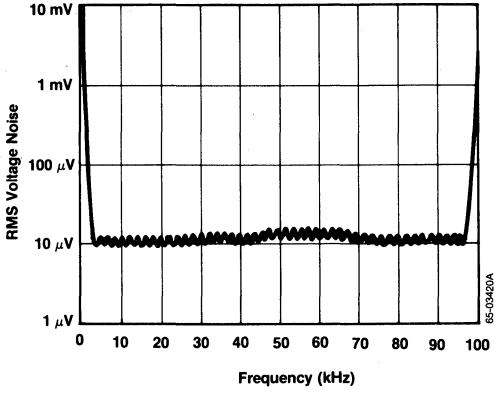


Typical Performance Characteristics (Continued)

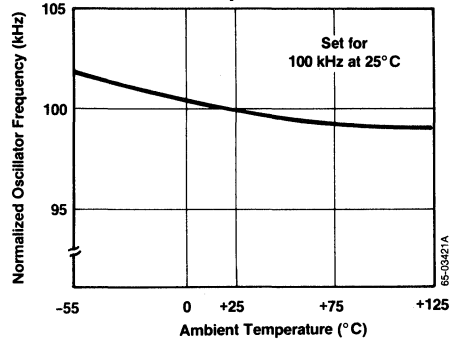
Reference Broadband Noise



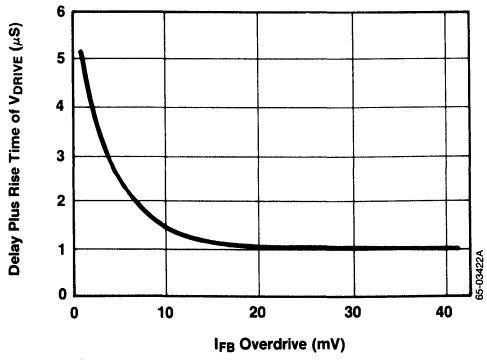
Reference Noise 0–100 kHz



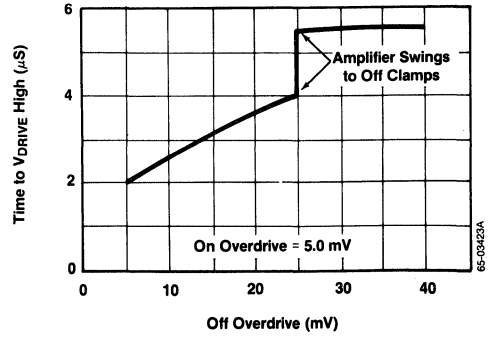
Typical Oscillator Frequency Change vs. Temperature



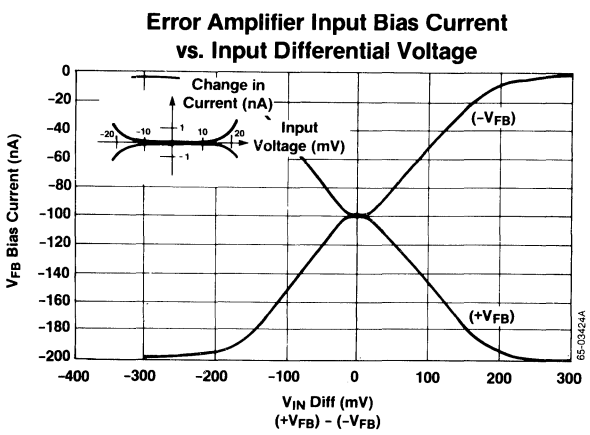
Response Time of I_{FB} to V_{DRIVE} High

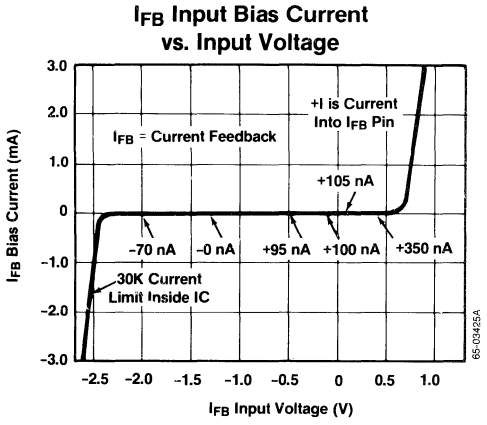


Error Amplifier Response Time vs. Off Overdrive



Typical Performance Characteristics (Continued)





Principles of Operation

Simple Flyback Circuit

Flyback voltage regulators and voltage converters are based on a two-cycle energy transfer. First, energy is stored in an inductor, and then it is transferred to the load capacitor.

A simplified diagram of a negative input, positive output voltage inverter circuit with ideal components is shown in Figure 1. When the switch S1 is closed, charging current from the battery flows through the inductor L1, which builds up a magnetic field, increasing as the switch is held closed. When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a current which flows through the inductor in the same direction as the charging current. Because there is no path for this current to flow through the switch, the current must flow through the diode to charge the capacitor C1. The key to the inversion is the ability of the inductor to become a source when the charging current is removed.

The equation V = (L)(dI/dT) gives the maximum possible voltage across the inductor; in the actual application, feedback circuitry and the output capacitor will decrease the output voltage to a regulated fixed value.

During discharge, the current in inductor L1 decreases and when it reaches zero, diode D1 stops conducting. It should be noted that the rate of change (with time) of the current in an inductor is proportional to the voltage across the inductor and inversely proportional to the inductance. Also, the load voltage and/or current can be regulated by controlling the on time of switch S1. It should also be noted that the load capacitor stores the energy until it is used by the load.

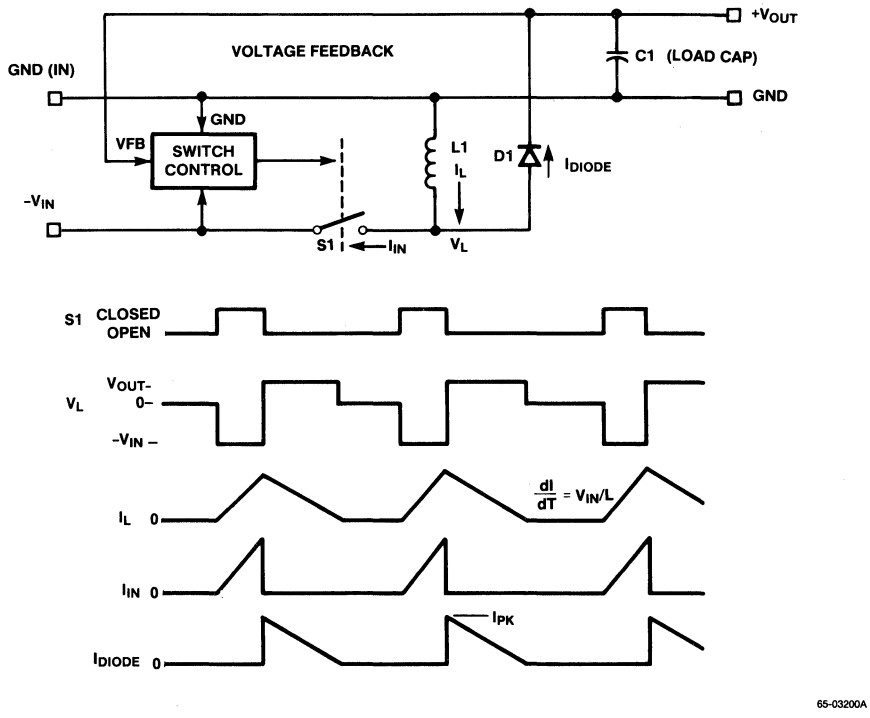


Figure 1. Simple Flyback Converter (Negative Input, Positive Output)

Transformer Flyback Circuit

In 4292 applications, S1 is an external transistor switch connected to ground, not the negative supply input. So, a simple inductor cannot be used to supply a positive V_{OUT}. But if L1 is replaced with a transformer, a positive V_{OUT} can be produced with a negative input. Transformers can be operated in two input to output modes. When the input and output current flow at the same time it is called a feed forward transformer. If the input current flow and the output current flow alternates, one preceding the other, it is a flyback transformer.

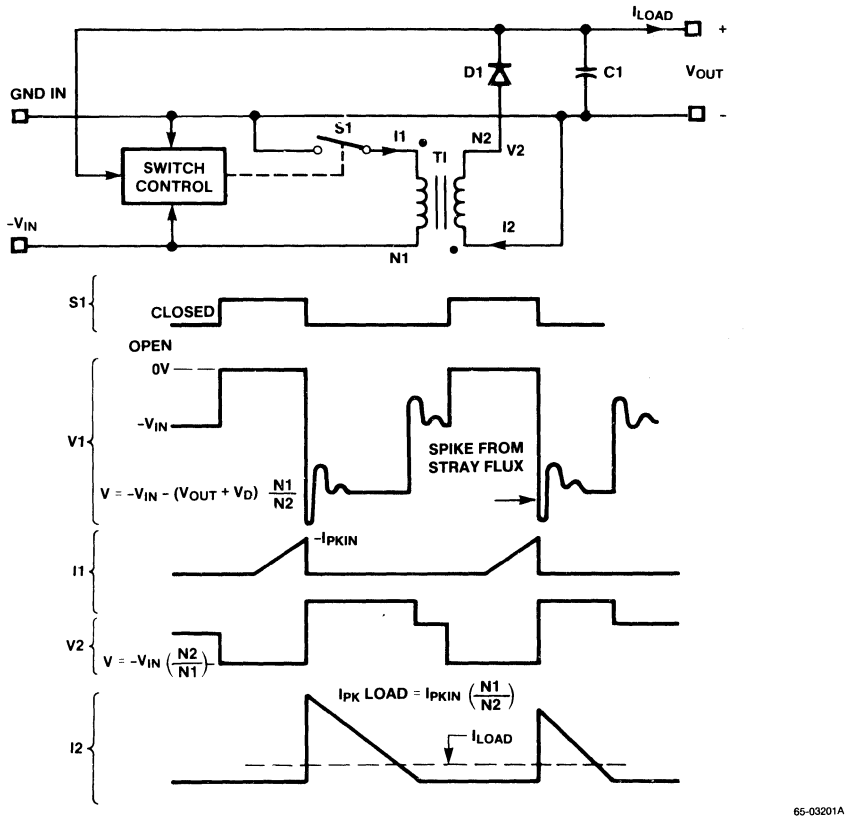


Figure 2. Transformer Flyback Circuit (Negative Input, Positive Output)

Because the magnetic flux paths in a transformer are common to both windings, the voltage at V1 changes almost instantly down and the voltage at V2 changes almost instantly up until D1 starts to conduct. The energy that was stored in the form of flux is transferred to the load capacitor. When only winding N1 or N2 is conducting current they act as simple inductors, and the equations for determining the type of transformer used can be derived from this fact. An additional key idea in deriving these equations is that the flux in the core is the same just before and just after S1 opens. If N1 and N2 share all the same flux paths then L1/# turns N1 = L2/# turns N2. Also, if the stray capacitance is zero then (I_{IN} PK)(#N1) = (I_{OUT} PK)(#N2).

If the two-cycle energy transfer is examined it can be seen that the energy stored in the inductor is stored in the form of magnetic flux. A simple inductor stores and removes the energy with the same winding. But a flyback transformer stores energy with one winding and removes energy with a second winding. Figure 2 shows the basic operation of a negative input positive output switching regulator having a ground connected switch and flyback transformer. The operation is very much like the operation of the circuit shown in Figure 1.

As before, the first cycle starts with the closing of S1; this pulls V1 up to ground and current starts from zero and ramps up in winding N1. This stores energy in the magnetic flux in the core of the flyback transformer. After a controlled time switch S1 opens and the energy is transferred from the core to the secondary, and then to the output.

Complete 4292 Application

The circuit of Figure 3 is similar to Figure 2 but includes the 4292 as the controller IC and also includes all the external components needed to produce positive output voltages.

When $-V_{IN}$ power is applied to this circuit, the first event is the shunt regulator starting up. It limits the voltage applied to the IC and prevents overvoltage. It also provides a pre-regulator for the IC supply voltage, which helps improve line regulation and PSRR. The next event is the activation of the internal voltage reference (pin 4). This reference serves two purposes: it provides a temperature stabilized voltage to compare the feedback signal to, and it also generates bias currents that power up the other functional blocks inside the IC.

At this time the error amplifier will sense that the output voltage is lower than it should be, and sends an error signal to the PWM circuitry in the control section. The PWM circuitry will begin switching the external FET switch (M1), and the output voltage will increase. When the output voltage reaches its regulated value the PWM circuitry will decrease the peak transformer current to maintain the output at a constant value.

Functional Description of the Components in the Complete 4292 Application (Figure 3)

R1, R2 — Their ratio determines V_{OUT}. The equivalent resistance of this combination should be kept in the range from 25 kΩ to 100 kΩ to minimize input bias current and input current noise errors. A good choice of resistor type is RN55 metal film.

Typical Specifications for 4292 Flyback Application (Figure 3)

(T_A = +25°C, V_{OUT} = +5.0V unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
Input Range	R3 = 5kΩ	-60	-48	-30	V
Input Range	R3 = 7.5kΩ	-90	-48	-40	V
Output Voltage	V_{IN} = -48V, I_L = +60mA		5.0		V
Line Regulation	R3 = 5kΩ, -60V to -30V_{IN}, I_L = 60mA		20		mV
Load Regulation	V_{IN} = -48V, I_L = 10mA to 120mA		15		mV
Load Regulation	V_{IN} = -48V, I_L = 0 to 10mA		20		mV
Efficiency	R3 = 7.5kΩ, V_{IN} = -48V I_{LOAD} = 120mA		60		%
Output Ripple	V_{IN} = 48V, I_L = 120mA		40		mV_{p-p}

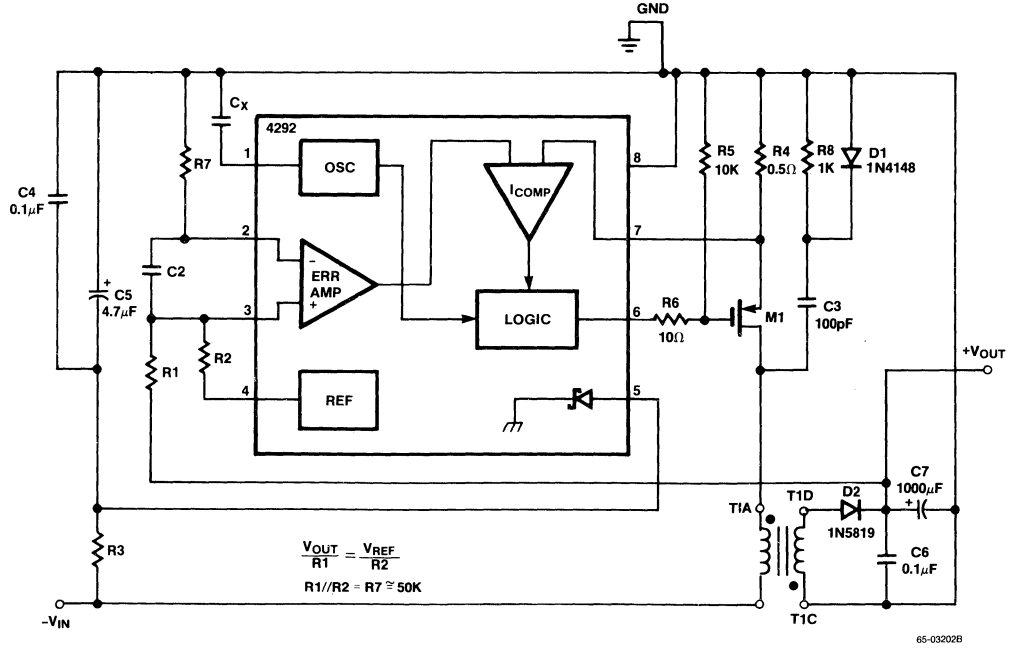


Figure 3. Complete 4292 Application Circuit (Negative Input, Positive Output)

R3 — Sets the shunt regulator current. This current and the power loss in R3 represent the major sources of efficiency losses in a typical 4292 application. A simple resistor here is best for applications having a fixed input voltage; for variable supply voltages, a current source such as that shown in Figure 4 can help keep efficiency high over a wide range of input voltage.

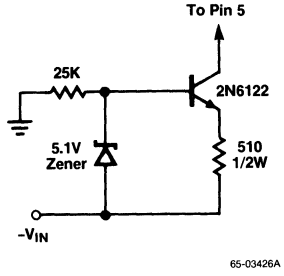


Figure 4. Current Source for I_{SHUNT} (instead of R3)

Other alternatives include putting an extra winding on the transformer and generating the shunt current from that with a rectifier diode and filter cap, or if a negative output greater than -15V is already being generated, a bootstrap circuit can be made by tapping that output with a diode and resistor connected to pin 5.

R4 — This low value (0.5Ω) resistor sets the maximum switch current. Current through the switch M1 develops a voltage across this resistor which is sensed by the current comparator. The level at which this voltage triggers the current comparator to end the cycle is a function of the amount of differential signal received by the error amplifier; see the graph of V_{FB} vs. I_{FB} under Typical Performance Characteristics. The purpose of designing this characteristic into the IC, instead of a fixed-value current limit, was to ensure that each cycle delivers the correct amount of charge to the output. For example, if the output is only lightly loaded, ΔV_{FB} will be very small with each cycle because the filter capacitor will not droop very much. Under these conditions it is desirable to keep each charging pulse small (by truncating the "on" portion of the cycle) to reduce output voltage ripple. The current comparator accomplishes this task, keeping ripple low over a wide range of load currents.

R5 — This resistor holds the power FET "off" during startup or any time the 4292 is inactive.

R6 — Provides for a signal loss in the gate drive to the FET to prevent possible oscillation (not always required).

R7 — Cancels input bias current errors at the error amplifier inputs (optional).

R8 — Part of a "scrubber" network that dampens ringing on the FET drain and transformer primary. This network reduces voltage spikes that might potentially overvoltage and damage the FET — depending on the type of FET used, the supply voltage, and the characteristics of the transformer, this scrubber network may not be required. A small increase in efficiency may be gained by omitting it.

C_X — Determines the oscillator frequency. Silver mica-type capacitors are recommended, as they have good temperature coefficients generally. See the graph of Oscillator Frequency vs. Timing Capacitor Value to select an appropriate value.

Operating frequencies in the range from 60 kHz to 100 kHz are typical. High frequencies will allow the use of a transformer having a small physical size; lower frequencies will help efficiency, as capacitive switching losses will be reduced.

C2 — Acts as a filter for the feedback signal. This low-value capacitor may not always be needed.

C3 — Part of the "scrubber" network — see R8.

C4,C5 — These capacitors filter the shunt regulator voltage. If the shunt current becomes too low to supply the 4292 properly, the output will shut down and turn on with low frequency

("motor boating"). This frequency will vary with the value of C5. C4 should have low impedance to high frequencies, as its purpose is to filter switching noise.

C6,C7 — Output filter capacitors.

D1 — Part of the "scrubber" network — see R8.

D2 — Rectifier diode for output. A power Schottky diode, such as a 1N5819, is recommended so as to maintain high efficiency.

M1 — MOSFET power switch. The fundamental limitation on the maximum load power that can be extracted from a 4292 power supply is determined by the gate-to-drain capacitance of the external FET. Although specifically designed to drive capacitive loads, the V_{DRIVE} output will not switch large FETs (I_D > 10A). The maximum FET size is also affected by the ratio of $-V_{IN}$ to V_{OUT}, since that ratio determines the effective gain of the FET and therefore its Miller capacitance. Recommended medium-power types follow:

- International Rectifier IRF9633 (1.2Ω channel resistance, 150V breakdown)
- Motorola MTP5P18 (1.0Ω channel resistance, 180V breakdown)

Negative Input, Negative Output Regulator (Figure 5)

The circuit in Figure 5 is a negative input-negative output step-down switching regulator. It operates similarly to the circuit shown in Figure 3 except that the transformer and output diode D2 are connected so as to produce a negative output voltage, and the feedback signal is applied to $-V_{FB}$ so as to maintain the correct sense of feedback polarity. Otherwise the same design criteria apply to this circuit as to Figure 3.

For applications where the negative output voltage is twice more of the negative input voltage a simple two terminal inductor can be used instead of a transistor. Figure 6 shows such a circuit.

Dual Output PBX Application (Figure 7)

This schematic is nearly identical to the one in Figure 3, except it has a center-tapped transformer secondary and additional components to create a negative output voltage. Also, component values are given that will work well in operating from the -48V off-hook voltage of a branch office or PBX telephone line.

The positive output is normally regulated by the PWM circuitry. The negative voltage is unregulated but will track the positive voltage if the voltage drops on D1 and D2 are matched. This type of regulation, through the magnetic loading produced by secondary taps, is best suited for applications where the load current is relatively constant.

The design of the transformer is critical in achieving best efficiency and minimum core size. The one here was designed to deliver +5V and -5.5V; to achieve different voltages or to meet other load requirements the turns ratio, core size, and core air gap may have to be adjusted. A good source for design information on this subject is *High Frequency Switch Power Supplies — Theory and Design* by G. Chryssis, McGraw Hill Book Company, New York, N.Y.

Low-Power Switched Capacitor Regulator (+5V and -15V Outputs)

This circuit, shown in Figure 8, does not require an inductor or transformer to generate positive output voltages. Instead, it uses the V_{DRIVE} output to charge a capacitor to the shunt voltage and then switch the more negative terminal to ground, much like the popular ICL 7660 IC. Like the 7660, the load current capability is limited; with +5V out, the maximum current ranges between 10 mA and 20 mA.

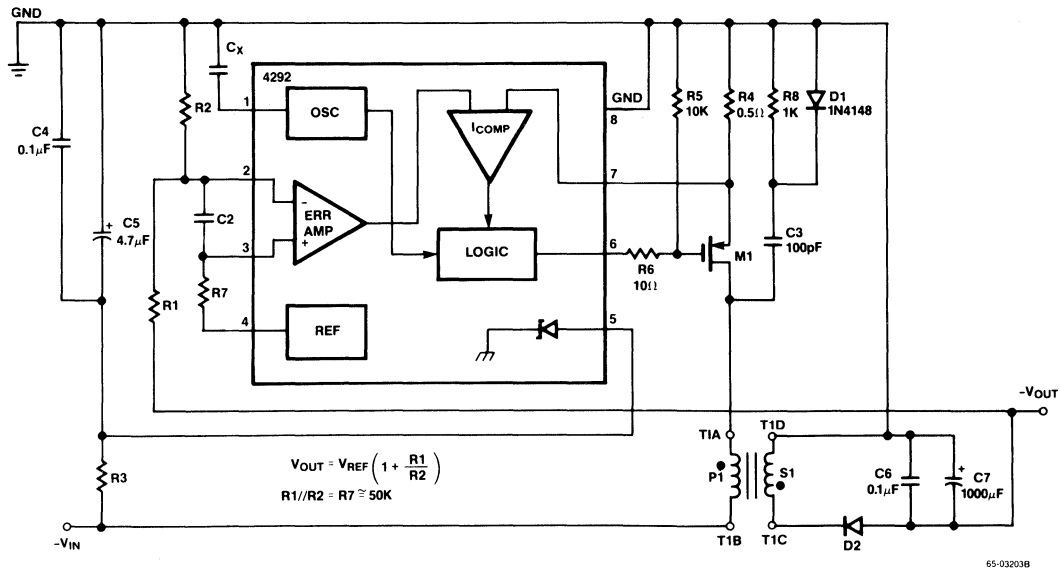


Figure 5. Negative Input, Negative Output Regulator With Transformer

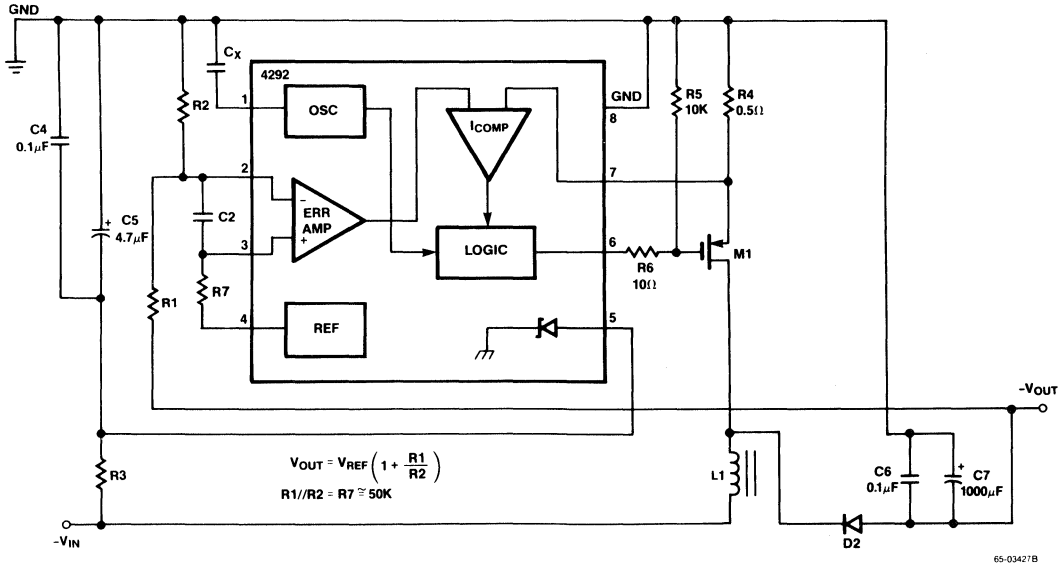


Figure 6. Negative Input, Negative Output Regulator With Simple Inductor

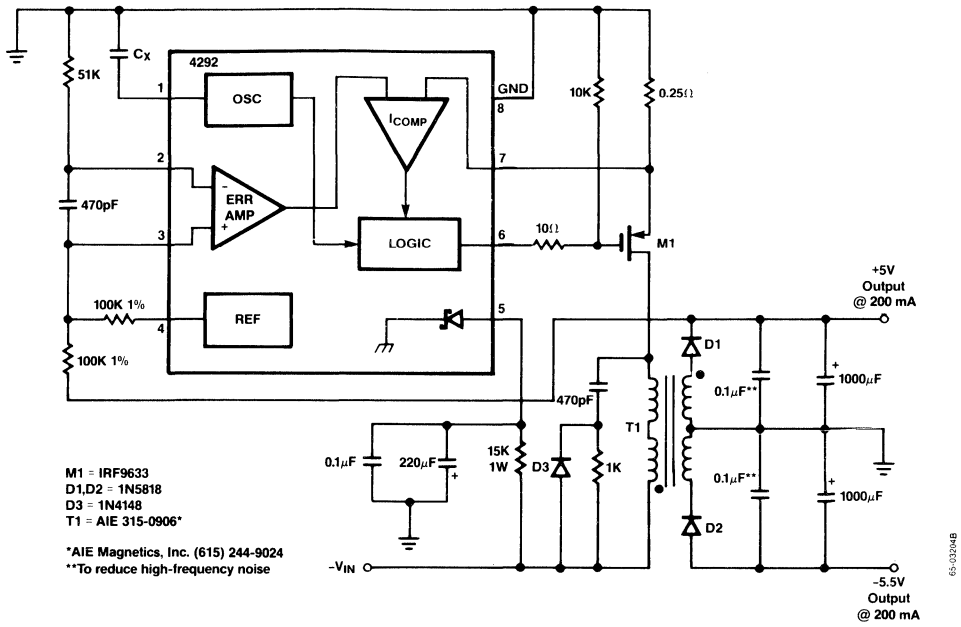
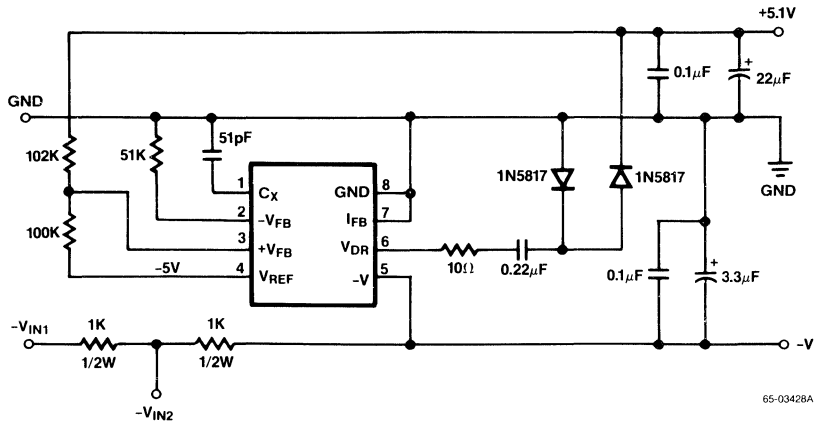


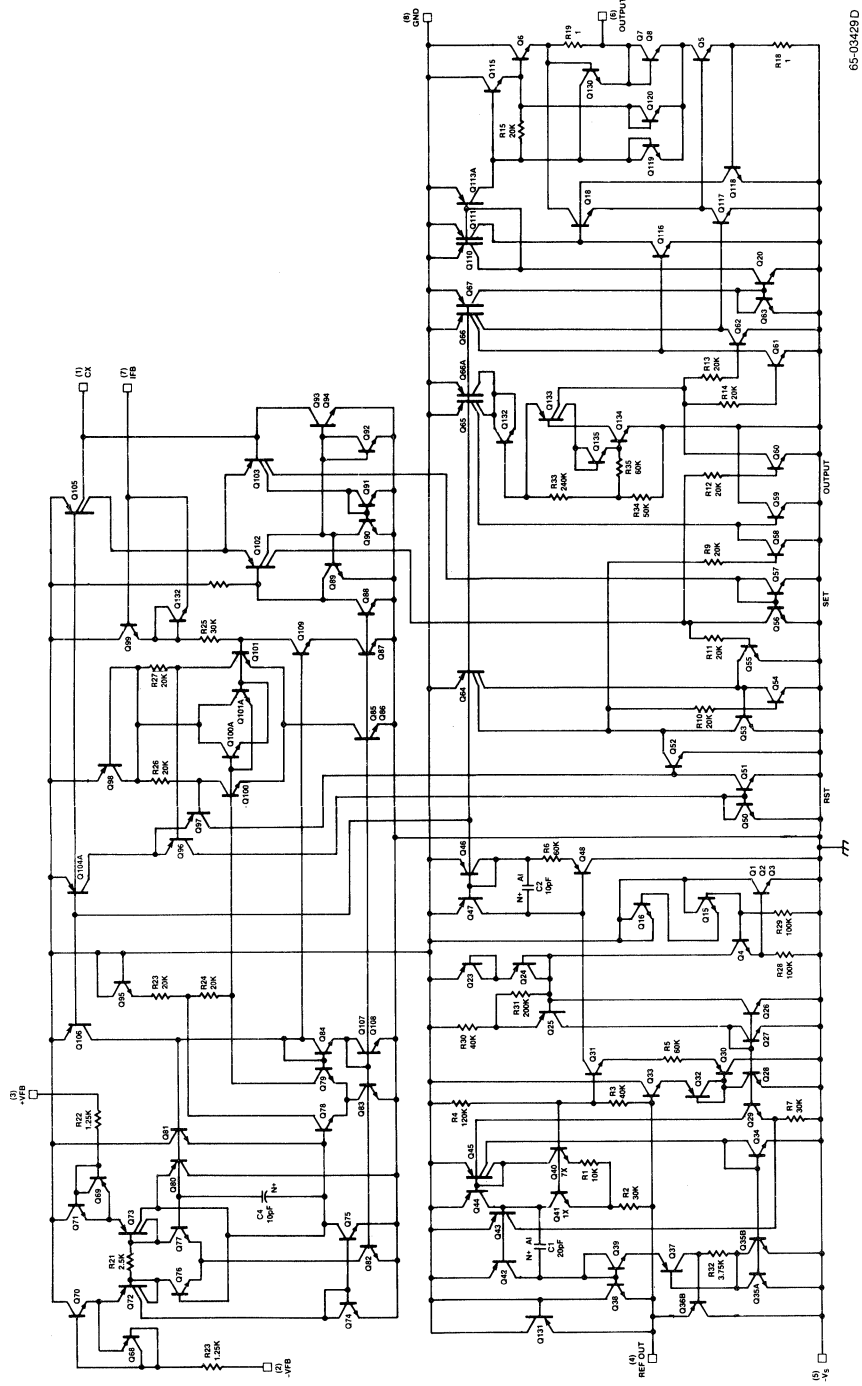
Figure 7. Dual-Output PBX Telephone Application (V_{OUT} = +5V and -5.5V)



Note: Use $-V_{IN2}$ for V_{IN} = -20V to -35V

Figure 8. Low-Power Switched-Capacitor Regulator

Complete Schematic Diagram



RC4391 Inverting and Step-Down Switching Regulator

Features

- Versatile —
  - Inverting function (+ to -)
  - Step-down function
  - Adjustable output voltage
  - Regulates supply changes
- Micropower —
  - Low quiescent current — 170 µA
  - Wide supply range — 4V to 30V
- High performance —
  - High switch current —375 mA
  - High efficiency — 70% typically
- Low battery detection capability
- 8-lead mini-DIP or S.O. package

Description

Raytheon's RC4391 is a monolithic switch mode power supply controller for micropower circuits. The 4391 integrates all the active functions needed for low power switching supplies, including oscillator, switch, reference and logic, into a small package. Also, the quiescent supply current drawn by the 4391 is extremely low; this combination of low supply current, function, and small package make it adaptable to a variety of miniature power supply applications.

The 4391 complements the other Raytheon switching regulator IC, the RC4190. The 4190 is dedicated to step-up ($V_{OUT} > V_{IN}$) applications, while the 4391 was designed up for inverting (positive input, negative output) and step-down ($V_{OUT} < V_{IN}$) applications. Between the two devices the ability to create all three basic switching regulator configurations is assured. Refer to the 4190 data sheet for information on step-up applications.

The functions provided are:

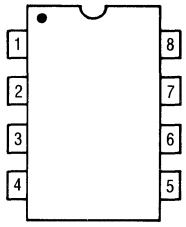
- Squarewave oscillator (adjustable externally)
- Bandgap voltage reference
- High current PNP switch transistor
- Feedback comparator
- Logic for gating the comparator
- Circuitry for detecting for a discharged battery condition (in battery powered systems)

Few external components are required to build a complete DC-to-DC converter:

- Inductor
- Low value capacitor to set the oscillator frequency
- Electrolytic filter capacitor
- Steering diode
- Two resistors

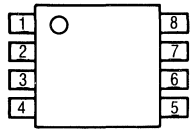
Connection Information

8-Lead DIP
(Top View)



65-00070

8-Lead Small Outline Plastic SO-8
(Top View)



65-02666A

Pin	Function
1	Low Battery Resistor (LBR)
2	Low Battery Detector (LBD)
3	Timing Capacitor (C_X)
4	Ground
5	External Inductor (L_X)
6	+Supply Voltage ($+V_S$)
7	+1.25V Reference Voltage (V_{REF})
8	Feedback Voltage (V_{FB})

Ordering Information

Part Number	Package	Operating Temperature Range
RC4391N	N	0°C to +70°C
RC4391M	M	0°C to +70°C
RV4391N	N	-25° C to +85°C
RM4391D	D	-55°C to +125°C
RM4391D/883B	D	-55°C to +125°C

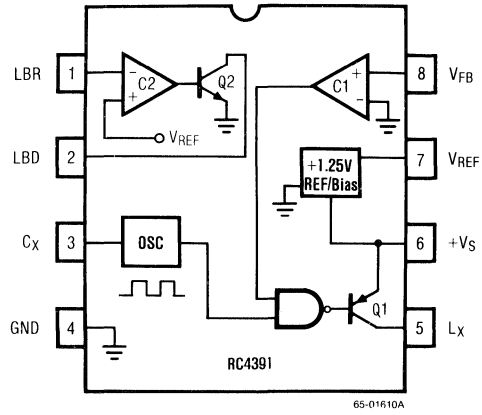
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Absolute Maximum Ratings

Internal Power Dissipation .....500 mW
Supply Voltage*
(Pin 6 to Pin 4 or
Pin 6 to Pin 5) .....+30V
Storage Temperature
Range .....-65°C to +150°C
Operating Temperature Range
RM4391 .....-55°C to +125°C
RV4391 .....-25°C to +85°C
RC4391 .....0°C to +70°C
Switch Current (I_{MAX}) .....375 mA peak

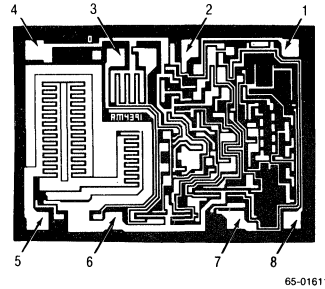
*The maximum allowable supply voltage ($+V_S$) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used in place of Q1.

Functional Block Diagram



65-01610A

Mask Pattern



65-01611A

Die Size: 69 x 50 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP	8-Lead Small Outline Plastic SO-8
Max. Junction Temp.	125°C	175°C	125°C
Max. P_D T_A <50°C	468 mW	833 mW	300 mW
Therm. Res θ_{JC}	—	45°C/W	—
Therm. Res. θ_{JA}	160°C/W	150°C/W	240°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.33 mW/°C	4.17 mW/°C

Electrical Chacteristics

(V_S = +6.0V, over the full operating temperature range unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage	$+V_S$	(Note 1)	+4.0		+30V	V
Supply Current	I_{SY}	V_S = +25V		300	500	μA
Reference Voltage	V_{REF}		1.13	1.25	1.36	V
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.5	-5.0	-4.5	V
		$V_{OUT\ nom}$ = -15V	-16.5	-15	-13.5	
Line Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 150pF, V_S = +5.8V to +15V		2.0	4.0	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X =150pF, V_S = +5.8V to +15V		1.5	3.0	
Load Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.5	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.3	
Switch Leakage Current	I_{CO}	Pin 5 = -20V		0.1	30	μA

Note 1. The maximum allowable supply voltage ($+V_S$) in inverting applications will be reduced by the value of the negative output voltage, unless an external power transistor is used in place of Q1.

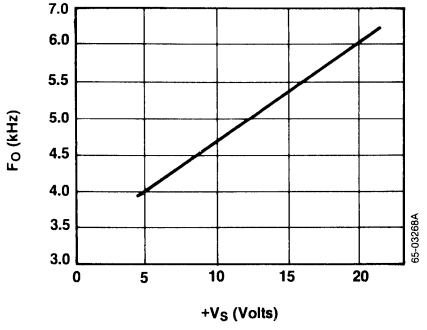
Electrical Characteristics

(V_S = +6.0V, T_A = +25° C unless otherwise noted)

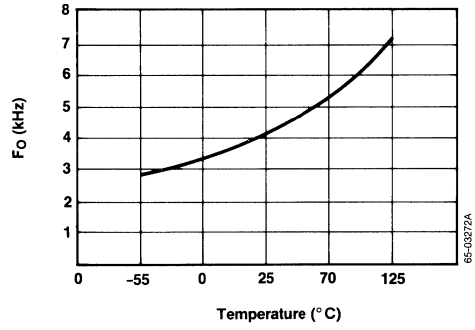
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current	I_{SY}	V_S = +4.0V, No External Loads		170	250	μA
		V_S = +25V, No External Loads		300	500	
Output Voltage	V_{OUT}	$V_{OUT\ nom}$ = -5.0V	-5.35	-5.0	-4.65	V
		$V_{OUT\ nom}$ = -15V	-15.85	-15	-14.15	
Line Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 150pF, V_S = +5.8V to +15V		1.5	3.0	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 150pF, V_S = +5.8V to +15V		1.0	2.0	
Load Regulation		$V_{OUT\ nom}$ = -5.0V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.2	0.4	% V_{OUT}
		$V_{OUT\ nom}$ = -15V, C_X = 350pF, V_S = +4.5V, P_{LOAD} = 0mW to 75mW		0.07	0.14	
Reference Voltage	V_{REF}		1.18	1.25	1.32	V
Switch Current	I_{SW}	Pin 5 = 5.5V	75	100		mA
Switch Leakage Current	I_{CO}	Pin 5 = -24V		0.01	5.0	μA
Timing Pin Current	I_{CX}	Pin 3 = 0V	6.0	10	14	μA
LBD Leakage Current		Pin 1 = 1.5V, Pin 2 = 6.0V		0.01	5.0	μA
LBD on Current		Pin 1 = 1.1V, Pin 2 = 0.4V	210	600		μA
LBR Bias Current		Pin 1 =1.5V		0.7		μA

Typical Performance Characteristics

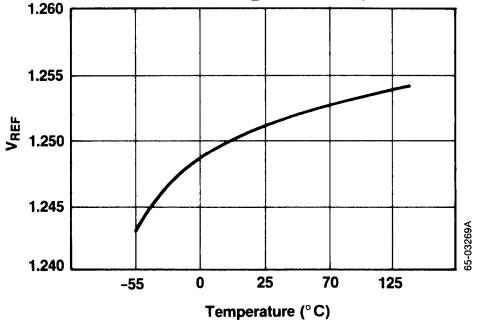
Oscillator Frequency vs. Supply Voltage



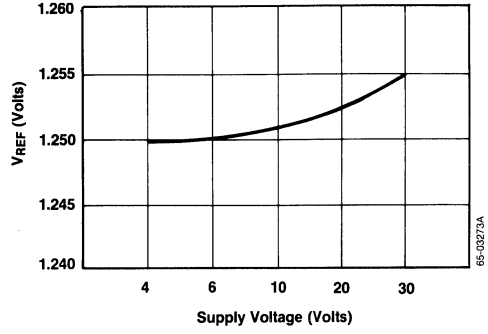
Oscillator Frequency vs. Temperature



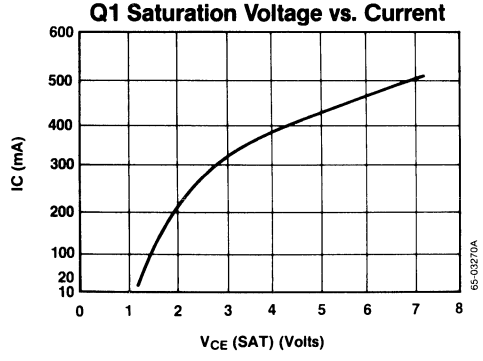
Reference Voltage vs. Temperature



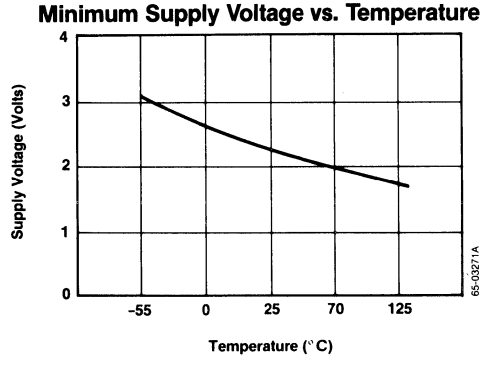
Reference Voltage vs. Supply Voltage



Q1 Saturation Voltage vs. Current



Minimum Supply Voltage vs. Temperature



Principles of Operation

Inverting Regulator

The basic switching inverter circuit is the building block on which the complete inverting application is based.

A simplified diagram of the voltage inverter circuit with ideal components and no feedback circuitry is shown in Figure 1. When the switch S is closed, charging current from the battery flows through the inductor L, which builds up a magnetic field, increasing as the switch is held closed. When the switch is opened, the magnetic field collapses, and the energy stored in the magnetic field is converted into a current which flows through the inductor in the same direction as the charging current. Because there is no path for this current to flow through the switch, the current must flow through the diode to charge the capacitor C. The key to the inversion is the ability of the inductor to become a source when the charging current is removed.

The equation V = (L) (di/dt) gives the maximum possible voltage across the inductor; in the actual application, feedback circuitry and the output capacitor will decrease the output voltage to a regulated fixed value.

A complete schematic for the standard inverting application is shown in Figure 2. The ideal switch in the simplified diagram is replaced by the PNP transistor switch between pins 5 and 6. C_F functions as the output filter capacitor, and D1 and L_X replace D and L.

When power is first applied, the ground sensing comparator (pin 8) compares the output voltage to the +1.25V voltage reference. Because C_F is initially discharged a positive voltage is applied to the comparator, and the output of the comparator gates the squarewave oscillator. This gated squarewave signal turns on, then off, the PNP output transistor. This turning on and off of the output transistor performs the same function as opening and closing the ideal switch in the simplified diagram; i.e., it stores energy in the inductor during the on time and releases it into the capacitor during the off time. See Figure 3 for a representation of the switching waveforms.

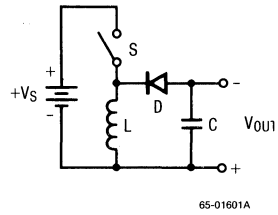
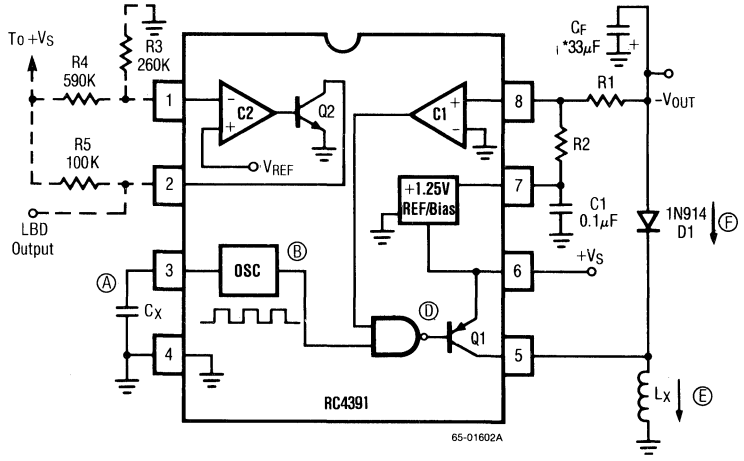


Figure 1. Simplified Voltage Inverter



Parts List	-5.0V Output	-15V Output
R1 =	300kΩ	900kΩ
R2 =	75kΩ	75kΩ
C_X =	150pF	150pF
L_X =	1.0mH Dale TE3 Q4 TA	

---- = Optional

$$-V_{OUT} = (1.25V)\left(\frac{R1}{R2}\right)$$

*Caution: Use current limiting protection circuit for high values of C_F (Fig. 13)

Figure 2. Inverting Regulator — Standard Circuit

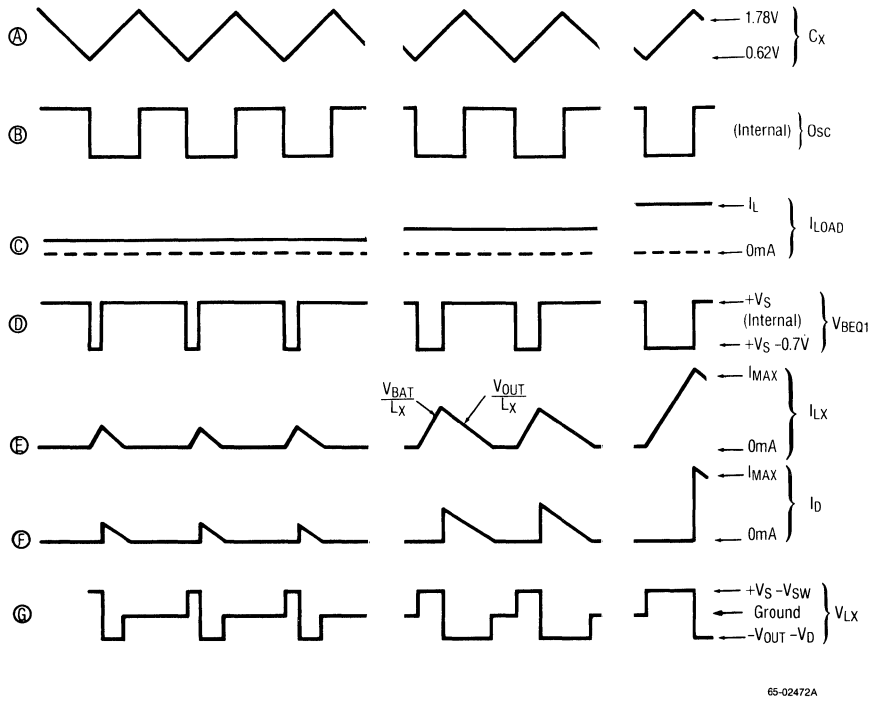


Figure 3. Inverting Regulator Waveforms

The comparator will continue to gate the oscillator to the switch transistor until enough energy has been stored in the output capacitor to make the comparator input voltage decrease to less than 0V. The voltage applied to the comparator is set by the output voltage, the reference voltage, and the ratio of R1 to R2.

Step-Down Regulator

The step-down circuit function is similar to inversion; it uses the same components (switch, inductor, diode, filter capacitor), and charges and discharges the inductor by closing and opening the switch. The great difference is that the inductor is in series with the load; therefore, both the charging current and the discharge current flow into the load. In the inverting circuit only the discharge current flows into the load. Refer to Figure 4.

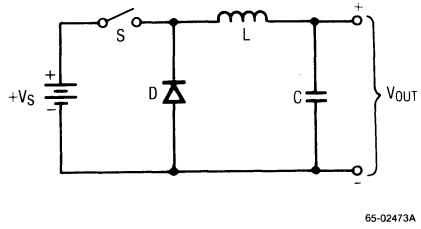
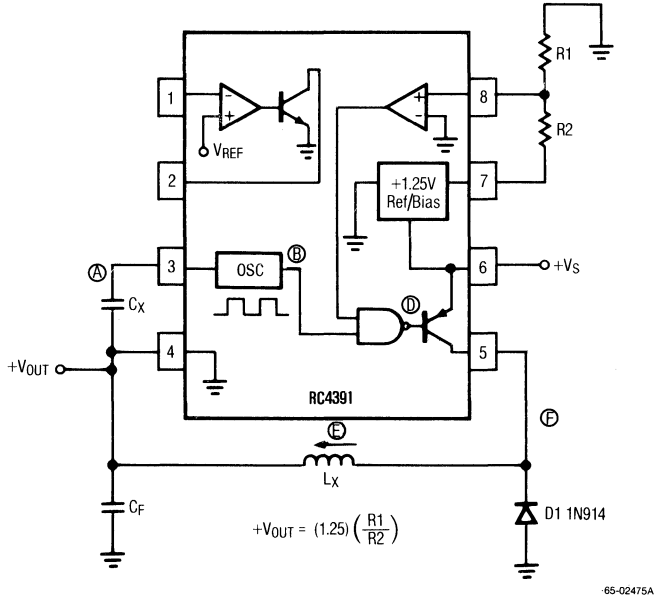


Figure 4. Simplified Step-Down Circuit

When the switch S is closed, current flows from the battery, through the inductor, and through the load resistor to ground. After the switch is opened, stored energy in the inductor causes current to keep flowing through the load, the circuit being completed by the catch diode D. Since current flows to the load during charge and discharge, the average load curent will be greater than in an inverting circuit. The significance of that is that for equal load currents the step-down circuit will require less peak inductor current than an inverting circuit. Therefore, the inductor will not require as large of a core, and the switch transistor will not be stressed as heavily for equal load currents.

Figure 5 depicts a complete schematic for a step-down circuit using the 4391. Observe that the ground lead of the 4391 is **not** connected to circuit ground; instead, it is tied to the output voltage. It is by this rearrangement that the feedback system, which senses voltages more negative than the ground lead, can be used to regulate a non-negative output voltage.

When power is first applied, the output filter capacitor is discharged so the ground lead potential starts at 0V. The reference voltage is forced to +1.25V above the ground lead and pulls the feedback input (pin 8) more positive than the ground lead. This positive voltage forces the control network to begin pulsing the switch transistor. As the switching action pumps up the output voltage, the ground lead rises with the output until the voltage on the ground lead is equal to the feedback voltage. At that point, the control network reduces the on time of the switch to maintain a constant output. See Figure 6 for a graph of step-down regulator waveforms.



Important Note: This circuit must have a minimum load ≥ 1 mA always connected

Figure 5. Step-Down Regulator — Standard Circuit

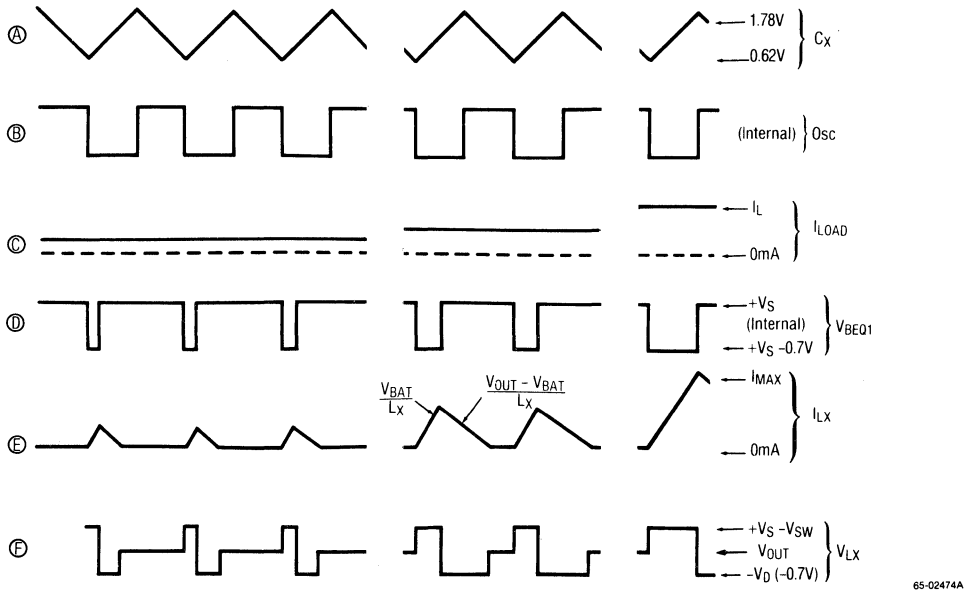


Figure 6. Step-Down Regulator Waveforms

Design Equations

The inductor value and timing capacitor (C_X) value must be carefully tailored to the input voltage, input voltage range, output voltage, and load current requirements of the application. The key to the problem is to select the correct inductor value for a given oscillator frequency, such that the inductor current rises to a high enough peak value (I_{MAX}) to meet the average load current drain. The selection of this inductor value must take into account the variation of oscillator frequency from unit to unit and the drift of frequency over temperature. Use ±30% as a maximum variation of oscillator frequency.

The oscillator creates a squarewave using a method similar to the 555 timer IC, with a current steering flip-flop controlled by two voltage sensing comparators. The oscillator frequency is set by the timing capacitor (C_X) according to the following equation:

$$f_O\ (Hz) = \frac{4.1 \times 10^{-6}}{C_X}$$

The squarewave output of the oscillator is internal and cannot be directly measured, but is equal in frequency to the triangle waveform measurable at pin 3. The switch transistor is normally on when the triangle waveform is ramping up and off when ramping down. Capacitor selection depends on the application; higher operating frequencies will reduce the output voltage ripple and will allow the use of an inductor with a physically smaller inductor core, but excessively high frequencies will reduce load driving capability and efficiency.

Inverting Design Procedure

1. Select an operating frequency and timing capacitor value as shown above (frequencies from 10kHz to 50kHz are typical).
2. Find the maximum on time T_{ON} (add 3μS for the turn off base recombination delay of Q1):

$$T_{ON} = \frac{1}{2f_O} + 3\mu S$$

3. Calculate the peak inductor current I_{MAX} (if this value is greater than 375mA then an external power transistor must be in place of Q1):

$$I_{MAX} = \frac{(V_{OUT} + V_D)\, 2I_L}{(f_O)\,(T_{ON})\,(V_S - V_{SW})}$$

Where:
V_S = Supply Voltage
V_{SW} = Saturation Voltage of Q1 (typically 0.5V)
V_D = Diode Forward Voltage (typically 0.7V)
I_L = DC Load Current

4. Find an inductance value for L_X:

$$L_X \text{ (Henries)} = \left(\frac{V_S - V_{SW}}{I_{MAX}}\right)\left(T_{ON}\right)$$

The inductor chosen must exhibit this value of inductance and have a current rating equal to I_{MAX}.

Step-Down Design Procedure

1. Select an operating frequency.
2. Determine the maximum on time T_{ON} as in the inverting design procedure.
3. Calculate I_{MAX}:

$$I_{MAX} = \frac{2I_L}{(f_O)\,(T_{ON})\left[\frac{(V_S - V_{OUT})}{(V_{OUT} - V_D)} + 1\right]}$$

4. Calculate L_X:

$$L_X = \left(\frac{V_S - V_{OUT}}{I_{MAX}}\right)\left(T_{ON}\right)$$

Alternate Design Procedure

The design equations above will not work for certain input/output voltage ratios, and for these circuits another method of defining component values must be used. If the slope of the current discharge waveform is much less than the slope of the current charging waveform, then the inductor current will become continuous (never discharging completely), and the equations will become extremely complex. So, if the voltage applied across the inductor during the charge time is greater than during the discharge time, use the design procedure below. For example, a step-down circuit with 20V input and 5V output will have approximately 15V across the inductor when charging, and approximately 5V when discharging. So in this example the inductor current will be continuous and the alternate procedure will be necessary. The alternate procedure may also be used for discontinuous circuits.

1. Select an operating frequency based on EMI and component size requirements (a value between 10kHz and 50kHz is typical).
2. Build the circuit and apply the worst cast conditions to it, i.e., the lowest battery voltage and the highest load current at the desired output voltage.
3. Adjust the inductor value down until the desired output voltage is achieved, then decrease its value by 30% to cover manufacturing tolerances.
4. Check the output voltage with an oscilloscope for ripple, at high supply voltages, at voltages as high as are expected. Also check for efficiency by monitoring supply and output voltages and currents (eff = $(V_{OUT})\ (I_{OUT})/(+V_S)\ (I_{SY})$ x 100%).
5. If the efficiency is poor, go back to step 1. and start over. If the ripple is excessive, then increase the output filter capacitor value or start over.

Inductors

Efficiency and load regulation will improve if a quality high Q inductor is used. A ferrite pot core is recommended; the wind-yourself type with an air gap adjustable by washers or spacers is very useful for bread-boarding prototypes. Care must be taken to choose a core with enough permeability to handle the magnetic flux produced at I_{MAX}. If the core saturates, then efficiency and output current capability are severely degraded and excessive current will flow through the switch transistor. An isolated AC current probe for an oscilloscope (example: Tektronix P6042) is an excellent tool for saturation problems; with it the inductor current can be monitored for nonlinearity at the peaks (a sign of saturation).

Low Battery Detector

An open collector signal transistor Q2 with comparator C2 provides the designer with a method of signaling a display or computer whenever the battery voltage falls below a programmed level (see Figure 7). This level is determined by the +1.25V reference level and by the selection of two external resistors according to the equation:

$$V_{TH} = V_{REF}\left(\frac{R4}{R3} + 1\right)$$

When the battery drops below this threshold Q2 will turn on and sink typically 600μA. The low battery detection circuit can also be used for other less conventional applications such as the voltage dependent oscillator circuit of Figure 12.

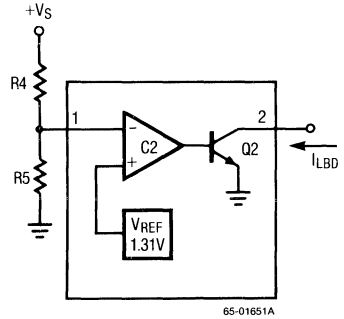


Figure 7. Low Battery Detector

Device Shutdown

The entire device may be shut down to an extremely low current non-operating condition by disconnecting the ground (pin 4). This can be easily done by putting an NPN transistor in series with the ground pin and switching it with an external signal. This switch will not affect the efficiency of operation, but will add to and increase the reference voltage by an amount equal to the saturation voltage of the transistor used. A mechanical switch can also be used in series between circuit ground and pin 4, without introducing any reference offset.

Compensation

When large values (>50kΩ) are used for the voltage setting resistors (R1 and R2 of Figure 2) stray capacitance at the V_{FB} input can add a lag to the feedback response, destabilizing the regulator, increasing low frequency ripple, and lowering efficiency. This can often be avoided by minimizing the stray capacitance at the V_{FB} node. It can also be remedied by adding a lead compensation capacitor of 100pF to 10nF. In inverting applications, the capacitor connects between $-V_{OUT}$ and V_{FB}; for step-down circuits it connects between ground and V_{FB}. Most applications do not require this capacitor.

Power Transistor Interfaces

The most important consideration in selecting an external power transistor is the saturation voltage at $I_C = I_{MAX}$. The lower the saturation voltage is, the better the efficiency will be. Also, a higher beta transistor requires less base drive and therefore less power will be consuming in driving it, improving efficiency losses in the interface. The part numbers given in the following applications are recommended, but other types may be more appropriate depending on voltage and power levels.

When troubleshooting external power transistor circuits, ensure that clean, sharp-edged waveforms are driving the interface and power transistors. Monitor these waveforms with an oscilloscope — disconnect the inductor, and tie the V_{FB} input (pin 8) high through a 10K resistor. This will cause the regulator to pulse at maximum duty cycle without drawing excessive inductor currents. Check for expected on time and off time, and look for slow rise times that might cause the power transistor to enter its linear operating region.

The following external power transistor circuits may demand some adjustment to resistor values to satisfy various power levels and input/output voltages. C_X and L_X values must be selected according to the design equations (pages 9 and 10).

Inverting Medium Power Interface

Figure 8 is a schematic of an inverting power supply using an external PNP switch transistor. Supply voltage is applied to the IC via R3; when the internal switch transistor is turned on current through R4 is also drawn through R3, creating a voltage drop from base to emitter of the external switch transistor. This drop turns on the external transistor.

Voltage pulses on the supply lead (pin 6) do not affect circuit operation because the internal reference and bias circuitry have good supply rejection capabilities. A power Schottky diode is used for higher efficiency.

Inverting High Power Interface

For higher power applications (500mW to 5W), refer to Figure 9. This circuit uses an extra external transistor to provide well controlled drive current in the correct phase to the power switch transistor. The value of R3 sets the drive current to the switch by making the interface transistor act as a current source. R4 and R5 must be selected such that the RC time constant of R4 and the base capacitance of Q2 do not slow the response time (and affect duty cycle), but not so low in value that excess power is consumed and efficiency suffers. The resistor values chosen should be proportional to the supply voltage (values shown are for +5V).

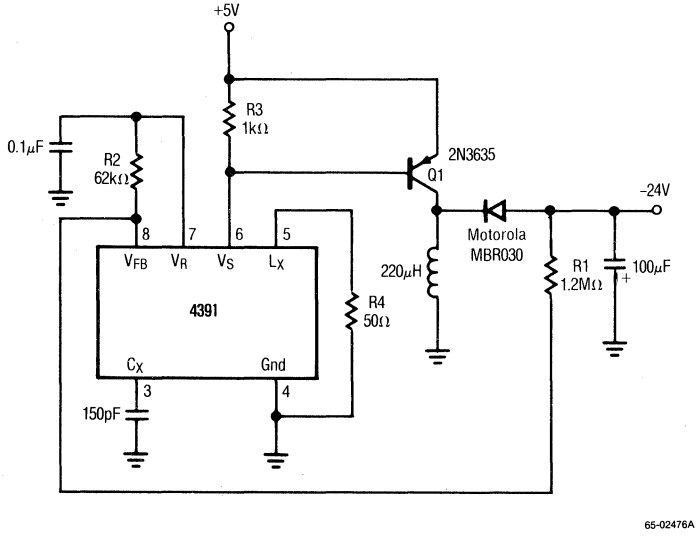


Figure 8. Inverting Medium Power (250mW to 1W) Application

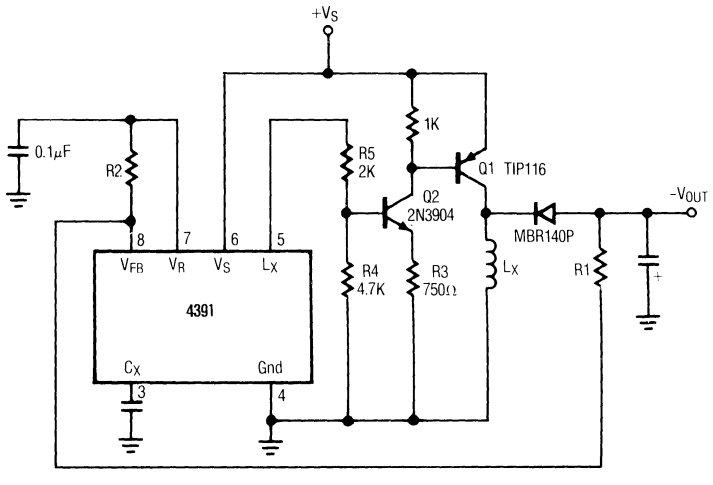


Figure 9. Inverting High Power Application

Step-Down Interfaces

Figures 10 and 11 show medium and high power interfaces modified to perform step-down functioning. The design equations and suggestions for the circuits of Figures 8 and 9 also apply to these circuits. For a certain range of load power, the RC4193 IC can be used for step-down applications. A load range from 400mW to 2W can be sustained with fewer components (especially when stepping down greater than 30V) than the comparable 4391 circuit. Refer to Raytheon's RC4191/4192/4193 data sheet for a schematic of this medium power step-down application.

Voltage Dependent Oscillator

The 4391's ability to supply load current at low battery voltages depends on the inductor value and the oscillator frequency. Low values of inductance or a low oscillator frequency will cause a higher peak inductor current and therefore increase the lead current capability. A large inductor current is not necessarily best, however, because the large amount of energy delivered with each cycle will cause a large voltage ripple at the output, especially at high input voltages. This tradeoff between load current capability and output ripple can be improved with the circuit connection shown in Figure 12. This circuit uses the low battery detector to sense for a low battery voltage condition and will decrease the oscillator frequency after a pre-progrmamed threshold is reached.

The threshold is programmed exactly as the normal low battery detector connection:

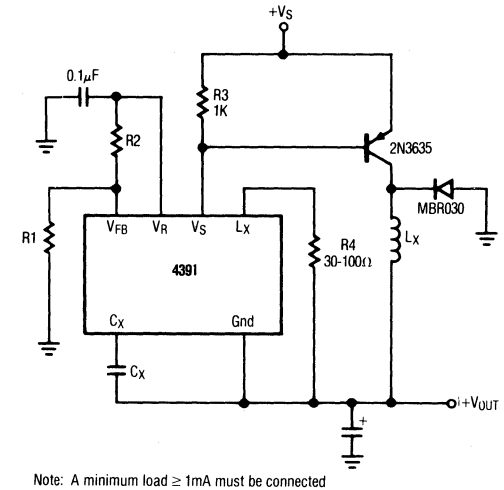
$$V_{TH} = V_{REF}\left(\frac{R4}{R3} + 1\right)$$

When the battery voltage reaches this threshold the comparator will turn on the open collector transistor at pin 2, effectively pulling C_Y in parallel with C_X. This added capacitance will reduce the oscillator frequency, according to the following equation:

$$f_O = \frac{4.1 \times 10^{-6}}{C_X + C_Y}$$

Current Limiting

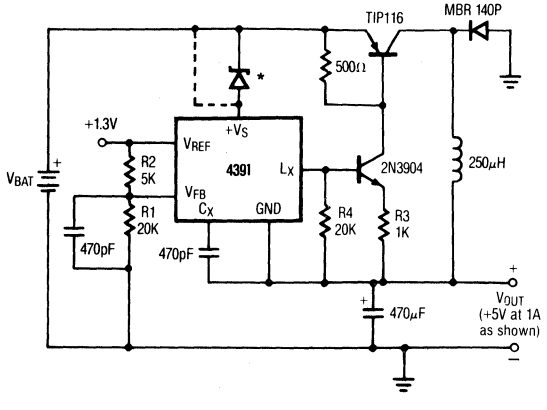
The oscillator (C_X) pin can be used to add short circuit protection and to protect against overcurrent at start-up (when using large values of output filter capacitor — greater than 100 μF). A transistor V_{BE} is used as a current sensing comparator which resets the oscillator upon sensing an overcurrent condition, thus providing cycle-by-cycle current limiting. Figure 13 shows how this is applied.



Note: A minimum load ≥ 1mA must be connected

65-02479A

Figure 10. Step-Down Medium Power Application



Note: A minimum load ≥ 1mA must be connected.
*Optional — Extends supply voltage range

65-02077A

Figure 11. High Power Step-Down Supply

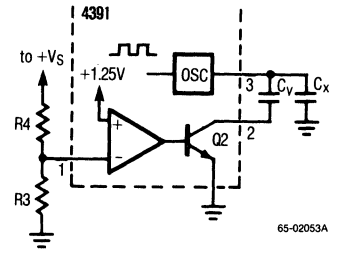


Figure 12. Voltage Dependent Oscillator

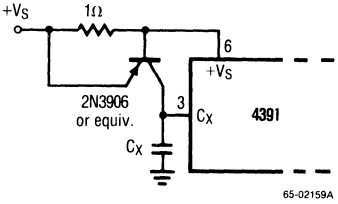
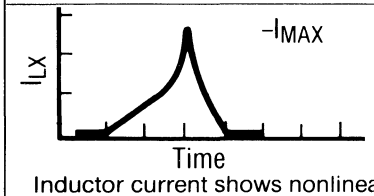
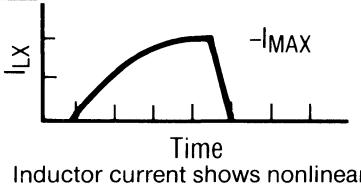
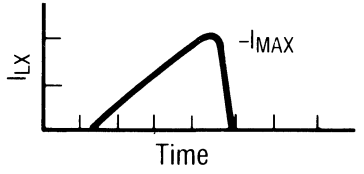


Figure 13. 4391 Short Circuit Current Limit

Troubleshooting Chart

Symptom	Possible Problems
Draws excessive supply current on start-up.	Inductance value too low. Operating frequency too low. Combination of low resistance inductor and high value filter capacitor — needs current limit circuit (Figure 13).
Output voltage is low.	Inductance value too high for F_O or core saturating.
Inductor "sings" with audible hum.	Not potted well or bolted loosely.
Lx pin appears noisy — scope will not synchronize.	Normal operating condition.
 Inductor current shows nonlinear waveform.	Inductor is saturating: 1. Core too small. 2. Core too hot. 3. Operating frequency too low.
 Inductor current shows nonlinear waveform.	Waveform has resistive component: 1. Wire size too small. 2. Power transistor lacks base drive. 3. Components not rated high enough. 4. Battery has high series resistance.
 Inductor current is linear until high current is reached.	External transistor lacks base drive or beta is too low.
Poor efficiency.	Core saturating. Diode or transistor: 1. Not fast enough. 2. Not rated for current level (high V_{CE} SAT). High series resistance. Operating frequency too high.
Motorboating (erratic current pulses).	Loop stability problem — needs feedback capacitor from V_{OUT} to pin 8 (100pF to 1000pF)

RC4194 Dual Tracking Voltage Regulators

Features

- Simultaneously adjustable outputs with one resistor to ±42V
- Load current — ±200 mA with 0.04% load regulation
- Internal thermal shutdown at T_J = +175°C
- External balance for $\pm V_O$ unbalancing
- 3W power dissipations

Description

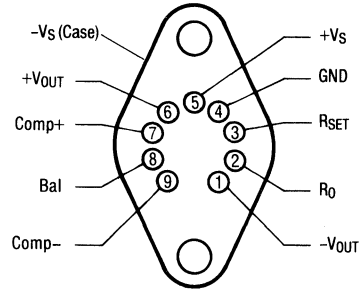
The RM4194 and RC4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200 mA. A single external resistor adjustment can be used to change both outputs between the limits of ±50 mV and ±42V.

These devices are designed for local "on-card" regulation, eliminating distribution problems associated with single-point regulation. To simplify application the regulators require a minimum number of external parts.

The device is available in three package types to accommodate various power requirements. The K (TO-66) power package can dissipate up to 3W at T_A = +25°C. The D 14-pin dual in-line will dissipate up to 1W and the N 14-pin dual in-line will dissipate up to 625 mW.

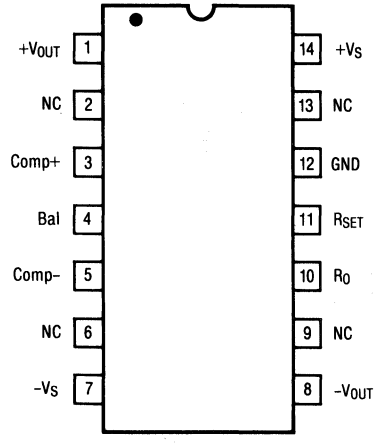
Connection Information

9-Lead
TO-66 Package
(Top View)



65-00199A

14-Lead
Plastic & Ceramic DIP
(Top View)



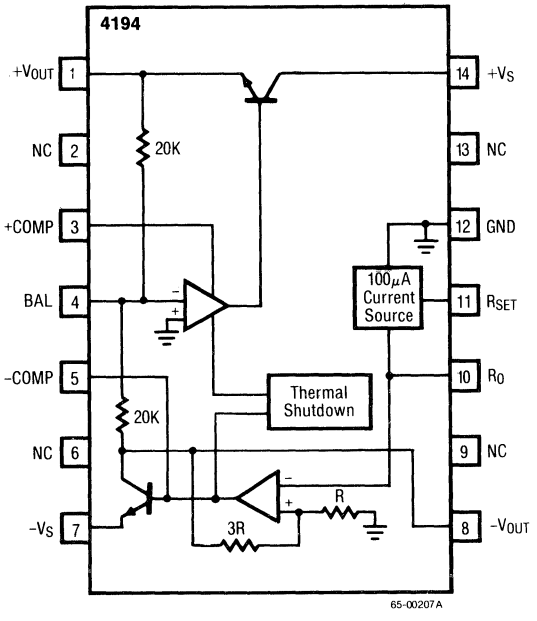
65-00200A

Ordering Information

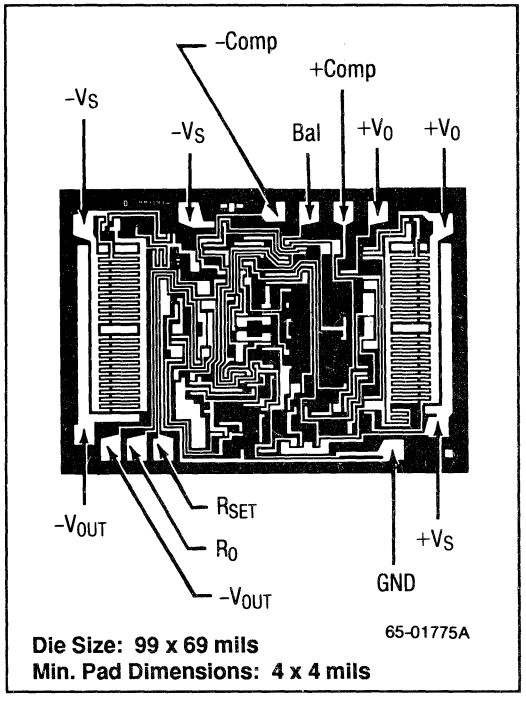
Part Number	Package	Operating Temperature Range
RC4194N	N	0°C to +70°C
RC4194D	D	0°C to +70°C
RC4194K	K	0°C to +70°C
RM4194D	D	-55°C to +125°C
RM4194D/883B	D	-55°C to +125°C
RM4194K	K	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14- lead ceramic DIP
K = 9-lead TO-66
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Functional Block Diagram



Mask Pattern



Die Size: 99 x 69 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Voltage
- RC4194 ..... ±35V
- RM4194 ..... ±45V

Supply Input to Output Voltage Differential
- RC4194 ..... ±35V
- RM4194 ..... ±45V

Load Current
- N Package ..... 100 mA
- D Package ..... 150 mA
- K Package ..... 250 mA

Operating Junction Temperature Range
- RC4194 ..... 0°C to +125°C
- RM4194 ..... -55°C to +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Soldering Temperature (60 sec) ..... +300°C

Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP	9-Lead TO-66 Metal Can
Max. Junction Temp.	125°C	175°C	150°C
Max. P_D T_A <50°C	468mW	1042mW	2381mW
Therm. Res θ_{JC}	—	60°C/W	7°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W	42°C/W
For T_A >50°C Derate at	6.25 mW/°C	8.38 mW/°C	23.81 mW/°C

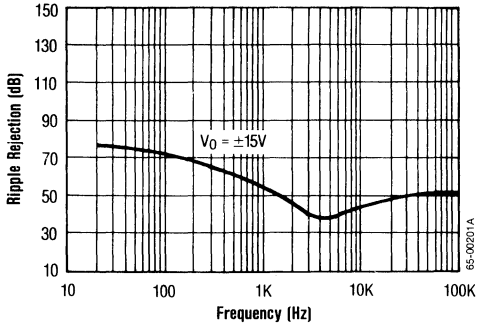
Electrical Characteristics ($\pm 5 \le V_{OUT} \le V_{MAX}$; $-V_{IN} \le -8V$; $I_L = \pm 1mA$; RM4194: $-55°C \le T_J \le +125°C$; RC4194: $0°C \le T_J \le +70°C$ unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
Line Regulation	$\Delta V_S = 0.1\ V_{IN}$		0.04	0.1	$\%V_{OUT}$
Load Regulation	4194K: $I_L < 200$ mA 4194D: $I_L < 100$ mA $\pm V_S = \pm(V_O + 5)V$		0.002	0.004	$\%V_O \times I_L$ (mA)
Output Voltage Drift With Temperature[3]					
Positive Output	$V_{OUT} = \pm 5V$		0.002	0.015	%/°C
Negative Output	$V_{OUT} = \pm 5V$		0.,003	0.015	%/°C
Supply Current[1] (Positive)	$V_S = \pm V_{MAX}$, $V_O = 0V$, $I_L = 0$ mA		+0.8	+2.5	mA
Supply Current[2] (Negative)	$V_S = \pm V_{MAX}$, $V_O = 0V$, IL = 0 mA		-1.8	-4.0	mA
Supply Voltage	RM4194	±9.5		±45	V
	RC4194	±9.5		±35	
Output Voltage Scale Factor	$R_{SET} = 71.5\ k\Omega$, $T_J = +25°C$ $V_S = \pm V_{MAX}$	2.38	2.5	2.62	kΩ/V
Output Voltage Range	RM4194: $R_{SET} = 71.5\ k\Omega$, $I_L = 25$ mA	0.05		±42	V
	RC4194: $R_{SET} = 71.5\ k\Omega$, $I_L = 25$ mA	0.05		±42	
Output Voltage Tracking			±0.4	±2.0	%
Ripple Rejection	F = 120 Hz, $T_J = +25°C$		70		dB
Input-Output Voltage Differential	$I_L = 50$ mA, $T_J = +25°C$	3.0			V
Short Circuit Current	$V_S = \pm 30V$, $T_J = +25°C$		300		mA
Output Noise Voltage	$C_L = 4.7\ \mu F$, $V_O = \pm 15V$ F = 10 Hz to 100 kHz		250		μV_{RMS}
Internal Thermal Shutdown			175		°C

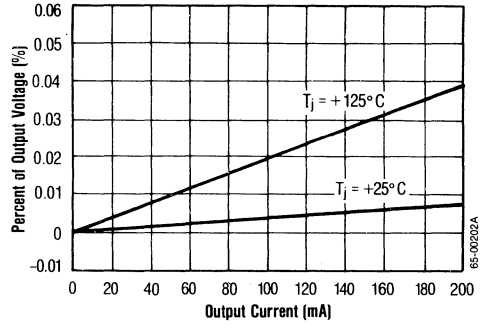
Notes:
1. The current drain will increase by $50\mu A/V_{OUT}$ on positive side and $100\mu A/V_{OUT}$ on negative side.
2. The specifications above apply for the given junction temperatures since pulse test conditions are used.
3. Output voltage temperature drift guaranteed by design.

Typical Performance Characteristics

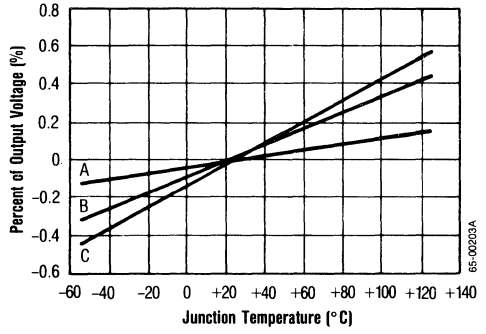
Ripple Rejection



Load Regulation vs. Output Current



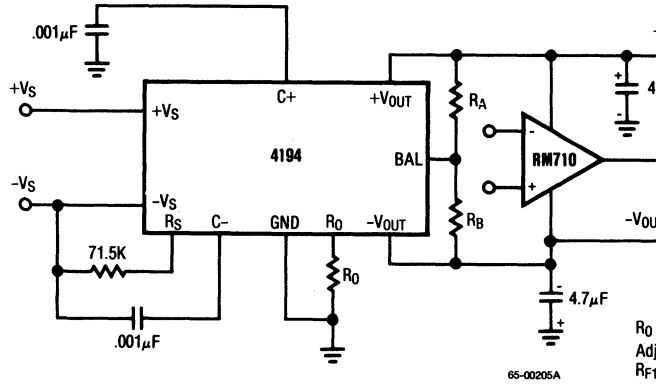
Output Voltage Tracking vs. Temperature



A = % Tracking of Output Voltage
B = T.C. for Positive Regulator
C = T.C. for Negative Regulator

Typical Applications

Unbalanced Output Voltage — Comparator Application

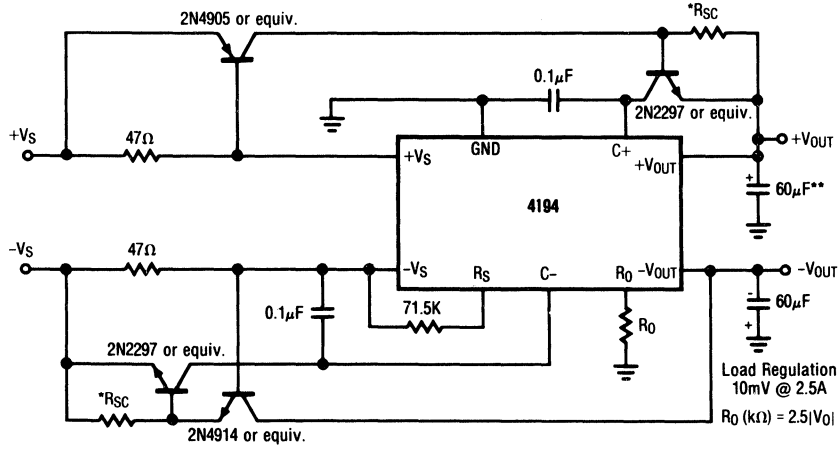


R_O (kΩ) = 2.5 ($-V_{OUT}$)
Adjust R_O for $-V_{OUT}$ = −6V (15kΩ)
$R_{F1} = R_{F2}$ = 20kΩ (see schematic)

$$|+V_{OUT}| = |-V_{OUT}| \frac{R_{F1} \,||\, R_A}{R_{F2} \,||\, R_B}$$

$R_A = \infty$ when $|+V_{OUT}| > |-V_{OUT}|$
$R_B = \infty$ when $|+V_{OUT}| < |-V_{OUT}|$
For $+V_{OUT}$ = 12 when $-V_{OUT}$ = 6V
$R_A = \infty$
R_B = 20kΩ

High Output Application



$$*R_{SC} = \frac{0.7}{I_{SC}}$$

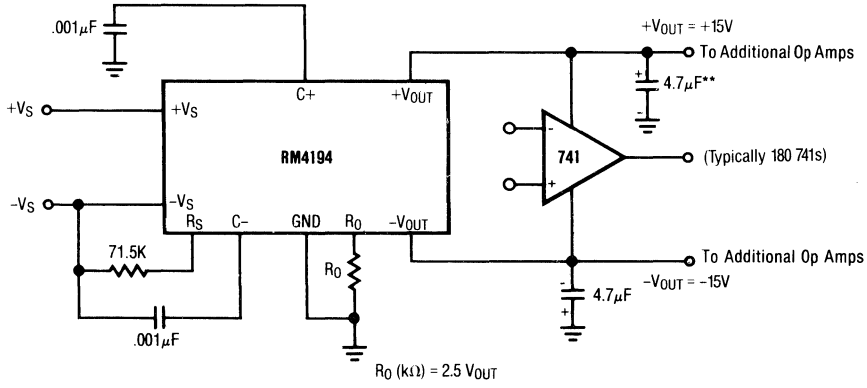
Note: Compensation and bypass capacitor connections should be close as possible to the 4194.

**Optional usage — not as critical as $-V_O$ bypass capacitors.

65-00206A

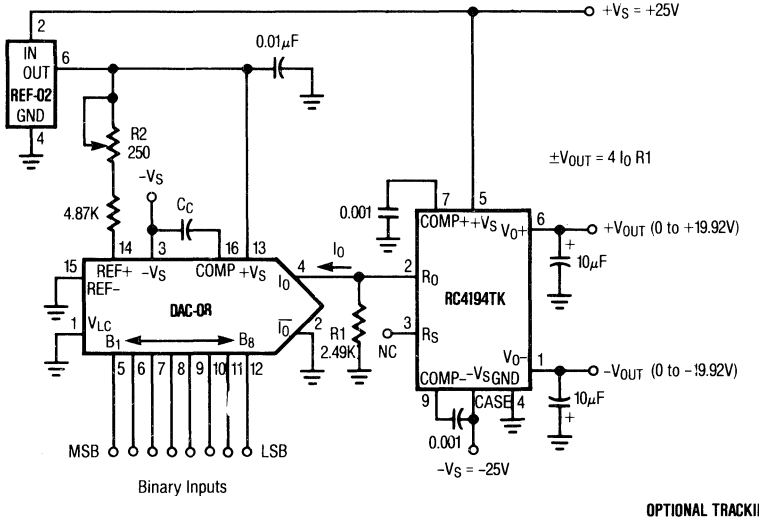
Typical Applications (Continued)

Balanced Output Voltage — Op Amp Application

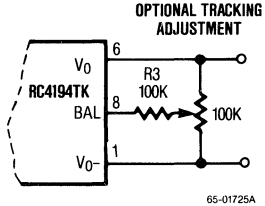


65-00204A

Digitally Controlled Dual 200mA Voltage Regulator



Adjust R2 for -19.92V at $-V_{OUT}$ with all "1s" at binary inputs, then optionally adjust R3 for +19.92V at $+V_{OUT}$



65-01725A

4194 Switchable Power Supply

The outputs of the 4194 can be simultaneously switched on or off under logic control as shown in Figure 1. In the "off" state, the outputs will be forced to a minimum voltage, or about ±20 mV, rather than becoming open-circuit. the turn-on time, with the outputs programmed to ±12V, is approximately 200 µS. This circuit works by forcing the R_O pin to ground with an analog switch. Refer to the 4194 internal schematic diagram. A reference voltage that regulates with respect to $-V_S$ is generated at the R_S pin by the zener diode Q12 and the buffer circuit of Q11 and Q13. When the external 71.5k R_S resistor is connected between the R_S pin and $-V_S$, a precision current of 100 µA is generated which then flows into Q13's collector. Since Q13's collector is tied to the R_O pin, the 100 µA current will develop a ground-referenced voltage drop proportional to the value of R_O, which is then amplified by the internal error amplifier. When the analog switch in Figure 1 turns on, it effectively shorts out R_O and causes 0V to be applied to the error amplifier. The output voltage in the off state will be approximately ±20 mV. If a higher value (50 to 100 mV) is acceptable, then the DG201 FET switch can be replaced with a low-cost small signal transistor, as shown in the alternate switch configuration.

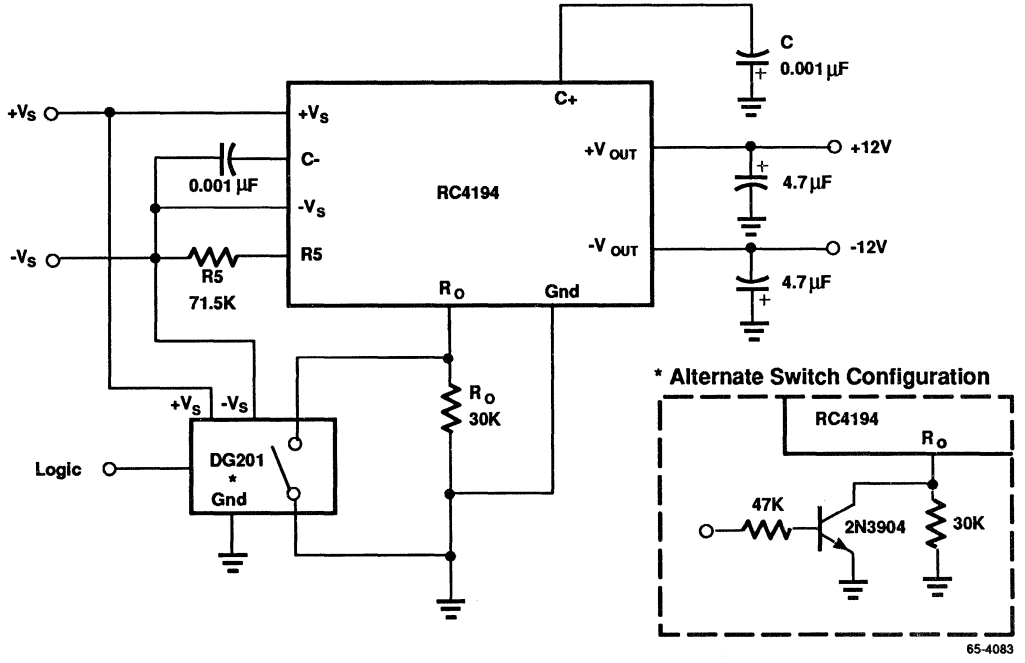


Figure 1. ±12V Switchable Power Supply

Compensation

For most applications, the compensation technique shown in the data sheet is sufficient. The positive regulator section of the 4194 is compensated by a 0.001 µF ceramic disc capacitor from the C+ terminal to ground. The negative regulator requires compensation at two points. The first is the C- pin, which should have 0.001 µF to the $-V_{IN}$ pin, or case. A ceramic disc is best here also. The second compensation point for the negative side is the $-V_{OUT}$ terminal, which ideally should be a 4.7 µF solid tantalum capacitor with enough reserve voltage capacity to avoid the momentary shorting and reforming which can occur with tantalum caps. For systems where the cost of a solid tantalum capacitor cannot be justified, it is usually sufficient to use an aluminum capacitor with a 0.03 µF ceramic disc in parallel to bypass high frequencies. In addition, if the rectifier filter capacitors have poor high frequency characteristics (like aluminum electrolytics) or if any impedance is in series with the $+V_{IN}$ and $-V_{IN}$ terminals, it is necessary to bypass these two points with 0.01 µF ceramic disc capacitors. Just as with monolithic op amps, some applications may not require these bypass caps, but if in doubt, be sure to include them.

All compensation and bypass caps should have short leads, solid grounds, and be located as close to the RM/RC4194 as possible. Refer to Figure 2 for recommended compensation circuitry.

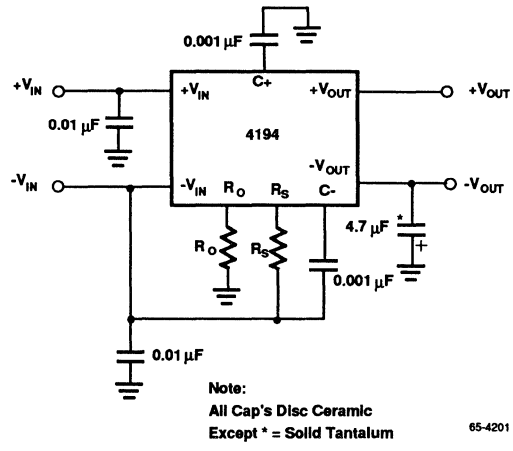


Figure 2. 4194 Recommended Compensation

Protection

In systems using monolithic voltage regulators, a number of conditions can exist which, left uncorrected, will destroy the regulator. Fortunately, regulators can easily be protected against these potentially destructive conditions. Monolithic regulators can be destroyed by any reversal of input or output voltage polarity, or if the input voltage drops below the output voltage in magnitude. These conditions can be caused by inductive loads at the inputs or outputs of the regulator. Other problems are caused by heavy loads at the unregulated inputs to the regulator, which might cause the input voltage to drop below the output voltage at turn-off. If any of the preceding problem conditions are present in your system, it is recommended that you protect the regulator using diodes. These diodes should be high speed types capable of handling large current surges. Figure 3 shows all six of the possible protection diodes. The diodes at the inputs and outputs prevent voltages at those points from becoming reversed. Diodes from outputs to inputs prevent the output voltage from exceeding the input voltage. Chances are that the system under consideration will not require all six diodes, but if in doubt, be sure to include them.

Brownout Protection

The 4194/4195 is one of the most easily applied and trouble-free monolithic ICs available. When used within the data sheet ratings (package power dissipation, maximum output cur-

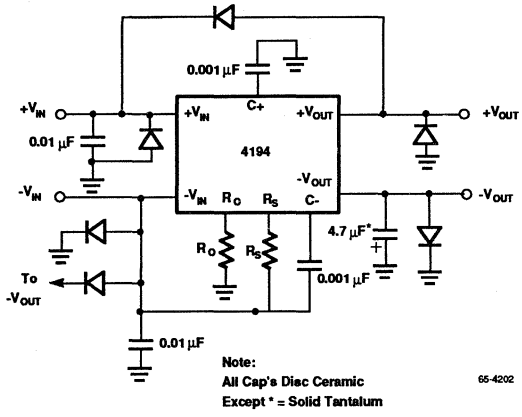


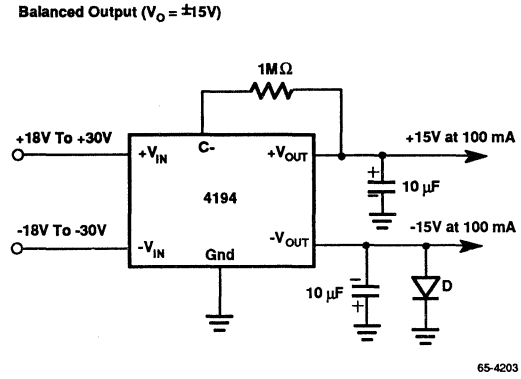
Figure 3. 4194 Regulator Showing All Protective Diodes

rent, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15V for powering linear ICs.

Sometimes occasions arise in which the 4194/4195 ratings must be exceeded. One example is the "brownout". During a brownout, line voltages may be reduced to as low as 75 VRMS, causing the input voltage to the 4194/4195 to drop below the minimum dropout voltage. When this happens, the negative output voltage can go to positive. The maximum amount of current available is approximately 5 mA.

In general this is not enough current to damage most ICs which the 4194/4195 might be supplying, but it is a potentially destructive condition. Fortunately, it is easy to protect against. As shown in the typical application circuit below, a diode, D, can be connected to the negative output.

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative at all times is the 1 mΩ resistor connected between the +15V output and the C- terminal. This resistor will then supply drive to the negative output transistor, causing it to saturate to -V1 during the brownout.



Heatsinking for 4194 and 4195

Voltage Regulators are power devices which are used in a wide range of applications.

When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. Both the 4194 and 4195 have this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.*

The following is the basic equation for junction temperature:

*In allowing for process deviations, the user should work with a maximum allowable function temperature of 150°C.

$$T_J = T_A + P_D \theta_{J-A} \quad (1)$$

where
T_J = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
θ_{J-A} = thermal resistance from junction to ambient air (°C/W)

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q \quad (2)$$

where
V_{IN} = input voltage
V_{OUT} = regulated output voltage
I_O = load current
I_Q = quiescent current drain

Let's look at an application where a user is trying to determine whether the RM4194 in a high temperature environment will need a heatsink.

Given:

T_J at thermal shutdown = 150°C

T_A = 125°C

θ_{J-A} = 41.6°C/W, K (TO-66) pkg.

V_{IN} = 40V

V_{OUT} = 30V

I_Q = 1 mA + 75 μA/V_{OUT} x 30V
= 3.25 mA *

$$\theta_{J-A} = \frac{T_J - T_A}{P_D}$$

$$P_D = \frac{T_J - T_A}{\theta_{J-A}} = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_J - T_A}{\theta_{J-A}(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{50°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

= 50 mA - 13 mA ≃ 47 mA

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In equation 1, θ_{J-A} can be broken into the following components:

$$\theta_{J-A} = \theta_{J-C} + \theta_{C-S} + \theta_{S-A}$$

where
θ_{J-C} = junction-to-case thermal resistance
θ_{C-S} = case-to-heatsink thermal resistance
θ_{S-A} = heatsink-to-ambient thermal resistance

In the above example, let's say that the user's load current is 200 mA and he wants to calculate the combined θ_{C-S} and θ_{S-A} he needs:

Given: I_O = 200 mA,

$$\theta_{J-A} = \frac{T_J - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200\ mA + 40 \times 3.25 \times 10\text{-}3}$$

= 11.75°C/W

* The current drain will increase by 50μA/V_{OUT} on positive side and 100μA/V_{OUT} on negative side.

Given θ_{J-C} = 7.15°C/W for the 4194 in the K package,

$$\theta_{C-S} + \theta_{S-A} = 11.75°C/W - 7.15°C/W$$

$$= 4.6°C/W$$

When using heatsink compound with a metal-to metal interface, a typical θ_{C-S} = 0.5°C/W for the K package. The remaining θ_{S-A} of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

Table 1. Commercial Heatsink Selection Guide

No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

θ_{S-A}*(°C/W)	Manufacturer/Series or Part Number
	TO-66 Package
0.31-1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0 - 3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0 - 5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3-3-2
5.0 - 7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver— V3-5-2
7.0 - 10.0	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA, uP Staver — V1-3, V1-5, V3-3, V3-5, V3-7
10.0-25.0	Thermalloy — 6-13, 6014, 6015, 6103, 6104, 6105, 6117
	TO-99 Package
12.0 - 20.0	Wakefield — 260 Thermalloy — 1101, 1103 Staver — V3A-5
20.0 - 30.0	Wakefield — 209 Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC — LP Staver — F5-5

* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

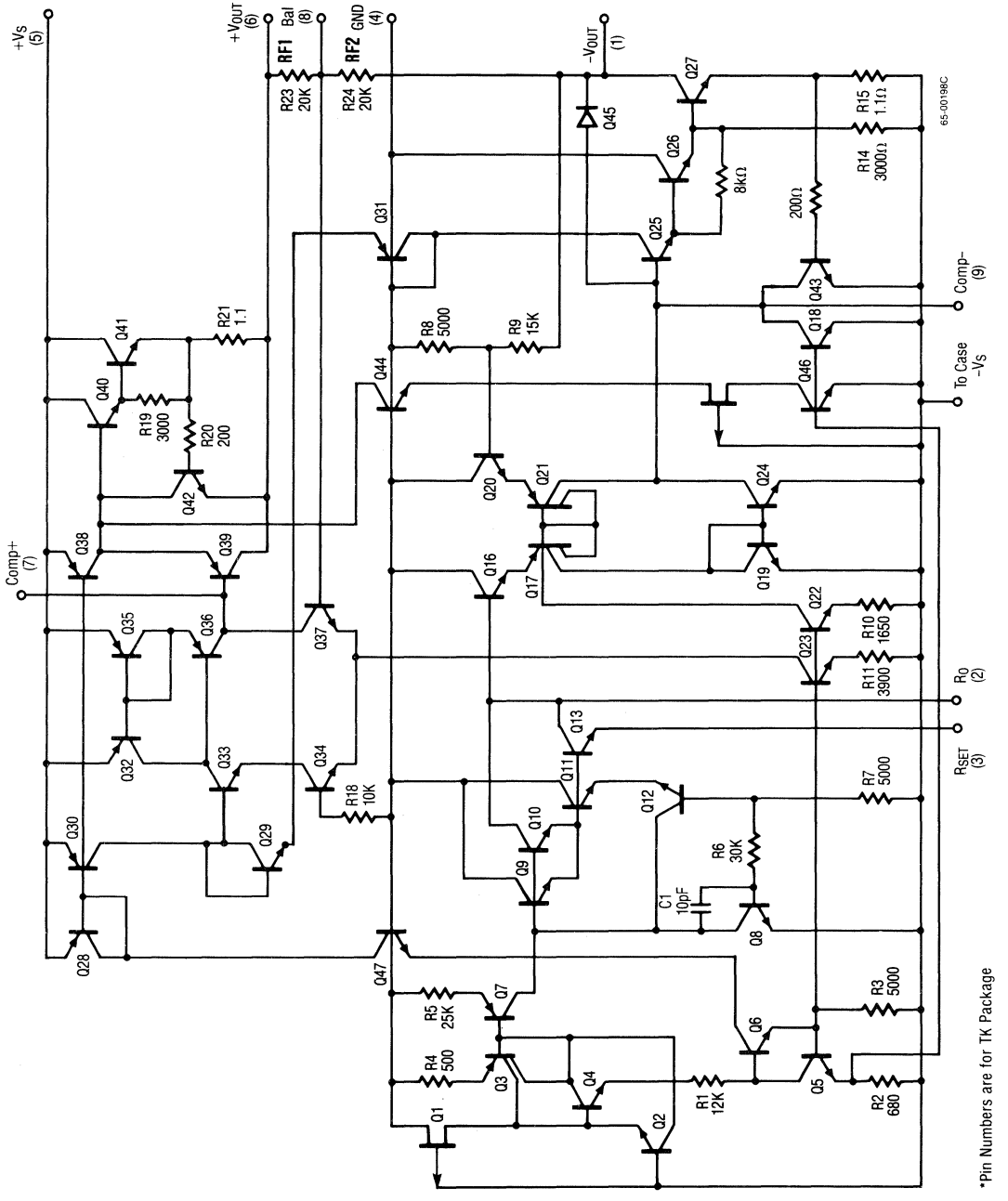
Table 1. Commercial Heatsink Selection Guide — Continued

θ_{S-A}*(°C/W)	Manufacturer/Series or Part Number
30.0 - 50.0	Wakefield — 207 Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264 Staver — F5-5, F6-5
	Dual-Inline Package
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LIC
60	Wakefield — 650, 651

* All values are typical as given by manufacturer or as determined from characteristic curves supplied by manufacturer.

Staver Co., Inc.: 41-51 N Saxon Ave., Bay Shore, NY 11706
IERC: 135 W Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

Schematic Diagram



RC4195 Fixed ±15V Dual Tracking Voltage Regulator

Features

- ±15V operational amplifier power at reduced cost and component density
- Thermal shutdown at Tj = +175°C in addition to short circuit protection
- Output currents to 100 mA
- May be used as single output regulator with up to +50V output
- Available in TO-66, TO-99 and 8-Pin Plastic Mini-DIP
- No external frequency compensation required

Description

The RC/RM4195 is a dual polarity tracking regulator designed to provide balanced positive and negative 15V output voltages at currents up to 100 mA. this device is designed for local "on-card" regulation, eliminating distribution problems associated with single point regulation. The regulator is intended for ease of application. Only two external components are required for operation (two 10 µF bypass capacitors).

The device is available in three package types to accommodate various applications requiring economy, high power, dissipation, and reduced component density.

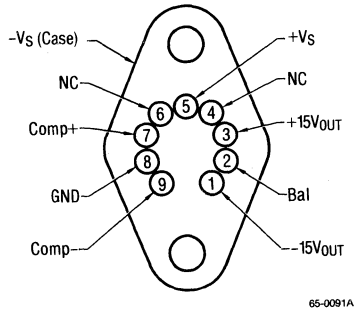
Ordering Information

Part Number	Package	Operating Temperature Range
RC4195N	N	0°C to +70°C
RC4195T	T	0°C to +70°C
RC4195K	K	0°C to +70°C
RM4195T	T	-55°C to +125°C
RM4195T/883B	T	-55°C to +125°C
RM4195TK	K	-55°C to +125°C
RM4195D	D	-55°C to +125°C
RM4195D/883B	D	-55°C to +125°C

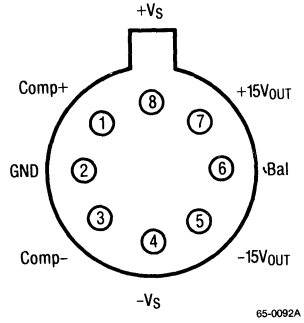
Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can TO-99
K = 9-lead power TO-66
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

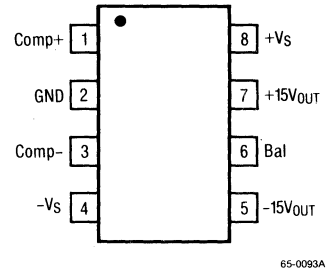
TO-66 Metal Can
(Top View)



TO-99 Metal Can
(Top View)



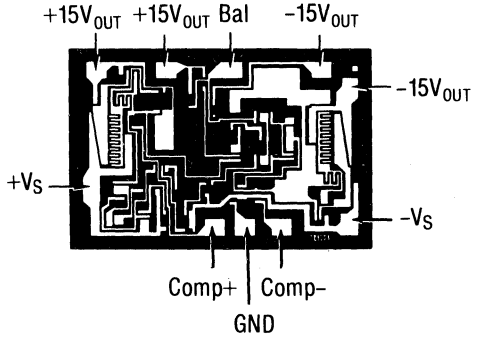
8-Lead DIP
(Top View)



Absolute Maximum Ratings

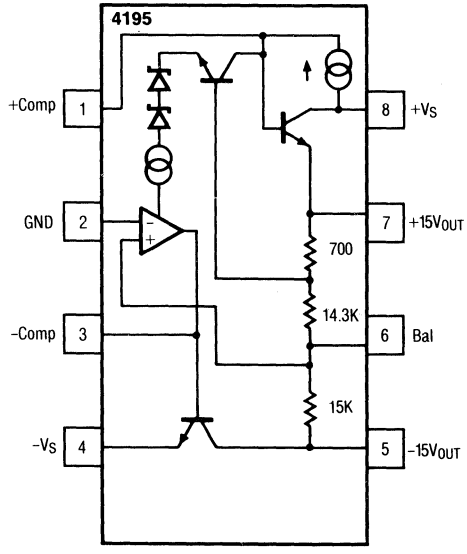
Supply Voltage ($\pm V_S$) to Ground ..... ±30V
Load Current
TK Package ..... 150 mA
T and N Package ..... 100 mA
Storage Temperature
Range ..... -65°C to +150°C
Operating Junction Temperature Range
RM4195 ..... -55°C to +150°C
RC4195 ..... 0°C to +125°C
Lead Soldering Temperature
(DIP, LCC, TO-99; 60 sec) ..... +300°C

Mask Pattern



Die Size: 49 x 74 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram



Pin out for dual in-line package shown.

65-00089A

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead TO-99 Metal Can	9-Lead TO-66 Metal Can	8-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C	150°C	175°C
Max. P_D T_A <50°C	468mW	658mW	2381mW	833mW
Therm. Res θ_{JC}	—	50°C/W	7°C/W	45°C/W
Therm. Res. θ_{JA}	160°C/W	190°C/W	42°C/W	150°C/W
For T_A >50°C Derate at	6.25 mW/°C	5.26 mW/°C	23.81 mW/°C	8.33 mW/°C

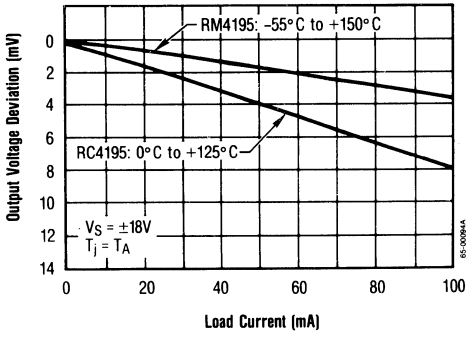
Electrical Characteristics (I_L = ±1mA, V_S = ±20V, C_L = 10μF
RM4195: -55°C ≤ T_j ≤ +125°C; RC4195: 0°C ≤ T_j ≤ +70°C unless otherwise specified)[1]

Parameters	Test Conditions	RC/RM4195 Min	RC/RM4195 Typ	RC/RM4195 Max	Units
Line Regulation	V_S = ±18V to ±30V		2	20	mV
Load Regulation	I_L = 1mA to 100mA		5	30	mV
Output Voltage Drift With Temperature			0.005	0.015	%/°C
Supply Current	V_S = ±30V, I_L = 0mA		±1.5	±4.0	mA
Supply Voltage		18		30	V
Output Voltage	T_j = +25°C	14.5	15.0	15.5	V
Output Voltage Tracking			±50	±300	mV
Ripple Rejection	f = 120Hz, T_j = +25°C		75		dB
Input-Output Voltage Differential	I_L = 50mA	3			V
Short Circuit Current	T_j = +25°C		220		mA
Output Voltage Noise	T_j = +25°C, f = 100Hz to 10kHz		60		μV_{RMS}
Internal Thermal Shutdown			175		°C

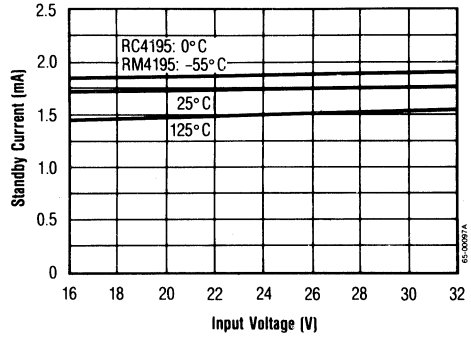
Notes: 1. The specifications above apply for the given junction temperature since pulse test conditions are used.

Typical Performance Characteristics

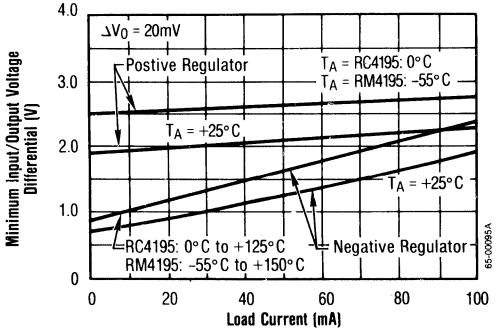
Output Load Regulation



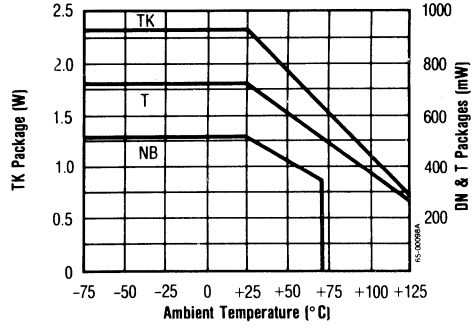
Standby Current Drain



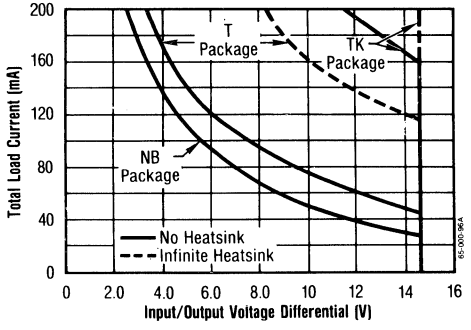
Regulator Dropout Voltage



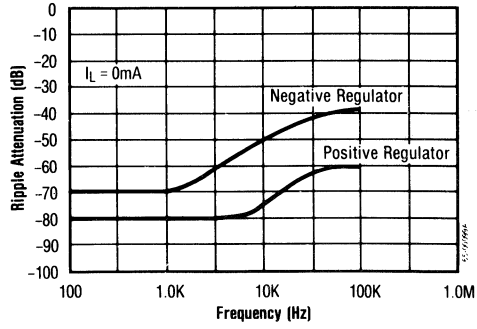
Power Dissipation



Maximum Current Capability

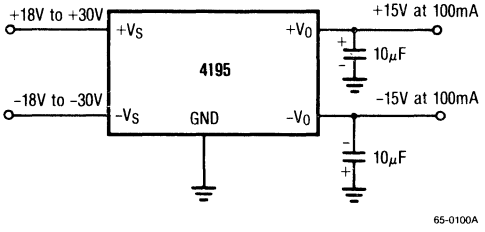


Ripple Rejection

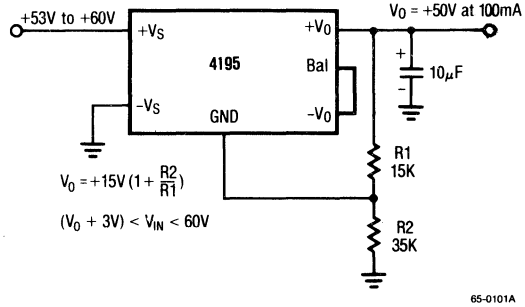


Typical Applications

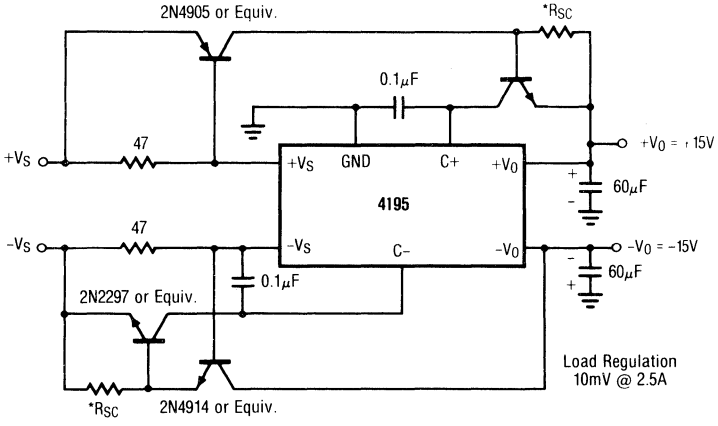
Balanced Output ($V_O = \pm 15V$)



Positive Single Supply ($+15V < V_O < +50V$)

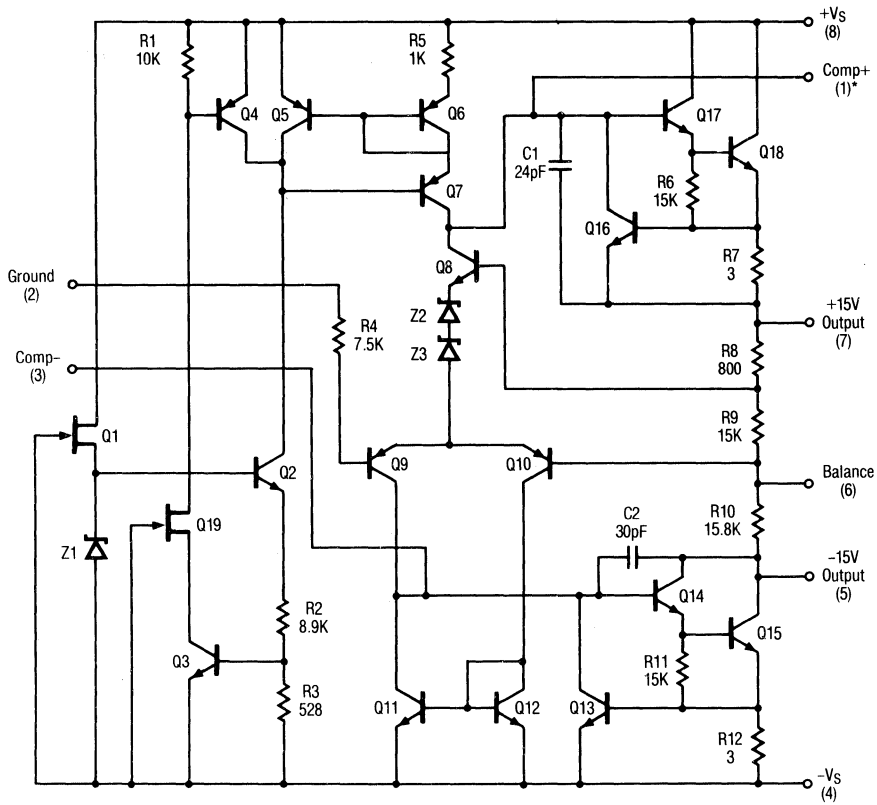


High Output Current



$$*R_{SC} = \frac{0.7}{I_{SC}}$$

Schematic Diagram



*Pin numbers are for 8-pin packages

65-0090B

SECTION 10
GROUND FAULT INTERRUPTERS

LM1851 Ground Fault Interrupter

Features

- Direct interface to SCR
- Adjustable fault current threshold
- Adjustable fault current integration time
- Complies with U.S. UL943 standard
- Operates under line reversal; both load vs. line and hot vs. neutral
- Detects grounded neutral faults
- Internal shunt regulator (26V)
- Small outline (SO-8) package available

Description

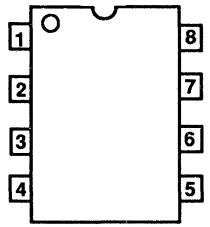
The LM1851 is a controller for ac outlet ground fault interrupters. These devices detect hazardous grounding conditions (example: a pool of water and electrical equipment connected to opposite phases of the ac line) in consumer and industrial environments. The output of the IC triggers an external SCR, which in turn opens a relay circuit breaker to prevent a harmful or lethal shock.

Full advantage of the U.S. UL943 timing specification is taken to ensure maximum immunity to false triggering due to line noise. A special feature is found in circuitry that rapidly resets the integrating timing capacitor in the event that noise pulses introduce unwanted charging currents. Also, a flip-flop is included that ensures firing of even a slow circuit breaker relay on either half-cycle of the line voltage when external full wave rectification is used.

The application circuit can be configured to detect both normal faults (hot wire to ground) and grounded neutral faults.

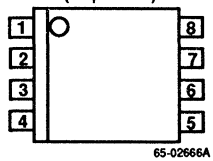
Connection Information

8-Lead Dual In-Line Package (Top View)



65-03206

8-Lead Plastic Dual In-Line SO-8 (Top View)



65-02666A

Pin	Function
1	SCR Trig
2	(-) Input
3	(+) Input
4	Gnd
5	Amp Out
6	RSET
7	CT
8	$+V_S$

Ordering Information

Part Number	Package	Operating Temperature Range
LM1851N	N	-40°C to +70°C
LM1851M	M	-40°C to +70°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

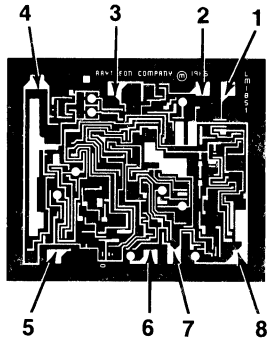
Absolute Maximum Ratings

Shunt Current ..... 19 mA
Power Dissipation ..... 570 mW
Operating Temperature
Range ..... -40°C to +70°C
Storage Temperature
Range ..... -65°C to +150°C
Lead Soldering Temperature
(SO-8, 10 sec) ..... +260°C
Lead Soldering Temperature
(DIP, 60 sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Small Outline
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A < 50°C	468 mW	300 mW
Therm. Res θ_{JC}	—	—
Therm. Res θ_{JA}	160°C/W	240°C/W
For T_A < 50°C Derate at	6.25 mW/°C	4.17 mW/°C

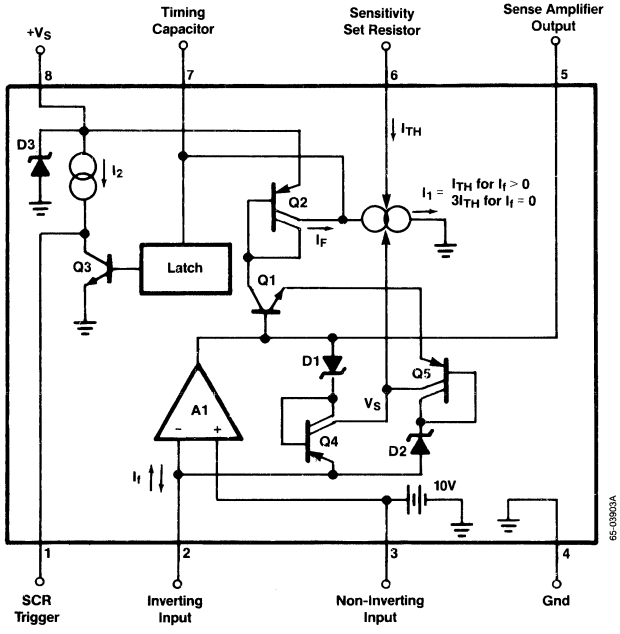
Mask Pattern



65-03978A

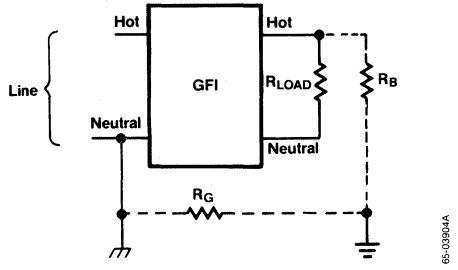
Die Size: 69 x 59 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram

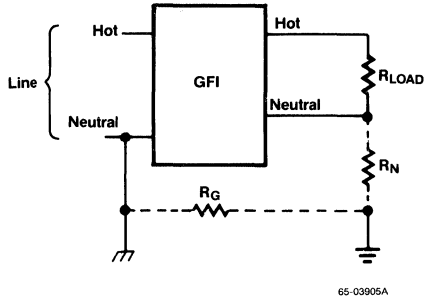


Definition of Terms

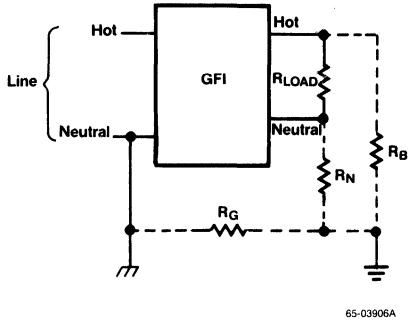
Normal Fault: An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines.



Grounded Neutral Fault: An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines.



Normal Fault Plus Grounded Neutral Fault: The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines.



DC Electrical Characteristics (T_A = +25°C, I_{SHUNT} = 5 mA)

Parameters	Test Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1 With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1 Without Fault		100	240	mV
Output Saturation Resistance	Pin 1 Without Fault		100		Ω
Output External Current Sinking Capability	Pin 1 Without Fault, $V_{pin\ 1}$ Held to 0.3V [3]	2	5		mA
Noise Integration Sink Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

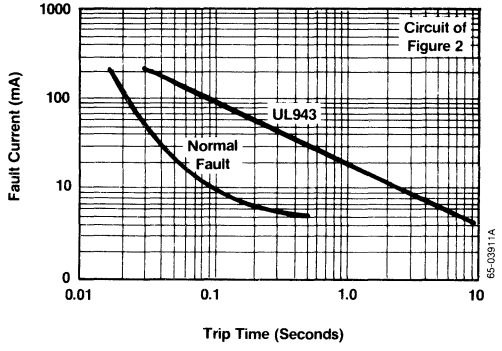
AC Electrical Characteristics (T_A = +25°C, I_{SHUNT} = 5 mA)

Parameter	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity	See Figure 1 [2]	3	5	7	mA
Normal Fault Trip Time	500Ω Fault (see Fig. 2) [1]		18		mS
Normal Fault With Grounded Neutral Fault Trip Time	500Ω Normal Fault, 2Ω Neutral (see Fig. 2) [1]		18		mS

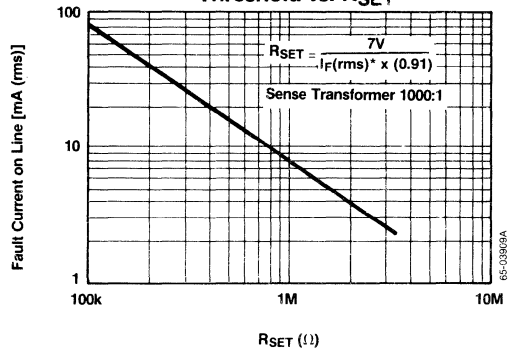
Notes:
1. Average of 10 trials.
2. Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity will be necessary.
3. This externally applied current is in addition to the internal "output drive current" source.

Typical Performance Characteristics (T_A = +25°C)

Average Trip Time vs. Fault Current

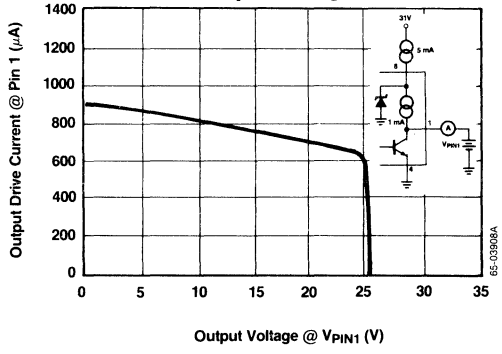


Normal Fault Current Threshold vs. R_{SET}

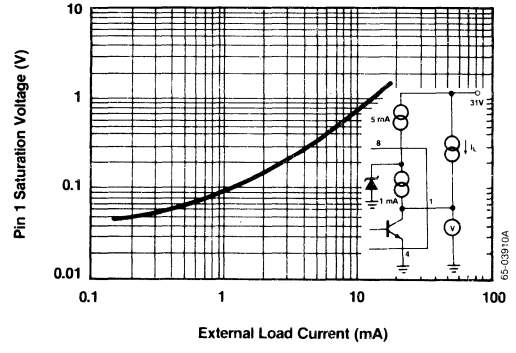


*See Block Diagram

Output Drive Current vs. Output Voltage



Pin 1 Saturation Voltage vs. External Load Current, I_L



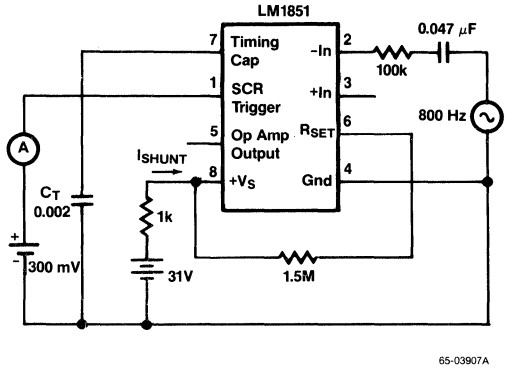


Figure 1. Normal Fault Sensitivity Test Circuit

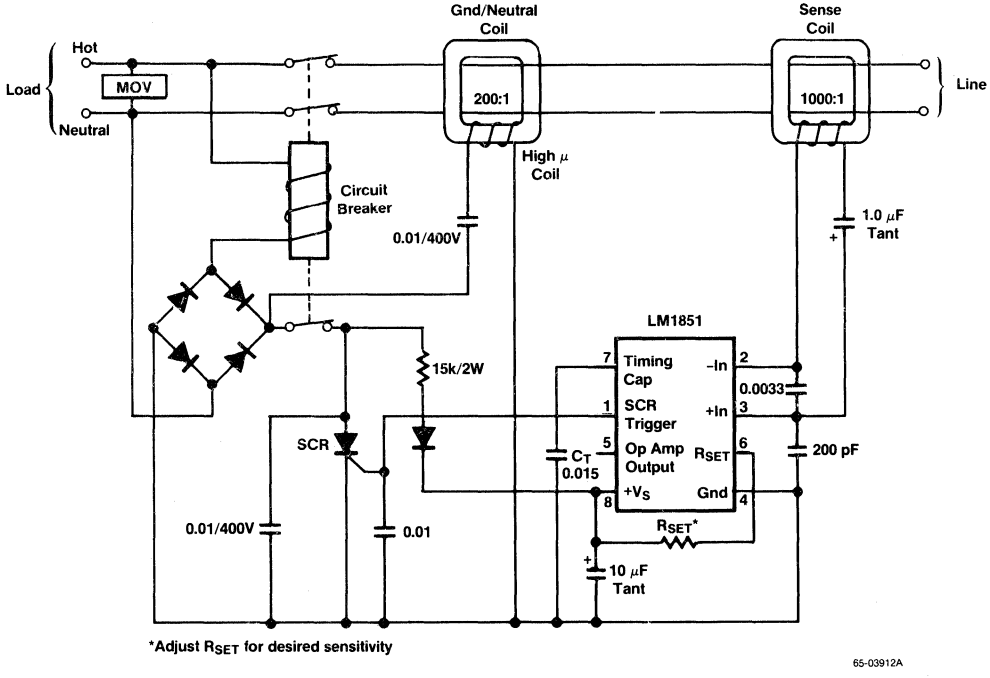


Figure 2. 120 Hz Neutral Transformer Application

Principles of Operation

(Refer to Functional Block Diagram)

The voltage at the supply pin is clamped to +26V by the internal shunt regulator D3. This shunt regulator also generates an artificial ground voltage for the noninverting input of A1 (shown as a +10V source). A1, Q1, and Q2 act as a current mirror for fault current signals (which are derived from an external transformer). When a fault signal is present, the mirrored current charges the external timing capacitor until its voltage exceeds the latch trigger threshold (typically 17.5V). When this threshold is exceeded, the latch engages and Q3 turns off, allowing I_2 to drive the SCR connected to pin 1.

Extra circuitry in the feedback path of A1 works with the switched current source I_1 to remove any charge on C_T induced by noise in the transformer. If no fault current is present, then I_1 discharges C_T with a current equal to 3 I_{TH}, where I_{TH} is the value of current set by the external R_{SET} resistor. If fault signals are present at the input of A1 (which is held at virtual ground, +10V), one of the two current mirrors in the feedback path of A1 (Q4 and Q5) will become active, depending on which half-cycle the fault occurs in. This action will raise the voltage at V_S, switching I_1 to a value equal to I_{TH}, and reducing the discharge rate of C_T to better allow fault currents to charge it.

Notice that I_{TH} discharges C_T during both half-cycles of the line, while I_F only charges C_T during the half-cycle in which I_F exits pin 2 (since Q1 will only carry fault current in one direction). Thus, during one half-cycle, I_F-I_{TH} charges C_T, while during the other half-cycle I_{TH} discharges it.

Application Circuit

A typical ground fault interrupter circuit is shown in Figure 2. It is designed to operate on 120 VAC line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the dc power required by the IC. A 1 μF capacitor at pin 8 used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load. At this time no fault current flows and the C_T discharge current increases from I_{TH} to $3I_{TH}$ (see Block Diagram). This quickly resets both the timing capacitor and the output latch. The circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the hot and neutral lines, is stepped down by 1000 and fed into the input pins of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH} = \frac{7V}{R_{SET}} \div 2 \qquad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH} = \frac{I_{F(rms)}}{2} \times 0.91 \qquad (2)$$

where $I_{F(rms)}$ is the rms input fault current to the operational amplifier and the factor of 2 is due to the fact that I_F charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have:

$$R_{SET} = \frac{7V}{I_{F(rms)} \times 0.91} \qquad (3)$$

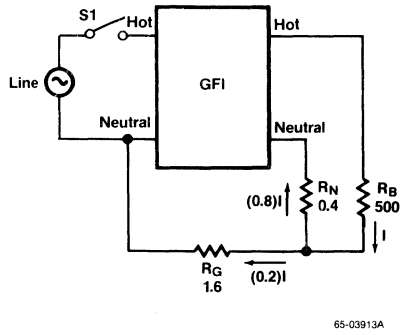
For example, to obtain 5 mA(rms) sensitivity for the circuit in Figure 2 we have:

$$R_{SET} = \frac{7V}{\frac{5\ mA \times 0.91}{1000}} = 1.5\ M\Omega \qquad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA to 6 mA, provision should be made to adjust R_{SET} with a potentiometer.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_T. Due to the large number of variables involved, proper selection of C_T is best done empirically. The following design example should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GFI start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagramatically below.



UL943 specifies ≤ 25 ms average trip time under these conditions. Calculation of C_T based upon charging currents due to normal fault only is as follows:

- Start with a ≤ 25 ms specification. Subtract 3 ms GFI turn-on time (15k and 1 μF). Subtract 8 ms potential loss of one half-cycle due to fault current sense of half-cycles only.
- Subtract 4 ms time required to open a sluggish circuit breaker.
- This gives a total ≤ 10 ms maximum integration time that could be allowed.
- To generate 8 ms value of integration time that accommodates component tolerances and other variables:

$$C_T = \frac{1 \times T}{V} \qquad (5)$$

where T = integration time
V = threshold voltage
I = average fault current into C_T

$$I = \underbrace{\left(\frac{120\ V_{AC(rms)}}{R_B}\right)}_{\substack{\text{heavy fault current generated (swamps } I_{TH})}} \times \underbrace{\left(\frac{R_N}{R_G + R_N}\right)}_{\substack{\text{portion of fault current shunted around GFI}}}$$

$$\times \underbrace{\left(\frac{1\ \text{turn}}{1000\ \text{turns}}\right)}_{\substack{\text{current division of input sense transformer}}} \times \underbrace{\left(\frac{1}{2}\right)}_{\substack{C_T \text{ charging on half-cycles only}}} \times \underbrace{(0.91)}_{\substack{\text{rms to average conversion}}} \qquad (6)$$

therefore:

$$C_T = \frac{\left[\left(\frac{120}{500}\right) \times \left(\frac{0.4}{1.6 + 0.4}\right) \times \left(\frac{1}{1000}\right) \times \left(\frac{1}{2}\right) \times (0.91)\right] \times 0.0008}{17.5}$$

$$C_T = 0.01\ \mu F \qquad (7)$$

In practice, the actual value of C_T will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C_T.

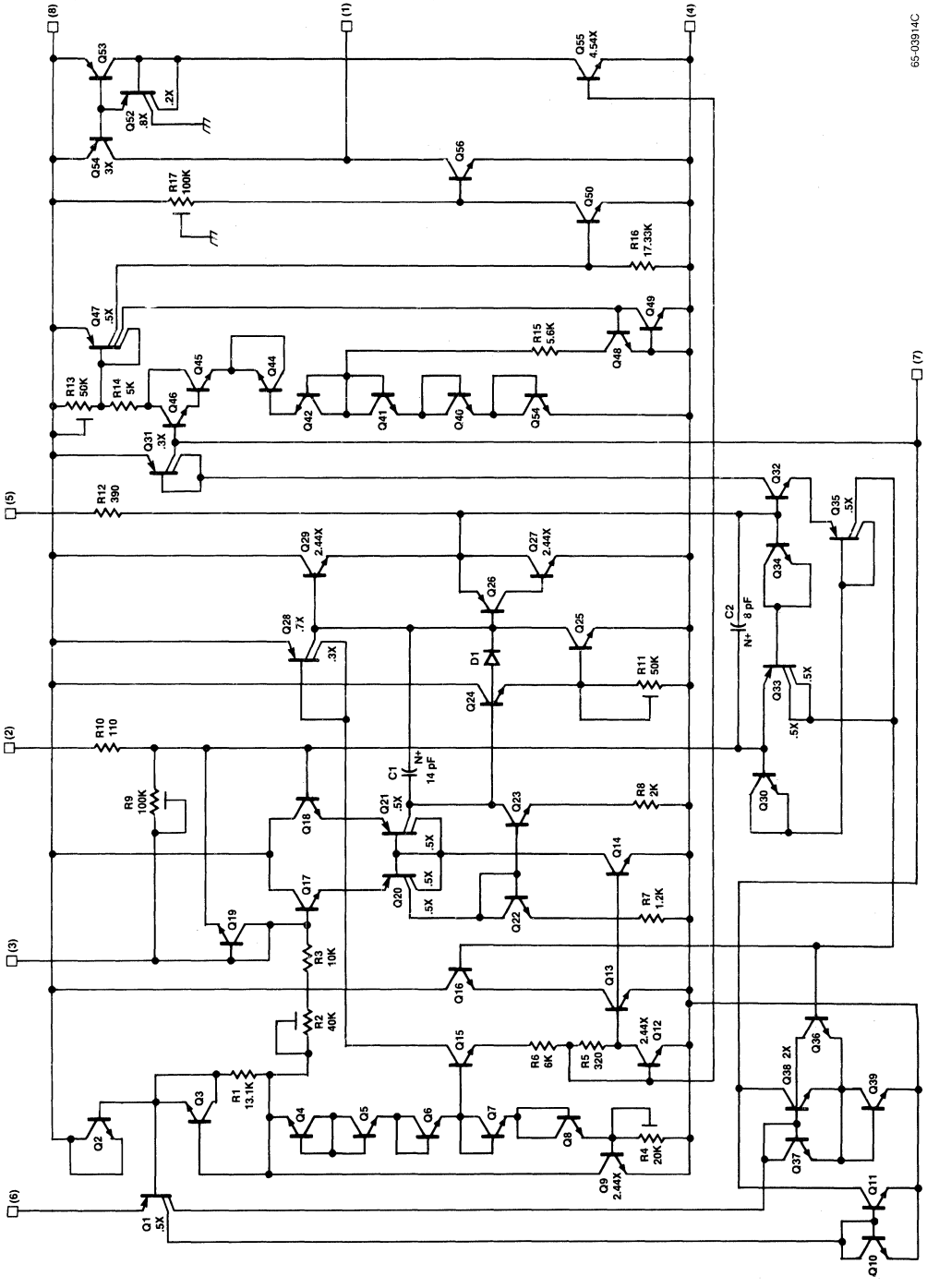
For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacitor can be used and better noise immunity obtained. The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In Figure 2, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Transformers may be obtained from Magnetic Metals, Inc., 21st Street and Hayes Street, Camden, NJ 08101 — (609) 964-7842.

Schematic Diagram



RV4143, 4144 Ground Fault Interrupters

Features

- Direct interface to SCR
- Supply voltage derived from ac line — 26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets U.L. 943 standards

Description

The RV4143 and RV4144 are controllers for ac outlet ground fault interrupters. These devices detect hazardous grounding conditions, such as a pool of water and equipment connected to opposite phases of the ac line, and open circuits the line before a harmful or lethal shock occurs.

Contained internally are a 26V zener shunt regulator, an op amp, and an SCR driver. With the addition of two sense coils, a bridge rectifier, an SCR, and a relay the 4143 or 4144 will detect and protect against both hot wire to ground and neutral wire to ground faults. The simple layout and conventional design ensure ease of application and long term reliability.

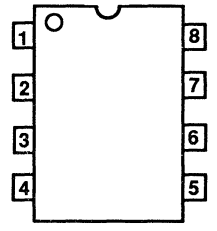
Ordering Information

Part Number	Package	Operating Temperature Range
RV4143N	N	-35°C to +85°C
RV4144N	N	-35°C to +85°C

Notes:
N = 8-lead plastic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

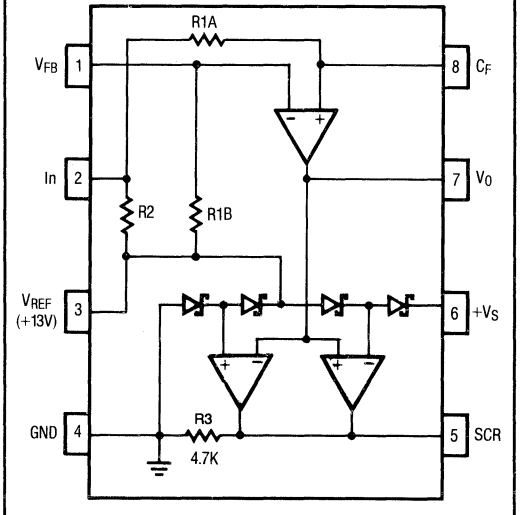
8-Lead
Dual In-Line Package
(Top View)



65-03206

Pin	Function
1	VFB
2	+Input
3	V_{REF} (+13V)
4	Ground
5	SCR Trigger
6	$+V_S$
7	Op Amp Output
8	NC

Functional Block Diagram

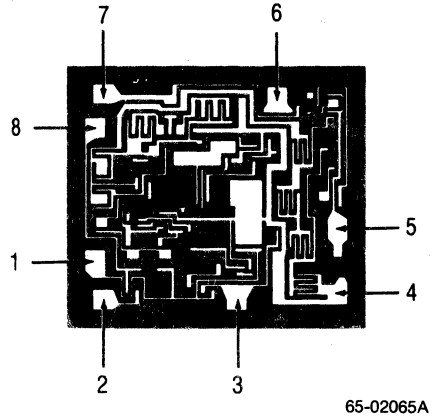


Input Resistor Values

R#	4143	4144
R1	1K	750Ω
R2	10K	2.5K

65-1748A

Mask Pattern



65-02065A

Die Size: 56 x 49 mils
Min. Pad Dimensions: 4 x 4 mils

Absolute Maximum Ratings

Supply Current 18mA
Internal Power Dissipation 500mW
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range ..... -35°C to +80°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Thermal Characteristics

	8-Lead Plastic DIP
Max. Junction Temp.	125°C
Max. P_D T_A < 50°C	468mW
Therm. Res. θ_{JC}	—
Therm. Res. θ_{JA}	160°C/W
For T_A > 50°C Derate at	6.25mW per °C

Electrical Characteristics (I_S = 5mA and T_A = +25°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Shunt Voltage	Pin 6	25	26	29.2	V
Reference Voltage	Pin 3	12.5	13	14.6	V
Op Amp					
Input Offset Voltage	Pin 2 to Pin 3	-3	±1	+3	mV
Output Voltage Swing	Pin 7 to Pin 3	±11	±13.5		V
AC Output Voltage	A_V = 500, f_{IN} = 50kHz V_{IN} = 1mV_{RMS}	50		180	mV_{RMS}
Resistors					
R3		3.8	4.7	5.7	
R1 RV4143		0.8	1.0	1.2	
R1 RV4144		0.6	0.75	0.9	kΩ
R2 RV4143		8.0	10.0	12.0	
R2 RV4144		2.0	2.5	3.0	
SCR Trigger					
V_{OH}	Across 4.7kΩ	1.5	2.8	6	V
V_{OL}			.001	.01	

Electrical Characteristics (I_S = 5mA, over the specified temperature range)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Shunt Voltage	Pin 6	24	26	30	V
Reference Voltage	Pin 3	12	13	15	
Op Amp					
Input Offset Voltage	Pin 2 to Pin 3	-6	±2	+6	mV
Output Voltage Swing	Pin 7 to Pin 3	±10.5	±13		V
AC Output Voltage	A_V = 500, f_{IN} = 50kHz V_{IN} = 1mV_{RMS}	50		200	mV_{RMS}
Resistors					
R3		3.3	4.7	6.1	kΩ
R1 RV4143		0.7	1.0	1.3	
R1 RV4144		0.52	0.75	0.98	
R2 RV4143		7.0	10	13.0	
R2 RV4144		1.75	2.5	3.25	
SCR Trigger					
V_{OH}	Across 4.7kΩ	1.3	2.8	5	V
V_{OL}			.003	.05	

Principles of Operation

The 26V shunt regulator voltage generated by the string of zener diodes is divided into three reference voltages: 3/4V_S, 1/2V_S, and 1/4V_S. V_{REF} is at 1/2V_S and is used as a reference to create an artificial ground of +13V at the op amp non-inverting input. Fault signals from the sense coil are AC coupled into the input and are amplified according to the following equation:

$$A_V = \frac{R5}{R1B} + 1$$

Where R1B equals the value of an internal resistor. When the output of the op amp swings above 3/4V_S or below 1/4V_S the SCR trigger output will go high and fire an external SCR.

Grounded neutral fault detection is accomplished when a short or fault closes a magnetic path between two sense coils. The resultant AC coupling through the three coils (the sense coil to the single-turn fault to the feedback coil) closes a positive feedback path around the op amp, and therefore the op amp oscillates. When the peaks of the oscillation voltage exceed the SCR trigger comparator thresholds the SCR output will go high.

Application Circuit

Figure 1 shows the diagram of a 120V AC outlet type GFI using a 4144 (circuits using the 4143 may require a lower value for C2 to maintain noise immunity).

Shunt Regulator

R4 limits the current into the shunt regulator; 220V applications will require substituting a 30K 4W resistor. D3 prevents the bridge output from discharging the supply bypass capacitor (C6). In addition to supplying power to the IC, the shunt regulator creates internal references voltages (see above).

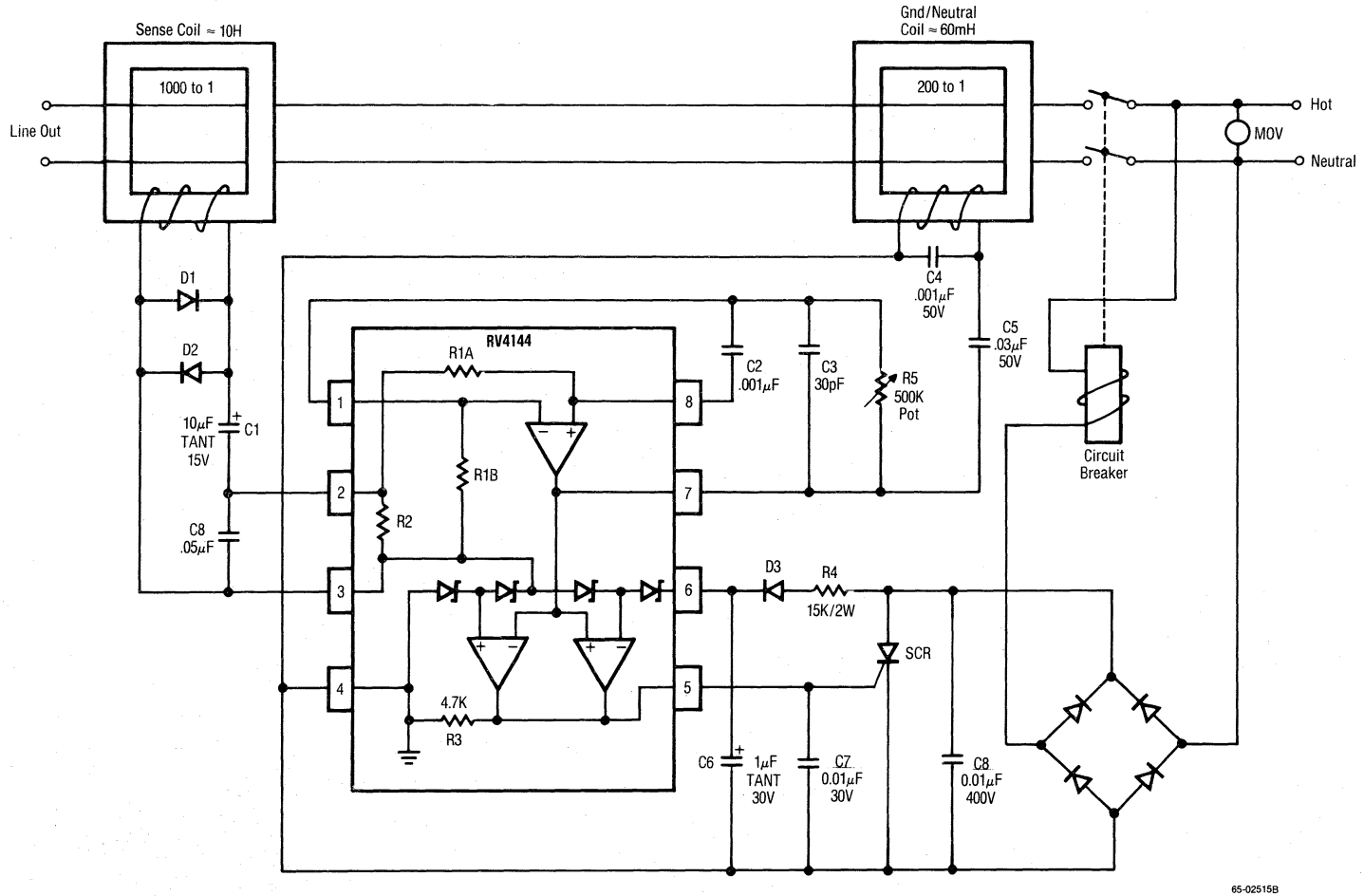


Figure 1. GFI Application Circuit (RV4144)

Operational Amplifier

R2 is a feedback resistor that sets gain and therefore sensitivity to normal faults. To adjust R2, follow this procedure: apply the desired fault current (a difference in current of 5mA is the U.L. 943 standard). Adjust R5 upward until the SCR activates. A fixed resistor should not be used for R5, as the resultant ±30% variation in sensitivity will not meet U.L.'s 4-6mA specification window.

C2 and C3 are noise filter capacitors. C3 and R5 combine to set a high frequency roll off point at 10kHz. The roll off frequency should be greater than the grounded neutral fault oscillation frequency, in order to preserve loop gain for oscillation (set by the inductance of the 200:1 coil and C5). As shown, with an inductance of about 60mH, it oscillates at 5.4kHz.

The sensitivity to grounded neutral faults is adjusted by changing the frequency of oscillation. Increasing the frequency reduces the sensitivity by reducing the loop gain of the positive feedback circuit. As frequency increases, the signal becomes attenuated by R5 C3 and the loop gain decreases. With the values shown the circuit will detect a grounded neutral fault having resistance of 2Ω or less.

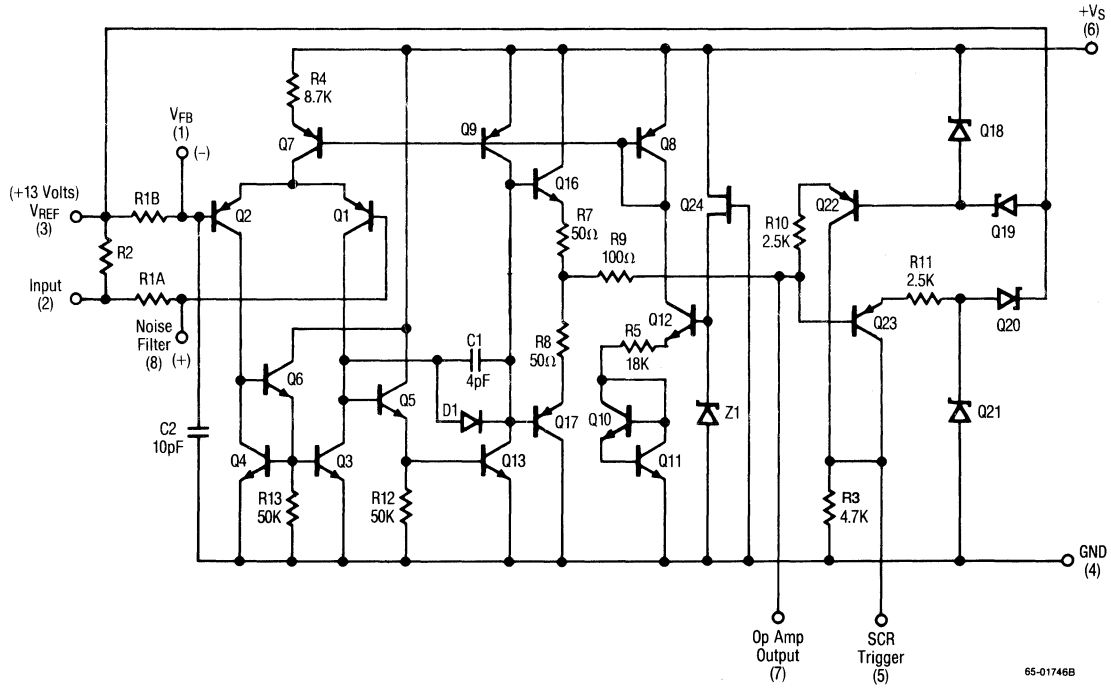
The inputs to the op amp are protected from overvoltage by D1 and D2. The input filter capacitor, C2, must be adjusted downward for 4143 applications; a value of 820pF is typical.

SCR Driver

The SCR used must have a high dV/dt rating to ensure that noise (generated by noisy appliances such as a drill motor) does not falsely trigger the SCR. Also, the SCR must have a gate drive requirement of less than 300μA. C7 is another noise filter capacitor that prevents narrow pulses from firing the SCR.

The circuit breaker used should have a 5mS or less response time in order to meet the U.L. 943 timing requirement.

Schematic Diagram



RV4145 Low Power Ground Fault Interrupter

Features

- No potentiometer required
- Direct interface to SCR
- Supply voltage derived from ac line — 26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets U.L. 943 standards
- 450 µA quiescent current
- Ideal for 120V or 220V systems

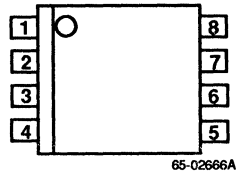
Description

The RV4145 is a low power controller for ac outlet ground fault interrupters. These devices detect hazardous grounding conditions, such as a pool of water and equipment connected to opposite phases of the ac line, and open circuits the line before a harmful or lethal shock occurs.

Contained internally is a 26V zener shunt regulator, an op amp, and an SCR driver. With the addition of two sense coils, a bridge rectifier, an SCR, and a relay, the 4145 will detect and protect against both hot wire to ground and neutral wire to ground faults. The simple layout and conventional design ensure ease of application and long term reliability.

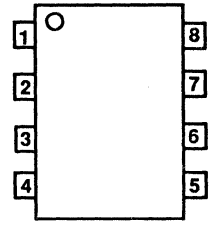
Connection Information

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

8-Lead Plastic Dual In-Line Package
(Top View)



65-0093

Pin	Function
1	VFB
2	+Input
3	V_{REF} (+13V)
4	Ground
5	SCR Trigger
6	$+V_S$
7	Op Amp Output
8	NC

Ordering Information

Part Number	Package	Operating Temperature Range
RV4145N	N	-35°C to +85°C
RV4145M	M	-35°C to +85°C

Notes:
N = 8-lead plastic DIP
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

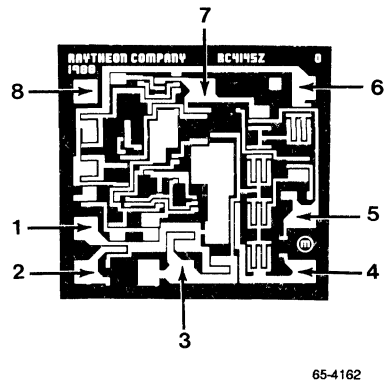
Absolute Maximum Ratings

Supply Current ..... 18 mA
Internal Power Dissipation ..... 500 mW
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature
Range ..... -35°C to +80°C
Lead Soldering Temperature
(60 Sec, DIP) ..... +300°C
(10 Sec, SO) ..... +260°C

Thermal Characteristics

	8-Lead Plastic SOIC	8-Lead Plastic DIP
Max. Junction Temp.	+125°C	+125°C
Max. P_D T_A <50°C	300 mW	468 mW
Therm. Res θ_{JC}	—	—
Therm. Res. θ_{JA}	240°C/W	160°C/W
For T_A >50°C Derate at	4.1 mW per °C	6.25 mW per °C

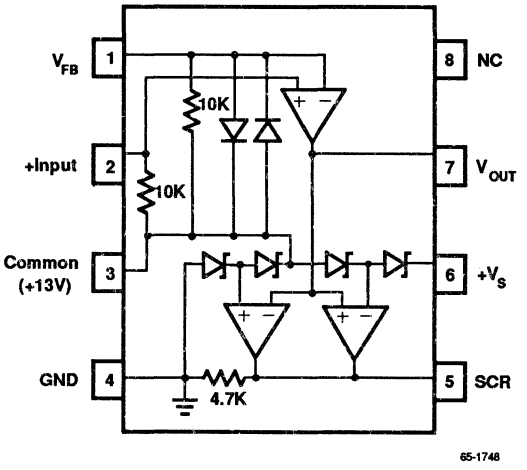
Mask Pattern



65-4162

Die Size: 49 x 46 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram



65-1748

Electrical Characteristics (I_S = 1.5 mA and T_A = +25°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Voltage (V_S)	Pin 6 to Pin 4	25	26	29.2	V
Reference Voltage	Pin 3 to Pin 4	12.5	13	14.6	V
Quiescent Current (I_S)	$+V_S$ = 24V		450	750	µA
Operational Amplifier					
Offset Voltage	Pin 2 to Pin 3	-3.0	0.5	+3.0	mV
+Output Voltage Swing	Pin 7 to Pin 3	6.8	7.2	8.1	V
-Output Voltage Swing	Pin 7 to Pin 3	-9.5	-11.2	-13.5	V
+Output Source Current	Pin 7 to Pin 3		650		µA
-Output Sink Current	Pin 7 to Pin 3		1.0		mA
Gain Bandwidth Product	f = 50 kHz	1.0	1.8		MHz
Detector Reference Voltage	Pin 7 to Pin 3	6.8	7.2	8.1	±V
Resistors	I_S = 0 mA				
R1	Pin 2 to Pin 3		10		kΩ
R2	Pin 1 to Pin 3		10		kΩ
R5	Pin 5 to Pin 4	4.0	4.7	5.4	kΩ
SCR Trigger Voltage	Pin 5 to Pin 4				
Detector On		1.5	2.8		V
Detector Off		0	1	10	mV

Electrical Characteristics (I_S = 1.5 mA, < over the specified temperature range)

Parameters	Test Conditions	Min	Typ	Max	Units
Shunt Regulator					
Zener Voltage (V_S)	Pin 6 to Pin 4	24	26	30	V
Reference Voltage	Pin 3 to Pin 4	12	13	15	V
Quiescent Current (I_S)	$+V_S$ = 23V		500		µA
Operational Amplifier					
Offset Voltage	Pin 2 to Pin 3	-5.0	0.5	+5.0	mV
+Output Voltage Swing	Pin 7 to Pin 3	6.5	7.2	8.3	V
-Output Voltage Swing	Pin 7 to Pin 3	-9	-11.2	-14	V
Gain Bandwidth Product	f = 50 kHz		1.8		MHz
Detector Reference Voltage	Pin 7 to Pin 3	6.5	7.2	8.3	±V
Resistors	I_S = 0 mA				
R1	Pin 2 to Pin 3		10		kΩ
R2	Pin 1 to Pin 3		10		kΩ
R5	Pin 5 to Pin 4	3.8	4.7	5.6	kΩ
SCR Trigger Voltage	Pin 5 to Pin 4				
Detector On		1.3	2.8		V
Detector Off		0	3	50	mV

Principles of Operation

The 26V shunt regulator voltage generated by the string of zener diodes is divided into three reference voltages: 3/4 VS, 1/2 VS, and 1/4 VS. VREF is at 1/2 VS and is used as a reference to create an artificial ground of +13V at the op amp non-inverting input. Fault signals from the sense coil are ac coupled into the input and are amplified according to the following equation:

$$V7 = R2 \times Isense/N$$

Where V7 is the RMS voltage at pin 7 relative to pin 3, R2 is the value of the feedback resistor connected from pin 7 to pin 1, Isense is the fault current in amps RMS and N is the turns ratio of the sense coil. When V7 exceeds plus or minus 7.2V relative to pin 3 the SCR Trigger output will go high and fire an external SCR.

The formula for V7 is approximate because it does not include the sense coil characteristics.

Grounded neutral fault detection is accomplished when a short or fault closes a magnetic path between two sense coils. The resultant ac coupling through the three coils (the sense coil to the single-turn fault to the feedback coil) closes a positive feedback path around the op amp, and therefore the op amp oscillates. When the peaks of the oscillation voltage exceed the SCR trigger comparator thresholds the SCR output will go high.

Application Circuit

Figure 1 shows the diagram of a 120V ac outlet type GFI using a 4145.

Shunt Regulator

R3 limits the current into the shunt regulator; 220V applications will require substituting a 90 kΩ 1W resistor. D1 prevents the bridge output from discharging the supply bypass capacitor (C6). In addition to supplying power to the IC, the shunt regulator creates internal reference voltages (see above).

Operational Amplifier

R2 is a feedback resistor that sets gain and therefore sensitivity to normal faults. To adjust R2 follow this procedure: apply the desired fault current (a difference in current of 5 mA is the U.L. 943 standard). Adjust R2 upward until the SCR activates. A fixed resistor can be used for R2, since the resultant ±15% variation in sensitivity will meet U.L.'s 4-6 mA specification window.

C3 is a noise filter capacitor. C3 and R2 combine to set a high frequency roll-off point at 10 kHz. The roll-off frequency should be greater than the grounded neutral fault oscillation frequency, in order to preserve loop gain for oscillation (set by the inductance of the 200:1 coil and C5). As shown, with an inductance of about 60 mH, it oscillates at 5.4 kHz.

The sensitivity to grounded neutral faults is adjusted by changing the frequency of oscillation. Increasing the frequency reduces the sensitivity by reducing the loop gain of the positive feedback circuit. As frequency increases, the signal becomes attenuated by R2 C3 and the loop gain decreases. With the values shown the circuit will detect a grounded neutral fault having resistance of 2Ω or less.

The inputs to the op amp are protected from overvoltage by back-to-back diodes.

SCR Driver

The SCR used must have a high dV/dt rating to ensure that noise (generated by noisy appliances such as a drill motor) does not falsely trigger the SCR. Also, the SCR must have a gate drive requirement of less than 300 μA. C7 is another noise filter capacitor that prevents narrow pulses from firing the SCR.

The circuit breaker used should have a 5 mS or less response time in order to meet the U.L. 943 timing requirement.

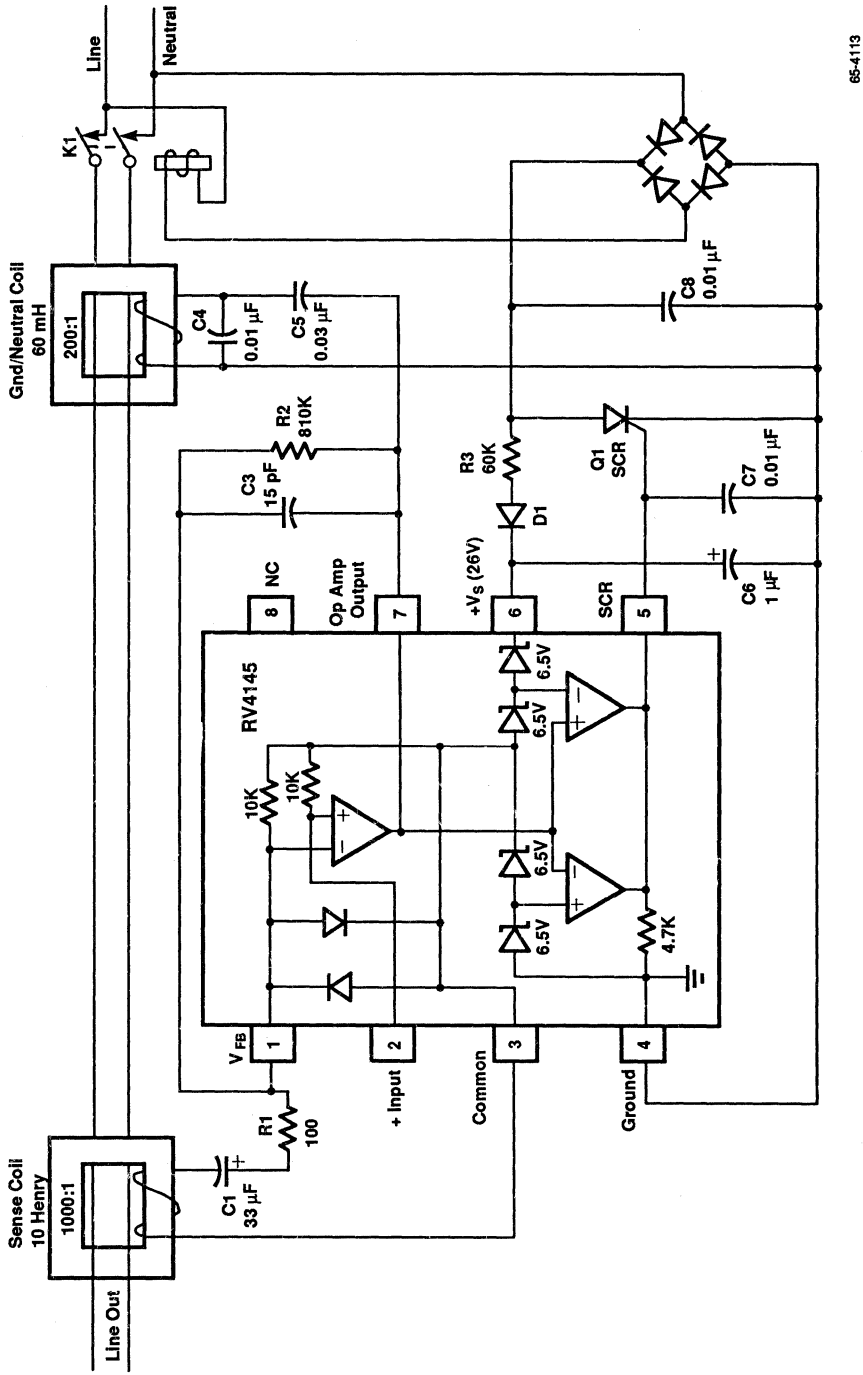
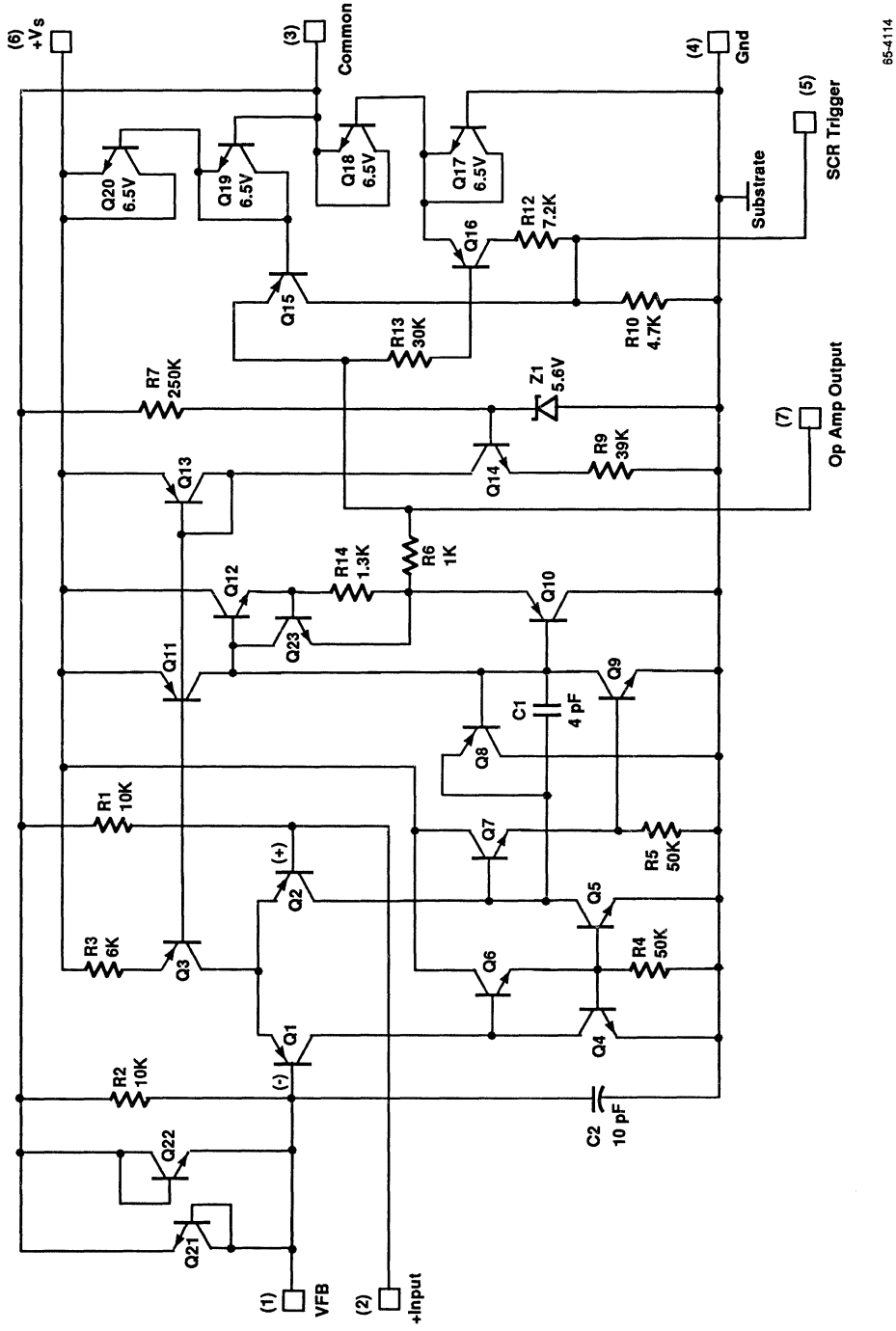


Figure 1. GFI Application Circuit

Schematic Diagram



SECTION 11

SPECIAL FUNCTIONS

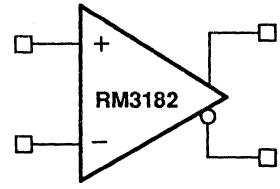
RM3182 ARINC 429 Differential Line Driver

Features

- Adjustable rise and fall times
- Adjustable output voltage swing
- Short circuit protected
- Output overvoltage protected
- Sync and clock enable inputs
- TTL and CMOS compatible inputs
- Mil-Std-883B types available
- 100 Kbits/second data rate

Description

The RM3182 consists of a bus interface line driver circuit plus auxiliary gating and synchronization circuitry. Designed to address the ARINC 429 standard, the RM3182 has output rise and fall times adjustable by the selection of two external capacitor values, and the output voltage swing range can be adjusted through an externally applied VREF signal. The logic inputs as well as the sync control inputs are TTL/CMOS compatible. The device is constructed on a monolithic IC using a junction-isolated bipolar process. Sputtered SiCr resistors are used in the internal bias circuitry, providing stable internal bias currents and also providing a tighter distribution of output impedance (±10%) when compared to industry-standard 3182 types. The RM3182 is available in 16-lead ceramic DIP and 28-pad LCC, and can be ordered with Mil-Std-883B high reliability screening.



65-4184

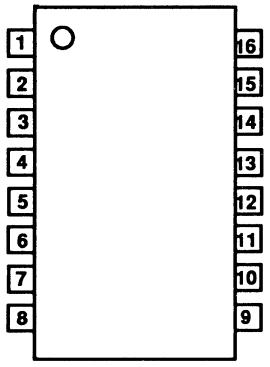
Ordering Information

Part Number	Package	Operating Temperature Range
RM3182S	S	-55°C to +125°C
RM3182S/883B	S	-55°C to +125°C
RM3182L	L	-55°C to +125°C
RM3182L/883B	L	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
S = 16-lead sidebraze ceramic DIP
L = 28-pad leadless chip carrier
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Connection Information

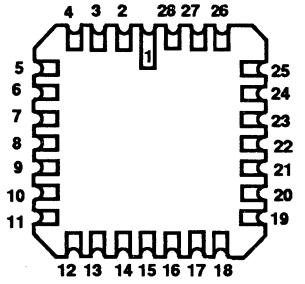
16-Lead Sidebraze DIP (Top View)



65-04192

Pin	Function	Pin	Function
1	V_{REF}	9	$+V_S$
2	Pwr Enable	10	NC
3	Sync	11	B_{OUT}
4	Data(A)	12	C_B
5	C_A	13	Data(B)
6	A_{OUT}	14	Clock
7	$-V_S$	15	NC
8	Gnd	16	V1

28-Pad LCC (Top View)



65-4193

Pin	Function	Pin	Function
1	V_{REF}	15	Gnd
2	NC	16	$+V_S$
3	Pwr Enable	17	B_{OUT}
4	Sync	18	NC
5	NC	19	NC
6	Data(A)	20	NC
7	NC	21	NC
8	NC	22	C_B
9	C_A	23	Data(B)
10	NC	24	NC
11	NC	25	Clock
12	NC	26	NC
13	A_{OUT}	27	NC
14	$-V_S$	28	V1

Absolute Maximum Ratings

Supply Voltage ($+V_S$ to $-V_S$) 36V
V1 Voltage ..... +7V
V_{REF} Voltage ..... +6V
Logic Input Voltage ..... -0.3V to $+V_S$+0.3V
Output Short Circuit Duration ..... See Note 1
Output Overvoltage ..... ±6.5V
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range ..... -55°C to +125°C
..... See Note 2
Lead Soldering Temperature (60 sec) ..... +300°C

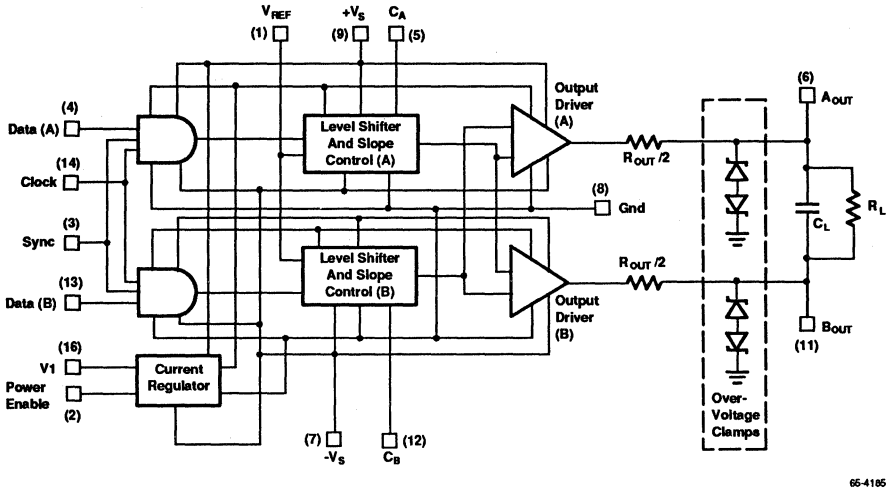
Notes:
1. Heatsinking may be required for output short circuit at +125°C.
2. Heatsinking may be required depending on load and signal frequencies.

Thermal Characteristics

(still air, soldered into PC board)

	16-Lead Sidebrazed DIP	28-Pad LCC
Max. Junction Temp.	+175°C	+175°C
Max. P_D T_A <50°C	1470 mW	1040 mW
Therm. Res θ_{JC}	25°C/W	25°C/W
Therm. Res. θ_{JA}	85°C/W	120°C/W
For T_A >50°C Derate at	11.7 mW per °C	8.3 mW per °C

Functional Block Diagram

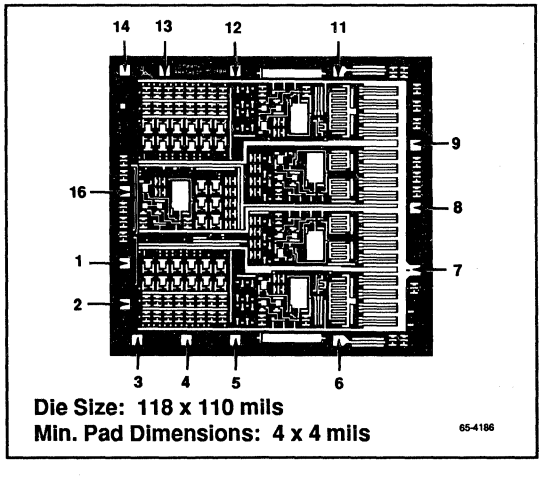


Notes:
1. R_L and C_L are external. Full load values are: R_L = 400 Ω, C_L = 0.03 µF.
2. Pin numbers are for 16-lead DIP.

Truth Table

Sync	Clock	Data (A)	Data (B)	A_{OUT}	B_{OUT}	Comments
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	$-V_{REF}$	$+V_{REF}$	Low
H	H	H	L	$+V_{REF}$	$-V_{REF}$	High
H	H	H	H	0V	0V	Null

Mask Pattern



Electrical Characteristics

(V_S = ±15V, V_{REF} = V1 = +5V, Pwr Enable = 0V, R_L = open circuit, -55°C ≤ T_A ≤ +125°C)

Parameters	Test Conditions	Min	Typ	Max	Units
Positive Supply Current	Data Rate = 0 to 100 Kbits/sec		11	16	mA
Negative Supply Current	Data Rate = 0 to 100 Kbits/sec	-16	-10		mA
V1 Supply Current	Data Rate = 0 to 100 Kbits/sec		200	975	µA
V_{REF} Supply Current	Data Rate = 0 to 100 Kbits/sec	-1.0	-0.4	-0.15	mA
Input Logic Level High		2.0			V
Input Logic Level Low				0.5	V
Output Voltage High	With Respect to Ground	4.75	5.0	5.25	V
Output Voltage Low	With Respect to Ground	-5.25	-5.0	-4.75	V
Output Voltage Null	Both Data Input = Logic 0	-250	0	+250	mV
Input Current High	V_{IN} = 2.0V		1	10	µA
Input Current Low	V_{IN} = 0.5V	-20	-1		µA
Output Short Circuit Current	Output in High State, to Gnd		-133	-80	mA
Output Short Circuit Current	Output in Low State, to Gnd	80	133		mA
Positive Supply Current	Output High and Shorted to Gnd			165	mA
Negative Supply Current	Output Low and Shorted to Gnd	-165			mA
Input Capacitance*				15	pF

*Guaranteed by design.

Typical Power Dissipation Characteristics

(V_S = ±15V, V1 = V_{REF} = +5V, Pwr Enable = 0V, T_A = +25°C)

Data Rate (Kbits/sec)	Load	Positive Supply Current	Negative Supply Current	Pin V1 Supply Current	Internal Power Dissipation	Load Power Dissipation
0 to 100	Open Circuit	11 mA	-10 mA	200 µA	325 mW	0
12.5 to 14	Full Load**	24 mA	-24 mA	200 µA	660 mW	60 mW
100	Full Load**	46 mA	-46 mA	200 µA	1000 mW	325 mW

**R_L = 400Ω, C_L = 0.03 µF (see Functional Block Diagram).

Principles of Operation

Each device consists of one differential driver and associated gating circuitry. The gating circuitry consists of clock and sync signal inputs which are ANDed with the two data inputs. See the block diagram and truth table on page 3. Three power supplies are required to operate the RM3182 in a typical ARINC 429 bus application: +15V, -15V, and +5V. The +5V supply, in addition to powering the internal bus current regulator, provides a reference voltage that determines the output voltage swing. The differential output swing will equal $2V_{REF}$. If a value of V_{REF} other than +5V is used, then a separate +5V supply is required for pin V1.

Figure 1 depicts connections for the ARINC 429 application. The driver output impedance is nominally 75Ω. With the Data(A) input at a logic high and Data (B) input at a logic low, A_{OUT} will swing to $+V_{REF}$ and B_{OUT} will swing to $-V_{REF}$ (constituting a logic high state). Reversing the data input states will cause A_{OUT} to swing to $-V_{REF}$ and B_{OUT} to $+V_{REF}$. With both data input signals at a logic low state, the outputs will both swing to 0V (output in null state).

The slew rate of the outputs, and consequently rise and fall times, can be adjusted through the selection of two external capacitor values. Typical values are $C_A = C_B = 75$ pF for high-speed operation (100 Kbits/sec) and $C_A = C_B = 500$ pF for low-speed operation (12.5 to 14 Kbits/sec).

The device can be powered down by applying a logic high signal to the Power Enable pin. If the power down feature is not used, then the Power Enable pin should be tied directly to ground.

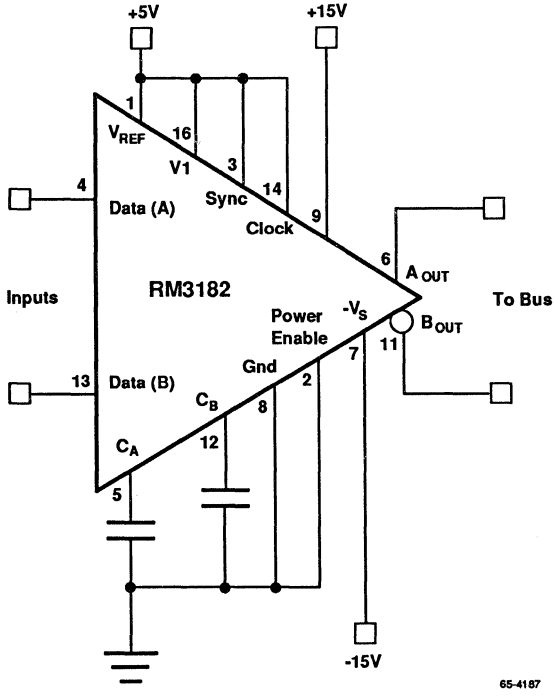
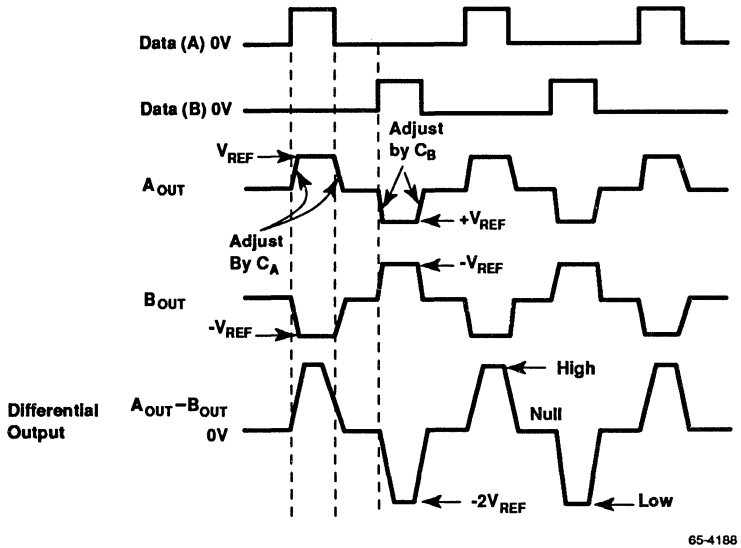


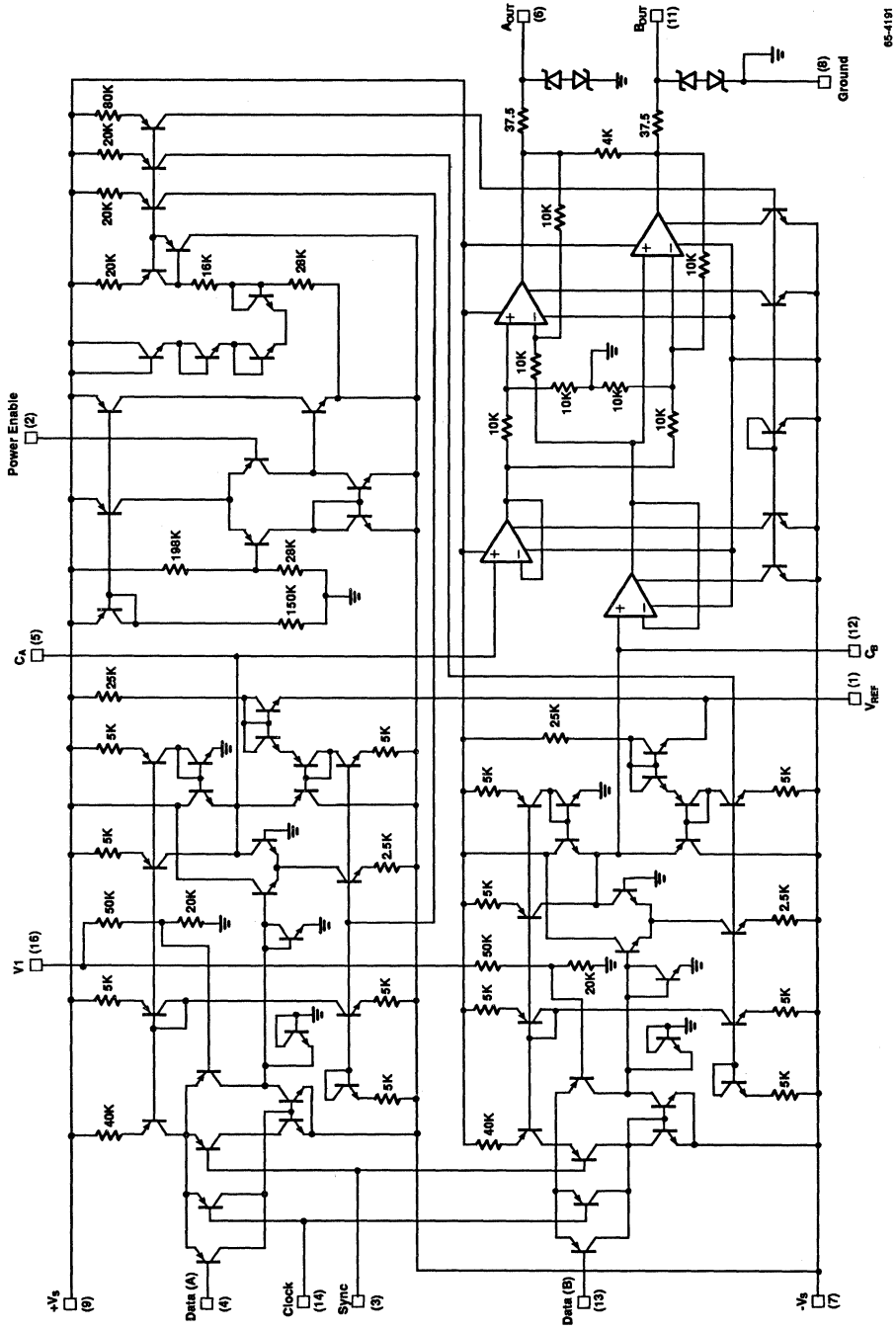
Figure 1. ARINC 429 Bus Application



Note: Outputs unloaded

Figure 2. Switching Waveforms

Schematic Diagram



RC4200
Analog Multiplier

Features

- High accuracy
  Non-linearity — 0.1% maximum
  Temperature coefficient — 0.005%/° C typical
- Multiple functions
  Multiply, divide square, square root, RMS-to-DC conversion, AGC, and modulate/demodulate
- Wide bandwidth — 4MHz
- Signal-to-noise ratio — 94dB

Description

The Raytheon RC4200 is the industry's first integrated circuit multiplier to have complete compensation for nonlinearity, the primary source of error and distortion. This is also the first IC multiplier to have three on-board operational amplifiers designed specifically for use in multiplier logging circuits. These specially designed amplifiers are frequency compensated for optimum AC response in a logging circuit, the heart of a multiplier, and can therefore provide superior AC response in comparison to other analog multipliers.

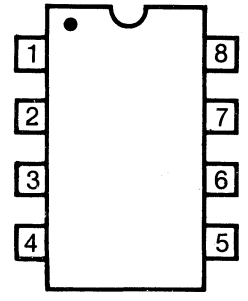
Versatility is unprecedented; this is the first IC multiplier that can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square-rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well designed monolithic chip provides a very low accuracy tempco.

The excellent linearity and versatility were achieved through circuit design rather than special grading or trimming, and therefore unit cost is very low. Analog multipliers can now be used in applications where price was previously an inhibiting factor.

The Raytheon RC4200 is ideal for use in low distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

Connection Information

8-Lead
DE and NB
Dual In-Line Package
(Top View)



Pin	Function
1	I_2
2	V_{OS2}
3	$-V_S$
4	I_3 (Output)
5	I_4
6	GND
7	V_{OS1}
8	I_1

65-01886A

Absolute Maximum Ratings

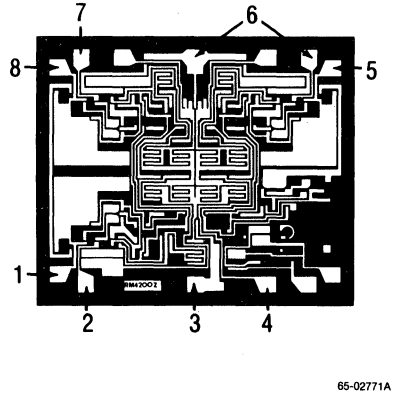
Supply Voltage ..... -22V
Internal Power Dissipation** ..... 500 mV
Input Current ..... -5mA
Storage Temperature Range
RM4200/4200A ..... -65°C to +150°C
RV4200/4200A ..... -55°C to +125°C
RC4200/4200A ..... -55°C to +125°C
Operating Temperature Range
RM4200/4200A ..... -55°C to +125°C
RV4200/4200A ..... -25°C to +85°C
RC4200/4200A ..... 0°C to +70°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Plastic DIP	8-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	468mW	833mW
Therm. Res. θ_{JC}	—	45°C/W
Therm. Res. θ_{JA}	160°C/W	150°C/W
For T_A > 50°C Derate at	6.25mW per °C	8.33mW per °C

Mask Pattern



Die Size: 78 × 66 mils
Min. Pad Dimensions: 4 × 4 mils

Ordering Information

Part Number	Package	Operating Temperature Range
RC4200N	N	0°C to +70°C
RC4200AN	N	0°C to +70°C
RV4200D	D	-25°C to +85°C
RV4200AD	D	-25°C to +85°C
RM4200D	D	-55°C to +125°C
RM4200D/883B	D	-55°C to +125°C
RM4200AD	D	-55°C to +125°C
RM4200AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Electrical Characteristics

(Over Operating Temperature Range, V_S = −15V unless otherwise noted)

Parameters	Test Conditions	4200A			4200			Units
		Min	Typ	Max	Min	Typ	Max	
Total Error as Multiplier Untrimmed	T_A = +25°C (Note 1)			±2.0			±3.0	%
With External Trim			±0.2			±0.2		%
Versus Temperature			±0.005			±0.005		%/°C
Versus Supply (−9 to −18V)			±0.1			±0.1		%/V
Nonlinearity	50μA ≤ $I_{1,2,4}$ ≤ 250μA, T_A = +25°C (Note 2)			±0.1			±0.3	%
Input Current Range (I_1, I_2 and I_4)		1.0		1000	1.0		1000	μA
Input Offset Voltage	I_1 = I_2 = I_4 = 150μA, T_A = +25°C			±5.0			±10	mV
Input Bias Current	I_1 = I_2 = I_4 = 150μA, T_A = +25°C			300			500	nA
Average Input Offset Voltage Drift	I_1 = I_2 = I_4 = 150μA			±50			±100	μV/°C
Output Current Range (I_3)	(Note 3)	1.0		1000	1.0		1000	μA
Frequency Response, −3dB point			4.0			4.0		MHz
Supply Voltage		−18	−15	−9.0	−18	−15	−9.0	V
Supply Current	I_1 = I_2 = I_4 = 150μA, T_A = +25°C			4.0			4.0	mA

Notes:
1. Refer to Figure 6 for example.
2. The input circuits tend to become unstable at I_1, I_2, I_4 < 50μA and linearity decreases when I_1, I_2, I_4 > 250μA (eq. @ I_1 = I_2 = 500μA, nonlinearity error ≈ 0.5%).
3. These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700Ω and must be pulled up to a positive supply such that the voltage on pin (4) stays within a range of 0 to +5V.

Functional Description

The RC4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in Figure 1. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{I_1 I_2}{I_4} \qquad (1)$$

The three input currents must be positive and restricted to a range of 1μA to 1mA. These currents go into the multiplier chip at op-amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2, and Q4 equal to their respective input currents (I_1, I_2, and I_4). These op amps are designed with current-source outputs and are phase-compensated for optimum frequency

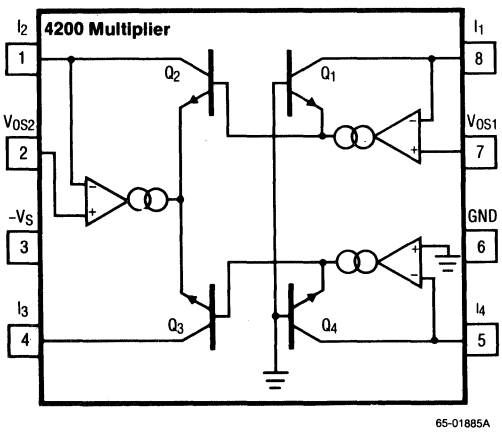


Figure 1. Functional Diagram

response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single supply voltage (nominally -15V) and total quiescent current drain is less than 4mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship

$$V_{BEN} = \frac{kT}{q} \ln \frac{I_{CN}}{I_{SN}} \qquad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. This $I_C r_E$ term introduces a parabolic nonlinearity even with matched transistors. Raytheon has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this Raytheon-developed circuit technique compensates linearity error over temperature changes. The nonlinearity versus temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{kT}{q}\left[\ln \frac{I_1}{I_{S1}} = \ln \frac{I_2}{I_{S2}} - \ln \frac{I_3}{I_{S3}} - \ln \frac{I_4}{I_{S4}}\right] = 0 \qquad (3)$$

This equation reduces to:

$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \qquad (4)$$

The ratio of reverse saturation currents, $I_{S1}I_{S2}/I_{S3}I_{S4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the ratio is very close to unity, typically 1.0 $\pm$1%. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_1}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

Basic Circuits

Current Multiplier/Divider

The basic design criteria for all circuit configurations using the 4200 multiplier is contained in equation (1):

$$\text{i.e.,} \qquad I_3 = \frac{I_1 I_2}{I_4}$$

The current-product-balance equation restates this as:

$$I_1 I_2 = I_3 I_4 \quad (6)$$

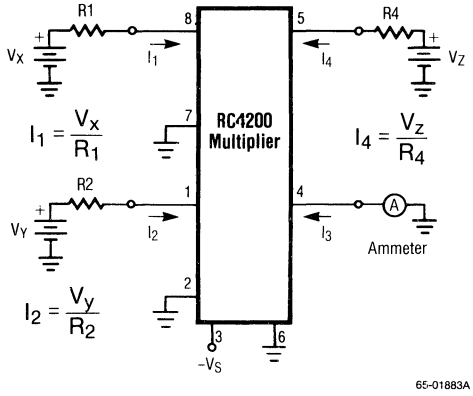
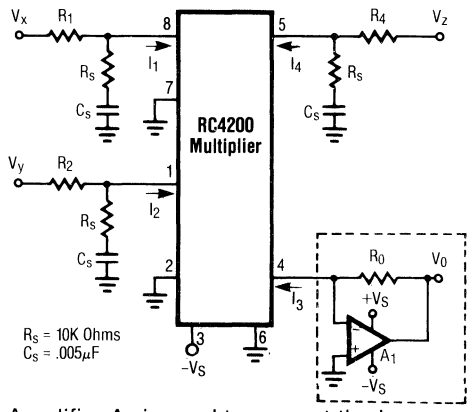


Figure 2

Dynamic Range and Stability

The precision dynamic range for the 4200 is from +50μA to +250μA inputs for I_1, I_2 and I_4. Stability and accuracy degrade if this range is exceeded.

To improve the stability for input currents less than 50μA, filter circuits ($R_S C_S$) are added to each input (see Figure 3).



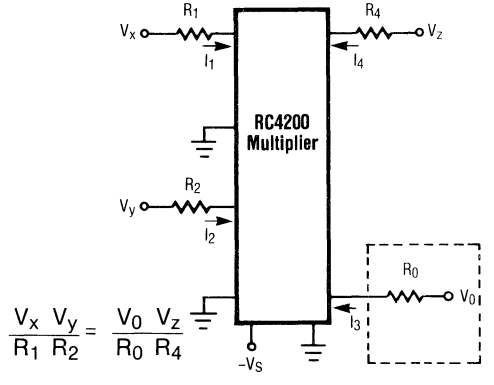
Amplifier A_1 is used to convert the I_3 current to an output voltage.

Multiplier: V_Z = constant ≠ 0

Divider: V_y = constant ≠ 0

Figure 3

Voltage Multiplier/Divider



Solving for V_0: $V_0 = \frac{V_x V_y}{V_z} \frac{R_0 R_4}{R_1 R_2}$

For a multiplier circuit $V_Z = V_R$ = constant

Therefore: $V_0 = V_x V_y K$ where $K = \frac{R_0 R_4}{V_R R_1 R_2}$

For a divider circuit $V_y = V_R$ = constant

Therefore: $V_0 = \frac{V_x}{V_z} K$ where $K = \frac{V_R R_0 R_4}{R_1 R_2}$

Figure 4

Extended Range

The input and output voltage ranges can be extended to include 0 and negative voltage signals by adding bias currents. The R_SC_S filter circuits are eliminated when the input and biasing resistors are selected to limit the respective currents to 50μA min. and 250μA max.

Extended Range Multiplier

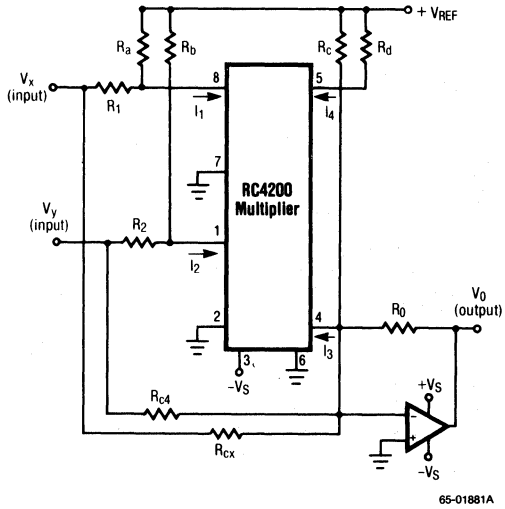


Figure 5

Resistors R_a and R_b extend the range of the V_x and V_y inputs by picking values such that:

$$I_1(\text{min.}) = \frac{V_x(\text{min.})}{R_1} + \frac{V_{REF}}{R_a} = 50\mu A,$$

$$\text{and } I_1(\text{max.}) = \frac{V_x(\text{max.})}{R_1} + \frac{V_{REF}}{R_a} = 250\mu A;$$

$$\text{also } I_2(\text{min.}) = \frac{V_y(\text{min.})}{R_2} + \frac{V_{REF}}{R_b} = 50\mu A,$$

$$\text{and } I_2(\text{max.}) = \frac{V_y(\text{max.})}{R_2} + \frac{V_{REF}}{R_b} = 250\mu A.$$

Resistor R_c supplies bias current for I_3 which allows the output to go negative.

Resistors R_{cx} and R_{cy} permit equation (6) to balance, i.e.:

$$\left(\frac{V_x}{R_1} + \frac{V_{REF}}{R_a}\right)\left(\frac{V_y}{R_2} + \frac{V_{REF}}{R_b}\right) = \left(\frac{V_0}{R_0} + \frac{V_{REF}}{R_c} + \frac{V_x}{R_{cx}} + \frac{V_y}{R_{cy}}\right)\left(\frac{V_{REF}}{R_d}\right)$$

$$\frac{V_xV_y}{R_1R_2} + \frac{V_xV_{REF}}{R_1R_b} + \frac{V_yV_{REF}}{R_2R_a} + \frac{V_{REF}^2}{R_aR_b} =$$

$$\frac{V_0V_{REF}}{R_0R_d} + \frac{V_xV_{REF}}{R_{cx}R_d} + \frac{V_yV_{REF}}{R_{cy}R_d} + \frac{V_{REF}^2}{R_cR_d}$$

Cross-Product Cancellation

Cross-products are a result of the V_xV_R and V_yV_R terms. To the extent that: $R_1R_b = R_{cx}R_d$ and $R_2R_a = R_{cy}R_d$, cross-product cancellation will occur.

Arithmetic Offset Cancellation

The offset caused by the V_{REF}^2 term will cancel to the extent that: $R_aR_b = R_cR_d$, and the result is:

$$\frac{V_xV_y}{R_1R_2} = \frac{V_0V_{REF}}{R_0R_d} \quad \text{or } V_0 = V_xV_y\,K$$

$$\text{where } K = \frac{R_0R_d}{V_{REF}R_1R_2}$$

Resistor Values

Inputs:

$$V_x(\text{min.}) \le V_x \le V_x(\text{max.})$$

$$\Delta V_x = V_x(\text{max.}) - V_x(\text{min.})$$

$$V_y(\text{min.}) \le V_y \le V_y(\text{max.})$$

$$\Delta V_y = V_y(\text{max.}) - V_y(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

$$K = \frac{V_0}{V_xV_y} \text{ (Design Requirement)}$$

$$R_1 = \frac{\Delta V_x}{200\mu A},\ R_2 = \frac{\Delta V_y}{200\mu A},\ R_d = \frac{V_{REF}}{250\mu A}$$

$$R_a = \frac{\Delta V_xV_{REF}}{250\mu A\ \Delta V_x - 200\mu A\ V_x(\text{max.})}$$

$$R_b = \frac{\Delta V_yV_{REF}}{250\mu A\ \Delta V_y - 200\mu A\ V_y(\text{max.})}$$

$$R_c = \frac{R_aR_b}{R_d},\ R_{cx} = \frac{R_1R_b}{R_d},\ R_{cy} = \frac{R_2R_a}{R_d}$$

$$R_0 = \frac{\Delta V_x\,\Delta V_y\,K}{160\mu A}$$

Multiplying Circuit Offset Adjust

$$10K \leq R_5 = R_9 = R_{16} \leq 50K$$

$$R_7 = R_{11} = R_{14} = 100\Omega$$

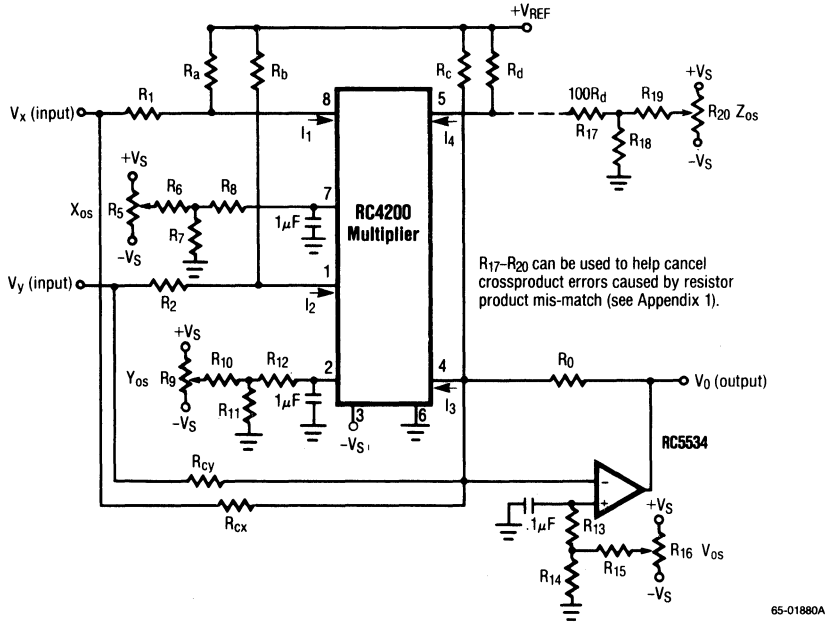
$$R_6 = R_{10} = 100\Omega \frac{V_S}{.05}$$

$$R_{15} = 100\Omega \frac{V_S}{.10}$$

$$R_8 = R_1 || R_a$$

$$R_{12} = R_2 || R_b$$

$$R_{13} = R_0 || R_c || R_{cx} || R_{cy}$$



Procedure:

1. Set all trimmer pots to 0V on the wiper.
2. Connect V_x input to ground. Put in a full scale square wave on V_y input. Adjust $X_{OS}(R_5)$ for no square wave on V_0 output (adjust for 0 feedthrough).
3. Connect V_y input to ground. Put in a full scale square wave on V_x input. Adjust $Y_{OS}(R_9)$ for no square wave on V_0 output (adjust for 0 feedthrough).
4. Connect V_x and V_y to ground. Adjust $V_{OS}(R_{16})$ for 0V on V_0 output.

Figure 6

Extended Range Divider

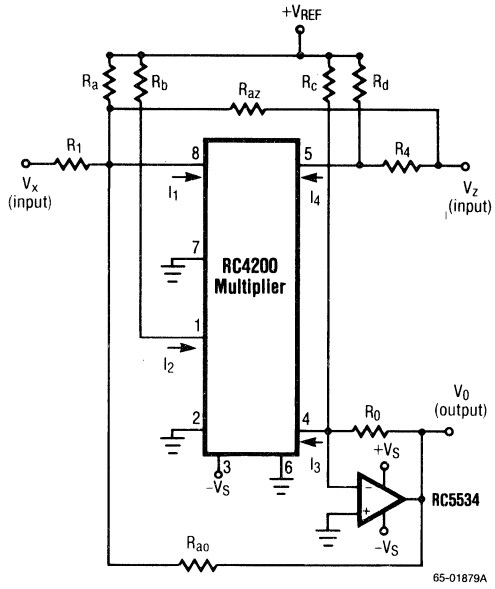


Figure 7

As with the extended range multiplier, resistors R_{az} and R_{ao} are added to cancel the cross-product error caused by the biasing resistors, i.e.,

$$\left(\frac{V_x}{R_1}+\frac{V_0}{R_{ao}}+\frac{V_z}{R_{az}}+\frac{V_{REF}}{R_a}\right)\left(\frac{V_{REF}}{R_b}\right)=\left(\frac{V_0}{R_0}+\frac{V_{REF}}{R_c}\right)\left(\frac{V_z}{R_4}+\frac{V_{REF}}{R_d}\right)$$

$$\frac{V_xV_{REF}}{R_1R_b}+\frac{V_0V_{REF}}{R_{ao}R_b}+\frac{V_zV_{REF}}{R_{az}R_b}+\frac{V_{REF}^2}{R_aR_b}=$$

$$\frac{V_0V_z}{R_0R_4}+\frac{V_0V_{REF}}{R_0R_d}+\frac{V_zV_{REF}}{R_4R_c}+\frac{V_{REF}^2}{R_cR_d}$$

To cancel cross-product and arithmetic offset:

$R_{ao}R_b = R_0R_d$, $R_{az}R_b = R_4R_c$ and $R_aR_b = R_cR_d$

and the result is:

$$\frac{V_xV_{REF}}{R_1R_b}=\frac{V_0V_z}{R_0R_4} \quad \text{or } V_0 = V_x/V_zK$$

$$\text{where } K=\frac{V_{REF}R_0R_4}{R_1R_b}$$

NOTE: It is necessary to match the resistor cross-products above to within the amount of error tolerable in the output offset, i.e., with a 10V F.S. output, 0.1% resistor cross-product match will give 0.1% x 10V = 10mV untrimmable output offset voltage.

Resistor Values

Inputs:

$$V_x(\text{min.}) \le V_x \le V_x(\text{max.})$$

$$\Delta V_x = V_x(\text{max.}) - V_x(\text{min.})$$

$$V_z(\text{min.}) \le V_z \le V_z(\text{max.})$$

$$\Delta V_z = V_z(\text{max.}) - V_z(\text{min.})$$

$$V_{REF} = \text{Constant (+7V to +18V)}$$

Outputs:

$$V_0(\text{min.}) \le V_0 \le V_0(\text{max.})$$

$$\Delta V_0 = V_0(\text{max.}) - V_0(\text{min.})$$

$$K=\frac{V_0V_z}{V_x} \text{ (Design Requirement)}$$

$$R_0=\frac{\Delta V_0}{750\mu A},\ R_b=\frac{V_{REF}}{250\mu A},\ R_4=\frac{\Delta V_z}{200\mu A}$$

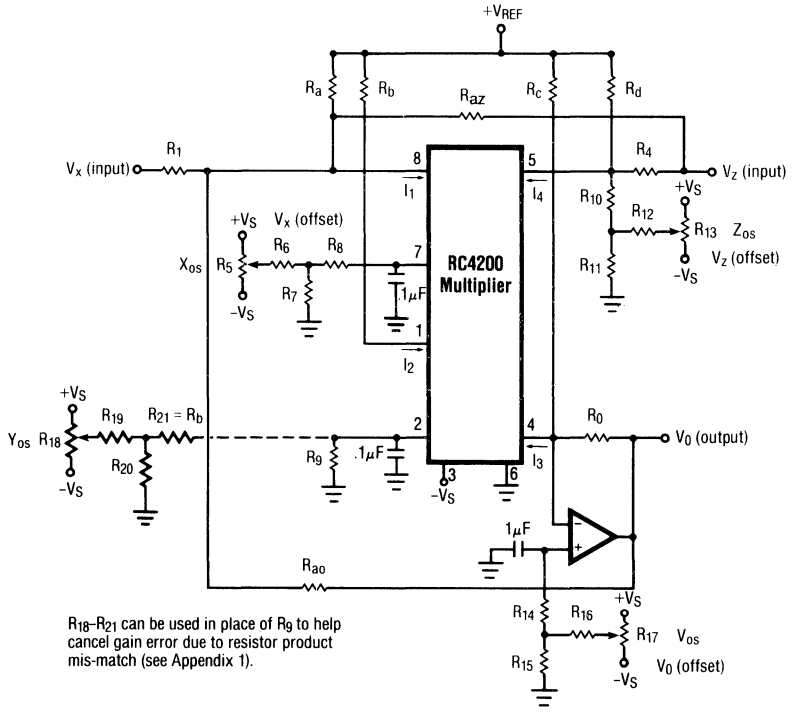
$$R_c=\frac{\Delta V_0V_{REF}}{750\mu A\ \Delta V_0 - 700\mu A\ V_0(\text{max.})}$$

$$R_d=\frac{\Delta V_zV_{REF}}{250\mu A\ \Delta V_z - 200\mu A\ V_z(\text{max.})}$$

$$R_a=\frac{R_cR_d}{R_b},\ R_{az}=\frac{R_cR_4}{R_b},\ R_{ao}=\frac{R_0R_d}{R_b}$$

$$R_1=\frac{\Delta V_0\ \Delta V_z}{600\mu AK}$$

Divider Circuit with Offset Adjustment



General

$10K \leq R_5 = R_{13} = R_{17} \leq 50K$

$R_7 + R_8 \approx R_1 || R_a || R_{az} || R_{ao}$

$R_6 \approx \frac{V_S}{.05} R_7$

$R_9 = R_b$

$R_{10} \approx 100 \times R_4$

$R_{11} = 20K$

$R_{12} = 100K$

$R_{14} + R_{15} \approx R_o || R_c$

$R_{16} \approx \frac{V_S}{.10} R_{15}$

Example: Two-Quad Divider

$V_0 = K\frac{V_x}{V_z}$, K = k, $V_{REF} = +V_S = +15V$

$-10 \leq V_x \leq +10$, therefore $\Delta V_x = 20$
$0 \leq V_z \leq +10$, therefore $\Delta V_z = 10$
$-10 \leq V_0 \leq +10$, therefore $\Delta V_0 = 20$

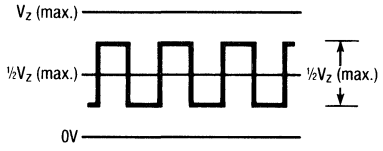
$R_0 = 26.7K$
$R_b = 60K$
$R_4 = 50K$
$R_c = 37.5K$
$R_d = 300K$
$R_a = 187.5K$
$R_{az} = 31.25K$
$R_{ao} = 133K$
$R_1 = 333K$
$R_5, R_{13}\ R_{17} = 10K$
$R_7, R_{15} = 1K$
$R_8, R_{11} = 20K$
$R_6, R_9, R_{16} = 300K$
$R_{10} = 4.7M$
$R_{12} = 100K$

Figure 8

Divider Circuit Offset Adjustment Procedure

1. Set each trimmer pot to 0V on the wiper.

2. Connect V_X (input) to ground. Put a DC voltage of approximately ½V_Z (max.) DC on the V_Z (input) with an AC (squarewave is easiest) voltage of ½V_Z (max.) peak-to-peak superimposed on it. Adjust $X_{OS}(R_5)$ for zero feedthrough. (No AC at V_O)



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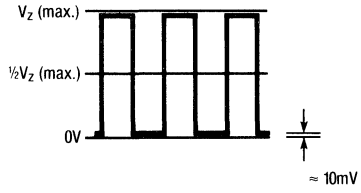
3. Connect V_X (input to V_Z (input) and put in the ½V_Z (max.) DC with an AC of approximately 20mV less than V_Z (max.).

   Adjust $Z_{OS}(R_{13})$ for zero feedthrough.

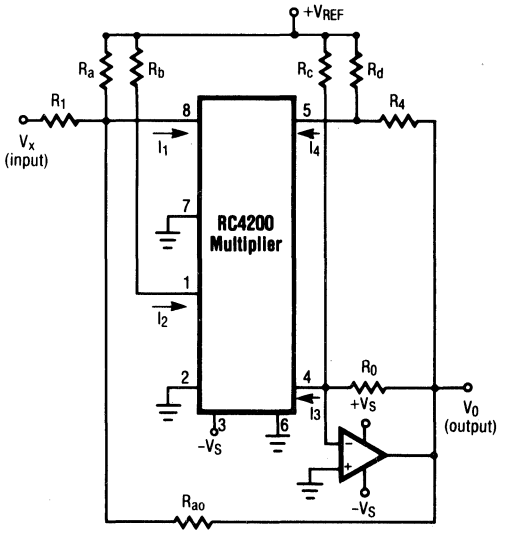


4. Return V_X (input) to ground and connect V_Z (max.) DC on V_Z (input). Adjust output $V_{OS}(R_{17})$ for V_O =.

5. Connect V_X (input) to V_Z (input) and put in V_Z (max.) DC. (The output will equal K.) Decrease the input slowly until the output (V_O = K) deviates beyond the desired accuracy. Adjust Z_{OS} to bring it back into tolerance and return to Step 4. Continue Steps 4 and 5 until V_Z reduces to the lowest value desired.

NOTE: As the input to V_X and V_Z gets closer to zero (an illegal state) the system noise will predominate so much that an integrating voltmeter will be very helpful.

Square Root Circuit $V_O = N\sqrt{V_X}$



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$$\frac{V_X V_{REF}}{R_1 R_b} + \frac{V_{REF}^2}{R_a R_b} + \frac{V_O V_{REF}}{R_{ao} R_b} = \frac{V_O^2}{R_O R_4} + \frac{V_O V_{REF}}{R_c R_4} + \frac{V_O V_{REF}}{R_O R_d} + \frac{V_{REF}^2}{R_c R_d}$$

If $R_a R_b = R_c R_d$ and $R_{ao} R_b R_O R_d + R_{ao} R_b R_c R_4 = R_c R_d R_O R_4$

Then $\frac{V_O^2}{R_O R_4} = \frac{V_X V_{REF}}{R_1 R_b}$ or $V_O^2 = V_X K$ where $K = \frac{V_{REF} R_O R_4}{R_1 R_b}$

and $V_O = N\sqrt{V_X}$ where $N = \sqrt{K}$

$0 \le V_X \le V_X$ (max) and V_O (max) $= N\sqrt{V_X}$ (max)

$$N = \frac{V_O}{\sqrt{V_X}} \text{ (Design Requirement)}$$

$$R_1 = \frac{V_O(max)^2}{75\mu A\ N^2}$$

$$R_a = R_d = \frac{V_{REF}}{50\mu A}$$

$$R_b = R_c = \frac{V_{REF}}{150\mu A}$$

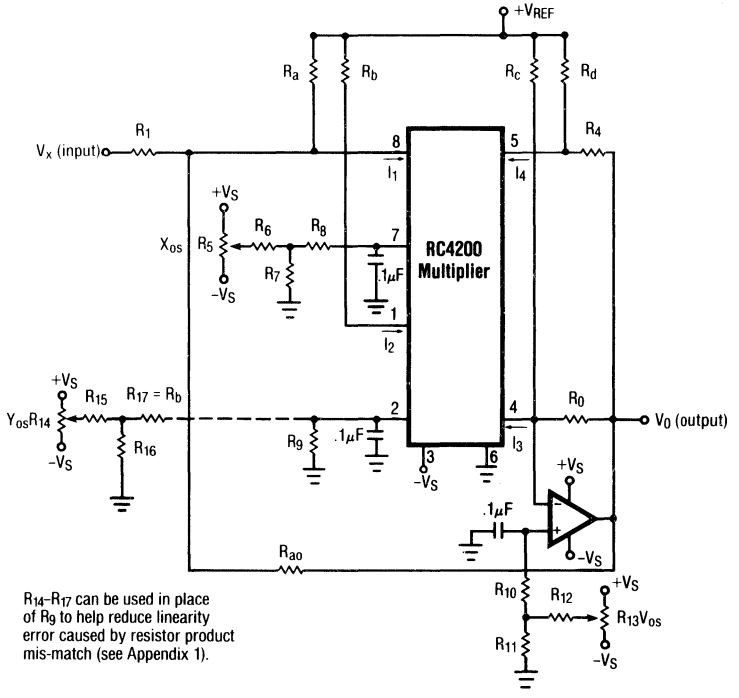
$$R_4 = \frac{V_O(max)}{50\mu A}$$

$$R_{ao} = \frac{V_O(max)}{125\mu A}$$

$$R_O = \frac{V_O(max)}{225\mu A}$$

Figure 9

Square Root Circuit Offset Adjust



$$10K \leq R_5 = R_{13} \leq 50K$$

$$R_7 = 100\Omega$$

$$R_6 = R_7 \frac{V_S}{.05}$$

$$R_8 = R_1 || R_a || R_{ao}$$

$$R_9 = R_b$$

$$R_{10} = R_0 || R_c$$

$$R_{11} = 100\Omega$$

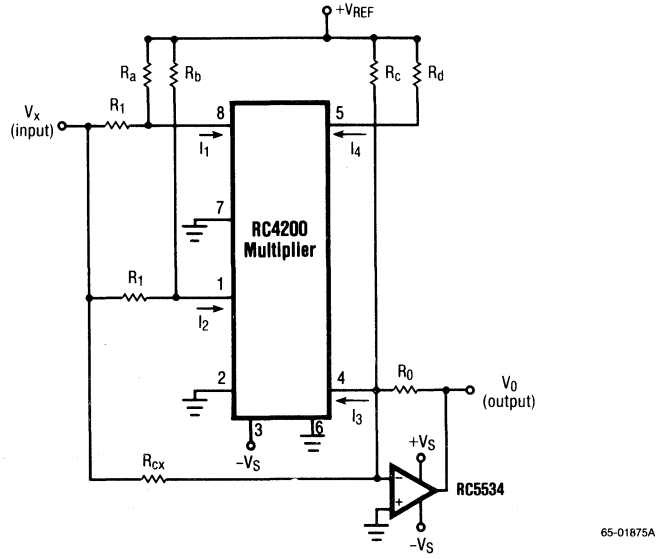
$$R_{12} = R_{11} \frac{V_S}{.1}$$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale (0 to V_x(max.)) squarewave on V_x input. Adjust $X_{os}(R_5)$ for proper peak-to-peak amplitude on V_0 output. (Scaling adjust)
3. Connect V_x input to ground. Adjust $V_{os}(R_{13})$ for 0V on V_0 output.

Figure 10

Squaring Circuits $V_0 = K V_x^2$



$$\frac{V_x^2}{R_1^2} + \frac{2V_xV_{REF}}{R_1R_a} + \frac{V_{REF}^2}{R_a^2} = \frac{V_0V_{REF}}{R_0R_d} + \frac{V_{REF}^2}{R_cR_d} + \frac{V_xV_{REF}}{R_{cx}R_d}$$

if $R_a^2 = R_cR_d$ and $R_1R_a = 2R_{cx}R_d$

then $\frac{V_0V_{REF}}{R_0R_d} = \frac{V_x^2}{R_1^2}$ or $V_0 = KV_x^2$ where $K = \frac{R_0R_d}{V_{REF}R_1^2}$

$V_x(min.) \leq V_x \leq V_x(max.)$ $\Delta V_x = V_x(max.) - V_x(min.)$

$K = \frac{V_0}{V_x^2}$ (Design Requirement)

$$R_1 = \frac{\Delta V_x}{200\mu A}$$

$$R_a = \frac{\Delta V_x V_{REF}}{250\mu A\ \Delta V_x - 200\mu A\ V_x(max.)}$$

$$R_d = \frac{V_{REF}}{250\mu A}$$

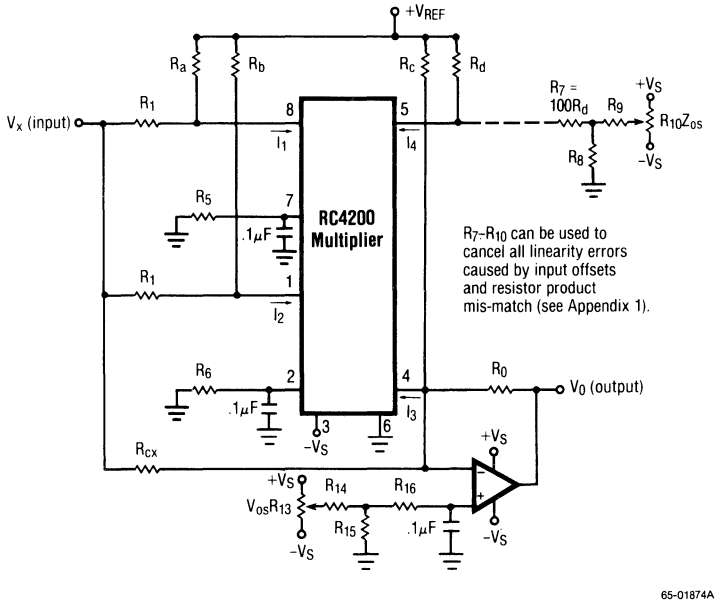
$$R_c = \frac{R_a^2}{R_d}$$

$$R_{cx} = \frac{R_1R_a}{2R_d}$$

$$R_0 = \frac{\Delta V_x^2 K}{160\mu A}$$

Figure 11

Squaring Circuits Offset Adjust



$$10K \leq R_{10}, R_{11} \leq 50K$$

$$R_8, R_{15} = 100\Omega$$

$$R_9, R_{14} = 100\Omega \frac{V_S}{.1}$$

$$R_5, R_6 = R_1 || R_a$$

$$R_{16} = R_0 || R_c || R_{cx}$$

Procedure

1. Set both trimmer pots to 0V on the wiper.
2. Put in a full scale ($\pm V_x$) squarewave on V_x input. Adjust $Z_{os}(R_{10})$ for uniform output.
3. Connect V_x input to ground. Adjust $V_{os}(R_{11})$ for 0V on V_0 output.

Figure 12

Appendix 1 — System Errors

There are four types of accuracy errors which effect overall system performance. They are:

1. Nonlinearity — Incremental deviation from absolute accuracy.(1)
2. Scaling Error — Linear deviation from absolute accuracy.
3. Output Offset — Constant deviation from absolute accuracy.
4. Feedthrough(2) — Crossproduct errors caused by input offsets and external circuit limitations.

The nonlinearity error in the transfer function of the 4200 is ±0.1% max. (±0.03% max. for 4200A).

$$\text{i.e., } I_3 = \frac{I_1 I_2}{I_4} \pm 0.1\%\ \text{F.S.}^{(4)}$$

The other system errors are caused by voltage offsets on the inputs of the 4200 and can be as high as ±3.0% (±2.0% for 4200A).

$$\text{i.e., } V_0 = \frac{V_x V_y}{V_z}\frac{R_0 R_4}{R_1 R_2} \pm 3.0\%\ \text{F.S.}^{(3)(4)}$$

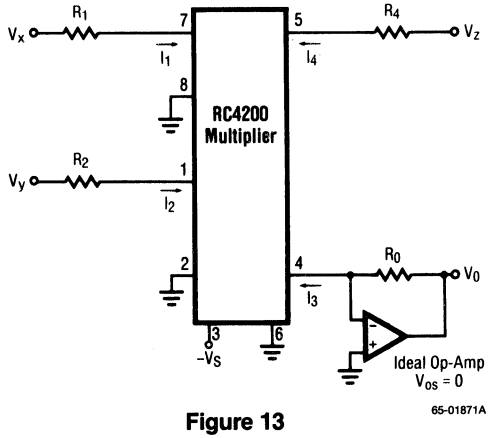


Figure 13

Notes:
1. The input circuits tend to become unstable at I_1, I_2, $I_4 <$ 50μA and linearity decreases when I_1, I_2, $I_4 >$ 250μA (e.g., @ $I_1 = I_2$ = 500μA nonlinearity error ≈ 0.5%).
2. This section will not deal with feedthrough which is proportional to frequency of operation and caused by stray capacitance and/or bandwidth limitations. (Refer to Figure 21.)
3. Not including resistor tolerance or output offset on the op amp.
4. For 50μA ≤ I_1, I_2, I_4 ≤ 250μA.

Errors caused by input offsets.

$$V_0 = \frac{R_0 R_4}{R_1 R_2}\left[\frac{V_x V_y}{V_z} \pm \frac{1}{V_z} V_y V_{osx} \pm V_x V_{osy} \pm V_0 V_{osz} \pm V_{osx} V_{osy}\right]$$

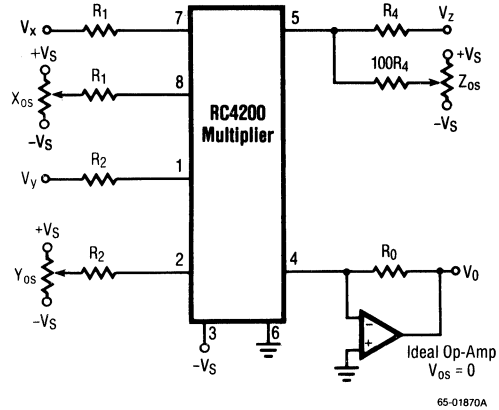
V_y Feedthrough

V_x Feedthrough

Scaling Error

Output Offset Error

Systems errors can be greatly reduced by externally trimming the input offset voltages of the 4200. (±0.3% F.S. for 4200 and ±0.1% F.S. for 4200A.)



if; $X_{os} = V_{osx}$, $Y_{os} = V_{osy}$, $Z_{os} = -V_{osz}$,

$$\text{then } V_0 = \frac{V_x V_y}{V_z}\frac{R_0 R_4}{R_1 R_2} \pm 0.3\%\ \text{F.S.}^{(3)}$$

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Figure 14. 4200 With Input Offset Adjustment

Extended Range Circuit Errors

The extended range configurations have a disadvantage in that additional accuracy errors may be introduced by resistor product mismatching.

Multiplier (Figure 6)

An error in resistor product matching will cause an equivalent feedthrough or output offset error:

1. $R_1R_b = R_{cx}R_d \pm \alpha$,
   V_x feedthrough ($V_y = 0$) = $\pm\alpha V_x$
2. $R_2R_a = R_{cy}R_d \pm \beta$,
   V_y feedthrough ($V_x = 0$) = $\pm\beta V_y$
3. $R_aR_b = R_cR_d \pm \gamma$,
   V_0 offset ($V_x = V_y = 0$) = $\pm\gamma V_{REF}$*

*Output offset errors can always be trimmed out with the output op amp offset adjust, $V_{os}(R_{16})$.

Reducing Mis-Match Errors (Figure 6)

You need not run out and buy .01% resistors to reduce resistor product mis-match errors. Here are a couple of ways to squeeze maximum accuracy out of the extended range multiplier (see Figure 6) using 1% resistors.

Method #1

V_x feedthrough, for example, occurs when $V_y = 0$ and $V_{osy} \neq 0$. This V_x feedthrough will equal $\pm V_xV_{osy}$. Also, if $V_{osz} \neq 0$, there is a V_x feedthrough equal to $\pm V_xV_{osz}$. A resistor-product error of α will cause a V_x feedthrough of $\pm \alpha V_x$. Likewise, V_y feedthrough errors are: $\pm V_yV_{osx}$, $\pm V_yV_{osz}$ and $\pm \beta V_y$.

Total feedthrough =
$\pm V_xV_{osy} \pm V_yV_{osx} \pm \alpha V_x \pm \beta V_y \pm (V_x + V_y)\, V_{osz}$

By carefully adjusting $X_{os}(R_5)$, $Y_{os}(R9)$ and $Z_{os}(R_{20})$ this equation can be made to very nearly equal zero and the feedthrough error will practically disappear.

A residual offset will probably remain which can be trimmed out with $V_{os}(R_{16})$ at the output op amp.

Method #2

Notice that the ratios of $R_1R_b : R_{cx}R_d$ and $R_2R_a : R_{cy}R_d$ are both dependent on R_d, also that R_1, R_2, R_a and R_b are all functions of the maximum input requirements. By designing a multiplier for the same input ranges on both V_x and V_y then $R_1 = R_2$, $R_{cx} = R_{cy}$ and $R_a = R_b$. (Note: It is acceptable to design a four quadrant multiplier and use only two quadrants of it.)

Select R_d to be 1% or 2% below (or above) the calculated value. This will cause α and β to both be positive (or negative) by nearly the same amount. Now the effective value of R_d can be trimmed with an offset adjustment $Z_{os}(R_{20})$ on pin 5.

This technique will cause: 1) a slight gain error which can be compensated for with the R_0 value, and 2) an output offset error that can be trimmed out with $V_{os}(R_{16})$ on the output op amp.

Extended Range Divider (Figure 8)

The only crossproduct error of interest is the V_z feedthrough ($V_x = 0$ and $V_{osx} \neq 0$) which is easily adjusted with $X_{os}(R_5)$.

Resistor product mis-match will cause scaling errors (gain) that could be a problem for very low values of V_z. Adjustments to $Y_{os}(R_{18})$ can be made to improve the high gain accuracy.

Square Root and Squaring (Figures 10 and 12)

These circuits are functions of single variables so feedthrough, as such, is not a consideration. Crossproduct errors will effect incremental accuracy that can be corrected with $Y_{os}(R_{14})$ or $Z_{os}(R_{10})$.

Appendix 2 — Applications

Design Considerations for RMS-to-DC Circuits

Average Value

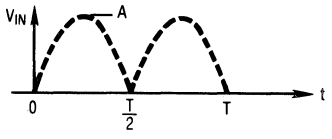
Consider $V_{in} = A\sin\omega t$. By definition,

$$V_{AVG} \equiv \frac{2}{T}\int_0^{\frac{T}{2}} V_{in}dt$$

Where T = Period

$\omega = 2\pi f$

$= \frac{2\pi}{T}$



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$$V_{AVG} \equiv \frac{2}{T}\int_0^{\frac{T}{2}} A\sin\omega t\, dt$$

$$= \frac{2A}{T}\left[-\frac{1}{\omega}\cos\omega t\right]_0^{\frac{T}{2}}$$

$$= \frac{2A}{2\pi}\left[-\cos(\pi) + \cos(0)\right]$$

$$= \frac{2}{\pi}A$$

Avg. Value of $A\sin\omega t$ is $\frac{2}{\pi}A$

RMS Value

Again consider $V_{in} = A\sin\omega t$

$$V_{rms} = \sqrt{V_{AVG}} = \sqrt{\frac{1}{T}\int_0^T [V_{in}]^2\, dt}$$

V_{rms} for $A\sin\omega t$:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^{\frac{T}{2}} A^2\sin^2\omega t\, dt}$$

$$= \sqrt{\frac{A^2}{T}\int_0^T\left(\frac{1}{2} - \frac{1}{2}\cos 2\omega t\right)dt}$$

$$= \sqrt{\frac{A^2}{2}\left(\frac{T}{2} - \frac{1}{4\omega}\sin 2\omega t\right)_0^T}$$

$$= \sqrt{\frac{A^2}{T}\left(\frac{T}{2}\right)}$$

$$= \sqrt{\frac{A^2}{2}}$$

therefore the rms value of $A\sin\omega t$ becomes:

$$V_{rms} = \frac{A}{\sqrt{2}}$$

RMS Value for Rectified Sine Wave

Consider $V_{in} = |A\sin\omega t|$, a rectified wave. To solve, integrate over each half cycle.

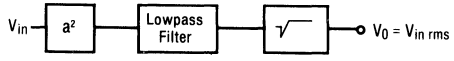
$$\text{i.e. } \frac{1}{T}\int_0^T V_{in}^2\, dt =$$

$$\frac{1}{T}\left[\int_0^{\frac{T}{2}} A^2\sin^2\omega t\, dt + \int_{\frac{T}{2}}^T (-A\sin\omega t)^2 dt\right]$$

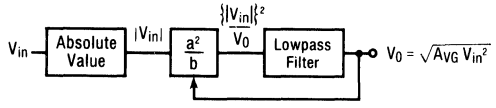
This is the same as $\frac{1}{1}\int_0^T A^2\sin^2\omega t\, dt$

so, $|A\sin\omega t|_{rms} = A\sin\omega t_{rms}$

Practical Consideration: $|A\sin\omega t|$ has high-order harmonics; $A\sin\omega t$ does not. Therefore, non-ideal integrators may cause different errors for two approaches:



(a)



(b)

$$\text{Avg}\left\{\frac{V_{in}^2}{V_0}\right\} = V_0$$

$$\text{implies } V_0 = \sqrt{\text{Avg}\{|V_{in}|^2\}}$$

$$V_0 = \sqrt{\text{Avg } V_{in}^2}$$

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Figure 15

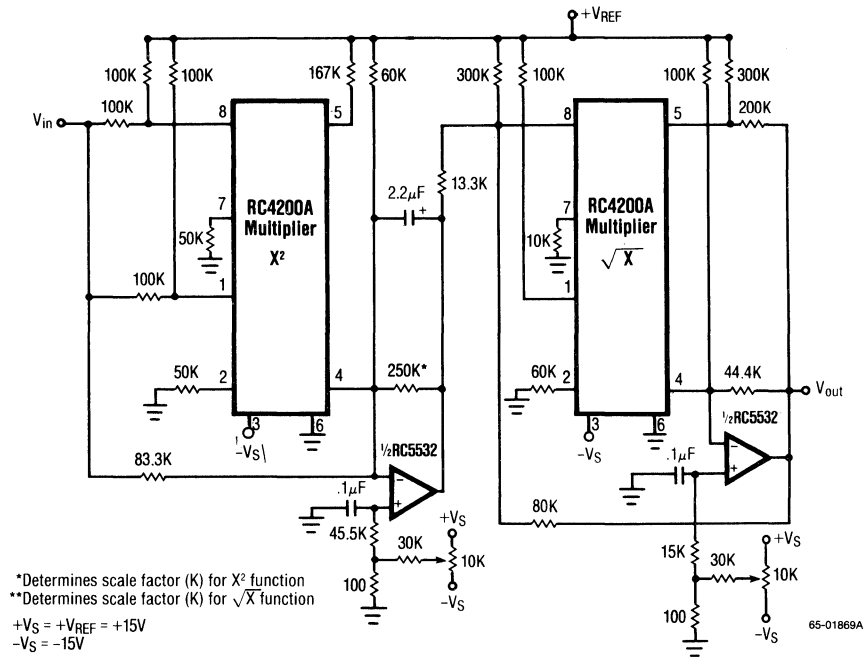


Figure 16. RMS to DC Converter $V_{out} = \sqrt{\int V_{in}^2}$

Amplitude Modulator with A.G.C. (Figure 17)

In many AC modulator applications unwanted output modulation is caused by variations in carrier input amplitude. The versatility of the RC4200 multiplier can be utilized to eliminate this undesired fluctuation. The extended range multiplier circuit (Figure 5) shows an output amplitude inversely proportional to the reference voltage V_{REF}.

$$\text{i.e., } V_0 = \frac{V_x V_y}{V_{REF}} \frac{R_0 R_d}{R_1 R_2}$$

By making V_{REF} proportional to V_y (where V_y is the carrier input) such that:

$$V_{REF} = V_H = f(|V_y|),$$

Then the denominator becomes a variable value that automatically provides constant gain, such that the modulating input (V_x) modulates the carrier (V_y) with a fixed scale factor even though the carrier varies in amplitude.

If V_H is made proportional to the average value of $A\sin\omega t$ (i.e., $2A/\pi$) and scaled by a value of $\pi/2$ then:

$$V_H = A$$

and if: V_x = Modulating input (V_M)
and: V_y = Carrier input ($A\sin\omega t$)

then: $V_0 = K V_M \sin\omega t$ where $K = \frac{R_0 R_d}{R_1 R_2}$

The resistor scaling is determined by the dynamic range of the carrier variation and modulating input.

The resistor values are solved, as with the other extended range circuits, in terms of the input voltages.

Input voltages:
Modulation Voltage (V_M): $0 \le V_M \le V_x(\text{max.})$
Carrier (V_y: $V_y = A\sin\omega t$
Carrier amplitude fluctuation (ΔA):
$A(\text{min.})\sin\omega t \le V_y \le A(\text{max.})\sin\Omega\omega t$
Dynamic Range (N): A(max.)/A(min.)
$A(\text{max.}) = V_H(\text{max.})$ and $A(\text{min.}) = V_H(\text{min.})$

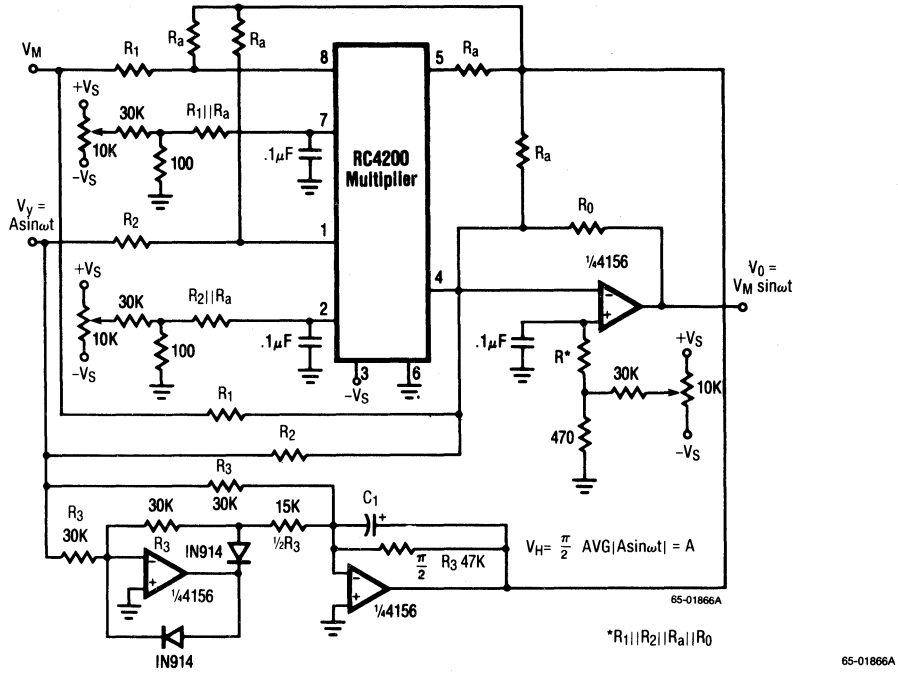


Figure 17. Amplitude Modulator with A.G.C.

The maximum and minimum values for I_1 and I_2 lead to:

$$I_1(max.) = \frac{V_x(max.)}{R_1} + \frac{V_H(max.)}{R_a} = 250\mu A$$

$$I_1(min.) = \frac{V_H(min.)}{R_a} = 50\mu A \quad V_M(min.) = 0$$

$$I_2(max.) = \frac{A(max.)}{R_2} + \frac{V_H(max.)}{R_a} = 250\mu A$$

$$I_2(min.) = \frac{V_H(min.)}{R_a} = 50\mu A$$

For a dynamic range of N, where

$$N = \frac{A(max.)}{A(min.)} < 5,$$

These equations combine to yield:

$$R_1 = \frac{V_x(max.)}{(5 - N)50\mu A}, \; R_2 \frac{A(max.)}{(5 - N)50\mu A},$$

$$R_a = \frac{A(min.)}{50\mu A} \text{ and } R_0 = K \frac{R_1R_2}{R_a}$$

Example #1

$V_y = A\sin\omega t$ $2.5V \leq A \leq 10V$, therefore N = 4
$0V \leq V_M \leq 10V$, therefore $V_x(max.) = 10V$
K = 1, therefore $V_0 = V_M \sin\omega t$

$$R_1 = \frac{V_x(max.)}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_2 = \frac{A(max.)}{50\mu A} = \frac{10V}{50\mu A} = 200K$$

$$R_a = \frac{A(min.)}{50\mu A} = \frac{2.5V}{50\mu A} = 50K$$

$$R_0 = K \frac{R_1R_2}{R_a} = 1 \frac{200K \times 200K}{50K} = 800K$$

Example #2

$V_y = A\sin\omega t$ $3 \leq A \leq 6$, therefore N = 2
$0V \leq V_M \leq 8V$, therefore $V_x(max.) = 8V$
K = .2, therefore $V_0 = .2V_M\sin\omega t$
so:
$R_1 = 53.3K$, $R_2 = 40K$
$R_a = 60K$ and $R_0 = 7.11K$

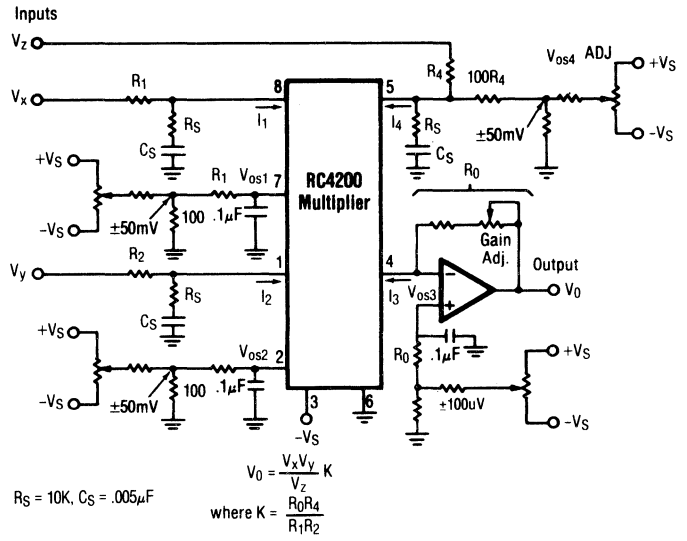


Figure 18. First Quadrant Multiplier/Divider

Limited Range, First Quadrant Applications

The following circuit has the advantage that cross-product errors are due only to input offsets and nonlinearity error is slightly less for lower input currents.

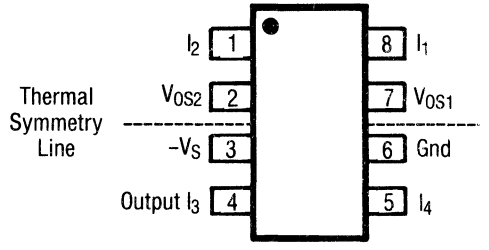
The circuit also has no standby current to add to the noise content although the signal-to-noise ratio worsens at very low input currents (1–5μA) due to the noise current of the input stages.

The R_SC_S filter circuits are added to each input to improve the stability for input currents below 50μA.

Caution

The bandpass drops off significantly for lower currents (<50μA) and nonsymmetrical rise and fall times can cause second harmonic distortion.

Thermal Symmetry



The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that sources generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.

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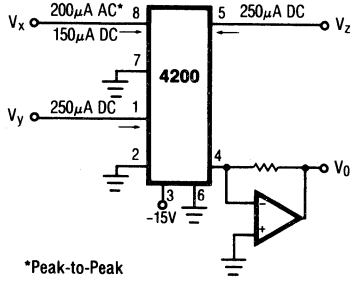
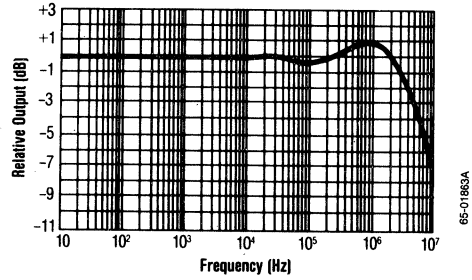
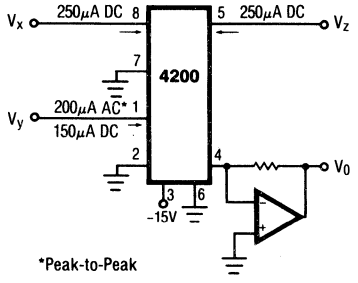
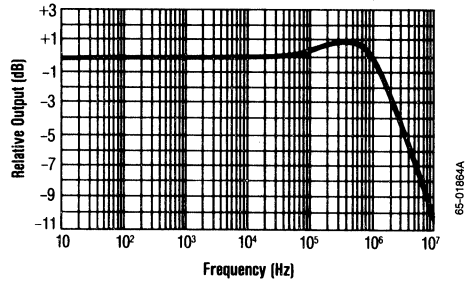
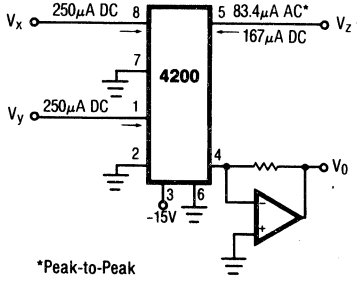

V_x
200μA AC* 8
150μA DC
5 250μA DC
V_z
7
4200
V_y
250μA DC 1
2
4
V_0
3
6
-15V
*Peak-to-Peak


+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-01863A


V_x
250μA DC 8
5 250μA DC
V_z
7
4200
V_y
200μA AC* 1
150μA DC
2
4
V_0
3
6
-15V
*Peak-to-Peak


+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-01864A


V_x
250μA DC 8
5 83.4μA AC*
167μA DC
V_z
7
4200
V_y
250μA DC 1
2
4
V_0
3
6
-15V
*Peak-to-Peak

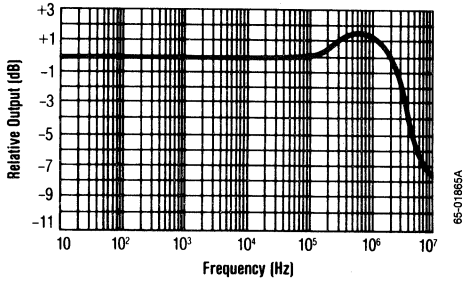

+3
+1
-1
-3
-5
-7
-9
-11
Relative Output (dB)
10
10^2
10^3
10^4
10^5
10^6
10^7
Frequency (Hz)
65-01865A

Figure 19.

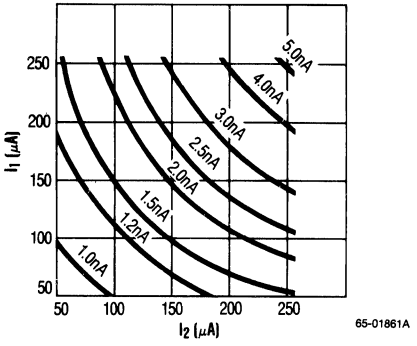


Figure 20a. Output Noise Current vs. Input Current (I_4 = 250μA)

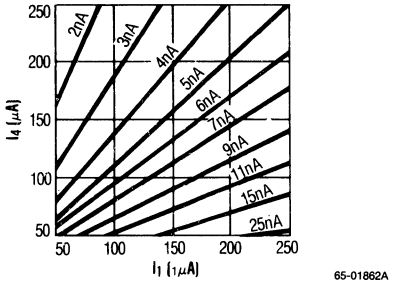


Figure 20b. Output Noise Current vs. Input Current (I_2 = 250μA)

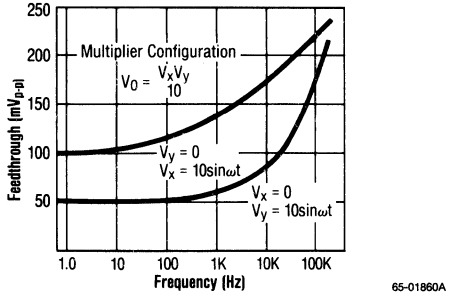
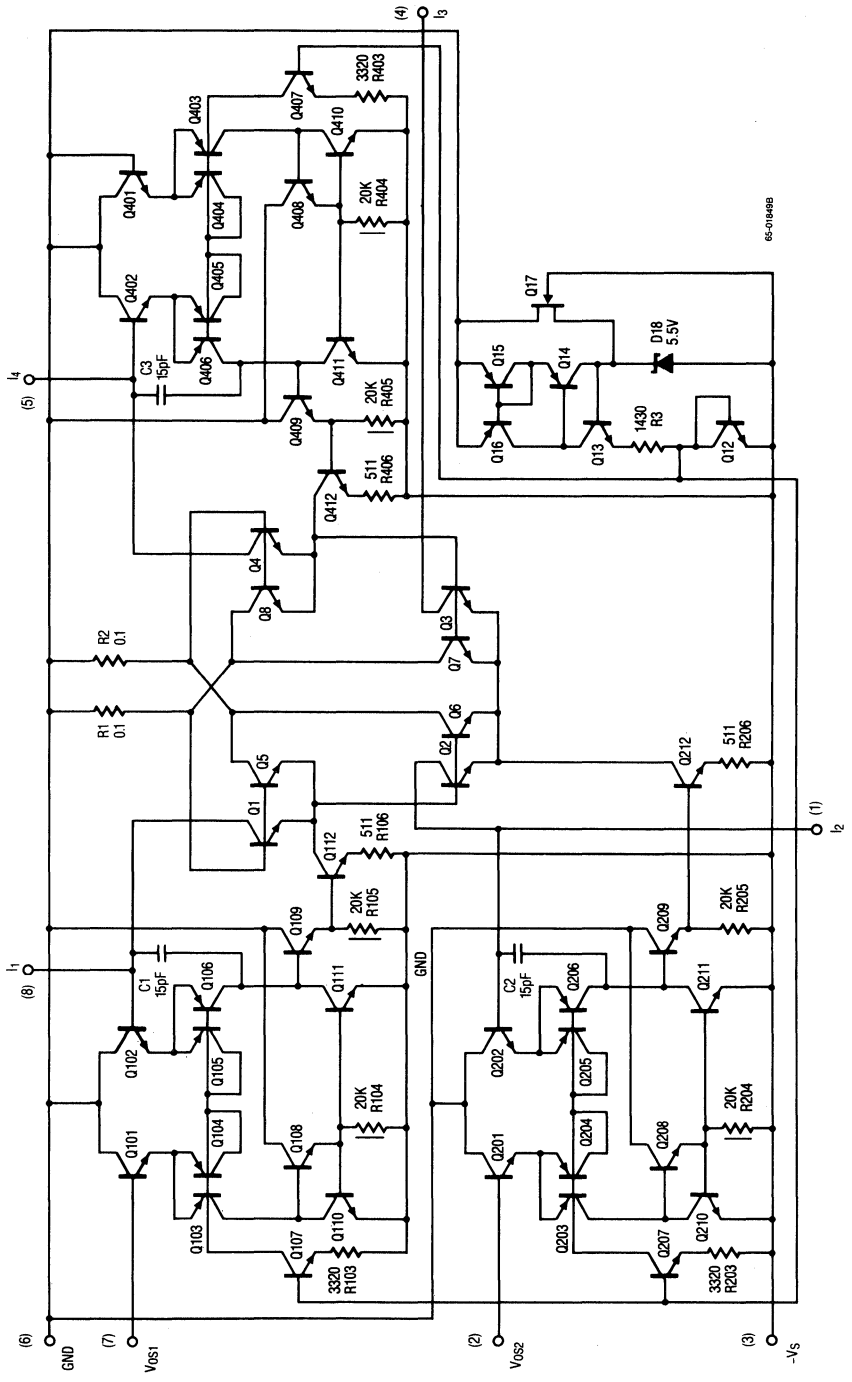


Figure 21. AC Feedthrough vs. Frequency

Schematic Diagram



RC4444
4 × 4 × 2 Balanced Switching Crosspoint Array

Features

- Low bidirectional R_{ON}
- High R_{OFF}
- Excellent matching of gates
- Low capacitance
- High rate firing
- Predictable holding current

Description

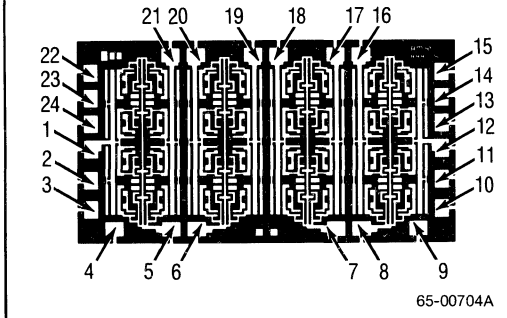
The RC4444 is a monolithic dielectrically isolated crosspoint array arranged into a 4 × 4 × 2 matrix. The primary application is for balanced switching of 600Ω transmission lines. The ring and tip are selected by selective biasing of the P+ and P- gate.

Designed to replace reed relays in telephone switchboards, it does not require a constant gate drive to keep the SCR in the "ON" condition. It is several orders faster, with no bouncing, and has a much longer operating life than its mechanical counterpart.

The 16 SCR pairs with the gating system are packaged in a 24-pin dual in-line package.

The RC4444 is a monolithic pin-for-pin replacement for the MC3416 and MCBH7601.

Mask Pattern

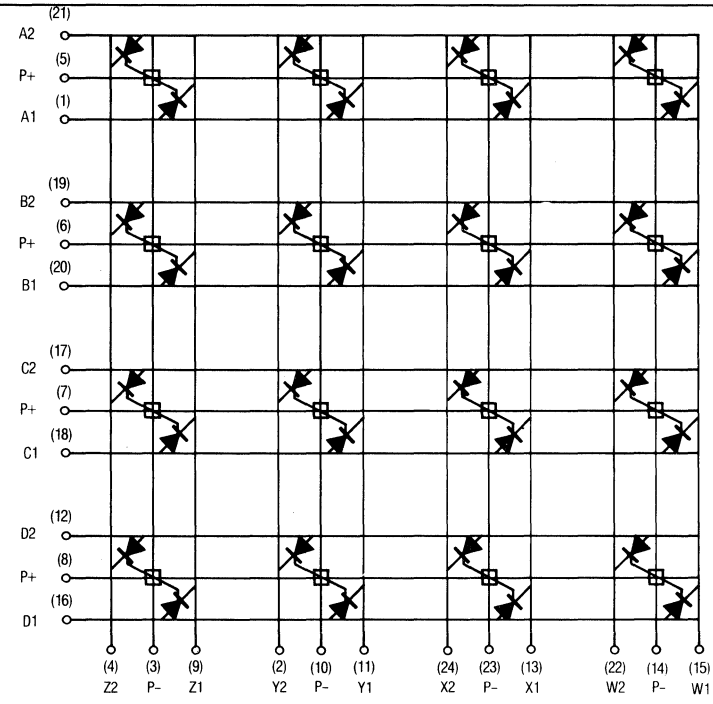


Die Size: 60 x 108 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

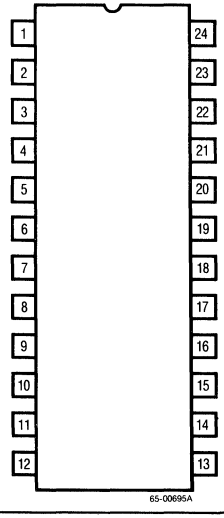
	24-Lead Plastic DIP	24-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A < 50°C	555mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	135°C/W	120°C/W
For T_A > 50°C Derate at	7.41mW per °C	8.33mW per °C

Block Diagram



Connection Information

24-Lead
Dual In-Line Package
(Top View)



Pin	Function	Pin	Function
1	Anode A1	13	Cathode X1
2	Cathode Y2	14	Row Select W
3	Row Select Z	15	Cathode W1
4	Cathode Z2	16	Anode D1
5	Column Select A	17	Anode C2
6	Column Select B	18	Anode C1
7	Column Select C	19	Anode B2
8	Column Select D	20	Anode B1
9	Cathode Z1	21	Anode A2
10	Row Select Y	22	Cathode W2
11	Cathode Y1	23	Row Select X
12	Anode D2	24	Cathode X2

Absolute Maximum Ratings

Operating Voltage[1] ..... +25V
Operating Current per Crosspoint 100mA
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
RC4444 ..... 0°C to +70°C
Lead Soldering Temperature
(60 Sec) ..... +300°C

Notes: 1. Maximum voltage from anode to cathode.

Ordering Information

Part Number	Package	Operating Temperature Range
RC4444N	N	0°C to +70°C
RC4444D	D	0°C to +70°C

Notes:
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

Electrical Characteristics ($0°C \leq T_A \leq +70°C$ unless otherwise noted)

Parameters	Test Conditions	Min	Typ	Max	Units
Anode-Cathode Breakdown Voltage	$I_{AK} = 25\mu A$	25			V
Cathode-Anode Breakdown Voltage	$I_{KA} = 25\mu A$	25			V
Base-Cathode Breakdown Voltage	$I_{BK} = 25\mu A$	25			V
Cathode-Base Breakdown Voltage	$I_{KB} = 25\mu A$	25			V
Base-Emitter Breakdown Voltage	$I_{BE} = 25\mu A$	25			V
Emitter-Cathode Breakdown Voltage	$I_{EK} = 25\mu A$	25			V
OFF State Resistance	$V_{AK} = 10V$	100			MΩ
Dynamic ON Resistance	Center Current = 10mA	4.0		12	Ω
	Center Current = 20mA	2.0		10	
Holding Current		0.9		3.8	mA
Enable Current	$V_{BE} = 1.5V$ (Fig. 2)	4.0			mA
Anode-Cathode ON Voltage	$I_{AK} = 10mA$			1.0	V
	$I_{AK} = 20mA$			1.1	
Gate Sharing Current Ratio at Cathodes	Under Select Conditions with Anodes Open (Fig. 1)	0.8		1.25	mA/mA
Inhibit Voltage	$V_B = 3.0V$ (Fig. 3)			0.3	V
Inhibit Current	$V_B = 3.0V$ (Fig. 3)			0.1	mA
OFF State Capacitance	$V_{AK} = 0V$			2.0	pF
Turn-ON Time	(Fig. 5)			1.0	μS
Minimum Voltage Ramp	Which Could Fire the SCR Under Transient Conditions (Fig. 5)	800			V/μS

Test Circuits

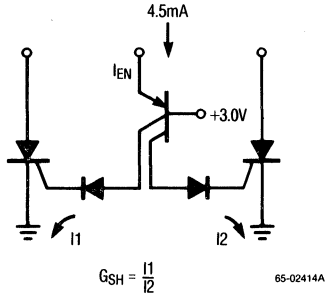


Figure 1. Test Circuit for Gate Sharing Current Ratio

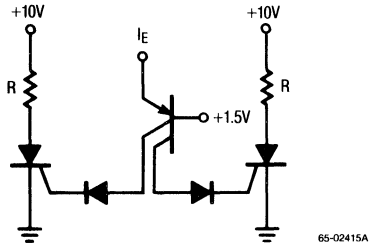


Figure 2. Enable Current (both SCRs must turn on)

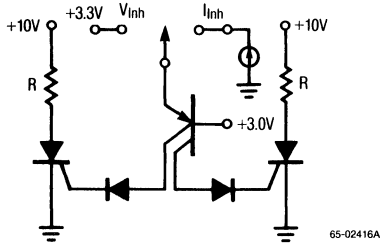


Figure 3. Inhibit Voltage and Inhibit Current (both SCRs must remain off)

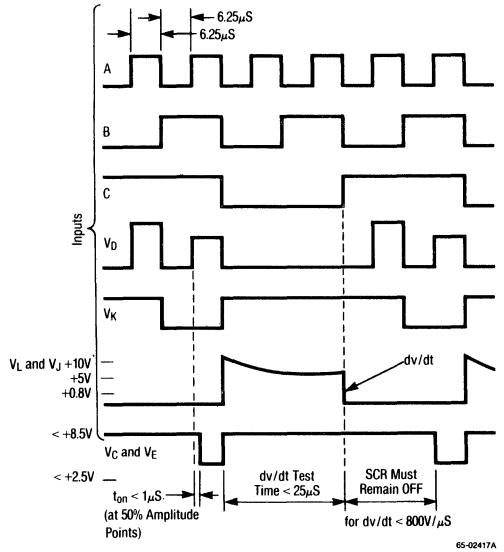


Figure 4. Test Waveforms for dv/dt and t_{on}

Test Circuits (Continued)

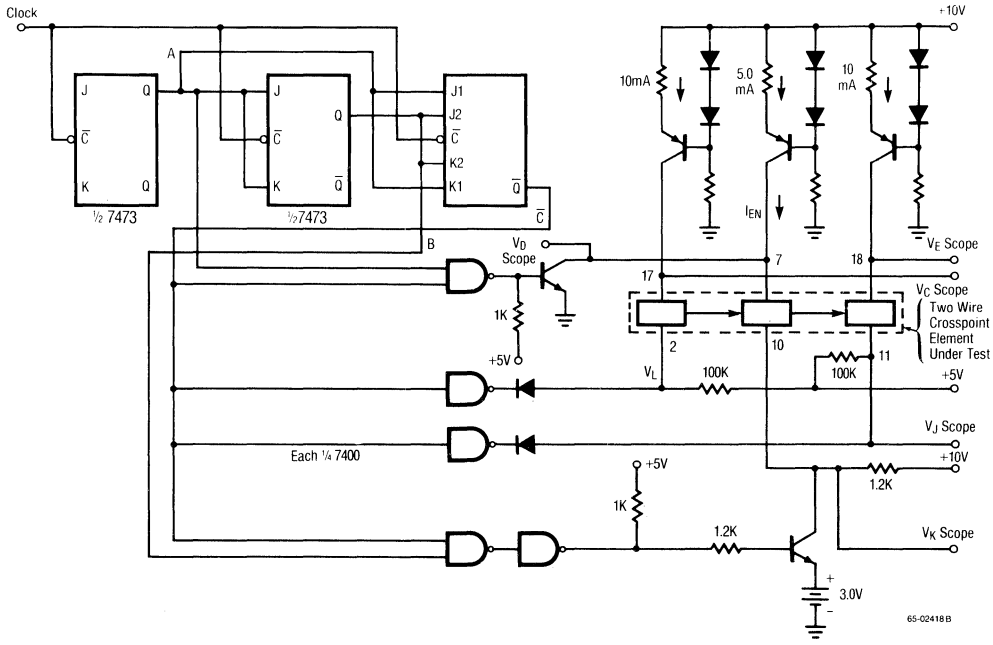
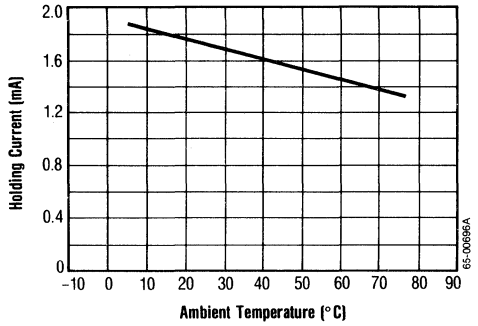


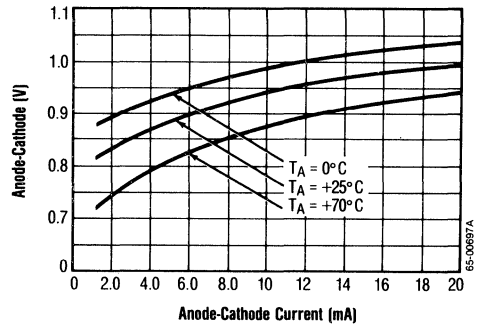
Figure 5. Test Circuit for dv/dt and t_{on}

Typical Performance Characteristics

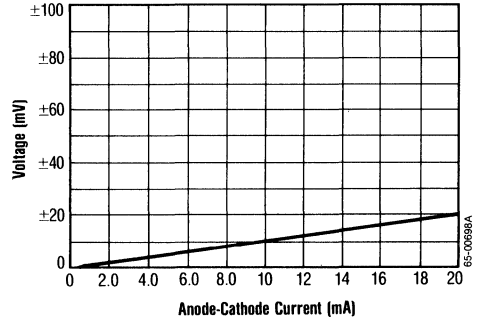
Holding Current vs. Ambient Temperature



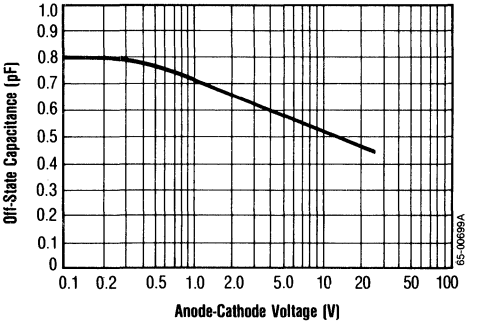
Anode-Cathode on Voltage vs. Current and Temperature



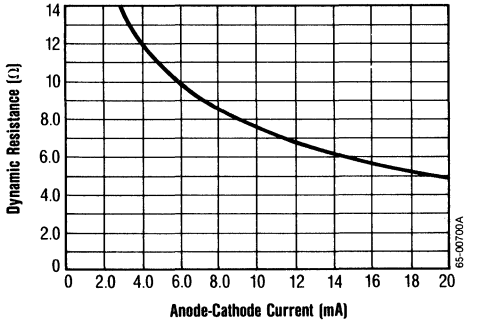
Difference in Anode-Cathode on Voltage (Between Associate Pairs of SCRs) vs. Anode-Cathode Current



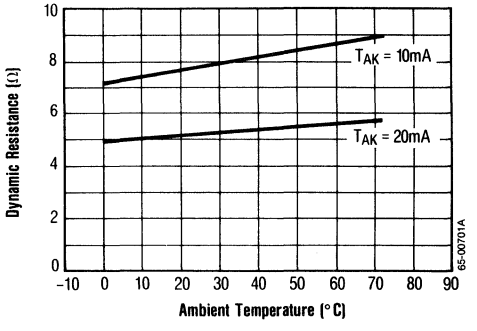
Off-Site Capacitance vs. Anode-Cathode Voltage



Dynamic on Resistance vs. Anode-Cathode Current

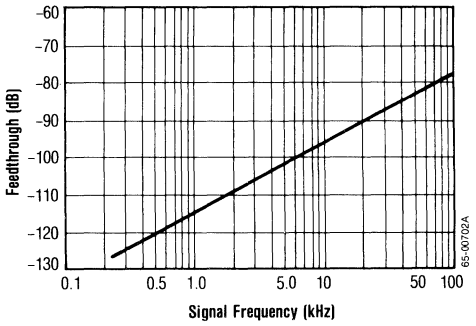


Dynamic on Resistance vs. Ambient Temperature

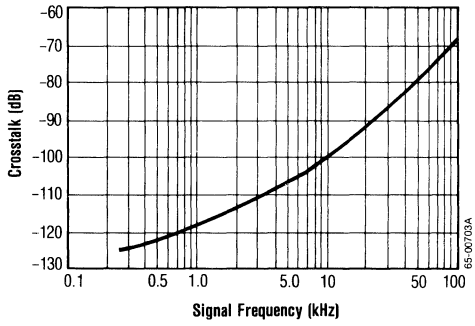


Typical Performance Characteristics (Continued)

Feedthrough vs. Signal Frequency



Crosstalk vs. Signal Frequency



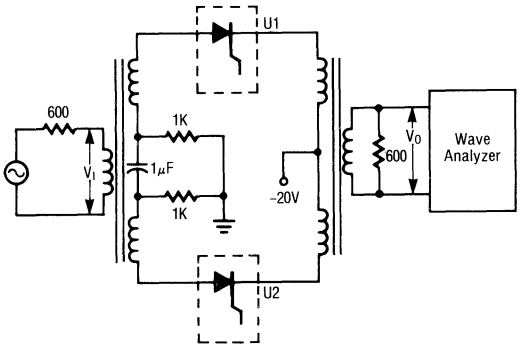


Figure 6. Test Circuit for Feedthrough vs. Frequency

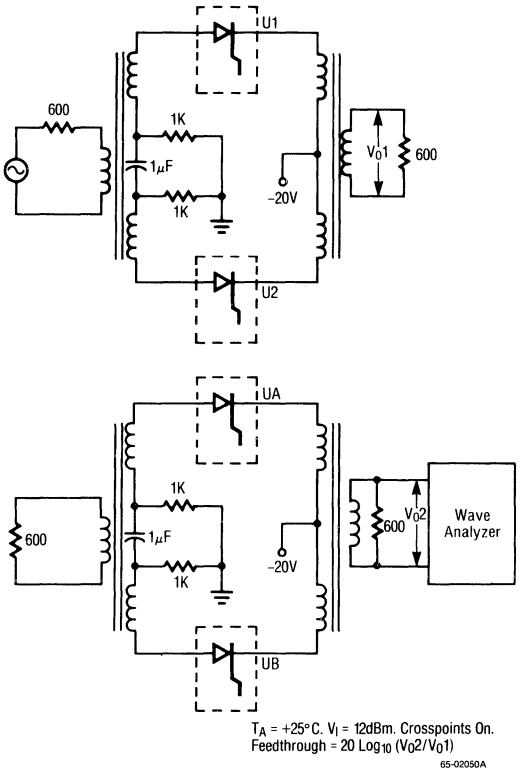


Figure 7. Test Circuit for Crosstalk vs. Frequency

Typical Applications

The RC4444 crosspoint switch is designed to provide a low-loss analog switching element for telephony signals. It can be addressed and controlled from standard binary decoders and is CMOS compatible. With proper system organization the RC4444 can significantly reduce the size and cost of existing crosspoint matrices.

Signal Path Considerations

The RC4444 is a balanced 4 × 4 2-wire crosspoint array. It is ideal for balanced transmission systems, but may be applied effectively in a number of single ended applications. Multiple chips may be interconnected to form larger crosspoint arrays. The major design constraint in using SCR crosspoints is that a forward DC current must be maintained through the SCR to retain an AC signal path. This requires that each subscriber-input to the array be capable of sourcing DC current as well as its AC signal. With each subscriber acting as a DC source, each trunk output then acts as a current sink. The instrument-to-trunk connection in Figure 8 shows this configuration. However, with each subscriber acting as a DC source, some method of interconnecting them without a trunk must be provided. Such a local or intercom termination is shown in Figure 9. Here both subscribers source DC current and exchange AC signals. The central current sink accepts current from both subscribers while the high output impedance of the current sink does not disturb the system.

These configurations are system compatible. The DC current restriction is not a restriction in the design of an efficient crosspoint array. Because of the current sink terminations, a signal path may use differing numbers of crosspoints in any connection or in two sides of the same connection further relaxing restrictions in array design.

Figure 10 demonstrates circuit operation. S1, S2, and S3 are open. The Crosspoint SCRs are off as they have no gate drive or DC current path through S1. By closing S2 and S3, gate drive is provided, but the SCRs still remain off as there is no DC current path to hold them on. Close S1 and the circuit is enabled, but with S2 and S3 off there is still no signal path. Closing S2 and S3 with S1 closed — current is injected into both gates and they switch on. DC current through R_L splits around the center-tapped winding and flows through each SCR, back through the lower winding and through S1 to ground. If S2 and S3 are opened, that current path still remains and the SCRs remain on. If an AC signal is injected at either G1 or G2, it will be transmitted to the other signal port with negligible loss in the SCRs. To disconnect the AC signal path the SCRs must be commutated off. By opening S1 the DC current path is interrupted and the SCRs switch off. The AC signal path is disconnected. With S1 closed the circuit is enabled and may be addressed again from S2 and S3. This circuit demonstrates a balanced transmission configuration. The transmission characteristics of the SCRs simulate a relay contact in that the AC signal does not incur a contact voltage drop across the crosspoint. The memory characteristics of the crosspoint are demonstrated by the selective application of S1, S2, and S3.

The selection of R_L is governed by the power supply voltage and the desired DC current. If 10mA is to flow through each SCR then R_L must pass 20mA. Thus, $(+V_S - V_{AK})/R_L = 20mA$. The selection of R_P is governed by the characteristics for crosspoint turn on. Adequate enable current must be injected into the column select and R_P should drop at least 1.5V. The PNP transistor has a typical gain of one. Thus, R_P should pass at least 2mA to provide 4mA column select current.

Addressing Considerations

The RC4444 crosspoint switch is addressed by selecting and turning on the PNP transistor that controls the SCR pair desired. The drive requirements of the RC4444 can be met with standard CMOS outputs. A particular crosspoint is addressed by putting a logical "1" on the emitter and a logical "0" on the base of the appropriate transistor. A resistor in the base circuit of the transistor is required to limit the current and must also drop 1.5V to assure forward bias of the two diodes in the collector circuits.

The gate current required for SCR turn on is 1mA typically. CMOS one-of-n decoders are available that provide both active high and active low outputs and are well suited for standard addressing organizations. The major design constraint in organizing the addressing structure is that any signal path which is to be addressed must create a DC path from a source to a sink. If that path requires two crosspoints they must be addressed simultaneously. Of course, once the path is selected, the addressing hardware is free to initiate other signal paths. To meet the DC path requirement, crosspoint arrays should be designed in blocks such that any given DC path requires only one crosspoint per block. A signal path, however, may still use two crosspoints in the same block by sequentially addressing two DC paths to the same terminator. For example, the left or right pairs of crosspoints in Figure 9 must be addressed simultaneously but the left pair may be addressed in sequence after addressing the right pair. This is not a difficult constraint to meet and it does not require unnecessary addressing hardware.

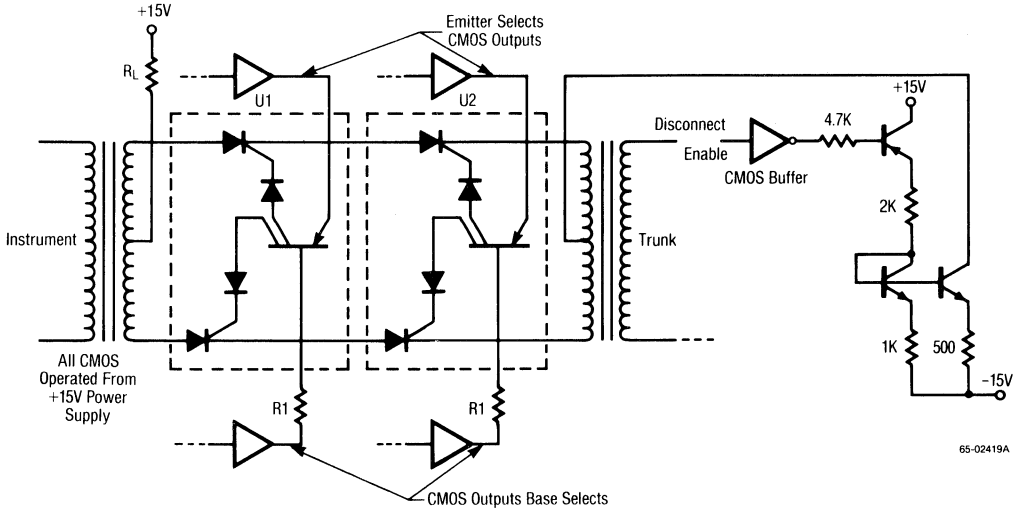


Figure 8. Instrument-to-Trunk Connection

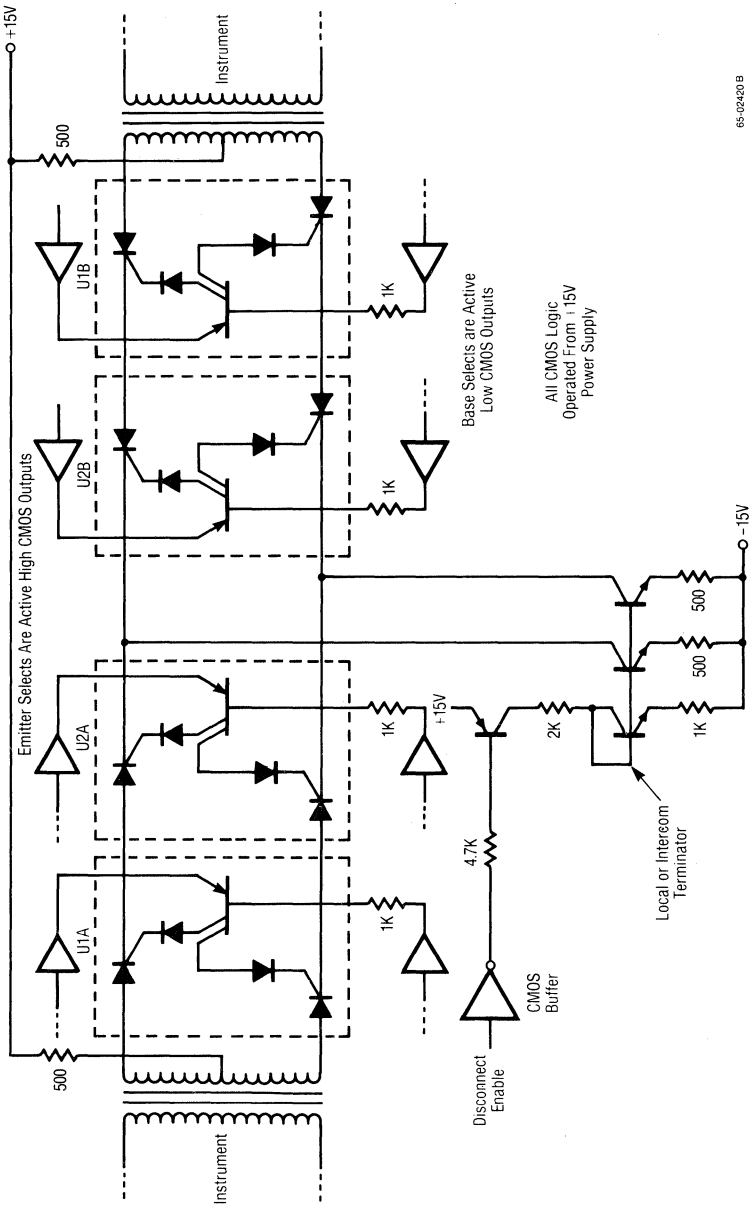
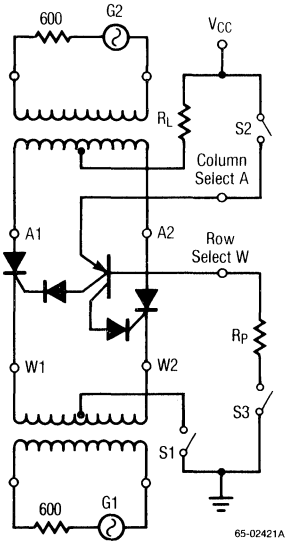


Figure 9. Typical Instrument-to-Instrument Connection

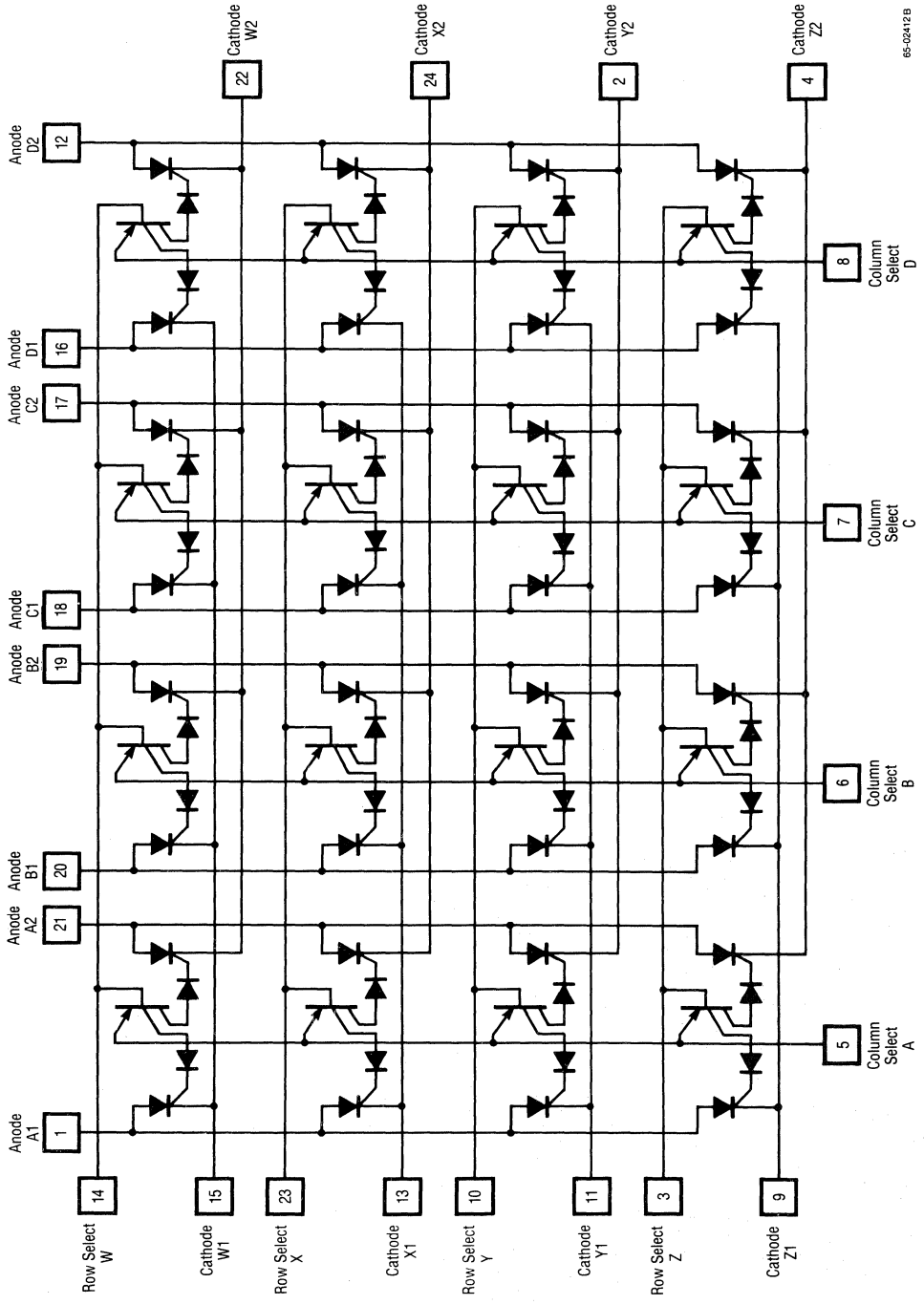


S1	S2	S3	Line Condition
ON	X	OFF	Enabled, Not Connected
ON	OFF	X	Enabled, Not Connected
ON	ON	ON	Addressed and Connected
ON	X	X	G1 Connected to G2
OFF	X	X	Disconnected

X = Don't Care

Figure 10. Crosspoint Operation Demonstration Circuit

Simplified Schematic Diagram



RC4447 Quad PIN Diode Switch Driver

Features

- Monolithic construction
- Four drivers per package
- True and complementary outputs
- TTL/DTL compatible inputs
- Drives PIN diodes or MOSFETs
- Pulse rates to 10 MHz
- Available in dice form
- Mil-Std-883 versions

Description

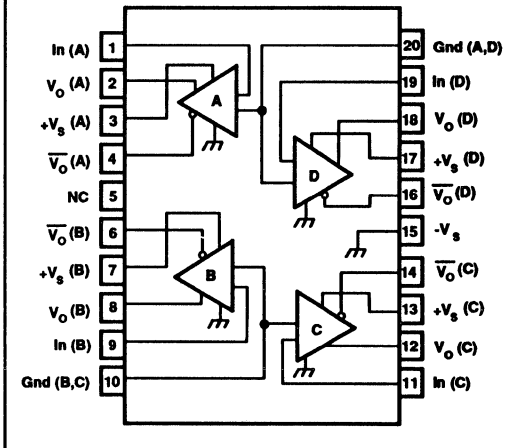
The RC4447 monolithic IC consists of four independent driver circuits. Each driver is a TTL/DTL compatible gain block designed specifically for driving PIN diode RF switches. Each driver has both true and complementary outputs and can power PIN diodes in both grounded-anode and grounded-cathode modes. The voltage and current ratings of the RC4447 make it suitable for driving low- and medium-power PIN diodes.

Constructed via a rugged Schottky bipolar fabrication process, the RC4447 provides a space efficient and cost effective alternative to hybrid devices for microwave signal switching and modulation applications. The internal stage currents of the RC4447 are closely controlled through the use of Si-Cr thin-film resistor networks, resulting in repeatable ac characteristics and a stable dc bias point. Well-matched high speed switching characteristics are provided at a moderate level of power dissipation. The maximum response time is 50 nS, allowing switching repetition rates to 10 MHz.

The RM4447 version is packaged in a 20-lead ceramic DIP and is specified over a -55 to +125°C temperature range. The RM4447 is offered with Mil-Std-883 Level B processing. High reliability dice are available with visual inspection to Mil-Std-883, Method 2010. The RC4447 is a commercial version packaged in a 20-lead plastic DIP and specified over a 0°C to +70°C range.

Connection Information

20-Lead Ceramic DIP (Top View)



Ordering Information

Type	Package	Operating Temperature Range
RC4447N	N	0°C to +70°C
RM4447S	S	-55°C to +125°C
RM4447S/883B	S	-55°C to +125°C
RM4447CH	CH	-55°C to +125°C

Notes:
/883B suffix denotes MIL-STD-883, Level B Processing.
S = 20-lead, 0.3-inch wide side-brazed ceramic DIP.
N = 20-lead, 0.3-inch wide plastic DIP.
CH = waffle-packed dice.
Contact a Raytheon Sales Office or Representative for ordering information on other package/temperature range combinations.

Absolute Maximum Ratings

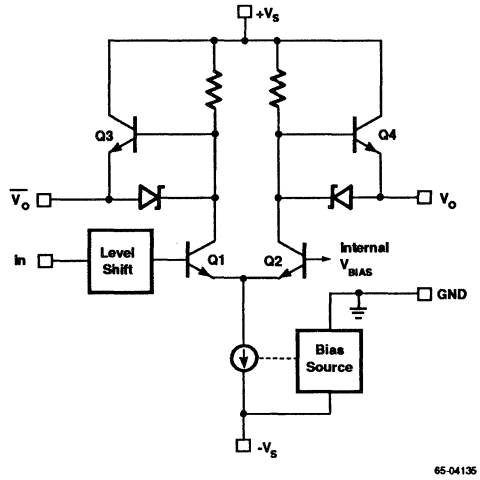
Supply Voltage ($+V_S$ to $-V_S$) ..... +22V
($+V_S$ to GND) ..... +10V
($-V_S$ to GND) ..... -15V
Input Voltage ..... -2V to $+V_S$
Output Short Circuit ..... Not Protected
Output Current ..... -100 mA
Internal Power Dissipation ..... See Table of Thermal Characteristics
Operating Temperature Range
RM4447 ..... -55°C to +125°C
RC4447 ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Soldering Temperature (60 Sec) ..... +300°C

Thermal Characteristics

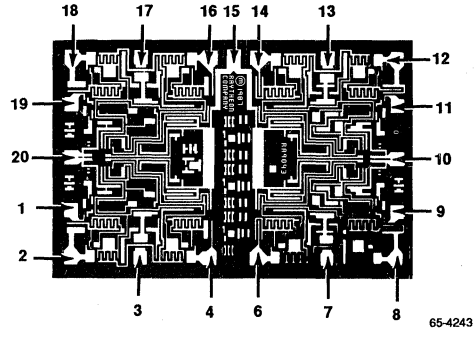
(soldered in place, still air)

	20-Lead SB Ceramic DIP	20-Lead Plastic DIP
Max. Junction Temp.	+175°C	+125°C
Max. P_D T_A <50°C	1780 mW	1250 mW
Therm. Res θ_{JC}	25°C/W	20°C/W
Therm. Res θ_{JA}	70°C/W	60°C/W
For T_A >50°C Derate at	14.2 mW/°C	16.7 mW/°C

Block Diagram



Mask Pattern



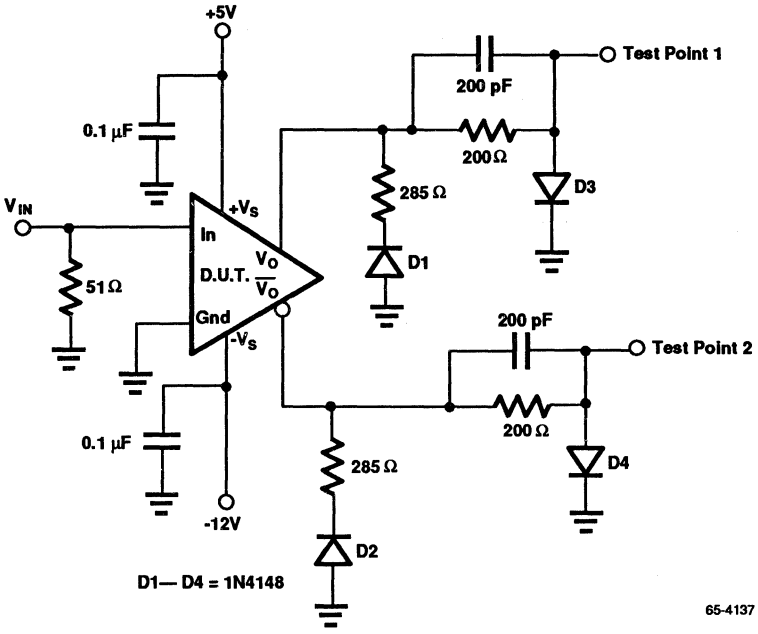
Die Size: 101 mils x 66 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics

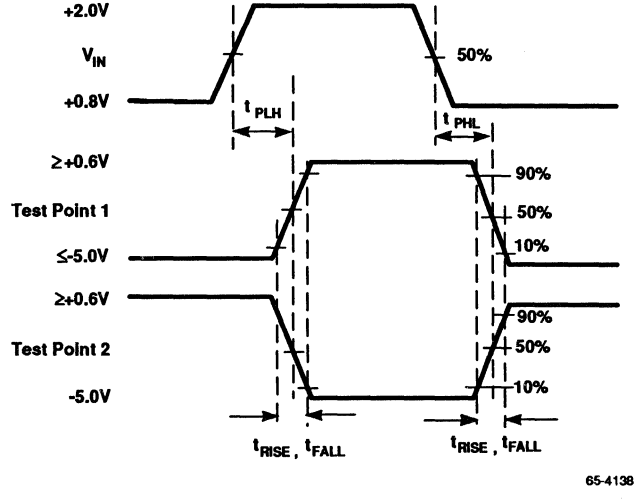
(Over the operating temperature range; V_S = +5V, -12V; unless otherwise specified)

Parameters	Test Conditions	Min	Typ	Max	Units
Output Voltage High	I_{LOAD} = 20 mA	3.0	3.5		V
Output Voltage High	I_{LOAD} = 100 µA		3.7		V
Output Voltage Low [1]	I_{LOAD} = 0, Tested at I_O		-8.0	-7.0	V
Output Voltage Low [1]	I_{LOAD} = 0,Tested at I_O Bar, V_{IN} = 2.0V		-7.7	-7.0	V
Output Source Current	V_O > +2.5V		-60	-40	mA
Output Sink Current	V_O = -6V, Tested at I_O	15	19	23	mA
Output Sink Current	$\overline{V_O}$ = -6V, Tested at I_O Bar, V_{IN} = 2.0V	15	20	23	mA
Output Impedance	V_O in low state; V_O = -6.0V		1.9		kΩ
Logic Input Levels:					
Low				0.8	V
High		2.4			V
Logic Input Currents:					
Low	V_{IN} = 0.8V		8.0	15	µA
High	V_{IN} = 2.4V		10	25	µA
Logic Input Levels:					
Low	V_S = ±10V			3.5	V
High	V_S = ±10V	5.0			V
Logic Input Currents:					
Low	V_S = ±10V; V_{IN} = 3.0V		15	40	µA
High	V_S = ±10V; V_{IN} = 7.0V		10	50	µA
Power Dissipation [3]	I_{OH} = -20 mA; V_{OL} = -6V; Two sections powered		590	700	mW
Power Dissipation [3]	I_{OH} = -20 mA; V_{OL} = -6V; V_S = +5V, -10V; Two sections powered		435	530	mW
Response Time [4]	See Response Time Test Circuit				
Tp Low to High	T_A= +25°C		35	50	nS
Tp High to Low	T_A = +25°C		30	50	nS
Response Time [4]	See Response Time Test Circuit				
Tp Low to High			40	60	nS
Tp High to Low			35	60	nS
Rise Time			10		nS
Fall Time			10		nS
Pulse Repetition Rate [4]	50% Duty Cycle; T_A = +25°C	10	14		MHz
Output Capacitance	V_O in Low state		10		pF
Input Capacitance			2.0		pF

Notes:
1. V_{OL} is a function of load resistance; see Typical Performance Characteristics, V_{OL} vs. I_{OL}.
2. Output switching characteristics apply to both true and complementary outputs.
3. Power dissipation equation: $(+V_S\text{-}V_{OH})(20mA) + (+I_{SY}\text{-}20mA)(+V_S) + (+V_S\text{-}V_{OL})(10mA) + (-V_S)(-I_{SY}\text{-}10mA)$.
4. Guaranteed by design.



Response Time Test Circuit



Response Time Test Conditions

Principles of Operation

Three functional blocks comprise the RC4447: a TTL compatible input stage/level shifter, a differential current-mode switch, and a complementary output stage. The resultant circuit is similar to a differential line driver IC, but the output is designed specifically for driving PIN diode RF switches.

Voltage Source/Current Sink Output

A fundamental design feature of the RM4447 is its NPN push-pull output stage, which employs both a voltage source (NPN emitter follower) and a current sink. Refer to the block diagram on page 2. When one of the two outputs is driven low, it sinks 19 mA (nominal) I_{OL} current that is supplied by the current source. When the output is driven high, it acts as a low impedance emitter follower, and will act as a voltage source two V_{BE} below the positive supply voltage (Q3 and Q4 in Figure 1 are Darlington-connected). Thus the output presents a low impedance in the high state, and a (relatively) high impedance (acting as a current source) in the low state.

Grounded-Cathode Application

The RC4447 was designed for driving PIN diodes in a grounded-cathode configuration, although grounded-anode circuits also work well. Both the forward PIN diode current and the PIN diode off-bias reverse voltage can be adjusted by selecting external resistor values. A simple grounded-cathode circuit is shown in Figure 1. The reverse voltage is determined by the values of I_{OL} and R2 plus the diode voltage of steering diode D1:

$$V_{REV} = I_{OL}(R2) + V_{D1}$$

Where V_{D1} = Forward Diode Voltage of D1 at $I_F = I_{OL}$.

The forward current through the PIN diode (D2) is:

$$I_{FWD} = \frac{V_{OH} - V_{D2}}{R1}$$

Where V_{D2} = Forward Diode Voltage of the PIN diode.

The off-bias voltage V_{REV} can be adjusted to any value within the compliance range of the current source. The compliance range is determined at the negative extreme by the voltage at which the differential switch transistor saturates. The point at which the output saturates is a function of the positive supply voltage (see the discussion on saturation under "Grounded Anode Application" below.) At $+V_S$ = 5V, the output will saturate at about -7.7V. The positive

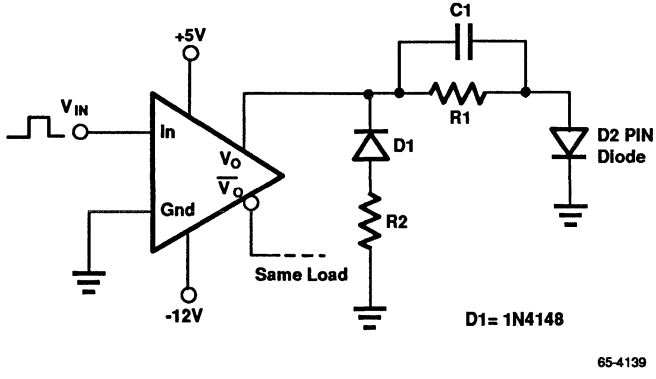


Figure 1. Grounded Cathode Application

extreme of the compliance range can be as high as $+V_s$.

The response time can be improved a small amount by limiting the input signal swing in the high state to a minimum level (+2.5V to +3V works well).

Grounded-Anode Application

In the grounded anode configuration of Figure 2, the forward PIN diode current is fixed at I_{OL}, and the off-bias reverse voltage is equal to V_{OH}. V_{OH} can be adjusted by changing the positive supply voltage as long as the Absolute Maximum Ratings aren't exceeded; V_{OH} (open circuit load) will be about 1.5V below $+V_S$. I_{OL} can be adjusted over a relatively narrow range of values by changing the value of $-V_S$. Keep in mind that changing $+V_S$ to a value other than +5V will affect both the input logic threshold level and the output sink current compliance range. The logic threshold, normally +1.4V at $+V_S = 5V$, will become:

$$V_{TH} = 0.28(+V_S)$$

The lower limit of the V_{OL} compliance range, the point at which the output transistor saturates, will also vary as the positive supply varies. See the graph of $V_{OL(SAT)}$ vs. $+V_S$ under Typical Performance Characteristics. **If either output is allowed to saturate (as might be caused by making R_{LOAD} too high in value), the response time will be relatively unaffected, but internal power dissipation will rise due to shunted I_{OL} current.** Saturating the output will have a similar effect on both grounded-anode and grounded-cathode circuits.

Raising the positive supply voltage any significant amount will change the logic threshold to be outside the range of TTL compatibility. However, the threshold can be made compatible with MOS logic families.

Power Dissipation and Thermal Effects

Allowable power dissipation determines how many sections of an RC4447 can be used in a given application. The value of allowable power dissipation depends on the type of package used and its thermal resistance qualities, and the maximum ambient temperature. In hybrid applications where a package having low thermal resistance is available, all four sections can be used to their full 60 nS speed capability over the entire military temperature range. The standard ceramic DIP package must be well heatsinked or supplied with forced-air cooling to operate all four sections at +125°C ambient

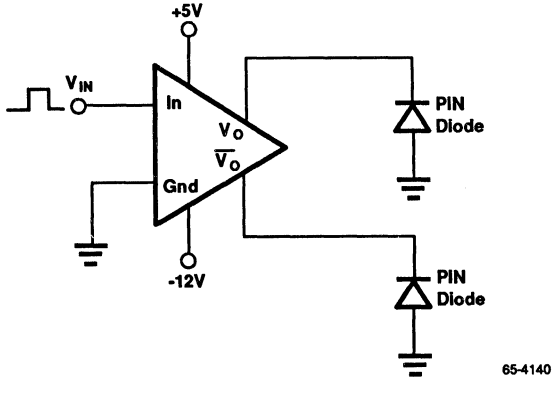


Figure 2. Grounded Anode Application

temperature. One method of reducing temperature rise is to decrease the negative supply voltage to a value less than the standard -12V; changing $-V_S$ will affect the nominal value of I_{OL} however. See the graph of I_{OL} vs. $-V_S$ under Typical Performance Characteristics. Also, reducing $-V_S$ will affect the output low saturation voltage. Make sure that there is enough headroom for the selected value of voltage.

Worst-Case Power Calculation (grounded-cathode circuit)

Several sources contribute to the total internal power dissipation. The dc terms include supply voltage, load current in the output high state, and selected output voltage in the low state. For a typical application using standard +5, -12V supplies, V_{OL} set to -6.0V, and a 20 mA I_{OH} load current, the worst-case power dissipation is:

$$P_{D(INTERNAL)} = P_{BIAS} + P_{LOW} + P_{HIGH} = 373 \text{ mW}$$

Where P_{BIAS} is the power consumed by the start-up and level shift circuitry, and P_{LOW} and P_{HIGH} are figures for power consumption in the complementary output stage. This assumes supply voltages having a maximum tolerance of 5%.

The worst case for P_{BIAS} is 81 mW:

$$P_{BIAS} = (-V_S)(I12+I13+I15+I16+I17) + (+V_S)(I12+I16)$$
$$= 12.6V(5)(1.1 \text{ mA}) + 5.25V(2)(1.1 \text{ mA})$$
$$= 81\text{mW}$$

Where the numbered currents refer to the collector currents of the respectively labeled transistors in the Internal Schematic Diagram. These transistors have equal emitter areas and, accounting for base current errors, the currents will all have the same value (1.0 mA nominal and 1.1 mA worst-case). If the negative supply voltage is changed, these currents will change in nearly direct proportion.

The worst case for P_{LOW} is 247 mW:

$$P_{LOW} = (-V_S-V_{OL})(I_{OLMAX}) + \frac{(+V_S+V_{OL}+V_{SCHOTTKY})^2}{R3}$$

$$= (12.6V-6.0V)(23 \text{ mA}) + \frac{(5.25V+6.0V+0.8V)^2}{1530}$$

$$= 247 \text{ mW}$$

Where $V_{SCHOTTKY}$ is the forward drop across D2, I_{OLMAX} is the maximum specification limit for I_{OL} and R3 is the low tolerance limit value for R3 in the Internal Schematic Diagram (±10% tolerance). Use the worst-case low value of 1530Ω for R1.

The worst case for P_{HIGH} is 45 mW:

$$P_{HIGH} = (+V_S-V_{OH})I_{LOAD} = (5.25V-3.0V)20 \text{ mA}$$
$$= 45 \text{ mW}$$

The total internal dc power dissipation is 81 mW + 247 mW + 45 mW = 373 mW.

AC Effects on Power Dissipation

A possible ac factor in the power dissipation calculation is duty cycle, but only if the outputs are asymmetrically loaded. With unequal loading, the duty cycle will determine the power contributed by P_{HIGH} and P_{LOW}. This fact can be used to advantage in saving power, as shown in the Single Output, Reduced Power Configuration of Figure 3.

Package Thermal Resistance

With both dc and ac effects accounted for, the total internal power dissipation in a typical grounded-cathode application with four sections powered is 373 mW(4) = 1.49 Watts. The thermal resistance of the 24-lead sidebraze DIP is 70°C/Watt in still air. The temperature rise will

be (70°C/Watt)(1.49) = 104°C. The maximum ambient temperature is the maximum junction temperature minus the temperature rise, or +175°C (for the sidebraze DIP) - 104°C = +71°C. This is the maximum safe ambient temperature without heatsinking, hybrid mounting, or forced-air cooling. If the power is reduced through disconnecting the $+V_S$ pins of two or more sections, then the ground pin corresponding to the two unused sections should be left open. This will shut down the bias currents associated with those sections. A further reduction in power dissipation can be obtained by reducing $-V_S$ to -10V.

Single-Output Power Saver

A method of gaining a small but useful reduction in power dissipation that can be used if complementary outputs are not required is shown in the schematic of Figure 3. The true output operates like that of the standard grounded-cathode circuit, while the inverted output has a steering diode and resistor that shunts the unused I_{OL} current to ground. There is no P_{HIGH} term for the unused output as the steering diode prevents the output from sourcing current. The I_{OL} current must flow somewhere, but in this case the majority of the power generated by I_{OL} is dissipated in the 300Ω resistor and not inside the IC. The resistor should be selected such that the IR drop does not cause the unused output to saturate (300Ω works well for -12V supplies).

Since the single-output configuration is assymetrically loaded, the duty cycle of the input signal will have a great influence on the power dissipation. A calculation of internal power dissipation with a 25% duty cycle (the true output high 25% of the time) follows.

$$P_{D(INTERNAL)} = P_{BIAS} + P_{LOW} + (\text{Duty Cycle})(P_{HIGH})$$
$$= 81\ \text{mW} + 247\ \text{mW} + (0.25)(45\ \text{mW})$$
$$= 340\ \text{mW}$$

RM4447 SPICE Subcircuit Listing

The SPICE subcircuit model given in Figure 4 simulates a typical device for dc bias characteristics including power dissipation, input currents, V_{OL} saturation point, and logic thresholds. The subcircuit also models response time.

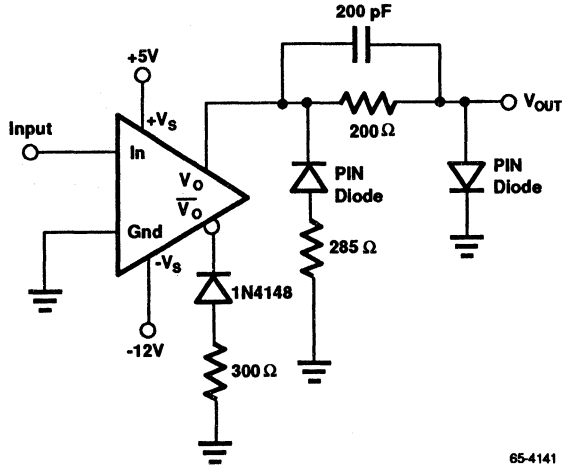
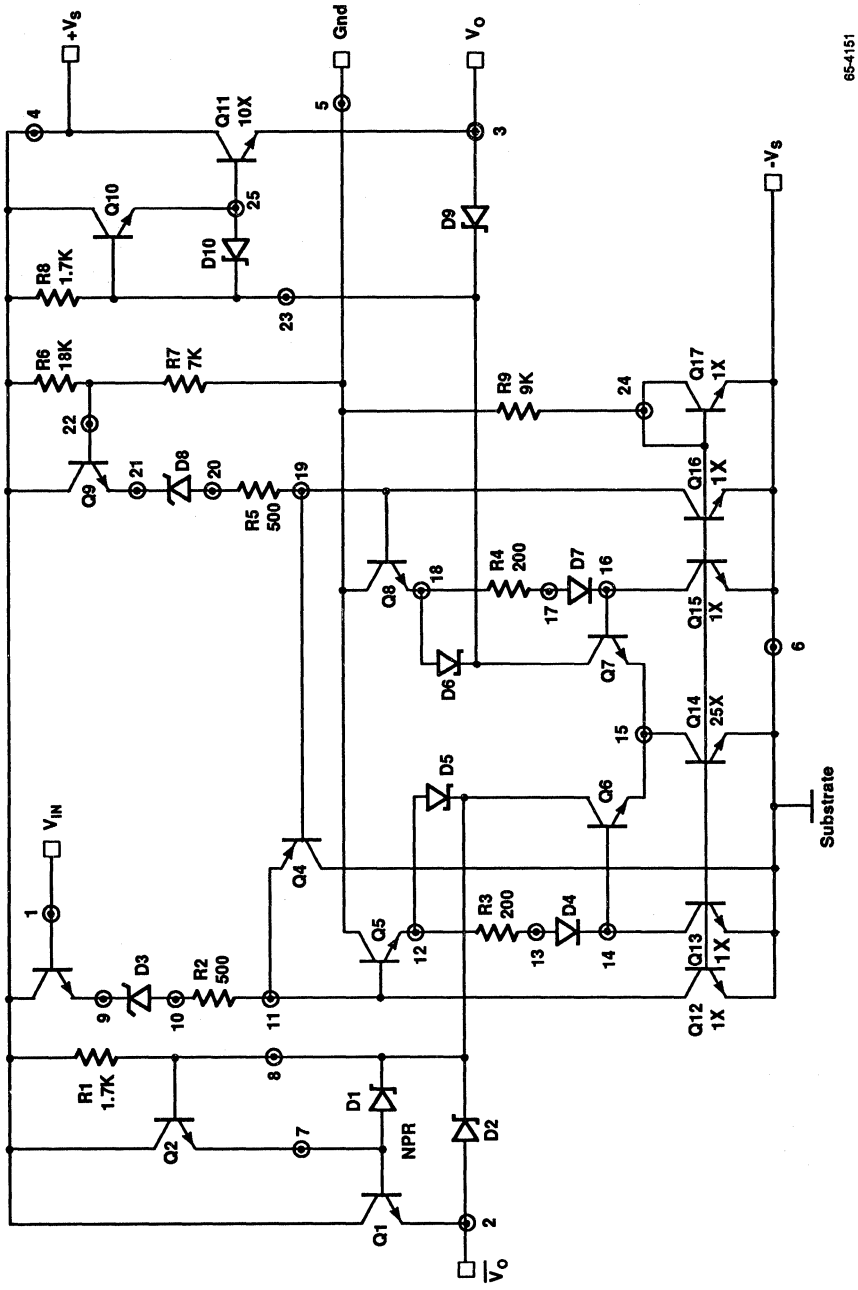


Figure 3. Single-Output Power Saver

```
*RM4447 TRANSIENT RESPONSE
.OPT LIST NODE RELTOL=.001
.WIDTH OUT=80
.TRAN 20NS 2US
.OP
.PRINT TRAN V(2)
.PROBE
XDUT 1 2 3 4 5 6 RM4447
V1 1 0 PULSE (2 0 100NS 1NS 1NS 500NS 1.5US)
VS+ 4 0 DC 5.0
VS- 0 6 DC 12.0
RL1 2 7 200
RL2 3 8 200
RL3 2 9 285
RL4 3 10 285
RGND 5 0 0.01
DA 7 0 DIODE
DB 8 0 DIODE
DC 0 9 DIODE
DD 0 10 DIODE
C1 2 7 200PF
C2 3 8 200PF
.SUBCKT RM4447 1 2 3 4 5 6
*
*          IN VO VO +VS GND -VS
Q1 4 7 2 6 QNPNL
Q2 4 8 7 6 QNPN
Q3 4 1 9 6 QNPN
Q4 6 19 11 6 QPNPV
Q5 5 11 12 6 QNPN
Q6 8 14 15 6 QNPN 5X
Q7 23 16 15 6 QNPN 5X
Q8 5 19 18 6 QNPN
Q9 4 22 21 6 QNPN
Q10 4 23 25 6 QNPN
Q11 4 25 3 6 QNPNL
Q12 11 24 6 6 QNPN
Q13 14 24 6 6 QNPN
Q14 15 24 6 6 QNPN 25X
Q15 16 24 6 6 QNPN
Q16 19 24 6 6 QNPN
Q17 24 24 6 6 QNPN
*
D1 7 8 SCHOT
D2 2 8 SCHOT 5X
D3 10 9 DIODE
D4 13 14 DIODE
D5 12 8 SCHOT
D6 18 23 SCHOT
D7 17 16 DIODE
D8 20 21 DIODE
D9 3 23 SCHOT 5X
D10 25 23 SCHOT
*
R1 4 8 1.7K
R2 10 11 500
R3 12 13 200
R4 18 17 200
R5 19 20 500
R6 4 22 18K
R7 22 5 7K
R8 4 23 1.7K
R9 5 24 9.0K
.ENDS
.MODEL QNPN NPN IS=1.5FA BF=150
+VAF=80 ISC=0 RB=200 RE=2 RC=75
+CJE=1.4PF CJC=1.3PF VJC=0.6
+MJC=0.5 XCJC=0.7 CJS=3.0PF
+VJS=0.58 MJS=0.5 TF=0.18NS
.MODEL QNPNL NPN IS=30FA BF=150
+VAF=80 ISC=2NA RB=75 RE=1 RC=30
+CJE=26.0PF CJC=11PF VJC=0.6
+MJC=0.5 XCJC=0.7 CJS=9PF
+VJS=0.58 MJS=0.5 TF=0.25NS
.MODEL QPNPV PNP IS=9.04E-16 BF=76
+NF=1.0 VAF=108 IKF=1.6E-4
+ISE=3.2E-15 IKR=8E-4 ISC=1.8E-14
+NE=1.37 BR=.137 NR=1 VAR=33.8
+RB=500 IRB=1.0E-3 RBM=500 RE=37.9
+NC=1.02 CJE=0.56PF VJE=0.4
+MJE=0.22 TF=8.0NS TR=9.5E-8
+CJC=5.2E-12 VJC=0.4 MJC=0.13
+RC=68
.MODEL DIODE D IS=9.4E-16 RS=2
+N=1.0 TT=1.0NS CJO=0.8PF
+VJ=0.7 EG=1.11 BV=6.8
.MODEL SCHOT D IS=20PA RS=50
*
.END
```

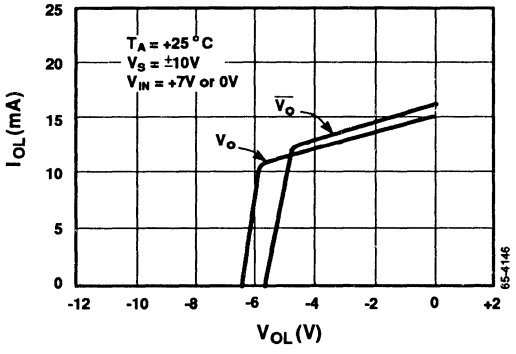
Figure 4. SPICE Subcircuit Model

RM4447 SPICE Subcircuit Node Schematic Diagram

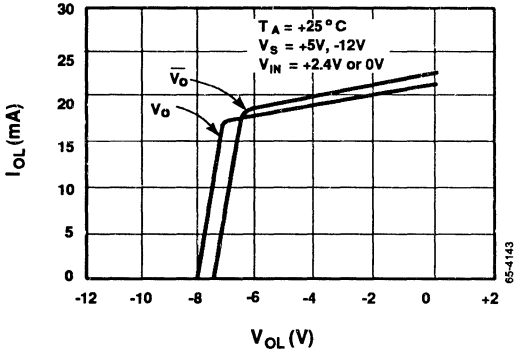


Typical Performance Characteristics

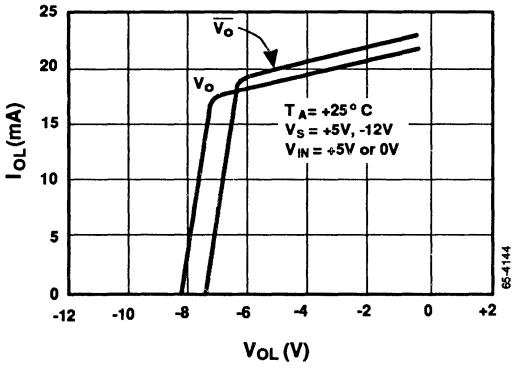
I_{OUT} Low vs. V_{OUT} Low



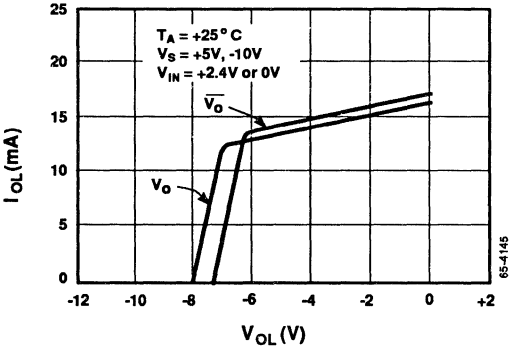
I_{OUT} Low vs. V_{OUT} Low



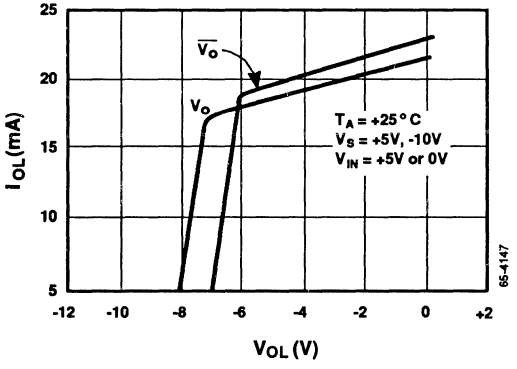
I_{OUT} Low vs. V_{OUT} Low



I_{OUT} Low vs. V_{OUT} Low

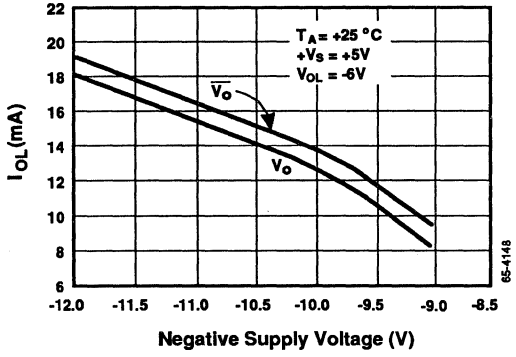


I_{OUT} Low vs. V_{OUT} Low

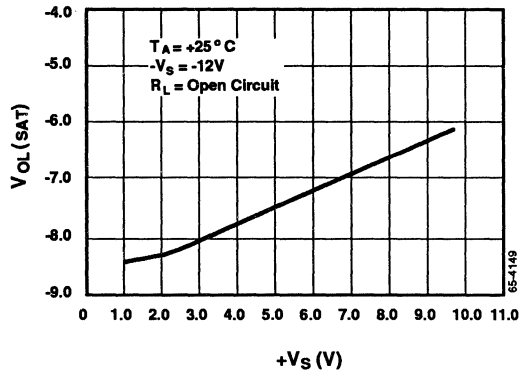


Typical Performance Characteristics (Continued)

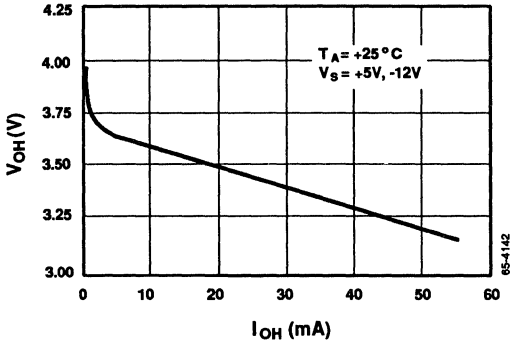
Output Sink Current vs. $-V_S$



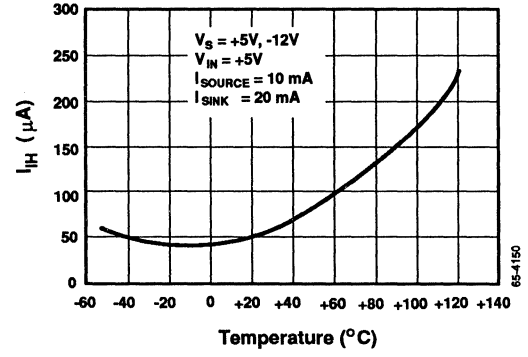
$V_{OL(SAT)}$ vs. Positive Supply Voltage



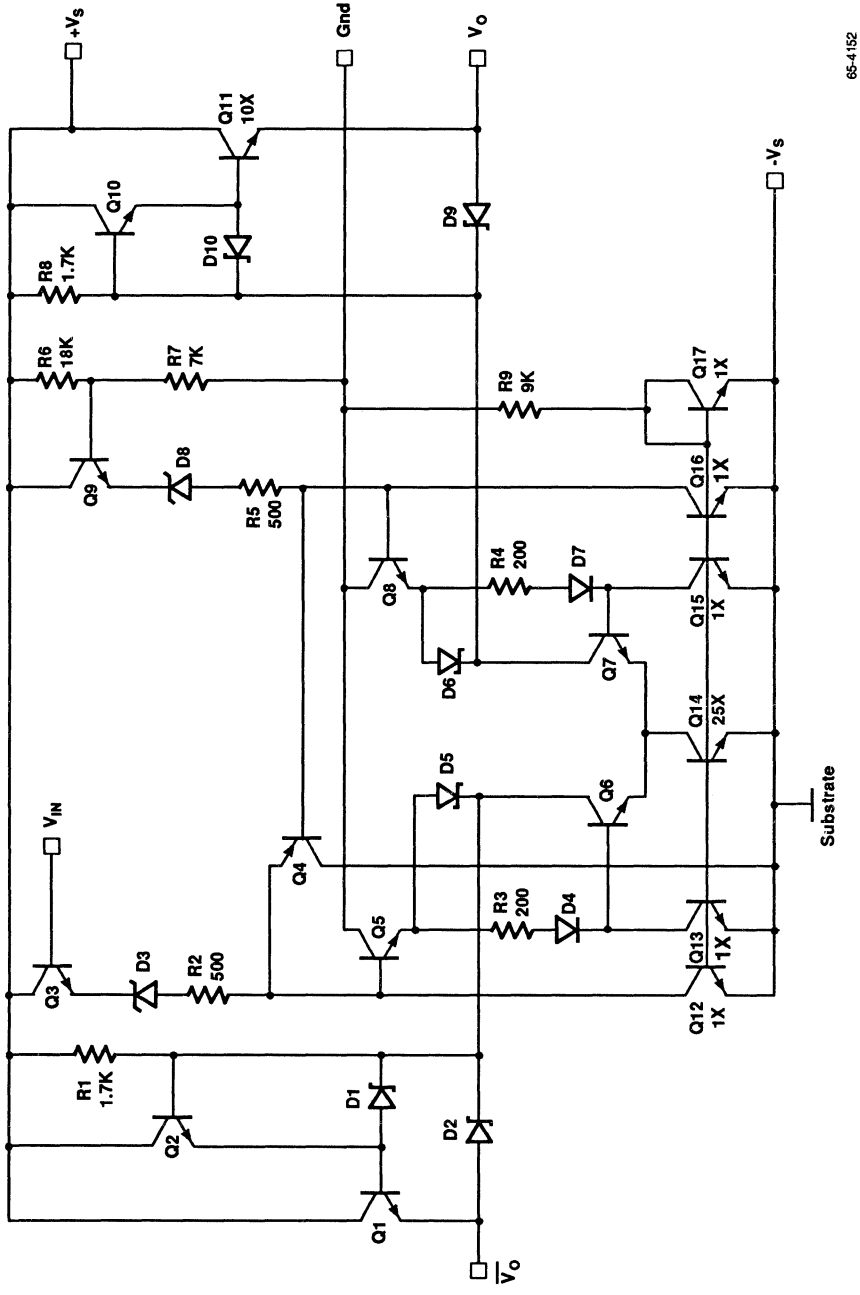
V_{OUT} High vs. Output Source Current



Input Current High vs. Temperature



RM4447 Internal Schematic Diagram



XR-2207 Voltage-Controlled Oscillator

Features

- Excellent temperature stability — 20ppm/°C
- Linear frequency sweep
- Adjustable duty cycle — 0.1% to 99.9%
- Two or four level FSK capability
- Wide sweep range — 1000:1 min
- Logic compatible input and output levels
- Wide supply voltage range — ±4V to ±13V
- Low supply sensitivity — 0.15%/V
- Wide frequency range — 0.01Hz to 1MHz
- Simultaneous triangle and squarewave outputs

Applications

- FSK generation
- Voltage and current-to-frequency conversion
- Stable phase-locked loop
- Waveform generation triangle, sawtooth, pulse, squarewave
- FM and sweep generation

Description

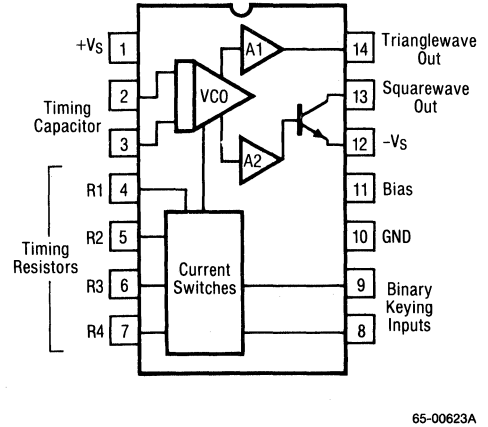
The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01Hz to 1MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

As shown in the Schematic Diagram, the circuit is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The XR-2207 has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

Connection Information

14-Lead
Dual In-Line Package
(Top View)



65-00623A

Ordering Information

Part Number	Package	Operating Temperature Range
XR2207CN	N	0°C to +70°C
XR2207N	N	-25°C to +85°C
XR2207MD	D	-55°C to +125°C
XR2207MD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

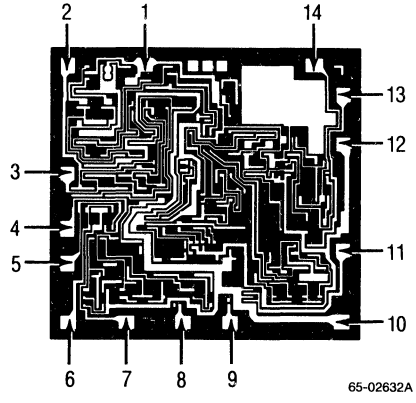
Thermal Characteristics

	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D $T_A < 50°C$	468mW	1042mW
Therm. Res. θ_{JC}	—	60°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For $T_A > 50°C$ Derate at	6.25mW per °C	8.33mW per °C

Absolute Maximum Ratings

Supply Voltage ..... +26V
Storage Temperature Range ..... -65°C to +150°C

Mask Pattern



Die Size: 85 x 80 mils
Min. Pad Dimensions: 4 x 4 mils

Electrical Characteristics

(Test Circuit of Figure 1, $V_S = \pm 6V$, $T_A = +25°C$ = 5000pF, R1 = R2 = R3 = R4 = 20kΩ, R_L = 4.7kΩ, Binary inputs grounded, S1 and S2 closed unless otherwise specified)

Parameters	Test Conditions	XR-2207 Min	XR-2207 Typ	XR-2207 Max	XR-2207C Min	XR-2207C Typ	XR-2207C Max	Units
General Characteristics								
Supply Voltage Single Supply Split Supplies	See Typical Performance Characteristics	 +8.0 ±4	 +12 ±6	 +26 ±13	 +8.0 ±4	 +12 ±6	 +26 ±13	V
Supply Current Single Supply	Measured at pin 1, S1 open (See Fig. 2)		5.0	7.0		5.0	8.0	mA
Split Supplies Positive	Measured at pin 1, S1 open (See Fig. 1)		5.0	7.0		5.0	8.0	
Negative	Measured at pin 12, S1, S2 open		4.0	6.0		4.0	7.0	
Binary Keying Inputs								
Switching Threshold	Measured at pins 8 and 9. Refer to pin 10	1.4	2.2	2.8	1.4	2.2	2.8	V
Input Resistance			5.0			5.0		kΩ

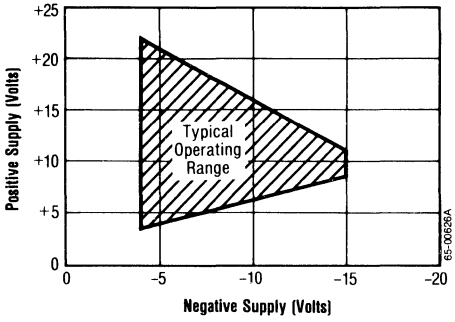
Electrical Characteristics (Continued)

Parameters	Test Conditions	XR-2207			XR-2207C			Units
		Min	Typ	Max	Min	Typ	Max	
Oscillator Section — Frequency Characteristics								
Upper Frequency Limit	C = 500pF, R3 = 2kΩ	0.5	1.0		0.5	1.0		MHz
Lower Practical Frequency	C = 50μF, R3 = 2Ω		0.01			0.01		Hz
Frequency Accuracy			±1.0	±3.0		±1.0	±5.0	% of f_0
Frequency Matching			0.5			0.5		% of f_0
Frequency Stability Vs. Temperature (Note 1)	0°C < T_A < +75°C		20	50		30		ppm/°C
Vs. Supply Voltage			0.15			0.15		%/V
Sweep Range	R3 = 1.5kΩ for f_H R3 = 2MΩ for f_L	1000:1	3000:1			1000:1		f_H/f_L
Sweep Linearity 10:1 Sweep	C = 5000pF f_H = 10kHz, f_L = 1kHz		1.0	2.0		1.5		%
1000:1 Sweep	f_H = 100kHz, f_L = 100Hz		5.0			5.0		%
FM Distortion	±10% FM Deviation		0.1			0.1		%
Recommended Range of Timing Resistors	See Characteristic Curves	1.5		2000	1.5		2000	kΩ
Impedance at Timing Pins	Measured at pins 4, 5, 6 or 7		75			75		Ω
DC Level at Timing Terminals			10			10		mV
Output Characteristics								
Triangle Output Amplitude	Measured at pin 14	4	6		4	6		V_{p-p}
Impedance			10			10		Ω
DC Level	Referenced to pin 10 from 10% to 90% of swing		+100			+100		mV
Linearity			0.1			0.1		%
Squarewave Output Amplitude	Measured at pin 13, S2 Closed	11	12		11	12		V_{p-p}
Saturation Voltage	Referenced to pin 12		0.2	0.4		0.2	0.4	V
Rise Time	$C_L \leq$ 10pF		200			200		nS
Fall Time	$C_L \leq$ 10pF		20			20		nS

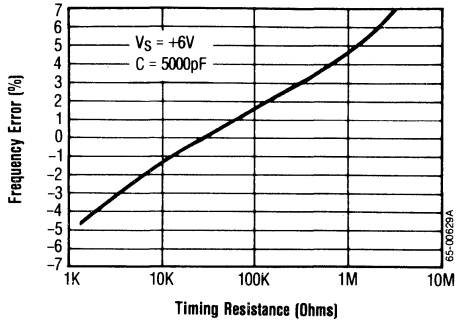
Note: 1. Guaranteed by design

Typical Performance Characteristics

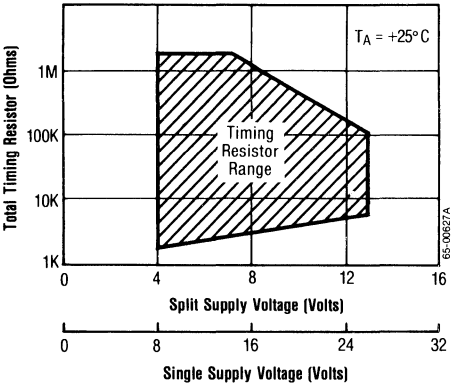
Typical Operating Range for Split Supply Voltage



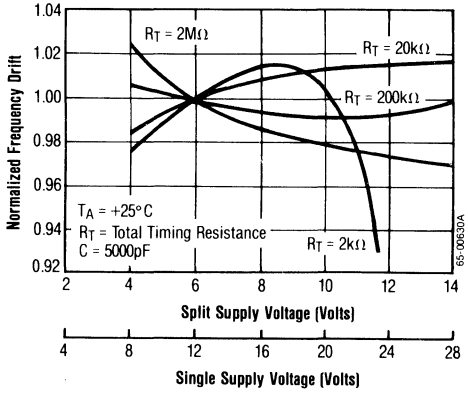
Frequency Accuracy vs. Timing Resistance



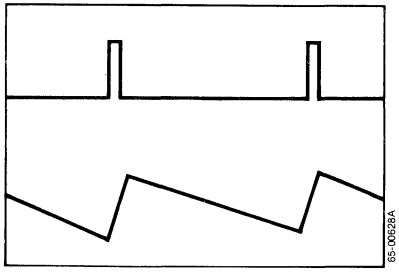
Recommended Timing Resistor Value vs. Power Supply Voltage*



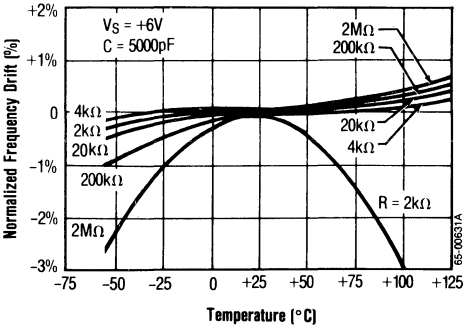
Frequency Drift vs. Supply Voltage



Pulse and Sawtooth Outputs



Normalized Frequency Drift With Temperature



* RT = Parallel Combination of Activated Timing Resistors

Description of Circuit Controls

Timing Capacitor (pins 2 and 3)
The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100pF to 100μF. The capacitor should be non-polarized.

Timing Resistors (pins 4, 5, 6, and 7)
The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 1.5kΩ to 2MΩ; however, for optimum temperature and power supply stability, recommended values are 4kΩ to 200kΩ. To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noisy environments, unused or deactivated timing terminals should be bypassed to ground through 0.1μF capacitors. Otherwise, they may be left open.

Supply Voltage (pins 1 and 12)
The XR-2207 is designed to operate over a power supply range of $\pm$4V to $\pm$13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced. Performance is optimum for $\pm$6V, or 12V single supply operation.

Binary Keying Inputs (pins 8 and 9)
The internal impedance at these pins is approximately 5kΩ. Keying levels are <1.4V for "zero" and >3V for "one" logic levels referenced to the DC voltage at pin 10.

Bias for Single Supply (pin 11)
For single supply operations, pin 11 should be externally biased to a potential between $+V_S/3V$ and $+V_S/2V$ (see Figure 1). The bias current as pin 11 is nominally 5% of the total oscillation timing current I_T.

Ground (pin 10)
For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be AC grounded through a 1μF bypass capacitor. During split supply operation, a ground current of 2 I_T flows out of this terminal, where I_T is the total timing current.

Squarewave Output (pin 13)
The squarewave output at pin 13 is an "open-collector" stage capable of sinking up to 20mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1kΩ to 10kΩ.

Triangle Output (pin 14)
The output at pin 14 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10Ω and is internally protected against short circuits.

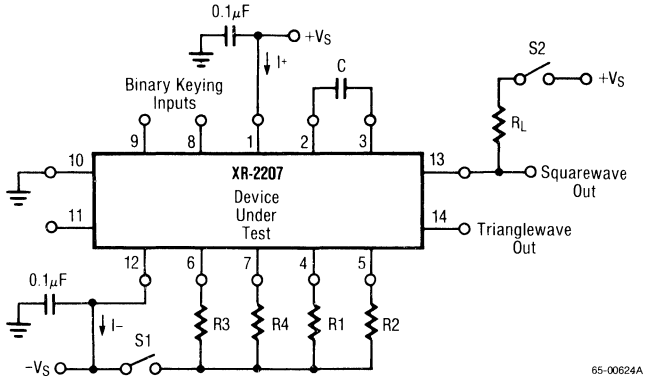
Note: Triangle waveform linearity is sensitive to parasitic coupling between the square and the triangle-wave outputs (pins 13 and 14). In board layout or circuit wiring care should be taken to minimize stray wiring capacitance between these pins.

Operating Instructions

Precautions
The following precautions should be observed when operating the XR-2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the total current drawn from pins 4, 5, 6, and 7 be limited to <6mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10mA.
2. Terminals 2, 3, 4, 5, 6, and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. The keying logic pulse amplitude should not exceed the supply voltage.

Split Supply Operation
Figure 1 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R1 through R4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in Table 1. If a single timing resistor is activated, the frequency is 1/RC.



Note: This circuit is for Bench Tests only. DC testing is normally performed with automated test equipment using an equivalent circuit.

Figure 1. Test Circuit for Split Supply Operation

Table 1. Logic Table for Binary Keying Controls

Logic Level 8	Logic Level 9	Selected Timing Pins	Frequency	Definitions
0	0	6	f_1	$f_1 = 1/R3C$, $\Delta f_1 = 1/R4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R2C$, $\Delta f_2 = 1/R1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	Logic Levels: 1 = >3V

Note: For single-supply operation, logic levels are referenced to voltage at pin 10.

Otherwise, the frequency is either 1/(R1||R2)C or 1/(R1||R4)C.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5kΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $+V_S/2$.

The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6V supplies.

Single Supply Operation
The circuit should be interconnected as shown in Figure 2 for single supply operation. Pin 12 should be grounded, and pin 11 biased from $+V_S$ through a resistive divider to a value of bias voltage between $+V_S/3$ and $+V_S/2$. Pin 10 is bypassed to ground through a 0.1μF capacitor.

For single supply operation, the DC voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

On-Off Keying
The XR-2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1Hz) residual oscillation in the "off" state due to internal bias current. If this effect is undesirable, it can be eliminated by connecting a 10MΩ resistor from 3 to $+V_S$.

Frequency Control (Sweep and FM)
The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figure 3.

For split supply operation, a *negative* control voltage, V_C, applied to the circuit of Figure 3 causes the total timing current, I_T, and the frequency, to increase.

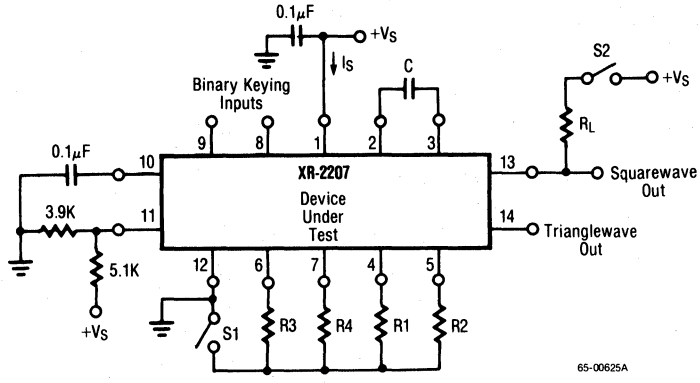


Figure 2. Test Circuit for Single Supply Operation

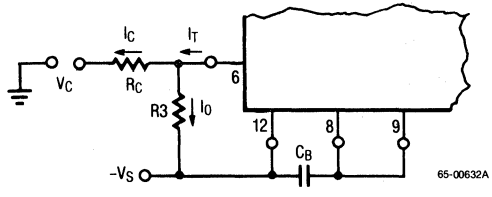


Figure 3. Frequency Sweep Operation

As an example, in the circuit of Figure 3, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation is determined by:

$$f = \frac{1}{R3C_B}\left[1 - \frac{V_C R3}{(R_C)(-V_S)}\right] Hz$$

Pulse and Sawtooth Operation

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the square-wave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

Figure 4 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0,0" and the "1,0" logic states given in Table 1. Timing pin 5 is activated when the output is "high", and pin 6 is activated when the square-wave output goes to a "low" state.

The duty cycle of the output waveforms is given as:

$$\text{Duty Cycle} = \frac{R2}{R2 + R3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R2 + R3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R2 and R3 to a common control voltage V_C instead of to $-V_S$. The sawtooth and the pulse output waveforms are shown in the Typical Performance Characteristics Graphs.

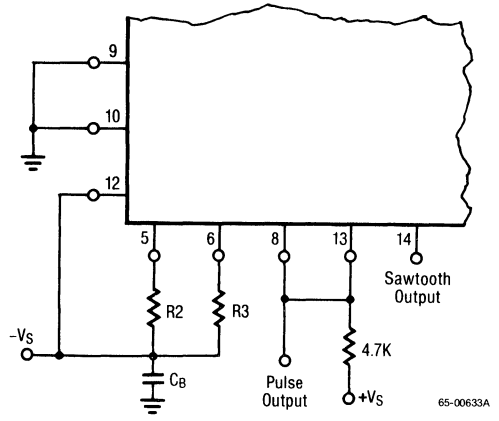
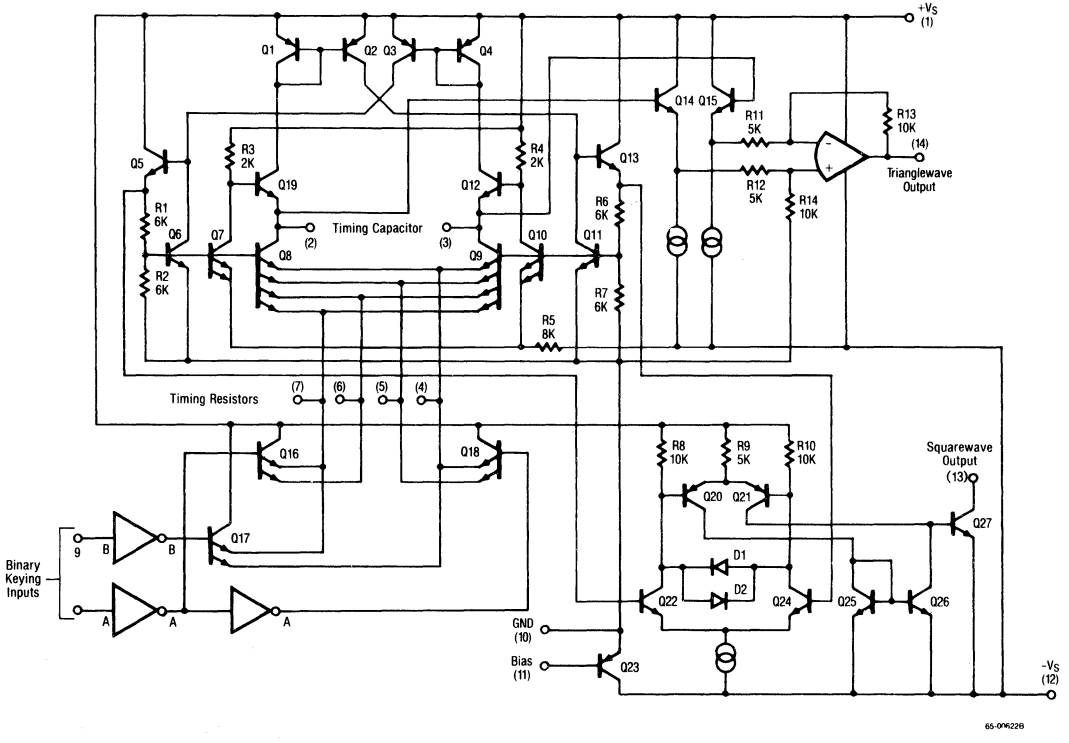


Figure 4. Pulse and Sawtooth Generation

Schematic Diagram



XR-2211 FSK Demodulator/ Tone Decoder

Features

- Wide frequency range — 0.01 Hz to 300 kHz
- Wide supply voltage range — 4.5V to 20V
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range — 2 mV to 3 V_{RMS}
- Adjustable tracking range — ±1% to ±80%
- Excellent temperature stability — 20 ppm/°C typical

Applications

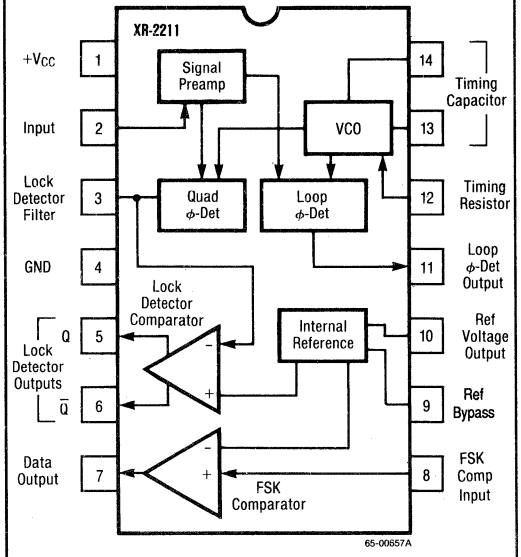
- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

Description

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications, and operates over a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.

Connection Information

14-Lead
Dual In-Line Package
(Top View)



Absolute Maximum Ratings

Supply Voltage ..... +20V
Input Signal Level ..... 3 V_{RMS}
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
XR2211MD ..... -55°C to +125°C
XR2211N ..... -25°C to +85°C
XR2211CN ..... 0°C to +70°C
Lead Soldering Temperature
(60 sec) ..... +300°C

Ordering Information

Part Number	Package	Operating Temperature Range
XR2211CN	N	0°C to +70°C
XR2211N	N	-25°C to +85°C
XR2211MD	D	-55°C to +125°C
XR2211MD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 14-lead plastic DIP
D = 14-lead ceramic DIP
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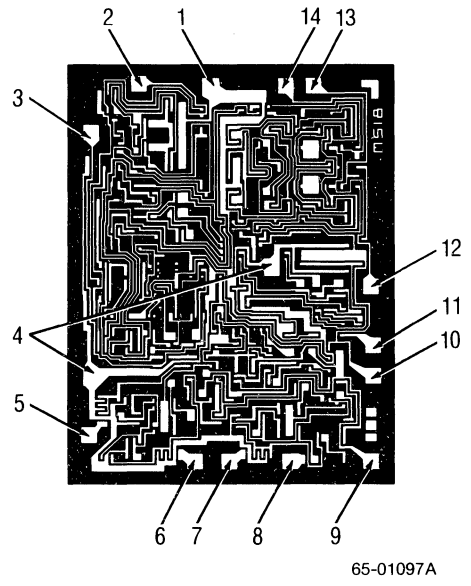
Thermal Characteristics

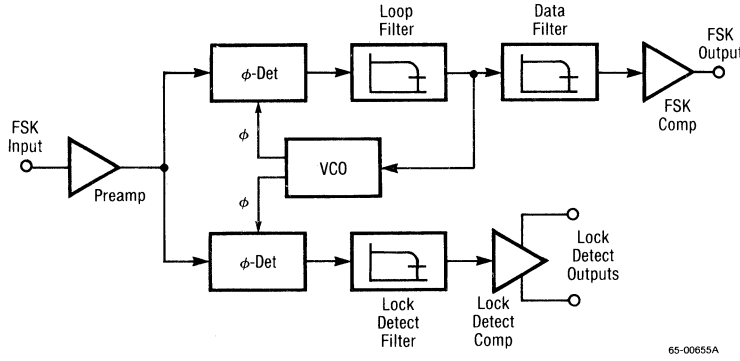
	14-Lead Plastic DIP	14-Lead Ceramic DIP
Max. Junction Temp.	125°C	175°C
Max. P_D T_A <50°C	468 mW	1042 mW
Therm. Res θ_{JC}	—	50°C/W
Therm. Res. θ_{JA}	160°C/W	120°C/W
For T_A >50°C Derate at	6.25 mW per °C	8.33 mw per °C

Mask Pattern



Die Size: 103 x 80 mils
Min. Pad Dimensions: 4 x 4 mils

Functional Block Diagram



Electrical Characteristics (Test Conditions $+V_S$ = +12V, T_A = +25°C, R0 = 30kΩ, C0 = 0.033μF. See Figure 1 for component designations.)

Parameters	Test Conditions	XR-2211/M			XR-2211C			Units
		Min	Typ	Max	Min	Typ	Max	
General								
Supply Voltage		4.5		20	4.5		20	V
Supply Current	R0 ≥ 10kΩ		4.0	9.0		5.0	11	mA
Oscillator								
Frequency Accuracy	Deviation from $f_0 = 1/R0C0$		±1.0	±3.0		±1.0		%
Frequency Stability[1] Temperature Coefficient	R1 = ∞		±20	±50		±20		ppm/°C
Power Supply Rejection	$+V_S$ = 12 ±1V		0.05	0.5		0.05		%/V
	$+V_S$ = 5 ±0.5V		0.2			0.2		%/V
Upper Frequency Limit	R0 = 8.2kΩ, C0 = 400pF	100	300			300		kHz
Lowest Practical Operating Frequency[1]	R0 = 2MΩ C0 = 50μF			0.01		0.01		Hz
Timing Resistor, R0 Operating Range		5.0		2000	5.0		2000	kΩ
Recommended Range		15		100	15		100	kΩ

Note: 1. Guaranteed by design.

Electrical Characteristics (Continued)

(V_S = +12V, T_A = +25° C, R0 = 30kΩ, C0 = 0.033μF. See Figure 1 for component designations.)

Parameters	Test Conditions	XR-2211/M			XR-2211C			Units
		Min	Typ	Max	Min	Typ	Max	
Loop Phase Detector								
Peak Output Current	Meas. at Pin 11	±150	±200	±300	±100	±200	±300	μA
Output Offset Current			±1.0			±2.0		μA
Output Impedance			1.0			1.0		MΩ
Maximum Swing	Ref. to Pin 10	±4.0	±5.0		±4.0	±5.0		V
Quadrature Phase Detector								
Peak Output Current[2]	Meas. at Pin 3	100	150			150		μA
Output Impedance			1.0			1.0		MΩ
Maximum Swing			11			11		V_{p-p}
Input Preamp								
Input Impedance	Meas. at Pin 2		20			20		kΩ
Input Signal Voltage Required to Cause Limiting[2]			2.0	10		2.0		mV_{RMS}
Voltage Comparator								
Input Impedance	Meas. at Pins 3 & 8		2.0			2.0		MΩ
Input Bias Current			100			100		nA
Voltage Gain[1]	R_L = 5.1kΩ	55	70		55	70		dB
Output Voltage Low	I_C = 3mA		300			300		mV
Output Leakage Current	V_O = 12V		0.01			0.01		μA
Internal Reference								
Voltage Level	Meas. at Pin 10	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		Ω

Notes:
1. Guaranteed by design.
2. Sample tested.

Description of Circuit Controls

Signal Input (Pin 2)
The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20 kΩ. Recommended input signal level is in the range of 10 mV_{RMS} to 3 V_{RMS}.

Quadrature Phase Detector Output (Pin 3)
This is the high-impedance output of the quadrature phase detector, and is internally connected to the input of lock-detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.

Lock-Detect Output, Q (Pin 5)
The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting stage when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to $+V_S$ for proper operation. In the "low " state it can sink up to 5 mA of load current.

Lock-Detect Complement, $\overline{Q}$ (Pin 6)
The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open collector type stage which can sink 5 mA of load current in the low or "on" state.

FSK Data Output (Pin 7)
This output is an open collector logic stage which requires a pull-up resistor, R_L, to $+V_S$ for proper operation. It can sink 5 mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK Comparator Input (Pin 8)
This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

Reference Bypass (Pin 9)
This pin can have an optional 0.1 µF capacitor connected to the ground.

Reference Voltage, VR (Pin 10)
This pin is internally biased at the reference voltage level, V_R; V_R = V+/2 - 650 mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 µF capacitor.

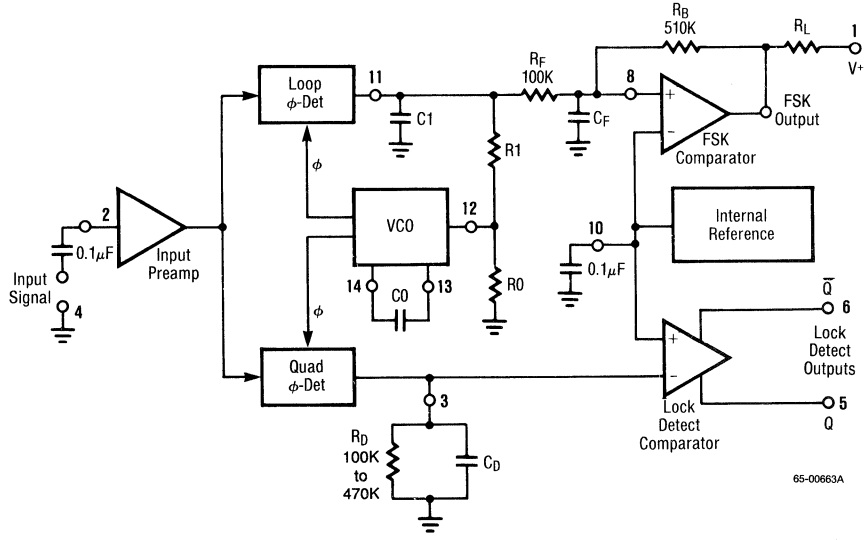


Figure 1. Generalized Circuit Connection for FSK and Tone Detection

Loop Phase Detector Output (Pin 11)
This terminal provides a high impedance output for the loop phase-detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO Control Input (Pin 12)
VCO free-running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free-running frequency, f_0, is given by:

$$f_0(\text{Hz}) = \frac{1}{R0C0}$$

where C0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R0 must be in the range of 10kΩ to 100kΩ (see Typical Electrical Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≤3mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14)
VCO frequency is inversely proportional to the external timing capacitor, C0, connected across these terminals. C0 must be non-polarized, and in the range of 200pF to 10μF.

VCO Frequency Adjustment
VCO can be fine tuned by connecting a potentiometer, R_X, in series with R0 at pin 12 (see Figure 2).

VCO Free-Running Frequency, f_0
The XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for setup or adjustment purposes, the VCO free-running frequency can be measured at pin 3 (with C_D disconnected) with no input and with pin 2 shorted to pin 10.

Design Equations

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, f_0:

$$f_0(\text{Hz}) = \frac{1}{R0C0}$$

2. Internal Reference Voltage, V_R (measured at pin 10):

$$V_R = \left(\frac{+V_S}{2}\right) - 650\text{mV}$$

3. Loop Lowpass Filter Time Constant, τ:

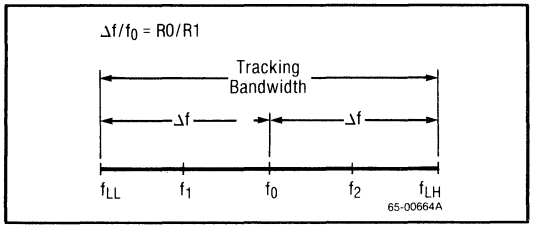
$$\tau = R1C1$$

4. Loop Damping, ζ:

$$\zeta = \left(\sqrt{\frac{C0}{C1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

$$\Delta f/f_0 = R0/R1$$



6. FSK Data Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$K\phi \text{ (in volts per radian)} = \frac{(-2)(V_R)}{\pi}$$

8. VCO Conversion Gain, K0, is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0 \text{ (in Hertz per volt)} = \frac{-1}{C0R1V_R}$$

9. Total Loop Gain, K_T:

$$K_T \text{ (in radians per second per volt)} = 2\pi K\phi K0 = 4/C0R1$$

10. Peak Phase-Detector Current, I_A:

$$I_A \text{ (mA)} = \frac{V_R}{25}$$

Applications

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R0 and C0 set the PLL center frequency, R1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (= 510kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

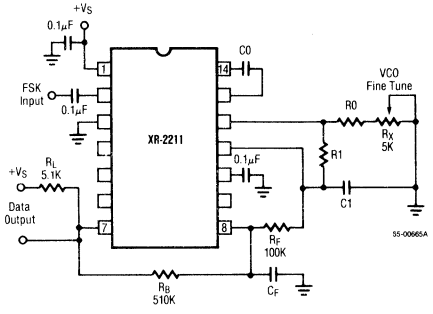


Figure 2. Circuit Connection for FSK Decoding

Table 1. Recommended Component Values for Commonly Used FSK Bands
(See Circuit of Figure 2)

FSK Band	Component Values
300 Baud	C0 = 0.039μF C_F = 0.005μF
f_1 = 1070Hz	C1 = 0.01μF R0 = 18kΩ
f_2 = 1270Hz	R1 = 100kΩ
300 Baud	C0 = 0.022μF C_F = 0.005μF
f_1 = 2025Hz	C1 = 0.0047μF R1 = 18kΩ
f_2 = 2225Hz	R1 = 200kΩ
1200 Baud	C0 = 0.027μF C_F = 0.0022μF
f_1 = 1200Hz	C1 = 0.01μF R0 = 18kΩ
f_2 = 2200Hz	R1 = 30kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components; R0, R1, C0, C1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, f_0

$$f_0 = \frac{f_1 + f_2}{2}$$

2. Choose a value of timing resistor R0 to be in the range of 10kΩ to 100kΩ. This choice is arbitrary. The recommended value is R0 ≅ 20kΩ. The final value of R0 is normally fine-tuned with the series potentiometer, R_X.

3. Calculate value of C0 from Design Equation No. 1 or from Typical Performance Characteristics:

$$C0 = 1/R0f_0$$

4. Calculate R1 to give a Δf equal to the mark-space deviation:

$$R1 = R0\,[f_0/(f_1 - f_2)]$$

5. Calculate C1 to set loop damping. (See Design Equation No. 4.)
   Normally, $\zeta \approx 1/2$ is recommended
   Then: C1 = C0/4 for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, C_F:
   For R_F = 100kΩ, R_B = 510kΩ, the recommended value of C_F is:

$$C_F\ (\text{in } \mu F) = \frac{3}{\text{Baud Rate}}$$

Note: All calculated component values except R0 can be rounded off to the nearest standard value, and R0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Baud FSK demodulator with mark/space frequencies of 1110/1170Hz:

Step 1: Calculate f_0:
f_0 = (1110 + 1170) (1/2) = 1140Hz

Step 2: Choose R0 = 20kΩ (18kΩ fixed resistor in series with 5kΩ potentiometer)

Step 3: Calculate C0 from V_{CO} Frequency vs. Timing Capacitor: C0 = 0.044μF

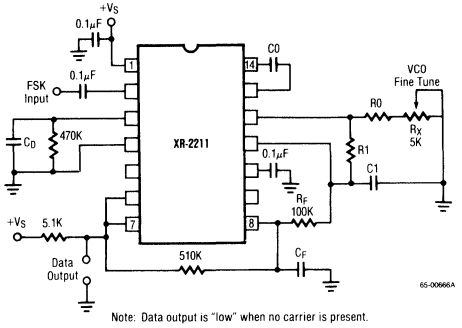
Step 4: Calculate R1: R1 = R0 (2240/60) = 380kΩ

Step 5: Calculate C1: C1 = C0/4 = 0.011μF

Note: All values except R0 can be rounded off to nearest standard value.

FSK Decoding With Carrier Detect

The lock-detect section of the XR-2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock-detect output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.



Note: Data output is "low" when no carrier is present.

Figure 3. External Connections for FSK Demodulation With Carrier Detect Capability

The minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C1. For most applications, $\Delta f_c < \Delta f/2$. For R_D = 470kΩ, the approximate minimum value of C_D can be determined by:

$$C_D(\mu F) \geq 16/\text{capture range in Hz}$$

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock-detect output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

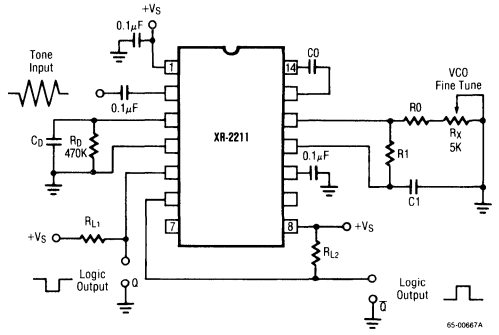


Figure 4. Circuit Connection for Tone Detection

With reference to Figures 1 and 4, the function of the external circuit components can be explained as follows: R0 and C0 set VCO center frequency, R1 sets the detection bandwidth, C1 sets the lowpass-loop filter time constant and the loop damping factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R0, R1, C0, C1, and C_D. For a given input tone frequency, f_S, these parameters are calculated as follows:

1. Choose R0 to be in the range of 15kΩ to 100kΩ. This choice is arbitrary.
2. Calculate C0 to set center frequency, f_0 equal to f_S: $C0 = 1/R0f_S$.
3. Calculate R1 to set bandwidth $\pm\Delta f$ (see Design Equation No. 5): $R1 = R0(f_0/\Delta f)$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

4. Calculate value of C1 for a given loop damping factor:

$$C1 = C0/16\zeta^2$$

Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving C1 = 0.25 C0.

Increasing C1 improves the out-of-band signal rejection, but increases the PLL capture time.

5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470kΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1kHz ±20Hz:

Step 1: Choose R0 = 20kΩ (18kΩ in series with 5kΩ potentiometer).

Step 2: Choose C0 for f_0 = 1kHz: C0 = 0.05μF.

Step 3: Calculate R1: R1 = (R0) (1000/20) = 1MΩ.

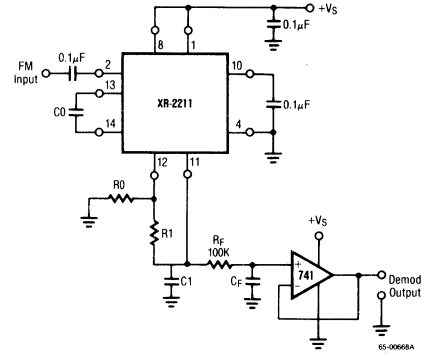
Step 4: Calculate C1: for ζ = 1/2, C1 = 0.25μF, C0 = 0.013μF.

Step 5: Calculate C_D: C_D = 16/38 = 0.42μF.

Step 6: Fine tune the center frequency with the 5kΩ potentiometer, R_X.

Linear FM Detection

The XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.



Note: See section on Design Equations for Component Values.

Figure 5. Linear FM Detector Using XR-2211 and an External Op Amp

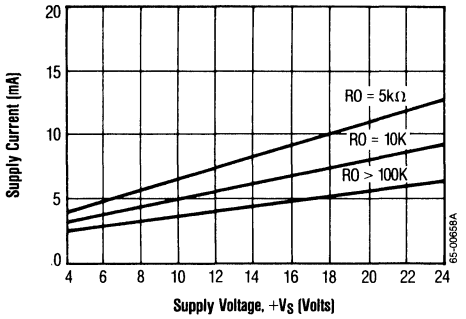
The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{OUT} = R1\ V_R/100\ R0 \text{ Volts/\% deviation}$$

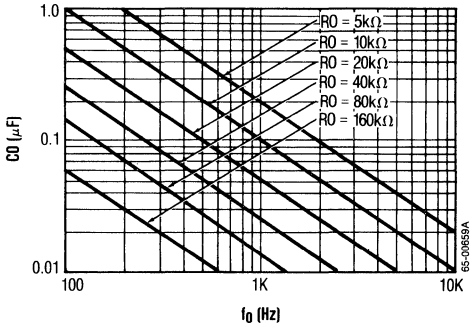
where V_R is the internal reference voltage. For the choice of external components R1, R0, C_D, C1 and C_F, see the section on Design Equations.

Typical Performance Characteristics

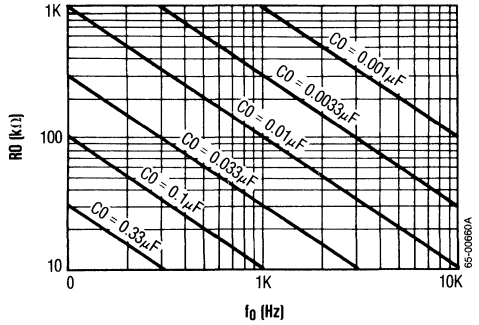
Typical Supply Current vs. $+V_S$ (Logic Outputs Open Circuited)



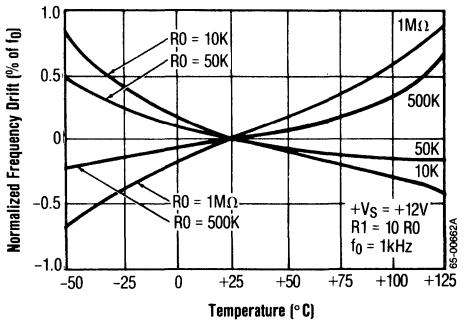
VCO Frequency vs. Timing Resistor



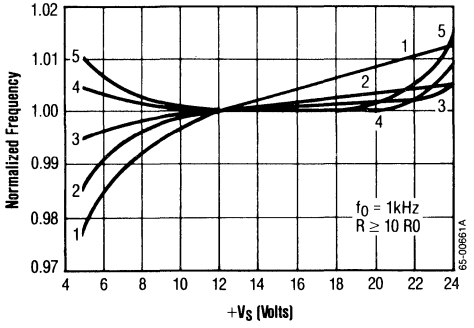
VCO Frequency vs. Timing Capacitor



Typical Center Frequency Drift vs. Temperature

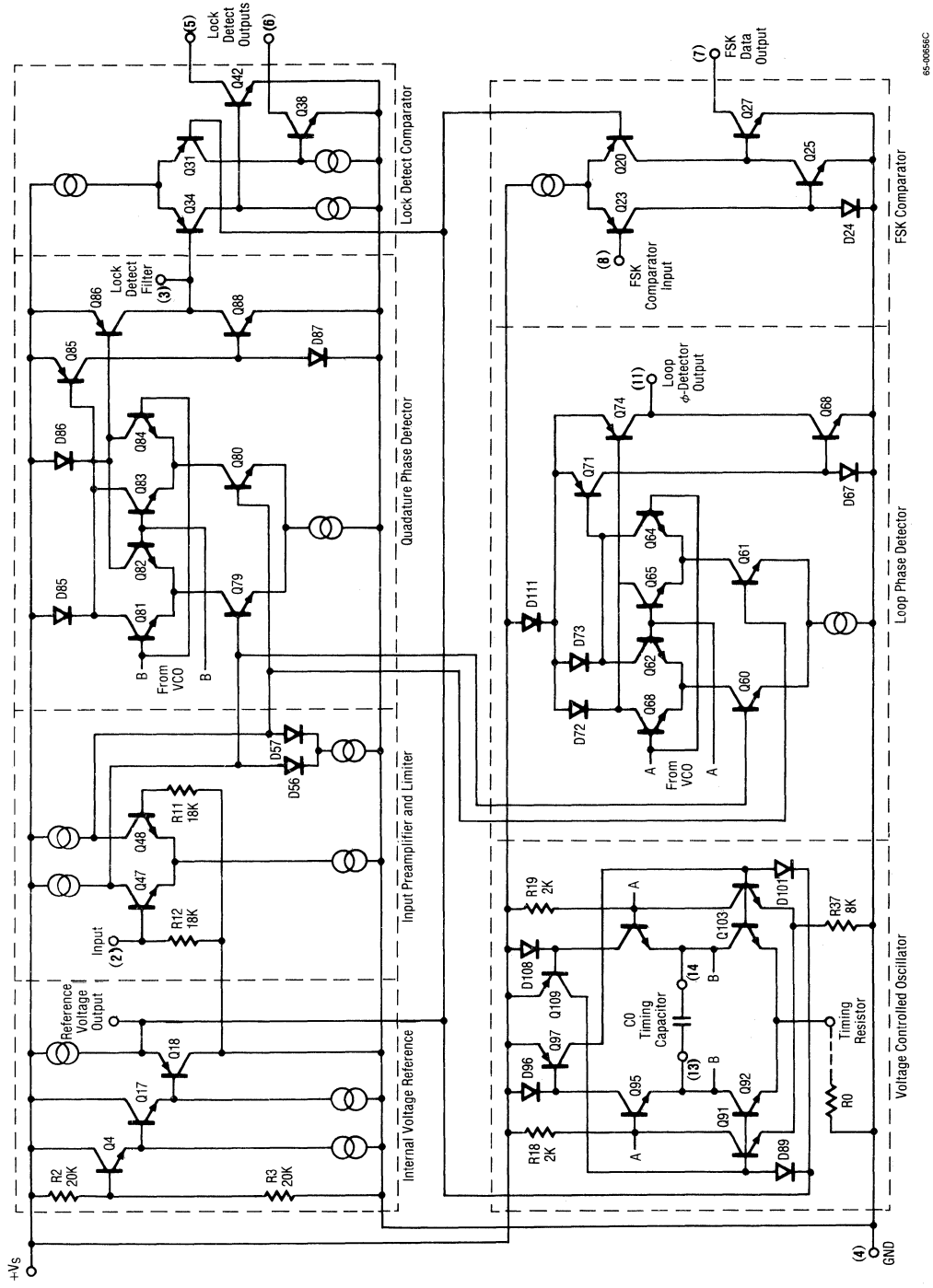


Typical f_0 vs. Power Supply Characteristics



Curve	RO
1	5K
2	10K
3	30K
4	100K
5	300K

Schematic Diagram



SECTION 12
ORDERING INFORMATION & PACKAGES

Raytheon Series **RM 4077 A L /883B**

Temperature Range
RM = Military -55°C to +125°C
RV = Industrial -25°C to +85°C*
RC = Commercial 0°C to +70°C

Basic Part Type
Four digits max

Electrical Grade
See data sheet

Package Type
See page 12-3 for
package codes

High Reliability Processing
(optional)

*Temperature range may be extended to -35°C or -40°C for specific device types.

LT-Series & DAC-Series

DAC - 6012 A M D /883B

Prefix: DAC = D/A Converter
LT = Industry Type (2nd source)

Basic Part Type
Four digits max

Electrical Grade
See data sheet

Temperature Range
M = Military -55°C to +125°C
C = Commercial 0°C to +70°C

Package Type
See data sheet for
package outline

High Reliability Processing
(optional)

LM Series

LM 101 A D /883B

Prefix: (2nd source)
LM = Industry Type

Basic Part Type and
Temperature Range
First digit denotes temperature range
1 = Military -55°C to +125°C
2 = Industrial -25°C to +85°C
3 = Commercial 0°C to +70°C

Electrical Grade
See data sheet

Package Type
See page 12-3 for
package codes

High Reliability Processing
(optional)

XR Series

XR - 2211 C P /883B

Prefix: (2nd source)
XR = Industry Type

Basic Part Type
Four digits max

Temperature Range
M = Military -55°C to +125°C
[ ] No designator =
Industrial -25°C to +85°C
C = Commercial 0°C to +70°C

Package Type
See below for
package codes

High Reliability Processing
(optional)

Branding Codes

RM4447D
RAY T 8850

Raytheon

Assembly
Plant
(see table)

Year (19XX)

Work Week
(1 to 52)

Package Codes

CH	Waffle-Packed Dice
D	Ceramic DIP
H	Metal Can (epoxy die attach)
K	9-Lead Metal Can Power Package
L	Ceramic Leadless Chip Carrier (LCC)
M	Small Outline Package (SOIC)
N	Plastic Dual In-Line Package (DIP)
S	Sidebraze Ceramic DIP
T	Metal Can (eutectic die attach)

Refer to the individual data sheet or to the Packaging Information for outline dimensions.

Approved Assembly Plants & Brand Codes

"O" M.V.
Raytheon Semiconductor, 490 E. Middlefield Road,
Mountain View, CA 94043

"T" TEPIC
ENSA Electronica Nayarit, S.A., Juan Escutia
No. 122 Tepic Nayarit, Mexico

"C" Epic/M
Epic Semiconductor Inc.
2100 Pasong Tamo Extension, Makati,
Metro Manile, Philippines

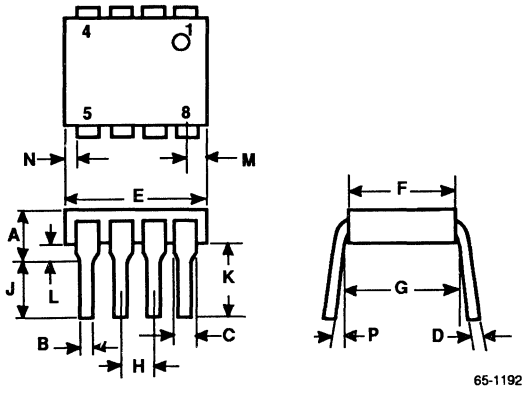
"L" NJRC
New Japan Radio (Saga Electronics Co., Ltd.)
950 Tateno Mitagawa-Machi
Kanzaki-Gun Saga Pref. Fakuoka, Japan

"P" SDPI
Semiconductor Devices Inc.
GMTFM Compound, Tagoig, Rizal
P.O. Box 7438
Air Mail Exchange Office, MIA, Philippines

"F" Talent Electronics Corp.
3rd Floor No. 2, Lane 49
Chung HSIAO E. Road Section 4
Taipei, Taiwan, R.O.C.

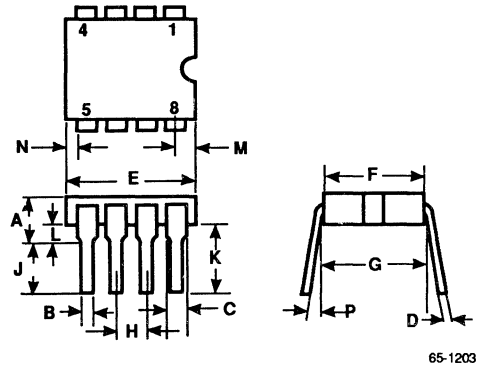
Packaging Information

8-Lead Plastic Dual In-Line Package



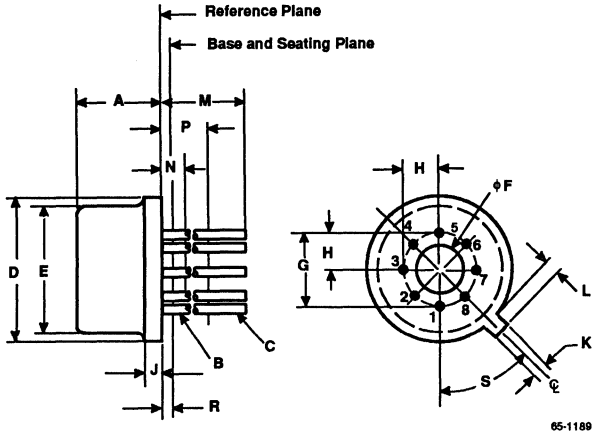
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.012	0.20	0.30
E	.330	.370	8.38	9.40
F	.240	.260	6.09	6.60
G	.290	.310	7.37	7.87
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	0.38	1.52
M		.055		1.35
N	.005		0.13	
P	0°	15°	0°	15°

8-Lead Ceramic Dual In-Line Package



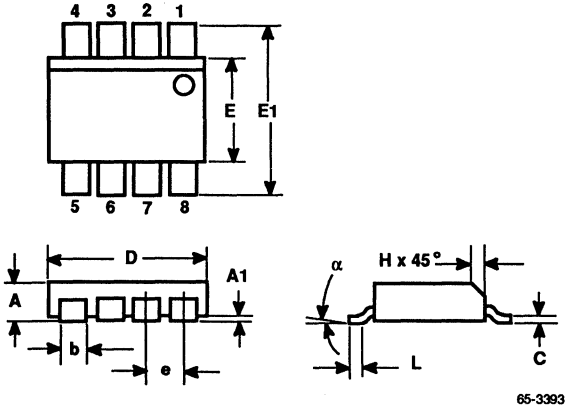
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
C	.050	.065	1.27	1.65
D	.008	.012	0.20	0.38
E	.372	.405	9.49	10.29
F	.240	.271	6.10	6.88
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	0.38	1.52
M		.055		1.35
N	.005		0.13	
P	0°	15°	0°	15°

8-Lead TO-99 Metal Can



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.165	.185	4.19	4.70
B	.016	.019	.41	.48
C	.016	.021	.41	.53
D	.335	.370	8.51	9.40
E	.305	.335	7.75	8.51
ϕF	.110	.160	2.79	4.06
G	.200 BSC		5.08 BSC	
H	.100 BSC		2.54 BSC	
J		.040		1.02
K	.027	.034	.69	.86
L	.027	.045	.69	1.14
M	.500	.750	12.70	19.05
N		.050		1.27
P	.250		6.35	
R	.010	.045	.25	1.14
S	45° BSC		45° BSC	

8-Lead Plastic Small Outline Dual In-Line Package

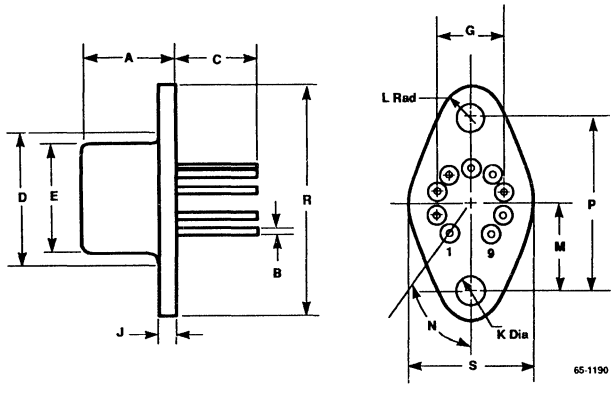


Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.053	.069	1.35	1.75
A1	.004	.008	.10	.20
b	.014	.018	.350	.450
C	.007	.009	.19	.22
D	.188	.197	4.80	5.00
E	.150	.158	3.80	4.00
e	.050 BSC		1.27BSC	
E1	.228	.244	5.80	6.20
L	.020	.045	.508	1.143
α	0°	8°	0°	8°
h	.01	.02	.25	.50

Note: C Dimension does not include Hot Solder Dip thickness.

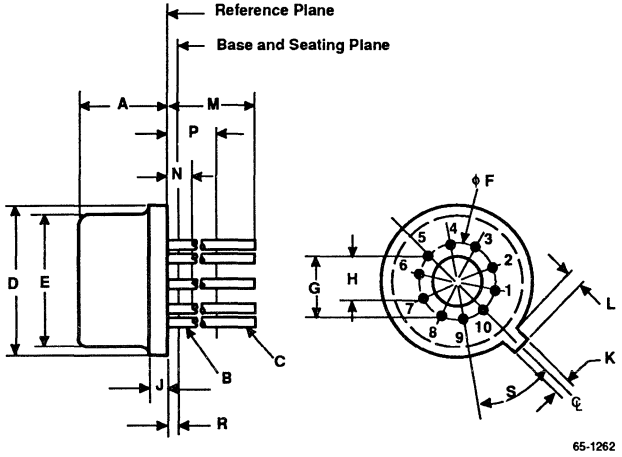
Dimensions conform to JEDEC specification MS-012-AA for SO packages.

9-Lead TO-66 Metal Can



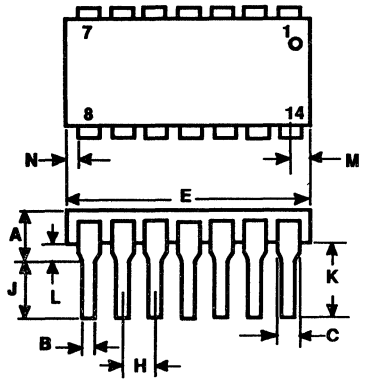
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.250	.340	6.35	8.63
B	.028	.034	.71	.863
C	.360		9.14	
D		.620		15.748
E	.300	.500	7.62	12.70
G	.325 BSC		5.84 BSC	
J	.050	.075	1.27	1.90
K	.142	.152	3.60	3.86
L		.145		3.68
M	.477	.483	12.11	12.26
N	36° Typ		36° Typ	
P	.958	.962	24.33	24.43
R		1.252		31.80
S		.700		17.80

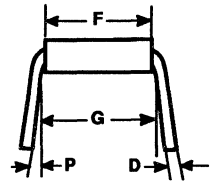
10-Lead TO-100 Metal Can



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.185	4.19	4.70
B	0.016	0.019	0.41	0.48
C	0.016	0.021	0.41	0.53
D	0.335	0.370	8.51	9.40
E	0.305	0.335	7.75	8.51
ϕF	0.110	0.160	2.79	4.06
G	0.230 BSC		5.84 BSC	
H	0.115 BSC		2.92 BSC	
J		0.040		1.02
K	0.028	0.034	0.69	0.86
L	0.029	0.045	0.69	1.14
M	0.500	0.750	12.70	19.05
N		0.050		1.27
P	0.250		6.35	
R	0.010	0.045	0.25	1.14
S	36° BSC		36° BSC	

14-Lead Plastic Dual In-Line Package

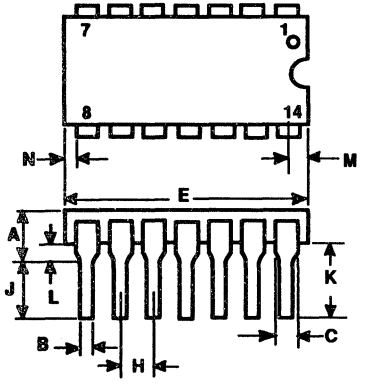


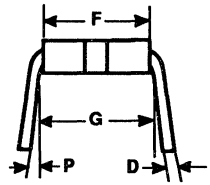


65-1194

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.012	0.20	0.30
E	.745	.755	18.92	19.18
F	.240	.260	6.10	6.60
G	.290	.310	7.37	7.87
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	0.38	1.52
M		.098		2.49
N	.005		0.13	
P	0°	15°	0°	15°

14-Lead Ceramic Dual In-Line Package

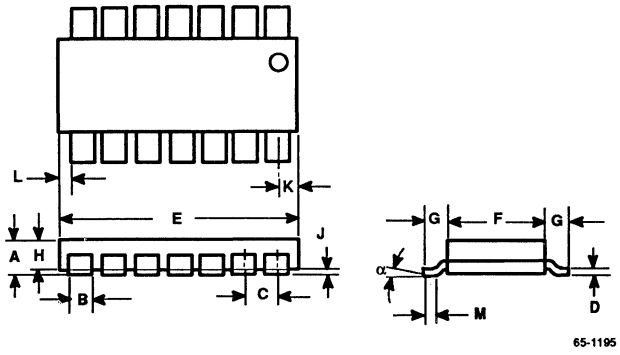




65-1204

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
C	.050	.065	1.27	1.65
D	.008	.012	0.20	0.30
E	.750	.785	19.05	19.94
F	.245	.271	6.22	6.88
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	0.38	1.52
M		.098		2.49
N	.005		0.13	
P	0°	15°	0°	15°

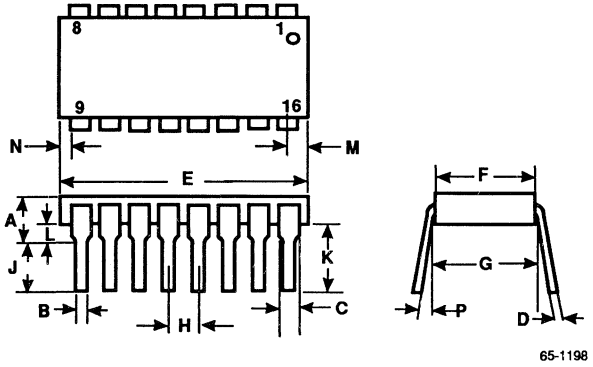
14-Lead Plastic Small Outline Dual In-Line Package



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.053	0.069	1.35	1.75
B	0.014	0.019	0.36	0.46
C	0.050 BSC		1.2 BSC	
D	0.0075	0.009	0.19	0.23
E	0.336	0.344	8.54	8.74
F	0.150	0.158	3.81	4.01
G	0.035		0.900	
J	0.004	0.008	0.10	0.20
K	0.034		0.690	
L	0.025		0.450	
M	0.020	0.045	0.51	1.14
α	0°		8°	

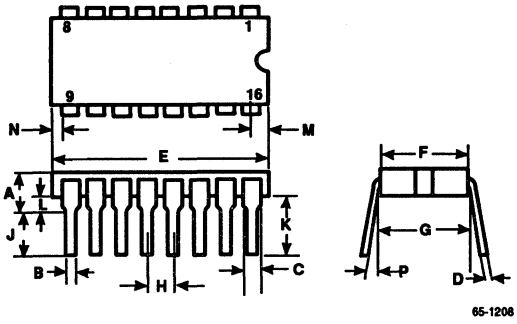
Dimensions conform to JEDEC Specification MS-012-AA for SO packages.

16-Lead Plastic Dual In-Line Package



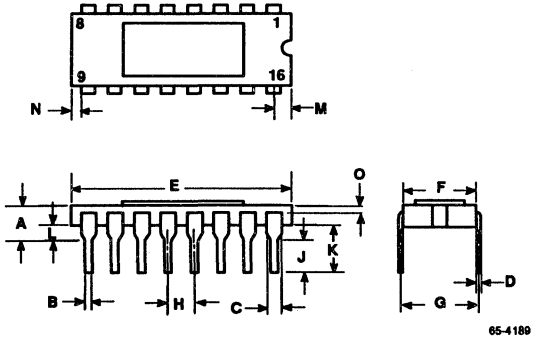
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.012	0.20	0.30
E	.740	.760	18.80	19.30
F	.240	.260	6.10	6.60
G	.290	.310	7.37	7.87
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	0.38	1.52
M	.080		2.03	
N	.005		0.13	
P	0°	15°	0°	15°

16-Lead Ceramic Dual In-Line Package



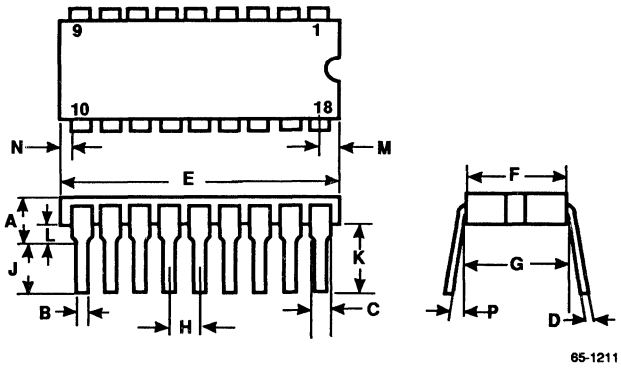
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	.36	.58
C	.050	.065	1.27	1.65
D	.008	.012	.20	.30
E	.749	.785	19.02	19.94
F	.260	.291	6.60	7.30
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.098		2.49
N	.005		.13	
P	.0°	15°	0°	15°

16-Lead Ceramic Sidebraze Dual In-Line Package



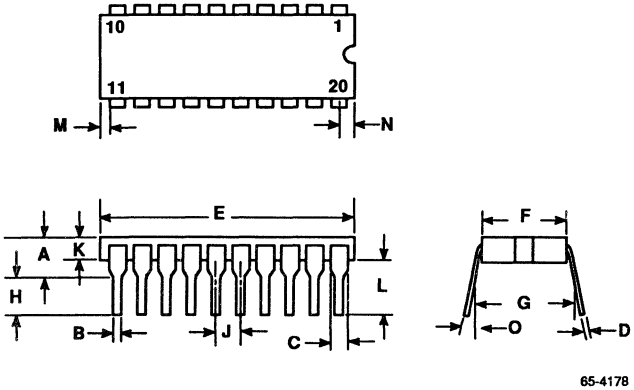
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	.36	.58
C	.038	.065	.96	1.65
D	.008	.013	.20	.33
E	.785	.830	19.34	21.08
F	.282	.310	7.16	7.87
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	.33	1.52
M		.098		2.49
N	.005		.13	
O	.005		.13	

18-Lead Ceramic Dual In-Line Package



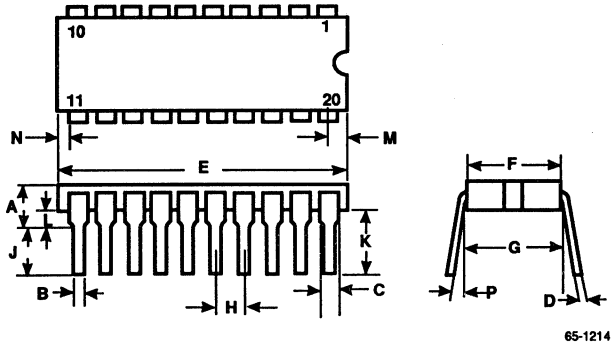
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.014	.023	.36	.58
C	.050	.065	1.27	1.65
D	.008	.012	.20	.30
E	.877	.918	22.28	23.32
F	.280	.310	7.11	7.87
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.060	.38	1.52
M		.098		2.49
N	.005		.13	
P	0°	15°	0°	15°

20-Lead Plastic Dual In-Line Package



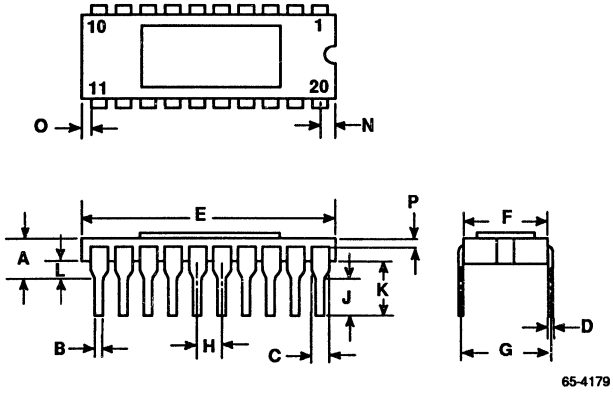
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.210		5.33
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.012	0.20	0.30
E	.995	1.065	25.27	27.05
F	.245	.310	6.22	7.87
G	.290	.320	7.37	8.13
H	.125	.200	3.18	5.08
J	.100 BSC		2.54 BSC	
K	.015		0.38	
L	.135		3.43	
M	.005		0.13	
N		.098		2.49
O	0°	15°	0°	15°

20-Lead Ceramic Dual In-Line Package



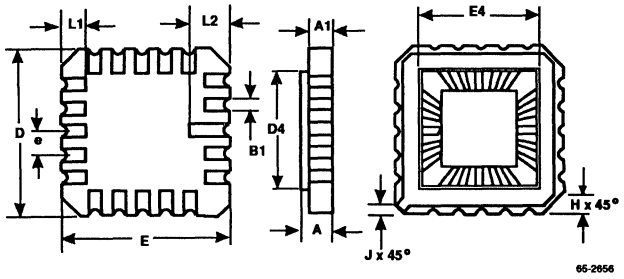
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.015	.021	.38	.53
C	.05	.065	1.27	1.65
D	.008	.012	.20	.30
E	.930	.975	23.60	24.80
F	.280	.310	7.11	7.87
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.070	.38	1.78
M		.098		2.49
N	.005		.13	
P	0°	15°	0°	15°

20-Lead Ceramic Sidebraze Dual In-Line Package



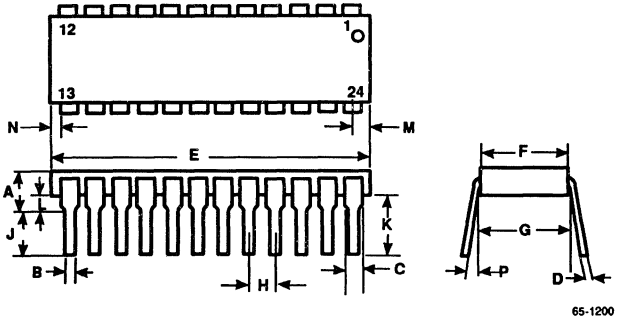
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.015	.021	.38	.53
C	.05	.065	1.27	1.65
D	.008	.012	.20	.30
E	.965	1.01	24.51	25.63
F	.277	.310	7.04	7.87
G	.290	.320	7.37	8.13
H	.100 BSC		2.54 BSC	
J	.125	.200	3.18	5.08
K	.150		3.81	
L	.015	.070	.38	1.78
M	.020		.51	
N		.080		2.03
O	.005		.13	
P	.005		.13	

20-Pad Leadless Chip Carrier



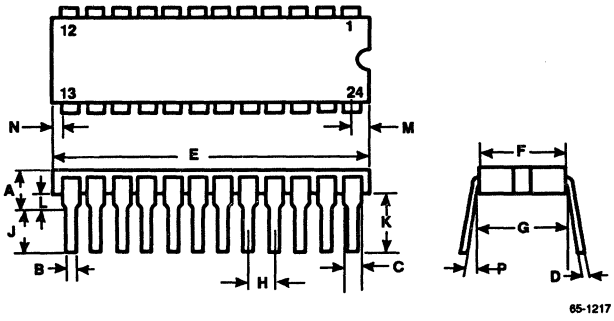
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.064	0.086	1.63	2.18
A1	0.054	0.066	1.37	1.68
B1	0.022	0.028	0.56	0.71
D	0.342	0.358	8.69	9.09
D4/E4		0.319		8.10
E	0.342	0.358	8.69	9.09
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L1	.045	.055	1.14	1.40
L2	.075	.095	1.91	2.41

24-Lead Plastic Dual In-Line Package (0.6" Wide)



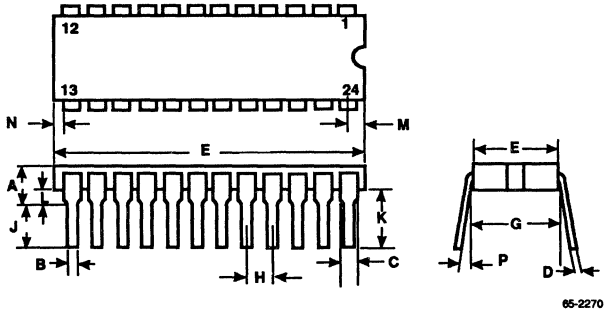
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.225		5.72
B	.014	.023	0.36	0.58
C	.030	.070	0.76	1.78
D	.008	.012	0.20	0.30
E	1.24	1.26	31.5	32.0
F	.530	.550	13.46	13.97
G	.590	.620	14.99	15.75
H	.100 BSC		2.54 BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.075	0.38	1.91
M		.098		2.49
N	.005		0.13	
P	0°	15°	0°	15°

24-Lead Ceramic Dual In-Line Package (0.6" Wide)



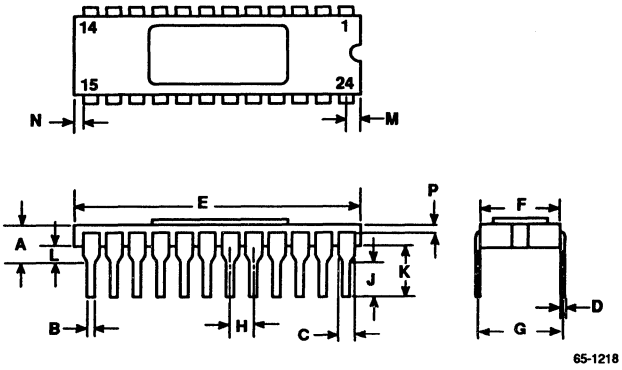
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.225		5.72
B	.014	.023	.36	.58
C	.038	.065	.96	1.65
D	.008	.012	.20	.30
E	1.234	1.284	31.34	32.61
F	.509	.546	12.93	13.87
G	.590	.620	14.99	15.75
H	.100 BSC		2.54 BSC	
J	.120	.200	3.05	5.08
K	.150		3.81	
L	.015	.075	.38	1.91
M		.098		2.49
N	.005		.13	
P	0°	15°	0°	15°

24-Lead Ceramic Dual In-Line Package (0.3" Wide)



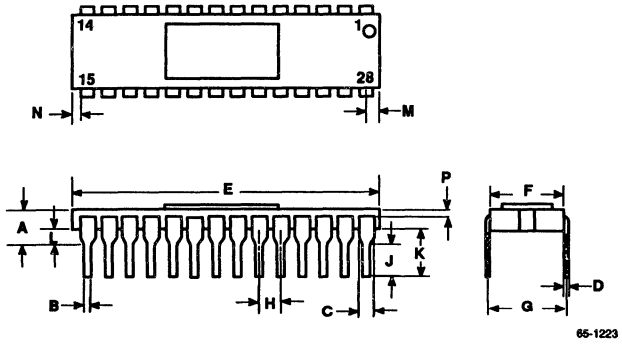
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	.015	.021	0.38	0.53
C	0.050	0.060	1.27	1.52
D	0.009	0.011	0.23	0.28
E		1.29		32.77
F	0.280	0.310	7.11	7.87
G	0.290	0.320	7.37	8.13
H	0.100 BSC		2.54 BSC	
J	0.120	0.200	3.05	5.08
K	0.150		3.81	
L	0.015	0.060	0.38	1.91
M		0.080		2.03
N	0.005		0.13	
P	0°	15°	0°	15°

24-Lead Ceramic Sidebraze Dual In-Line Package (0.3" wide)



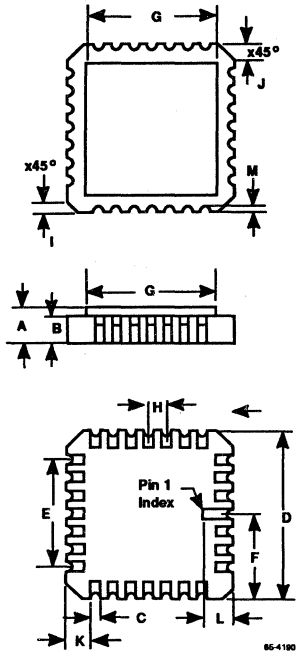
Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		0.200		5.08
B	0.016	0.022	0.40	0.56
C	0.038	0.065	0.96	1.65
D	0.008	0.012	0.20	0.30
E	1.10	1.29	27.94	32.77
F	0.280	0.310	7.11	7.87
G	0.290	0.320	7.37	8.13
H	0.100 BSC		2.54 BSC	
J	0.125	0.200	3.18	5.08
K	0.150		3.04	5.08
L	0.015	0.060	0.38	1.52
M		0.08		2.03
N	0.005		0.13	
P	0.005		0.13	

28-Lead Ceramic Sidebraze Dual In-Line Package



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A		.200		5.08
B	0.016	0.022	0.41	0.51
C	0.038	0.065	0.97	1.65
D	0.008	0.012	0.20	0.30
E	1.30	1.50	33.02	38.10
F	0.550	0.610	13.97	15.49
G	0.580	0.620	14.74	15.75
H	0.100 BSC		2.54 BSC	
J	0.125	0.200	3.175	5.08
K	0.150		3.81	
L	0.020	0.070	0.51	1.78
M		0.098		2.49
N	0.005		0.13	
P	0.005		0.13	

28-Pad Ceramic Leadless Chip Carrier



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	.091	.115	2.31	2.92
B	.063	.077	1.60	1.96
C	.020	.030	0.51	0.76
D	.44	.46	11.18	11.68
E	30 BSC		7.62 BSC	
F	.150 BSC		3.81 BSC	
G	.396	.404	10.06	10.26
H	.050 BSC		1.27 BSC	
J	.035	.045	0.89	1.14
K	.015	.025	0.38	0.64
L	.077	.093	1.96	2.36
M	.006	.013	.08	0.33

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