RCA Solid State

DATABOOK

Power MOSFETs

RCA Solid State

Power MOSFETs

SSD-223

RCA Power MOSFETs

This DATABOOK contains detailed technical information on the broad line of RCA power MOSFET products. These products include standard power MOSFETs (the popular RF-series types, the IRF series of industry replacement types, and JEDEC types), logic-level power MOSFETs (L^2FETs), COMFETs (conductivity-modulated FETs), power MOSFET chips, and high-reliability power MOSFETs. Moreover, in recognition of the frequent need for high-speed rectifiers in power MOSFET switching circuits, descriptive data on the RCA RUR series of ultra-fast-recovery rectifiers are also included in this DATABOOK.

The DATABOOK is divided into twelve major sections. The first section includes a complete index to types, product classification and selection charts, and industry replacement guides. Brief profiles of the various product categories are then presented followed by a technical overview that explains key performance characteristics, manufacturing operations, and quality-assurance provisions for RCA power MOSFETs.

Separate data sections provide definitive ratings and characteristics for each major product category of devices. Within each section, data pages for individual devices are included, as nearly as possible, in alpha-numerical sequence. Because some devices are grouped together to show similarity of function or data, some individual types numbers may be out of sequence. *If you don't find the type number that you are looking for where you expect it to be, check the Index to Devices.*

The DATABOOK also includes dimensional outlines of the various packages used for RCA power MOSFETs and ultra-fast-recovery rectifiers, application notes on RCA power MOSFETs, and listings of RCA sales offices, authorized distributors, and manufacturer's representatives.

RCA Solid State | Somerville, NJ • Brussels • Paris • London
Hamburg • Sao Paulo • Hong Kong

Contents

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices," Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, NJ 08876.

Information furnished by RCA is believed to be accurate and reliable. However, no responsibility is assumed by RCA for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of RCA.

Printed in USA/4-86

Quick-Reference Product Guide

RCA Power MOSFET Products

Index to Types

RCA Power MOSFET Products

Index to Types

Selection Charts

Standard Power MOSFETs — N-Channel

RCA TYPE	PKG	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS	Page No.	File No.
50V — 60V							
RFL2N05	TO-205	2	50	8.33	0.75	56	1497
RFP4N05	TO-220	4	50	25	0.60	56	1497
RFM15N05	TO-204	15	50	75	0.14	112	1478
RFP15N05	TO-220	15	50	60	0.14	112	1478
RFM25N05	TO-204	25	50	100	0.07	124	1492
RFP25N05	TO-220	25	50	75	0.07	124	1492
RFH45N05	TO-218	45	50	150	0.04	152	1635
RFK45N05	TO-204	45	50	150	0.04	156	1498
RFL2N06	TO-205	2	60	8.33	0.75	56	1497
IRFF113	TO-205	3	60	15	0.80	192	1562
IRF513	TO-220	3.5	60	20	0.80	272	1573
IRFF111	TO-205	3.5	60	15	0.60	192	1562
IRF511	TO-220	4	60	20	0.60	272	1573
RFP4N06	TO-220	4	60	25	0.60	56	1497
IRFF123	TO-205	5	60	20	0.40	197	1563
IRFF121	TO-205	6	60	20	0.30	197	1563
IRF123	TO-204	7	60	40	0.40	207	1565
IRF523	TO-220	7	60	40	0.40	277	1574
IRFF133	TO-205	7	60	25	0.25	202	1564
IRF121	TO-204	8	60	40	0.30	207	1565
IRF521	TO-220	8	60	40	0.30	277	1574
IRFF131	TO-205	8	60	25	0.18	202	1564
IRF133	TO-204	12	60	75	0.25	212	1566
IRF533	TO-220	12	60	75	0.25	282	1575
IRF131	TO-204	14	60	75	0.18	212	1566
IRF531	TO-220	14	60	75	0.18	282	1575
RFM15N06	TO-204	15	60	75	0.14	112	1478
RFP15N06	TO-220	15	60	60	0.14	112	1478
RFM25N06	TO-204	25	60	100	0.07	124	1492
RFP25N06	TO-220	25	60	75	0.07	124	1492
IRF153	TO-204	33	60	150	0.08	217	1824
IRF151	TO-204	40	60	150	0.055	217	1824
RFH45N06	TO-218	45	60	150	0.04	152	1635
RFK45N06	TO-204	45	60	150	0.04	156	1498
80V — 100V							
RFL1N08	TO-205	1	80	8.33	1.20	40	1385
RFP2N08	TO-220	2	80	25	1.05	40	1385
RFM12N08	TO-204	12	80	75	0.20	96	1386
RFP12N08	TO-220	12	80	60	0.20	96	1386
RFM18N08	TO-204	18	80	100	0.10	120	1446
RFP18N08	TO-220	18	80	75	0.10	120	1446
RFH35N08	TO-218	35	80	150	0.055	144	1634
RFK35N08	TO-204	35	80	150	0.055	148	1499
RFL1N10	TO-205	1	100	8.33	1.20	40	1385
RFP2N10	TO-220	2	100	25	1.05	40	1385
IRFF112	TO-205	3	100	15	0.80	192	1562
IRF512	TO-220	3.5	100	20	0.80	272	1573
IRFF110	TO-205	3.5	100	15	0.60	192	1562
IRF510	TO-220	4	100	20	0.60	272	1573
IRFF122	TO-205	5	100	20	0.40	197	1563
IRFF120	TO-205	6	100	20	0.30	197	1563
IRF122	TO-204	7	100	40	0.40	207	1565
IRF522	TO-220	7	100	40	0.40	277	1574
IRFF132	TO-205	7	100	25	0.25	202	1564
IRF120	TO-204	8	100	40	0.30	207	1565
IRF520	TO-220	8	100	40	0.30	277	1574
IRFF130	TO-205	8	100	25	0.18	202	1564
IRF132	TO-204	12	100	75	0.25	212	1566
IRF532	TO-220	12	100	75	0.25	96	1575
RFM12N10	TO-220	12	100	75	0.20	282	1386
RFP12N10	TO-220	12	100	60	0.20	96	1386
IRF130	TO-204	14	100	75	0.18	212	1566
IRF530	TO-220	14	100	75	0.18	282	1575
RFM18N10	TO-204	18	100	100	0.10	120	1446
RFP18N10	TO-220	18	100	75	0.10	120	1446
IRF152	TO-204	33	100	150	0.08	217	1824
RFH35N10	TO-218	35	100	150	0.055	144	1634
RFK35N10	TO-204	35	100	150	0.055	148	1499
IRF150	TO-204	40	100	150	0.055	217	1824

RCA TYPE	PKG	I_o (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS	Page No.	File No.
120V — 150V							
RFL1N12	TO-205	1	120	8.33	1.90	44	1444
RFP2N12	TO-220	2	120	25	1.75	44	1444
RFL4N12	TO-205	4	120	8.33	0.40	64	1462
RFM10N12	TO-204	10	120	75	0.30	84	1445
RFP10N12	TO-220	10	120	60	0.30	84	1445
RFM15N12	TO-204	15	120	100	0.15	116	1443
RFP15N12	TO-220	15	120	75	0.15	116	1443
RFH30N12	TO-218	30	120	150	0.075	136	1633
RFK30N12	TO-204	30	120	120	0.075	140	1455
RFL1N15	TO-205	1	150	8.33	1.90	44	1444
IRF613	TO-220	2	150	20	2.40	287	1576
RFP2N15	TO-220	2	150	25	1.75	44	1444
IRF611	TO-220	2.5	150	20	1.50	287	1576
RFL4N15	TO-205	4	150	8.33	0.40	64	1462
IRF223	TO-204	4	150	40	1.20	222	1567
IRF623	TO-220	4	150	40	1.20	292	1577
IRF221	TO-204	5	150	40	0.80	222	1567
IRF621	TO-220	5	150	40	0.80	292	1577
IRF233	TO-204	8	150	75	0.60	227	1568
IRF633	TO-220	8	150	75	0.60	297	1578
IRF231	TO-204	9	150	75	0.40	227	1568
IRF631	TO-220	9	150	75	0.40	297	1578
RFM10N15	TO-204	10	150	75	0.30	84	1445
RFP10N15	TO-220	10	150	60	0.30	84	1445
RFM15N15	TO-204	15	150	100	0.15	116	1443
RFP15N15	TO-220	15	150	75	0.15	116	1443
IRF243	TO-204	16	150	75	0.22	232	1584
IRF643	TO-220	16	150	125	0.22	302	1585
IRF241	TO-204	18	150	75	0.18	232	1584
IRF641	TO-220	18	150	125	0.18	302	1585
IRF253	TO-204	25	150	150	0.12	237	1825
IRF251	TO-204	30	150	150	0.085	237	1825
RFH30N15	TO-218	30	150	150	0.075	136	1633
RFK30N15	TO-204	30	150	120	0.075	140	1455
180V — 350V							
RFL1N18	TO-205	1	180	8.33	3.65	48	1442
RFP2N18	TO-220	2	180	25	3.50	48	1442
RFM8N18	TO-204	8	180	75	0.50	80	1447
RFP8N18	TO-220	8	180	60	0.50	80	1447
RFM12N18	TO-204	12	180	100	0.25	100	1461
RFP12N18	TO-220	12	180	75	0.25	100	1461
RFH25N18	TO-218	25	180	150	0.15	128	1631
RFK25N18	TO-204	25	180	150	0.15	132	1500
RFL1N20	TO-205	1	200	8.33	3.65	48	1442
IRF612	TO-220	2	200	20	2.40	287	1576
RFP2N20	TO-220	2	200	25	3.50	48	1442
IRF610	TO-220	2.5	200	20	1.50	287	1576
IRF222	TO-204	4	200	40	1.20	222	1567
IRF622	TO-220	4	200	40	1.20	292	1577
IRF220	TO-204	5	200	40	0.80	222	1567
IRF620	TO-220	5	200	40	0.80	292	1577
IRF232	TO-204	8	200	75	0.60	227	1568
IRF632	TO-220	8	200	75	0.60	297	1578
RFM8N20	TO-204	8	200	75	0.50	80	1447
RFP8N20	TO-220	8	200	60	0.50	80	1447
IRF230	TO-204	9	200	75	0.40	227	1568
IRF630	TO-220	9	200	75	0.40	297	1578
RFM12N20	TO-204	12	200	100	0.25	100	1461
RFP12N20	TO-220	12	200	75	0.25	100	1461
IRF252	TO-204	25	200	150	0.12	237	1825
RFH25N20	TO-218	25	200	150	0.15	128	1631
RFK25N20	TO-204	25	200	150	0.15	132	1500
IRF250	TO-204	30	200	150	0.085	237	1825
RFP1N35	TO-220	1	350	25	9.00	52	1537
IRF323	TO-204	2.5	350	40	2.50	242	1569
IRF723	TO-220	2.5	350	40	2.50	307	1579
IRF321	TO-204	3	350	40	1.80	242	1569
IRF721	TO-220	3	350	40	1.80	307	1579
RFM4N35	TO-204	4	350	75	1.50	68	1491

Selection Charts

Standard Power MOSFETs — N-Channel

RCA TYPE	PKG	I_o (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS	Page No.	File No.
180V — 350V							
RFP4N35	TO-220	4	350	60	1.50	68	1491
IRF333	TO-204	4.5	350	75	1.50	247	1570
IRF733	TO-220	4.5	350	75	1.50	312	1580
IRF331	TO-204	5.5	350	75	1.00	247	1570
IRF731	TO-220	5.5	350	75	1.00	312	1580
RFM7N35	TO-204	7	350	100	0.75	76	1536
RFP7N35	TO-220	7	350	75	0.75	76	1536
RFH12N35	TO-218	12	350	150	0.38	104	1630
RFM12N35	TO-204	12	350	150	0.38	108	1515
IRF353	TO-204	13	350	150	0.4	252	1826
IRF351	TO-204	15	350	150	0.3	252	1826
400V — 500V							
RFP1N40	TO-220	1	400	25	9.00	52	1537
IRF322	TO-204	2.5	400	40	2.50	242	1569
IRF722	TO-220	2.5	400	40	2.50	307	1579
IRF320	TO-204	3	400	40	1.80	242	1569
IRF720	TO-220	3	400	40	1.80	307	1579
RFM4N40	TO-204	4	400	75	1.50	68	1491
RFP4N40	TO-220	4	400	60	1.50	68	1491
IRF332	TO-204	4.5	400	75	1.50	247	1570
IRF732	TO-220	4.5	400	75	1.50	312	1580
IRF330	TO-204	5.5	400	75	1.00	247	1570
IRF730	TO-220	5.5	400	75	1.00	312	1580
RFM7N40	TO-204	7	400	100	0.75	76	1536
RFP7N40	TO-220	7	400	75	0.75	76	1536
RFH12N40	TO-218	12	400	150	0.38	104	1630
RFM12N40	TO-204	12	400	150	0.38	108	1515
IRF352	TO-204	13	400	150	0.4	252	1826
IRF350	TO-204	15	400	150	0.3	252	1826
IRF423	TO-204	2	450	40	4.00	257	1571
IRF823	TO-220	2	450	40	4.00	317	1581
IRF421	TO-204	2.5	450	40	3.00	257	1571
IRF821	TO-220	2.5	450	40	3.00	317	1581
RFM3N45	TO-204	3	450	75	2.50	60	1384
RFP3N45	TO-220	3	450	60	2.50	60	1384
IRF433	TO-204	4	450	75	2.00	262	1572
IRF833	TO-220	4	450	75	2.00	322	1582
IRF431	TO-204	4.5	450	75	1.50	262	1572
IRF831	TO-220	4.5	450	75	1.50	322	1582
RFM6N45	TO-204	6	450	100	1.25	72	1494
RFP6N45	TO-220	6	450	75	1.25	72	1494
RFH10N45	TO-218	10	450	150	0.60	88	1629
RFM10N45	TO-204	10	450	150	0.60	92	1493
IRF453	TO-204	12	450	150	0.5	267	1827
IRF451	TO-204	13	450	150	0.4	267	1827
IRF422	TO-204	2	500	40	4.00	257	1571
IRF822	TO-220	2	500	40	4.00	317	1581
IRF420	TO-204	2.5	500	40	3.00	257	1571
IRF820	TO-220	2.5	500	40	3.00	317	1581
RFM3N50	TO-204	3	500	75	2.50	60	1384
RFP3N50	TO-220	3	500	60	2.50	60	1384
IRF432	TO-204	4	500	75	2.00	262	1572
IRF832	TO-220	4	500	75	2.00	322	1582
IRF430	TO-204	4.5	500	75	1.50	262	1572
IRF830	TO-220	4.5	500	75	1.50	322	1582
RFM6N50	TO-204	6	500	100	1.25	72	1494
RFP6N50	TO-220	6	500	75	1.25	72	1494
RFH10N50	TO-218	10	500	150	0.60	88	1629
RFM10N50	TO-204	10	500	150	0.60	92	1493
IRF452	TO-204	12	500	150	0.5	267	1827
IRF450	TO-204	13	500	150	0.4	267	1827

JEDEC Types

RCA TYPE	PKG	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS	Page No.	File No.
60V — 150V							
2N6755	TO-204	12	60	75	0.25	327	1586
2N6782	TO-205	3.5	100	15	0.60	351	1592
50V — 100V							
2N6788	TO-205	6	100	20	0.30	356	1593
2N6796	TO-205	8	100	25	0.18	361	1594
2N6756	TO-204	14	100	75	0.18	327	1586
2N6764	TO-204	38	100	150	0.055	343	1590
2N6757	TO-204	8	150	75	0.60	331	1587
200V — 500V							
2N6758	TO-204	9	200	75	0.40	331	1587
2N6766	TO-204	30	200	150	0.085	347	1591
2N6759	TO-204	4.5	350	75	1.50	335	1588
2N6760	TO-204	5.5	400	75	1.00	335	1588
2N6761	TO-204	4	450	75	2.00	339	1589
2N6762	TO-204	4.5	500	75	1.50	339	1589

Standard Power MOSFETs — P-Channel

RCA TYPE	PKG	I_D (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS	Page No.	File No.
80V — 100V							
RFL1P08	TO-205	1	80	8.33	3.15	160	1535
RFP2P08	TO-220	2	80	25	3.00	160	1535
RFM6P08	TO-204	6	80	60	0.60	168	1490
RFP6P08	TO-220	6	80	60	0.60	168	1490
RFM8P08	TO-204	8	80	100	0.40	172	1496
RFP8P08	TO-220	8	80	75	0.40	172	1496
RFM12P08	TO-204	12	80	100	0.30	180	1495
RFP12P08	TO-220	12	80	75	0.30	180	1495
RFH25P08	TO-218	25	80	150	0.15	184	1632
RFK25P08	TO-204	25	80	150	0.15	188	1516
RFL1P10	TO-205	1	100	8.33	3.15	160	1535
RFP2P10	TO-220	2	100	25	3.00	160	1535
RFM6P10	TO-204	6	100	60	0.60	168	1490
RFP6P10	TO-220	6	100	60	0.60	168	1490
RFM8P10	TO-204	8	100	100	0.40	172	1496
RFP8P10	TO-220	8	100	75	0.40	172	1496
RFM12P10	TO-204	12	100	100	0.30	180	1495
RFP12P10	TO-220	12	100	75	0.30	180	1495
RFH25P10	TO-218	25	100	150	0.15	184	1632
RFK25P10	TO-204	25	100	150	0.15	188	1516
120V — 150V							
RFM5P12	TO-204	5	120	60	1.00	164	1463
RFP5P12	TO-220	5	120	60	1.00	164	1463
RFM10P12	TO-204	10	120	100	0.50	176	1595
RFP10P12	TO-220	10	120	75	0.50	176	1595
RFM5P15	TO-204	5	150	60	1.00	164	1463
RFP5P15	TO-220	5	150	60	1.00	164	1463
RFM10P15	TO-204	10	150	100	0.50	176	1595
RFP10P15	TO-220	10	150	75	0.50	176	1595

L^2FETs — N-Channel Types

RCA TYPE	PKG	I_o (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS	Page No.	File No.
50V — 100V							
RFL2N05L	TO-205	2	50	8.33	0.75	380	1560
RFP4N05L	TO-220	4	50	25	0.60	380	1560
RFM15N05L	TO-204	15	50	75	0.14	396	1558
RFP15N05L	TO-220	15	50	60	0.14	396	1558
RFL2N06L	TO-205	2	60	8.33	0.75	380	1560
RFP4N06L	TO-220	4	60	25	0.60	380	1560
RFM15N06L	TO-204	15	60	75	0.14	396	1558
RFP15N06L	TO-220	15	60	60	0.14	396	1558
RFL1N08L	TO-205	1	80	8.33	1.20	368	1510
RFP2N08L	TO-220	2	80	25	1.05	368	1510
RFM12N08L	TO-204	12	80	75	0.20	392	1512
RFP12N08L	TO-220	12	80	60	0.20	392	1512
RFL1N10L	TO-205	1	100	8.33	1.20	368	1510

Selection Charts

L²FETs — N-Channel Types

RCA TYPE	PKG	I_o (A)	V_{DSS} (V)	P_D (W)	$r_{DS(ON)}$ OHMS	Page No.	File No.
50V — 100V							
RFP2N10L	TO-220	2	100	25	1.05	368	1510
RFM12N10L	TO-204	12	100	75	0.20	392	1512
RFP12N10L	TO-220	12	100	60	0.20	392	1512
120V — 200V							
RFL1N12L	TO-205	1	120	8.33	1.90	372	1513
RFP2N12L	TO-220	2	120	25	1.75	372	1513
RFM10N12L	TO-204	10	120	75	0.30	388	1559
RFP10N12L	TO-220	10	120	60	0.30	388	1559
RFL1N15L	TO-205	1	150	8.33	1.90	372	1513
RFP2N15L	TO-220	2	150	25	1.75	372	1513
RFM10N15L	TO-204	10	150	75	0.30	388	1559
RFP10N15L	TO-220	10	150	60	0.30	388	1559
RFL1N18L	TO-205	1	180	8.33	3.65	376	1511
RFP2N18L	TO-220	2	180	25	3.50	376	1511
RFM8N18L	TO-204	8	180	75	0.50	384	1514
RFP8N18L	TO-220	8	180	60	0.50	384	1514
RFL1N20L	TO-205	1	200	8.33	3.65	376	1511
RFP2N20L	TO-220	2	200	25	3.50	376	1511
RFM8N20L	TO-204	8	200	75	0.50	384	1514
RFP8N20L	TO-220	8	200	60	0.50	384	1514

Conductivity-Modulated Field-Effect Transistors — COMFETS

RCA TYPE	PKG	I_D (A)	V_{DSS} (V)	P_D (W)	$V_{DS(ON)}$ (V)	Page No.	File No.
350V — 400V							
RCH10N35	TO-218	10	350	75	2.70	402	1697
RCP10N35	TO-220	10	350	60	2.70	402	1697
RCH10N40	TO-218	10	400	75	2.70	402	1697
RCP10N40	TO-220	10	400	60	2.70	402	1697

Ultra-Fast — Recovery Rectifiers

RCA TYPE	PKG	I_F	V_{RRM}	Circuit	Page No.	File No.
BYW51-100	TO-220	8	100	D	460	1412
RUR-810	TO-220	8	100	S	462	1355
RUR-D810	TO-220	8	100	D	464	1356
RUR-D1610	TO-204	16	100	D	466	1383
BYW51-150	TO-220	8	150	D	460	1412
RUR-815	TO-220	8	150	S	462	1355
RUR-D815	TO-220	8	150	D	464	1356
RUR-D1615	TO-204	16	150	D	466	1383
BYW51-200	TO-220	8	200	D	460	1412
RUR-820	TO-220	8	200	S	462	1355
RUR-D820	TO-220	8	200	D	464	1356
RUR-D1620	TO-204	16	200	D	466	1383

S = Single diode circuit

D = Dual common cathode

Industry Replacement Guide

Power MOSFETs

Industry Type	RCA Type
2N6659	RFL1N08
2N6660	RFL1N12
2N6661	RFL1N12
2N6755	2N6755
2N6756	2N6756
2N6757	2N6757
2N6758	2N6758
2N6759	2N6759
2N6760	2N6760
2N6761	2N6761
2N6762	2N6762
2N6763	RFK45N06
2N6764	2N6764
2N6765	RFM15N15
2N6766	2N6766
2N6782	2N6782
2N6788	2N6788
2N6796	2N6796
2N6829	RFM12N10
2N6830	RFM12N08
BUZ10B	RFP15N05
BUZ14	RFK45N05
BUZ14A	RFK45N05
BUZ14B	RFM25N05
BUZ14C	RFM15N05
BUZ14D	RFM15N05
BUZ20	RFP12N10
BUZ20A	RFP12N10
BUZ20B	RFP12N10
BUZ23	RFM12N10
BUZ23A	RFM15N12
BUZ23B	RFM10N12
BUZ24B	RFK30N12
BUZ30	RFP8N20
BUZ32	RFP12N20
BUZ32A	RFP10N15
BUZ32B	RFP8N20
BUZ32C	RFP8N18
BUZ33	RFM8N20
BUZ33A	RFM8N20
BUZ33B	RFM10N15
BUZ35	RFM12N20
BUZ35A	RFM10N15
BUZ41A	RFP6N50
BUZ41B	RFP6N45
BUZ42	RFP6N50
BUZ42A	RFP6N45
BUZ42B	RFP3N50
BUZ42C	RFP3N45
BUZ42D	RFP3N50
BUZ44A	RFM6N50
BUZ44B	RFM6N45
BUZ45A	RFM10N50
BUZ46	RFM6N50
BUZ46A	RFM6N45
BUZ46B	RFM3N50
BUZ60	RFP7N40
BUZ60A	RFP7N35
BUZ60B	RFP7N40
BUZ60C	RFP7N35
BUZ60D	RFP7N40
BUZ63	RFM7N40
BUZ63A	RFM7N35
BUZ63B	RFM7N40
BUZ63C	RFM7N35

Industry Type	RCA Type
BUZ63D	RFM7N40
BUZ71A	RFP15N05
D84CK1	RFP15N05
D84CK2	RFP15N06
D84CL1	RFP12N08
D84CL2	RFP12N10
D84CM1	RFP8N18
D84CM2	RFP8N18
D84CN1	RFP8N18
D84CN2	RFP8N20
D84CQ1	RFP4N35
D84CQ2	RFP4N40
D84CR1	RFP3N45
D84CR2	RFP3N50
D84DK1	RFP15N05
D84DK2	RFP15N06
D84DL1	RFP18N08
D84DL2	RFP18N10
D84DM1	RFP10N12
D84DM2	RFP10N15
D84DN1	RFP12N18
D84DN2	RFP12N20
D84DQ1	RFP7N35
D84DQ2	RFP7N40
D84DR1	RFP6N45
D84DR2	RFP6N50
D84EK1	RFP25N05
D84EK2	RFP25N06
D84EM1	RFP15N12
D84EM2	RFP15N15
D86DK1	RFM15N05
D86DK2	RFM15N06
D86DL1	RFM18N08
D86DL2	RFM18N10
D86DM1	RFM10N12
D86DM2	RFM10N15
D86DN1	RFM12N18
D86DN2	RFM12N20
D86DQ1	RFM7N35
D86DQ2	RFM7N40
D86DR1	RFM6N45
D86DR2	RFM6N50
D86EK1	RFM25N05
D86EK2	RFM25N06
D86EL1	RFM35N08
D86EL2	RFM35N10
D86EM1	RFM15N12
D86EM2	RFM15N15
D86EN1	RFK25N18
D86EN2	RFK25N20
D86EQ1	RFM12N35
D86EQ2	RFM12N40
D86ER1	RFM10N45
D86ER2	RFM10N50
D86FK1	RFK45N05
D86FK2	RFK45N06
D86FL1	RFK35N08
D86FL2	RFK35N10
D86FM1	RFK30N12
D86FM2	RFK30N15
D86FQ1	RFM12N35
D86FQ2	RFM12N40
D88FK1	RFH45N05
D88FK2	RFH45N06
D88FL1	RFH35N05

Industry Type	RCA Type
D88FL2	RFH35N06
D88FM1	RFH30N12
D88FM2	RFH30N15
IRF120	IRF120
IRF121	IRF121
IRF122	IRF122
IRF123	IRF123
IRF130	IRF130
IRF131	IRF131
IRF132	IRF132
IRF133	IRF133
IRF140	RFM18N10
IRF141	RFM25N06
IRF142	RFM18N10
IRF143	RFM25N06
IRF150	IRF150
IRF151	IRF151
IRF152	IRF152
IRF153	IRF153
IRF220	IRF220
IRF221	IRF221
IRF222	IRF222
IRF223	IRF223
IRF230	IRF230
IRF231	IRF231
IRF232	IRF232
IRF233	IRF233
IRF240	RFM12N20
IRF241	IRF241
IRF242	RFM12N20
IRF243	IRF243
IRF250	IRF250
IRF251	IRF251
IRF252	IRF252
IRF253	IRF253
IRF320	IRF320
IRF321	IRF321
IRF322	IRF322
IRF323	IRF323
IRF330	IRF330
IRF331	IRF331
IRF332	IRF332
IRF333	IRF333
IRF340	RFM12N40
IRF341	RFM12N35
IRF342	RFM7N40
IRF343	RFM7N35
IRF350	IRF350
IRF351	IRF351
IRF352	IRF352
IRF353	IRF353
IRF420	IRF420
IRF421	IRF421
IRF422	IRF422
IRF423	IRF423
IRF430	IRF430
IRF431	IRF431
IRF432	IRF432
IRF433	IRF433
IRF440	RFM10N50
IRF441	RFM10N45
IRF442	RFM6N50
IRF443	RFM6N45
IRF450	IRF450
IRF451	IRF451

Industry Type	RCA Type
IRF452	IRF452
IRF453	IRF453
IRF510	IRF510
IRF511	IRF511
IRF512	IRF512
IRF513	IRF513
IRF520	IRF520
IRF521	IRF521
IRF522	IRF522
IRF523	IRF523
IRF530	IRF530
IRF531	IRF531
IRF532	IRF532
IRF533	IRF533
IRF540	RFP18N10
IRF541	RFP25N06
IRF542	RFP18N10
IRF543	RFP25N06
IRF610	IRF610
IRF611	IRF611
IRF612	IRF612
IRF613	IRF613
IRF620	IRF620
IRF621	IRF621
IRF622	IRF622
IRF623	IRF623
IRF630	IRF630
IRF631	IRF631
IRF632	IRF632
IRF633	IRF633
IRF640	RFP12N20
IRF641	IRF641
IRF642	RFP12N20
IRF643	IRF643
IRF710	RFP4N40
IRF711	RFP4N35
IRF712	RFP4N40
IRF713	RFP4N35
IRF720	IRF720
IRF721	IRF721
IRF722	IRF722
IRF723	IRF723
IRF730	IRF730
IRF731	IRF731
IRF732	IRF732
IRF733	IRF733
IRF742	RFP7N40
IRF743	RFP7N35
IRF820	IRF820
IRF821	IRF821
IRF822	IRF822
IRF823	IRF823
IRF830	IRF830
IRF831	IRF831
IRF832	IRF832
IRF833	IRF833
IRF9130	RFM12P10
IRF9131	RFM12P08
IRF9132	RFM8P10
IRF9133	RFM8P08
IRF9231	RFM10P15
IRF9233	RFM5P15
IRF9510	RFP5P12
IRF9511	RFP5N12
IRF9512	RFP5P12

Industry Replacement Guide

Power MOSFETs

Industry Type	RCA Type
IRF9513	RFP5P12
IRF9520	RFP6P10
IRF9521	RFP6P08
IRF9522	RFP6P10
IRF9523	RFP6P08
IRF9530	RFP12P10
IRF9531	RFP12P08
IRF9532	RFP8P10
IRF9533	RFP8P08
IRF9611	RFP5P15
IRF9613	RFP5P15
IRF9621	RFP5P15
IRF9623	RFP5P15
IRF9631	RFP10P15
IRF9633	RFP5P15
IRFF110	IRFF110
IRFF111	IRFF111
IRFF112	IRFF112
IRFF113	IRFF113
IRFF120	IRFF120
IRFF121	IRFF121
IRFF122	IRFF122
IRFF123	IRFF123
MTH8N35	RFH12N35
MTH8N40	RFH12N40
MTH15N18	RFH25N18
MTH15N20	RFH25N20
MTH20N12	RFH30N12
MTH20N15	RFH30N15
MTH25N08	RFH35N08
MTH25N10	RFH35N10
MTH35N05	RFH45N05
MTH35N06	RFH45N06
MTM2N45	RFM3N45
MTM2N50	RFM3N50
MTM3N40	RFM4N40
MTM3N45	RFM4N35
MTM4N45	RFM6N45
MTM4N50	RFM6N50
MTM5N18	RFM8N18
MTM5N20	RFM8N20
MTM5N35	RFM7N35
MTM5N40	RFM7N40
MTM7N12	RFM8N18
MTM7N15	RFM8N18
MTM7N18	RFM8N18
MTM7N20	RFM8N20
MTM8N08	RFM8N18
MTM8N10	RFM8N18
MTM8N12	RFM10N12
MTM8N15	RFM10N15
MTM8N18	RFM8N18
MTM8N20	RFM8N20
MTM10N05	RFM15N05
MTM10N06	RFM15N06
MTM10N08	RFM12N08
MTM10N10	RFM12N10
MTM10N12	RFM10N12
MTM10N15	RFM10N15
MTM12N05	RFM15N05
MTM12N06	RFM15N06
MTM12N08	RFM12N08
MTM12N10	RFM12N10
MTM12N18	RFM12N18
MTM12N20	RFM12N20

Industry Type	RCA Type
MTM15N05	RFM15N05
MTM15N06	RFM15N06
MTM15N12	RFM15N12
MTM15N15	RFM15N15
MTM20N08	RFM18N08
MTM20N10	RFM18N10
MTM25N05	RFM25N05
MTM25N06	RFM25N06
MTP1N45	RFP3N45
MTP1N50	RFP3N50
MTP2N35	RFP4N35
MTP2N40	RFP4N40
MTP2N45	RFP3N45
MTP2N50	RFP3N50
MTP3N35	RFP4N35
MTP3N40	RFP4N40
MTP4N45	RFP6N45
MTP4N50	RFP6N50
MTP5N18	RFP8N18
MTP5N20	RFP8N20
MTP5N35	RFP7N35
MTP5N40	RFP7N40
MTP7N12	RFP8N18
MTP7N15	RFP8N18
MTP7N18	RFP8N18
MTP7N20	RFP8N20
MTP8N08	RFP8N18
MTP8N10	RFP8N18
MTP8N12	RFP10N12
MTP8N15	RFP10N15
MTP8N18	RFP8N18
MTP8N20	RFP8N20
MTP10N05	RFP15N05
MTP10N06	RFP15N06
MTP10N08	RFP12N08
MTP10N10	RFP12N10
MTP10N12	RFP10N12
MTP10N15	RFP10N15
MTP12N05	RFP15N05
MTP12N06	RFP15N06
MTP12N08	RFP12N08
MTP12N10	RFP12N10
MTP12N18	RFP12N18
MTP12N20	RFP12N20
MTP15N05	RFP15N05
MTP15N06	RFP15N06
MTP15N12	RFP15N12
MTP15N15	RFP15N15
MTP20N08	RFP18N08
MTP20N10	RFP18N10
MTP25N05	RFP25N05
MTP25N06	RFP25N06
VN30AB	RFL1N12
VN35AB	RFL1N12
VN40AD	RFP2N12
VN46AD	RFP2N12
VN64GA	RFM10N12
VN66AD	RFP2N12
VN67AB	RFL1N12
VN67AD	RFP2N12
VN88AD	RFP2N12
VN89AB	RFL1N12
VN89AD	RFP2N12
VN90AB	RFL1N12
VN99AB	RFL1N12

Industry Type	RCA Type
VN010N2	RFL1N12
VN0104N5	RFP2N12
VN0106N2	RFL1N12
VN0106N5	RFP2N12
VN0108N2	RFL1N12
VN0108N5	RFP2N12
VN0109N2	RFL1N12
VN0109N5	RFP2N12
VN0204N2	RFL1N08
VN0204N5	RFP2N08
VN0206N2	RFL1N08
VN0206N5	RFP2N08
VN0208N2	RFL1N08
VN0208N5	RFP2N08
VN0209N2	RFL1N10
VN0209N5	RFP2N10
VN0330N1	RFM3N45
VN0330N5	RFP3N45
VN0335N1	RFM3N45
VN0335N5	RFP3N45
VN0340N1	RFM3N45
VN0340N5	RFP3N45
VN0345N1	RFM3N45
VN0345N5	RFP3N45
VN1204N1	RFM10N12
VN1204N5	RFP10N12
VN1206N1	RFM10N12
VN1206N5	RFP10N12
VN1208N1	RFM10N12
VN1208N5	RFP10N12
VN1209N1	RFM10N12
VN1209N5	RFP10N12
ZVN01A2B	RFL1N08
ZVN01A2L	RFP2N08
ZVN01A3B	RFL1N08
ZVN01A3L	RFP2N08
ZVN11A2L	RFP10N12
ZVN11A2M	RFM10N12
ZVN11A3L	RFP10N12
ZVN11A3M	RFM10N12
ZVN12A2L	RFP12N08
ZVN12A2M	RFM12N08
ZVN12A3L	RFP12N08
ZVN12A3M	RFM12N08
ZVN020FL	RFP2N08
ZVN0104B	RFL1N12
ZVN0104L	RFP2N12
ZVN0106B	RFL1N12
ZVN0106L	RFP2N12
ZVN0108B	RFL1N12
ZVN0108L	RFP2N12
ZVN0109B	RFL1N12
ZVN0109L	RFP2N12
ZVN0110B	RFL1N12
ZVN0110L	RFP2N12
ZVN0114B	RFL1N15
ZVN0114L	RFP2N15
ZVN0204B	RFL1N12
ZVN0206B	RFL1N12
ZVN0206L	RFP2N08
ZVN0208B	RFL1N12
ZVN0208L	RFP2N08
ZVN0209B	RFL1N12
ZVN0209L	RFP2N08
ZVN0210B	RFL1N12

Industry Type	RCA Type
ZVN0210L	RFP2N08
ZVN0214B	RFL1N15
ZVN0214L	RFP2N15
ZVN0216B	RFL1N18
ZVN0216L	RFP2N18
ZVN0220B	RFL1N20
ZVN0220L	RFP2N20
ZVN0330L	RFP3N45
ZVN0330M	RFM3N45
ZVN0335L	RFP3N45
ZVN0335M	RFM3N45
ZVN0340L	RFP3N45
ZVN0340M	RFM3N45
ZVN0345L	RFP3N45
ZVN0345M	RFM3N50
ZVN0350L	RFP3N50
ZVN0350M	RFM3N50
ZVN1104L	RFP10N12
ZVN1104M	RFM10N12
ZVN1106L	RFP10N12
ZVN1106M	RFM10N12
ZVN1108L	RFP10N12
ZVN1108M	RFM10N12
ZVN1109L	RFP10N12
ZVN1109M	RFM10N12
ZVN1110B	RFL1N12
ZVN1110L	RFP2N12
ZVN1114B	RFL1N15
ZVN1114L	RFP2N15
ZVN1116B	RFL1N18
ZVN1116L	RFP2N18
ZVN1120B	RFL1N20
ZVN1120L	RFP2N20
ZVN1204L	RFP10N12
ZVN1204M	RFM10N12
ZVN1206L	RFP10N12
ZVN1206M	RFM10N12
ZVN1208L	RFP10N12
ZVN1208M	RFM10N12
ZVN1209L	RFP10N12
ZVN1209M	RFM10N12
ZVN1210L	RFP10N12
ZVN1210M	RFM10N12
ZVN1214L	RFP10N15
ZVN1214M	RFM10N15
ZVN1216L	RFP8N18
ZVN1216M	RFM8N18
ZVN1220L	RFP8N20
ZVN1220M	RFM8N20

Industry Replacement Guide

Ultra-Fast-Recovery Rectifiers

Rectifier Type	RCA Replacement Type
BYV32-50	RUR-D810, BYW51-100
BYV32-100	RUR-D810, BYW51-100
BYV32-150	RUR-D815, BYW51-150
BYV32-200	RUR-D820, BYW51-200
BYW29-50	RUR-810
BYW29-100	RUR-810
BYW29-150	RUR-815
BYW29-200	RUR-820
BYW51-50	RUR-D810, BYW51-100
BYW51-100	RUR-D810, BYW51-100
BYW51-150	RUR-D815, BYW51-150
BYW80-50	RUR-810
BYW80-100	RUR-810
BYW80-150	RUR-815
BYW80-200	RUR-820
BYW99-50	RUR-D1610
BYW99-100	RUR-D1610
BYW99-150	RUR-D1615
FE8A	RUR-810
FE8B	RUR-810
FE8C	RUR-815
FE8D	RUR-820
FE16A	RUR-D810, BYW51-100
FE16B	RUR-D810, BYW51-100
FE16C	RUR-D815, BYW51-150
FE16D	RUR-D820, BYW51-200
FE30A	RUR-D1610
FE30B	RUR-D1610
FE30C	RUR-D1615
FE30D	RUR-D1620

Rectifier Type	RCA Replacement Type
MUR805	RUR-810
MUR810	RUR-810
MUR815	RUR-815
MUR1605CT	RUR-D810, BYW51-100
MUR1610CT	RUR-D810, BYW51-100
MUR1615CT	RUR-D815, BYW51-150
SES5401	RUR-810
SES5402	RUR-810
SES5403	RUR-815
SES5401C	RUR-D810, BYW51-100
SES5402C	RUR-D810, BYW51-100
SES5403C	RUR-D815, BYW51-150
SES5601C	RUR-D1610
SES5602C	RUR-D1610
SES5603C	RUR-D1615
UES1401	RUR-810
UES1402	RUR-810
UES1403	RUR-815
UES2401	RUR-D810
UES2402	RUR-D810
UES2403	RUR-D815
UES2601	RUR-D1610
UES2602	RUR-D1610
UES2603	RUR-D1615
VHE1401	RUR-810
VHE1402	RUR-810
VHE1403	RUR-815
VHE1404	RUR-820

Product Profiles

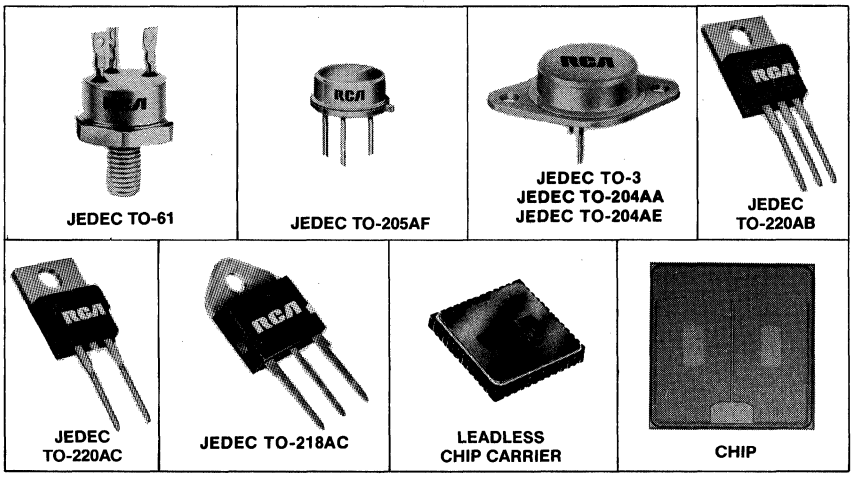
Standard Power MOSFETs

RCA power MOS field-effect transistors offer unique features that make them especially useful in a wide variety of power-switching applications at frequencies up to several hundred kilohertz. Innovative design techniques and advanced processing technology are used to produce these state-of-the-art power switching devices.

The RCA power MOSFET product line includes the standard line of n- and p-channel power MOSFETs, a newly announced line of low-threshold FETs, called logic-level field-effect transistors (or more simply, L²FETs), and a series of conductivity-modulated FETs, called COMFETS, that significantly extend the voltage and current capabilities of the power MOSFET technology. This line of products currently includes more than 250 types supplied in five basic package styles: TO-205AF, TO-220AB/TO-220AC, TO-3/TO-204AA/TO-204AE/TO-204MA, TO-61, and TO-218. RCA multiple-chip power MOSFETs can also be obtained in leadles chip carriers. In addition, power MOSFET chips are available for use in hybrid circuits. Chips may be purchased either in wafer form or as separated die. A coded type number indicates the current and voltage ratings, identifies n- or p-channel types, and specifies the package for RCA power MOSFETs.

Because of its electrically isolated gate, a MOSFET can be described as a high-input-impedance, voltage-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch fast, faster than a bipolar device. But majority-carrier semiconductors also become more resistive as temperature increases. This effect, brought about by a phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) causes the individual cells of the MOSFET to become more resistive at elevated temperatures and, therefore, makes the over-all MOSFET much less susceptible to the on-chip, localized thermal-runaway problems experienced by bipolar devices.

The RCA power MOSFET structure integrates vertical and horizontal geometries to achieve its unique characteristics. RCA's power MOSFETs are manufactured



RCA Power MOSFETs are available as packaged devices and in chip form.

RCA Power MOSFET Nomenclature System

<< EXAMPLE >>

R	F	X	XX	X	XX	L*

RCA — **FET**

PACKAGE
M = TO-3 (METAL)
P = TO-220 (PLASTIC)
L = TO-39 (SHORT LEAD)
K = TO-204AE (60-MIL METAL)

CURRENT
1 = 1A
10 = 10A
15 = 15A
45 = 45A

POLARITY
N = N CHANNEL
P = P CHANNEL

VOLTAGE
05 = 50V
10 = 100V
20 = 200V
50 = 500V

*An "L" suffix is added for Logic-Level FETS.

Note: Nomenclature code does not apply to IRF-Series and JEDEC power MOSFETs.

Standard Power MOSFETs

using the vertical double-diffused process called VDMOS, or simply DMOS. A DMOS MOSFET silicon chip is structured with a large number of closely packed hexagonal cells. The number of cells varies according to the dimensions of the chip. For example, 240-by-240-mil chips contain 25,000 hexagonal cells. The area of each cell is 1000 square microns, and the total packing density may be as high as 113,000 cells (with as much as 7.5 meters of channel periphery) per square centimeter of active area.

The structures of the standard, L^2FET, and COMFET n-channel devices are basically the same. Both the standard power MOSFET and the L^2FET are based on an n^+ substrate, the COMFET on a p^+ substrate. In addition, the COMFET structure includes a median n^+ epitaxial layer. (The reason for this layer is explained in a later section.) The channel regions for all MOSFETs are created by a double (DMOS) diffusion of p and n-type material into the top epitaxial layer of the substrate. A thin oxide then covers these regions.

The industry standard thickness of this oxide, or gate insulator, is 100 nanometers, the oxide thickness used in both standard MOSFETs and COMFETs. In L^2FETs, however, the thickness of this insulator is only 50 nanometers, the chief structural difference between this device and conventional 10-volt MOSFETs, and is the prime reason for lower-voltage gate-drive requirement of the L^2FET.

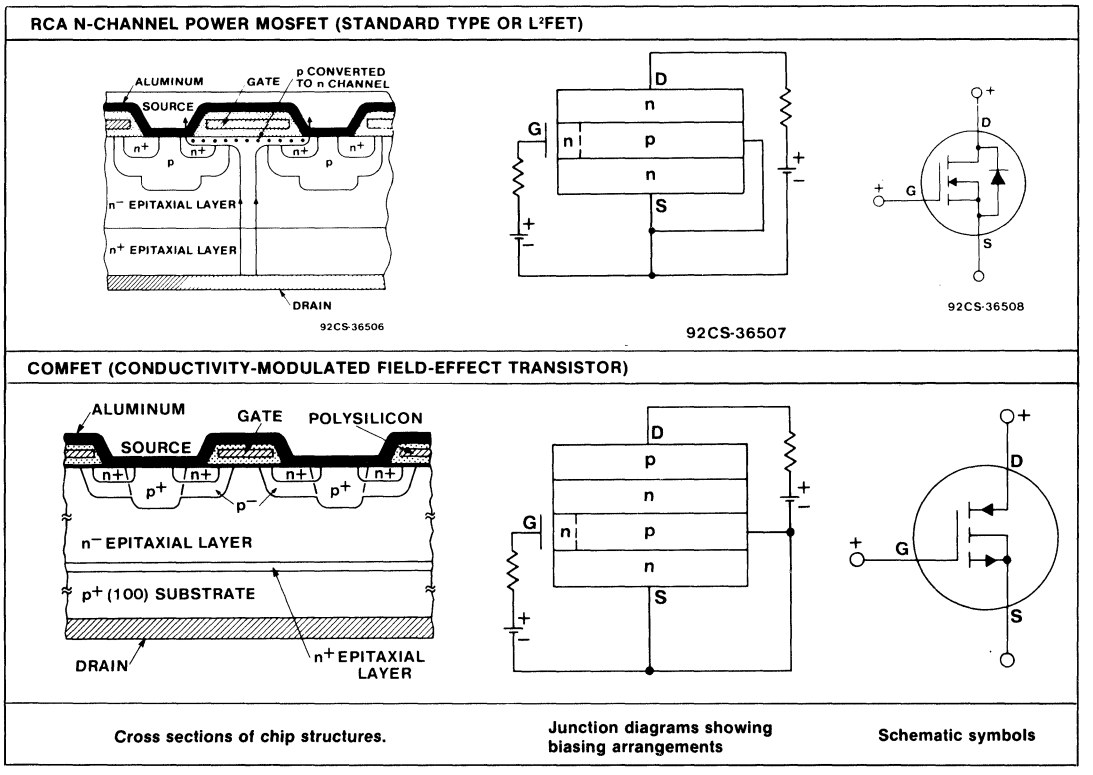
A polysilicon layer is deposited on the oxide. This layer serves as the gate electrode for the device and creates the electric field over the channel. An insulating oxide and glass layer is then deposited over the polysilicon layer. Finally, all the source cells are connected together by a single metallization layer to form the source terminal, and the back side of the chip is metallized to form the drain terminal.

The designs of RCA power MOSFET structures are optimized to achieve simultaneously high voltage, current, and dissipation capability, together with fast switching speeds, on competitively sized chips. The critical considerations are:

1. A low resistance, $r_{DS}(on)$, from the drain to the source.
2. The resistivity and spacings of the silicon layers necessary to assure the required drain-to-source voltage breakdown capability.
3. A uniform gate-to-source threshold voltage.
4. Minimizing the effect of device junction capacitances on switching speed.

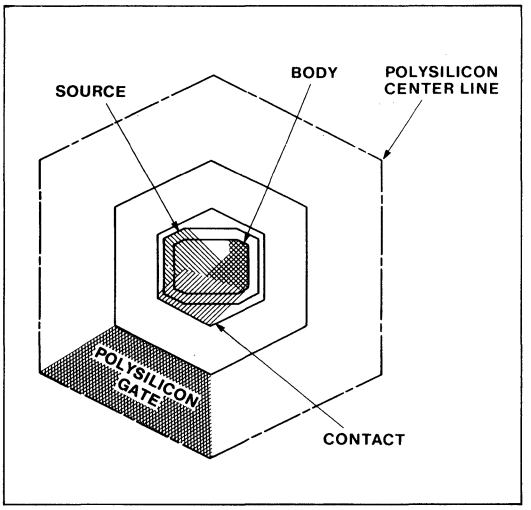
The standard MOSFET and the L^2FET geometries form an inherent diode in an inverse parallel connection. This diode is very useful as the clamp diode in inductive-load switching circuits. The COMFET geometry yields the equivalent of an MOS-gated thyristor circuit except for the presence of the shunting resistance R_s in each unit cell. This resistance has the effect of preventing latching over a wide current and voltage operating range.

The resultant structures feature low leakage currents,



RCA n-channel standard power MOSFET or L^2FET (top) and COMFET (bottom).

Standard Power MOSFETs



Hexagonal unit cell used in RCA power MOSFET chips.

good thermal characteristics (low thermal resistance and excellent thermal stability), large safe-operating areas, and high operating efficiencies.

A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the positive electric charge on the gate converts the p-region beneath the gate to an n-type region. This surface-inversion phenomenon allows current to flow between the drain and source through an n-type material. In effect, the MOSFET becomes an n-n-n device when in this state. The region between the drain and source can then be represented as a temperature-dependent resistor. Detailed explanations of basic design features and key performance characteristics are given in the section "Power MOSFET Technical Overview."

The following paragraphs provide a brief overview of the various categories of products that comprise the RCA line of power MOSFET devices. In addition, the RCA RUR series of ultra-fast-recovery rectifiers, which can frequently be used to advantage in power MOSFET switching circuits, are also described briefly.

RCA power MOSFETs are available in both n and p-channel enhancement-mode types with drain-current (I_{DS}) ratings from 1 to 45 amperes, drain-to-source voltage (V_{DS}) ratings of 50 to 500 volts, and switching times in the nanosecond range. Additional application advantages are offered by exceptionally low drain-to-source on resistances, r_{DS}(on), excellent thermal stability, and safe-operating-area ratings that are limited only by the dissipation capabilities of the devices.

RCA standard power MOSFETs include three groups of devices: The RF series of n- and p-channel types, n-channel types registered with JEDEC (Joint Electron Devices Engineering Council), identified by a "2N" prefix, and the IRF series of devices that are direct replacements for International Rectifier IRF types.

Features

- **Fast switching speeds and low switching losses, both of which are independent of temperature.**
- **No storage time and, thus, no temperature-dependent delay times.**
- **High resistance to thermal runaway.**
- **Simple drive circuitry.**
- **Safe operating area limited only by device dissipation ratings.**
- **Stable gain and switching response over a wide temperature range.**

The RCA IRF series of Power MOSFETs are more than just industry drop-ins! This new series offers the most advanced state-of-the-art technological breakthroughs in design, processing, and electrical features available in the industry today.

- Over 850,000 active hexagonal cells per square inch.
- Process disciplines similar to those of 3-micron QMOS Integrated Circuits.
- 125-MM wafer facility.
- Fully automated wafer transfer and handling capability.
- Fully automated TO-3 and TO-220 assembly line, capable of producing over 10M units per month.
- 100% automated electrical testing of pellet and finished device.
- Plasma-etching of polysilicon and oxide films.
- Direct step on wafer-projection lithography.
- ION implantation (low and high dose).
- Class 100 computer-controlled diffusion room.
- Perform in-line HTRB wafer reliability tests.
- Short-duration accelerated-stress testing, power cycling, bias life.
- AOQ 50 ppm.
- Competitive pricing and delivery (4 to 12 weeks) that's our commitment!
- Power MOSFET spice modeling and applications hot-line (1-800-RCA-APPL)

Logic-Level Power MOSFETs

RCA has developed a new series of power MOSFETs that feature a gate-oxide insulation only 50 nm thick — one-half the industry standard for power MOSFETs. The surface inversion of the MOS channel is a direct function of the gate-oxide thickness; consequently, the gate-to-source threshold voltage — i.e., the applied gate voltage required for uncompromised drain characteristics — on the new series of devices is only half that of conventional power MOSFETs.

The reduced gate-drive requirement allows on-off switching of the new MOSFETs directly from logic-level voltage of 5 volts, rather than the nominal 10 volts required for conventional power MOSFETs with 100-nm-thick gate oxides. For this reason, the new devices are called *logic-level Fets* (or more simply L²FETs). The L²FETs feature the same low on-resistance characteristics, drain-current ratings, and blocking-voltage capability of corresponding types with the higher gate-drive requirements. In addition, the L²FETs offer

Logic Level Power MOSFETs

twice the transconductance and half the threshold-voltage temperature coefficient of conventional types having the same on resistance and voltage ratings and demonstrate a comparable switching speed for the same gate drive power.

The initial series of L²FETs includes 32 n-channel types with drain-current ratings that range from 1 to 15 amperes, drain-to-source voltage ratings of 50 to 200 volts, and are totally interchangeable with corresponding standard power MOSFETs, but offer twice the gate sensitivity.

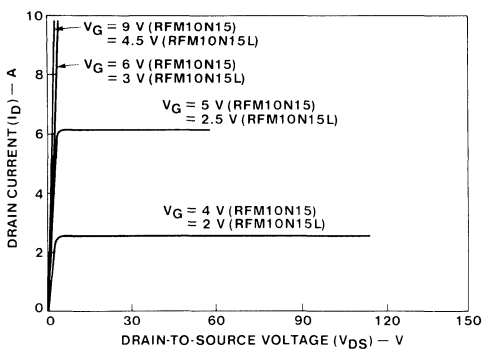
Special Features

- 5-Volt Gate Drive
- Compatible with CMOS, QMOS, TTL, PMOS, and NMOS Logic Circuits
- Compatible with Automotive Drive Requirements

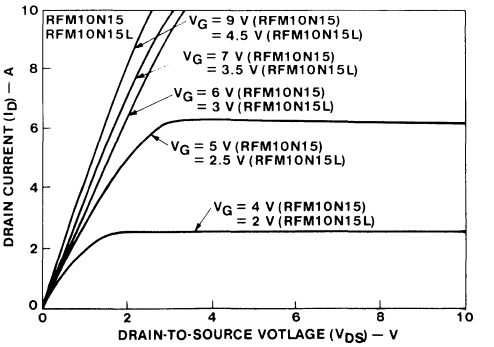
The "Logic-Level," or L², portion of the name for the L²FET MOSFETs reflects their compatability with the 5-volt power-supply requirement of logic circuitry. An L²FET does not require an interface circuit between it and the CMOS logic driver; therefore, the extra cost of the interface circuit power supply is eliminated.

The chief physical structural difference between the L²FET and other MOSFETs, and the electrical reason for its difference in performance, is its gate insulation thickness, which has been reduced from the 100 nanometers standard in the industry to 50 nanometers (500 angstroms), yet which retains the dynamic strength to handle the high voltages applied to power transistors. Since the surface inversion of the MOS channel is determined by the gate-insulator voltage field, the halving of the gate-oxide thickness should be expected to have a major effect on the gate voltage required. In fact, the reduction in gate insulator thickness is the reason for the reduction in voltage to 5 volts from the 10 volts of the standard MOSFET.

Tight control of the temperature-versus-time and oxygen-versus-time profiles applied to the silicon substrate during oxide growth assures consistent L²FET performance through the development of good transition regions between the oxide, the silicon below it, and the polysilicon above it. The reduction in gate insulator thickness makes possible easy on/off control of the L²FETs by CMOS logic alone, and by microprocessors. Yet the on-resistance, drain current rating, and blocking voltage capability are consistent with other RCA MOSFETs.



Drain current as a function of drain voltage for L²FETs and standard MOSFETs at high voltage.

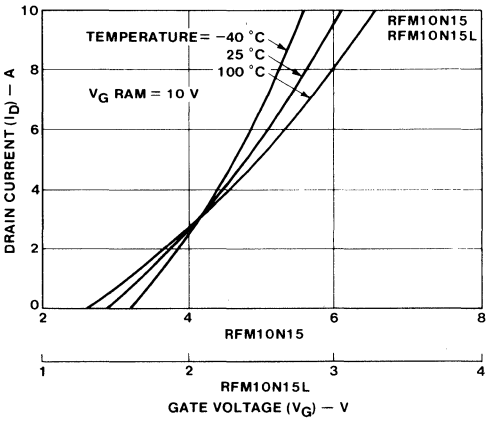


Drain current as a function of drain voltage for L²FETs and standard MOSFETs at low voltages.

Although it might be expected that halving the gate-oxide thickness would double the gate capacitance and halve the switching speed, measurements demonstrate a 2:1 increase in switching speed for the L²FET over the 10-volt MOSFET when gate drive power is the same for both devices. For example, the rise time of a 10-volt MOSFET is typically 120 ns, that of an L²FET, 60ns, even though drain-to-gate feedback capacitance is higher than in the 10-volt type.

A comparison of L²FETs with standard power MOSFETs show that for L²FETs the threshold voltage-temperature coefficient is half that of a standard MOSFET having the same drain-to-source on resistance and voltage rating, the threshold temperature in mV/°C is scaled down, the current level for zero temperature coefficient is unchanged, and that the transconductance is twice that of a standard MOSFET.

A plot of the drain voltage as a function of time of the RFM10N15 standard power MOSFET and the RFM10N15L L²FET, when each is driven with a 5 ampere, 75-volt resistive load line, shows that the rise

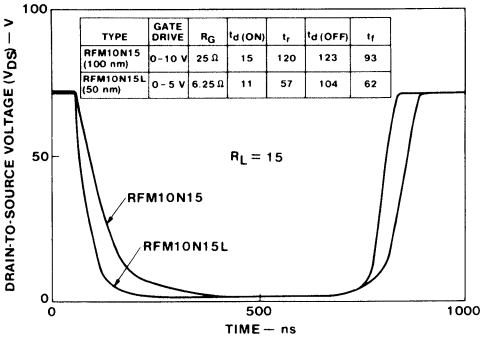


Drain current as a function of gate voltage for L²FETs and standard MOSFETs.

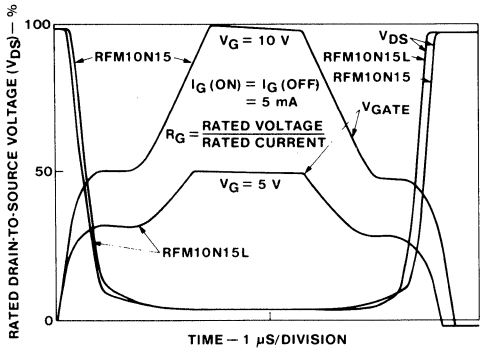
Logic Level Power MOSFETs

and fall times of the devices are not symmetrical, and that the L²FET is faster. Moreover, the dynamic saturation voltage of the L²FET is 4 volts instead of the 8 volts typical of standard MOSFETs.

If the standard MOSFET and the L²FET are both driven from a current generator, where $I_g(on)=I_g(off)$ with gate voltage limits of zero and 10 or 5 volts, the rise and fall times of the devices are the same with current drive, and the two devices have similar output waveforms in most regions.



Drain voltage turn-on waveforms for L²FETs and standard MOSFETs.



Drain voltage switching waveforms for L²FETs and standard MOSFETs.

COMFETs

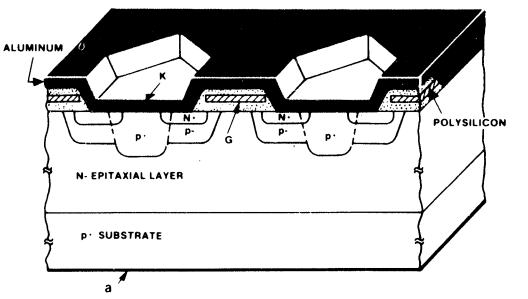
Although vertical MOSFETs have become increasingly important in discrete power-device applications (primarily because of their high input impedance, rapid switching times, and low on-resistance), the fact that their on-resistance increases with increasing drain-source voltage capability has limited their practical value to applications below a few hundred volts. This limitation is effectively overcome in the COMFET or **CO**nductivity **M**odulated **F**ield **E**ffect **T**ransistor, a device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate.

The COMFET operates basically the same as a standard MOSFET and combines the characteristics of a power MOS transistor, a bipolar transistor, and a thyristor in a single device. The COMFET has an exceptionally low on resistance, $r_{DS(on)}$, which permits improved utilization of silicon chip area. This resistance is less than 0.2 ohms for a 0.09 cm^2 chip area, a factor of ten less than that of comparably sized MOSFETs. The on resistance of COMFETs has been measured at less than 0.1 ohm with full drain current, 20 amperes, flowing through the device, and the conductivity-modulated device blocks 400 to 600 volts in the forward direction and 100 volts in the reverse direction. These characteristics combine to make the COMFET an ideal power device for high-voltage, high-power applications.

By modifying the epitaxial structure of the MOSFET and adding recombination centers to the epitaxial drain region, drain-current fall times, t_f, as low as 100 nanoseconds and latching-current values, I_L, as high as 50 amperes with rapid gate turn off have been achieved. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping.

Features
- Low on-state resistance
- Microsecond switching speed
- High input impedance

Applications
- Motor drives
- Power supplies
- Crowbar circuits
- Protective circuits

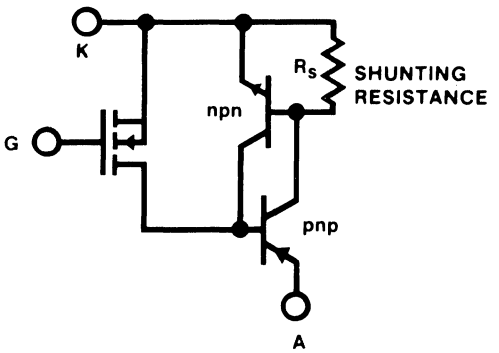


Cross section of COMFET structure

The unique high-voltage, low-resistance characteristics of the COMFET are achieved by use of a p-type substrate on the drain side of a conventional n-channel power MOSFET. When a positive voltage is applied to the gate terminal, electrons enter the n-type drain region and cause a corresponding hole injection into the drain from the p-type substrate. The carriers, or holes, modulate the conductivity of the high-resistance drain and thereby substantially reduce the overall $r_{DS}(on)$ value.

COMFETs

The cross-sectional structure of the COMFET is similar to that of an MOS-gated thyristor, except for the presence of the equivalent shunting resistance, R_S, in each unit cell. The fabrication of the COMFET is like that of a standard n-channel power MOSFET, except that the n^--epitaxial layer is grown on a p^+ substrate instead of an n^+ substrate, and a thin n^+ layer is added.



Equivalent circuit of a COMFET

The heavily doped p^+ region in the center of each unit cell, combined with the aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance R_S. This resistance has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit, so that the individual gains of both the n-p-n and p-n-p transistor equivalents are less than 1, thereby preventing latching over a large operating range of drain voltage, V_D, and drain current, i_D.

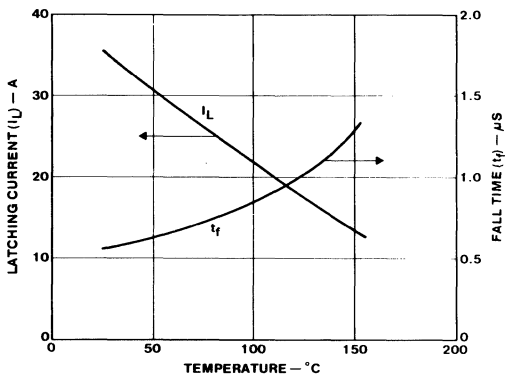
For sufficiently large i_D, emitter injection in the n-p-n transistor increases and is accompanied by an increase in the n-p-n transistor's current gain. When the total gain for both transistors increases to 1, the four-layer device latches. The level of i_D at which this latching occurs is the latching current level, I_L.

The addition of the thin (approximately 10 nanometer) layer of n^+ silicon in the epitaxial structure between the n^- region and the p^+ substrate lowers the gain of the equivalent p-n-p and allows a greater range of i_D without latching. A reduction in the current gain of the p-n-p equivalent corresponds to an increase in I_L; in fact, the added n^+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in I_L by a factor of 2 to 3.

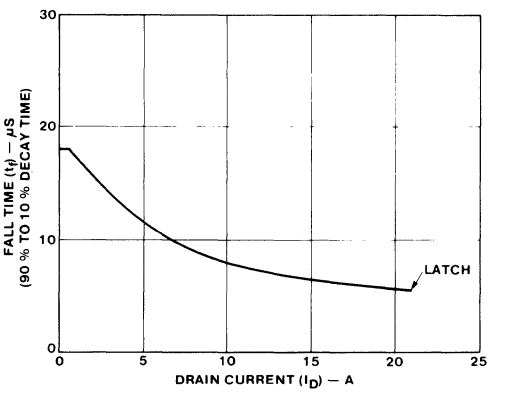
There is also a reduction in fall time, t_f. The COMFETs can block the high voltage only in the forward voltage direction since the emitter junction (p^+-n^+) of the p-n-p equivalent transistor breaks down at a low level when the polarity of the applied voltage is reversed. The smallest values of t_f that have been obtained for COMFETs are in the range of 100 to 200 ns.

The reduction in minority-carrier lifetime that allows faster switching in a COMFET also carries with it a penalty: higher forward voltage drop when the device is turned on, i.e., higher on-resistance. Clearly, there is a tradeoff involved, and the optimum choice of a value for t_f and the corresponding on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100ns), the on-resistance value of 0.2 ohms is, again, approximately ten times less than that of a comparably-sized n-channel MOSFET.

Because power devices are often operated at elevated temperatures, it is important to determine how their performance varies with temperature. A plot of the variation of t_f and I_L for a COMFET as a function of temperature in the range of 25° C to 150° C shows that t_f increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval of 25° C to 150° C.



Variation in drain-current fall time t_f and latching current I_L as a function of temperature.



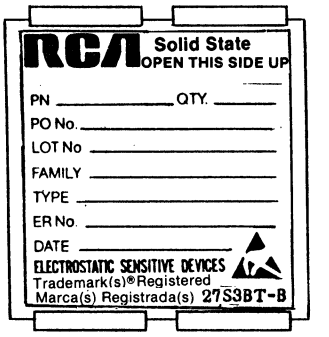
Drain current fall time as a function of drain current magnitude.

High-Reliability Power MOSFETs

RCA has developed an aggressive program to quality power MOSFETs to MIL-S-19500. This plan includes qualification to the TXV level. This program has two parts, (a) a plan to quality RCA devices to existing QPL specifications, and (b) a plan to propose new QPL types to fill "product holes" in the existing MIL type matrix.

Also, in the plan are seven additional RCA candidates for types already on the QPL, four original RCA QPL submissions on 60-volt N-channel types, four P-channel 100-V types and six logic-level N-channel types for 60-V, 100-V, and 200-V applications.

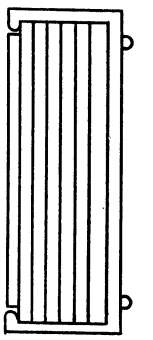
In addition to planned QPL types, RCA will offer high-reliability custom selections of all hermetic Power MOSFETs.



Power MOSFET Chips

RCA offers power chips in three (3) different form factors:

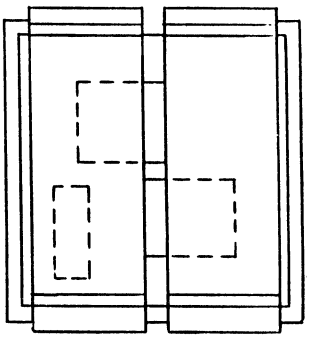
Suffix Letter	Form Factor Definition
H	Chips: Individual test-accepted chips.
W	Unsawed Wafer: Wafter not sawed; 100% tested; reject chips are inked out for easy identification.
WS	Sawed Wafer: Wafer completely sawed after mounting on tape; 100% tested; rejects are inked out for easy identification.



Specify the proper suffix letter when ordering as follows:

Order Option	Example
Chip	PCF2N08H
Unsawed Wafer	PCF2N08W
Sawed Wafer	PCF2N08WS

All quoted and stated prices are per chip regardless of form factor. Actual shipments may vary ±5% of purchase order quantity. Shipments will conform to RCA Terms and Conditions found at the end of this booklet.

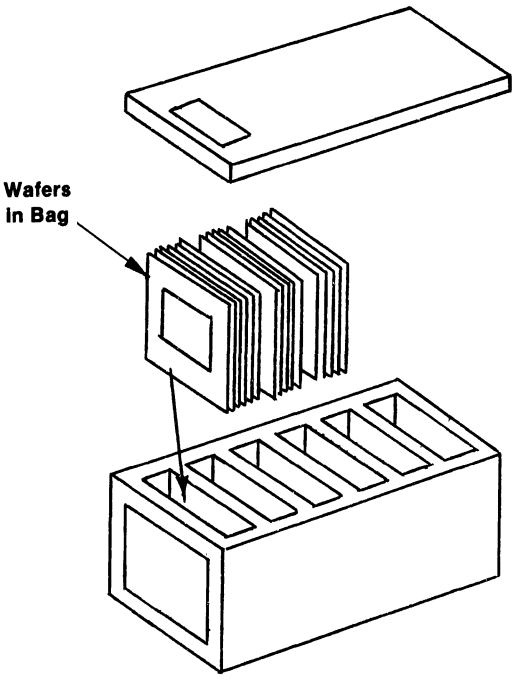


RCA chips and wafers are packed in protective enclosures to assure reliability.

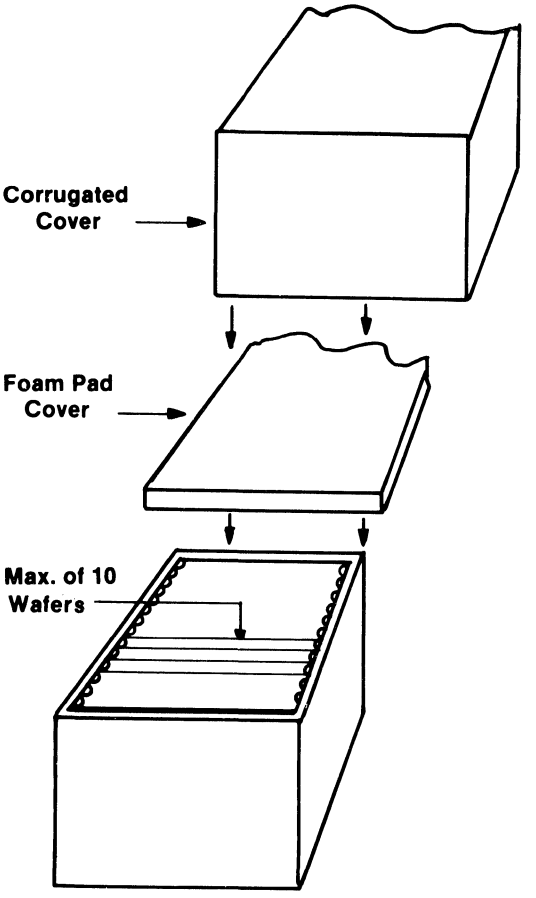
A. **Chips** — H Suffix
Chips are packed in 2" x 2" (waffle pack) trays in which the chips are placed in individual pockets for easy use. The number of chips per tray depends upon the chip size and may be anywhere from 36 to 400. The trays are provided with covers and sealed in plastic bags.

Power MOSFET Chips

B. **Unsawed Wafers** — W Suffix
Unsawed wafers are placed in wafer holders (fitting in depressions), provided with covers, and sealed in plastic bags.



C. **Sawed Wafers** — WS Suffix
Unsawed wafers are mounted on tape and then sawed. The sawed wafers are placed in sealed plastic bags.



Electrical Parameters — RCA 100% electrical tests each chip on each wafer to the electrical tests specified in the Technical Data section under the individual RCA power chip device type number. All rejects are inked out. Product is guaranteed to an LTPD of 10%.

Visual Inspection — RCA 100% visually inspects each chip on each wafer in accordance with the chip visual inspection criteria of MIL-STD-750, Test Method 2072. All rejects are inked out.

Ultra-Fast-Recovery Rectifiers

The latest state-of-the-art processing technology is employed in the manufacture of the new series of RCA ultra-fast-recovery (35-ns) rectifiers. The cathode region is created by the growth of an n^- epitaxial layer onto a low-resistivity n^+ substrate. The anode region is formed by ion implantation and high-temperature diffusion. Aluminum metal on the anode provides for aluminum wire bonding. Trimetal (aluminum-titanium-nickel) evaporated onto the cathode surface provides cathode metallization for high-temperature solder mounting.

Modern planar technology is used to form the edges of the rectifier structure. The structure features an n^+ "channel stopper," an evaporated metal field shield, and an ion trap to assure reverse-bias stability. The p-n junction is insulated by a silicon-dioxide ($Si0_2$) layer. A phosphorous-doped silicon-glass overcoat provides mechanical protection during assembly.

The resultant structure features low forward voltage drops, excellent bias stability, low dissipation, and very short reverse-recovery times (less than 35 ns).

RCA ultra-fast-recovery rectifiers incorporate several construction features that are ideal for mounting the rectifier pellets in hybrid circuits, as follows:

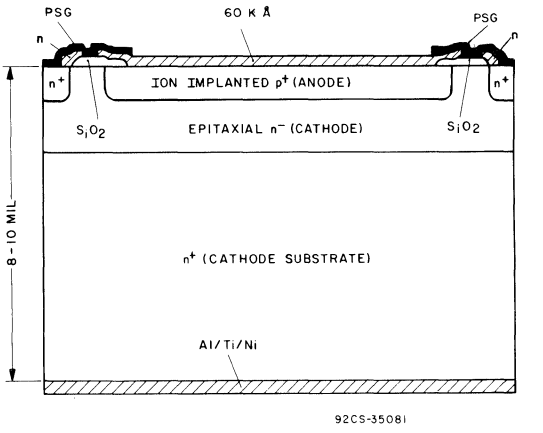
- The trimetal cathode metallization is particularly suited for high-temperature solder mounting. (A eutectic solder bond formed with 95/5 lead-tin solder at a temperature of 320°C is recommended.)
- The aluminum anode metallization facilitates aluminum wire bonding.
- The glass-passivated planar structure assures excellent mechanical protection during processing.
- Large bonding surfaces (3600 $mils^2$ on 8-ampere types, 10,000 $mils^2$ on 15-ampere types) are available.

RCA ultra-fast-recovery rectifiers offer several important benefits for use in high-speed power-switching circuits. These benefits include:

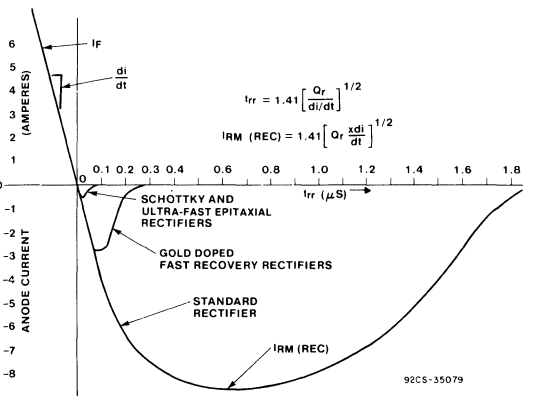
- Decrease in the short-circuit energy that impinges on the power switches
- Less RFI generation in the rectifier filter system
- Reduction in, or elimination of, the RC damping networks frequently required with Schottky and ordinary fast-recovery rectifiers
- Dissipations that are 20 to 30 percent less than those in ordinary fast-recovery rectifiers
- Breakdown voltages three to five times greater than those of Schottky rectifiers

The RUR series of ultra-fast-recovery rectifiers feature a passivated epitaxial structure that combines the advantages of fast switching speed, low forward-voltage drop, good breakdown capability, and wide operating temperature range. The low stored charge and attendant fast reverse-recovery behavior of these rectifiers minimize electrical noise generation and, in many circuits, markedly reduce the turn-on dissipation of associated power switching transistors. These attributes make RUR-series types excellent choices for use in switching power supplies.

Thin anode and cathode regions in the RUR series of RCA ultra-fast-recovery rectifiers limit the build up of excess charge during forward conduction. Gold doping causes this minimal charge to be dissipated quickly during the recovery period so that the recovery time of RUR-series rectifiers is comparable to that of Schottky rectifiers.



Planar, high-speed, glass-passivated pellet structure used in RCA ultra-fast-recovery rectifiers.



Relative reverse-recovery-time (t_{rr}) characteristics of various rectifier structures. Curves show the excellent recovery behavior of the RCA ultra-fast epitaxial structure.

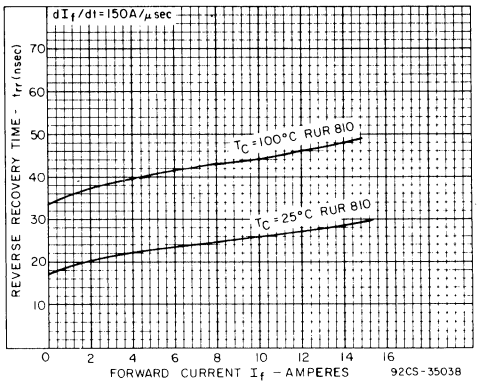
Precise manufacturing control of the anode and cathode vertical structure makes possible low forward-voltage drops — typically less than 0.9 volt at the rated current — significantly lower than those of conventional high-voltage fast-recovery rectifiers.

The vertical structure used in RCA ultra-fast rectifiers is optimized for high-speed switching capability, achieved as a tradeoff against reverse-voltage breakdown capability. As a result, the ultra-fast-recovery series are suitable for use as output rectifiers in 100-kHz switching power supplies that provide outputs of 5 to 48 volts. Despite the trade-off for switching speed, the RUR-series rectifiers have a breakdown capability three to five times greater than that of Schottky rectifiers with similar recovery times.

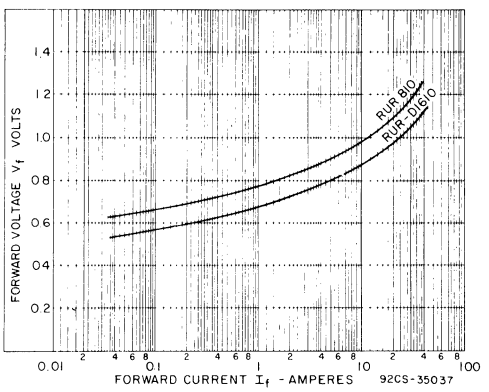
The low forward voltage drop of the ultra-fast-recovery rectifiers permit safe operation of these devices at case temperatures of 125°C at the rated average forward current. At this case temperature, the RUR-810 series rectifi-

Ultra-Fast-Recovery Rectifiers

ers can operate safely at average currents up to 8 amperes or at peak currents up to 16 amperes in an output circuit with a 50 per cent duty cycle.

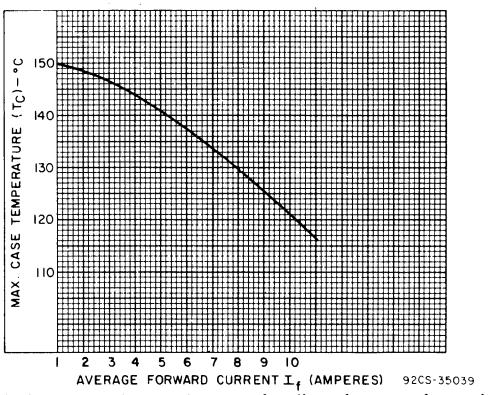


Typical reverse-recovery-time as a function of forward current.



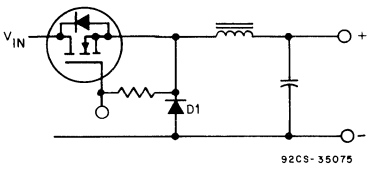
Maximum forward voltage as a function of forward current.

Reverse-recovery-time (t_{rr}) measurements are, to some extent, dependent upon the circuit configuration in which the measurement is made and the level of current from which the device must recover. The test-circuit configuration and the test method used in the recovery measurements on the RCA ultra-fast-recovery rectifiers assures realistic current levels and various rates of change of current (-di/dt).

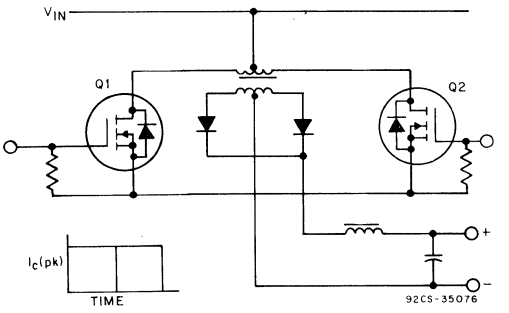


Maximum case temperature as a function of average forward current.

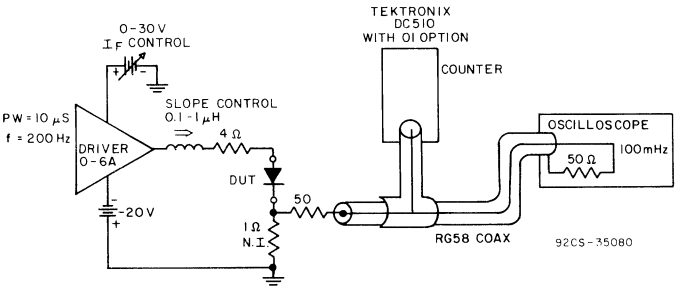
Circuit Examples



Buck-type Switching Regulator



Push-Pull Converter



Test circuit used for reverse-recovery-time measurements.

Handling Precautions for Power MOSFETs

Insulated-Gate Field-Effect Transistors (MOSFETs) are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling a MOSFET, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no damage problems due to electrostatic discharge.

MOSFETs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive materials such as "ECCOSORB* LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hands being used should be grounded by any suitable means — for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. Gate Voltage Rating — Never exceed the gate-voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.
6. Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.
7. Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. If gate protection is required an external zener is recommended.

*Trademark Emerson and Cumming, Inc.

Power MOSFET Technical Overview

Performance Characteristics

RCA power MOSFETs operate with very high efficiencies and modest drive requirements at switching frequencies up to several hundred kilohertz. At the lower frequencies, they can be driven directly from the signal levels of CMOS and other logic integrated circuits.

Switching losses in power MOSFETs are independent of temperature, and a major contributor to thermal runaway is thereby eliminated. The on-resistance in power MOSFETs has a positive temperature coefficient so that localized "hot spots" are defocused; the devices, therefore, can be readily operated in parallel with the need for costly compensating and balancing techniques substantially reduced.

The published data on RCA power MOSFETs fully characterize these devices with respect to the maximum stresses that they can safely withstand and the performance levels they are expected to achieve.

Characteristics data for RCA power MOSFETs are based on the determination of the inherent qualities and traits of the device. These data, which are usually obtained by direct measurements, provide information that a circuit designer needs to predict the performance capabilities of his circuit and form the basis for the ratings that define the safe operating limtis of the device.

Drain-to-Source On Resistance, $r_{DS}(on)$

The multiple-cell construction used in RCA power MOSFETs substantially reduces the resistance from drain to source when the device is in the on state. The on resistance $r_{DS}(on)$, of the standard MOSFET and L^2FET devices, which is specified at one-half the rated drain current, typically range from 0.04 ohm for a 60-volt, 6-by-6-mm chip to 20 ohms for a 500-volt, 1.5-by-1.5-mm chip. When $r_{DS}(on)$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, r_N, to the total resistance. An individual cell has a fairly high resistance, but to minimize $r_{DS}(on)$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS}(on)$ value:

$$r_{DS}(on) = r_N/N \qquad (1)$$

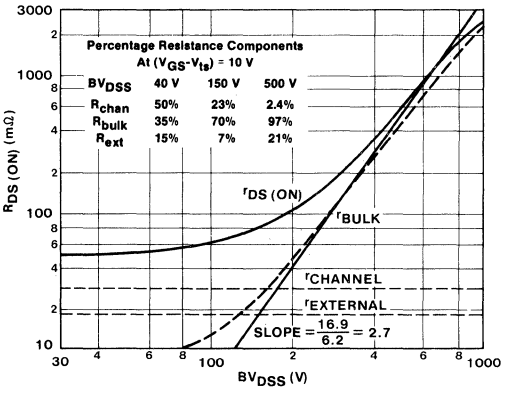
where N is the number of cells.

In reality, $r_{DS}(on)$ is composed of three separate resistances. The value of $r_{DS}(on)$ at any point on the curve is found by adding the values of the three components at that point:

$$r_{DS}(on) = r_{bulk} + r_{chan} + r_{ext}$$

where r_{chan} represents the resistance of the channel beneath the gate, and r_{ext} includes all resistances resulting from the substrate, solder connections, leads, and the package. r_{bulk} represents the resistance resulting from the narrow neck of n material between the two p layers, plus the resistance of the current path below the neck and through the body of the device to the drain.

The resistances r_{chan} and r_{ext} are completely independent of voltage, while r_{bulk} is highly dependent on applied voltage. Below about 150 volts, $r_{DS}(on)$ is dominated by the sum of r_{chan} and r_{ext}. Above 150 volts, $r_{DS}(on)$ is increasingly dominated by r_{bulk}. Obviously, $r_{DS}(on)$ must increase with increasing breakdown-voltage capability of a MOSFET or chip size must be increased to accommodate more cells.



Three resistive components contribute to over-all value of the on resistance $r_{DS(on)}$.

Use of CAD Techniques to Optimize Power MOSFET Design

An RCA-developed computer program is used to optimize the many variables involved in the design of the hexagonal MOSFET chip. (See sample program results in highlighted box.) This optimization must be consistent with practical tradeoffs of tolerances, processing yields, and other factors. Accordingly, the computer-aided-design (CAD) techniques employed are reviewed continuously as new processing equipment and techniques become available. In this way, the end-user is assured that state-of-the-art products will always be available.

On-Resistance Calculations — The on-resistance is a complex function of many contributing resistances. All computer calculations of the total on-resistance quantity are carried out at zero drain voltage in order to obtain a meaningful result.

Wire resistance and substrate resistance are usually small, typically in the order of 5 per cent of the over-all total. The metal resistance used in the calculation of on-resistance is a lumped-constant approximation in which certain assumptions are made relative to the placement of the source pad and the size of the wire-bond "foot print." Provisions are included for multiple source pads.

The channel resistance, which consists of several parts, has a complex effect on the on-resistance calculation. The first part consists of the metal channel length provided by the body lateral diffusion and bounded by the source and epitaxial regions. In this part, the surface concentration varies by one or more orders of magnitude and results in a graded threshold voltage along the length of the channel. The second includes the added channel length that results from the zero-bias depletion width. For high-voltage devices, the depletion-width channel-resistance component may exceed the diffused-channel resistance component. The third part of the channel resistance is a distributed portion that is attributable to the combination of the lateral current through the accumulation beneath the gate in the "neck" region and the vertical current in this same region. Finally, a fourth component results solely from the resistance of

Performance Characteristics

RESULTS OF OPTIMIZING PROGRAM FOR MOSFET

VOLTS	= 165.	DIE MILS	= 120.	EDGE MILS	= 8.9	WIRE MILS	= 10.0
PAD W.D	= 4.00	PAD H/D	= 2.00	SOURCE PADS	= 1.00	METAL MICR	= 4.00
P+ P-	= 1.50	N+/P-	= 0.250	UP/P-	= 0.375	SUB OHM-CM	= 0.150
SUB MILS	= 12.00	RHO NECK/EPI	= 1.000	MOBILITY	= 400.	CHANNEL TYPE	= 1.
POLY HEX MIC	= 22.40	DIELECTRIC	= 4.00	GATE VOLTS	= 10.00	THRESHOLD V	= 3.00
CELL PITCH	= 36.30	P- DEPTH MIC	= 4.00	GATE ANGS	= 1000.		

ON RESISTANCE (OHMS x 0.001)	= 195.702	= 100.00%	P+ DEPTH	=	6.00
WIRE RESISTANCE	= 2.820	= 1.44%	N+ DEPTH	=	1.00
SUBSTRATE RESISTANCE	= 6.485	= 3.31%	UP DIFFUSION	=	1.50
METAL RESISTANCE	= 2.355	= 1.19%	CHANNEL LENGTH	=	2.40
DIFFUSED CHANNEL RESISTANCE	= 44.038	= 22.50%	0 VOLT DEPLETION	=	0.85
0 VOLT DEPLETION CHANNEL	= 11.663	= 5.96%	EPI RESISTIVITY	=	2.59
DISTRIBUTED NECK RESISTANCE	= 33.128	= 16.93%	NECK RESISTIVITY	=	2.59
EPITAXIAL RESISTANCE	= 95.293	= 48.69%	EPI THICKNESS	=	17.21
(LATERAL NECK RESISTANCE)	= 24.629		NUMBER OF CELLS	=	5001.
(VERTICAL NECK RESISTANCE)	= 24.787		ACTIVE SQUARE CM	=	0.05528
V PINCH (VOLTS)	= 18.5		EDGE EFFICIENCY %	=	72.5
CAP. G TO D(INT) PF	= 1101.9		PAD EFFICIENCY %	=	84.7
SWITCH TIME (APPROX) AMP NSEC	= 20.410		POLY SQUARE CM	=	0.03423
			POLY EDGE CM	=	38.8

Typical design chart for optimization of $r_{DS(on)}$. This chart represents one of many design possibilities. The top of the chart lists 23 input possibilities. The 13 parameters in the lower left column are expected electrical characteristics consistent with the inputs, and the 14 parameters in the lower right column are physical characteristics.

the epitaxial material. This component is usually larger than one would expect because the current is confined by the device geometry.

Metal contact resistances, package lead resistances, and the resistance of the nonmetallized source silicon material are neglected in the on-resistance calculation.

Equivalent-Model Analyses — At low current levels, the accumulation layer beneath the gate, in effect, becomes a source for a depletion-mode vertical junction field-effect transistor (J-FET), and the neck becomes most of the J-FET channel. The body serves as the J-FET drain. As drain voltage is applied, the depletion channel and the depletion layer adjacent to the body both lengthen; at a sufficiently high voltage, this vertical J-FET may pinch off. The equivalent J-FET model, in essence, is the key to understanding the hexagonal power MOS/FET design. This cascode configuration clearly demonstrates that most of the drain voltage is supported by the J-FET. CAD programs are used to predict pinch-off voltages for the analyzed structure.

Further study of the cascode equivalent model reveals that the dominant factors in the determination of switching speed are gate drive current, gate-to-J-FET-source capacitance (Cx), and pinch-off voltage of the J-FET. All other capacitive effects are buffered by the cascode circuitry provided drain current is present. CAD techniques are used to optimize for the required capacitance-frequency relationships.

Excellent agreement exists between the parameters calculated from the computer model and measurements on finished devices.

Breakdown Voltage

Both low- and high-voltage designs have shields for the source field (to minimize the peak electric field in this region) and the drain field (to terminate the electric field within the n-type material). The high-voltage design includes a diffused guard ring that assures a more even distribution of the drain voltage and thereby reduces the peak electric field. The edges of the MOSFET structure are designed so that a uniform bulk breakdown occurs under the active area instead of at the edge. The power density at voltage breakdown is, therefore, reduced, and device reliability is improved.

Because the on resistance of a standard MOSFET must increase with increasing drain-source voltage capability, these devices are commonly used in applications up to 500 volts. The COMFET, in which the conductivity of the n-type expitaxial drain region is greatly increased (modulated) by the injection of minority carriers from the p-type substrate offers significant advantages in $r_{DS(on)}$ at higher voltage levels. However, a trade off is involved and the on resistance depends to some extent on other factors dictated by the intended application. However, even for the shortest switching times (100 nanoseconds), the on resistance value of 0.2 ohms is approximately a factor of ten less in the COMFET than in a comparably sized standard n-channel MOSFET.

Gate Voltage

To permit the flow of drain-to-source current in an n-channel MOSFET, a positive voltage must be applied between the gate and source terminal. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

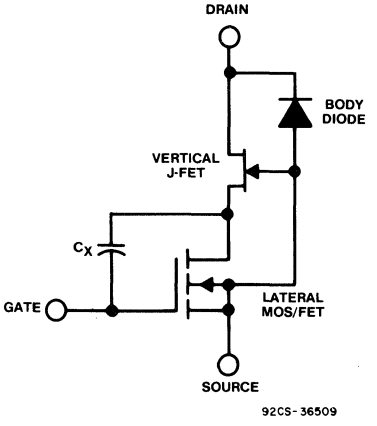
The basic input circuit of a MOSFET can be represented by an equivalent resistance and capacitance. The capacitance, called C_{iss} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

Gate Threshold Voltage, $V_{gs}(th)$ — When considering the V_{gs} level required to operate a MOSFET, the device is not turned on (no drain current flows) unless V_{gs} is

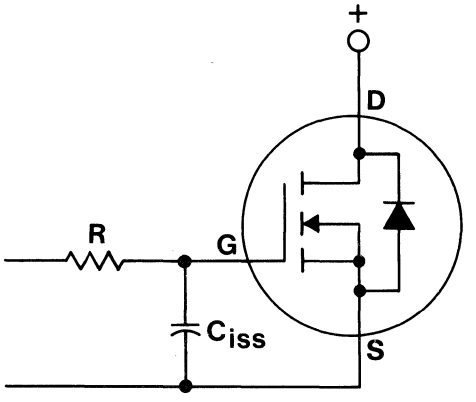
Performance Characteristics

greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally, V_{gs} for standard power MOSFETs is at least 2 volts. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate. The gate-drive circuit must provide at least the threshold-voltage level but, preferably, a much higher one.

The gate threshold voltage is determined on the basis of relative diffusion profiles of the source and the drain required for the body concentration that must be inverted. In addition, the diffusion from the points of the hexagon, the gate-oxide thickness, and the drain-neck resistivity must be optimized to assure a voltage threshold in the range of from 2 to 4 volts. For L²FETs, this range is reduced from 1 to 2 volts.



Computer equivalent model of RCA power MOSFET consists of cascode connection of vertical J-FET and horizontal MOSFET.



Basic power MOSFET input circuit.

On-State Gate Voltage, V_{gs}(on) — The halving of the gate-oxide thickness in the L²FET, as compared with the standard 10-volt MOSFET and COMFET types, reduces the threshold voltage of the L²FET by a factor of two over the other devices. Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, the reduction of the gate insulator thickness from 100 nanometers to 50 nanometers in the L²FET also halves the applied gate drive voltage required for the L²FET to sustain the same drain characteristics as the standard 10-volt and COMFET devices.

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has higher gate resistance. This property accounts for the frequent use of metal-gate MOSFETs in high-frequency (greater than 20 MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from data-sheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20 ohms per square. But whereas the total R value is not found on data sheets, the C value (C_{iss}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{iss} is closely related to chip size; the larger the chip, the greather the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1 to 10 MHz.

Device Capacitances

Power MOSFETs are majority-carrier devices and are, therefore, innately capable of high-speed switching. However, this switching capability is limited by the charging and discharging time of the gate-to-source capacitance C_{GS} and the gate-to-drain capacitance C_{GD}. In RCA power MOSFETs, the gate-to-source capacitance is reduced by minimizing the polysilicon area of the gate and by controlling the oxide dielectric under all gate- and source-pad runners. The resistance of the gate is minimized by close control of the doped polysilicon and by use of metallized gate runners.

Measurements of the switching speeds of the L²FET devices indicate that the 50% reduction in gate oxide thickness, compared with standard MOSFETs and COMFETs, produces approximately a 2:1 increase in switching speed for any given value of gate-drive power.

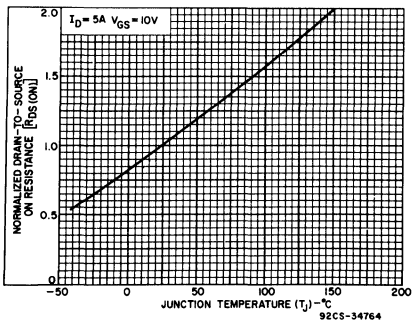
Thermal Stability

The "hot-spotting" phenomenon, manifest in bipolar transistors by the localized high temperatures that can result from the tendency of current to concentrate in areas around the emitter, a phenomenon that can lead

Performance Characteristics

to device failure from the mechanism of thermal runaway, is not a factor in MOSFET operation because the current flow in these devices is in the form of majority carriers. The mobility of majority carriers is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slow down as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance. The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that when MOSFETs are operated in parallel and any device begins to overheat, its resistance increases and its current is directed away to cooler chips.

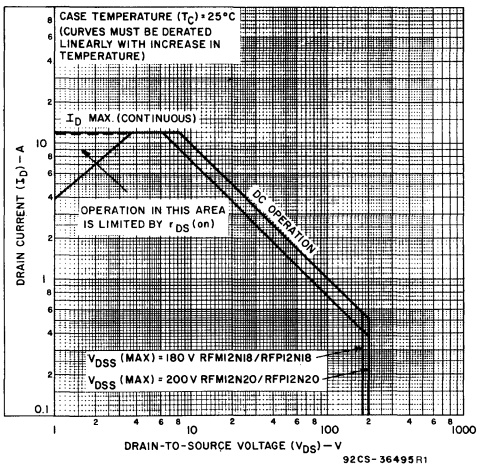


Normalized drain-to-source on resistance $r_{DS(on)}$ as a function of junction temperature.

The positive temperature coefficient of the MOSFET on resistance is a result of the proximity of the channel region to the gate. A bias on the gate can pull additional mobile charge carriers into the channel and, in this way, control the resistance and, in turn, the current in this region. However, carriers in this section are all of a single polarity, and the concentration of these carriers, which is primarily a function of the gate bias, is essentially independent of temperature. Therefore, the temperature coefficient of the on resistance is positive over the entire length of the current path, and the current always tends to defocus away from hot spots.

Safe Operating Area

The differences in the thermal characteristics of MOSFETs and bipolar transistors result in a fundamental difference in the safe-operating areas of these devices. Both types of device are limited only by thermal dissipation considerations when operated at high current and low voltage. In the high-voltage/low-current region of the safe-operating area, the positive-temperature-coefficient portion of the current path in bipolar transistors cannot counterbalance the negative-temperature-coefficient portion of the current path, which is higher in this region. Therefore, bipolar transistors must be derated more rapidly to avoid the high current concentration that may lead to second breakdown. In RCA power MOSFETs, the total current path has a positive temperature coefficient of resistivity, and the MOSFETs are rated for a constant thermal-dissipation limit over the entire area defined by the maximum current and voltage ratings.



Safe-operating-area curve for an RCA power MOSFET.

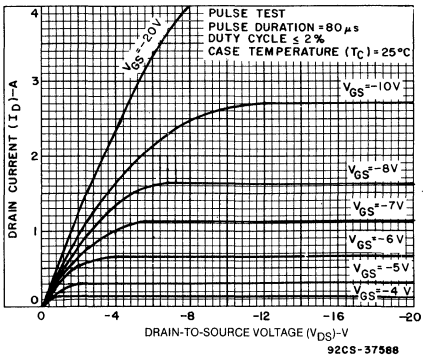
Output Characteristics

Probably the most used MOSFET graphical data is the output characteristic or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic shows the drain current, at various V_{DS} values, as a function of the gate-to-source voltage (V_{gs}). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

A standard power MOSFET must be driven by a fairly high voltage, on the order of 10 volts, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage level unless they are modified with external pull-up resistors. Even with a pull-up to 5 volts, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of 10 volts, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering

Performance Characteristics

chips are inserted between the IC output and gate input to match the needs of the MOSFET gate. Of course, this limitation is eliminated with the use of the L^2FET.



Typical output characteristic for an RCA power MOSFET.

Switching Characteristic's

A Power MOSFET is usually considered as a gate-voltage controlled device. In reality, an appreciable current must be provided in order to switch the device. In measurements of the switching characteristics of RCA power MOSFETs, the gate current is used as the input parameter.

A family of curves is presented for a constant load resistance with V_{DD} varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts (0 and 5 volts for L^2FETs). This new format is a plot of drain voltage and gate voltage as a function of normalized time. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

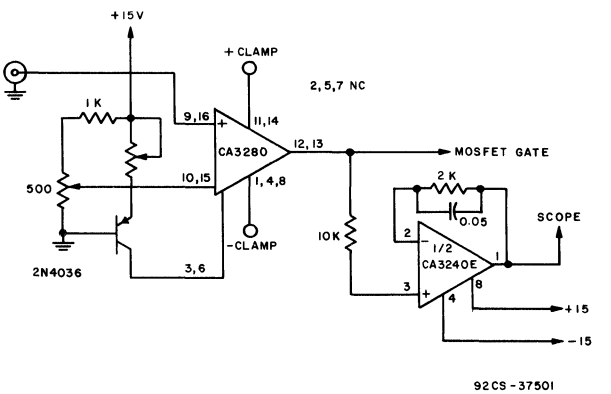
Test Circuit — The heart of the switching-time test circuit is an RCA CA3280 integrated-circuit operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The CA3280 is actually two OTA's in parallel.

A value of I_{ABC} is established from the collector of a 2N4036 transistor. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approx. a0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large, resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. These supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET (0 volts and +5 volts for L^2FETs). The behavior of the CA3280 IC is excellent from submicroamperes to about 2-1/2 ma. Higher current may be achieved by stacking many CA3280 packages atop one another and soldering the leads to parallel the chips rather than wiring many sockets. This arrangement may require an increase in the bypass capacitor values.

An RCA CA3240E BiMOS input op amp is used as a unity-gain follower. Otherwise, the 1-megohm or 10-megohm shunting impedance of the scope would load the high-impedance circuitry associated with the MOSFET gate.

Test Conditions and Waveforms — The input test signal applied to the CA3280 OTA is supplied by a pulse generator set for an on-time duration of 50 μs and a repetition rate of approximately 25-ms (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.

With a low value of drain supply voltages, the gate voltage is observed while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several microseconds exists at the + 10-volt level (+ 5-volt level for L^2FETs). Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased



Test circuit used to measure switching characteristics of RCA power MOSFETs.

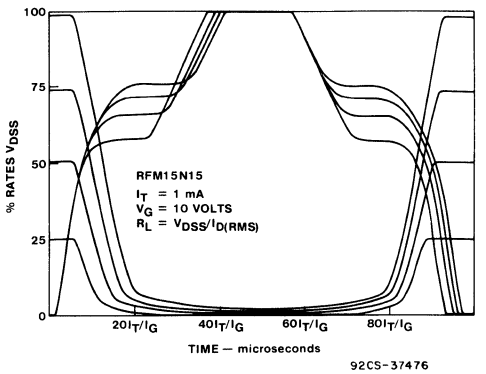
Performance Characteristics

to the maximum rate value.

There are some features of the gate and drain voltage waveforms which should be noted.

1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time.
   Exceptions occur for very fast or very slow switching, and for non-symmetrical current drive.
2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the gate and drain voltage curves above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS(on)}$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

Family of Characterization Curves — The published switching data on RCA power MOSFETs include a family of gate and drain voltage curves in which the drain supply voltage is fixed at four values. The ordinate is 10 volts (5 volts for L²FETs) full scale for the gate voltage and is normalized to 100% of the maximum rated drain-voltage curves. All four sets of



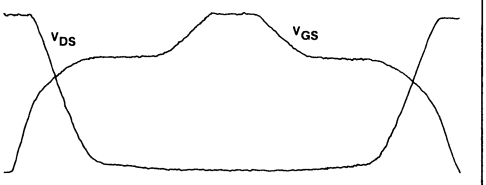
Family of switching-characterization curves for an RCA power MOSFET.

curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_G) microseconds full scale, where I_G is the actual gate drive current. With this family of characteristic curves, switching behavior may be readily predicted for almost any driving circuit provided the load is resistive.

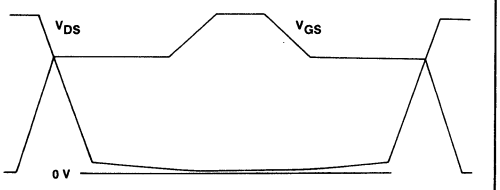
Characterization-Curve Limits — The gate and drain voltage switching waveforms can be scaled in an inverse manner with gate current. This scaling shows that the switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. The characterization, however, is valid over many decades of gate current so that all but a very few applications can be described by the family of switching characterization curves.

Input test signal applied to CA3280 (2 volts peak).

Power MOSFET gate-current waveform (±1 mA).



Power MOSFET gate voltage (10 volts peak) and drain voltage (150 volts peak-to-peak) waveforms.



Linear approximation of power MOSFET gate- and drain-voltage waveforms.

Test waveforms for measurement of switching characteristics of standard power MOSFETs. (Time base for waveforms is 100 microseconds full scale.)

Asymmetrical Current Drive — The positive and negative gate drive will often be dissimilar. The scaling of course must reflect this condition. At other times, the gate current varies with amplitude. This is always true when driving from a pulse generator of fixed resistance. Piece-wise linear methods will yield the gate current, which will permit the proper piece-wise linear scaling. This could be done in the following manner:

1. Mark eleven small x's along the gate waveform, dividing it into 10 equal voltage segments; for example, V_S = 0, 1, 2, . . . 9, 10 volts.

Performance Characteristics

2. Draw a vertical line through each X the full height of the gate waveform, creating 10 time segments.

3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, the piece-wise linear gate current for each time segment can be calculated, I_{g1} = (10-0.5)/100 = 95 mA, I_{g2} = (10-1.5)/100 = 85 mA, etc.

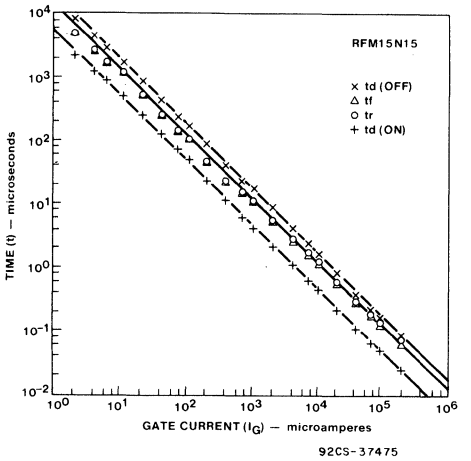
4. Then each waveform is scaled within the pertinent time segment by the proper gate current.

5. Smooth the curves.

6. Create 10 more time segments for the right half of the gate waveform corresponding to an average gate voltage of 9.5, 8.5, . . . 1.5, 0.5 volts. Call these segments 11, 12, . . . 19, 20.

7. In that the pulse-generator voltage is now zero volts, calculate I_g as:
   I_g11 = (0-9.5)/100 = -95 mA, I_{g12} = (0-8.5)/100 = -85 mA, etc.

8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.



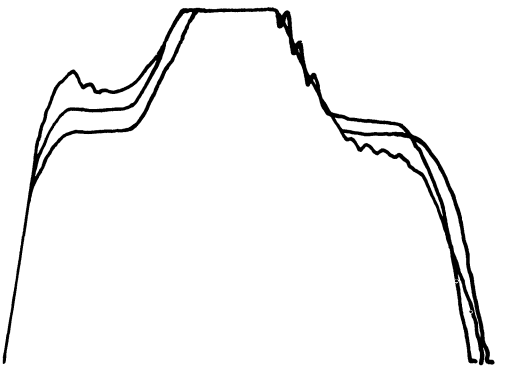
Linearly, sealed correlation curves show that switching characterization curves are valid over five decades of gate current.

Generally, the gate-voltage plateau will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "non-symmetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Gate-Voltage Propagation Effects — Most power-MOSFET applications need switch no faster than tenths of a microsecond. Should faster switching be required, it must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage wavefront applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each call, the delay cannot be characterized by a pure number of so many nanoseconds.

At present, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result. Therefore, this is usually near the upper limit of usefulness.



Curves show the increasing effect of gate-voltage propagation.

Manufacturing Operations

The process technology and disciplines required to fabricate Power MOSFETs are very similar to LSI processing of integrated circuits. Current design rules accommodate 575,000 individual MOS cells per square inch of active die area. Design rules for 1986 increased the density of active cells to 725,000 per square inch.

To manufacture Power MOS devices effectively, RCA has funded a multi-million dollar wafer fabrication facility specifically for MOS. Features of this facility include:

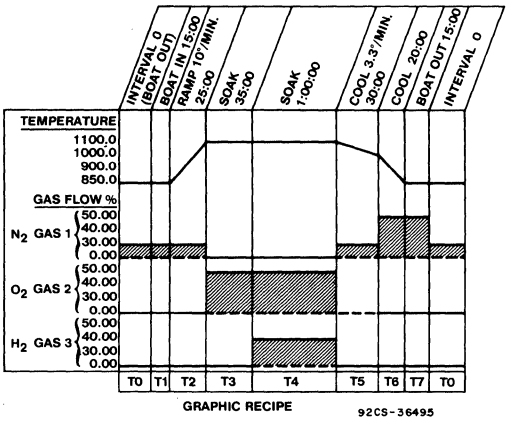
- 125-mm wafer capacity.
- Fully automated wafer transfer and handling.
- Microprocessor-controlled diffusion/LPCVD/metallization operation.
- Plasma etching of polysilicon and oxide films.
- Direct step on wafer-projection lithography.
- LPCVD polysilicon/doped oxides/undoped oxides.
- Ion implantation (low and high dose).
- Microprocessor-controlled photolithography operations.
- Computer-aided design and process simulation.
- Automated TO-220 and TO-3 Packaging.
- Automated pellet/finished-goods testing.

Diffusion Operations

RCA power MOSFETs are processed in a Class 100 environment using state-of-the-art computer-controlled diffusion, LPCVD, and monitoring equipment. All diffu-

Manufacturing Operations

sion and LPCVD tubes have a dedicated microcontroller specifically designed to control furnaces engaged in semiconductor wafer processing. The microcontrollers provide complete recipe creation and storage capabilities, constant monitoring of furnace conditions, automatic control of all furnace functions (time sequencing,



Micrographic recipe for a typical diffusion sequence.

temperature profiling/ramping, mass-flow controlled gases, and wafer-boat movements), alert/alarm provisions, and extensive diagnostic capabilities. The microcontrollers are supervised by a central computer console which provides additional recipe storage, inventory control, and centralized process monitoring.

Wafers are handled by first-generation robotics (cassette-to-cassette) at all stages of processing to eliminate human-handling induced defects. In addition, only the purest available gases, chemicals, and ultra filtered water are used to process RCA Power MOS/FETs. Ion implantation is used exclusively for all diffusion dopant sources to achieve exceptional uniformity and repeatability.

Lithography Operations

The Power MOSFET Lithography is performed in a temperature and humidity-controlled Class 100 environment using the most recent static-neutralizing equipment. Both coating and developing is performed on microprocessor controlled tracks. Each step is designed for cassette-to-cassette operation.

Mix and match exposure tools employ automatic laser alignment schemes throughout. Proximity machines are used for non-critical levels, while the registration and critical defect layers are printed by use of a 1.1 direct wafer stepper.

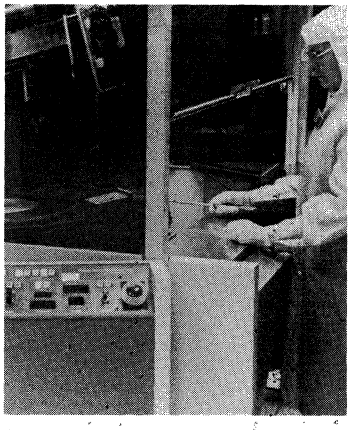
A metal ion-free developer is used exclusively to guard against any trace impurities. Inspection and critical dimension control are handled in a cassette-to-cassette manner by the successful marriage of the Nanometrics line-width computer with the OSI inspection station incorporating automatic laser focusing.

A high temperature positive resist is used on all product to assure line-width fidelity through high-current ion implantation. Plasma etching is used for pattern delineation using the single-wafer approach with end-point detection.

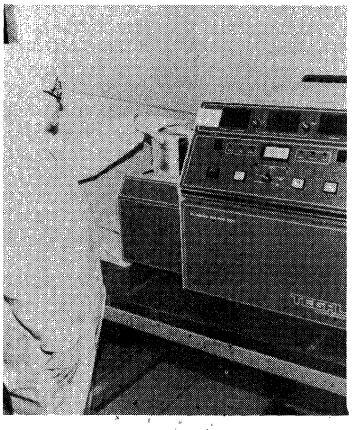
Assembly

Automation is being introduced to improve product quality and reliability.

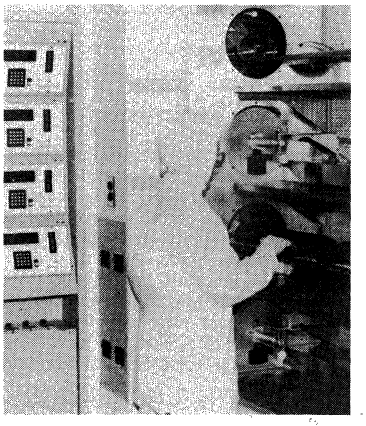
Automatic equipment has been installed to assemble the TO-220; additional equipment currently is installed to fully automate assembly of TO-3 devices. Both of these assembly lines utilize the latest state-of-the-art techniques, such as pattern recognition systems, to identify "good" pellets for automatic transfer from a sawed wafer array and also to identify and locate the bond pads for automatic placement of the interconnect bond wires. Wire bond integrity is determined automatically as resonant frequency values registered after each ultra-



Ion-implantation system used for all diffusion operations.

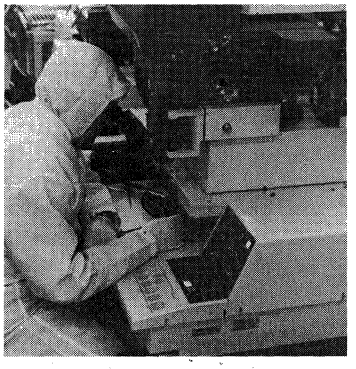


System used for polysilicon plasma-etch operation.

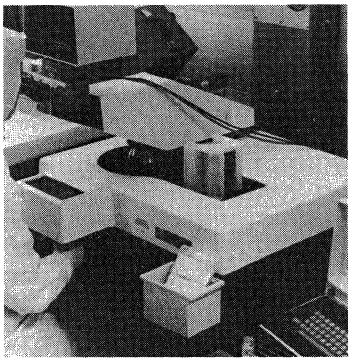


Computer controlled system provides direct digital control of all furnace operations.

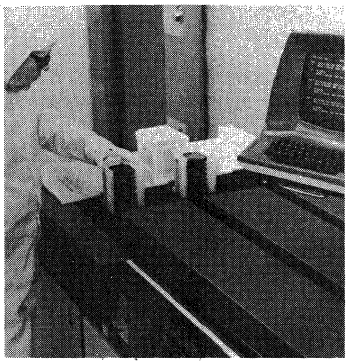
Manufacturing Operations



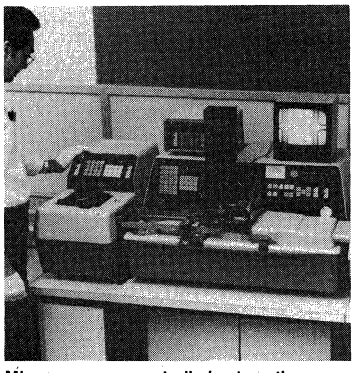
Direct wafer stepper (1X) used for critical lithography alignment.



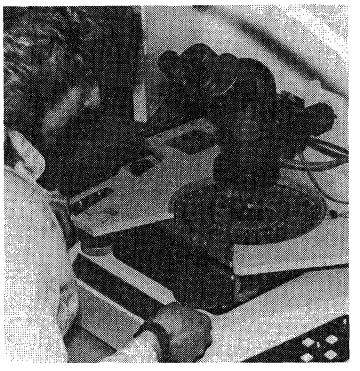
OSI inspection system provides resolution to nanoline widths.



Microprocessor-controlled macronetic coating track.



Microprocessor-controlled automatic wafer dicing system.



Wafer circuit probe test station.

sonic bond. Oxygen level sensors and moisture monitors are used at the sealing operation to TO-3 devices to guarantee the proper environment to assure reliable hermetic product. In addition, the latest state-of-the-art electronic tests have been instituted for all dc static tests, hot switching, inductive testing, Is/b and other tests required to assure that product does indeed meet specifications.

TO-3 Assembly System

The TO-3 manufacturing system is fully automatic from wafer sawing through brand and pack operations. This system is designed to eliminate all handling of product by the operator. It reduces cycle time, improves reliability levels, and is potentially capable of a 30 parts-per-million quality level.

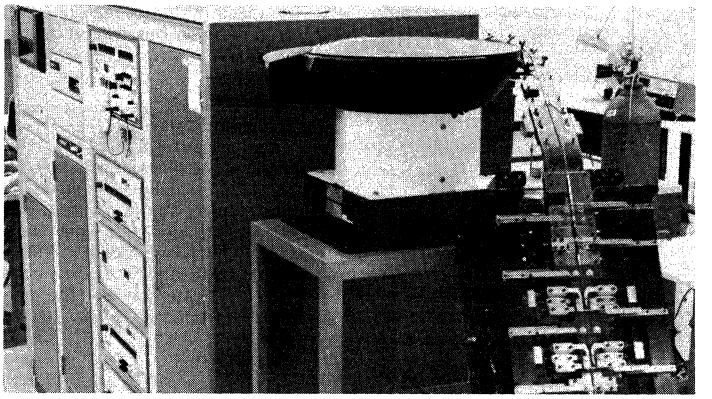
System operation begins with the feeding of TO-3 stems from vibratory bowls into an automatic chip-mounting machine. Stems with chips mounted are then output to a storage cart. The storage cart provides the input to the automatic aluminum-wire bond machine, which ultrasonically bonds the wires to the chip and leads on the TO-3 stems. After wire bonding, the product is auto-loaded into the storage carts, which are then loaded into the automatic sealing machine. This machine processes the product through a one-hour bake prior to weld sealing. Sealing is done in a nitrogen atmosphere to assure device hermeticity; the product then moves again to a storage cart. The sealed product is next loaded into a machine that automatically coats the TO-3 leads with solder and then loads the product back into the storage cart for transportation to the test handlers. At the test-handler station, the devices are automatically dispensed into one of twenty bins according to test specifications, and then stored in an automatic storage and retrieval system. A robot stores the product automatically and keeps track of it through a bar code system that identifies each test bin. The bins are stored at random locations by the robot and retrieved when needed to satisfy an order from a customer. When retrieved, a bin is brought to a brand and pack machine where the bin bar code is verified by a code reader. If the bar code is correct, the product is fed from a vibratory feed bowl into the machine where it is tested again to assure compliance to tests specifications, branded, and packed for shipment to the customer.

Quality audits are taken on-line after each operation to assure the quality level of the product. Checks for voids under the pellet, bonded wire pull strengths, hermeticity after sealing, solder coverage of leads, correlation of test specifications at testing, and the final test at branding to guarantee the integrity of the device to the customer are all monitored on a scheduled basis throughout the production process.

Manufacturing Operations

Testing

All MOSFET testing is done on automatic test equipment. Stations are provided for both wafer probe and finished-goods testing. All finished devices in TO-220 and TO-3 packages are automatically handled and tested to assure the highest possible quality levels at the final-test operation. The water prober is attached to a wafer mapper so that device parameters can be mapped to determine variation across the wafer. This data can then be compared with the statistical information that is generated. Given the proper command, statistical tables and histograms are printed out.



Automatic TO-3 and TO-220 power MOSFET test set.

Quality and Reliability Assurance

The ability to build and maintain the high levels of quality and reliability required today, depends on inherent design and process capability, and not the degree of test and inspection. Both the design and production facilities for RCA's Power MOSFET are totally new, with state-of-the-art equipment and process techniques which deliver this needed capability.

In-Process Quality Control

All critical phases of the highly automated power MOSFET manufacturing cycle have been characterized with respect to their intrinsic variability. Statistical limits have been established to give early warning of abnormal process trends and fluctuations, based on this intrinsic capability. These limits are constantly tightened as the process improves and are well within the engineering specifications. The emphasis at RCA is to employ statistical methods at the point of control, rather than an inspection point at the end of a process.

Control of Outgoing Product

The quality control lot acceptance sampling of finished product is performed after manufacturing has performed 100% inspection of all specified electrical characteristics. The current sampling level is 0.1% AQL for electrical parameters, and is constantly being improved. However, due to tight parameter distributions gained through process control and inherent design capability, the average outgoing quality level (AOQ) to the customer has been in the order of 100 PPM (0.01%).

Reliability Assurance

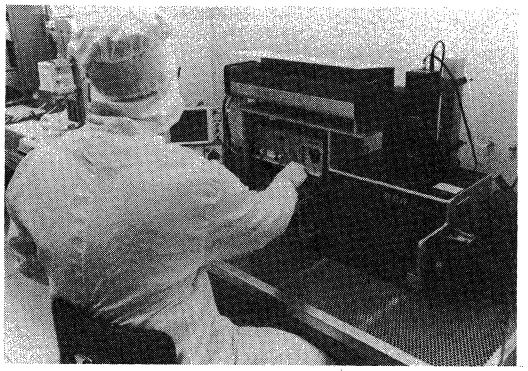
RCA Solid State has a world-wide reliability program that helps to shape the direction of new product development, assures that the reliability level is maintained throughout the production cycle, and develops specific models to predict the reliability in the end-use application. In order to meet these objectives, a reliability facility is maintained at each manufacturing location for real-time feedback. A centralized reliability engineering organization develops all new test methods and supports new product/process development. Each group is fully trained in the reliability and applied statistics disciplines, as well as failure analysis, and are responsible for using these techniques to monitor and improve product capability.

The Reliability program

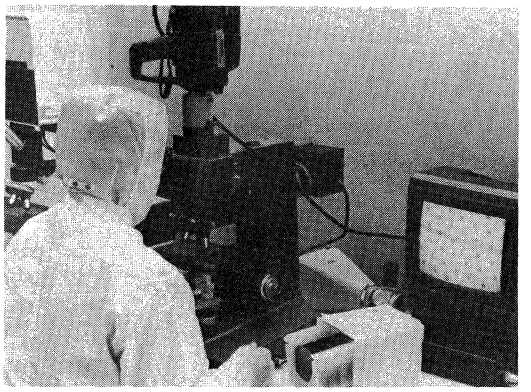
The reliability-assurance program operates at all stages of production, using the following four-pronged approach:

Product Design and Development — During early development, initial product lots are characterized through accelerated reliability tests which establish the product capability. Once the design has been fine-tuned,

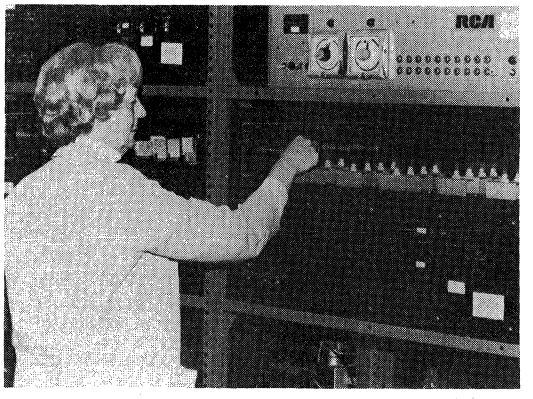
Quality and Reliability Assurance



Laser scanner used to detect processing defects.



Electronic microscope with TV monitor used for visual inspection of wafers.



Thermal-fatigue and operating-life test racks.

multiple production runs are initiated and samples are subjected to a full range of standardized accelerated tests. All lots must meet pre-established reliability standards before any new design or process can be released for production.

Wafer HTRB — RCA has developed a totally unique in-line reliability test performed at the wafer level. Samples from each wafer lot receive a 24-hour 150°C bias-life test to measure passivation integrity and surface cleanliness.

Real Time Indicators (RTI) — RTI's are short-duration accelerated-stress tests used to control the occurrence of specific failure mechanisms that can significantly affect product reliability. The stress levels are designed to induce failures, so that product-capability shifts can be detected and corrected. They are performed weekly at each manufacturing location. In this real-time method of determining reliability, a continuous flow of data is provided to indicate how well the manufacturing process is producing product.

Table I — Typical MOSFET RTI Tests

TEST	CONDITIONS	PACKAGE	TYPICAL DURATION
Power Cycling	PD = 4.75 Watts Tj = 35°-175°C (approx.)	Plastic	10-15K cycles
Power Cycling	PD = 56 Watts Tj = 90°-168°C (approx.)	TO-3	20-50K cycles
D-S Bias Life	TA = 150°C 80% of Drain-Source	All	168 hrs.
G-S Bias Life	G - S = 16 V, TA = 150°C	All	168 hrs.

Requalification Program (RQP) — Each product is requalified every six to twelve months to the same matrix of tests required for the initial production release. This operation measures the changes in the total capability of each MOS/FET family to meet the original reliability design objectives. Table II is typical of the data generated for RQP.

Quality and Reliability Assurance

Table II — Accelerated Power MOSFET Test Reliability Summary

PACKAGE	TEST AND CONDITIONS	DURATION	CUM. HOURS OR CYCLES	% NON-FUNCTIONAL
All	Bias Life Drain-Source = 80% of rated TA = 150°C	500 hrs.	300,000	0.33
All	Bias Life Gate-Source = 16V, TA = 150°C	500 hrs.	270,000	0.00
All	Operating Life TA = 150°C, Free Air	500 hrs.	230,000	0.00
TO-31 TO-39	Thermal Cycling -65°C to +150°C	400 cycles	133,600	0.30
TO-220	Thermal Shock -65°C to +150°C	400 cycles	100,000	0.00
TO-31 TO-39	Power Cycling Delta Tj = 78°C PD = 56 W (TO-3) or 2 W (TO-39)	20,000 cycles	5,480K	0.73
TO-220	Power Cycling Delta Tj = 135°C, PD = 4.75 W	10,000 cycles	1,850K	0.00
TO-220	Pressure Cooker	24 hrs.	3,072	0.00

Failure Rate in %/1000 Hours at 60% UCL

TEST	TA = 125°C	TA = 90°C	TA = 75°C
Bias Life	0.09	0.005	0.001
Operating Life	0.07	0.004	0.001

NOTE: Failure rate based on Nonfunctional performance in an operating mode, extrapolated from 150°C data using 1.0 eV activation energy.

Standard Power MOSFETs

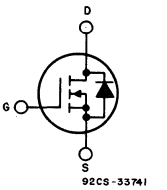
RFL1N08, RFL1N10, RFP2N08, RFP2N10

File Number **1385**

N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, 80 and 100 V
$r_{DS}(on)$: 1.05Ω and 1.2Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

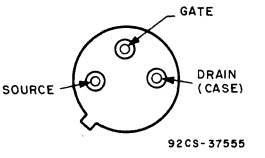
The RFL1N08 and RFL1N10 and the RFP2N08 and RFP2N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9282 and TA9283, respectively.

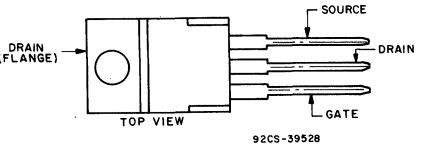
TERMINAL DESIGNATIONS

RFL1N08
RFL1N10



JEDEC TO-205AF

RFP2N08
RFP2N10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

		RFL1N08	RFL1N10	RFP2N08	RFP2N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100	80	100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	80	100	80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION @ T_C=25°C	P_T	8.33	8.33	25	25	W
Derate above T_C=25°C		0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFL1N08, RFL1N10, RFP2N08, RFP2N10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N08 RFP2N08 Min.	LIMITS RFL1N08 RFP2N08 Max.	LIMITS RFL1N10 RFP2N10 Min.	LIMITS RFL1N10 RFP2N10 Max.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0	80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	μA
		V_{DS}=80 V	—	—	—	1	
		T_C=125° C, V_{DS}=65 V	—	50	—	—	
		T_C=125° C, V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A RFP	—	1.05	—	1.05	V
		V_{GS}=10 V RFL	—	1.2	—	1.2	
		I_D=2 A RFP	—	3.0	—	3.0	
		V_{GS}=10 V RFL	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A RFP	—	1.05	—	1.05	Ω
		V_{GS}=10 V RFL	—	1.4	—	1.4	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A	400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V, V_{GS}=0 V, f = 1MHz	—	150	—	150	pF
Output Capacitance	C_{oss}		—	80	—	80	
Reverse-Transfer Capacitance	C_{rss}		—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V, I_D=1 A, R_{gen}=R_{gs}=50 Ω, V_{GS}=10 V RFP	17(Typ)	25	17(Typ)	25	ns
Rise Time	t_r		30(Typ)	45	30(Typ)	45	
Turn-Off Delay Time	$t_d(off)$		30(Typ)	45	30(Typ)	45	
Fall Time	t_f	RFP	17(Typ)	25	17(Typ)	25	
		RFL	30(Typ)	50	30(Typ)	50	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1N08, RFL1N10	—	15	—	15	°C/W
		RFP2N08, RFP2N10	—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N08 RFP2N08 Min.	LIMITS RFL1N08 RFP2N08 Max.	LIMITS RFL1N10 RFP2N10 Min.	LIMITS RFL1N10 RFP2N10 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	100(typ.)		100(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFL1N08, RFL1N10, RFP2N08, RFP2N10

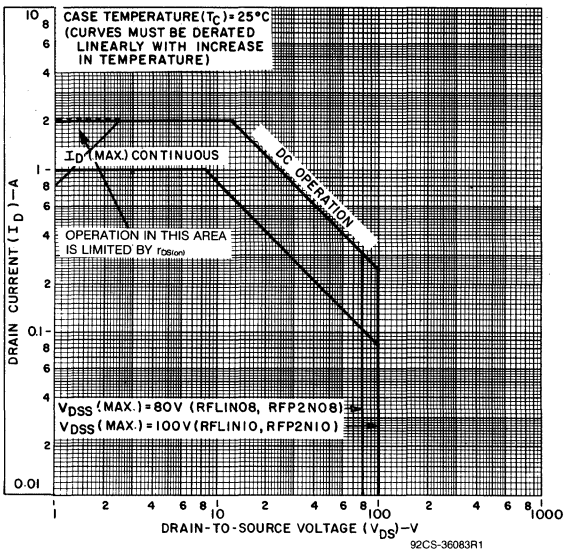


Fig. 1 - Maximum operating areas for all types.

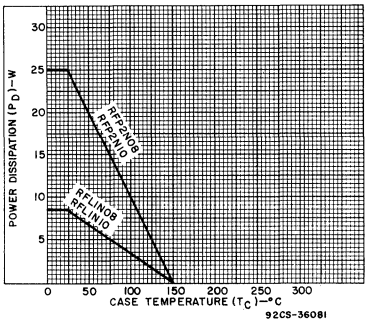


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

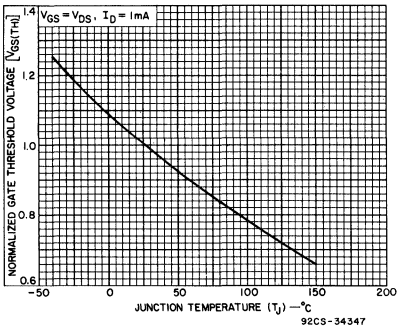


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

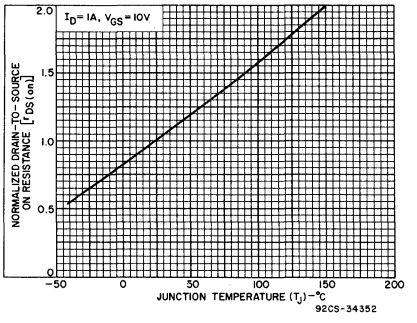


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

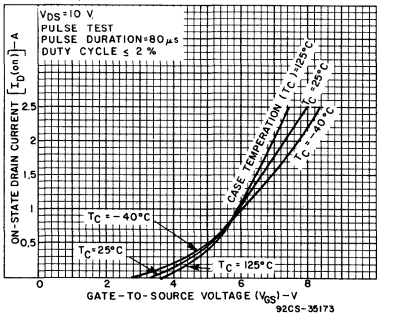


Fig. 5 - Typical transfer characteristics for all types.

RFL1N08, RFL1N10, RFP2N08, RFP2N10

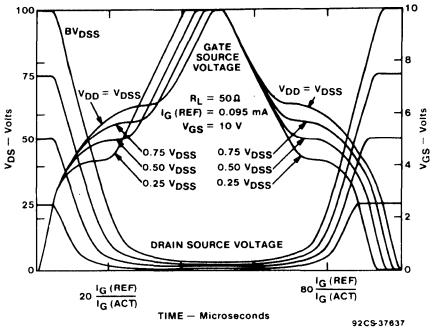


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

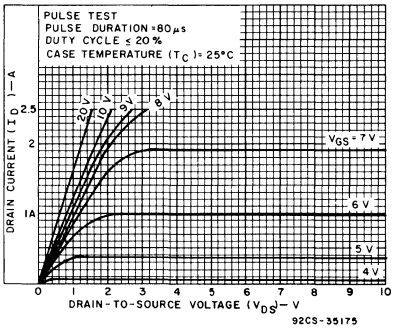


Fig. 7 - Typical saturation characteristics for all types.

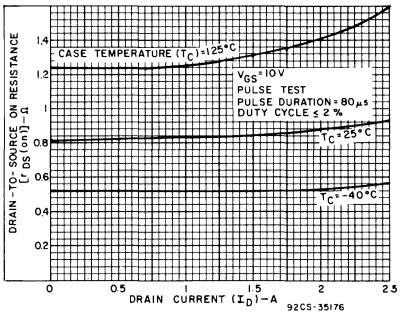


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

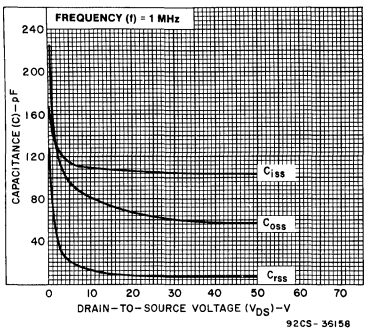


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

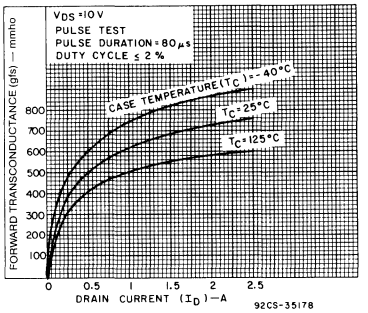


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

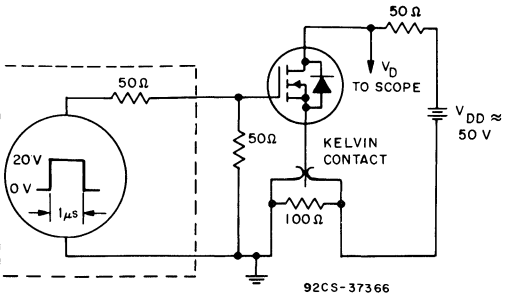


Fig. 11 - Switching Time Test Circuit.

RFL1N12, RFL1N15, RFP2N12, RFP2N15

File Number **1444**

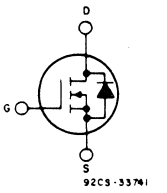
N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 Amperes 120 V — 150 V

$r_{DS}(on)$: 1.75Ω and 1.9Ω

Features:

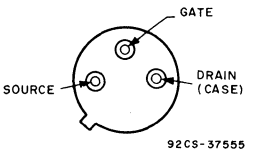
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

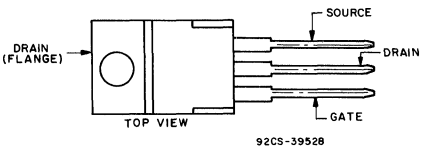
TERMINAL DESIGNATIONS

RFL1N12
RFL1N15



JEDEC TO-205AF

RFP2N12
RFP2N15



JEDEC TO-220AB

The RFL1N12 and RFL1N15 and the RFP2N12 and RFP2N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9196 and TA9213, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFL1N12	RFL1N15	RFP1N12	RFP2N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1A	1A	2A	2A	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION @ T_C=25°C	P_T	8.33	8.33	25	25	W
Derate above T_C=25°C		0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150				°C

RFL1N12, RFL1N15, RFP2N12, RFP2N15

ELECTRICAL CHARACTERISTICS *at Case Temperature (T_c) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		LIMITS RFL1N12 RFP2N12 MIN.	LIMITS RFL1N12 RFP2N12 MAX.	LIMITS RFL1N15 RFP2N15 MIN.	LIMITS RFL1N15 RFP2N15 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0		120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2 mA		2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V		—	1	—	—	μA
		V_{DS} = 120 V		—	—	—	1	
		T_C = 125°C, V_{DS} = 100 V		—	50	—	—	
		T_C = 125°C, V_{DS} = 120 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 1 A, V_{GS} = 10 V	RFP	—	1.75	—	1.75	V
			RFL	—	1.9	—	1.9	
		I_D = 2 A, V_{GS} = 10 V	RFP	—	6.0	—	6.0	
			RFL	—	6.3	—	6.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 1 A, V_{GS} = 10 V	RFP	—	2	—	2	Ω
			RFL	—	2.15	—	2.15	
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 1 A		400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz		—	150	—	150	pF
Output Capacitance	C_{oss}			—	80	—	80	
Reverse Transfer Capacitance	C_{rss}			—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 75 V, I_D = 1 A, R_{gen} = R_{gs} = 50 Ω, V_{GS} = 10 V		17(typ.)	25	17(typ.)	25	ns
Rise Time	t_r			30(typ.)	45	30(typ.)	45	
Turn-Off Delay Time	$t_d(off)$			30(typ.)	45	30(typ.)	45	
Fall Time	t_f		RFP	17(typ.)	25	17(typ.)	25	
			RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	RθJC	RFL1N12, RFL1N15		—	15	—	15	°C/W
		RFP2N12, RFP2N15		—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N12 RFP2N12 Min.	LIMITS RFL1N12 RFP2N12 Max.	LIMITS RFL1N15 RFP2N15 Min.	LIMITS RFL1N15 RFP2N15 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	150(typ.)		150(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs duty cycle = 2%.

RFL1N12, RFL1N15, RFP2N12, RFP2N15

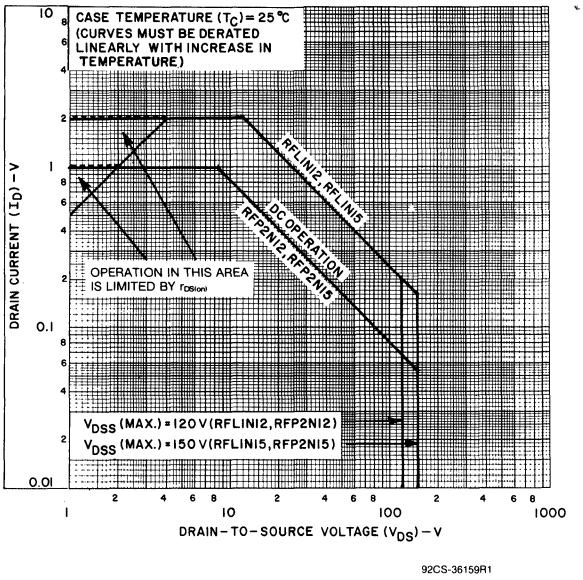


Fig. 1 — Maximum operating areas for all types.

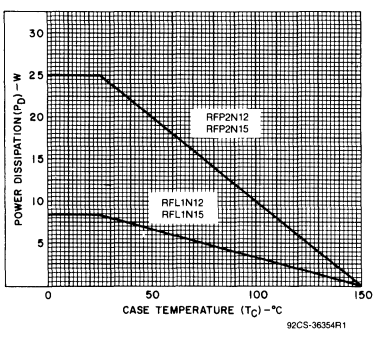


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

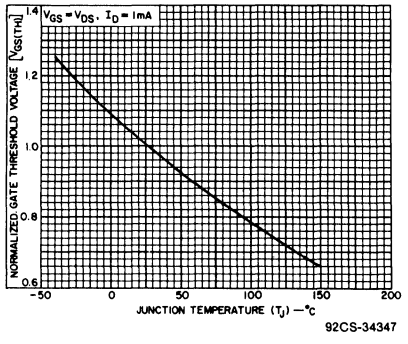


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

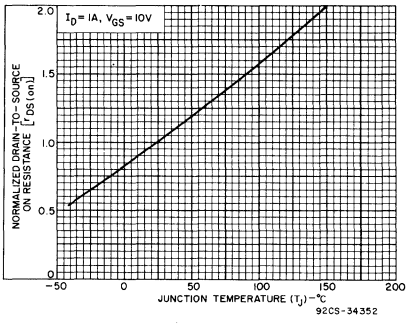


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

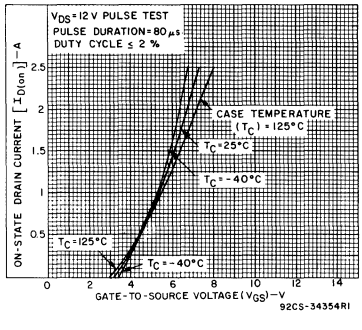


Fig. 5 — Typical transfer characteristics for all types.

RFL1N12, RFL1N15, RFP2N12, RFP2N15

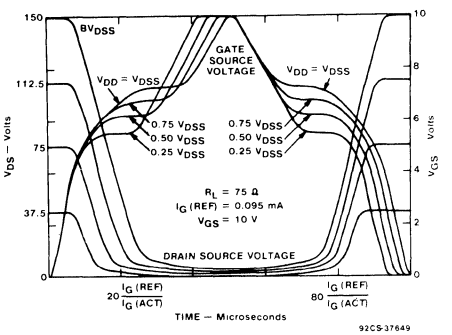


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

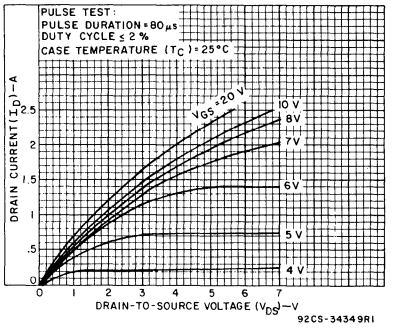


Fig. 7 — Typical saturation characteristics for all types.

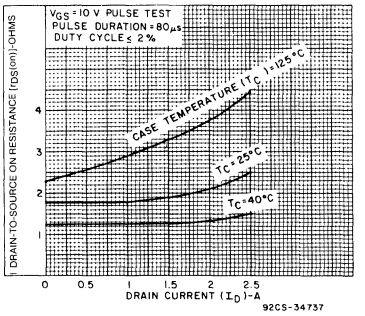


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

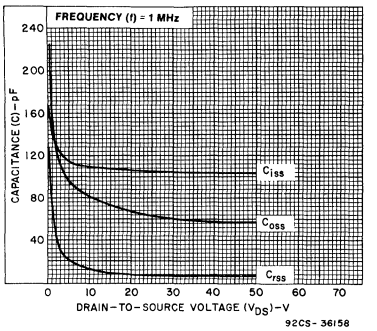


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

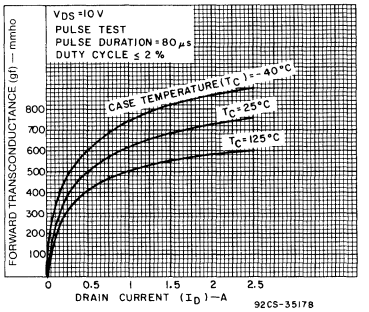


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

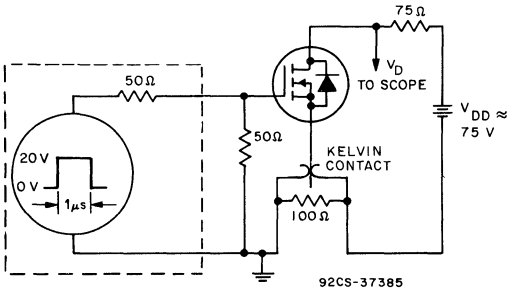


Fig. 11 — Switching Time Test Circuit.

RFL1N18, RFL1N20, RFP2N18, RFP2N20

File Number **1442**

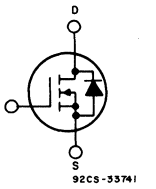
N-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, 180 and 200 V

$r_{DS}(on)$: 3.5Ω and 3.65Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

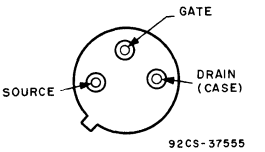
The RFL1N18 nd RFL1N20 and the RFP2N18 and RFP2N20 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9289 and TA9290, respectively.

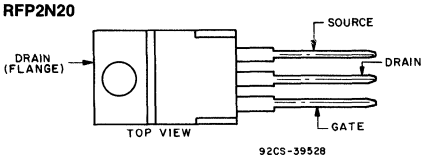
TERMINAL DESIGNATIONS

RFL1N18
RFL1N20



JEDEC TO-205AF

RFP2N18
RFP2N20



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25° C):

		RFL1N18	RFL1N20	RFP2N18	RFP2N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	180	200	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	180	200	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION	P_T					
@ T_C=25° C		8.33	8.33	25	25	W
Derate above T_C=25° C		0.0667	0.0667	0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFL1N18, RFL1N20, RFP2N18, RFP2N20

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N18 RFP2N18 Min.	LIMITS RFL1N18 RFP2N18 Max.	LIMITS RFL1N20 RFP2N20 Min.	LIMITS RFL1N20 RFP2N20 Max.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0		180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA		2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V		—	1	—	—	μA
		V_{DS}=160 V		—	—	—	1	
		T_C=125° C, V_{DS}=145 V		—	50	—	—	
		T_C=125° C, V_{DS}=160 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V	RFP	—	3.5	—	3.5	V
			RFL	—	3.65	—	3.65	
		I_D=2 A, V_{GS}=10 V	RFP	—	8.0	—	8.0	
			RFL	—	8.3	—	8.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V	RFP	—	3.5	—	3.5	Ω
			RFL	—	3.65	—	3.65	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A		400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V, V_{GS}=0 V, f = 1MHz		—	200	—	200	pF
Output Capacitance	C_{oss}			—	60	—	60	
Reverse-Transfer Capacitance	C_{rss}			—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V, I_D=1 A, R_{gen}=R_{gs}=50 Ω, V_{GS}=10 V		15(Typ)	25	15(Typ)	25	ns
Rise Time	t_r			20(Typ)	30	20(Typ)	30	
Turn-Off Delay Time	$t_d(off)$			25(Typ)	40	25(Typ)	40	
Fall Time	t_f		RFP	15(Typ)	25	15(Typ)	25	
			RFL	30(Typ)	50	30(Typ)	50	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1N18, RFL1N20		—	15	—	15	°C/W
		RFP2N18, RFP2N20		—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N18 RFP2N18 Min.	LIMITS RFL1N18 RFP2N18 Max.	LIMITS RFL1N20 RFP2N20 Min.	LIMITS RFL1N20 RFP2N20 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	200(typ.)		200(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFL1N18, RFL1N20, RFP2N18, RFP2N20

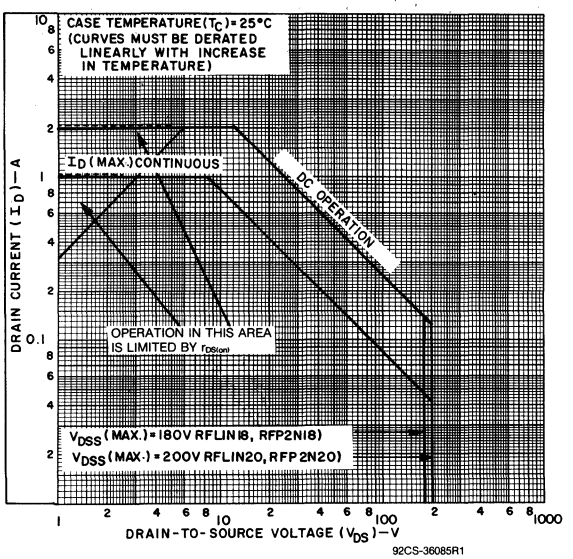


Fig. 1 - Maximum operating areas for all types.

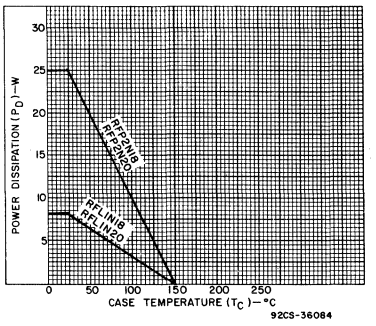


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

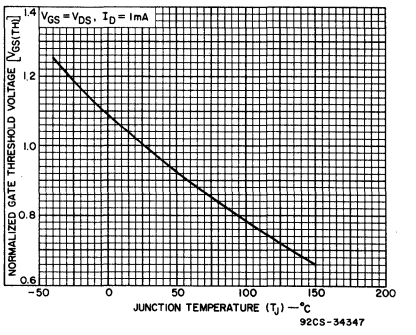


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

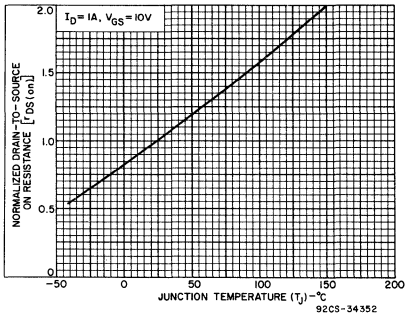


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

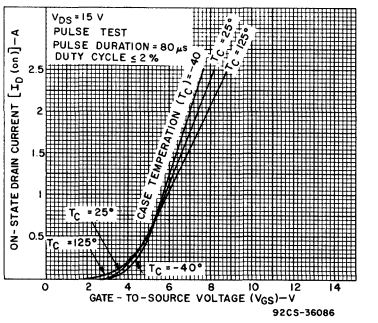


Fig. 5 - Typical transfer characteristics for all types.

RFL1N18, RFL1N20, RFP2N18, RFP2N20

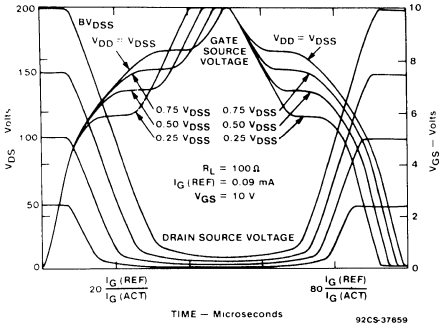


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

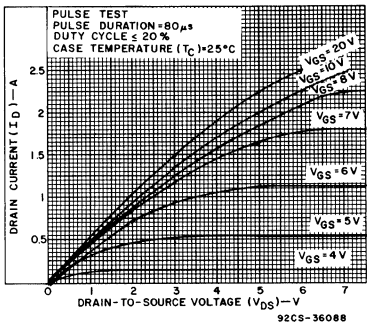


Fig. 7 - Typical saturation characteristics for all types.

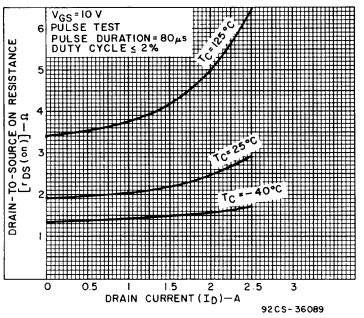


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

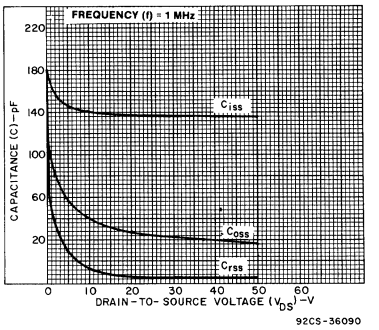


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

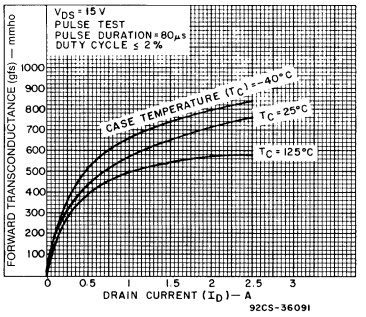


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

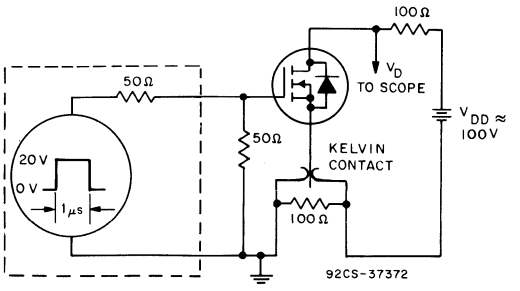


Fig. 11 — Switching Time Test Circuit.

RFP1N35, RFP1N40

File Number **1537**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

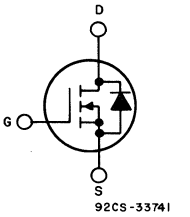
1 A, 350 and 400 V

$r_{DS}(on)$: 9 Ω

Features

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

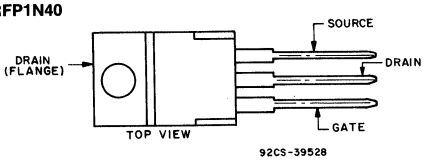
The RFP1N35 and RFP1N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFP-series types are supplied in the JEDEC TO-220AB plastic package.

*The RFP series were formerly RCA developmental number TA9390.

TERMINAL DESIGNATIONS

RFP1N35
RFP1N40



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

	RFP1N35		RFP1N40	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	350		400	V
DRAIN-GATE VOLTAGE, R_{GS}=1 MΩ..... V_{DGR}	350		400	V
GATE-SOURCE VOLTAGE ..... V_{GS}		±20		V
DRAIN CURRENT				
Rms Continuous ..... I_D		1		A
Pulsed ..... I_{DM}		2		A
POWER DISSIPATION @ T_C=25°C ..... P_T		25		W
Derate above T_C=25°C		0.2		W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}		-55 to +150		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFP1N35		RFP1N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V	—	1	—	—	μA
		V_{DS}=320 V	—	—	—	1	
		T_C=125° C V_{DS}=280 V	—	50	—	—	
		V_{DS}=320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=0.5 A V_{GS}=10 V	—	4.5	—	4.5	V
		I_D=1 A V_{GS}=10 V	—	11	—	11	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=0.5 A V_{GS}=10 V	—	9	—	9	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=0.5 A	250	—	250	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	50	—	50	
Reverse-Transfer Capacitance	C_{rss}	f=1 MHz	—	25	—	25	
Turn-On Delay Time	$t_d(on)$	V_{DS}=200 V	7(typ)	25	7(typ)	25	ns
Rise Time	t_r	I_D=1 A	8(typ)	25	8(typ)	25	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	28(typ)	60	28(typ)	60	
Fall Time	t_f	V_{GS}=10 V	29(typ)	60	29(typ)	60	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFP1N35, RFP1N40	—	5	—	5	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFP1N35		RFP1N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=0.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A di_F/dt=50 A/μs	760 (typ)				ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFP1N35, RFP1N40

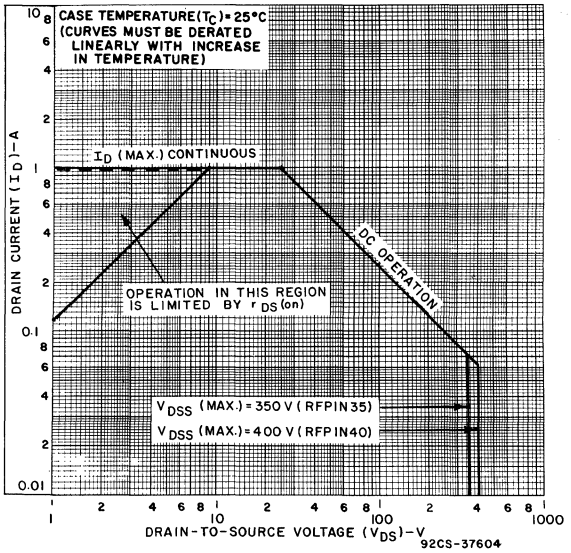


Fig. 1 - Maximum operating areas for all types.

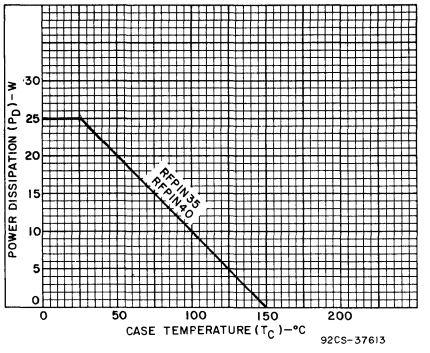


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

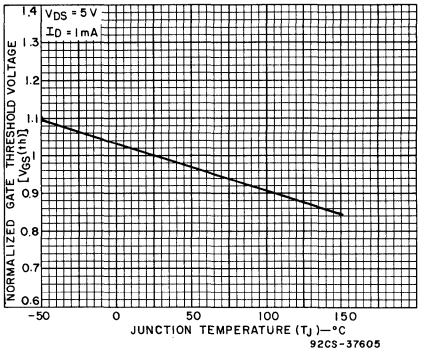


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

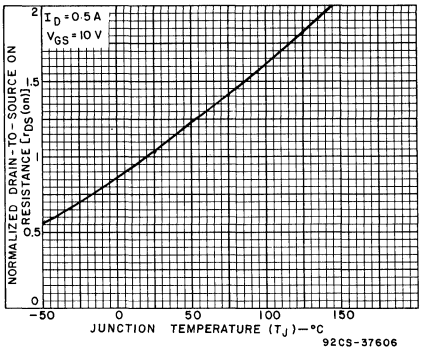


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

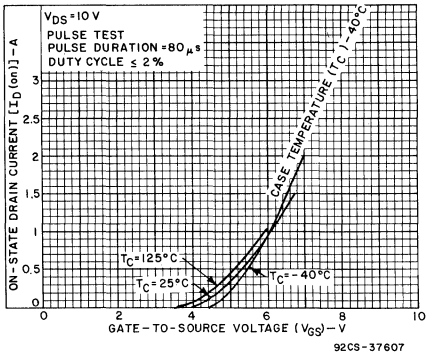


Fig. 5 - Typical transfer characteristics for all types.

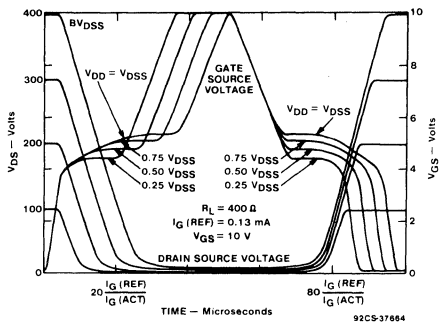


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

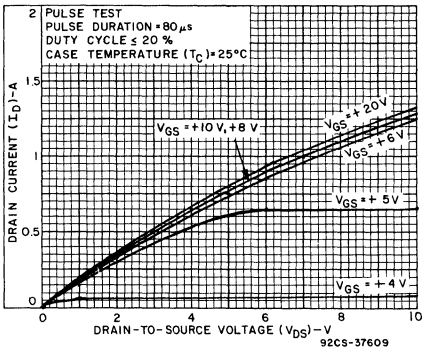


Fig. 7 - Typical saturation characteristics for all types.

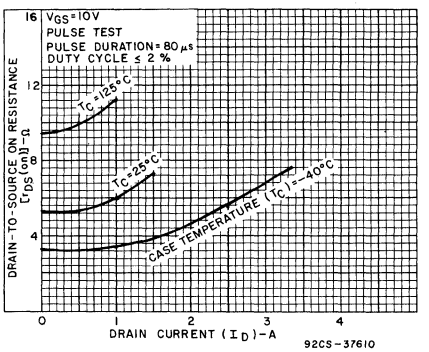


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

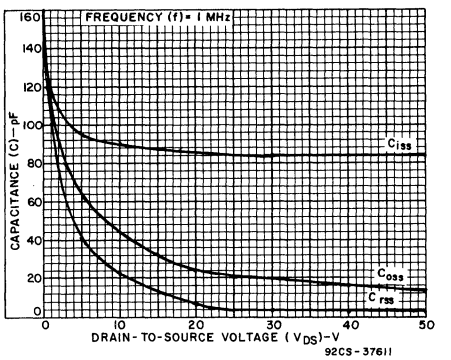


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

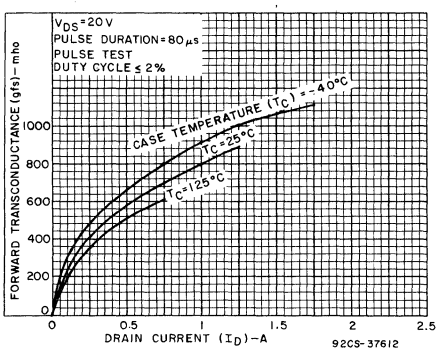


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

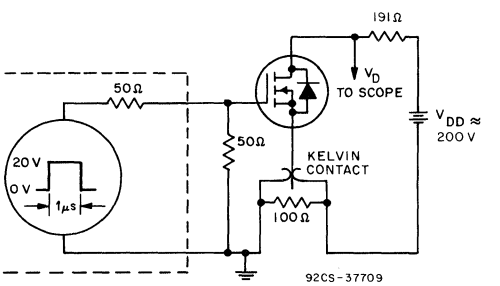


Fig. 11 - Switching time test circuit.

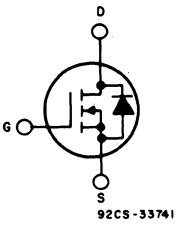
RFL2N05, RFL2N06, RFP4N05, RFP4N06

File Number **1497**

N-Channel Enhancement-Mode Power Field-Effect Transistors

2 and 4 Amperes, 50 V - 60 V
$r_{DS}(on)$ = 0.6Ω and 0.75Ω

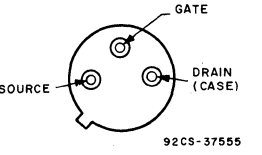
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

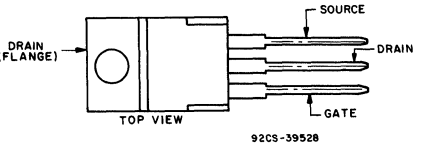
TERMINAL DESIGNATIONS

RFL2N05
RFL2N06



JEDEC TO-205AF

RFP4N05
RFP4N06



JEDEC TO-220AB

The RFL2N05 and RFL2N06 and the RFP4N05 and RFP4N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9378 and TA9379, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL2N05	RFL2N06		RFP4N05	RFP4N06	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60		50	60	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	50	60		50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D	2	2		4	4	A
Pulsed ..... I_{DM}			10			A
POWER DISSIPATION @ T_C=25°C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25°C	0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL2N05, RFL2N06, RFP4N05, RFP4N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFL2N05 RFP4N05 MIN.	LIMITS RFL2N05 RFP4N05 MAX.	LIMITS RFL2N06 RFP4N06 MIN.	LIMITS RFL2N06 RFP4N06 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA, V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	μA
		V_{DS}=50 V	—	—	—	1	
		T_C=125° C, V_{DS}=40 V	—	50	—	—	
		T_C=125° C, V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V RFP	—	0.6	—	0.6	V
		I_D=1 A, V_{GS}=10 V RFL	—	0.75	—	0.75	
		I_D=2 A, V_{GS}=10 V	—	2.0	—	2.0	
		I_D=4 A, V_{DS}=15 V	—	4.8	—	4.8	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A, V_{GS}=10 V RFP	—	0.6	—	0.6	Ω
		I_D=1 A, V_{GS}=10 V RFL	—	0.75	—	0.75	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A	400	—	400	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	150	—	150	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	85	—	85	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	30	—	30	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V	6(typ)	15	6(typ)	15	ns
Rise Time	t_r	I_D=1 A	14(typ)	30	14(typ)	30	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	16(typ)	30	16(typ)	30	
Fall Time	t_f	V_{GS}=10 V RFP	14(typ)	25	14(typ)	25	
		V_{GS}=10 V RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL2N05, RFL2N06	—	15	—	15	°C/W
		RFP4N05, RFP4N06	—	5	—	5	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL2N05 RFP4N05 Min.	LIMITS RFL2N05 RFP4N05 Max.	LIMITS RFL2N06 RFP4N06 Min.	LIMITS RFL2N06 RFP4N06 Max.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, d_{IF}/d_t = 50A/μs	100(typ.)		100(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFL2N05, RFL2N06, RFP4N05, RFP4N06

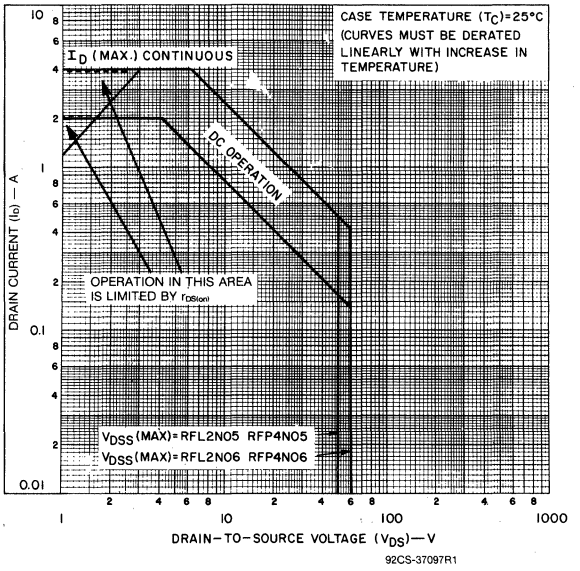


Fig. 1 — Maximum operating areas for all types.

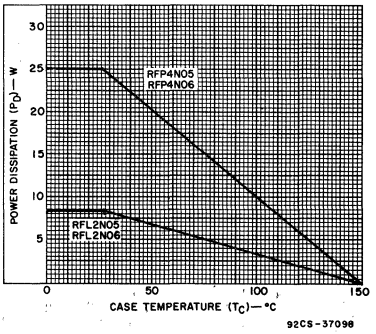


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

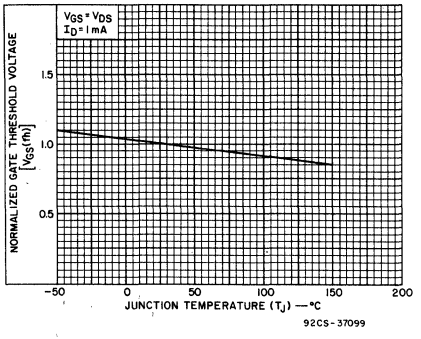


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

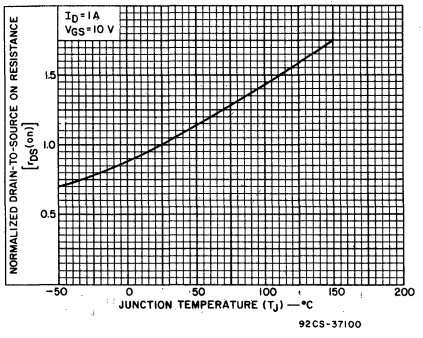


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

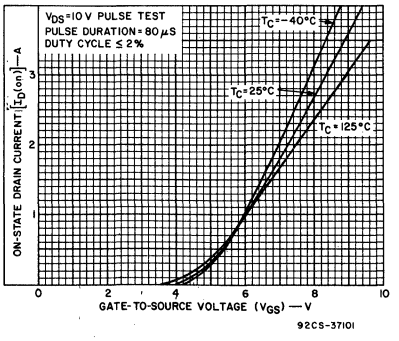


Fig. 5 — Typical transfer characteristics for all types.

RFL2N05, RFL2N06, RFP4N05, RFP4N06

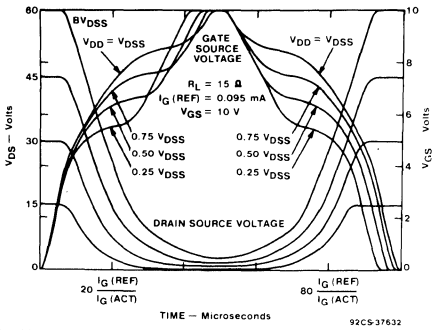


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

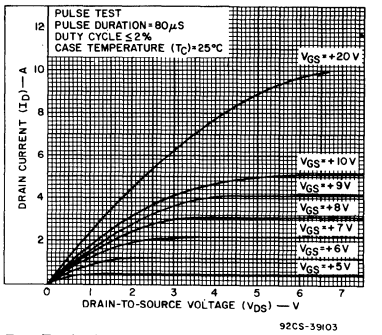


Fig. 7 — Typical saturation characteristics for all types.

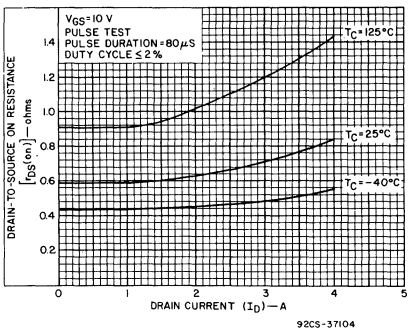


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

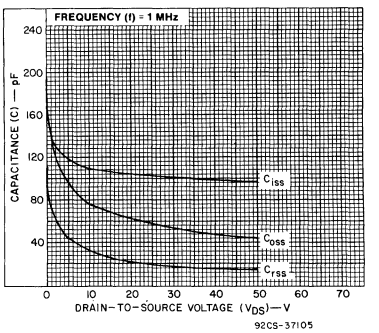


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

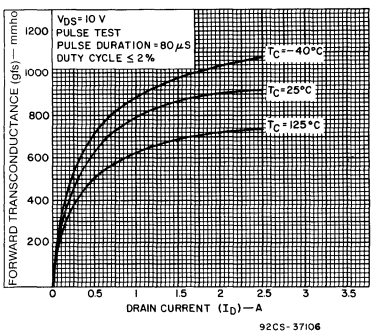


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

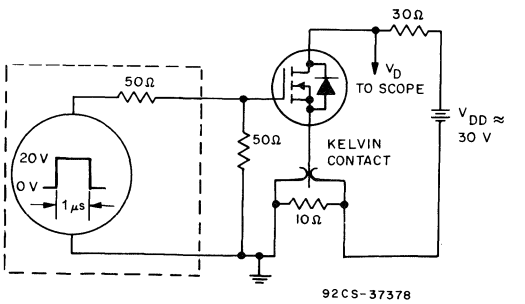


Fig. 11 — Switching Time Test Circuit.

RFM3N45, RFM3N50, RFP3N45, RFP3N50

File Number **1384**

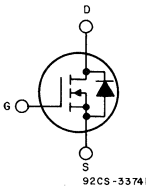
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3 A, 450 and 500 V
r_{DS}(on): 2.5Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

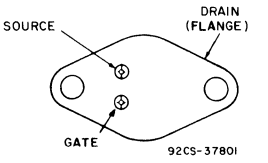
The RFM3N45 and RFM3N50 and the RFP3N45 and RFP3N50 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9193 and TA9232, respectively.

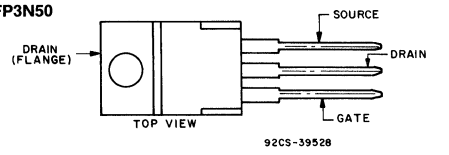
TERMINAL DESIGNATIONS

RFM3N45
RFM3N50



JEDEC TO 204AA

RFP3N45
RFP3N50



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM3N45	RFM3N50		RFP3N45	RFP3N50	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	450	500		450	500	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	450	500		450	500	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			3			A
Pulsed ..... I_{DM}			5			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM3N45, RFM3N50, RFP3N45, RFP3N50

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS}=0	450	—	500	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V	—	10	—	—	μA
		V_{DS}=400 V	—	—	—	10	
		T_C=125° C V_{DS}=360 V	—	50	—	—	
		T_C=125° C V_{DS}=400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	4.5	—	4.5	V
		I_D=3 A V_{GS}=10 V	—	10.5	—	10.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1.5 A V_{GS}=10 V	—	2.5	—	2.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=1.5 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	600	—	600	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	150	—	150	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	50	—	50	
Turn-On Delay Time	$t_d(on)$	V_{DD}=250 V	30(Typ)	45	30(Typ)	45	ns
Rise Time	t_r	I_D=1.5 A	40(Typ)	60	40(Typ)	60	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	90(Typ)	135	90(Typ)	135	
Fall Time	t_f	V_{GS}=10 V	50(Typ)	75	50(Typ)	75	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM3N45, RFM3N50	—	1.67	—	1.67	°C/W
		RFP3N45, RFP3N50	—	2.083	—	2.083	

[a] Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM3N45 RFP3N45		RFM3N50 RFP3N50		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=1.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM3N45, RFM3N50, RFP3N45, RFP3N50

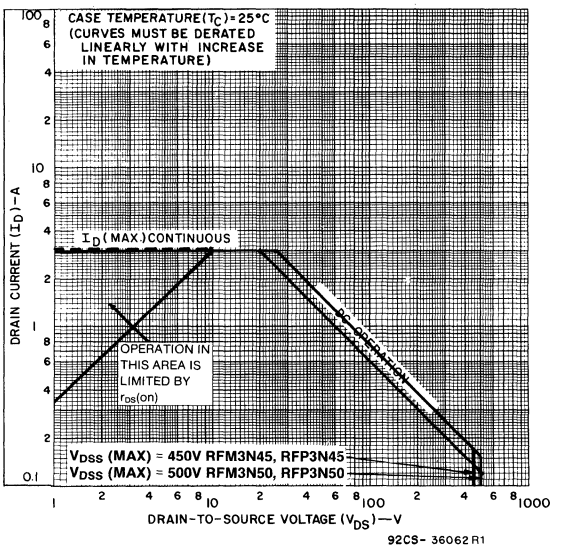


Fig. 1 - Maximum operating areas for all types.

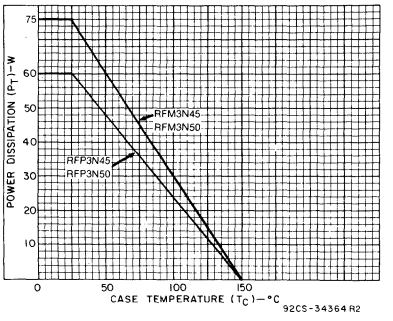


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

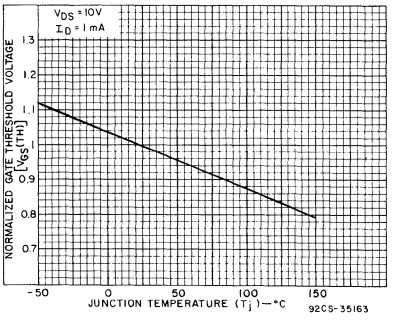


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

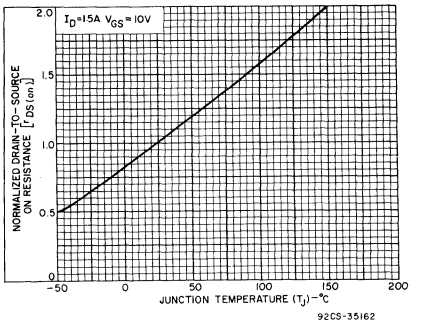


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

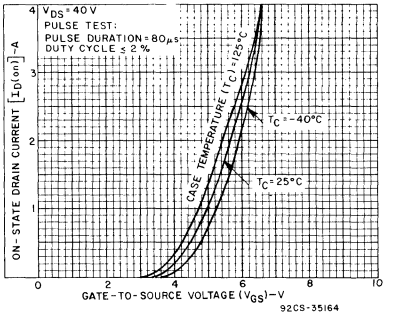


Fig. 5 - Typical transfer characteristics for all types.

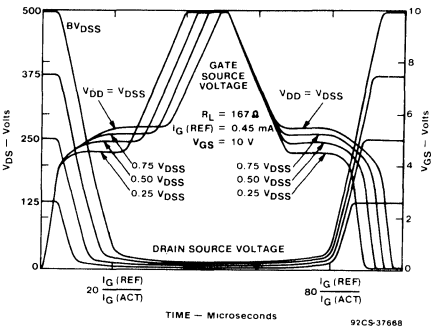


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

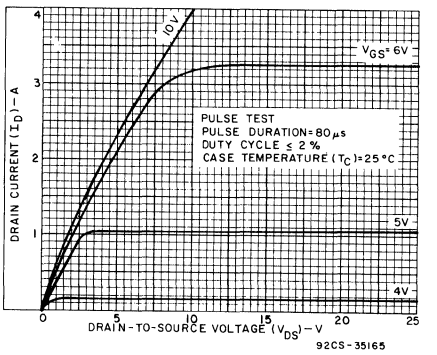


Fig. 7 - Typical saturation characteristics for all types.

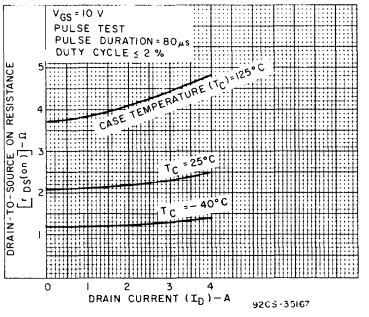


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

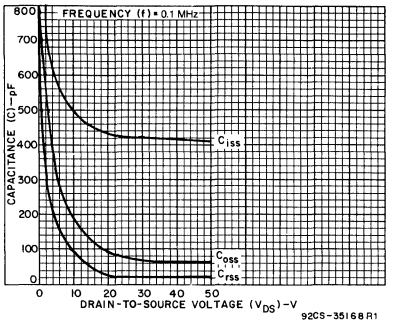


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

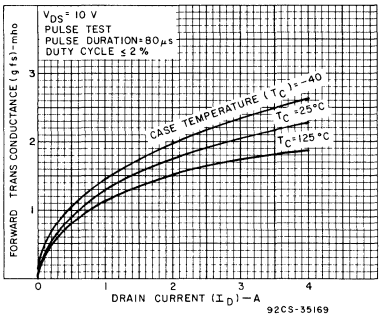


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

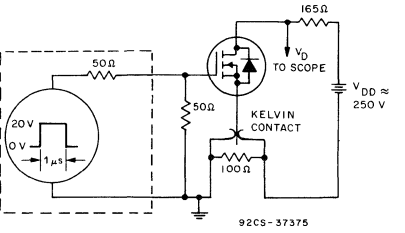


Fig. 11 — Switching Time Test Circuit

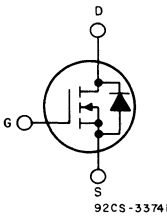
RFL4N12, RFL4N15

File Number **1462**

N-Channel Enhancement-Mode Power Field-Effect Transistors

4 A, 120 and 150 V
$r_{DS}(on)$: 0.4Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



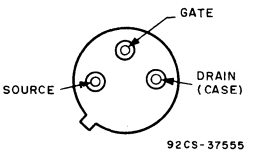
N-CHANNEL ENHANCEMENT MODE

The RFL4N12 and RFL4N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package.

*The RFL4N12 and RFL4N15 series were formerly RCA developmental numbers TA9256A and TA9256B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-205AF

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

		RFL4N12	RFL4N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20	±20	V
DRAIN CURRENT RMS Continuous	I_D	4	4	A
Pulsed	I_{DM}	15	15	A
POWER DISSIPATION @ T_C=25°C	P_T	8.33	8.33	W
Derate above T_C=25°C		0.0667	0.0667	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150	-55 to +150	°C

RFL4N12, RFL4N15

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125°C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	0.8	—	0.8	V
		I_D=4 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	0.40	—	0.40	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	650	—	650	pF
Output Capacitance	C_{oss}		—	230	—	230	
Reverse-Transfer Capacitance	C_{rss}		—	60	—	60	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 75 V I_D=2 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	40(typ)	60	40(typ)	60	ns
Rise Time	t_r		165(typ)	250	165(typ)	250	
Turn-Off Delay Time	$t_d(off)$		90(typ)	135	90(typ)	135	
Fall Time	t_f		90(typ)	135	90(typ)	135	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL4N12, RFL4N15	—	15	—	15	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL4N12		RFL4N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 2A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFL4N12, RFL4N15

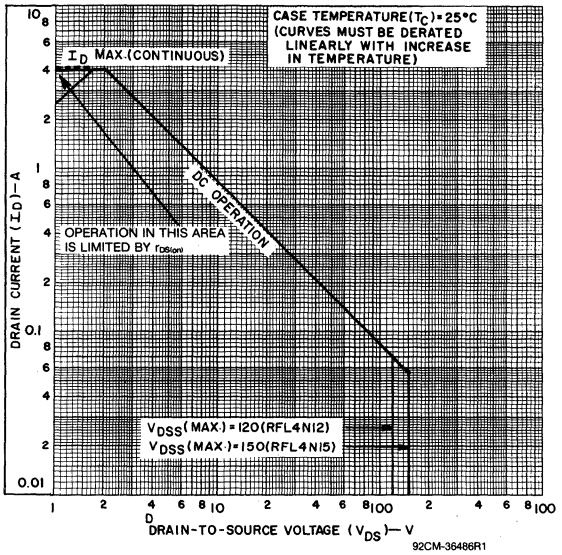


Fig. 1 - Maximum safe operating areas for all types.

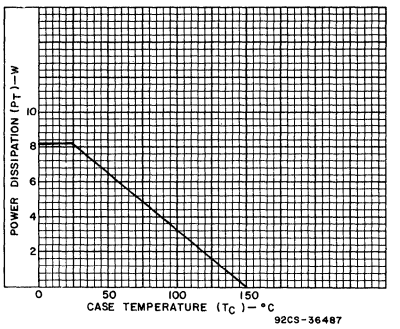


Fig. 2 - Power vs. temperature derating curve for all types.

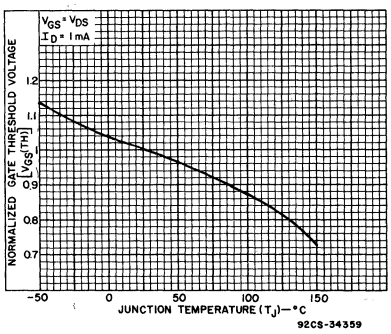


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

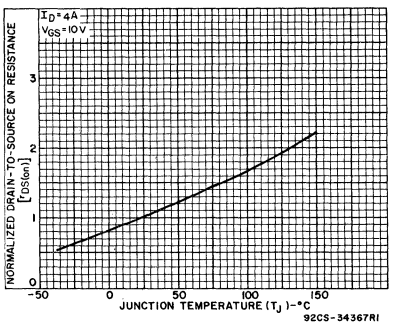


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

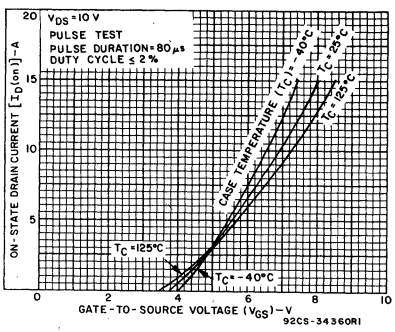


Fig. 5 - Typical transfer characteristics for all types.

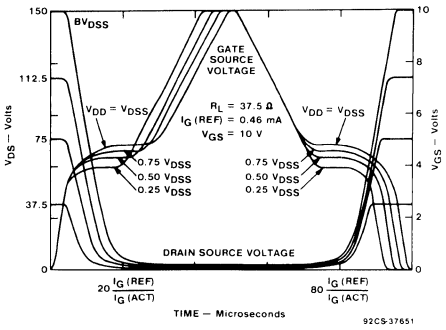


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

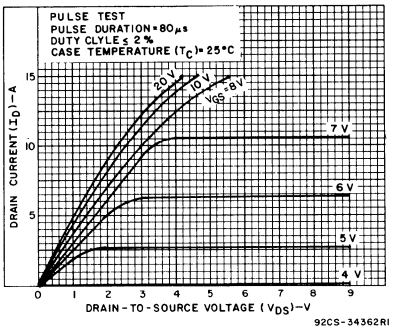


Fig. 7 - Typical saturation characteristics for all types.

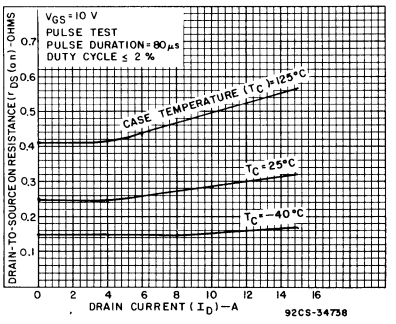


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

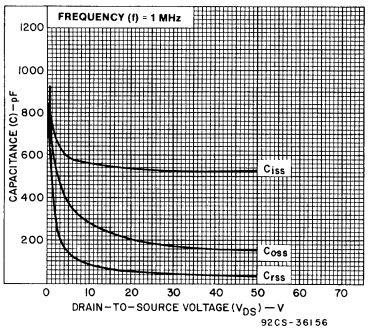


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

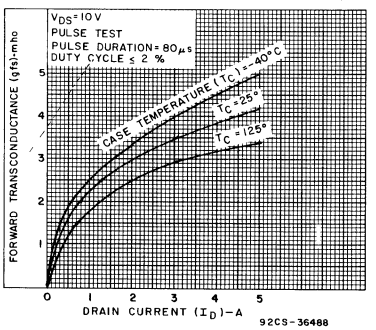


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

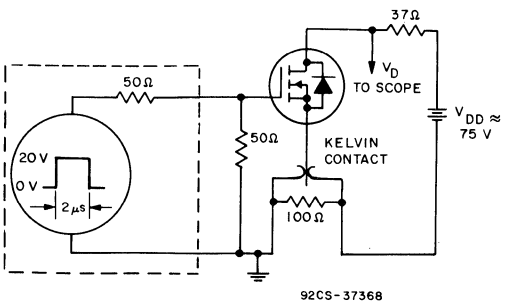


Fig. 11 - Switching Time Test Circuit.

RFM4N35, RFM4N40, RFP4N35, RFP4N40

File Number **1491**

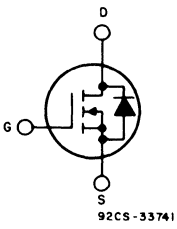
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

4 A, 350 V and 400 V
$r_{DS}(on)$ = 1.5Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

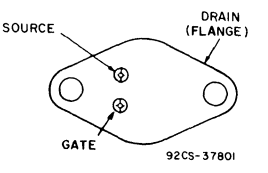
The RFM4N35 and RFM4N40 and the RFP4N35 and RFP4N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9393 and TA9394, respectively.

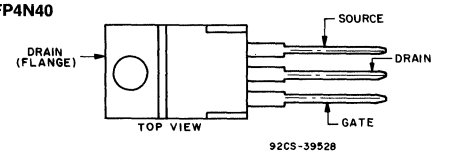
TERMINAL DESIGNATIONS

RFM4N35
RFM4N40



JEDEC TO-204AA

RFP4N35
RFP4N40



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM4N35	RFM4N40		RFP4N35	RFP4N40	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	350	400		350	400	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	350	400		350	400	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			4			A
Pulsed ..... I_{DM}			8			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM4N35, RFM4N40, RFP4N35, RFP4N40

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V V_{DS}=320 V	— —	10 —	— —	— 10	μA
		T_C=125°C V_{DS}=280 V V_{DS}=320 V	— —	100 —	— —	— 100	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	4	—	4	V
		I_D=4 A V_{GS}=10 V	—	12	—	12	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=2 A V_{GS}=10 V	—	1.5	—	1.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=2 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	650	—	650	pF
Output Capacitance	C_{oss}		—	150	—	150	
Reverse Transfer Capacitance	C_{rss}		—	50	—	50	
Turn-On Delay Time	$t_d(on)$	V_{DD}=200 V I_D=2 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	12(typ)	45	12(typ)	45	ns
Rise Time	t_r		42(typ)	60	42(typ)	60	
Turn-Off Delay Time	$t_d(off)$		130(typ)	200	130(typ)	200	
Fall Time	t_f		62(typ)	100	62(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM4N35, RFM4N40	—	1.67	—	1.67	°C/W
		RFP4N35, RFP4N40	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM4N35 RFP4N35		RFM4N40 RFP4N40		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=2 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	800(typ)		800(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM4N35, RFM4N40, RFP4N35, RFP4N40

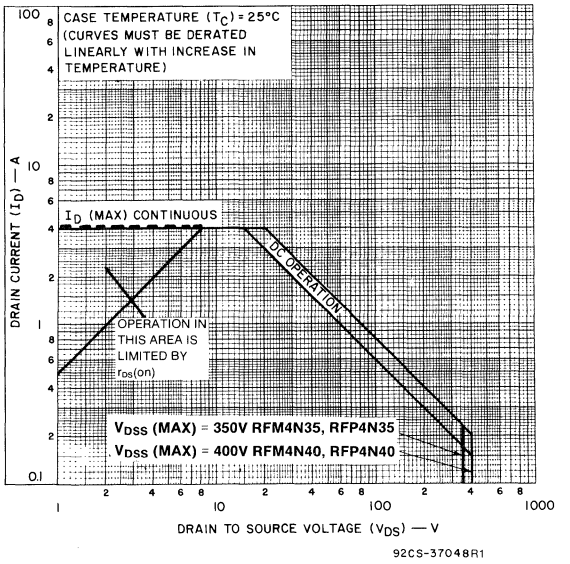


Fig. 1 — Maximum operating areas for all types.

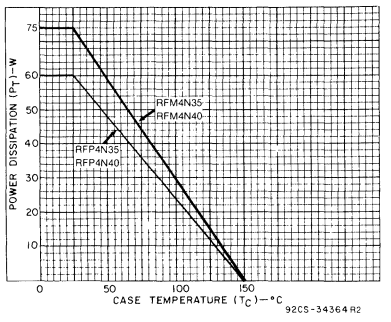


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

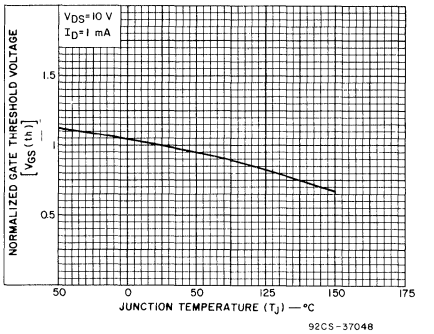


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

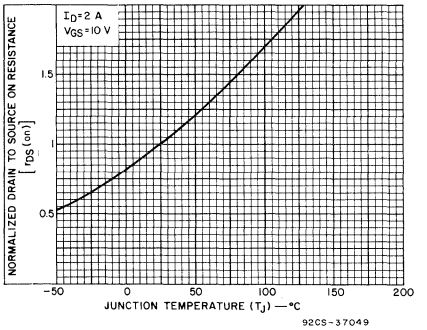


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

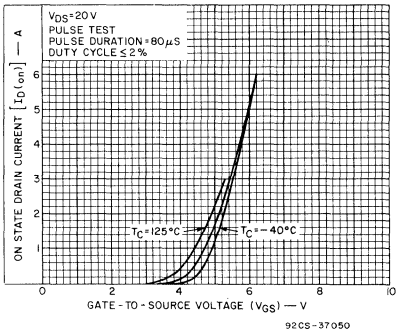


Fig. 5 — Typical transfer characteristics for all types.

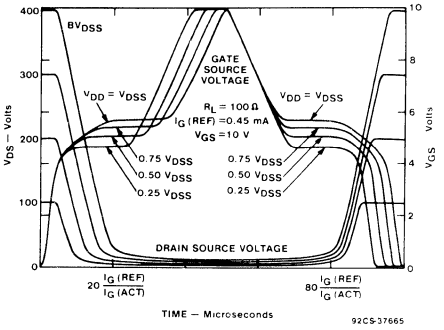


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

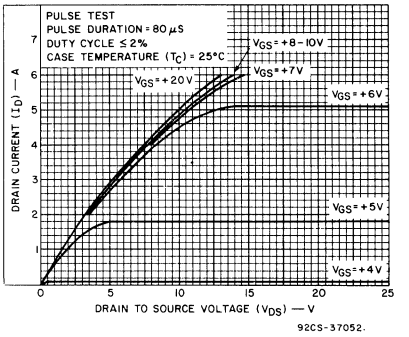


Fig. 7 — Typical saturation characteristics for all types.

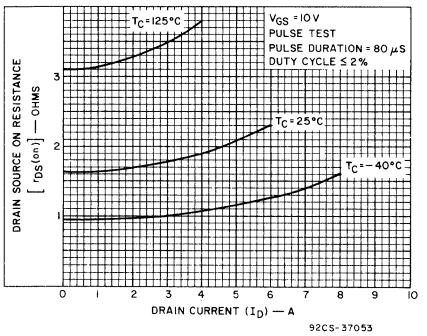


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

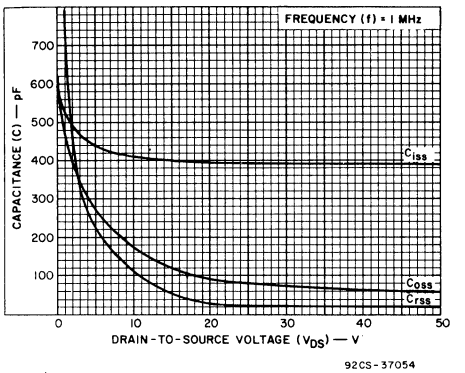


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

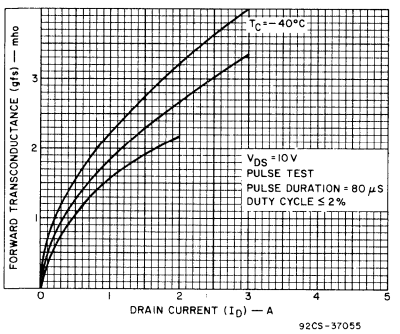


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

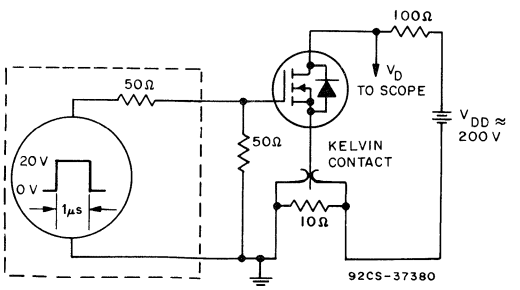


Fig. 11 — Switching Time Test Circuit

RFM6N45, RFM6N50, RFP6N45, RFP6N50

File Number **1494**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

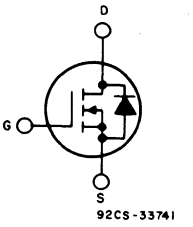
6 A, 450 V and 500 V

$r_{DS}(on)$ = 1.25Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

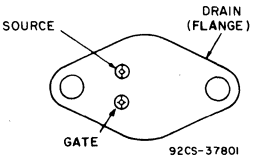
The RFM6N45 and RFM6N50 and the RFP6N45 and RFP6N50* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9191 and TA9231, respectively.

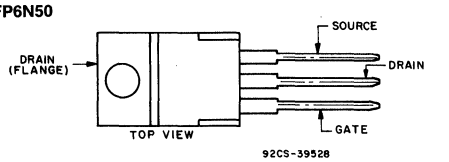
TERMINAL DESIGNATIONS

RFM6N45
RFM6N50



JEDEC TO-204AA

RFP6N45
RFP6N50



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM6N45	RFM6N50		RFP6N45	RFP6N50	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	450	500		450	500	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	450	500		450	500	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			6			A
Pulsed ..... I_{DM}			15			A
POWER DISSIPATION @ T_C=25°C ..... P_T	100	100		75	75	W
Derate above T_C=25°C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM6N45, RFM6N50, RFP6N45, RFP6N50

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=360 V V_{DS}=400 V	— —	10 —	— —	— 10	μA
		T_C=125° C V_{DS}=360 V V_{DS}=400 V	— —	50 —	— —	— 50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	4.5	—	4.5	V
		I_D=6 A V_{GS}=10 V	—	12	—	12	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=10 V	—	1.25	—	1.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	250	—	250	
Reverse Transfer Capacitance	C_{rss}	f=1 MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 250 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r	I_D=3 A	40(typ)	80	40(typ)	80	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	190(typ)	300	190(typ)	300	
Fall Time	t_f	V_{GS}=10 V	60(typ)	100	60(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6N45, RFM6N50	—	1.25	—	1.25	°C/W
		RFP6N45, RFP6N50	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6N45 RFP6N45		RFM6N50 RFP6N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} [a]	I_{SD} = 3A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	800(typ.)		800(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM6N45, RFM6N50, RFP6N45, RFP6N50

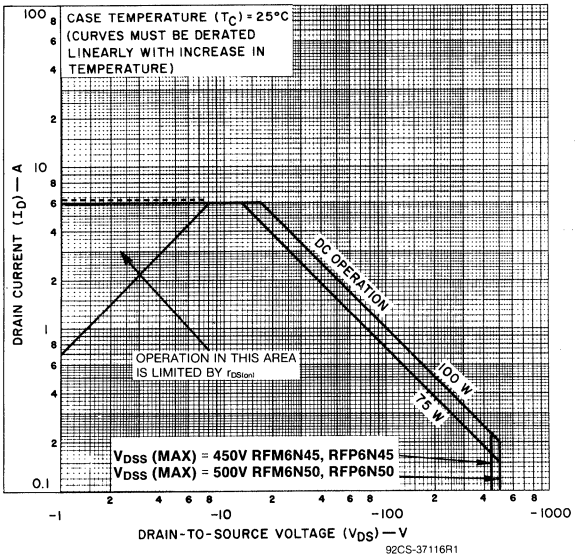


Fig. 1 — Maximum operating areas for all types.

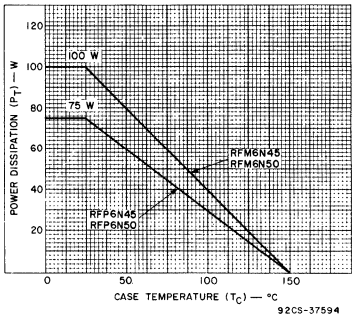


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

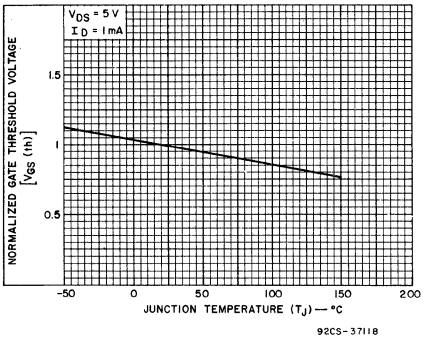


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

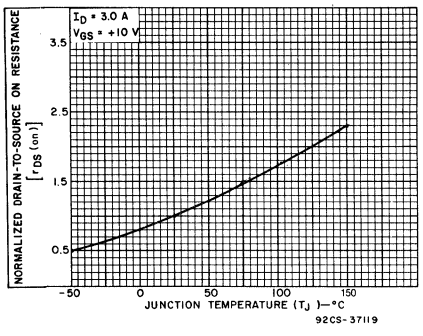


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

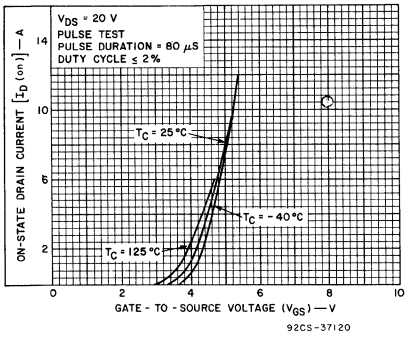


Fig. 5 — Typical transfer characteristics for all types.

RFM6N45, RFM6N50, RFP6N45, RFP6N50

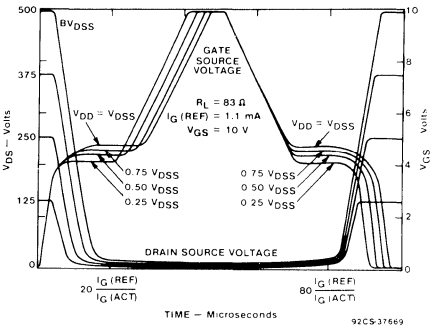


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

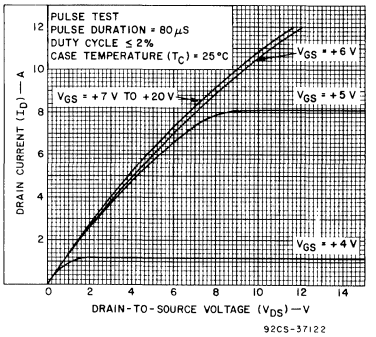


Fig. 7 — Typical saturation characteristics for all types.

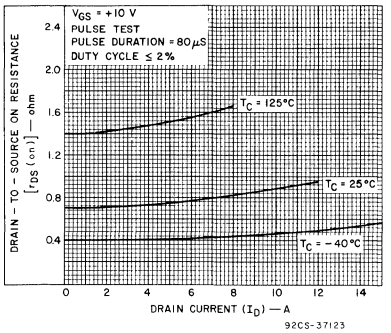


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

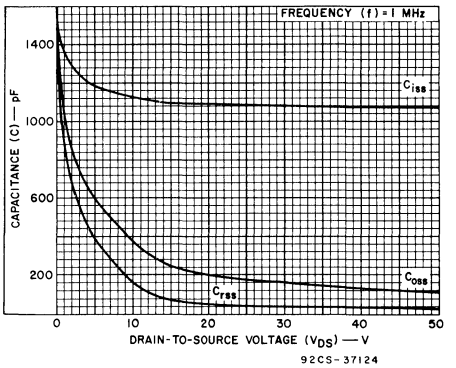


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

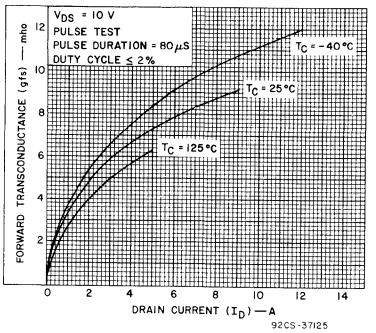


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

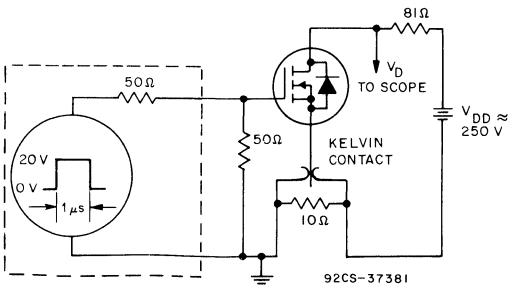


Fig. 11 — Switching Time Test Circuit.

RFM7N35, RFM7N40, RFP7N35, RFP7N40

File Number **1536**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

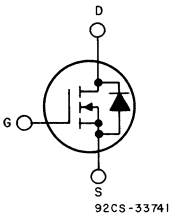
7 A, 350 V and 400 V

$r_{DS}(on)$: 0.75Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

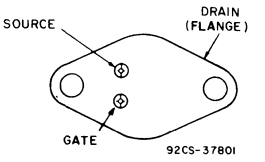
The RFM7N35 and RFM7N40 and the RFP7N35 and RFP7N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9397 and TA9398, respectively.

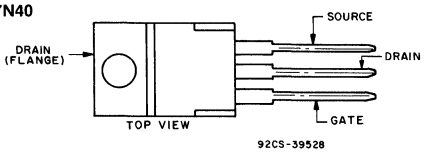
TERMINAL DESIGNATIONS

RFM7N35
RFM7N40



JEDEC TO-204AA

RFP7N35
RFP7N40



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C=25°C):

	RFM7N35	RFM7N40		RFP7N35	RFP7N40	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	350	400		350	400	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)..... V_{DGR}	350	400		350	400	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT						
Rms Continuous ..... I_D			7			A
Pulsed ..... I_{DM}			15			A
POWER DISSIPATION @ T_C=25°C ..... P_T	100	100		75	75	W
Derate above T_C=25°C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM7N35, RFM7N40, RFP7N35, RFP7N40

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25° C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	400	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=280 V	—	1	—	—	μA
		V_{DS}=320 V	—	—	—	1	
		T_C=125° C V_{DS}=280 V	—	50	—	—	
		V_{DS}=320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3.5 A V_{GS}=10 V	—	3.5	—	3.5	V
		I_D=7 A V_{GS}=10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3.5 A V_{GS}=10 V	—	0.75	—	0.75	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f= 1 MHz	—	1600	—	1600	pF
Output Capacitance	C_{oss}		—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}		—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DS}=200 V I_D=3.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	16(typ)	45	16(typ)	45	ns
Rise Time	t_r		54(typ)	75	54(typ)	75	
Turn-Off Delay Time	$t_d(off)$		170(typ)	250	170(typ)	250	
Fall Time	t_f		62(typ)	100	62(typ)	100	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM7N35, RFM7N40	—	1.25	—	1.25	°C/W
		RFP7N35, RFP7N40	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM7N35 RFP7N35		RFM7N40 RFP7N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=3.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A di_F/dt=100 A/μs	870 (typ)				ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFM7N35, RFM7N40, RFP7N35, RFP7N40

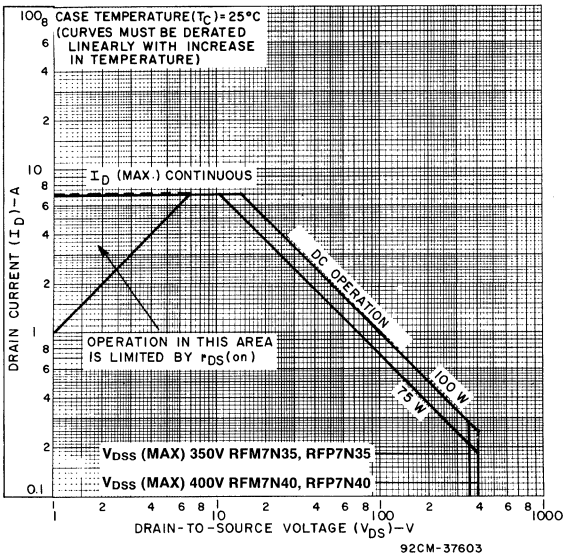


Fig. 1 - Maximum safe operating areas for all types.

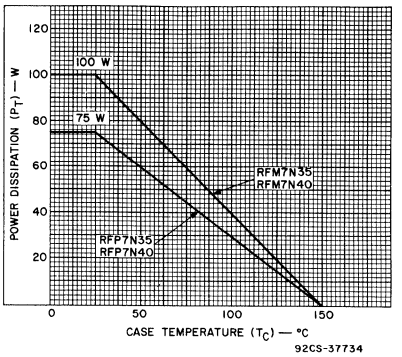


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

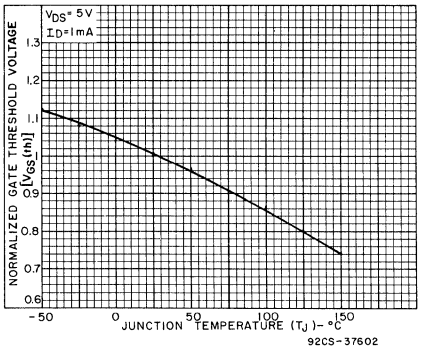


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

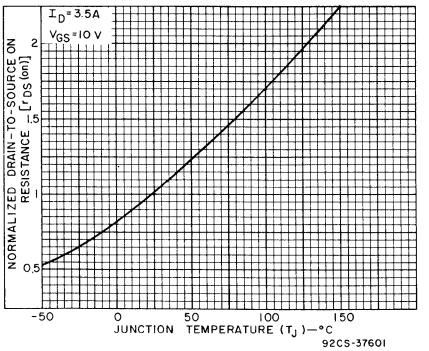


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

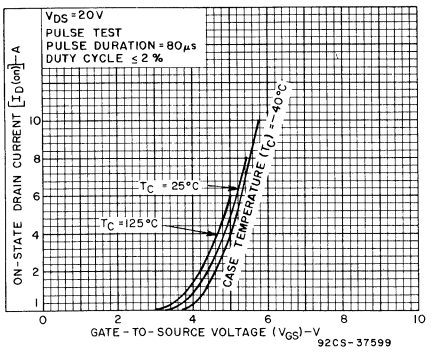


Fig. 5 - Typical transfer characteristics for all types.

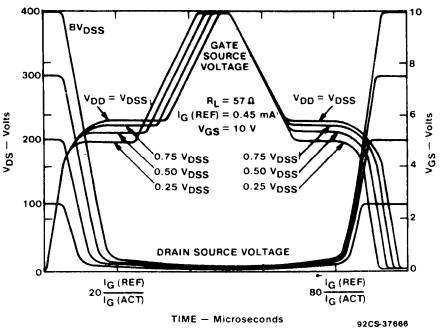


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

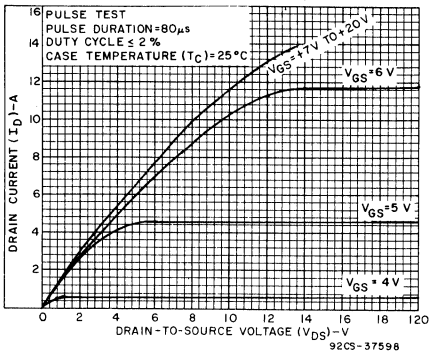


Fig. 7 - Typical saturation characteristics for all types.

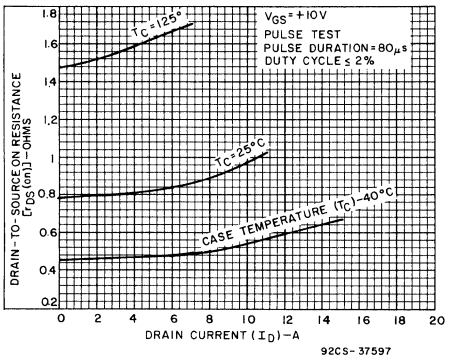


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

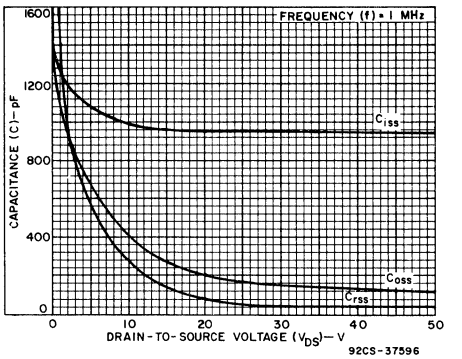


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

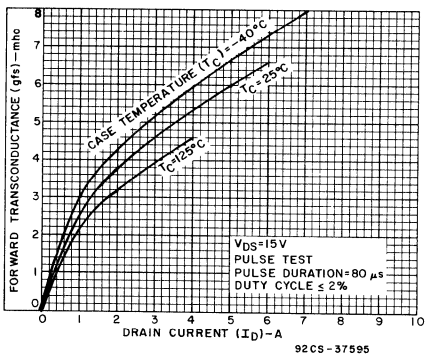


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

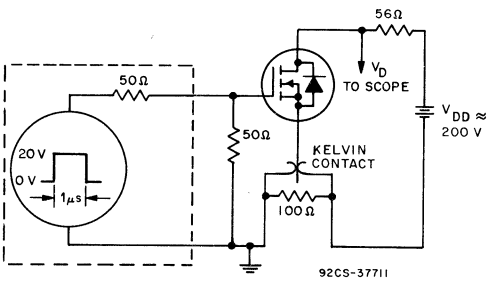


Fig. 11 - Switching time test circuit.

RFM8N18, RFM8N20, RFP8N18, RFP8N20

File Number **1447**

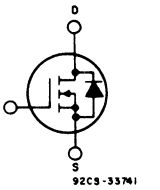
N-Channel Enhancement-Mode Power Field-Effect Transistors

8 A, 180 V — 200 V

$r_{DS}(on)$: 0.5 Ω

Features:

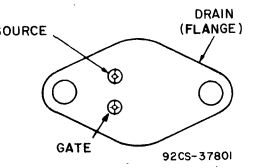
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

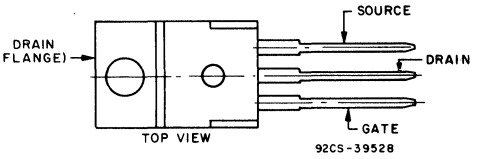
TERMINAL DESIGNATIONS

RFM8N18
RFM8N20



JEDEC TO-204AA

RFP8N18
RFP8N20



JEDEC TO-220AB

The RFM8N18 and RFM8N20 and the RFP8N18 and RFP8N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9291 and TA9292, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFM8N18	RFM8N20	RFP8N18	RFP8N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	180	200	V
DRAIN-GATE VOLTAGE (R_{GS} = 1MΩ)	V_{DGR}	180	200	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	8				A
Pulsed	I_{DM}	20				A
POWER DISSIPATION						
@ T_C = 25°C	P_T	75	75	60	60	W
Derate above T_C = 25°C		0.6	0.6	0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150				°C

RFM8N18, RFM8N20, RFP8N18, RFP8N20

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM8N18 RFP8N18 MIN.	LIMITS RFM8N18 RFP8N18 MAX.	LIMITS RFM8N20 RFP8N20 MIN.	LIMITS RFM8N20 RFP8N20 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145 V	—	1	—	—	μA
		V_{DS} = 160 V	—	—	—	1	
		T_C = 125°C, V_{DS} = 145 V	—	50	—	—	
		T_C = 125°C, V_{DS} = 160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 4 A, V_{GS} = 10 V	—	2.0	—	2.0	V
		I_D = 8 A, V_{GS} = 10 V	—	5.5	—	5.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 4 A, V_{GS} = 10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 4 A	1.5	—	1.5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	—	750	—	750	pF
Output Capacitance	C_{oss}		—	250	—	250	
Reverse Transfer Capacitance	C_{rss}		—	70	—	70	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 100 V, I_D = 4 A, R_{gen} = R_{gs} = 50 Ω, V_{GS} = 10 V	30(typ.)	45	30(typ.)	45	ns
Rise Time	t_r		100(typ.)	150	100(typ.)	150	
Turn-Off Delay Time	$t_d(off)$		90(typ.)	135	90(typ.)	135	
Fall Time	t_f		70(typ.)	105	70(typ.)	105	
Thermal Resistance Junction-to-Case	$R\theta JC$	RFM8N18, RFM8N20	—	1.67	—	1.67	°C/W
		RFP8N18, RFP8N20	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM8N18 RFP8N18 Min.	LIMITS RFM8N18 RFP8N18 Max.	LIMITS RFM8N20 RFP8N20 Min.	LIMITS RFM8N20 RFP8N20 Max.	UNITS
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	225(typ.)		225(typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM8N18, RFM8N20, RFP8N18, RFP8N20

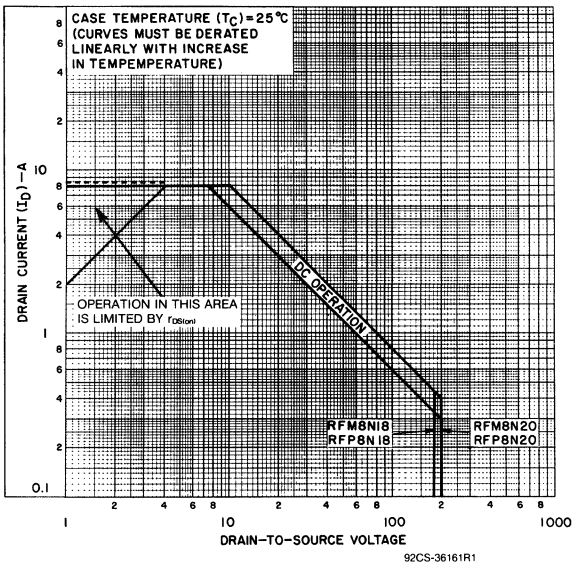


Fig. 1 — Maximum safe operating areas for all types.

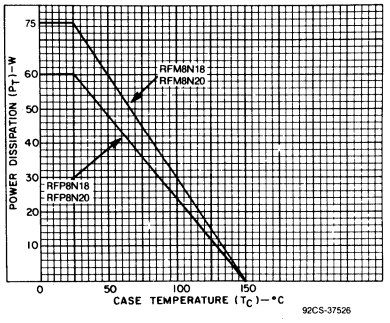


Fig. 2 — Power vs. temperature derating curve for all types.

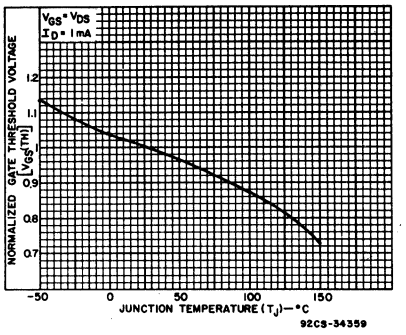


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

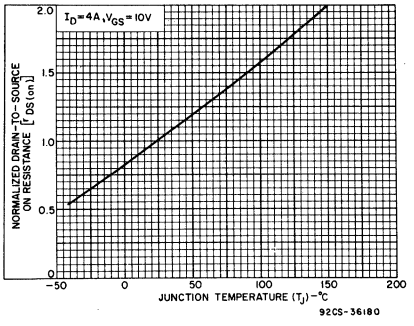


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

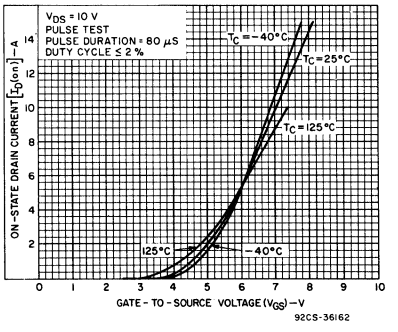


Fig. 5 — Typical transfer characteristics for all types.

RFM8N18, RFM8N20, RFP8N18, RFP8N20

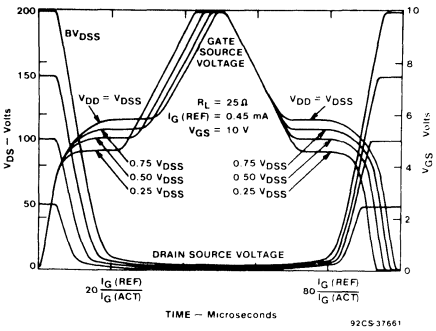


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

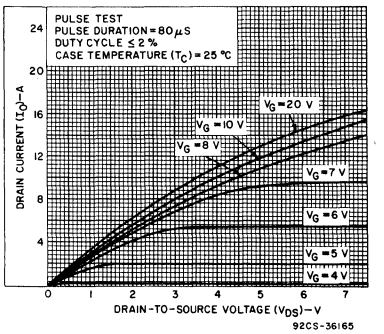


Fig. 7 — Typical saturation characteristics for all types.

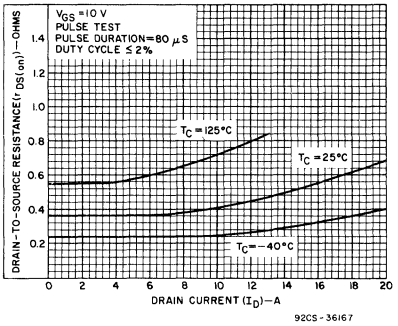


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

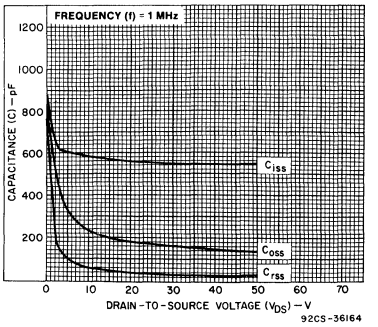


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

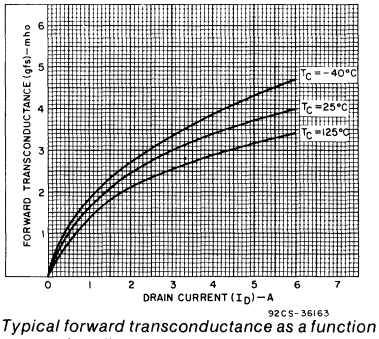


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

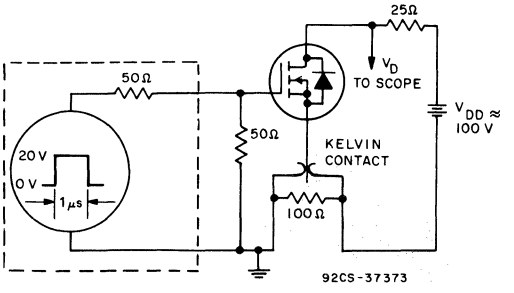


Fig. 11 — Switching Time Test Circuit.

RFM10N12, RFM10N15, RFP10N12, RFP10N15

File Number **1445**

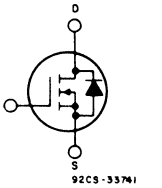
N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 120 V — 150 V

$r_{DS}(on)$: 0.3 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

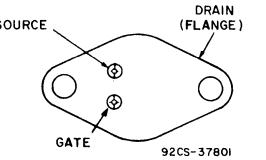
The RFM10N12 and RFM10N15 and the RFP10N12 and RFP10N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9192 and TA9212, respectively.

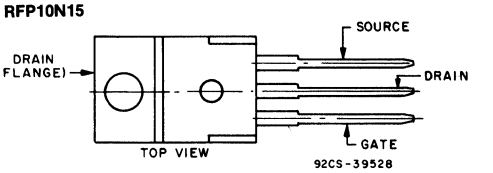
TERMINAL DESIGNATIONS

RFM10N12
RFM10N15



JEDEC TO-204AA

RFP10N12
RFP10N15



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM10N12	RFM10N15		RFP10N12	RFP10N15	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			10			A
Pulsed ..... I_{DM}			25			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM10N12, RFM10N15, RFP10N12, RFP10N15

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM10N12 RFP10N12 MIN.	LIMITS RFM10N12 RFP10N12 MAX.	LIMITS RFM10N15 RFP10N15 MIN.	LIMITS RFM10N15 RFP10N15 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 100 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	1.5	—	1.5	V
		I_D = 10 A, V_{GS} = 10 V	—	4	—	4	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5 A, V_{GS} = 10 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	650	—	650	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	230	—	230	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	60	—	60	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V	40(typ.)	60	40(typ.)	60	ns
Rise Time	t_r	I_D = 5 A	165(typ.)	250	165(typ.)	250	
Turn-Off Delay Time	$t_d(off)$	R_{gen} = R_{gs} = 50 Ω	90(typ.)	135	90(typ.)	135	
Fall Time	t_f	V_{GS} = 10 V	90(typ.)	135	90(typ.)	135	
Thermal Resistance Junction-to-Case	RθJC	RFM10N12, RFM10N15	—	1.67	—	1.67	°C/W
		RFP10N12, RFP10N15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM10N12 RFP10N12 MIN.	LIMITS RFM10N12 RFP10N12 MAX.	LIMITS RFM10N15 RFP10N15 MIN.	LIMITS RFM10N15 RFP10N15 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFM10N12, RFM10N15, RFP10N12, RFP10N15

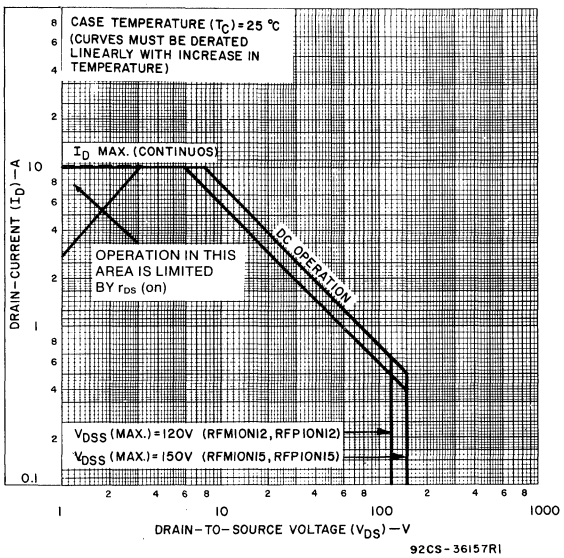


Fig. 1 — Maximum safe operating areas for all types.

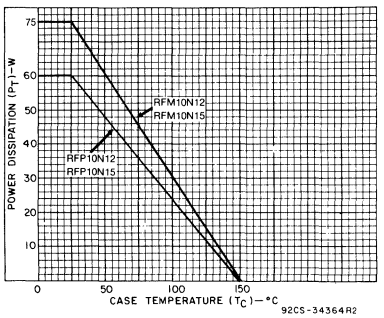


Fig. 2 — Power vs. temperature derating curve for all types.

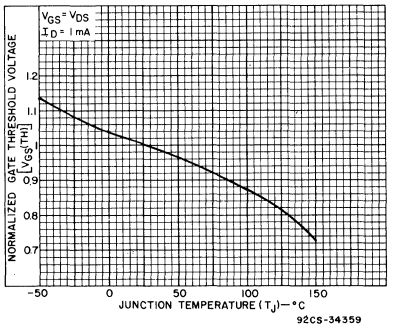


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

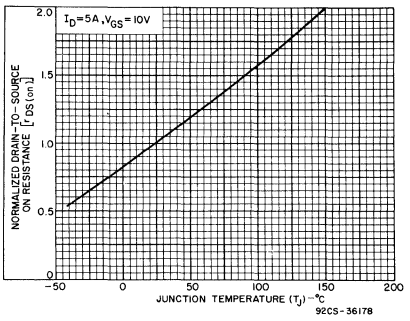


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

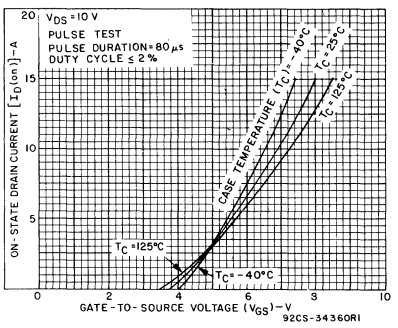


Fig. 5 — Typical transfer characteristics for all types.

RFM10N12, RFM10N15, RFP10N12, RFP10N15

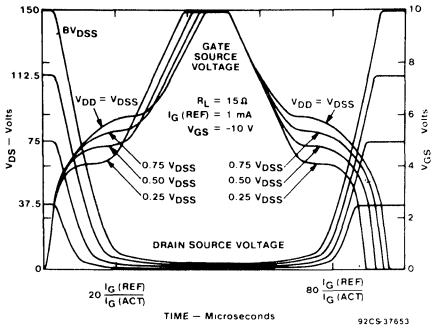


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

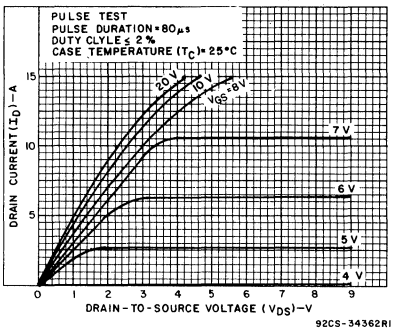


Fig. 7 — Typical saturation characteristics for all types.

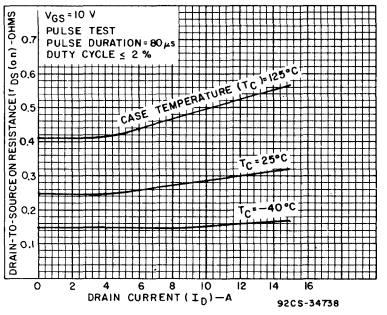


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

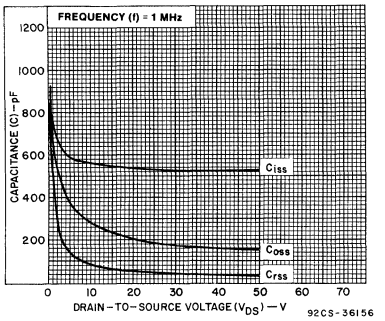


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

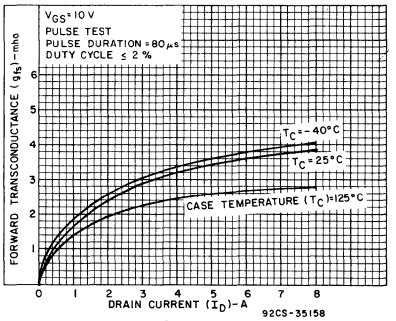


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

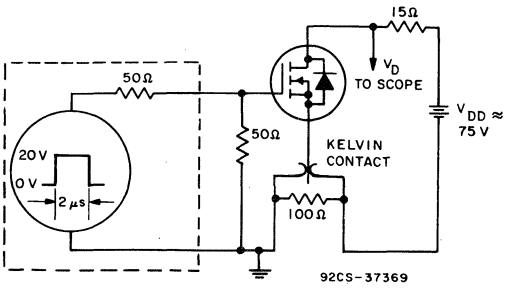


Fig. 11 — Switching Time Test Circuit

RFH10N45, RFH10N50

File Number **1629**

Power MOS Field-Effect Transistors

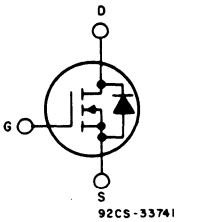
N-Channel Enhancement-Mode Power Field-Effect Transistors

10 A, 450 V - 500 V
$r_{DS(on)}$ = 0.6 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



92CS-33741

N-CHANNEL ENHANCEMENT MODE

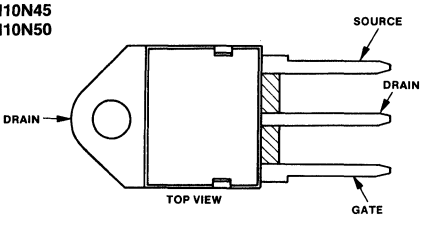
The RFH10N45 and RFH10N50* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH10N45 and RFH10N50 types were formerly RCA developmental numbers TA9579A and TA9579B respectively.

TERMINAL DESIGNATIONS

RFH10N45
RFH10N50



92CS-39967

JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		RFH10N45	RFH10N50	
DRAIN-SOURCE VOLTAGE	V_{DSS}	450	500	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	450	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	10		A
Pulsed	I_{DM}	20		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V V_{DS} = 400 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 360 V V_{DS} = 400 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	600	—	600	pF
Reverse Transfer Capacitance	C_{rss}		—	200	—	200	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 250 V I_D = 5 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	26(typ)	60	26(typ)	60	ns
Rise Time	t_r		50(typ)	100	50(typ)	100	ns
Turn-Off Delay Time	$t_d(off)$		525(typ)	900	525(typ)	900	ns
Fall Time	t_f		105(typ)	180	105(typ)	180	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH10N45, RFH10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH10N45		RFH10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH10N45, RFH10N50

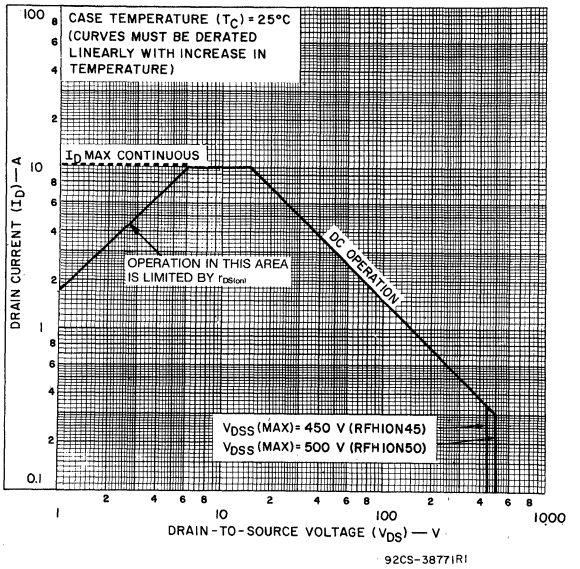


Fig. 1 - Maximum safe operating areas for all types.

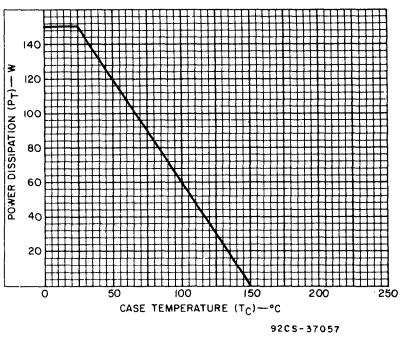


Fig. 2 - Power vs. temperature derating curve for all types.

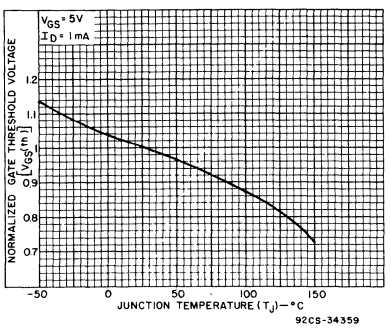


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

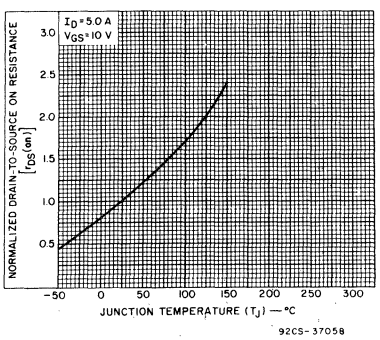


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

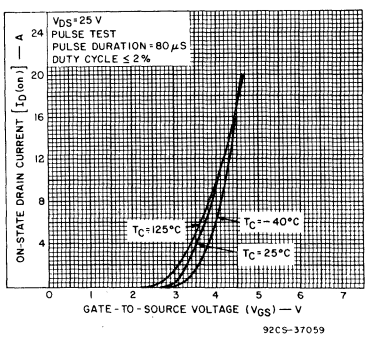


Fig. 5 - Typical transfer characteristics for all types.

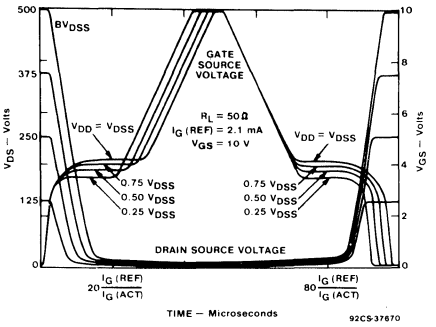


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

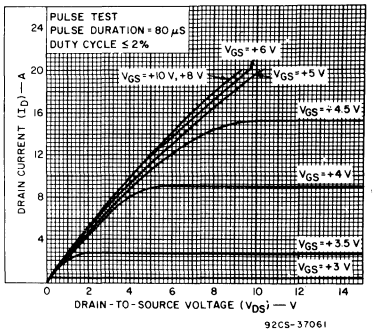


Fig. 7 - Typical saturation characteristics for all types.

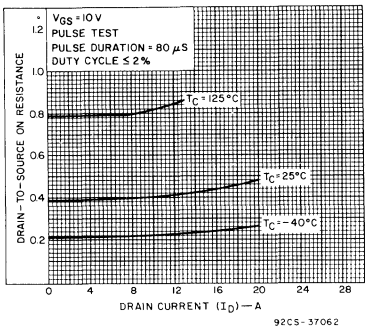


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

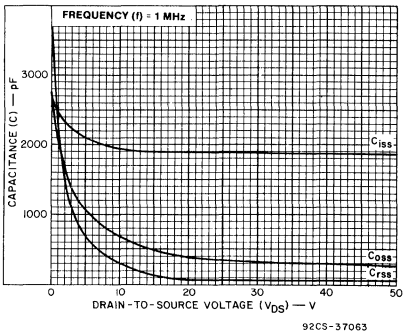


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

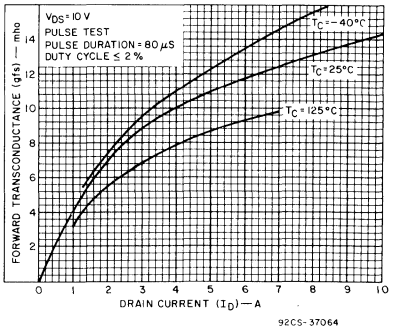


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

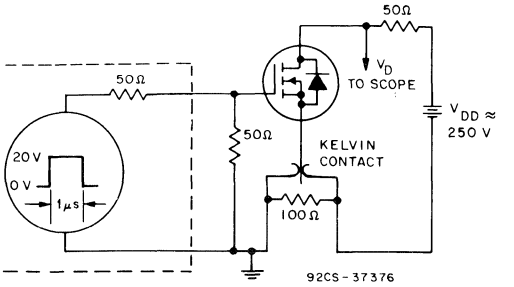


Fig. 11 - Switching Time Test Circuit.

RFM10N45, RFM10N50

File Number **1788**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

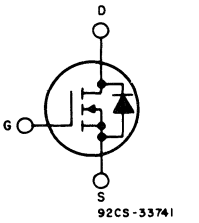
10 A, 450 V - 500 V

$r_{DS(on)}$: 0.6 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

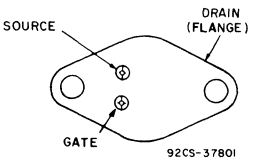
The RFM10N45 and RFM10N50* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package.

*The RFM10N45 and RFM10N50 types were formerly RCA developmental numbers TA9189A and TA9189B, respectively.

TERMINAL DESIGNATION

RFM10N45
RFM10N50



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFM10N45	RFM10N50	
DRAIN-SOURCE VOLTAGE	V_{DSS}	450	500	V
DRAIN-GATE VOLTAGE, R_{GS} = 1 MΩ	V_{DGR}	450	500	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	10		A
Pulsed	I_{DM}	20		A
POWER DISSIPATION @ T_C = 25°C	P_T	150		W
Derate above T_C = 25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFM10N45, RFM10N50

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	450	—	500	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 360 V	—	1	—	—	μA
		V_{DS} = 400 V	—	—	—	1	
		T_C = 125°C V_{DS} = 360 V	—	50	—	—	
		V_{DS} = 400 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 5 A V_{GS} = 10 V	—	3.0	—	3.0	V
		I_D = 10 A V_{GS} = 10 V	—	10	—	10	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 5A V_{GS} = 10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	600	—	600	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	200	—	200	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 250	26(typ)	60	26(typ)	60	ns
Rise Time	t_r	I_D = 5 A	50(typ)	100	50(typ)	100	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	525(typ)	900	525(typ)	900	
Fall Time	t_f	V_{GS} = 10 V	105(typ)	180	105(typ)	180	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N45, RFM10N50 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM10N45		RFM10N50		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFM10N45, RFM10N50

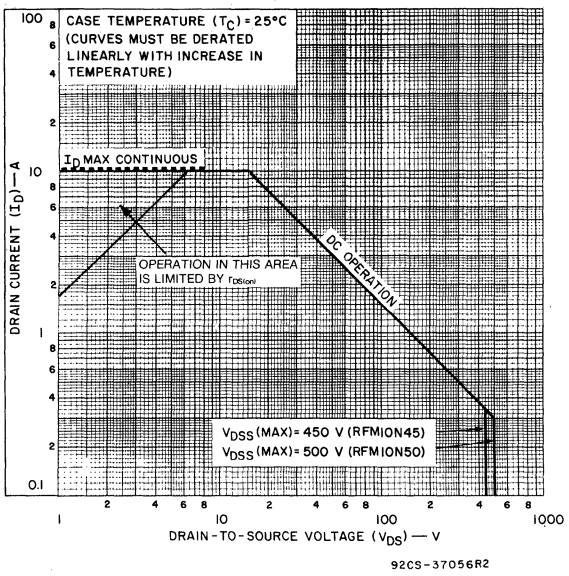


Fig. 1 - Maximum safe operating areas for all types.

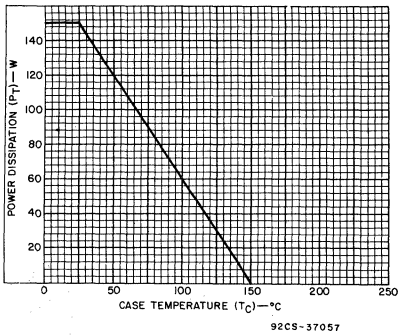


Fig. 2 - Power vs. temperature derating curve for all types.

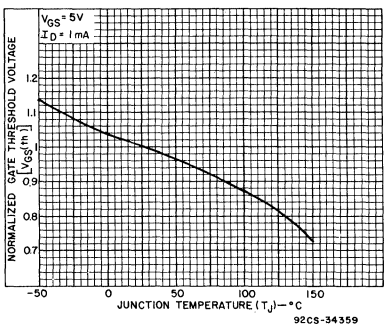


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

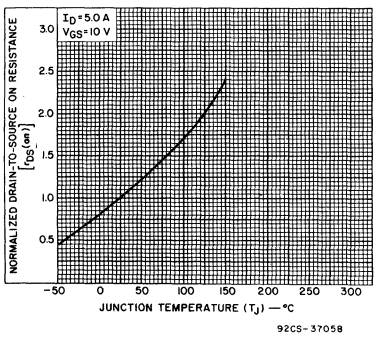


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

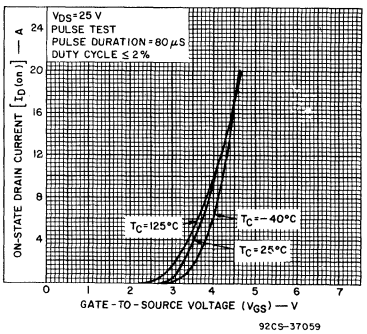


Fig. 5 - Typical transfer characteristics for all types.

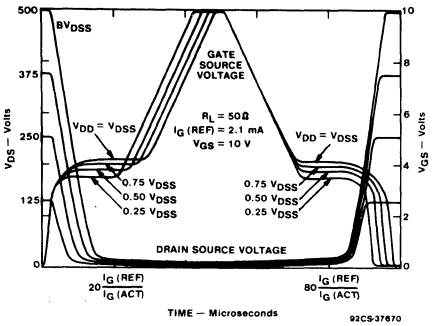


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

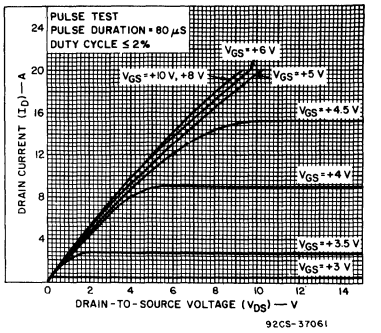


Fig. 7 - Typical saturation characteristics for all types.

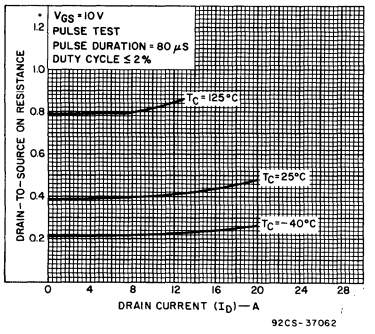


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

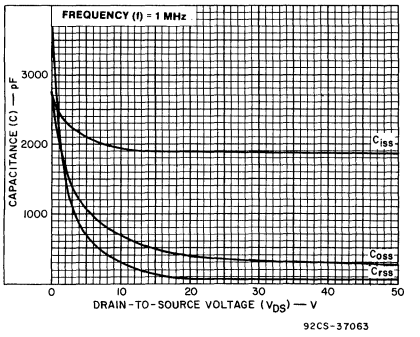


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

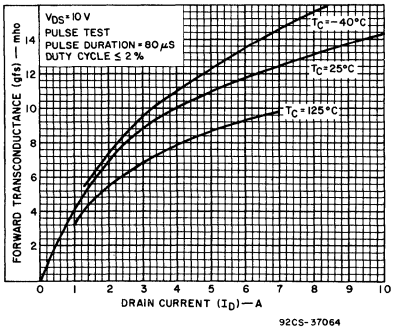


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

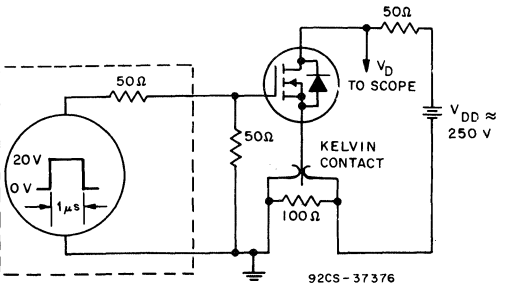


Fig. 11 - Switching Time Test Circuit.

RFM12N08, RFM12N10, RFP12N08, RFP12N10

File Number **1386**

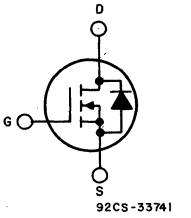
N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 80 and 100 V

$r_{DS\ (on)}$: 0.2 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

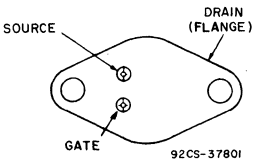
The RFM12N08 and RFM12N10 and the RFP12N08 and RFP12N10 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9284 and TA9285.

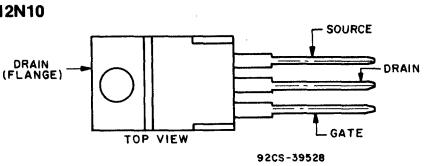
TERMINAL DESIGNATIONS

RFM12N08
RFM12N10



JEDEC TO-204AA

RFP12N08
RFP12N10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12N08	RFM12N10		RFP12N08	RFP12N10	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM12N08, RFM12N10, RFP12N08, RFP12N10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFP12N08		RFM12N10 RFP12N10		
			Min.	Max.	Min.	Max.	
Drain Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V	—	1	—	—	μA
		V_{DS}=80 V	—	—	—	1	
		T_C=125°C V_{DS}=65 V	—	50	—	—	
		V_{DS}=80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm$20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=10 V	—	3.3	—	3.3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	650	—	650	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	45(Typ)	70	45(Typ)	70	ns
Rise Time	t_r	I_D=6 A	250(Typ)	375	250(Typ)	375	
Turn-Off Delay Time	$t_d(off)$	$R_{gen}=R_{gs}$=50 Ω	85(Typ)	130	85(Typ)	130	
Fall Time	t_f	V_{GS}=10 V	100(Typ)	150	100(Typ)	150	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N08, RFM12N10	—	1.67	—	1.67	°C/W
		RFP12N08, RFP12N10	—	2.083	—	2.083	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08 RFM12N10		RFP12N08 RFP12N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM12N08, RFM12N10, RFP12N08, RFP12N10

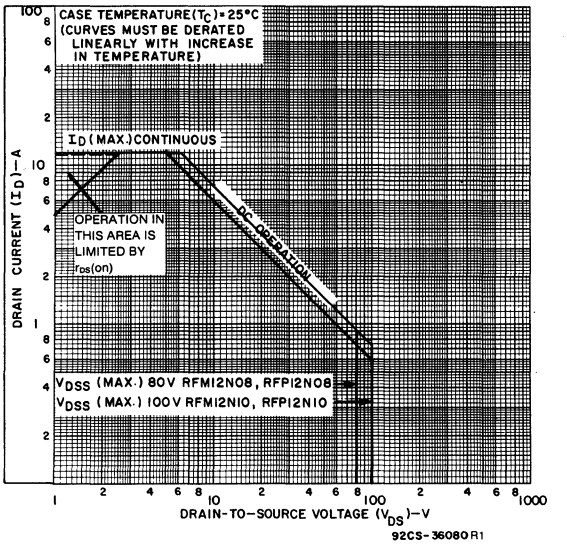


Fig. 1 - Maximum operating areas for all types.

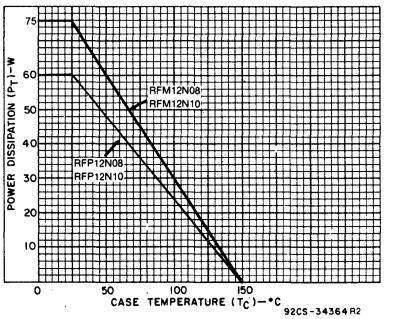


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

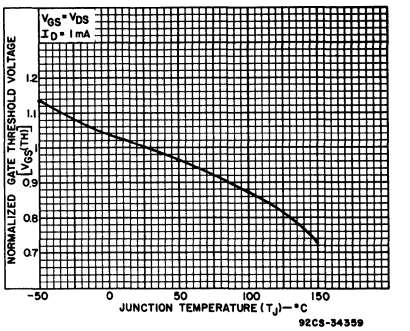


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

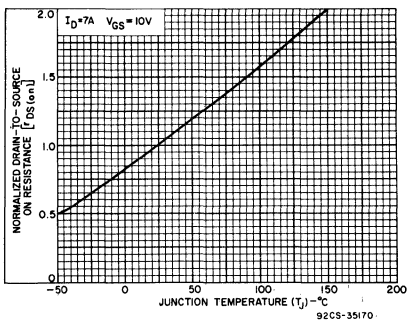


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

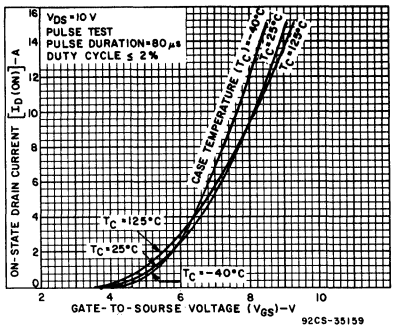


Fig. 5 - Typical transfer characteristics for all types.

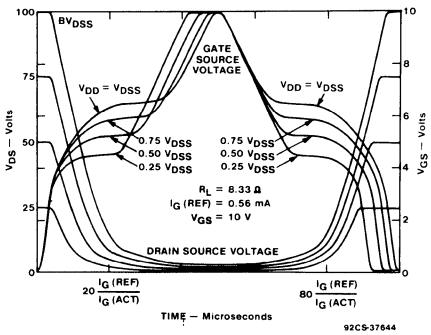


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

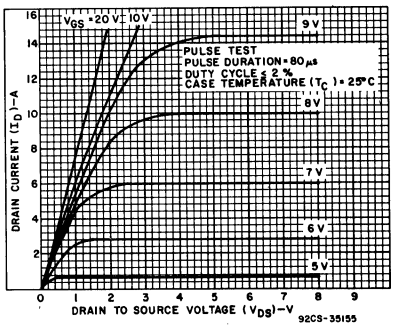


Fig. 7 - Typical saturation characteristics for all types.

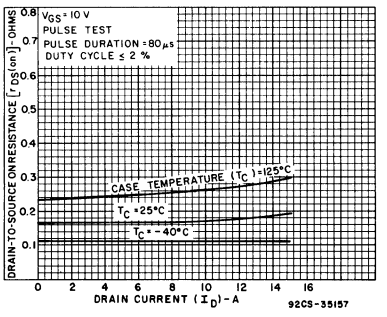


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

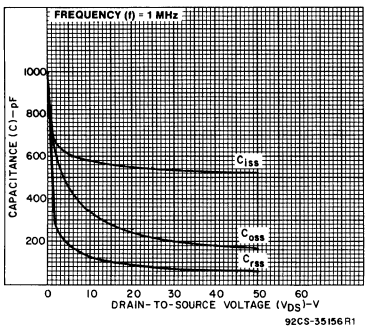


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

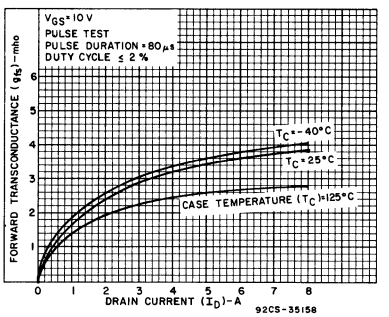


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

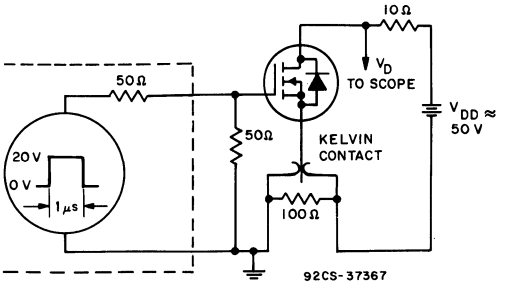


Fig. 11 — Switching Time Test Circuit

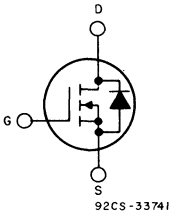
RFM12N18, RFM12N20, RFP12N18, RFP12N20

File Number **1461**

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, 180 and 200 V
$r_{DS}(on)$: 0.25 Ω

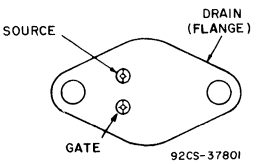
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

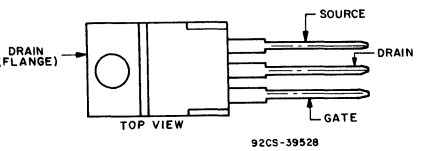
TERMINAL DESIGNATIONS

RFM12N18
RFM12N20



JEDEC TO-204AA

RFP12N18
RFP12N20



JEDEC TO-220AB

The RFM12N18 and RFM12N20 and the RFP12N18 and RFP12N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9293 and TA9294, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12N18	RFM12N20		RFP12N18	RFP12N20	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) .. V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT						
RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION						
@ T_C=25° C ..... P_T	100	100		75	75	W
Derate above T_C=25° C	0.8	0.8		0.6	0.6	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM12N18, RFM12N20, RFP12N18, RFP12N20

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V	—	1	—	—	μA
		V_{DS}=160 V	—	—	—	1	
		T_C=125°C V_{DS}=145 V	—	50	—	—	
		V_{DS}=160 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	1.5	—	1.5	V
		I_D=12 A V_{GS}=10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=10 V	—	0.25	—	0.25	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1700	—	1700	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	600	—	600	
Reverse-Transfer Capacitance	C_{rss}	f=1 MHz	—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r	I_D=6 A	130(typ)	200	130(typ)	200	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	120(typ)	180	120(typ)	180	
Fall Time	t_f	V_{GS}=10 V	105(typ)	160	105(typ)	160	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM12N18, RFM12N20	—	1.25	—	1.25	°C/W
		RFP12N18, RFP12N20	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N18 RFP12N18		RFM12N20 RFP12N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	325(typ)		325(typ)		ns

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

RFM12N18, RFM12N20, RFP12N18, RFP12N20

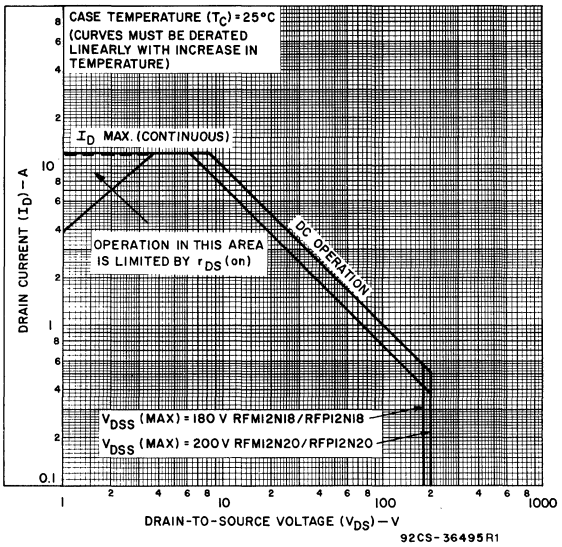


Fig. 1 - Maximum safe operating areas for all types.

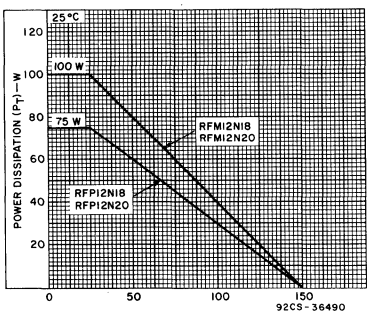


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

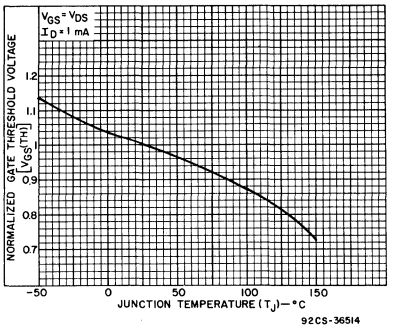


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

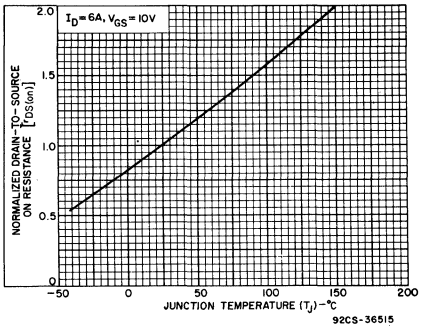


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

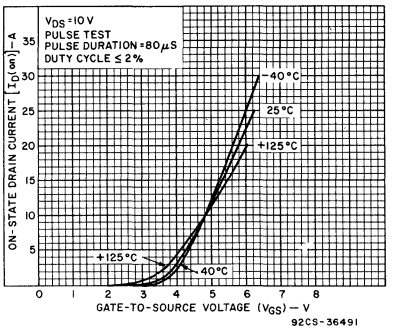


Fig. 5 - Typical transfer characteristics for all types.

RFM12N18, RFM12N20, RFP12N18, RFP12N20

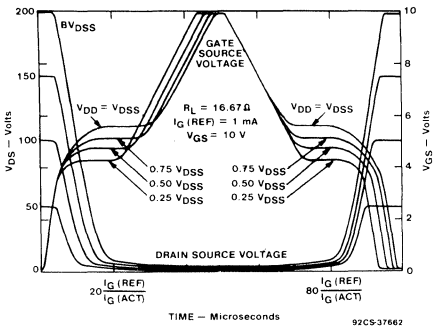


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

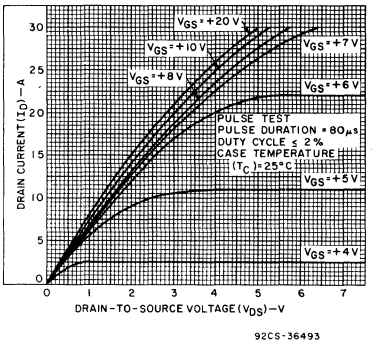


Fig. 7 - Typical saturation characteristics for all types.

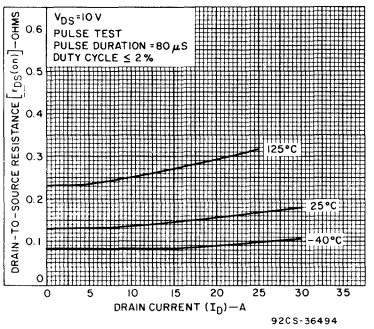


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

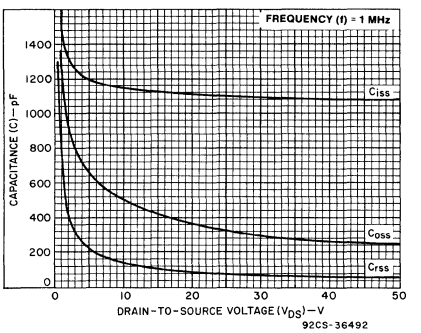


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

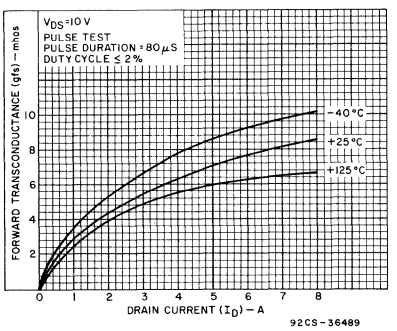


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

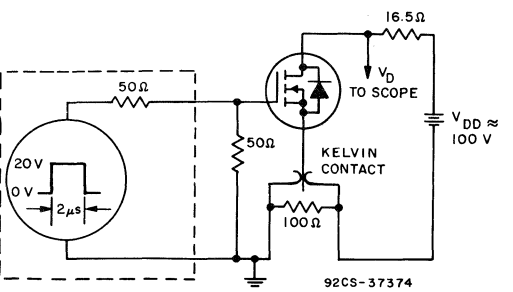


Fig. 11 — Switching Time Test Circuit

RFH12N35, RFH12N40

File Number **1630**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

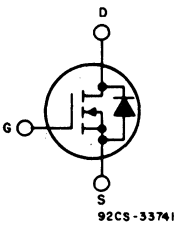
12 A, 350 V - 400 V

$r_{DS(on)}$ = 0.38 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



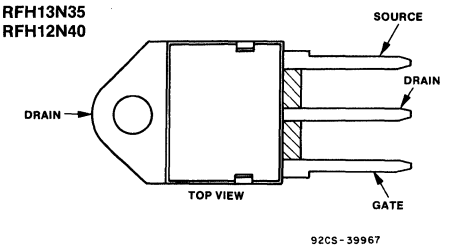
N-CHANNEL ENHANCEMENT MODE

The RFH12N35 and RFH12N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH12N35 and RFH12N40 types were formerly RCA developmental numbers TA9482A and TA9482B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH12N35	RFH12N40	
DRAIN-SOURCE VOLTAGE	V_{DSS}	350	400	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	350	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	12		A
Pulsed	I_{DM}	24		A
POWER DISSIPATION @ T_C = 25°C	P_T	150		W
Derate above T_C = 25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V V_{DS} = 320 V	— —	1 —	— —	— 1	μA
		T_C = 125°C V_{DS} = 280 V V_{DS} = 320 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	2.28	—	2.28	V
		I_D = 12 A V_{GS} = 10 V	—	6.75	—	6.75	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	0.38	—	0.38	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 200 V I_D = 6 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	30(typ)	50	30(typ)	50	ns
Rise Time	t_r		105(typ)	150	105(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		480(typ)	750	480(typ)	750	ns
Fall Time	t_f		140(typ)	200	140(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH12N35, RFH12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH12N35		RFH12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 6A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 (typ.)		950 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH12N35, RFH12N40

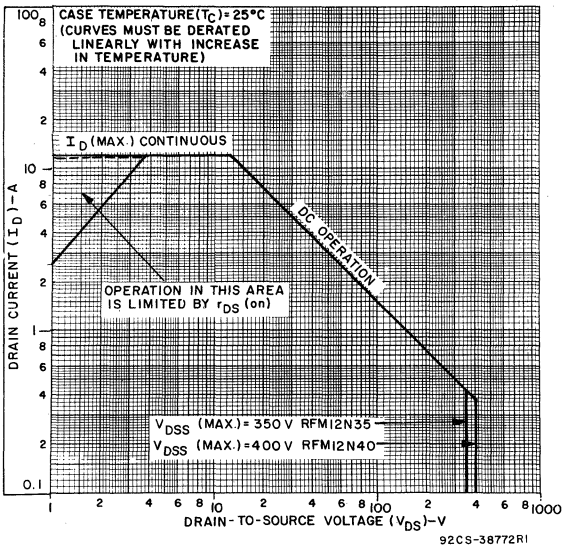


Fig. 1 - Maximum safe operating areas for all types.

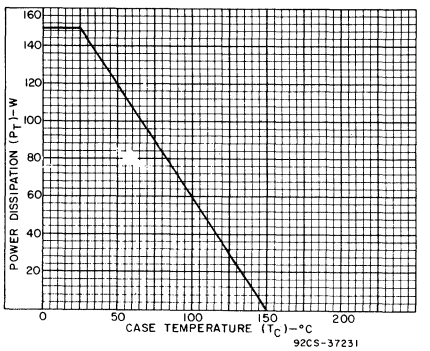


Fig. 2 - Power vs. temperature derating curve for all types.

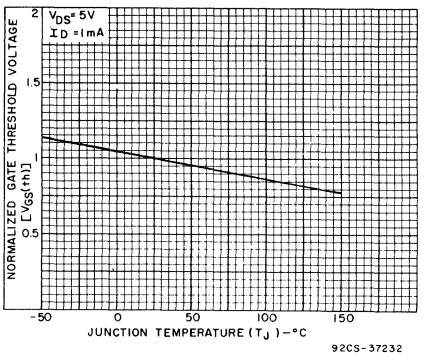


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

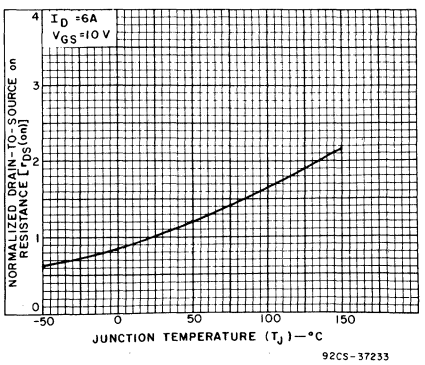


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

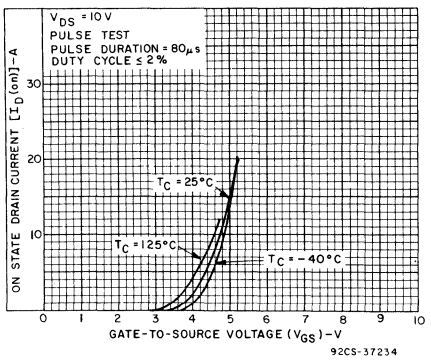


Fig. 5 - Typical transfer characteristics for all types.

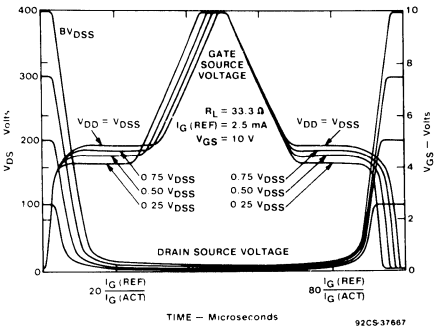


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

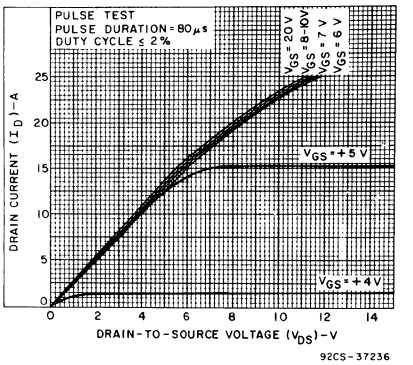


Fig. 7 - Typical saturation characteristics for all types.

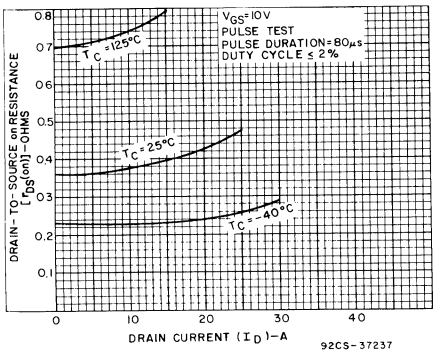


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

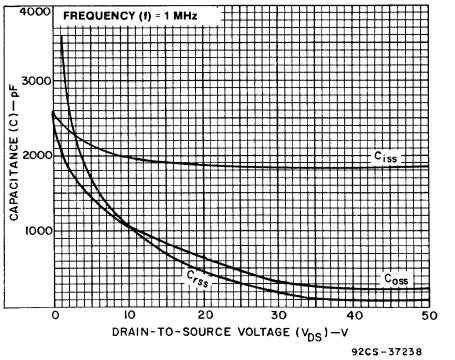


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

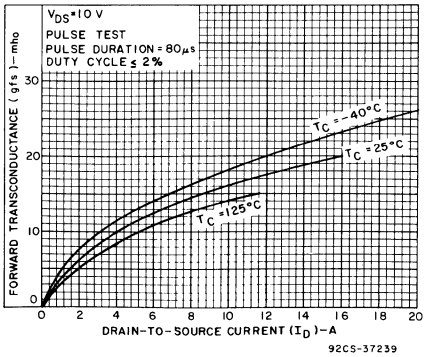


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

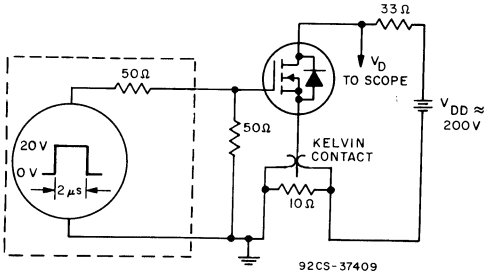


Fig. 11 - Switching Time Test Circuit.

RFM12N35, RFM12N40

File Number **1787**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

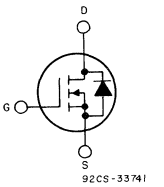
12A, 350 V - 400 V

$r_{DS(on)}$ = 0.38 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

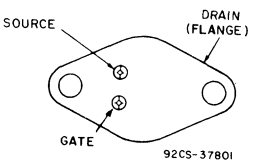
The RFM12N35 and RFM12N40* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package.

*The RFM12N35 and RFM12N40 types were formerly RCA developmental numbers TA9399A and TA9399B respectively.

TERMINAL DESIGNATION

RFM12N35
RFM12N40



JEDEC TO-204AA

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

		RFM12N35	RFM12N40	
DRAIN-SOURCE VOLTAGE	V_{DSS}	350	400	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	350	400	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	12		A
Pulsed	I_{DM}	24		A
POWER DISSIPATION[1] @ T_C = 25°C	P_T	150		W
Derate above T_C = 25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFM12N35, RFM12N40

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 10 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 280 V	—	1	—	—	μA
		V_{DS} = 320 V	—	—	—	1	
		T_C = 125°C V_{DS} = 280 V	—	50	—	—	
		V_{DS} = 320 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 6 A V_{GS} = 10 V	—	2.28	—	2.28	V
		I_D = 12 A V_{GS} = 10 V	—	6.75	—	6.75	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 6A V_{GS} = 10 V	—	0.38	—	0.38	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 6 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	900	—	900	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 200	30(typ)	50	30(typ)	50	ns
Rise Time	t_r	I_D = 6 A	105(typ)	150	105(typ)	150	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	480(typ)	750	480(typ)	750	
Fall Time	t_f	V_{GS} = 10 V	140(typ)	200	140(typ)	200	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12N35, RFM12N40 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFM12N35		RFM12N40		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 6A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	950 typ.		950 typ.		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFM12N35, RFM12N40

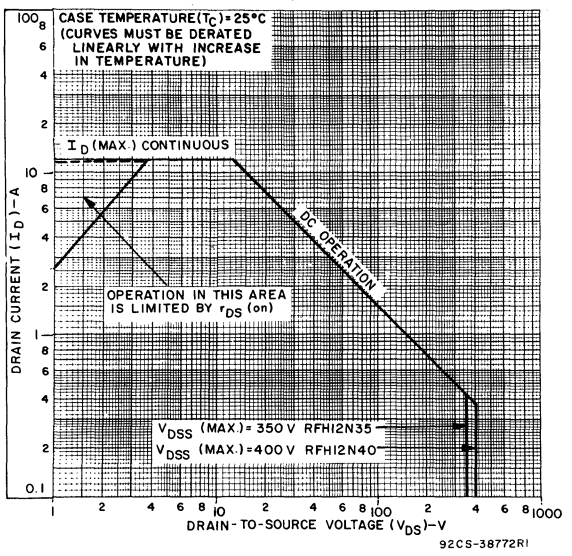


Fig. 1 - Maximum safe operating areas for all types.

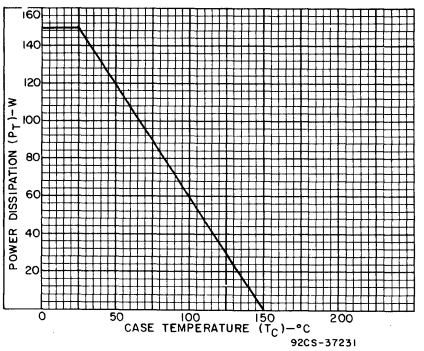


Fig. 2 - Power vs. temperature derating curve for all types.

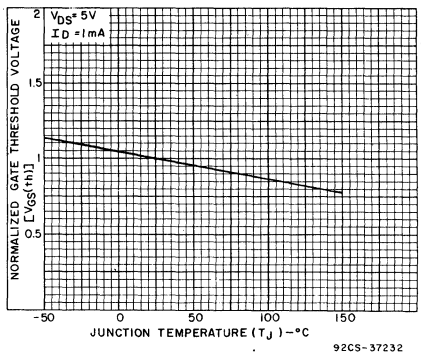


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

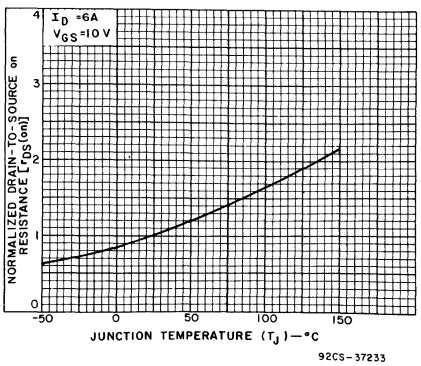


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

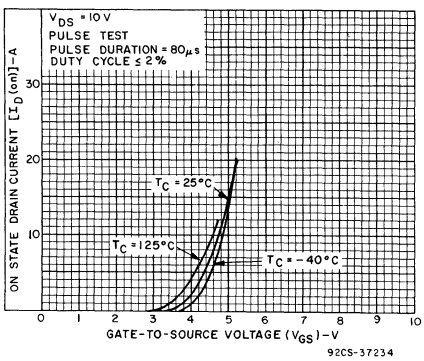


Fig. 5 - Typical transfer characteristics for all types.

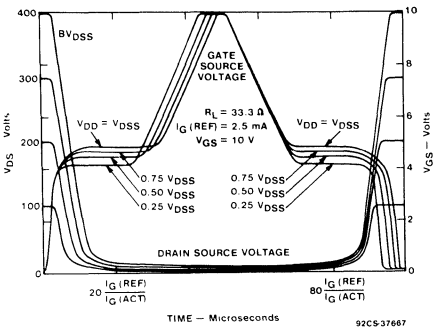


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

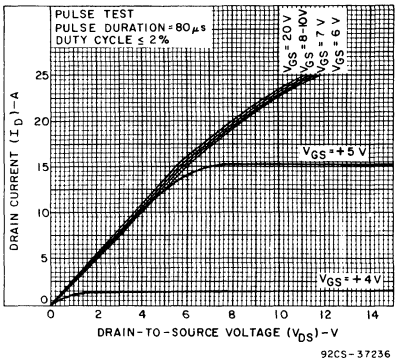


Fig. 7 - Typical saturation characteristics for all types.

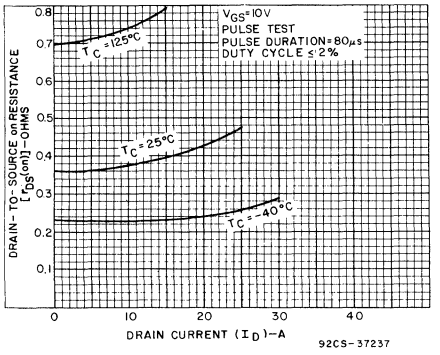


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

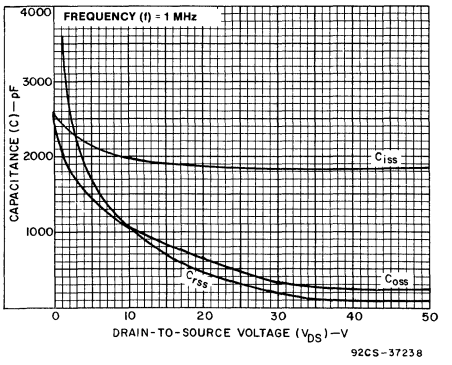


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

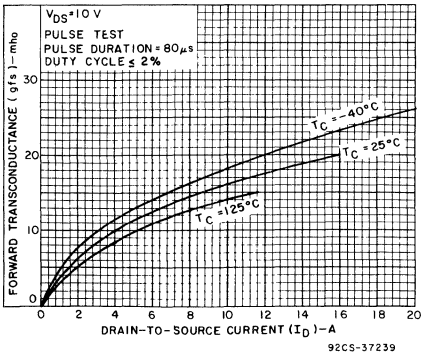


Fig. 10 - Typical forward transconductance as a function of drain for all types.

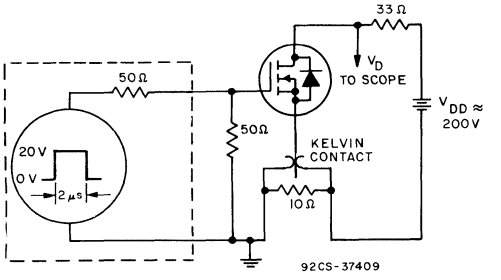


Fig. 11 - Switching Test Time Circuit.

RFM15N05, RFM15N06, RFP15N05, RFP15N06

File Number **1478**

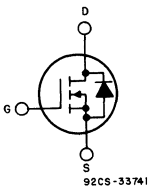
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

15 A, 50 and 60 V
$r_{DS}(on)$: 0.14 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

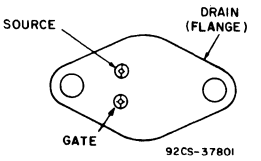
The RFM15N05 and RFM15N06 and the RFP15N05 and RFP15N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9382 and TA9383, respectively.

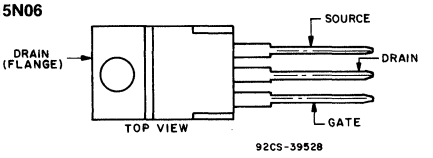
TERMINAL DESIGNATIONS

RFM15N05
RFM15N06



JEDEC TO-204AA

RFP15N05
RFP15N06



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM15N05	RFM15N06		RFP15N05	RFP15N06	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60		50	60	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) ... V_{DGR}	50	60		50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			15			A
Pulsed ..... I_{DM}			40			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM15N05, RFM15N06, RFP15N05, RFP15N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_c)=25°C unless otherwise specified*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V	—	1	—	—	μA
		V_{DS}=50 V	—	—	—	1	
		T_C=125°C V_{DS}=40 V	—	50	—	—	
		V_{DS}=50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=7.5 A V_{GS}=10 V	—	1.05	—	1.05	V
		I_D=15 A V_{GS}=10 V	—	2.5	—	2.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=7.5 A V_{GS}=10 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=7.5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	750	—	750	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	180	—	180	
Turn-On Delay Time	$t_d(on)$	V_{DD}=30 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r	I_D=7.5 A	100(typ)	175	100(typ)	175	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	72(typ)	175	72(typ)	175	
Fall Time	t_f	V_{GS}=10 V	66(typ)	140	66(typ)	140	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFM15N05, RFM15N06	—	1.67	—	1.67	°C/W
		RFP15N05, RFP15N06	—	2.083	—	2.083	

[a]Pulsed: Pulse duration=300 μs max., duty cycle=2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05 RFP15N05		RFM15N06 RFP15N06		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	100 (typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM15N05, RFM15N06, RFP15N05, RFP15N06

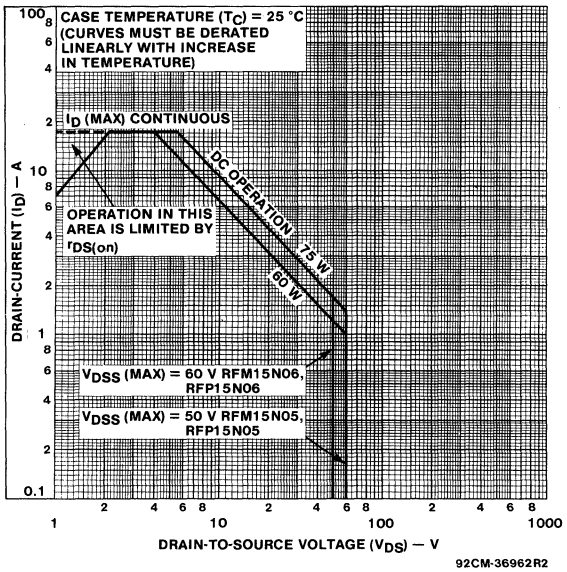


Fig. 1 - Maximum safe operating areas for all types.

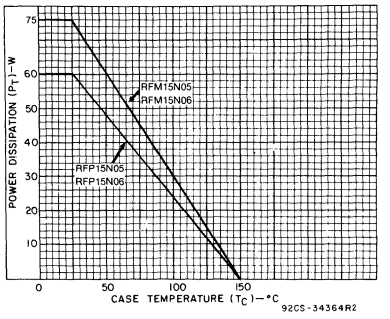


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

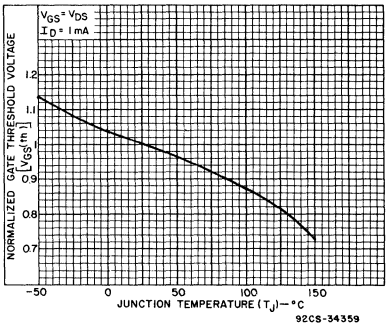


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

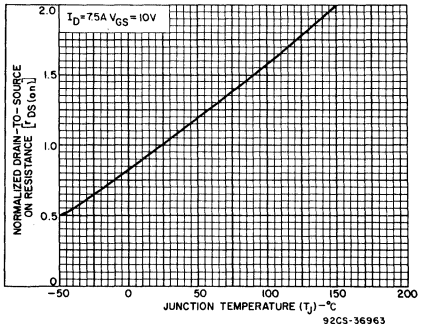


Fig. 4 - Normalized drain-to-source on resistance as a function of junction temperature for all types.

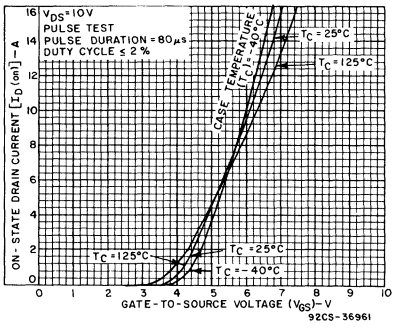


Fig. 5 - Typical transfer characteristics for all types.

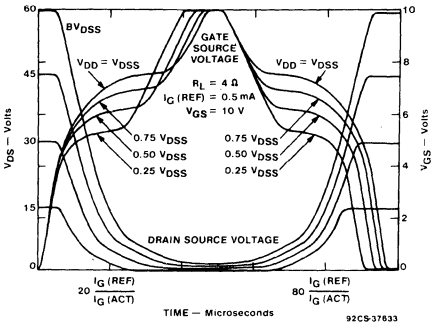


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

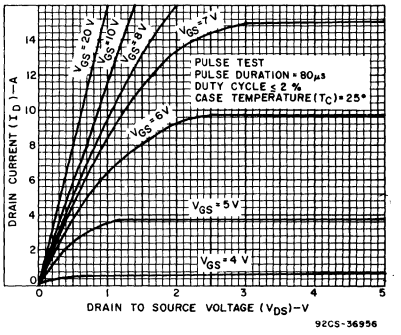


Fig. 7 - Typical saturation characteristics for all types.

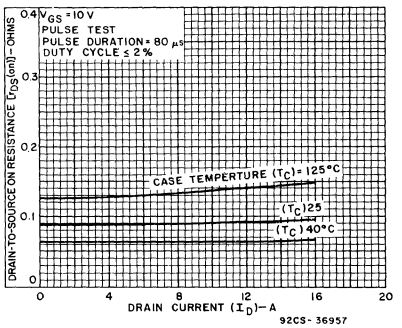


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

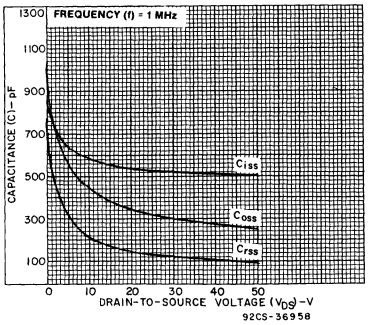


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

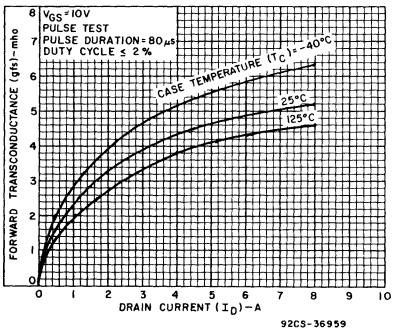


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

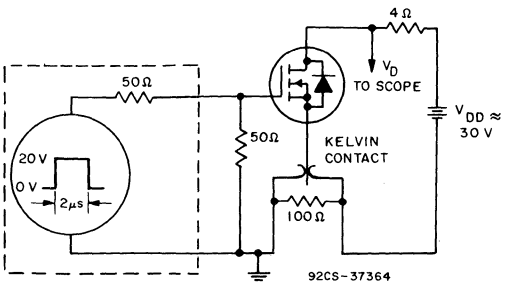


Fig. 11 — Switching Time Test Circuit

RFM15N12, RFM15N15, RFP15N12, RFP15N15

File Number **1443**

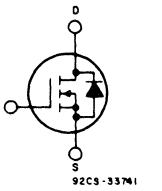
N-Channel Enhancement-Mode Power Field-Effect Transistors

15 A, 120 V — 150 V

$r_{DS}(on)$: 0.15 Ω

Features:

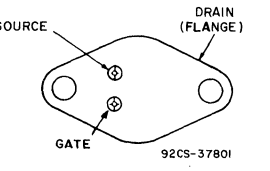
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

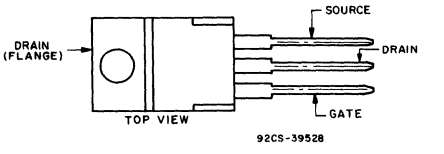
TERMINAL DESIGNATIONS

RFM15N12
RFM15N15



JEDEC TO-204AA

RFP15N12
RFP15N15



JEDEC TO-220AB

The RFM15N12 and RFM15N15 and the RFP15N12 and RFP15N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9195 and TA9230, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFM15N12	RFM15N15	RFP15N12	RFP15N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	120	150	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT RMS Continuous	I_D	15				A
Pulsed	I_{DM}	40				A
POWER DISSIPATION						
@ T_C=25°C	P_T	100	100	75	75	W
Derate above T_C=25°C		0.80	0.80	0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	−55 to +150				°C

RFM15N12, RFM15N15, RFP15N12, RFP15N15

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25°C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N12 RFP15N12		RFM15N15 RFP15N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125°C					
		V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 7.5 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 15 A V_{GS} = 10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 7.5 A V_{GS} = 10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 7.5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	750	—	750	
Reverse Transfer Capacitance	C_{rss}		—	350	—	350	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V I_D = 7.5 A R_{gen} = R_{gs} = 50 Ω V_{GS} = 10 V	50(typ.)	75	50(typ.)	75	ns
Rise Time	t_r		150(typ.)	225	150(typ.)	225	
Turn-Off Delay Time	$t_d(off)$		185(typ.)	280	185(typ.)	280	
Fall Time	t_f		125(typ.)	190	125(typ.)	190	
Thermal Resistance Junction-to-Case	RθJC	RFM15N12, RFM15N15	—	1.25	—	1.25	°C/W
		RFP15N12, RFP15N15	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N12 RFP15N12		RFM15N15 RFP15N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=7.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM15N12, RFM15N15, RFP15N12, RFP15N15

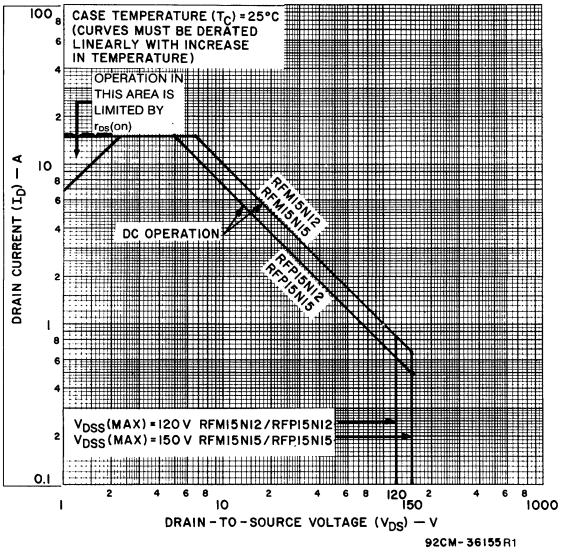


Fig. 1 — Maximum operating areas for all types.

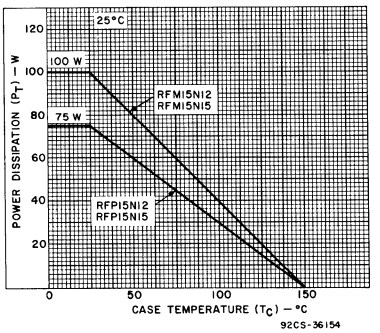


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

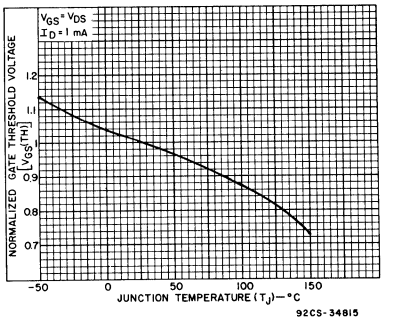


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

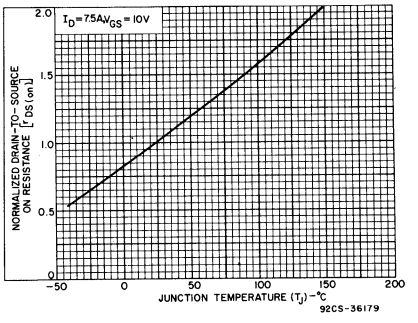


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

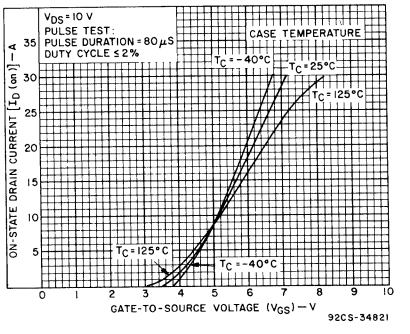


Fig. 5 — Typical transfer characteristics for all types.

RFM15N12, RFM15N15, RFP15N12, RFP15N15

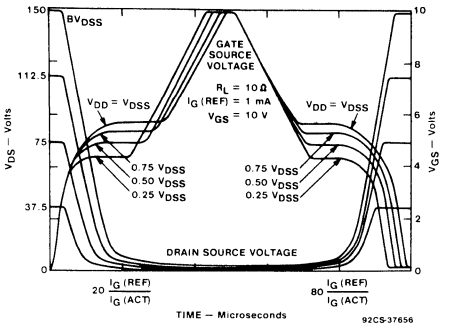


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

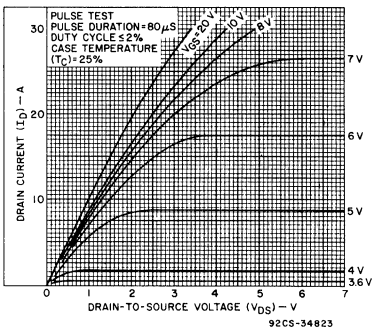


Fig. 7 — Typical saturation characteristics for all types.

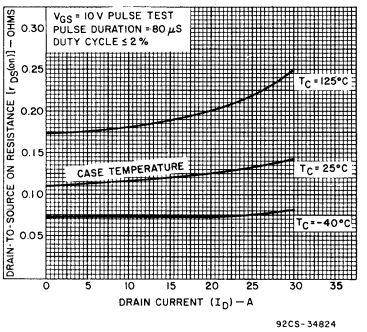


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

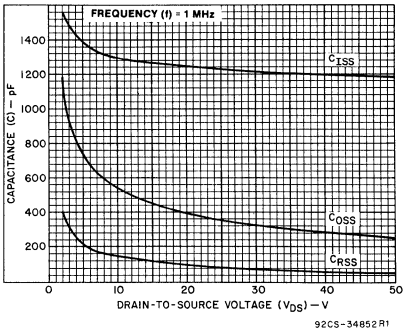


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

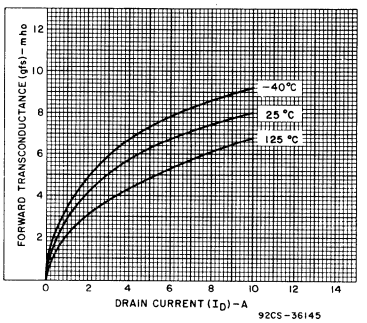


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

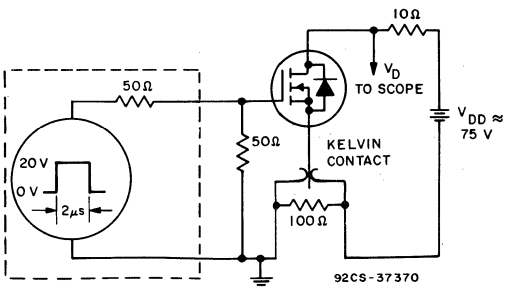


Fig. 11 — Switching Time Test Circuit

RFM18N08, RFM18N10, RFP18N08, RFP18N10

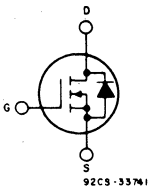
File Number **1446**

N-Channel Enhancment-Mode Power Field-Effect Transistors

18 A, 80 V — 100 V
$r_{DS}(on)$: 0.1Ω

Features:

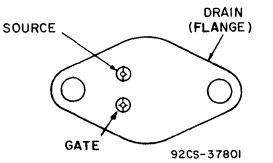
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-Channel Enhancement Mode

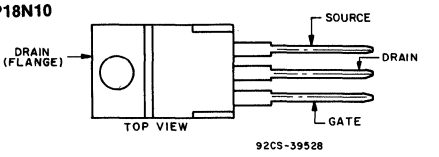
TERMINAL DESIGNATIONS

RFM18N08
RFM18N10



JEDEC TO-204AA

RFP18N08
RFP18N10



JEDEC TO-220AB

The RFM18N08 and RFM18N10 and the RFP18N08 and RFP18N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9286 and TA9287, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFM18N08	RFM18N10		RFP18N08	RFP18N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20					V
DRAIN CURRENT RMS Continuous	I_D	18					A
Pulsed	I_{DM}	45					A
POWER DISSIPATION							
@ T_C=25°C	P_T	100	100		75	75	W
Derate above T_C=25°C		0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	−55 to +150					°C

RFM18N08, RFM18N10, RFP18N08, RFP18N10

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_c) = 25° C unless otherwise specified*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFP18N08 MIN.	LIMITS RFM18N08 RFP18N08 MAX.	LIMITS RFM18N10 RFP18N10 MIN.	LIMITS RFM18N10 RFP18N10 MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V	—	1	—	—	μA
		V_{DS} = 80 V	—	—	—	1	
		T_C = 125° C, V_{DS} = 65 V	—	50	—	—	
		T_C = 125° C, V_{DS} = 80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 9 A, V_{GS} = 10 V	—	1.08	—	1.08	V
		I_D = 18 A, V_{GS} = 10 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 9 A, V_{GS} = 10 V	—	0.10	—	0.10	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V, I_D = 9 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	750	—	750	
Reverse Transfer Capacitance	C_{rss}		—	300	—	300	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V, I_D = 9 A, R_{gen} = R_{gs} = 50 Ω, V_{GS} = 10 V	60(typ.)	90	60(typ.)	90	ns
Rise Time	t_r		300(typ.)	450	300(typ.)	450	
Turn-Off Delay Time	$t_d(off)$		150(typ.)	225	150(typ.)	225	
Fall Time	t_f		150(typ.)	225	150(typ.)	225	
Thermal Resistance Junction-to-Case	RθJC	RFM18N08, RFM18N10	—	1.25	—	1.25	°C/W
		RFP18N08, RFP18N10	—	1.67	—	1.67	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFM18N08 RFM18N10 MIN.	LIMITS RFM18N08 RFM18N10 MAX.	LIMITS RFP18N08 RFP18N10 MIN.	LIMITS RFP18N08 RFP18N10 MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=9 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A, d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM18N08, RFM18N10, RFP18N08, RFP18N10

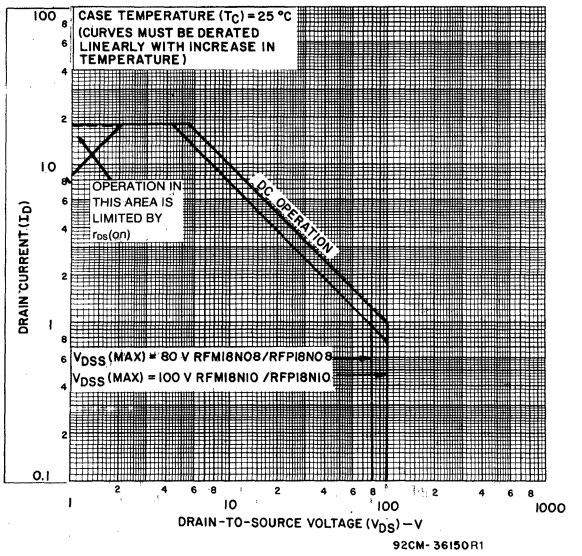


Fig. 1 — Maximum operating areas for all types.

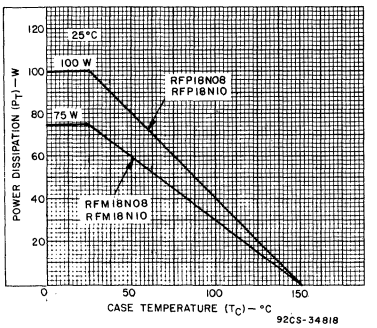


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

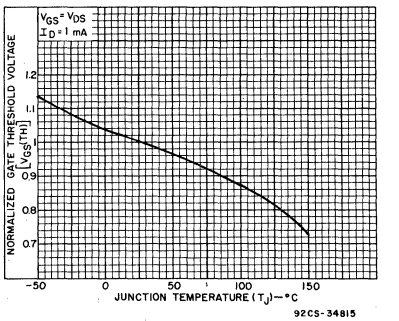


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

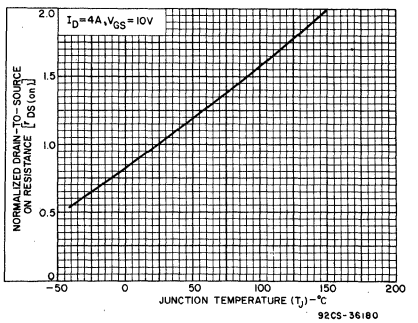


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

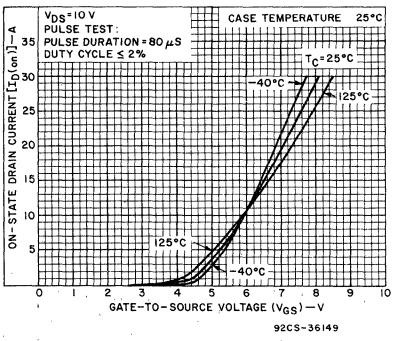


Fig. 5 — Typical transfer characteristics for all types.

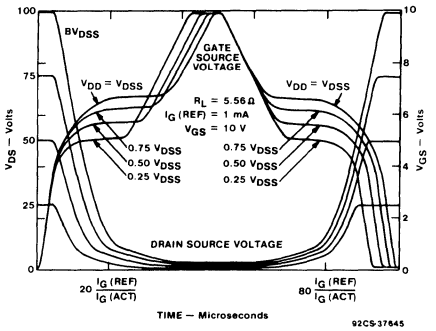


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

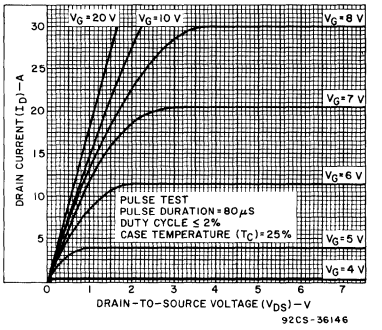


Fig. 7 — Typical saturation characteristics for all types.

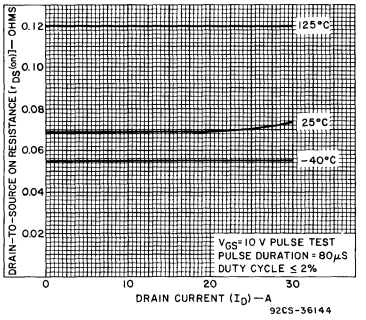


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

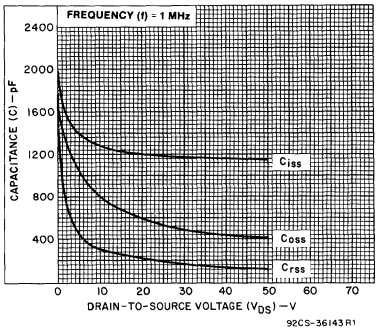


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

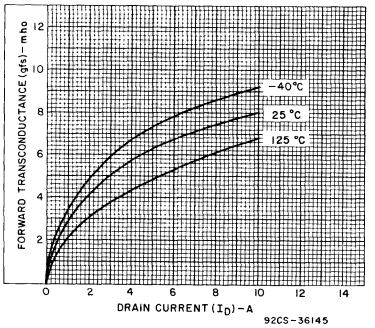


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

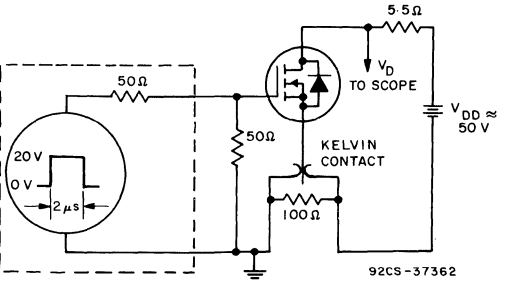


Fig. 11 — Switching Time Test Circuit

RFM25N05, RFM25N06, RFP25N05, RFP25N06

File Number **1492**

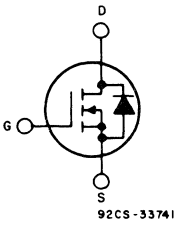
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 50 V - 60 V
$r_{DS}(on)$ = 0.07Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

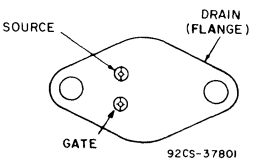
The RFM25N05 and RFM25N06 and the RFP25N05 and RFP25N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9386 and TA9387, respectively.

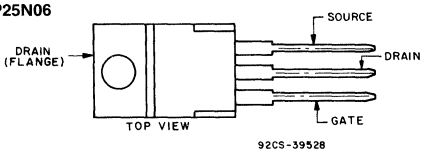
TERMINAL DESIGNATIONS

RFM25N05
RFM25N06



JEDEC TO-204AA

RFP25N05
RFP25N06



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T$_C$=25° C):*

	RFM25N05	RFM25N06		RFP25N05	RFP25N06	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60		50	60	V
DRAIN-GATE VOLTAGE (R_{GS}= 1 MΩ) .... V_{DGR}	50	60		50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			25			A
Pulsed ..... I_{DM}			60			A
POWER DISSIPATION @ T_C 25°C ..... P_T	100	100		75	75	W
Derate above T_C 25°C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM25N05, RFM25N06, RFP25N05, RFP25N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM25N05 RFP25N05		RFM25N06 RFP25N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V V_{DS}=50 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=40 V V_{DS}=50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	1.06	—	1.06	V
		I_D=25 A. V_{GS}=10 V	—	2.5	—	2.5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	0.07	—	0.07	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	5	—	5	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1700	—	1700	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=30 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=12.5 A	120(typ)	225	120(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	123(typ)	225	123(typ)	225	ns
Fall Time	t_f	V_{GS}=10 V	123(typ)	200	123(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM25N05, RFM25N06	—	1.25	—	1.25	°C/W
		RFP25N05, RFP25N06	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM25N05 RFP25N05		RFM25N06 RFP25N06		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM25N05, RFM25N06, RFP25N05, RFP25N06

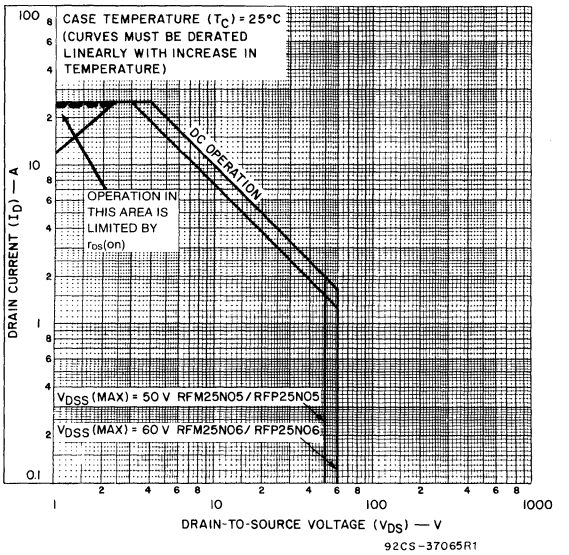


Fig. 1 — Maximum operating areas for all types.

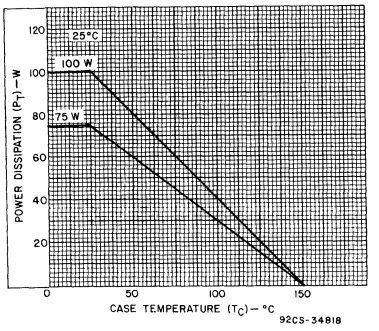


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

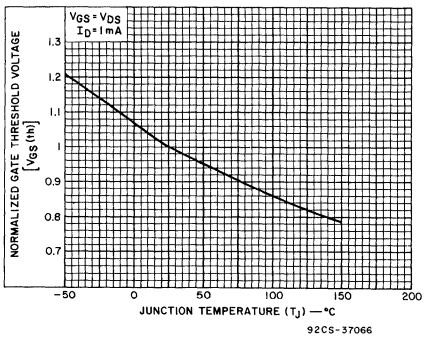


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

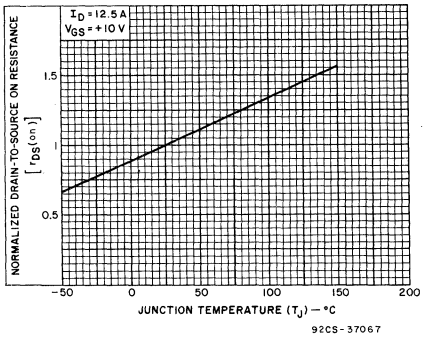


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

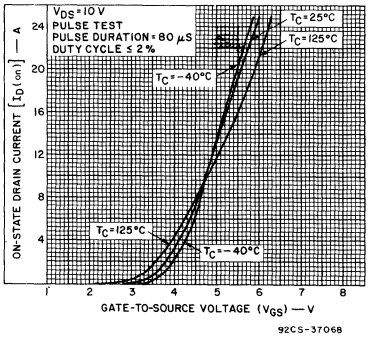


Fig. 5 — Typical transfer characteristics for all types.

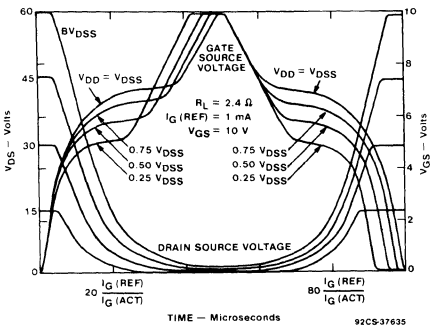


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

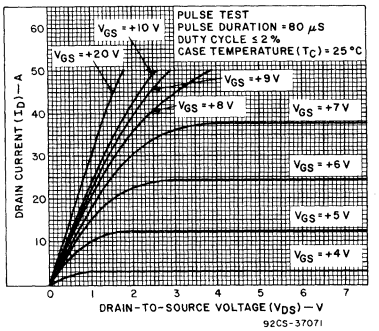


Fig. 7 — Typical saturation characteristics for all types.

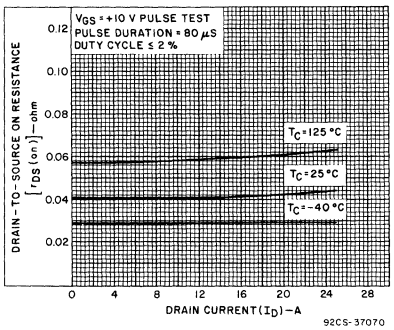


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

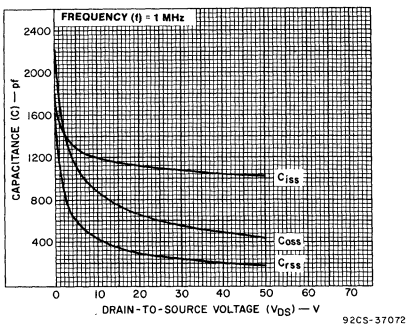


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

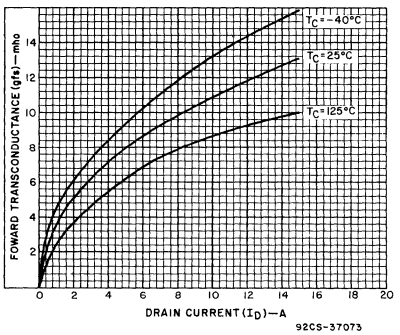


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

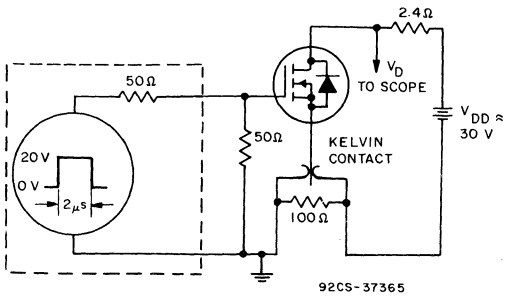


Fig. 11 — Switching Time Test Circuit

RFH25N18, RFH25N20

File Number **1631**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

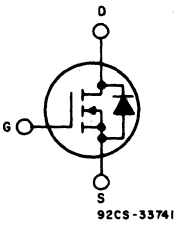
25 A, 180 V - 200 V

$r_{DS(on)}$ = 0.15 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



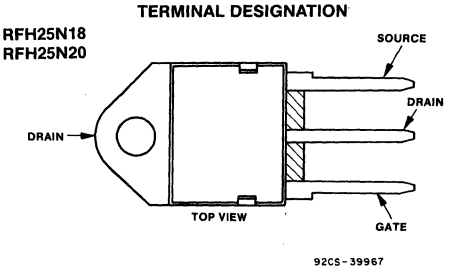
N-CHANNEL ENHANCEMENT MODE

The RFH25N18 and RFH25N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH25N18 and RFH25N20 types were formerly RCA developmental numbers TA9483A and TA9483B respectively.

TERMINAL DESIGNATION



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH25N18	RFH25N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180	200	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	180	200	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	25		A
Pulsed	I_{DM}	60		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		° C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25°C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 145 V V_{DS} = 160 V	— —	1 —	— —	— 1	μA
		T_C = 125°C V_{DS} = 145 V V_{DS} = 160 V	 — —	 50 —	 — —	 — 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	1.875	—	1.875	V
		I_D = 25 A V_{GS} = 10 V	—	5	—	5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = 10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	3500	—	3500	pF
Output Capacitance	C_{oss}		—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}		—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DS} = 100 V I_D = 12.5 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		150(typ)	225	150(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$		300(typ)	400	300(typ)	400	ns
Fall Time	t_f		120(typ)	200	120(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH25N18, RFH25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH25N18		RFH25N20		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 12.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	300 (typ.)		300 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH25N18, RFH25N20

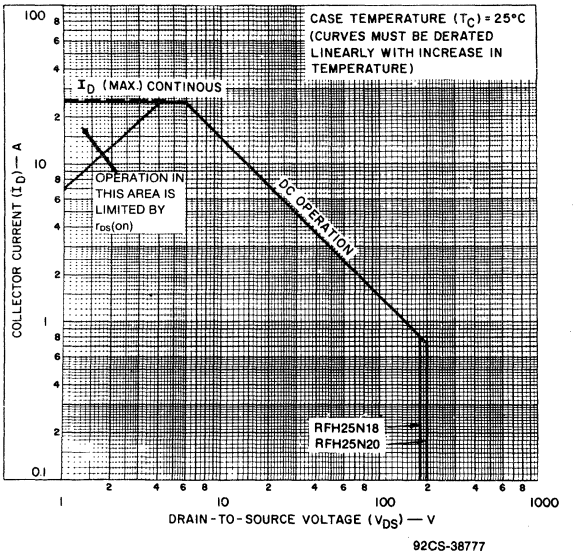


Fig. 1 - Maximum safe operating areas for all types.

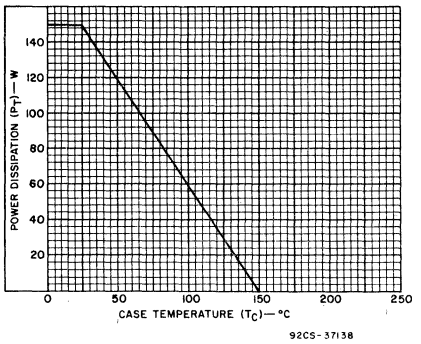


Fig. 2 - Power vs. temperature derating curve for all types.

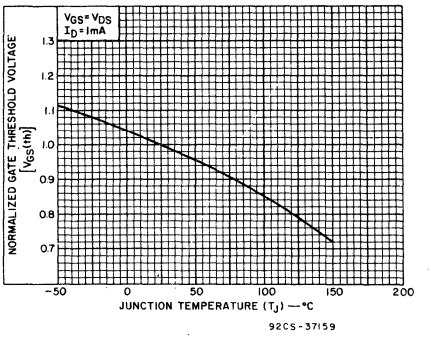


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

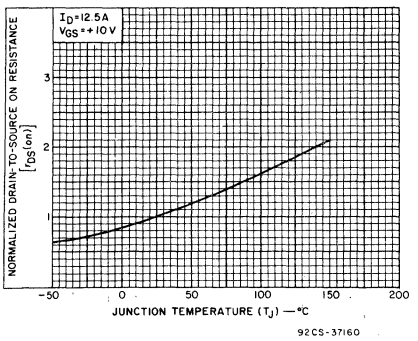


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

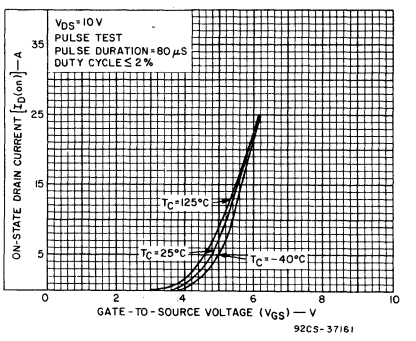


Fig. 5 - Typical transfer characteristics for all types.

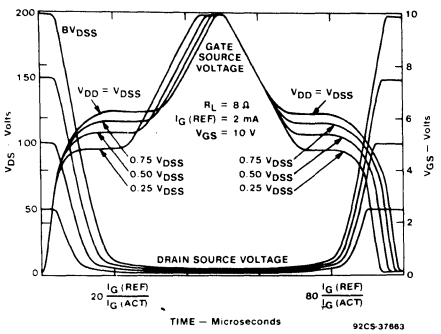


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

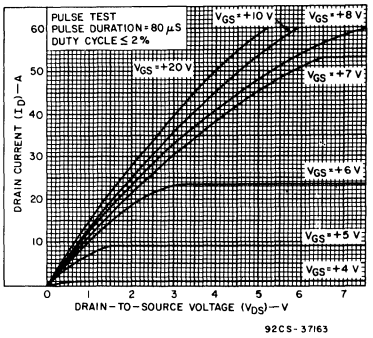


Fig. 7 - Typical saturation characteristics for all types.

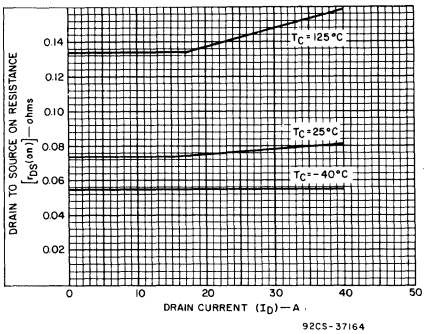


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

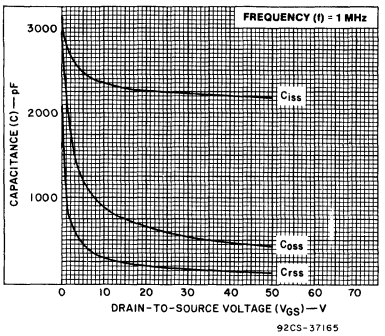


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

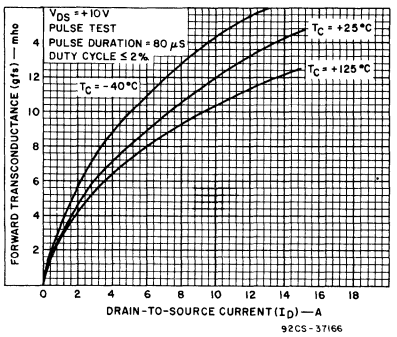


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

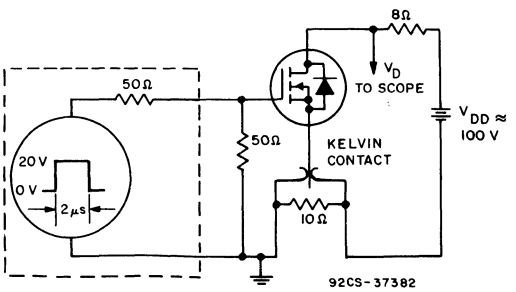


Fig. 11 - Switching Time Test Circuit.

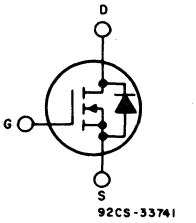
RFK25N18, RFK25N20

File Number **1500**

N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, 180 V - 200 V
$r_{DS}(on)$ = 0.15 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



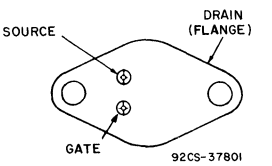
N-CHANNEL ENHANCEMENT MODE

The RFK25N18 and RFK25N20* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK25N18 and RFK25N20 types were formerly RCA developmental numbers TA9295A and TA9295B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK25N18		RFK25N20	
DRAIN-SOURCE VOLTAGE	V_{DSS}	180		200	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	180		200	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		25		A
Pulsed	I_{DM}		60		A
POWER DISSIPATION @ T_C=25° C	P_T		150		W
Derate above T_C=25° C			1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

RFK25N18, RFK25N20

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	1.875	—	1.875	V
		I_D=25 A V_{GS}=10 V	—	5	—	5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=10 V	—	.15	—	.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	7	—	7	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3500	—	3500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	900	—	900	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	400	—	400	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r	I_D=12.5 A	150(typ)	225	150(typ)	225	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	300(typ)	400	300(typ)	400	ns
Fall Time	t_f	V_{GS}=10 V	120(typ)	200	120(typ)	200	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK25N18, RFK25N20 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25N18		RFK25N20		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300(typ)		300(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFK25N18, RFK25N20

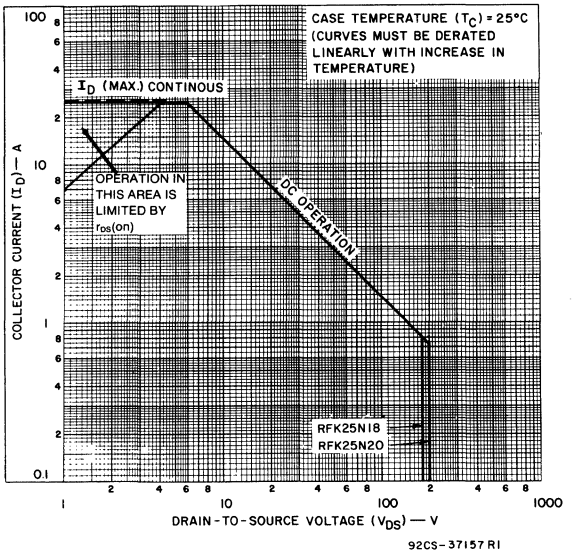


Fig. 1 — Maximum safe operating areas for all types.

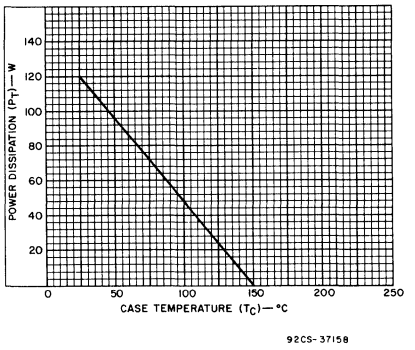


Fig. 2 — Power vs. temperature derating curve for all types.

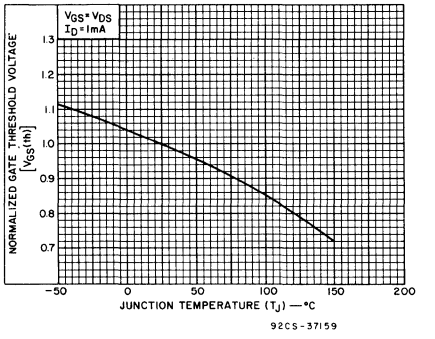


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

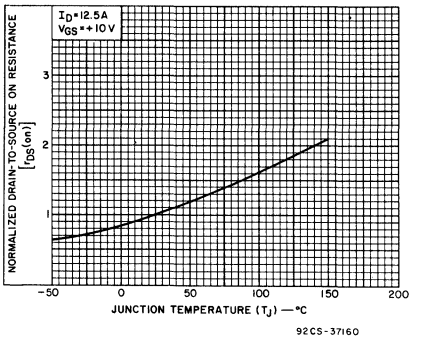


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

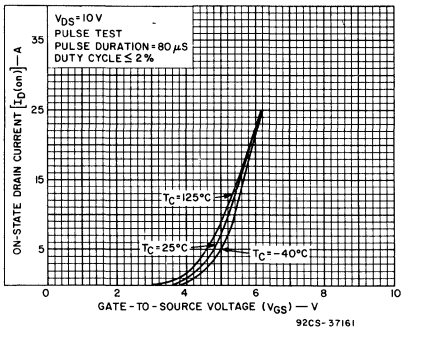


Fig. 5 — Typical transfer characteristics for all types.

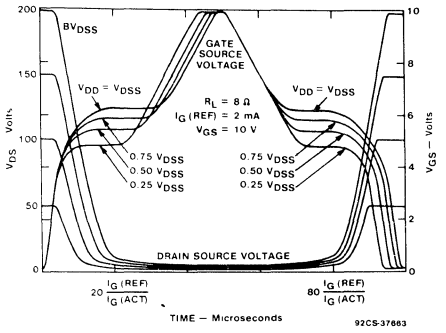


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

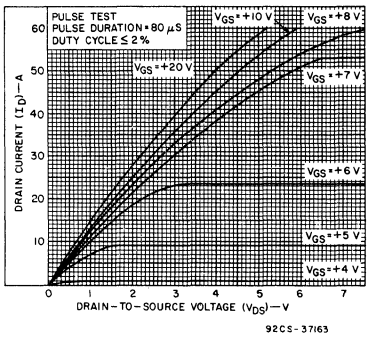


Fig. 7 — Typical saturation characteristics for all types.

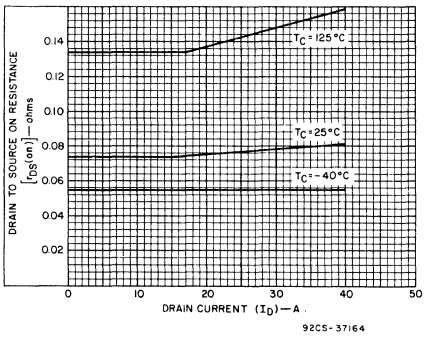


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

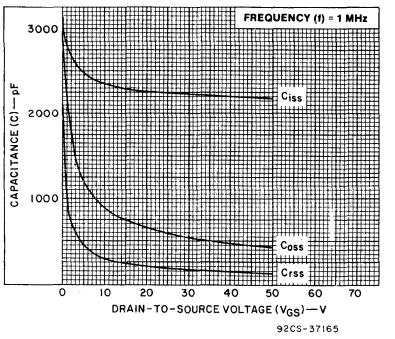


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

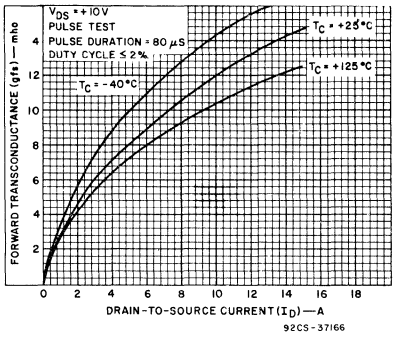


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

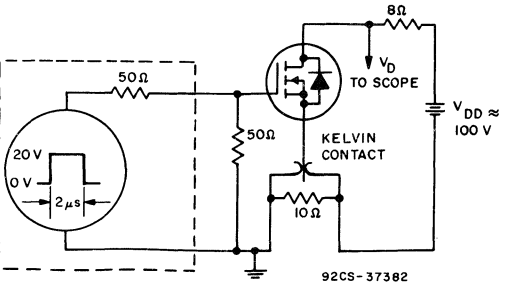


Fig. 11 — Switching Time Test Circuit

RFH30N12, RFH30N15

File Number **1633**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

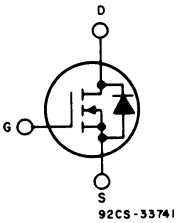
30 A, 120 V - 150 V

$r_{DS(on)}$ = 0.075 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



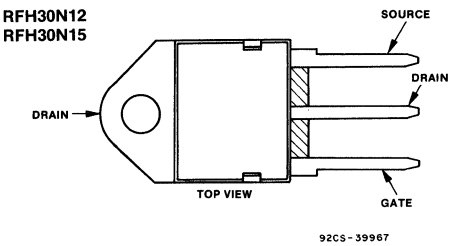
N-CHANNEL ENHANCEMENT MODE

The RFH30N12 and RFH30N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH30N12 and RFH30N15 types were formerly RCA developmental numbers TA9578A and TA9578B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH30N12	RFH30N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	30		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_J, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V	—	1	—	—	μA
		V_{DS} = 120 V	—	—	—	1	
		T_C = 125° C V_{DS} = 100 V	—	50	—	—	
		V_{DS} = 120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
On-State Gate Voltage	$V_{GS}(on)$[a]	V_{DS} = 5 V I_D = 15 A	—	8	—	8	V
		V_{DS} = 10 V I_D = 30 A	—	10	—	10	
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	1.125	—	1.125	V
		I_D = 30 A V_{GS} = 10 V	—	2.65	—	2.65	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 15 A V_{GS} = 10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 75 V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D = 15 A	420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	300(typ)	450	300(typ)	450	
Fall Time	t_f	V_{GS} = 10 V	250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH30N12, RFH30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH30N12		RFH30N15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 15A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH30N12, RFH30N15

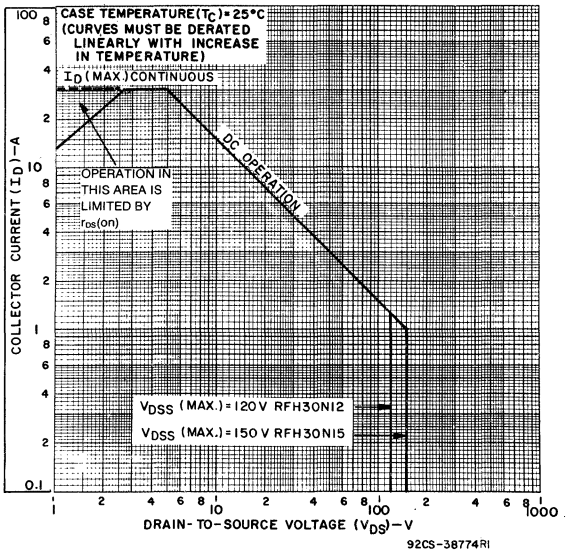


Fig. 1 - Maximum safe operating areas for all types.

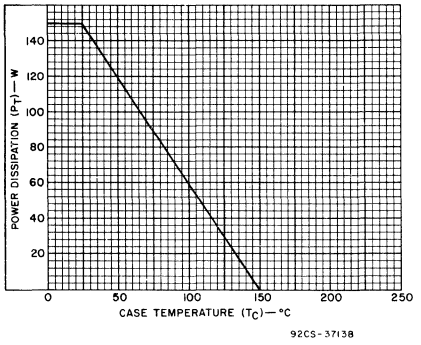


Fig. 2 - Power vs. temperature derating curve for all types.

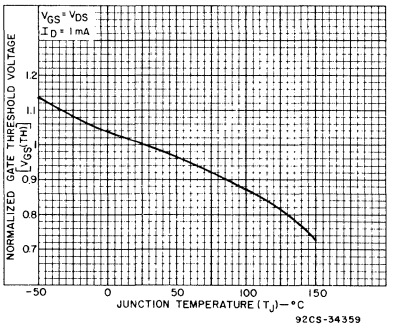


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

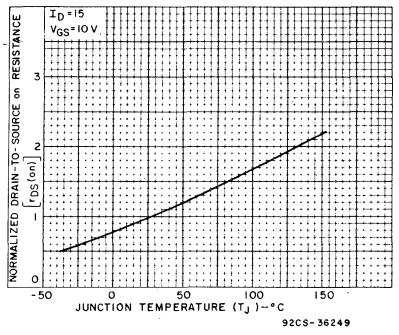


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

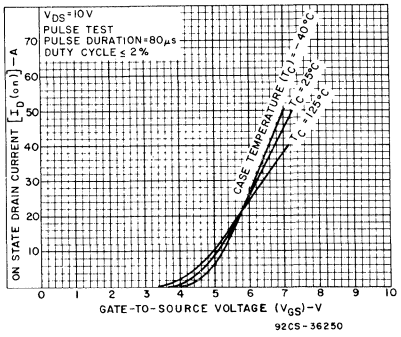


Fig. 5 - Typical transfer characteristics for all types.

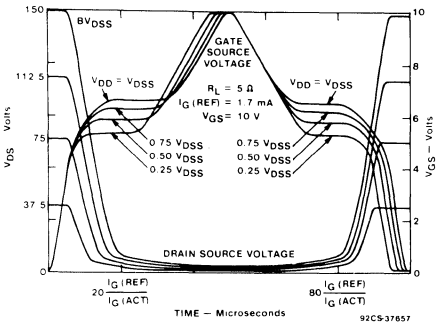


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

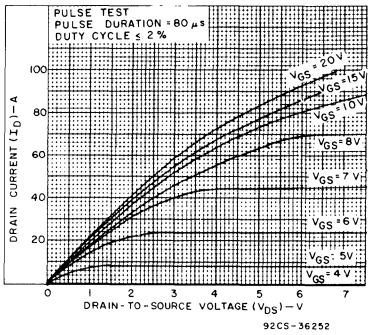


Fig. 7 - Typical saturation characteristics for all types.

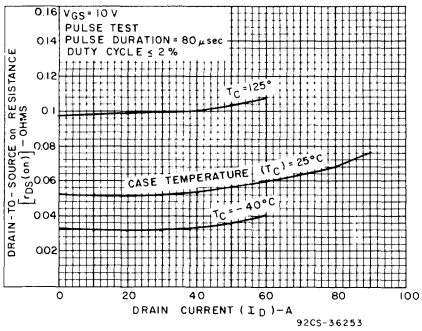


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

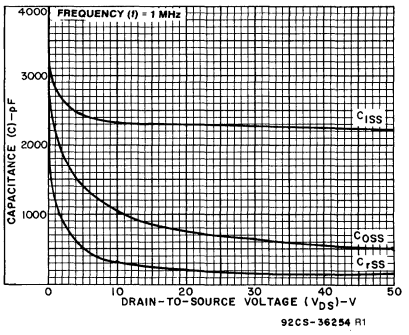


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

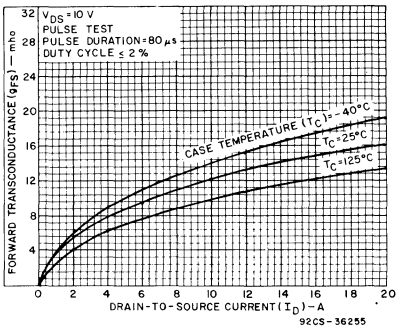


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

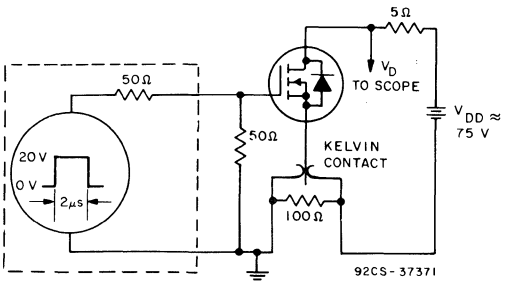


Fig. 11 - Switching Time Test Circuit.

RFK30N12, RFK30N15

File Number **1455**

Power MOS Field-Effect Transistors

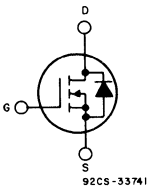
N-Channel Enhancement-Mode Power Field-Effect Transistors

30 A, 120 V - 150 V
$r_{DS}(on)$=0.075 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

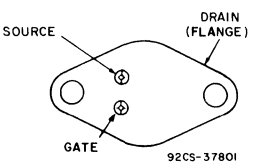
The RFK30N12 and RFK30N15* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK30N12 and RFK30N15 types were formerly RCA developmental numbers TA9188A and TA9188B, respectively.

TERMINAL DESIGNATIONS

RFK30N12
RFK30N15



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK30N12	RFK30N15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	120	150	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	120	150	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	30		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @T_C=25°C	P_T	120		W
Derate above T_C=25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +125		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V	—	1	—	—	μA
		V_{DS}=120 V	—	—	—	1	
		T_C=125° C V_{DS}=100 V	—	50	—	—	
		V_{DS}=120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ± 20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	1.125	—	1.125	V
		I_D=30 A V_{GS}=10 V	—	3	—	3	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=15 A V_{GS}=10 V	—	0.075	—	0.075	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=15 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1200	—	1200	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75V	75(typ)	115	75(typ)	115	ns
Rise Time	t_r	I_D=15 A	420(typ)	630	420(typ)	630	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	300(typ)	450	300(typ)	450	
Fall Time	t_f	V_{GS}=10 V	250(typ)	375	250(typ)	375	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK30N12, RFK30N15 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK30N12		RFK30N15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=15 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFK30N12, RFK30N15

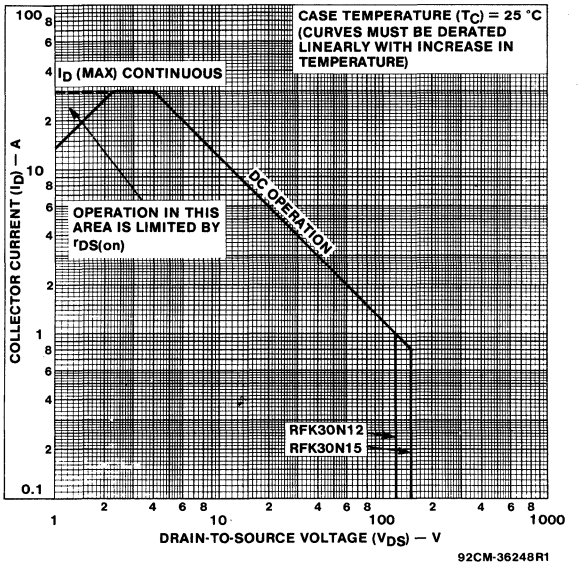


Fig. 1 - Maximum safe operating areas for all types.

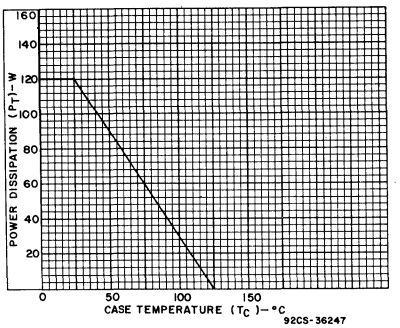


Fig. 2 - Power vs. temperature derating curve for all types.

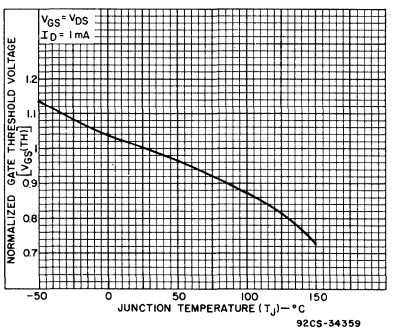


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

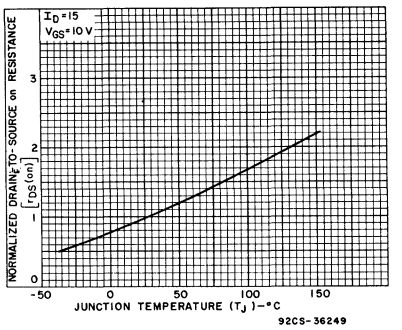


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

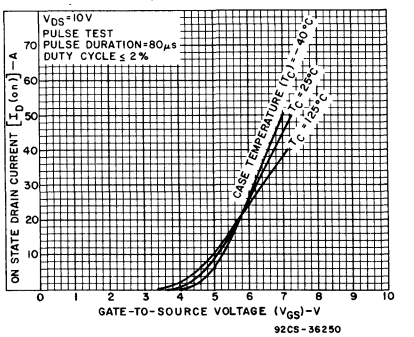


Fig. 5 - Typical transfer characteristics for all types.

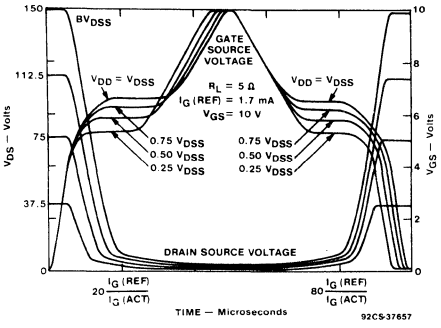


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

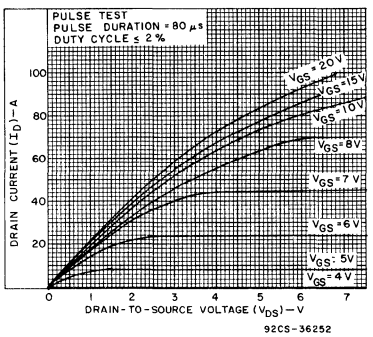


Fig. 7 - Typical saturation characteristics for all types.

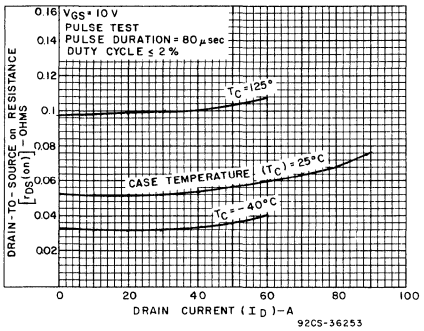


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

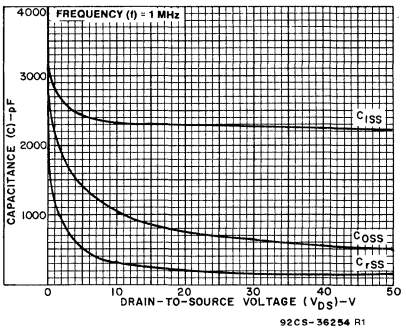


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

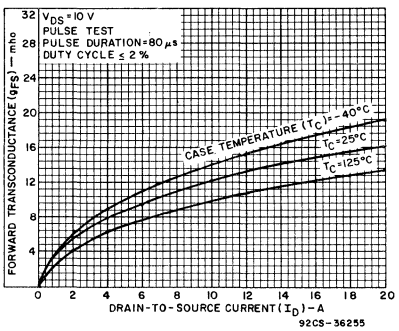


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

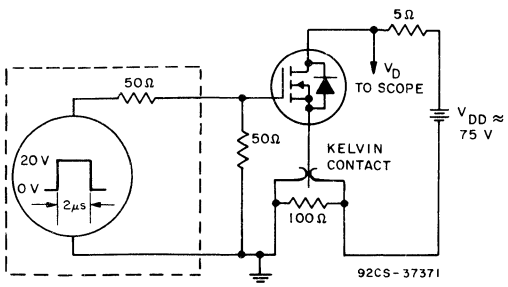


Fig. 11 — Switching Time Test Circuit

RFH35N08, RFH35N10

File Number **1634**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

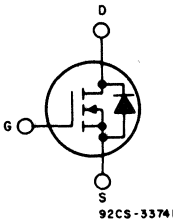
35 A, 80 V - 100 V

$r_{DS(on)}$ = 0.055 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



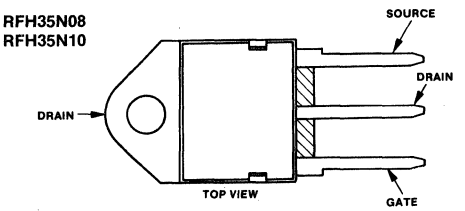
N-CHANNEL ENHANCEMENT MODE

The RFH35N08 and RFH35N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH35N08 and RFH35N10 types were formerly RCA developmental numbers TA9481A and TA9481B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

		RFH35N08	RFH35N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80	100	V
DRAIN-GATE VOLTAGE, R_{GS} = 1 MΩ	V_{DGR}	80	100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	35		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65 V	—	1	—	—	μA
		V_{DS} = 80 V	—	—	—	1	
		T_C = 125° C V_{DS} = 65 V	—	50	—	—	
		V_{DS} = 80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.963	—	0.963	V
		I_D = 35 A V_{GS} = 10 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 17.5 A V_{GS} = 10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}		—	600	—	600	
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V I_D = 17.5 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r		225(typ)	450	225(typ)	450	
Turn-Off Delay Time	$t_d(off)$		240(typ)	450	240(typ)	450	
Fall Time	t_f		165(typ)	350	165(typ)	350	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH35N08, RFH35N10 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH35N08		RFH35N10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}*	I_{SD} = 17.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	200 (typ.)		200 (typ.)		ns

* Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFH35N08, RFH35N10

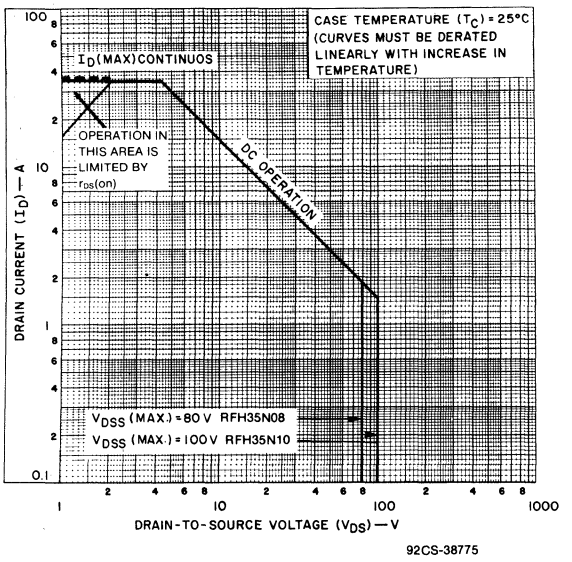


Fig. 1 - Maximum safe operating areas for all types.

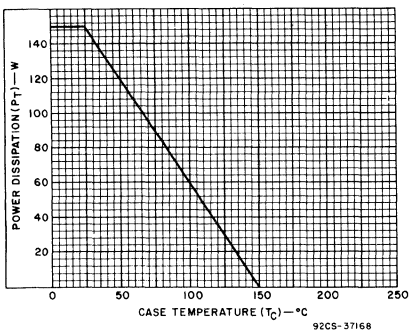


Fig. 2 - Power vs. temperature derating curve for all types.

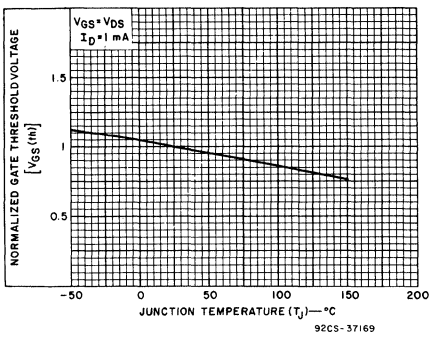


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

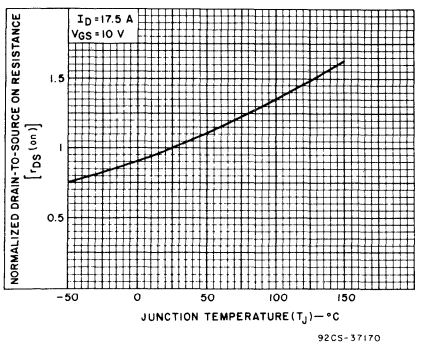


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

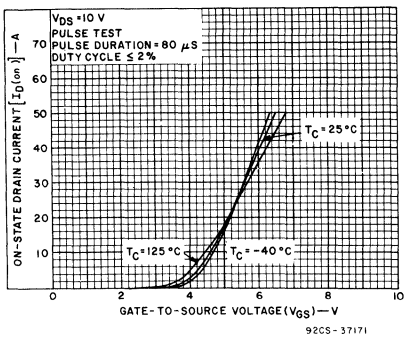


Fig. 5 - Typical transfer characteristics for all types.

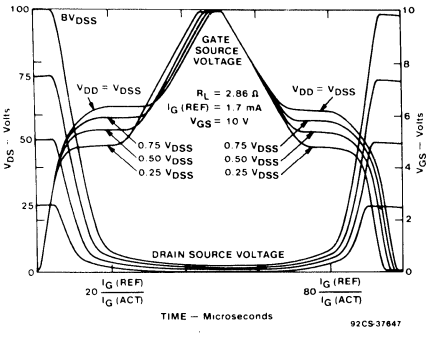


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

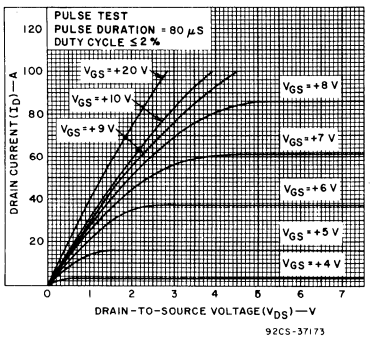


Fig. 7 - Typical saturation characteristics for all types.

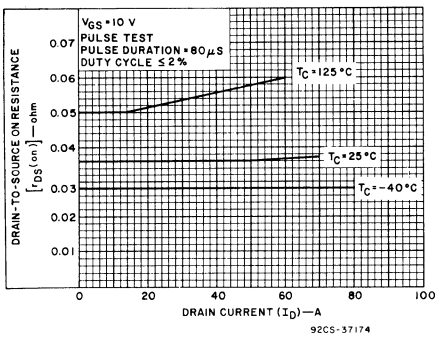


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

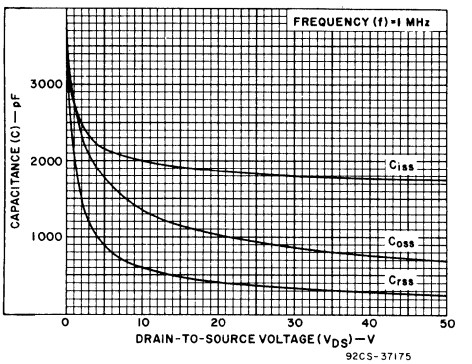


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

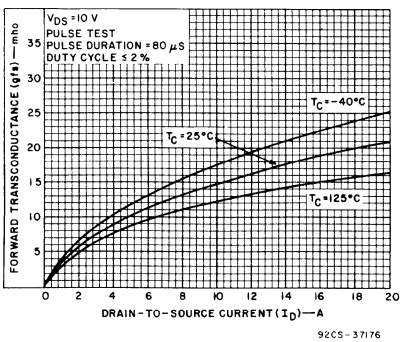


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

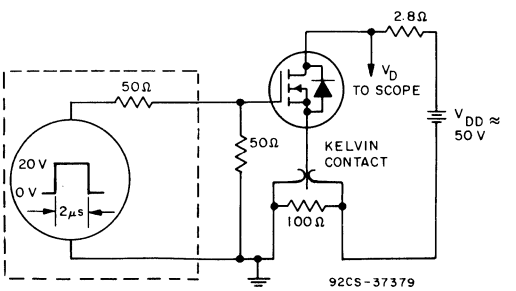


Fig. 11 - Switching Time Test Circuit.

RFK35N08, RFK35N10

File Number **1499**

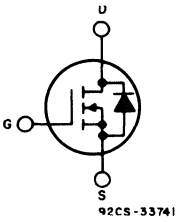
Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

35 A, 80 V - 100 V
$r_{DS}(on)$ = 0.055 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

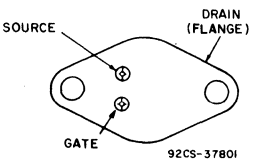
The RFK35N08 and RFK35N10* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK35N08 and RFK35N10 types were formerly RCA developmental numbers TA9288A and TA9288B, respectively.

TERMINAL DESIGNATIONS

RFK35N08
RFK35N10



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK35N08		RFK35N10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	80		100	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	80		100	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		35		A
Pulsed	I_{DM}		100		A
POWER DISSIPATION @ T_C=25° C	P_T		150		W
Derate above T_C=25° C			1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.9625	—	0.9625	V
		I_D=35 A V_{GS}=10 V	—	3.5	—	3.5	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=17.5 A V_{GS}=10 V	—	0.055	—	0.055	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=17.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1 MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1500	—	1500	pF
Reverse Transfer Capacitance	C_{rss}		—	600	—	600	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=17.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	45(typ)	100	45(typ)	100	ns
Rise Time	t_r		225(typ)	450	225(typ)	450	ns
Turn-Off Delay Time	$t_d(off)$		240(typ)	450	240(typ)	450	ns
Fall Time	t_f		165(typ)	350	165(typ)	350	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK35N08, RFK35N10 Series	—	0.83	—	0.83	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK35N08		RFK35N10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD} [a]	I_{SD}=17.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFK35N08, RFK35N10

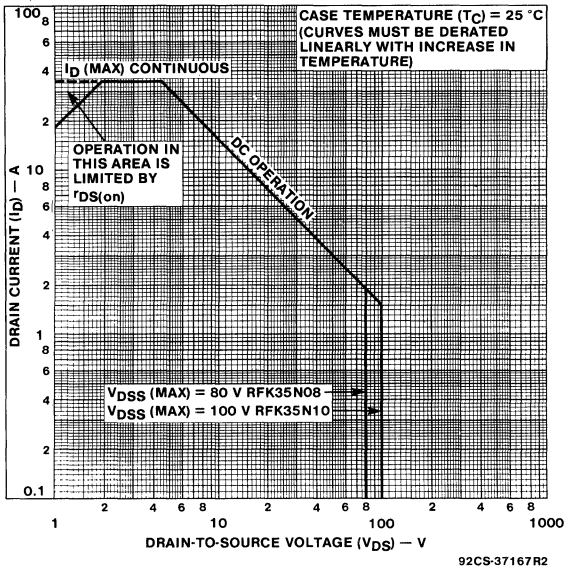


Fig. 1 — Maximum safe operating areas for all types.

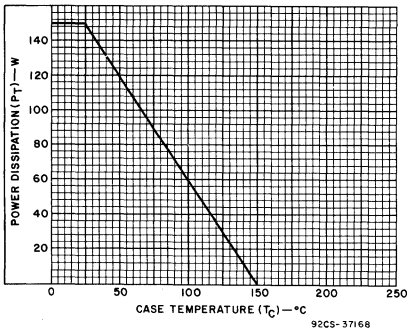


Fig. 2 — Power vs. temperature derating curve for all types.

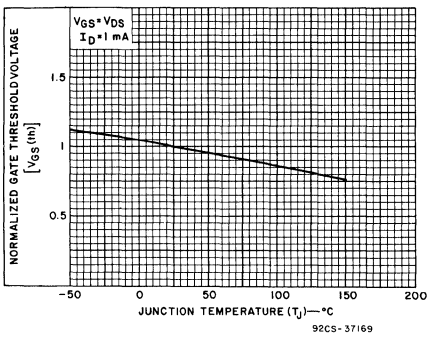


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

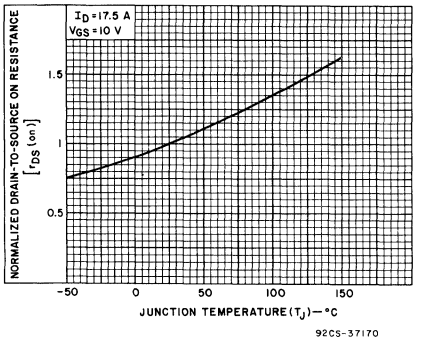


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

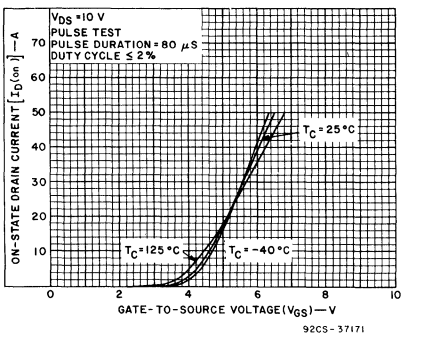


Fig. 5 — Typical transfer characteristics for all types.

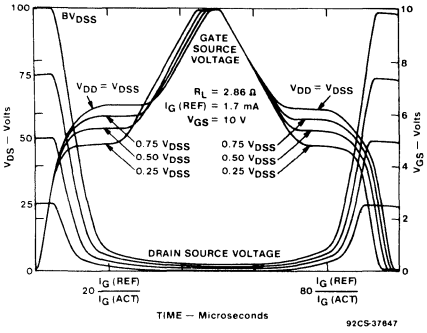


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

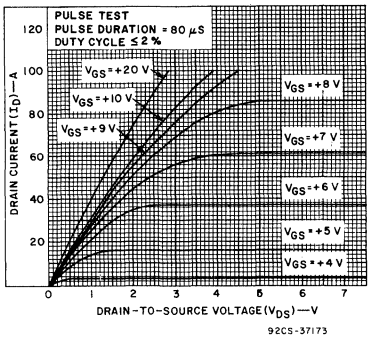


Fig. 7 — Typical saturation characteristics for all types.

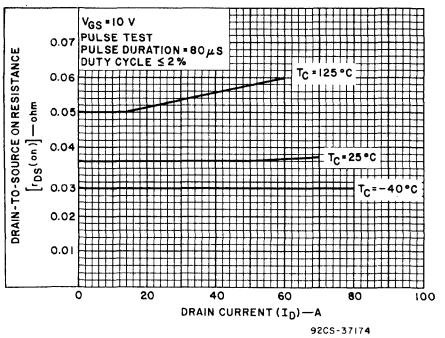


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

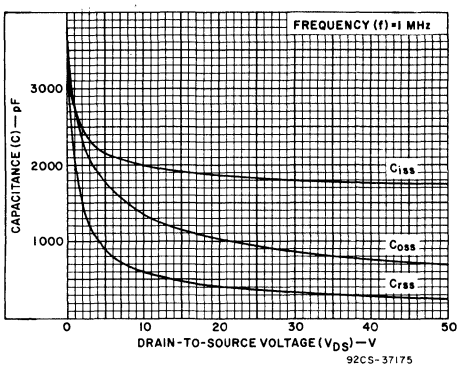


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

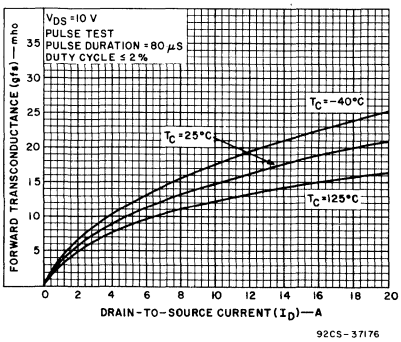


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

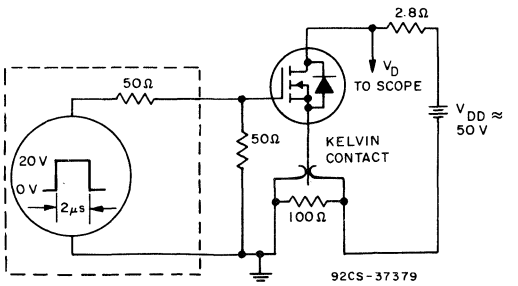


Fig. 11 — Switching Time Test Circuit.

RFH45N05, RFH45N06

File Number **1635**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

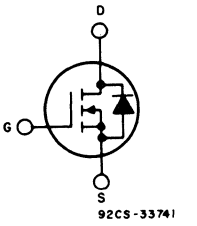
45 A, 50 V - 60 V

$r_{DS(on)}$ = 0.040 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



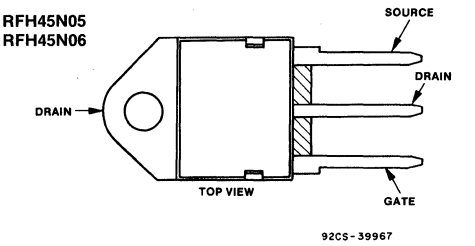
N-CHANNEL ENHANCEMENT MODE

The RFH45N05 and RFH45N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH45N05 and RFH45N06 types were formerly RCA developmental numbers TA9480A and TA9480B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH45N05	RFH45N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50	60	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	50	60	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	45		A
Pulsed	I_{DM}	100		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125° C V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	0.9	—	0.9	V
		I_D = 45 A V_{GS} = 10 V	—	3.6	—	3.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 22.5 A V_{GS} = 10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1800	—	1800	
Reverse Transfer Capacitance	C_{rss}		—	750	—	750	
Turn-On Delay Time	$t_d(on)$	V_{DS} = 30 V I_D = 22.5 A R_{gen}=R_{gs}=50Ω V_{GS} = 10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		310(typ)	475	310(typ)	475	
Turn-Off Delay Time	$t_d(off)$		220(typ)	350	220(typ)	350	
Fall Time	t_f		240(typ)	375	240(typ)	375	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH45N05, RFH45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH45N05		RFH45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH45N05, RFH45N06

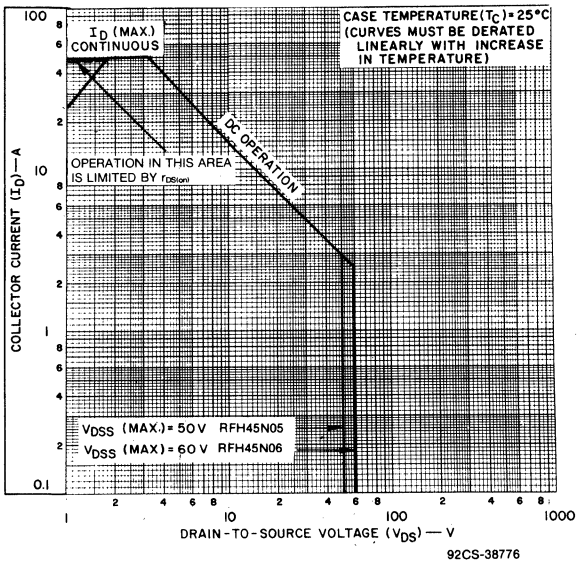


Fig. 1 - Maximum safe operating areas for all types.

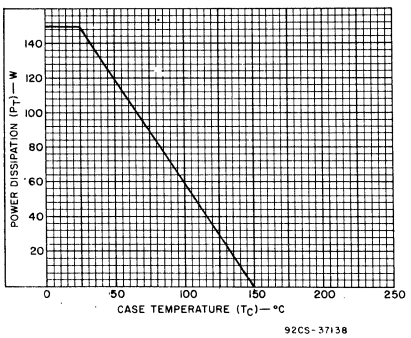


Fig. 2 - Power vs. temperature derating curve for all types.

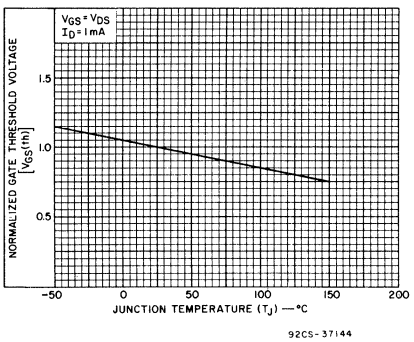


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

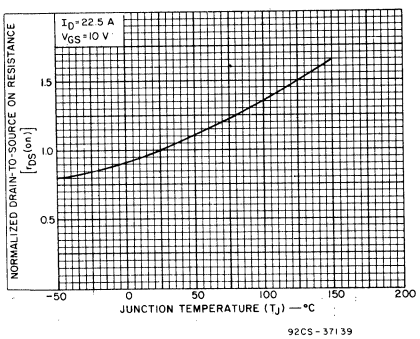


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

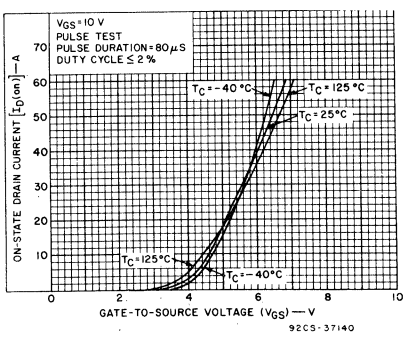


Fig. 5 - Typical transfer characteristics for all types.

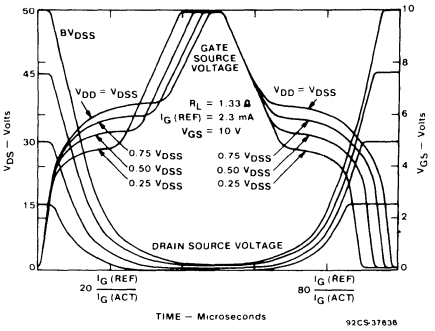


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

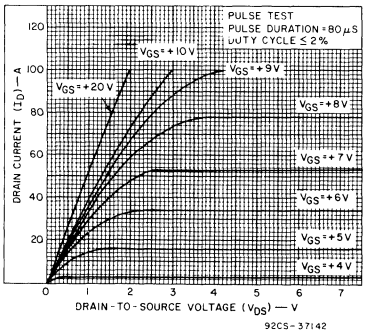


Fig. 7 - Typical saturation characteristics for all types.

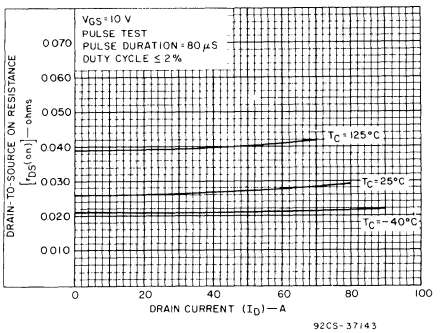


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

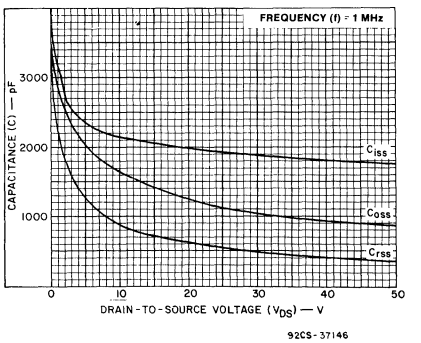


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

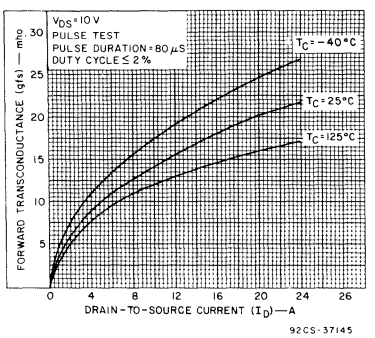


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

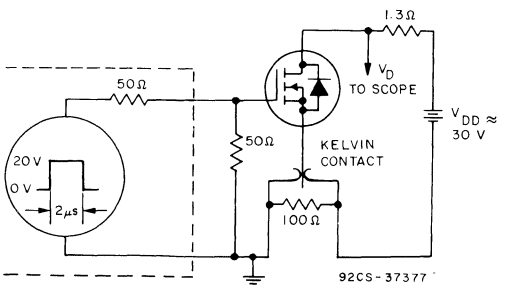


Fig. 11 - Switching Time Test Circuit.

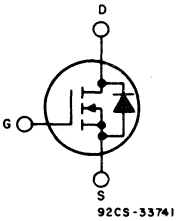
RFK45N05, RFK45N06

File Number **1498**

N-Channel Enhancement-Mode Power Field-Effect Transistors

45 A, 50 V - 60 V
$r_{DS}(on)$ = 0.040 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



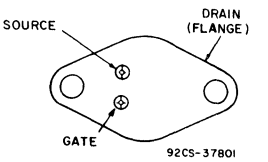
N-CHANNEL ENHANCEMENT MODE

The RFK45N05 and RFK45N06* are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK45N05 and RFK45N06 types were formerly RCA developmental numbers TA9388A and TA9388B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

		RFK45N05		RFK45N06	
DRAIN-SOURCE VOLTAGE	V_{DSS}	50		60	V
DRAIN-GATE VOLTAGE, R_{gs}=1 MΩ	V_{DGR}	50		60	V
GATE-SOURCE VOLTAGE	V_{GS}		±20		V
DRAIN CURRENT, RMS Continuous	I_D		45		A
Pulsed	I_{DM}		100		A
POWER DISSIPATION @ T_C=25° C	P_T		150		W
Derate above T_C=25° C			1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}		-55 to +150		°C

RFK45N05, RFK45N06

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	60	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	2	4	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40 V V_{DS}=50 V	— —	1 —	— —	— 1	μA
		T_C=125° c V_{DS}=40 V V_{DS}=50 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	0.9	—	0.9	V
		I_D=45 A V_{GS}=10 V	—	3.6	—	3.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=22.5 A V_{GS}=10 V	—	.04	—	.04	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=22.5 A	10	—	10	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	3000	—	3000	pF
Output Capacitance	C_{oss}		—	1800	—	1800	pF
Reverse Transfer Capacitance	C_{rss}		—	750	—	750	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 30 V I_D=22.5 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	40(typ)	80	40(typ)	80	ns
Rise Time	t_r		310(typ)	475	310(typ)	475	ns
Turn-Off Delay Time	$t_d(off)$		220(typ)	350	220(typ)	350	ns
Fall Time	t_f		240(typ)	375	240(typ)	375	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFK45N05, RFK45N06 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK45N05		RFK45N06		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 22.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	150(typ.)		150(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFK45N05, RFK45N06

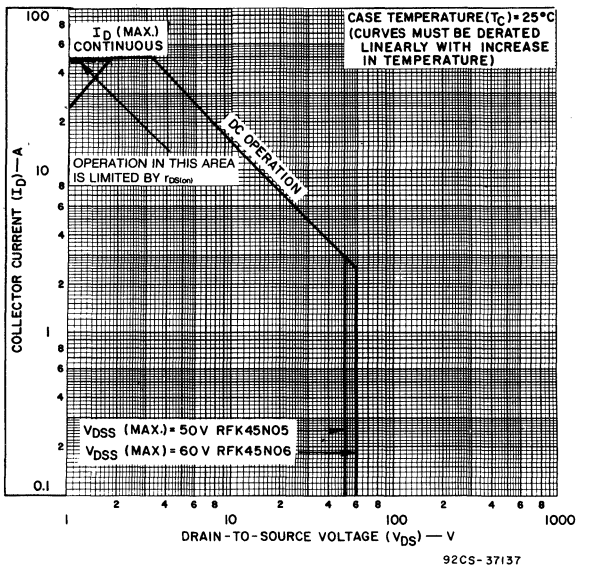


Fig. 1 — Maximum safe operating areas for all types.

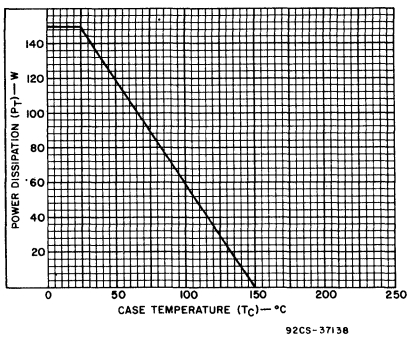


Fig. 2 — Power vs. temperature derating curve for all types.

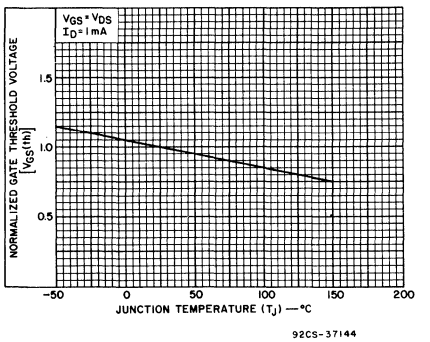


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

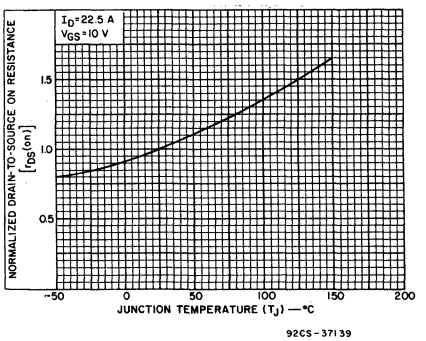


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

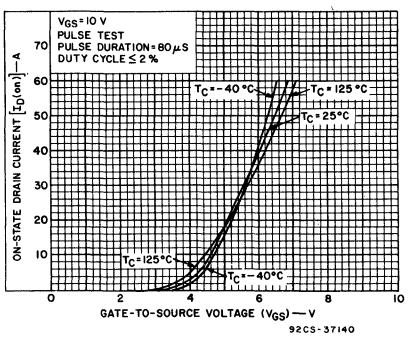


Fig. 5 — Typical transfer characteristics for all types.

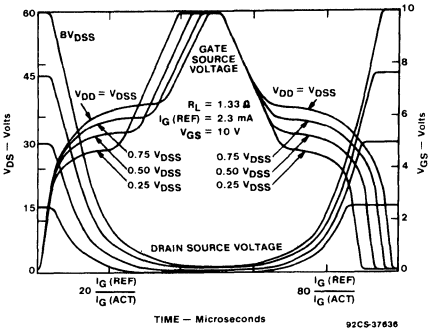


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

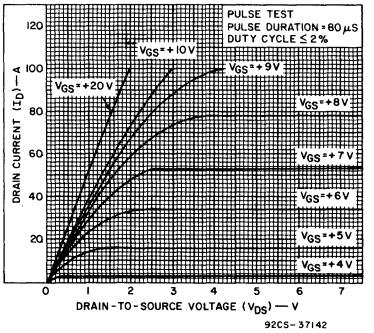


Fig. 7 — Typical saturation characteristics for all types.

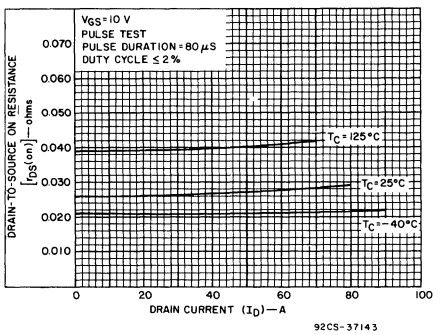


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

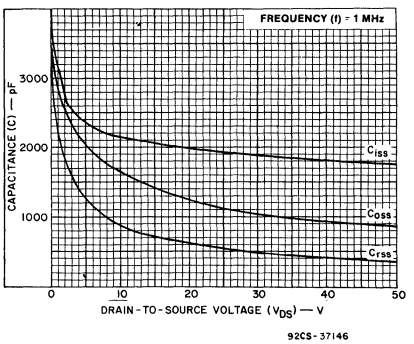


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

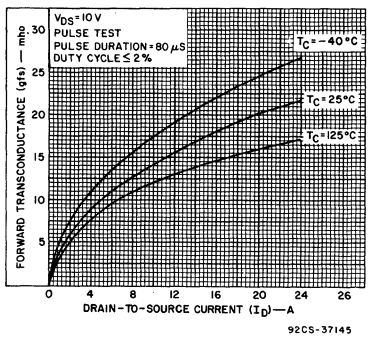


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

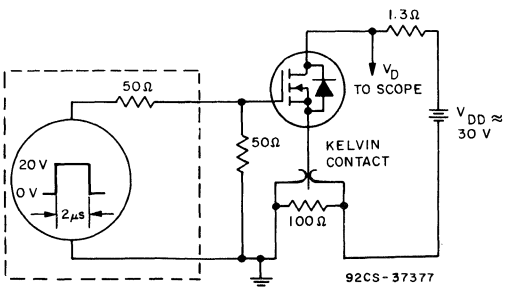


Fig. 11 - Switching Time Test Circuit.

RFL1P08, RFL1P10, RFP2P08, RFP2P10

File Number **1535**

Power MOS Field-Effect Transistors

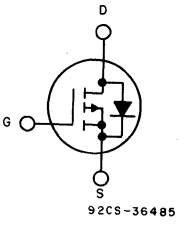
P-Channel Enhancement-Mode Power Field-Effect Transistors

1 and 2 A, -80 V and -100 V
$r_{DS}(on)$: 3.0Ω and 3.15Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

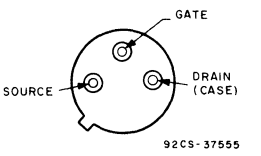
The RFL1P08 and RFL1P10 and the RFP2P08 and RFP2P10 are P-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9400 and TA9401, respectively.

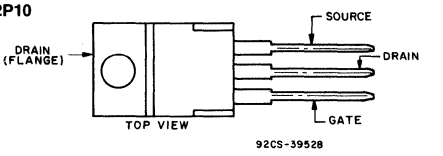
TERMINAL DESIGNATIONS

RFL1P08
RFL1P10



JEDEC TO-205AF

RFP2P08
RFP2P10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFL1P08	RFL1P10	RFP2P08	RFP2P10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100	-80	-100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ)	V_{DGR}	-80	-100	-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20				V
DRAIN CURRENT Rms Continuous	I_D	1	1	2	2	A
Pulsed	I_{DM}	5				A
POWER DISSIPATION	P_T					
@ T_C=25° C		8.33	8.33	25	25	W
Derate above T_C=25° C		0.0667	0.0667	0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150				°C

RFL1P08, RFL1P10, RFP2P08, RFP2P10

ELECTRICAL CHARACTERISTICS, at Case Temperature (Tc) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL1P08 RFP2P08		RFL1P10 RFP2P10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA, V_{GS} = 0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -65 V	—	1	—	—	μA
		V_{DS} = -80 V	—	—	—	1	
		T_C = 125° C, V_{DS} = -65 V	—	50	—	—	
		T_C = 125° C, V_{DS} = -80 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V, V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 1 A, V_{GS} = -10 V, RFP	—	-3.0	—	-3.0	V
		I_D = 1 A, V_{GS} = -10 V, RFL	—	-3.15	—	-3.15	
		I_D = 2 A, V_{GS} = -10 V, RFP	—	-9	—	-9	
		I_D = 2 A, V_{GS} = -10 V, RFL	—	-9.3	—	-9.3	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 1A, V_{GS} = -10 V, RFP	—	3.0	—	3.0	Ω
		I_D = 1A, V_{GS} = -10 V, RFL	—	3.15	—	3.15	
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V, I_D = 1 A	200	—	200	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V, V_{GS} = 0 V, f=1 MHz	—	150	—	150	pF
Output Capacitance	C_{oss}		—	80	—	80	
Reverse Transfer Capacitance	C_{rss}		—	30	—	30	
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -50 V, I_D = 1 A, R_{gen}=R_{gs}=50Ω, V_{GS} = -10 V, RFP	7(typ)	25	7(typ)	25	ns
Rise Time	t_r		15(typ)	45	15(typ)	45	
Turn-Off Delay Time	$t_{d(off)}$		14(typ)	45	14(typ)	45	
Fall Time	t_f		11(typ)	25	11(typ)	25	
		V_{GS} = -10 V, RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFL1P08, RFL1P10	—	15	—	15	°C/W
		RFP2P08, RFP2P10	—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFL1P08 RFP2P08		RFL1P10 RFP2P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2A, dI_F/dt = 50 A/μs	135 (typ.)		135 (typ.)		ns

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFL1P08, RFL1P10, RFP2P08, RFP2P10

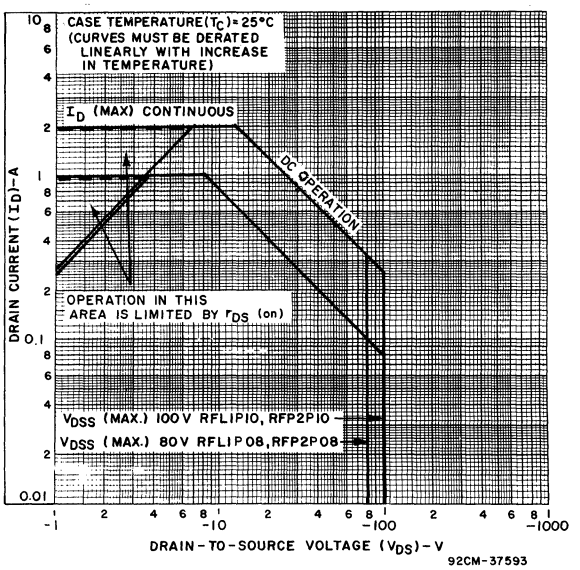


Fig. 1 - Maximum operating areas for all types.

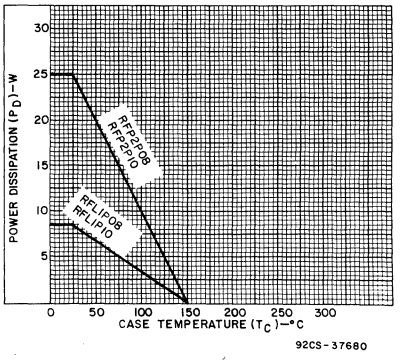


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

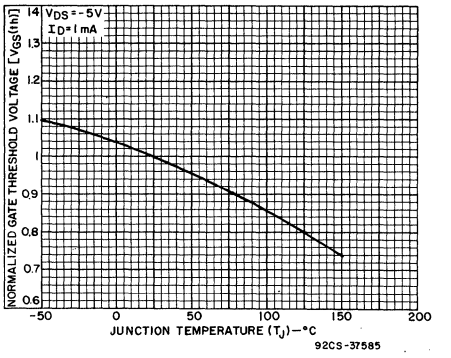


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

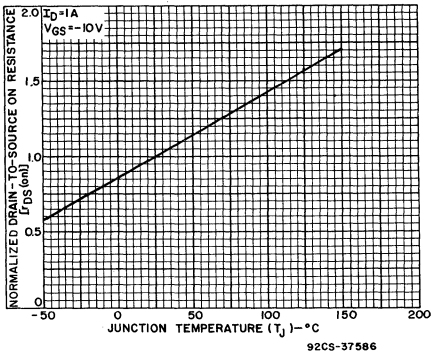


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

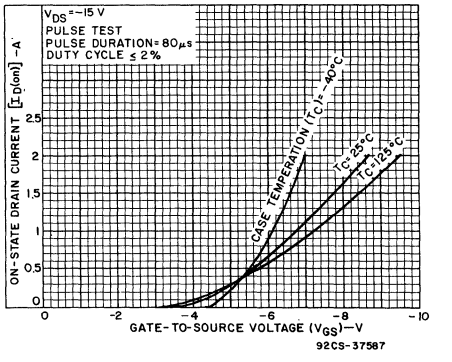


Fig. 5 - Typical transfer characteristics for all types.

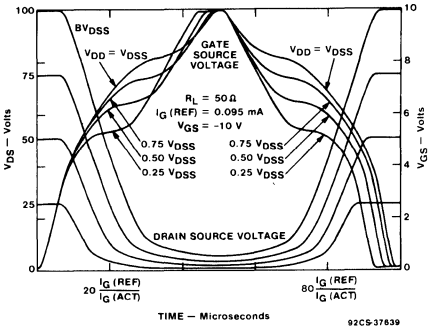


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

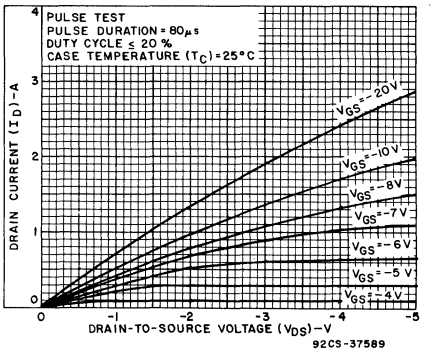


Fig. 7 - Typical saturation characteristics for all types.

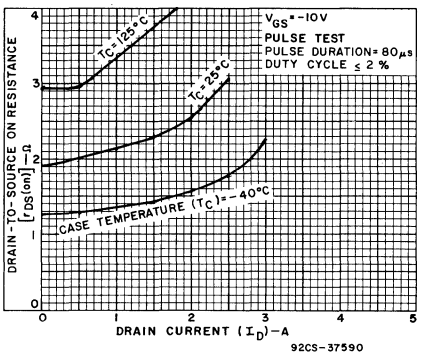


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

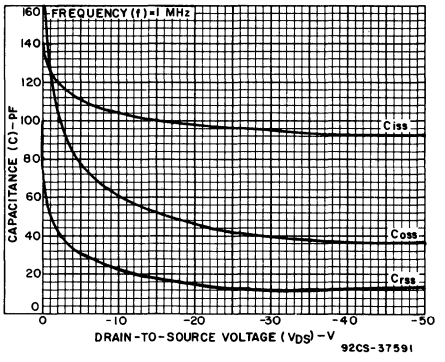


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

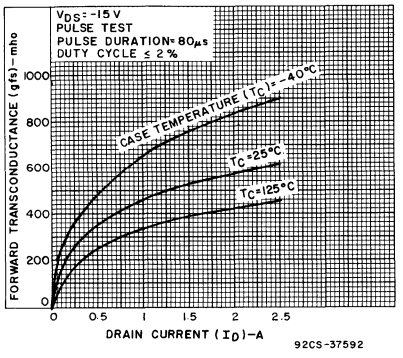


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

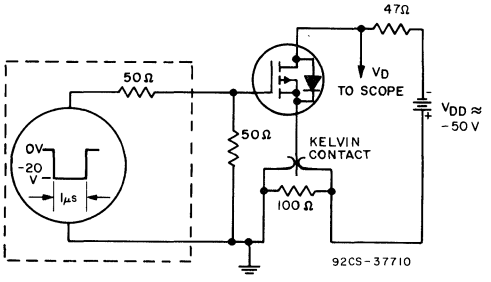


Fig. 11 - Switching time test circuit.

RFM5P12, RFM5P15, RFP5P12, RFP5P15

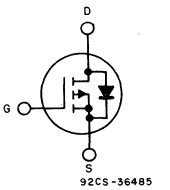
File Number **1463**

P-Channel Enhancement-Mode Power Field-Effect Transistors

5 A, 120 V — 150 V
$r_{DS(on)}$: 1Ω

Features:

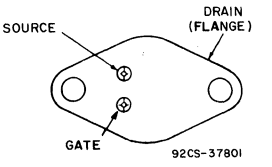
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



P-CHANNEL ENHANCEMENT MODE

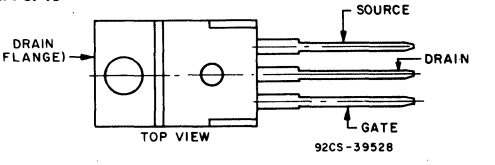
TERMINAL DESIGNATIONS

RFM5P12
RFM5P15



JEDEC TO-204AA

RFP5P12
RFP5P15



JEDEC TO-220AB

The RFM5P12 and RFM5P15 and the RFP5P12 and RFP5P15 * are P-Channel enhancement-mode silicon gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The RFM-Series types are supplied in the JEDEC TO-204AA metal package and the RFP-Series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate Zener diode.

* The RFM and RFP series were formerly RCA developmental numbers TA9320 and TA9321 respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (Tc = 25° C):*

		RFM5P12	RFM5P15		RFP5P12	RFP5P15	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-120	-150		-120	-150	V
DRAIN-GATE VOLTAGE (R_{GS} = 1MΩ)	V_{DGR}	-120	-150		-120	-150	V
GATE-SOURCE VOLTAGE	V_{GS}			±20			V
DRAIN CURRENT RMS Continuous	I_D			5			A
Pulsed	I_{DM}			15			A
POWER DISSIPATION	P_T						
@ T_C = 25°C		75	75		60	60	W
Derate above T_C = 25°C		0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}			-55 to +150			°C

RFM5P12, RFM5P15, RFP5P12, RFP5P15

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V	—	1	—	—	μA
		V_{DS} = -120 V	—	—	—	1	
		T_C = 125°C V_{DS} = -100 V	—	50	—	—	
		V_{DS} = -120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 2.5 A V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 5A V_{GS} = -10 V	—	-8	—	-8	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 2.5 A V_{GS} = -10 V	—	1	—	1	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 2.5 A	0.75	—	0.75	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	700	—	700	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	300	—	300	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz	—	100	—	100	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1/2 BV_{DSS}	20(typ.)	60	20(typ.)	60	ns
Rise Time	t_r	I_D = 2.5 A	36(typ.)	100	36(typ.)	100	
Turn-Off Delay Time	$t_{d(off)}$	R_{gen} = R_{gs} = 50Ω	63(typ.)	150	63(typ.)	150	
Fall Time	t_f	V_{GS} = 10 V	40(typ.)	100	40(typ.)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM5P12, RFM5P15	—	1.67	—	1.67	°C/W
		RFP5P12, RFP5P15	—	2.083	—	2.083	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM5P12 RFP5P12		RFM5P15 RFP5P15		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 2.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	300(typ.)		300(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFM5P12, RFM5P15, RFP5P12, RFP5P15

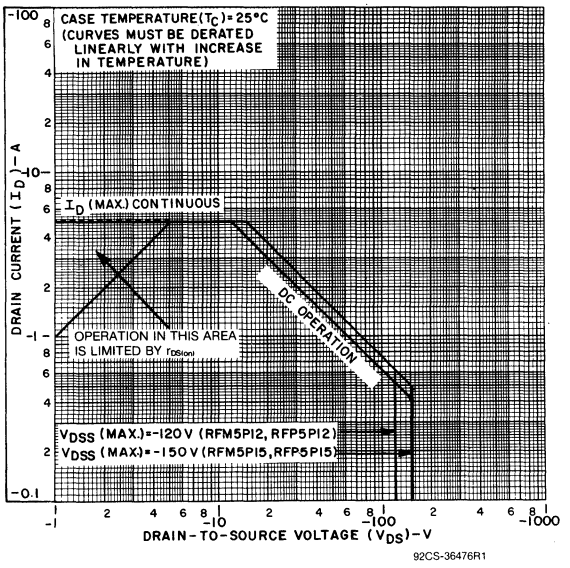


Fig. 1 - Maximum safe operating areas for all types.

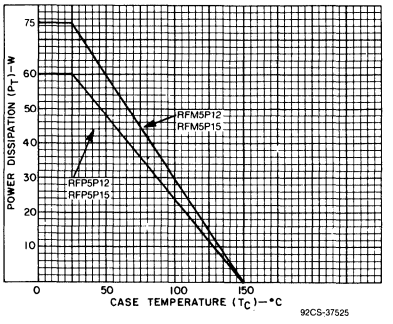


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

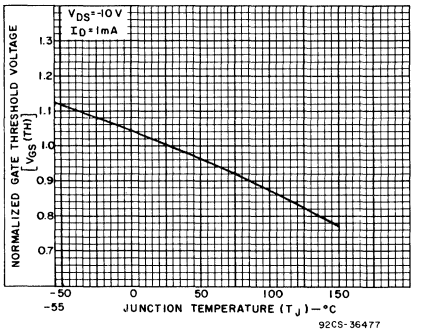


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

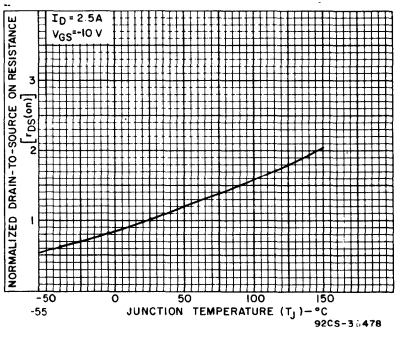


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

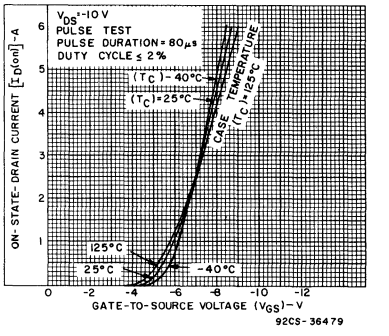


Fig. 5 - Typical transfer characteristics for all types.

RFM5P12, RFM5P15, RFP5P12, RFP5P15

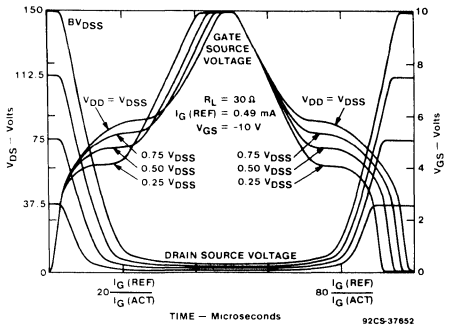


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

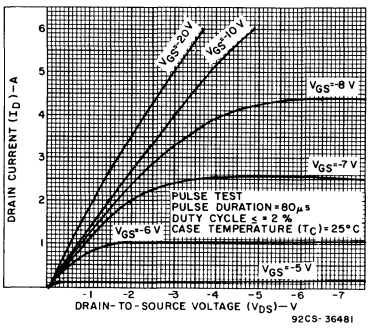


Fig. 7 - Typical saturation characteristics for all types.

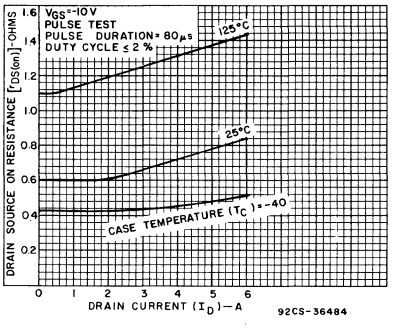


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

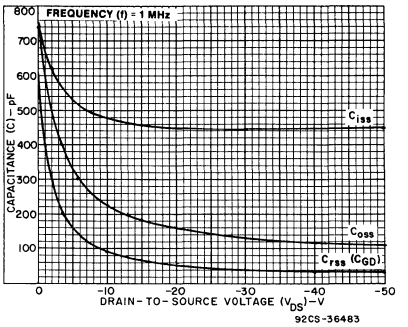


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

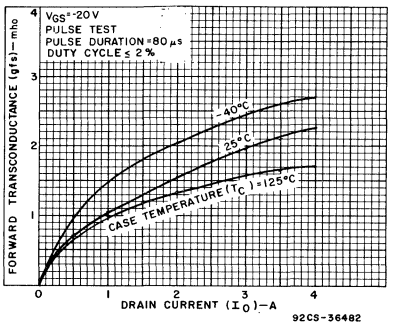


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

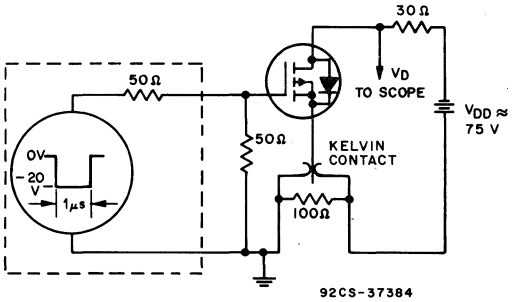


Fig. 11 - Switching Time Test Circuit.

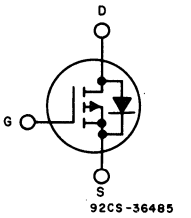
RFM6P08, RFM6P10, RFP6P08, RFP6P10

File Number **1490**

P-Channel Enhancement-Mode Power Field-Effect Transistors

6 A, 80 V — 100 V
$r_{DS}(on)$ = 0.6 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



P-CHANNEL ENHANCEMENT MODE

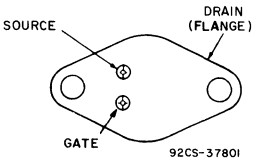
The RFM6P08 and RFM6P10 and the RFP6P08 and RFP6P10* are P-Channel enhancement-mode silicon-gate power field-effect transistors designed for high-speed applications such as switching regulators, switching converters, relay drivers, and drivers for high-power bipolar switching transistors.

The RFM-Series types are supplied in the JEDEC TO-204AA metal package and the RFP-Series types in the JEDEC TO-220AB plastic package. All these types are supplied without an internal gate Zener diode.

*The RFM and RFP series were formerly RCA developmental numbers TA9406 and TA9407, respectively.

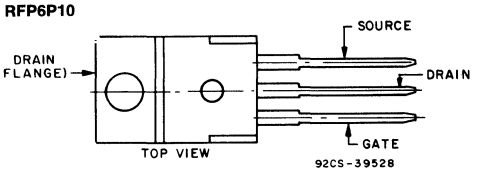
TERMINAL DESIGNATIONS

RFM6P08
RFM6P10



JEDEC TO-204AA

RFP6P08
RFP6P10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM6P08	RFM6P10		RFP6P08	RFP6P10	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) ... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			6			A
Pulsed ..... I_{DM}			20			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM6P08, RFM6P10, RFP6P08, RFP6P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=6 A V_{GS}=-10 V	—	-6	—	-6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=3 A V_{GS}=-10 V	—	0.6	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=3 A	1	—	1	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f = 1MHz	—	800	—	800	pF
Output Capacitance	C_{oss}		—	350	—	350	pF
Reverse Transfer Capacitance	C_{rss}		—	150	—	150	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V I_D=3 A R_{gen}=R_{gs}=50 Ω V_{GS}=10 V	11(typ)	60	11(typ)	60	ns
Rise Time	t_r		48(typ)	100	48(typ)	100	ns
Turn-Off Delay Time	$t_d(off)$		102(typ)	150	102(typ)	150	ns
Fall Time	t_f		70(typ)	100	70(typ)	100	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM6P08, RFM6P10	—	1.67	—	1.67	°C/W
		RFP6P08, RFP6P10	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM6P08 RFP6P08		RFM6P10 RFP6P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=3 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=50 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM6P08, RFM6P10, RFP6P08, RFP6P10

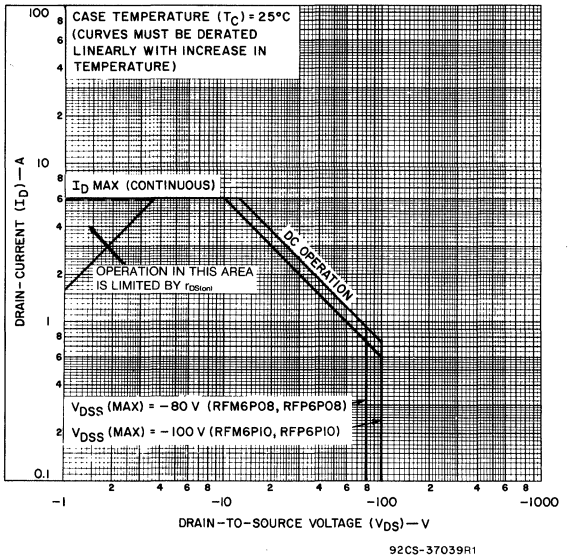


Fig. 1 — Maximum safe operating areas for all types.

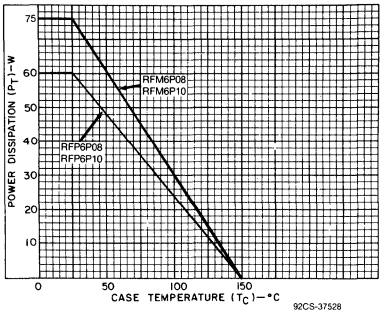


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

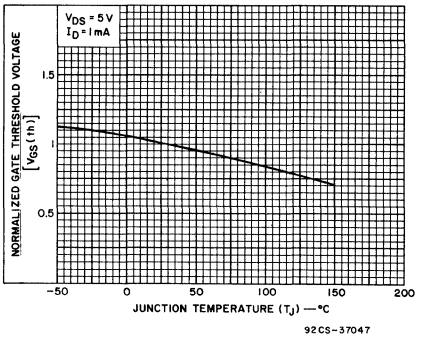


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

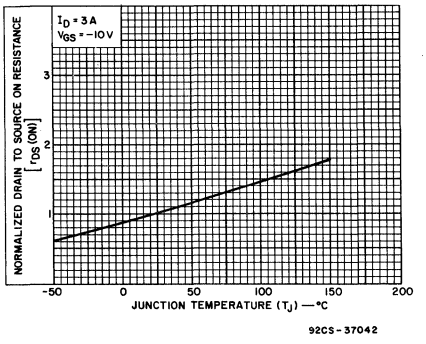


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

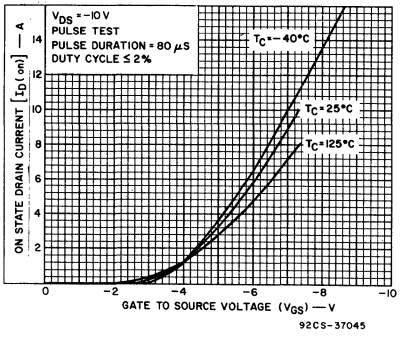


Fig. 5 — Typical transfer characteristics for all types.

RFM6P08, RFM6P10, RFP6P08, RFP6P10

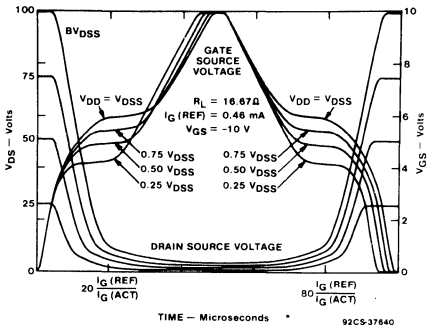


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

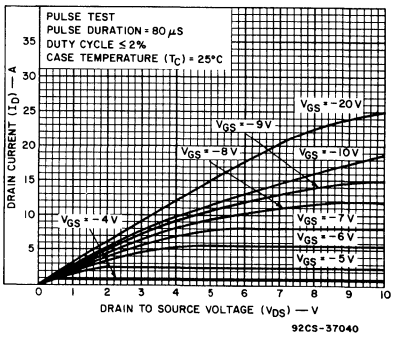


Fig. 7 — Typical saturation characteristics for all types.

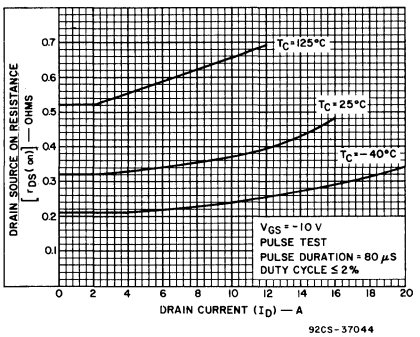


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

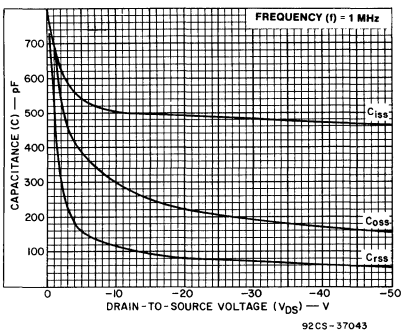


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

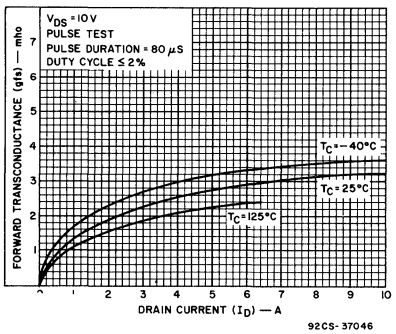


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

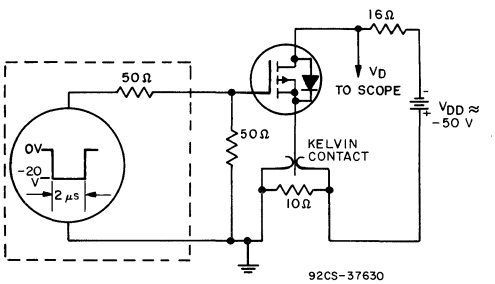


Fig. 11 - Switching Time Test Circuit.

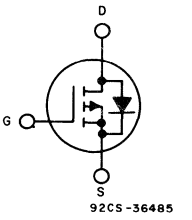
RFM8P08, RFM8P10, RFP8P08, RFP8P10

File Number **1496**

P-Channel Enhancement-Mode Power Field-Effect Transistors

8 A, -80 V and -100 V
$r_{DS}(on)$ = 0.4 Ω

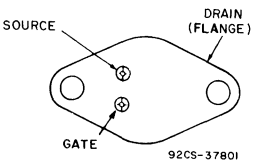
Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



P-CHANNEL ENHANCEMENT MODE

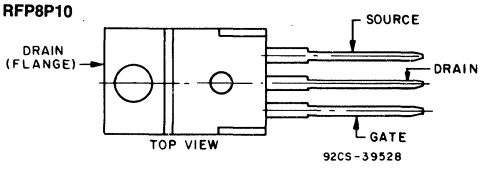
TERMINAL DESIGNATIONS

RFM8P08
RFM8P10



JEDEC TO-204AA

RFP8P08
RFP8P10



JEDEC TO-220AB

The RFM8P08 and RFM8P10 and the RFP8P08 and RFP8P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9410 and TA9411, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM8P08	RFM8P10		RFP8P08	RFP8P10	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	-80	-100		-80	-100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	-80	-100		-80	-100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			8			A
Pulsed ..... I_{DM}			20			A
POWER DISSIPATION @ T_C=25°C ..... P_T	100	100		75	75	W
Derate above T_C=25°C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM8P08, RFM8P10, RFP8P08, RFP8P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125°C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	-1.6	—	-1.6	V
		I_D=8 A V_{GS}=-10 V	—	-4.0	—	-4.0	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=-10 V	—	.4	—	.4	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=4 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	240	—	240	pF
Turn-On Delay Time	$t_d(on)$	V_{DD} = 50 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=4 A	70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	166(typ)	275	166(typ)	275	ns
Fall Time	t_f	V_{GS}=-10 V	94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8P08, RFM8P08	—	1.25	—	1.25	°C/W
		RFP8P10, RFP8P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8P08 RFP8P08		RFM8P10 RFP8P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD}	I_{SD} = 4A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A d_{IF}/d_t = 100A/μs	200(typ.)		200(typ.)		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFM8P08, RFM8P10, RFP8P08, RFP8P10

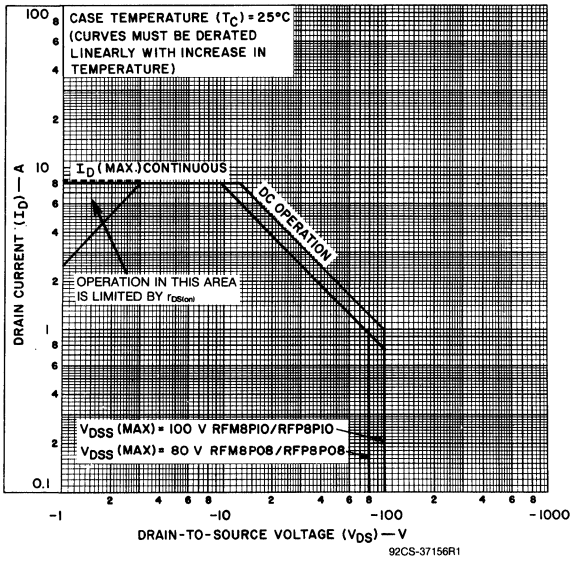


Fig. 1 — Maximum operating areas for all types.

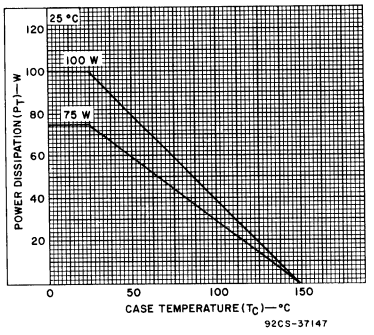


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

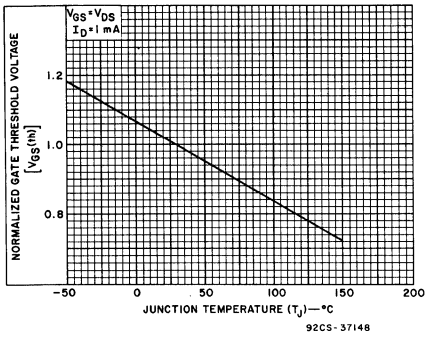


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

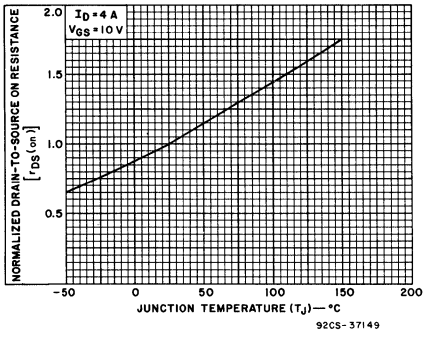


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

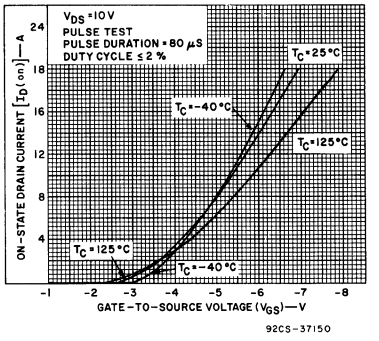


Fig. 5 — Typical transfer characteristics for all types.

RFM8P08, RFM8P10, RFP8P08, RFP8P10

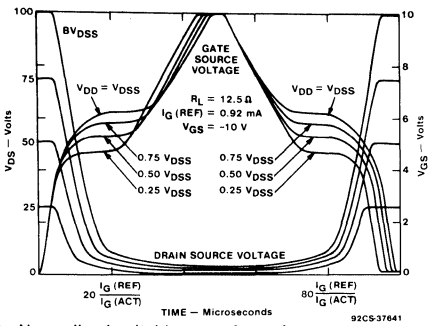


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

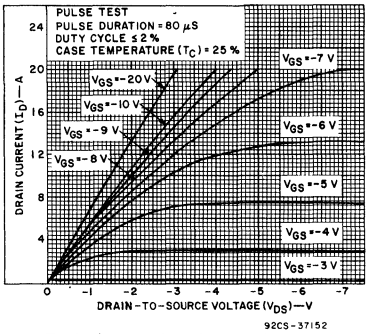


Fig. 7 — Typical saturation characteristics for all types.

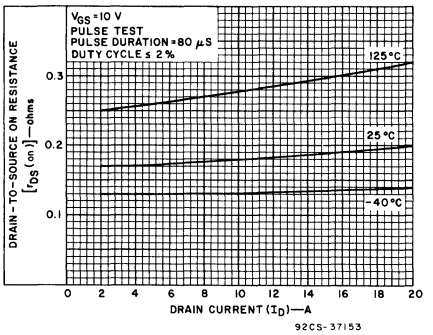


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

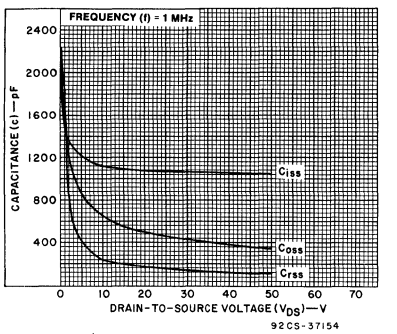


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

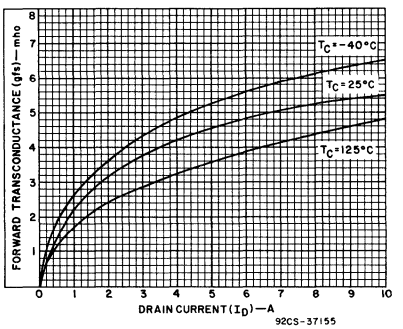


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

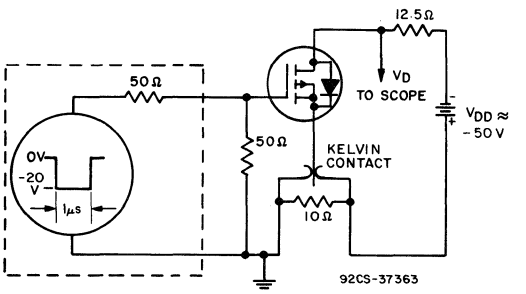


Fig. 11 — Switching Time Test Circuit.

RFM10P12, RFM10P15, RFP10P12, RFP10P15

File Number **1595**

P-Channel Enhancement-Mode Power Field-Effect Transistors

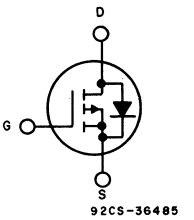
10 A, -120V and -150 V

$r_{DS(on)}$ = 0.5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

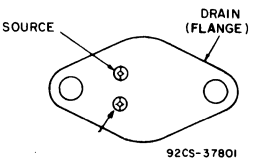
The RFM10P12 and RFM10P15 and the RFP10P12 and RFP10P15* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental TA9404 and TA9405, respectively.

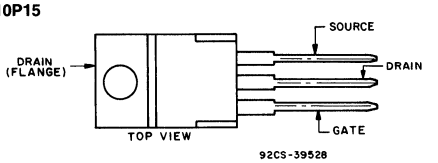
TERMINAL DESIGNATIONS

RFM10P12
RFM10P15



JEDEC TO-204AA

RFP10P12
RFP10P15



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

	RFM10P12	RFM10P15	RFP10P12	RFP10P15	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	-120	-150	-120	-150	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ) ..... V_{DGR}	-120	-150	-120	-150	V
GATE-SOURCE VOLTAGE ..... V_{GS}	±20				V
DRAIN CURRENT, RMS Continuous ..... I_D	10				A
Pulsed ..... I_{DM}	30				A
POWER DISSIPATION @ T_C = 25°C ..... P_T	100	100	75	75	W
Derate above T_C = 25°C	0.8	0.8	0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}	-55 to +150				°C

RFM10P12, RFM10P15, RFP10P12, RFP10P15

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-120	—	-150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100 V	—	1	—	—	μA
		V_{DS} = -120 V	—	—	—	1	
		T_C = 125° C V_{DS} = -100 V	—	50	—	—	
		V_{DS} = -120 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	-2.5	—	-2.5	V
		I_D = 10 A V_{GS} = -10 V	—	-6.0	—	-6.0	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = -10 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V I_D = 5 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V V_{GS} = 0 V f = 1MHz	—	1700	—	1700	pF
Output Capacitance	C_{oss}		—	600	—	600	
Reverse Transfer Capacitance	C_{rss}		—	150	—	150	
Turn-On Delay Time	$t_{d(on)}$	V_{DS} = -75 V I_D = 5 A R_{gen} = R_{gs} = 50 Ω V_{GS} = -10 V	24(typ)	50	24(typ)	50	ns
Rise Time	t_r		74(typ)	150	74(typ)	150	
Turn-Off Delay Time	$t_{d(off)}$		138(typ)	225	138(typ)	225	
Fall Time	t_f		61(typ)	100	61(typ)	100	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10P12, RFM10P15	—	1.25	—	1.25	°C/W
		RFP10P12, RFP10P15	—	1.67	—	1.67	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10P12 RFP10P12		RFM10P15 RFP10P15		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	210 (typ.)		210 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

RFM10P12, RFM10P15, RFP10P12, RFP10P15

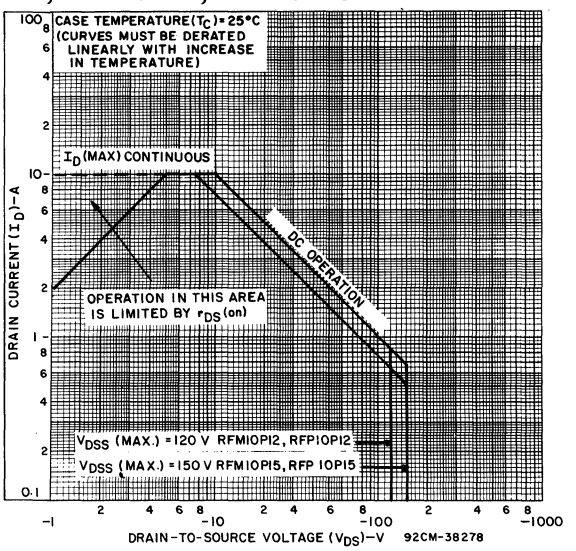


Fig. 1 - Maximum safe operating areas for all types.

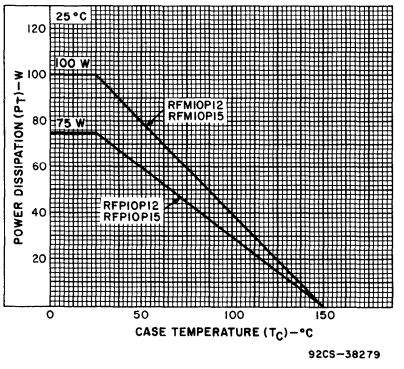


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

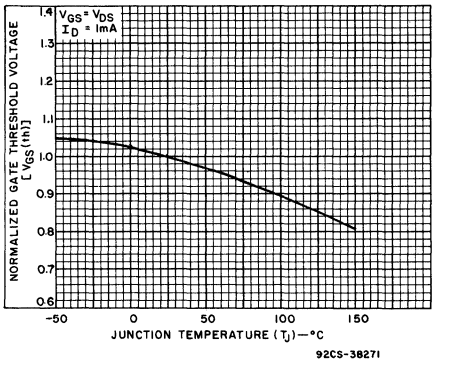


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

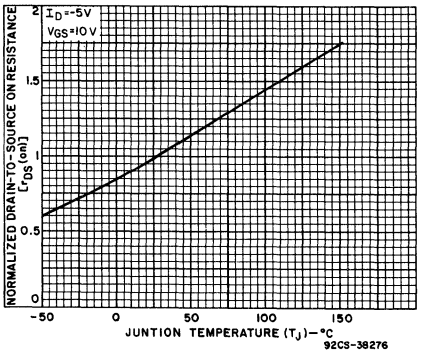


Fig. 4 - Normalized drain-to-source on resistance as as function of junction temperature for all types.

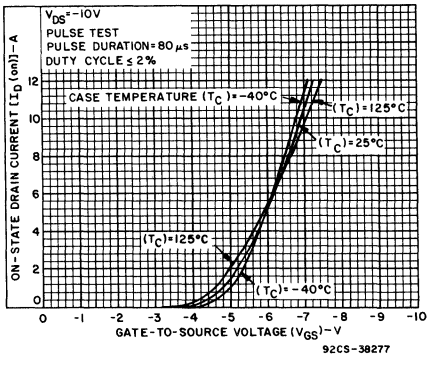


Fig. 5 - Typical transfer characteristics for all types.

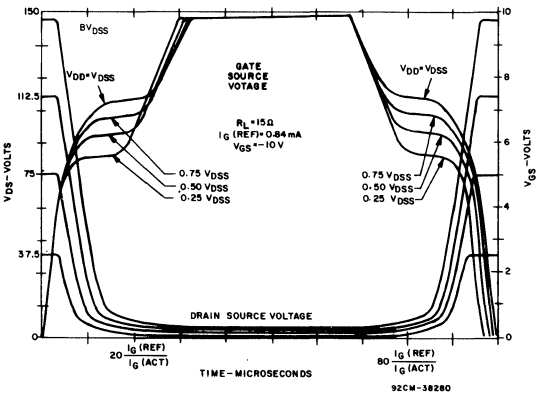


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

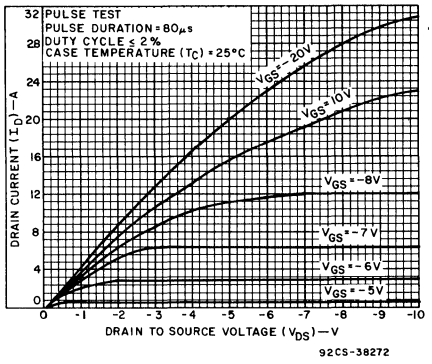


Fig. 7 - Typical saturation characteristics for all types.

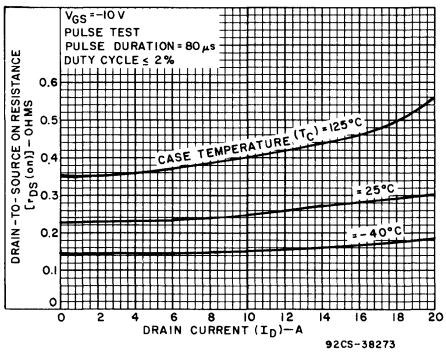


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

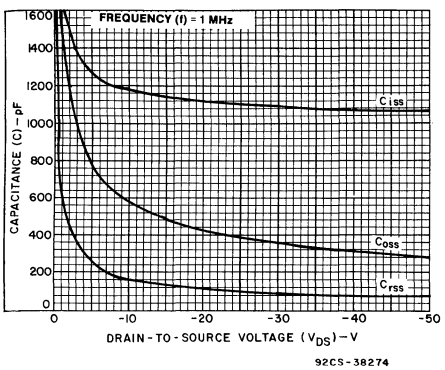


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

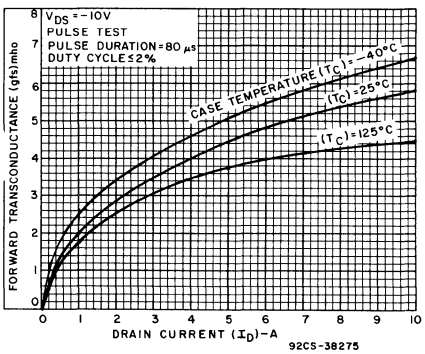


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

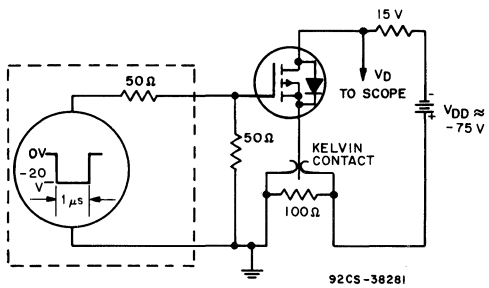


Fig. 11 - Switching Time Test Circuit.

RFM12P08, RFM12P10, RFP12P08, RFP12P10

File Number **1495**

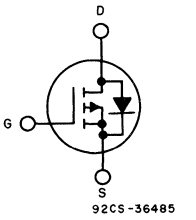
Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power Field-Effect Transistors

12 A, -80 V and -100 V
$r_{DS}(on)$ = 0.3 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



P-CHANNEL ENHANCEMENT MODE

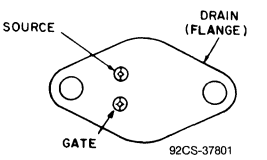
The RFM12P08 and RFM12P10 and the RFP12P08 and RFP12P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFM-types are supplied in the JEDEC TO-204AA steel package and the RFP-types in the JEDEC TO-220AB plastic package.

*The RFM and RFP series were formerly RCA developmental numbers TA9410 and TA9411, respectively.

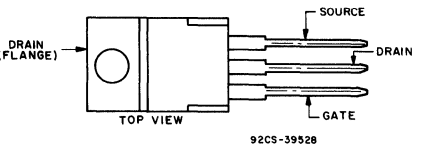
TERMINAL DESIGNATIONS

RFM12P08
RFM12P10



JEDEC TO-204AA

RFP12P08
RFP12P10



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12P08	RFM12P10		RFP12P08	RFP12P10	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	-80	-100		-80	-100	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) .... V_{DGR}	-80	-100		-80	-100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±20			V
DRAIN CURRENT, RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C ..... P_T	100	100		75	75	W
Derate above T_C=25°C	0.8	0.8		0.6	0.6	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}			-55 to +150			°C

RFM12P08, RFM12P10, RFP12P08, RFP12P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-65 V V_{DS}=-80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=-65 V V_{DS}=-80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	-1.8	—	-1.8	V
		I_D=12 A V_{GS}=-10 V	—	-4.8	—	-4.8	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=-10 V	—	.3	—	.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=6 A	2	—	2	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V	—	1500	—	1500	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	700	—	700	pF
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	240	—	240	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V	18(typ)	60	18(typ)	60	ns
Rise Time	t_r	I_D=6 A	90(typ)	175	90(typ)	175	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50 Ω	144(typ)	275	144(typ)	275	ns
Fall Time	t_f	V_{GS}=-10 V	94(typ)	175	94(typ)	175	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12P08, RFM12P10	—	1.25	—	1.25	°C/W
		RFP12P08, RFP12P10	—	1.67	—	1.67	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12P08 RFP12P08		RFM12P10 RFP12P10		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM12P08, RFM12P10, RFP12P08, RFP12P10

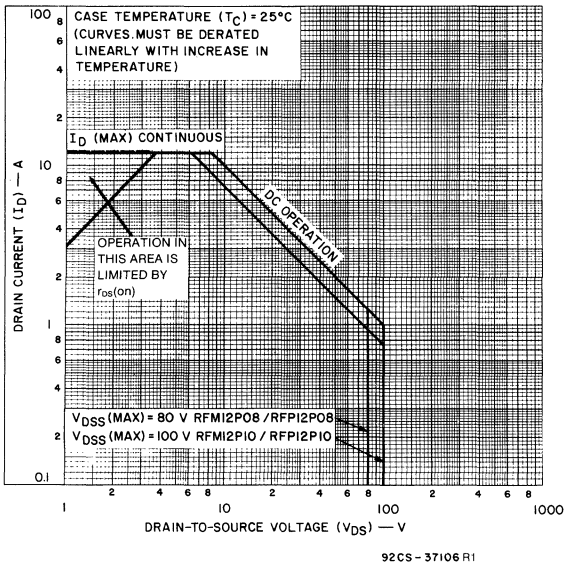


Fig. 1 — Maximum safe operating areas for all types.

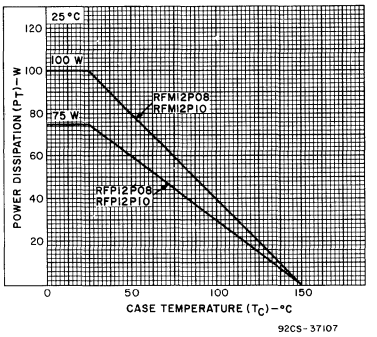


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

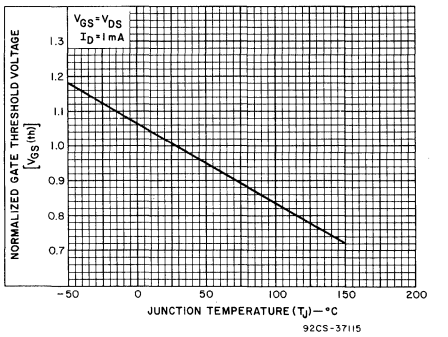


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

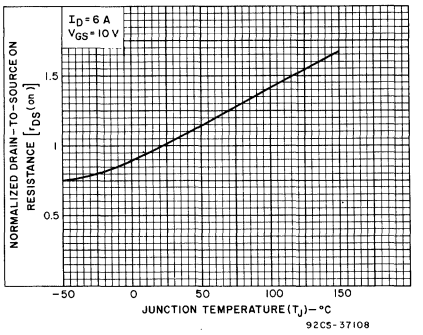


Fig. 4 — Normalized drain-to-source on resistance as a function of junction temperature for all types.

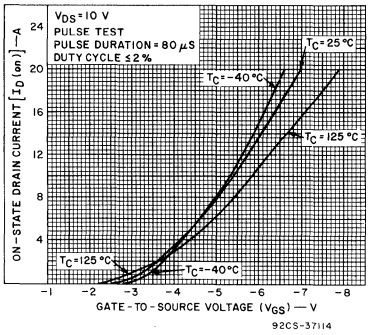


Fig. 5 — Typical transfer characteristics for all types.

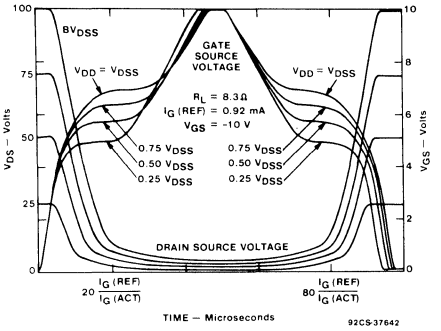


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

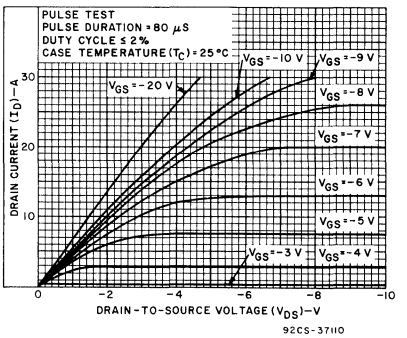


Fig. 7 — Typical saturation characteristics for all types.

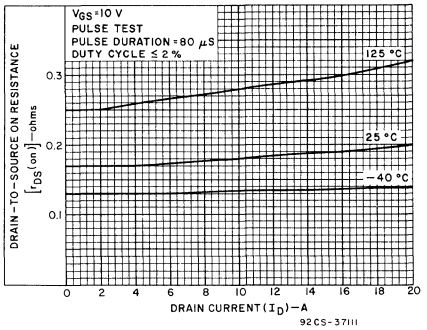


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

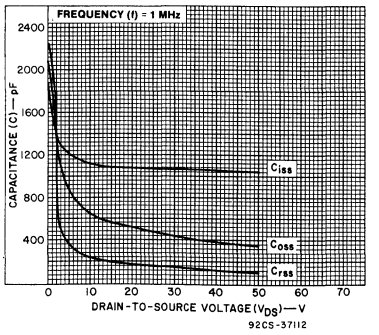


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

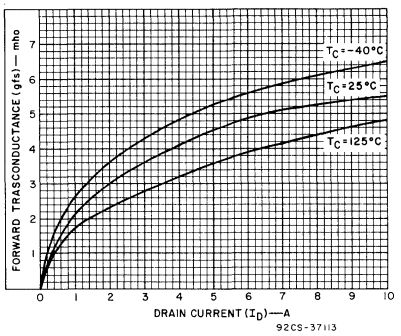


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

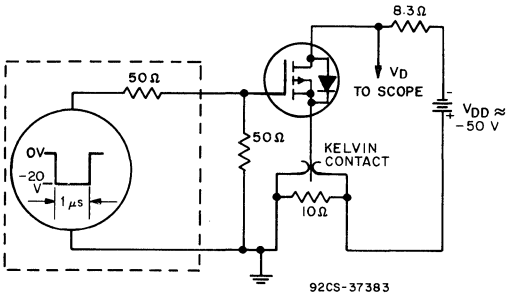


Fig. 11 — Switching Time Test Circuit

RFH25P08, RFH25P10

File Number **1632**

Power MOS Field-Effect Transistors

P-Channel Enhancement-Mode Power Field-Effect Transistors

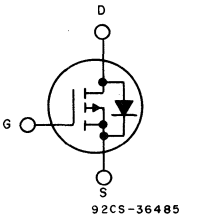
25 A, -80 V - -100 V

$r_{DS(on)}$ = 0.15 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*
- *High-current, low-inductance package*

TERMINAL DIAGRAM



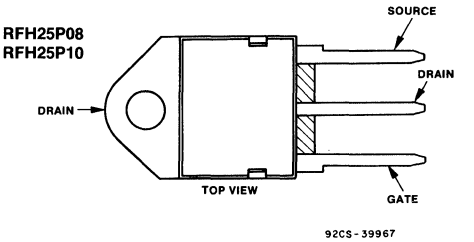
P-CHANNEL ENHANCEMENT MODE

The RFH25P08 and RFH25P10* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFH-types are supplied in the JEDEC TO-218AC plastic package.

*The RFH25P08 and RFH25P10 types were formerly RCA developmental numbers TA9577A and TA9577B respectively.

TERMINAL DESIGNATIONS



JEDEC TO-218AC

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

		RFH25P08	RFH25P10	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-80	-100	V
DRAIN-GATE VOLTAGE, R_{gs} = 1 MΩ	V_{DGR}	-80	-100	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	25		A
Pulsed	I_{DM}	60		A
POWER DISSIPATION @ T_C = 25° C	P_T	150		W
Derate above T_C = 25° C		1.2		W/° C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFH25P08, RFH25P10

ELECTRICAL CHARACTERISTICS, at Case Temperature (T_C) = 25° C unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFH25P08		RFH25P10		
			Min.	Max.	Min.	Max.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	-80	—	-100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -80 V	—	—	—	1	μA
		V_{DS} = -65 V	—	1	—	—	
		T_C = 125° C V_{DS} = -80 V	—	—	—	50	
		V_{DS} = -65 V	—	50	—	—	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = -10 V	—	-1.88	—	-1.88	V
		I_D = 25 A V_{GS} = -10 V	—	-4.5	—	-4.5	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D = 12.5 A V_{GS} = -10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = -10 V I_D = 12.5 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS} = -25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	500	—	500	
Turn-On Delay Time	$t_d(on)$	V_{DD} = -50 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r	I_D = 12.5 A	165(typ)	250	165(typ)	250	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=R_{gs}=50Ω	270(typ)	400	270(typ)	400	
Fall Time	t_f	V_{GS} = -10 V	165(typ)	250	165(typ)	250	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFH25P08, RFH25P10 Series	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS				UNITS
			RFH25P08		RFH25P10		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage	V_{SD} *	I_{SD} = 12.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	300 (typ.)		300 (typ.)		ns

* Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFH25P08, RFH25P10

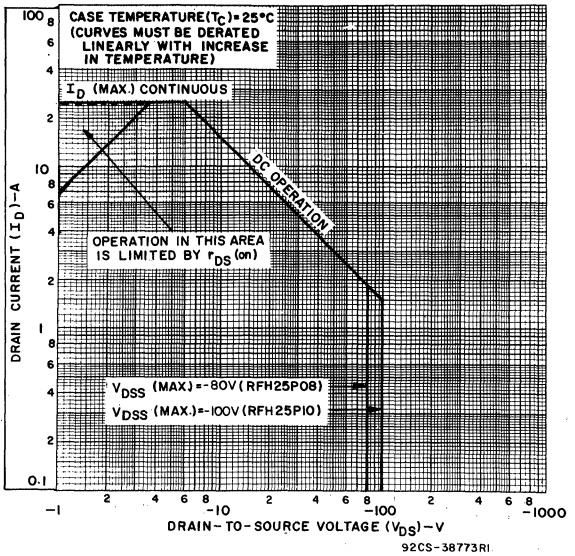


Fig. 1 - Maximum safe operating areas for all types.

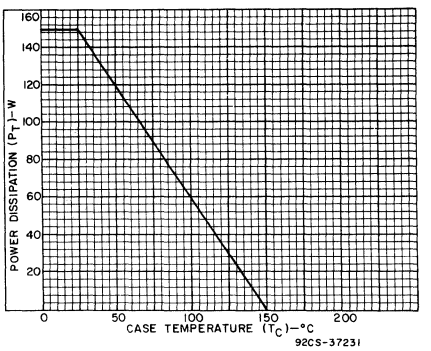


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

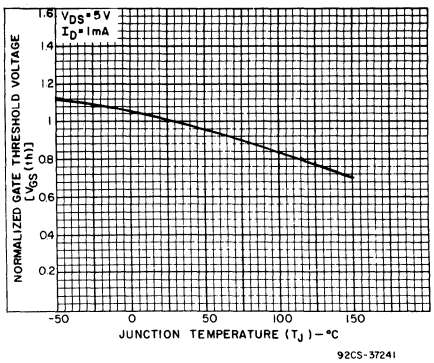


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

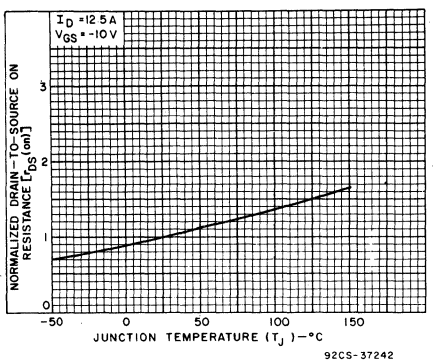


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

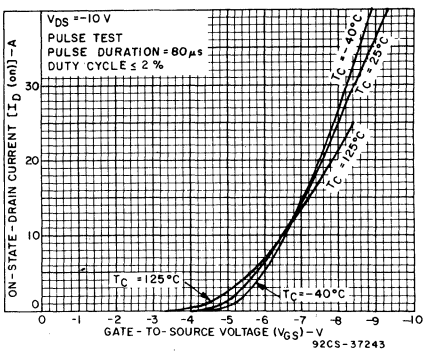


Fig. 5 - Typical transfer characteristics for all types.

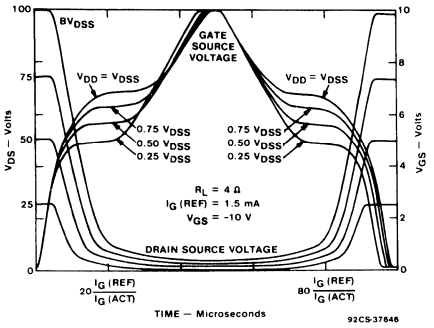


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

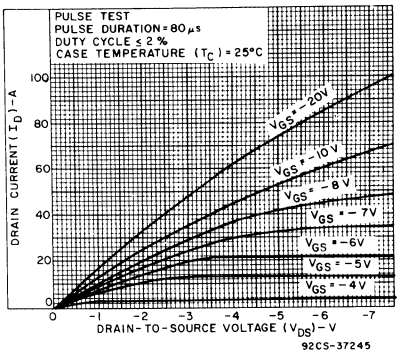


Fig. 7 - Typical saturation characteristics for all types.

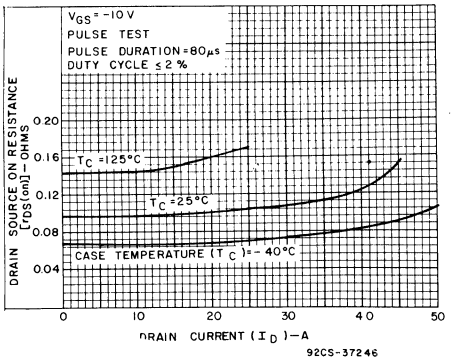


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

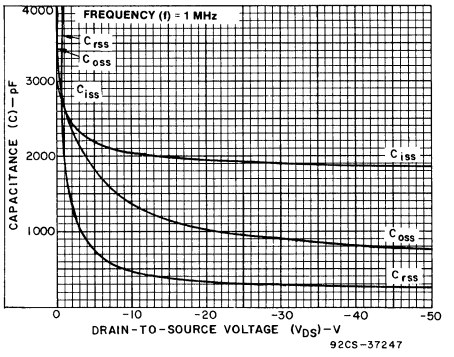


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

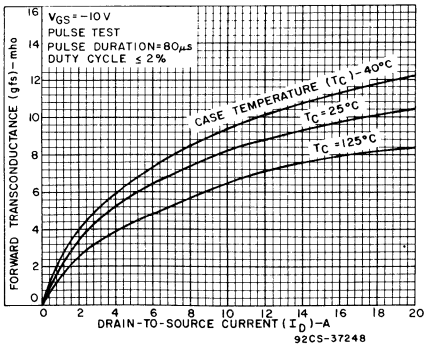


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

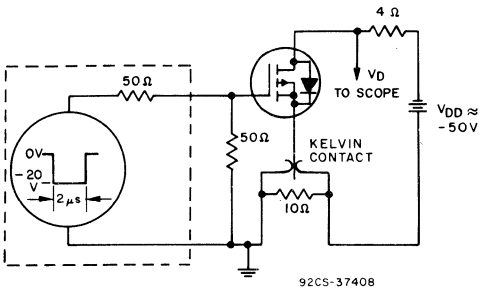


Fig. 11 - Switching Time Test Circuit.

RFK25P08, RFK25P10

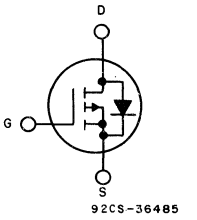
File Number **1516**

P-Channel Enhancement-Mode Power Field-Effect Transistors

25 A, -100 V — -80 V
$r_{DS}(on)$: 0.15Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



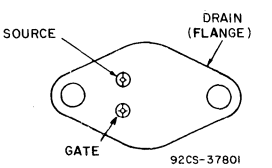
P-CHANNEL ENHANCEMENT MODE

The RFK25P10 and RFK25P08* are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFK-types are supplied in the JEDEC TO-204AE steel package.

*The RFK25P10 and RFK25P08 types were formerly RCA developmental numbers TA9412A and TA9412B, respectively.

TERMINAL DESIGNATIONS



JEDEC TO-204AE

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25°C):*

		RFK25P10	RFK25P08	
DRAIN-SOURCE VOLTAGE	V_{DSS}	-100	-80	V
DRAIN-GATE VOLTAGE, R_{GS}=1 MΩ)	V_{DGR}	-100	-80	V
GATE-SOURCE VOLTAGE	V_{GS}	±20		V
DRAIN CURRENT, RMS Continuous	I_D	25		A
Pulsed	I_{DM}	60		A
POWER DISSIPATION	P_T			
@ T_C = 25°C		150		W
Derate above T_C=25°C		1.2		W/°C
OPERATING AND STORAGE TEMPERATURE	T_j, T_{stg}	-55 to +150		°C

RFK25P08, RFK25P10

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25°C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25P10		RFK25P08		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=1 mA V_{GS}=0	-100	—	-80	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	-2	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80 V	—	1	—	—	μA
		V_{DS}=-65 V	—	—	—	1	
		T_C=125°C V_{DS}=-80 V	—	50	—	—	
		V_{DS}=-65 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}= ± 20 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=12.5 A V_{GS}=-10 V	—	-2.5	—	-2.5	V
		I_D=25 A V_{GS}=-10 V	—	-6	—	-6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=12.5 A V_{GS}=-10 V	—	0.15	—	0.15	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=-10 V I_D=12.5 A	4	—	4	—	mho
Input Capacitance	C_{iss}	V_{DS}=-25 V	—	3000	—	3000	pF
Output Capacitance	C_{oss}	V_{GS}=0 V	—	1500	—	1500	
Reverse Transfer Capacitance	C_{rss}	f = 1MHz	—	500	—	500	
Turn-On Delay Time	t_d (on)	V_{DD}=-50 V	35(typ)	50	35(typ)	50	ns
Rise Time	t_r	I_D=12.5 A	165(typ)	250	165(typ)	250	
Turn-Off Delay Time	t_d (off)	R_{gen}=R_{gs}=50 Ω	270(typ)	400	270(typ)	400	
Fall Time	t_f	V_{GS}=-10 V	165(typ)	250	165(typ)	250	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	RFK25P10, RFK25P08	—	0.83	—	0.83	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFK25P10		RFK25P08		
			Min.	Max.	Min.	Max.	
Diode Forward Voltage*	V_{SD}	I_{SD}=12.5 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	300 typ.		300 typ.		ns

*Pulse Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RFK25P08, RFK25P10

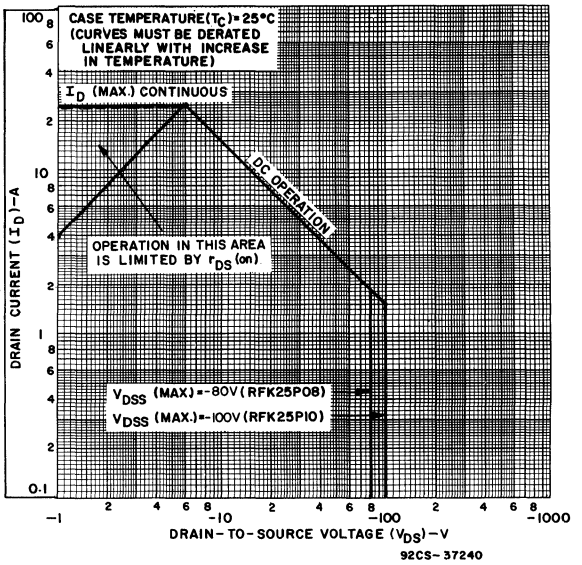


Fig. 1 - Maximum safe operating areas for all types.

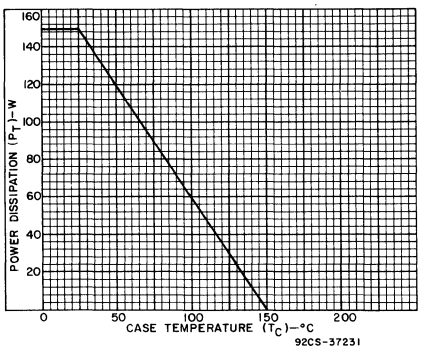


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

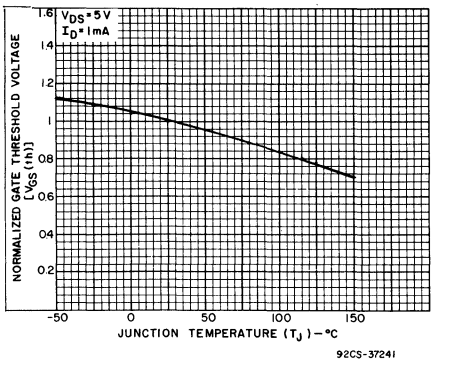


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

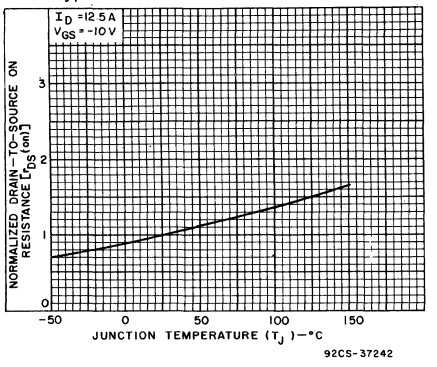


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

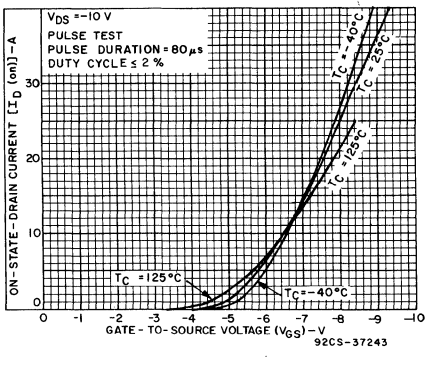


Fig. 5 - Typical transfer characteristics for all types.

RFK25P08, RFK25P10

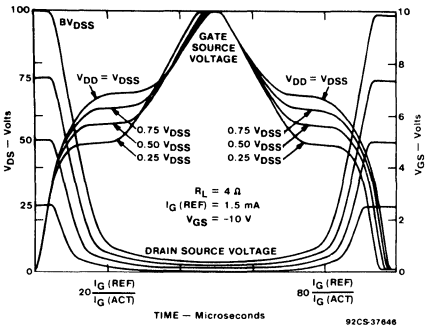


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

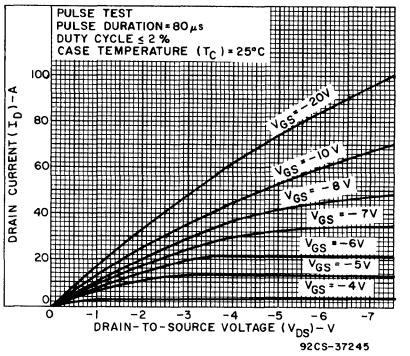


Fig. 7 - Typical saturation characteristics for all types.

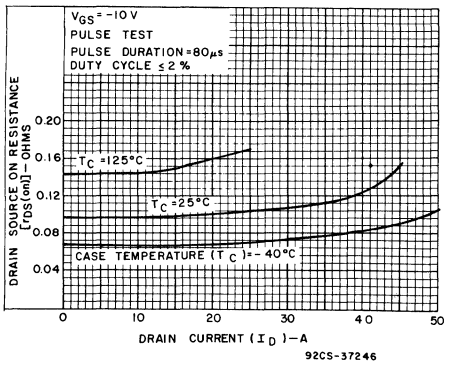


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

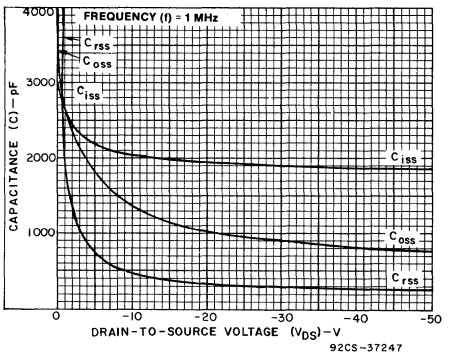


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

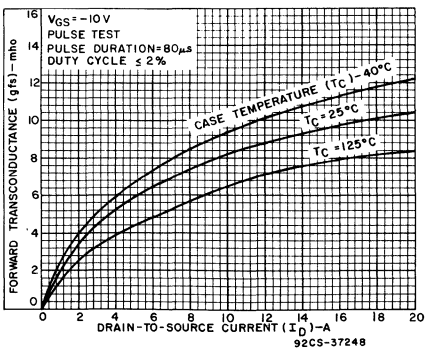


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

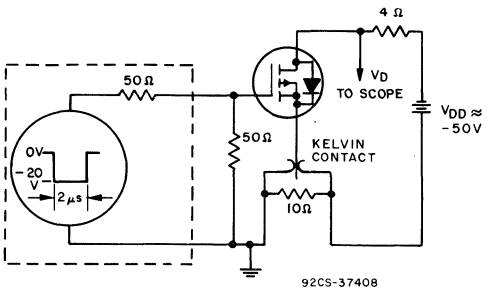


Fig. 11 - Switching time test circuit.

IRFF110, IRFF111, IRFF112, IRFF113

File Number **1562**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

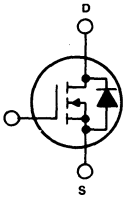
3.0A and 3.5A, 60V-100V

$r_{DS}(on)$ = 0.6 Ω and 0.8 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

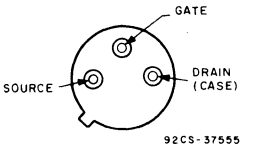
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

The IRFF110, IRFF111, IRFF112 and IRFF113 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

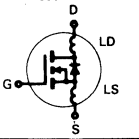
Absolute Maximum Ratings

	Parameter	IRFF110	IRFF111	IRFF112	IRFF113	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	14	14	12	12	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	15 (See Fig. 14)				W
	Linear Derating Factor	0.12 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		14	14	12	12	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF110 IRFF112	100	–	–	V	V_{GS} = 0V
		IRFF111 IRFF113	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF110 IRFF111	3.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF112 IRFF113	3.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF110 IRFF111	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 1.5A
		IRFF112 IRFF113	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	135	200	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D ≈ 1.5A, Z_o ≈ 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D ≈ 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	8.33	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF110 IRFF111	–	–	3.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF112 IRFF113	–	–	3.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF110 IRFF111	–	–	14	A	
		IRFF112 IRFF113	–	–	12	A	
V_{SD}	Diode Forward Voltage ②	IRFF110 IRFF111	–	–	2.5	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
		IRFF112 IRFF113	–	–	2.0	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	200	–	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.0	–	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRFF110, IRFF111, IRFF112, IRFF113

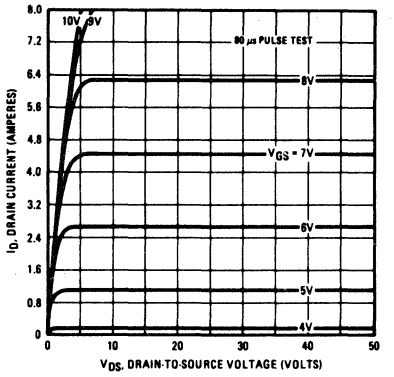


Fig. 1 – Typical Output Characteristics

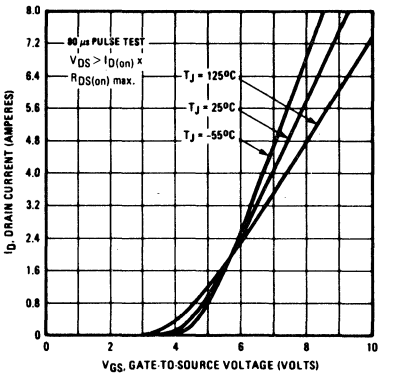


Fig. 2 – Typical Transfer Characteristics

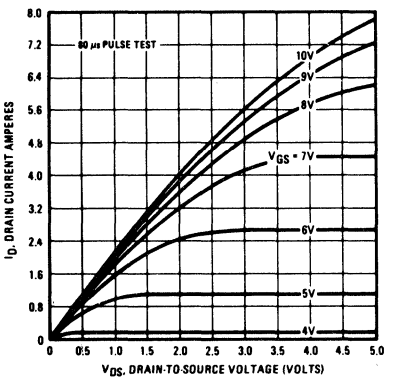


Fig. 3 – Typical Saturation Characteristics

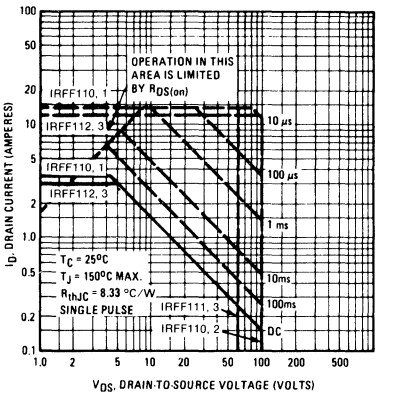


Fig. 4 – Maximum Safe Operating Area

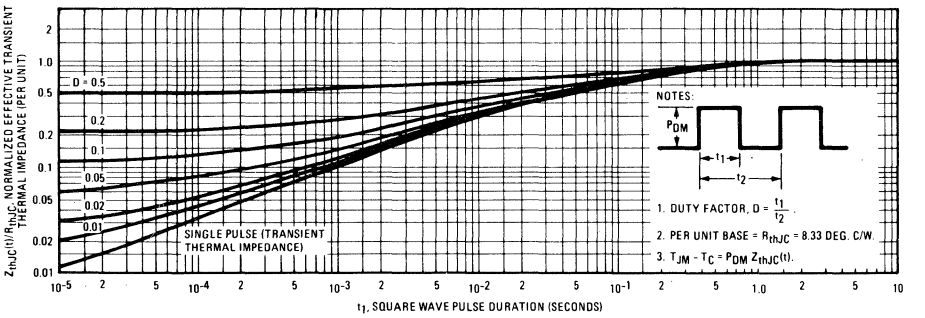


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

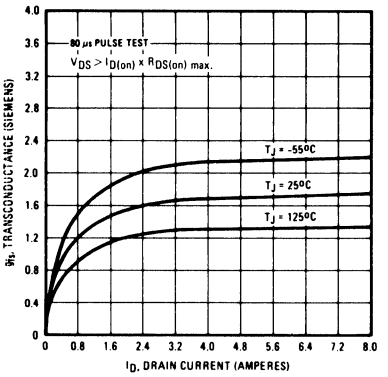


Fig. 6 – Typical Transconductance Vs. Drain Current

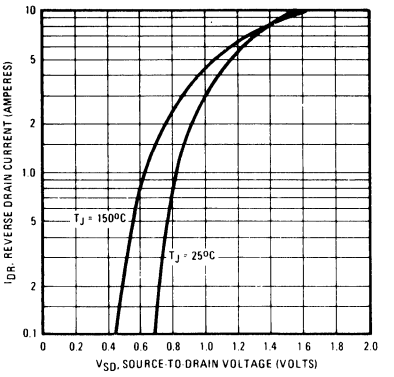


Fig. 7 – Typical Source-Drain Diode Forward Voltage

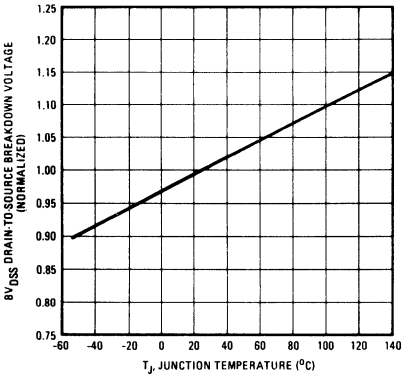


Fig. 8 – Breakdown Voltage Vs. Temperature

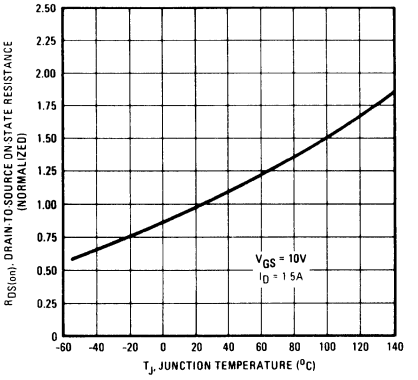


Fig. 9 – Normalized On-Resistance Vs. Temperature

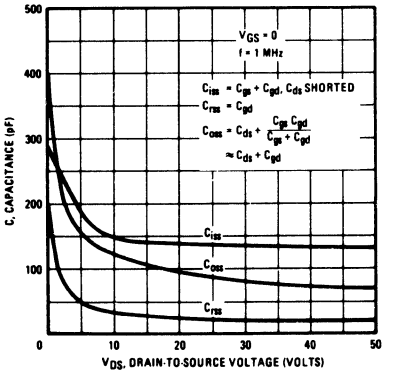


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

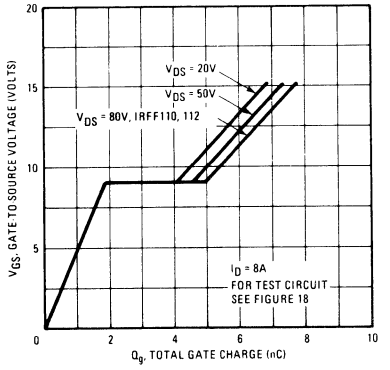


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRFF110, IRFF111, IRFF112, IRFF113

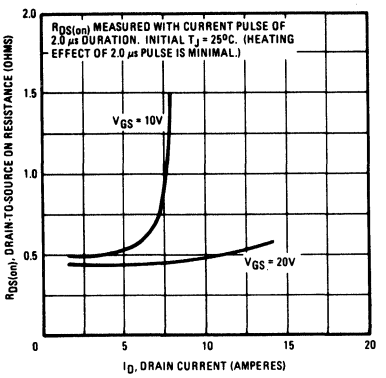


Fig. 12 – Typical On-Resistance Vs. Drain Current

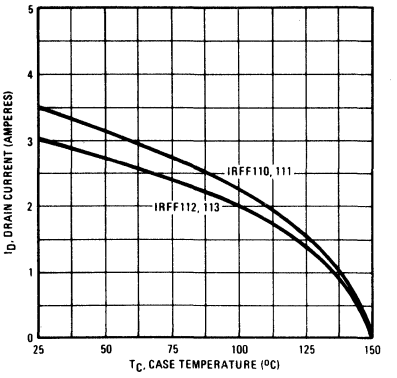


Fig. 13 – Maximum Drain Current Vs. Case Temperature

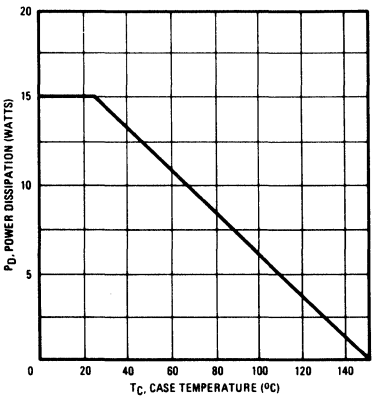


Fig. 14 – Power Vs. Temperature Derating Curve

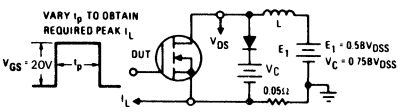


Fig. 15 – Clamped Inductive Test Circuit

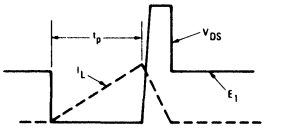


Fig. 16 – Clamped Inductive Waveforms

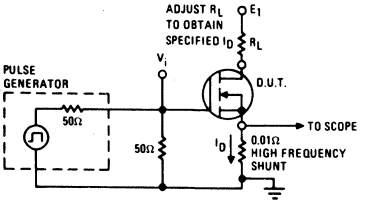


Fig. 17 – Switching Time Test Circuit

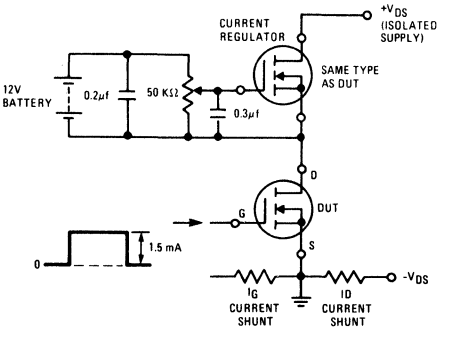


Fig. 18 – Gate Charge Test Circuit

File Number **1563**

IRFF120, IRFF121, IRFF122, IRFF123

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

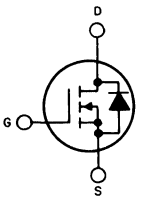
5.0A and 6.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

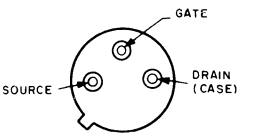
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

The IRFF120, IRFF121, IRFF122 and IRFF123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

Absolute Maximum Ratings

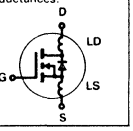
	Parameter	IRFF120	IRFF121	IRFF122	IRFF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)* ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	24	24	20	20	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		24	24	20	20	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF120, IRFF121, IRFF122, IRFF123

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF120 IRFF122	100	–	–	V	V_{GS} = 0V
		IRFF121 IRFF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF120 IRFF121	6.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF122 IRFF123	5.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF120 IRFF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 3.0A
		IRFF122 IRFF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 3.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	37	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

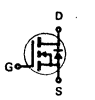


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.25	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF120 IRFF121	–	–	6.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF122 IRFF123	–	–	5.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF120 IRFF121	–	–	24	A	
		IRFF122 IRFF123	–	–	20	A	
V_{SD}	Diode Forward Voltage ②	IRFF120 IRFF121	–	–	2.5	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
		IRFF122 IRFF123	–	–	2.3	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.2	–	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

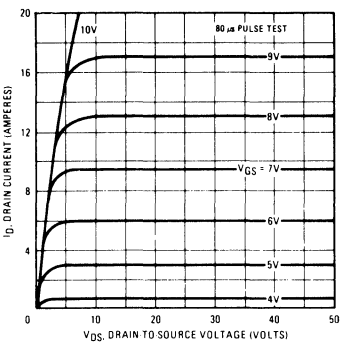


Fig. 1 – Typical Output Characteristics

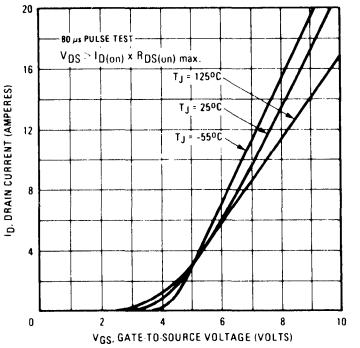


Fig. 2 – Typical Transfer Characteristics

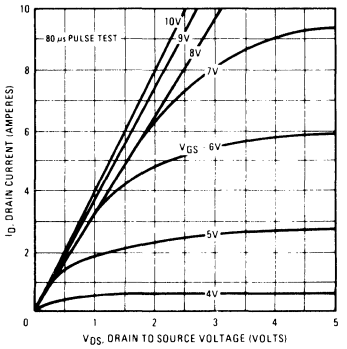


Fig. 3 – Typical Saturation Characteristics

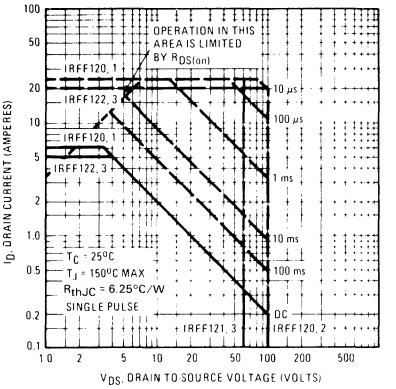


Fig. 4 – Maximum Safe Operating Area

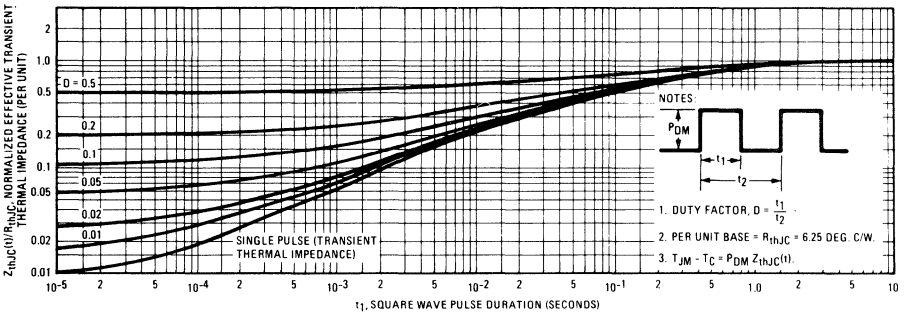


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRFF120, IRFF121, IRFF122, IRFF123

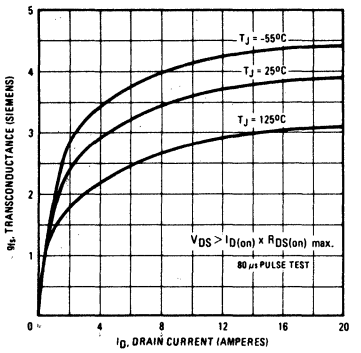


Fig. 6 – Typical Transconductance Vs. Drain Current

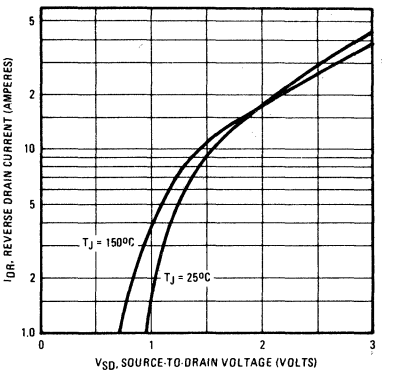


Fig. 7 – Typical Source-Drain Diode Forward Voltage

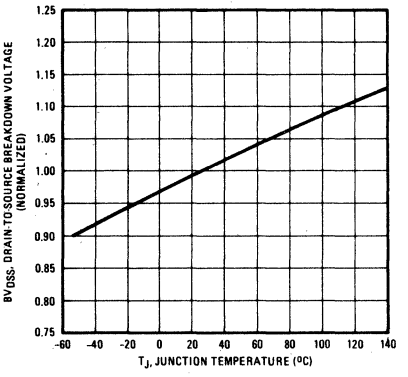


Fig. 8 – Breakdown Voltage Vs. Temperature

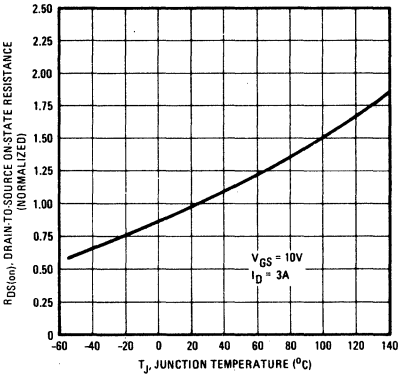


Fig. 9 – Normalized On-Resistance Vs. Temperature

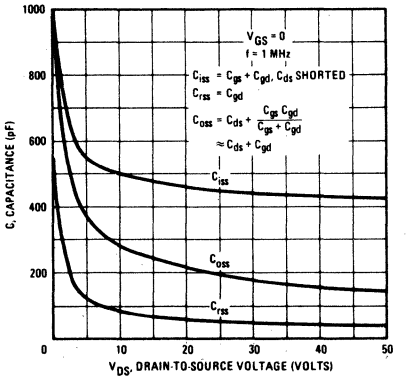


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

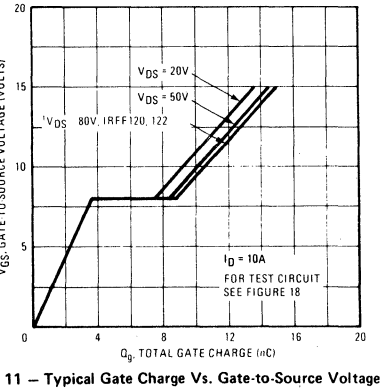


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

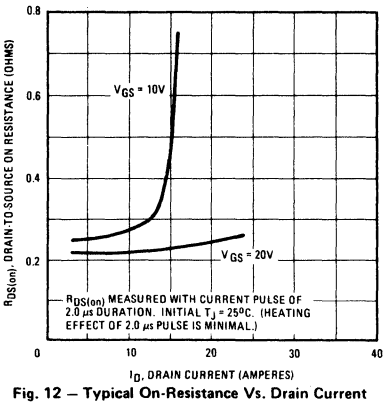


Fig. 12 – Typical On-Resistance Vs. Drain Current

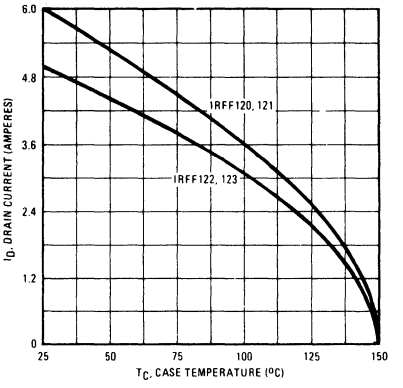


Fig. 13 – Maximum Drain Current Vs. Case Temperature

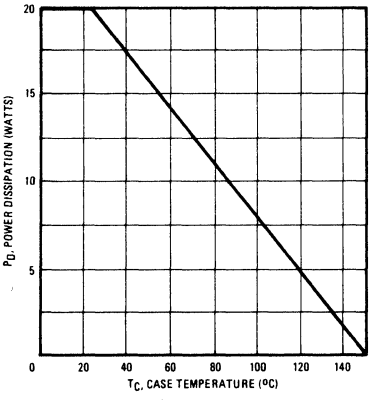


Fig. 14 – Power Vs. Temperature Derating Curve

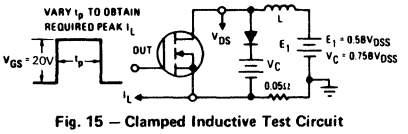


Fig. 15 – Clamped Inductive Test Circuit

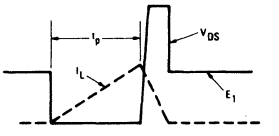


Fig. 16 – Clamped Inductive Waveforms

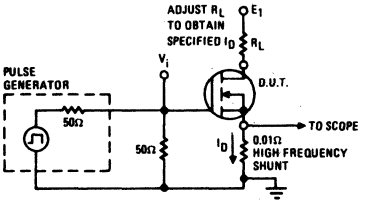


Fig. 17 – Switching Time Test Circuit

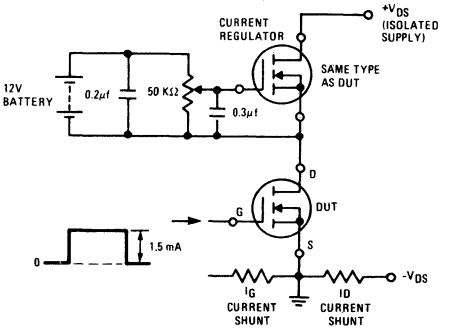


Fig. 18 – Gate Charge Test Circuit

IRFF130, IRFF131, IRFF132, IRFF133

File Number **1564**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

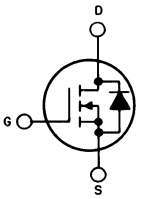
7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

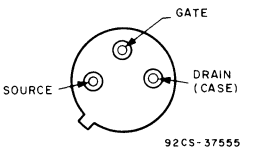
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

The IRFF130, IRFF131, IRFF132 and IRFF133 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF **(LOW-PROFILE TO-39)** metal package.

Absolute Maximum Ratings

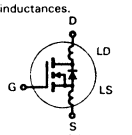
Parameter		IRFF130	IRFF131	IRFF132	IRFF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} - 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	25 (See Fig. 14)				W
	Linear Derating Factor	0.2 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRFF130, IRFF131, IRFF132, IRFF133

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFF130 IRFF132	100	–	–	V	V_{GS} = 0V
		IRFF131 IRFF133	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRFF130 IRFF131	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRFF132 IRFF133	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFF130 IRFF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 4.0A
		IRFF132 IRFF133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	50	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	80	150	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	80	150	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 5 mm (0.2 in.) from header to center of die.
L_S	Internal Source Inductance	ALL	–	15	–	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	ALL	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRFF130 IRFF131	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFF132 IRFF133	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRFF130 IRFF131	–	–	32	A	
		IRFF132 IRFF133	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRFF130 IRFF131	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRFF132 IRFF133	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.5	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRFF130, IRFF131, IRFF132, IRFF133

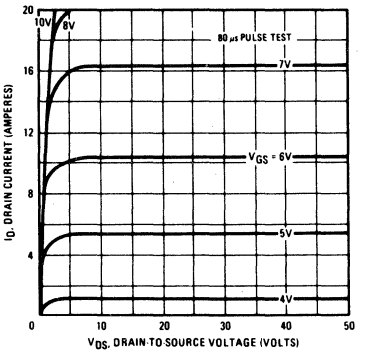


Fig. 1 – Typical Output Characteristics

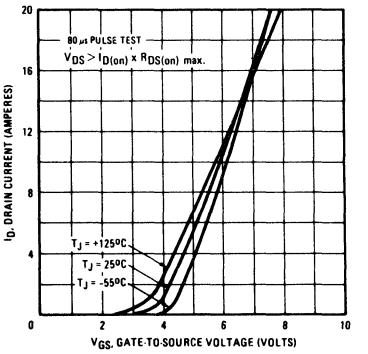


Fig. 2 – Typical Transfer Characteristics

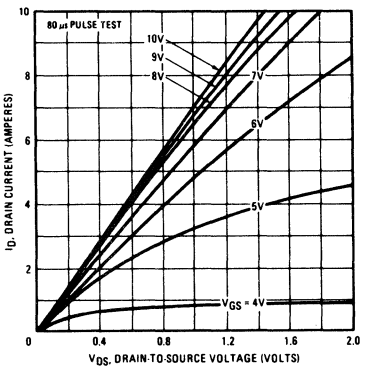


Fig. 3 – Typical Saturation Characteristics

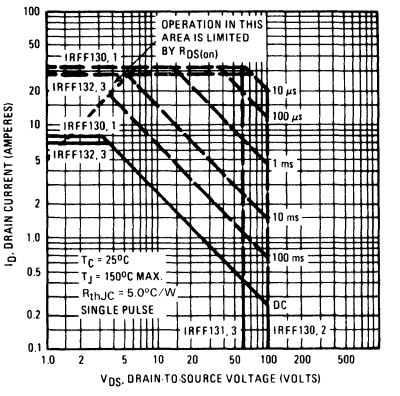


Fig. 4 – Maximum Safe Operating Area

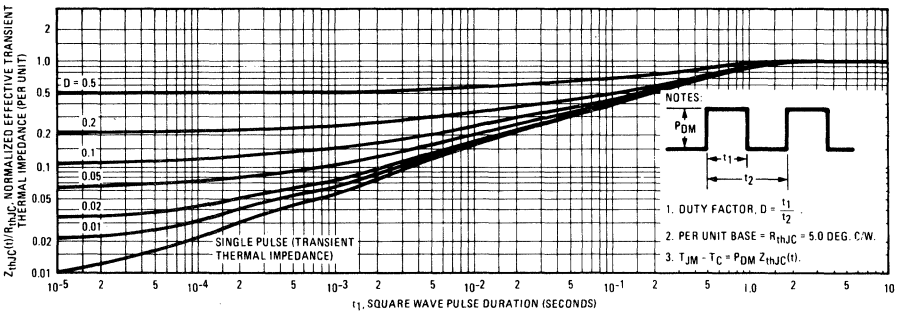


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

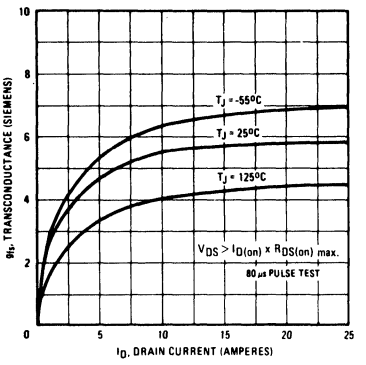


Fig. 6 – Typical Transconductance Vs. Drain Current

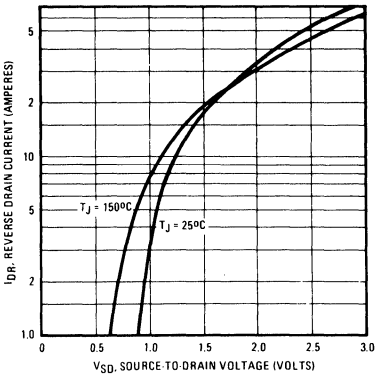


Fig. 7 – Typical Source-Drain Diode Forward Voltage

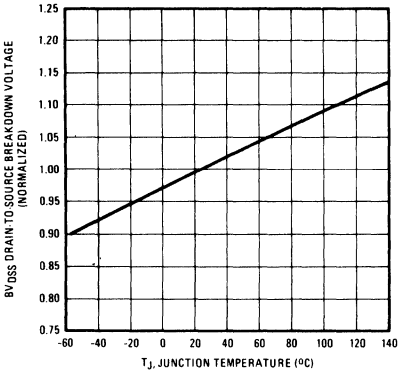


Fig. 8 – Breakdown Voltage Vs. Temperature

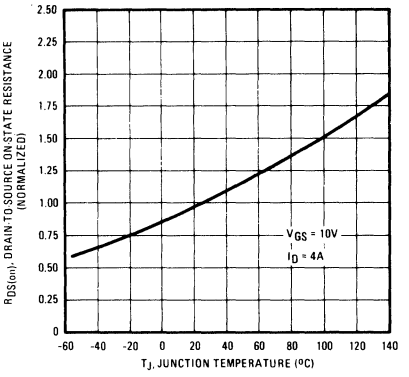


Fig. 9 – Normalized On-Resistance Vs. Temperature

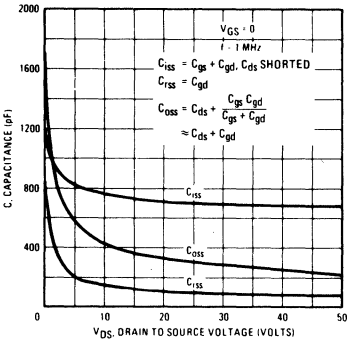


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

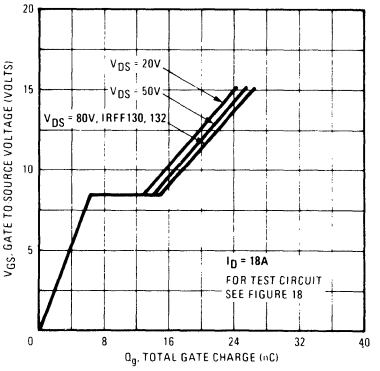


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRFF130, IRFF131, IRFF132, IRFF133

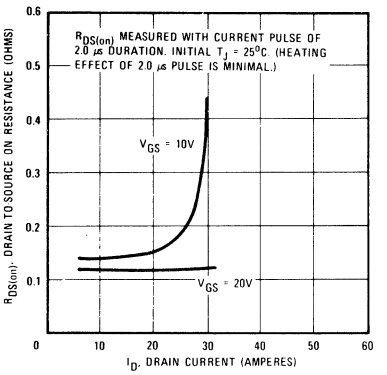


Fig. 12 – Typical On-Resistance Vs. Drain Current

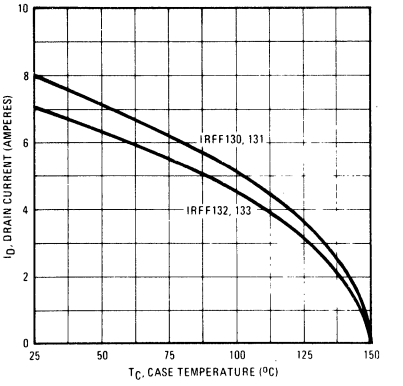


Fig. 13 – Maximum Drain Current Vs. Case Temperature

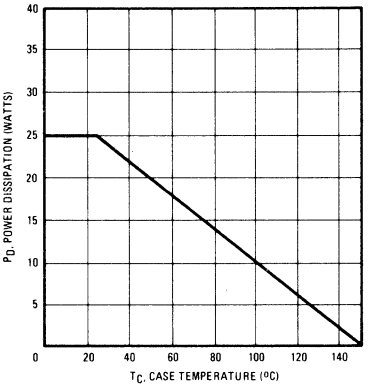


Fig. 14 – Power Vs. Temperature Derating Curve

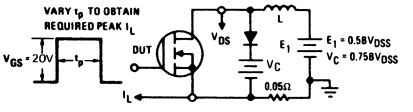


Fig. 15 – Clamped Inductive Test Circuit

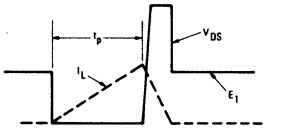


Fig. 16 – Clamped Inductive Waveforms

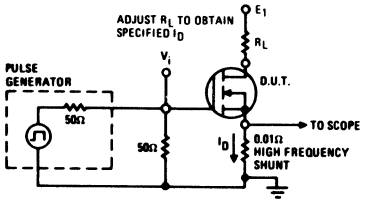


Fig. 17 – Switching Time Test Circuit

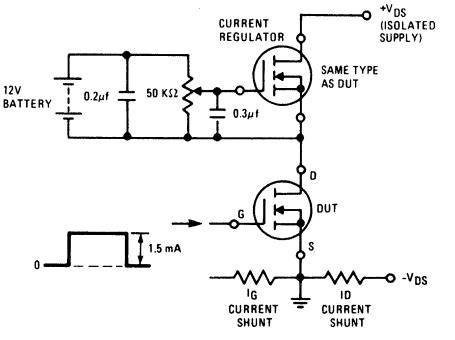


Fig. 18 – Gate Charge Test Circuit

File Number **1565**

IRF120, IRF121, IRF122, IRF123

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

7.0A and 8.0A, 60V-100V

$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

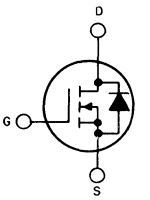
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF120, IRF121, IRF122 and IRF123 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

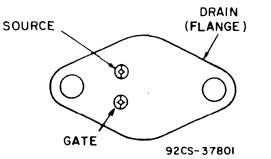
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

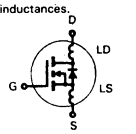
Parameter		IRF120	IRF121	IRF122	IRF123	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF120, IRF121, IRF122, IRF123

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF120 IRF122	100	–	–	V	V_{GS} = 0V
		IRF121 IRF123	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF120 IRF121	8.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF122 IRF123	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF120 IRF121	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF122 IRF123	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 10V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF120 IRF121	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF122 IRF123	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF120 IRF121	–	–	32	A	
		IRF122 IRF123	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF120 IRF121	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF122 IRF123	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

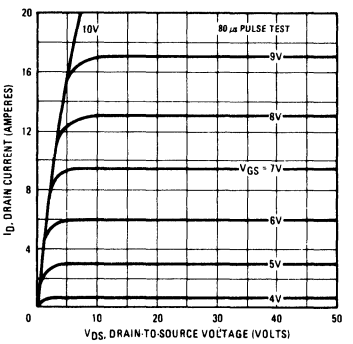


Fig. 1 – Typical Output Characteristics

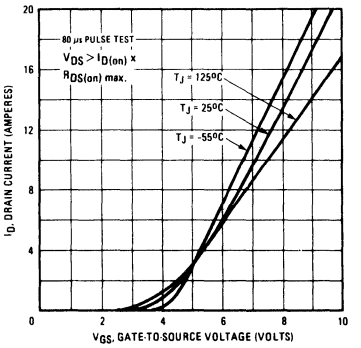


Fig. 2 – Typical Transfer Characteristics

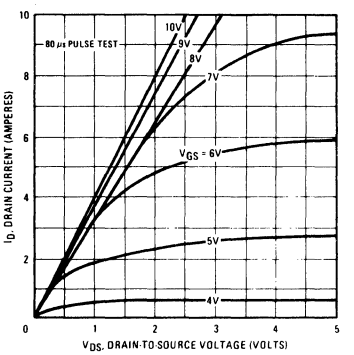


Fig. 3 – Typical Saturation Characteristics

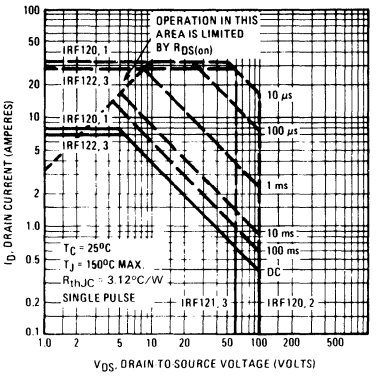


Fig. 4 – Maximum Safe Operating Area

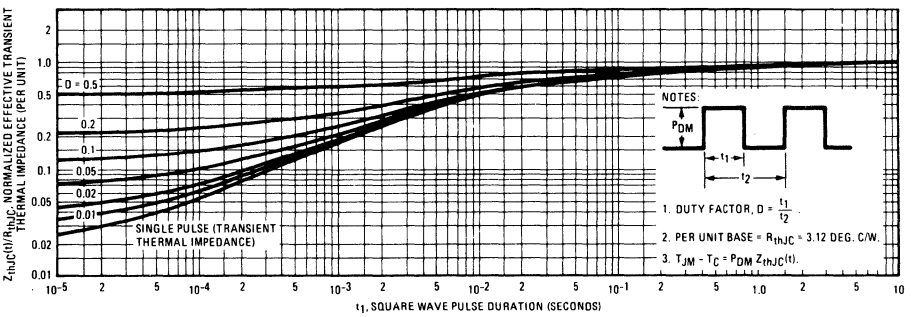


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

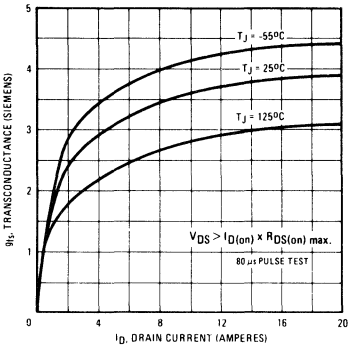


Fig. 6 – Typical Transconductance Vs. Drain Current

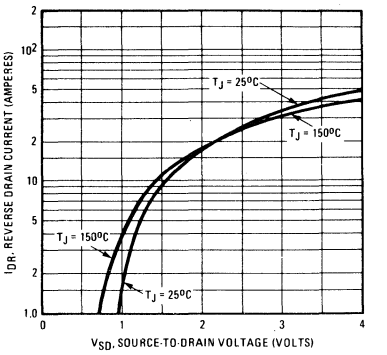


Fig. 7 – Typical Source-Drain Diode Forward Voltage

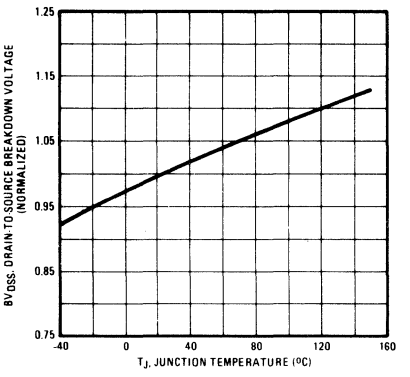


Fig. 8 – Breakdown Voltage Vs. Temperature

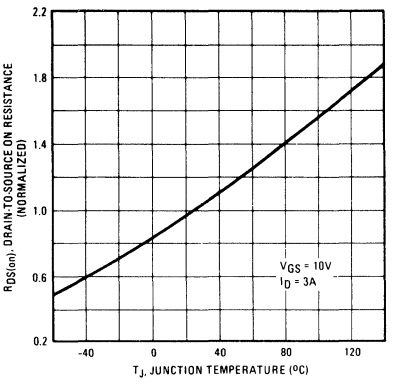


Fig. 9 – Normalized On-Resistance Vs. Temperature

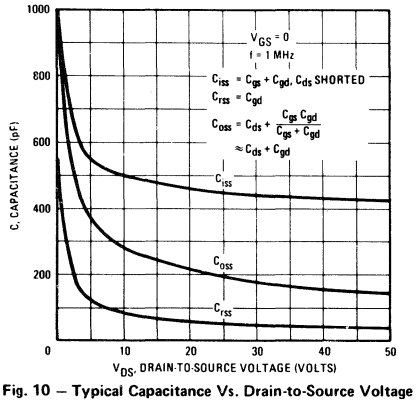


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

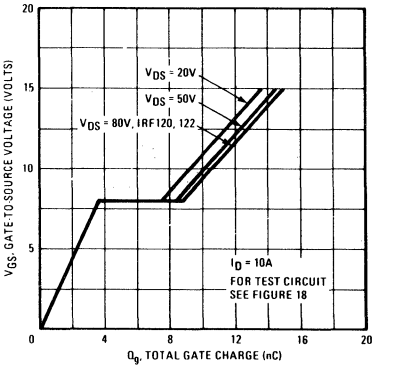


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

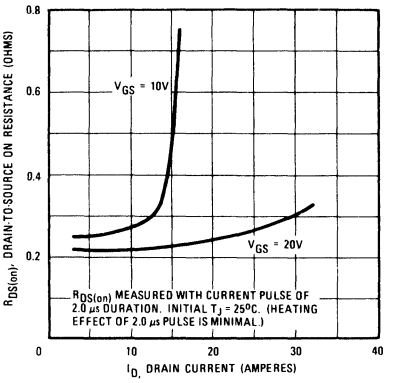


Fig. 12 – Typical On-Resistance Vs. Drain Current

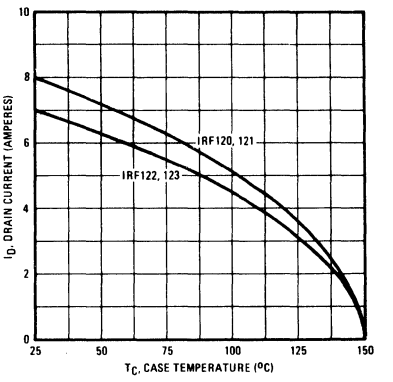


Fig. 13 – Maximum Drain Current Vs. Case Temperature

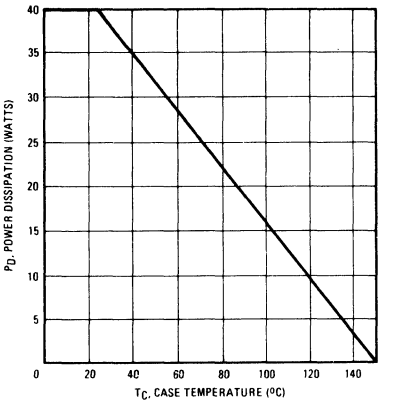


Fig. 14 – Power Vs. Temperature Derating Curve

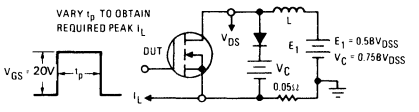


Fig. 15 – Clamped Inductive Test Circuit

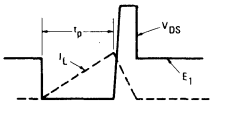


Fig. 16 – Clamped Inductive Waveforms

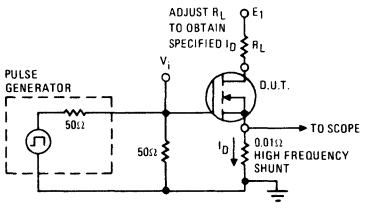


Fig. 17 – Switching Time Test Circuit

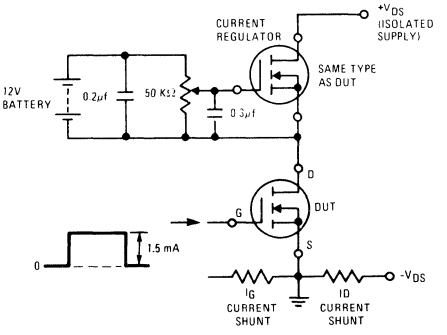


Fig. 18 – Gate Charge Test Circuit

IRF130, IRF131, IRF132, IRF133

File Number **1566**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

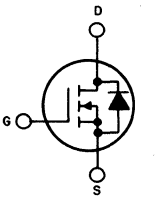
12A and 14A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

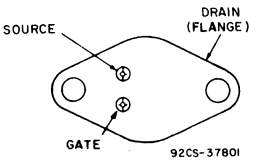
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

The IRF130, IRF131, IRF132 and IRF133 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

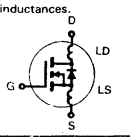
Absolute Maximum Ratings

	Parameter	IRF130	IRF131	IRF132	IRF133	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		56	56	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF130 IRF132	100	–	–	V	V_{GS} = 0V
		IRF131 IRF133	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF130 IRF131	14	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF132 IRF133	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF130 IRF131	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF132 IRF133	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17
t_r	Rise Time	ALL	–	–	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f	Fall Time	ALL	–	–	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF130 IRF131	–	–	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF132 IRF133	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF130 IRF131	–	–	56	A	
		IRF132 IRF133	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF130 IRF131	–	–	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF132 IRF133	–	–	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	360	–	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.1	–	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF130, IRF131, IRF132, IRF133

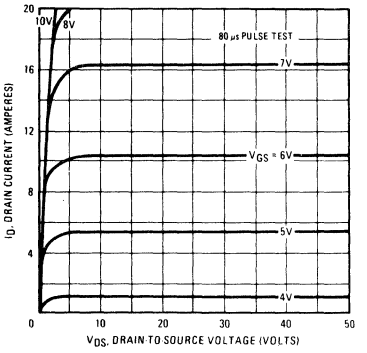


Fig. 1 – Typical Output Characteristics

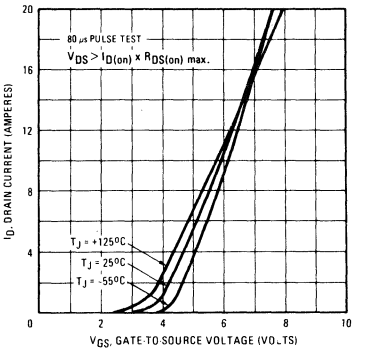


Fig. 2 – Typical Transfer Characteristics

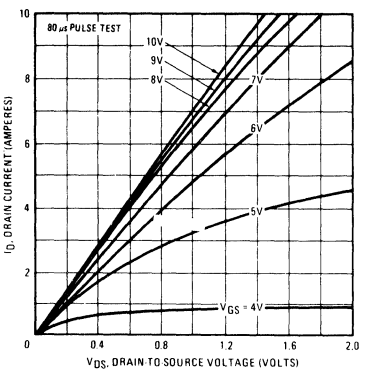


Fig. 3 – Typical Saturation Characteristics

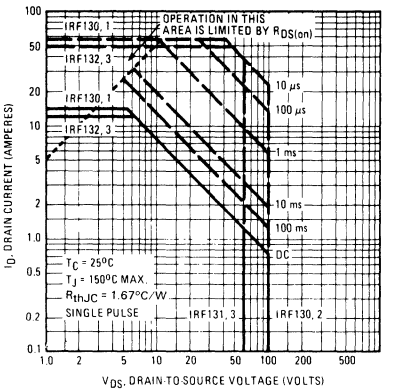


Fig. 4 – Maximum Safe Operating Area

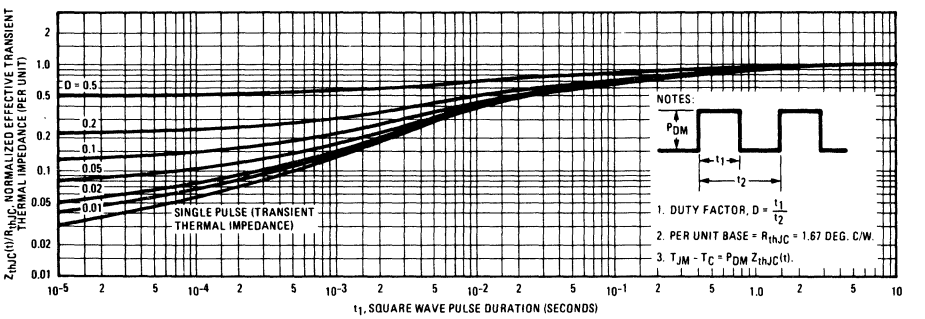


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

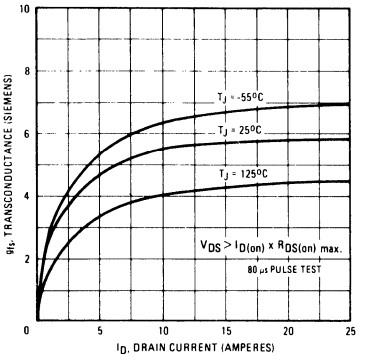


Fig. 6 – Typical Transconductance Vs. Drain Current

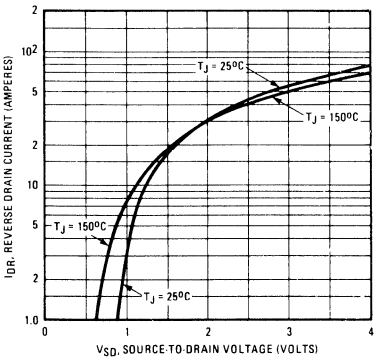


Fig. 7 – Typical Source-Drain Diode Forward Voltage

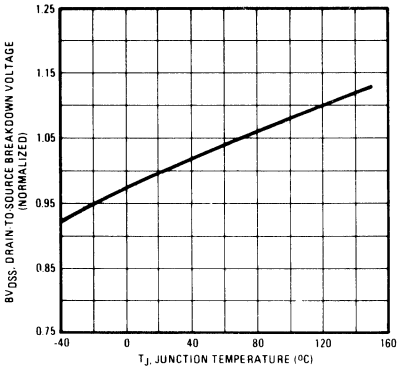


Fig. 8 – Breakdown Voltage Vs. Temperature

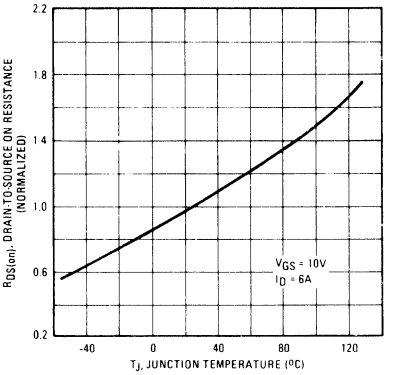


Fig. 9 – Normalized On-Resistance Vs. Temperature

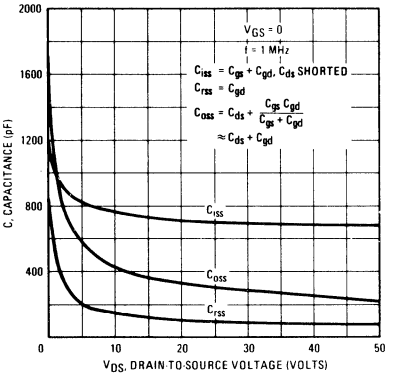


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

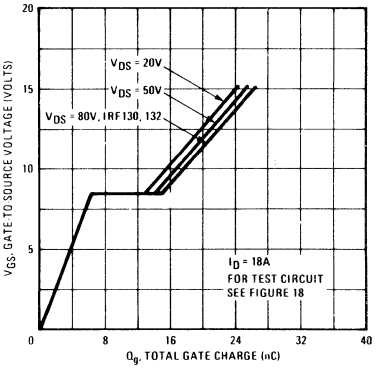


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF130, IRF131, IRF132, IRF133

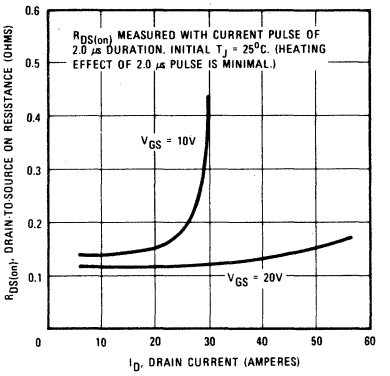


Fig. 12 – Typical On-Resistance Vs. Drain Current

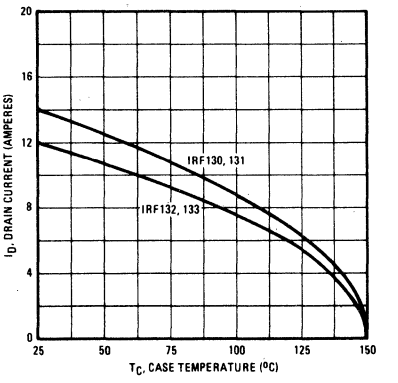


Fig. 13 – Maximum Drain Current Vs. Case Temperature

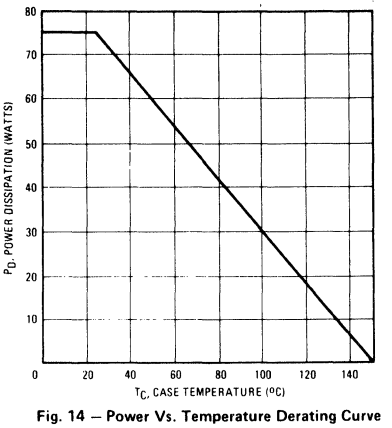


Fig. 14 – Power Vs. Temperature Derating Curve

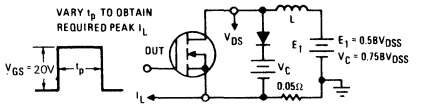


Fig. 15 – Clamped Inductive Test Circuit

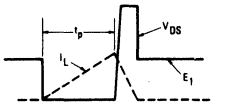


Fig. 16 – Clamped Inductive Waveforms

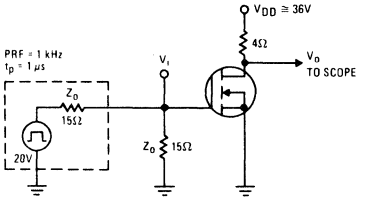


Fig. 17 – Switching Time Test Circuit

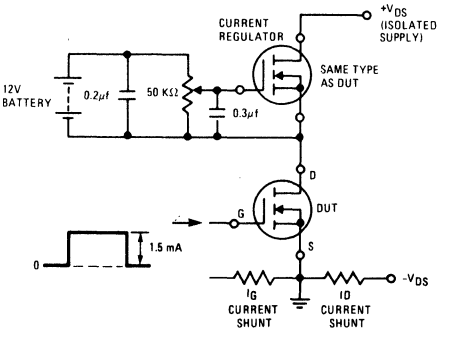


Fig. 18 – Gate Charge Test Circuit

File Number **1824**

IRF150, IRF151, IRF152, IRF153

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

33 A and 40 A, 60 V - 100 V
$r_{DS}(on)$ = 0.055 Ω and 0.08 Ω

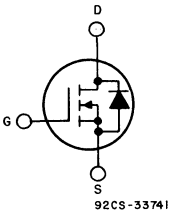
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF150, IRF151, IRF152 and IRF153 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

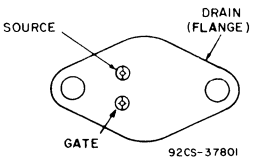
The IRF-types are supplied in the JEDEC TO-204AE metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AE

Absolute Maximum Ratings

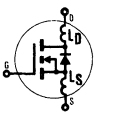
	Parameter	IRF150	IRF151	IRF152	IRF153	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	40	40	33	33	A
I_D @ T_C = 100°C	Continuous Drain Current	25	25	20	20	A
I_{DM}	Pulsed Drain Current ③	160	160	132	132	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		160	160	132	132	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF150, IRF151, IRF152, IRF153

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF150, IRF152	100	–	–	V	V_{GS} = 0V
		IRF151, IRF153	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF150, IRF151	40	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF152, IRF153	33	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF150, IRF151	–	0.045	0.055	Ω	V_{GS} = 10V, I_D = 20A
		IRF152, IRF153	–	0.06	0.08	Ω	
g_{fs}	Forward Transconductance ②	ALL	9.0	11	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 20A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	1000	1500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	350	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 24V, I_D = 20A, Z_o = 4.7Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	63	120	nC	V_{GS} = 10V, I_D = 50A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	27	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	36	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF150, IRF151	–	–	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF152, IRF153	–	–	33	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF150, IRF151	–	–	160	A	
		IRF152, IRF153	–	–	132	A	
V_{SD}	Diode Forward Voltage ②	IRF150, IRF151	–	–	2.5	V	T_C = 25°C, I_S = 40A, V_{GS} = 0V
		IRF152, IRF153	–	–	2.3	V	T_C = 25°C, I_S = 33A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.3	–	μC	T_J = 150°C, I_F = 40A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

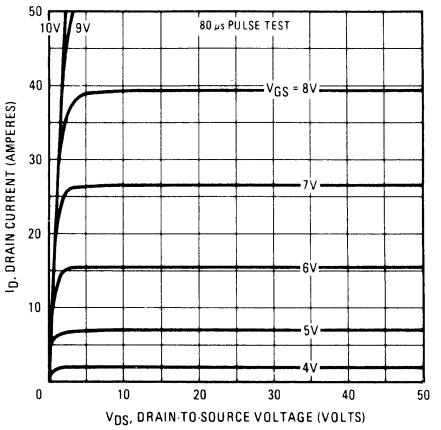


Fig. 1 — Typical Output Characteristics

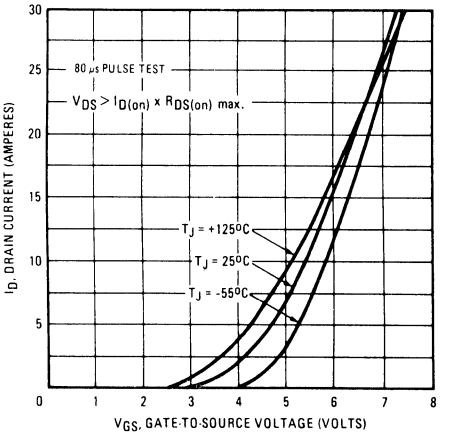


Fig. 2 — Typical Transfer Characteristics

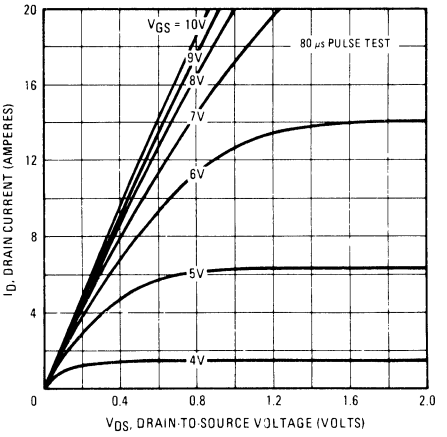


Fig. 3 — Typical Saturation Characteristics

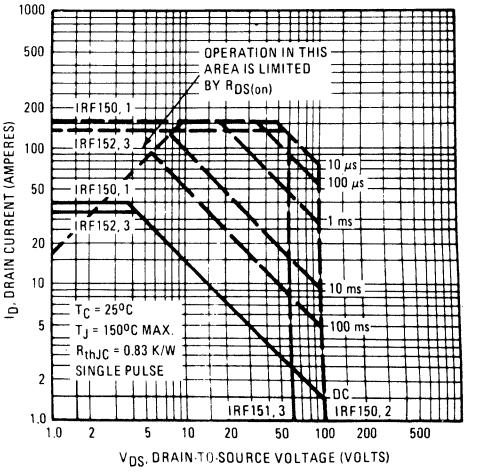


Fig. 4 — Maximum Safe Operating Area

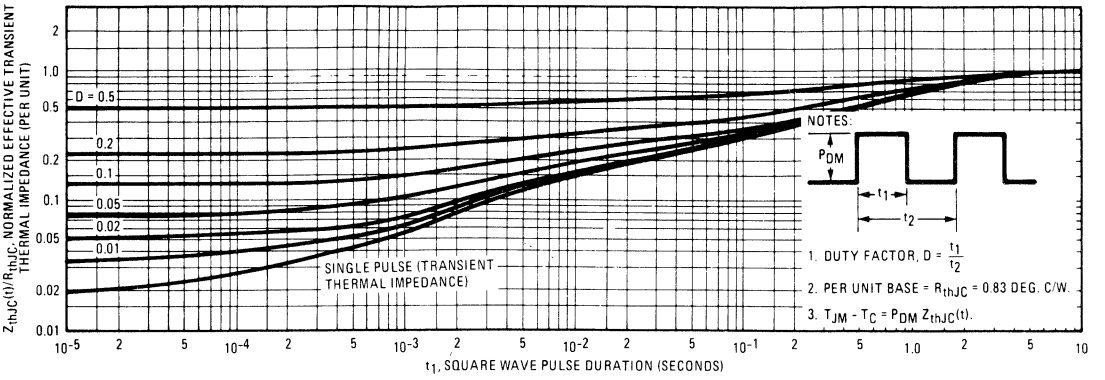


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF150, IRF151, IRF152, IRF153

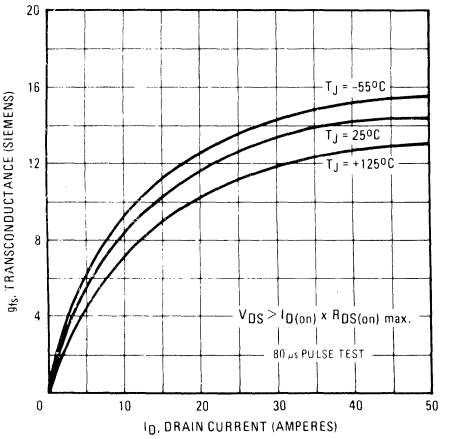


Fig. 6 — Typical Transconductance Vs. Drain Current

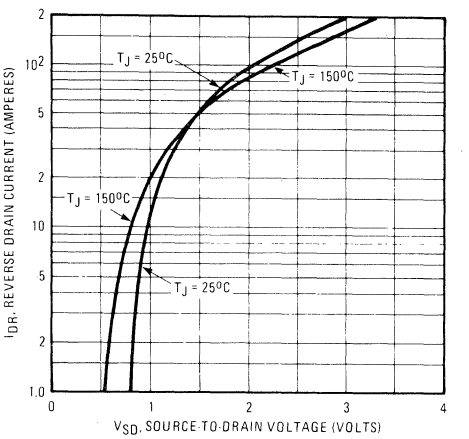


Fig. 7 — Typical Source-Drain Diode Forward Voltage

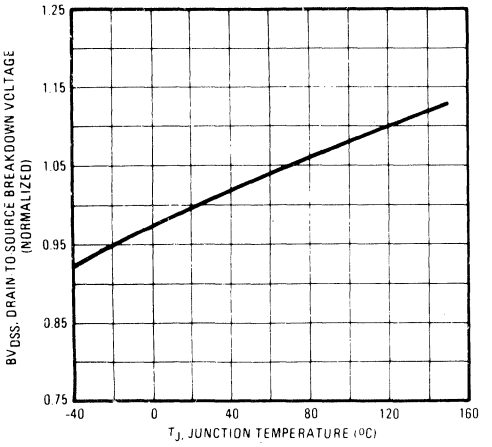


Fig. 8 — Breakdown Voltage Vs. Temperature

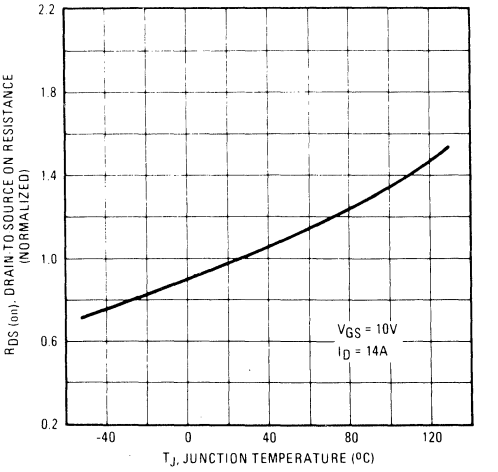


Fig. 9 — Normalized On-Resistance Vs. Temperature

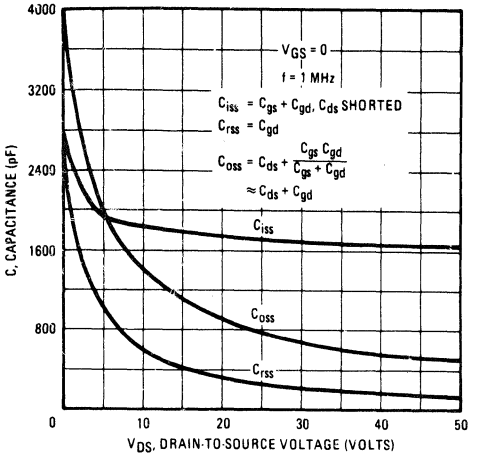


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

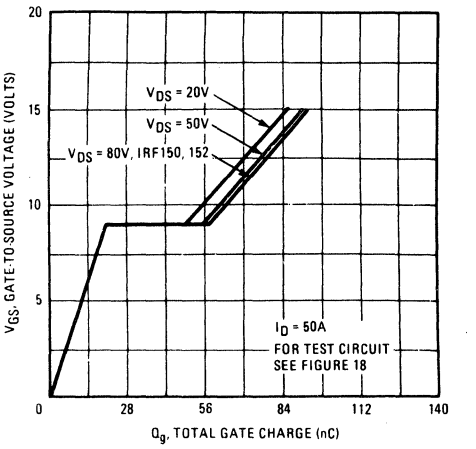


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

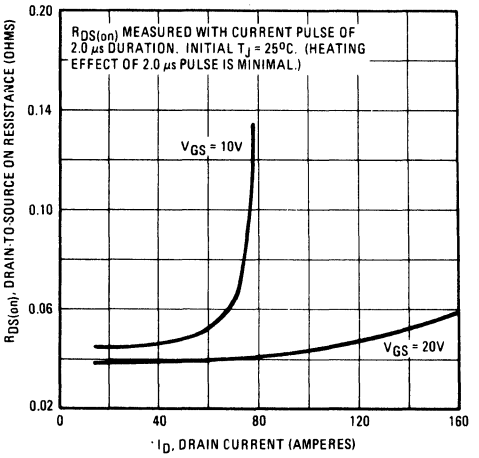


Fig. 12 – Typical On-Resistance Vs. Drain Current

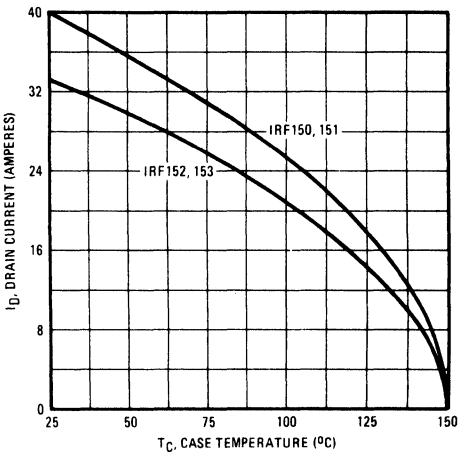


Fig. 13 – Maximum Drain Current Vs. Case Temperature

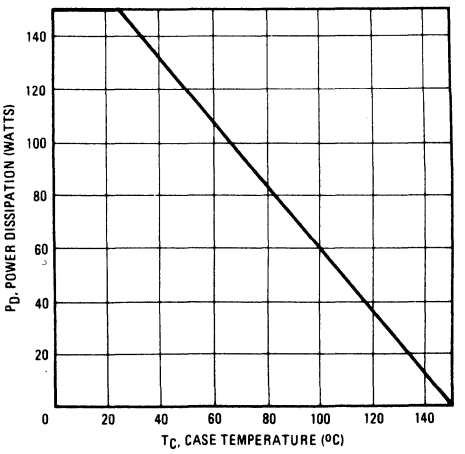


Fig. 14 – Power Vs. Temperature Derating Curve

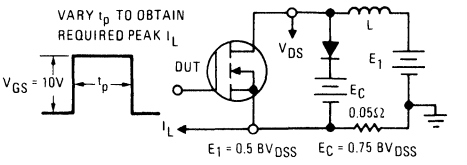


Fig. 15 – Clamped Inductive Test Circuit

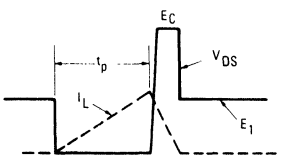


Fig. 16 – Clamped Inductive Waveforms

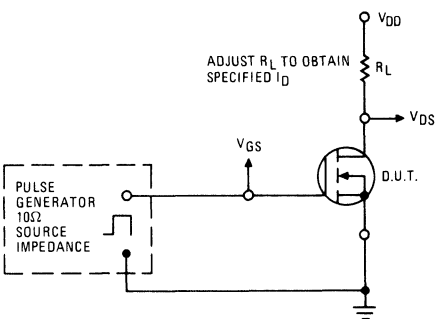


Fig. 17 – Switching Time Test Circuit

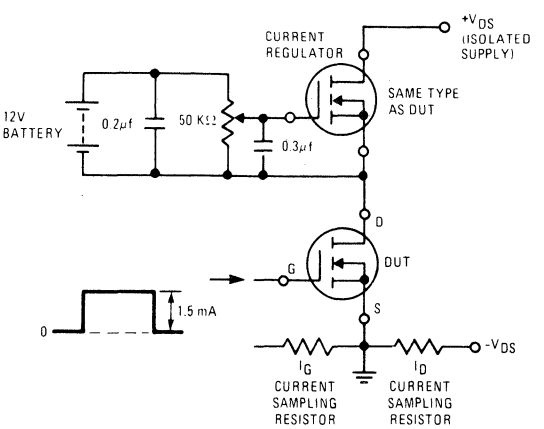


Fig. 18 – Gate Charge Test Circuit

IRF220, IRF221, IRF222, IRF223

File Number **1567**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

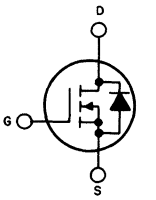
4.0A and 5.0A, 150V-200V

$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



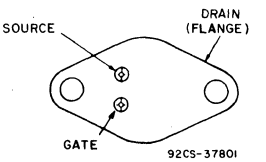
92CS-33741

TERMINAL DIAGRAM

The IRF220, IRF221, IRF222 and IRF223 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

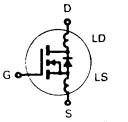
Absolute Maximum Ratings

Parameter		IRF220	IRF221	IRF222	IRF223	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		20	20	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-50 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF220 IRF222	200	–	–	V	V_{GS} = 0V
		IRF221 IRF223	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF220 IRF221	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF222 IRF223	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF220 IRF221	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF222 IRF223	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF220 IRF221	–		5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF222 IRF223	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF220 IRF221	–	–	20	A	
		IRF222 IRF223	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF220 IRF221	–	–	2.0	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF222 IRF223	–	–	1.8	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF220, IRF221, IRF222, IRF223

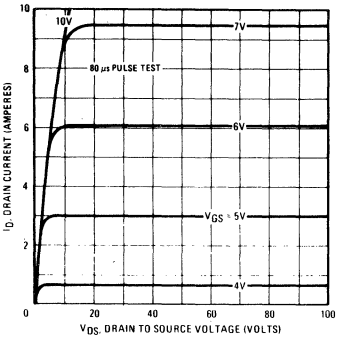


Fig. 1 — Typical Output Characteristics

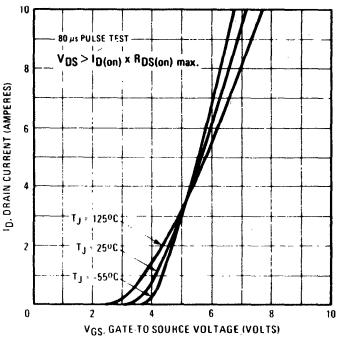


Fig. 2 — Typical Transfer Characteristics

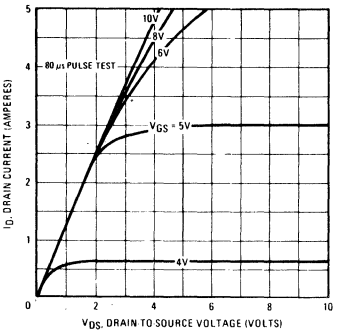


Fig. 3 — Typical Saturation Characteristics

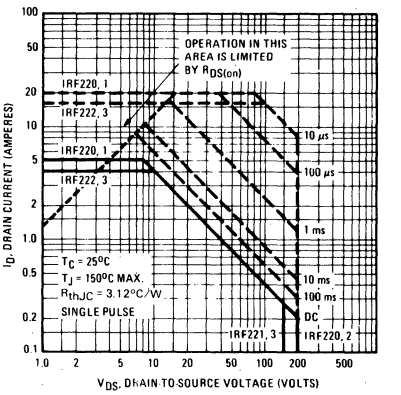


Fig. 4 — Maximum Safe Operating Area

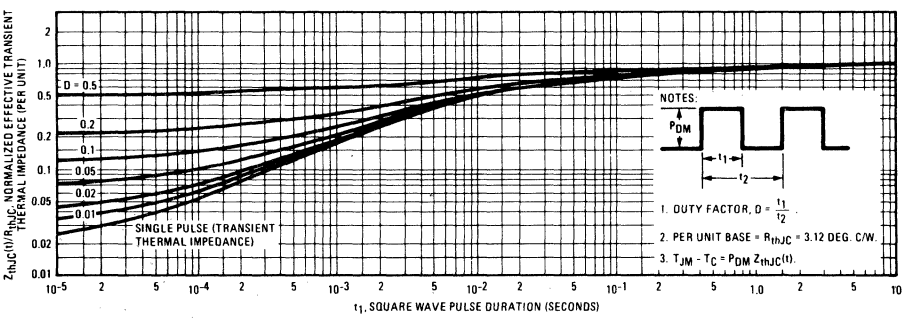


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

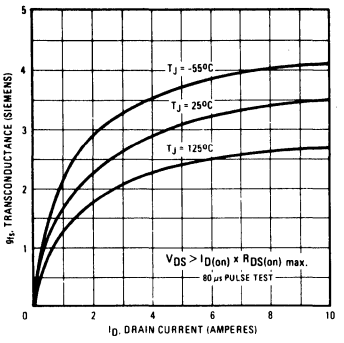


Fig. 6 — Typical Transconductance Vs. Drain Current

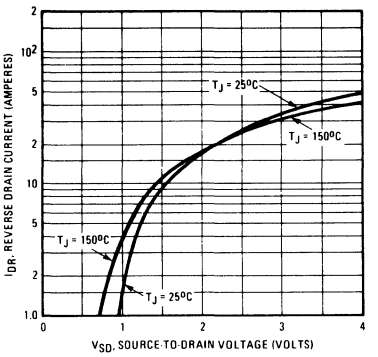


Fig. 7 — Typical Source-Drain Diode Forward Voltage

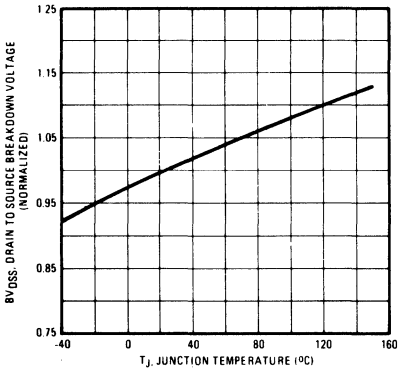


Fig. 8 — Breakdown Voltage Vs. Temperature

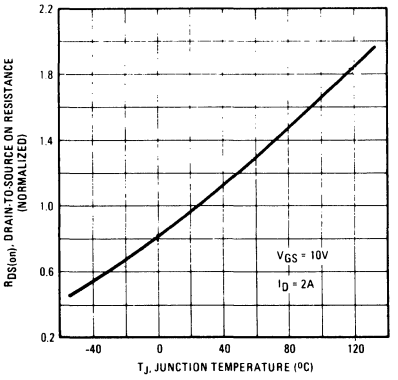


Fig. 9 — Normalized On-Resistance Vs. Temperature

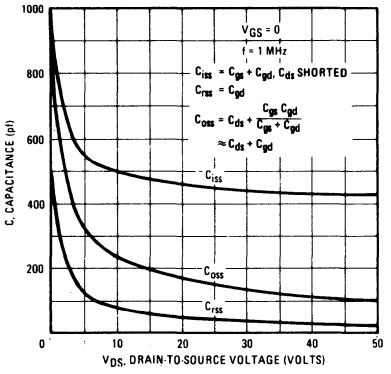


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

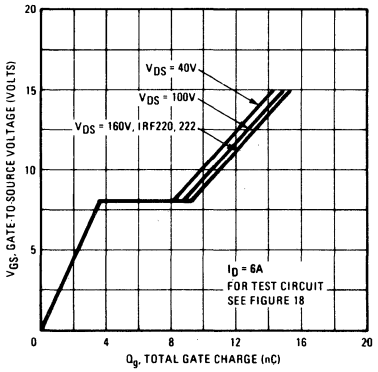


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF220, IRF221, IRF222, IRF223

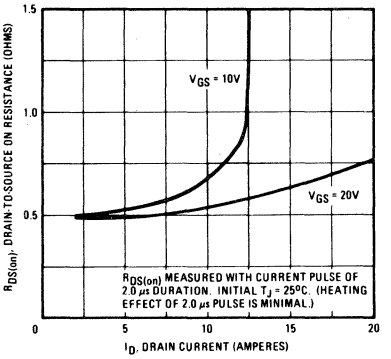


Fig. 12 – Typical On-Resistance Vs. Drain Current

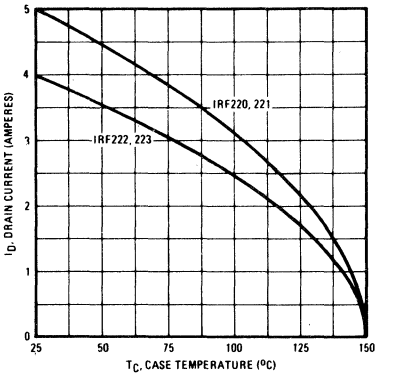


Fig. 13 – Maximum Drain Current Vs. Case Temperature

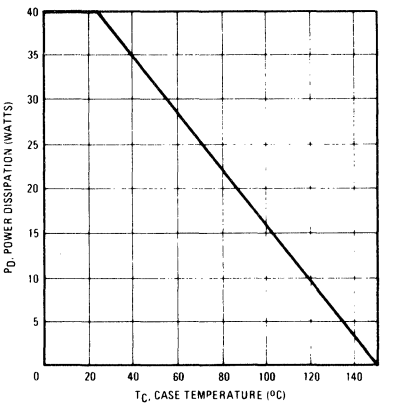


Fig. 14 – Power Vs. Temperature Derating Curve

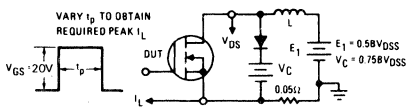


Fig. 15 – Clamped Inductive Test Circuit

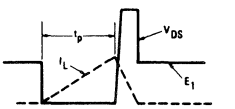


Fig. 16 – Clamped Inductive Waveforms

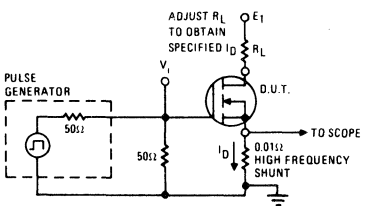


Fig. 17 – Switching Time Test Circuit

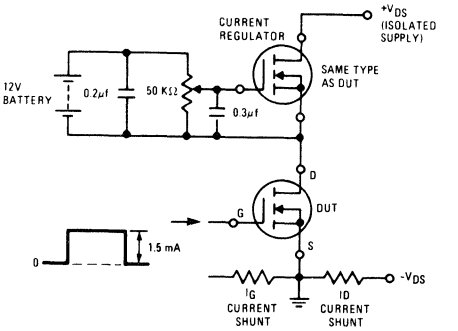


Fig. 18 – Gate Charge Test Circuit

File Number **1568**

IRF230, IRF231, IRF232, IRF233

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

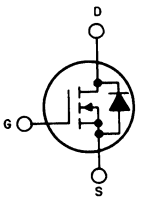
8.0A and 9.0A, 150V-200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

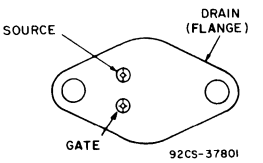
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

The IRF230, IRF231, IRF232 and IRF233 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

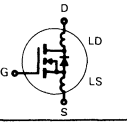
Parameter		IRF230	IRF231	IRF232	IRF233	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		36	36	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF230, IRF231, IRF232, IRF233

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF230 IRF232	200	–	–	V	V_{GS} = 0V
		IRF231 IRF233	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF230 IRF231	9.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF232 IRF233	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF230 IRF231	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF232 IRF233	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF230 IRF231	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF232 IRF233	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF230 IRF231	–	–	36	A	
		IRF232 IRF233	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF230 IRF231	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF232 IRF233	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Modified MOSFET symbol showing the integral reverse P-N junction rectifier.

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

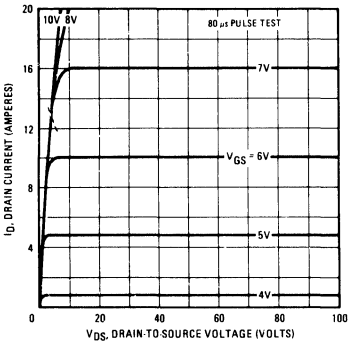


Fig. 1 – Typical Output Characteristics

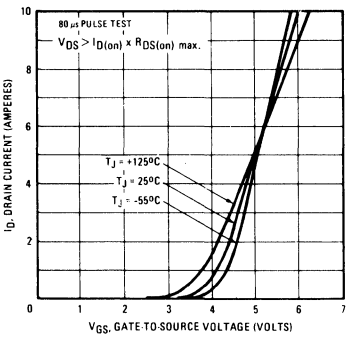


Fig. 2 – Typical Transfer Characteristics

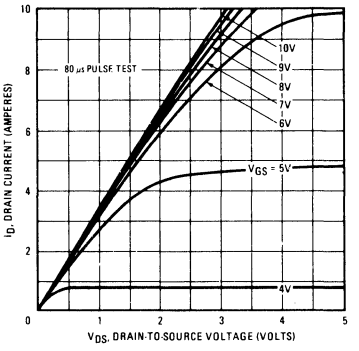


Fig. 3 – Typical Saturation Characteristics

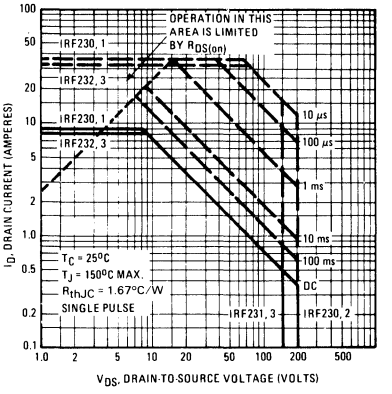


Fig. 4 – Maximum Safe Operating Area

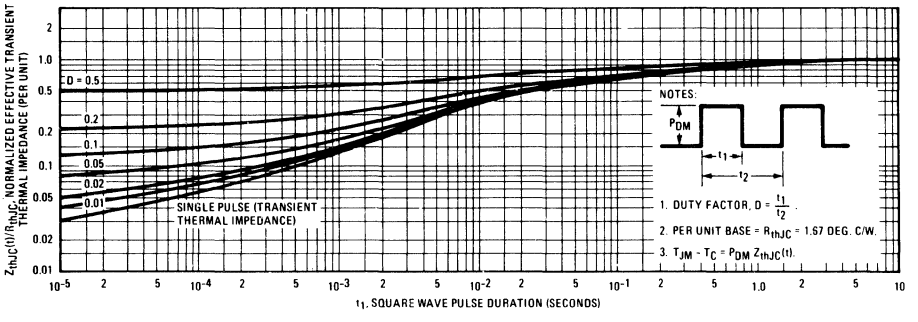


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF230, IRF231, IRF232, IRF233

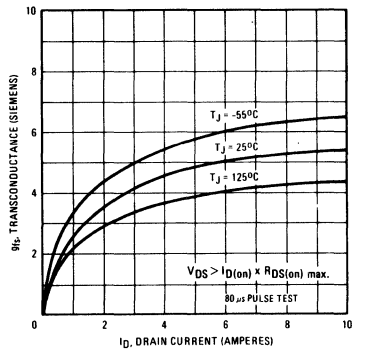


Fig. 6 – Typical Transconductance Vs. Drain Current

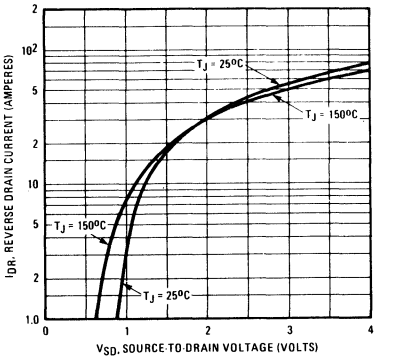


Fig. 7 – Typical Source-Drain Diode Forward Voltage

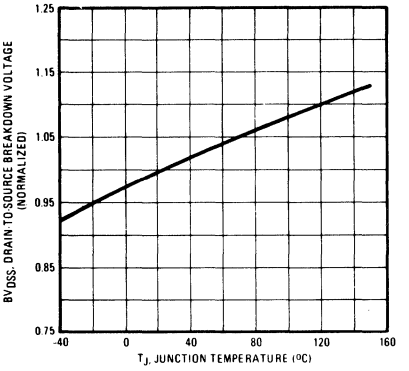


Fig. 8 – Breakdown Voltage Vs. Temperature

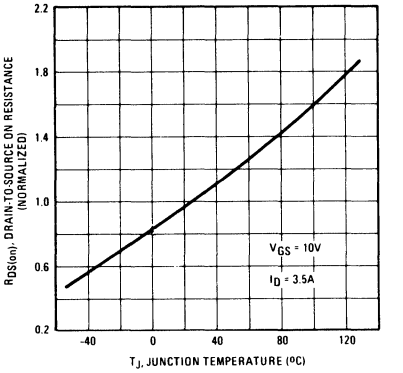


Fig. 9 – Normalized On-Resistance Vs. Temperature

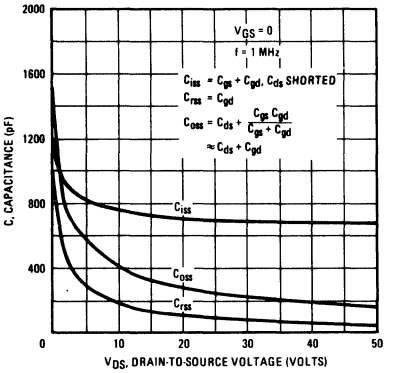


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

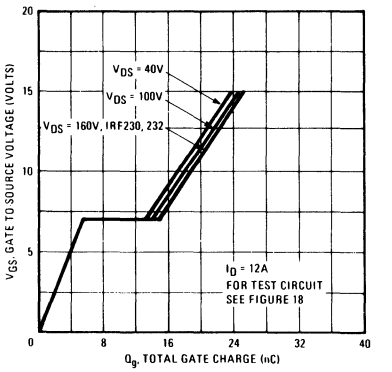


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

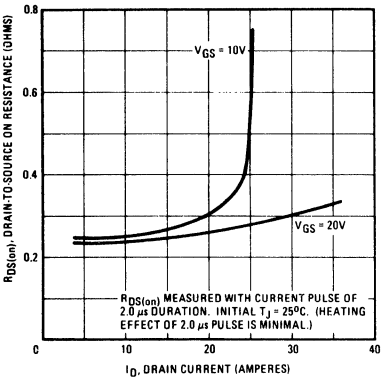


Fig. 12 – Typical On-Resistance Vs. Drain Current

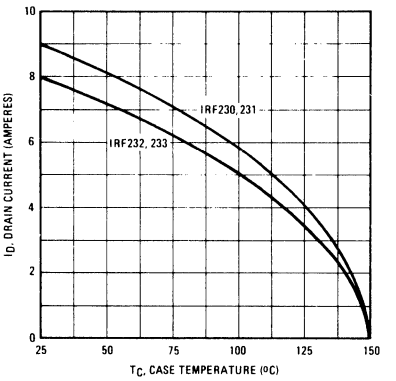


Fig. 13 – Maximum Drain Current Vs. Case Temperature

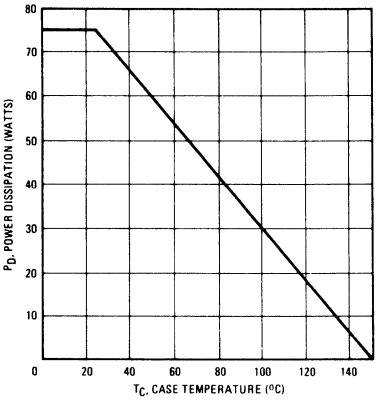


Fig. 14 – Power Vs. Temperature Derating Curve

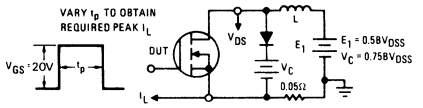


Fig. 15 – Clamped Inductive Test Circuit

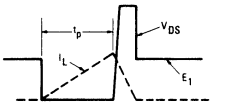


Fig. 16 – Clamped Inductive Waveforms

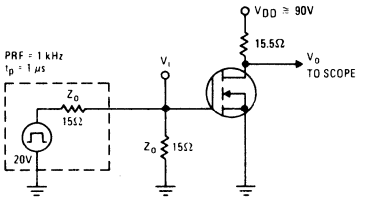


Fig. 17 – Switching Time Test Circuit

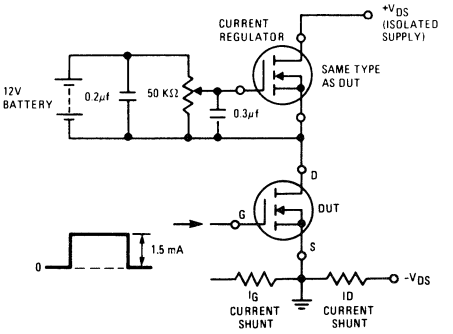


Fig. 18 – Gate Charge Test Circuit

IRF241, IRF243

File Number **1584**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

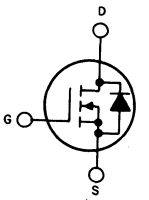
16A and 18A, 150V

$r_{DS}(on)$ = 0.18 Ω and 0.22 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

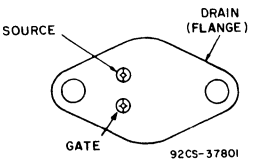
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

The IRF241 and IRF243 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE steel package.

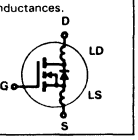
Absolute Maximum Ratings

	Parameter	IRF241	IRF243	Units
V_{DS}	Drain - Source Voltage ①	150	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	150	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	10	A
I_{DM}	Pulsed Drain Current ③	72	64	A
V_{GS}	Gate - Source Voltage	±20		V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)		W
	Linear Derating Factor	1.0 (See Fig. 14)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH		A
		72 | 72	64 | 64	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF241 IRF243	150	–	–	V	V_{GS} = 0V I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF241	18	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF243	16	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF241	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRF243	–	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	9.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} ≈ 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	40	80	ns	
t_f	Fall Time	ALL	–	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	16	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

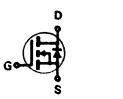


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF241	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF243	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF241	–	–	72	A	
		IRF243	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	IRF241	–	–	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRF243	–	–	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

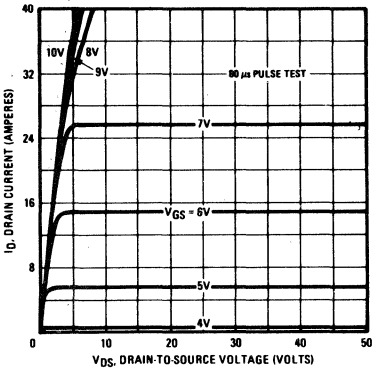


Fig. 1 – Typical Output Characteristics

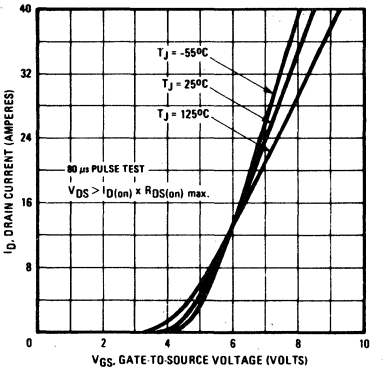


Fig. 2 – Typical Transfer Characteristics

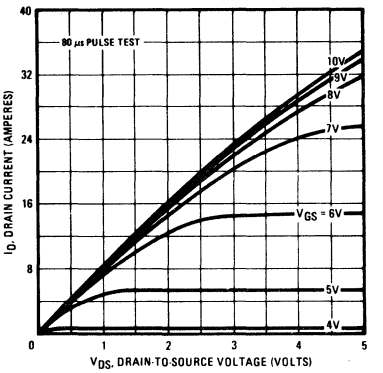


Fig. 3 – Typical Saturation Characteristics

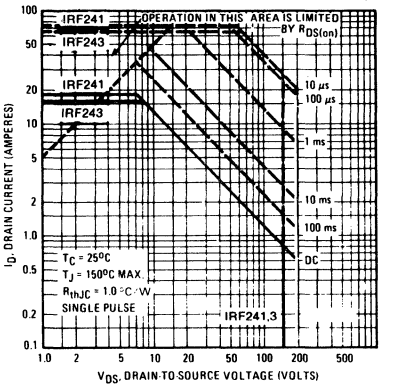


Fig. 4 – Maximum Safe Operating Area

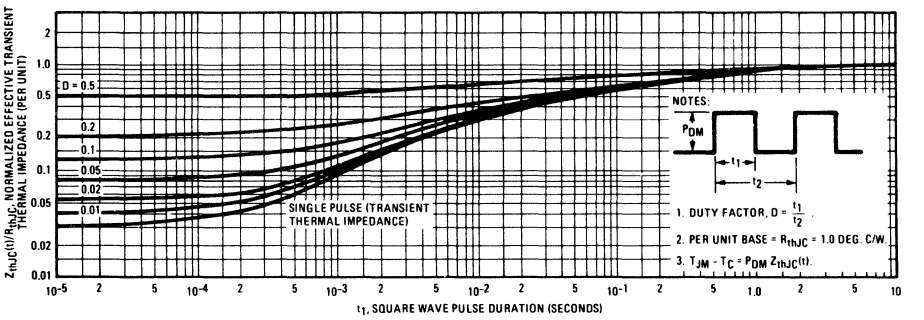


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

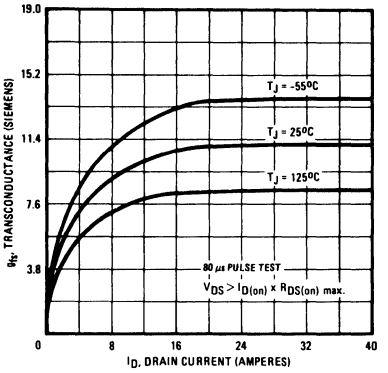


Fig. 6 – Typical Transconductance Vs. Drain Current

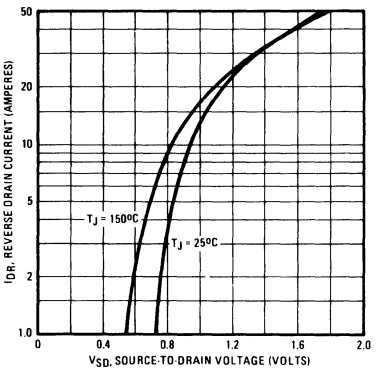


Fig. 7 – Typical Source-Drain Diode Forward Voltage

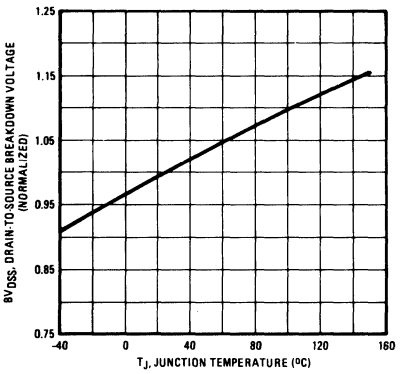


Fig. 8 – Breakdown Voltage Vs. Temperature

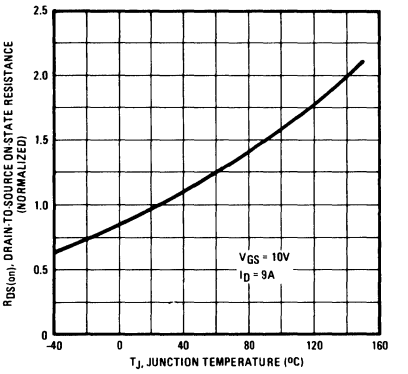


Fig. 9 – Normalized On-Resistance Vs. Temperature

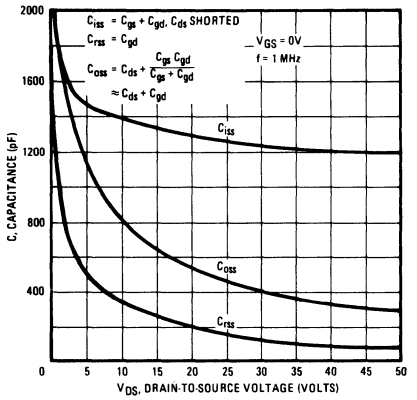


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

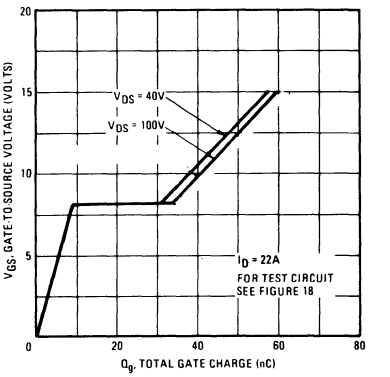


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

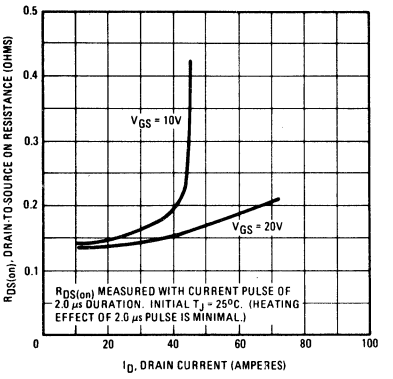


Fig. 12 – Typical On-Resistance Vs. Drain Current

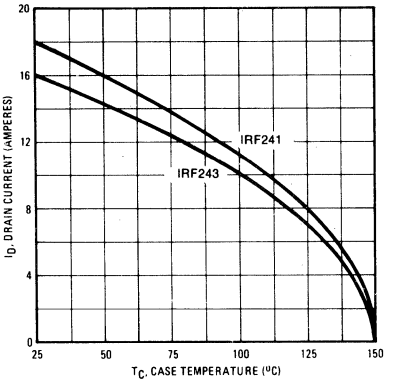


Fig. 13 – Maximum Drain Current Vs. Case Temperature

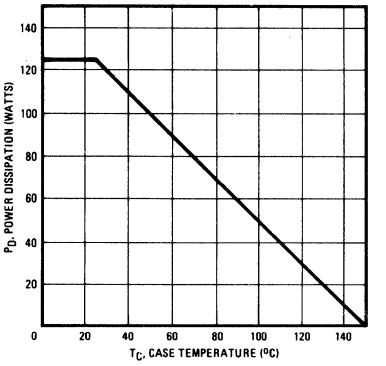


Fig. 14 – Power Vs. Temperature Derating Curve

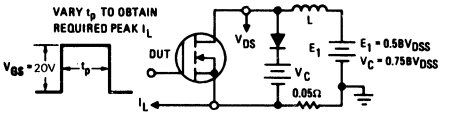


Fig. 15 – Clamped Inductive Test Circuit

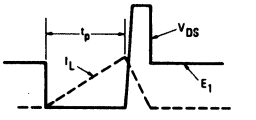


Fig. 16 – Clamped Inductive Waveforms

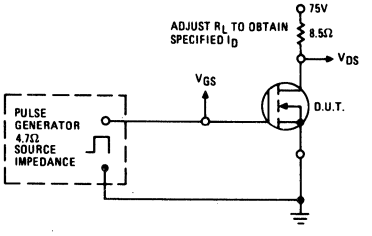


Fig. 17 – Switching Time Test Circuit

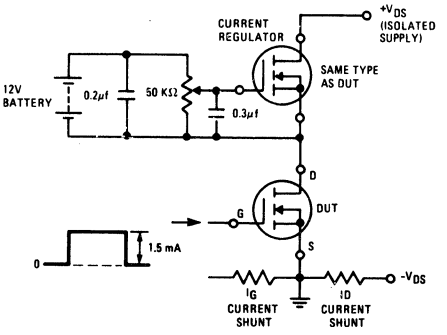


Fig. 18 – Gate Charge Test Circuit

File Number **1825**

IRF250, IRF251, IRF252, IRF253

Power MOS Field-Effect Transistors

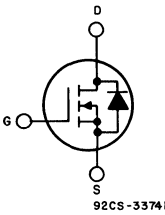
N-Channel Enhancement-Mode Power Field-Effect Transistors

25 A and 30 A, 150 V - 200 V
$r_{DS}(on)$ = 0.085 Ω and 0.120 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

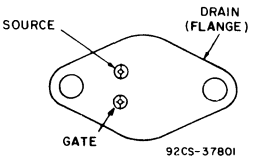


TERMINAL DIAGRAM

The IRF250, IRF251, IRF252 and IRF253 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

TERMINAL DESIGNATION



JEDEC TO-204AE

Absolute Maximum Ratings

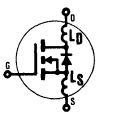
	Parameter	IRF250	IRF251	IRF252	IRF253	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	30	30	25	25	A
I_D @ T_C = 100°C	Continuous Drain Current	19	19	16	16	A
I_{DM}	Pulsed Drain Current ③	120	120	100	100	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM} ④	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		120	120	100	100	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF250, IRF251, IRF252, IRF253

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF250 IRF252	200	–	–	V	V_{GS} = 0V
		IRF251 IRF253	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF250 IRF251	30	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, V_{GS} = 10V
		IRF252 IRF253	25	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF250 IRF251	–	0.07	0.085	Ω	V_{GS} = 10V, I_D = 16A
		IRF252 IRF253	–	0.09	0.120	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	14	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\ max.}$, I_D = 16A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	800	1200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	300	500	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 95V, I_D = 16A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125	ns	
t_f	Fall Time	ALL	–	–	100	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 38A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	37	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF250 IRF251	–	–	30	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF252 IRF253	–	–	25	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF250 IRF251	–	–	120	A	
		IRF252 IRF253	–	–	100	A	
V_{SD}	Diode Forward Voltage ②	IRF250 IRF251	–	–	2.0	V	T_C = 25°C, I_S = 30A, V_{GS} = 0V
		IRF252 IRF253	–	–	1.8	V	T_C = 25°C, I_S = 25A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	750	–	ns	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.7	–	μC	T_J = 150°C, I_F = 30A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

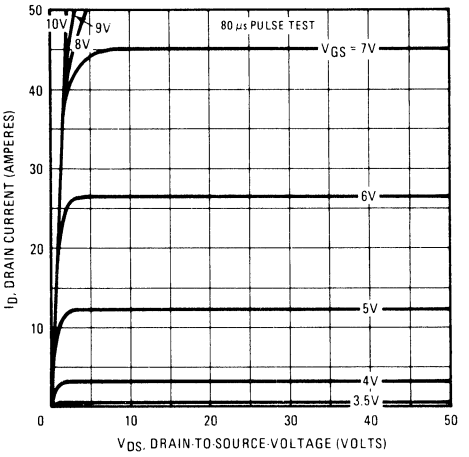


Fig. 1 — Typical Output Characteristics

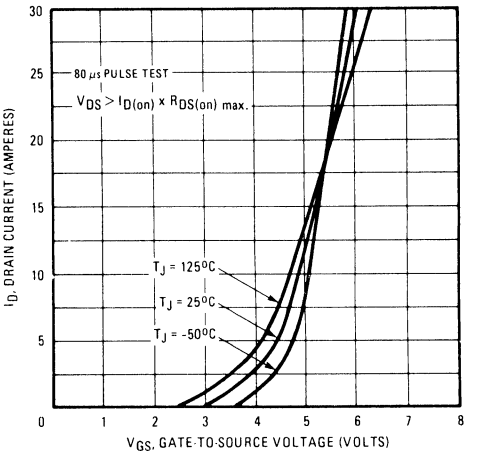


Fig. 2 — Typical Transfer Characteristics

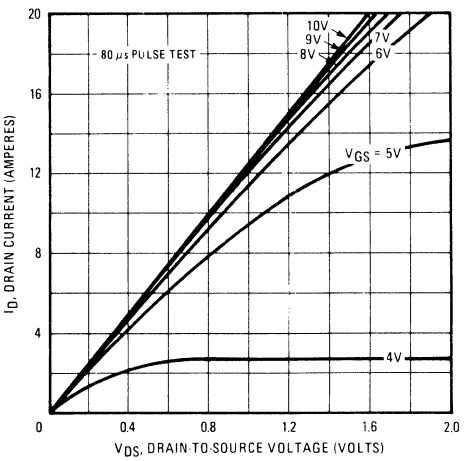


Fig. 3 — Typical Saturation Characteristics

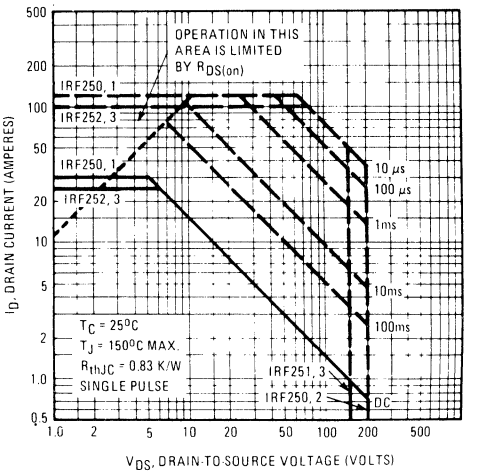


Fig. 4 — Maximum Safe Operating Area

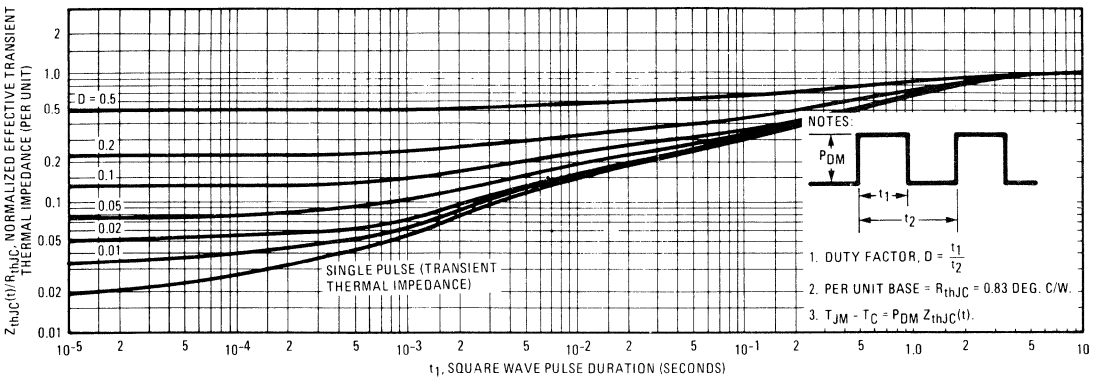


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF250, IRF251, IRF252, IRF253

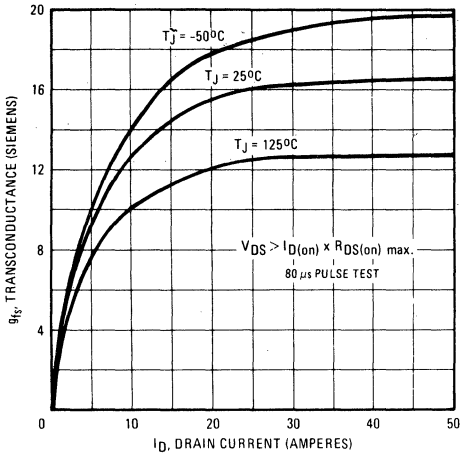


Fig. 6 – Typical Transconductance Vs. Drain Current

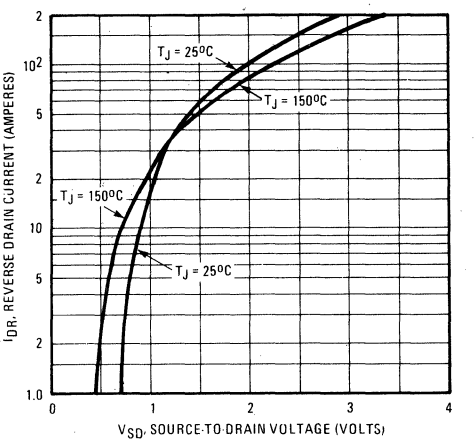


Fig. 7 – Typical Source-Drain Diode Forward Voltage

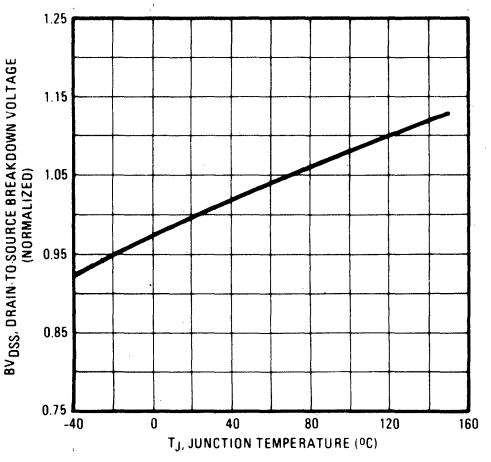


Fig. 8 – Breakdown Voltage Vs. Temperature

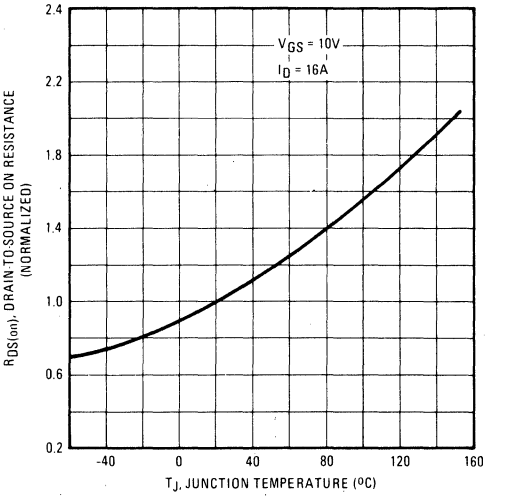


Fig. 9 – Normalized On-Resistance Vs. Temperature

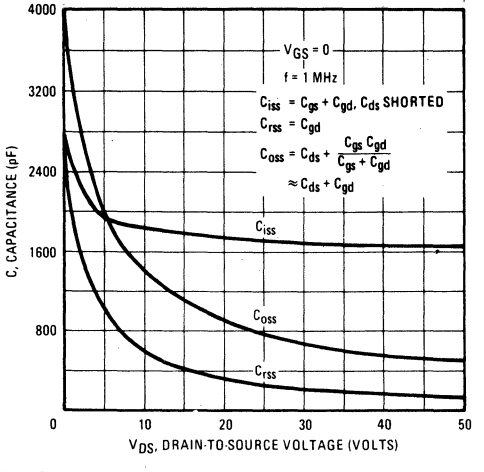


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

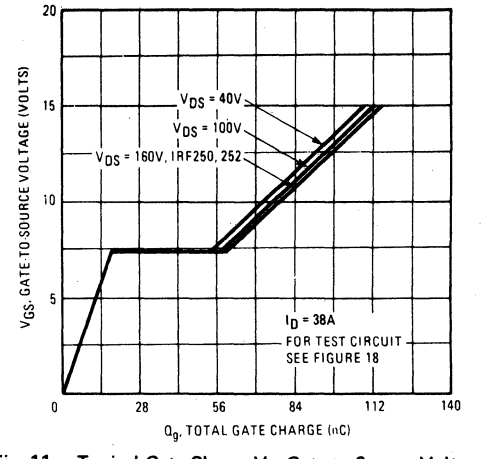


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

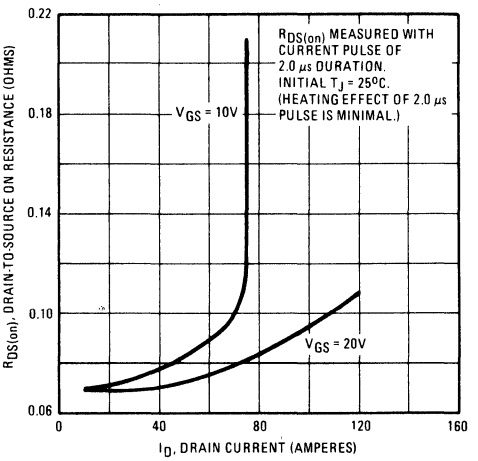


Fig. 12 – Typical On-Resistance Vs. Drain Current

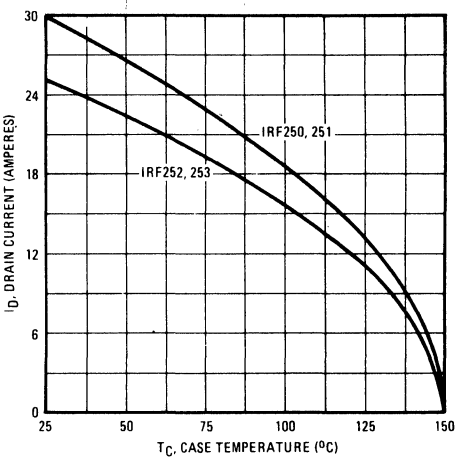


Fig. 13 – Maximum Drain Current Vs. Case Temperature

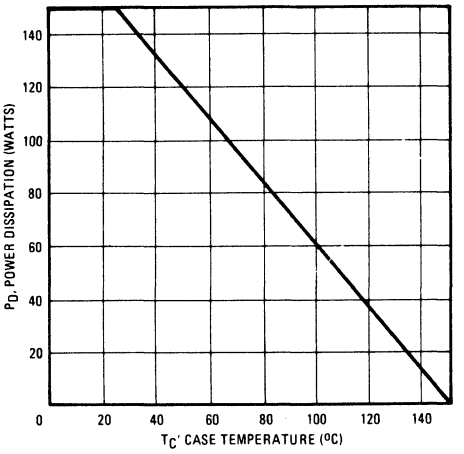


Fig. 14 – Power Vs. Temperature Derating Curve

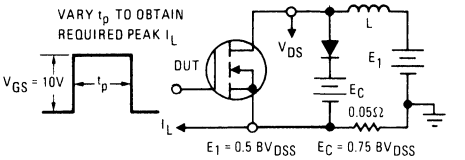


Fig. 15 – Clamped Inductive Test Circuit

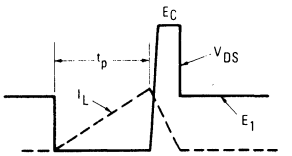


Fig. 16 – Clamped Inductive Waveforms

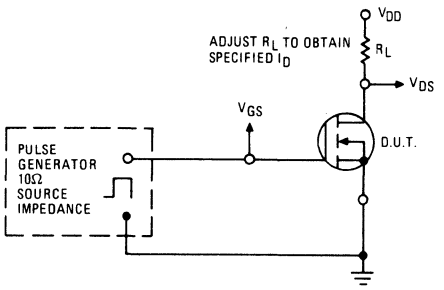


Fig. 17 – Switching Time Test Circuit

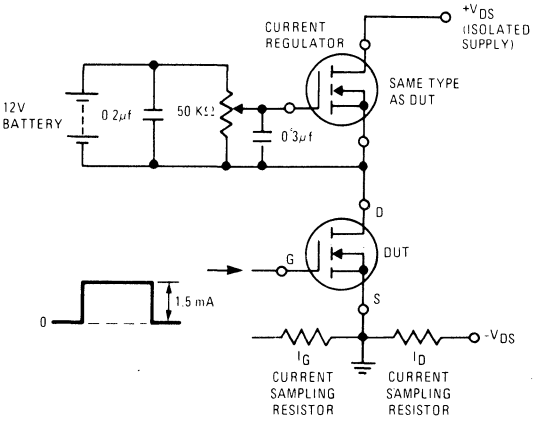


Fig. 18 – Gate Charge Test Circuit

IRF320, IRF321, IRF322, IRF323

File Number **1569**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

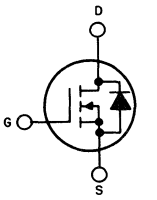
2.5A and 3.0A, 350V-400V

$r_{DS}(on)$ = 1.8 Ω and 2.5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

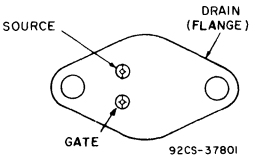
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

The IRF320, IRF321, IRF322 and IRF323 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

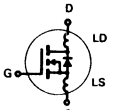
Parameter		IRF320	IRF321	IRF322	IRF323	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		12	12	10	10	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF320, IRF321, IRF322, IRF323

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF320 IRF322	400	–	–	V	V_{GS} = 0V
		IRF321 IRF323	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF320 IRF321	3.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF322 IRF323	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF320 IRF321	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF322 IRF323	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.5A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

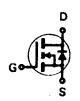


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF320 IRF321	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF322 IRF323	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF320 IRF321	–	–	12	A	
		IRF322 IRF323	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	IRF320 IRF321	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		IRF322 IRF323	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2% ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF320, IRF321, IRF322, IRF323

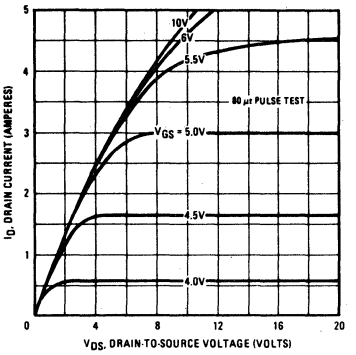


Fig. 1 – Typical Output Characteristics

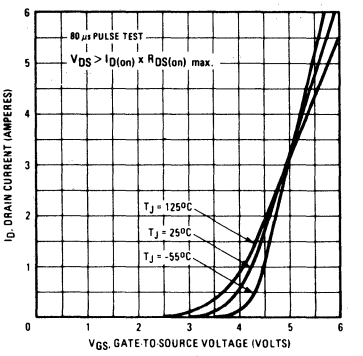


Fig. 2 – Typical Transfer Characteristics

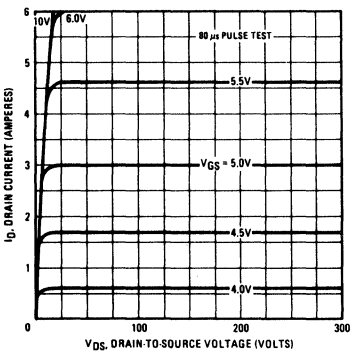


Fig. 3 – Typical Saturation Characteristics

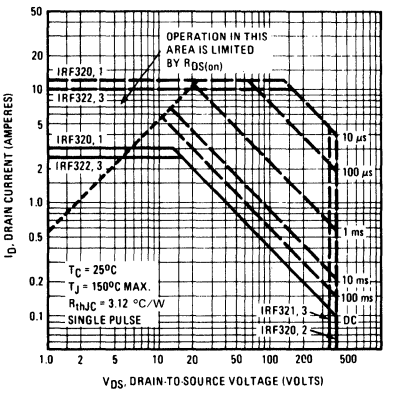


Fig. 4 – Maximum Safe Operating Area

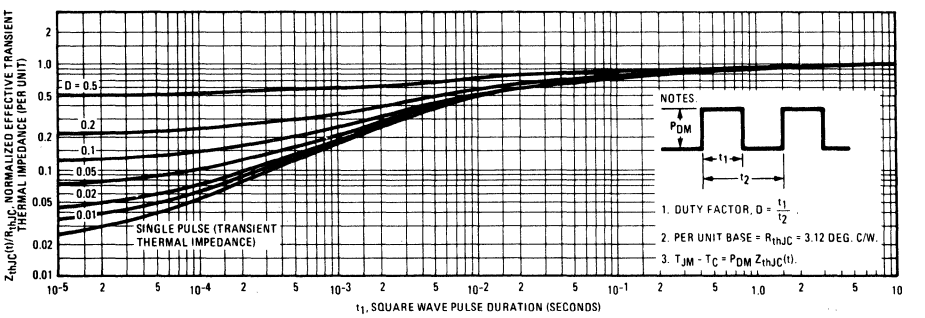


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

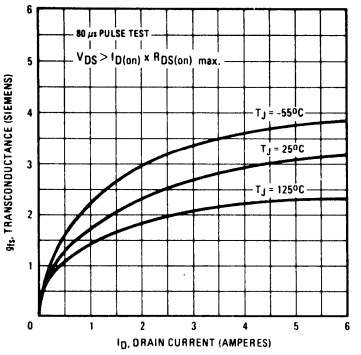


Fig. 6 – Typical Transconductance Vs. Drain Current

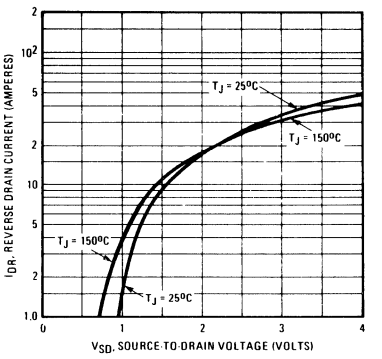


Fig. 7 – Typical Source-Drain Diode Forward Voltage

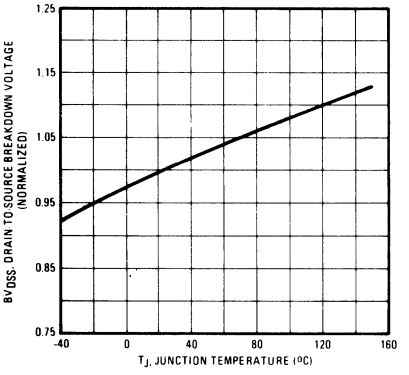


Fig. 8 – Breakdown Voltage Vs. Temperature

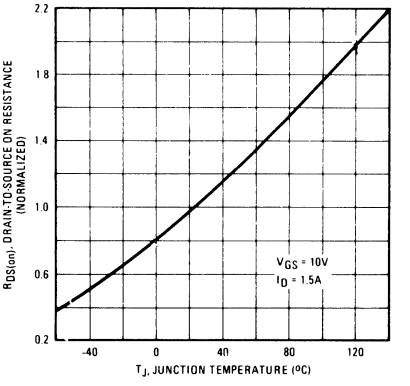


Fig. 9 – Normalized On-Resistance Vs. Temperature

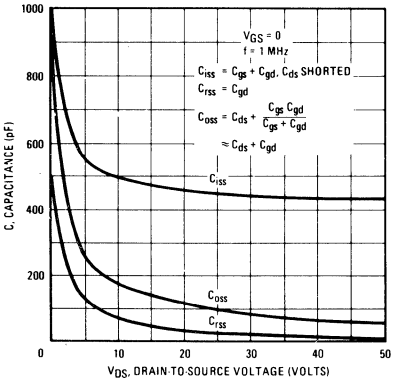


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

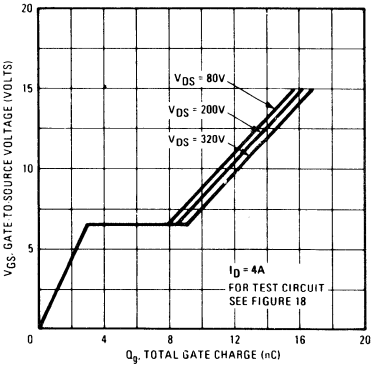


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF320, IRF321, IRF322, IRF323

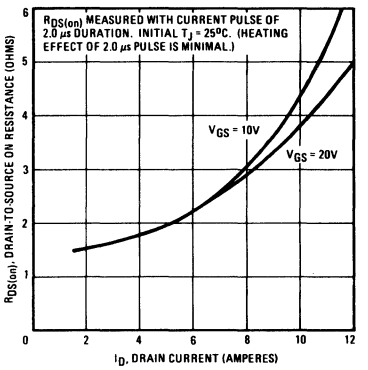


Fig. 12 – Typical On-Resistance Vs. Drain Current

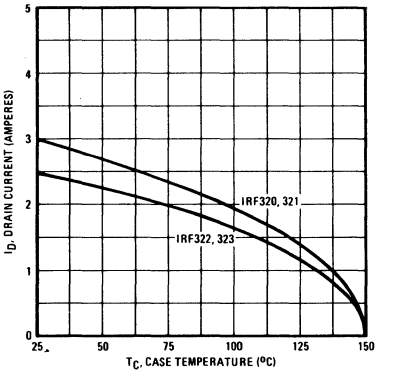


Fig. 13 – Maximum Drain Current Vs. Case Temperature

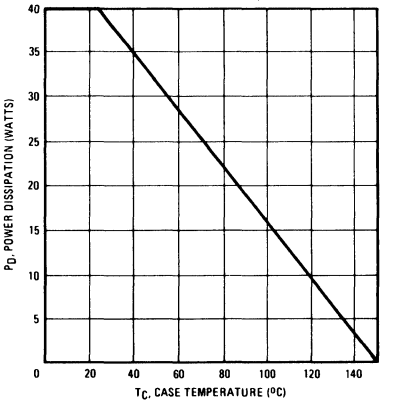


Fig. 14 – Power Vs. Temperature Derating Curve

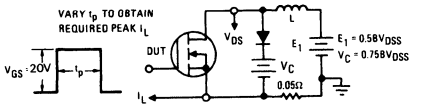


Fig. 15 – Clamped Inductive Test Circuit

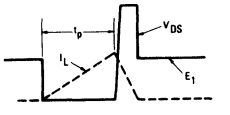


Fig. 16 – Clamped Inductive Waveforms

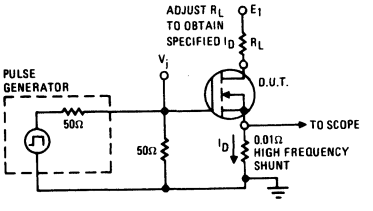


Fig. 17 – Switching Time Test Circuit

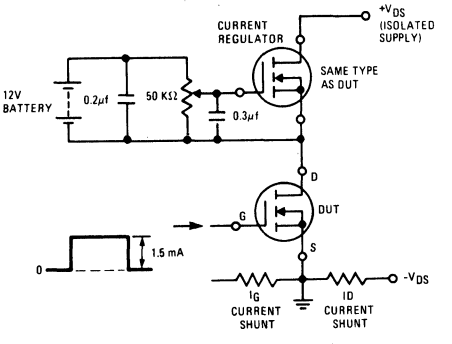


Fig. 18 – Gate Charge Test Circuit

File Number **1570**

IRF330, IRF331, IRF332, IRF333

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

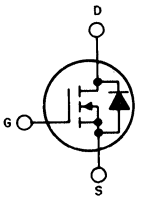
4.5A and 5.5A, 350V-400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

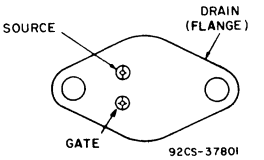
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

The IRF330, IRF331, IRF332 and IRF333 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

Absolute Maximum Ratings

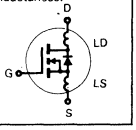
Parameter		IRF330	IRF331	IRF332	IRF333	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF330, IRF331, IRF332, IRF333

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF330 IRF332	400	–	–	V	V_{GS} = 0V
		IRF331 IRF333	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF330 IRF331	5.5	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF332 IRF333	4.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF330 IRF331	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF332 IRF333	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	700	900	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF330 IRF331	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF332 IRF333	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF330 IRF331	–	–	22	A	
		IRF332 IRF333	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	IRF330 IRF331	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF332 IRF333	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

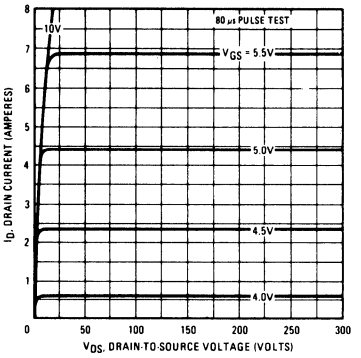


Fig. 1 – Typical Output Characteristics

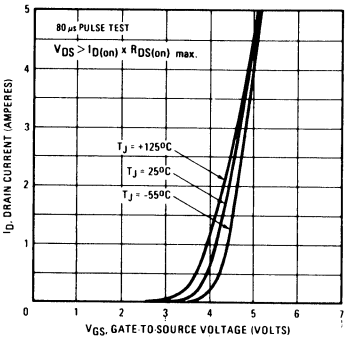


Fig. 2 – Typical Transfer Characteristics

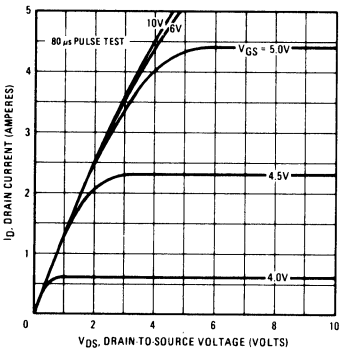


Fig. 3 – Typical Saturation Characteristics

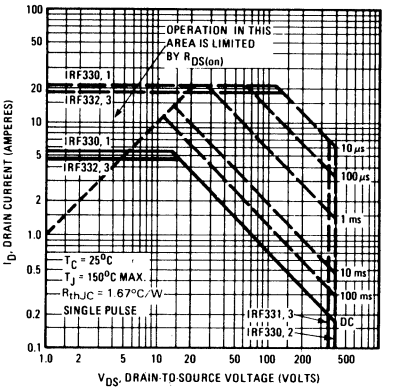


Fig. 4 – Maximum Safe Operating Area

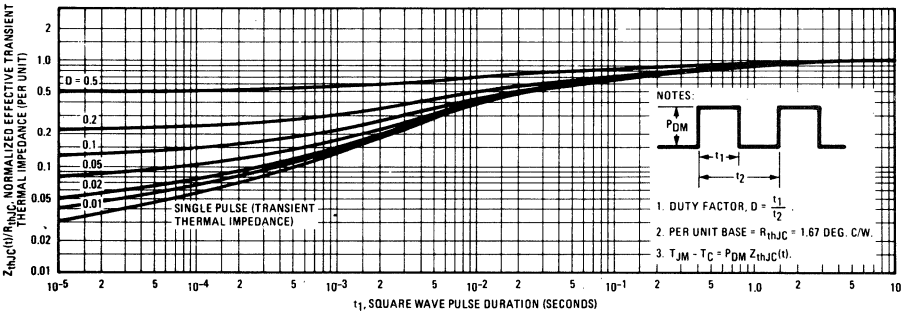


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF330, IRF331, IRF332, IRF333

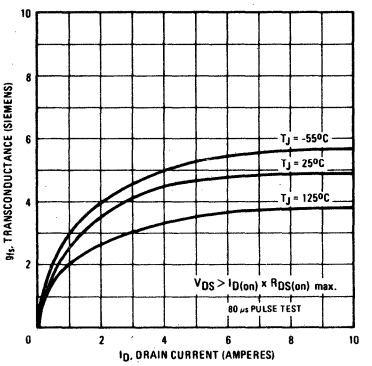


Fig. 6 — Typical Transconductance Vs. Drain Current

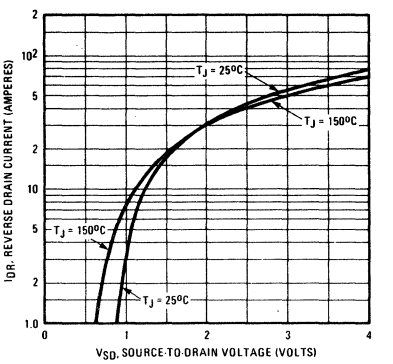


Fig. 7 — Typical Source-Drain Diode Forward Voltage

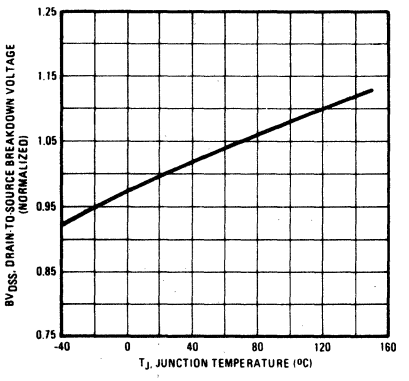


Fig. 8 — Breakdown Voltage Vs. Temperature

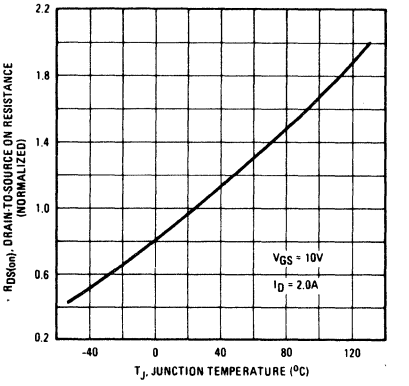


Fig. 9 — Normalized On-Resistance Vs. Temperature

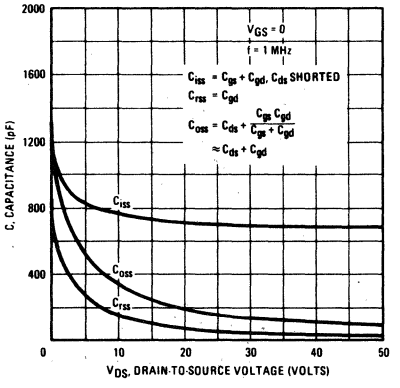


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

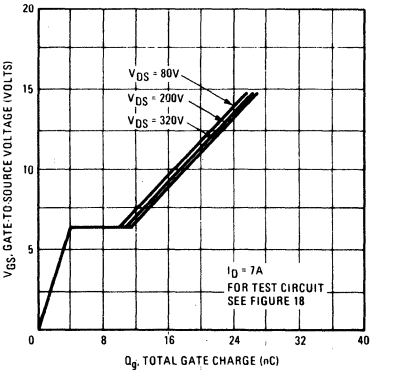


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

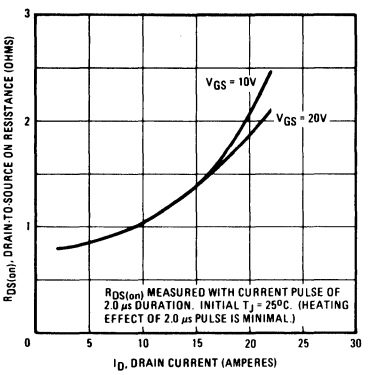


Fig. 12 – Typical On-Resistance Vs. Drain Current

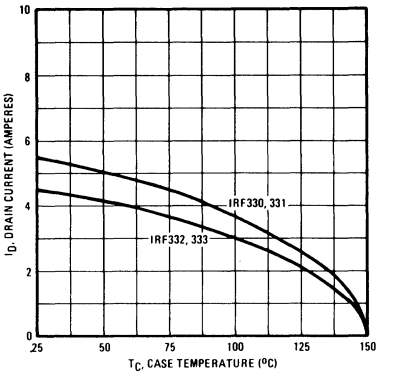


Fig. 13 – Maximum Drain Current Vs. Case Temperature

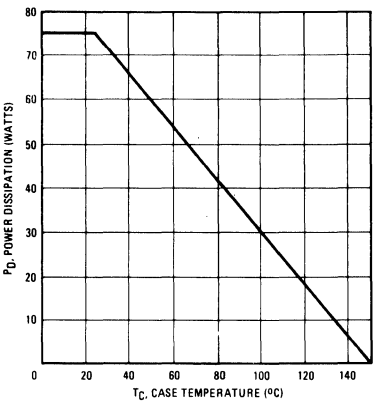


Fig. 14 – Power Vs. Temperature Derating Curve

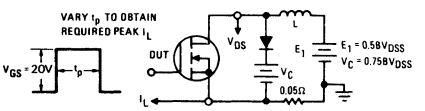


Fig. 15 – Clamped Inductive Test Circuit

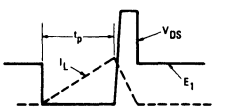


Fig. 16 – Clamped Inductive Waveforms

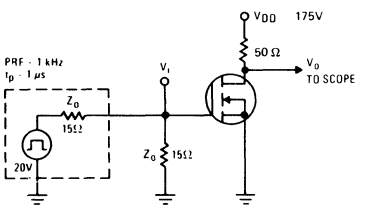


Fig. 17 – Switching Time Test Circuit

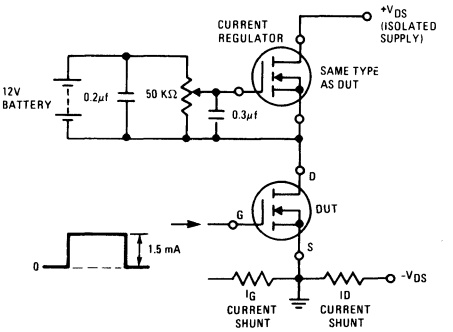


Fig. 18 – Gate Charge Test Circuit

IRF350, IRF351, IRF352, IRF353

File Number **1826**

Power MOS Field-Effect Transistors

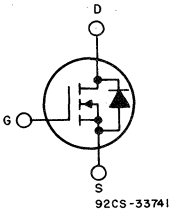
N-Channel Enhancement-Mode Power Field-Effect Transistors

13 A and 15 A, 350 V - 400 V
$r_{DS}(on)$ = 0.3 Ω and 0.4 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE

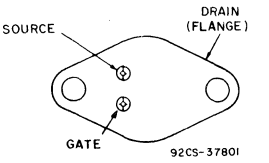


TERMINAL DIAGRAM

The IRF350, IRF351, IRF352 and IRF353 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA metal package.

TERMINAL DESIGNATION



JEDEC TO-204AA

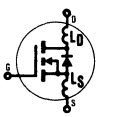
Absolute Maximum Ratings

Parameter		IRF350	IRF351	IRF352	IRF353	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	15	15	13	13	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	60	60	52	52	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		60	60	52	52	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF350 IRF352	400	–	–	V	V_{GS} = 0V
		IRF351 IRF353	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF350 IRF351	15	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF352 IRF353	13	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF350 IRF351	–	0.25	0.3	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF352 IRF353	–	0.3	0.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	8.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} = 180V, I_D = 8.0A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	65	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	75	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	79	120	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	38	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	41	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF350 IRF351	–	–	15	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF352 IRF353	–	–	13	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF350 IRF351	–	–	60	A	
		IRF352 IRF353	–	–	52	A	
V_{SD}	Diode Forward Voltage ②	IRF350 IRF351	–	–	1.6	V	T_C = 25°C, I_S = 15A, V_{GS} = 0V
		IRF352 IRF353	–	–	1.5	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1000	–	ns	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.6	–	μC	T_J = 150°C, I_F = 15A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF350, IRF351, IRF352, IRF353

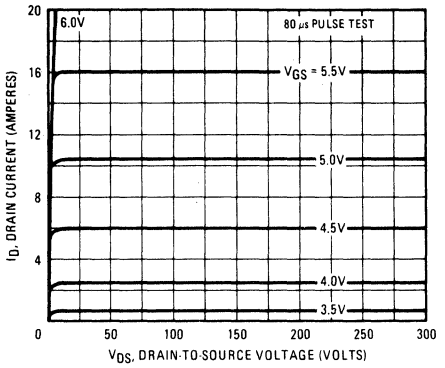


Fig. 1 — Typical Output Characteristics

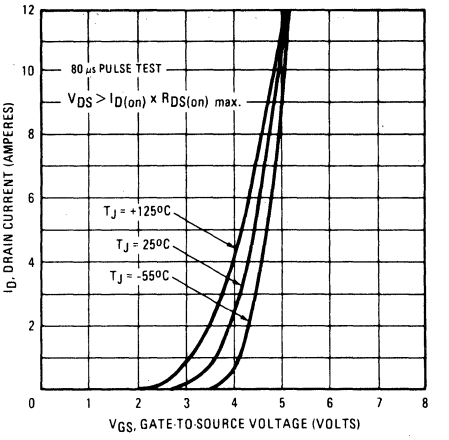


Fig. 2 — Typical Transfer Characteristics

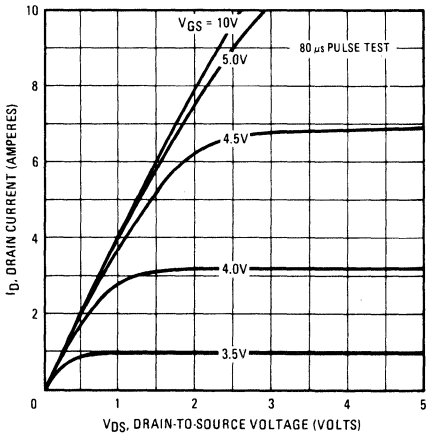


Fig. 3 — Typical Saturation Characteristics

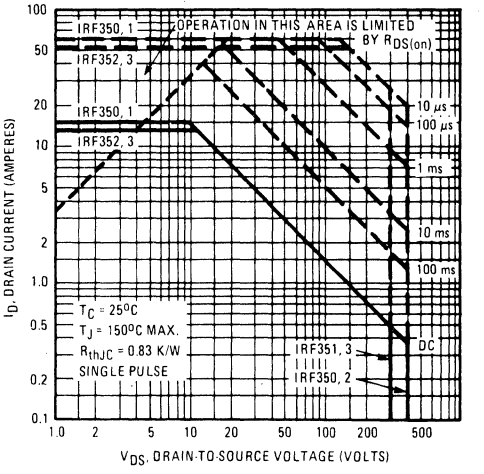


Fig. 4 — Maximum Safe Operating Area

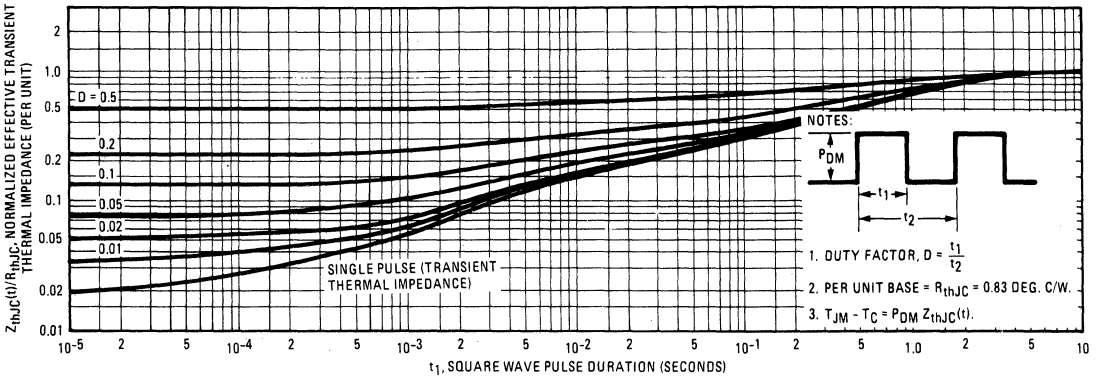


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

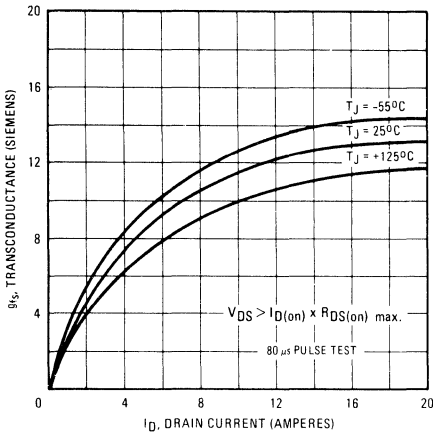


Fig. 6 – Typical Transconductance Vs. Drain Current

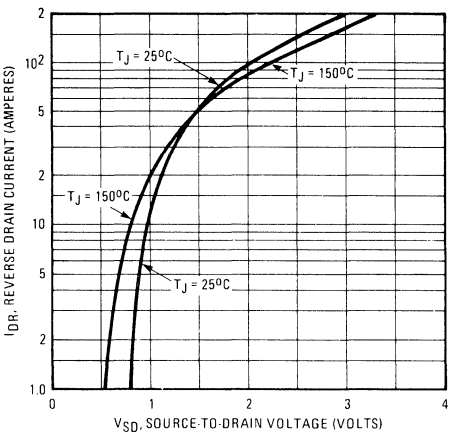


Fig. 7 – Typical Source-Drain Diode Forward Voltage

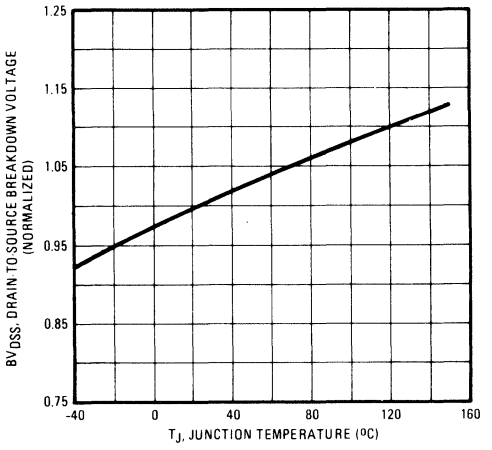


Fig. 8 – Breakdown Voltage Vs. Temperature

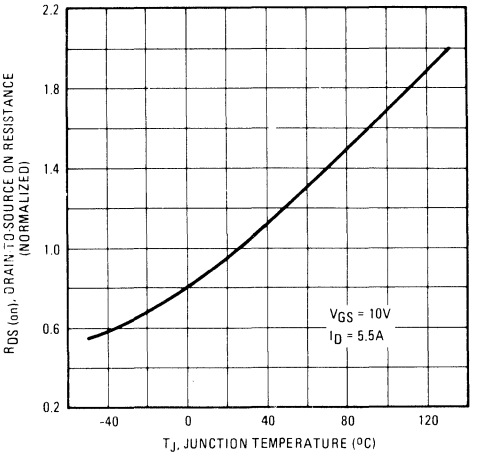


Fig. 9 – Normalized On-Resistance Vs. Temperature

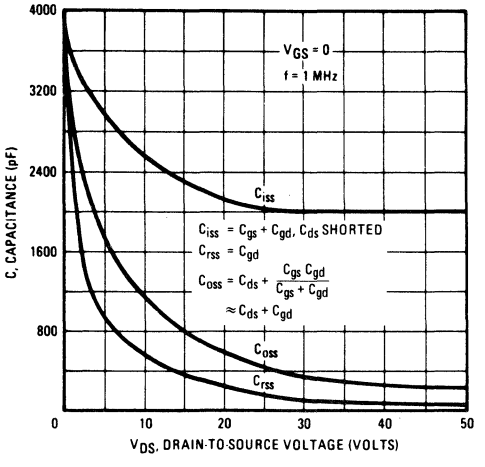


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

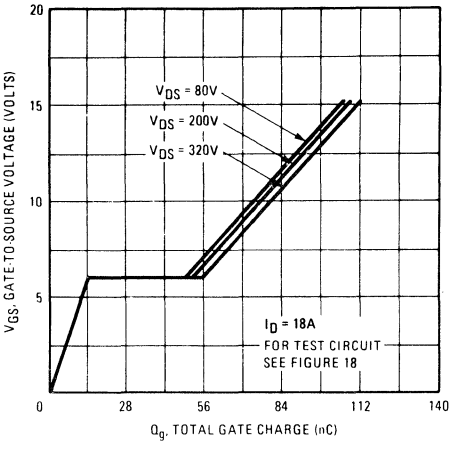


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF350, IRF351, IRF352, IRF353

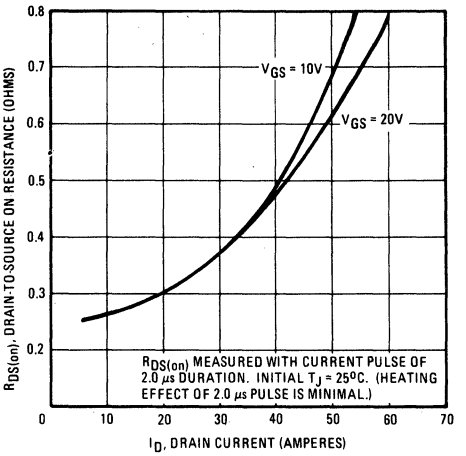


Fig. 12 – Typical On-Resistance Vs. Drain Current

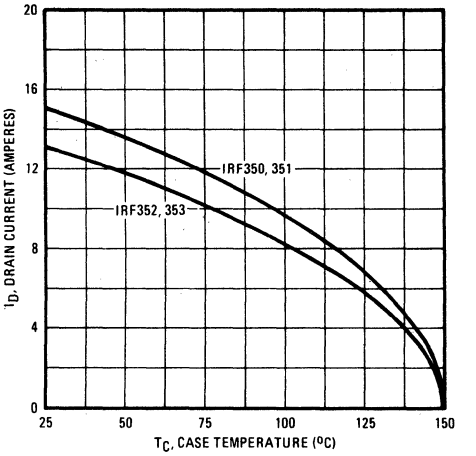


Fig. 13 – Maximum Drain Current Vs. Case Temperature

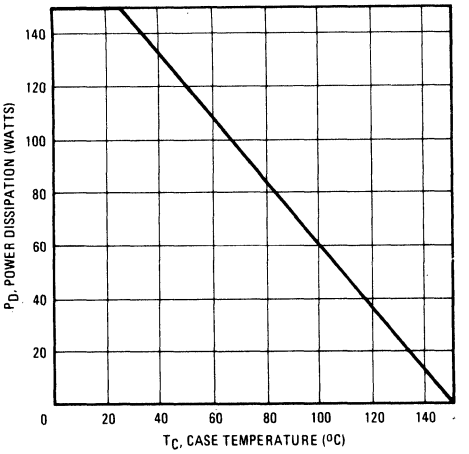


Fig. 14 – Power Vs. Temperature Derating Curve

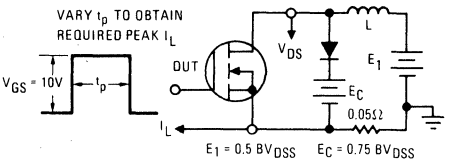


Fig. 15 – Clamped Inductive Test Circuit

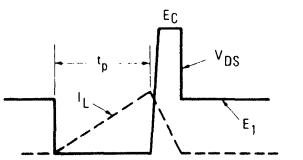


Fig. 16 – Clamped Inductive Waveforms

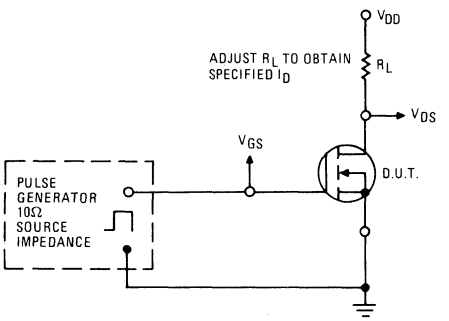


Fig. 17 – Switching Time Test Circuit

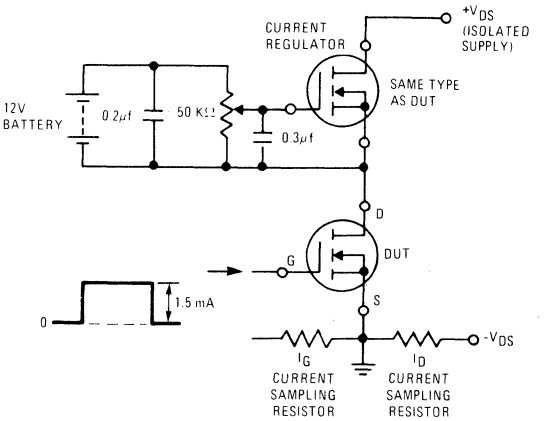


Fig. 18 – Gate Charge Test Circuit

File Number **1571**

IRF420, IRF421, IRF422, IRF423

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.0A and 2.5A, 450V-500V

$r_{DS}(on)$ = 3.0 Ω and 4.0 Ω

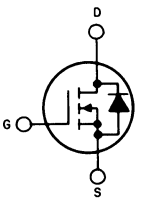
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF420, IRF421, IRF422 and IRF423 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AA steel package.

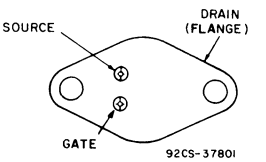
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

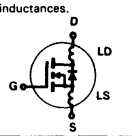
Parameter		IRF420	IRF421	IRF422	IRF423	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF420, IRF421, IRF422, IRF423

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF420, IRF422	500	–	–	V	V_{GS} = 0V
		IRF421, IRF423	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF420, IRF421	2.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF422, IRF423	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF420, IRF421	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF422, IRF423	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.0A, Z_O = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

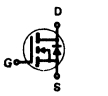


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF420, IRF421	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF422, IRF423	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF420, IRF421	–	–	10	A	
		IRF422, IRF423	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF420, IRF421	–	–	1.4	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF422, IRF423	–	–	1.3	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

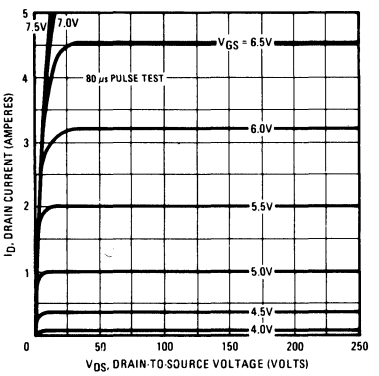


Fig. 1 – Typical Output Characteristics

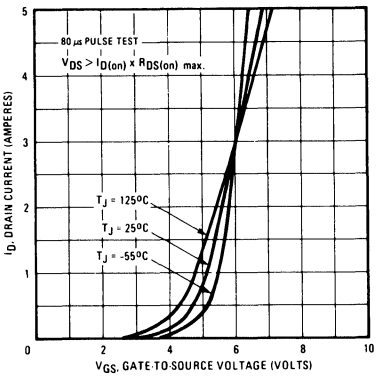


Fig. 2 – Typical Transfer Characteristics

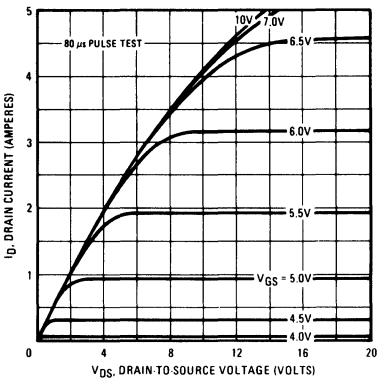


Fig. 3 – Typical Saturation Characteristics

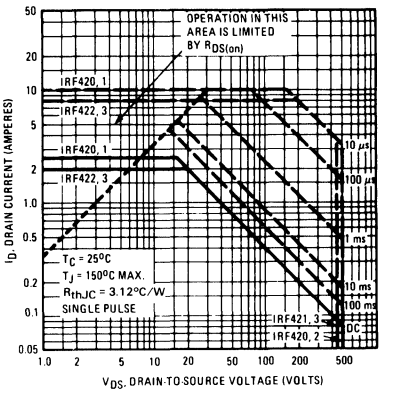


Fig. 4 – Maximum Safe Operating Area

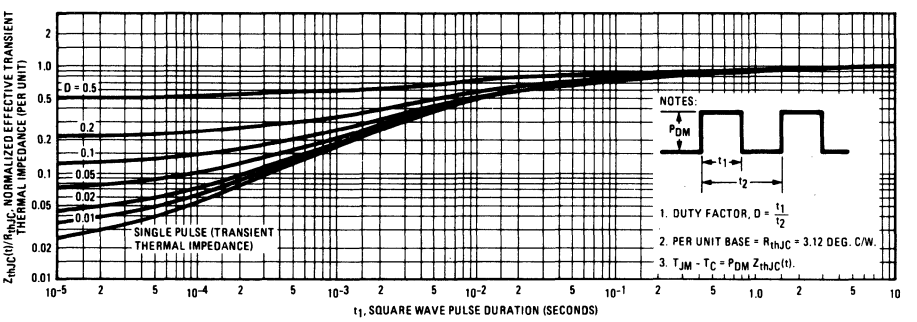


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

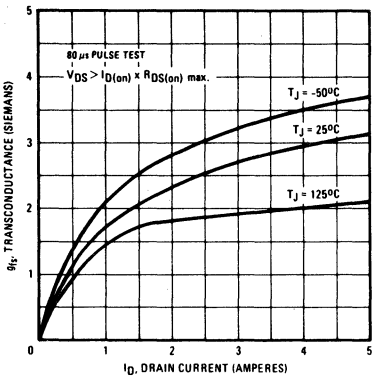


Fig. 6 – Typical Transconductance Vs. Drain Current

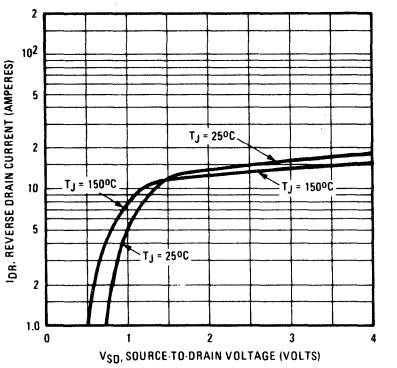


Fig. 7 – Typical Source-Drain Diode Forward Voltage

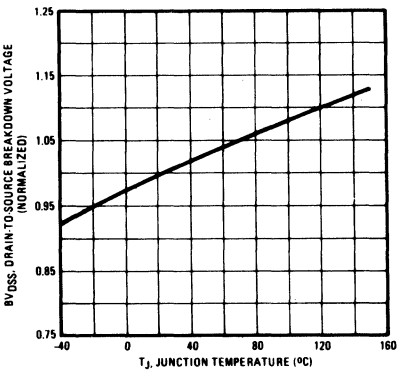


Fig. 8 – Breakdown Voltage Vs. Temperature

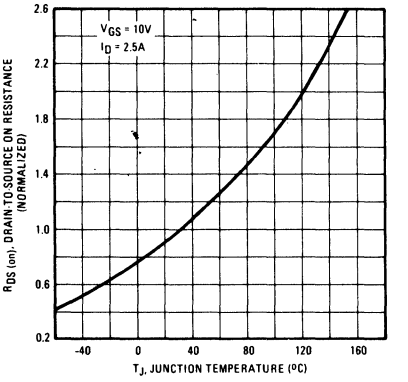


Fig. 9 – Normalized On-Resistance Vs. Temperature

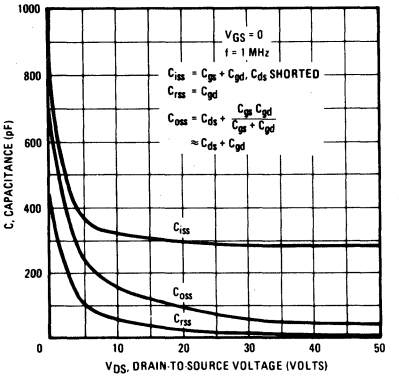


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

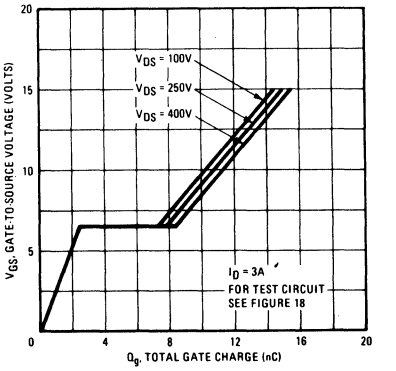


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

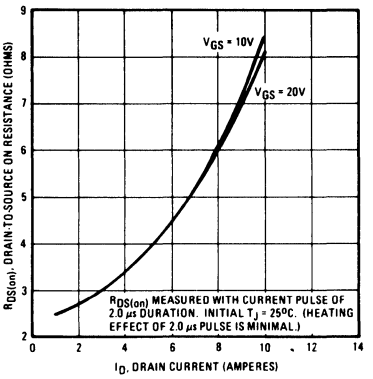


Fig. 12 – Typical On-Resistance Vs. Drain Current

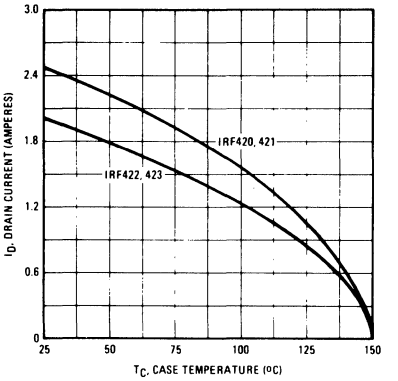


Fig. 13 – Maximum Drain Current Vs. Case Temperature

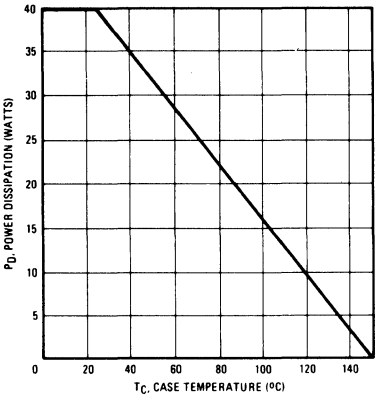


Fig. 14 – Power Vs. Temperature Derating Curve

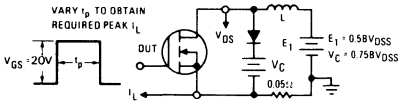


Fig. 15 – Clamped Inductive Test Circuit

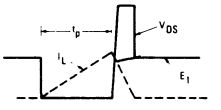


Fig. 16 – Clamped Inductive Waveforms

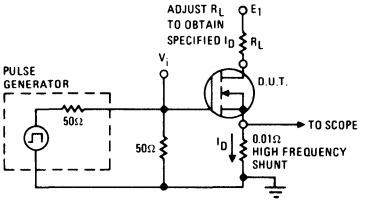


Fig. 17 – Switching Time Test Circuit

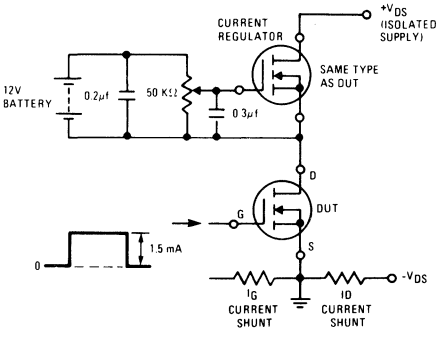


Fig. 18 – Gate Charge Test Circuit

IRF430, IRF431, IRF432, IRF433

File Number **1572**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

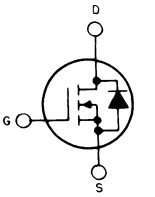
4.0A and 4.5A, 450V-500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



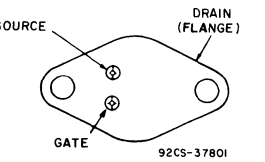
92CS-33741

TERMINAL DIAGRAM

The IRF430, IRF431, IRF432 and IRF433 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The **IRF-types** are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



JEDEC TO-204AA

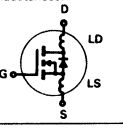
Absolute Maximum Ratings

Parameter		IRF430	IRF431	IRF432	IRF433	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		18	18	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF430, IRF432	500	–	–	V	V_{GS} = 0V
		IRF431, IRF433	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF430, IRF431	4.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF432, IRF433	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF430, IRF431	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF432, IRF433	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.2	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} ≈ 225V, I_D = 2.5A, Z_0 = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF430, IRF431	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF432, IRF433	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF430, IRF431	–	–	18	A	
		IRF432, IRF433	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF430, IRF431	–	–	1.4	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF432, IRF433	–	–	1.3	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF430, IRF431, IRF432, IRF433

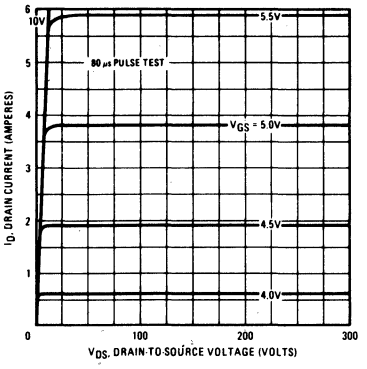


Fig. 1 – Typical Output Characteristics

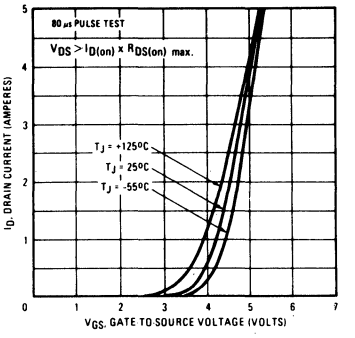


Fig. 2 – Typical Transfer Characteristics

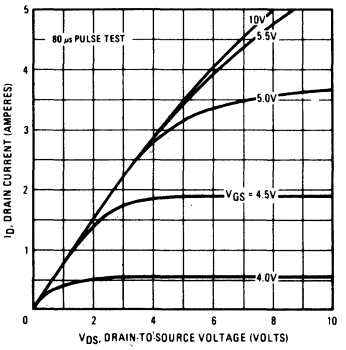


Fig. 3 – Typical Saturation Characteristics

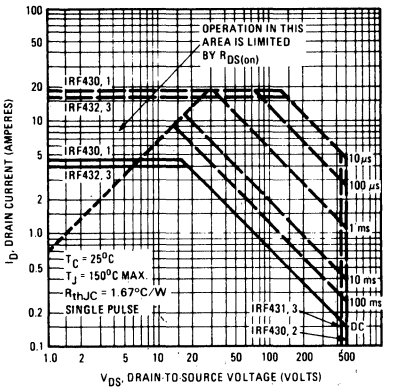


Fig. 4 – Maximum Safe Operating Area

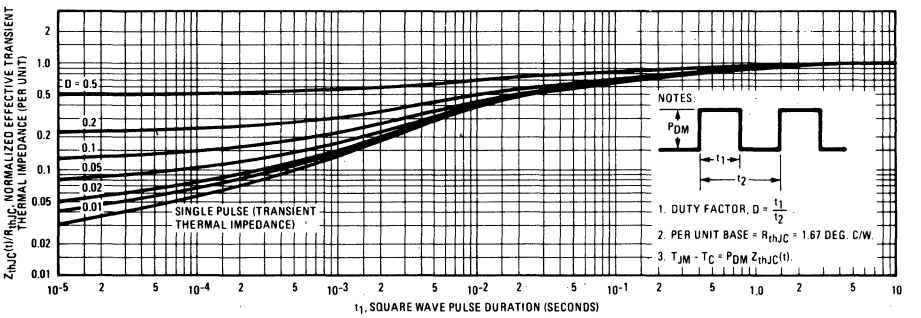


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

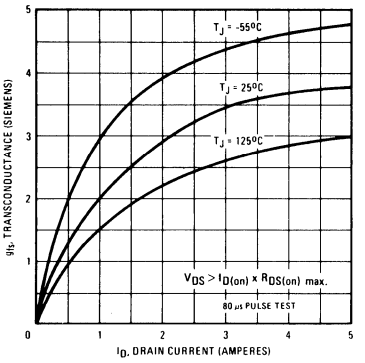


Fig. 6 — Typical Transconductance Vs. Drain Current

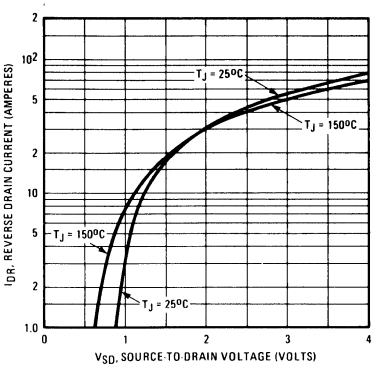


Fig. 7 — Typical Source-Drain Diode Forward Voltage

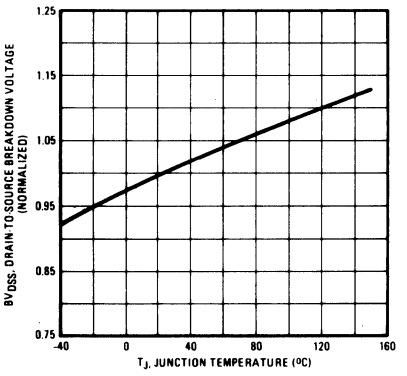


Fig. 8 — Breakdown Voltage Vs. Temperature

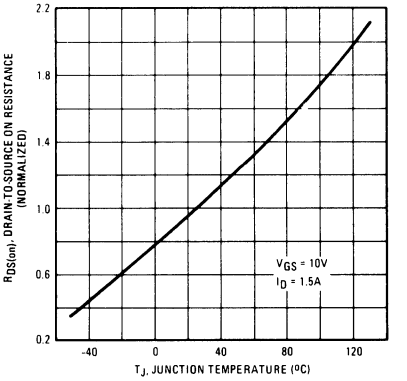


Fig. 9 — Normalized On-Resistance Vs. Temperature

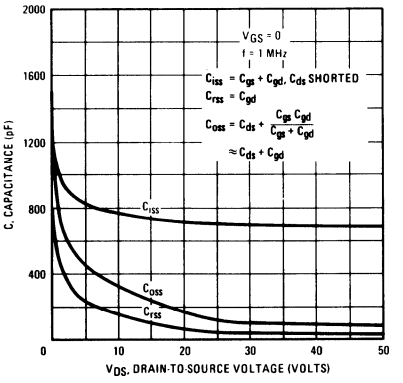


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

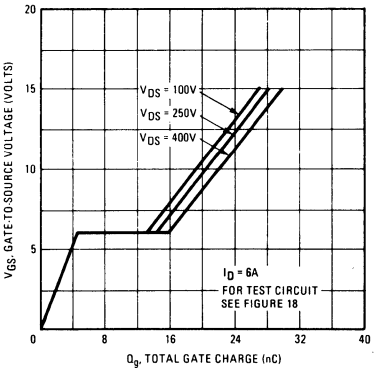


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF430, IRF431, IRF432, IRF433

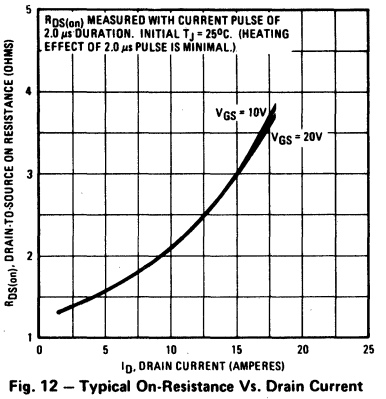


Fig. 12 – Typical On-Resistance Vs. Drain Current

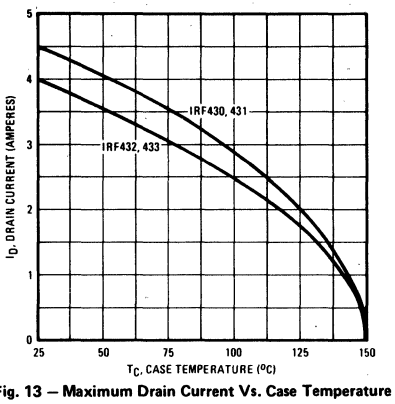


Fig. 13 – Maximum Drain Current Vs. Case Temperature

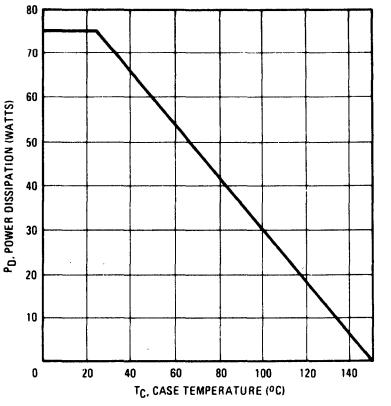


Fig. 14 – Power Vs. Temperature Derating Curve

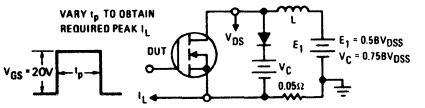


Fig. 15 – Clamped Inductive Test Circuit

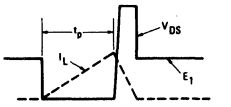


Fig. 16 – Clamped Inductive Waveforms

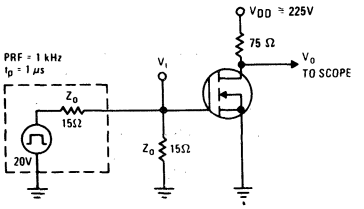


Fig. 17 – Switching Time Test Circuit

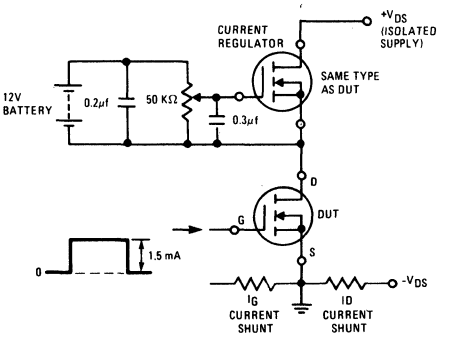


Fig. 18 – Gate Charge Test Circuit

File Number **1827**

IRF450, IRF451, IRF452, IRF453

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

12 A and 13 A, 450 V - 500 V
$r_{DS}(on)$ = 0.4 Ω and 0.5 Ω

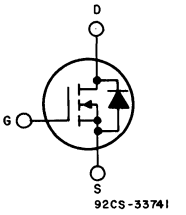
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF450, IRF451, IRF452 and IRF453 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

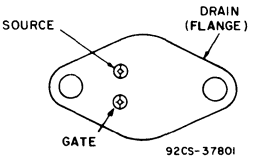
The IRF-types are supplied in the JEDEC TO-204AA metal package.

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-204AA

Absolute Maximum Ratings

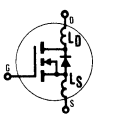
Parameter		IRF450	IRF451	IRF452	IRF453	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 kΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	13	13	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM}	Pulsed Drain Current ③	52	52	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	150 (See Fig. 14)				W
	Linear Derating Factor	1.2 (See Fig. 14)				W/K
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH				A
		52	52	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF450, IRF451, IRF452, IRF453

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF450 IRF452	500	–	–	V	V_{GS} = 0V
		IRF451 IRF453	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	100	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF450 IRF451	13	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF452 IRF453	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF450 IRF451	–	0.3	0.4	Ω	V_{GS} = 10V, I_D = 7.0A
		IRF452 IRF453	–	0.4	0.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	11	–	S(℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 7.0A
C_{iss}	Input Capacitance	ALL	–	2000	3000	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	400	600	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	200	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35	ns	V_{DD} ≈ 210V, I_D = 7.0A, Z_0 = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	150	ns	
t_f	Fall Time	ALL	–	–	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	82	120	nC	V_{GS} = 10V, I_D = 16A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentialiv independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	40	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	42	–	nC	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured between the contact screw on header that is closer to source and gate pins and center of die.
L_S	Internal Source Inductance	ALL	–	12.5	–	nH	Measured from the source pin, 6 mm (0.25 in.) from header and source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	.83	K/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	K/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	K/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF450 IRF451	–	–	13	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF452 IRF453	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF450 IRF451	–	–	52	A	
		IRF452 IRF453	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF450 IRF451	–	–	1.4	V	T_C = 25°C, I_S = 13A, V_{GS} = 0V
		IRF452 IRF453	–	–	1.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	1300	–	ns	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.4	–	μC	T_J = 150°C, I_F = 13A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

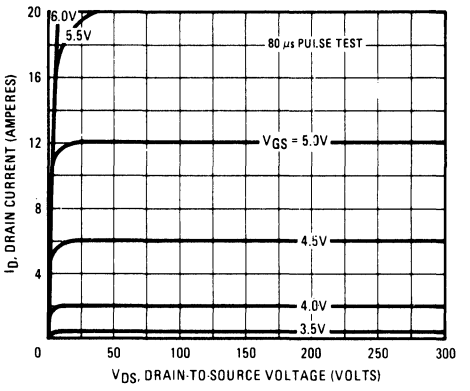


Fig. 1 — Typical Output Characteristics

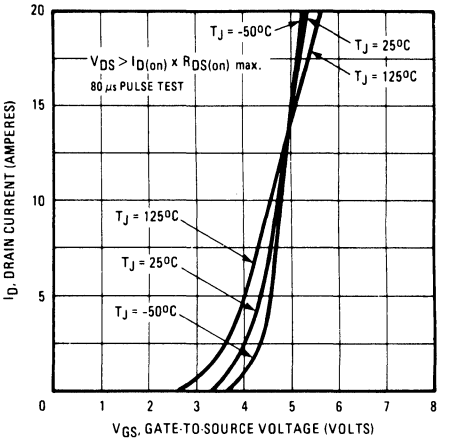


Fig. 2 — Typical Transfer Characteristics

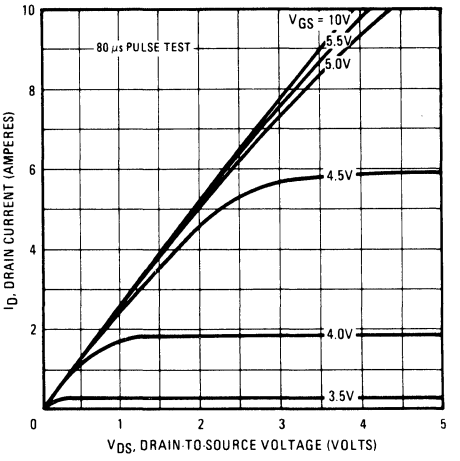


Fig. 3 — Typical Saturation Characteristics

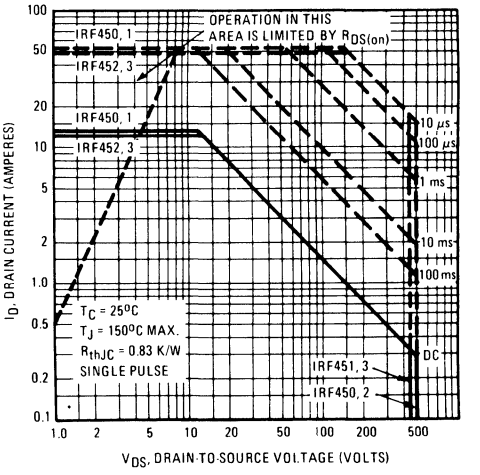


Fig. 4 — Maximum Safe Operating Area

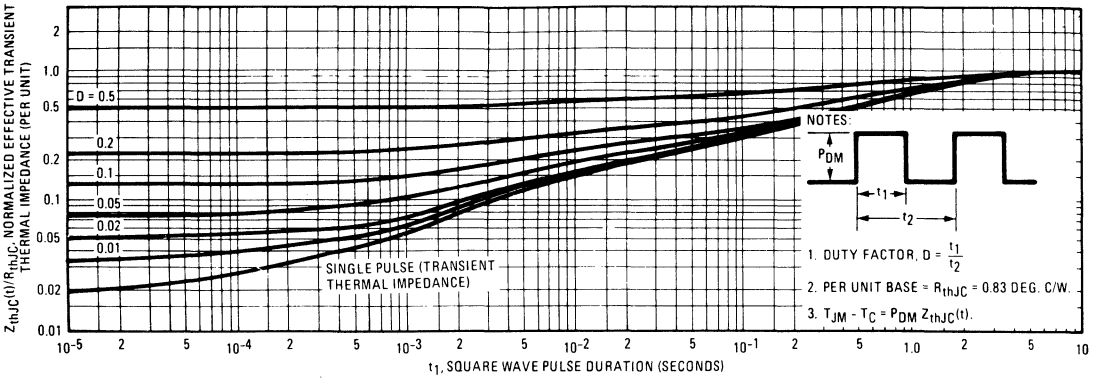


Fig. 5 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

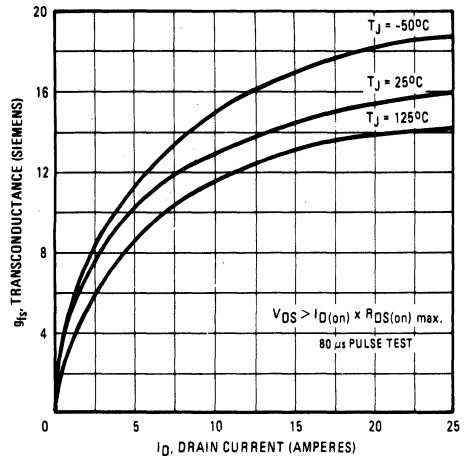


Fig. 6 — Typical Transconductance Vs. Drain Current

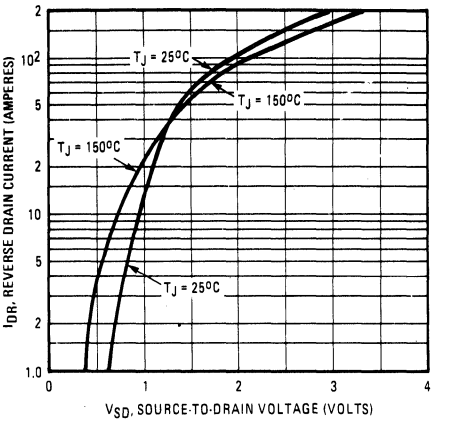


Fig. 7 — Typical Source-Drain Diode Forward Voltage

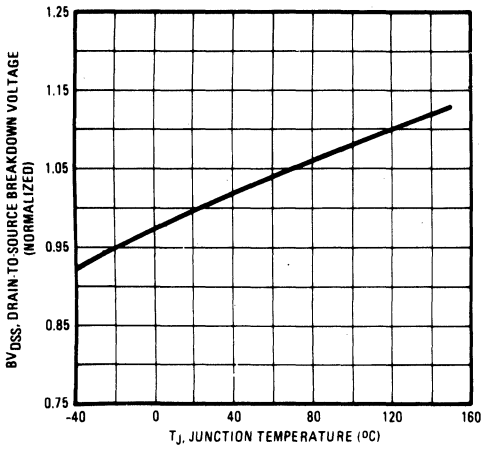


Fig. 8 — Breakdown Voltage Vs. Temperature

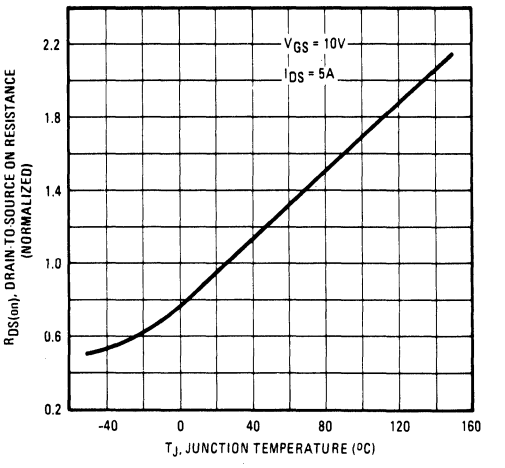


Fig. 9 — Normalized On-Resistance Vs. Temperature

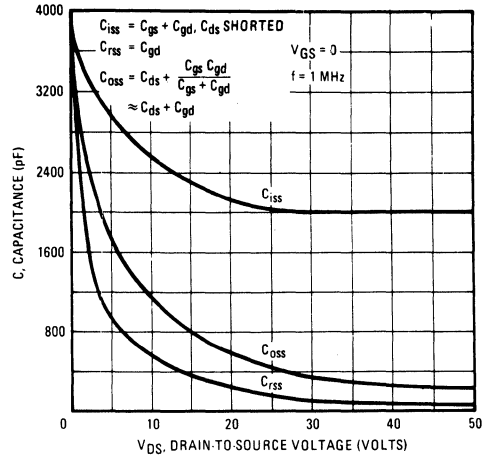


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

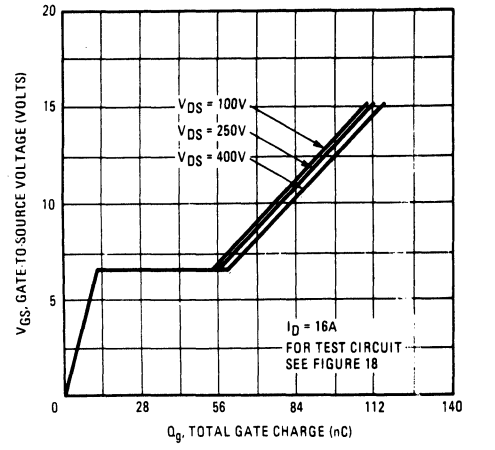


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

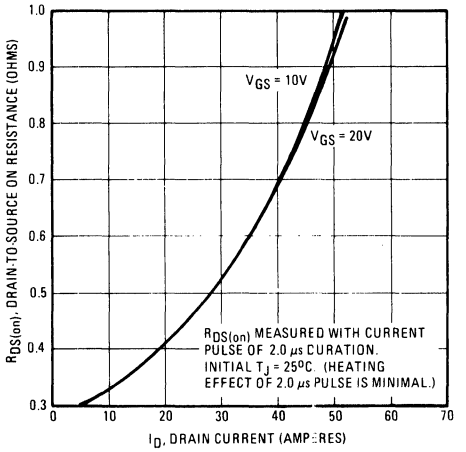


Fig. 12 – Typical On-Resistance Vs. Drain Current

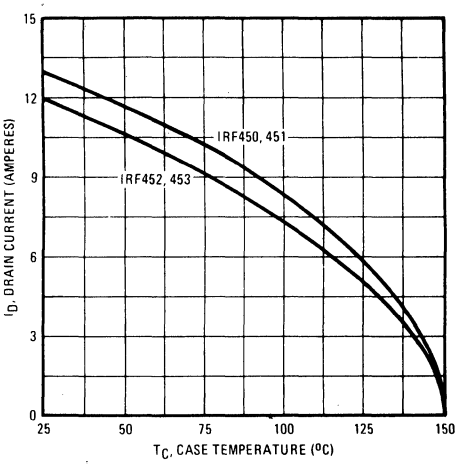


Fig. 13 – Maximum Drain Current Vs. Case Temperature

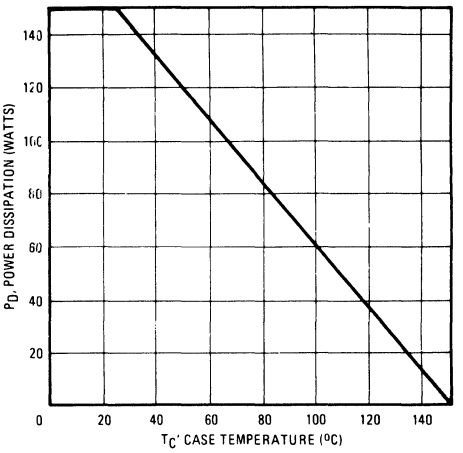


Fig. 14 – Power Vs. Temperature Derating Curve

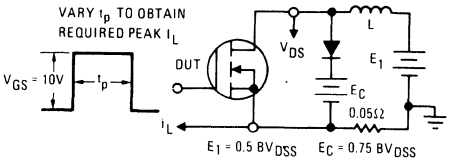


Fig. 15 – Clamped Inductive Test Circuit

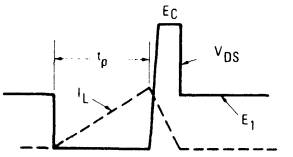


Fig. 16 – Clamped Inductive Waveforms

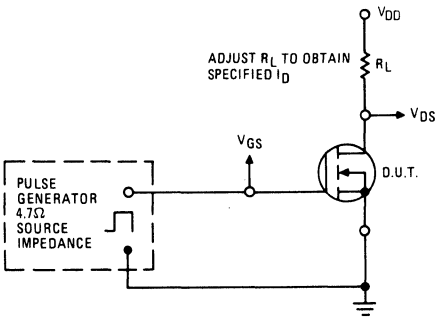


Fig. 17 – Switching Time Test Circuit

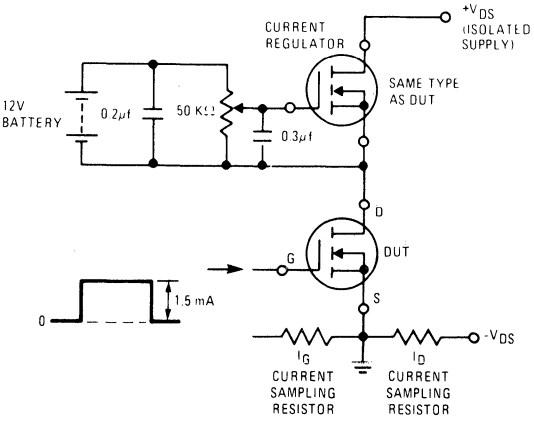


Fig. 18 – Gate Charge Test Circuit

IRF510, IRF511, IRF512, IRF513

File Number **1573**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

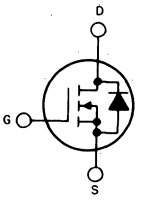
3.5A and 4.0A, 60V-100V

$r_{DS}(on)$ = 0.6 Ω and 0.8 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

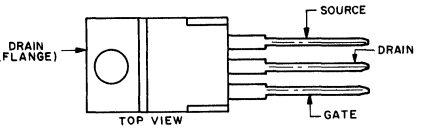
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF510, IRF511, IRF512 and IRF513 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

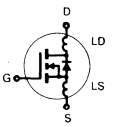
Absolute Maximum Ratings

Parameter		IRF510	IRF511	IRF512	IRF513	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0	4.0	3.5	3.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_{DM}	Pulsed Drain Current ③	16	16	14	14	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		16	16	14	14	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF510 IRF512	100	–	–	V	V_{GS} = 0V
		IRF511 IRF513	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF510 IRF511	4.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF512 IRF513	3.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF510 IRF511	–	0.5	0.6	Ω	V_{GS} = 10V, I_D = 2.0A
		IRF512 IRF513	–	0.6	0.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.5	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 2.0A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	80	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	10	20	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 2.0A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	15	25	ns	
t_f	Fall Time	ALL	–	10	20	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	5.0	7.5	nC	V_{GS} = 10V, I_D = 8.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	3.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

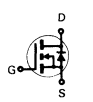


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF510 IRF511	–	–	4.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF512 IRF513	–	–	3.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF510 IRF511	–	–	16	A	
		IRF512 IRF513	–	–	14	A	
V_{SD}	Diode Forward Voltage ②	IRF510 IRF511	–	–	2.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
		IRF512 IRF513	–	–	2.0	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	230	–	ns	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.4	–	μC	T_J = 150°C, I_F = 4.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF510, IRF511, IRF512, IRF513

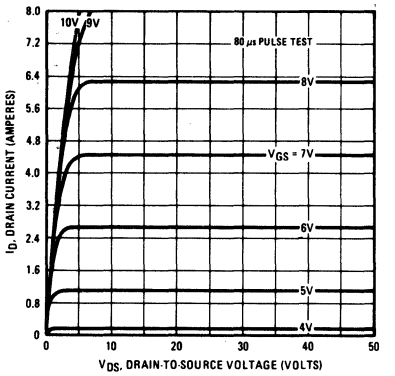


Fig. 1 – Typical Output Characteristics

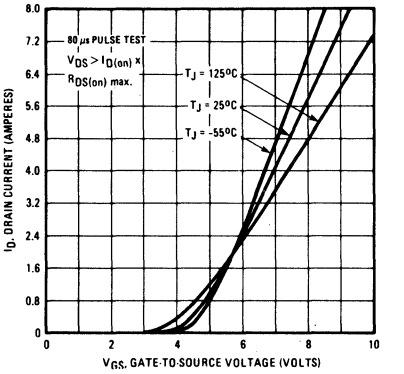


Fig. 2 – Typical Transfer Characteristics

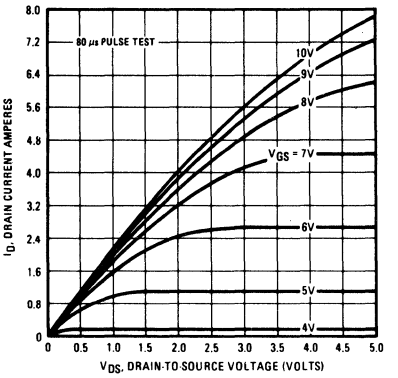


Fig. 3 – Typical Saturation Characteristics

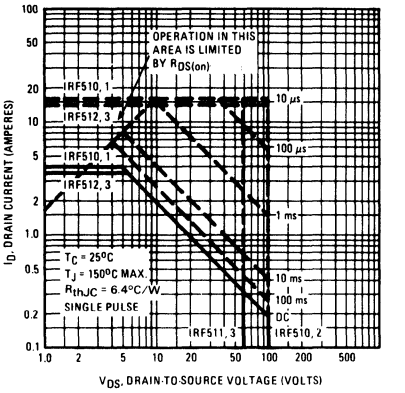


Fig. 4 – Maximum Safe Operating Area

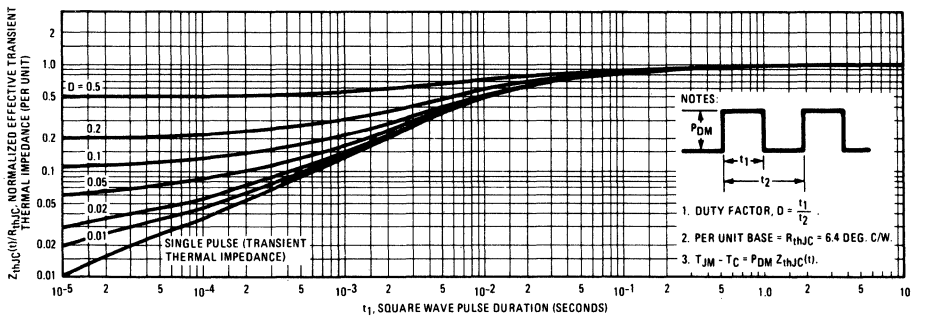


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

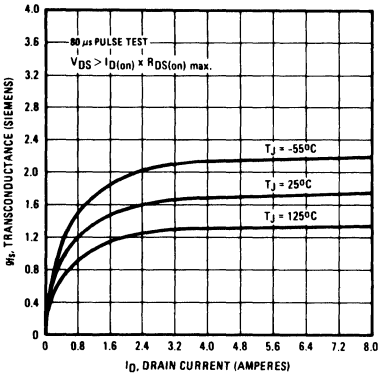


Fig. 6 — Typical Transconductance Vs. Drain Current

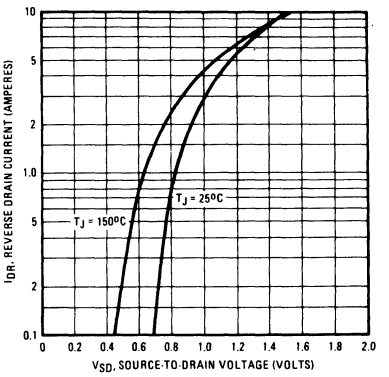


Fig. 7 — Typical Source-Drain Diode Forward Voltage

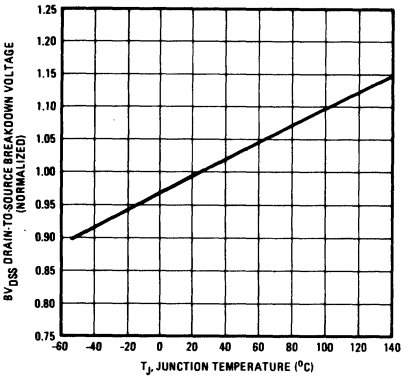


Fig. 8 — Breakdown Voltage Vs. Temperature

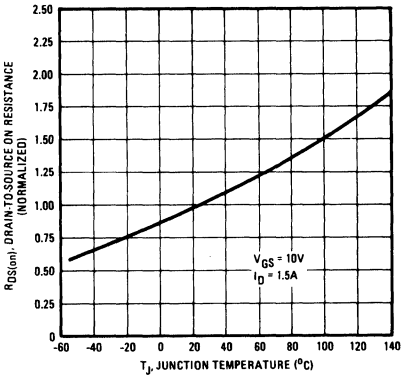


Fig. 9 — Normalized On-Resistance Vs. Temperature

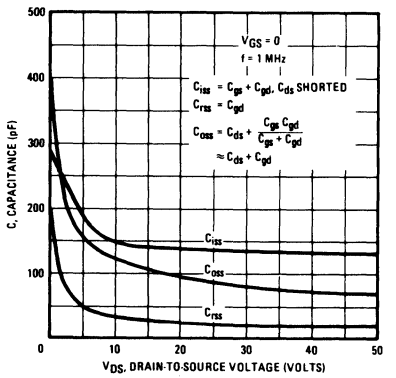


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

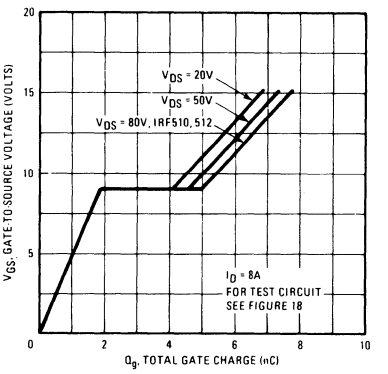


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF510, IRF511, IRF512, IRF513

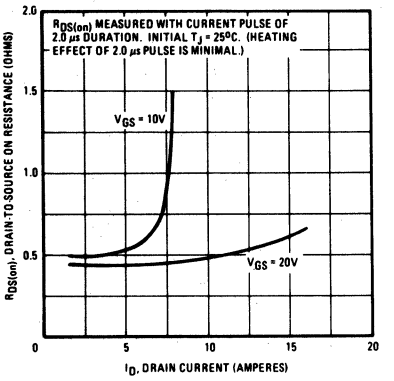


Fig. 12 – Typical On-Resistance Vs. Drain Current

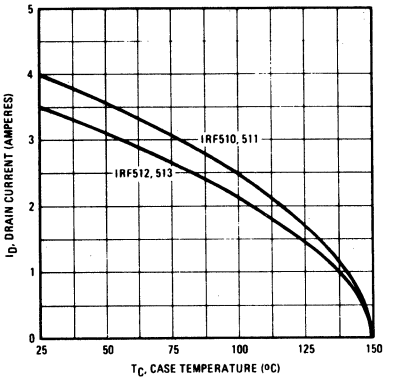


Fig. 13 – Maximum Drain Current Vs. Case Temperature

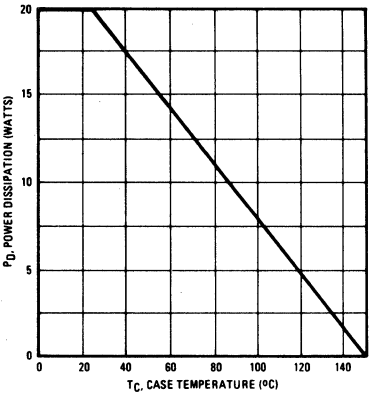


Fig. 14 – Power Vs. Temperature Derating Curve

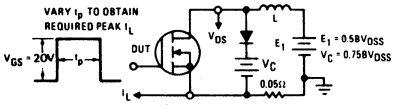


Fig. 15 – Clamped Inductive Test Circuit

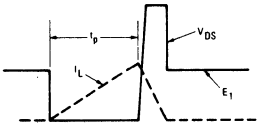


Fig. 16 – Clamped Inductive Waveforms

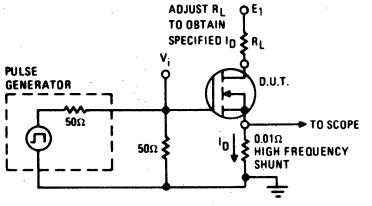


Fig. 17 – Switching Time Test Circuit

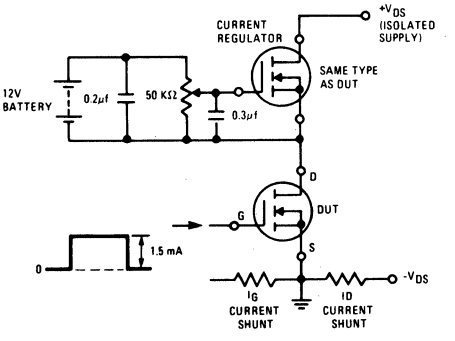


Fig. 18 – Gate Charge Test Circuit

File Number **1574**

IRF520, IRF521, IRF522, IRF523

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

7.0A and 8.0A, 60V-100V

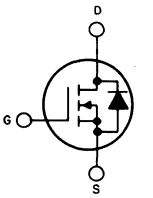
$r_{DS}(on)$ = 0.30 Ω and 0.40 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF520, IRF521, IRF522 and IRF523 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

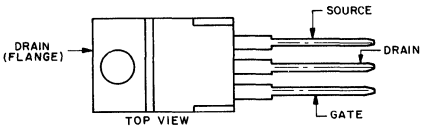
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

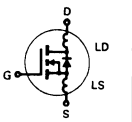
Parameter		IRF520	IRF521	IRF522	IRF523	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_{DM}	Pulsed Drain Current ③	32	32	28	28	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		32	32	28	28	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF520, IRF521, IRF522, IRF523

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF520 IRF522	100	–	–	V	V_{GS} = 0V
		IRF521 IRF523	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF520 IRF521	8.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF522 IRF523	7.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF520 IRF521	–	0.25	0.30	Ω	V_{GS} = 10V, I_D = 4.0A
		IRF522 IRF523	–	0.30	0.40	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.5	2.9	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 4.0A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	200	400	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	50	100	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 4.0A, Z_0 = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	35	70	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	35	70	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	10	15	nC	V_{GS} = 15V, I_D = 10A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	4.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF520 IRF521	–	–	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF522 IRF523	–	–	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF520 IRF521	–	–	32	A	
		IRF522 IRF523	–	–	28	A	
V_{SD}	Diode Forward Voltage ②	IRF520 IRF521	–	–	2.5	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
		IRF522 IRF523	–	–	2.3	V	T_C = 25°C, I_S = 7.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	280	–	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	1.6	–	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

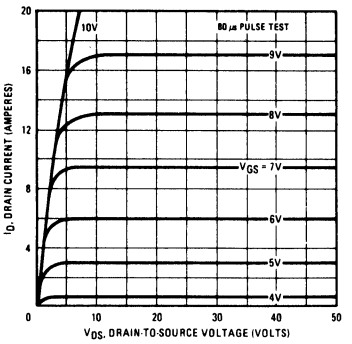


Fig. 1 – Typical Output Characteristics

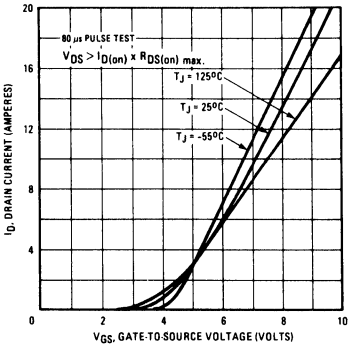


Fig. 2 – Typical Transfer Characteristics

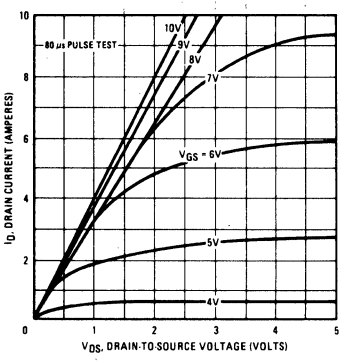


Fig. 3 – Typical Saturation Characteristics

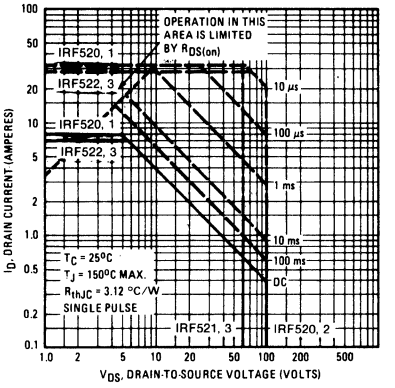


Fig. 4 – Maximum Safe Operating Area

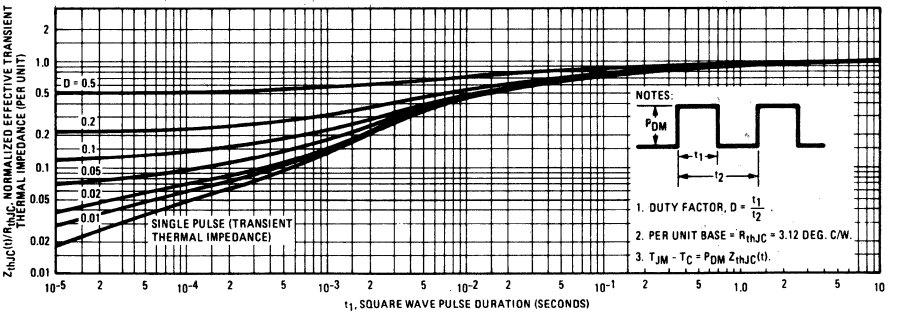


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF520, IRF521, IRF522, IRF523

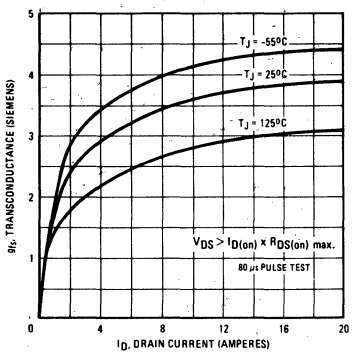


Fig. 6 – Typical Transconductance Vs. Drain Current

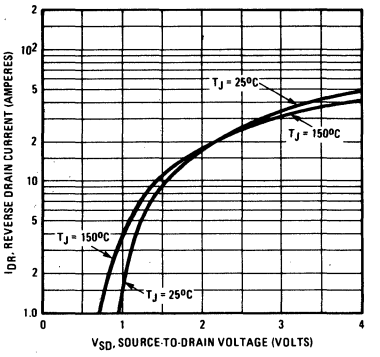


Fig. 7 – Typical Source-Drain Diode Forward Voltage

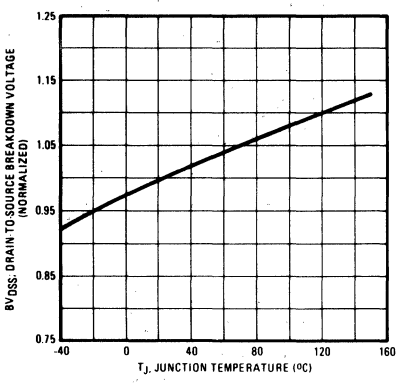


Fig. 8 – Breakdown Voltage Vs. Temperature

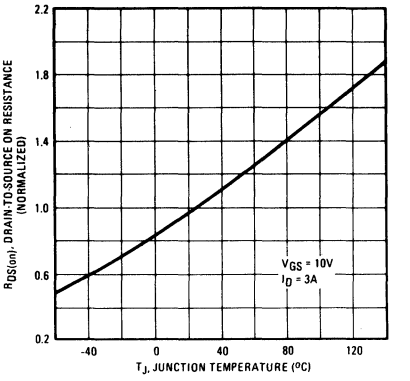


Fig. 9 – Normalized On-Resistance Vs. Temperature

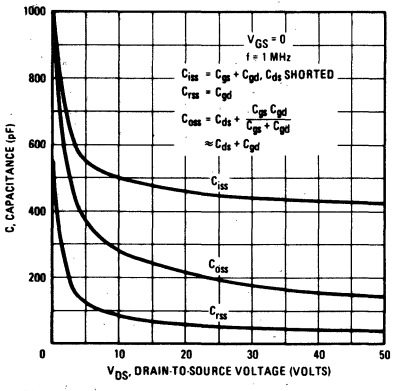


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

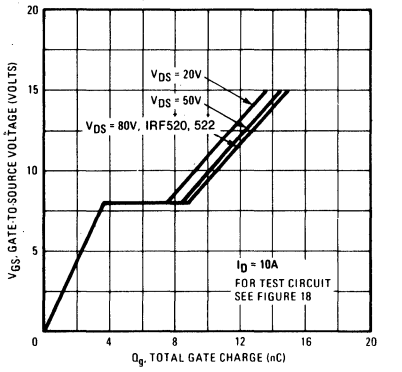


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

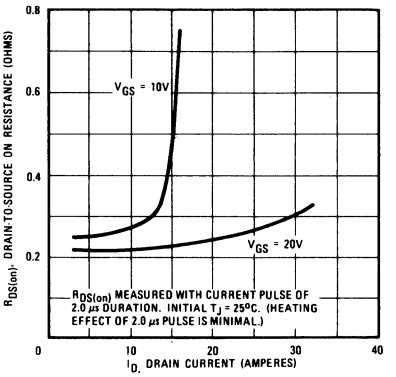


Fig. 12 – Typical On-Resistance Vs. Drain Current

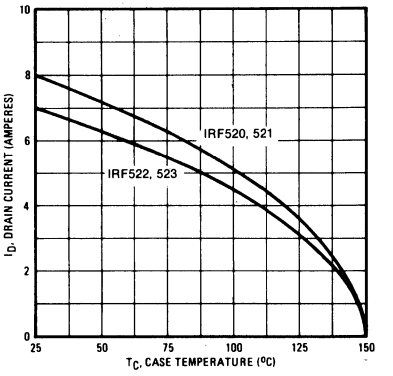


Fig. 13 – Maximum Drain Current Vs. Case Temperature

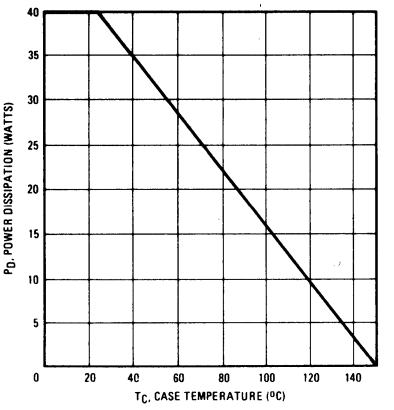


Fig. 14 – Power Vs. Temperature Derating Curve

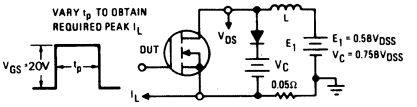


Fig. 15 – Clamped Inductive Test Circuit

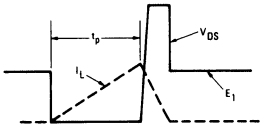


Fig. 16 – Clamped Inductive Waveforms

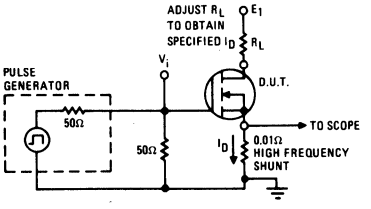


Fig. 17 – Switching Time Test Circuit

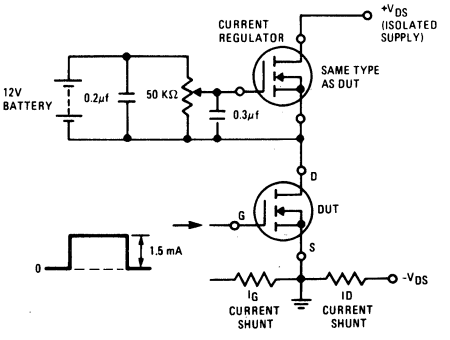


Fig. 18 – Gate Charge Test Circuit

IRF530, IRF531, IRF532, IRF533

File Number **1575**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

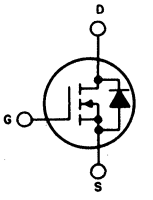
12A and 14A, 60V-100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



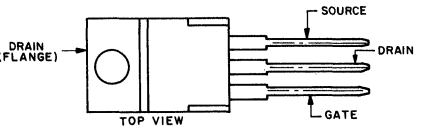
92CS-33741

TERMINAL DIAGRAM

The IRF530, IRF531, IRF532 and IRF533 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

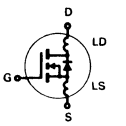
Absolute Maximum Ratings

Parameter		IRF530	IRF531	IRF532	IRF533	Units
V_{DS}	Drain - Source Voltage ①	100	60	100	60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100	60	100	60	V
I_D @ T_C = 25°C	Continuous Drain Current	14	14	12	12	A
I_D @ T_C = 100°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_{DM}	Pulsed Drain Current ③	56	56	48	48	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		56	56	48	48	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF530 IRF532	100	–	–	V	V_{GS} = 0V
		IRF531 IRF533	60	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF530 IRF531	14	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF532 IRF533	12	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF530 IRF531	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 8.0A
		IRF532 IRF533	–	0.20	0.25	Ω	
g_{fs}	Forward Transconductance ②	ALL	4.0	5.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 8.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	300	500	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	100	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 36V, I_D = 8.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	75	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40	ns	
t_f	Fall Time	ALL	–	–	45	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	9.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

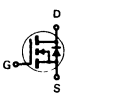


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF530 IRF531	–	–	14	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF532 IRF533	–	–	12	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF530 IRF531	–	–	56	A	
		IRF532 IRF533	–	–	48	A	
V_{SD}	Diode Forward Voltage ②	IRF530 IRF531	–	–	2.5	V	T_C = 25°C, I_S = 14A, V_{GS} = 0V
		IRF532 IRF533	–	–	2.3	V	T_C = 25°C, I_S = 12A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	360	–	ns	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.1	–	μC	T_J = 150°C, I_F = 14A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF530, IRF531, IRF532, IRF533

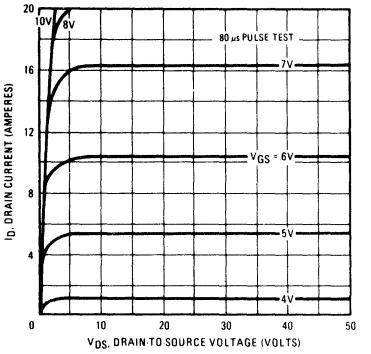


Fig. 1 – Typical Output Characteristics

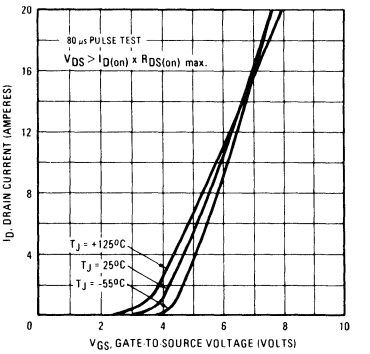


Fig. 2 – Typical Transfer Characteristics

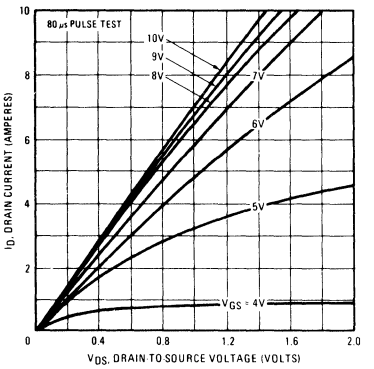


Fig. 3 – Typical Saturation Characteristics

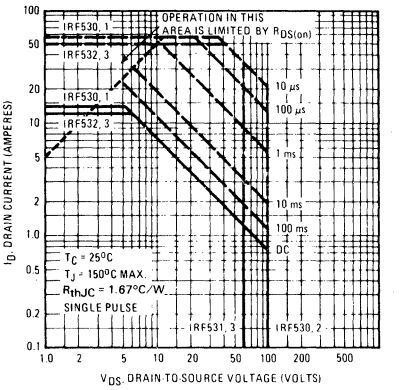


Fig. 4 – Maximum Safe Operating Area

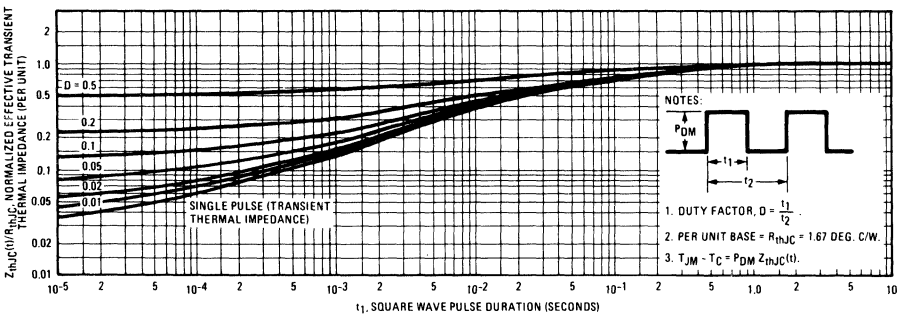


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

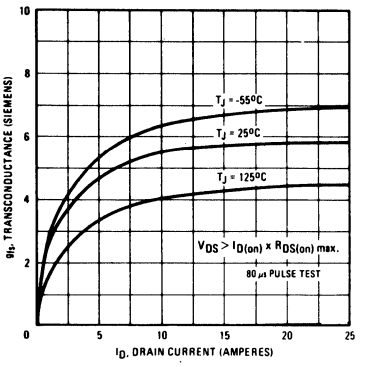


Fig. 6 – Typical Transconductance Vs. Drain Current

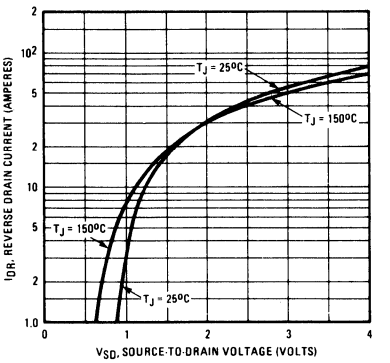


Fig. 7 – Typical Source-Drain Diode Forward Voltage

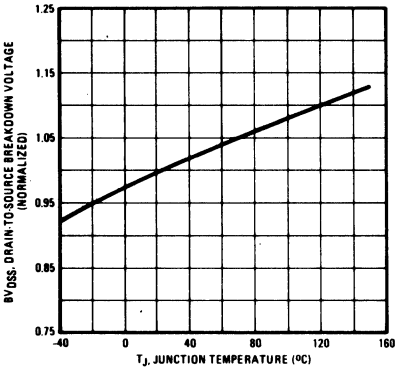


Fig. 8 – Breakdown Voltage Vs. Temperature

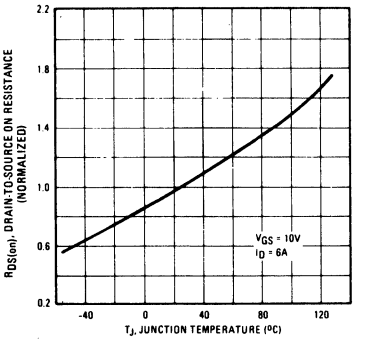


Fig. 9 – Normalized On-Resistance Vs. Temperature

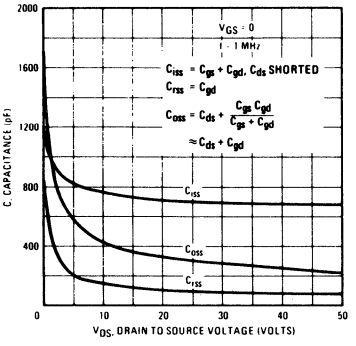


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

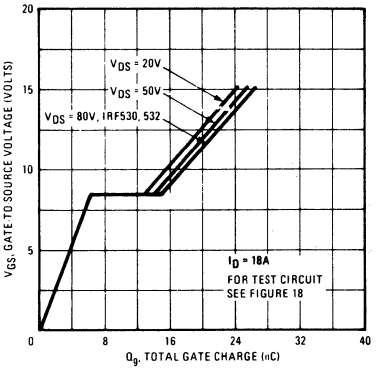


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF530, IRF531, IRF532, IRF533

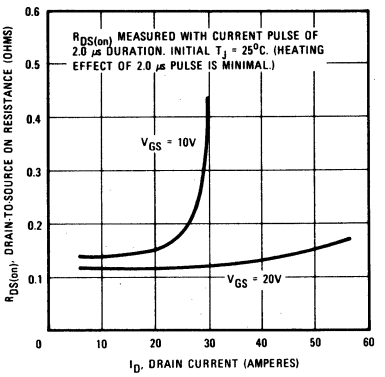


Fig. 12 – Typical On-Resistance Vs. Drain Current

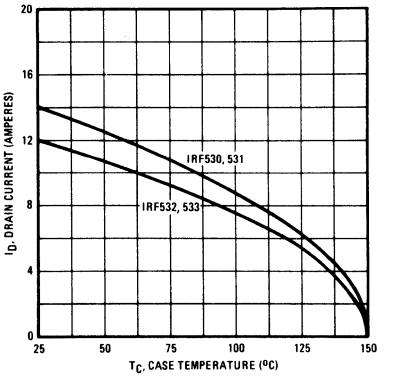


Fig. 13 – Maximum Drain Current Vs. Case Temperature

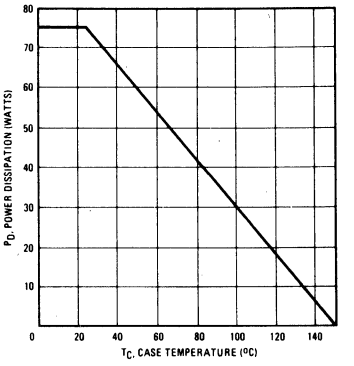


Fig. 14 – Power Vs. Temperature Derating Curve

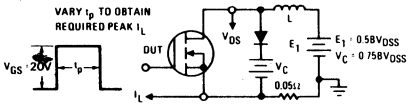


Fig. 15 – Clamped Inductive Test Circuit

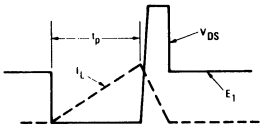


Fig. 16 – Clamped Inductive Waveforms

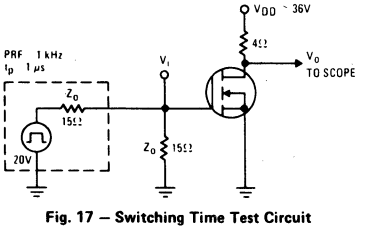


Fig. 17 – Switching Time Test Circuit

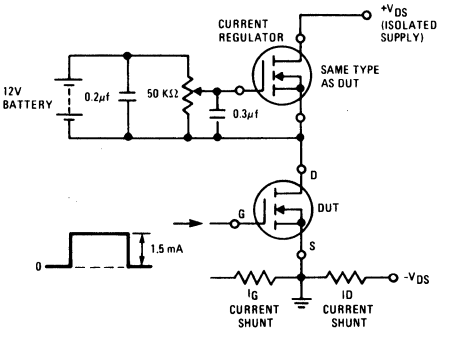


Fig. 18 – Gate Charge Test Circuit

File Number **1576**

IRF610, IRF611, IRF612, IRF613

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

2.0A and 2.5A, 150V-200V

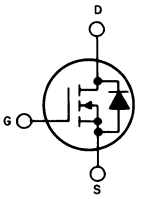
$r_{DS}(on)$ = 1.5 Ω and 2.4 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF610, IRF611, IRF612 and IRF613 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

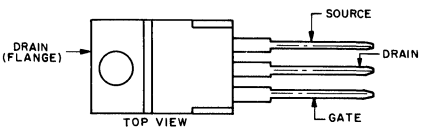
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

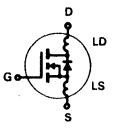
Parameter		IRF610	IRF611	IRF612	IRF613	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	**Drain - Gate Voltage (R_{GS} = 20 KΩ)** ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C 100°C	Continuous Drain Current	1.5	1.5	1.25	1.25	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	20 (See Fig. 14)				W
	Linear Derating Factor	0.16 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF610, IRF611, IRF612, IRF613

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF610 IRF612	200	–	–	V	V_{GS} = 0V
		IRF611 IRF613	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF610 IRF611	2.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF612 IRF613	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF610 IRF611	–	1.0	1.5	Ω	V_{GS} = 10V, I_D = 1.25A
		IRF612 IRF613	–	1.5	2.4	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.8	1.3	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.25A
C_{iss}	Input Capacitance	ALL	–	135	150	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	60	80	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	16	25	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	8.0	15	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.25A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	15	25	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	10	15	ns	
t_f	Fall Time	ALL	–	8.0	15	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL		5.0	7.5	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL		2.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL		3.0	–	nC	
L_D	Internal Drain Inductance	ALL		3.5		nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.

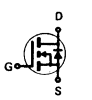


Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	6.4	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF610 IRF611			2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF612 IRF613			2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF610 IRF611			10	A	
		IRF612 IRF613			8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF610 IRF611			2.0	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF612 IRF613			1.8	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL		290		ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL		2.0		μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

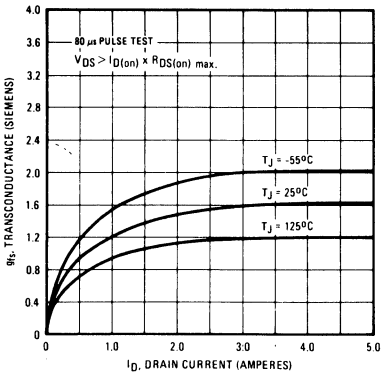


Fig. 6 — Typical Transconductance Vs. Drain Current

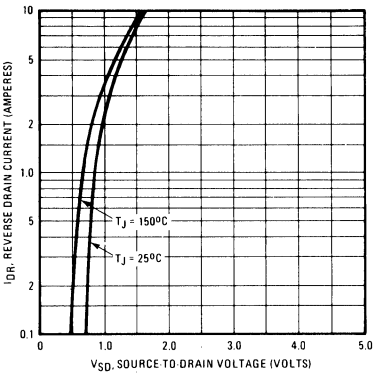


Fig. 7 — Typical Source-Drain Diode Forward Voltage

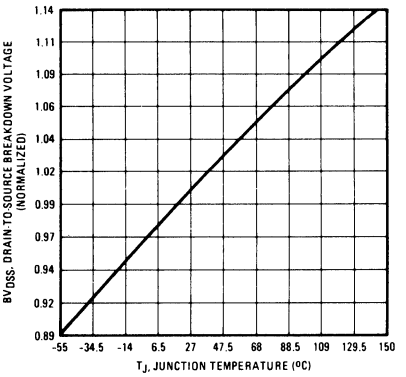


Fig. 8 — Breakdown Voltage Vs. Temperature

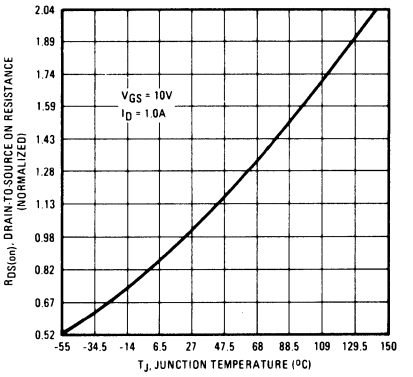


Fig. 9 — Normalized On-Resistance Vs. Temperature

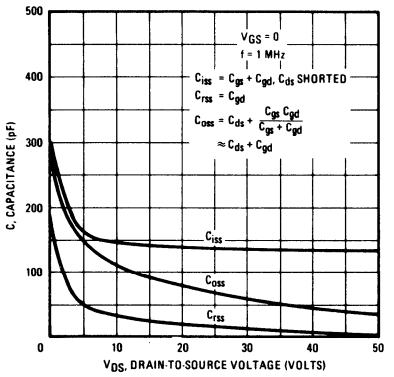


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

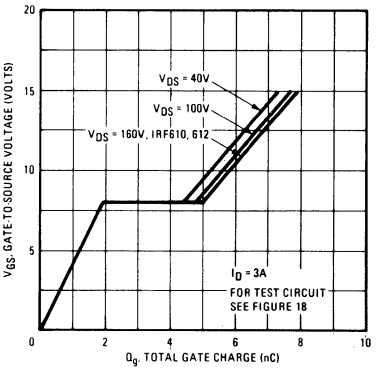


Fig. 11 — Typical Gate Charge Vs. Gate-to-Source Voltage

IRF610, IRF611, IRF612, IRF613

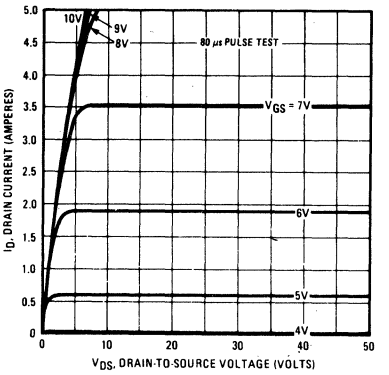


Fig. 1 – Typical Output Characteristics

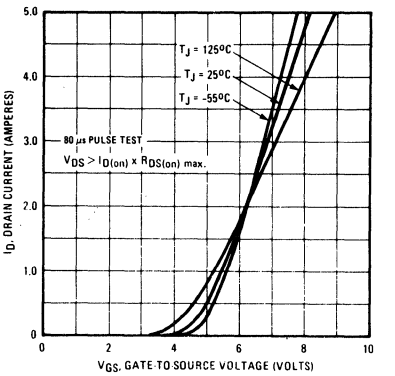


Fig. 2 – Typical Transfer Characteristics

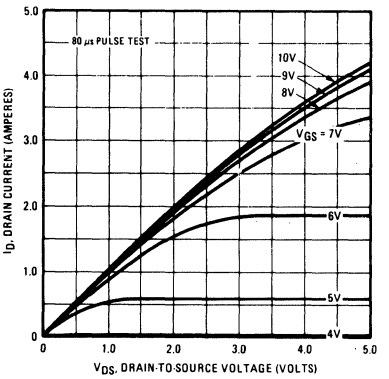


Fig. 3 – Typical Saturation Characteristics

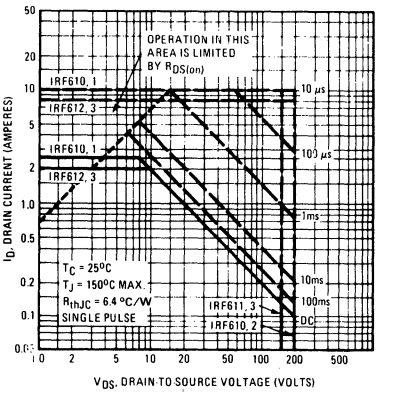


Fig. 4 – Maximum Safe Operating Area

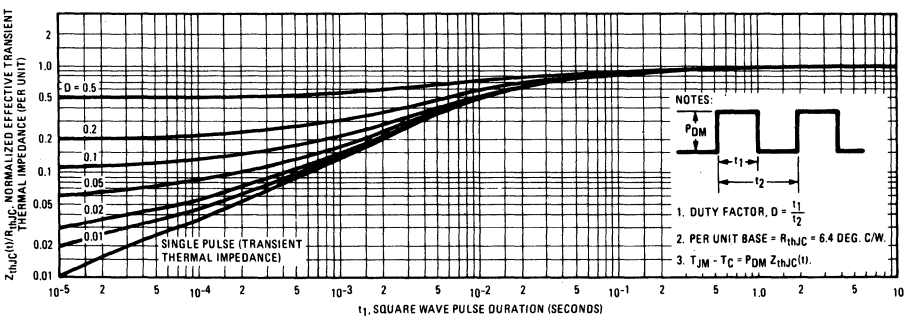


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

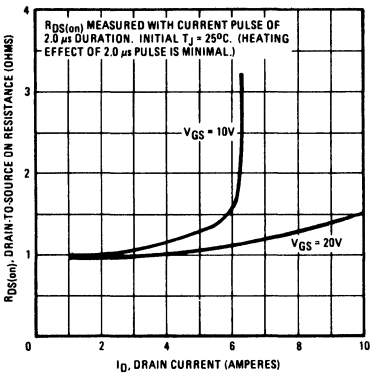


Fig. 12 – Typical On-Resistance Vs. Drain Current

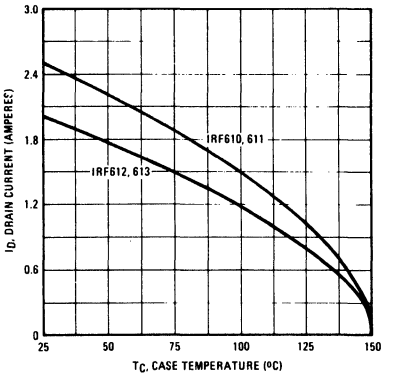


Fig. 13 – Maximum Drain Current Vs. Case Temperature

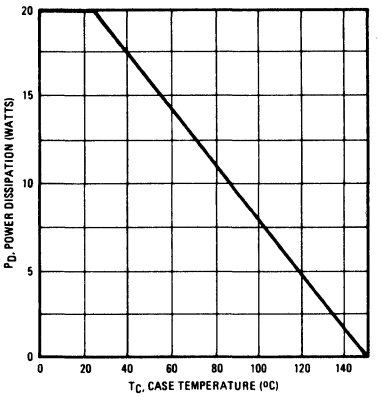


Fig. 14 – Power Vs. Temperature Derating Curve

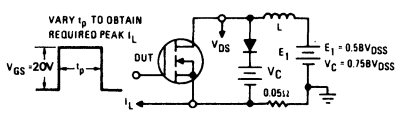


Fig. 15 – Clamped Inductive Test Circuit

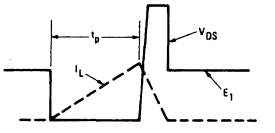


Fig. 16 – Clamped Inductive Waveforms

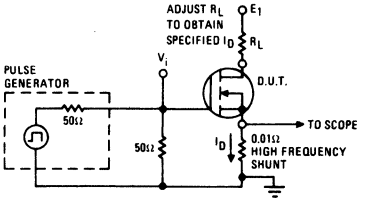


Fig. 17 – Switching Time Test Circuit

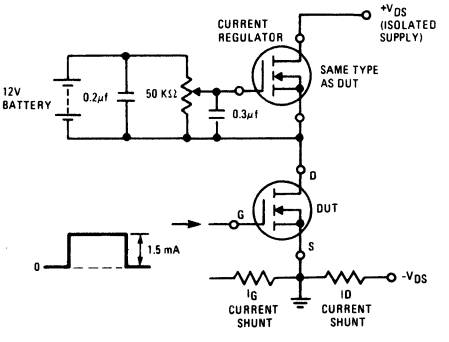


Fig. 18 – Gate Charge Test Circuit

IRF620, IRF621, IRF622, IRF623

File Number **1577**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

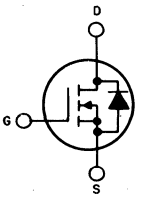
4.0A and 5.0A, 150V-200V

$r_{DS}(on)$ = 0.8 Ω and 1.2 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



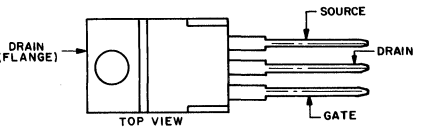
92CS-33741

TERMINAL DIAGRAM

The IRF620, IRF621, IRF622 and IRF623 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

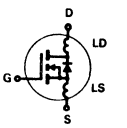
Absolute Maximum Ratings

Parameter		IRF620	IRF621	IRF622	IRF623	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	5.0	5.0	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	20	20	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		20	20	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF620 IRF622	200	–	–	V	V_{GS} = 0V
		IRF621 IRF623	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF620 IRF621	5.0	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF622 IRF623	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF620 IRF621	–	0.5	0.8	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF622 IRF623	–	0.8	1.2	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.3	2.5	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 2.5 BV_{DSS}, I_D = 2.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	30	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 50V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF620 IRF621	–	–	5.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF622 IRF623	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF620 IRF621	–	–	20	A	
		IRF622 IRF623	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF620 IRF621	–	–	1.8	V	T_C = 25°C, I_S = 5.0A, V_{GS} = 0V
		IRF622 IRF623	–	–	1.4	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	350	–	ns	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	2.3	–	μC	T_J = 150°C, I_F = 5.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF620, IRF621, IRF622, IRF623

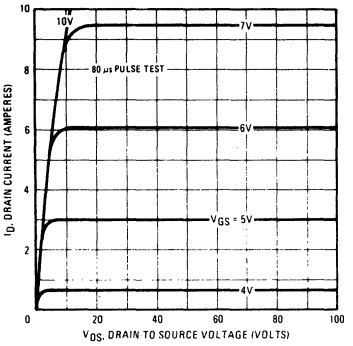


Fig. 1 – Typical Output Characteristics

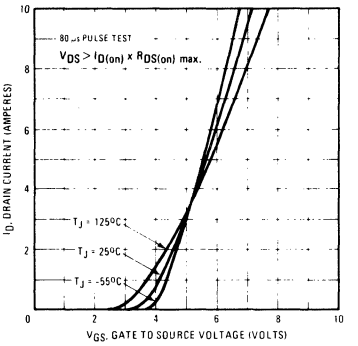


Fig. 2 – Typical Transfer Characteristics

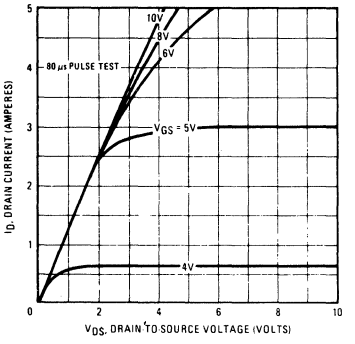


Fig. 3 – Typical Saturation Characteristics

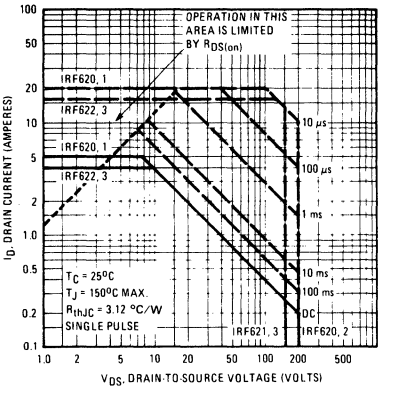


Fig. 4 – Maximum Safe Operating Area

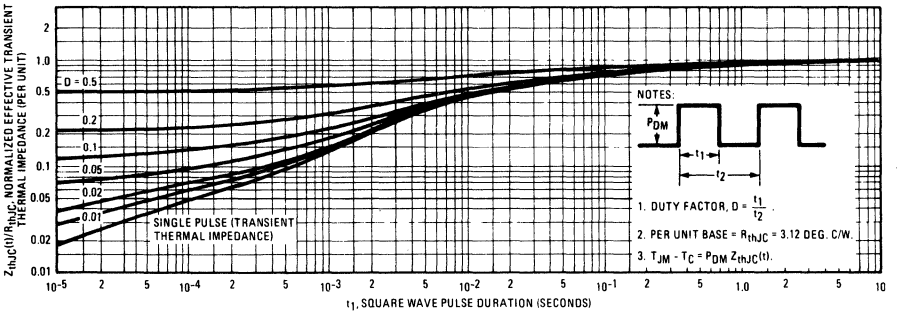


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

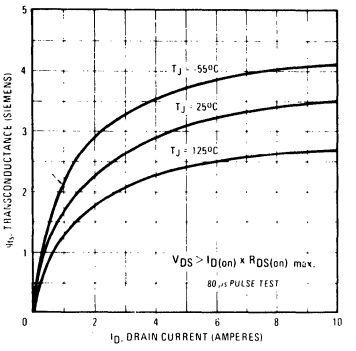


Fig. 6 – Typical Transconductance Vs. Drain Current

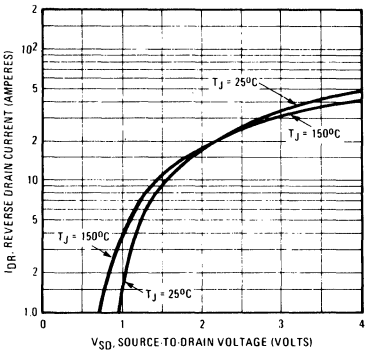


Fig. 7 – Typical Source-Drain Diode Forward Voltage

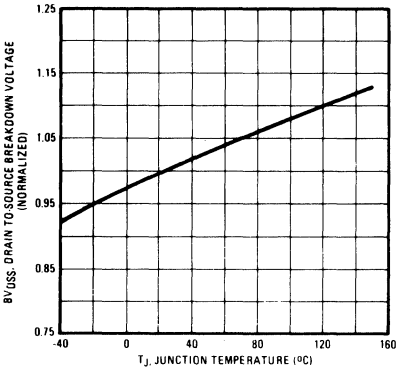


Fig. 8 – Breakdown Voltage Vs. Temperature

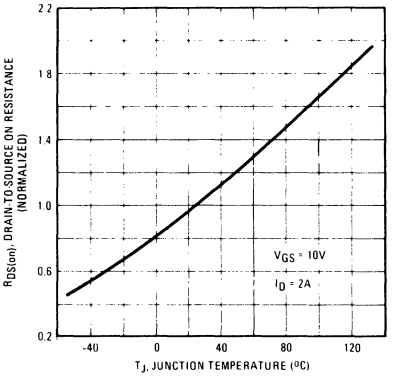


Fig. 9 – Normalized On-Resistance Vs. Temperature

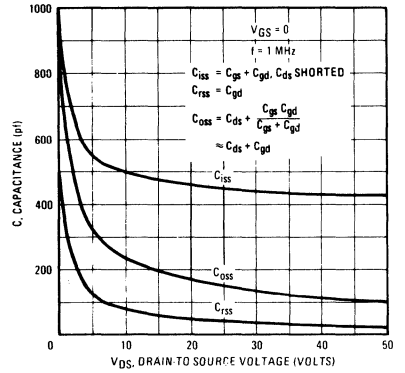


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

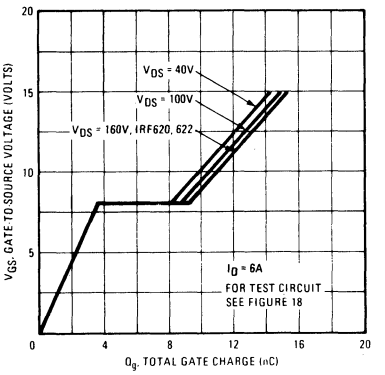


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF620, IRF621, IRF622, IRF623

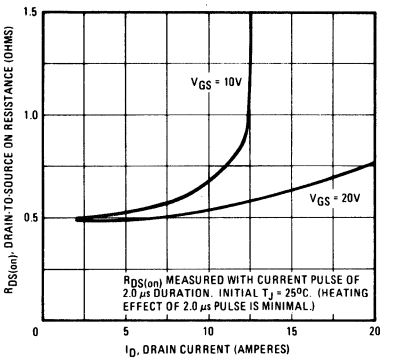


Fig. 12 – Typical On-Resistance Vs. Drain Current

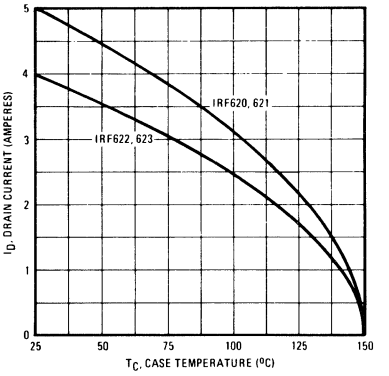


Fig. 13 – Maximum Drain Current Vs. Case Temperature

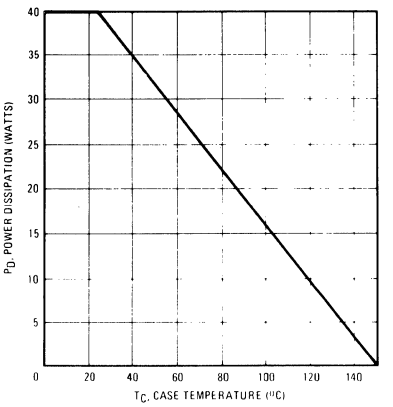


Fig. 14 – Power Vs. Temperature Derating Curve

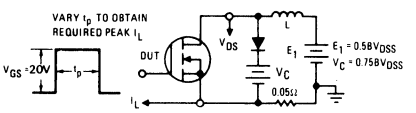


Fig. 15 – Clamped Inductive Test Circuit

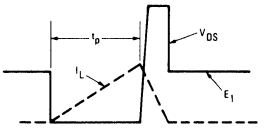


Fig. 16 – Clamped Inductive Waveforms

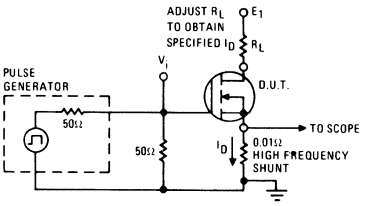


Fig. 17 – Switching Time Test Circuit

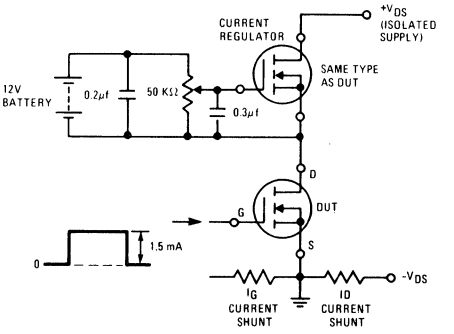


Fig. 18 – Gate Charge Test Circuit

File Number **1578**

IRF630, IRF631, IRF632, IRF633

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8.0A and 9.0A, 150V-200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

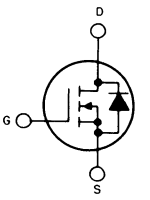
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The IRF630, IRF631, IRF632 and IRF633 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

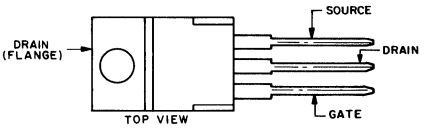
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

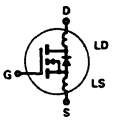
Parameter		IRF630	IRF631	IRF632	IRF633	Units
V_{DS}	Drain - Source Voltage ①	200	150	200	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	200	150	200	150	V
I_D @ T_C = 25°C	Continuous Drain Current	9.0	9.0	8.0	8.0	A
I_D @ T_C = 100°C	Continuous Drain Current	6.0	6.0	5.0	5.0	A
I_{DM}	Pulsed Drain Current ③	36	36	32	32	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		36	36	32	32	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF630, IRF631, IRF632, IRF633

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF630, IRF632	200	–	–	V	V_{GS} = 0V
		IRF631, IRF633	150	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF630, IRF631	9.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF632, IRF633	8.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF630, IRF631	–	0.25	0.4	Ω	V_{GS} = 10V, I_D = 5.0A
		IRF632, IRF633	–	0.4	0.6	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.8		S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 5.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	250	450	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	80	150	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 90V, I_D = 5.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50	ns	
t_f	Fall Time	ALL	–	–	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	19	30	nC	V_{GS} = 10V, I_D = 12A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	10	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	9.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF630, IRF631	–	–	9.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF632, IRF633	–	–	8.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF630, IRF631	–	–	36	A	
		IRF632, IRF633	–	–	32	A	
V_{SD}	Diode Forward Voltage ②	IRF630, IRF631	–	–	2.0	V	T_C = 25°C, I_S = 9.0A, V_{GS} = 0V
		IRF632, IRF633	–	–	1.8	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.0	–	μC	T_J = 150°C, I_F = 9.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

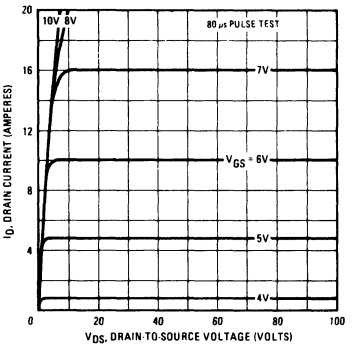


Fig. 1 – Typical Output Characteristics

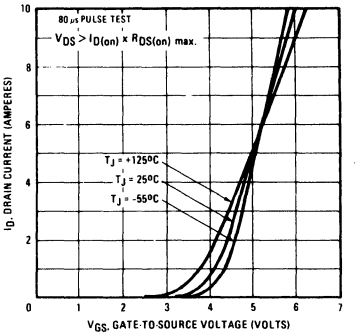


Fig. 2 – Typical Transfer Characteristics

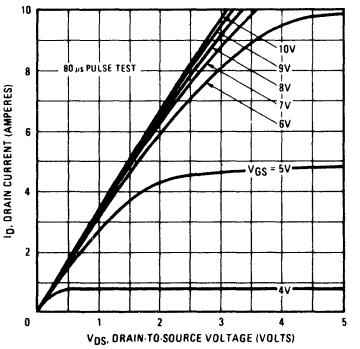


Fig. 3 – Typical Saturation Characteristics

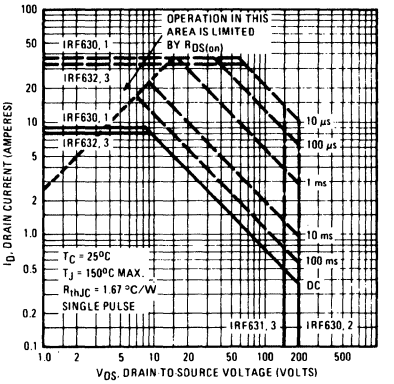


Fig. 4 – Maximum Safe Operating Area

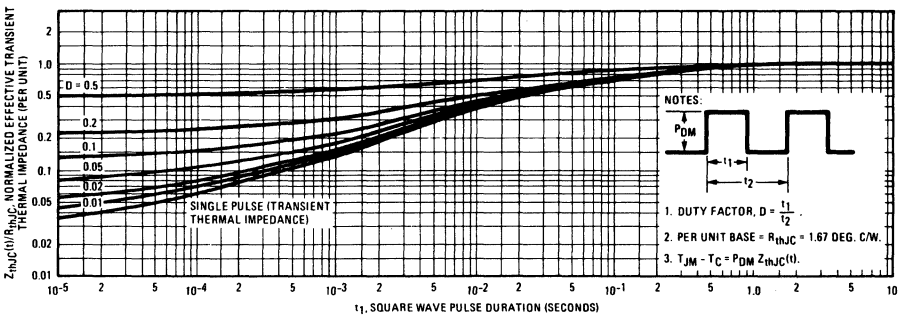


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

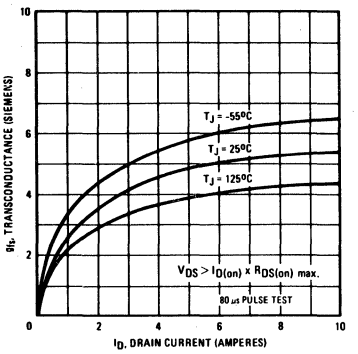


Fig. 6 – Typical Transconductance Vs. Drain Current

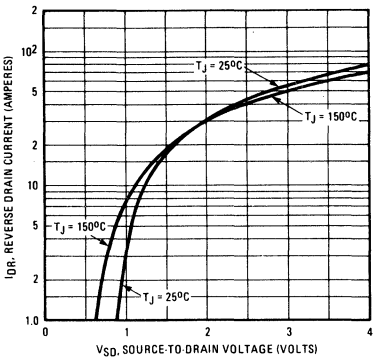


Fig. 7 – Typical Source-Drain Diode Forward Voltage

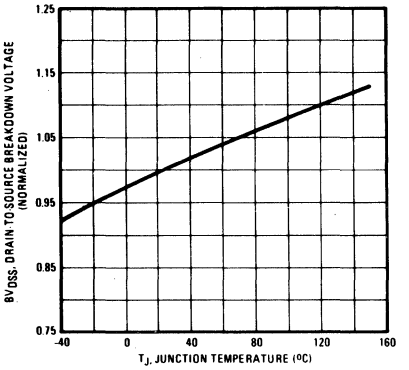


Fig. 8 – Breakdown Voltage Vs. Temperature

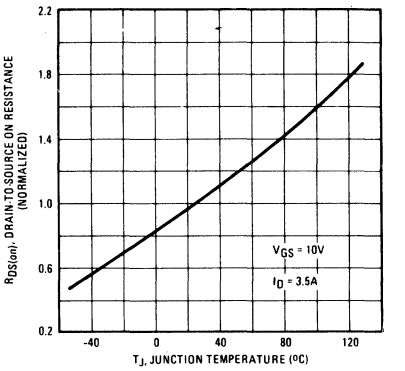


Fig. 9 – Normalized On-Resistance Vs. Temperature

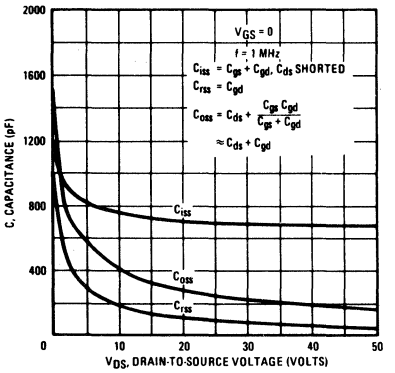


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

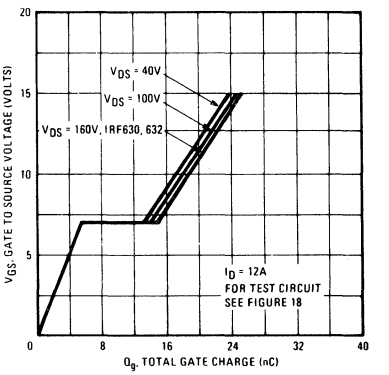


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

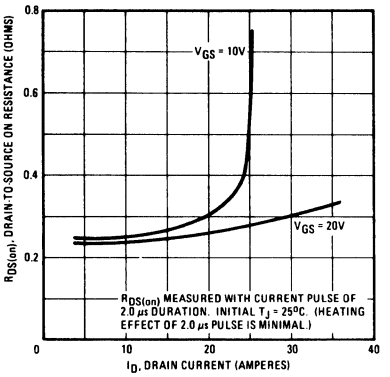


Fig. 12 – Typical On-Resistance Vs. Drain Current

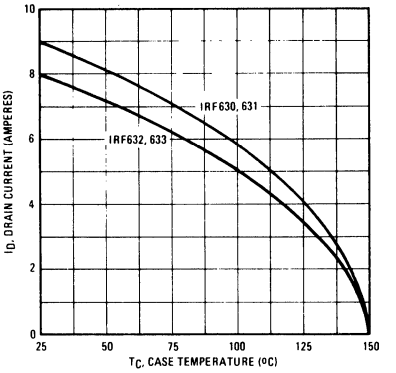


Fig. 13 – Maximum Drain Current Vs. Case Temperature

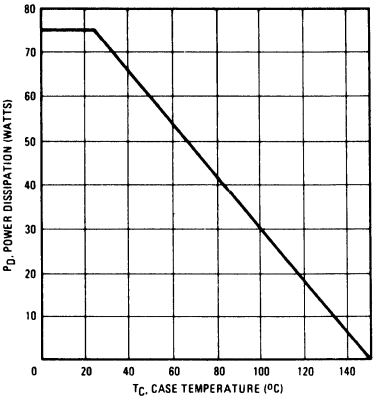


Fig. 14 – Power Vs. Temperature Derating Curve

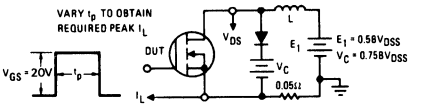


Fig. 15 – Clamped Inductive Test Circuit

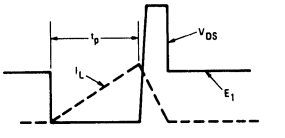


Fig. 16 – Clamped Inductive Waveforms

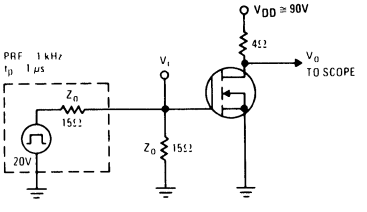


Fig. 17 – Switching Time Test Circuit

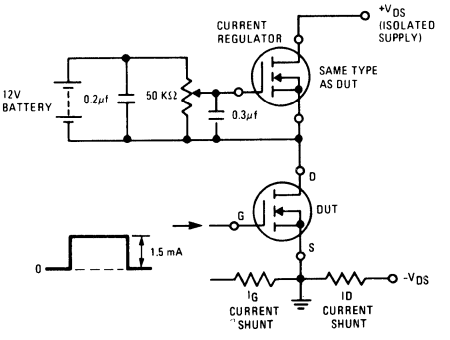


Fig. 18 – Gate Charge Test Circuit

IRF641, IRF643

File Number **1585**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

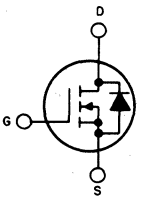
16A and 18A, 150V

$r_{DS}(on)$ = 0.18 Ω and 0.22 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

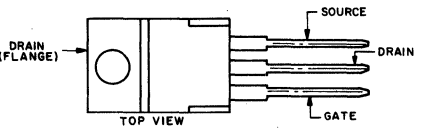
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF641 and IRF643 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

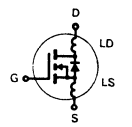
Absolute Maximum Ratings

Parameter		IRF641	IRF643	Units
V_{DS}	Drain - Source Voltage ①	150	150	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	150	150	V
I_D @ T_C = 25°C	Continuous Drain Current	18	16	A
I_D @ T_C = 100°C	Continuous Drain Current	11	10	A
I_{DM}	Pulsed Drain Current ③	72	64	A
V_{GS}	Gate - Source Voltage	±20		V
P_D @ T_C = 25°C	Max. Power Dissipation	125 (See Fig. 14)		W
	Linear Derating Factor	1.0 (See Fig. 14)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH 72 | 72 | 64 | 64		A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 100		°C
	Lead Temperature	300 (0.064 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF641 IRF643	150	–	–	V	V_{GS} = 0V I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF641	18	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., V_{GS} = 10V
		IRF643	16	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF641	–	0.14	0.18	Ω	V_{GS} = 10V, I_D = 10A
		IRF643	–	0.20	0.22	Ω	
g_{fs}	Forward Transconductance ②	ALL	6.0	10	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = 10A
C_{iss}	Input Capacitance	ALL	–	1275	1600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	500	750	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	160	300	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	16	30	ns	V_{DD} = 75V, I_D = 10A, Z_o = 4.7Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	27	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	40	80	ns	
t_f	Fall Time	ALL	–	31	60	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	43	60	nC	V_{GS} = 10V, I_D = 22A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	16	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	27	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.0	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF641	–	–	18	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF643	–	–	16	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF641	–	–	72	A	
		IRF643	–	–	64	A	
V_{SD}	Diode Forward Voltage ②	IRF641	–	–	2.0	V	T_C = 25°C, I_S = 18A, V_{GS} = 0V
		IRF643	–	–	1.9	V	T_C = 25°C, I_S = 16A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.1	–	μC	T_J = 150°C, I_F = 18A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature.
See Transient Thermal Impedance Curve (Fig. 5).

IRF641, IRF643

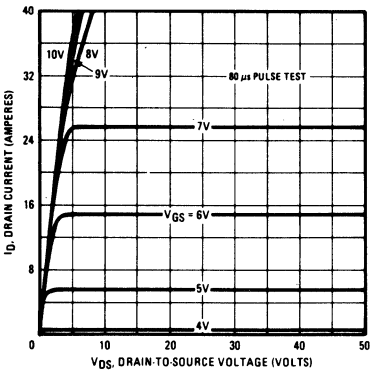


Fig. 1 – Typical Output Characteristics

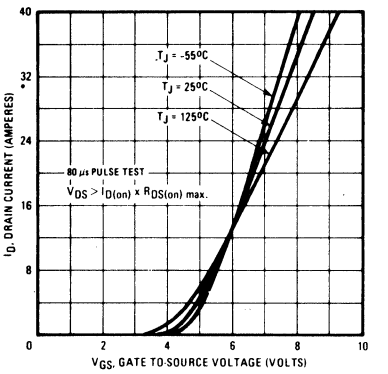


Fig. 2 – Typical Transfer Characteristics

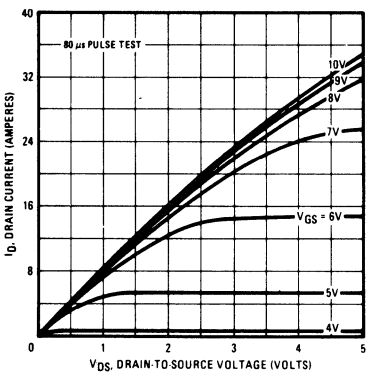


Fig. 3 – Typical Saturation Characteristics

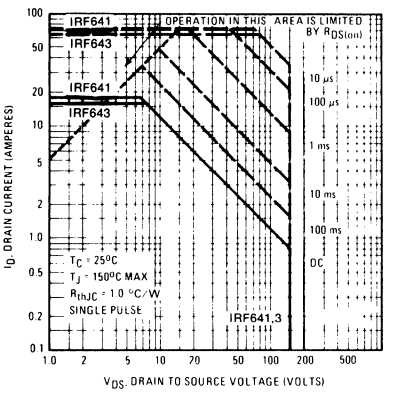


Fig. 4 – Maximum Safe Operating Area

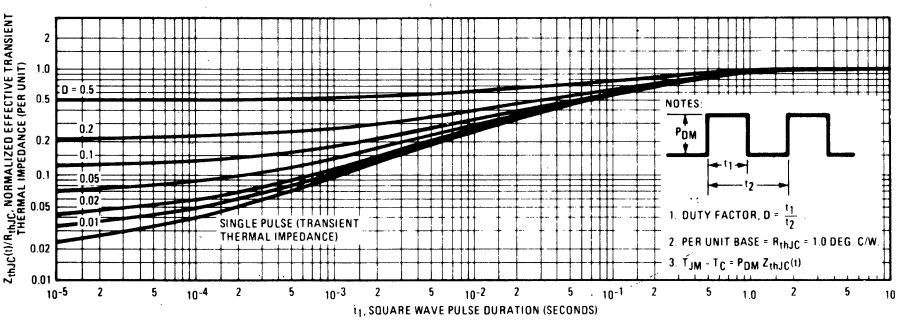


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

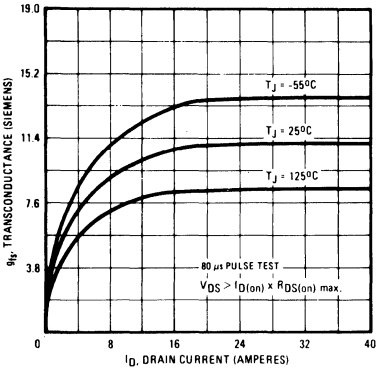


Fig. 6 – Typical Transconductance Vs. Drain Current

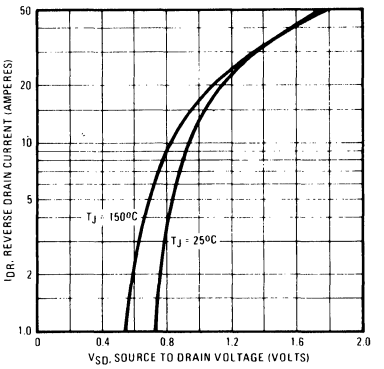


Fig. 7 – Typical Source-Drain Diode Forward Voltage

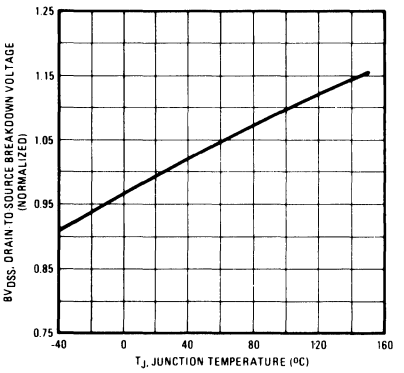


Fig. 8 – Breakdown Voltage Vs. Temperature

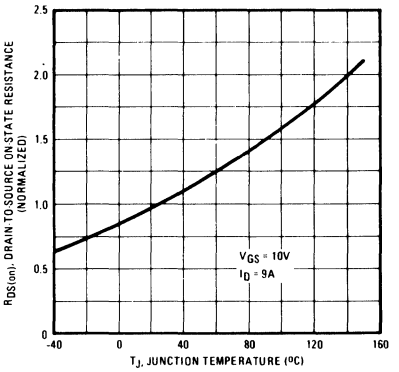


Fig. 9 – Normalized On-Resistance Vs. Temperature

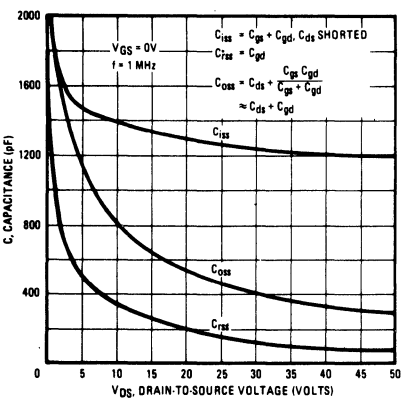


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

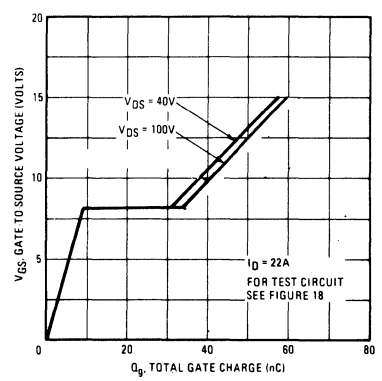


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

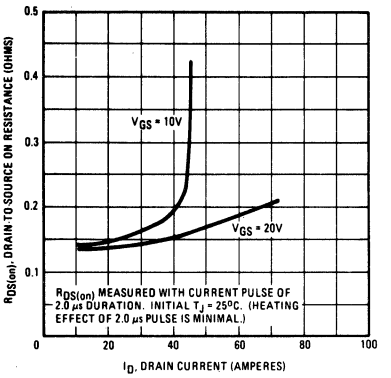


Fig. 12 – Typical On-Resistance Vs. Drain Current

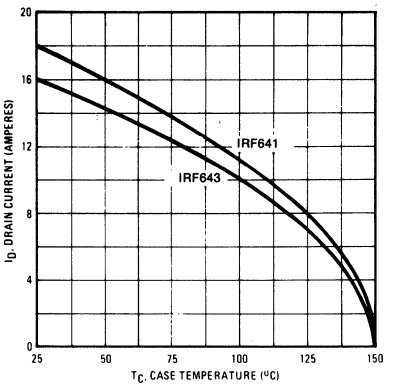


Fig. 13 – Maximum Drain Current Vs. Case Temperature

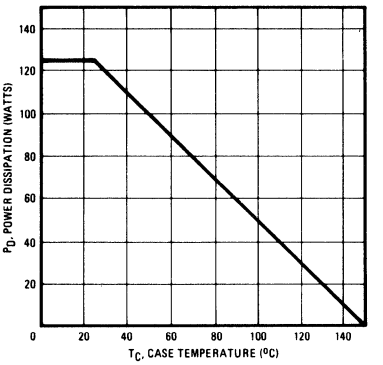


Fig. 14 – Power Vs. Temperature Derating Curve

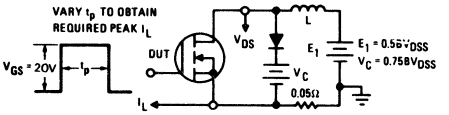


Fig. 15 – Clamped Inductive Test Circuit

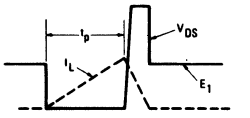


Fig. 16 – Clamped Inductive Waveforms

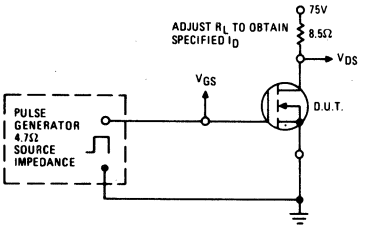


Fig. 17 – Switching Time Test Circuit

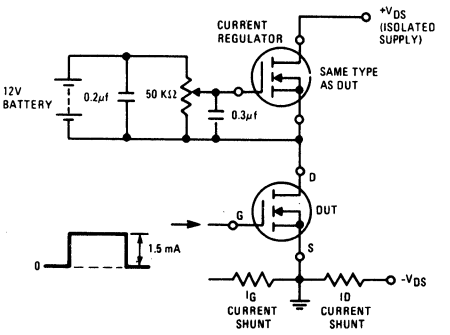


Fig. 18 – Gate Charge Test Circuit

File Number **1579**

IRF720, IRF721, IRF722, IRF723

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

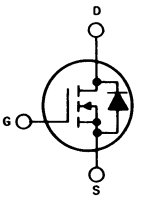
2.5A and 3.0A, 350V-400V

$r_{DS}(on)$ = 1.8 Ω and 2.5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



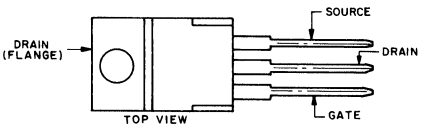
92CS-33741

TERMINAL DIAGRAM

The IRF720, IRF721, IRF722 and IRF723 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

Absolute Maximum Ratings

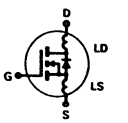
Parameter		IRF720	IRF721	IRF722	IRF723	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_D @ T_C = 100°C	Continuous Drain Current	2.0	2.0	1.5	1.5	A
I_{DM}	Pulsed Drain Current ③	12	12	10	10	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		12	12	10	10	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF720, IRF721, IRF722, IRF723

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF720 IRF722	400	–	–	V	V_{GS} = 0V
		IRF721 IRF723	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF720 IRF721	3.0	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF722 IRF723	2.5	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF720 IRF721	–	1.5	1.8	Ω	V_{GS} = 10V, I_D = 1.5A
		IRF722 IRF723	–	1.8	2.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	2.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 1.5A
C_{iss}	Input Capacitance	ALL	–	450	600	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	20	40	ns	V_{DD} = 0.5 BV_{DSS}, I_D = 1.5A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	50	100	ns	
t_f	Fall Time	ALL	–	25	50	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	12	15	nC	V_{GS} = 10V, I_D = 4.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	6.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF720 IRF721	–	–	3.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF722 IRF723	–	–	2.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF720 IRF721	–	–	12	A	
		IRF722 IRF723	–	–	10	A	
V_{SD}	Diode Forward Voltage ②	IRF720 IRF721	–	–	1.6	V	T_C = 25°C, I_S = 3.0A, V_{GS} = 0V
		IRF722 IRF723	–	–	1.5	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	450	–	ns	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.1	–	μC	T_J = 150°C, I_F = 3.0A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

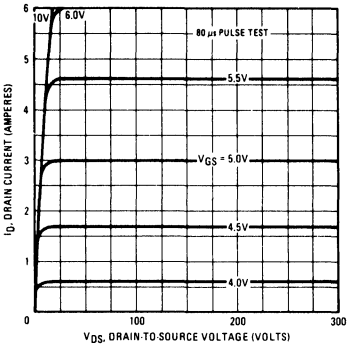


Fig. 1 – Typical Output Characteristics

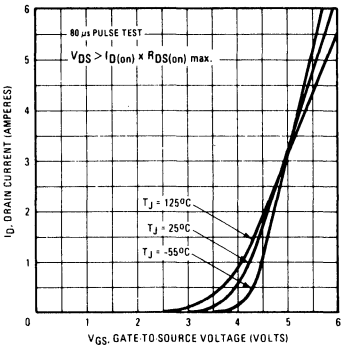


Fig. 2 – Typical Transfer Characteristics

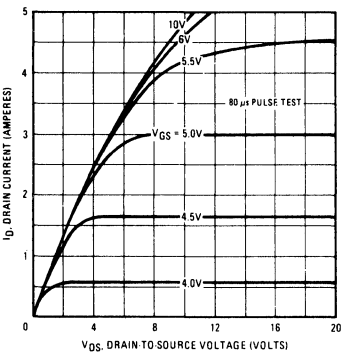


Fig. 3 – Typical Saturation Characteristics

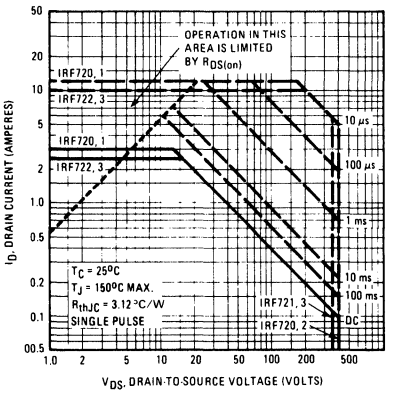


Fig. 4 – Maximum Safe Operating Area

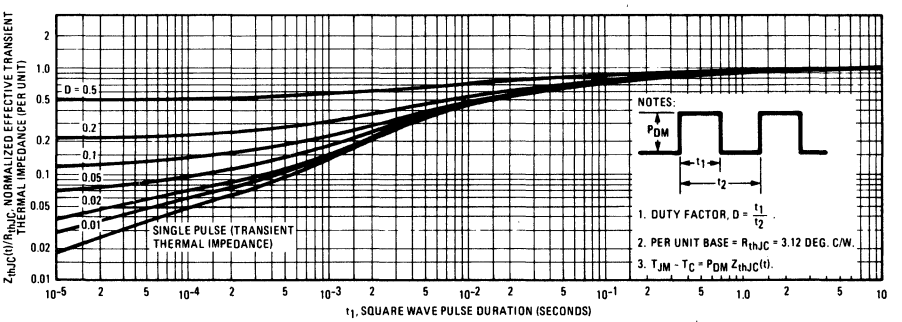


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF720, IRF721, IRF722, IRF723

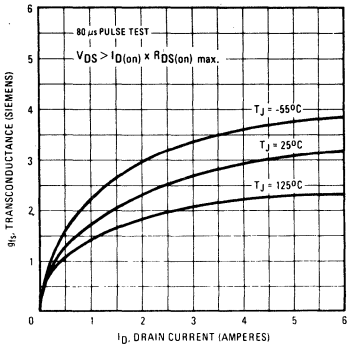


Fig. 6 – Typical Transconductance Vs. Drain Current

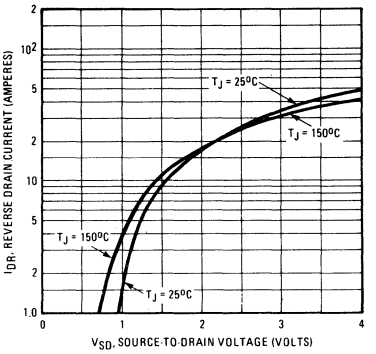


Fig. 7 – Typical Source-Drain Diode Forward Voltage

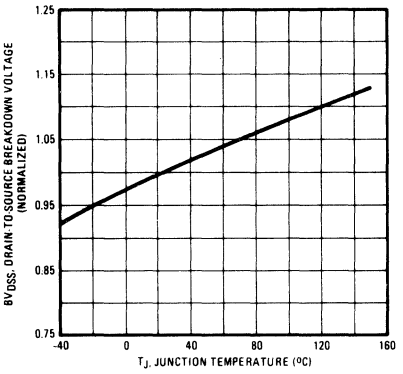


Fig. 8 – Breakdown Voltage Vs. Temperature

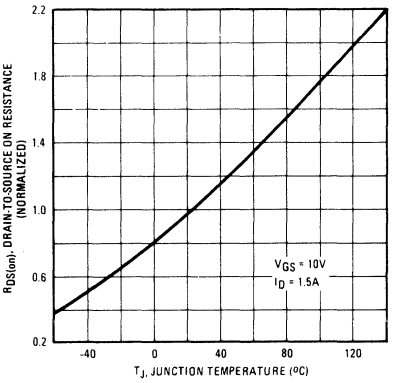


Fig. 9 – Normalized On-Resistance Vs. Temperature

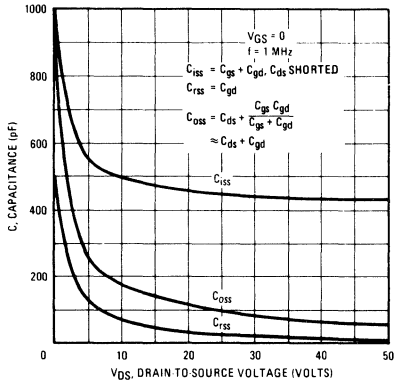


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

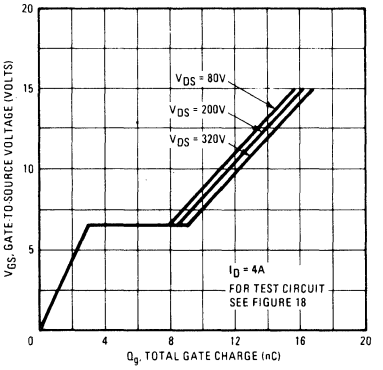


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

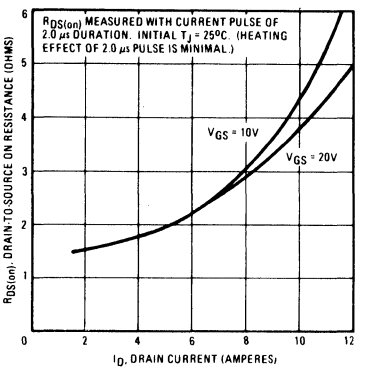


Fig. 12 – Typical On-Resistance Vs. Drain Current

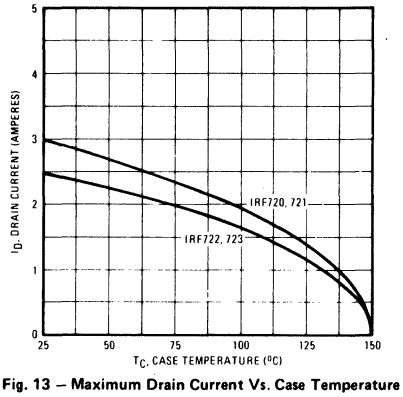


Fig. 13 – Maximum Drain Current Vs. Case Temperature

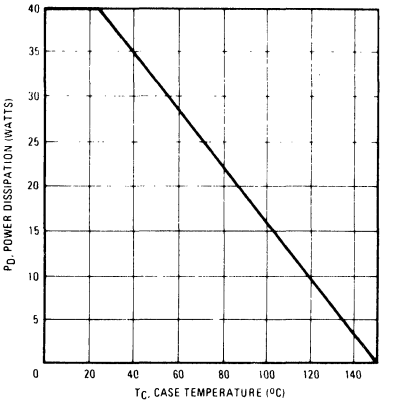


Fig. 14 – Power Vs. Temperature Derating Curve

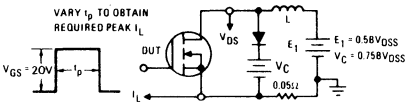


Fig. 15 – Clamped Inductive Test Circuit

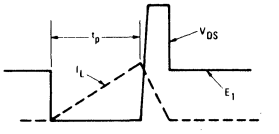


Fig. 16 – Clamped Inductive Waveforms

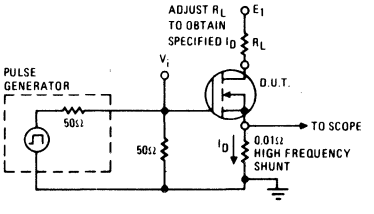


Fig. 17 – Switching Time Test Circuit

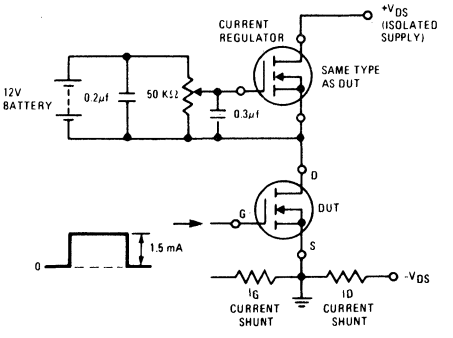


Fig. 18 – Gate Charge Test Circuit

IRF730, IRF731, IRF732, IRF733

File Number **1580**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

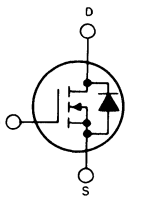
4.5A and 5.5A, 350V-400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



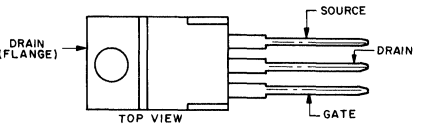
92CS-33741

TERMINAL DIAGRAM

The IRF730, IRF731, IRF732 and IRF733 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

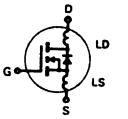
Absolute Maximum Ratings

Parameter		IRF730	IRF731	IRF732	IRF733	Units
V_{DS}	Drain - Source Voltage ①	400	350	400	350	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	400	350	400	350	V
I_D @ T_C = 25°C	Continuous Drain Current	5.5	5.5	4.5	4.5	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5	3.5	3.0	3.0	A
I_{DM}	Pulsed Drain Current ③	22	22	18	18	A
V_{GS}	Gate - Source Voltage	± 20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		22	22	18	18	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF730 IRF732	400	–	–	V	V_{GS} = 0V
		IRF731 IRF733	350	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF730 IRF731	5.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF732 IRF733	4.5	–	--	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF730 IRF731	–	0.8	1.0	Ω	V_{GS} = 10V, I_D = 3.0A
		IRF732 IRF733	–	1.0	1.5	Ω	
g_{fs}	Forward Transconductance ②	ALL	3.0	4.0	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 3.0A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	150	300	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	40	80	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 175V, I_D = 3.0A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	35	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	35	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	18	30	nC	V_{GS} = 10V, I_D = 7.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	7.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF730 IRF731	–	–	5.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF732 IRF733	–	–	4.5	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF730 IRF731	–	–	22	A	
		IRF732 IRF733	–	–	18	A	
V_{SD}	Diode Forward Voltage ②	IRF730 IRF731	–	–	1.6	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0V
		IRF732 IRF733	–	–	1.5	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = 5.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF730, IRF731, IRF732, IRF733

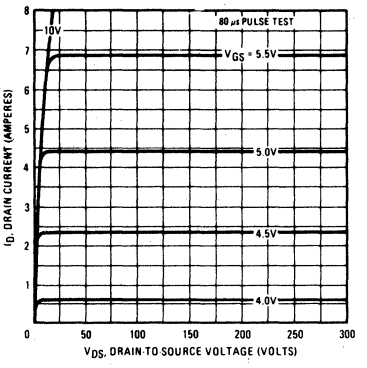


Fig. 1 – Typical Output Characteristics

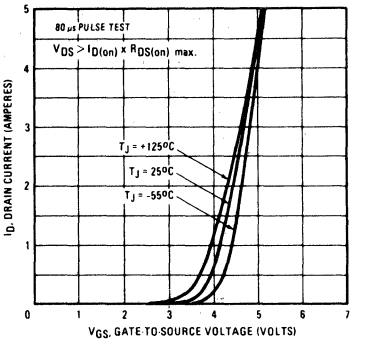


Fig. 2 – Typical Transfer Characteristics

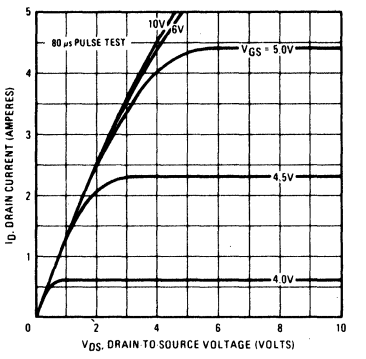


Fig. 3 – Typical Saturation Characteristics

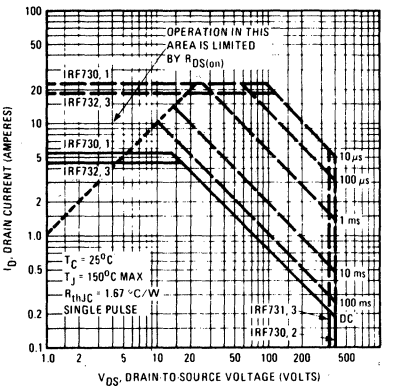


Fig. 4 – Maximum Safe Operating Area

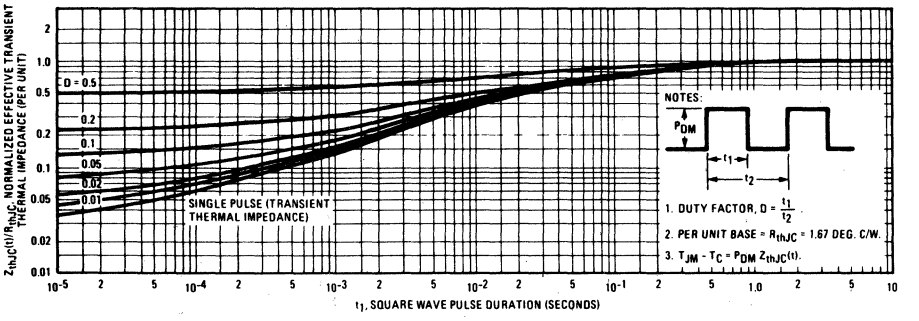


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

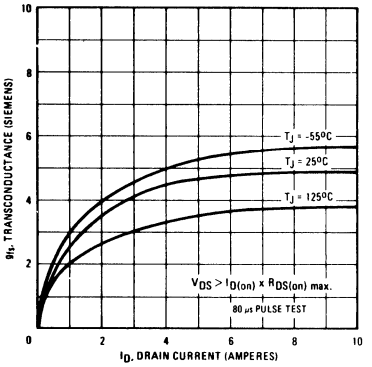


Fig. 6 – Typical Transconductance Vs. Drain Current

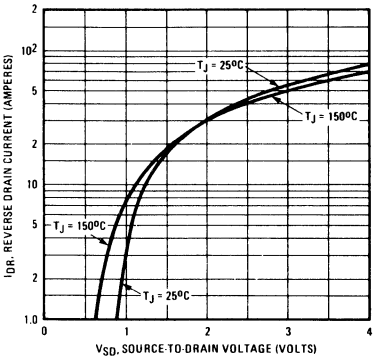


Fig. 7 – Typical Source-Drain Diode Forward Voltage

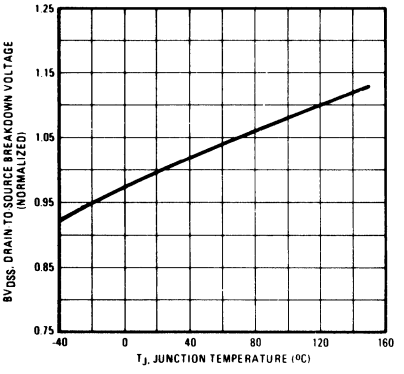


Fig. 8 – Breakdown Voltage Vs. Temperature

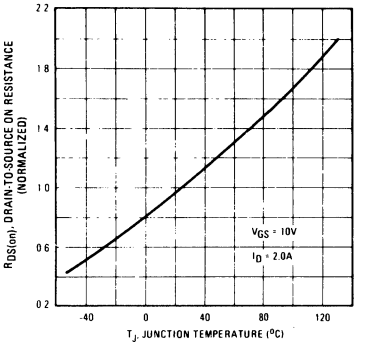


Fig. 9 – Normalized On-Resistance Vs. Temperature

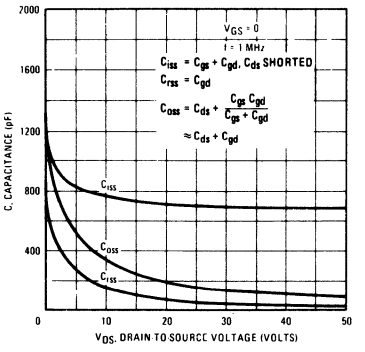


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

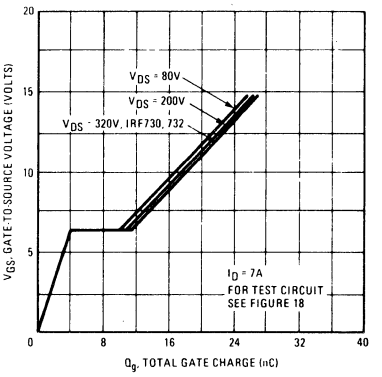


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF730, IRF731, IRF732, IRF733

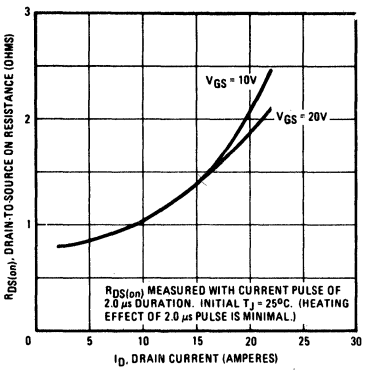


Fig. 12 – Typical On-Resistance Vs. Drain Current

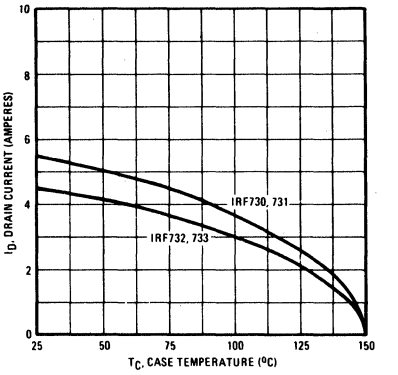


Fig. 13 – Maximum Drain Current Vs. Case Temperature

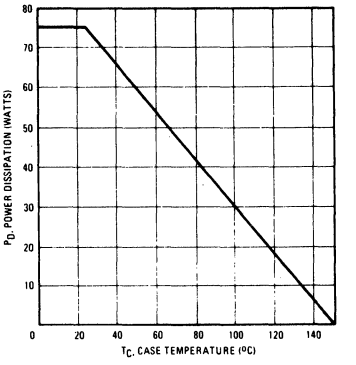


Fig. 14 – Power Vs. Temperature Derating Curve

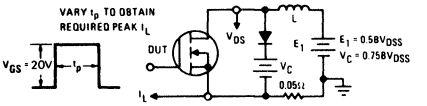


Fig. 15 – Clamped Inductive Test Circuit

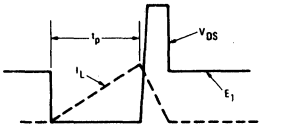


Fig. 16 – Clamped Inductive Waveforms

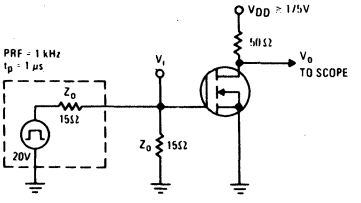


Fig. 17 – Switching Time Test Circuit

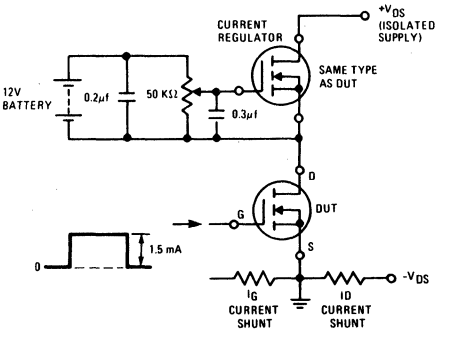


Fig. 18 – Gate Charge Test Circuit

File Number **1581**

IRF820, IRF821, IRF822, IRF823

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

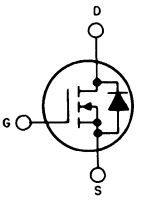
2.0A and 2.5A, 450V-500V

$r_{DS}(on)$ = 3.0 Ω and 4.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

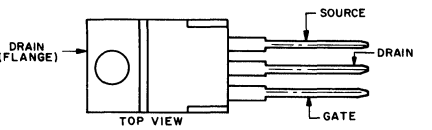
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

The IRF820, IRF821, IRF822 and IRF823 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

Absolute Maximum Ratings

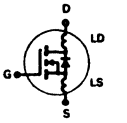
	Parameter	IRF820	IRF821	IRF822	IRF823	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	2.5	2.5	2.0	2.0	A
I_D @ T_C = 100°C	Continuous Drain Current	1.5	1.5	1.0	1.0	A
I_{DM}	Pulsed Drain Current ③	10	10	8.0	8.0	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	40 (See Fig. 14)				W
	Linear Derating Factor	0.32 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		10	10	8.0	8.0	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

IRF820, IRF821, IRF822, IRF823

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF820 IRF822	500	–	–	V	V_{GS} = 0V
		IRF821 IRF823	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF820 IRF821	2.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, V_{GS} = 10V
		IRF822 IRF823	2.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF820 IRF821	–	2.5	3.0	Ω	V_{GS} = 10V, I_D = 1.0A
		IRF822 IRF823	–	3.0	4.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	1.0	1.75	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)\,max.}$, I_D = 1.0A
C_{iss}	Input Capacitance	ALL	–	300	400	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	75	150	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	20	40	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	30	60	ns	V_{DD} ≈ 0.5 BV_{DSS}, I_D = 1.0A, Z_o = 50Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	25	50	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	30	60	ns	
t_f	Fall Time	ALL	–	15	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	15	nC	V_{GS} = 10V, I_D = 3.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.0	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	6.0	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	3.12	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF820 IRF821	–	–	2.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF822 IRF823	–	–	2.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF820 IRF821	–	–	10	A	
		IRF822 IRF823	–	–	8.0	A	
V_{SD}	Diode Forward Voltage ②	IRF820 IRF821	–	–	1.6	V	T_C = 25°C, I_S = 2.5A, V_{GS} = 0V
		IRF822 IRF823	–	–	1.5	V	T_C = 25°C, I_S = 2.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	600	–	ns	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	3.5	–	μC	T_J = 150°C, I_F = 2.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

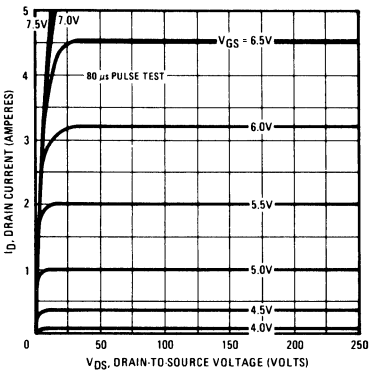


Fig. 1 – Typical Output Characteristics

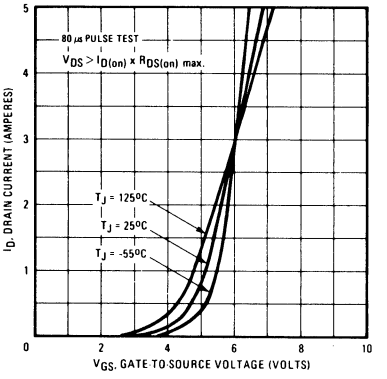


Fig. 2 – Typical Transfer Characteristics

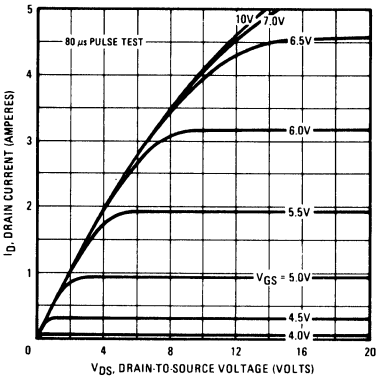


Fig. 3 – Typical Saturation Characteristics

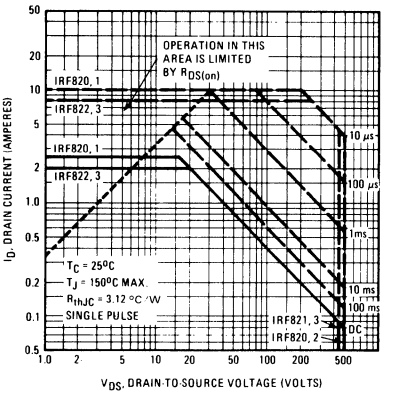


Fig. 4 – Maximum Safe Operating Area

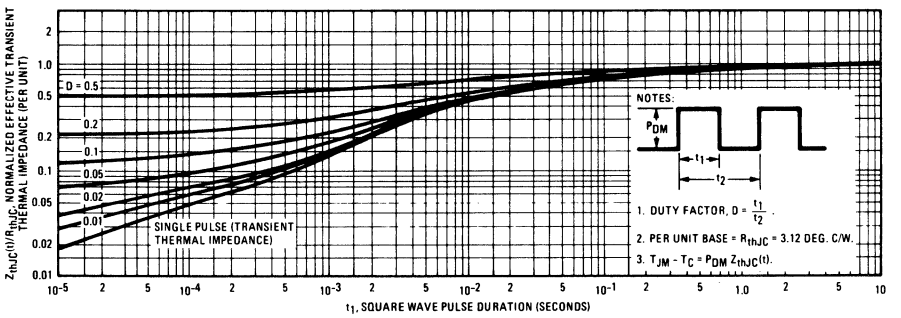


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

IRF820, IRF821, IRF822, IRF823

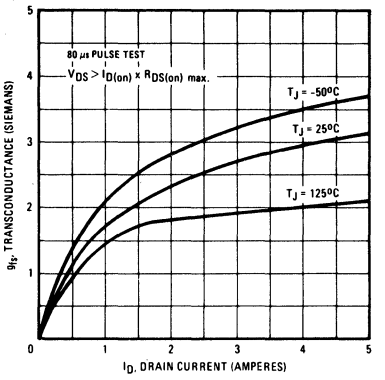


Fig. 6 – Typical Transconductance Vs. Drain Current

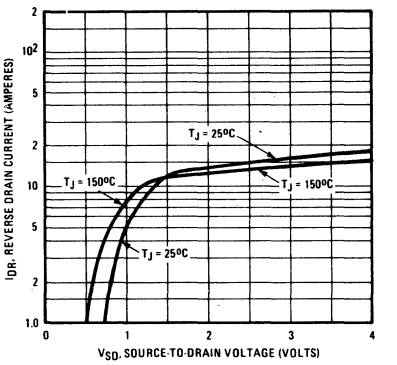


Fig. 7 – Typical Source-Drain Diode Forward Voltage

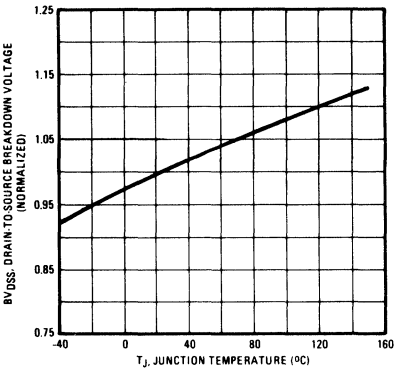


Fig. 8 – Breakdown Voltage Vs. Temperature

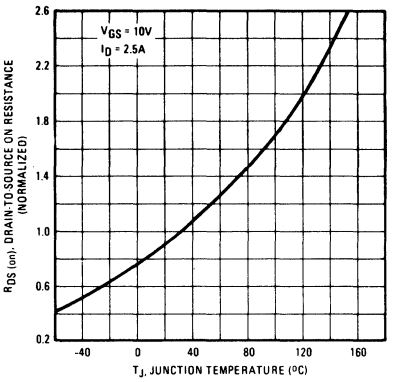


Fig. 9 – Normalized On-Resistance Vs. Temperature

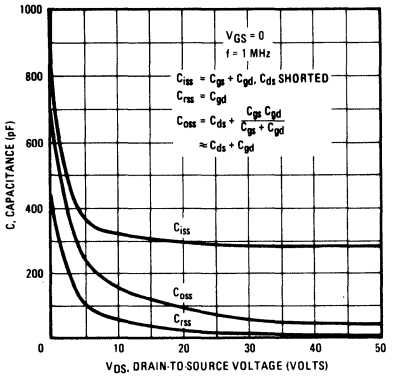


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

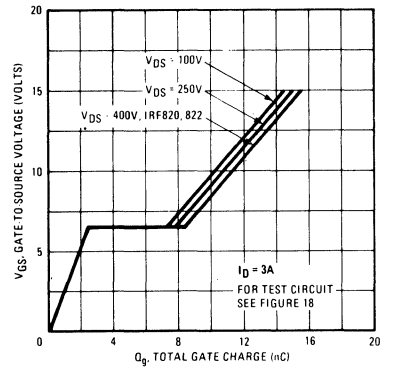


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

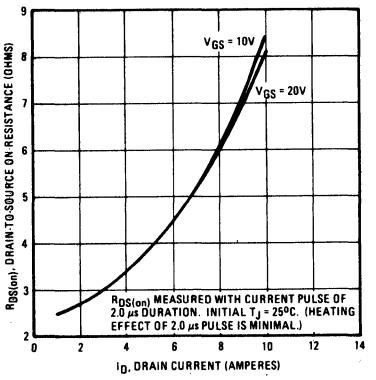


Fig. 12 – Typical On-Resistance Vs. Drain Current

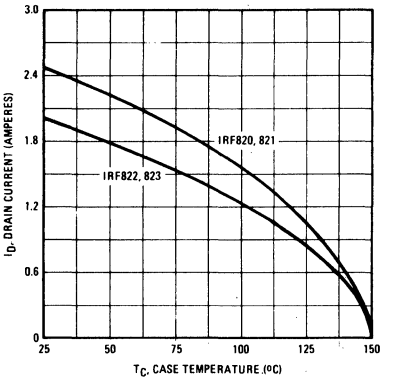


Fig. 13 – Maximum Drain Current Vs. Case Temperature

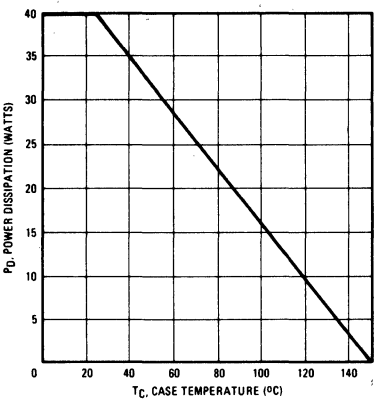


Fig. 14 – Power Vs. Temperature Derating Curve

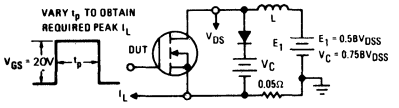


Fig. 15 – Clamped Inductive Test Circuit

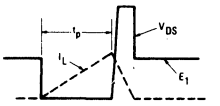


Fig. 16 – Clamped Inductive Waveforms

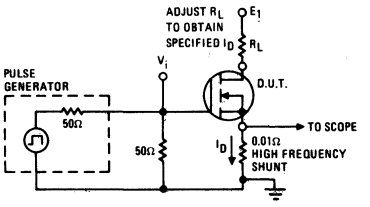


Fig. 17 – Switching Time Test Circuit

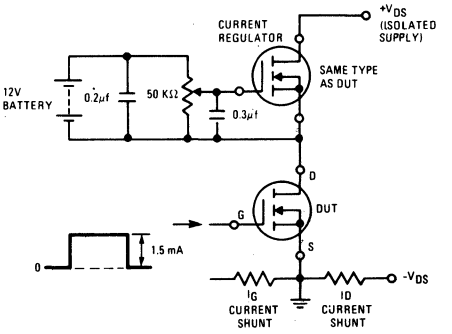


Fig. 18 – Gate Charge Test Circuit

IRF830, IRF831, IRF832, IRF833

File Number **1582**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

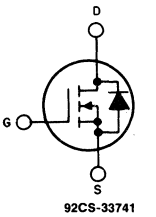
4.0A and 4.5A, 450V-500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



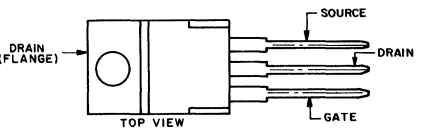
92CS-33741

TERMINAL DIAGRAM

The IRF830, IRF831, IRF832 and IRF833 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-220AB plastic package.

TERMINAL DESIGNATION



92CS-39528

JEDEC TO-220AB

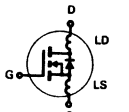
Absolute Maximum Ratings

Parameter		IRF830	IRF831	IRF832	IRF833	Units
V_{DS}	Drain - Source Voltage ①	500	450	500	450	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	500	450	500	450	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5	4.5	4.0	4.0	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0	3.0	2.5	2.5	A
I_{DM}	Pulsed Drain Current ③	18	18	16	16	A
V_{GS}	Gate - Source Voltage	±20				V
P_D @ T_C = 25°C	Max. Power Dissipation	75 (See Fig. 14)				W
-	Linear Derating Factor	0.6 (See Fig. 14)				W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 15 and 16) L = 100μH				A
		18	18	16	16	
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150				°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				°C

Electrical Characteristics @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRF830 IRF832	500	–	–	V	V_{GS} = 0V
		IRF831 IRF833	450	–	–	V	I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{GSS}	Gate-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$I_{D(on)}$	On-State Drain Current ②	IRF830 IRF831	4.5	–	–	A	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., V_{GS} = 10V
		IRF832 IRF833	4.0	–	–	A	
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRF830 IRF831	–	1.3	1.5	Ω	V_{GS} = 10V, I_D = 2.5A
		IRF832 IRF833	–	1.5	2.0	Ω	
g_{fs}	Forward Transconductance ②	ALL	2.5	3.25	–	S (℧)	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max., I_D = 2.5A
C_{iss}	Input Capacitance	ALL	–	600	800	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	–	100	200	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	60	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30	ns	V_{DD} = 225V, I_D = 2.5A, Z_o = 15Ω See Fig. 17 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55	ns	
t_f	Fall Time	ALL	–	–	30	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	22	30	nC	V_{GS} = 10V, I_D = 6.0A, V_{DS} = 0.8 Max. Rating. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	11	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	11	–	nC	
L_D	Internal Drain Inductance	ALL	–	3.5	–	nH	Measured from the contact screw on tab to center of die.
			–	4.5	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	7.5	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	1.0	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	80	°C/W	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	IRF830 IRF831	–	–	4.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRF832 IRF833	–	–	4.0	A	
I_{SM}	Pulse Source Current (Body Diode) ③	IRF830 IRF831	–	–	18	A	
		IRF832 IRF833	–	–	16	A	
V_{SD}	Diode Forward Voltage ②	IRF830 IRF831	–	–	1.6	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0V
		IRF832 IRF833	–	–	1.5	V	T_C = 25°C, I_S = 4.0A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	800	–	ns	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.6	–	μC	T_J = 150°C, I_F = 4.5A, dI_F/dt = 100 A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

IRF830, IRF831, IRF832, IRF833

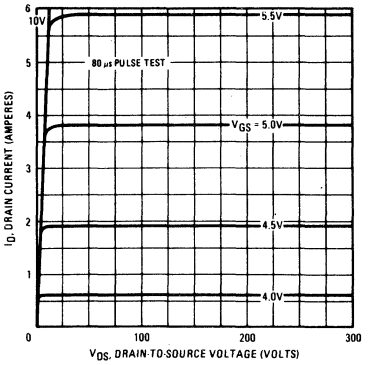


Fig. 1 – Typical Output Characteristics

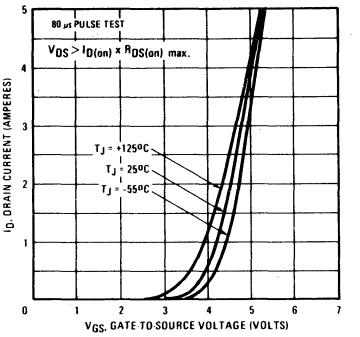


Fig. 2 – Typical Transfer Characteristics

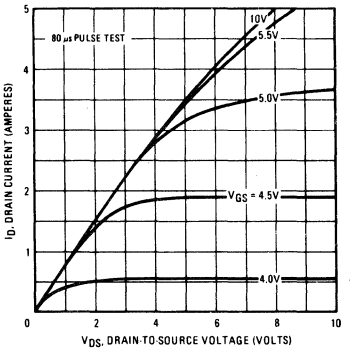


Fig. 3 – Typical Saturation Characteristics

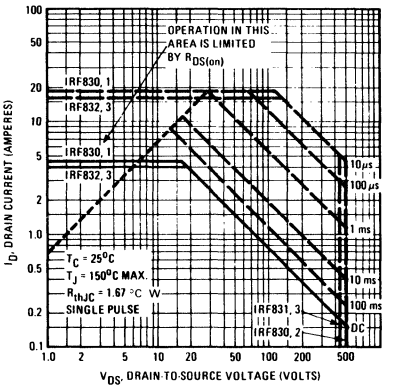


Fig. 4 – Maximum Safe Operating Area

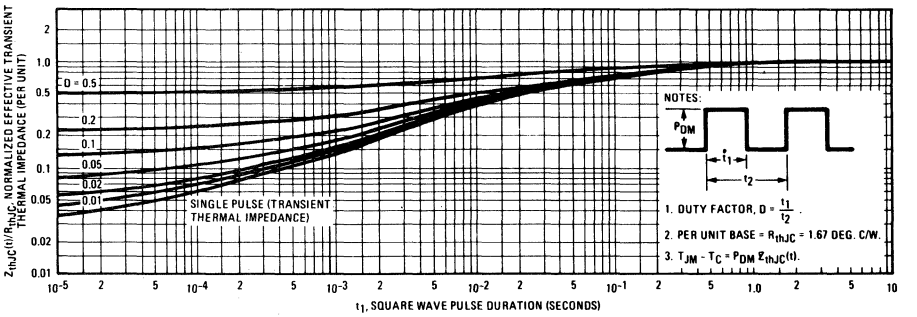


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

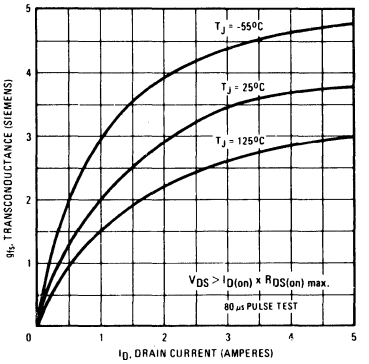


Fig. 6 – Typical Transconductance Vs. Drain Current

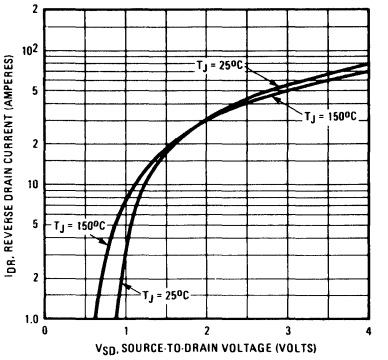


Fig. 7 – Typical Source-Drain Diode Forward Voltage

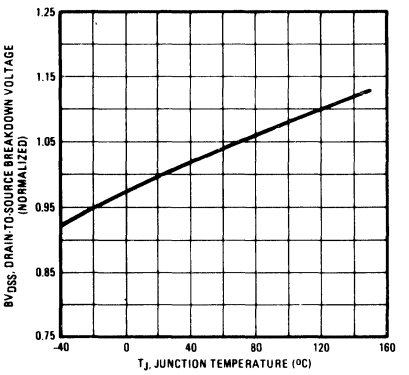


Fig. 8 – Breakdown Voltage Vs. Temperature

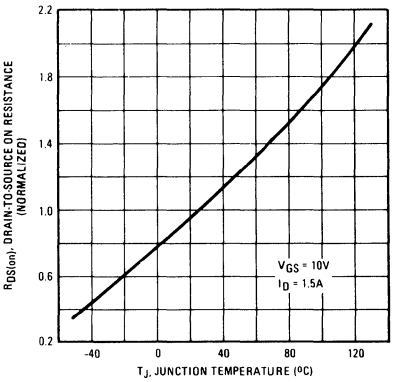


Fig. 9 – Normalized On-Resistance Vs. Temperature

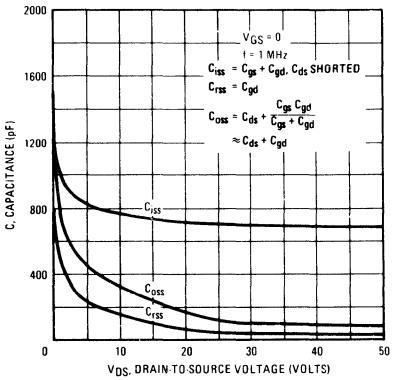


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

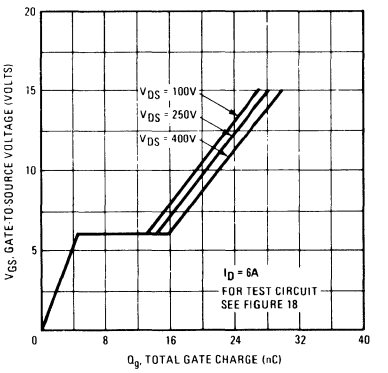


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

IRF830, IRF831, IRF832, IRF833

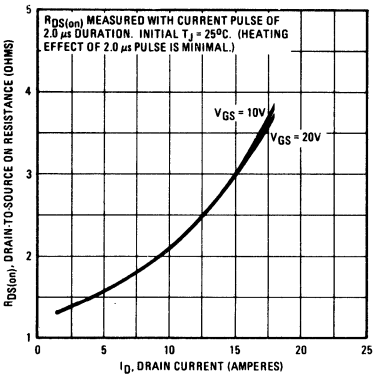


Fig. 12 – Typical On-Resistance Vs. Drain Current

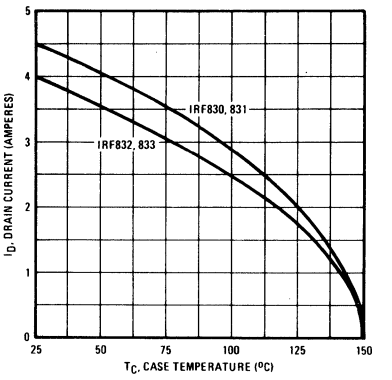


Fig. 13 – Maximum Drain Current Vs. Case Temperature

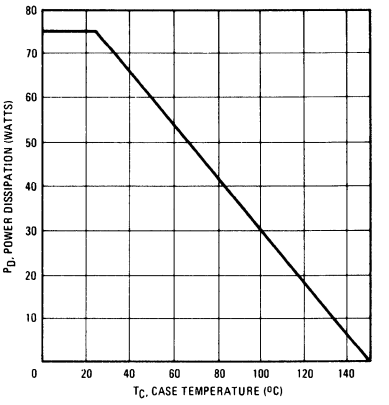


Fig. 14 – Power Vs. Temperature Derating Curve

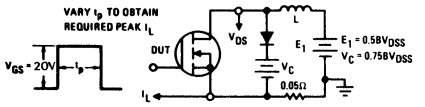


Fig. 15 – Clamped Inductive Test Circuit

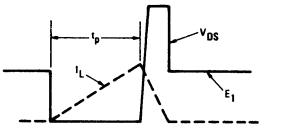


Fig. 16 – Clamped Inductive Waveforms

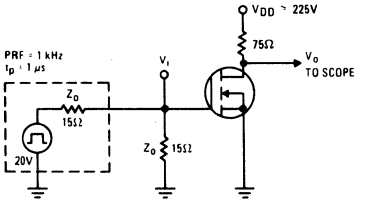


Fig. 17 – Switching Time Test Circuit

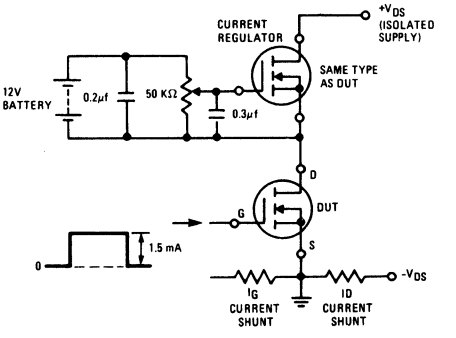


Fig. 18 – Gate Charge Test Circuit

File Number **1586**

2N6755, 2N6756

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

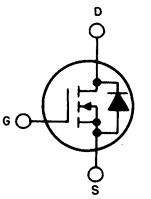
12A and 14A, 60V - 100V

$r_{DS}(on)$ = 0.18 Ω and 0.25 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

N-CHANNEL ENHANCEMENT MODE



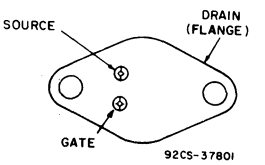
92CS-33741

TERMINAL DIAGRAM

The 2N6755 and 2N6756 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6755	2N6756	Units
V_{DS}	Drain – Source Voltage	60*	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} 20 KΩ)	60*	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	12*	14*	A
I_D @ T_C = 100°C	Continuous Drain Current	8.0*	9.0*	A
I_{DM}	Pulsed Drain Current	25	30	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		25	30	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

2N6755, 2N6756

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, T_C = 125°C
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 36V, I_D = 9A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	75*	ns	(See Figs. 13 and 14)
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	45*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage ①	2N6755	0.85*	–	1.7*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	300	–	ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

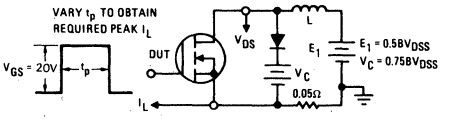


Fig. 1 – Clamped Inductive Test Circuit

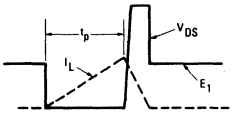


Fig. 2 – Clamped Inductive Waveforms

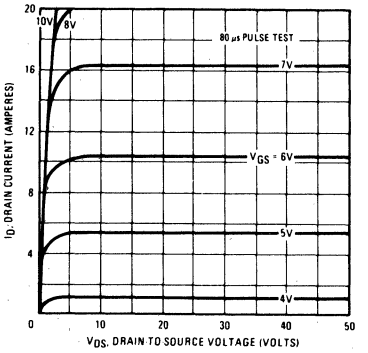


Fig. 3 – Typical Output Characteristics

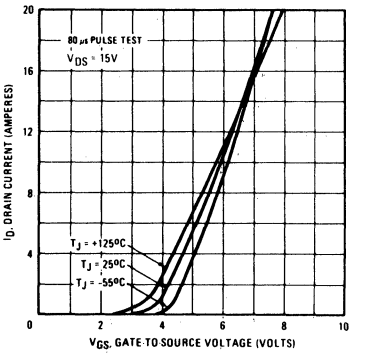


Fig. 4 – Typical Transfer Characteristics

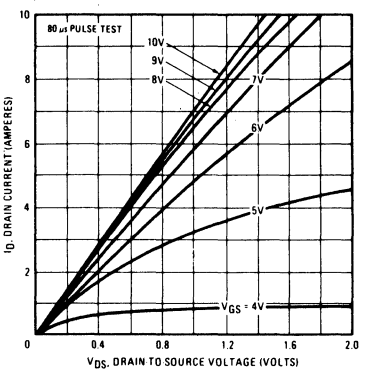


Fig. 5– Typical Saturation Characteristics (2N6755)

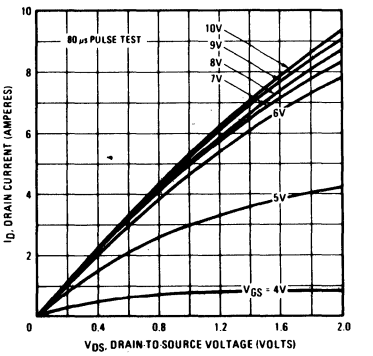


Fig. 6– Typical Saturation Characteristics (2N6756)

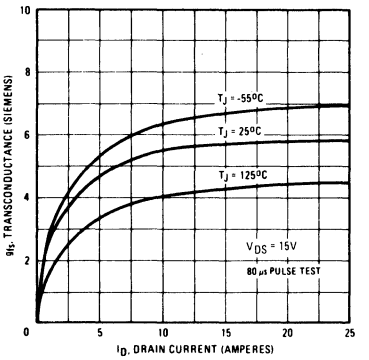


Fig. 7 – Typical Transconductance Vs. Drain Current

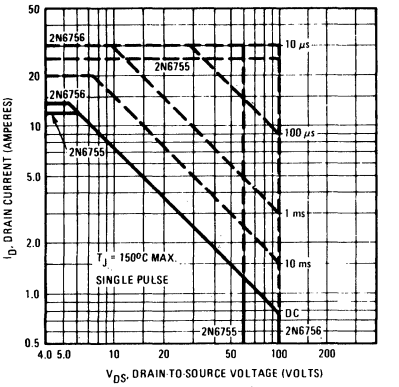


Fig. 8 – Maximum Safe Operating Area

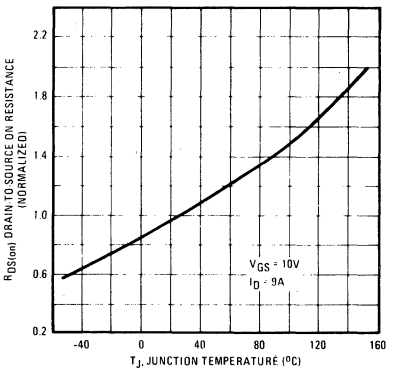


Fig.9–Normalized Typical On-Resistance Vs. Temperature

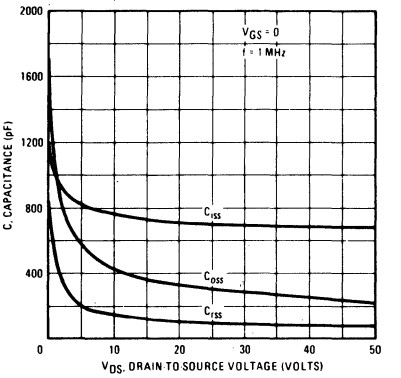


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

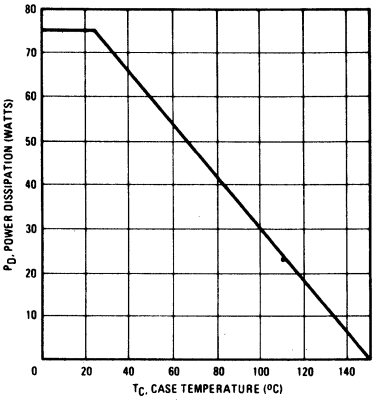


Fig. 11 – Power Vs. Temperature Derating Curve

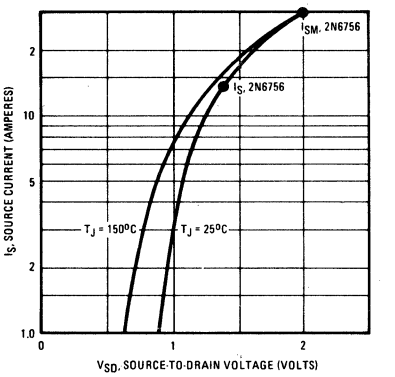


Fig. 12 – Typical Body-Drain Diode Forward Voltage

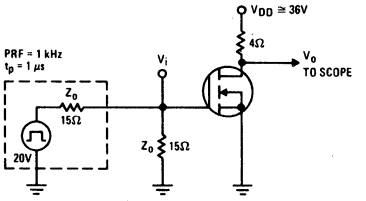


Fig. 13 – Switching Time Test Circuit

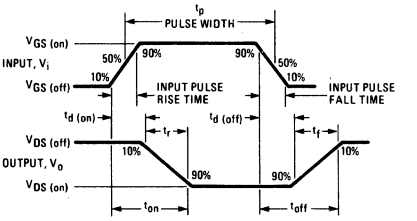


Fig. 14 – Switching Time Waveforms

File Number **1587**

2N6757, 2N6758

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

8A and 9A, 150V - 200V

$r_{DS}(on)$ = 0.4 Ω and 0.6 Ω

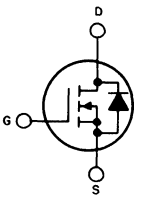
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6757 and 2N6758 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

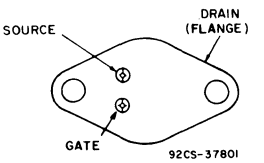
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6757	2N6758	Units
V_{DS}	Drain – Source Voltage	150*	200*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	150*	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	9.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	6.0*	A
I_{DM}	Pulsed Drain Current	12	15	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		12	15	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

2N6757, 2N6758

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6757	150	–	–	V	$V_{GS} = 0$
		2N6758	200	–	–	V	$I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6757	–	–	4.8*	V	$V_{GS} = 10V$, $I_D = 8A$
		2N6758	–	–	3.6*	V	$V_{GS} = 10V$, $I_D = 9A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	0.4	0.6*	Ω	$V_{GS} = 10V$, $I_D = 5A$
		2N6758	–	0.25	0.4*	Ω	$V_{GS} = 10V$, $I_D = 6A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6757	–	–	1.13*	Ω	$V_{GS} = 10V$, $I_D = 5A$, $T_C = 125^oC$
		2N6758	–	–	0.75*	Ω	$V_{GS} = 10V$, $I_D = 6A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	3.0*	5.0	9.0*	S (℧)	$V_{DS} = 15V$, $I_D = 6A$
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	100*	250	450*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 90V$, $I_D = 6A$, $Z_o = 15\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	50*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	50*	ns	
t_f	Fall Time	ALL	–	–	40*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6757	–	–	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6758	–	–	9.0*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6757	–	–	12	A	
		2N6758	–	–	15		
V_{SD}	Diode Forward Voltage ①	2N6757	0.75*	–	1.50*	V	$T_C = 25^oC$, $I_S = 8A$, $V_{GS} = 0$
		2N6758	0.80*	–	1.60*	V	$T_C = 25^oC$, $I_S = 9A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	650	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

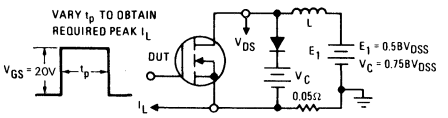


Fig. 1 – Clamped Inductive Test Circuit

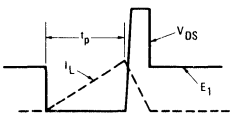


Fig. 2 – Clamped Inductive Waveforms

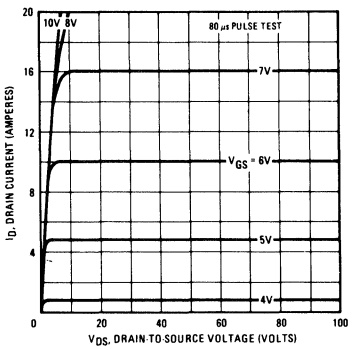


Fig. 3 – Typical Output Characteristics

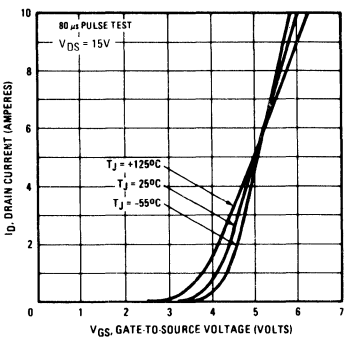


Fig. 4 – Typical Transfer Characteristics

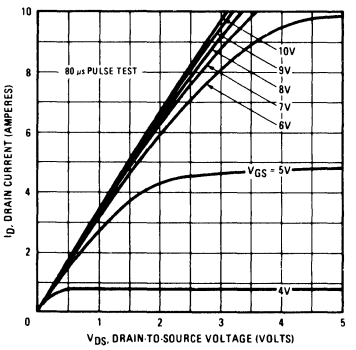


Fig. 5— Typical Saturation Characteristics (2N6757)

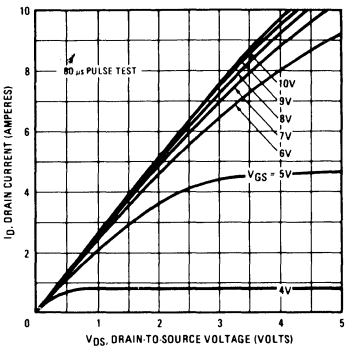


Fig. 6— Typical Saturation Characteristics (2N6758)

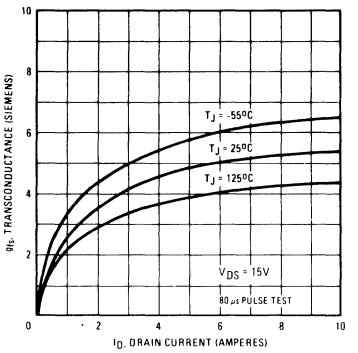


Fig. 7 — Typical Transconductance Vs. Drain Current

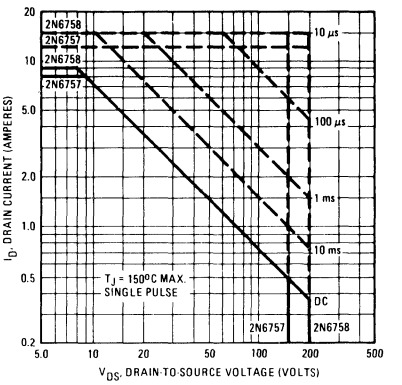


Fig. 8 — Maximum Safe Operating Area

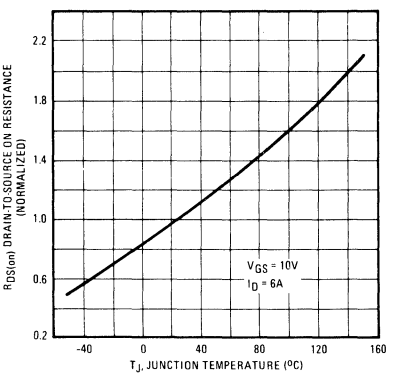


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

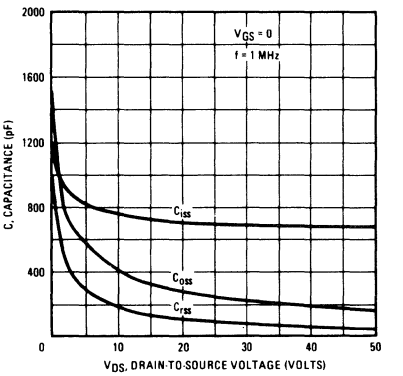


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

2N6757, 2N6758

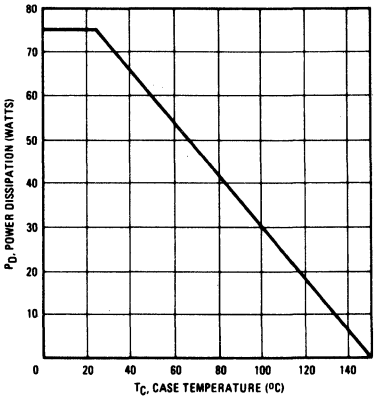


Fig. 11 – Power Vs. Temperature Derating Curve

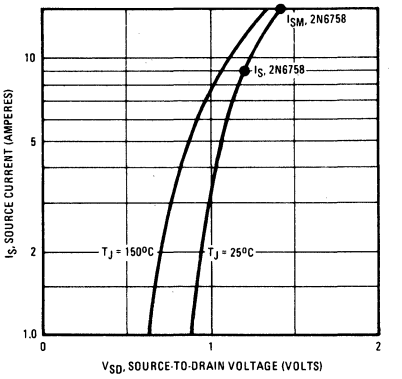


Fig. 12 – Typical Body-Drain Diode Forward Voltage

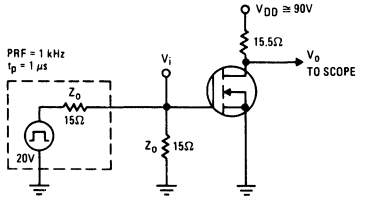


Fig. 13 – Switching Time Test Circuit

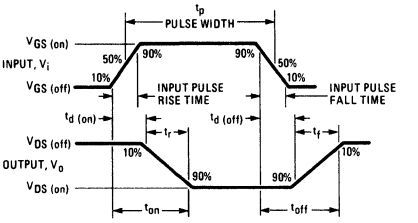


Fig. 14 – Switching Time Waveforms

File Number **1588**

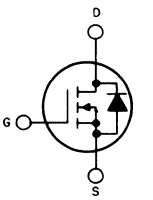
2N6759, 2N6760

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.5A and 5.5A, 350V - 400V

$r_{DS}(on)$ = 1.0 Ω and 1.5 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

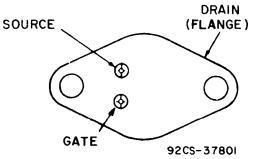


N-CHANNEL ENHANCEMENT MODE

The 2N6759 and 2N6760 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6759	2N6760	Units
V_{DS}	Drain – Source Voltage	350*	400*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	350*	400*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.5*	5.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.0*	3.5*	A
I_{DM}	Pulsed Drain Current	7.0	8.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		7.0	8.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

2N6759, 2N6760

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6759	350	–	–	V	V_{GS} = 0
		2N6760	400	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6759	–	–	7.0*	V	V_{GS} = 10V, I_D = 4.5A
		2N6760	–	–	6.7*	V	V_{GS} = 10V, I_D = 5.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	1.0	1.5*	Ω	V_{GS} = 10V, I_D = 3A
		2N6760	–	0.8	1.0*	Ω	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6759	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3A, T_C = 125°C
		2N6760	–	–	2.2*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	3.0*	4.5	9.0*	S (℧)	V_{DS} = 15V, I_D = 3.5A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	50*	150	300*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	20*	40	80*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong$ 175V, I_D = 3.5A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	35*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	35*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6759	–	–	4.5*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6760	–	–	5.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6759	–	–	7.0	A	
		2N6760	–	–	8.0		
V_{SD}	Diode Forward Voltage ①	2N6759	0.70*	–	1.4*	V	T_C = 25°C, I_S = 4.5A, V_{GS} = 0
		2N6760	0.75*	–	1.5*	V	T_C = 25°C, I_S = 5.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	550	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	8.0	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

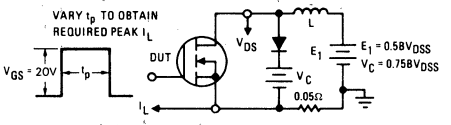


Fig. 1 – Clamped Inductive Test Circuit

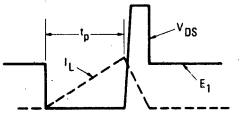


Fig. 2 – Clamped Inductive Waveforms

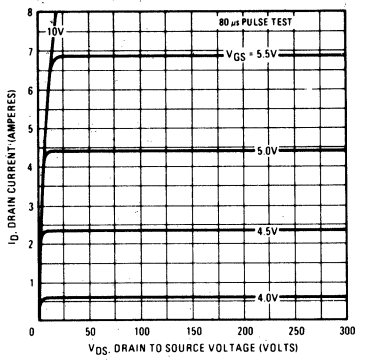


Fig. 3 – Typical Output Characteristics

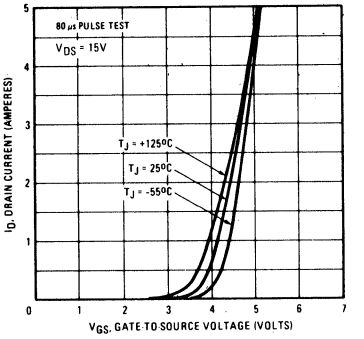


Fig. 4 – Typical Transfer Characteristics

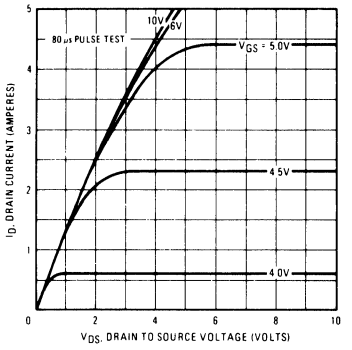


Fig. 5– Typical Saturation Characteristics (2N6759)

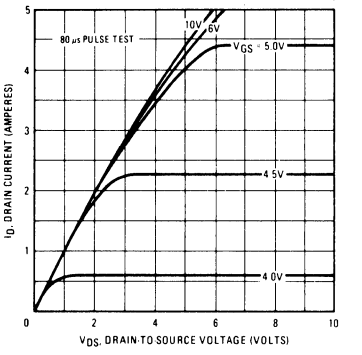


Fig. 6– Typical Saturation Characteristics (2N6760)

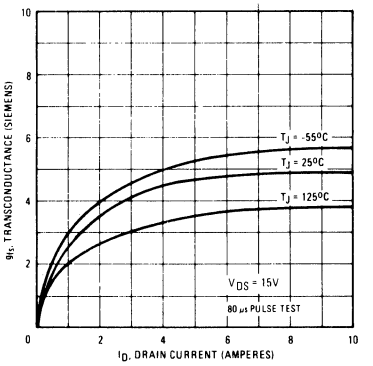


Fig. 7 – Typical Transconductance Vs. Drain Current

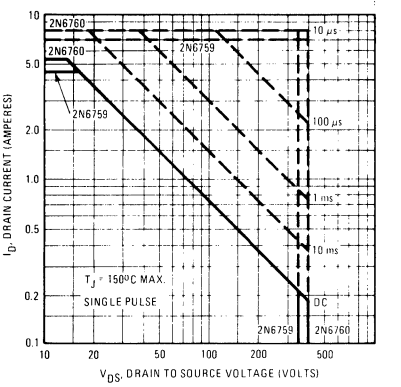


Fig. 8 – Maximum Safe Operating Area

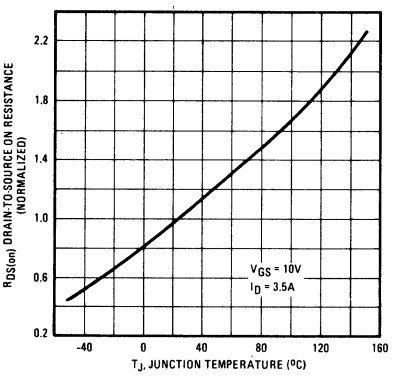


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

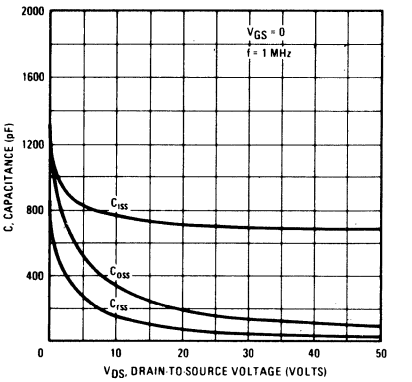


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

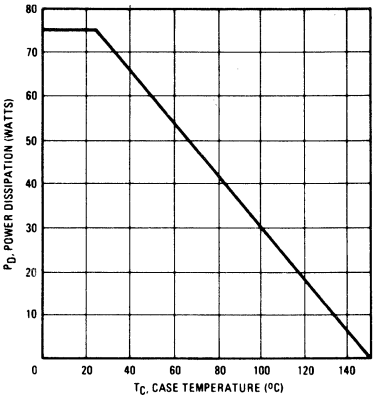


Fig. 11 – Power Vs. Temperature Derating Curve

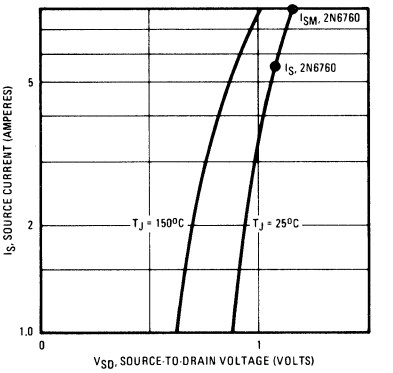


Fig. 12 – Typical Body-Drain Diode Forward Voltage

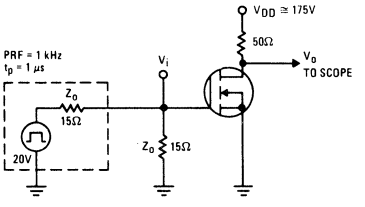


Fig. 13 – Switching Time Test Circuit

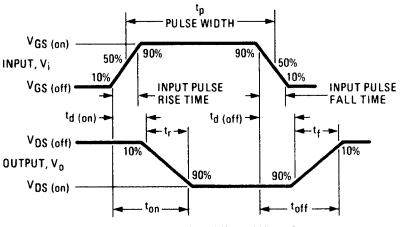


Fig. 14 – Switching Time Waveforms

File Number **1589**

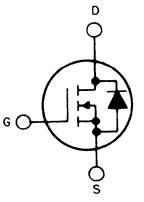
2N6761, 2N6762

N-Channel Enhancement-Mode Power Field-Effect Transistors

4.0A and 4.5A, 450V - 500V

$r_{DS}(on)$ = 1.5 Ω and 2.0 Ω

Features:
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



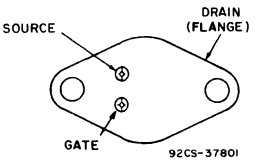
92CS-33741

N-CHANNEL ENHANCEMENT MODE

The 2N6761 and 2N6762 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

TERMINAL DESIGNATIONS



92CS-37801

JEDEC TO-204AA

Absolute Maximum Ratings

Parameter		2N6761	2N6762	Units
V_{DS}	Drain – Source Voltage	450*	500*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	450*	500*	V
I_D @ T_C = 25°C	Continuous Drain Current	4.0*	4.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.5*	3.0*	A
I_{DM}	Pulsed Drain Current	6.0	7.0	A
V_{GS}	Gate – Source Voltage	±20*		V
P_D @ T_C = 25°C	Max. Power Dissipation	75* (See Fig. 11)		W
P_D @ T_C = 100°C	Max. Power Dissipation	30* (See Fig. 11)		W
	Linear Derating Factor	0.6* (See Fig. 11)		W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH		A
		6.0	7.0	
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*		°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)		°C

2N6761, 2N6762

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6761	450	–	–	V	V_{GS} = 0
		2N6762	500	–	–	V	I_D = 4.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = 0.8 x Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, $T_C = 25^oC$ to 125^oC
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6761	–	–	8.0*	V	V_{GS} = 10V, I_D = 4A
		2N6762	–	–	7.7*	V	V_{GS} = 10V, I_D = 4.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	1.5	2.0*	Ω	V_{GS} = 10V, I_D = 2.5A
		2N6762	–	1.3	1.5*	Ω	V_{GS} = 10V, I_D = 3.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6761	–	–	4.4*	Ω	V_{GS} = 10V, I_D = 2.5A, $T_C = 125^oC$
		2N6762	–	–	3.3*	Ω	V_{GS} = 10V, I_D = 3.0A, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	2.5*	3.5	7.5*	S (℧)	V_{DS} = 16V, I_D = 3A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	25*	100	200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	15*	30	60*	pF	
$t_{d\ (on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	$V_{DD} \cong 225V$, I_D = 3A, $Z_o = 15\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	30*	ns	
$t_{d\ (off)}$	Turn-Off Delay Time	ALL	–	–	55*	ns	
t_f	Fall Time	ALL	–	–	30*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6761	–	–	4.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
		2N6762	–	–	4.5*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6761	–	–	6.0	A	
		2N6762	–	–	7.0		
V_{SD}	Diode Forward Voltage ①	2N6761	0.65*	–	1.3*	V	$T_C = 25^oC$, I_S = 4A, V_{GS} = 0
		2N6762	0.7*	–	1.4*	V	$T_C = 25^oC$, I_S = 4.5A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	7.0	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

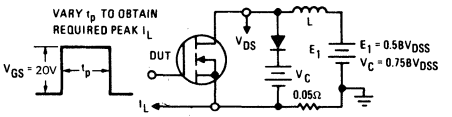


Fig. 1 – Clamped Inductive Test Circuit

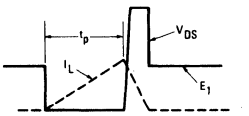


Fig. 2 – Clamped Inductive Waveforms

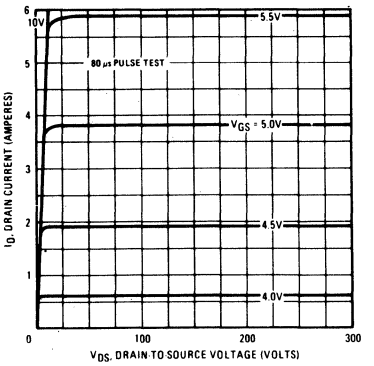


Fig. 3 – Typical Output Characteristics

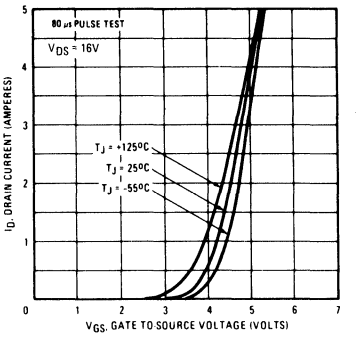


Fig. 4 – Typical Transfer Characteristics

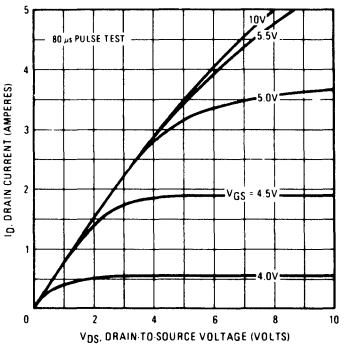


Fig. 5– Typical Saturation Characteristics (2N6761)

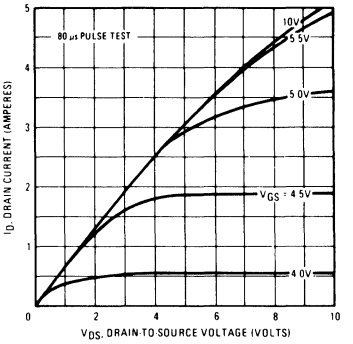


Fig. 6– Typical Saturation Characteristics (2N6762)

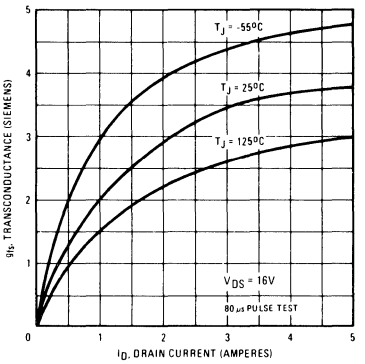


Fig. 7 – Typical Transconductance Vs. Drain Current

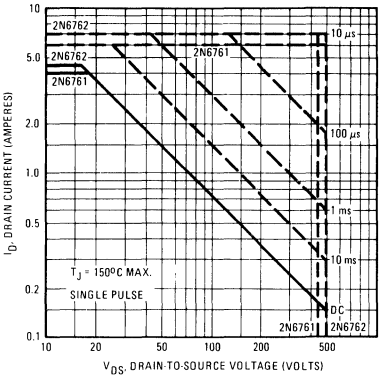


Fig. 8 – Maximum Safe Operating Area

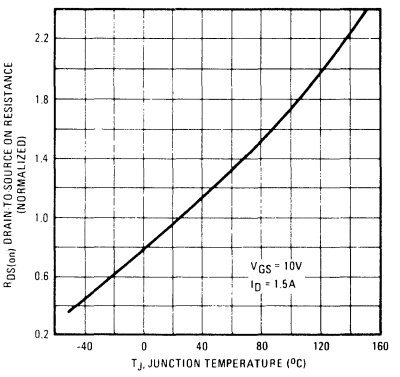


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

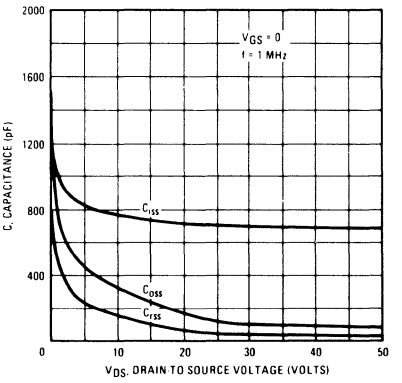


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

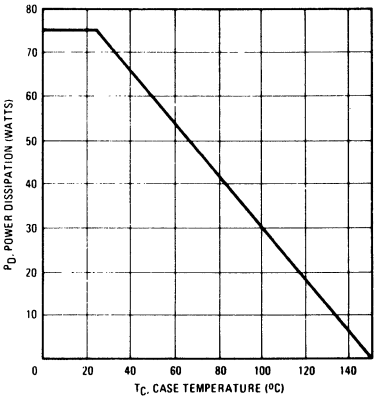


Fig. 11 — Power Vs. Temperature Derating Curve

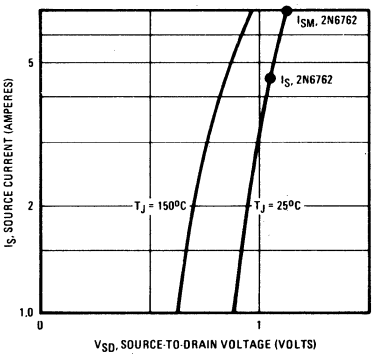


Fig. 12 — Typical Body-Drain Diode Forward Voltage

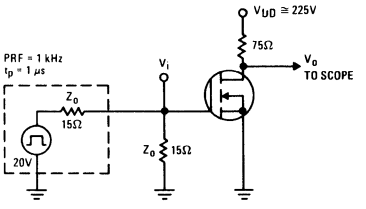


Fig. 13 — Switching Time Test Circuit

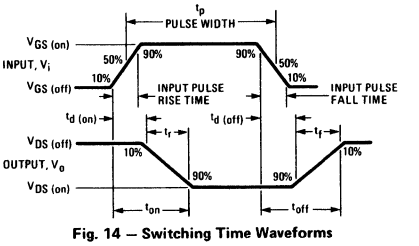


Fig. 14 — Switching Time Waveforms

File Number **1590**

2N6764

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

38A, 100V

$r_{DS}(on)$ = 0.055 Ω

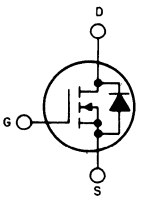
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6764 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6764 is supplied in the JEDEC TO-204AE steel package.

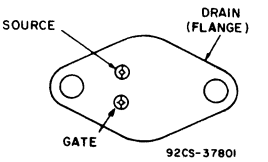
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

Absolute Maximum Ratings

Parameter		2N6764	Units
V_{DS}	Drain – Source Voltage	100*	V
V_{DGR}	Drain – Gate Voltage (R_{GS} = 20 KΩ)	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	38*	A
I_D @ T_C = 100°C	Continuous Drain Current	24*	A
I_{DM}	Pulsed Drain Current	70	A
V_{GS}	Gate – Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)	W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)	W
	Linear Derating Factor	1.2* (See Fig. 11)	W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 60 | 70	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

2N6764

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6764	100	–	–	V	V_{GS} = 0, I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6764	–	–	2.09*	V	V_{GS} = 10V I_D = 31A V_{GS} = 10V, I_D = 38A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6764	–	0.045	0.055*	Ω	V_{GS} = 10V, I_D = 20A V_{GS} = 10V, I_D = 24A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6764	–	–	0.094*	Ω	V_{GS} = 10V, I_D = 20A, T_C = 125°C V_{GS} = 10V, I_D = 24A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	9.0*	12.5	27*	S (℧)	V_{DS} = 15V, I_D = 24A
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	500*	1000	1500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	350	500*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong 24V$, I_D = 24A, Z_o = 4.7Ω (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	
t_f	Fall Time	ALL	–	–	100*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6764	–	–	38*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulsed Source Current (Body Diode)	2N6764	–	–	70	A	
V_{SD}	Diode Forward Voltage ①	2N6764	0.95*	–	1.9*	V	T_C = 25°C, I_S = 31A, V_{GS} = 0
						V	T_C = 25°C, I_S = 38A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	T_J = 150°C, $I_F = I_{SM}$, dI_F/dt = 100 A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

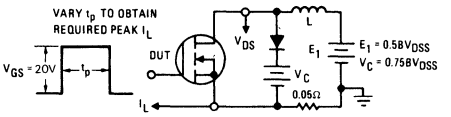


Fig. 1 – Clamped Inductive Test Circuit

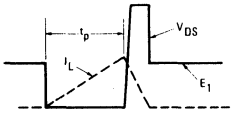


Fig. 2 – Clamped Inductive Waveforms

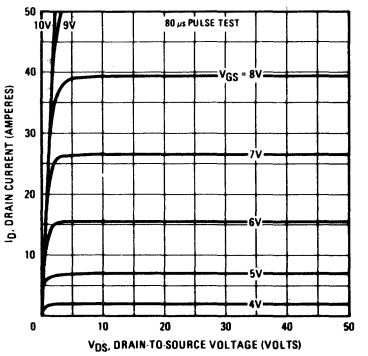


Fig. 3 – Typical Output Characteristics

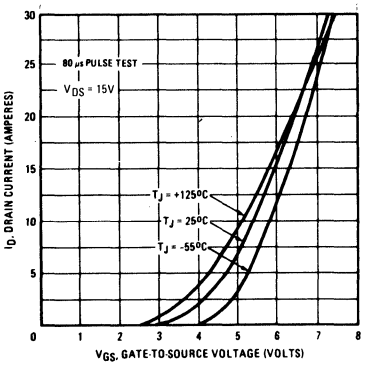


Fig. 4 – Typical Transfer Characteristics

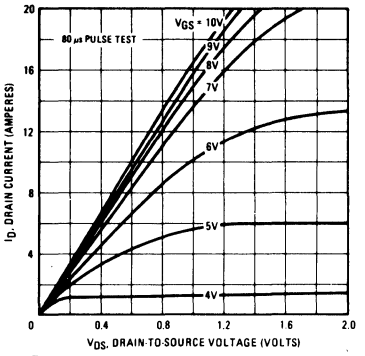


Fig. 5– Typical Saturation Characteristics (2N6764)

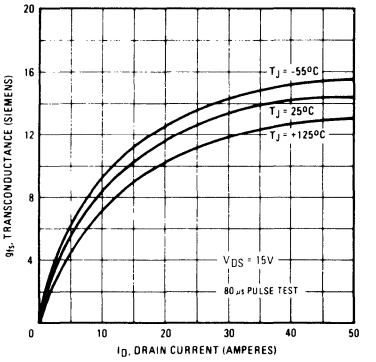


Fig. 6– Typical Transconductance Vs. Drain Current

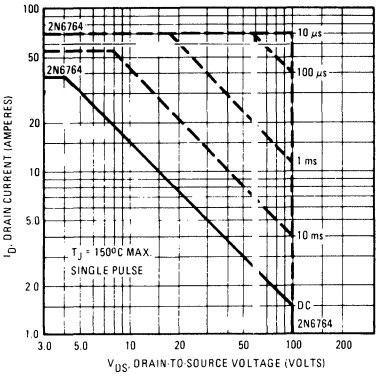


Fig. 7 – Maximum Safe Operating Area

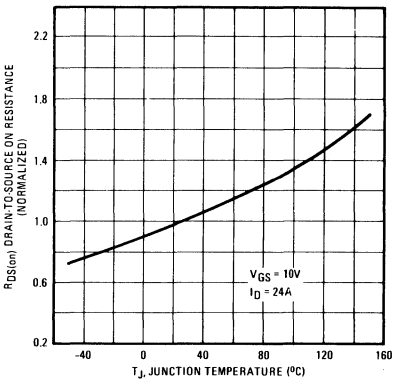


Fig. 8 –Normalized Typical On-Resistance Vs. Temperature

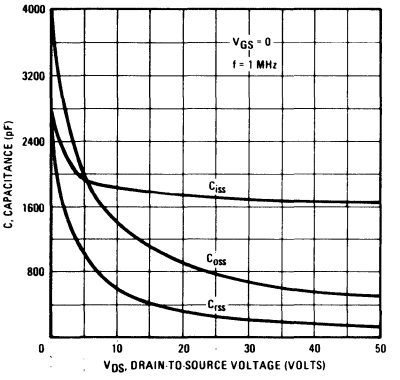


Fig.9 – Typical Capacitance Vs. Drain-to-Source Voltage

2N6764

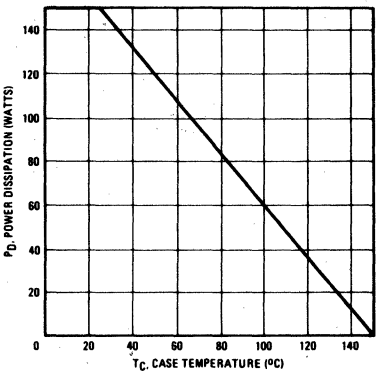


Fig. 10 – Power Vs. Temperature Derating Curve

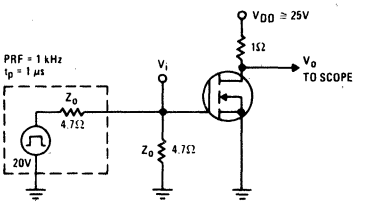


Fig. 12 – Switching Time Test Circuit

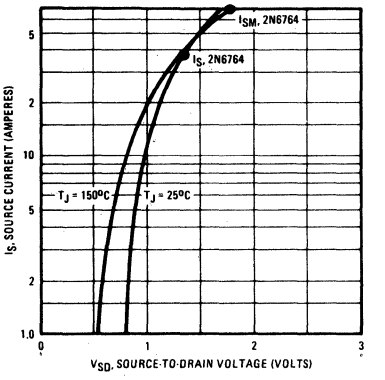


Fig. 11 – Typical Body-Drain Diode Forward Voltage

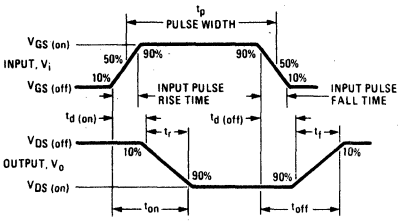


Fig. 13 – Switching Time Waveforms

File Number **1591**

2N6766

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

30A, 200V

$r_{DS}(on)$ = 0.085 Ω

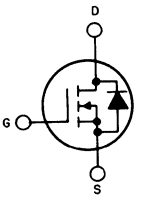
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6766 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6766 is supplied in the JEDEC TO-204AE steel package.

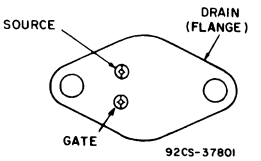
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37801

JEDEC TO-204AE

Absolute Maximum Ratings

Parameter		2N6766	Units
V_{DS}	Drain – Source Voltage	200*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ)	200*	V
I_D @ T_C = 25°C	Continuous Drain Current	30*	A
I_D @ T_C = 100°C	Continuous Drain Current	19*	A
I_{DM}	Pulsed Drain Current	60	A
V_{GS}	Gate – Source Voltage	±20*	V
P_D @ T_C = 25°C	Max. Power Dissipation	150* (See Fig. 11)	W
P_D @ T_C = 100°C	Max. Power Dissipation	60* (See Fig. 11)	W
	Linear Derating Factor	1.2* (See Fig. 11)	W/°C
I_{LM}	Inductive Current, Clamped	(See Fig. 1 and 2) L = 100 μH 50 | 60	A
T_J T_{stg}	Operating and Storage Temperature Range	-55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

2N6766

Electrical Characteristics @ $T_C = 25^oC$ (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6766	200	–	–	V	$V_{GS} = 0$, $I_D = 1.0$ mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1$ mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	$V_{GS} = 20V$
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	$V_{GS} = -20V$
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, $V_{GS} = 0$, $T_C = 125^oC$
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6766	–	–	2.7*	V	$V_{GS} = 10V$, $I_D = 25A$
							$V_{GS} = 10V$, $I_D = 30A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6766	–	0.07	0.085*	Ω	$V_{GS} = 10V$, $I_D = 16A$
							$V_{GS} = 10V$, $I_D = 19A$
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6766	–	–	0.153*	Ω	$V_{GS} = 10V$, $I_D = 16A$, $T_C = 125^oC$
							$V_{GS} = 10V$, $I_D = 19A$, $T_C = 125^oC$
g_{fs}	Forward Transconductance ①	ALL	9.0*	15.5	27*	S (℧)	$V_{DS} = 15V$, $I_D = 19A$
C_{iss}	Input Capacitance	ALL	1000*	2000	3000*	pF	$V_{GS} = 0$, $V_{DS} = 25V$, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	450*	800	1200*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	150*	300	500*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	35*	ns	$V_{DD} \cong 95V$, $I_D = 19A$, $Z_o = 4.7\Omega$ (See Figs. 13 and 14) (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	–	100*	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	125*	ns	
t_f	Fall Time	ALL	–	–	100*	ns	

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	0.83*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6766	–	–	30*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
I_{SM}	Pulsed Source Current (Body Diode)	2N6766	–	–	60	A	
V_{SD}	Diode Forward Voltage ①	2N6766	0.9*	–	1.8*	V	$T_C = 25^oC$, $I_S = 25A$, $V_{GS} = 0$
							$T_C = 25^oC$, $I_S = 30A$, $V_{GS} = 0$
t_{rr}	Reverse Recovery Time	ALL	–	500	–	ns	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	10	–	μC	$T_J = 150^oC$, $I_F = I_{SM}$, $dI_F/dt = 100$ A/μs

*JEDEC registered values. ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

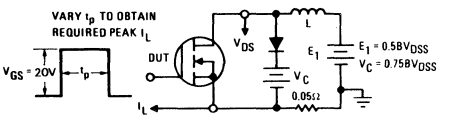


Fig. 1 – Clamped Inductive Test Circuit

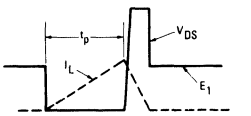


Fig. 2 – Clamped Inductive Waveforms

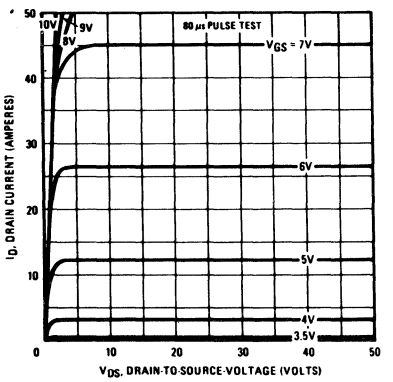


Fig. 3 – Typical Output Characteristics

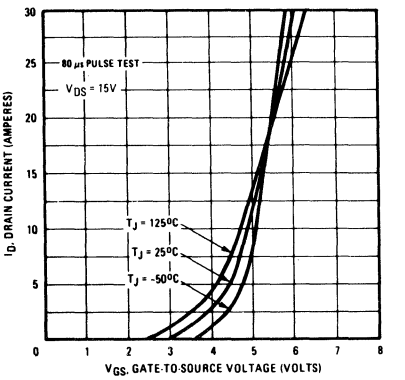


Fig. 4 – Typical Transfer Characteristics

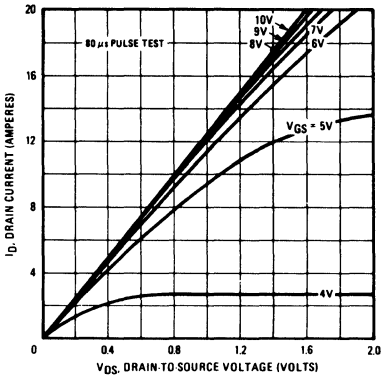


Fig. 5– Typical Saturation Characteristics (2N6765)

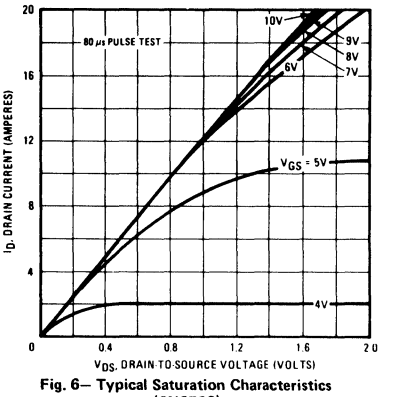


Fig. 6– Typical Saturation Characteristics (2N6766)

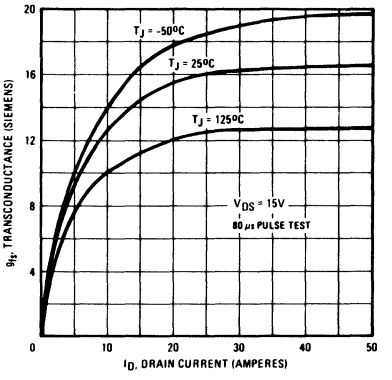


Fig. 7 – Typical Transconductance Vs. Drain Current

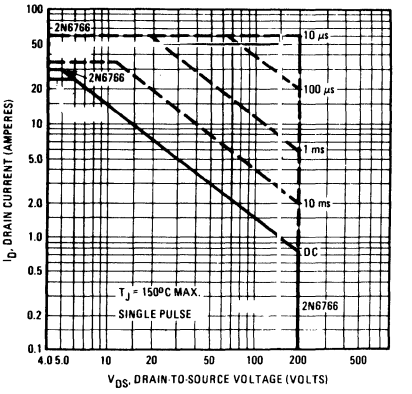


Fig. 8 – Maximum Safe Operating Area

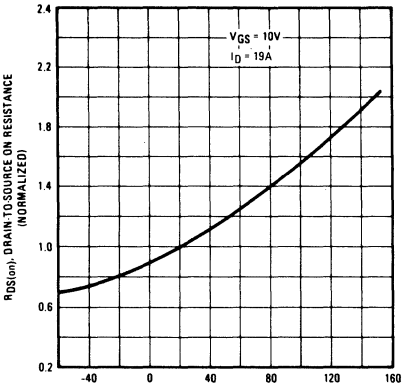


Fig. 9 – Normalized Typical On-Resistance Vs. Temperature

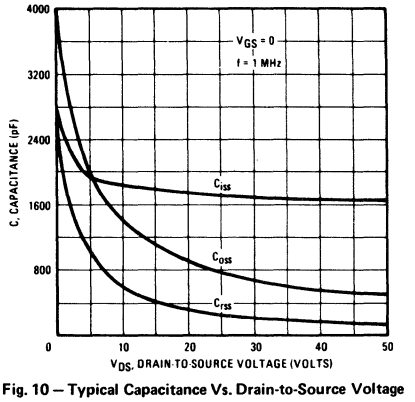


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

2N6766

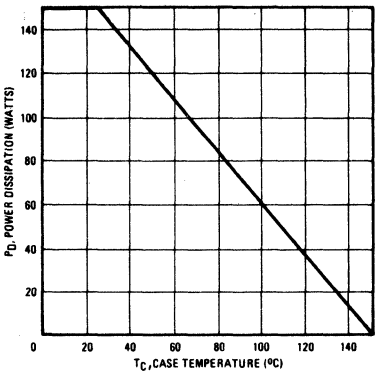


Fig. 11 – Power Vs. Temperature Derating Curve

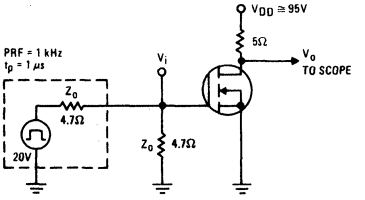


Fig. 13 – Switching Time Test Circuit

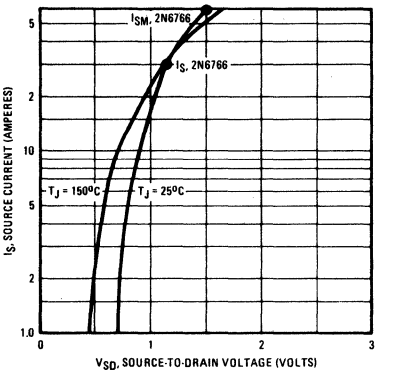


Fig. 12 – Typical Body-Drain Diode Forward Voltage

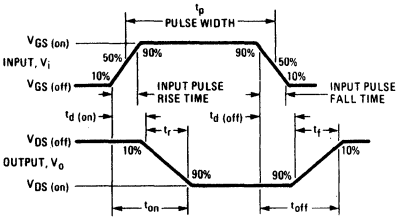


Fig. 14 – Switching Time Waveforms

File Number **1592**

2N6782

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

3.5A, 100V

$r_{DS}(on)$ = 0.6 Ω

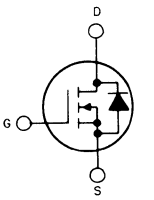
Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

The 2N6782 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6782 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

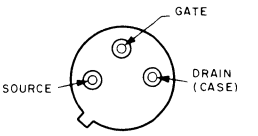
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

Absolute Maximum Ratings

Parameter		2N6782	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	3.5*	A
I_D @ T_C = 100°C	Continuous Drain Current	2.25*	A
I_{DM}	Pulsed Drain Current ③	14*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	3.50*	A
I_{SM}	Pulse Source Current (Body Diode) ③	14*	A
P_D @ T_C = 25°C	Max. Power Dissipation	15* (See Fig. 14)	W
	Linear Derating Factor	0.12* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 14	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

2N6782

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	2.1*	V	V_{GS} = 10V, I_D = 3.5A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.5	0.6*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 25°C
		–	–	1.08*	Ω	V_{GS} = 10V, I_D = 2.25A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 3.5A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.0*	1.5	3.0*	S(℧)	V_{DS} = 5V, I_D = 2.25A
C_{iss}	Input Capacitance	60*	135	200*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	40*	80	100*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	10*	20	25*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	15*	ns	V_{DD} ≅ 34V, I_D = 2.25A, Z_o = 50Ω
t_r	Rise Time	–	–	25*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	25*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	20*	ns	of operating temperature.)
SOA	Safe Operating Area	15	–	–	W	V_{DS} = 80V, I_D = 188 mA, See Fig. 16.
		15	–	–	W	V_{DS} = 4.28V, I_D = 3.5A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	8.33*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	200	ns	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.0	μC	T_J = 150°C, I_F = 3.5A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

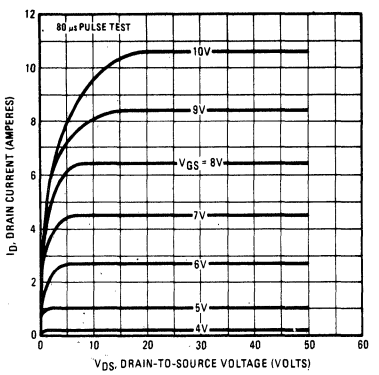


Fig. 1 – Typical Output Characteristics

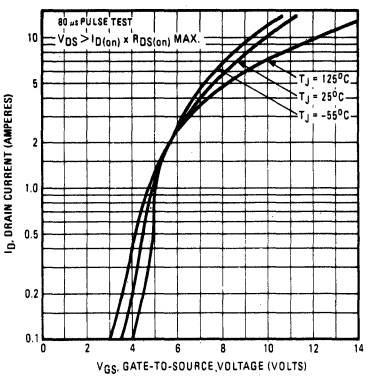


Fig. 2 – Typical Transfer Characteristics

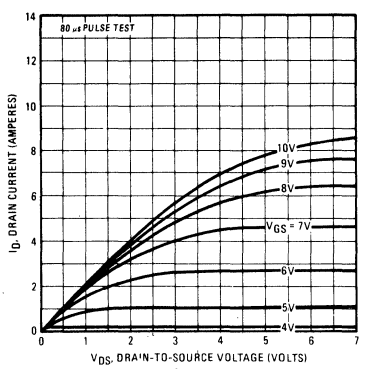


Fig. 3 – Typical Saturation Characteristics

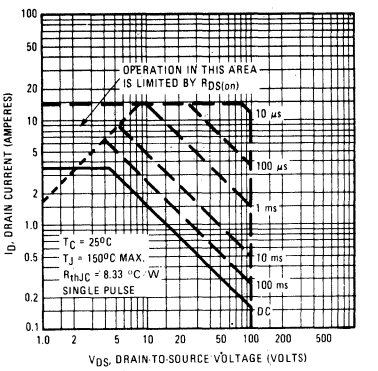


Fig. 4 – Maximum Safe Operating Area

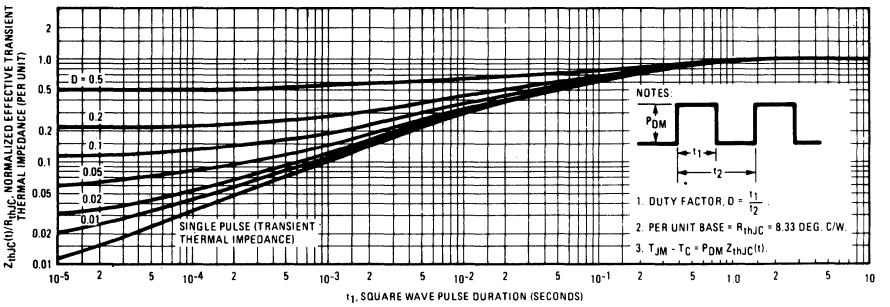


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

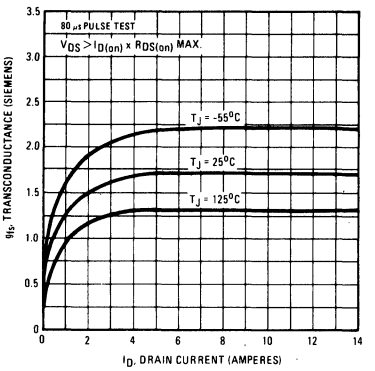


Fig. 6 – Typical Transconductance Vs. Drain Current

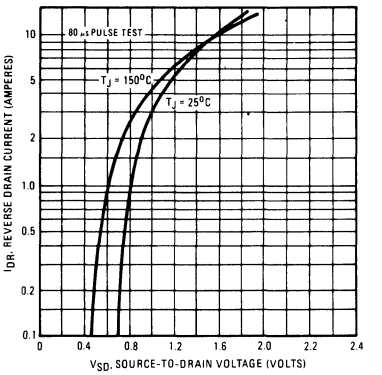


Fig. 7 – Typical Source-Drain Diode Forward Voltage

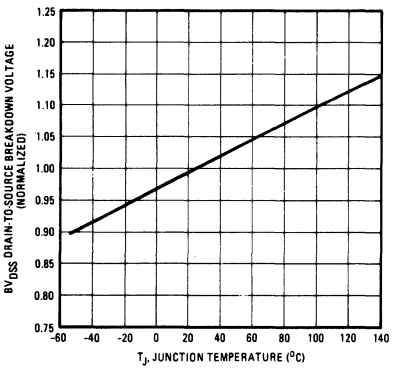


Fig. 8 – Breakdown Voltage Vs. Temperature

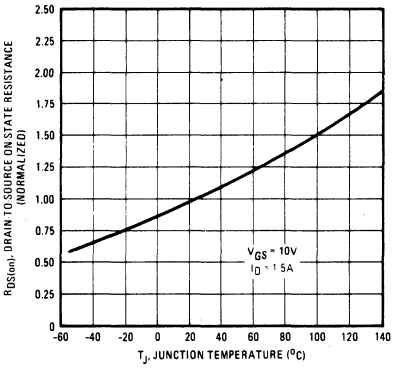


Fig. 9 – Normalized On-Resistance Vs. Temperature

2N6782

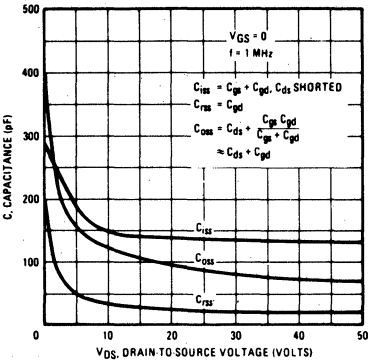


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

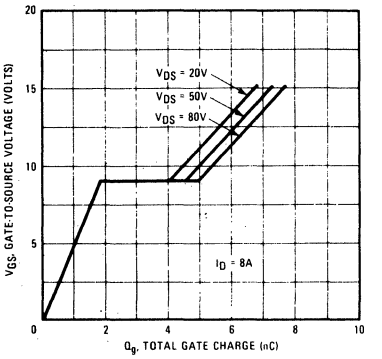


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

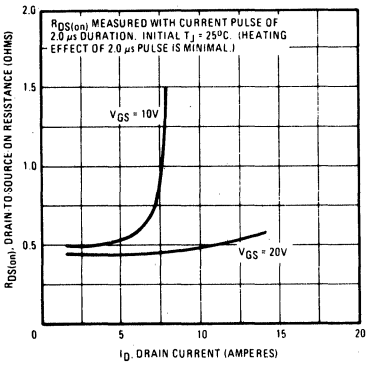


Fig. 12 – Typical On-Resistance Vs. Drain Current

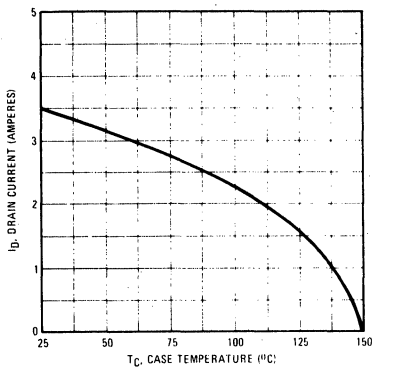


Fig. 13 – Maximum Drain Current Vs. Case Temperature

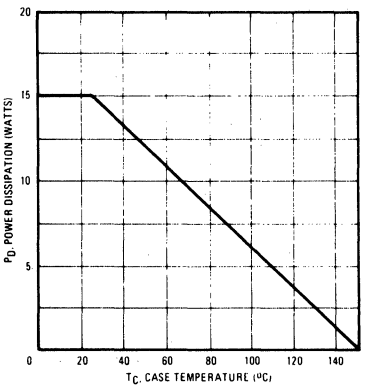
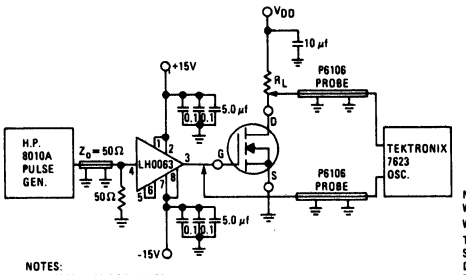
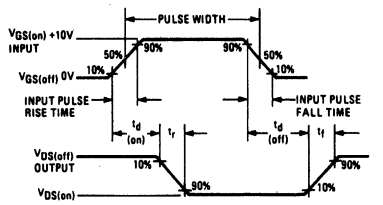


Fig. 14 – Power Vs. Temperature Derating Curve

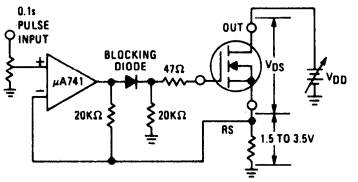


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 – Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 – Safe Operating Area Test Circuit

2N6788

File Number **1593**

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

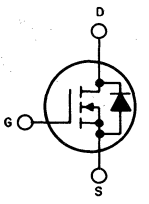
6.0A, 100V

$r_{DS}(on)$ = 0.30 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

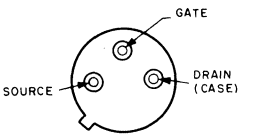
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

The 2N6788 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6788 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

Absolute Maximum Ratings

Parameter		2N6788	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	6.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	3.5*	A
I_{DM}	Pulsed Drain Current ③	24*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	6.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	24*	A
P_D @ T_C = 25°C	Max. Power Dissipation	20* (See Fig. 14)	W
	Linear Derating Factor	0.16* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 24	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	—	—	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	—	4.0*	V	V_{DS} = V_{GS}, I_D = 1.0 mA
I_{GSS}	Gate - Source Leakage Forward	—	—	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	—	—	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		—	—	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	—	—	2.10*	V	V_{GS} = 10V, I_D = 6.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	—	0.25	0.30*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 25°C
		—	—	0.54*	Ω	V_{GS} = 10V, I_D = 3.5A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.8*	—	1.8*	V	T_C = 25°C, I_S = 6.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	1.5*	2.9	4.5*	S(℧)	V_{DS} = 5V, I_D = 3.5A
C_{iss}	Input Capacitance	200*	450	600*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	100*	200	400*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	20*	50	100*	pF	
$t_{d(on)}$	Turn-On Delay Time	—	—	40*	ns	V_{DD} ≅ 35V, I_D = 3.5A, Z_o = 50Ω
t_r	Rise Time	—	—	70*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	—	—	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	—	—	70*	ns	of operating temperature.)
SOA	Safe Operating Area	20	—	—	W	V_{DS} = 80V, I_D = 250 mA, See Fig. 16.
		20	—	—	W	V_{DS} = 3.3V, I_D = 60A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	—	—	6.25*	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	230	ns	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.2	μC	T_J = 150°C, I_F = 6.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

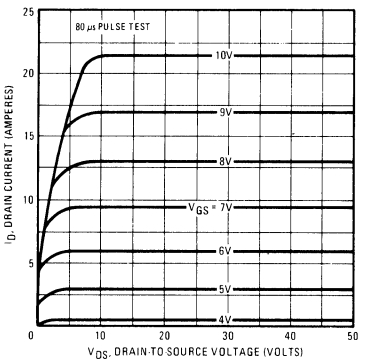


Fig. 1 — Typical Output Characteristics

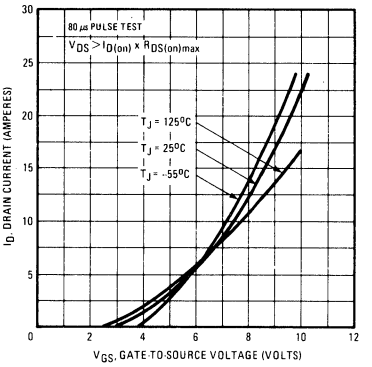


Fig. 2 — Typical Transfer Characteristics

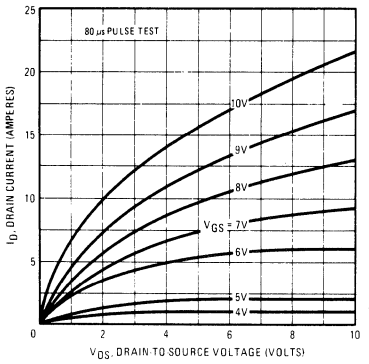


Fig. 3 — Typical Saturation Characteristics

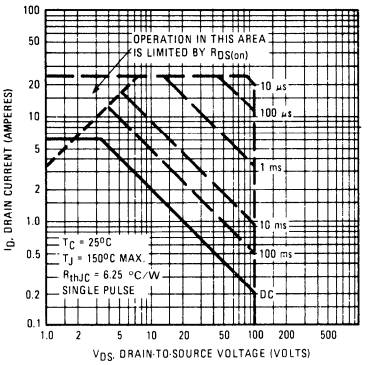


Fig. 4 — Maximum Safe Operating Area

2N6788

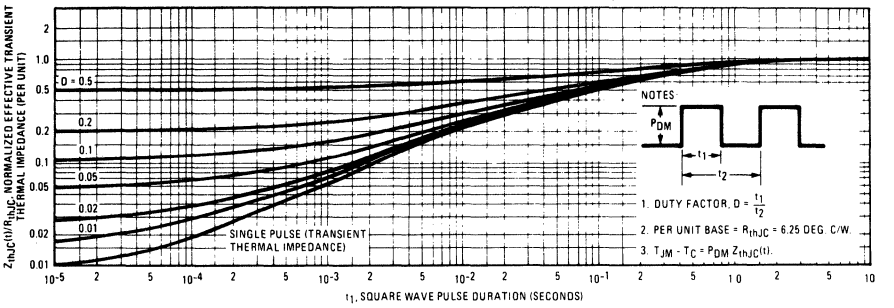


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

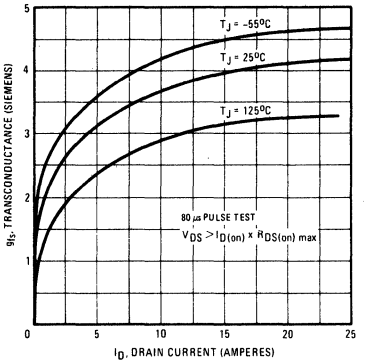


Fig. 6 – Typical Transconductance Vs. Drain Current

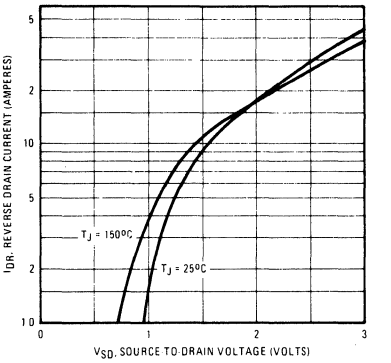


Fig. 7 – Typical Source-Drain Diode Forward Voltage

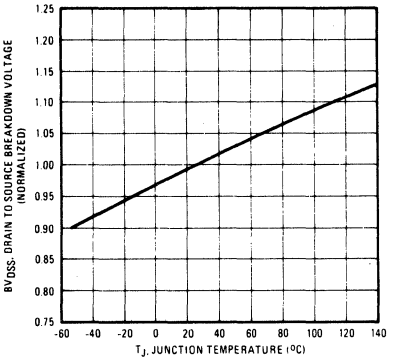


Fig. 8 – Breakdown Voltage Vs. Temperature

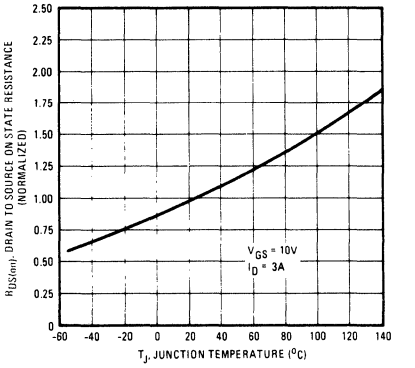


Fig. 9 – Normalized On-Resistance Vs. Temperature

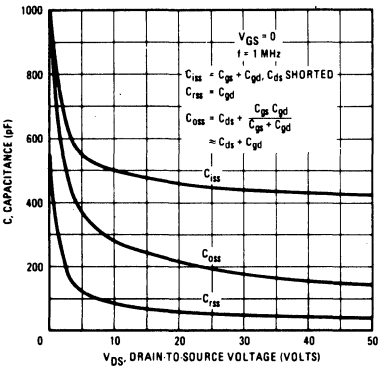


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

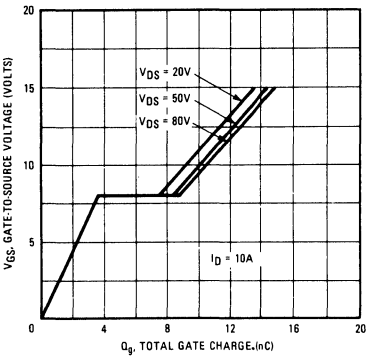


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

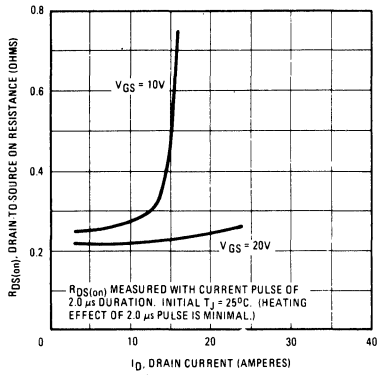


Fig. 12 – Typical On-Resistance Vs. Drain Current

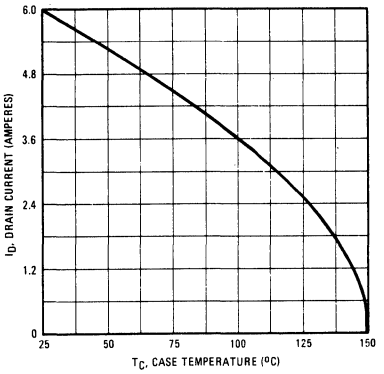


Fig. 13 – Maximum Drain Current Vs. Case Temperature

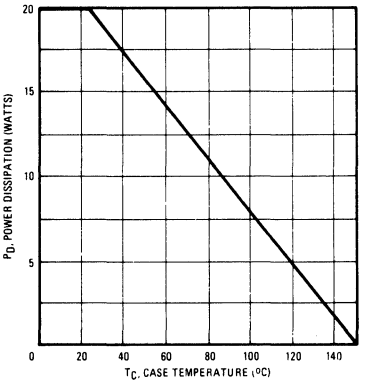
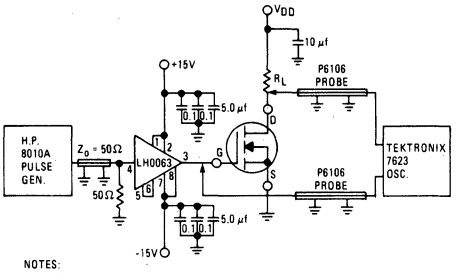
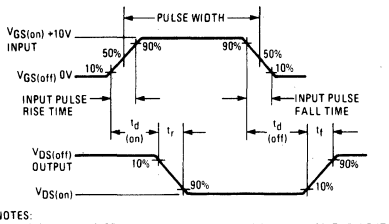


Fig. 14 – Power Vs. Temperature Derating Curve

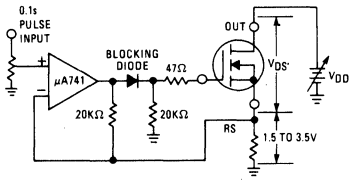


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 μs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 – Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D * R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 – Safe Operating Area Test Circuit

File Number **1594**

2N6796

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode Power Field-Effect Transistors

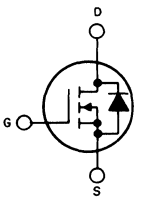
8.0A, 100V

$r_{DS}(on)$ = 0.18 Ω

Features:

- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

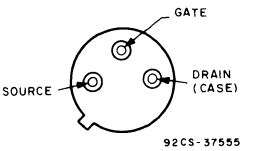
N-CHANNEL ENHANCEMENT MODE



92CS-33741

TERMINAL DIAGRAM

TERMINAL DESIGNATION



92CS-37555

JEDEC TO-205AF

The 2N6796 is an n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The 2N6796 is supplied in the JEDEC TO-205AF **(LOW PROFILE TO-39)** metal package.

Absolute Maximum Ratings

	Parameter	2N6796	Units
V_{DS}	Drain - Source Voltage ①	100*	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	100*	V
I_D @ T_C = 25°C	Continuous Drain Current	8.0*	A
I_D @ T_C = 100°C	Continuous Drain Current	5.0*	A
I_{DM}	Pulsed Drain Current ③	32*	A
V_{GS}	Gate - Source Voltage	±20*	V
I_S	Continuous Source Current (Body Diode)	8.0*	A
I_{SM}	Pulse Source Current (Body Diode) ③	32*	A
P_D @ T_C = 25°C	Max. Power Dissipation	25* (See Fig. 14)	W
	Linear Derating Factor	0.20* (See Fig. 14)	W/°C
I_{LM}	Inductive Current, Clamped	L = 100μH 32	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	−55* to 150*	°C
	Lead Temperature	300* (0.063 in. (1.6mm) from case for 10s)	°C

2N6796

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	100*	–	–	V	V_{GS} = 0V, I_D = 0.25 mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 0.5 mA
I_{GSS}	Gate - Source Leakage Forward	–	–	100*	nA	V_{GS} = 20V, V_{DS} = 0V
I_{GSS}	Gate - Source Leakage Reverse	–	–	100*	nA	V_{GS} = −20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current	–	–	250*	μA	V_{DS} = 100V, V_{GS} = 0V
		–	–	1000*	μA	V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	–	–	1.56*	V	V_{GS} = 10V, I_D = 8.0A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 25°C
		–	–	0.35*	Ω	V_{GS} = 10V, I_D = 5.0A, T_C = 125°C
V_{SD}	Diode Forward Voltage ②	0.75*	–	1.5*	V	T_C = 25°C, I_S = 8.0A, V_{GS} = 0V
g_{fs}	Forward Transconductance ②	3.0*	5.5	9.0*	S(℧)	V_{DS} = 5V, I_D = 5.0A
C_{iss}	Input Capacitance	350*	600	900*	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz
C_{oss}	Output Capacitance	150*	300	500*	pF	See Fig. 10
C_{rss}	Reverse Transfer Capacitance	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	–	–	30*	ns	V_{DD} ≅ 30V, I_D = 5.0A, Z_O = 50Ω
t_r	Rise Time	–	–	75*	ns	See Fig. 15
$t_{d(off)}$	Turn-Off Delay Time	–	–	40*	ns	(MOSFET switching times are essentially independent
t_f	Fall Time	–	–	45*	ns	of operating temperature.)
SOA	Safe Operating Area	25	–	–	W	V_{DS} = 80V, I_D = 310 mA, See Fig. 16.
		25	–	–	W	V_{DS} = 3.12V, I_D = 8.0A, See Fig. 16.

Thermal Resistance

R_{thJC}	Junction-to-Case	–	–	5.0*	°C/W	
R_{thJA}	Junction-to-Ambient	–	–	175	°C/W	Free Air Operation

Source-Drain Diode Switching Characteristics (Typical)

t_{rr}	Reverse Recovery Time	300	ns	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	1.5	μC	T_J = 150°C, I_F = 8.0A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.		

① T_J = 25°C to 150°C. ② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%. ③ Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Fig. 5).

*JEDEC registered value

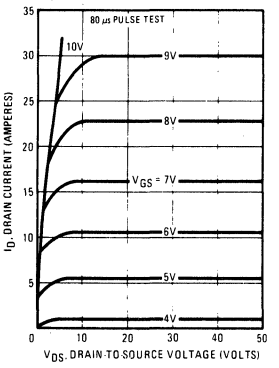


Fig. 1 – Typical Output Characteristics

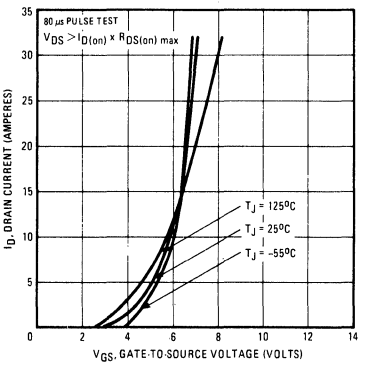


Fig. 2 – Typical Transfer Characteristics

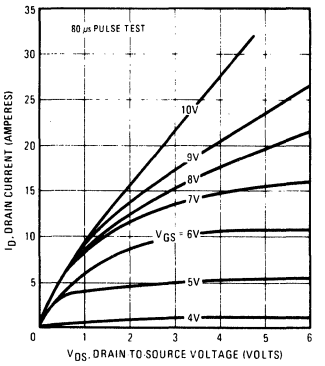


Fig. 3 – Typical Saturation Characteristics

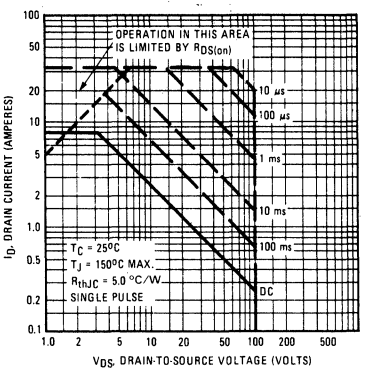


Fig. 4 – Maximum Safe Operating Area

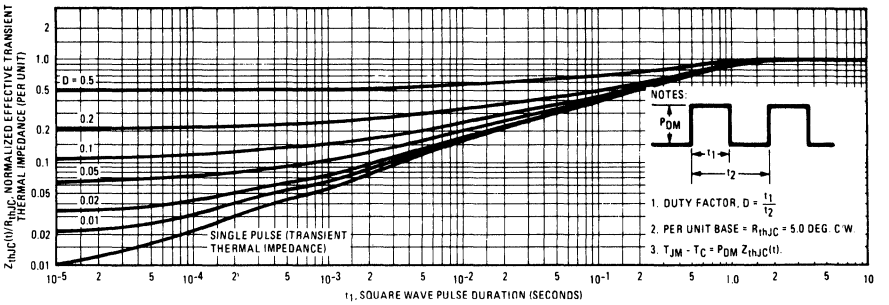


Fig. 5 – Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

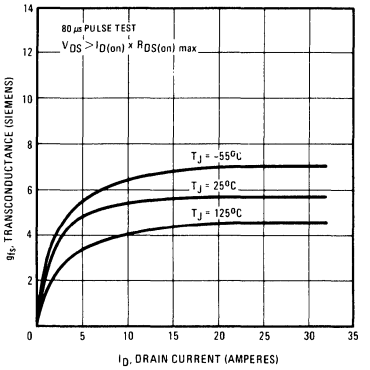


Fig. 6 – Typical Transconductance Vs. Drain Current

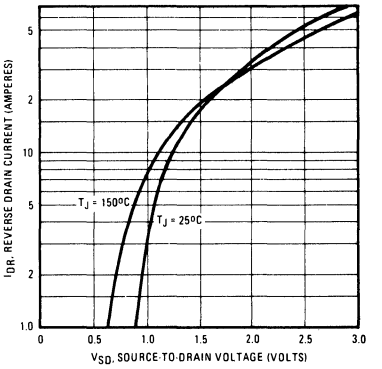


Fig. 7 – Typical Source-Drain Diode Forward Voltage

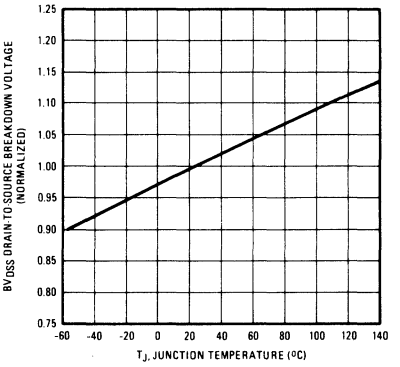


Fig. 8 – Breakdown Voltage Vs. Temperature

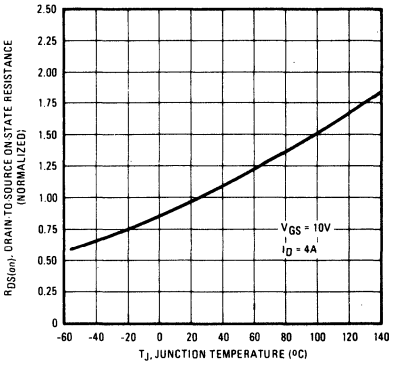


Fig. 9 – Normalized On-Resistance Vs. Temperature

2N6796

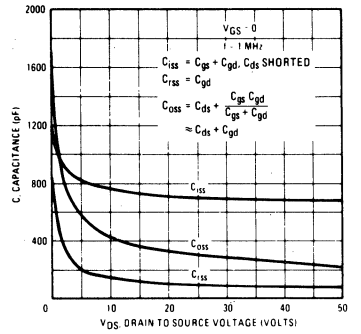


Fig. 10 – Typical Capacitance Vs. Drain-to-Source Voltage

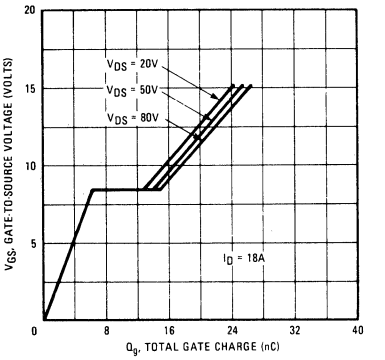


Fig. 11 – Typical Gate Charge Vs. Gate-to-Source Voltage

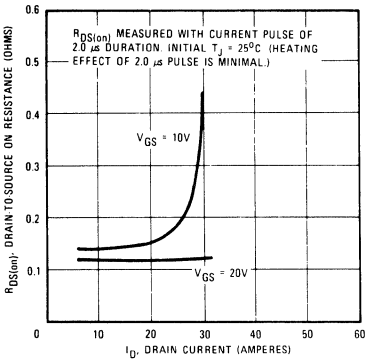


Fig. 12 – Typical On-Resistance Vs. Drain Current

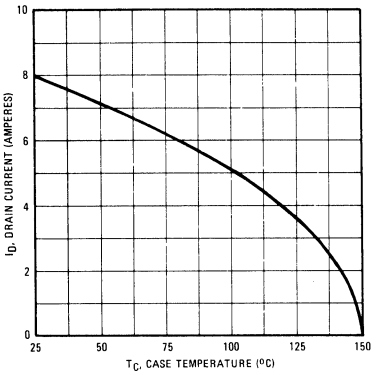


Fig. 13 – Maximum Drain Current Vs. Case Temperature

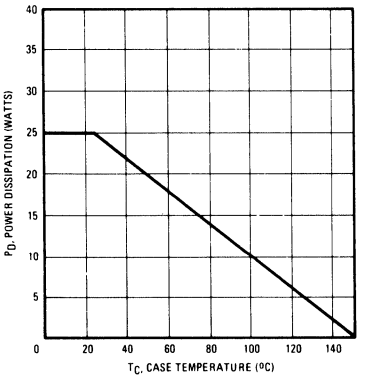
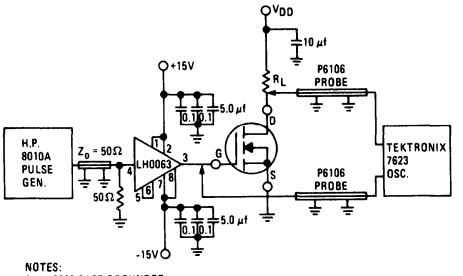
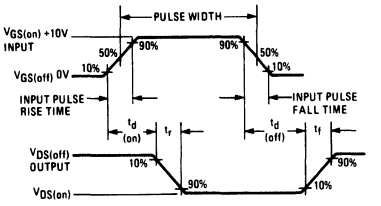


Fig. 14 – Power Vs. Temperature Derating Curve

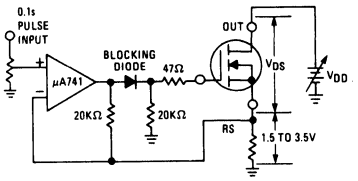


NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH = 3 µs, PERIOD = 1 ms, AMPLITUDE = 10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 15 — Switching Time Test Circuit



NOTES:
1. SET V_{DS} TO THE VALUE SPECIFIED UNDER DETAILS USING A 0.1s PULSE WIDTH WITH A MINIMUM OF 1 MINUTE BETWEEN PULSES. INCREASE V_{GS} UNTIL THE SPECIFIED VALUE OF I_D AND V_{DS} ARE OBTAINED. CASE TEMPERATURE = 25°C.
2. SELECT R_S SUCH THAT $I_D \cdot R_S = 2.5 \pm 1.0$ Vdc.

Fig. 16 — Safe Operating Area Test Circuit

Logic Level Power MOSFETs (L^2FETs)

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

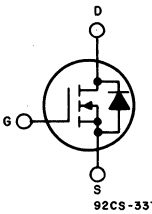
File Number **1510**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 80 V and 100 V
$r_{DS}(on)$: 1.05Ω and 1.2Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

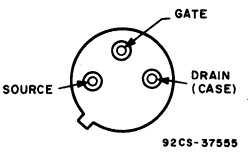
The RFL1N08L and RFL1N10L and the RFP2N08L and RFP2N10L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9524 and TA9525.

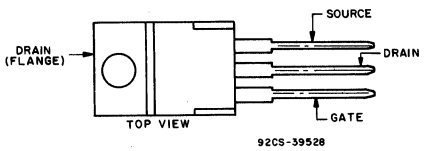
TERMINAL DESIGNATIONS

RFL1N08L
RFL1N10L



JEDEC TO-205AF

RFP2N08L
RFP2N10L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N08L	RFL1N10L		RFP2N08L	RFP2N10L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D	1	1		2	2	A
Pulsed ..... I_{DM}			5			A
POWER DISSIPATION @ T_C=25°C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25°C	0.0667	0.0667		0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N08L RFP2N08L MIN.	LIMITS RFL1N08L RFP2N08L MAX.	LIMITS RFL1N10L RFP2N10L MIN.	LIMITS RFL1N10L RFP2N10L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA, V_{GS}=0		80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=1 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V		—	1	—	—	μA
		V_{DS}=80 V		—	—	—	1	
		T_C=125° C, V_{DS}=65 V		—	50	—	—	
		V_{DS}=80 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V, V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A	RFP	—	1.05	—	1.05	V
		V_{GS}=5 V	RFL	—	1.2	—	1.2	
		I_D=2 A	RFP	—	2.5	—	2.5	
		V_{GS}=5 V	RFL	—	2.9	—	2.9	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A	RFP	—	1.05	—	1.05	Ω
		V_{GS}=5 V	RFL	—	1.2	—	1.2	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A		800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	80	—	80	
Reverse-Transfer Capacitance	C_{rss}	f=1MHz		—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r	I_D=1 A		15(typ)	45	15(typ)	45	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=∞		25(typ)	45	25(typ)	45	
Fall Time	t_f	R_{gs}=6.25 Ω, V_{GS}=5 V	RFP	20(typ)	25	20(typ)	25	
			RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N08L, RFL1N10L		—	15	—	15	°C/W
		RFP2N08L, RFP2N10L		—	5	—	5	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N08L RFP2N08L MIN.	LIMITS RFL1N08L RFP2N08L MAX.	LIMITS RFL1N10L RFP2N10L MIN.	LIMITS RFL1N10L RFP2N10L MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A, d_{IF}/d_t=50 A/μs	100(typ)		100(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFL1N08L, RFL1N10L, RFP2N08L, RFP2N10L

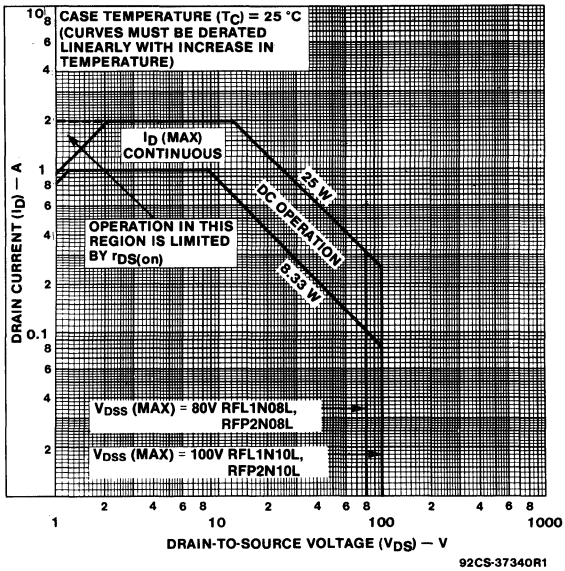


Fig. 1 — Maximum operating areas for all types.

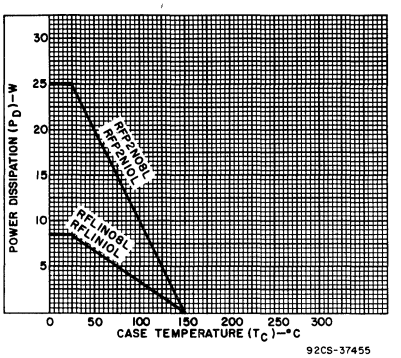


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

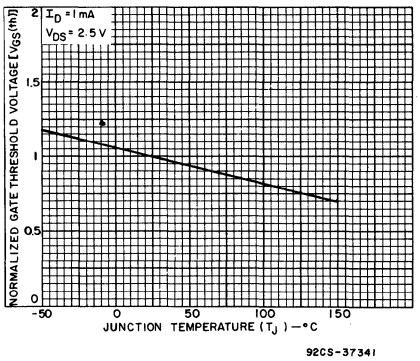


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

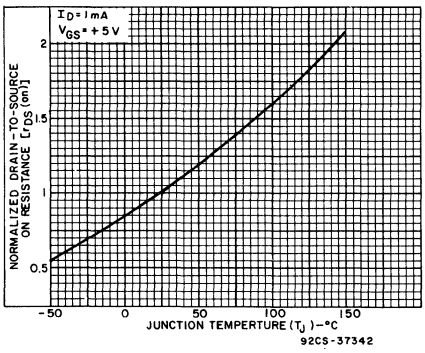


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

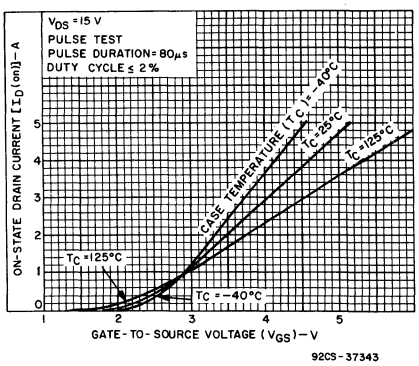


Fig. 5 — Typical transfer characteristics for all types.

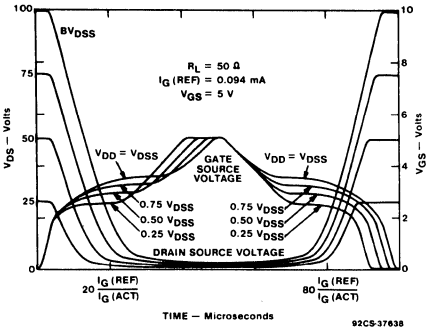


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

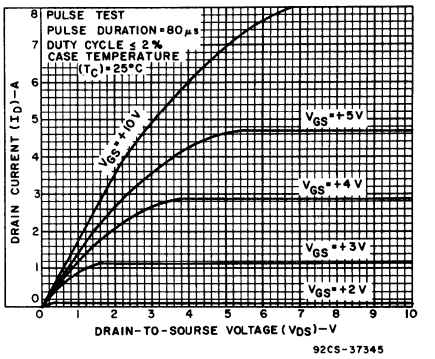


Fig. 7 — Typical saturation characteristics for all types.

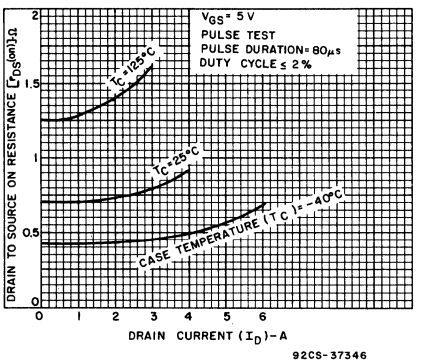


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

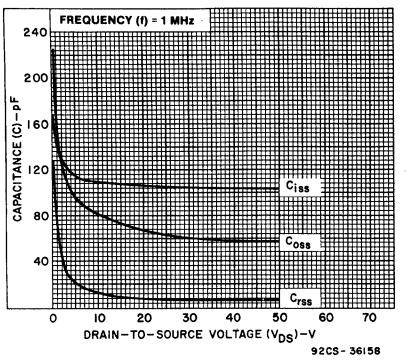


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

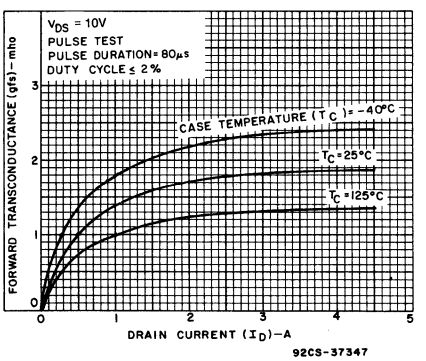


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

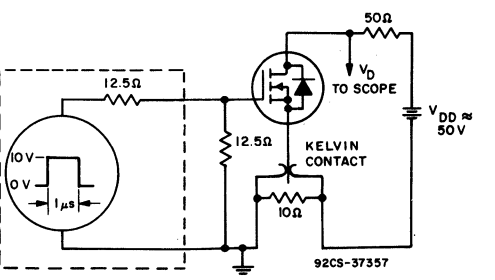


Fig. 11 — Switching Time Test Circuit.

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

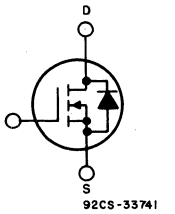
File Number **1513**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 120 V and 150 V
$r_{DS}(on)$: 1.75Ω and 1.9Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

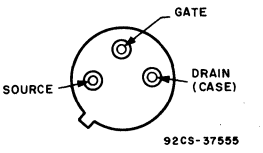
The RFL1N12L and RFL1N15L and the RFP2N12L and RFP2N15L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9528 and TA9529.

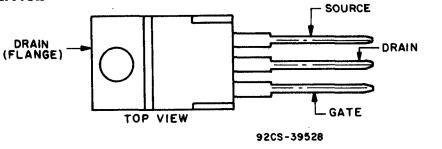
TERMINAL DESIGNATIONS

RFL1N12L
RFL1N15L



JEDEC TO-205AF

RFP2N12L
RFP2N15L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N12L	RFL1N15L		RFP1N12L	RFP2N15L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	120	150		120	150	V
DRAIN-GATE VOLTAGE (R_{GS}=1 MΩ) .... V_{DGR}	120	150		120	150	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D	1	1		2	2	A
Pulsed ..... I_{DM}			5			A
POWER DISSIPATION @ T_C=25° C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25° C	0.0667	0.0667		0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N12L RFP2N12L MIN.	LIMITS RFL1N12L RFP2N12L MAX.	LIMITS RFL1N15L RFP2N15L MIN.	LIMITS RFL1N15L RFP2N15L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA, V_{GS}=0		120	—	150	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS}, I_D=2 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100 V		—	1	—	—	μA
		V_{DS}=120 V		—	—	—	1	
		T_C=125° C, V_{DS}=100 V		—	50	—	—	
		V_{DS}=120 V		—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V, V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A	RFP	—	1.75	—	1.75	V
		V_{GS}=5 V	RFL	—	1.9	—	1.9	
		I_D=2 A	RFP	—	4.2	—	4.2	
		V_{GS}=5 V	RFL	—	4.6	—	4.6	
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A	RFP	—	1.75	—	1.75	Ω
		V_{GS}=5 V	RFL	—	1.9	—	1.9	
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V, I_D=1 A		800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	80	—	80	
Reverse-Transfer Capacitance	C_{rss}	f = 1MHz		—	20	—	20	
Turn-On Delay Time	$t_d(on)$	V_{DD}=75 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r	I_D=1 A		10(typ)	45	10(typ)	45	
Turn-Off Delay Time	$t_d(off)$	R_{gen}=∞		24(typ)	45	24(typ)	45	
Fall Time	t_f	R_{gs}=6.25 Ω, V_{GS}=5 V	RFP	20(typ)	25	20(typ)	25	
			RFL	30(typ)	50	30(typ)	50	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N12L, RFL1N15L		—	15	—	15	°C/W
		RFP2N12L, RFP2N15L		—	5	—	5	

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N12L RFP2N12L MIN.	LIMITS RFL1N12L RFP2N12L MAX.	LIMITS RFL1N15L RFP2N15L MIN.	LIMITS RFL1N15L RFP2N15L MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A, d_{IF}/d_t=50 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

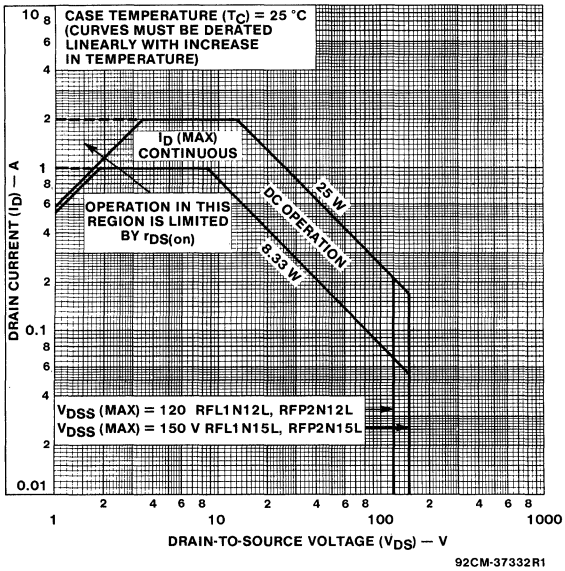


Fig. 1 — Maximum operating areas for all types.

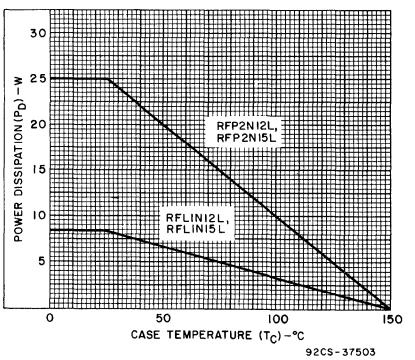


Fig. 2 — Power dissipation vs. case temperature derating curve for all types.

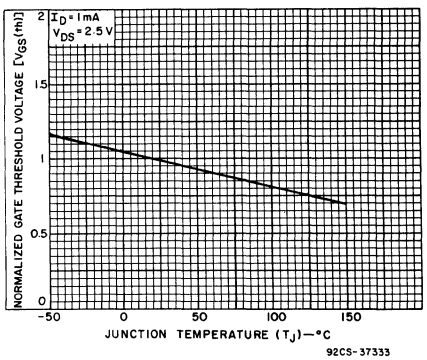


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

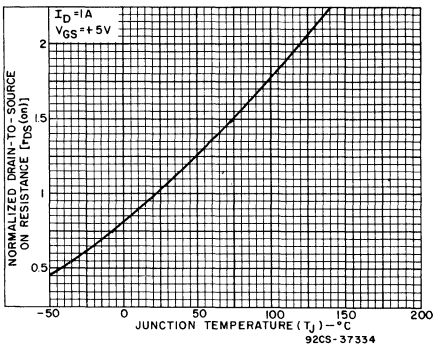


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

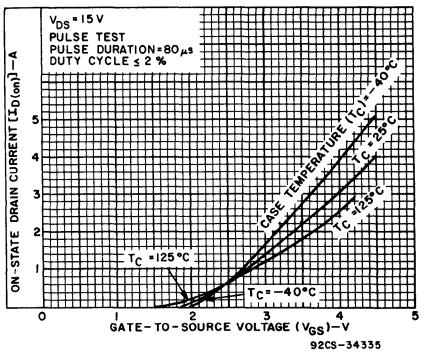


Fig. 5 — Typical transfer characteristics for all types.

RFL1N12L, RFL1N15L, RFP2N12L, RFP2N15L

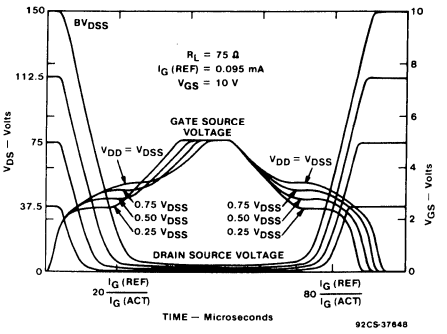


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

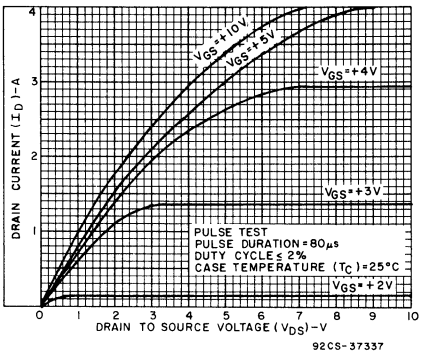


Fig. 7 — Typical saturation characteristics for all types.

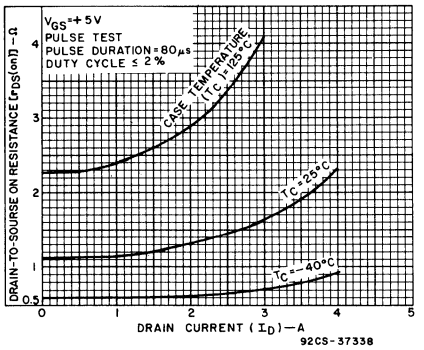


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

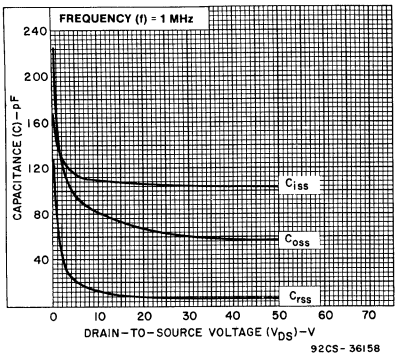


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

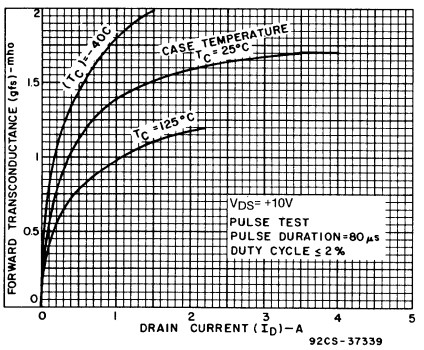


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

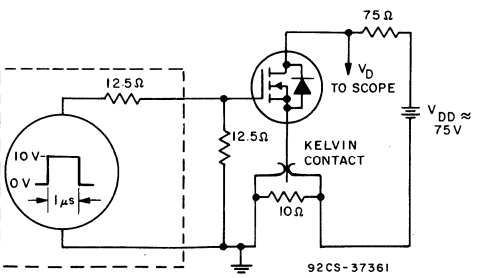


Fig. 11 — Switching Time Test Circuit.

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

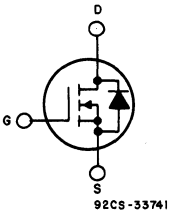
File Number **1511**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

1 and 2 A, 180 V and 200 V
$r_{DS(on)}$: 3.5 Ω and 3.65 Ω

Features:

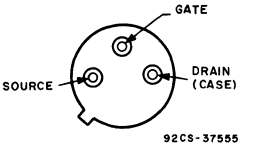
- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

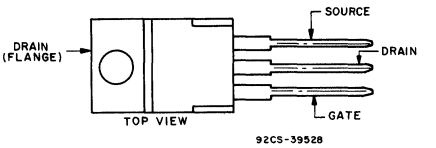
TERMINAL DESIGNATIONS

RFL1N18L
RFL1N20L



JEDEC TO-205AF

RFP2N18L
RFP2N20L



JEDEC TO-220AB

The RFL1N18L and RFL1N20L and the RFP2N18L and RFP2N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFL and RFP series were formerly RCA developmental numbers TA9532 and TA9533.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFL1N18L	RFL1N20L		RFP2N18L	RFP2N20L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D	1	1		2	2	A
Pulsed ..... I_{DM}			4			A
POWER DISSIPATION @ T_C=25° C ..... P_T	8.33	8.33		25	25	W
Derate above T_C=25° C	0.0667	0.0667		0.2	0.2	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS RFL1N18L RFP2N18L MIN.	LIMITS RFL1N18L RFP2N18L MAX.	LIMITS RFL1N20L RFP2N20L MIN.	LIMITS RFL1N20L RFP2N20L MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0		180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	$V_{GS}=V_{DS}$ I_D=1 mA		1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V		— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V		— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0		—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=1 A	RFP	—	3.5	—	3.5	V
		V_{GS}=5 V	RFL	—	3.65	—	3.65	V
		I_D=2 A	RFP	—	9	—	9	V
		V_{GS}=5 V	RFL	—	9.3	—	9.3	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=1 A	RFP	—	3.5	—	3.5	Ω
		V_{GS}=5 V	RFL	—	3.65	—	3.65	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=1 A		800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS}=25 V		—	200	—	200	pF
Output Capacitance	C_{oss}	V_{GS}=0 V		—	60	—	60	pF
Reverse-Transfer Capacitance	C_{rss}	f=1MHz		—	20	—	20	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=100 V		10(typ)	25	10(typ)	25	ns
Rise Time	t_r	I_D=1 A		10(typ)	30	10(typ)	30	ns
Turn-Off Delay Time	$t_d(off)$	R_{gen}=∞		25(typ)	40	25(typ)	40	ns
Fall Time	t_f	R_{gs}=6.25 Ω V_{GS}=5 V	RFP	20(typ)	25	20(typ)	25	ns
			RFL	30(typ)	50	30(typ)	50	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL1N18L, RFL1N20L		—	15	—	15	°C/W
		RFP2N18L, RFP2N20L		—	5	—	5	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS RFL1N18L RFP2N18L MIN.	LIMITS RFL1N18L RFP2N18L MAX.	LIMITS RFL1N20L RFP2N20L MIN.	LIMITS RFL1N20L RFP2N20L MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD}=1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=2 A d_{IF}/d_t=50 A/μs	200(typ)		200(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

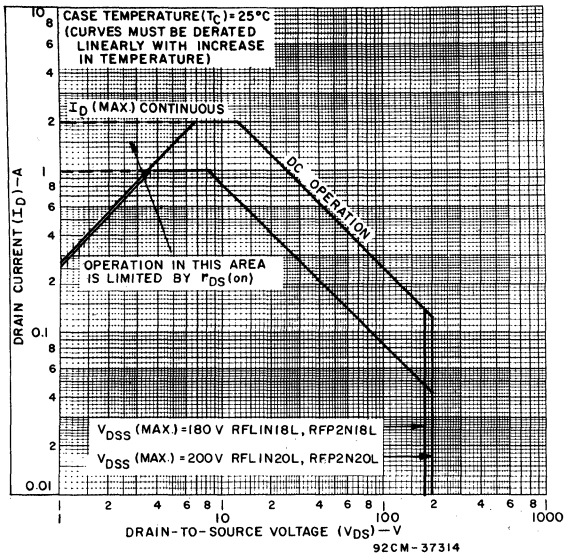


Fig. 1 — Maximum operating areas for all types.

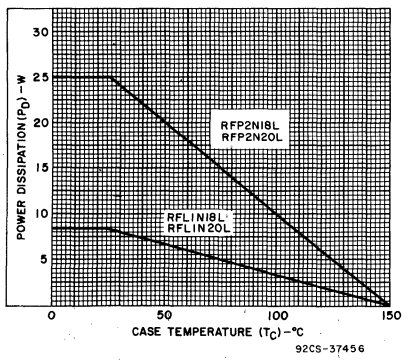


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

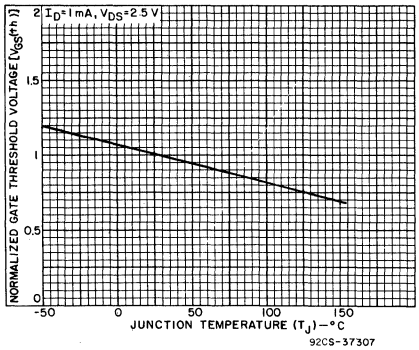


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

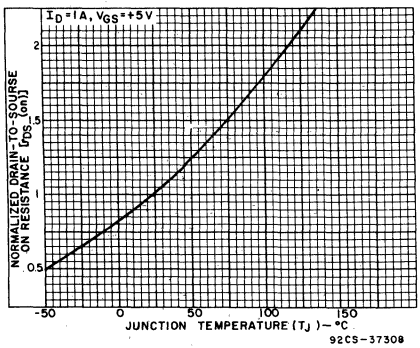


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

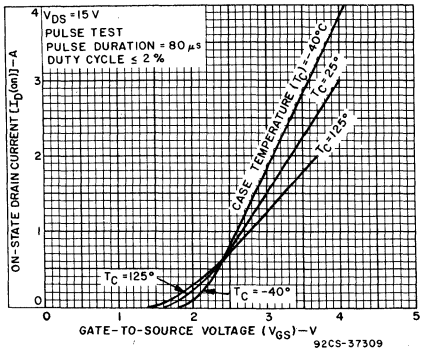


Fig. 5 — Typical transfer characteristics for all types.

RFL1N18L, RFL1N20L, RFP2N18L, RFP2N20L

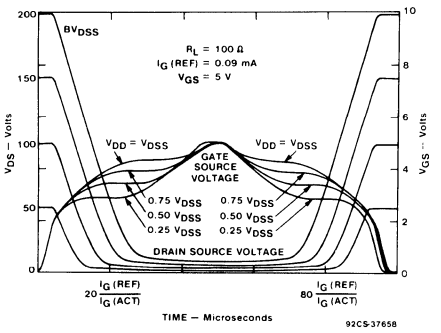


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

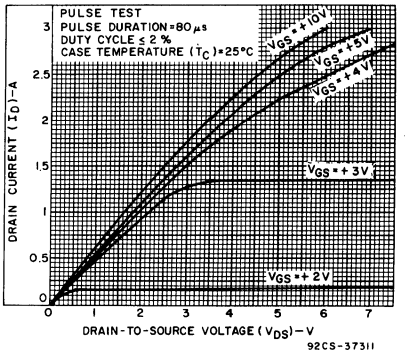


Fig. 7 — Typical saturation characteristics for all types.

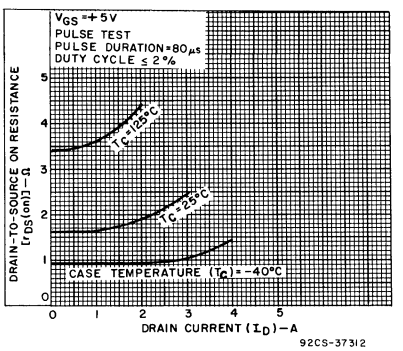


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

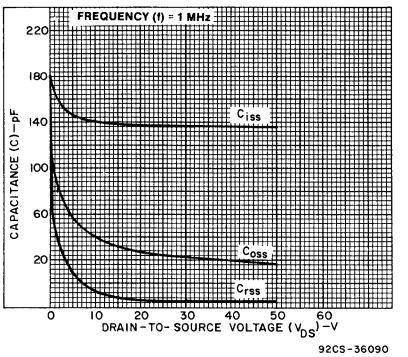


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

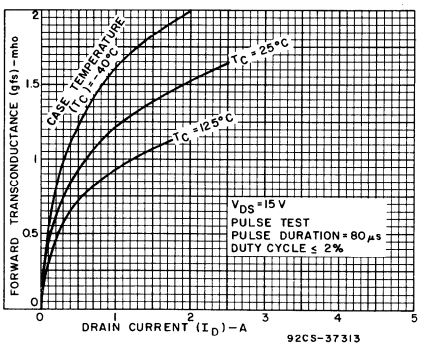


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

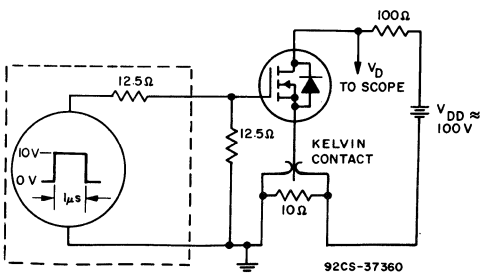


Fig. 11 — Switching Time Test Circuit.

RFL2N05L, RFL2N06L, RFP4N05L, RFP4N06L

File Number **1560**

Power Logic Level MOSFETs

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

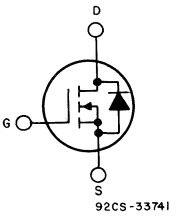
2 and 4 A, 50 V — 60 V

r_{DS}(on): 0.6Ω and 0.75Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

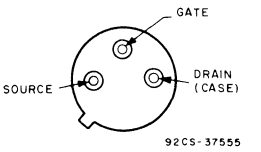
The RFL2N05L and RFL2N06L and the RFP4N05L and RFP4N06L* are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The RFL-series types are supplied in the JEDEC TO-205AF metal package and the RFP-series types in the JEDEC TO-220AB plastic package.

*The RFL and RFP series were formerly RCA developmental numbers TA9520 and TA9521, respectively.

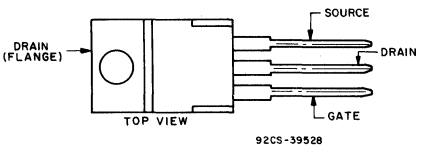
TERMINAL DESIGNATIONS

RFL2N05L
RFL2N06L



JEDEC TO-205AF

RFP4N05L
RFP4N06L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

	RFL2N05L	RFL2N06L	RFP4N05L	RFP4N06L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60	50	60	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ) ..... V_{DGR}	50	60	50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}	±10				V
DRAIN CURRENT, RMS Continuous ..... I_D	2	2	4	4	A
Pulsed ..... I_{DM}	10				A
POWER DISSIPATION @ T_C = 25°C ..... P_T	8.33	8.33	25	25	W
Derate above T_C = 25°C	0.0667	0.0667	0.2	0.2	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}	-55 to +150				°C

RFL2N05L, RFL2N06L, RFP4N05L, RFP4N06L

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05L RFP4N05L		RFL2N06L RFP4N06L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 2 mA	2	4	2	4	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125° C V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 1 A V_{GS} = 5 V	—	.8	—	.8	V
		I_D = 2 A V_{GS} = 5 V	—	2.0	—	2.0	
		I_D = 4 A V_{GS} = 7.5 V	—	4.8	—	4.8	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 1 A, V_{GS} = 5 V — RFP	—	0.6	—	0.6	Ω
		RFL	—	0.75	—	0.75	
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 1 A	800	—	800	—	mmho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	225	—	225	pF
Output Capacitance	C_{oss}		—	100	—	100	
Reverse-Transfer Capacitance	C_{rss}		—	40	—	40	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V I_D = 1 A R_{gen} = ∞ R_{gs} = 6.25 Ω V_{GS} = 5 V	10(typ)	20	10(typ)	20	ns
Rise Time	t_r		65(typ)	130	65(typ)	130	
Turn-Off Delay Time	$t_{d(off)}$		20(typ)	40	20(typ)	40	
Fall Time	t_f		30(typ)	60	30(typ)	60	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFL2N05L, RFL2N06L	—	15	—	15	°C/W
		RFP4N05L, RFP4N06L	—	5	—	5	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFL2N05L RFP4N05L		RFL2N06L RFP4N06L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 1 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 2 A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%.

RFL2N05L, RFL2N06L, RFP4N05L, RFP4N06L

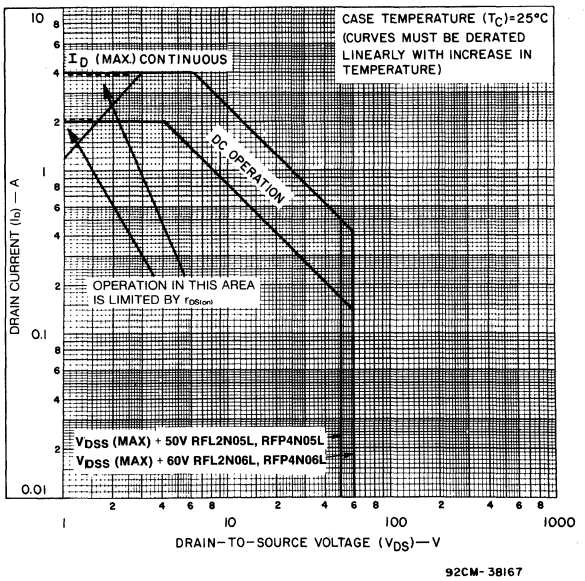


Fig. 1 - Maximum operating areas for all types.

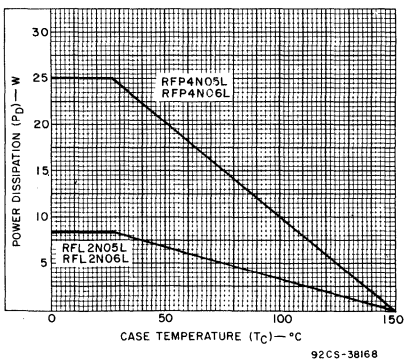


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

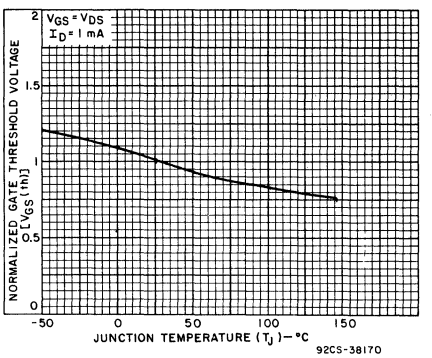


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

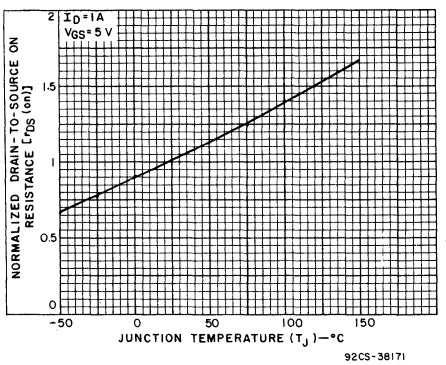


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

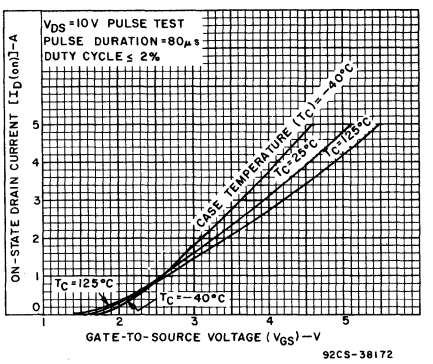


Fig. 5 - Typical transfer characteristics for all types.

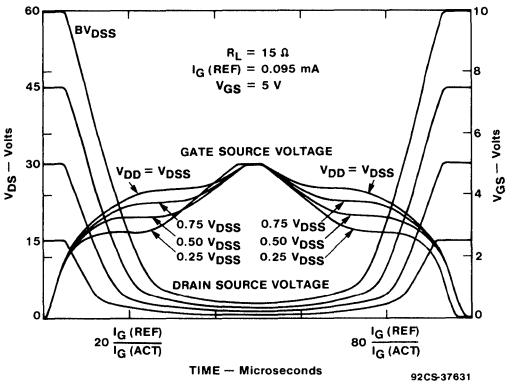


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

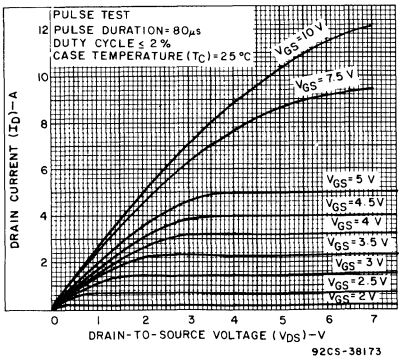


Fig. 7 - Typical saturation characteristics for all types.

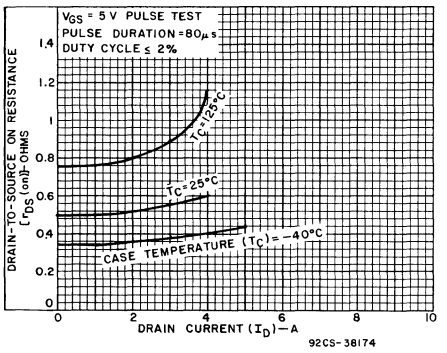


Fig. 8 - Typical drain-to-source on resistance as a function of drain current for all types.

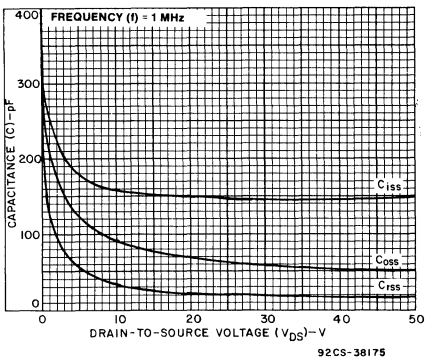


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

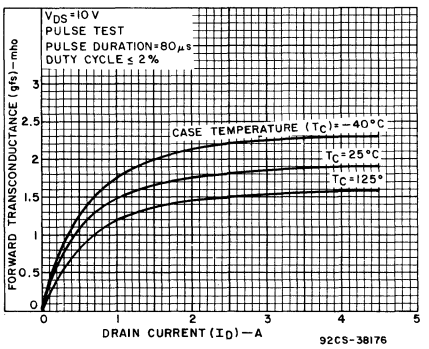


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

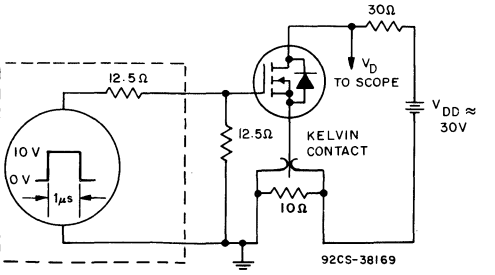


Fig. 11 - Switching Time Test Circuit.

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

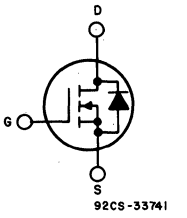
File Number **1514**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

12 A, 80 V and 100 V
$r_{DS}(on)$: 0.5Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

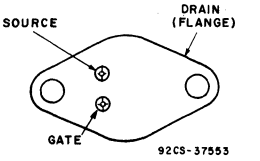
The RFM8N18L and RFM8N20L and the RFP8N18L and RFP8N20L are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

The RFM and RFP series were formerly RCA developmental numbers TA9534 and TA9535.

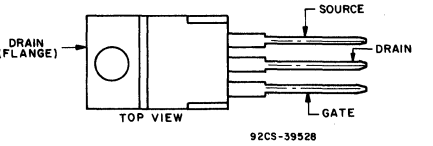
TERMINAL DESIGNATIONS

RFM8N18L
RFM8N20L



JEDEC TO-204AA

RFP8N18L
RFP8N20L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM8N18L	RFM8N20L		RFP8N18L	RFP8N20L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	180	200		180	200	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	180	200		180	200	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D			8			A
Pulsed ..... I_{DM}			20			A
POWER DISSIPATION @ T_C=25° C ..... P_T	75	75		60	60	W
Derate above T_C=25° C	0.6	0.6		0.48	0.48	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	2.0	—	2.0	V
		I_D=8 A V_{GS}=5 V	—	4.6	—	4.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	0.5	—	0.5	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=4 A	3.0	—	3.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	250	—	250	pF
Reverse-Transfer Capacitance	C_{rss}		—	100	—	100	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=4A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r		45(typ)	150	45(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	135	100(typ)	135	ns
Fall Time	t_f		60(typ)	105	60(typ)	105	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8N18L, RFM8N20L	—	1.67	—	1.67	°C/W
		RFP8N18L, RFP8N20L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=4 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	250(typ)		250(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM8N18L, RFM8N20L, RFP8N18L, RFP8N20L

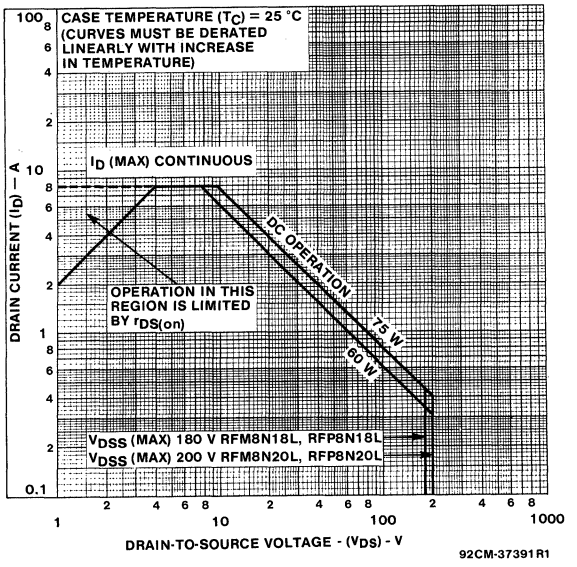


Fig. 1 — Maximum safe operating areas for all types.

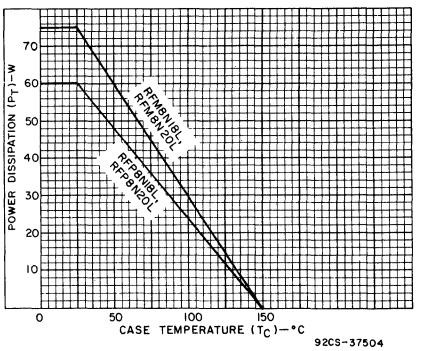


Fig. 2 — Power vs. temperature derating curve for all types.

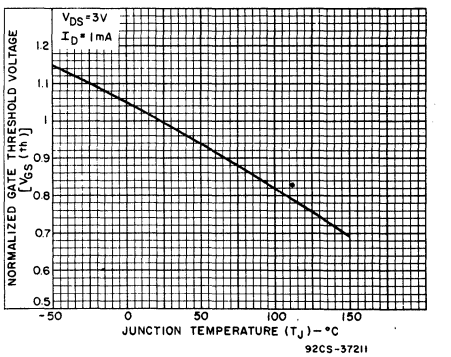


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

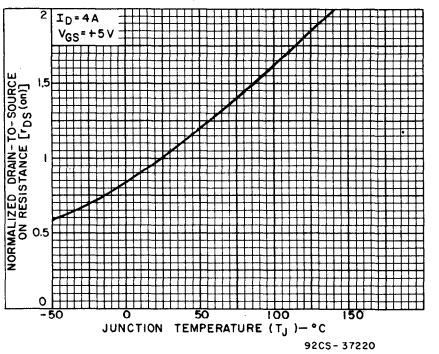


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

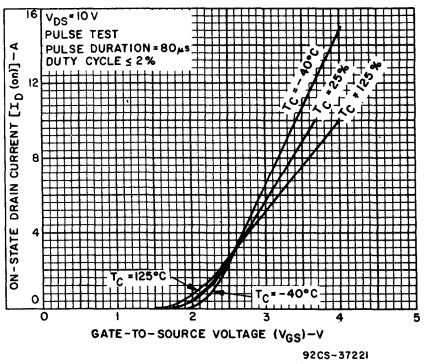


Fig. 5 — Typical transfer characteristics for all types.

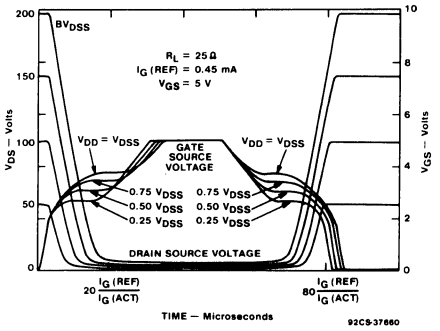


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

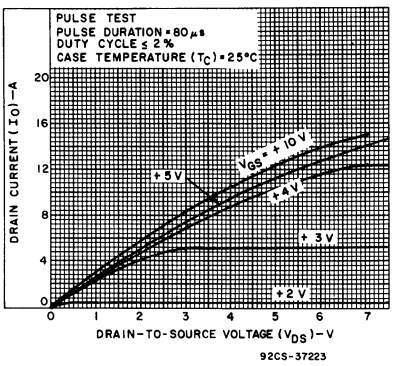


Fig. 7 — Typical saturation characteristics for all types.

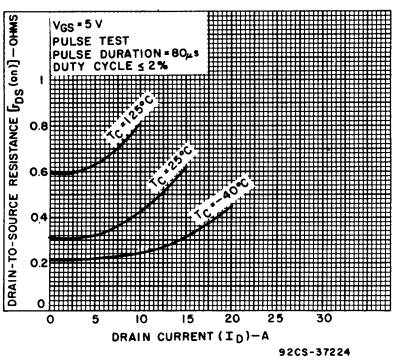


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

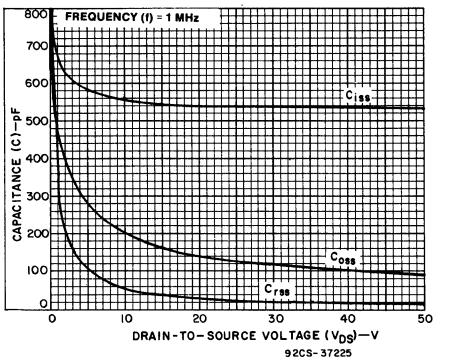


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

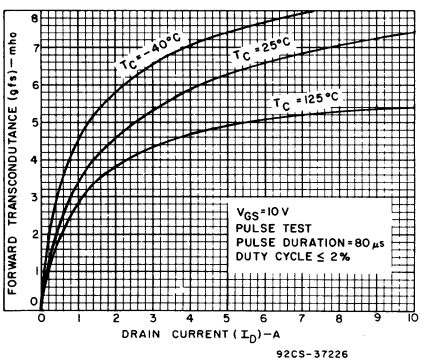


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

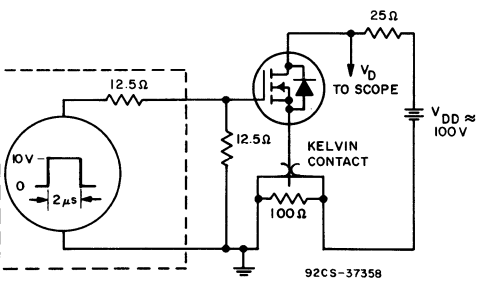


Fig. 11 — Switching Time Test Circuit.

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

File Number **1559**

Power Logic Level MOSFETs

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

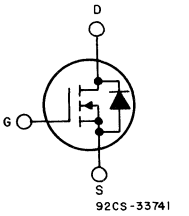
10 A, 120 V — 150 V

$r_{DS(on)}$: 0.3 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

The RFM10N12L and RFM10N15L and the RFP10N12L and RFP10N15L* are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

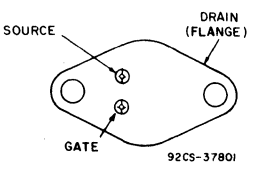
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP10N12L is F10N12L and on type RFP10N15L is F10N15L.

*The RFM and RFP series were formerly RCA developmental numbers TA9530 and TA9531, respectively.

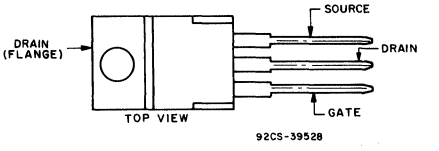
TERMINAL DESIGNATIONS

RFM10N12L
RFM10N15L



JEDEC TO-204AA

RFP10N12L
RFP10N15L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C = 25° C):*

	RFM10N12L	RFM10N15L	RFP10N12L	RFP10N15L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	120	150	120	150	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ) ..... V_{DGR}	120	150	120	150	V
GATE-SOURCE VOLTAGE ..... V_{GS}	±10				V
DRAIN CURRENT, RMS Continuous ..... I_D	10				A
Pulsed ..... I_{DM}	25				A
POWER DISSIPATION @ T_C = 25° C ..... P_T	75	75	60	60	W
Derate above T_C = 25° C	0.6	0.6	0.48	0.48	W/° C
OPERATING AND STORAGE TEMPERATURE ..... T_J, T_{stg}	-55 to +150				°C

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	120	—	150	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 2 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100 V V_{DS} = 120 V	— —	1 —	— —	— 1	μA
		T_C = 125° C V_{DS} = 100 V V_{DS} = 120 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	1.5	—	1.5	V
		I_D = 10 A V_{GS} = 5 V	—	4	—	4	V
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 5 A V_{GS} = 5 V	—	0.3	—	0.3	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1MHz	—	1200	—	1200	pF
Output Capacitance	C_{oss}		—	250	—	250	pF
Reverse-Transfer Capacitance	C_{rss}		—	60	—	60	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 75 V I_D = 5 A R_{gen} = ∞ R_{gs} = 6.25 Ω V_{GS} = 5 V	15(typ)	60	15(typ)	60	ns
Rise Time	t_r		50(typ)	135	50(typ)	135	ns
Turn-Off Delay Time	$t_{d(off)}$		90(typ)	135	90(typ)	135	ns
Fall Time	t_f		90(typ)	135	90(typ)	135	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM10N12L, RFM10N15L	—	1.67	—	1.67	°C/W
		RFP10N12L, RFP10N15L	—	2.083	—	2.083	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM10N12L RFP10N12L		RFM10N15L RFP10N15L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100 A/μs	150 (typ.)		150 (typ.)		ns

[a] Pulse Test: Width ≤ 300 μs, Duty cycle ≤ 2%

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

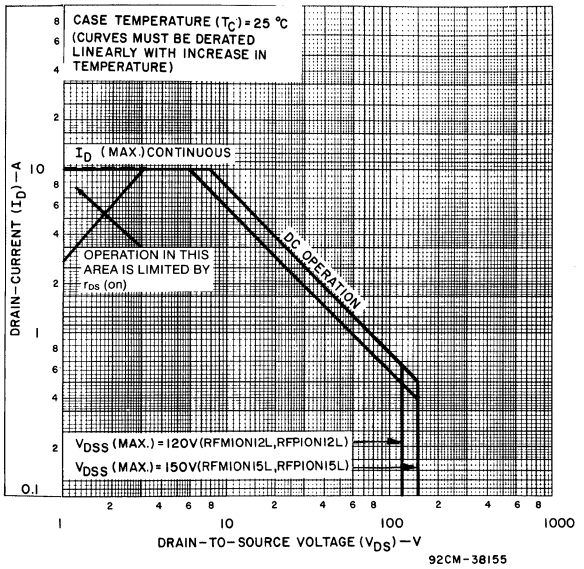


Fig. 1 - Maximum safe operating areas for all types.

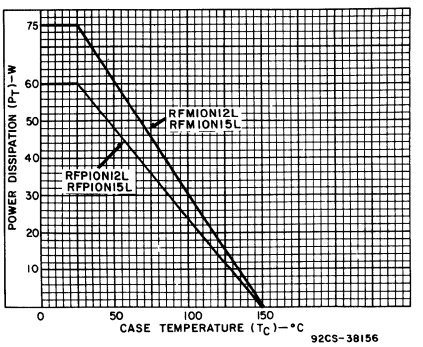


Fig. 2 - Power vs. temperature derating curve for all types.

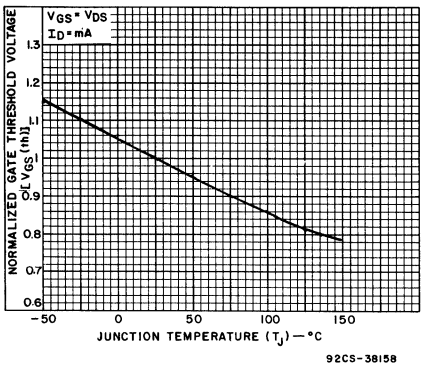


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

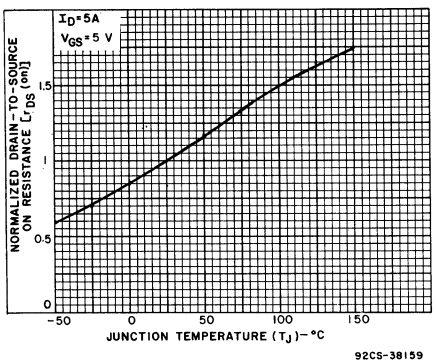


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

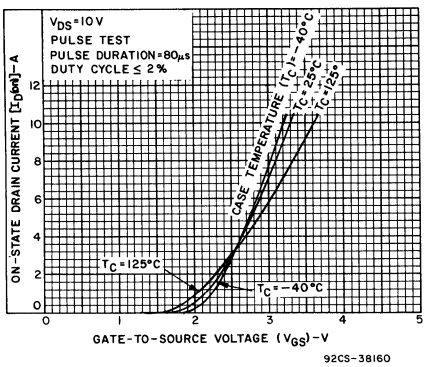


Fig. 5 - Typical transfer characteristics for all types.

RFM10N12L, RFM10N15L, RFP10N12L, RFP10N15L

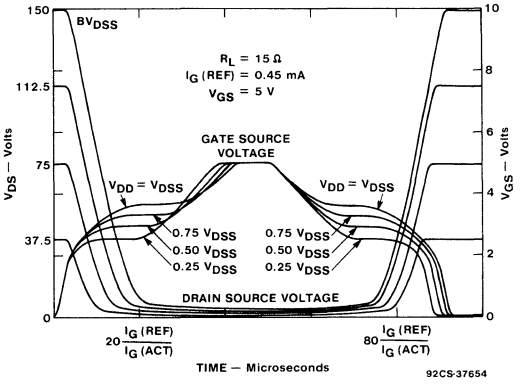


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

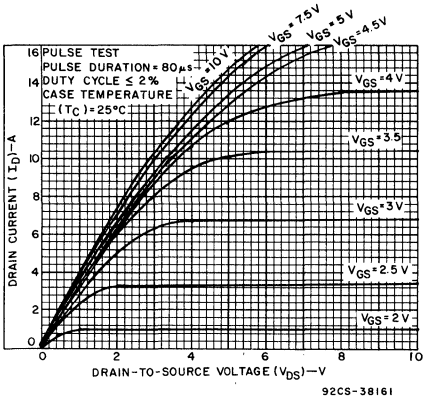


Fig. 7 - Typical saturation characteristics for all types.

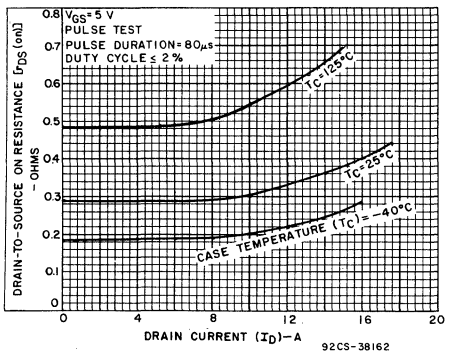


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

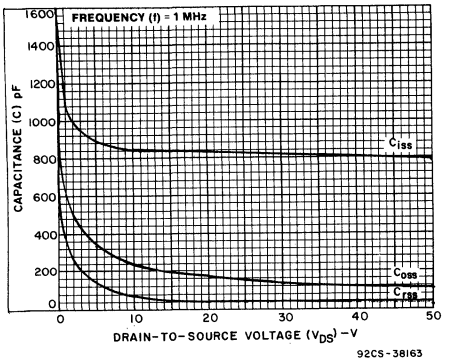


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

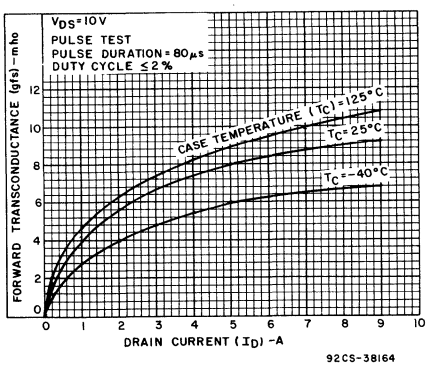


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

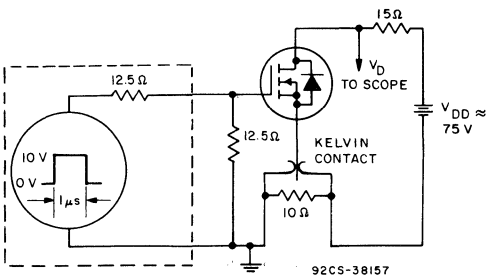


Fig. 11 - Switching Time Test Circuit.

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

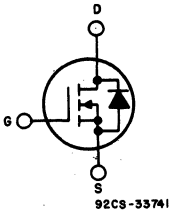
File Number **1512**

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

8 A, 180 V and 200 V
$r_{DS}(on)$: 0.2 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*



N-CHANNEL ENHANCEMENT MODE

The RFM12N08L and RFM12N10L and the RFP12N08L and RFP12N10L* are n-channel enhancement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

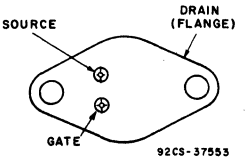
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP12N08L is F12N08L and on type RFP12N10L is F12N10L.

*The RFM and RFP series were formerly RCA developmental number TA9526 and TA9527.

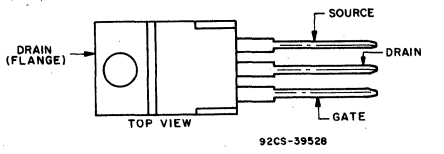
TERMINAL DESIGNATIONS

RFM12N08L
RFM12N10L



JEDEC TO-204AA

RFP12N08L
RFP12N10L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

	RFM12N08L	RFM12N10L		RFP12N08L	RFP12N10L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	80	100		80	100	V
DRAIN-GATE VOLTAGE (R_{gs}=1 MΩ) .... V_{DGR}	80	100		80	100	V
GATE-SOURCE VOLTAGE ..... V_{GS}			±10			V
DRAIN CURRENT, RMS Continuous ..... I_D			12			A
Pulsed ..... I_{DM}			30			A
POWER DISSIPATION @ T_C=25°C ..... P_T	75	75		60	60	W
Derate above T_C=25°C	0.6	0.6		0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}			-55 to +150			°C

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	80	—	100	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=65 V V_{DS}=80 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=65 V V_{DS}=80 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	1.2	—	1.2	V
		I_D=12 A V_{GS}=5 V	—	3.3	—	3.3	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=6 A V_{GS}=5 V	—	0.2	—	0.2	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=6 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	325	—	325	pF
Reverse-Transfer Capacitance	C_{rss}		—	100	—	100	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=6 A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	50	15(typ)	50	ns
Rise Time	t_r		70(typ)	150	70(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	130	100(typ)	130	ns
Fall Time	t_f		80(typ)	150	80(typ)	150	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM12N08L, RFM12N10L	—	1.67	—	1.67	°C/W
		RFP12N08L, RFP12N10L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM12N08L RFP12N08L		RFM12N10L RFP12N10L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=6 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	150(typ)		150(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

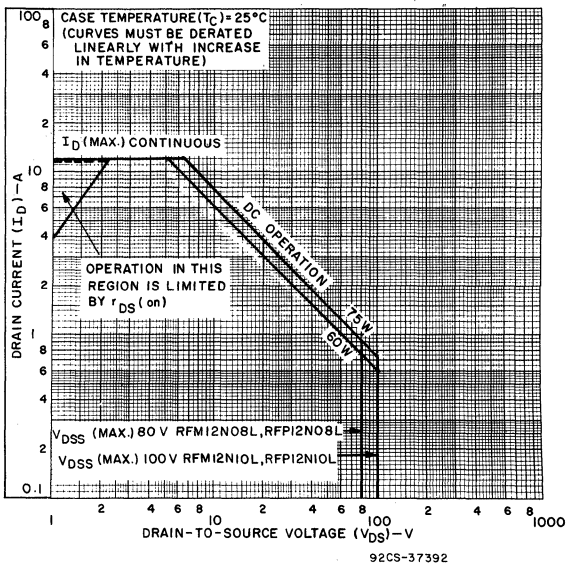


Fig. 1 — Maximum operating areas for all types.

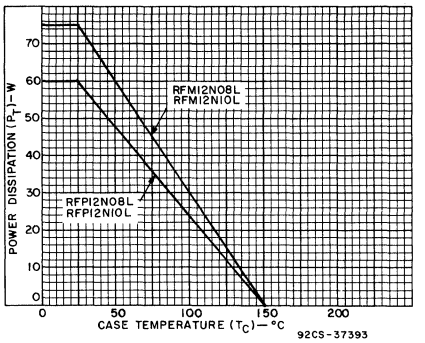


Fig. 2 — Power dissipation vs. temperature derating curve for all types.

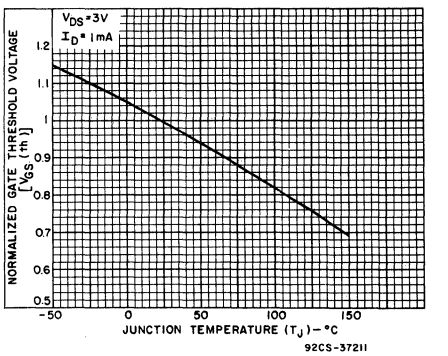


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

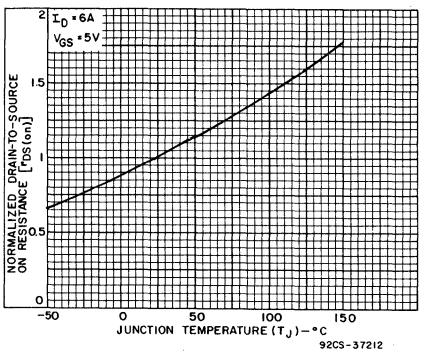


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

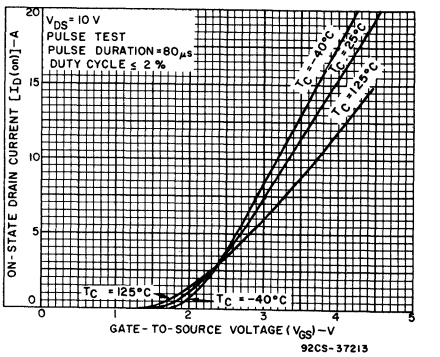


Fig. 5 — Typical transfer characteristics for all types.

RFM12N08L, RFM12N10L, RFP12N08L, RFP12N10L

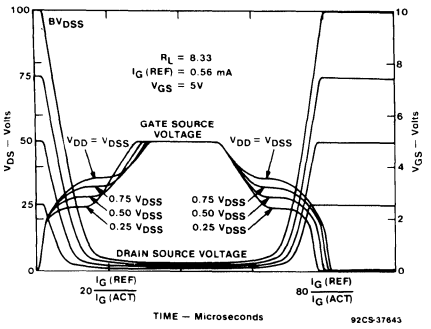


Fig. 6 - Normalized switching waveforms for constant gate-current drive.

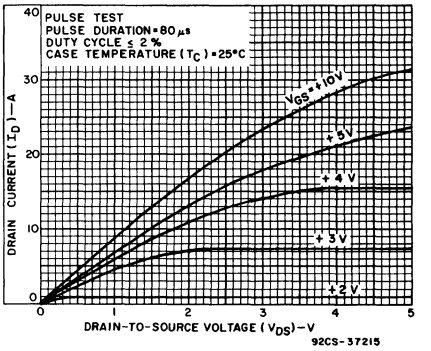


Fig. 7 — Typical saturation characteristics for all types.

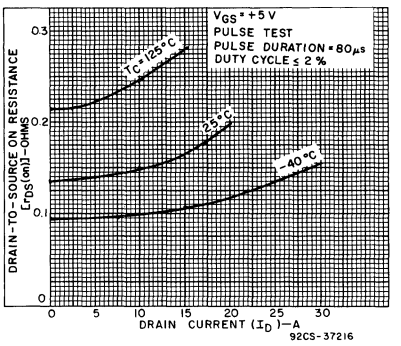


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

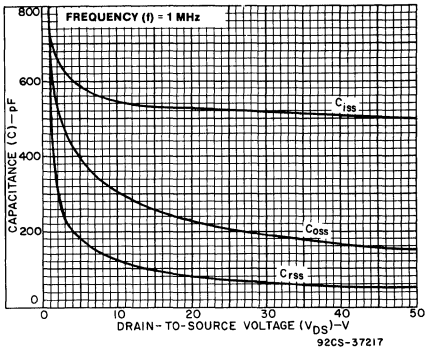


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

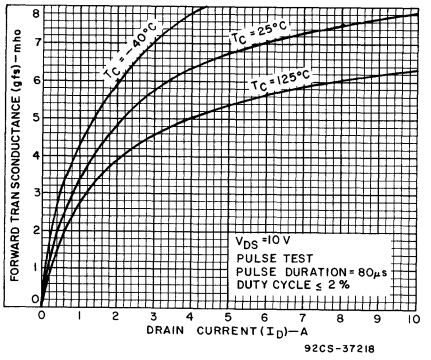


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

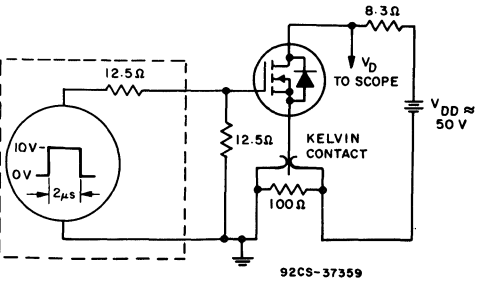


Fig. 11 — Switching Time Test Circuit.

RFM15N05L, RFM15N06L, RFP15N05L, RFP15N06L

File Number **1558**

Power Logic Level MOSFETs

N-Channel Logic Level Power Field-Effect Transistors (L^2 FET)

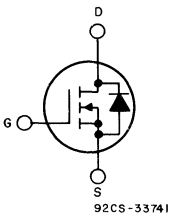
15 A, 50 and 60 V

$r_{DS}(on)$: 0.14 Ω

Features:

- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



N-CHANNEL ENHANCEMENT MODE

The RFM15N05L and RFM15N06L and the RFP15N05L and RFP15N06L* are N-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

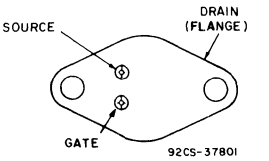
The RFM-series types are supplied in the JEDEC TO-204AA steel package and the RFP-series types in the JEDEC TO-220AB plastic package.

Because of space limitations branding (marking) on type RFP15N05L is F15NO5L and on type RFP15N06L is F15N06L.

*The RFM and RFP series were formerly RCA developmental numbers TA9522 and TA9523, respectively.

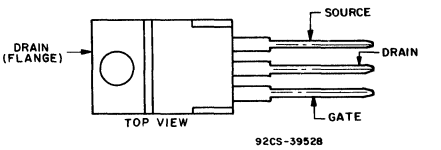
TERMINAL DESIGNATIONS

RFM15N05L
RFM15N06L



JEDEC TO-204AA

RFP15N05L
RFP15N06L



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25° C):

	RFM15N05L	RFM15N06L	RFP15N05L	RFP15N06L	
DRAIN-SOURCE VOLTAGE ..... V_{DSS}	50	60	50	60	V
DRAIN-GATE VOLTAGE (R_{gs} = 1 MΩ) ..... V_{DGR}	50	60	50	60	V
GATE-SOURCE VOLTAGE ..... V_{GS}	±10				V
DRAIN CURRENT, RMS Continuous ..... I_D	15				A
Pulsed ..... I_{DM}	40				A
POWER DISSIPATION @ T_C = 25°C ..... P_T	75	75	60	60	W
Derate above T_C = 25°C	0.6	0.6	0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE ..... T_j, T_{stg}	-55 to +150				°C

RFM15N05L, RFM15N06L, RFP15N05L, RFP15N06L

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	50	—	60	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS} I_D = 1 mA	1	2	1	2	V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V	—	1	—	—	μA
		V_{DS} = 50 V	—	—	—	1	
		T_C = 125° C V_{DS} = 40 V	—	50	—	—	
		V_{DS} = 50 V	—	—	—	50	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V V_{DS} = 0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	1.125	—	1.125	V
		I_D = 15 A V_{GS} = 5 V	—	3.0	—	3.0	
Static Drain-Source On Resistance	$r_{DS(on)}$[a]	I_D = 7.5 A V_{GS} = 5 V	—	0.14	—	0.14	Ω
Forward Transconductance	g_{fs}[a]	V_{DS} = 10 V I_D = 7.5 A	4.0	—	4.0	—	mho
Input Capacitance	C_{iss}	V_{DS} = 25 V	—	900	—	900	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	—	450	—	450	
Reverse-Transfer Capacitance	C_{rss}	f = 1 MHz	—	180	—	180	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V	16(typ)	40	16(typ)	40	ns
Rise Time	t_r	I_D = 7.5 A R_{gen} = ∞	250(typ)	325	250(typ)	325	
Turn-Off Delay Time	$t_{d(off)}$	R_{gs} = 6.25 Ω	200(typ)	325	200(typ)	325	
Fall Time	t_f	V_{GS} = 5 V	225(typ)	325	225(typ)	325	
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM15N05L, RFM15N06L	—	1.67	—	1.67	°C/W
		RFP15N05L, RFP15N06L	—	2.083	—	2.083	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM15N05L RFP15N05L		RFM15N06L RFP15N06L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}[a]	I_{SD} = 7.5A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F = 4A, d_{IF}/d_t = 100A/μs	225 (typ.)		225 (typ.)		ns

[a] Pulsed: Pulse duration = 300 μs, duty cycle = 2%.

RFM15N05L, RFM15N06L, RFP15N05L, RFP15N06L

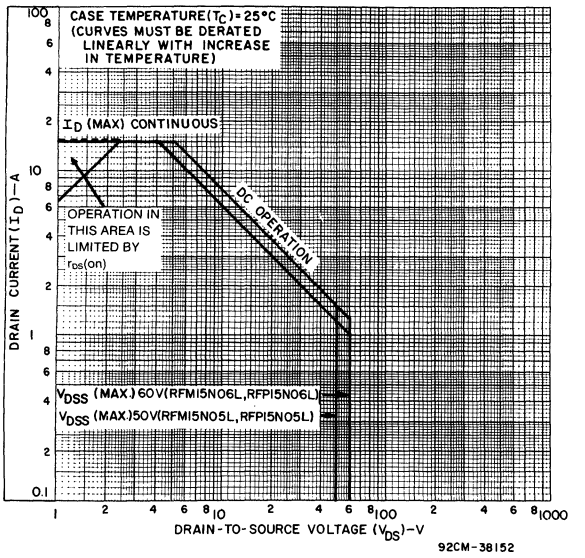


Fig. 1 - Maximum safe operating areas for all types.

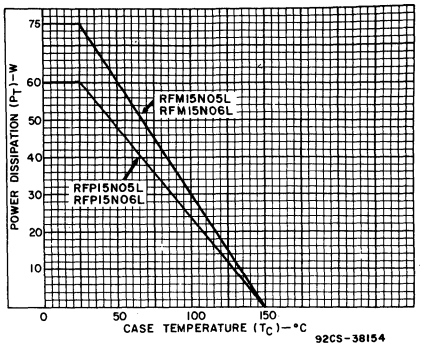


Fig. 2 - Power dissipation vs. case temperature derating curve for all types.

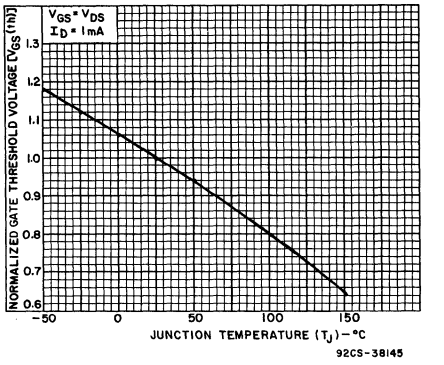


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

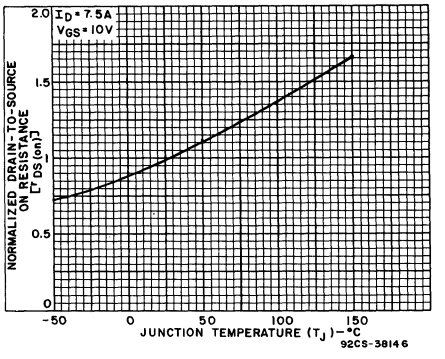


Fig. 4 - Normalized drain-to-source on resistance vs. junction temperature for all types.

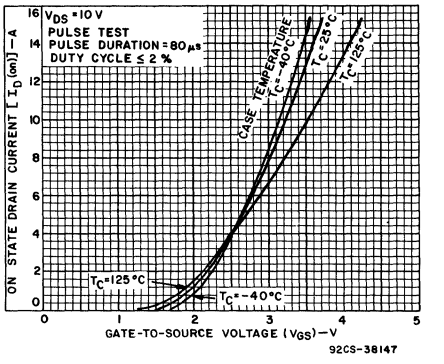


Fig. 5 - Typical transfer characteristics for all types.

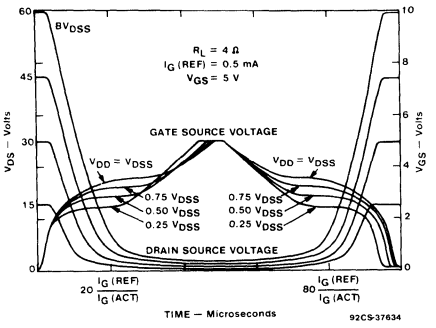


Fig. 6 - Normalized switching waveforms for constant gate-current drive. Refer to RCA Power MOSFETs PMP411A.

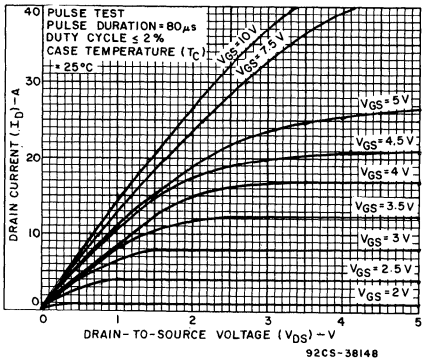


Fig. 7 - Typical saturation characteristics for all types.

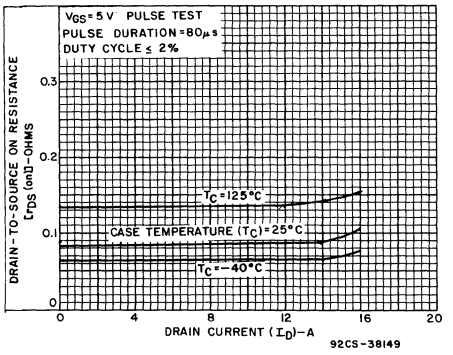


Fig. 8 - Typical drain-to-source on resistance as a function drain current for all types.

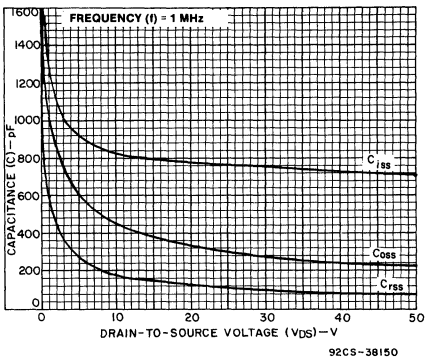


Fig. 9 - Capacitance as a function of drain-to-source voltage for all types.

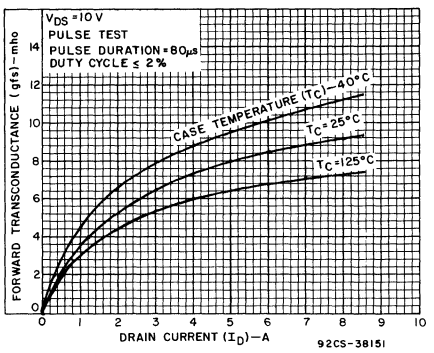


Fig. 10 - Typical forward transconductance as a function of drain current for all types.

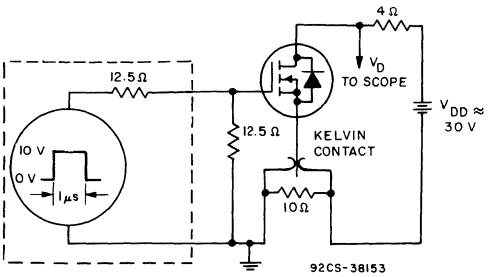


Fig. 11 - Switching Time Test Circuit.

COMFETs

RCH10N35, RCH10N40, RCP10N35, RCP10N40
Power Devices

File Number **1697**

N-Channel Enhancement Mode Conductivity-Modulated Power Field-Effect Transistors (COMFETs)

10A, 350V and 400V
$V_{DS(on)}$: 2.7 V

Features:
- *Low on-state voltage*
- *Fast switching speeds*
- *High input impedance*
- *No anti-parallel diode*

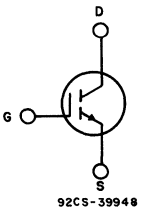
Applications:
- *Power supplies*
- *Motor drives*
- *Protective circuits*

The RCH10N35 and RCH10N40 and the RCP10N35 and RCP10N40* are n-channel enhancement-mode conductivity-modulated power field-effect transistors (COMFETs) designed for high-voltage, low on-dissipation applications such as switching regulators and motor drivers. These types can be operated directly from low-power integrated circuits.

The RCH-types are supplied in the JEDEC TO-218AC plastic package and the RCP-types in the JEDEC TO-220AB plastic package.

*The RCH and RCP series were formerly RCA Development Type Numbers TA9687 and TA9438, respectively.

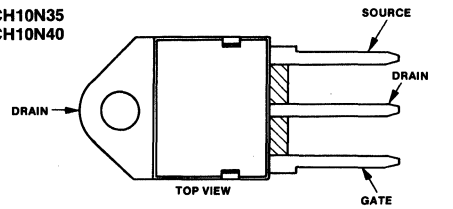
SCHEMATIC SYMBOL



N-CHANNEL ENHANCEMENT MODE

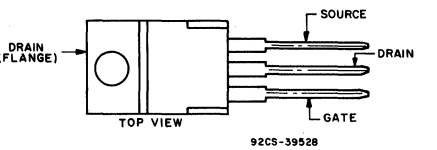
TERMINAL DESIGNATION

RCH10N35
RCH10N40



JEDEC TO-218 AC 92CS-39967

RCP10N35
RCP10N40



JEDEC TO-220AB

MAXIMUM RATINGS, *Absolute-Maximum Values* (T_C = 25°C):

	RCH10N35	RCH10N40	RCP10N35	RCP10N40	
DRAIN-SOURCE VOLTAGE, V_{DSS}	350	400	350	400	V
DRAIN-GATE VOLTAGE (R_{GS} = 1 MΩ), V_{DGR}	350	400	350	400	V
GATE-SOURCE VOLTAGE, V_{GS}	±20				V
SOURCE-DRAIN VOLTAGE, V_{SDS}	5				V
DRAIN CURRENT, RMS Continuous, I_D	10				A
Pulsed, I_{DM}	17.5				A
POWER DISSIPATION @ T_C = 25°C, P_T	75	75	60	60	W
Derate above T_C = 25°C	0.6	0.6	0.48	0.48	W/°C
OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg}	-55 to +150				°C

RCH10N35, RCH10N40, RCP10N35, RCP10N40

ELECTRICAL CHARACTERISTICS, At Case Temperature (T_C = 25° C) unless otherwise specified.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RCH10N35 RCP10N35		RCH10N40 RCP10N40		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1 mA V_{GS} = 0	350	—	400	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS} I_D = 1 mA	2	4.5	2	4.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 350 V V_{DS} = 400 V	—	250	—	—	μA
			—	—	—	250	
		T_C = 125° C V_{DS} = 350 V	—	1000	—	—	
		V_{DS} = 400 V	—	—	—	1000	
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ± 20 V V_{DS} = 0	—	100	—	100	nA
Source-Drain Leakage Current	I_{SDS}	R_{gs} = 0 Ω V_{SD} = 5 V	—	5	—	5	mA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D = 10 A V_{GS} = 10 V	—	2.7 1.9(typ.)	—	2.7 1.9(typ.)	V
		I_D = 17.5 A V_{GS} = 20 V	—	3.5 2.2(typ.)	—	3.5 2.2(typ.)	
Input Capacitance	C_{iss}	V_{DS} = 25 V V_{GS} = 0 V f = 1 MHz	—	800	—	800	pF
Output Capacitance	C_{oss}		—	150	—	150	
Reverse-Transfer Capacitance	C_{rss}		—	50	—	50	
Turn-On Delay Time	$t_d(on)$	T_C = 100° C V_{DS} = 350 V I_D = 10 A R_{gen}=R_{gs}=100Ω V_{GS} = 10 V See Fig. 9	—	100	—	100	ns
Rise Time	t_r		—	600	—	600	
Turn-Off Delay Time	$t_d(off)$		—	500	—	500	
Fall Time	t_f		—	1000	—	1000	
Turn-Off Energy Loss Per Cycle (off switching dissipation = E_{off} x frequency)	E_{off}	I_D = 10 A V_{CL} = 300 V L = 50 μH T_J = 100° C V_{GS} = 10 V R_g = 50 Ω	330(typ.)		330(typ.)		μJ
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RCH10N35, RCH10N40	—	1.67	—	1.67	°C/W
		RCP10N35 RCP10N40	—	2.083	—	2.083	

[a]Pulsed Test: Width ≤ 300 μs, Duty Cycle ≤ 2%.

RCH10N35, RCH10N40, RCP10N35, RCP10N40

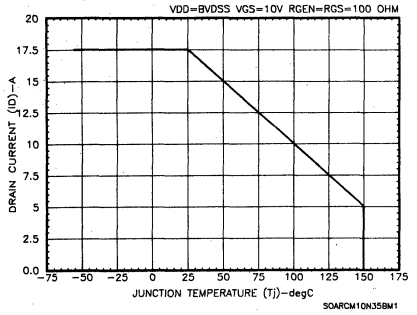


Fig. 1 - Maximum operating area for all types.

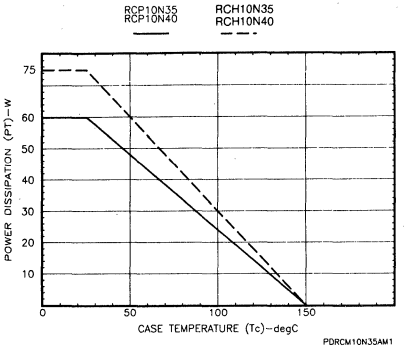


Fig. 2 - Power dissipation vs. temperature derating curve for all types.

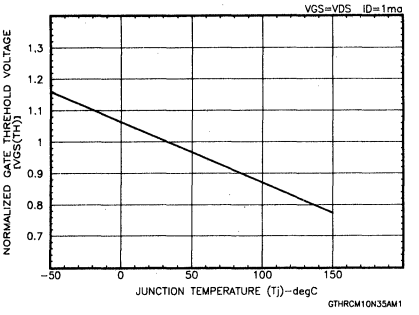


Fig. 3 - Typical normalized gate threshold voltage as a function of junction temperature for all types.

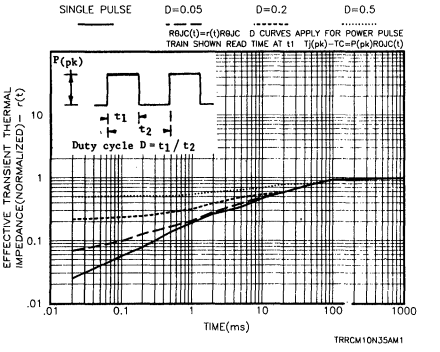


Fig. 4 - Normalized thermal response characteristics for all types.

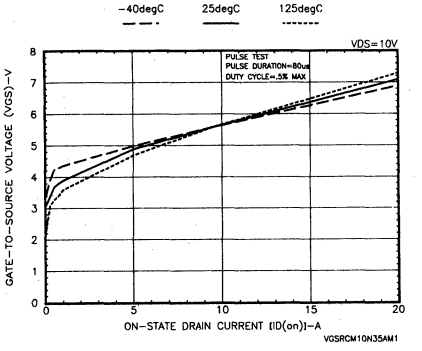


Fig. 5 - Typical transfer characteristics for all types.

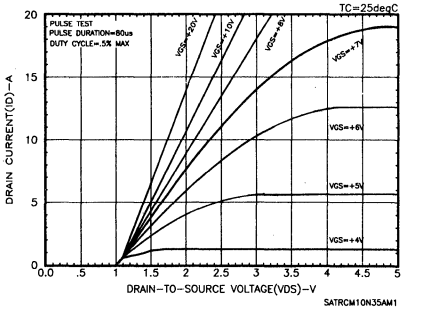


Fig. 6 - Typical saturation characteristics for all types.

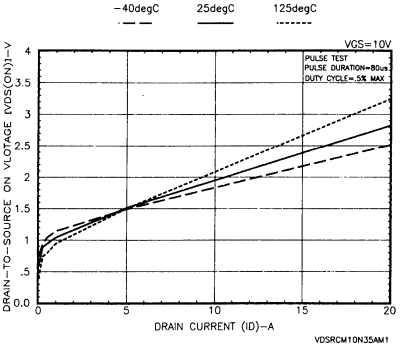


Fig. 7 - Typical drain-to-source on voltage as a function of drain current for all types.

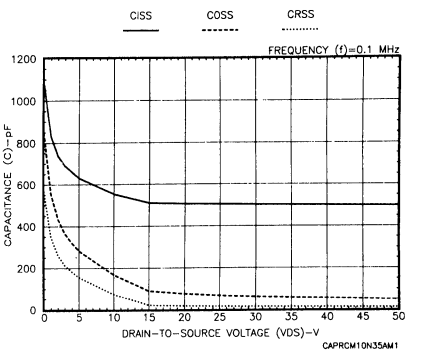


Fig. 8 - Capacitance as a function of drain-to-source voltage for all types.

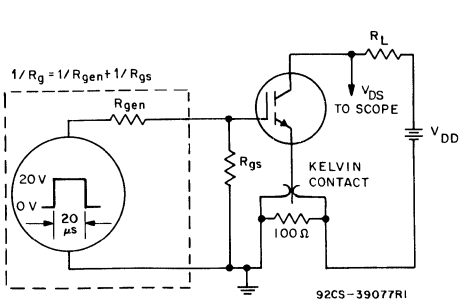


Fig. 9 - Resistive switching time test circuit.

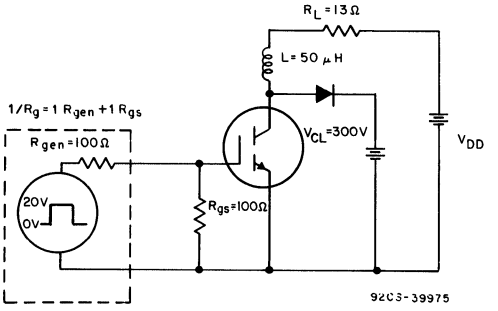


Fig. 10 - Inductive switching test circuit.

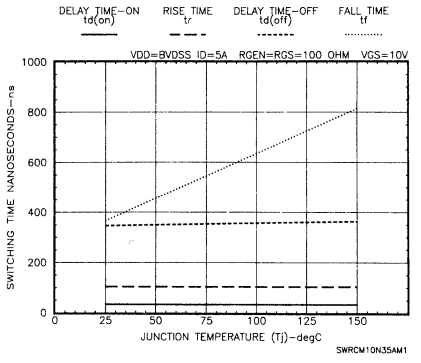


Fig. 11 - Typical resistive switching-time characteristics vs. temperature.

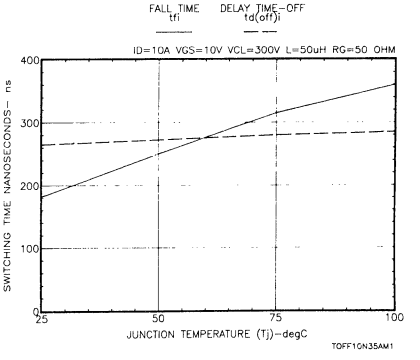


Fig. 12 - Typical clamped inductive turn-off switching time.

RCH10N35, RCH10N40, RCP10N35, RCP10N40

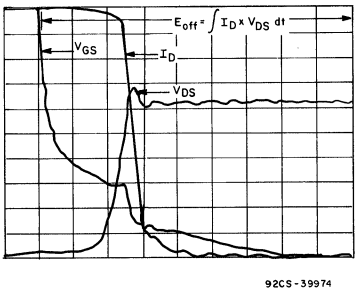


Fig. 13 - Typical inductive switching waveforms.

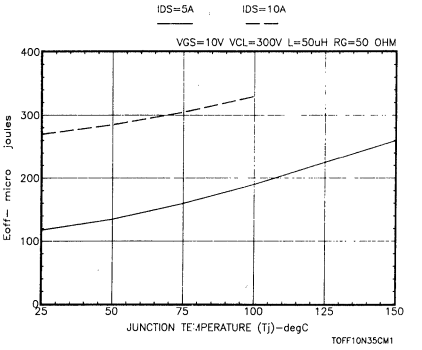


Fig. 14 - Typical clamped inductive turn-off switching loss/cycle.

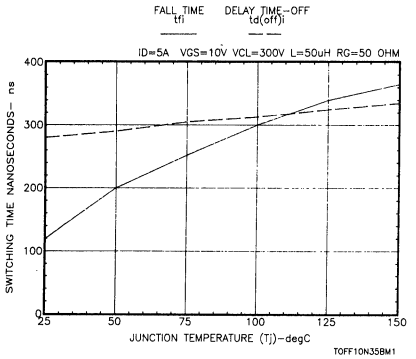


Fig. 15 - Typical clamped inductive turn-off switching time.

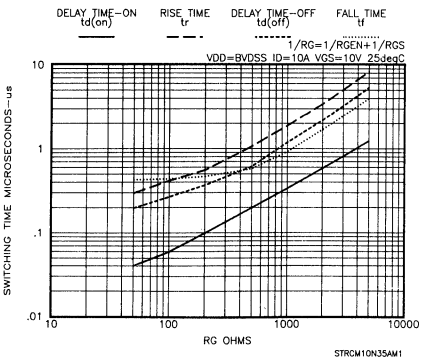


Fig. 16 - Typical resistive switching-time characteristics vs. gate driving resistance (R_g).

Power MOSFET Chips

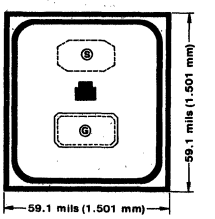
PCF2N05 File Number **1522**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 2 A, 0.75 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09378*
- *Device types that are derived from PCF2N05-*
  RFL2N05 *RFP4N05*
  RFL2N06 *RFP4N06*



ATTACH AREAS: 92CS-39992
Ⓢ Source, Ⓖ Gate } 0.010" x 0.020" (0.254 mm x 0.508 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N05		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=40 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A V_{GS}=10 V	—	0.75	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1756**

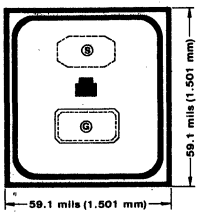
PCF2N05L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 2 A, 0.75 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09520*
- *Device types that are derived from PCF2N05L-*
  RFL2N05L *RFP4N05L*
  RFL2N06L *RFP4N06L*



ATTACH AREAS: 92CS-39992
Ⓢ Source } 0.010" x 0.020" (0.254 mm x 0.508 mm)
Ⓖ Gate
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N05L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=40 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A V_{GS}=5 V	—	0.75	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF2N08

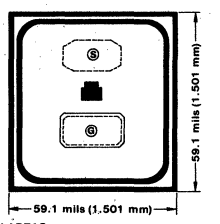
File Number **1458**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 2 A, 1.05 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09282*
- *Device types that are derived from PCF2N08-*
  RFL1N08 *RFP2N08*
  RFL1N10 *RFP2N10*



ATTACH AREAS: 92CS-39992
Ⓢ Source, Ⓖ Gate } 0.010" x 0.020" (0.254 mm x 0.508 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=1 A V_{GS}=10 V	—	1.05	V
g_{fs}[a]	V_{DS}=10 V I_D 1 A	400	—	mmho

[a]Pulsed; pulse duration = 300 *us* max., duty factor = 2%.

File Number **1757**

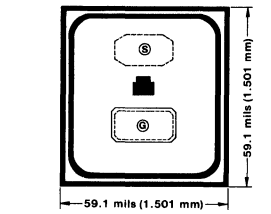
PCF2N08L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 2 A, 1.05 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09524*
- *Device types that are derived from PCF2N08L-*
  RFL1N08L RFP2N08L
  RFL1N10L RFP2N10L



CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N08L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=65 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A V_{GS}=5 V	—	1.05	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF2P08

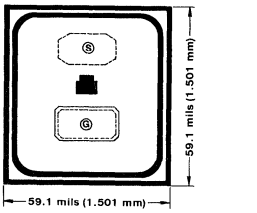
File Number **1750**

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 2 A, 3.0 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number 09400*
- *Device types that are derived from PCF2P08-*
  RFM2P08 *RFP2P08*
  RFM2P10 *RFP2P10*



CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2P08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A V_{GS}=-10 V	—	-3.0	V
g_{fs}[a]	V_{DS}=-10 V I_D=1 A	0.1	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1425**

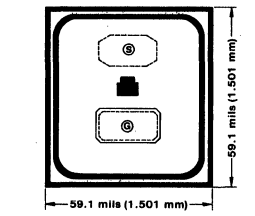
PCF2N12

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

120 V, 2 A, 1.75 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09196*
- *Device types that are derived from PCF2N12-*
  RFL1N12 RFP2N12
  RFL1N15 RFP2N15



CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N12		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A V_{GS}=10 V	—	1.75	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a] Pulsed; pulse duration = 300 *us* max., duty factor = 2%.

PCF2N12L

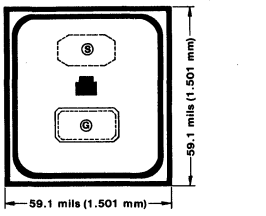
File Number **1758**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

120 V, 2 A, 1.75 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09528*
- *Device types that are derived from PCF2N12L-*
  RFL1N12L RFP2N12L
  RFL1N15L RFP2N15L



ATTACH AREAS: 92CS-39992
Ⓢ Source } 0.010" x 0.020" (0.254 mm x 0.508 mm)
Ⓖ Gate
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N12L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=100 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=1 A V_{GS}=5 V	—	1.75	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1459**

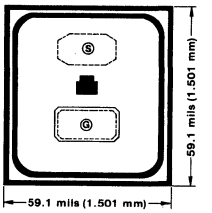
PCF2N18

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 2 A, 3.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09289*
- *Device types that are derived from PCF2N18-*
  RFL1N18 *RFP2N18*
  RFL1N20 *RFP2N20*



ATTACH AREAS: 92CS-39992
Ⓢ Source, Ⓖ Gate } 0.010" x 0.020" (0.254 mm x 0.508 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N18		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=1 A V_{GS}=10 V	—	3.5	V
g_{fs}[a]	V_{DS}=10 V I_D=1 A	400	—	mmho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

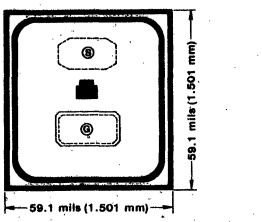
PCF2N18L File Number **1759**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 2 A, 3.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09532*
- *Device types that are derived from PCF2N18L-*
  RFL1N18L RFP2N18L
  RFL1N20L RFP2N20L



ATTACH AREAS: 92CS-39992
(S) Source, (G) Gate } 0.010" x 0.020" (0.254 mm x 0.508 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF2N18L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA, V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=145 V	—	1	μA
I_{GSS}	V_{GS}=±10 V, V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A, V_{GS}=5 V	—	3.5	V
g_{fs}[a]	V_{DS}=10 V, I_D=1 A	400	—	mmho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1460**

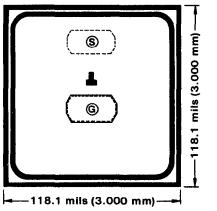
PCF3N45

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

450 V, 3 A, 2.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09193*
- *Device types that are derived from PCF3N45-*
  RFM3N45 RFP3N45
  RFM3N50 RFP3N50



ATTACH AREAS: 92CS-39995
(S)Source, (G)Gate } 0.016" x 0.032" (0.406 mm x 0.813 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF3N45		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=360 V	—	10	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1.5 A V_{GS}=10 V	—	3.75	V
g_{fs}[a]	V_{DS}=10 V I_D 1.5 A	1	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor = 2%

PCF4N35

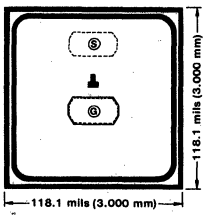
File Number **1755**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

350 V, 4 A, 1.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09393*
- *Device types that are derived from PCF4N35-*
  RFM4N35 *RFP4N35*
  RFM4N40 *RFP4N40*



ATTACH AREAS: 92CS-39995
Ⓢ Source } 0.016" x 0.032" (0.406 mm x 0.813 mm)
Ⓖ Gate
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF4N35		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=280 V	—	10	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=2 A V_{GS}=10 V	—	3	V
g_{fs}[a]	V_{DS}=10 V I_D=2 A	1	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1523**

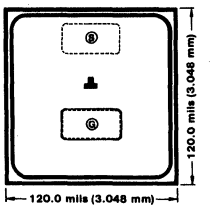
PCF5P12

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

5 A, 120 V, 1 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09320*
- *Device types that are derived from PCF5P12-*
  RFM5P12 *RFP5P12*
  RFM5P15 *RFP5P15*



ATTACH AREAS: 92CS-39990
(S)Source, (G)Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF5P12		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-100 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=2.5 A V_{GS}=-10 V	—	-2.5	V
g_{fs}[a]	V_{DS}=-10 V I_D=2.5 A	0.75	—	mho

[a]Pulsed; pulse duration = 300 us max., duty factor = 2%.

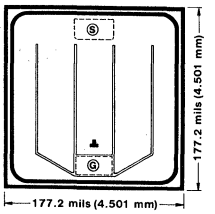
PCF6N45 File Number **1746**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

450 V, 6 A, 1.25 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09191*
- *Device types that are derived from PCF6N45-*
  RFM6N45 RFP6N45
  RFM6N50 RFP6N50



ATTACH AREAS: 92CS-39988
Ⓢ Source, Ⓖ Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF6N45 Min.	Limits PCF6N45 Max.	Units
BV_{DSS}	I_D=1 mA, V_{GS}=0	450	—	V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=360 V	—	10	μA
I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=3 A, V_{GS}=10 V	—	3.75	V
g_{fs}[a]	V_{DS}=10 V, I_D=3 A	2	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1518**

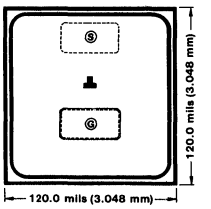
PCF6P08

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 6 A, 0.6 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09406*
- *Device types that are derived from PCF6P08-*
  RFM6P08 RFP6P08
  RFM6P10 RFP6P10



ATTACH AREAS: 92CS-39990
(S)Source, (G)Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF6P08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=3 A V_{GS}=-10 V	—	-1.8	V
g_{fs}[a]	V_{DS}=-10 V I_D=3 A	1	—	mho

[a]Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

PCF7N35

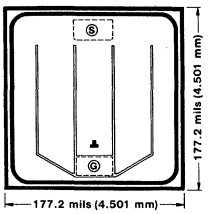
File Number **1747**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

350 V, 7 A, 0.75 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09397*
- *Device types that are derived from PCF7N35-*
  RFM7N35 *RFP7N35*
  RFM7N40 *RFP7N40*



ATTACH AREAS: 92CS-39988
Ⓢ Source, Ⓖ Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF7N35		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=280 V	—	10	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=3.5 A V_{GS}=10 V	—	2.63	V
g_{fs}[a]	V_{DS}=10 V I_D=3.5 A	2	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1520**

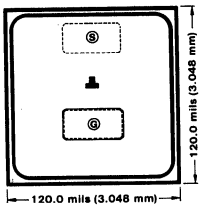
PCF8N18

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 8 A, 0.5 Ω

Features

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09291*
- *Device types that are derived from PCF8N18-*
  RFM8N18 *RFP8N18*
  RFM8N20 *RFP8N20*



ATTACH AREAS: 92CS-39990
Ⓢ Source } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Ⓖ Gate
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF8N18		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=4 A V_{GS}=10 V	—	2.0	V
g_{fs}[a]	V_{DS}=10 V I_D 4 A	1.5	—	mho

[a] Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

PCF8N18L

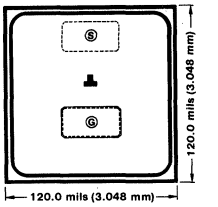
File Number **1760**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 8 A, 0.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09534*
- *Device types that are derived from PCF8N18L-*
  RFM8N18L RFP8N18L
  RFM8N20L RFP8N20L



ATTACH AREAS: 92CS-39990
Ⓢ Source, Ⓖ Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF8N18L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=145 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=4 A V_{GS}=5 V	—	2.0	V
g_{fs}[a]	V_{DS}=10 V I_D=4 A	1.5	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1524**

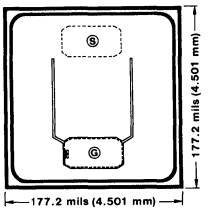
PCF8P08

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 8 A, 0.4 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09410*
- *Device types that are derived from PCF8P08-*
  RFM8P08 *RFP8P08*
  RFM8P10 *RFP8P10*



ATTACH AREAS: 92CS-39989
(S)Source, (G)Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF8P08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=4 A V_{GS}=-10 V	—	-1.6	V
g_{fs}[a]	V_{DS}=-10 V I_D=4 A	2	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

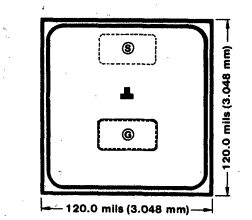
PCF10N12 File Number **1422**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

10 A, 120 V, 0.3 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09192*
- *Device types that are derived from PCF10N12-*
  RFM10N12 RFP10N12
  RFM10N15 RFP10N15



CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

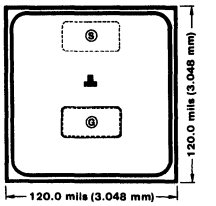
Characteristic	Test Conditions	Limits		Units
		PCF10N12		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=5 A V_{GS}=10 V	—	1.5	V
g_{fs}[a]	V_{DS}=10 V I_D 5 A	2	—	mho

File Number **1761**

PCF10N12L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

10 A, 120 V, 0.3 Ω



ATTACH AREAS: 92CS-39990
(S) Source } 0.020" x 0.040" (0.508 mm x 1.016 mm)
(G) Gate
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09530*
- *Device types that are derived from PCF10N12L-*
  RFM10N12L RFP10N12L
  RFM10N15L RFP10N15L

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF10N12L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=100 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=5 A V_{GS}=5 V	—	1.5	V
g_{fs}[a]	V_{DS}=10 V I_D=5 A	2	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF10P12

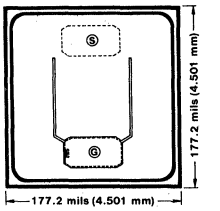
File Number **1752**

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

10 A, 120 V, 0.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09404*
- *Device types that are derived from PCF10P12-*
  RFM10P12 RFP10P12
  RFM10P15 RFP10P15



ATTACH AREAS: 92CS-39989
Ⓢ Source, Ⓖ Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF10P12		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-100 V	—	1	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=5 A V_{GS}=-10 V	—	-2.5	V
g_{fs}[a]	V_{DS}=-10 V I_D=5 A	2	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1525**

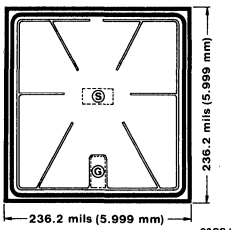
PCF10N45

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

450 V, 10 A, 0.6 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09189*
- *Device types that are derived from PCF10N45-*
  RFM10N45
  RFM10N50



ATTACH AREAS: 92CS-39985
ⓈSource 0.020" x 0.040" (0.508 mm x 1.016 mm)
ⒼGate 0.040" x 0.020" (1.016 mm x 0.508 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF10N45		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	450	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=360 V	—	10	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=5 A V_{GS}=10 V	—	3.0	V
g_{fs}[a]	V_{DS}=10 V I_D=5 A	5	—	mho

[a]Pulsed; pulse duration = 300 *us* max., duty factor = 2%.

PCF12N08

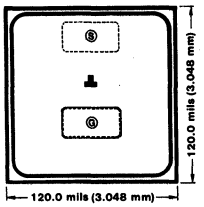
File Number **1457**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 12 A, 0.2 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09284*
- *Device types that are derived from PCF12N08-*
  RFM12N08 RFP12N08
  RFM12N10 RFP12N10



ATTACH AREAS: 92CS-39990
Source, Gate: 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF12N08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=6 A V_{GS}=10 V	—	1.2	V
g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	mho

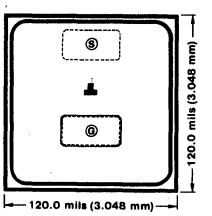
[a]Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1762**

PCF12N08L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 12 A, 0.2 Ω



CHIP LAYOUT

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09526*
- *Device types that are derived from PCF12N08L-*
  RFM12N08L RFP12N08L
  RFM12N10L RFP12N10L

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF12N08L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=65 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=6 A V_{GS}=5 V	—	1.2	V
g_{fs}[a]	V_{DS}=10 V I_D=6 A	2	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF12P08

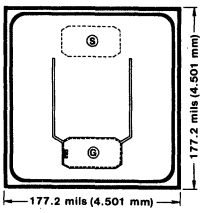
File Number **1519**

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 12 A, 0.3 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09410*
- *Device types that are derived from PCF12P08-*
  RFM12P08 RFP12P08
  RFM12P10 RFP12P10



ATTACH AREAS: 92CS-39989
Ⓢ Source } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Ⓖ Gate
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF12P08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=6 A V_{GS}=-10 V	—	-1.8	V
g_{fs}[a]	V_{DS}=-10 V I_D 6 A	2	—	mho

[a] Pulsed; pulse duration = 300 *us* max., duty factor = 2%.

File Number **1521**

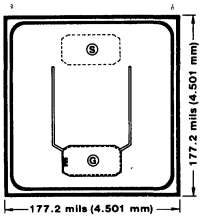
PCF12N18

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 12 A, 0.25 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09293*
- *Device types that are derived from PCF12N18-*
  RFM12N18 RFP12N18
  RFM12N20 RFP12N20



ATTACH AREAS: 92CS-39989
(S)Source, (G)Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF12N18		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=6 A V_{GS}=10 V	—	1.5	V
g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	mho

[a]Pulsed; pulse duration = 300 *us* max., duty factor = 2%.

PCF12N18L

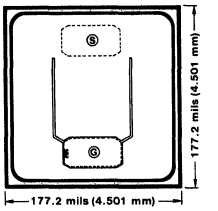
File Number **1763**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 12 A, 0.25 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number 09668*
- *Device types that are derived from PCF12N18L-*
  RFM12N18L RFP12N18L
  RFM12N20L RFP12N20L



ATTACH AREAS: 92CS-39989
Ⓢ Source, Ⓖ Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF12N18L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=145 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=6 A V_{GS}=5 V	—	1.5	V
g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	mho

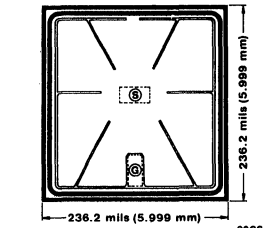
[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1748**

PCF12N35

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

350 V, 12 A, 0.38 Ω



CHIP LAYOUT

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09399*
- *Device types that are derived from PCF12N35-*
  RFM12N35 *RFP12N35*
  RFM12N40 *RFP12N40*

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF12N35		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	350	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=280 V	—	10	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=6 A V_{GS}=10 V	—	2.28	V
g_{fs}[a]	V_{DS}=10 V I_D=6 A	4	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF15N05

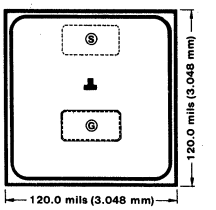
File Number **1526**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 15 A, 0.14 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09382*
- *Device types that are derived from PCF15N05-*
  RFM15N05 RFP15N05
  RFM15N06 RFP15N06



ATTACH AREAS: 92CS-39990
Ⓢ Source, Ⓖ Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF15N05 Min.	Limits PCF15N05 Max.	Units
BV_{DSS}	I_D=1 mA, V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=40 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=7.5 A, V_{GS}=10 V	—	1.05	V
g_{fs}[a]	V_{DS}=10 V, I_D=7.5 A	2	—	mho

[a]Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1764**

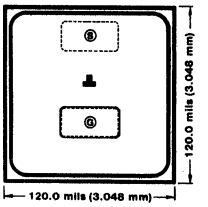
PCF15N05L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 15 A, 0.14 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09522*
- *Device types that are derived from PCF15N05L-*
  RFM15N05L RFP15N05L
  RFM15N06L RFP15N06L



ATTACH AREAS: 92CS-39990
(S) Source } 0.020" x 0.040" (0.508 mm x 1.016 mm)
(G) Gate
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF15N05L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=40 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=7.5 A V_{GS}=5 V	—	1.05	V
g_{fs}[a]	V_{DS}=10 V I_D=7.5 A	2	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

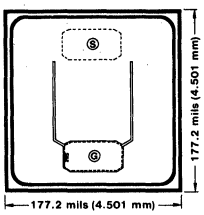
PCF15N12 File Number **1424**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

120 V, 15 A, 0.15 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-15-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09195*
- *Device types that are derived from PCF15N12-*
  RFM15N12 RFP15N12
  RFM15N15 RFP15N15



ATTACH AREAS: 92CS-39989
Ⓢ Source, Ⓖ Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF15N12		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=7.5 A V_{GS}=10 V	—	1.125	V
g_{fs}[a]	V_{DS}=10 V I_D=7.5 A	5		mho

[a]Pulsed; pulse duration=300 μs max., duty factor = 2%

File Number **1765**

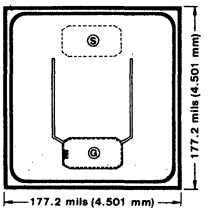
PCF15N12L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

120 V, 15 A, 0.15 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-15-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number 09666*
- *Device types that are derived from PCF15N12L-*
  RFM15N12L RFP15N12L
  RFM15N15L RFP15N15L



ATTACH AREAS: 92CS-39989
(S)Source, (G)Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF15N12L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=100 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=7.5 A V_{GS}=5 V	—	1.125	V
g_{fs}[a]	V_{DS}=10 V I_D=7.5 A	5	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF18N08

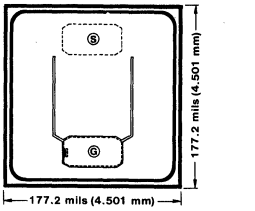
File Number **1527**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 18 A, 0.1 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09286*
- *Device types that are derived from PCF18N08-*
  RFM18N08 RFP18N08
  RFM18N10 RFP18N10



ATTACH AREAS: 92CS-39989
(S)Source, (G)Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C.

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF18N08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=9 A V_{GS}=10 V	—	0.9	V
g_{fs}[a]	V_{DS}=10 V I_D 9 A	5	—	mho

[a]Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1766**

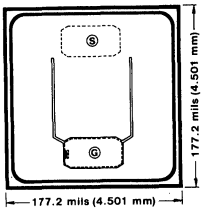
PCF18N08L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 18 A, 0.1 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09664*
- *Device types that are derived from PCF18N08L-*
  RFM18N08L RFP18N08L
  RFM18N10L RFP18N10L



ATTACH AREAS: 92CS-39989
(S)Source, (G)Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF18N08L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=65 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=9 A V_{GS}=5 V	—	0.9	V
g_{fs}[a]	V_{DS}=10 V I_D=9 A	5	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF25N05

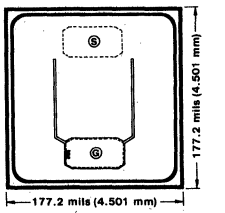
File Number **1749**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 25 A, 0.07 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09386*
- *Device types that are derived from PCF25N05-*
  RFM25N05 RFP25N05
  RFM25N06 RFP25N06



ATTACH AREAS: 92CS-39989
S Source, G Gate } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF25N05		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=40 V	—	1	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=12.5 A V_{GS}=10 V	—	0.875	V
g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	5	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1754**

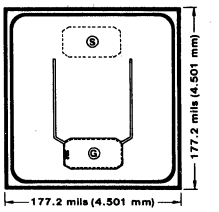
PCF25N05L

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 25 A, 0.07 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09637*
- *Device types that are derived from PCF25N05L-*
  RFM25N05L RFP25N05L
  RFM25N06L RFP25N06L



ATTACH AREAS: 92CS-39989
Ⓢ Source } 0.030" x 0.060" (0.762 mm x 1.524 mm)
Ⓖ Gate
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

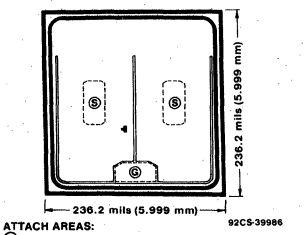
Characteristic	Test Conditions	Limits		Units
		PCF25N05L		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	1	2	V
I_{DSS}	V_{DS}=40 V	—	1	μA
I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=12.5 A V_{GS}=5 V	—	0.875	V
g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	5	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF25N18 File Number **1528**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

180 V, 25 A, 0.15 Ω



CHIP LAYOUT

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09295*
- *Device types that are derived from PCF25N18-*
  RFK25N18
  RFK25N20

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF25N18		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	180	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=145 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=12.5 A V_{GS}=10 V	—	1.875	V
g_{fs}[a]	V_{DS}=10 V I_D=12.5 A	7	—	mho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1753**

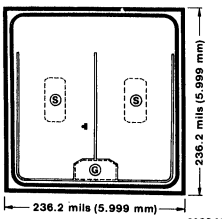
PCF25P08

P-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 25 A, 0.15 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09412*
- *Device types that are derived from PCF25P08-*
  RFK25P08
  RFK25P10



ATTACH AREAS: 92CS-39986
Ⓢ Source 0.060" x 0.030" (1.524 mm x 0.762 mm)
Ⓖ Gate 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF25P08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	-80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	-2	-4	V
I_{DSS}	V_{DS}=-65 V	—	1	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=12.5 A V_{GS}=-10 V	—	-1.875	V
g_{fs}[a]	V_{DS}=-10 V I_D=12.5 A	4	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF30N12

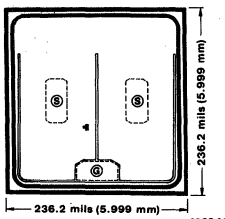
File Number **1529**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

30 V, 120 A, 0.075 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09188*
- *Device types that are derived from PCF30N12-*
  RFK30N12
  RFK30N15



ATTACH AREAS: 92CS-39986
Ⓢ Source 0.060" x 0.030" (1.524 mm x 0.762 mm)
Ⓖ Gate 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF30N12		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	120	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=100 V	—	1	*u*A
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=15 A V_{GS}=10 V	—	1.125	V
g_{fs}[a]	V_{DS}=10 V I_D=15 A	10	—	mho

[a]Pulsed; pulse duration = 300 *u*s max., duty factor = 2%.

File Number **1530**

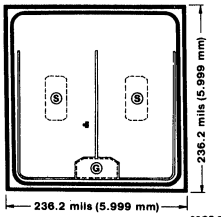
PCF35N08

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

80 V, 35 A, 0.055 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09288*
- *Device types that are derived from PCF35N08-*
  RFK35N08
  RFK35N10



ATTACH AREAS:
Ⓢ Source 0.060" x 0.030" (1.524 mm x 0.762 mm)
Ⓖ Gate 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF35N08		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	80	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=65 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
V_{DS} (ON)[a]	I_D=17.5 A V_{GS}=10 V	—	0.963	V
g_{fs}[a]	V_{DS}=10 V I_D=17.5 A	10	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor = 2%

PCF45N05

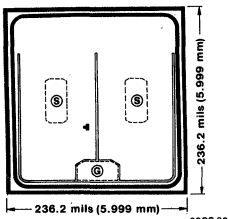
File Number **1531**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

50 V, 45 A, 0.04 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09388*
- *Device types that are derived from PCF45N05-*
  RFK45N05
  RFK45N06



92CS-39986

ATTACH AREAS:
Ⓢ Source 0.060" x 0.030" (1.524 mm x 0.762 mm)
Ⓖ Gate 0.030" x 0.060" (0.762 mm x 1.524 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25° C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF45N05		
		Min.	Max.	
BV_{DSS}	I_D=1 mA V_{GS}=0	50	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=1 mA	2	4	V
I_{DSS}	V_{DS}=40 V	—	1	uA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=22.5 A V_{GS}=10 V	—	0.9	V
g_{fs}[a]	V_{DS}=10 V I_D=22.5 A	10	—	mho

[a] Pulsed; pulse duration = 300 us max., duty factor = 2%.

File Number **1736**

PCF111

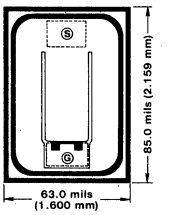
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

60 V, 3.5 A, 0.6 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09592*
- *Device types that are derived from PCF111-*

  IRFF110 *IRFF112*
  IRFF111 *IRFF113*
  IRF510 *IRF512*
  IRF511 *IRF513*



ATTACH AREAS: 92CS-39987
Ⓢ Source 0.012" x 0.019" (0.305 mm x 0.483 mm)
Ⓖ Gate 0.012" x 0.022" (0.350 mm x 0.559 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF111		
		Min.	Max.	
BV_{DSS}	I_D=250 μA V_{GS}=0	60	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=60 V	—	250	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1.5 A V_{GS}=10 V	—	0.9	V
g_{fs}[a]	V_{DS}=2.1 V I_D=1.5 A	1	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF121

File Number **1737**

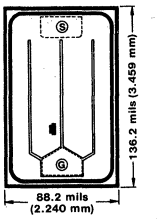
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

60 V, 6 A, 0.3 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09594*
- *Device types that are derived from PCF121-*

IRFF120	*IRFF122*
IRFF121	*IRFF123*
IRF120	*IRF122*
IRF121	*IRF123*
IRF520	*IRF522*
IRF521	*IRF523*



ATTACH AREAS: 92CS-39994
Ⓢ Source 0.016" x 0.032" (0.406 mm x 0.813 mm)
Ⓖ Gate 0.022" x 0.032" (0.559 mm x 0.813 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF121 Min.	Limits PCF121 Max.	Units
BV_{DSS}	I_D=250 μA, V_{GS}=0	60	—	V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=60 V	—	250	μA
I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=3 A, V_{GS}=10 V	—	0.9	V
g_{fs}[a]	V_{DS}=1.8 V, I_D=3 A	1.5	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1738**

PCF131

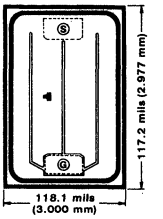
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

60 V, 14 A, 0.18 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09596*
- *Device types that are derived from PCF131-*

IRFF130	*IRFF132*
IRFF131	*IRFF133*
IRF130	*IRF132*
IRF131	*IRF133*
IRF530	*IRF532*
IRF531	*IRF533*



ATTACH AREAS: 92CS-39991
Ⓢ Source, Ⓖ Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF131 Min.	Limits PCF131 Max.	Units
BV_{DSS}	I_D=250 μA, V_{GS}=0	60	—	V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=60 V	—	250	μA
I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=8 A, V_{GS}=10 V	—	1.44	V
g_{fs}[a]	V_{DS}=2.52 V, I_D=8 A	4	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF211

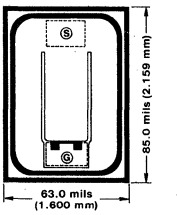
File Number **1739**

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

150 V, 2.5 A, 1.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09598*
- *Device types that are derived from PCF211-*
  IRF610 *IRF612*
  IRF611 *IRF613*



ATTACH AREAS: 92CS-39987
Ⓢ Source 0.012" x 0.019" (0.305 mm x 0.483 mm)
Ⓖ Gate 0.012" x 0.022" (0.350 mm x 0.559 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF211 Min.	Limits PCF211 Max.	Units
BV_{DSS}	I_D=250 μA, V_{GS}=0	150	—	V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=150 V	—	250	μA
I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1.25 A, V_{GS}=10 V	—	1.875	V
g_{fs}[a]	V_{DS}=3.75 V, I_D=1.25 A	0.8	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1740**

PCF221

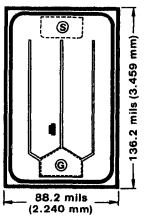
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

150 V, 5 A, 0.8 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09600*
- *Device types that are derived from PCF221-*

IRF220	*IRF222*
IRF221	*IRF223*
IRF620	*IRF622*
IRF621	*IRF623*



ATTACH AREAS: 92CS-39994
Ⓢ Source 0.016" x 0.032" (0.406 mm x 0.813 mm)
Ⓖ Gate 0.022" x 0.032" (0.559 mm x 0.813 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits PCF221 Min.	Limits PCF221 Max.	Units
BV_{DSS}	I_D=250 μA, V_{GS}=0	150	—	V
$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=150 V	—	250	μA
I_{GSS}	V_{GS}=±20 V, V_{DS}=0	—	100	nA
$V_{DS(ON)}$[a]	I_D=2.5 A, V_{GS}=10 V	—	2	V
g_{fs}[a]	V_{DS}=4 V, I_D=2.5 A	1.3	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF231

File Number **1741**

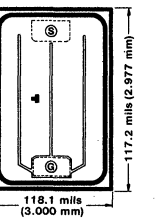
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

150 V, 9 A, 0.4 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-5-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09602*
- *Device types that are derived from PCF231-*

  IRF230 *IRF232*
  IRF231 *IRF233*
  IRF630 *IRF632*
  IRF631 *IRF633*



ATTACH AREAS: 92CS-39991
Ⓢ Source, Ⓖ Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF231		
		Min.	Max.	
BV_{DSS}	I_D=250 μA V_{GS}=0	150	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=150 V	—	250	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=5 A V_{GS}=10 V	—	2	V
g_{fs}[a]	V_{DS}=3.6 V I_D=5 A	3	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1742**

PCF321

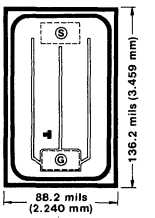
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

350 V, 3 A, 1.8 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09610*
- *Device types that are derived from PCF321-*

  IRF320 *IRF322*
  IRF321 *IRF323*
  IRF720 *IRF722*
  IRF721 *IRF723*



ATTACH AREAS: 92CS-39993
Ⓢ Source } 0.016" x 0.032" (0.406 mm x 0.813 mm)
Ⓖ Gate
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF321		
		Min.	Max.	
BV_{DSS}	I_D=250 μA V_{GS}=0	350	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=350 V	—	250	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1.5 A V_{GS}=10 V	—	2.7	V
g_{fs}[a]	V_{DS}=5.4 V I_D=1.5 A	1	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF331

File Number **1743**

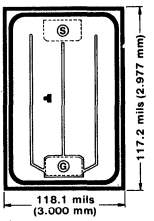
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

350 V, 5.5 A, 1 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09608*
- *Device types that are derived from PCF331-*

IRF330	*IRF332*
IRF331	*IRF333*
IRF730	*IRF732*
IRF731	*IRF733*



ATTACH AREAS: 92CS-39991
(S) Source, (G) Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF331		
		Min.	Max.	
BV_{DSS}	I_D=250 μA V_{GS}=0	350	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=350 V	—	250	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=3 A V_{GS}=10 V	—	3	V
g_{fs}[a]	V_{DS}=5.5 V I_D=3 A	3	—	mho

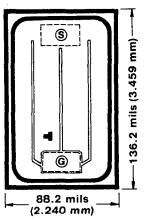
[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

File Number **1744**

PCF421

N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

450 V, 2.5 A, 3 Ω



ATTACH AREAS: 92CS-39993
(S)Source } 0.016" x 0.032" (0.406 mm x 0.813 mm)
(G)Gate
Back Side – Drain
DIE THICKNESS – 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09606*
- *Device types that are derived from PCF421-*

  IRF420 *IRF422*
  IRF421 *IRF423*
  IRF820 *IRF822*
  IRF821 *IRF823*

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF421		
		Min.	Max.	
BV_{DSS}	I_D=250 μA V_{GS}=0	450	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=450 V	—	250	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=1 A V_{GS}=10 V	—	3	V
g_{fs}[a]	V_{DS}=7.5 V I_D=1 A	1	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

PCF431

File Number **1745**

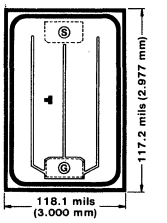
N-Channel Enhancement-Mode Power Field-Effect Transistor Chip

450 V, 4.5 A, 1.5 Ω

Features:

- *Contact metallization:*
  Gate and source-aluminum
  Drain-tri-metal (Al-Ti-Ni)
- *Assembly recommendations:*
  Gate and source-10-mil aluminum wire
  Drain-mounted with 95/5 lead-tin solder
- *Die Number-09604*
- *Device types that are derived from PCF431-*

  IRF430 *IRF432*
  IRF431 *IRF433*
  IRF830 *IRF832*
  IRF831 *IRF833*



ATTACH AREAS: 92CS-39991
Ⓢ Source, Ⓖ Gate } 0.020" x 0.040" (0.508 mm x 1.016 mm)
Back Side - Drain
DIE THICKNESS - 14 ± 1 mils (0.356 ± 0.025 mm)

CHIP LAYOUT

Electrical Characteristics at 25°C

The chip is 100% probed to the actual conditions and limits specified.

Characteristic	Test Conditions	Limits		Units
		PCF431		
		Min.	Max.	
BV_{DSS}	I_D=250 μA V_{GS}=0	450	—	V
$V_{GS(th)}$	V_{GS}=V_{DS} I_D=250 μA	2	4	V
I_{DSS}	V_{DS}=450 V	—	250	μA
I_{GSS}	V_{GS}=±20 V V_{DS}=0	—	100	nA
$V_{DS}(ON)$[a]	I_D=2.5 A V_{GS}=10 V	—	3.75	V
g_{fs}[a]	V_{DS}=6.75 V I_D=2.5 A	2.5	—	mho

[a]Pulsed; pulse duration=300 μs max., duty factor=2%.

Ultra-Fast-Recovery Rectifiers

BYW51-100, BYW51-150, BYW51-200

File Number **1412**

Ultra High Speed Rectifiers
BYW51-100
BYW51-150
BYW51-200

Dual 8-A, High-Speed, High Efficiency Epitaxial Silicon Rectifiers

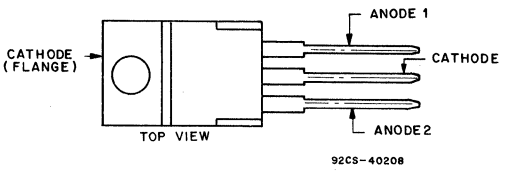
Features:

- *Ultra fast recovery time (< 35 ns)*
- *Low forward voltage*
- *Low thermal resistance*
- *Planar design*
- *Wire-bonded construction*

Applications:

- *General purpose*
- *Power switching circuits to 100 kHz*
- *Full-wave rectification*

TERMINAL DESIGNATION



JEDEC TO-220AB

The BYW51 series devices are low forward voltage drop, ultra-fast-recovery rectifiers (trr < 35 ns). They use a planar ion-implanted epitaxial construction.

These devices are intended for use as output rectifiers and fly-wheel diodes in a variety of high-frequency pulse-width-modulated and switching regulators. Their low stored charge and attendant fast reverse-recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

All are supplied in TO-220AB plastic packages.

MAXIMUM RATINGS, *Absolute-Maximum Values, per Junction:*

	BYW 51-100	BYW 51-150	BYW 51-200	
V_{RRM}	100	150	200	V
V_{RSM}	110	165	220	V
I_{FRM}, $t_p < 10\ \mu s$	100	100	100	A
I_F(RMS), total	20	20	20	A
I_F(Average), total T_C = 125°C, δ = 0.5	20	20	20	A
I_{FSM}(Surge) t_p = 10 ms, sinusoidal	100	100	100	A
P_D, T_C = 125°C	20	20	20	W
T_j	-40 + 150	-40 + 150	-40 + 150	°C
T_L (Lead temperature during soldering) At distance > 1/8 in. (3.17 mm) from case for 10 S max.	260	260	260	°C

BYW51-100, BYW51-150, BYW51-200

ELECTRICAL CHARACTERISTICS, per junction

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	T_J °C	Voltage V_R V	Current I_F A	BYW51-100		BYW51-150		BYW51-200		
				Min.	Max.	Min.	Max.	Min.	Max.	
i_R	25	100		—	5	—	—	—	—	μA
		150		—	—	—	5	—	—	
		200		—	—	—	—	—	5	
	100	100		—	1	—	—	—	—	mA
		150		—	—	—	1	—	—	
		200		—	—	—	—	—	1	
V_F	25		8	—	0.95	—	0.95	—	0.95	V
	100		8	—	0.89	—	0.89	—	0.89	
t_{rr}	25		1(a)	—	35	—	35	—	35	ns
$R_{\theta JC}$, per leg				—	2.5		2.5	—	2.5	°C/W
$R_{\theta JC}$, total				—	1.3	—	1.3	—	1.3	
$R_{\theta JA}$				—	60	—	60	—	60	
C_J	25	10	0	All types (typ.) 40						pF

(a) $di_F/dt > 50A/\mu s$, $I_{RM}(rec) < 1A$, $I_{RR} = 0.25A$

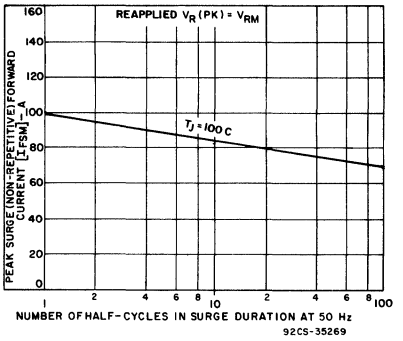


Fig. 1 - Peak surge forward current vs. surge duration.

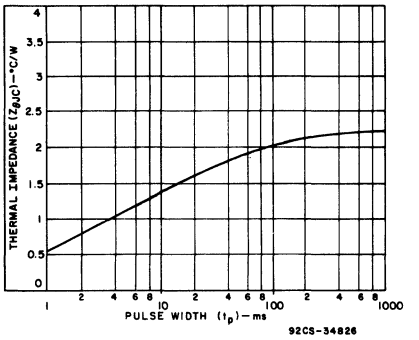


Fig. 2 - Thermal impedance vs. pulse width (per junction).

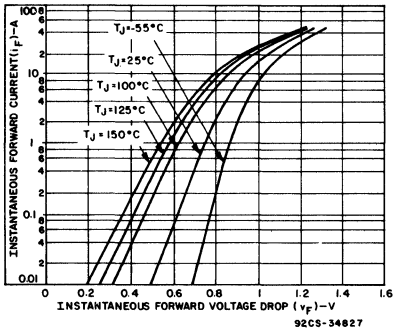


Fig. 3 - Typical forward current vs. forward-voltage drop.

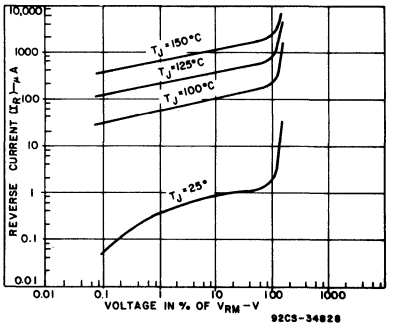


Fig. 4 - Typical reverse current vs. voltage.

RUR-810, RUR-815, RUR-820

File Number **1355**

Ultra High Speed Rectifiers
RUR-810 RUR-815 RUR-820

8-A, High Speed, High Efficiency Epitaxial Silicon Rectifiers

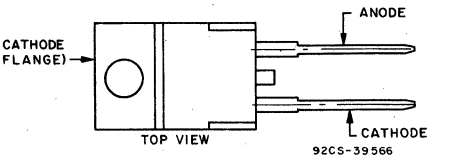
Features:

- *Ultra fast recovery time (<35 ns)*
- *Low forward voltage*
- *Low thermal resistance*
- *Planar design*
- *Wire-bonded construction*

Applications:

- *General Purpose*
- *Power switching circuits to 100 kHz*
- *Output rectification in switching power supplies*

TERMINAL DESIGNATION



JEDEC TO-220AC

The RCA RUR-810, RUR-815, and RUR-820* are low forward voltage drop ultra fast-recovery rectifiers (trr <35 ns). They use a glass passivated ion-implanted epitaxial construction.

These devices are intended for use as output rectifiers and fly wheel diodes in a variety of high-frequency pulse-width modulated and switching regulators. Their low stored charge and attendant fast reverse-recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

All are supplied in TO-220AC plastic packages.

*Formerly RCA Dev. No. TA9223A, TA9223B, and TA9223C, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	RUR-810	RUR-815	RUR-820	
VRM	100	150	200	V
IF (Average)				
T_A = 25°C (No Heat Sink)	3			A
T_A = 25°C (With Heat Sink)[a]	8			A
T_C = 125°C	8			A
IFSM (surge)				
8.3ms, 1/2 cycle, non-repetitive	100			A
Tstg, T_J	−55 to 150			°C
T_L (Lead temperature during soldering)				
At distance > 1/8in. (3.17mm) from case for 10 S max.	260			°C

(a) Wakefield type 295 heat sink with convection cooling

RUR-810, RUR-815, RUR-820

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
				RUR-810		RUR-815		RUR-820		
	T_J °C	Voltage V_R V	Current i_F A	Min.	Max.	Min.	Max.	Min.	Max.	
i_R	25	100		—	5	—	—	—	—	μA
		150		—	—	—	5	—	—	
		200		—	—	—	—	—	5	
	100	100		—	400	—	—	—	—	
		150		—	—	—	400	—	—	
		200		—	—	—	—	—	400	
V_F	25		8	—	0.95	—	0.95	—	1	V
	100		8	—	0.89	—	0.89	—	0.94	
t_{rr}	25		2(a)	—	35	—	35	—	35	ns
$R_{\theta JC}$				—	2.25	—	2.25	—	2.25	°C/W
$R_{\theta JA}$				—	60	—	60	—	60	
C_J	25	10	0	40 Typ.		40 Typ.		40 Typ.		pF

(a) $di_F/dt > 40A/\mu s$, I_{RM} (rec) $< 1A$, $I_{RR} = 0.25A$

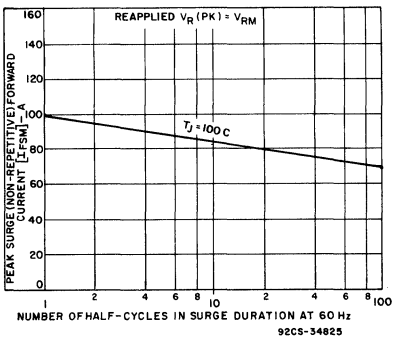


Fig. 1 — Peak surge forward current vs. surge duration.

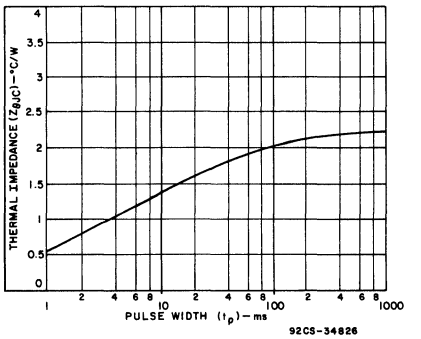


Fig. 2 — Thermal impedance vs. pulse width.

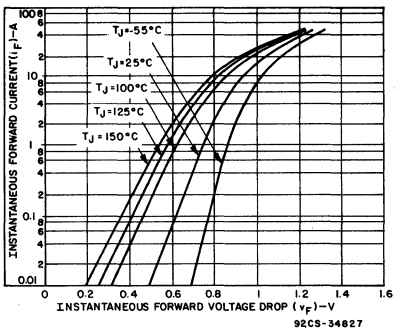


Fig. 3 — Typical forward current vs. forward-voltage drop.

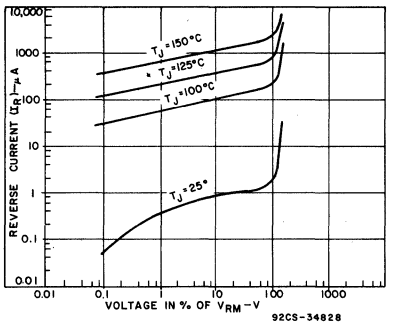


Fig. 4 — Typical reverse current vs. voltage.

RUR-D810, RUR-D815, RUR-D820

File Number **1356**

Ultra High Speed Rectifiers
RUR-D810 RUR-D815 RUR-D820

Dual 8-A, High-Speed, High Efficiency Epitaxial Silicon Rectifiers

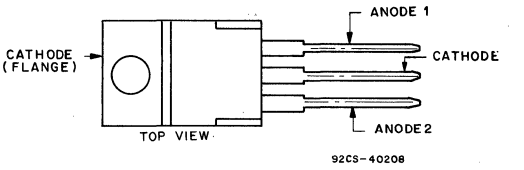
Features:

- *Ultra fast recovery time [<35 ns]*
- *Low forward voltage*
- *Low thermal resistance*
- *Planar design*
- *Wire-bonded construction*

Applications:

- *General Purpose*
- *Power switching circuits to 100 kHz*
- *Full-wave rectification*

TERMINAL DESIGNATION



JEDEC TO-220AB

The RCA RUR-D810, RUR-D815, and RUR-D820* are low forward voltage drop ultra fast-recovery rectifiers (trr <35 ns). They use a glass passivated ion-implanted epitaxial construction.

These devices are intended for use as output rectifiers and fly wheel diodes in a variety of high-frequency pulse-width modulated and switching regulators. Their low stored charge and attendant fast reverse recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

All are supplied in TO-220AB plastic packages.

*Formerly RCA Dev. No. TA9224A, TA9224B, and TA9224C, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values, per Junction:*

	RUR-D810	RUR-D815	RUR-D820	
VRM	100	150	200	V
IF (Average)				
T_A = 25°C (No Heat Sink)		3		A
T_A = 25°C (With Heat Sink)[a]		8		A
T_C = 125°C		8		A
IFSM (surge)				
8.3ms, 1/2 cycle, non-repetitive		100		A
Tstg, T_J		−55 to 150		°C
T_L (Lead temperature during soldering)				
At distance > 1/8in. (3.17mm) from case for 10 S max.		260		°C

(a) Wakefield type 295 heat sink with convection cooling

RUR-D810, RUR-D815, RUR-D820

ELECTRICAL CHARACTERISTICS, per junction

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
				RUR-D810		RUR-D815		RUR-D820		
	T_J °C	Voltage V_R V	Current i_F A	Min.	Max.	Min.	Max.	Min.	Max.	
i_R	25	100		—	5	—	—	—	—	μA
		150		—	—	—	5	—	—	
		200		—	—	—	—	—	5	
	100	100		—	400	—	—	—	—	
		150		—	—	—	400	—	—	
		200		—	—	—	—	—	400	
v_F	25		8	—	0.95	—	0.95	—	1	V
	100		8	—	0.89	—	0.89	—	0.94	
t_{rr}	25		8(a)	—	35	—	35	—	35	ns
$R\theta_{JC}$				—	2.25	—	2.25	—	2.25	°C/W
$R\theta_{JA}$				—	60	—	60	—	60	
C_J	25	10	0	40 Typ.		40 Typ.		40 Typ.		pF

(a) $di_F/dt > 40A/\mu s$, I_{RM} (rec) $< 1A$, $I_{RR} = 0.25A$

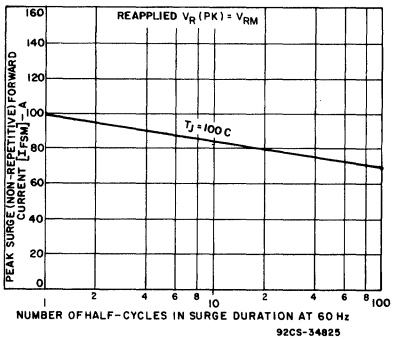


Fig. 1 — Peak surge foward current vs. surge duration.

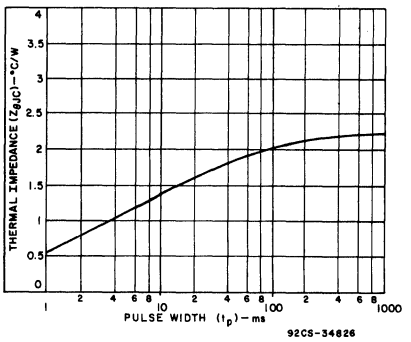


Fig. 2 - Thermal impedance vs. pulse width (per junction).

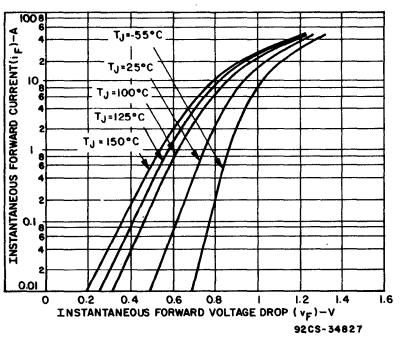


Fig. 3 — Typical forward current vs. forward-voltage drop.

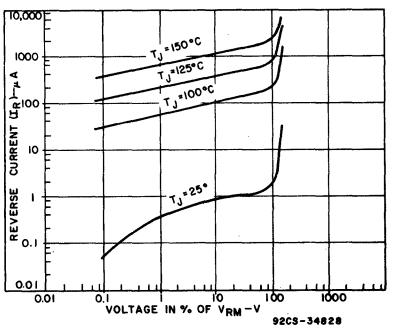


Fig. 4 — Typical reverse current vs. voltage.

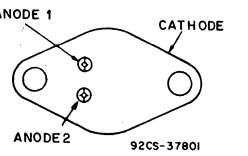
RUR-D1610, RUR-D1615, RUR-D1620

File Number **1383**

Ultra High Speed Rectifiers
RUR-D1610, RUR-D1615, RUR-D1620

Dual 16-A, High-Speed, High Efficiency Epitaxial Silicon Rectifiers

TERMINAL DESIGNATION



JEDEC TO-204AA

Features:
- *Ultra fast recovery time (< 35 ns)*
- *Low forward voltage*
- *Low thermal resistance*
- *Planar design*
- *Wire-bonded construction*

Applications:
- *General purpose*
- *Power switching circuits to 100 kHz*
- *Full-wave rectification*

The RCA RUR-D1610, RUR-D1615 and RUR-D1620• are low forward voltage drop, ultra fast-recovery rectifiers (trr< 35 ns). They use an ion-implanted planar epitaxial construction.

These devices are intended for use as output rectifiers and fly wheel diodes in a variety of high-frequency pulse-width modulated power supplies, amplifiers and switching regulators. Their low stored charge and attendant fast reverse recovery behavior minimize electrical noise generation and, in many circuits, markedly reduce the turn-on dissipation of the associated power switching transistors.

All are supplied in steel JEDEC TO-204AA hermetic packages.

•Formerly RCA Developmental Nos. TA9226A, B and C respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values, per Junction:*

	RUR-D1610	RUR-D1615	RUR-D1620	
V_{RM}	100	150	200	V
I_F (Average)				
T_A = 25°C (No Heat Sink)		6		A
T_A = 25°C (With Heat Sink)■		16		A
T_C = 125°C		16		A
I_{FSM} (surge)				
8.3 ms, 1/2 cycle, non-repetitive		275		A
Thermal Resistance (J-C)		1.5		°C/W
Thermal Resistance (J-C) Total		1.2		°C/W
Thermal Resistance (J-A)		30		°C/W
T_{stg}, T_J		-55 to 150		°C
T_L (Lead temperature during soldering)				
At distance > 1/8 in. (3.17 mm) from case for 10 s max.		260		°C

■ Wakefield type 621 heat sink with convection cooling

RUR-D1610, RUR-D1615, RUR-D1620

ELECTRICAL CHARACTERISTICS, per junction

CHARACTERISTICS	TEST CONDITIONS			LIMITS						UNITS
	T_J °C	Voltage V_H V	Current I_I A	RUR-D1610		RUR-D1615		RUR-D1620		
				Min.	Max.	Min.	Max.	Min.	Max.	
i_R	25	100		—	15	—	—	—	—	μA
		150		—	—	—	15	—	—	
		200		—	—	—	—	—	15	
	100	100		—	1.5	—	—	—	—	mA
		150		—	—	—	1.5	—	—	
		200		—	—	—	—	—	1.5	
V_F	25		16	—	0.95	—	0.95	—	1	V
	125		16	—	0.83	—	0.83	—	0.88	
t_{rr}	25		4(a)	—	35	—	35	—	35	ns
$R\theta JC$				—	1.5	—	1.5	—	1.5	°C/W
$R\theta JA$				—	30	—	30	—	30	
C_J	25	10	0	80 Typ.		80 Typ.		80 Typ.		pF

(a) $di_F/dt > 40A/\mu s$, $I_{RM}(rec) < 1A$, $I_{RR} = 0.25A$

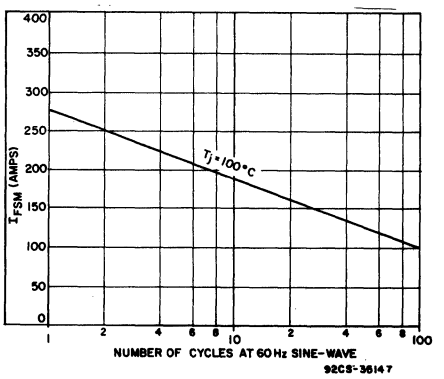


Fig. 1 - Peak surge forward current vs. surge duration.

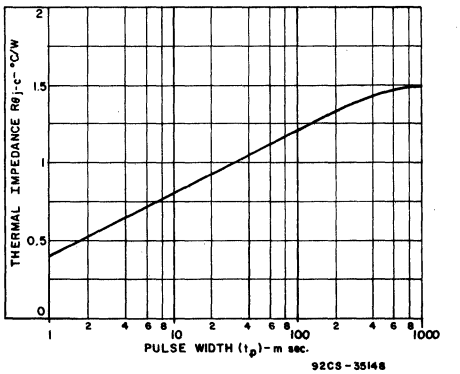


Fig. 2 - Thermal impedance vs. pulse width (per junction).

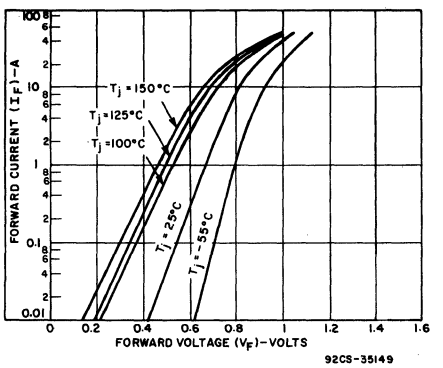


Fig. 3 - Typical forward current vs. forward-voltage drop.

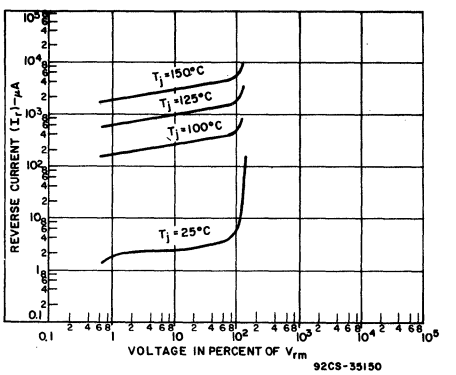


Fig. 4 - Typical reverse current vs. voltage.

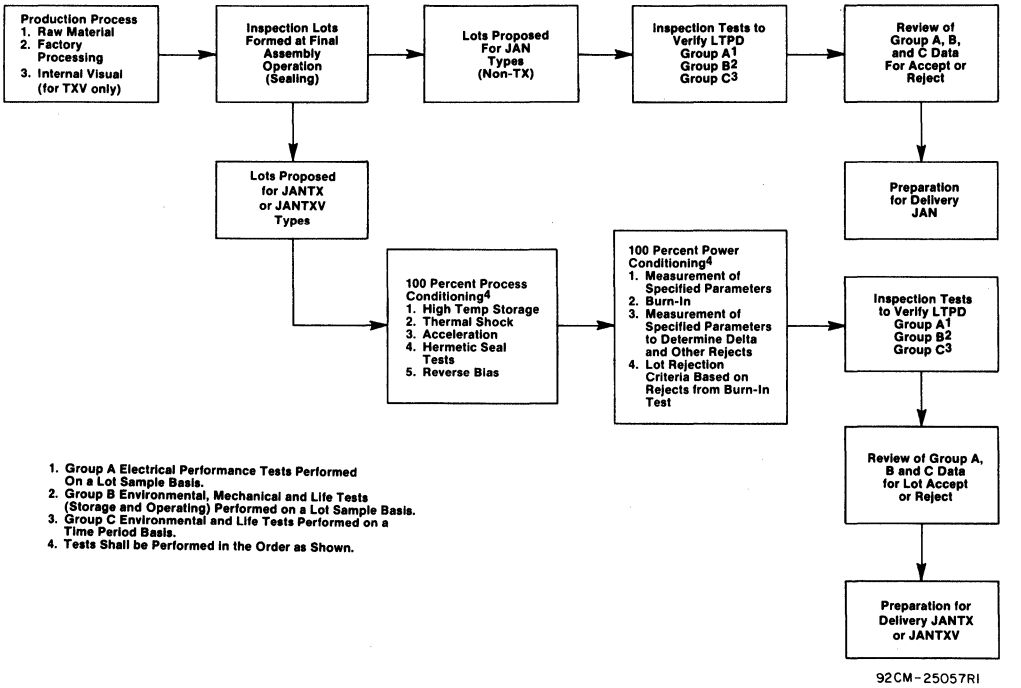
High Reliability Power MOSFETs

High-Reliability Power Products

Solid-state devices classified as high-reliability types have come to be primarily associated with military and aerospace applications. In many ways, this association is misleading because the commerical equipment market is probably the largest user of high-reliability products, but not necessarily by that label. Military and aerospace agencies, however, have been largely responsible for establishment of comprehensive published reliability specifications and standards which have been accepted by the solid-state industry. MIL standards dominate the procedures used to specify high-reliability solid-state devices and represent a common reference point frequently used by commerical users to define their requirements.

Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured: rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed those required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment. These standards also cover a wide range of requirements for the manufacturer on such things as:

(a) The procedure and requirements for a manufacturer to become certified to manufacture MIL-spec parts.
(b) The requirements for qualifying parts.
(c) Product-assurance provisions in such areas as quality control, inspection procedures, personnel training, cleanliness, failure analysis, and documentation.
(d) Test methods and procedures.
(e) Marking and identification of product.
(f) Preservation and packing.



Order of procedure diagram for JAN, JANTX, and JANTXV solid-state devices.

JAN, JANTX, and JANTXV

JAN, JANTX, and JANTXV Solid-State Power Devices

The major military specification used for the procurement of standard solid-state devices by the military is MIL-S-19500, which covers the devices such as discrete transistors, thyristors, and diodes.

MIL-S-19500 is the specification for the familiar "JAN" type solid state devices. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center (DESC).

Levels of reliability are defined by MIL-S-19500. JAN types receive Group A, Group B, and Group C lot sampling only, and are the least expensive. JANTX types receive 100 percent process conditioning, and power conditioning, and are subjected to lot rejection based on delta parameter criteria in addition to Group A, Group B, and Group C lot sampling. JANTXV types are subjected to 100 percent (JTXV) internal visual inspection in addition to all of the JANTX tests in accordance with MIL-STD-750 test methods and MIL-S-19500.

DESC publishes "QPL-19500", a Qualified Products List of all types and suppliers approved to produce and brand devices in accordance with MIL-S-19500.

The following tables list approved "QPL" types and types that are process of testing preliminary to QPL approval by DESC, respectively.

Custom high reliability selections of RCA Power devices can also be supplied with similar process and power conditioning tests and delta criteria.

QPL Approved Types

RCA is presently qualified on the following devices. Prices and delivery quotations may be obtained from your local sales representative.

Power MOSFETs

N-Channel Types	MIL-S 19500/	Package	Channel	P_T (W)	I_D (A)	V_{BR}(DSS) (V)	r_{DS}(on) Ω
2N6764	543A	TO-204AE	N	150	38	100	0.055
2N6766	543A	TO-204AE	N	150	30	200	0.085
2N6756	542A	TO-204AA	N	75	14	100	0.18
2N6758	542A	TO-204AA	N	75	9	200	0.4
2N6760	542A	TO-204AA	N	75	5.5	400	1
2N6762	542A	TO-204AA	N	75	4.5	500	1.5
2N6782	556	TO-205AF	N	15	3.5	100	0.6
2N6788	555	TO-205AF	N	20	6	100	0.3
2N6796	557	TO-205AF	N	25	8	100	0.18

Types Planned for 1986 QPL Approval

RCA plans to request authorization to qualify the following types for QPL listing and presently anticipates completion of the required test procedures by the date noted below.

Power MOSFETs

Types	MIL-S 19500/	Package	Channel	P_T (W)	I_D (A)	V_{BR}(DSS) (V)	r_{DS}(on) Ω	Anticipated Approval Date
2N6768	543A	TO-204AA	N	150	14	400	0.3	6/86
2N6770	543A	TO-204AA	N	150	12	500	0.4	6/86
2N6784	556	TO-205AF	N	15	2.25	200	1.50	6/86
2N6786	556	TO-205AF	N	15	1.25	400	3.60	9/86
2N6790	555	TO-205AF	N	20	3.50	200	0.80	6/86
2N6792	555	TO-205AF	N	20	2	400	1.80	6/86
2N6794	555	TO-205AF	N	20	1.50	500	3	6/86
2N6798	557	TO-205AF	N	25	5.50	100	0.40	5/86
2N6800	557	TO-205AF	N	25	3	400	1	6/86
2N6802	557	TO-205AF	N	25	2.5	500	1.50	6/86
2N6895	565	TO-205AF	P	8.33	-1.5	100	3.65	5/86
2N6896	565	TO-204AA	P	60	-6	100	0.6	5/86
2N6897	565	TO-204AA	P	100	-12	100	0.3	5/86
2N6898	565	TO-204AE	P	150	-25	100	0.2	5/86
Logic-Level Types								
2N6901	566	TO-205AF	N	8.33	-1.5	100	1.4	5/86
2N6902	566	TO-204AA	N	75	-12	100	0.2	5/86
2N6903	566	TO-205AF	N	8.33	-1.5	200	3.65	5/86
2N6904	566	TO-204AA	N	75	-8	200	0.65	5/86

Added Value Screening

RCA added Value Screening for Power MOSFETs

Many solid-state devices not yet covered by military specifications, because they are too new, offer the most recent technological advances or have special performance characteristics which offer advantages to the designer of high-reliability equipment. RCA cooperates with the users of such devices in establishment of high-reliability specifications patterned after MIL standards, which allow these designs to be approved for use in military and aerospace systems, as well as commercial equipment.

Most procurements of solid-state devices for military systems are made by the equipment contractor from the MIL-STD parts list as awards are received for electronic equipment. Some military and aerospace programs, because of their size, duration, or special requirements (Minuteman and Peacekepper are two examples), require that special specifications and process methods, or even special production lines, be established and tailored to the particular functional, reliability, and economic needs of the program. RCA Solid State Division has frequently used the resources of its laboratories, production, facilities, and expert technical staff to contribute to the success of such programs.

All RCA high-reliability solid-state power devices are processed in accordance with provisions of MIL-S-19500. The desired screening test sequence can be chosen from the models shown in Table III.

Class S devices provide wafer lot control traceability from wafer diffusion through screening.

Class S chips also provide wafer lot control traceability from wafer diffusion through screening. A sample of 22 devices taken from this lot is assembled in a suitable package. The assembled sample devices are subjected to the Class S screening sequence in the table below. Class S chips are released for shipment when the assembled sample devices successfully pass the screen.

Group B and Group C tests will be performed when requested in accordance with MIL-S-19500.

ADDED VALUE HIGH-RELIABILITY SCREENING

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
1. Internal Visual	2072	For transistors.	100%	100%	—
2. High Temp Life (LTPD) (stabilization bake)	1032	24 hrs min at max rated storage temp.	100%	100%	100%
3. Thermal shock (temp cycling)	1051	No dwell is required at 25° C. Test condition C, 20 cycles, t (extremes) > 10 min.	100%	100%	100%
4. Constant acceleration 1/	2006	Y_1 direction at 20,000 G min except at 10,000 G min for devices with power rating of > 10 watts at T_C = 25° C. The 1 min hold time requirement shall not apply.	100%	100%	100%

Added Value Screening

ADDED VALUE HIGH-RELIABILITY SCREENING (Continued)

SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
5. Hermetic Seal Fine 1/	1071	Test condition G or H, max leak rate = $5x10^{-8}$ atm cc/s except $5x10^{-7}$ atm cc/s for devices with internal cavity > 0.3 cc.	Optional if done in screen 14.	100% 4/	100% 4/
Gross		Test condition A, C, D, E, or F.	Optional	100% 4/	100% 4/
6. Serialization		See 3.7.9.	100%		
7. Interim Electrical Parameters		As specified.	100% (Read and record)		
8. High Temp Reverse Bias (HTRB)		48 hrs min at T_A = 150° C (min) and minimum applied voltage as follows:			
Burn-in (for transistors)	1039	Transistors - 80% (min) of rated V_{CB} (bipolar), $V_{GS(FET)}$, or $V_{DS(FET)}$ as applicable. Test condition A.	100%	100%	100%
9. Interim electrical and delta parameters		As specified but including all delta parameters as a minimum. Leakage current shall be measured on each device before any other test is made.	100% (Measure all specified parameters within 16 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)	100% (Measure all specified parameters within 24 hrs after removal of applied voltage in HTRB. Record those parameters which have a delta limit.) (See screen 11.)

Added Value Screening

ADDED VALUE HIGH-RELIABILITY SCREENING (Continued)

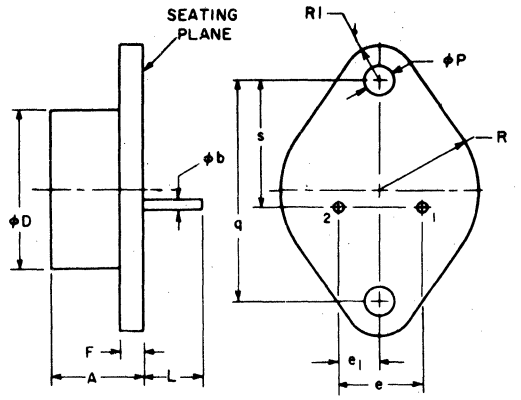
SCREEN	MIL-STD-750 METHOD	CONDITION	CLASS S REQUIREMENTS	CLASS V REQUIREMENTS	CLASS X REQUIREMENTS
10. Power Burn-In		As specified.	100%	100%	100%
Burn-In (Transistors)		Transistors. Test condition B.	240 hrs (min)	160 hrs (min)	160 hrs (min)
Burn-In (Thyristors) 3/	1040	Thyristors.	240 hrs (min)	96 hrs (min)	96 hrs (min)
11. Final Electrical Test		As specified.	100%	100%	100%
Interim Electrical		All interim and delta parameter measurements must be completed within 96 hrs after removal from burn-in conditions.	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)	Interim electrical and delta parameters as a minimum. (Read and record.)
Other Electrical Parameters			Group A, sub-groups 2 and 3.	Group A, sub-groups 2 and 3.	Group A, sub-roups 2 and 3.
12. Hermetic Seal	1071	(Same as 5 on previous page) 2/	100%	Optional 4/	Optional 4/
Fine 1/					
Gross					
13. Radiography	2076	2/	100%	—	—
14. External Visual Examination	2071	To be performed after complete marking.	100%	—	—

*1/ Omit fine leak seal test and constant acceleration test for double plug, non-internal cavity diode construction.
*2/ The radiographic and seal screens for JANS may be performed in any order following final electrical test. Glass diodes shall not be painted until after seal tests. When hermetic seal testing is performed in screen 5 it does not have to be performed again in screen 12 for double plug, non-internal cavity diode construction.
*3/ Reverse-blocking test shall replace power burn-in for power rectifiers at $\geq$ 10 amp rating at $T_C \geq 100°$ C and all thyristors.
4/ Fine and gross seal leak test for JANTX and JANTXV shall be performed in either block 5 or block 12.

Dimensional Outlines and Mounting Hardware

Dimensional Outlines

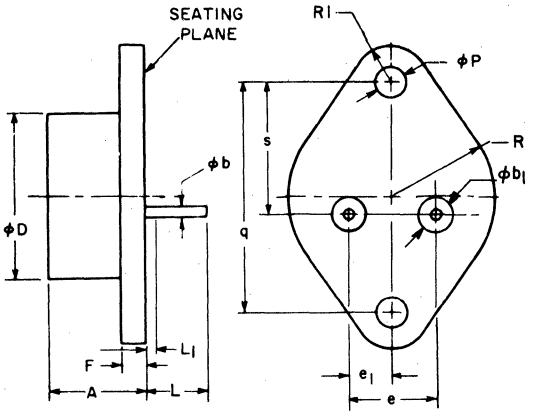
JEDEC TO-204AA



SYMBOL	INCHES		MILLIMETERS		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
φb	0.038	0.043	0.966	1.092	
φD	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	—	0.135	—	3.42	
L	0.312	—	7.93	—	
φP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	—	0.525	—	13.33	
R_1	—	0.188	—	4.77	
s	0.655	0.675	16.64	17.14	

92CS-37249R1

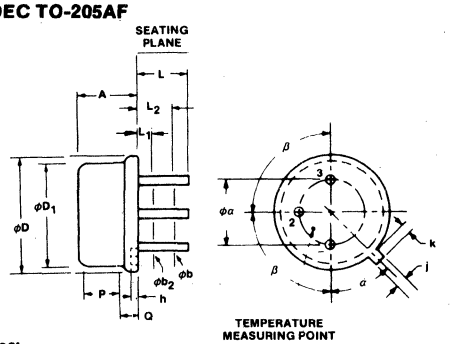
JEDEC TO-204AE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.250	0.450	6.4	11.4	
φb	0.057	0.063	1.45	1.60	
$φb_1$	0.141 NOM		3.58 NOM		
$φD_2$	—	0.875	—	22.22	
e	0.420	0.440	10.67	11.17	
e_1	0.205	0.225	5.21	5.71	
F	0.060	0.135	1.53	3.42	
L	0.440	0.480	11.18	12.19	
φP	0.151	0.161	3.84	4.08	
q	1.187 BSC		30.15 BSC		
R	0.495	0.525	12.58	13.33	
R_1	0.131	0.188	3.33	4.77	
s	0.655	0.675	16.64	17.14	

92CS-37523

JEDEC TO-205AF



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
φa	0.200 BSC		5.08 BSC		4
A	0.160	0.180	4.07	4.57	
φb	0.016	0.021	0.41	0.53	5
$φb_2$	0.016	0.019	0.41	0.48	5
φD	0.340	0.370	8.64	9.39	
$φD_1$	0.315	0.355	8.01	9.01	2
h	0.009	0.041	0.23	1.04	
j	0.028	0.034	0.72	0.86	
k	0.029	0.045	0.74	1.14	1
L	0.500	0.750	12.70	19.05	5
L_1	—	0.050	—	1.27	5
L_2	0.250	—	6.35	—	5
P	0.070	—	1.78	—	2
Q	—	0.050	—	1.27	3
α	45° NOMINAL				
β	90° NOMINAL				

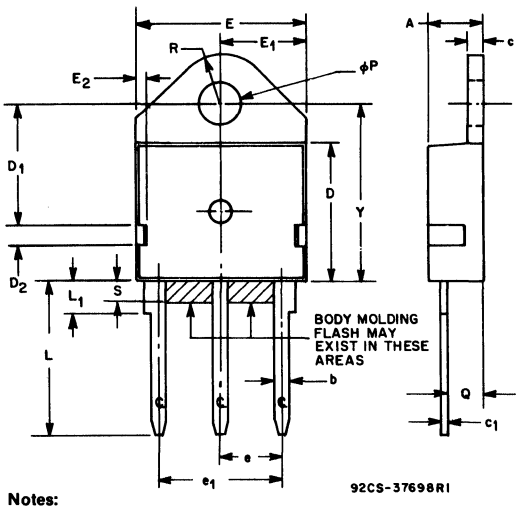
92CS-38248R1

Notes:

1. Dimension k measured from φD maximum.
2. $φD_1$ shall not vary more than 0.010 in Zone P. This zone controlled for automatic handling.
3. Details of outline in this zone optional.
4. Leads at gauge plane 0.054-0.055 below seating plane shall be within 0.007 radius of positional tolerance at MMC relative to tab at MMC. Device may be measured by direct methods or by gauge and gauging procedure described on JEDEC gauge drawing GS-1.
5. $φb_2$ applies between L_1 and L_2. φb applies between L_2 and L minimum. Diameter is uncontrolled in L_1 and beyond L minimum.

Dimensional Outlines

JEDEC TO-218AC



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.165	.200	4.191	5.080	
b	.040	.063	1.016	1.600	
c	.053	.065	1.346	1.651	
c_1	.018	.030	.457	.762	
D	.485	.505	12.319	12.827	
D_1	.395	.415	10.033	10.541	
D_2	.070	.090	1.778	2.286	
E	.610	.640	15.494	16.256	1
E_1	.305	.320	7.747	8.128	
E_2	.040	.060	1.016	1.524	
e	.205	.225	5.207	5.715	
e_1	.420	.440	10.688	11.176	
L	.500	.610	12.700	15.494	
L_1	—	.125	—	3.175	2
φP	.157	.167	3.988	4.241	
Q	.094	.126	2.388	3.200	
R	.170	.190	4.318	4.826	
S	—	0.60	—	1.524	
Y	.626	.670	15.900	17.018	

92CS-37698R1

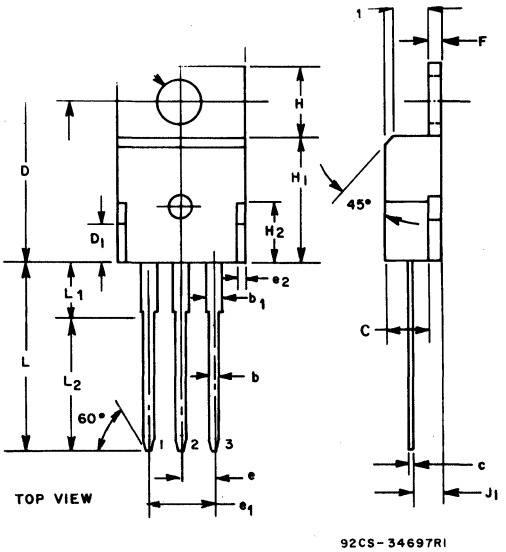
Notes:

1: Tab outline optional within boundaries of dimensions E and R.

2: Lead dimensions uncontrolled in L_1.

3: Controlling dimensions: inch.

JEDEC TO-220AB



SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.140	0.190	3.56	4.82
A_1	0.080	0.085	2.03	2.16
b	0.020	0.045	0.51	1.14
b_1	0.045	0.070	1.14	1.77
C	—	0.125	—	3.18
c	0.015	0.025	0.38	0.63
D	0.560	0.625	14.23	15.87
D_1	—	0.100	—	2.54
E	0.380	0.420	9.66	10.66
e	0.090	0.110	2.29	2.79
e_1	0.190	0.210	4.83	5.33
e_2	—	0.030	—	0.76
F	0.045	0.055	1.14	1.39
H	0.230	0.270	5.85	6.85
H_1	0.355	0.370	9.02	9.40
H_2	—	0.160	—	4.06
J_1	0.080	0.115	2.04	2.92
L	0.500	0.562	12.70	14.27
L_1	—	0.250	—	6.35
L_2	0.400	0.410	10.16	10.41
φP	0.139	0.161	3.531	4.089
Q	0.100	0.120	2.54	3.04

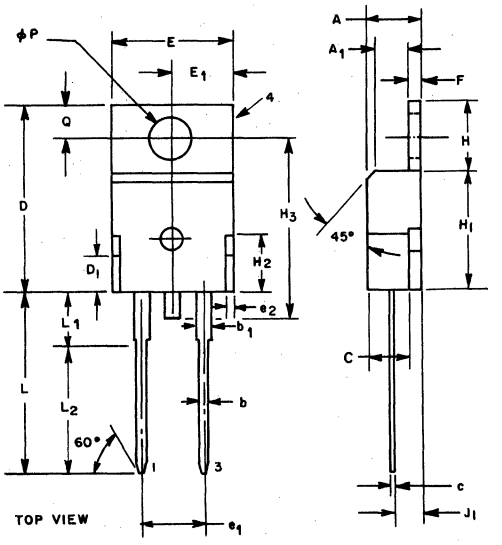
92CS-34697R1

NOTES:

1. Position of lead to be measured 0.250-0.255 in. (6.350-6.477 mm) from case.

Dimensional Outlines

JEDEC TO-220AC



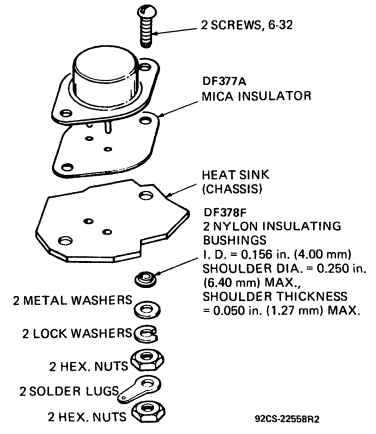
SYMBOL	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.140	0.190	3.56	4.82
A_1	0.080	0.085	2.03	2.16
b	0.020	0.045	0.51	1.14
b_1	0.045	0.070	1.14	1.77
C	—	0.125	—	3.18
c	0.015	0.025	0.38	0.63
D	0.560	0.625	14.23	15.87
D_1	—	0.100	—	2.54
E	0.380	0.420	9.66	10.66
e_1	0.190	0.210	4.83	5.33
e_2	—	0.030	—	0.76
F	0.045	0.055	1.14	1.39
H	0.230	0.270	5.85	6.85
H_1	0.355	0.370	9.02	9.40
H_2	—	0.160	—	4.06
H_3	—	0.600	—	15.24
J_1	0.080	0.115	2.04	2.92
L	0.500	0.562	12.70	14.27
L_1	—	0.250	—	6.35
L_2	0.400	0.410	10.16	10.41
ϕP	0.139	0.161	3.531	4.089
Q	0.100	0.120	2.54	3.04

NOTES:

1. **Position of lead to be measured 0.250-0.255 in. (6.350-6.477 mm) from case.**

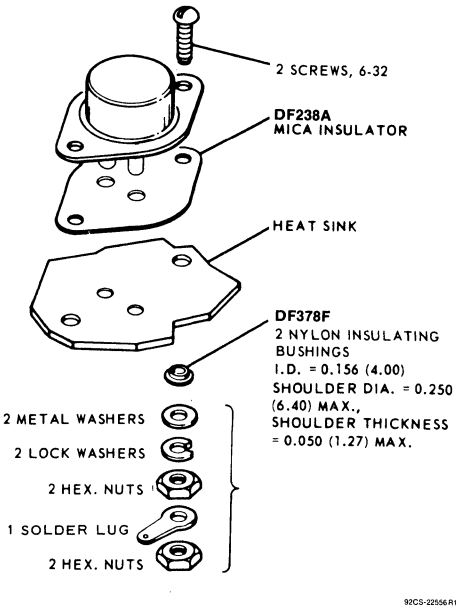
92CS-34830R1

Mounting Hardware

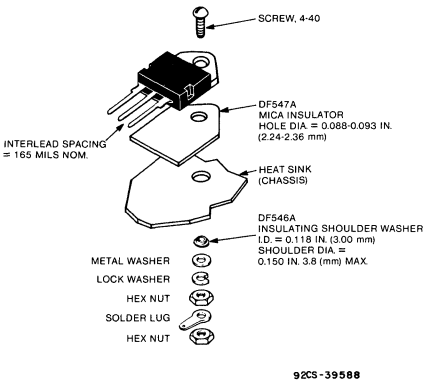


NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 12 in.-lbs. (0.14 kgf m).

Suggested mounting hardware for JEDEC TO-204AA (formerly JEDEC TO-3)

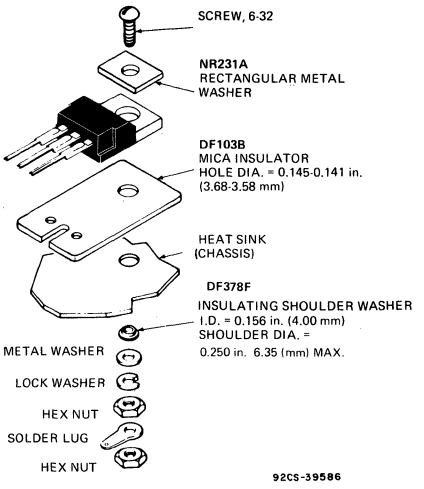


Suggested mounting hardware for JEDEC TO-204AE (formerly JEDEC TO-3)



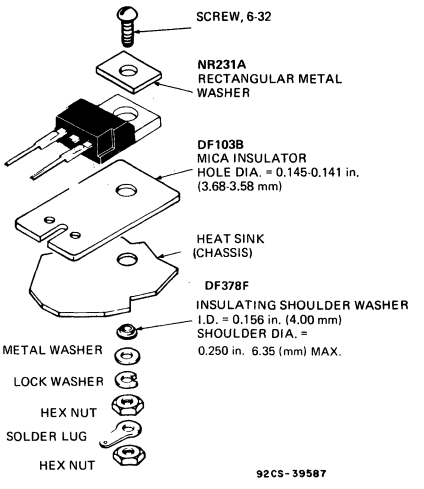
Suggested mounting hardware for JEDEC TO-218AC

Mounting Hardware



NOTE MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 8 in. lb. (0.09 kgf m)

Suggested mounting hardware for JEDEC TO-220AB



NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING FLANGE IS 8 in.-lb. (0.09 kgf-m)

Suggested mounting hardware for JEDEC TO-220AC

Application Notes

Understanding Power MOSFETS

by Tom McNulty

Power MOSFETs (Metal Oxide Semiconductor, Field-Effect Transistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This Note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the body by silicon contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor present a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Fig. 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Fig. 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely diffent from that of a bipolar transistor, which always retain its n-p-n character.

By virture of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful byproduct of the MOSFET process is the internal parasitic diode formed between source and drain, Fig. 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

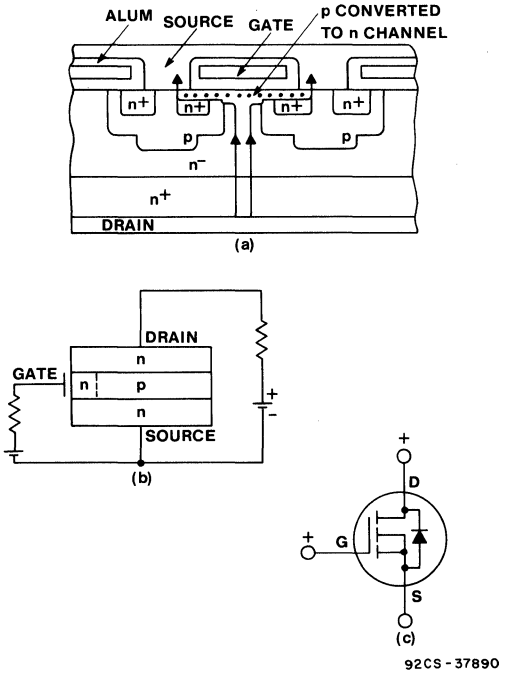


Fig. 1 - The MOSFET, a voltage-controlled device with an electrically isolated gate, uses majority carriers to move current from source to drain (a). The key to MOSFET operation is the creation of the inversion channel beneath the gate when an electric charge is applied to the gate (b). Because of the MOSFET's construction, an integral diode is formed on the device (c), and the designer can use this diode for a number of circuit functions.

Structure

RCA's power MOSFETs are manufactured using the vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cells varies according to the dimensions of the chip. For example, a 120-mil^2 chip contains about 5,000 cells; a 240-mil^2 chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(on)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(on)}$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_n, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(on)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(on)}$ value:

$$r_{DS(on)} = R_N/N$$

where N is the number of cells.

In reality, $r_{DS(on)}$ is composed of three separate resistances. Fig. 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(on)}$. The value of $r_{DS(on)}$ at any point of the curve is found by adding the values of the three components at that point:

$$r_{DS(on)} = R_{bulk} + R_{chan} + R_{ext}$$

where R_{chan} represents the resistance of the channel beneath the gate, and R_{ext} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{bulk} represents the resistance resulting from the narrow neck of n material between the two p layers, as shown in Fig. 1(a), plus the resistance of the current path below the neck and through the body of the device to the drain.

Note in Fig. 2 that R_{chan} and R_{ext} are completely independent of voltage, while R_{bulk} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(on)}$ is dominated by the sum of R_{chan} and R_{ext}. Above 150 volts, $r_{DS(on)}$ is increasingly dominated by R_{bulk}. Table I gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(on)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(on)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{bulk} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and more resistive to support high voltages, the bulk component of resistance rapidly increases (see Fig. 2) and begins to dominate the channel and external resistance. The $r_{DS(on)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(on)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(on)}$ in Fig. 2 holds only for a relatively small chip. Using a larger chip results in a lower value for $r_{DS(on)}$ because a large chip has more cells (See Fig. 3). A larger chip also increases MOSFET breakdown voltage capability.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(on)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the orginal. Although the cost does not rise exponentially, it is substantially more than the original cost.

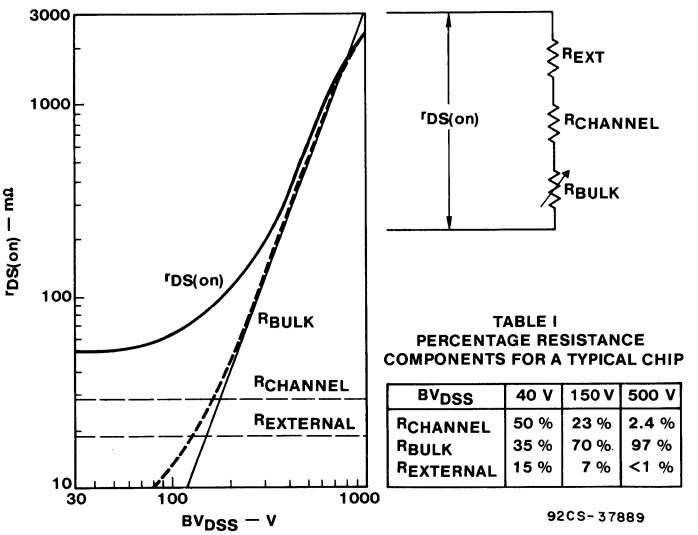


TABLE I
PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

BV_{DSS}	40 V	150 V	500 V
$R_{CHANNEL}$	50 %	23 %	2.4 %
R_{BULK}	35 %	70 %	97 %
$R_{EXTERNAL}$	15 %	7 %	<1 %

Fig. 2 - The drain-to-source resistance ($r_{DS(on)}$) of a MOSFET is not one but three separate resistance components.

AN-7244

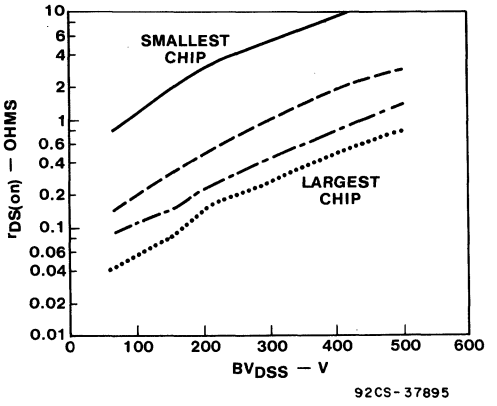


Fig. 3 - As chip size increases, $r_{DS(on)}$ decreases, and voltage handling capability increases.

Effects of Temperature

The high operating temperatures of bipolar transistors are a frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dicates that the carriers slow down as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Fig. 4.

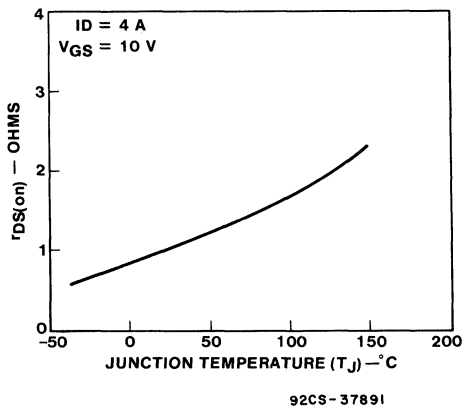


Fig. 4 - MOSFETs have a positive temperature coefficient of resistance, which greatly reduces the possibility of thermal runaway as temperature increases.

The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Fig. 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R, and capacitance, C. The capacitance, called C_{iss} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

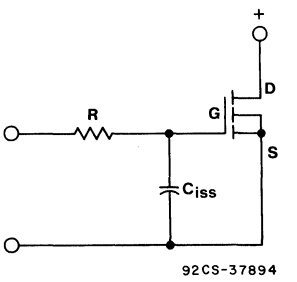


Fig. 5 - A MOSFET's switching speed is determined by its input resistance R and its input capacitance C_{iss}.

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure (R in Fig. 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFET in high-frequency (greater than 20 MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from data-sheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20 Ω/□. But whereas the total R value is not found on data sheets, the C value (C_{iss}) is; it is recorded as both a maximum value and in graphical form as

a function of drain-to-source voltage. The value of C_{iss} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1 to 10 MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic, shown in Fig. 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage ($_{gs}$). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{gs} level required to operate a MOSFET, note, from Fig. 6, that the device is not turned on (no drain current flows) unless V_{gs} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally V_{gs} for many types of DMOS devices is at least 2 volts. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Fig. 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10 volts, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5 volts, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of 10 volts, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

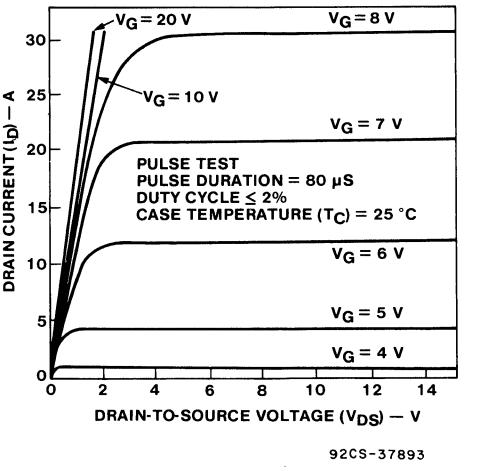


Fig. 6 - MOSFETs require a high input voltage (at least 10 V) in order to deliver their full rated drain current.

Switching Waveforms of the L²FET: A 5-Volt Gate-Drive Power MOSFET

by C. Frank Wheatley, Jr. and Harold R. Ronan, Jr.

The switching waveforms of a newly announced series of power-MOSFET devices called Logic-Level-FETs (L^2FETs) and featuring a 5-volt gate drive are presented and contrasted with those of the more conventional 10-volt-gate-drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascode from a low-voltage lateral MOS. The 2:1 advantage in rise and fall-time and the 4:1 reduction in switching "dynamic V(sat)" dissipation with constant drive power of the L^2FET over the 10-volt MOSFET are demonstrated and discussed.

BACKGROUND

A new series of power-MOSFET devices called Logic-Level FETs, or L^2FETs, is compatible with the 5-volt power supply used for logic circuitry. L^2FETs retain the on-resistance, drain-current, and blocking-voltage ratings of their 10-volt predecessors, but operate from a much less costly 5-volt supply.

The reduction in gate-drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100 nm to 50 nm (500 Å). Since the surface inversion of the MOS channel is determined by the gate-insulator voltage field, halving the insulator thickness halves the applied gate voltage without compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate-oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L^2FET over its 100-nm predecessor, where gate drive power is the same for both devices. The "dynamic V(sat)" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded-gate, depletion-mode, vertical JFET driven in cascode by a grounded-source, enhancement-mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L^2FET Characteristics Compared to Standard Types—A Brief Review

Thirty-two different power MOSFETs of the L^2FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figs. 1, 2, and 3, which are comparisons of the industry-standard RFM10N15 with its Logic-Level-FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L^2FET product currently available is limited to n-channel devices handling 200 volts or less, with 15 ampere ratings or less.)

Figs. 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L^2FET gate voltage is in parenthesis. The low-drain-voltage curves of Fig. 2 demonstrate that R_{on} has not been sacrificed in the L^2FET. Fig. 3 is the transfer characteristic comparison for

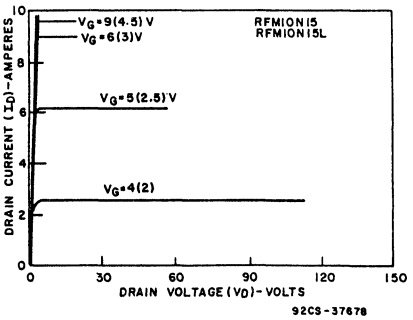


Fig. 1 - Drain-current versus drain-voltage curves for representative standard and L^2FET devices.

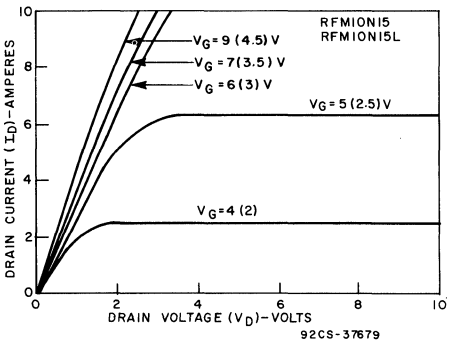


Fig. 2 - Drain-current versus low-drain-voltage curves for representative standard and L^2FET devices demonstrating that R_{on} has not been sacrificed in the L^2FET.

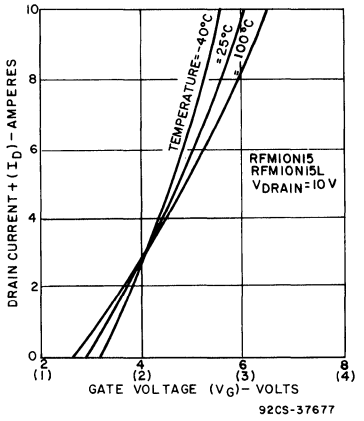


Fig. 3 - Transfer characteristic.

three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, L²FET values are in parentheses. It is evident from this curve that:

1. The threshold voltage is scaled down by a factor of two for the L²FET.
2. The threshold-voltage temperature coefficient in mV/° C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L²FETs have similar relationships to their respective predecessors.

SWITCHING WAVEFORMS WITH CONVENTIONAL DRIVE

The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal." If the standard device is driven between zero and ten volts with an R_g of 25 ohms, impedance transformation dictates that the L²FET should be driven between zero and five volts with an R_g of 6-1/4 ohms, thereby transforming open-circuit voltage and short-circuit current by factors of 2 (or 1/2). With these parameters, either drive system will supply a peak R_g, or generator dissipation, of one watt.

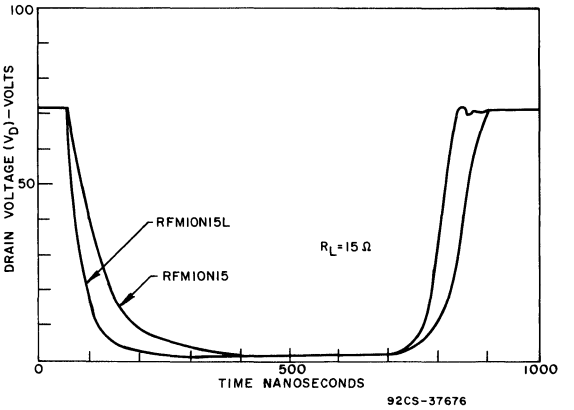
Fig. 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5-ampere, 75-volt resistive load line. The time scale is 100 nanoseconds per division. The table under the graph compares on-delay time, rise time, off-delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input-voltage and output-voltage waveforms.
Note that:

1. The rise and fall times are not symmetrical.
2. The L²FET is faster.
3. There is a "dynamic V(sat)" type of behavior.
4. The "dynamic V(sat)" is of a lesser amplitude for the L²FET.

These observations are discussed below.

SWITCHING WAVEFORMS WITH CONSTANT CURRENT DRIVE

The power MOSFET is a current-driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first-order approximation to a constant current where the



Type	Gate Drive	R_g (ohms)	td(on) (ns)	t(rise) (ns)	td(off) (ns)	t(fall) (ns)
RFM10N15 (100 nm)	0-10V	25	15	120	123	73
RFM10N15L (50 nm)	0-5V	6.25	11	57	104	62

Fig. 4 - Drain voltage versus time curves for representative standard and L²FET devices.

voltage compliance is determined by ground potential or the drive-circuit power-supply voltage. The on current may not equal the off current; this situation is addressed below.

Fig. 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{g1} = I_{g2}$, with gate-voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L²FET receives less drive power or energy. The value for I_{g1} and I_{g2} was chosen as 5 mA; the time scale is 1 μs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic V(sat)" even at slow switching speeds.

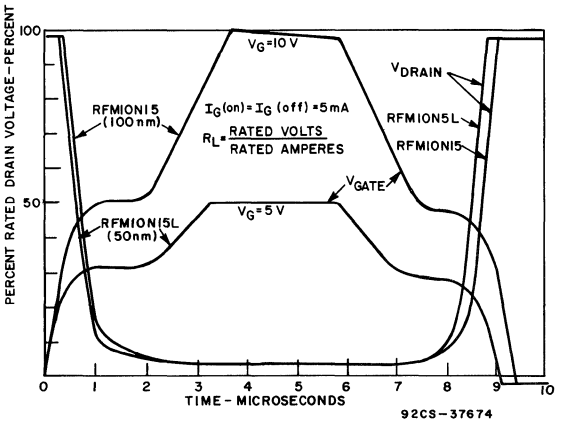


Fig. 5 - Characterization curves for representative devices driven from a current generator.

4. The "dynamic V(sat)" curves are symmetrical during the low-drain-voltage portion of the turn-on and turn-off portion.
5. The "dynamic V(sat)" curves are lower in amplitude by a factor of approximately two for the L^2FET.

LARGE-SIGNAL EQUIVALENT CIRCUIT OF THE MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional power MOSFET must first be understood. Fig. 6 shows a properly proportioned cross-sectional view of the power MOSFET.

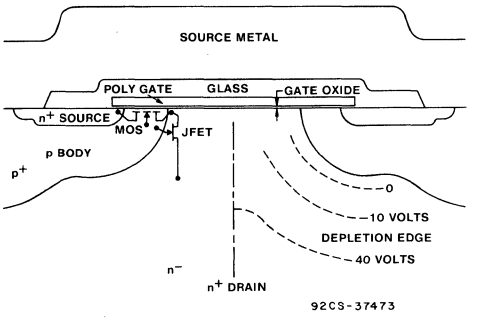


Fig. 6 - Cross section of power MOSFET.

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n^- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion-mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n^+ region usually thought of as being the MOSFET drain. This situation is shown in Fig. 6, where the cross-sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Fig. 6. The right half indicates the edge of the depletion width for several drain voltages. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Fig. 7. Note that the third-quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

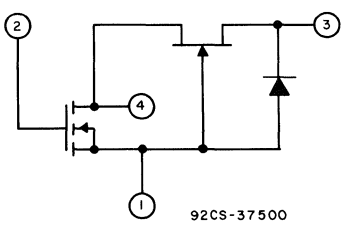


Fig. 7 - Schematic representation of the cross section of Fig. 6.

Interelectrode Capacitance

The equivalent circuit of Fig. 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the small-signal equivalent circuit of the MOS and the JFET. Of course, the MOS and JFET small-signal equivalent circuits are nonlinear functions of voltage and current and invariant with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three-terminal characterization of this four-node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reduces the power MOSFET to the capacitor network of Fig. 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

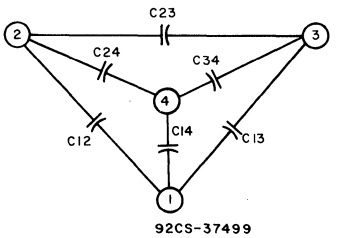


Fig. 8 - Capacitor-network representation of the power MOSFET.

When current does flow, node (4) of Fig. 7 is a low-impedance node due to the source-follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate-To-Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Fig. 6 shows that the gate-to-source capacitance (C_{12}) is that from the poly gate upward through the thick oxide to the source metal. In addition, there is a contribution from the poly gate to the n^+ source through the thin gate oxide. Additionally a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate-To-Drain Capacitance, C_{23}

Capacitor C_{23} exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C_{23} exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate-to-Internal-Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the middle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n^- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulation layer ceases to exist when the external drain voltage minus the IR drop through the n^- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

WAVEFORMS EXPECTED FROM THE MODEL

The following discussion relates the prior model discussion to the waveforms of Fig. 5. The discussion begins with the gate voltage at +5 or +10 volts and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to I_D(max) and the drain voltage equals I_D(max) times r_{DS}(on).

Gate-Voltage Slope — t_{off} Delay

As time progresses, $I_g = -5$ mA, which must flow through $C_{12} + C_{23} + C_{24}$ of Fig. 8 because the MOS and the JFET are both heavily biased into conduction. Therefore, $dV_4/dt = dV_3/dt =$ nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_g/dt = I_g/(C_{12} = C_{24}) \quad (1)$$

Gate-Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant-current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no long flows from C_{12} during the constant gate-voltage plateau.

Drain-Voltage Shallow Slope

Since C_{23} is still zero, all gate current must flow from C_{24}. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Fig. 7 must ramp at a linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_d/dt = I_g/C_{24} \quad (2)$$

Again this curve will approximate a straight line.

Drain-Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n^- voltage directly beneath the gate oxide, and differs from the drain voltage by an amount nearly equal to $I_D r_{DS}$[on].)

Since the drain voltage is still fairly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_d/dt.

JFET Pinch-Off Voltage — Drain-Voltage Steep Slope

As the drain voltage approaches the pinch-off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET source-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate-Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain-voltage waveform.

Gate-Voltage Slope — t(on) Delay

When the drain is totally off, most of the gate current flows from C_{12}. Again, this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_g/dt = I_g/C_{12} \quad (3)$$

NEW SWITCHING CHARACTERIZATION FOR POWER MOSFETS

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant-current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate-charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive circuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit — Drive

A test circuit is shown in Fig. 9. The heart of this circuit is the RCA-CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Fig. 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximately 0.9). The actual value depends upon the input differential-input voltage. As a comparator, the differential voltage is large, resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5 mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads to parallel the chips rather than wiring many sockets. However, this arrangement may require an increase in the bypass-capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1 megohm or 10 megohm shunting impedance of the scope would load the high-impedance circuitry associated with the MOSFET gate.

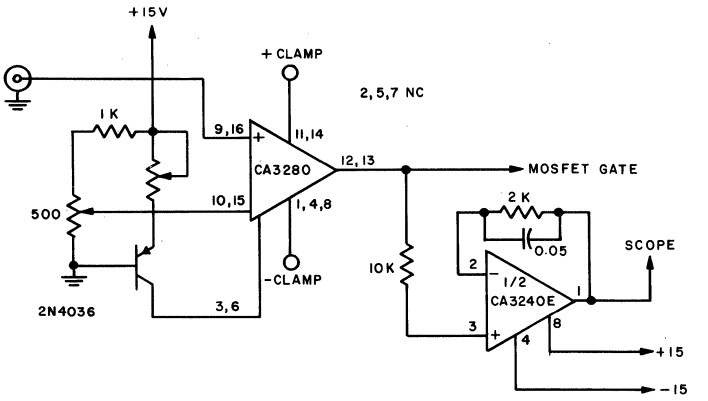


Fig. 9 - Test circuit. 92CS-37501

Testing Conditions

A pulse generator is set for 50-μs on-time duration and approximately 25-ms repetition rate (about 0.2% duty cycle). The $\pm$ clamp voltages are set to the appropriate values. The power-MOSFET load resistor is chosen to equal the maximum-rated voltage divided by the maximum-rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several microseconds exists at the +10-volt level. Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased to maximum-rated value. The L^2FETs would be tested at +5-volts gate clamp.

Fig. 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Fig. 10(a) is the 3-volt signal to the CA3280. Fig. 10(b) is the power-MOSFET gate current. In this example, the amplitude is $\pm$1 mA with a third state of 0 mA. Fig. 10(c) displays the gate voltage and the drain voltage, 10 volts peak-to-peak and 150 volts peak-to-peak. Fig. 10(d) is a piece-wise linear approximation of Fig. 10(c). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Fig. 10 is 100 microseconds full scale.

There are some features of the gate and drain-voltage waveforms that should be noted. These features are consistent with the equivalent-model discussion.

1. The waveforms during the positive gate-current time are symmetrical to those during the negative gate-current time. Exceptions will occur for very fast or very slow switching, and for nonsymmetrical current drive. These exceptions are discussed below.
2. The drain-voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain-voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain-voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times r_{DS}(on).
5. The gate-voltage waveform contains three near-straight-line segments during the positive-gate-current transition time.

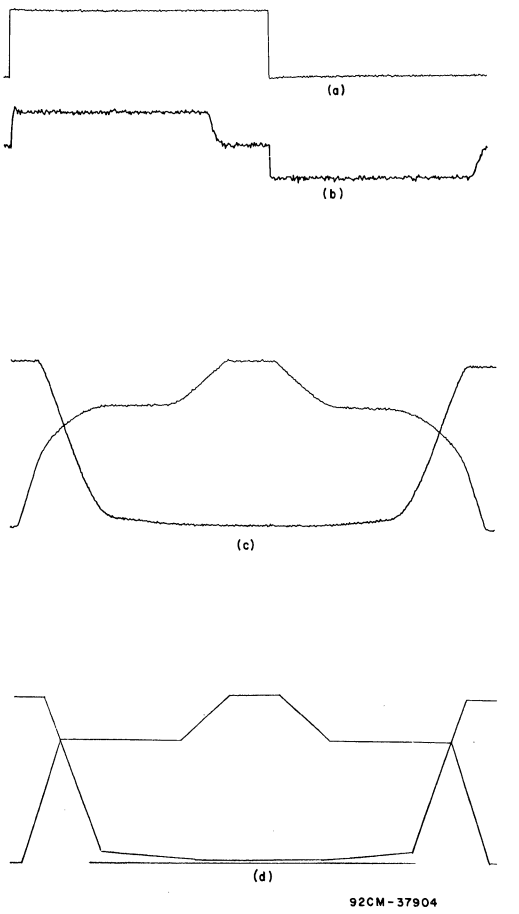


Fig. 10 - (a) 3-volt signal to the CA3280, (b) power-MOSFET gate current, (c) gate and drain voltage, (d) piece-wise linear approximation of 10(c).

Application of the Switching Data

Fig. 11 is a family of curves similar to Fig. 10(c), where the drain supply voltage is fixed at four values. Note that the ordinate is 10-volts full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_g) microseconds full scale, where I_g is the actual gate-drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

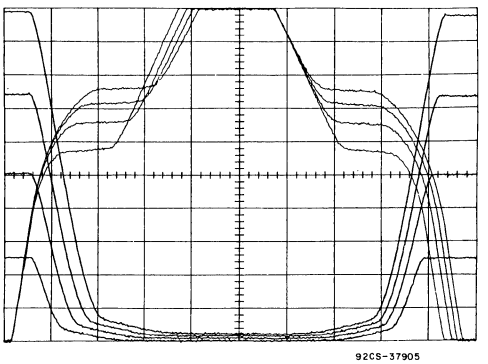


Fig. 11 - Curves similar to those of Fig. 10(c) with drain supply voltage fixed at four values.

Symmetrical Current Drive

Waveforms of Fig. 11 will scale in an inverse manner with gate current. Driving current was varied from ±200 mA to ±2 μA for the device of Fig. 11. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Fig. 12 and compared to the inverse scaling suggested by Fig. 11.

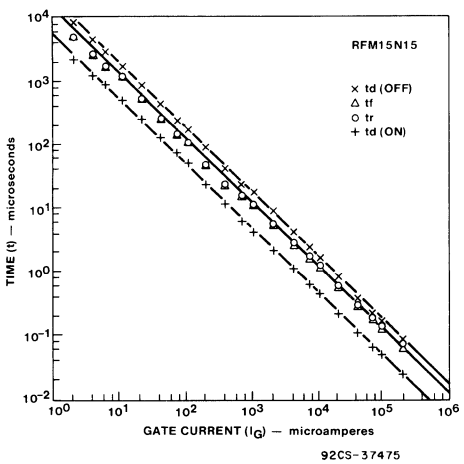


Fig. 12 - Various time measurements compared to the inverse scaling suggested by Fig. 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the inverse scaling. This condition was not noted on Fig. 12 for gate currents as low as ±2 μA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. As a result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Fig. 12, even though the gate current was increased to ±200 mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piece-wise linear methods will yield the gate current, which will permit the proper piece-wise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Fig. 11, dividing it into 10 equal voltage segments; for example, V_g = 0, 1, 2, ... 9, 10 volts.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piece-wise linear gate current for each time segment. I_{g1} = (10 - 0.5)/100 = 95 mA, I_{g2} = (10 - 1.5)/100 = 85 mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Fig. 11 corresponding to an average gate voltage of 9.5, 8.5, ... 1.5, 0.5 volts. Call these segments 11, 12, ... 19, 20.
7. In that the pulse-generator voltage is now zero volts, calculate I_g as:
   I_{g11} = (0 - 9.5)/100 = -95 mA, I_{g12} = (0 - 8.5)/100 = -85 mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Fig. 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymmetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Fig. 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100 mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

AN-7254

GATE-VOLTAGE PROPAGATION EFFECTS

Most power-MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage wavefront applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figs. 13(a), (b), and (c) show the increasing effect of gate-voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Fig. 13(c).

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher R_{ON}).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield "breakthrough" devices unless used in combination.

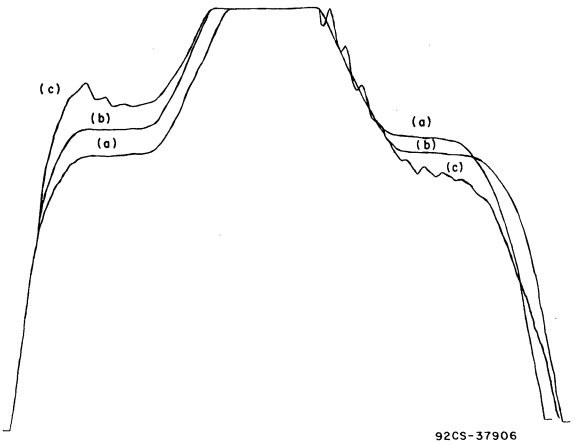


Fig. 13 - Curves showing the increasing effect of gate-voltage propagation.

Any of the above methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of R_{ON} per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

REFERENCES

1. "Power MOSFET Switching Waveforms—A New Insight," H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.
2. "Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed," E. Oxner, Proc. Powercon 9, April 1982.

Power MOSFET Switching Waveforms: A New Insight

by Harold R. Ronan, Jr. and C. Frank Wheatley, Jr.

The examination of power MOSFET voltage and current waveforms during switching transitions reveals that the device characterization now practiced by industry is inadequate. In this Note, device waveforms are explained by considering the interaction of a vertical JFET driven in cascode from a lateral MOSFET in combination with the interelectrode capacitances. Particular attention is given to the drain-voltage waveform and its dual-slope nature. The three terminal capacitances now published by the industry are shown to be valid only for zero drain current. For cases where the gate drive is a voltage step generator with internal fixed resistance, the drain voltage characteristics are inferred from the gate current drive behavior and compared to observed waveforms. The nature of the "asymmetric switching times" is explained.

A waveform family is proposed as a more descriptive and accurate method of characterization. This new format is a plot of drain voltage and gate voltage versus normalized time. A family of curves is presented for a constant load resistance with V_{DD} varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

DEVICE MODELS

The keystone of an understanding of power MOSFET switching performance is the realization that the active device is bimodal and must be described using a model that accounts for the dual nature. Buried in today's power MOSFET devices is the equivalent of a depletion layer JFET that contributes significantly to switching speed. Fig. 1 is a cross-sectional view of a typical power MOSFET, with MOSFET/JFET symbols superimposed on the structure.

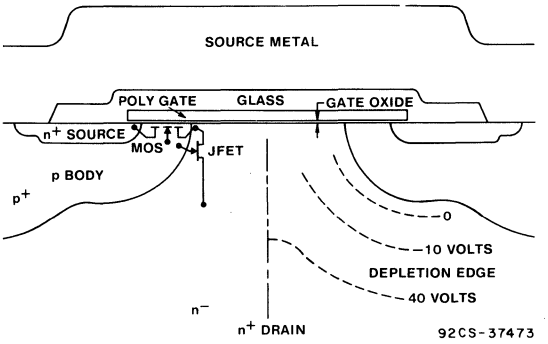


Fig. 1 - Cross-sectional view of MOSFET showing equivalent MOS transistor and JFET.

Fig. 2 is obtained by taking the lateral MOS and vertical JFET from this conception and adding all the possible node-to-node capacitances. Computed values of the six capacitances for a typical device structure suggest that device behavior may be adequately modeled using only three capacitors in the manner of Fig. 3. This is the model to be employed for analysis and study.

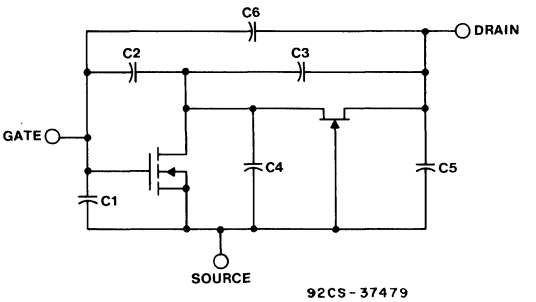


Fig. 2 - MOS transistor with cascode-connected JFET and all capacitors.

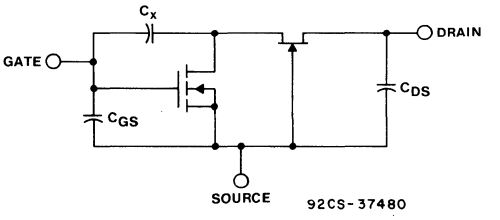


Fig. 3 - Fig. 2 simplified.

GATE DRIVE: CONSTANT VOLTAGE OR CONSTANT CURRENT

Before moving on to the study of the equivalent circuit states of the model, a gate-drive forcing function which is easy to represent, relates to reality, and best illustrates device behavior must be chosen. The choice may be immediately narrowed to two:

(1) An instantaneous step voltage with internal resistance R, Fig. 4.
(2) An instantaneous step current with infinite internal resistance, Fig. 5.

Power MOSFET devices are highly capacitive in nature; hence, simple capacitor responses to the forcing functions offer a good vehicle for comparison. The advantageous choice is immediately obvious: Fig. 5. Voltage/time responses dominated by capacitance are straight lines (when constant current is used). The slope of these lines is

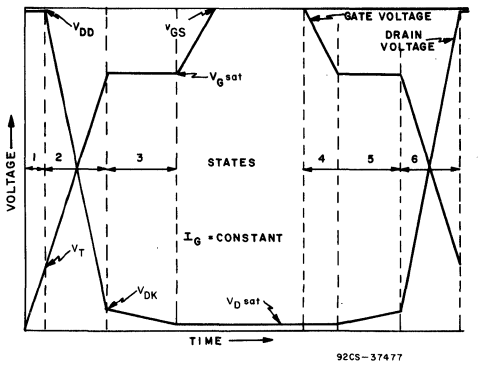


Fig. 4 - Idealized power-MOSFET waveforms.

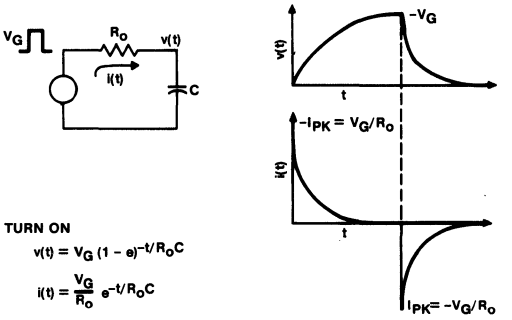


Fig. 5 - Step-voltage forcing function.

proportional to current and inversely proportional to capacitance. Analytically, then, constant current is most convenient. It is quite another matter, however, to build a bidirectional current drive that is accurate across the many decades of both current and time required to establish experimental verification.

SIX STATES

To completely characterize power MOSFET switching waveforms, the six states that a device assumes, Fig. 6, must be addressed:

STATE	MOS	JFET
Turn-on 1	Off	Off
Turn-on 2	Active	Active
Turn-on 3	Active	Saturated*
Turn-off 4	Saturated	Saturated
Turn-off 5	Active	Saturated
Turn-off 6	Active	Active

*The term saturated is taken to mean a constant low-voltage drain-source condition.

Equivalent Circuit

The lumped-parameter model of Fig. 3, with the cascode-connected JFET, can now be reduced to the linear equivalent circuit of Fig. 7, and the six device states investigated from full off to full on.

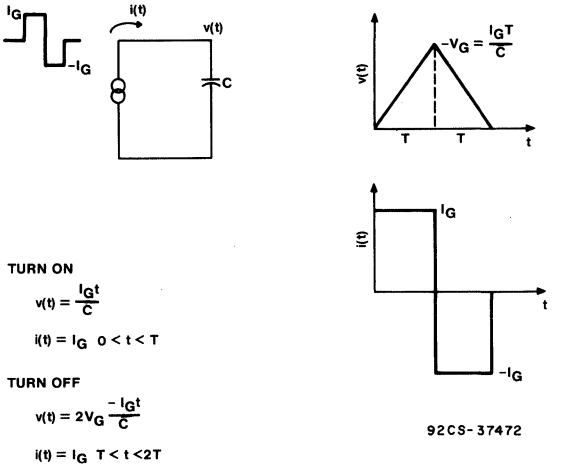
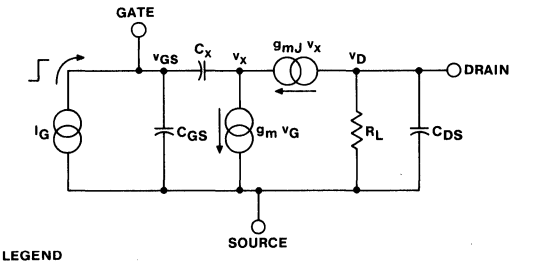


Fig. 6 - Step-current forcing function.



LEGEND

v_{GS} - Gate Voltage	C_{DS} - Drain-Source Capacitance
v_x - JFET Driving Voltage	g_m - MOSFET Transconductance
v_D - Drain Voltage	g_{mJ} - JFET Transconductance
C_{GS} - Gate-Source Capacitance	R_L - Drain Load Resistance
C_x - MOSFET Feedback Capacitance	I_G - Constant Current Amplitude

92CS-37485

Fig. 7 - Power MOSFET equivalent circuit.

State 1: MOS Off, JFET Off

In a power-MOSFET device, no drain current will flow until the device gate threshold voltage, V_T, is reached. During this time, the gate current drive is only charging the gate-source capacitance. More accurately, I_G is charging C_{iss} ($C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted), the capacitance designation published by the industry.

The current generators, $g_m v_G$ and $g_{mJ} v_x$ are open circuits for zero drain current, and R_L is presumed to be so low as to represent a short circuit (generally true for practical applications). This is academic however since C_{GS} is very much larger that C_e. The time to reach threshold, then, is simply:

$$t = \frac{C_{iss} V_T}{I_G}$$

State 2: MOS Active, JFET Active

This state graphically illustrates the dramatic influence that the JFET has on the power MOSFET drain-voltage waveform. Instead of having to discharge Cx from V_{DD} to ground, the lateral MOSFET need only swing v_x to ground, a much smaller voltage thanks to the grounded gate JFET. Since

the interaction of R_L with the device capacitances has a second-order effect on the drain voltage, the equivalent circuit of Fig. 7 predicts a drain voltage change of:

$$dv_G/dt = g_m R_L I_G/[C_{GS} + C_x(1 + g_m/g_{mJ})]$$

In all but the smallest power-MOSFET devices, C_x is several thousand picofarads and g_m/g_{mJ} is of the order of 3:1. Power-MOSFET devices exhibit a high dv_D/dt switching rate because of the cascode-connected JFET, not because C_{rss} ($C_{rss} = C_{GD}$) is a small value, as zero-drain-current data-sheet capacitance values might lead one to believe. If C_{rss} were, in actuality, small, long drain voltage tails would not exist. The tail response is a direct result of JFET saturation. In order to delineate the transition from state 2 to state 3, a drain voltage at which the transition occurs must be defined. V_{DK} is the knee voltage at which linear extrapolations of drain-voltage slopes intersect. The time duration of state 2 is:

$$t = (V_{DD} - V_{DK})[C_{GS} + C_x(1 + g_m/g_{mJ})]/g_m R_L I_G$$

State 3: MOS Active, JFET Saturated

When the JFET saturates, the $g_{mJ}v_x$ current generator becomes a short circuit and the equivalent circuit predicts:

$$dv_D/dt = g_m R_L I_G/[C_{GS} + C_x(1 + g_m R_L)]$$

This is the Miller effect so often referred to in older texts that describe the behavior of grounded-cathode vacuum-tube amplifier circuits. Allowing for the fact that $1 + g_m R_L$ is approximately equal to $g_m R_L$ and $C_x(1 + g_m R_L)$ is very much larger than C_{GS}, the expression for drain-voltage tail time is:

$$t = (V_{DK} - V_D[sat])C_x/I_G$$

State 4: MOS Saturated, JFET Saturated (Turn-Off)

In this state, in addition to $g_{mJ}V_x$ being shorted, the $g_m V_G$ current generator is shorted, and I_G is occupied with charging C_x and C_{GS}, in parallel, from the peak value of V_G to V_G(sat). The time required for this is:

$$t = (V_G - V_G(sat)(C_{GS} + C_x)/I_G$$

Since a value for C_{GS} may be measured independently of switching time, the method described is the simplest way of determining C_x.

On turn-off, the state time equations are equally applicable, but in reverse order (states 5 and 6); see the idealized waveform of Fig. 4.

Experimental Verification

The four switching states just analyzed indicate that for a given device, all four switching state times are inversely proportional to the magnitude of the gate drive current. Fig. 8 illustrates the switching performance of a typical power MOSFET across three decades of gate drive current and time. In each case the data slope is almost a perfect -1.

A NEW DEVICE CHARACTERIZATION

Fig. 8 could not be a reasonable device data sheet presentation because it does not give the designer any information on a typical value for C_x, nor does it convey how V_{DK}, g_m, g_m/g_{mJ}, and V_G(sat) vary with drain current. What would be of enormous value to the designer is a plot of $v_D(t)$, $v_G(t)$ for selected values of V_{DD} and I_D within device ratings. A reasonable characterization would be as follows:

1. The x axis would be normalized in terms of gate current drive.
2. The y axis would be normalized in terms of percent maximum rated V_D (0 to 100%).
3. $R_L = V_D(max)/I_D(max)$ would define the drain load resistance.
4. Four plots of $v_D(t)$, $v_G(t)$ at 100%, 75%, 50%, and 25% V_D(max) would be shown.

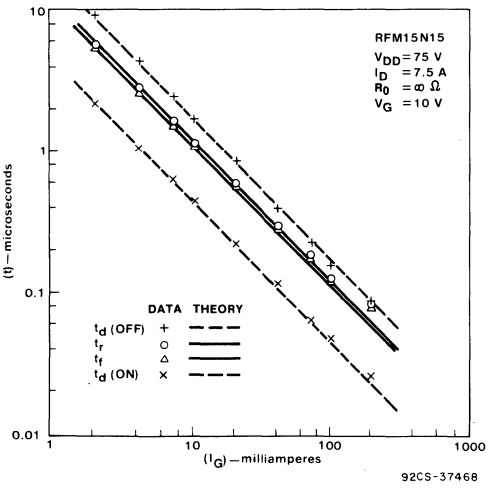


Fig. 8 - Constant gate current switching time.

Fig. 9 is such a plot for the RFM15N15 power MOSFET. With such a plot, a designer can estimate device switching performance under any resistive gate/drain conditions.

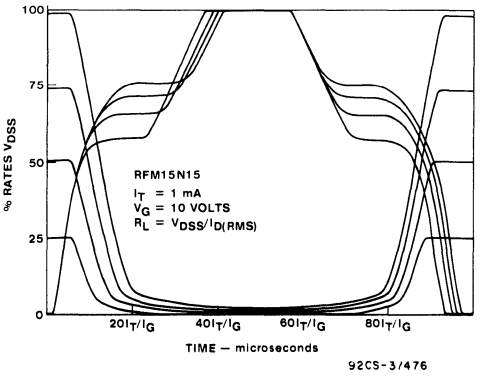


Fig. 9 - Normalized RFM15N15 switching waveforms for constant gate-current drive.

STEP-VOLTAGE GATE DRIVE

The majority of power MOSFET applications employ a step gate-voltage input with a finite source resistance R_o. Often R_o for turn-on is not the same as R_o for turn-off. How can switching times for these situations be estimated using the switching characterization curves just described? The analysis for resistive step voltage inputs, which is complex because the gate current is no longer constrained to be constant, but is a function of device gate-voltage response, is covered in Appendix A. (A second, shorter appendix, B, has been added to illustrate the estimation of R_o for some practical gate drive circuits.) Table I summarizes the common switching equations, and indicates the appropriate I_G to be used in each state for relating step voltage drives to the characterization curves.

Table I - Common Switching Equations

	CONSTANT CURRENT	STATE 1: MOS OFF, JFET OFF	CONSTANT VOLTAGE
TURN ON	$t = \frac{C_{iss} V_T}{I_G}$		$t = R_o C_{iss} \ln \frac{[1]}{[1 - V_T/V_G]}$
	$I_G = I_T$	STATE 2: ACTIVE, ACTIVE	$I_G = (V_G - V_T)/R_o$
	$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		
	$I_G = I_T$	STATE 3: ACTIVE, SATURATED	$I_G = (V_G - V_{Gsat})/R_o$
	$t = \frac{(V_{DK} - V_{Dsat})C_X}{I_G}$		
TURN OFF	$I_G = -I_T$	STATE 4: SATURATED, SATURATED	$I_G = -V_G/R_o$
	$t = \frac{(C_{GS} + C_X)(V_G - V_{Gsat})}{I_G}$		$t = R_o(C_{GS} + C_X) \ln (V_G/V_{Gsat})$
	$I_G = -I_T$	STATE 5: ACTIVE, SATURATED	$I_G = -V_{Gsat}/R_o$
	$t = \frac{(V_{DK} - V_{Dsat})C_X}{I_G}$		
	$I_G = -I_T$	STATE 6: ACTIVE, ACTIVE	$I_G = -V_{Gsat}/R_o$
	$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_X(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		

92CS-37469

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_o$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Fig. 10 is merely a variation of Fig. 8. Using the relationships of Table I, the observed differences between Figs. 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_o equalling the constant I_G, $t_d(on)$, t_r, $t_d(off)$, and t_f will all be longer, as predicted by the ratios of the gate drive currents of Table I. Notice also that t_r, t_f switching symmetry is disrupted by the use of a step voltage with source resistance R_o.

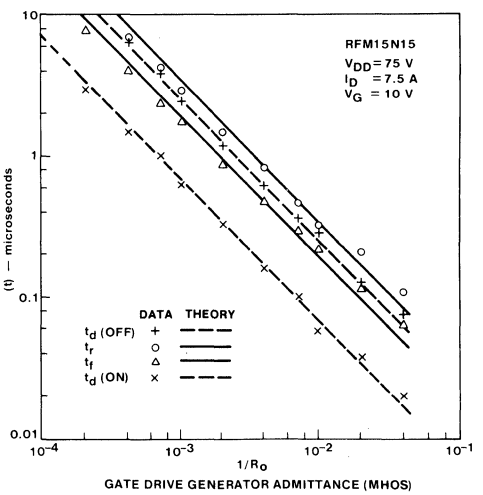
For states 2 and 6 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_T}$$

For states 3 and 5 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_G(sat)}$$

Utilization of available maximum gate drive voltage and current can be optimized for fastest power MOSFET switching speed through the use of constant-current gate drive at the expense of increased gate-drive circuit complexity.



92CS-37474

Fig. 10 - Constant gate voltage switching time.

USING THE CHARACTERIZATION CURVES, FIG. 9

To estimate the switching times for an RFM15N15 power MOSFET under the conditions V_G = 10V, V_{DD} = 75V, R_o = 100 ohms, and R_L = 10 ohms, proceed as follows.

State 1: MOS Off, JFET Off

This time can be estimated without recourse to the curves.

$$t = 100(1200 \times 10^{-12}) \ln[1/(1 - 4/10)]$$

$$t = 61 \text{ ns}$$

State 2: MOS Active, JFET Active

$$I_G = (10 - 4)/100 = 60 \text{ mA}$$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{60} = \frac{9}{60} = 150 \text{ ns}$$

State 3: MOS Active, JFET Saturated

$$I_G = (10 - 7)/100 = 30 \text{ mA}$$

$$t = \frac{(\text{curve division}) \times I_T\ \mu s}{30} = \frac{14}{30} = 467 \text{ ns}$$

State 4: MOS Saturated, JFET Saturated

$$C_{GS} + C_x = (\text{gate voltage slope})(\text{test current})$$

$$= (1.5 \times 10^{-6} \text{s}/5 \text{ volts})(10 \text{ mA})$$

$$= 3000 \text{ pF}$$

$$t = 100(3000 \times 10^{-12}) \ln[10/6.6]$$

$$t = 125 \text{ ns}$$

State 5: MOS Active, JFET Saturated

$$I_G = 6.6/100 = 66 \text{ mA}$$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{66} = \frac{8}{66} = 121 \text{ ns}$$

Fig. 11 shows RFM15N15 waveforms using the conditions specified in the example.

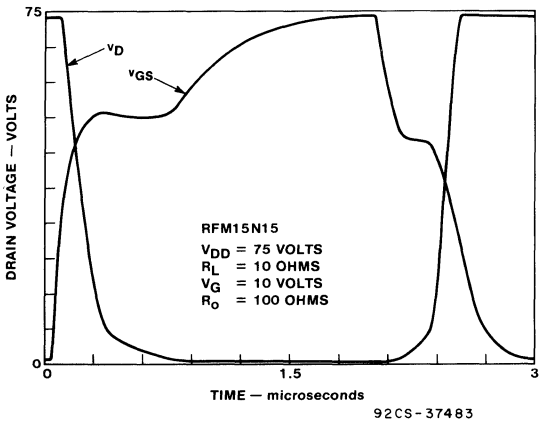


Fig. 11 - Step gate voltage input to an RFM15N15.

State	Calculated Time (t_c, ns)	Measured Time (t_m, ns)	Ratio (t_c/t_m)
1	61	60	1.02
2 + 3	671	670	0.92
4	125	137	0.91
5 + 6	318	375	0.85

For peak gate voltages other than 10 volts, and load resistances other than $V_{DSS}/I_{D(rms)}$, the equations of Table I may be used in conjunction with slope estimates from the characterization curves for C_x and $C_{GS} + C_x(1 + g_m/g_{mJ})$ at the appropriate drain-current level.

CHARACTERIZATION-CURVE LIMITS

The switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of microamperes, device dissipation is the limiting factor. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. However, as Fig. 12 graphically shows, the characterization is valid across five decades of gate current and switching time, allowing all but a very few switching applications to be described by the characterization curves of Fig. 9.

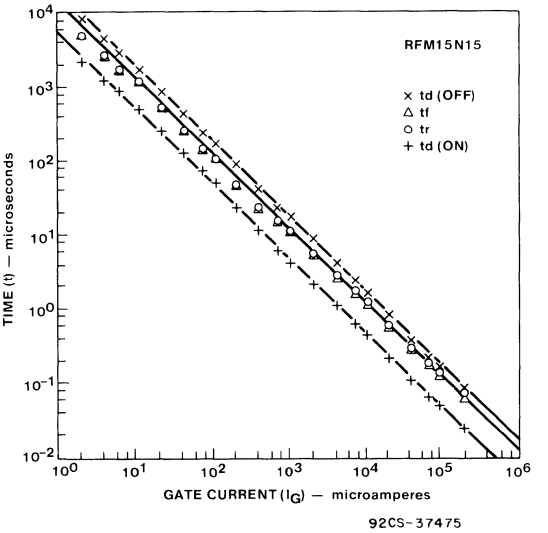


Fig. 12 - Five decades of linear response.

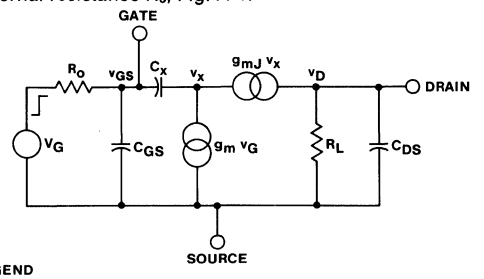
CONCLUSIONS

The viability of the proposed characterization curves using constant current has been demonstrated and the limits of application defined. The existence of a vertical JFET in a power MOSFET makes data-sheet capacitances of little use for estimating switching times. The classical method of defining switching time by 10% and 90% is a poor representation for power MOSFETs because of the dual-slope nature of the drain waveforms. Switching influences are masked because the 10% level is controlled by one mechanism and the 90% level by another. Device comparisons based on the classical switching definition can be very misleading.

APPENDIX A - ANALYSIS FOR RESISTIVE STEP VOLTAGE INPUTS

STEP VOLTAGE GATE DRIVE

To obtain the necessary relationships, six device switching states must be examined using the same device equivalent circuit as was used for the constant-gate-current case, but with the forcing function replaced with a step voltage with internal resistance R_o, Fig. A-1.



LEGEND

v_{GS} - Gate Voltage	C_{DS} - Drain-Source Capacitance
v_x - JFET Driving Voltage	g_m - MOSFET Transconductance
v_D - Drain Voltage	g_{mJ} - JFET Transconductance
C_{GS} - Gate-Source Capacitance	R_L - Drain Load Resistance
C_x - MOSFET Feedback Capacitance	v_G - Constant Voltage Amplitude

92CS-37470

Fig. A-1 - Power MOSFET equivalent circuit.

STATE 1: MOS OFF, JFET OFF

As before, both current generators are open circuits, reducing the equivalent circuit to simply charging C_{iss} through R_o.

$$t = R_o C_{iss} \ln(1/(1 - V_T/V_G))$$

$$I_{PK1} = V_G/R_o$$

STATE 2: MOS ACTIVE, JFET ACTIVE

Before proceeding, it is wise to examine an actual device response and make use of available simplifications. Fig. A-2 shows $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage. For truly resistive switching, realize that these waveforms are only mirror images of their voltage counterparts $v_G(t)$ and $v_D(t)$. Using Fig. A-2, applicable gate currents for each of the device states may be listed.

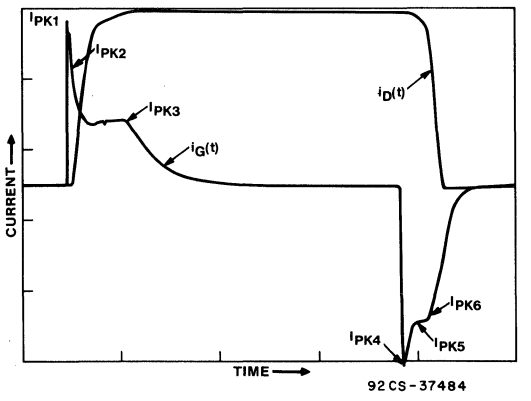


Fig. A-2 - $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage.

Turn-On

State 1: MOS Off, JFET Off

$$I_{PK1} = V_G/R_o$$

State 2: MOS Active, JFET Active

$$I_{PK2} = (V_G - V_T)/R_o$$

State 3: MOS Active, JFET Saturated

$$I_{PK3} = (V_G - V_G(sat))/R_o$$

Turn-Off

State 4: MOS Saturated, JFET Saturated

$$I_{PK4} = V_G/R_o$$

State 5: MOS Active, JFET Saturated

$$I_{PK5} = V_G(sat)/R_o$$

State 6: MOS Active, JFET Active

$$I_{PK6} = V_G(sat)/R_o$$

The equivalent circuit of Fig. A-1 predicts that:

$$dv_D/dt = - g_m R_L (V_G - V_T) e^{-t/T1} / T1$$

where $T_1 = R_o C_{GS} + (1 + g_m/g_{mJ}) R_o C_x$

Note that $g_m R_L (V_G - V_T)$ is usually an order of magnitude greater than V_{DD}, indicating that the drain voltage is discharging toward a very large negative value. The device operation, then, is on the early, almost linear, portion of the exponential, where $e^{-t/T1}$ approximates unity. The drain current of Fig. A-2, and hence the drain voltage, does indeed exhibit a linear decrease with time.

Thus, for state 2:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PK2}}$$

where $I_{PK2} = (V_G - V_T)/R_o$

STATE 3: MOS ACTIVE, JFET SATURATED

Because of the Miller effect, the gate voltage and, hence, the gate current, is almost constant during the tail time. The equivalent circuit then predicts:

$$\frac{dv_D}{dt} = \frac{g_m R_L I_G}{C_{GS} + (1 + g_m R_L) C_x} = \frac{I_G}{C_x}$$

$$I_G = I_{PK3} = (V_G - V_G[sat])/R_o$$

$$\text{and } t = \frac{(V_{DK} - V_D[sat]) C_x}{I_{PK3}}$$

STATE 4: MOS SATURATED, JFET SATURATED (TURN-OFF)

Both equivalent-circuit generators are short circuits, and the gate drive is discharging C_x in parallel with C_{GS} through R_o.

$$t = R_o(C_{GS} + C_x) \ln[V_G/V_G(sat)]$$

$$I_{PK4} = V_G/R_o$$

APPENDIX A (Cont'd)

STATE 5: MOS ACTIVE, JFET SATURATED

The JFET current generator $v_x g_{mJ}$ remains shorted and the MOS generator, $v_G g_m$, is operative.

$$t = \frac{(V_{DK} - V_D[sat])C_x}{I_{PK5}}$$

$$I_{PK5} = V_G(sat)/R_o$$

STATE 6: MOS ACTIVE, JFET ACTIVE

The Miller effect is now reduced by the activation of $V_G g_{mJ}$, and the equivalent circuit predicts:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PK6}}$$

$$I_{PK6} = V_G(sat)/R_o$$

APPENDIX B - ESTIMATING R_O FOR SOME TYPICAL GATE-DRIVE CIRCUITS

CASE 1: TYPICAL PULSE-GENERATOR DRIVE, FIG. B-1

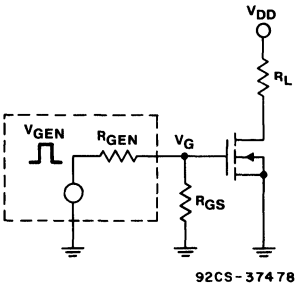


Fig. B-1 - Typical pulse-generator drive circuit.

Turn-On and Turn-Off

$R_o = R_{GEN}R_{GS}/(R_{GEN} + R_{GS})$

For the typical case where R_{GEN} = 50 ohms, and a coaxial-cable termination of 50 ohms, R_o = 25 ohms and $V_G = V_{GEN}/2$

CASE 2: VOLTAGE-FOLLOWER GATE DRIVE, FIG. B-2

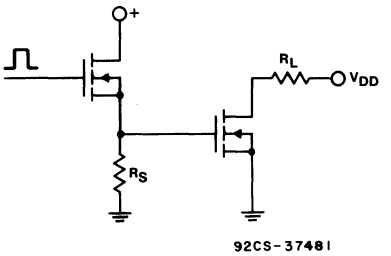


Fig. B-2 - Voltage-follower gate-drive circuit.

Turn-On

R_o is approximately equal to $1/g_m$ for R_s very much greater than $1/g_m$.

g_m = transconductance of driving MOSFET transistor.

Turn Off

$R_o = R_s$

CASE 3: COMMON-SOURCE GATE DRIVE, FIG. B-3

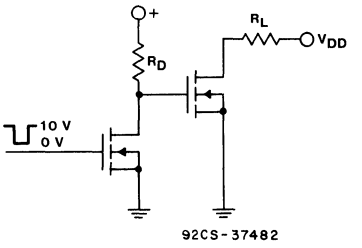


Fig. B-3 - Common-source gate-drive circuit.

Turn-On

$R_o = R_D$ (drain-to-ground capacitance of driving device adds to C_{GS} of driven MOSFET.)

Turn-Off

$R_o = R_{DS}(on)$ of driving MOSFET

R_D is very much greater than $R_{DS}(on)$

The Application of Conductivity-Modulated Field-Effect Transistors

by Jack Wojslawowicz

SUMMARY

The development of conductivity-modulated field-effect transistors, FETs, makes available to the system designer another solid-state device that can be used to implement power switching control. This paper reviews differences between the standard and the newly developed FET. It shows the significant advantages that the conductivity-modulated FET has over the standard FET. Several applications are presented to show that this new type of device works well in practical situations. The relative inmaturity of the conductivity-modulated FET may limit its initial utilization. But as the family grows and product innovation and refinement takes place, this newest member of the power semiconductor family will become a viable alternative to the other members.

GENERAL CONSIDERATIONS

The development of the power field-effect transistor has made available to the power-stage designer an entire new family of power semiconductors. Over the past 5 to 6 years, the breadth of product has grown to encompass the requirements of a large number of applications. A limiting factor that has slowed the utilization of power FETs in the high-current, high-voltage applications is the fact that the on-state resistance ($R_{DS}(on)$) in a standard FET is related to its breakdown voltage (BV_{DSS}) by a nearly cubic power, i.e., $R_{DS}(on) \approx BV_{DSS}$ 2.8. What this implies, as Fig. 1 shows, is that as the breakdown voltage increases, the on-state resistance climbs even faster.

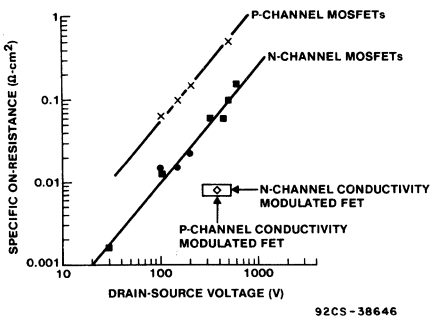


Fig. 1 - Specific on-resistance of p and n-channel MOSFETs and conductivity-modulated FETs versus forward blocking voltage.

The MOSFET on-state resistance is contributed to primarily by three components of the transistor: the MOS channel, the neck region, and the extended drain region. The extended drain region contributes the most to the on-state resistance in high-voltage MOSFETs. To achieve a lower on-state resistance at a given blocking voltage, the usual technique is simply to make the die larger. However, increasing the die size has its limitations from a manufacturing point of view, since MOSFETs, with their very fine horizontal geometries, are highly defect-yield sensitive. As die size increases, the likelihood of a defect resulting in a nonfunctional part increases exponentially. This tendency, combined with a smaller number of parts per wafer, limits the availability of low-on-state-resistance, high-voltage MOSFETs.

A change in the horizontal geometry of the MOSFET can lower the specific on-state resistance per unit area. By using more channel width with smaller source cells placed closer together, a reduction in on-state resistance can be achieved. A limitation on how close these cells can be placed arises from a possible localization of field concentrations that will limit the voltage breakdown of the structure to less than the theoretical rating due only to impurity concentrations. Therefore, for a given breakdown voltage, there exists a minimum spacing of the cell structure. Generally, the higher the required breakdown voltage, the further apart the cells must be placed.

As stated earlier, the extended drain region of the MOSFET generally contributes the most to the on-state resistance in high-voltage MOSFETs. As the required blocking voltage is increased, this region must be made thicker and more lightly doped to be able to support the desired voltage. It is this region's contribution to on-state resistance that the condictivity-modulated field-effect transistor drastically reduces. This reduction occurs as the result of the injection of minority carriers from the substrate and, in specific on-state resistance per unit area, is about 10 times less than in a standard MOSFET at the 400-volt BV_{DSS} level, as shown in Fig. 1.

Further analysis has shown that the specific on-state resistance may be nearly independent of blocking-voltage level. This finding implies that at a BV_{DSS} of 1000 volts, the reduction in conductivity-modulated FETs over the standard MOSFETs could be perhaps 50 to 1. These reductions in on-state resistance per unit area that the conductivity-modulated FETs can achieve present the possibility that high-voltage high-current FET-type devices can become more readily available because of the smaller die sizes associated with conductivity-modulated FETs.

COMPARISON OF STANDARD AND CONDUCTIVITY-MODULATED FETs

Standard and conductivity-modulated FETs share some characteristics, but are substantially different in others. Shown in Table I is a listing of the major characteristics that make the conductivity-modulated FETs unique among power semiconductor families. Foremost, it is a voltage-gated device; its input characteristics are similar to standard power MOSFETs of comparable chip size. Very little drive power is required at low to moderate switching frequencies. The device remains under the control of the gate within its normal operating conditions. It exhibits the normal linear mode as well as the fully saturated on-state of conventional power MOSFETs. When the gate voltage is removed, the device turns off, unlike the thyristor family of power semiconductors, which must be either externally or naturally (internally) commutated.

Table I - Conductivity-Modulated FET Characteristics

Voltage Gated	—	Small gate power required. Similar to standard power MOSFET.
Turn Off	—	When gate drive is removed... Unlike an SCR!
Nonlinear On-State Voltage Drop	—	Like that of an SCR.
Turn On Speed	—	Fast! - Comparable to a standard power MOSFET.
Turn-Off Speed	—	Slow! - Comparable to a bipolar transistor.
Temperature Independent On-State Voltage Drop	—	Unlike the typical 2x variation of a power MOSFET.

The on-state voltage drop or resistance characteristic of a conductivity-modulated FET is markedly different from that of a standard power MOSFET, and is similar to that of a thyristor family member, the SCR. There is an offset voltage component (typically 0.6 volt) due to the p-n junction on the drain side, and a somewhat nonlinear resistive component, both of which are in series between the drain and source terminals. This series arrangement results in a highly nonlinear equivalent resistance, unlike the linear resistive characteristic of $V_{DS}(on)$ of a standard FET.

The structure of the conductivity-modulated FET operates during its turn on just as a standard FET does, hence its turn-on speed is very similiar to that of a standard FET. With its high input impedance and its short propagation delay, the turn-on transistion of the conductivity-modulated FET, as well as the standard power FET, is easily controlled by the gate driving circuit. This characterstic allows the designer the ability to control EMI and RFI generation easily. With other power semiconductors, it may be necessary to employ elaborate circuit schemes to limit rapidly rising in-rush currents.

A significant characteristic that must be considered in power switching applications is that of turn-off speed. The internal action that makes the conductivity-modulated FET such a silicon-efficient device also makes it an inherently slower device during turn-off. The injection of the minority carriers during the on-state conduction of current results in these carriers being present at the moment of turn-off. Without any way of removing these carriers by external means, they must recombine within the structure itself before the device can revert to its fully off-state condition. The quantity of these carriers and how fast they can deplete themselves determines the turn-off switching speed of the conductivity-modulated FET. This process of recombination is considerably slower than the simple discontinuance of majority carrier flow by which the standard power FET turns off. Hence, again, the conductivity-modulated FET is an inherently slower device. Its turn-off speed lies somewhere between the performance of a thyristor and that of a bipolar transistor.

The final characteristic that makes the conductivity-modulated FET different from a conventional FET is the variance of on-state voltage with temperature. The characteristic of the conductivity-modulated FET is similar to that of an SCR, varying about -0.6 mV/°C. The conventional FET has a positive temperature coefficient such that on high-voltage devices the $R_{DS}(on)$ will double from its 25° C value when the junction temperature reaches 150° C. The system designer must take this characteristic into consideration when the heat sink is being designed for the system.

It is these similarities and differences that make the conductivity-modulated FET a unique member of the family of power-semiconductor switching devices. Applications of this alternative power switching device invariably make use of one or more of its unique characteristics.

APPLICATIONS

Automotive Ignition

An application that can take advantage of the low drive-power capability of the conductivity-modulated FET is the electronic automotive ignition system. In Fig. 2, the control IC takes the signal from the pickup coil located in the distributor and regulates the current through the ignition coil. At the proper time, the IC removes base drive from the bipolar transistor, which all systems currently employ as their coil driver. This removal of base drive allows the transistor to shut off which, in turn, causes a rapid decrease in the ignition-coil primary current. As the primary current decreases to zero, the energy stored in the field surrounding the primary is transferred to the secondary coil. The secondary coil, consisting of many more turns than the primary, transforms this energy into a higher voltage, resulting in a spark being generated in the cylinder. The control IC determines when this spark occurs, so as to derive usable power. With the use of a bipolar transistor, it is estimated that approximately two-thirds of the power dissipation that occurs in the control IC is the result of the need to be able to drive the required base current of the ignition output transistor. The high-impedance input of the conductivity-modulated FET virtually eliminates the base-current drive dissipation of the control IC.

With improved silicon usage, the conductivity-modulated FET brings to power semiconductor switching devices the die size necessary to attain the required voltage and current-handling capabilities of the electronic ignition. This smaller-sized die makes possible smaller modules, whether they be hybrid or standard PC-based systems, than those currently implemented with bipolar-transistor technology.

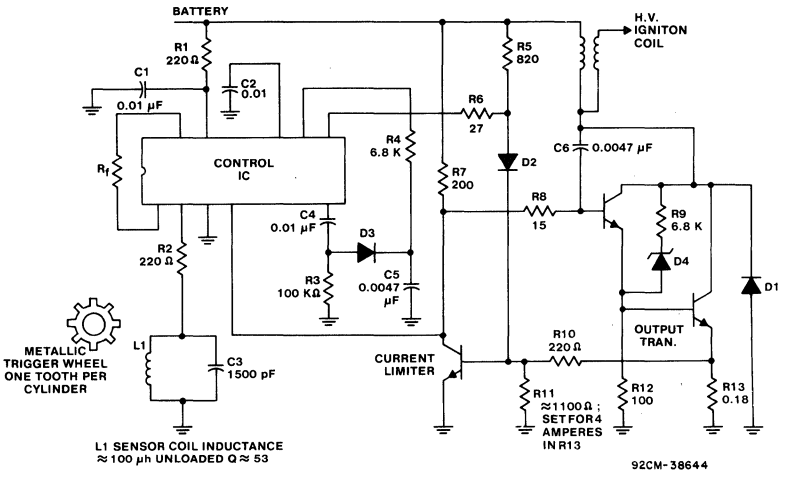


Fig. 2 - Typical ignition system.

Brushless DC Motors

Another emerging application that can make use of conductivity-modulated FETs is the emerging field of brushless dc motors. In this class of application, the solid-state devices are used to electronically switch the voltage to the multiplicity of windings that are employed. The motor consists of an armature that has a number of N and S poles consisting of high-strength permanent magnets. The stator is made up of the multiplicity of windings that were mentioned above; the windings are spaced incrementally about the outside frame of the housing. The voltages to these windings are all electronically switched to create a rotating magnetic field. The armature then rotates to maintain its relative position within the moving magnetic field. The switching of the voltage on the stator windings is done by means of power semiconductor devices. A basic block diagram of such a system is shown in Fig. 3.

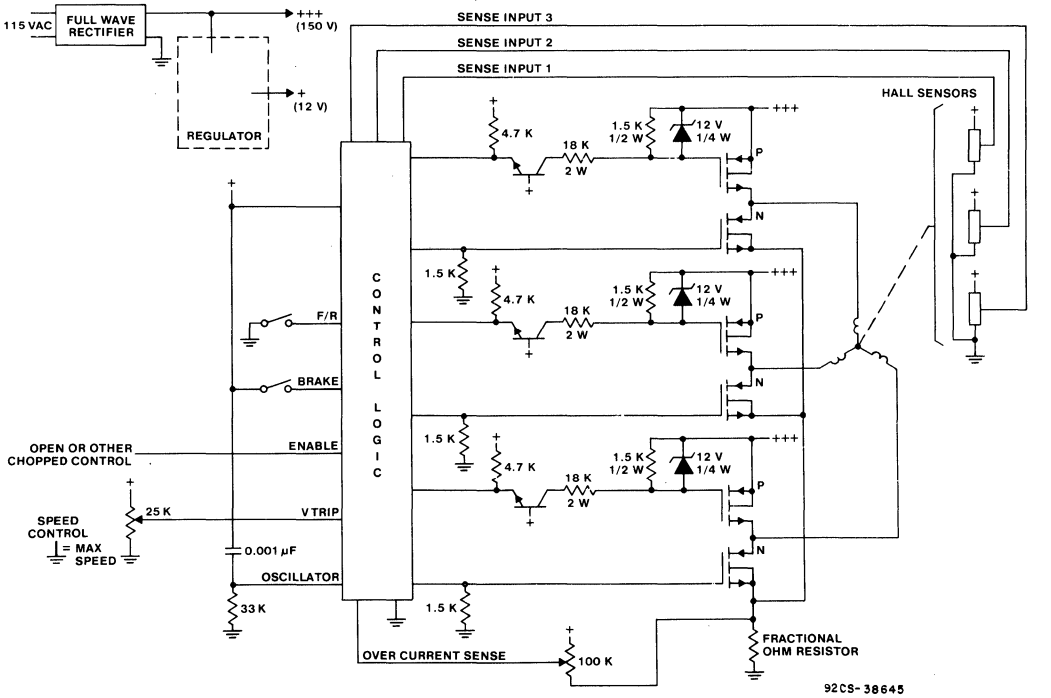


Fig. 3 - Control circuit for three-phase brushless dc motor.

The control logic provides the proper sequence of drive signals based on the rotation direction desired, the speed desired, and the enable input. These requirements are combined with the inputs from the hall-effect sensors to determine which power devices should be activated. Since the current through the stator windings must be bidirectional, the half-bridge or totem-pole output configuration is used to steer the current. This circuit implementation is generally performed with complementary devices, although single-polarity devices can be used with increased circuit complexity.

In a typical 120-volt off-line system, like the one shown in Fig. 3, the switching devices must have a 300 to 400-volt blocking capability. For larger size motors, where larger currents are necessary, the use of power FETs generally implies the use of large die to achieve a low power dissipation to meet the heat-dissipation capability of the packaging. The conductivity-modulated FET, with its temperature-independent on-state-voltage-drop characteristic, helps this situation by keeping the dissipation lower than can be achieved with a standard power FET because of the increasing $R_{DS}(on)$ characteristic of that device. The small die size of the conductivity-modulated FET, the result of better silicon utilization, again makes them the practical choice in motor control not only because of their electrical characteristics, but also because of the lower manufacturing cost of the die.

As stated above, system complexity can be reduced with complementary devices. Although p-channel conductivity-modulated FETs are not yet commerically available, laboratory samples have been fabricated which offers better silicon utilization efficiency than their conventional p-channel counterparts. This statement is based on the fact that p-channel MOSFETs require a 2.5 times larger area than an n-channel device for the same $R_{DS}(on)$.

The easier drive requirements for the n-channel (directly driven from the control IC) and the simplified voltage-translation circuit for driving the p-channel devices, combined with the smaller die size with potentially lower device cost for comparable power handling capability, makes the conductivity-modulated FET a natural for the brushless dc motor application.

Switching Power Supply

One final application that has the potential for conductivity-modulated FET usage is the switching power supply. A half bridge configuration implementation is presented in Fig. 4. The system shown uses a standard PWM control IC to drive the conductivity-modulated FETs through the T2 transformer. The voltage drive characteristic of these devices makes the design of transformer T2 quite simple. The control IC is more lightly loaded because it does not have to supply a continuous base drive, as would be necessary with bipolar transistors.

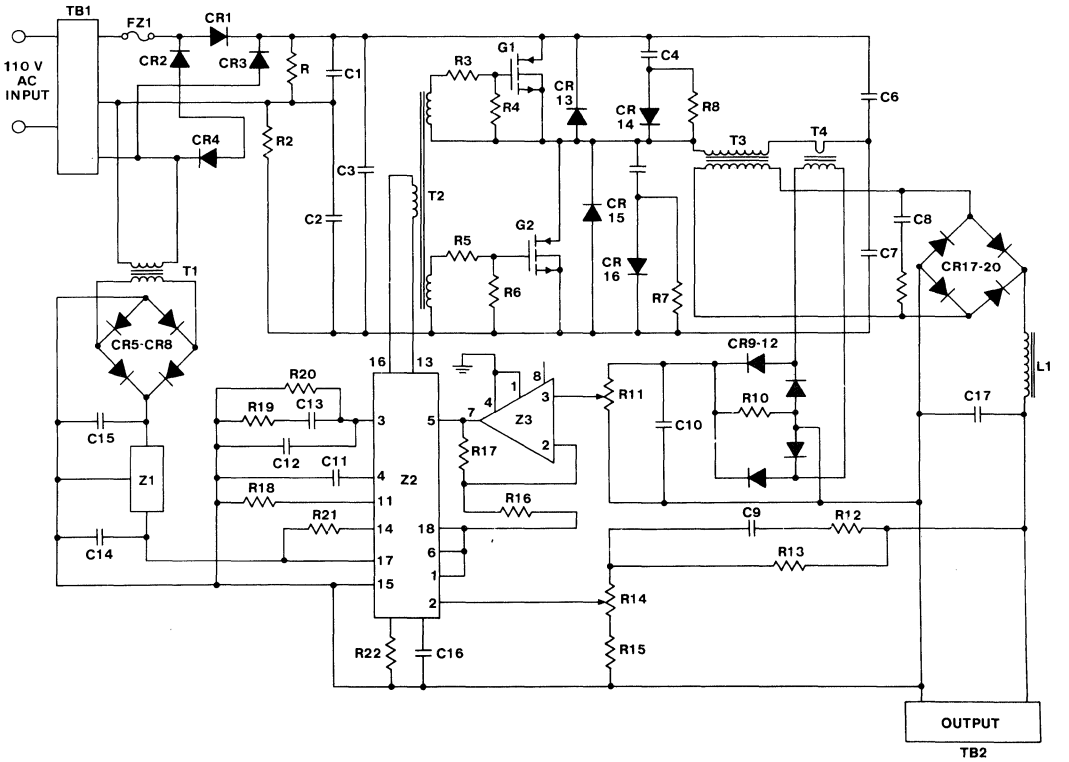


Fig. 4 - Half-bridge switching power supply.

The operating frequency and the "dead time" are the limitations placed on this system when conductivity-modulated FETs are used. The inherent lower switching speeds of these types of devices make these limitations necessary. The system is currently limited to the 20 to 30-kHz range, with dead times as low as 1 to 2 microseconds. This characteristic is comparable to many existing bipolar systems.

Improvements in switching speeds will occur as the conductivity-modulated FET matures. It is, however, unlikely that they will ever have the same switching speeds as standard power FETs. This limitation prohibits their use in some of the newer higher-frequency power supplies being designed now with conventional FETs. However, in higher-power supplies, where conventional FETs must be paralled to achieve a low enough $R_{DS}(on)$ for good efficiency, the conductivity-modulated FET may present a viable alternative with its smaller die size. Although the operating frequency of the system may have to be compromised to use them.

CONCLUSION

The conductivity-modulated FET represents a progression in the ever-advancing state-of-the-art development that occurs in the world of solid-state devices. The unique structure of these devices presents characteristics that make them equivalent in many ways to conventional FETs but superior in other ways. The system designer must take into account these similar and dissimilar characteristics to properly use them. The capabilities of the conductivity-modulated FETs allow them to make inroads into applications currently served by bipolar transistors, and in some cases conventional power FETs. As the devices mature through innovation and product refinement, conductivity-modulated FETs will become vital members of the family of solid-state power-semiconductor devices.

BIBILOGRAPHY

1. J.P. Russell, L.A. Goodman, A.M. Goodman, and J.M. Neilson, **"The COMFET - A New High Conductance MOS-Gated Device,"** IEEE Electron Device Letters EDL-4, 1983, pg. 63-65
2. A.M. Goodman, J.P. Russell, L.A. Goodman, C.J. Nuese, and J.M. Neilson, **"Improved COMFETs with Fast Switching Speeds and High Current Capability,"** Proceeding of the IEEE International Electron Devices Mtg., Dec. 1983, pg. 79-83
3. B.J. Baliga and Marvin Smith, **"Modulated Conductivity Devices Reduce Switching Losses,"** EDN, Sept. 29, 1983,. pg. 153-162
4. M. Smith, W. Sahm, and S. Bahu, **"Insulated Gate Transistors Simplify AC-Motor Speed Control,"** EDN, Feb. 9, 1984, pg. 181-200
5. B.J. Baliga, M.S. Adler, R.P. Love, P.V. Gray, and N.D. Zammer, **"The Insulated Gated Transistor a New Three Terminal MOS-Controlled Bipolar Power Device,"** IEEE Transactions on Electron Devices, Vol. ED-31 No. 6, June 1984, pg. 821-828

The COMFET—A New High Conductance MOS-Gated Device

J. P. Russell, A. M. Goodman
L. A. Goodman and J. M. Neilson

ABSTRACT

A new MOS gate-controlled power switch with a very low on-resistance is described. The fabrication process is similar to that of an n-channel power MOSFET but employs an n^--epitaxial layer grown on a p^+ substrate. In operation, the epitaxial region is conductivity modulated (by excess holes and electrons) thereby eliminating a major component of the on-resistance. For example, on-resistance values have been reduced by a factor of about 10 compared with those of conventional n-channel power MOSFETs of comparable size and voltage capability.

INTRODUCTION

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times, and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability, [1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. In this letter, we describe the fabrication and characteristics of a new vertical power MOSFET structure that provides an on-resistance value about 10 times smaller than that of conventional power MOSFETs of the same size and voltage capability. In this device, the conductivity of the epitaxial drain region of a conventional MOSFET is dramatically increased (modulated) by injected carriers; this mechanism results in a significant reduction in the device on-resistance and leads to the acronym COMFET (COnductivity-Modulated FET).

This device, while similar in structure to the MOS-gated thyristor,[4, 5] is different in a fundamental way; it maintains gate control (doesn't latch) over a wide range of anode current and voltage.[6] The structure and the equivalent circuit for the COMFET are shown in Fig. 1(a) and (b); they are similar to those of an MOS-gated thyristor, except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET except that the n^--epitaxial Si layer is grown on a p^+ substrate instead of an n^+ substrate. The heavily doped p^+ region in the center of each unit cell, combined with the sintered aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance shown in Fig. 1(b). This has the effect of lowering the current gain of the n-p-n transistor (α_{n-p-n}) so that $\alpha_{n-p-n} + \alpha_{p-n-p} < 1$. Thus latching is prevented and gate control is maintained within a large operating range of anode voltage and current.[6]

In the remainder of this note we describe the operation and characteristics of this device.

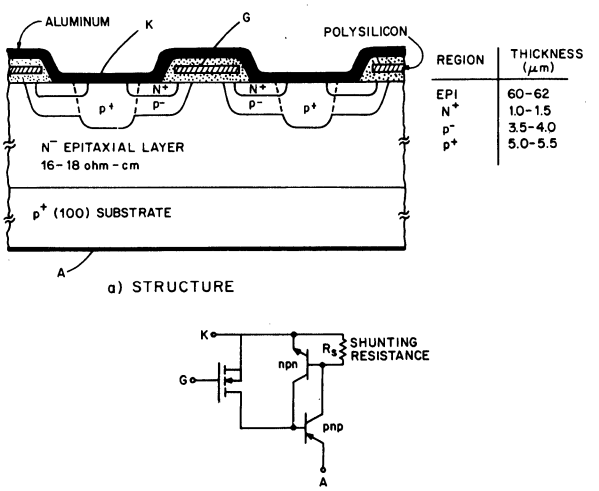


Fig. 1 - (a) Schematic diagram of COMFET structure; (b) Equivalent circuit.

DEVICE OPERATION

The COMFET is a four-layer (n-p-n-p) device with an MOS-gated channel connecting the two n-type regions. In the normal mode of operation, a positive voltage is applied to the anode (A) relative to the cathode (K). When the gate (G) is at zero potential with respect to K, no anode current (i_A) flows for anode voltage v_A below the breakdown level V_{BF}. When $v_A < V_{BF}$ and the gate voltage is larger than the threshold value V_{gt}, electrons pass into the n^--region (base of the p-n-p transistor). These electrons lower the potential of the n^--region, forward biasing the $p^+ - n^-$ (substrate-epi-layer) junction, thereby causing holes to be injected from the p^+ substrate into the n^- epi-layer region. The excess electrons and holes modulate the conductivity of the high-resistivity n^- region, which dramatically reduces the on-resistance of the device. During normal operation, the shunting resistor (R_S) keeps the emitter current of the n-p-n transistor very low, which keeps α_{n-p-n} very low. However, for sufficiently large i_A, significant emitter injection may occur in the n-p-n transistor, causing α_{n-p-n} to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering i_A below some "holding" value, as is typical of a thyristor.

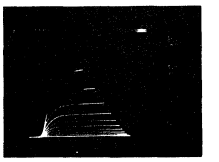
DEVICE CHARACTERIZATION

Two different lots of COMFET structures, consisting of about 10 wafers/lot, have been successfully prepared to date. From these wafers, 1.5 and 3-mm square devices were fabricated using a standard HEXFET geometry[7] with a polysilicon gate electrode over an SiO_2 gate dielectric. Several hundred COMFETs were mounted in standard TO-3 and TO-66 packages and characterized under dc and pulsed conditions, as described below.

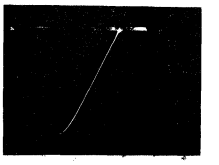
With zero gate bias, the forward characteristic of a COMFET shows very low current (< 1 nA) up to about 390 V, where it breaks up sharply to much larger current levels with only a slight increase in voltage. If the internal junction between the p^+ substrate and the n^- epitaxial layer had been edge-passivated, a similar reverse breakdown characteristic would be expected. The actual reverse breakdown voltage for our devices was about 100 V because edge passivation was not used.

Fig. 2(a) shows the MOSFET-like transfer characteristics of a COMFET in the low gate-voltage region. A noteworthy feature of the COMFET characteristic is the ~ 0.7 V offset, from the origin, of the steeply rising portion of the i(v) characteristics. This offset is the voltage required to forward bias the $p^+ - n^-$ (substrate-epi-layer) junction, and is an integral characteristic of the present device.

Fig. 2(b) shows the i(v) characteristic of a COMFET with v_g = 20 V, and demonstrates the low on-resistance of the device (~ 0.084 Ω at 20 A). The on-resistance values of nearly all of the many COMFETs fabricated to date have been less than 0.1 Ω (at 20 A) for the 3-mm square devices. Such values compare very favorably with those of conventional power MOS structures, as illustrated in Fig. 3. Here, the open data points (and the upper curve) are from data sheet specifications of commercial power MOSFETs (RCA, IRC, and Motorola). The solid data points (and the lower curve) are those of Baliga, which he labelled "state-of-the-art",[3] supplemented with some of the "best" of RCA's commercial



a) MOSFET - Like Characteristic



b) COMFET i(v) with v_g = 20 V

Fig. 2 - (a) MOSFET-like characteristic; (b) COMFET i(v) with v_g = 20 V.

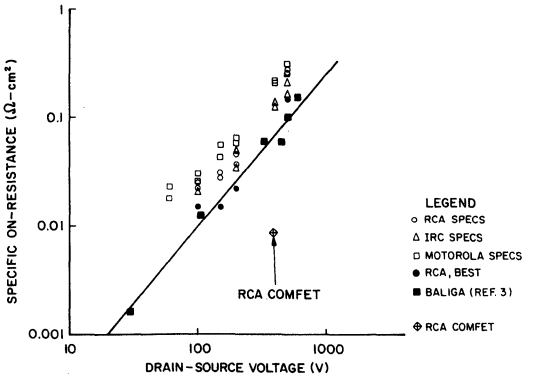


Fig. 3 - Specific on-resistance versus drain-source voltage capability for state-of-the-art power MOSFETs and the COMFET.

and developmental MOSFETs. Note that the on-resistance of the COMFETs is approximately 10 times less than that of a 400-V state-of-the-art MOSFET. Moreover, similarly low on-resistance values should be obtainable from COMFETs designed for higher drain-source voltages. This is due to the fact that the resistance of the modulated region is determined by the concentrations and mobilities of the excess carriers (as in a p-i-n diode)[8] rather than by the background doping of the layer. In particular, the epi-layer doping and thickness of our present COMFET structures were designed for 600 V, but V_{BF} was limited to 400 V by the edge design of the device. An improved edge design should provide a blocking capability closer to bulk breakdown, without altering the on-resistance of the device. This would make the COMFET on-resistance of less than 0.1 Ω even more attractive for high-voltage applications.

TRANSIENT RESPONSE MEASUREMENT

Switching time measurements under pulsed gate-voltage operation were used to characterize the transient operation of the device. The response of the anode current to a square-wave gate-voltage pulse is comprised of a rapid turn-on (with a typical time less than 1 μs) and a somewhat slower turn-off. We observed that the turn-off transient consists of an initial "fast" component, followed by a "slow" tail, as shown in Fig. 4.

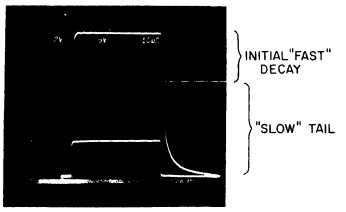


Fig. 4 - Gate voltage (lower trace) and anode current (upper trace) waveforms for $i_A(max) = 8$ A.

We believe that the initial rapid decay is due to the turn-off of the MOS portion of the equivalent circuit, and the turn-off tail is due to the time required for the excess carriers in the epitaxial drain region to decay. In general, turn-off times in the range of 5 to 20 μs were observed, with the precise value depending on circuit conditions and the turn-off time of the gate pulse.

The n-p-n-p structure of the COMFET is similar to that of a thyristor and can be forced to latch under sufficiently high drive conditions. We have observed latching currents in the range 10-30 A in 3-mm square chips. The magnitude of the latching current has been found to depend on both anode voltage and temperature, decreasing with increasing anode voltage or increasing temperature.

More interestingly, the latching current is also strongly influenced by the gate voltage turn-off time. Slow gate turn-off ($\sim$ 10 μs) permits anode currents up to 30 A without latching. However, rapid gate turn-off ($\lesssim$ 1 μs) leads to latching at a much lower anode current level ($\sim$ 10 A) in the same device. We believe that latching during rapid turn-off of the gate voltage is due to current being forced through the n-p-n transistor causing α_{n-p-n} to increase, and leading to the condition for latching, $\alpha_{n-p-n} + \alpha_{p-n-p} = 1$. Slow turn-off of the gate voltage prevents this, since the induced channel turns off slowly and partially shunts the n-p-n transistor; the small current through this transistor keeps α_{n-p-n} sufficiently low to avoid latching.

SUMMARY

A new MOS-gate-controlled power device, the COMFET, has been described. The device has the desirable feature of a very low on-resistance similar to that of a thyristor, but is capable of maintaining gate control of the anode current over a wide range of operating conditions. The low on-resistance is due to conductivity modulation of the n^- epitaxial layer equivalent to the extended drain in a power MOSFET; this carries with it the penalty of slow switching compared with that of a conventional power MOSFET.

ACKNOWLEDGMENT

The authors gratefully acknowledge the various helpful contributions of C. Nuese, D. Bergman, R. Ford, R. Jarl, G. Looney, P. Robinson, W. Romito, L. Skurkey, R. Stolzenberger, C. Wheatley, J. Wojslawowicz, and the staff of the Integrated Circuit Technology Center at RCA Laboratories.

Added Note: Following submission of this Note, a similar device was described by B. J. Baliga in a presentation on December 14, 1982 at the International Electron Devices Meeting in San Francisco, CA. (B. J. Baliga et al., "The Insulated Gate Rectifier (IGR): A New Power-Switching Device", in IEDM Tech. Dig. 1982, pp 264-267.

REFERENCES

1. M. L. Tarng, "On-Resistance Characterization of VDMOS Power Transistors", in IEDM Tech. Dig., 1981, pp 429-433.
2. C. Hu, "Optimum Doping Profile for Minimum Ohmic Resistance and High Breakdown Voltage", IEEE Trans. Electron Devices, Vol. ED-26, p 243, 1979.
3. B. J. Baliga, "Switching Lots of Watts at High Speeds", IEEE Spectrum, Vol. 18, p 42, Dec. 1981.
4. J. Tihanyi, "Functional Integration of Power MOS and Bipolar Devices", in IEDM Tech. Dig., 1980, p 75-78.
5. L. Leipold et al., "A FET Controlled Thyristor in SIPMOS technology", in IEDM Tech. Dig., 1980, pp 79-82.
6. H. W. Becke and C. F. Wheatley, "Power MOSFET With An Anode Region", U. S. Patent 4,364,073, issued Dec. 14, 1982.
7. H. W. Collins and B. Pelly, "HEXFET, A New Power Technology Cuts On-Resistance, Boosts Ratings", Electron. Des., Vol. 12, p 36, 1979.
8. S. M. Sze, **Physics of Semiconductor Devices**. 2nd Edition, New York; Wiley, 1981, p 120.

Improved COMFETs with Fast Switching Speed and High-Current Capability

A. M. Goodman, J. P. Russell, L. A. Goodman
C. J. Nuese, and J. M. Neilson*

ABSTRACT

Conventional vertical power MOSFETs are limited at high voltages (>500 V) by the appreciable resistance of their epitaxial drain region. In a new MOS-gate controlled device called a COMFET (or an IGR), this limitation is overcome by modulating the conductivity of the resistive drain region, thereby reducing the on-resistance of the device by a factor of at least 10. However, the device previously described is slow in turn-off, having a fall time in the range 8 to 40 μs.

The purpose of our present work has been to reduce the fall time significantly and to increase the latching current level of the COMFET, while retaining its desirable features. By modification of the epitaxial structure and addition of recombination centers, we have achieved fall times as low as 0.1 μs and latching currents as high as 50 A, while retaining on-resistance values < 0.2 ohm for a 0.09 cm^2 chip area. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping. For a series of COMFETs (with forward-blocking voltage capabilities of 400-600 V), the fall time can be reduced by more than one order of magnitude with a penalty of less than a 20% increase in on-resistance.

INTRODUCTION

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. This limitation has been effectively overcome by the development of a new MOS power device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate.[4-6] We have called this device a COMFET—an acronym for COnductivity Modulated Field Effect Transistor;[4] the device has also been called an IGR or insulated gate rectifier.[5]

The devices, as originally described, had most of the advantages of conventional power MOSFETs; in addition, they exhibited more than an order-of-magnitude reduction in high current on-resistance values, permitting improved utilization of silicon chip area. However, they also had two disadvantages:

1. When a COMFET (or IGR) is turned off, the injected minority carriers that remain in the epitaxial drain region decay by recombination with majority carriers at a rate determined by the minority-carrier lifetime, τ. Large values of τ resulted in anode-current fall time, t_f, in the range 8-40 μs.[4, 5]
2. The maximum operating current is limited by latchup of the parasitic thyristor that is inherent in the device structure. Typical latching current levels of $I_L \lesssim 10$ A were observed in 0.09 cm^2 area devices when the gate voltage was turned off rapidly (< 1 μs); for slower gate voltage turnoff (~ 10 μs), I_L values as high as ~ 30 A were observed.

The purpose of the present work has been to reduce t_f and to increase I_L while retaining the desirable features of the device. By modifying the epitaxial structure and adding recombination centers to the epitaxial drain region, we have achieved t_f values as low as 100 ns and I_L values as high as 50 A with rapid gate voltage turnoff.

MODIFIED STRUCTURE

A schematic diagram of the original COMFET structure[4] is shown in Fig. 1(a), and the equivalent circuit is shown in Fig. 1(b); they are similar to those of an MOS-gated thyristor

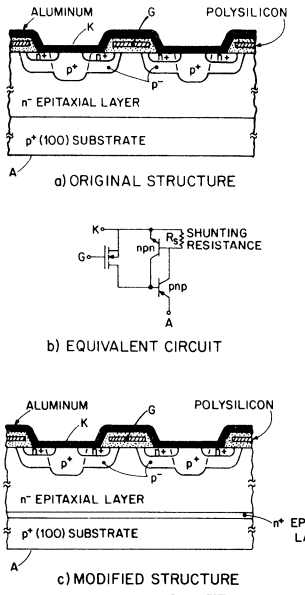


Fig. 1 - (a) Schematic diagram of original COMFET structure. (b) Equivalent circuit. (c) Schematic diagram of modified structure.

except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET, except that the n^--epitaxial layer is grown on a p^+ substrate instead of an n^+ substrate. The heavily doped p^+ region in the center of each unit cell, combined with the aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance R_S. This has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit so that $\alpha_{npn} + \alpha_{pnp} < 1$, thereby preventing latching over a large operating range of anode voltage v_A and anode current i_A. However, for sufficiently large i_A, emitter injection in the n-p-n transistor will increase, accompanied by an increase in α_{npn}. When $\alpha_{npn} + \alpha_{pnp}$ increases to 1, the four-layer device will latch; the level of i_A at which this occurs is the latching current level, I_L. Thus, it can be seen that a structure modification that lowers α_{pnp} will allow a greater range of i_A (and α_{npn}) without latching; that is, a reduction in α_{pnp} corresponds to an increase in I_L.

The modified structure shown in Fig. 1(c) differs from that in Fig. 1(a) by the addition of a thin (~ 10 μm) layer of n^+ silicon in the epitaxial structure between the n^- region and the p^+ substrate. This n^+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in I_L by a factor of 2 to 3. In addition, there is also a reduction in t_f.

These results are illustrated in Fig. 2, in which t_f is plotted versus i_A for each device structure. It should be noted that COMFETs with the modified structure can block high voltage only in the forward voltage direction since the emitter junction ($p^+ - n^+$) of the p-n-p transistor breaks down at a low level when the polarity of the applied voltage is reversed.

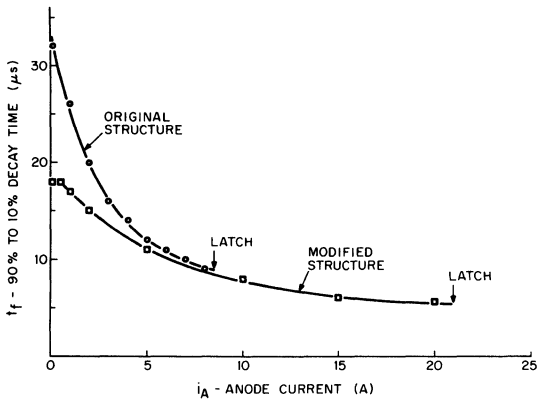


Fig. 2 - Anode-current fall time t_f versus anode current for original structure and modified structure.

ADDITION OF RECOMBINATION CENTERS

We have used a variety of techniques to add recombination centers to COMFETs; these include high-energy electron, gamma-ray, and fast-neutron irradiation, as well as heavy metal doping. The irradiations were carried out after completion of all of the high-temperature processing steps, but in each case an additional heat treatment was necessary to stabilize the devices by annealing out gate-oxide charge, as well as those radiation-induced defects in the silicon (recombination centers) that would otherwise anneal out slowly at the device operating temperature.[7] Typical values of t_f of the order of 1 μs or less were achievable using any of the techniques.

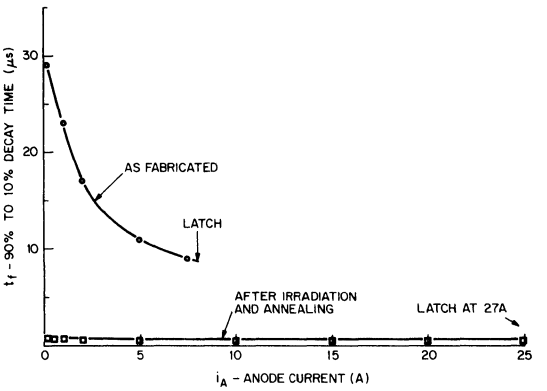


Fig. 3 - Anode-current fall time t_f versus anode current for an as-fabricated device and after 14 MeV neutron irradiation (10^{13}n/cm^2) followed by annealing at 300° C.

An example of the variation of t_f with i_A (1) as fabricated and (2) after irradiation with 14 MeV neutrons and annealing is shown in Fig. 3. Here, the neutron fluence was ~ 10^{13} n/cm^2; this was followed by annealing at 300° C. Note that t_f has not only been drastically reduced, but is virtually constant at ~ 0.6 μs; i.e., almost independent of i_A.

It is possible to lower t_f still further by appropriate irradiation and annealing or by heavy metal doping procedures, although this is not necessarily desirable for reasons that are discussed below. The smallest values of t_f that we have obtained for fully stabilized COMFETs are in the range 100 to 200 ns. This is illustrated in Fig. 4.

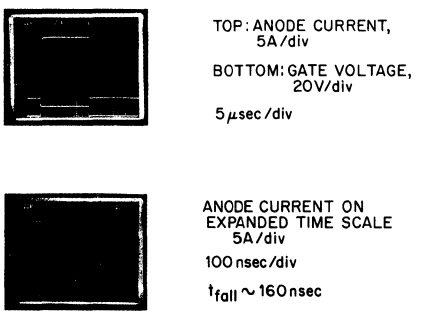


Fig. 4 - COMFET anode current and gate voltage waveforms.

The reduction in minority-carrier lifetime that allows faster switching also carries with it a penalty—higher forward voltage drop when the device is turned on; i.e., higher on-resistance. Since, in the forward conduction of a COMFET, current and voltage are not linearly related, it is necessary to specify a current level at which to compare on-resistance values of different devices. In Fig. 5 we plot the on-resistance (at i_A=20 A) of a series of devices with 0.09 cm^2 chip area against their t_f values after irradiation and annealing. All t_f values shown were obtained at i_A=5 A; for the devices with short switching times, t_f is virtually independent of i_A. Clearly, there is a tradeoff involved, and the optimum choice of a value for t_f and the corresponding

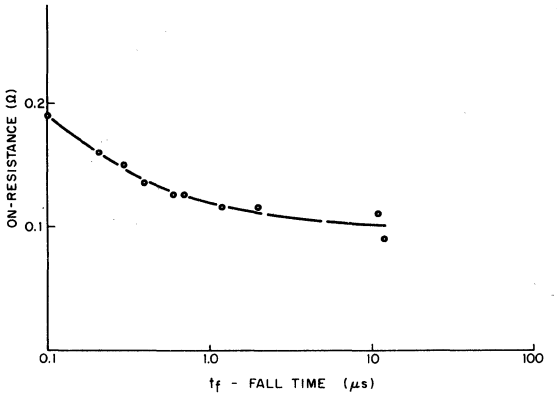


Fig. 5 - On-resistance versus anode-current fall time t_f for a series of COMFETs after various irradiation and annealing treatments.

on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100 ns), the on-resistance value of 0.2 ohm is approximately an order-of-magnitude less than that of comparably-sized n-channel MOSFETs.

TEMPERATURE DEPENDENCE OF t_f AND I_L

All of the device performance data presented thus far have been measured at room temperature. However, power devices are often operated at elevated temperatures, and it is important to determine how their performance varies with temperature. In Fig. 6 the variation of t_f and I_L for a device that has been irradiated and annealed is plotted versus temperature in the range 25 to 150°C. This behavior is typical of all of the devices we have tested; i.e., t_f increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval 25°C to 150°C.

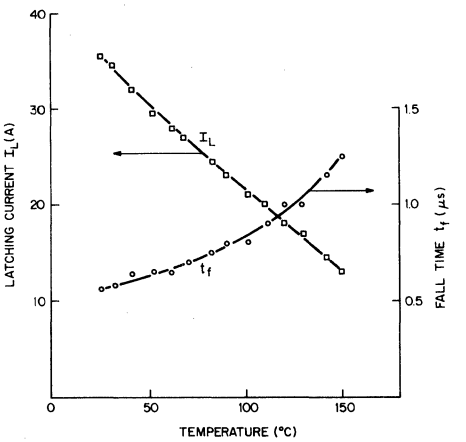


Fig. 6 - Variation of anode-current fall time t_f and latching current I_L with temperature.

SUMMARY

By modification of the epitaxial structure of the COMFET and the addition of recombination centers, we have achieved anode-current fall times as low as 100 ns in COMFETs with latching currents as high as 50 A for a 0.09 cm^2 chip area. We have described the tradeoff between on-resistance and anode-current fall time that may be obtained, and have demonstrated the variation of anode-current fall time and latching current with operating temperature.

ACKNOWLEDGMENT

The authors are indebted to D. Bergman, R. Ford, F. DiGeronimo, G. Looney, P. Robinson, W. Romito, L. Skurkey, M. Snowden, R. Stolzenberger, and the staff of the Integrated Circuit Technology Center at RCA Laboratories for their various contributions to the fabrication and characterization of the COMFETs. A special thank you goes to F. Taft, Z. Streletz, and H. Hendel who carried out the device irradiations.

REFERENCES

1. M. L. Tarng, "On-Resistance Characterization of VDMOS Power Transistors", IEDM Tech. Dig., 1981, pp 429-433.
2. C. Hu, "Optimum Doping Profile for Minimum Ohmic Resistance and High Breakdown Voltage", IEEE Trans. Electron Devices **ED-26**, p 243, (1979).
3. B. Jayant Baliga, "Switching Lots of Watts at High Speeds", IEEE Spectrum **18**, p 42 (Dec. 1981).
4. J. P. Russell, A. M. Goodman, L. A. Goodman and J. M. Neilson, "The COMFET—A New High Conductance MOS-Gated Device", IEEE Electron Device Letters **EDL-4**, pp 63-65 (1983).
5. B. J. Baliga, M. S. Adler, P. V. Gray, R. P. Love and N. Zommer, "The Insulated Gate Rectifier (IGR): A New Power Switching Device", IEDM Tech. Dig., 1982, pp 264-267.
6. H. W. Becke and C. F. Wheatley, "Power MOSFET With An Anode Region", U. S. Patent 4,364,073, issued Dec. 1982.
7. S. K. Ghandi, **Semiconductor Power Devices** (John Wiley, New York, 1977) p 296.

Operating Considerations for RCA Solid-State Devices

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid-state devices.

The ratings included in RCA Solid-State Devices data bulletins are based on the Absolute-Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

> Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid-state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the device package. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid-state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Similarly, the TO-5-style package often used for integrated circuits usually has the substrate or most negative supply voltage connected to the case. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device and result in destruction and/or possible shattering of the enclosure.

TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, for the electrical connection, but more importantly for conduction of the heat generated, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Soldering is the preferred method for mounting. The package may be soldered to the heat sink by use of lead-tin solder, however a solder with a lower melting point than the 95/5 lead/tin solder used for assembly should be used. The soldering process should be carefully controlled to prevent permanent damage to the device. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCRs and triacs) in molded-epoxy-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

Lead-Forming Techniques

The leads of the RCA VERSAWATT and VERSATAB in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping.

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. When the use of a properly designed fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least ⅛ inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT and TO-202 VERSATAB in-line packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 235° C. The soldering instrument must be at least 1/8 inch from the device and must not be applied for more than 10 seconds. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

Mounting

TO-220. Recommended mounting arrangements and suggested hardware for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4124. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided. Damage to the device can also result from the use of a non-flat mounting surface. This surface should be flat within 0.002 inch from the mounting hole to either side of the TO-220 device.

Modification of the flange can also result in flange distortion and should not be attempted. The package may be soldered to the heat sink by use of lead-tin solder, however this solder should have a lower melting point than the 95/5 lead/tin solder used for assembly. The soldering process should be carefully controlled to prevent permanent damage to the device.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PTD-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.

2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

TO-3. The high power-handling capability of the TO-3 package requires the use of very large silicon die. Large die are susceptible to damage when the TO-3 package is fastened to a non-flat surface, or when unequal torque is applied during mounting.

When mounting a TO-3 device, the following precautions must be observed to avoid internal damage to the device:
1. The mounting surface should be flat within 0.007 inch.
2. **Both** mounting screws should be tightened lightly to 2 inch-pounds **first**, and then to no more than 12 inch-pounds.
3. The use of impact wrenches is not recommended.
4. Care should be exercised with thermal greases to avoid an increase in viscosity and the formation of lumps as a result of excessive exposure to air prior to application. These conditions will place additional stress on the device during mounting.

Thermal Considerations

The maximum allowable power dissipation in a solid-state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid-state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid-state power devices, the following special precautions should be observed:
1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
   Note: Silicone-oil fluids that come into direct physical contact with silicone-molded transistors may react chemically with and cause damage to the packages. These silicone oils are commonly formulated into thermal-grease heat-transfer compounds. Selection of these greases is therefore critical and based on the bleed rate of the oil from the grease. For example, in mounting arrangements that employ an insulating washer, a thermal-grease heat-sink compound, such as Dow Corning No. 340 or equivalent, for which the bleed rate does not exceed 0.5 per cent after 24 hours of 200° C is recommended for use on both sides of the insulating washer.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers ranges from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

Cleaning After Mounting

A wide variety of chemicals and solvents is available for fluxing, degreasing, and flux removal. Care must be exercised in the selection of materials, such that from a reliability standpoint, there is no adverse effect on component life. A major contributor, effecting device reliability, is the chemical reaction of chloride with the aluminum metallization of the die. Eventually this etching process will result in electrical open circuits. The mechanism is defined as Electrolytic Metal Attack (EMA) and is accelerated in a moisture environment. Cleaning and fluxing compounds free of chloride will therefore maximize device life. Chloride is defined as the dissociated ion, which is soluble in water, as contrasted to the water insoluble organic chlorine of compounds such as perchloroethylene and trichloroethane. It is, of course, impractical to evaluate the long-term effect on semiconductor life of all chemicals which are marketed under a variety of brand names.

The choice of fluxes for electronic applications should be restricted to rosin types, R, RMA and RA and water soluble organic acid, OA, formulations. Inorganic acid fluxes should not be used as they can attack the internal metallization of the semiconductor. As stated above, it is further recommended, where applicable, that non-halide type fluxes be used for improved device reliability. Some examples of acceptable fluxes are:

A. Rosin Types (RA)
   Alpha 711
   Alpha 809 foam flux
   Alpha 811 foam flux
   Alpha 815 foam flux
   Alpha TL33M halide free
B. Water soluble organic acid (OA) types, halide free
   Blackstone 1452
   Kenco 183
   Alpha 260HF and 265HF

Since circuit boards can fall into several categories, such as single sided, double sided with plated-through holes and densely populated multilayer types, it must be stressed that the manufacturer's recommendation be considered when choosing the proper flux for the process being used.

Flux cleaning and/or degreasing is necessary to assure that the final soldered assembly is free of contaminating soils. The choice of the cleaning system is relative to the soil being removed. Water-based cleaners are generally used to remove polar soils, such as rosin activators, organic acid residues, and finger salts. Solvent cleaners are chosen for removal of organic (non-polar) contaminants, which include rosins, oils, and greases. Cleaning methods can incorporate immersion (with or without ultrasonics), brushing, and spraying. The choice of cleaner should be based on affinity for the contaminant, ability to thoroughly wet the parts, and compatibility with components. It should also be safe to use. use.

Solvent cleaners are generally divided into two classes: chlorinated and fluorinated. These can be used for cleaning rosin-activated (RA) fluxes. The chlorinated solvents are more aggressive and care must be taken to assure there is

no damage to components or substrate. This type solvent should not be used with silicone-encapsulated transistors as the solvent will tend to dissolve the plastic. The use of chlorinated solvents must be closely monitored because of a breakdown to form acid components in the presence of moisture. The solvent should be checked regularly and discarded when acid levels exceed manufacturer's guidelines. Fluorinated solvents are normally blends of trifluorotrichloroethane with other solvents, such as: methanol, ethanol, isopropanol, acetone, methylene chloride, or chloroform. These solvents can be purchased under trade names as Freon TE, TE35, TP35, Frigen 113 TR-M, Haltron 113 MOM, and Flugene 113 MA. Fluorinated systems are milder acting and are used in vapor degreasing systems at the boiling point of the solvent mixture.

The solvents may be used for a maximum of 4 hours at 25° C or for a maximum of 1 hour at 50° C.

Rosin fluxes can be removed by either solvent or aqueous cleaners. The water systems contain an additive that reacts with the rosin acids to convert the acids to a water-soluble biodegradable soap. Water-soluble organic-acid fluxes may require the use of a neutralizer to accelerate the solubility of the acid residues and neutralize any residues that may remain. Alcohols are acceptable solvents for rosin-based flux removal; but because of flammability concerns, the fluorinated alcohol blends are preferred. Examples of suitable alcohols are methanol, isopropanol, and special denatured ethyl alcohols, such as SDA1, SDA30, SDA34, and SDA44.

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and physical standpoint.

RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the TO-205AF package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an epoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN-3822, "Thermal Considerations in Mounting of RCA Thyristors".

MOS FIELD-EFFECT TRANSISTORS

Small-Signal and Power MOSFETs

Insulated-Gate Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in a MOSFET if a type with an unprotected gate is picked up and the static charge on the handler's body allowed to discharge through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOSFETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOSFETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB• LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

Power MOSFETs

In addition to the above basic precautions, the following precautions should be taken for safe handling of Power MOSFETs:

1. Gate Voltage Rating — Never exceed the gate-voltage rating of ±20 V.* Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.
2. Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.
3. Gate Protection — These devices do not have an internal monolithic zener diodes connected from gate to source. If gate protection is required an external zener is recommended.

INTEGRATED CIRCUITS

Mounting

Integrated circuits are normally supplied with tin-lead dipped leads to facilitate soldering into circuit boards.

When integrated circuits are welded onto printed-circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. When solder-dipped leads are formed, they must be reflowed or redipped within 40 mils of the package body. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

• Trade Name: Emerson and Cumming, Inc.
*±10 V for logic-level MOSFETs.

CMOS INTEGRATED CIRCUITS

Handling

All CMOS gate inputs have a diode or resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect CMOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. It is recommended that ionizers be used in the handling and assembly areas to minimize damage from electrostatic discharge (ESD). See ICAN-6525, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

Operating

Unused Inputs

All unused input leads must be connected to either the low rail (V_{SS}, V_{EE}, or GND) or the high rail (V_{CC} or V_{DD}), whichever is appropriate for the logic circuit involved. A floating input on a high-current type such as the CD4049 or CD4050, operating at a supply voltage above 5 V, not only can result in faulty logic operation, but can cause the maximum-rated power dissipation to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to the high or low voltage supply rails. A useful range of values for such resistors is from 10 kilohms to 1 megohm. Pins that are I/O must have a terminating resistor.

Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady-state value of less than the absolute-maximum rating. This value is either 10 mA or 20 mA depending on device family. Input currents of less than the maximum rating prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

Output Short Circuits

Shorting of outputs to the high or low supply rail can damage many of the higher-output-current CMOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For the QMOS HC/HCT/HCU types, outputs may be shorted to V_{CC} (5 V ± 10%) for 1 second maximum and only one output at a time. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below the device maximum-rated output power.

For detailed CMOS IC operating and handling considerations, refer to Application Note ICAN-6525 "Handling and Operating Considerations for MOS Integrated Circuits".

CMOS Power-Supply Distribution and Decoupling

Power distribution should be a prime consideration in all CMOS designs. Although DC power dissipation is very low, dynamic power (due to switching transients) can be high. High-voltage and/or low-temperature operation increase dynamic current transients.

A low-impedance power source and supply-to-ground capacitance bypass placed near each device will significantly reduce noise generation on signal and power lines; system reliability is greatly changed.

Decoupling

Higher speeds, faster edges and higher output-drive currents cause higher-frequency current transients to be imposed on ground and V_{CC} rails of an IC. For LSI, HC, and HCT families, consideration of power-supply distribution and decoupling become important. Before decoupling can be utilized for noise reduction, there must first be a good power-supply distribution network. A good ground connection system and capacitive decoupling must be employed. For details refer to Application Note ICAN-7329, "Power-Supply Distribution and Decoupling for QMOS High-Speed-Logic ICs".

LINEAR INTEGRATED CIRCUITS

BIMOS, BIPOLAR AND CMOS

In linear integrated circuits that employ diode-isolation techniques, there are numerous parasitic devices associated with the primary circuit components. These devices may be activated or turned on by driving inputs and/or outputs beyond the supply-voltage range of the integrated circuit. For example, externally driving the collector terminal of a transistor array below the isolation or substrate potential will forward bias the parasitic isolation diode shown in Fig. 1. Since the collector region and substrate form a comparatively large-area diode, high currents will be sustained, often at levels sufficiently high to melt the metallization to these devices.

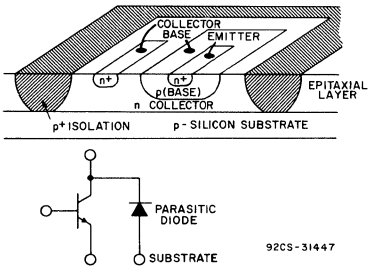


Fig. 1 - Sectional view of conventional "vertical" n-p-n transistor commonly used on IC chip. Also shown is the equivalent circuit and associated parasitic diode.

Operational amplifiers like the 741, and other similar structures, can be damaged by driving a positive-going signal into the input device with power off. The signal will forward bias the collector-to-base junction of the input transistor and, if the positive supply impedance is low enough, drive current back into the supply. Current above the maximum rating may result in damage to the amplifier.

Supply transients are another possible source of damage. They can activate or trigger parasitic SCR devices which can cause an integrated circuit to draw extremely high current. If the supply impedance is sufficiently high, the SCR gate drive in the latched condition is removed by the limiting action of the supply. If the supply impedance is too low, the device will continue to demand high currents until the metallization of either the device or the printed-circuit board fuses open.

1CE-402

Although device manufacturers take precautions to keep the number of these parasitic devices at a minimum, normal device process variations occasionally make the formation of parasitic devices inevitable. It is essential, therefore, that the user take precautions to insure that an integrated circuit is never operated beyond its maximum ratings, even under momentary transient conditions.

SOLID-STATE CHIPS

Solid-state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special-handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40° C
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. MOS chips that are ESD-sensitive should be handled in an environment where ionizers are employed.
4. During mounting and lead bonding of chips, the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
5. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmospheres which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

Sales Offices, Authorized Distributors, and Manufacturers' Representatives

Sales Offices

UNITED STATES

Alabama
RCA
Park Plaza
303 Williams Avenue
Suite 133
Huntsville, AL 35801-6001
Tel: (205) 533-5200
TACNET: 8-721-1110

Arizona
RCA
6900 E. Camelback Road
Suite 460
Scottsdale, AZ 85251-2441
Tel: (602) 947-7235

California
RCA
3150 De La Cruz Blvd.
Bldg. D, Suite 206
Santa Clara, CA95054-2486
Tel: (408) 748-0933
TACNET: 8-528-1605

RCA
Suite 420
4827 No. Sepulveda Blvd.
Sherman Oaks, CA 91403-1993
Tel: (818) 783-3955
TACNET: 8-522-4200

RCA
17731 Irvine Blvd., Suite 104
Magnolia Plaza Bldg.
Tustin, CA 92680-3235
Tel: (714) 832-5302
TACNET: 8-542-1120

Colorado
RCA Corp.
6767 So. Spruce Street
Englewood, CO 80112-1284
Tel: (303) 740-8441

Florida
RCA
P.O. Box 12247
Lake Park, FL 33403-0247
Tel: (305) 626-6350
TACNET: 8-722-1291

Georgia
RCA
Suite 304
2872 Woodcock Blvd.
Atlanta, GA 30341-4002
Tel: (404) 452-2355
TACNET: 8-727-2344

Illinois
RCA
One Pierce Place
Suite 325, West Tower
Itasca, IL 60143-2681
Tel: (312) 250-0070
TACNET: 8-439-6160

Indiana
RCA
Mark I - Suite 660
11611 N. Meridian Street
Carmel, IN 46032-9487
Tel: (317) 267-6375
TACNET: 8-422-6375

Kansas
RCA
Suite 208
8575 West 110th Street
Overland Park, KS 66210-2620
Tel: (913) 345-2224
TACNET: 8-422-6371

Massachusetts
RCA
Suite 101
One Newton Exec. Park
Newton, MA 02162-1435
Tel: (617) 969-0141
TACNET: 8-341-1210

Michigan
RCA
30400 Telegraph Road
Birmingham, MI 48010-3095
Tel: (313) 644-1151
TACNET: 8-438-1281

Minnesota
RCA
3600 West 80th Street
Suite 515
Minneapolis, MN 55431-1070
Tel: (612) 835-2004

New Jersey
RCA
485B Route 1, South
Iselin, NJ 08830-3013
Tel: (201) 750-9000
TACNET: 8-325-6090

RCA
700 E. Gate Drive
Mt. Laurel, NJ 08054
Tel: (609) 338-5042
TACNET: 8-222-4473

New York
RCA
160 Perinton Hill Office Park
Fairport, NY 14450-3665
Tel: (716) 223-5240

North Carolina
RCA
2000 Regency Parkway
Suite 150
Cary, NC 27511-8506
Tel: (919) 481-4221

Ohio
RCA
3700 Corporate Drive
Suite 101
Columbus, OH 43229-1739
Tel: (614) 899-9009
TACNET: 8-448-1210

Texas
RCA
La Promenade Center
Suite 111
7115 Burnet Road
Austin, TX 78757-2214
Tel: (512) 467-0386

RCA
17000 Dallas Parkway
Suite 100
Dallas, TX 75248-1921
Tel: (214) 733-0800
TACNET: 8-639-1260

Virginia
RCA
1901 N. Moore Street
Arlington, VA 22209-1766
Tel: (703) 558-4161
TACNET: 8-232-4162

CANADA

Ontario
RCA Inc.
411 Roosevelt Avenue
Suite 203A
Ottawa, Ontario K2A 3X9
Tel: (613) 728-0031

ASIA PACIFIC

Hong Kong
RCA International, Ltd.
13th Floor, Fourseas Bldg.
208-212 Nathan Road
Tsimshatsui, Kowloon
Tel: 3-7236339

Singapore
RCA International, Ltd.
24-15 International Plaza
10 Anson Road
Singapore 0207
Tel: 2224156

Taiwan
RCA SSD
Room 1103, No. 600
Ming Chuan East Road
Taipei
Tel: (02) 7169310

LATIN AMERICA

Argentina
Ramiro E. Podetti Reps.
Casilla de Correo 4622
1000 Buenos Aires
Tel: (01) 393-3919

Mexico
RCA S.A. de C.V./SSD
Avenida Cuithahuac 2519
Apartado Postal 17-570
Mexico City, D.F. 11410
Tel: (905) 399-7228

EUROPE

Belgium
RCA, s.a.
Mercure Centre
Rue de la Fusee 100
1130 Brussels
Tel: 02/720.89.80

France
RCA, s.a.
2-4, Avenue de L'Europe
78140 Velizy
Tel: 33-1-39.46.56.56

Germany
RCA GmbH
Ridlerstrasse 35A
8000 Munchen 2
West Germany
Tel: 089/5026014

RCA GmbH
Justus-von-Liebig-Ring 10
2085 Quickborn
West Germany
Tel: 04106/613-0

RCA GmbH
Zeppelinstrasse 35
7302 Ostfildern 4
West Germany
Tel: 0711/454001

Italy
RCA SpA
Viale Milanofiori L1
20089 Rozzano (MI)
Tel: (02) 8242006

Spain
RCA S.A.
Monte Esquinza 28
28010 Madrid 4
Tel: 01/442 11 00

Sweden
RCA International Ltd
P.O. Box 3047
Hagalundsgatan 8
17103 Solna 3
Tel: 08/83 42 25

U.K.
RCA Ltd
Lincoln Way, Windmill Road
Sunbury-on-Thames
Middlesex TW16 7HW
Tel: 093 27 85511

RCA Authorized Distributors

U.S. and Canada

ALABAMA

Hamilton Avnet Electronics
4940 Research Drive
Huntsville, AL 35805
Tel: (205)837-7210

ARIZONA

Hamilton Avnet Electronics
505 South Madison Drive
Tempe, AZ 85281
Tel: (602)231-5100

Kierulff Electronics, Inc.
4134 East Wood Street
Phoenix, AZ 85040
Tel: (602)243-4101

Schweber Electronics Corp.
11049 N. 23rd Drive, Suite 1100
Phoenix, AZ 85029
Tel: (602)997-4874

Sterling Electronics, Inc.
3501 E. Broadway Road
Phoenix, AZ 85040
Tel: (602)268-2121

Wyle Electronics Marketing Group
17855 N. Black Canyon Highway
Phoenix, AZ 85023
Tel: (602)249-2232

CALIFORNIA

Arrow Electronics, Inc.
19748 Dearborn Street
North Ridge Business Center
Chatsworth, CA 91311
Tel: (213)701-7500

Arrow Electronics, Inc.
1502 Crocker Avenue
Hayward, CA 94544
Tel: (415)487-4600

Arrow Electronics, Inc.
9511 Ridge Haven Court
San Diego, CA 92123
Tel: (619)741-3411

Arrow Electronics, Inc.
521 Weddell Drive
Sunnyvale, CA 94086
Tel: (408)745-6600

Arrow Electronics, Inc.
2961 Dow Avenue
Tustin, CA 92680
Tel: (714)838-5422

Avnet Electronics
20501 Plummer Street
Chatsworth, CA 91311
Tel: (818)700-2600

Avnet Electronics
350 McCormick Avenue
Costa Mesa, CA 92626
Tel: (714)754-6051

Hamilton Avnet Electronics
1361-B W. 190th Street
Gardena, CA 90248
Tel: (213)615-3900

Hamilton Avnet Electronics
3002 E.G. Street
Ontario, CA 91764
Tel: (714)989-4602

Hamilton Avnet Electronics
4103 Northgate Boulevard
Sacramento, CA 95834
Tel: (916)920-3150

Hamilton Avnet Electronics
4545 Viewridge Avenue
San Diego, CA 92123
Tel: (714)571-7510

Hamilton Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, CA 94086
Tel: (408)743-3300

Hamilton Electro Sales
9650 Desoto Avenue
Chatsworth, CA 91311
Tel: (818)700-1222

Hamilton Electro Sales
3170 Pullman Street
Costa Mesa, CA 92626
Tel: (714)641-4107

Hamilton Electro Sales
10912 W. Washington Boulevard
Culver City, CA 90230
Tel: (213)558-2121

Kierulff Electronics, Inc.
10824 Hope Street
Cypress, CA 90630
Tel: (714)220-6300

Kierulff Electronics, Inc.
5650 Jillson Street
Los Angeles, CA 90040
Tel: (213)725-0325

Kierulff Electronics, Inc.
8797 Balboa Avenue
San Diego, CA 92123
Tel: (714)278-2112

Kierulff Electronics, Inc.
1180 Murphy Avenue
San Jose, CA 95131
Tel: (408)971-2600

Kierulff Electronics, Inc.
14101 Franklin Avenue
Tustin, CA 92680
Tel: (714)731-5711

Schweber Electronics Corp.
21139 Victory Boulevard
Canoga Park, CA 91303
Tel: (818)999-4702

Schweber Electronics Corp.
17822 Gillette Avenue
Irvine, CA 92714
Tel: (714)863-0200

Schweber Electronics Corp.
6730 Nancyridge Drive
San Diego, CA 92121
Tel: (619)450-0454

Schweber Electronics Corp.
90 East Tasman Drive
San Jose, CA 95134
Tel: (408)946-7171

Wyle Electronics Marketing Group
26677 Agoura Road
Calabasas, CA 91302
Tel: (818)880-9001

Wyle Electronics Marketing Group
124 Maryland Avenue
El Segundo, CA 90245
Tel: (213)322-8100

Wyle Electronics Marketing Group
17872 Cowan Avenue
Irvine, CA 92714
Tel: (714)863-9953

Wyle Electronics Marketing Group
1151 Sun Center Drive
Rancho Cordova, CA 95670
Tel: (916)638-5282

Wyle Electronics Marketing Group
9525 Chesapeake Drive
San Diego, CA 92123
Tel: (714)565-9171

Wyle Electronics Marketing Group
3000 Bowers Avenue
Santa Clara, CA 95052
Tel: (408)727-2500

COLORADO

Arrow Electronics Inc.
1390 So. Potomac Street
Suite 136
Aurora, CO 80012
Tel: (303)696-1111

Hamilton Avnet Electronics
8765 E. Orchard Road
Suite 708, Englewood, CO 80111
Tel: (303)740-1000

Kierulff Electronics, Inc.
7060 So. Tucson Way
Englewood, CO 80112
Tel: (303)790-4444

Schweber Electronics Corp.
8955 E. Nichols Avenue
Englewood, CO 80112
Tel: (303)799-0258

Wyle Electronics Marketing Group
451 East 124th Avenue
Thornton, CO 80241
Tel: (303)457-9953

CONNECTICUT

Arrow Electronics, Inc.
12 Beaumont Road
Wallingford, CT 06492
Tel: (203)265-7741

Hamilton Avnet Electronics
Commerce Drive
Commerce Industrial Park
Danbury, CT 06810
Tel: (203)797-2800

Kierulff Electronics, Inc.
10 Capital Drive
Wallingford, CT 06492
Tel: (203)265-1115

Milgray Electronics, Inc.
378 Boston Post Road
Orange, CT 06477
Tel: (203)795-0711

Schweber Electronics Corp.
Finance Drive
Commerce Industrial Park
Danbury, CT 06810
Tel: (203)748-7080

FLORIDA

Arrow Electronics, Inc.
350 Fairway Drive
Deerfield, FL 33441
Tel: (305)429-8200

Arrow Electronics, Inc.
1530 Bottlebush Drive
Palm Bay, FL 32905
Tel: (305)725-1480

***Chip Supply**
7725 No. Orange Blossom Trail
Orlando, FL 32810
Tel: (305)298-7100

*Chip distributor only.

RCA Authorized Distributors

U.S. and Canada (Cont'd)

FLORIDA

Hamilton Avnet Electronics
6801 NW 15th Way
Ft. Lauderdale, FL 33309
Tel: (305)971-2900

Hamilton Avnet Electronics
3197 Tech Drive, No.
St. Petersburg, FL 33702
Tel: (813)576-3930

Hamilton Avnet Electronics
6947 University Boulevard
Winter Park, FL 32792
Tel: (305)628-3888

Kieruiff Electronics, Inc.
5410 N.W. 33rd Avenue
Ft. Lauderdale, FL 33309-6316
Tel: (305)486-4004

Kieruiff Electronics, Inc.
3247 Tech Drive
St. Petersburg, FL 33702
Tel: (813)576-1966

Milgray Electronics, Inc.
1850 Lee World Center
Suite 104
Winter Park, FL 32789
Tel: (305)647-5747

Schweber Electronics Corp.
2830 North 28th Terrace
Hollywood, FL 33020
Tel: (305)927-0511

GEORGIA

Arrow Electronics, Inc.
3155 Northwood Parkway
Suite A
Norcross, GA 30071
Tel: (404)449-8252

Hamilton Avnet Electronics
5825D Peachtree Corners
Norcross, GA 30092
Tel: (404)447-7503

Kieruiff Electronics, Inc.
5824 Peachtree Corners East
Norcross, GA 30092
Tel: (404)447-5252

Schweber Electronics Corp.
303 Research Drive
Suite 210
Norcross, GA 30092
Tel: (404)449-9170

ILLINOIS

Arrow Electronics, Inc.
2000 Algonquis Road
Schaumburg, IL 60193
Tel: (312)397-3440

Hamilton Avnet Electronics
1130 Thorndale Avenue
Bensenville, IL 60106
Tel: (312)860-7700

Kieruiff Electronics, Inc.
1140 West Thorndale
Itasca, IL 60143
Tel: (312)640-0200

Newark Electronics
4801 N. Ravenswood
Chicago, IL 60640-4496
Tel: (312)784-5100

Schweber Electronics Corp.
904 Cambridge Drive
Elk Grove Village, IL 60007
Tel: (312)364-3750

INDIANA

Arrow Electronics, Inc.
2495 Directors Row, Suite H
Indianapolis, IN 46241
Tel: (317)243-9353

Graham Electronics Supply, Inc.
133 S. Pennsylvania Street
Indianapolis, IN 46204
Tel: (317)634-8202

Hamilton Avnet Electronics, Inc.
485 Gradle Drive
Carmel, IN 46032
Tel: (317)844-9333

IOWA

Hamilton/Avnet Electronics
915 33rd Avenue, S.W.
Cedar Rapids, IA 52404
Tel: (319)362-4757

KANSAS

Hamilton Avnet Electronics
9219 Quivira Road
Overland Park, KS 66215
Tel: (913)888-8900

Milgray Electronics, Inc.
6901 W. 63rd Street
Overland Park, KS 66202
Tel: (913)236-8800

MARYLAND

Arrow Electronics, Inc.
8300 Guildford Road
Columbus, MD 21046
Tel: (301)995-0003

Hamilton Avnet Electronics
6822 Oakhill Lane
Columbia, MD 21045
Tel: (301)995-3500

Kieruiff Electronics, Inc.
825D Hammons Ferry Road
Linthicum, MD 21090
Tel: (301)636-5800

Schweber Electronics Corp.
9330 Gaithers Road
Gaithersburg, MD 20877
Tel: (301)840-5900

MASSACHUSETTS

Arrow Electronics, Inc.
Arrow Drive
Woburn, MA 01801
Tel: (617)933-8130

Hamilton Avnet Electronics
10D Centennial Drive
Peabody, MA 01960
Tel: (617)531-7430

***Hybrid Components Inc.**
72 Cherry Hill Drive
Beverly, MA 01915
Tel: (617)927-5820

Kieruiff Electronics, Inc.
13 Fortune Drive
Billerica, MA 01821
Tel: (617)667-8331

A. W. Mayer Co.
34 Linnell Circle
Billerica, MA 01821
Tel: (617)229-2255

Schweber Electronics Corp.
25 Wiggins Avenue
Bedford, MA 01710
Tel: (617)275-5100

***SerTech**
10B Centennial Drive
Peabody, MA 01960
Tel: (617)531-8673

Sterling Electronics, Inc.
15D Constitution Way
Woburn, MA 01801
Tel: (617)938-6200

MICHIGAN

Arrow Electronics, Inc.
755 Phoenix Drive
Ann Arbor, MI 48104
Tel: (313)971-8220

Hamilton Avnet Electronics
2215 29th Street
Grand Rapids, MI 49503
Tel: (616)243-8805

Hamilton Avnet Electronics
32487 Schoolcraft Road
Livonia, MI 48150
Tel: (313)522-4700

Schweber Electronics Corp.
12060 Hubbard Avenue
Livonia, MI 48150
Tel: (313)525-8100

MINNESOTA

Arrow Electronics, Inc.
5230 West 73rd Street
Edina, MN 55435
Tel: (612)830-1800

Hamilton Avnet Electronics
10300 Bren Road, East
Minnetonka, MN 55343
Tel: (612)932-0600

Kieruiff Electronics, Inc.
7667 Cahill Road
Edina, MN 55435
Tel: (612)941-7500

Schweber Electronics Corp.
7424 W. 78th Street
Edina, MN 55435
Tel: (612)941-5280

MISSOURI

Arrow Electronics, Inc.
2380 Schultz Road
St. Louis, MO 63141
Tel: (314)567-6888

Hamilton Avnet Electronics
13743 Shoreline Court East
Earth City, MO 63045
Tel: (314)344-1200

Kieruiff Electronics, Inc.
2608 Metro Park Boulevard
Maryland Heights, MO 63043
Tel: (314)739-0855

NEW HAMPSHIRE

Arrow Electronics, Inc.
One Perimeter Drive
Manchester, NH 03103
Tel: (603)668-6968

Hamilton Avnet Electronics
444 E. Industrial Park Drive
Manchester, NH 03103
Tel: (603)624-9400

*Chip distributor only.

RCA Authorized Distributors

U.S. and Canada (Cont'd)

NEW JERSEY

Arrow Electronics, Inc.
6000 Lincoln Drive East
Marlton, NJ 08053
Tel: (609)596-8000

Arrow Electronics, Inc.
Two Industrial Road
Fairfield, NJ 07006
Tel: (201)575-5300

Hamilton Avnet Electronics
Ten Industrial Road
Fairfield, NJ 07006
Tel: (201)575-3390

Hamilton Avnet Electronics
One Keystone Avenue
Cherry Hill, NJ 08003
Tel: (609)424-0110

Kierulff Electronics, Inc.
37 Kulick Road
Fairfield, NJ 07006
Tel: (201)575-6750

Kierulff Electronics, Inc.
520 Fellowship Road
Mt. Laurel, NJ 08054
Tel: (609)235-1444

Schweber Electronics Corp.
18 Madison Road
Fairfield, NJ 07006
Tel: (201)227-7880

NEW MEXICO

Arrow Electronics, Inc.
2460 Alamo, SE
Albuquerque, NM 87106
Tel: (505)243-4566

Hamilton Avnet Electronics
2524 Baylor S.E.
Albuquerque, NM 87106
Tel: (505)765-1500

Sterling Electronics, Inc.
3540 Pan American
Freeway, N.E.
Albuquerque, NM 87107
Tel: (505)884-1900

NEW YORK

Arrow Electronics, Inc.
20 Oser Avenue
Hauppauge, L.I., NY 11788
Tel: (516)231-1000

Arrow Electronics, Inc.
7705 Maltlage Drive
Liverpool, NY 13088
Tel: (315)652-1000

Arrow Electronics, Inc.
25 Hub Drive
Melville, L.I., NY 11747
Tel: (516)391-1300

Arrow Electronics, Inc.
3375 Brighton Henrietta Towline Rd.
Rochester, NY 14623
Tel: (716)427-0300

Hamilton Avnet Electronics
933 Motor Parkway
Hauppauge, L.I., NY 11788
Tel: (516)231-9800

Hamilton Avnet Electronics
333 Metro Park
Rochester, NY 14623
Tel: (716)475-9130

Hamilton Avnet Electronics
103 Twin Oaks Drive
Syracuse, NY 13206-1200
Tel: (315)437-2641

Milgray Electronics, Inc.
77 Schmitt Boulevard
Farmingdale, L.I., NY 11735
Tel: (516)420-9800

Schweber Electronics Corp.
Two Townline Circle
Rochester, NY 14623
Tel: (716)424-2222

Schweber Electronics Corp.
Jericho Turnpike
Westbury, L.I., NY 11590
Tel: (516)334-7474

Summit Distributors, Inc.
916 Main Street
Buffalo, NY 14202
Tel: (716)884-3450

NORTH CAROLINA

Arrow Electronics, Inc.
5240 Greensdairy Road
Raleigh, NC 27604
Tel: (919)876-3132

Hamilton Avnet Electronics
3510 Spring Forest Road
Raleigh, NC 27604
Tel: (919)878-0810

Kierulff Electronics Inc.
One North Commerce Center
5249 North Boulevard
Raleigh, NC 27604
Tel: (919)872-8410

Schweber Electronics Corp.
5285 North Boulevard
Raleigh, NC 27604
Tel: (919)876-0000

OHIO

Arrow Electronics, Inc.
7620 McEwen Road
Centerville, OH 45459
Tel: (513)435-5563

Arrow Electronics, Inc.
6238 Cochran Road
Solon, OH 44139
Tel: (216)248-3990

Hamilton Avnet Electronics
4588 Emery Industrial Parkway
Warrensville Hts., OH 44128
Tel: (216)831-3500

Hamilton Avnet Electronics
954 Senate Drive
Dayton, OH 45459
Tel: (513)433-0610

Hamilton Avnet Electronics
777 Brooksedge Boulevard
Westerville, OH 43081
Tel: (614)882-7004

Hughes-Peters, Inc.
481 East Eleventh Avenue
Columbus, OH 43211
Tel: (614)294-5351

Kierulff Electronics, Inc.
23060 Miles Road
Cleveland, OH 44128
Tel: (216)587-6558

Milgray Electronics, Inc.
6155 Rockside Road
Cleveland, OH 44131
Tel: (216)447-1520

Schweber Electronics Corp.
23880 Commerce Park Road
Beachwood, OH 44122
Tel: (216)464-2970

OKLAHOMA

Kierulff Electronics, Inc.
Metro Park 12318 East 60th
Tulsa, OK 74145
Tel: (918)252-7537

Sterling Electronics, Inc.
5119 So. 10th E. Avenue
Tulsa, OK 74146
Tel: (918)663-2410

OREGON

Arrow Electronics, Inc.
10260 S.W. Nimbus Ave., Suite M-3
Portland, OR 97223
Tel: (503)684-1690

Hamilton Avnet Electronics
6024 S.W. Jean Road
Bldg. C, Suite 10
Lake Oswego, OR 97034
Tel: (503)635-8157

Wyle Electronics Marketing Group
5289 N.E. Ezram Young Parkway
Hillsboro, OR 97123
Tel: (503)640-6000

PENNSYLVANIA

Arrow Electronics, Inc.
650 Seco Road
Monroeville, PA 15146
Tel: (412)856-7000

Hamilton Avnet Electronics
2800 Liberty Avenue, Bldg. E
Pittsburgh, PA 15222
Tel: (412)281-4150

Herbach & Rademan, Inc.
401 East Erie Avenue
Philadelphia, PA 19134
Tel: (215)426-1700

Schweber Electronics Corp.
231 Gibralter Road
Horsham, PA 19044
Tel: (215)441-0600

TEXAS

Arrow Electronics, Inc.
22227 West Breaker Lane
Austin, TX 78758
Tel: (512)835-4180

Arrow Electronics, Inc.
3220 Commander Drive
Carrollton, TX 75006
Tel: (214)380-6464

Arrow Electronics, Inc.
10899 Kinghurst Dr., Suite 100
Houston, TX 77099
Tel: (713)530-4700

Hamilton Avnet Electronics
1807A W. Braker Lane, #A
Austin, TX 78758-3605
Tel: (512)837-8911

Hamilton Avnet Electronics
2111 West Walnut Hill Lane
Irving, TX 75060
Tel: (214)659-4111

RCA Authorized Distributors

U.S. and Canada (Cont'd)

TEXAS

Hamilton Avnet Electronics
4850 Wright Road, Suite 190
Stafford, TX 77477
Tel: (713)240-7898

Kieruiff Electronics, Inc.
3007 Longhorn Blvd., Suite 105
Austin, TX 78758
Tel: (512)835-2090

Kieruiff Electronics, Inc.
9610 Skillman Avenue
Dallas, TX 75243
Tel: (214)343-2400

Kieruiff Electronics, Inc.
10415 Landsbury Drive, Suite 210
Houston, TX 77099
Tel: (713)530-7030

Schweber Electronics Corp.
4202 Beltway
Dallas, TX 75234
Tel: (214)661-5010

Schweber Electronics Corp.
10625 Richmond Ste. 100
Houston, TX 77042
Tel: (713)784-3600

Sterling Electronics, Inc.
2335A Kramer Lane, Suite A
Austin, TX 78758
Tel: (512)836-1341

Sterling Electronics, Inc.
11090 Stemmons Freeway
Stemmons at Southwell
Dallas, TX 75229
Tel: (214)243-1600

Sterling Electronics, Inc.
4201 Southwest Freeway
Houston, TX 77027
Tel: (713)627-9800

Wyle Electronics Marketing Group
1840 Greenville Avenue
Richardson, TX 75081
Tel: (214)235-9953

UTAH

Hamilton Avnet Electronics
1585 West 2100 South
Salt Lake City, UT 84119
Tel: (801)972-2800

Kieruiff Electronics, Inc.
2121 S. 3600 West Street
Salt Lake City, UT 84119
Tel: (801)973-6913

Wyle Electronics Marketing Group
1959 South 4130 West Unit B
Salt Lake City, UT 84104
Tel: (801)974-9953

WASHINGTON

Arrow Electronics, Inc.
14320 N.E. 21st Street
Bellevue, WA 98005
Tel: (206)643-4800

Hamilton Avnet Electronics
14212 N.E. 21st Street
Bellevue, WA 98005
Tel: (206)453-5874

Kieruiff Electronics, Inc.
19450 68th Avenue
South Kent, WA 98032
Tel: (206)575-4420

Priebe Electronics, Inc.
12908 N.E. 125th Way
Kirkland, WA 98034
Tel: (206)821-4695

Wyle Electronics Marketing Group
1750 132nd Avenue, N.E.
Bellevue, WA 98005
Tel: (206)453-8300

WISCONSIN

Arrow Electronics, Inc.
200 No. Patrick Boulevard
Brookfield, WI 53005
Tel: (414)792-0150

Hamilton Avnet Electronics
2975 South Moorland Road
New Berlin, WI 53151
Tel: (414)784-4510

Kieruiff Electronics, Inc.
2238 E.W. Bluemound Road
Waukesha, WI 53186-2916
Tel: (414)784-8160

Taylor Electric Company
1000 W. Donges Bay Road
Mequon, WI 53092
Tel: (414)241-4321

Canada

ALBERTA

Hamilton/Avnet (Canada) Ltd.
2816 21st St. N.E.
Calgary, Alberta T2E 6Z2
Tel: (403)230-3586

L. A. Varah, Ltd.
6420 6A Street SE
Calgary, Alberta T2H ZB7
Tel: (403)255-9550

BRITISH COLUMBIA

L. A. Varah, Ltd.
2077 Alberta Street
Vancouver, B.C. V5Y 1C4
Tel: (604)873-3211

R.A.E. Industrial Electronics, Ltd.
3455 Gardner Court
Burnaby, B.C. V5G 4J7
Tel: (604)291-8866

MANITOBA

L. A. Varah, Ltd.
#12 1832 King Edward Street
Winnipeg, Manitoba R2R 0N1
Tel: (204)633-6190

ONTARIO

Arrow/Cesco
24 Martin Ross Road
Downsview, Ontario M3J 2K9
Tel: (416)661-0220

Arrow/Cesco
148 Colonnade Road
Nepean, Ontario K2E 7J5

Hamilton Avnet (Canada) Ltd.
6845 Rexwood Drive
Units 3,4,5
Mississauga, Ontario L4V 1M5
Tel: (416)677-7432

Hamilton Avnet (Canada) Ltd.
210 Colonnade Street
Nepean, Ontario K2E 7L5
Tel: (613)226-1700

L. A. Varah, Ltd.
504A Iroquois Shore Drive
Ontario L6H 3K4
Tel: (416)561-9311

QUEBEC

Arrow/Cesco
4050 Jean Talon Street, West
Montreal, Quebec H4P 1W1
Tel: (514)735-5511

Hamilton Avnet (Canada) Ltd.
2670 Sabourin Street
St. Laurent, Quebec H4S 1M2
Tel: (514)331-6443

Europe, Middle East, and Africa

AUSTRIA

TVG
Transistor Vertriebsgesellschaft
mbH & Co KG
Auhofstrasse 41A
1130 Vienna
Tel: 0222/8294510

BELGIUM

Ineico Belgium S.A.
Avenue des Croix de Guerre 94
1120 Brussels
Tel: 02/216 01 60

DENMARK

Tage Olsen A/S
P.O. Box 225
2750 Ballerup
Tel: 02/65 81 11

EGYPT

Sakrco Enterprises
P.O. Box 1133
37 Kasr El Nil Street, Apt. 5
Cairo
Tel: 744440

ETHIOPIA

General Trading Agency
P.O. Box 1684
Addis Ababa
Tel: 132718-137275

FINLAND

Telercas OY
P.O. Box 33
04201 Kerava
Tel: 0/248.055

FRANCE

Almex
48, rue de l'Aubepine
92160 Antony
Tel: (1)46.66.21.12

***Hybritech**
Route de Bua
ZAC des Godets
91370 Verrieres-Le-Buisson
Tel: (1)69.20.22.10

Radio Equipements
Antares S.A.
9, rue Ernest Cognacq
92301 Levallois Perret
Tel: (1)47.58.11.11

Radio Television Francais
9, rue D'Arcueil
94250 Gentilly
Tel: (1)46.64.11.01

*Chip Distributor only.

RCA Authorized Distributors

Europe, Middle East, and Africa (Cont'd)

FRANCE

Tekelec Airtronic S.A.
Cite des Bruyeres
Rue Carle Vernet
92310 Sevres
Tel: (1)45.34.75.35

GERMANY

Alfred Neye Enatechnik GmbH
Schillerstrasse 14
2085 Quickborn
West Germany
Tel: 04106/6120

▪Asternetics GmbH
Lindenring 3
8021 Taufkirchen
Tel: 089/61 21007

ECS Hilmar Frehsdorf GmbH
Electronic Components Service
Carl-Zeiss-Strasse 3
2085 Quickborn
West Germany
Tel: 04106/70 050

ELECTRONIC 2000
Stahlgruberring 12
8000 Munchen 82
Tel: 089/42 001-0

Elkose GmbH
Bahnhofstrasse 44
7141 Moeglingen
West Germany
Tel: 07141/487-1

Sasco GmbH
Hermann-Oberth-Strasse 16
8011 Putzbrunn bei Munchen
West Germany
Tel: 089/46111

Spoerle Electronic KG
Max-Planck-Strasse 1-3
6072 Dreieich bei Frankfurt
West Germany
Tel: 06103/3041

GREECE

Semicon Co.
104 Aeolou Str.
TT 131 Athens
Tel: 3253626

HUNGARY

Hungagent
P.O. Box 542
1374 Budapest
Tel: 01/669-385

ICELAND

Georg Amundason
P.O. Box 698, Reykjavik
Tel: 81180

ISRAEL

Aviv Electronics
Kehilat Venezia Street 12
69010 Tel-Aviv
Tel: 03-494450

ITALY

Eledra SpA
Viale Elvezia 18
20154 Milano
Tel: (02)349 751

IDAC Elettronica SpA
Via Verona 8
35010 Busa di Vigonza
Tel: (049)72.56.99

LASI Elettronica SpA
Viale Fulvio Testi 126
20092 Cinisello Balsamo (MI)
Tel: (02)24 40 012

Silverstar Ltd.
Via dei Gracchi 20
20146 Milano
Tel: (02)49 96

KUWAIT

Morad Yousuf Behbehani
P.O. Box 146
Kuwait

MOROCCO

Societe d'Equipement Mecanique et Electrique SA (S.E.M.E.)
rue Ibn Batouta 29
Casablanca
Tel: (212)22.08.65

THE NETHERLANDS

Koning en Hartman Elektrotechniek BV
Postbus 125
2600 AC Delft
Tel: (15)60 99 06

Vekano BV
Postbus 6115
5600 HC Eindhoven
Tel: (40)82 98 98

NORWAY

National Elektro A/S
P.O. Box 53, Ulvenveien 75
Okern, Oslo 5
Tel: (472)64 49 70

PORTUGAL

Cristalonica Componentes de Radio e Televisao, Lda
Rua Bernardim Ribeiro, 25
1100 Lisbon
Tel: (019)53 46 31

SOUTH AFRICA

Allied Electronic Components (PTY) Ltd.
P.O. Box 6387
Dunswart 1508
Tel: (011)528-661

SPAIN

Diode Espana S.A.
Edifico Iberia Mart
Avda. de Brasil, 5, 1
28020 Madrid
Tel: 1/455 36 86

Kontron S.A.
Salvatierra 4
Madrid 34
Tel: 1/729.11.55

SWEDEN

Ferner Electronics AB
Snormakarvagen 35
P.O. Box 125
16126 Bromma Stockholm
Tel: 08/80 25 40

Nordisk Elektronik AB
P.O. Box 1409
17127 Solna
Tel: 08/734 97 70

SWITZERLAND

Baerlocher AG
Forrlibuckstrasse 110
8005 Zurich
Tel: (01)42.99.00

TURKEY

Zer Kollektif Sti
Guniz Sokak 17
Kavaklidere
Ankara
Tel: (41)67.08.39

U.K.

ACCESS Electronic Components Ltd.
Jubilee House, Jubilee Road
Letchworth, Hertfordshire SG6 1QH
Tel: Letchworth (0462)68 2333

Gothic Crellon Electronics Ltd.
3 The Business Centre
Molly Millars Lane
Wokingham, Berkshire RG11 2EY
Tel: (0734)78 7848

Jermyn Distribution
Vestry Industrial Estate
Otford Road
Sevenoaks, Kent TN14 5EU
Tel: Sevenoaks (0732)450144

Macro Marketing Ltd.
Burnham Lane
Slough, Berkshire SL1 6LN
Tel: Burnham (06286)4422

Micromark Electronics, Ltd.
Boyn Valley Road
Maidenhead, Berks SL6 4DT
Tel: (0628)76 176

STC Electronics Services
Edinburgh Way
Harlow, Essex, CM20 2DF
Tel: Harlow (0279)26777

VSI Electronics Ltd.
Roydonbury Industrial Park
Horsecroft Road
Harlow, Essex CM19 5BY
Tel: Harlow (0279)29666

YUGOSLAVIA

Avtotehna
P.O. Box 593, Celovska 175
61000 Ljubljana
Tel: (061)552 341

ZAMBIA

African Technical Associates Ltd.
Stand 5196 Luanshya Road
Lusaka

ZIMBABWE

BAK Electrical Holdings (Pvt) Ltd.
30 Pioneer Street
Harare

▪High-Rel Specialist

RCA Authorized Distributors

Asia Pacific

AUSTRALIA

AWA (Aust.) Ltd.
North Ryde Division
Corner Lane Cove & Talavera Roads
Macquarie Park
North Ryde, N.S.W. 2113

Amtron Tyree Pty. Ltd.
176 Cope Street
Waterloo, N.S.W. 2017

BANGLADESH

Electronic Engineers & Consultants Ltd.
103 Elephant Road, 1st Floor
Dacca 5

HONG KONG

Gibb Livingston & Co., Ltd.
13/F., Tai Yau Building
181 Johnston Road
Wanchai

Hong Kong Electronic Components Co.
Flat A Yun Kai Bldg. 1/F1
466-472 Nathan Road
Kowloon

INDIA

Photophone Ltd.
179-5 Second Cross Road
Lower Palace Orchards
Bangalore 560 003

INDONESIA

NVPD Soedarpo Corp.
Samudera Indonesia Building
JL Letten, Jen. S
Parman No. 35 Slipi
Jakarta Barat

JAPAN

Okura & Company Ltd.
3-6 Ginza, Nichome, Chuo-Ku
Tokyo 104

KOREA

Panwest Company, Ltd.
Room 1202 Sam Heung Bldg.
32 Eulchi-ro 1-ka, Chung-Ku
Seoul, Republic of South Korea

Shin-A Trading Company
Room 406, Koryo Bldg.
88-7 Nonhyon-Dong
Kangnam-ku
Seoul, Republic of South Korea

NEPAL

Continental Commercial Distributors
Phohara Durbar
Durbarmarga
Kathmandu

NEW ZEALAND

AWA NZ Ltd.
N.Z. P.O. Box 50-248
Porirua

PHILIPPINES

Philippine Electronics Inc.
P.O. Box 498
3rd Floor, Rose
Industrial Bldg., 11 Pioneer St.
Pasig, Metro Manila

Semitronics Philippines
P.O. Box 445 Greenhills
San Juan 3113
Metro Manila

SINGAPORE

Device Electronics Pte. Ltd.
101 Kitchener Road No. 02-04
Singapore 0820

Microtronics Assoc. Pte. Ltd.
8 Lorong Bakar Batu, No. 03-01
Kolam Ayer Industrial Park
Singapore 1334

SRI LANKA

C.W. Mackie & Co. Ltd.
36 D.R. Wijewardena Mawatha
Colombo 10

TAIWAN

Delta Engineering Ltd.
No. 42 Hsu Chang Street
8th Floor, Taipei

Sertek International Inc.
No. 315, Fu Shin North Road
Taipei 104

Teco Enterprise Co. Ltd.
2nd Floor, No. 120, Sec. 2
Chung Hsiao East Road
Taipei

THAILAND

Better Pro Co. Ltd.
71 Chakkawat Road
Wat Tuk, Bangkok

Latin America

ARGENTINA

Eneka S.A.I.C.F.I.
Tucuman 299
1049 Buenos Aires
Tel: 31-3363

Radiocom S.A.
Conesa 1003
1426 Buenos Aires
Tel: 551-2780

Tecnos S.R.L.
Independencia 1861
1225 Buenos Aires
Tel: 37-0239

BRAZIL

Commercial Bezerra Ltda.
Rua Costa Azevedo, 139
CEP-69.000 Manaus/AM
Tel: 322-5363

Panamericana Comercial Importadora Ltda.
Rua Aurora, 263
01209, Sao Paulo, SP
Tel: 222-3211

CHILE

Raylex Ltda.
Av Providencia 1244
Depto.D, 3er Piso
Casilla 13373, Santiago
Tel: 749835

Industria de Radio y Television S.A. (IRT)
Vic. MacKenna 3333
Casilla 170-D, Santiago
Tel: 510081

COLOMBIA

Miguel Antonio Pena Pena Y Cia. S. En C.
Carrera 12 #1906
Bogota
Tel: 243-7317

Electronica Moderna
Carrera 9A, NRO 19-52
Apartado Aereo 5361
Bogota, D.E.1
Tel: 282286

COSTA RICA

J. G. Valldeperas, S.A.
Calle 1, Avenidas 1-3
Apartado Postal 3923
San Jose
Tel: 223614

DOMINICAN REPUBLIC

Humberto Garcia, C. por A.
El Conde 366
Apartado de Correos 771
Santo Domingo
Tel: 682-3645

ECUADOR

Elecom, S.A.
Junin 618 y Boyaca
P.O. Box 9611, Guayaquil
Tel: 307786

EL SALVADOR

Radio Electrica, S.A.
4A Avenida Sur Nb. 228
San Salvador
Tel: 21-5609

Radio Parts, S.A.
Sra. Bertha de Diaz
4a Avenida Sur #425
P.O. Box 1262, San Salvador
Tel: 21-3019

GUATEMALA

Electronica Guatemalteca
13 Calle 5-59, Zona 1
P.O. Box 514
Guatemala City
Tel: 25-649

Tele-Equipos, S.A.
Torre Professional 2, Of. 501
6a, Av. 0-60, Zona 4
Apartado Postal 1798
Guatemala City
Tel: 29-805

RCA Authorized Distributors

Latin America (Cont'd)

HAITI

Societe Haitienne D'Automobiles, S.A.
P.O. Box 428
Port-Au-Prince
Tel: 2-2347

HONDURAS

Francisco J. Yones
3A Avenida S.O. 5
San Pedro Sula
Honduras, Central America
Tel: 543001

MEXICO

Dicopel, S.A.
Tochtli No. 368 Fracc.
San Antonio Azcapotzalco
02760 Mexico, D.F.

Electronica Remberg, S.A. de C.V.
Rep. Del Salvador No. 30-101
Mexico City 1, D.F.
Tel: 510-47-49

Mexicana de Bulbos, S.A.
Michoacan No. 30
Mexico 11, D.F.
Tel: 564-92-33

Partes Electronicas, S.A.
Republica Del Salvador 30-501
Mexico City 1, DF
Tel: (905)585-3640

Raytel, S.A.
Sullivan 47 Y 49
Mexico 4, D.F.
Tel: (905)546-0663

NICARAGUA

Comercial F. A. Mendieta, S.A.
Apartado Postal No. 1956
C.S.T. 5c A1 Sur 2c 1/2 Abajo
Managua
Tel: 61406

PANAMA

Tropelco, S.A.
P.O. Box 8465
Via Espana 20-18, Panama 7
Rep. de Panama
Tel: 23-1285

PARAGUAY

Compania Comercial Del Paraguay, S.A.
Casilla de Correo 344
Calle Chile 877, Asuncion
Tel: 91-460

PERU

Arven S.A.
PSJ Adan Mejia 103, OF. 33
Lima 11
Tel: 716229

SURINAM

Kirpalani's Ltd.
17-27 Maagdenstreet
P.O. Box 251, Paramaribo
Tel: 71-400

Surinam Electronics
Keizerstreet 206
P.O. Box 412
Paramaribo
Tel: 76-555

TRINIDAD

Kirpalani's Limited
Kirpalani's Komplex
Churchill Roosevelt Highway
San Juan, Port-of-Spain
Tel: 638-2224/9

URUGUAY

American Products S.A. (APSA)
Casilla de Correo 1438
Canelones 1133
Montevideo
Tel: 902735

VENEZUELA

P. Benavides, P., S.R.L.
Residencies Camarat, Local 7
La Candelaria, Caracas
MAIL ADDRESS: Apartado Postal 20.249
San Martin, Caracas
Tel: 571-21-46

WEST INDIES

Da Costa and Musson Ltda.
Carlisle House
Hincks Street
P.O. Box 103
Bridgetown, Barbados
Tel: 608-50

RCA Manufacturers' Representatives

United States

ALABAMA

Electronic Sales, Inc. (ESI)
303 Williams Avenue
Suite 422
Huntsville, AL 35801
Tel: (205)533-1735

CALIFORNIA

CK Associates
8333 Clairemont Mesa Blvd.
Suite 102
San Diego, CA 92111
Tel: (619)279-0420

Pinnacle Sales
275 Saratoga Avenue
Suite 200
Santa Clara, CA 95050
Tel: (408)249-7400

CONNECTICUT

COM-SALE, Inc.
5 Shire Drive
P.O. Box 946
Wallingford, CT 06492
Tel: (203)269-7964

FLORIDA

G.F. Bohman Assoc., Inc.
130 N. Park Avenue
Apopka, FL 32703
Tel: (305)886-1882

G.F. Bohman Assoc., Inc.
2020 W. McNab Road
Ft. Lauderdale, FL 33309
Tel: (305)979-0008

GEORGIA

Electronic Sales, Inc. (ESI)
3103A Medlock Bridge Road
Norcross, GA 30071
Tel: (404)448-6554

INDIANA

Electronic Mktg. Consultants, Inc. (EMCI)
5259 No. Tacoma Avenue
Suite 8
Indianapolis, IN 46220
Tel: (317)253-1668

IOWA

REP Associates Corp.
4905 Lakeside Drive, NE
Cedar Rapids, IA 52402
Tel: (319)373-0152

KANSAS

Electri-Rep Inc.
7050 W. 107th Street
Suite 210
Overland Park, KS 66212
Tel: (913)649-2168

MASSACHUSETTS

COM-SALE, Inc.
105 Chestnut Street
Needham, MA 02192
Tel: (617)444-8071

MICHIGAN

Rathsburg Assocs., Inc.
16621 E. Warren Avenue
Detroit, MI 48224
Tel: (313)882-1717

MINNESOTA

Comprehensive Technical Sales (COM-TEK)
8053 Bloomington Freeway
Suite 138
Minneapolis, MN 55420
Tel: (612)888-7011

MISSOURI

Electri-Rep Inc.
2300 Westport Plaza Drive
Suite 303
St. Louis, MO 63146
Tel: (314)878-8209

NEW HAMPSHIRE

COM-SALE, Inc.
101 High Street
Exeter, NH 03833
Tel: (603)772-3300

NEW JERSEY

Astrorep, Inc.
717 Convery Boulevard
Perth Amboy, NJ 08861
Tel: (201)826-8050

Tritek Sales, Inc.
21 East Euclid Avenue
Haddonfield, NJ 08033
Tel: (609)429-1551

RCA Manufacturers' Representatives (Cont'd)

United States

NEW YORK

Astrorep, Inc.
103 Cooper Street
Babylon, L.I., NY 11702
Tel: (516)422-2500

Foster & Wager, Inc.
2507 Browncraft Blvd.
Rochester, NY 14625
Tel: (716)385-7744

NORTH CAROLINA

Electronic Sales, Inc. (ESI)
315 No. Academy Street
Suite 206
Cary, NC 27511
Tel: (919)467-8486

OHIO

Lyons Corporation
4812 Frederick Road
Suite 101
Dayton, OH 45414
Tel: (513)278-0714

Lyons Corporation
4615 W. Streetsboro Road
Richfield, OH 44286
Tel: (216)659-9224

OREGON

Vantage Corp.
7100 S.W. Hampton Street
Suite 205
Tigard, OR 97223
Tel: (503)620-3280

UTAH

Simpson Assocs.
7324 So. 1300 E.
Suite 350
Midvale, UT 84047
Tel: (801)566-3691

WASHINGTON

Vantage Corp.
300 120th Avenue N.E.
Bldg. 7, Suite 207
Bellevue, WA 98005
Tel: (206)455-3460

Canada

ALBERTA

Hi-Tech Sales, Ltd.
Box 115
339-10 Avenue, S.E.
Calgary, Alberta T2G 0W2
Tel: (403)229-6990

BRITISH COLUMBIA

Hi-Tech Sales, Ltd.
7510B Kingsway
Burnaby, B.C. V3N 3C2
Tel: (604)524-2131

MANITOBA

Hi-Tech Sales, Ltd.
102-902 St. James Street
Winnepeg, Manitoba R3G 3J7
Tel: (204)786-3343

ONTARIO

Bytewide Marketing, Inc.
7528 Bath Road
Mississauga, Ontario L4T 4C1
Tel: (416)675-1868

QUEBEC

Bytewide Marketing, Inc.
5020 Fairway Avenue
Suite 226
Lachine, Quebec H8T 1B8
Tel: (514)636-4121

RCA Solid State

DATABOOK