1. INTRODUCTION

1.1. SUMMARY

The Rockwell C29/C39 Microcontroller (MCU) is a complete 8-bit microcontroller fabricated on a single chip using a twin tub 1.0μ CMOS silicon gate process. The C29/C39 MCU complements an industry standard line of R6500 and R65C00 microprocessors, as well as R6500*/, R65CXX, and C19 microcomputers, and their compatible peripheral devices. The C29/C39 has a wide range of controller applications where high 8-bit performance, minimal chip count and low power consumption are required.

Note: The capabilities and architecture of the C29 and C39 MCU are similar and, in many cases, identical. Additional capabilities may also be added to new versions. The terms "MCU" or "C29/C39" are used with reference to features and capabilities common to the C29, C39 and any derivative microcontrollers described in this document. Terms like "C29" and "C39" are used with reference to features unique to a specific microcontroller.

Features common to the C29 and the C39 include an enhanced 6502 Central Processing Unit (CPU), 8k bytes of mask programmable read only memory (ROM), 1k bytes of random access memory (RAM), two 16-bit counter/timers, two 17-bit precision timing generators, an asynchronous/synchronous USART port, a 16-bit cyclic redundancy check (CRC), a 16-bit address/8-bit data expansion bus, 8 bank select registers for flexible memory banking control, and up to 40 general purpose input/output ports. Thirty two I/O lines can be assigned to special purpose functions under software control.

The C29 provides a 16-byte dual port RAM host interface which can emulate a 16450 UART or be used for general purpose scratch pad.

The C39 provides an enhanced 16-byte dual port RAM with 16-byte FIFO and DMA control which can emulate a 16450 or 16550A UART interface or be used for general purpose scratch pad. In addition, the C39 provides an ultra-low active Stop mode.

The innovative architecture and the demonstrated high performance of the R65C02 CPU, as well as instruction simplicity, result in system cost effectiveness and a wide range of computational power. These features make the C29/C39 a leading candidate for low power single chip microcontroller applications.

1.2. FEATURES

- Single-chip microcomputer
  - Enhanced R6502 CPU
  - 8k bytes internal read-only memory (ROM)
  - 1024 bytes internal random access memory (RAM)
  - Two 16-bit counter/timers
  - Two 17-bit precision time generators
  - Universal asynchronous/synchronous receiver transmitter (USART)
  - Host bus interface for 16450 or scratchpad RAM interface (C29)
  - Host bus for interface 16450/16550A or scratchpad RAM interface with 16-byte FIFO and DMA
  - Eight levels of prioritized, vectored interrupts
  - 10 MHz operation
  - Low power sleep mode
  - Ultra-low power stop mode (C39)
- Enhanced R6502 CPU
  - 12 new bit manipulation and branching instructions to shorten code and speed up execution
  - 21 new arithmetic processing instructions to optimize arithmetic processing
  - 10 new direct threaded code instructions to support high level languages that compile linked machine instructions
  - R6502 instruction compatible except "(indirect,X)" addressing mode changed to "(Indirect)" and "(Indirect),Y" addressing mode changed to "(Indirect),X"
- Internal Memory
  - Internal masked ROM: 8192 bytes
  - RAM: 1024 bytes
    - Page 0: 128 bytes
    - Pages 1-3: 768 bytes
    - Page 4: 128 bytes
  - Dual port RAM for general purpose host bus interface or for 16450 (C29) or 16450/16550 emulation (C39)
- General purpose input/output (GPIO), output (GPO), or input (GPI) lines
  - 28 GPIO lines with data latches and direction registers for 80-pin PQFP and 84-pin PLCC packages: Ports A, C, D (0-3), and E
  - 20 GPIO lines with data latches and direction registers for 68-pin PLCC package: Ports A, C, and D (0-3),
  - 8 output only lines with data latches: Port B
  - 4 input only lines with data latches: Port D (4-7)
  - 32 I/O lines can be assigned to special purpose functions under software control

- Two identical 16-bit programmable counter/timers with latches
  - Four modes: Interval Timer, Pulse Generation, Pulse Width Measurement, Event Counter
  - Selectable divide-by-32 prescaler
  - Timer interrupt can be vectored to either ROM or page 1 RAM
  - I/O port interface
- Two 17-bit precision time generators (PTGs) with latches
  - Increment/decrement capability with counter option (clear accumulator on overflow)
  - Interrupt enables
- Selectable Host Bus for 16450 or scratchpad RAM interface (C29)
  - 16450 interface (application software dependent)
    - 10 bytes for 16450 registers
    - 1 byte for dual port scratch pad RAM
    - 1 byte for dual port handshake
  - General purpose dual port RAM interface
    - 15 bytes for dual port scratch pad RAM
    - 1 byte for host control register
    - 1 byte for dual port handshake
- Selectable Host Bus for 16450/16550 or scratchpad RAM interface (C39)
  - 16450/16550 interface (application software dependent)
    - 6 bytes for 16450 registers
    - 7 bytes for dual port scratch pad RAM
    - 1 byte for dual port general purpose RAM
    - 1 byte for dual port handshake
    - 1 byte for receiver and transmitter FIFO interface (16 byte deep FIFO)
    - 2 bytes for FIFO status
    - 1 byte for GP FIFO status
    - DMA interface
  - General purpose dual port RAM interface
    - 13 bytes for dual port scratch pad RAM
    - 1 byte for dual port handshake
    - 1 byte for FIFO interface (16 byte deep FIFO)
    - 2 bytes for FIFO status
    - 1 byte for GP FIFO status
    - DMA interface
- USART Serial I/O
  - Common asynchronous/synchronous features
    - Full double buffering
    - Serial in and serial out individually enabled

Interrupt enables for receiver buffer full and transmitter buffer empty

Echo modes

Timer B or PTGA/PTGB timing

Speed recognition

- Asynchronous features

  5-, 6-, 7-, or 8-bit characters

  Even, odd, stuff or no parity bit generation and detection

  1, 1-1/2 or 2 stop bit generation with 3/4 or 7/8 stop bit control

  False start bit detection

  Interrupt enables

  Line break generation and detection

- Synchronous features

  Transmit data (TXD) serial input timing – internal, external TXCLK, or external TXREF

  Received data (RXD) serial output timing – internal or external RXCLK

  5-, 6-, 7-, or 8-bit characters

  Automatic word sync on first 1 to 0 transition

  Interrupt enables for serial input clock (TXCLK) and serial output clock (RXCLK)

- Expansion Bus

  - Built-in memory banking allows up to 512k bytes of external memory to be addressed
  - Eight Bank Select Registers independently control 8k-byte memory banks
  - Each BSR defines address translation (A13-A15), A16 control, and chip select (ES0-ES3)

- Eight levels of prioritized, vectored interrupts

  - RESP (highest priority)
  - Non-mask interrupt (NMI)
  - Six prioritized interrupt requests (IRQ1-IRQ6)

    Six IRQ ROM vectors

    Two software selectable Timer IRQ page 1 RAM vectors

- Internal 1 MHz to 10 MHz internal clock with crystal or clock input
  - Internal divide-by-2 (C29) or divide-by-1 (C39) input frequency divider
  - 2 MHz to 20 MHz (C29) or 1 MHz to 10 MHz (C39) input frequency
  - Sleep (idle) mode, software enabled
    Low power dissipation, normal operation resumption within 2 clock cycles
    Awakened by a low on NMIP
    Awakened by a low detected on PA0, on PA2, or on PD4 and PD5, software enabled
    Awakened by a low detected on PD4 or on PD5, software enabled (C39)
  - Stop mode, software enabled (C39)
    Ultra-low power dissipation, normal operation resumption within 12 clock cycles
    Awakened by a low on NMIP
    Awakened by a low detected on PA0, on PA2, or on PD4 and PD5, software enabled
    Awakened by a low detected on PD4 or on PD5, software enabled

Available in plastic leaded chip carrier (PLCC) or low profile plastic quad flat pack (PQFP) packages
  - 68-pin PLCC
  - 84-pin PLCC
  - 80-pin PQFP

- Emulator Device
  - 84-pin PLCC
- +5 V 5% power

1.3. C19/C29/C39 FAMILY COMPARISON

Feature	C19	C29	C39	Units
RAM	512	1K	1K	Bytes
ROM	16K	8K	8K	Bytes
Serial	16C450	16C450	16C450/16C550	
GP Scratchpad RAM	15	15	13	Bytes
16-byte FIFO	No	No	Yes	
DMA access	No	No	Yes	
CRC	--	1(16)	1(16)	
Expansion Bus	64K	64K+	64K+	
Max Speed	8	10	10	MHz
BRK Vector	IRQ6	IRQ6	NMI	
Low power mode	Sleep	Sleep	Sleep/Stop	

1.4. DEVELOPMENT SUPPORT

1.4.1. AMC EL Development System

The AMC EL Development System, available from Applied Microsystems Corporation, provides extensive hardware and software tools for application software development and debugging. Major features include:

- Support for C19, C29, C39, and FAXENGINE processors
- Hosts on 386 PC or compatible (DOS 5.0 or later)
- Runs in real time at speeds to 12 MHz.
- Language tools include C and ANSI compilers, C29 Assembler, Disassembler, Linker, Loader, and Librarian.
- Source level debugger
- Trace memory (optional)
- Target diagnostics
- RS-232C serial host interface at 9600-115.2K baud
- Banked memory support
- Access or violation, hardware execution breakpoints and event-system breaks
- Advanced break/event system
- Optional overlay memory
- Overlay and target memory

Additional information is available from:

Applied Microsystems Corporation
5020 148th Ave. N.E.
P.O. Box 97002
Redmond, WA 98073-9702

(206) 882-2000
1-800-426-3925
TRT TELEX 185196
FAX (206) 883-3049

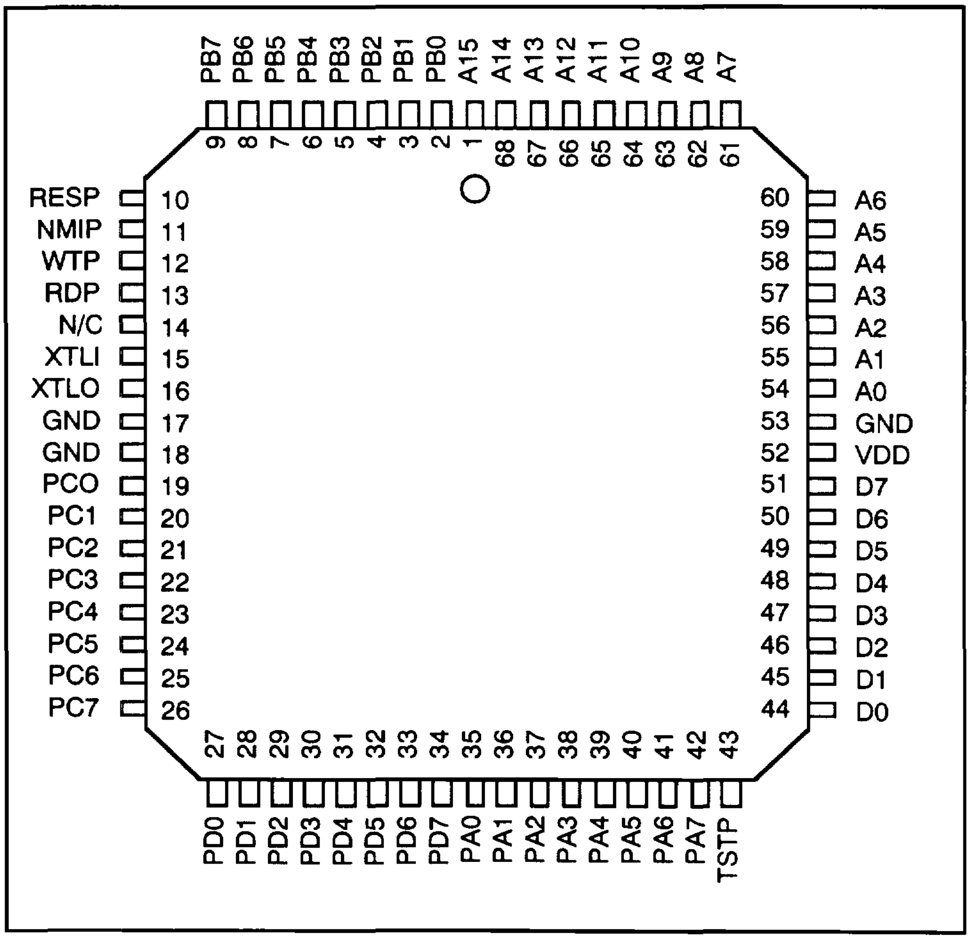
2. INTERFACE DESCRIPTION

2.1. PIN ASSIGNMENTS

The pin assignments for the 68-pin PLCC, the 84-pin PLCC, and the 80-pin PQFP packages are shown in Figure 2-1. The I/O signals are shown in Figure 2-2 along with the major interfacing MPU functions.

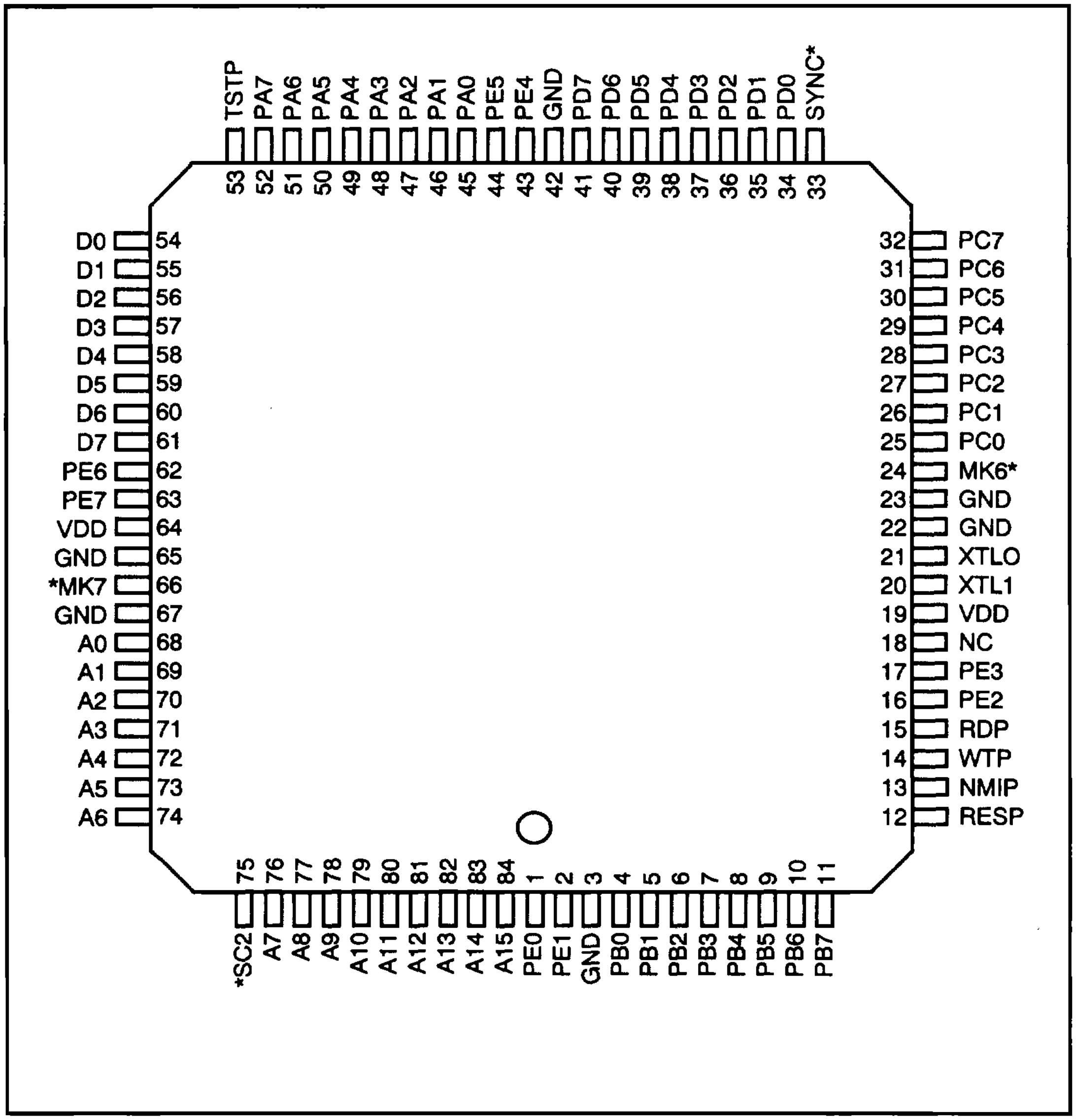
2.2. I/O PIN SIGNALS

The I/O pin signals are defined in Table 2-1.



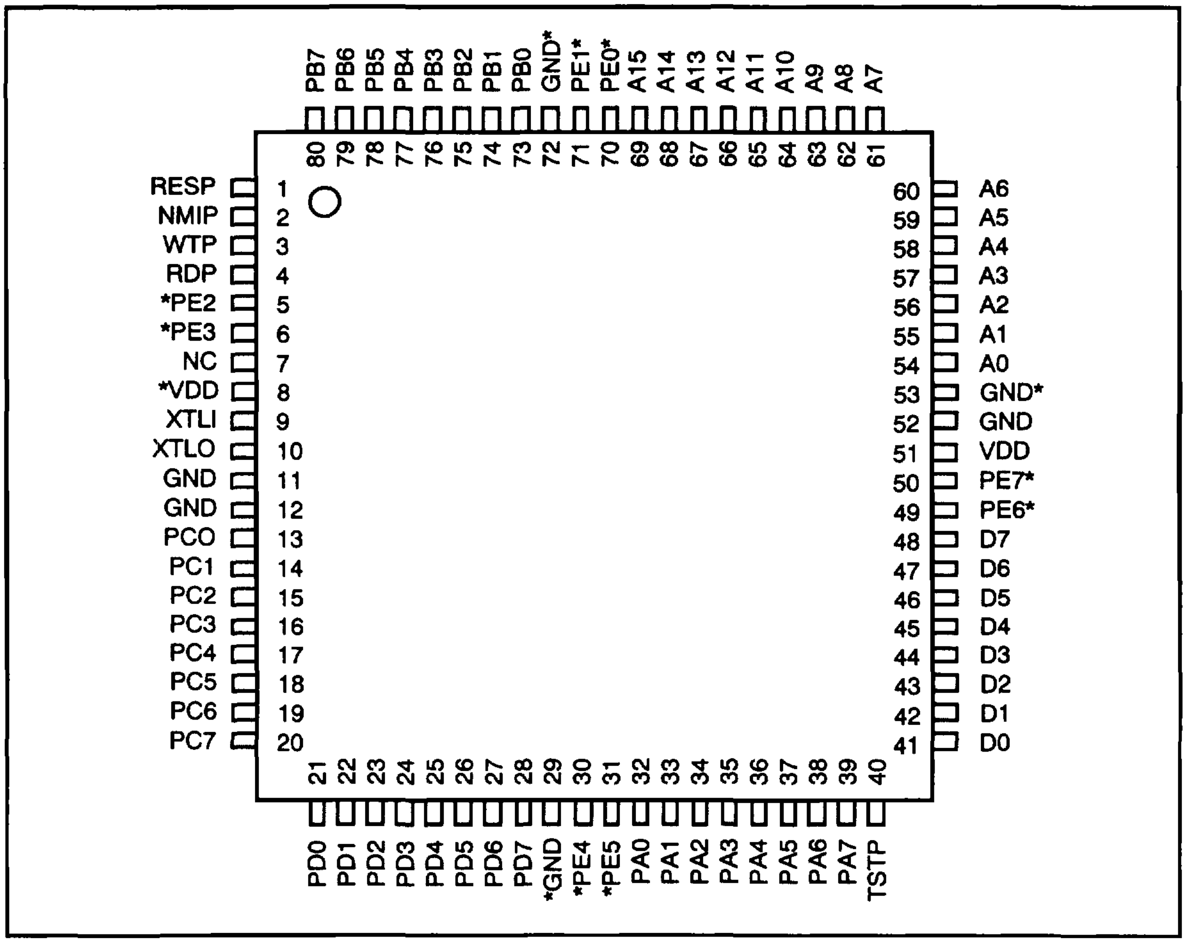
NOTE: Pin 14 is SYNC on C29; NC on C39.

Figure 2-1a. Pin Assignments - 68-Pin PLCC



NOTE: SYNC, SC2, MK6 and MK7 are only available in the emulator package.

Figure 2-1b. Pin Assignments - 84-Pin PLCC



NOTE: * Indicates pins not bonded in the 68 pin PLCC package.

Figure 2-1c. Pin Assignments - 80-Pin PQFP

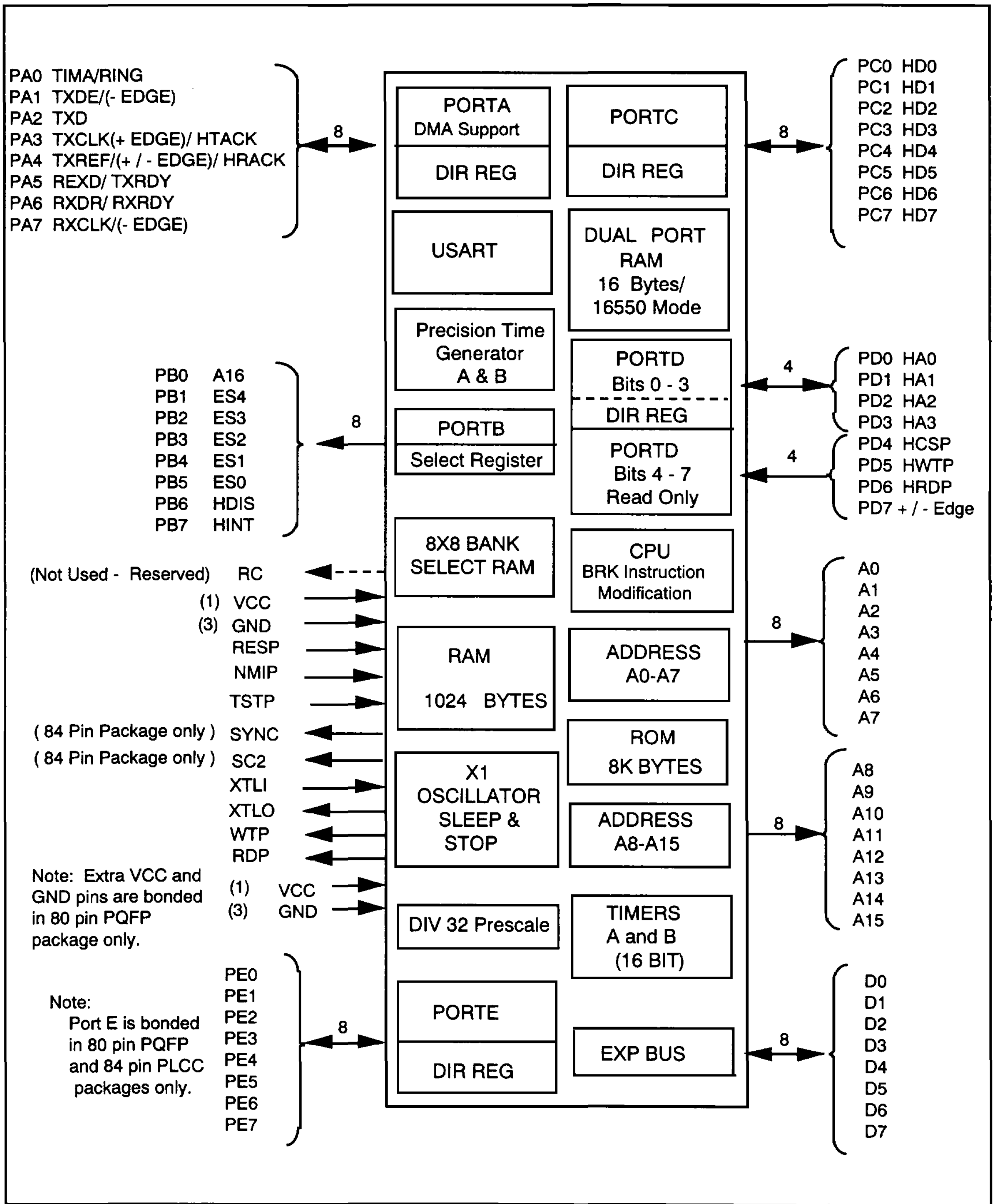


Figure 2-2. Internal Functions and I/O Signals

Table 2-1. Interface Signal Description

Symbol	I/O	Name / Function
PA0-PA7	I/O	**General Purpose 8-Bit I/O Port A.** All pins can be assigned special functions under software control. The Port A Direction Register (PAD) must be set appropriately for all pins in both general and special use. PA1, PA3, PA4 and PA7 have edge detect circuitry that remains active regardless of data direction.
TIMA (PA0)	I/O	**Timer A I/O.** An input in Timer A Event Counter or Pulse Width Measurement mode and an output in Timer A Pulse Generation mode.
RING (PA0)	I/O	**Ring.** An unclocked input whose positive level is used to clear the low power mode. Ring is enabled by LPR5.
CTSP (PA0)	I	**Clear To Send.** The negative edge of an external CTSP signal can be used to initialize the USART TXD synchronous mode word counter (SM1 = 1).
TXDE (PA1)	O	**Serial Input Passthrough.** PA2 input is connected to the PA1 output when the serial passthrough is selected (SF7 = 1).
Edge (PA1)	I/O	**PA1 Negative Edge Detect.** The PA1 edge detect flag (EI7) is set on each detected edge and is cleared by writing a zero to register bit CI7. When the PA1 edge detect flag is set (EI7 = 1), IRQ5 will be asserted if its enable is set (EI4 = 1).
TXD (PA2)	I	**TXD Serial Input.** PA2 input is connected to the USART as the serial input stream when USART TXD mode is selected (SM6 = 1).
TXCLK (PA3)	I/O	**TXCLK Clock.** PA3 is internally connected to the serial input clock when synchronous USART operation is selected (SM4 = 1). TXCLK can be an external signal, an internal signal, or can be internally connected to TXREF (PA4). TXD is clocked on the rising edge of TXCLK.
TX Edge (PA3/PA2)	I/O	**PA3/PA2 Positive Edge Detect.** The PA3/PA2 edge detect flag (SI6) is set on each detected edge and is cleared by writing a zero to register bit CI3. When the PA3/PA2 edge detect flag is set (SI6 = 1), IRQ4 will be asserted if its enable is set (SI4 = 1).
HTACKP (PA3)	I	**Host Transmit Acknowledge.** PA3 is an is an active low transmit acknowledge input in the DMA from the host bus acknowledging that the DMA controller received the Transmit Ready (TXRDY) data transfer request (HCR2 = 1). Non-operational in the 16450 mode. (C39 only.)
TXREF (PA4)	I	**External TXD Reference Clock.** PA4 input is connected internally to PA3 output when synchronous USART operation is selected (SM4 = 1) and TXREF is selected as the TXCLK source (SM2 = 1).
or Edge (PA4)	I/O	**PA4 Positive/Negative Edge Detect.** The PA4 edge detect flag (EI6) is set on each detected edge and is cleared by writing a zero to register bit CI6. When the PA4 edge detect flag is set (EI6 = 1), IRQ2 will be asserted if its enable is set (EI3 = 1). PA4 will detect a negative (EI1 = 0) or a positive (EI1 = 1) edge.
RLSDP (PA4)	O	**Receiver Line Signal Detect.** The negative edge of an external RLSDP signal can be used to initialize the USART RXD synchronous mode word counter (SMR1 = 1).

Table 2-1. Interface Signal Description

Symbol	I/O	Name / Function
HRACKP (PA4)	I	**Host Receive Acknowledge.** PA4 is an is an active low receive acknowledge input from the host bus acknowledging that the DMA controller received the Receive Ready (RXRDY) data transfer request (HCR2 = 1). Non-operational in the 16450 mode. (C39 only.)
REXD (PA5)	I	**Serial Output Passthrough.** PA5 input is internally connected to the PA6 output when serial out passthrough mode is selected (SM7 = 1, SF5 = 0, and SF6 = 1).
TXRDY (PA5)	O	**Transmit Ready.** PA5 is an active high transmit ready output in the host 16550 DMA TX FIFO write mode and the 16450 mode (HCR2 = 1). When asserted, TXRDY indicates that the TX FIFO is not full, i.e., can accept data to be transmitted. Non-operational in the GP host mode. (C39 only.)
RXD (PA6)	O	**RXD Serial Output.** PA6 is connected as the USART serial output stream (SFR7 = 1). When loopback is selected (SF5 = 1) the PA2 signal is internally connected to the PA6 output. PA6 is also modified by the serial output passthrough mode (SF6 = 1).
RXRDY (PA6)	O	**Receive Ready.** PA6 is an active high receive ready output in the host 16550 DMA RX FIFO read mode and the 16450 mode (HCR2 = 1). When asserted, RXRDY indicates that the RX FIFO is not empty, i.e., has received data ready for transfer. Non-operational in the GP host mode. (C39 only.)
RXCLK (PA7)	I/O	**RXD Serial Output Clock.** PA7 output is internally connected to the USART in the synchronous mode (SM7 = 1 and SM4 = 1). RXCLK can be an external input signal or can be generated internally and become an output signal. Serial out is clocked on the negative edge of RXCLK.
Edge (PA7)	I/O	**PA7 Negative Edge Detect.** The PA7 edge detect flag (SI5) is set on each detected edge and is cleared by writing a zero to register bit CI4. When the PA7 edge detect flag is set (SI5 = 1), IRQ6 will be asserted if its enable is set (SI3 = 1).

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
PB0-PB7	O	**General Purpose 8-Bit Output Port B.** All pins can be assigned special functions under software control. The Port B Selection Register (PBS) must be set appropriately for all pins in both general and special use. All Port B outputs float during reset active low.
A16 (PB0)	O	**A16.** When PBS0 = 0, the PB0 pin becomes the A16 address function from the selected or active (i) Banking RAM register bit 4 (BRi4).
ES4 (PB1)	O	**ES4.** When PBS1 = 0, the PB1 pin becomes the ES4 chip select signal. ES4 is active low from addresses $0600 to $07FF.
ES3 (PB2)	O	**ES3.** When PBS2 = 0, the PB2 pin becomes the ES3 chip select signal. ES3 is controlled by bit 7 of the selected or active (i) Banking RAM register (BRi7).
ES2 (PB3)	O	**ES2.** When PBS3 = 0, the PB3 pin becomes the ES2 chip select signal. ES2 is controlled by bit 6 of the selected or active (i) Banking RAM register (BRi6).
ES1 (PB4)	O	**ES1.** When PBS4 = 0, the PB4 pin becomes the ES1 chip select signal. ES1 is controlled by bit 5 of the selected or active (i) Banking RAM register (BRi5).
ES0 (PB5)	O	**ES0.** When PBS5 = 0, the PB5 pin becomes the ES0 chip select signal. ES0 is controlled by bit 4 of the selected or active (i) Banking RAM register (BRi4).
HDIS (PB6)	O	**Host Bus Driver Disable.** Active low output asserted when the host is selected (HCR2 = 1) and is reading data from the MCU host data bus. HDIS can be used to control an external transceiver driver. (PBS6 = 0)
HINT (PB7)	O	**Host Bus Interrupt.** Active high output asserted in both the general purpose (GP) host interface (HC2 = 1 and HC1 = 0) or the 16450 host interface (HC2 = 1 and HC1 = 1) under various conditions. (PBS7 = 0)
PC0-PC7	I/O	**General Purpose 8-Bit I/O Port C.** All pins can be assigned in a group to host bus data lines by a software option. The Port C Direction Register (PCD) must be set appropriately for all pins.
HD0-HD7 (PC0-PC7)	I/O	**Host Bus Data Lines.** PC0-PC7 are dedicated to the host bus interface bidirectional data lines HD0-HD7, respectively, as a software option (HC2 = 1). The Port C direction register must be set to the output mode when the host bus software option is selected.

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
PD0-PD3 PD4-PD7	I/O I	**General Purpose 4-Bit I/O and 4-Bit Input Port D.** PD0-PD3 are general purpose I/O pins while PD4-PD7 are input only. PD0-PD3 output latch is controlled by writing bits 0-3 at address $0003, while their direction control is contained in bits 4-7, respectively. PD0- PD6 can be assigned in a group to host bus address and control lines by a software option (HCR2 = 1).
HA0-HA3 (PD0-PD3)	I	**Host Bus Address Lines.** PD0-PD3 are dedicated to the host bus interface as address lines HA0-HA3, respectively, as a software option (HC2 = 1, HC1 = 1). PD3 remains a GP pin in the 16450 mode (HC2 = 1, HC1 = 0).
HCSP (PD4)	I	**Host Bus Chip Select.** PD4 is dedicated to the host bus interface as the active low chip select input as a software option (HC2 = 1).
HWTP (PD5)	I	**Host Bus Write.** PD5 is dedicated to the host bus interface as an active low write control input as a software option (HC2 = 1).
HRDP (PD6)	I	**Host Bus Read.** PD6 is dedicated to the host bus interface as an active low read control input as a software option (HC2 = 1).
↑ or ↓ Edge (PD7)	I	**PD7 Positive/Negative Edge Detect.** The PD7 edge detect flag (EI5) is set on each detected edge and is cleared by writing a zero to register bit CI5. When the PD7 edge detect flag is set (EI5 = 1), IRQ1 will be asserted if its enable is set (EI2 = 1). PD7 will detect a negative (EI0 = 0) or a positive (EI0 = 1) edge.
PE0-PE7	I/O	**General Purpose 8-Bit I/O Port E.** The Port E Direction Register (PED) must be set appropriately for all pins. Port E is only available in the 80-pin PQFP and 84-pin PLCC packages.

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
A0-A12	O	**A0-A12 .** Address lines for external memory bus. These lines float during reset active.
A13-A15	O	**A13-A15 .** Address lines for external memory bus. These lines float during reset active. Address lines A13 - A15 are controlled by bits 0 - 2 (m), respectively, of the active or selected (i) Banking RAM register (BRim).
D0-D7	I/O	**Expansion Bus Data .** D0-D7 provide an 8-bit bi-directional data bus for interfacing to external memories. D0-D7 float during reset active.
WTP	O	**Expansion Bus Write.** Active low write strobe for the expansion bus. When WTP is asserted, data on the expansion data bus is to be written into the selected peripheral device. WTP remains high during MCU reset active.
RDP	O	**Expansion Bus Read.** Active low read strobe for the expansion bus. When RDP is asserted, data is read from the selected peripheral onto the expansion data bus. RDP remains high during MCU reset active.
RESP	I	**Reset.** Active low input resets all MCU circuits and registers to their initial state. MCU operation resumes when the RESP input goes high; program execution starts at the location defined by the reset address vector.
NMIP	I	**Non-Maskable Interrupt.** Non- Maskable negative edge sensitive interrupt input. Interrupts program execution upon completion of current instruction and jumps to interrupt service subroutine starting at location defined by the NMI address vector.
LPWU NMIP	I	**Low Power Wake Up - NMIP.** When the MCU is operating in the low power Sleep mode, a low level on the NMIP pin will cause normal operation to resume. When the C39 is operating in the low power Stop mode, a low level on the NMIP pin for at least 12 clock cycles will cause normal operation to resume.
LPWU Ring (PA0)	I	**Low Power Wake Up - Ring .** When the C39 is operating in the low power mode, a high level on PA0 will cause normal operation to resume if the PA0 enable term is set (LPR5 = 1).
LPWU HBW (PD4 + PD5)P	I	**Low Power Wake Up - Host Bus Write.** When the C39 is operating in the low power mode, a low level on both PD4 and PD5 will cause normal operation to resume if the host write enable term is set (LPR4 = 1).
LPWU TXD (PA2)P	I	**Low Power Wake Up - TXD (USART Start Bit).** When the C39 is operating in the low power mode, a low level on PA2 will cause normal operation to resume if the USART start bit enable term is set (LPR3 = 1).
LPWU DTR (PD4)P	I	**Low Power Wake Up - DTR .** When the C39 is operating in the low power mode a low level on PD4 will cause normal operation to resume if the host write enable term is set (LPR2 = 1).
LPWU AL (PD5)P	I	**Low Power Wake Up - AL.** When the C39 is operating in the low power mode a low level on PD5 will cause normal operation to resume if the host write enable term is set (LPR1 = 1).

Table 2-1. Interface Signal Description (Cont'd)

Symbol	I/O	Name / Function
TSTP	I	**Emulator Mode.** The TSTP is an input with an internal pull-up. TSTP high places the MCU in the normal operating mode. 1. Internal ROM is enabled. 2. RDP and WTP reflect CPU activity. 3. Internal CPU read activity on pages 0, 1, 2, 3, or 4 (internal RAM and registers) do not appear on the expansion bus. TSTP low places the MCU in a special emulation mode. 1. Internal ROM is disabled and all ROM fetches are transferred to the expansion bus. 2. Internal bus activity on pages 0, 1, 2, 3, or 4 now impact D0-D7. An internal read from pages 0-3 cause the internal data to appear on D0-D7.
SYNC	O	**Sync.** When sync is asserted high it denotes that the current cycle is an op code fetch for the next instruction (Emulator package only.)
SC2	O	**SC2.** SC2 is an output operating at the crystal frequency or slower depending upon the external memory selected and is in phase with the internal C2 clock (Emulator package only.)
XTLI	I	**Crystal Oscillator Input Pin.** Input connection from crystal or external clock circuit.
XTLO	O	**Crystal Return.** Oscillator output connection to an external crystal. Open when the XTLI input is connected to an external clock.
VDD	I	**Power.** +5 VDC.
GND	I	**Ground.** Signal and power ground.

3. SYSTEM ARCHITECTURE

3.1. OVERVIEW AND MEMORY MAPS

3.1.1. Block Diagrams

Block diagrams of the C29 and C39 are shown in Figure 3-1a and 3-1b, respectively.

3.1.2. Top Level Memory Map

The top level memory map in Figures 3-2 shows major boundaries between I/O, internal ROM, internal RAM, and external addresses. The individual registers are identified in Table 3-1.

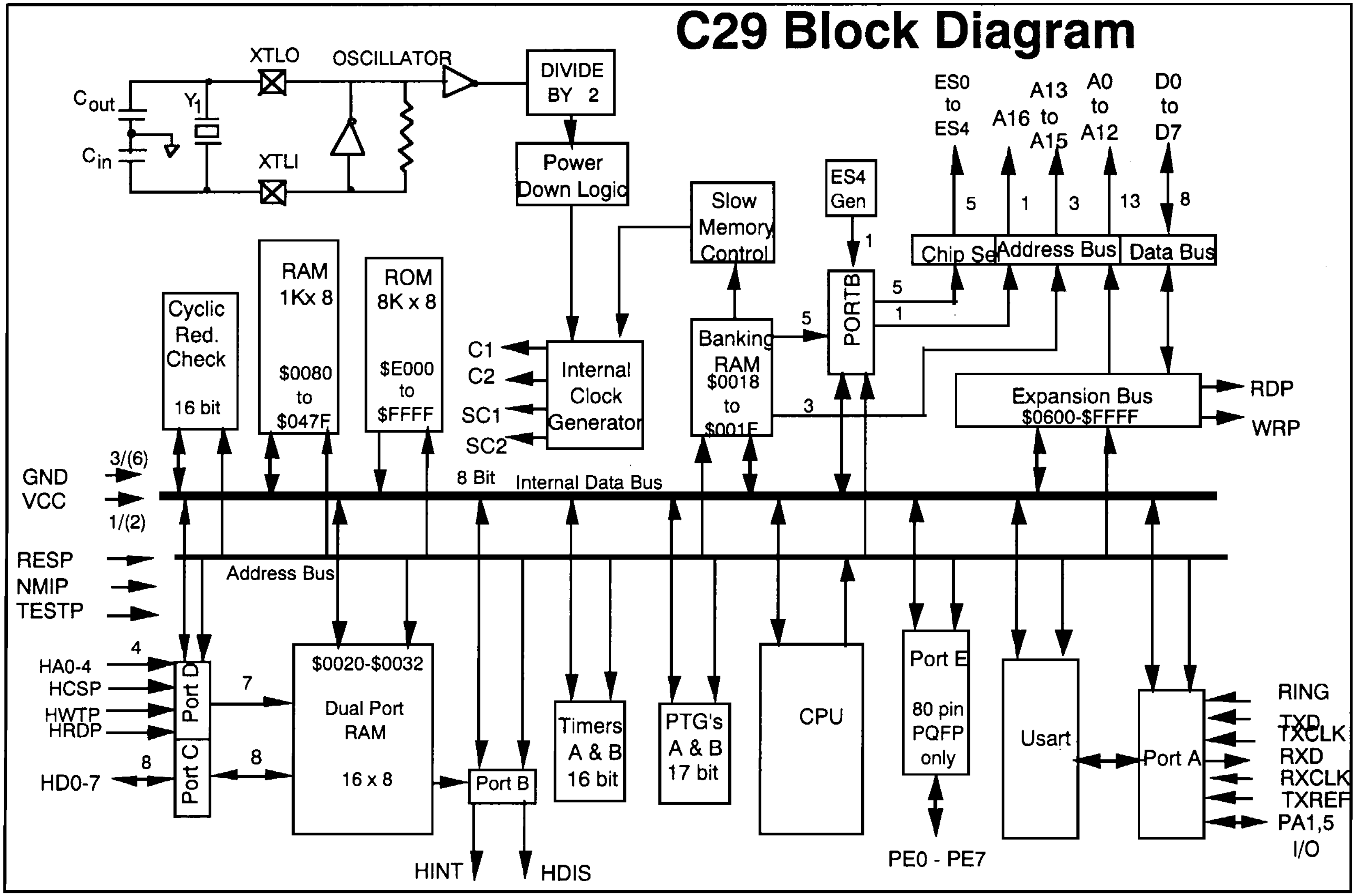


Figure 3-1a. C29 Block Diagram

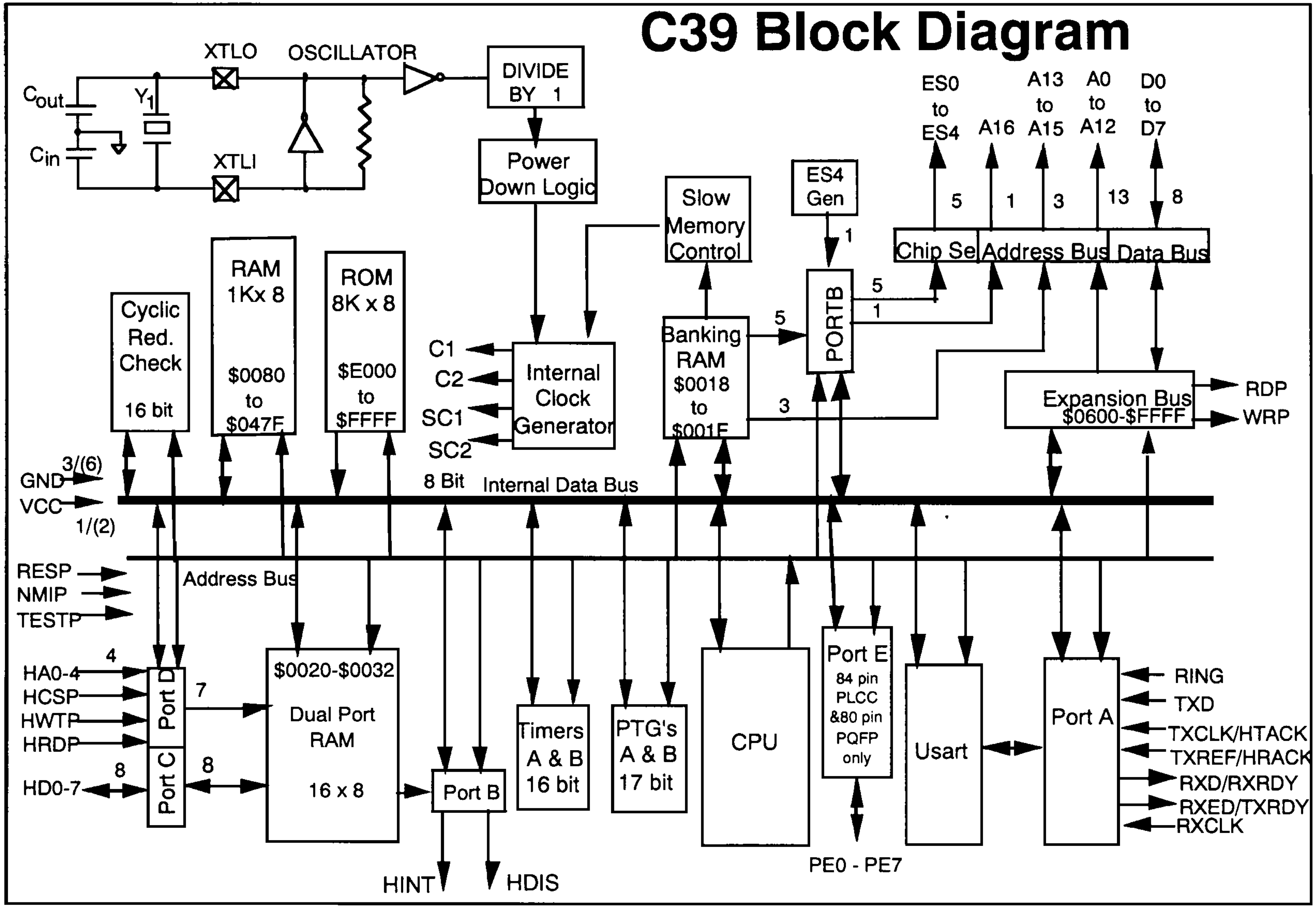


Figure 3-1b. C39 Block Diagram

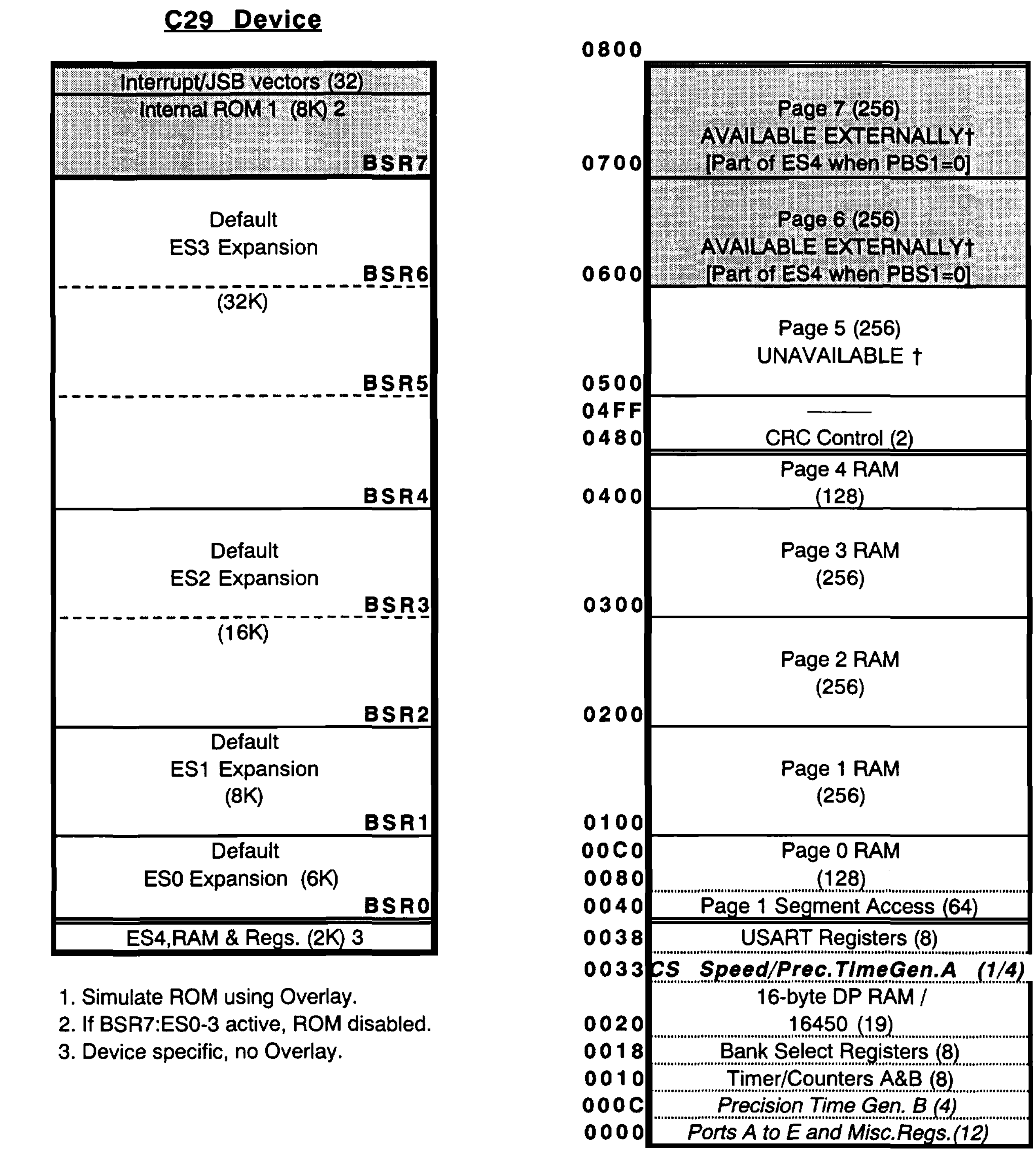
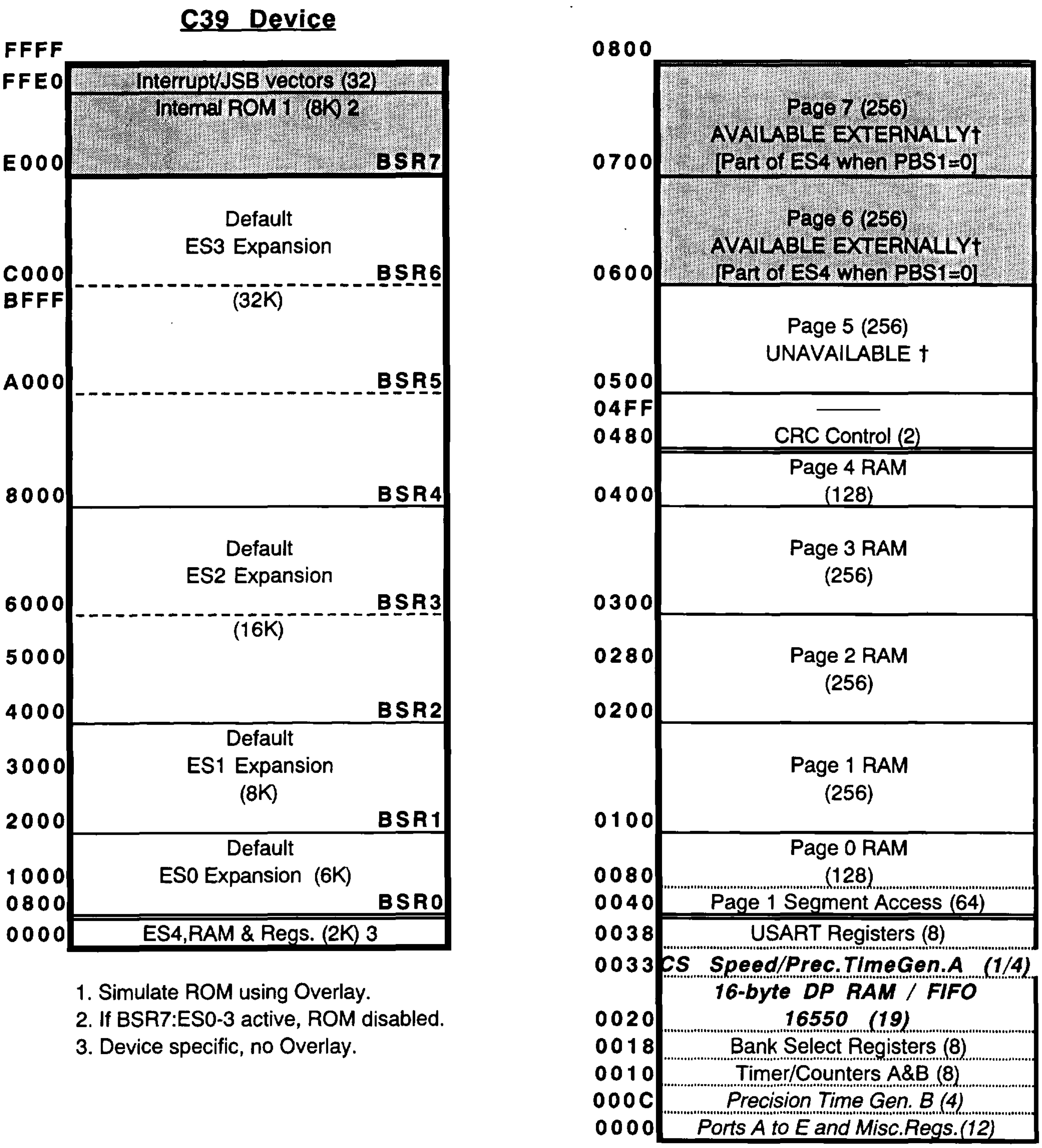


Figure 3-2a. C29 Memory Map - Overview



1. Simulate ROM using Overlay.
2. If BSR7:ES0-3 active, ROM disabled.
3. Device specific, no Overlay.

Figure 3-2b. C39 Memory Map - Overview

Table 3-1a. Memory Map 0-001Fh

Address	Read	Write
0000	Port A	Port A
0001	Port B (Output Only)	Port B (Output Only)
0002	Port C	Port C
0003	Port D	Port D (0-3), Direction (4-7)
0004	--	Port A Direction
0005	Port B Select	Port B Select
0006	--	Port C Direction
0007	Port E	Port E
0008	Mask Option Register	Port E Direction
0009	Low Power Register (LPR)	Low Power Register (LPR)
000A	External Interrupt Register	External Interrupt Register
000B	Clear External Interrupt	Clear External Interrupt
000C	PTG B Mode	PTG B Mode
000D	PBB	PBB
000E	PBUL	PBUL, PBB to PBLL
000F	PBUL, Clear Flag	PBUL,PBB to PBLL, Download, Clear Flag
0010	Timer A Mode	Timer A Mode
0011	TALC, TAUC to TAS	TALL
0012	TAS	TAUL
0013	TAS, Clear Flag	TAUL, Download, Clear Flag
0014	Timer B Mode	Timer B Mode
0015	TBLC, TBUC to TBS	TBLL
0016	TBS	TBUL
0017	TBS, Clear Flag	TBUL, Download , Clear Flag
0018	Bank 0	Bank 0
0019	Bank 1	Bank 1
001A	Bank 2	Bank 2
001B	Bank 3	Bank 3
001C	Bank 4	Bank 4
001D	Bank 5	Bank 5
001E	Bank 6	Bank 6
001F	Bank 7	Bank 7

Table 3-1b. Memory Map - 0020h-0032h - Host General Purpose Mode

	C29 Only		C39 Only	
Address	**Read**	**Write**	**Read**	**Write**
0020	SP RAM 0	SP RAM 0	TX FIFO Buffer	RX FIFO Buffer
0021	SP RAM 1	SP RAM 1	SP RAM 1	SP RAM 1
0022	SP RAM 2	SP RAM 2	SP RAM 2	SP RAM 2
0023	SP RAM 3	SP RAM 3	SP RAM 3	SP RAM 3
0024	SP RAM 4	SP RAM 4	SP RAM 4	SP RAM 4
0025	SP RAM 5	SP RAM 5	SP RAM 5	SP RAM 5
0026	SP RAM 6	SP RAM 6	SP RAM 6	SP RAM 6
0027	SP RAM 7	SP RAM 7	SP RAM 7	SP RAM 7
0028	SP RAM 8	SP RAM 8	SP RAM 8	SP RAM 8
0029	SP RAM 9	SP RAM 9	SP RAM 9	SP RAM 9
002A	SP RAM A	SP RAM A	SP RAM A	SP RAM A
002B	SP RAM B	SP RAM B	SP RAM B	SP RAM B
002C	SP RAM C	SP RAM C	SP RAM C	SP RAM C
002D	SP RAM D	SP RAM D	SP RAM D	SP RAM D
002E	SP RAM E	SP RAM E	SP RAM E	SP RAM E
002F	Host Handshake Register (HHR)	HosH Handshake Register (HHR)	Host Handshake Register (HHR)	HosH Handshake Register (HHR)
0030	--	--	FIFO Status Register (FSR)	FIFO Status Register (FSR)
0031	--	--	FIFO Interrupt Enable Register (FIER)	FIFO Interrupt Enable Register (FIER)
0032	Host Control Register (HCR)	Host Control Register (HCR)	Host Control Register (HCR)	Host Control Register (HCR)

Table 3-1c. Memory Map - 0020h-0032h - Host 16450 (C29) and 16450/16550A (C39) Emulation Mode

	C29 Only (16450)		C39 Only (16450/16550)	
Address	**Read**	**Write**	**Read**	**Write**
0020	RX Buffer	RX Buffer	TX FIFO Buffer	RX FIFO Buffer
0021	TX Buffer	--	Line Status Register (LSR)	Line Status Register (LSR)
0022	SP RAM 2	SP RAM 2	Modem Status Register MSR)	Modem Status Register (MSR)
0023	Line Control Register (LCR)	*	Line Control Register (LCR)	*
0024	Modem Control Register (MCR)	*	Modem Control Register (MCR)	*
0025	SP RAM 5	SP RAM 5	FIFO Control Register (FCR)	FIFO Control Register (FCR)
0026	SP RAM 6	SP RAM 6	SP RAM 6	SP RAM 6
0027	SP RAM 7	*	Scratch Register (SCR)	Scratch Register (SCR)
0028	Divisor Latch LSB	*	Divisor Latch LSB	*
0029	Divisor Latch MSB	*	Divisor Latch MSB	*
002A	SP RAM A	SP RAM A	SP RAM A	SP RAM A
002B	SP RAM B	SP RAM B	SP RAM B	SP RAM B
002C	SP RAM C	SP RAM C	SP RAM C	SP RAM C
002D	SP RAM D	SP RAM D	SP RAM D	SP RAM D
002E	SP RAM E	SP RAM E	GP DP FIFO Status (GPFS)	GP DP FIFO Status (GPFS)
002F	Host Handshake Register (HHR)	HosH Handshake Register (HHR)	Host Handshake Register (HHR)	HosH Handshake Register (HHR)
0030	Line Status Register (LSR)	Line Status Register (LSR)	FIFO Status Register (FSR)	FIFO Status Register (FSR)
0031	Modem Status Register (MSR)	Modem Status Register (MSR)	FIFO Interrupt Enable Register (FIER)	FIFO Interrupt Enable Register (FIER)
0032	Host Control Register (HCR)	Host Control Register (HCR)	Host Control Register (HCR)	Host Control Register (HCR)

Table 3-1d. Memory Map - 0033h-003Fh

Address	Read	Write
0033	Chip Select Fast / Slow	Chip Select Fast / Slow
0034	PTG A Mode	PTG A Mode
0035	PAB	PAB
0036	PAUL	PAUL, PAB to PALL
0037	PAUL, Clear Flag	PAUL,PAB to PALL, Download, Clear Flag
0038	Serial In Buffer (SIB)	Serial Out Buffer (SOB)
0039	Serial Interrupt Enable (SIR)	Serial Interrupt Enable (SIR)
003A	Serial Mode Register (SMR)	Serial Mode Register (SMR)
003B	Serial Line Control Register (SLC)R	Serial Line Control Register (SLCR)
003C	Serial Status Register (SSR)	Serial Status Register (SSR)
003D	Serial Form Register (SFR)	Serial Form Register (SFR)
003E	--	SOUT (RXD) Divider Latch (SODL)
003F	--	SIN (TXD) Divider Latch (SIDL)

Table 3-1e. Memory Map - 0040h-1FFFh

Address	Read	Write
0040 . . 007F	64 BYTES PAGE 1 SEGMENT ADDRESS	64 BYTES PAGE 1 SEGMENT ADDRESS
0080 . . 00FF	128 BYTES PAGE 0 RAM	128 BYTES PAGE 0 RAM
0100 . . 01FF	256 BYTES PAGE 1 RAM	256 BYTES PAGE 1 RAM
0200 . . 02FF	256 BYTES PAGE 2 RAM	256 BYTES PAGE 2 RAM
0300 . . 03FF	256 BYTES PAGE 3 RAM	256 BYTES PAGE 3 RAM
0400 . . 047F	128 BYTES PAGE 4 RAM	128 BYTES PAGE 4 RAM
0480 0481	CRC-L CRC-H	CRC INPUT BUFFER INITIALIZE CRC
0600 . . 07FF	ES4 Active, PBS1 = 0	ES4 Inactive, PBS1 =1
0800 . . 1FFF	Bank Select 0 (6K PBS1 = 0, or 6.5K PBS1 = 1)	

3.1.3. I/O Register Bit Assignments

The individual I/O signal and data bits are identified in Table 3-2.

Table 3-2a. Register Bit Assignments - 0000h - 0017h

Addr.	Function	Bit 7	6	5	4	3	2	1	0
0000	Port A Data (0-7; I/O)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
0001	Port B Data (0-7; Output Only)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
0002	Port C Data (0-7; I/O)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
0003	Port D Data (0-3; I/O), Port D Direction (4-7)	PDD3	PDD2	PDD1	PDD0	PD3	PD2	PD1	PD0
0004	Port C Direction (0-7)	PAD7	PAD6	PAD5	PAD4	PAD3	PAD2	PAD1	PAD0
0005	Port B Select (0-7)	PBS7	PBS6	PBS5	PBS4	PBS3	PBS2	PBS1	PBS0
0006	Port C Direction (0-7)	PCD7	PCD6	PCD5	PCD4	PCD3	PCD2	PCD1	PCD0
0007	Port E Data (0-7)	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
0008	Mask Option Register (MSR)	Option 2	Option 1	Not Used					
0009	Low Power Register (LPR)	Low Power Mode Enable	Low Power Mode Select	Wake up Enable PA0 (Ring)	Wake up Enable PD4 (Wrt) PD5 (CS)	Wake up Enable PA2 (TXD)	Wake up Enable PD4 (DTR)	Wake up Enable PD5 (AL)	Not Used
000A	External Interrupt Register (EIR)	External Interrupt Flag PA1	External Interrupt Flag PA4	External Interrupt Flag PD7	External Interrupt Enable PA1	External Interrupt Enable PA4	External Interrupt Enable PD7	Edge Detect Polarity PA4	Edge Detect Polarity PD7
000B	Clear Interrupt Register (CIR)	Clear Interrupt Flag PA1	Clear Interrupt Flag PA4	Clear Interrupt Flag PD7	Clear Interrupt Flag PA7	Clear Interrupt Flag PA3	ES4 Fast	RAM Segment Select Bit 1 (CI1)	RAM Segment Select Bit 0 (CI0)
000C	Precision Time Generator B (PTG B) Mode (PBM)	PTG B Interrupt Flag	PTG B Interrupt Enable	Not Used					PTG B Timer Mode
0010	Timer A Mode (TAM)	Timer A Interrupt Flag	Timer A Interrupt Enable	Timer A Vector Select	Not Used		Timer A Div by 32 Prescale	Timer A Mode Bit 1 (TAM1)	Timer A Mode Bit 0 (TAM0)
0011	Timer A Lower Latch	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0012	Timer A Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8
0013	Timer A Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8
0014	Timer B Mode (TBM)	Timer B Interrupt Flag	Timer B Interrupt Enable	Timer B Vector Select	Not Used		Timer B Div by 32 Prescale	0	0
0015	Timer B Latch Low	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0016	Timer B Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8
0017	Timer B Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8

Table 3-2b. Register Bit Assignments - 0018h - 001Fh

Addr.	Function	Bit 7	6	5	4	3	2	1	0
0018	Bank Select Register 0 (BSR0)	ES3 (0)	ES2 (0)	ES1 (0)	ES0 (0)	A16 (0)	A15 (0)	A14 (0)	A13 (0)
0019	Bank Select Register 1 (BSR1)	ES3 (1)	ES2 (1)	ES1 (1)	ES0 (1)	A16 (1)	A15 (1)	A14 (1)	A13 (1)
001A	Bank Select Register 2 (BSR2)	ES3 (2)	ES2 (2)	ES1 (2)	ES0 (2)	A16 (2)	A15 (2)	A14 (2)	A13 (2)
001B	Bank Select Register 3 (BSR3)	ES3 (3)	ES2 (3)	ES1 (3)	ES0 (3)	A16 (3)	A15 (3)	A14 (3)	A13 (3)
001C	Bank Select Register 4 (BSR4)	ES3 (4)	ES2 (4)	ES1 (4)	ES0 (4)	A16 (4)	A15 (4)	A14 (4)	A13 (4)
001D	Bank Select Register 5 (BSR5)	ES3 (5)	ES2 (5)	ES1 (5)	ES0 (5)	A16 (5)	A15 (5)	A14 (5)	A13 (5)
001E	Bank Select Register 6 (BSR6)	ES3 (6)	ES2 (6)	ES1 (6)	ES0 (6)	A16 (6)	A15 (6)	A14 (6)	A13 (6)
001F	Bank Select Register 7 (BSR7)	ES3 (7)	ES2 (7)	ES1 (7)	ES0 (7)	A16 (7)	A15 (7)	A14 (7)	A13 (7)

Table 3-2c. Register Bit Assignments - 0020h - 0032h (C29 Only)

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0020	RX Buffer	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0021	TX Buffer	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
Host Read/ Write @ x1	Interrupt Enable Register (IER)	0	0	0	0	Modem Status Interrupt Enable (EDSSI)	RX Line Status Interrupt Enable (ELSI)	TX Buffer Empty Interrupt Enable (ETBEI)	RX Data Avail Interrupt Enable (ERBFI)
Host Read @ x2	Interrupt Identifier Register (IIR)	0	0	0	0	0	Int ID Bit 1	Int ID Bit 0	0 if Interrupt Pending
0023	Line Control Register (LCR)	DLAB	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop Bits	Word Length (WLS1)	Word Length (WLS0)
0024	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
0028	Divisor Latch LSB	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0029	Divisor Latch MSB	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8
002F	Host Handshake Register (HHR)	Controller Intrpt 1 Flag (CF1)	Controller Intrpt 2 Flag (CF2)	Host Intrpt 1 Flag (HF1)	Host Intrpt 2 Flag (HF2)	Controller Intrpt 1 Enable (CE1)	Controller Intrpt 2 Enable (CE2)	Host Intrpt 1 Enable (HE1)	Host Intrpt 2 Enable (HE2)
0030	Line Status Register (LSR)	0	Xmitter Empty (TEMT)	Xmitter Holding Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	RX Data Ready (DR)
0031	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
0032	Host Control Register (HCR)	TX FIFO Buffer Full Interrupt	MCR Write Flag	LCR Write Flag	Divisor Latch Write Flag	1	Host Mode Select	16450 Mode	16450 Interrupt Enable

Table 3-2d. Register Bit Assignments - 0020h - 0032h (C39 Only)

Addr.	Function	Bit 7	6	5	4	3	2	1	0
0020	RX FIFO Buffer (Host Read/C39 Write()	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0020	TX FIFO Buffer (Host Write/C39 Read)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0021	Line Status Register (LSR)	RX FIFO Error	TX FIFO Empty (TEMT)	TX FIFO Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	RX Data Ready (DR)
0022	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
0023	Line Control Register (LCR)	DLAB	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop Bits	Word Length (WLS1)	Word Length (WLS0)
0024	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
0025	FIFO Control Register (FCR)	RCVR Trigger MSB	RCVR Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
Host Rd/Wt @ x1	Interrupt Enable Register (IER)	0	0	0	0	Modem Status Interrupt Enable (EDSSI)	RX Line Status Interrupt Enable (ELSI)	TX Hold Empty Interrupt Enable (ETBEI)	RX Data Avail Interrupt Enable (ERBFI)
Host Read @ x2	Interrupt Identifier Register (IIR)	FIFO Enable (FCR0)	FIFO Enable (FCR0)	0	0	Interrupt ID Bit 2	Interrupt ID Bit 1	Interrupt ID Bit 0	0 if Interrupt Pending
0027	Scratch Register (SCR)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0028	Divisor Latch LSB	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0029	Divisor Latch MSB	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
002E	GP FIFO Status (GPFS)	Tx Empty Interrupt Enable	Tx Empty Interrupt Flag	Tx FIFO Half Empty	Rx Trig Level Sel (RTL1)	Rx Trig Level Sel (RTL0)	Rx Trig Level Int Enable	Rx Trig Level Int Flag	Rx FIFO Data Avail
002F	Host Handshake Register (HHR)	Controller Intrpt 1 Flag (CF1)	Controller Intrpt 2 Flag (CF2)	Host Intrpt 1 Flag (HF1)	Host Intrpt 2 Flag (HF2)	Controller Intrpt 1 Enable (CE1)	Controller Intrpt 2 Enable (CE2)	Host Intrpt 1 Enable (HE1)	Host Intrpt 2 Enable (HE2)
0030	FIFO Status Register (FSR)	TX FIFO Half Full Flag (TCHF)	Data Avail TCDA	RX FIFO Freeze	Receiver Break Interrupt (BI)	Receiver Framing Error (FE)	Receiver Parity Error (PE)	RX FIFO Empty Flag RCEMT	RX FIFO Half Empty Flag (RCHE)
0031	FIFO Interrupt Enable (FIER)	TX FIFO Half Full Interrupt Enable (TCHFE)	Data Avail Interrupt Enable (TCDAE)	UART Timing Select	RUCLK Off	TX FIFO Reset	RX FIFO Reset	RX FIFO Empty Interrupt Enable (RCEMT)	RX FIFO Half Empty Interrupt Enable (RCHE)
0032	Host Control Register (HCR)	TX FIFO Full Interrupt Flag	MCR Write Flag	LCR Write Flag	Divisor Latch Write Flag	RX FIFO Interrupt	Host Mode Select	16450/ 16550 Mode	16450/ 16550 Interrupt Enable

Table 3-2e. Register Bit Assignments - 0034h - 003Fh

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0034	Precision Time Generator A (PTG A) Mode (PAM)	PTG A Interrupt Flag	PTG A Interrupt Enable	Not Used					PTGA Timer Mode
0038	Serial In Buffer (SIB) / Serial Out Buffer (SOB)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0039	Serial Interrupt Register (SIR)	TXD Status Interrupt Flag	TXCLK (PA3) ↑ Interrupt Flag	RXCLK (PA7) ↓ Interrupt Flag	TXCLK (PA3)↑ Interrupt Enable	RXCLK (PA7) ↓ Interrupt Enable	TXD Status Interrupt Enable	RXD Buf Empty Interrupt Enable (BE)	RXD Buf Full Interrupt Enable (BF)
003A	Serial Mode Register (SMR)	RXD On	TXD On	Timing Select 0 = PRGs 1 = TIMB	Sync Mode	TXD Sync Bit	TXREF Clock Select	TXREF RLSDP Sync Enable	Not Used
003B	Serial Line Control Register (SLC)	Parity Stuff Bit	Set Break	Stuff Parity	Even Parity	Enable Parity	Two Stop Bits	Word Length Bit 1 (SL1)	Word Length Bit 0 (SL0)
003C	Serial Status Register (SSR)	TXD Parity Bit	RXD Underrun (UR)	RXD Buffer Empty (BE)	TXD Break Int (BI)	TXD Framing Error (FE)	TXD Parity Error (PE)	TXD Overrun Error (OE)	TXD Buffer Full (BF)
003D	Serial Form Register (SFR)	TXD/ TXDE Echo	REXD/ TXD Echo	TXD/ RXD Echo	TIMA Input TXD Test	TXD/ Edge TXD Test	Not Used	7/8 Short Stop Bit	3/4 Short Stop Bit
003E	SOUT (RXD) Divider Latch (SODL)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
003F	SIN (TXD) Divider Latch (SIDL)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0

3.2. CENTRAL PROCESSING UNIT (CPU)

The central processing unit (CPU) is an enhanced 8-bit 6502 CPU. The CPU executes stored instructions fetched from memory (usually internal masked ROM) sequentially unless a jump to a new location is specified in the instruction or an interrupt occurs. Operation of the CPU instructions are described in Appendix A. The CPU is 6502 instruction compatible except "(indirect, X)" addressing mode changed to "(indirect)," and "(indirect), Y" changed to "(indirect), X".

The MCU CPU registers are the same as the 6502 CPU with the addition of the W-register and I-register.

The data flow for the CPU registers is illustrated in Figure 3-3.

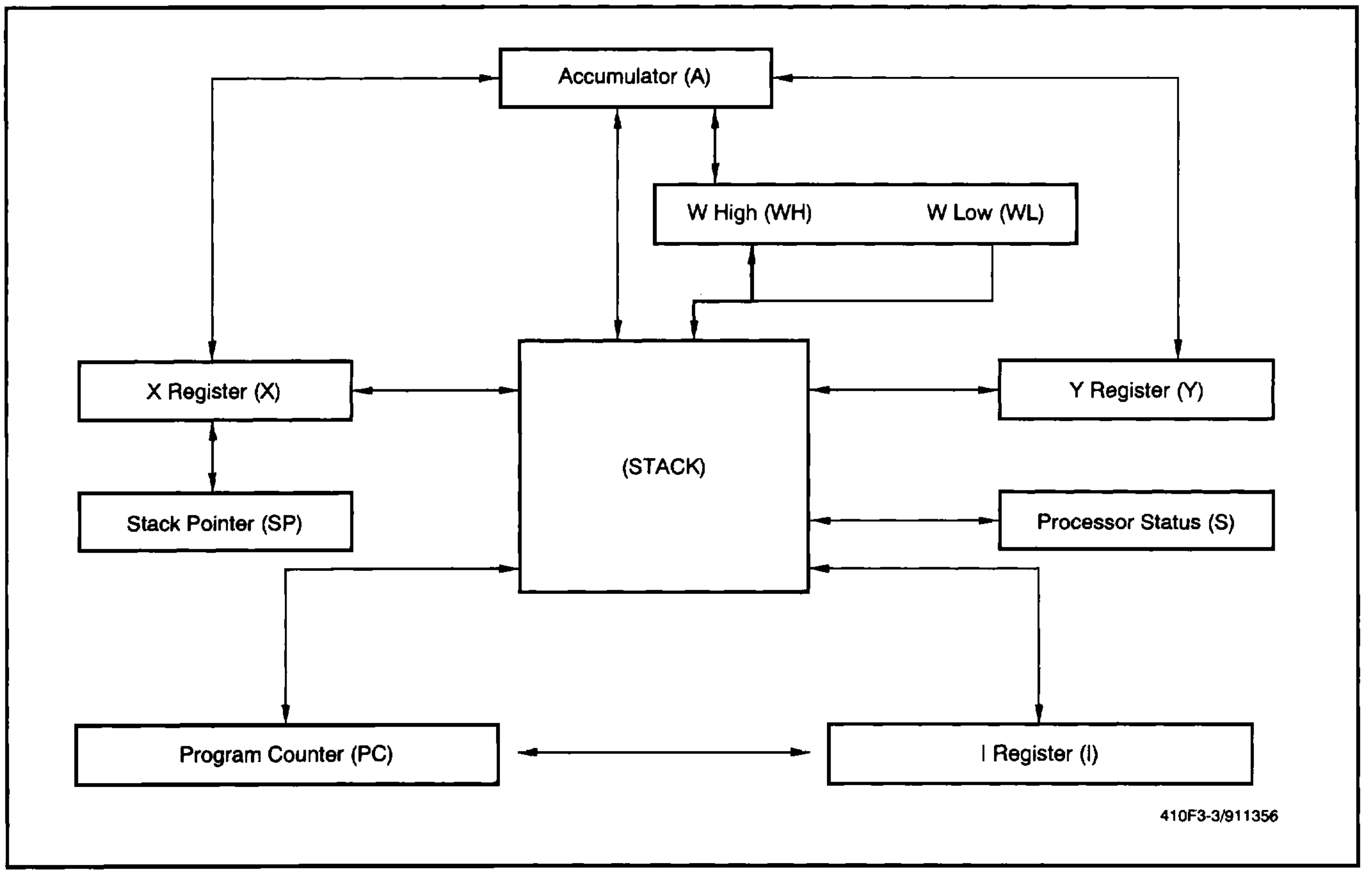


Figure 3-3. CPU Registers and Data Flow

3.2.1. Index Registers

There are two 8-bit index registers: X and Y. Either index register can be used as a base to modify the program counter contents and thus obtain a new address—the sum of the program counter contents and the index register contents. When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

3.2.2. Stack Pointer

The Stack Pointer is an 8-bit register that controls access to the stack. The stack is initialized under software control usually to the top of Page 1 RAM. The stack length can be up to 256 bytes ($1FF down to $100).

The Stack Pointer is automatically incremented and decremented under control of the CPU to perform stack manipulation in response to program instructions, a reset, a non-maskable interrupt (NMI), an internally generated interrupt request (IRQ), or execution of the CPU Break (BRK) instruction. The Stack Pointer must be initialized by the user program. The JSR, JPI, PIA, BRK, RTI, and RTS instructions use the stack and the Stack Pointer.

3.2.3. Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data is placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic 0; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.2.4. Accumulator (A)

The Accumulator (A) is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the Accumulator usually contains one of the two data bytes used in these operations.

3.2.5. Program Counter (PC)

The 16-bit Program Counter (PC) provides the addresses that step the processor through sequential instructions in a program. Each time the processor fetches an instruction from the program memory, the least significant byte of the Program Counter (PCL) is placed on the eight low-order lines of the internal address bus and the most significant byte of the Program Counter (PCH) is placed on the eight high-order lines of the internal address bus. The Program Counter is incremented each time an instruction or data byte is fetched from program memory.

3.2.6. Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the internal data bus. These instructions are latched then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.2.7. W Register (W)

The 16-bit W register is used exclusively to perform the accumulate function during execution of the Multiply Accumulate (MPA) instruction.

3.2.8. I Register (I)

The 16-bit I register is used for threaded code instructions. Note that the I register should not be confused with the CPU Instruction register which is not addressable.

3.2.9. Processor Status Register (PSR)

The 8-bit Processor Status Register (Table 3-3) contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user program and the CPU. The instruction set contains a number of conditional branch instructions which allow testing of these flags. Each of the seven processor status flags is described in the following paragraphs.

Table 3-3. Processor Status Register (PSR)

Function	Bit							
	7	6	5	4	3	2	1	0
Processor Status Register (PSR)	Negative (N)	Overflow (V)	Not Used	Break (B)	Decimal Mode (D)	IRQ Interrupt Disable (I)	Zero (Z)	Carry (C)

Bit 7: **Negative (N).** The Negative (N) bit copies the arithmetic sign bit value resulting from a data movement or an arithmetic operation. If the sign bit is set, the resulting values of the data movement or arithmetic operation is negative and the N bit is a logic 1; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive and the N bit is a logic 0. There are no instructions that set or clear the N bit since the N bit represents only the status of a result. Standard 6502 instructions that affect the state of the N bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA and TYA. New instructions that affect this bit are: ADD, ASR, LAB, LAI, LAN, MPA, MPY, NEG, PIA, RND, TAW, and TWA.

1 = Negative value
0 = Positive value

Bit 6: **Overflow (V).** The Overflow (V) bit indicates that the result of a signed, binary addition or subtraction operation is a value that cannot be contained in seven bits ($-128 \leq n \leq +127$). The V bit only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the V bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the V bit is cleared to logic 0. The V bit may also be cleared under program control by the Clear Overflow (CLV) instruction. There is no instruction to set V.

The Overflow bit may also be used with the BIT instruction. The BIT instruction, which may be used to sample interface devices, allows the V bit to reflect the condition of bit 6 in the sampled field. During a BIT instruction, the V bit is set to equal to the content of bit 6 of the data tested with the BIT instruction. When used in this mode, the V bit has nothing to do with signed arithmetic, but is just another sense bit for the CPU. Standard 6502 Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC. New instructions that affect this bit are: ADD (binary mode only), CLW, MPA, MPY and RND.

1 = Overflow set
0 = Overflow cleared

Bit 5: **Not Used.**

Bit 4: **Break (B).** The Break (B) bit indicates the condition which caused the IRQ service routine to be entered. If the IRQ service routine was entered because the CPU executed a BRK instruction, the B bit is set to logic 1. If the IRQ routine was entered as the result of an IRQ occurrence, the B bit is cleared to logic 0. There are no instructions which can set or clear this bit.

1 = BRK instruction
0 = No BRK instruction

Bit 3: **Decimal Mode (D).** The Decimal Mode (D) bit controls the arithmetic mode of the CPU. When the D bit is a logic 1, the adder operates as a decimal adder. When this bit is a logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by two instructions. The Set Decimal Mode (SED) instruction sets the D bit; the Clear Decimal Mode (CLD) instruction clears it. The PLP and RTI instructions also affect the D bit. The D bit is cleared by assertion of RESP thus initially establishing binary mode.

1 = Decimal mode selected
0 = Binary mode selected

Bit 2: **IRQ Interrupt Disable (I).** The Interrupt Disable (I) bit controls the servicing of the internal interrupt request (IRQ). If the I bit is a logic 0, the IRQ will be serviced. If the bit is a logic 1, the IRQ will be ignored. The CPU sets the I bit to logic 1 if the external NMIP, external RESP, or the internal IRQ input (with the I bit set to a logic 0) is asserted. The I bit is restored by the Pull Processor Status from Stack (PLP) instruction, or as the result of executing a Return from Interrupt (RTI) instruction (provided the Interrupt Disable bit was cleared prior to the interrupt). The Interrupt Disable bit may be set or cleared under program control using a Set Interrupt Disable (SEI) or a Clear Interrupt Disable (CLI) instruction, respectively.

1 = IRQ interrupt disabled
0 = IRQ interrupt enabled

Bit 1: **Zero (Z).** The Zero (Z) bit is set to logic 1 by the CPU during any data movement or by any calculation which sets all eight bits of the result to zero. This bit is cleared to logic 0 when the resultant eight bits of a data movement or calculation operation are not all zero. The instruction set contains no instruction to specifically set or clear the Zero bit. The Z bit is, however, affected by the following standard 6502 instructions: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX and TYA. New instructions that affect this bit are: ADD, ASR, LAB, LAI, LAN, NEG, PIA, TAW, and TWA.

1 = Zero result
0 = Non-zero result

Bit 0: **Carry (C).** The Carry (C) bit can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred, or cleared to logic 0 of no carry occurred, as the result of arithmetic operations. The Carry bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other standard 6502 operations which affect the C bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI and SBC. New instructions that affect this bit are: ADD (binary mode only).

1 = Carry set
0 = Carry cleared

3.2.10. CPU Interrupt Logic

CPU interrupt logic controls the sequencing of the RESP, NMIP, and IRQ activated interrupts and the CPU BRK instruction.

3.2.10.1. RES Sequencing

A low-to-high transition on RESP causes the Interrupt Disable (I) bit in the Processor Status Register to be set and program execution to begin at the address fetched from the RES vector ($FFFE and $FFFF).

3.2.10.2. NMI Sequencing

At the first operation code fetch following the high-to-low transition of the NMIP input, the interrupt logic forces execution of the Break (BRK) instruction and subsequent execution from the address vector stored at $FFFC and $FFFD. Simultaneous with the execution of the BRK instruction, the Interrupt Disable bit in the Processor Status Register is set to disable an IRQ.

3.2.10.3. IRQ Sequencing

An IRQ interrupt occurs when the Interrupt Disable (I) bit of the Process Status Register is cleared (0) and IRQ has been asserted from the IRQ Interrupt Logic. Upon IRQ interruption, the BRK instruction is forced and subsequent program execution begins at the IRQ interrupt service subroutine location specified by the IRQ interrupt vector corresponding to the IRQ number (1-6). The IRQ vector is located in one of six locations in ROM ($FFF0-$FFFB) or one of four locations in RAM ($0102-$0103, $0106-$0107, $0108-$0109, or $010A-$010B). The page 1 RAM IRQ vectors are Timer A and Timer B options, respectively.

The I bit is set to inhibit further IRQ interruption until completion of the IRQ interrupt service subroutine, at which time the I bit is automatically cleared by the RTI instruction. The I bit can also be cleared under program control with the CLI instruction.

For each IRQ that has multiple sources of interruption, the IRQ service subroutine must determine the source of the interrupt by examining applicable interrupts flags. The interrupt flag causing the IRQ should also be cleared after processing the interrupt and before returning to the interrupted routine.

3.3. CLOCK OSCILLATOR

The Clock Oscillator provides the basic timing signals used by the MCU internal circuits. The reference frequency can be supplied by either a parallel resonant crystal or a clock input. The input frequency is divided either by 2 (C29 only) or by 1 (C39 only) to generate the internal Ø2 clock. Typical Clock Oscillator input circuits are shown in Figure 3-4.

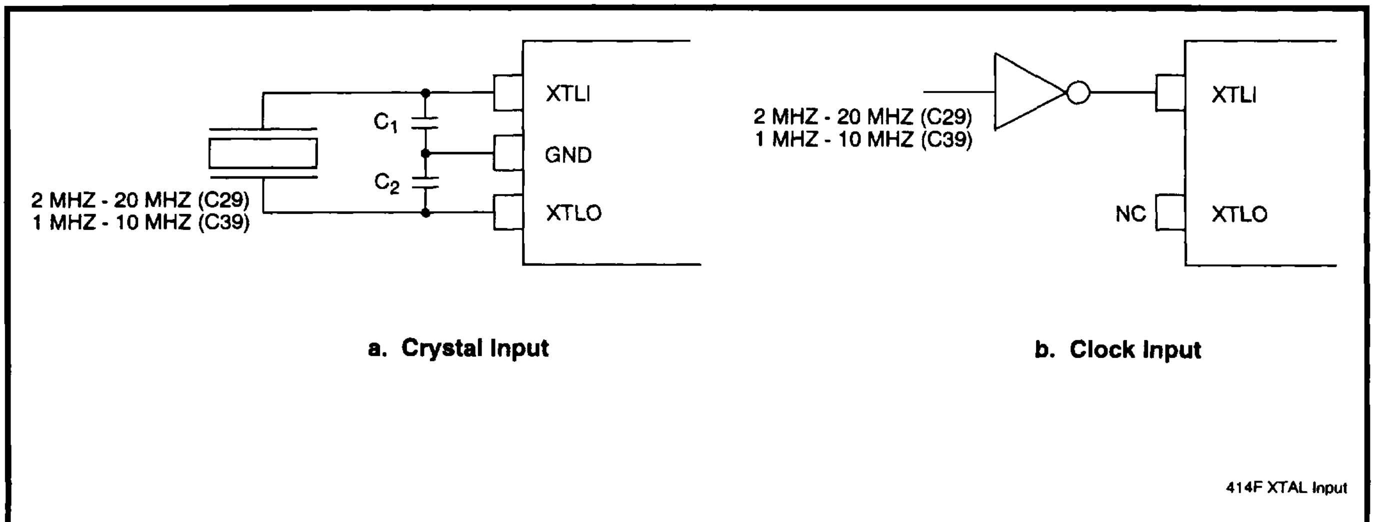


Figure 3-4. MCU Clock Oscillator Input Options

3.4. LOW POWER OPERATION

3.4.1. Low Power Mode (LPM)

The MCU provides a low power Sleep Mode and the C39 provides both a low power Sleep Mode and an ultra low power Stop Mode. Low power operation can be enabled and selected and wake up conditions defined by the host using the Low Power Register (LPR) at address $0009 (see Table 3-4).

3.4.2. Sleep Mode

The Sleep Mode provides low power consumption during periods of no host/modem interface activity and no telephone line activity while the modem internal clock is operating. In this mode, either host/modem or telephone line activity can be enabled to wake up the modem for immediate operation.

Wake up can be enabled to occur upon an edge being detected on PA2 (Ring), PD4 (Host Chip Select) and PD5 (Host Write Enable), or PA0 (Transmit Data), or a low on NMIP. The signals in parenthesis show the typical signals connected to the corresponding ports.

3.4.3. Stop Mode (C39 Only)

The Stop Mode allows the host to completely turn off microcontroller operation except for wake up capability during periods of no modem operation as determined by the host. In the Stop Mode, modem operation is available within 12 clock times following wake-up.

Wake up can be enabled to occur upon a low being detected on PA2 (Ring), PD4 (Host Chip Select) and PD5 (Host Write Enable), PA0 (Transmit Data), PD4 (DTR), or PD5 (AL), or a low on NMIP for at least 12 clock times. The signals in parenthesis show the typical signals connected to the corresponding port.

3.4.4. Low Power Register (LPR)

The Low Power Register (LPR) bits are identified in Table 3-4.

Table 3-4. Register Bit Assignments - Low Power Register (LPR) - 0009h

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0009	Low Power Register (LPR)	Low Power Mode Enable	Low Power Mode Select	Wake up Enable PA0 (Ring)	Wake up Enable PD4 (Wrt) PD5 (CS)	Wake up Enable PA2 (TXD)	Wake up Enable PD4 (DTR)	Wake up Enable PD5 (AL)	Not Used

Bits 0: **Not Used.**

Bits 1: **Wake-Up Enable for PD5 (AL) (C39 Only).** This bit, when set to a logic 1, enables the CPU to wake up from low power mode when a low is detected on PD5.

Bit 2: **Wake-Up Enable for PD4 (DTR) (C39 Only).** This bit, when set to a logic 1, enables the CPU to wake up from low power mode when a low is detected on PD4.

Bit 3: **Wake-Up Enable for PA2 (TXD Start Bit).** This bit, when set to a logic 1, enables the MCU to wake up from low power mode when a low is detected on PA2.

Bit 4: **Wake-Up Enable for PD4 and PD5 (Host Bus Write and MCU Chip Select).** This bit, when set to a logic 1, enables the MCU to wake up from low power mode when a low is detected on both PD4 and PD5.

Bit 5: **Wake Up Enable for PA0 (Ring).** This bit, when set to a logic 1, enables the MCU to wake up from low power mode when a low is detected on PA0.

Bit 6: **Low Power Mode Select (C39 Only).** This bit selects the low power mode (0 = Sleep; 1 = Stop) to be entered when low power conditions exist and low power mode is enabled by LPR7.

Bit 7: **Low Power Mode Enable.** C29: This bit enables or disables the Sleep Mode (1 = Sleep Mode; 0 = Normal Mode).

C39: This bit enables or disables the low power mode selected by LPR6 to be entered when low power conditions exist (1 = LPM enabled; 0 = LPM disabled).

3.5. IRQ INTERRUPT LOGIC

3.5.1. Interrupt Request (IRQ)Vector and Hardware Priority

The IRQ Interrupt Logic prioritizes the individual interrupt requests (IRQ1-IRQ6) from the various sources and passes a single IRQ along with an IRQ number (1-6) and the IRQ vector page indicator to the CPU Interrupt Logic. Figure 3-5 illustrates the IRQ Interrupt Logic interface. Table 3-5 shows the IRQ interrupt levels, sources and vector addresses.

If simultaneous IRQs occur on IRQ1-IRQ6 lines, the number of the highest priority IRQ (1 = highest) is passed to the CPU. When the interrupt flag causing the IRQ is cleared by the IRQ interrupt service subroutine, the IRQ number of the highest pending IRQ is then passed.

The selection of ROM or RAM IRQ interrupt vectors for Timer A (IRQ5) and Timer B (IRQ3) is determined by bits 5 and 6 in the Timer A Mode and Timer B Mode registers, respectively (3.7).

3.5.2. Break Command Priority Change (C39)

The BRK instruction in the C39 uses the NMI vector instead of the IRQ6 vector used in the C29. The C39 BRK instruction operates as follows:

BRK **Break Command**

Operation: Forced Interrupt Request: PC + **1** ↓ , P ↓

N	V	—	B	D	I	Z	C
—	—	—	1	—	1	—	—

The BRK command causes the processor to go through an interrupt request sequence under program control. The address in the program counter (which points to the location of the BRK command + **1**) is pushed on the stack, along with the processor status at the beginning of the BRK instruction. The processor then transfers control to the **NMI** interrupt vector **(FFFC,D)**. Note that the BRK command cannot be masked by setting the I flag.

Addressing Mode	Assembly Language Form	Op Code	No. Bytes	No. Cycles
Implied	BRK	00	1	7

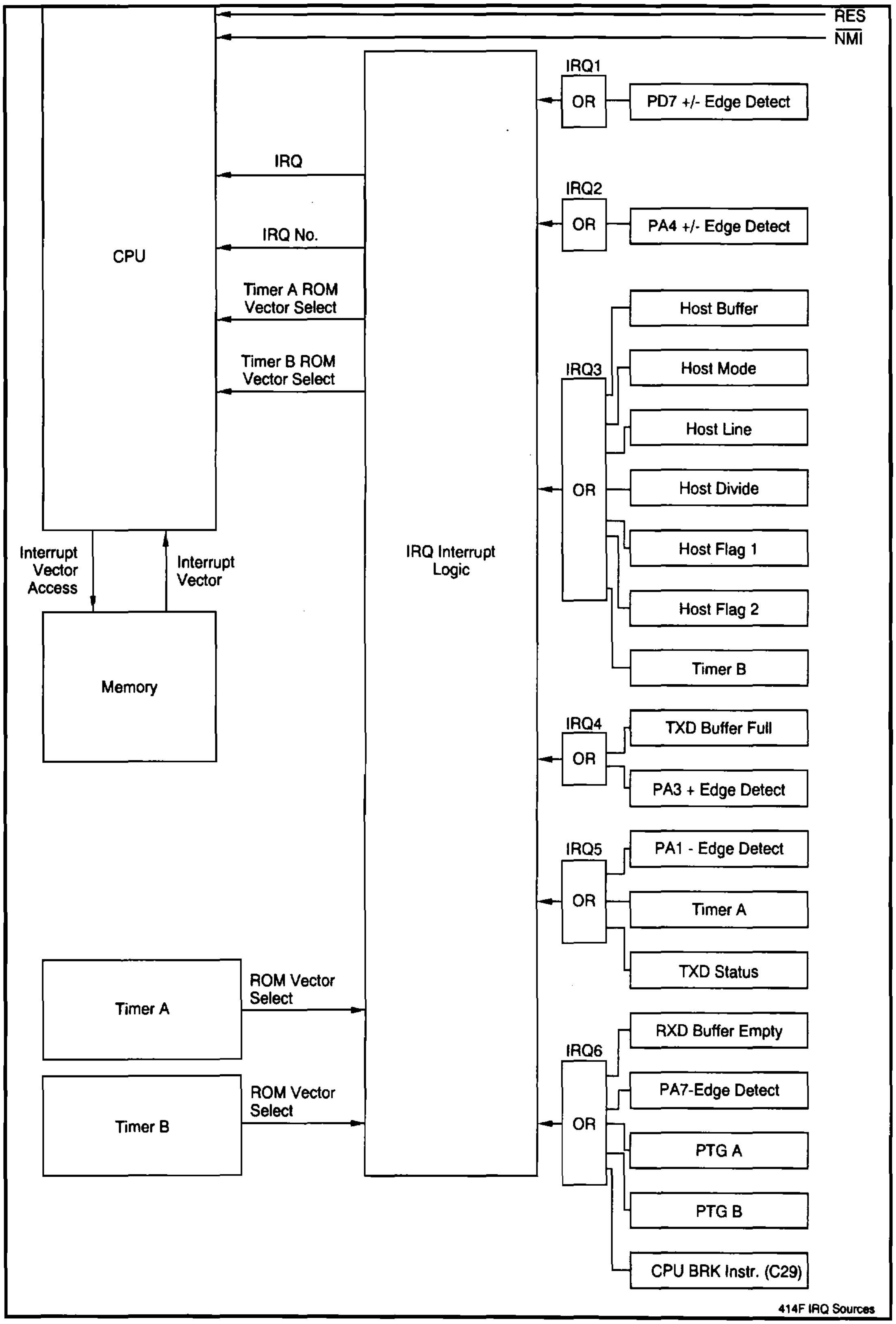


Figure 3-5. IRQ Interrupt Logic Interface

Table 3-5. Interrupt Request (IRQ)Vector and Hardware Priority

Source	Location		Interrupt Vector and Priority Level						Notes
	Flag	Enable	IRQ1	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	
PD7 Edge Detect (+,-)	EIR5	EIR2	FFFA,B						
PA4 Edge Detect(+,-)	EIR6	EIR3		FFF8,9					
PA1 Edge Detect (-)	EIR7	EIR4					FFF2,3		
RX FIFO Half Empty (RCHE)	FSR0	FIER0			FFF6,7				
RX FIFO Empty (RCEMT)	FSR1	FIER1			FFF6,7				
TX FIFO Data Avail (TCDA)	FSR6	FIER6			FFF6,7				
TX FIFO Half Full (TCHF).	FSR7	FIER7			FFF6,7				
RX FIFO Interrupt	HCR3	FIER0, FIER1			FFF6,7				C39 only
Divisor Latch Write	HCR4	HCR0			FFF6,7				
Line Control Register Write	HCR5	HCR0			FFF6,7				
Mode Control Register Write	HCR6	HCR0			FFF6,7				
TX Buffer Full	HCR7	HCR0			FFF6,7				C29 only
TX FIFO Interrupt	HCR7	FIER6, FIER7			FFF6,7				C39 only
Controller Attention 2 (CF2)	HHR6	HHR2			FFF6,7				
Controller Attention 1 (CF1)	HHR7	HHR3			FFF6,7				
Timer A (ROM)	TAM7	TAM6					FFF2,3		
Timer A (Page 1)	TAM6	TAM6					0102,3		
Timer B (ROM)	TBM7	TBM6			FFF6,7				
Timer B (Page 1)	TBM6	TBM6			0106,7				
TXD Buffer Full	SS0	SI0				FFF4,5			
TXD Status	SI7	SI2					FFF2,3		
PA3 Edge (+)	SI6	SI4				FFF4,5			
RXD Buffer Empty	SS5	SI1						FFF0,1	
PA7 Edge Detect (-)	SI5	SI3						FFF0,1	
PTGA	PAM7	PAM6						FFF0,1	
PTGB	PBM7	PBM6						FFF0,1	
CPU BRK Instruction *								FFF0,1	C29 only

* C39 uses NMI vector (see BRK instruction description).

3.6. INTERNAL ROM

The internal Read Only Memory (ROM) usually contains the user's program instructions and other fixed constants. These program instructions and constants are mask-programmed during fabrication.

The internal ROM size is 8192 bytes and is memory mapped from $E000 to $FFFF.

3.7. INTERNAL RAM

The internal Random Access Memory (RAM) contains the user program stack and is used for scratch pad memory during system operation. This RAM is completely static in operation and requires no clock or dynamic refresh. The data contained in RAM is read out nondestructively with the same polarity as the input data. In the event that execution stops, RAM data is retained until execution resumes.

The internal RAM size is 1024 bytes. A block of 128 bytes are assigned to page 0 ($80 to $FF). Three blocks of 256 bytes each are assigned to pages 1 through 3 ($100 to $1FF, $200 to $2FF, and $300 to $3FF). A fifth block of 128 bytes is assigned to page 4 ($400 to $47F).

3.8. MEMORY BANKING

The MCU has a special dual port RAM that allows the user to bank select external memory. See Figure 3-6. The dual port bank select RAM consists of 8 bytes of internal RAM shown below from address locations $0018 through $001F.

7	6	5	4	3	2	1	0
ES3	ES2	ES1	ES0	A16	A15	A14	A13

Each time the CPU provides address' AD15, AD14, and AD13 one of the eight BANK select RAM is selected.

Address	CPU Address Line			Bank Select	Reset	Default	
Map	AD15	AD14	AD13	RAM (Byte)	Values	Select	Speed
$0018	0	0	0	0	1110 0000	ES0	X1
$0019	0	0	1	1	1101 0001	ES1	X1
$001A	0	1	0	2	1011 0010	ES2	X1
$001B	0	1	1	3	1011 0011	ES2	X1
$001C	1	0	0	4	0111 0100	ES3	X1
$001D	1	0	1	5	0111 0101	ES3	X1
$001E	1	1	0	6	0111 0110	ES3	X1
$001F	1	1	1	7	0111 0111	ES3	X1

The device will output active low chip select lines on PB5, PB4, PB3, and PB2 according to the logic-0 bits of the selected banking RAM register bits 4 through 7 (ES3, ES2, ES1, and ES0) respectively when its respective port B select registers PBS5 = 0, PBS4 = 0, PBS3 = 0, or PBS2 = 0. PB1 outputs active low chip select ES4 for address space $0600 to $0800 when PBS1 = 0. The address space for ES4 is included when bank select RAM 0 is selected and PBS1 = 1.

The device will output address lines A15, A14, and A13 according to the contents of the selected banking RAM register bits 2-0 respectively. PB0 becomes bit 3 (A16) of the contents of the selected banking RAM register when the port B select register PBS0 = 0. Address A16 allows addressing 8K memory banks above 64 K of memory.

The user can alter the contents of each byte of banking RAM by writing to the individual register address or use its respective reset value shown above.

The selected banking RAM's speed choice for chip selects ES3, ES2, ES1, and ES0 are reflected in the ESS speed register shown below. During power up, bank select 7 is automatically selected with chip select ES3 running at the highest X1 speed. The user can alter the contents of the ESS register or use the highest X1 speed default value shown.

The following table shows the memory speed selected for the chip selects chosen in the selected banking RAM.

ESS Speed Control		
MSB	**LSB**	**Speed**
0	0	X 1
0	1	X 1/2
1	0	X 1/3
1	1	X 1/4

Priority logic will make the memory speed take on the choice of the highest active chip select ES3, ES2, or ES1 when two or more are enabled.

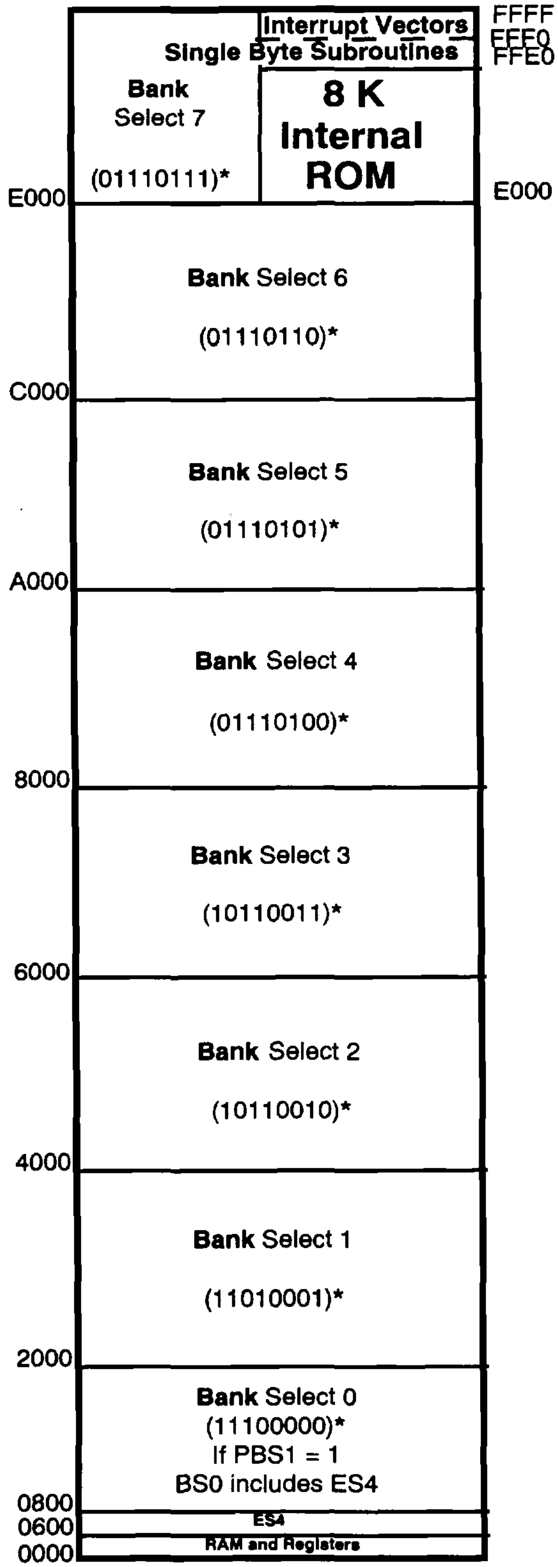
Memory banking is performed using internal address translation using eight Bank Select Registers (3.8.1). Each Bank Select Register (BSR) controls the address translation of A[15:13], controls the A16 pseudo-address bit, and defines an active bank select from ES[3:0] for a fixed 8k-byte region of linear address. This logic enables flexible banking while simultaneously eliminating the need for the external programmable logic device normally required to support banking. In addition, stretched internal clock cycles can be assigned independently to each BSR chip select range using the ES Speed Register (3.8.2) to allow the use of slower memories. The address translation allows several banks with the same logical address range to be physically relocated so that they can all reside within the same memory device with different physical address ranges.

This banking technique becomes more easily understood if one views the addition of A16 and ES[3:0] separately from the internal address translation. Although A16 functions identically to ES[3:0] in that it is a manually controlled bit in each BSR and drives an external pin, emulation support mandates that this signal not be used as a chip select. The new expanded address field A[16:0] maps directly to A[16:0] of a 128K memory device. When each ES signal drives the chip enable of a separate 128K memory device, this scheme supports a theoretical banked memory of 128K x 4 = 512K bytes.

The address translation feature does not increase the amount of banked memory beyond this theoretical limit, but it allows several banks with the same logical address range to be mapped within the same physical device.

Note that ES0-ES3 and A16 are Port B special purpose outputs and must be enabled using the Port B Select (PBS) register.

The memory banks are illustrated within the overall memory map in Figure 3-6. The MCU banking logic is shown in Figure 3-7. The bank select registers are shown in Table 3-6.



7	6	5	4	3	2	1	0
ES3	ES2	ES1	ES0	A16	A15	A14	A13

Bank Select RAM
* Reset values

Figure 3-6. Memory Map - RAM Banking

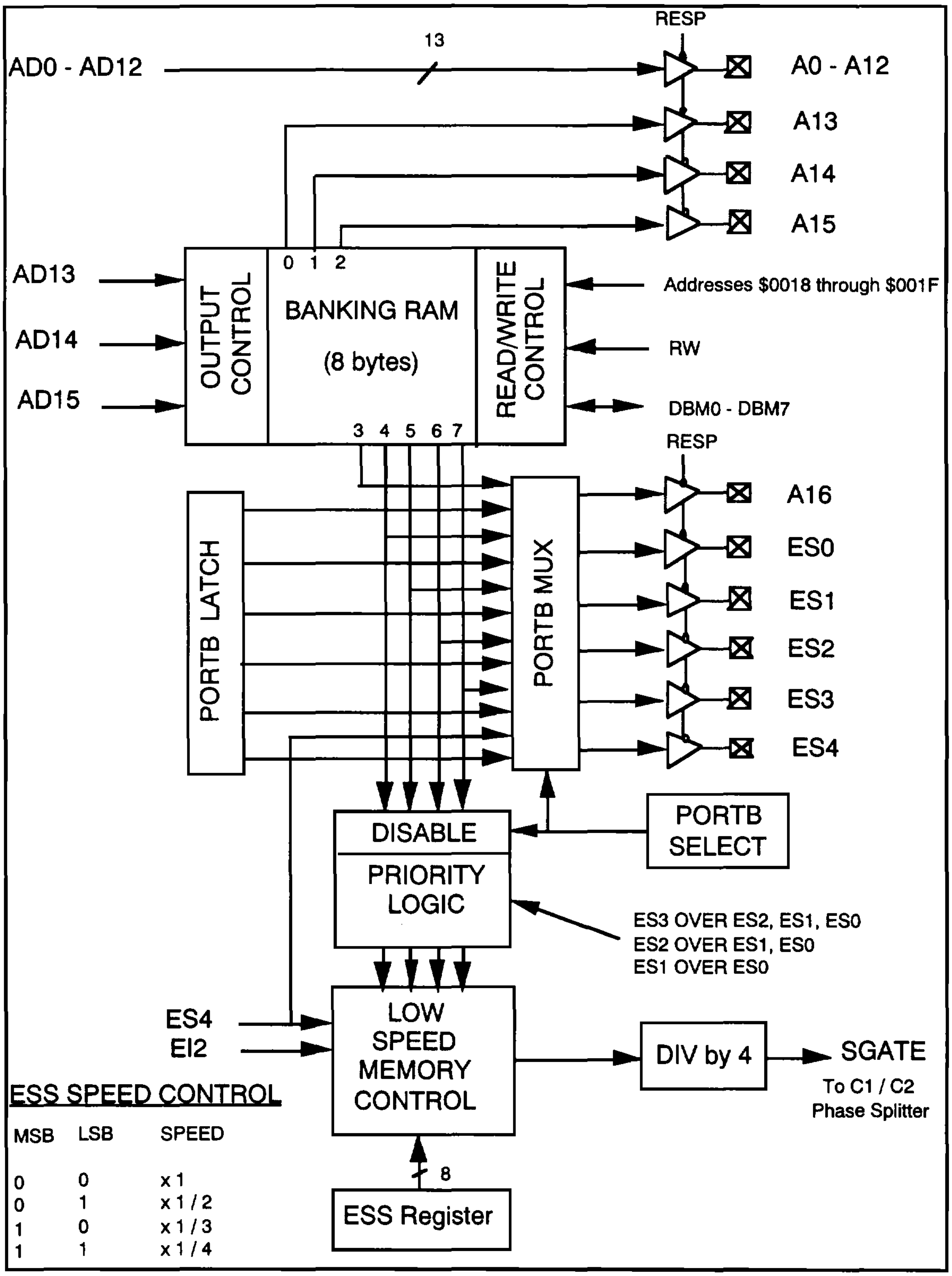


Figure 3-7. Banking Logic

3.8.1. Bank Select Register (BSR)

Table 3-6. Register Bit Assignments - Bank Select Register I (BSRI) - 0018h-001Fh

		Bit							
Addr.	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0018	Bank Select Register 0 (BSR0)	ES3 (0)	ES2 (0)	ES1 (0)	ES0 (0)	A16 (0)	A15 (0)	A14 (0)	A13 (0)
0019	Bank Select Register 1 (BSR1)	ES3 (1)	ES2 (1)	ES1 (1)	ES0 (1)	A16 (1)	A15 (1)	A14 (1)	A13 (1)
001A	Bank Select Register 2 (BSR2)	ES3 (2)	ES2 (2)	ES1 (2)	ES0 (2)	A16 (2)	A15 (2)	A14 (2)	A13 (2)
001B	Bank Select Register 3 (BSR3)	ES3 (3)	ES2 (3)	ES1 (3)	ES0 (3)	A16 (3)	A15 (3)	A14 (3)	A13 (3)
001C	Bank Select Register 4 (BSR4)	ES3 (4)	ES2 (4)	ES1 (4)	ES0 (4)	A16 (4)	A15 (4)	A14 (4)	A13 (4)
001D	Bank Select Register 5 (BSR5)	ES3 (5)	ES2 (5)	ES1 (5)	ES0 (5)	A16 (5)	A15 (5)	A14 (5)	A13 (5)
001E	Bank Select Register 6 (BSR6)	ES3 (6)	ES2 (6)	ES1 (6)	ES0 (6)	A16 (6)	A15 (6)	A14 (6)	A13 (6)
001F	Bank Select Register 7 (BSR7)	ES3 (7)	ES2 (7)	ES1 (7)	ES0 (7)	A16 (7)	A15 (7)	A14 (7)	A13 (7)

Bits 0-3: A13 (I) - A15(I). Address Translation Bits for Bank I.

Bits 4-7: ES0(I) - ES3(I). Memory Bank Select for Bank I.

Notes:

1. When 0 is not present in BSR7 (ES3 to ES0), the internal ROM is enabled. This allows a bootstrap routine in internal ROM to be run, e.g., to configure the ES Speed register to select the effective clock width during external memory access. When the internal ROM is enabled, the external transceivers are disabled for addresses within the BSR7 range.

   When the TST pin is disabled, the internal ROM is enabled until a new value is written into BSR7.

3.8.2. ES Speed Register

The ES Speed register at address $0033 (Table 3-7) selects the number clock times that the internal clock is stretched during a memory access in an address range corresponding to an ES0-ES3 chip select.

Table 3-7. Register Bit Assignments - ES Speed Register - 0033h

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0033	ES Speed (ESS)	ES3-1	ES3-0	ES2-1	ES2-0	ES1-1	ES1-0	ES0-1	ES0-0

Default = $00 (X1 - 1 clock time selected.)

Bits 0-1: Chip Select 0 (ES0) Effective Clock Width. These two bits select the number of clock times that the internal clock is stretched during a memory access when the ES0 chip select is active.

Bit 1 (ES0-1)	Bit 0 (ES0-0)	Effective Clock Width
0	0	X1 - 1 clock time
0	1	X2 - 2 clock times
1	0	X3 - 3 clock times
1	1	X4 - 4 clock times

Bits 2-3: Chip Select 1 (ES1) Effective Clock Width. These two bits select the number of clock times that the internal clock is stretched during a memory access when the ES1 chip select is active.

Bit 3 (ES1-1)	Bit 2 (ES1-0)	Effective Clock Width
0	0	X1 - 1 clock time
0	1	X2 - 2 clock times
1	0	X3 - 3 clock times
1	1	X4 - 4 clock times

Bits 4-5: Chip Select 2 (ES2) Effective Clock Width. These two bits select the number of clock times that the internal clock is stretched during a memory access when the ES2 chip select is active.

Bit 5 (ES2-1)	Bit 4 (ES2-0)	Effective Clock Width
0	0	X1 - 1 clock time
0	1	X2 - 2 clock times
1	0	X3 - 3 clock times
1	1	X4 - 4 clock times

Bits 6-7: Chip Select 3 (ES3) Effective Clock Width. These two bits select the number of clock times that the internal clock is stretched during a memory access when the ES3 chip select is active.

Bit 7 (ES3-1)	Bit 6 (ES3-0)	Effective Clock Width
0	0	X1 - 1 clock time
0	1	X2 - 2 clock times
1	0	X3 - 3 clock times
1	1	X4 - 4 clock times

3.9. PARALLEL INPUT/OUTPUT PORTS

The MCU parallel input/output interface consists of five 8-bit ports: A, B, C, D, and E. Port E is available only on 80-pin PQFP and 84-pin PLCC packages.

Ports A, C and E contain 24 bidirectional lines with the data direction determined by the direction registers. Port D has 4 bidirectional lines (0-3) with the data direction determined by its direction register, and 4 input only lines (4-7). Port B supports 8 output-only lines.

All port lines can be used for general purpose functions. Thirty two I/O lines can be assigned special functions under software control. The special purpose and mask option functions of the port lines are identified in Table 3-8. Table 3-9 further defines the special purpose applications along with software control and direction register requirements. Port read and write timing is described in Section 5.

Output Mode. The data written to each output pin is loaded into an output data latch. The data will remain in the output latch until new data is written to the port address or until power is removed. The output latches are individually connected to output drivers. The output drivers are double-ended, push-pull type. The drivers force the output pins high (≥ 2.4V) if the output data bit is a logic 1, or low (≤0.4V) if the output data bit is a logic 0. The output drivers are TTL compatible.

Input Mode. For each input port line, either permanently or direction register assigned as an input, the data is sampled by an input synchronizer. A low input level (≤0.8 v) is interpreted as a logic 0 and a high input level (≥2.0 V) is interpreted as a logic 1. Input data is sampled during internal C2 clock time and then temporarily held from C1 to C1 clock time. When the CPU reads the input port, the data is transferred to the CPU during C2 time and represents data sampled during the previous C2 time.

Table 3-8. I/O Port Special Purpose Functions

Port Bit	Port				
	A	B	C	D	E
0	TIMA/RING/CTSP	A16	HD0	HA0	None
1	TXDE/- Edge	ES4	HD1	HA1	None
2	TXD/LPWU TXD	ES3	HD2	HA2	None
3	TXCLK/+Edge/HTACKP (C39)	ES2	HD3	HA3	None
4	TXREF/+/- Edge/RLSDP/HRACKP (C39)	ES1	HD4	HCSP/ LPWU DTR/ LPWU HBW	None
5	REXD/TXRDY (C39)	ES0	HD5	HWTP/ LPWU AL/ LPWU HBW	None
6	RXD/RXRDY (C39)	HDIS	HD6	HRDP	None
7	RXCLK/- Edge	HINT	HD7	+/- Edge	None

Table 3-9. I/O Port Special Purpose Function Control

Port Line	Function	Option Selected by	I/O	Direction Register
		Port A		
PA0	TIMA - Timer A Pulse Generator Output	TAM1 = 0, TAM0 = 1	O	PAD0 = 1
	TIMA - Timer A Event Counter Input	TAM1 = 1, TAM0 = 0	I	PAD0 = 0
	TIMA - Timer A Pulse Width Measurement Input	TAM1 = 1, TAM0 = 1	I	PAD0 = 0
	RING - Ring Detect Input	LPR5 = 1	I	PAD0 = 0
	CTSP - USART TXD Sync to Falling Edge	SMR6 = 1, SMR1 = 1	I	PAD0 = 0
PA1	TXDE - USART PA1 Output Copies PA2 Input	SF7 = 1	O	PAD1 = 1
	PA1 - Negative Edge Detect	None, see EI7	I/O	PAD1 = X
PA2	TXD - USART Serial Input	SMR6 = 1	I	PAD2 = 0
	LPWU - PA2 Low (TXD)	LPR3 = 1	I	PAD2 = 0
PA3	TXCLK - USART Internal Timing		O	PAD3 = 1
	TXCLK - USART External Timing		I	PAD3 = 0
	TXCLK - USART Copy TXCLK (PA4)	SMR4 = 1	I/O	PAD3 = X
	PA3 - Positive Edge Detect	None, see SIR3	I/O	PAD3 = X
	HTACKP - TX Acknowledge Input (C39)	HCR2 = 1	I	PAD3 = 0
PA4	TXREF - External Clock Input	SMR4 = 1 and SMR2 = 1		PAD4 = 0
	PA4 - Positive and Negative Edge Detect	None, see IER6	I/O	PAD4 = X
	RLSDP USART RXD Sync to Falling Edge	SMR7 = 1, SMR1 = 1		PAD4 = 0
	HRACKP - 16550A RX Acknowledge Input (C39)	HCR2 = 1 (C39)	I	PAD4 = 0
PA5	REXD - USART Serial Input	SM7 = 1, SF5 = 0, SF6 = 1		PAD5 = 0
	TXRDY - TX Ready Output (C39)	HCR2 = 1 (C39)		PAD5 = 1
PA6	RXD - USART Serial Output	SMR7 = 1		PAD6 = 0
	RXRDY - RX Ready Output (C39)	HCR2 = 1 C39)		PAD6 = 1
PA7	RXCLK - RXD Serial Output Clock	SMR7 = 1, SMR4 = 1	O	PAD7 = 1
	PA7 - Falling Edge Detect	None, see SIR5	I	PAD7 = X
		Port B		
PB0	A16 - External Bus Address Line A16	PBS0 = 0	O	Output Only
PB1	ES4 - External Bus Chip Select	PBS1 = 0	O	
PB2	ES3- External Bus Chip Select	PBS2 = 0	O	
PB3	ES2- External Bus Chip Select	PBS3 = 0	O	
PB4	ES1- External Bus Chip Select	PBS4 = 0	O	
PB5	ES0- External Bus Chip Select	PBS5 = 0	O	
PB6	HDIS - Host Bus Driver Disable	PBS6 = 0, HCR2 = 1	O	
PB7	HINT - Host Bus Interrupt Line	PBS7 = 0, HCR2 = 1	O	

Table 3-9. I/O Port Special Purpose Function Control (Cont'd)

Port Line	Function	Option Selected by	I/O	Direction Register
Port C				
PC0	HD0 - Host Bus Data Line 0	HCR2 = 1	I/O	Controlled by HWTP and HRDP
PC1	HD1 - Host Bus Data Line 1			
PC2	HD2- Host Bus Data Line 2			
PC3	HD3- Host Bus Data Line 3			
PC4	HD4- Host Bus Data Line 4			
PC5	HD5- Host Bus Data Line 5			
PC6	HD6- Host Bus Data Line 6			
PC7	HD7- Host Bus Data Line 7			
Port D				
PD0	HA0 - Host Bus Address Line 0	HCR2 = 1	I	N/A
PD1	HA1- Host Bus Address Line 1	HCR2 = 1		
PD2	HA2- Host Bus Address Line 2	HCR2 = 1		
PD3	HA3- Host Bus Address Line 3	HCR2 = 1 and HCR1 =1		
PD4	HCSP- Host Bus Chip Select	HCR2 = 1	I	Input Only
	LPWU - PD4 Low (DTR)	LPR2 = 1		
	LPWU HBW - PD4 and PD5 Low (HB Write)	LPR4 = 1		
PD5	HWTP - Host Bus Write Enable	HCR2 = 1		
	LPWU AL - PD5 Low (AL)	LPR1 = 1		
	LPWU HBW - PD4 and PD5 Low (HB Write)	LPR4 = 1		
PD6	HRDP - Host Bus Read Enable	HCR2 = 1		
PD7	PA7 Falling or rising edge detect	None, see IER5		

3.9.1. Bidirectional Ports A, C, and E

Ports A, C, and E consist of 24 general purpose bidirectional input/output lines. The data direction for each I/O line is controlled by an associated direction register bit. For each direction register bit that is a logic 1, the corresponding port line is an output. Conversely, a 0 in a direction register bit defines the corresponding port line as an input. The direction register bits are initialized to a 0 by reset causing the I/O ports to be inputs.

All port A, and C lines can be assigned to special purpose functions during operation under software control. The port A lines can be assigned to special functions under software control (Tables 3-8 and 3-9). PA3 and PA7 have associated edge detect logic that can generate an IRQ interrupt .

Seven port B lines can be assigned to special functions under software control and one line can be permanently masked to a special function (Tables 3-8 and 3-9). PB2 and PB3 have associated edge detect logic that can generate an IRQ interrupt.

All eight port C lines can be assigned to host bus data lines under software control (Tables 3-8 and 3-9).

3.9.2. Bidirectional and Input Only Port D

The eight port D lines are grouped as four general purpose bidirectional input/output lines and as four input only lines (Tables 3-8 and 3-9). PD7 has associated edge detect logic that can generate an IRQ interrupt. Seven lines (PD0-PD6) can be assigned by software as host bus address and control line inputs (3.11). The direction register control bits for port D must be set high (1) for output and low (0) for input. The direction register control bits are initialized to 0 by reset.

3.9.3. Output Port B

The 8 port B lines (PB0-PB7) are general or special purpose output only (Table 3-8). Lines PB0-PB5 can be assigned to A16 address line and the ES0-ES4 chip select functions controlled by the Bus Select Registers and PB6 and PB7 can be assigned to HDIS and HINT functions (see Table 3- 9). Port B output latches are initialized low upon reset. The Port B output drivers tri-state (float) during reset active low.

3.9.4. Port B Select Register (PBS)

The Port B Select Register (PBS) bits are identified in Table 3-10.

Table 3-10. Port B Select Register (PBS)

Addr.	Function	Bit 7	6	5	4	3	2	1	0
0005	Port B Select (0-7)	PBS7 0-- HINT 1-- PB7	PBS6 0-- HDIS 1-- PB6	PBS5 0-- ES0 1-- PB5	PBS4 0-- ES1 1-- PB4	PBS3 0-- ES2 1-- PB3	PBS2 0-- ES3 1-- PB2	PBS1 0-- ES4 1-- PB1	PBS0 0-- A16 1-- PB0

Bit 0: **PB0 /A16 Select.** Selects the general purpose or special purpose function for port PB0.

0 = A16
1 = PB0

Bit 1: **PB1 /ES4 Select.** Selects the general purpose or special purpose function for port PB1.

0 = ES4
1 = PB1

Bit 2: **PB2 /ES3 Select.** Selects the general purpose or special purpose function for port PB2.

0 = ES3
1 = PB2

Bit 3: **PB3/ES2 Select.** Selects the general purpose or special purpose function for port PB3.

0 = ES2
1 = PB3

Bit 4: **PB4/ES1 Select.** Selects the general purpose or special purpose function for port PB4.

0 = ES1
1 = PB4

Bit 5: **PB5/ES0 Select.** Selects the general purpose or special purpose function for port PB5

0 = ES0
1 = PB5

Bit 6: **PB6 /HDIS Select.** Selects the general purpose or special purpose function for port PB6.

0 = HDIS
1 = PB6

Bit 7: **PB7/HINT Select.** Selects the general purpose or special purpose function for port PB7.

0 = HINT
1 = PB7

3.9.5. External Interrupt Register (EIR)

The External Interrupt Register (EIR) enables and reports interrupts associated with ports PA1, PA4, and PD7 (Table 3-11). All bits are cleared to zero by reset. The CPU can set or reset bits 0-4 by writing to address $000A. Bits 5-7 are cleared by writing a 0 to the corresponding bit position in the CIR. The CPU can monitor all bits by reading address $000A.

Table 3-11. External Interrupt Register (EIR) - $000A

Addr.	Function	Bit							
		7	6	5	4	3	2	1	0
000A	External Interrupt Register (EIR)	External Interrupt Flag PA1	External Interrupt Flag PA4	External Interrupt Flag PD7	External Interrupt Enable PA1 (IRQ5)	External Interrupt Enable PA4 (IRQ2)	External Interrupt Enable PD7 (IRQ1)	Edge Detect Polarity PA4 0=↓ Edge 1=↑ Edge	Edge Detect Polarity PD7 0=↓ Edge 1=↑ Edge

Bit 0: **PD7 Positive Edge Detect.** This bit controls the edge detection polarity on PD7 (0 = negative or falling (high-to-low) edge; 1 = positive or rising (low-to-high) edge).

Bit 1: **PA4 Positive Edge Detect.** This bit controls the edge detection polarity on PA4 (0 = negative or falling (high-to-low) edge; 1 = positive or rising (low-to-high) edge).

Bit 2: **PD7 Interrupt Enable.** This bit controls the assertion of IRQ1 when EIR5 is set to a logic 1 (0 = disable assertion; 1 = enable assertion).

Bit 3: **PA4 Interrupt Enable.** This bit controls the assertion of IRQ2 when EIR6 is set to a logic 1 (0 = disable assertion; 1 = enable assertion).

Bit 4: **PA1 Interrupt Enable.** This bit controls the assertion of IRQ5 when EIR7 is set to a logic 1 (0 = disable assertion; 1 = enable assertion).

Bit 5: **PD7 Interrupt Flag.** This bit is set to a logic 1 when a positive (EIR0 = 1) or negative (EIR0 = 0) edge is detected on PD7. This bit is cleared by writing a logic 0 to CIR5.

Bit 6: **PA4 Interrupt Flag.** This bit is set to a logic 1 when a positive (EIR1 = 1) or negative (EIR1 = 0) edge is detected on PA4. This bit is cleared by writing a logic 0 to CIR6.

Bit 7: **PA1 Interrupt Flag.** This bit is set to a logic 1 when a negative edge is detected on PA1. This bit is cleared by writing a logic 0 to CIR7.

3.9.6. Clear Interrupt Register (CIR)

The Clear Interrupt Register (CIR) at address $000B (Table 3-12) is used to clear five interrupt flags (PA3, PA7, PD7, PA4, and PA1), set the base address for extended page 0 RAM access, and set the fast/slow operation of ES4 expansion bus addressing. CIR0, CIR1 and CIR2 are initialized to 0 by reset.

Table 3-12. Clear Interrupt Register (CIR)- $000B

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000B	Clear Interrupt Register (CIR)	Clear Interrupt Flag PA1 (EIR7)	Clear Interrupt Flag PA4 (EIR6)	Clear Interrupt Flag PD7 (EIR5)	Clear Interrupt Flag PA7 (SIR5)	Clear Interrupt Flag PA3 (SIR6)	ES4 Fast	RAM Segment Select Bit 1 (CI1)	RAM Segment Select Bit 0 (CI0)

Bits 0-1: Extended Page 0 RAM Segment Select. These bits establish the base address in page 1 for mapping the 64-byte page 0 RAM. The page 0 address is $0040-$007F. Except for managing these two base address bits, the page 1 mapping is transparent to the application software. This allows up to four page 0 segments (256 bytes total - stack allowance) to be accessed using short page 0 addressing instructions. Allowance must be made for the number of items that can be placed in the stack (normally starting at $01FF and working downward). These bits can be set or reset by the CPU writing to address $000B. They can be monitored by the CPU reading address $000B. Reset initializes both bits to zero.

Bit 1	Bit 0	Page 1 Base Address
0	0	$0100
0	1	$0140
1	0	$0180
1	1	$01C0

Bit 2: ES4 Expansion Bus FAST Memory Cycle. Enables ES3 Expansion Bus Addresses and ES4 Expansion Bus Addresses to operate in a fast ø2 memory cycle. When CIR2 is a logic 0 ES3 expansion bus addresses and the top half of ES4 expansion bus addresses operate at slow speed requiring two Ø2 cycles per memory operation. This bit can be set or reset by the CPU writing to address $000B. The CPU can monitor the bit by reading address $000B. The bit is initialized to zero by reset.

Bit 3: Clear PA3 Interrupt Flag. Writing a logic 0 to this bit position resets the PA3 Interrupt Flag (SIR6) to a logic 0. Writing a logic 1 to this bit position has no effect. Reading this bit position always returns a 1.

Bit 4: Clear PA7 Interrupt Flag. Writing a logic 0 to this bit position resets the PA7 Interrupt Flag (SIR5) to a logic 0. Writing a logic 1 to this bit position has no effect. Reading this bit position always returns a 1.

Bit 5: Clear PD7 Interrupt Flag. Writing a logic 0 to this bit position resets the PD7 Interrupt Flag (EIR5) to a logic 0. Writing a logic 1 to this bit position has no effect. Reading this bit position always returns a 1.

Bit 6: Clear PA4 Interrupt Flag. Writing a logic 0 to this bit position resets the PA4 Interrupt Flag (EIR6) to a logic 0. Writing a logic 1 to this bit position has no effect. Reading this bit position always returns a 1.

Bit 7: Clear PA1 Interrupt Flag. Writing a logic 0 to this bit position resets the PA1 Interrupt Flag (EIR7) to a logic 0. Writing a logic 1 to this bit position has no effect. Reading this bit position always returns a 1.

3.10. COUNTER/TIMERS

There are two separate 16-bit counter/timer systems in the MCU: Counter/Timer A (called Timer A) and Counter/Timer B (called Timer B). Timer A operates in one of four modes and can drive an output port. Timer B operates only in the interval timer mode with no output port option. Otherwise, operation of the two counter/timers is similar except for register addresses, the generated IRQ (and priority level) and the interfacing I/O port. The operation of Timer A is described in detail followed by a description of Timer B differences. Block diagrams of Timer A and Timer B are shown in Figures 3-8 and 3-9, respectively.

A divide-by-32 counter connected to Ø2 clock is shared by both timers. The counter provides a Ø2/32 clock that can be individually selected by each timer.

3.10.1. Timer A Registers

Timer A is composed of a 16-bit latch, a 16-bit counter and an 8-bit snapshot register (Figure 3-8). The latch consists of two 8-bit registers, Timer A Upper Latch (TAUL) and Timer A Lower Latch (TALL). The counter also consists of two 8-bit registers, Timer A Upper Counter (TAUC) and Timer A Lower counter (TALC). The snapshot register is referred as Timer A Snapshot (TAS). Timer A operation is controlled and monitored using the Timer A Mode Register (Table 3-13).

TALL is loaded by the CPU writing to address $0011. TAUL can be loaded by writing to either $0012 or $0013. When the CPU writes to address $0013, the contents of TALL and TAUL are also downloaded into TALC and TAUC, respectively, and the Timer A Interrupt Flag (TAM7) is cleared. The contents of TALC can be monitored at any time by reading $0011. Reading $0011 also causes the contents of TAUC to transfer into TAS. The contents of TAS can be monitored by reading either $0012 or $0013.

When Timer A underflows, the Timer A Interrupt Flag bit in the (TAM7) is set to a logic 1. This bit can be used to assert IRQ5.

3.10.2. Timer B Registers

Timer B is to Timer A except only the interval timer mode is supported (Figure 3-9). Timer B registers are located at $0014-$0017. When the Timer B Underflow Flag is set (TBM7) and enabled (TBM5 and TBM6), IRQ3 is asserted. Timer B interfaces with I/O port PB0 rather than PA0.

Timer B is composed of a 16-bit latch, a 16-bit counter and an 8-bit snapshot register. The latch consists of two 8-bit registers, Timer B Upper Latch (TBUL) and Timer B Lower Latch (TBLL). The counter also consists of two 8-bit registers, Timer B Upper Counter (TBUC) and Timer B Lower counter (TBLC). The snapshot register is referred as Timer B Snapshot (TBS).

TBLL is loaded by the CPU writing to address $0015. TBUL can be loaded by writing to either $0016 or $0017. When the CPU writes to address $0017, the contents of TBLL and TBUL are also downloaded into TBLC and TBUC, respectively, and the Timer B Interrupt Flag (TBM7) is cleared. The contents of TBLC can be monitored at any time by reading $0015. Reading $0015 also causes the contents of TBUC to transfer into TBS. The contents of TBS can be monitored by reading either $0016 or $0017.

When Timer B underflows, the Timer B Interrupt Flag bit in the (TBM7) is set to a logic 1. This bit can be used to assert IRQ3.

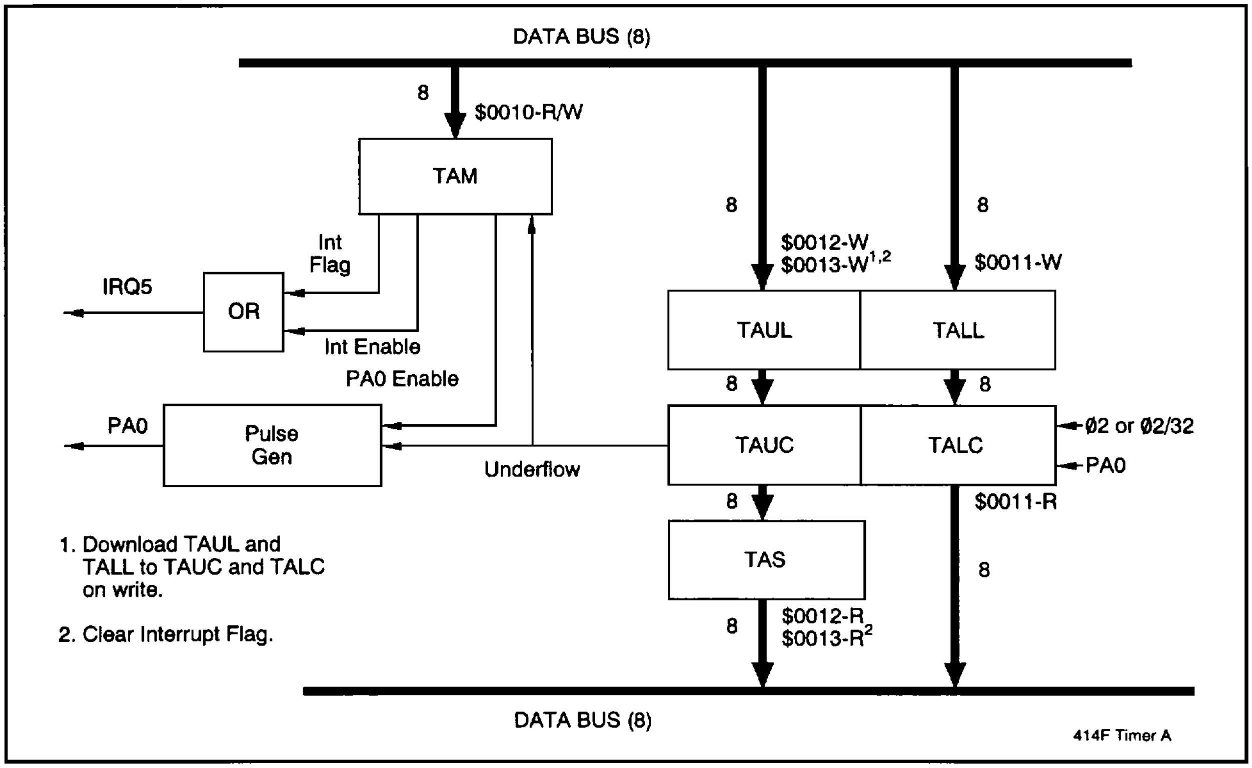


Figure 3-8. Counter/Timer A Block Diagram

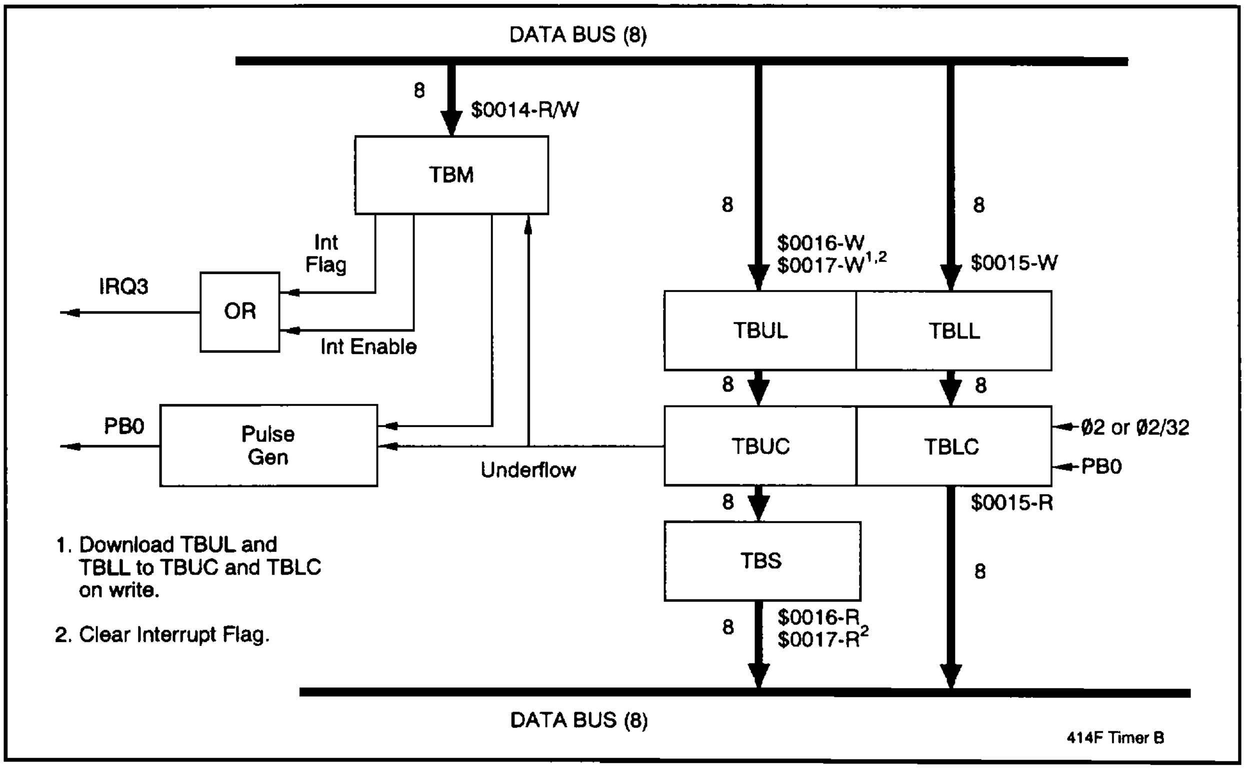


Figure 3-9 . Counter/Timer B Block Diagram

3.10.3. Timer A Mode Register (TAM)

The Timer A Mode Register (TAM) selects the Timer A operating mode selection, and controls and reports the Timer A interrupt (Table 3-13). Bits 0-2, 5, and 6 are cleared to zero by reset, and can be reset or set by the CPU writing to address $0010. Bits 0-2, and 5-7 can be read by the CPU.

Table 3-13. Register Bit Assignments - 0010h - 0013h

Addr.	Function	Bit 7	6	5	4	3	2	1	0
0010	Timer A Mode (TAM)	Timer A Interrupt Flag	Timer A Interrupt Enable	Timer A Vector Select	Not Used		Timer A Div by 32 Prescale	Timer A Mode Bit 1 (TAM1)	Timer A Mode Bit 0 (TAM0)
0011	Timer A Lower Latch	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0012	Timer A Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8
0013	Timer A Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8

Bits 0-1: **Timer A Mode Select.** These two bits select the Timer A operating mode. The interval timer mode is selected upon reset since these bits are reset to logic 0.

Bit 1	Bit 0	Mode
0	0	Interval Timer
0	1	Pulse Generator
1	0	Event Counter
1	1	Pulse Width Measurement

Bits 2: **Timer A Divide by 32.** When set to a logic 1, the Timer A ø2 clock is divided by 32. When reset to a logic 0, the Timer A ø2 clock is not divided by 32.

Bits 3-4: **Not used.**

Bit 5: **Timer A IRQ5 RAM Vector Enable.** When this bit is a logic 1 and the Timer A Interrupt Enable (TAM6) is a logic 1, IRQ5 is asserted through the Timer A IRQ5 RAM vector. When this bit is a logic 0 and the Timer A Interrupt Enable (TAM6) is a logic 1, IRQ5 is asserted through the Timer A IRQ5 ROM vector.

Bit 6: **Timer A Interrupt Enable.** When bit 6 is a logic 1, IRQ5 is asserted when the Timer A Interrupt Flag (TAM7) is set to a logic 1. When this bit is a logic 0, IRQ5 will not be asserted based on TAM7.

Bit 7: **Timer A Interrupt Flag.** This bit is set to logic 1 when the Timer A counter underflows, i.e., decrements from 0 to - 1 (0000 to $FFFF). Reading or writing $0013 clears the Timer A Interrupt Flag (TAM7).

3.10.4. Timer B Mode Register (TBM)

The Timer B Mode Register (TBM) controls and reports the Timer B interrupt (Table 3-14). Bits 0-2, 5, and 6 are cleared to zero by reset, and can be reset or set by the CPU writing to address $0014. Bits 0-2, and 5-7 can be-read by the CPU.

Table 3-14. Register Bit Assignments - 0014h - 0017h

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0014	Timer B Mode (TBM)	Timer B Interrupt Flag	Timer B Interrupt Enable	Timer B Vector Select	Not Used		Timer B Div by 32 Prescale	0	0
0015	Timer B Latch Low	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0016	Timer B Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8
0017	Timer B Upper Latch	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8

Bits 0-1: Not Used.

Bits 2: **Timer B Divide by 32.** When set to a logic 1, the Timer B ø2 clock is divided by 32. When reset to a logic 0, the Timer B ø2 clock is not divided by 32.

Bits 3-4: Not used.

Bit 5: **Timer B IRQ3 RAM Vector Enable.** When this bit is a logic 1 and the Timer B Interrupt Enable (TBM6) is a logic 1, IRQ3 is asserted through the Timer B IRQ3 RAM vector. When this bit is a logic 0 and the Timer B Interrupt Enable (TBM6) is a logic 1, IRQ3 is asserted through the Timer B IRQ3 ROM vector.

Bit 6: **Timer B Interrupt Enable.** When bit 6 is a logic 1, IRQ3 is asserted when the Timer B Interrupt Flag (TBM7) is set to a logic 1. When this bit is a logic 0, IRQ3 will not be asserted based on TBM7.

Bit 7: **Timer B Interrupt Flag.** This bit is set to logic 1 when the Timer B counter underflows, i.e., decrements from 0 to - 1 (0000 to $FFFF). Reading $0017 clears the Timer B Interrupt Flag (TBM7).

3.10.5. Timer Modes

Since mode operation of both counter/timers is similar, mode operation is described for Timer A with Timer B operation indicated in parentheses. The waveforms for the four timer modes are illustrated in Figures 3-10 through 3-13.

3.10.5.1. Mode 0 - Interval Timer

Writing to TAUL (TBUL) transfers the 16-bit latch value to the counter. The counter counts down at the Ø2 or Ø2/32 rate. When the counter counts through zero, the TAIF (TBIF) is set to a 1, the value in the latches is transferred to the counter and the counter continues to count down. (See Figure 3-10.)

3.10.5.2. Mode 1 - Pulse Generation

The PAD0 (PBD0) direction register bit must be set to a 1 to establish PA0 (PB0) as an output pin before starting this mode. Writing to TAUL (TBUL) forces the PA0 (PB0) output low and starts the timer. Each time the timer counts through zero, the PA0 (PB0) output changes state to generate a square wave at a rate dependent upon the value loaded into the latches. The timer counts at either the Ø2 or Ø2/32 rate. Each time the counter counts through zero, the latch values are automatically transferred to the timer registers and the TAIF (TBIF) is set to a 1. (See Figure 3-11.)

3.10.5.3. Mode 2 - Event Counter

The PAD0 (PBD0) direction register bit must be set to 0 to establish PA0 (PB0) as an input pin. The TAM2 (TBM2) clock divide-by-32 bit must be set to a 0 to select divide-by-1. The counter is initialized with the latch value when the TAUL (TBUL) value is written to address $0013 ($0017). The timer decrements by 1 at each positive transition on input port PA0 (PB0). TAIF (TBIF) is set to a 1 when the counter counts through zero. At the same time the latch value is reloaded into the counter. The maximum rate of the signal of PA0 (PB0) is one-half the timer clock rate. (See Figure 3-12.)

3.10.5.4. Mode 3 - Pulse Width Measurement

The PAD0 (PBD0) direction register bit must be set to an 0 to establish PA0 (PB0) as an input pin. Writing to TAUL (TBUL) at $0013 ($0017) transfers the 16-bit latch value to the counter. The value in the timer is decremented at the Ø2 or Ø2/32 rate when the PA0 (PB0) signal is low. Each time the PA0 (PB0) signal goes high, the counter stops and then continues when the signal is low again. If the counter counts through zero, TAIF (TBIF) is set to a 1 and the latch value transfers to reinitialize the counter. The countdown continues as long as PA0 (PB0) is low. (See Figure 3-13.)

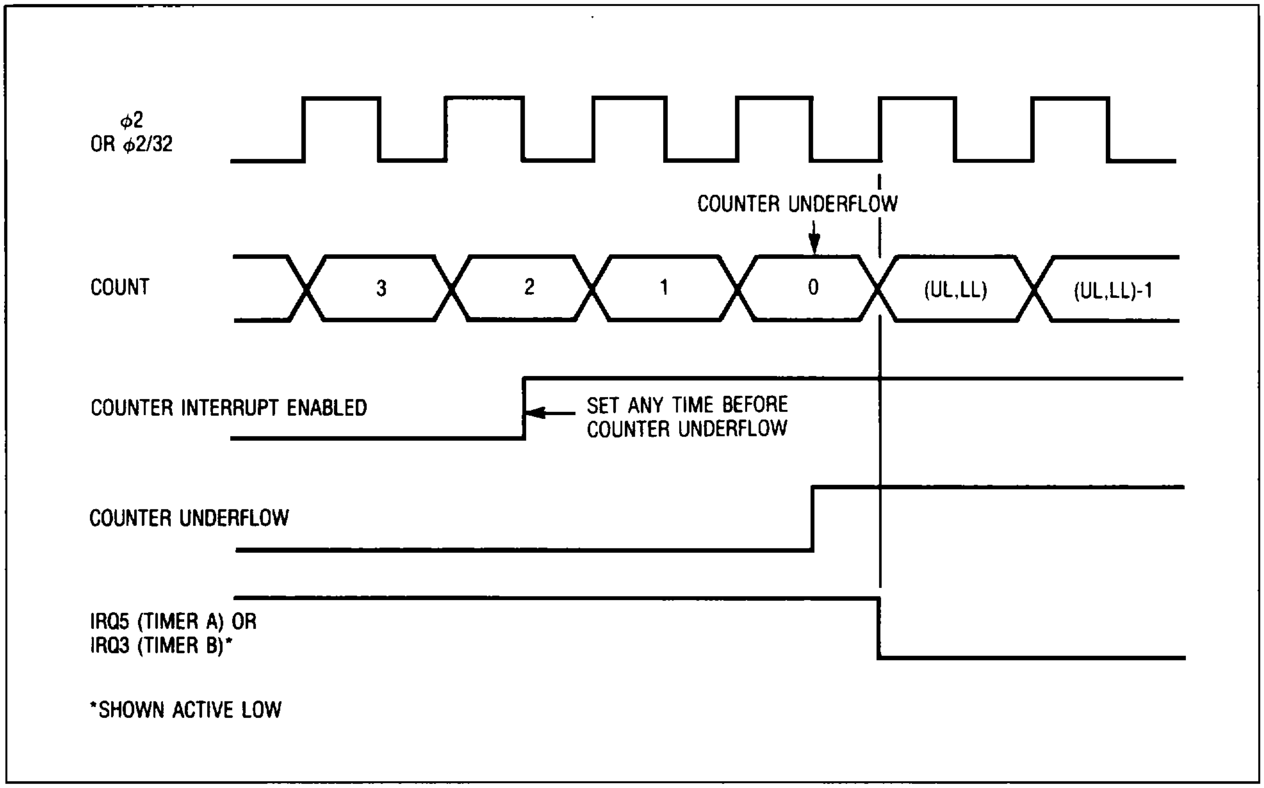


Figure 3-10. Interval Timer (Mode 0) Waveforms

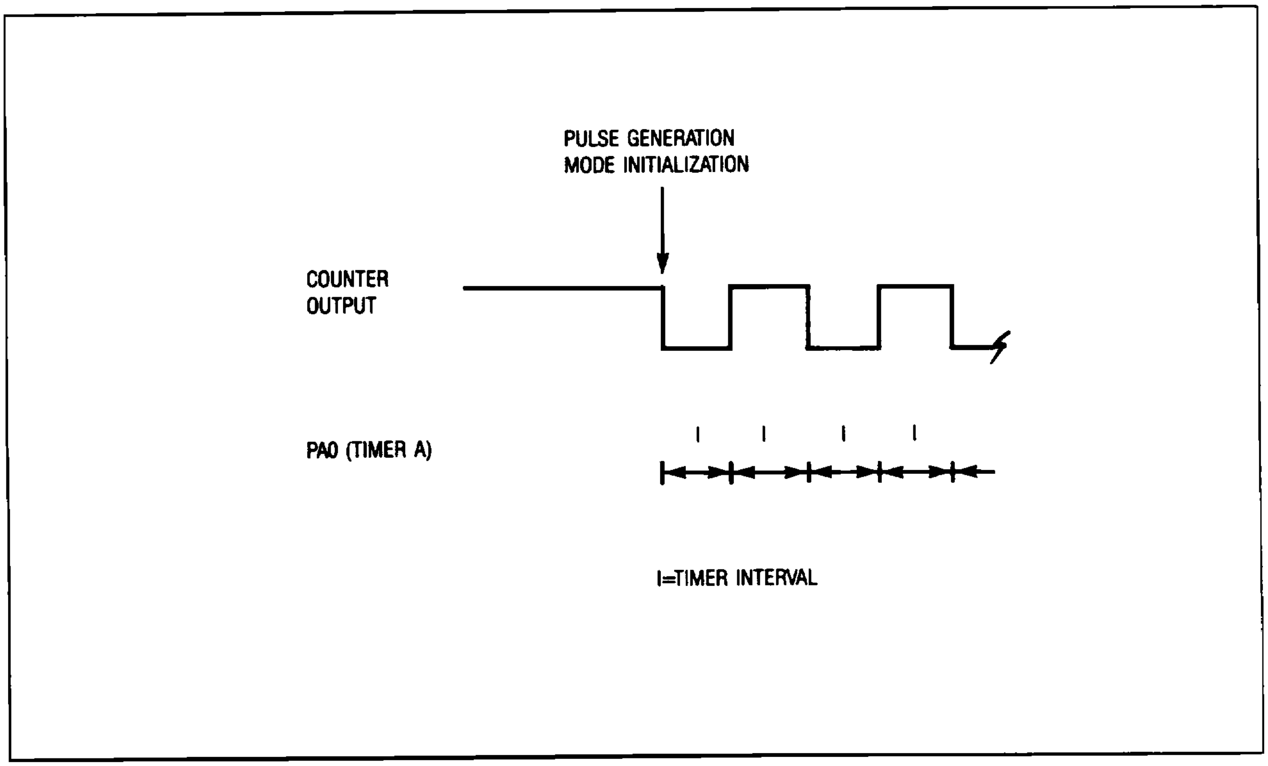


Figure 3-11. Pulse Generator (Mode 1) Waveforms

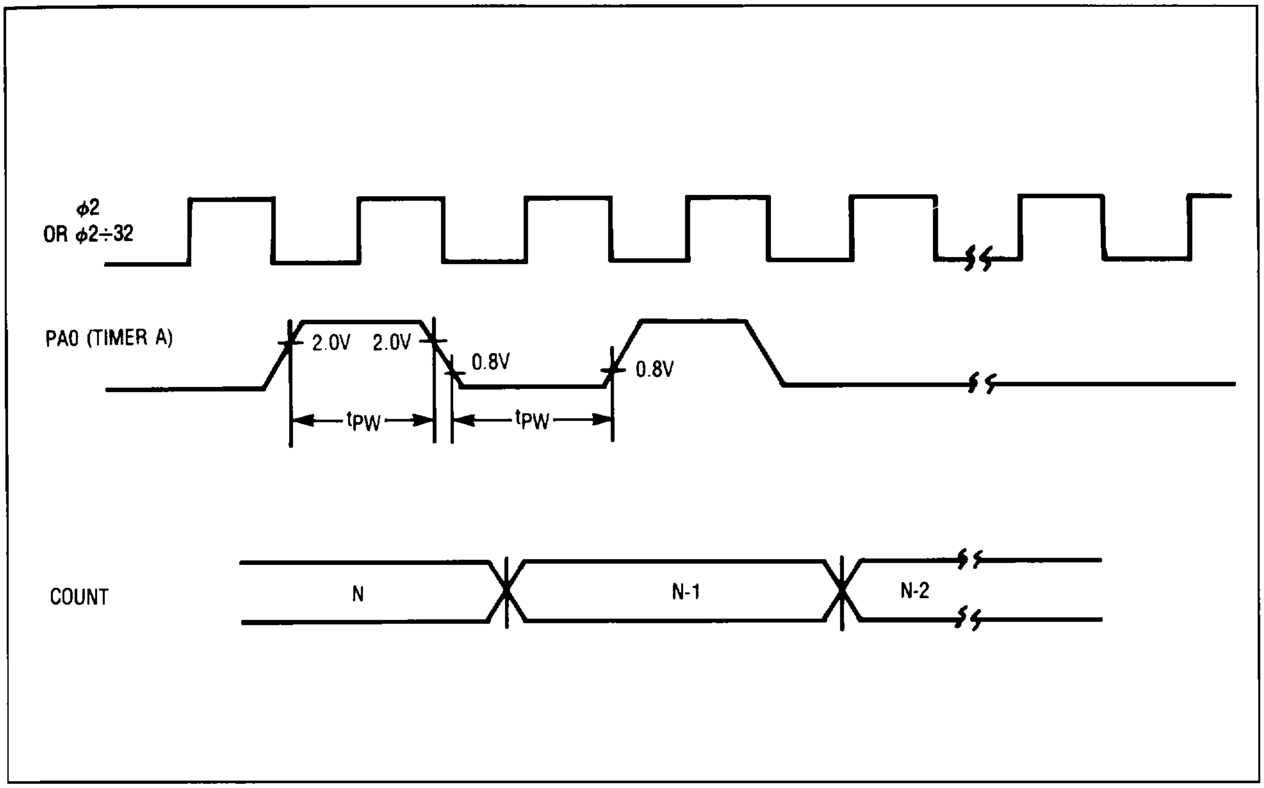


Figure 3-12. Event Counter (Mode 2) Waveforms

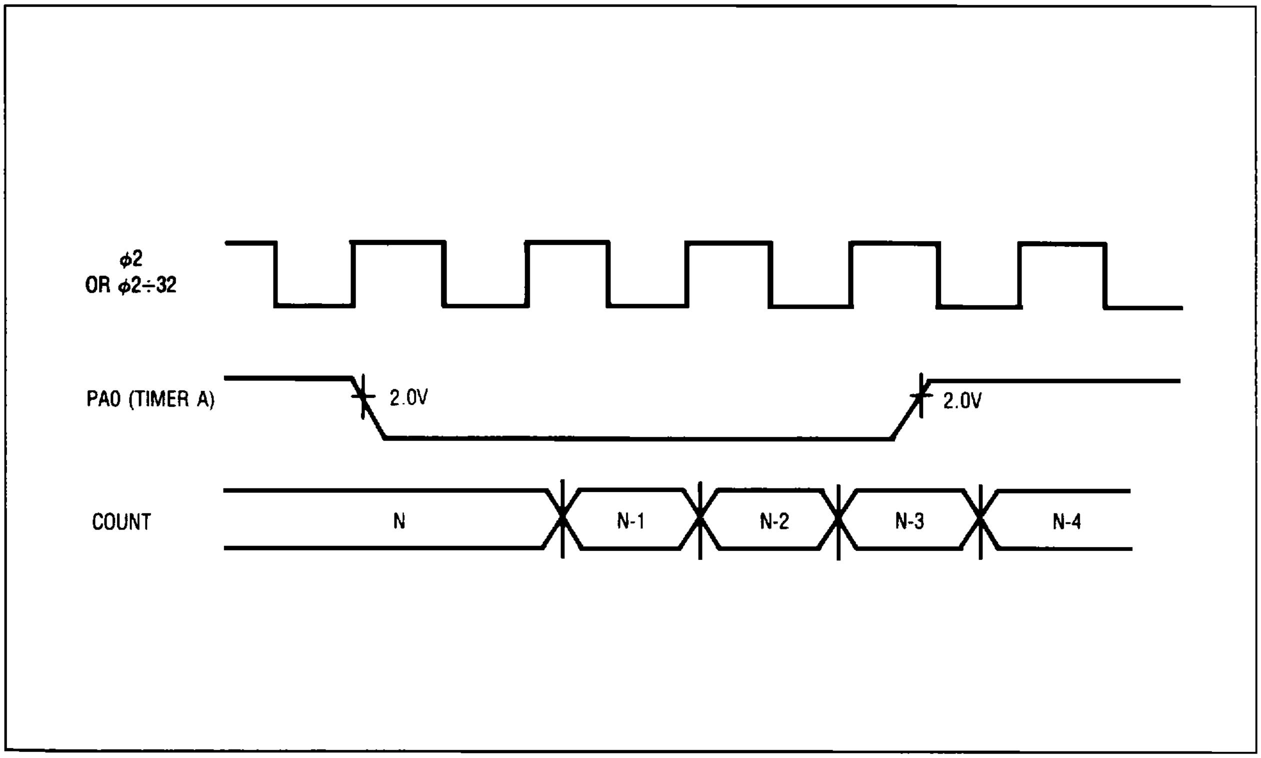


Figure 3-13. Pulse Width Measurement (Mode 3) Waveforms

3.11. PRECISION TIME GENERATORS

There are two identical 17-bit precision time generators: Precision Time Generator A (PTGA) and Precision Time Generator B (PTGB). Each PTG can be used for such functions as timing event interrupts, generating an external pulse train or as a source for synchronous USART timing.

Only PTGA is discussed in detail since both precision timer generators are identical in structure. Only the differences in I/O port addresses and IRQ interfaces are described. Block diagrams of PTGA and PTGB are shown in Figures 3-14 and 3-15, respectively.

3.11.1. Precision Time Generator A

PTGA consists of five 8-bit registers and a 17-bit pulse accumulator (Figure 3-14). The three input registers—PTGA Buffer (PAB), PTGA Lower Latch (PALL) and PTGA Upper Latch (PAUL)—are all 8-bit. There are two output registers: an 8-bit PTGA Lower Residue (PALR) and a 9-bit PTGA Upper Residue (PAUR). The PTGA Accumulator (PAAC)is 17-bits long. Operation is controlled by the PTGA Mode Register (PAM) located at $0034.

The CPU can read or write the contents of PAB using address $0035. The CPU can read or write the contents of PAUL at either address $0036 or $0037. Whenever the CPU writes to $0036 or $0037 the contents of PAB are transferred to PALL. This allows a simultaneous 16-bit update of the input latches. The 17th input bit to the pulse accumulator is always a logic 0. When the CPU writes to address $0037, PAB is transferred to PALL and the new contents of PALL and PAUL are downloaded into PALR and PAUR, respectively, and the most significant bit of PAUR is set to a logic 0. This feature is particularly helpful during testing.

Operation of the precision time generator is governed by the equation:

$$\text{Rate} = \text{Latch}*(Ø2/2^{17})$$

where:

Rate = Pulse rate in Hz

Latch = Latch value

Ø2 = Internal clock rate in Hz

For example, if Ø2 = 4 MHz and the latch is loaded with 7550 ($107E), the resulting rate is 230408 Hz.

Conversely. the latch value can be computed using the equation

Latch = Rate*(217/Ø2)

For example, if the desired rate = 342857 Hz, ø2 = 6 MHz , the required latch value is 7489.8 ($1D42).

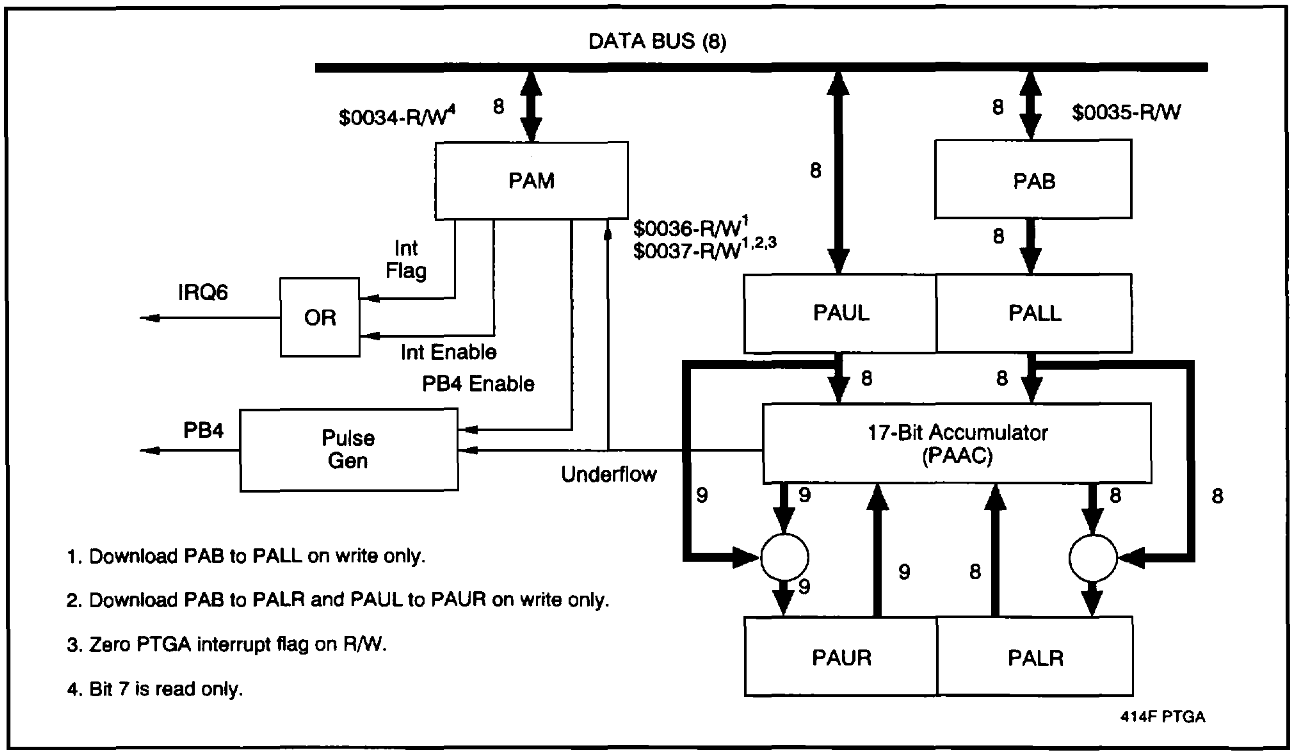


Figure 3-14. Precision Time Generator A Block Diagram

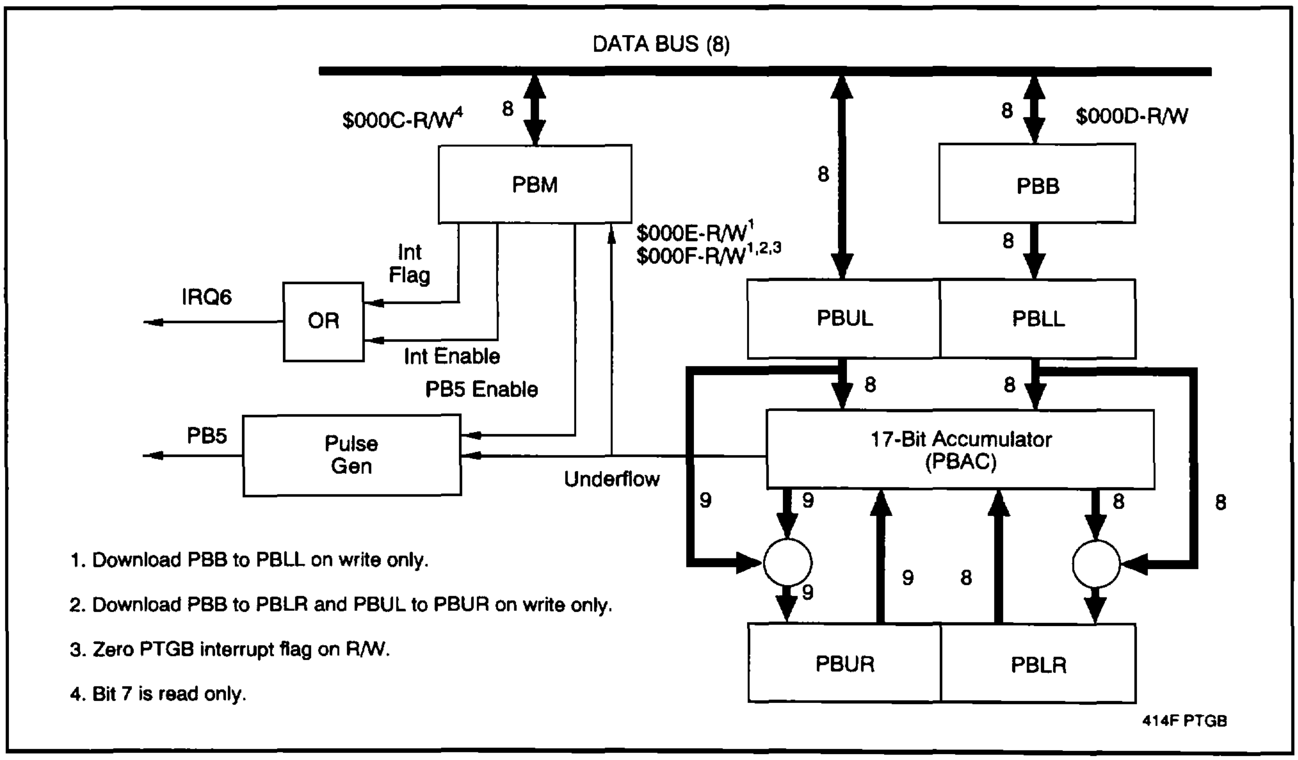


Figure 3-15. Precision Time Generator B Block Diagram

3.11.2. PTGA Mode Register (PAM)

The PTGA Mode Register (PAM) selects the PTGA timer and port options, and controls and reports the PTGA interrupt (Table 3-15). Bits 0, 1, and 6 are cleared by reset and can be set to a logic 1 or 0 by writing to address $0037. All bits can be read by the CPU.

Table 3-15. Register Bit Assignments - PTGA - 0034

		Bit							
Addr.	**Function**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0034	Precision Time Generator A (PTG A) Mode (PAM)	PTG A Interrupt Flag	PTG A Interrupt Enable	Not Used					PTGA Timer Mode

Bit 0: **PTGA Timer Mode Select.** When set to a logic 1, PTGA operates as a timer. When set to a logic 0, PTGA operates as a precision time generator.

Bit 1-5: **Not used.**

Bit 6: **PTGA Interrupt Enable.** When bit 6 is a logic 1, IRQ6 is asserted when the PRM A Interrupt Flag (PAM7) is set to a logic 1. Note that PTGB can also generate IRQ6. If both precision time generator interrupts are enabled, the IRQ6 interrupt service subroutine should examine the interrupt flag bit in both PTGA and PTGB mode registers to determine the IRQ6 source.

Bit 7: **PTGA Interrupt Flag.** This bit is set to logic 1 when the PTGA accumulator overflows. Reading or writing to address $0037 clears the PTGA Interrupt Flag (PAM7). Bit 7 is read only.

3.11.3. Precision Time Generator B

PTGB consists of five 8-bit registers and a 17-bit pulse accumulator (Figure 3-15). The three input registers—PTGB Buffer (PBB), PTGB Lower Latch (PBLL) and PTGB Upper Latch (PBUL)—are all 8-bit. There are two output registers: an 8-bit PTGB Lower Residue (PBLR) and a 9-bit PTGB Upper Residue (PBUR). The PTGB Accumulator (PBAC) is 17-bits long. Operation is controlled by the PTGB Mode Register (PBM) located at $000F.

Operation of PTGB is identical to PTGA with the exception of register addresses, and the port B interface line (Figure 3-15).

3.11.4. PTGB Mode Register (PBM)

The PTGB Mode Register (PBM) selects the PTGB timer and port options, and controls and reports the PTGB interrupt (Table 3-16). Bits 0, 1, and 6 are cleared by reset and can be set to a logic 1 or 0 by writing to address $001C. All bits can be read by the CPU. Bit 7 is read only.

Table 3-16. Register Bit Assignments - PTGB - 000Ch

Addr.	Function	Bit 7	6	5	4	3	2	1	0
000C	Precision Time Generator B (PTG B) Mode (PBM)	PTG B Interrupt Flag	PTG B Interrupt Enable	Not Used					PTG B Timer Mode

Bit 0: **PTGB Timer Mode Select.** When set to a logic 1, PTGB operates as a timer. When set to a logic 0, PTGB operates as a precision time generator.

Bit 1-5: **Not used.**

Bit 6: **PTGB Interrupt Enable.** When bit 6 is a logic 1, IRQ6 is asserted when the PRM B Interrupt Flag (PBM7) is set to a logic 1. Note that PTGA can also generate IRQ6. If both precision time generator interrupts are enabled, the IRQ6 interrupt service subroutine should examine the interrupt flag bit in both PTGA and PTGB mode registers to determine the IRQ6 source.

Bit 7: **PTGB Interrupt Flag.** This bit is set to logic 1 when the PTGB accumulator overflows. Reading or writing to address $001F clears the PTGB Interrupt Flag (PBM7).

3.11.5. Example Rates

Some examples of standard rates are shown in Table 3-17.

Table 3-17. PTGA or PTGB Generated Standard Data Rates

Rate	Ø2 = 6 MHz Latch (Hex)	Ø2 = 6 MHz Actual	Ø2 =8 MHz Latch (Hex)	Ø2 =8 MHz Actual	Ø2 = 10 MHz Latch (Hex)	Ø2 = 10 MHz Actual
576 KHz	3127	576004.03 Hz	24DD	575988.77 Hz		Hz
500 KHz	2AAB	500015.26 Hz	2000	500000.00 Hz		Hz
250 KHz	1555	249984.74 Hz	1000	250000.00 Hz		Hz
230.4 KHz	13A9	230392.46 Hz	0EBF	230407.71 Hz		Hz
200 KHz	1111	199996.95 Hz	0CCD	200012.21 Hz		Hz
100 KHz	0889	100021.36 Hz	0666	99975.59 Hz		Hz

3.12. USART

The MCU provides a full-duplex serial universal synchronous/asynchronous receiver/transmitter (USART) interface with programmable operating modes and data rates. Serial-to-parallel conversion is performed on data characters received from an external device and parallel-to-serial conversion is performed on data characters received from the MCU internal data bus. A block diagram of the USART is shown in Figure 3-16.

3.12.1. General Operation

Internal timing for both asynchronous and synchronous operation can be referenced to either Timer B or the Precision Timing Generators under software control. Synchronous transmit data (TXD) timing can also be derived externally by an external transmit clock (TXCLK) input on PA3 or an external transmit reference clock (TXREF) input on PA4. Synchronous received data (RXD) timing can be generated from an external receive clock (RXCLK) input on PA7. Note that the direction registers for PA1 through PA7 (PAD1 - PAD7) must be set correctly for the mode selected. Table 3-18 shows how standard data rates can be generated internally using either Timer B or the Precision Timing Generators A and B.

The serial interface registers are located at addresses $0034-$003F (Table 3-19). The CPU may read or write any of the serial interface registers with the exception of Serial Out Divider Latch (SODL) and Serial In Divider Latch (SIDL) which are write only. The Serial Status Register is read-only. Reading and/or writing to some of the registers also causes clearing of interrupt bits or data downloading actions.

3.12.2. Internal Timing

Since internal timing for TXD and RXD is similar, the following discussion covers only TXD timing. It differs only when precision timing generators (PTGs) are selected. TXD uses PTGB and RXD uses PTGA.

Case 1 - Asynchronous Timer B. Whenever short stop bits are selected (SFR0 = 1 or SFR1 = 1), or 5-bit operation is selected (SLCR0 = 0 and SLCR1 = 0), the user must program the SOUT (RXD) Divider Latch (SODL) to $0F. This restriction does not apply to the SIN (TXD) Divider Latch (SIDL).

$$UIB = øB/[(n + 1)(l + 1)]$$

where UIB is the TXD bit rate, øB is the internal clock rate of Timer B, n is the decimal value loaded into the Timer B Latch, and l is the decimal value loaded into the SIDL latch. If ø2 = 6 MHz and the DIV BY 32 option for Timer B is not selected, øB = 6 MHz. If n = 155 ($009B) and l = 15 ($0F), then

$$UIB = 6\ MHz/[(155 + 1)(15 + 1)] = 2403.85\ Hz.$$

Case 2 - Synchronous Timer B. An additional DIV BY 2 is required to generate the 50% duty cycle TXCLK (PA3) required for synchronous operation. Using the same values as in Case 1,

$$UIB = øB/[2(n + 1)(l + 1)] = 6\ MHz/[2\ (155 + 1)(15 + 1)] = 1201.92\ Hz$$

Case 3 - Asynchronous PTGB. Assume that PTGB is generating a rate of 230.4 KHz and that the ø2 internal timing is 6 MHz. From Table 3-18, the PTGB latch is loaded with $13A9. Also, from Table 3-18, PTGB = 230.39246 KHz. If l = 15 ($0F), then:

$$UIB = PTGB/\{[3(l + 1)]\} = 230392.46/[3\ (15 + 1)] = 4799.84\ Hz$$

This assumes that the USART DIV BY 2 mask option (Figure 3-16) is selected. If short stop bits or 5-bit operation is selected, the user must program the SOUT Divider Latch (SODL) to decimal 15 ($0F).

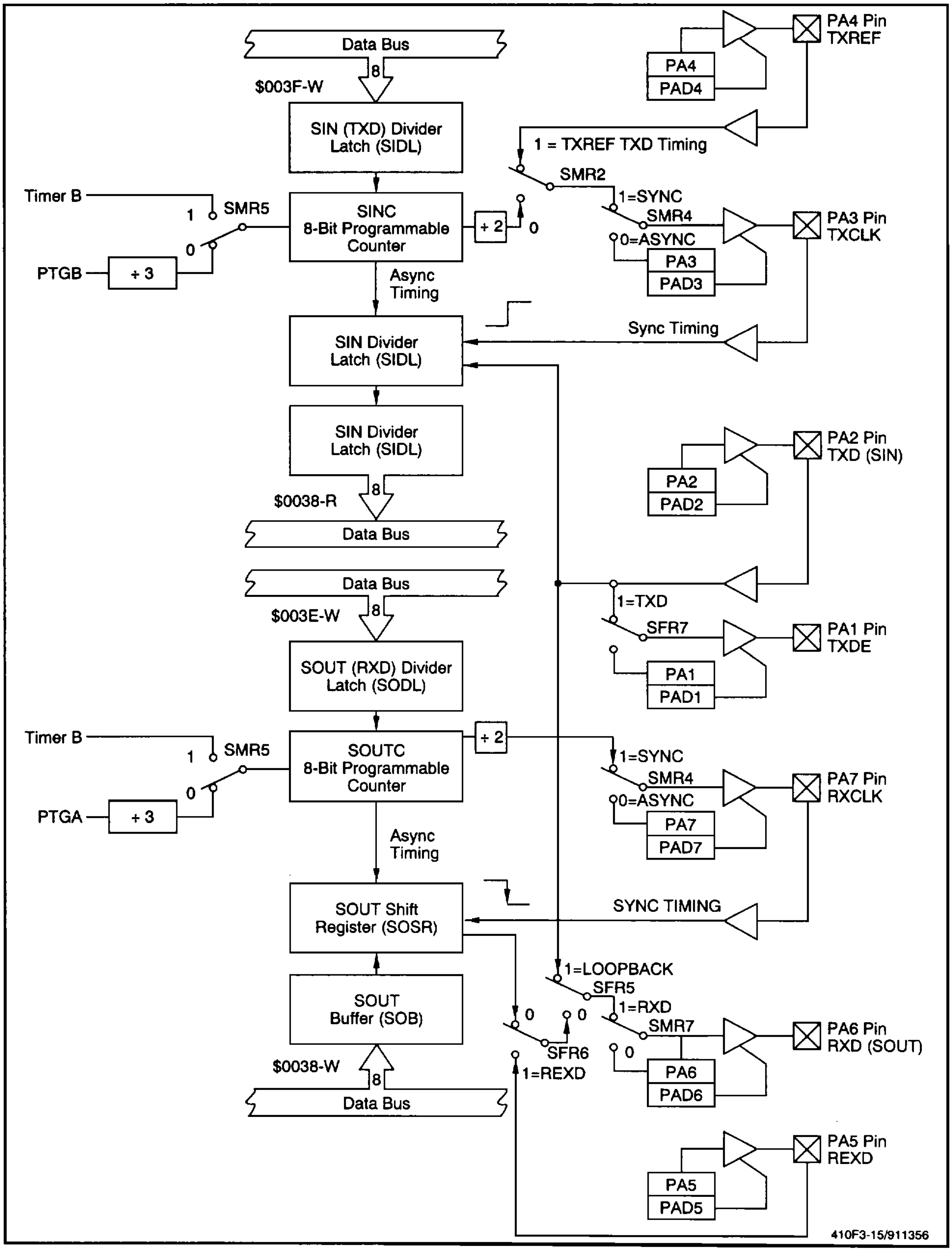


Figure 3-16. USART Block Diagram

Table 3-18. USART Generated Standard Data Rates

Standard	Asynchronous, Ø2 = 6 MHz (SIDL = SODL = $06)				Synchronous, Ø2 = 6 MHz			
	Timer B		PTGA and PTGB		TIMB Latch = 009B, Rate = 38461.54 Hz PTG Rate = 230.4 KHz, PTG Latches = $13A9			
Data Rate	TIMB Latch	Bit Rate	PTG Latch	Bit Rate	SIDL, SODL	Bit Rate	SIDL, SODL	Bit Rate
50 Hz	$1D4B	50.00	$0034	49.59	–	–	–	–
75 Hz	$1387	75.00	$004F	75.34	$FF	75.12	–	–
110 Hz	$0D50	110.00	$0073	109.76	–	–	–	–
150 Hz	$09C3	150.00	$009D	149.73	$7F	150.24	$FF	150.00
300 Hz	$04E1	300.00	$013B	300.41	$3F	300.48	$7F	299.99
600 Hz	$0270	600.00	$0275	599.86	$1F	600.96	$3F	599.98
1200 Hz	$0137	1201.92	$04EA	1199.72	$0F	1201.92	$1F	1199.96
2400 Hz	$009B	2403.85	$09D5	2400.40	$07	2403.85	$0F	2399.92
4800 Hz	$004D	4807.69	$13A9	4799.84	$03	4807.69	$07	4799.84
9600 Hz	$0026	9615.38	$2752	9599.69	$01	9615.38	$03	9599.69
14400 Hz	$0019	14423.08	$3AFB	14399.53	–	–	–	–
19200 Hz	$0013	18750.00	$4EA5	19200.32	$00	19230.77	$01	19199.37
							$00	38398.74

Case 4 - Synchronous PTGB. An extra DIV BY 2 also occurs in the synchronous mode. Using the same setup as in Case 3 and again assuming that the USART DIV BY 2 mask option (Figure 3-16) is selected.

UIB = PTGB/2[3 (I + 1)]= 230392.46/[6 (15 + 1)]= 2399.92 Hz.

3.12.3. USART Registers and Serial Buffer Registers (SB)

The USART control and status registers are shown in Table 3-19. The serial buffer (SB) registers provide double buffering for serial in and serial out data. Both buffers are located at address $0038. The Serial In Buffer is a read-only register and the Serial Out Buffer is a write-only register. All data is shifted least significant bit first. When odd or even parity is used with 5-, 6- or 7-bit character operation, the unused most significant bits in the Serial Out Buffer must be loaded with zeros. Zeros are automatically inserted in the Serial In Buffer.

Table 3-19. Register Bit Assignments - USART - 0039h - 003Fh

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0034	Precision Time Generator A (PTG A) Mode (PAM)	PTG A Interrupt Flag	PTG A Interrupt Enable	Not Used					PTGA Timer Mode
0038	Serial In Buffer (SIB) / Serial Out Buffer (SOB)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0039	Serial Interrupt Register (SIR)	TXD Status Interrupt Flag	TXCLK (PA3) ↑ Interrupt Flag	RXCLK (PA7) ↓ Interrupt Flag	TXCLK (PA3)↑ Interrupt Enable	RXCLK (PA7) ↓ Interrupt Enable	TXD Status Interrupt Enable	RXD Buf Empty Interrupt Enable (BE)	RXD Buf Full Interrupt Enable (BF)
003A	Serial Mode Register (SMR)	RXD On	TXD On	Timing Select 0 = PRGs 1 = TIMB	Sync Mode	TXD Sync Bit	TXREF Clock Select	TXREF RLSDP Sync Enable	Not Used
003B	Serial Line Control Register (SLC)	Parity Stuff Bit	Set Break	Stuff Parity	Even Parity	Enable Parity	Two Stop Bits	Word Length Bit 1 (SL1)	Word Length Bit 0 (SL0)
003C	Serial Status Register (SSR)	TXD Parity Bit	RXD Underrun (UR)	RXD Buffer Empty (BE)	TXD Break Int (BI)	TXD Framing Error (FE)	TXD Parity Error (PE)	TXD Overrun Error (OE)	TXD Buffer Full (BF)
003D	Serial Form Register (SFR)	TXD/ TXDE Echo	REXD/ TXD Echo	TXD/ RXD Echo	TIMA Input TXD Test	TXD/ Edge TXD Test	Not Used	7/8 Short Stop Bit	3/4 Short Stop Bit
003E	SOUT (RXD) Divider Latch (SODL)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
003F	SIN (TXD) Divider Latch (SIDL)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0

3.12.4. Serial Mode Register (SMR)

The Serial Mode Register (SMR), located at $003A, controls basic serial mode and timing selection. All bits are cleared to zero by reset and can be set or reset by the CPU. Bits 6 and 7 enable the TXD and the RXD modes, respectively, for both asynchronous and synchronous modes of operation. Bits 2-4 control synchronous functions. Bits 2-4 must be set to zero for asynchronous operation.

Bits 0: Not used.

Bits 1: **CTSP/RLSDP Enable.** When set to a logic 1 and TXD Mode is selected (SMR6 = 1), the USART TXD synchronous mode word counter is initialized upon detection of a negative edge on PA0 (normally connected to CTSP). When set to a logic 1 and RXD Mode is selected (SMR7 = 1), the USART RXD synchronous mode word counter is initialized upon detection of a negative edge on PA4 (normally connected to RLSDP). When set to a logic 0, PA0 and PA4 are not used for USART support.

Bit 2: **Select TXREF Source.** A logic 1 selects the TXREF on PA4 clock for TXD timing. A logic 0 selects internal TXD timing (see Figure 3-16).

Bit 3: **Enable TXD Sync Detect.** When set to a logic 1, the TXD data line is monitored for a high-to-low (1-0) character transition. This transition causes serial in word synchronization following the 0 character and resets bit SMR3.

Bit 4: **Sync Mode Select.** A logic 1 selects synchronous mode operation; PA7 is assigned to RXCLK and PA3 is assigned to TXCLK. A logic 0 selects asynchronous mode operation; PA7 and PA3 are general purpose I/O pins.

Bit 5: **Internal Timing Reference.** A logic 1 selects Timer B for both TXD and RXD. A logic 0 selects Precision time Generator B for TXD and Precision Time Generator A for RXD.

Bit 6: **TXD Mode Select.** When set to a logic 1, the TXD timing and shift register are operational. When set to a logic 0, PA2 remains a general purpose I/O pin.

Bit 7: **RXD Mode Select.** When set to a logic 1, the RXD timing and shift register are operational. When set to a logic 0, PA6 remains a general purpose I/O pin.

3.12.5. Serial Interrupt Register (SIR)

The Serial Interrupt Register (SIR) is located at address $0039. The SIR contains five enable bits (bits 0-4) and three interrupt flag bits (bits 5-7). The CPU can read all bits but can write only to the five interrupt enable bits. All SIR bits are cleared to zero by reset. An interrupt enable bit, when set to a logic 1, permits the corresponding condition to assert the associated IRQ.

Bit 0: **TXD (Serial In) Buffer Full Interrupt Enable.** This bit, when a logic 1, enables IRQ4 to be asserted when the Serial In Buffer Full bit (SSR0) is a logic 1. When this bit is a logic 0, IRQ4 will not be asserted based on SSR0.

Bit 1: **RXD (Serial Out) Buffer Empty Interrupt Enable.** This bit, when is a logic 1, enables IRQ6 to be asserted when the Serial Out Buffer Empty bit (SSR5) is a logic 1. When this bit is a logic 0, IRQ6 will not be asserted based on SSR5.

Bit 2: **Serial In Status Interrupt Enable.** This bit, when a logic 1, enables IRQ5 to be asserted when the Serial In Status bit (SIR7) is a logic 1. When this bit is a logic 0, IRQ5 will not be asserted based on SIR7.

Bit 3: **PA7 Interrupt Enable.** This bit, when a logic 1, enables IRQ6 to be asserted when the PA7 Interrupt Flag (SIR5) is a logic 1. When this bit is a logic 0, IRQ6 will not be asserted based on SIR5.

Bit 4: **PA3 Interrupt Enable.** This bit, when a logic 1, enables IRQ4 to be asserted when the PA3 Interrupt Flag (SIR6) is a logic 1. When this bit is a logic 0, IRQ4 will not be asserted based on SIR6.

Bit 5: **PA7 Interrupt Flag.** This bit is set to a logic 1 when a high-to-low transition is detected on the PA7. RXCLK is connected to this pin during synchronous serial output operation. Writing a 0 to bit 4 of the Clear Interrupt Register clears this bit to a logic 0.

Bit 6: **PA3 Interrupt Flag.** When SFR3 = 0, this bit is set to a logic 1 when a low-to-high transition is detected on PA3. TXCLK is normally connected to this pin in synchronous serial input operation. When SFR3 = 1, this bit is set to a logic 1 when a low-to-high transition is detected on PA2 (TXD). Writing a 0 to bit 3 of the Clear Interrupt Register clears this bit to a logic 0.

Bit 7: **Serial In Status Interrupt Flag.** This bit is set to a logic 1 when any of the following three flags are set to a logic 1 in the Serial Status Register (SSR): Framing Error (SSR3), Parity Error (SSR2), or Overrun Error (SSR1). The Serial In Status Interrupt Flag (SIR7) is also set to a logic one whenever the Break Interrupt (SSR4) changes state, i.e., whenever it changes from a 0 to a 1 or from a 1 to a 0. SIR7 is reset by writing to the Serial Status Register (SSR) at address $003C. Writing to $003C clears SIR7 but does not alter any bits in the Serial Status Register (SSR).

3.12.6. Serial Line Control Register (SLCR)

The Serial Line Control Register (SLCR) at $003B specifies the word length and parity generation and checks in asynchronous mode. Each bit can be set or reset by the CPU. All SLCR bits are initialized to zero by reset. The SLCR must be set to $03 for 8-bit synchronous operation. The Parity Enable bit (SLCR3) must be a zero in the synchronous mode. Both asynchronous and synchronous modes support 5-, 6-, 7-, and 8-bit word lengths.

Bits 0-1: **Word Length.** These two bits specify the number of bits in each serial in or serial out character. The encoding of bits 0 and 1 is:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Whenever 5 bits are selected in the asynchronous mode the transmitter will generate 1 and 1/2 stop bits. This requires that the SOUT Divider Latch (SODL) be loaded with a decimal 15 ($0F).

Bit 2: **Number Stop Bits.** This bit specifies the number of stop bits in each serial out character. If bit 2 is a logic 0, one stop bit is generated regardless of word length. If bit 2 is a logic 1 when a 5-bit word length is selected, one and a half stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The serial in logic checks the first stop bit only regardless of the number of stop bits selected.

Bit 3: **Enable Parity.** When bit 3 is a logic 1, a parity bit is inserted in the serial out data stream and checked for in the serial in data stream. The parity bit is located between the last data bit and the first stop bit.

Bit 4: **Even Parity Select.** When parity is enabled (SLCR3 = 1) and parity stuff is disabled (SLCR5 = 0), a one or zero is automatically inserted into the serial out parity position such that the total number of ones in the data and parity fields is either odd (SLCR4 = 0) or even (SLCR4 = 1).

Bit 5: **Enable Parity Stuff.** When parity is enabled (SLCR3 = 1) and parity stuff is enabled (SLCR5 = 1), the parity stuff bit value (SLCR7) is copied into the serial out parity position.

Bit 6: **Set Break.** This bit is the Break Control bit. When this bit is set to a logic 1, the received data (RXD) output is forced to the space (logic 0) state. The break is disabled by setting this bit to a logic 0. The Break Control bit acts only on RXD and has no effect on the serial in logic.

Bit 7: **Parity Stuff Bit.** This bit is copied into the RXD parity bit when both parity is enabled (SLCR3 =1) and parity stuff is enabled (SLCR5 = 1).

3.12.7. Serial Status Register (SSR)

The Serial Status Register (SSR) at $003C provides serial-in and serial-out status to the CPU. It is a read-only register. All bits are initialized by reset to a logic 0, except Serial Out Buffer Empty (SSR5), which is initialized to a logic 1. Writing to the Serial Status Register will not alter any bits in the register, but it will reset the Serial In Status Interrupt Flag (SIR7).

Bit 0: **Serial In Buffer Full (BF).** This bit is set to a logic 1 whenever a complete incoming character, asynchronous or synchronous, has been received and transferred to the Serial In Buffer. Bit 0 is reset to a logic 0 when the CPU reads the Serial In Buffer.

Bit 1: **Overrun Error (OE).** This bit indicates that data in the Serial In Buffer was not read by the CPU before the next received character was transferred into the Serial In Buffer, thereby destroying the previous character. The OE bit is reset as soon as a received data character can be safely transferred into an empty Serial In Buffer.

Bit 2: **Parity Error (PE).** This bit indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (SLCR4). The PE bit is set to a logic 1 upon detection of a parity error. It is reset to a logic 0 as soon as a received data character is found with a correct parity bit.

Bit 3: **Framing Error (FE).** This bit indicates that the received character did not have a valid stop bit. The FE is set to a logic 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (space level). The FE bit is reset as soon as a received data character is found with a correct first stop bit.

Bit 4: **Break Interrupt (BI).** This bit is set to a logic 1 whenever the serial in received data input is held in the space (logic 0) state continuously from the start bit to the first stop bit. The BI bit is cleared when a mark bit (logic 1) is detected on TXD.

Bit 5: **Serial Out Buffer Empty (BE).** When this bit is set to a logic 1, it indicates that the Serial Out Buffer is ready to accept a new character for transmission. When this bit is true simultaneously with the Serial Out Interrupt Enable bit (SIR1), IRQ6 is asserted. The BE flag is set to a logic 1 when the contents of the Serial Out Buffer are transferred into the Serial Out Shift Register. BE is reset to a logic 0 when the CPU writes to the Serial Out Buffer.

Bit 6: **Serial Out Underrun (UR).** This bit is set to a logic 1 whenever the Serial Out Shift Register empties and the Serial Out Buffer has not been reloaded by the CPU. When the UR bit is a logic 1 the Serial Out Shift Register will output mark bits (logic 1). It is reset to a logic 0 when the CPU writes to the Serial Out Buffer.

Bit 7: **Serial In Parity Bit.** This bit copies the received serial in parity bit.

3.12.8. Serial Form Register (SFR)

The Serial Form Register (SFR), located at $003D, controls TXD testing and specifies special routing of serial signals and stop bit length adjustment. Bits 5-7 can support local and remote loopback operation. The CPU on read and write all SFR bits except bit 2.

Bits 0-1: **Short Stop Bits.** When set, these bits shorten the width of the final transmitter stop bit. A normal stop bit width occurs when both bits are set to 0. Stop bit control requires the user to load the Serial Out Divider Latch (SODL) with a decimal 15 ($0F).

Bit 1	Bit 0	Final Stop Bit Width 5-bit Word Length, 2 Stop Bit Mode	Final Stop Bit Width All Other Modes
0	0	1/2 Bit	1.0 Bit
0	1	1/4 Bit	3/4 Bit
1	0	3/8 Bit	7/8 Bit
1	1	1/8 Bit	5/8 Bit

Bit 2: Not used, always reads logic 1.

Bit 3: **TXD Test - PA3 Edge.** When this bit is a logic 1, PA2 (TXD) is routed to the PA3 positive edge detect (see SI3). When this bit is a logic 0, PA3 (TXCLK) is routed to the PA3 positive edge detect logic.

Bit 4: **TXD Test - Timer A Input.** When this bit is a logic 1, PA2 (TXD) input is routed to the Timer A input detect logic. When this bit is a logic 0, PA0 is routed to the Timer A input detect logic. SFR3 and SFR4, when set, can be used to easily measure the TXD start pulse width.

Bit 5: **Loopback.** When this bit is a logic 1, TXD is routed back to RXD instead of the normal serial out data. When SFR5 is a logic 0, RXD will copy the SOUT shift register when SFR6 = 0 and SOP (PA6) when SFR6 = 1.

Bit 6: **Serial Out Passthrough on PA5.** When this bit is a logic 1, the serial out input on PA5 is routed to RXD output on PA6. Note that serial out mode must be selected (SMR7 = 1) and serial loopback must not be selected (SFR5 = 0). When this bit is a logic 0, PA5 is a general purpose I/O line.

Bit 7: **Serial In Passthrough on PA1.** When this bit is a logic 1, the TXD input on PA2 is routed to the serial in output on PA1. When this bit is a logic 0, PA1 is a general purpose I/O line.

3.12.9. Serial Out (RXD) Divider Latch (SODL)

The Serial Out Divider Latch (SODL) is a CPU write-only register at $003E that controls operation of the RXD timing (Figure 3-16). The SODL must be loaded with the value corresponding to the desired data. Table 3-18 contains standard values for asynchronous and synchronous operation. Note that the SODL must be loaded with $0F for asynchronous operation whenever Short Stop Bit operation is required. Each time that the CPU writes to the SODL, the new latch value is downloaded to the counter.

3.12.10. Serial In (TXD) Divider Latch (SIDL)

The Serial In Divider Latch (SIDL) is also a CPU write-only register at $003F that controls operation of the TXD timing (Figure 3-16). Its operation is similar to that of the SODL, except that it is not restricted to a value of $0F for asynchronous operation.

3.13. DUAL PORT RAM - GP/16450 INTERFACE (C29 ONLY)

The C29 Dual Port RAM interface can be configured to operate in one of two modes:

1. General purpose 15-byte Dual Port RAM (DP RAM) with host handshake register and Host Control Register.
2. 16450 register compatible mode.

The C29 device/host interface diagram is shown in Figure 3-17. Signal equivalence between the C29 and each mode is shown in Table 3-20.

The selectable host bus interface provides an 6500 or RDP/WTP bus compatible interface between the C29 and a host microprocessor (Figure 3-17). Signal equivalence between the C29 and each mode is shown in Table 3-20. This interface allows the C29 to act like a standard peripheral device connected to the host bus under control of the host processor. Under C29 software control, this interface can be a general purpose user defined interface or a user implemented emulation of the 16450 UART interface.

Built-in hardware registers and control signals allow a 16450 UART compatible interface to be presented to the host bus. C29 application firmware functions are required to fully implement the 16450 interface functions.

3.13.1. Host Bus Interface Signals and Registers

When the host bus interface software option is selected, the following host bus signals are supported instead of the general purpose I/O lines on ports B (2 lines), C (8 lines), and D (7 lines):

8-bit bidirectional data lines (HD0-HD7)

4-bit address inputs (HA0-HA3), HA3 remains a GP I/O in the 16450 mode.

1 chip select input (HCSP)

2 bus timing inputs (HWTP and HRDP, or Hø2 and HR/WP)

1 host interrupt output (HINT)

The host bus waveforms and timing are described in Section 5.

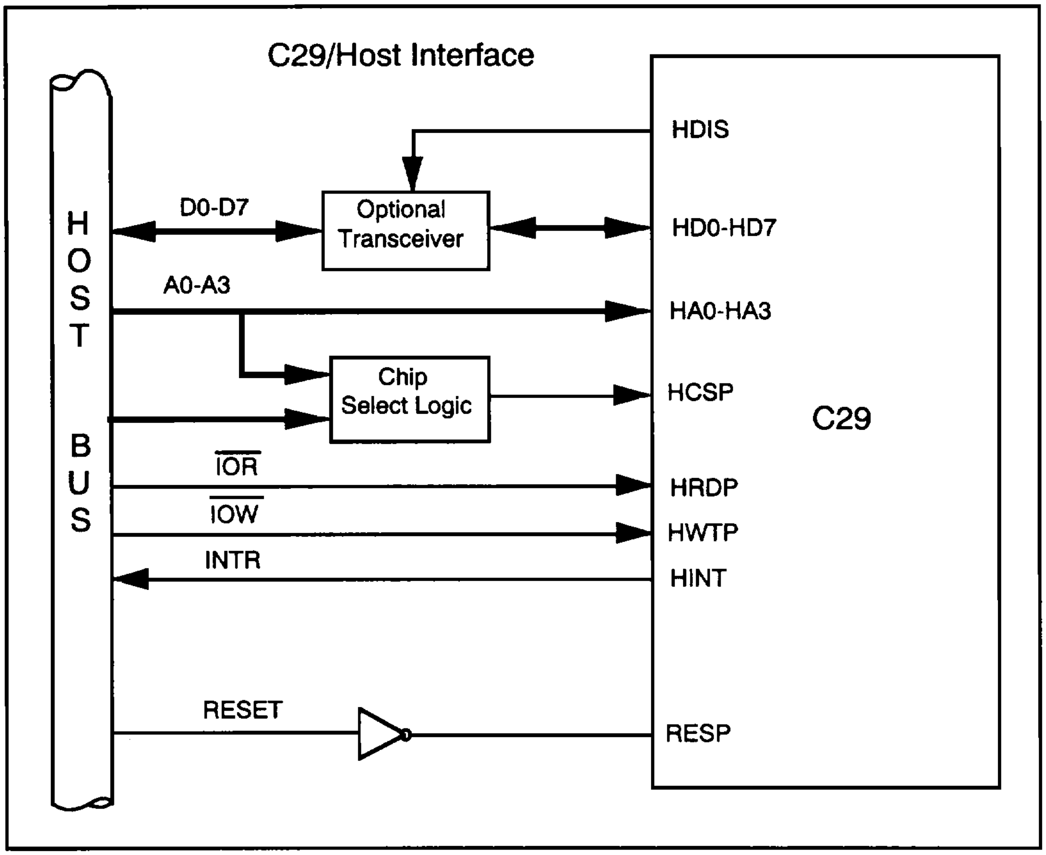


Figure 3-17. C29/Host Interface

Table 3-20 C29 Dual Port RAM Signal Equivalence

MCU Port Name	MCU Signal Name	GP RAM Mode	16450 Mode
PB6	HDIS	HDIS	DDIS
PB7	HINT	HINT	INTR
PC0-PC7	HD0-HD7	HD0-HD7	D0-D7
PD0-PD2	HA0-HA2	HA0-HA2	A0-A2
PD3	HA3	HA3	
PD4	HCSP	HCSP	CS2P
PD5	HWTP	HWTP	WTP
PD6	HRDP	HRDP	RDP
RESP	RESP	RESP	NR

3.13.2. General Purpose Interface

If the general purpose interface mode is selected (HCR1 = 0 and HCR2 = 1), 15 dual port RAM locations and the Host Handshake Register are accessible to both the C29 CPU and the external host bus. The host bus addresses are shown in Table 3-21.

Table 3-21. C29 Host Bus Interface Memory Map - GP RAM Mode

C 29 Address (Hex)	Function	Host Address (Hex)
0020	SP RAM 0	0
0021	SP RAM 1	1
0022	SP RAM 2	2
0023	SP RAM 3	3
0024	SP RAM 4	4
0025	SP RAM 5	5
0026	SP RAM 6	6
0027	SP RAM 7	7
0028	SP RAM 8	8
0029	SP RAM 9	9
002A	SP RAM A	A
002B	SP RAM B	B
002C	SP RAM C	C
002D	SP RAM D	D
002E	SP RAM E	E
002F	Host Handshake Register (HHR) [3,4]	F
0030	—	Not Accessible by Host
0031	—	Not Accessible by Host
0032	Host Control Register (HCR)	Not Accessible by Host

LEGEND: — = No assigned function.

NOTES:

1. User must prevent simultaneous C29 write/Host write to the same SP RAM location. This can be accomplished by using the Handshake register; or by dividing the SP RAM cells into two groups, one group which can only be written by the Host and the other group written only by the C29.
2. During simultaneous C29 write/Host read, or Host write/C29 read, the read operation will not interfere with write. The read operation may result in old data, new data or a combination of old and new. Reading can be resolved by using the Handshake Register or until consecutive reads are identical.
3. During read: Read until consecutive reads are identical.
4. During write: Handshake protocol required on bits 4-7 to avoid simultaneous write/write.

3.13.3. 16450 Interface

When the 16450 mode is selected (HCR1 = 1 and HCR2 = 1), the Host Bus Interface can be made to emulate the 16450 UART device. This is done through a combination of built-in hardware features and user-supplied software.

Emulation of the 16450 is equivalent when 16450 input signals CS0 and CS1 are tied high and DISTR, D0STR and ADSP are tied low (Table 3-20). All 16450 signals not included in Table 3-20 are not required for C29 16450 operation.

The C29 16450 register set and associated addresses are shown in Table 3-22. The C29 16450 register bits are identified in Table 3-23.

The Line Status Register (LSR), Modem Status Register (MSR), Interrupt Enable Register (IER) and Interrupt Identification Register (IDR) are implemented with dedicated hardware. The remaining 16450 registers are mapped directly into dual port RAM locations. Additionally, the Host Control Register provides the means to allow the C29 to control and monitor the 16450 interface.

Table 3-22 C29 Host Bus Interface Memory Map - 16450 Mode

C39 Access			Host Access			
Addr.	**Read**	**Write**	**DLAB**	**Addr.**	**Read**	**Write**
0020	Receiver Buffer	Receiver Buffer[1]	0	0	Receiver Buffer	_[4]
0021	Transmitter Buffer[2]	*	0	0	_[4]	Transmitter Buffer
—	_[4]	_[4]	0	1	Interrupt Enable Register	Interrupt Enable Register
—	_[4]	_[4]	X	2	Interrupt Identifier Register	_[4]
0022	SP RAM [2]	SP RAM [2]	—	—	_[4]	_[4]
0023	Line Control Register[2]	*	X	3	Line Control Register	Line Control Register
0024	Modem Control Register[2]	*	X	4	Modem Control Register	Modem Control Register
0025	SP RAM 5	SP RAM 5	—	—	_[4]	_[4]
0026	SP RAM 6	SP RAM 6	—	—	_[4]	_[4]
0027	SP RAM 7[2]	*	X	7	SP RAM 7	SP RAM 7
0028	Divisor LSB[2]	*	1	0	Divisor LSB	Divisor LSB
0029	Divisor MSB[2]	*	1	1	Divisor MSB	Divisor MSB
002A	SP RAM A	SP RAM A	—	—	_[4]	_[4]
002B	SP RAM B	SP RAM B	—	—	_[4]	_[4]
002C	SP RAM C	SP RAM C	—	—	_[4]	_[4]
002D	SP RAM D	SP RAM D	—	—	_[4]	_[4]
002E	SP RAM E	SP RAM E	—	—	_[4]	_[4]
002F	Host Handshake Register	Host Handshake Register	—	—	_[4]	_[4]
0030	Line Status Register	Line Status Register	X	5	Line Status Register[3]	Line Status Register[4]
0031	Modem Status Register	Modem Status Register	X	6	Modem Status Register[3]	Modem Status Register[4]
0032	Host Control Register	Host Control Register	—	—	_[4]	–

LEGEND: — = No assigned function.

* = Do not write to this location.

NOTES:

1. LSR0 = 0. Write handshake required to guarantee valid Host read data.
2. Read until data repeats.
3. During simultaneous C29 write, the host will read old value.
4. During simultaneous C29 write/Host read, or Host write/C29 read, the read operation will not interfere with write. The read operation may result in old data, new data, or a combination of old and new data. Reading can be resolved by using the Handshake Register or until consecutive reads are identical.

Table 3-23. Register Bit Assignments - 0020h - 0032h (C29 Only)

Addr.	Function	Bit 7	6	5	4	3	2	1	0
0020	Receiver Buffer	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0021	Transmitter Buffer	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
Host Read/ Write @ x1	Interrupt Enable Register (IER)	0	0	0	0	Modem Status Interrupt Enable (EDSSI)	RX Line Status Interrupt Enable (ELSI)	TX Buffer Empty Interrupt Enable (ETBEI)	RX Data Avail Interrupt Enable (ERBFI)
Host Read @ x2	Interrupt Identifier Register (IIR)	0	0	0	0	0	Int ID Bit 1	Int ID Bit 0	0 if Interrupt Pending
0023	Line Control Register (LCR)	DLAB	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop Bits	Word Length (WLS1)	Word Length (WLS0)
0024	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Read (DTR)
0028	Divisor LSB	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0029	Divisor MSB	data 15	data 14	data 13	data 12	data 11	data 10	data 9	data 8
002F	Host Handshake Register (HHR)	Controller Intrpt 1 Flag (CF1)	Controller Intrpt 2 Flag (CF2)	Host Intrpt 1 Flag (HF1)	Host Intrpt 2 Flag (HF2)	Controller Intrpt 1 Enable (CE1)	Controller Intrpt 2 Enable (CE2)	Host Intrpt 1 Enable (HE1)	Host Intrpt 2 Enable (HE2)
0030	Line Status Register (LSR)	0	Xmitter Empty (TEMT)	Xmitter Holding Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	RX Data Ready (DR)
0031	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
0032	Host Control Register (HCR)	Transmit Buffer Full Interrupt	Mode Control Write Flag	Line Control Write Flag	Divide By Write Flag	1	Host Mode Select	16450 Mode	16450 Interrupt Enable

3.13.4. Receiver and Transmitter Buffers

To the host, the Receiver Buffer Register (RBR) is a read-only register at host location 0 (with DLAB = 0), and the Transmitter Buffer Register (TBR) is a write-only register at host location 0 (with DLAB = 0). The RBR is mapped into dual port RAM at C29 address $0020, and the TBR is mapped into dual port RAM at C29 address $0021. HCR bit 7 is automatically set to logic 1 whenever the host writes to the TBR, providing a flag to the C29 that the TBR has been updated. User-provided software provides the interface between these RAM locations and the associated serial data channels.

3.13.5. Host Control Register (HCR)

The Host Control Register (HCR) controls and monitors the operation of the GP/16450 interface. This register cannot be accessed by the host. All bits can be read by the CPU. Bits 0-2 can be written to either state by the CPU. Bits 4-7 can be cleared (by the CPU by writing 0s to the corresponding bit locations) but cannot be set by the CPU. All HCR bits are cleared by device reset.

Bit 0: **16450 Interrupt Enable.** When this bit is cleared, IRQ3 will not be asserted due to any interrupt flag in HCR4 through HCR6 being set. When this bit is set and any interrupt flag in HCR4 through HCR7 is also set, IRQ3 is asserted.

Bit 1: **Host Mode Select.** When host mode is enabled (HCR2 = 1), this bit selects the type of host interface operation (0 = General Purpose DP RAM mode; 1 = 16450 DP RAM mode).

Bit 2: **Host Mode Enable.** This bit enables I/O port host mode (0 = PB6-PB7, PC0-PC7, and PD0-PD6 operate as general purpose I/O lines; 1 = PB6-PB7, PC0-PC7, and PD0-PD6 operate as dedicated host I/O pins). This bit must be set for DP RAM to operate in GP/16450 host mode.

Bit 3: **Not Used.** Will read as a 1.

Bit 4: **Divisor Latch Write Flag**. This bit is set when the host writes to either the Divisor Latch LSB or Divisor Latch MSB register. This bit is cleared by the CPU writing a 0 to this bit position; writing a 1 has no effect.

Bit 5: **Line Control Register Write Flag**. This bit is set when the host writes to the Line Control Register. This bit is cleared by the CPU writing a 0 to this bit position; writing a 1 has no effect.

Bit 6: **Mode Control Register Write Flag**. This bit is set when the host writes to the Mode Control Register. This bit is cleared by the CPU writing a 0 to this bit position; writing a 1 has no effect.

Bit 7: **Transmit Buffer Register Full.** This bit is set when the host writes to the Transmit Buffer Register (address 0 with DLAB = 0). It is cleared when the CPU writes a 0 to address $0032, bit 7.

3.13.6. Interrupt Enable Register (IER)

The host can read or write bits 0 through 3. The CPU can neither read nor write these bits. These bits are cleared by device reset.

The IER enables four types of interrupts that can separately assert the HINT output signal. A selected interrupt can be enabled by setting the corresponding enable bit to a logic 1, or disabled by setting the corresponding enable bit to a logic 0. Disabling all interrupts inhibits the Interrupt Identifier Register (IIR) and inhibits assertion of the HINT output.

The typical use of these bits in a 16450 interface application is:

Bit 0: **Enable Receiver Buffer Full Interrupt (ERBFI).** This bit, when a logic 1, enables assertion of the HINT output when the Data Ready bit (LSR0) is set to a logic 1. This bit, when a logic 0, disables assertion of HINT due to LSR0.

Bit 1: **Enable Transmitter Buffer Empty Interrupt (ETBEI).** This bit, when a logic 1, enables assertion of the HINT output when the Transmitter Empty bit in the Line Status Register (LSR5) is set to a logic 1. This bit, when a logic 0, disables assertion of HINT due to LSR5.

Bit 2: **Enable Receiver Line Status Interrupt (ELSI).** This bit, when a logic 1, enables assertion of the HINT output when bit 1, 2, 3, or 4 in the Line Status Register (LSR) is a logic 1. This bit, when a logic 0, disables assertion of HINT due to setting of any of these four LSR bits.

Bit 3: **Enable Modem Status Interrupt (EDSSI).** This bit, when a logic 1, enables assertion of the HINT output when bit 0, 1, 2, or 3 in the Modem Status Register (MSR) is a logic 1. This bit, when a logic 0, disables assertion of HINT due to setting of any of these four MSR bits.

Bits 4-7: **Not used.** Always 0.

3.13.7. Interrupt Identifier Register (IIR).

The host can read all bits but cannot write to the IIR. All bits are controlled by MCU hardware. The IIR is not accessible to the CPU.

The IIR identifies the existence and type of four prioritized pending interrupts. Four priority levels are set to assist interrupt processing in the host. When accessed, the IIR freezes the highest priority interrupt pending and acknowledges no other interrupts until the particular interrupt is serviced by the host.

Bit 0: **Interrupt Pending.** When this bit is a logic 0, an interrupt is pending. When this bit is a logic 1, no interrupt is pending. This bit can be used in a hardwired prioritized or polled environment to indicate whether an interrupt is pending. If an interrupt is pending. the IIR contents can be used as a pointer to the appropriate interrupt service routine in the host.

Bits 1-2: **Highest Priority Pending Interrupt.** These two bits identify the highest priority pending interrupt when bit 0 is a logic 0:

Bit 2	Bit 1	Priority Level	Pending Interrupt
1	1	1 (highest)	Receiver Line Status
1	0	2	Receiver Buffer Full
0	1	3	Transmitter Buffer Empty
0	0	4	Modem Status

Bits 3-7: **Not used.** Always 0.

3.13.8. Line Control Register (LCR).

All Line Control Register (LCR) bits can be read or written to either by the host or the CPU. The LCR is not initialized by device reset.

HCR bit 5 is automatically set to a logic 1 whenever the host writes to the LCR, providing a flag to the CPU that the LCR has been updated. User-provided software must read and interpret the LCR contents.

Bit 7 is duplicated as a separate hardware latch and provides the DLAB address extension bit used for register access. This bit cannot be written to by the CPU.

The typical use of these bits in a 16450 interface application are:

Bits 0-1: **Word Length Select (WLS0 and WLS1).** These two bits specify the number of bits in each transmitted or received serial character (word):

Bit 1	Bit 0	Word Length	No. of Stop Bits (LCR2 = 1)
0	0	5 Bits	1 1/2
0	1	6 Bits	2
1	0	7 Bits	2
1	1	8 Bits	2

Bit 2: **Number Stop Bits (STB).** LCR2 specifies the number of Stop bits in each transmitted and received in each serial character. If bit 2 is a 0, one Stop bit is generated. If bit 2 is a 1, the number of Stop bits generated depends on the word length (see bits 0 and 1). The receiver logic checks the first Stop bit only regardless of the number of stop bits selected.

Bit 3: **Parity Enable (PEN).** When parity is enabled (LCR3 = 1), an even or odd Parity bit is generated in the transmitted data or checked in the received data in accordance with Even Parity Select (LCR4) and Stick Parity (LCR5) bits. The parity bit is located between the last data bit and the first Stop bit.

Bit 4: **Even Parity Select (EPS).** When parity is enabled (LCR3 = 1) and stick parity is disabled (LCR5 = 0), the total number of ones in the data and parity fields is generated or checked for odd (LCR4 = 0) or even (LCR4 = 1) parity.

Bit 5: **Stick Parity.** When stick parity is enabled (LCR5 = 1) and parity is enabled (LCR3 = 1), the parity bit is generated and check in accordance with the inverted state of LCR4 (parity bit = 0 when LCR4 = 1; parity bit = 1 when LCR4 = 0).

Bit 6: **Set Break.** When Set Break is enabled (LCR6 = 1), the received data output is forced to the space (logic 0) state. The break is disabled by setting this bit to a logic 0. The Break Control bit acts only on RXD and has no effect on the transmitted data.

Bit 7: **Divisor Latch Access Bit (DLAB).** When Divisor Latch Access Bit (DLAB) is set (LCR7 = 1), access to the divisor latches of the baud generator is enabled during a read or write operation. When DLAB is reset (LCR7 = 0), access to the Receiver Buffer, Transmit Buffer, or Interrupt Enable Register is enabled.

3.13.9. Modem Control Register (MCR).

The Modem Control Register (MCR) is a read-write register. HCR bit 6 is automatically set to logic 1 whenever the host writes to the MCR, providing a flag to the C29 that the MCR has been updated. User-provided software must read and interpret the MCR contents.

The typical use of these bits in a 16450 interface application is:

Bit 0: **Data Terminal Ready (DTR).** This bit controls the Data Terminal Ready (DTR) function. When this bit is a logic 1, DTR is on. When this bit is a logic 0, DTR is off.

Bit 1: **Request to Send (RTS).** This bit controls the Request to Send (RTS) function. When this bit is a logic 1, RTS is on. When this bit is a logic 0, RTS is off.

Bit 2: **Output 1.** This bit is used in local loopback (see MCR4).

Bit 3: **Output 2.** When this bit is a logic 1, HINT is enabled. When this bit is a logic 0, HINT is in the high impedance state.

Bit 4: **Loop.** When this bit is set to a logic 1, the diagnostic mode is selected and the following occurs:

1. Data written to the Transmitter Buffer is looped back to the Receiver Buffer.
2. The contents of MCR bits 0-3 are internally connected to the four MSR bits during a host read of the MSR as follows:

Signal	MCR Bit	MSR Bit
DTR	MCR0	MSR5
RTS	MCR1	MSR4
Out1	MCR2	MSR6
Out2	MCR3	MSR7

Bit 5-7: Not Used. (Always 0).

3.13.10. Line Status Register (LSR)

With user-provided software, the LSR can emulate the functions provided by the LSR in the 16450 device. All bits are cleared to logic 0 at power-up. It is recommended that the Host not write to this register.

The typical use of these bits in a 16450 interface application is:

Bit 0: **Data Ready.** Can be set to logic 1 by the CPU. Cleared to 0 automatically when host reads the Receiver Buffer Register.

Bits 1-4: **Receive Line Status.** Four separate conditions which are ORed together. Each can be individually set to logic 1 by the CPU. Cleared to 0 automatically when the host reads the LSR.

Bit 1: **Overrun Error (OE).** See bits 1-4

Bit 2: **Parity Error (PE).** See bits 1-4.

Bit 3: **Framing Error (FE).** See bits 1-4.

Bit 4: **Break Interrupt (BI).** See bits 1-4.

Bit 5: **Transmitter Buffer Register Empty (THRE)).** Can be set to logic 1 by the CPU. Cleared to 0 automatically when the host writes to the THR. When HINT is caused by IER1 and LSR5 both being asserted, HINT will terminate when the host writes to the THR or reads the IIR.

Bit 6: **Transmitter Empty.** Can be set to logic 1 by the CPU. Cleared to zero automatically when host writes to the Transmitter Buffer.

Bit 7: **Not used.** Always 0.

Note: Bits 0-6 are set to logic 1 by the C29 by writing a 0 to the respective bit. Writing 1s has no effect.

3.13.11. Modem Status Register (MSR)

All Modem Status Register (MSR) bits can be read or written to by either the host or the CPU. With user-provided software, it can emulate the functions provided by the MSR in the 16450 device. All bits are cleared to logic 0 at power-up. It is recommended that the host not write to this register.

Bits 0-3: **Modem Status.** Each bit can be individually set to logic 1 by the CPU by writing a 0 to the bit. Writing 1s has no effect. Bits 0-3 are cleared when the host reads the MSR.

Bits 4-7: **Various Modem Status Conditions.** Can be written to either state by the CPU or the host. No automatic clear.

The typical use of these bits in a 16450 interface application is:

The Modem Status Register (MSR) reports current state and change information of the modem. Bits 4-7 supply current state and bits 0-3 supply change information. The change bits are set to a logic 1 whenever a control input from the modem changes state from the last MSR read by the host. Bits 0-3 are reset to logic 0 when the host reads the MSR or upon reset. Whenever bits 0, 1, 2, or 3 are set to a logic 1, a Modem Status Interrupt is generated.

Bit 0: **Delta Clear to Send (DCTS).** This bit is set to a logic 1 when the CTS bit has changed since the MSR was last read by the host.

Bit 1: **Delta Data Set Ready (DDSR).** This bit is set to a logic 1 when the DSR bit has changed since the MSR was last read by the host.

Bit 2: **Trailing Edge of Ring Indicator (TERI).** This bit is set to a logic 1 when the RI bit changes from a 1 to a 0 state since the MSR was last read by the host.

Bit 3: **Delta Data Carrier Detect (DDCD).** This bit is set to a logic 1 when the DCD bit changes state since the MSR was last read by the host.

Bit 4: **Clear to Send (CTS).** This bit indicates the logic state of the CTS output. If Loopback is selected (MCR4 = 1), this bit reflects the state of RTS in the MCR (MCR1).

Bit 5: **Data Set Ready (DSR).** This bit indicates the logic state of the DSR output. If Loopback is selected (MCR4 = 1), this bit reflects the state of DTR in the MCR (MCR0).

Bit 6. **Ring Indicator (RI).** This bit indicates the logic state of the RI output. If Loopback is selected (MCR4 = 1), this bit reflects the state of OUT1 in the MCR (MCR2).

Bit 7. **Data Carrier Detect (DCD).** This bit indicates the logic state of the DCD output. If Loopback is selected (MCR4 = 1), this bit reflects the state of OUT2 in the MCR (MCR3).

3.13.12. Divisor Latch Registers

The Divisor Latch LSB (least significant byte) and Divisor Latch MSB (most significant byte) are two read-write registers. HCR bit 4 is set automatically whenever the host writes to either divisor latch byte, thus providing a flag to the CPU that the Divisor Latch has been updated. User-provided software must read and interpret the Divisor Latch contents.

All bits in both registers can be read or written to by either the host or the CPU. This register is not initialized by device reset.

3.13.13. Scratch Register

All Scratch Register bits can be read or written to by either the host or the CPU (Table 3-23). There are no flag bits associated with this register. This register is not initialized by device reset.

3.13.14. Host Handshake Register (HHR)

The Host Handshake Register (HHR) supports a defined handshake protocol between the host and the CPU (Table 3-23). All bits can be read by either the host or the CPU. The host cannot access this register in 16450 mode. Bits 0-3 are interrupt enable bits and bits 4-7 are interrupt flag bits. All bits are cleared by device reset.

Bit 0: **Host Attention Flag 2 Interrupt Enable (HE2).** This bit, when set to a 1, enables HINT output to be asserted when the Host Attention Flag 2 (HHR4) is set. When this bit is reset to a 0, HINT will not be asserted based on HHR4. This bit can be written only by the host.

Bit 1: **Host Attention Flag 1 Interrupt Enable (HE1).** This bit, when set to a 1, enables HINT output to be asserted when the Host Attention Flag 1 (HHR5) is set. When this bit is reset to a 0, HINT will not be asserted based on HHR5. This bit can be written only by the host.

Bit 2: **Controller Attention Flag 2 Interrupt Enable (CE2).** This bit, when set to a 1, enables IRQ3 to be asserted when the CPU Attention Flag 2 (HHR6) is set. When this bit is reset to a 0, IRQ3 will not be asserted based on HHR6. This bit can be written only by the CPU.

Bit 3: **Controller Attention Flag 1 Interrupt Enable (CE1).** This bit, when set to a 1, enables IRQ3 to be asserted when the CPU Attention Flag 1 (HHR7) is set. When this bit is reset to a 0, IRQ3 will not be asserted based on HHR7. This bit can be written only by the CPU.

Bit 4: **Host Attention Flag 2 (HF2).** This is an attention bit from the CPU to the host. This bit can be set only by the CPU writing a 0 and can be cleared only by the host writing a 0 . HF2 is not affected by the CPU writing a 1 or the host writing a 1.

Bit 5: **Host Attention Flag 1. (HF1)** This is an attention bit from the CPU to the host. This bit can be set only by the CPU writing a 0 and can be cleared only by the host writing a 0. HF1 is not affected by the CPU writing a 1 or the host writing a 1.

Bit 6: **Controller Attention Flag 2 (CF2).** This is an attention bit from the host to the CPU. This bit can be set only by the host writing a 1 and can be cleared only by the CPU writing a 0. CF2 is not affected by the host writing a 0 or the CPU writing a 1.

Bit 7: **Controller Attention Flag 1 (CF1).** This is an attention bit from the host to the CPU. This bit can be set only by the host writing a 1 and can be cleared only by the CPU writing a 0. CF1 is not affected by the host writing a 0 or the CPU writing a 1.

3.14. DUAL PORT RAM - GP /16450/16550A INTERFACE (C39 ONLY)

The C39 Dual Port RAM interface can be configured to operate in one of three modes:

1. General purpose mode (GP mode) 13-byte Dual Port RAM (DP RAM) with host handshake register, GP FIFO status register, and transmit/receive 16-byte FIFOs.

2. 16450 register compatible mode.

3. 16550A register compatible mode with transmit/receive 16-byte FIFOs.

The C39 device/host interface diagram is shown in Figure 3-18. Signal equivalence between the C39 and each mode is shown in Table 3-24.

The selectable host bus interface provides an 6500 or RDP/WTP bus compatible interface between the C39 and a host microprocessor (Figure 3-18). This interface allows the C39 to act like a standard peripheral device connected to the host bus under control of the host processor. Under C39 software control, this interface can be a general purpose user-defined interface or an emulation of the 16450/16550A UART interface.

Built-in hardware registers and control signals allow a 16450/6550 UART compatible interface to be presented to the host bus. More supporting 16450/6550 interface functions are provided in C39 hardware than in C29 hardware in order to relieve the C39 application firmware from having to provide some time critical and overhead functions when servicing the interface. Supporting C39 application firmware functions are required to fully implement the 16450/16550A interface, however.

3.14.1. Host Bus Interface Signals and Registers

When the host bus interface is selected (HCR2 = 1), the following host bus signals are supported instead of the general purpose I/O lines on ports A (4 lines), B (2 lines), C (8 lines), and D (7 lines):

8-bit bidirectional data lines (HD0-HD7)

4-bit address inputs (HA0-HA3), HA3 remains a GP I/O in the 16450/16550A mode.

1 chip select input (HCSP)

2 bus timing inputs (HWTP and HRDP, or Hø2 and HR/WP)

1 host interrupt output (HINT)

2 data ready outputs (RXRDY and TXRDY)

2 data acknowledge inputs (RXACKP and TXACKP)

The host bus waveforms and timing are described in Section 5.

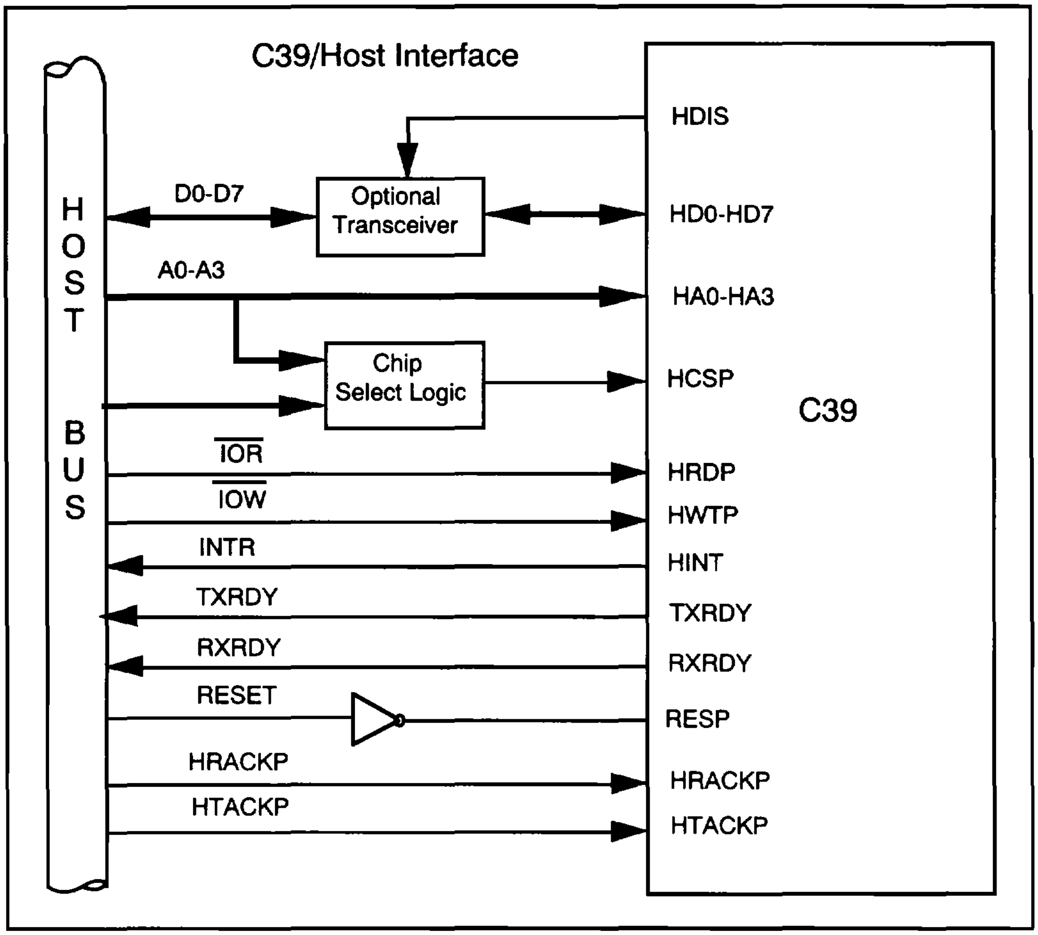


Figure 3-18. C39/Host Interface

Table 3-24. C39 Dual Port RAM Signal Equivalence

MCU Port Name	MCU Signal Name	GP RAM Mode	16450 Mode	16550A Mode
PB6	HDIS	HDIS	DDIS	DDIS
PB7	HINT	HINT	INTR	INTR
PC0-PC7	HD0-HD7	HD0-HD7	D0-D7	D0-D7
PD0-PD2	HA0-HA2	HA0-HA2	A0-A2	A0-A2
PD3	HA3	HA3	-	A3
PD4	HCSP	HCSP	CS2P	CS2P
PD5	HWTP	HWTP	WTP	WTP
PD6	HRDP	HRDP	RDP	RDP
RESP	RESP	RESP	NR	MR
PA5	TXRDY	-	TXRDY	TXRDY
PA6	RXRDY	-	RXRDY	RXRDY
PA4	HRACKP	-	HRACKP	HRACKP
PA3	HTACKP	-	HTACKP	HTACKP

3.14.2. General Purpose Interface

See Table 3-25 for a memory map of the general purpose dual port RAM. TXRDY, RXRDY, HTACKP, and HRACKP are **not** supported in the GP mode. The FIFO Status Register (FSR) and FIFO Interrupt Enable Register (FIER) have the same function as in the 16450/16550A mode. The host cannot access the FIFO Status and FIFO Interrupt Enable registers. In this mode, the Transmitter and Receiver FIFOs (TX FIFO and RX FIFO) are each 16 bytes deep and 8 bits wide. The host can only read data from the RX FIFO and can only write data to the TX FIFO. Similarly, the C39 can only write data to the RX FIFO and can only read data from the TX FIFO.

Both host and C39 can read and write to SP RAM locations $1 through $F. Simultaneously C39 write/host write to these locations are allowed but should be avoided. This can best be accomplished by using the Host Handshake Register (HHR). Tables 3-25 and Table 3-27 provide information on how the HHR can be polled or used to control both host and C39 interrupts. The GP FIFO Status Register (GPFS) provides the host with FIFO control and status information when using the TX FIFO and RX FIFO.

Table 3-25. C39 Host Bus Interface Memory Map - GP RAM Mode

C39 Address (Hex)	Function	Host Address (Hex)
0020	RX FIFO Buffer (Host Read/C39 Write)	0
0020	TX FIFO Buffer (Host Write/C39 Read)	0
0021	SP RAM 1	1
0022	SP RAM 2	2
0023	SP RAM 3	3
0024	SP RAM 4	4
0025	SP RAM 5	5
0026	SP RAM 6	6
0027	SP RAM 7	7
0028	SP RAM 8	8
0029	SP RAM 9	9
002A	SP RAM A	A
002B	SP RAM B	B
002C	SP RAM C	C
002D	SP RAM D	D
002E	GP FIFO Status (GPFS)	E
002F	Host Handshake Register (HHR)*	F
0030	FIFO Status Register (FSR)	Not Accessible by Host
0031	FIFO Interrupt Enable (FIER)	Not Accessible by Host
0032	Host Control Register (HCR)	Not Accessible by Host

* Host Handshake Register:
Host Interrupt = (HE1)(HF1) + (HE2)(HF2)
C39 Interrupt = (CE1)(CF1) + (CE2)(CF2)

3.14.3. 16550A Interface Mode and FIFOs

When the FIFO mode is selected (HCR1 = 1, HCR2 = 1, and FCR0 = 1), the C39 provides a 16550A register compatible interface mode . The 16550A interface registers are described in Tables 3-26 and 3-27. The 16550A interface uses the hardware signals shown in Figure 3-18 except the A3 signal is not used. The operation of the FIFOs is illustrated in Figures 3-19 to 3-21.

FIFO UART Timing Simulator. The FIFO UART Timing Simulator (see Figure 3-20) provides both an RUCLK and an TUCLK to simulate the 16450 UART word rate. These rates are driven by either TIMA or PTGB through divide by 16 counters. RUCLK is automatically re-synchronized to one sixteenth of the word rate by either the termination of Freeze (FSR5) or when the RX FIFO goes from empty to not empty. TUCLK will re-synchronize when the TX FIFO goes from empty to not empty.

TX FIFO. In the 16550A mode, the host can burst data into the TX FIFO Buffer until the TX FIFO is full. This can be accomplished under host control or by a supported DMA mode using TXRDY and TXACKP lines.

Both TXPTR and TUPTR advance together as the host fills the TX FIFO. The CPU unloads the TX FIFO using TXPTR. TUPTR simulates the UART by decrementing the TUCLK rate until TX FIFO is emptied. This causes THRE to be asserted which signals the host that the TX FIFO is empty. In the event the host does not write to the TX FIFO before the next TUCLK, TEMT is asserted. Two interrupt request conditions with enables are provided to the CPU: TCDA (TX FIFO data available) and TCHF (TX FIFO half full). If the TX FIFO contains between one and seven bytes of data and TCHF is enabled and neither the host or CPU have accessed the TX FIFO for three or four TUCLK intervals, a TCTO character time-out interrupt is provided to the CPU. Both TXPTR and TUPTR are reset whenever the TX FIFO bit (FCR2) is set to a 1 by the host, or whenever FIER3 is set to a 1 by the CPU. These reset controls are self clearing.

RX FIFO. In the 16550A mode, the host can burst read data from the RX FIFO Buffer until the RX FIFO is empty. This can be accomplished under host control or by a supported DMA mode using RXRDY and RXACKP lines.

The RX FIFO contains 16 eleven-bit words. Each eleven bits contain 8 bits of data and a 3-bit error field. The error field is established by the CPU loading PE, FE and BI data into the RX FIFO Status Register (FSR) bits 2 - 4. The next IWRX clock causes the error data stored in the FSR to be inserted together with CPU data into the RX FIFO. IWRX also processes or shifts older information contained in the RX FIFO. RXPTR always points to the oldest unread data and error bits contained in the RX FIFO. The RX FIFO error indication (LSR7) is asserted whenever there is an unread error in the RX FIFO error field. Both RXPTR and RUPTR are reset whenever the RX FIFO bit (FCR1) is set to a 1 by the host, or FIER2 is set to a 1 by the CPU. These reset control bits are self clearing.

RXPTR permits the C39 to burst-fill the error and data fields of the RX FIFO. The error field can be ignored by leaving BI, FE and PE in the FIFO Status Register in their zero state. Two CPU interrupt request conditions with separate enables are provided: RCEMT (RX FIFO empty) and RCHE (RX FIFO half empty) (see Figure 3-21).

The RXPTR pointer goes from empty to not empty when the CPU writes the first data into an empty RX FIFO. The RX FIFO is considered empty when both RXPTR and RUPTR are at zero. When the CPU writes to an empty RX FIFO, the RUCLK timer is resynchronized. The RUPTR transition from empty to not empty is delayed until the first RUCLK interval following the resynchronization. At this point the RUPTR pointer increments at the RUCLK rate until it reaches the value in RXPTR. If the trigger level has not been reached and RUPTR reaches the level in RXPTR, a receiver time-out event is started. Once started, if neither an IWRX or ERRX occur for three or four RUCLK intervals, an RXTO event is used to generate a host character time-out interrupt (IIR3). The host can set the RX FIFO trigger level at 1, 4, 8 or 14 using the FIFO Control Register.

3.14.4. 16450 Interface Mode and FIFOs

When the 16450 mode is selected (HCR1 = 1, HCR2 = 1, and FCR0 = 0), the C39 provides a 16450 register compatible interface mode. The 16450 interface uses the hardware signals shown in Figure 3-18 except the A3, TXRDY, RXRDY, HTACKP, or HRACKP signals are not used. The 16450 interface operation is a subset of the 16550A interface operation.

The 16450 interface registers are described in Tables 3-26 and 3-27. All registers are initialized as shown in Table 3- 28 by device reset. The CPU has access to both FIFOs while in the 16450 mode.

FIFO UART Timing Simulator. The FIFO UART Timing Simulator operates as described for the 16550A interface (see 3.14.3).

TX FIFO. In the 16450 mode, the host is limited to writing a single byte of data with each THRE interrupt. When the host writes to an empty TX FIFO Buffer, the THRE bit is cleared and after a short delay THRE is set. The host responds by sending new data to the TX FIFO Buffer which then clears THRE. TUCLK will cause THRE to be asserted one word time after the first host write to the empty TX FIFO Buffer. In the event that THRE has not been reset prior to the next TUCLK, TEMT is asserted. TUPTR simulates the responses of a 16450 UART while TXPTR provides normal TX FIFO support for the CPU The CPU must read the TX FIFO Buffer before a TX FIFO overrun can occur.

The TXRDY signal is non-operational in the 16450 mode.

RX FIFO. In the 16450 mode, the CPU has full use of the RX FIFO. The RX FIFO trigger level is set at one. Following a CPU write to an empty RX FIFO Buffer, the DR flag is not set until after an RUCLK delay. A host RX FIFO read, ERRX, decrements RUPTR and resets DR. As long as the RX FIFO contains data, the DR flag will continue to be set following the next RUCLK delay.

The RXRDY and RXTO (time-out) signals are non-operational in the 16450 mode.

Table 3-26. C39 Host Bus Interface Memory Map - 16450/16550 Mode

Internal (C39) Access				Host Access			
Addr.	**HCR1**	**Read**	**Write**	**DLAB**	**Addr.**	**Read**	**Write**
0020	X	TX FIFO Buffer	RX FIFO Buffer	0	0	RX FIFO Buffer	TX FIFO Buffer
0021	1	Line Status Register	LSR1 only	X	5	Line Status Register	Line Status Register
0022	1	Modem Status Register	Modem Status Register	X	6	Modem Status Register	Modem Status Register
0023	X	Line Control Register	Line Control Register	X	3	Line Control Register	Line Control Register
0024	1	Modem Control Register	—	X	4	Modem Control Register	Modem Control Register
—	—	—	—	0	1	Interrupt Enable Register	Interrupt Enable Register
—	—	—	—	X	2	Interrupt Identifier Register	—
0025	1	FIFO Control Register	—	X	2	—	FIFO Control Register
0026	X	SP RAM 6	SP RAM 6	—	—	—	—
0027	X	SP RAM 7	SP RAM 7	X	7	Scratch Register	Scratch Register
0028	X	Divisor Latch LSB (DLL)	Divisor Latch LSB	1	0	Divisor Latch LSB	Divisor Latch LSB
0029	X	Divisor Latch MSB (DLM)	Divisor Latch MSB	1	1	Divisor Latch MSB	Divisor Latch MSB
002A	X	SP RAM A	SP RAM A	—	—	—	—
002B	X	SP RAM B	SP RAM B	—	—	—	—
002C	X	SP RAM C	SP RAM C	—	—	—	—
002D	X	SP RAM D	SP RAM D	—	—	—	—
002E		GP FIFO Status	—	—	—	—	—
002F	X	Host Handshake Register (HHR)	Host Handshake Register	—	—	—	—
0030	X	FIFO Status Register	FIFO Status Register	—	—	—	—
0031	X	FIFO Interrupt Enable	FIFO Interrupt Enable	—	—	—	—
0032	X	Host Control Register	Host Control Register	—	—	—	—

Table 3-27. Register Bit Assignments - 0020h - 0032h (C39 Only)

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0020	RX FIFO Buffer (Host Read/C39 Write()	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0020	TX FIFO Buffer (Host Write/C39 Read)	data 7	data 6	data 5	data 4	data 3	data 2	data 1	data 0
0021	Line Status Register (LSR)	RX FIFO Error	TX Buffer Empty (TEMT)	TX Buffer Register Empty (THRE)	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrun Error (OE)	RX Data Ready (DR)
0022	Modem Status Register (MSR)	Data Carrier Detect (DCD)	Ring Indicator (RI)	Data Set Ready (DSR)	Clear to Send (CTS)	Delta Data Carrier Detect (DDCD)	Trailing Edge of Ring Indicator (TERI)	Delta Data Set Ready (DDSR)	Delta Clear to Send (DCTS)
0023	Line Control Register (LCR)	DLAB	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop Bits	Word Length (WLS1)	Word Length (WLS0)
0024	Modem Control Register (MCR)	0	0	0	Loop	Out 2	Out 1	Request to Send (RTS)	Data Terminal Ready (DTR)
0025	FIFO Control Register (FCR)	RCVR Trigger MSB	RCVR Trigger LSB	Reserved	Reserved	DMA Mode Select	TX FIFO Reset	RX FIFO Reset	FIFO Enable
Host Rd/Wt @ x1	Interrupt Enable Register (IER)	0	0	0	0	Modem Status Interrupt Enable (EDSSI)	RX Line Status Interrupt Enable (ELSI)	TX Hold Empty Interrupt Enable (ETBEI)	RX Data Avail Interrupt Enable (ERBFI)
Host Read @ x2	Interrupt Identifier Register (IIR)	FIFO Enable (FCR0)	FIFO Enable (FCR0)	0	0	Interrupt ID Bit 2	Interrupt ID Bit 1	Interrupt ID Bit 0	0 if Interrupt Pending
0027	Scratch Register (SCR)	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0028	Divisor Latch LSB	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0029	Divisor Latch MSB	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
002E	GP FIFO Status (GPFS)	Tx Empty Interrupt Enable	Tx Empty Interrupt Flag	Tx FIFO Half Empty	Rx Trig Level Sel (RTL1)	Rx Trig Level Sel (RTL0)	Rx Trig Level Int Enable	Rx Trig Level Int Flag	Rx FIFO Data Avail
002F	Host Handshake Register (HHR)	Controller Intrpt 1 Flag (CF1)	Controller Intrpt 2 Flag (CF2)	Host Intrpt 1 Flag (HF1)	Host Intrpt 2 Flag (HF2)	Controller Intrpt 1 Enable (CE1)	Controller Intrpt 2 Enable (CE2)	Host Intrpt 1 Enable (HE1)	Host Intrpt 2 Enable (HE2)
0030	FIFO Status Register (FSR)	TX Half Full Flag (TCHF)	Data Avail TCDA	RX FIFO Freeze	Receiver Break Interrupt (BI)	Receiver Framing Error (FE)	Receiver Parity Error (PE)	RX FIFO Empty Flag RCEMT	RX FIFO Half Empty Flag (RCHE)
0031	FIFO Interrupt Enable (FIER)	TX FIFO Half Full Interrupt Enable (TCHFE)	Data Avail Interrupt Enable (TCDAE)	UART Timing Select	RUCLK Off	TX FIFO Reset	RX FIFO Reset	RX FIFO Empty Interrupt Enable (RCEMT)	RX FIFO Half Empty Interrupt Enable (RCHE)
0032	Host Control Register (HCR)	TX FIFO Interrupt	Mode Control Write Flag	Line Control Write Flag	Divisor Latch Write Flag	RX FIFO Interrupt	Host Mode Select	16450/ 16550 Mode	16450/ 16550 Interrupt Enable

Table 3-28. 16550 Register Initialization

Register	Bit							
	7	6	5	4	3	2	1	0
Line Status Register (LSR)	0	1	1	0	0	0	0	0
Modem Status Register (MSR)	X	X	X	X	0	0	0	0
Line Control Register (LCR)	X	X	X	X	X	X	X	X
Modem Control Register (MCR)	0	0	0	0	0	0	0	0
Interrupt Enable Register (IER)	0	0	0	0	0	0	0	0
FIFO Control Register (FCR)	0	0	X	X	0	0	0	0
Interrupt Identifier Register (IIR)	0	0	0	0	0	0	0	1
GP FIFO Status (GPFS)	0	1	1	0	0	0	0	0
Host Handshake Register (HHR)	0	0	0	0	0	0	0	0
FIFO Status Register (FSR)	0	0	0	0	0	0	0	0
FIFO Interrupt Enable (FIER)	0	0	0	0	0	0	0	0
Host Control Register (HCR)	0	0	0	0	0	0	0	0

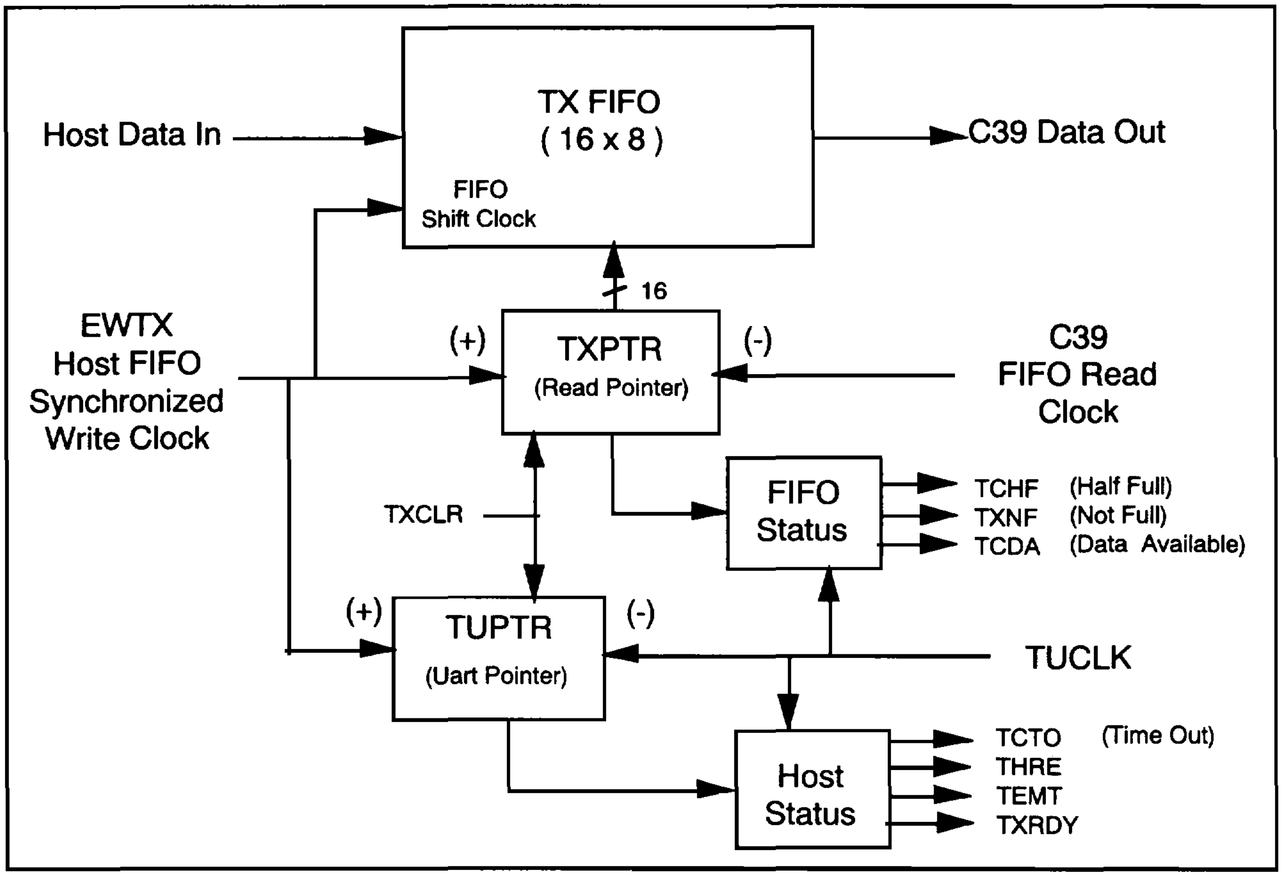


Figure 3-19. TX FIFO Block Diagram

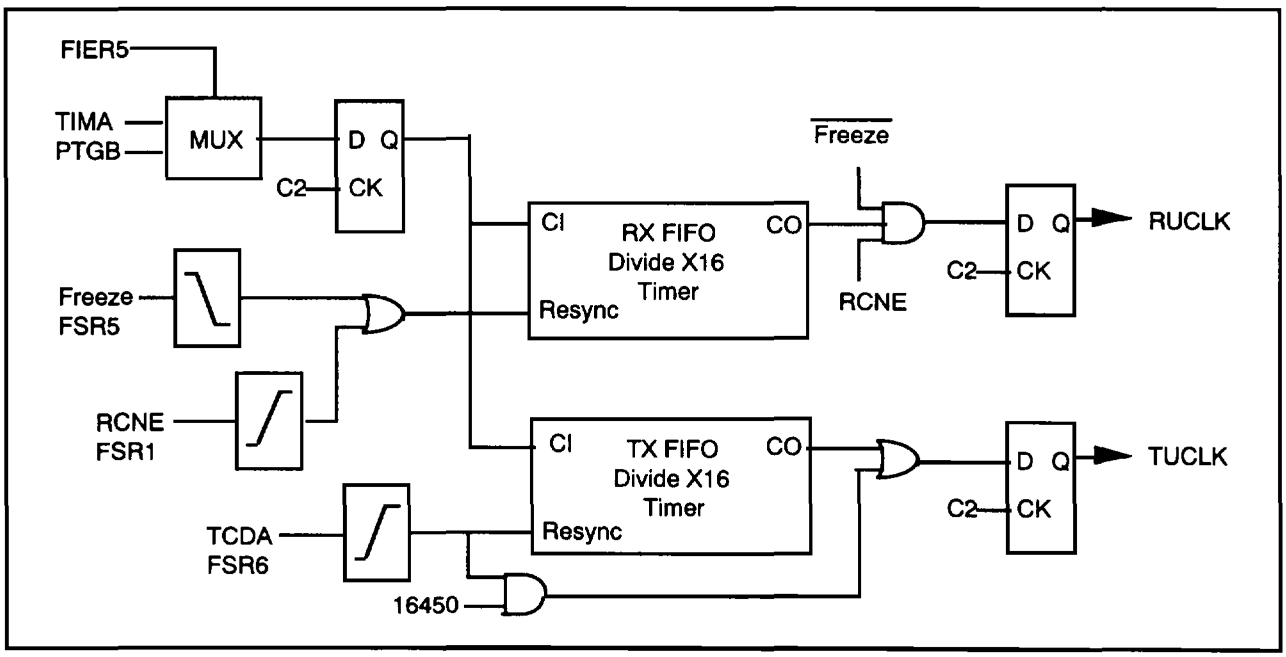


Figure 3-20. FIFO UART Timing Simulator

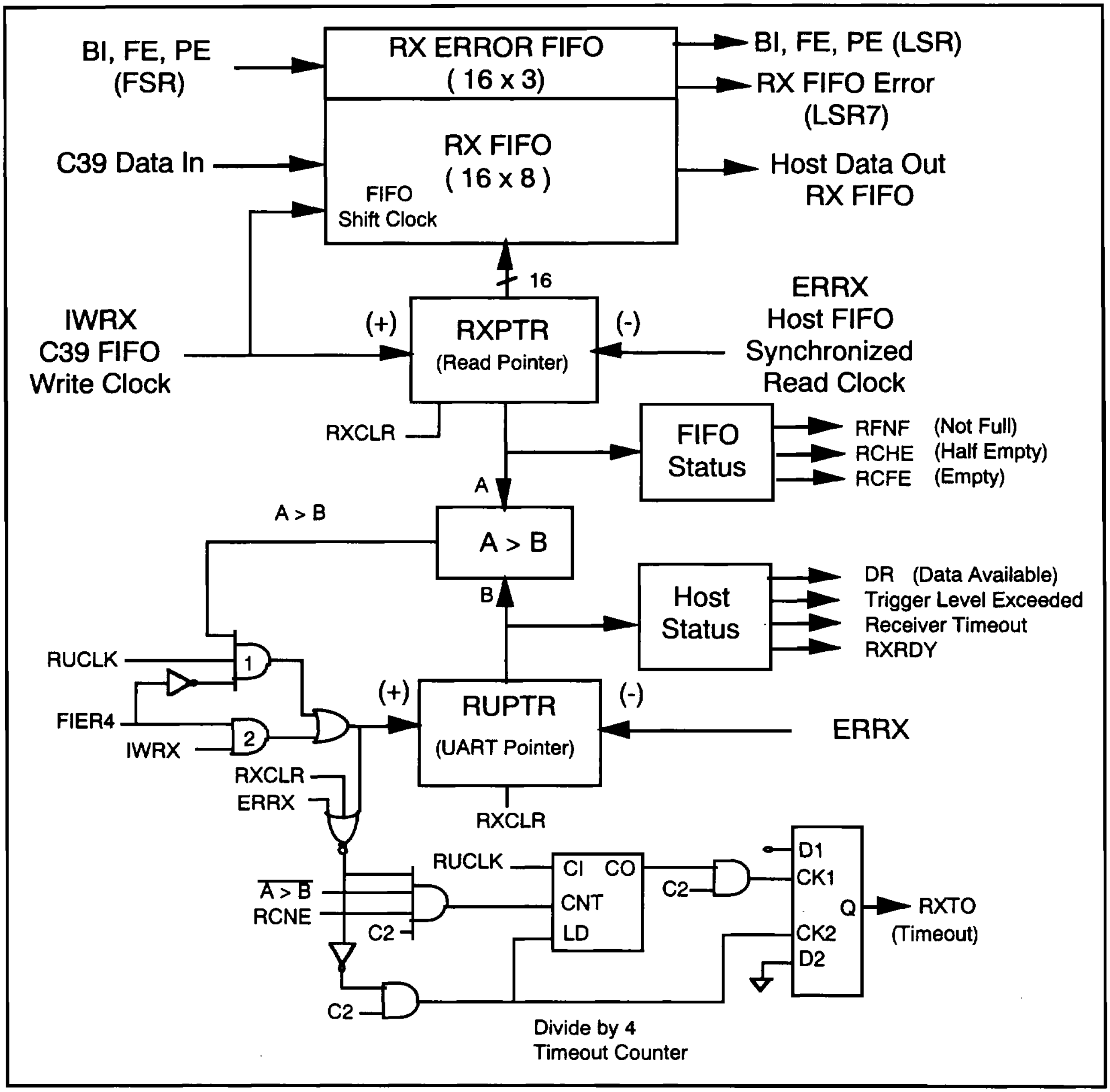


Figure 3-21. RX FIFO Block Diagram

3.14.5. Host Control Register (HCR)

The Host Control Register (HCR) controls and monitors the operation of the 16450/16550 interface. This register cannot be accessed by the host. All bits can be read by the CPU Bits 0-2 can be written to either state by the CPU. Bits 4-6 can be cleared by the CPU (by writing 0s to the corresponding bit locations) but cannot be set by the CPU. All HCR bits are cleared by device reset.

Bit 0: **16450/16550 Interrupt Enable**. When this bit is a cleared, IRQ3 will not be asserted due to any interrupt flag in HCR4 through HCR6 being set. When this bit is set, and any interrupt flag in HCR4 through HCR6 is also set, IRQ3 is asserted..

Bit 1: **16450 Mode** . When host mode is enabled (HCR2 = 1), this bit selects the type of host interface operation (0 = General Purpose DP RAM mode; 1 = 16450/16550 DP RAM mode).

Bit 2: **Host Mode Enable**. This bit enables I/O port host mode (0 = PA3-PA6, PB6-PB7, PC0-PC7, and PD0-PD6 operate as general purpose I/O lines; 1 = PA3-PA6, PB6-PB7, PC0-PC7, and PD0-PD6 operate as dedicated host I/O pins). This bit must be set for DP RAM to operate in GP/16450/16550 host mode.

Bit 3: **RX FIFO Interrupt**. This bit indicates that IRQ3 has been asserted due the RX FIFO Half Empty Flag (FSR0) being set or the RX FIFO Empty Flag (FSR1) being set. This bit is set whenever the following logic term is true:

(FSR0)(FIER0) + (FSR1P)(FIER1)

Bit 4: **Divisor Latch Write Flag**. This bit is set when the host writes to either the Divisor Latch LSB or Divisor Latch MSB register. IRQ3 is asserted if HCR0 is a 1 and this bit is a 1. This bit is cleared by the CPU writing a 0 to this bit position; writing a 1 has no effect.

Bit 5: **Line Control Register Write Flag**. This bit is set when the host writes to the Line Control Register. IRQ3 is asserted if HCR0 is a 1 and this bit is a 1. This bit is cleared by the CPU writing a 0 to this bit position; writing a 1 has no effect.

Bit 6: **Mode Control Register Write Flag**. This bit is set when the host writes to the Mode Control Register. IRQ3 is asserted if HCR0 is a 1 and this bit is a 1. This bit is cleared by the CPU writing a 0 to this bit position; writing a 1 has no effect.

Bit 7: **TX FIFO Interrupt**. This bit indicates that IRQ3 has been asserted due the TX FIFO Data Available Flag (FSR6) being set, TX FIFO Half Full Flag (FSR7) being set, or TX FIFO Time-out (FSR7)(FSR6)(TX FIFO Time-out) occurring. A TX time out occurs when neither a EWTX, IRTX or a TXCLR occur for three or four TUCLK intervals. The TX time out is cleared by EWTX, IRTX or a TXCLR. This bit is set whenever the following logic term is true:

(FSR6)(FIER6) + (FSR7)(FIER7) + (FSR7P)(FSR6)(FIER7)(TX Time out).

3.14.6. Interrupt Enable Register (IER)

The host can read or write bits 0 through 3. The CPU can neither read nor write these bits. These bits are cleared by device reset.

The IER enables five types of interrupts that can separately assert the HINT output signal. A selected interrupt can be enabled by setting the corresponding enable bit to a logic 1, or disabled by setting the corresponding enable bit to a logic 0. Disabling all interrupts inhibits the Interrupt Identifier Register (IIR) and inhibits assertion of the HINT output.

The typical use of these bits in a 16450/16550A interface application is:

Bit 0: **Enable Receiver Buffer Full Interrupt (ERBFI) and Character Time-out In FIFO Mode.** This bit, when a logic 1, enables assertion of the HINT output when the Data Ready bit (LSR0) is set to a logic 1 or character time-out occurs in FIFO mode. This bit, when a logic 0, disables assertion of HINT due to LSR0 or character time-out.

Bit 1: **Enable Transmitter Buffer Empty Interrupt (ETBEI).** This bit, when a logic 1, enables assertion of the HINT output when the Transmitter Empty bit in the Line Status Register (LSR5) is set to a logic 1. This bit, when a logic 0, disables assertion of HINT due to LSR5.

Bit 2: **Enable Receiver Line Status Interrupt (ELSI).** This bit, when a logic 1, enables assertion of the HINT output when bit 1, 2, 3, or 4 in the Line Status Register (LSR) is a logic 1. This bit, when a logic 0, disables assertion of HINT due to setting of any of these four LSR bits.

Bit 3: **Enable Modem Status Interrupt (EDSSI).** This bit, when a logic 1, enables assertion of the HINT output when bit 0, 1, 2, or 3 in the Modem Status Register (MSR) is a logic 1. This bit, when a logic 0, disables assertion of HINT due to setting of any of these four MSR bits.

Bits 4-7: **Not used.** Always 0.

3.14.7. Interrupt Identifier Register (IIR)

The host can read all bits but cannot write to the IIR. All bits are controlled by MCU hardware. The IIR is not accessible to the CPU.

The IIR identifies the existence and type of five prioritized pending interrupts. Four priority levels are set to assist interrupt processing in the host. When accessed, the IIR freezes the highest priority interrupt pending and acknowledges no other interrupts until the particular interrupt is serviced by the host.

Bits 4 and 5 are not used and always read low. Bits 6 and 7 copy the state of FCR0, the host-controlled FIFO Enable bit. The IIR is initialized to 001b by device reset.

Bit 0: **Interrupt Pending.** When this bit is a logic 0, an interrupt is pending. When this bit is a logic 1, no interrupt is pending. This bit can be used in a hardwired prioritized or polled environment to indicate whether an interrupt is pending. If an interrupt is pending. the IIR contents can be used as a pointer to the appropriate interrupt service routine in the host.

Bits 1-3: **Highest Priority Pending Interrupt.** These three bits identify the highest priority pending interrupt when bit 0 is a logic 0:

Bit 3	Bit 2	Bit 1	Priority Level	Pending Interrupt
0	1	1	1 (highest)	Receiver Line Status
0	1	0	2	Receiver Buffer Full
1	1	0	2	Character Timeout
0	0	1	3	Transmitter Buffer Empty
0	0	0	4	Modem Status

Bits 4-5: **Not used.** Always 0.

Bits 6-7: **FIFO Mode.** These two bits copy FCR0.

3.14.8. Line Control Register (LCR)

All Line Control Register (LCR) bits can be read or written to either by the host or the CPU. The LCR is not initialized by device reset.

HCR bit 5 is automatically set to a logic 1 whenever the host writes to the LCR, providing a flag to the CPU that the LCR has been updated. User-provided software must read and interpret the LCR contents.

Bit 7 is duplicated as a separate hardware latch and provides the DLAB address extension bit used for register access. This bit cannot be written to by the CPU.

The typical use of these bits in a 16450/16550 interface application is:

Bits 0-1: Word Length Select (WLS0 and WLS1). These two bits specify the number of bits in each transmitted or received serial character (word):

Bit 1	Bit 0	Word Length	No. of Stop Bits (LCR2 = 1)
0	0	5 Bits	1 1/2
0	1	6 Bits	2
1	0	7 Bits	2
1	1	8 Bits	2

Bit 2: **Number Stop Bits (STB).** LCR2 specifies the number of Stop bits in each transmitted and received in each serial character. If bit 2 is a 0, one Stop bit is generated. If bit 2 is a 1, the number of Stop bits generated depends on the word length (see bits 0 and 1). The receiver logic checks the first Stop bit only regardless of the number of stop bits selected.

Bit 3: **Parity Enable (PEN).** When parity is enabled (LCR3 = 1), an even or odd Parity bit is generated in the transmitted data or checked in the received data in accordance with Even Parity Select (LCR4) and Stick Parity (LCR5) bits. The parity bit is located between the last data bit and the first Stop bit.

Bit 4: **Even Parity Select (EPS).** When parity is enabled (LCR3 = 1) and stick parity is disabled (LCR5 = 0), the total number of ones in the data and parity fields is generated or checked for odd (LCR4 = 0) or even (LCR4 = 1) parity.

Bit 5: **Stick Parity.** When stick parity is enabled (LCR5 = 1) and parity is enabled (LCR3 = 1), the parity bit is generated and check in accordance with the inverted state of LCR4 (parity bit = 0 when LCR4 = 1; parity bit = 1 when LCR4 = 0).

Bit 6: **Set Break.** When Set Break is enabled (LCR6 = 1), the received data output is forced to the space (logic 0) state. The break is disabled by setting this bit to a logic 0. The Break Control bit acts only on RXD and has no effect on the transmitted data.

Bit 7: **Divisor Latch Access Bit (DLAB).** When Divisor Latch Access Bit (DLAB) is set (LCR7 = 1), access to the divisor latches of the baud generator is enabled during a read or write operation. When DLAB is reset (LCR7 = 0), access to the RX FIFO Buffer, TX FIFO Buffer, or Interrupt Enable Register is enabled.

3.14.9. Modem Control Register (MCR)

Bits 0-4 of the Modem Control Register (MCR) can be read or written to by the host. The CPU can only read the MCR. When the host mode is selected, the HINT output driver is placed in a three-state mode when either Out2 is false (MCR3 = 0) or Loop is selected (MCR4 = 1). In addition, when the Loop is selected, the operation of the MSR is modified as described under Modem Status Register. The MCR is cleared by device reset.

The typical use of these bits in a 16450/16550A interface application is:

Bit 0: **Data Terminal Ready (DTR).** This bit controls the Data Terminal Ready (DTR) function. When this bit is a logic 1, DTR is on. When this bit is a logic 0, DTR is off.

Bit 1: **Request to Send (RTS).** This bit controls the Request to Send (RTS) function. When this bit is a logic 1, RTS is on. When this bit is a logic 0, RTS is off.

Bit 2: **Output 1.** This bit is used in local loopback (see MCR4).

Bit 3: **Output 2.** When this bit is a logic 1, HINT is enabled. When this bit is a logic 0, HINT is in the high impedance state.

Bit 4: **Loop.** When this bit is set to a logic 1, the diagnostic mode is selected and the following occurs:

1. Data written to the TX FIFO Buffer is looped back to the RX FIFO Buffer.
2. The contents of MCR bits 0-3 are internally connected to the four MSR bits during a host read of the MSR as follows:

Signal	MCR Bit	MSR Bit
DTR	MCR0	MSR5
RTS	MCR1	MSR4
Out1	MCR2	MSR6
Out2	MCR3	MSR7

Bit 5-7: Not Used. (Always 0).

3.14.10. Line Status Register (LSR)

The host can read and write all bits in this register, however it is recommended that the host not write to the LSR register. The CPU can read all bits but can only write to LSR1 (Overrun Error).

The typical use of these bits in a 16450/16550A interface application is:

Bit 0: **Receiver Data Ready (DR).** This bit is cleared by device reset. DR is set by hardware whenever the RX UART simulator pointer, RUPTR, goes from empty to not empty. Cleared when the RUPTR pointer indicates empty. When Freeze (FSR5) is set, LSR0 is no longer controlled by the state of the RUPTR. When FSR5 = 1, the DR bit can be cleared by reading the RX FIFO Buffer.

Bit 1: **Overrun Error (OE).** This bit is set and reset by CPU write. This bit is reset when the host reads LSR. This bit is cleared by device reset.

Bit 2-4: **Receive Line Status**. They are updated automatically from the error field of RX FIFO following each CPU write or host read to the RX FIFO. LSR bits 2, 3, 4 and 7 and the RX FIFO output data latch are all updated at this time. LSR error data must be read prior to reading the RX FIFO output or the error data is lost. These bits are cleared to zero when the host reads LSR. These bits are cleared by device reset.

Bit 2: **Parity Error (PE).** See bits 2-4.

Bit 3: **Framing Error (FE).** See bits 2-4.

Bit 4: **Break Interrupt (BI)**. See bits 2-4.

Bit 5: **TX FIFO Buffer Empty (THRE)**. This bit is set by device reset. THRE is set by hardware each time the transmitter UART pointer, TUPTR, transitions from not empty to empty. It is reset by a host write to the TX FIFO. If a HINT interrupt occurs and IIR identifies THRE as the source, the interrupt is cleared while THRE remains set. Whenever the host writes to the Interrupt Enable Register enabling a THRE interrupt and THRE is set, a THRE interrupt is regenerated.

Bit 6: **Transmitter Underrun (TEMT)**. Set by device reset or by hardware when the TX FIFO has been empty for at least one TUCLK time. Reset when the host writes to an empty TX FIFO.

Bit 7: **RX FIFO Error**. Set by MCU hardware if at least one error bit is set in the unread error field of the RX FIFO. Reads zero in the 16450 mode.

3.14.11. Modem Status Register (MSR)

All Modem Status Register (MSR) bits can be read or written to by either the host or the CPU. The CPU can write all bits, however the host can only write to bits 0-3. Bits 0-3 are set to a 1 by the CPU writing a 0 to the particular bit. Bits 0-3 are unaffected when the C39 writes a 1 to a bit position. Bits 0-3 are cleared when the host reads the MSR. It is recommended that the host not write to the MSR. A host MSR read is modified when Loop is selected (MCR4 = 1). Bits 0-3 are cleared by device reset.

When Loop is not selected (MCR4 = 0), a host MSR read generates the following data:

(MSR7/MSR6/MSR5/MSR4/MSR3/MSR2/MSR1/MSR0).

When Loop is selected (MCR4 = 1), a host MSR read generates the following data:

(MCR3/MCR2/MCR0/MCR1/MSR3/MSR2/MSR1/MSR0).

The typical use of these bits in a 16450/16550A interface application is:

The Modem Status Register (MSR) reports current state and change information of the modem. Bits 4-7 supply current state and bits 0-3 supply change information. The change bits are set to a logic 1 whenever a control input from the modem changes state from the last MSR read by the host. Bits 0-3 are reset to logic 0 when the host reads the MSR or upon reset. Whenever bits 0, 1, 2, or 3 are set to a logic 1, a Modem Status Interrupt is generated.

Bit 0: **Delta Clear to Send (DCTS).** This bit is set to a logic 1 when the CTS bit has changed since the MSR was last read by the host.

Bit 1: **Delta Data Set Ready (DDSR).** This bit is set to a logic 1 when the DSR bit has changed since the MSR was last read by the host.

Bit 2: **Trailing Edge of Ring Indicator (TERI).** This bit is set to a logic 1 when the RI bit changes from a 1 to a 0 state since the MSR was last read by the host.

Bit 3: **Delta Data Carrier Detect (DDCD).** This bit is set to a logic 1 when the DCD bit changes state since the MSR was last read by the host.

Bit 4: **Clear to Send (CTS).** This bit indicates the logic state of the CTS output. If Loopback is selected (MCR4 = 1), this bit reflects the state of RTS in the MCR (MCR1).

Bit 5: **Data Set Ready (DSR).** This bit indicates the logic state of the DSR output. If Loopback is selected (MCR4 = 1), this bit reflects the state of DTR in the MCR (MCR0).

Bit 6. **Ring Indicator (RI).** This bit indicates the logic state of the RI output. If Loopback is selected (MCR4 = 1), this bit reflects the state of OUT1 in the MCR (MCR2).

Bit 7. **Data Carrier Detect (DCD).** This bit indicates the logic state of the DCD output. If Loopback is selected (MCR4 = 1), this bit reflects the state of OUT2 in the MCR (MCR3).

3.14.12. Divisor Latch Registers

The Divisor Latch LSB (least significant byte) and Divisor Latch MSB (most significant byte) are two read-write registers. HCR bit 4 is set automatically whenever the host writes to either divisor latch byte, thus providing a flag to the CPU that the Divisor Latch has been updated. User-provided software must read and interpret the Divisor Latch contents.

All bits in both registers can be read or written to by either the host or the CPU. This register is not initialized by device reset.

3.14.13. Scratch Register

All Scratch Register bits can be read or written to by either the host or the CPU. There are no flag bits associated with this register. This register is not initialized by device reset.

3.14.14. FIFO Control Register (FCR)

The host can write all bits but cannot read this register. The CPU can read all bits but cannot write to this register. Bits 1, 2, 4 and 5 read high to the CPU.

The typical use of these bits in a 16450/16550A interface application is:

Bit 0: **FIFO Enable.** 16450 mode is selected and all bits are cleared in both FIFOs when FCR0 is cleared. FIFO mode (16550A mode) is selected and both FIFOs are enabled when FCR0 is set.

Bit 1: **RX FIFO Reset.** All bytes in the RX FIFO are cleared when FCR1 is set. This bit is cleared automatically by the CPU.

Bit 2: **TX FIFO Reset.** All bytes in the TX FIFO are cleared when FCR2 is set. This bit is cleared automatically by the CPU.

Bit 3: **DMA Mode Select.** FCR3 selects the DMA operation (FCR3 = 1) or non-DMA operation (FCR3 = 0) when FIFO mode is selected (FCR0 = 1). The non-DMA mode is selected when 16450 mode is selected (FCR0 = 0).

DMA operation in FIFO mode. RXRDY will be asserted when the number of characters in the RX FIFO exceeds the value in the RX FIFO Trigger Level (FCR6-7) or the RXTO time-out has occurred. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there one or more unfilled locations in the TX FIFO. TXRDY will go inactive when the TX FIFO is completely full.

Non-DMA operation in FIFO mode. RXRDY will be asserted when there is one or more characters in the RX FIFO. RXRDY will go inactive when there are no more characters in the RX FIFO.

TXRDY will be asserted when there no characters in the TX FIFO. TXRDY will go inactive when the first character is located into the TX FIFO Buffer.

Bits 4-5: Not used.

Bits 6-7: Receiver FIFO Trigger Level. FCR7 and FCR6 set the trigger level for the RX FIFO interrupt.

FCR7	FCR6	RX FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

3.14.15. FIFO Interrupt Enable Register (FIER)

The CPU can read and write all bits. The host cannot access this register. The FIER is cleared by device reset.

Bit 0: **RCHE Interrupt Enable.** This bit is set and cleared by a CPU write to the FIER.

Bit 1: **RCEMT Interrupt Enable.** This bit is set and cleared by a CPU write to the FIER.

Bit 2: **RX FIFO Reset.** This bit is set and cleared by a CPU write to the FIER. When set, FIER2 clears the RXPTR pointer, the RUPTR pointer and the RX time-out counter. FIER2 automatically resets itself to zero.

Bit 3: **TX FIFO Reset.** This bit is set and cleared by a CPU write to the FIER. When set, FIER3 clears the TXPTR pointer, the TUPTR pointer and the TX time-out counter. FIER3 automatically resets itself to zero.

Bit 4: **RUCLK Off.** When FIER4 is set, IWRX rather than RUCLK is used to increment RUPTR (see Figure 3-21). As a result, when set, the RXPTR and RUPTR become locked together. In the GP Mode only, setting FIER4 causes both the TXPTR and TUPTR to be decremented by a CPU FIFO read. As a result, the TXPTR and TUPTR are also locked together. This bit is set and cleared by a CPU write to the FIER.

Bit 5: **UART Timing Select.** When FIER5 is set, RUCLK and TUCLK timing is derived from PTGB. When XFS5 is reset RUCLK and TUCLK timing is derived from TIMA (see Figure 3-20) This bit is set and cleared by a CPU write to the FIER.

Bit 6: **TCDA Interrupt Enable.** This bit is set and cleared by a CPU write to the FIER. When this bit is a 1 and TCDA (FSR6) is also a 1, IRQ3 is asserted.

Bit 7: **TCHF Interrupt Enable.** This bit is set and cleared by a CPU write to the FIER. When this bit is a 1 and TCHF (FSR7) is a 1, IRQ3 is asserted.

3.14.16. FIFO Status Register (FSR)

The CPU can read all bits but can only write to bits 2 through 5. The host cannot access this register. Except for bit 0 which initializes high, all bits are initialized to zero by device reset. Bits 2 - 4 are inputs to the error field of the RX FIFO.

Bit 0: **RX FIFO Half Empty Flag (RCHE)**. This bit is set and cleared by hardware. It provides RX FIFO status to the CPU. RCHE is set whenever the RX FIFO contains between 0 and 7 unread bytes of data. If FIER0 and FSR0 are both set, IRQ3 is asserted.

Bit 1: **RX FIFO Empty Flag (RCEMT)**. This bit is set and cleared by hardware. It provides RX FIFO status to the C39 CPU. RCEMT is set whenever the RX FIFO is empty. If FIER1 and FSR1 are both set, IRQ3 is asserted.

Bit 2: **Receiver Parity Error (PE)**. This bit is set and cleared by a CPU write to the FSR.

Bit 3: **Receiver Framing Error (FE).** This bit is set and cleared by a CPU write to the FSR.

Bit 4: **Receiver Break Interrupt (BI).** This bit is set and cleared by a CPU write to the FSR.

Bit 5: **DR Freeze (DRF).** Freeze halts the assertion of DR by RUPTR logic. Freeze is only used in the 16450 mode. If DR is asserted while Freeze is true, DR is cleared by a host read of the RX FIFO Buffer. This bit is set and cleared by a CPU write to the FSR.

Bit 6: **TX FIFO Data Available Flag (TCDA).** This bit is set and cleared by hardware. It provides TX FIFO status to the CPU. It is true whenever the TX FIFO contains between 1 and 16 unread bytes of data. If FIER6 and FSR6 are both set, IRQ3 is asserted.

Bit 7: **TX FIFO Half Full Flag (TCHF).** This bit is set and cleared by hardware. It provides TX FIFO status to the CPU. It is true whenever the TX FIFO contains between 8 and 16 unread bytes of data. If FIER7 and FSR7 are both set, IRQ3 is asserted.

3.14.17. GP FIFO Status Register (GPFS)

All bits can be read by either the host or the CPU (see Table 3-27). The host cannot access this register in either the 16450 or 16550A mode. The host can write to bits 2, 3, 4 and 7 only. Device reset initializes bits 0-4 and bit 7 to 0 and initializes bits 5 and 6 to 1.

Bit 0: **RX FIFO Data Available.** When operating in the GP FIFO mode, GPFS0 = 1 indicates the not empty status of RUPTR. When operating in the 16450 or 16550 mode, GPFS0 = 1 indicates that the RX FIFO is full.

Bit 1: **RX FIFO Trigger Level Flag.** GPFS1 = 1 indicates that the RUPTR has reached or exceeds the trigger level specified by RTL0 and RTL1.

Bit 2: **RX FIFO Trigger Level Interrupt Enable.** GPFS2 = 1 enables an HINT interrupt to be automatically generated whenever GPFS1 is set.

Bit 3 - 4: **RUPTR Trigger Level (RTL0 and RTL1).** GPFS3 and GPFS4 set the trigger level for the RX FIFO interrupt.

GPFS4	GPFS3	RUPTR Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 5: **Tx FIFO Half Empty.** GPFS5 is a 1 when there are 0 to 7 data bytes in the TX FIFO.

Bit 6: **Tx FIFO Empty Flag.** GPFS6 is a 1 when there are no data bytes in the TXFIFO.

Bit 7: **Tx FIFO Empty Interrupt Enable.** GPFS7 = 1 enables an HINT interrupt to be automatically generated whenever GPRS6 is a 1.

3.14.18. Host Handshake Register (HHR)

The Host Handshake Register (HHR) supports a defined handshake protocol between the host and the CPU (Table 3-27). All bits can be read by either the host or the CPU. The host cannot access this register in 16450 or 16550A mode. Bits 0-3 are interrupt enable bits and bits 4-7 are interrupt flag bits. All bits are cleared by device reset.

Bit 0: **Host Attention Flag 2 Interrupt Enable (HE2).** This bit, when set to a 1, enables HINT output to be asserted when the Host Attention Flag 2 (HHR4) is set. When this bit is reset to a 0, HINT will not be asserted based on HHR4. This bit can be written only by the host.

Bit 1: **Host Attention Flag 1 Interrupt Enable (HE1).** This bit, when set to a 1, enables HINT output to be asserted when the Host Attention Flag 1 (HHR5) is set. When this bit is reset to a 0, HINT will not be asserted based on HHR5. This bit can be written only by the host.

Bit 2: **Controller Attention Flag 2 Interrupt Enable (CE2).** This bit, when set to a 1, enables IRQ3 to be asserted when the CPU Attention Flag 2 (HHR6) is set. When this bit is reset to a 0, IRQ3 will not be asserted based on HHR6. This bit can be written only by the CPU.

Bit 3: **Controller Attention Flag 1 Interrupt Enable (CE1).** This bit, when set to a 1, enables IRQ3 to be asserted when the CPU Attention Flag 1 (HHR7) is set. When this bit is reset to a 0, IRQ3 will not be asserted based on HHR7. This bit can be written only by the CPU.

Bit 4: **Host Attention Flag 2 (HF2).** This is an attention bit from the CPU to the host. This bit can be set only by the CPU writing a 0 and can be cleared only by the host writing a 0 . HF2 is not affected by the CPU writing a 1 or the host writing a 1.

Bit 5: **Host Attention Flag 1. (HF1)** This is an attention bit from the CPU to the host. This bit can be set only by the CPU writing a 0 and can be cleared only by the host writing a 0. HF1 is not affected by the CPU writing a 1 or the host writing a 1.

Bit 6: **Controller Attention Flag 2 (CF2).** This is an attention bit from the host to the CPU. This bit can be set only by the host writing a 1 and can be cleared only by the CPU writing a 0. CF2 is not affected by the host writing a 0 or the CPU writing a 1.

Bit 7: **Controller Attention Flag 1 (CF1).** This is an attention bit from the host to the CPU. This bit can be set only by the host writing a 1 and can be cleared only by the CPU writing a 0. CF1 is not affected by the host writing a 0 or the CPU writing a 1.

3.15. EXPANSION BUS

The expansion bus extends internal address, data and control bus lines outside the MCU. This allows the MCU to operate as a microprocessor by interfacing with external memory and/or other peripheral devices. The expansion bus waveforms and timing are described in Section 5.

3.16. LOW POWER OPERATION

3.16.1. Low Power Register (LPR)

The Low Power Register (LPR), located at $0009, controls the low power mode (LPM) enable, mode selection, and wake-up condition enables (Table 3-29). All bits are cleared to logic 0 upon reset. All bits can be written and read. However, neither bit 6 nor 7 can be read in the logic 1 state since the CPU will be in the Sleep or Stop mode. Figure 3-22 illustrates the MCU low power mode logic and timing.

Table 3-29. Register Bit Assignments - Low Power Register (LPR) - 0009h

Addr.	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0009	Low Power Register (LPR)	Low Power Mode Enable	Low Power Mode Select 0 = Sleep 1 = Stop	Wake up Enable PA0 (Ring)	Wake up Enable PD4 (Wrt) PD5 (CS)	Wake up Enable PA2 (TXD)	Wake up Enable PD4 (DTR)	Wake up Enable PD5 (AL)	Not Used

Bits 0: **Not Used.**

Bits 1: **Wake-Up Enable for PD5 (AL) (C39 Only).** This bit, when set to a logic 1, enables the C39 to wake up from low power mode when a low is detected on PD5.

Bit 2: **Wake-Up Enable for PD4 (DTR) (C39 Only).** This bit, when set to a logic 1, enables the C39 to wake up from low power mode when a low is detected on PD4.

Bit 3: **Wake-Up Enable for PA2 (USART Start Bit) .** This bit, when set to a logic 1, enables the C39 to wake up from low power mode when a low is detected on PA2.

Bit 4: **Wake-Up Enable for PD4 and PD5 (Host Bus Write).** This bit, when set to a logic 1, enables the C39 to wake up from low power mode when a low is detected on both PD4 and PD5.

Bit 5: **Wake Up Enable for PA0 (Ring) .** This bit, when set to a logic 1, enables the C39 to wake up from low power mode when a low is detected on PA0.

Bit 6: **Low Power Mode Select.** This bit selects the low power mode to be entered when low power conditions exist and low power mode is enabled by LPR7 (1 = Stop; 0 = Sleep). This bit applies to C39 only; C29 allows enters sleep mode.

Bit 7: **Low Power Mode Enable.** This bit enables or disables the low power mode selected by LPR6 to be entered when low power conditions exist (1 = LPM enabled; 0 = LPM disabled).

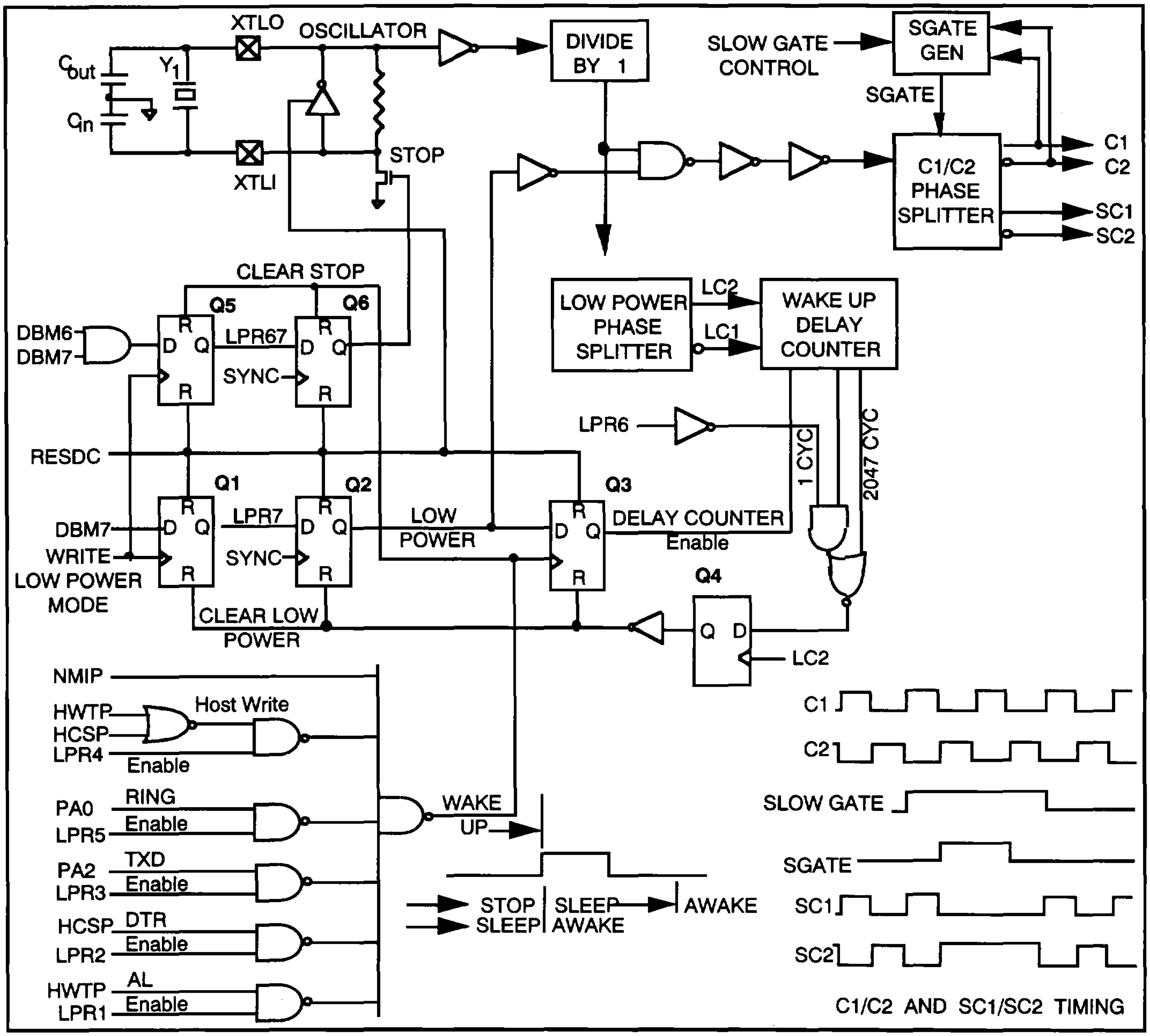


Figure 3-22. Low Power Mode Logic and Timing

3.17. TEST MODE

The Test mode is selected by applying a low voltage to the TSTP pin.

In the Test mode, the internal ROM is deactivated and the expansion bus activated when ROM addresses are selected. Reads from addresses $000C-$000F are mapped to the expansion port for growth application.

Internal reads from Page 0, 1 and 2 are mapped externally on the expansion bus whenever the TSTP pin is active. This provides for monitoring of internal read operations.

3.18. MASK OPTIONS

3.18.1. Selectable Options

The mask options are selectable upon production part order.

3.18.2. Mask Option Register (MOR)

The Mask Option Register (MOR) at location $0008 reports the selected mask options (Table 3-30).

Table 3-30. Register Bit Assignments - Mask Option Register - 0008h

Addr.	Function	Bit 7	6	5	4	3	2	1	0
0008	Mask Option Register (MSR)	Option 2	Option 1	Reserved					

Bit 0-5: **Reserved.**

Bit 6: **Bond Option 1.** Product specific.

Bit 7: **Bond Option 2.** Product specific.

4. GENERAL SPECIFICATIONS

4.1 MAXIMUM RATINGS AND HANDLING

4.1.1. Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V_{DD}	-0.5 to + 7.0	V
Input Voltage	V_{IN}	-0.5 to VDD + 0.5	V
Operating Temperature Range	T_A		
Commercial		-0 to + 70	°C
Extended		-40 to + 85	°C
Storage Temperature Range	T_S	-55 to +150	°C
Voltage Applied to Outputs in High Z State	V_{HZ}	-0.5 to VDD + 05	V
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	ESD	±2500	V
Latch-up Current (25°C)	I_{TRIG}	±200	mA

4.1.2. Handling CMOS Devices

a. The device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage.

b. An unterminated input can acquire unpredictable voltages through coupling with stray capacitances and internal crosstalk. Both power dissipation and device noise immunity degrades. Therefore, all inputs should be connected to an appropriate supply voltage.

c. Input signals should never exceed the voltage range from 0.5V or more negative than GND to 0.5V or more positive than V_{DD}. This prevents forward biasing the input protection diodes and possibly causing a latch up mode due to high current transients.

4.2 ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%, T_A = -40°C to +85°C)

Characteristics	Symbol	Min	Typ	Max	Units	Test Conditions
Input High Voltage TTL RESP, NMIP, TSTP	V_{IH}	 2.0 0.7 VDD	 -- --	 VDD + 0.3 VDD + 0.3	 V V	
Input Low Voltage TTL RESP, NMI, TSTP	V_{IL}	 -0.3 -0.3	 -- --	 0.8 0.8	 V V	
Output High Voltage	V_{OH}	2.4	--	--	V	I_{load}= -100µA
Output Low Voltage	V_{OL}	--	--	0.4	V	I_{load}= -1.6mA
3-state Output Hi-Z Current	I_{OZ}	--	--	± 10	µA	V_{in} = 0 V to V_{DD}
Input Leakage Current RESP and PD5 - PD7 only	I_I	--	--	± 2.5	µA	V_{in} = 0 V to V_{DD}
Input Leakage Current XTLI	I_I	--	--	± 10	µA	V_{in} = 0 V to V_{DD}
Input Leakage Current NMIP, TSTP, MK6 and MK7 inputs only	I_I	15	--	100	µA	V_{in} = 0 V to V_{DD}
Power Dissipation Operating Sleep Mode (C29) Sleep Mode (C39) Stop Mode (C39)	 P_D P_I P_I P_S	 -- -- -- --	 16 1.7+ 0.8 1.0+ 0.8 0.8	 20 2.5+ 1.1 1.4+ 1.1 1.1	 mW/MHz mW/MHz mW mW/MHz mW mW	

5. TIMING CHARACTERISTICS

5.1 TEST CONDITIONS

The following conditions apply for all timing descriptions:

1. T_A = -40°C to +85°C.
2. V_{DD} = 5V ± 5%.
3. Output loads = 50 pF + one TTL load.
4. Data bus, address bus, chip selects, RDP, and WTP input loads = 70 pF + one TTL load.
5. All times in nanoseconds except where noted.

5.2 OSCILLATOR TIMING

The MCU internal oscillator is designed to operate with an external crystal and external capacitors C_{out} and C_{in}. Be aware that at these frequencies component placement, lead lengths and grounding are critical and that component fine tuning may be required for each new circuit layout.

5.3 GENERAL I/O TIMING PORTS A, B, C, D

Figure 5-1 shows how port pins are read by the CPU. Table 5-1 lists the port timing. The received data is synchronized by the C2 internal clock and then held by the C1 clock. The CPU reads the sampled data that is being held by the C1 clock. Timing for pins configured in the output mode is also shown in Figure 5-1. The CPU transfers data to the port latch at C2 time. This data is transferred to the output pin by the C1 clock.

Table 5-1. Port A, B, C, D, and E Port Read/Write Timing

Parameter	Symbol	Min	Max	Units
Input Data Setup Time	tPRS	20	-	ns
Input Data Hold Time	tPRH	5	-	ns
Output Data Delay Time	tPWD	-	20	ns

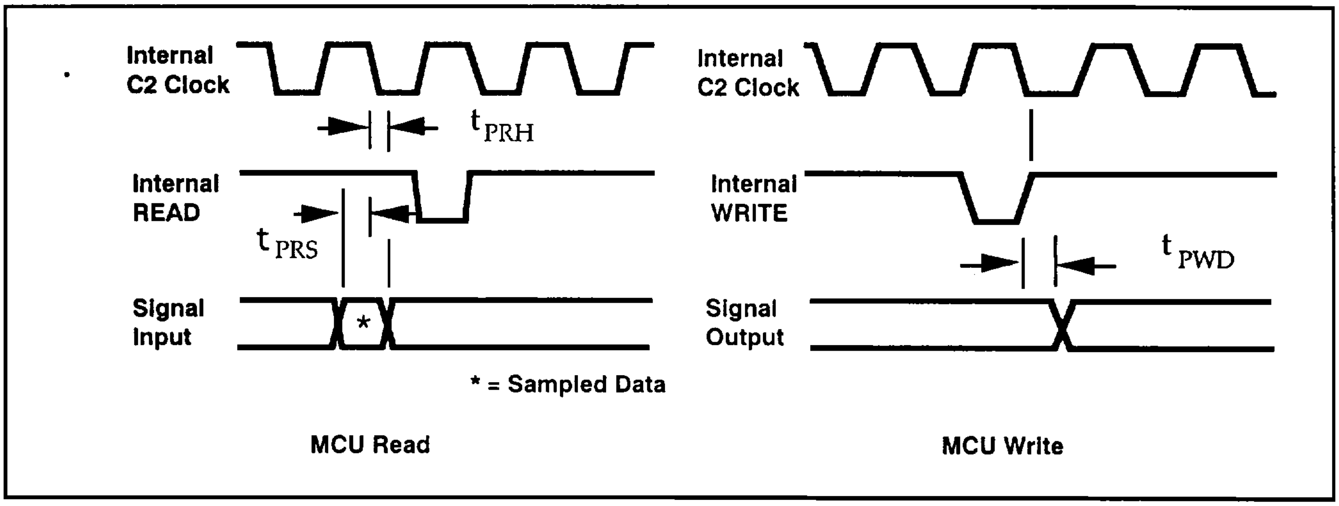


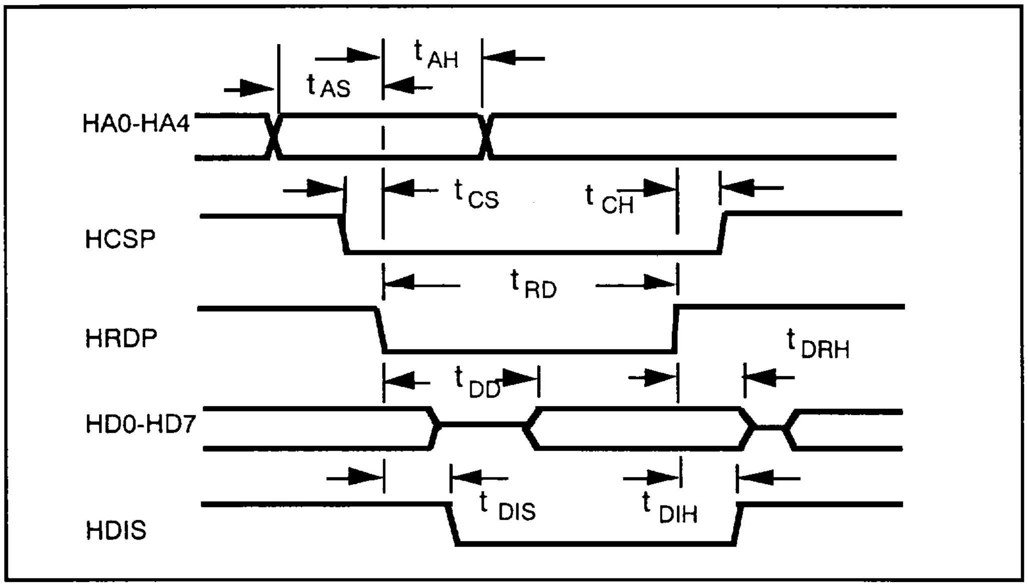
Figure 5-1. Port A, B, C, D, and E Read/Write Waveforms

5.4 HOST BUS INTERFACE

The Host Bus read timing is listed in Table 5-2 and is shown in Figure 5-2. The Host Bus write timing is listed in Table 5-3 and is shown in Figure 5-3. Host Bus interrupt timing is described in Table 5-4 and Figure 5-4.

Table 5-2. Host Bus Read Timing

Parameter	Symbol	C29		C39		Units
		Min	Max	Min	Max	
Address Setup	t_{AS}	20	-	10	-	ns
Address Hold	t_{AH}	0	-	15	-	ns
Chip Select Setup	t_{CS}	5	-	0	-	ns
Chip Select Hold	t_{CH}	0	-	10	-	ns
Read Pulse Width	t_{RD}	45	-	45	-	ns
HRDP to Data Delay	t_{DD}	-	25	-	35	ns
HRDP to Data Hold	t_{DRH}	10	-	10	-	ns
HDIS Enable	t_{DIS}	-	25	-	25	ns
HDIS Hold	t_{DIH}	10	-	0	-	ns



* When the Host executes consecutive Rx FIFO reads, a minimum delay of 3 times the internal MCU clock cycle time (300 ns at 10 MHz) is required from the rising edge of HRDP to the falling edge of the next Host Rx FIFO HRDP clock.

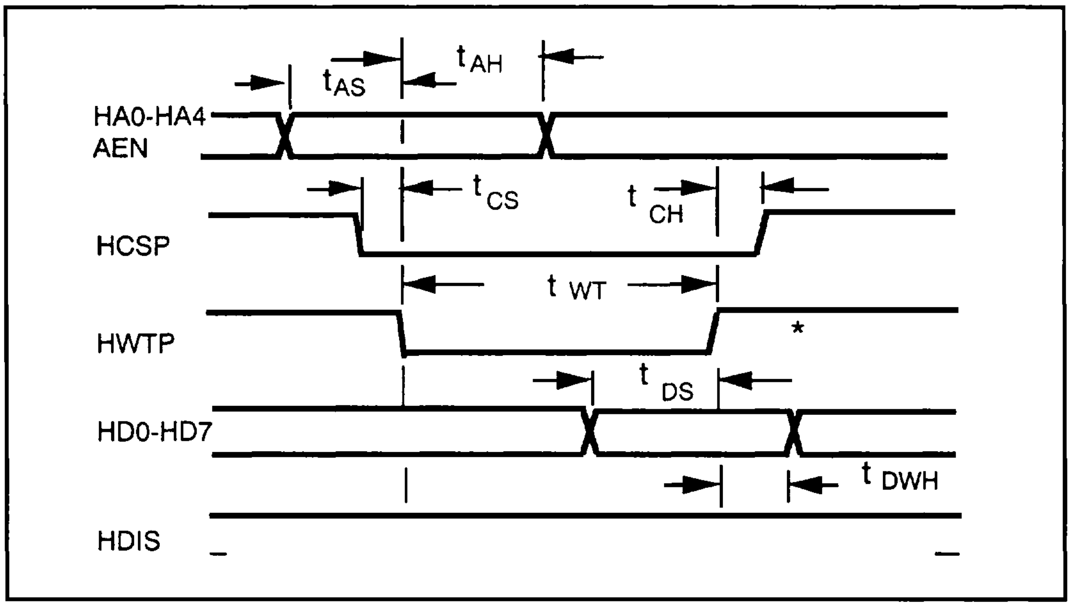
** Following a Host LSR or MSR read, a minimum delay of 2 times the internal C39 clock cycle time (200 ns at 10 MHz) is required from the rising edge of HRDP to the falling edge of the next selected Host HWTP or HRDP clock.

*** Following any other Host read, a minimum delay of 50 ns is required from the rising edge of HRDP to the falling edge of the next selected Host HWTP or HRDP clock.

Figure 5-2. Host Bus Read Waveforms

Table 5-3. Host Bus Write Timing

Parameter	Symbol	C29		C39		Units
		Min	Max	Min	Max	
Address Setup	t_{AS}	20	-	10	-	ns
Address Hold	t_{AH}	0	-	15	-	ns
Chip Select Setup	t_{CS}	5	-	0	-	ns
Chip Select Hold	t_{CH}	0	-	10	-	ns
Write Pulse Width	t_{WT}	45	-	45	-	ns
Write Data Setup	t_{DS}	10	-	10	-	ns
Write Data Hold	t_{DWH}	10	-	10	-	ns



* Following any Host write, a minimum delay of 2 times the internal MCU clock cycle time (200 ns at 10 MHz) is required from the rising edge of HWTP to the falling edge of the next selected Host HWTP or HRDP clock.

Figure 5-3. Host Bus Write Waveforms

Table 5-4. Host Bus HINT Timing

Parameter	Symbol	Typ	Units
HINT Interrupt	tINT	60	ns

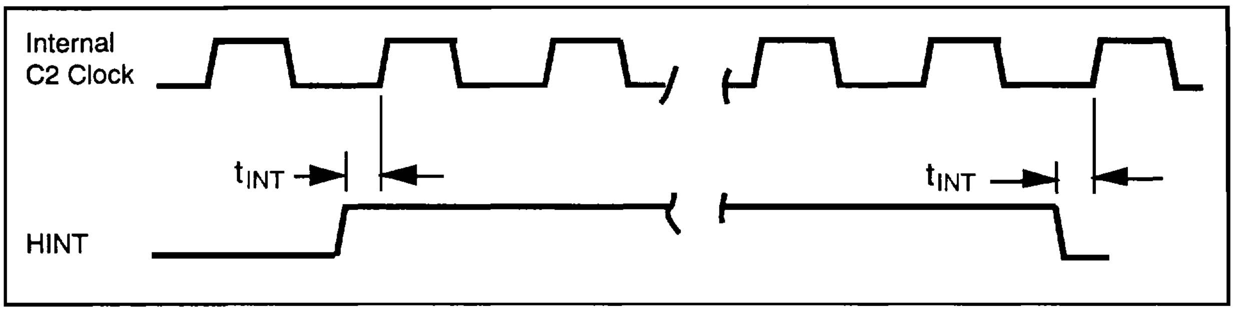


Figure 5-4. Host Bus HINT Waveforms

5.5 EXPANSION BUS TIMING

The Expansion Bus read timing is listed in Table 5-5 and is shown in Figure 5-5. The Expansion Bus write timing is listed in Table 5-6 and is shown in Figure 5-6.

Table 5-5. Expansion Bus Read Timing

Parameter	Symbol	Min	Max	Units
Internal Clock Operating Cycle	t_{CYC}	100	10^4	ns
RDP ↑ to Address Valid	t_{AS}	-	15	ns
RDP ↑ to ES Valid	t_{ES}	-	15	ns
↓ RDP to RDP ↑ Pulse Width	t_{RW}	50	-	ns
↓ RDP to Read Data Valid	t_{RDS}	15	-	ns
RDP ↑ to Read Data Hold	t_{RDH}	10	-	ns

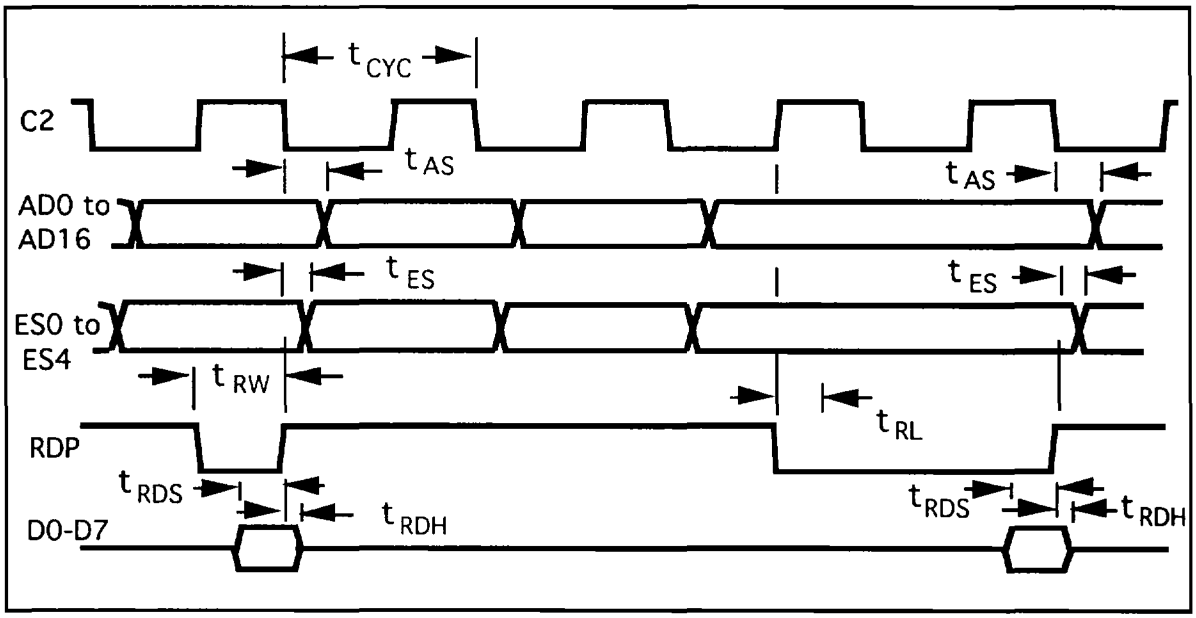


Figure 5-5. Expansion Bus Read Waveforms

Table 5-6. Expansion Bus Write Timing

Parameter	Symbol	Min	Max	Units
Internal Clock Operating Cycle	t_{CYC}	100	10^4	ns
WTP ↑ to Address Valid	t_{AS}	-	15	ns
WTP ↑ to ES Valid	t_{ES}	-	15	ns
↓ WTP to WTP ↑ Pulse Width	t_{WW}	50	-	ns
↓ WTP to Write Data Valid	t_{WTD}	-	25	ns
WTP ↑ to Write Data Hold	t_{WTH}	10	-	ns

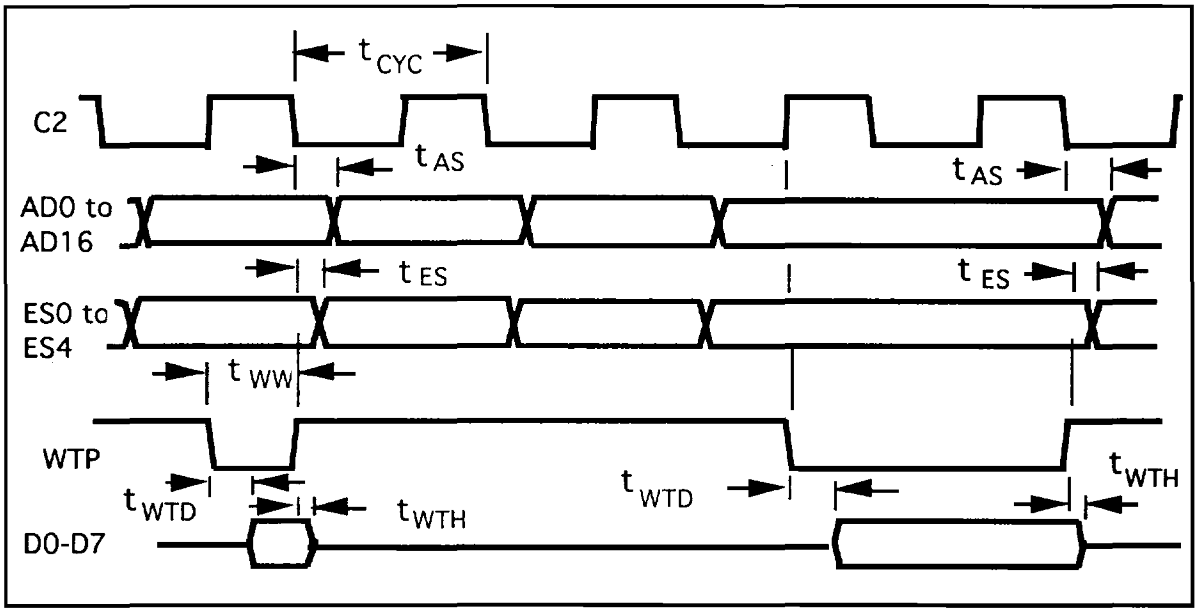


Figure 5-6. Expansion Bus Write Waveforms

5.6 RESP, NMIP, and TSTP ASYNCHRONOUS INPUTS

The timing for the RESP, NMIP, and TSTP asynchronous inputs is shown in Figure 5-7 and is listed in Table 5-7. These inputs can have only one transition during each C2 period. The XTLI and RESP timing during MCU power turn-on is shown in Figure 5-8.

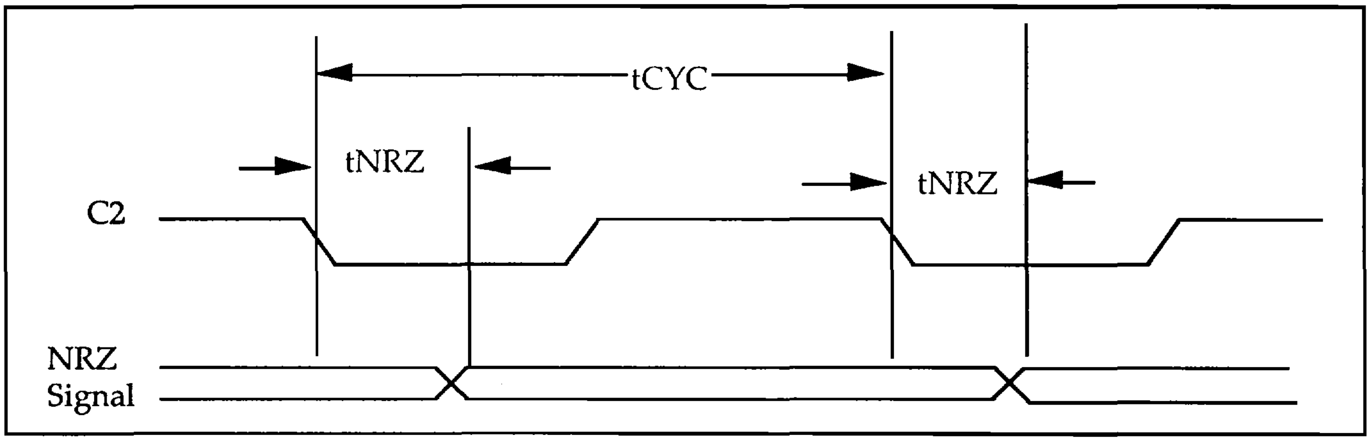


Figure 5-7. RESP, NMIP, and TSTP Input Waveforms

Table 5-7. Power On RESP, NMIP, and TSTP Timing

Term Name	t_{NRZ}	Signal Active State	Signal Active State	Remarks
RESP	40 ns	low	*2 tcyc	MCU reset
NMIP	40 ns	low	tcyc	Non-Maskable Interrupt
TSTP	40 ns	low	tcyc	Emulate mode

*During power up, a minimum of 10 t_{cyc} must occur after the crystal oscillator has stabilized.

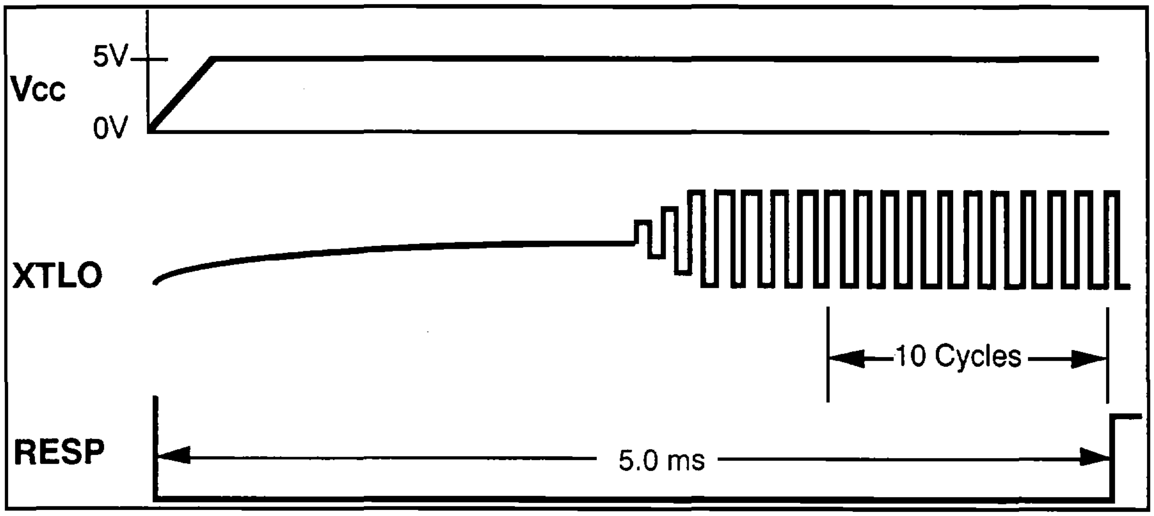


Figure 5-8. Power On RESP Timing