SPARCplug: Best of Both Worlds

About SPARCplug™

Taking advantage of our expertise in system design and miniaturization, ROSS engineers have created a high-end SPARC™ workstation that fits in the full-height drive bay of a PC, running both systems off a single power supply. Inside SPARCplug, you will find a single or dual hyperSPARC™ processor module, room for up to 256 MB of RAM, Ethernet and SCSI connectors, and an SBus slot, providing the options of ISDN, High-Speed Ethernet or High-Speed Serial Interface (T-1 or T-3) connections. SPARCplug makes use of a new 66 MHz MBus developed by ROSS; competing full-size systems currently run at 50 MHz. To complete the package, ROSS has designed SPARCplug to deliver high-end workstation performance at an entry-level price.

Utilizing the strongest contenders for cross-platform software utility and functionality, we have developed a number of market-defined product offerings around SPARCplug technology. By loading today's best software and offering our product through authorized Resellers and OEMs (needed to analyze the user requirements and if necessary, to upgrade the power supply in the PC), we can deliver turnkey customer solutions with the stability and robustness of the Solaris® operating system, while minimizing the tasks of administration. Our current product lineup includes machines configured as a Java™ Development Station, an Intranet Server, an Internet Firewall/Server, a 3-D Multiprocessing RenderStation™, and an Engineering Workstation. All are designed to coexist with your Windows™-based PC, providing new horizons for network stability, business communications (whether departmental, enterprise-wide or worldwide), and personal productivity.

SPARCplug Compatibility

SPARCplug products utilize hyperSPARC microprocessors which, like all ROSS products, maintain absolute compliance with SPARC standards, including SPARC SCD, SPARC Version 8 Architecture, and Level 2 (multiprocessing) MBus. In addition, the Solaris® 1.1 (SunOS® 4.1.3 or 4.1.4), 1.1.1B, 2.3, 2.4 and the new Solaris 2.5 operating systems are all fully qualified on hyperSPARC and supported by SunSoft™. hyperSPARC offers full compatibility and the highest performance on all 10,000+ existing applications for SPARC, which is the platform of choice for over half of all workstation users in the world today.

hyperSPARC Processors and the Competition

Unlike the simple "measurement by megahertz" (MHz) so typical in comparison of the processors that are utilized by PCs, RISC processors have wide differences in performance due to architectural or design differences between them (e.g., SPARC, MIPS, Alpha, PowerPC, PA, etc.). Of course, there are differences arising from the clock speed, which is the "MHz" measurement, but chip architecture can be more important. For example, the 125 MHz hyperSPARC processor delivers integer performance of 133 (SPEC_int92) and floating point performance of 154 (SPEC_fp92); by comparison, the 175 MHz MIPS chip provides 130 and 100, and the 166 MHz Alpha offers 108 and 135, respectively. Typically, RISC microprocessors offer greatly increased floating-point performance over x86-based processors (such as Pentium™), which is important in applications like 3-D rendering, graphics, and scientific modeling. Other factors, such as amount, speed and proximity of second-level cache memory, the latency to access main memory, and the speed and width of the data bus affect system performance as well, so system performance on an array of computing tests is necessary to fairly evaluate any competing systems.

hyperSPARC is designed as a tightly coupled chip set and implemented as a SPARC MBus module using Multi-Die Packaging (MDP). Each hyperSPARC CPU supports either 256, 512, or 1024 Kbytes of second-level cache, and each module contains one or two CPUs. The chip set is comprised of the RT620 Central Processing Unit (CPU), the RT625 or RT626 Cache Controller, Memory Management, and Tag Unit (CMTU), and four RT627 Cache Data Units (CDUs) for 256 Kbytes of second-level cache, four RT628 CDUs for 512 Kbytes of second-level cache, or eight RT628 CDUs for 1 Mbyte second-level cache. The chip set can be configured for uniprocessing (Level 1 MBus) or multiprocessing (Level 2 MBus).

Using MDP technology, hyperSPARC integrates these multiple bare die into a single IC package. Instead of driving high-frequency signals from chip to chip across a PCB, these signals travel millimeters through a silicon substrate with only a fraction of the capacitive and inductive loads. This not only results in higher attainable clock speeds, but also a considerable reduction in power consumption. hyperSPARC's high performance is also attributed to its parallel program execution, which is based on the idea that software tasks can be dissected into pieces at several levels, and can run concurrently. Hardware can be designed to take advantage of the parallelism offered by software. hyperSPARC was designed with this in mind.

At the top level of hyperSPARC's parallel processing model is the industry's most efficient use of shared-memory multiprocessing support. This VLSI hardware support for connecting multiple CPUs provides a cost-effective solution for creating a tightly coupled multiprocessing system. Combining this configuration with a symmetric, multithreading operating system provides users with a powerful computing node that has many times the performance of a single-CPU system.

In addition to multiprocessing capability, hyperSPARC modules offer easy upgradeability. As faster hyperSPARC CPUs become available, users can simply replace the older modules with newer ones. Utilizing the MBus standard allows for CPU modules to be quickly

removed and replaced, providing a wide range of processor options to suit growing performance needs.

Since the SPARCplug is installed in a PC, you can have the processor you want on the PC side, and the stability, performance and huge application library of hyperSPARC on the server or workstation side.

SPARCplug: An OEM Solution

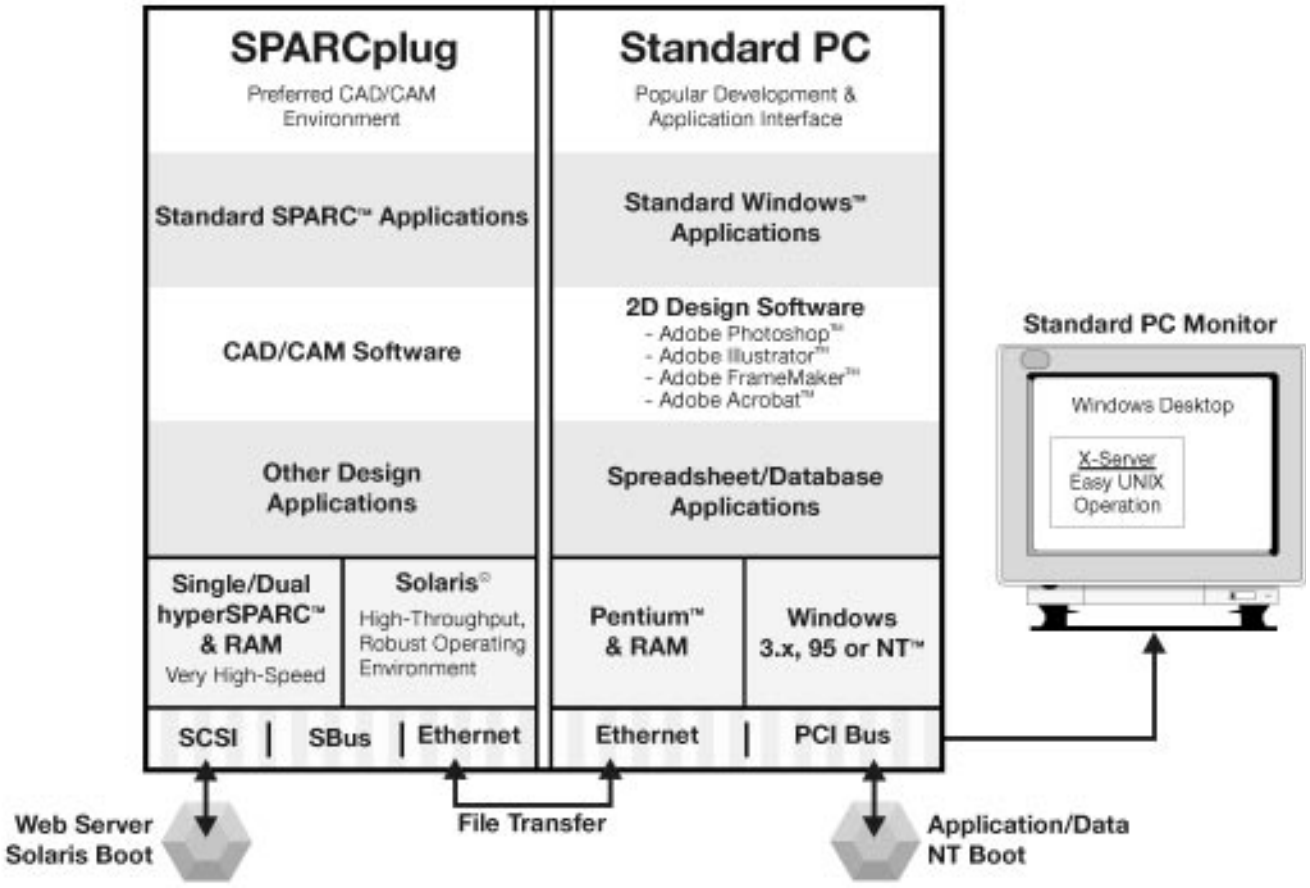
When ROSS designers develop a product, they don't stop thinking. We have solved some interesting problems for our OEM customers, and we believe the SPARCplug development effort can now benefit forward-thinking OEMs—companies that recognize ROSS Technology as the SPARC Solutions Company. Our system solutions, including CPUs, motherboards, and ASICs, outperform any competitive products in their class, and run not only the latest software such as Solaris 2.5, but also your customers' legacy software such as SunOS 4.1.x and Solaris 1.x. Ask the competitors if their latest systems support these legacy software OS's, which constitute the vast majority of the SPARC installed base.

ROSS' motherboard solutions are fully multiprocessing capable and offer absolute SPARC compatibility. Our motherboards are available in two form-factors: the classic SPARCstation™ form-factor, and now a compact footprint that enables a high performance workstation to fit in a PC tower ("SPARCplug").

The uniquely compact size of SPARCplug makes it ideal for other applications such as clustering to create enterprise servers, telecommunications, notebook computers, embedded control, and other markets that only you can imagine.

The following pages describe different SPARCplug software and hardware configurations to address a handful of interesting vertical markets: Engineering Workstation, 3-D Design/ Rendering Station, Internet Firewall/Server, Intranet Server and Java Development Station.

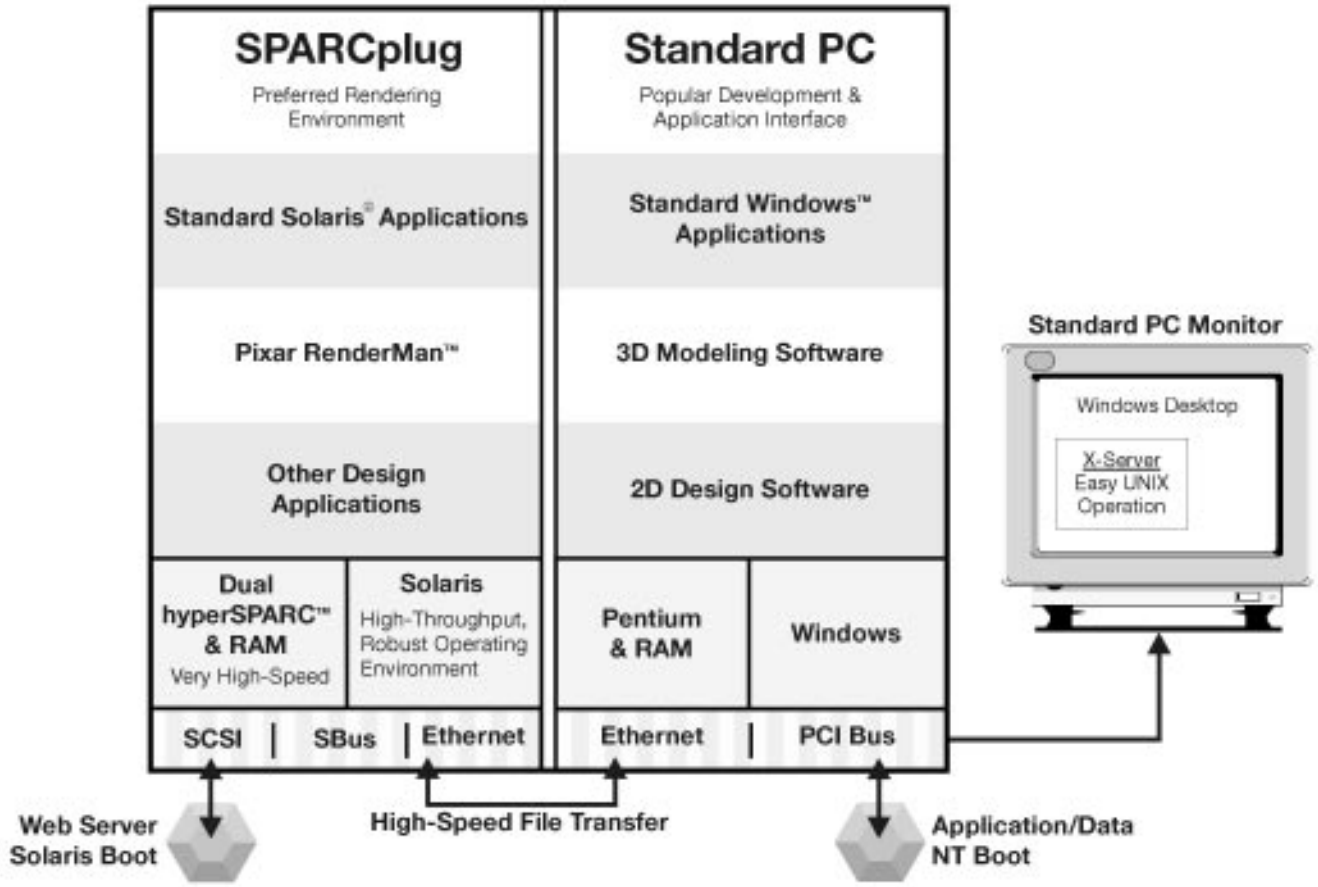
SPARCplug™ Engineering Workstation



SPARCplug delivers better-than-SPARCstation™ 20 performance on SPARC™ applications, and offers complete PC productivity just a mouse click away. Available with cross-platform authoring software such as Adobe's Photoshop™, Illustrator™, Acrobat™, FrameMaker™ and Hummingbird's Exceed™ 5 24-bit windowing environment.

The software shown represents a technology demonstration only. SPARCplug is designed to be a total solution, configured with any of the 10,000+ SPARC applications. © 1996, ROSS Technology, Inc.

SPARCplug™ 3-D Design/Rendering Station



Real multitasking at last—run multithreaded rendering applications like Pixar's RenderMan™ on a multiprocessing system! Develop under the friendly PC environment, off-load the heavy rendering jobs to the dual-processor SPARCplug, and then go right back to work on your PC. Pixar used 294 of the same ROSS hyperSPARC™ processors for Toy Story!

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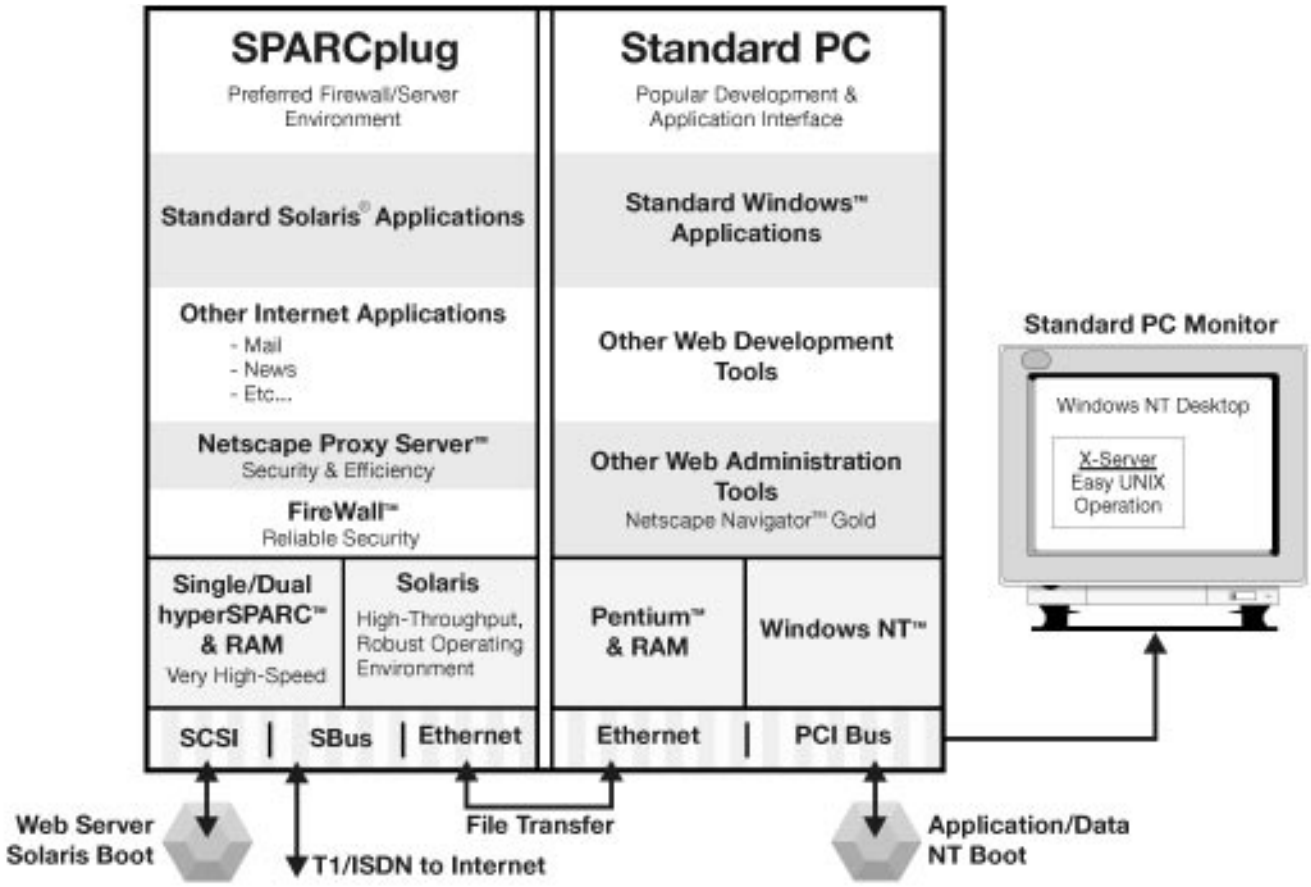
SPARCplug™ Internet Firewall/Server



Get on the Net quickly and safely with FireWall™ 2.1 from SunSoft™, simply by installing SPARCplug in a PC. FireWall is easy to use, is very secure and highly scalable. Netscape's Proxy Server™ adds security and caches Web pages for optimum throughput. Navigator™ Gold gives you the rest of the author's toolset; from the PC side, drop directly into your existing network, whether Microsoft, Novell or Apple, on LAN or WAN. Over 50% of Internet hosts are Sun systems, making SPARCplug the optimum choice as your server.

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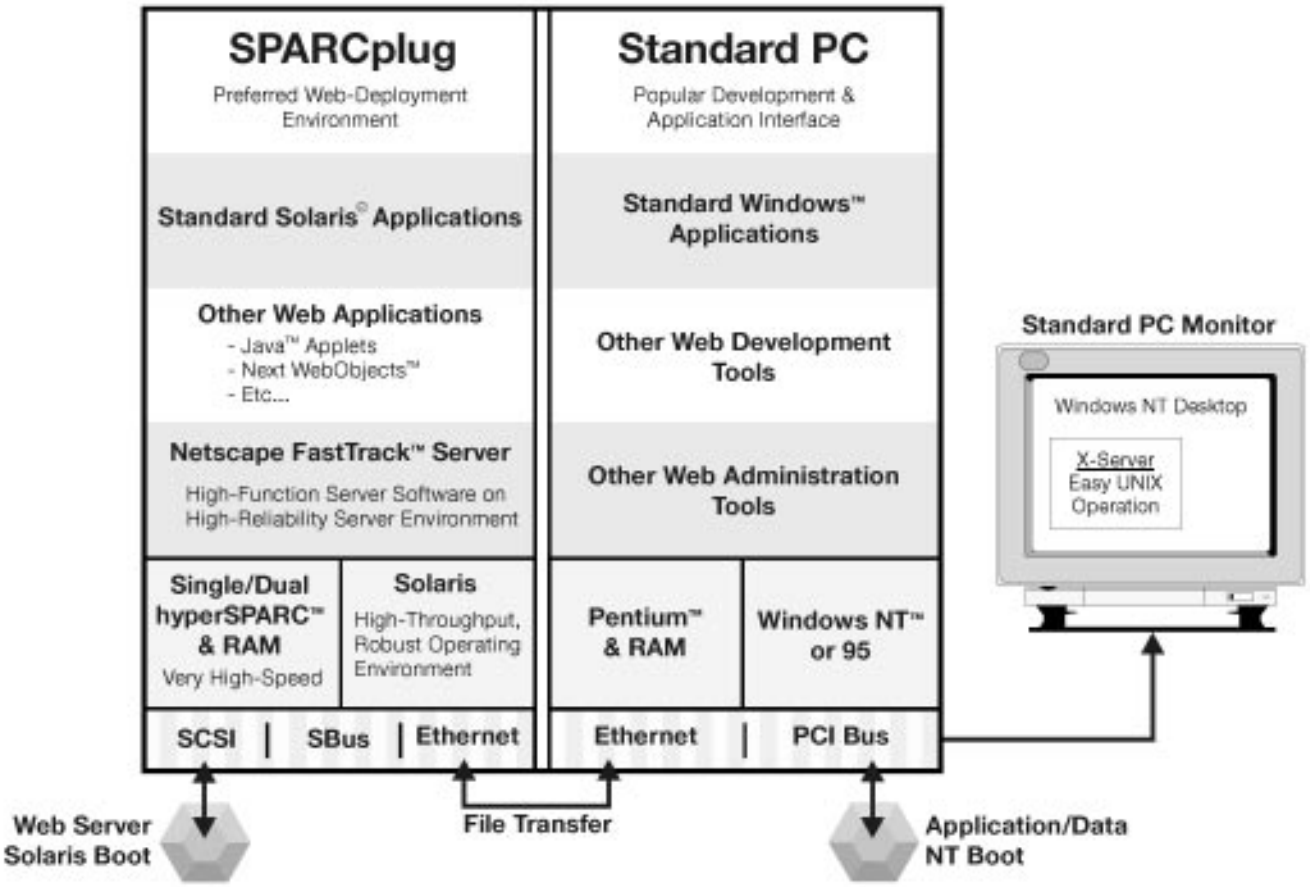
SPARCplug™ Intranet Server



SPARCplug can transform a PC into a departmental Web server and deliver a stable and robust Solaris Web platform, with the convenience of PC WYSIWYG page editing from any client. Netscape's FastTrack™ and Navigator™ Gold provide smooth and easy setup—in minutes—of a Web site; your Intranet is 70X faster than 28.8 modem access to the Internet.

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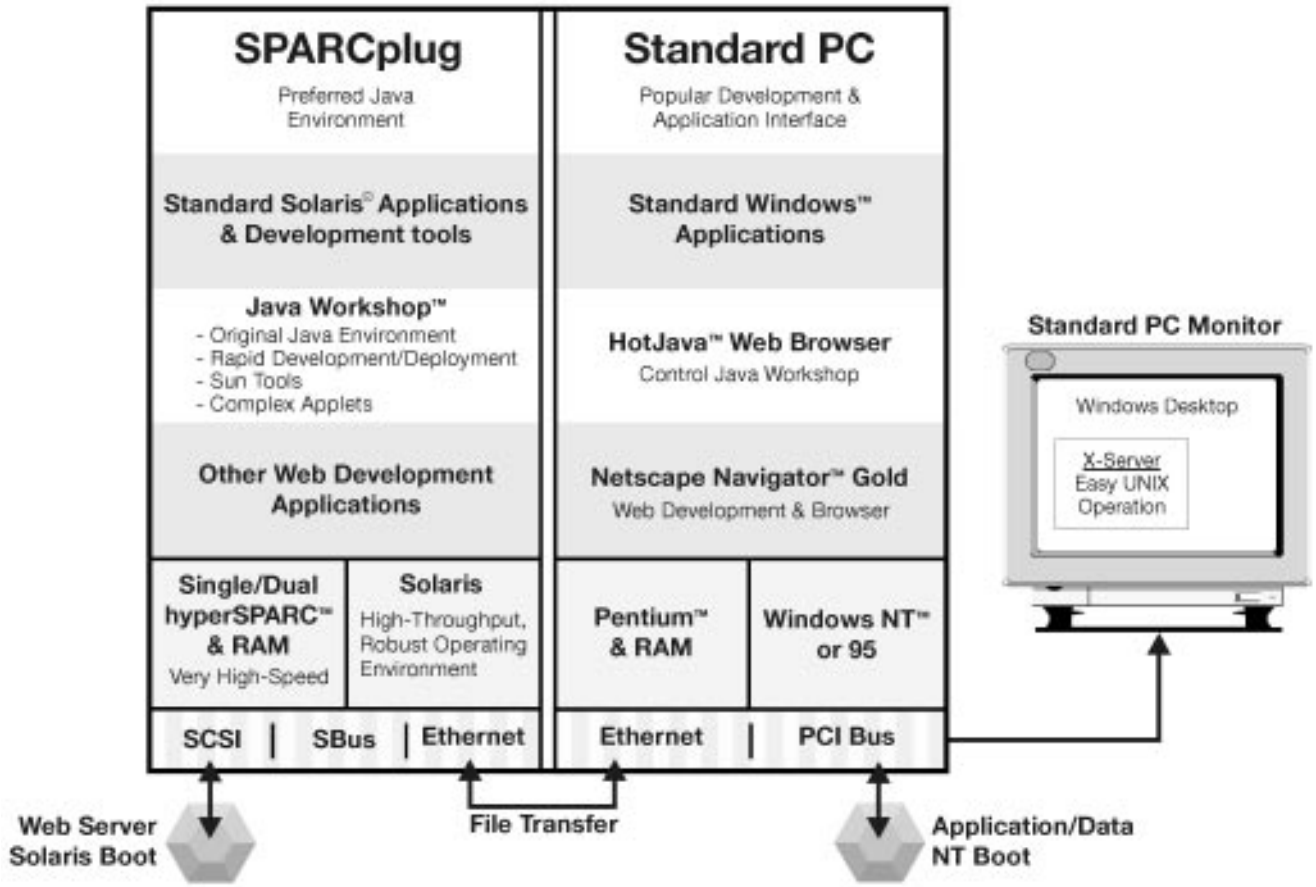
SPARCplug Java Development Station



Developers can now fast-track their new Java™ applets, using Sun's Java Workshop™ on SPARCplug. Using Netscape Navigator™ Gold and HotJava™ browsers on the PC side, the SPARCplug Java Station provides the best of both worlds. Web page designers can immediately test the applets, all with one box. SPARCplug can also be used as a Solaris-based server.

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Technical Specifications

The SPARCplug motherboard supports one standard MBus connector (up to 2 CPUs) and one SBus slot. It can also hold up to four 144 bit-wide SIMMs, supporting up to 256 MBytes of memory. It includes on-board devices for Ethernet, Fast SCSI-2, 8-bit audio, keyboard, mouse, floppy disk control and two serial ports.

The chipset used is ROSS Technology's 66 MHz MBus chipset, which makes SPARCplug compatible with SPARCstation 20 machines. Thus, it is bootable from a standard SunOS® or Solaris® CD.

MBus and Memory Support

MBus 66 MHz, 64-Bit wide MBus with one MBus connector to support single or dual CPUs.

Memory 128-bit wide MBus Error Correcting Memory Controller with 4 SIMM slots supporting 16 and 64-MByte, 60 ns, 200 pin SIMM modules. Maximum capacity is 256 MBytes.

Embedded I/O Support

SCSI Bus 1 x SCSI-2 Fast/Narrow bus using NCR 89C100 MACIO which incorporates a fully compatible NCR53C90A SCSI and LSI DMA-2 compatible interface.

Network 1 x IEEE 802.3/Ethernet AUI Port using NCR 89C100 MACIO which incorporates a fully compatible AM7990 ethernet controller. Maximum packet rate is 10 MBits/s.

Serial 2 x RS-232 or RS-423 Ports Sync/Async using 85C30 SCC. Async transfer to 38.4 KBits/s, Sync to 64 KBits/s.

Audio 1 x 8-bit Analog I/O port using AMD 79C30

Floppy 1 x floppy interface using Intel i82077AA

SBus 1 x 25 MHz, 32-Bit SBus slot

User Interface Options

Keyboard Sun Type-4 or Type-5, sealed or open

System Software

Operating System	Solaris 1.x (SunOS), Solaris 2.x
Language Support	C/C++, FORTRAN 77/90
Networking	ONC, NFS, TCP/IP

Chassis Support

SPARCplug is available in a PC-tower standard 5.25" full height slot package

Maximum power consumption 100 W at +5 V (without CPUs)

Functional Overview

SPARCplug utilizes the following ASICs: the MBus-SBus Interface (MSI), the Error Correcting Memory Controller (EMC), the Master Controller for I/O (MACIO) and the SBus to EBus Controller (SETC).

The CPU(s) on the system access data through the SPARC-standard MBus. SPARCplug supports up to two CPUs, and arbitration between CPUs for access to the MBus is performed by circuitry in the MSI. When a CPU is given access to the MBus, it generates an MBus cycle.

The EMC converts MBus cycles addressed to memory into memory cycles using RAS, CAS and data transfer cycles. The memory is 128 bits wide, and the EMC generates/checks and additional 16 bits of data, allowing it to correct single bit errors and detect multiple bit errors. The EMC also generates DRAM refresh cycles. The timing of DRAM access cycles is programmable by registers in the EMC, as is the DRAM refresh rate.

MBus cycles addressed to SBus space are converted into SBus cycles by the MSI. The SBus is primarily used for I/O. As the SBus may have multiple masters, all SBus arbitration is handled by the MSI. The MSI can also act as an MBus master, allowing SBus master devices to access memory through the MSI, thus allowing I/O DMA transactions. The MSI also contains a small I/O cache as well as lookup tables for virtual to physical address mapping of I/O devices, allowing SBus devices to access virtual memory space.

Two SBus slots are used by on-board devices. Slot F is taken by the MACIO, which has SBus master capabilities. It incorporates a fast SCSI-2 controller, an ethernet controller, an 8-bit bi-directional parallel port and the DMA control circuitry to allow all three devices to use DMA transfers. The SCSI bus connects externally to storage devices such as disks, CD-ROMs and tape drives. The ethernet controller allows connection to thin wire or twisted pair ethernet transceivers for networking. The parallel port is used to drive an LCD status panel and is thus not accessible to users.

The SETC chip converts special SBus cycles addressed to any of the 8-bit on-board devices into EBus cycles. The special SBus protocol used between the MSI and SEC is a private protocol that uses the physical SBus signals. The EBus is an 8-bit bus that allows the 8-bit devices (i.e., EPROM, NVRAM, audio, serial ports, keyboard/mouse and floppy disk controller) to be accessed. Each device on the EBus has its own set of read and write enable signals, the timing of which are programmable through a register in the SETC. This allows devices with different access times to be connected to the EBus. The SETC also handles all interrupt mapping, converting interrupts from each device on board into CPU interrupt levels and routing them to the appropriate processor. Interrupts can be mapped to particular CPUs by programmable registers in the SETC chip. The SETC also contains a number of counters/timers for systems timing. These are fully programmable, and can be used to generate interrupts.

ROSS Overview

ROSS Technology was incorporated in 1988 and is a majority owned subsidiary of Fujitsu Limited. A minority position in ROSS is held by Sun Microsystems, Inc. The Company's objective is to drive SPARC, the industry's highest-volume reduced instruction set computing architecture, to increased performance leadership and market share in the 1990s. ROSS Technology is one of the industry's most prominent suppliers of SPARC microprocessors and microprocessor related products to both the OEM and end user markets, having completed our first year as a public company with revenues of over $100 million. ROSS stock is traded on the NASDAQ exchange under the symbol RTEC.