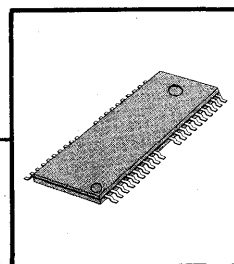


SAMSUNG

1110-4091

MOS Memory

1995



• DRAM



PRINTED IN KOREA

Circuit diagrams utilizing SAMSUNG products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of SAMSUNG or others. SAMSUNG reserves the right to change device specifications.

Certified ISO 9001



Certificate No. FM 24651

TABLE OF CONTENTS

I. FUNCTION GUIDE

1. Introduction	11
2. Product Guide	38
3. Cross Reference Guide	54
4. Ordering Information	61

II. 1M DRAM Data Sheet

1. KM41C1000C/CL/CSL	73
2. KM44C256C/CL/CSL	90

III. 4M DRAM Data Sheet

3. KM41C4000C/CL/CSL	109
4. KM41C4002C	127
5. KM44C1000C/CL/CSL	146
6. KM44C1010C	165
7. KM44C1002C	184
8. KM44C1003C/CL/CSL	204
9. KM44C1004C/CL/CSL	226
10. KM41V4000C/CL/CLL	248
11. KM44V1000C/CL/CLL	267
12. KM44V1004C/CL/CLL	286

IV. 4M B/W DRAM Data Sheet

13. KM48C512B/BL/BLL	309
14. KM48C514B/BL/BLL	323
15. KM49C512B/BL/BLL	338
16. KM416C256B/BL/BLL	351
17. KM416C254B/BL/BLL	373
18. KM416C156B/BL/BLL	409
19. KM416C157B/BL/BLL	430
20. KM418C256B/BL/BLL	451
21. KM48V512B/BL/BLL	472
22. KM48V514B/BL/BLL	485
23. KM416V256B/BL/BLL	500
24. KM416V254B/BL/BLL	521

V. 16M DRAM Data Sheet

25. KM41C16000A/AL/ALL/ASL	559
26. KM41C16002A/AL/ALL/ASL	575
27. KM44C4000A/AL/ALL/ASL	591
28. KM44C4100A/AL/ALL/ASL	608
29. KM44C4010A/AL/ALL/ASL	625

TABLE OF CONTENTS (Continued)

30. KM44C4110A/AL/ALL/ASL	642
31. KM44C4002A/AL/ALL/ASL	659
32. KM44C4102A/AL/ALL/ASL	677
33. KM44C4003A/AL/ALL/ASL	695
34. KM44C4103A/AL/ALL/ASL	714
35. KM44C4004A/AL/ALL/ASL	733
36. KM44C4104A/AL/ALL/ASL	751
37. KM41V16000A/AL/ALL/ASL	769
38. KM44V4000A/AL/ALL/ASL	784
39. KM44V4100A/AL/ALL/ASL	801
40. KM44V4004A/AL/ALL/ASL	818
41. KM44V4104A/AL/ALL/ASL	836

VI. 16M B/W DRAM Data Sheet

42. KM48C2000A/AL/ALL/ASL	857
43. KM48C2100A/AL/ALL/ASL	871
44. KM48C2004A/AL/ALL/ASL	885
45. KM48C2104A/AL/ALL/ASL	906
46. KM48V2000A/AL/ALL/ASL	927
47. KM48V2100A/AL/ALL/ASL	941
48. KM48V2004A/AL/ALL/ASL	955
49. KM48V2104A/AL/ALL/ASL	976
50. KM416C1000A/A-L/A-F	997
51. KM416C1200A/A-L/A-F	1019
52. KM416C1004A/A-L/A-F	1041
53. KM416C1204A/A-L/A-F	1076
54. KM416V1000A/A-L/A-F	1111
55. KM416V1200A/A-L/A-F	1133
56. KM416V1004A/A-L/A-F	1155
57. KM416V1204A/A-L/A-F	1190

VII. 64M DRAM Data Sheet

58. KM48V8000	1227
59. KM48V8004	1228
60. KM48V8100	1229
61. KM48V8104	1230

IX. SALES OFFICES and MANUFACTURER'S REPRESENTATIVES

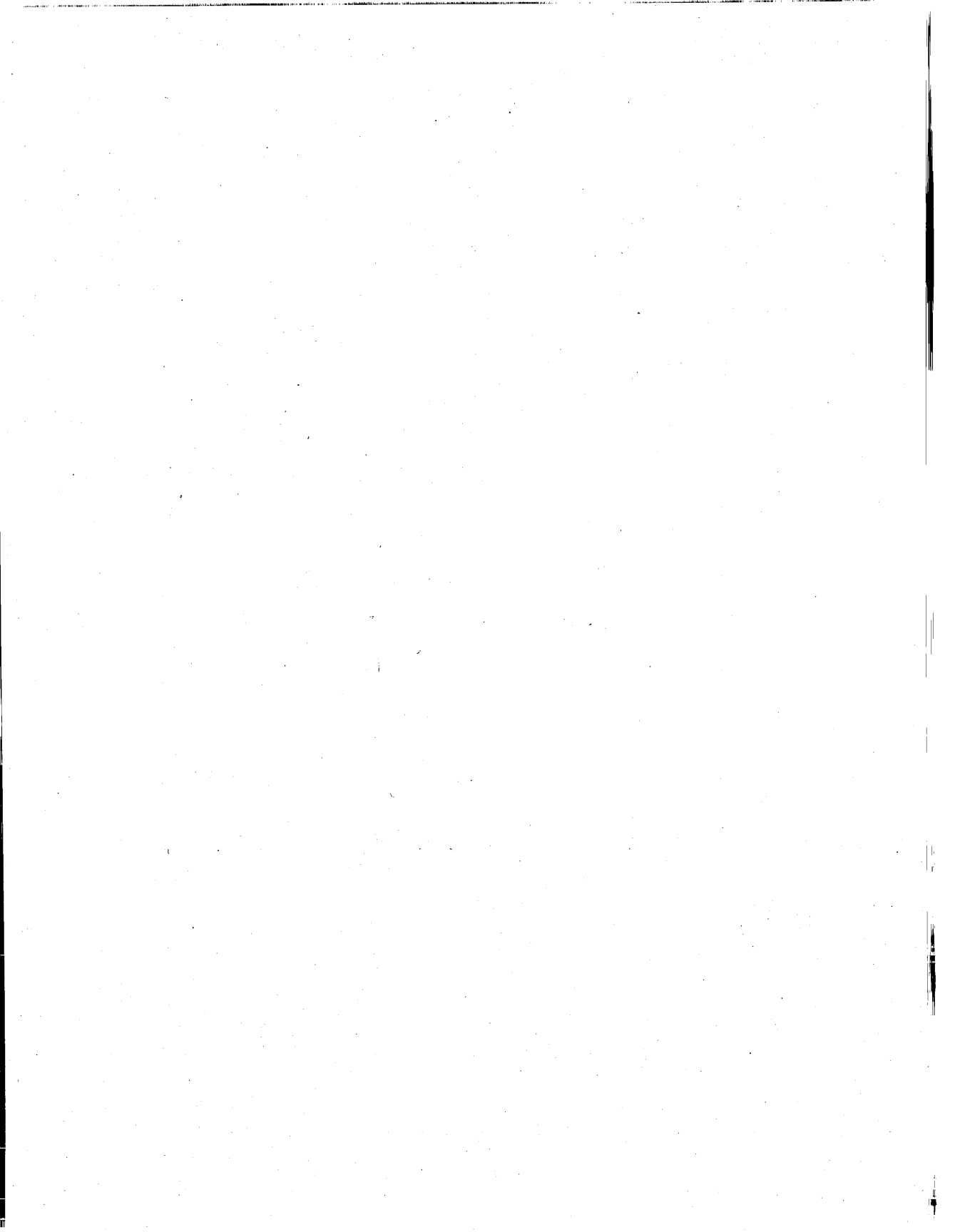
1233

Function Guide	1
1M DRAM Data Sheet	2
4M DRAM Data Sheet	3
4M B/W DRAM Data Sheet	4
16M DRAM Data Sheet	5
16M B/W DRAM Data Sheet	6
64M DRAM Data Sheet	7
Sales Offices and Manufacturer's Representatives	8

FUNCTION GUIDE 1

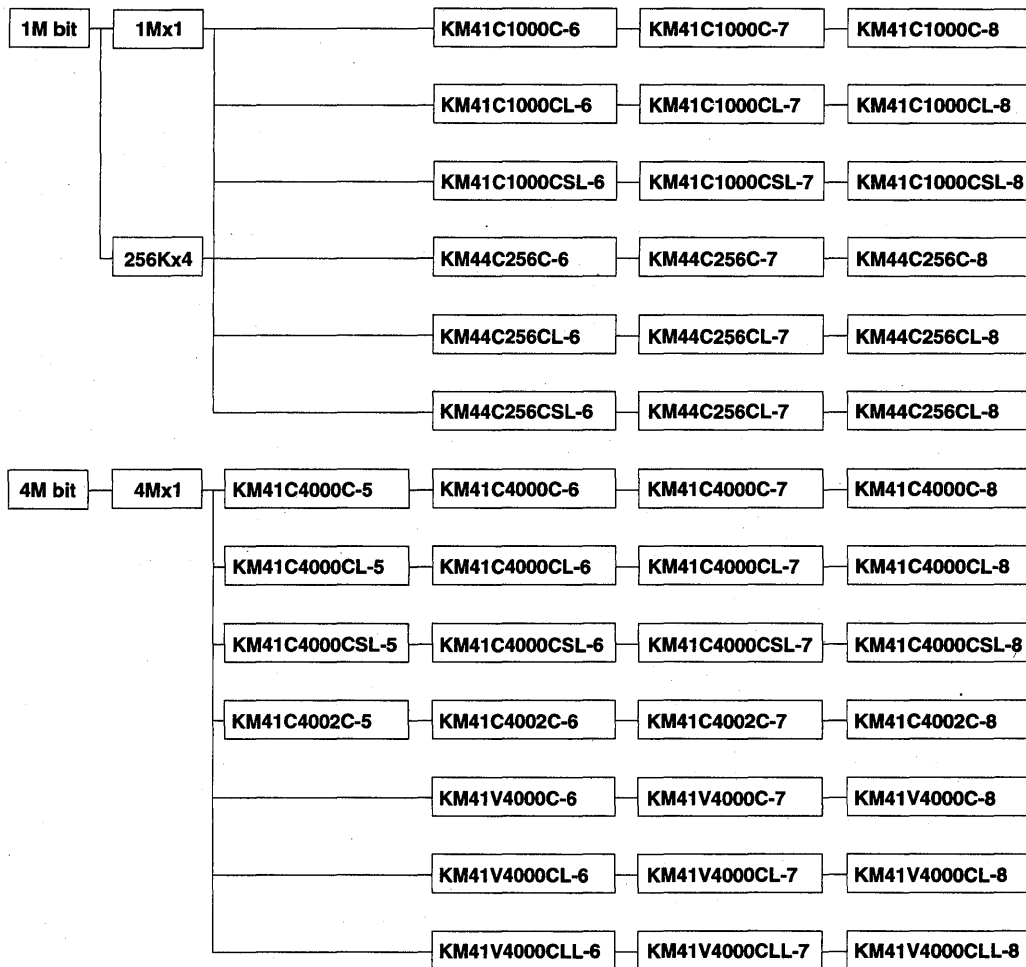
1. Introduction
2. Product Guide
3. Cross Reference
4. Ordering Info



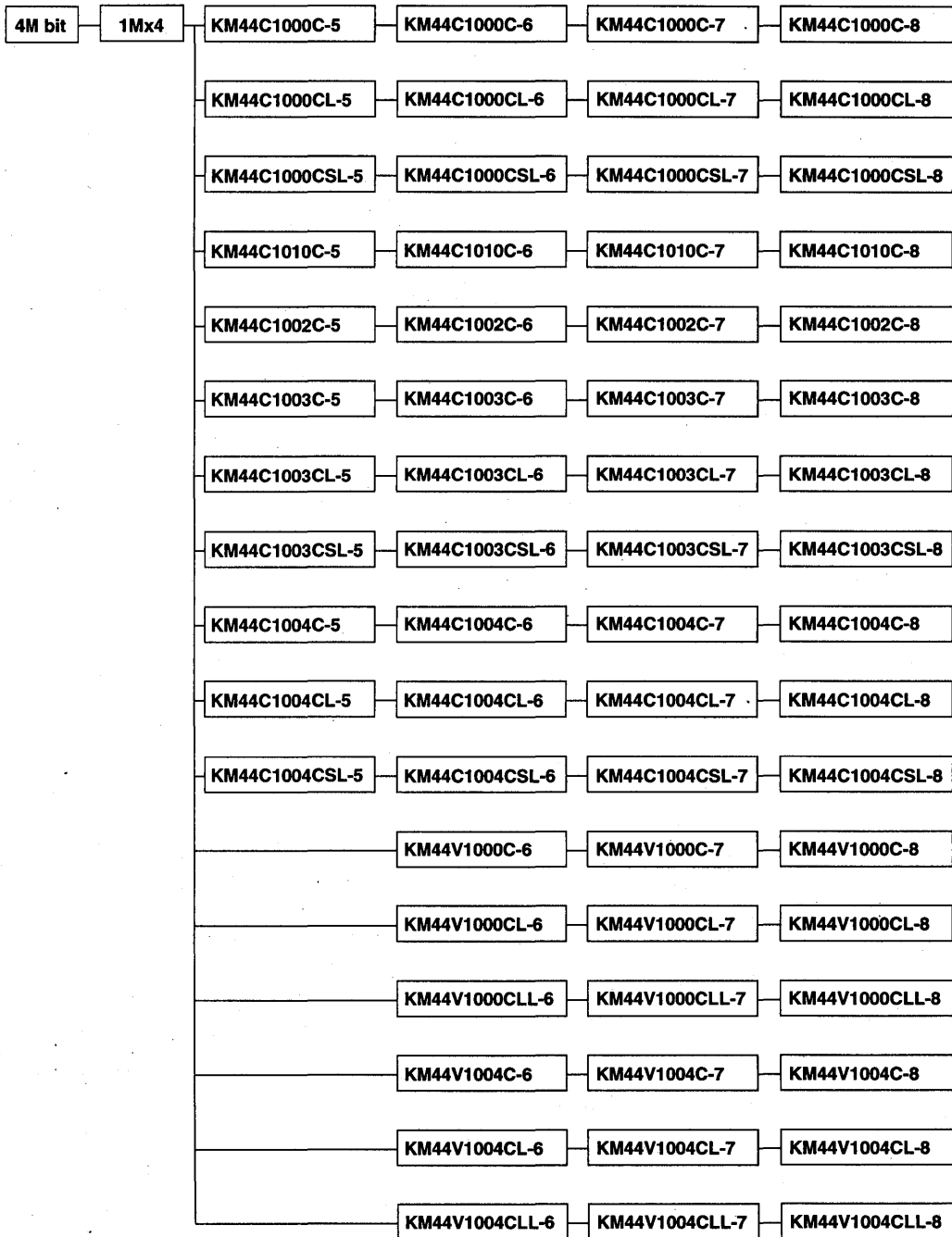


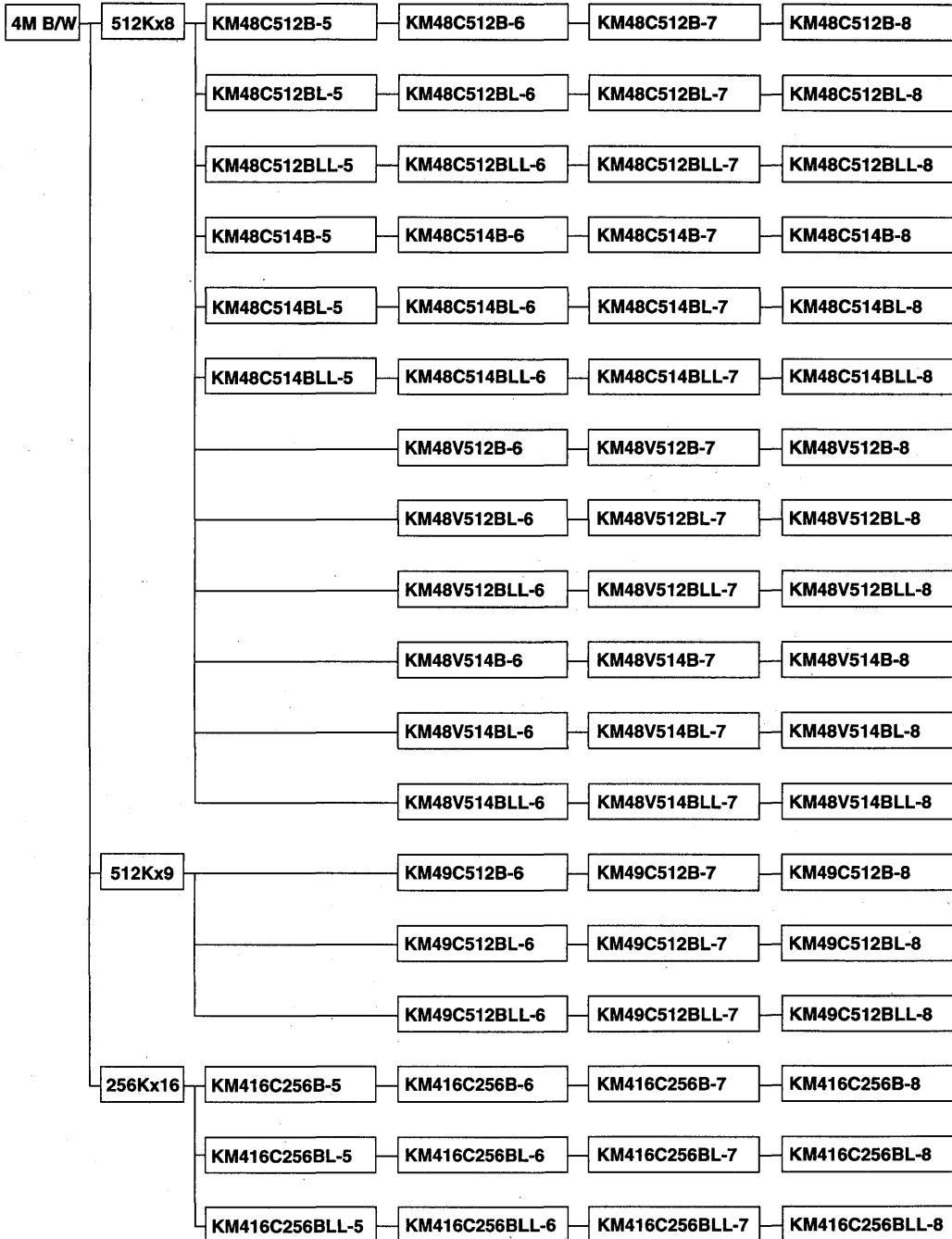
1. INTRODUCTION

1.1 Dynamic RAM

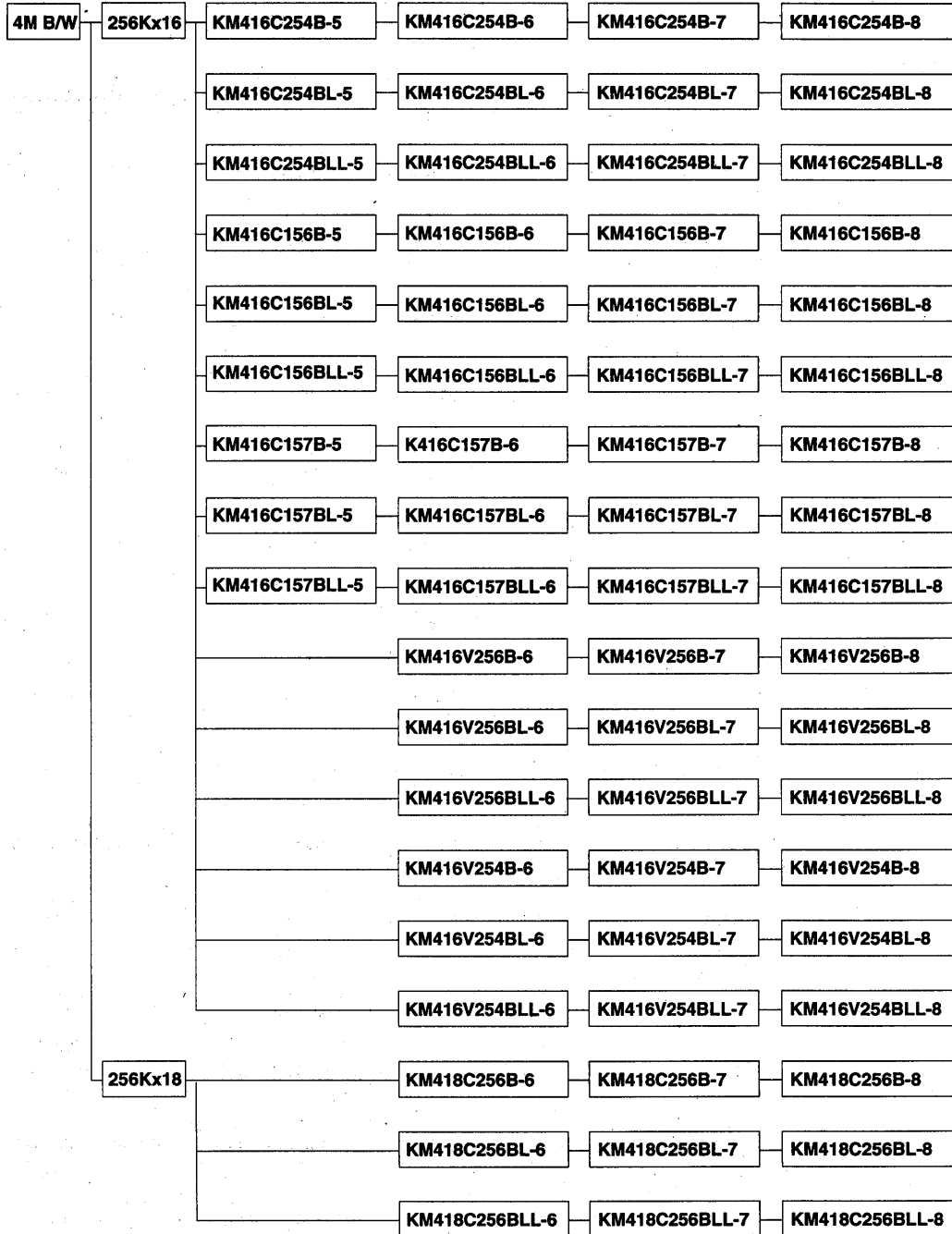


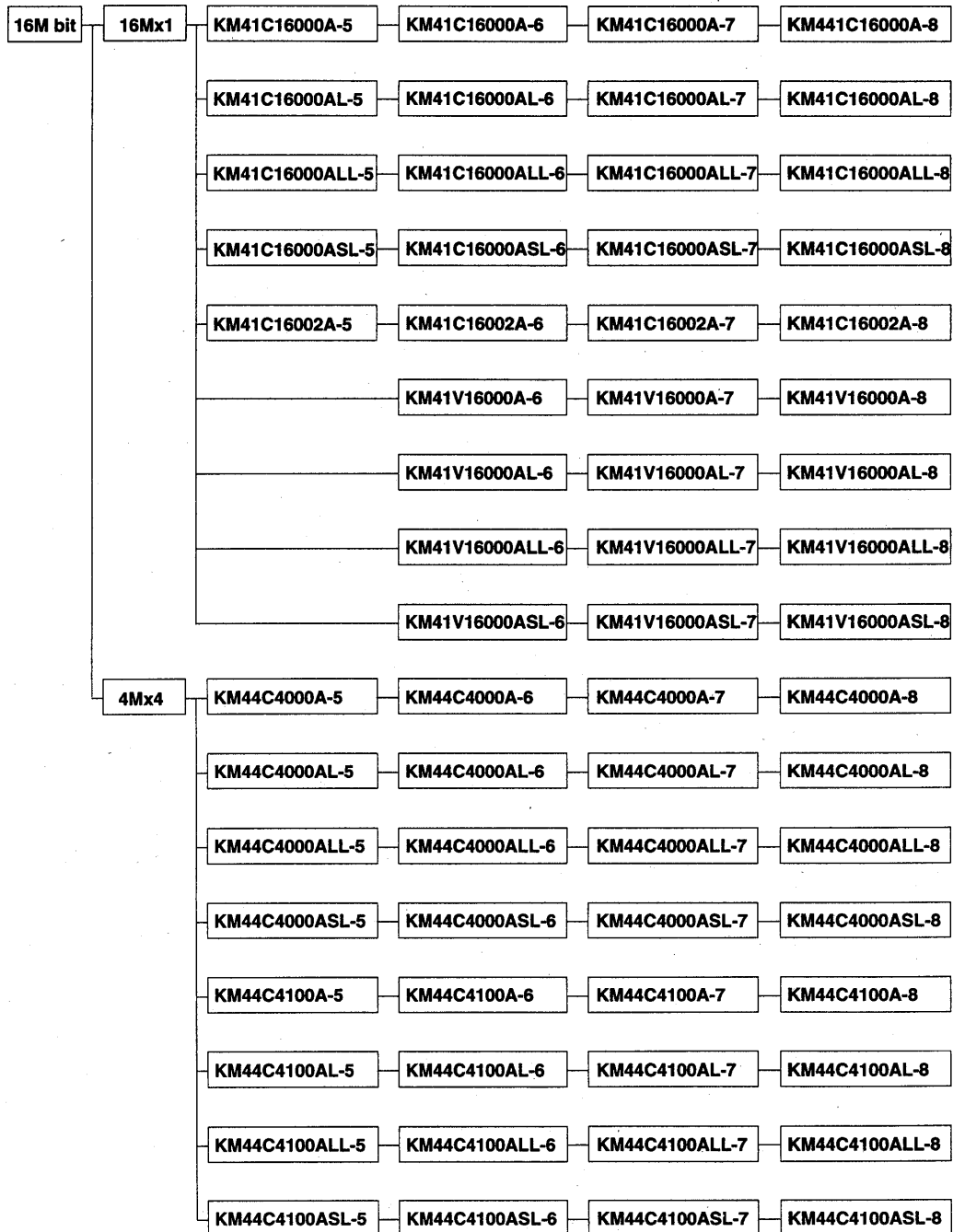
1



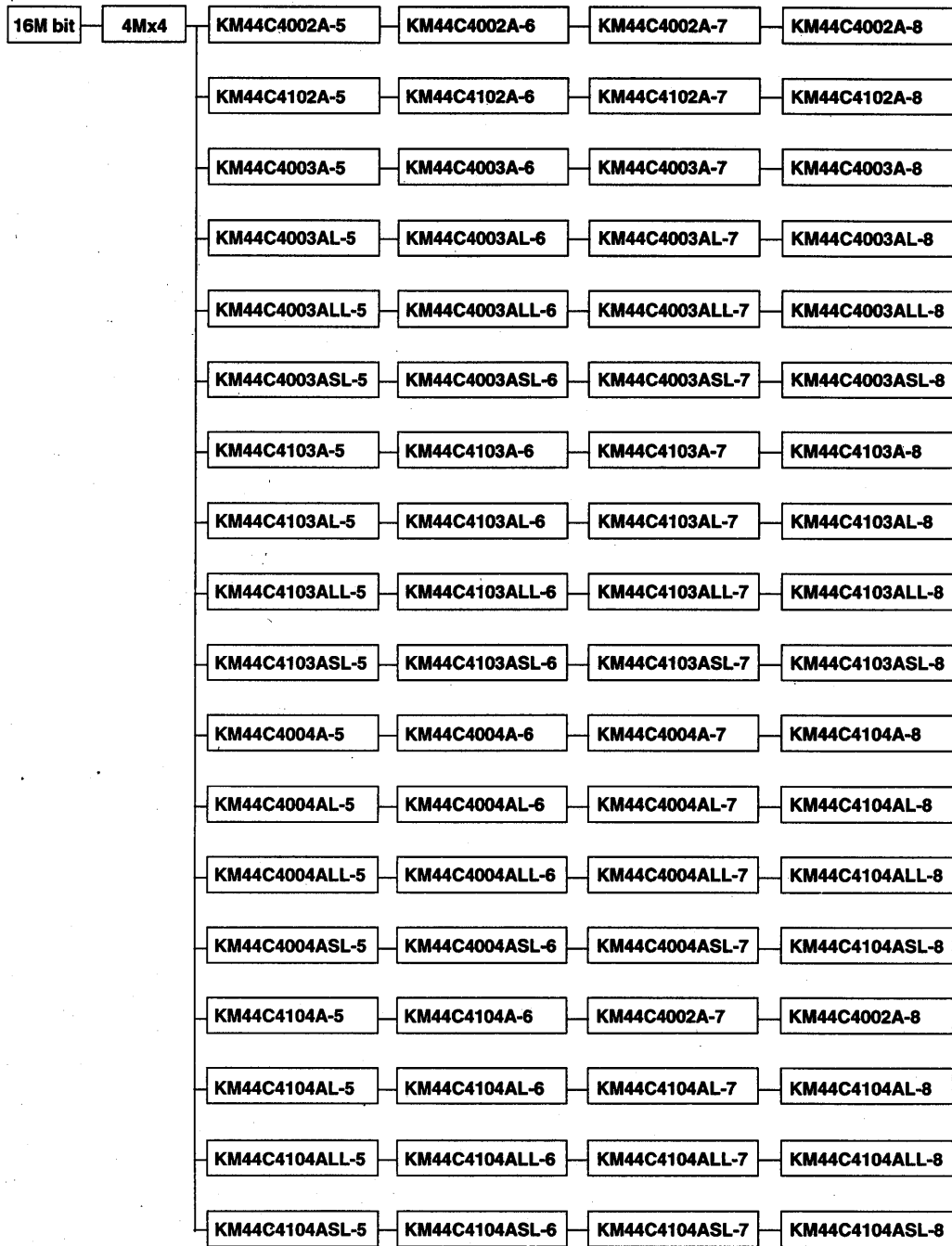


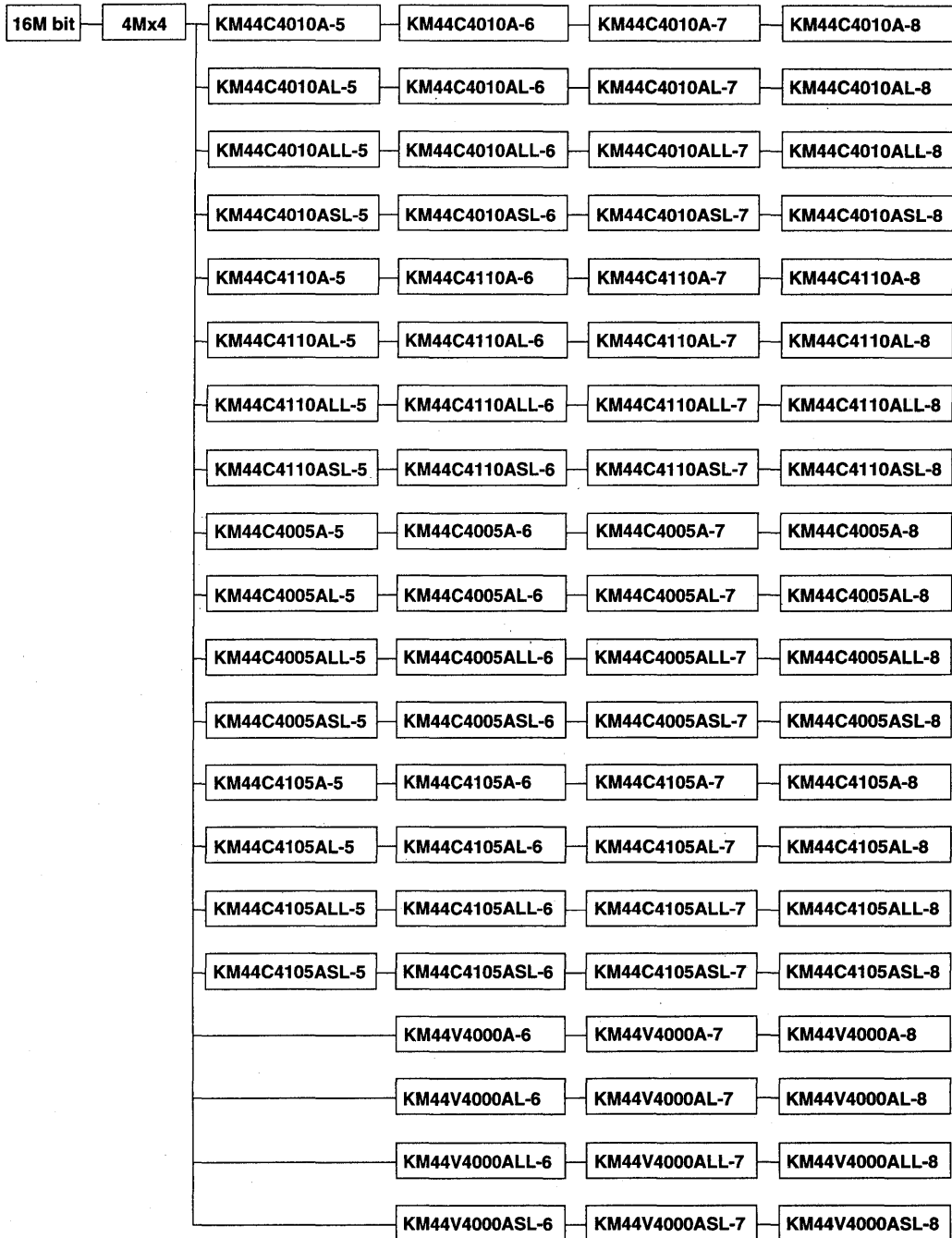
1



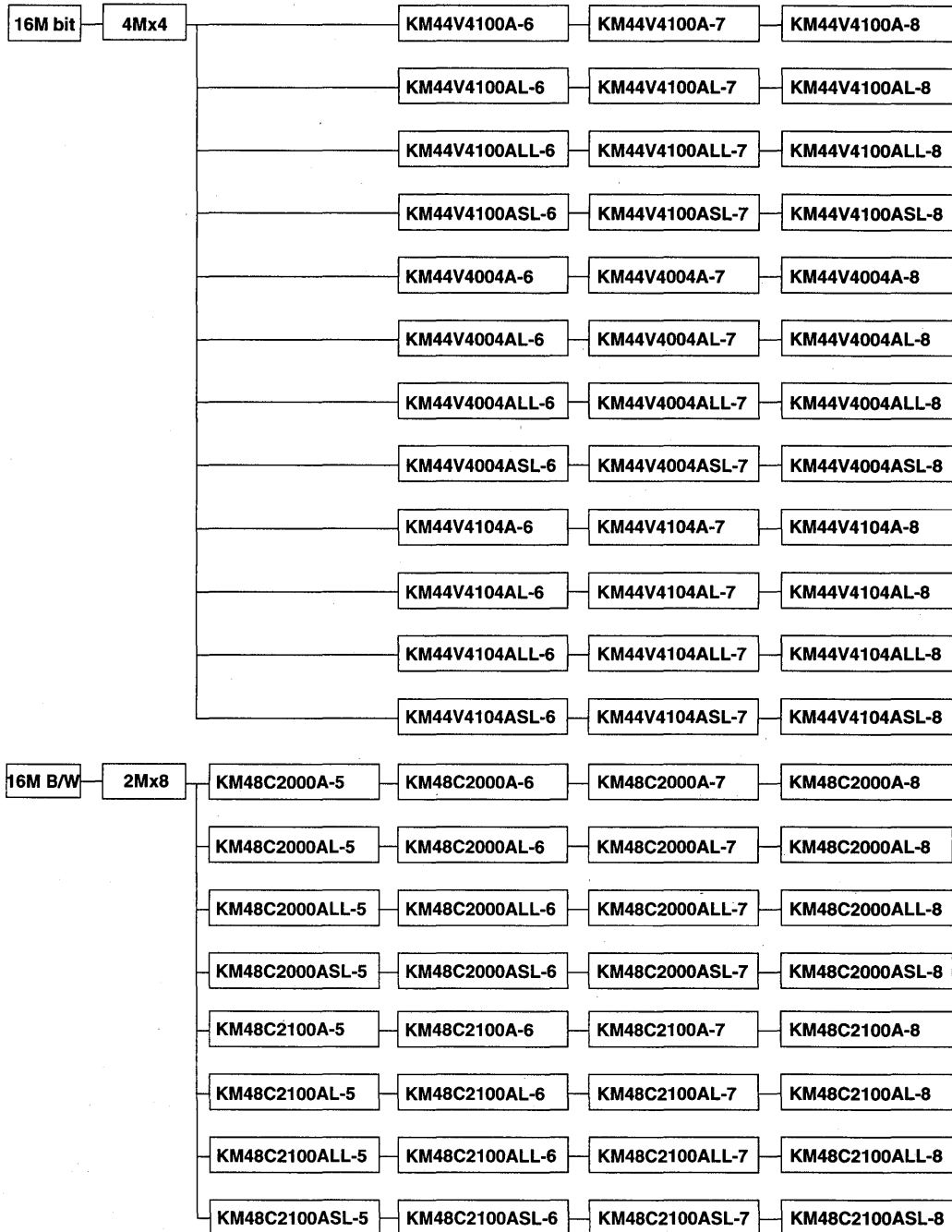


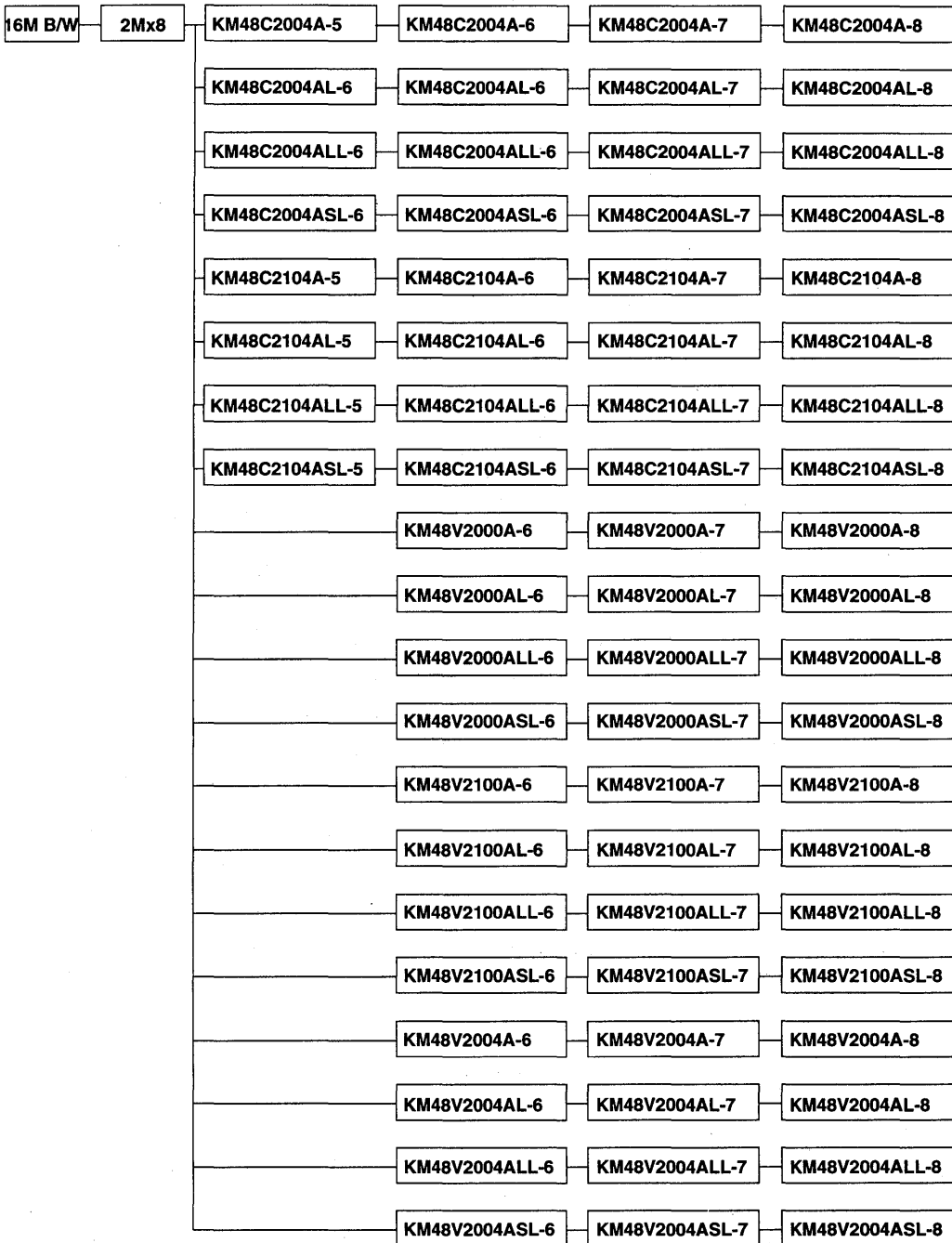
1



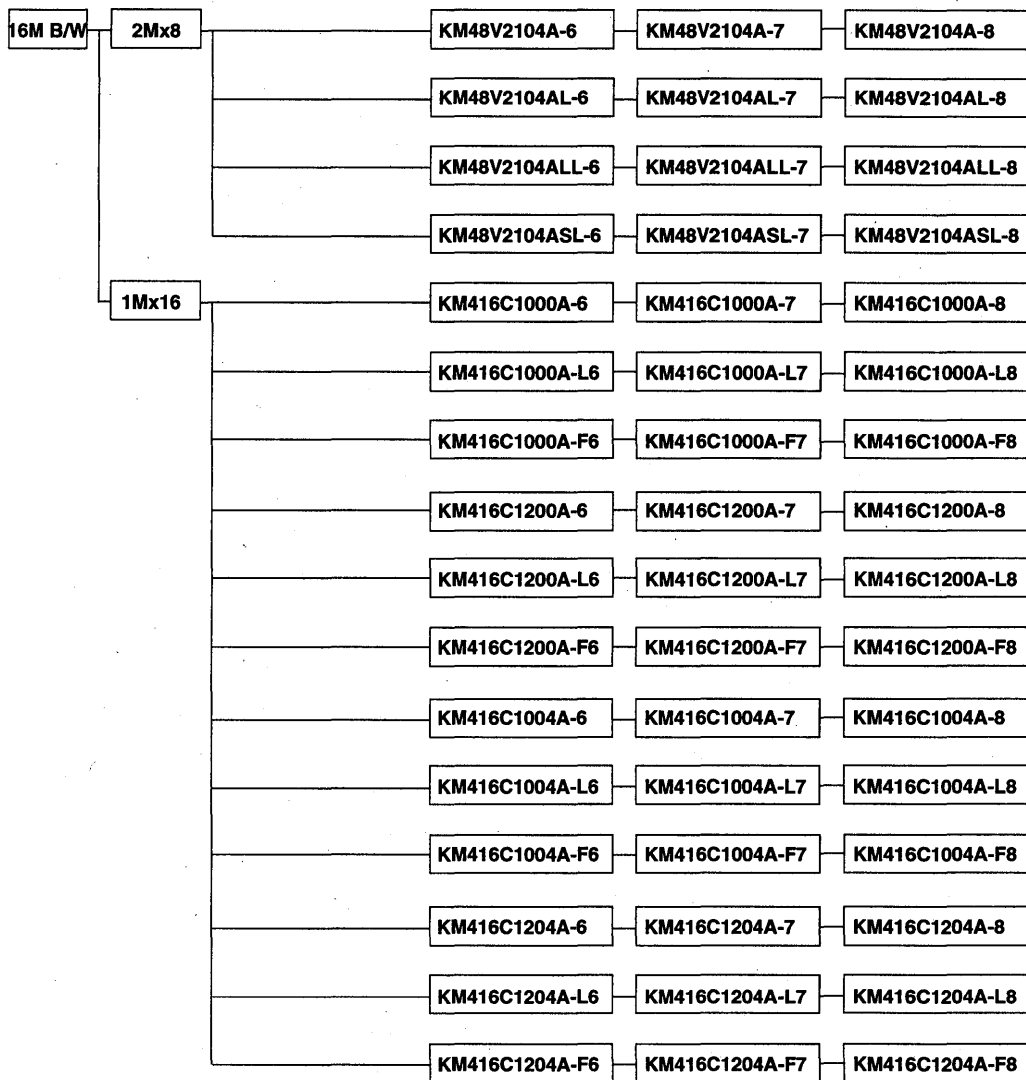


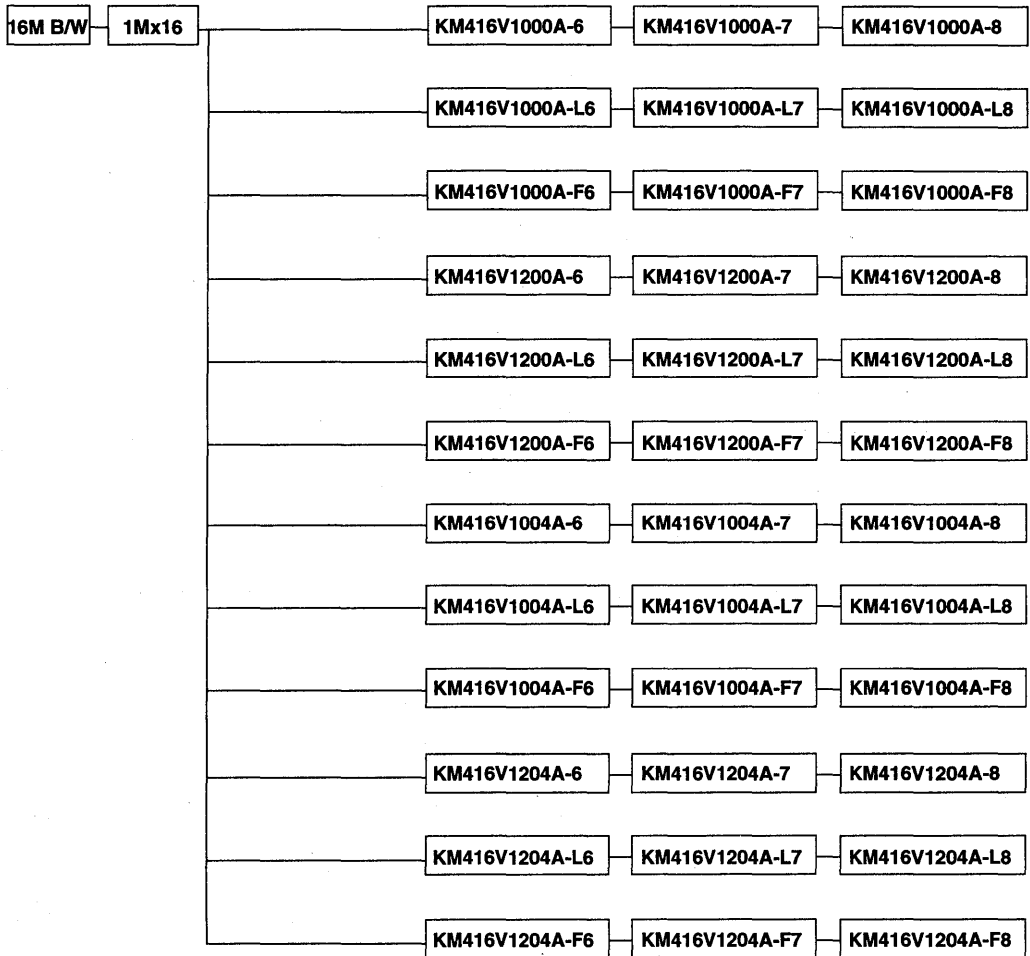
1



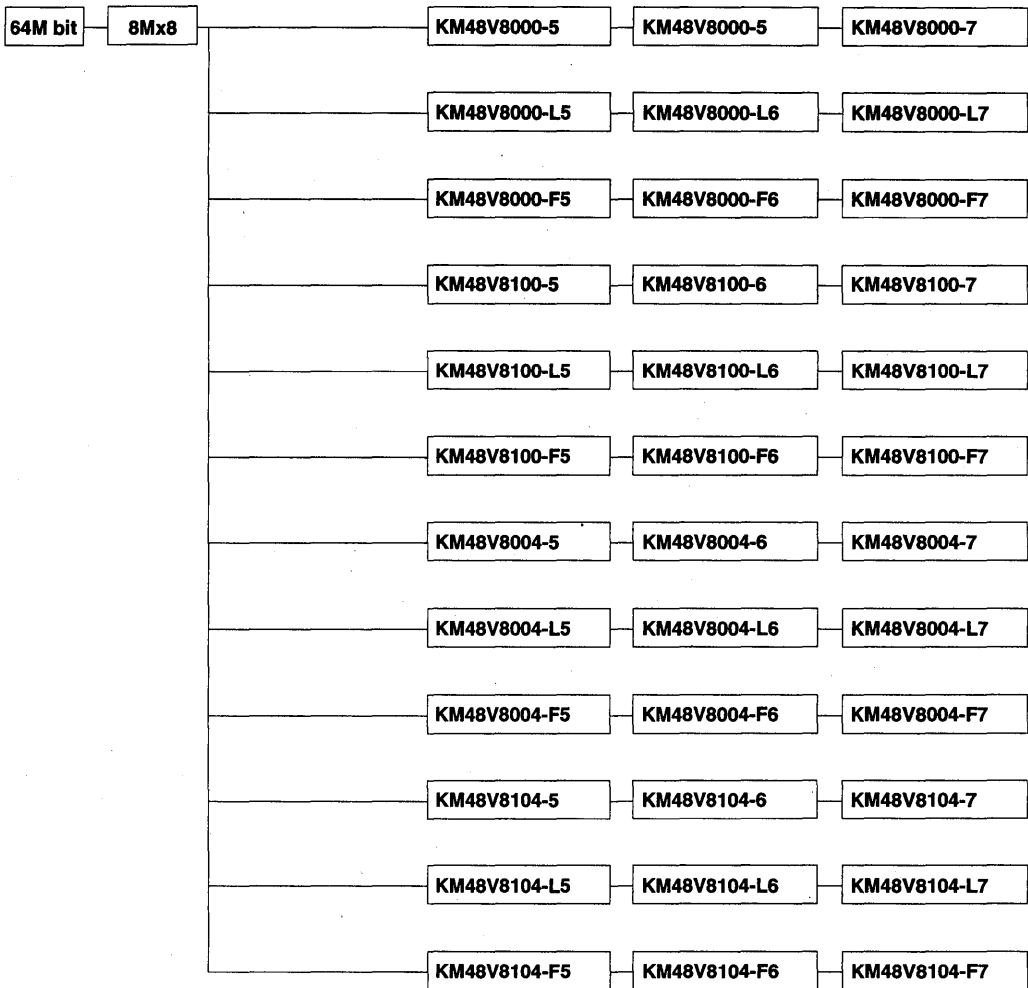


1





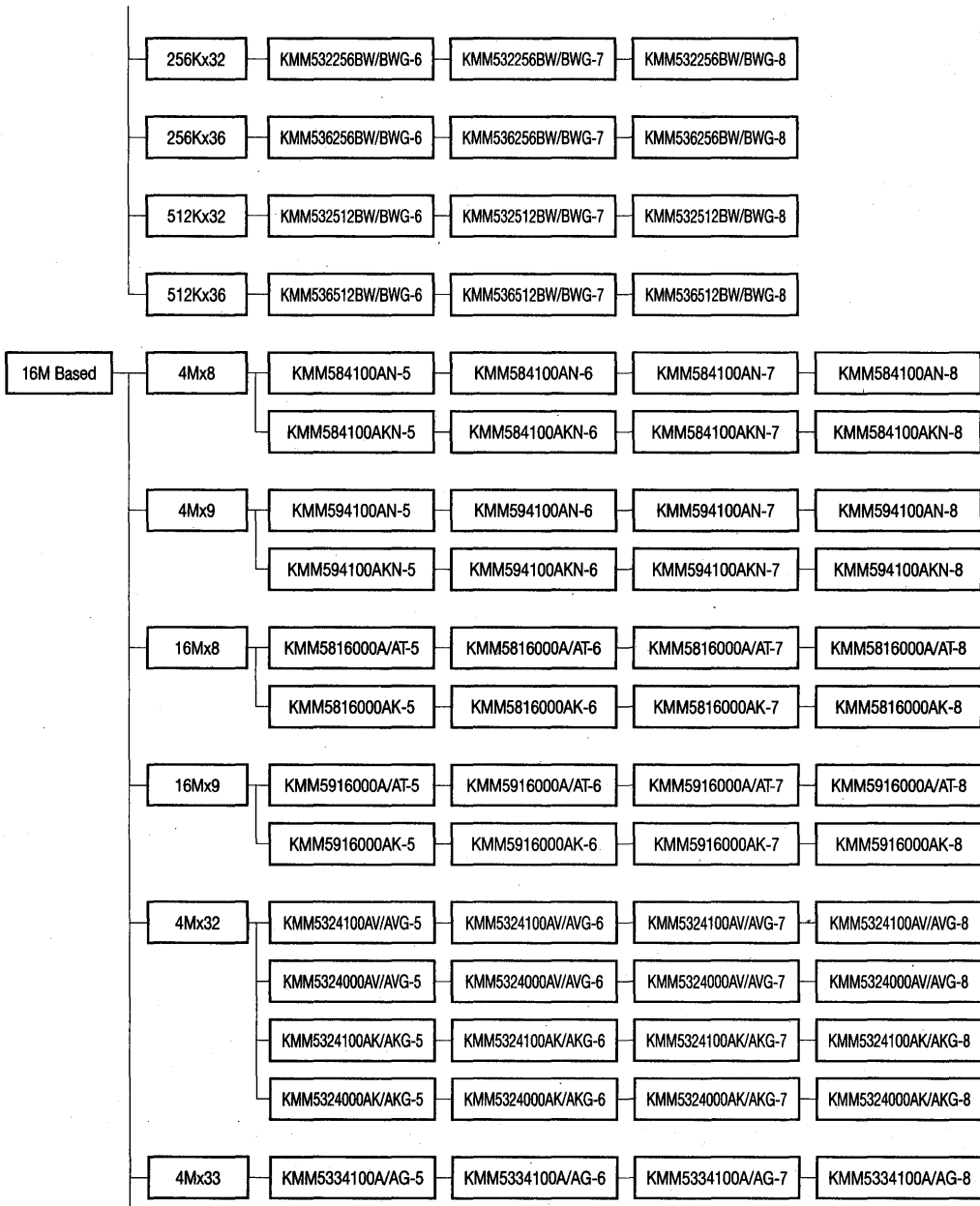
1



1.2 Dynamic RAM Module

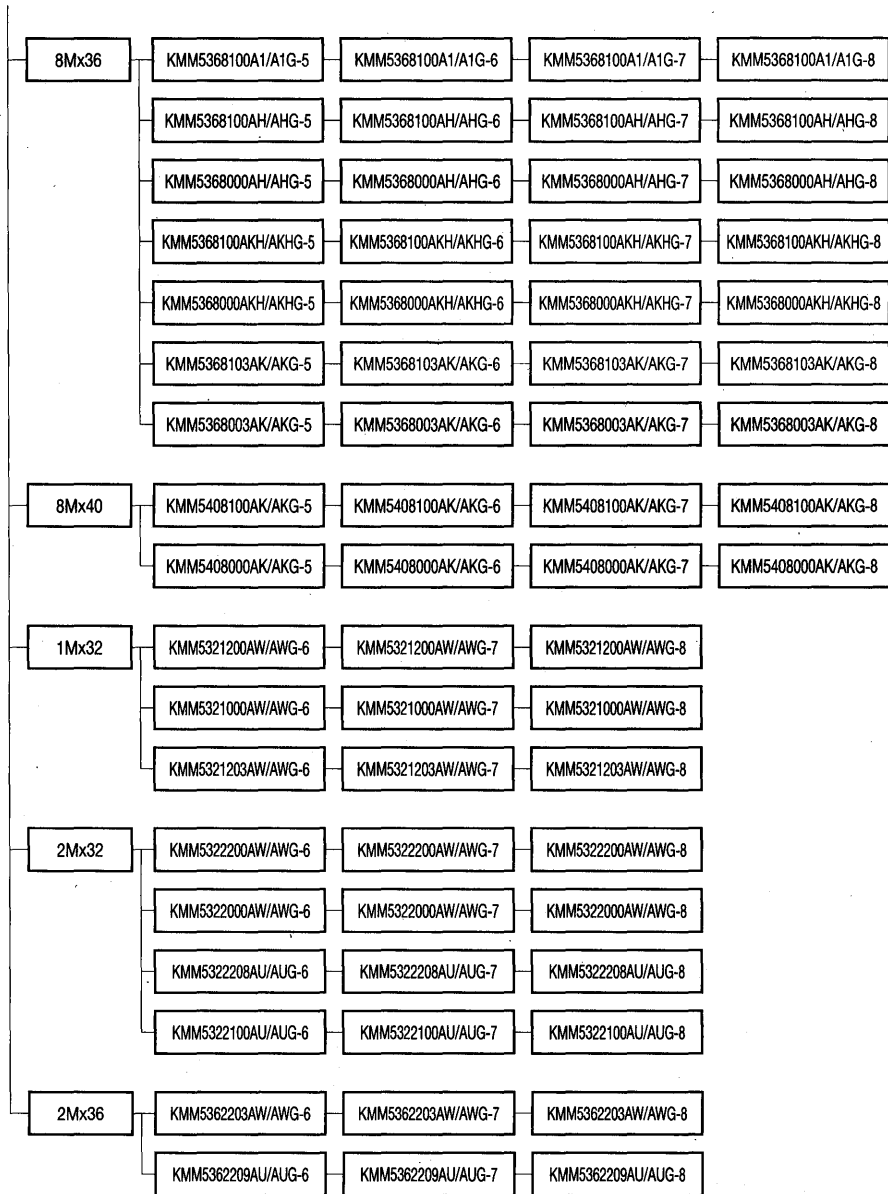
4M Based	1Mx8	KMM581000CN-6	KMM581000CN-7	KMM581000CN-8	
	1Mx9	KMM591000CN-6	KMM591000CN-7	KMM591000CN-8	
	4Mx8	KMM584000C-5	KMM584000C-6	KMM584000C-7	KMM584000C-8
	4Mx9	KMM594000C-5	KMM594000C-6	KMM594000C-7	KMM594000C-8
	1Mx32	KMM5321000CV/CVG-5	KMM5321000CV/CVG-6	KMM5321000CV/CVG-7	KMM5321000CV/CVG-8
	1Mx33	KMM5331000C/CG-6	KMM5331000C/CG-7	KMM5331000C/CG-8	
	1Mx36	KMM5361000C2/C2G-6	KMM5361000C2/C2G-7	KMM5361000C2/C2G-8	
		KMM5361000CH-5	KMM5361000CH-6	KMM5361000CH-7	KMM5361000CH-8
		KMM5361003C/CG-5	KMM5361003C/CG-6	KMM5361003C/CG-7	KMM5361003C/CG-8
	1Mx40	KMM5401000C/CG/CM-5	KMM5401000C/CG/CM-6	KMM5401000C/CG/CM-7	KMM5401000C/CG/CM-8
	2Mx32	KMM5322000CV/CVG-5	KMM5322000CV/CVG-6	KMM5322000CV/CVG-7	KMM5322000CV/CVG-8
	2Mx36	KMM5362000C2/C2G-6	KMM5362000C2/C2G-7	KMM5362000C2/C2G-8	
		KMM5362000CH-5	KMM5362000CH-6	KMM5362000CH-7	KMM5362000CH-8
		KMM5362003C/CG-5	KMM5362003C/CG-6	KMM5362003C/CG-7	KMM5362003C/CG-8
	2Mx40	KMM5402000C/CG/CM-5	KMM5402000C/CG/CM-6	KMM5402000C/CG/CM-7	KMM5402000C/CG/CM-8
	4Mx32	KMM5324000CV/CVG-5	KMM5324000CV/CVG-6	KMM5324000CV/CVG-7	KMM5324000CV/CVG-8
	4Mx33	KMM5334000CV/CVG-5	KMM5334000CV/CVG-6	KMM5334000CV/CVG-7	KMM5334000CV/CVG-8
	4Mx36	KMM5364000C/CG-5	KMM5364000C/CG-6	KMM5364000C/CG-7	KMM5364000C/CG-8

1

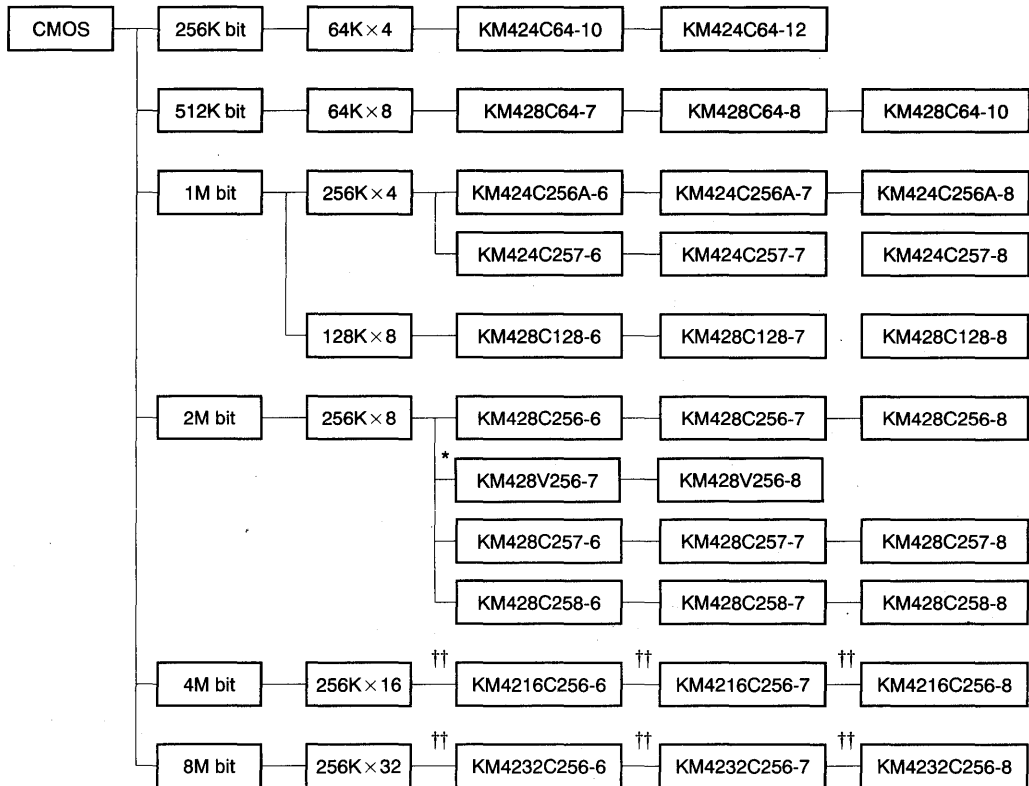


4Mx36	KMM5364100A/AG-5	KMM5364100A/AG-6	KMM5364100A/AG-7	KMM5364100A/AG-8
	KMM5364100A1/A1G-5	KMM5364100A1/A1G-6	KMM5364100A1/A1G-7	KMM5364100A1/A1G-8
	KMM5364100AH/AHG-5	KMM5364100AH/AHG-6	KMM5364100AH/AHG-7	KMM5364100AH/AHG-8
	KMM5364000AH/AHG-5	KMM5364000AH/AHG-6	KMM5364000AH/AHG-7	KMM5364000AH/AHG-8
	KMM5364100AKH/AKHG-5	KMM5364100AKH/AKHG-6	KMM5364100AKH/AKHG-7	KMM5364100AKH/AKHG-8
	KMM5364000AKH/AKHG-5	KMM5364000AKH/AKHG-6	KMM5364000AKH/AKHG-7	KMM5364000AKH/AKHG-8
	KMM5364103AK/AGK-5	KMM5364103AK/AGK-6	KMM5364103AK/AGK-7	KMM5364103AK/AGK-8
	KMM5364003AK/AGK-5	KMM5364003AK/AGK-6	KMM5364003AK/AGK-7	KMM5364003AK/AGK-8
4Mx39	KMM5394100AM-5	KMM5394100AM-6	KMM5394100AM-7	KMM5394100AM-8
	KMM5394000AM-5	KMM5394000AM-6	KMM5394000AM-7	KMM5394000AM-8
4Mx40	KMM5404100A/AG-5	KMM5404100A/AG-6	KMM5404100A/AG-7	KMM5404100A/AG-8
	KMM5404000A/AG-5	KMM5404000A/AG-6	KMM5404000A/AG-7	KMM5404000A/AG-8
	KMM5404100AK/AGK-5	KMM5404100AK/AGK-6	KMM5404100AK/AGK-7	KMM5404100AK/AGK-8
	KMM5404000AK/AGK-5	KMM5404000AK/AGK-6	KMM5404000AK/AGK-7	KMM5404000AK/AGK-8
8Mx32	KMM5328100AV/AVG-5	KMM5328100AV/AVG-6	KMM5328100AV/AVG-7	KMM5328100AV/AVG-8
	KMM5328000AV/AVG-5	KMM5328000AV/AVG-6	KMM5328000AV/AVG-7	KMM5328000AV/AVG-8
	KMM5328100AK/AGK-5	KMM5328100AK/AGK-6	KMM5328100AK/AGK-7	KMM5328100AK/AGK-8
	KMM5328000AK/AGK-5	KMM5328000AK/AGK-6	KMM5328000AK/AGK-7	KMM5328000AK/AGK-8
8Mx33	KMM5338100AKV/AVKG-5	KMM5338100AKV/AVKG-6	KMM5338100AKV/AVKG-7	KMM5338100AKV/AVKG-8

1



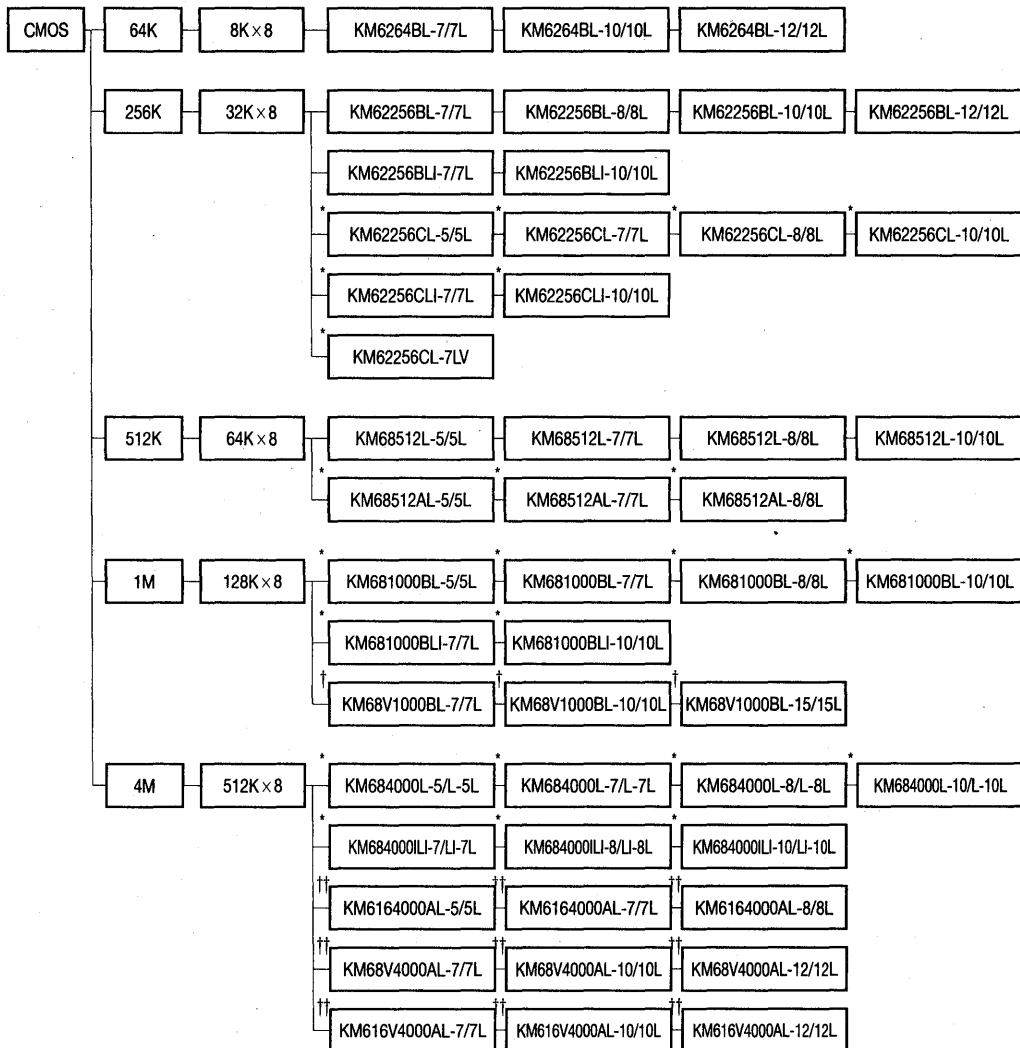
1.3 Video RAM



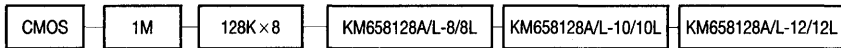
†† Under Development

1.4 Static RAM

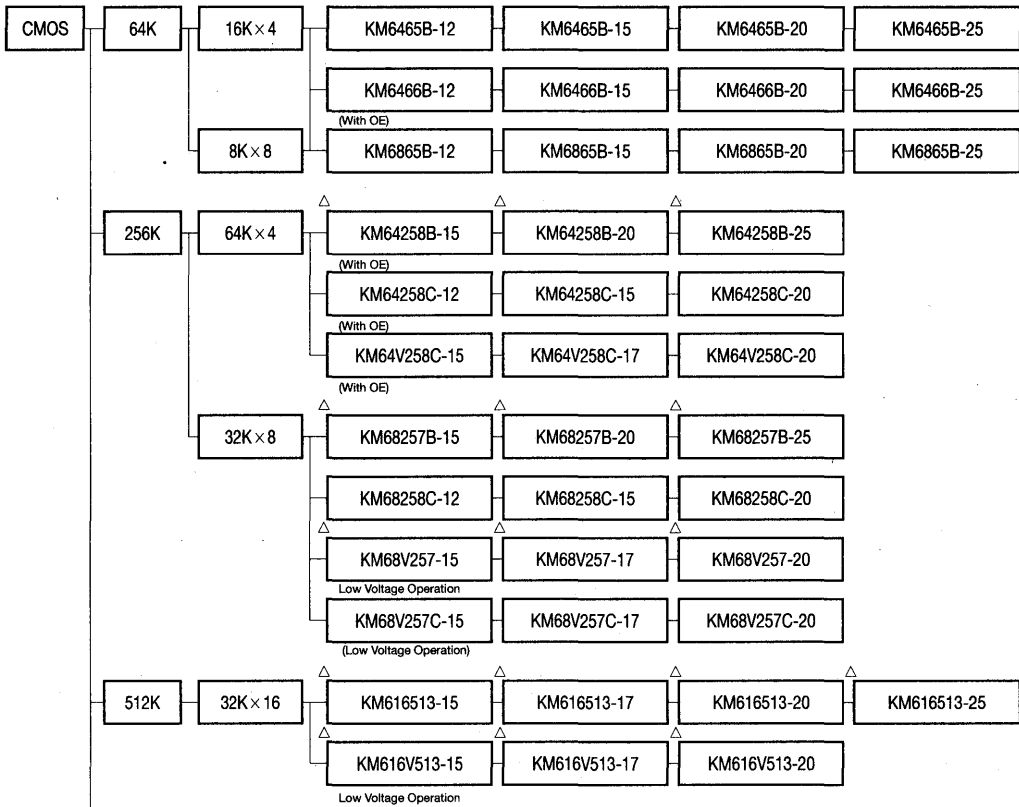
Standard SRAM



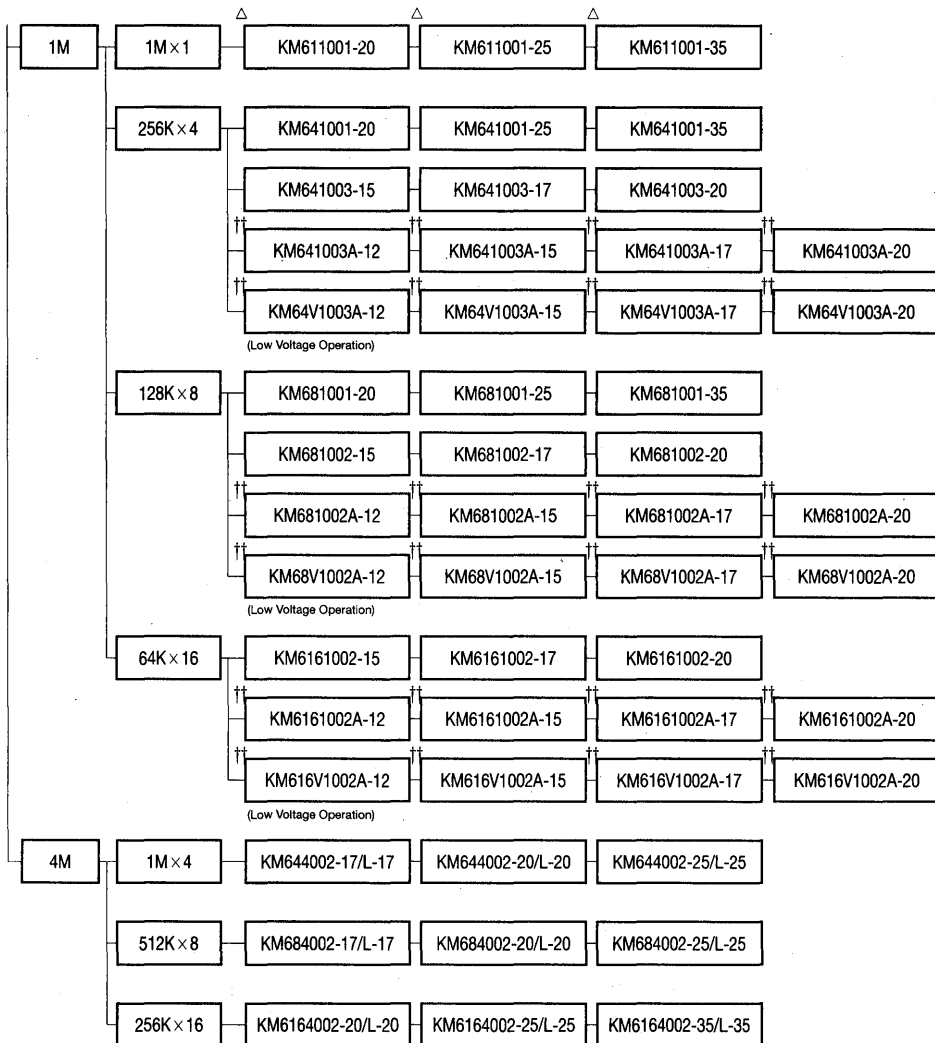
Pseudo SRAM



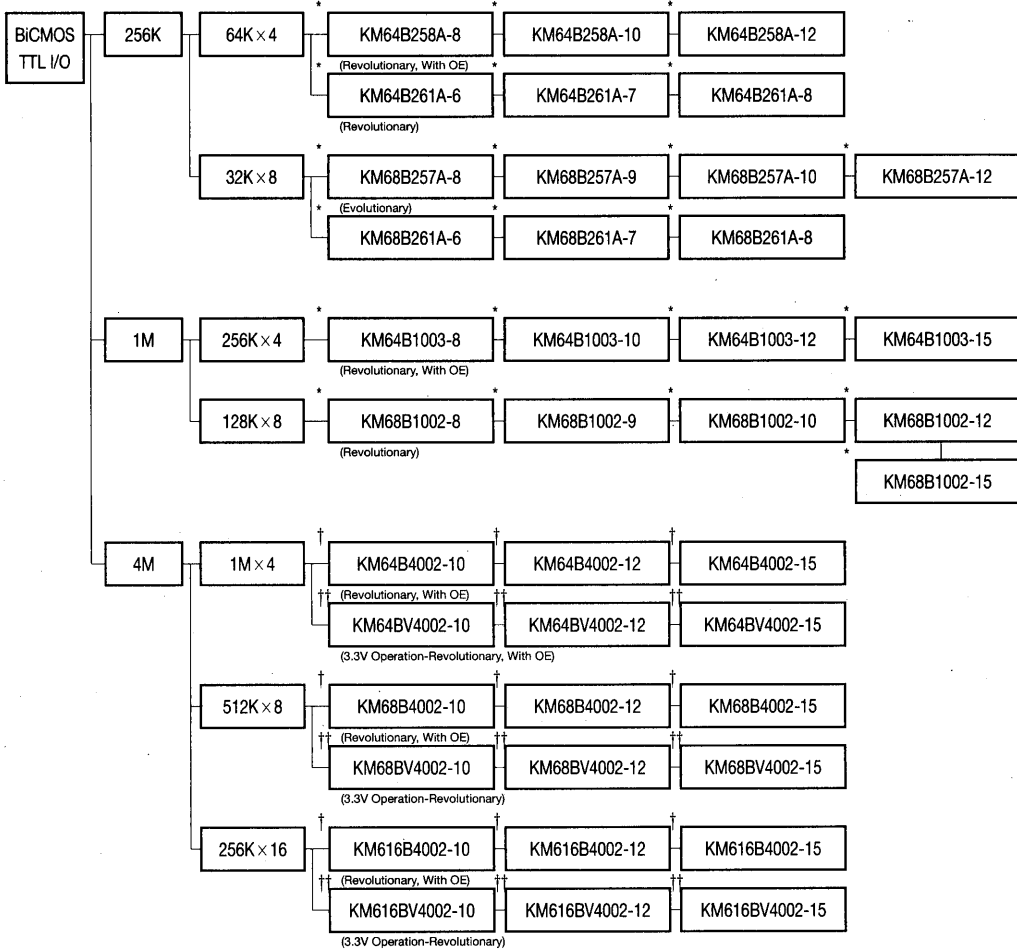
High Speed SRAM



1

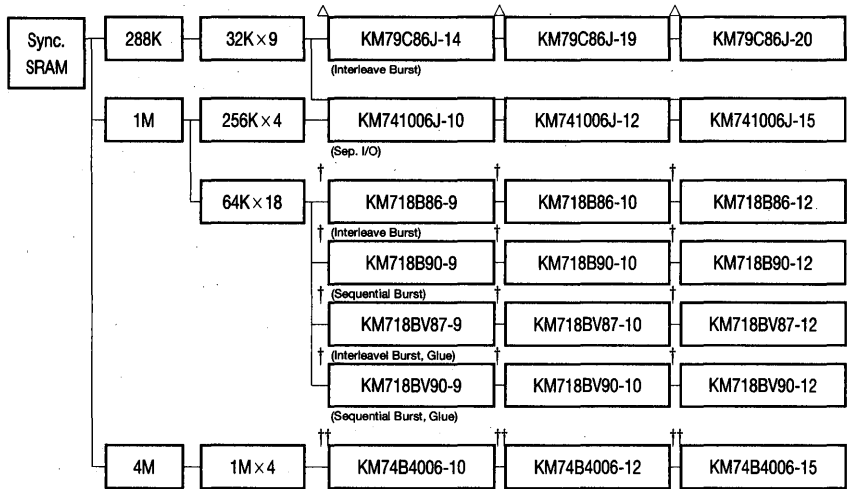


BiCMOS SRAM



1

Specialty SRAM



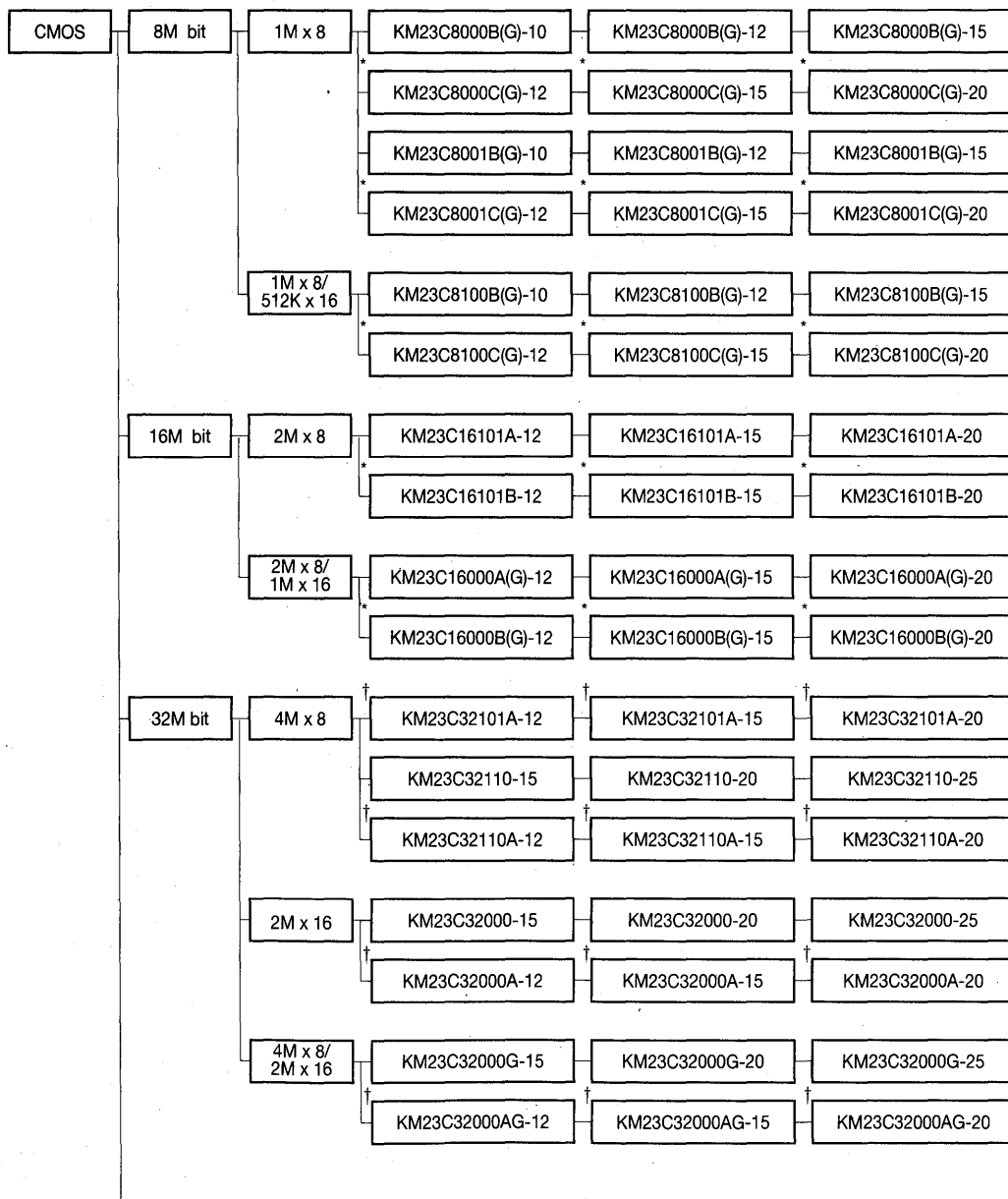
* : New Product † : Preliminary Product †† : Advanced Information △ : Last Time by Product

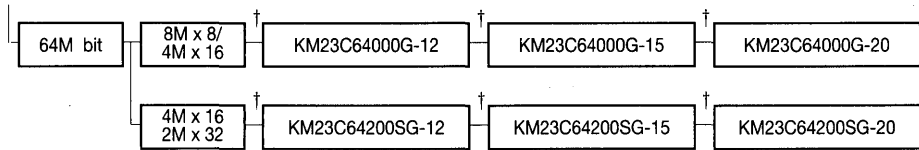
1.5 MASK ROM

Standard Product

CMOS	256K bit	32K x 8	KM23C256(G)-12	KM23C256(G)-15	KM23C256(G)-20	
	512K bit	64K x 8	KM23C512(G)-12	KM23C512(G)-15	KM23C512(G)-20	
	1M bit	128K x 8	KM23C1000-12	KM23C1000-15	KM23C1000-20	
			KM23C1001-12	KM23C1001-15	KM23C1001-20	
			KM23C1010(G)-12	KM23C1010(G)-15	KM23C1010(G)-20	
			KM23C1011(G)-12	KM23C1011(G)-15	KM23C1011(G)-20	
	2M bit	256K x 8	KM23C2000A(G)-10	KM23C2000A(G)-12	KM23C2000A(G)-15	
			KM23C2000B(G)-10	KM23C2000B(G)-12	KM23C2000B(G)-15	
			KM23C2001A(G)-10	KM23C2001A(G)-12	KM23C2001A(G)-15	
			KM23C2001B(G)-10	KM23C2001B(G)-12	KM23C2001B(G)-15	
		256K x 8/ 128K x 16	KM23C2100A-10	KM23C2100A-12	KM23C2100A-15	
			KM23C2100B-10	KM23C2100B-12	KM23C2100B-15	
		4M bit	512K x 8	KM23C4000B(G)-10	KM23C4000B(G)-12	KM23C4000B(G)-15
				KM23C4000C(G)-10	KM23C4000C(G)-12	KM23C4000C(G)-15
				KM23C4001B(G)-10	KM23C4001B(G)-12	KM23C4001B(G)-15
				KM23C4001C(G)-10	KM23C4001C(G)-12	KM23C4100B(G)-15
			512K x 8/ 256K x 16	KM23C4100B(G)-10	KM23C4100B(G)-12	KM23C4100B(G)-15
				KM23C4100C(G)-10	KM23C4100C(G)-12	KM23C4100C(G)-15
	KM23C4200B-12			KM23C4200B-15	KM23C4200B-20	
	KM23C4200C-10			KM23C4200C-12	KM23C4200C-15	

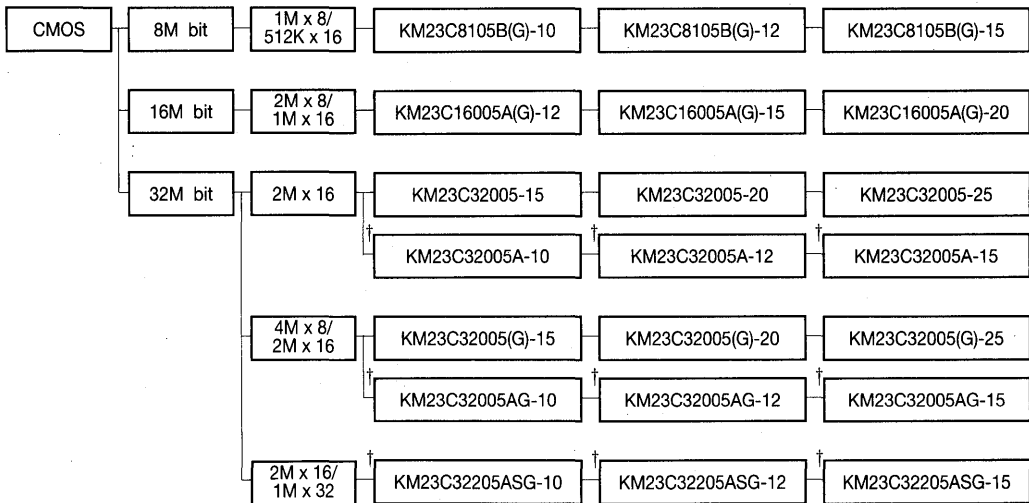
1



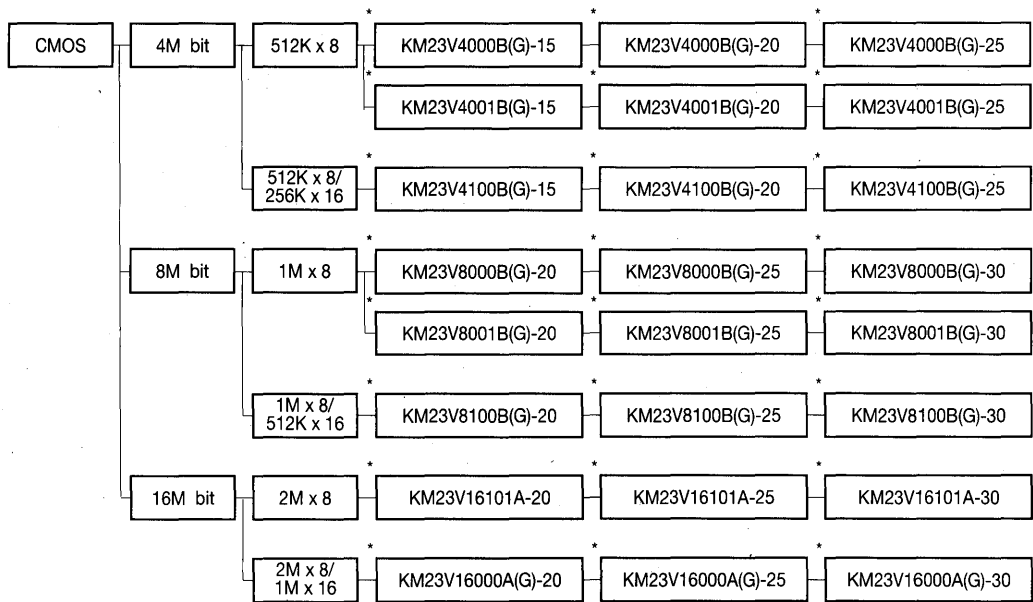


* : New Product
 † : Under Development

Page Mode Product



Low Voltage Product

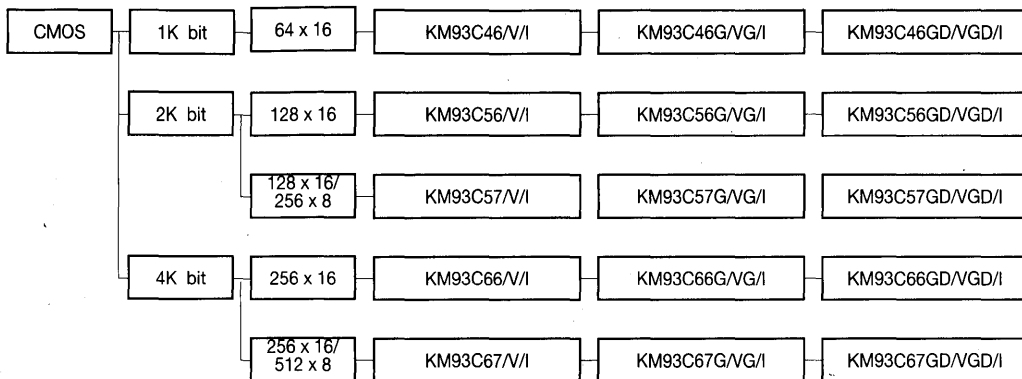


* : New Product

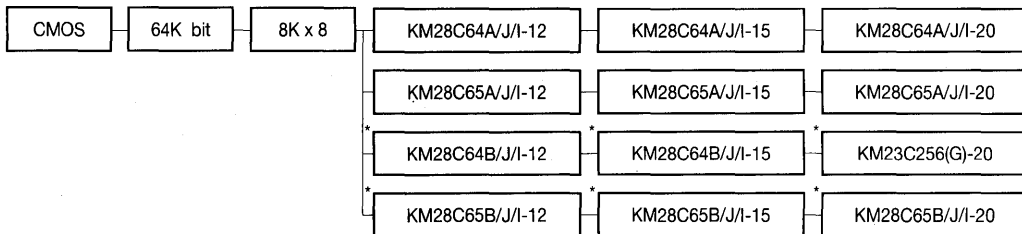
† : Under Development

1.6 EEPROM

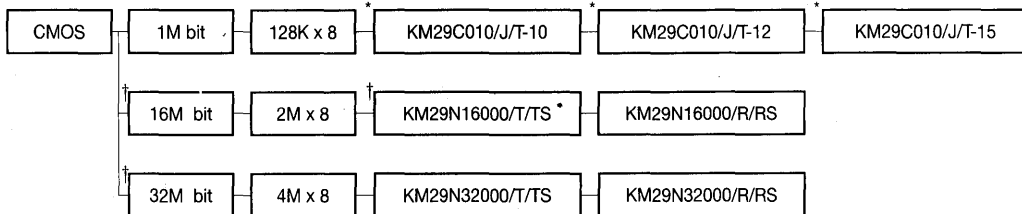
*Serial EEPROM



*Parallel EEPROM



1.7 Flash



* : New Product

† : Preliminary Product

2. PRODUCT GUIDE

2.1 Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
1M bit	1Mx1	5V±10%	KM41C1000C# KM41C1000CL# KM41C1000CSL#	60/70/80	Fast Page	P:18 Pin DIP J:20 Pin SOJ Z:20 Pin ZIP V:20 Pin TSOP-I (Forward) VR:20 Pin TSOP-I (Reverse) T:20 Pin TSOP-II (Forward) TR:20 Pin TSOP-II (Reverse)
	256Kx4	5V±10%	KM44C256C# KM44C256CL# KM44C256CSL#	60/70/80	Fast Page	
4M bit	4Mx1	5V±10%	KM41C4000C# KM41C4000CL# KM41C4000CSL# KM41C4002C#	50/60/70/80	Fast Page Static Column	P:20 Pin DIP J:20 Pin SOJ Z:20 Pin ZIP V:20 Pin TSOP-I (Forward) VR:20 Pin TSOP-I (Reverse) T:20 Pin TSOP-II (Forward) TR:20 Pin TSOP-II (Reverse)
		3.3V±10%	KM41V4000C# KM41V4000CL# KM41V4000CLL#	60/70/80	Fast Page	
	1Mx4	5V±10%	KM44C1000C# KM44C1000CL# KM44C1000CSL# KM44C1010C# KM44C1002C# KM44C1003C# KM44C1003CL# KM44C1003CSL# KM44C1004C# KM44C1004CL# KM44C1004CSL#	50/60/70/80	Fast Page Fast Page with WPB Static Column Quad CAS EDO	
		3.3V±10%	KM44V1000C# KM44V1000CL# KM44V1000CLL# KM44V1004C# KM44V1004CL# KM44V1004CLL#	60/70/80	Fast Page EDO	
4M B/W	512Kx8	5V±10%	KM48C512B# KM48C512BL#	50/60/70/80	Fast Page	

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)					
4M B/W	512Kx8	5V±10%	KM48C512BLL# KM48C514B# KM48C514BL# KM48C514BLL#	50/60/70/80	Fast Page EDO	J:28 Pin SOJ Z:28 Pin ZIP T:28 Pin TSOP-II (Forward) TR:28 Pin TSOP-II (Reverse)					
		3.3V±10%	KM48V512B# KM48V512BL# KM48V512BLL# KM48V514B# KM48V514BL# KM48V514BLL#	60/70/80	Fast Page EDO						
	512Kx9	5V±10%	KM49C512B# KM49C512BL# KM49C512BLL#	60/70/80	Fast Page						
	256Kx16	5V±10%	KM416C256B# KM416C256BL# KM416C256BLL# KM416C254B# KM416C254BL# KM416C254BLL# KM416C156B# KM416C156BL# KM416C156BLL# KM416C157B# KM416C157BL# KM416C157BLL#	50/60/70/80	Fast Page EDO Fast Page with 2WE						
							3.3V±10%	KM416V256B# KM416V256BL# KM416V256BLL# KM416V254B# KM416V254BL# KM416V254BLL#	60/70/80	Fast Page EDO	
							256Kx18	5V±10%	KM418C256B# KM418C256BL# KM418C256BLL#	60/70/80	Fast Page
							16M bit	16Mx1	5V±10%	KM41C16000A# KM41C16000AL# KM41C16000ALL# KM41C16000ASI #	50/60/70/80

1

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)	
16M bit	16Mx1	5V±10%	KM41C16002A#	50/60/70/80	Static Column(4K)	TR: 24 Pin TSOP-II (Reverse) (400mil) K: 24 Pin SOJ (300mil) S: 24 Pin TSOP-II(Forward) (300mil) SR: 24 Pin TSOP-II(Reverse) (300mil)	
		3.3V±10%	KM41V16000A# KM41V16000AL# KM41V16000ALL# KM41V16000ASL#	60/70/80	Fast Page(4K)		
4Mx4	4Mx4	5V±10%	KM44C4000A#	50/60/70/80	Fast Page(4K)	SR: 24 Pin TSOP-II(Reverse) (300mil)	
			KM44C4000AL#				
			KM44C4000ALL#				
			KM44C4000ASL#				
			KM44C4100A#				Fast Page(2K)
			KM44C4100AL#				
			KM44C4100ALL#				
			KM44C4100ASL#				
			KM44C4002A#				Static Column(4K) Static Column(2K)
			KM44C4102A#				
			KM44C4003A#				Quad CAS(4K)
			KM44C4003AL#				
			KM44C4003ALL#				
			KM44C4003ASL#				
			KM44C4103A#				Quad CAS(2K)
			KM44C4103AL#				
			KM44C4103ALL#				EDO(4K)
			KM44C4103ASL#				
			KM44C4004A#				
			KM44C4004AL#				
			KM44C4004ALL#				EDO(2K)
			KM44C4004ASL#				
			KM44C4104A#				
			KM44C4104AL#				
			KM44C4104ALL#				Fast Page with WPB (4K)
			KM44C4104ASL#				
			KM44C4010A#				
			KM44C4010AL#				
			KM44C4010ALL#				Fast Page with WPB (2K)
			KM44C4010ASL#				
			KM44C4110A#				
			KM44C4110AL#				
KM44C4110ALL#	EDO with Quad CAS (4K)						
KM44C4110ASL#							
KM44C4005A#							
KM44C4005AL#							
KM44C4005ALL#							

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M bit	4Mx4	5V±10%	KM44C4005ASL# KM44C4105A# KM44C4105AL# KM44C4105ALL# KM44C4105ASL#	50/60/70/80	EDO with Quad CAS (2K)	J: 24 Pin SOJ (400mil) T:24 Pin TSOP-II (Forward) (400mil) TR:24 Pin TSOP-II (Reverse) (400mil) K: 24 Pin SOJ (300mil)
		3.3V±10%	KM44V4000A# KM44V4000AL# KM44V4000ALL# KM44V4000ASL# KM44V4100A# KM44V4100AL# KM44V4100ALL# KM44V4100ASL# KM44V4004A# KM44V4004AL# KM44V4004ALL# KM44V4004ASL# KM44V4104A# KM44V4104AL# KM44V4104ALL# KM44V4104ASL#	60/70/80	Fast Page(4K) Fast Page(2K) EDO(4K) EDO(2K)	S:24 Pin TSOP-II (Forward) (300mil) SR:24 Pin TSOP-II(Reverse) (300mil)
16M B/W	2Mx8	5V±10%	KM48C2000A# KM48C2000AL# KM48C2000ALL# KM48C2000ASL# KM48C2100A# KM48C2100AL# KM48C2100ALL# KM48C2100ASL# KM48C2004A# KM48C2004AL# KM48C2004ALL# KM48C2004ASL# KM48C2104A# KM48C2104AL# KM48C2104ALL# KM48C2104ASL#	50/ 60/70/80	Fast Page(4K) Fast Page(2K) EDO(4K) EDO(2K)	J:28 Pin SOJ T:28 Pin TSOP-II (Forward) TR:24 Pin TSOP-II(Reverse)

1

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M B/W	2Mx8	3.3V±10%	KM48V2000A#	60/70/80	Fast Page(4K)	J:28 Pin SOJ T:28 Pin TSOP-II (Forward) TR:28 Pin TSOP-II(Reverse)
			KM48V2000AL#			
			KM48V2000ALL#		Fast Page(2K)	
			KM48V2100A#			
			KM48V2100AL#			
			KM48V2100ALL#		EDO(4K)	
			KM48V2004A#			
			KM48V2004AL#			
			KM48V2004ALL#		EDO(2K)	
			KM48V2104A#			
KM48V2104AL#						
KM48V2104ALL#						
1Mx16	5V±10%	3.3V±10%	KM416C1000A#	60/70/80	Fast Page(4K)	J:42 Pin SOJ T:44 Pin TSOP-II (Forward) R:44 Pin TSOP-II(Reverse)
			KM416C1000A#-L			
			KM416C1000A#-F		Fast Page(1K)	
			KM416C1200A#			
			KM416C1200A#-L			
			KM416C1200A#-F		EDO(4K)	
			KM416C1004A#			
			KM416C1004A#-L			
			KM416C1004A#-F		EDO(1K)	
			KM416C1204A#			
KM416C1204A#-L						
KM416C1204A#-F						
1Mx16	5V±10%	3.3V±10%	KM416V1000A#	60/70/80	Fast Page(4K)	
			KM416V1000A#-L			
			KM416V1000A#-F		Fast Page(1K)	
			KM416V1200A#			
			KM416V1200A#-L			
			KM416V1200A#-F			

Dynamic RAM

Density	Org.	Power Supply	Part Number	Speed(ns)	Features	Packages (#)
16M B/W	1Mx16	3.3V±10%	KM416V1004A# KM416V1004A#-L KM416V1004A#-F KM416V1204A# KM416V1204A#-L KM416V1204A#-F	50/60/70	EDO(4K) EDO(1K)	J:42 Pin SOJ T:44 Pin TSOP-II (Forward) R:44 Pin TSOP-II(Reverse)
64M bit	8Mx8	3.3V±10%	KM48V8000# KM48V8000#-L KM48V8000#-F KM48V8100# KM48V8100#-L KM48V8100#-F KM48V8004# KM48V8004#-L KM48V8004#-F KM48V8104# KM48V8104#-L KM48V8104#-F	50/60/70	Fast Page(8K) Fast Page(4K) EDO(8K) EDO(4K)	J:34 Pin SOJ T:34 Pin TSOP-II (Forward) R:34 Pin TSOP-II(Reverse)

1

2.2 Dynamic RAM Module

Org.	Part No.	Feature	Speed(ns)	Package	PCB Height	Refresh cycle/ms	C/S
DRAM SIMM Based on 4M DRAM							
1Mx8	KMM581000CN	F/P	60/70/80	S, 30 Pin SIMM	650	1024/16	NOW
1Mx9	KMM591000CN	F/P	60/70/80	S, 30 Pin SIMM	650	1024/16	NOW
4Mx8	KMM584000C	F/P	60/70/80	S, 72 Pin SIMM	805	1024/16	NOW
4Mx9	KMM594000C	F/P	60/70/80	S, 72 Pin SIMM	805	1024/16	NOW
1Mx32	KMM5321000CV/CVG	F/P	50/60/70/80	S, 72 Pin SIMM	855	1024/16	NOW
1Mx33	KMM5331000C/CG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361000C2/C2G	F/P, PLCC	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361000CH	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx36	KMM5361003C/CG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
1Mx40	KMM5401000C/CG/CM	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322000CV/CVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362000C2/C2G	F/P, PLCC	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362000CH	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362003C/CG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx40	KMM5402000C/CG/CM	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
4Mx32	KMM5324000CV/CVG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
4Mx33	KMM5334000CV/CVG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
4Mx36	KMM5364000C/CG	Double Nocth	50/60/70/80	D, 72 Pin SIMM	1290	1024/16	NOW
DRAM SIMM Based on 4M B/W DRAM							
256Kx32	KMM532256BW/BWG	F/P	60/70/80	S, 72 Pin SIMM	1000	512/8	NOW
256Kx36	KMM536256BW/BWG	F/P	60/70/80	S, 72 Pin SIMM	1000	512/8	NOW
512Kx32	KMM532512BW/BWG	F/P	60/70/80	D, 72 Pin SIMM	1000	512/8	NOW
512Kx36	KMM536512BW/BWG	F/P	60/70/80	D, 72 Pin SIMM	1000	512/8	NOW
DRAM SIMM Based on 16M DRAM							
4Mx8	KMM584100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	NOW
4Mx8	KMM584100AKN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	'94, 4Q
4Mx9	KMM594100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	NOW
4Mx9	KMM594100AN	F/P	50/60/70/80	S, 30 Pin SIMM	650	2048/32	'94, 4Q
16Mx8	KMM5816000A/AT	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	NOW
16Mx8	KMM5816000AK	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	'94, 4Q
16Mx9	KMM5916000A/AT	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	NOW
16Mx9	KMM5916000AK	F/P	50/60/70/80	D, 30 Pin SIMM	900	4096/64	'94, 4Q
4Mx32	KMM5324100AV/AVG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx32	KMM5324000AV/AVG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx32	KMM5324100AK/AKG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx32	KMM5324000AK/AKG	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx33	KMM5334100A/AG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW

2.2 Dynamic RAM Module (Continued)

Org.	Part No.	Feature	Speed(ns)	Package	PCB Height	Refresh cycle/ms	C/S
DRAM SIMM Based on 16M DRAM							
4Mx36	KMM5364100A/AG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364100A1/A1G	F/P	50/60/70/80	S, 72 Pin SIMM	1250	2048/32	NOW
4Mx36	KMM5364100AH/AHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364000AH/AHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx36	KMM5364100AKH/AKHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	'94, 4Q
4Mx36	KMM5364000AKH/AKHG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	'94, 4Q
4Mx36	KMM5364103AK/AKG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx36	KMM5364003AK/AKG	F/P, QCAS	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx39	KMM5394100AM	F/P	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx39	KMM5394000AM	F/P	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx40	KMM5404100A/AG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	NOW
4Mx40	KMM5404000A/AG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	NOW
4Mx40	KMM5404100AK/AKG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	2048/32	'94, 4Q
4Mx40	KMM5404000AK/AKG	F/P, ECC	50/60/70/80	S, 72 Pin SIMM	1000	4096/64	'94, 4Q
8Mx32	KMM5328100AV/AVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx32	KMM5328000AV/AVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx32	KMM5328100AK/AKG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx32	KMM5328000AK/AKG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx33	KMM5338100AKV/AKVG	F/P	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx36	KMM5368100A1/A1G	F/P	50/60/70/80	D, 72 Pin SIMM	1375	2048/32	NOW
8Mx36	KMM5368100AH/AHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1250	2048/32	NOW
8Mx36	KMM5368000AH/AHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1250	4096/64	NOW
8Mx36	KMM5368100AKH/AKHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	'94, 4Q
8Mx36	KMM5368000AKH/AKHG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	'94, 4Q
8Mx36	KMM5368103AK/AKG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
8Mx36	KMM5368003AK/AKG	F/P, QCAS	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
8Mx40	KMM5408100AK/AKG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	2048/32	'94, 4Q
8Mx40	KMM5408000AK/AKG	F/P, ECC	50/60/70/80	D, 72 Pin SIMM	1000	4096/64	'94, 4Q
DRAM SIMM Based on 16M B/W DRAM							
1Mx32	KMM5321200AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
1Mx32	KMM5321000AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
1Mx32	KMM5321203AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322200AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	1024/16	NOW
2Mx32	KMM5322000AW/AWG	F/P	60/70/80	D, 72 Pin SIMM	1000	4096/64	NOW
2Mx32	KMM5322103AU/AUG	F/P, QCAS	60/70/80	D, 72 Pin SIMM	1000	2048/32	NOW
2Mx32	KMM5322208AU/AUG	F/P, AND	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW
2Mx36	KMM5362209AU/AUG	F/P, AND	60/70/80	S, 72 Pin SIMM	1000	1024/16	NOW



2.3 Video RAM

Capacity	Part Number	Orgnization	Speed(ns)	Technology	Features	Package	Remark
256K	KM424C64	64K × 4	100/120	CMOS	M/F	24Pin DIP/ZIP	NOW
512K	KM428C64	64K × 8	70/80/100	CMOS	M/F	40PIN SOJ	NOW
1M	KM424C256A	256K × 4	60/70/80	CMOS	M/F	28Pin ZIP/SOJ	NOW
	KM424C257	256K × 4	60/70/80	CMOS	E/F	28Pin ZIP/SOJ	NOW
	KM428C128	128K × 8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP- II	NOW
2M	KM428C256	256K × 8	60/70/80	CMOS	E/F	40Pin SOJ/TSOP- II	NOW
	KM428V256	256K × 8	70/80	CMOS	E/F(3.3V)	40Pin SOJ/TSOP- II	NOW
	KM428C257	256K × 8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP- II	NOW
	KM428C258	256K × 8	60/70/80	CMOS	F/F	40Pin SOJ/TSOP- II	NOW
4M	† KM4216C256	256K × 16	60/70/80	CMOS	F/F	64Pin SSOP/TSOP- II	2Q '94

* : New Product † : Under Development

2.4 Static RAM

Low power SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μ A)	
64K	KM6264BL/BL-L	8K x 8	70/100/120	CMOS	55	100/50	DIP/SDIP/SOP
256K	KM62256BL/BL-L	32K x 8	70/85/100/120	CMOS	70	100/20	DIP/SDIP/SOP/TSOP
	KM62256BLI/BLI-L	32K x 8	70/100	CMOS	70	100/20	DIP/SOP
	* KM62256CL/CL-L	32K x 8	55/70/85/100	CMOS	70	100/20	DIP/SDIP/SOP/TSOP
	* KM62256CLI/CLI-L	32K x 8	70/100	CMOS	70	100/20	SOP/TSOP
512K	KM68512L/L-L	64K x 8	70/85/100	CMOS	70	100/20	SOP/TSOP
	* KM68512AL/AL-L	64K x 8	55/70	CMOS	70	100/20	SOP/TSOP
1M	* KM681000BL/BL-L	128K x 8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP
	* KM681000BLI/BLI-L	128K x 8	70/100	CMOS	70	100/20	SOP/TSOP
4M	* KM684000L/L-L	512K x 8	55/70/85/100	CMOS	70	100/20	DIP/SOP/TSOP
	* KM684000LI/LI-L	512K x 8	70/85/100	CMOS	70	100/50	SOP/TSOP

Low Voltage SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μ A)	
256K	† KM62256CL-LV	32K x 8	70	CMOS	40	20/10	SOP/TSOP
1M	† KM68V1000BL/BL-L	128K x 8	70/100	CMOS	40	50/10	SOP/TSOP
4M	†† KM68V4000AL/AL-L	512K x 8	70/100/120	CMOS	70	50/10	SOP/TSOP
	†† KM616V4000AL/AL-L	256K x 16	70/100	CMOS	70	50/10	SOP/TSOP

Low Voltage SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μ A)	
1M	KM658128A/AL/AL-L	128K x 8	80/100/120	CMOS	70	100/20	DIP/SOP

* : New Product † : Preliminary Product †† : Under Development Δ : Last Time by Product

High speed & Ultra High Speed SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μ A)	
64K	KM6465B	16K x 4	12/15/20/25	CMOS	140	1	22 SDIP
	KM6466B	16K x 4	12/15/20/25	CMOS	140	1	24 SDIP/SOJ
	KM6865B	8K x 8	12/15/20/25	CMOS	140	1	28 SDIP/SOJ
256K	Δ KM64258B	64K x 4	15/20/25	CMOS	140	2	28 SDIP/SOJ
	KM64258C	64K x 4	12/15/20	CMOS	140	2	28 SOJ
	KM64V258C	64K x 4	15/17/20	CMOS	110	2	28 DIP/SOJ
	* KM64B261A	64K x 4	6/7/8	BICMOS	160	20	28 SOJ
	* KM64B258A	64K x 4	8/10/12	BICMOS	185	20	28 SOJ
	Δ KM68257B	32K x 8	15/20/25	CMOS	150	2	28 DIP/SOJ
	KM68257C	32K x 8	12/15/20	CMOS	150	2	28 DIP/SOJ
	KM68V257C	32K x 8	15/17/20	CMOS	110	2	28 DIP/SOJ
	* KM68B261A	32K x 8	6/7/8	CMOS	170	20	32 SOJ
	* KM68B257A	32K x 8	8/10/12	CMOS	185	20	28 SOJ
	Δ KM68V257	32K x 8	20/25/35	CMOS	90	0.1	28 DIP/SOJ
1M	Δ KM611001	1M x 1	20/25/35	CMOS	130	2	28 DIP/SOJ
	KM641001	256K x 4	17/20/25/35	CMOS	150	2	28 SDIP/SOJ
	KM641003	256K x 4	15/17/20	CMOS	170	10	32 SOJ
	\ddagger KM641003A	256K x 4	12/15/17/20	CMOS	185	3/0.2	32 SOJ/TSOP(II)
	\ddagger KM64V1003A	256K x 4	12/15/17/20	CMOS	95	2/0.1	32 SOJ/TSOP(II)
	* KM64B1003	256K x 4	8/10/12/15	BICMOS	165	10	32 SOJ
	KM681001	128K x 8	20/25/35	CMOS	170	2	32 SDIP/SOJ
	KM681002	128K x 8	15/17/20	CMOS	170	10	32 SOJ/TSOP(II)
	\ddagger KM681002A	128K x 8	12/15/17/20	CMOS	185	3/0.2	32 SOJ/TSOP(II)
	\ddagger KM68V1002A	128K x 8	12/15/17/20	CMOS	95	2/0.1	32 SOJ/TSOP(II)
	* KM68B1002	128K x 8	8/9/10/12/15	BICMOS	175	10	32 SOJ/TSOP(II)
	KM6161002	64K x 16	15/17/20	CMOS	230	10	44 SOJ/TSOP(II)
	\ddagger KM6161002A	64K x 16	12/15/20	CMOS	250	3/0.2	44 SOJ/TSOP(II)
	\ddagger KM616V1002A	64K x 16	13/15/17/20	CMOS	170	2/0.1	44 SOJ/TSOP(II)
4M	KM644002/L	1M x 4	17/20/25	CMOS	170	10/0.5	32 SOJ
	\dagger KM68B4002	1M x 4	10/12/15	BICMOS	180	60/30	32 SOJ
	\ddagger KM68BV4002	1M x 4	12/15/20	BICMOS	170	60/30	32 SOJ
	KM684002/L	512k x 8	17/20/25	CMOS	160	10/0.5	36 SOJ
	\dagger KM68B4002	512K x 8	10/12/15	BICMOS	200	60/30	36 SOJ
	\ddagger KM68BV4002	512K x 8	12/15/20	BICMOS	180	60/30	36 SOJ
	KM6164002/L	256K x 16	20/25/35	CMOS	160	10/0.5	44 SOJ
	\dagger KM616B4002	256K x 16	10/12/15	BICMOS	240	60/30	44 SOJ/54 SOJ
	\ddagger KM616BV4002	256K x 16	12/15/20	BICMOS	200	60/30	44 SOJ/54 SOJ

* : New Product \dagger : Preliminary Product \ddagger : Under Development Δ : Last Time by Product

Specialty SRAM

Den.	Part Name	Org.	Speed(ns)	Technology	Power Dissipation		Package
					Active Max.(mA)	Standby Max.(μ A)	
288K	Δ KM79C86	32K x 9	14/19/24	CMOS	190	50	44 PLCC
1M	KM741006	256K x 4	6.5/7/8	CMOS	190	40	46 SOJ
	\dagger KM718B86	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	\dagger KM718B91	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	\dagger KM718BV87	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC
	\dagger KM718BV91	64K x 18	9/10/12	BiCMOS	280	80	52 PLCC

* : New Product \dagger : Preliminary Product \ddagger : Under Development Δ : Last Time by Product

1

2.5. MASK ROM

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
256K	KM23C256(G)	32K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	NOW
512K	KM23C512(G)	64K x 8	120/150/200	CMOS	Programmable CE & OE	28DIP(32SOP)	NOW
1M	KM23C1000	128K x 8	120/150/200	CMOS	Programmable CE	28DIP	NOW
	KM23C1001	128K x 8	120/150/200	CMOS	Programmable OE	28DIP	NOW
	KM23C1010(G)	128K x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C1011(G)	128K x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	NOW
2M	KM23C2000A(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C2001A(G)	256K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C2100A	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	NOW NOW
	† KM23C2000B(G)	256K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	4Q.'94
	† KM23C2001B(G)	256K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	4Q.'94
	† KM23C2100B	256K x 8/ 128K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	4Q.'94
4M	KM23C4000B(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C4001B(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C4100B(G)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(40SOP)	NOW
	KM23C4200B	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	NOW
	† KM23C4000C(G)	512K x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	4Q.'94
	† KM23C4001C(G)	512K x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	4Q.'94
	† KM23C4100C(G)	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP(40SOP)	4Q.'94
	† KM23C4200C	512K x 8/ 256K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	40DIP	4Q.'94
	* KM23V4000B(G)	512K x 8	150/200/250	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V4001B(G)	512K x 8	150/200/250	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V4100B(G)	512K x 8/ 256K x 16	150/200/250	CMOS	3.3V Operation	40DIP(40SOP)	NOW
8M	KM23C8000B(G)	1M x 8	100/120/150	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	KM23C8001B(G)	1M x 8	100/120/150	CMOS	Programmable OE	32DIP(32SOP)	NOW
	KM23C8100B(G)	1M x 8/ 512K x 16	100/120/150	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	* KM23C8000C(G)	1M x 8	120/150/200	CMOS	Programmable CE & OE	32DIP(32SOP)	NOW
	* KM23C8001C(G)	1M x 8	120/150/200	CMOS	Programmable OE	32DIP(32SOP)	NOW
	* KM23C8100C(G)	1M x 8/ 512K x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode	42DIP(44SOP)	NOW
	KM23C8105B(G)	1M x 8/ 512K x 16	100/120/150 (tP>50)	CMOS	4Word Page	42DIP(44SOP)	NOW
	* KM23V8000B(G)	1M x 8	200/250/300	CMOS	3.3V Operation	32DIP(32SOP)	NOW
	* KM23V8001B(G)	1M x 8	200/250/300	CMOS	3.3V Operation	32DIP(32SOP)	NOW
		* KM23V8100B(G)	1M x 8/ 512K x 16	200/250/300	CMOS	3.3V Operation	42DIP(44SOP)

MASK ROM (Continued)

Capacity	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
16M	KM23C16101A	2M x 8	120/150/200	CMOS	Programmable OE Programmable CE & OE Word/Byte Mode	36DIP	NOW
	KM23C16000A(G)	2M x 8/ 1M x 16	120/150/200	CMOS		42DIP(44SOP)	NOW
	* KM23C16101B	2M x 8	120/150/200	CMOS	Programmable OE Programmable CE & OE Word/Byte Mode	36DIP	NOW
	* KM23C16000B(G)	2M x 8/ 1M x 16	120/150/200	CMOS		42DIP(44SOP)	NOW
	KM23C16005A(G)	2M x 8/ 1M x 16	120/150/200 (tP > 50)	CMOS	8Word Page	42DIP(44SOP)	NOW
* KM23V16101A	2M x 8	200/250/300	CMOS	3.3V Operation	36DIP	NOW	
* KM23V16000A(G)	2M x 8/ 1M x 16	200/250/300	CMOS	3.3V Operation	42DIP(44SOP)	NOW	
32M	KM23C32110	4M x 8	150/200/250	CMOS	Programmable CE & OE Programmable CE & OE Programmable CE & OE	42DIP	NOW
	KM23C32000	2M x 16	150/200/250	CMOS		42DIP(44SOP)	NOW
	KM23C32000G	4M x 8/ 2M x 16	150/200/250	CMOS		42DIP(44SOP)	NOW
	† KM23C32101A	4M x 8	120/150/200	CMOS	Programmable OE Programmable CE & OE Programmable CE & OE Programmable CE & OE Word/Byte Mode	36DIP	4Q.'94
	† KM23C32110A	4M x 8	120/150/200	CMOS		42DIP	4Q.'94
	† KM23C32000A	2M x 16	120/150/200	CMOS		42DIP	4Q.'94
	† KM23C32000AG	4M x 8/ 2M x 16	120/150/200	CMOS		44SOP	4Q.'94
	KM23C32005	2M x 16	150/200/250	CMOS	8Word Page	42DIP	NOW
	KM23C32005G	4M x 8/ 2M x 16	150/200/250	CMOS	8word Page	44SOP	NOW
† KM23C32005AG	4M x 8/ 2M x 16	100/120/150 (tP > 30)	CMOS	8Word Page	44SOP	1Q.'95	
† KM23C32205ASG	2M x 16 1M x 32	100/120/150 (tP > 30)	CMOS	8word Page	70SSOP	2Q.'95	
64M	† KM23C64000G	8M x 8/ 4M x 16	120/150/200	CMOS	Programmable CE & OE Word/Byte Mode Programmable CE & OE	44SOP	3Q.'95
	KM23C64200SG	4M x 16/ 2M x 32	120/150/200	CMOS		70SSOP	3Q.'95

* : New Product

† : Under Development

2.6 EEPROM/FLASH

Density	Part Number	Organization	Speed(ns)	Technology	Features	Package	Remark
1K bit	KM93C46/G/GD/I	64 × 16	1MHz	CMOS	Self-timed	8DIP/8SOP	Now
	KM93C46V/VG/VGD/I	64 × 16	250KHz	CMOS	3.0V-Operation	8DIP/8SOP	Now
2K bit	KM93C56/G/GD/I	128 × 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93C57/G/GD/I	128 × 16/256 × 8	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q,94
	KM93C56V/VG/VGD/I	128 × 16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
	KM93C57V/VG/VGD/I	128 × 16/256 × 8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
4K bit	KM93C66/G/GD/I	256 × 16	1MHz	CMOS	Auto Erase, Self-timed	8DIP/8SOP	Now
	KM93C67/G/GD/I	256 × 16/512 × 8	1MHz	CMOS	Select Organization	8DIP/8SOP	3Q,94
	KM93C66V/VG/VGD/I	256 × 16	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
	KM93C67V/VG/VGD/I	256 × 16/512 × 8	1MHz	CMOS	3.0V Operation	8DIP/8SOP	Now
64K bit	KM28C64A/AJ	8K × 8	120/150/200	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	Now
	KM28C64A/AJI	8K × 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C65A/AJ	8K × 8	120/150/200	CMOS	64B Page Mode, D-P, T-B R-B	28DIP/32PLCC	Now
	KM28C65A/AJI	8K × 8	120/150/200	CMOS	Industrial	28DIP/32PLCC	Now
	KM28C64B/BJ	8K × 8	90/120/150	CMOS	64B Page Mode, D-P, T-B	28DIP/32PLCC	3Q,94
	KM28C64B/BJI	8K × 8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q,94
	KM28C65B/BJ	8K × 8	90/120/150	CMOS	64B Page Mode, D-P, T-B, R-B	28DIP/32PLCC	3Q,94
	KM28C65B/BJI	8K × 8	90/120/150	CMOS	Industrial	28DIP/32PLCC	3Q,94
1M bit	KM29C010/J/T	128K × 8	100/120/150	CMOS	128B Page Mode, D-P, T-B	32DIP/32PLCC	Now
16M bit	KM29N16000T/TS	2M × 8	tr = 15 μs	CMOS	256B Page Mode	44(40)TSOP	3Q,94
	KM29N16000R/RS		trc = 80ns		4K Block Erase		
32M bit	KM29N32000T/TS	4M × 8	tr = 10 μs	CMOS	512B Page Mode	44(40)TSOP	2Q,94
	KM29N32000R/RS		trc = 50ns		8K Block Erase		

* D-P : Data-Polling, R/B : Ready/Busy, T-B : Toggle Bit

2.7 DRAM Card

Card Style	Vcc	Density	Part No.	Organization	Speed(ns)	PKG	Features
JEIDA/JEDEC	5.0V	2M Byte	KMCJ532512	512Kx32/1Mx16	60/70/80	88 Pin Two Piece	<ul style="list-style-type: none"> • Fast Page Mode Operation • Low Power Consumption • $\overline{\text{RAS}}$ only and Hidden Refresh • $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
			KMCJ536512	512Kx36/1Mx18	60/70/80	88 Pin Two Piece	
		4M Byte	KMCJ5321000	1Mx32/2Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5361000	1Mx36/2Mx18	60/70/80	88 Pin Two Piece	
		8M Byte	KMCJ5322000	2Mx32/4Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5362000	2Mx36/4Mx18	60/70/80	88 Pin Two Piece	
		16M Byte	KMCJ5324000	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5324100	4Mx32/8Mx16	60/70/80	88 Pin Two Piece	
			KMCJ5364100	4Mx36/8Mx18	60/70/80	88 Pin Two Piece	
		3.3V	2M Byte	KMCV532512	512Kx32/1Mx16	60/70/80	
	KMCV5321000			1Mx32/2Mx16	60/70/80	88 Pin Two Piece	
	KMCV5322000			2Mx32/4Mx16	60/70/80	88 Pin Two Piece	
	16M Byte			KMCV5324000	4Mx32/8Mx16	60/70/80	
		KMCV5324100	4Mx32/8Mx16	60/70/80	88 Pin Two Piece		

SRAM Card

Card Style	Vcc	Capacity	Part No.	Organization	Speed(ns)	PKG	Features
PCMCIA/JEIDA Standard	5.0V	512K Byte	KMCJ616256	256Kx16/512Kx8	150/200/250	68 Pin Two Piece	• 8KByte Attribute Memory
		1M Byte	KMCJ616512	512Kx16/1Mx8	150/200/250	68 Pin Two Piece	• Replaceable & Rechargeable Battery
		2M Byte	KMCJ6161000	1Mx16/2Mx8	150/200/250	68 Pin Two Piece	• High Speed : 150ns

3. CROSS REFERENCE GUIDE

3.1 Video RAM

Density	Feature	Organization	Samsung	Micron	Toshiba	NEC	Hitachi	Ti
256K	Minimum	64K×4	KM424C64	MT42C4064		μPD41264 μPD42264	HM53461(2)	TMS4461
512K	Minimum	64K×8	KM428C64					
1M	Minimum	256K×4	KM424C256 KM424C256A		TC524256 TC524256A TC524256B TC524257	μPD42273	HM534251 HM534251A HM534252	TMS44C250 SMJ44C250
		128K×8			TC528126A TC528126B		HM538121 HM538121A	TMS48C121
	Extended	256K×4	KM424C257	MT42C4256 MT42C4255	TC524258A TC524258B TC524259B	μPD42274	HM534253A	TMS44C251 SMJ44C251 SMJ44C251A
		128K×8	KM428C128	MT42C8128 MT42C8128	TC528128A TC528128B TC528129B	μPD42275	HM538123A	
2M	Extended	256K×8	KM428C256	MT42C8255				
	Full	256K×8	KM428C257 KM428C258	MT42C8256 MT42C8254	TC528267	μPD482234 μPD482235	HM538253	
4M	Full	256K×32	KM4216C256	MT42C256K16A1				

3.2 Static RAM

Low power SRAM

Den.	Org.	SAMSUNG	HITACHI	SONY	TOSHIBA	MITSUBISHI	NEC
64K	8K x 8	KM6264BL/BL-L	HM6264A/AL/AL-L	CXK5864B-L/B-LL	TC6565AL/AL-L	M5M5165/L	μ PD4364L/L-L
256K	32K x 8	KM62256CL/CL-L	HM62256AL/AL-L	CXK58257A-L/A-LL	TC55257BL/BL-L	M5M5255B-L/B-LL	μ PD43256B/BL
512K	64K x 8	KM68512AL/AL-L					
1M	128K x 8	KM681000BL/BL-L	HM628128AL/AL-L	CXK581000/L	TC551001AL-AL-L	M5M51008/L	μ PD431000AL/ALL
4M	512K x 8	KM628512	HM628512/L/L-L	CXK584000(1)-L	TC554002	M5M54008/LL	μ PD434000/L/LL

Low power SRAM

Den.	Org.	SAMSUNG	HITACHI	TSOHIBA	NEC	OKI	MOTOROLA
1M	128K x 8	KM658128A/AL/AL-L	HM658128A/AL/AL-L	TC518129A/AL/AL-L	μ PD428128A/AL/AL-L	MSM548128	MCM518128

High Speed SRAM

Den.	Org.	Samsung	Hitachi	Cypress	Fujitsu	Micron	IDT	Motorola	Toshiba	sony
64K	16K x 4	KM6465B	HM6288	CY7C164A	MB81C74	MT5C6404	IDT7188	MCM6288C	TC55416	CXK5466
	16Kx4(With OE)	KM6466B	HM6289	CY7C166A	MB81C75	MT5C6405	IDT6198		TC55417	CXK5465
	8K X 8	KM6865B		CY7C186A	MB81C78	MT5C6408	IDT7164	MCM6264C	TC5588	CXK5863
256K	64K X 4(5V)	KM64458C	HM67909A	CY7C196	MB81C84A	MT5C2565	IDT61298SA	MCM629C	TC55464A	
	64K X 4(3.3V)	KM64B258C				MT5LC2565				
	32K X 8(5V)	KM68257C	HM62832H	CY7C199		MT5C2568	IDT71256SA	MCM6206D	TC55328A	CXK58258B
	32K x 8(3.3V)	KM68V257C				MT5LC2568	IDT713256	MCM62V06D	TC55V328	
1M	1M x 1(E)	KM11001		CY7C1007		MT5C1001	IDT71281	MCM6227B		
	256K x 4(E)	KM641001	HM624256A	CY7C1006		MT5C1005	IDT71028	MCM6229A		CXK541000
	256K x 4(F)	KM641003	HM674256UH			MT5C256K4A1				
	128K x 8(E)	KM681001	HM6268127H	CY7C1009	MB82008	MT5C1008	IDT71024	MCM6226B		CXK541020
	128K x 8(F)	KM681002				MT5C128K8A1				
	64K x 16(F)	KM6161002		CY7C108		MT5C64K16A1			TC551664	
4M	1M x 4	KM644002	HM624100		MB82201	MT5C1M4B2			TC551402	
	512K x 8	KM684002				MT5C512K8B2				
	256K x 16	KM6164002				MT5C256KX16				

BICMOS SRAM

Den.	Org.	Samsung	Hitachi	NEC	Toshiba	Motorola	IDT
256K	64K x 4(With OE)-R	KM64B261A				MCM6709R	
	64K x 4(with-OE)-E	KM64B258A	HM6709SH		TC55B465	MCM6709A	IDT61B298
	32K x 8-R	KM68B261A		μ PD46258		MCM6706R	
	32K x 8-E	KM68B257A	HM6783SH		TC55B328	MCM6706A	IDT71256
1M	256K x 4(With OE)-R	KM64B1003			TC55B4257	MCM6729A	
	128K x 8-R	KM68B1002			TC55B8128	MCM6726A	IDT71B024

Specialty SRAM

Den.	Org.	SMAMSUNG	Motorola	Micron	Cypress	ICW
1M	256K x 4	KM741006	MCM67Q804			
	64K x 18	KM718B86	MCM67B618		CY7C1031	ICW73B596
		KM718B90		MT58LC64K18M1		
		KM718BV87	MCM67H618	MT58LC64K18B2		
		KM718BV90		MT58LC64K18M1		

3.3 MASK ROM

DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
256K	KM23C256		HN623257P HN623258P		LH23255 LH53259	M5M23256P	MB83256	CXK38256
512K	KM23C512			TC53512C	LH53514 LH53515		MB83512	
1M	KM23C1000	uPD23C1000A	HN62321P HN62321BP HN62331P	TC531000C	LH231000B LH531000A	M5M23C100 M5M231000	MB831000 MB831124	CXK381000P
	KM23C1001	uPD23C1010A	HN62321EP HN62331EP			M5M231001		
	KM23C1010	uPD23C1001E uPD23C1000E	HN62321A HN62331A	TC531001C	LH231100B LH530800 LH530900			
	KM23C1011	uPD23C100EA						
2M	KM23C2000A	uPD23C2001	HN62302B	TC532000A	LH532300 LH532100B LH532200B LH532400		MB832000 MB832001	CXK382001
	KM23C2001A				LH532000B LH532500			
	KM23C2100A	uPD23C2000 uPD23C2000A	HN62412P HN62422P					
4M	KM23C4000B	uPD23C4001E	HN62335 HN62344B HN62335 HN62344B HN62W335B	TC534000A	LH534100B	M5M23C401AP	MB834000A	CXK384001
	KM23C4000C				LH534300 LH534400 LH534300 LH534400		MB834000AL	
	KM23V4001B KM23C4001B							
	KM23C4001C							
	KM23C4100B	uPD23C4000 uPD23C4000A	HN62404P HN62414P HN62424P HN62444P	TC534200	LH534000B LH534500'	M5M23C400AP	MB834100A MB834200A	
	KM23C4100C	uPD23C4000 uPD23C4000A	HN62404P HN62414P HN62424P HN62444P HNW15		LH534000B LH534500		MB834100AL	
	KM23V4100B KM23C4200B KM23C4200C							

1

3.3 MASK ROM (Continued)

DTY	Samsung	NEC	Hitachi	Toshiba	Sharp	Mitsubishi	Fujitsu	Sony
8M	KM23C8000B	uPD23C8001E	HN62318B	TC538000A	LH538100 LH538200	M5M23801P	MB838000	CXK388000
	KM23C8000C	uPD23C8001E	HN62318B		LH538100 LH538200	M5M23801P	MB838000	
	KM23V8000B		HN62W328B					
	KM23C8001B							
	KM23C8001C							
	KM23V8001B							
	KM23C8100B	uPD23C8000	HN62418P	TC538200A	LH538000	M5M23800P	MB838200	
	KM23C8100C	uPD23C8000	HN62428P	TC538200A	LH538000	M5M23800P		
	KM23C8105B						MB838200L	
	KM23V8100B							
16M	KM23C16101A							
	KM23C16101B							
	KM23V16101A							
	KM23C16000A	uPD23C16000	HN624316P	TC5316200A	LH53160000	M5M23160P	MB831620P	
	KM23C16000B	uPD23C16000	HN624316P	TC5316200A	LH53160000	M5M23160P	MB831620P	
	KM23C16005A					M5M23168P		
	KM23V16000A		HN62W4116					
32M	KM23C32000	uPD23C32000			LH5332000			
	KM23C32000A	uPD23C32000			LH5332000			
	KM23C32005							
	KM23C32005A							
	KM23C32205A							

3.4 EEPROM

*Serial I/O EEPROM

Density	Samsung	N. S	Exar	Micro Chip	SGSThompson	Catalyat	Rohm	Atmel
1K	KM93C46	NM9346	XRM93C46A	93C46	ST93C46T	CAT93C46A	BR93C46	AT93C46
	KM93C46V	NM93C46L						
2K	KM93C56	NM93C56A	XRM93C56A				BR93C56A	AT93C56
	KM93C57			93C56	ST93C56	CAT36C102		
	KM93C56V	NM93C56L					BR93C56B	
	KM93C57V							
4K	KM93C66	NM93C66	XRM93C66B				BR93C66A	AT93C66
	KM93C67			93C66		CAT35C104		
	KM93C66V	NM93C66L					BR93C66B	
	KM93C67V					CAT33T104		

*Parallel EEPROM

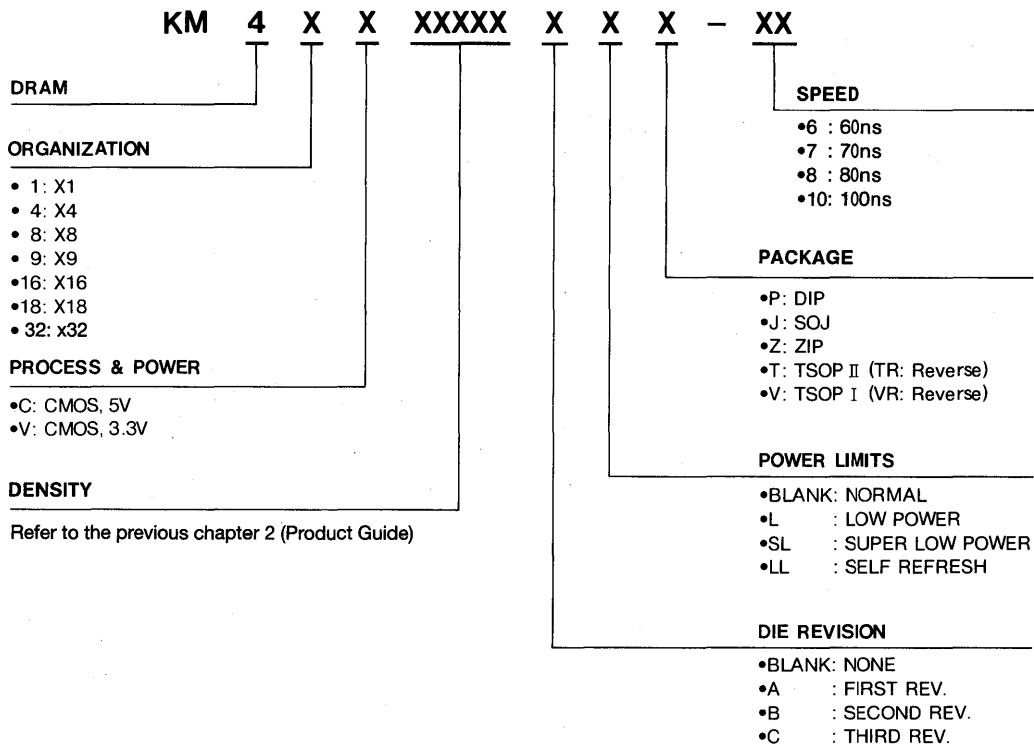
Density	Samsung	Xicor	Seeq	Exel	Atmel	Hitachi	Oki	Catalyat
64K	KM28C64A	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65A		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A
	KM28C64B	X2864A/B X28C64	DQ28C64	XL2864 XL28C64A	AT28C64	HN58064	MSM28C64A	CAT28C65A
	KM28C65B		DQ28C65 DQ2864	XL2865 XL28C65A		HN58C65/66		CAT28C65A

3.5 Flash

Density	Samsung	Toshiba	Seeq	Exel	Atmel	Hitachi	Oki	Catalyat
1M	KM29C010				AT29C010			
16M	KM29N16000	TC5816FT/TR						
32M	KM29N32000	TC5832FT/TR						

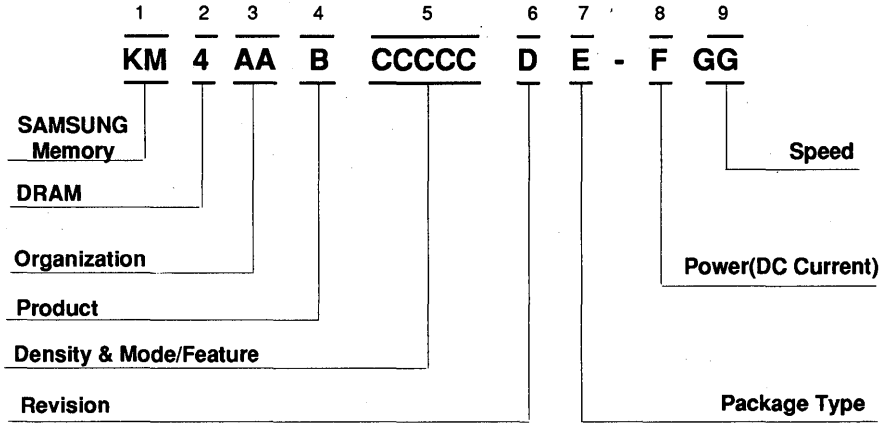
4. ORDERING INFORMATION

4.1 DRAM



*** NEW DRAM ORDERING SYSTEM**

This new DRAM ordering system will be used for all SAMSUNG's DRAM products in '95. In '94 DRAM Databook, only used for 16M Byte Word Wide 2nd Gen. and 64M DRAM.



1. SAMSUNG Memory

2. DRAM(4)

3. Organization

- 1 ----- x 1
- 4 ----- x 4
- 8 ----- x 8
- 9 ----- x 9
- 16 ----- x 16
- 18 ----- x 18
- 32 ----- x 32

4. Product

- C ----- 5V
- V ----- 3.3V

5. Density & Mode/Feature (Same)

6. Revision

- Blank ----- 1st Gen.
- A ----- 2nd Gen.
- B ----- 3rd Gen.
- C ----- 4th Gen.

7. Package Type

- J ----- SOJ
- T ----- TSOP II (Forward)
- R ----- TSOP II (Reverse)
- V ----- TSOP I (Forward)
- U ----- TSOP I (Reverse)
- K ----- SOJ(Shrunked PKG,SOJ)
- S ----- TSOP II (Shrunked PKG,Forward)
- W ----- TSOP II (Shrunked PKG,Reverse)

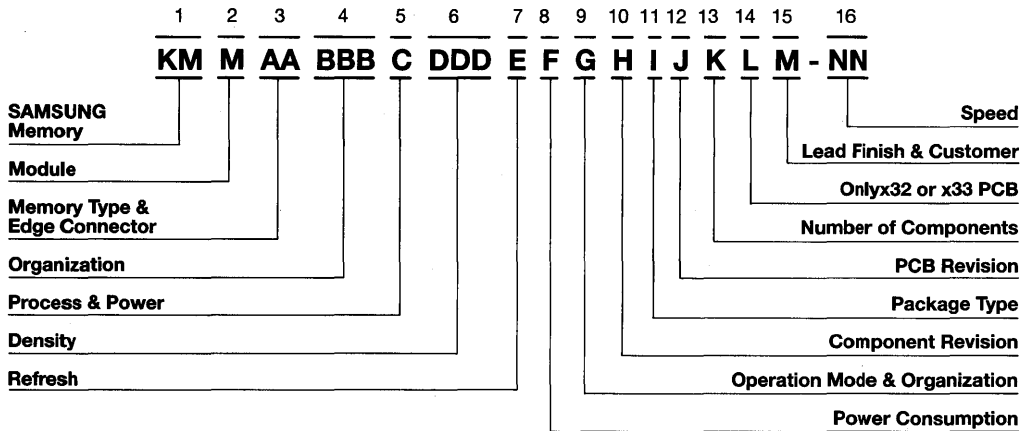
8. Power(DC Current)

- Blank ----- Normal
- L ----- Low power
- H ----- Super Low power
- F ----- Self Refresh with L.P

9. Speed

- 5 ----- 50 ns
- 6 ----- 60 ns
- 7 ----- 70 ns
- 8 ----- 80 ns

4.2 DRAM Module



1. SAMSUNG Memory

2. Module

3. Memory Type & Edge Connector

- 1 FLASH
- 2 Mask ROM
- 3 DRAM DIMM
- 4 DRAM SIP
- 5 DRAM SIMM
- 6 SRAM
- 7 Pseudo SRAM
- 8 ASSP
- 9 VRAM

4. Organization

- 8/9 x8/x9 bit wide
- 18 x18 bit wide
- 32/33 x32/x33
- 36/40 x36/x39/x40
- 64/66 x64/x66
- 72/80 x72/x80
- 144 x144 bit wide

5. Process & Operation Voltage

- Blank CMOS 5V
- V CMOS 3.3V
- S Sync 3.3V

6. Density

- 16 16M
- 8 8M
- 4 4M
- 2 2M
- 1 2M
- 512 512K
- 256 256K

7. Refresh (16M DRAM Based)

- 0 4K
- 1 2K
- 2 1K

8. Power Consumption

- 0 Normal
- 2 Low Power
- 4 Super Low Power
- 6 Self Refresh

9. Operation Mode & Organization

- 0 F/P
- 1 Nibble
- 2 Static Column
- 3 Using Quad CAS
- 4 Using EDO
- 5 Using EDO & Quad CAS
- 8 Using Non Memory Logic
- 9 Using Non Memory Logic & Quad CAS

10. Component Revision

- Blank None
- A First Rev.
- B Second Rev.
- C Third Rev.

11. Package Type

- Blank SOJ or PLCC
- T TSOP

12. PCB Revision

- Blank None
- 1 First Rev.
- 2 Second Rev.
- 3 Third Rev.

13. Number of Components

- Blank more than 7 chip
- N less than 8 chip
- U Byte Wide Base
- W Word Wide Base

14. Only x32 or x33 PCB

- V x32 or x33 PCB

15. Lead Finish & Customer

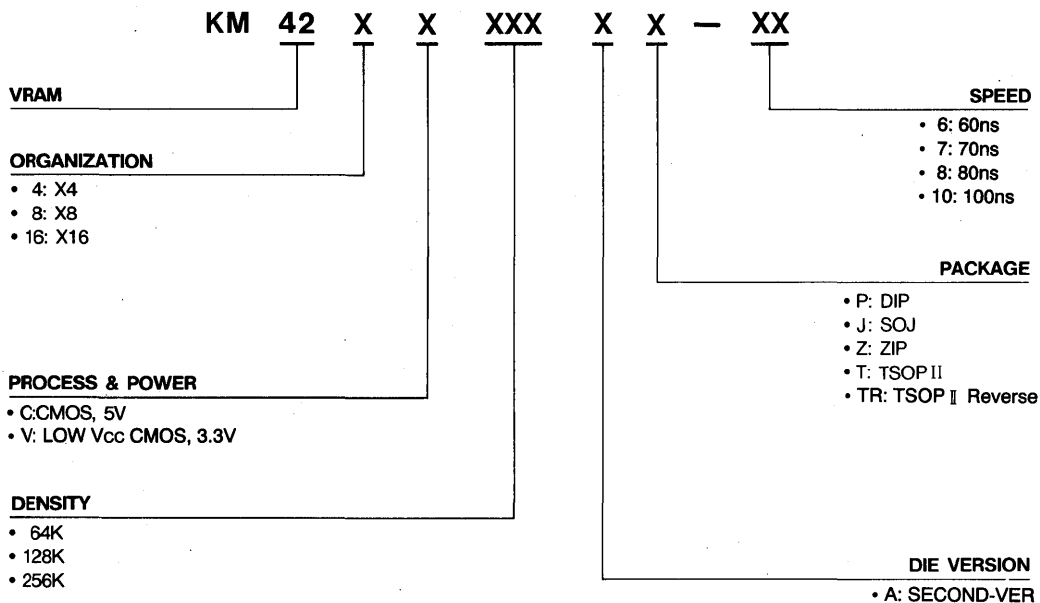
- Blank Solder
- G Gold
- D DEC
- H HP
- M IBM
- P Nickel
- Q Compaq
- X Cambex

16. Speed

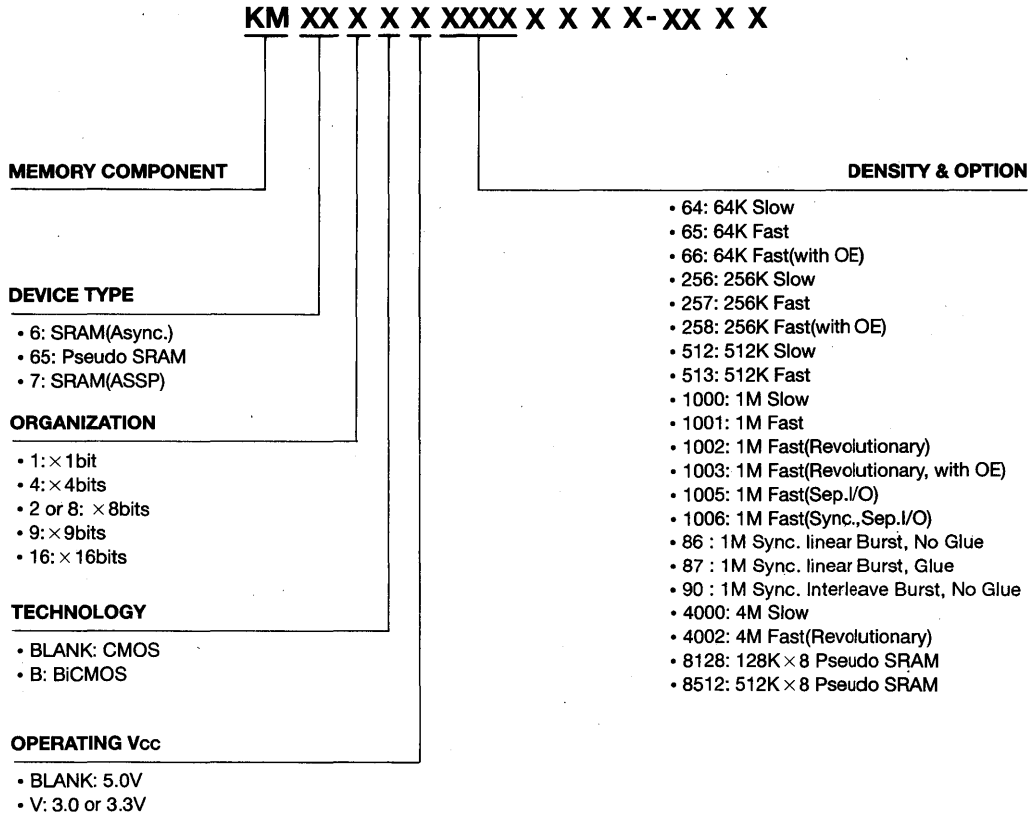
- 5 50ns
- 6 60ns
- 7 70ns
- 8 80ns



4.3 VRAM



4.4 Static RAM



4.4 Static RAM

KM XX X X X XXXXX X X X -XX X X

VERSION

- BLANK → A → B → C

OPERATING V_{cc}

- BLANK: 5.0V
- V: Wide Voltage

PACKAGES

- P: DIP
- G: SOP
- J: SOJ or PLCC
- T: TSOP(Standard Type)
- R: TSOP(Reverse Type)

POWER LIMITS

- BLANK: High Power
- L: Low Power
- L-L: Low Low Power

OPERATING TEMP

- BLANK: Commercial
- I: Industrial

SPEED

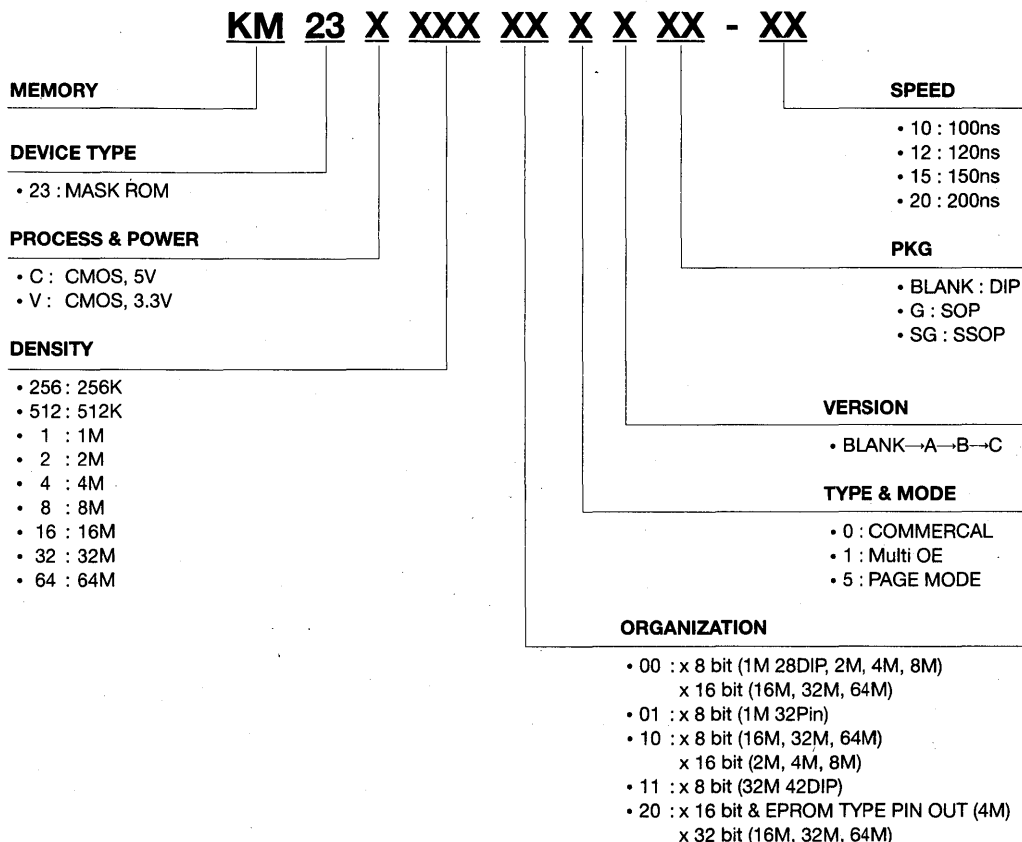
Slow

- 5: 55ns
- 7: 70ns
- 8: 80ns
- 10: 100ns
- 12: 120ns

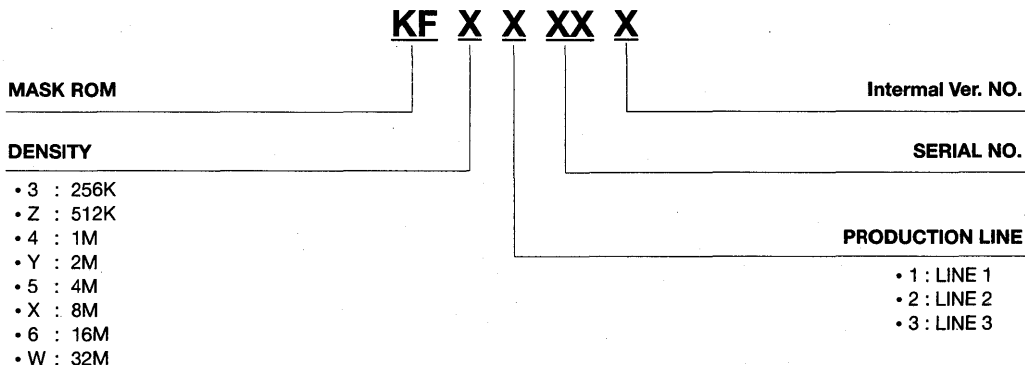
Fast

- 8: 8ns
- 9: 9ns
- 10: 10ns
- 12: 12ns
- 14: 14ns
- 15: 15ns
- 17: 17ns
- 19: 19ns
- 20: 20ns
- 24: 24ns
- 25: 25ns
- 30: 30ns
- 35: 35ns
- 45: 45ns

4.5 MASK ROM

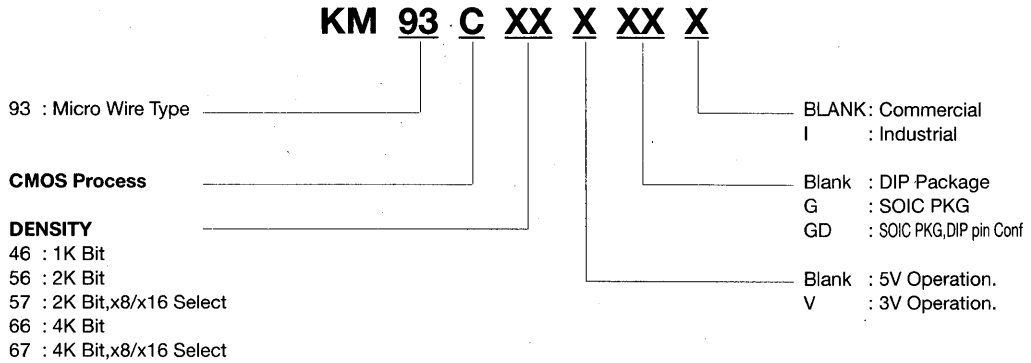


*** Internal KF · CODE Inforamtion**

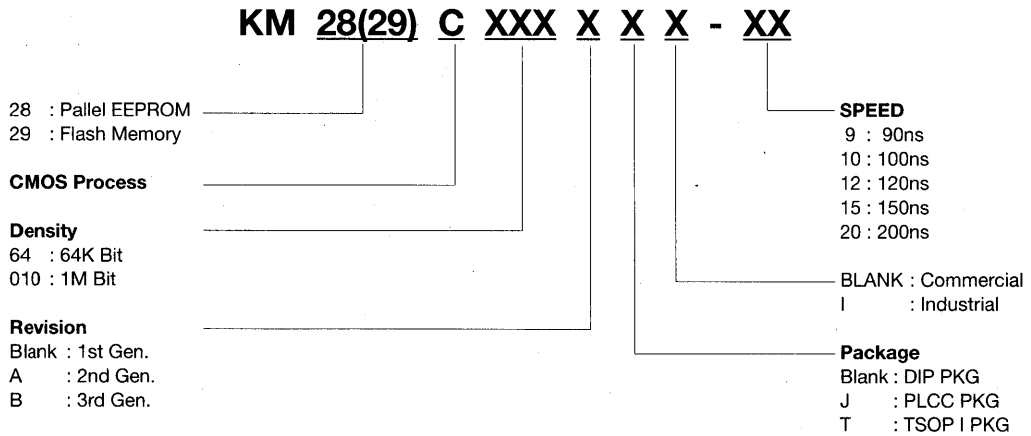


4.6 EEPROM

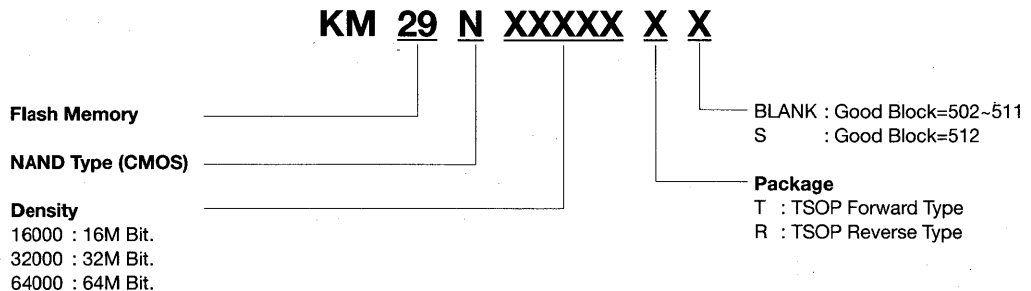
*Serial EEPROM



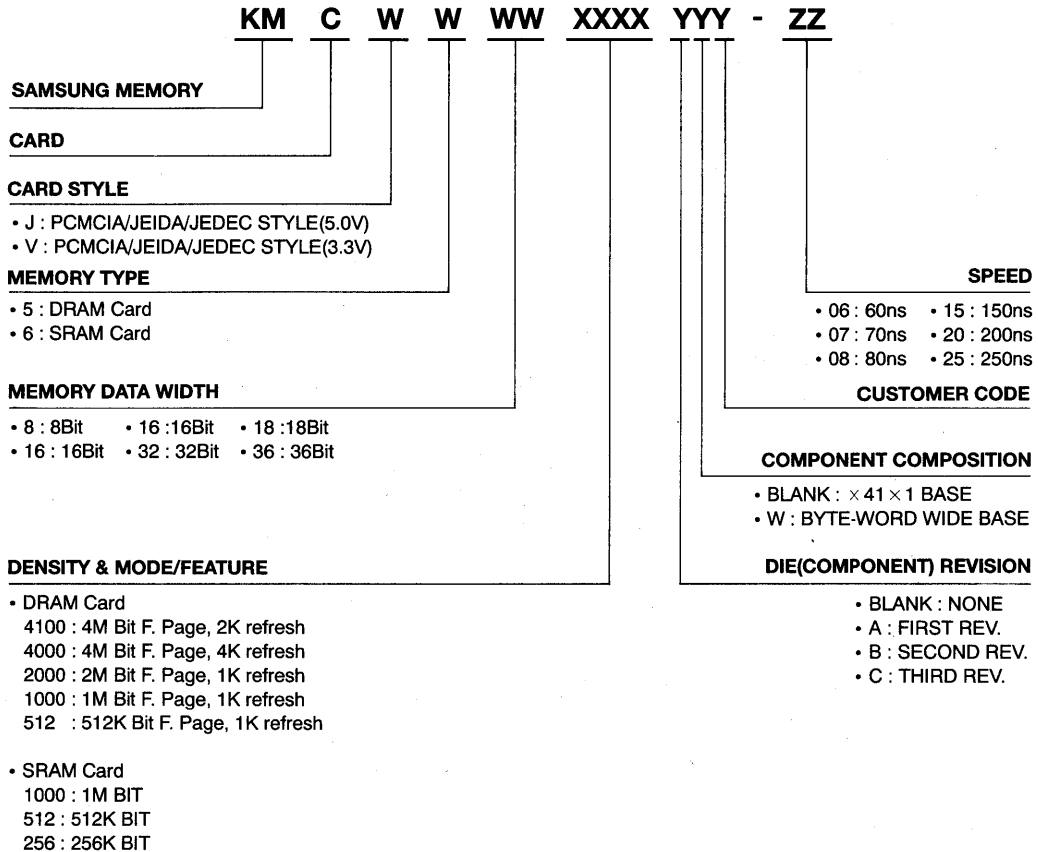
*Parallel EEPROM



4.7 Flash

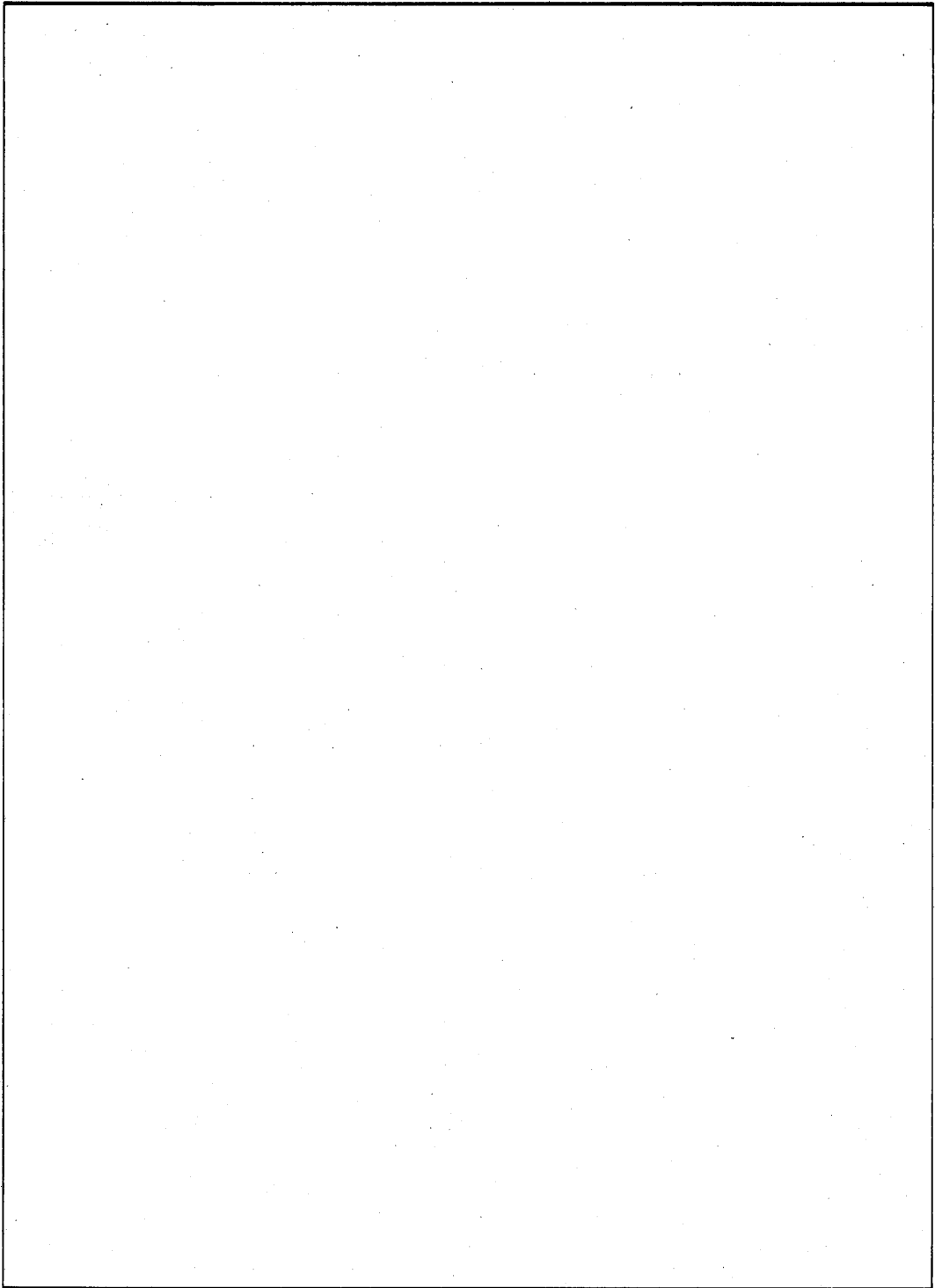


4.8 Memory Card

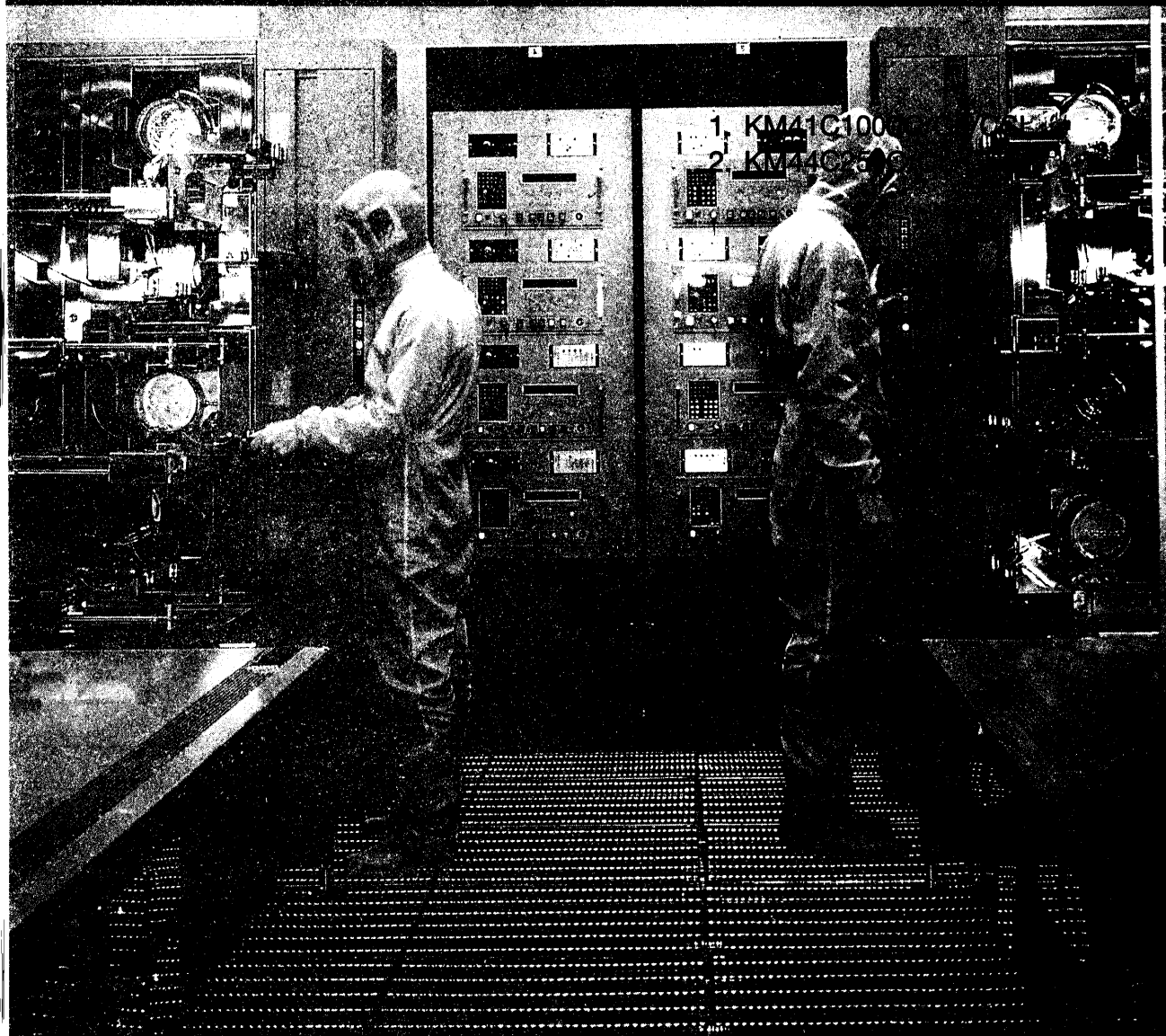


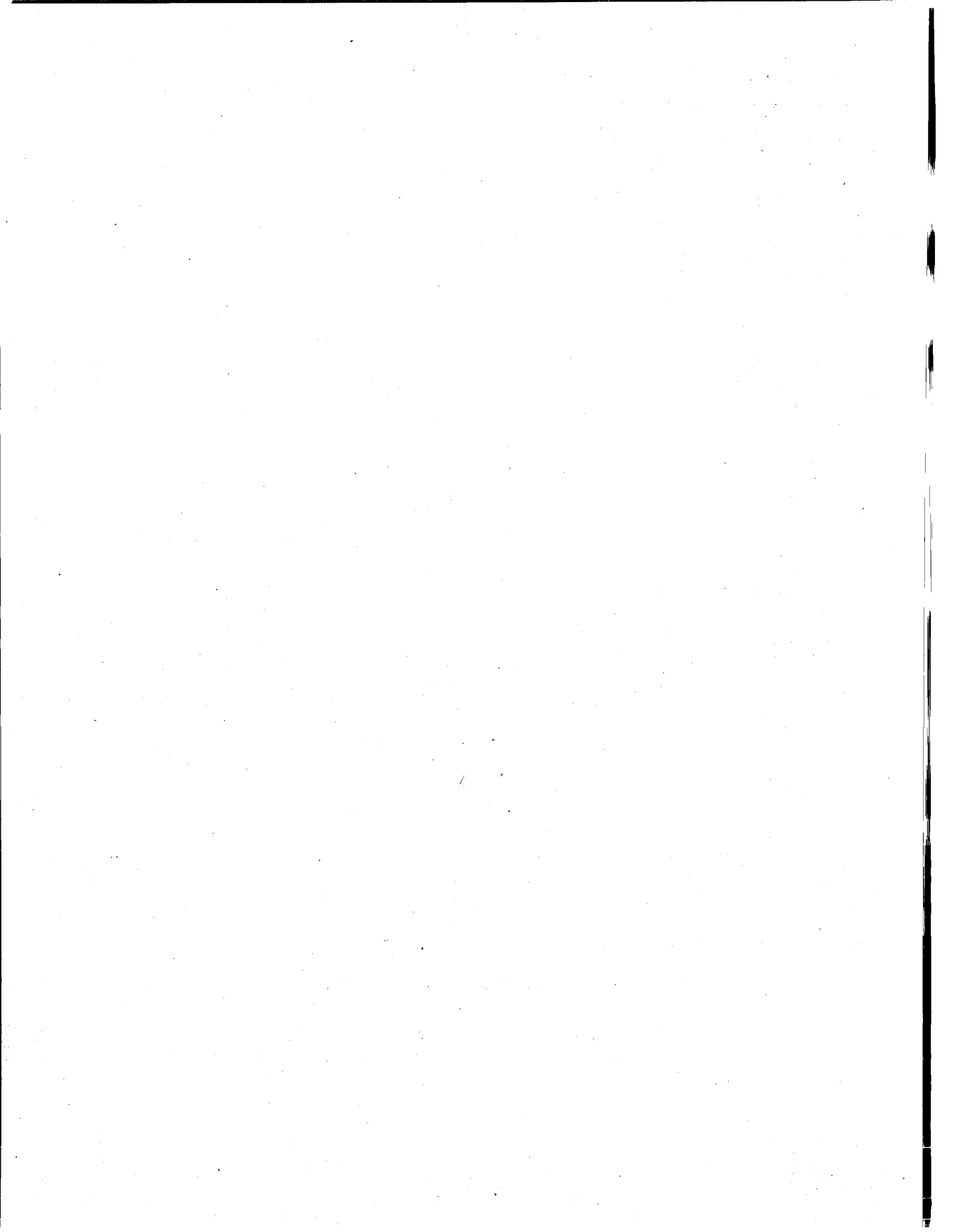
1

NOTES

A large, empty rectangular box with a thin black border, occupying most of the page below the 'NOTES' header. It is intended for handwritten notes.

1M DRAM DATA SHEET 2





1M x 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	trAC	tcAC	trC
KM41C1000C/CL/CSL-6	60ns	15ns	110ns
KM41C1000C/CL/CSL-7	70ns	20ns	130ns
KM41C1000C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden refresh capability**
- **TTL compatible input and output**
- **Single 5V ± 10% power supply**
- **Refresh Cycle**
 - 512 cycle/8ms refresh (Normal)
 - 512 cycle/64ms refresh (L-version)
 - 512 cycle/128ms refresh (SL-version)
- **Power Dissipation**
 - Standby : 5.5mW (Normal)
1.1mW (L-version)
0.55mW (SL-version)
 - Active(60/70/80ms) : 385/358/330mW
- **256K x 4 fast test mode**
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP, TSOP(I), TSOP(II) and PLCC Packages**

GENERAL DESCRIPTION

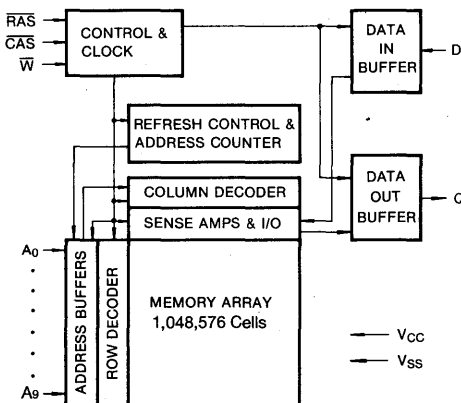
The Samsung KM41C1000C/CL/CSL is a CMOS high speed 1,048,576 x 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM41C1000C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and output are fully TTL compatible.

The KM41C1000C/CL/CSL is fabricated using Samsung's advanced CMOS process.

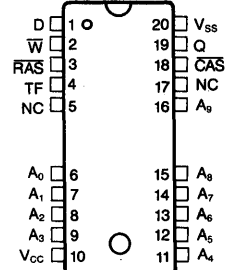
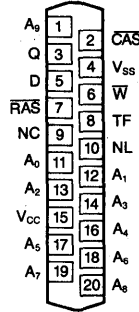
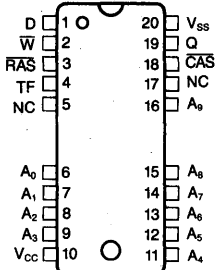
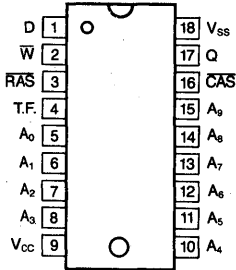
2

FUNCTIONAL BLOCK DIAGRAM



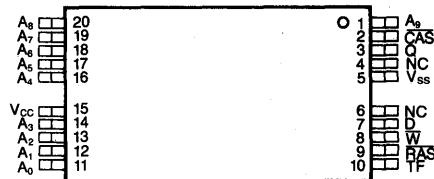
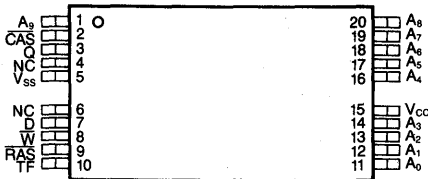
PIN CONFIGURATION (Top Views)

• KM41C1000CP/CLP/CSLP • KM41C1000CJ/CLJ/CSLJ • KM41C1000CZ/CLZ/CSLZ • KM41C1000CT/CLT/CSLT



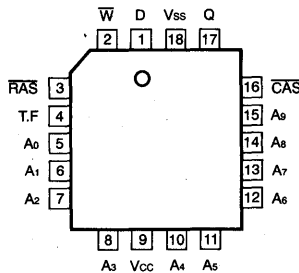
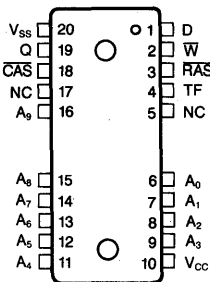
• KM41C1000CV/CLV/CSLV

• KM41C1000CVR/CLVR/CSLVR



• KM41C1000CTR/CLTR/CSLTR

• KM41C1000CG/CLG/CSLG



Pin Names	Pin Function
A_0 - A_9	Address Inputs
D	Data In
Q	Data Out
\bar{W}	Read/Write Input
RAS	Row Address Strobe
CAS	Column Address Strobe
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{DD}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} and \overline{CAS} , Address Cycling @trc=min.)	KM41C1000C/CL/CSL-6	-	70	mA
	KM41C1000C/CL/CSL-7	-	65	mA
	KM41C1000C/CL/CSL-8	-	60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	I _{CC2}	-	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @trc=min.)	KM41C1000C/CL/CSL-6	-	70	mA
	KM41C1000C/CL/CSL-7	-	65	mA
	KM41C1000C/CL/CSL-8	-	60	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @tpc=min.)	KM41C1000C/CL/CSL-6	-	55	mA
	KM41C1000C/CL/CSL-7	-	50	mA
	KM41C1000C/CL/CSL-8	-	45	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)	KM41C1000C	-	1	mA
	KM41C1000CL	-	200	μA
	KM41C1000CSL	-	100	μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM41C1000C/CL/CSL-6	-	70	mA
	KM41C1000C/CL/CSL-7	-	65	mA
	KM41C1000C/CL/CSL-8	-	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode ($\overline{CAS}=\overline{CAS}$ -Before- \overline{RAS} Cycling or 0.2V, W= $V_{CC}-0.2V$ or 0.2V, A ₀ -A ₉ = $V_{CC}-0.2V$ or 0.2V, DIN= $V_{CC}-0.2V$, 0.2V or OPEN : trc=250μS, tras=tras min.~1μS)	KM41C1000CL	-	200	μA
	KM41C1000CSL	-	100	μA
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ 6.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μA



DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, Address can be changed maximum two times while RAS=V_{IL}, I_{CC4}, Address can be changed maximum once during a Fast Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C _{IN1}	-	5	pF
Input Capacitance (A ₀ -A ₉)	C _{IN2}	-	6	pF
Input Capacitance (RAS, CAS, W)	C _{IN3}	-	7	pF
Output Capacitance (Q)	C _{OUT}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_a ≤ 70°C, V_{CC}=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	130		150		170		ns	
Access time from RAS	trac		60		70		80	ns	3,4,11
Access time from CAS	tcac		15		20		20	ns	3,4,5
Access time from column address	t _{aa}		30		35		40	ns	3,10
CAS to output in Low-Z	t _{clz}	0		0		0		ns	3
Output buffer turn-off delay	t _{off}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t _t	3	50	3	50	3	50	ns	2
RAS precharge time	trp	40		50		60		ns	
RAS pulse width	tr _{as}	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	tr _{sh}	15		20		20		ns	
CAS hold time	tc _{sh}	60		70		80		ns	
CAS pulse width	tc _{as}	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	tr _{cd}	20	45	20	50	20	60	ns	4
RAS to column address delay time	tr _{ad}	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tc _{rp}	5		5		5		ns	
Row address set-up time	t _{asr}	0		0		0		ns	
Row address hold time	tr _{ah}	10		10		10		ns	
Column address set-up time	t _{asc}	0		0		0		ns	
Column address hold time	tc _{ah}	15		15		15		ns	
Column address to RAS lead time	tr _{al}	30		35		40		ns	
Read command set-up time	tr _{cs}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command hold time	twCH	10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	15		15		15		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	15		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tdHR	50		55		60		ns	6
Refresh period (Normal)	trEF		16		16		16	ms	
Refresh period (Low power)	trEF		64		64		64	ms	
Refresh period (Super Low power)	trEF		128		128		128	ms	
Write command set-up time	twCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	15		20		20		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	60		70		80		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	30		35		40		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	15		15		15		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	trPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tcPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		35		35		40	ns	3
Fast Page mode cycle time	tpC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tpRWC	60		60		65		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	trASP	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	40		45		50		ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	tcp	10		10		10		ns	

2

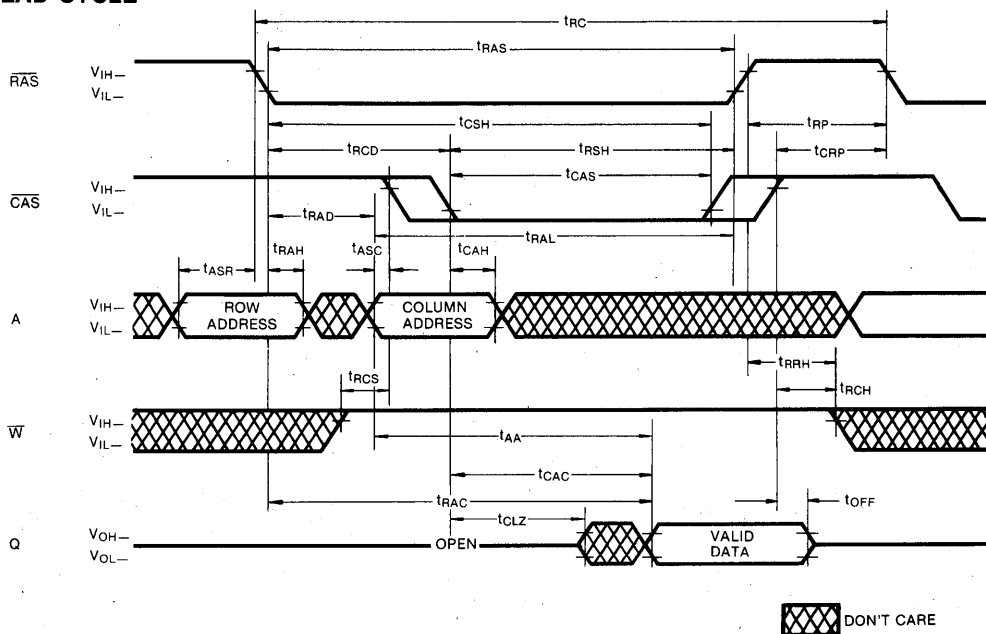
NOTES

1. An initial pause of 200 μ s is required after power up followed by any 8 RAS cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and

- the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\min)$ and $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. Normal operation requires the "T.F" pin to be connected to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
13. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact Samsung for specific operational details of the "test function."
14. In a test mode read cycle, the value of t_{RAC} , t_{CAC} , t_{AA} is delayed for 3ns.

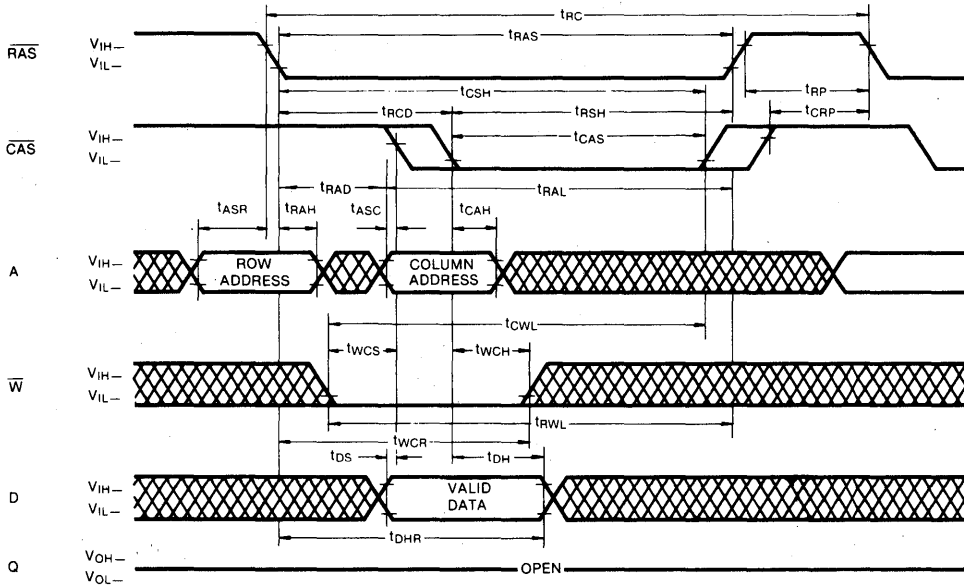
TIMING DIAGRAMS

READ CYCLE



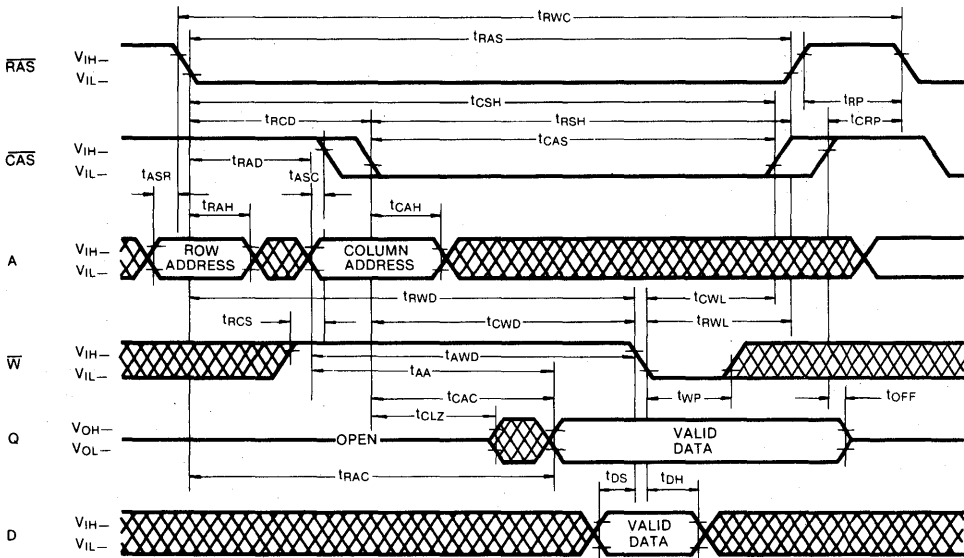
TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



2

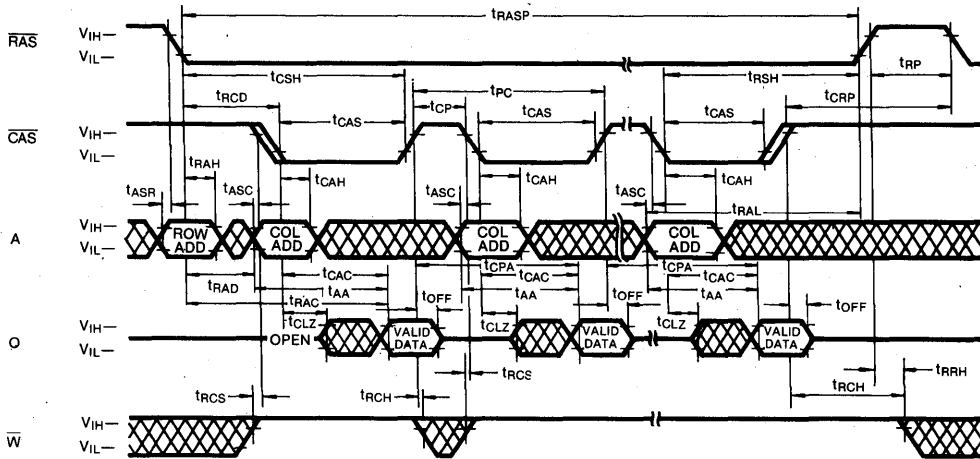
READ-WRITE/READ-MODIFY-WRITE CYCLE



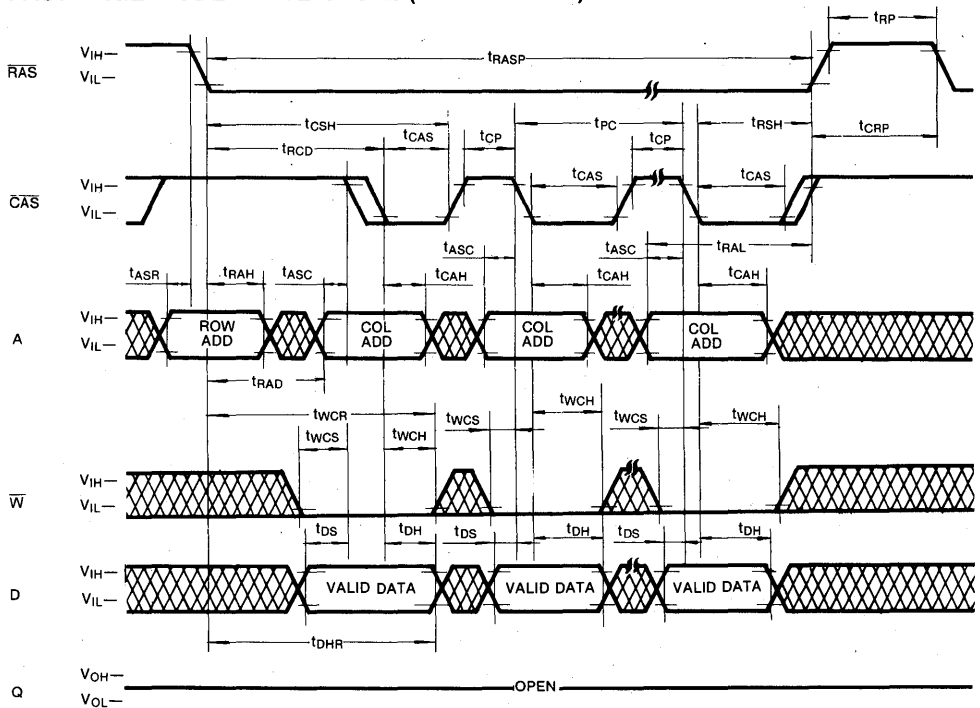
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



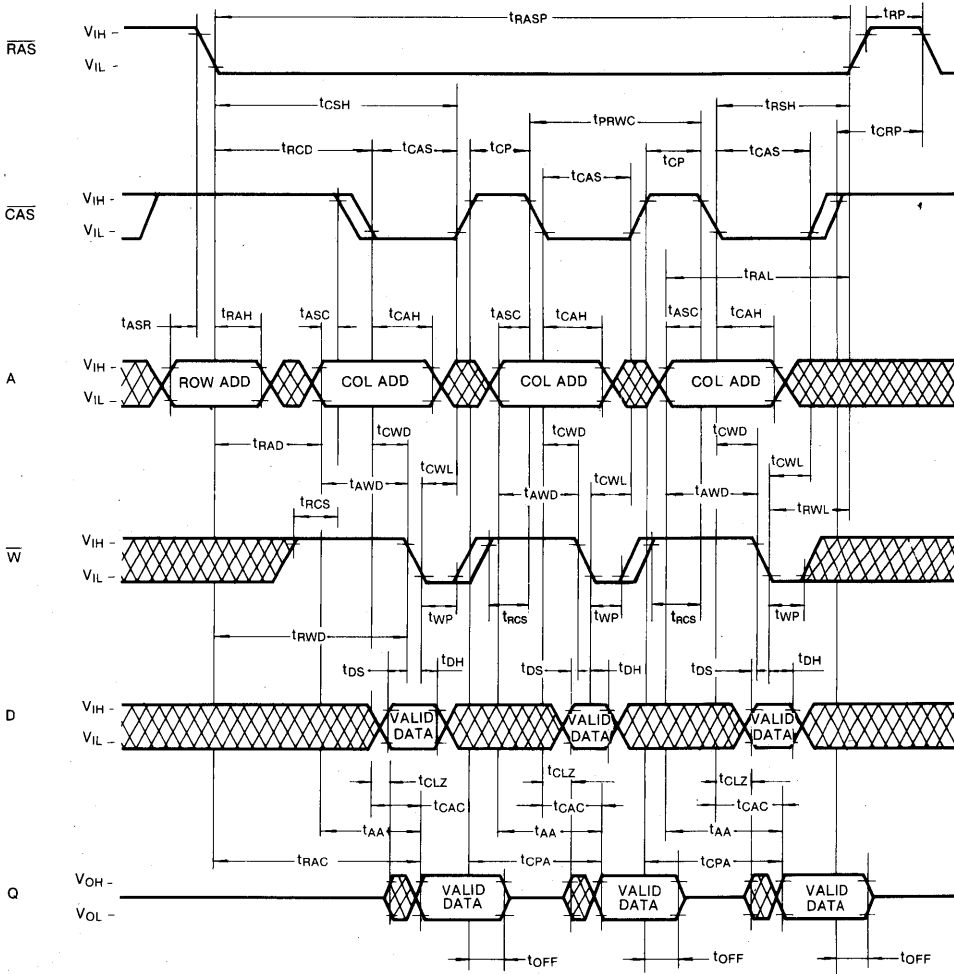
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



⊗ DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-WRITE CYCLE

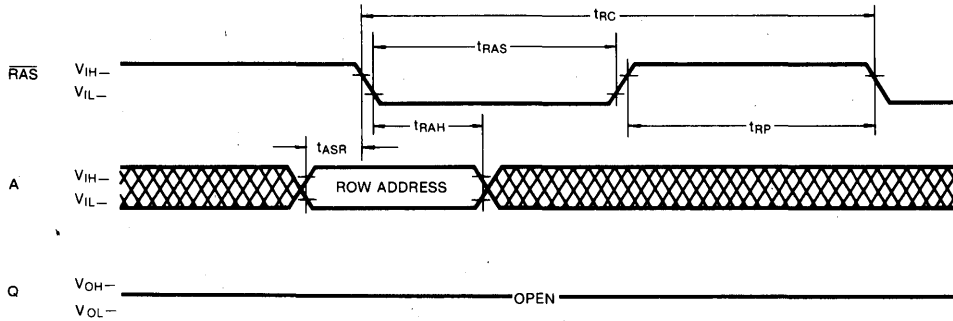


DON'T CARE

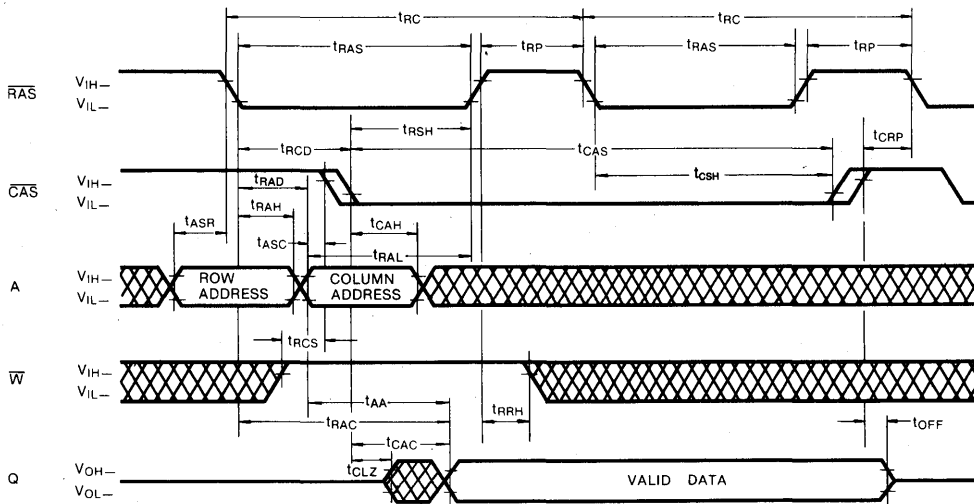
TIMING DIAGRAMS (Continued)

RAS-ONLY REFRESH CYCLE

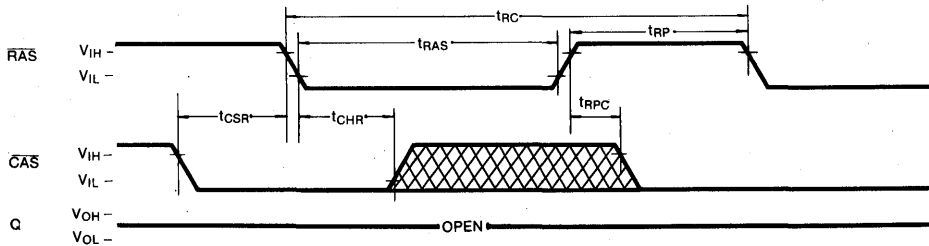
Note: CAS = V_{IH}, W, D, A₉ = Don't Care



HIDDEN REFRESH CYCLE



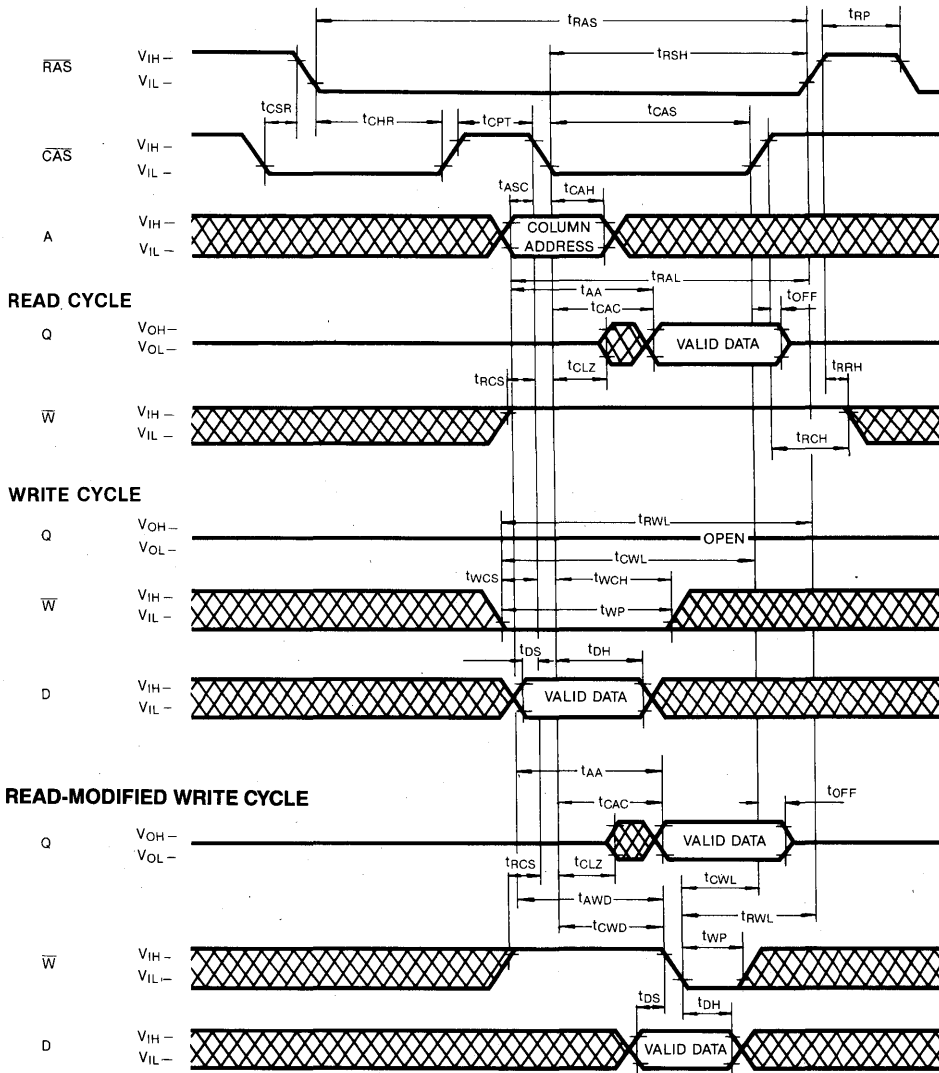
CAS-BEFORE-RAS REFRESH CYCLE



 DON'T CARE

TIMING DIAGRAMS (Continued)

$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DON'T CARE

2

DEVICE OPERATION

The KM41C1000C/CL/CSL contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the KM41C1000C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}), and the valid row and column address inputs.

Operation of the KM41C1000C/CL/CSL begins by strobing in a valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM41C1000C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C1000C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition.

If \overline{CAS} goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However if \overline{CAS} goes low after $t_{RCD(max)}$, or if the column address becomes valid after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

Write

The KM41C1000C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} and \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention

Late Write: If \overline{W} is brought low after \overline{CAS} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{CWD} and t_{AWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C1000C/CL/CSL has a three-state output buffer which is controlled by \overline{CAS} . Whenever \overline{CAS} is high (V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until \overline{CAS} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM41C1000C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Fast Page Mode Write, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh, $\overline{\text{CAS}}$ only cycle.

Indeterminate Output State: Delayed Write.

Refresh

The data in the KM41C1000C/CL/CSL is stored on a tiny capacitor with each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/64/128 ms. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A₀-A₈). The state of address A₉ is ignored during refresh.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM41C1000C/CL/CSL has $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held low for the specified set up time (tCS_R) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CAS}}$ active time and cycling $\overline{\text{RAS}}$. The KM41C1000C/CL/CSL hidden refresh cycle is actually a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C1000C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry. The cycle begins as a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation. Then, if $\overline{\text{CAS}}$ is brought high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled. In this mode, the low address bits A₀ through A₈ are supplied by the on-chip refresh counter. The A₉ bit is set low internally.

Fast Page Mode

The KM41C1000C/CL/CSL has Fast page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{\text{RAS}}$ is kept low to maintain the row address $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page

Power-up

If $\overline{\text{RAS}} = V_{\text{SS}}$ during power-up, the KM41C1000C/CL/CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{CC} during power-up or be held at a valid V_{IN} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8msec period in which there are no $\overline{\text{RAS}}$ cycles. An initialization cycle is any cycle in which $\overline{\text{RAS}}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM41C1000C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C1000C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

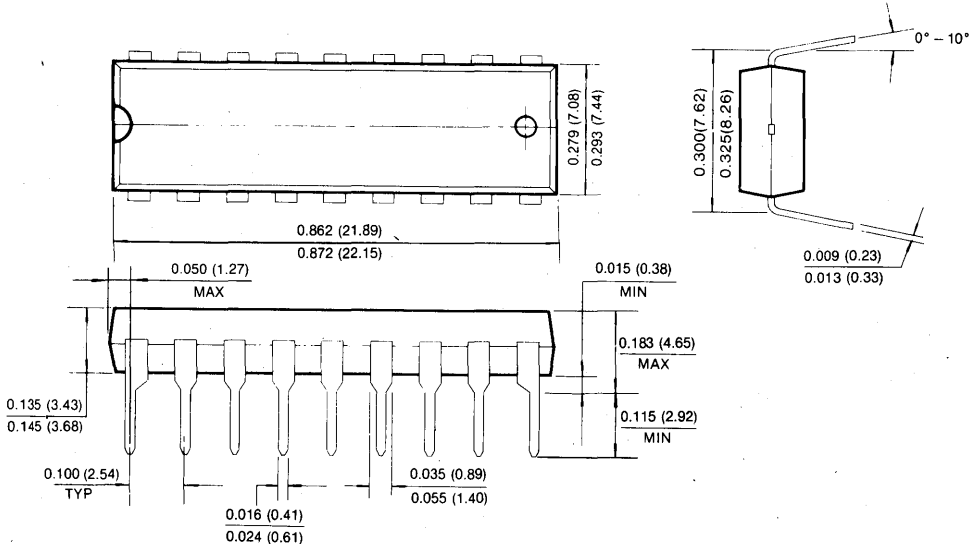
A high frequency 0.1μF ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41C1000C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C1000C/CL/CSL and they supply much of the current used by the KM41C1000C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47μF to 100μF should be used for bulk decoupling to recharge the 0.1μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

18-LEAD PLASTIC DUAL IN-LINE PACKAGE

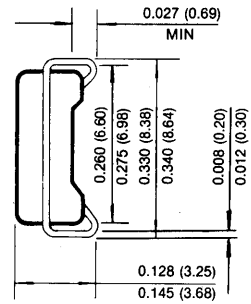
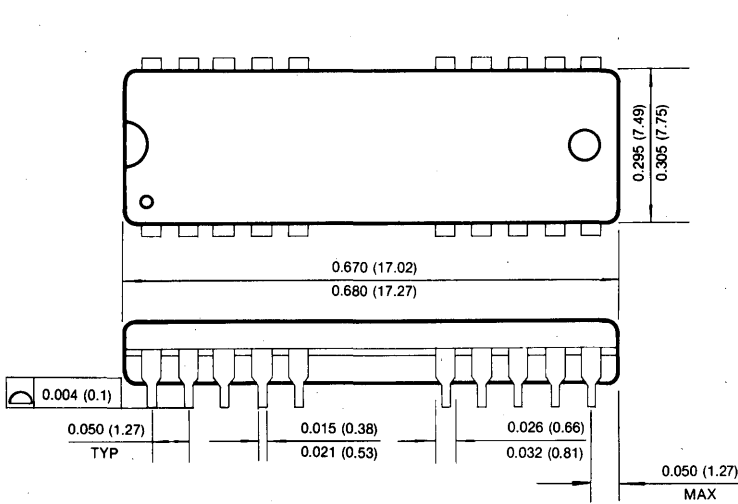
Units: Inches (Millimeters)



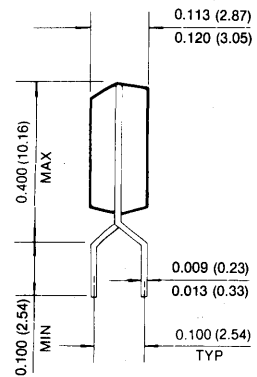
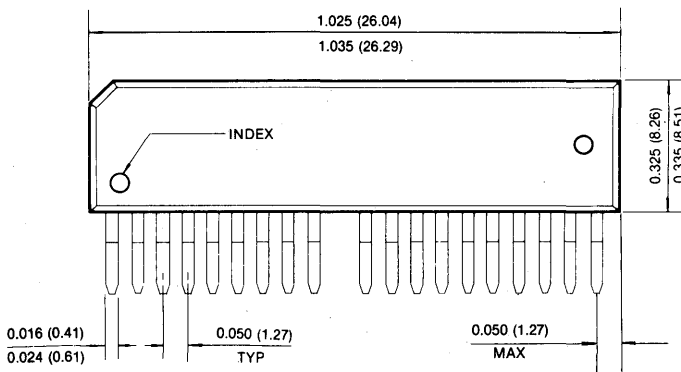
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

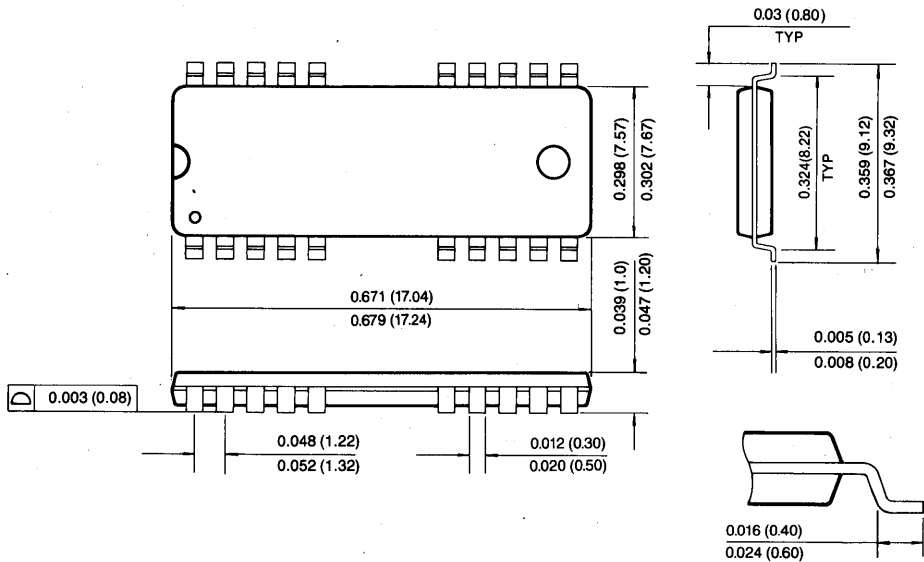


2

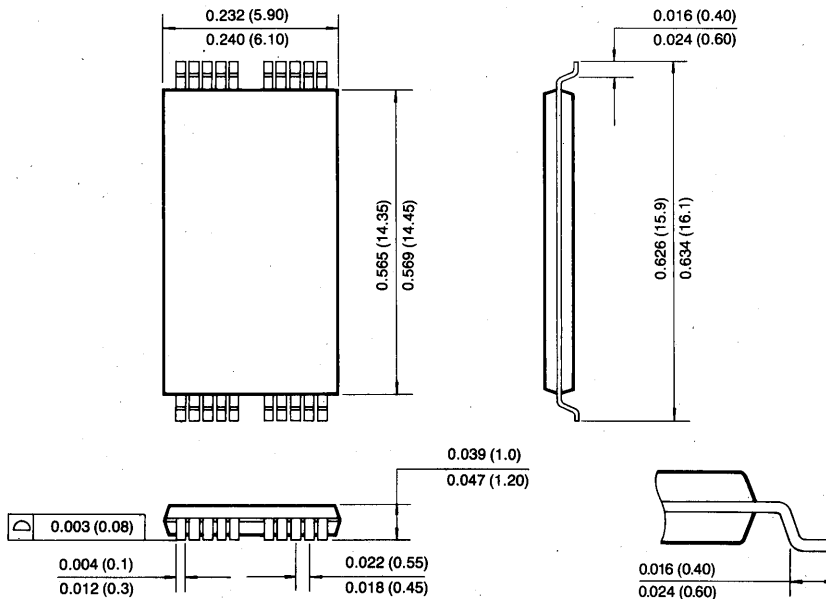
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)

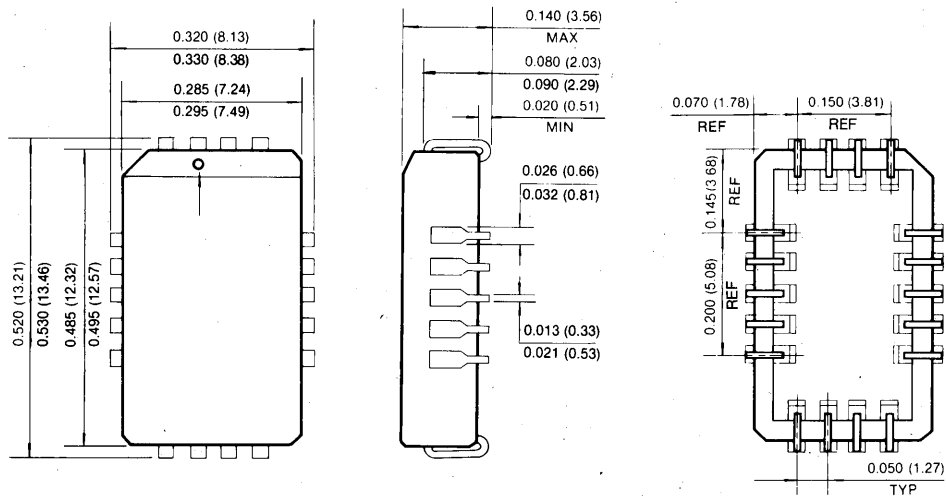


20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



PACKAGE DIMENSIONS (Continued)

18-LEAD PLASTIC CHIP CARRIER



2

256K x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	t _{RAC}	t _{CAC}	t _{RC}
KM44C256C/CL/CSL-6	60ns	15ns	110ns
KM44C256C/CL/CSL-7	70ns	20ns	130ns
KM44C256C/CL/CSL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or Output Enable Controlled Write**
- **Single 5V ± 10% power supply**
- **Refresh Cycle**
 - 512 cycle/8ms refresh (Normal)
 - 512 cycle/64ms refresh (L-version)
 - 512 cycle/128ms refresh (SL-version)
- **Power Dissipation**
 - Standby : 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.55mW (SL-version)
 - Active(60/70/80ms) : 385/360/330mW
- **JEDEC standard pinout**
- **Available in plastic DIP, SOJ, ZIP, TSOP(I), and TSOP(II) Packages**

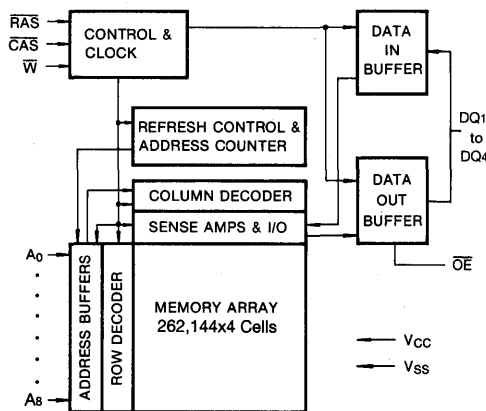
GENERAL DESCRIPTION

The Samsung KM44C256C/CL/CSL is a CMOS high speed 262,144 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The KM44C256C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

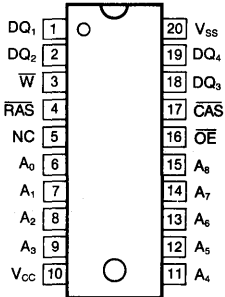
The KM44C256C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

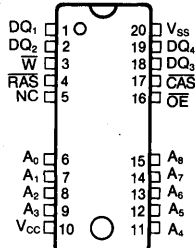


PIN CONFIGURATION (Top Views)

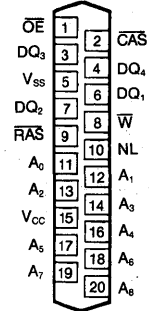
• KM44C256CP/CLP/CSLP



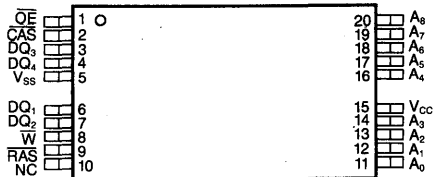
• KM44C256CJ/CLJ/CSLJ



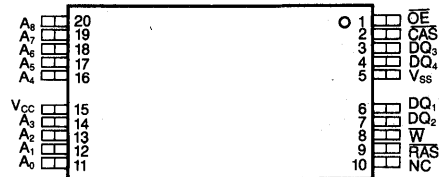
• KM44C256CZ/CLZ/CSLZ



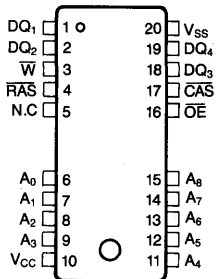
• KM44C256CV/CLV/CSLV



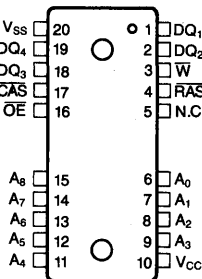
• KM44C256CVR/CLVR/CSLVR



• KM44C256CT/CLT/CSLT



• KM44C256CTR/CLTR/CSLTR



Pin Names	Pin Function
A ₀ -A ₈	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
DQ ₁ -DQ ₄	Data In/Data Out
V _{CC}	Power (+5V)
V _{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{DD}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS, Address Cycling @trc=min.)	KM44C256C/CL/CSL-6	-	70	mA
	KM44C256C/CL/CSL-7	-	65	mA
	KM44C256C/CL/CSL-8	-	60	mA
Standby Current (RAS=CAS=W=V _{IH})	I _{CC2}	-	2	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM44C256C/CL/CSL-6	-	70	mA
	KM44C256C/CL/CSL-7	-	65	mA
	KM44C256C/CL/CSL-8	-	60	mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM44C256C/CL/CSL-6	-	55	mA
	KM44C256C/CL/CSL-7	-	50	mA
	KM44C256C/CL/CSL-8	-	45	mA
Standby Current (RAS=CAS=W=V _{CC} -0.2V)	KM44C256C	-	1	mA
	KM44C256CL	-	200	μA
	KM44C256CSL	-	100	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44C256C/CL/CSL-6	-	70	mA
	KM44C256C/CL/CSL-7	-	65	mA
	KM44C256C/CL/CSL-8	-	60	mA
Battery Back Up Current Average Power Supply Current, Battery back up Mode (CAS=CAS-Before-RAS Cycling or 0.2V, W=V _{CC} -0.2V or 0.2V, A ₀ -A ₉ =V _{CC} -0.2V or 0.2V, D _{IN} =V _{CC} -0.2V, 0.2V or OPEN : trc=250μS, tras=tras min.~1μS)	I _{CC7}	-	200	μA
		-	100	μA
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ 6.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0 ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μA



DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$, I_{CC4}, Address can be changed maximum once during a Fast Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₈)	C _{IN1}	-	6	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W})	C _{IN2}	-	7	pF
Output Capacitance (DQ ₁ ~DQ ₄)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC}=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		175		195		ns	
Access time from \overline{RAS}	t _{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,10
\overline{CAS} to output in Low-Z	t _{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t _{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t _T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t _{RP}	40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	15		20		20		ns	
\overline{CAS} hold time	t _{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t _{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	15		15		15		ns	
Column address to \overline{RAS} lead time	t _{RAL}	30		35		40		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	15		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	55		55		60		ns	6
Write command pulse width	tWP	15		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		15		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	15		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	50		55		60		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (Low power)	tREF		64		64		64	ms	
Refresh period (Super Low power)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		45		45		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		65		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		5		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	15		15		15		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C-B-R}}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		35		40	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		85		90		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	40		45		50		ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	tROH	15		20		20		ns	
$\overline{\text{OE}}$ access time	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tO EZ	0	15	0	20		20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	15		20		20		ns	

NOTES

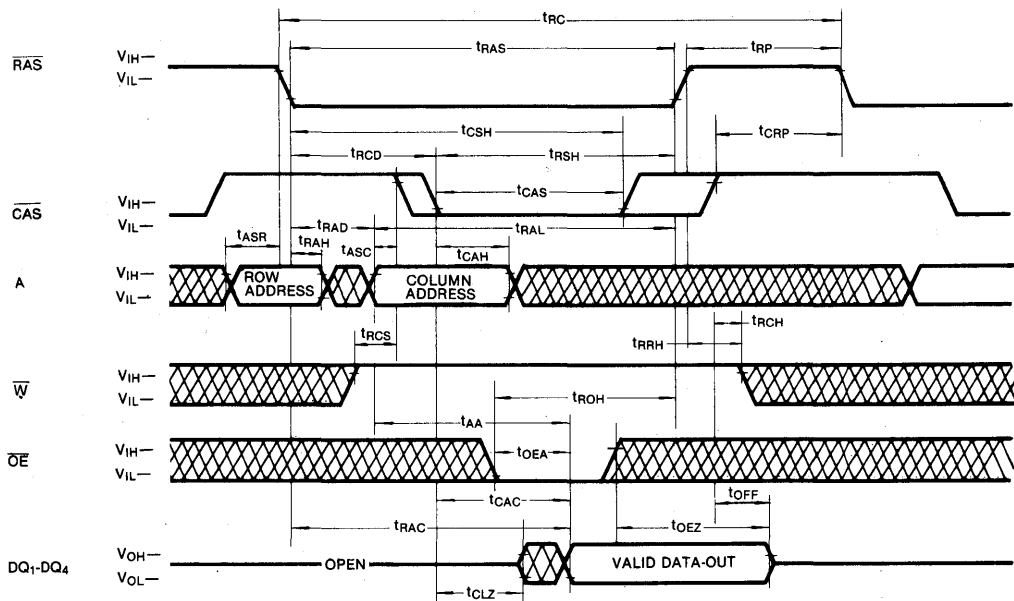
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC} .

NOTES (Continued)

5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{WCR} , t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAC(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA} .

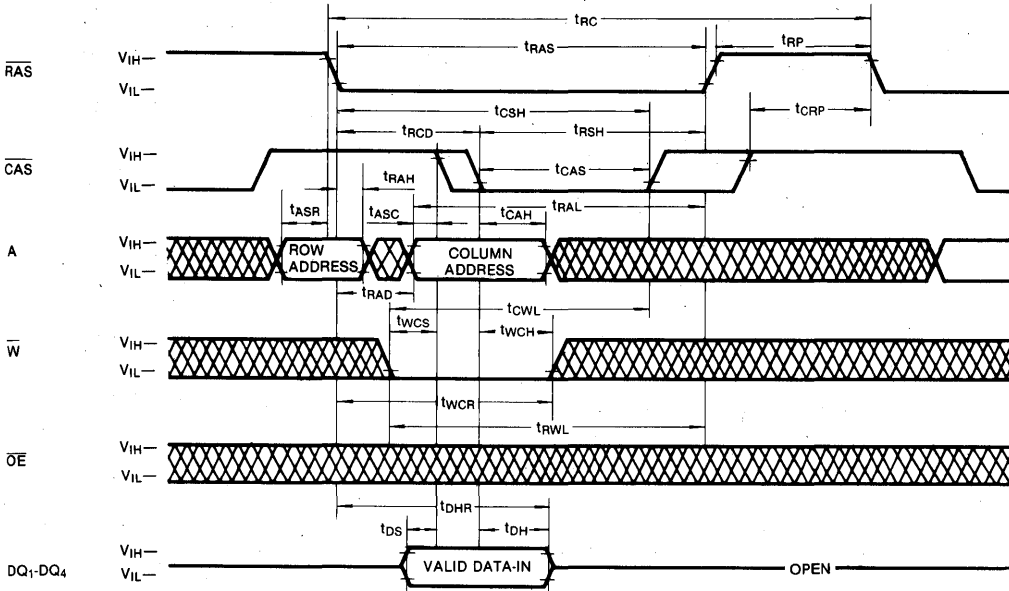
TIMING DIAGRAMS

READ CYCLE

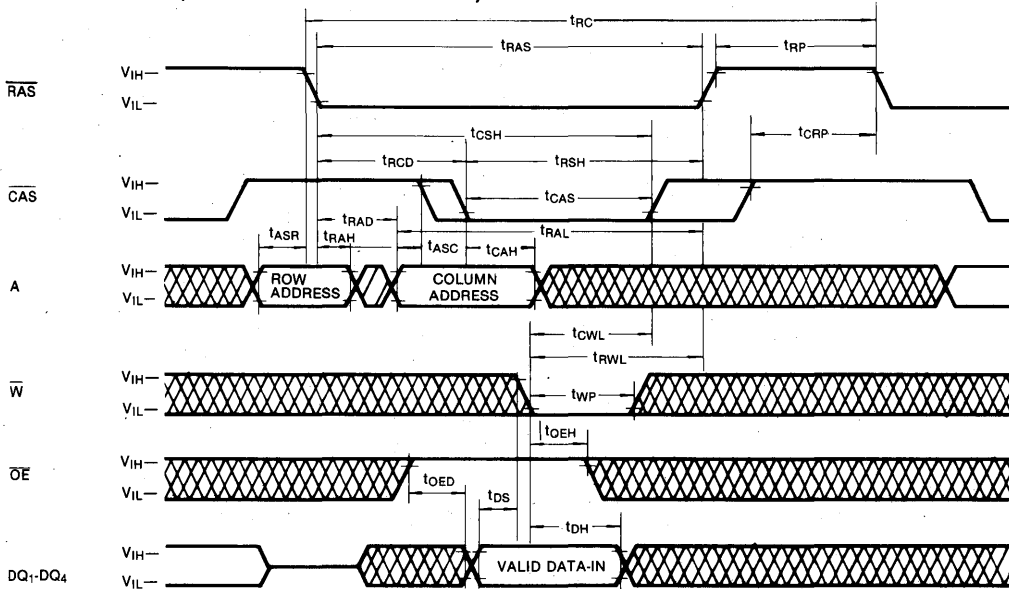


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



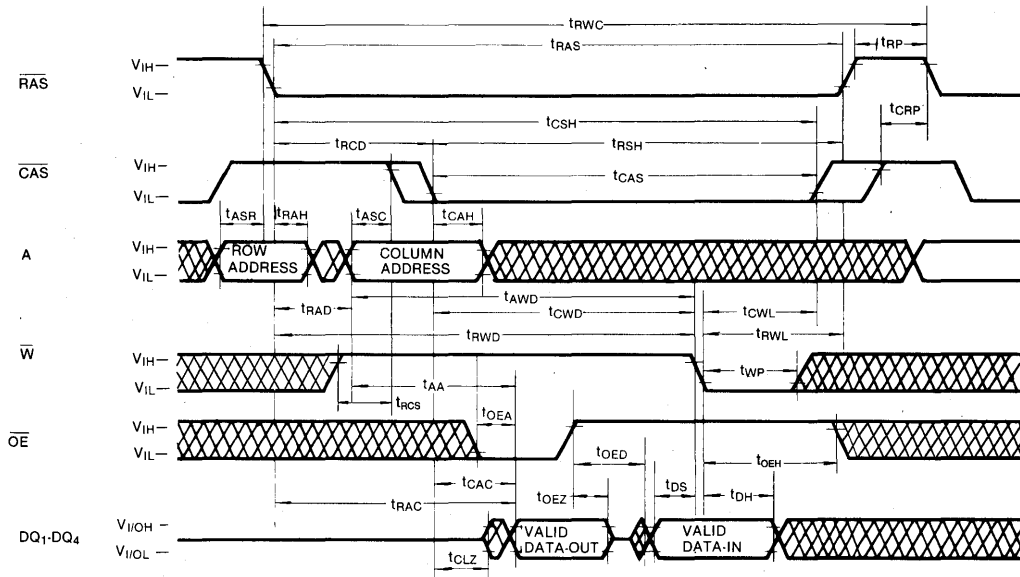
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



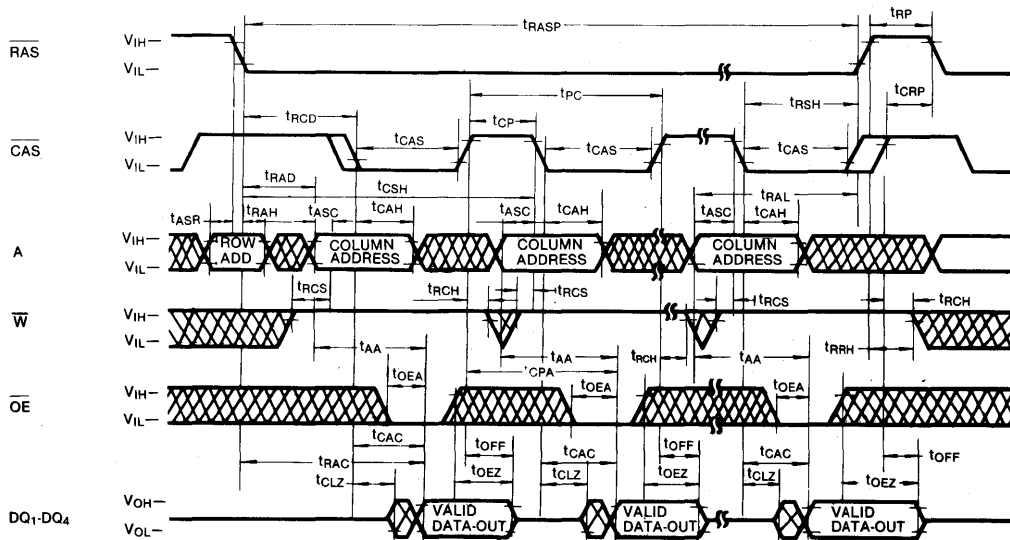
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

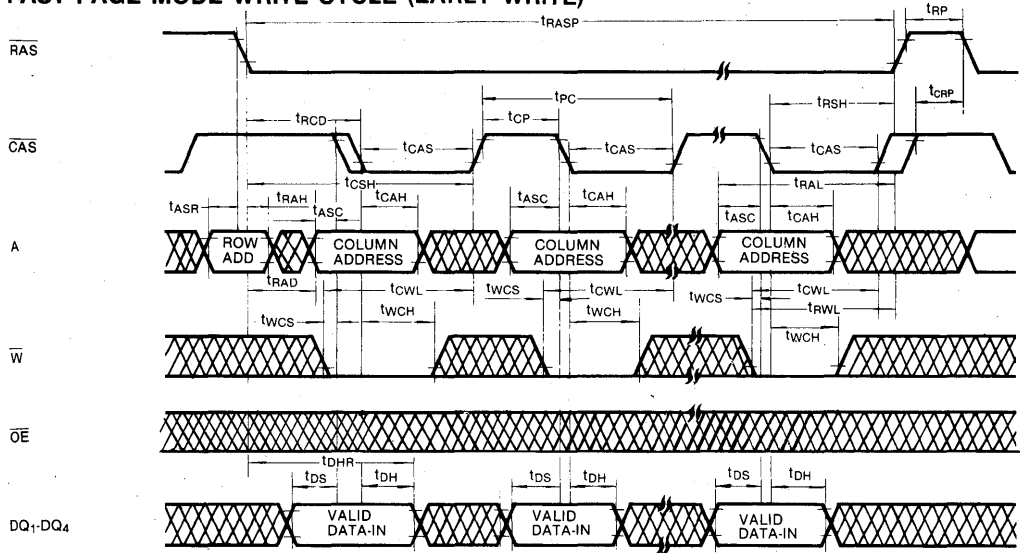


 DON'T CARE

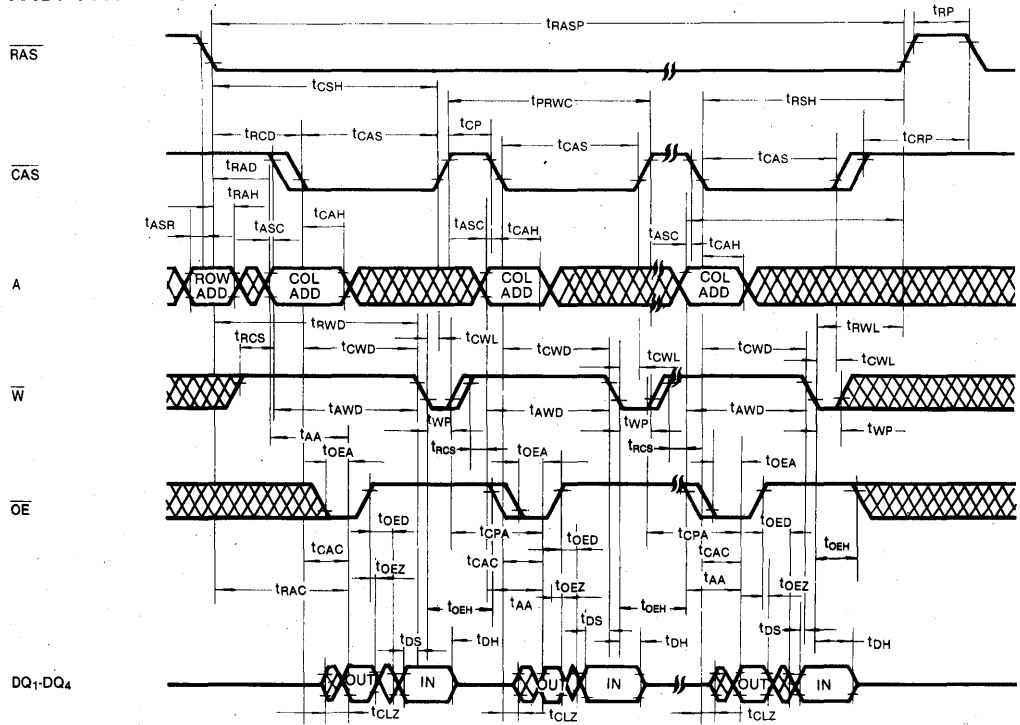
2

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE

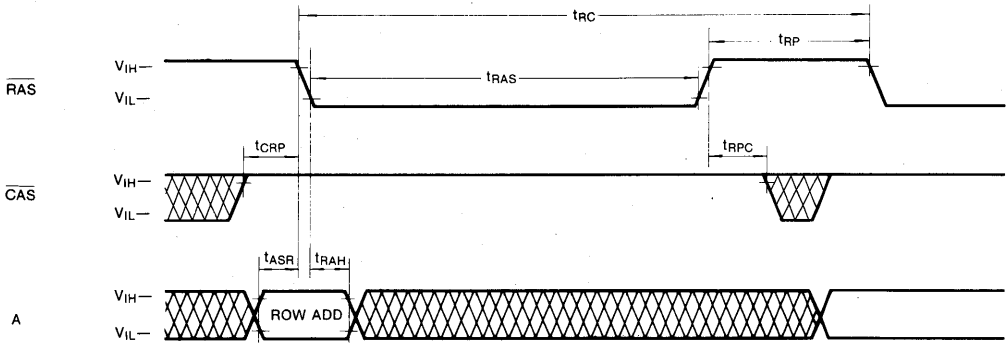


 DON'T CARE

TIMING DIAGRAMS (Continued)

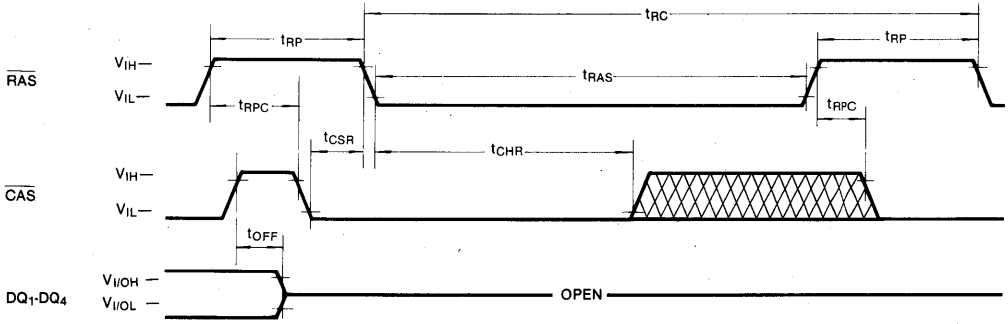
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} = Don't care



CAS-BEFORE-RAS REFRESH CYCLE

Note: \overline{W} , \overline{OE} , A = Don't care

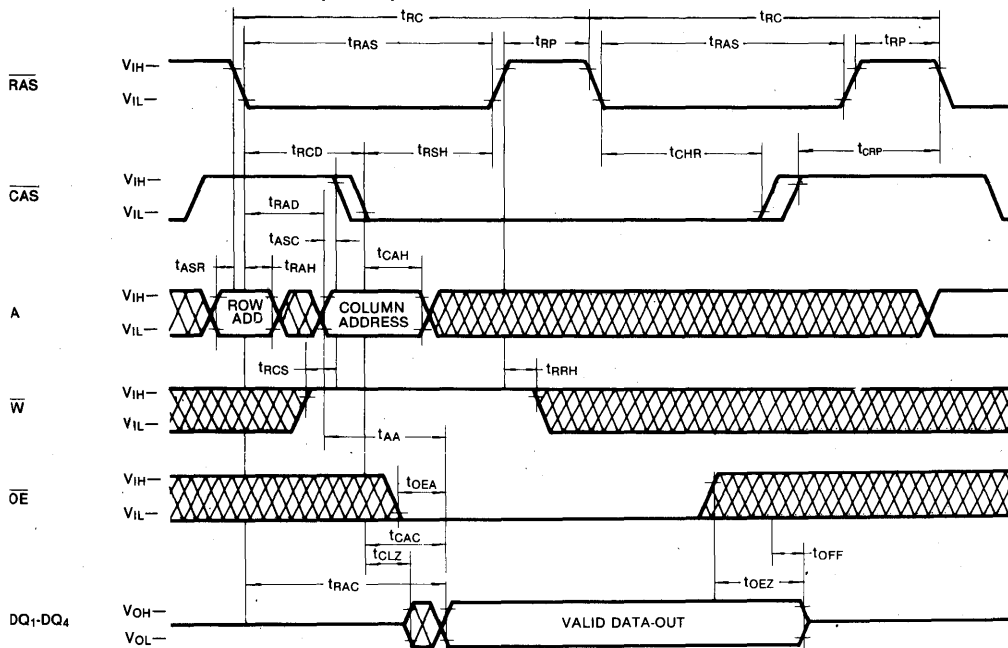


 DON'T CARE

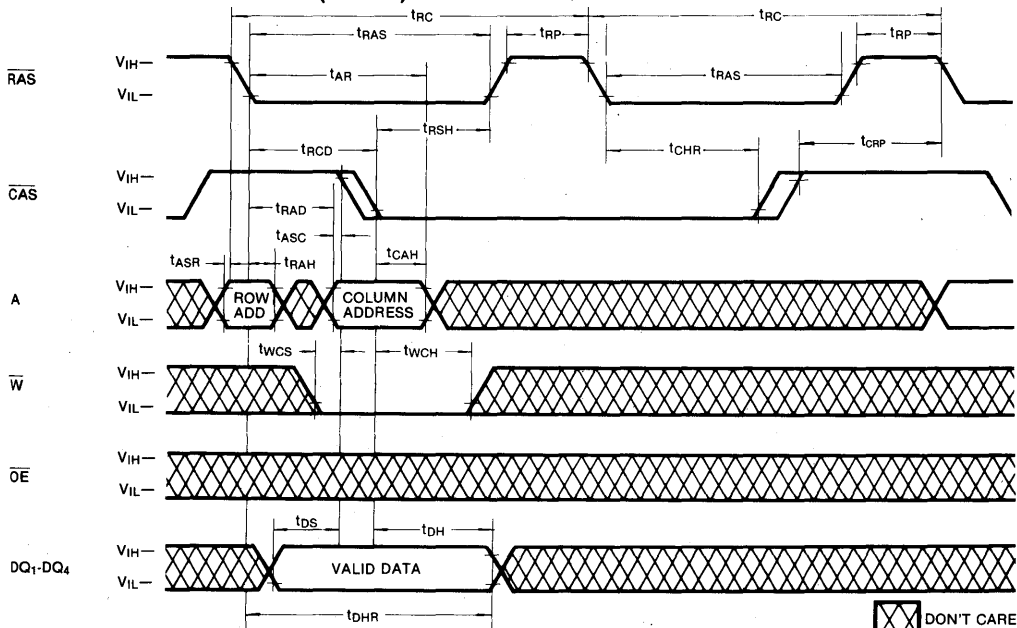
2

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



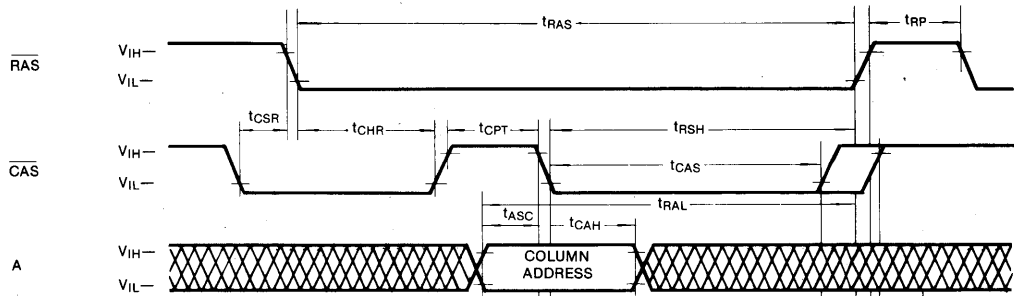
HIDDEN REFRESH CYCLE (WRITE)



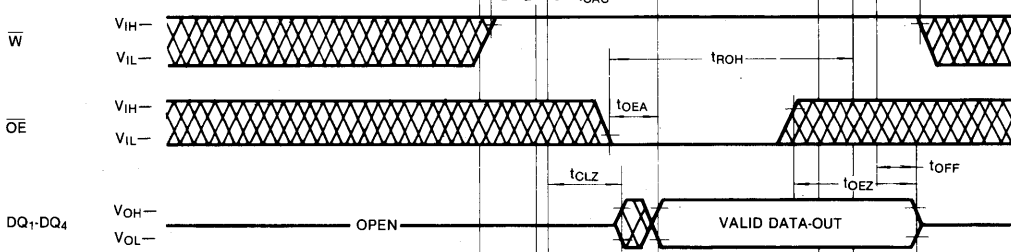
 DON'T CARE

TIMING DIAGRAMS (Continued)

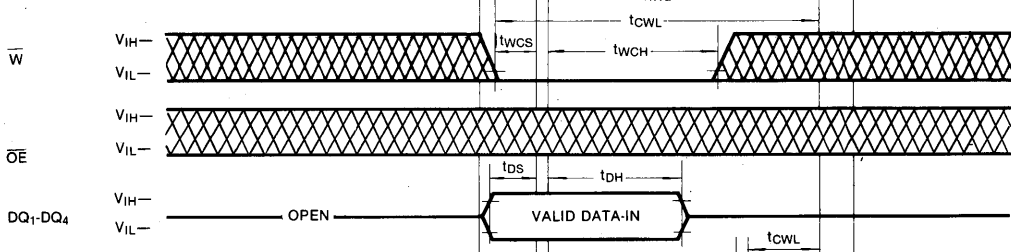
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



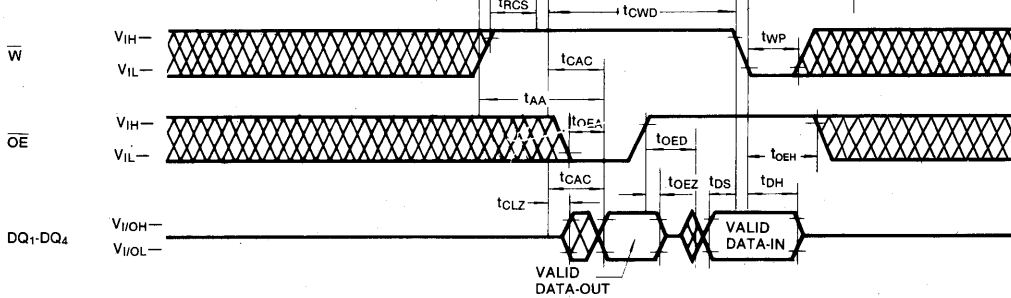
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



DON'T CARE

2

DEVICE OPERATION

Device operation

The KM44C256C/CL/CSL contains 1,048,576 memory locations organized as 262,144 four-bit words. Eighteen address bits are required to address a particular 4-bit word in the memory array. Since the KM44C256C/CL/CSL has only 9 address input pins, time multiplexed addressing is used to input 9 row and 9 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}), and the valid row and column address inputs.

Operation of the KM44C256C/CL/CSL begins by strobing in a valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 9 address input pins is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM44C256C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C256C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition.

If \overline{CAS} goes low before $t_{RCB(max)}$ and if the column address is valid before $t_{RAD(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However if \overline{CAS} goes low after $t_{RCB(max)}$, or if the column address becomes valid after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{TAA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCB(max)}$ and $t_{RAD(max)}$.

The KM44C256C/CL/CSL has common data I/O pins. For this reason an output enable control input (\overline{OE}) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, \overline{OE} must be low for the period of time defined by t_{OEa} and t_{OEz} .

Write

The KM44C256C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} and \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The 4-bit wide data at the data input pin is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write timing requirements. This output enable input (\overline{OE}) must be low during the time defined by t_{OEa} and t_{OEz} for data to appear at the outputs. If t_{CWD} and t_{TRWD} are not met the output may contain invalid data. Conforming to the \overline{OE} timing requirements prevents bus contention on the KM44C256C/CL/CSL's DQ pins.

Data Output

The KM44C256C/CL/CSL has a three-state output buffer which is controlled by \overline{CAS} and \overline{OE} . Whenever \overline{CAS} or \overline{OE} is high (V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{TAA} specify when the valid data will be present at the output. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM44C256C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode

DEVICE OPERATION (Continued)

Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Fast Page Mode Write, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh, $\overline{\text{CAS}}$ only cycle.

Indeterminate Output State: Delayed Write (t_{cwd} or t_{awd} are not met)

Refresh

The data in the KM44C256C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 8/64/128 ms. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. This cycle must be repeated for each of the 512 row addresses, (A_0 - A_8).

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM44C256C/CL/CSL has $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held low for the specified set up time (t_{CSR}) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CAS}}$ active time and cycling $\overline{\text{RAS}}$. The KM44C256C/CL/CSL hidden refresh cycle is actually a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C256C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry. The cycle

begins as a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation. Then, if $\overline{\text{CAS}}$ is brought high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled. In this mode, the low address bits A_0 through A_8 are supplied by the on-chip refresh counter.

Fast Page Mode

The Fast page mode Provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. Then, while $\overline{\text{RAS}}$ is kept low to maintain the row address $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page

Power-up

If $\overline{\text{RAS}}=\text{V}_{\text{SS}}$ during power-up, the KM44C256C/CL/CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8msec period in which there are no $\overline{\text{RAS}}$ cycles. An initialization cycle is any cycle in which $\overline{\text{RAS}}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C256C/CL/CSL inputs act like unteminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C256-C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS

DEVICE OPERATION (Continued)

run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

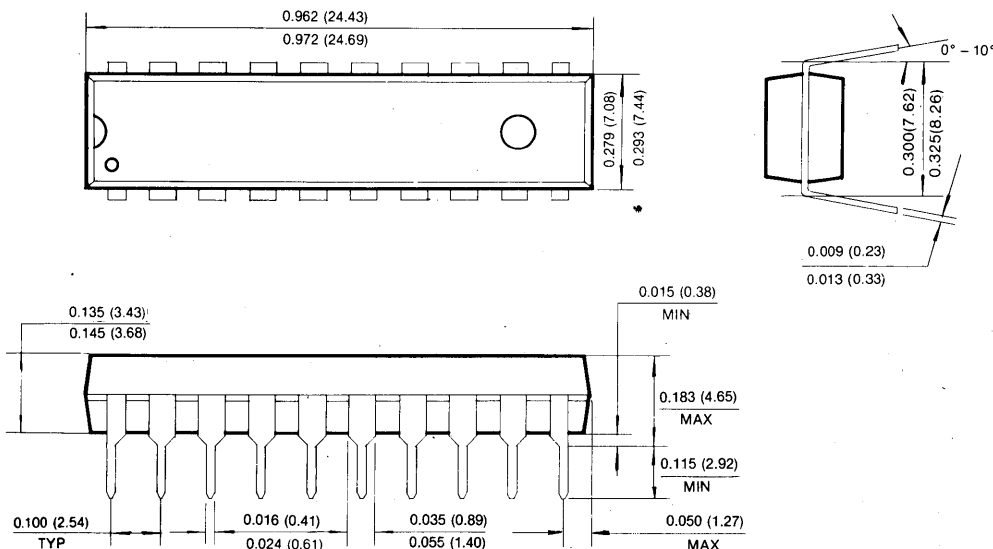
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C256C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C256C/CL/CSL and they supply much of the current used by the KM44C256C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

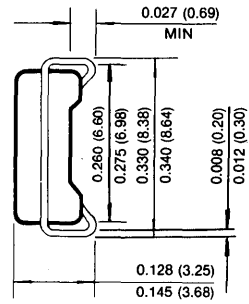
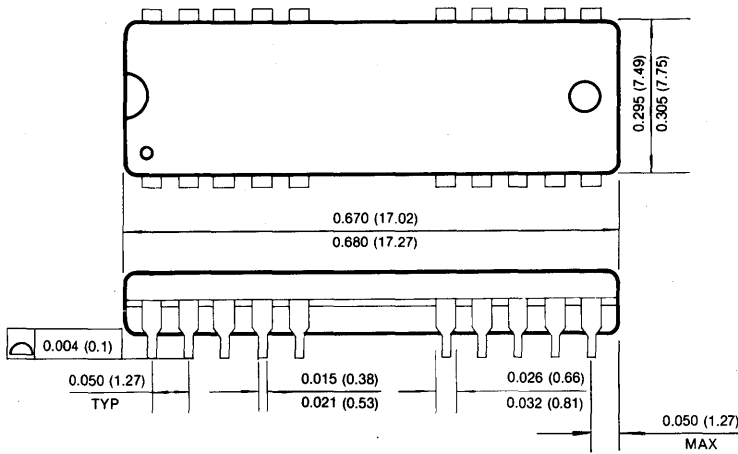
Units: Inches (Millimeters)



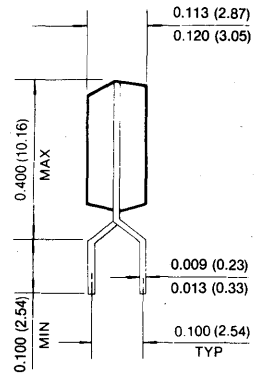
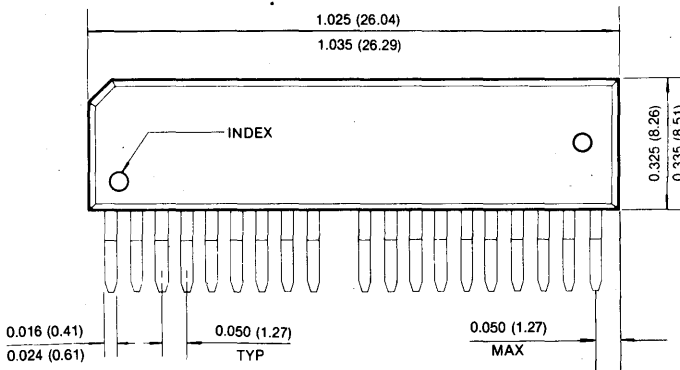
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

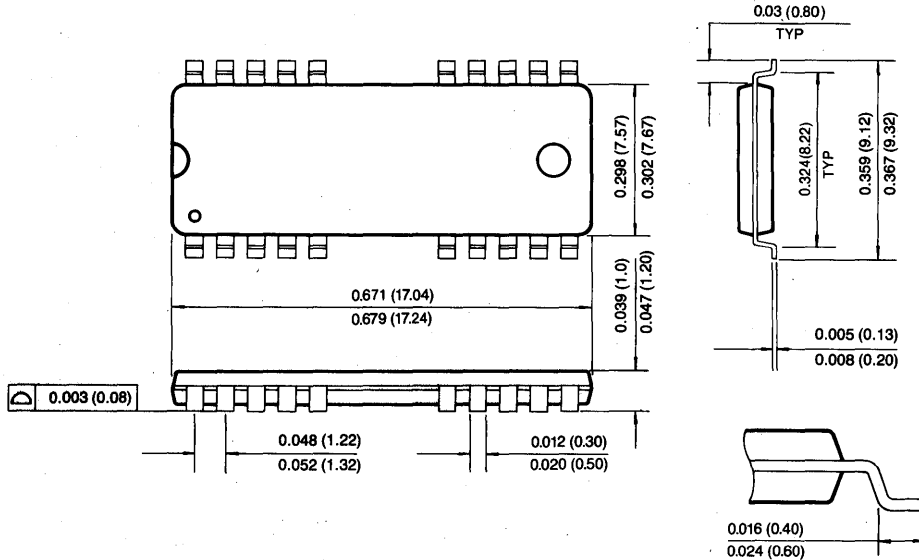


2

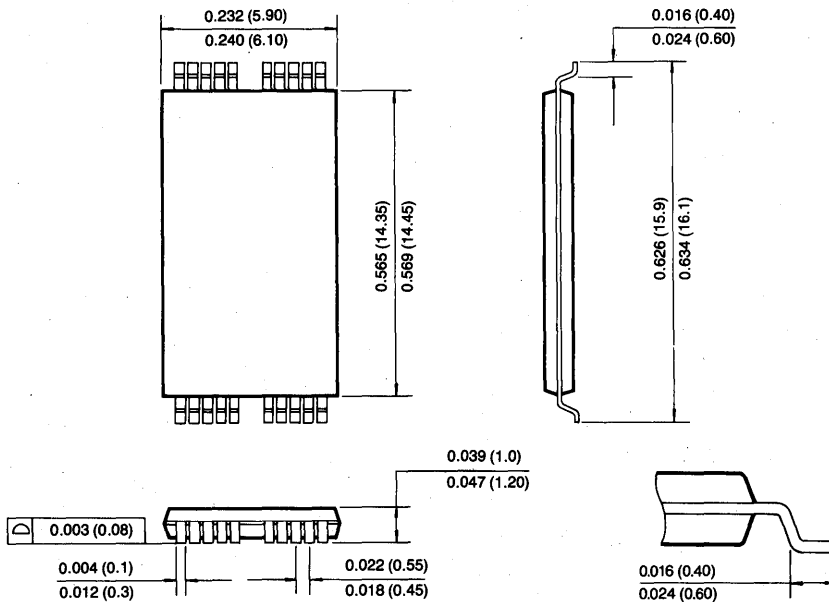
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)

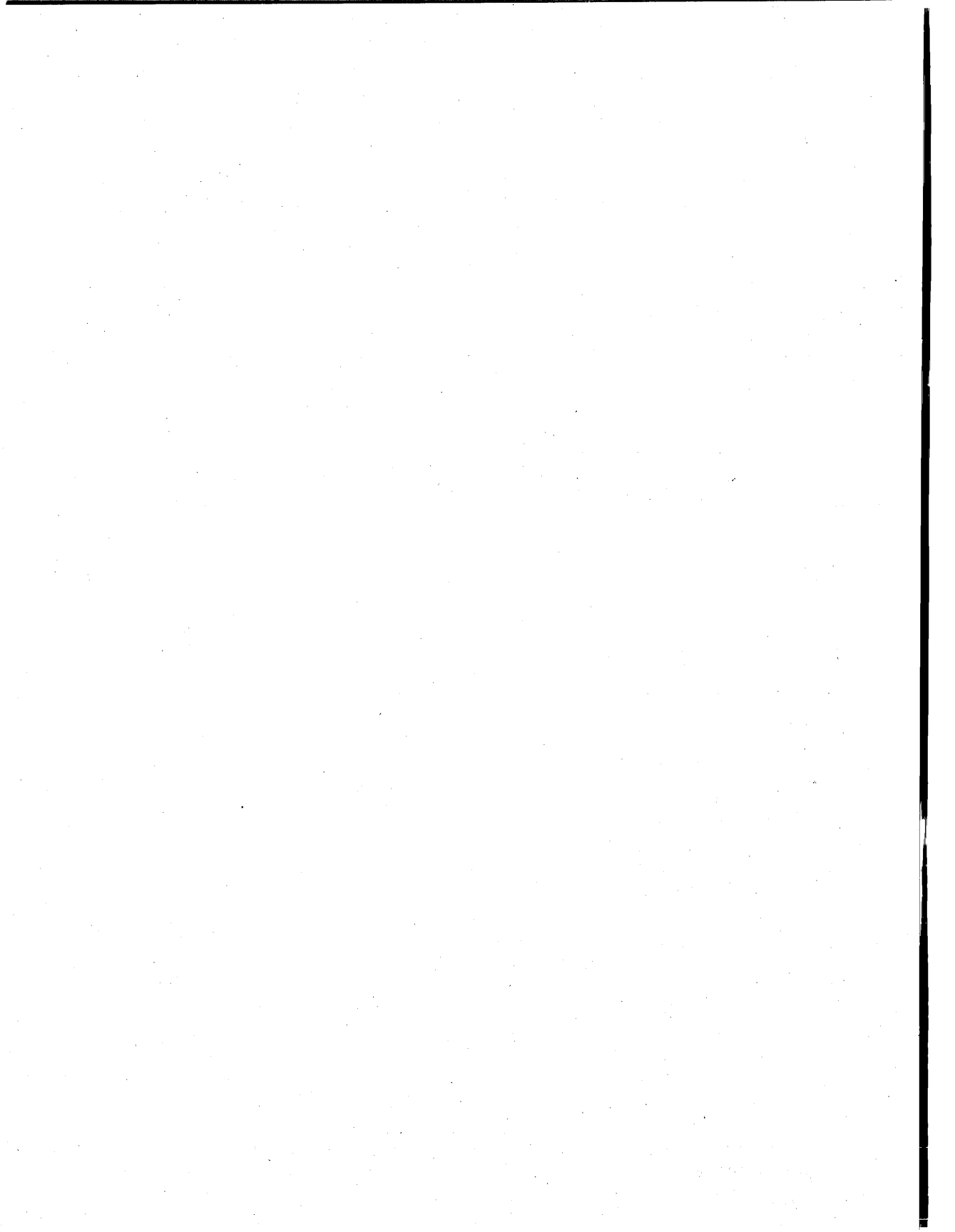


20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



A black and white photograph of a person wearing a full-body white protective suit, including a hood and gloves. The person is standing in a server room, with their right hand touching a dark server cabinet. The room has a dark, perforated floor and a ceiling with a grid of lights. A small, dark, horn-shaped object is mounted on the wall above the person. The overall scene suggests a high-security or cleanroom environment.

4M DRAM DATA SHEET 3



4M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM41C4000C/CL/CSL-5	50ns	13ns	90ns
KM41C4000C/CL/CSL-6	60ns	15ns	110ns
KM41C4000C/CL/CSL-7	70ns	20ns	130ns
KM41C4000C/CL/CSL-8	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and output
- Common I/O using early write
- Single + 5V ± 10% power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/256ms (SL-version)
- Power dissipation
 - Standby : 5.5mW(Normal)
1.1mW(L-version)
0.55mW(SL-version)
 - Active (50/60/70/80): 470/415/360/305mW
- JEDEC standard pinout
- Available in plastic SOJ, ZIP and TSOP-II packages

GENERAL DESCRIPTION

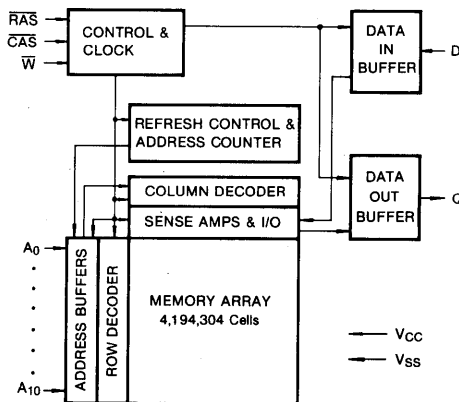
The Samsung KM41C4000C/CL/CSL is a high speed CMOS 4,194,304 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41C4000C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only Refresh. All inputs and output are fully TTL compatible.

The KM41C4000C/CL/CSL is fabricated using Samsung's advanced CMOS process.

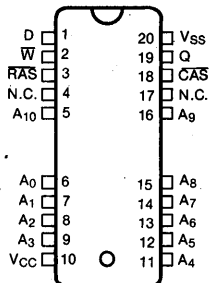
3

FUNCTIONAL BLOCK DIAGRAM

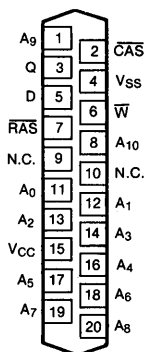


PIN CONFIGURATION (Top Views)

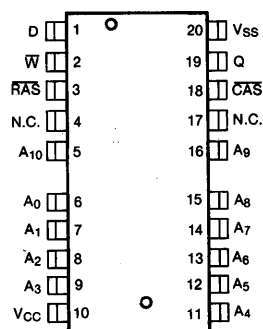
• KM41C4000CJ/CLJ/CSLJ



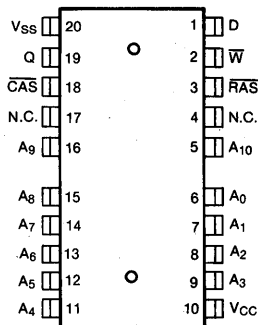
• KM41C4000CZ/CLZ/CSLZ



• KM41C4000CT/CLT/CSLT



• KM41C4000CTR/CLTR/CSLTR



Pin Names	Pin Function
A ₀ -A ₁₀	Address Inputs
D	Data In
Q	Data Out
\bar{W}	Read/Write Input
\bar{RAS}	Row Address Strobe
\bar{CAS}	Column Address Strobe
V _{CC}	Power (+5V)
V _{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS, CAS, Address Cycling @trc=min.)	KM41C4000C/CL/CSL-5	-	85	mA	
	KM41C4000C/CL/CSL-6	-	75	mA	
	KM41C4000C/CL/CSL-7	-	65	mA	
	KM41C4000C/CL/CSL-8	-	55	mA	
Standby Current (RAS=CAS=W=V _{IH})	I _{CC2}	-	2	mA	
RAS-Only Refresh Current* (CAS=V _{IH} , RAS, Cycling @trc=min.)	KM41C4000C/CL/CSL-5	-	85	mA	
	KM41C4000C/CL/CSL-6	-	75	mA	
	KM41C4000C/CL/CSL-7	-	65	mA	
	KM41C4000C/CL/CSL-8	-	55	mA	
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tPC=min.)	KM41C4000C/CL/CSL-5	-	65	mA	
	KM41C4000C/CL/CSL-6	-	55	mA	
	KM41C4000C/CL/CSL-7	-	45	mA	
	KM41C4000C/CL/CSL-8	-	35	mA	
Standby Current (RAS=CAS=W=V _{CC} -0.2V)	KM41C4000C	-	1	mA	
	KM41C4000CL	-	200	μA	
	KM41C4000CSL	-	100	μA	
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM41C4000C/CL/CSL-5	-	85	mA	
	KM41C4000C/CL/CSL-6	-	75	mA	
	KM41C4000C/CL/CSL-7	-	65	mA	
	KM41C4000C/CL/CSL-8	-	55	mA	
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V CAS=CAS-Before-RAS Cycling or 0.2V DIN=Don't Care TRC=125(L-ver.)μS TRC=250(SL-ver.)μS TRAS=TRAS min~300ns	KM41C4000CL KM41C4000CSL	I _{CC7}	-	300	μA
			-	150	μA



DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.5V$ all other pins not under test=0 volts.)	$I_{i(L)}$	-10*	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{o(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)	V_{OL}	-	0.4	V

* Note: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1} , I_{CC3} , I_{CC6} . Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. I_{CC4} . Address can be changed maximum once during a Fast Page Mode Cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{CC} = 5V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	—	5	pF
Input Capacitance ($A_0 - A_{10}$)	C_{IN2}	—	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , W)	C_{IN3}	—	7	pF
Output Capacitance (Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{CC} = 5.0 \pm 10\%$, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	108		130		155		175		ns	
Access time from \overline{RAS}	trac		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	trp	30		40		50		60		ns	
\overline{RAS} pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	trSH	13		15		20		20		ns	
\overline{CAS} hold time	tcSH	50		60		70		80		ns	
\overline{CAS} pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	trCD	20	35	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tcRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	trAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	13		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (Low power)	tREF		128		128		128		128	ms	
Refresh period (Super low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	13		15		20		20		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	50		60		70		80		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	25		30		35		40		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tcPT	20		20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		30		35		40		45	ns	3
Fast page mode cycle time	tpc	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tpRWC	53		60		70		75		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page Mode)	trASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	tcp	10		10		10		10		ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	30		35		40		45		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ cycle)	tWRP	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ cycle)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	95		115		135		135		ns	
Read-modify-write cycle time	t _{RWC}	113		135		160		180		ns	
Access time from RAS	t _{RAC}		55		65		75		85	ns	3,4,11
Access time from CAS	t _{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t _{AA}		30		35		40		45	ns	3,11
RAS pulse width	t _{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
CAS pulse width	t _{CAS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	t _{RSH}	18		20		25		25		ns	
CAS hold time	t _{CSH}	55		65		75		85		ns	
Column address to RAS lead time	t _{RAL}	30		35		40		45		ns	
CAS to write enable delay	t _{CWD}	18		20		25		25		ns	8
RAS to write enable delay	t _{RWD}	55		65		75		85		ns	8
Column address to \bar{W} delay time	t _{AWD}	30		35		40		45		ns	8
Fast mode cycle time	t _{PC}	40		45		50		55		ns	
Fast page mode read-modify-write	t _{PRWC}	58		65		75		80		ns	
RAS pulse width(Fast page mode)	t _{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	t _{CPA}		35		40		45		50	ns	3

NOTES

1. An initial pause of 200μs is required after power up followed by any 8 CAS-before-RAS or RAS-only Refresh cycles before proper device operation is achieved.
2. V_{IH(min)} and V_{IL(max)} are reference levels for measuring timing of input signals. Transition times are measured between V_{IH(min)} and V_{IL(max)} and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD(max)} limit insures that t_{RAC(max)} can be met. t_{RCD(max)} is specified as a reference point only. If t_{RCD(max)} is greater than the specified t_{RCD(max)} limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RCD} ≥ t_{RCD(max)}.
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD(max)}.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS(min)}

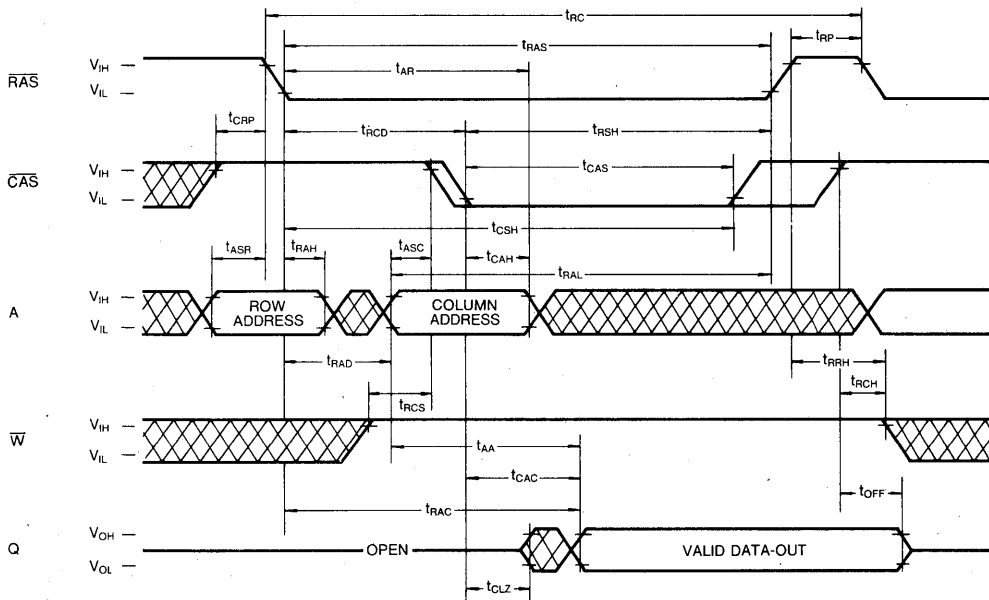
the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If t_{CWD} ≥ t_{CWD(min)} and t_{RWD} ≥ t_{RWD(min)} and t_{AWD} ≥ t_{AWD(min)}, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.

9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\bar{C}AS$ leading edge in early write cycles and to the \bar{W} leading edge in read-modify-write cycles.
11. Operation within the t_{RAD(max)} limit insures that t_{RAC(max)} can be met. t_{RAD(max)} is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD(max)} limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{OFF(max)} and t_{OEZ(max)} define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.

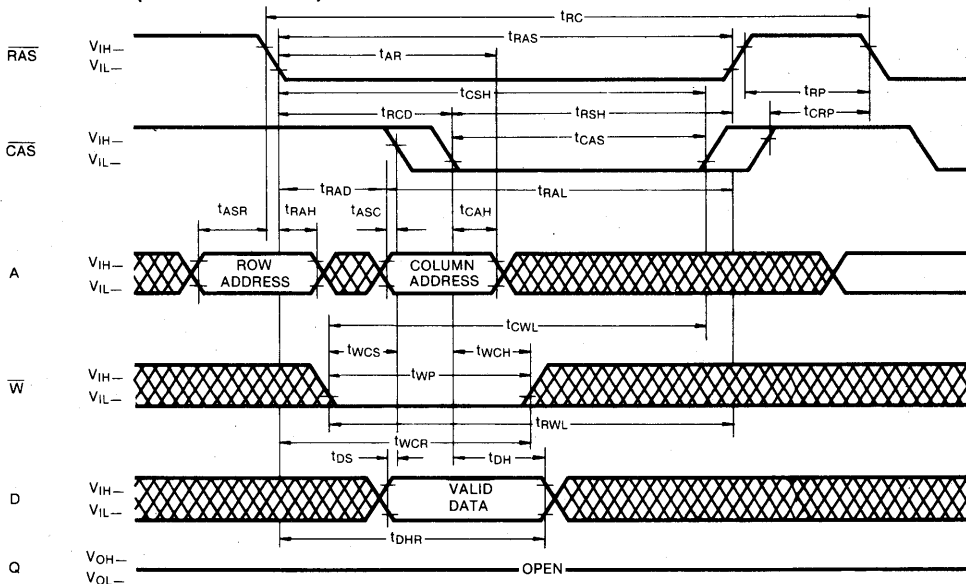


TIMING DIAGRAMS

READ CYCLE



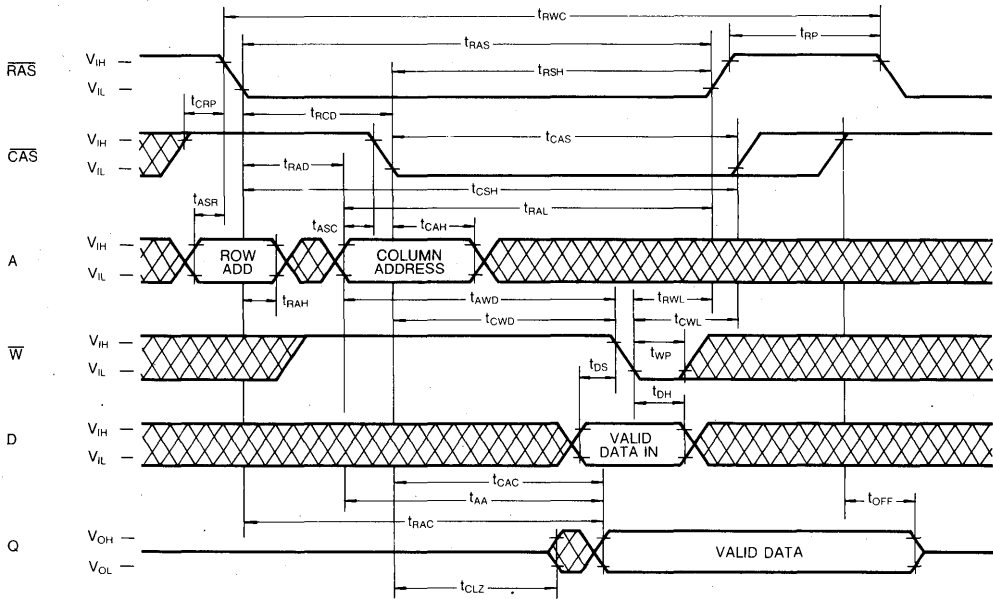
WRITE CYCLE (EARLY WRITE)



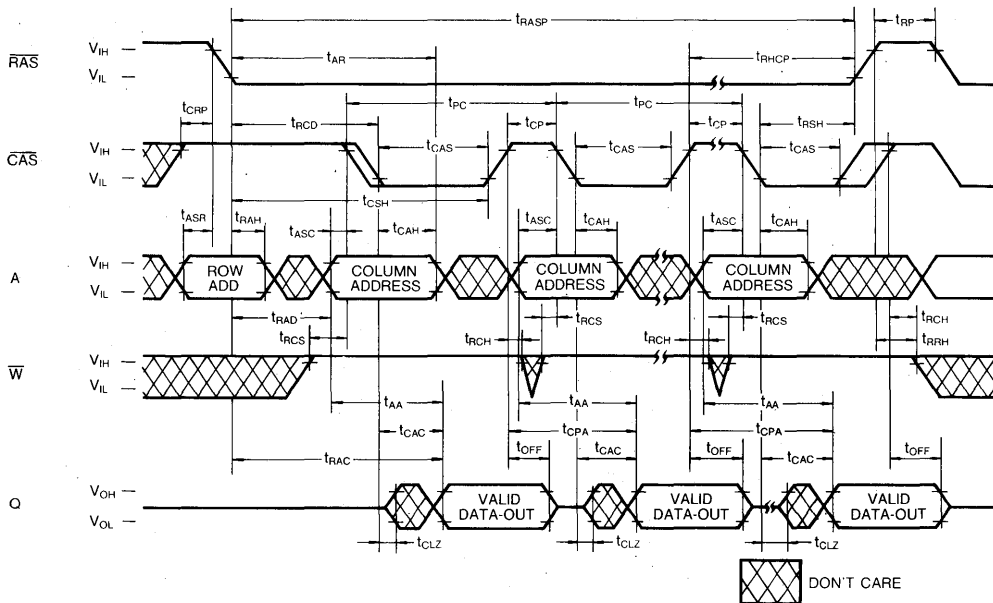
⊗ DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

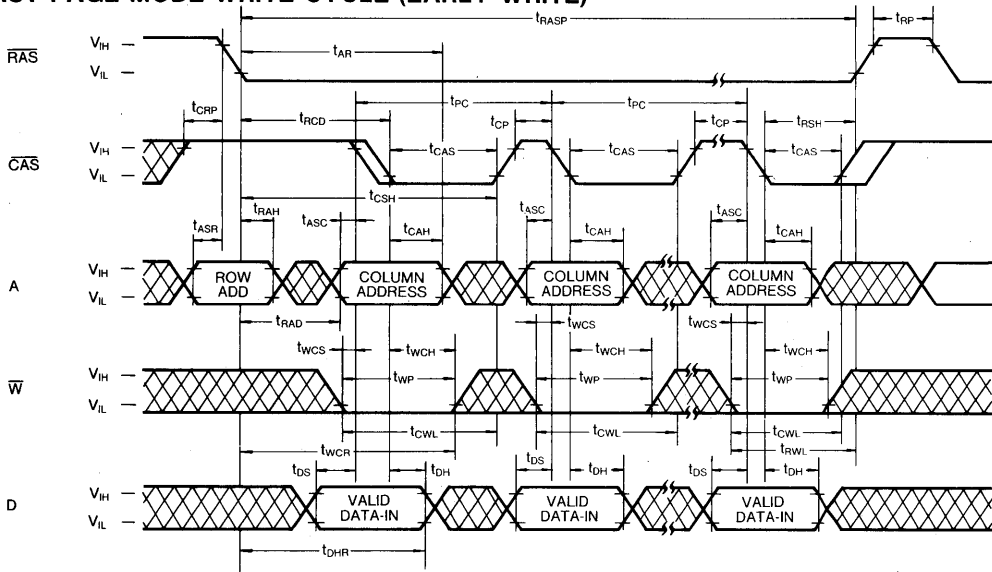


FAST PAGE MODE READ CYCLE

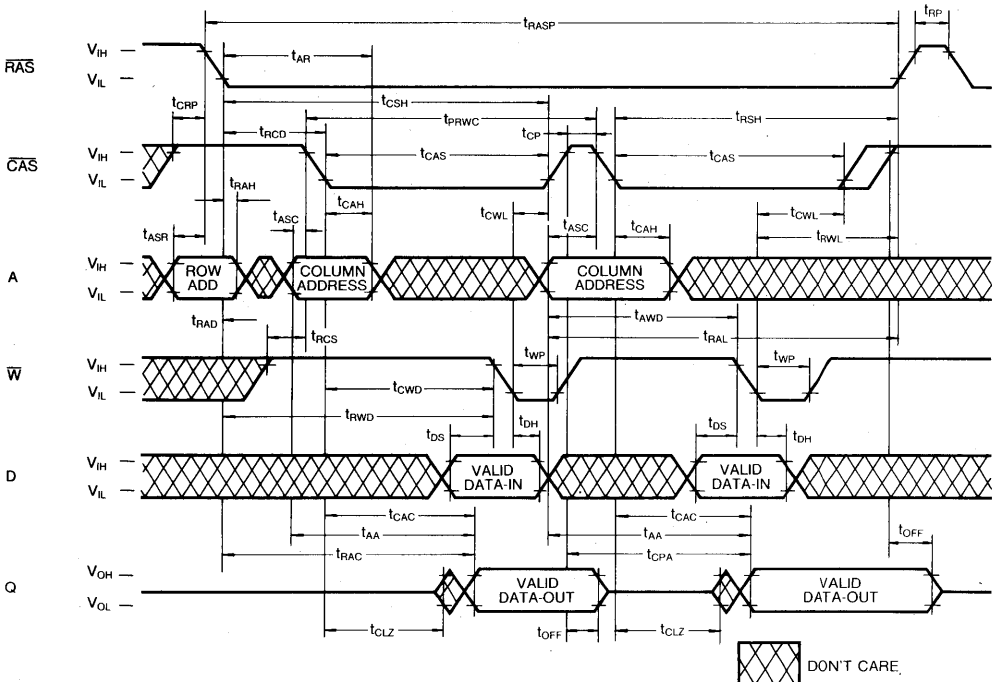


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-WRITE CYCLE

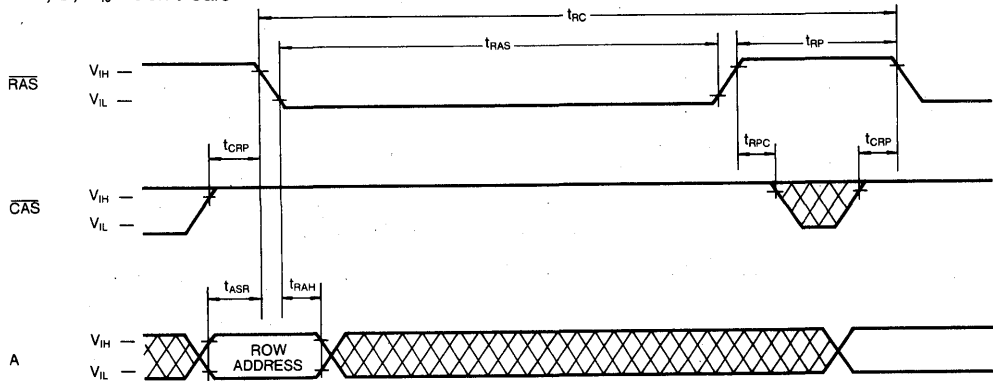


3

TIMING DIAGRAMS (Continued)

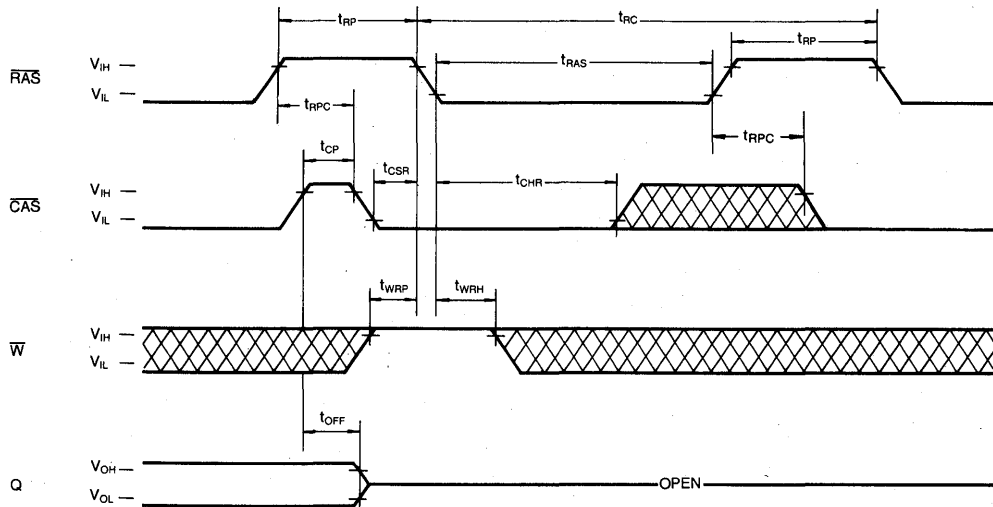
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , D, A_{10} = Don't Care



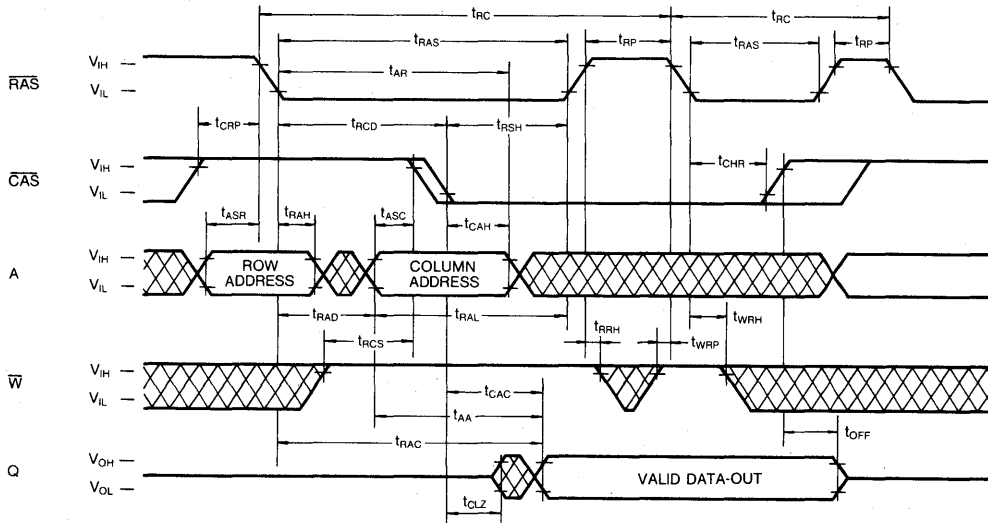
CAS-BEFORE-RAS REFRESH CYCLE

Note: Address = Don't Care

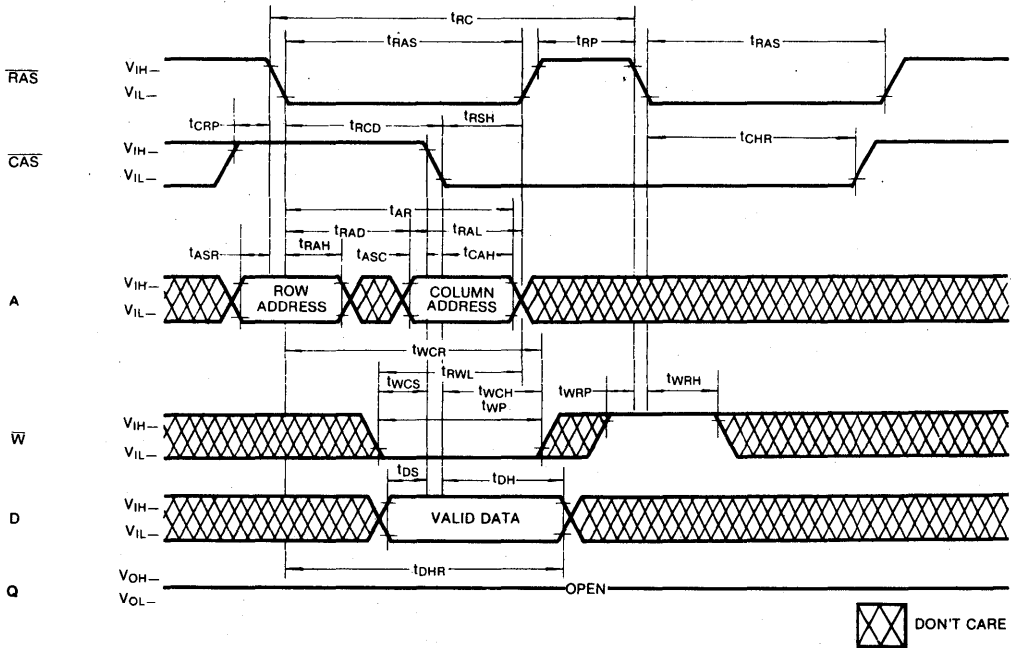


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



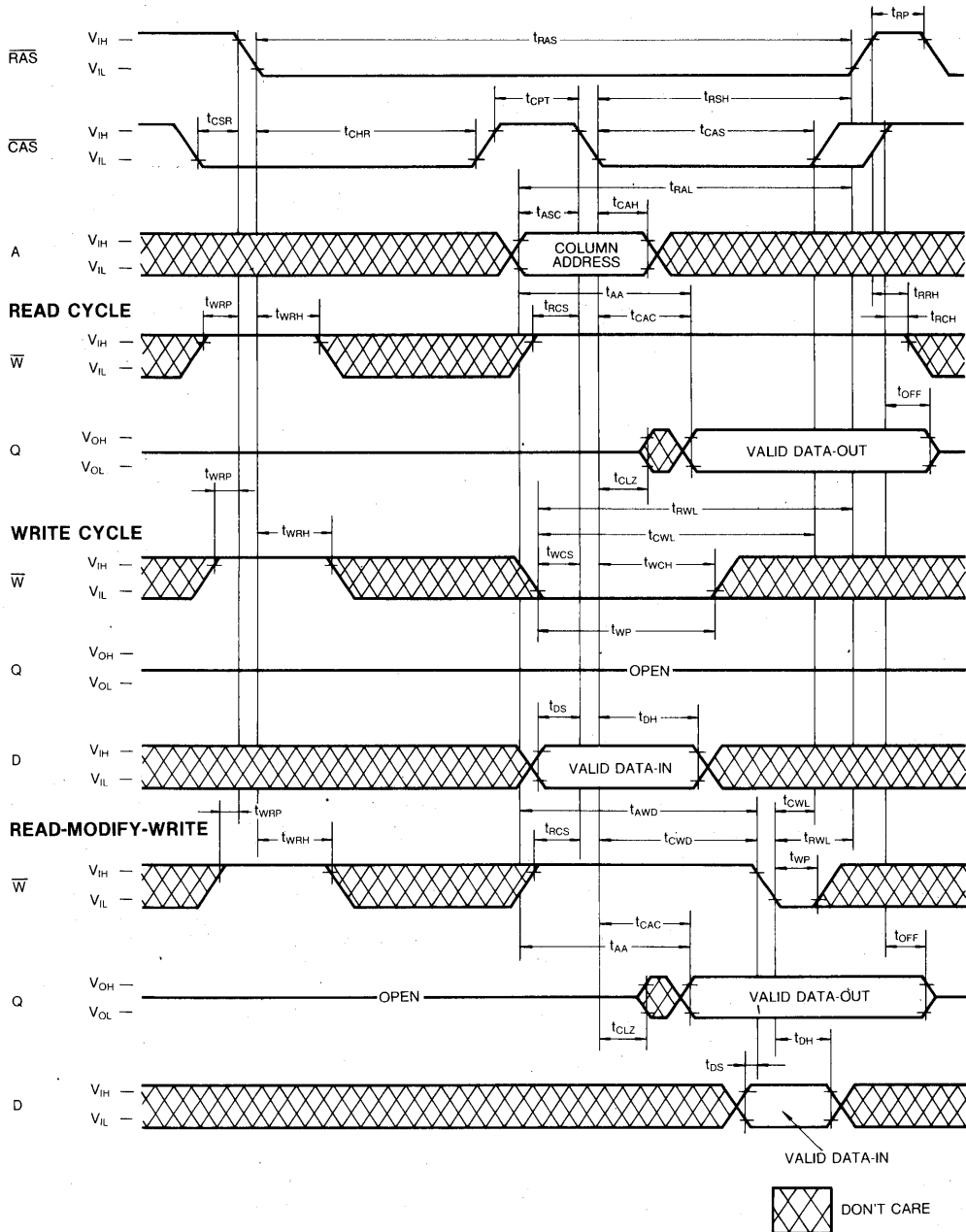
HIDDEN REFRESH CYCLE (WRITE)



3

TIMING DIAGRAMS (Continued)

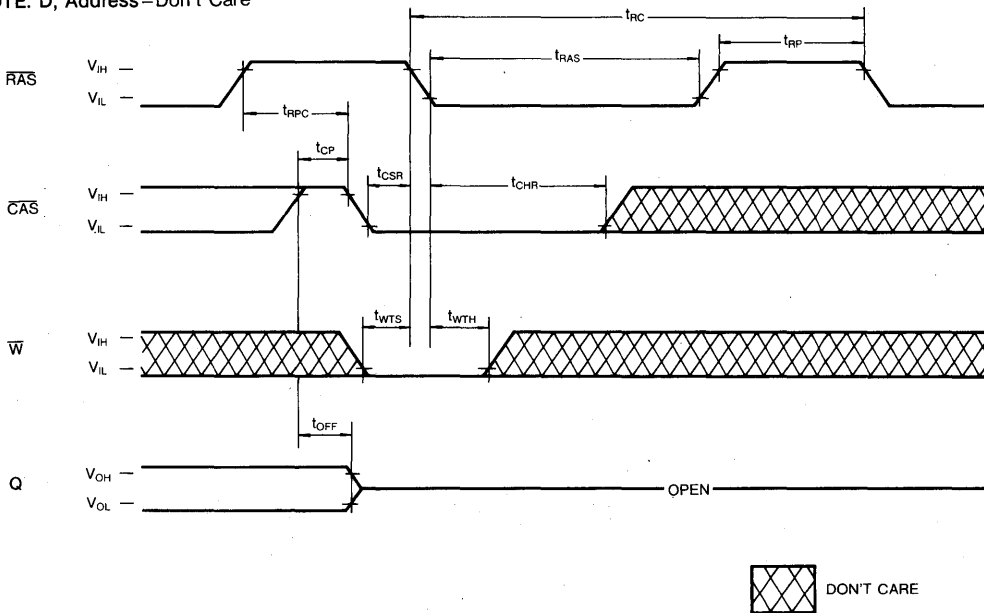
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



3

TEST MODE DESCRIPTION

The KM41C4000C/CL/CSL is the RAM organized 4, 194,304 words by 1 bit it is internally organized 524, 288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A₀ and A₁₀ are not used. If, upon reading, all bits are equal (all "1" or "0"s) the Q pin indicates a "1". If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. W, CAS-BEFORE-RAS Cycle (Test Mode in Cycle) puts the device into "Test Mode", And "CAS-BEFORE-RAS REFRESH CYCLE" or "RAS-only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time(1/8 in cases of N test pattern.)

DEVICE OPERATION

Device Operation

The KM41C4000C/CL/CSL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4000C/CL/CSL has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column address. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}), and the valid row and column address inputs.

Operating of the KM41C4000C/CL/CSL begins by strobing in valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM41C4000C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4000C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during a $\overline{RAS}/\overline{CAS}$ cycle. If \overline{CAS} goes low before $t_{RCD(max)}$ the access time to valid data is specified by t_{RAC} . If \overline{CAS} goes low after $t_{RCD(max)}$, the access time is measured from \overline{CAS} and is specified by t_{CAC} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to bring \overline{CAS} low before $t_{RCD(max)}$.

Write

The KM41C4000C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} and \overline{CAS} . In any type of write cycle, Data-in must be valid at

or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention

Late Write: If \overline{W} is brought low after \overline{CAS} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} , t_{CWD} and t_{LWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4000C/CL/CSL has three-state output buffer which are controlled by \overline{CAS} . Whenever \overline{CAS} is high (V_{IH}), the outputs is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data the output until \overline{CAS} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM41C4000C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, \overline{RAS} -only Refresh, Fast Page Mode Write, \overline{CAS} -before- \overline{RAS} Refresh, \overline{CAS} -only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4000C/CL/CSL is stored on a

DEVICE OPERATION (Continued)

tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256 ms. There several ways to accomplish this.

\overline{RAS} -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with \overline{RAS} while \overline{CAS} remains high. This cycle must be repeated for each row.

\overline{CAS} -before- \overline{RAS} Refresh: The KM41C4000C/CL/CSL has \overline{CAS} -before- \overline{RAS} on-chip refresh capability that eliminates the need for external refresh addresses. If \overline{CAS} input is held low for the specified set up time (tcsr) before \overline{RAS} goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next \overline{CAS} -before- \overline{RAS} refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the \overline{CAS} active time and cycling \overline{RAS} . The KM41C4000C/CL/CSL hidden refresh cycle is actually a \overline{CAS} -before- \overline{RAS} refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4000C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh is the preferred method.

Fast Page Mode

The KM41C4000C/CL/CSL has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. Then, while \overline{RAS} is kept low to maintain the \overline{CAS} is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

 \overline{CAS} -before- \overline{RAS} Refresh Counter Test Cycle

A special timing sequence using the \overline{CAS} -before- \overline{RAS} counter test cycle provides a convenient method of verifying the functionality of the \overline{CAS} -before- \overline{RAS} refresh activated circuitry.

After the \overline{CAS} -before- \overline{RAS} refresh operation, is \overline{CAS} goes high and then low again while \overline{RAS} is held low, the read and write operations are enabled.

This is shown in the \overline{CAS} -before- \overline{RAS} counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows

Row Address- Bits A₀ through A₉ are supplied by the on-chip refresh counter. This A₁₀ bit is set high internally.

Column Address-Bits A₀ through A₁₀ are strobed -in by the falling edge of \overline{CAS} as in a normal memory cycle.

Suggested \overline{CAS} -before- \overline{RAS} Counter Test Procedure

The \overline{CAS} -before- \overline{RAS} refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 \overline{CAS} -before- \overline{RAS} cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address (The row addresses are supplied by the on-chip refresh counter)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If \overline{RAS} =V_{ss} during power-up, the KM41C4000C/CL/CSL could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that \overline{RAS} and \overline{CAS} track with V_{cc} during power-up or be held a valid V_{ih} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by any 8 \overline{RAS} cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L-version:128, SL-version:256) msec period in which there are no \overline{RAS} cycles. An

DEVICE OPERATION (Continued)

initialization cycle in which RAS is cycled.

Termination

The lines from the TTL driver circuits to the KM41C4000C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws on additional power. It consists of a resistor in series with the input line placed close to the KM41C4000C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each inter

section or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV

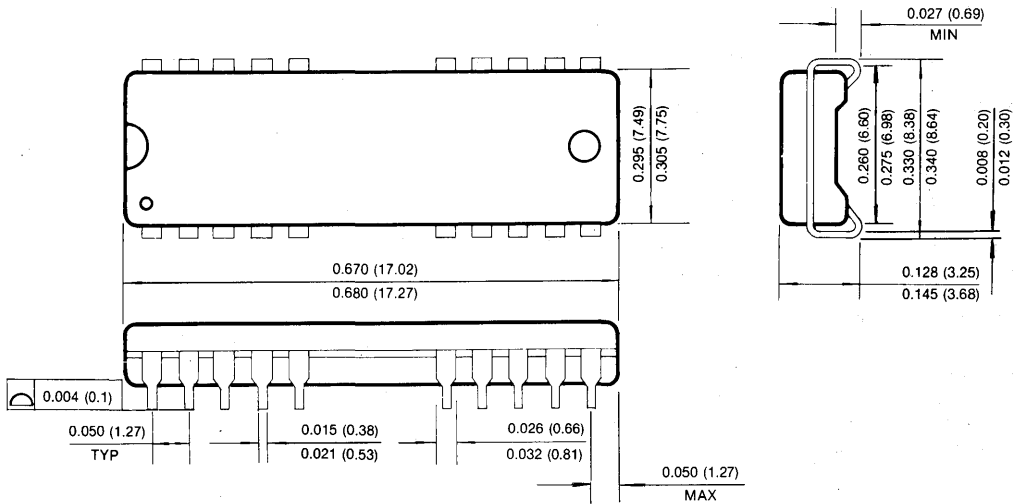
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41C4000C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C4000C/CL/CSL and they supply much of the current used by the KM41C4000C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

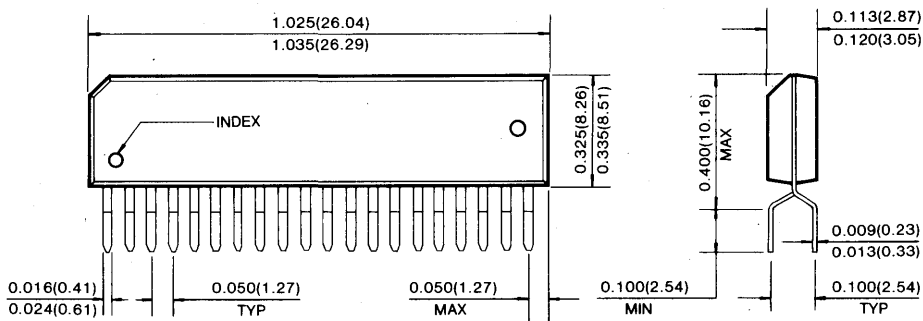
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

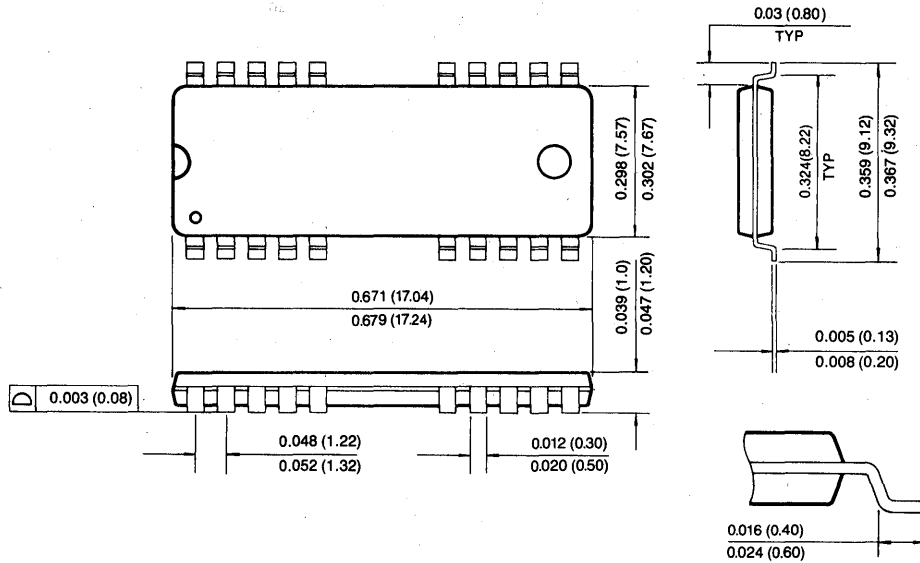


3

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



4M × 1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• **Performance range:**

	trAC	tcAC	trC
KM41C4002C-5	50ns	13ns	90ns
KM41C4002C-6	60ns	15ns	110ns
KM41C4002C-7	70ns	20ns	130ns
KM41C4002C-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **\overline{CS} -before- \overline{RAS} refresh capability**
- **\overline{RAS} -only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Common I/O using Early Write**
- **Single +5.0V ± 10% power supply**
- **1024 cycles/16ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ, ZIP and TSOP(II) Packages**

GENERAL DESCRIPTION

The Samsung KM41C4002C is a CMOS high speed 4, 194,304 × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

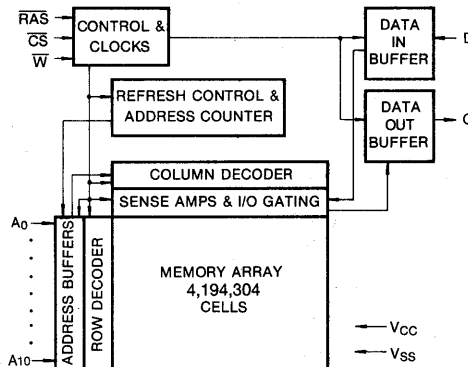
The KM41C4002C features Static Column Mode operation which allows high speed random or Sequential access within a row. Static Column Mode operation offers high performance while relaxing many critical system timing requirements for fast usable speed.

\overline{CS} -before- \overline{RAS} refresh capability provides on-chip auto refresh as an alternative to \overline{RAS} -only refresh. All inputs and output are fully TTL compatible.

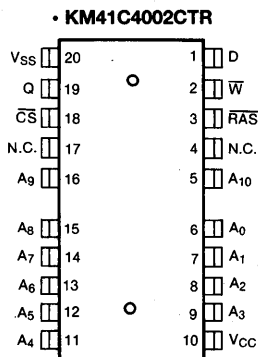
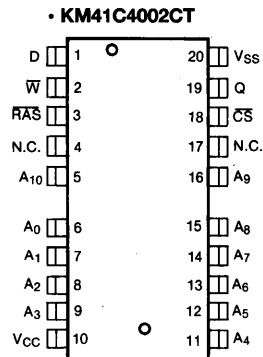
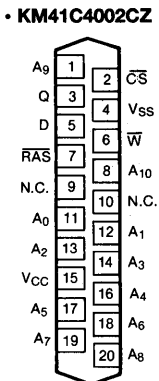
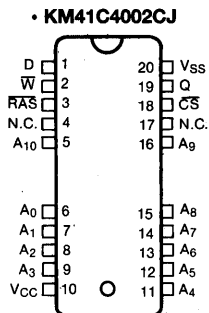
The KM41C4002C is fabricated using Samsung's advanced CMOS process.

3

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Names	Pin Function
A ₀ -A ₁₀	Address Inputs
D	Data In
Q	Data Out
\bar{W}	Read/Write Input
\overline{RAS}	Row Address Strobe
\overline{CS}	Chip Select Input
V _{CC}	Power (+5V)
V _{SS}	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CS Cycling @trc=min.)	KM41C4002C-5	-	85	mA
	KM41C4002C-6	-	75	mA
	KM41C4002C-7	-	65	mA
	KM41C4002C-8	-	55	mA
Standby Current (RAS=CS=W=V _{IH})	I _{CC2}	-	2	mA
RAS-Only Refresh Current* (CS=V _{IH} , RAS, Address Cycling @trc=min.)	KM41C4002C-5	-	85	mA
	KM41C4002C-6	-	75	mA
	KM41C4002C-7	-	65	mA
	KM41C4002C-8	-	55	mA
Static Column Mode Current* (RAS=CS=V _{IL} , Address Cycling @trc=min.)	KM41C4002C-5	-	65	mA
	KM41C4002C-6	-	55	mA
	KM41C4002C-7	-	45	mA
	KM41C4002C-8	-	35	mA
Standby Current (RAS=CS=W=V _{CC} -0.2V)	I _{CC5}	-	1	mA
CS-Before-RAS Refresh Current* (RAS and CS Cycling @trc=min.)	KM41C4002C-5	-	85	mA
	KM41C4002C-6	-	75	mA
	KM41C4002C-7	-	65	mA
	KM41C4002C-8	-	55	mA
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{CC} +0.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, Address can be changed maximum once during a Static Column mode cycle.

CAPACITANCE ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$, $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(D)	C _{IN1}	-	5	pF
Input Capacitance (A0-A10)	C _{IN2}	-	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CS}}$, $\overline{\text{W}}$)	C _{IN3}	-	7	pF
Input Capacitance (Q)	C _{OUT}	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CC}=5.0\text{V} \pm 10\%$, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	108		130		150		170		ns	
Static column mode cycle time	t _{SC}	30		35		40		45		ns	
Static column mode read-write cycle time	t _{SRWC}	53		65		75		85		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60		70		80	ns	3,4,11
Access time from $\overline{\text{CS}}$	t _{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35		40	ns	3,11
Access time from last write	t _{ALW}		50		55		65		75	ns	3
$\overline{\text{CS}}$ to output in Low-Z	t _{CLZ}	0		0		0		0		ns	7
Output buffer turn-off delay	t _{OFF}	0	13	0	15	0	20	0	20	ns	2
Output data hold time from column address	t _{AOH}	5		5		5		5		ns	
Output data enable time from $\overline{\text{W}}$	t _{OW}		35		40		45		55	ns	
Output data hold time from $\overline{\text{W}}$	t _{WOH}	0		0		0		0		ns	
Transition time (rise and fall)	t _T	3	50	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ pulse width(static column mode)	t _{RASC}	50	100,000	60	100,000	70	100,000	80	100,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	13		15		20		20		ns	
$\overline{\text{CS}}$ hold time	t _{CSH}	50		60		70		80		ns	
$\overline{\text{CS}}$ pulse width	t _{CS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{CS}}$ pulse width (static column mode)	t _{CSC}	13	100,000	15	100,000	20	100,000	20	100,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ delay time	t _{RCD}	20	37	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	15	35	15	40	ns	11
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		5		5		ns	
$\overline{\text{CS}}$ precharge time (static column mode)	t _{CP}	10		10		10		10		ns	
Row address set-up time	t _{ASR}	0		0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		0		ns	
Column address hold	t _{CAH}	10		10		15		15		ns	
Write address hold time referenced to $\overline{\text{RAS}}$	t _{AWR}	40		45		55		60		ns	6

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address hold time referenced to \overline{RAS}	tAR	60		70		80		90		ns	
Column address to \overline{RAS} lead time	tRAL	25		30		35		40		ns	
Column address hold time referenced to \overline{RAS} rise,	tAH	5		5		5		5		ns	
Last Write to column address to delay time	tLWAD	20	25	20	30	20	35	20	40	ns	12
Last write to column address gold time	tAHLW	50		55		65		75		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to \overline{CS}	tRCH	0		0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to \overline{RAS}	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command inactive time	tWI	10		10		10		10		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		15		15		ns	
Write command to \overline{CS} lead time	tCWL	13		15		15		15		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to \overline{RAS}	tDHR	40		45		55		60		ns	6
Refresh period (1024 cycles)	tREF		16		16		16		16	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
\overline{CS} to \overline{W} delay time	tCWD	13		15		15		15		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	50		60		70		80		ns	8
Column address to \overline{W} delay time	tAWD	25		30		35		40		ns	8
\overline{CS} setup time (\overline{CS} -before- \overline{RAS} refresh)	tCSR	10		10		10		10		ns	
\overline{CS} hold time (\overline{CS} -before- \overline{RAS} refresh)	tCHR	10		10		10		10		ns	
Write command set-up time (test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{CS} -before- \overline{RAS} cycle)	tWRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{CS} -before- \overline{RAS} cycle)	tWRH	10		10		10		10		ns	
\overline{RAS} precharge to \overline{CS} hold time	tRPC	5		5		5		5		ns	
Refresh counter test \overline{CS} precharge time	tCPT	20		20		25		30		ns	

3

TEST MODE CYCLE

(Note.13)

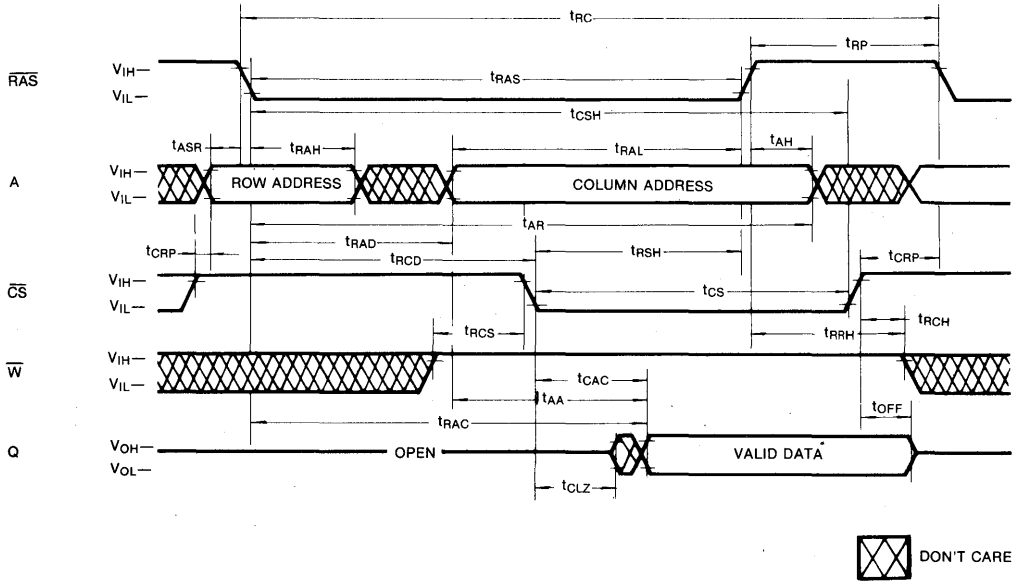
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t _{RWC}	113		135		155		175		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{\text{CS}}$	t _{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t _{AA}		30		35		40		45	ns	3,11
$\overline{\text{RAS}}$ pulse width	t _{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{\text{CS}}$ pulse width	t _{CS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	18		20		25		25		ns	
$\overline{\text{CS}}$ hold time	t _{CSH}	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		40		45		ns	
$\overline{\text{CS}}$ to Write enable delay	t _{CWD}	18		20		20		20		ns	8
$\overline{\text{RAS}}$ to Write enable delay	t _{RWD}	55		65		75		85		ns	8
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	30		35		40		45		ns	8
Static column mode cycle time	t _{SC}	35		40		45		50		ns	
Static column mode read-modify-write	t _{SRWC}	58		70		80		90		ns	
$\overline{\text{RAS}}$ pulse width (Static column mode)	t _{RASC}	55	100,000	65	100,000	75	100,000	85	100,000	ns	
Access time from last write	t _{ALW}		55		65		75		85	ns	3,12
$\overline{\text{CS}}$ pulse width (static column mode)	t _{CSC}	18	100,000	20	100,000	25	100,000	25	100,000	ns	

NOTES

- An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{CBR}}$ or $\overline{\text{ROR}}$ cycles before proper device operation is achieved.
- V_{IH(min)} and V_{IL(max)} are reference levels for measuring timing of input signals. Transition times are measured between V_{IH(min)} and V_{IL(max)}, and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF
- Operation within the t_{RCD(max)} limit insures that t_{RAC(max)} can be met. t_{RCD(max)} is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD(max)} limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{RCD} > t_{RCD(max)}.
- t_{AWR}, t_{WCR}, t_{DHR} are referenced to t_{RAD(max)}
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} > t_{WCS(min)} the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If t_{CWD} > t_{CWD(min)} and t_{RWD} > t_{RWD(min)} and t_{AWD} > t_{AWD(min)}, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
- Operation within the t_{RAD(max)} limit insures that t_{RAC(max)} can be met. t_{RAD(max)} is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD(max)} limit, then access time is controlled by t_{AA}.
- Operation within the t_{LWAD(max)} limit insures that t_{ALW(max)} can be met. t_{LWAD(max)} is specified as a reference point only. t_{LWAD} is greater than the specified t_{LWAD(max)} limit, then access time is controlled by t_{AA}.
- These specifications are applied in the test mode.

TIMING DIAGRAMS

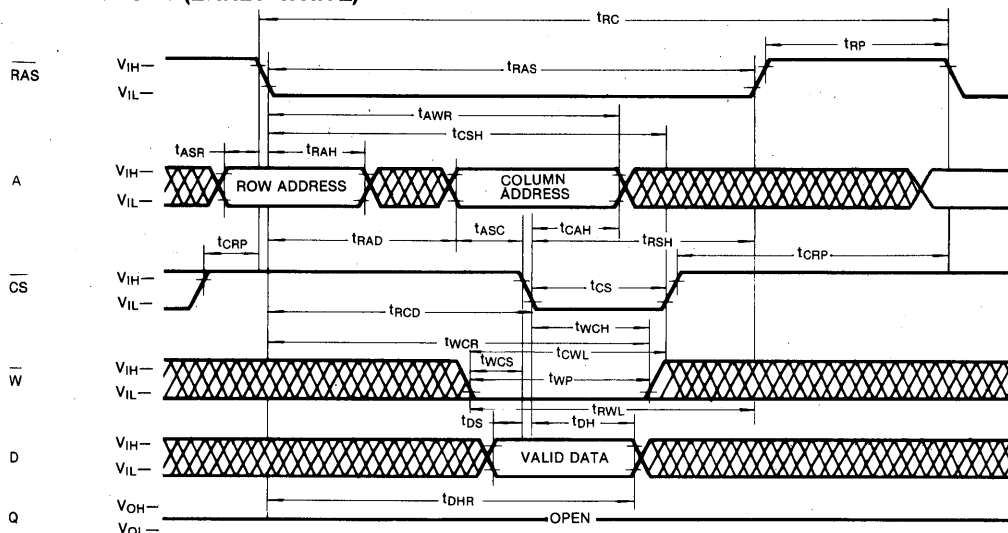
READ CYCLE



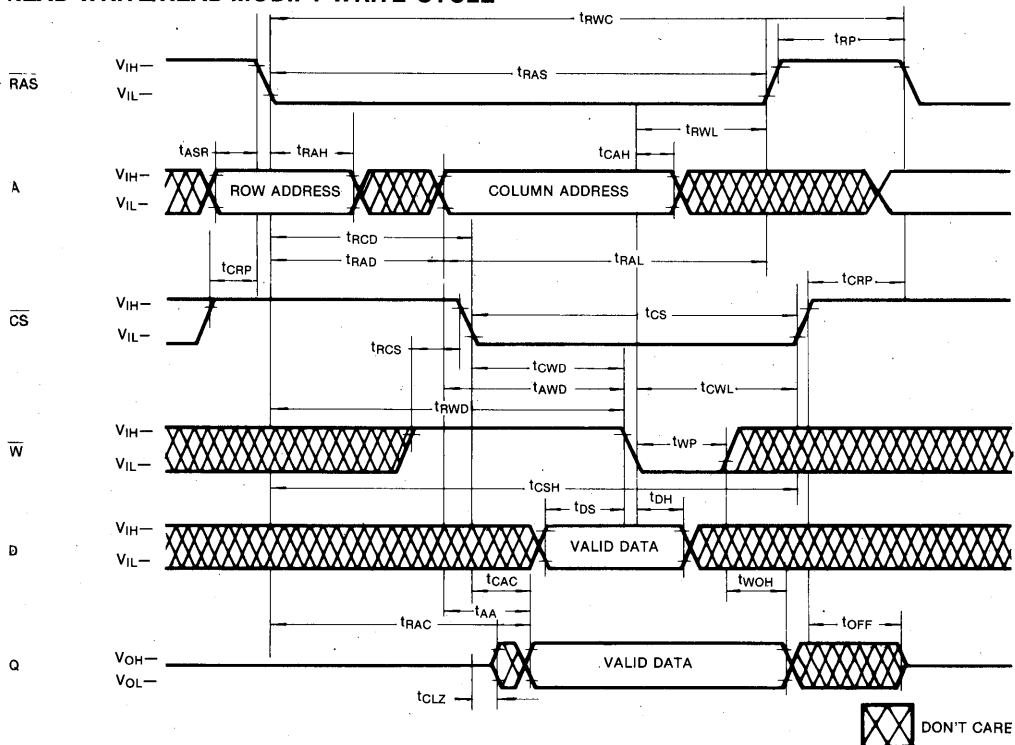
3

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



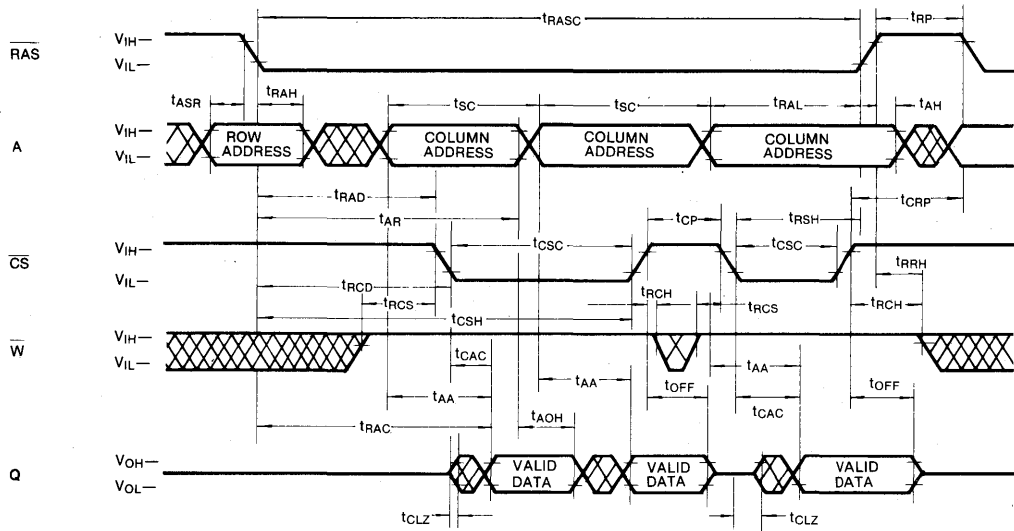
READ-WRITE/READ-MODIFY-WRITE CYCLE



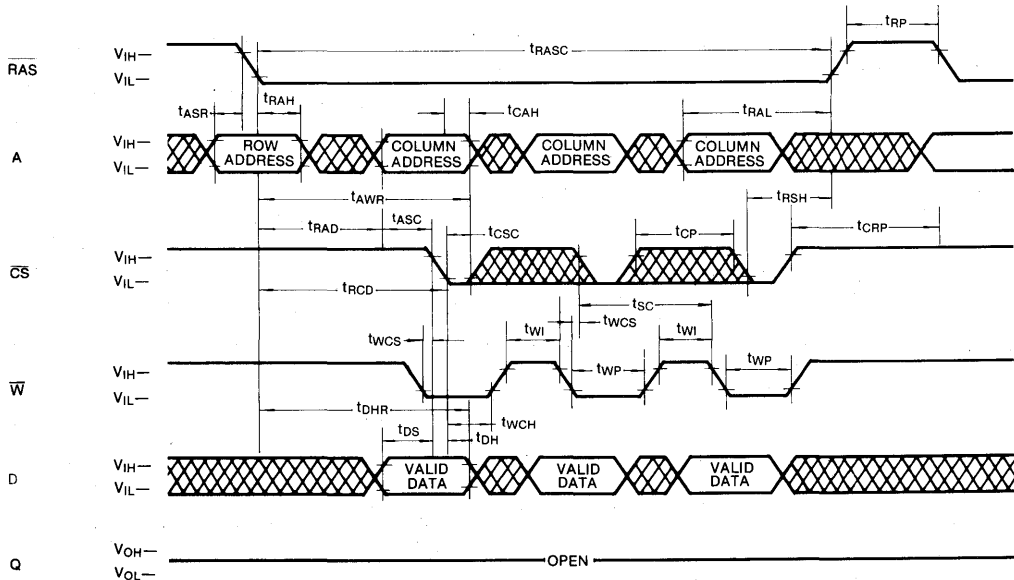
DON'T CARE

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ CYCLE



STATIC COLUMN MODE WRITE CYCLE (\bar{W} controlled early write)

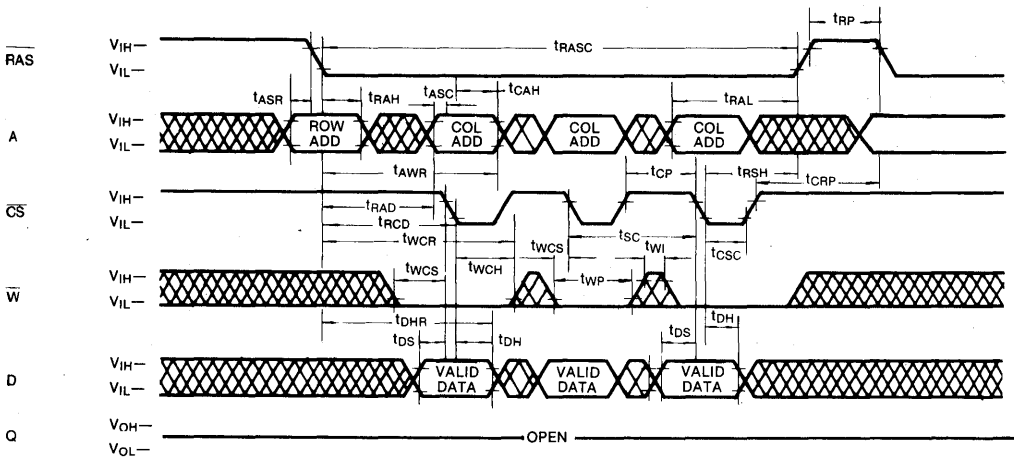


DON'T CARE

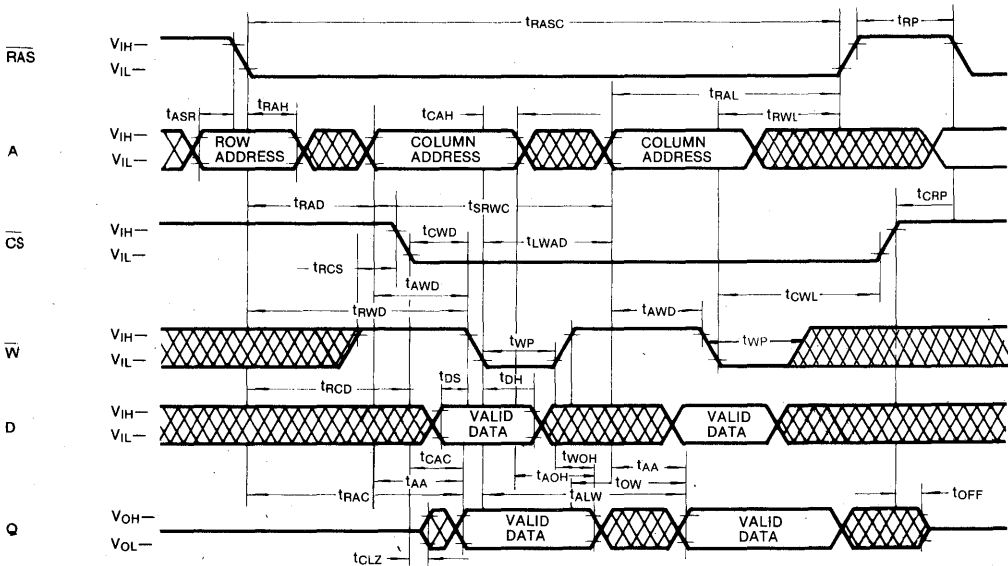
3

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE (\overline{CS} controlled early write)

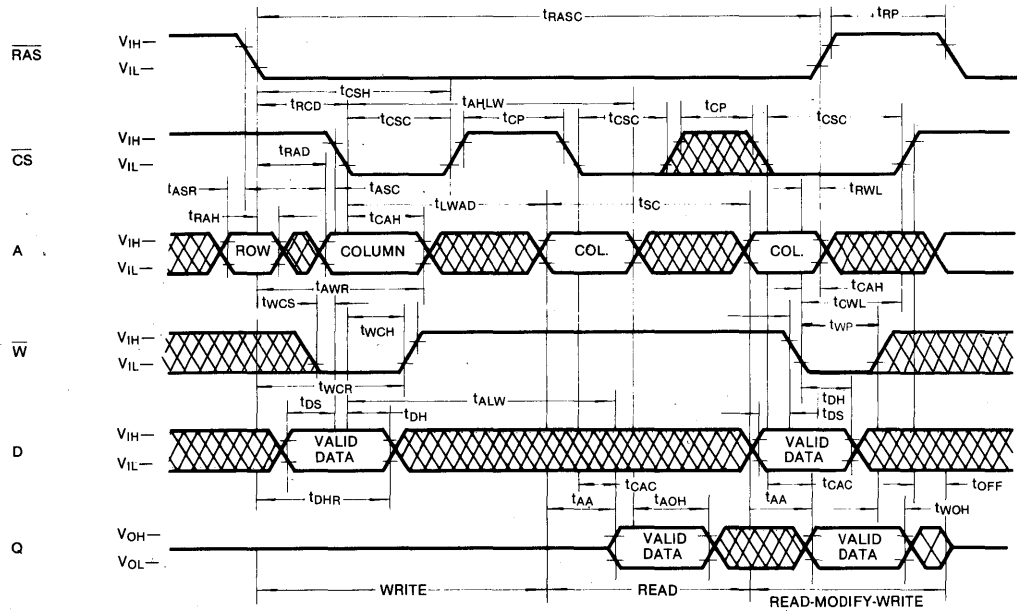


STATIC COLUMN MODE READ-WRITE CYCLE



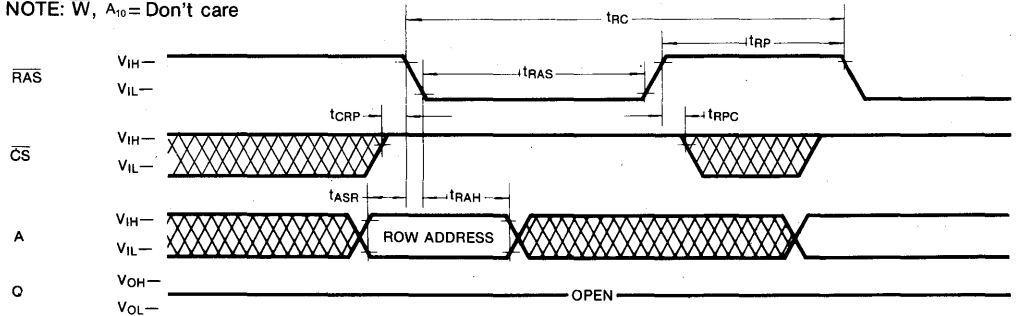
 DON'T CARE

TIMING DIAGRAMS (Continued)
STATIC COLUMN MODE MIXED CYCLE



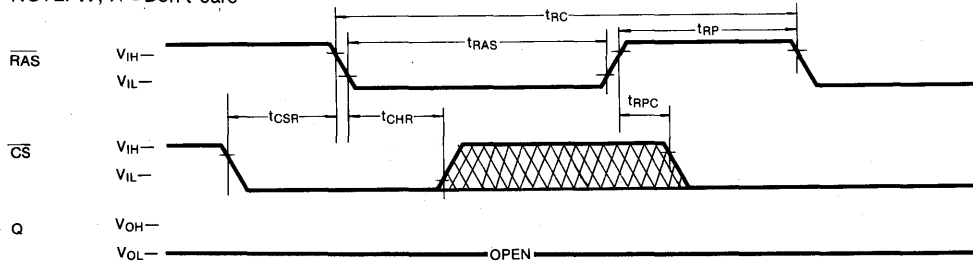
RAS-ONLY REFRESH CYCLE

NOTE: \bar{W} , A_{10} = Don't care



CS-BEFORE-RAS REFRESH CYCLE

NOTE: \bar{W} , A = Don't care

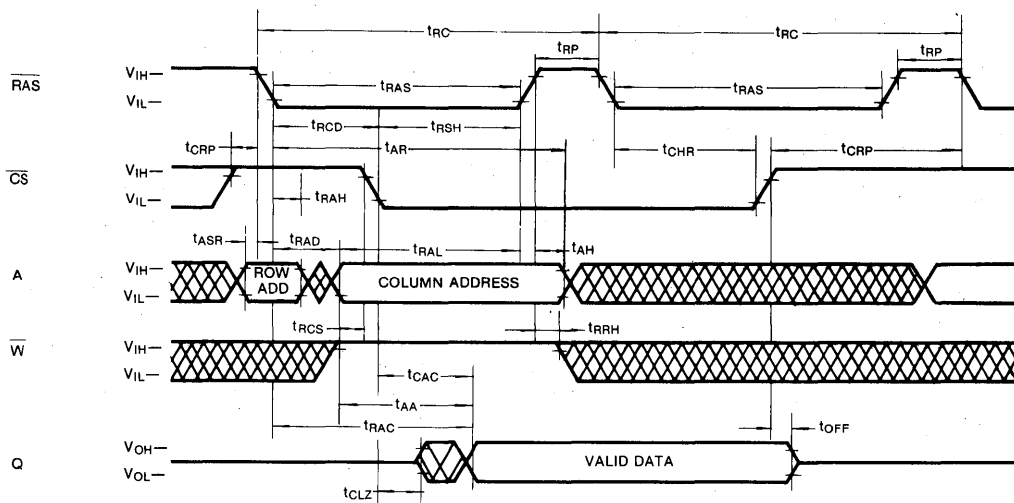


DON'T CARE

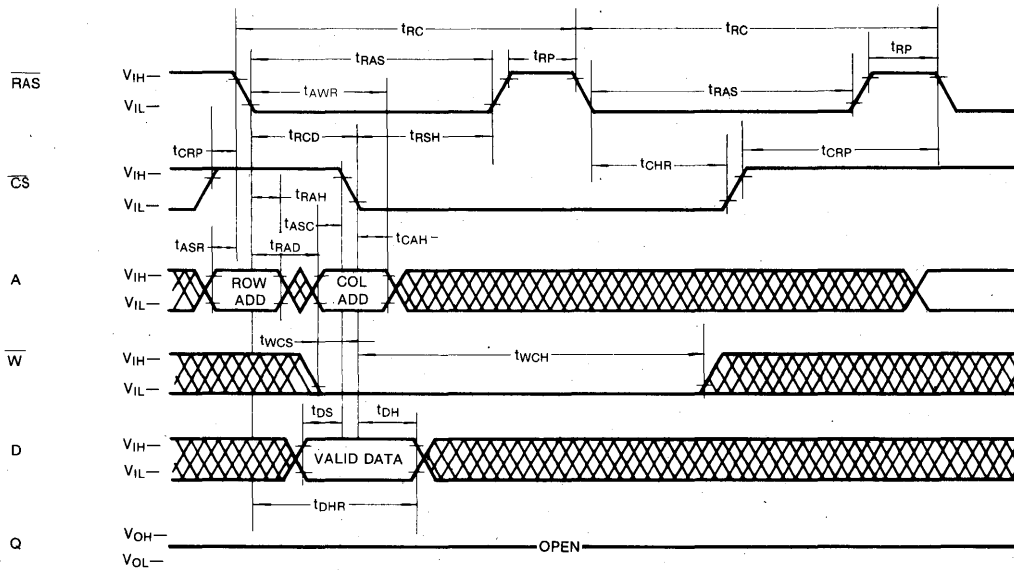
3

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



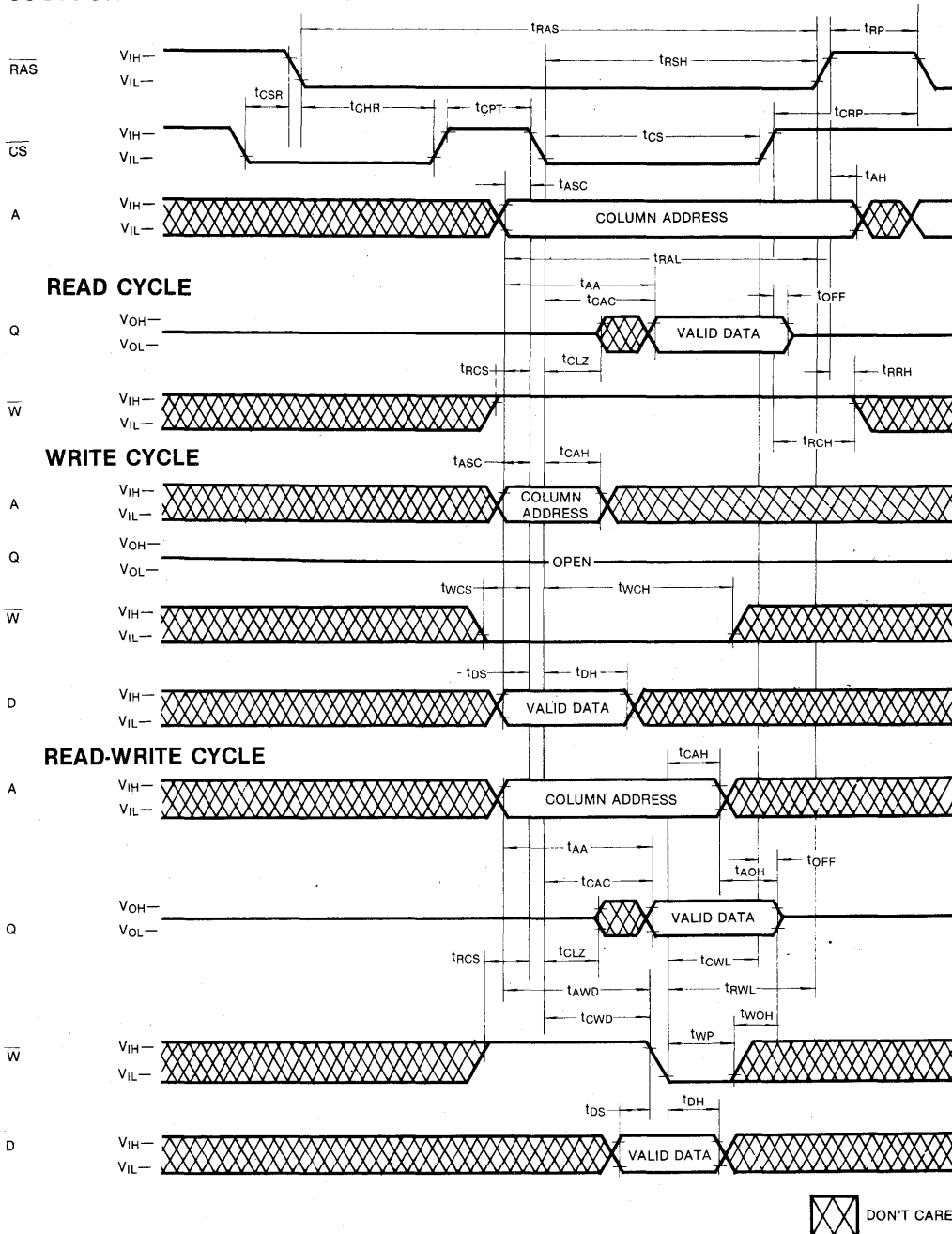
HIDDEN REFRESH CYCLE (WRITE)



 DON'T CARE

TIMING DIAGRAMS (Continued)

CS-BEFORE-RAS BEFRESH COUNTER TEST CYCLE

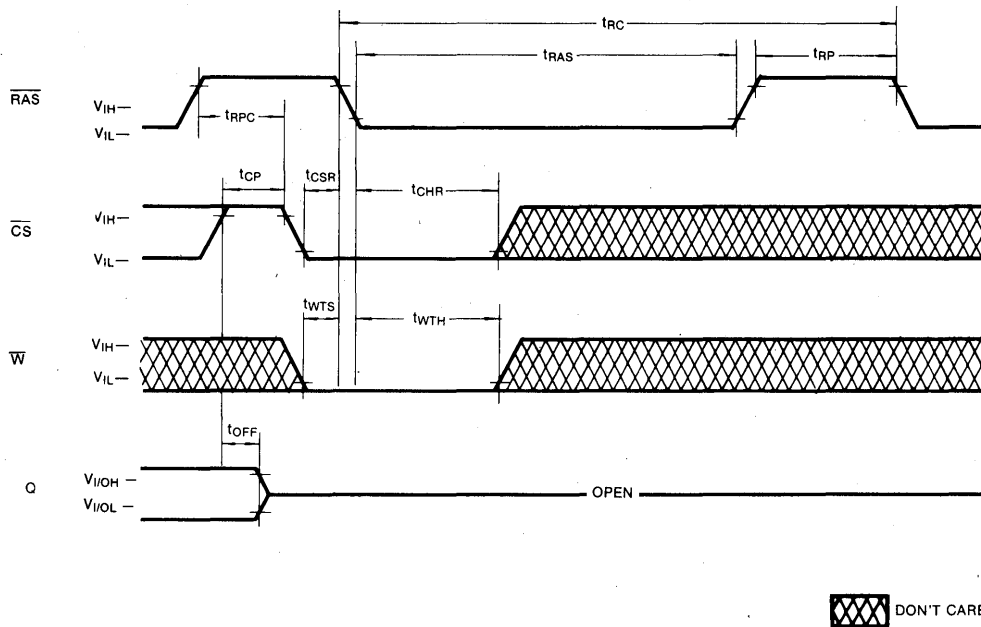


3

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM41C4002C is the RAM organized 4,194,304 words by 1 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. A10R, A10C and A0C are not used. If, upon reading, all bits are equal (all "1"s or "0"s), the data output pin indicates a "1". If any of the bits differed, the data output pin would in-

dicates a "0". In "Test Mode", the 4M DRAM can be tested as if it were a 512K DRAM. W, CS-Before-RAS Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "CS-Before-RAS Refresh Cycle" or "RAS only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/8 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM41C4002C contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41C4002C has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the chip select input (\overline{CS}) and the valid row and column address inputs.

Operation of the KM41C4002C begins by strobing in a valid row address with \overline{RAS} while \overline{CS} remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by \overline{CS} . This is the beginning of any KM41C4002C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CS} Timing

The minimum \overline{RAS} and \overline{CS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41C4002C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{WE}) high during a $\overline{RAS}/\overline{CS}$ cycle. If \overline{CS} goes low before $t_{RCD(max)}$, the access time to valid data is specified with respect to the falling edge of \overline{RAS} . But the address time also depends on the falling edge of \overline{CS} and on the valid column address transition.

If \overline{CS} goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$ then the access time to valid data is specified by $t_{RAC(min)}$. However, if \overline{CS} goes low after $t_{RCD(max)}$ or if the column address becomes valid after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

Write

The KM41C4002C can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} and \overline{CS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CS} . The data at the data input pin(D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CS} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If \overline{W} is brought low after \overline{CS} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{CWD} and t_{AWD} are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41C4002C has a three-state output buffer which is controlled by \overline{CS} . Whenever \overline{CS} is high(VIH) the output is in the high impedance(Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until \overline{CS} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM41C4002C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Static Column Mode Write, $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ Refresh, $\overline{\text{CS}}$ -only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the KM41C4002C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only-Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CS}}$ remains high. This cycle must be repeated for each row.

$\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM41C4002C has $\overline{\text{CS}}$ -Before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CS}}$ is held low for the specified set up time (t_{CSR}) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CS}}$ active time and cycling $\overline{\text{RAS}}$. The KM41C4002C hidden refresh cycle is actually $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM41C4002C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

Static Column Mode

Static Column Mode allows high speed read, write or read-modify-write random access to all the memory cells within a selected row. Operation within a selected row is similar to a static RAM. The read, write or readmodify-write cycles may be mixed in any order. A Static Column mode read cycles starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{\text{W}}=\overline{\text{Vih}}$ and $\overline{\text{RAS}}=\overline{\text{Vil}}$.

A Static Column mode write cycle starts as a normal cycle. Additional cells within the selected row are written by applying a new column address while $\overline{\text{RAS}}=\overline{\text{Vil}}$ and toggling either $\overline{\text{W}}$ or $\overline{\text{CS}}$. The data is written into the cell triggered by the latter fallin edge of $\overline{\text{W}}$ or $\overline{\text{CS}}$.

 $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry.

After the $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh operation, $\overline{\text{CS}}$ goes high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows.

Row Address — Bits A0 through A9 are supplied by the on-chip refresh counter. The A10 bit is set High internally.

Column Address — Bits A0 through A10 are strobed-in by the falling edge of $\overline{\text{CS}}$ as in a normal memory cycle.

Suggested $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ Counter Test Procedure

The $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle timing is used in each of the following steps:

1. initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 512 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 512 times so that highs are written into the 512 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4

Power-up

If $\overline{\text{RAS}}=\overline{\text{Vss}}$ during power-up, the KM41C4002C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ track with $\overline{\text{Vcc}}$ during power-up or be held at a valid $\overline{\text{Vih}}$ in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no RAS cycles. An initialization cycle is any cycle in which RAS is cycled.

Termination

The lines from the TTL driver circuits to the KM41C4002C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM41C4002C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both

horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

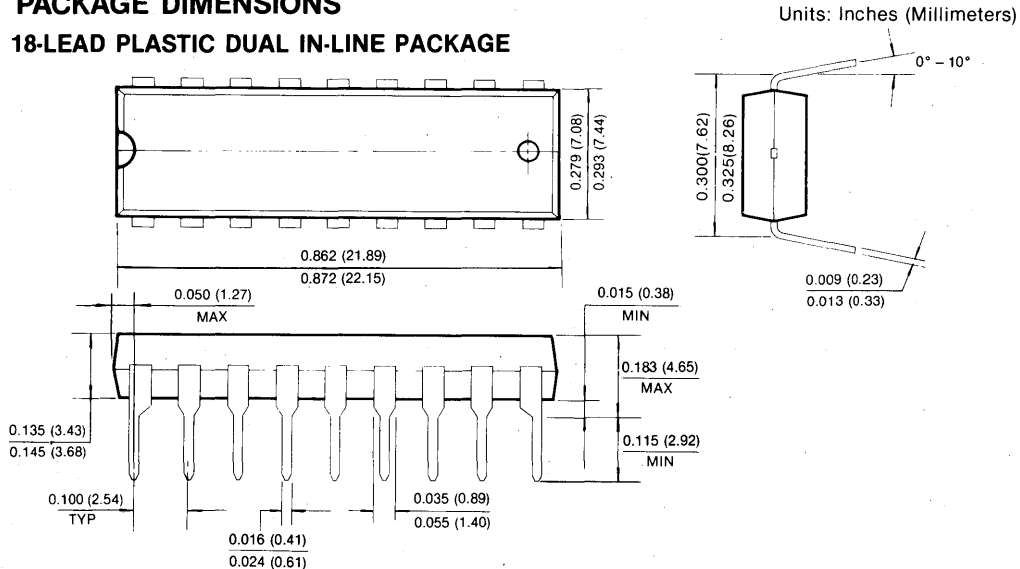
The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41C4002C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41C4002C and they supply much of the current used by the KM41C4002C during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

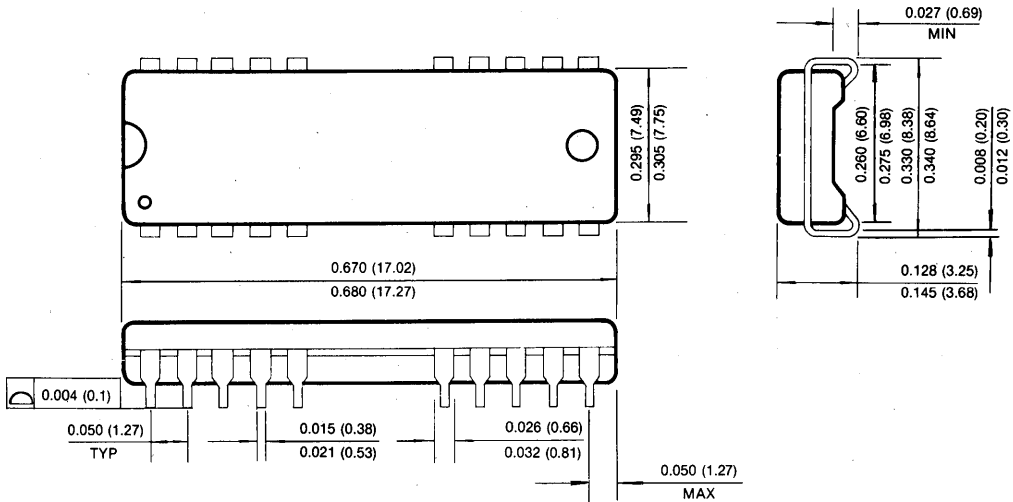
18-LEAD PLASTIC DUAL IN-LINE PACKAGE



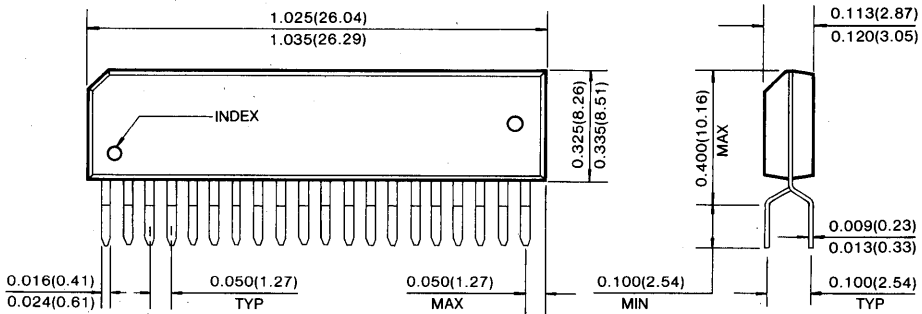
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



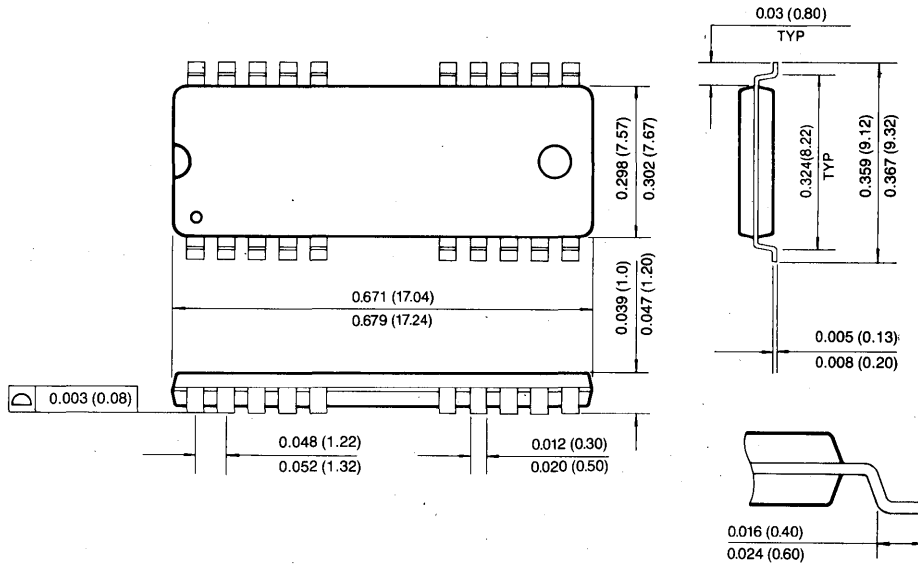
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



3

1M x 4Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	trAC	tcAC	trC
KM44C1000C/CL/CSL-5	50ns	13ns	90ns
KM44C1000C/CL/CSL-6	60ns	15ns	110ns
KM44C1000C/CL/CSL-7	70ns	20ns	130ns
KM44C1000C/CL/CSL-8	80ns	20ns	150ns

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single + 5V \pm 10% power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/256ms (SL-version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
1.1mW (L-Ver.)
0.55mW (SL-Ver.)
 - Active (50/60/70/80): 470/415/360/305mW
- JEDEC standard pinout
- Available in plastic DIP, SOJ, ZIP and TSOP -II packages

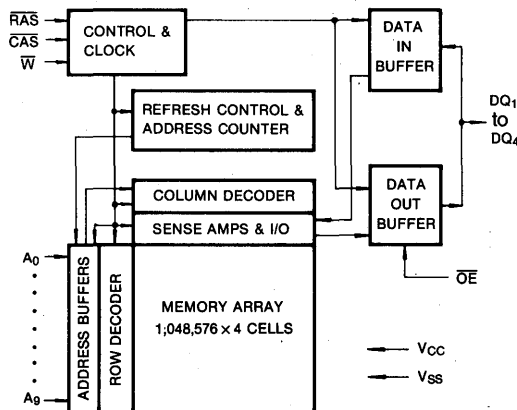
GENERAL DESCRIPTION

The Samsung KM44C1000C/CL/CSL is a high speed CMOS 1,048,576 x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1000C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only Refresh. All inputs and outputs are fully TTL compatible.

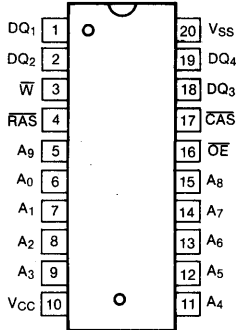
The KM44C1000C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

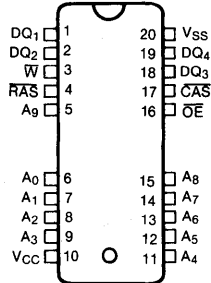


PIN CONFIGURATION (Top Views)

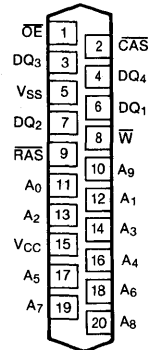
• KM44C1000CP/CLP/CSLP



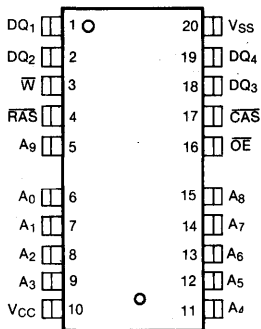
• KM44C1000CJ/CLJ/CSLJ



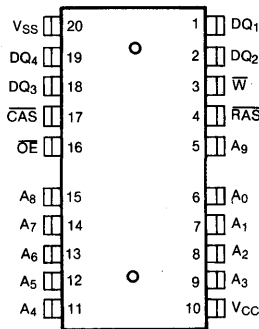
• KM44C1000CZ/CLZ/CSLZ



• KM44C1000CT/CLT/CSLT



• KM44C1000CTR/CLTR/CSLTR



Pin Names	Pin Function
A ₀ -A ₉	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
DQ ₁ ~DQ ₄	Data In/Data Out
V _{CC}	Power (+5V)
V _{SS}	Ground

3

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44C1000C/CL/CSL-5	I _{CC1}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Standby Current (RAS=CAS=W=V _{IH})		I _{CC2}	-	2	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM44C1000C/CL/CSL-5	I _{CC3}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tPC=min.)	KM44C1000C/CL/CSL-5	I _{CC4}	-	65	mA
	KM44C1000C/CL/CSL-6		-	55	mA
	KM44C1000C/CL/CSL-7		-	45	mA
	KM44C1000C/CL/CSL-8		-	35	mA
Standby Current (RAS=CAS=W=V _{CC} -0.2V)	KM44C1000C	I _{CC5}	-	1	mA
	KM44C1000CL		-	200	µA
	KM44C1000CSL		-	100	µA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44C1000C/CL/CSL-5	I _{CC6}	-	85	mA
	KM44C1000C/CL/CSL-6		-	75	mA
	KM44C1000C/CL/CSL-7		-	65	mA
	KM44C1000C/CL/CSL-8		-	55	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DQ1-4=Don't Care, TRC=125µs(L-Ver.) TRC=250µs(SL-Ver.), TRAS=TRAS min~300ns	KM44C1000CL	I _{CC7}	-	300	µA
	KM44C1000CSL		-	150	µA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.5V$ all other pins not under test=0 volts.)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)	V_{OL}	-	0.4	V

* Note: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1} , I_{CC3} , I_{CC6} , Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. I_{CC4} , Address can be changed maximum once during a fast page Mode cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{CC} = 5V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_9)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Output Capacitance (DQ_1-DQ_4)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t_{RW}	133		155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		13		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	30		40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	13		15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	50		60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	37	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	25	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		0		ns	
Column address hold time	t_{CAH}	10		10		15		15		ns	
Column address hold time referenced to \overline{RAS}	t_{AR}	40		45		55		60		ns	6
Column address to \overline{RAS} lead time	t_{RAL}	25		30		35		40		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read command set-up time	trCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		0		ns	9
Write command hold time	twCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	13		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	13		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	twCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tcPT	20		20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		30		35		40		45	ns	3
Fast page mode cycle time	tpC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tpMWC	76		85		100		105		ns	
$\overline{\text{RAS}}$ pulse width(Fast Page Mode)	trASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{CAS}}$ precharge time(Fast page mode)	tcp	10		10		10		10		ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	toEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	toED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	toEH	13		15		20		20		ns	
Write command hold time (test mode in)	twTH	10		10		10		10		ns	
Write command gold time (test mode in)	twPH	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time($\overline{\text{C}}$ -B- $\overline{\text{R}}$ rcycle)	tWRP	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time($\overline{\text{C}}$ -B- $\overline{\text{R}}$ rcycle)	tWRH	10		10		10		10		ns	

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-5		-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	95		115		135		155		ns	
Read-modify-write cycle time	trwc	138		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	trac		55		65		75		85	ns	3,4,11
Access time from $\overline{\text{CAS}}$	tcac		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{\text{RAS}}$ pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{\text{CAS}}$ pulse width	tcAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ hold time	trSH	18		20		25		25		ns	
$\overline{\text{CAS}}$ hold time	tcSH	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	trAL	30		35		40		45		ns	
$\overline{\text{CAS}}$ to write enable delay	tcWD	41		45		55		55		ns	8
$\overline{\text{RAS}}$ to write enable delay	trWD	78		90		105		115		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	53		60		70		75		ns	8
Fast mode cycle time	tpc	40		45		50		55		ns	
Fast page mode read-modify-write	tpRWC	81		85		100		105		ns	
$\overline{\text{RAS}}$ pulse width(Fast page mode)	trASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	toEA		20		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	toED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	toEH	18		20		25		25		ns	

NOTES

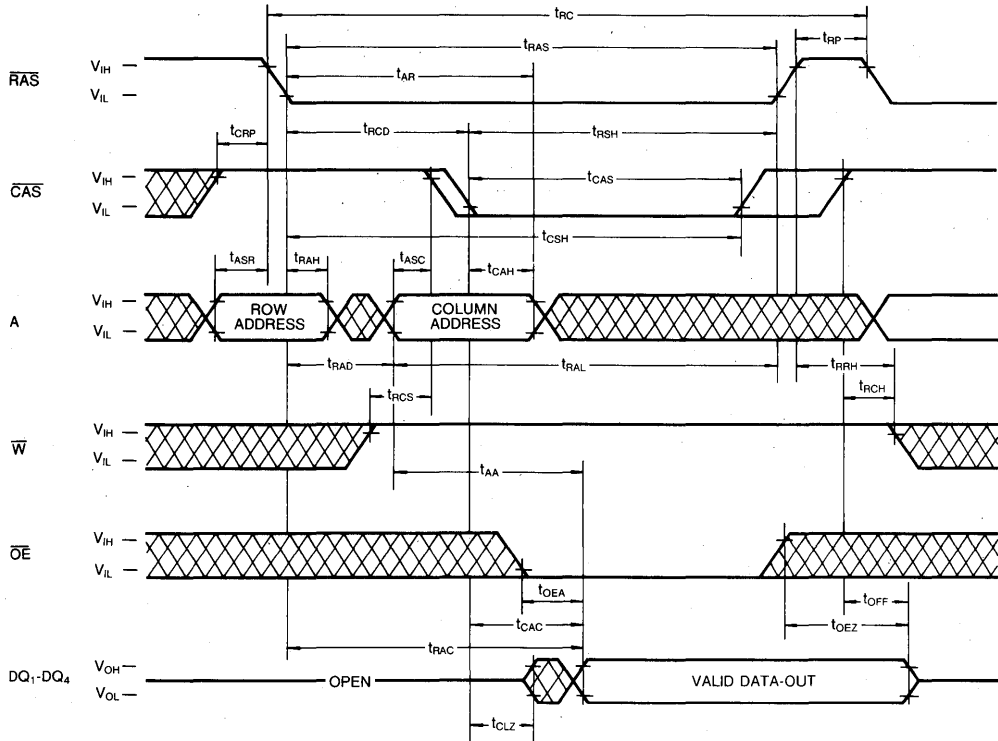
1. An initial pause of 200 μ s is required after power up followed by any 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only Refresh cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD(max)}$ is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD(max)}$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data out

pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.

9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-modify-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF(max)}$ and $t_{OEZ(max)}$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.



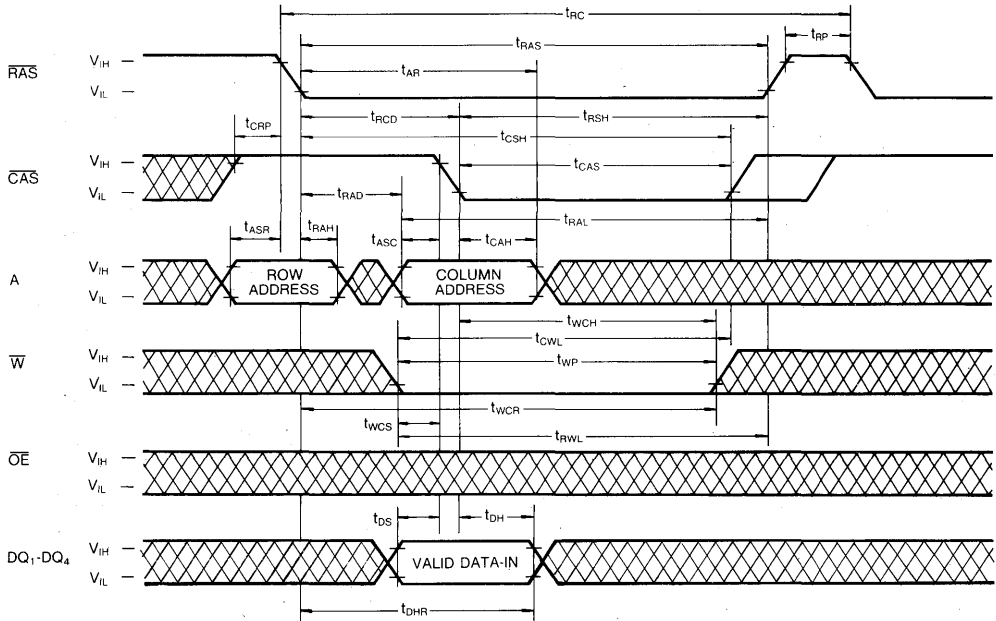
TIMING DIAGRAMS
READ CYCLE



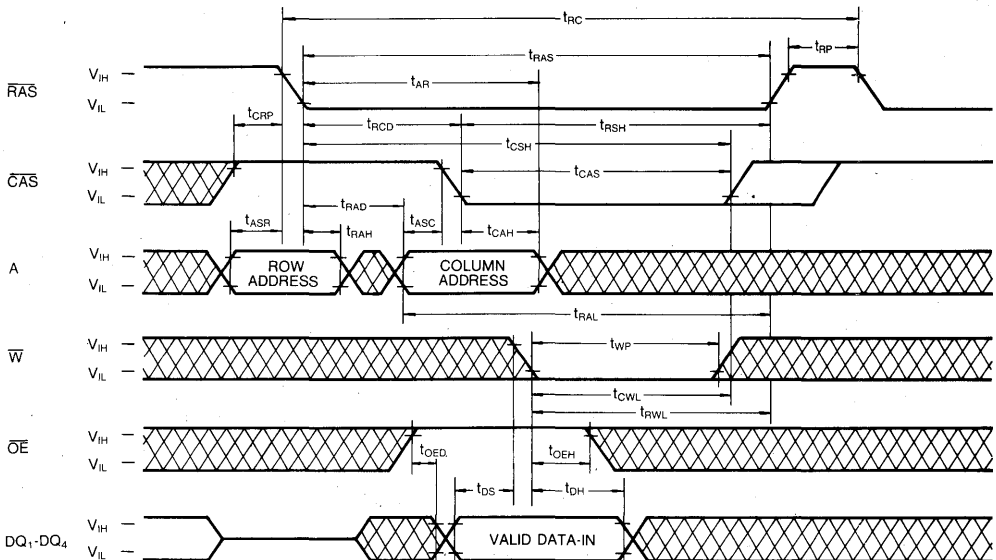
 DON'T CARE

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

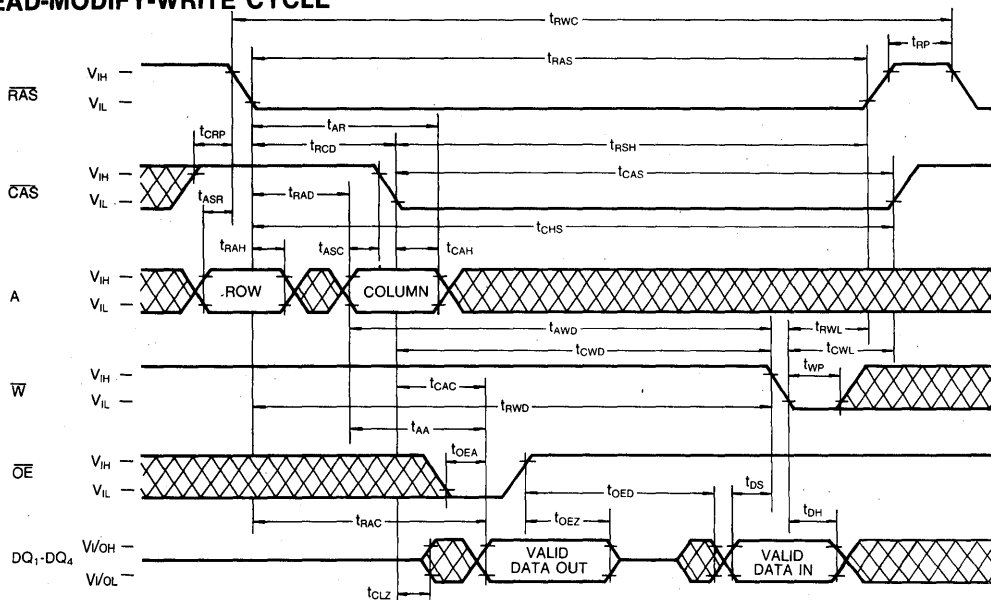


 DON'T CARE

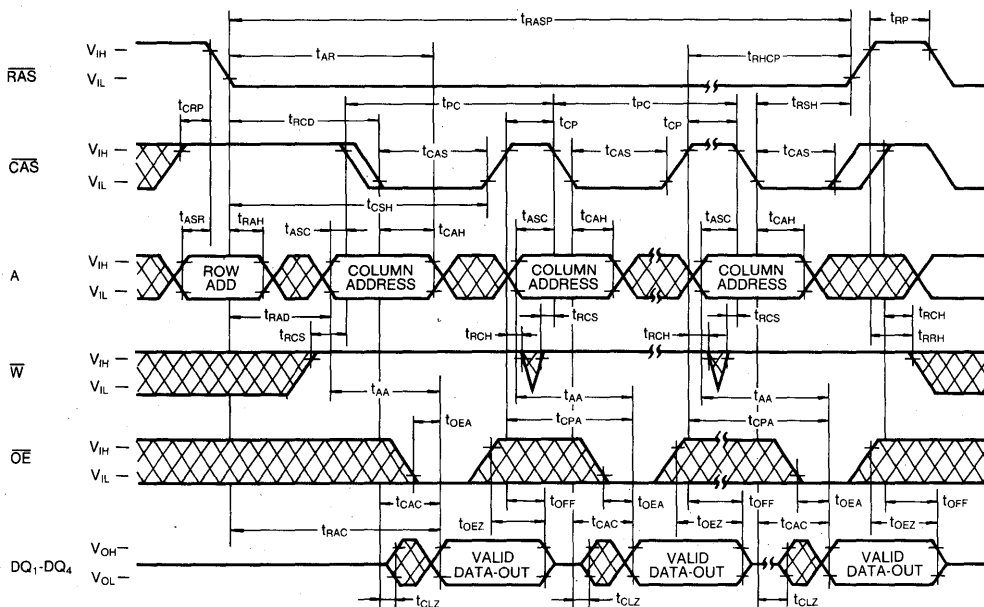
3

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



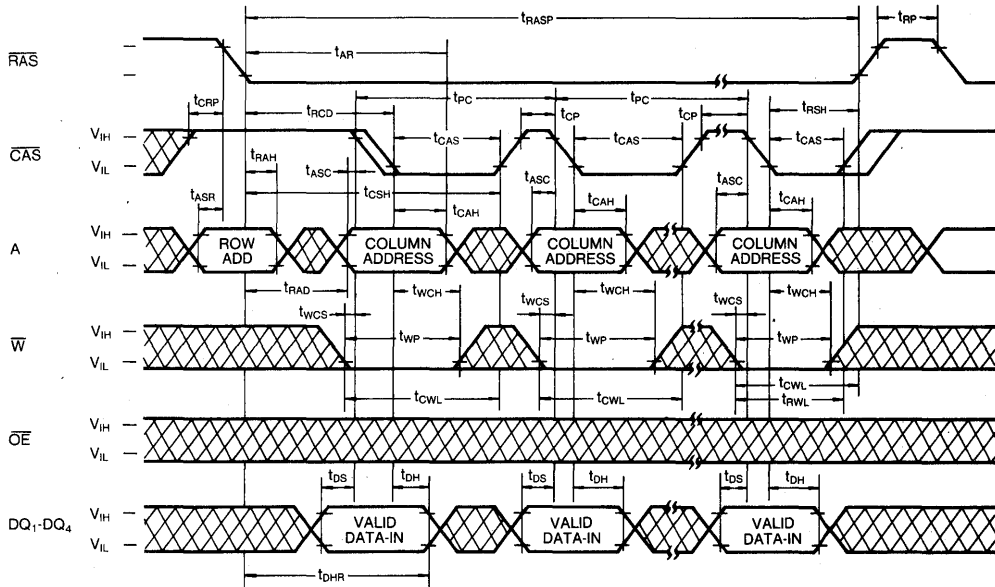
FAST PAGE MODE READ CYCLE



 DON'T CARE

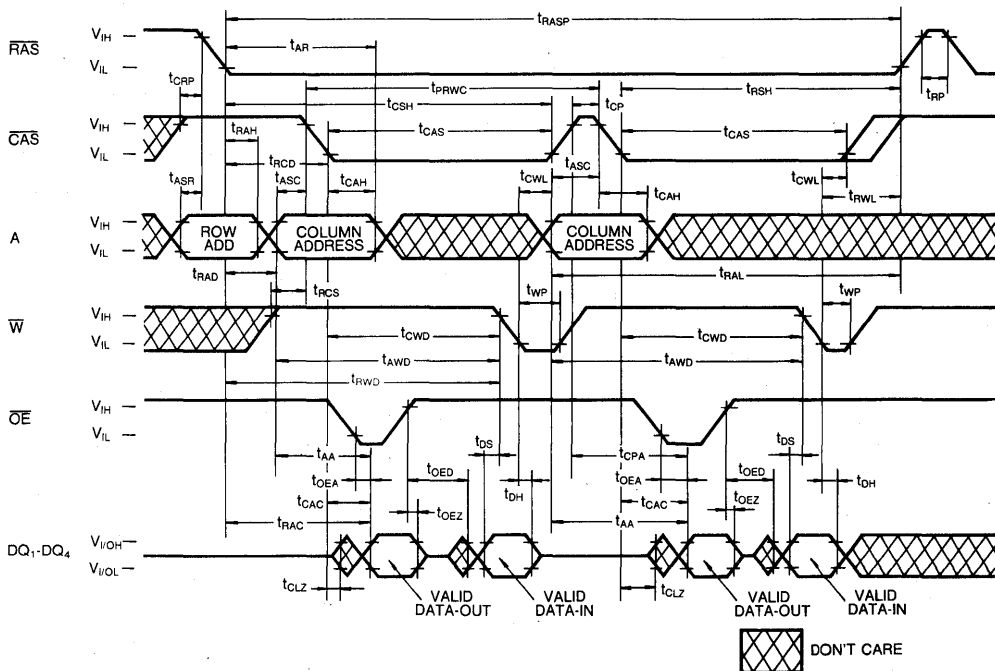
TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



3

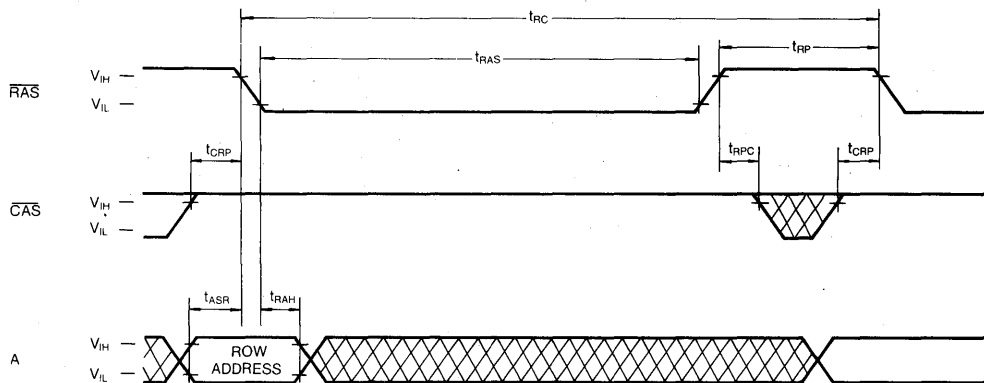
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

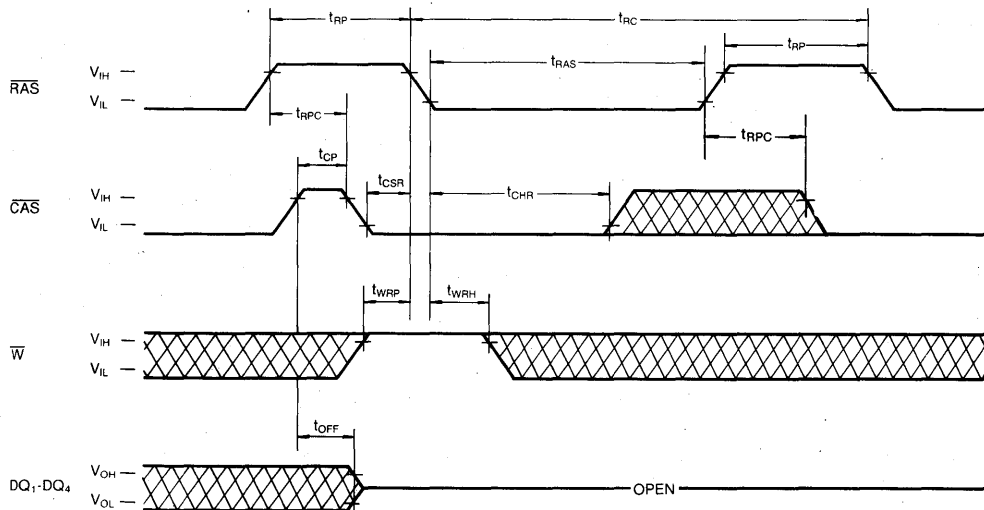
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} =Don't Care

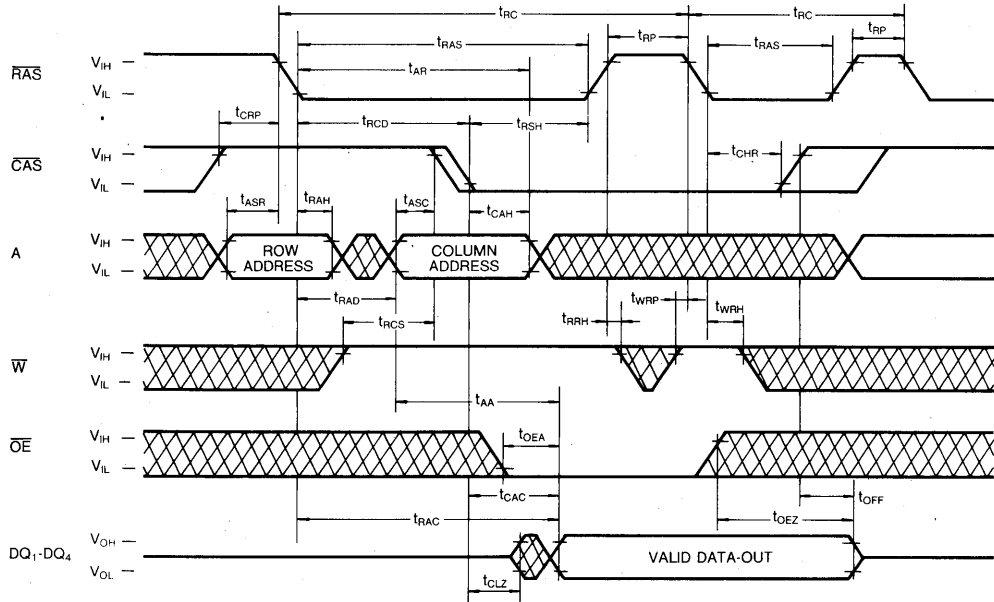


CAS-BEFORE-RAS REFRESH CYCLE

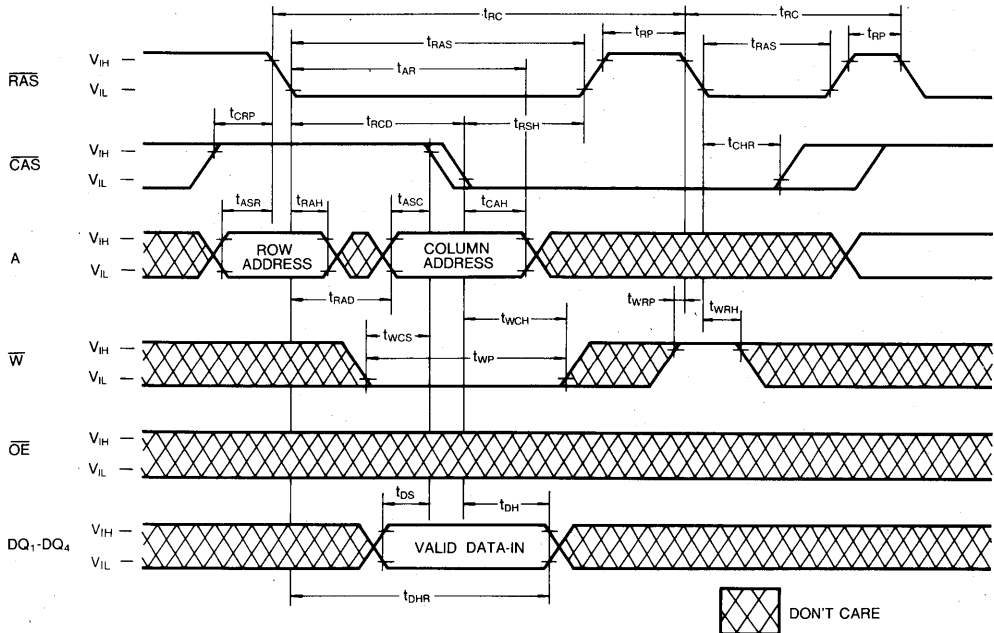
Note: \overline{OE} , Address=Don't Care



TIMING DIAGRAMS (Continued) HIDDEN REFRESH CYCLE (READ)

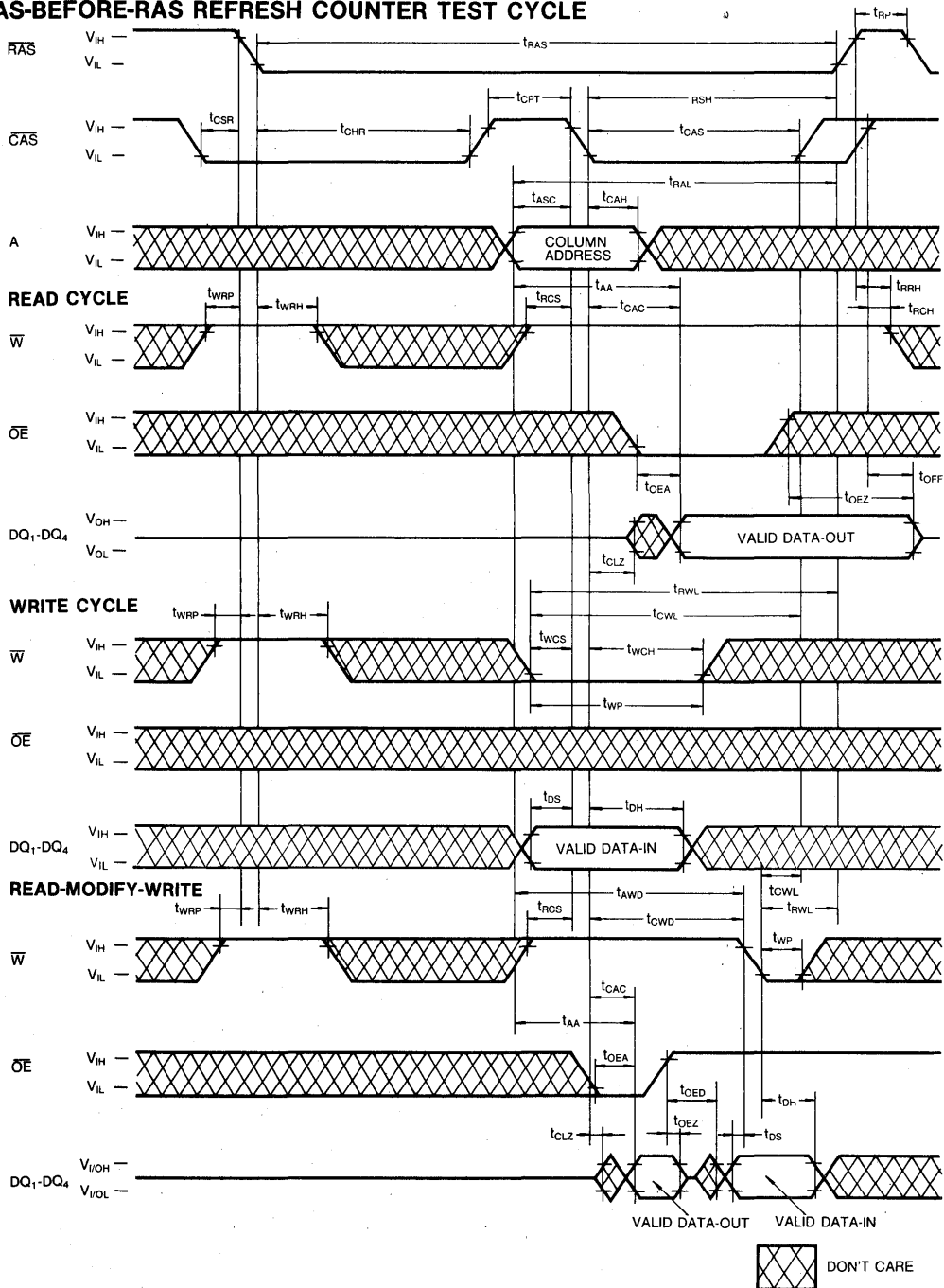


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

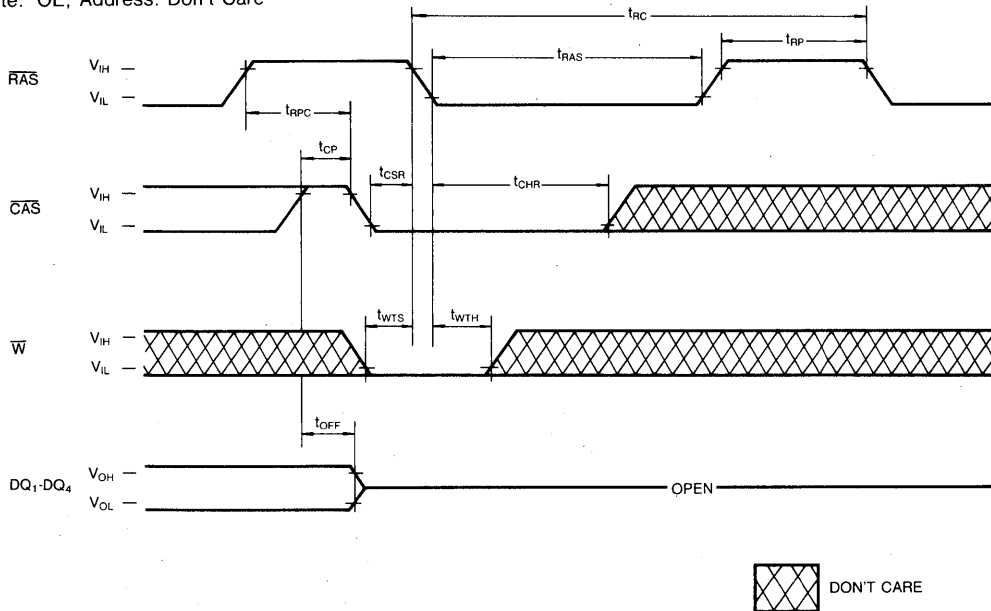
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



3

TEST MODE DESCRIPTION

The KM44C1000C/CL/CSL is the RAM organized 1, 048,576 words by 4 bit internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A₀ is not used. If, upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M x 4 DRAM

can be tested as if it were a 512K x 4DRAM. \overline{W} , \overline{CAS} -BEFORE-RAS Cycle (Test Mode in Cycle) puts the device into "Test Mode", And "CAS-BEFORE-RAS REFRESH CYCLE" or "RAS-only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time(1/2 in cases of N test pattern.)

DEVICE OPERATION

The KM44C1000C/CL/CSL contains 4,194,304 memory locations. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1000C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0 - A_9) and 10 column (A_0 - A_9) address. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}), and the valid row and column address inputs.

Operating of the KM44C1000C/CL/CSL begins by strobing in a valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 10 address input pins (A_0 - A_9) is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM44C1000C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1000C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition.

If \overline{CAS} goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RCD(max)}$, the access time to valid data is specified by $t_{RAC(min)}$. However if \overline{CAS} goes low after $t_{RCD(max)}$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, t_{RAC} (min), it is necessary to meet both $t_{RCD(max)}$ and t_{RAD} (max). The KM44C1000C/CL/CSL has common data I/O pins

For this reason an output enable control input (\overline{OE}) has been provided so the output buffer can be precisely

controlled. For data to appear at the output, \overline{OE} must be low for the period of time defined by t_{OEA} and $t_{O EZ}$.

Write

The KM44C1000C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} and \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention

Late Write: If \overline{W} is brought low after \overline{CAS} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} , t_{CWD} and t_{AWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1000C/CL/CSL has a three-state output buffer which is controlled by \overline{CAS} and \overline{OE} . Whenever \overline{CAS} and \overline{OE} are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until \overline{CAS} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM44C1000C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Fast Page Mode Write, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh, $\overline{\text{OE}}$ controlled write.

Indeterminate Output State: Delayed Write (tcwd or trwd are not met)

Refresh

The data in the KM44C1000C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256ms. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. This cycle must be repeated for each row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM44C1000C/CL/CSL has $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held low for the specified set up time (tcsr) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CAS}}$ active time and cycling $\overline{\text{RAS}}$. The KM44C1000C/CL/CSL hidden refresh cycle is actually a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1000C/CL/CSL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order.

A fast page mode cycle begins with a normal cycle. Then, while $\overline{\text{RAS}}$ is kept low to maintain the $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page

 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry.

After the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation, $\overline{\text{CAS}}$ goes high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell be addressed with 10 row address bits and 10 column address bits defined as follows

Row Address- Bits A₀ through A₉ are supplied by the on-chip refresh counter.

Column Address- Bits A₀ through A₉ are supplied by the falling edge of $\overline{\text{CAS}}$ as in a normal memory cycle.

Suggested $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter Test Procedure

The $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address (The row addresses are supplied by the on-chip refresh counter)
3. Using read-modify-write cycle, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{\text{RAS}}=V_{\text{ss}}$ during power-up, the KM44C1000C/CL/CSL could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{cc} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μsec is required after

DEVICE OPERATION (Continued)

power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L-ver:128, SL-ver:256) msec period in which there are no \overline{RAS} cycles. An initialization cycle is any cycle in which \overline{RAS} is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1000C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1000C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS.

The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV

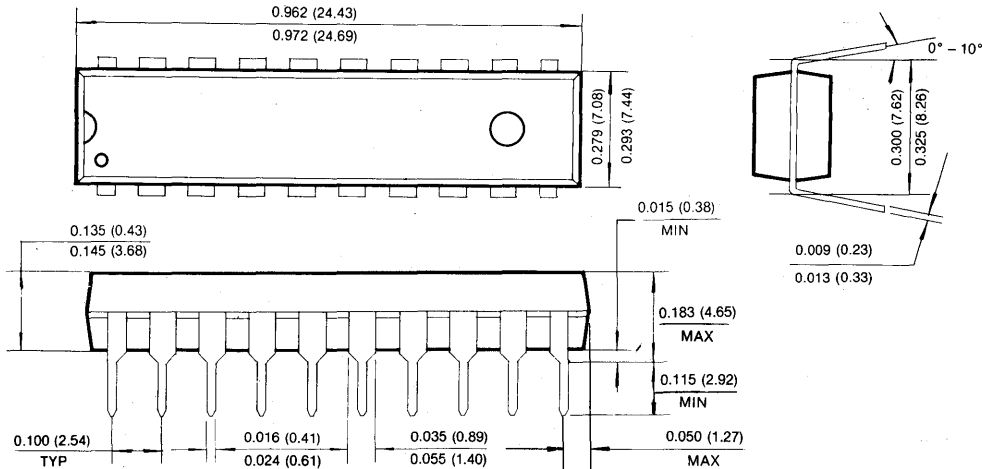
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C1000C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1000C/CL/CSL and they supply much of the current used by the KM44C1000C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

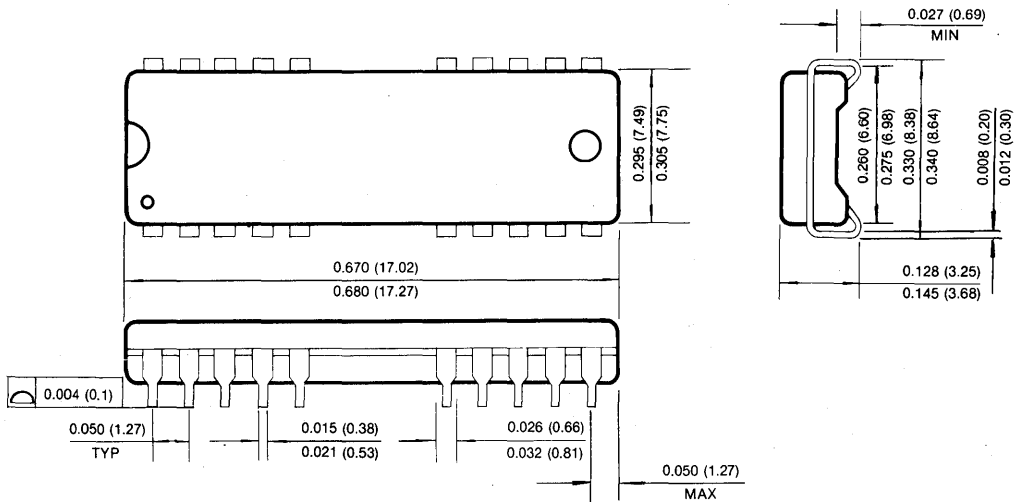
Units: Inches (Millimeters)



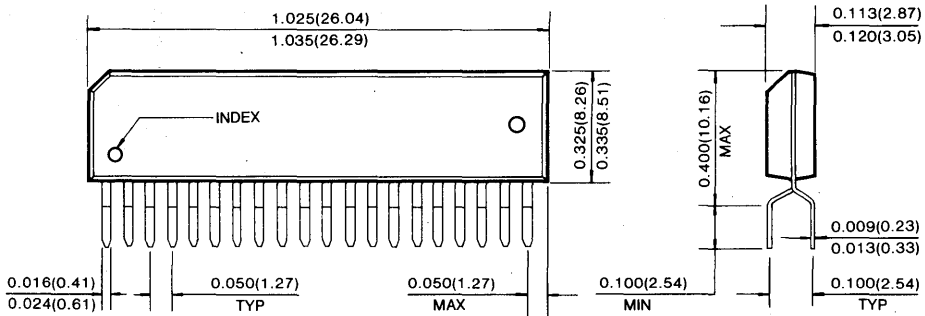
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

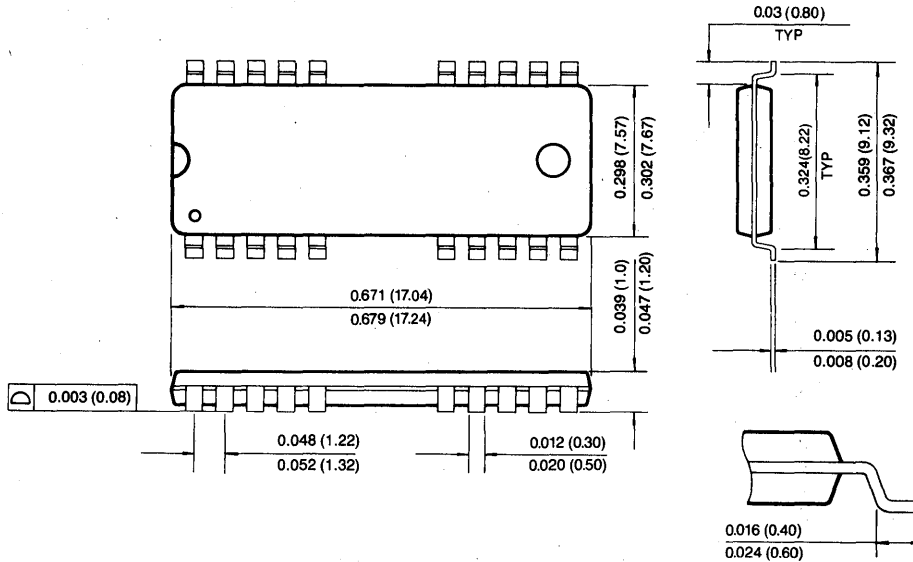


3

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



*1M × 4 Bit CMOS Dynamic RAM with Fast Page Mode
(Write Per Bit Mode)*

FEATURES

• Performance range:

	t _{RAC}	t _{CAC}	t _{RC}
KM44C1010C-5	50ns	13ns	90ns
KM44C1010C-6	60ns	15ns	110ns
KM44C1010C-7	70ns	20ns	130ns
KM44C1010C-8	80ns	20ns	150ns

- Fast Page Mode operation
- Write Per Bit Mode Capability
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early Write or Output Enable Controlled Write
- Single +5V ± 10% power supply
- 1024 cycles/16ms refresh
- JEDEC standard pinout
- Available in plastic DIP, SOP ZIJ and TSOP(II) Packages

GENERAL DESCRIPTION

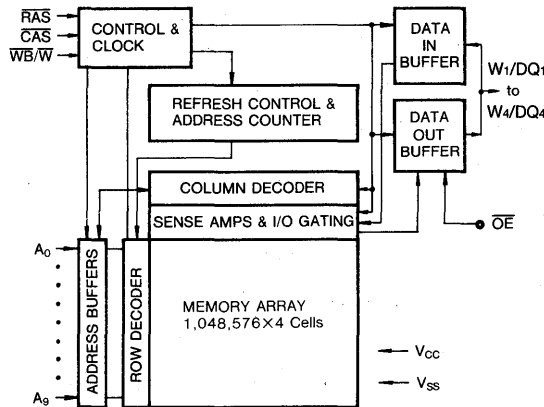
The Samsung KM44C1010C is a high speed CMOS 1, 048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1010C features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM44C1010C is fabricated using Samsung's advanced CMOS process.

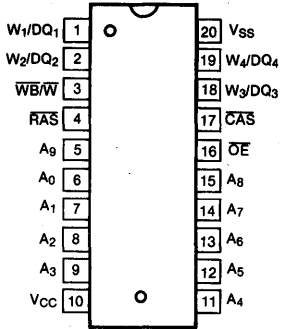
FUNCTIONAL BLOCK DIAGRAM



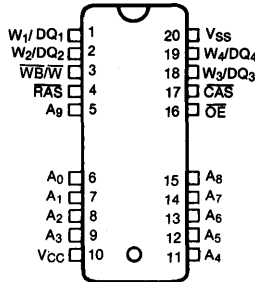
3

PIN CONFIGURATION (Top Views)

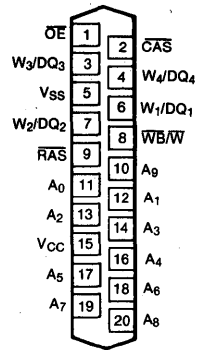
• **KM44C1010CP**



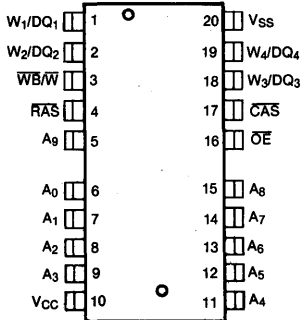
• **KM44C1010CJ**



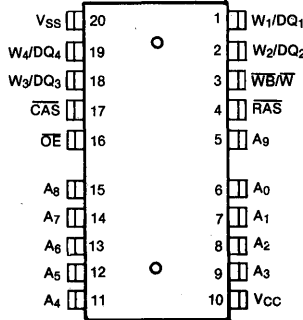
• **KM44C1010CZ**



• **KM44C1010CT**



• **KM44C1010CTR**



Pin Names	Pin Function
A ₀ -A ₉	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
WB/W	Write per bit/Read/Write input
OE	Data Output Enable
W ₁ /DQ ₁ ~ W ₄ /DQ ₄	Write select/Data In/Out
V _{CC}	Power (+ 5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} and \overline{CAS} Cycling @ t _{RC} =min.)	KM44C1010C-5	-	85	mA
	KM44C1010C-6	-	75	mA
	KM44C1010C-7	-	65	mA
	KM44C1010C-8	-	55	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{WB}/\overline{W}=V_{IH}$)	I _{CC2}	-	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} Cycling @ t _{RC} =min.)	KM44C1010C-5	-	85	mA
	KM44C1010C-6	-	75	mA
	KM44C1010C-7	-	65	mA
	KM44C1010C-8	-	55	mA
Standby Column Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @ t _{PC} =min.)	KM44C1010C-5	-	65	mA
	KM44C1010C-6	-	55	mA
	KM44C1010C-7	-	45	mA
	KM44C1010C-8	-	35	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{WB}/\overline{W}=V_{CC}-0.2V$)	I _{CC5}	-	1	mA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @ t _{RC} =min.)	KM44C1010C-5	-	85	mA
	KM44C1010C-6	-	75	mA
	KM44C1010C-7	-	65	mA
	KM44C1010C-8	-	55	mA
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{CC} +0.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. In I_{CC4}, Address can be changed maximum once during a Fast Page mode cycle.

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A9)	CIN1	-	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WB/W}}$, $\overline{\text{OE}}$)	CIN2	-	7	pF
Input Capacitance (W1/DQ1~W4/DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VCC=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		130		150		ns	
Read-modify-write cycle time	tRWC	133		155		185		205		ns	
Fast page mode cycle time	tPC	30		40		45		50		ns	
Fast page mode read-write cycle time	tPRWC	76		85		100		105		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60		70		80	ns	3,4,11
Access time from $\overline{\text{CAS}}$	tCAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ pulse width (fast page mode)	tRASC	50	200,000	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	50		60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time (fast page mode)	tCP	10		10		10		10		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold	tCAH	10		10		15		15		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command hold time referenced to \overline{RAS}	twCRT	40		45		55		60		ns	6
Write command pulse width	WP	10		10		15		15		ns	
Write command to \overline{RAS} lead time	trWL	15		15		20		20		ns	
Write command to \overline{CAS} lead time	tcWL	13		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to \overline{RAS}	tDHR	40		45		55		60		ns	6
Refresh period	tREF		16		16		16		16	ms	
Write command set-up time	twCS	0		0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	tcWD	36		40		50		50		ns	8
\overline{RAS} to \overline{W} delay time	trWD	73		85		100		110		ns	8
Column address to \overline{W} delay time	tAWD	40		55		65		70		ns	8
\overline{CAS} setup time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		15		15		ns	
\overline{RAS} to \overline{CAS} hold time	trPC	5		5		5		5		ns	
\overline{CAS} precharge time (\overline{CAS} -before- \overline{RAS} counter test cycle)	tcPT	20		20		25		30		ns	
Write command set-up time (test mode in)	twTS	10		10		10		10		ns	
Write command hold time (test mode in)	twTH	10		10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{CAS} -before- \overline{RAS} cycle)	twRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{CAS} -before- \overline{RAS} cycle)	twRH	10		10		10		10		ns	
\overline{OE} access time	toEA		13		15		20		20	ns	
\overline{OE} to data delay	toED	13		15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	toEZ	0	13	0	15	0	20	0	20	ns	
\overline{OE} command hold time	toEH	13		15		20		20		ns	
Write per bit set-up time	twBS	0		0		0		0		ns	
Write per bit hold time	twBH	10		10		10		15		ns	
Write per bit selection set-up time	twDS	0		0		0		0		ns	
Write per bit selection hold time	twDH	10		10		10		15		ns	

3

TEST MODE CYCLE

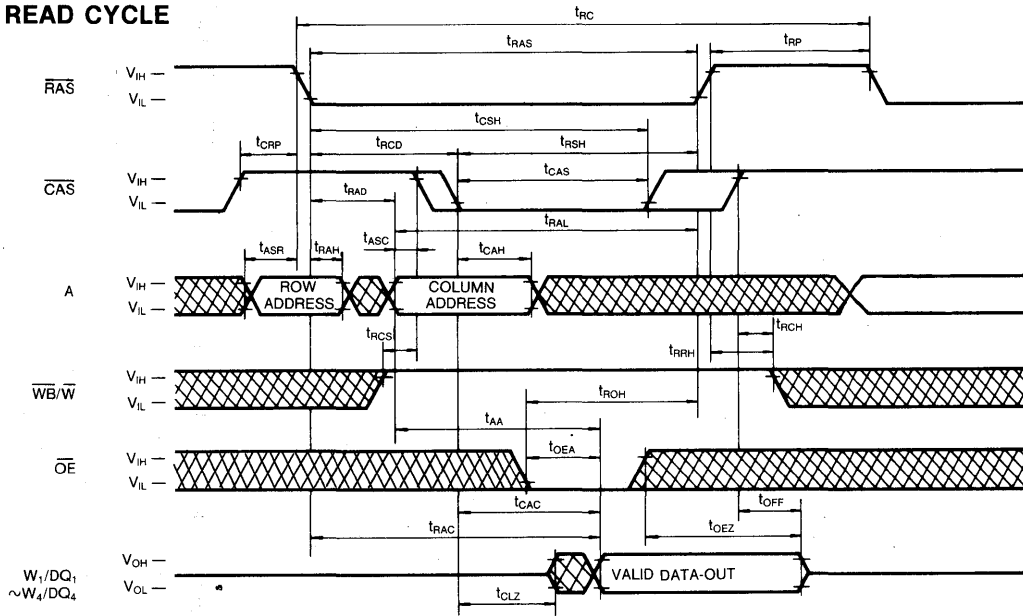
(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t _{RWC}	138		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{\text{CS}}$	t _{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t _{AAC}		30		35		40		45	ns	3,11
$\overline{\text{RAS}}$ pulse width	t _{RAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	18		20		25		25		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		40		45		ns	
$\overline{\text{CAS}}$ to Write enable delay	t _{CWD}	41		45		55		55		ns	8
$\overline{\text{RAS}}$ to Write enable delay	t _{RWD}	78		90		105		115		ns	8
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	53		60		70		75		ns	8
Fast mode cycle time	t _{PC}	40		45		50		55		ns	
Fast page mode read-modify-write	t _{PRWC}	81		85		100		105		ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t _{RASP}	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	t _{OEA}		20		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	t _{OED}	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	t _{OEH}	18		20		25		25		ns	

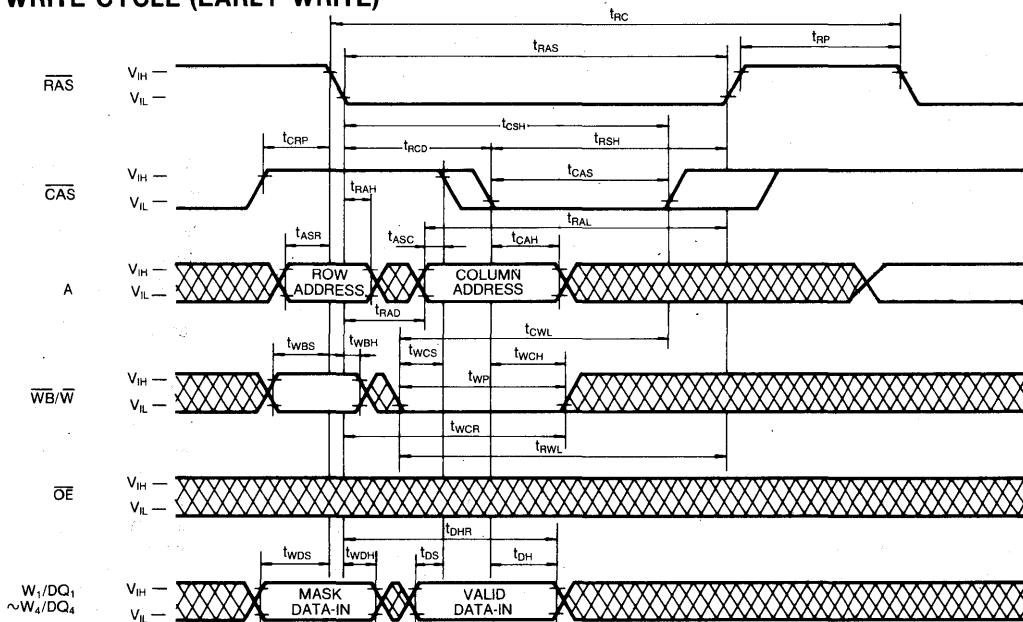
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RCD} \leq t_{RCD}(max).
6. t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} \geq t_{WCS}(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If t_{CWD} \geq t_{CWD}(min) and t_{RWD} \geq t_{RWD}(min) and t_{AWD} \geq t_{AWD}(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AAC}.
12. These specifications are applied in the test mode.

TIMING DIAGRAMS
READ CYCLE



WRITE CYCLE (EARLY WRITE)

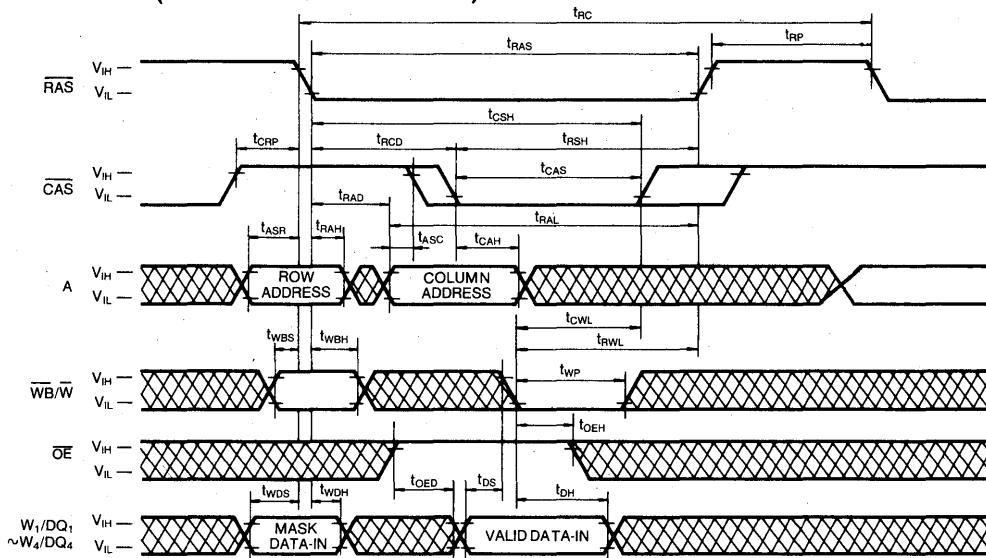


 DON'T CARE

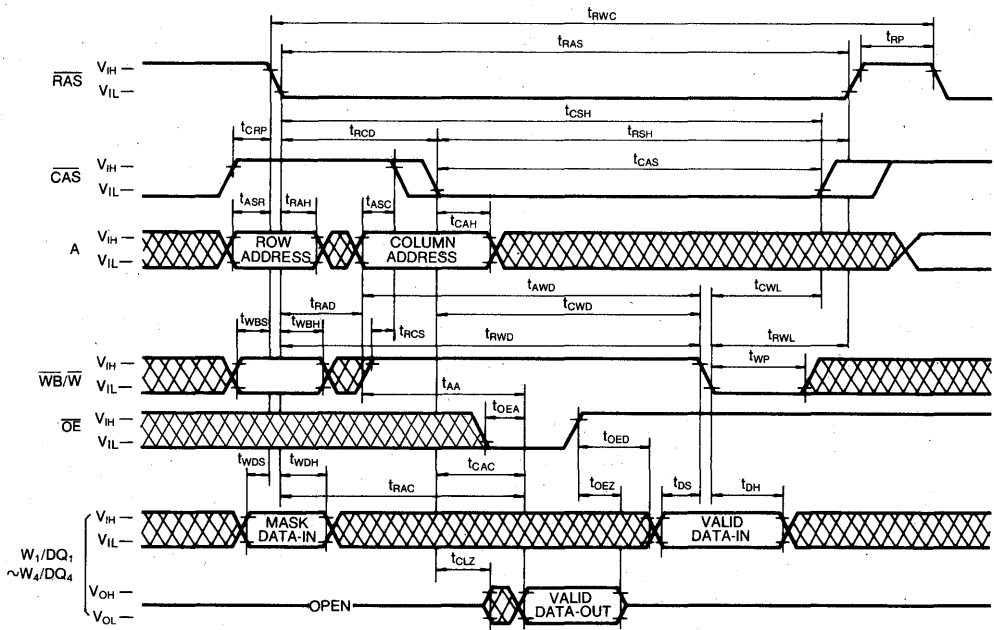
3

TIMING DIAGRAMS (Continued)

WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

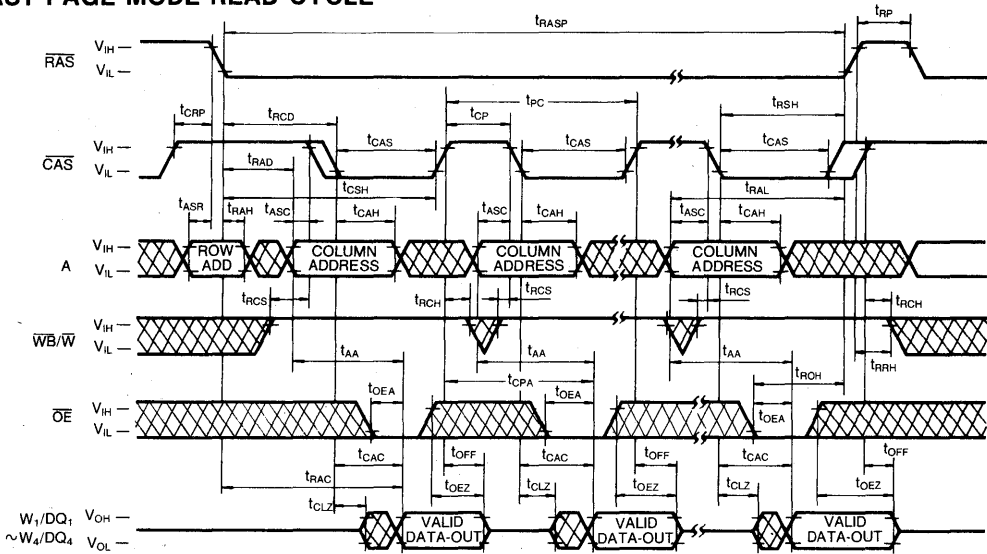


READ-MODIFY-WRITE CYCLE



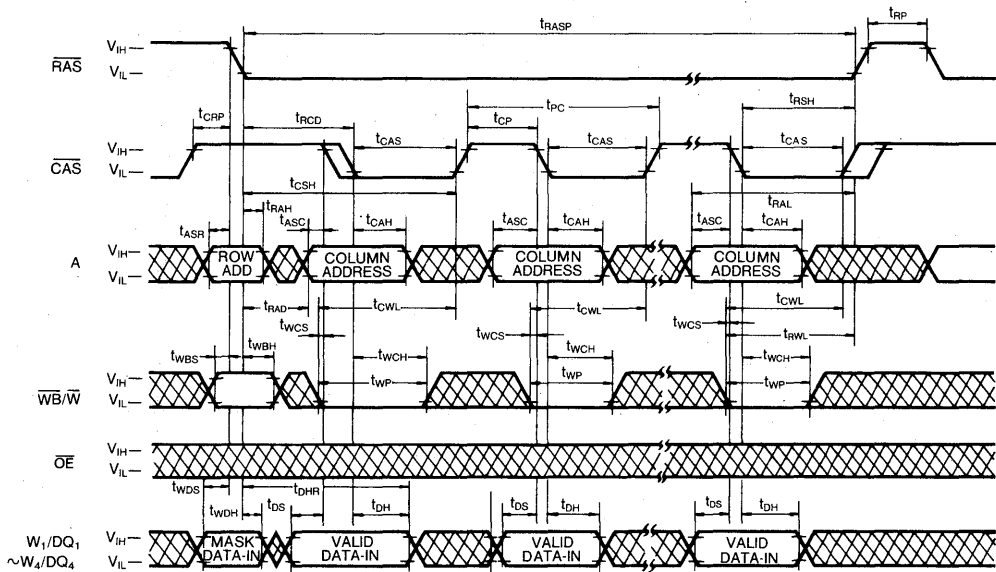
 DON'T CARE

TIMING DIAGRAMS (Continued)
FAST PAGE MODE READ CYCLE



3

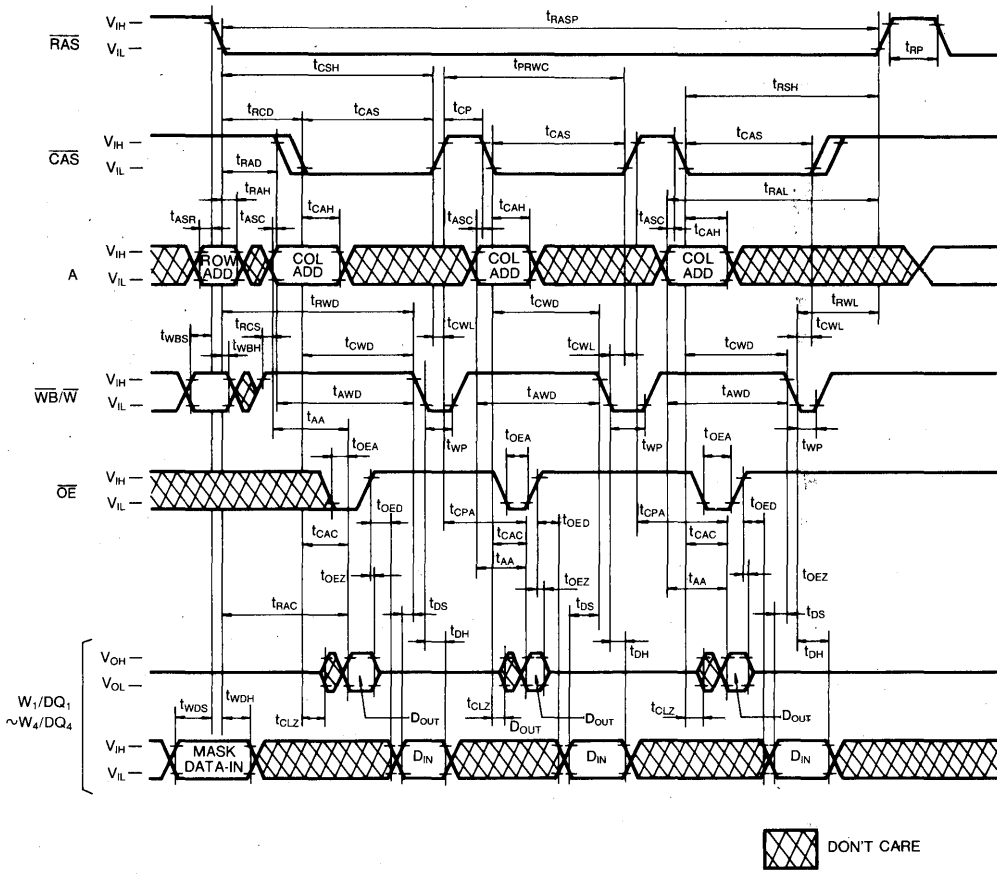
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



 DON'T CARE

TIMING DIAGRAMS (Continued)

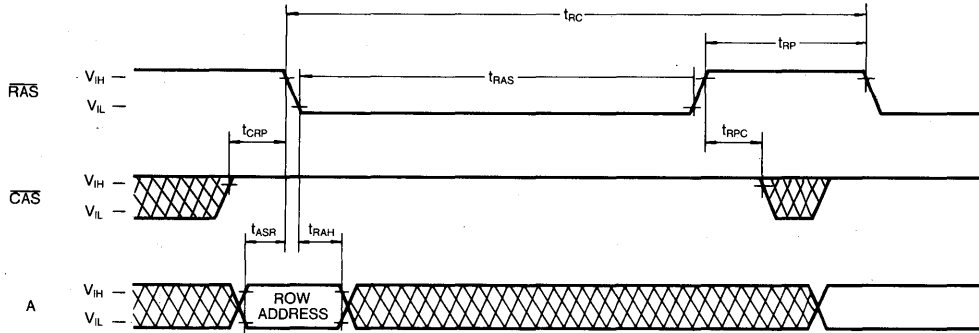
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE

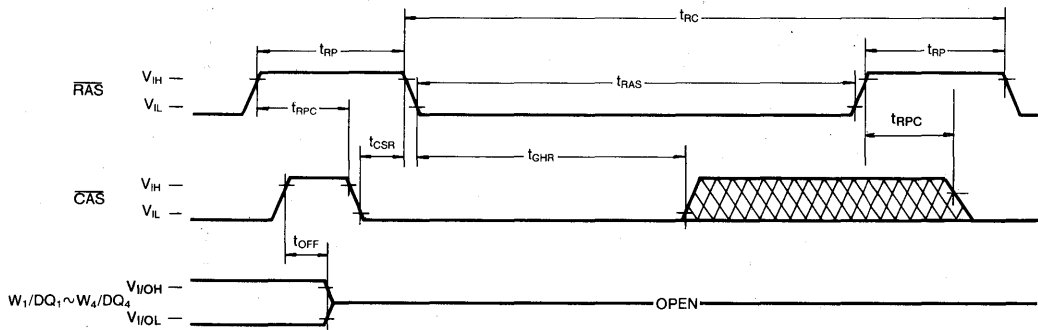
NOTE: $\overline{\text{WB}}/\overline{\text{W}}$, $\overline{\text{OE}}$ =Don't Care



3

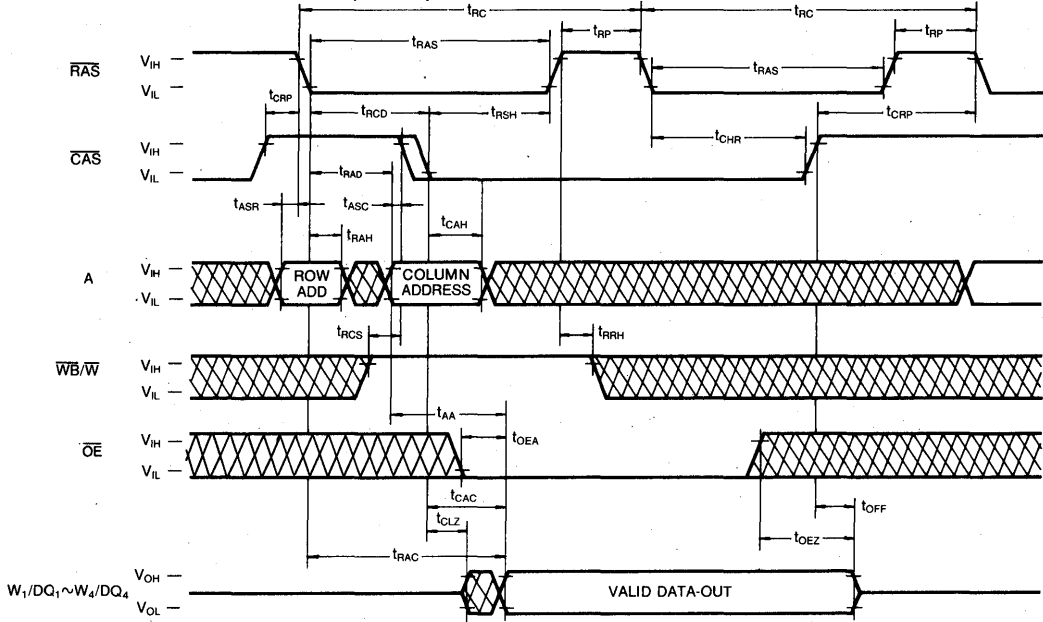
$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE: $\overline{\text{WB}}/\overline{\text{W}}$, $\overline{\text{OE}}$, A=Don't Care

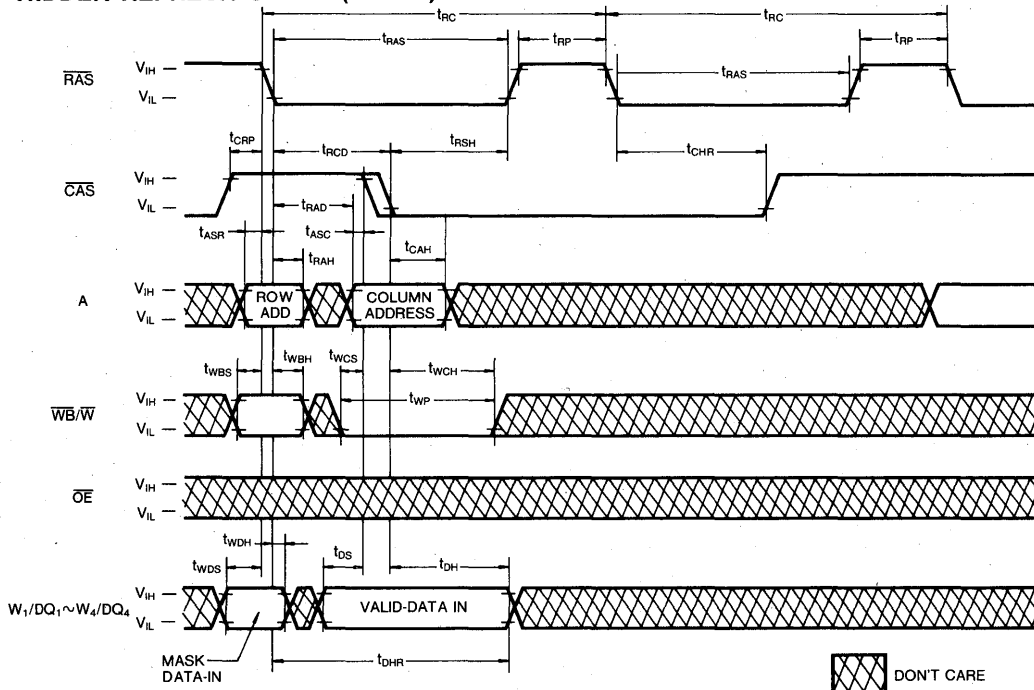


 DON'T CARE

TIMING DIAGRAMS (Continued)
HIDDEN REFRESH CYCLE (READ)

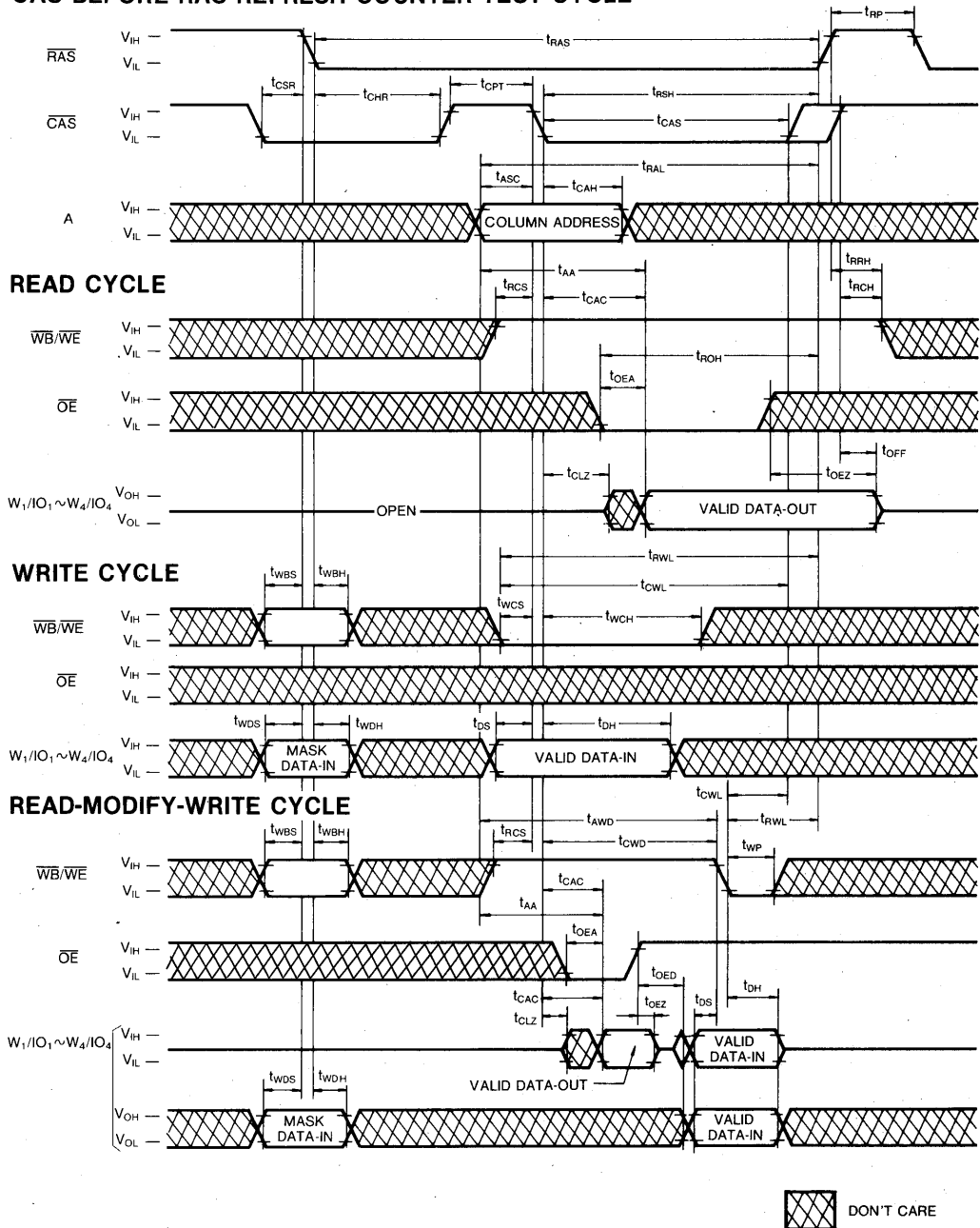


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

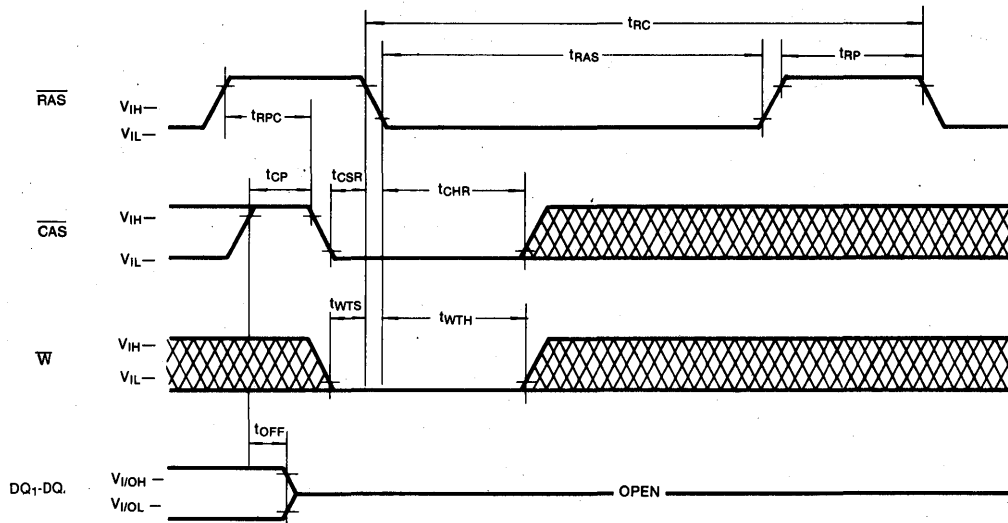


3

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: OE, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1010C is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would

indicate a "0". In "Test Mode", the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. W , $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle" or " $\overline{\text{RAS}}$ only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1010C contains 4,194,304 memory locations organized as 1,048,576 four-bit words. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1010C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}) and the valid address inputs.

Operation of the KM44C1010C begins by strobing in a valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM44C1010C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1010C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition.

If \overline{CAS} goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAD(max)}$ then the access time to valid data is specified by $t_{RAC(min)}$. However, if \overline{CAS} goes low after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

The KM44C1010C has common data I/O pins. For this reason an output enable control input (\overline{OE}) has been provided so the output buffer can be precisely controlled.

For data to appear at the outputs, \overline{OE} must be low for the period of time defined by t_{OEa} and t_{OEz} .

Write

The KM44C1010C can perform early write. \overline{OE} controlled write and read-modify-write cycles. Each of these write cycles is achieved by maintaining the write per bit write enable ($\overline{WB}/\overline{W}$) input high at the falling edge of \overline{RAS} . If write-per bit function is performed, $\overline{WB}/\overline{W}$ is kept low at the falling edge of \overline{RAS} . The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} and \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write timing requirements. This output enable input (\overline{OE}) must be low during the time defined by t_{OEa} and t_{OEz} for data to appear at the outputs. If t_{CWD} and t_{RWD} are not met the output may contain invalid data. Conforming to the \overline{OE} timing requirements prevents bus contention on the KM44C1010C DQ pins.

Write-Per-Bit

Write-per-bit function is performed in the write cycle, that is early write. \overline{OE} controlled write, read-modify-write. Write-per-bit makes it possible selectively to write one or more of the four I/O pins. To perform write per-bit function at the falling edge of \overline{RAS} the write-per-bit/Write enable ($\overline{WB}/\overline{W}$) is kept low and at the same time Mask data of input pins to write among 4 I/O pins must be in high. If I/O pins that Mask data is kept low, write operation is inhibited.

Data Output

The KM44C1010C has a three state output buffer which are controlled by \overline{CAS} and \overline{OE} . When either \overline{CAS} or \overline{OE} is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify

DEVICE OPERATION (Continued)

when the valid data will be present at the output. This is true even if a new $\overline{\text{RAS}}$ cycle occurs (as in hidden refresh). Each of the KM44C1010C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Fast Page Mode Write, $\overline{\text{CAS}}$ -only cycle.

Indeterminate Output State: Delayed Write (t_{cwp} or t_{rwd} are not met)

Refresh

The data in the KM44C1010C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. This cycle must be repeated for each of the 1024 row addresses, (A_0 - A_9).

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM44C1010C has $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held low for the specified set up time (t_{CSR}) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CAS}}$ active time and cycling $\overline{\text{RAS}}$. The KM44C1010C hidden refresh cycle is actually a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1010C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry. The cycle begins as a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation. Then, if $\overline{\text{CAS}}$ is brought high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled. In this mode, the row address bits A_0 through A_9 are supplied by the on-chip refresh counter.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle.

Then, while $\overline{\text{RAS}}$ is kept low to maintain the row address, $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{\text{RAS}} = V_{\text{SS}}$ during power-up, the KM44C1010C could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μsec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{\text{RAS}}$ cycles. An initialization cycle is any cycle in which $\overline{\text{RAS}}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1010C inputs act like unterminated transmission lines resulting in significant positive and negative overshoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1010C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are

DEVICE OPERATION (Continued)

gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop

on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C1010C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1010C and they supply much of the current used by the KM44C1010C during cycling.

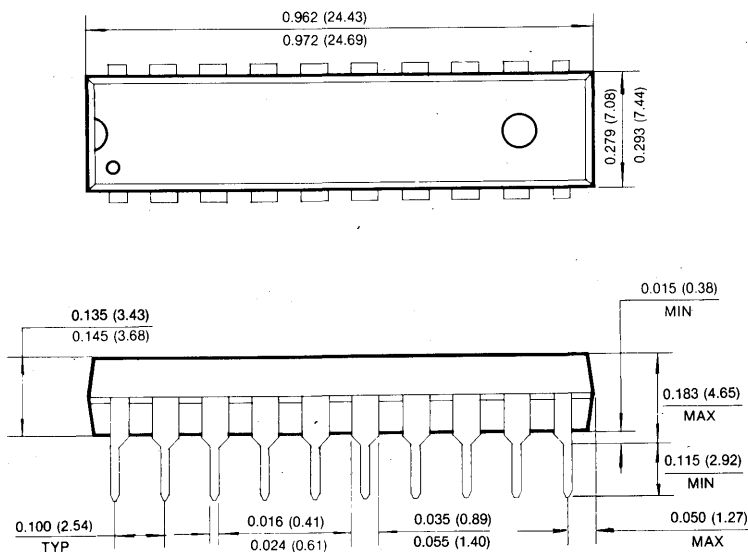
In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

3

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

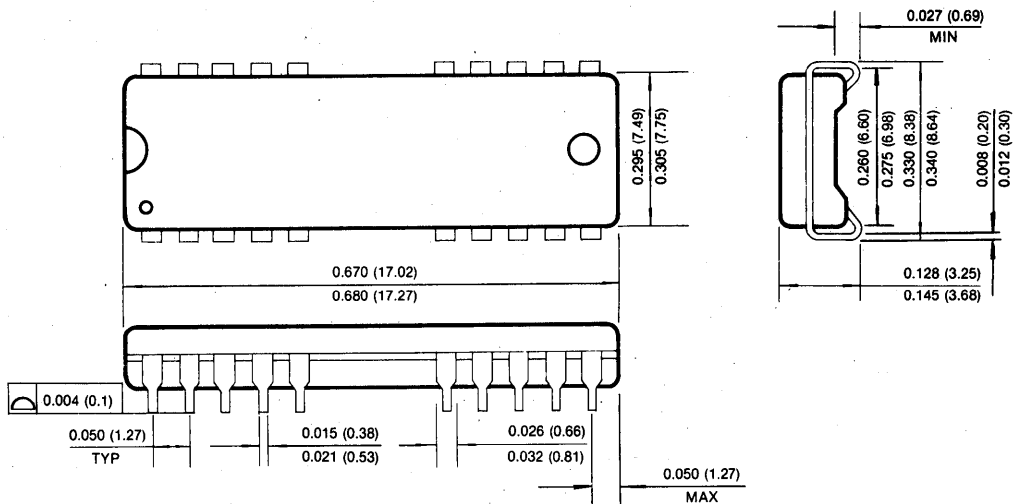
Units: Inches (Millimeters)



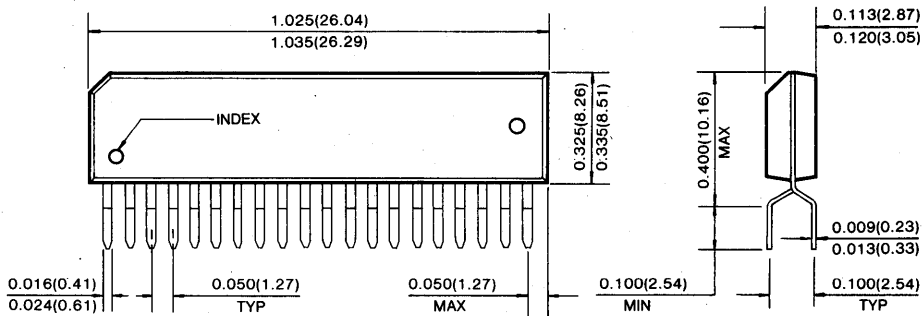
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



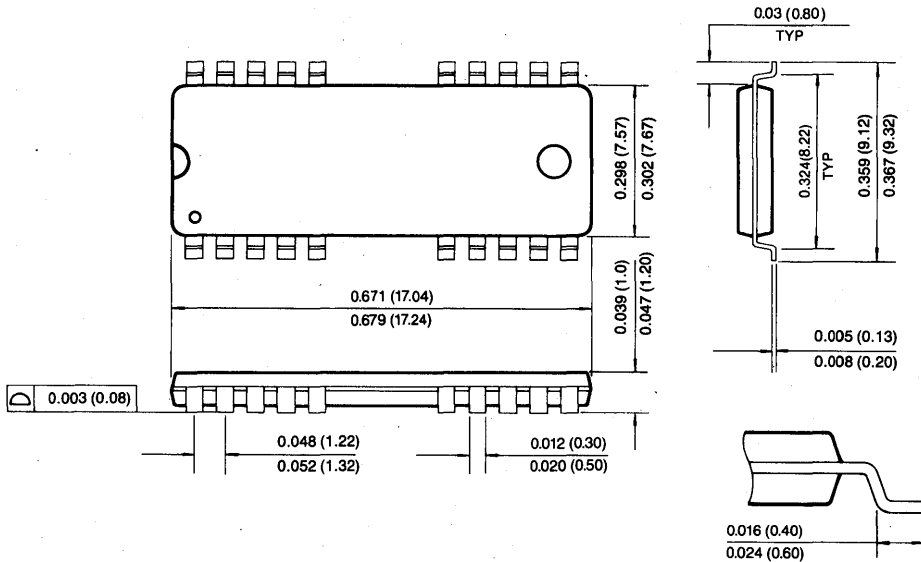
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



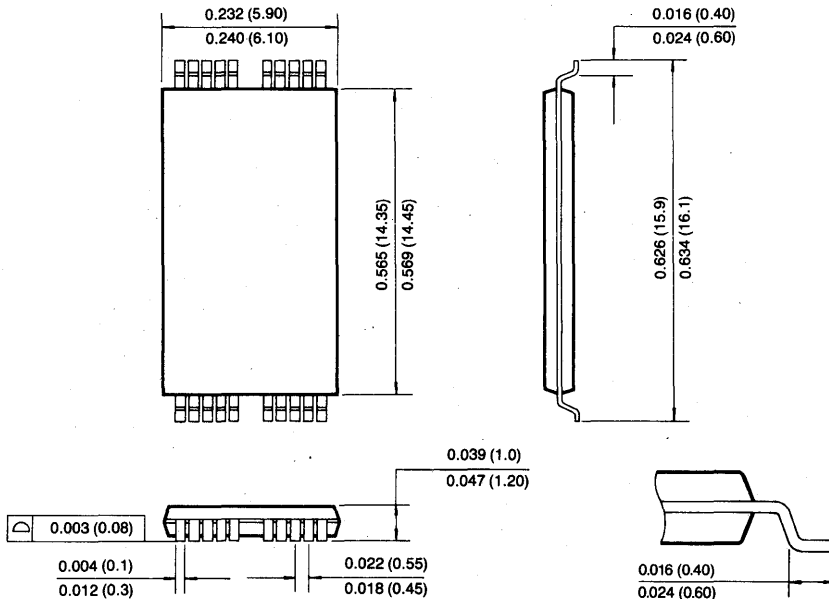
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



1M × 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

- Performance range:

	trAC	tcAC	trc
KM44C1002C-5	50ns	13ns	90ns
KM44C1002C-6	60ns	15ns	110ns
KM44C1002C-7	70ns	20ns	130ns
KM44C1002C-8	80ns	20ns	150ns

- Static Column Mode operation
- \overline{CS} -before- \overline{RAS} refresh capability
- \overline{RAS} -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early Write or Output Enable Controlled Write
- Single +5V ± 10% power supply
- 1024 cycles/16ms refresh
- JEDEC standard pinout
- Available in plastic DIP, SOJ, ZIP and TSOP(II) Packages

GENERAL DESCRIPTION

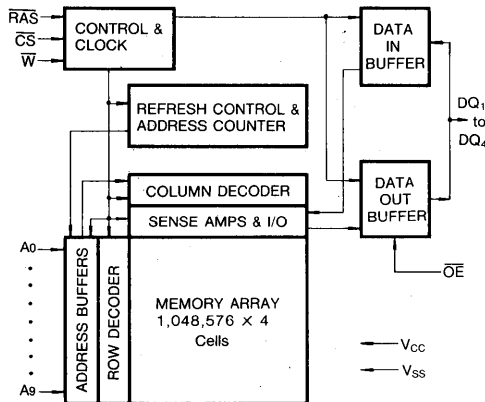
The Samsung KM44C1002C is a CMOS high speed 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

Static Column Mode Operation allows high speed random or sequential access within a row. The KM44C1002C offers high performance while relaxing many critical system timing requirements for fast usable speed.

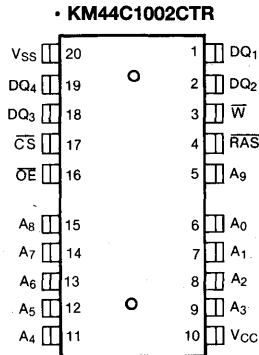
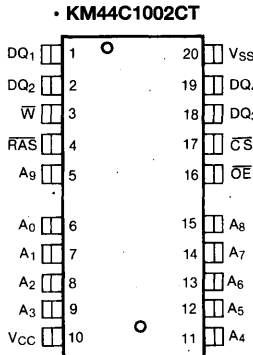
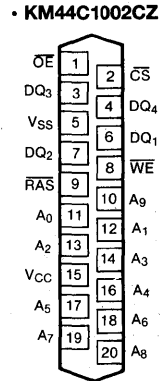
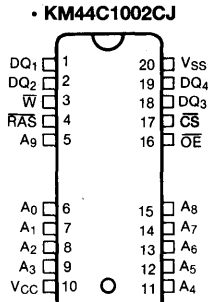
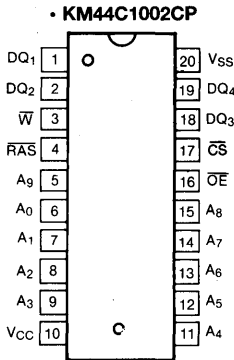
\overline{CS} -before- \overline{RAS} refresh capability provides on-chip auto refresh as an alternative to \overline{RAS} -only refresh. All inputs and outputs are fully TTL compatible.

The KM44C1002C is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Names	Pin Function
A ₀ -A ₉	Address Inputs
RAS	Row Address Strobe
\bar{CS}	Chip Select Input
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
DQ ₁ /DQ ₄	Data In/Data Out
V _{CC}	Power (+ 5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	Vcc + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} and \overline{CS} Cycling @ $t_{RC}=\text{min.}$)	KM44C1002C-5	-	85	mA
	KM44C1002C-6	-	75	mA
	KM44C1002C-7	-	65	mA
	KM44C1002C-8	-	55	mA
Standby Current ($\overline{RAS}=\overline{CS}=\overline{W}=\overline{V_{IH}}$)	I _{CC2}	-	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{CS}=\overline{V_{IH}}$, \overline{RAS} , Address Cycling @ $t_{RC}=\text{min.}$)	KM44C1002C-5	-	85	mA
	KM44C1002C-6	-	75	mA
	KM44C1002C-7	-	65	mA
	KM44C1002C-8	-	55	mA
Standby Column Mode Current* ($\overline{RAS}=\overline{CS}=\overline{V_{IL}}$ Address Cycling @ $t_{PC}=\text{min.}$)	KM44C1002C-5	-	65	mA
	KM44C1002C-6	-	55	mA
	KM44C1002C-7	-	45	mA
	KM44C1002C-8	-	35	mA
Standby Current ($\overline{RAS}=\overline{CS}=\overline{W}=\overline{V_{CC}-0.2V}$)	I _{CC5}	-	1	mA
\overline{CS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CS} Cycling @ $t_{RC}=\text{min.}$)	KM44C1002C-5	-	85	mA
	KM44C1002C-6	-	75	mA
	KM44C1002C-7	-	65	mA
	KM44C1002C-8	-	55	mA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. I_{CC1}, I_{CC3}, I_{CC6} Address can be changed maximum two times while $\overline{RAS}=\overline{V_{IL}}$. In I_{CC4}, Address can be changed maximum once during a static column mode cycle.

CAPACITANCE ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$, $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0\sim A_9$)	CIN1	-	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{CS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$)	CIN2	-	7	pF
Input Capacitance ($\text{DQ1}\sim\text{DQ4}$)	COUT	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C}\leq T_A\leq 70^\circ\text{C}$, $V_{CC}=5.0\text{V}\pm 10\%$, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Static column mode cycle time	tsc	30		35		40		45		ns	
Static column mode read-write cycle time	tsrwc	80		85		100		110		ns	
Access time from $\overline{\text{RAS}}$	trac		50		60		70		80	ns	3,4,11
Access time from $\overline{\text{CS}}$	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
Access time from last write	tALW		50		55		65		75	ns	3
$\overline{\text{CS}}$ to output in Low-Z	tCLZ	0		0		0		0		ns	7
Output buffer turn-off delay	toff	0	13	0	15	0	20	0	20	ns	
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{\text{W}}$	tOW		35		40		45		55	ns	
Transition time (rise and fall)	tr	3	50	3	50	3		3		ns	
$\overline{\text{RAS}}$ precharge time	trp	30		40		50	50	60	50	ns	2
$\overline{\text{RAS}}$ pulse width	trAS	50	10,000	60	10,000	70		80		ns	
$\overline{\text{RAS}}$ pulse width (static column mode)	trASC	50	100,000	60	100,000	70	10,000	80	10,000	ns	
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ hold time	trSH	13		15		20	100,000	20	100,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ hold time	trSH	50		60		70		80		ns	
$\overline{\text{CS}}$ pulse width	tCS	13	10,000	15	10,000	20		20		ns	
$\overline{\text{CS}}$ pulse width (static column mode)	tCSC	13	100,000	15	100,000	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ delay time	trCD	20	37	20	45	20	100,000	20	100,000	ns	
$\overline{\text{RAS}}$ to column address delay time	trAD	15	25	15	30	15	50	15	60	ns	4
$\overline{\text{CS}}$ to $\overline{\text{RAS}}$ precharge time	trCP	5		5		5	35	5	40	ns	11
$\overline{\text{CS}}$ precharge time (static column mode)	tCP	10		10		10		10		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold	tCAH	10		10		15		15		ns	
Write address hold time referenced to $\overline{\text{RAS}}$	tAWR	40		45		55		60		ns	6
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	60		70		80		90		ns	

3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Column address to $\overline{\text{RAS}}$ lead time	trAL	25		30		35		40		ns	
Column address hold time referenced to $\overline{\text{RAS}}$ rise	tAH	5		5		5		5		ns	
Last Write to column address to delay time	tLWAD	20	25	20	25	25	35	25	40	ns	12
Last write to column address hold time	tAHLW	50		60		70		80		ns	
Read command set-up time	trCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CS}}$	trCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		0		ns	9
Write command hold time	twCH	10		15		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	40		50		55		60		ns	6
Write command pulse width	tWP	10		15		15		15		ns	
Write command inactive time	tWI	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		15		20		20		ns	
Write command to $\overline{\text{CS}}$ lead time	tcWL	13		15		20		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		15		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	40		50		55		60		ns	6
Refresh period (1024 cycles)	tREF		16		16		16		16	ms	
Write command set-up time	twCS	0		0		0		0		ms	8
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	tcWD	36		40		50		50		ms	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CS}}$ setup time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CS}}$ hold time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ hold time	trPC	5		5		5		5		ns	
$\overline{\text{CS}}$ precharge time($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ counter test cycle)	tcPT	20		20		25		30		ns	
$\overline{\text{OE}}$ access time	toEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	toED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	toEH	13		15		15		15		ns	

TEST MODE CYCLE

(Note.13)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	95		115		135		155		ns	
Read-modify-write cycle time	t _{RWC}	138		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		55		65		75		85	ns	3,4,11
Access time from $\overline{\text{CS}}$	t _{CAC}		18		20		25		25	ns	3,4,5
Access time from column address	t _{AA}		30		35		40		45	ns	3,11
$\overline{\text{RAS}}$ pulse width	t _{TRAS}	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{\text{CS}}$ pulse width	t _{CSS}	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{TRSH}	18		20		25		25		ns	
$\overline{\text{CS}}$ hold time	t _{CSSH}	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{TRAL}	30		35		40		45		ns	
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	41		45		55		55		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{TRWD}	78		90		105		115		ns	8
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	53		60		70		75		ns	8
Static column mode cycle time	t _{SC}	35		40		45		50		ns	
Static column mode read-modify-write	t _{SRWC}	85		90		105		115		ns	
$\overline{\text{RAS}}$ pulse width (Static column mode)	t _{RASC}	55	100,000	65	100,000	75	100,000	85	100,000	ns	
Access time from last write	t _{ALW}		55		60		70		80	ns	3,12
$\overline{\text{CS}}$ pulse width (static column mode)	t _{CSC}	18	100,000	20	100,000	25	100,000	25	100,000	ns	
$\overline{\text{OE}}$ access time	t _{OEa}		18		25		25		30		
$\overline{\text{OE}}$ to data delay	t _{OED}	18		20		25		25			
$\overline{\text{OE}}$ command hold time	t _{OEh}	18		20		25		25			

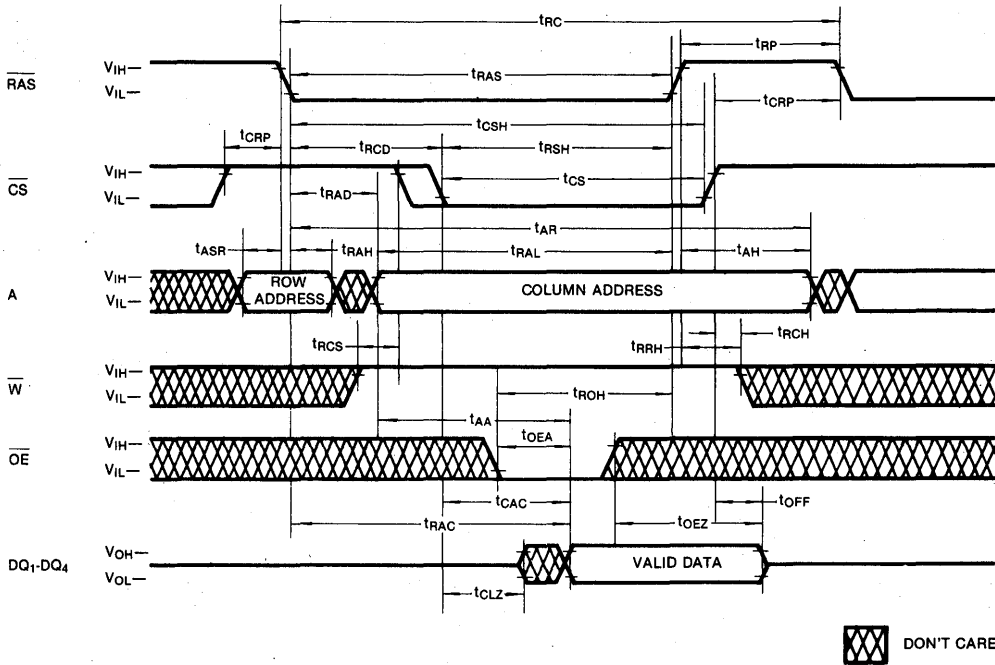
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{CBR}}$ or $\overline{\text{ROR}}$ cycles before proper device operation is achieved.
2. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the t_{RC(Dmax)} limit insures that t_{RAC(max)} can be met. t_{RC(Dmax)} is specified as a reference point only. If t_{RC(D)} is greater than the specified t_{RC(Dmax)} limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RC(D)} > t_{RC(Dmax)}.
6. t_{AWR}, t_{WCR}, t_{DHR} are referenced to t_{RAD(max)}
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{TRWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} > t_{WCS(min)} the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If t_{CWD} > t_{CWD(min)} and t_{TRWD} > t_{TRWD(min)} and t_{AWD} > t_{AWD(min)}, then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the t_{RAD(max)} limit insures that t_{RAC(max)} can be met. t_{RAD(max)} is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD(max)} limit, then access time is controlled by t_{AA}.
12. Operation within the t_{LWAD(max)} limit insures that t_{ALW(max)} can be met. t_{LWAD(max)} is specified as a reference point only. t_{LWAD} is greater than the specified t_{LWAD(max)} limit, then access time is controlled by t_{AA}.
13. These specifications are applied in the test mode.



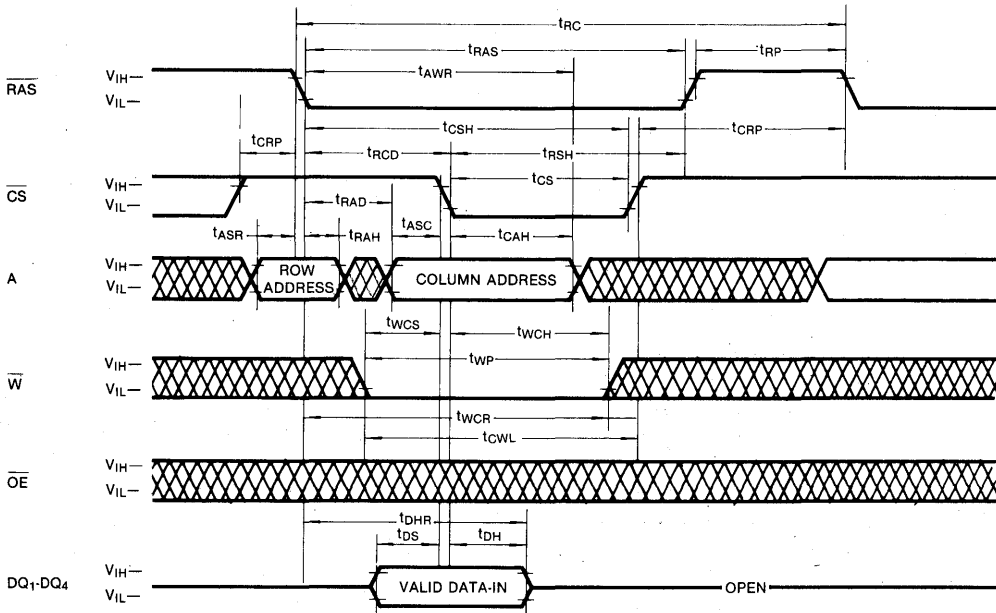
3

TIMING DIAGRAMS
READ CYCLE

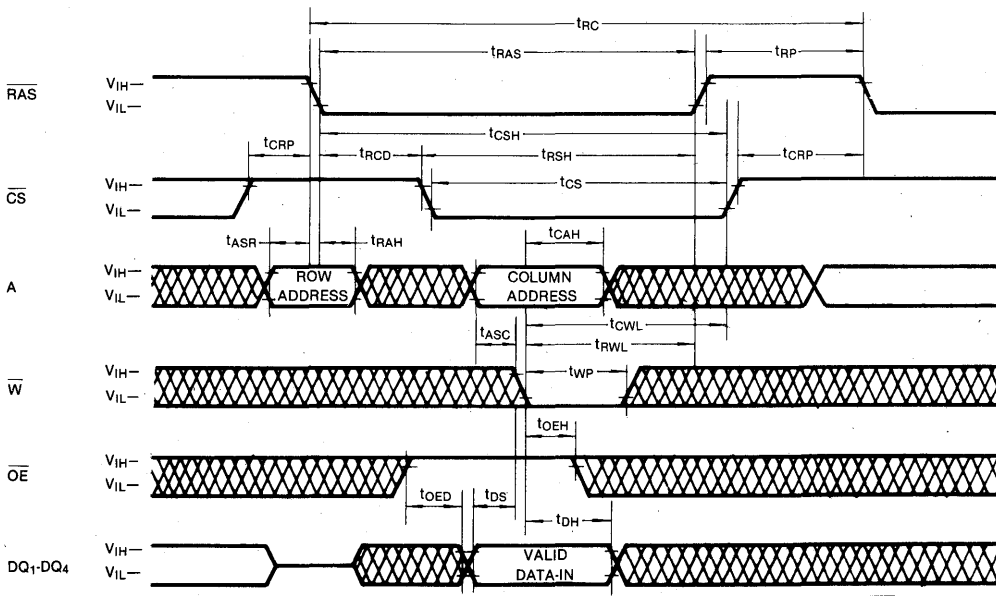


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



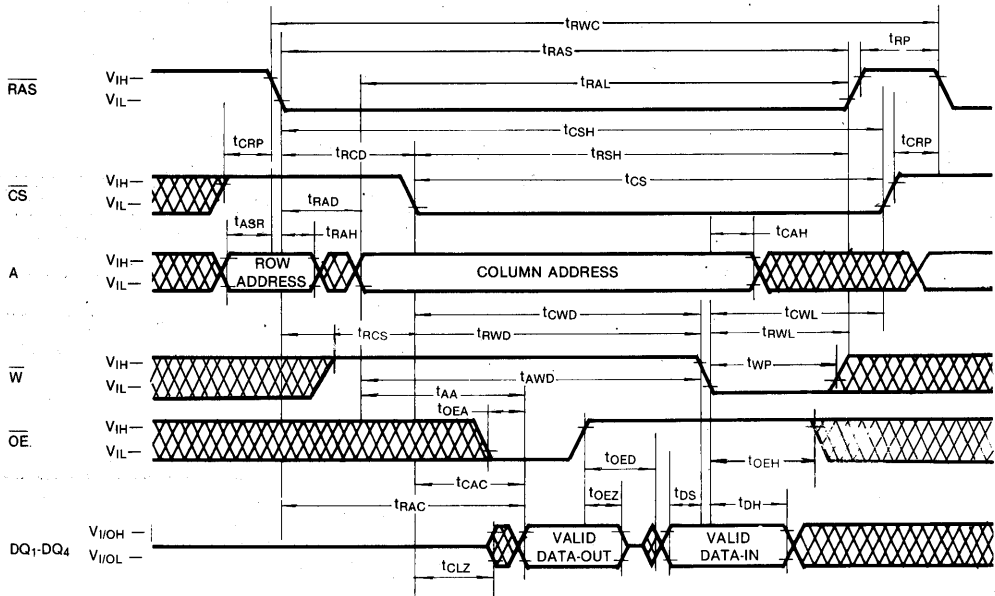
WRITE CYCLE (OE CONTROLLED WRITE)



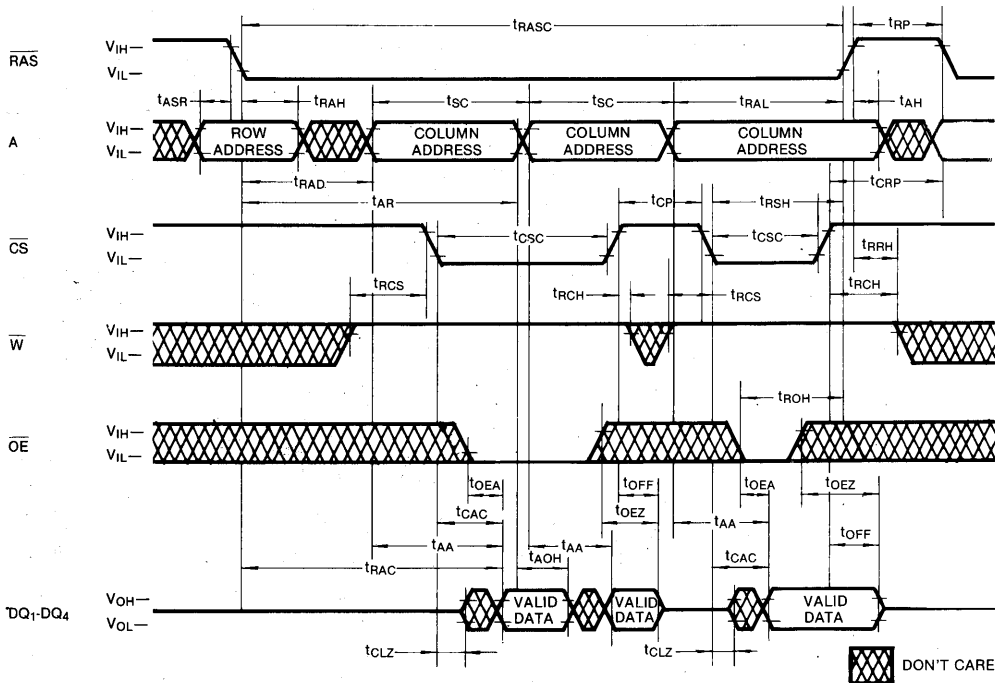
 DON'T CARE

3

TIMING DIAGRAMS (Continued)
READ-WRITE/READ-MODIFY-WRITE CYCLE

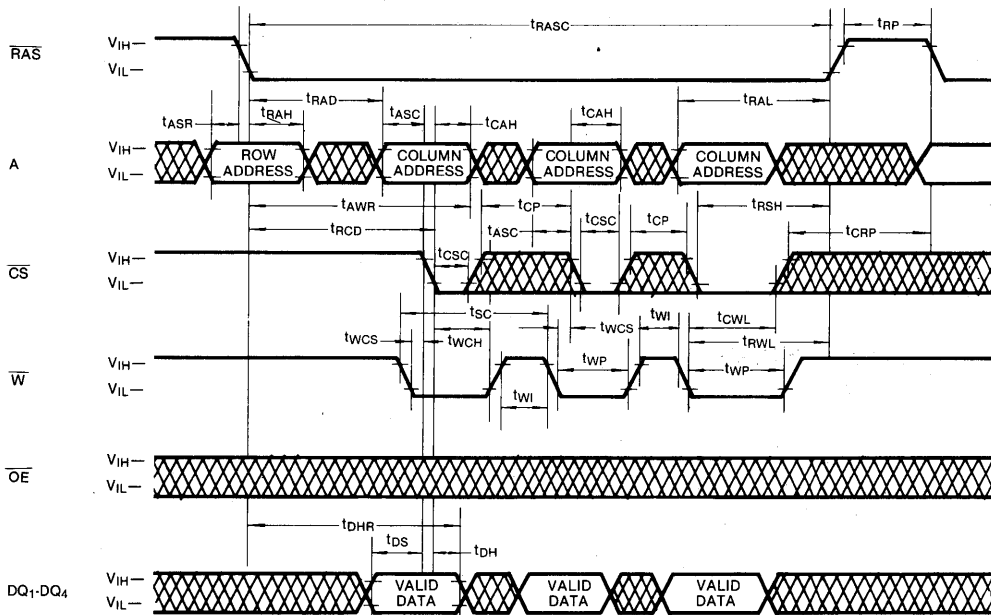


STATIC COLUMN MODE READ CYCLE

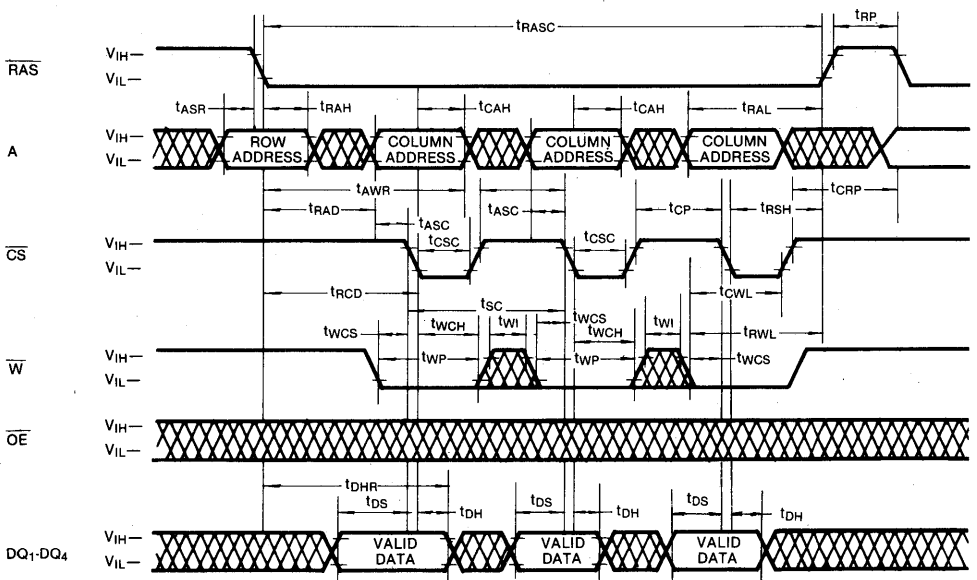


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE (\overline{W} controlled early write)



STATIC COLUMN MODE WRITE CYCLE (\overline{CS} controlled early write)

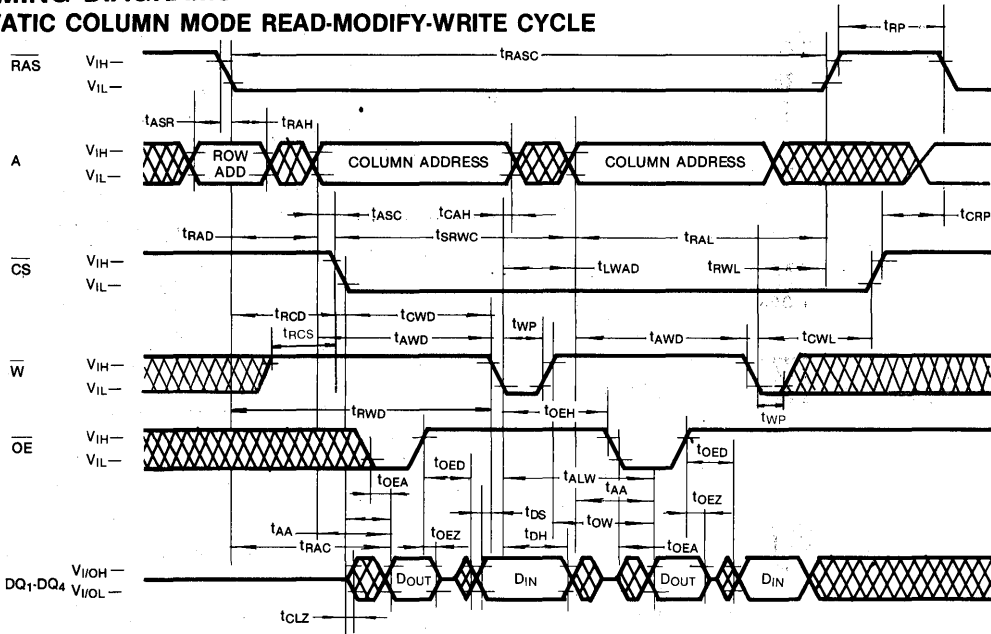


 DON'T CARE

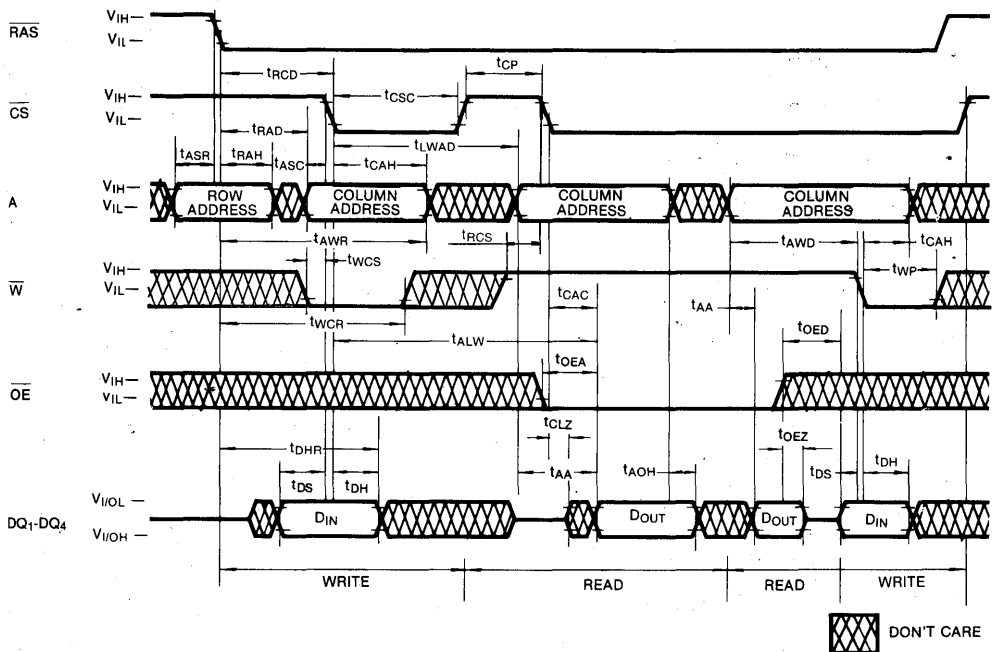
3

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

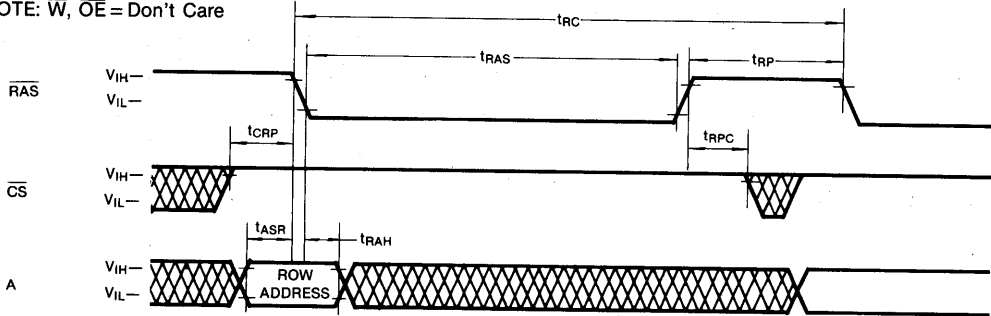


DON'T CARE

TIMING DIAGRAMS (Continued)

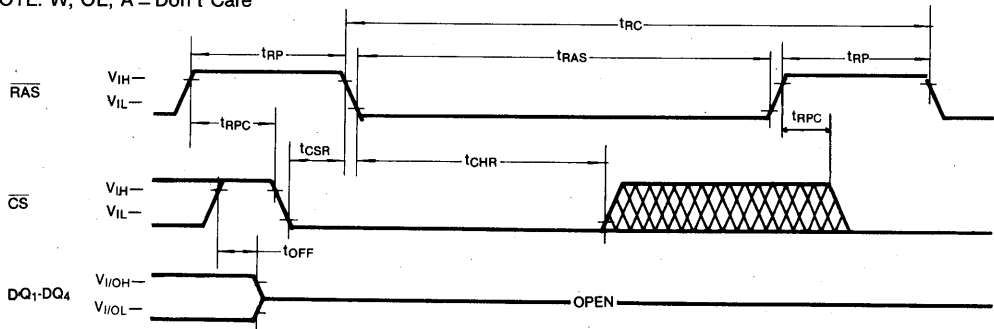
RAS-ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care



\bar{CS} -BEFORE- \bar{RAS} REFRESH CYCLE

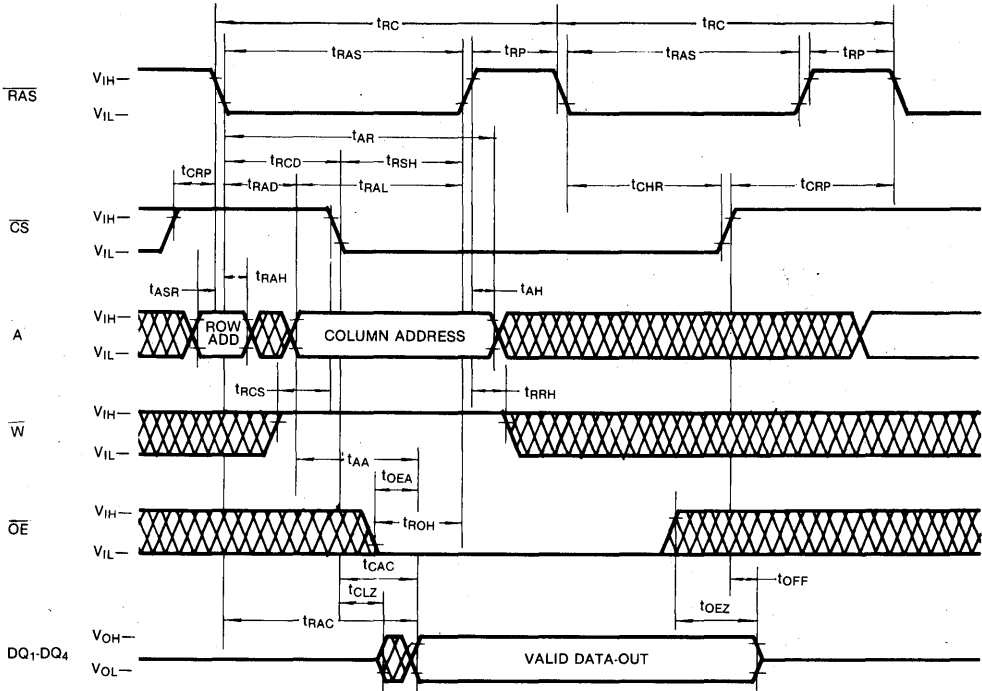
NOTE: \bar{W} , \bar{OE} , A = Don't Care



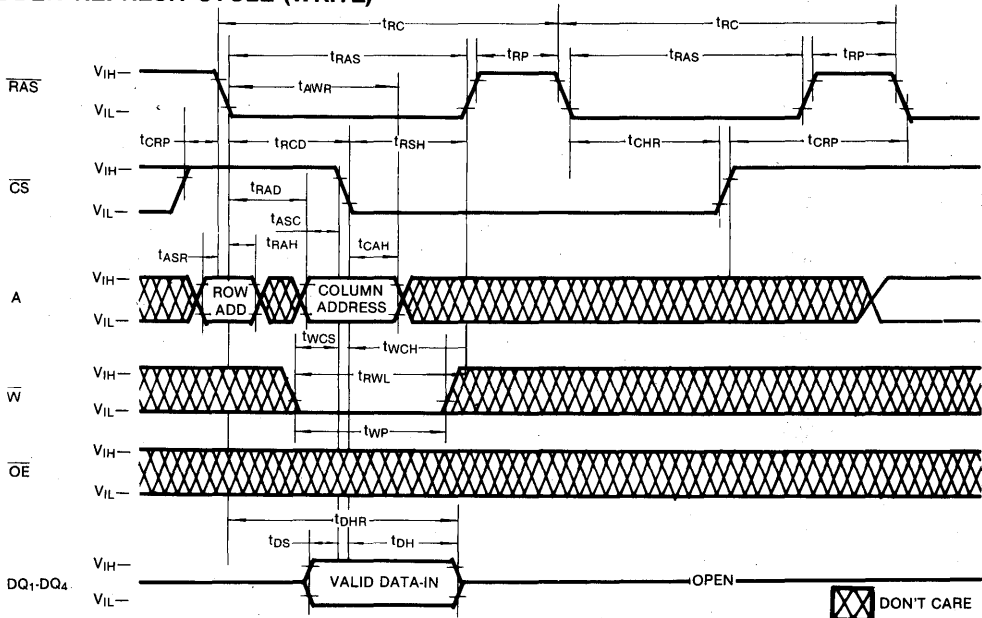
 DON'T CARE

3

TIMING DIAGRAMS (Continued)
HIDDEN REFRESH CYCLE (READ)

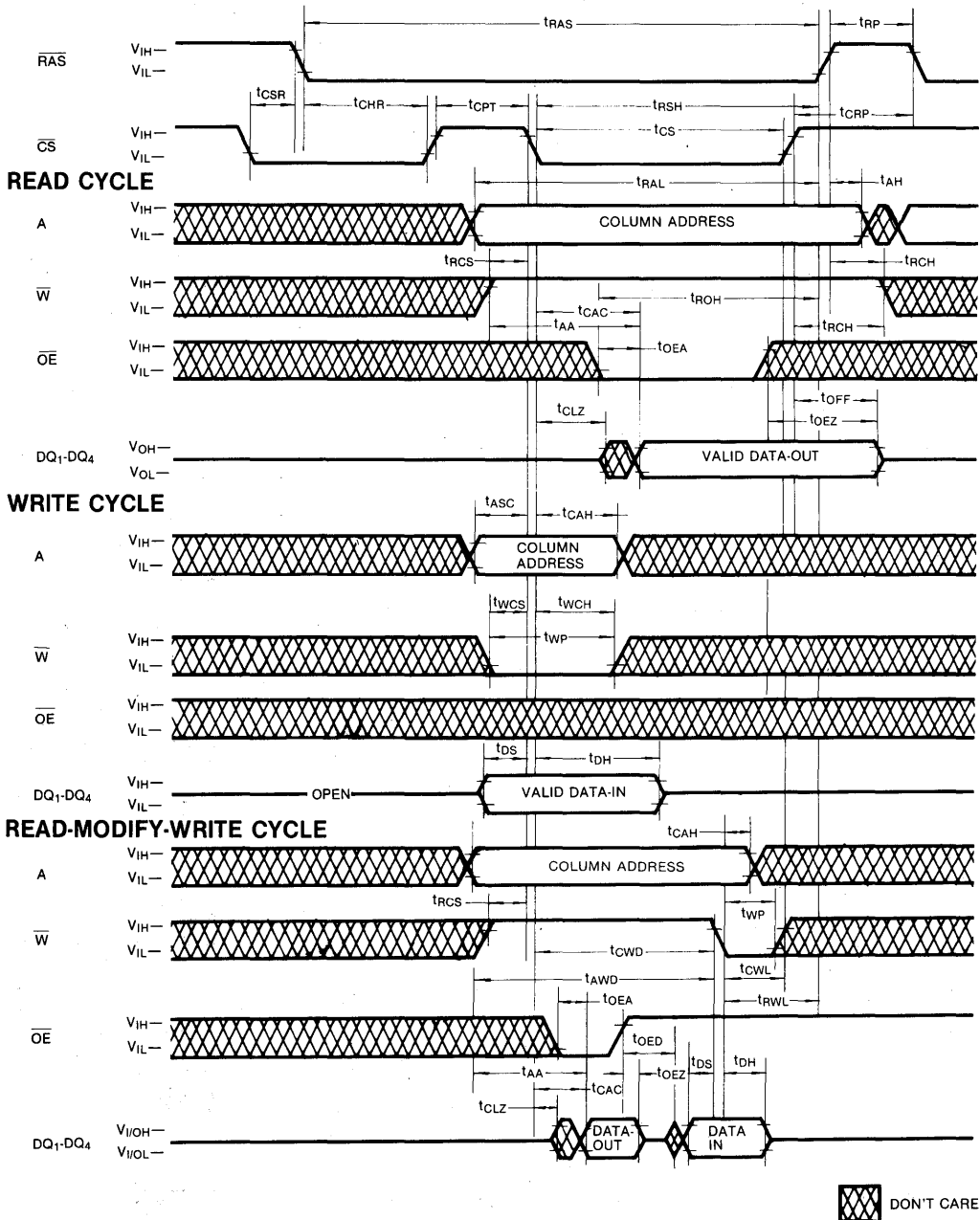


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

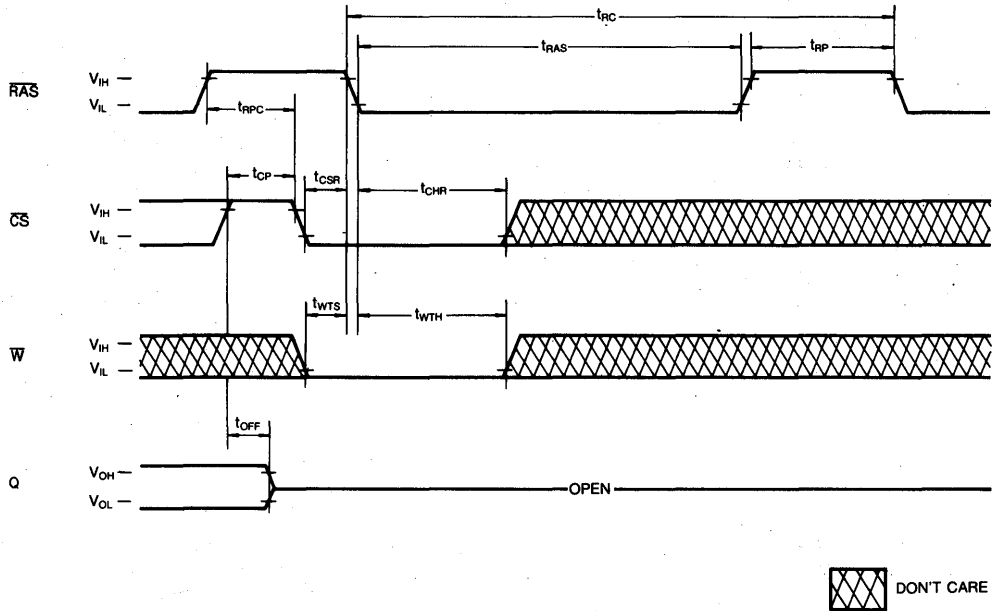


3

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



TEST MODE DESCRIPTION

The KM44C1002C is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would

indicate a "0". In "Test Mode", the 1Mx4 DRAM can be tested as if it were a 512Kx4 DRAM. \bar{W} , \bar{CS} Before \bar{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "CS-Before-RAS Refresh Cycle" or "RAS only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

Device Operation

The KM44C1002C contains 4,194,304 memory locations, organized as 1,048,576 four-bit words. Twenty-two address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1002C has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{\text{RAS}}$), the column address strobe $\overline{\text{CS}}$ and the valid row and column address inputs.

Operation of the KM44C1002C begins by strobing in a valid row address with $\overline{\text{RAS}}$ while $\overline{\text{CS}}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{\text{CS}}$. This is the beginning of any KM44C1002C cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ have returned to the high state. Another cycle can be initiated after $\overline{\text{RAS}}$ remains high long enough to satisfy the $\overline{\text{RAS}}$ precharge time (t_{RP}) requirement.

$\overline{\text{RAS}}$ and $\overline{\text{CS}}$ Timing

The minimum $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ pulse widths are specified by $t_{\text{RAS}}(\text{min})$ and $t_{\text{CS}}(\text{min})$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{\text{RAS}}$ low, it must not be aborted prior to satisfying the minimum $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{\text{RAS}}$ precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1002C begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{\text{WE}}$) high during a $\overline{\text{RAS}}/\overline{\text{CS}}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{\text{RAS}}$. But the access time also depends on the falling edge of $\overline{\text{CS}}$ and on the valid column address transition.

If $\overline{\text{CS}}$ goes low before $t_{\text{RCD}}(\text{max})$ and if the column address is valid before $t_{\text{RAD}}(\text{max})$ then the access time to valid data is specified by $t_{\text{RAC}}(\text{min})$. However, if $\overline{\text{CS}}$ goes low after $t_{\text{RCD}}(\text{max})$ or if the column address becomes valid after $t_{\text{RAD}}(\text{max})$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{\text{RAC}}(\text{min})$, it is necessary to meet both $t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}}(\text{max})$.

The KM44C1002C has common data I/O pins. For this reason and output enable control input ($\overline{\text{OE}}$) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{\text{OE}}$ must be low for the period of time defined by t_{OE} and t_{OZ} .

Write

The KM44C1002C can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{\text{W}}$, $\overline{\text{OE}}$ and $\overline{\text{CS}}$. In any type of write cycle, Data-in must be valid at or before the falling edge of $\overline{\text{W}}$ or $\overline{\text{CS}}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{\text{W}}$ low before $\overline{\text{CS}}$. The 4-bit wide data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remain in the Hi-Z state. In the early write cycle the output buffers remain in the Hi-Z state regardless of the state of the $\overline{\text{OE}}$ input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{\text{W}}$ low after $\overline{\text{CS}}$ and meeting the data sheet read-modify-write cycle timing requirements. The output enable input ($\overline{\text{OE}}$) must be low during the time defined by t_{OE} and t_{OZ} for data to appear at the outputs if t_{CWD} and t_{RDW} are not to the $\overline{\text{OE}}$ timing requirements prevents bus contention on the KM44C1002C's DQ pins.

Data Output

The KM44C1002C has a three-state output buffer which is controlled by $\overline{\text{CS}}$ and $\overline{\text{OE}}$. Whenever $\overline{\text{CS}}$ or $\overline{\text{OE}}$ is high (V_{IH}) the output are in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{\text{CS}}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. This is true even if a new $\overline{\text{RAS}}$ cycle occurs (as in hidden refresh). Each of the KM44C1002C operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Static Column Mode Read, Static Column Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Static Column Mode Write, $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ Refresh, $\overline{\text{CS}}$ -only cycle.

Indeterminate Output State: Delayed Write (tcwd or trwd)

Refresh

The data in the KM44C1002C is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only-Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CS}}$ remains high. This cycle must be repeated for each of the 1024 row address. (A0-A9).

$\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM44C1002C has $\overline{\text{CS}}$ -Before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CS}}$ is held low for the specified set up time (tcsr) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CS}}$ active time and cycling $\overline{\text{RAS}}$. The KM44C1002C hidden refresh cycle is actually $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1002C by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

Power-up

If $\overline{\text{RAS}} = \text{Vss}$ during power-up, the KM44C1002C might begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CS}}$ track with Vcc during power-up or be held at a valid Vih in order to minimize the power-up current.

An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{\text{RAS}}$ cycles. An initialization cycle is any cycle in which $\overline{\text{RAS}}$ is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1002C inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1002C input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C1002C using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1002C and they supply much of the current used by the KM44C1002C during cycling.

DEVICE OPERATION (Continued)

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMS these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on the memory boards to facilitate the shortest possible address and control lines to all the DRAMS.

Decoupling

The importance of proper decoupling can not be over

emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

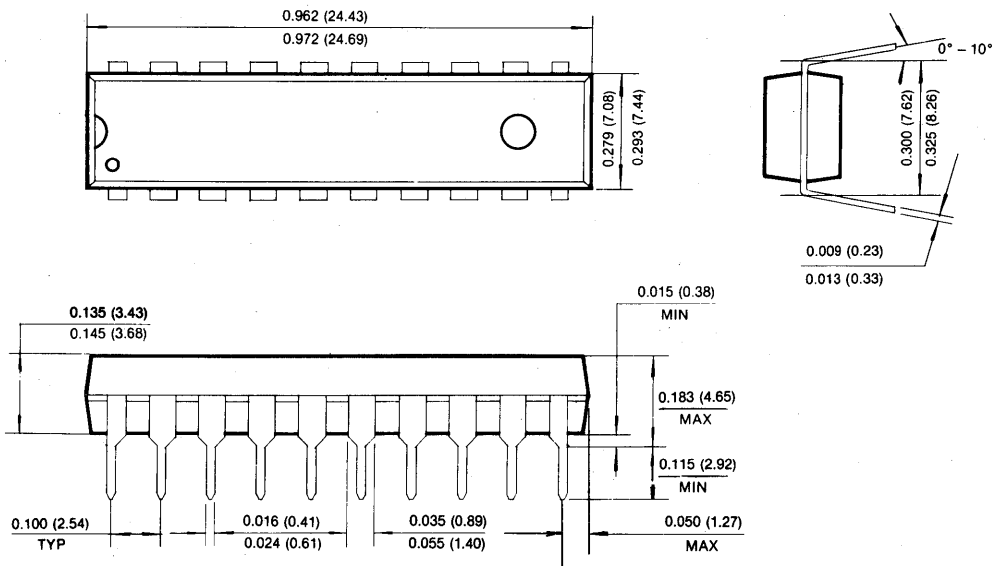
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44C1002B using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1002B and they supply much of the current used by the KM44C1002B during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

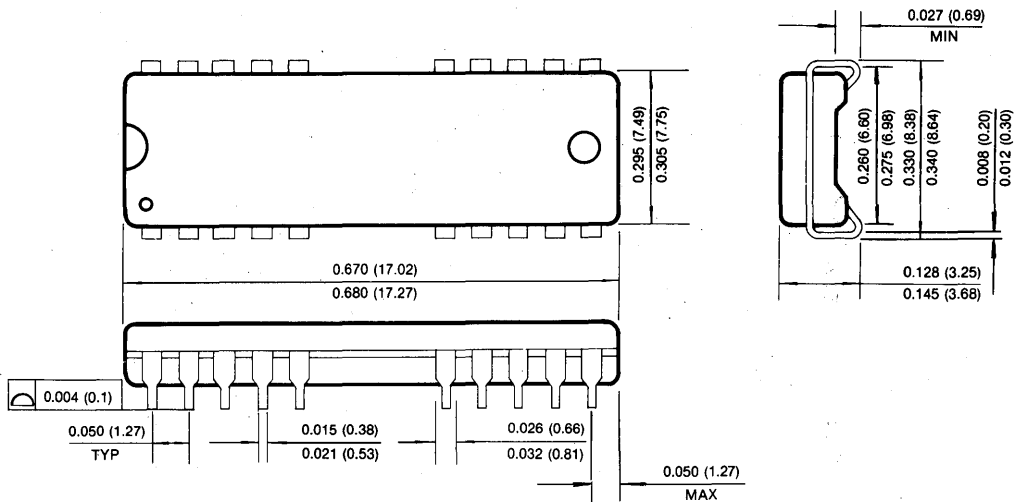
Units: Inches (millimeters)



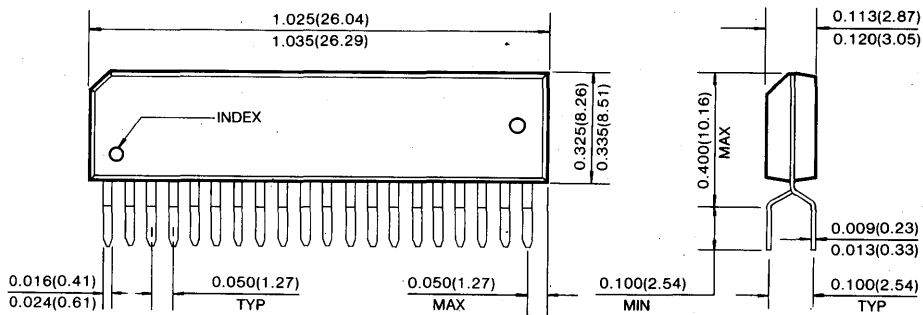
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



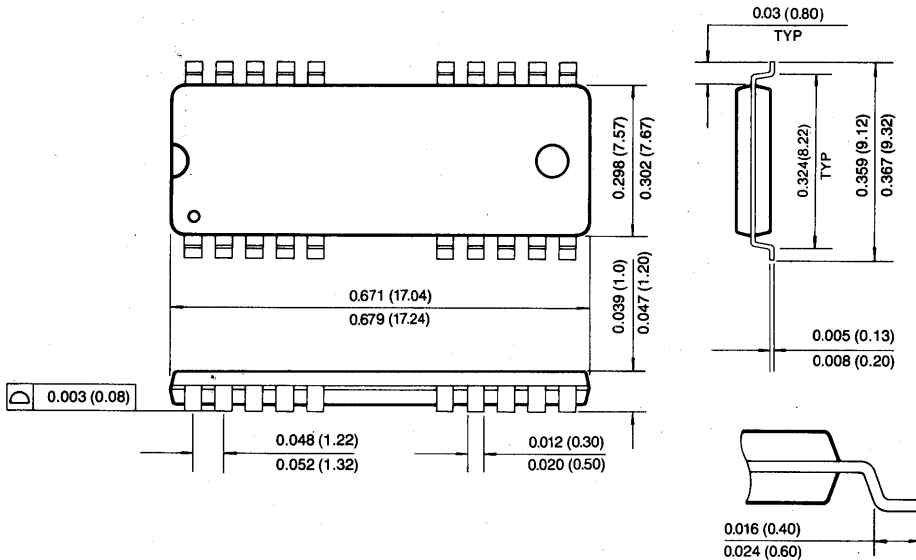
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



3

1M × 4Bit CMOS Quad CAS RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM44C1003C/CL/CSL-5	50ns	13ns	90ns
KM44C1003C/CL/CSL-6	60ns	15ns	110ns
KM44C1003C/CL/CSL-7	70ns	20ns	130ns
KM44C1003C/CL/CSL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single + 5.0V ± 10% power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/256ms (SL-version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
1.1mW (L-version)
0.55mW (SL-version)
 - Active (50/60/70/80) : 468/413/358/303mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP -II packages

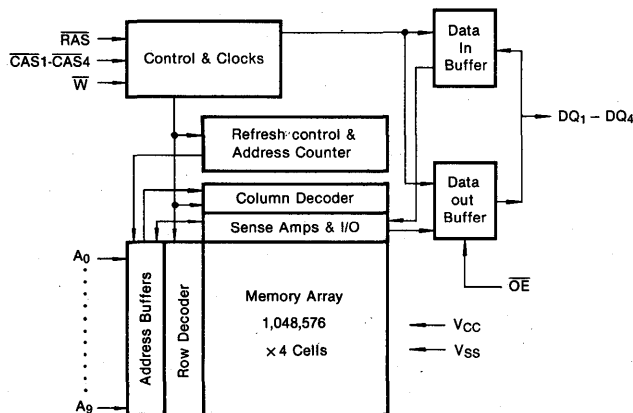
GENERAL DESCRIPTION

The Samsung KM44C1003C/CL/CSL is a CMOS high speed 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM44C1003C/CL/CSL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides in-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible and four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation allowing this device to operate in parity mode.

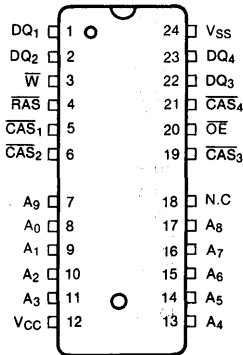
The KM44C1003C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

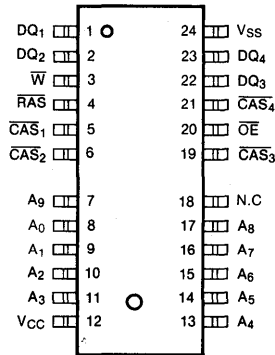


PIN CONFIGURATION (Top Views)

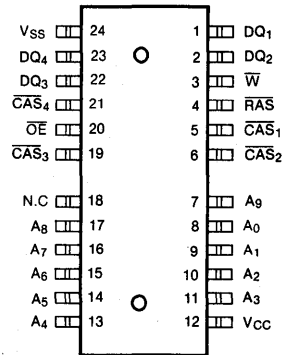
• KM44C1003CJ/CLJ/CSLJ



• KM44C1003CT/CLT/CSLT



• KM44C1003CTR/CLTR/CSLTR



Pin Name	Pin Function
A ₀ -A ₉	Address Inputs
DQ ₁ -DQ ₄	Data In/Out
V _{SS}	Ground
\bar{RAS}	Row Address Strobe
\bar{CAS}_1 - \bar{CAS}_4	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
V _{CC}	Power(+5.0V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	Pd	600	mW
Short Circuit Output Current	I _{os}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	Vcc + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* (\overline{RAS} , \overline{CAS} , Address Cycling @trc=min.)	KM44C1003C/CL/CSL-5	I _{cc1}	-	85	mA
	KM44C1003C/CL/CSL-6		-	75	mA
	KM44C1003C/CL/CSL-7		-	65	mA
	KM44C1003C/CL/CSL-8		-	55	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	KM44C1003C	I _{cc2}	-	2	mA
	KM44C1003CL		-	1	mA
	KM44C1003CSL		-	1	mA
RAS-Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @trc=min.)	KM44C1003C/CL/CSL-5	I _{cc3}	-	85	mA
	KM44C1003C/CL/CSL-6		-	75	mA
	KM44C1003C/CL/CSL-7		-	65	mA
	KM44C1003C/CL/CSL-8		-	55	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @tpc=min.)	KM44C1003C/CL/CSL-5	I _{cc4}	-	65	mA
	KM44C1003C/CL/CSL-6		-	55	mA
	KM44C1003C/CL/CSL-7		-	45	mA
	KM44C1003C/CL/CSL-8		-	35	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{cc}-0.2V$)	KM44C1003C	I _{cc5}	-	1	mA
	KM44C1003CL		-	200	μA
	KM44C1003CSL		-	100	μA
CAS-Before-RAS Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44C1003C/CL/CSL-5	I _{cc6}	-	85	mA
	KM44C1003C/CL/CSL-6		-	75	mA
	KM44C1003C/CL/CSL-7		-	65	mA
	KM44C1003C/CL/CSL-8		-	55	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{CAS}=\overline{CAS}$ -Before- \overline{RAS} Cycling or 0.2V DQ1-DQ4=Don't Care TRC=125 μ S(L-Ver), 250 μ S(SL-Ver), TRAS=TRASmin~300ns	lcc7	-	300 150	μ A μ A
Input Leakage Current (Any input 0 \leq V _{IN} \leq V _{CC} +0.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μ A
Output Leakage Current (Data out is disabled, 0V \leq V _{OUT} \leq V _{CC})	I _{O(L)}	-10	10	μ A
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: lcc1, lcc3, lcc4 and lcc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. lcc is specified as an average current. In lcc1 and lcc3, Address can be changed maximum two times while $\overline{RAS}=\overline{VIL}$. In lcc4, Address can be changed maximum once during a fast page mode cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5.0V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₉)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} 1- \overline{CAS} 4, \overline{W} , \overline{OE})	C _{IN2}	-	7	pF
Output Capacitance (DQ1~DQ4)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C \leq T_A \leq 70°C, V_{CC}=5.0V \pm 0.5V, See notes 1,2)

Test condition : V_{IH}/V_{IL}=2.4/0.8V, V_{OH}/V_{OL}=2.4/0.4V, output loading C_L=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	133		155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		13		15		20		20	ns	3,4,5,19
Access time from column address	t _{AA}		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	0		0		0		0		ns	3,19
Output buffer turn-off delay	t _{OFF}	0	13	0	15	0	20	0	20	ns	7,19
Transition time(rise and fall)	t _r	3	50	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t _{RP}	30		40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	13		15		20		20		ns	17
\overline{CAS} hold time	t _{CSH}	50		60		70		80		ns	18
\overline{CAS} pulse width	t _{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	24
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	37	20	45	20	50	20	60	ns	4,17

AC CHARACTERISTICS (Continued)

Test condition : $V_{in}/V_i=2.4/0.8V$, $V_{oh}/V_{ol}=2.4/0.4V$, output loading $C_L=100pF$

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		5		ns	18
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	17
Column address hold time	tCAH	10		10		15		15		ns	17
Column address hold time referenced to RAS	tAR	40		45		55		60		ns	6
Column address to RAS lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	17
Read command hold time referenced to CAS	tRCH	0		0		0		0		ns	9,18
Read command hold time referenced to RAS	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	25
Write command hold time referenced to RAS	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to RAS lead time	tRWL	13		15		20		20		ns	
Write command to CAS lead time	tCWL	13		15		20		20		ns	18
Data set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		15		15		15		ns	10
Data-in hold time referenced to RAS	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8,17
CAS to W delay time	tCWD	36		40		50		50		ns	8,17
RAS to W delay time	tRWD	73		85		100		110		ns	8
Column address to W delay time	tAWD	48		55		65		70		ns	8
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	17
CAS hold time(CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	18
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		20		25		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3,19
Fast page mode cycle time	tPC	35		45		45		50		ns	20
Fast page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	20
CAS precharge time	tCP	10		10		10		10		ns	21
RAS pulse width(Fast Page Mode)	tRASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	22

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
\overline{OE} to data delay	toED	13		15		20		20		ns	23
Output buffer turn off delay time from \overline{OE}	toEZ	0	13	0	15	0	20	0	20	ns	
\overline{OE} command hold time	toEH	13		15		20		20		ns	
Write command set-up time (test mode in)	twTS	10		10		10		10		ns	
Write command hold time (test mode in)	twPH	10		10		10		10		ns	
\overline{W} to \overline{RAS} precharge time(\overline{C} -B- \overline{R} cycle)	twRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time(\overline{C} -B- \overline{R} cycle)	twRH	10		10		10		10		ns	
Hold time \overline{CAS} low to \overline{CAS} high	tcLCH	5		5		5		5		ns	15,26

TEST MODE CYCLE

(Note.12)

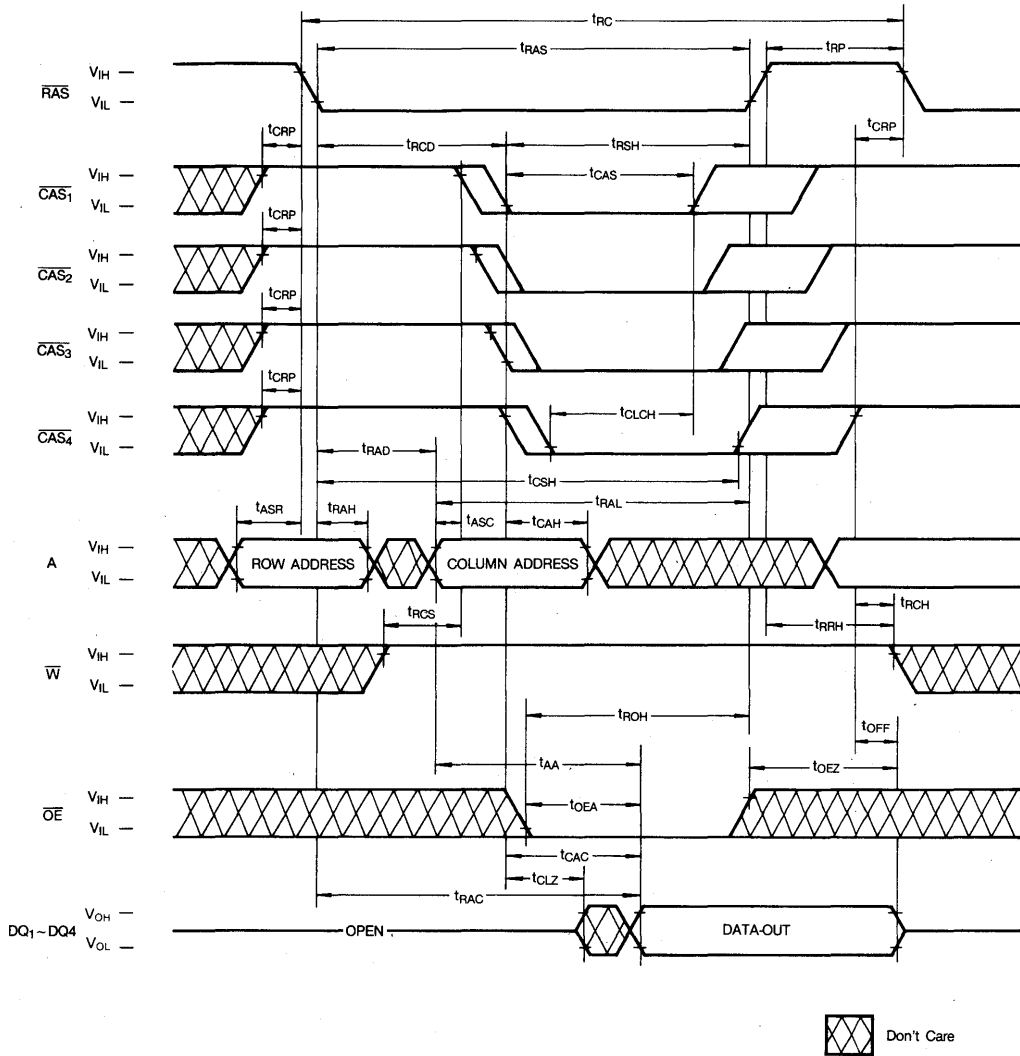
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from \overline{RAS}	trAC		60		65		75		85	ns	3,4,11,13
Access time from \overline{CAS}	tcAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
\overline{RAS} pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	tcAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	18		20		25		25		ns	
\overline{CAS} hold time	tcSH	55		65		75		85		ns	
Column address to \overline{RAS} lead time	trAL	30		35		40		45		ns	
\overline{CAS} to \overline{W} delay time	tcWD	41		45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	78		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tpc	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tpRWC	81		90		100		105		ns	
\overline{RAS} pulse width (Fast Page Mode)	trASP	55		65	200,000	75	200,000	85	200,000	ns	
Access time from \overline{CAS} precharge	tcPA	35		40		45		50		ns	3
\overline{OE} access time	toEA	18		20		25		25		ns	
\overline{OE} to data delay	toED	18		20		25		25		ns	
\overline{OE} command hold time	toEH	18		20		25		25		ns	

3

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only Refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\text{max})$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. In order to hold the address latched by the first $\overline{\text{CAS}} \times$ going low, the parameter t_{CLCH} must be met.
16. If at least one $\overline{\text{CAS}}$ is low at the falling edge of $\overline{\text{RAS}}$, $\overline{\text{DQ}}$ will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, all four $\overline{\text{CAS}}$ must be pulsed high for t_{CP} .
17. The first $\overline{\text{CAS}} \times$ edge to transition low.
18. The last $\overline{\text{CAS}} \times$ edge to transition low.
19. Output parameter is referenced to corresponding $\overline{\text{CAS}} \times$ input.
20. Last rising $\overline{\text{CAS}} \times$ edge to next cycle's last rising $\overline{\text{CAS}} \times$ edge.
21. Last rising $\overline{\text{CAS}} \times$ edge to first falling $\overline{\text{CAS}} \times$ edge.
22. First $\overline{\text{DQ}} \times$ controlled by the first $\overline{\text{CAS}} \times$ to go low.
23. Last $\overline{\text{DQ}} \times$ controlled by the first $\overline{\text{CAS}} \times$ to go low.
24. Each $\overline{\text{CAS}} \times$ must meet minimum pulse width.
25. Last $\overline{\text{CAS}} \times$ to go low.
26. The last falling $\overline{\text{CAS}} \times$ edge to the first rising $\overline{\text{CAS}} \times$ edge.

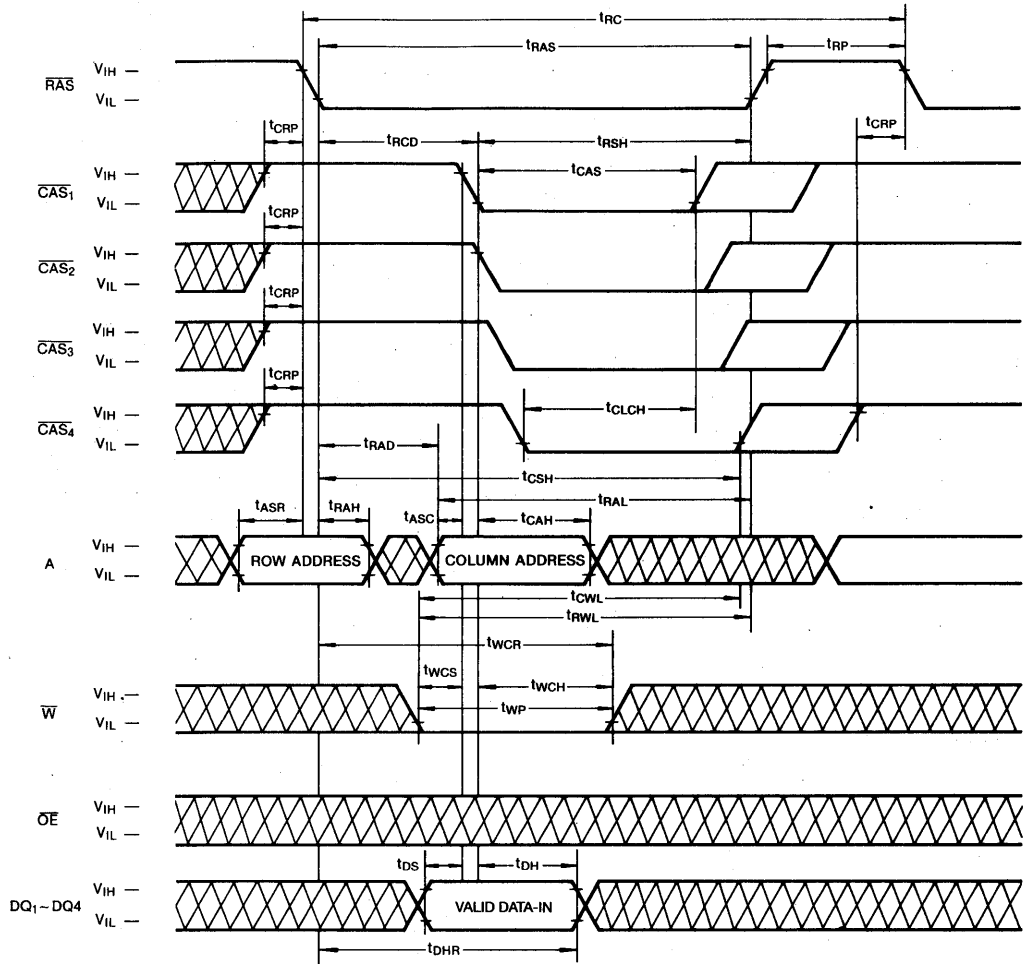
TIMING DIAGRAM
READ CYCLE



3

TIMING DIAGRAM (Continued)

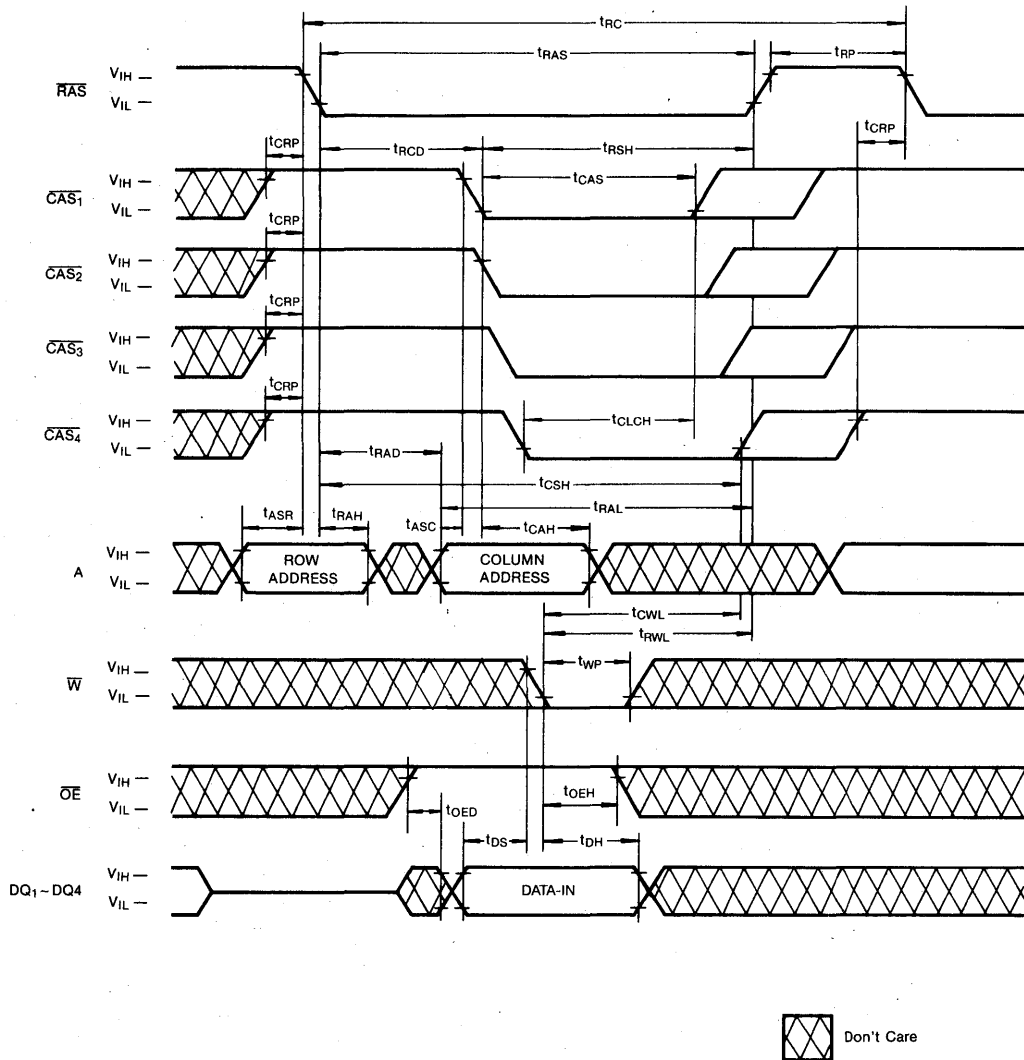
WRITE CYCLE (EARLY WRITE)



 Don't Care

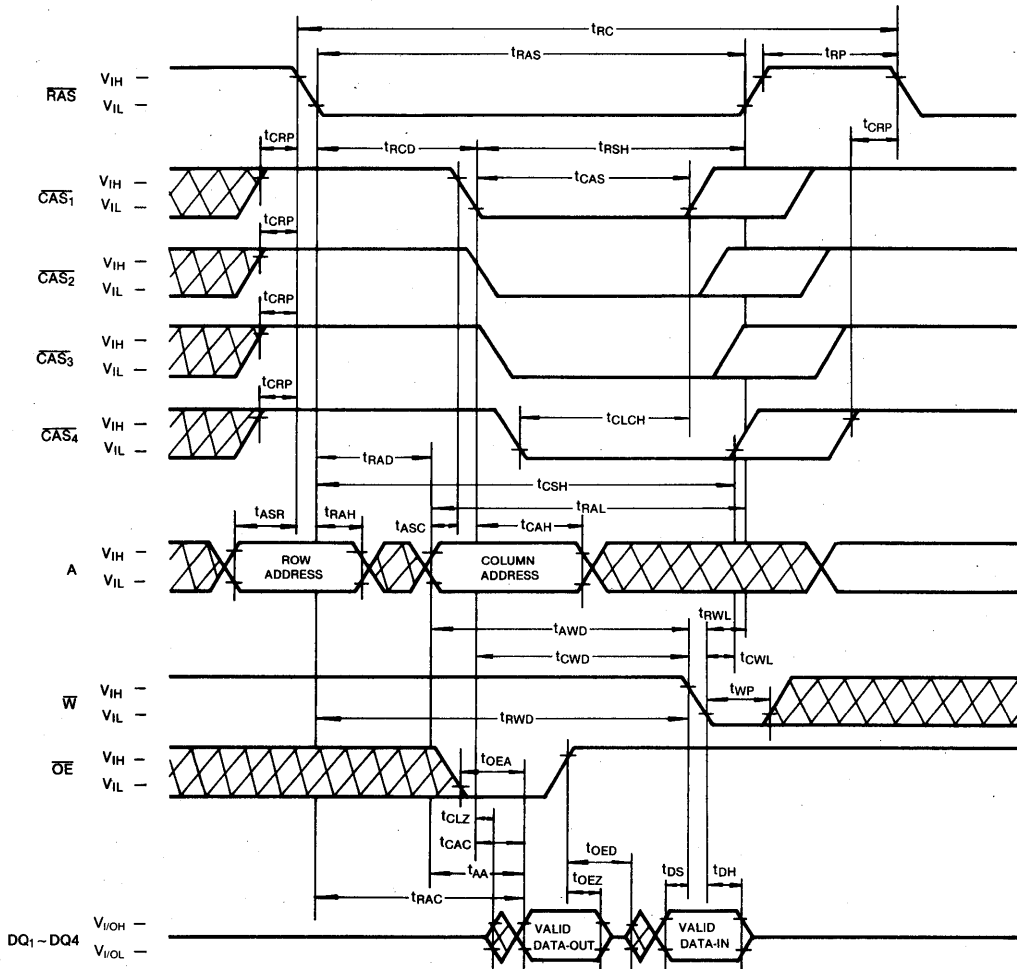
TIMING DIAGRAM (Continued)

WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



3

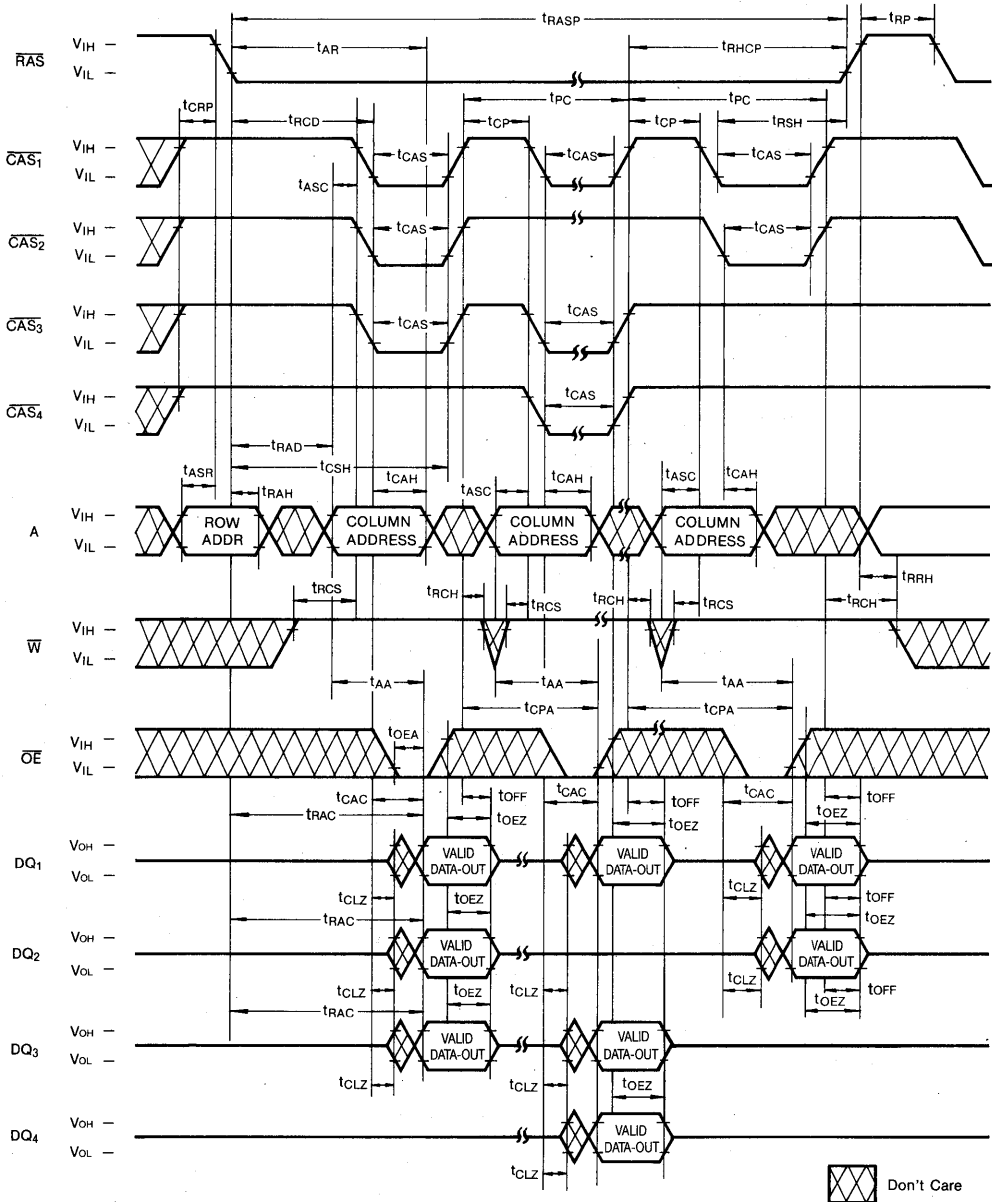
TIMING DIAGRAM (Continued)
READ-MODIFY-WRITE CYCLE



 Don't Care

TIMING DIAGRAM (Continued)

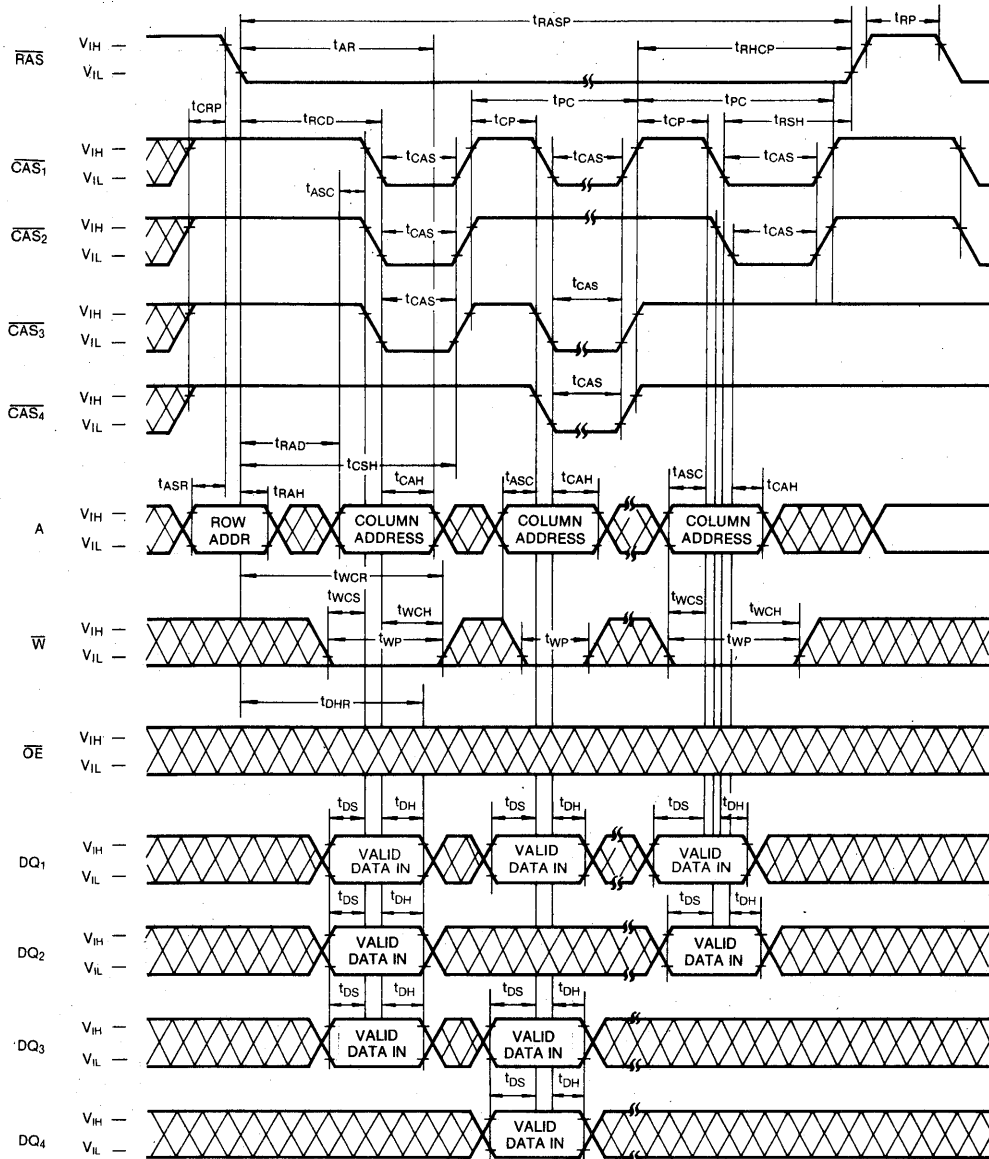
FAST PAGE MODE READ CYCLE



3

TIMING DIAGRAM (Continued)

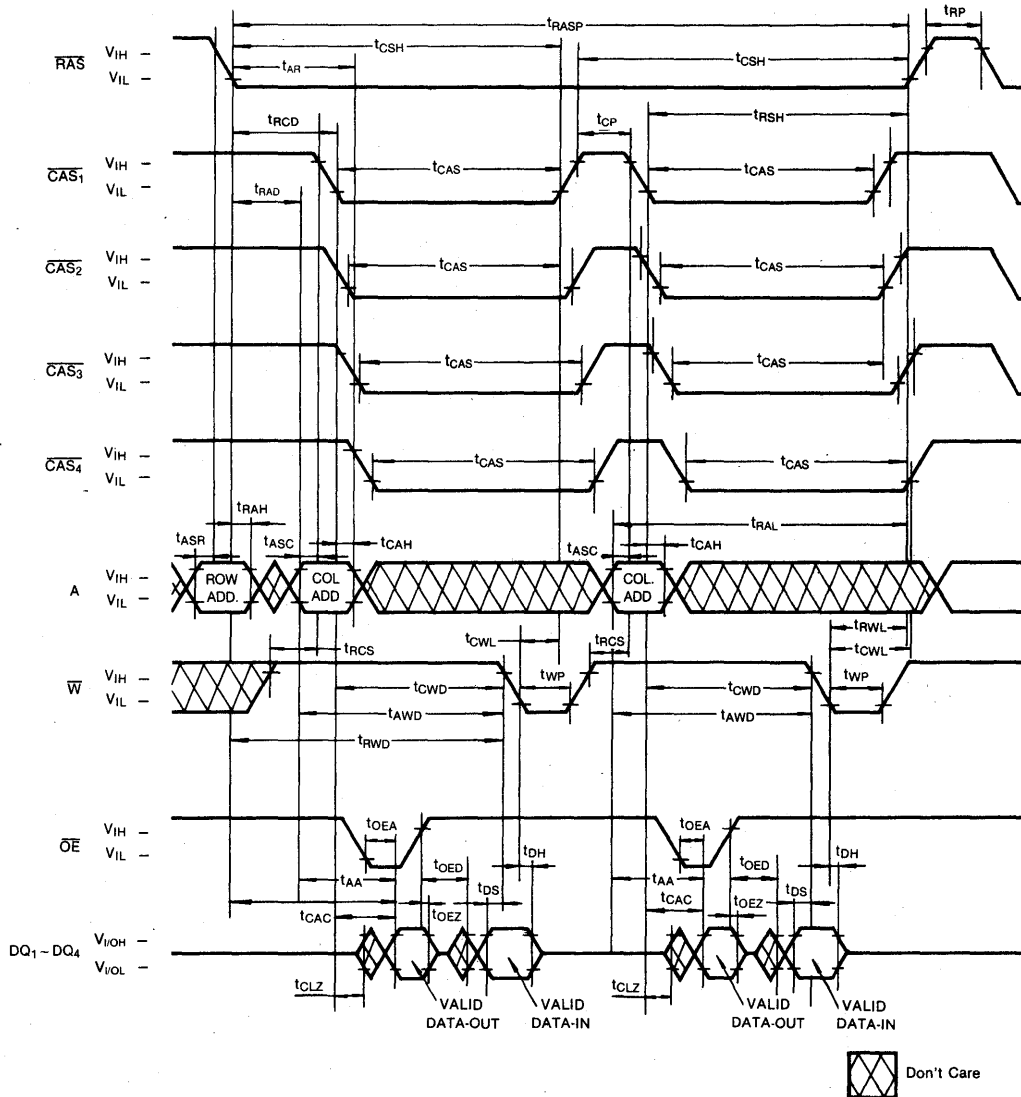
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



 Don't Care

TIMING DIAGRAM (Continued)

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

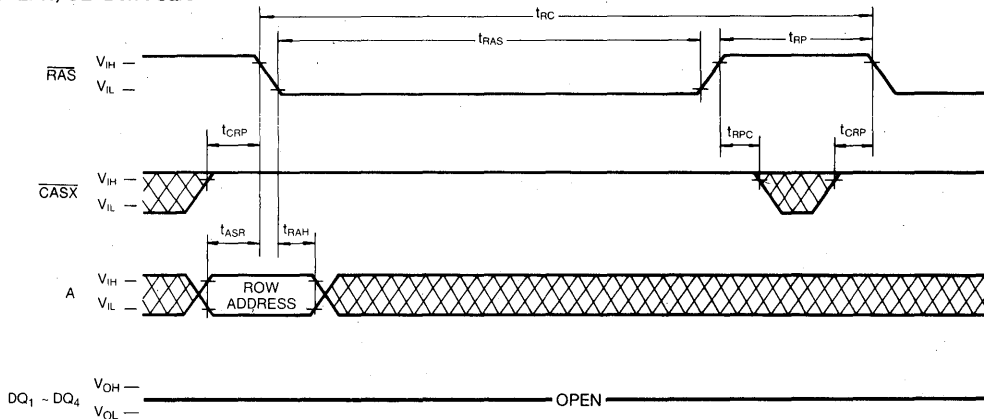


3

TIMING DIAGRAMS (Continued)

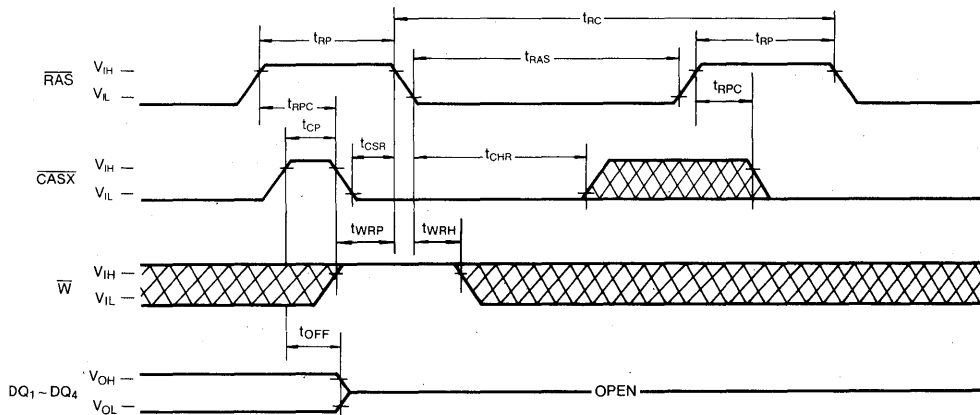
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

NOTE: $\overline{\text{W}}$, $\overline{\text{OE}}$ =Don't Care



$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH CYCLE

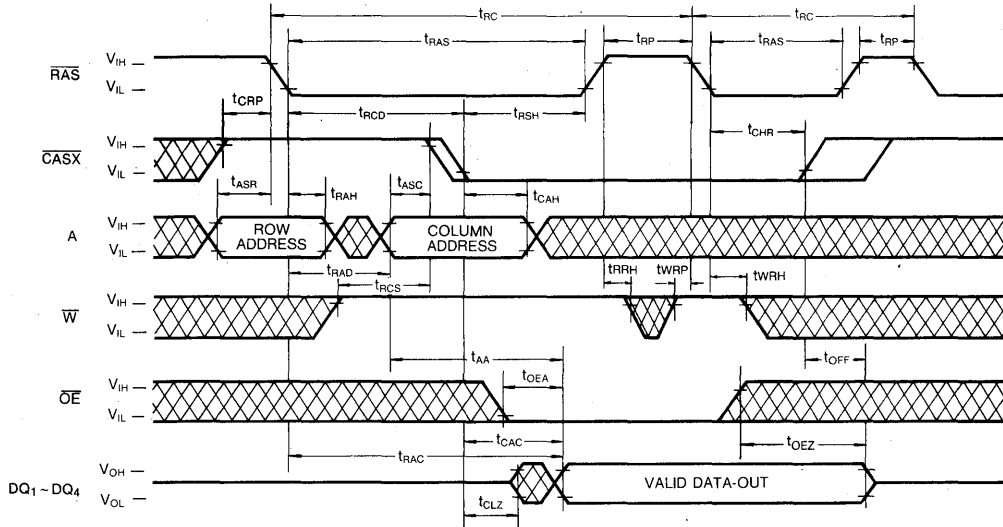
NOTE: $\overline{\text{W}}$, $\overline{\text{OE}}$, A = Don't Care



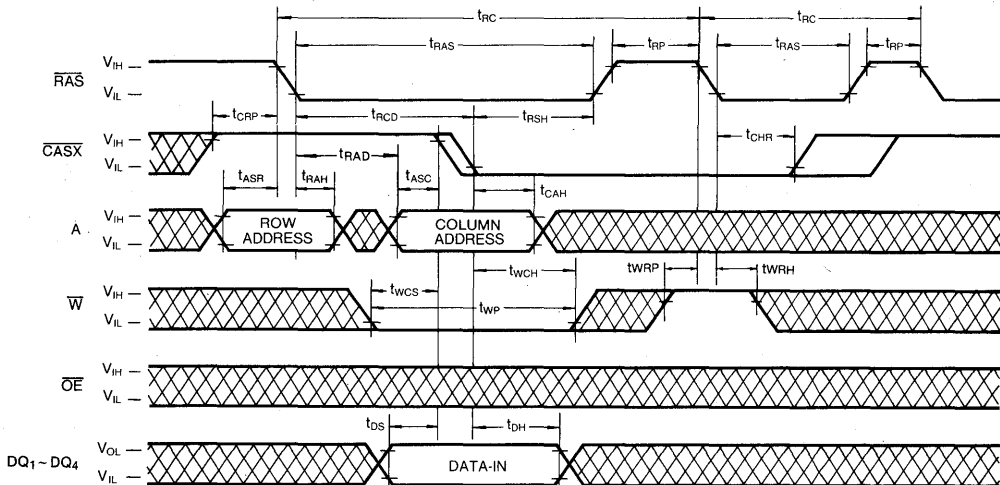
 DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

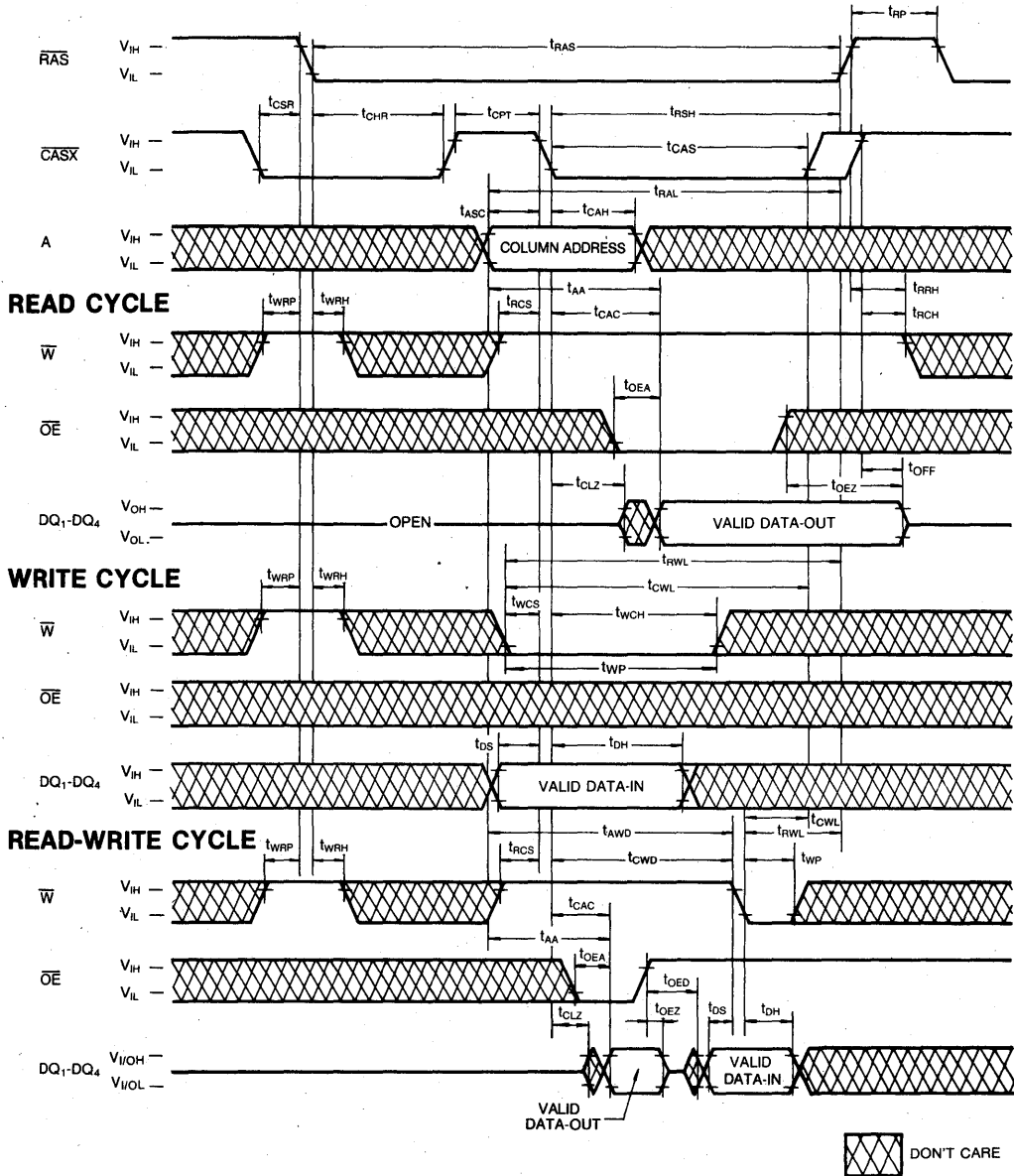


 DON'T CARE

3

TIMING DIAGRAMS (Continued)

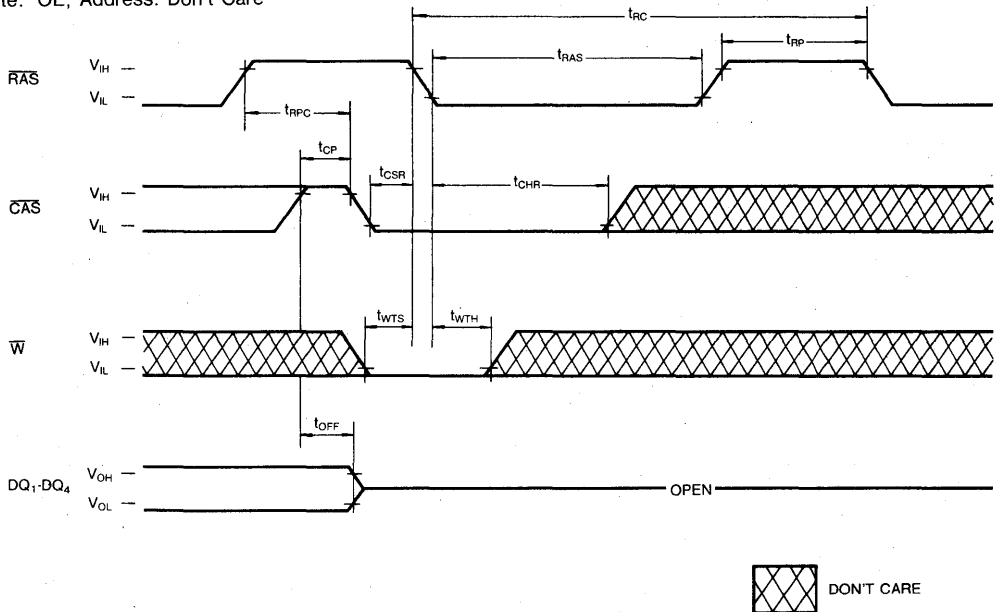
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



3

TEST MODE DESCRIPTION

The KM44C1003C/CL/CSL is the RAM organized 1,048,576 words by 4 bit, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would

indicate a "0". In "Test Mode", the $1M \times 4$ DRAM can be tested as if it were a $512K \times 4$ DRAM. \overline{W} , \overline{CAS} -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " \overline{CAS} -BEFORE- \overline{RAS} REFRESH CYCLE" or " \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

The KM44C1003C/CL/CSL contains 4,194,304 memory locations. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1003C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0-A_9) and 10 column ($A_{10}-A_{19}$) addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CASx}) and the valid row and column address inputs.

Operating of the KM44C1003C/CL/CSL begins by strobing in a valid row address with \overline{RAS} while \overline{CASx} remains high. Then the address on the 10 address input pins (A_0-A_9) is changed from a row address to a column address and is strobed in by \overline{CASx} . This is the beginning of any KM44C1003C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CASx} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

RAS and CASx Timing

The minimum \overline{RAS} and \overline{CASx} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CASx} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1003C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during a $\overline{RAS}/\overline{CASx}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CASx} and on the valid column address transition.

If \overline{CASx} goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAC(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However, if \overline{CASx} goes low after $t_{RCD(max)}$ or if the column address becomes valid after $t_{RAC(max)}$, access is specified by t_{CAC} or t_{CAA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAC(max)}$. The KM44C1003C/CL/CSL has common data I/O pins. The this reason an output enable control

input (\overline{OE}) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, \overline{OE} must be low for the period of time defined by t_{OE} and t_{OEZ} .

Write

The KM44C1003C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} and \overline{CASx} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CASx} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CASx} . The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CASx} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If \overline{W} is brought low after \overline{CASx} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} , t_{OWD} and t_{AWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1003C/CL/CSL has a three-state output buffers which is controlled by \overline{CASx} and \overline{OE} . Whenever \overline{CASx} and \overline{OE} are high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CASx} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{CAA} specify when the valid data will be present at the output. The valid data remains at the output until \overline{CASx} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM44C-1003C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

DEVICE OPERATION (Continued)

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Fast Page Mode Write, $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ Refresh, $\overline{\text{OE}}$ controlled write.

Indeterminate Output State: Delayed Write (tcwd or trwd are not met)

Refresh

The data in the KM44C1003C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16ms. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CASx}}$ remains high. This cycle must be repeated for each row.

$\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM44C1003C/CL/CSL has $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CASx}}$ is held low for the specified set up time (tcsr) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CASx}}$ active time and cycling $\overline{\text{RAS}}$. The KM44C1003C/CL/CSL hidden refresh cycle is actually a $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1003C/CL/CSL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in the row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a

selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{\text{RAS}}$ is kept low to maintain the $\overline{\text{CASx}}$ is cycled to strobe in additional column address. This eliminates the time required to set up and strobe sequential row addresses for the same page.

 $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry.

After the $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ refresh operation, is $\overline{\text{CASx}}$ goes high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address — Bits A_0 through A_9 are supplied by the falling edge of $\overline{\text{CASx}}$ as in a normal memory cycle.

Suggested $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ Counter Test Procedure

The $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle timing is used in each of the following steps.

1. Initialize the internal refresh counter by performing 8 $\overline{\text{CASx}}$ -before- $\overline{\text{RAS}}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4.

Power-up

If $\overline{\text{RAS}} = V_{SS}$ during power-up, the KM44C1003C/CL/CSL could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CASx}}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

DEVICE OPERATION (Continued)

An initial pause of 200 μ sec is required after power-up followed by any 8 RAS cycles before proper device operation is assured. Eight initialization cycles are also required after any 64 msec period in which there are no RAS cycles. An initialization cycle is any cycle in which RAS is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1003C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1003C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The

impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

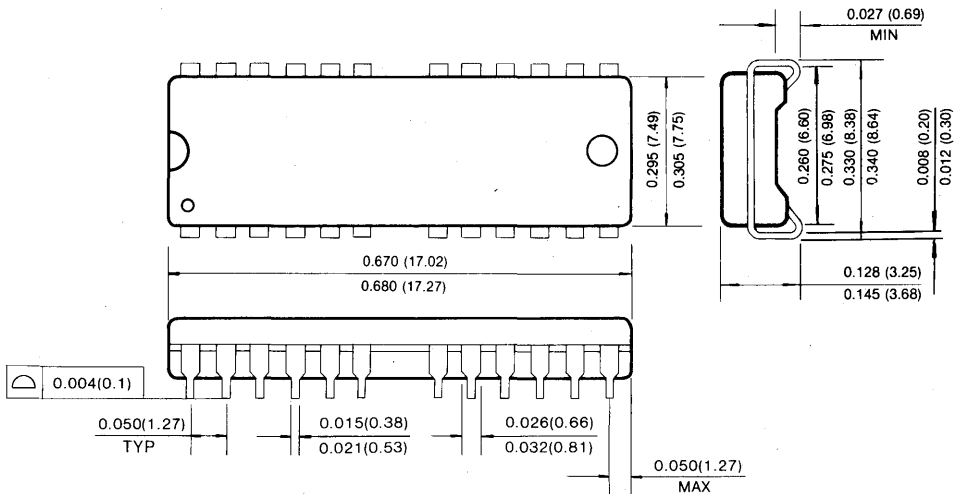
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C1003C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1003C/CL/CSL and they supply much of the current used by the KM44C1003C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

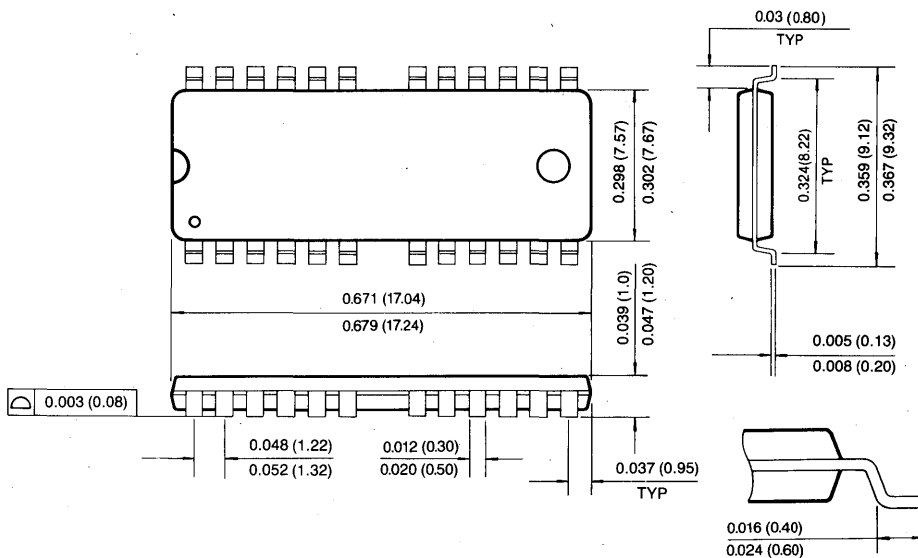
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



1M × 4Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trC	tHPC
KM44C1004C/CL/CSL-5	50ns	13ns	90ns	20ns
KM44C1004C/CL/CSL-6	60ns	15ns	110ns	24ns
KM44C1004C/CL/CSL-7	70ns	20ns	130ns	29ns
KM44C1004C/CL/CSL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- CAS-before-RAS refresh capability
- RAS-only and hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single + 5.0V ± 10% power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/256ms (SL-version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
1.1mW (L-version)
0.55mW (SL-version)
 - Active (50/60/70/80): 468/413/358/303mW
- JEDEC standard pinout
- Available in plastic DIP,SOJ,ZIP and TSOP -II packages

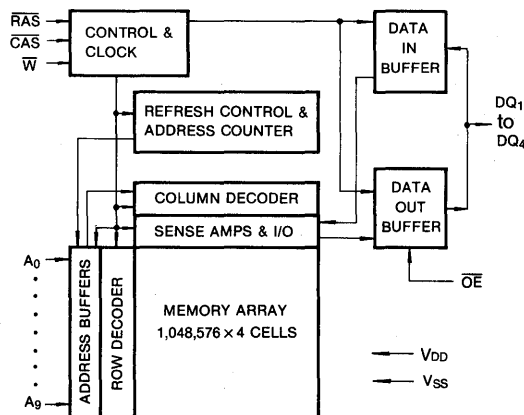
GENERAL DESCRIPTION

The Samsung KM44C1004C/CL/CSL is a high speed CMOS 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM44C1004C/CL/CSL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only Refresh. All inputs and outputs are fully TTL compatible.

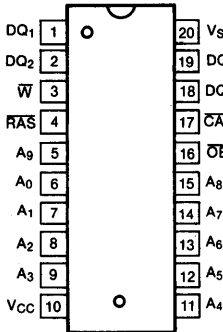
The KM44C1004C/CL/CSL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

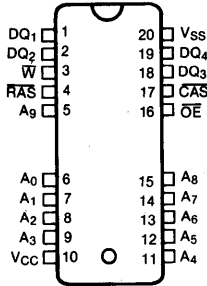


PIN CONFIGURATION (Top Views)

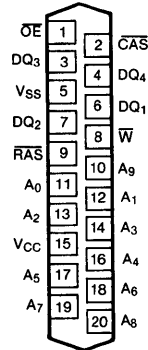
• KM44C1004CP/CLP/CSLP



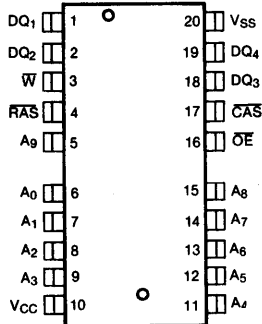
• KM44C1004CJ/CLJ/CSLJ



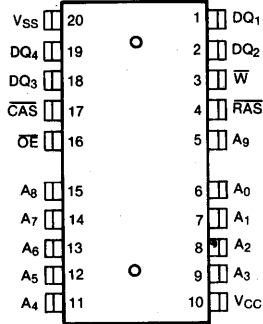
• KM44C1004CZ/CLZ/CSLZ



• KM44C1004CT/CLT/CSLT



• KM44C1004CTR/CLTR/CSLTR



Pin Names	Pin Function
A ₀ -A ₉	Address Inputs
RAS	Row Address Strobe
$\bar{C}AS$	Column Address Strobe
\bar{W}	Read/Write Input
$\bar{O}E$	Data Output Enable
DQ ₁ ~DQ ₄	Data In/Data Out
V _{CC}	Power (+5V)
V _{SS}	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} and \overline{CAS} Cycling @ t _{RC} =min.)	KM44C1004C/CL/CSL-5	-	85	mA
	KM44C1004C/CL/CSL-6		75	mA
	KM44C1004C/CL/CSL-7		65	mA
	KM44C1004C/CL/CSL-8		55	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	KM44C1004C	-	2	mA
	KM44C1004CL/CSL		1	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @ t _{RC} =min.)	KM44C1004C/CL/CSL-5	-	85	mA
	KM44C1004C/CL/CSL-6		75	mA
	KM44C1004C/CL/CSL-7		65	mA
	KM44C1004C/CL/CSL-8		55	mA
EDO Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @ t _{HPC} =min.)	KM44C1004C/CL/CSL-5	-	85	mA
	KM44C1004C/CL/CSL-6		75	mA
	KM44C1004C/CL/CSL-7		65	mA
	KM44C1004C/CL/CSL-8		55	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)	KM44C1004C	-	1	mA
	KM44C1004CL		200	μA
	KM44C1004CSL		100	μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @ t _{RC} =min.)	KM44C1004C/CL/CSL-5	-	85	mA
	KM44C1004C/CL/CSL-6		75	mA
	KM44C1004C/CL/CSL-7		65	mA
	KM44C1004C/CL/CSL-8		55	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V \overline{CAS} = \overline{CAS} -Before- \overline{RAS} Cycling or 0.2V DQ1-DQ4=Don't Care, TRC=125 μ S(L-Ver.) TRC=250 μ S(SL-Ver.), TRAS=TRAS min.-300nS	KM44C1004CL KM44C1004CSL I _{CC7}	-	300 150	μ A μ A
Input Leakage Current V _{CC} +0.5V (Any input 0 ≤ V _{IN} ≤ V _{CC} +0.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μ A
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μ A
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, Address can be changed maximum two times while \overline{RAS} =V_{IL}. In I_{CC4}, Address can be changed maximum once during a Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ -A ₉)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C _{IN2}	-	7	pF
Output Capacitance (DQ1~DQ4)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_a ≤ 70°C, V_{CC}=5.0V ± 0.5V, See notes 1,2)

Test condition: V_{IH}/V_{IL}=2.4/0.8V, V_{OH}/V_{OL}=2.0/0.8V, output loading C_L=100 pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	TRC	90		110		130		150		ns	
Read-modify-write cycle time	TRWC	133		155		185		205		ns	
Access time from \overline{RAS}	TRAC		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	TCAC		13		15		20		20	ns	3,4,5
Access time from column address	TAA		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	3		3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	tCEZ	3	13	3	15	3	20	3	20	ns	7
Transition time(rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	TRP	30		40		50		60		ns	
\overline{RAS} pulse width	TRAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	TRSH	13		15		20		20		ns	
\overline{CAS} hold time	TCSH	40		50		60		70		ns	
\overline{CAS} pulse width	TCAS	8	10,000	10	10,000	15	10,000	20	10,000	ns	16
\overline{RAS} to \overline{CAS} delay time	TRCD	20	37	20	45	20	50	20	60	ns	4

3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to RAS	tAR	40		45		55		60		ns	6
Column address to RAS lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to RAS	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to RAS lead time	tRWL	13		15		20		20		ns	
Write command to CAS lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to RAS	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
CAS to W delay time	tCWD	36		40		50		50		ns	8
RAS to W delay time	tRWD	73		85		100		110		ns	8
Column address to W delay time	tAWD	48		55		65		70		ns	8
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	
CAS hold time(CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		20		25		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	16
Hyper Page read-modify-write cycle time	tHPRWC	62		73		88		98		ns	
RAS pulse width (Hyper Page Cycle)	tRASP	50	200,000	60	200,000	70	200,000	80	200,000	ns	
CAS precharge time (Hyper Page Cycle)	tCP	8		10		10		10		ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
\overline{OE} to data delay	toED	13		15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	toEZ	3	13	3	15	3	20	3	20	ns	
\overline{OE} command hold time	toEH	13		15		20		20		ns	
Write command set-up time (test mode in)	twTS	10		10		10		10		ns	
Write command hold time (test mode in)	twTH	10		10		10		10		ns	
\overline{W} to \overline{RAS} precharge time(\overline{C} -B- \overline{R} refresh)	twRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time(\overline{C} -B- \overline{R} refresh)	twRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	treZ	3	13	3	15	3	20	3	20	ns	7,15
Output buffer turn off delay from \overline{W}	twEZ	3	13	3	15	3	20	3	20	ns	7
\overline{W} to data delay	twED	15		15		20		20		ns	
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		5		ns	

3

TEST MODE CYCLE

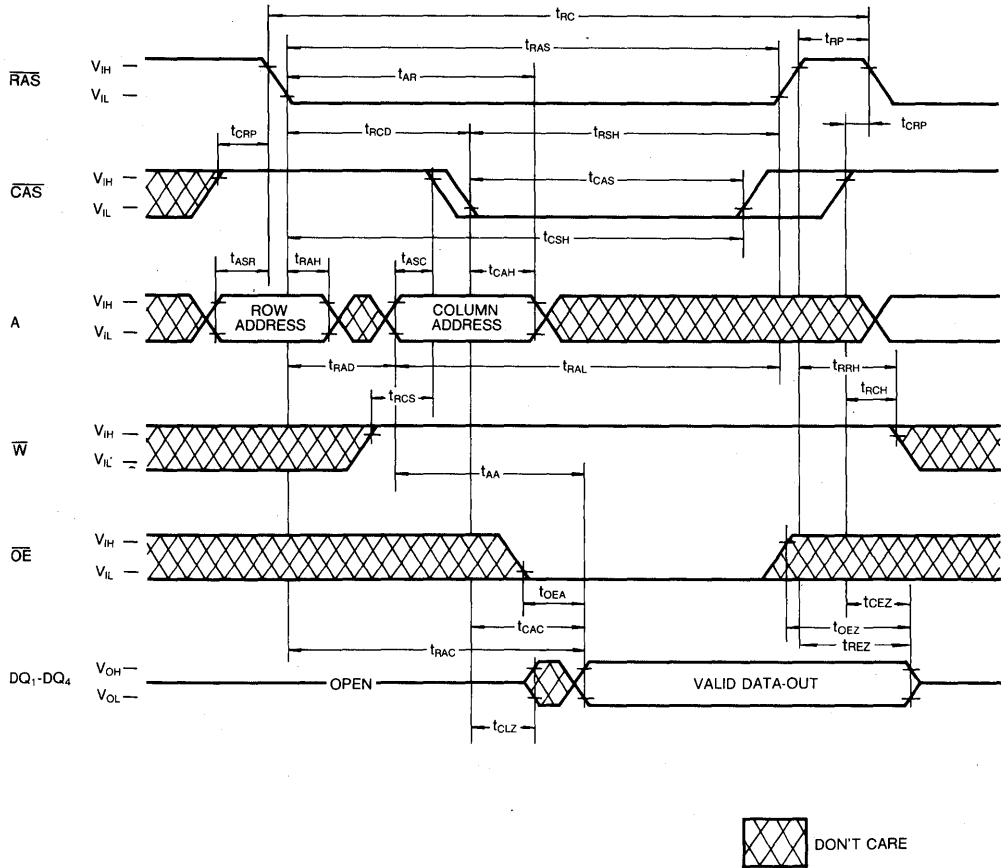
(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	95		115		135		155		ns	
Read-modify-write cycle time	trwc	138		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	trac		55		65		75		85	ns	3,4,11
Access time from $\overline{\text{CAS}}$	tcac		18		20		25		25	ns	3,4,5
Access time from column address	tac		30		35		40		45	ns	3,11
$\overline{\text{RAS}}$ pulse width	traw	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{\text{CAS}}$ pulse width	tcas	13	10,000	15	10,000	20	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ hold time	trsh	18		20		25		25		ns	
$\overline{\text{CAS}}$ hold time	tcs	43		50		55		65		ns	
Column address to $\overline{\text{RAS}}$ lead time	tral	30		35		40		45		ns	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcwd	41		45		55		55		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trwd	78		90		105		115		ns	8
Column address to $\overline{\text{W}}$ delay time	tawd	53		60		70		75		ns	8
Hyper Page cycle time	thpc	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	trpwc	67		78		93		103		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page Cycle)	trasp	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{\text{CAS}}$ precharge	tcpa		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	toea		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	toed	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	toeh	18		20		25		25		ns	

NOTES

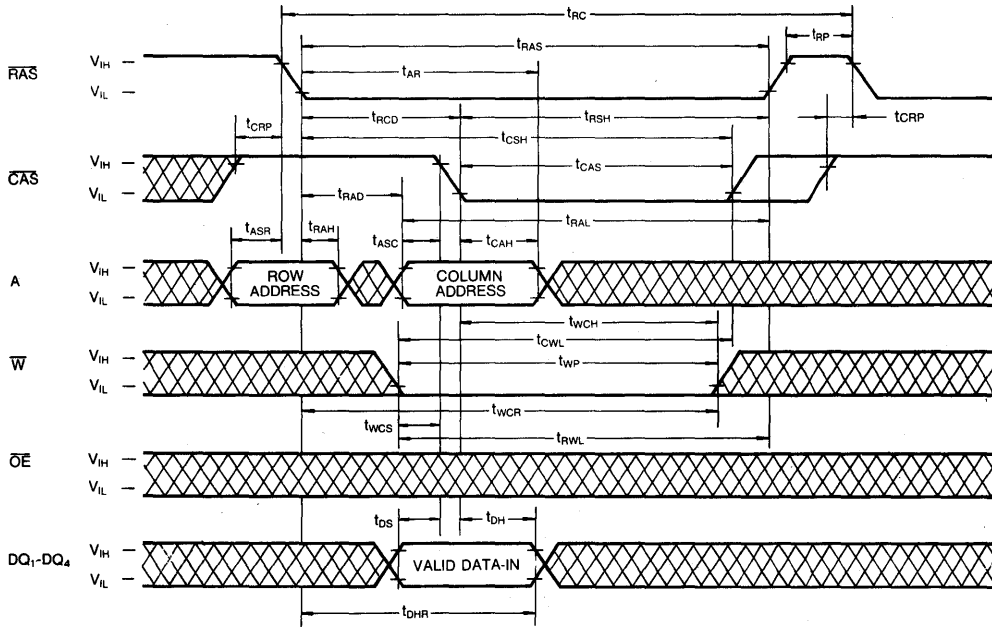
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only Refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are assumed to be 5ns for all inputs, except t_{HPC} and t_{HPRWC} .
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\text{max})$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{CEZ}(\text{max})$, $t_{REZ}(\text{max})$, $t_{OEZ}(\text{max})$ and $t_{WEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
16. $t_{ASC} \geq t_{CP \text{ min}}$, Assume $t_T=2.0\text{ns}$.

TIMING DIAGRAMS
READ CYCLE

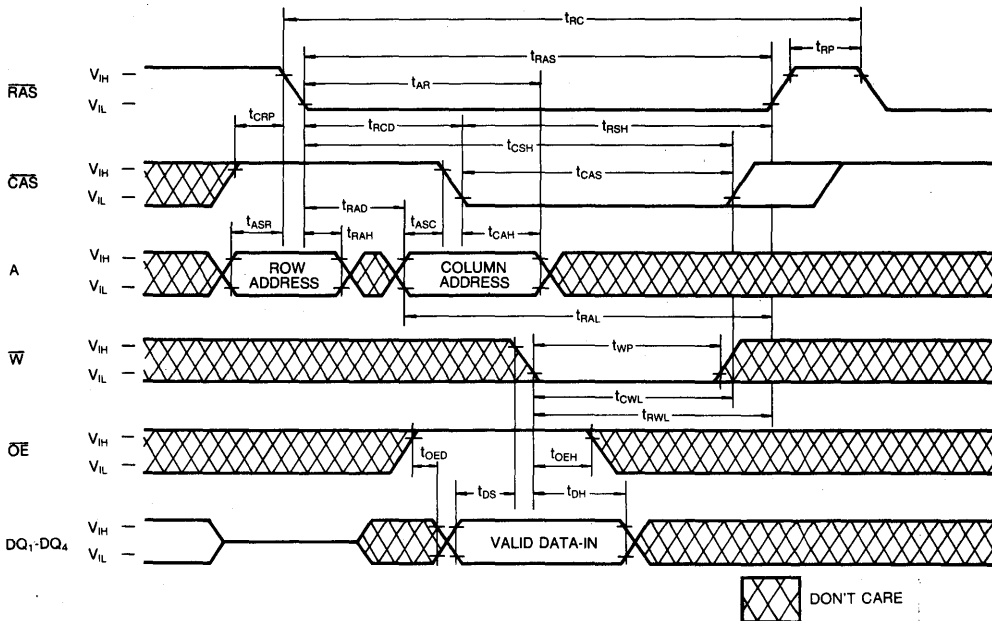


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

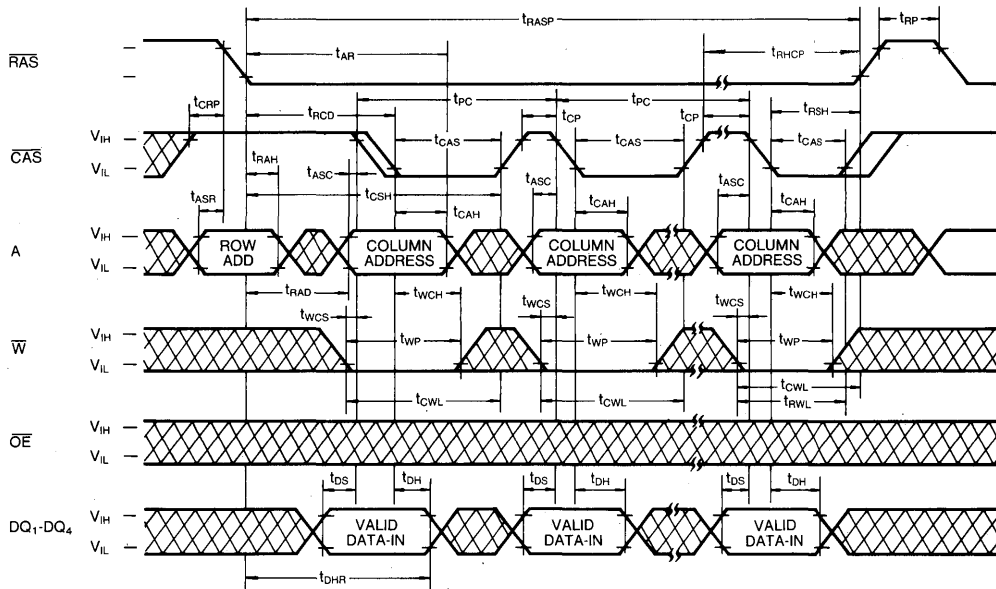


 DON'T CARE

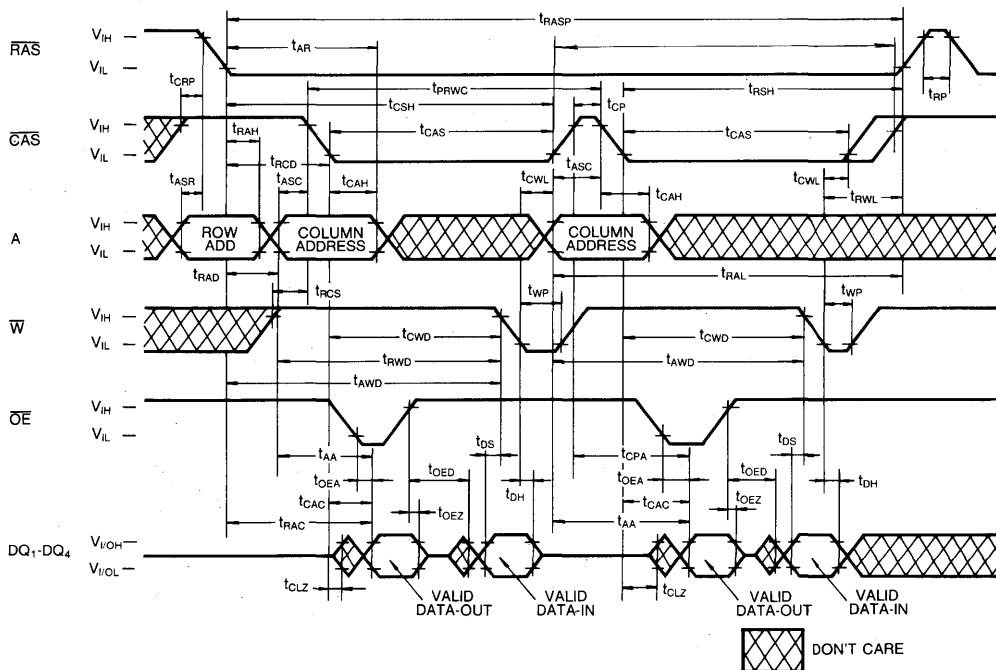
3

TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)

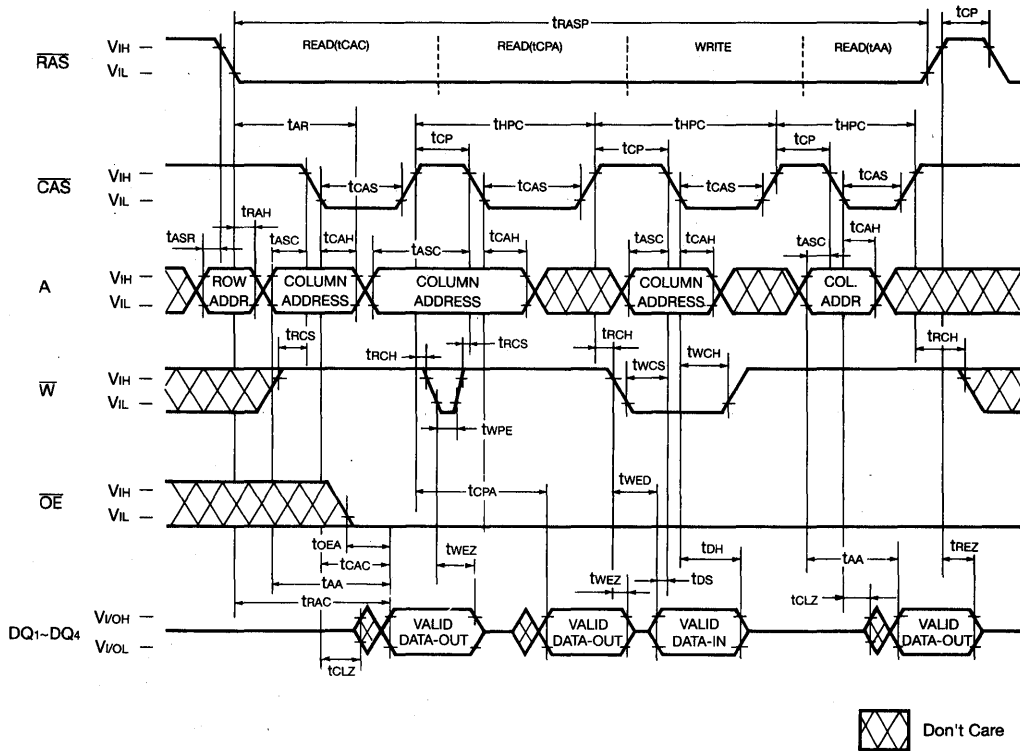


HYPER PAGE READ-MODIFY-WRITE CYCLE



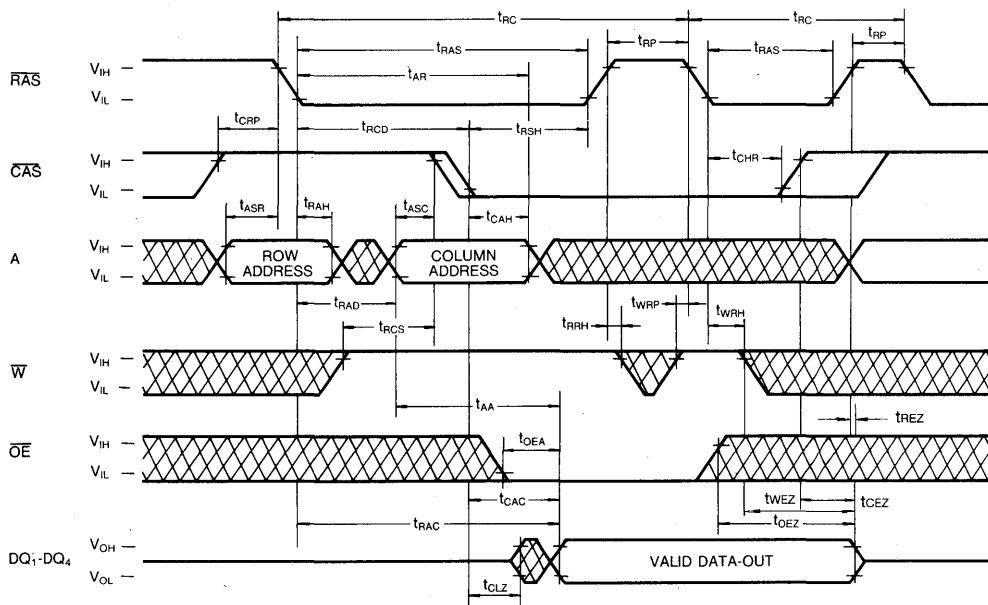
3

HYPER PAGE READ AND WRITE MIXED CYCLE

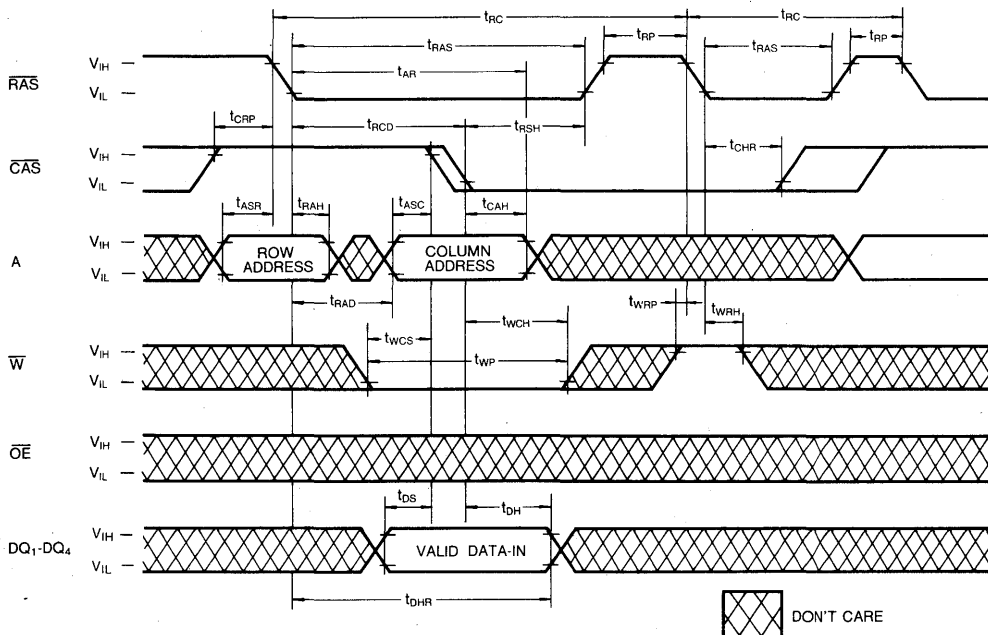


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

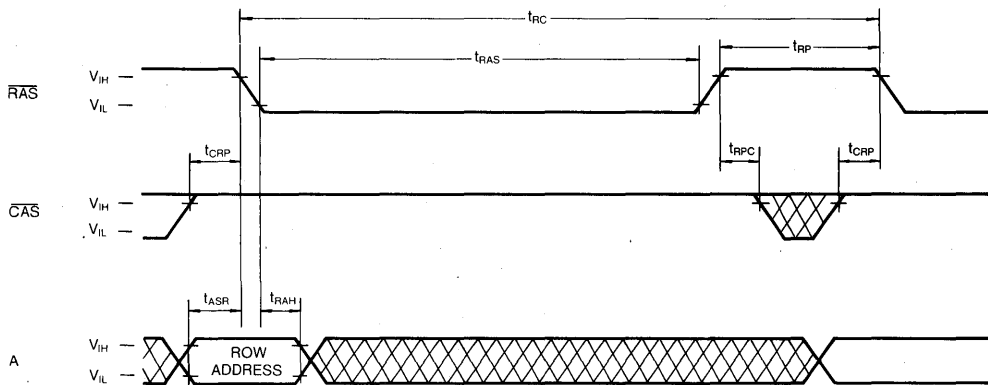


3

TIMING DIAGRAMS (Continued)

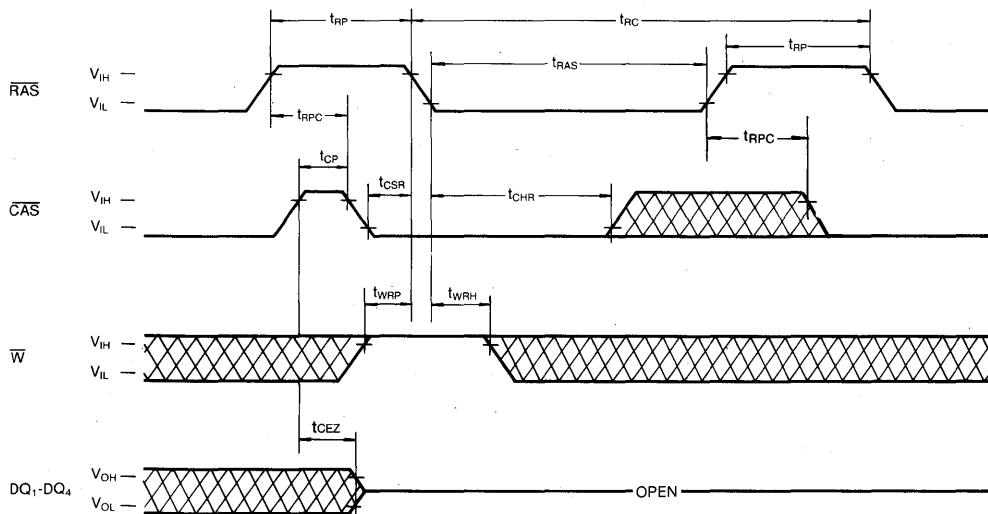
$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE

Note: $\overline{\text{W}}$, $\overline{\text{OE}}$ =Don't Care



$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH CYCLE

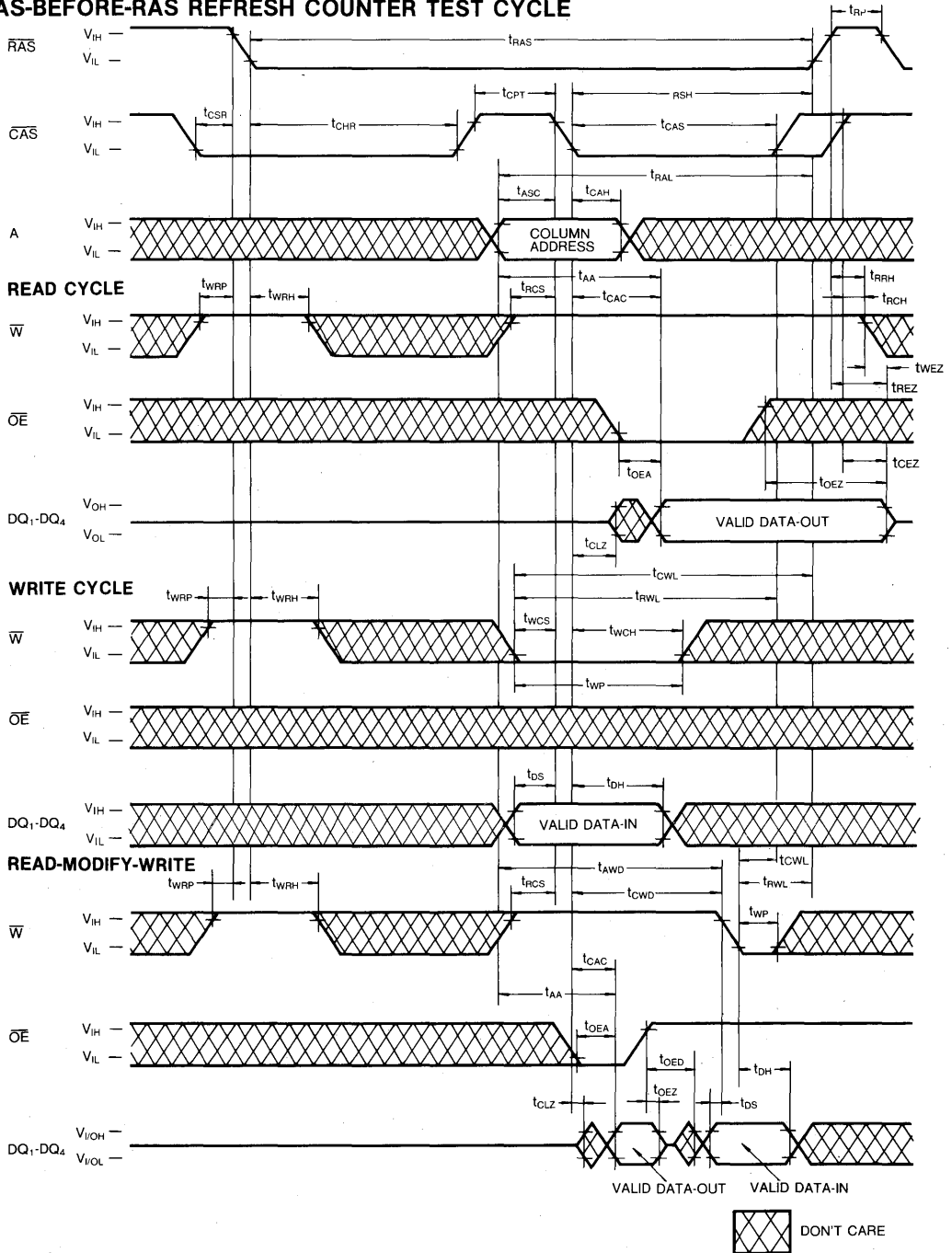
Note: $\overline{\text{OE}}$, Address=Don't Care



 DON'T CARE

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

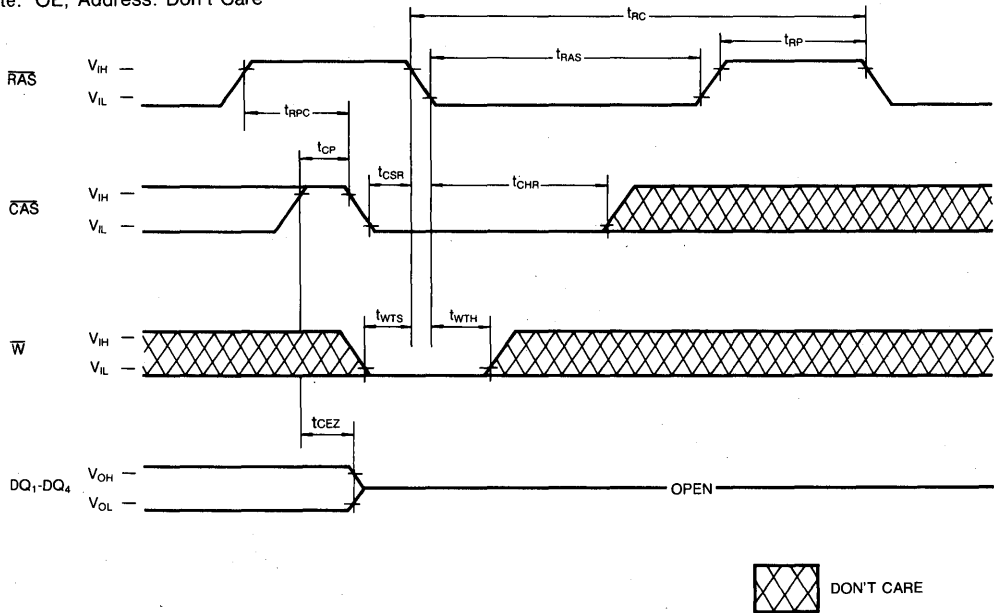


3

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



TEST MODE DESCRIPTION

The KM44C1004C/CL/CSL is the RAM organized 1, 048,576 words by 4 bit, it is internally organized 524, 288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A₀ is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would

indicate a "0". In "Test Mode", the 1M×4 DRAM can be tested as if it were a 512K×4 DRAM. \overline{W} , \overline{CAS} -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " \overline{CAS} -BEFORE- \overline{RAS} REFRESH CYCLE" or " \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

The KM44C1004C/CL/CSL contains 4,194,304 memory locations. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44C1004C/CL/CSL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0 - A_9) and 10 column (A_0 - A_9) address. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}), and the valid row and column address inputs.

Operating of the KM44C1004C/CL/CSL begins by strobing in a valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 10 address input pins (A_0 - A_9) is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM44C1004C/CL/CSL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

RAS and CAS Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44C1004C/CL/CSL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition. If \overline{CAS} goes low before $t_{RCB(max)}$ and if the column address is valid before $t_{RAC(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However, if \overline{CAS} goes low after $t_{RCB(max)}$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCB(max)}$ and $t_{RAD(max)}$. The KM44C1004C/CL/CSL has common data I/O pins. This reason an output enable control input (\overline{OE}) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, \overline{OE} must be low for the period of time defined by t_{OEA} and $t_{O EZ}$.

Write

The KM44C1004C/CL/CSL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} and \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If \overline{W} is brought low after \overline{CAS} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} , t_{CWD} and t_{AWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44C1004C/CL/CSL has a three-state output buffer which is controlled by \overline{RAS} , \overline{CAS} and \overline{OE} . When \overline{RAS} and \overline{CAS} go high (V_{IH}) or \overline{OE} goes high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data at the output cannot be eliminated by \overline{CAS} rising only and it remains until both \overline{RAS} and \overline{CAS} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM44C1004C/CL/CSL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, EDO Mode Read, EDO Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Fast Page with EDO Mode Write, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh, OE controlled write.

Indeterminate Output State: Delayed Write (tcwd or tawd are not met)

Refresh

The data in the KM44C1004C/CL/CSL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256ms. There are several ways to accomplish this.

$\overline{\text{RAS}}$ -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. This cycle must be repeated for each row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh: The KM44C1004C/CL/CSL has $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ is held low for the specified set up time (tcsr) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CAS}}$ active time and cycling $\overline{\text{RAS}}$. The KM44C1004C/CL/CSL hidden refresh cycle is actually a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44C1004C/CL/CSL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

Fast Page Mode with Extended Data Out

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{\text{RAS}}$ is kept low to maintain the $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This

eliminates the time required to set up and strobe sequential row addresses for the same page.

 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry.

After the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation, is $\overline{\text{CAS}}$ goes high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A₀ through A₉ are supplied by the on-chip refresh counter.

Column Address — Bits A₀ through A₉ are supplied by the falling edge of $\overline{\text{CAS}}$ as in a normal memory cycle.

Suggested $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Counter Test Procedure

The $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle timing is used in each of the following steps;

1. Initialize the internal refresh counter by performing 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycle, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4.

Power-up

If $\overline{\text{RAS}} = V_{\text{ss}}$ during power-up, the KM44C1004C/CL/CSL could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ track with V_{cc} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μsec is required after power-up followed by any 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L-ver: 128, SL-ver:256) msec period in which there are no $\overline{\text{RAS}}$

DEVICE OPERATION (Continued)

cycles. An initialization cycle is any cycle in which \overline{RAS} is cycled.

Termination

The lines from the TTL driver circuits to the KM44C1004C/CL/CSL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44C1004C/CL/CSL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each

intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

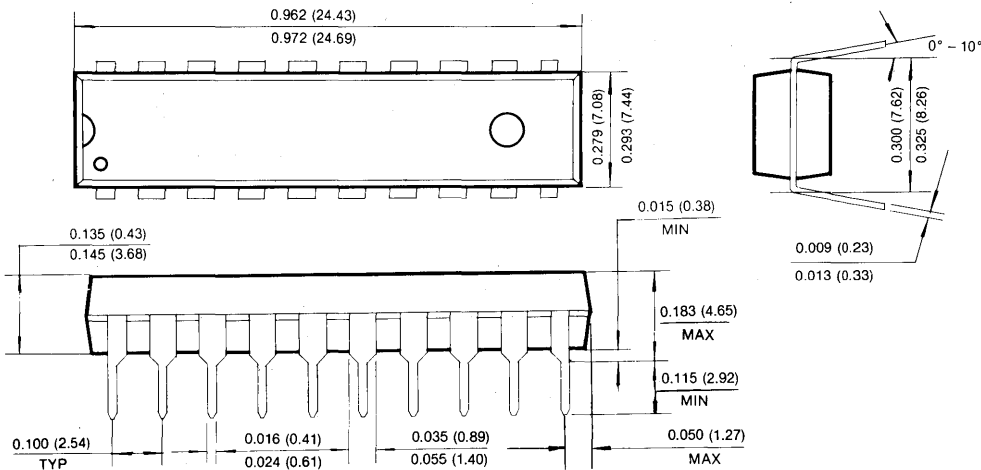
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM44C1004C/CL/CSL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44C1004C/CL/CSL and they supply much of the current used by the KM44C1004C/CL/CSL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

3

PACKAGE DIMENSIONS
20-LEAD PLASTIC DUAL IN-LINE PACKAGE

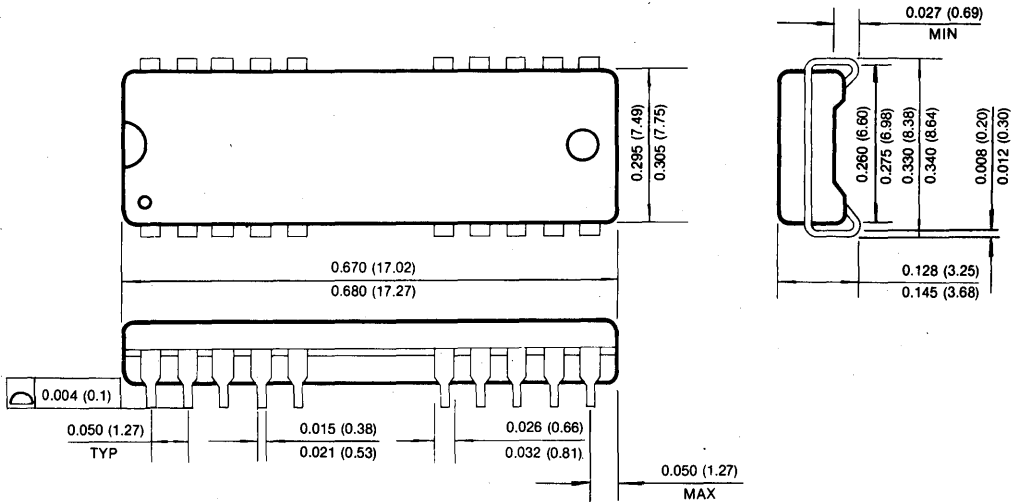
Units: Inches (Millimeters)



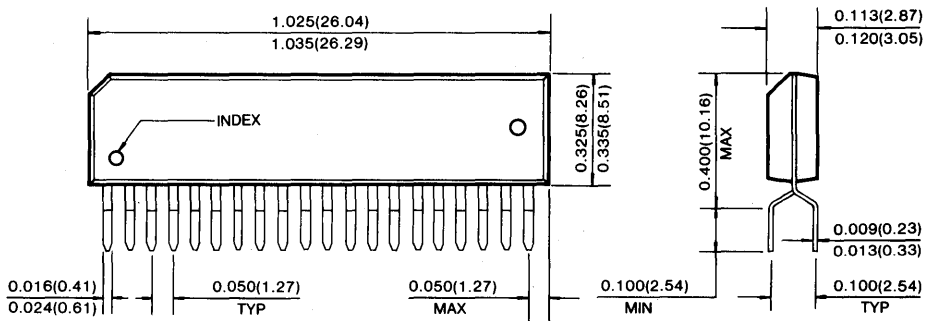
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



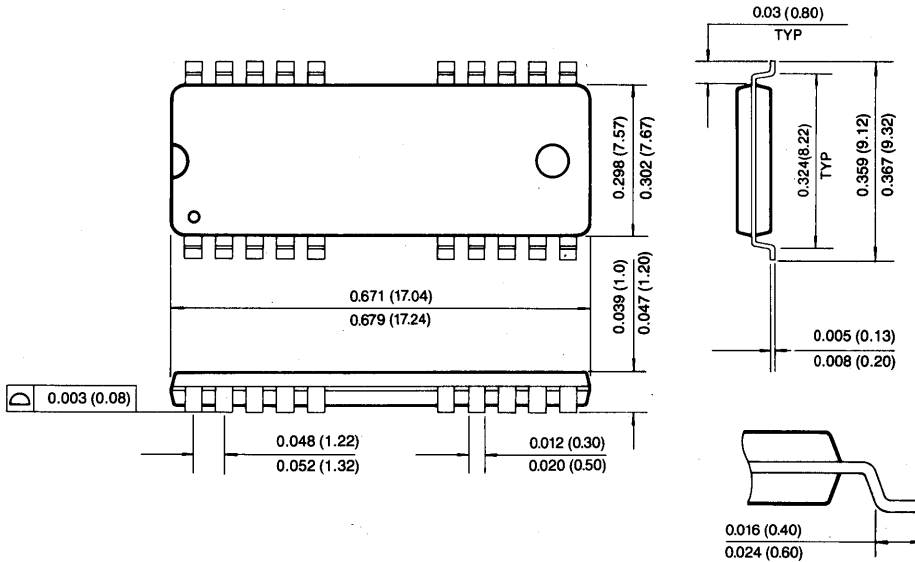
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



3

4M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM41V4000C/CL/CLL-6	60ns	15ns	110ns
KM41V4000C/CL/CLL-7	70ns	20ns	130ns
KM41V4000C/CL/CLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refresh operation (LL-version)
- CAS-before-RAS refresh capability
- RAS-only and hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Common I/O using early write
- Single + 3.3V ± 0.3V power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/128ms (LL-version)
- Power Dissipation
 - Standby: 3.6mW(Nomal)
 - 0.18 mW(L-version)
 - 0.18mW(LL-version)
 - Active (60/70/80ns):220/200/180mW
- JEDEC standard pinout
- Available in plastic SOJ, ZIP and TSOP II packages

GENERAL DESCRIPTION

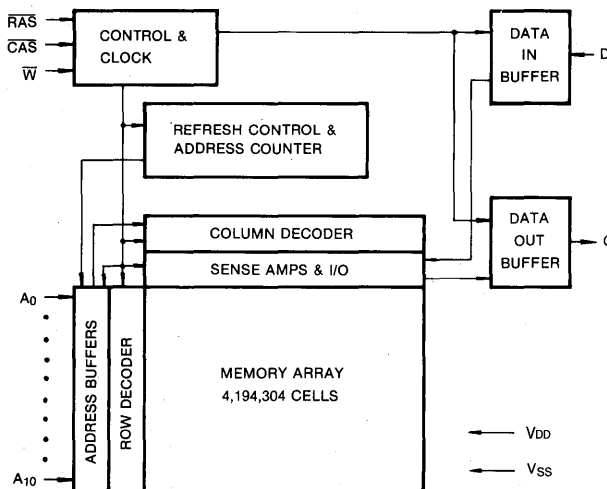
The Samsung KM41V4000C/CL/CLL is a high speed CMOS 4,194,304 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

The KM41V4000C/CL/CLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only Refresh. All inputs and output are fully TTL compatible.

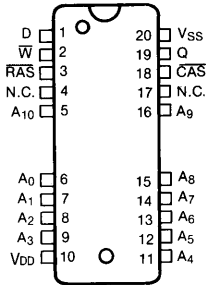
The KM41V4000C/CL/CLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

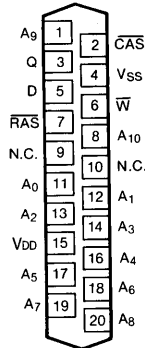


PIN CONFIGURATION (Top Views)

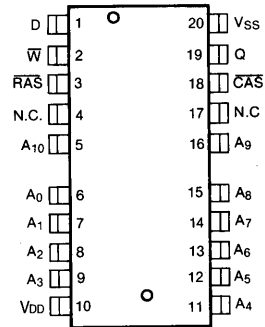
• KM41V4000CJ/CLJ/CLLJ



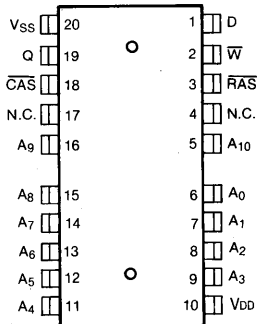
• KM41V4000CZ/CLZ/CLLZ



• KM41V4000CT/CLT/CLLT



• KM41V4000CTR/CLTR/CLLTR



Pin Names	Pin Function
A ₀ -A ₁₀	Address Inputs
D	Data In
Q	Data Out
W	Read/Write Input
RAS	Row Address Strobe
CAS	Column Address Strobe
VDD	Power (+ 3.3V)
VSS	Ground
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	- 0.5~V _{DD} + 0.5	V
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	- 0.5~4.6	V
Storage Temperature	T _{stg}	- 55 to + 150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	- 0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD} = 3.3V ± 0.3V)

Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Operating Current* (RAS, CAS, Address Cycling @trc=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8 Icc1		60 55 50	mA mA mA
Standby Current (RAS=CAS=W=V _{IH})	Icc2		1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8 Icc3		60 55 50	mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tPC=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8 Icc4		45 40 35	mA mA mA
STANDBY CURRENT (RAS=CAS=W=V _{DD} -0.2V)	KM41V4000C KM41V4000CL KM41V4000CLL Icc5		500 100 100	μA μA μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM41V4000C/CL/CLL-6 KM41V4000C/CL/CLL-7 KM41V4000C/CL/CLL-8 Icc6		60 55 50	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DIN=Don't Care TRC=125(L-ver) μS TRAS=TRAS min~300ns	KM41V4000CL Icc7		200	μA
Self Refresh Current RAS=CAS=V _{IL} D=W=A0~A10=D=V _{DD} -0.2V or 0.2V	KM41V4000CLL Icc8		150	μA

DC AND OPERATING CHARACTERISTICS(Continued)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test=0V)	$I_{(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

* Note: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1} , I_{CC3} , I_{CC6} , Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. I_{CC4} , Address can be changed maximum once during a Fast Page Mode Cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(A ₀ -A ₁₀ ,D)	C_{IN1}	—	5	pF
Input Capacitance(\overline{RAS} , \overline{CAS} , \overline{W})	C_{IN2}	—	7	pF
output Capacitance(Q)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	130		155		175		ns	
Access time from \overline{RAS}	trac		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	tt	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	trp	40		50		60		ns	
\overline{RAS} pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	trSH	15		20		20		ns	
\overline{CAS} hold time	tcSH	60		70		80		ns	
\overline{CAS} pulse width	tcAS	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	trCD	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	trAD	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tcRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	trAH	10		10		10		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold referenced to $\overline{\text{RAS}}$	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		20		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (1024 cycles)	tREF		16		16		16	ms	
Refresh period (L/LL-version)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to Write enable delay	tCWD	15		20		20		ns	8
$\overline{\text{RAS}}$ to Write enable delay	tRWD	60		70		80		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	30		35		40		ns	8
$\overline{\text{CAS}}$ setup time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycle)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test)	tCPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Fast page mode cycle time	tPC	40		45		50		ns	
$\overline{\text{CAS}}$ precharge time(fast page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
Fast page mode read-modify-write	tPRWC	60		70		75		ns	
$\overline{\text{RAS}}$ pulse width (fast page mode)	tRASP	60	200,000	70	200,000	80	200,000	ns	
Write command set-up time (test mode in)	tWTS	10		10		10		ns	
Write command hold time (test mode in)	tWTH	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRP	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRH	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tPASS	100		100		100		μs	13
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRPS	110		130		150		ns	13
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	13

TEST MODE CYCLE

(Note. 12)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	115		135		155		ns	
Read-modify-write cycle time	t _{RWC}	135		160		180		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		65		75		85	ns	3,4,11
Access time from $\overline{\text{CAS}}$	t _{CAC}		20		25		25	ns	3,4,5
Access time from column address	t _{AA}		35		40		45	ns	3,11
$\overline{\text{RAS}}$ pulse width	t _{RAS}	65	10,000	75	10,000	85	10,000	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	20		25		25		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	35		40		45		ns	
$\overline{\text{CAS}}$ to write enable delay	t _{CWD}	20		25		25		ns	8
$\overline{\text{RAS}}$ to write enable delay	t _{RWD}	65		75		85		ns	8
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	35		40		45		ns	8
Fast mode cycle time	t _{PC}	45		50		55		ns	
Fast page moderated-modify-write	t _{PRWC}	65		80		85		ns	
$\overline{\text{RAS}}$ pulse width(fast page mode)	t _{RASP}	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		40		45		50	ns	3

NOTES

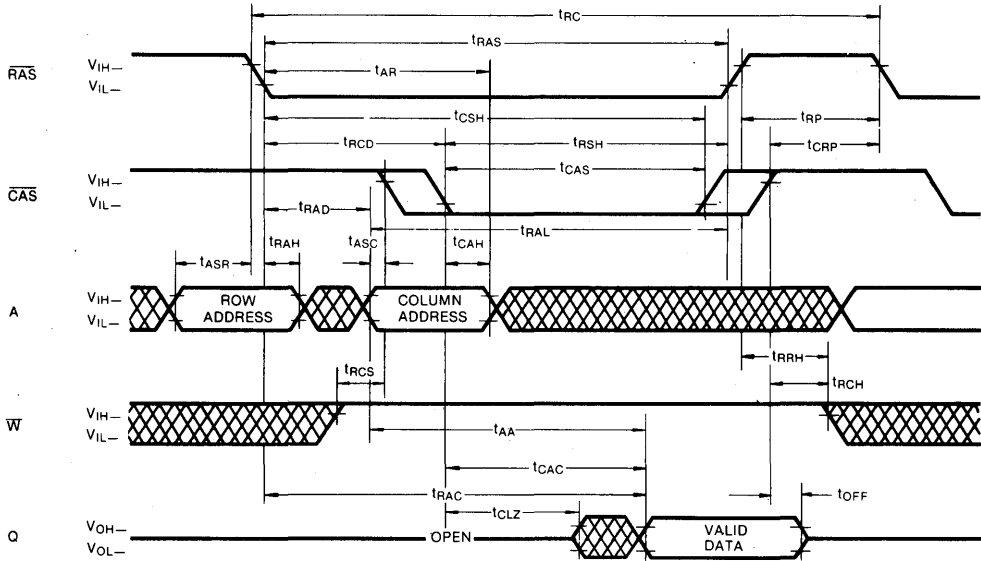
1. An initial pause of 200 μ s is required after power-up followed by and 8 $\overline{\text{CBR}}$ or $\overline{\text{ROR}}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and 100pF, and V_{oh}=2.0V, V_{ol}=0.8V
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that t_{RCD} \geq t_{RCD}(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} \geq t_{WCS}(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{CWD} \geq t_{CWD}(min), t_{RWD} \geq t_{RWD}(min) and t_{AWD} \geq t_{AWD}(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification



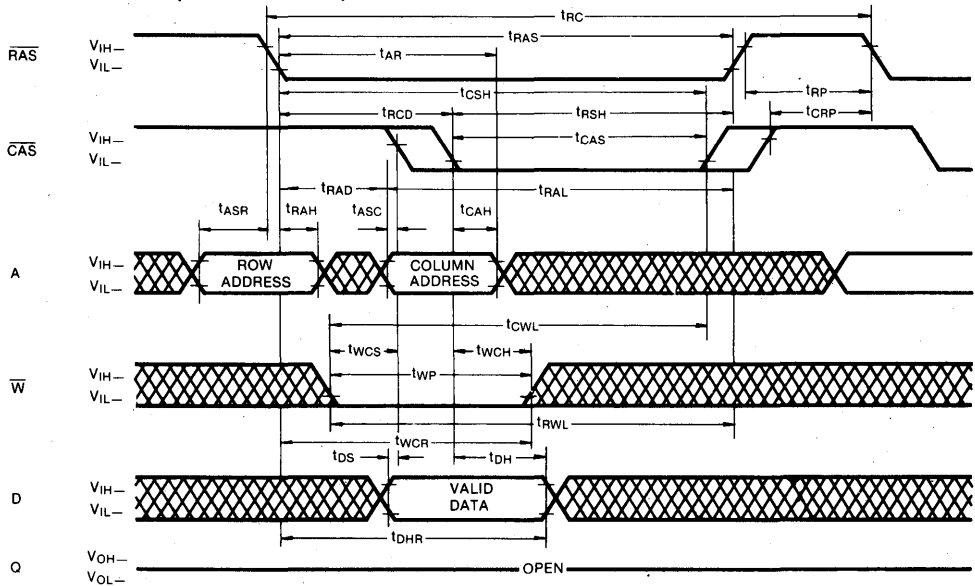
3

TIMING DIAGRAMS

READ CYCLE



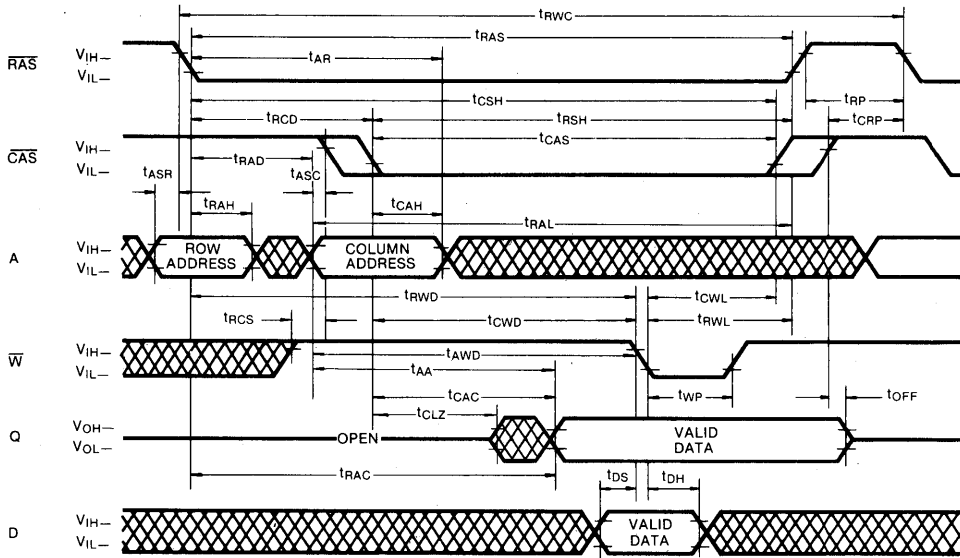
WRITE CYCLE (EARLY WRITE)



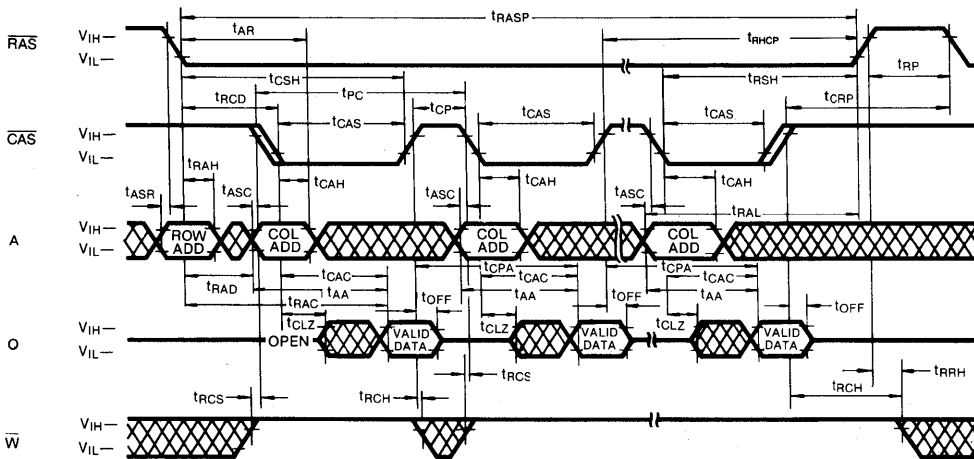
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

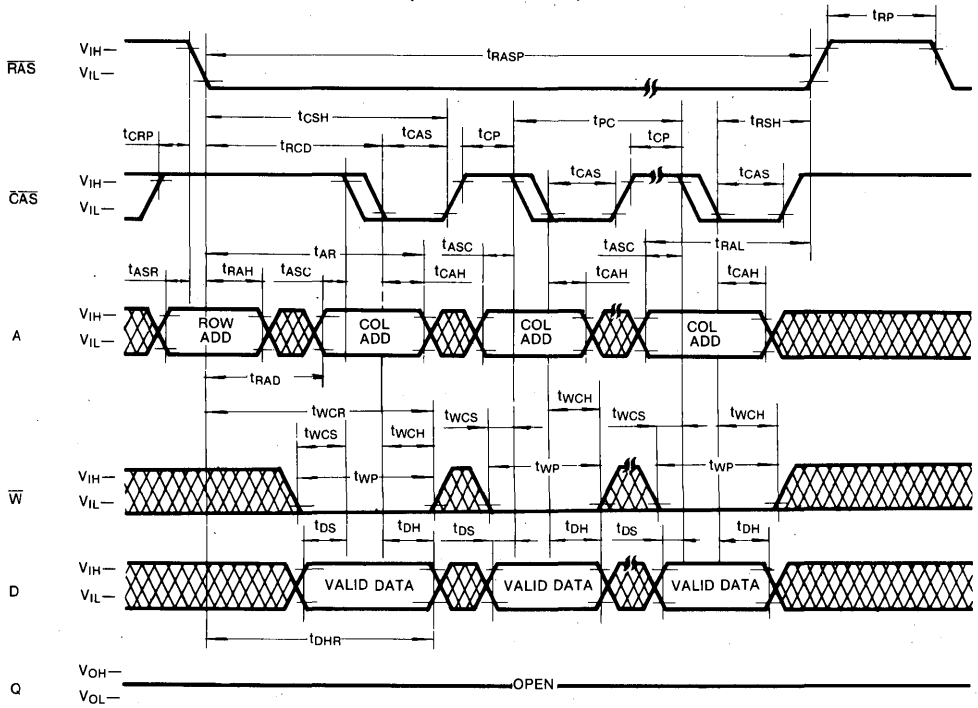


DON'T CARE

3

TIMING DIAGRAMS (Continued)

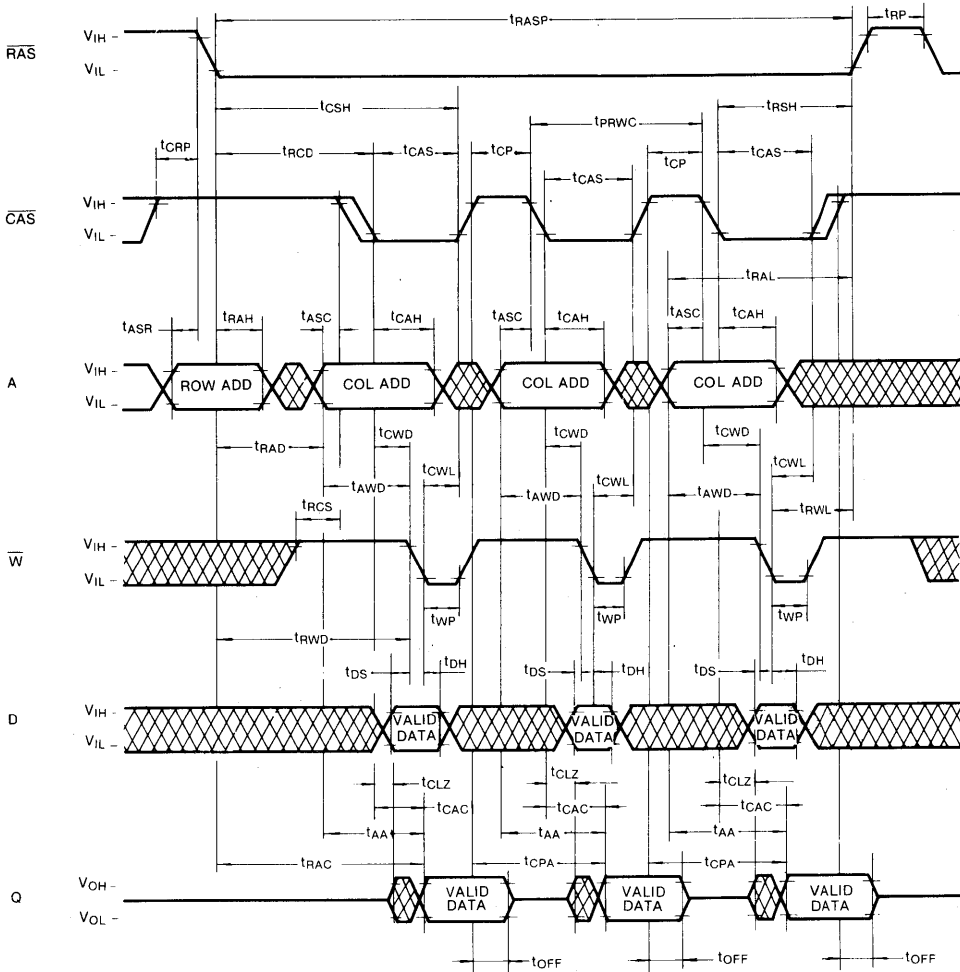
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-WRITE CYCLE



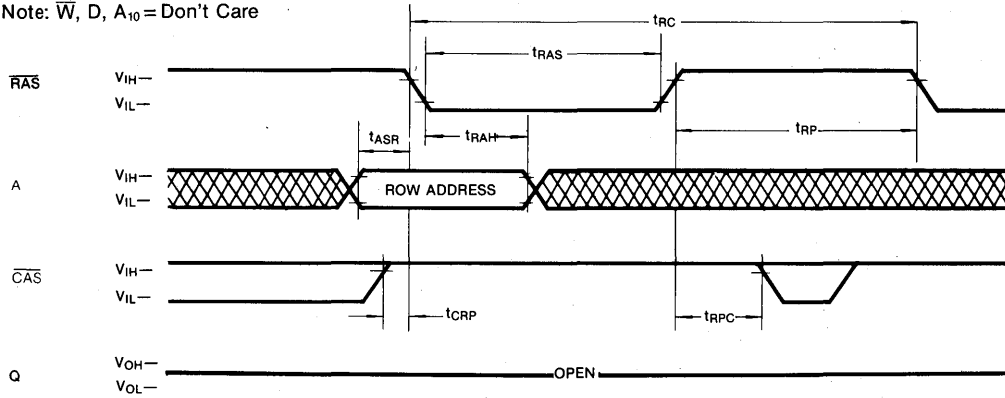
 DON'T CARE

3

TIMING DIAGRAMS (Continued)

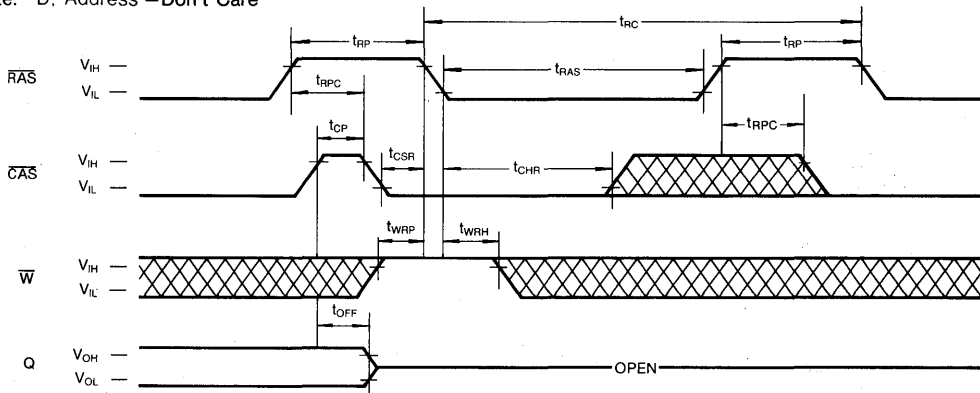
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , D, A₁₀ = Don't Care



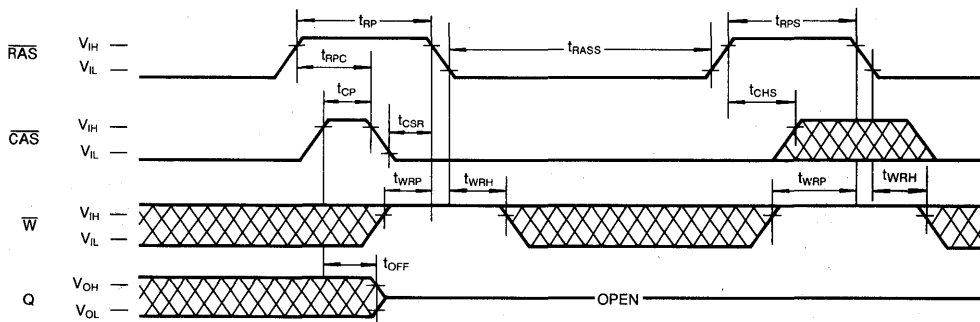
CAS BEFORE RAS REFRESH CYCLE

Note: D, Address = Don't Care



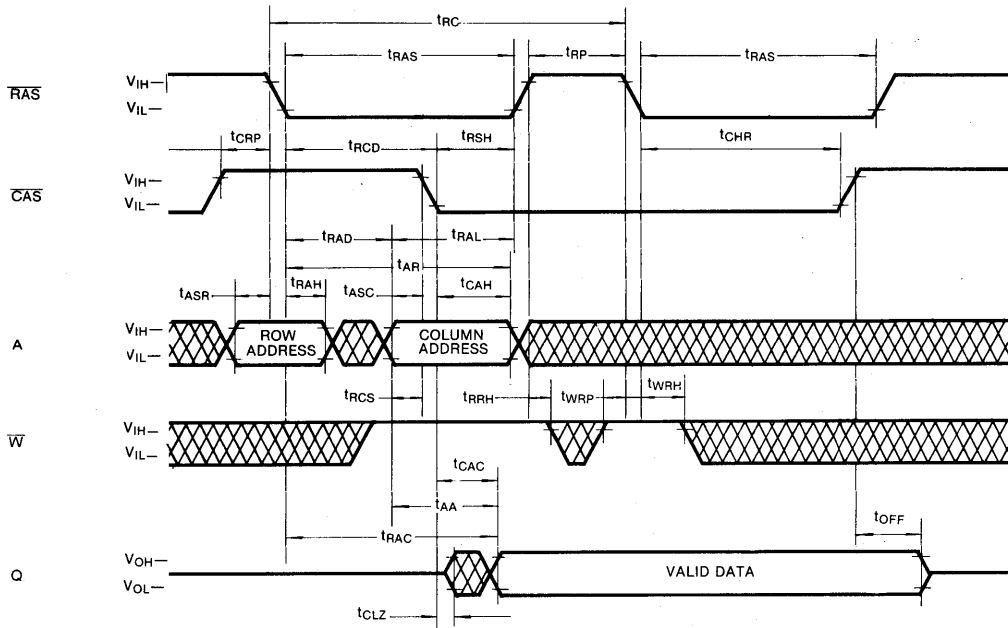
CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-ver only)

Note: Address = Don't Care

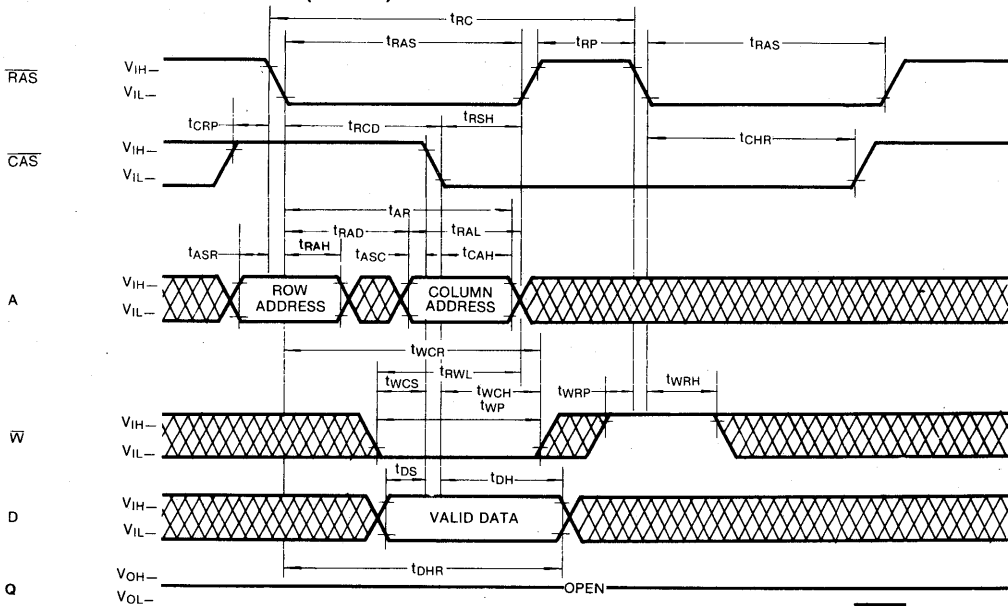


 DON'T CARE

TIMING DIAGRAMS (Continued)
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

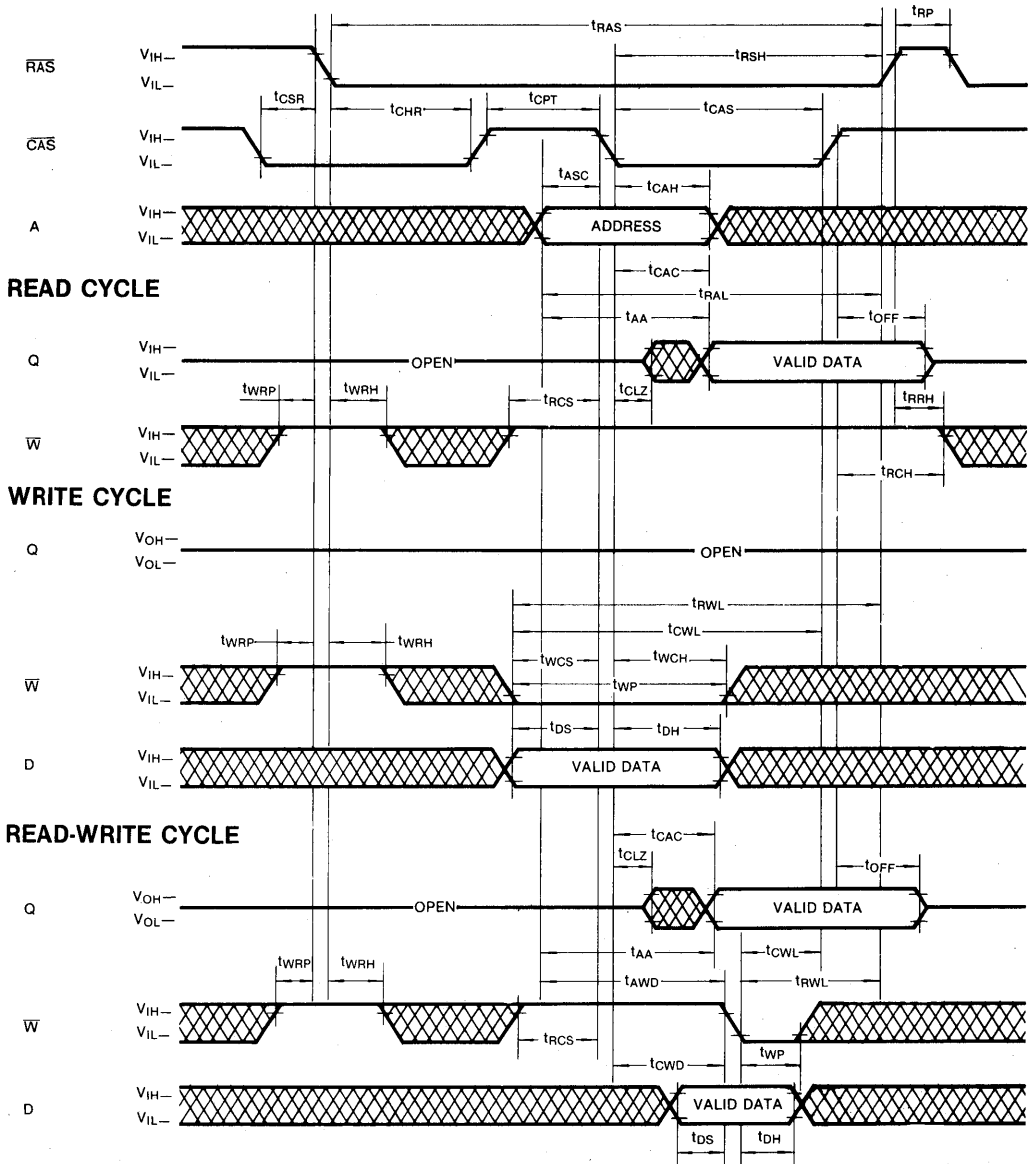


DON'T CARE

3

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

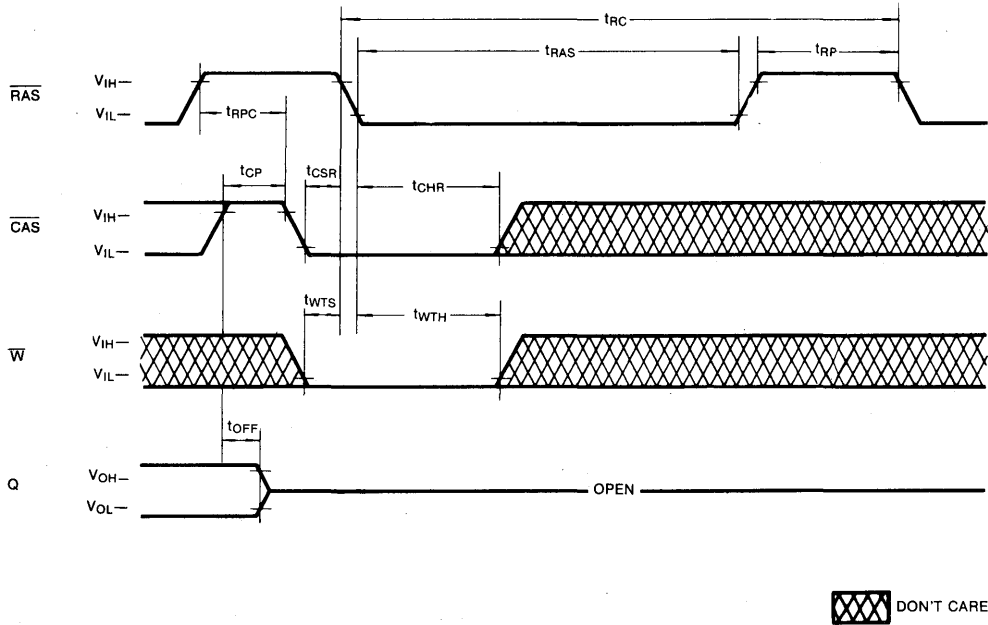


 DON'T CARE

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: D, Address=Don't Care



3

TEST MODE DESCRIPTION

The KM41V4000C/CL/CLL is the RAM organized 4, 194,304 words by 1 bit it is internally organized 524, 288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A₀ and A₁₀ are not used. If, upon reading, all bits are equal (all "1" or "0"s), the data output pin indicates a "1" if any of the bits differed the data output pin would indicate a "0". In "Test Mode",

the 4M DRAM can be tested as if it were a 512K DRAM. \overline{W} , \overline{CAS} -Before- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode", And " \overline{CAS} -Before- \overline{RAS} Refresh Cycle" or " \overline{RAS} -only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time(1/8 in cases of N test pattern.)

DEVICE OPERATION

Device Operation

The KM41V4000C/CL/CLL contains 4,194,304 memory locations. Twenty-two address bits are required to address a particular memory location. Since the KM41V4000C/CL/CLL has only 11 address input pins, time multiplexed addressing is used to input 11 row and 11 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{\text{RAS}}$), the column address strobe ($\overline{\text{CAS}}$) and the valid row and column address inputs.

Operating of the KM41V4000C/CL/CLL begins by strobing in valid row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. Then the address on the 11 address input pins is changed from a row address to a column address and is strobed in by $\overline{\text{CAS}}$. This is the beginning of any KM41V4000C/CL/CLL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ have returned to the high state. Another cycle can be initiated after $\overline{\text{RAS}}$ remains high long enough to satisfy the $\overline{\text{RAS}}$ precharge time (t_{RP}) requirement.

RAS and CAS Timing

The minimum $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths are specified by $t_{\text{RAS}}(\text{min})$ and $t_{\text{CAS}}(\text{min})$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{\text{RAS}}$ low, it must not be aborted prior to satisfying the minimum $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{\text{RAS}}$ precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM41V4000C/CL/CLL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{\text{W}}$) high during a $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycle. If $\overline{\text{CAS}}$ goes low before $t_{\text{RC}}(\text{max})$, the access time to valid data is specified by $t_{\text{RAC}}(\text{min})$. If $\overline{\text{CAS}}$ goes low after $t_{\text{RC}}(\text{max})$, the access time is measured from $\overline{\text{CAS}}$ and is specified by t_{CAC} . In order to achieve the minimum access time, $t_{\text{RAC}}(\text{min})$, it is necessary to bring $\overline{\text{CAS}}$ low before $t_{\text{RC}}(\text{max})$.

Write

The KM41V4000C/CL/CLL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{\text{W}}$ and $\overline{\text{CAS}}$. In any type of write cycle, Data-in must be valid at

or before the falling edge of $\overline{\text{W}}$ or $\overline{\text{CAS}}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{\text{W}}$ low before $\overline{\text{CAS}}$. The data at the data input pin ($\overline{\text{D}}$) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. The cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{\text{W}}$ is brought low after $\overline{\text{CAS}}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} , t_{CWD} and t_{AWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM41V4000C/CL/CLL has three-state output buffer which are controlled by $\overline{\text{CAS}}$. Whenever $\overline{\text{CAS}}$ is high (V_{IH}), the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{\text{CAS}}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{\text{CAS}}$ returns high. This is true even if a new $\overline{\text{RAS}}$ cycle occurs (as in hidden refresh). Each of the KM41V4000C/CL/CLL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{\text{RAS}}$ -only Refresh, Fast Page Mode Write, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh, $\overline{\text{CAS}}$ -only cycle.

Indeterminate Output State: Delayed Write

Refresh

DEVICE OPERATION (Continued)

The data in the KM41V4000C/CL/CLL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16(L,LL-ver:128ms). There are several ways to accomplish this.

RAS-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. This cycle must be repeated for each row.

CAS-before-RAS Refresh: The KM41V4000C/CL/CLL has $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{\text{CAS}}$ input is held low for the specified set up time (tcsr) before $\overline{\text{RAS}}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{\text{CAS}}$ active time and cycling $\overline{\text{RAS}}$. The KM41V4000C/CL/CLL hidden refresh cycle is actually a $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh to be used for long periods of standby, such as at battery back-up. In normal $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ condition, when $\overline{\text{RAS}}$ is held low above 100 ns an internal timer activates a refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ goes high (VIH).

Other Refresh Methods: It is also possible to refresh the KM41V4000C/CL/CLL by using read, write or read-modify write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh is the preferred method.

Fast Page Mode

The KM41V4000C/CL/CLL has Fast page mode capability. Fast page mode memory cycles provides faster access and lower power dissipation than normal memory cycles. In Fast page mode, it is possible to perform read, write or read-modify-write cycles. As long as the

applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{\text{RAS}}$ is kept low to maintain the $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page. Up to 2048 memory cells can be accessed with the same row address.

CAS-before-RAS Refresh Counter Test Cycle

A special timing sequence using the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh activated circuitry.

After the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh operation, $\overline{\text{CAS}}$ goes high and then low again while $\overline{\text{RAS}}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ counter test cycle timing diagram. A memory cell can be addressed with 11 row address bits and 11 column address bits defined as follows:

Row Address- Bits A0 through A9 are supplied by the on-chip refresh counter. This A10 bit is set high internally.

Column Address- Bits A0 through A10 are strobed in by the falling edge of $\overline{\text{CAS}}$ as in a normal memory cycle.

Suggested CAS-before-RAS counter Test Procedure

The $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{\text{RAS}} = V_{SS}$ during power-up, the KM41V4000C/CL/CLL can begin an active cycle. This condition results in

DEVICE OPERATION (Continued)

higher than necessary current demands from the power supply during power-up. It is recommended that RAS and CAS track with Vcc during power-up or be held at a valid VIH in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by any 8 RAS cycles before proper device operation is assured. Eight initialization cycles are also required after any 16 msec period in which there are no RAS cycles. An initialization cycle is any cycle in which RAS is cycled.

Termination

The lines from the TTL driver circuits to the KM41V4000C/CL/CLL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws on additional power. It consists of a resistor in series with the input line placed close to the KM41V4000C/CL/CLL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like

transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the Vcc line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the Vcc to Vss voltage (measured at the device pins) should not exceed 500mV.

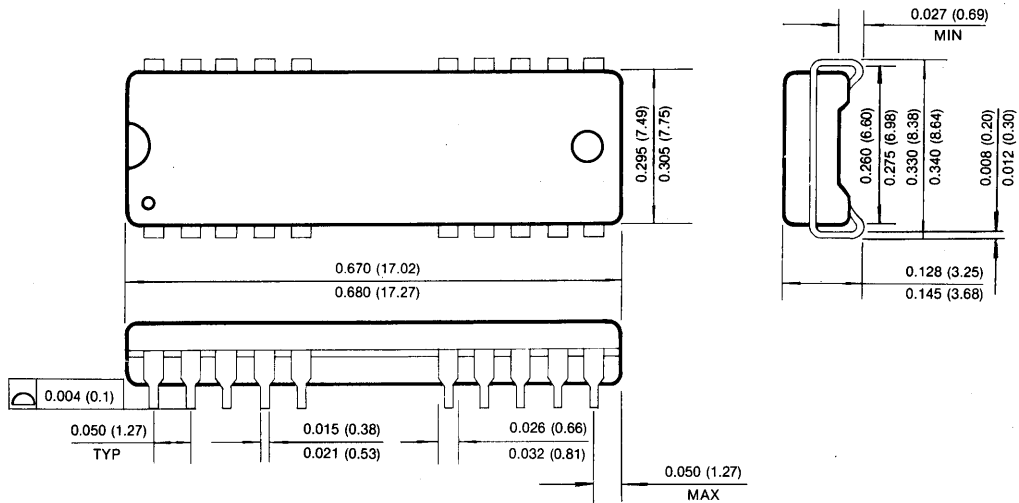
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the Vcc and ground pins of each KM41V4000C/CL/CLL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM41V4000C/CL/CLL and they supply much of the current used by the KM41V4000C/CL/CLL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

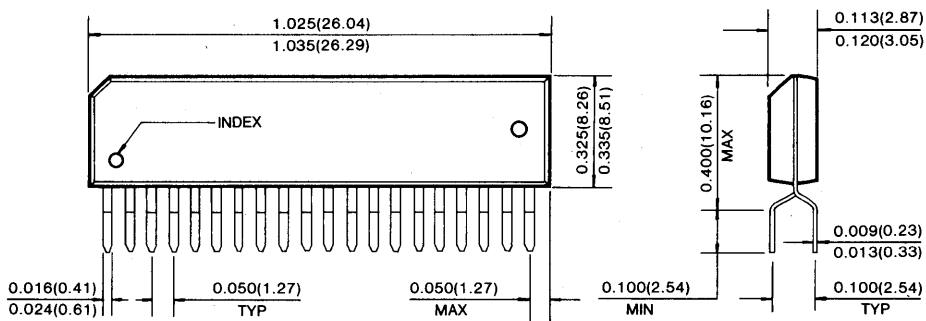
PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

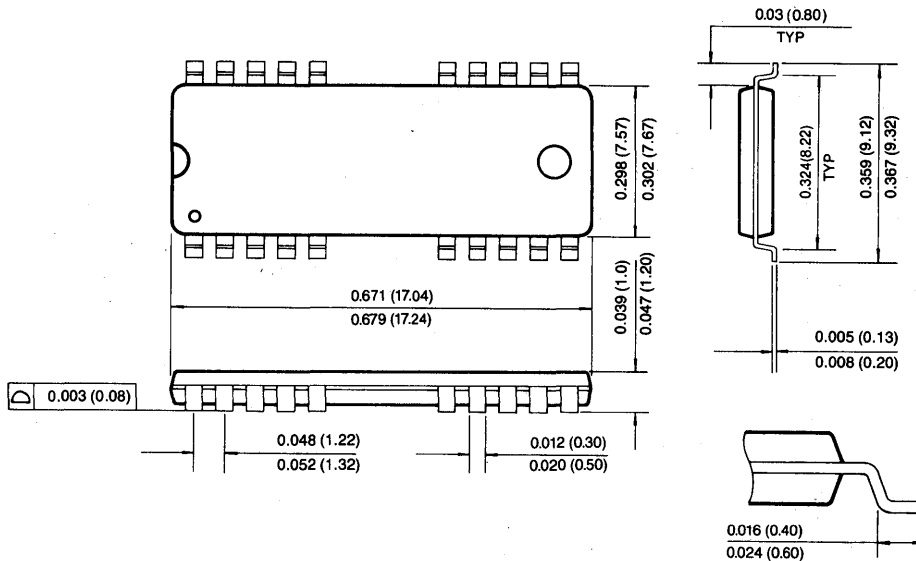


3

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



1M × 4Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{TRC}
KM44V1000C/CL/CLL-6	60ns	15ns	110ns
KM44V1000C/CL/CLL-7	70ns	20ns	130ns
KM44V1000C/CL/CLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refresh operation (LL-version)
- CAS-before-RAS refresh capability
- RAS-only and hidden refresh capability
- Fast parallel test mode capability.
- TTL compatible inputs and output
- Early write or output enable controlled write
- Single + 3.3V ± 0.3V power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/128ms (LL-version)
- Power dissipation
 - Standby: 3.6mW (Normal)
0.18mW(L-version)
0.18mW(LL-version)
 - Active (60/70/80ns):220/200/180mW
- JEDEC standard pinout
- Available in Plastic SOJ, DIP, ZIP and TSOP -II packages

GENERAL DESCRIPTION

The Samsung KM44V1000C/CL/CLL is a high speed CMOS 1,048,576 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes and mini computers, graphics and high performance microprocessor systems.

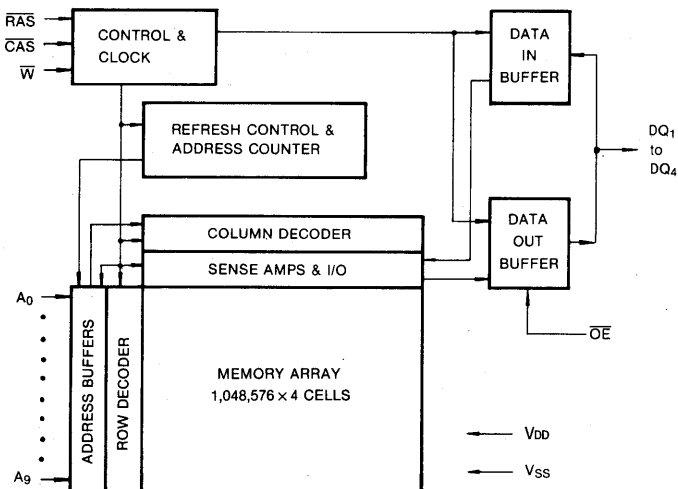
The KM44V1000C/CL/CLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alter native to RAS-only Refresh. All inputs and outputs are fully TTL compatible.

The KM44V1000C/CL/CLL is fabricated using Samsung's advanced CMOS process.

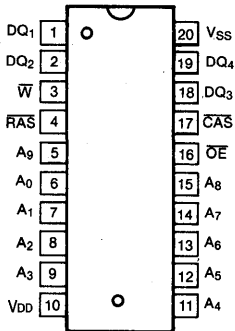
3

FUNCTIONAL BLOCK DIAGRAM

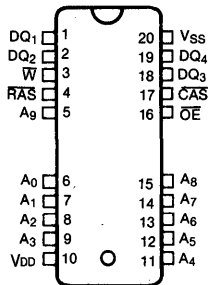


PIN CONFIGURATION (Top Views)

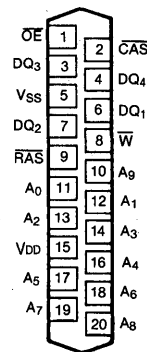
• KM44V1000CP/CLP/CLLP



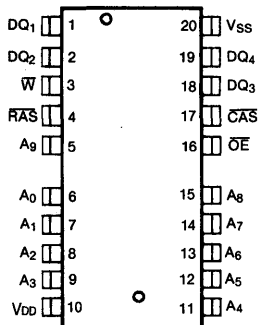
• KM44V1000CJ/CLJ/CLLJ



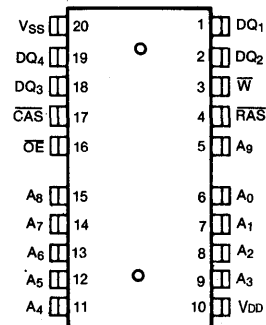
• KM44V1000CZ/CLZ/CLLZ



• KM44V1000CT/CLT/CLLT



• KM44V1000CTR/CLTR/CLLTR



Pin Names	Pin Function
A ₀ -A ₉	Address Inputs
RAS	Row Address Strobe
\bar{CAS}	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
DQ ₁ ~DQ ₄	Data In/Data Out
VDD	Power (+ 3.3V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	- 0.5~V _{DD} + 0.5	V
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	- 0.5 ~ 4.6	V
Storage Temperature	T _{stg}	- 55 to + 150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS}, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	- 0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD} = 3.3V ± 0.3V)
 (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Operating Current* (\overline{RAS} , \overline{CAS} , Address Cycling @trc=min.)	KM44V1000C/CL/CLL-6	-	60	mA
	KM44V1000C/CL/CLL-7	-	55	mA
	KM44V1000C/CL/CLL-8	-	50	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	I _{CC2}	-	1	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @trc=min.)	KM44V1000C/CL/CLL-6	-	60	mA
	KM44V1000C/CL/CLL-7	-	55	mA
	KM44V1000C/CL/CLL-8	-	50	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @tpc=min.)	KM44V1000C/CL/CLL-6	-	45	mA
	KM44V1000C/CL/CLL-7	-	40	mA
	KM44V1000C/CL/CLL-8	-	35	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{DD}-0.2V$)	KM44V1000C	-	500	μA
	KM44V1000CL	-	100	μA
	KM44V1000CLL	-	100	μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44V1000C/CL/CLL-6	-	60	mA
	KM44V1000C/CL/CLL-7	-	55	mA
	KM44V1000C/CL/CLL-8	-	50	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{CAS}=\overline{CAS}$ -Before- \overline{RAS} Cycling or 0.2V DQ1~DQ4=Don't Care TRC=125(L-ver.)μS TRAS=TRAS min.~300ns	KM44V1000CL	-	200	μA
Self Refresh Current $\overline{RAS}=\overline{CAS}=V_{IL}$ $\overline{W}=\overline{OE}=\overline{A0}\sim\overline{A9}=V_{DD}-0.2V$ or 0.2V DQ1~DQ4=V _{DD} -0.2V or 0.2V	KM44V1000CLL	-	150	μA

3



DC AND OPERATING CHARACTERISTICS(Continued)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test=0V)	$I_{i(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{o(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

* Note: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1} , I_{CC3} , I_{CC6} , Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. I_{CC4} , Address can be changed maximum once during a fast page Mode cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance(A_0-A_9)	C_{IN1}	—	5	pF
Input Capacitance(\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	—	7	pF
output Capacitance(DQ_1-DQ_4)	C_{OUT}	—	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time(rise and fall)	t_T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	
Column address hold time referenced to \overline{RAS}	t_{AR}	45		55		60		ns	6
Column address to \overline{RAS} lead time	t_{RAL}	30		35		40		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read command set-up time	trCS	0		0		0		ns	
Read command hold referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	9
Read command hold referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command hold time	twCH	10		15		15		ns	
Write command hold referenced to $\overline{\text{RAS}}$	twCR	45		55		60		ns	6
Write command pulse width	twP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	15		20		20		ns	
Data-inset-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tdHR	45		55		60		ns	6
Refresh period (1024 cycles)	tREF		16		16		16	ms	
Refresh period (L-version/LL-version, 1024 cycles)	tREF		128		128		128	ms	
Write command set-up time	twCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to write enable delay	tcWD	40		40		50		ns	8
$\overline{\text{RAS}}$ to write enable delay	trWD	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		65		70		ns	8
$\overline{\text{CAS}}$ setup time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ cycle)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	trPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test)	tcPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		35		40		45	ns	3
Fast page mode cycle time	tPC	40		45		50		ns	
$\overline{\text{CAS}}$ precharge time(Fast page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	35		40		45		ns	
Fast page mode read-modify-write	tPRWC	80		95		100		ns	
$\overline{\text{RAS}}$ pulse width(Fast Page Mode)	trASP	60	200,000	70	200,000	80	200,000	ns	
Write command set-up time (test mode in)	twTS	10		10		10		ns	
Write command hold time (test mode in)	twTH	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	twRP	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	twRH	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	trOH	15		20		20		ns	
$\overline{\text{OE}}$ access time	toEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	toED	15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toEZ	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	toEH	15		20		20		ns	
$\overline{\text{RAS}}$ pulse width($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	trASS	100		100		100		μs	13
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	trPS	110		130		150		ns	13
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	13

3

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	115		135		155		ns	
Read-modify-write cycle time	trwc	160		190		210		ns	
Access time from RAS	trac		65		75		85	ns	3,4,11
Access time from CAS	tcac		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
RAS pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
CAS pulse width	tcAS	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	trSH	20		25		25		ns	
CAS hold time	tCSH	65		75		85		ns	
Column address to RAS lead time	trAL	35		40		45		ns	
CAS to write enable delay	tcWD	45		45		55		ns	8
RAS to write enable delay	trWD	90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	60		70		75		ns	8
Fast mode cycle time	tpc	45		50		55		ns	
Fast page mode read-modify-write	tpRWC	85		100		105		ns	
RAS pulse width(Fast page mode)	trASP	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tcPA		40		45		50	ns	3
\bar{OE} access time	toEA		20		25		25	ns	
\bar{OE} to data delay	toED	20		25		25		ns	
\bar{OE} command hold time	toEH	20		25		25		ns	

NOTES

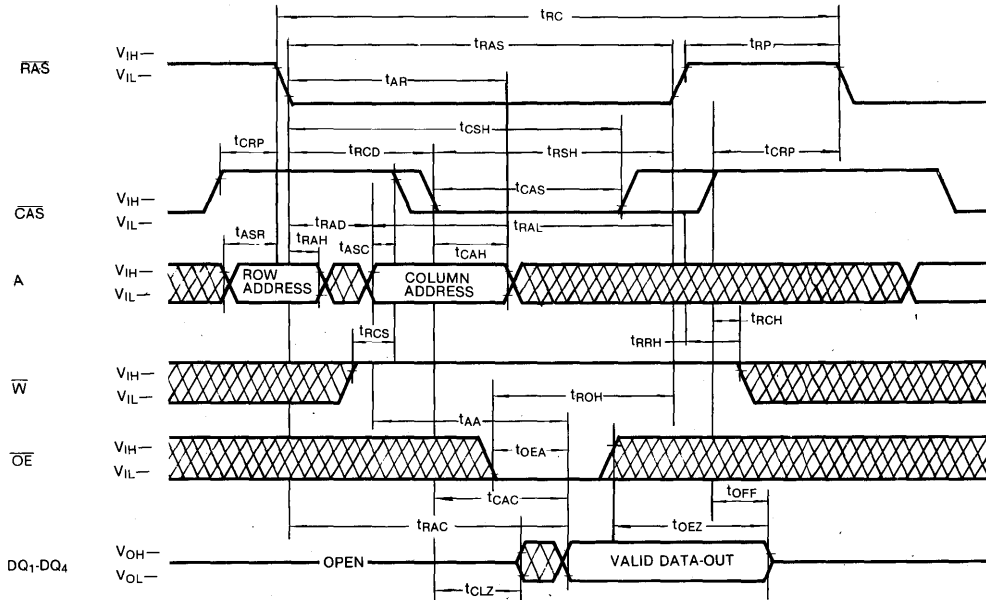
1. An initial pause of 200 μ s is required after power-up followed by and 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL load and 100pF, and $V_{OH}=2.0V$, $V_{OL}=0.8V$
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\text{max})$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$

the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.

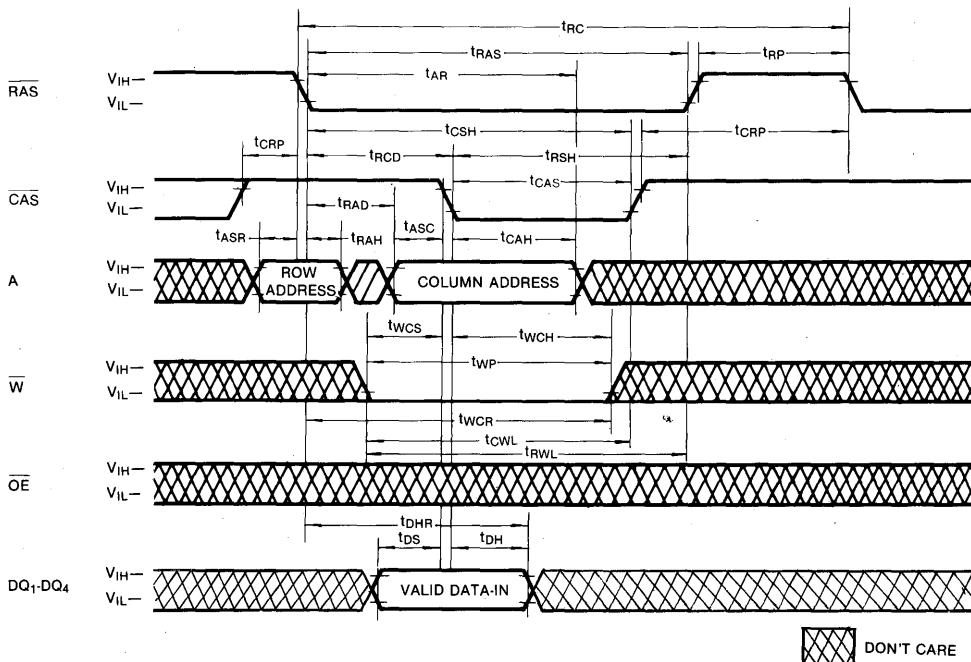
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \bar{CAS} leading edge in early write cycles and to the \bar{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

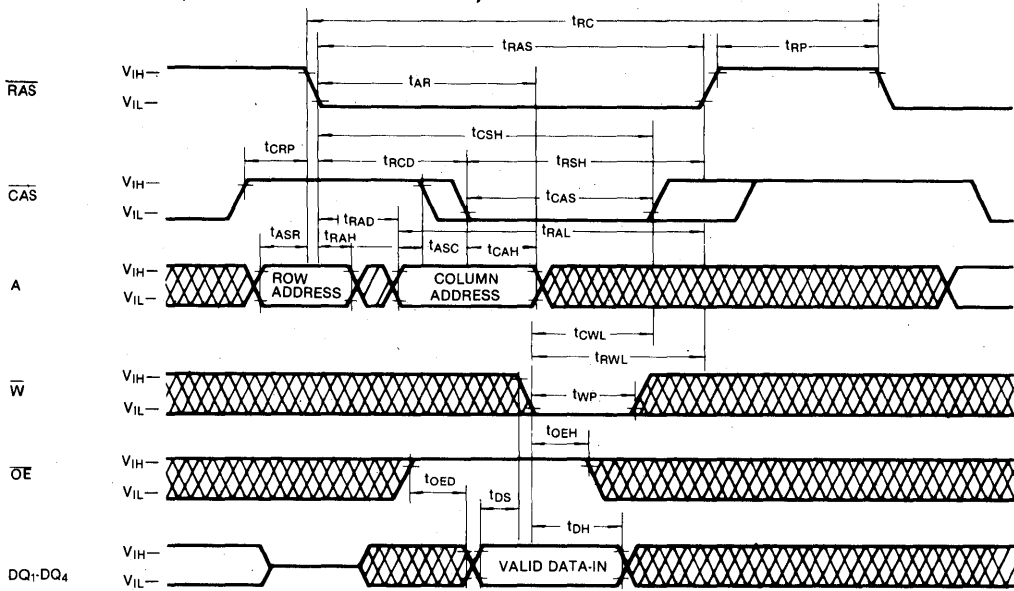


 DON'T CARE

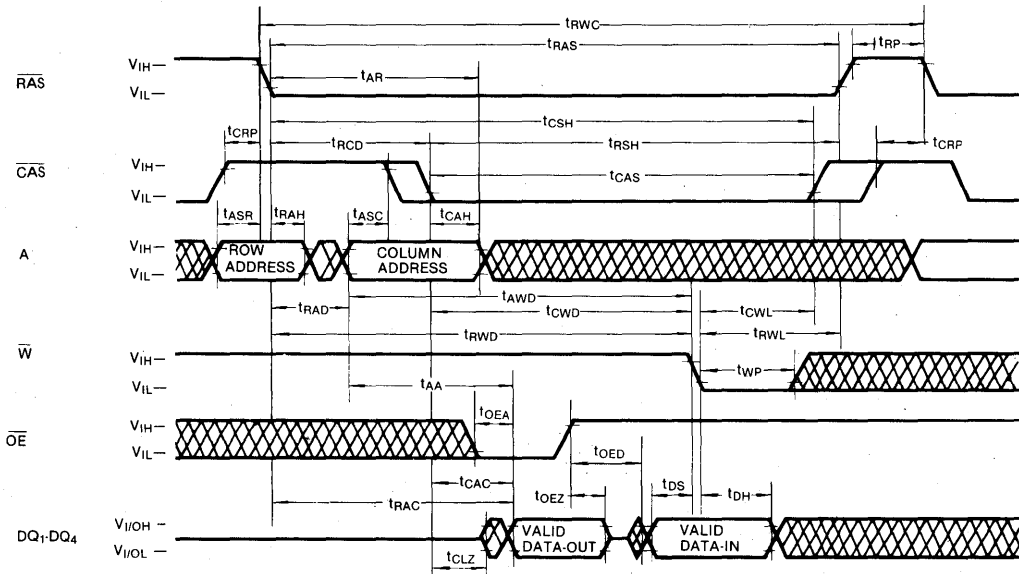
3


TIMING DIAGRAMS (Continued)

WRITE CYCLE (OE CONTROLLED WRITE)



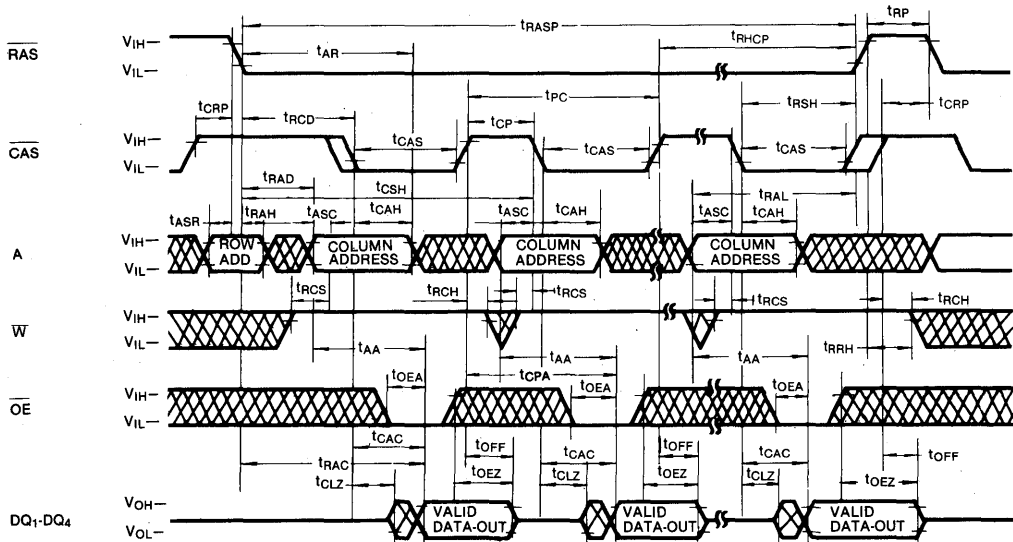
READ-MODIFY-WRITE CYCLE



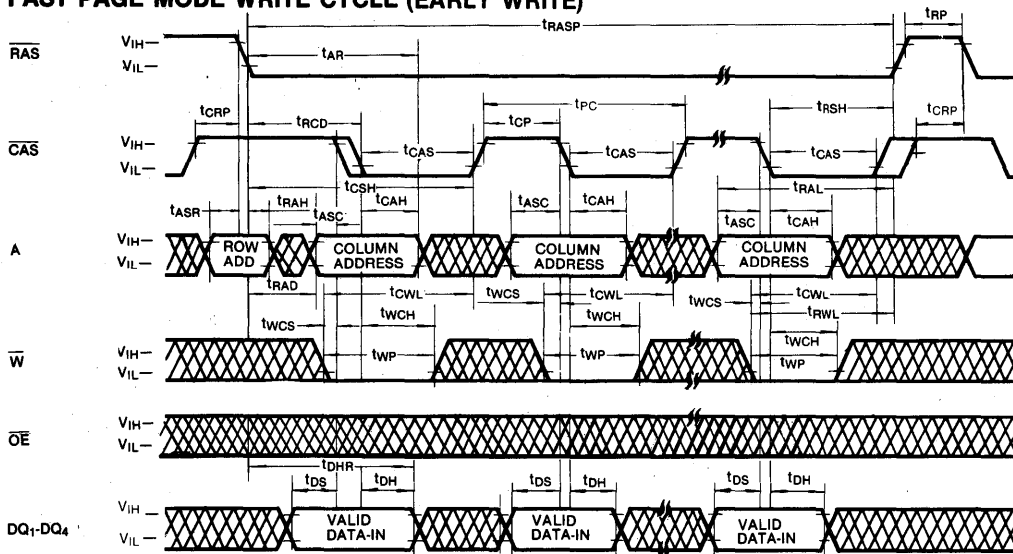
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



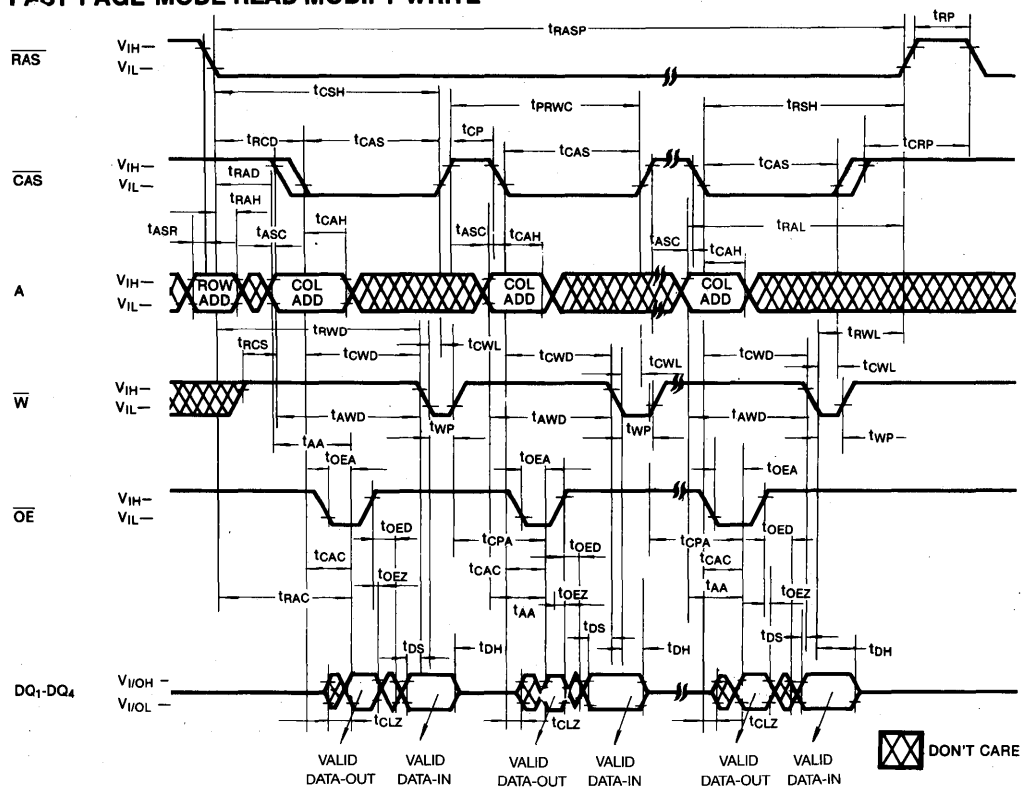
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

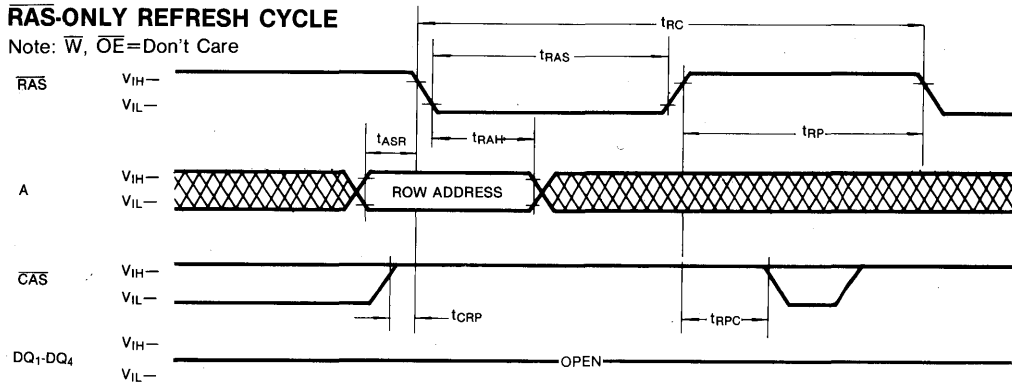
FAST PAGE MODE READ-MODIFY-WRITE



TIMING DIAGRAMS (Continued)

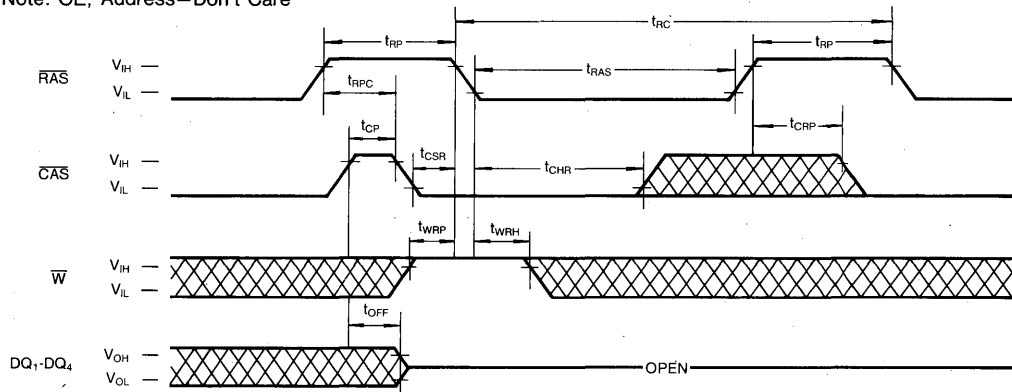
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} =Don't Care



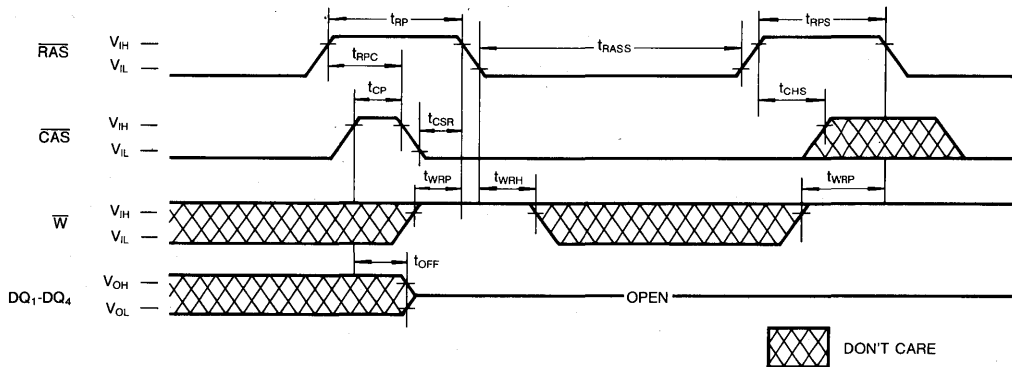
CAS-BEFORE-RAS REFRESH CYCLE

Note: \overline{OE} , Address=Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-ver only)

Note: \overline{OE} , Address: Don't Care

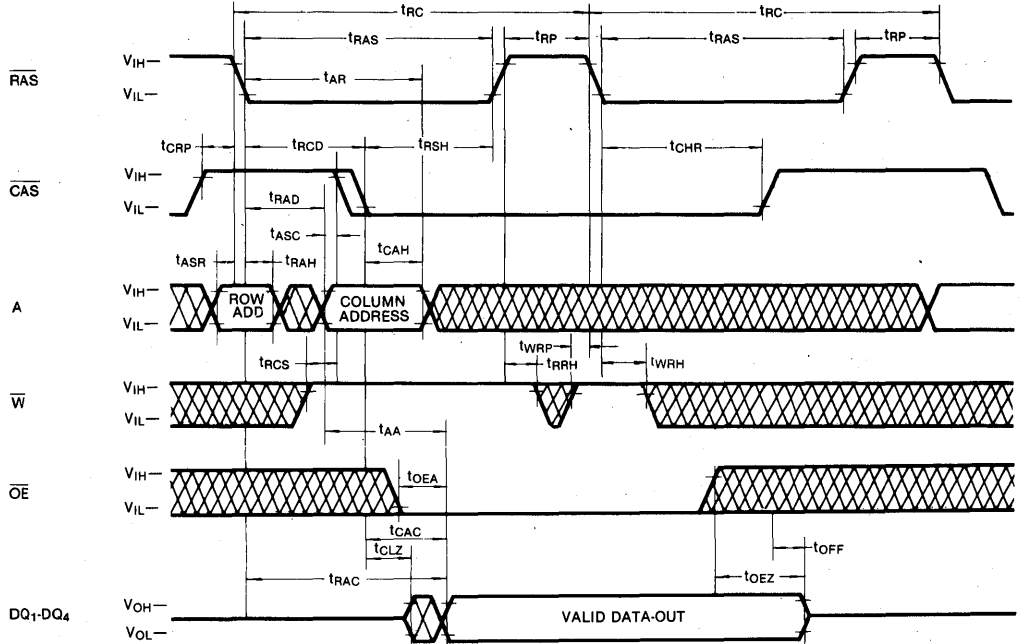


 DON'T CARE

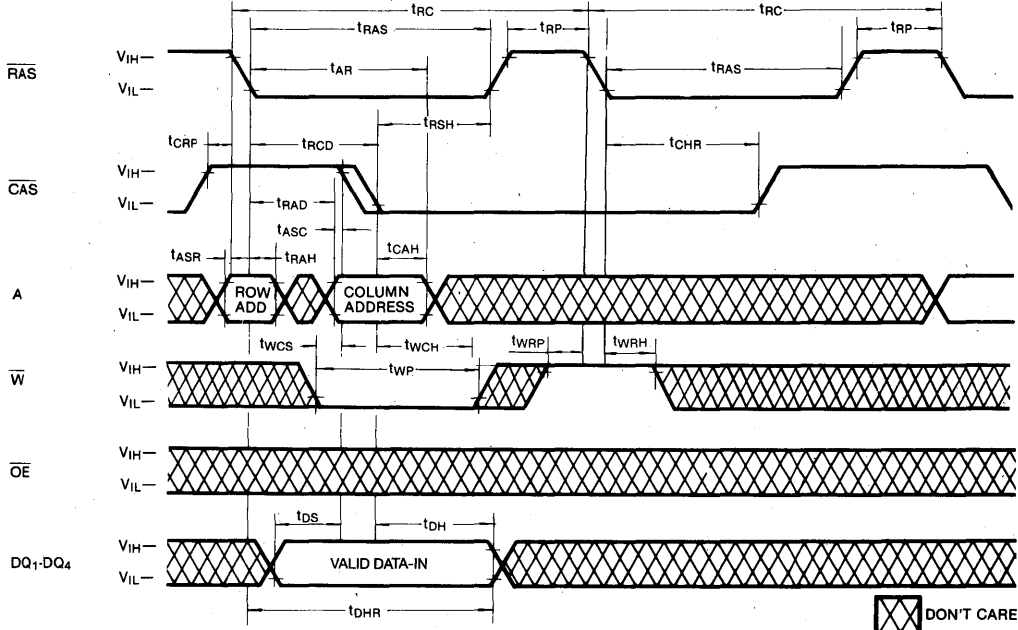
3

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



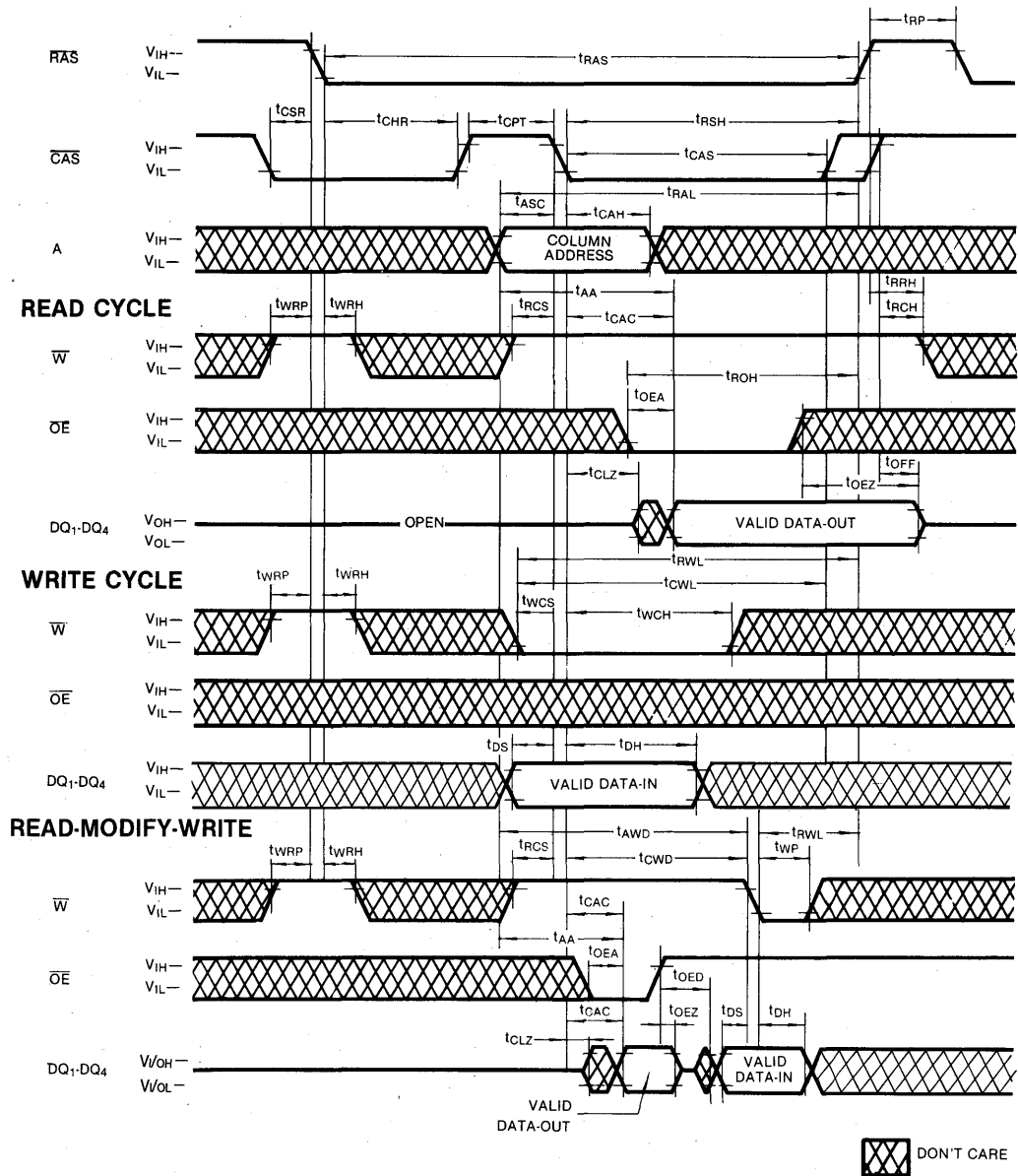
HIDDEN REFRESH CYCLE (WRITE)



DON'T CARE

TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

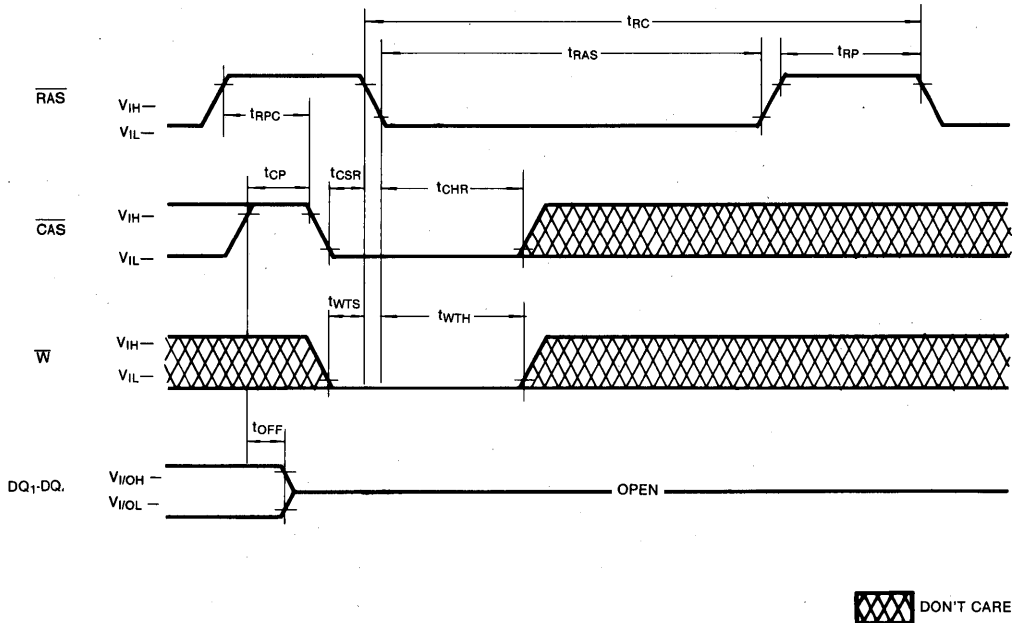


3

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: \overline{OE} , Address=Don't Care



TEST MODE DESCRIPTION

The KM44V1000C/CL/CSL is the RAM organized 1,048,576 words by 4 bit internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M x 4 DRAM

can be tested as if it were a 512K x 4 DRAM. \overline{W} , \overline{CAS} -Before- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode", And " \overline{CAS} -Before- \overline{RAS} Refresh Cycle" or " \overline{RAS} -only-Refresh Cycle" puts it back into "Normal Mode". During the test mode operation, a WCBR cycle is used to perform refresh. The "Test Mode" function reduces test time (1/2 in cases of N test pattern.)

DEVICE OPERATION

DEVICE OPERATION

The KM44V1000C/CL/CLL contains 4,194,304 memory locations. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44V1000C/CL/CLL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0 - A_9) and 10 column (A_{10} - A_{19}) addresses. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}), and the valid row and column address inputs.

Operating of the KM44V1000C/CL/CLL begins by strobing in valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 10 address input pins (A_0 - A_9) is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM44V1000C/CL/CLL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

\overline{RAS} and \overline{CAS} Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44V1000C/CL/CLL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition.

If \overline{CAS} goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAC(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However, if \overline{CAS} goes low after $t_{RCD(max)}$, or if the column address becomes valid after $t_{RAC(max)}$, access is specified by t_{RAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAC(max)}$. The KM44V1000C/CL/CLL has common data

I/O pins

This reason an output enable control input (\overline{OE}) has been provided so the output buffer can be precisely controlled. For data to appear at the output, \overline{OE} must be low for the period of time defined by t_{OE} and t_{OEZ} .

Write

The KM44V1000C/CL/CLL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} and \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early cycle the output buffers remain in the three state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If \overline{W} is brought low after \overline{CAS} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} , t_{CWD} and t_{LWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44V1000C/CL/CLL has three-state output buffer which are controlled by \overline{CAS} and \overline{OE} . Whenever \overline{CAS} and \overline{OE} are high (V_{IH}), the outputs is in the high impedance state. In any cycle in which valid data appears at the output the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until \overline{CAS} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM44V1000C/CL/CLL operating cycles is listed below after the corresponding output state produced by the

DEVICE OPERATION (Continued)

cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, \overline{RAS} -only Refresh, Fast Page Mode Write, \overline{CAS} -before- \overline{RAS} Refresh, \overline{OE} controlled write.

Indeterminate Output State: Delayed Write(t_{DWB} or t_{DWD} are not met)

Refresh

The data in the KM44V1000C/CL/CLL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 (L,LL-ver:128ms). There are several ways to accomplish this.

\overline{RAS} -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with \overline{RAS} while \overline{CAS} remains high. This cycle must be repeated for each row.

\overline{CAS} -before- \overline{RAS} Refresh: The KM44V1000C/CL/CLL has \overline{CAS} -before- \overline{RAS} on-chip refresh capability that eliminates the need for external refresh addresses. If \overline{CAS} is held low for the specified set up time (t_{CSR}) before \overline{RAS} goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next \overline{CAS} -before- \overline{RAS} refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the \overline{CAS} active time and cycling \overline{RAS} . The KM44V1000C/CL/CLL hidden refresh cycle is actually a \overline{CAS} -before- \overline{RAS} refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Other Refresh Methods: It is also possible to refresh the KM44V1000C/CL/CLL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh is the preferred method.

Fast Page Mode

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while \overline{RAS} is kept low to maintain the \overline{CAS} is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

\overline{CAS} -before- \overline{RAS} Refresh Counter Test Cycle

A special timing sequence using the \overline{CAS} -before- \overline{RAS} counter test cycle provides a convenient method of verifying the functionality of the \overline{CAS} -before- \overline{RAS} refresh activated circuitry.

After the \overline{CAS} -before- \overline{RAS} refresh operation, is \overline{CAS} goes high and then low again while \overline{RAS} is held low, the read and write operations are enabled.

This is shown in the \overline{CAS} -before- \overline{RAS} counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address- Bits A_0 through A_9 are supplied by the on-chip refresh counter.

Column Address- Bits A_0 through A_9 are supplied -in by the falling edge of \overline{CAS} as in a normal memory cycle.

Suggested \overline{CAS} -before- \overline{RAS} counter Test Procedure

The \overline{CAS} -before- \overline{RAS} refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 \overline{CAS} -before- \overline{RAS} cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycles, red the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44V1000C/CL/CLL could possibly begin an active cycle. This condition results in higher than necessary current demands from

DEVICE OPERATION (Continued)

the power supply during power-up. It is recommended that \overline{RAS} and \overline{CAS} track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μ sec is required after power-up followed by 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16 msec period in which there are no \overline{RAS} cycles. An initialization cycle is any cycle in which \overline{RAS} is cycled.

Termination

The lines from the TTL driver circuits to the KM44V1000C/CL/CLL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44V1000C/CL/CLL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like

transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

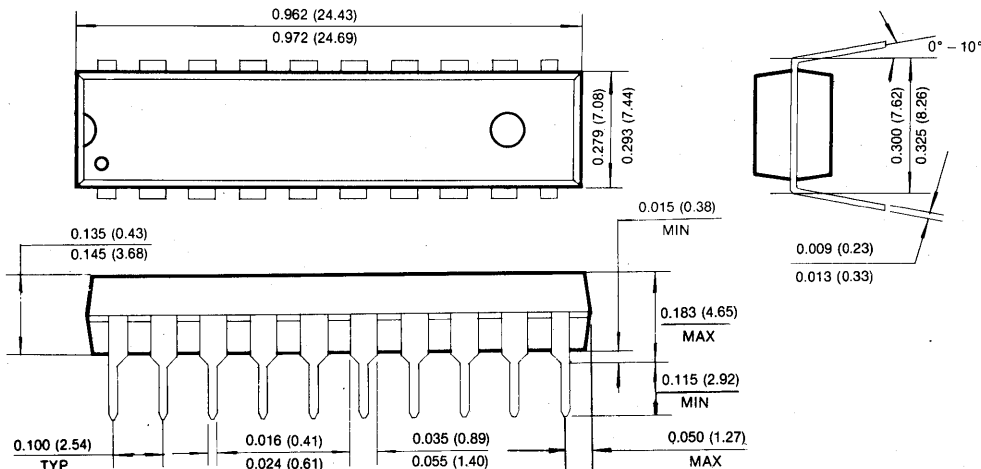
A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44V1000C/CL/CLL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44V1000C/CL/CLL and they supply much of the current used by the KM44V1000C/CL/CLL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

Units: Inches (Millimeters)

PACKAGE DIMENSIONS

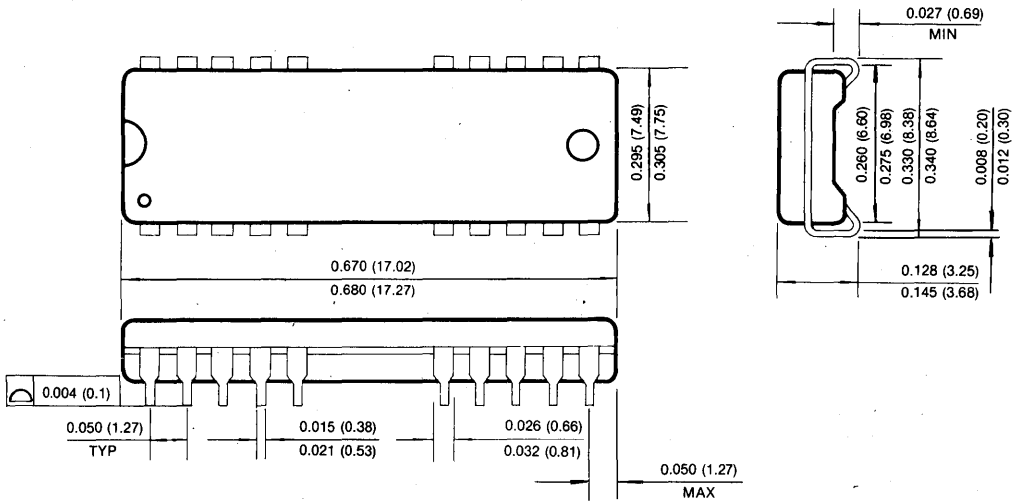
20-LEAD PLASTIC DUAL IN-LINE PACKAGE



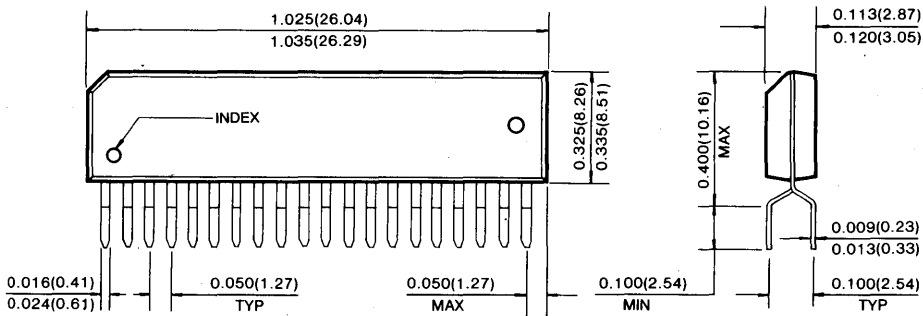
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



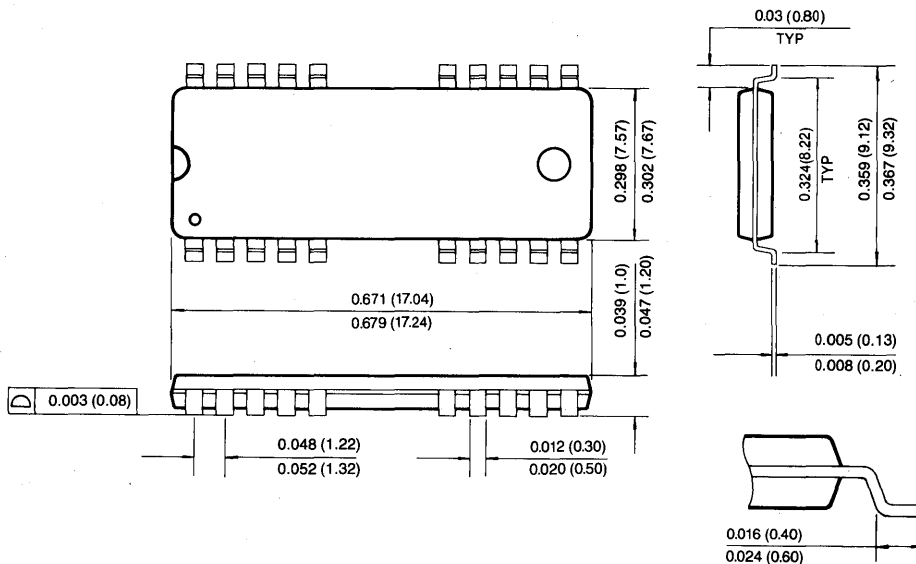
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

Units: Inches (millimeters)



3

1M × 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- Performance range:

	trAC	tCAC	trC	tHPC
KM44V1004C/CL/CLL-6	60ns	15ns	110ns	24ns
KM44V1004C/CL/CLL-7	70ns	20ns	130ns	29ns
KM44V1004C/CL/CLL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with extended data out
- Self refresh operation (LL-ver.)
- CAS-before-RAS refresh capability
- RAS-only and hidden refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single +3.3V ± 0.3V power supply
- 1024 cycles/16ms refresh (Normal)
- 1024 cycles/128ms refresh (L/LL-ver)
- Power dissipation
 - Standby : 3.6mW(Normal)
0.36mW(L-ver)
0.36mW(LL-ver)
 - Active(60/70/80) : 220/200/180mW
- JEDEC standard pinout
- Available in plastic DIP, SOJ, ZIP and TSOP(II)

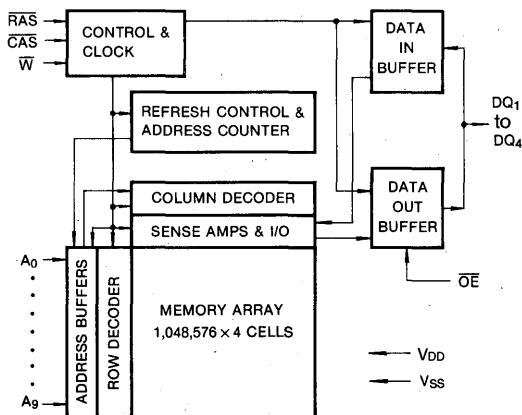
GENERAL DESCRIPTION

The Samsung KM44V1004C/CL/CLL is a CMOS high speed 1,048,576 × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM44V1004C/CL/CLL features EDO Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

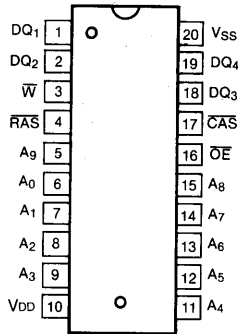
The KM44V1004C/CL/CLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

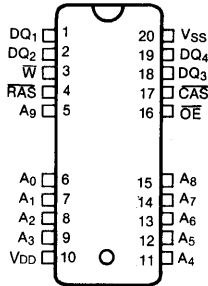


PIN CONFIGURATION (Top Views)

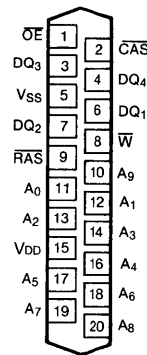
• KM44V1004CP/CLP/CLLP



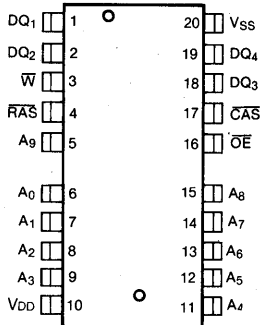
• KM44V1004CJ/CLJ/CLLJ



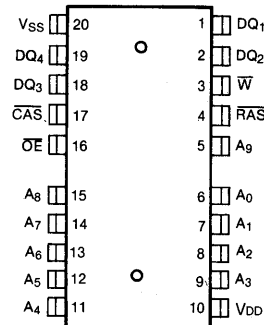
• KM44V1004CZ/CLZ/CLLZ



• KM44V1004CT/CLT/CLLT



• KM44V1004CTR/CLTR/CLLTR



Pin Names	Pin Function
A ₀ -A ₉	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
DQ ₁ ~DQ ₄	Data In/Data Out
VDD	Power (+3.3V)
VSS	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5~ 4.6	V
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.5~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	600	mW
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @ t _{RC} =min.)	KM44V1004C/CL/CLL-6		60	mA
	KM44V1004C/CL/CLL-7		55	mA
	KM44V1004C/CL/CLL-8		50	mA
Standby Current (RAS=CAS=W=V _{IH})	KM44V1004C		500	μA
	KM44V1004CL		500	μA
	KM44V1004CCLL		500	μA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @ t _{RC} =min.)	KM44V1004C/CL/CLL-6		60	mA
	KM44V1004C/CL/CLL-7		55	mA
	KM44V1004C/CL/CLL-8		50	mA
EDO Mode Current* (RAS=V _{IL} , CAS, Address Cycling @ t _{PC} =min.)	KM44V1004C/CL/CLL-6		60	mA
	KM44V1004C/CL/CLL-7		55	mA
	KM44V1004C/CL/CLL-8		50	mA
Standby Current (RAS=CAS=W=V _{DD} -0.2V)	KM44V1004C		1	mA
	KM44V1004CL		100	μA
	KM44V1004CCLL		100	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @ t _{RC} =min.)	KM44V1004C/CL/CLL-6		60	mA
	KM44V1004C/CL/CLL-7		55	mA
	KM44V1004C/CL/CLL-8		50	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DQ1-DQ4=Don't Care t _{RC} =125μs t _{RAS} =t _{RAS} min.~300ns	KM44V1004CL		200	μA
Self Refresh Current RAS=CAS=V _{IL} W=OE=A0-A9=V _{DD} -0.2V or 0.2V DQ1-DQ4=V _{DD} -0.2V, 0.2V or Open	KM44V1004CCLL		150	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	$I_{i(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{o(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4} , Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 - A_9$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{OE})	C_{IN2}	-	7	pF
Output Capacitance ($DQ_1 - DQ_4$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Test Condition : $V_{IH}/V_{IL} = 2.0V/0.8V$, $V_{OH}/V_{OL} = 2.0V/0.8V$, Output Loading $C_L = 100pF$

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from \overline{RAS}	trac		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	3		3		3		ns	3
\overline{OE} to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	tCEZ	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	tt	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	trp	40		50		60		ns	
\overline{RAS} pulse width	trAS	60	10K	70	10K	80	10K	ns	
\overline{RAS} hold time	trSH	15		20		20		ns	
\overline{CAS} hold time	tcSH	50		60		70		ns	
\overline{CAS} pulse width	tcAS	10	10K	15	10K	20	10K	ns	16
\overline{RAS} to \overline{CAS} delay time	trCD	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	trAD	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tcRP	5		5		5		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t _{AR}	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		40		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	9
Write command hold time	t _{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t _{WCR}	45		55		60		ns	6
Write command pulse width	t _{WP}	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	10		15		20		ns	
Data set-up time	t _{DS}	0		0		0		ns	10
Data hold time	t _{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	45		55		60		ns	6
Refresh period (Normal)	t _{REF}		16		16		16	ms	
Refresh period (L-ver & LL-ver)	t _{REF}		128		128		128	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	55		65		70		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	60		70		75		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		10		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	t _{CPT}	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40		45	ns	3
Hyper Page cycle time	t _{HPC}	24		29		34		ns	16
Hyper Page read-modify-write cycle time	t _{HPRWC}	73		88		98		ns	
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	t _{RASP}	60	200K	70	200K	80	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	35		40		45		ns	
$\overline{\text{OE}}$ access time	t _{OEa}		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	t _{OEED}	15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	t _{OEZ}	3	15	3	20	3	20	ns	7,14

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} command hold time	TOEH	15		20		20		ns	
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	TWRP	10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	TWRH	10		10		10		ns	
Output data hold time	TDOH	5		5		5		ns	
Output buffer turn off delay form \overline{RAS}	TREZ	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay form \overline{W}	TWEZ	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	TWED	15		20		20		ns	
\overline{OE} to \overline{CAS} hold time	TOCH	5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	TCHO	5		5		5		ns	
\overline{OE} precharge time	TOEP	5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	TWPE	5		5		5		ns	
\overline{RAS} pulse width (\overline{C} - \overline{B} - \overline{R} self refresh)	TRASS	100		100		100		μ s	17
\overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} self refresh)	TRPS	110		130		150		ns	17
\overline{CAS} hold time (\overline{C} - \overline{B} - \overline{R} self refresh)	TCHS	-50		-50		-50		ns	17

3

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	TRC	115		135		155		ns	
Read-modify-write cycle time	TRWC	160		190		210		ns	
Access time from \overline{RAS}	TRAC		65		75		85	ns	3,4,11
Access time from \overline{CAS}	TCAC		20		20		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\overline{RAS} pulse width	TRAS	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	tcAS	18	10,000	20	10,000	20	10,000	ns	
\overline{RAS} hold time	TRSH	20		25		25		ns	
\overline{CAS} hold time	tCSH	55		65		70		ns	
Column address to \overline{RAS} lead time	TRAL	35		40		45		ns	
\overline{CAS} to \overline{W} delay time	tcWD	45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	60		70		75		ns	8
Hyper Page mode cycle time	tHPC	29		34		39		ns	16
Hyper Page mode read-modify-write cycle time	tHPRWC	78		93		103		ns	
\overline{RAS} pulse width (Hyper Page Mode)	trASP	65	200,000	75	200,000	85	200,000	ns	

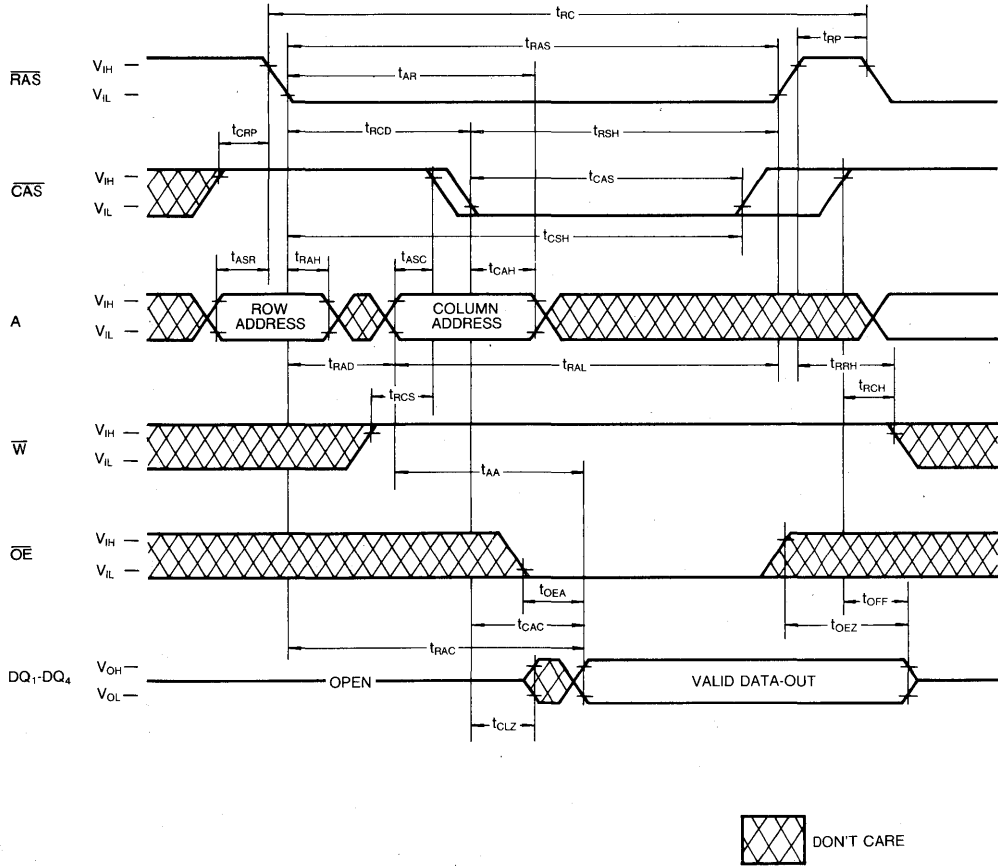
TEST MODE CYCLE(Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are assumed to be 5ns for all inputs except tHPC and tHPRWC.
3. Measured with a load equivalent to 1TTL load and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. twcs, trwd, tcwd and tawd are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twcs \geq twcs(min) the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcwd \geq tcwd(min), trwd \geq trwd(min) and tawd \geq tawd(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tCEZ(max), tREZ(max), tWEZ(max) and tO EZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
16. tASC \geq tCP min, Assumt t τ =2.0ns
17. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.(LL-ver)

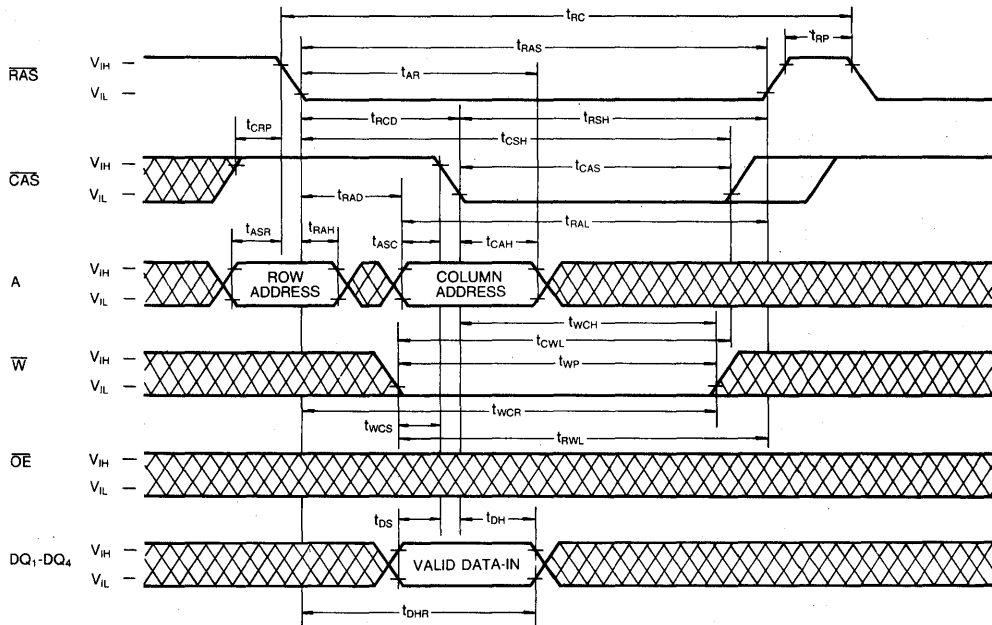
TIMING DIAGRAMS
READ CYCLE



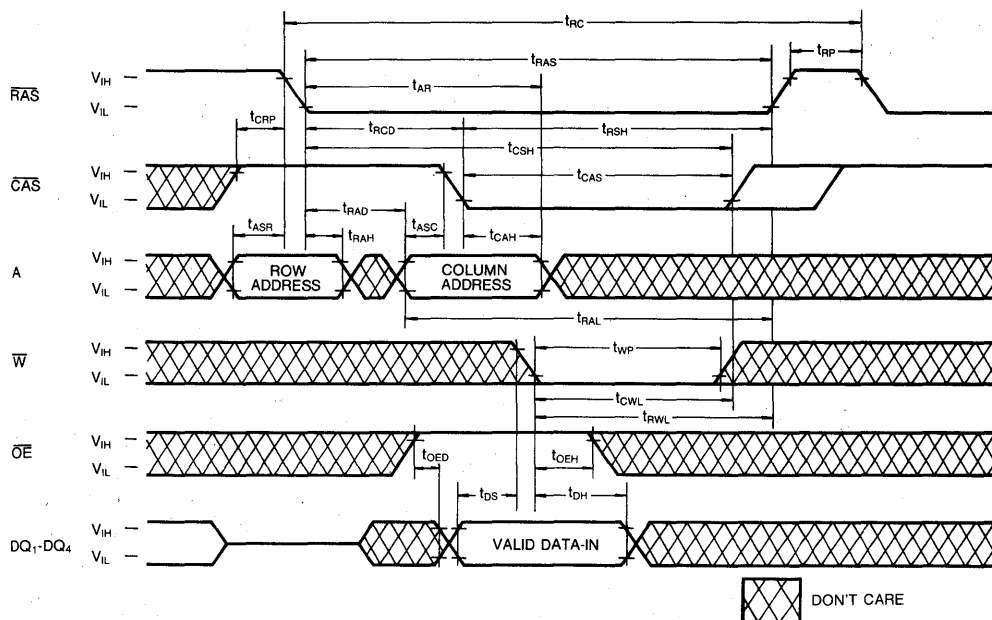
3

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

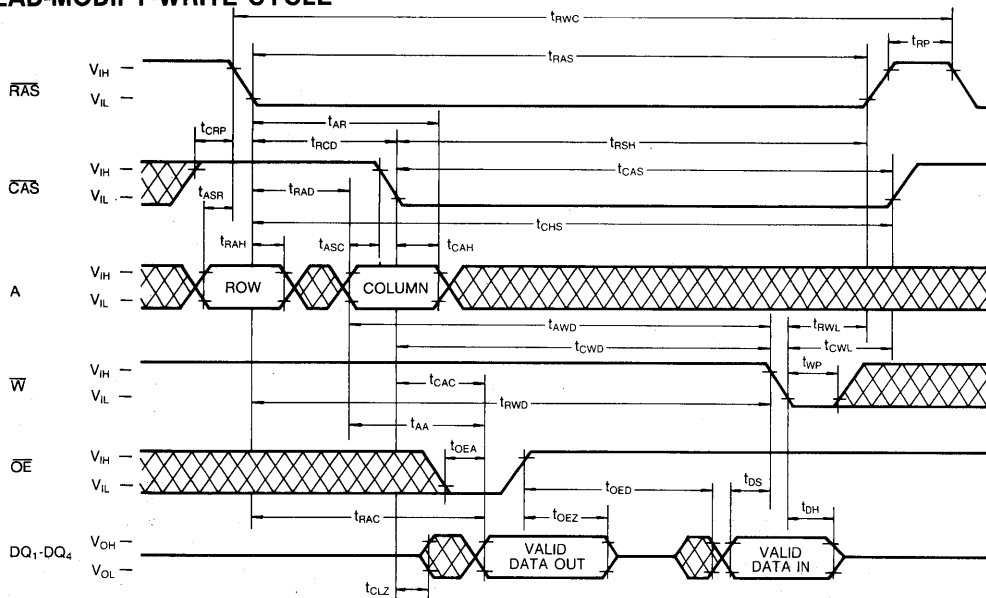


WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



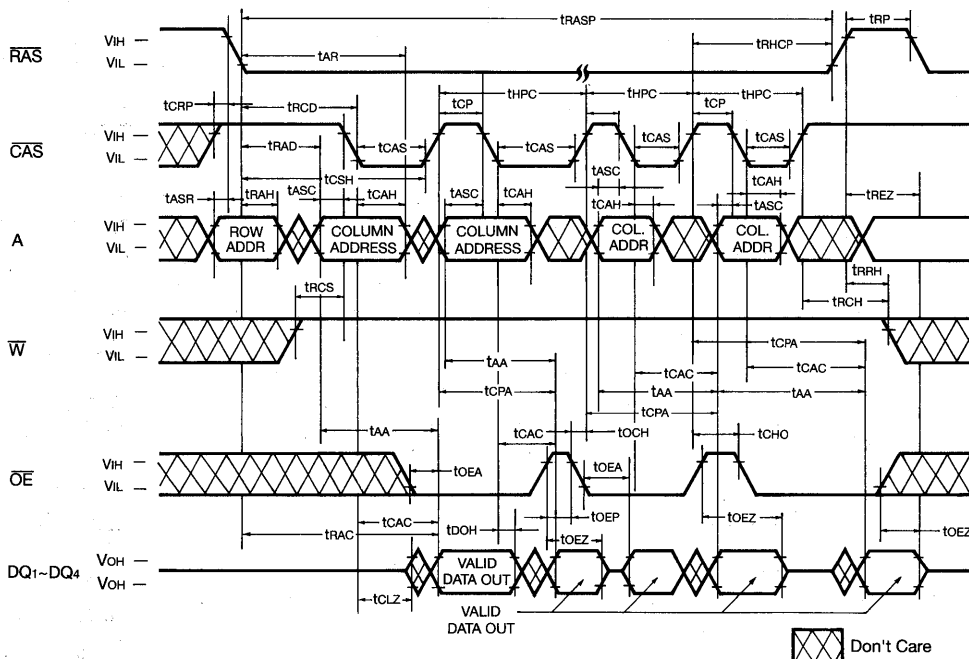
TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



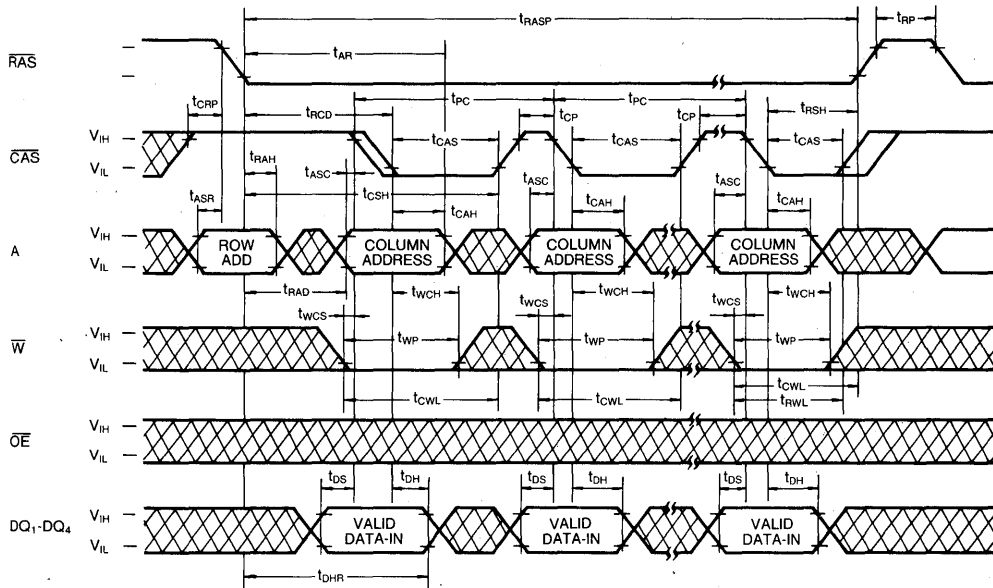
3

HYPER PAGE READ CYCLE

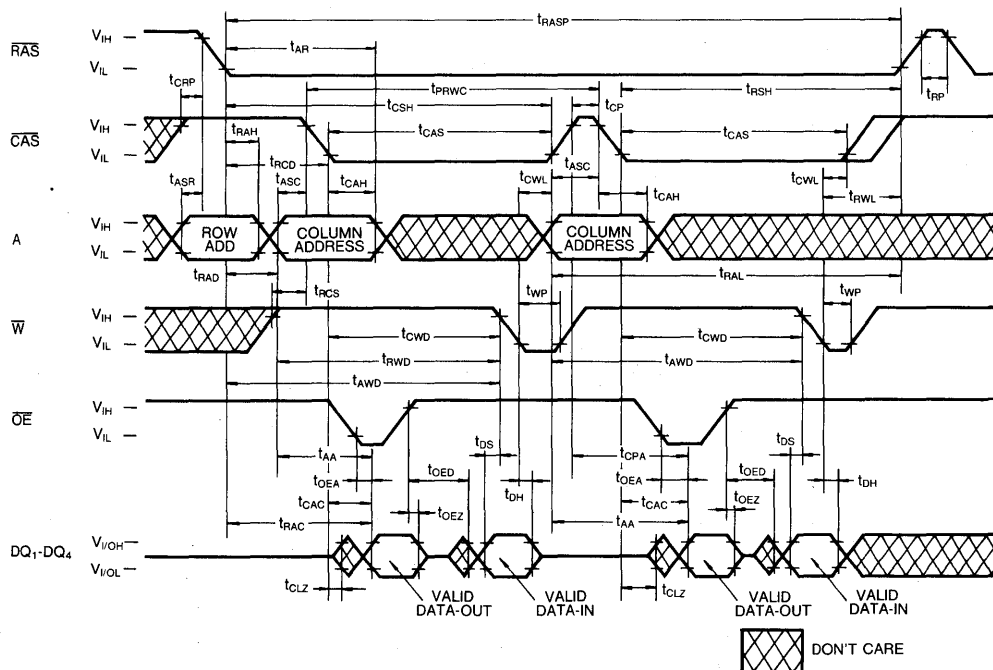


TIMING DIAGRAMS (Continued)

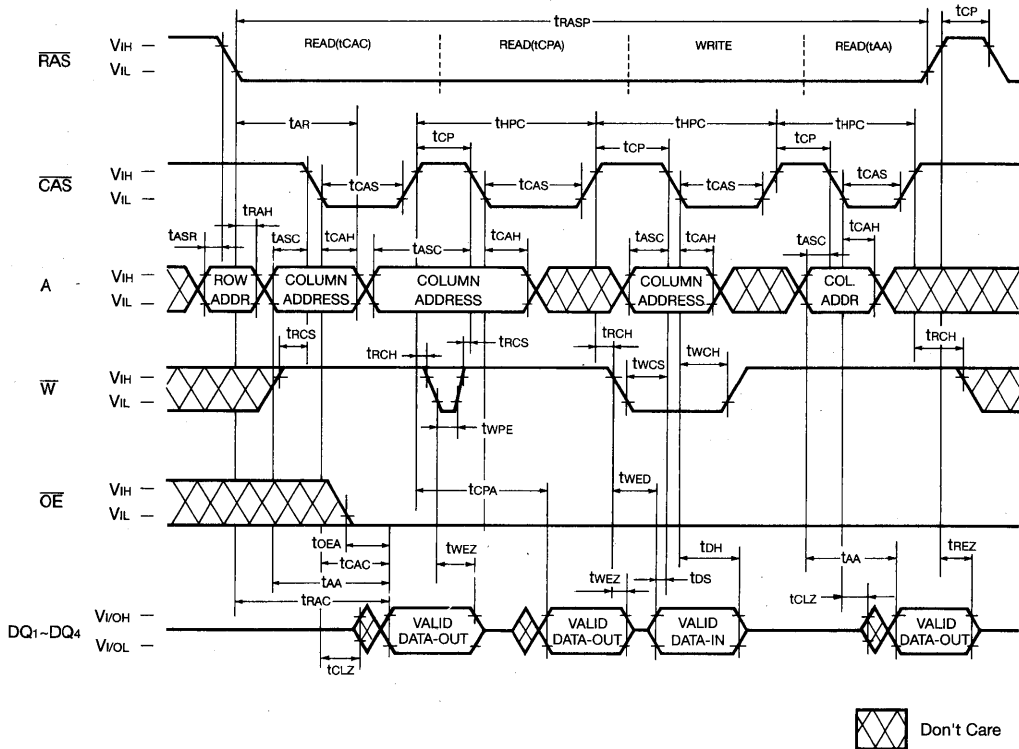
FAST PAGE MODE WITH EDO WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE WITH EDO READ-MODIFY-WRITE CYCLE



PAGE WITH EDO READ AND WRITE MIXED CYCLE

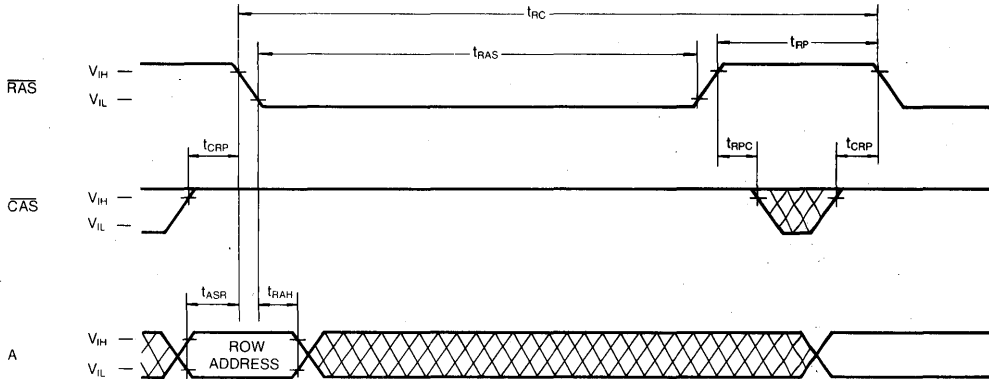


3

TIMING DIAGRAMS (Continued)

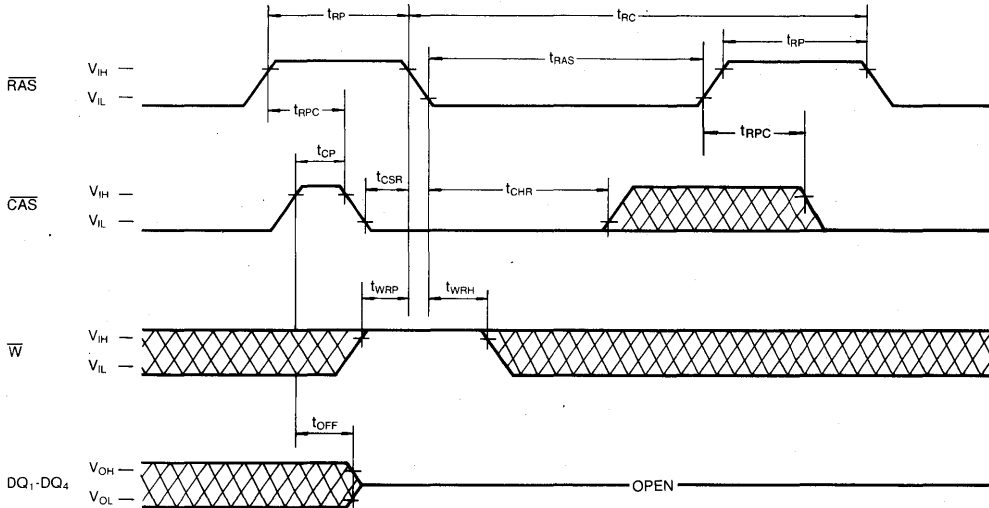
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

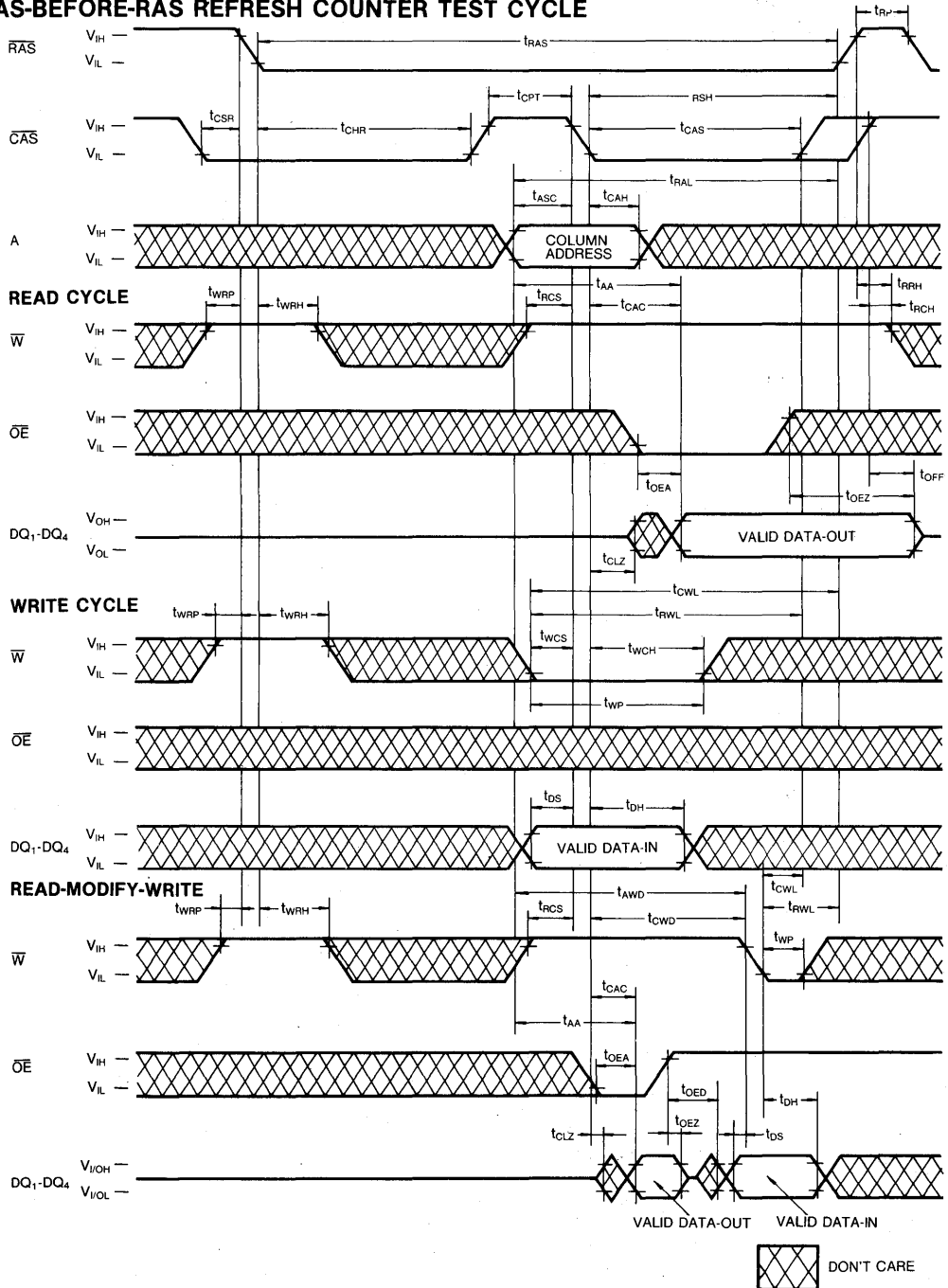
Note: \overline{OE} , Address=Don't Care



 DONT CARE

TIMING DIAGRAMS (Continued)

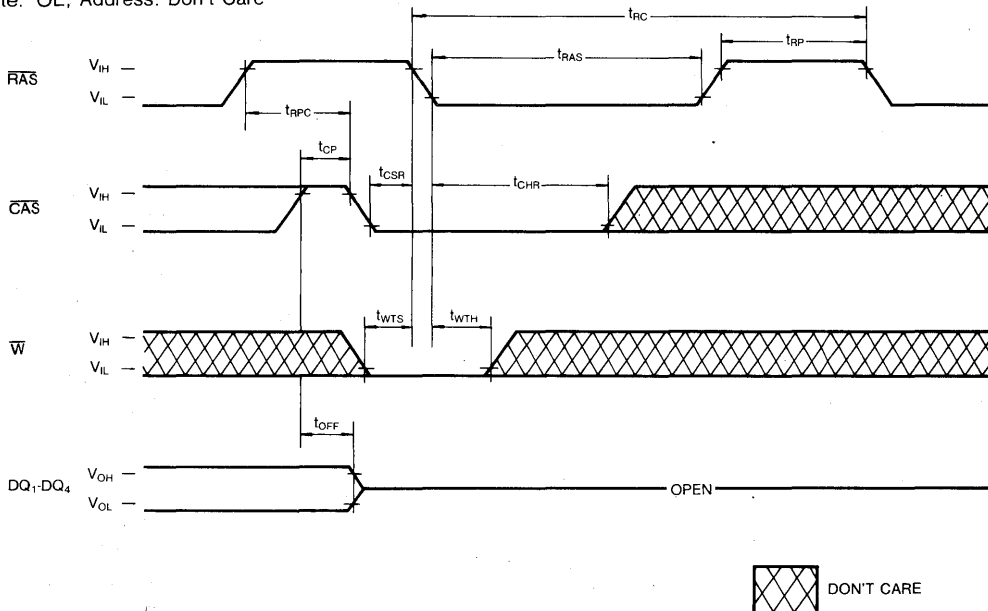
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



3

TEST MODE DESCRIPTION

The KM44V1004C/CL/CLL is the RAM organized 1, 048,576 words by 4 bit, it is internally organized 524, 288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A_0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would

indicate a "0". In "Test Mode", the $1M \times 4$ DRAM can be tested as if it were a $512K \times 4$ DRAM. \overline{W} , \overline{CAS} -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And \overline{CAS} -BEFORE- \overline{RAS} REFRESH CYCLE" or " \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

DEVICE OPERATION

The KM44V1004C/CL/CLL contains 4,194,304 memory locations. Twenty address bits are required to address a particular 4-bit word in the memory array. Since the KM44V1004C/CL/CLL has only 10 address input pins, time multiplexed addressing is used to input 10 row (A_0 - A_9) and 10 column (A_0 - A_9) address. The multiplexing is controlled by the timing relationship between the row address strobe (\overline{RAS}), the column address strobe (\overline{CAS}), and the valid row and column address inputs.

Operating of the KM44V1004C/CL/CLL begins by strobing in a valid row address with \overline{RAS} while \overline{CAS} remains high. Then the address on the 10 address input pins (A_0 - A_9) is changed from a row address to a column address and is strobed in by \overline{CAS} . This is the beginning of any KM44V1004C/CL/CLL cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both \overline{RAS} and \overline{CAS} have returned to the high state. Another cycle can be initiated after \overline{RAS} remains high long enough to satisfy the \overline{RAS} precharge time (t_{RP}) requirement.

RAS and CAS Timing

The minimum \overline{RAS} and \overline{CAS} pulse widths are specified by $t_{RAS(min)}$ and $t_{CAS(min)}$ respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing \overline{RAS} low, it must not be aborted prior to satisfying the minimum \overline{RAS} and \overline{CAS} pulse widths. In addition, a new cycle must not begin until the minimum \overline{RAS} precharge time, t_{RP} , has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM44V1004C/CL/CLL begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input (\overline{W}) high during a $\overline{RAS}/\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of \overline{RAS} . But the access time also depends on the falling edge of \overline{CAS} and on the valid column address transition. If \overline{CAS} goes low before $t_{RCD(max)}$ and if the column address is valid before $t_{RAC(max)}$, then the access time to valid data is specified by $t_{RAC(min)}$. However, if \overline{CAS} goes low after $t_{RCD(max)}$, access is specified by t_{CAC} or t_{AA} . In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$. The KM44V1004C/CL/CLL has common data I/O pins. This is the reason an output enable control input (\overline{OE}) has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, \overline{OE} must be low for the period of time defined by t_{OEa} and t_{OEz} .

Write

The KM44V1004C/CL/CLL can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between \overline{W} , \overline{OE} and \overline{CAS} . In any type of write cycle, Data-in must be valid at or before the falling edge of \overline{W} or \overline{CAS} , whichever is later.

Early Write: An early write cycle is performed by bringing \overline{W} low before \overline{CAS} . The data at the data input pins is written into the addressed memory cells. Throughout the early write cycle the output remains in the Hi-Z state. In the early write cycle the output buffers remain in the three state regardless of the state of the \overline{OE} input.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing \overline{W} low after \overline{CAS} and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If \overline{W} is brought low after \overline{CAS} , a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} , t_{CWD} and t_{AWD} , are not necessarily met. The state of data-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The KM44V1004C/CL/CLL has a three-state output buffer which is controlled by \overline{RAS} , \overline{CAS} and \overline{OE} . When \overline{RAS} and \overline{CAS} go high (V_{IH}) or \overline{OE} goes high (V_{IH}), the outputs are in the high impedance state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of \overline{CAS} . Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC} , t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data at the output cannot be eliminated by \overline{CAS} rising only and it remains until both \overline{RAS} and \overline{CAS} returns high. This is true even if a new \overline{RAS} cycle occurs (as in hidden refresh). Each of the KM44V1004C/CL/CLL operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, EDO Mode Read, EDO Mode Read-Modify-Write.

DEVICE OPERATION (Continued)

Hi-Z Output State: Early Write, \overline{RAS} -only Refresh, Fast Page with EDO Mode Write, \overline{CAS} -before- \overline{RAS} Refresh, \overline{OE} controlled write.

Indeterminate Output State: Delayed Write (tcwd or trwd are not met)

Refresh

The data in the KM44V1004C/CL/CLL is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16/128/256ms. There are several ways to accomplish this.

\overline{RAS} -Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with \overline{RAS} while \overline{CAS} remains high. This cycle must be repeated for each row.

\overline{CAS} -before- \overline{RAS} Refresh: The KM44C1004C/CL/CLL has \overline{CAS} -before- \overline{RAS} on-chip refresh capability that eliminates the need for external refresh addresses. If \overline{CAS} is held low for the specified set up time (tcsr) before \overline{RAS} goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next \overline{CAS} -before- \overline{RAS} refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the \overline{CAS} active time and cycling \overline{RAS} . The KM44V1004C/CL/CLL hidden refresh cycle is actually a \overline{CAS} -before- \overline{RAS} refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter.

Self Refresh: The self refresh is \overline{CAS} -before- \overline{RAS} refresh to be used for long periods of standby, such as a battery back-up. In normal \overline{CAS} -before- \overline{RAS} condition, when \overline{RAS} is held low above 100 μ s an internal timer activates an refresh operation of consecutive row addresses in DRAM. The self refresh mode is exited when either \overline{RAS} or \overline{CAS} goes high(V_{IH}).

Other Refresh Methods: It is also possible to refresh the KM44V1004C/CL/CLL by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh is the preferred method.

Fast Page Mode with Extended Data Out

Fast page mode provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while \overline{RAS} is kept low to maintain the \overline{CAS} is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

 \overline{CAS} -before- \overline{RAS} Refresh Counter Test Cycle

A special timing sequence using the \overline{CAS} -before- \overline{RAS} counter test cycle provides a convenient method of verifying the functionality of the \overline{CAS} -before- \overline{RAS} refresh activated circuitry.

After the \overline{CAS} -before- \overline{RAS} refresh operation, \overline{CAS} goes high and then low again while \overline{RAS} is held low, the read and write operations are enabled.

This is shown in the \overline{CAS} -before- \overline{RAS} counter test cycle timing diagram. A memory cell be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address — Bits A₀ through A₉ are supplied by the on-chip refresh counter.

Column Address — Bits A₀ through A₉ are supplied by the falling edge of \overline{CAS} as in a normal memory cycle.

Suggested \overline{CAS} -before- \overline{RAS} Counter Test Procedure

The \overline{CAS} -before- \overline{RAS} refresh counter test cycle timing is used in each of the following steps;

1. Initialize the internal refresh counter by performing 8 \overline{CAS} -before- \overline{RAS} cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row address. (The row addresses are supplied by the on-chip refresh counter).
3. Using read-modify-write cycle, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2,3 and 4.

Power-up

If $\overline{RAS}=V_{SS}$ during power-up, the KM44C1004C/CL/CLL could possibly begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is

DEVICE OPERATION (Continued)

recommended that \overline{RAS} and \overline{CAS} track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current. An initial pause of 200 μ sec is required after power-up followed by any 8 initialization cycles before proper device operation is assured. Eight initialization cycles are also required after any 16(L/LL-ver:128, SL-ver:256) msec period in which there are no \overline{RAS} cycles. An initialization cycle is any cycle in which \overline{RAS} is cycled.

Termination

The lines from the TTL driver circuits to the KM44V1004C/CL/CLL inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the KM44V1004C/CL/CLL input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like

transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

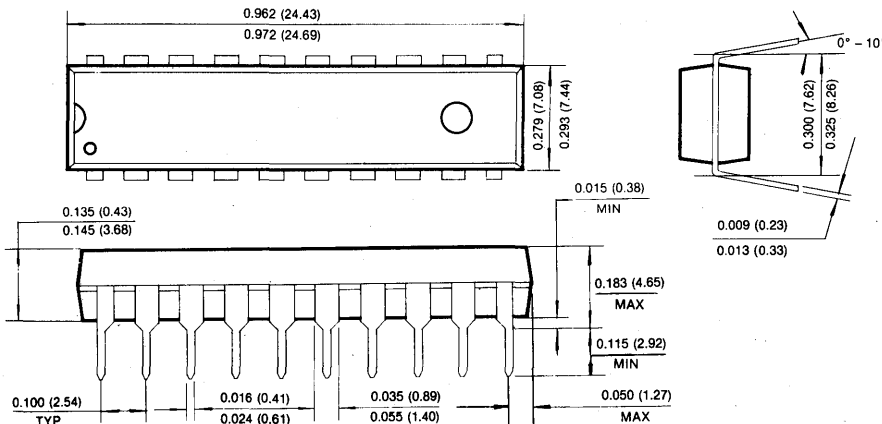
The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity(soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

A high frequency 0.1 μ F ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each KM44V1004C/CL/CLL using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the KM44V1004C/CL/CLL and they supply much of the current used by the KM44V1004C/CL/CLL during cycling.

In addition, a large tantalum capacitor with a value of 47 μ F to 100 μ F should be used for bulk decoupling to recharge the 0.1 μ F capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS
20-LEAD PLASTIC DUAL IN-LINE PACKAGE

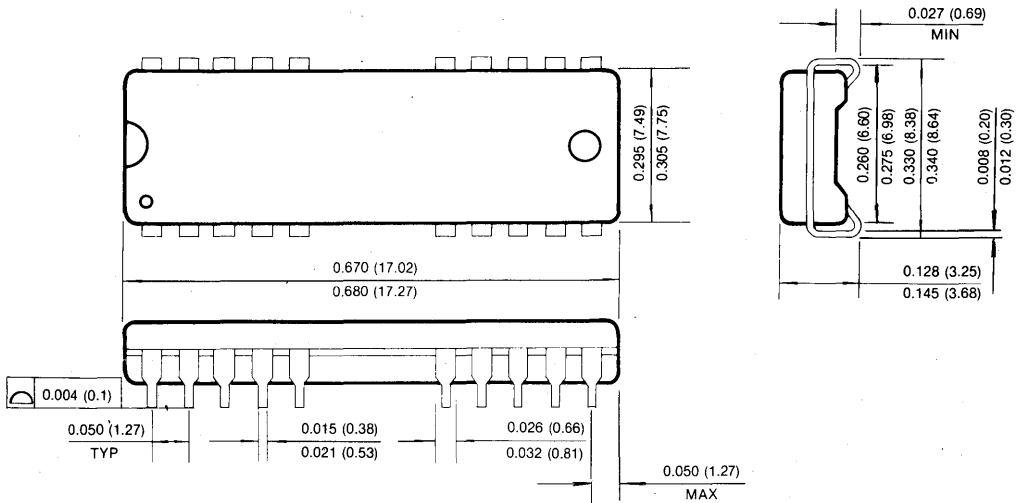
Units: Inches (Millimeters)



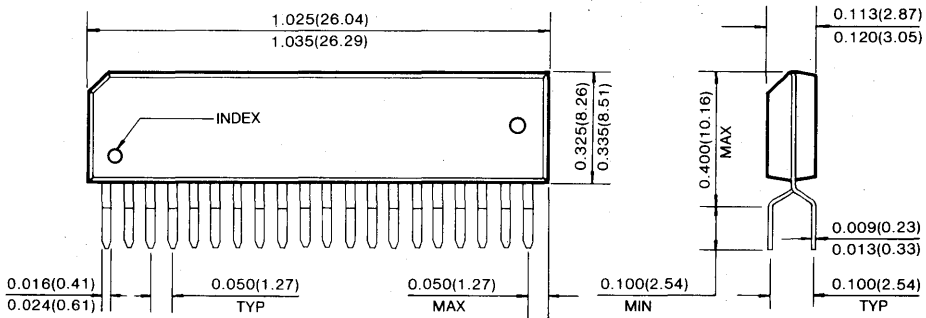
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE

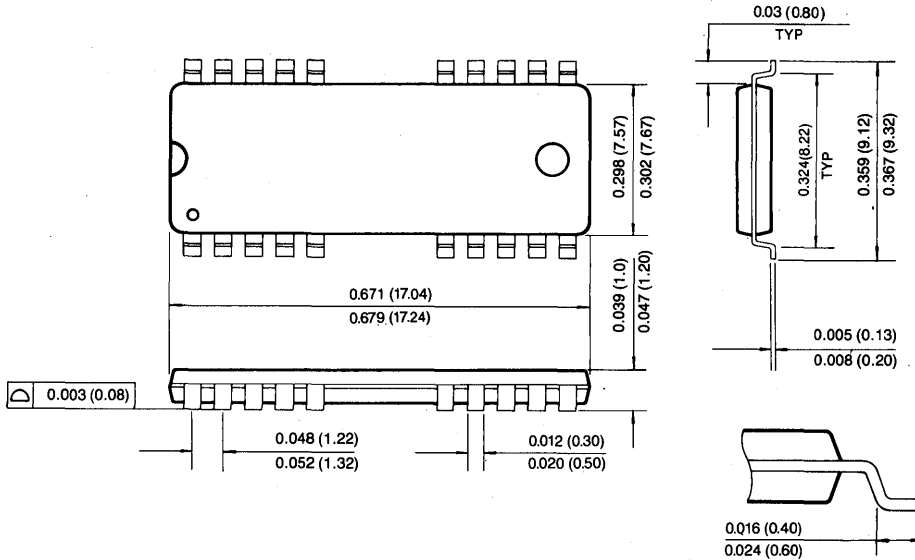


3

PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

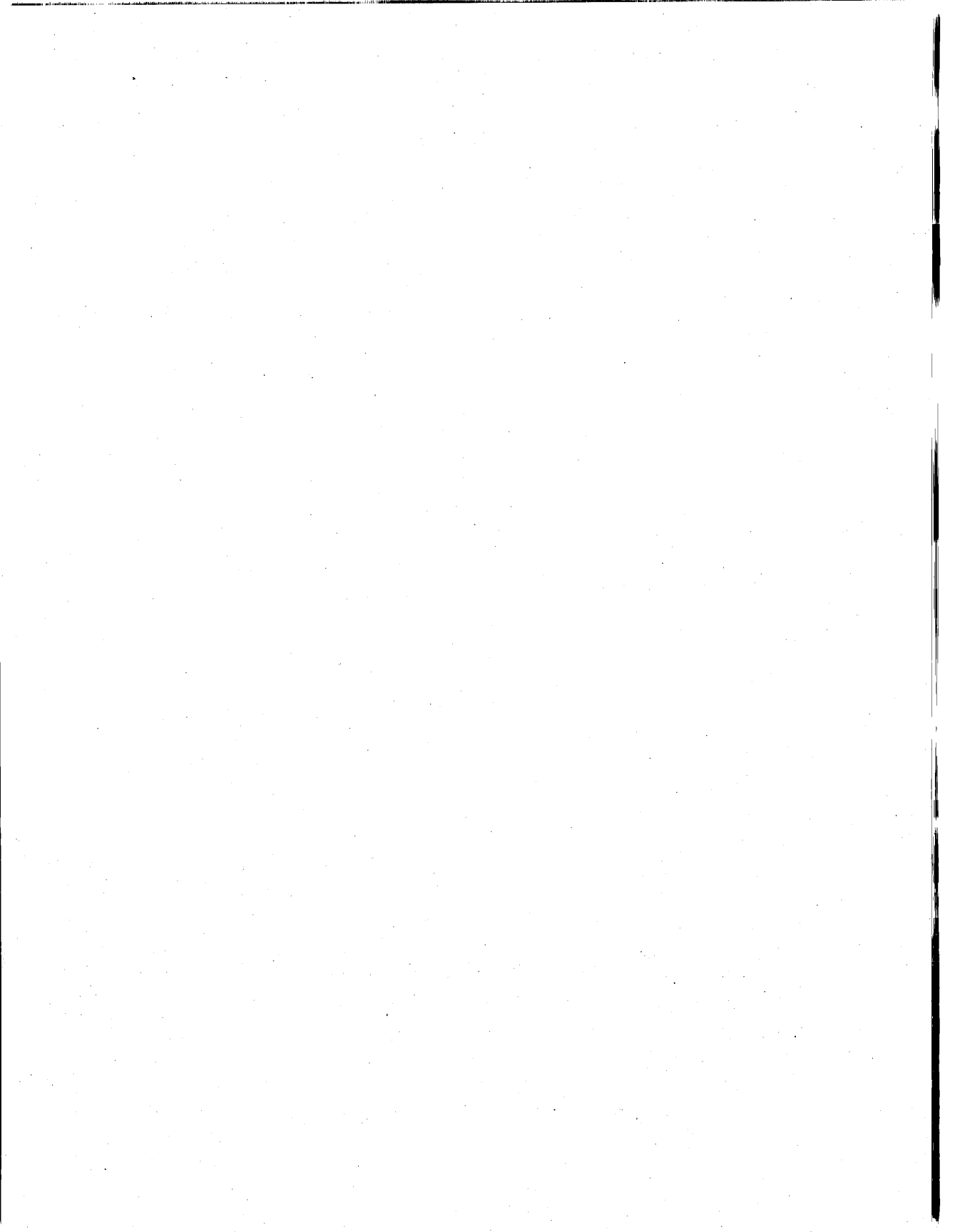
Units: Inches (millimeters)





4M B/W DRAM DATA SHEET 4

- 16. KM416C256B/BL/BLL
- 17. KM416C254B/BL/BLL
- 18. KM416C156B/BL/BLL
- 19. KM416C157B/BL/BLL
- 20. KM418C256B/BL/BLL
- 21. KM48V512B/BL/BLL
- 22. KM48V514B/BL/BLL
- 23. KM416V256B/BL/BLL
- 24. KM416V254B/BL/BLL



512K × 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	t _{TRAC}	t _{CAC}	t _{RC}
KM48C512B/BL/BLL-5	50ns	15ns	90ns
KM48C512B/BL/BLL-6	60ns	15ns	110ns
KM48C512B/BL/BLL-7	70ns	20ns	130ns
KM48C512B/BL/BLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refresh operation (LL-version)
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Dual +5.0V ± 10% power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/128ms (LL-version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.83mW (LL-version)
 - Active (50/60/70/80): 470/385/360/330mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

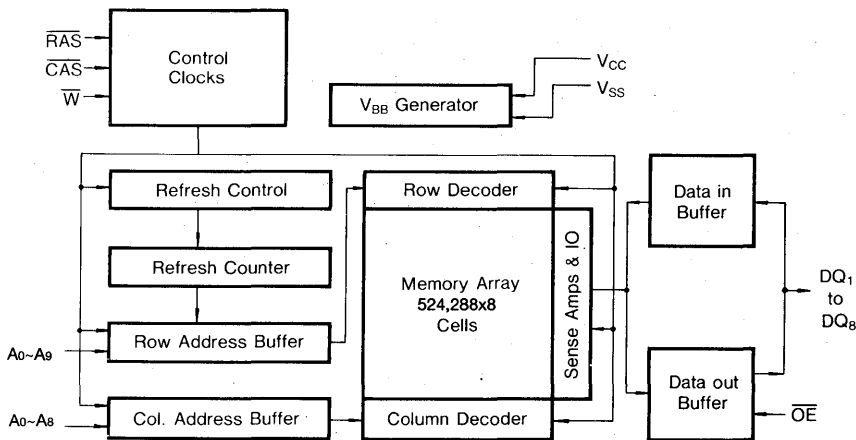
GENERAL DESCRIPTION

The Samsung KM48C512B/BL/BLL is a CMOS high speed 524,288 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C512B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

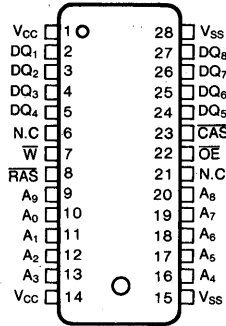
The KM48C512B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



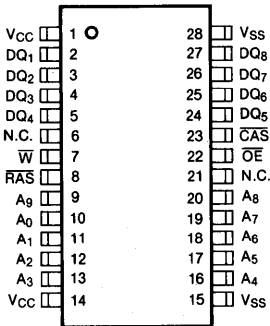
PIN CONFIGURATION (Top Views)

• KM48C512BJ/BLJ/BLLJ



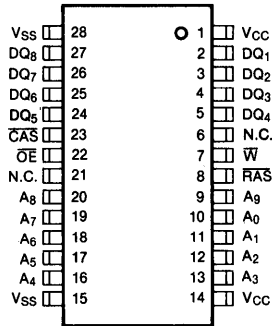
(SOJ)

• KM48C512BT/BLT/BLLT



(TSOP (II)-Forward Type)

• KM48C512BTR/BLTR/BLLTR



(TSOP (II)-Reverse Type)

Pin Name	Pin Function
A ₀ -A ₉	Address Input
DQ ₁₋₈	Data In/Out
V _{SS}	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe

Pin Name	Pin Function
W	Read/Write Input
OE	Data Output Enable
V _{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{os}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	Vcc + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

4

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} , \overline{CAS} , Address Cycling @ t _{RC} =min.)	I _{cc1}	-	85	mA
			70	mA
			65	mA
			60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	I _{cc2}	-	2	mA
			85	mA
			70	mA
			65	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @ t _{RC} =min.)	I _{cc3}	-	85	mA
			70	mA
			65	mA
			60	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @ t _{PC} =min.)	I _{cc4}	-	65	mA
			55	mA
			50	mA
			45	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{cc}-0.2V$)	I _{cc5}	-	1	mA
			200	μA
			150	μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @ t _{RC} =min.)	I _{cc6}	-	85	mA
			70	mA
			65	mA
			60	mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V \overline{CAS} =0.2V DIN=Don't Care, TRC=125 μ S TRAS=TRAS min. ~300ns	lcc7	-	300	μ A
Self Refresh Current \overline{RAS} = \overline{CAS} =0.2V W= \overline{OE} =A ₀ -A ₉ =V _{CC} -0.2V or 0.2V DQ1-DQ ₈ =V _{CC} -0.2V, 0.2V or Open	lccs	-	200	μ A
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{CC} +0.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μ A
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μ A
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while \overline{RAS} =V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₉)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , W, \overline{OE})	C _{IN2}	-	7	pF
Output Capacitance (DQ1~DQ ₈)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_a ≤ 70°C, V_{CC}=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	135		155		185		205		ns	
Access time from \overline{RAS}	trac		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		15		15		20		20	ns	3,4,5
Access time from column address	taa		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tclz	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	trp	30		40		50		60		ns	
\overline{RAS} pulse width	tras	50	10,000	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	trsh	15		15		20		20		ns	
\overline{CAS} hold time	tcsh	50		60		70		80		ns	
\overline{CAS} pulse width	tcas	15	10,000	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	trcd	20	35	20	45	20	50	20	60	ns	4

(*) 50ns Product: V_{CC}=5V ± 5%, C_{out}=50pF



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		0		ns	8
Write command hold time	tWCH	10		10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		50		55		ns	6
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		15		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	10
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128		128	ms	
Refresh period (LL-version)	tREF		128		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	75		85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	50		55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{F}}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tRMC	80		80		95		100		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page Mode)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	

(*) 50ns Product:Vcc=5V ± 5%, Cout=50pF



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ precharge time (Fast Page Mode)	tCP	10		10		10		10		ns	
access time from $\overline{\text{OE}}$	tOEA		15		15		20		20	ns	
$\overline{\text{OE}}$ to data-in delay time	tOED	15		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	15		15		20		20		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C-B-R}}$ self refresh)	tRASS	100		100		100		100		μs	12
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C-B-R}}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{\text{CAS}}$ hold time ($\overline{\text{C-B-R}}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

(*) 50ns Product:Vcc=5V \pm 5%, Cout=50pF

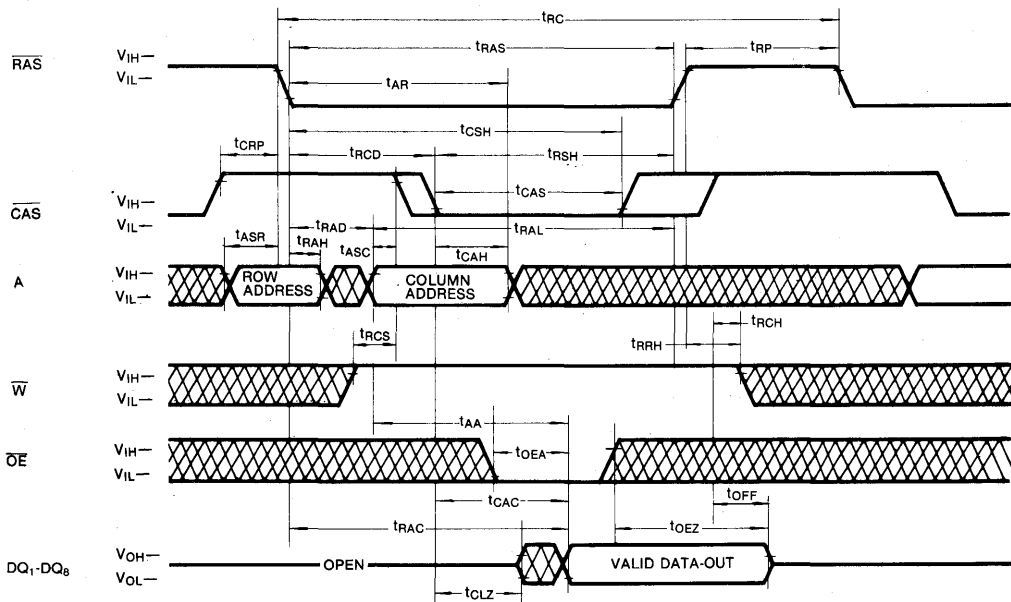
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}}(\text{max})$.
7. $t_{\text{OFF}(\text{max})}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification. (LL-version)

4

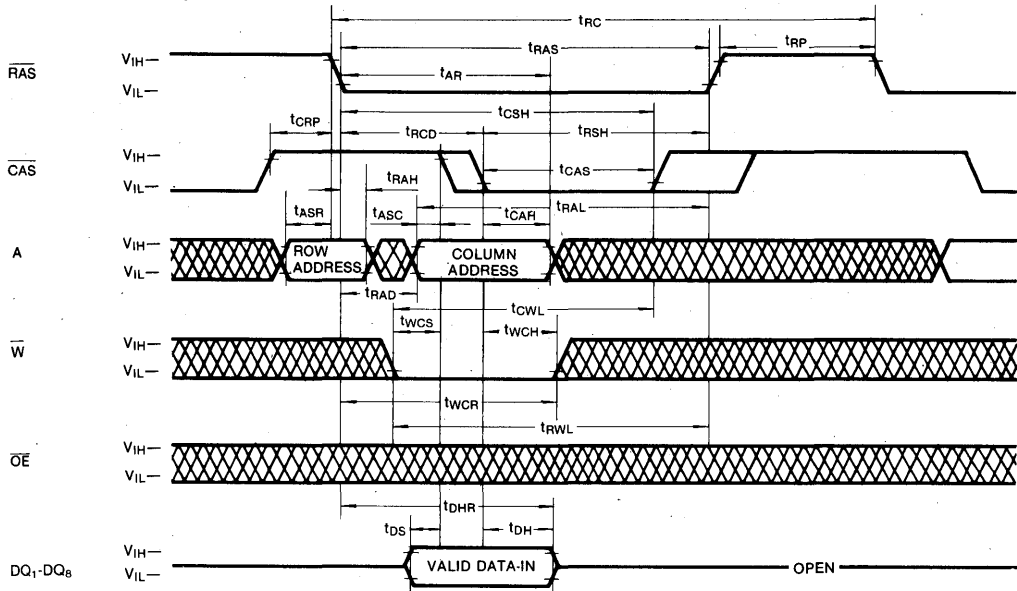
TIMING DIAGRAMS

READ CYCLE

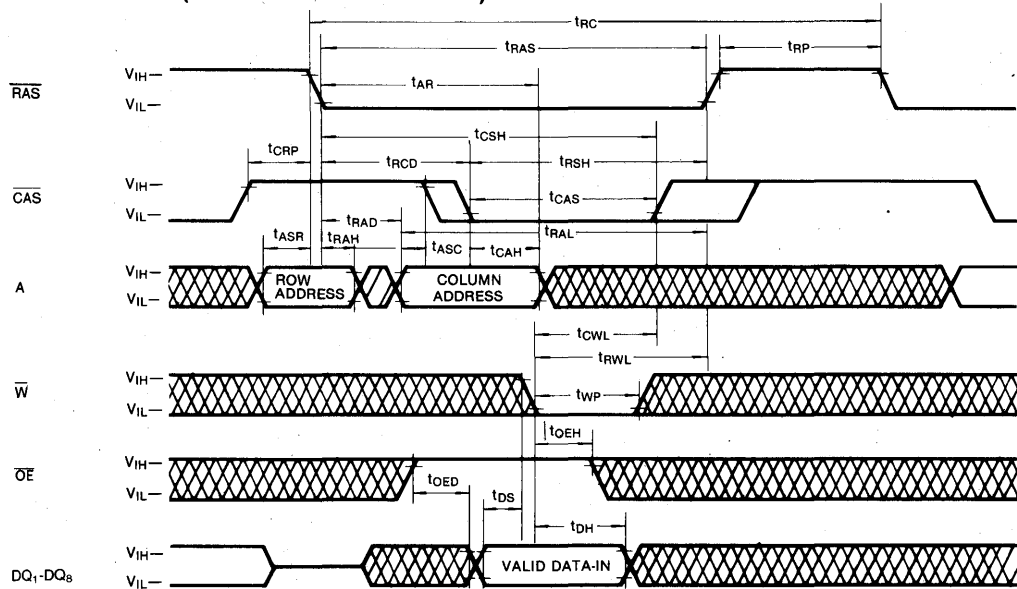


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



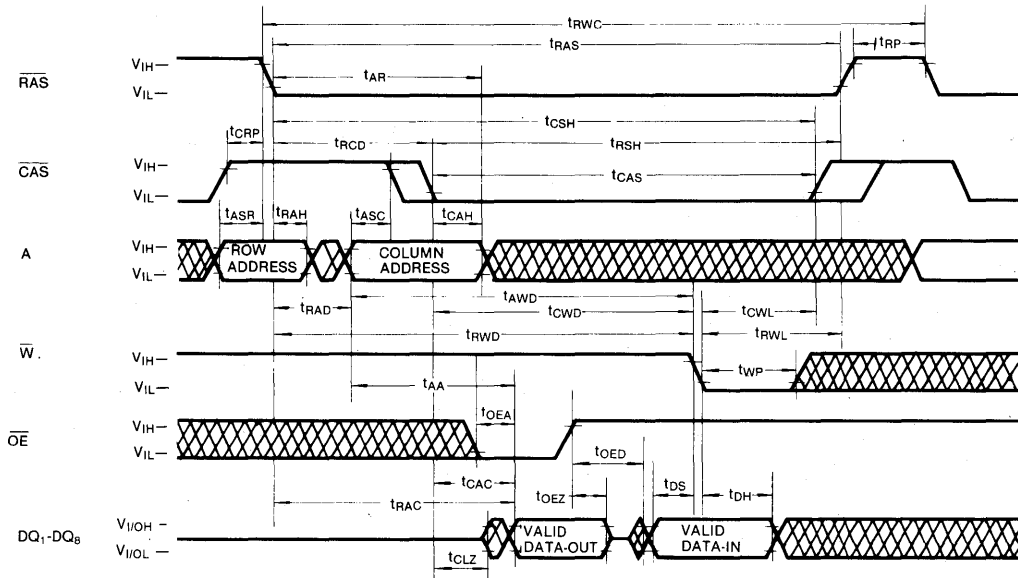
WRITE CYCLE (OE CONTROLLED WRITE)



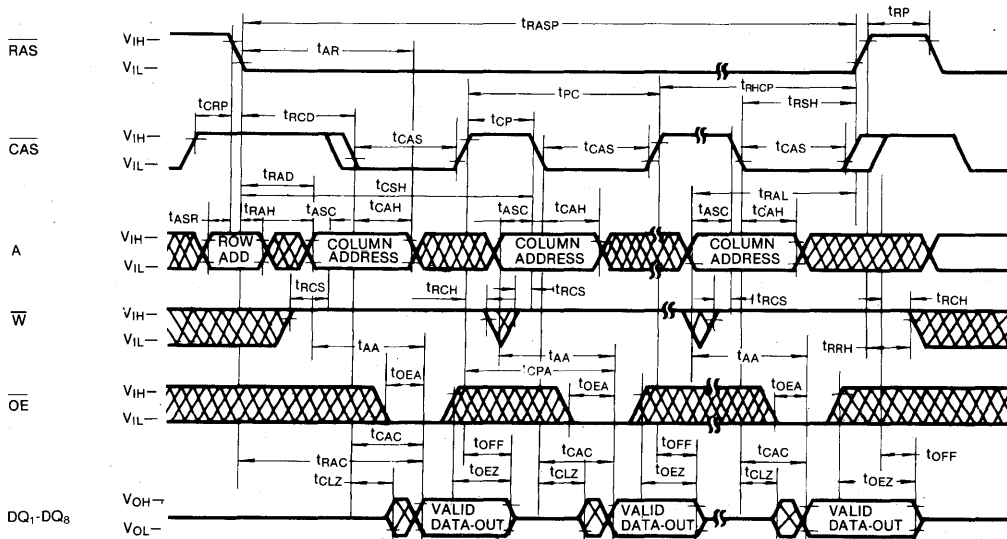
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

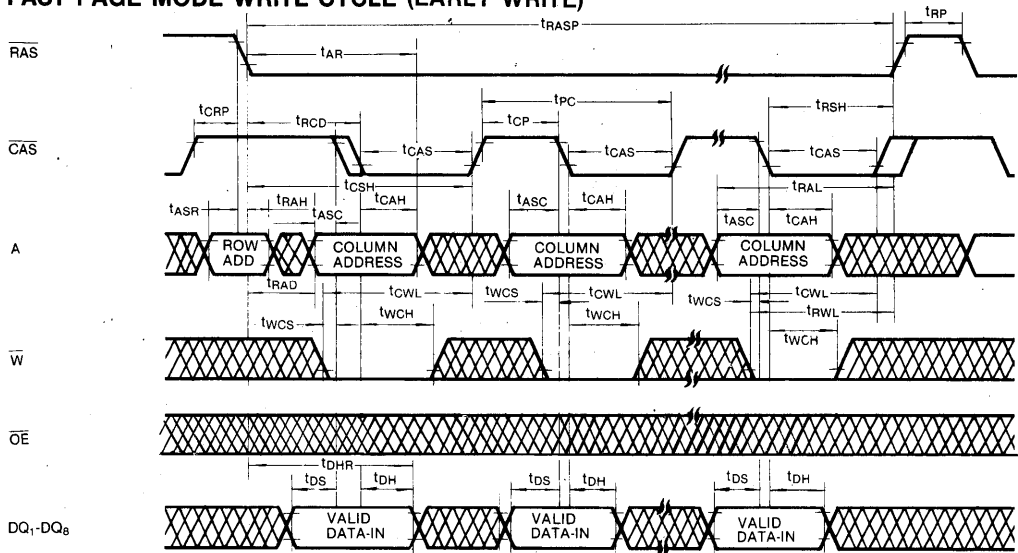


DON'T CARE

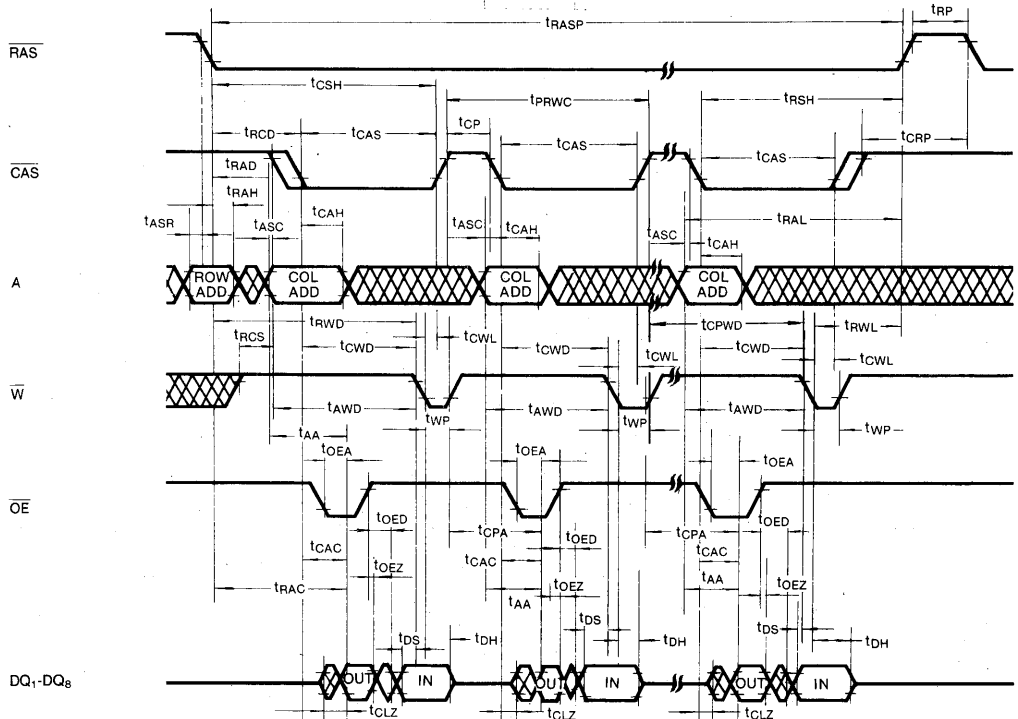
4

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

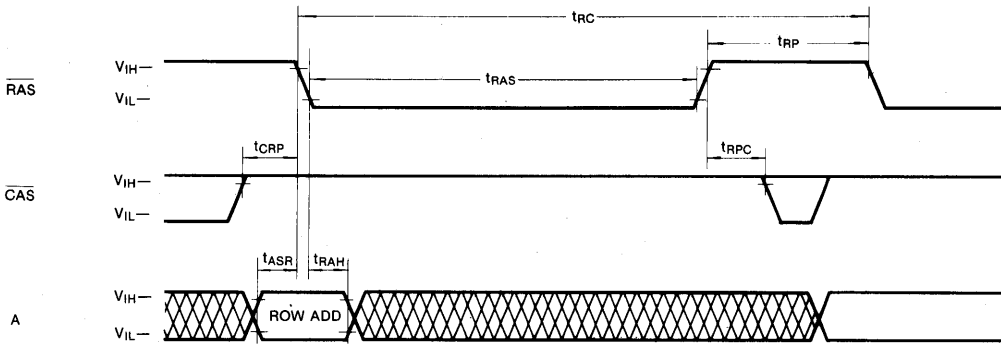


DON'T CARE

TIMING DIAGRAMS (Continued)

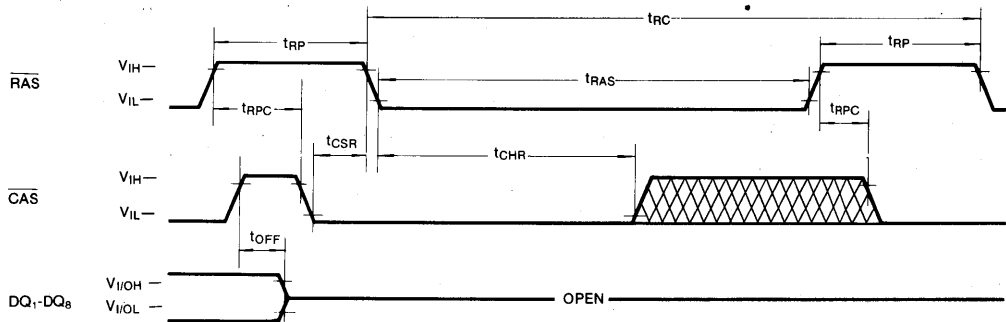
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



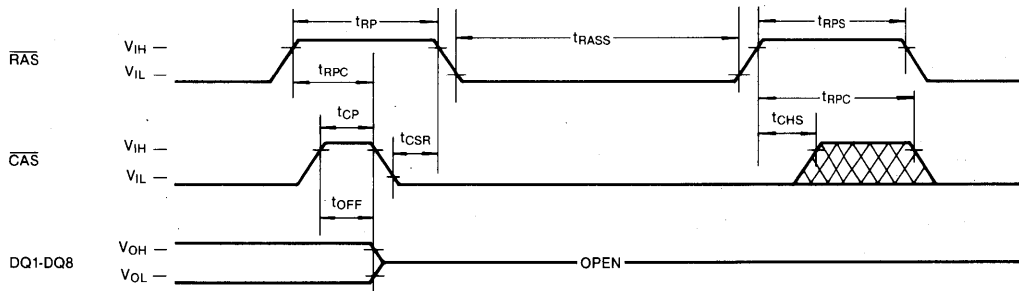
CAS-BEFORE-RAS REFRESH CYCLE


NOTE: \bar{W} , \bar{OE} , \bar{A} = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

NOTE: \bar{W} , \bar{OE} , \bar{A} = Don't Care

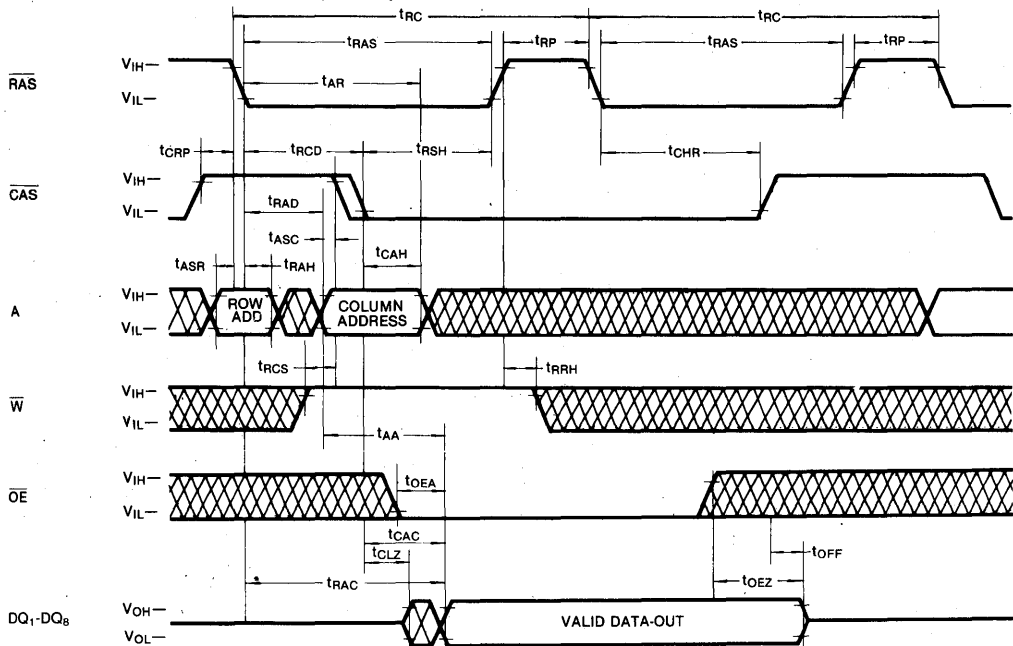


 DON'T CARE

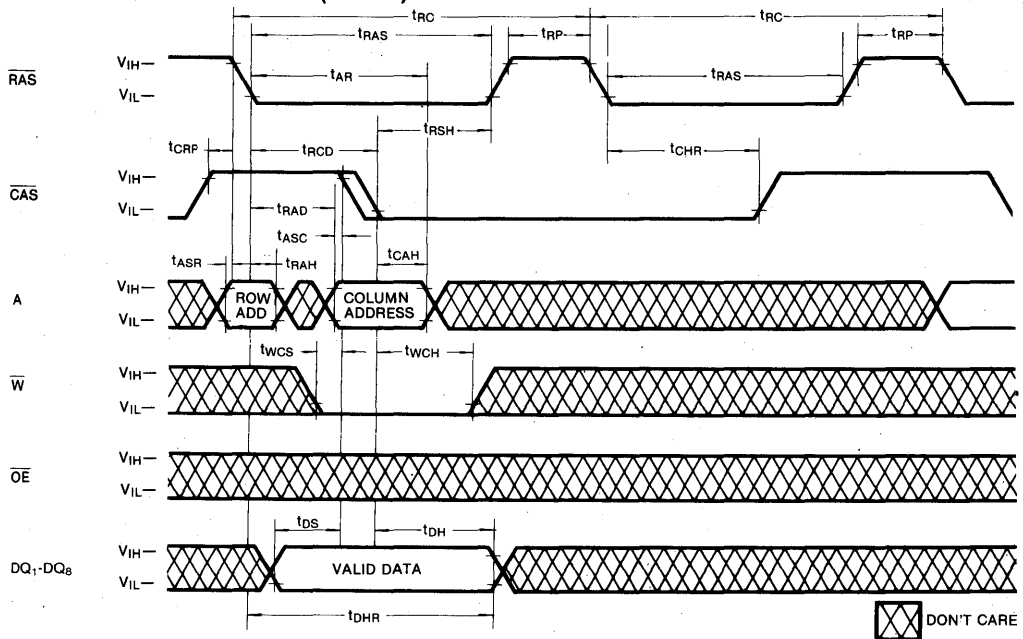
4

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

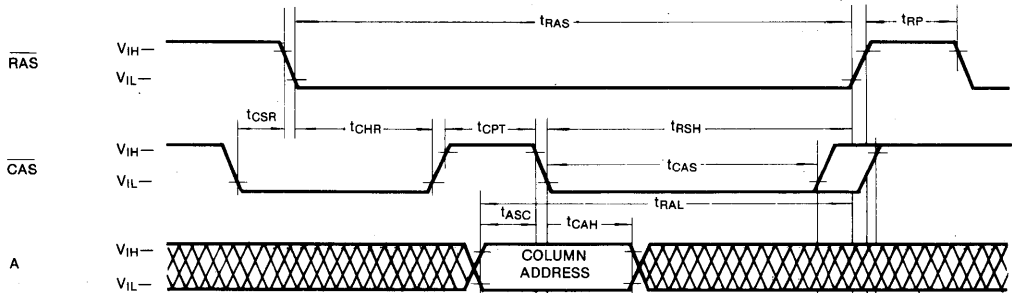


HIDDEN REFRESH CYCLE (WRITE)

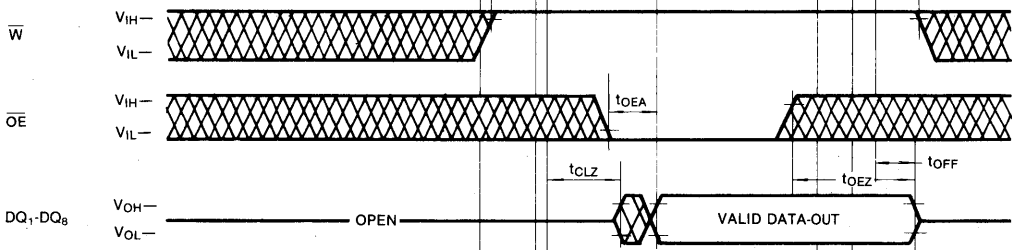


TIMING DIAGRAMS (Continued)

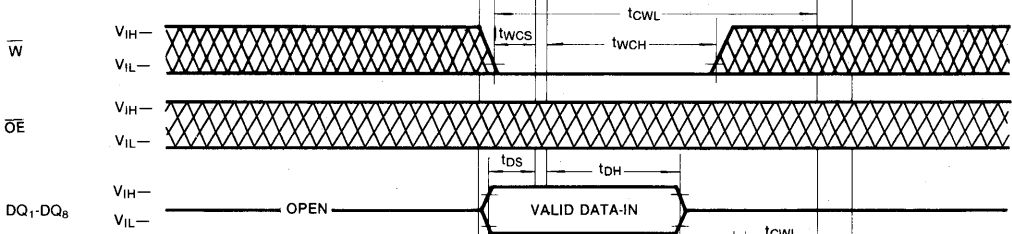
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



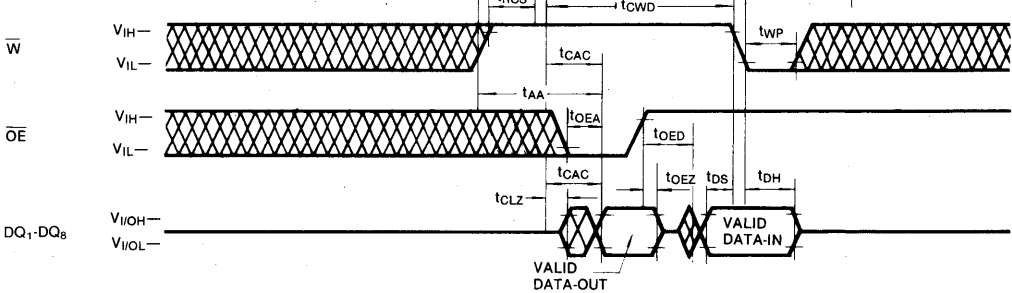
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



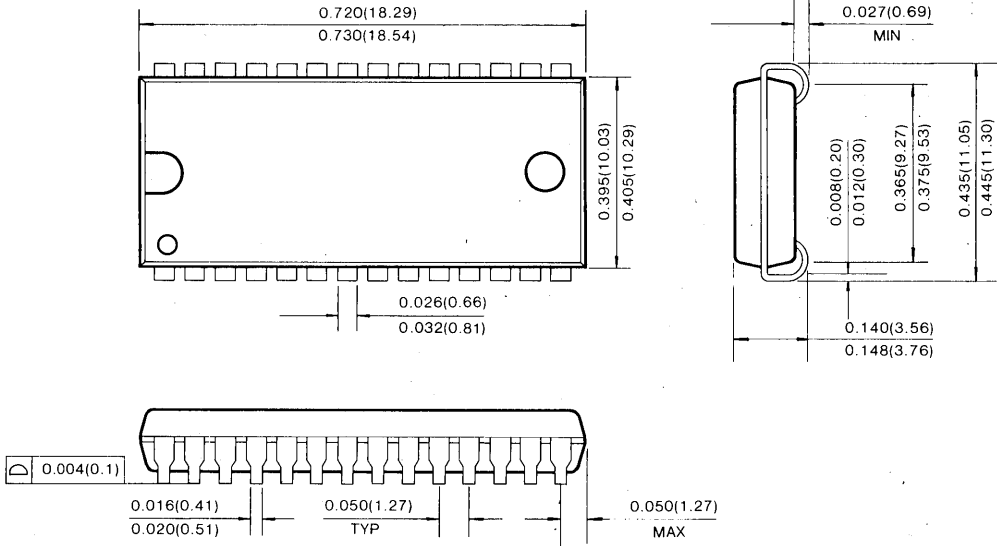
DON'T CARE

4

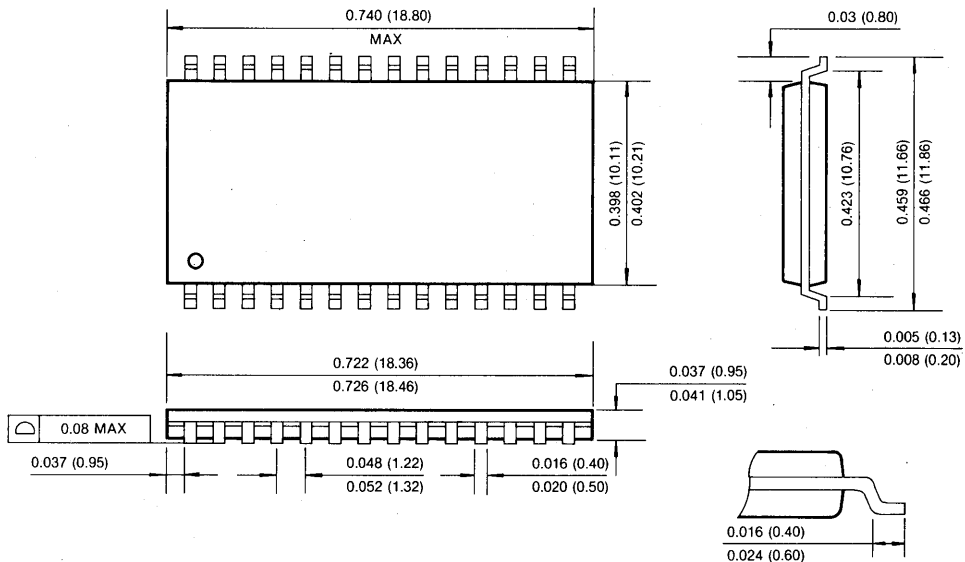
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



512K × 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trC	tHPC
KM48C514B/BL/BLL-5	50ns	17ns	90ns	20ns
KM48C514B/BL/BLL-6	60ns	17ns	110ns	24ns
KM48C514B/BL/BLL-7	70ns	20ns	130ns	29ns

- Fast Page Mode with Extended Data Out
- Self Refresh operation (LL-ver)
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Byte Read/Write Operation
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Dual +5V ± 10% power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L/LL-ver)
- Power Dissipation
 - Standby: 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.83mW (LL-version)
 - Active (50/60/70): 470/385/360mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

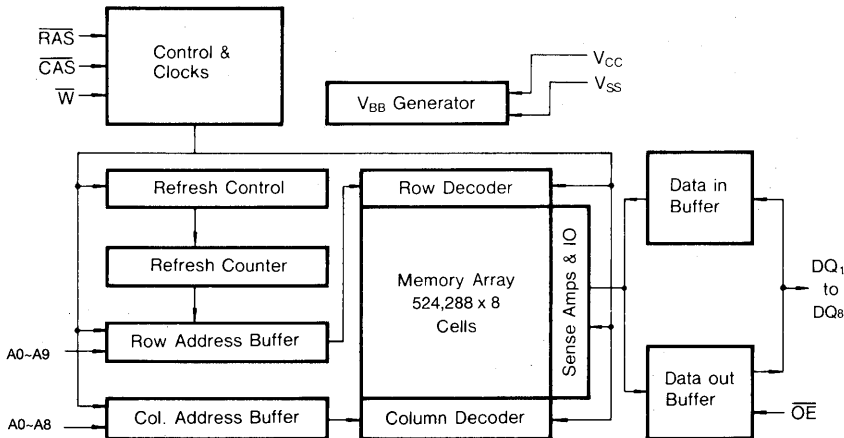
GENERAL DESCRIPTION

The Samsung KM48C514B/BL/BLL is a CMOS high speed 524,288 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48C514B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

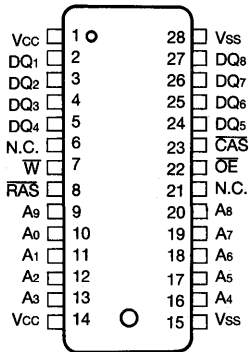
The KM48C514B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



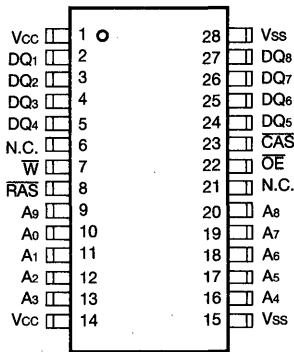
PIN CONFIGURATION (Top Views)

• KM48C514BJ/BLJ/BLLJ



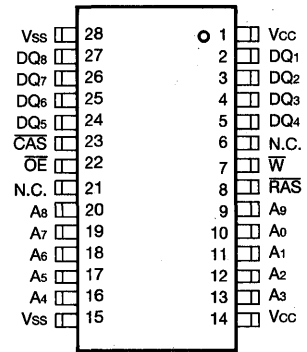
(SOJ)

• KM48C514BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM48C514BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-8	Data In/Out
Vss	Ground
\bar{RAS}	Row Address Strobe
\bar{CAS}	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
Vcc	Power(+5 V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to 7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1 to 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	W

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} , \overline{CAS} , Address Cycling @ $t_{RC}=\text{min.}$)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7 I _{CC1}	-	85 70 65	mA mA mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	I _{CC2}	-	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @ $t_{RC}=\text{min.}$)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7 I _{CC3}	-	85 70 65	mA mA mA
EDO Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @ $t_{PC}=\text{min.}$)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7 I _{CC4}	-	65 55 50	mA mA mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)	KM48C514B KM48C514BL KM48C514BLL I _{CC5}	-	1 200 150	mA μA μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @ $t_{RC}=\text{min.}$)	KM48C514B/BL/BLL-5 KM48C514B/BL/BLL-6 KM48C514B/BL/BLL-7 I _{CC6}	-	85 70 65	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CAS=0.2V DIN=Don't Care, TRC=125 μ S TRAS=TRAS min.~300ns	KM48C514BL I _{CC7}	-	300	μA
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A9=VCC-0.2V or 0.2V DQ1-DQ8=VCC-0.2V, 0.2V or Open	KM48C514BLL I _{CC8}	-	200	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.5V$, all other pins not under test = 0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} = -5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} = 4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A = 25°C, V_{CC} = 5V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₉)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , W, \overline{OE})	C _{IN2}	-	7	pF
Input Capacitance (DQ ₁ ~DQ ₈)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5V ± 10%, See notes 1,2)

Test condition: V_{ih}/V_{il} = 2.4/0.8V, V_{oh}/V_{ol} = 2.0/0.8V, Output loading C_L = 100pF

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		ns	
Read-modify-write cycle time	t _{RWC}	135		155		185		ns	
Access time from \overline{RAS}	t _{RAC}		50		60		70	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		17		17		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	3		3		3		ns	3
Turn-off delay from \overline{CAS}	t _{CEZ}	3	13	3	15	3	20	ns	7,14
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	t _{RP}	30		40		50		ns	
\overline{RAS} pulse width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
\overline{RAS} hold time	t _{RSH}	17		17		20		ns	
\overline{CAS} hold time	t _{CSH}	40		50		60		ns	
\overline{CAS} pulse width	t _{CAS}	8	10,000	10	10,000	15	10,000	ns	12
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	37	20	45	20	50	ns	4
\overline{RAS} to column address delay time	t _{RAD}	15	25	15	30	15	35	ns	11
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	

(*) -50ns Product : Output Loading (C_L) = 50pF, V_{CC} = 5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		50		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		15		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		10		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh Period(LL-version)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		42		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		95		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		60		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	53		60		65		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40	ns	3
Hyper Page mode cycle time	tHPC	20		24		29		ns	12
Hyper Page mode read-modify-write cycle time	tHPMC	62		71		81		ns	12
$\overline{\text{CAS}}$ precharge time (Hyper Page mode)	tCP	8		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page mode)	tRASP	50	100K	60	100K	70	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		ns	
$\overline{\text{OE}}$ access time	tOEA		15		15		20	ns	
$\overline{\text{OE}}$ to data dela	tOED	13		15		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	3	13	3	15	3	20	ns	7
$\overline{\text{OE}}$ to output in Low-Z	tOLZ	3		3		3		ns	3

(*) -50ns Product : Output Loading (CL)=50pF, Vcc=5V ± 5%



4

AC CHARACTERISTICS (Continued)

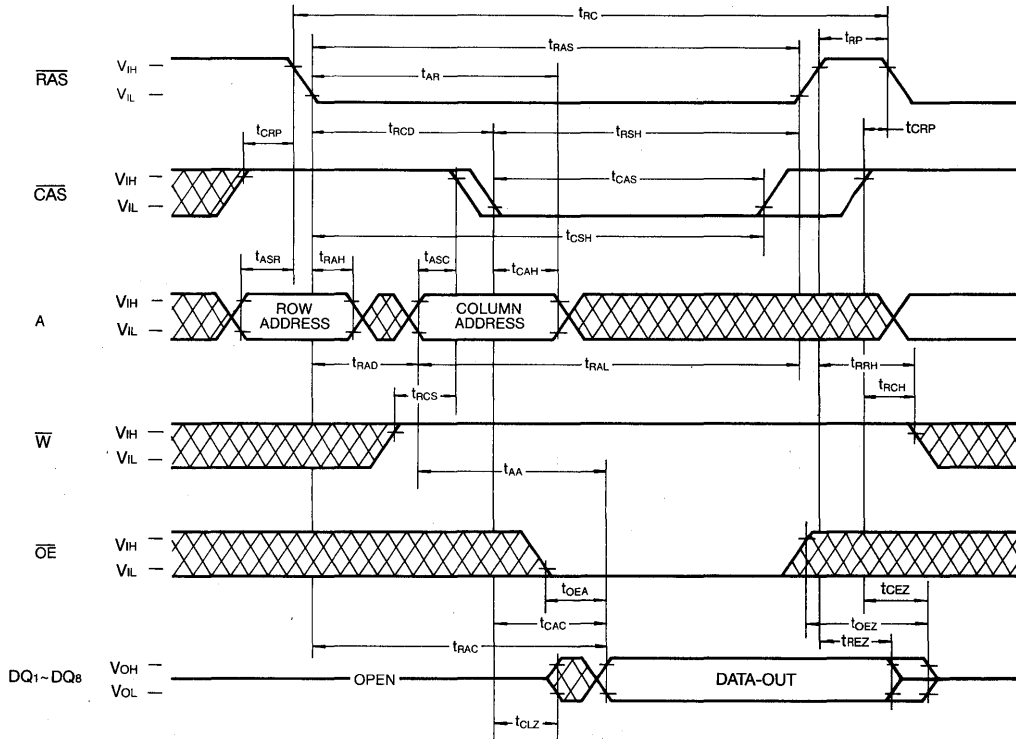
Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} commend hold time	toEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	treZ	3	13	3	15	3	20	ns	7,14
Output buffer turn off delay from \overline{W}	tweZ	3	13	3	15	3	20	ns	7
\overline{W} to data delay	twED	13		15		20		ns	
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		ns	
\overline{W} pulse width(Hyper page Cycle)	twPE	5		5		5		ns	
\overline{RAS} pulse width(LL-ver)	trASS	100		100		100		μ s	13
\overline{RAS} precharge time (LL-ver)	trPS	90		110		130		ns	13
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		ns	13

(*) -50ns Product : Output Loading (CL)=50pF, Vcc=5V \pm 5%

NOTES

- An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs except t_{HPC} and t_{HPRWC}.
- Measured with a load equivalent to 2 TTL loads and 100pF
- Operation within the tr_{CD}(max) limit insures that tr_{AC}(max) can be met. tr_{CD}(max) is specified as a reference point only. If tr_{CD} is greater than the specified tr_{CD}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that tr_{CD} \geq tr_{CD} (max).
- t_{AR}, t_{WCR}, t_{DHR} are referenced to tr_{AD}(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCS}, tr_{WD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If t_{WCS} \geq t_{WCS}(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{CWD} \geq t_{CWD}(min), tr_{WD} \geq tr_{WD}(min) and t_{AWD} \geq t_{AWD}(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either tr_{CH} or tr_{RH} must be satisfied for a read cycle.
- These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
- Operation within the tr_{AD}(max) limit insures that tr_{AC}(max) can be met. tr_{AD}(max) is specified as a reference point only. If tr_{AD} is greater than the specified tr_{AD}(max) limit, then access time is controlled by t_{AA}.
- t_{ASC} \geq t_{CPmin}, Assume t_T=2.0 ns
- 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (LL-ver)
- If \overline{RAS} goes high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going, If \overline{CAS} goes high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going

TIMING DIAGRAMS
READ CYCLE

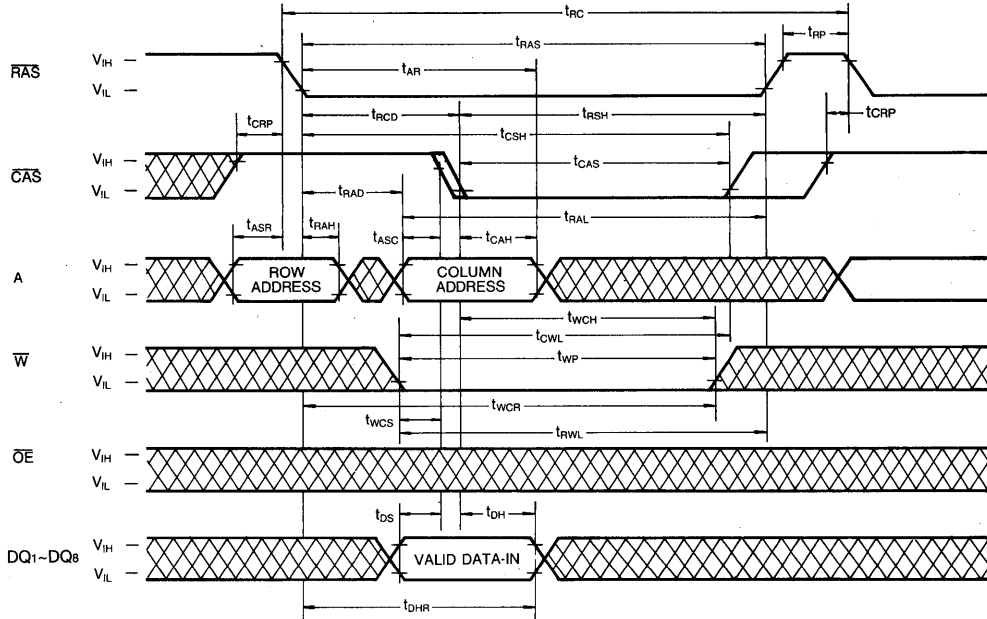


 Don't Care

4

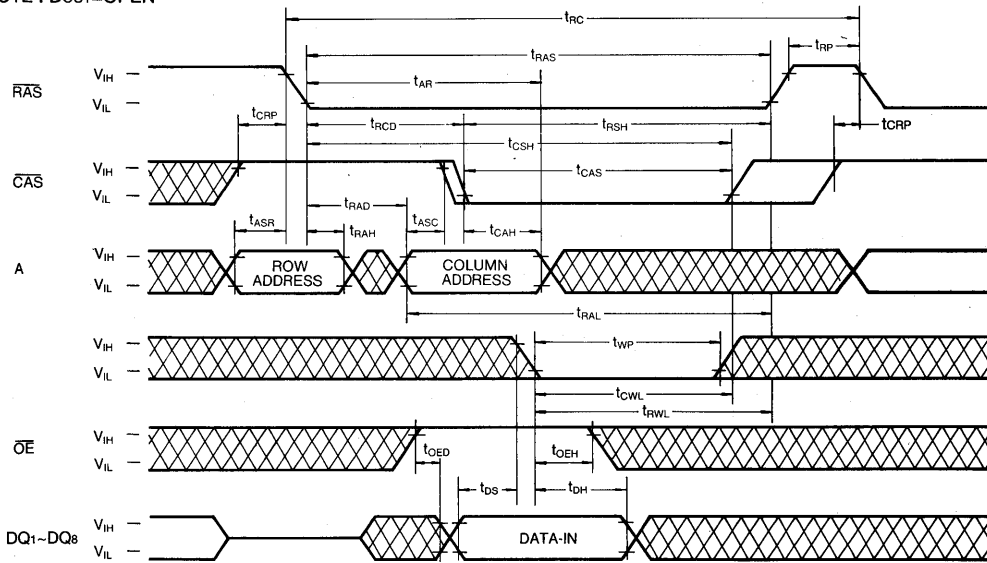
WRITE CYCLE (EARLY CYCLE)

NOTE : DOUT=OPEN



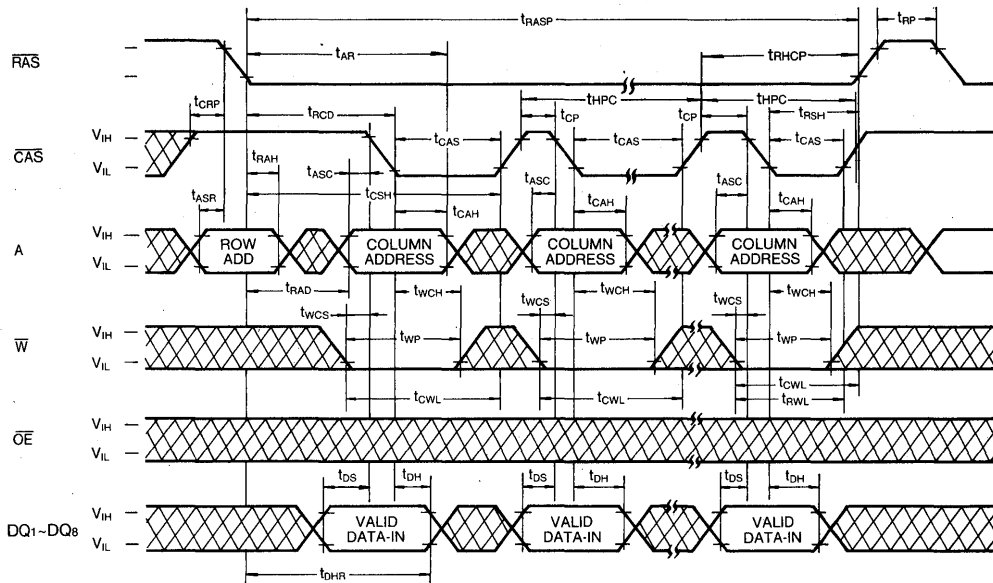
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT=OPEN

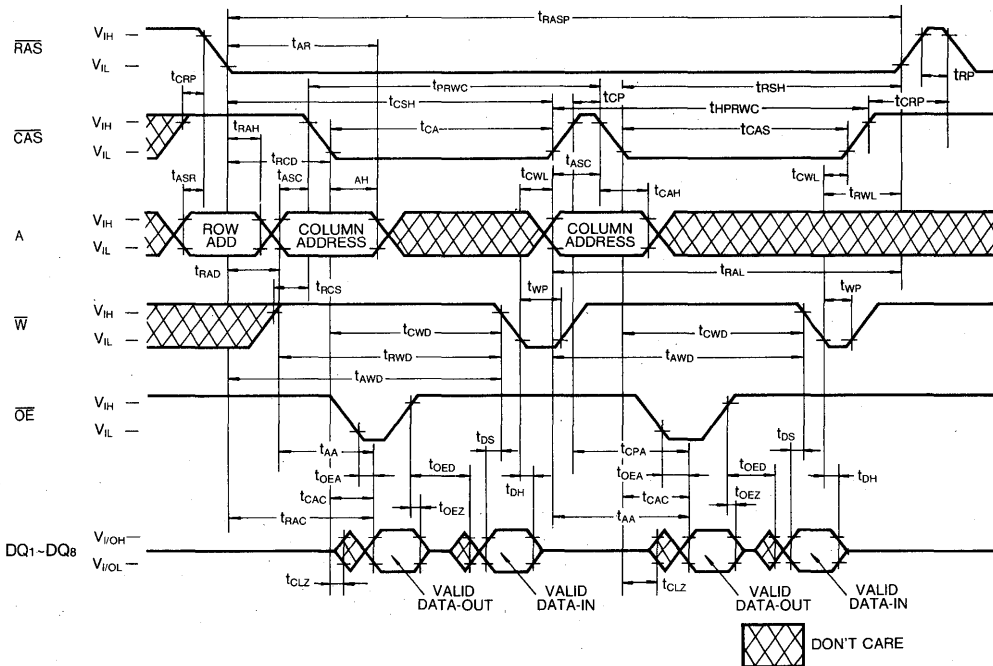


 Don't Care

HYPER PAGE WRITE CYCLE (EARLY WRITE)

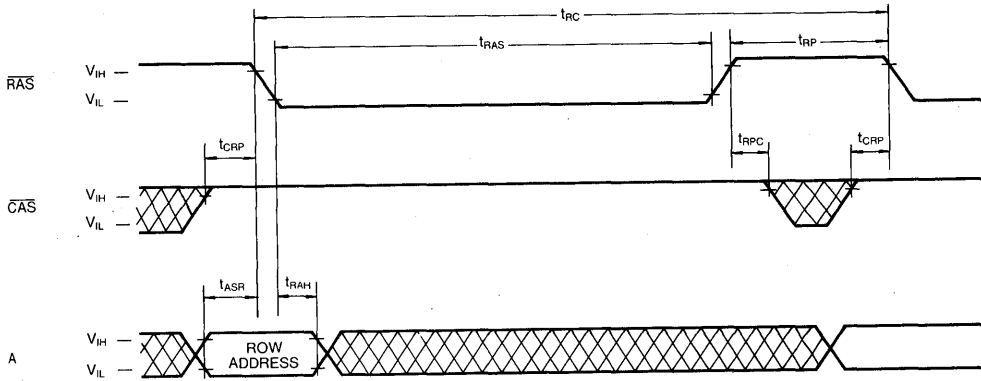


HYPER PAGE READ-MODIFY-WRITE CYCLE



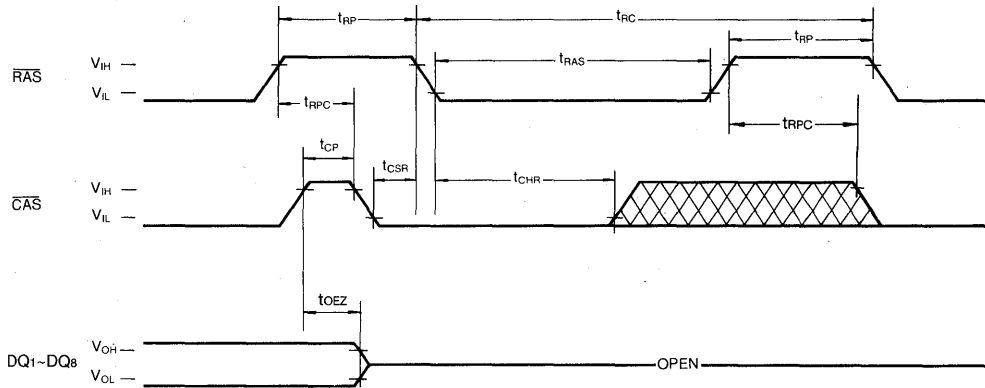
RAS-ONLY REFRESH CYCLE

NOTE : \overline{W} , \overline{OE} , DIN=Don't Care
Dout=Open



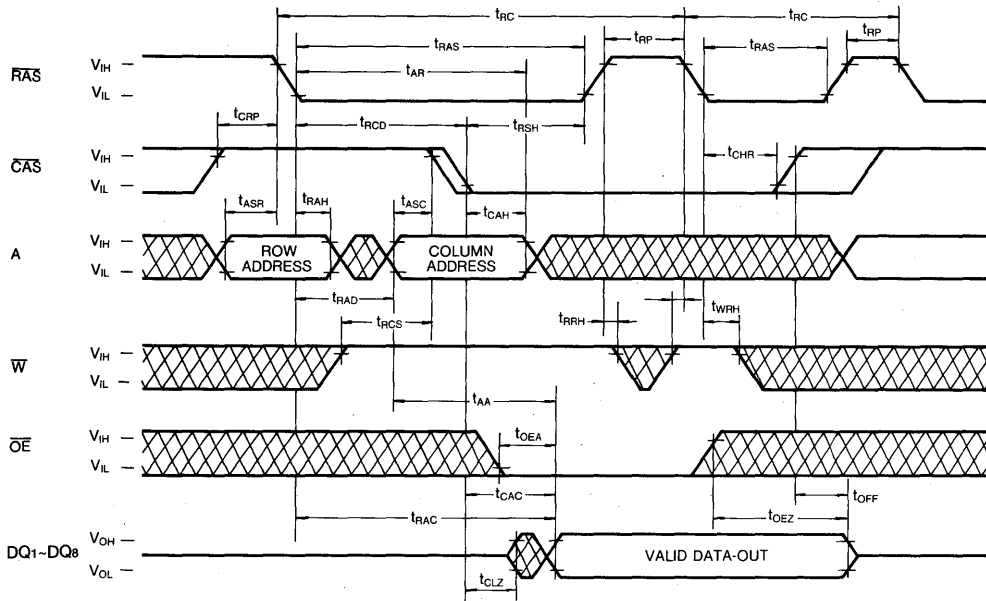
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \overline{W} , \overline{OE} , A=Don't Care

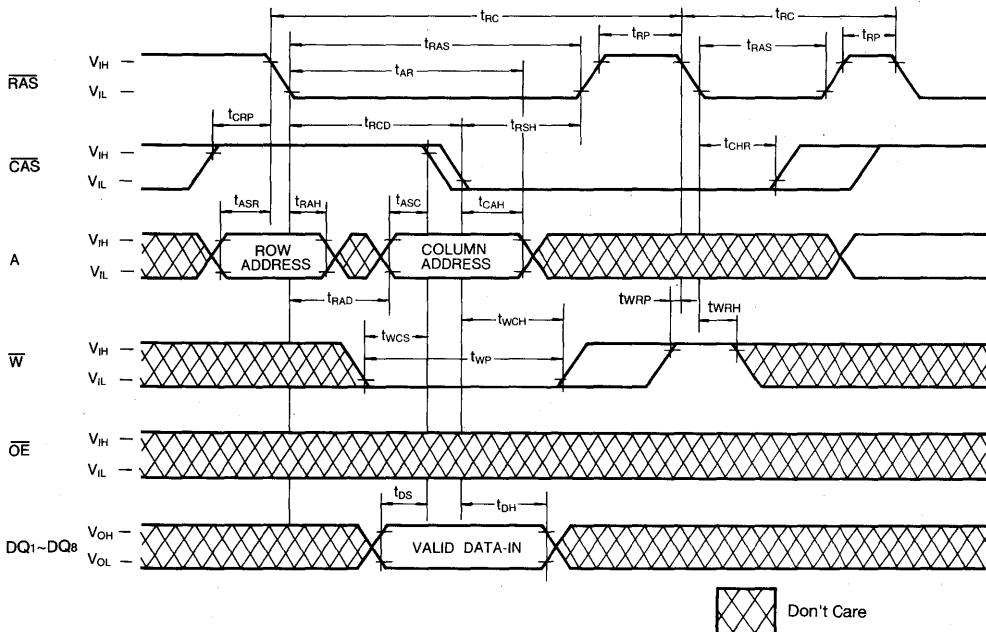


 Don't Care

HIDDEN REFRESH CYCLE (READ)

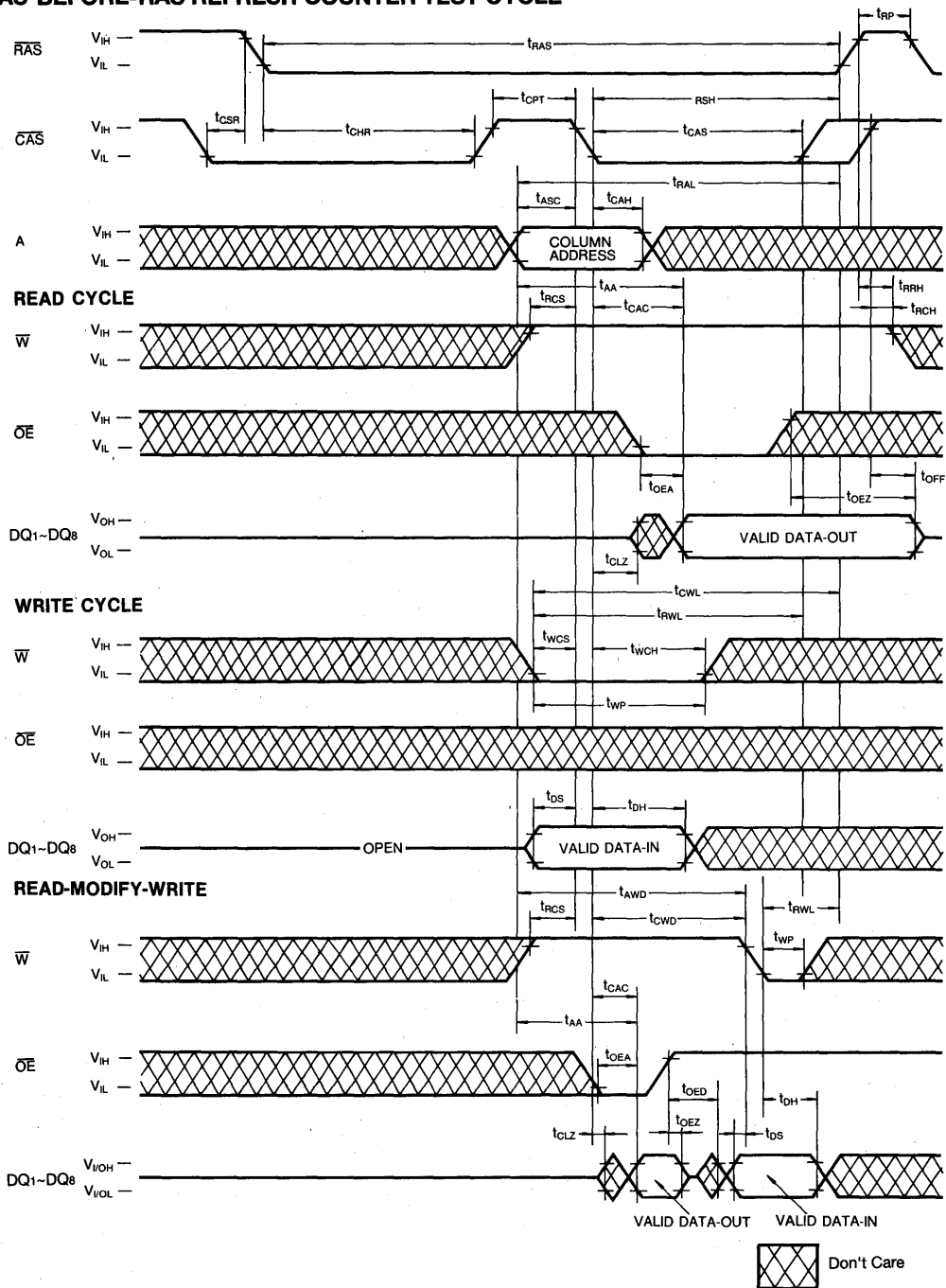


HIDDEN REFRESH CYCLE (WRITE)



4

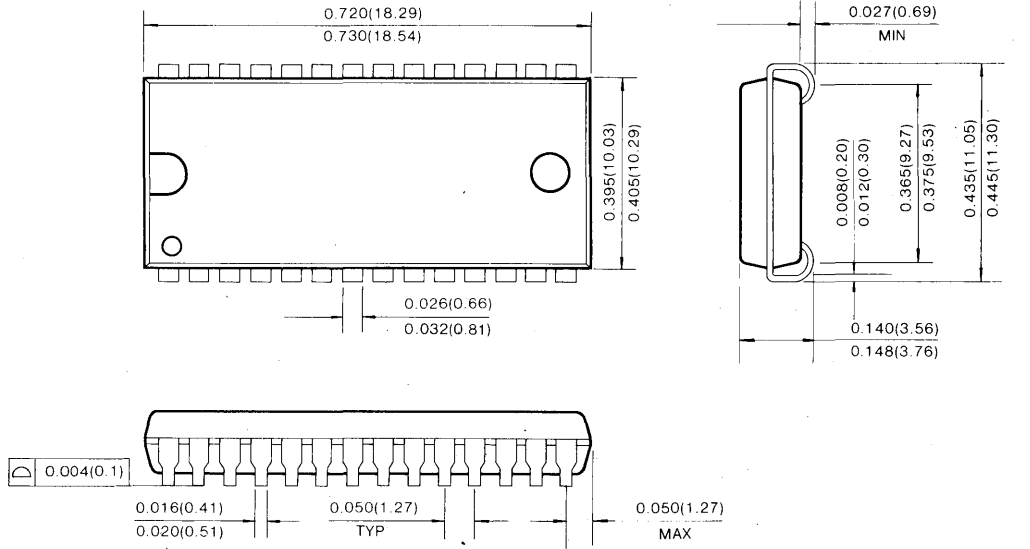
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



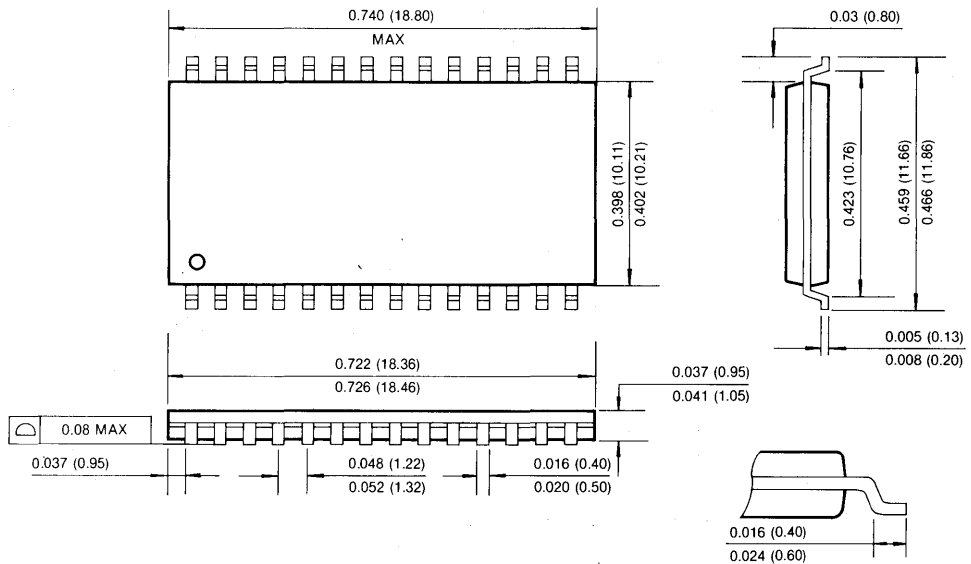
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



512K × 9 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	trAC	tcAC	trC
KM49C512B/BL/BLL-6	60ns	15ns	110ns
KM49C512B/BL/BLL-7	70ns	20ns	130ns
KM49C512B/BL/BLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refresh operation (LL-version)
- Byte Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Dual +5.0V ± 10% power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/128ms (LL-version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.83mW (LL-version)
 - Active (60/70/80): 415/385/360mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

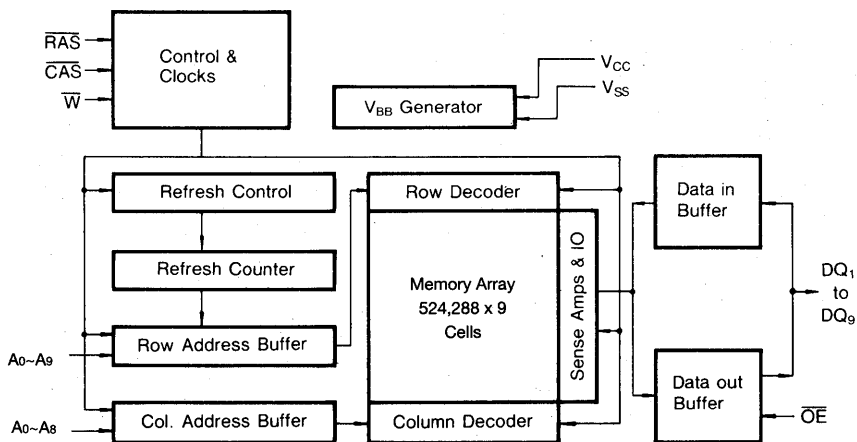
GENERAL DESCRIPTION

The Samsung KM49C512B/BL/BLL is a CMOS high speed 524,288 bit × 9 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM49C512B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

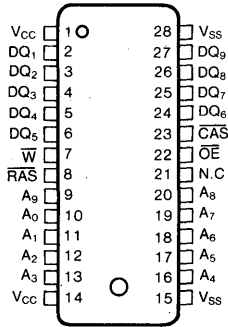
The KM49C512B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



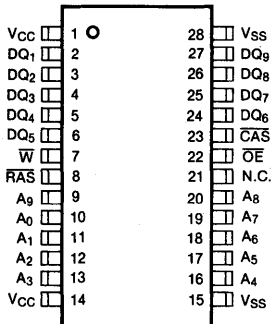
PIN CONFIGURATION (Top Views)

• KM49C512BJ/BLJ/BLLJ



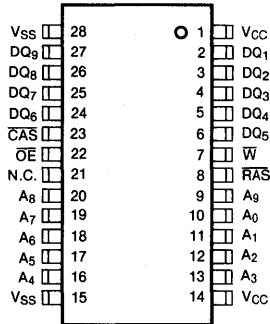
(SOJ)

• KM49C512BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM49C512BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A ₀ -A ₉	Address Input
DQ ₁₋₉	Data In/Out
V _{SS}	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe

Pin Name	Pin Function
W	Read/Write Input
OE	Data Output Enable
V _{CC}	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* (\overline{RAS} , \overline{CAS} , Address Cycling @ t _{RC} =min.)	KM49C512B/BL/BLL-6	I _{CC1}	-	75	mA
	KM49C512B/BL/BLL-7			70	mA
	KM49C512B/BL/BLL-8			65	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)		I _{CC2}	-	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @ t _{RC} =min.)	KM49C512B/BL/BLL-6	I _{CC3}	-	75	mA
	KM49C512B/BL/BLL-7			70	mA
	KM49C512B/BL/BLL-8			65	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @ t _{PC} =min.)	KM49C512B/BL/BLL-6	I _{CC4}	-	55	mA
	KM49C512B/BL/BLL-7			50	mA
	KM49C512B/BL/BLL-8			45	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)	KM49C512B	I _{CC5}	-	1	mA
	KM49C512BL			200	μA
	KM49C512BLL			150	μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @ t _{RC} =min.)	KM49C512B/BL/BLL-6	I _{CC6}	-	75	mA
	KM49C512B/BL/BLL-7			70	mA
	KM49C512B/BL/BLL-8			65	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{CAS}=0.2V$ D _{IN} =Don't Care, T _{RC} =125μS T _{RAS} =T _{RAS} min.~300ns	KM49C512BL	I _{CC7}	-	300	μA
Self Refresh Current $\overline{RAS}=\overline{CAS}=0.2V$ $\overline{W}=\overline{OE}=A_0-A_9=V_{CC}-0.2V$ or 0.2V DQ1-DQ8=V _{CC} -0.2V, 0.2V or Open	KM49C512BLL	I _{CC8}	-	200	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.5V$, all other pins not under test = 0 V)	$I_{I(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -5mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 4.2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , address can be changed maximum two times while $RAS = V_{IL}$. In I_{CC4} , address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{CC} = 5V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 - A_9$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Input Capacitance ($DQ_1 - DQ_9$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{CC} = 5.0V \pm 10\%$, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	10		15		15		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to \overline{RAS}	tAR	45		55		60		ns	6
Column address to \overline{RAS} lead time	trAL	30		35		40		ns	
Read command set-up time	trCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	trCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	trRH	0		0		0		ns	9
Write command set-up time	twCS	0		0		0		ns	8
Write command hold time	twCH	10		10		10		ns	
Write command hold time referenced to \overline{RAS}	twCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to \overline{RAS} lead time	trWL	15		15		20		ns	
Write command to \overline{CAS} lead time	tcWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to \overline{RAS}	tdHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (LL-version)	tREF		128		128		128	ms	
\overline{CAS} to \overline{W} delay time	tcWD	40		50		50		ns	8
\overline{RAS} to \overline{W} delay time	trWD	85		95		105		ns	8
Column address to \overline{W} delay time	tAWD	55		60		65		ns	8
\overline{CAS} precharge to \overline{W} delay time	tcpWD	60		65		70		ns	
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		10		ns	
\overline{RAS} precharge to \overline{CAS} hold time	trPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} - \overline{B} - \overline{R} counter test cycle)	tcPT	20		25		30		ns	
Access time from \overline{CAS} precharge	tcPA		35		40		45	ns	3
Fast Page mode cycle time	tpC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tpRWC	80		95		100		ns	
\overline{RAS} pulse width (Fast Page mode)	trASP	60	100K	70	100K	80	100K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	trHCP	35		40		45		ns	
\overline{CAS} precharge time (Fast Page mode)	tcp	10		10		10		ns	
Access time from \overline{OE}	toEA		15		20		20	ns	
\overline{OE} to data-in delay time	toED	15		20		20		ns	
Out put buffer turn off delay time from \overline{OE}	toEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	toEH	15		20		20		ns	
\overline{RAS} pulse width (\overline{C} - \overline{B} - \overline{R} self refresh)	trASS	100		100		100		μ s	12
\overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} self refresh)	trPS	110		130		150		ns	12
\overline{CAS} hold time (\overline{C} - \overline{B} - \overline{R} self refresh)	tchs	-50		-50		-50		ns	12

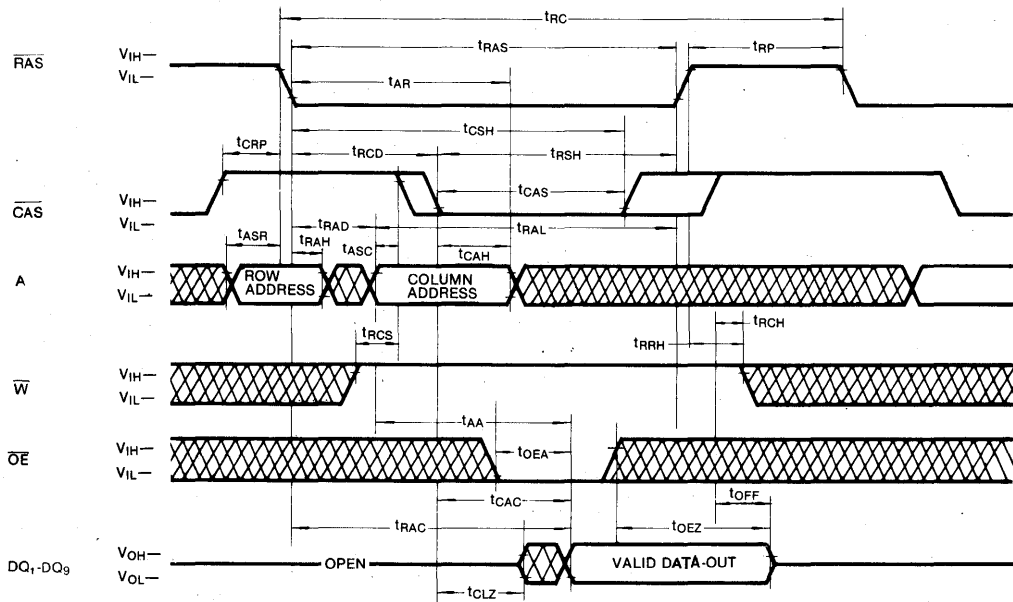
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}}(\text{max})$.
7. $t_{\text{OFF}}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. 1024 cycle of burst refresh must be executed within 16ms before and after refresh, in order to meet refresh specification(LL-version).

4

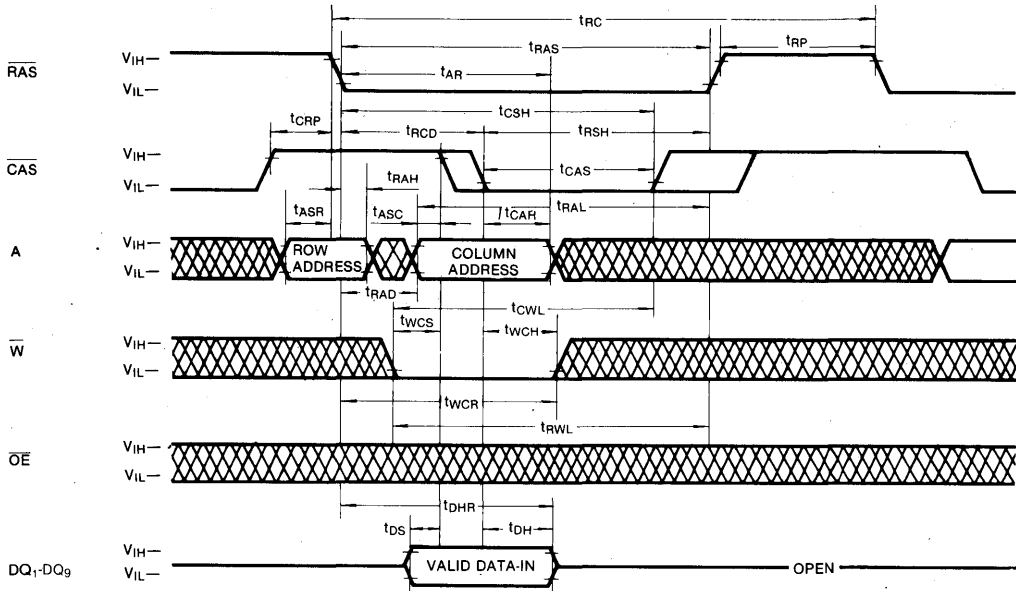
TIMING DIAGRAMS

READ CYCLE

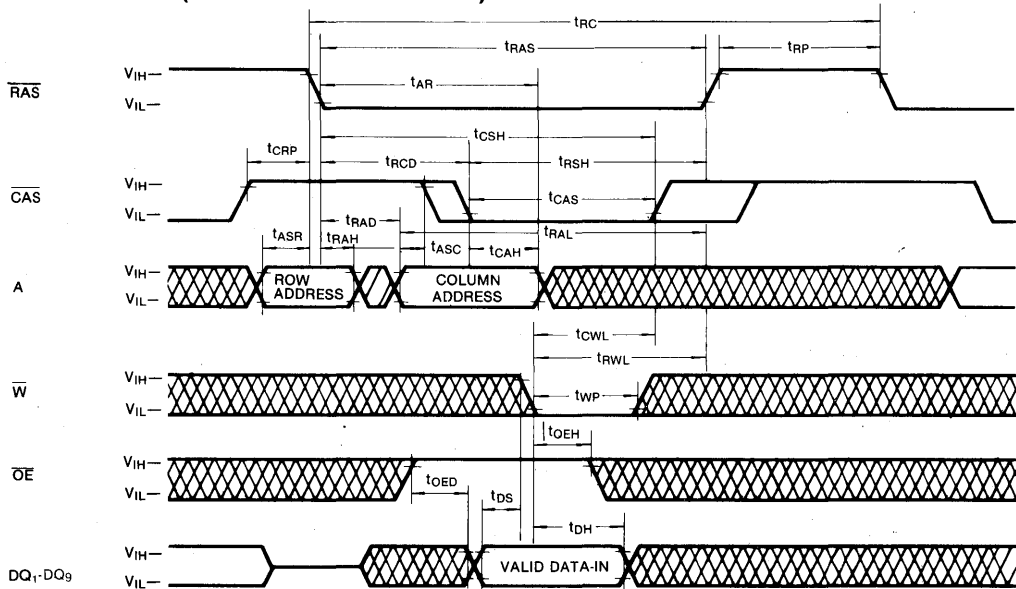


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



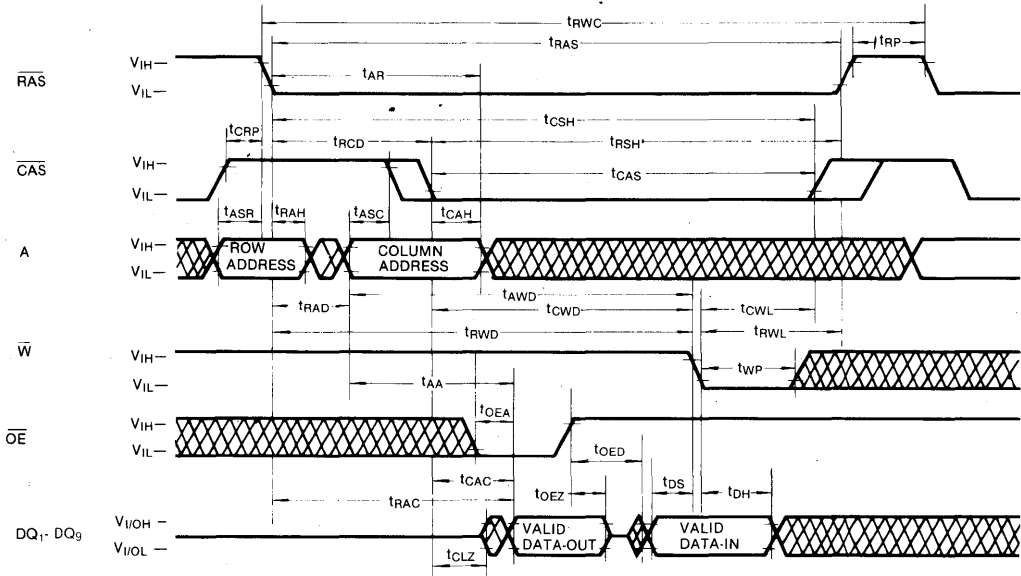
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)



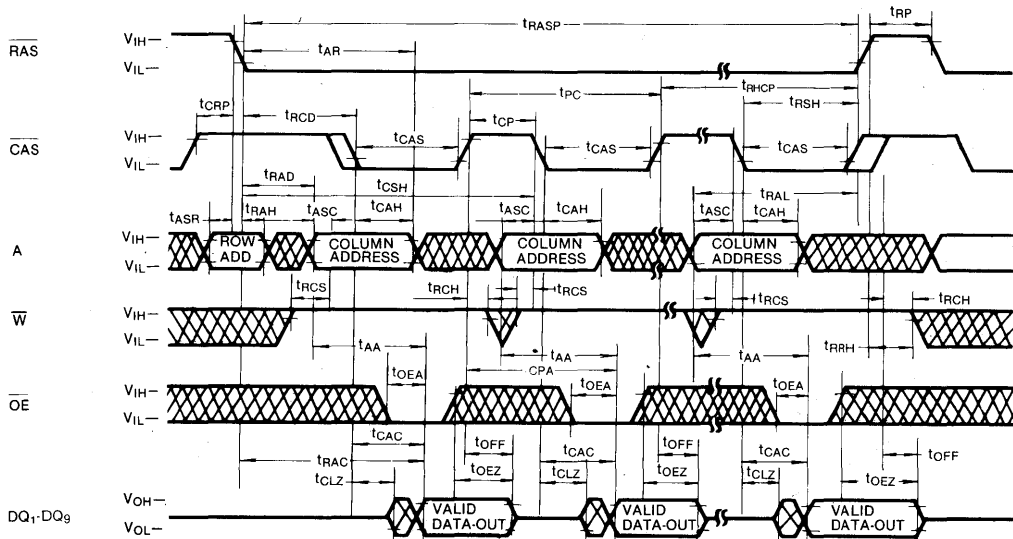
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

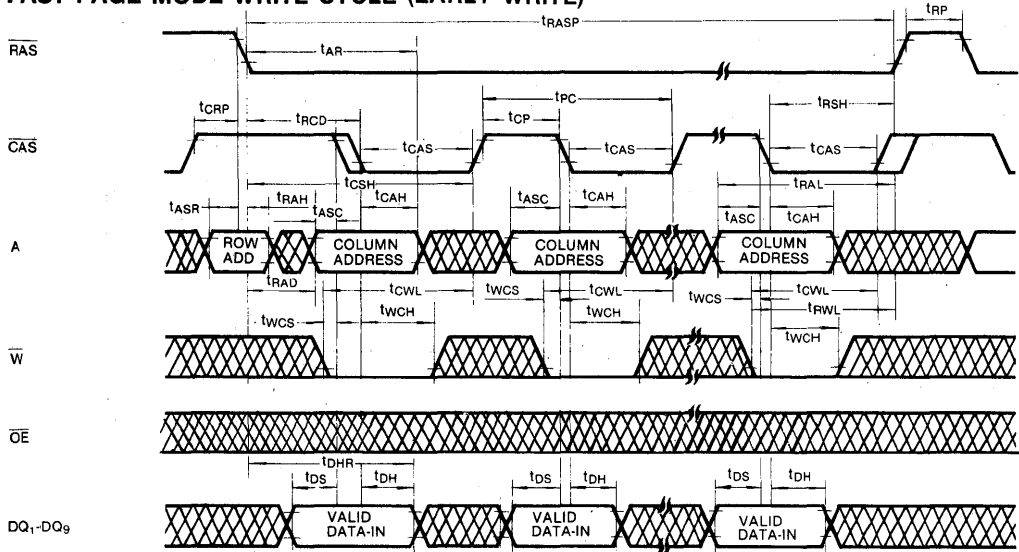


DON'T CARE

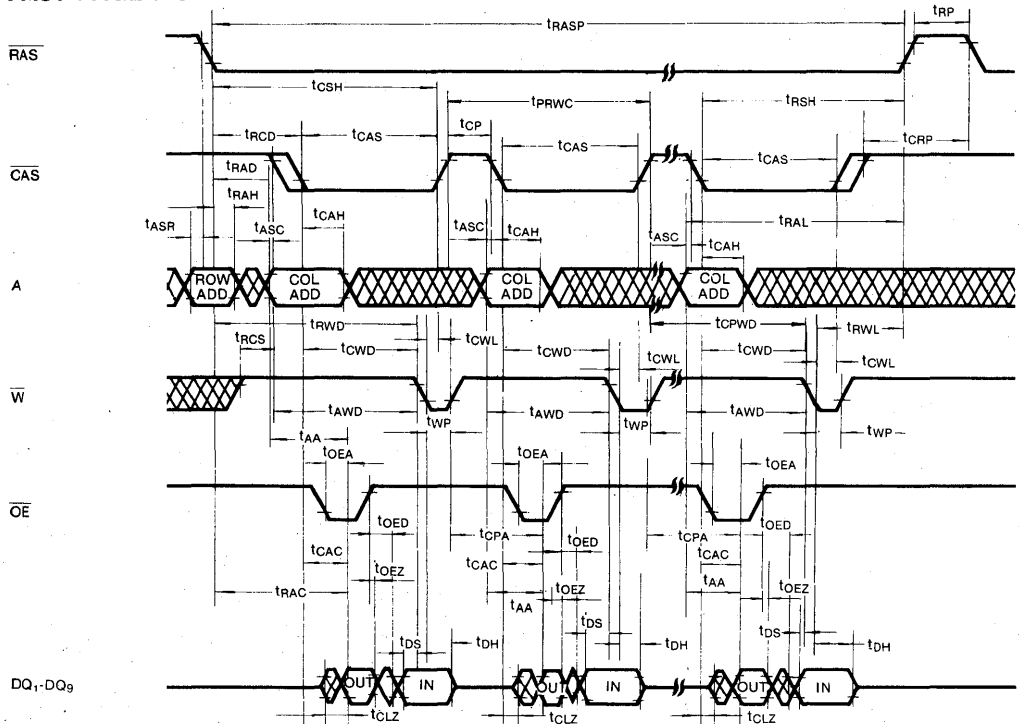
4

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

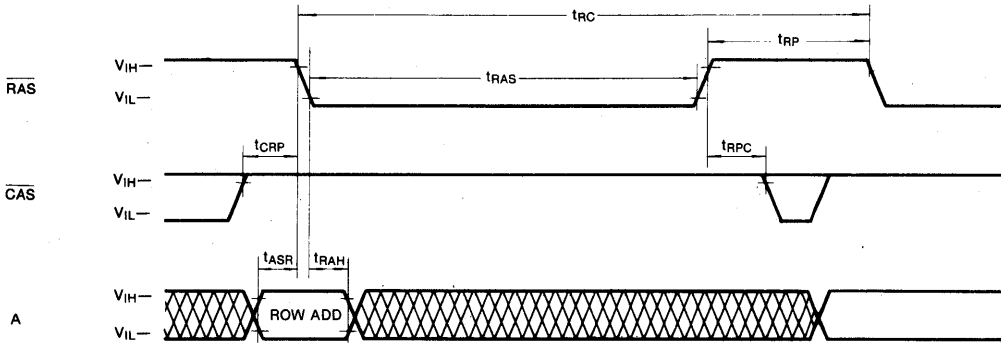


DON'T CARE

TIMING DIAGRAMS (Continued)

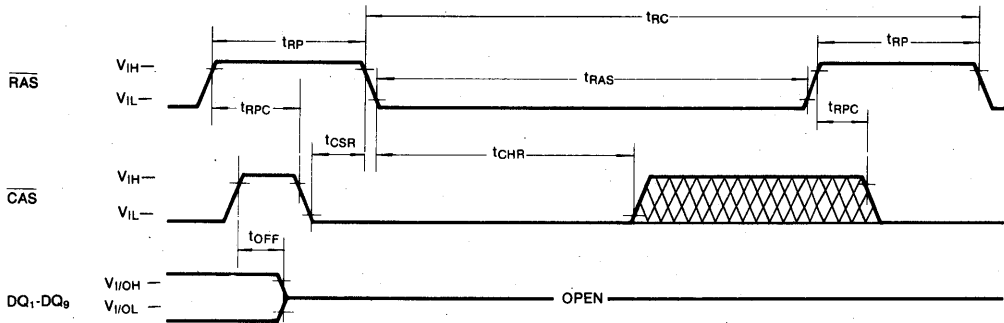
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



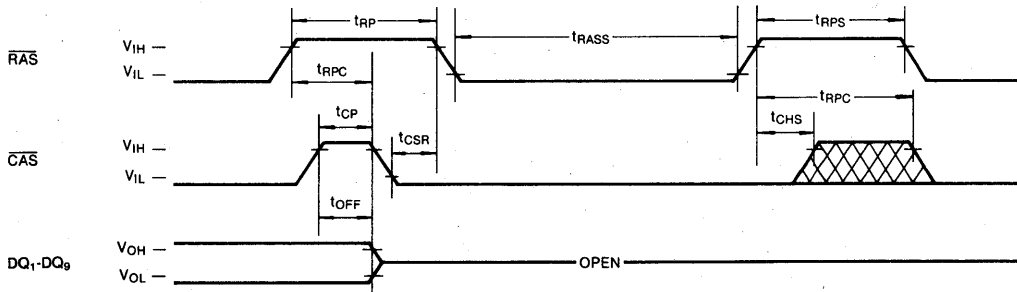
CAS-before-RAS REFRESH CYCLE


NOTE: \bar{W} , \bar{OE} , A = Don't Care



CAS-before-RAS SELF REFRESH CYCLE (LL-version)

NOTE: \bar{W} , \bar{OE} , A = Don't Care

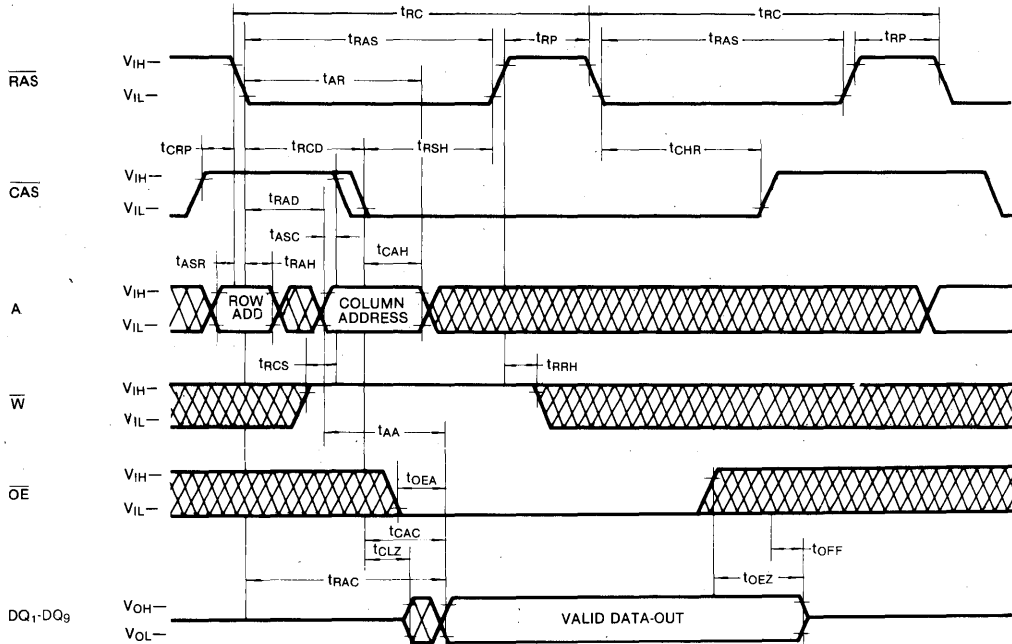


 DON'T CARE

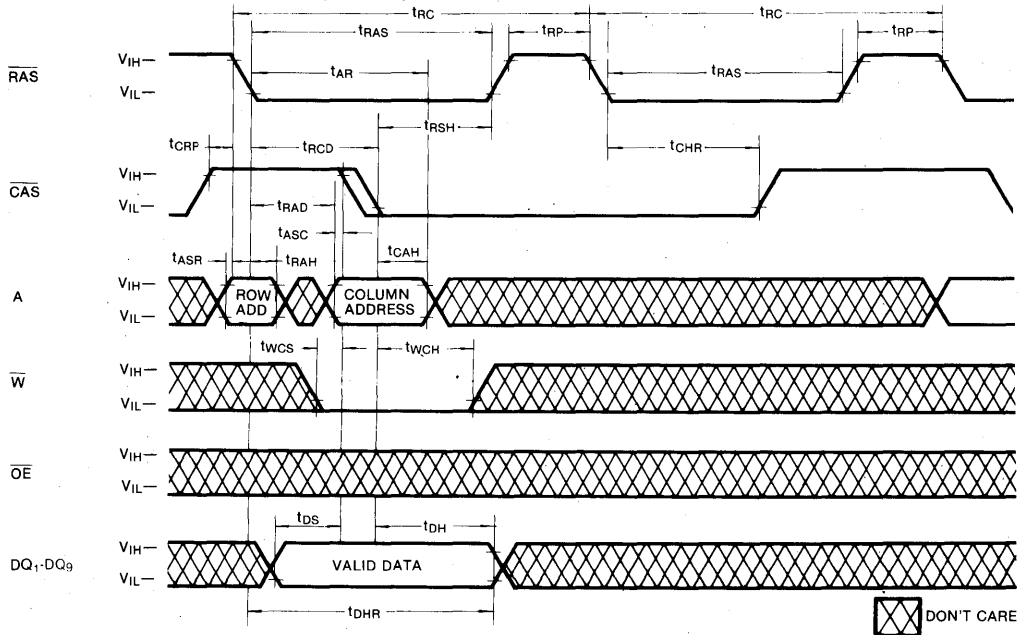
4

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



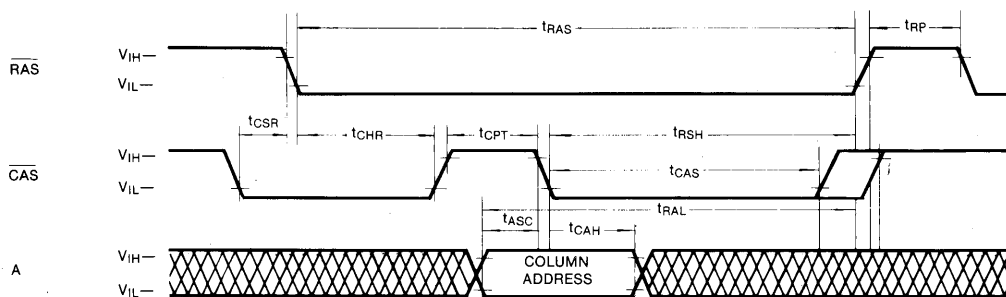
HIDDEN REFRESH CYCLE (WRITE)



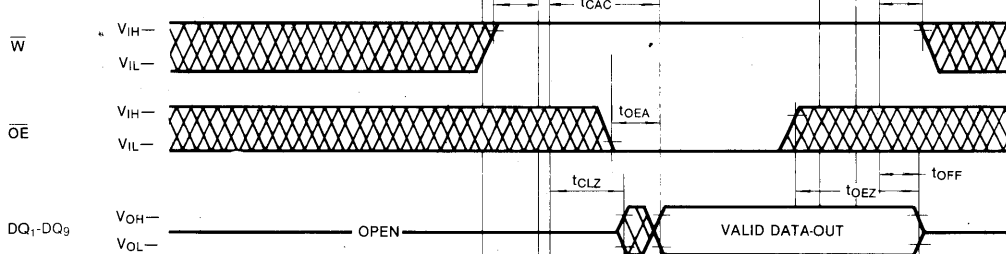
DON'T CARE

TIMING DIAGRAMS (Continued)

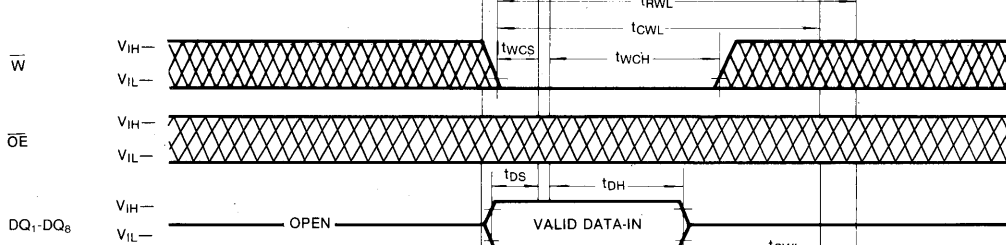
CAS-before-RAS REFRESH COUNTER TEST CYCLE



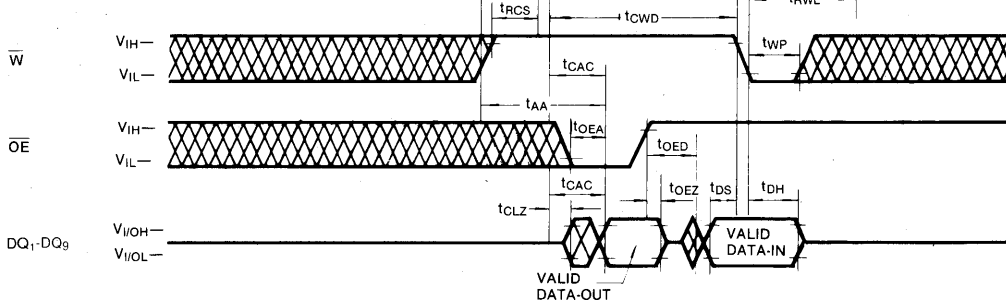
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



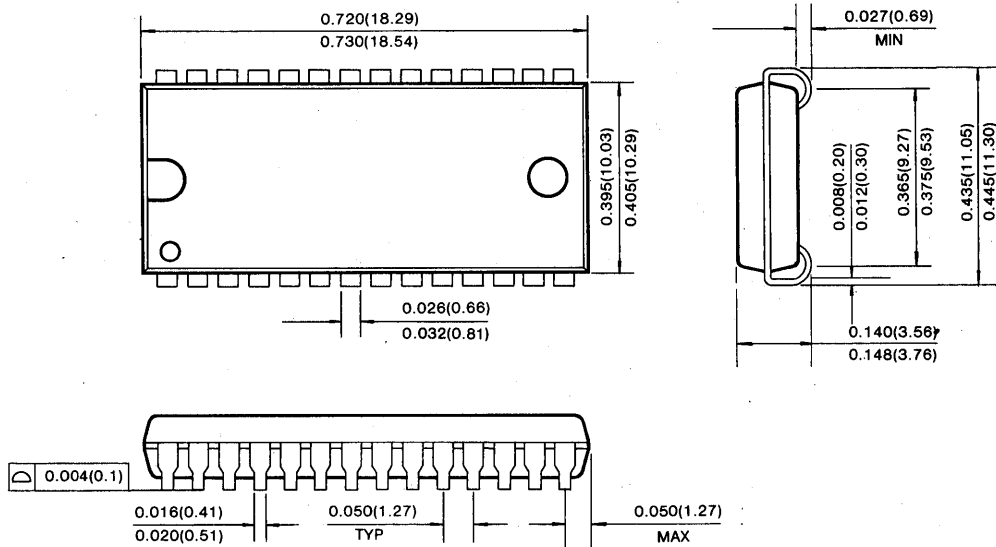
 DON'T CARE

4

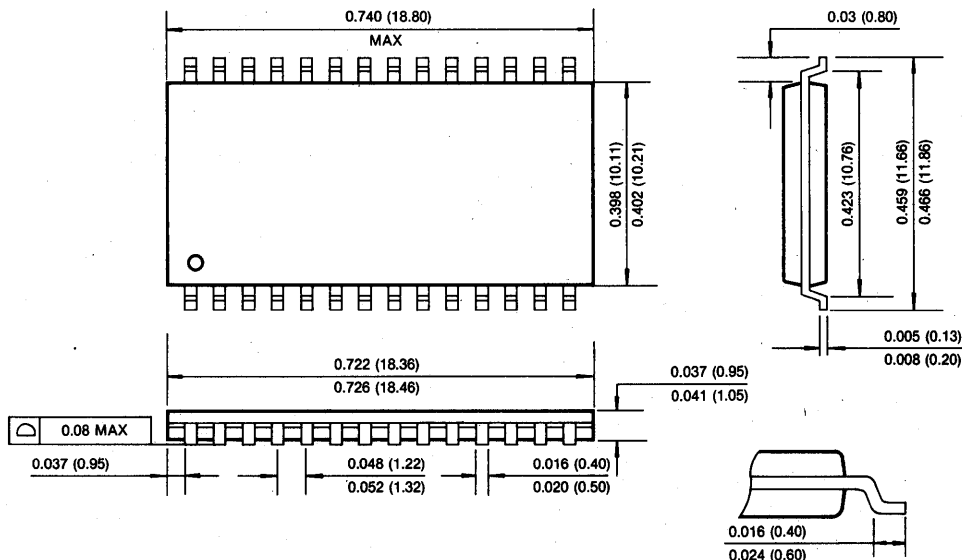
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM416C256B/BL/BLL-5	50ns	15ns	90ns
KM416C256B/BL/BLL-6	60ns	15ns	110ns
KM416C256B/BL/BLL-7	70ns	20ns	130ns
KM416C256B/BL/BLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Self Refresh operation (LL-version)
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +5.0V ± 10% power supply
- Refresh Cycle
 - 512 cycle/8ms (Normal)
 - 512 cycle/64ms (L-version)
 - 512 cycle/128ms (LL-version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.83mW (LL-version)
 - Active (50/60/70/80): 605/495/440/415mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

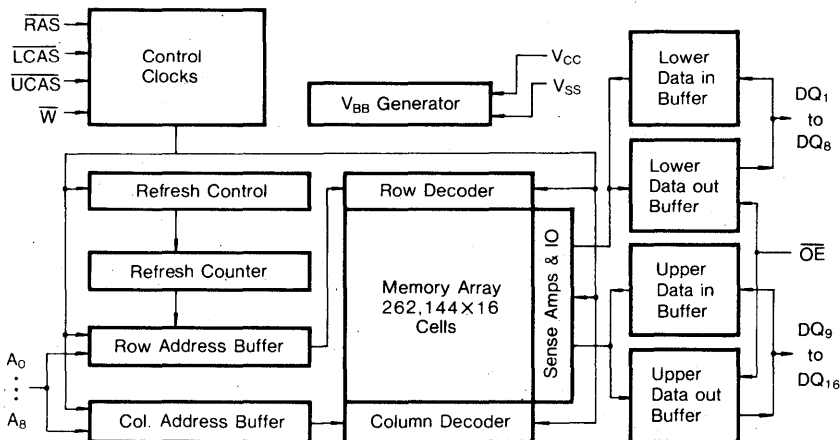
GENERAL DESCRIPTION

The Samsung KM416C256B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C256B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

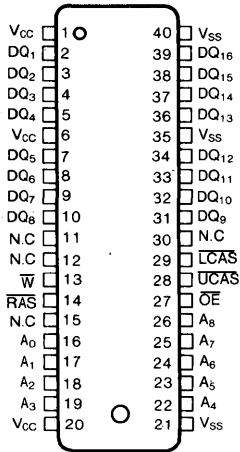
The KM416C256B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



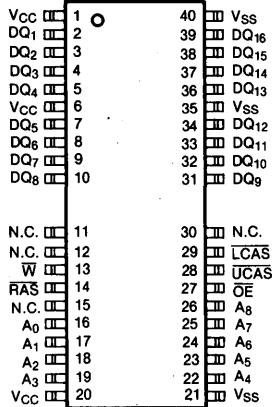
PIN CONFIGURATION (Top Views)

• KM416C256B/BLJ/BLLJ



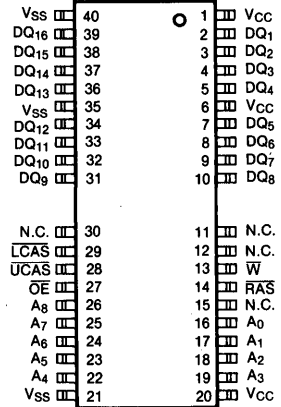
(SOJ)

• KM416C256BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM416C256BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function	Pin Name	Pin Function
A ₀ -A ₈	Address Inputs	\bar{LCAS}	Lower Column Address Strobe
DQ ₁₋₁₆	Data In/Out	\bar{W}	Read/Write Input
V _{SS}	Ground	\bar{OE}	Data Output Enable
\bar{RAS}	Row Address Strobe	V _{CC}	Power (+ 5V)
\bar{UCAS}	Upper Column Address Strobe	N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

4

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} , \overline{UCAS} or \overline{LCAS} , Address Cycling @trc=min.)	KM416C256B/BL/BLL-5 KM416C256B/BL/BLL-6 KM416C256B/BL/BLL-7 KM416C256B/BL/BLL-8 I _{CC1}	-	110 90 80 75	mA mA mA mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)	I _{CC2}	-	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, \overline{RAS} , Address Cycling @trc=min.)	KM416C256B/BL/BLL-5 KM416C256B/BL/BLL-6 KM416C256B/BL/BLL-7 KM416C256B/BL/BLL-8 I _{CC3}	-	110 90 80 75	mA mA mA mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{UCAS} or \overline{LCAS} , Address Cycling @tpc=min.)	KM416C256B/BL/BLL-5 KM416C256B/BL/BLL-6 KM416C256B/BL/BLL-7 KM416C256B/BL/BLL-8 I _{CC4}	-	70 60 55 50	mA mA mA mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$)	KM416C256B KM416C256BL KM416C256BLL I _{CC5}	-	1 200 150	mA μA μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} , \overline{UCAS} or \overline{LCAS} Cycling @trc=min.)	KM416C256B/BL/BLL-5 KM416C256B/BL/BLL-6 KM416C256B/BL/BLL-7 KM416C256B/BL/BLL-8 I _{CC6}	-	110 90 80 75	mA mA mA mA

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V UCAS=LCAS=0.2V DIN=Don't Care, TRC=125μS TRAS=TRAS min.~300ns	KM416C256BL I _{CC7}	-	300	μA
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A ₀ -A ₈ =V _{CC} -0.2V or 0.2V DQ1-DQ16=V _{CC} -0.2V, 0.2V or Open	KM416C256BLL I _{CC5}	-	200	μA
Input Leakage Current (Any input 0V ≤ V _{IN} ≤ V _{CC} +0.5V, all other pins not under test=0 volts)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ -A ₈)	C _{IN1}	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	C _{IN2}	-	7	pF
Output Capacitance (DQ1-DQ16)	C _{DO}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC}=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	135		155		185		205		ns	
Access time from RAS	t _{RAC}		50		60		70		80	ns	3,4,11
Access time from CAS	t _{CAC}		15		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35		40	ns	3,11
CAS to output in Low-Z	t _{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t _{OFF}	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t _T	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	t _{RP}	30		40		50		60		ns	
RAS pulse width	t _{RS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	t _{RSH}	15		15		20		20		ns	
CAS hold time	t _{CSH}	50		60		70		80		ns	
CAS pulse width	t _{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	

(*) 50ns Product:V_{CC}=5V ± 5%, C_{out}=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS to CAS delay time	tRCD	20	35	20	45	20	50	20	60	ns	
RAS to column address delay time	tRAD	15	25	15	30	15	35	15	40	ns	4
CAS to RAS precharge time	tCRP	5		5		5		5		ns	11
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to RAS	tAR	40		45		55		60		ns	
Column address to RAS lead time	tRAL	25		30		35		40		ns	6
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		0		ns	
Read command hold time referenced to RAS	tRRH	0		0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		10		10		ns	8
Write command hold time referenced to RAS	tWCR	40		45		50		55		ns	
Write command pulse width	tWP	10		10		10		10		ns	6
Write command to RAS lead time	tRWL	15		15		15		20		ns	
Write command to CAS lead time	tCWL	15		15		15		20		ns	
Data-in set-up time	tDS	0		0		0		0		ns	
Data-in hold time	tDH	10		10		15		15		ns	10
Data-in hold time referenced to RAS	tDHR	40		45		55		60		ns	10
Refresh period (Normal)	tREF		8		8		8		8	ms	6
Refresh period (L-version)	tREF		64		64		64		64	ms	
Refresh period (LL-version)	tREF		128		128		128		128	ms	
CAS to W delay time	tCWD	40		40		50		50		ns	
RAS to W delay time	tRWD	75		85		95		105		ns	8
Column address to W delay time	tAWD	50		55		60		65		ns	8
CAS precharge to W delay time	tCPWD	55		60		65		70		ns	8
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	
CAS hold time(CAS-before-RAS refresh)	tCHR	10		10		10		10		ns	
RAS precharge to CAS hold time	tRPC	5		5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		20		25		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Fast page mode cycle time	tPC	35		40		45		50		ns	
Fast page mode read-modify-write cycle time	tRMC	80		80		95		100		ns	
RAS pulse width (Fast Page Mode)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	

(*) 50ns Product:VCC=5V ± 5%, Cout=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS hold time from CAS precharge	trHCP	30		35		40		45		ns	
CAS precharge time (Fast Page Mode)	tCP	10		10		10		10		ns	
access time from OE	toEA		15		15		20		20	ns	
OE to data-in delay time	toED	15		15		20		20		ns	
Output buffer turn off delay time from OE	toEZ	0	15	0	15	0	20	0	20	ns	
OE command hold time	toEH	15		15		20		20		ns	
RAS pulse width (C-B-R self refresh)	trASS	100		100		100		100		μs	12
RAS precharge time (C-B-R self refresh)	trPS	90		110		130		150		ns	12
CAS hold time (C-B-R self refresh)	tCHS	-50		-50		-50		-50		ns	12

(*) 50ns Product:VCC=5V ± 5%, Cout=50pF

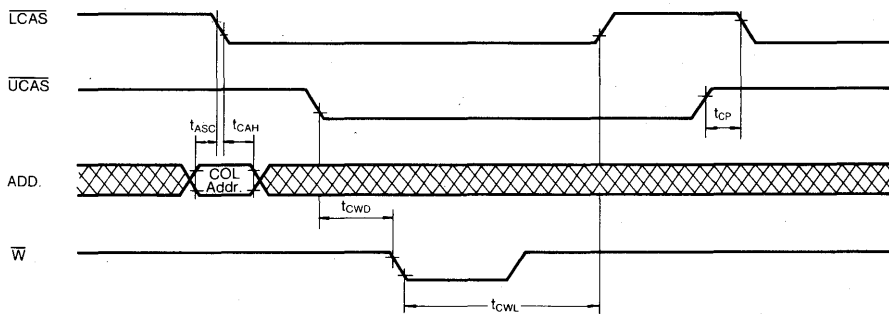
KM416C256B Truth Table

RAS	LCAS	UCAS	W	OE	DQ1-DQ8	DQ9-DQ16	STATE
H	H	H	H	H	HI-Z	HI-Z	Standby
L	H	H	H	H	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

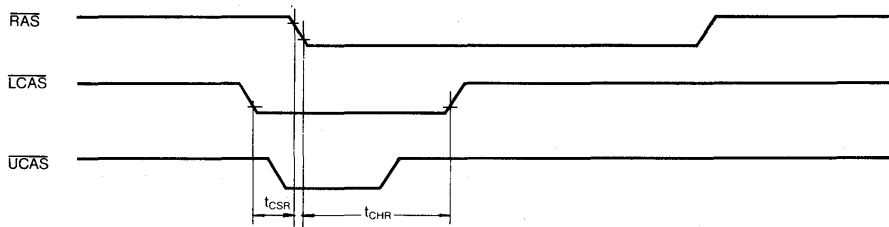
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}(\text{max})}$ limit insures that $t_{\text{RAC}(\text{max})}$ can be met. $t_{\text{RCD}(\text{max})}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}(\text{max})}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}(\text{max})}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}(\text{max})}$.
7. $t_{\text{OFF}(\text{max})}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}(\text{min})}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}(\text{min})}$, $t_{\text{RWD}} \geq t_{\text{RWD}(\text{min})}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\text{min})}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}(\text{max})}$ limit insures that $t_{\text{RAC}(\text{max})}$ can be met. $t_{\text{RAD}(\text{max})}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}(\text{max})}$ limit, then access time is controlled by t_{AA} .
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, in order to meet refresh specification.
13. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
14. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.

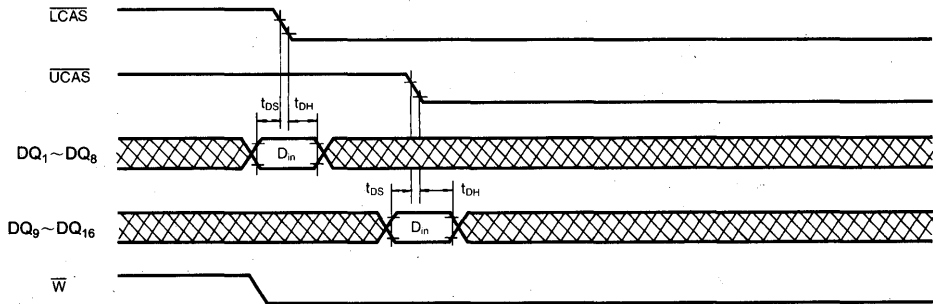
4



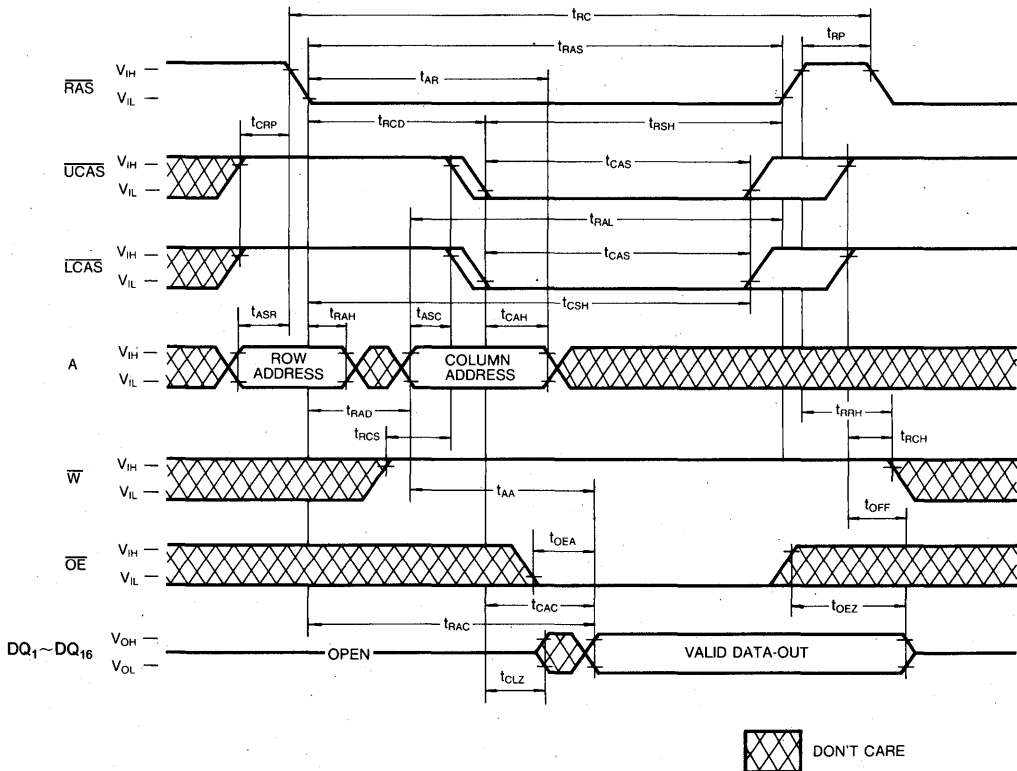
17. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
18. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



19. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1-8)}$, upper byte $D_{in(9-16)}$.

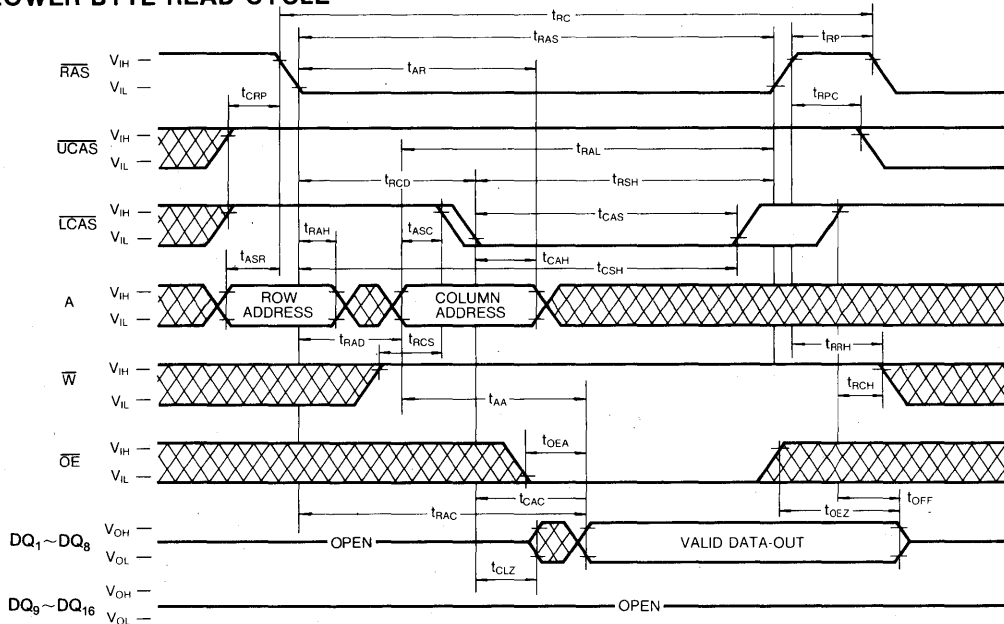


TIMING DIAGRAMS
WORD READ CYCLE

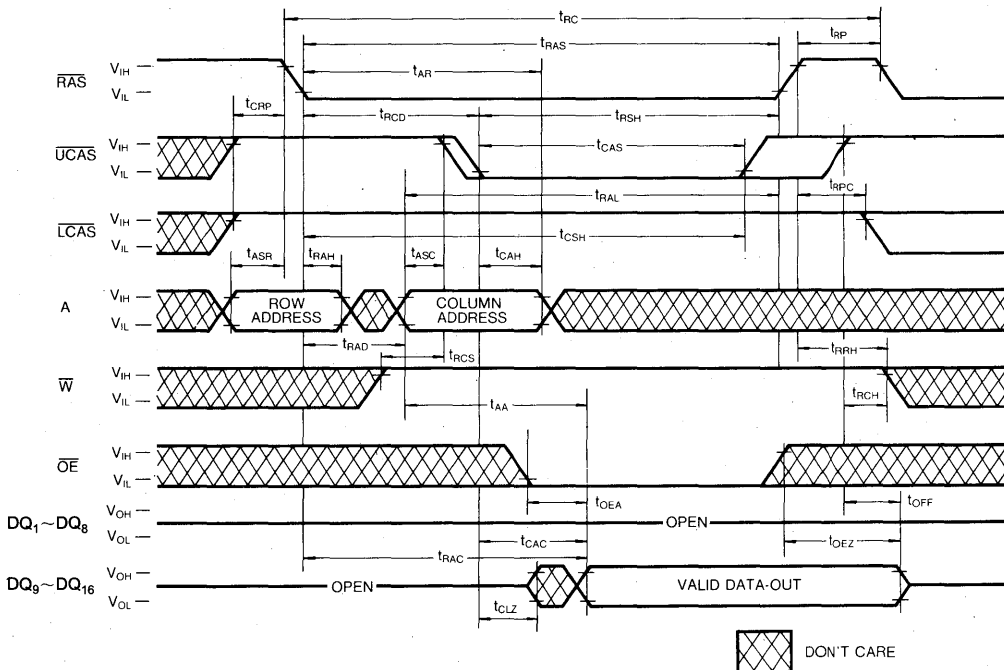


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



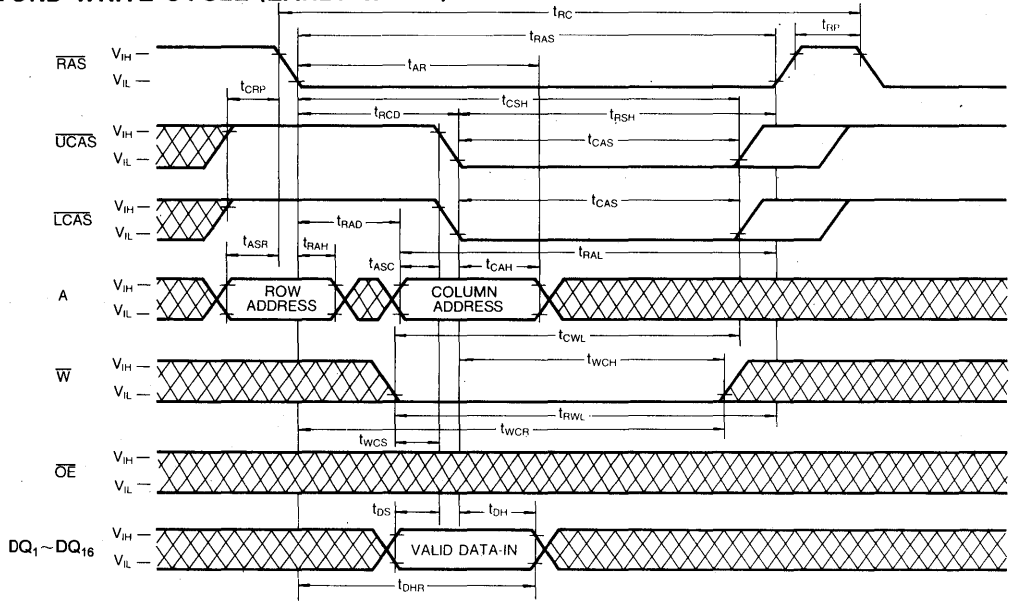
UPPER BYTE READ CYCLE



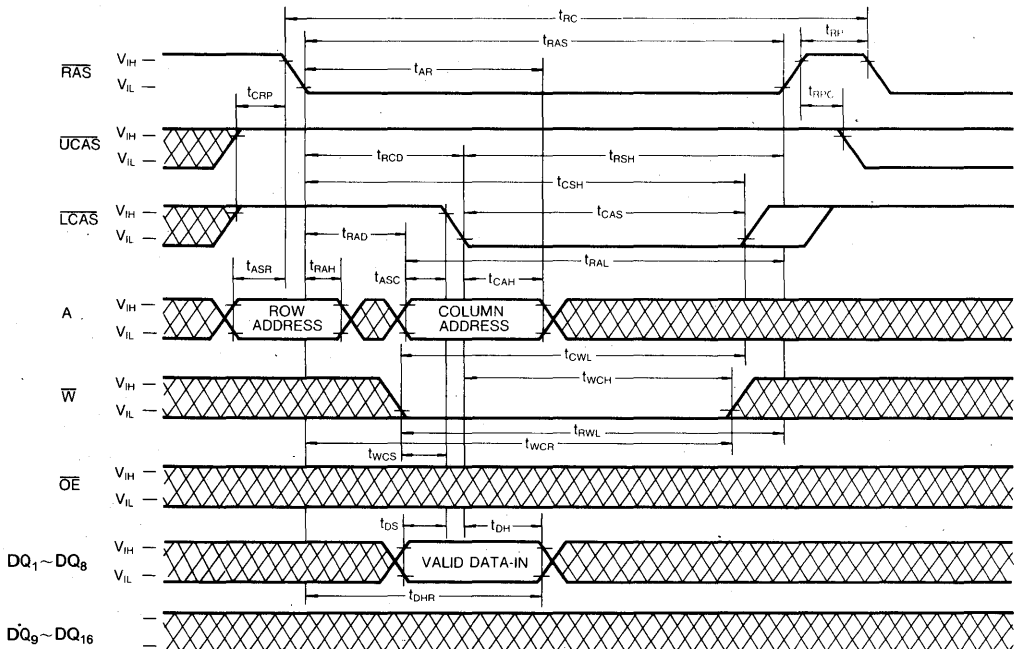
4

TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



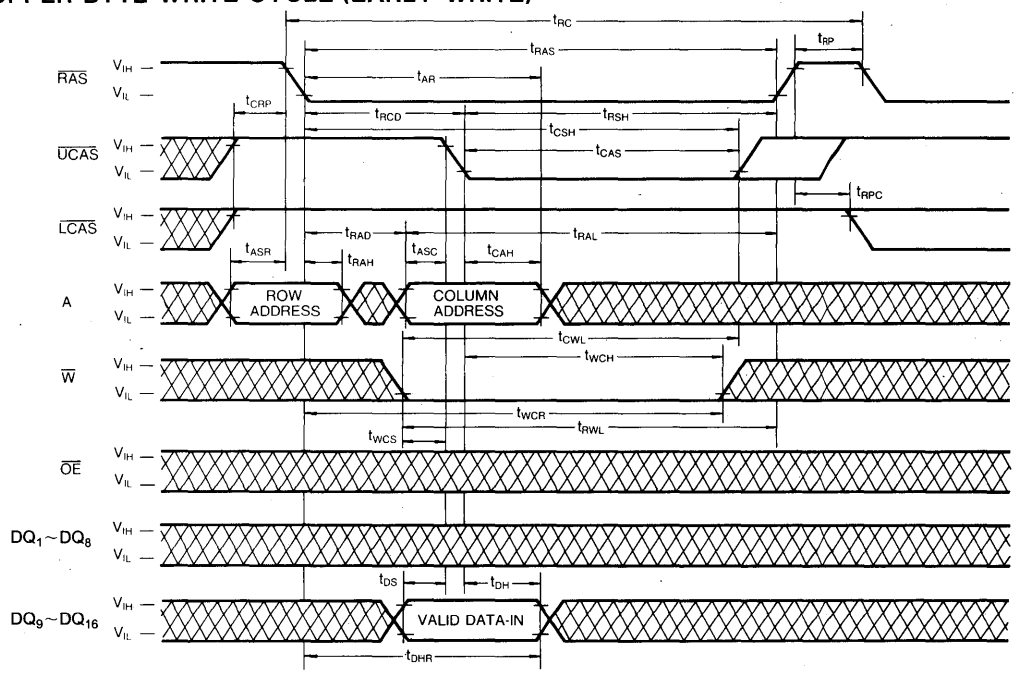
LOWER BYTE WRITE CYCLE (EARLY WRITE)



 DON'T CARE

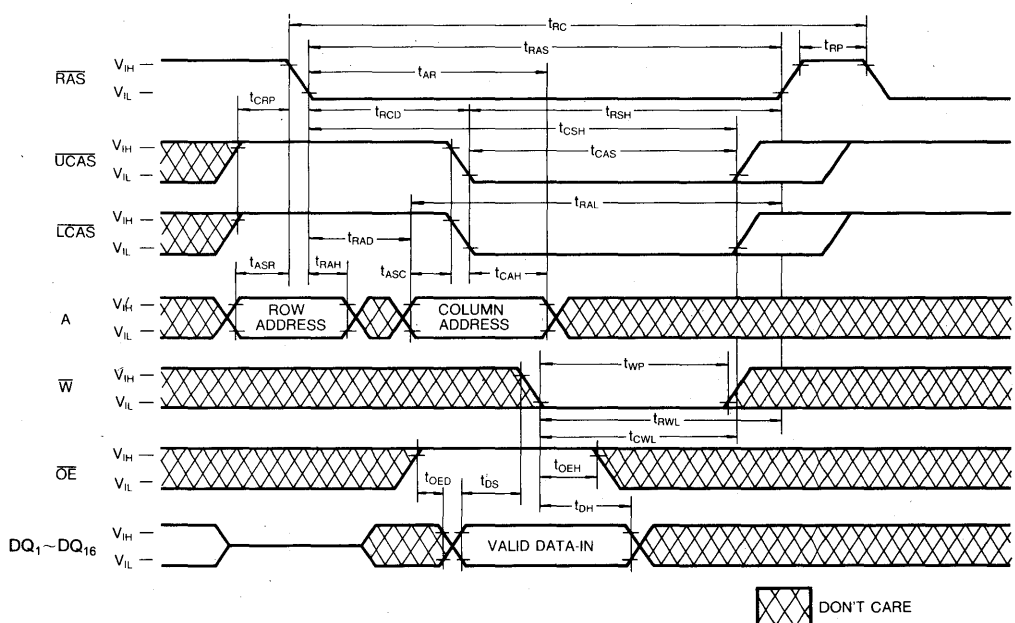
TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



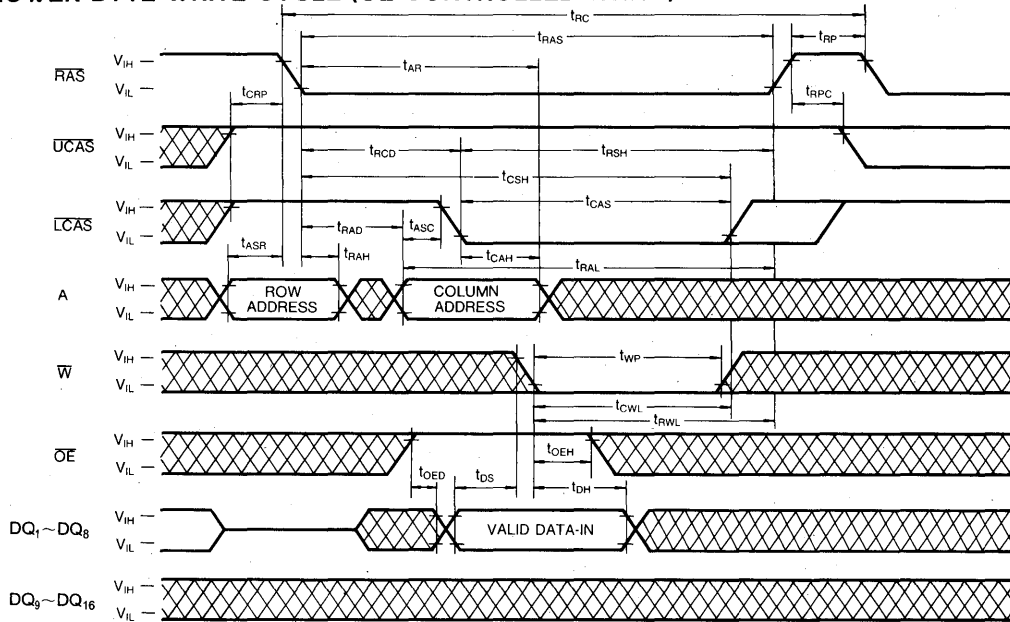
4

WORD WRITE CYCLE (OE CONTROLLED WRITE)

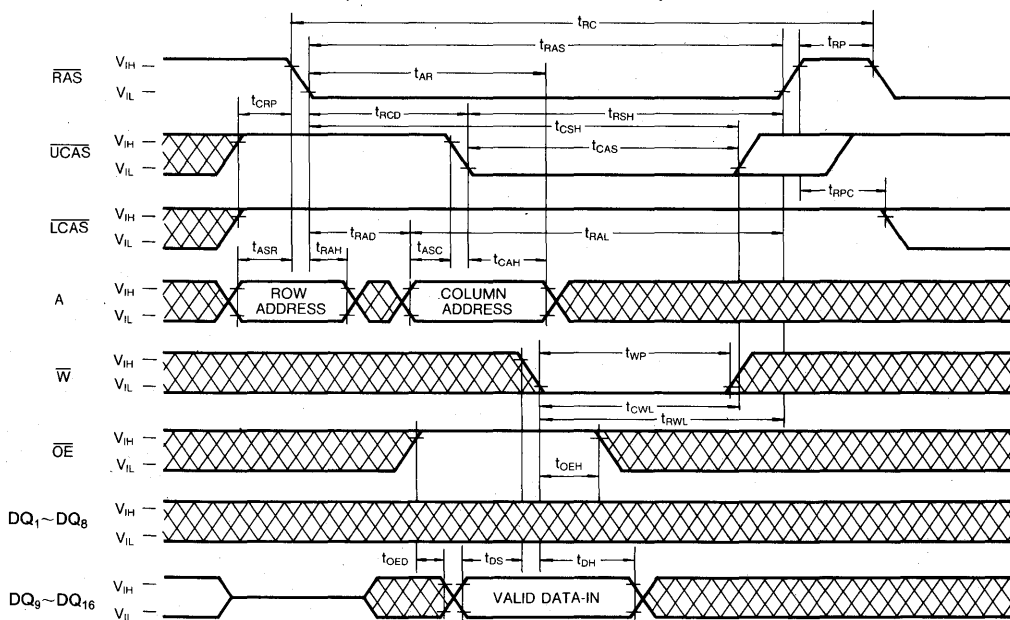


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



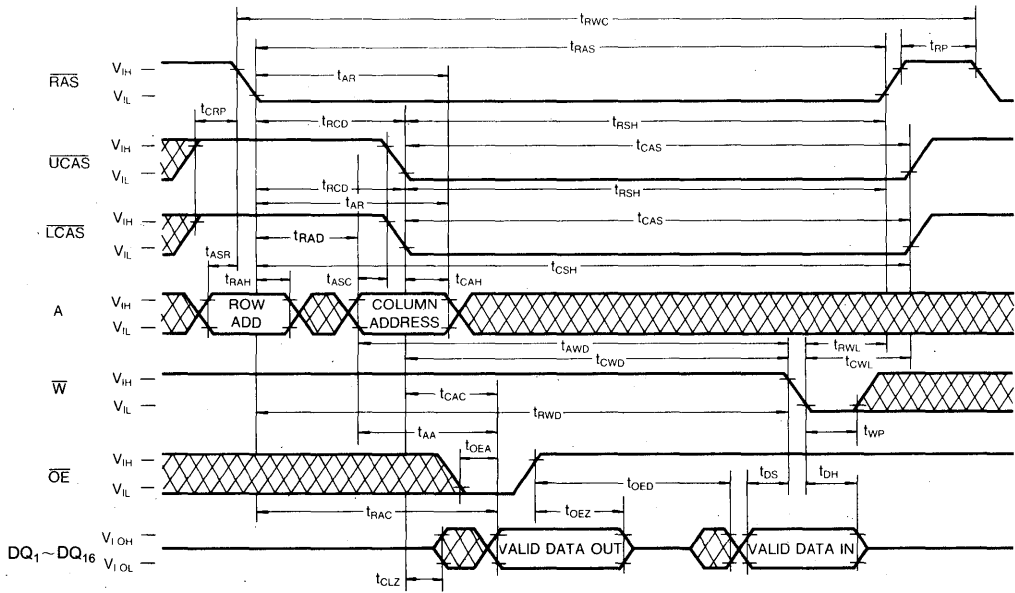
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



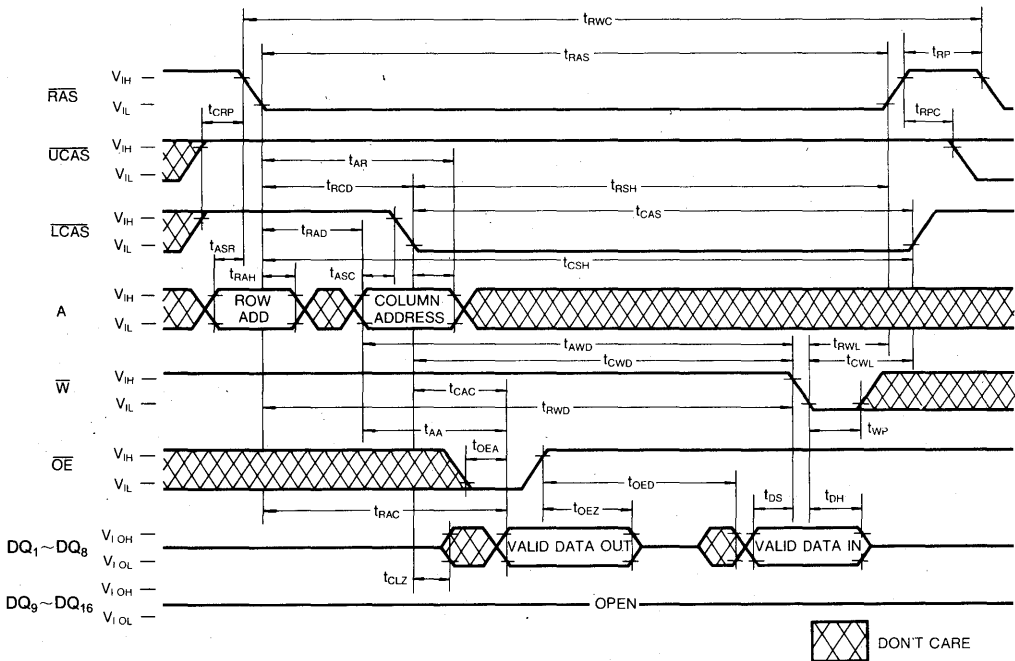
 DONT CARE

TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

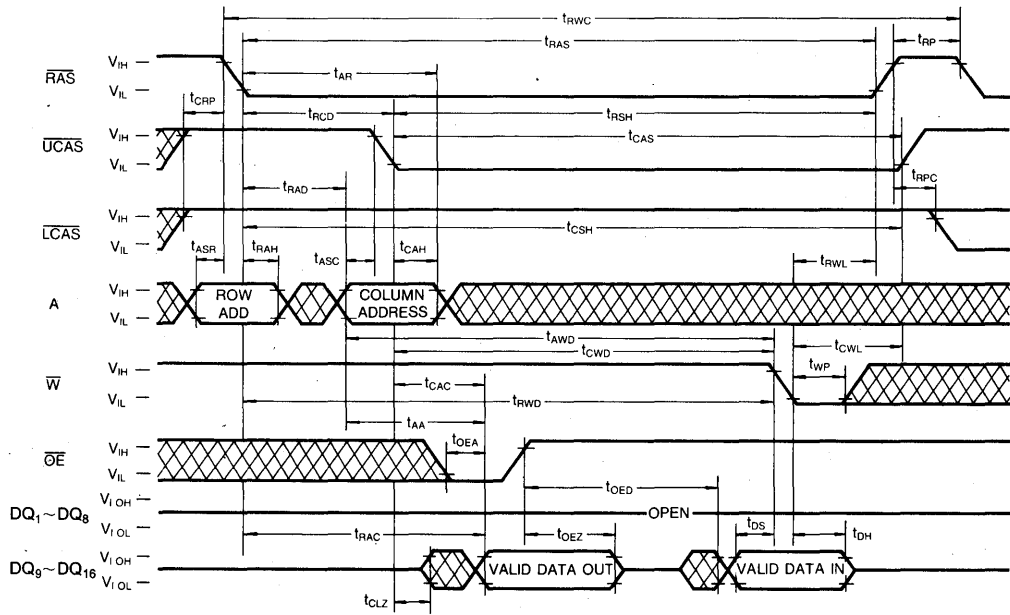


LOWER-BYTE READ-MODIFY-WRITE CYCLE

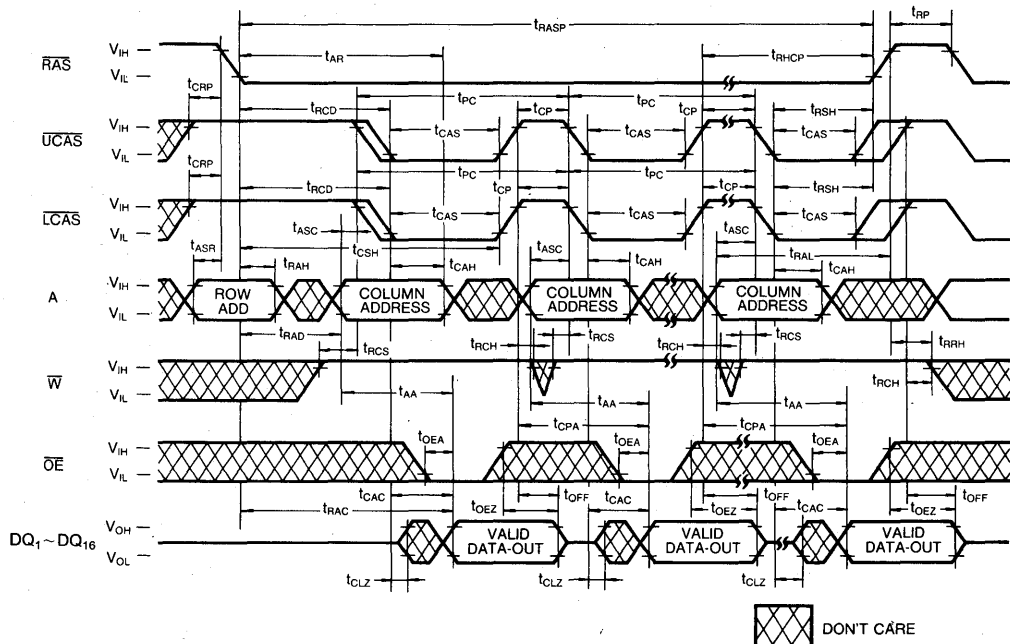


TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE



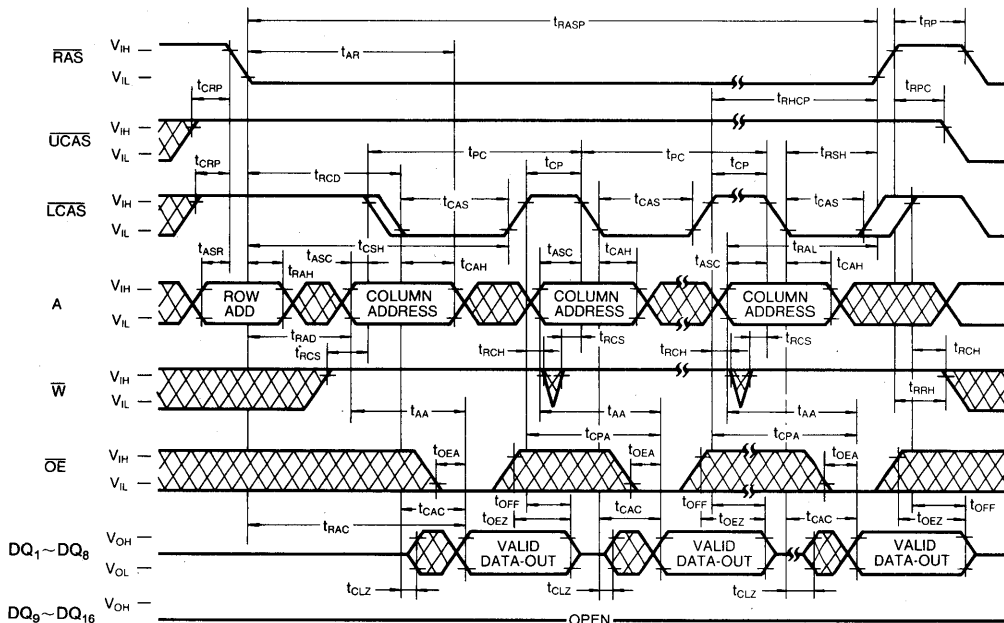
FAST PAGE MODE WORD READ CYCLE



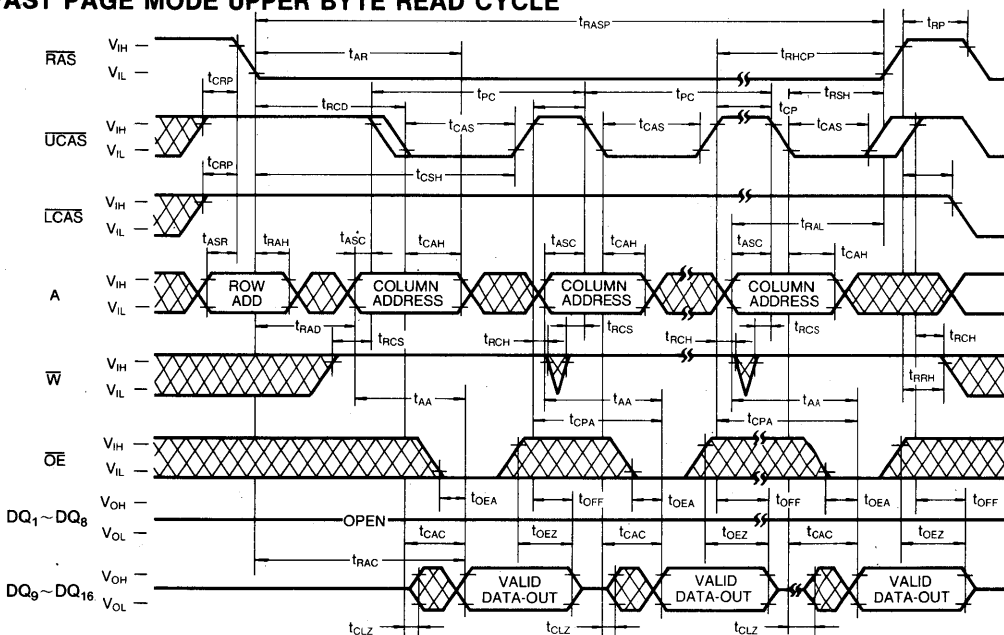
 DONT CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



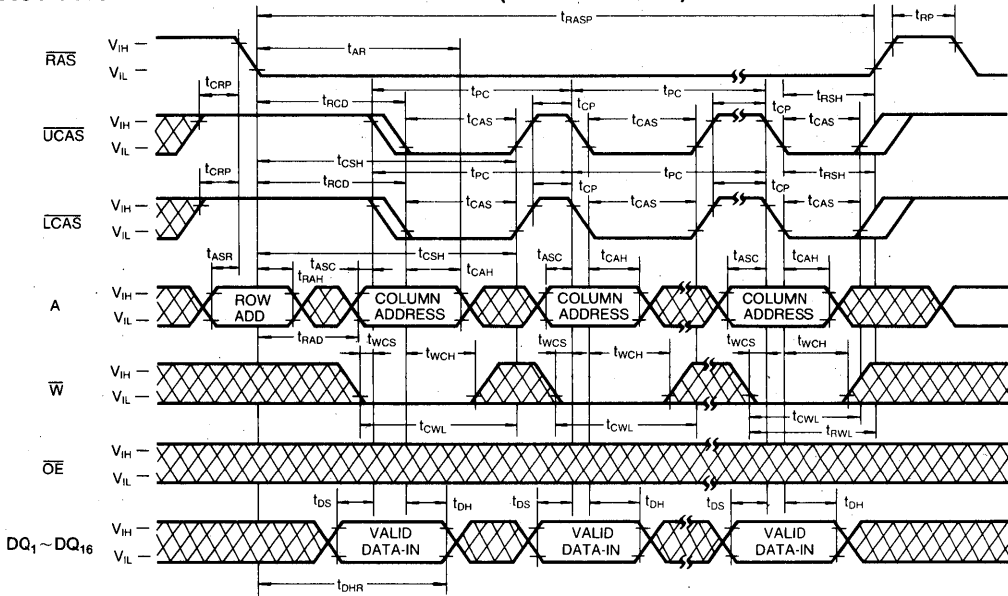
FAST PAGE MODE UPPER BYTE READ CYCLE



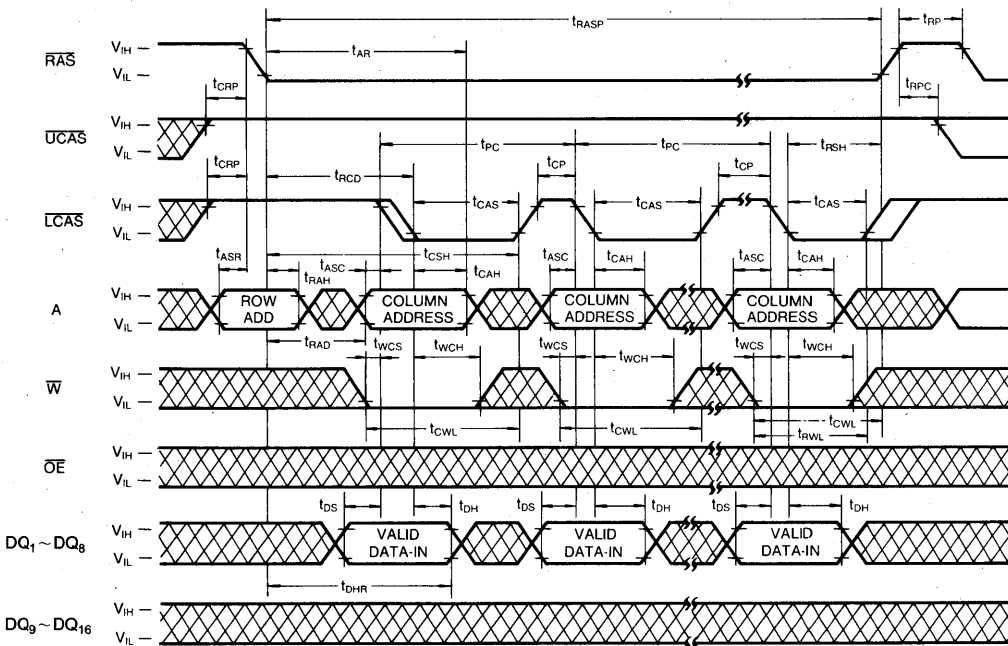
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



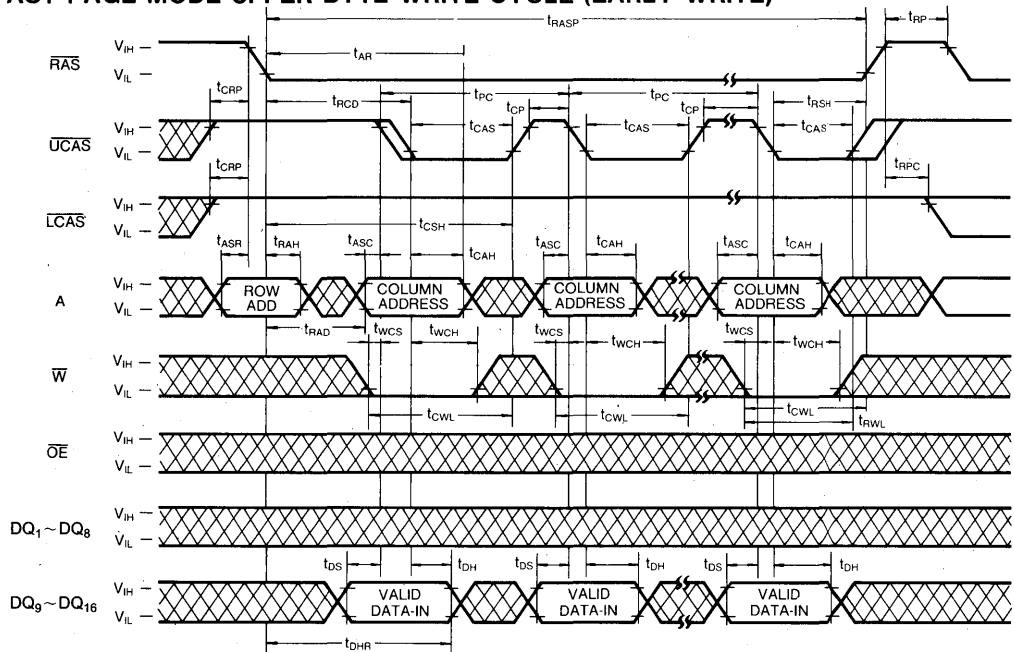
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



 DON'T CARE

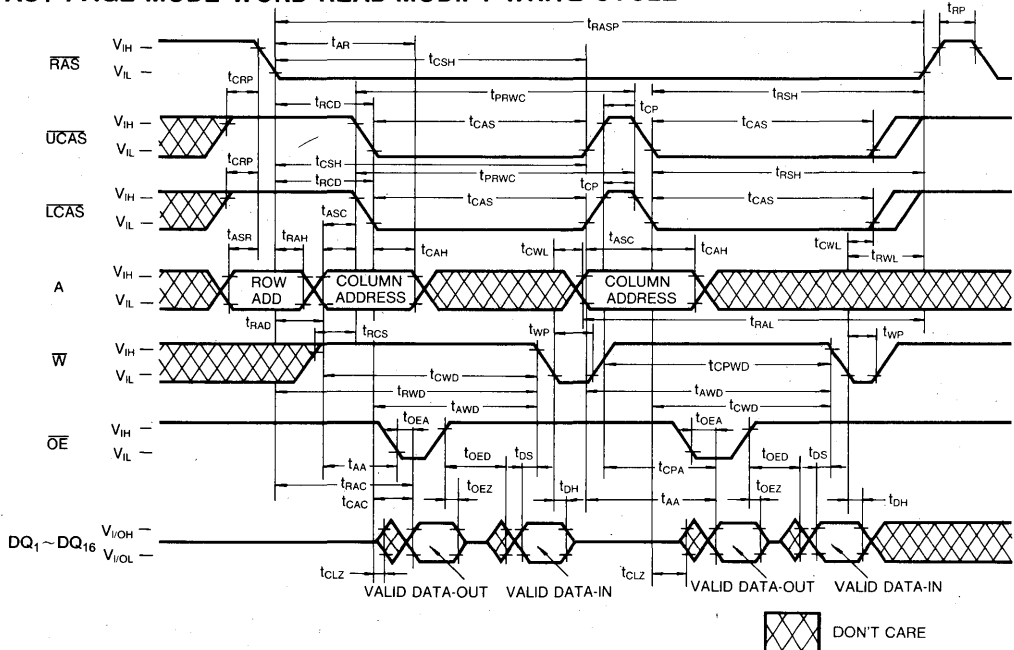
TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



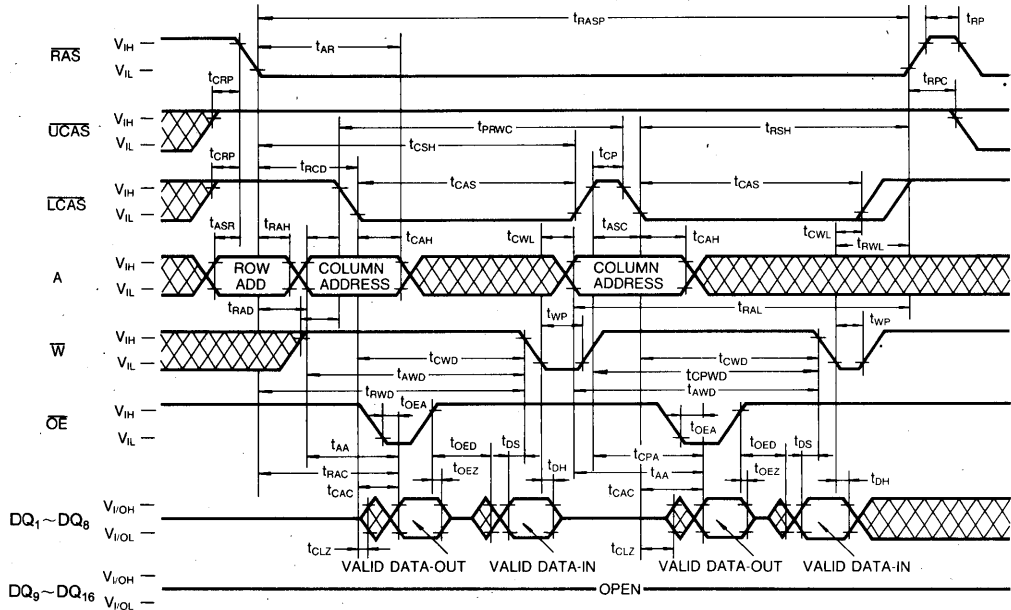
4

FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

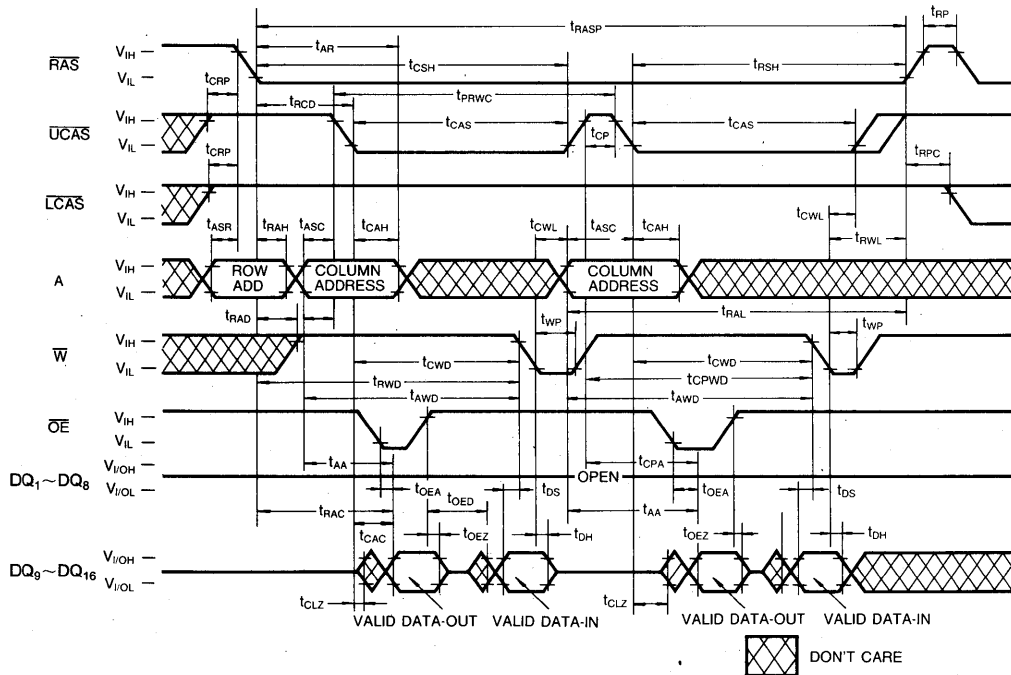


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



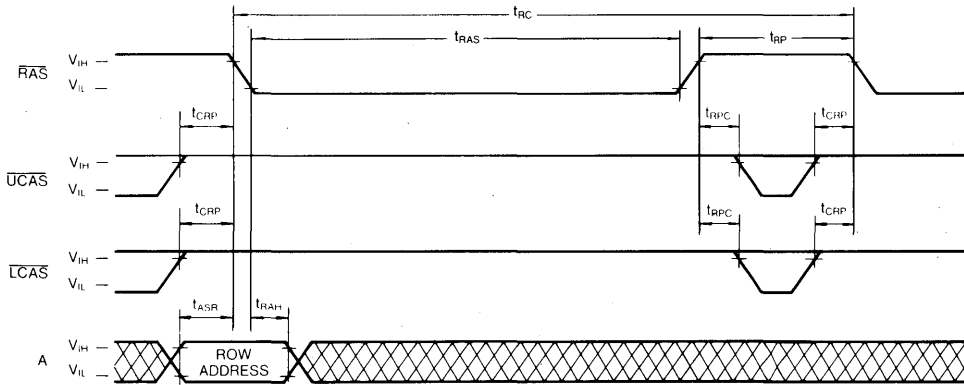
FAST PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

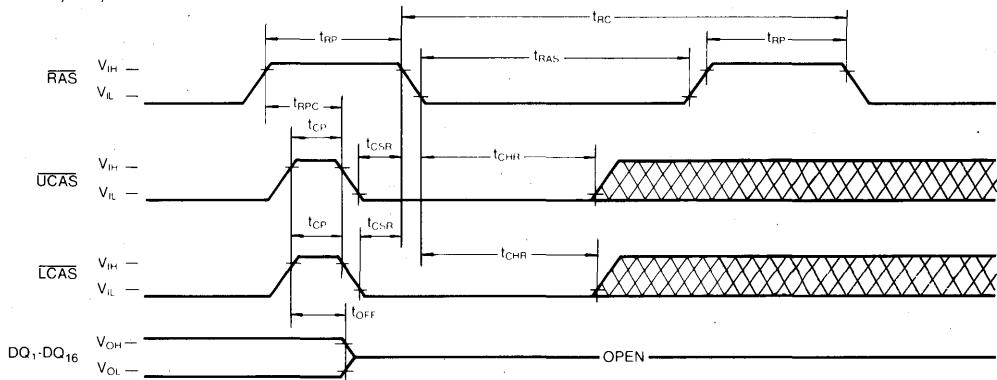
RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care



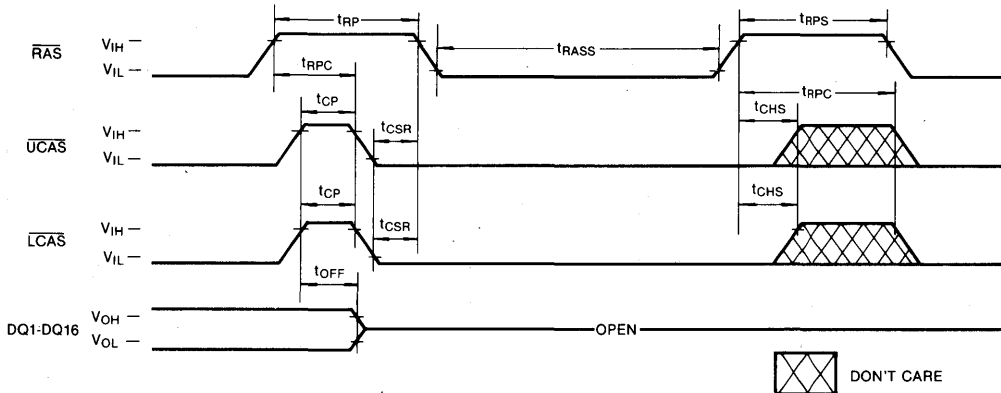
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} , A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

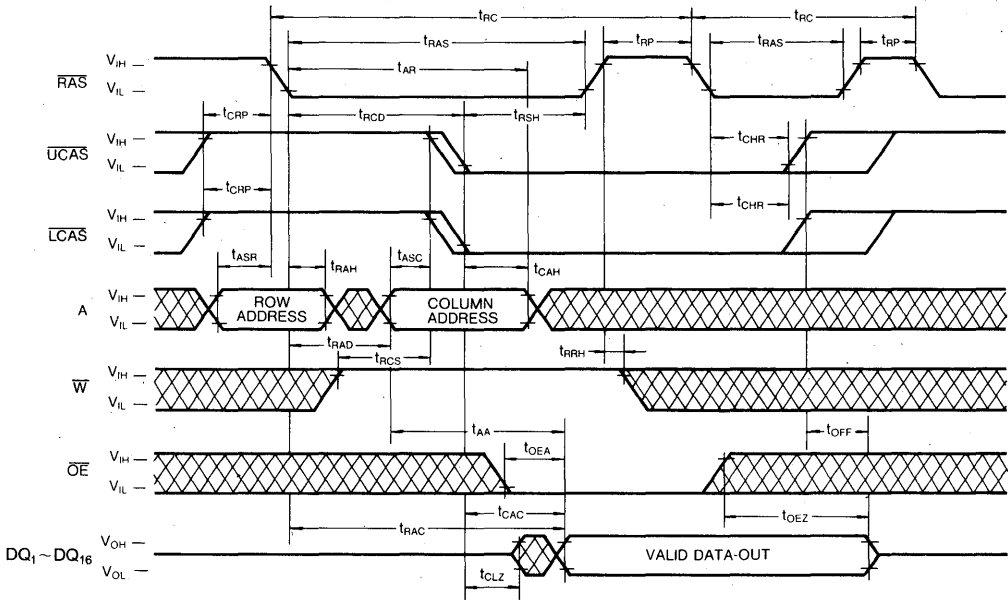
NOTE: \bar{W} , \bar{OE} , A = Don't Care



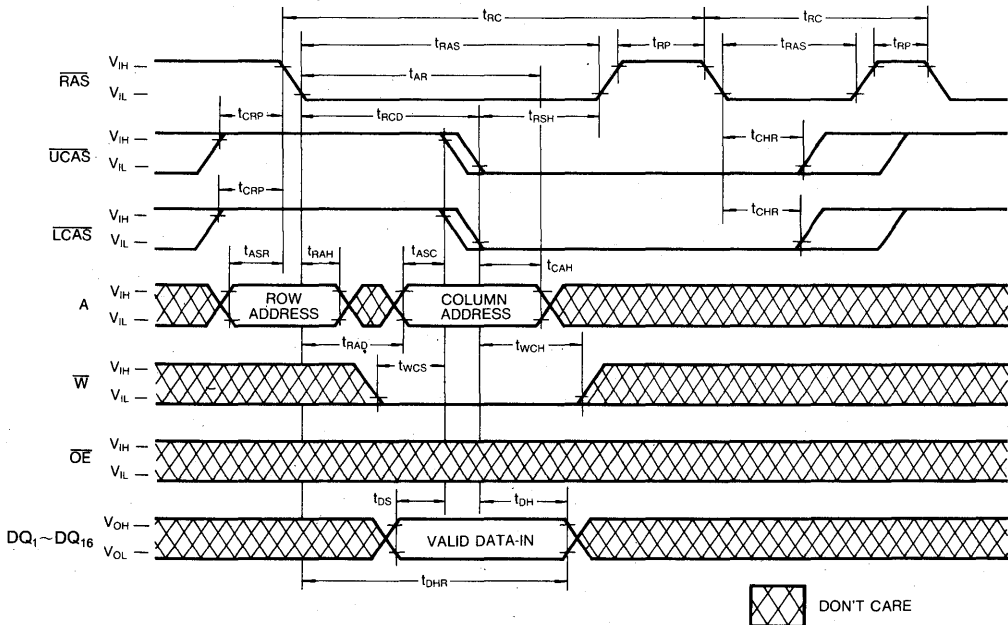
4

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



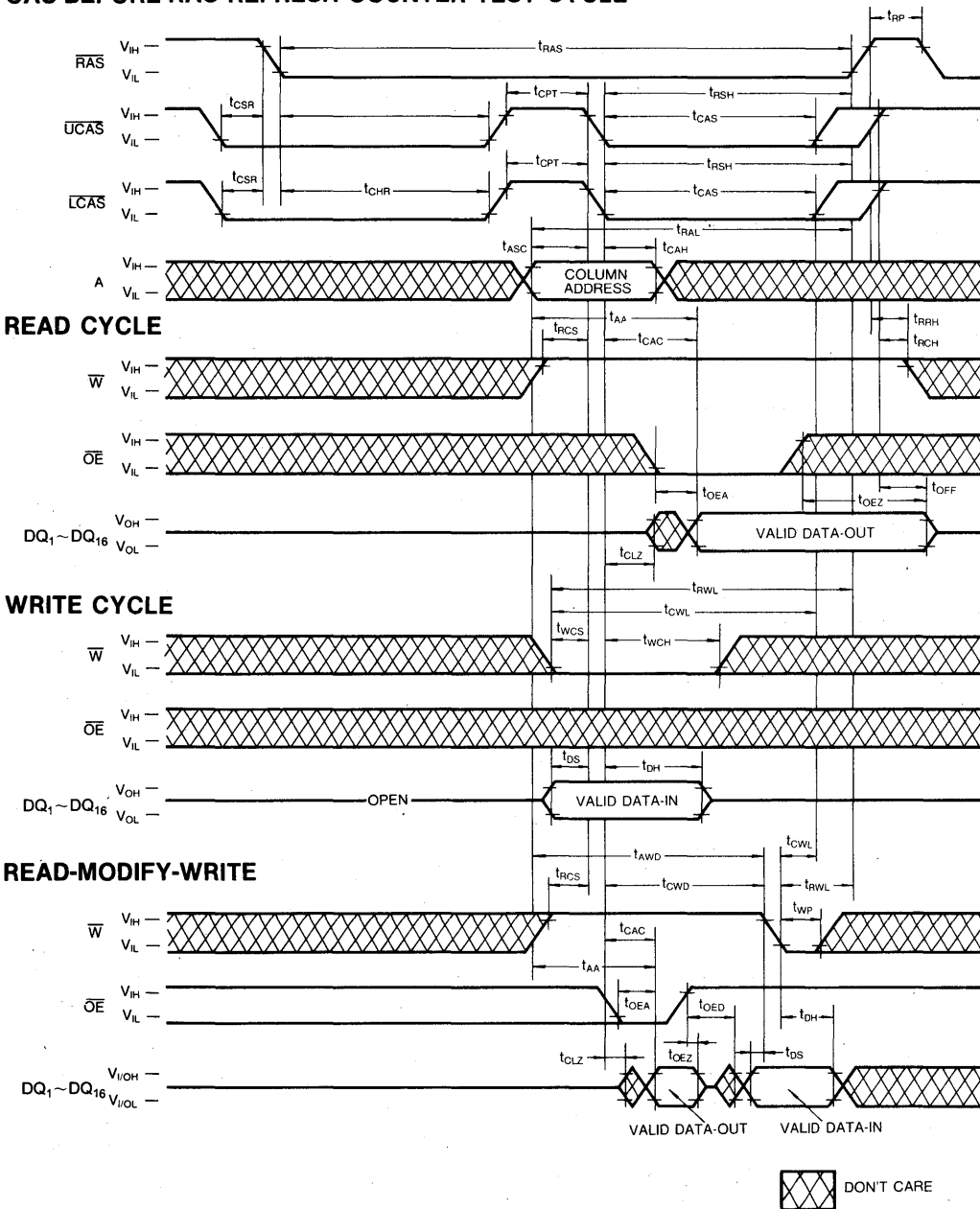
HIDDEN REFRESH CYCLE (WRITE)



 DON'T CARE

TIMING DIAGRAMS (Continued)

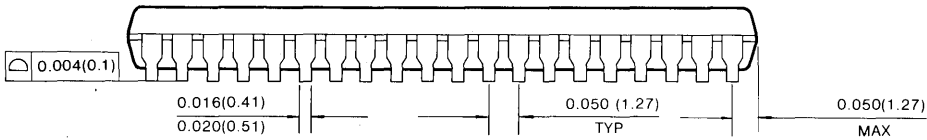
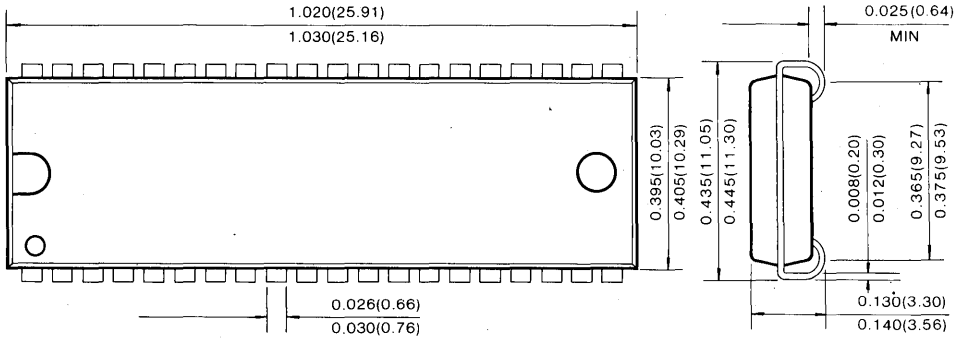
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



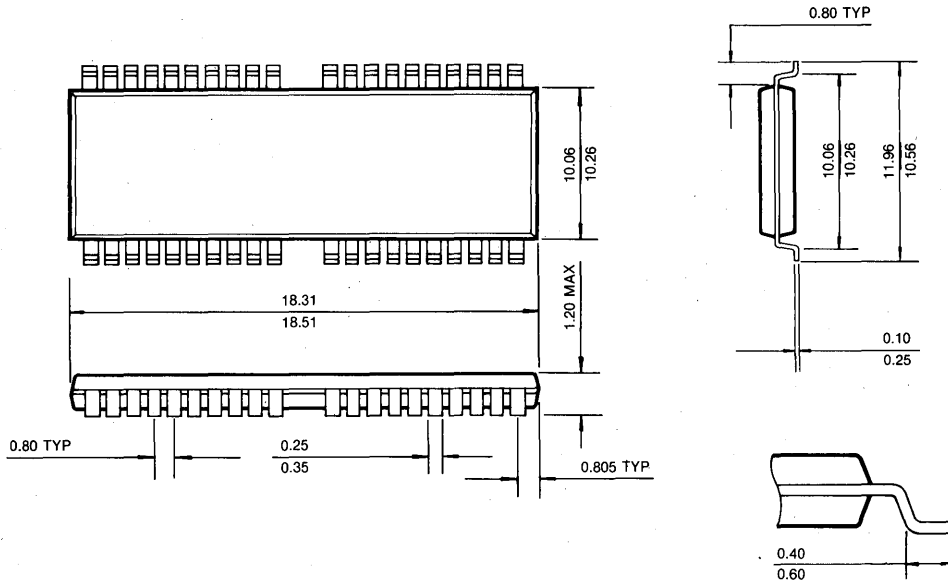
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- Performance range:

	trAC	tcAC	trC	tHPC
KM416C254B/BL/BLL-5	50ns	17ns	90ns	20ns
KM416C254B/BL/BLL-6	60ns	17ns	110ns	24ns
KM416C254B/BL/BLL-7	70ns	20ns	130ns	29ns

- Fast Page Mode with Extended Data Out
- Byte word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Self Refresh operation (LL-ver)
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +5V ± 10% power supply
- Refresh Cycle
 - 512 cycle/8ms (Normal)
 - 512 cycle/64ms (L-version)
 - 512 cycle/128ms (LL-version)
- Power Dissipation
 - Standby : 5.5mW(Normal)
 - 1.1mW(L-version)
 - 0.83mW(LL-version)
- Active (50/60/70) : 605/495/440 mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

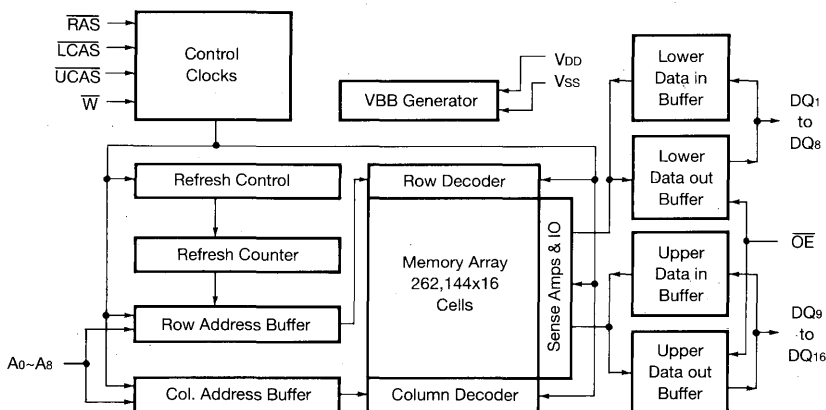
GENERAL DESCRIPTION

The Samsung KM416C254B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416C254B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

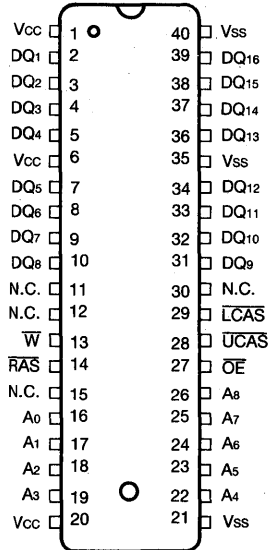
The KM416C254B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

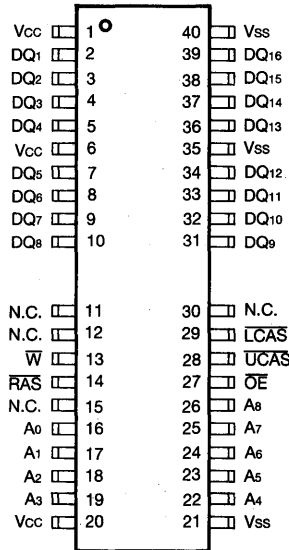


PIN CONFIGURATION (Top Views)

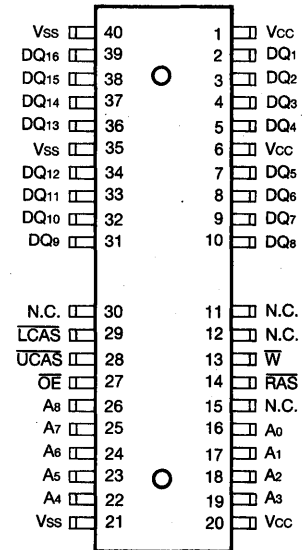
• KM416C254BJ/BLJ/BLLJ



• KM416C254BT/BLT/BLLT



• KM416C254BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1~+7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1~+7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (R _{AS} , C _{AS} , Address Cycling @trc=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I _{CC1}	-	110 90 80 mA
Standby Current (R _{AS} =UCAS=LCAS=W=V _{IH})		I _{CC2}	-	2 mA
R _{AS} -Only Refresh Current* (UCAS=LCAS=V _{IH} , R _{AS} , Address Cycling @trc=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I _{CC3}	-	110 90 80 mA
Hyper page Mode Current* (R _{AS} =V _{IL} , UCAS=LCAS, Address Cycling @trc=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I _{CC4}	-	70 60 55 mA
Standby Current (R _{AS} =UCAS=LCAS=W=V _{CC} -0.2V)	KM416C254B KM416C254BL KM416C254BLL	I _{CC5}	-	1 200 150 mA μA μA
C _{AS} -Before-R _{AS} Refresh Current* (R _{AS} and UCAS=LCAS Cycling @trc=min.)	KM416C254B/BL/BLL-5 KM416C254B/BL/BLL-6 KM416C254B/BL/BLL-7	I _{CC6}	-	110 90 80 mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V UCAS=LCAS= 0.2V DIN=Don't Care, TRC=125μS TRAS=TRAS min.~300ns	KM416C254BL	I _{CC7}	-	300 μA
Self Refresh Current R _{AS} =UCAS=LCAS=0.2V W=OE=A0-A8=V _{CC} -0.2V or 0.2V DQ1-DQ16=V _{CC} -0.2V, 0.2V or Open	KM416C254BLL	I _{CC8}	-	200 μA

4

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ -A ₈)	C _{IN1}	-	5	pF
Input Capacitance (RAS, UCAS, LCAS, W, OE)	C _{IN2}	-	7	pF
Input Capacitance (DQ ₁ -DQ ₁₆)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC}=5V ± 10%, See notes 1,2)

Test condition : V_{ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		ns	
Read-modify-write cycle time	t _{RWC}	135		155		185		ns	
Access time from RAS	t _{RAC}		50		60		70	ns	3,4,11
Access time from CAS	t _{CAC}		17		17		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35	ns	3,11
CAS to output in Low-Z	t _{CLZ}	3		3		3		ns	3
Turn-off delay from CAS	t _{CEZ}	3	13	3	15	3	20	ns	7,14
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	2
RAS precharge time	t _{RP}	30		40		50		ns	
RAS pulse width	t _{RAS}	50	10,000	60	10,000	70	10,000	ns	
RAS hold time	t _{RSH}	17		17		20		ns	
CAS hold time	t _{CSH}	40		50		60		ns	
CAS pulse width	t _{CAS}	8	10,000	10	10,000	15	10,000	ns	12
RAS to CAS delay time	t _{RCD}	20	37	20	45	20	50	ns	4
RAS to column address delay time	t _{RAD}	15	25	15	30	15	35	ns	11
CAS to RAS precharge time	t _{CRP}	5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	

(*) -50ns Product : Output Loading (C_L)=50pF, V_{CC}=5V ± 5%



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	8		10		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		ns	6
Column address to $\overline{\text{RAS}}$ lead time	trAL	25		30		35		ns	
Read command set-up time	trCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command hold time	twCH	10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	40		45		50		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	13		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	8		10		15		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		10		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tdHR	40		45		55		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh Period(LL-version)	tREF		128		128		128	ms	
Write command set-up time	twCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	40		42		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	73		85		95		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		60		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tcPWD	53		60		65		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B-R counter test cycle)	tcPT	20		20		25		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		30		35		40	ns	3
Hyper Page mode cycle time	tHPC	20		24		29		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	62		71		81		ns	12
$\overline{\text{CAS}}$ precharge time (Hyper Page mode)	tcP	8		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page mode)	trASP	50	100K	60	100K	70	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	30		35		40		ns	
$\overline{\text{OE}}$ access time	toEA		15		15		20	ns	
$\overline{\text{OE}}$ to Output in Low-z	tolZ	3		3		3		ns	
$\overline{\text{OE}}$ to data delay	toED	13		15		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toEZ	3	13	3	15	3	20	ns	7

(*) -50ns Product : Output Loading (CL)=50pF, Vcc=5V ± 5%

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} command hold time	toEH	13		15		20		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	tREZ	3	13	3	15	3	20	ns	7,14
Output buffer turn off delay from \overline{W}	tWEZ	3	13	3	15	3	20	ns	7
\overline{W} to data delay	twED	13		15		20		ns	
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		ns	
\overline{RAS} pulse width(LL-ver)	trASS	100		100		100		μ s	13
\overline{RAS} precharge time (LL-ver)	trPS	90		110		130		ns	13
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		ns	13

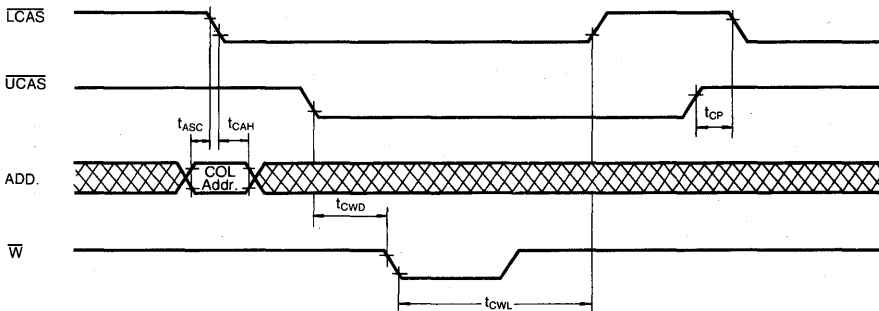
(*) -50ns Product : Output Loading (CL)=50pF, Vcc=5V \pm 5%

KM416C254B/BL/BLL Truth Table

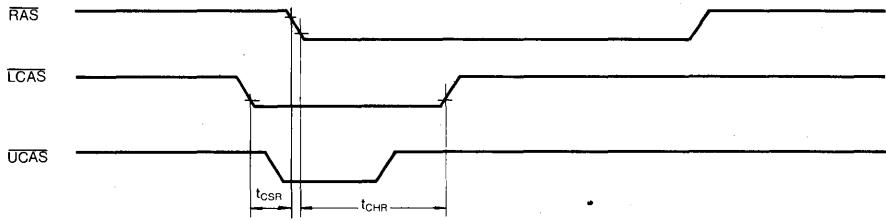
RAS	LCAS	UCAS	W	OE	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

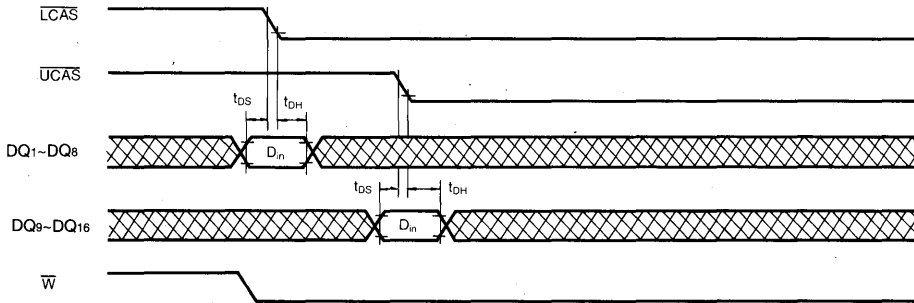
1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs except t_{HPC} and t_{HPRWC} .
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. $t_{ASC} \geq t_{CP} \min$, Assume $t_T=2.0$ ns
13. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (LL-Ver)
14. If \overline{RAS} goes high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
15. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
16. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
17. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.



19. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
20. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low



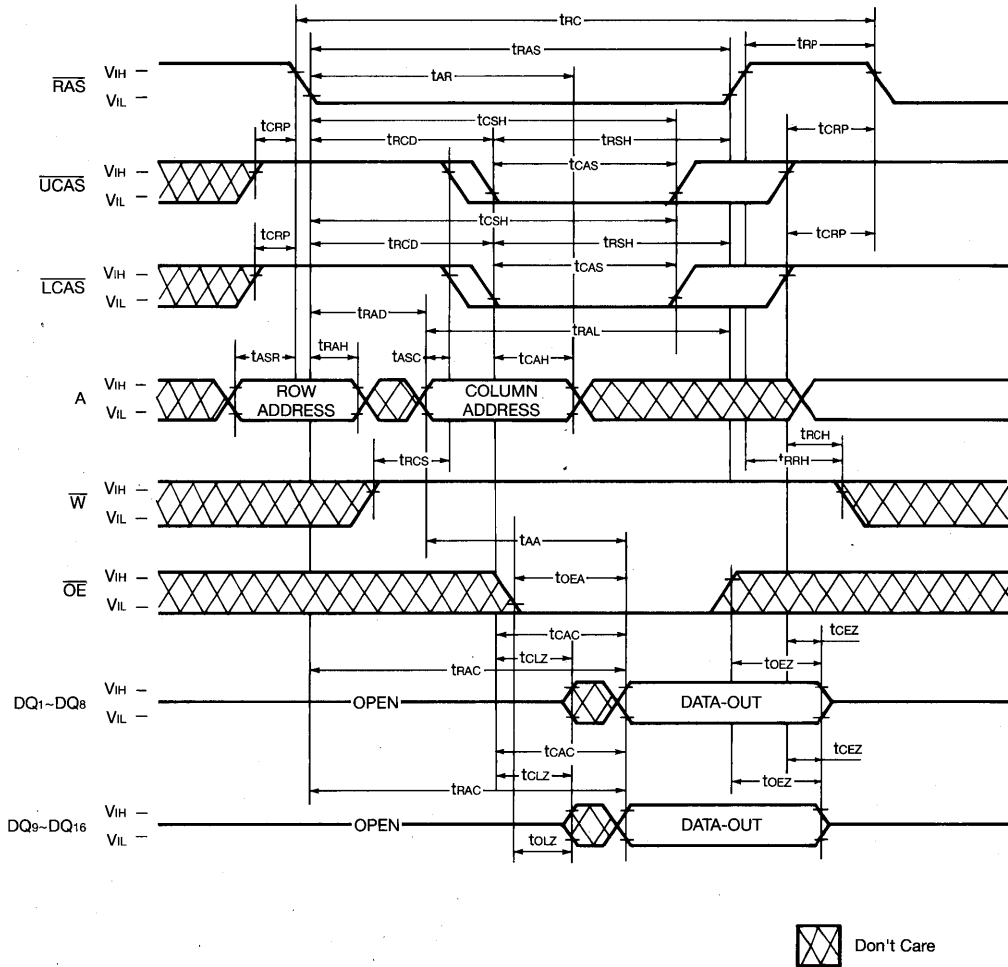
21. t_{DS} , t_{DH} , is independently specified for lower byte $D_{IN(1-8)}$, upper byte $D_{IN(9-16)}$.



TIMING DIAGRAM

WORD READ CYCLE

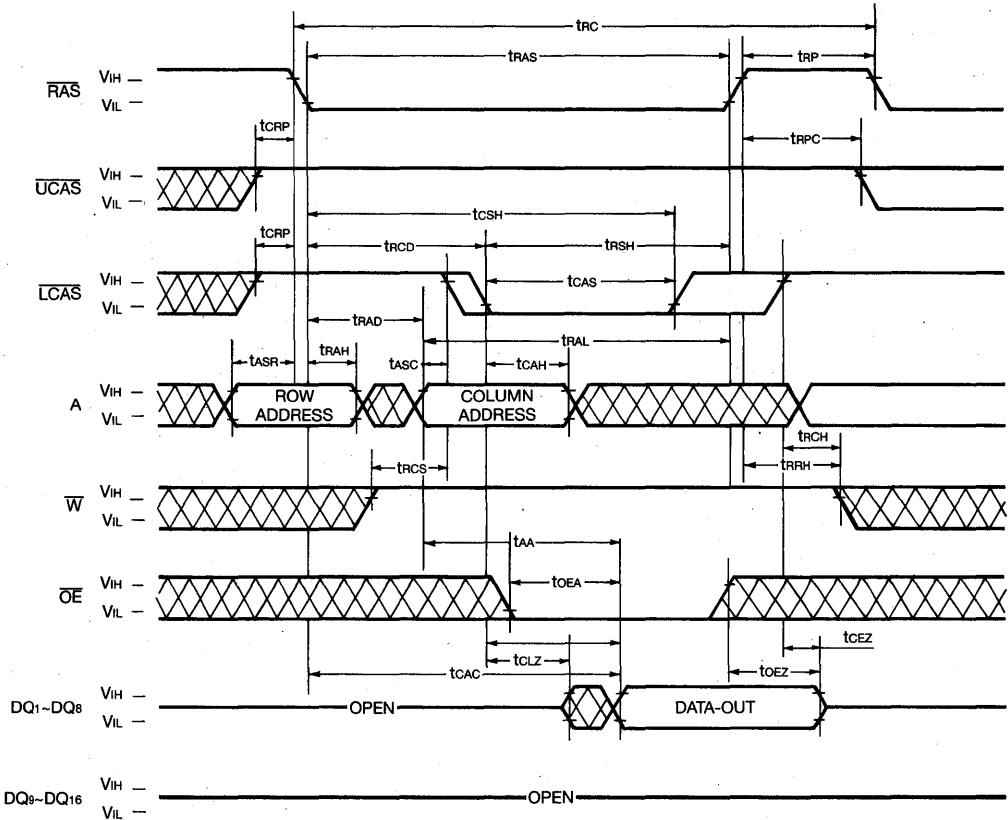
NOTE : DIN=OPEN



TIMING DIAGRAM

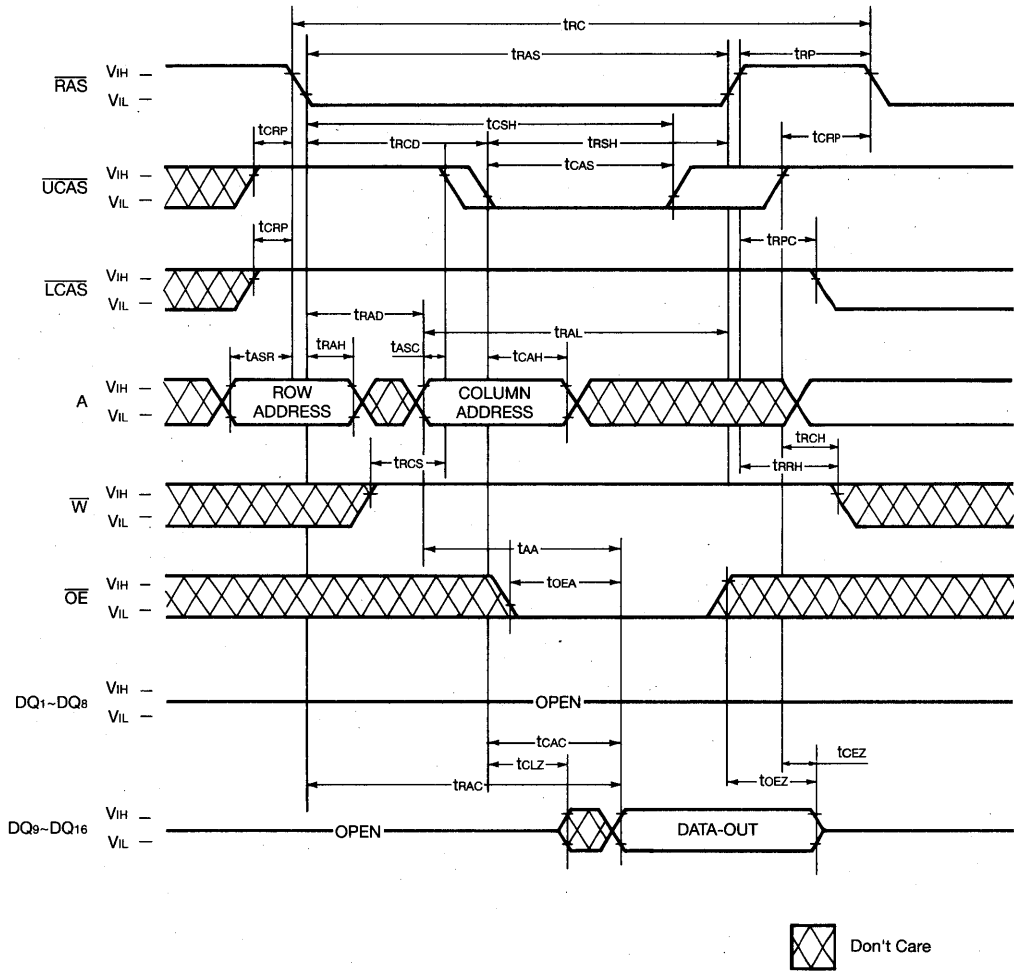
LOWER BYTE READ CYCLE

NOTE : D_{in}=OPEN



UPPER BYTE READ CYCLE

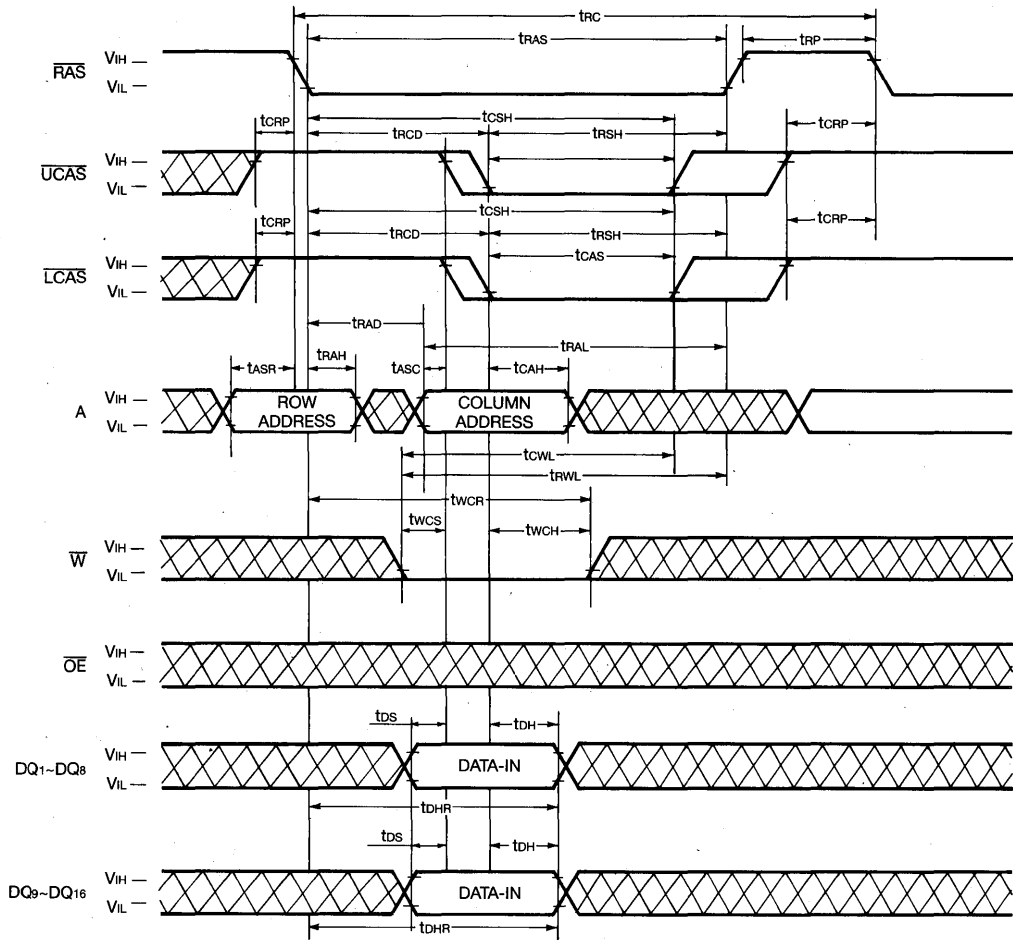
NOTE : DIN=OPEN



4

WORD WRITE CYCLE (EARLY WRITE)

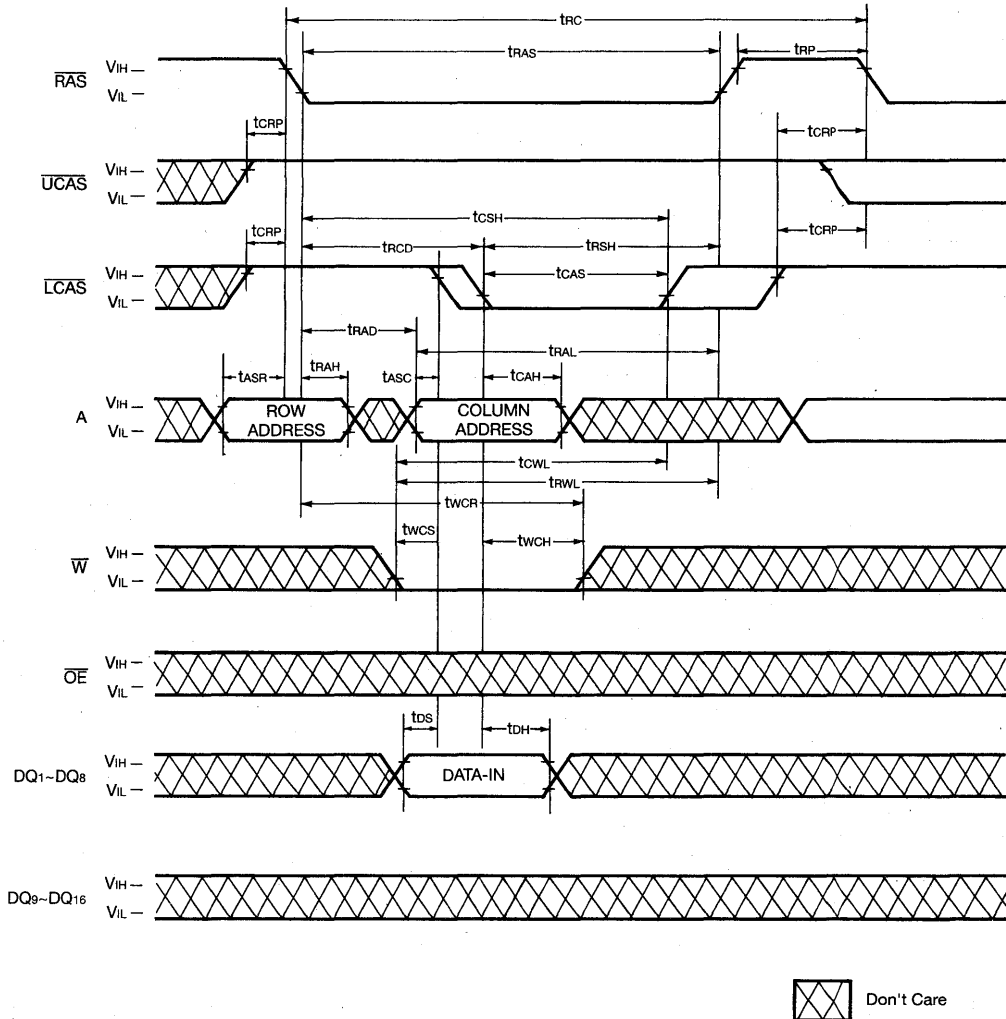
NOTE : Dout=OPEN



 Don't Care

LOWER BYTE WRITE CYCLE (EARLY WRITE)

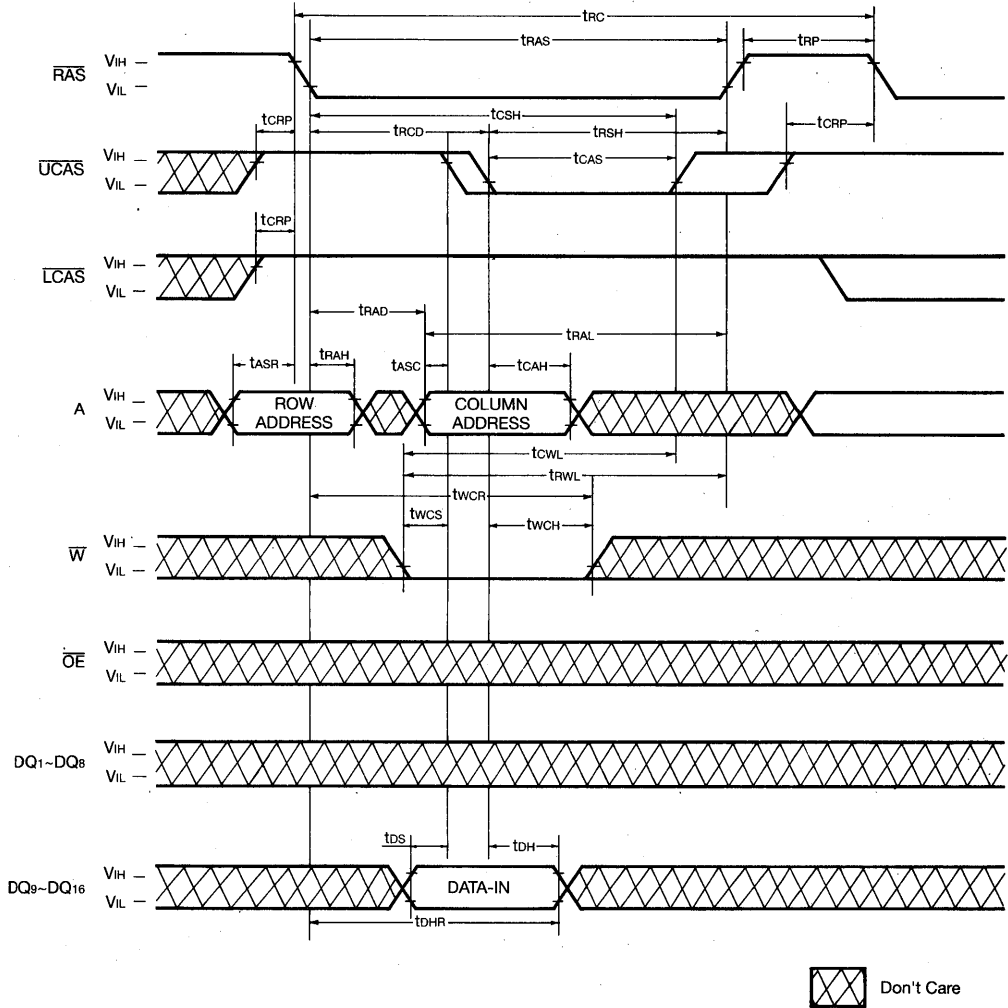
NOTE : DOUT=OPEN



4

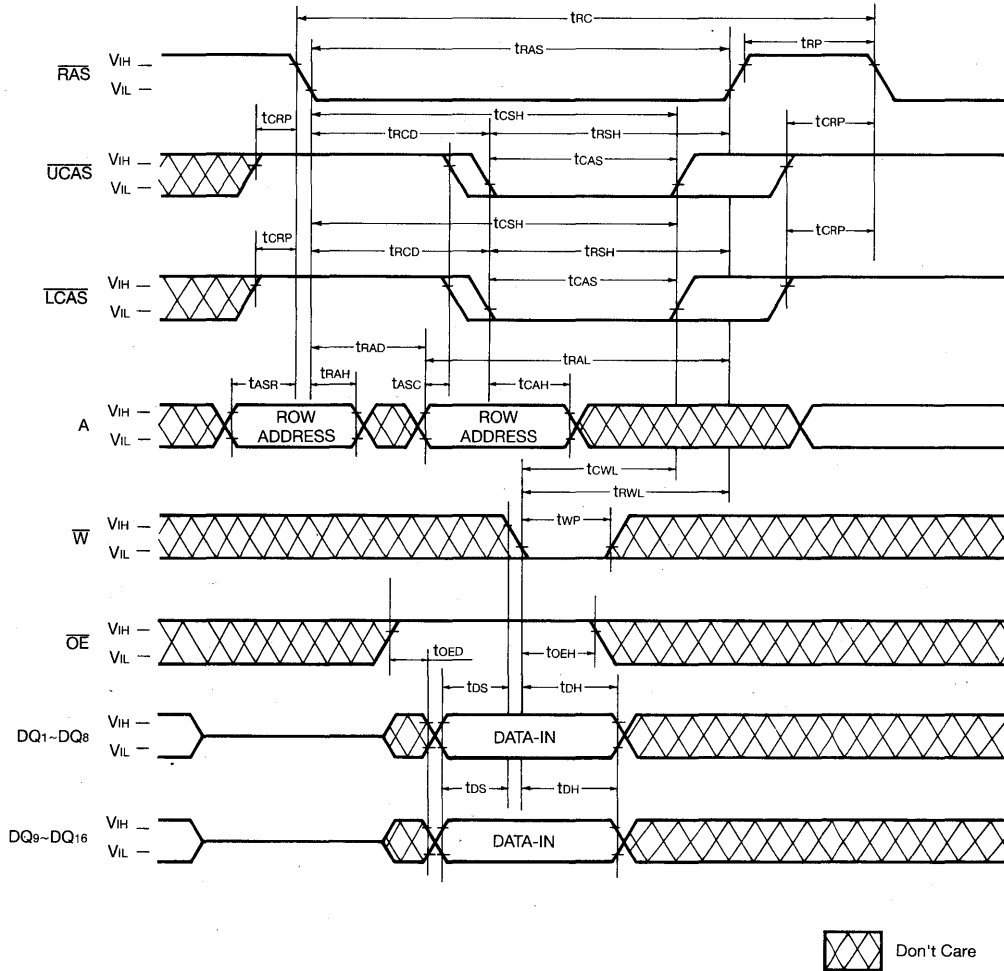
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



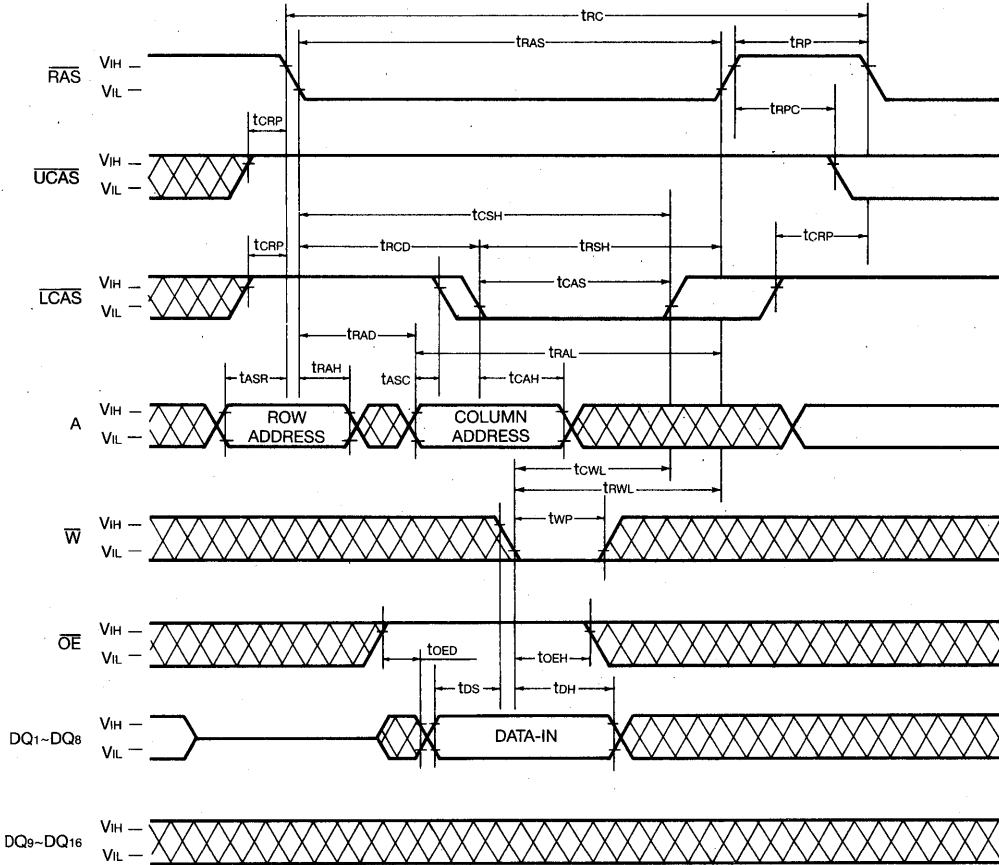
WORD WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : Dout=OPEN



LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

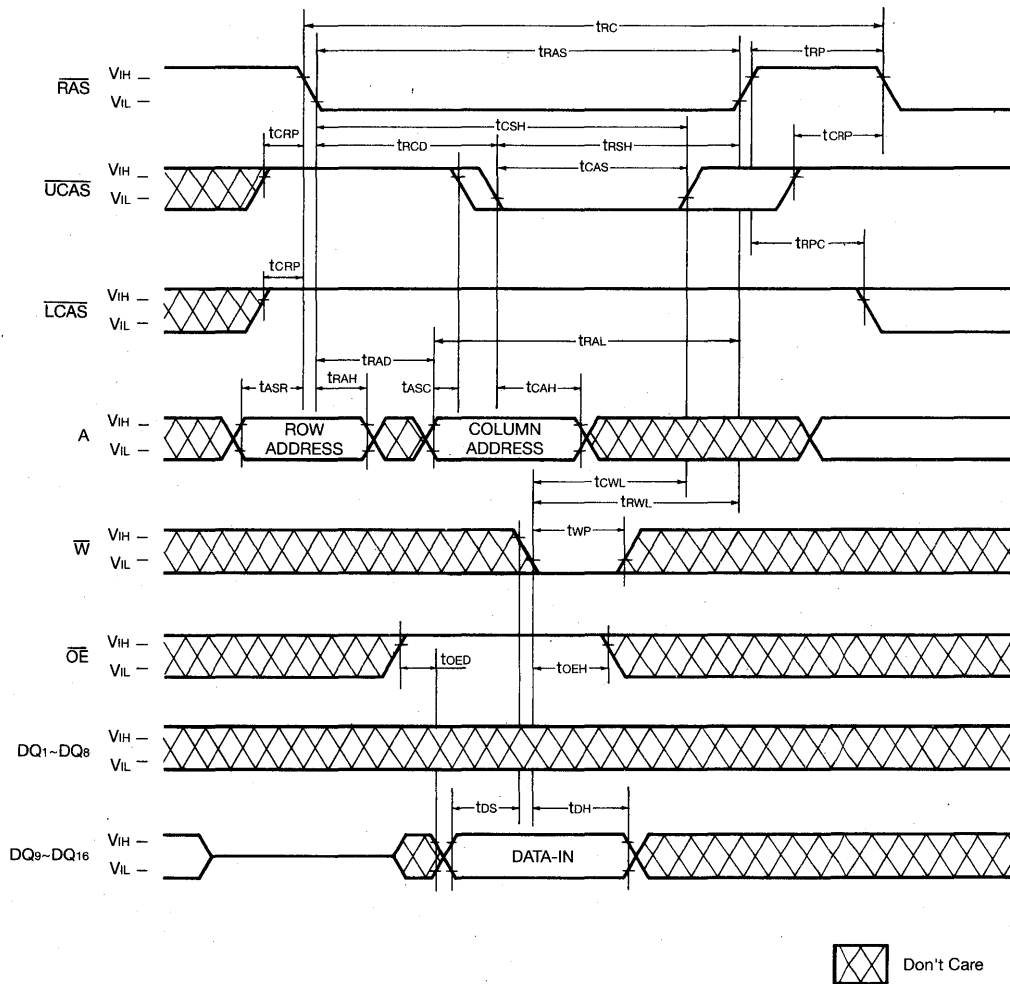
NOTE : DOUT=OPEN



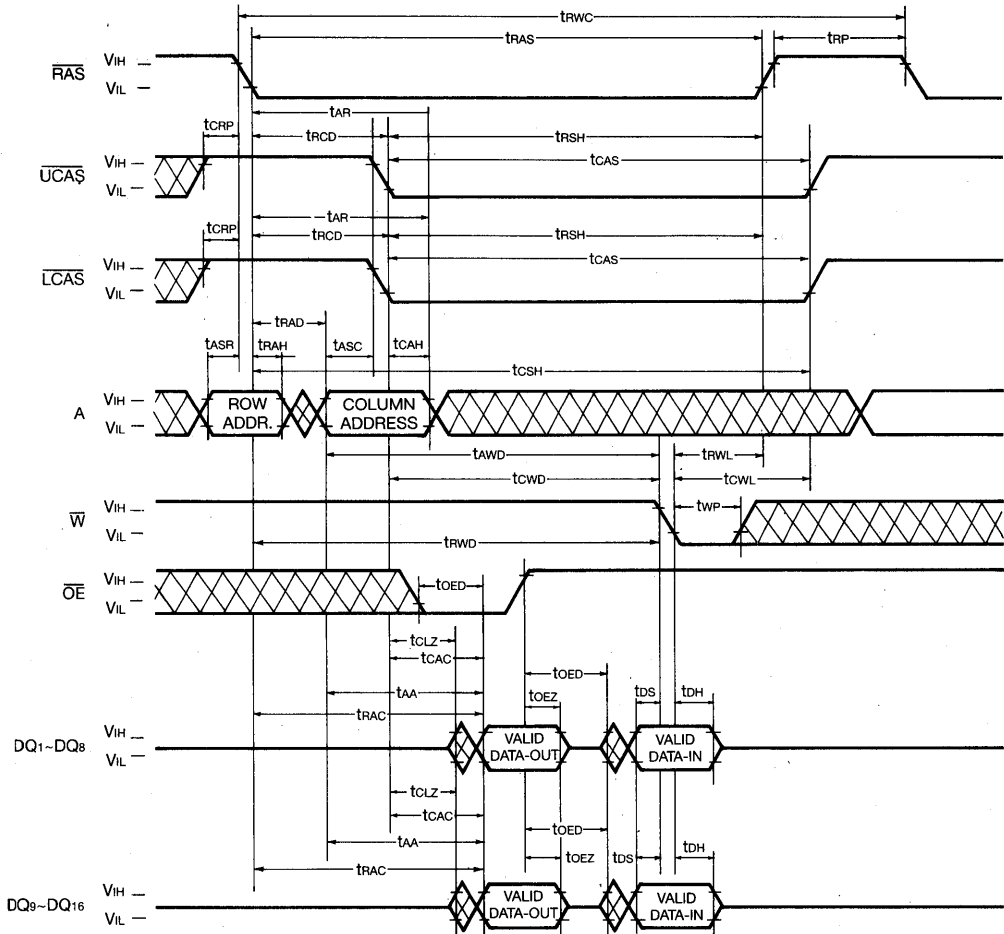
 Don't Care

UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT=OPEN

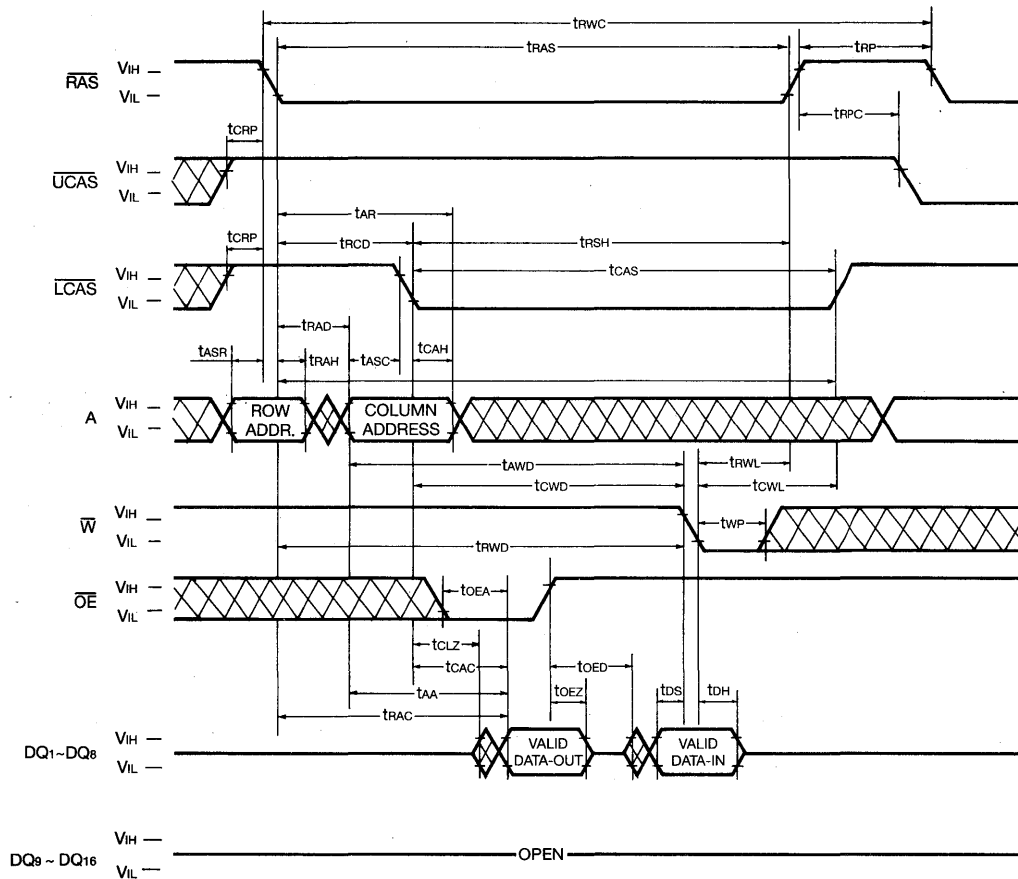


WORD READ-MODIFY-WRITE CYCLE



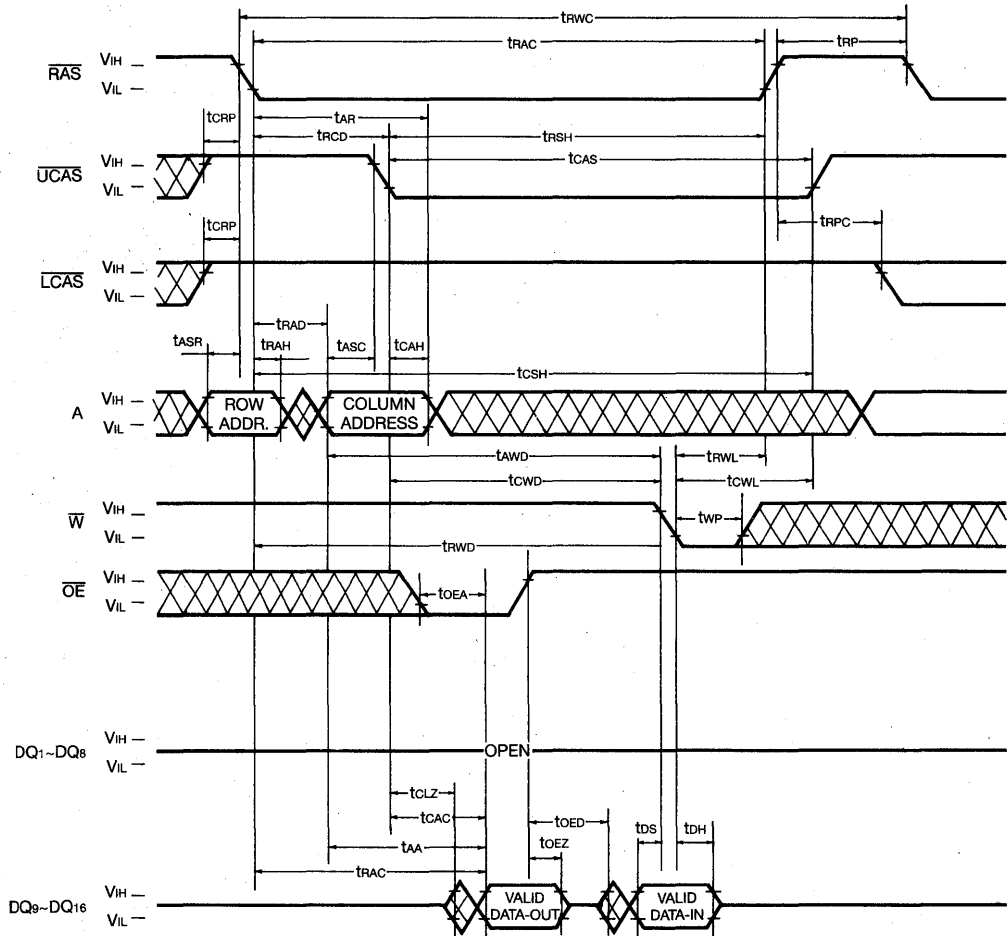
 Don't Care

LOWER-BYTE READ-MODIFY-WRITE CYCLE



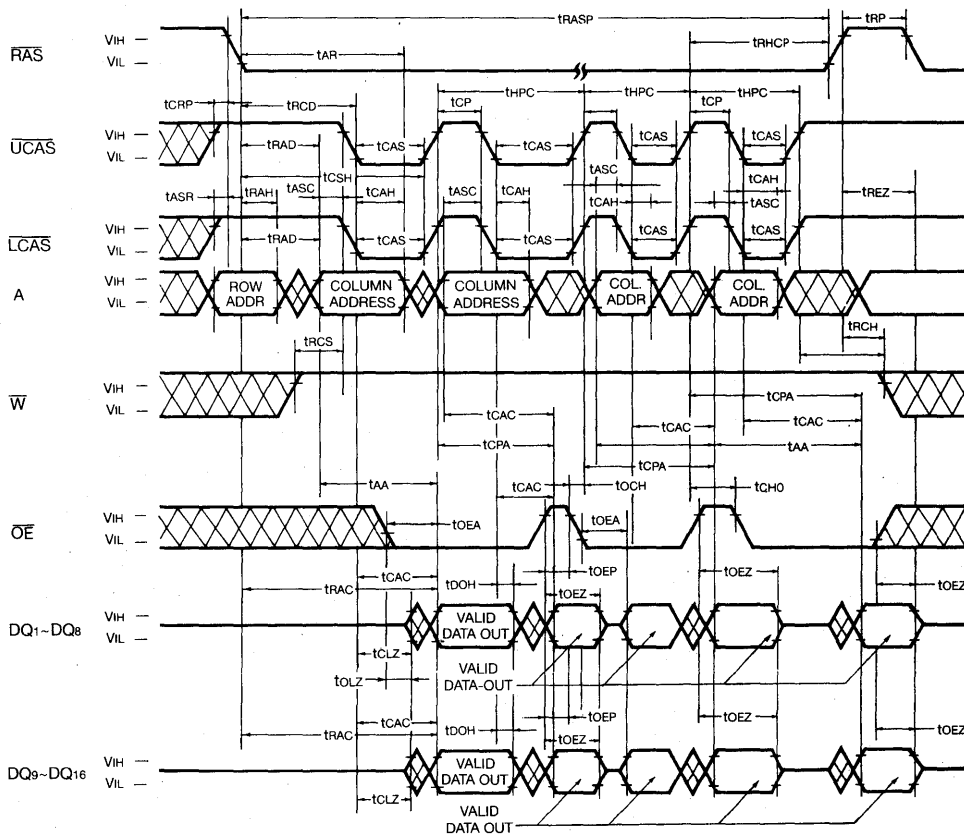
4

UPPER-BYTE READ-MODIFY-WRITE CYCLE



 Don't Care

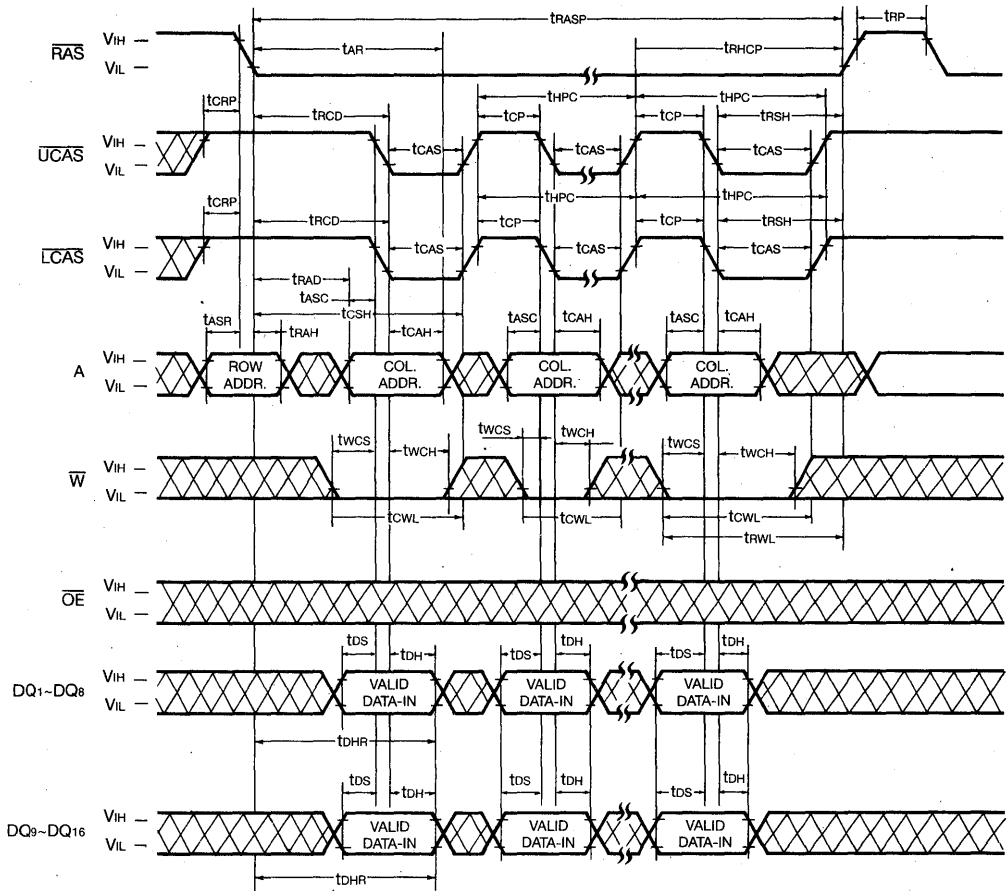
HYPER PAGE MODE WORD READ CYCLE



 Don't Care

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

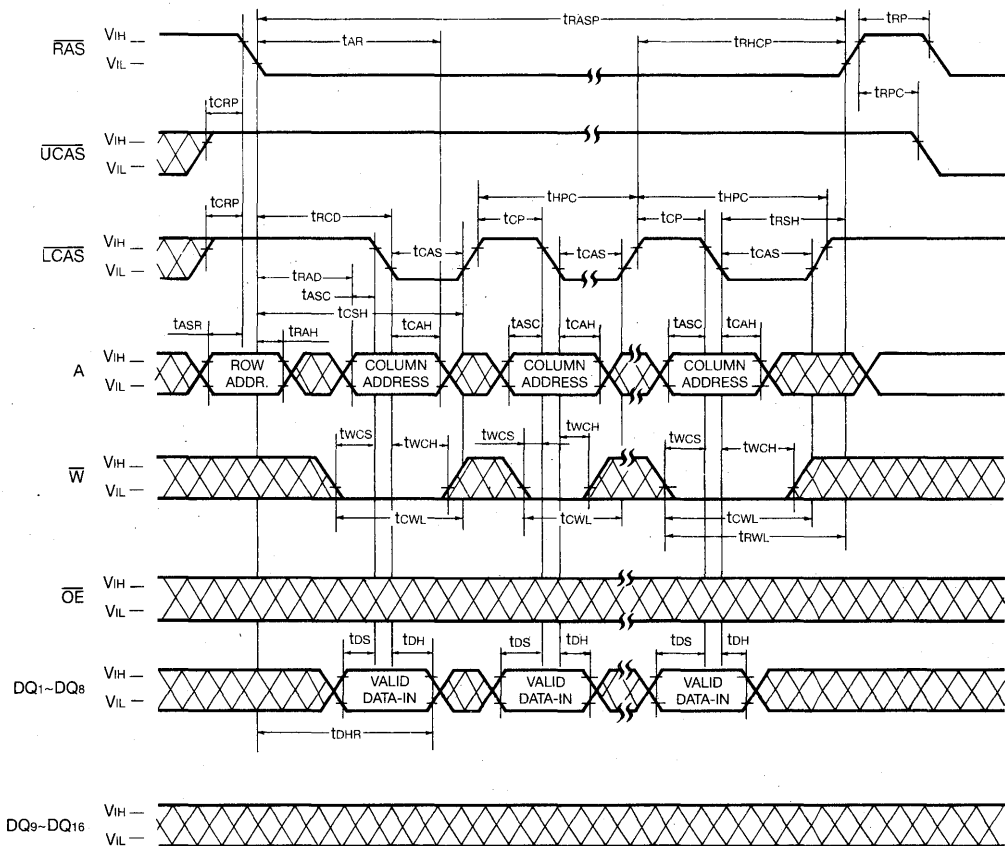
NOTE : DOUT=OPEN



 Don't Care

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : Dout=OPEN

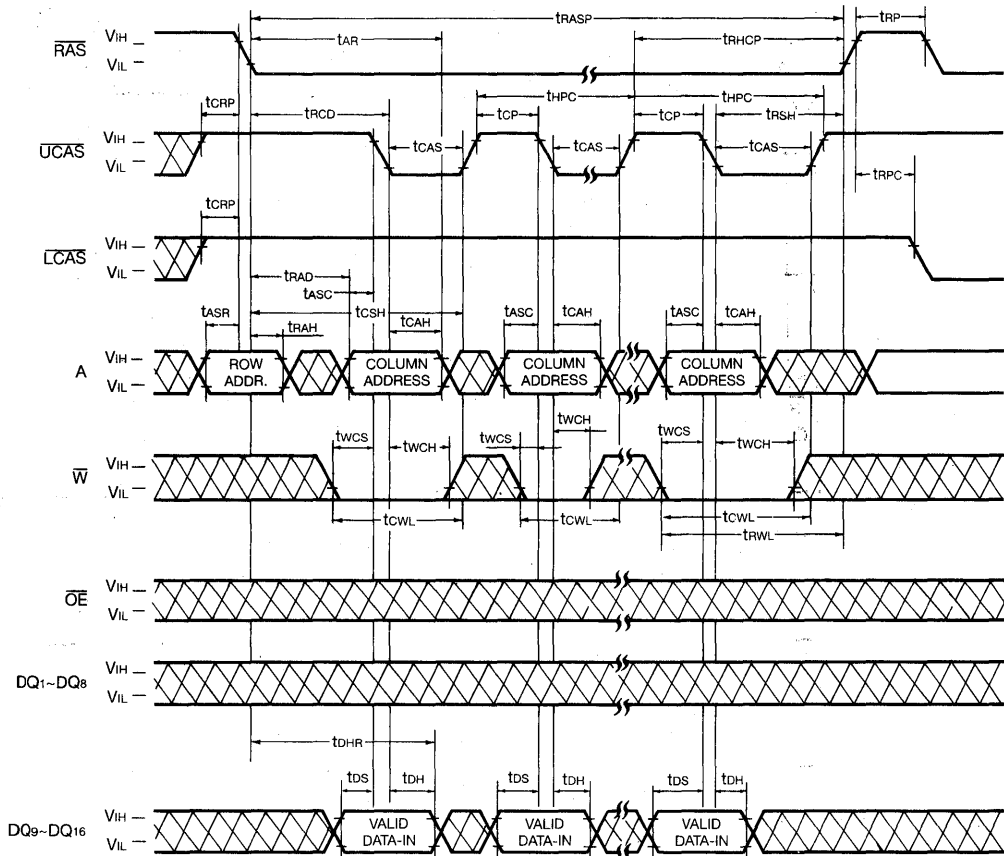


 Don't Care

4

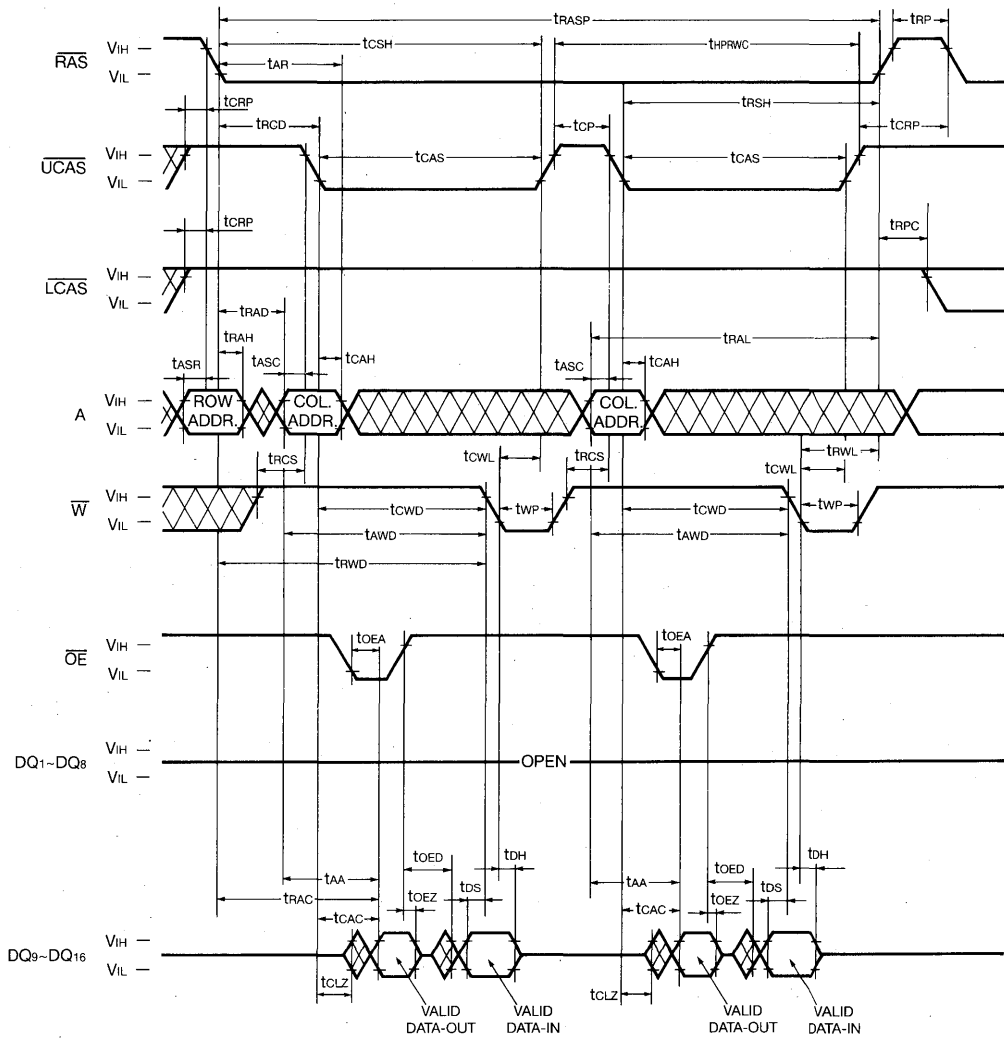
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



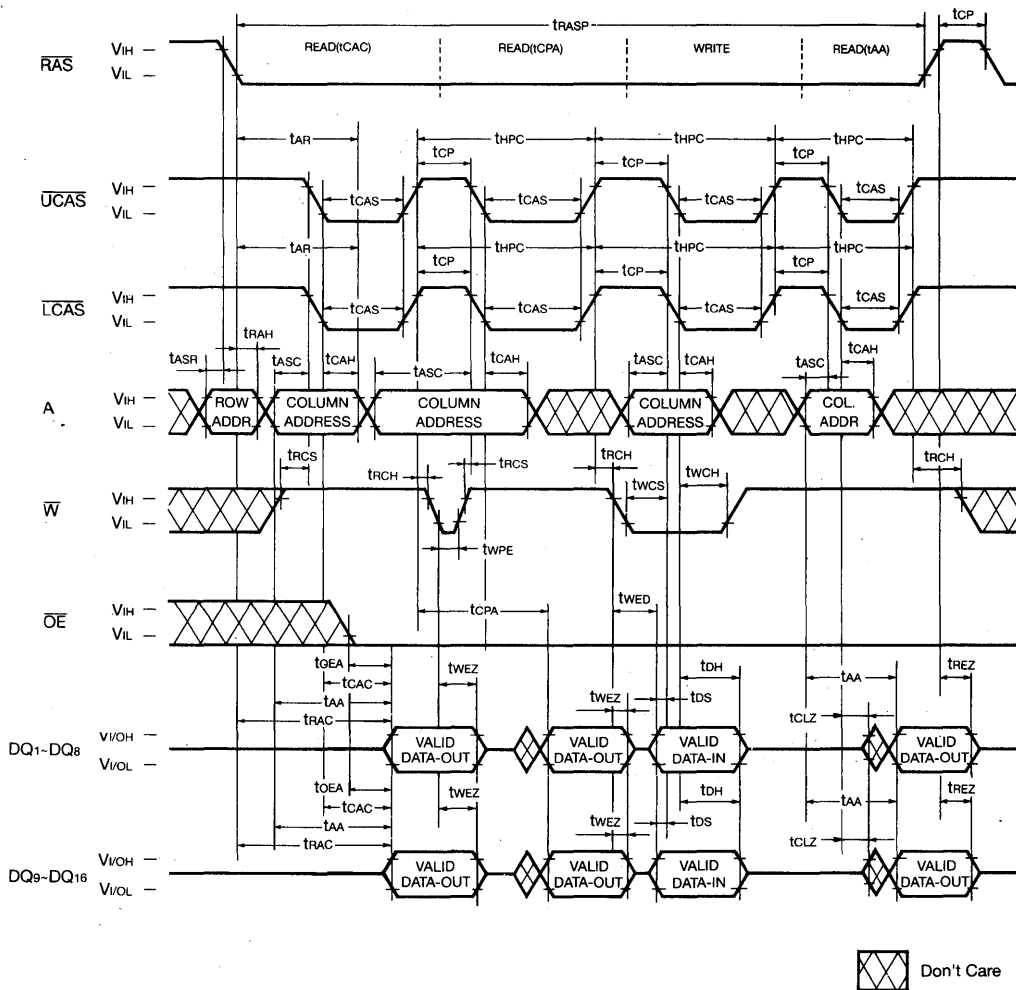
 Don't Care

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



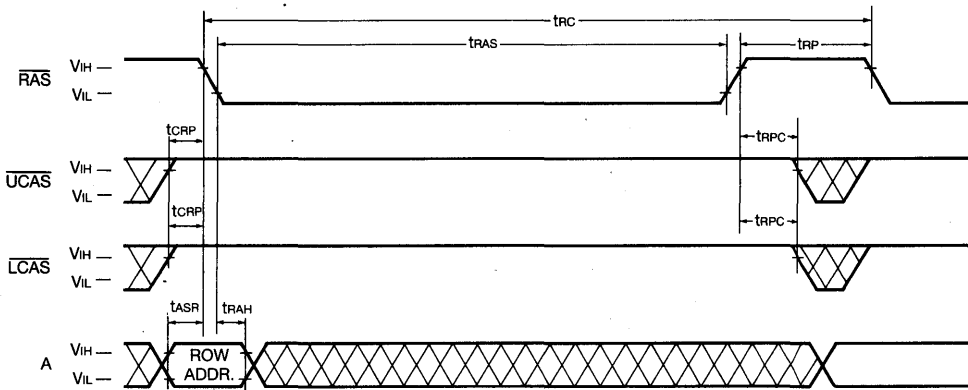
 Don't Care

HYPER PAGE READ AND WRITE MIXED CYCLE



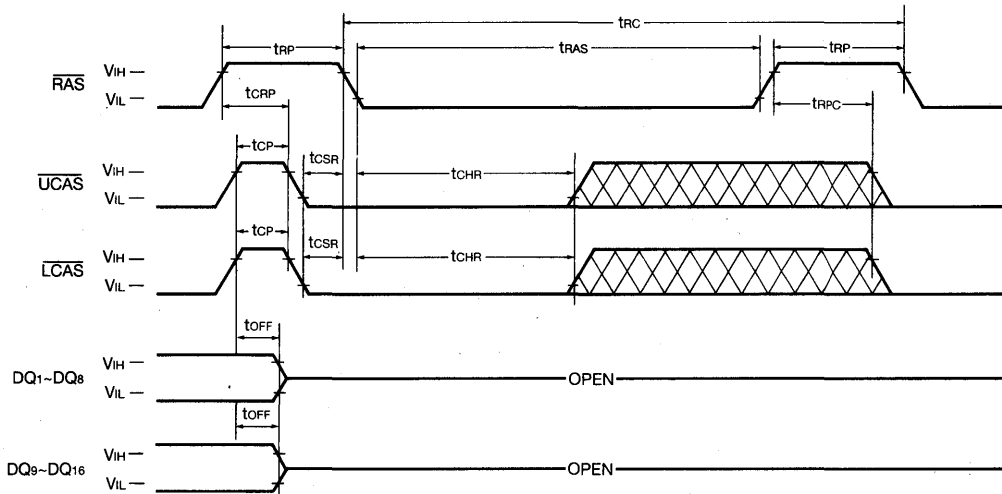
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} =Don't Care
 D_{OUT} =OPEN



CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A =Don't Care

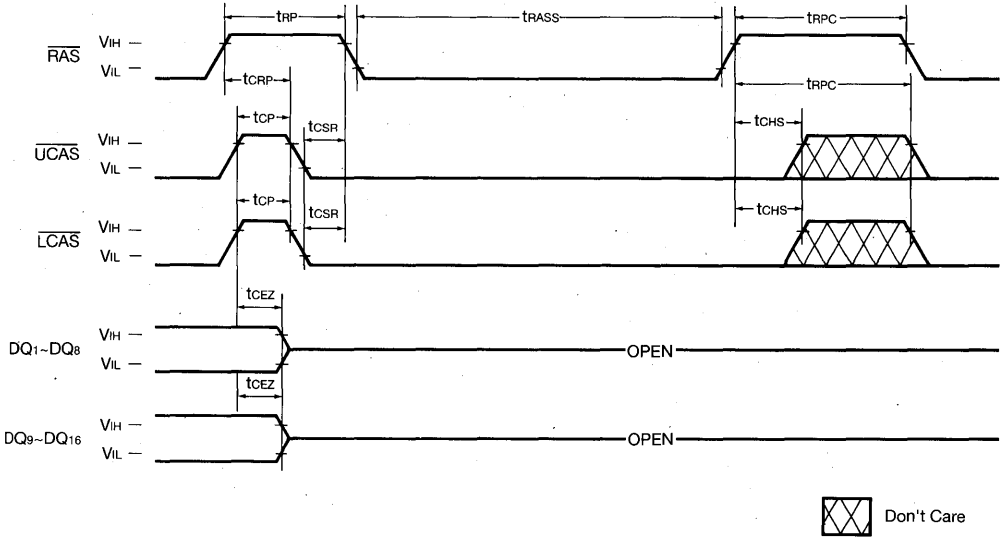


 Don't Care

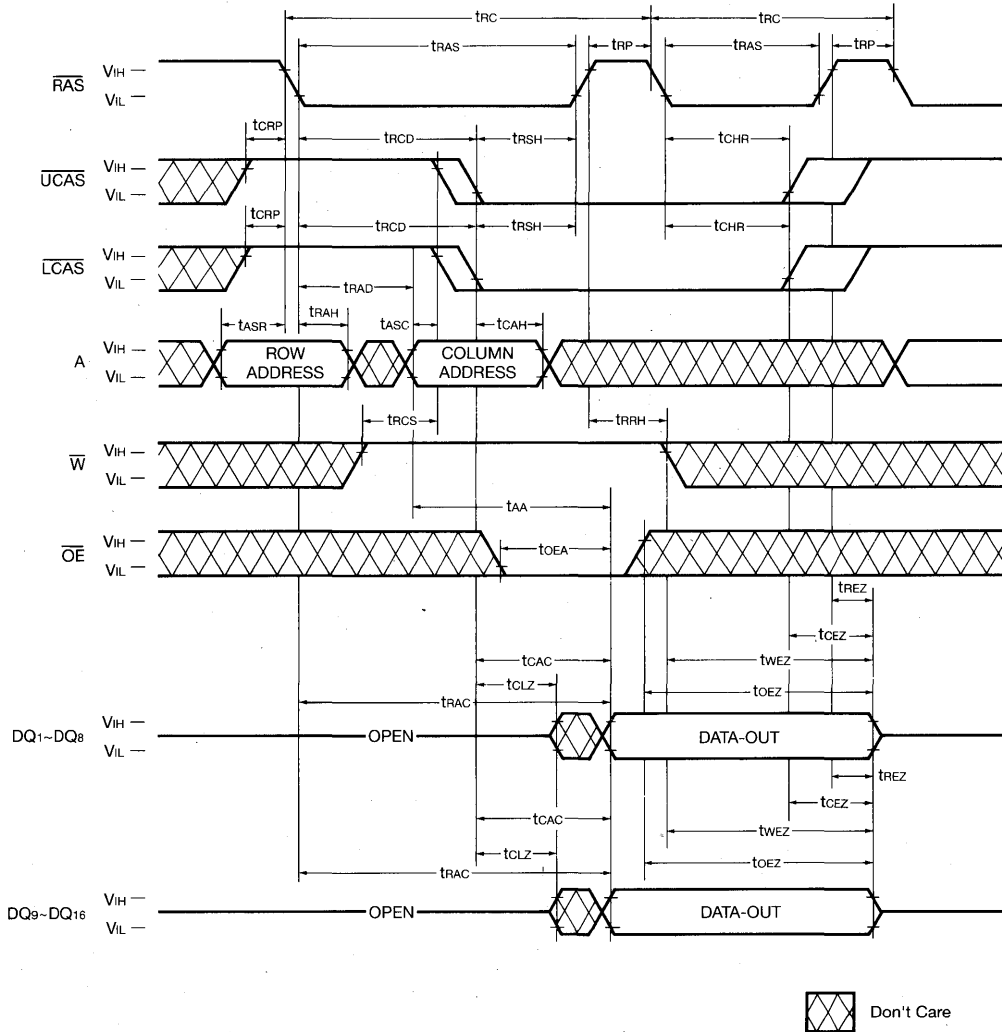
4

CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-Version)

NOTE : W, OE, A=Don't Care

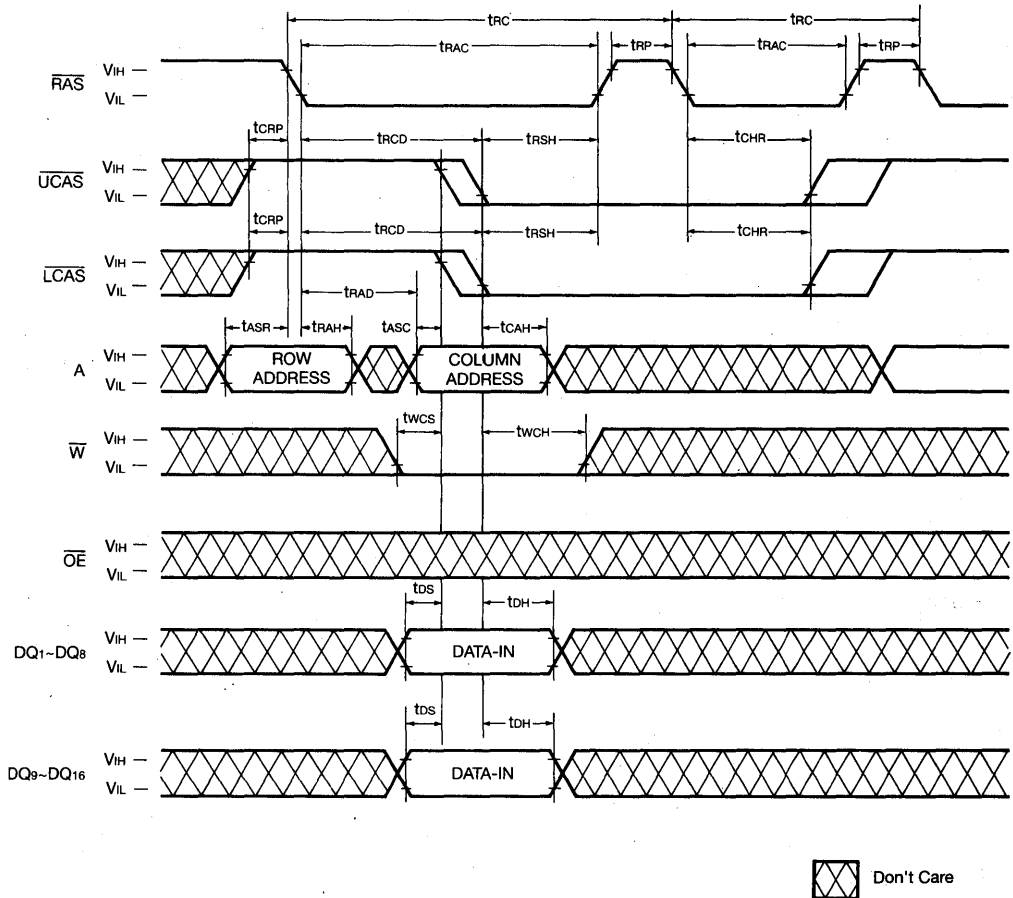


HIDDEN REFRESH CYCLE (READ)

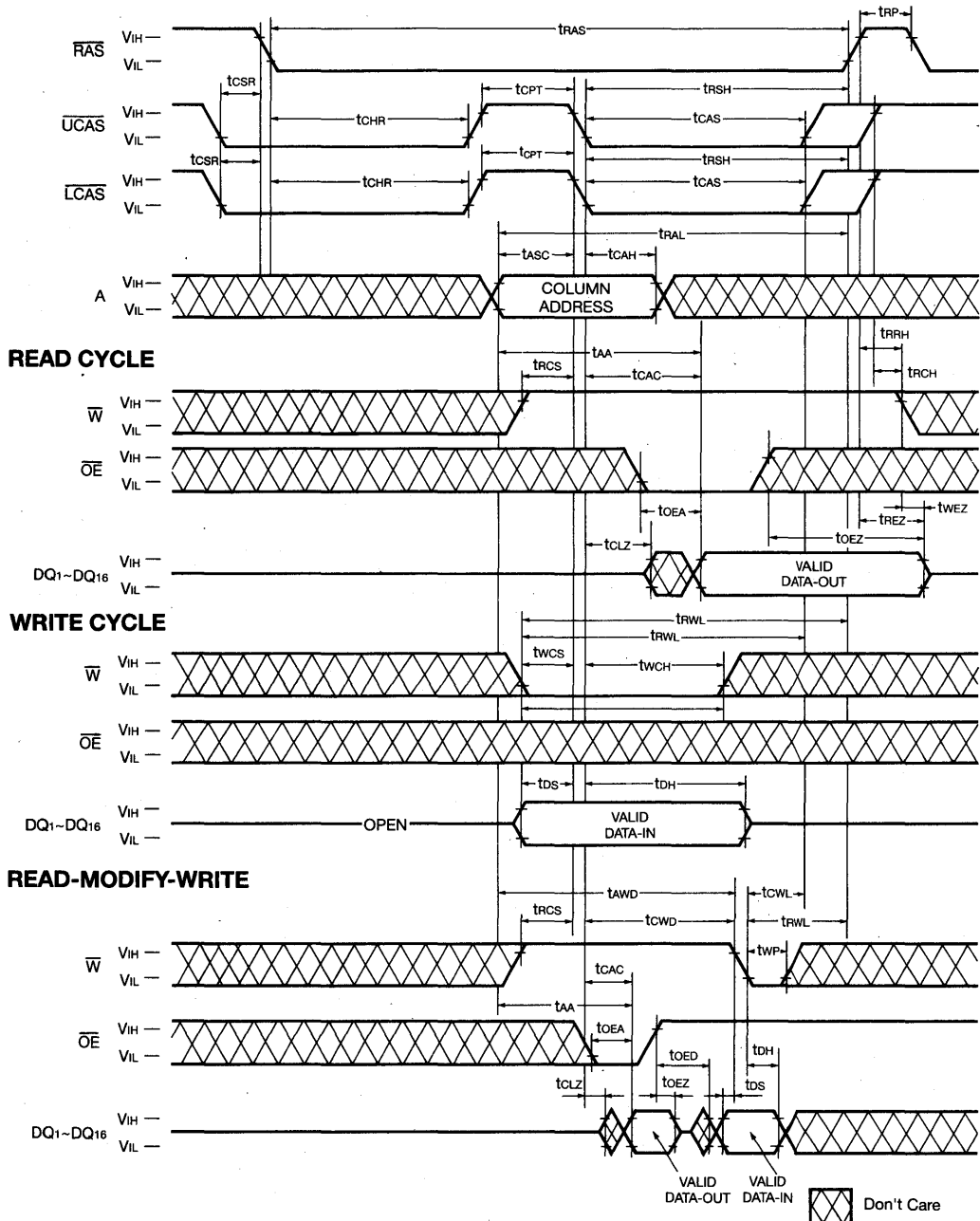


HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT=OPEN



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

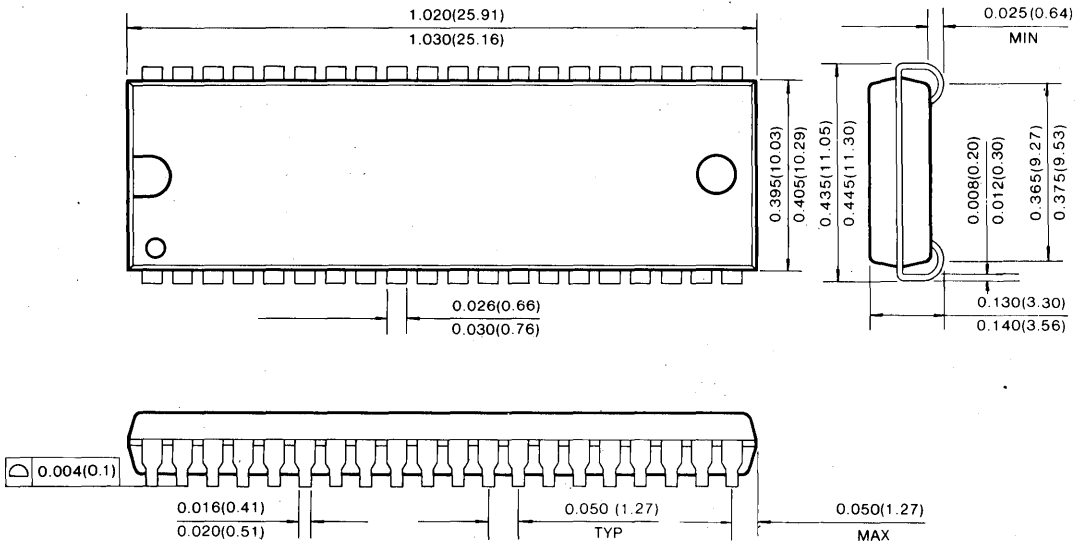


4

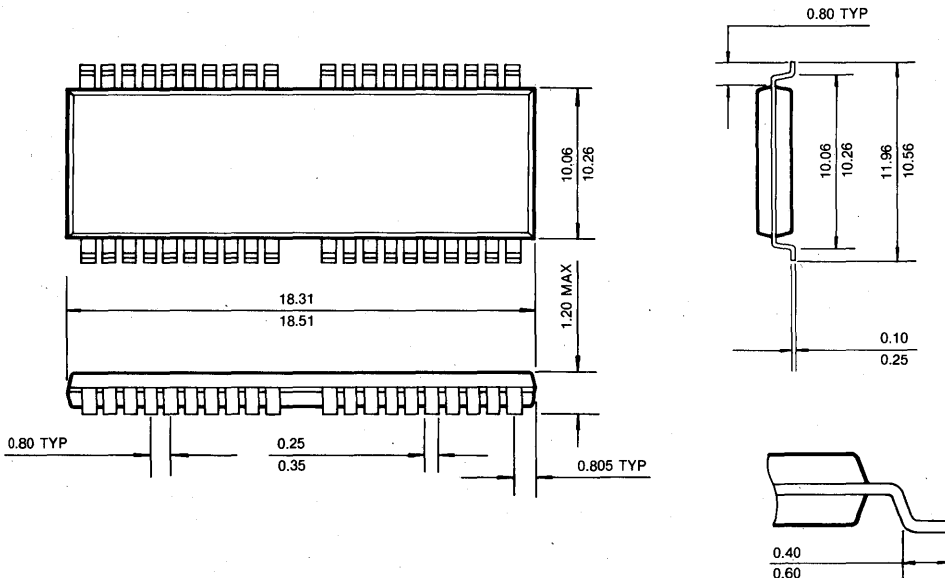
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{TRC}
KM416C156B/BL/BLL-5	50ns	15ns	90ns
KM416C156B/BL/BLL-6	60ns	15ns	110ns
KM416C156B/BL/BLL-7	70ns	20ns	130ns
KM416C156B/BL/BLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Byte Write operation (2W)
- Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Self Refresh Operation (LL-version)
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +5V ± 10% power supply
- Refresh Cycle
 - 512 cycle/8ms refresh
 - 512 cycle/64ms (L-Version)
 - 512 cycle/128ms (LL-Version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.83mW (LL-version)
 - Active (50/60/70/80): 605/495/440/415mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP (II)

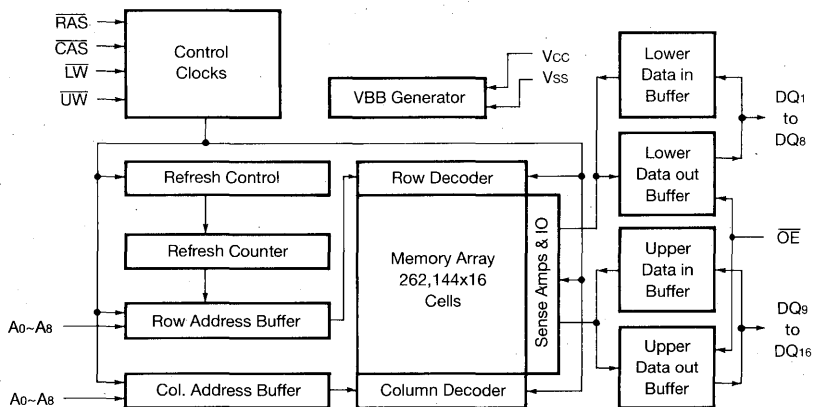
GENERAL DESCRIPTION

The Samsung KM416C156B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM416C156B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

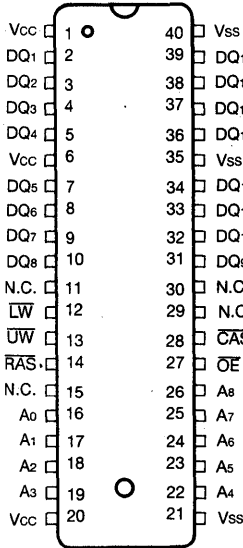
The KM416C156B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

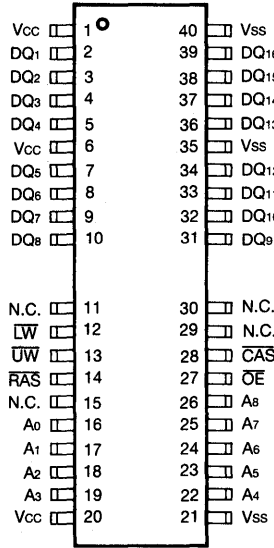


PIN CONFIGURATION (Top Views)

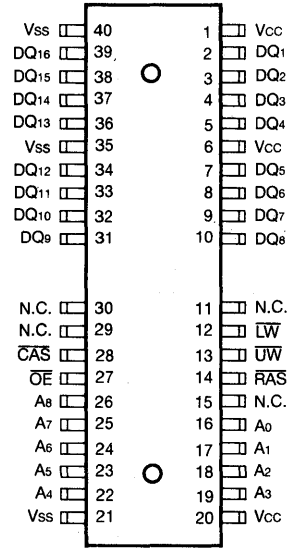
• KM416C156BJ/BLJ/BLLJ



• KM416C156BT/BLT/BLLT



• KM416C156BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A8	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
UW	Read Upper Byte Write Input
LW	Read Lower Byte Write Input
OE	Data Output Enable
Vcc	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CAS Cycling @trc=min.)	KM416C156B/BL/BLL-5	I _{CC1}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Standby Current (RAS=CAS=UW=LW=V _{IH})	I _{CC2}	-	2	mA	
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM416C156B/BL/BLL-5	I _{CC3}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tPC=min.)	KM416C156B/BL/BLL-5	I _{CC4}	-	70	mA
	KM416C156B/BL/BLL-6			60	mA
	KM416C156B/BL/BLL-7			55	mA
	KM416C156B/BL/BLL-8			50	mA
Standby Current (RAS=CAS=UW=LW=V _{CC} -0.2V)	KM416C156B	I _{CC5}	-	1	mA
	KM416C156BL			200	μA
	KM416C156BLL			150	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM416C156B/BL/BLL-5	I _{CC6}	-	110	mA
	KM416C156B/BL/BLL-6			90	mA
	KM416C156B/BL/BLL-7			80	mA
	KM416C156B/BL/BLL-8			75	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CAS=0.2V DIN=Don't Care, TRC=125μS(L-ver), TRAS=TRAS min.-300ns	KM416C156BL	I _{CC7}	-	300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}=\overline{CAS}=0.2V$ $\overline{XW}=\overline{OE}=A_0-A_8=V_{CC}-0.2V$ or $0.2V$	KM416C156BLL I _{CCS}		200	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{O(H)} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{O(L)} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₈)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{LW} , \overline{UW} , \overline{OE})	C _{IN2}	-	7	pF
Input Capacitance (DQ ₁ ~DQ ₁₆)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC}=5V ± 10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	135		155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		15		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	0		0		0		0		ns	3
Output buffer turn-off delay	t _{OFF}	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t _r	3	50	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t _{RP}	30		40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	15		15		20		20		ns	
\overline{CAS} hold time	t _{CSH}	50		60		70		80		ns	
\overline{CAS} pulse width	t _{CAS}	15	10,000	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	35	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t _{RAD}	15	25	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		0		ns	

(*) 50ns Product: V_{CC}=5V ± 5%, C_{out}=50pF

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWOR	40		45		50		55		ns	6
Write command pulse width	tWP	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		8		8		8		8	ms	
Refresh period (L-Version)	tREF		64		64		64		64	ms	
Refresh period (LL-Version)	tREF		128		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{LW}}$, $\overline{\text{UW}}$ delay time	tCWD	40		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{LW}}$, $\overline{\text{UW}}$ delay time	tRWD	75		85		95		105		ns	8
Column address to $\overline{\text{LW}}$, $\overline{\text{UW}}$ delay time	tAWD	50		55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	55		60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		80		95		100		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		15		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	15	0	20	0	20	ns	7

(*) 50ns Product:Vcc=5V ± 5%, Cout=50pF



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
\overline{OE} command hold time	tOEH	15		15		20		20		ns	
Masked write set-up time	tMCS	0		0		0		0		ns	
Masked write hold time referenced to \overline{RAS}	tMRH	0		0		0		0		ns	
Masked write hold time referenced to \overline{CAS}	tMCH	0		0		0		0		ns	
\overline{RAS} pulse width (\overline{C} - \overline{B} - \overline{R} self refresh)	tRASS	100		100		100		100		μ s	12
\overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} self refresh)	tRPS	90		110		130		150		ns	12
\overline{CAS} hold time (\overline{C} - \overline{B} - \overline{R} self refresh)	tCHS	-50		-50		-50		-50		ns	12

(*) 50ns Product: Vcc=5V \pm 5%, Cout=50pF

KM416C156B Truth Table

\overline{RAS}	\overline{CAS}	\overline{UW}	\overline{LW}	\overline{OE}	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	X	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	L	L	X	DQ-IN	DQ-IN	Word Write
L	L	H	L	X	DQ-IN	-	Byte Write
L	L	L	H	X	-	DQ-IN	Byte Write

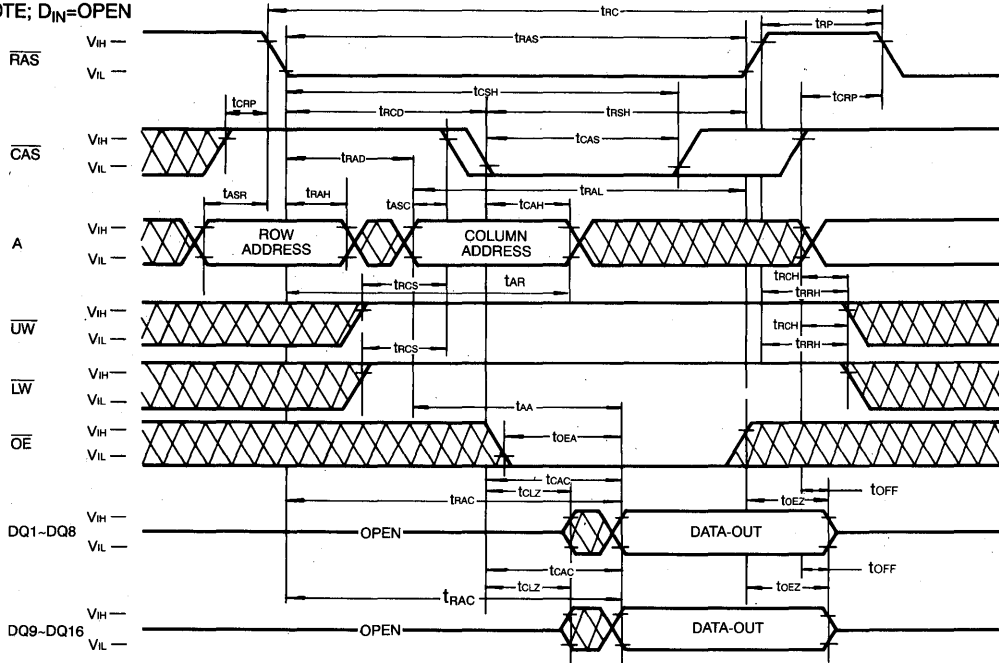
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh. In order to meet refresh specification.
13. t_{RCS} , t_{MCS} are referenced to the later \overline{W} rising edge at early write cycle.
14. t_{WCS} is referenced to the later \overline{W} falling edge at early write cycle.
15. t_{CWL} , t_{RWL} are referenced to the later \overline{W} falling edge at early write cycle.
16. t_{WCH} , t_{WP} are referenced to the earlier \overline{W} falling edge at early write cycle.
17. t_{RWD} , t_{AWD} , t_{CWD} are referenced to the earlier \overline{W} falling edge at Read-Modify-write cycle.

TIMING DIAGRAM

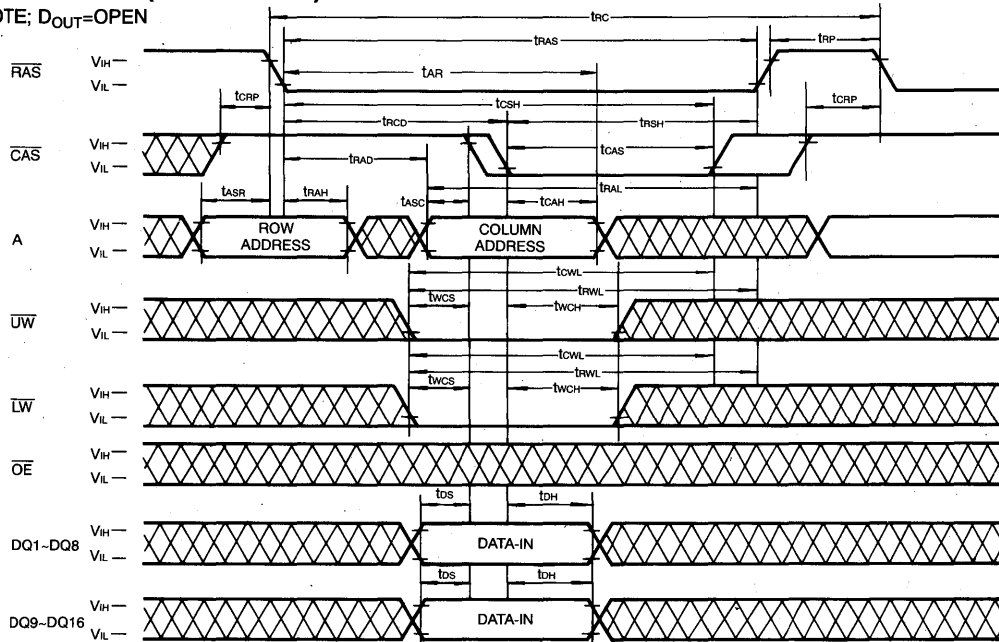
READ CYCLE


NOTE: $D_{IN} = OPEN$



WRITE CYCLE (EARLY WRITE)

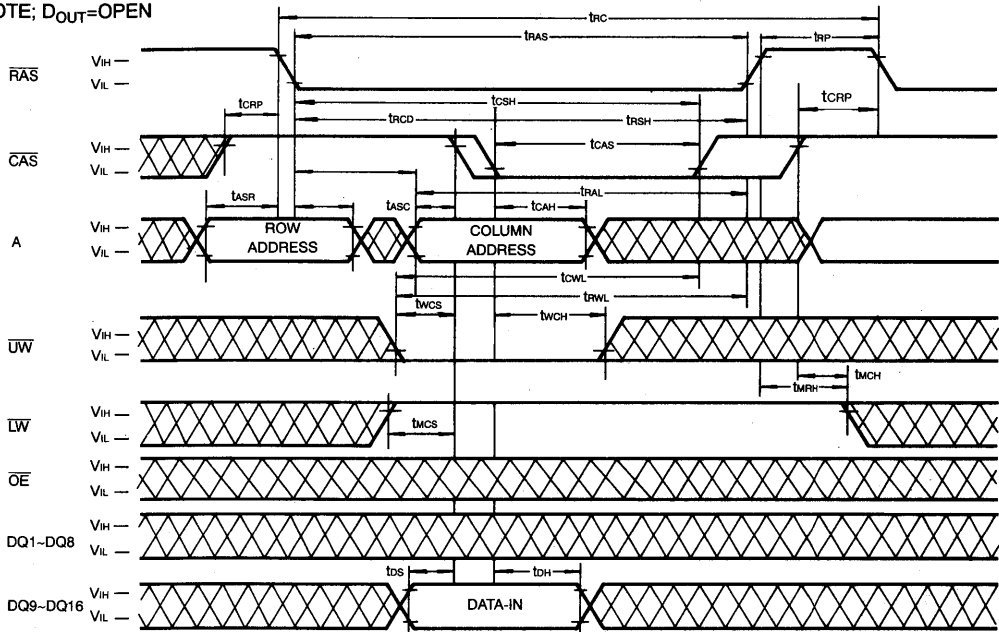
NOTE: $D_{OUT} = OPEN$



 DON'T CARE

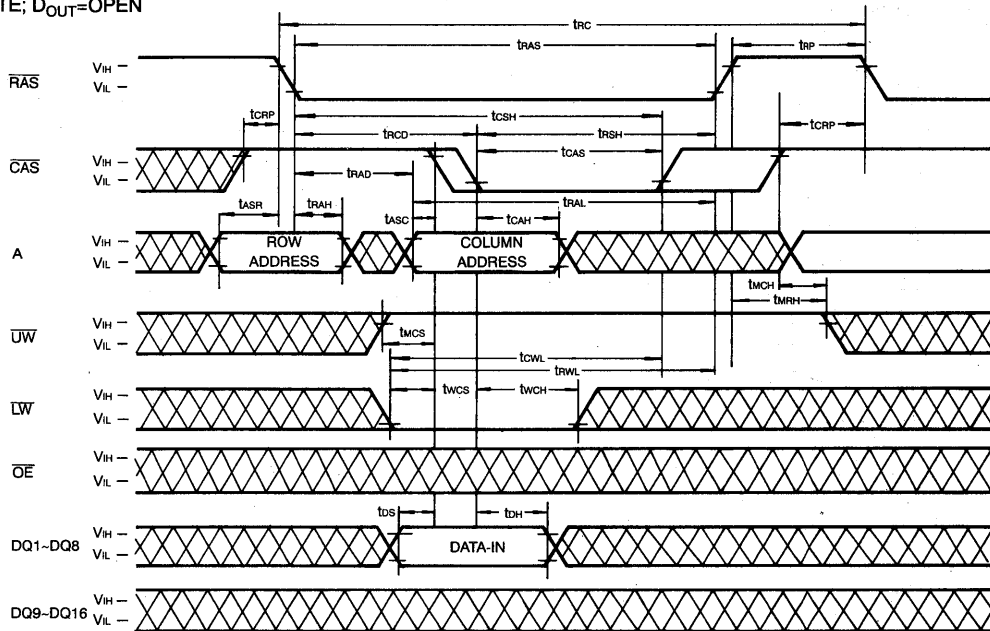
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE: D_{OUT}=OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE: D_{OUT}=OPEN

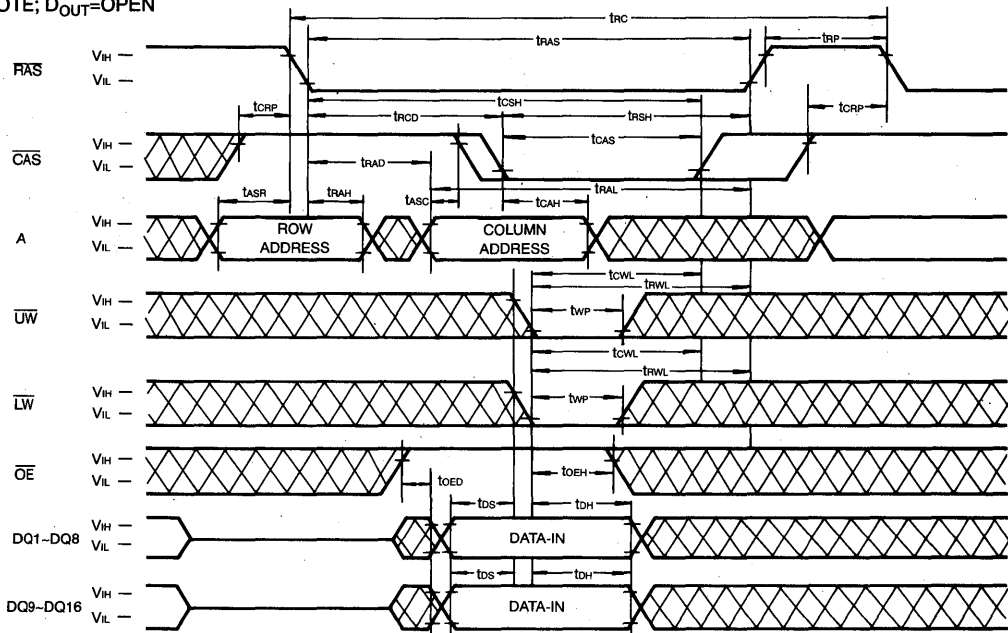


DON'T CARE

4

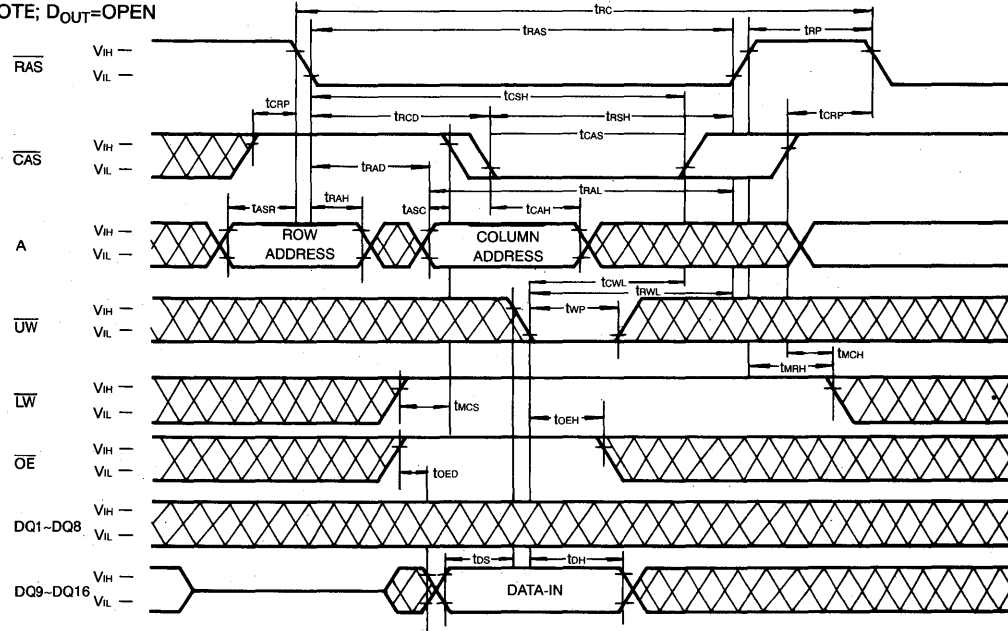
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE: D_{OUT} =OPEN



UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

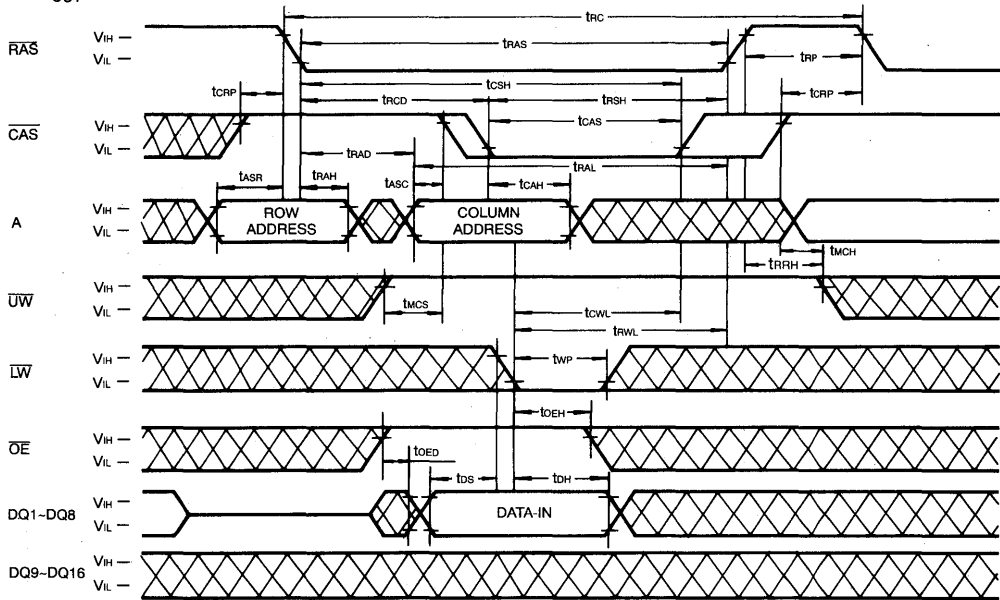
NOTE: D_{OUT} =OPEN



 DONT CARE

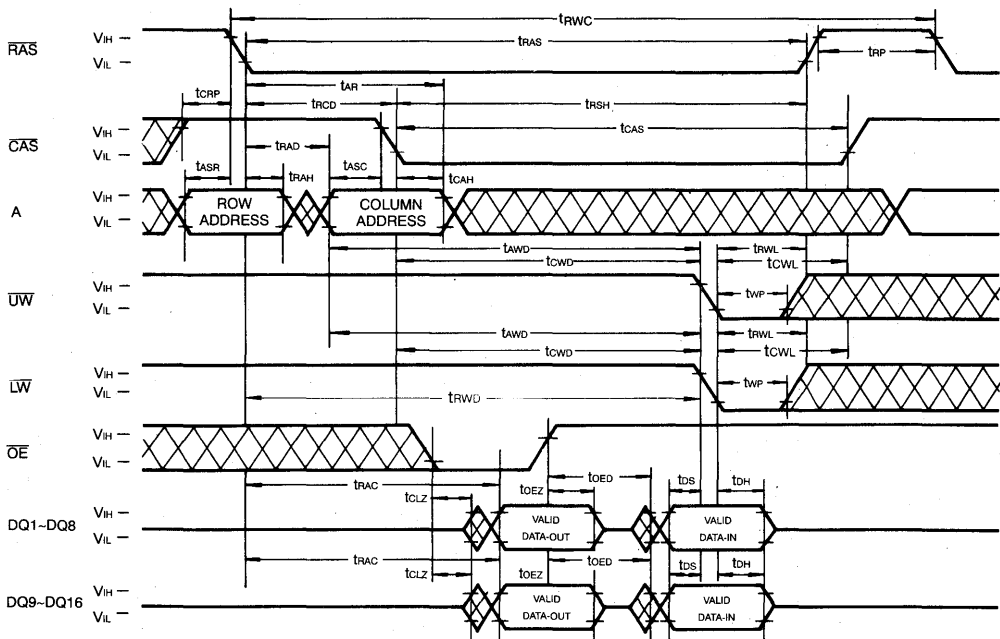
LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE; D_{OUT}=OPEN



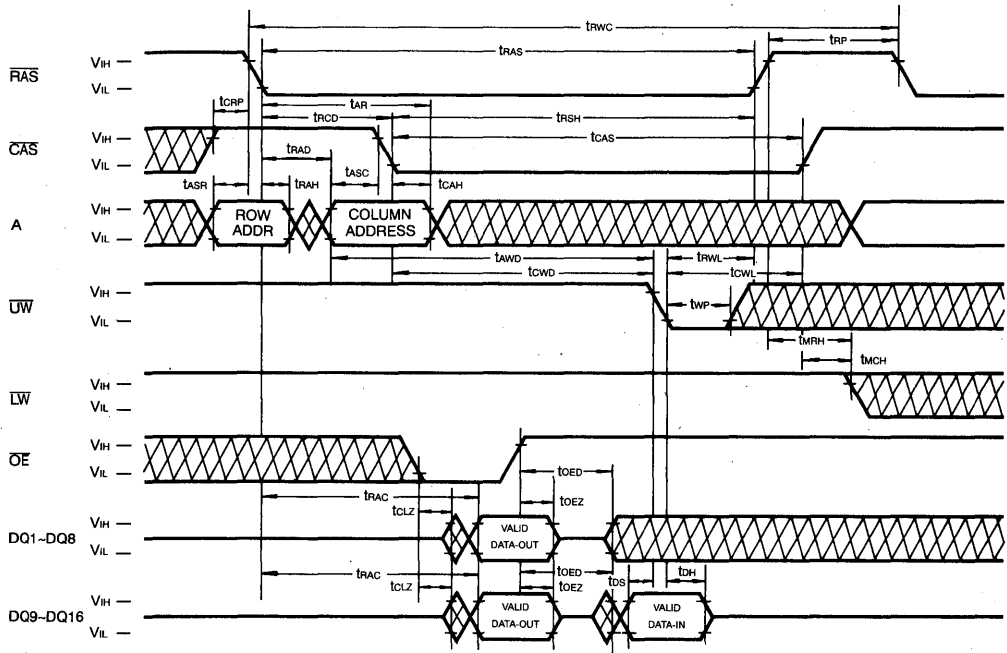
4

READ-MODIFY-WRITE CYCLE

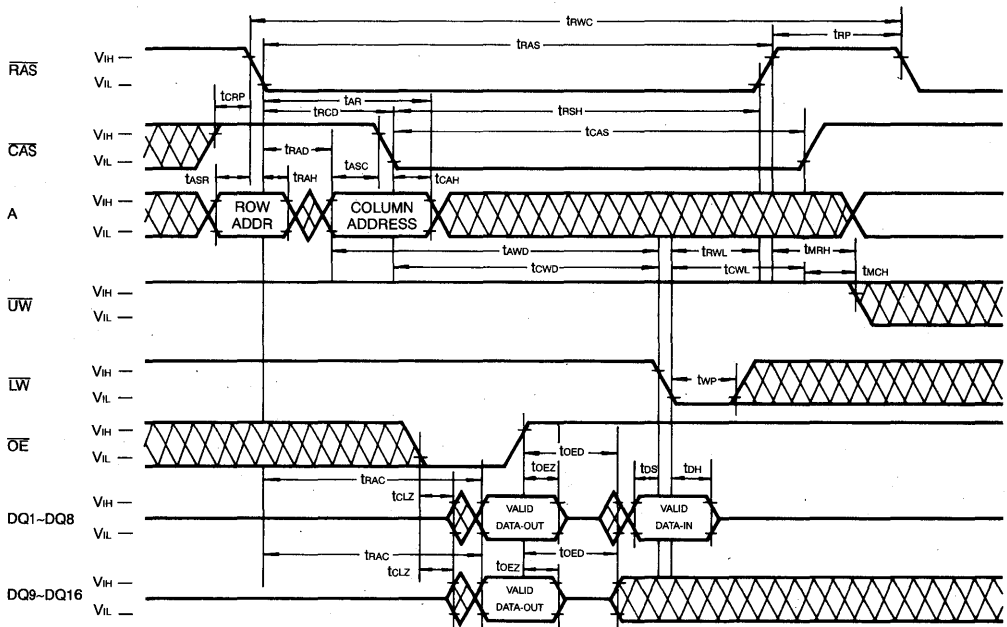


 DON'T CARE

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

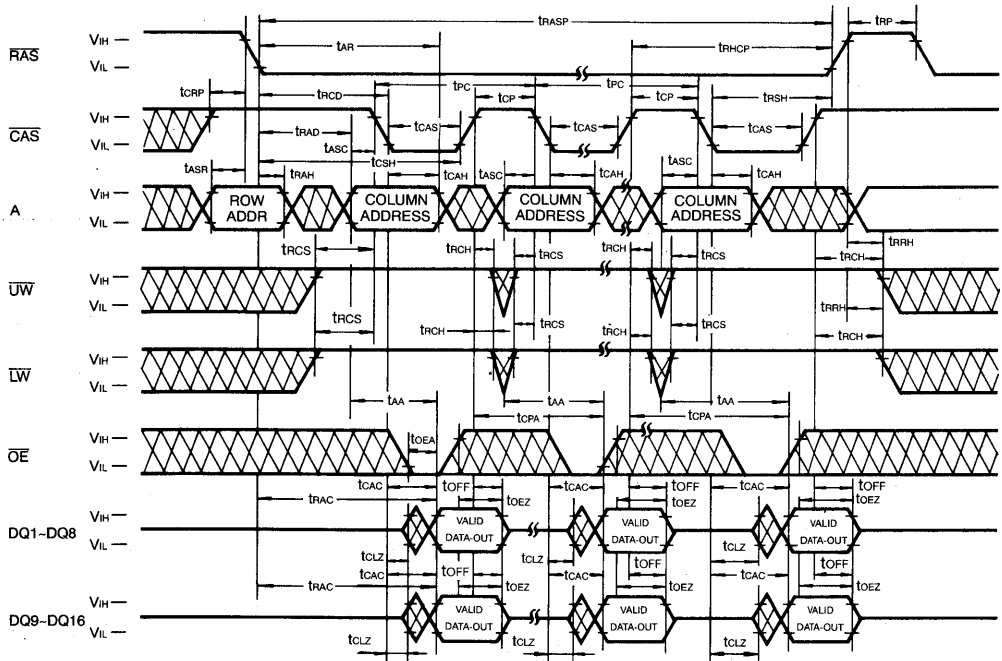


READ-MODIFY-LOWER-BYTE-WRITE CYCLE



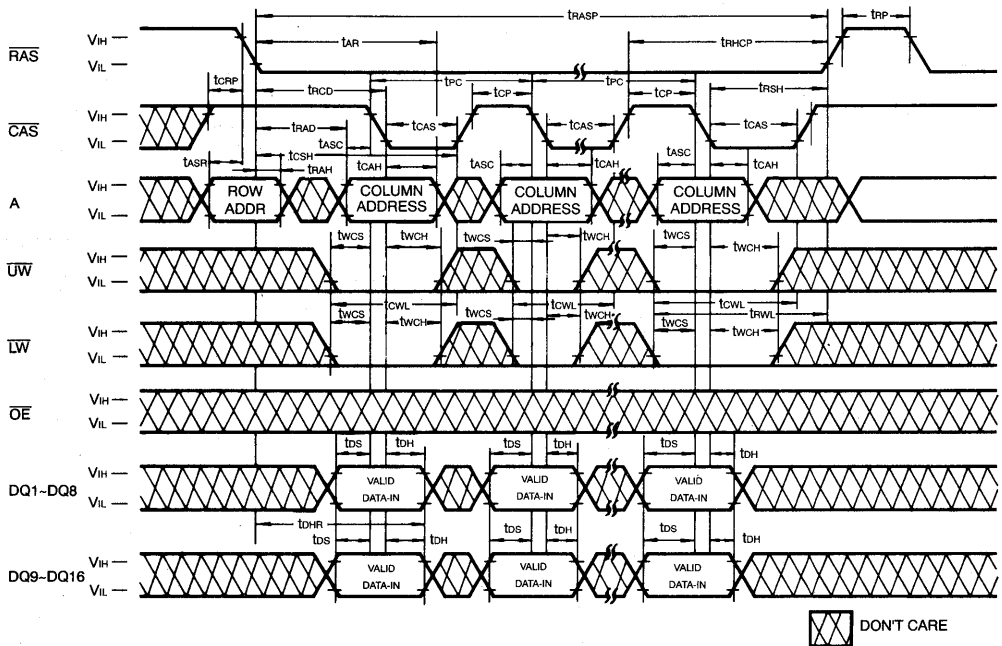
DON'T CARE

FAST PAGE MODE WORD READ CYCLE



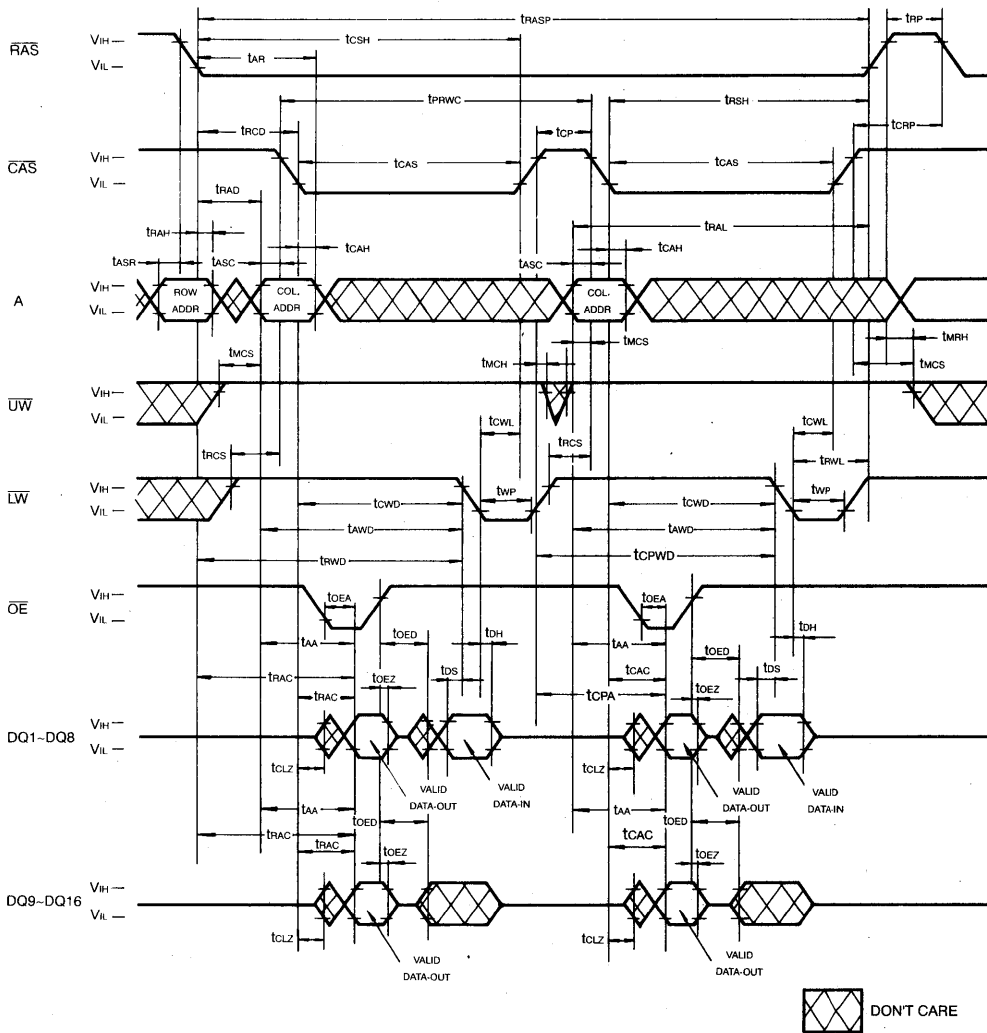
4

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



⊠ DON'T CARE

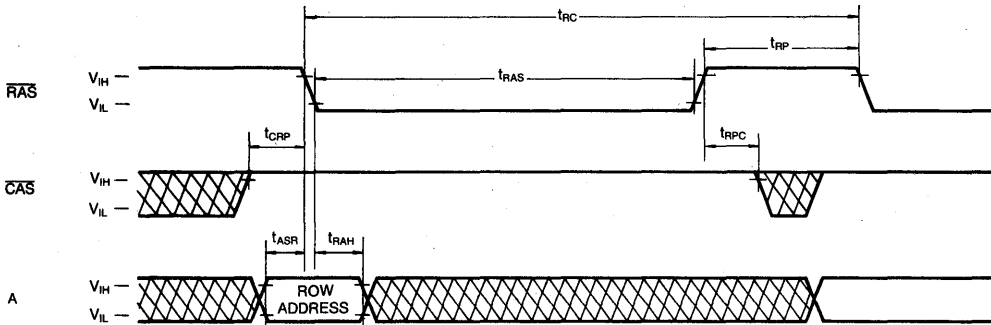
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



4

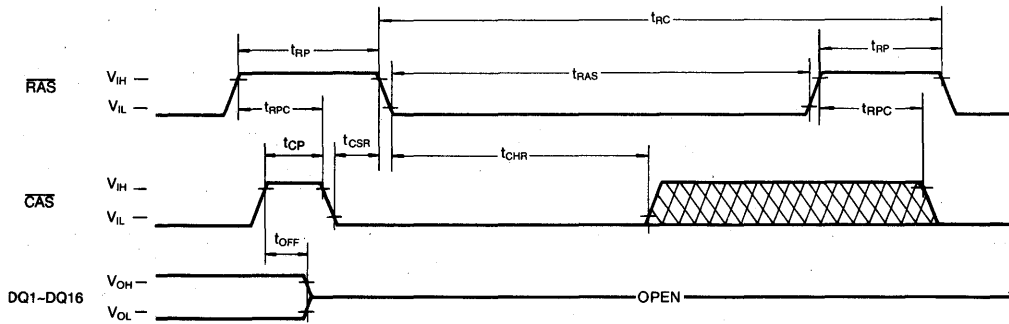
RAS-ONLY REFRESH CYCLE

NOTE: \overline{UW} , \overline{LW} , \overline{OE} , D_{IN} =Don't Care D_{OUT} =OPEN



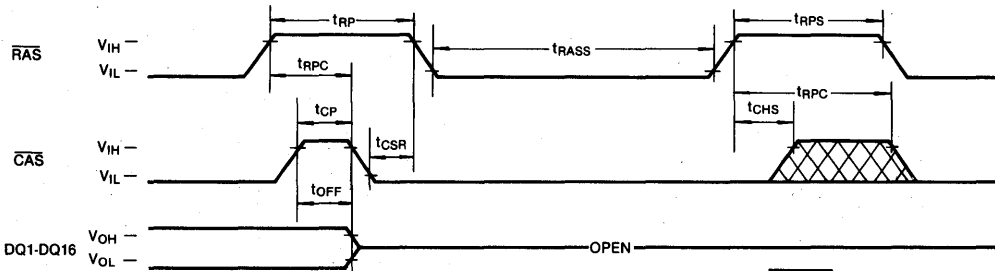
CAS-before-RAS REFRESH CYCLE

NOTE: \overline{UW} , \overline{LW} , \overline{OE} , A=Don't Care

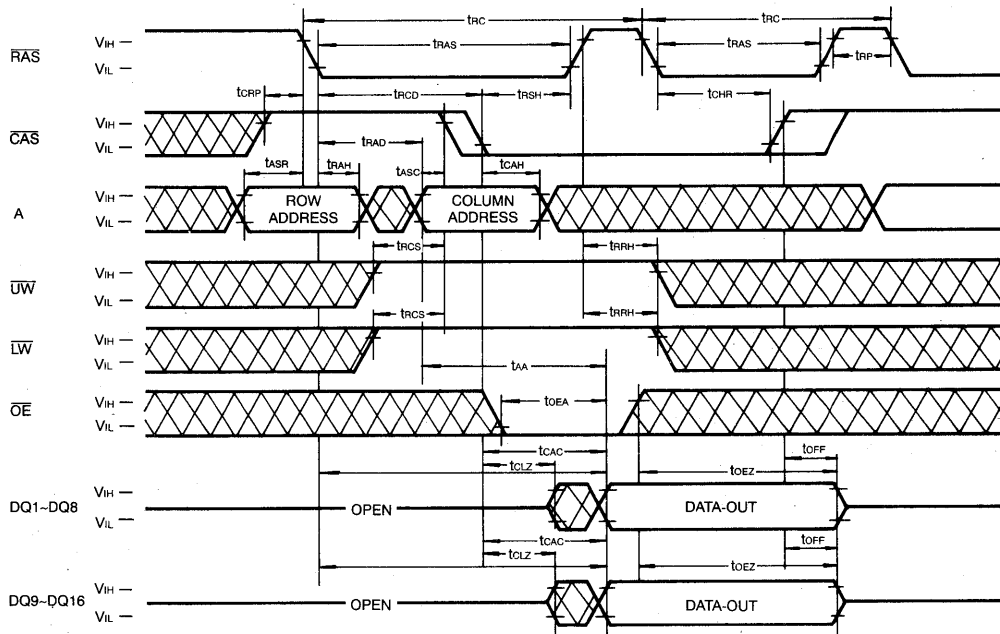


CAS-before-RAS SELF REFRESH CYCLE (LL-version)

NOTE: \overline{W} , \overline{OE} , A=Don't Care

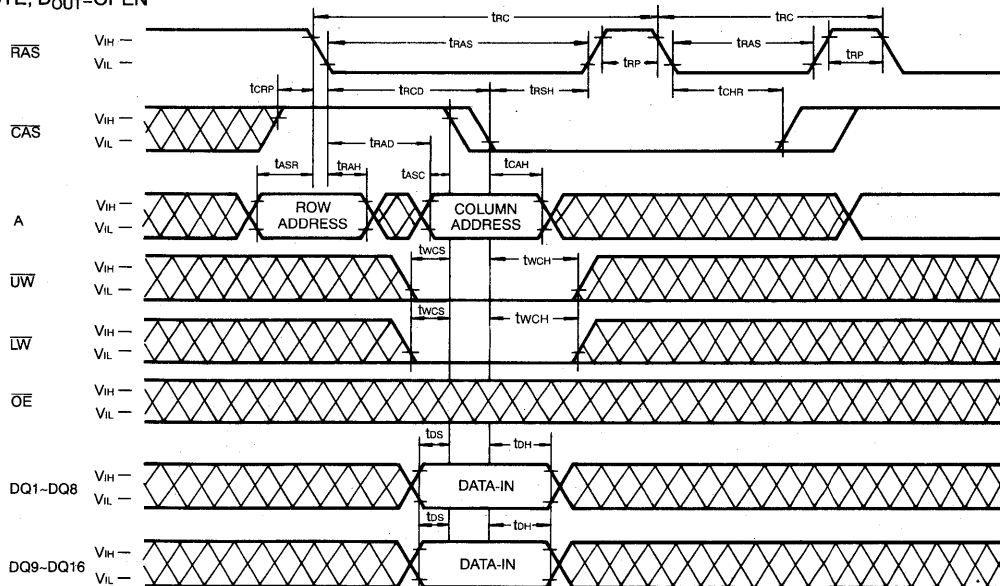


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE: D_{OUT} =OPEN

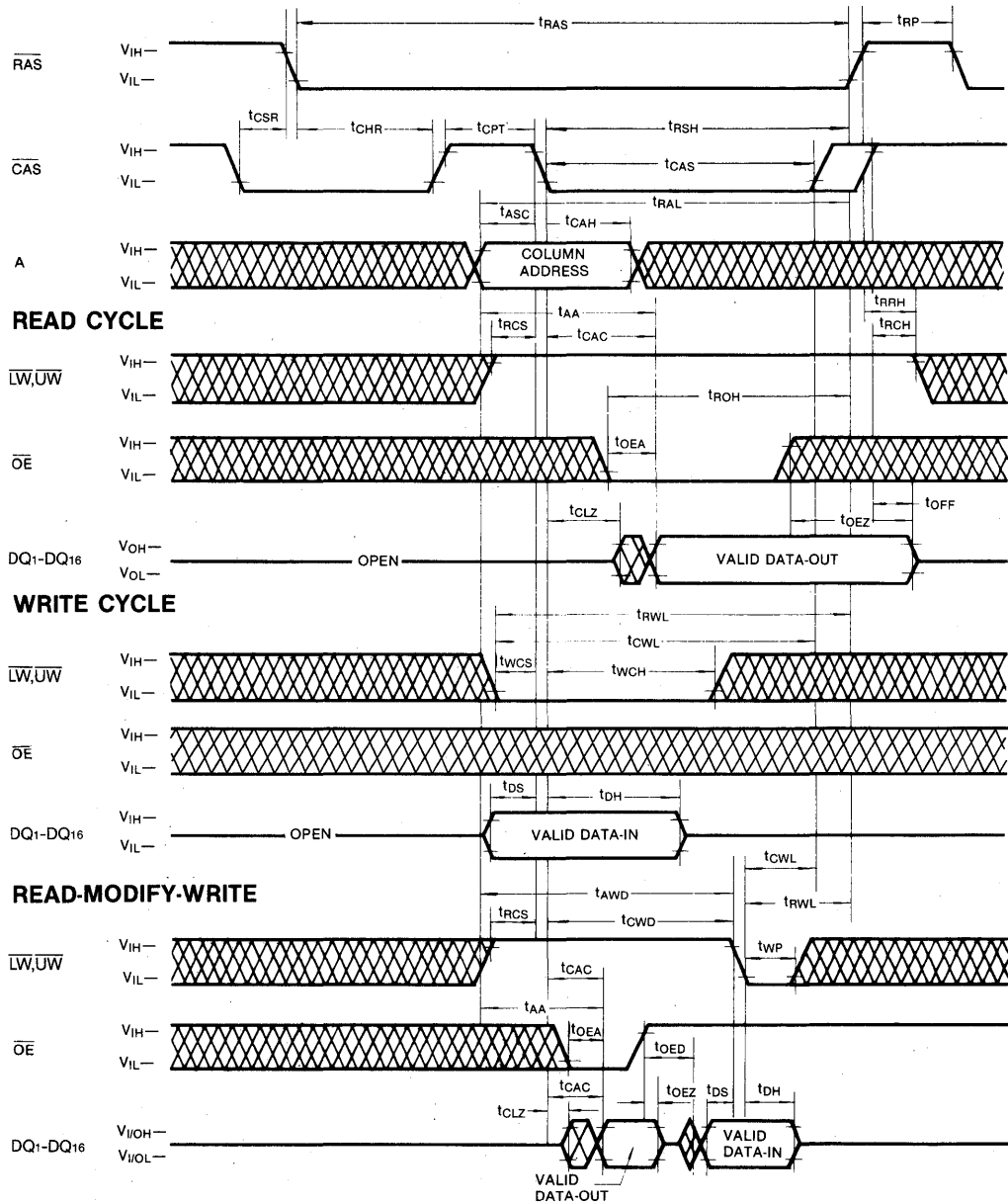


DONT CARE

4

TIMING DIAGRAMS (Continued)

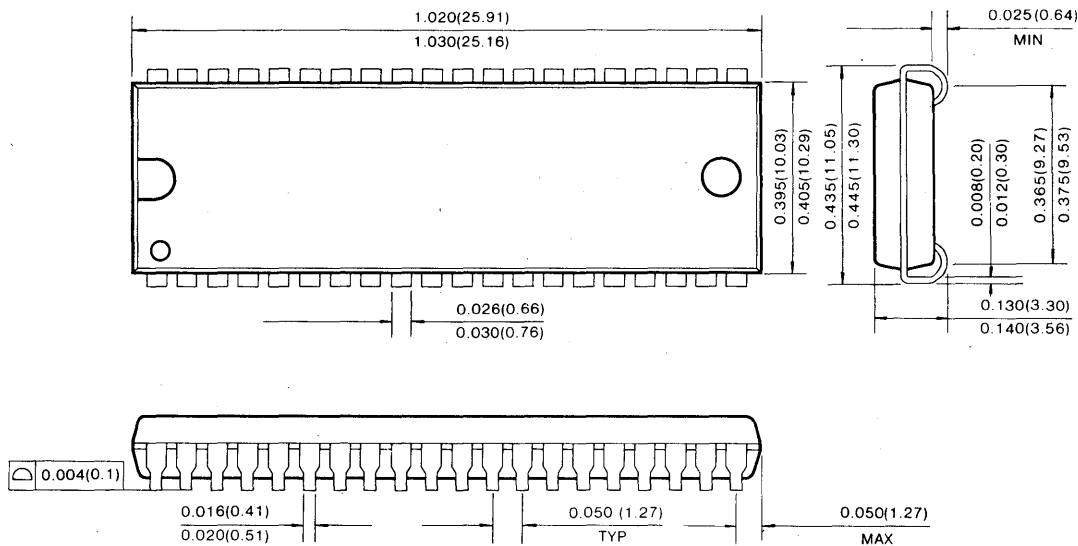
CAS-before-RAS REFRESH COUNTER TEST CYCLE



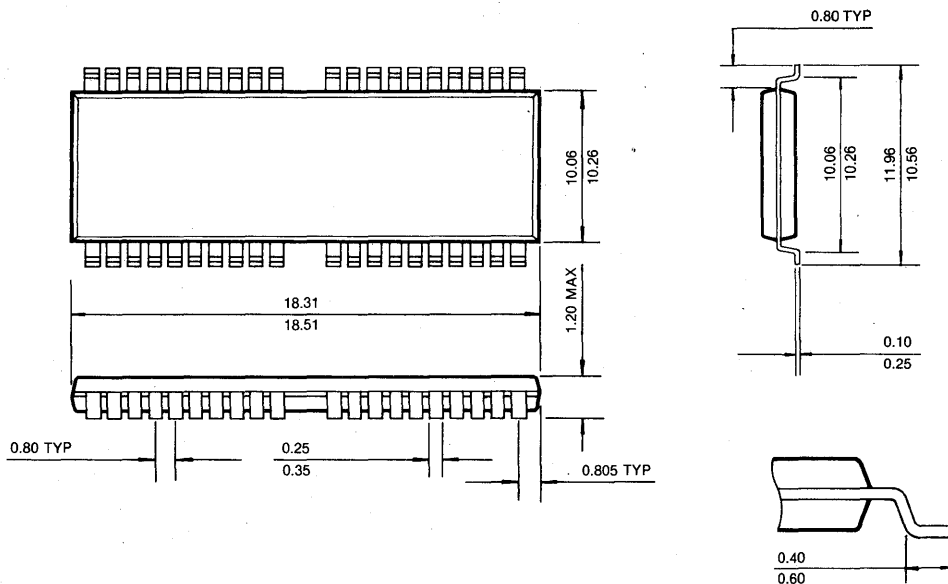
 DON'T CARE

PACKAGE DIMENSION
40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



4

256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	t_{TRAC}	t_{CAC}	t_{RC}
KM416C157B/BL/BLL-5	50ns	15ns	90ns
KM416C157B/BL/BLL-6	60ns	15ns	110ns
KM416C157B/BL/BLL-7	70ns	20ns	130ns
KM416C157B/BL/BLL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Byte Write operation(2W)**
- **Word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V ± 10% power supply**
- **Refresh cycle**
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L & LL-Ver)
- **Power Dissipation**
 - Standby: 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.83mW (LL-version)
 - Active (50/60/70/80): 470/385/360/330mW
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP (II)**

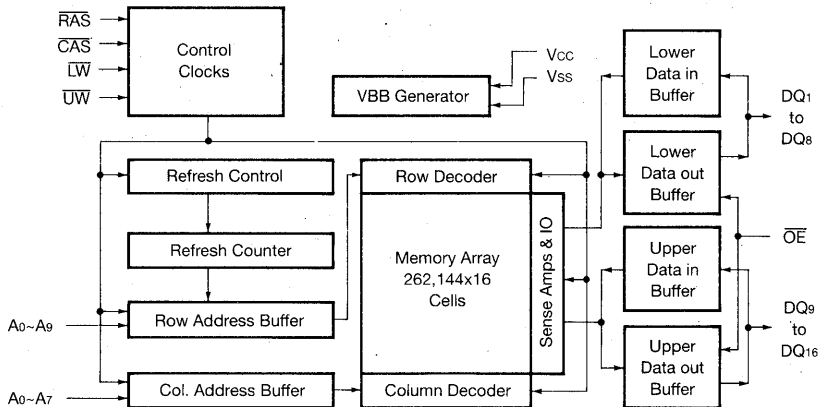
GENERAL DESCRIPTION

The Samsung KM416C157B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as minicomputers, graphics and high performance portable computers.

The KM416C157B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

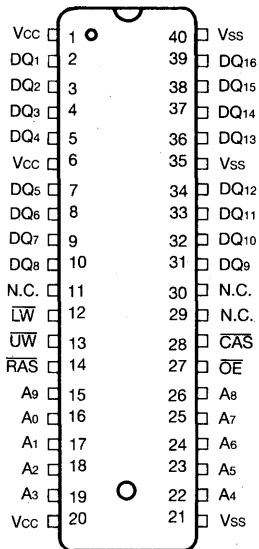
The KM416C157B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

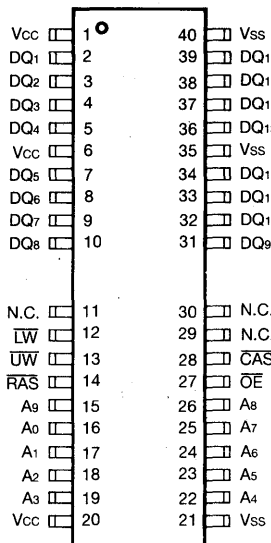


PIN CONFIGURATION (Top Views)

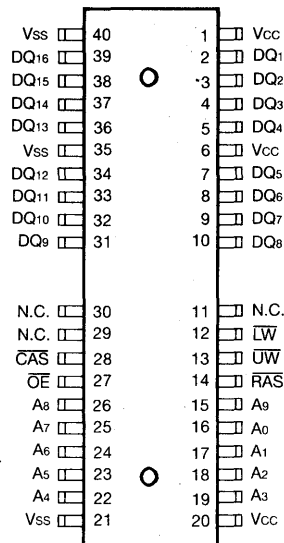
• KM416C157BJ/BLJ/BLLJ



• KM416C157BT/BLT/BLLT



• KM416C157BTR/BLTR/BLLTR



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
UW	Read/Upper Byte Write Input
LW	Read/Lower Byte Write Input
OE	Data Output Enable
Vcc	Power(+5V)
N.C.	No Connection

4

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ t _{RC} =min.)	KM416C157B/BL/BLL-5 KM416C157B/BL/BLL-6 KM416C157B/BL/BLL-7 KM416C157B/BL/BLL-8 I _{CC1}	-	85 70 65 60	mA mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{UW}}=\overline{\text{LW}}=\text{V}_{\text{IH}}$)	I _{CC2}	-	2	mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\overline{\text{CAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$ Cycling @ t _{RC} =min.)	KM416C157B/BL/BLL-5 KM416C157B/BL/BLL-6 KM416C157B/BL/BLL-7 KM416C157B/BL/BLL-8 I _{CC3}	-	85 70 65 60	mA mA mA mA
Fast Page Mode Current* ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{CAS}}$, Address Cycling @ t _{PC} =min.)	KM416C157B/BL/BLL-5 KM416C157B/BL/BLL-6 KM416C157B/BL/BLL-7 KM416C157B/BL/BLL-8 I _{CC4}	-	65 55 50 45	mA mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{UW}}=\overline{\text{LW}}=\text{V}_{\text{CC}}-0.2\text{V}$)	KM416C157B KM416C157BL KM416C157BLL I _{CC5}	-	1 200 150	mA μA μA
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ t _{RC} =min.)	KM416C157B/BL/BLL-5 KM416C157B/BL/BLL-6 KM416C157B/BL/BLL-7 KM416C157B/BL/BLL-8 I _{CC6}	-	85 70 65 60	mA mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{\text{CAS}}=0.2\text{V}$ D _{IN} =Don't Care, T _{RC} =125 μS (L-ver), T _{RAS} =T _{RAS} min.~300ns	KM416C157BL I _{CC7}	-	300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V xW=OE=A0-A9=VCC-0.2V or 0.2V	lccs		200	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ VCC+0.5V, all other pins not under test=0 volts.)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ VCC)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum two times while RAS=VIL. In Icc4, address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A9)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, LW, UW, OE)	CIN2	-	7	pF
Input Capacitance (DQ1-DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VCC=5V ± 10%, See notes 1,2)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	135		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		15		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tt	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	15		15		20		20		ns	
CAS hold time	tcSH	50		60		70		80		ns	
CAS pulse width	tcAS	15	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	35	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tcRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

* 50ns Product : VCC=5V ± 5%, Cout=50pF



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	TRAH	10		10		10		10		ns	
Column address set-up time	TASC	0		0		0		0		ns	
Column address hold time	TCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	TAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	TRAL	25		30		35		40		ns	
Read command set-up time	TRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	TRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	TRRH	0		0		0		0		ns	9
Write command hold time	TWCH	10		10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	TWCR	40		45		50		55		ns	6
Write command pulse width	TWP	10		10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	TRWL	15		15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	TCWL	15		15		15		20		ns	
Data set-up time	TDS	0		0		0		0		ns	10
Data hold time	TDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	TDHR	40		45		55		60		ns	6
Refresh period (Normal)	TREF		16		16		16		16	ms	
Refresh period (L,LL-Version)	TREF		128		128		128		128	ms	
Write command set-up time	TWCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{LW}}$, $\overline{\text{UW}}$ delay time	TCWD	40		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{LW}}$, $\overline{\text{UW}}$ delay time	TRWD	75		85		95		105		ns	8
Column address to $\overline{\text{LW}}$, $\overline{\text{UW}}$ delay time	TAWD	50		55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	TCPWD	55		60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	TCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	TCHR	10		10		10		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	TRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	TCPT	20		20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	TCPA		30		35		40		45	ns	3
Fast Page mode cycle time	TPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	TPRWC	80		80		95		100		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	TCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	TRASP	50	100K	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	TRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	TOEA		15		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	TOED	15		15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	TOEZ	0	15	0	15	0	20	0	20	ns	7
$\overline{\text{OE}}$ commend hold time	TOEH	15		15		20		20		ns	

* 50ns Product : $V_{CC} = 5V \pm 5\%$, $C_{out} = 50pF$

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5(*)		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Masked write set-up time	tMCS	0		0		0		0		ns	
Masked write hold time referenced to $\overline{\text{RAS}}$	tMRH	0		0		0		0		ns	
Masked write hold time referenced to $\overline{\text{CAS}}$	tMCH	0		0		0		0		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}\text{-B-}\overline{\text{R}}$ self refresh)	tRASS	100		100		100		100		μs	
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}\text{-B-}\overline{\text{R}}$ self refresh)	tRPS	90		110		130		150		ns	12
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}\text{-B-}\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		-50		ns	12

* 50ns Product : $V_{cc}=5V \pm 5\%$, $C_{out}=50\text{pF}$

KM416C157B Truth Table

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{UW}}$	$\overline{\text{LW}}$	$\overline{\text{OE}}$	$\text{DQ}_1\sim\text{DQ}_8$	$\text{DQ}_9\sim\text{DQ}_{16}$	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	X	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	L	L	X	DQ-IN	DQ-IN	Word Write
L	L	H	L	X	DQ-IN	-	Byte Write
L	L	L	H	X	-	DQ-IN	Byte Write

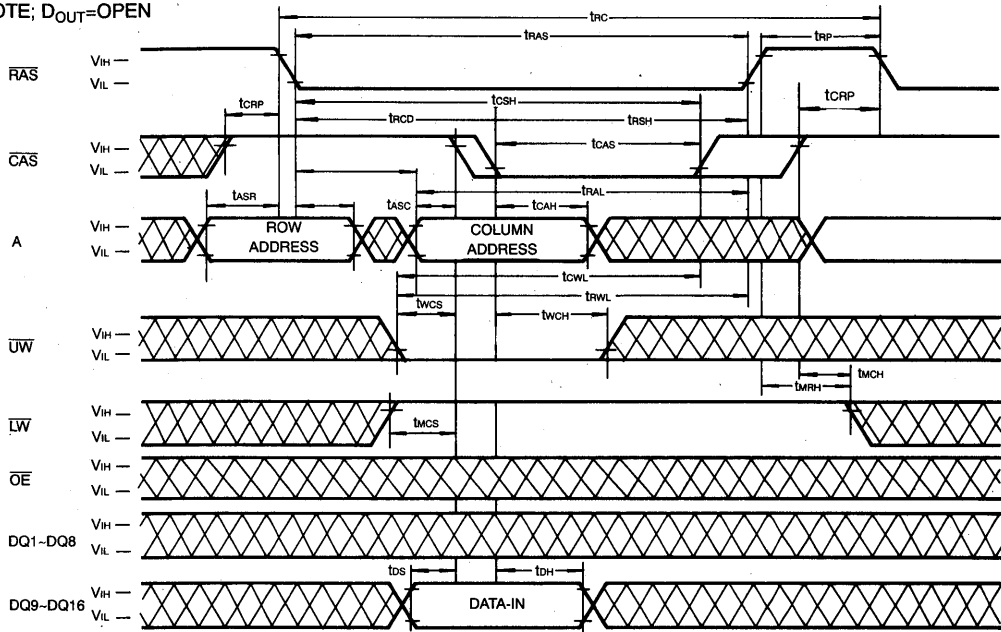
4

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCDB}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCDB}(\max)$ is specified as a reference point only. If t_{RCDB} is greater than the specified $t_{RCDB}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCDB} \geq t_{RCDB}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. 1024 cycles of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification
13. t_{RCS} , t_{MCS} are referenced to the later \overline{W} rising edge at early write cycle.
14. t_{WCS} is referenced to the later \overline{W} falling edge at early write cycle.
15. t_{CWL} , t_{RWL} are referenced to the later \overline{W} falling edge at early write cycle.
16. t_{WCH} , t_{WP} are referenced to the earlier \overline{W} falling edge at early write cycle.
17. t_{RWD} , t_{AWD} , t_{CWD} are referenced to the earlier \overline{W} falling edge at Read-Modify-write cycle.

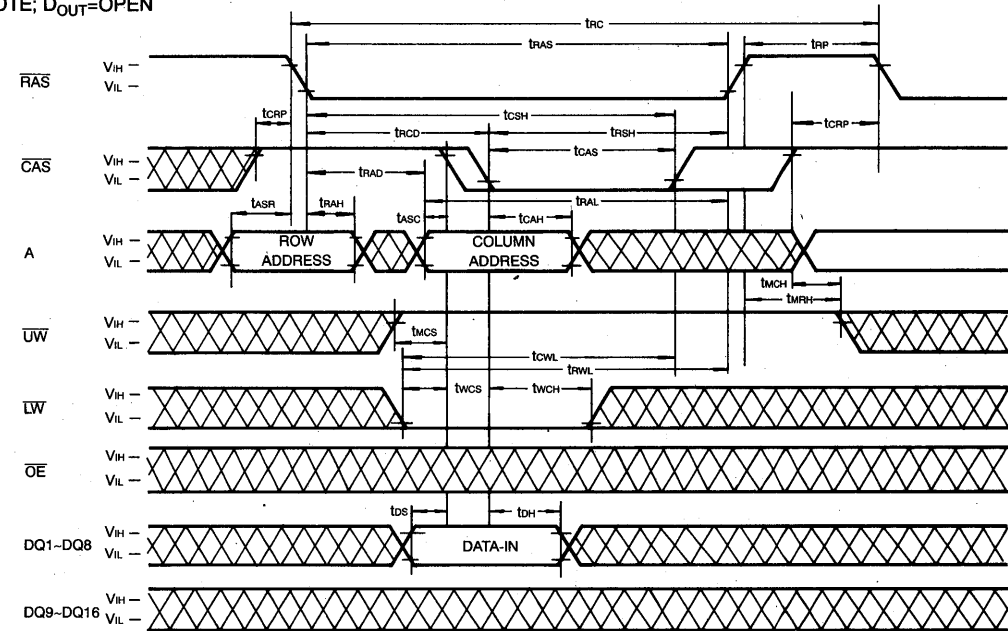
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE: D_{OUT}=OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

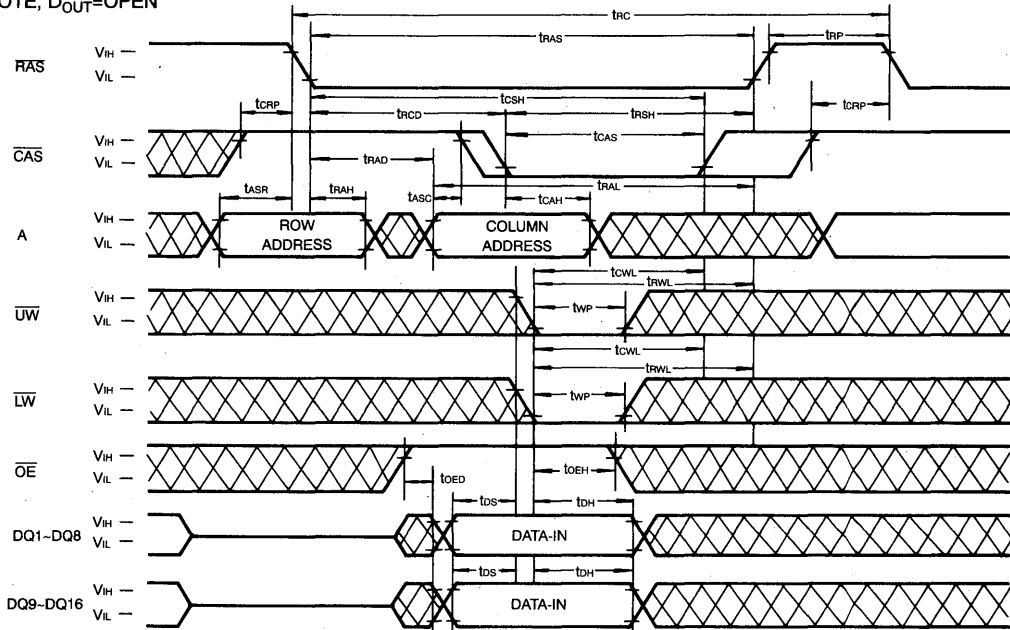
NOTE: D_{OUT}=OPEN



DONT CARE

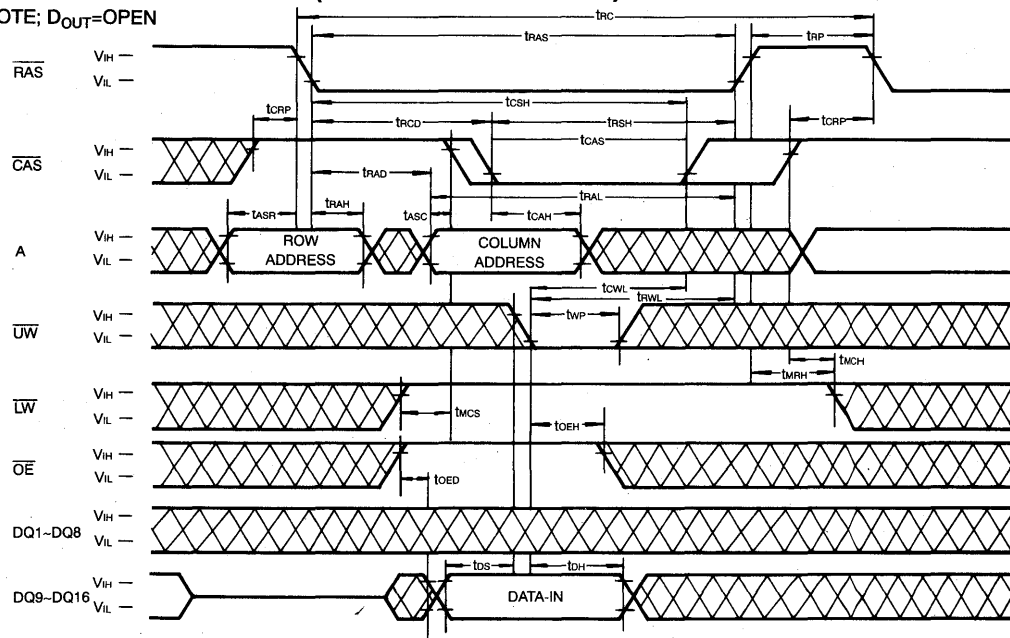
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE; $D_{OUT} = OPEN$



UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE; $D_{OUT} = OPEN$

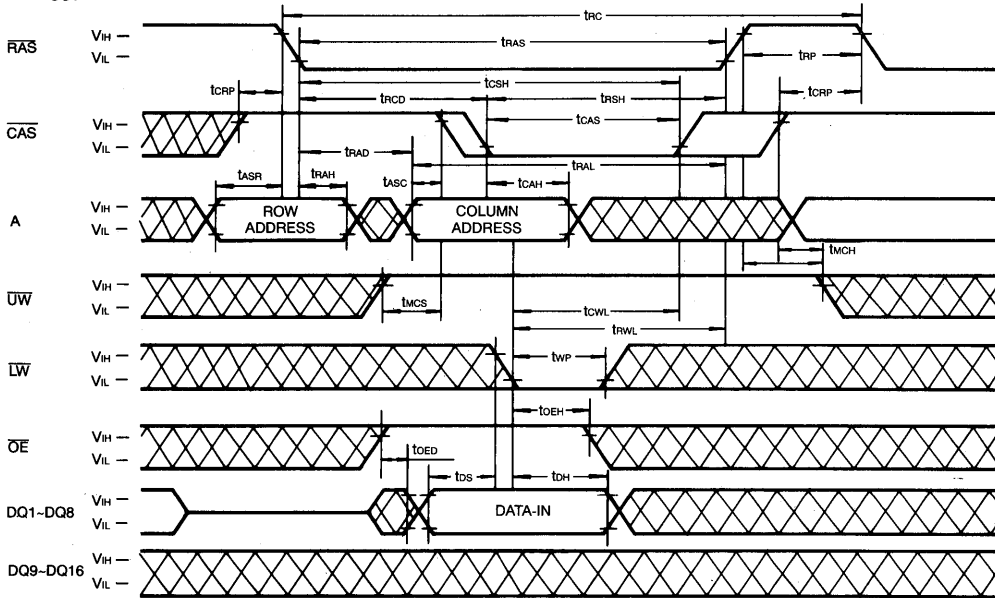


 DON'T CARE

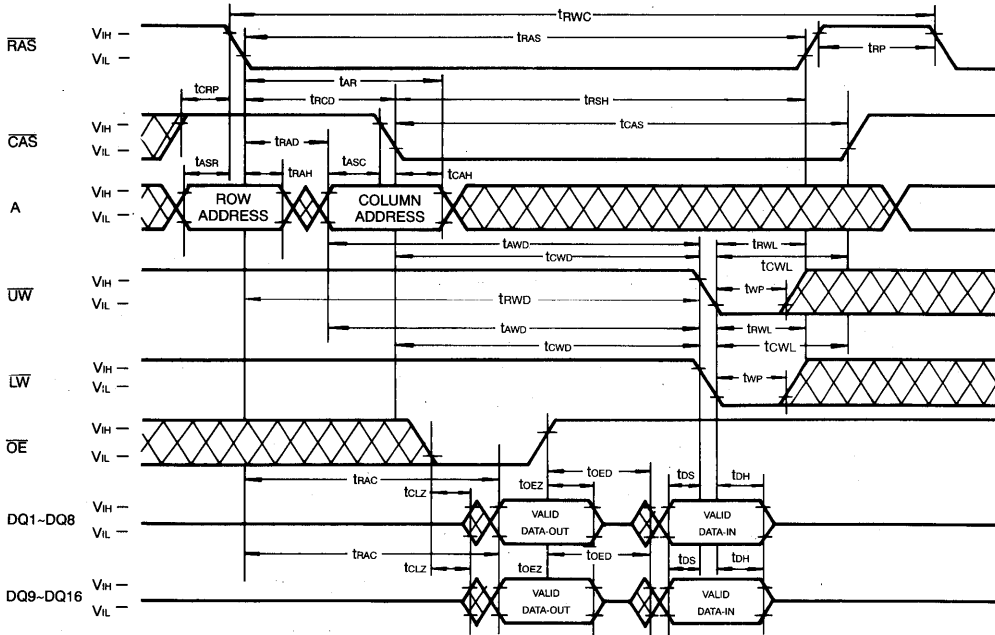
4

LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE: D_{OUT}=OPEN

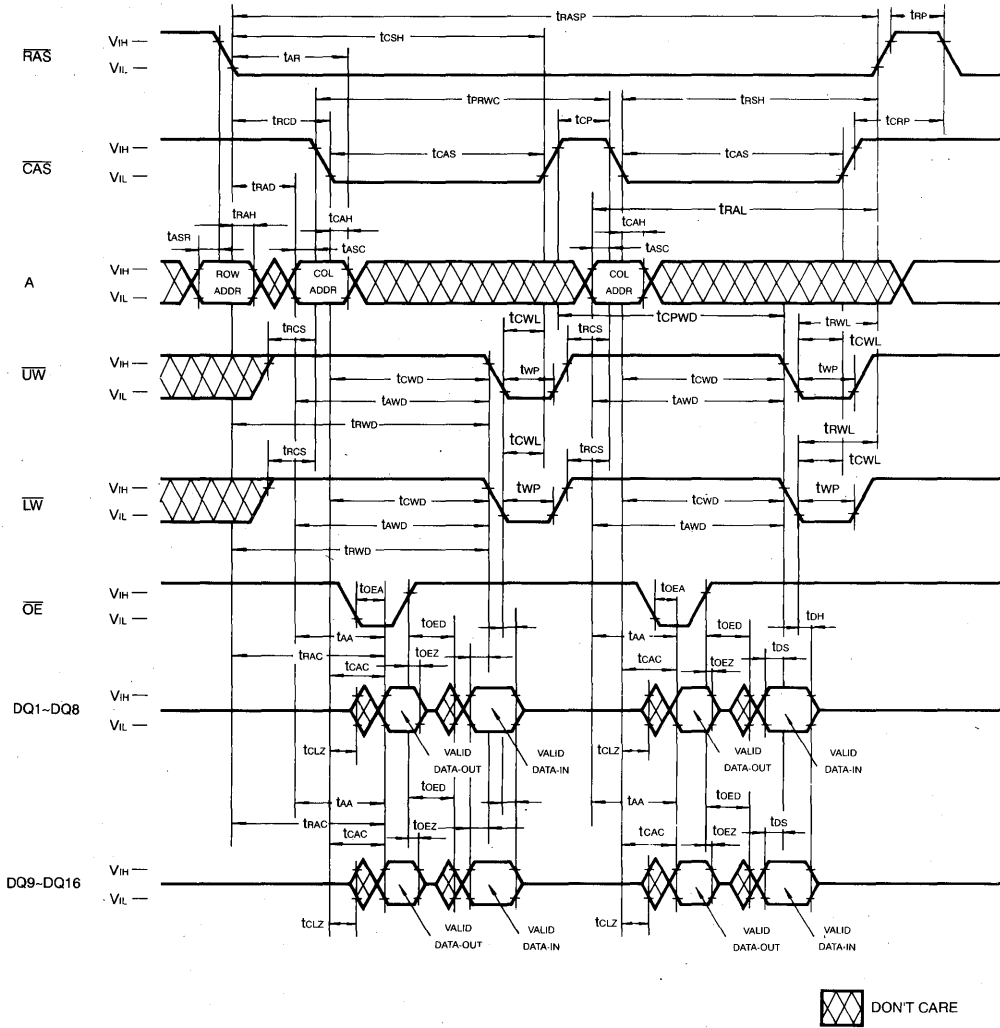


READ-MODIFY-WRITE CYCLE

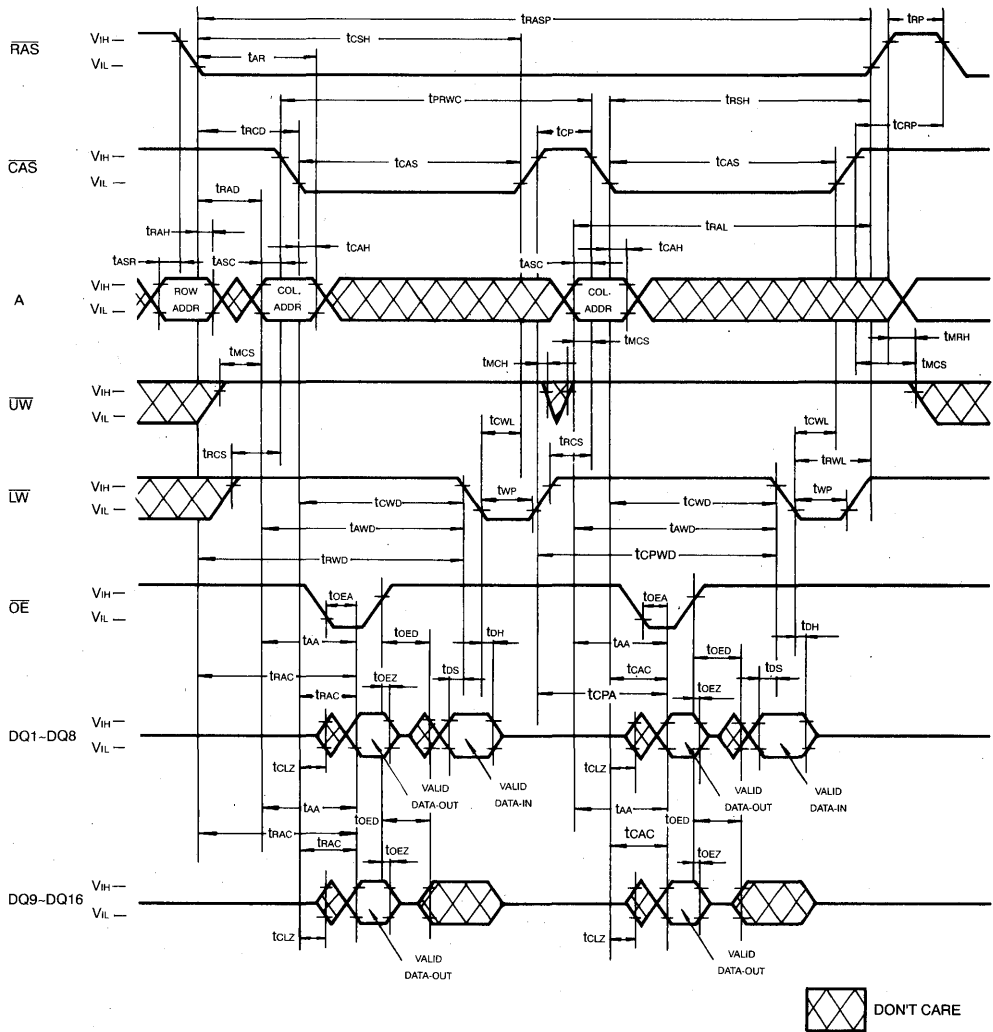


 DON'T CARE

FAST PAGE MODE READ-MODIFY- WRITE CYCLE

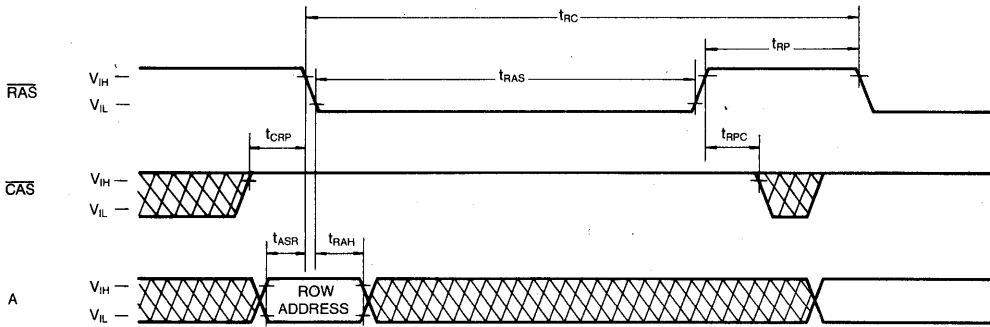


FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



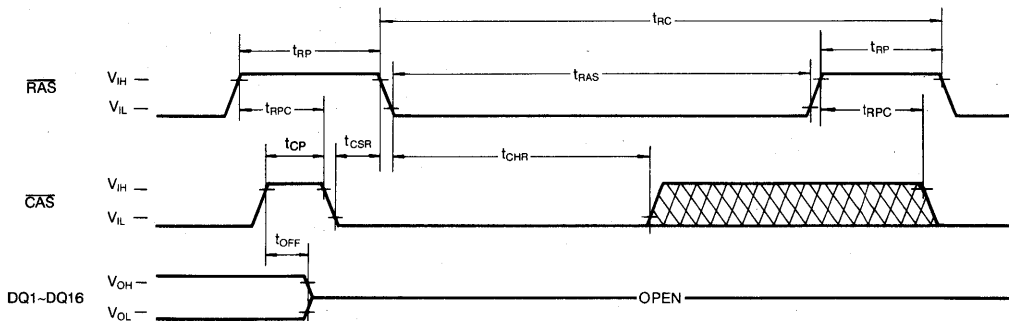
RAS-ONLY REFRESH CYCLE

NOTE: \bar{UW} , \bar{LW} , \bar{OE} , D_{IN} =Don't Care D_{OUT} =OPEN



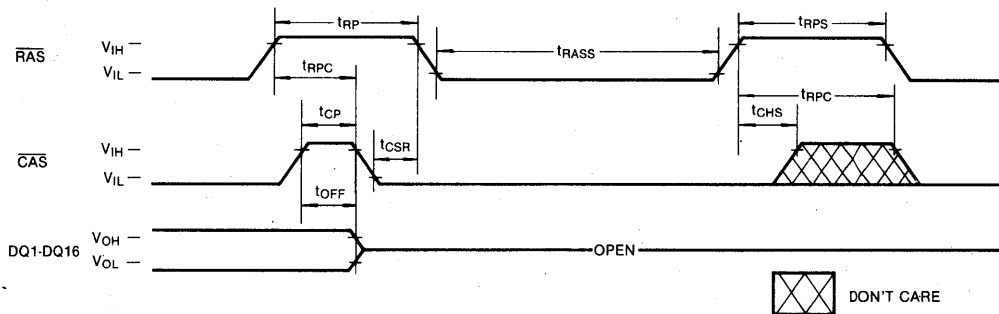
CAS-before-RAS REFRESH CYCLE

NOTE: \bar{UW} , \bar{LW} , \bar{OE} , A=Don't Care



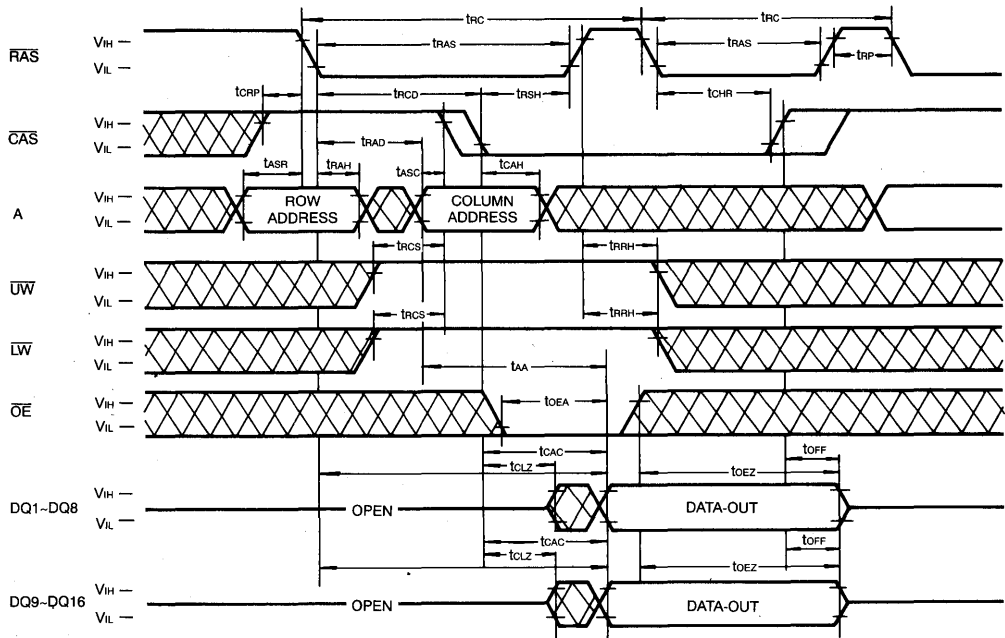
CAS-before-RAS SELF REFRESH CYCLE (LL-version)

NOTE: \bar{W} , \bar{OE} , A=Don't Care



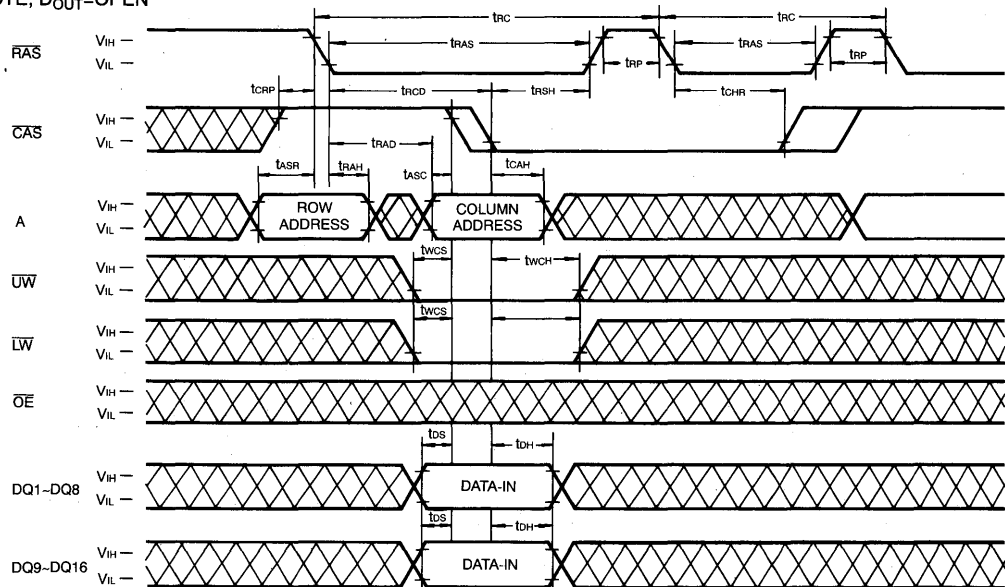
4

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

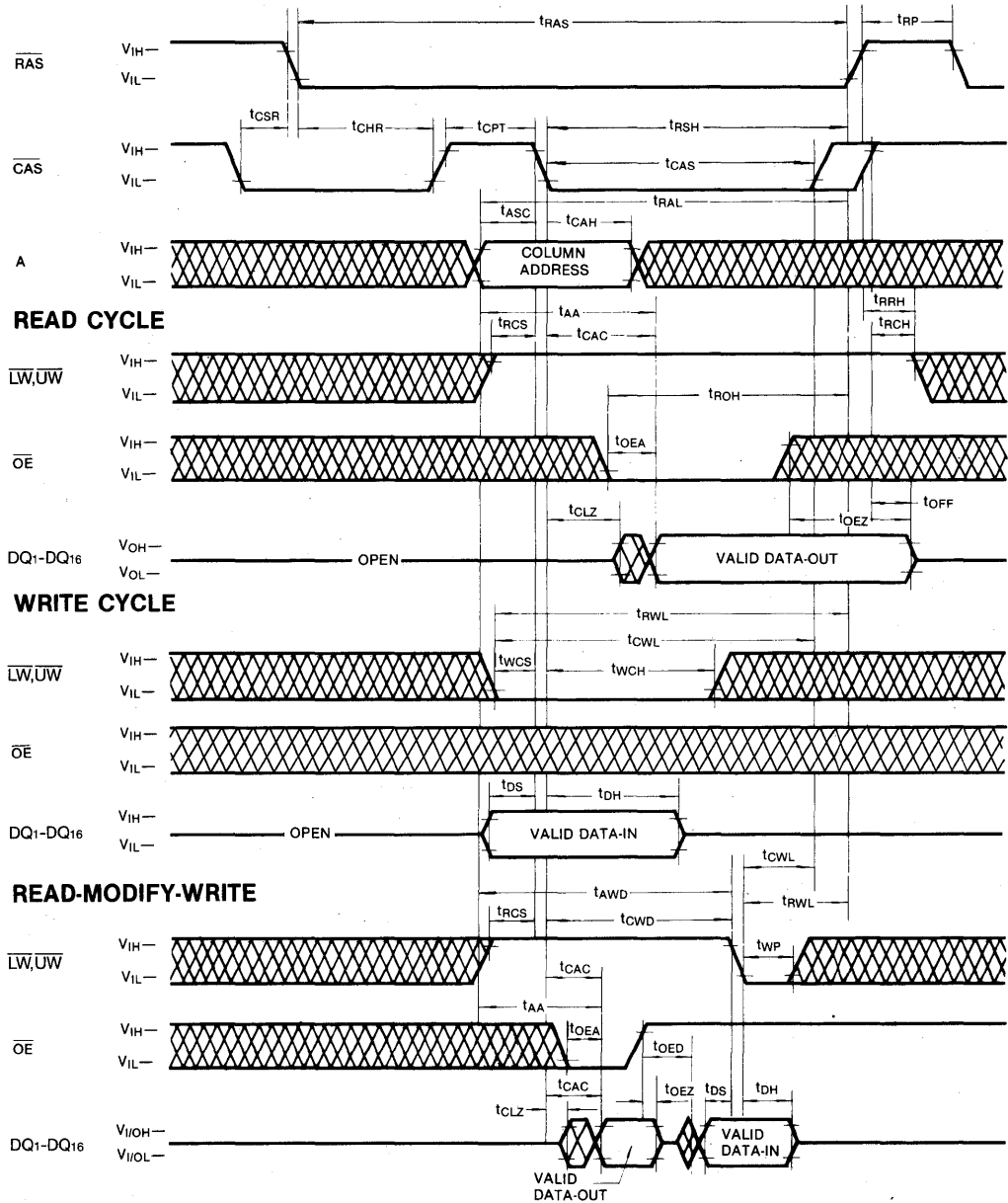
NOTE; D_{OUT} =OPEN



 DON'T CARE

TIMING DIAGRAMS (Continued)

CAS-before-RAS REFRESH COUNTER TEST CYCLE

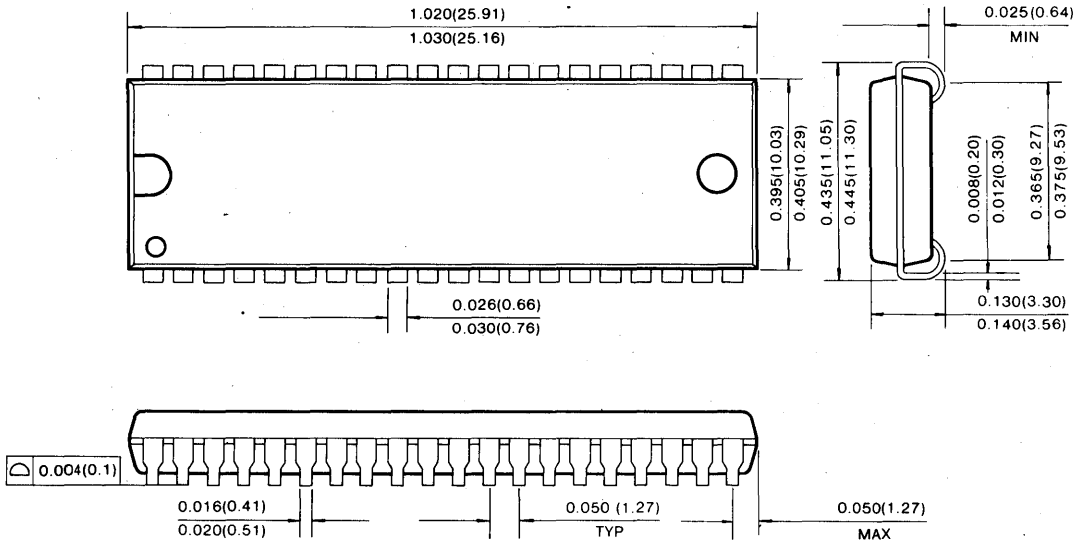


 DON'T CARE

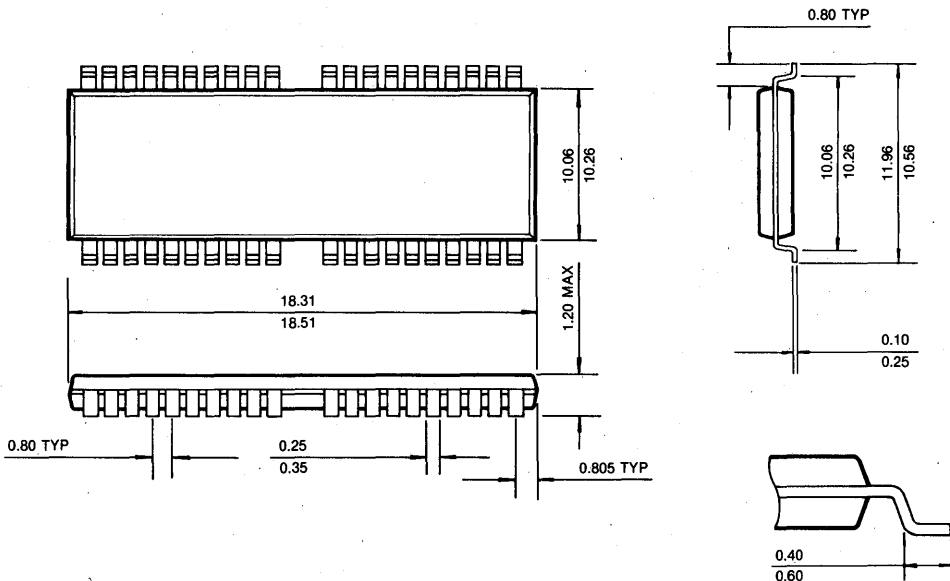
4

PACKAGE DIMENSION
40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K × 18 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	trAC	tcAC	trC
KM418C256B/BL/BLL-6	60ns	15ns	110ns
KM418C256B/BL/BLL-7	70ns	20ns	130ns
KM418C256B/BL/BLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Self Refresh operation (LL-version)
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +5.0V ± 10% power supply
- Refresh Cycle
 - 512 cycle/8ms (Normal)
 - 512 cycle/64ms (L-version)
 - 512 cycle/128ms (LL-version)
- Power Dissipation
 - Standby: 5.5mW (Normal)
 - 1.1mW (L-version)
 - 0.83mW (LL-version)
 - Active (60/70/80): 525/470/440mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

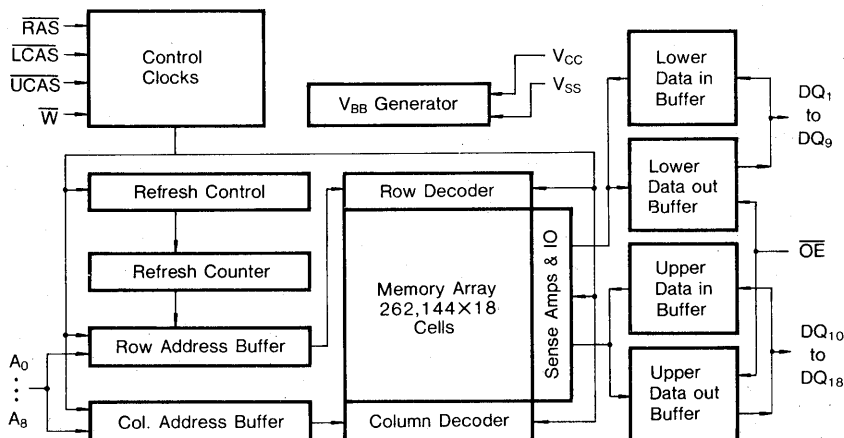
GENERAL DESCRIPTION

The Samsung KM418C256B/BL/BLL is a CMOS high speed 262,144 bit × 18 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM418C256B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

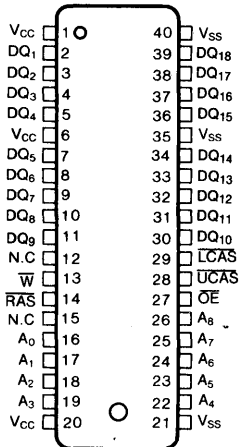
The KM418C256B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



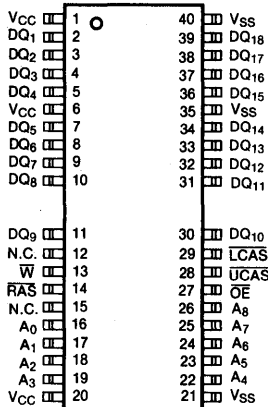
PIN CONFIGURATION (Top Views)

• KM418C256BJ/BLJ/BLLJ



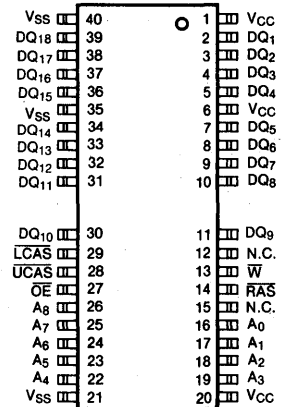
(SOJ)

• KM418C256BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM418C256BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function	Pin Name	Pin Function
A ₀ -A ₈	Address Inputs	\overline{LCAS}	Lower Column Address Strobe
DQ ₁₋₁₈	Data In/Out	\overline{W}	Read/Write Input
V _{SS}	Ground	\overline{OE}	Data Output Enable
\overline{RAS}	Row Address Strobe	V _{CC}	Power (+5V)
\overline{UCAS}	Upper Column Address Strobe	N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* (\overline{RAS} , \overline{UCAS} or \overline{LCAS} , Address Cycling @trc=min.)	KM418C256B/BL/BLL-6	I _{CC1}	-	95	mA
	KM418C256B/BL/BLL-7			85	mA
	KM418C256B/BL/BLL-8			80	mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{IH}$)		I _{CC2}	-	2	mA
\overline{RAS} -Only Refresh Current* ($\overline{UCAS}=\overline{LCAS}=V_{IH}$, \overline{RAS} , Address Cycling @trc=min.)	KM418C256B/BL/BLL-6	I _{CC3}	-	95	mA
	KM418C256B/BL/BLL-7			85	mA
	KM418C256B/BL/BLL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{UCAS} or \overline{LCAS} , Address Cycling @trc=min.)	KM418C256B/BL/BLL-6	I _{CC4}	-	60	mA
	KM418C256B/BL/BLL-7			55	mA
	KM418C256B/BL/BLL-8			50	mA
Standby Current ($\overline{RAS}=\overline{UCAS}=\overline{LCAS}=\overline{W}=V_{CC}-0.2V$)	KM418C256B	I _{CC5}	-	1	mA
	KM418C256BL			200	μ A
	KM418C256BLL			150	μ A
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} , \overline{UCAS} or \overline{LCAS} Cycling @trc=min.)	KM418C256B/BL/BLL-6	I _{CC6}	-	95	mA
	KM418C256B/BL/BLL-7			85	mA
	KM418C256B/BL/BLL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V, xCAS=0.2V D _{IN} =Don't Care, T _{RC} =125 μ S T _{RAS} =T _{RAS} min. ~300ns	KM418C256BL	I _{CC7}	-	300	μ A
Self Refresh Current $\overline{RAS}=\overline{xCAS}=0.2V$ $\overline{W}=\overline{OE}=\overline{A_0}-\overline{A_8}=V_{CC}-0.2V$ or 0.2V DQ1-DQ16=V _{CC} -0.2V, 0.2V or Open	KM418C256BLL	I _{CC8}	-	200	μ A
Input Leakage Current (Any input 0 \leq V _{IN} \leq V _{CC} +0.5V, all other pins not under test=0 volts.)		I _{I(L)}	-10	10	μ A
Output Leakage Current (Data out is disabled, 0V \leq V _{OUT} \leq V _{CC})		I _{O(L)}	-10	10	μ A
Output High Voltage Level (I _{OH} =-5mA)		V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)		V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A=25^{\circ}\text{C}$, $V_{CC}=5\text{V}$, $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0\text{--}A_8$)	CIN1	-	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$)	CIN2	-	7	pF
Input Capacitance ($\text{DQ}_1\text{--}\text{DQ}_{18}$)	CDQ	-	7	pF

AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CC}=5.0\text{V} \pm 10\%$, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from $\overline{\text{RAS}}$	trac		60		70		80	ns	3,4,11
Access time from $\overline{\text{CAS}}$	tcac		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	trp	40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ hold time	trSH	15		20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	tcAS	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	trCD	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	trAD	15	30	15	35	15	40	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	trAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	trAL	30		35		40		ns	
Read command set-up time	trCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command set-up time	twCS	0		0		0		ns	8
Write command hold time	twCH	10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh period (LL-version)	tREF		128		128		128	ms	
CAS to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		65		ns	8
CAS precharge to $\overline{\text{W}}$ delay time	tCPWD	60		65		70		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		ns	
RAS precharge to CAS hold time	tRPC	5		5		5		ns	
CAS precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from CAS precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	85		95		100		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from CAS precharge	tRHCP	35		40		45		ns	
CAS precharge time (Fast Page mode)	tCP	10		10		10		ns	
Access time from $\overline{\text{OE}}$	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data-in delay time	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ commend hold time	tOEH	15		20		20		ns	
RAS pulse width ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRASS	100		100		100		μs	12
RAS precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRPS	110		130		150		ns	12
CAS hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	12

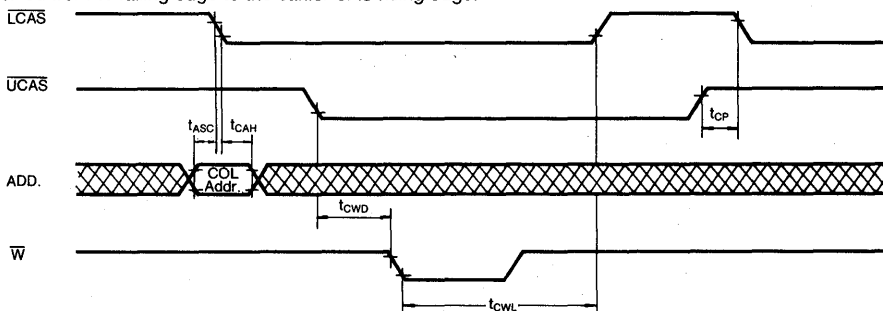
KM418C256B Truth Table

RAS	LCAS	UCAS	W	OE	DQ _{1~9}	DQ _{10~18}	State
H	H	H	H	H	Hi-Z	Hi-Z	Standby
L	H	H	H	H	Hi-Z	Hi-Z	Refresh
L	L	H	H	L	DQ-OUT	Hi-Z	Lower Byte Read
L	H	L	H	L	Hi-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	Hi-Z	Hi-Z	—

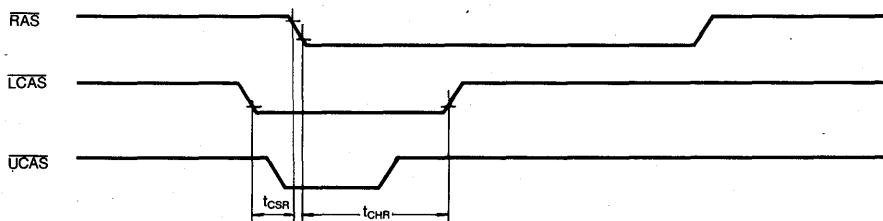
4

NOTES

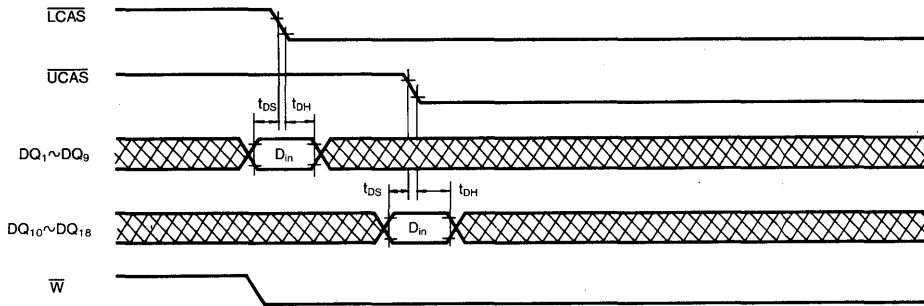
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}(\text{max})}$ limit insures that $t_{\text{RAC}(\text{max})}$ can be met. $t_{\text{RCD}(\text{max})}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}(\text{max})}$ limit, then access time is controlled exclusively by t_{ACD} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}(\text{max})}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}(\text{max})}$.
7. $t_{\text{OFF}(\text{max})}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating aparameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}(\text{min})}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}(\text{min})}$, $t_{\text{RWD}} \geq t_{\text{RWD}(\text{min})}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\text{min})}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}(\text{max})}$ limit insures that $t_{\text{RAC}(\text{max})}$ can be met. $t_{\text{RAD}(\text{max})}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}(\text{max})}$ limit, then access time is controlled by t_{AA} .
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, in order to meet refresh specification.
13. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
14. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
15. t_{OWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.



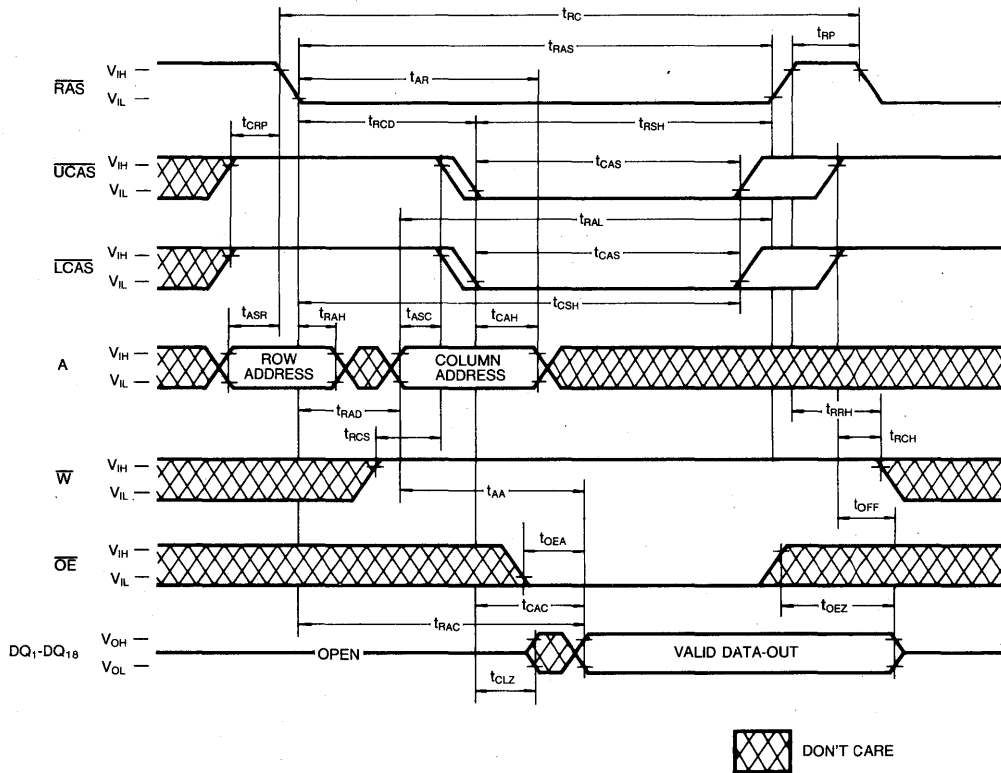
17. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
18. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



19. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1\sim9)}$, upper byte $D_{in(10\sim18)}$.

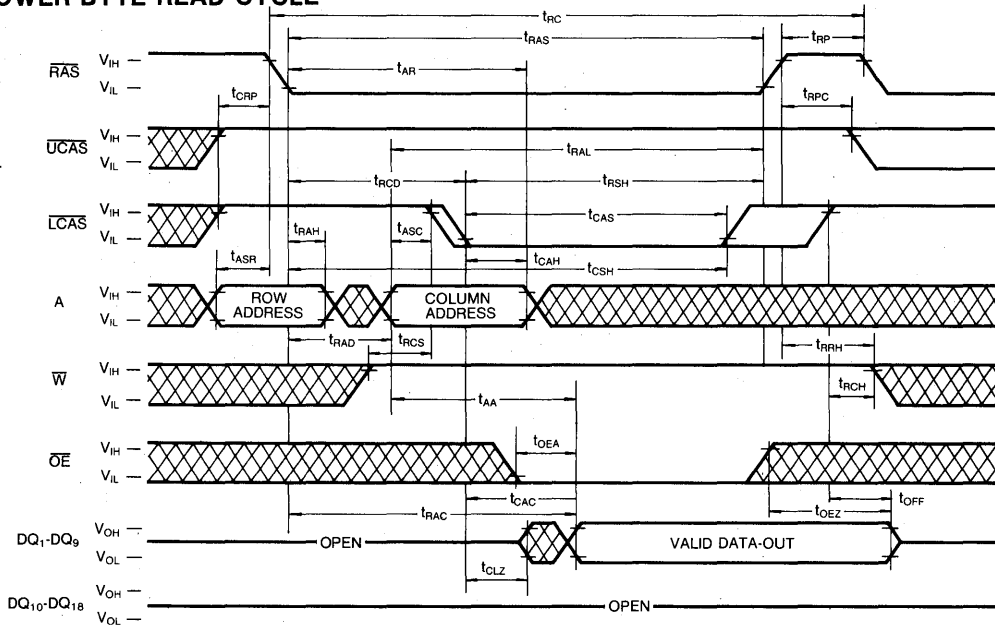


TIMING DIAGRAMS
WORD READ CYCLE

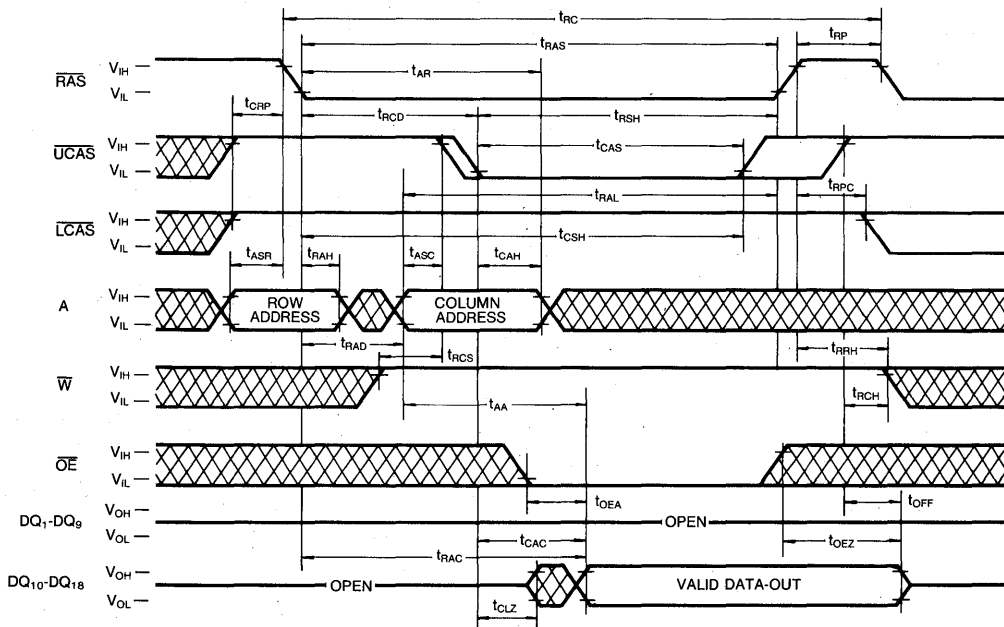


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



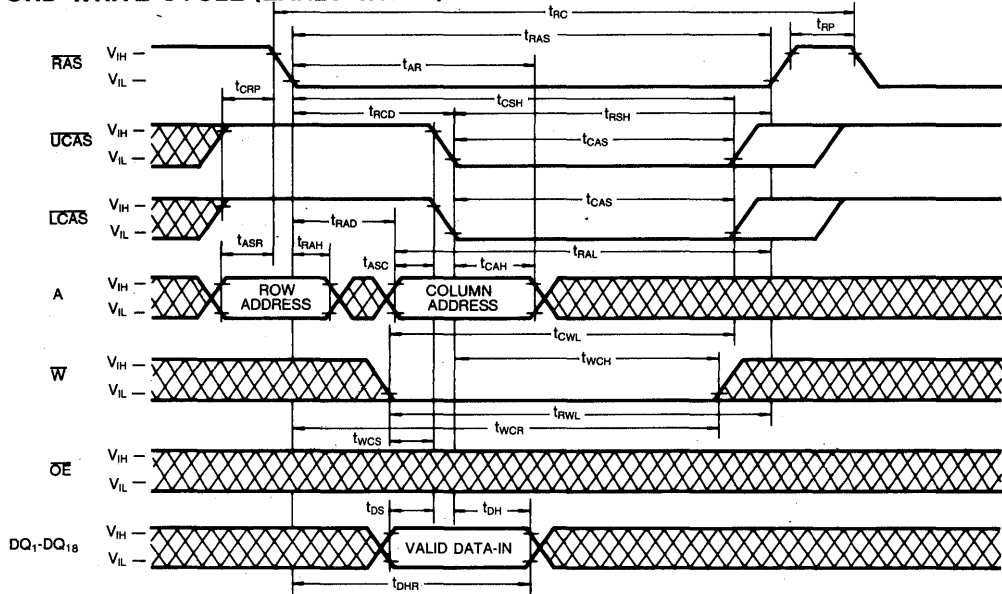
UPPER BYTE READ CYCLE



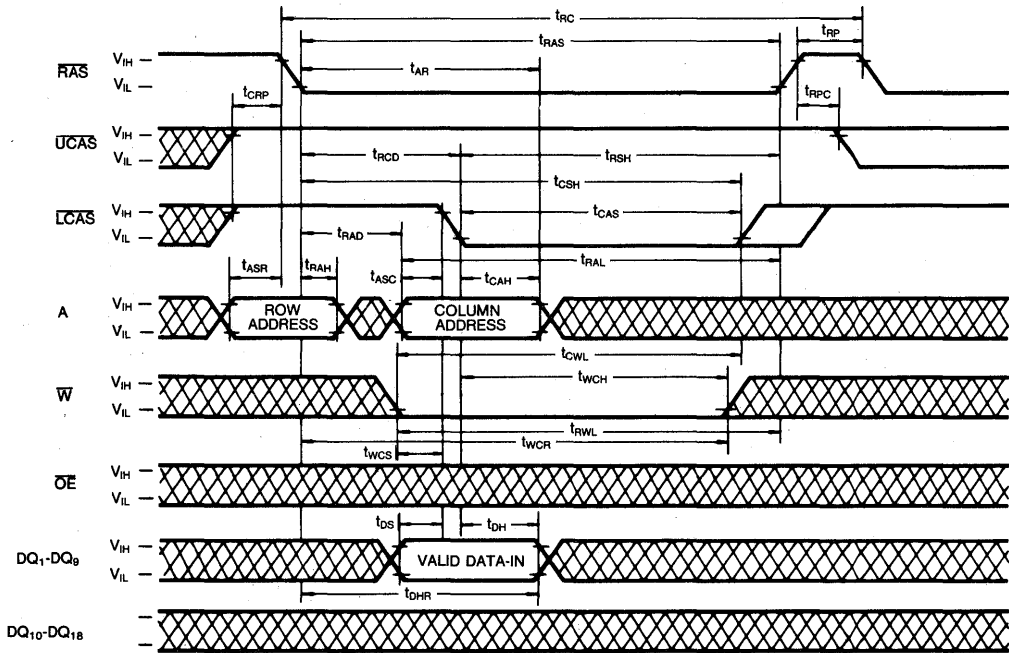
 DON'T CARE

TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



LOWER BYTE WRITE CYCLE (EARLY WRITE)

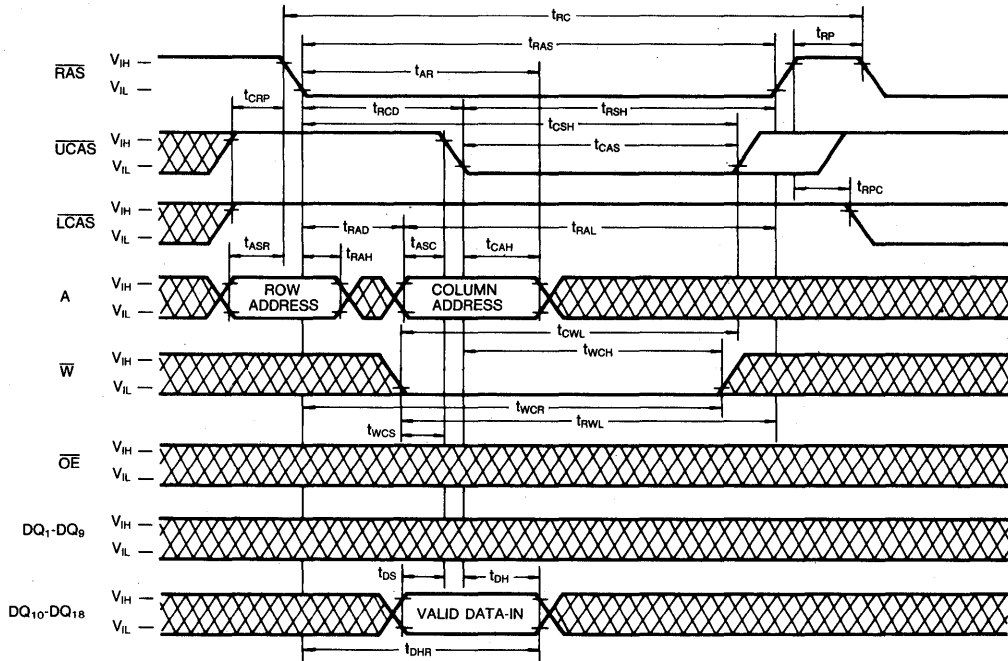


 DONT CARE

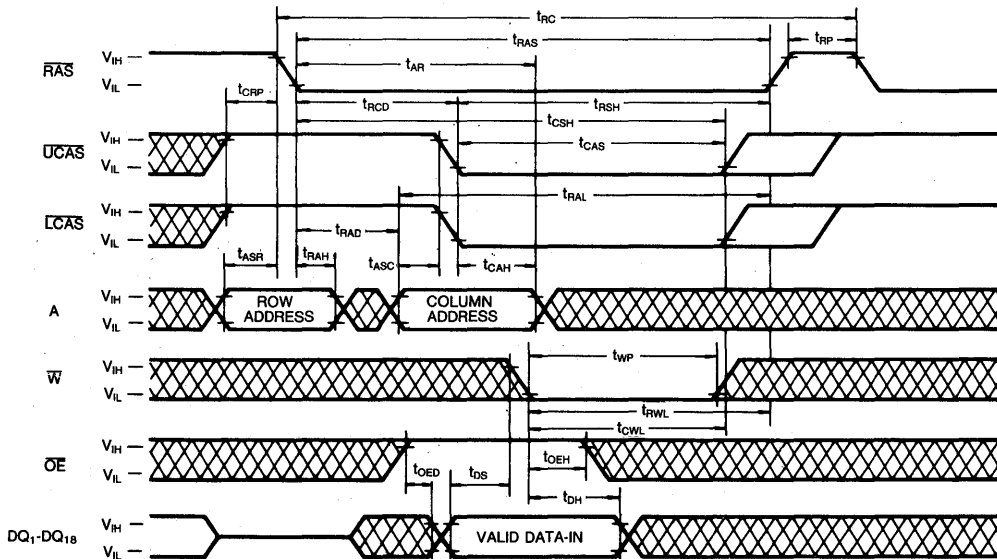
4

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



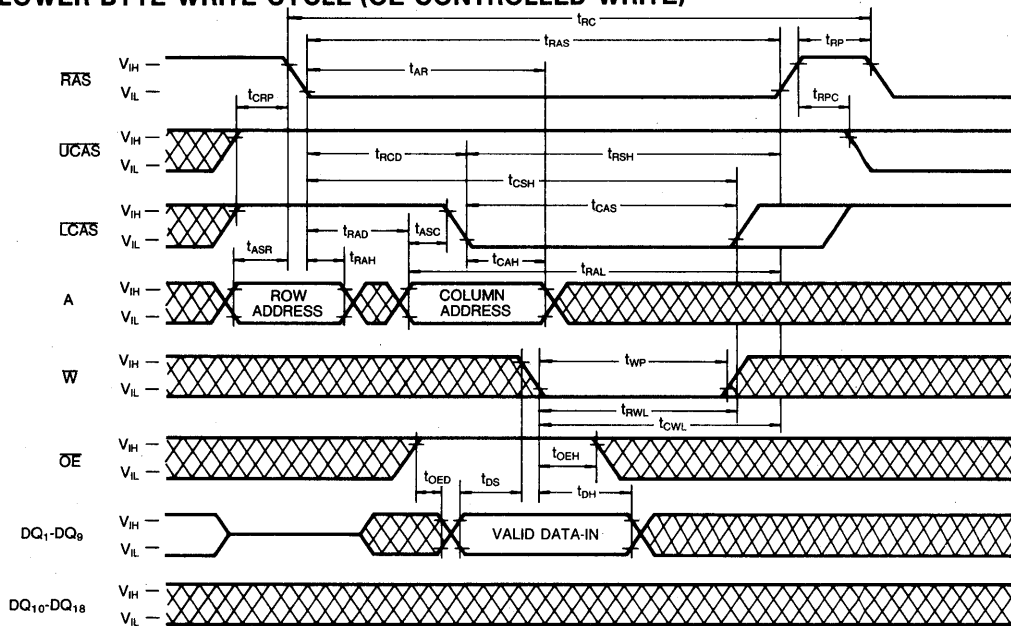
WORD WRITE CYCLE (OE CONTROLLED WRITE)



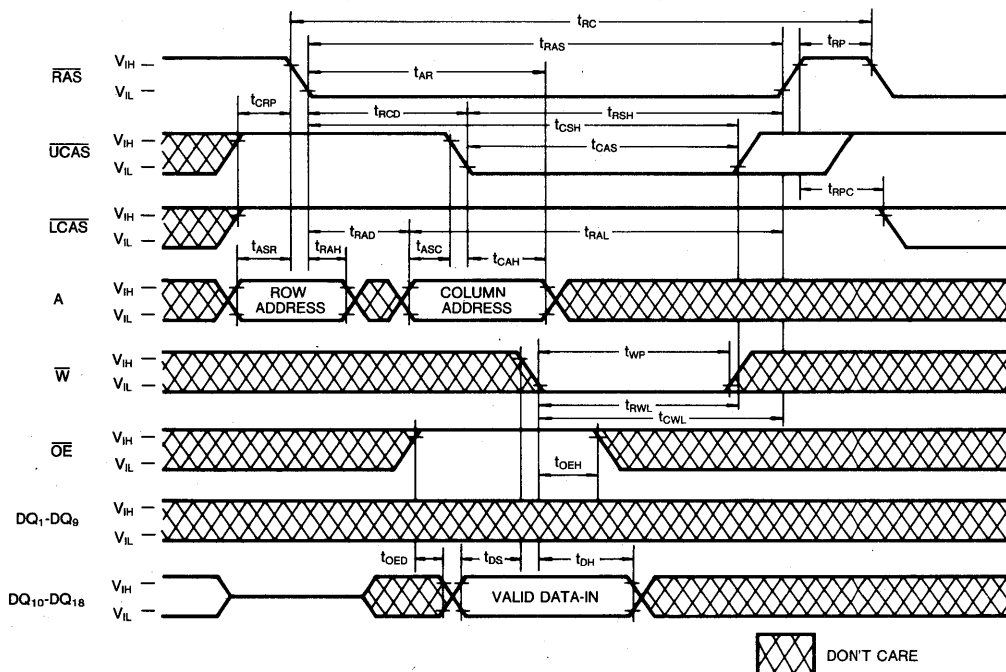
 DON'T CARE

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



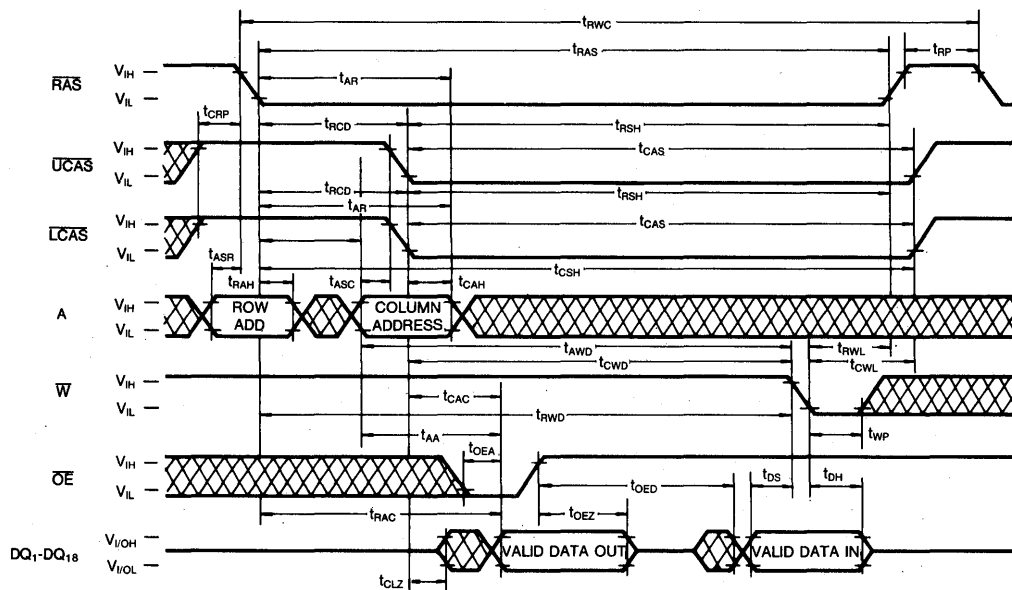
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



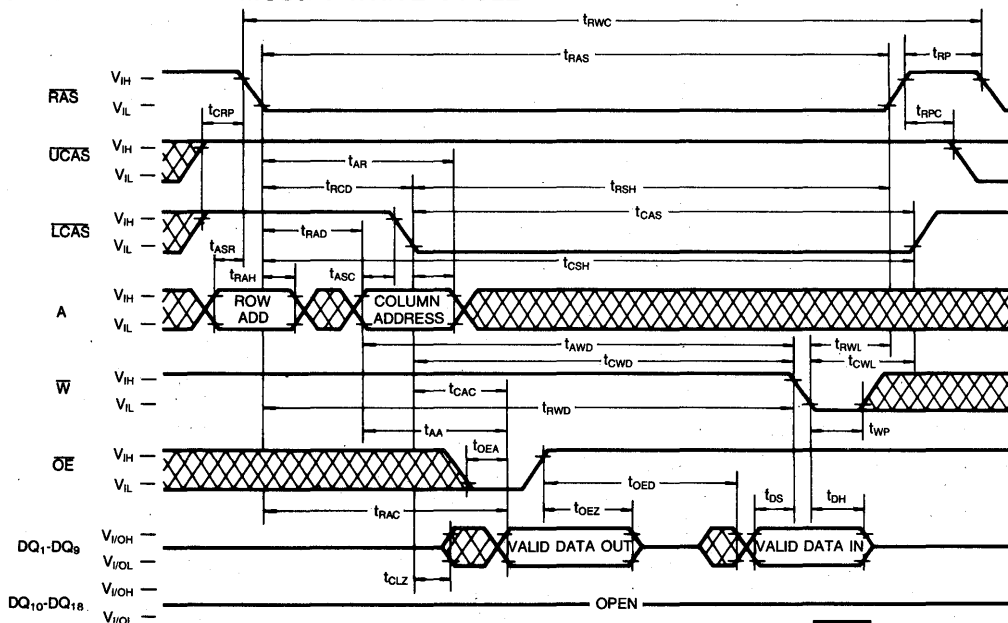
4

TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE



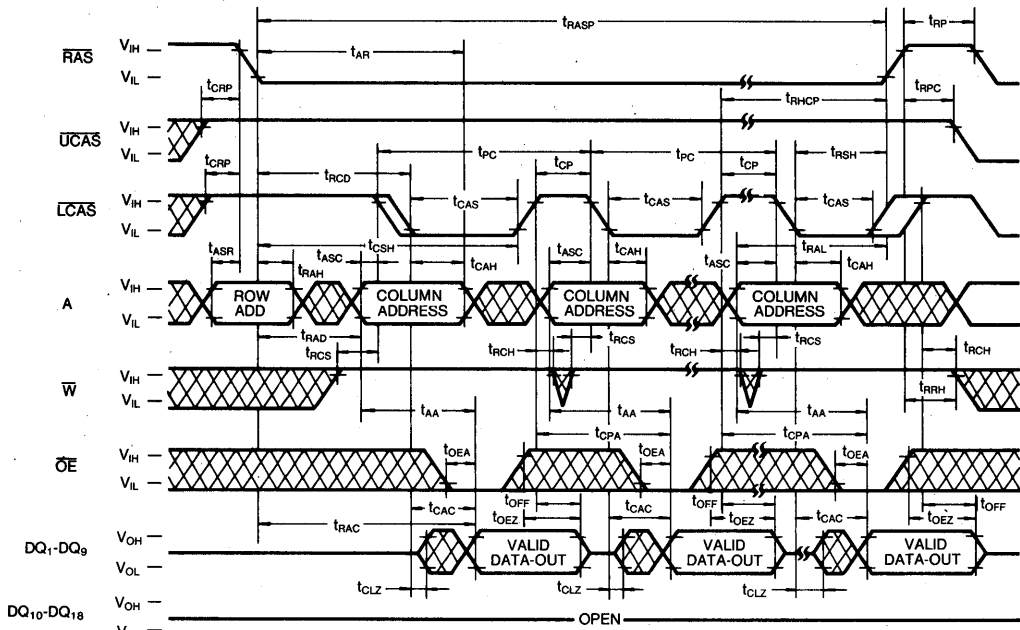
LOWER-BYTE READ-MODIFY-WRITE CYCLE



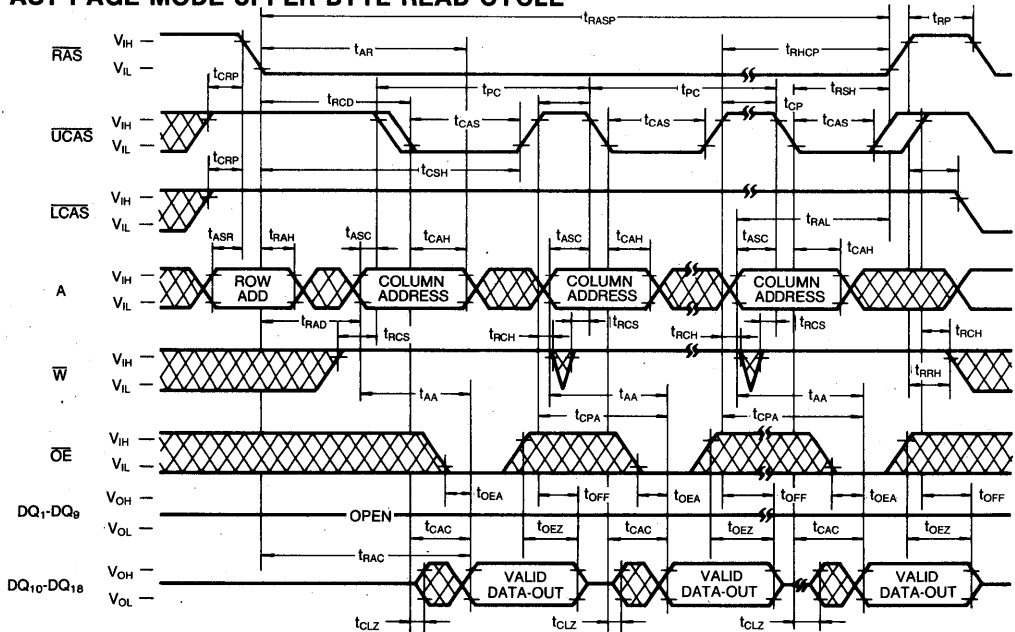
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



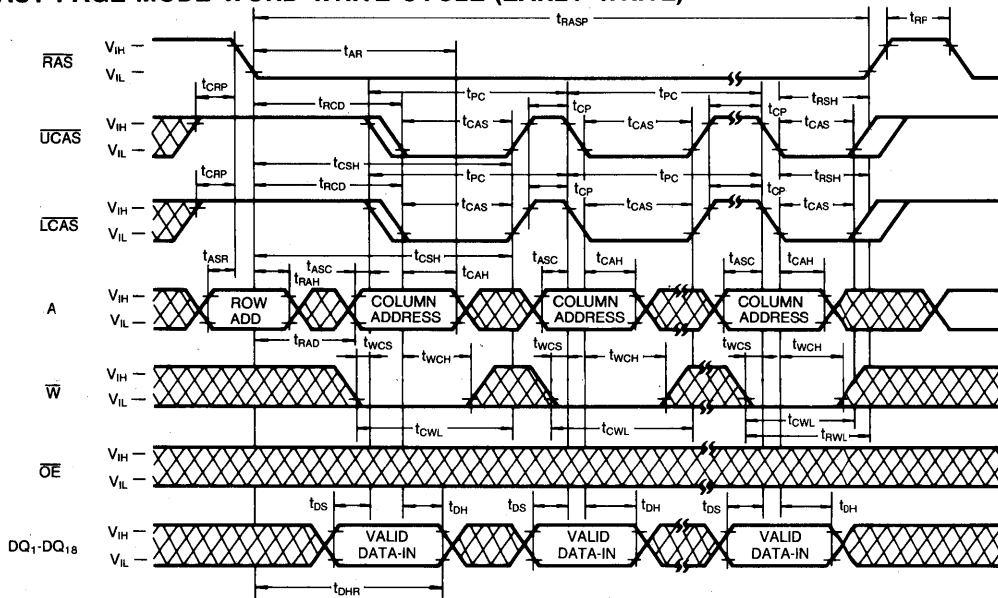
FAST PAGE MODE UPPER BYTE READ CYCLE



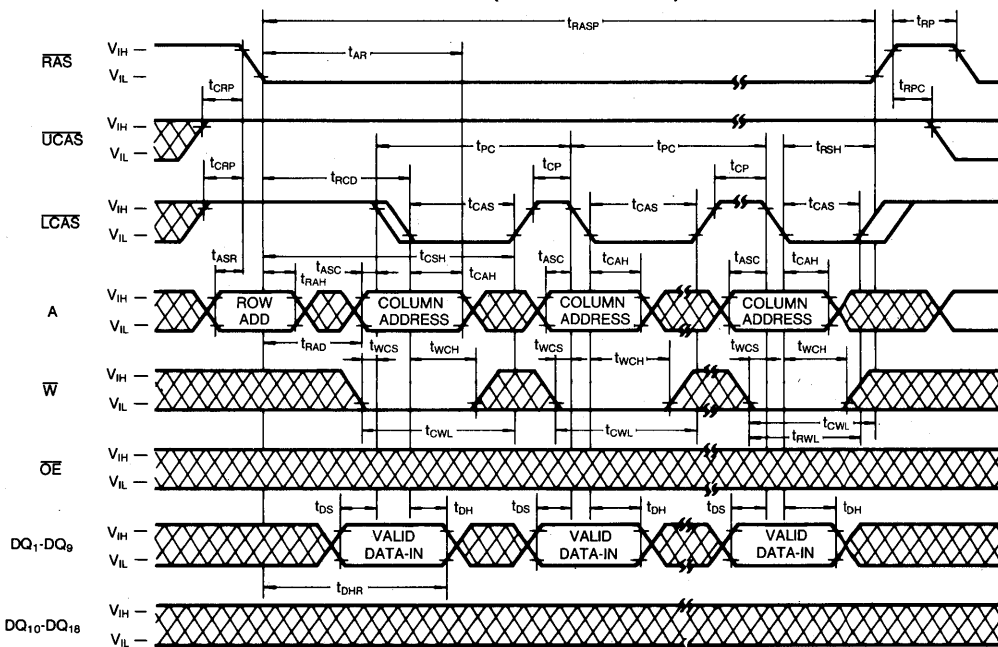
 DONT CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



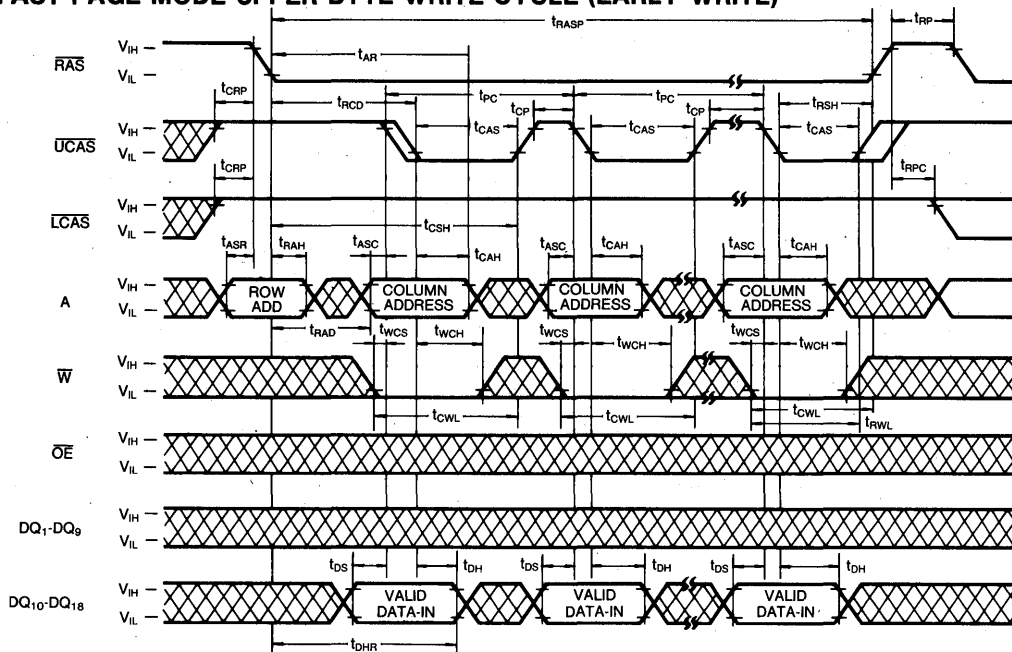
FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)



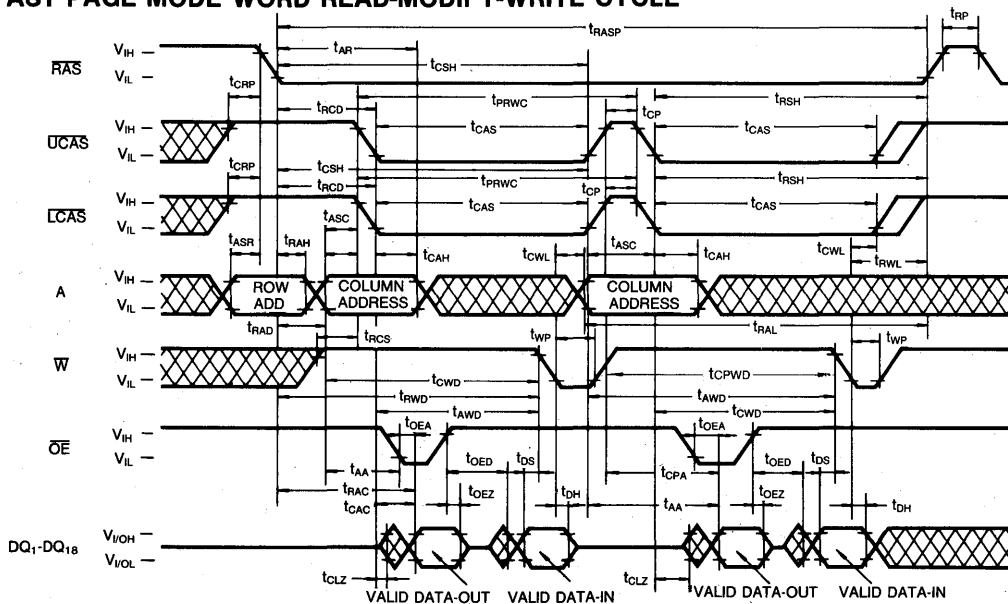
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



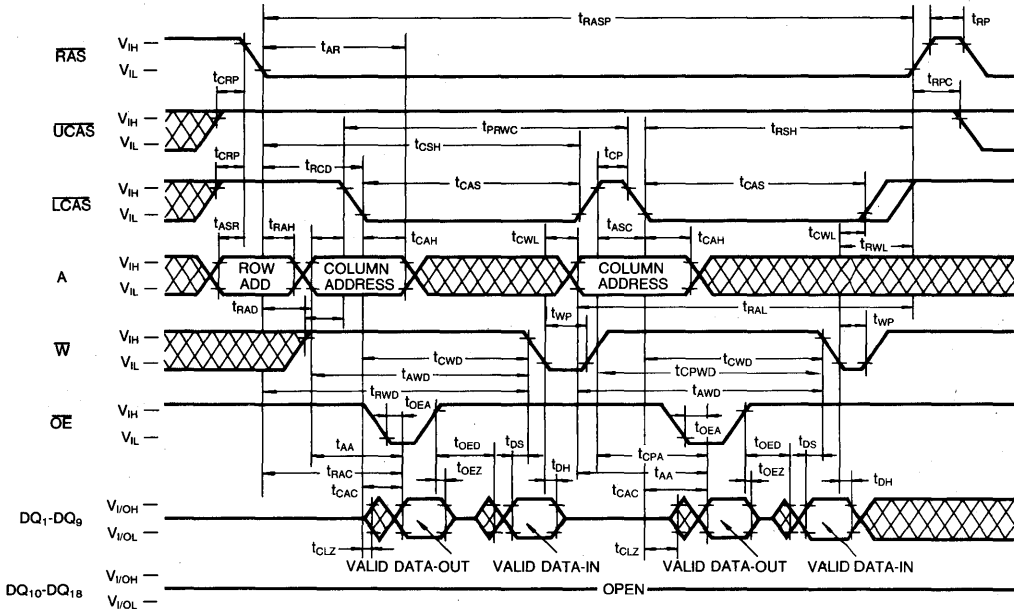
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



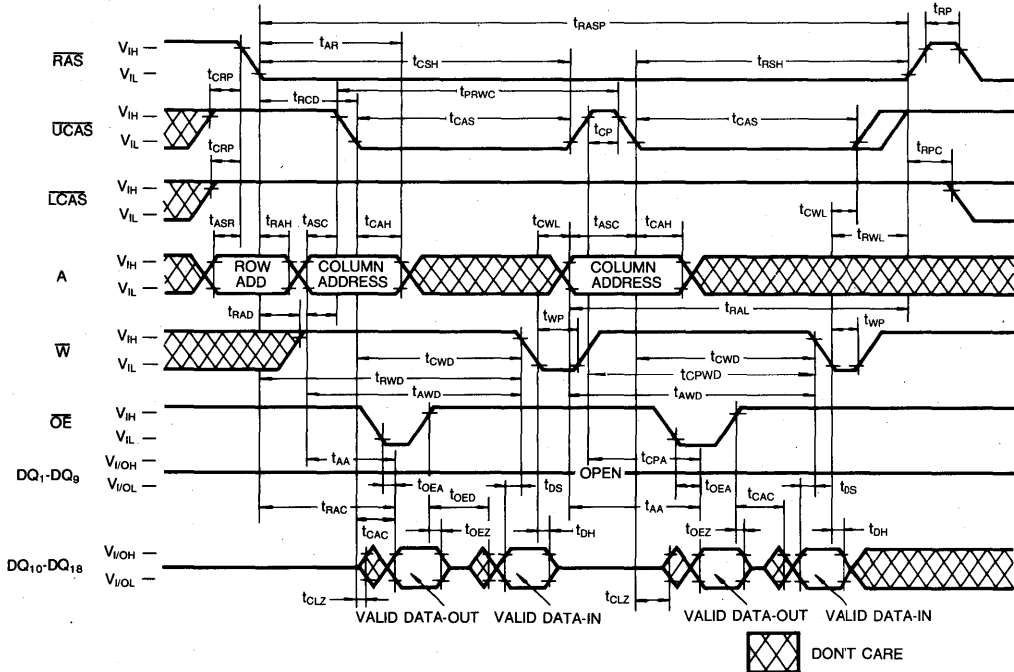
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ-MODIFY-WRITE CYCLE



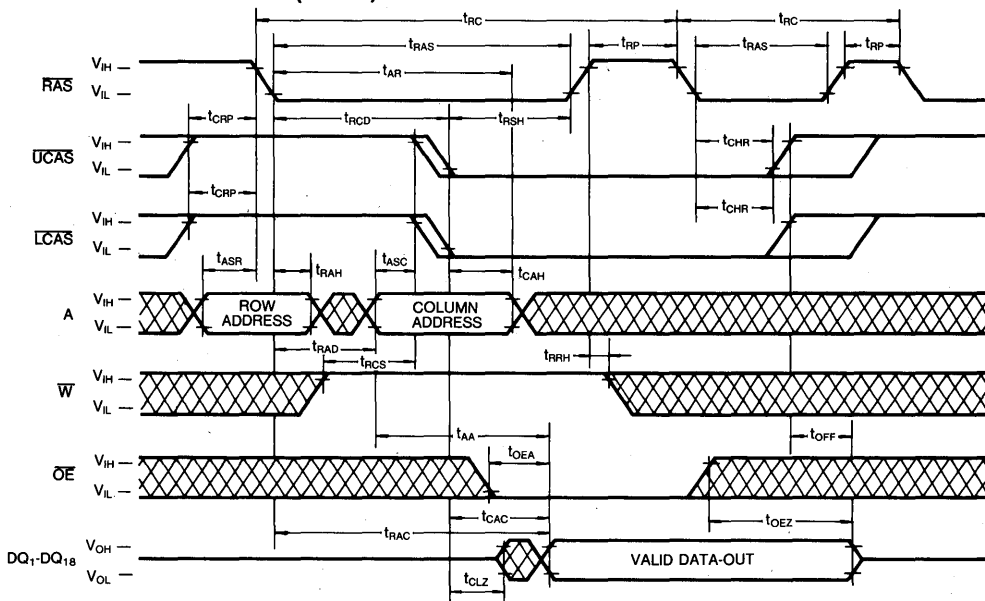
FAST PAGE MODE UPPER BYTE READ-MODIFY-WRITE CYCLE



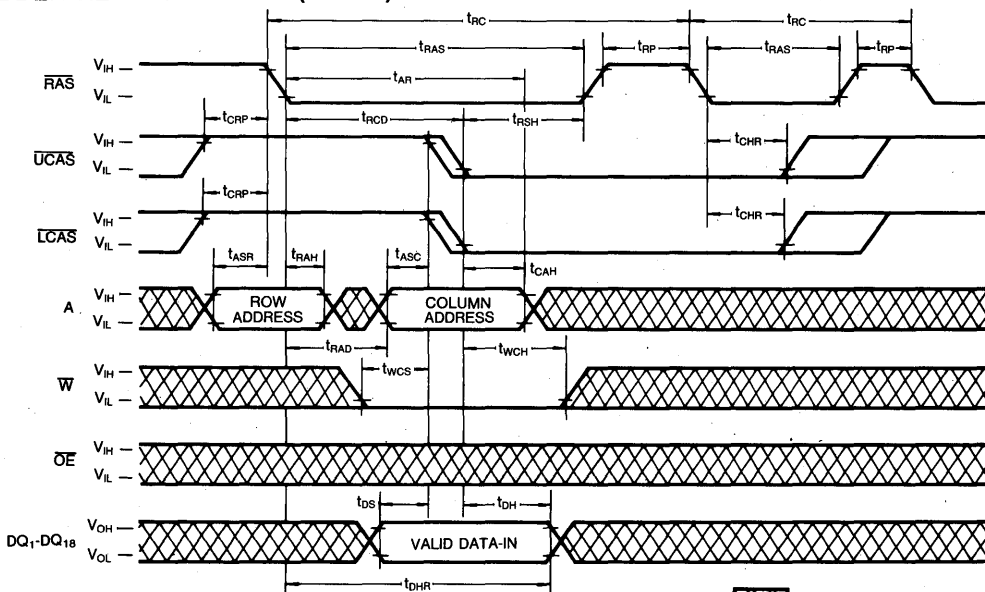
4

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



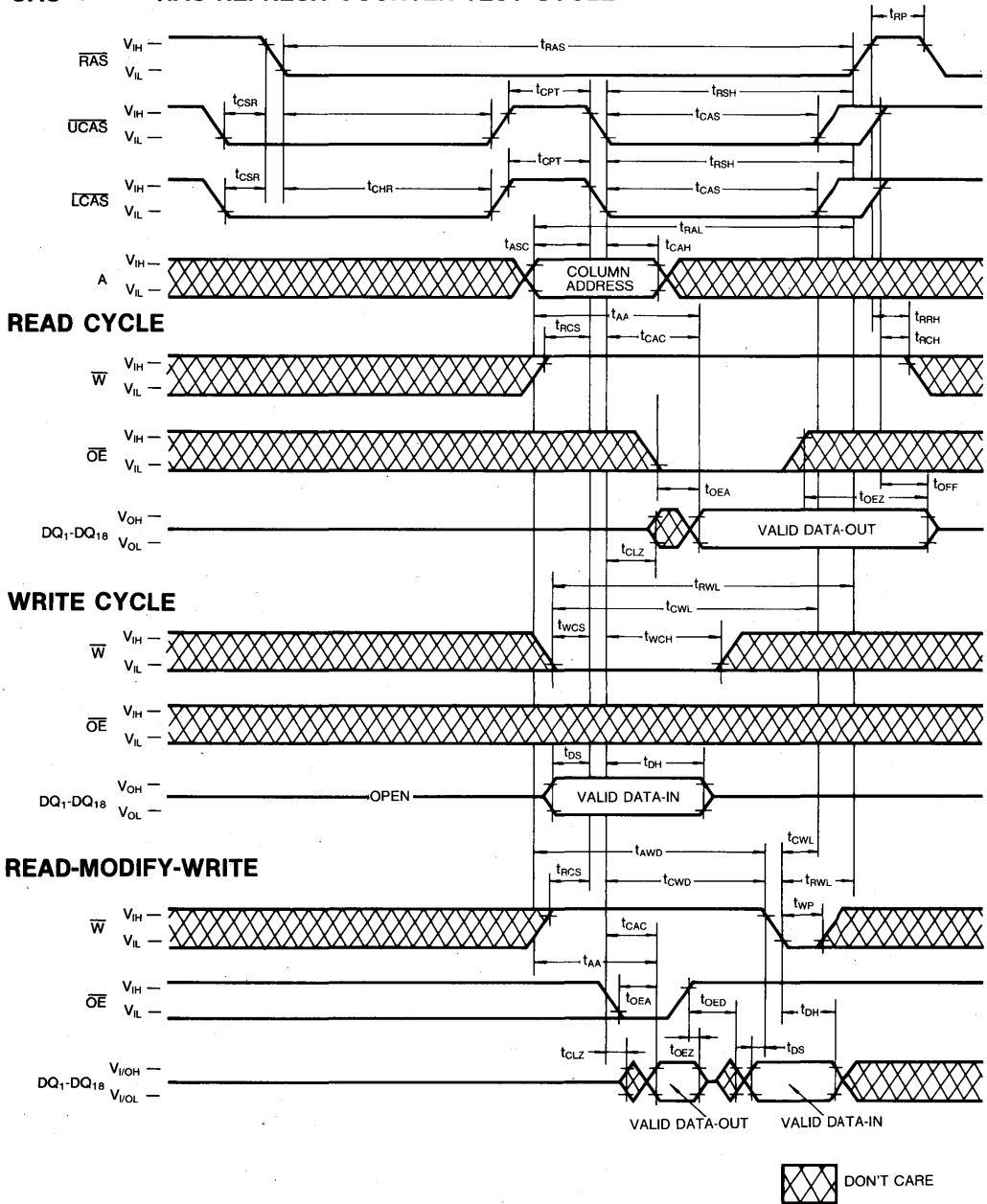
HIDDEN REFRESH CYCLE (WRITE)



 DON'T CARE

TIMING DIAGRAMS (Continued)

CAS-before-RAS REFRESH COUNTER TEST CYCLE

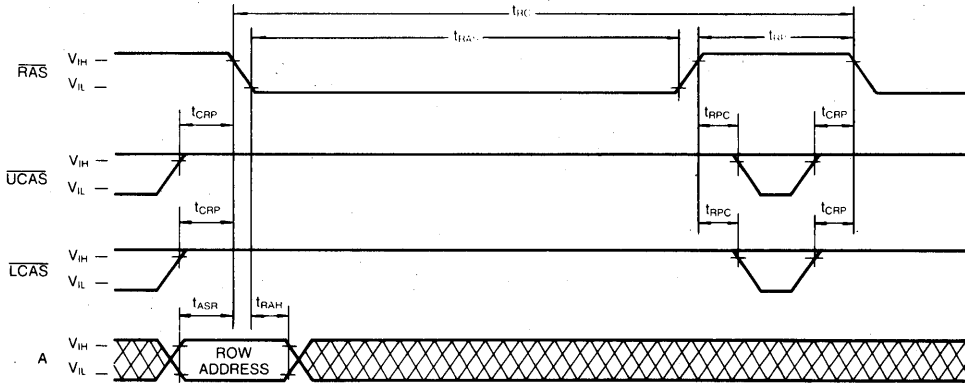


4

TIMING DIAGRAMS (Continued)

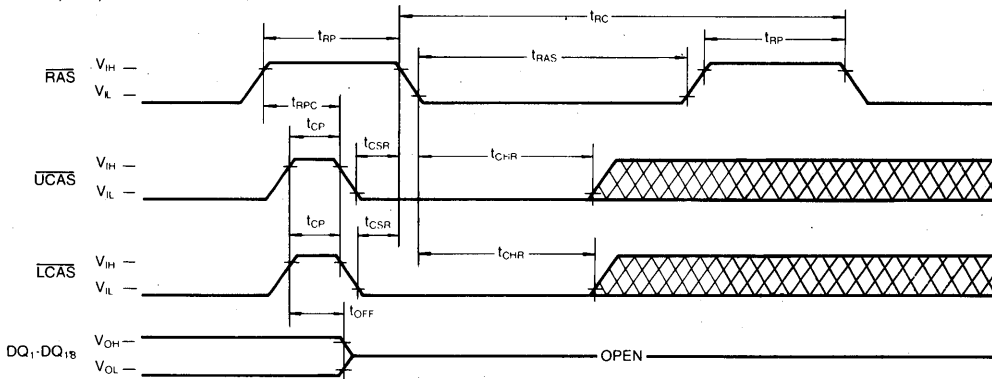
RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care



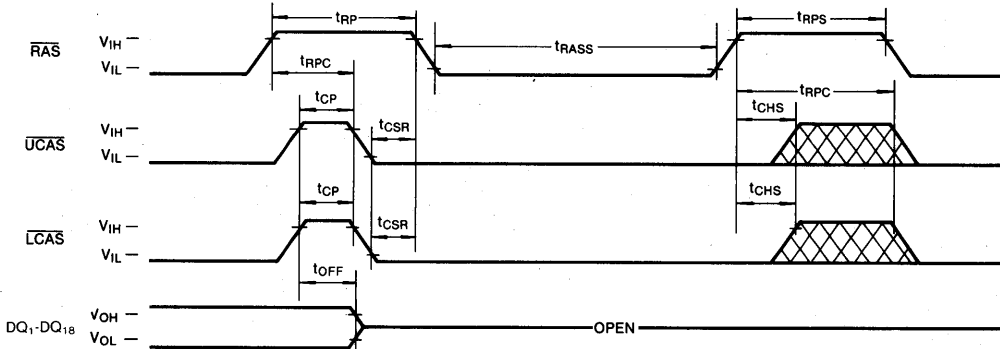
CAS-before-RAS REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} , A = Don't Care



CAS-before-RAS SELF REFRESH CYCLE (Self refresh only)

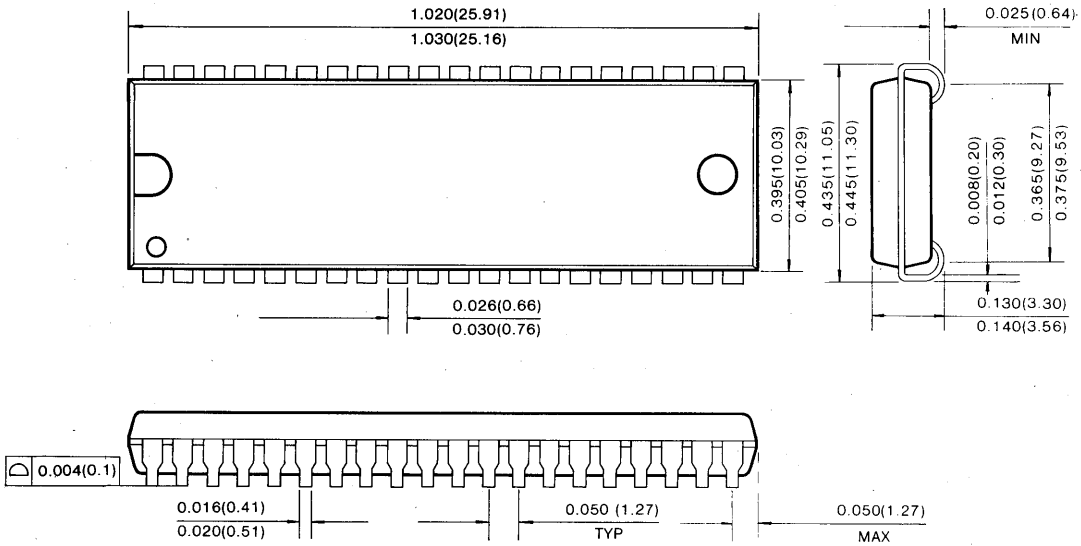
NOTE: \bar{W} , \bar{OE} , A = Don't Care



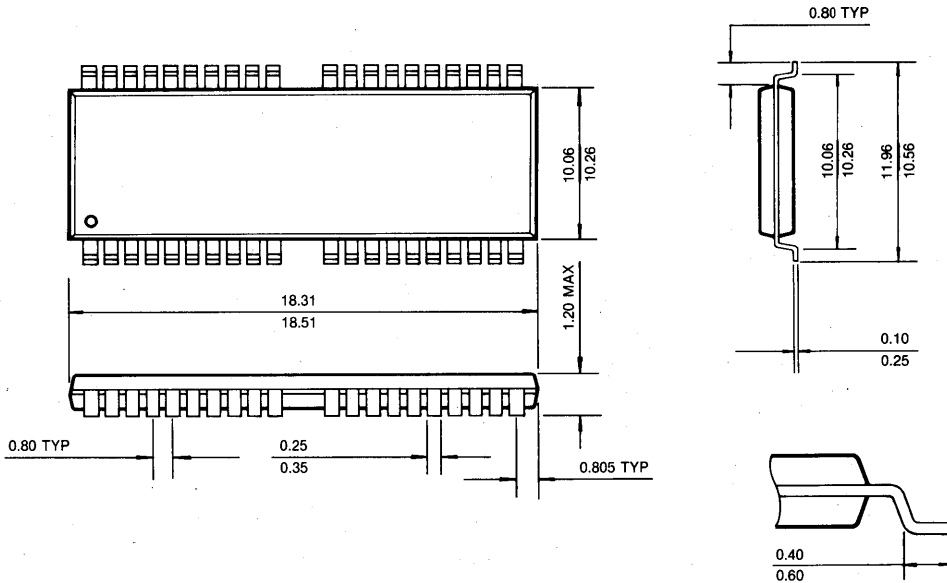
 DON'T CARE

PACKAGE DIMENSION
40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



4

512K × 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM48V512B/BL/BLL-6	60ns	15ns	110ns
KM48V512B/BL/BLL-7	70ns	20ns	130ns
KM48V512B/BL/BLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refresh operation (LL-version)
- Byte Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Dual +3.3V ± 0.3V power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/128ms (LL-version)
- Power Dissipation
 - Standby: 1.8mW (Normal)
 - 0.36mW (L-version)
 - 0.36mW (LL-version)
 - Active (60/70/80): 255/235/220mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

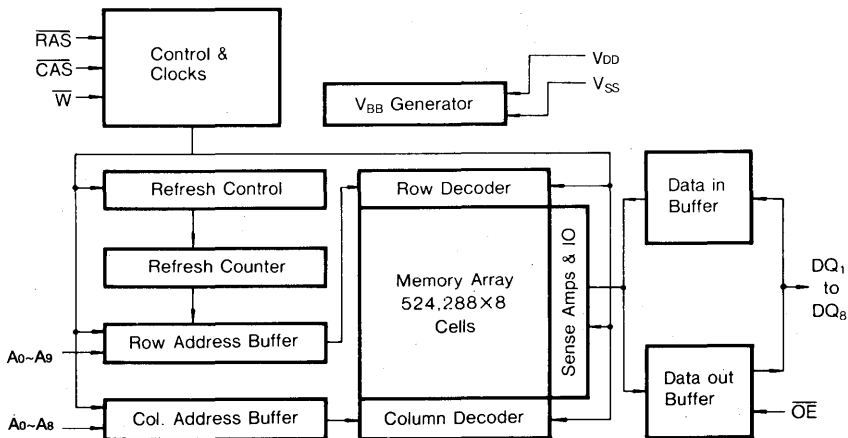
GENERAL DESCRIPTION

The Samsung KM48V512B/BL/BLL is a CMOS high speed 524,288 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48V512B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

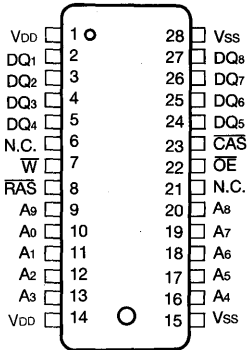
The KM48V512B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



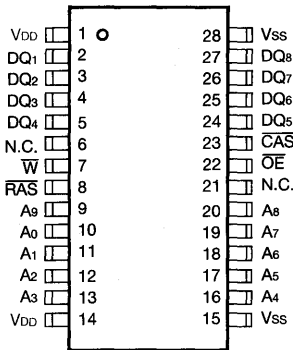
PIN CONFIGURATION (Top Views)

• KM48V512BJ/BLJ/BLLJ



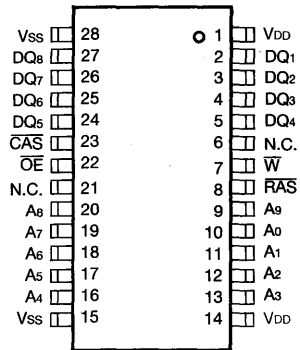
(SOJ)

• KM48V512BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM48V512BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-8	Data In/Out
VSS	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD}	-0.5 to 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{os}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} , \overline{CAS} , Address Cycling @trc=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I _{CC1}	-	70 65 60 mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)		I _{CC2}	-	1 mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address Cycling @trc=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I _{CC3}	-	70 65 60 mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @tpc=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I _{CC4}	-	55 50 45 mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{DD}-0.2V$)	KM48V512B KM48V512BL KM48V512BLL	I _{CC5}	-	500 100 100 μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM48V512B/BL/BLL-6 KM48V512B/BL/BLL-7 KM48V512B/BL/BLL-8	I _{CC6}	-	70 65 60 mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{CAS}=0.2V$ D _{IN} =Don't Care, T _{RC} =125 μS T _{RA} S=T _{RA} S min.~300ns	KM48V512BL	I _{CC7}	-	200 μA
Self Refresh Current $\overline{RAS}=\overline{CAS}=0.2V$ $\overline{W}=\overline{OE}=\overline{A_0}-\overline{A_9}=V_{DD}-0.2V$ or 0.2V DQ ₁ -DQ ₈ =V _{DD} -0.2V, 0.2V or Open	KM48V512BLL	I _{CC8}	-	100 μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 V)	$I_{(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC8} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4} , address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 - A_9$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Input Capacitance ($DQ_1 - DQ_8$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	

AC CHARACTERISTICS (Continued)

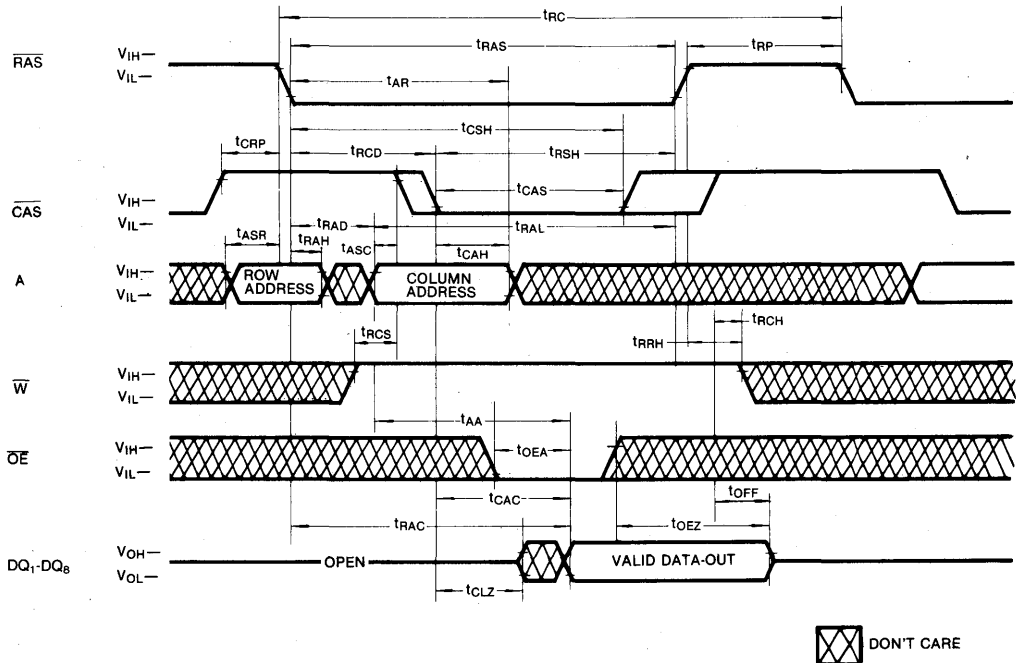
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to \overline{RAS}	tAR	50		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to \overline{RAS}	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		20		ns	
Write command to \overline{CAS} lead time	tCWL	15		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
Data hold time referenced to \overline{RAS}	tDHR	50		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (LL-version)	tREF		128		128		128	ms	
\overline{CAS} to \overline{W} delay time	tCWD	40		50		50		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	85		95		105		ns	8
Column address to \overline{W} delay time	tAWD	55		60		65		ns	8
\overline{CAS} precharge to \overline{W} delay time	tCPWD	60		65		70		ns	
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		10		ns	
\overline{RAS} precharge to \overline{CAS} hold time	tRPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} - \overline{B} - \overline{R} counter test cycle)	tCPT	20		25		30		ns	
Access time from \overline{CAS} precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
\overline{RAS} pulse width (Fast Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	tRHCP	35		40		45		ns	
\overline{CAS} precharge time (Fast Page mode)	tCP	10		10		10		ns	
Access time from \overline{OE}	tOEA		15		20		20	ns	
\overline{OE} to data-in delay time	tOED	15		20		20		ns	
Out put buffer turn off delay time from \overline{OE}	tOEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	tOEH	15		20		20		ns	
\overline{RAS} pulse width (\overline{C} - \overline{B} - \overline{R} self refresh)	tRASS	100		100		100		μ s	12
\overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} self refresh)	tRPS	110		130		150		ns	12
\overline{CAS} hold time (\overline{C} - \overline{B} - \overline{R} self refresh)	tCHS	-50		-50		-50		ns	12

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF, $V_{OH}=2.0V$ and $V_{OL}=0.8V$
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}}(\text{max})$.
7. $t_{\text{OFF}}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} to V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. 1024 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification. (LL-version)

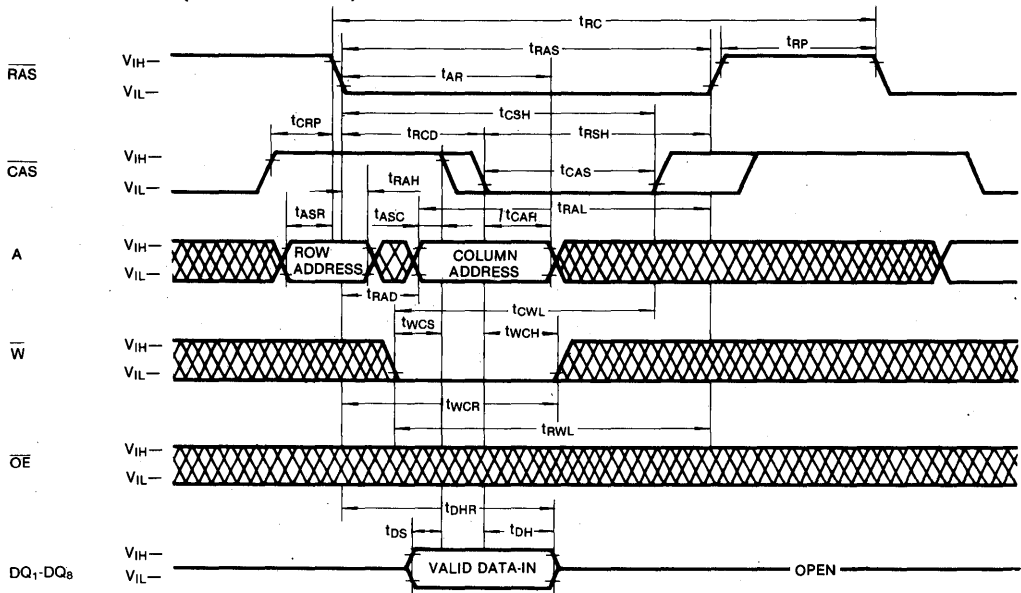
TIMING DIAGRAMS

READ CYCLE

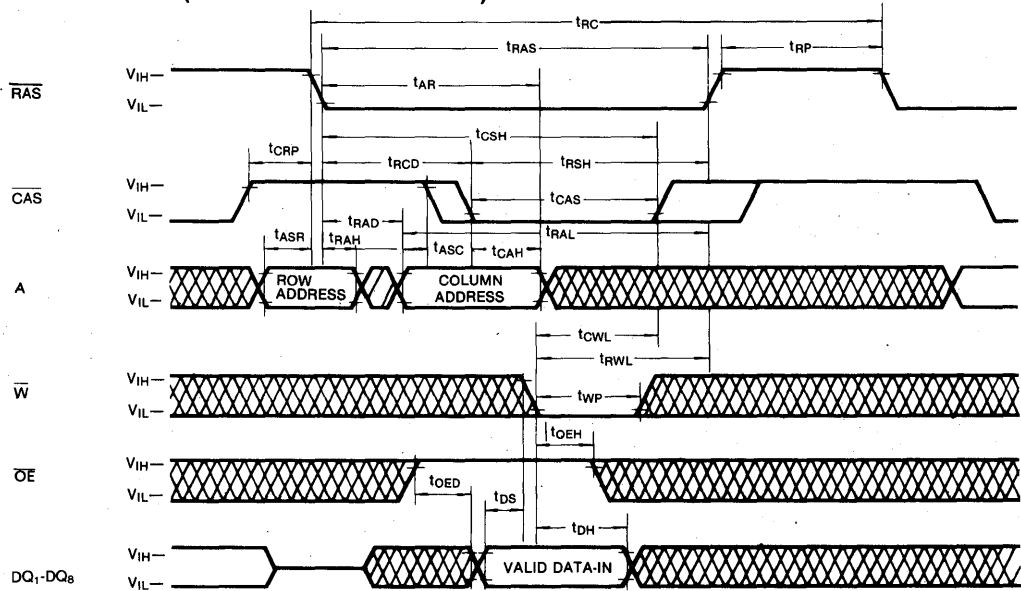


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



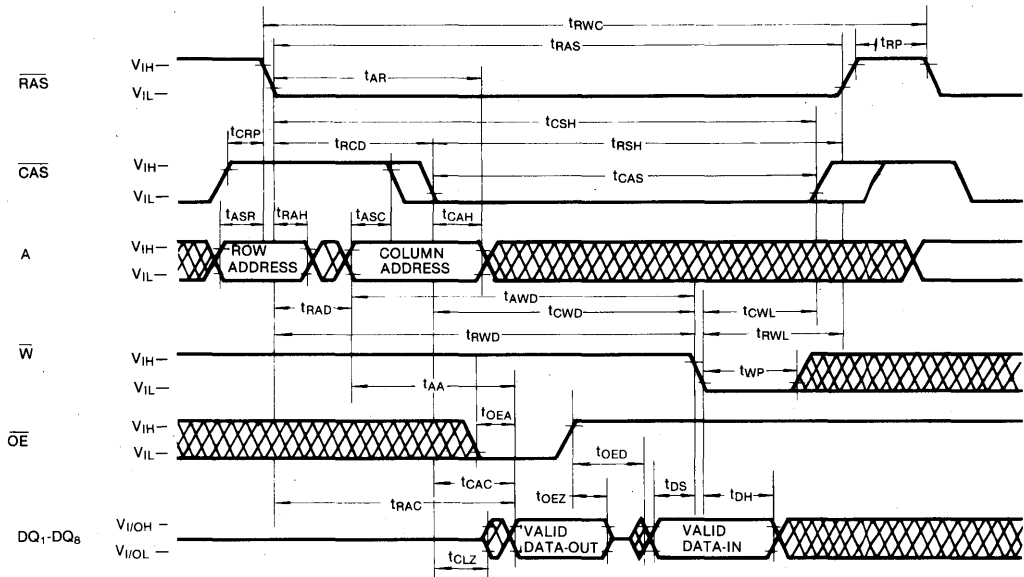
WRITE CYCLE (OE CONTROLLED WRITE)



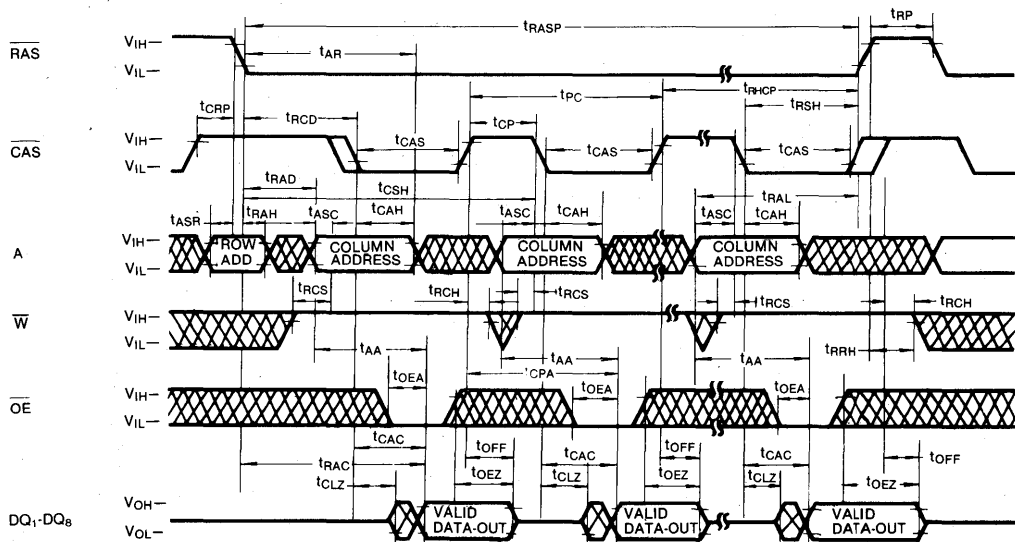
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

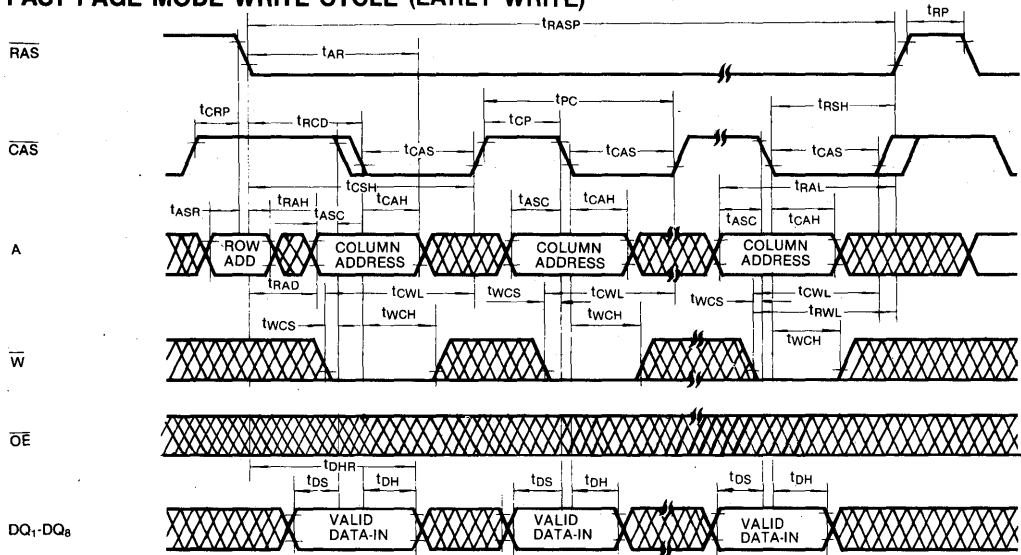


 DON'T CARE

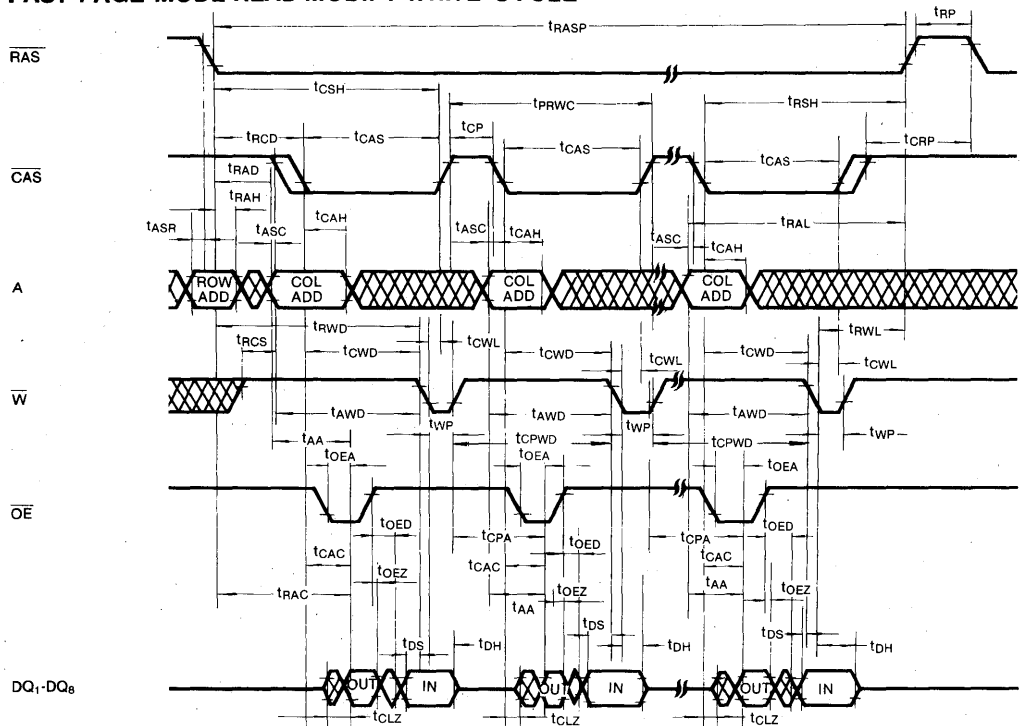
4

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

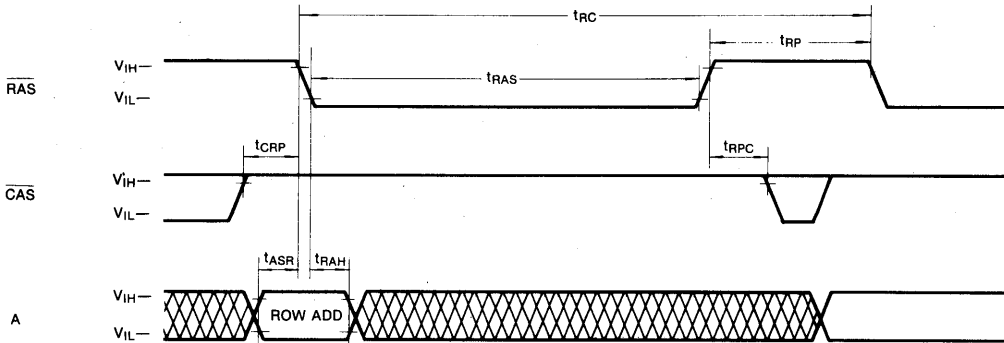


DON'T CARE

TIMING DIAGRAMS (Continued)

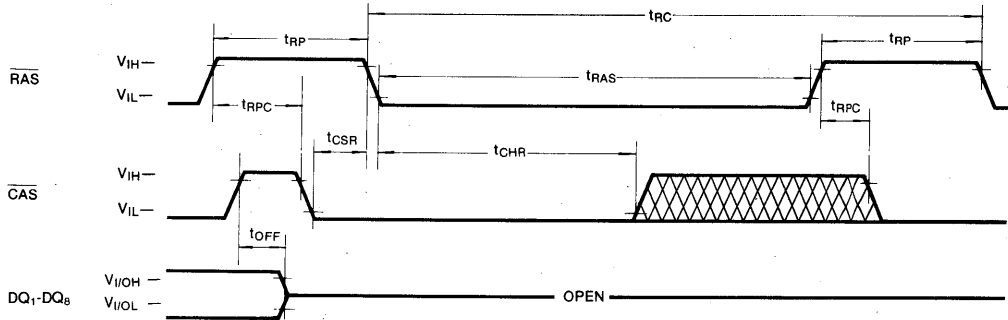
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} = Don't care



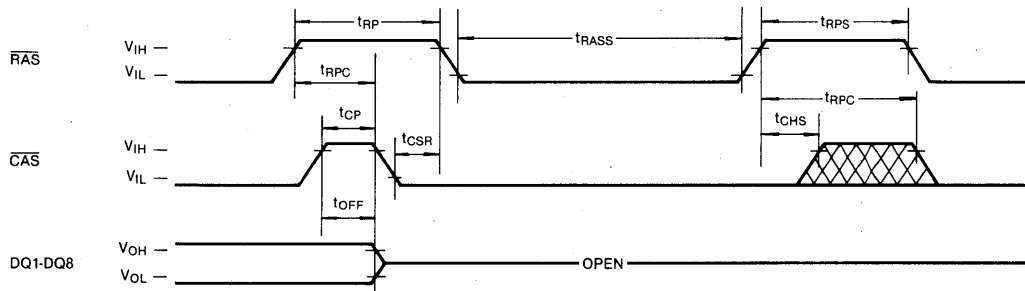
CAS-before-RAS REFRESH CYCLE

NOTE: \overline{W} , \overline{OE} , A=Don't Care



CAS-before-RAS SELF REFRESH CYCLE

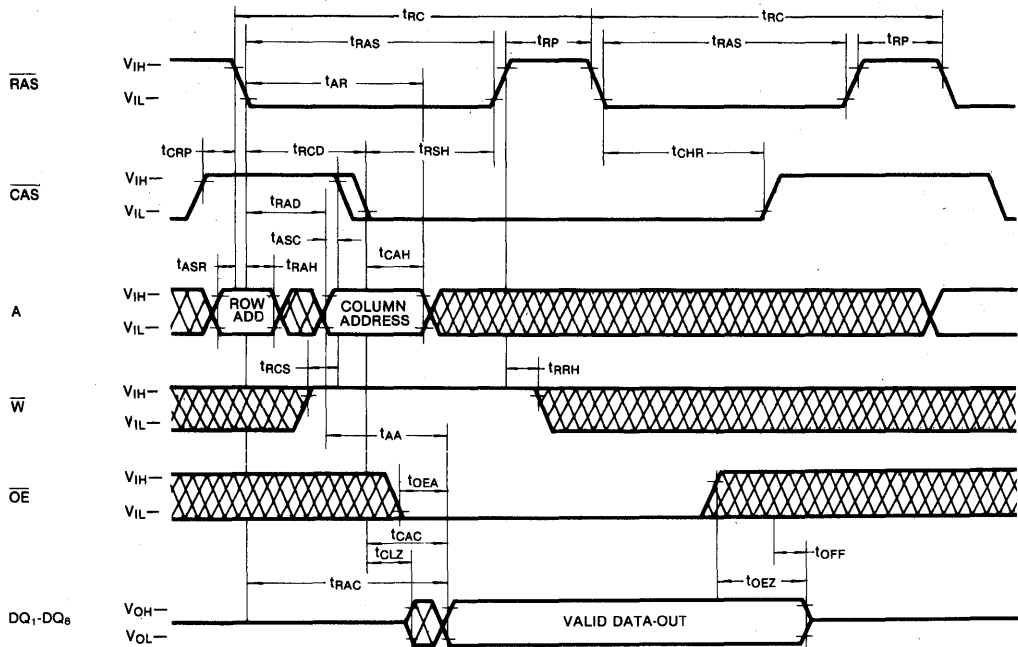
NOTE: \overline{W} , \overline{OE} , A = Don't Care



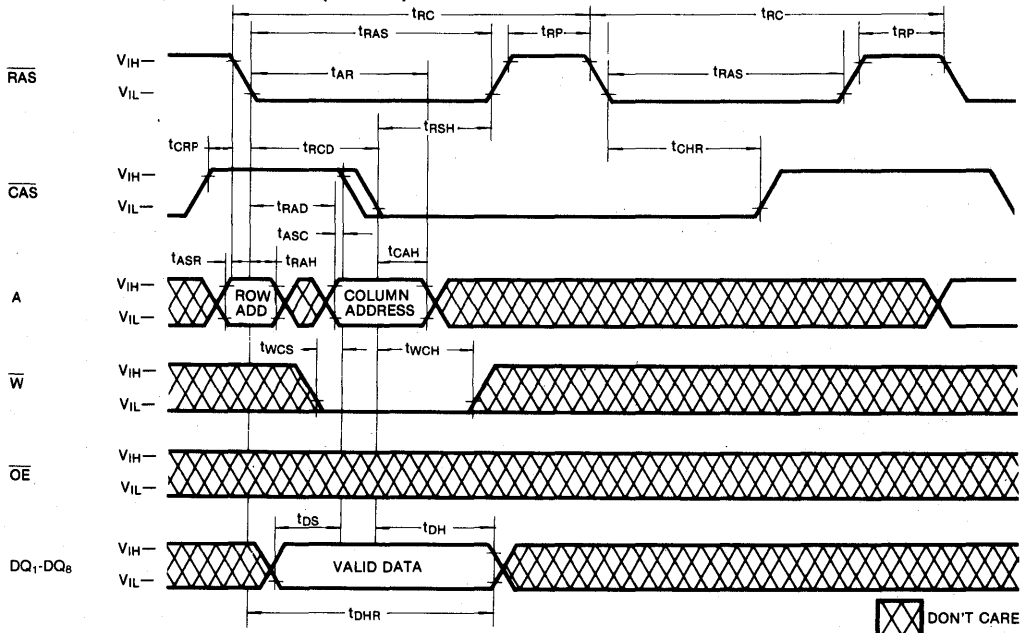
 DON'T CARE


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

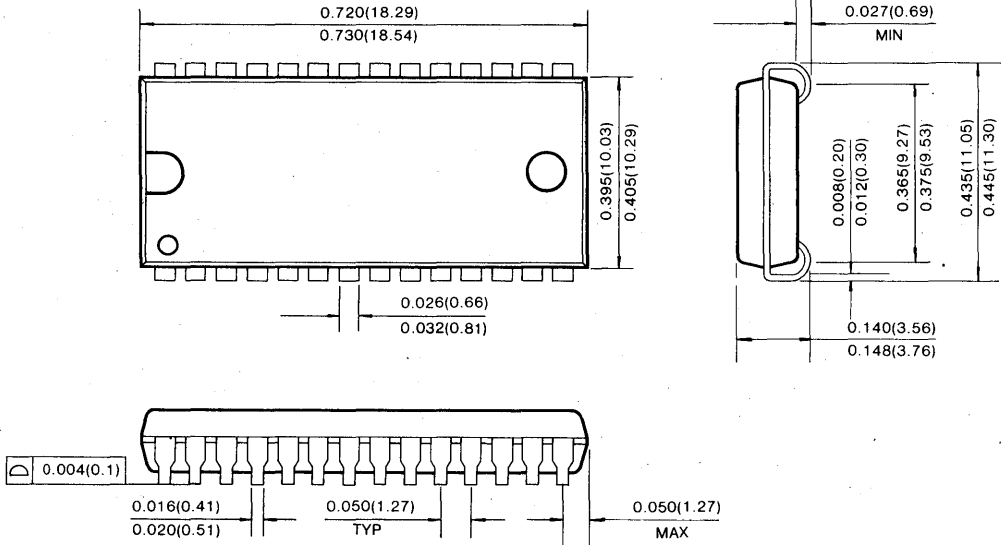


 DON'T CARE

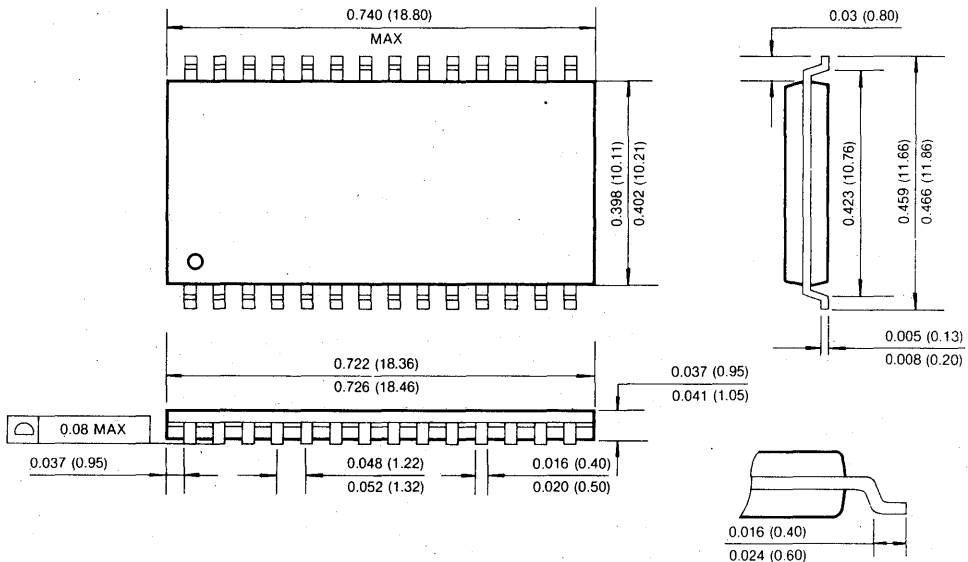
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



512K × 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trC	tHPC
KM48V514B/BL/BLL-6	60ns	17ns	110ns	24ns
KM48V514B/BL/BLL-7	70ns	20ns	130ns	29ns
KM48V514B/BL/BLL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended Data Out
- Self Refresh operation (LL-version)
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Byte Read/write operation
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Dual +3.3V ± 0.3V power supply
- Refresh Cycle
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L/LL-ver)
- Power Dissipation
 - Standby : 1.8mW (Normal)
 - 0.36mW (L-Version)
 - 0.36mW (LL-version)
- Active (60/70/80) : 255/235/220mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

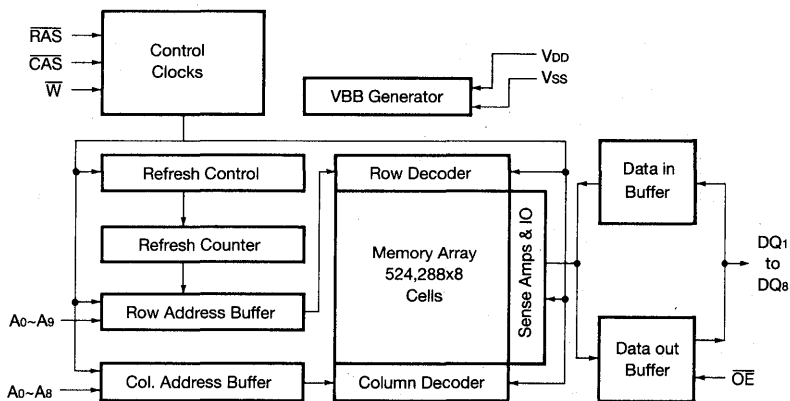
GENERAL DESCRIPTION

The Samsung KM48V514B/BL/BLL is a CMOS high speed 524,288 × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM48V514B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

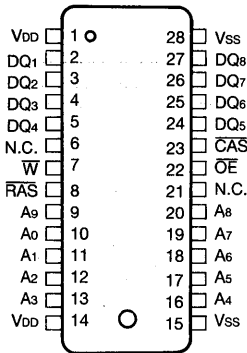
The KM48V514B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



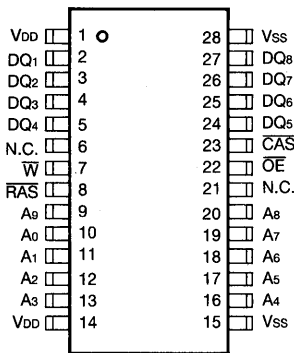
PIN CONFIGURATION (Top Views)

• KM48V514BJ/BLJ/BLLJ



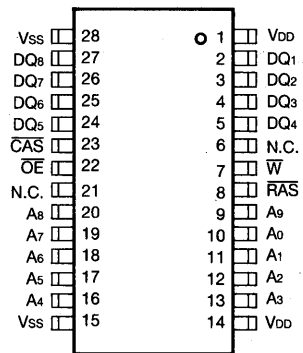
(SOJ)

• KM48V514BT/BLT/BLLT



(TSOP(II)-Forward Type)

• KM48V514BTR/BLTR/BLLTR



(TSOP(II)-Reverse Type)

Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-8	Data In/Out
VSS	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5-4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD}	-0.5-4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (R _{AS} , C _{AS} , Address Cycling @trc=min.)	KM48V514B/BL/BLL-6 KM48V514B/BL/BLL-7 KM48V514B/BL/BLL-8 I _{CC1}	-	70 65 60	mA mA mA
Standby Current (R _{AS} =C _{AS} =W=V _{IH})	I _{CC2}	-	1	mA
R _{AS} -Only Refresh Current* (C _{AS} =V _{IH} , R _{AS} , Address Cycling @trc=min.)	KM48V514B/BL/BLL-6 KM48V514B/BL/BLL-7 KM48V514B/BL/BLL-8 I _{CC3}	-	70 65 60	mA mA mA
EDO Mode Current* (R _{AS} =V _{IL} , C _{AS} , Address Cycling @tpc=min.)	KM48V514B/BL/BLL-6 KM48V514B/BL/BLL-7 KM48V514B/BL/BLL-8 I _{CC4}	-	55 50 45	mA mA mA
Standby Current (R _{AS} =C _{AS} =W=V _{DD} -0.2V)	KM48V514B KM48V514BL KM48V514BLL I _{CC5}	-	500 100 100	μA μA μA
C _{AS} -Before-R _{AS} Refresh Current* (R _{AS} and C _{AS} Cycling @trc=min.)	KM48V514B/BL/BLL-6 KM48V514B/BL/BLL-7 KM48V514B/BL/BLL-8 I _{CC6}	-	70 65 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V Input Low Voltage(V _{IL})=0.2V C _{AS} =0.2V DIN=Don't Care, TRC=125μS TRAS=TRAS min.-300ns	KM48V514BL I _{CC7}	-	200	μA
Self Refresh Current R _{AS} =C _{AS} =0.2V W=OE=A0-A9=V _{DD} -0.2V or 0.2V DQ1-DQ8=V _{DD} -0.2V, 0.2V or Open	KM48V514BLL I _{CC8}	-	100	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	$I_{(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{o(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4} , address can be changed maximum once within one hyper page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 \sim A_9$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Input Capacitance ($DQ_1 \sim DQ_8$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from \overline{RAS}	trac		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	3		3		3		ns	3
Turn-off delay from \overline{CAS}	tCEZ	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	trp	40		50		60		ns	
\overline{RAS} pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	trSH	17		20		20		ns	
\overline{CAS} hold time	tcSH	50		60		70		ns	
\overline{CAS} pulse width	tcAS	10	10,000	15	10,000	20	10,000	ns	12
\overline{RAS} to \overline{CAS} delay time	trCD	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	trAD	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tcRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	trAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to \overline{RAS}	tAR	50		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to \overline{RAS}	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		20		ns	
Write command to \overline{CAS} lead time	tCWL	15		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
Data hold time referenced to \overline{RAS}	tDHR	50		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh Period(L & LL-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	tCWD	42		50		50		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	85		95		105		ns	8
Column address to \overline{W} delay time	tAWD	55		60		65		ns	8
\overline{CAS} precharge to \overline{W} delay time	tCPWD	60		65		70		ns	
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		10		ns	
\overline{RAS} to \overline{CAS} precharge time	tRPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} -B- \overline{R} counter test cycle)	tCPT	20		25		30		ns	
Access time from \overline{CAS} precharge	tCPA		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
\overline{CAS} precharge time (Hyper Page mode)	tCP	10		10		10		ns	
\overline{RAS} pulse width (Hyper Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	tRHCP	35		40		45		ns	
\overline{OE} access time	tOEA		15		20		20	ns	
\overline{OE} to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	3	15	3	20	3	20	ns	7
\overline{OE} command hold time	tOEH	15		20		20		ns	
\overline{OE} to output in Low-z	tOLZ	3		3		3		ns	3
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from \overline{W}	tWEZ	0	15	0	20	0	20	ns	7

4

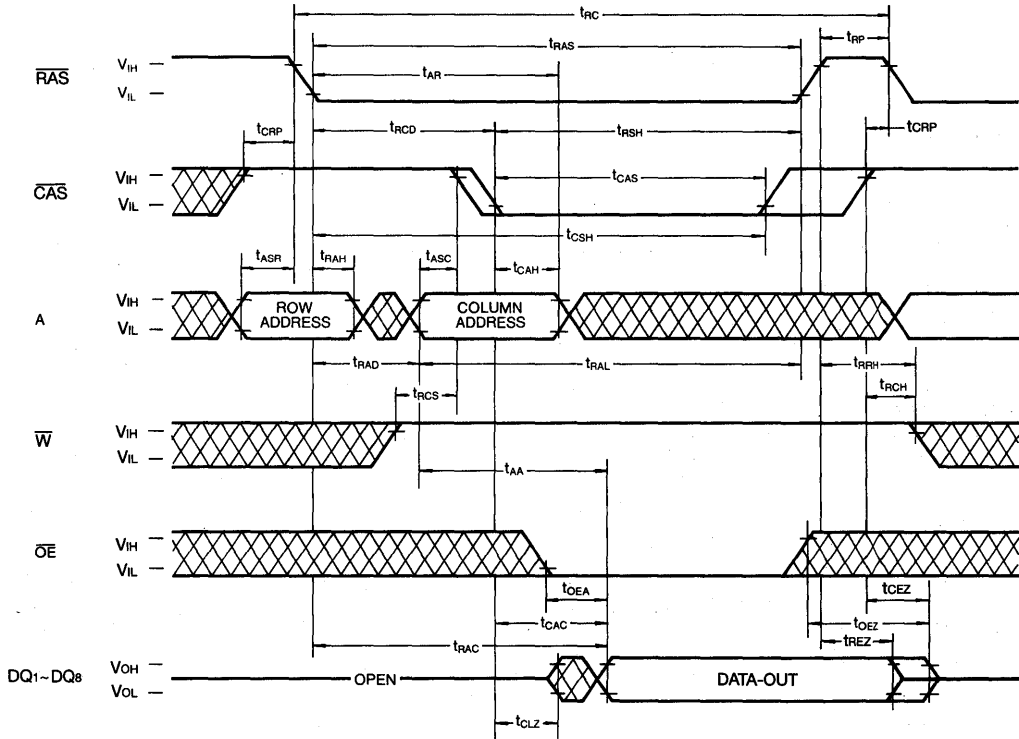
AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\bar{W} to data delay	twED	15		20		20		ns	
$\bar{O}E$ to $\bar{C}AS$ hold time	toCH	5		5		5		ns	
$\bar{C}AS$ hold time to $\bar{O}E$	tCHO	5		5		5		ns	
$\bar{O}E$ precharge time	toEP	5		5		5		ns	
\bar{W} Pulse width (Hyper Page Cycle)	twPE	5		5		5		ns	
$\bar{R}AS$ pulse width ($\bar{C}-B-\bar{R}$ self refresh)	trASS	100		100		100		μ s	13
$\bar{R}AS$ precharge time ($\bar{C}-B-\bar{R}$ self refresh)	trPS	110		130		150		ns	13
$\bar{C}AS$ hold time ($\bar{C}-B-\bar{R}$ self refresh)	tCHS	-50		-50		-50		ns	13

NOTES

- An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
- $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs except thPC and tHPRWC.
- Measured with a load equivalent to 1 TTL loads and 100pF, $V_{oh}/V_{ol}=2.0/0.8V$.
- Operation within the trCD(max) limit insures that trAC(max) can be met. trCD(max) is specified as a reference point only. If trCD is greater than the specified trCD(max) limit, then access time is controlled exclusively by tCAC.
- Assumes that trCD \geq trCD (max).
- tAR, twCR, tdHR are referenced to trAD(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
- twCS, trWD, tcWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If twCS \geq twCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcWD \geq tcWD(min), trWD \geq trWD(min) and tAWD \geq tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either trCH or trRH must be satisfied for a read cycle.
- These parameters are referenced to the $\bar{C}AS$ leading edge in early write cycles and to the \bar{W} leading edge in read-write cycles.
- Operation within the trAD(max) limit insures that trAC(max) can be met. trAD(max) is specified as a reference point only. If trAD is greater than the specified trAD(max) limit, then access time is controlled by tAA.
- tASC \geq tCPmin, Assume tT=2.0 ns
- 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (LL-ver)
- If $\bar{R}AS$ goes high before $\bar{C}AS$ high going, the open circuit condition of the output is achieved by $\bar{C}AS$ high going, If $\bar{C}AS$ goes high before $\bar{R}AS$ high going, the open circuit condition of the output is achieved by $\bar{R}AS$ high going.

TIMING DIAGRAMS
READ CYCLE

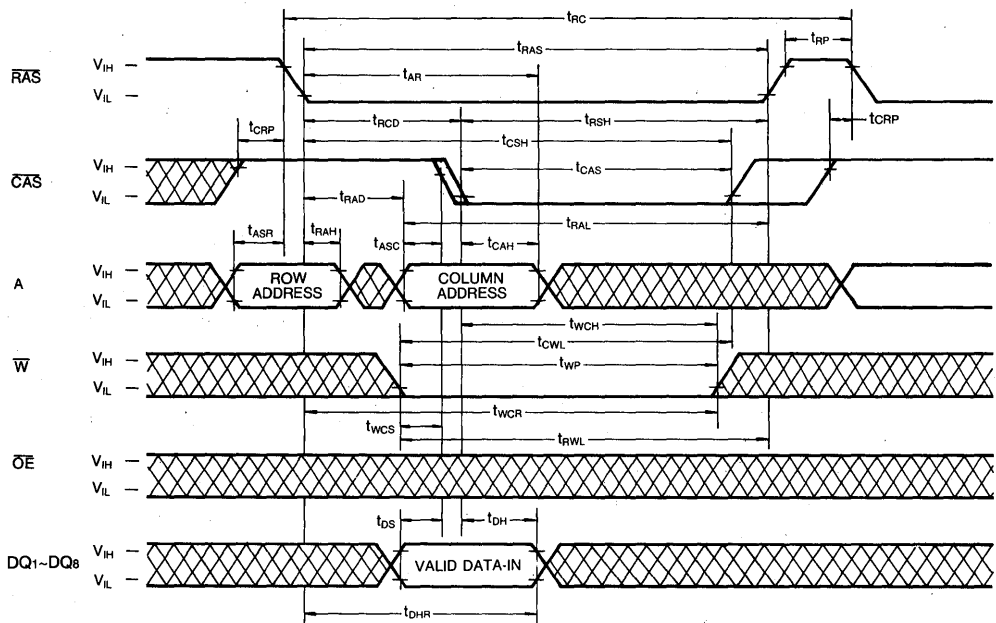


 Don't Care

4

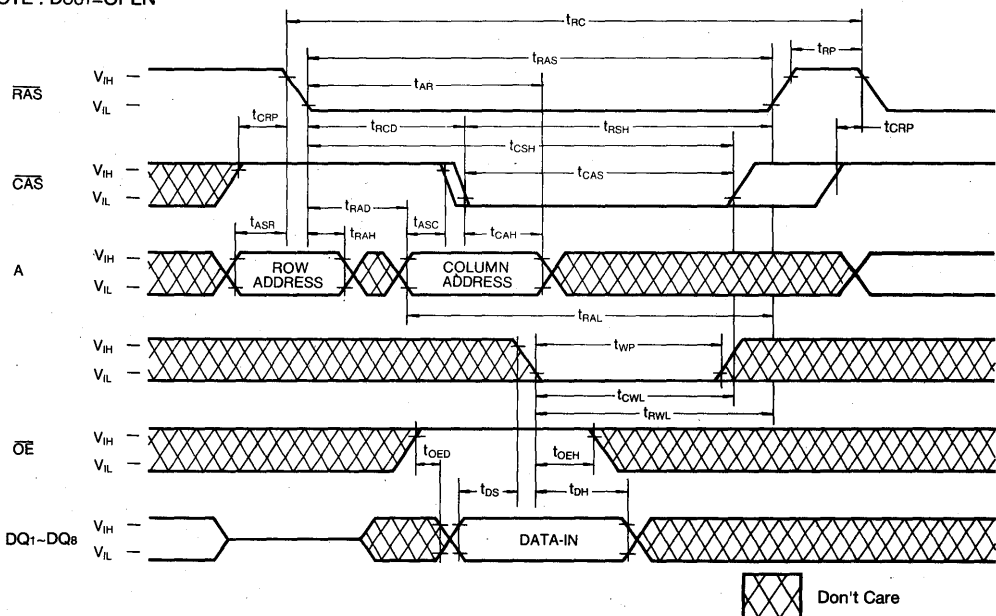
WRITE CYCLE (EARLY CYCLE)

NOTE : DOUT=OPEN



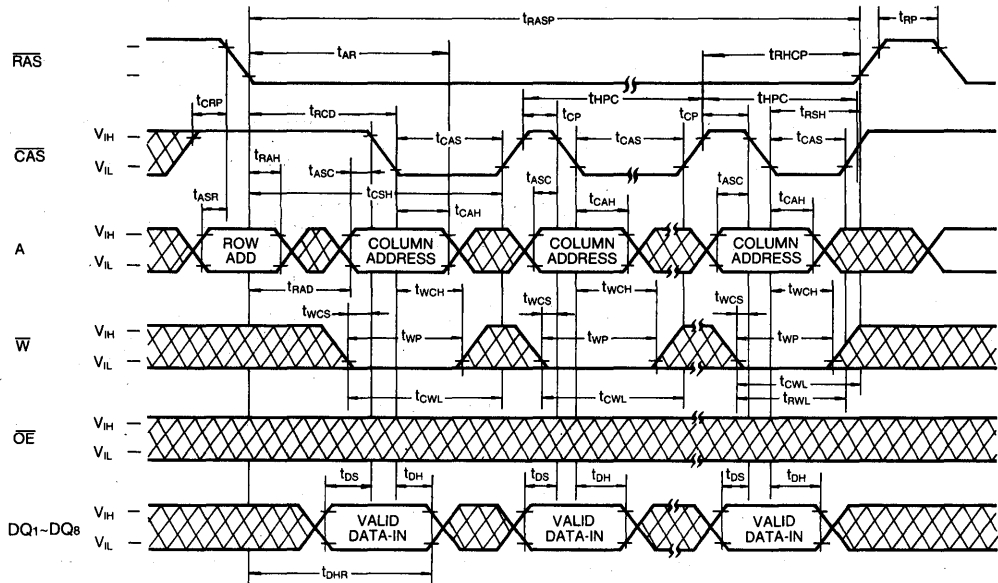
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

NOTE : DOUT=OPEN

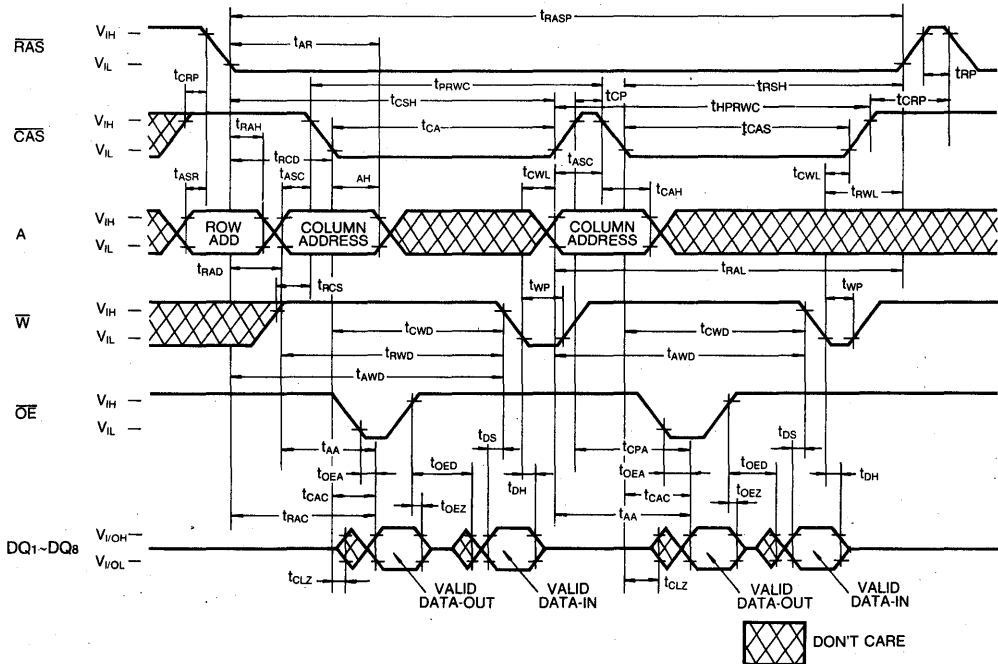


 Don't Care

HYPER PAGE WRITE CYCLE (EARLY WRITE)

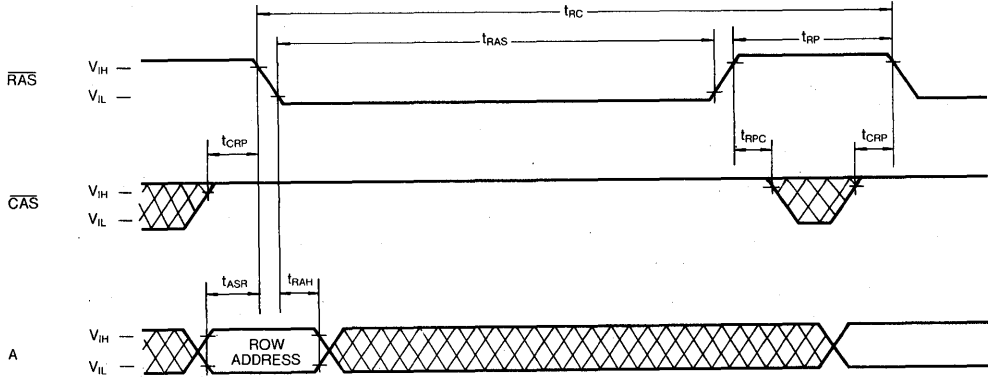


HYPER PAGE READ-MODIFY-WRITE CYCLE



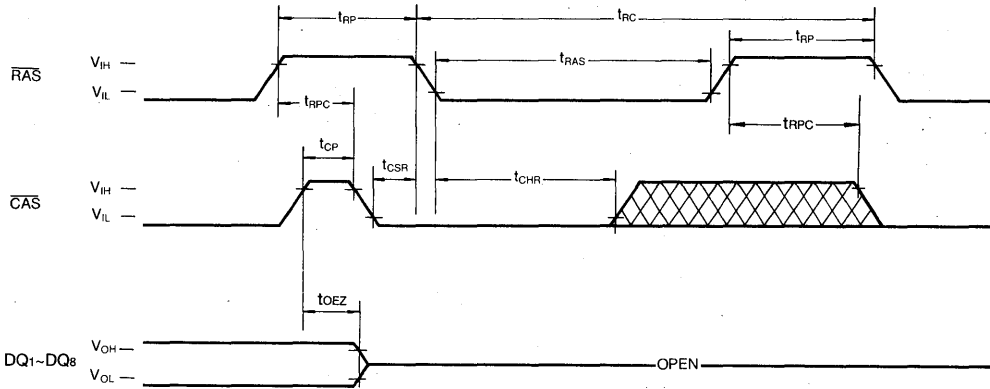
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , DIN =Don't Care
 Dout=Open



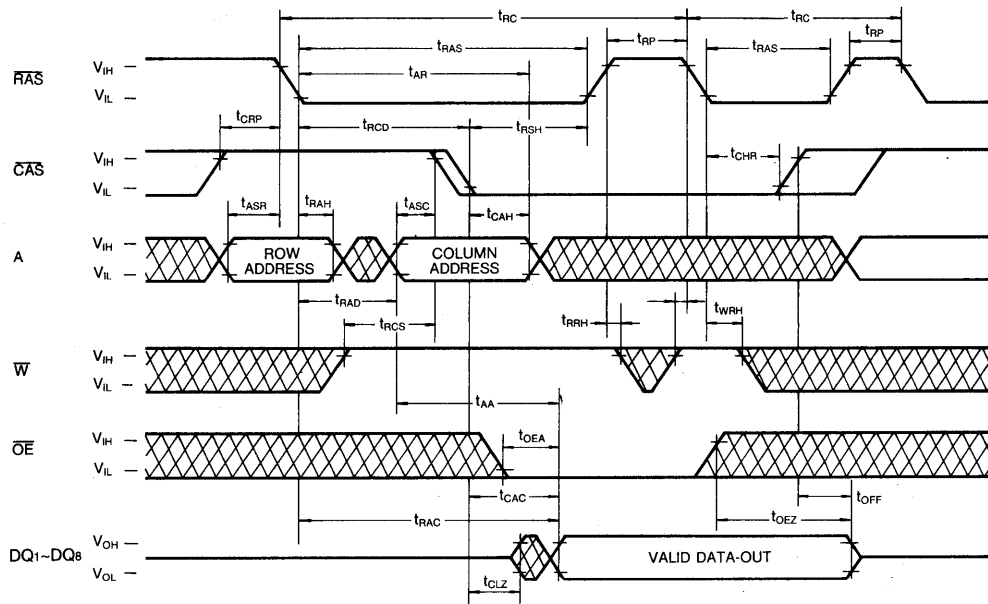
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A =Don't Care

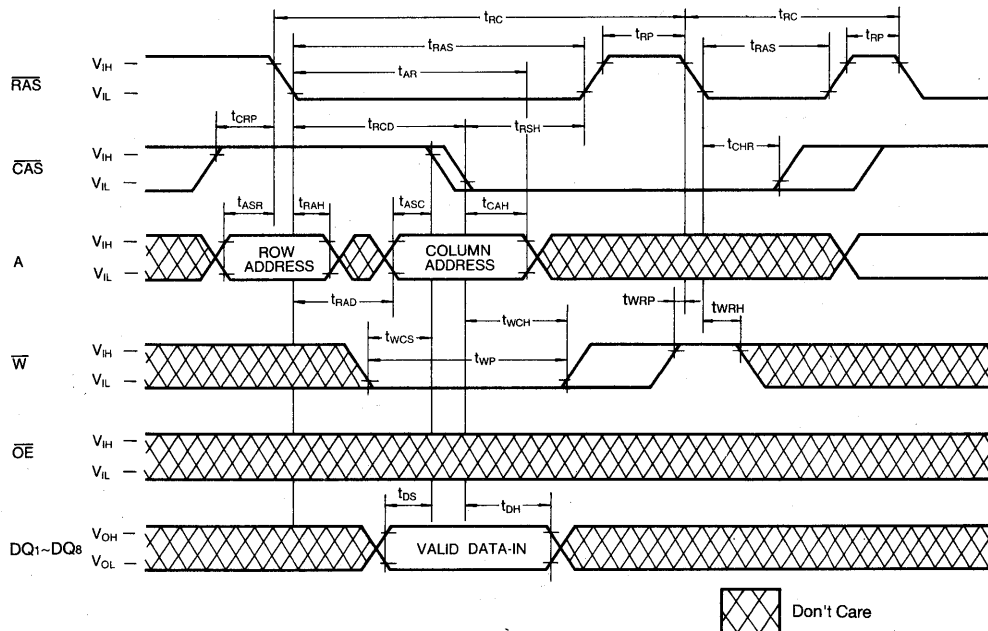


 Don't Care

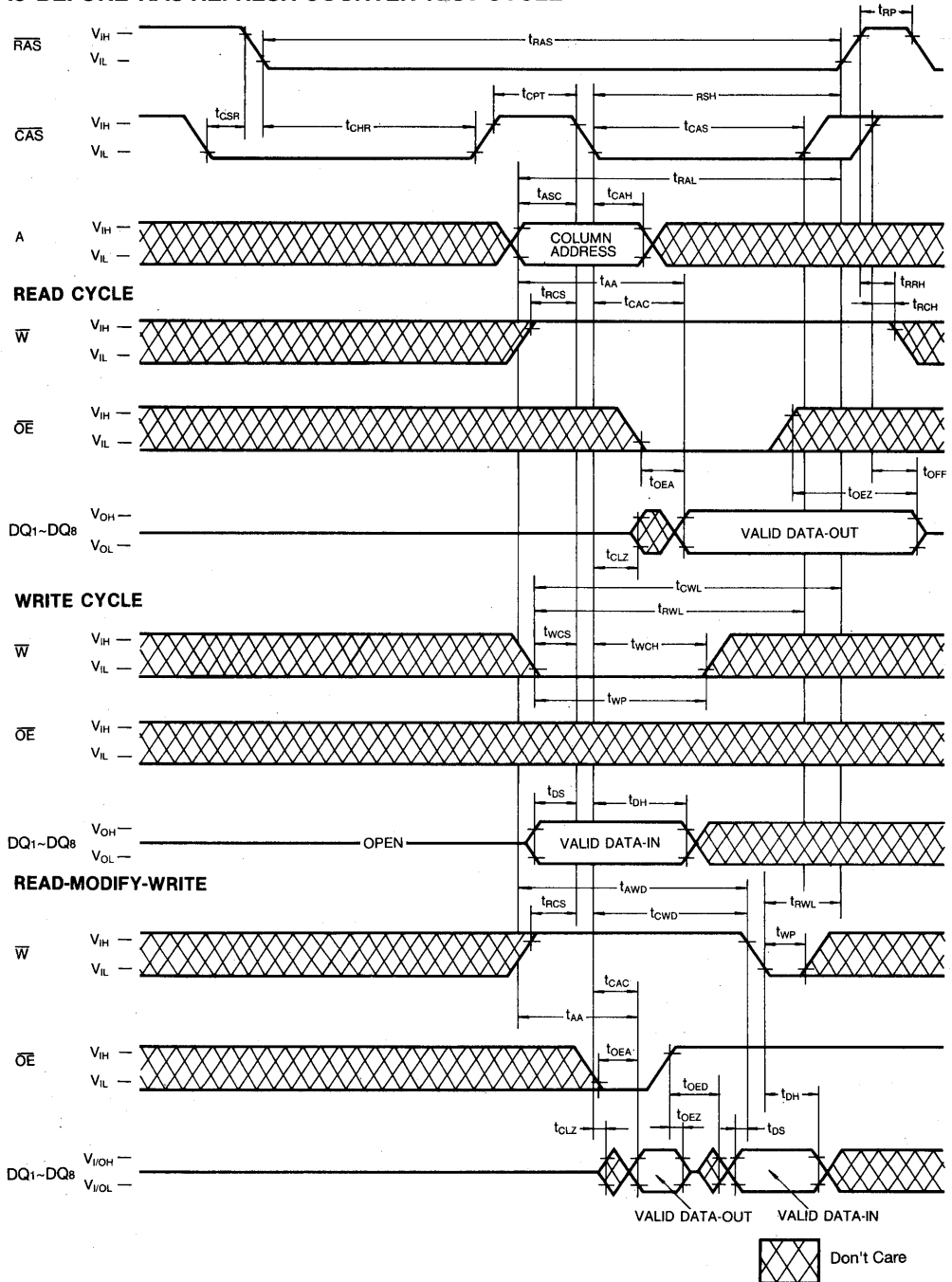
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



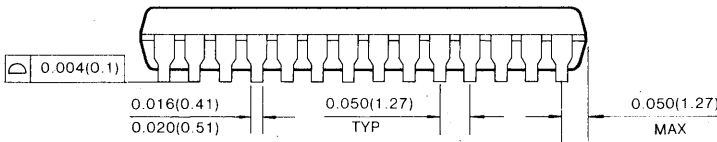
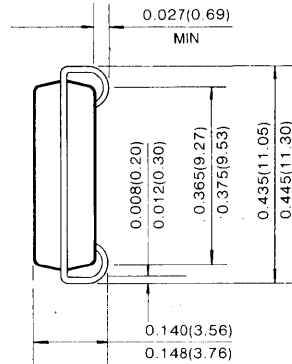
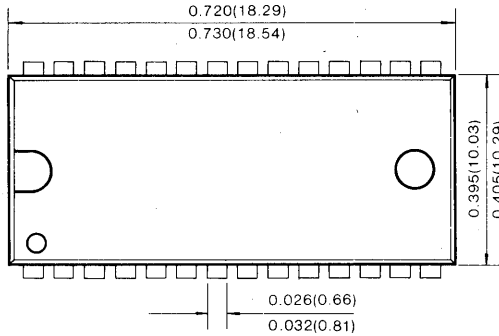
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



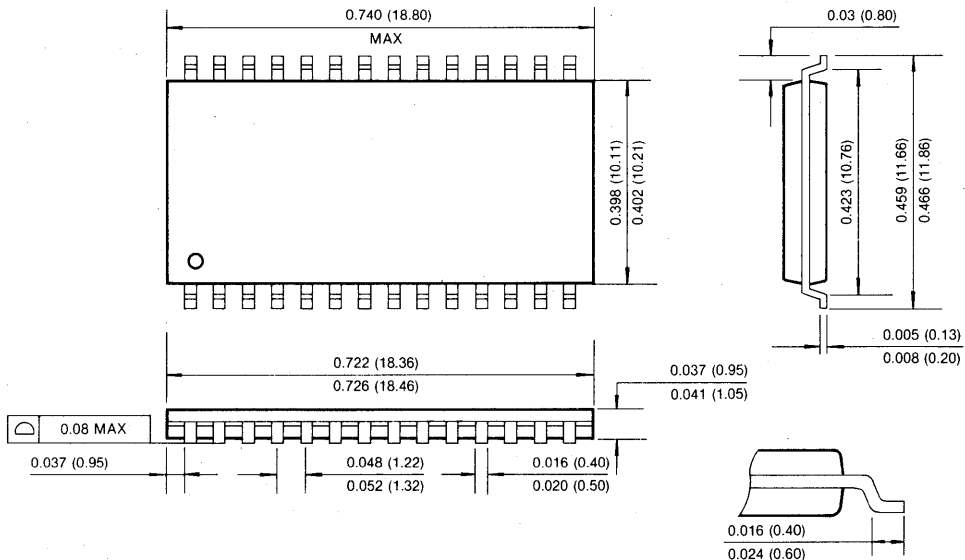
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



4

256K × 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	t _{TRAC}	t _{CAC}	t _{RC}
KM416V256B/BL/BLL-6	60ns	15ns	110ns
KM416V256B/BL/BLL-7	70ns	20ns	130ns
KM416V256B/BL/BLL-8	80ns	20ns	150ns

- Fast Page Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Self Refresh operation (LL-version)
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +3.3V ± 0.3V power supply
- Refresh Cycle
 - 512 cycle/8ms (Normal)
 - 512 cycle/64ms (L-version)
 - 512 cycle/128ms (LL-version)
- Power Dissipation
 - Standby: 1.8mW (Normal)
 - 0.36mW (L-version)
 - 0.36mW (LL-version)
 - Active (60/70/80): 325/290/270mW
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II

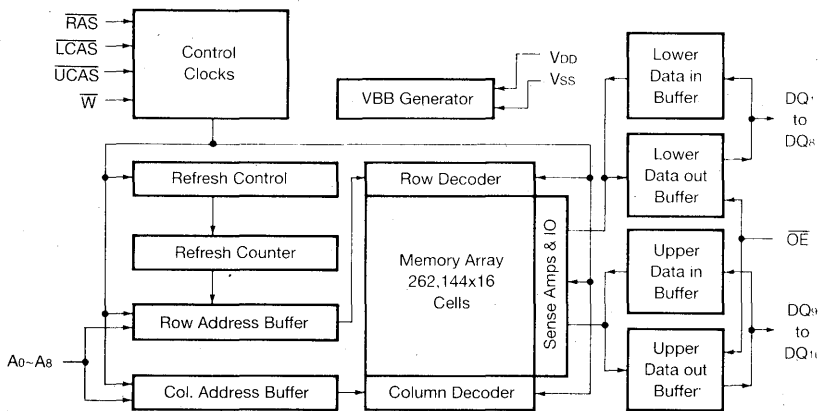
GENERAL DESCRIPTION

The Samsung KM416V256B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for low power applications such as portable computer and hand-held system.

The KM416V256B/BL/BLL features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

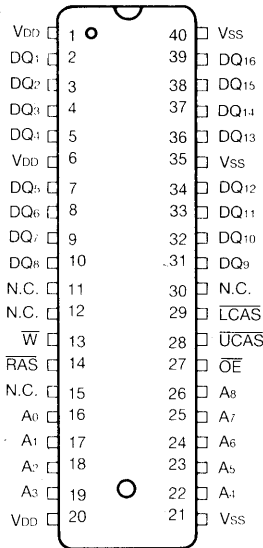
The KM416V256B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

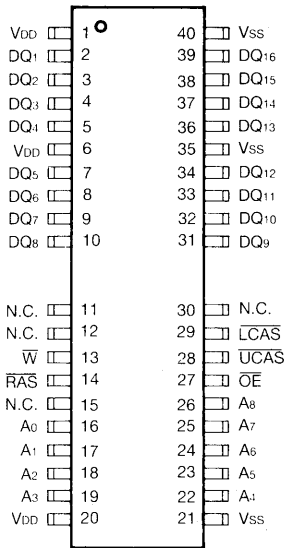


PIN CONFIGURATION (Top Views)

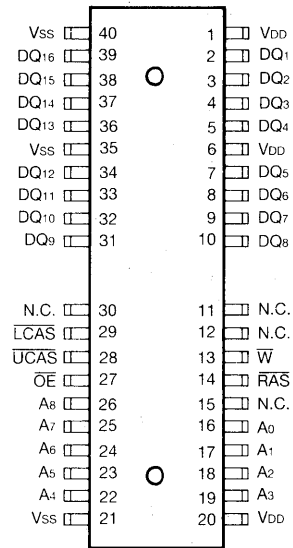
• KM416V256BJ/BLJ/BLLJ



• KM416V256BT/BLT/BLLT



• KM416V256BTR/BLTR/BLLTR



Pin Name	Pin Function
A ₀ -A ₈	Address Inputs
DQ ₁ -16	Data In/Out
V _{SS}	Ground
$\overline{\text{RAS}}$	Row Address Strobe
UCAS	Upper Column Address Strobe

Pin Name	Pin Function
$\overline{\text{LCAS}}$	Lower Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
V _{DD}	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5~4.6	V
Voltage on V _{DD} supply relative to V _{SS}	V _{DD}	-0.5~4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS, UCAS or LCAS, Address Cycling @trc=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8 I _{CC1}	-	90 80 75	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{IH})	I _{CC2}	-	1	mA
RAS-Only Refresh Current* (UCAS=LCAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8 I _{CC3}	-	90 80 75	mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , UCAS or LCAS, Address Cycling @tpc=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8 I _{CC4}	-	60 55 50	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{DD} -0.2V)	KM416V256B KM416V256BL KM416V256BLL I _{CC5}	-	500 100 100	μA μA μA
CAS-Before-RAS Refresh Current* (RAS, UCAS or LCAS Cycling @trc=min.)	KM416V256B/BL/BLL-6 KM416V256B/BL/BLL-7 KM416V256B/BL/BLL-8 I _{CC6}	-	90 80 75	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V Input Low Voltage(V _{IL})=0.2V xCAS=V _{IL} DIN=Don't Care, TRC=125μS TRAS=TRAS min.~300ns	KM416V256BL I _{CC7}	-	200	μA
Self Refresh Current RAS=xCAS=0.2V W=OE=A0-A8=V _{DD} -0.2V or 0.2V DQ1-DQ16=V _{DD} -0.2V, 0.2V or Open	KM416V256BLL I _{CC8}	-	100	μA
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{DD} +0.3V, all other pins not under test=0 V)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{DD})	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, VDD=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A6)	CIN1	-	5	pF
Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VDD=3.3V ± 0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from $\overline{\text{RAS}}$	tRAC		60		70		80	ns	3,4,11
Access time from $\overline{\text{CAS}}$	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	40		50		60		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
$\overline{\text{RAS}}$ hold time	tRSH	15		20		20		ns	
$\overline{\text{CAS}}$ hold time	tCSH	60		70		80		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	15	10,000	20	10,000	20	10,000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	45	20	50	20	60	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	30	15	35	15	40	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	15		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	50		55		60		ns	6
Refresh period (Normal)	tREF		8		8		8	ms	
Refresh period (L-version)	tREF		64		64		64	ms	
Refresh period (LL-version)	tREF		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCFA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		ns	
Access time from $\overline{\text{OE}}$	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data-in delay time	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ commend hold time	tOEH	15		20		20		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRASS	100		100		100		μ s	12
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRPS	110		130		150		ns	12
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		ns	12

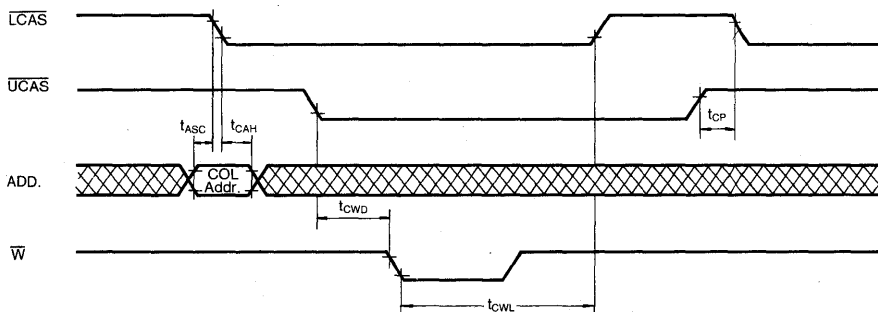
KM416V256B/BL/BLL Truth Table

$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ ₁ ~DQ ₈	DQ ₉ ~DQ ₁₆	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

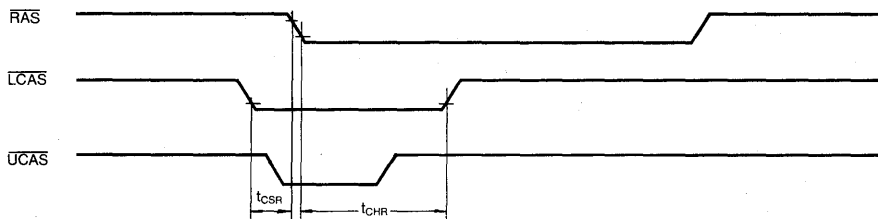


NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF, $V_{OH}=2.0V$ and $V_{OL}=0.8V$
4. Operation within the $t_{RCO}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCO}(\text{max})$ is specified as a reference point only. If t_{RCO} is greater than the specified $t_{RCO}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCO} \geq t_{RCO}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\text{max})$.
7. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{RWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. 512 cycles of burst refresh must be executed within 8ms before and after self refresh, In order to meet refresh specification.
13. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
14. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
15. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
16. t_{CWL} is specified from \overline{W} falling edge to the earlier $\overline{\text{CAS}}$ rising edge.

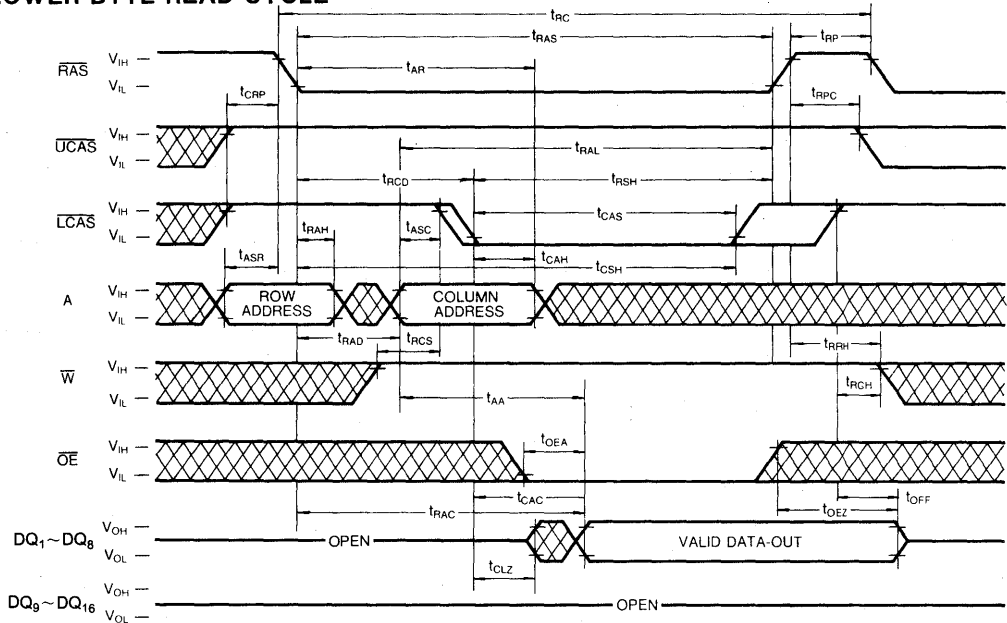


17. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
18. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.

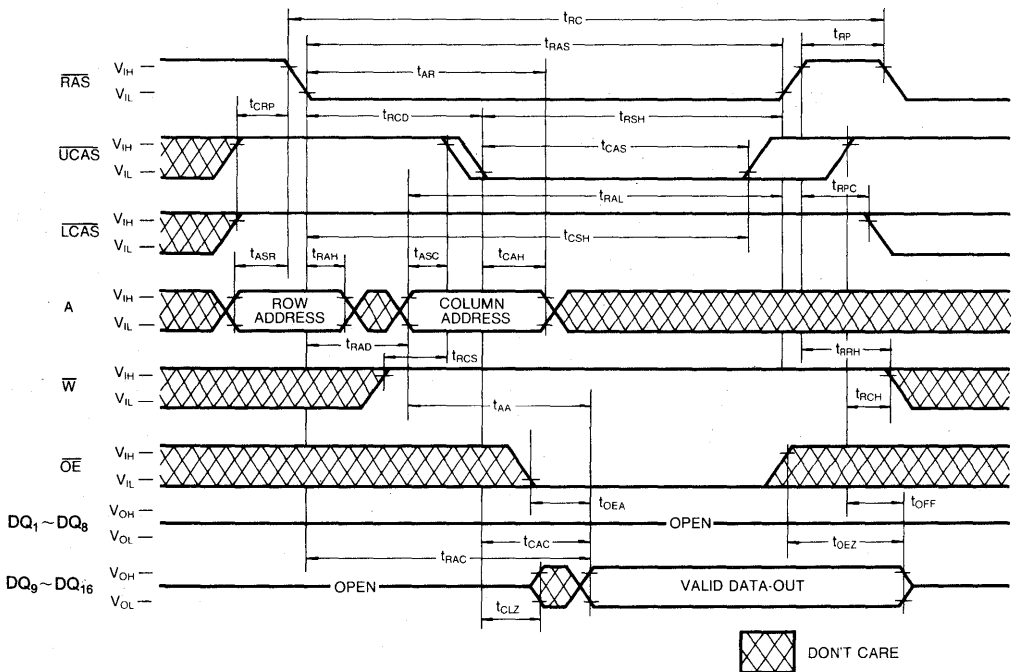


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



UPPER BYTE READ CYCLE

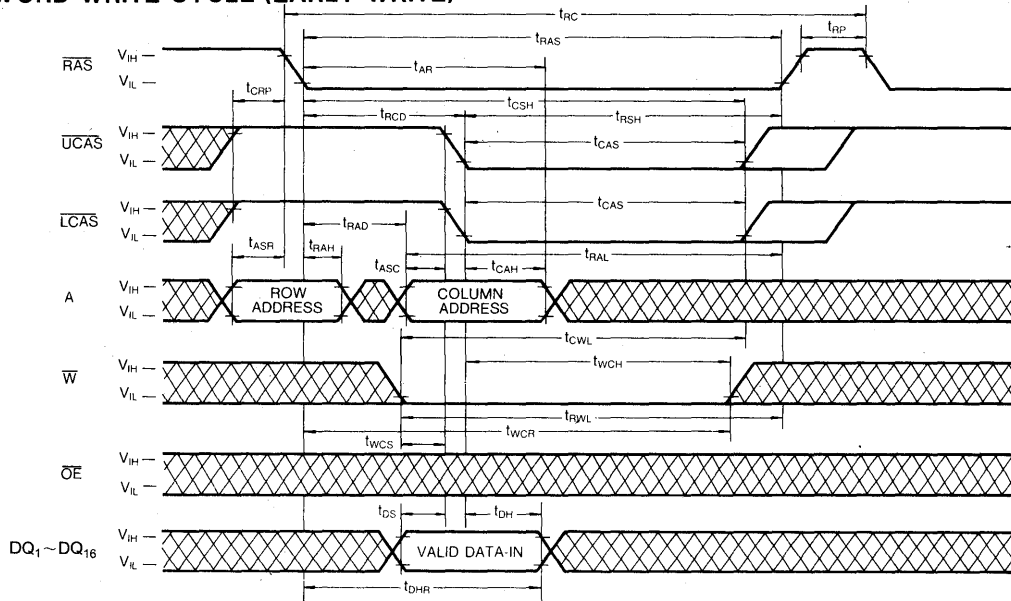


 DON'T CARE

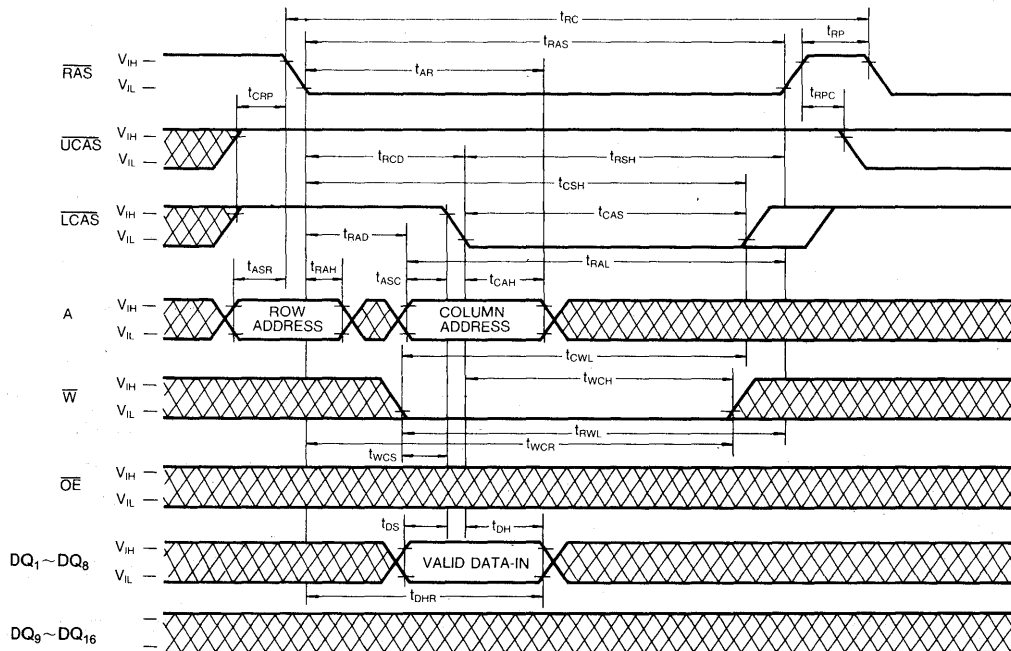
4

TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



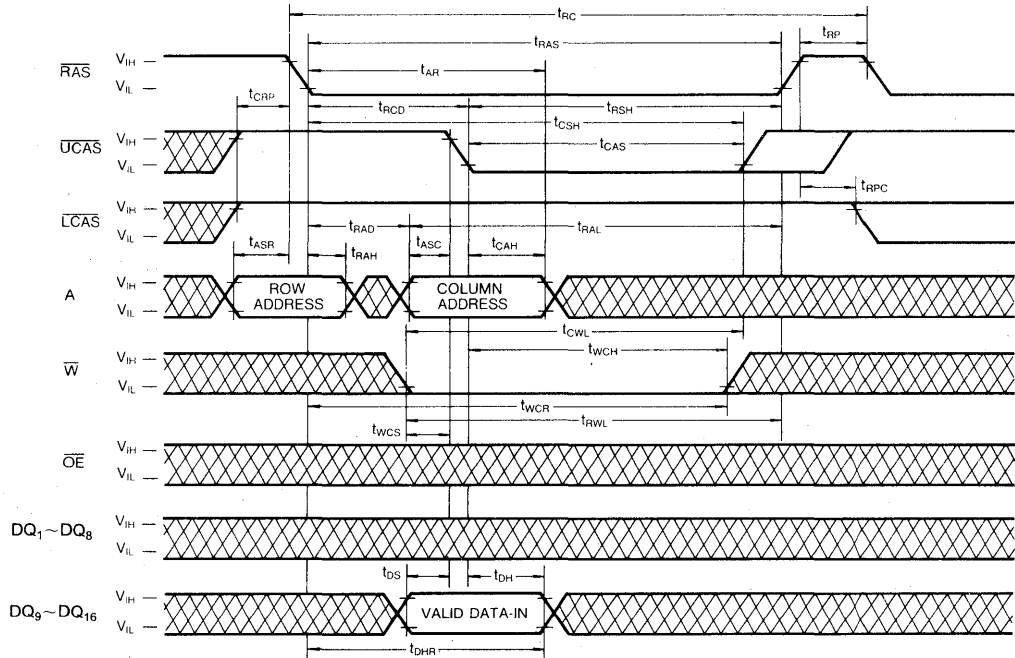
LOWER BYTE WRITE CYCLE (EARLY WRITE)



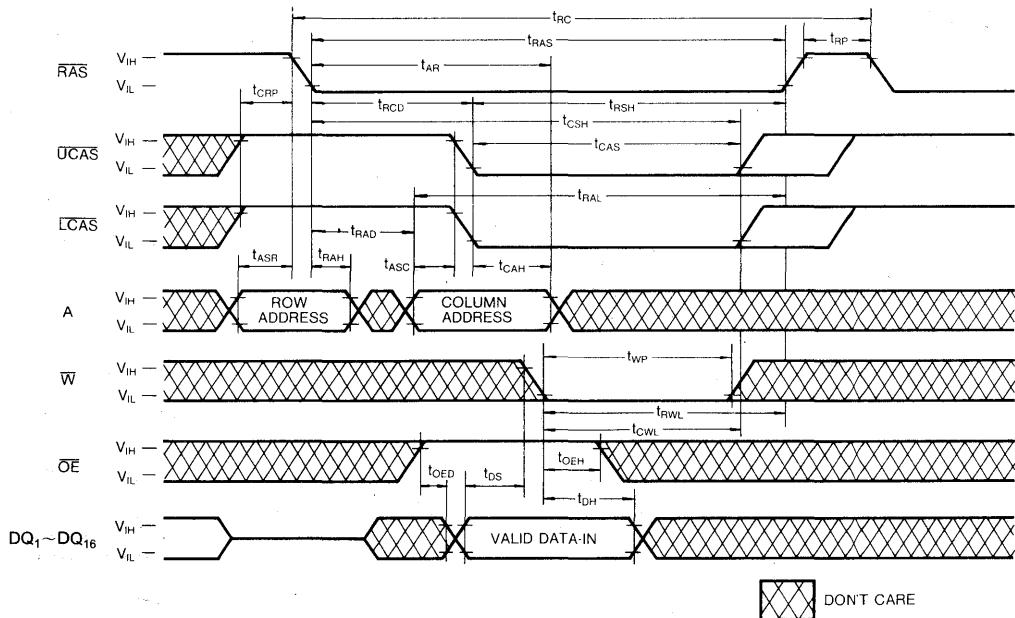
 DONT CARE

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



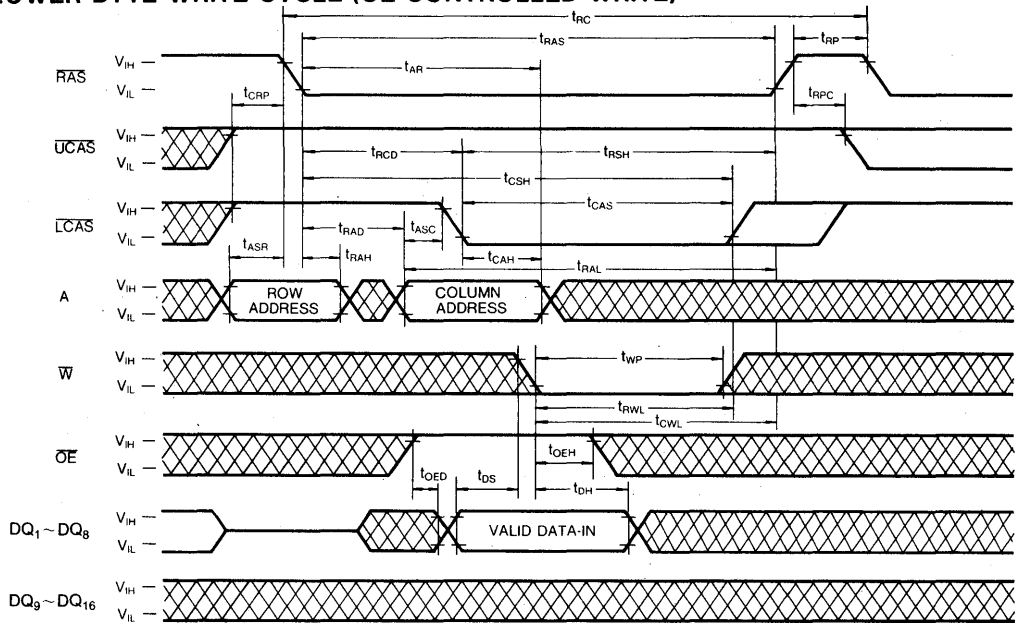
WORD WRITE CYCLE (OE CONTROLLED WRITE)



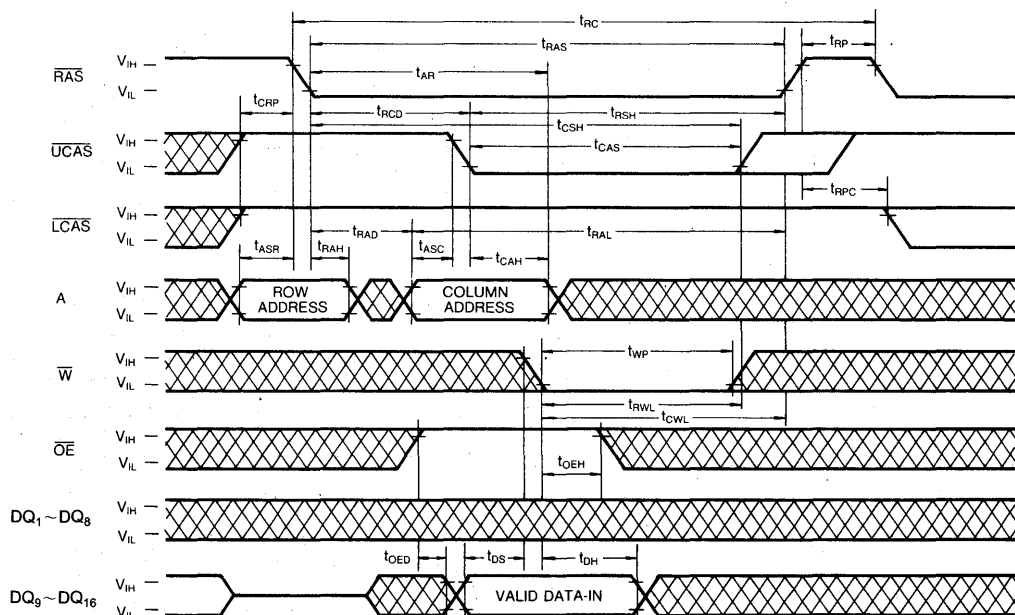
4

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



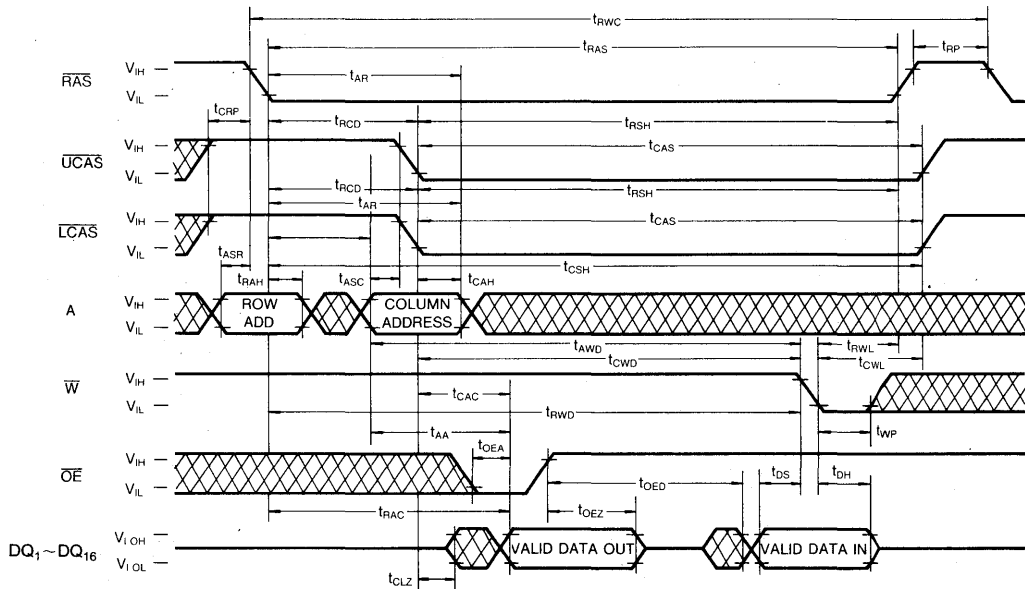
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



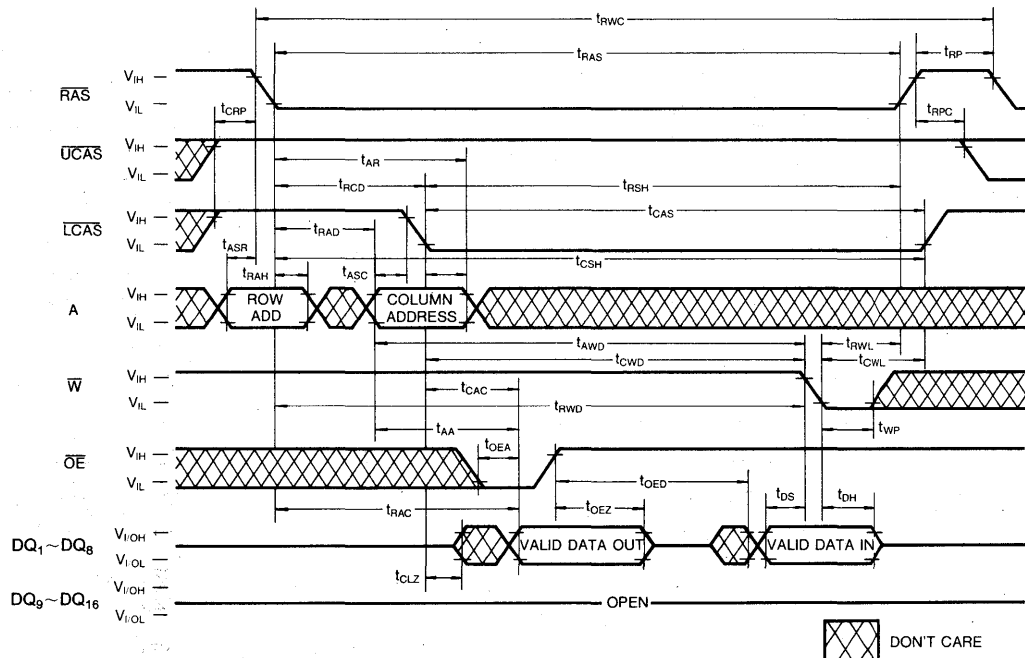
 DONT CARE

TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE



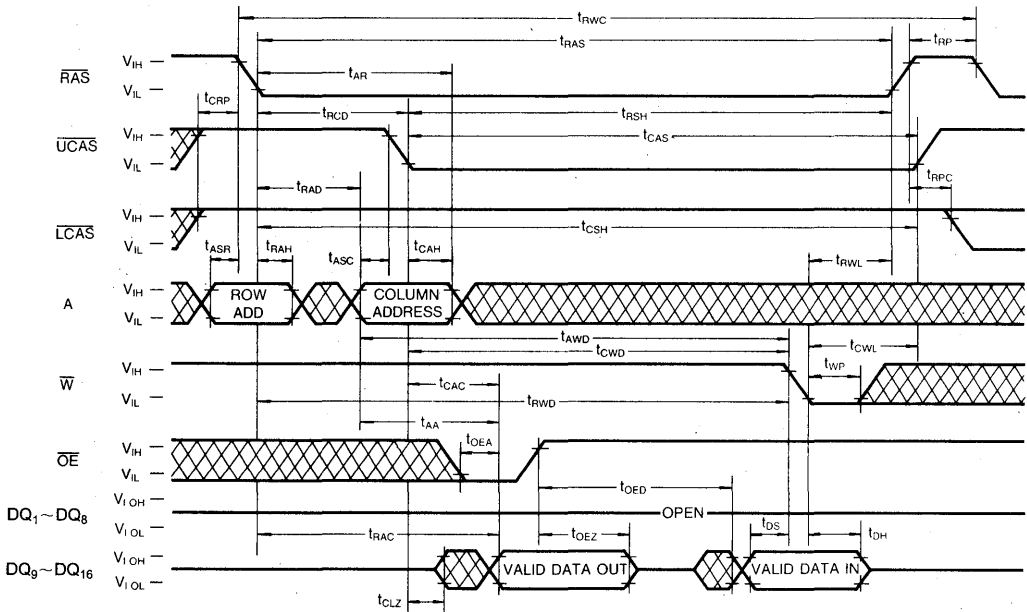
LOWER-BYTE READ-MODIFY-WRITE CYCLE



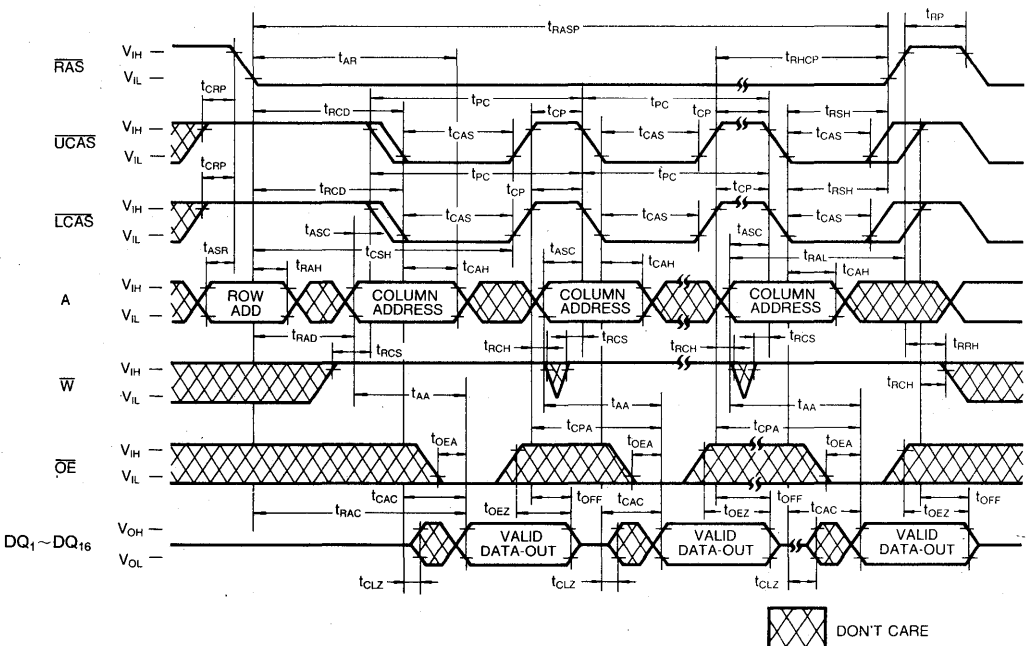
DON'T CARE

TIMING DIAGRAMS (Continued)

UPPER-BYTE READ-MODIFY-WRITE CYCLE



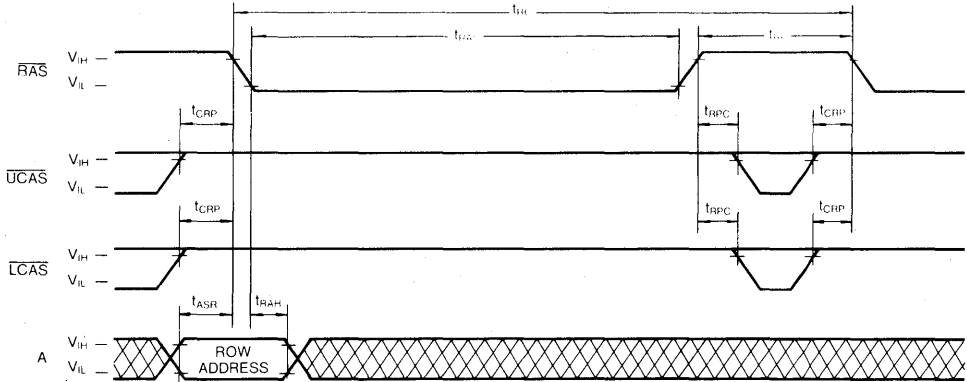
FAST PAGE MODE WORD READ CYCLE



TIMING DIAGRAMS (Continued)

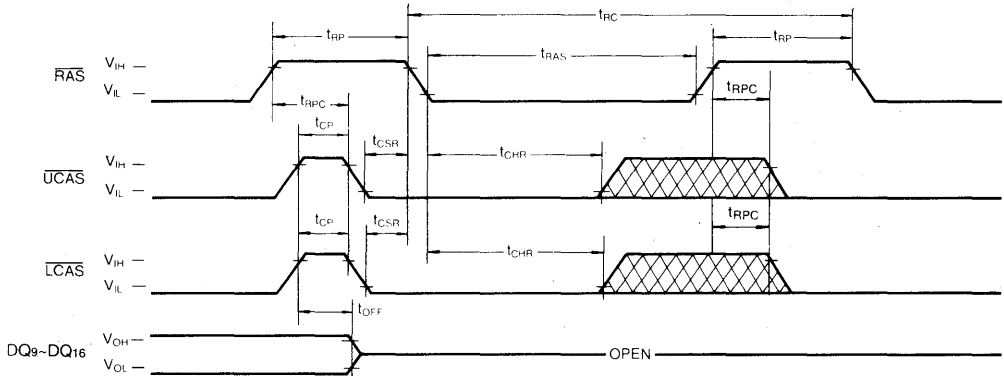
RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care



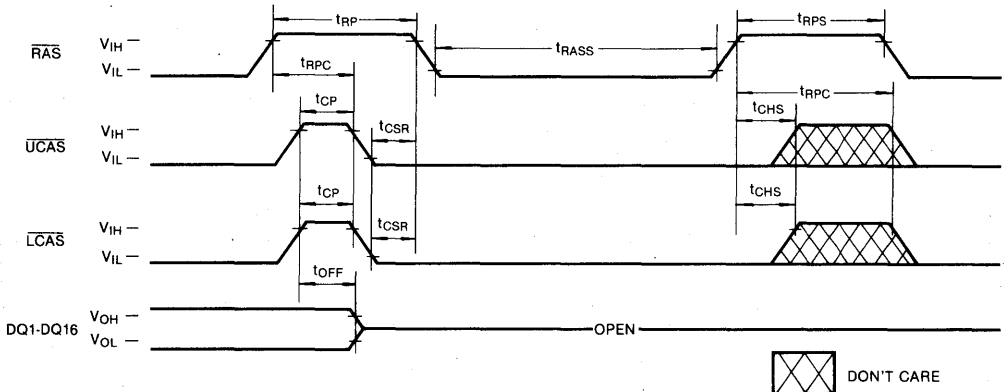
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} , A = Don't Care



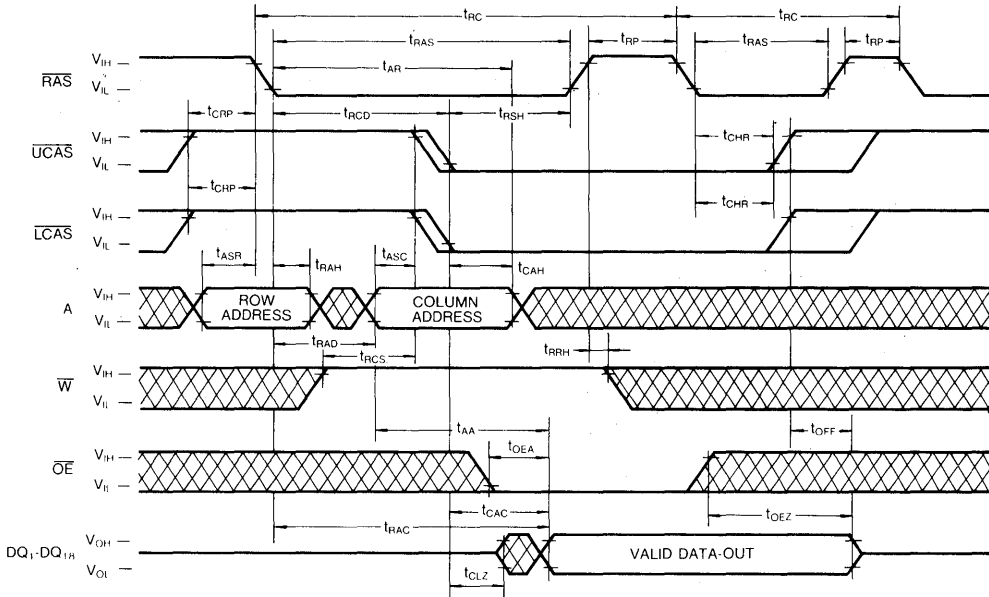
CAS-BEFORE-RAS SELF REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} , A = Don't Care

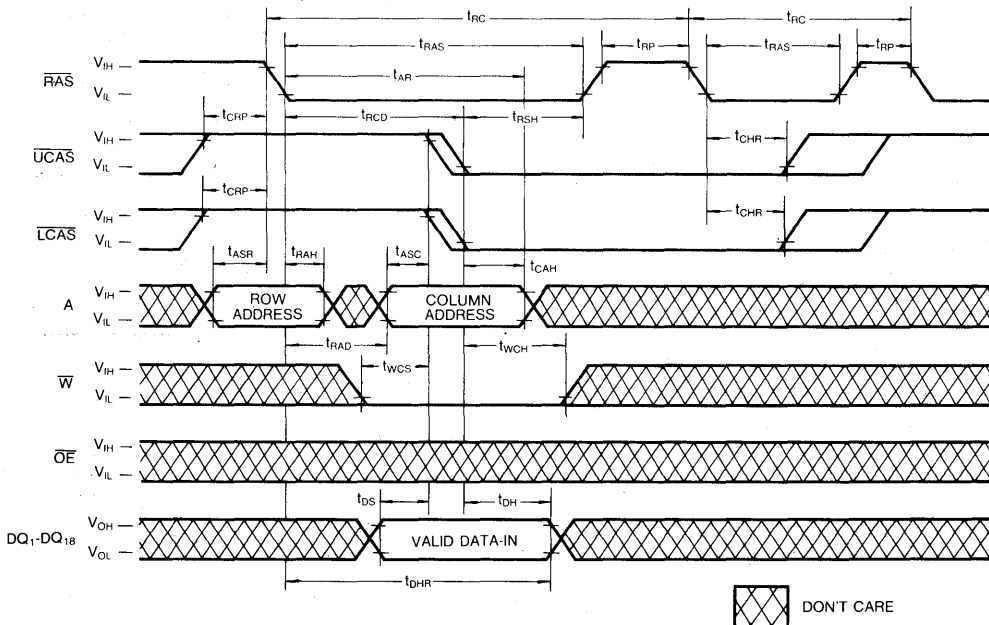


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

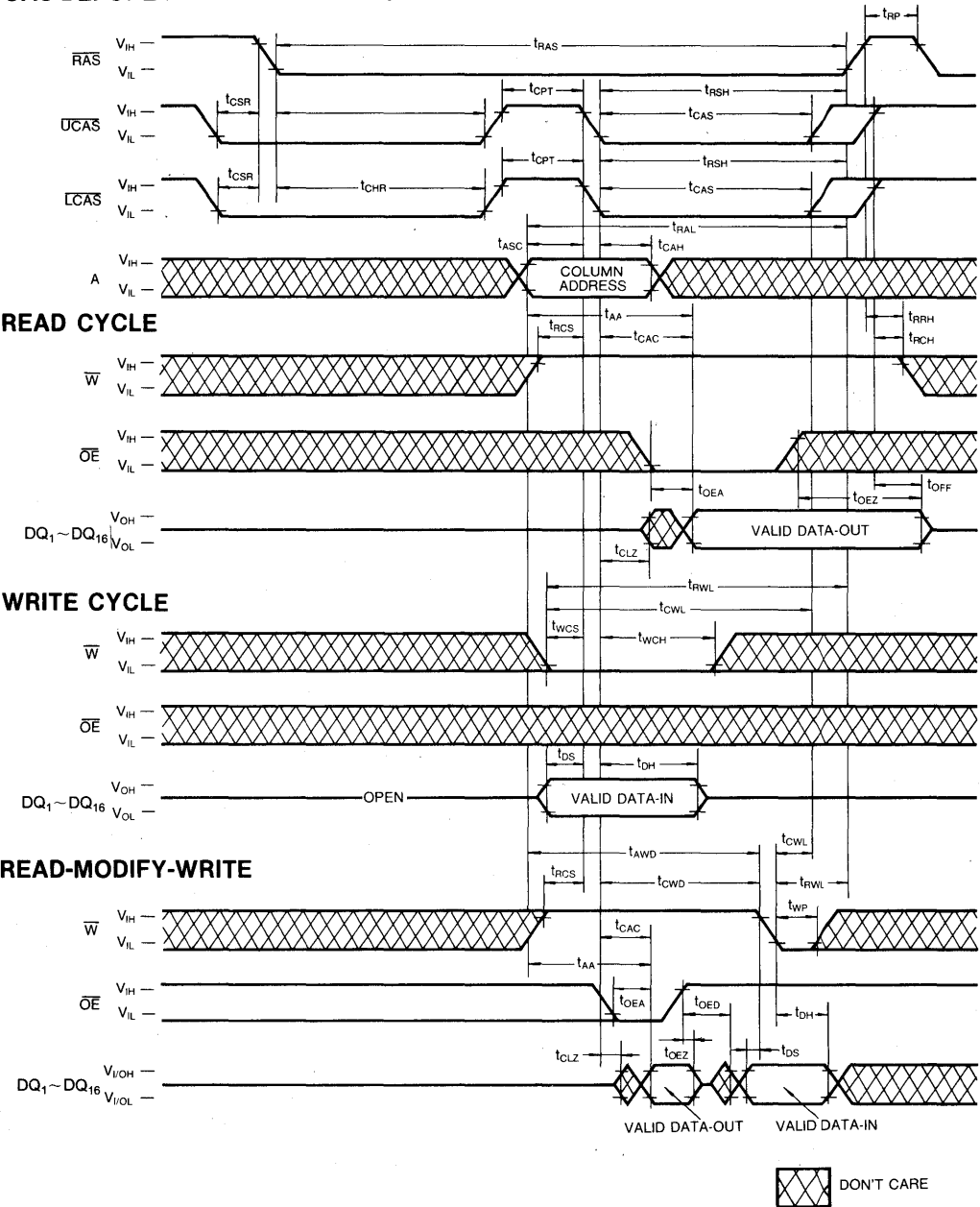


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

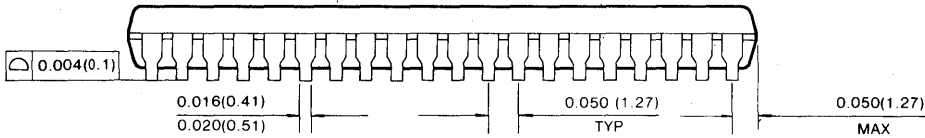
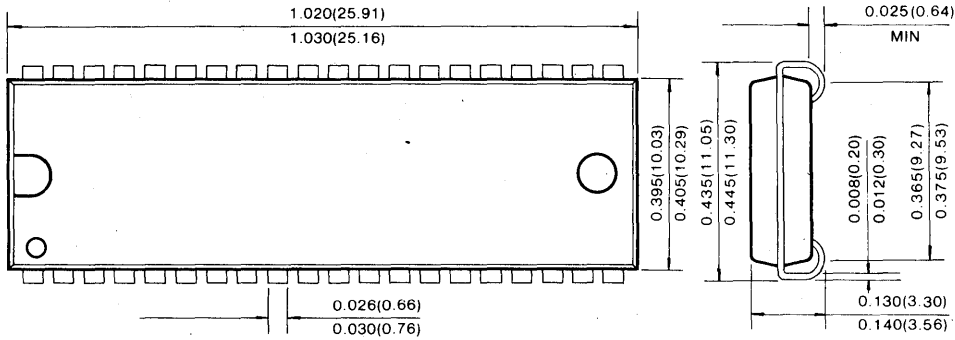


4

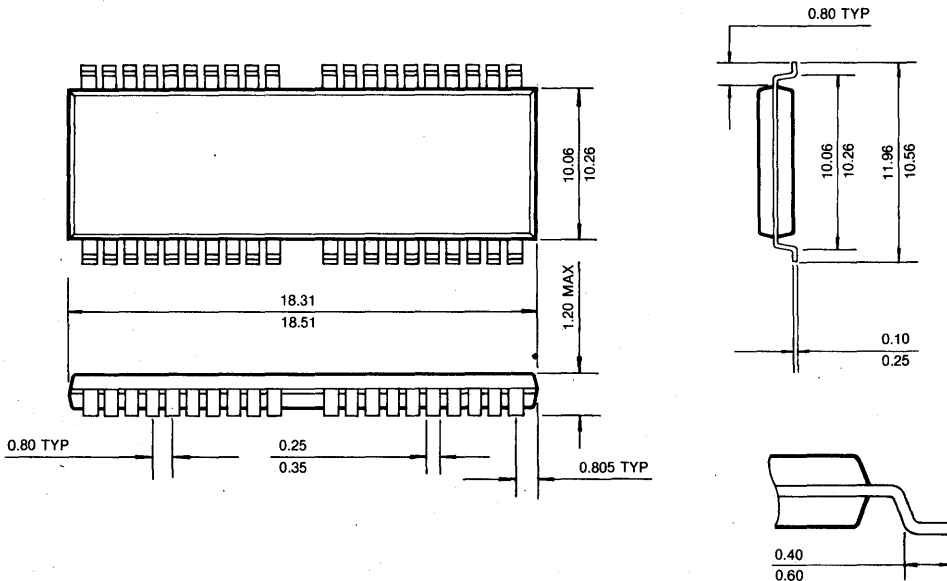
PACKAGE DIMENSION

40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



256K × 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	trAC	tcAC	trC	thPC
KM416V254B/BL/BLL-6	60ns	17ns	110ns	24ns
KM416V254B/BL/BLL-7	70ns	20ns	130ns	29ns
KM416V254B/BL/BLL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended Data out**
- **Byte word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Self Refresh operation (LL-version)**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple 3.3V ± 0.3V power supply**
- **Refresh Cycle**
 - 512 cycle/8ms (Normal)
 - 512 cycle/64ms (L-version)
 - 512 cycle/128ms (LL-version)
- **Power Dissipation**
 - Standby : 1.8mW(Normal)
 - 0.36mW(L-version)
 - 0.36mW(LL-version)
 - Active (60/70/80): 255/235/220mW
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP II**

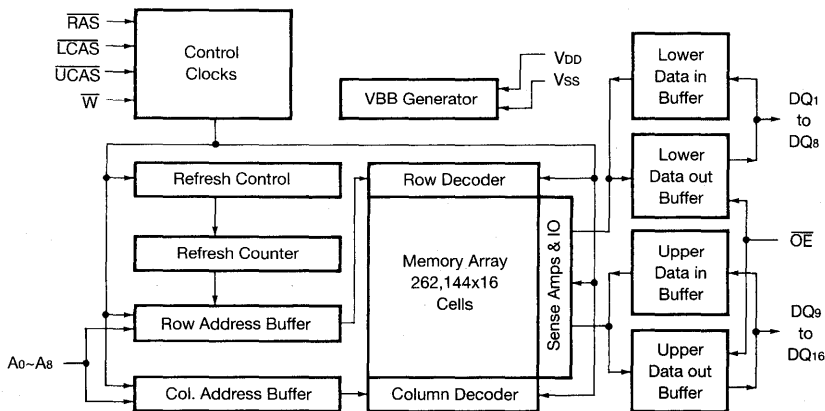
GENERAL DESCRIPTION

The Samsung KM416V254B/BL/BLL is a CMOS high speed 262,144 bit × 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, graphics and high performance portable computers.

The KM416V254B/BL/BLL features EDO Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

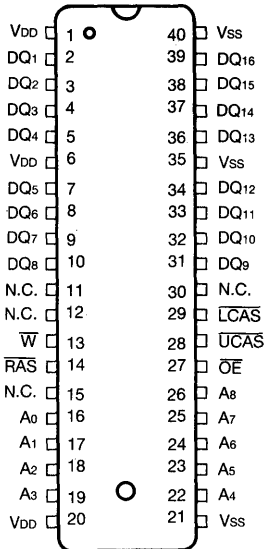
The KM416V254B/BL/BLL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

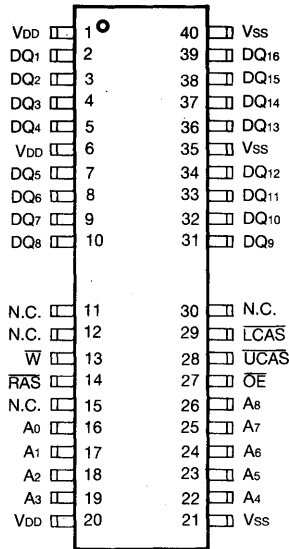


PIN CONFIGURATION (Top Views)

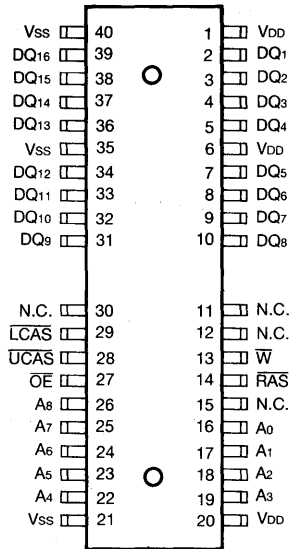
• KM416V254BJ/BLJ/BLLJ



• KM416V254BT/BLT/BLLT



• KM416V254BTR/BLTR/BLLTR



Pin Name	Pin Function
A ₀ -A ₈	Address Inputs
DQ ₁ -16	Data In/Out
V _{SS}	Ground
\bar{RAS}	Row Address Strobe
\bar{UCAS}	Upper Column Address Strobe
\bar{LCAS}	Lower Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
V _{DD}	Power(+3.3V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5~4.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD}	-0.5~4.6	V
Storage Temperature	T _{stg}	-55 to + 150	° C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS, UCAS=LCAS, Address Cycling @trc=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8 I _{CC1}	-	70 65 60	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{IH})	I _{CC2}	-	1	mA
RAS-Only Refresh Current* (UCAS=LCAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8 I _{CC3}	-	70 65 60	mA mA mA
Hyper page Mode Current* (RAS=V _{IL} , UCAS=LCAS, Address Cycling @tpc=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8 I _{CC4}	-	60 55 50	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{DD} -0.2V)	KM416V254B KM416V254BL KM416V254BLL I _{CC5}	-	500 100 100	μA μA μA
CAS-Before-RAS Refresh Current* (RAS and UCAS=LCAS Cycling @trc=min.)	KM416V254B/BL/BLL-6 KM416V254B/BL/BLL-7 KM416V254B/BL/BLL-8 I _{CC6}	-	70 65 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V Input Low Voltage(V _{IL})=0.2V UCAS=LCAS=0.2V DIN=Don't Care, TRC=125μS TRAS=TRAS min.~300ns	KM416V254BL I _{CC7}	-	200	μA
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A8=V _{DD} -0.2V or 0.2V DQ1-DQ16=V _{DD} -0.2V, 0.2V or Open	KM416V254BLL I _{CC8}	-	100	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} = -2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} = 2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum two times while RAS = V_{IL}. In I_{CC4}, address can be changed maximum once within one hyper page cycle.

CAPACITANCE (T_A = 25°C, V_{DD} = 3.3V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ -A ₈)	C _{IN1}	-	5	pF
Input Capacitance (RAS, UCAS, LCAS, W, OE)	C _{IN2}	-	7	pF
Input Capacitance (DQ1-DQ16)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD} = 3.3V ± 0.3V, See notes 1,2)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		185		205		ns	
Access time from RAS	t _{RAC}		60		70		80	ns	3,4,11
Access time from CAS	t _{CAC}		17		20		20	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,11
CAS to output in Low-Z	t _{CLZ}	3		3		3		ns	3
Turn-off delay from CAS	t _{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	2
RAS precharge time	t _{RP}	40		50		60		ns	
RAS pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	t _{RSH}	17		20		20		ns	
CAS hold time	t _{CSH}	50		60		70		ns	
CAS pulse width	t _{CAS}	10	10,000	15	10,000	20	10,000	ns	12
RAS to CAS delay time	t _{RCD}	20	45	20	50	20	60	ns	4
RAS to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	t _{CRP}	5		5		5		ns	
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	15		15		15		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time referenced to \overline{RAS}	tAR	50		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		10		10		ns	
Write command hold time referenced to \overline{RAS}	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		10		10		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		20		ns	
Write command to \overline{CAS} lead time	tCWL	15		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	15		15		15		ns	10
Data hold time referenced to \overline{RAS}	tDHR	50		55		60		ns	6
Refresh Period (Normal)	tREF		8		8		8	ms	
Refresh Period (L-ver)	tREF		64		64		64	ms	
Refresh Period (LL-ver)	tREF		128		128		128	ms	
Write command set-up time	tWCS	0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	tCWD	42		50		50		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	85		95		105		ns	8
Column address to \overline{W} delay time	tAWD	55		60		65		ns	8
\overline{CAS} precharge to \overline{W} delay time	tCPWD	60		65		70		ns	
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		10		ns	
\overline{RAS} to \overline{CAS} precharge time	tRPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} -B- \overline{R} counter test cycle)	tCPT	20		25		30		ns	
Access time from \overline{CAS} precharge	tCPA		35		40		45	ns	3
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
\overline{CAS} precharge time (Hyper Page mode)	tCP	10		10		10		ns	
\overline{RAS} pulse width (Hyper Page mode)	tRASP	60	100K	70	100K	80	100K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	tRHCP	35		40		45		ns	
\overline{OE} access time	tOEA		15		20		20	ns	
\overline{OE} to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	3	15	3	20	3	20	ns	7
\overline{OE} command hold time	tOEH	15		20		20		ns	
\overline{OE} to Output in Low-Z	tOLZ	3		3		3		ns	3
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	tREZ	3	15	3	20	3	20	ns	7,14

AC CHARACTERISTICS (Continued)

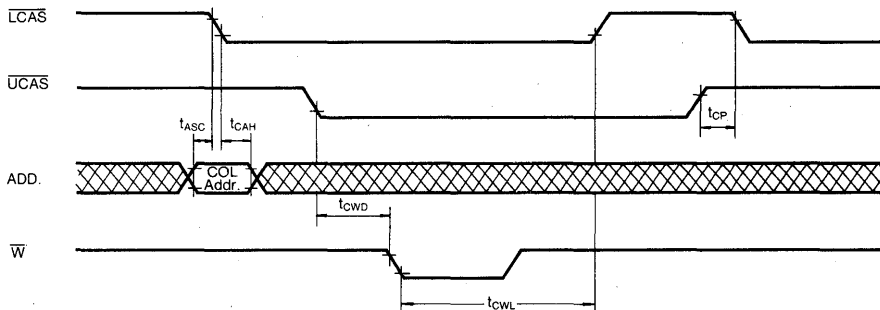
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay from \bar{W}	tWEZ	3	15	3	20	3	20	ns	7
\bar{W} to data delay	twED	15		20		20		ns	
\bar{OE} to \bar{CAS} hold time	tOCH	5		5		5		ns	
\bar{CAS} hold time to \bar{OE}	tCHO	5		5		5		ns	
\bar{OE} precharge time	tOEP	5		5		5		ns	
\bar{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		ns	
\bar{RAS} pulse width(\bar{C} - \bar{B} - \bar{R} self refresh)	trASS	100		100		100		μ s	13
\bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} self refresh)	trPS	110		130		150		ns	13
\bar{CAS} hold time (\bar{C} - \bar{B} - \bar{R} self refresh)	tCHS	-50		-50		-50		ns	13

KM416V254B/BL/BLL Truth Table

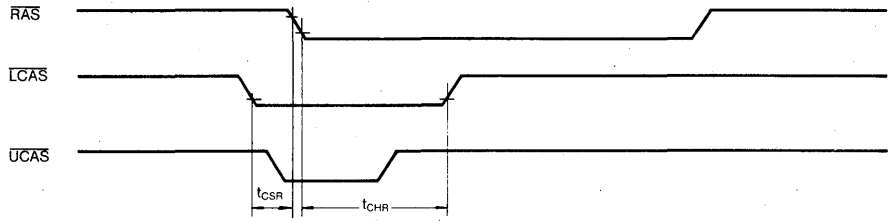
RAS	LCAS	UCAS	\bar{W}	\bar{OE}	DQ ₁ -DQ ₈	DQ ₉ -DQ ₁₆	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	-	Byte Write
L	H	L	L	H	-	DQ-IN	Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

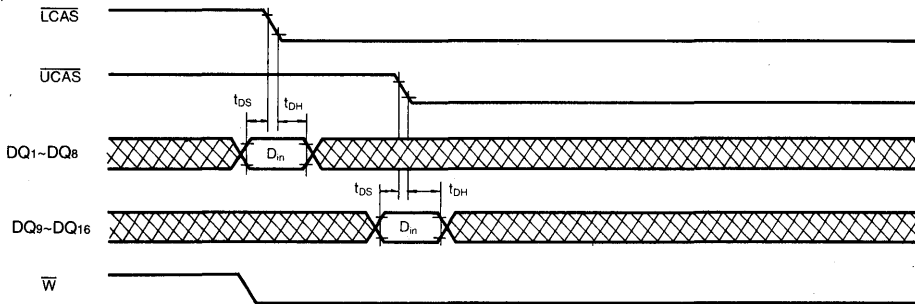
1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs except t_{HPC} and t_{HPRWC} .
3. Measured with a load equivalent to 1 TTL loads and 100pF, $V_{oh}=2.0V$ and $V_{ol}=0.8V$
4. Operation within the $trCD(\max)$ limit insures that $trAC(\max)$ can be met. $trCD(\max)$ is specified as a reference point only. If $trCD$ is greater than the specified $trCD(\max)$ limit, then access time is controlled exclusively by $tCAC$.
5. Assumes that $trCD \geq trCD(\max)$.
6. tAR , $tWCR$, $tDHR$ are referenced to $trAD(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. $twCS$, $trWD$, $tcWD$ and $tAWD$ are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $twCS \geq twCS(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $tcWD \geq tcWD(\min)$, $trWD \geq trWD(\min)$ and $tAWD \geq tAWD(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either $trCH$ or $trRH$ must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $trAD(\max)$ limit insures that $trAC(\max)$ can be met. $trAD(\max)$ is specified as a reference point only. If $trAD$ is greater than the specified $trAD(\max)$ limit, then access time is controlled by tAA .
12. $tASC \geq tCP \min$, Assume $tT=2.0 \text{ ns}$
13. 512 cycle of burst refresh must be executed within 8ms before and after self refresh in order to meet refresh specification (LL-Ver)
14. If \overline{RAS} goes high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
15. $tASC$, $tCAH$ are referenced to the earlier \overline{CAS} falling edge.
16. tCP is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
17. $tcWD$ is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
18. $tcWL$ is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.



19. $tCSR$ is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
20. $tCHR$ is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low



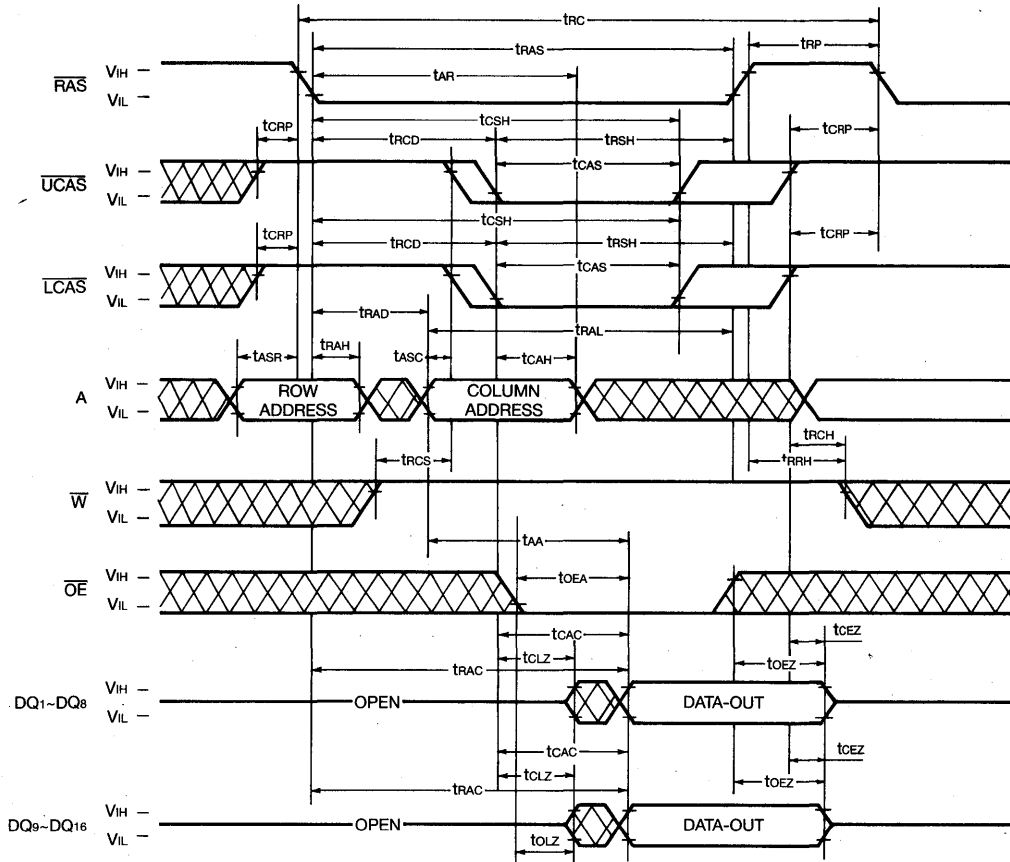
21. t_{DS} , t_{DH} , is independently specified for lower byte $D_{IN(1-8)}$, upper byte $D_{IN(9-16)}$.



TIMING DIAGRAM

WORD READ CYCLE

NOTE : DIN=OPEN

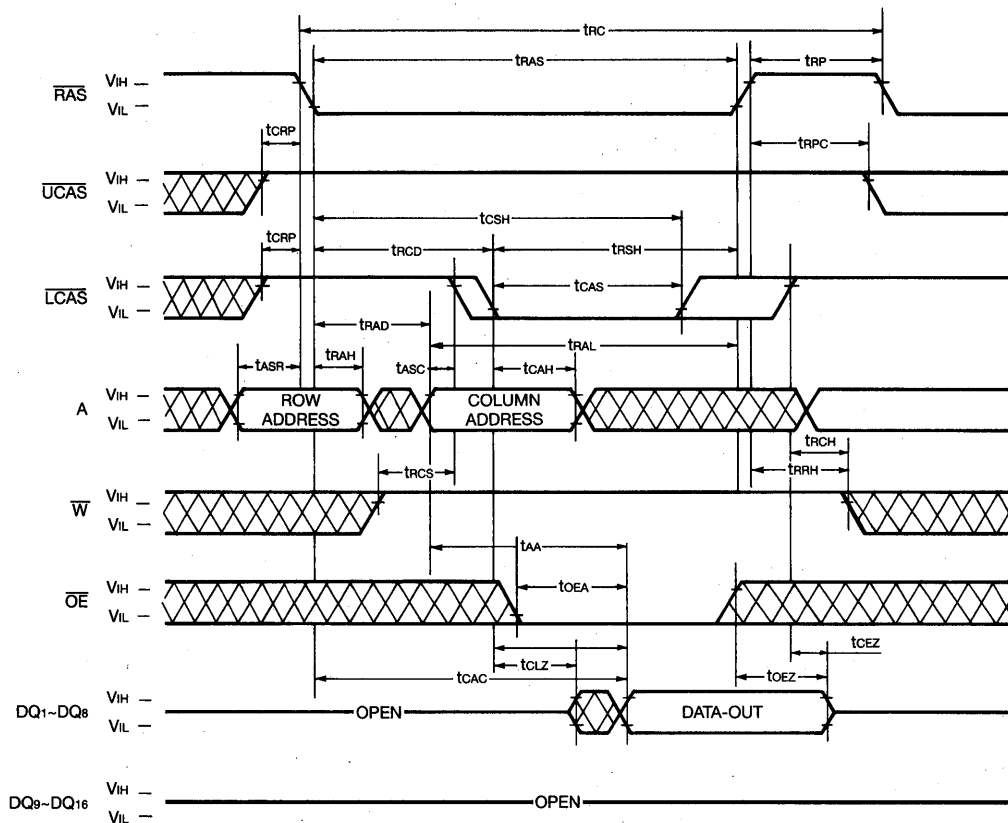


Don't Care

TIMING DIAGRAM

LOWER BYTE READ CYCLE

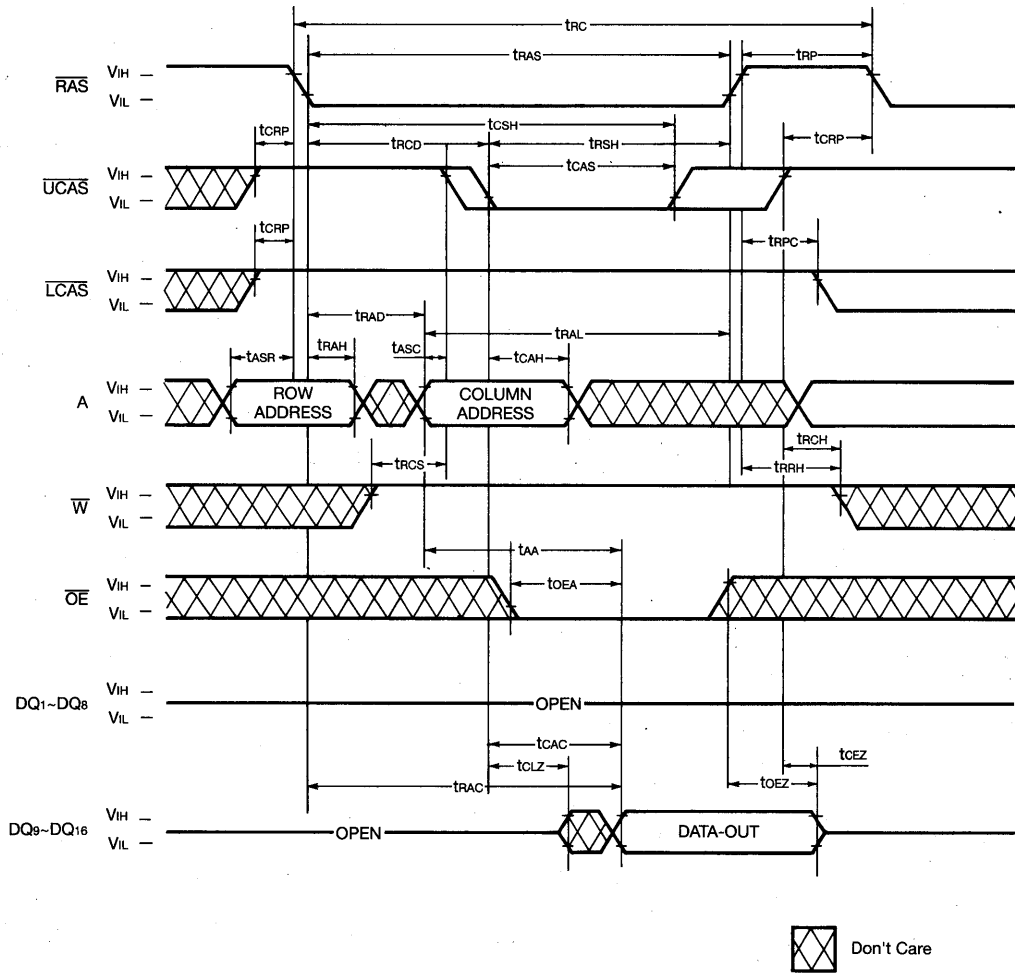
NOTE : DIN=OPEN



 Don't Care

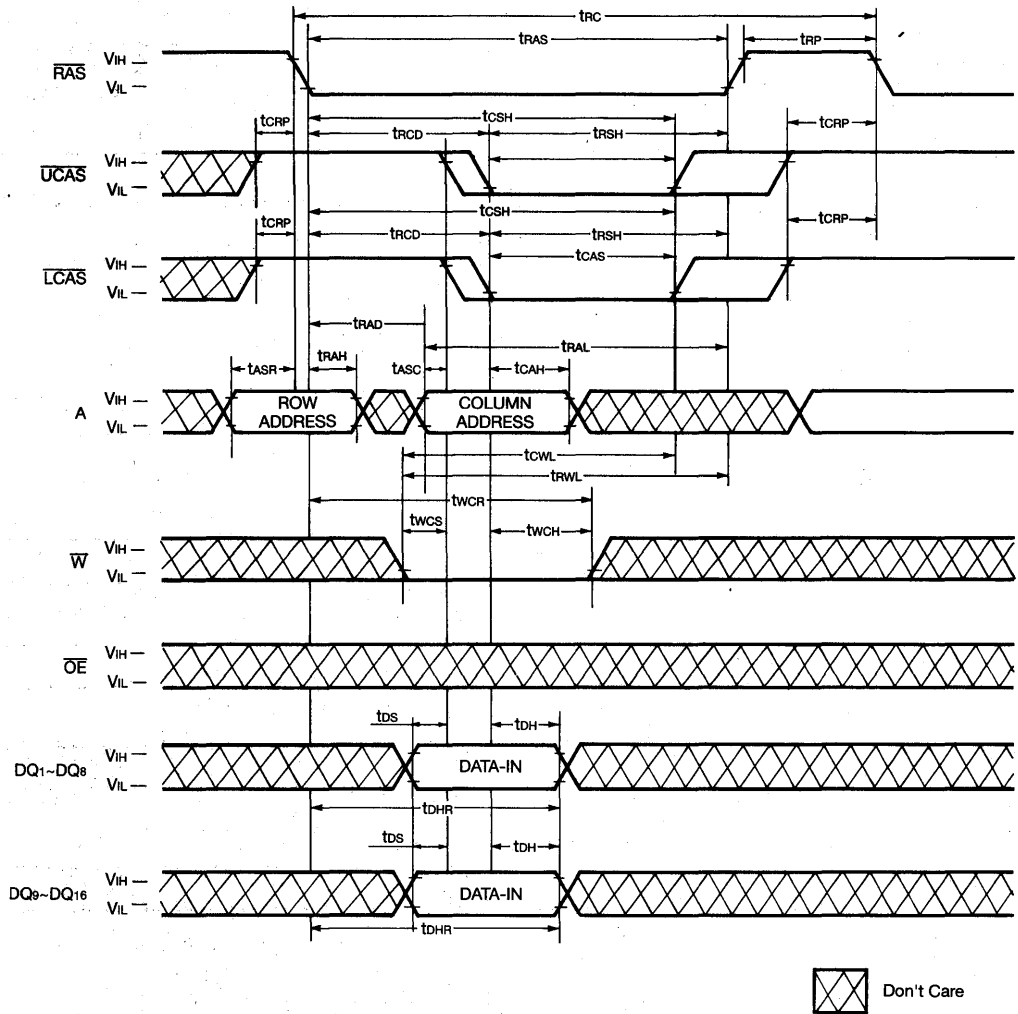
UPPER BYTE READ CYCLE

NOTE : DIN=OPEN



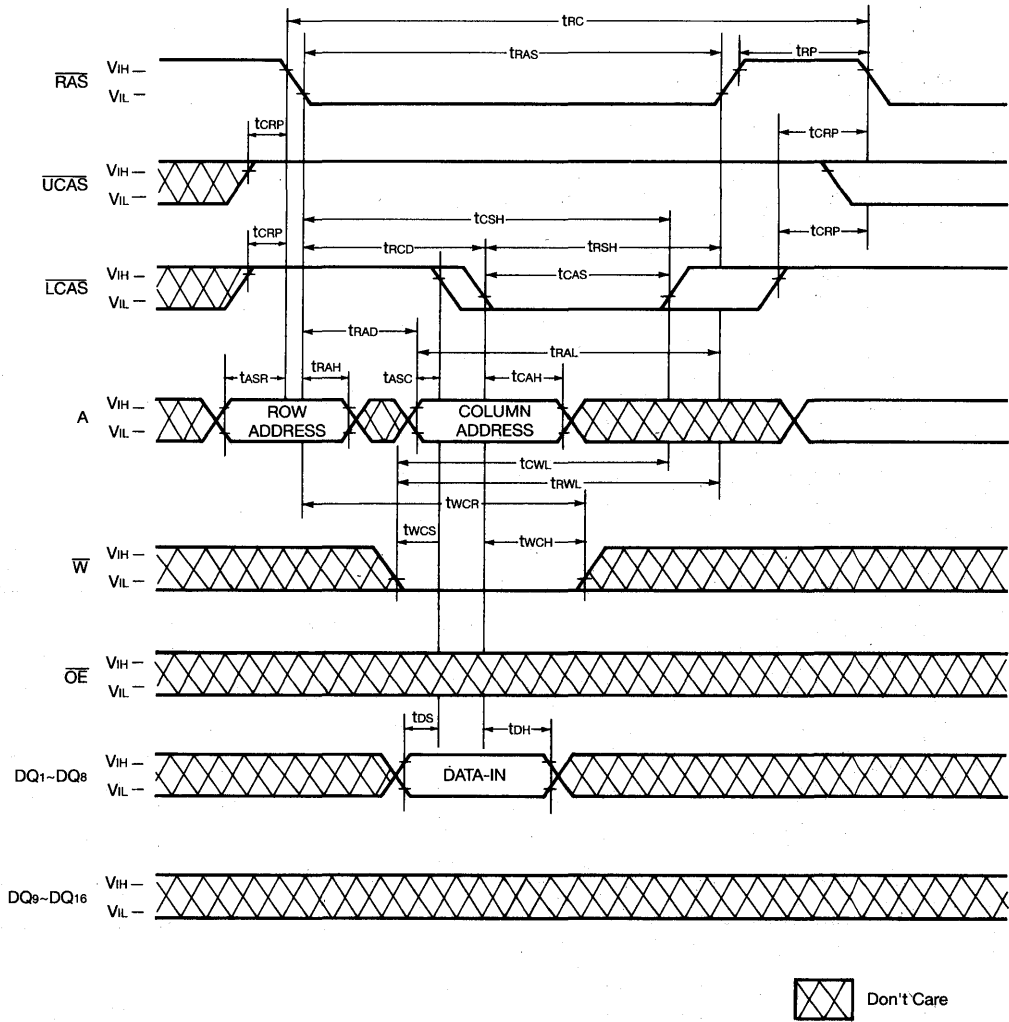
WORD WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

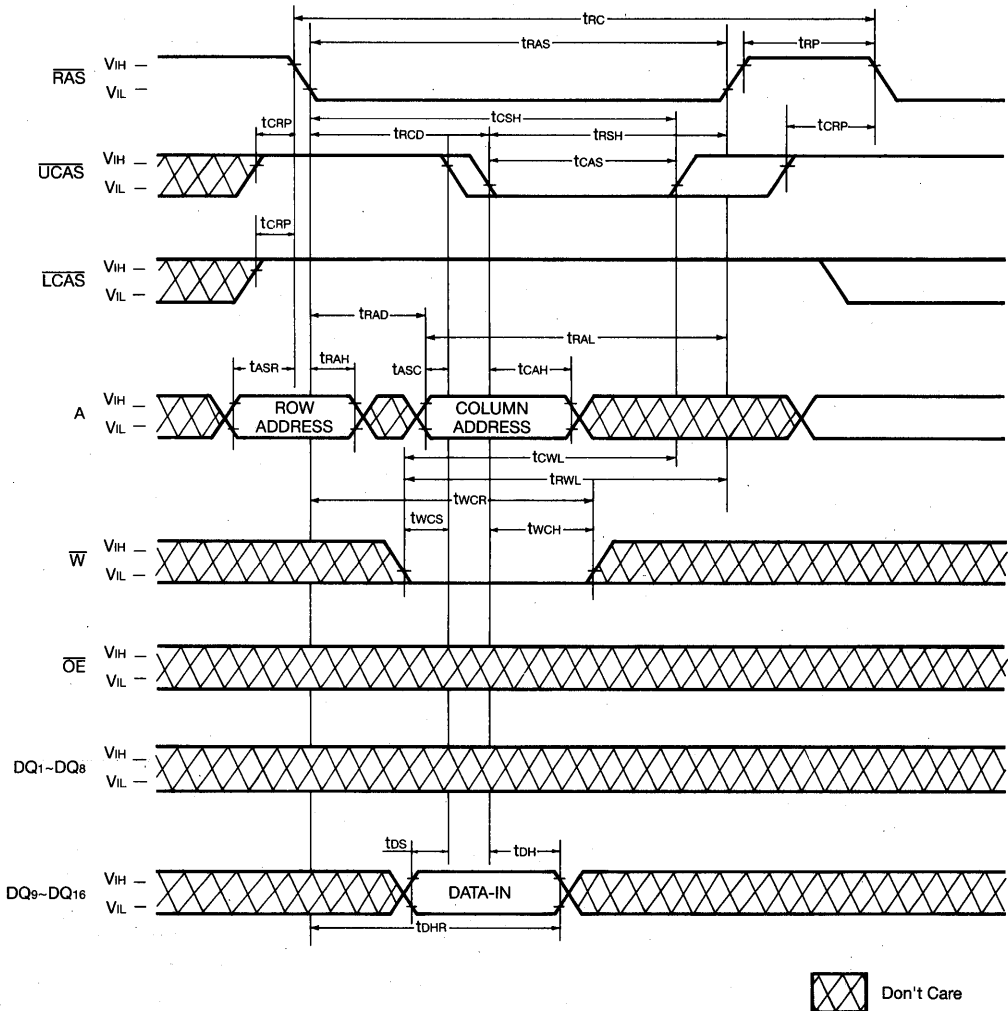
NOTE : DOUT=OPEN



4

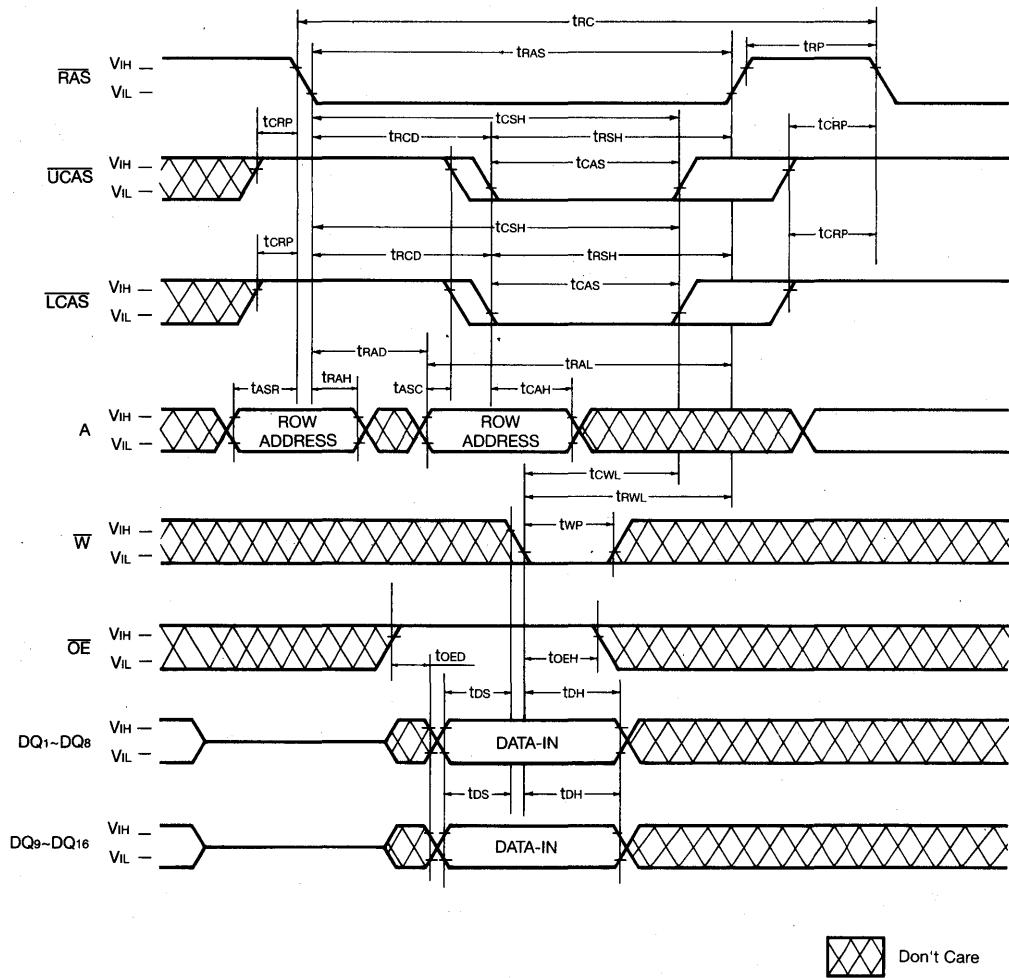
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT=OPEN



WORD WRITE CYCLE (OE CONTROLLED WRITE)

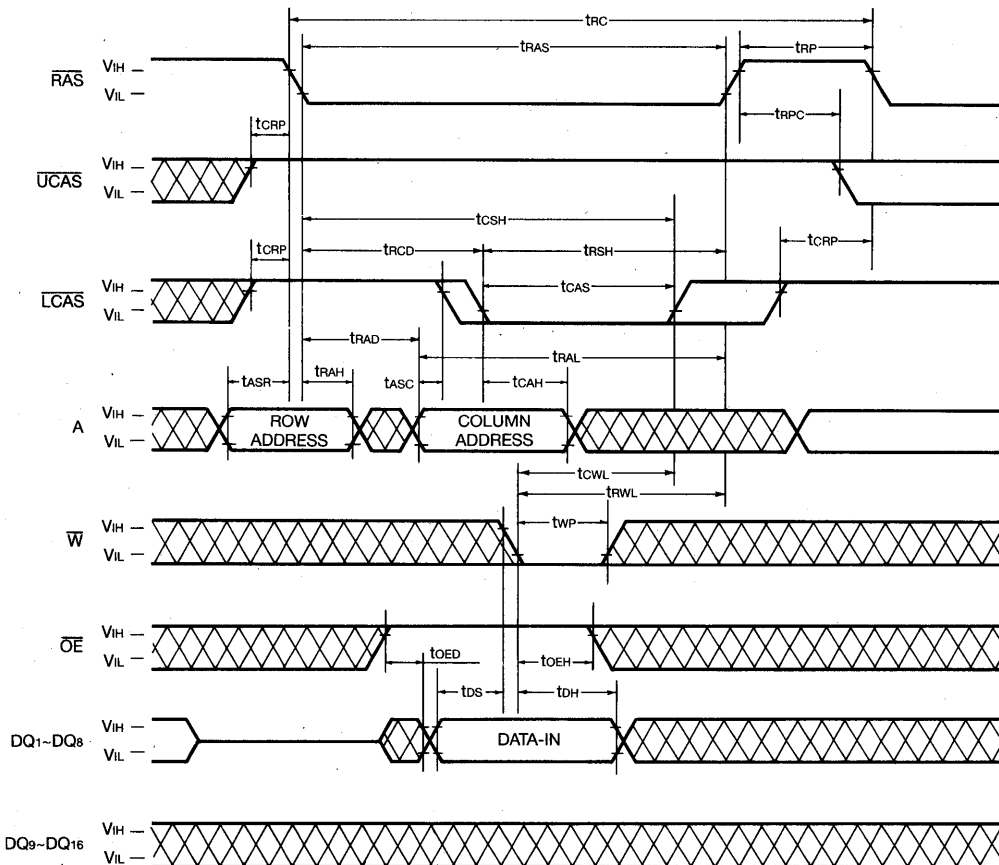
NOTE : DOUT=OPEN



4

LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

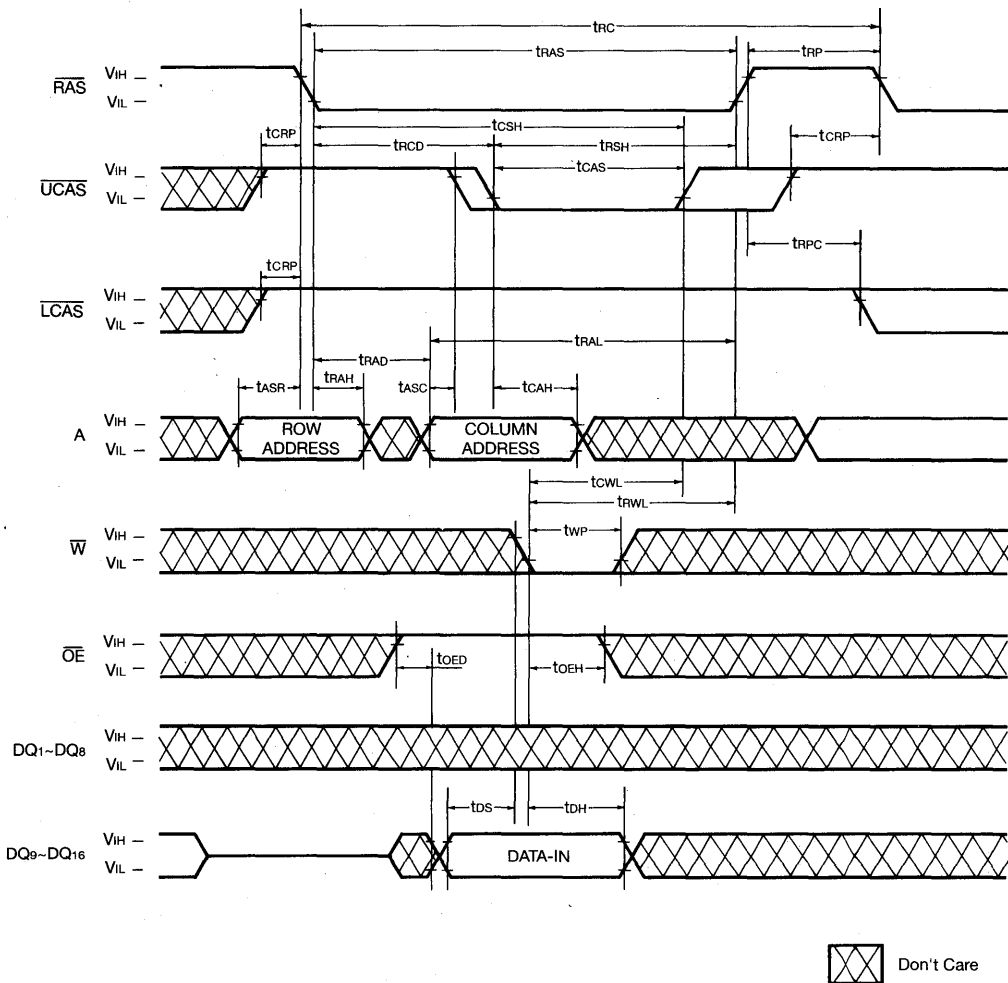
NOTE : DOUT=OPEN



 Don't Care

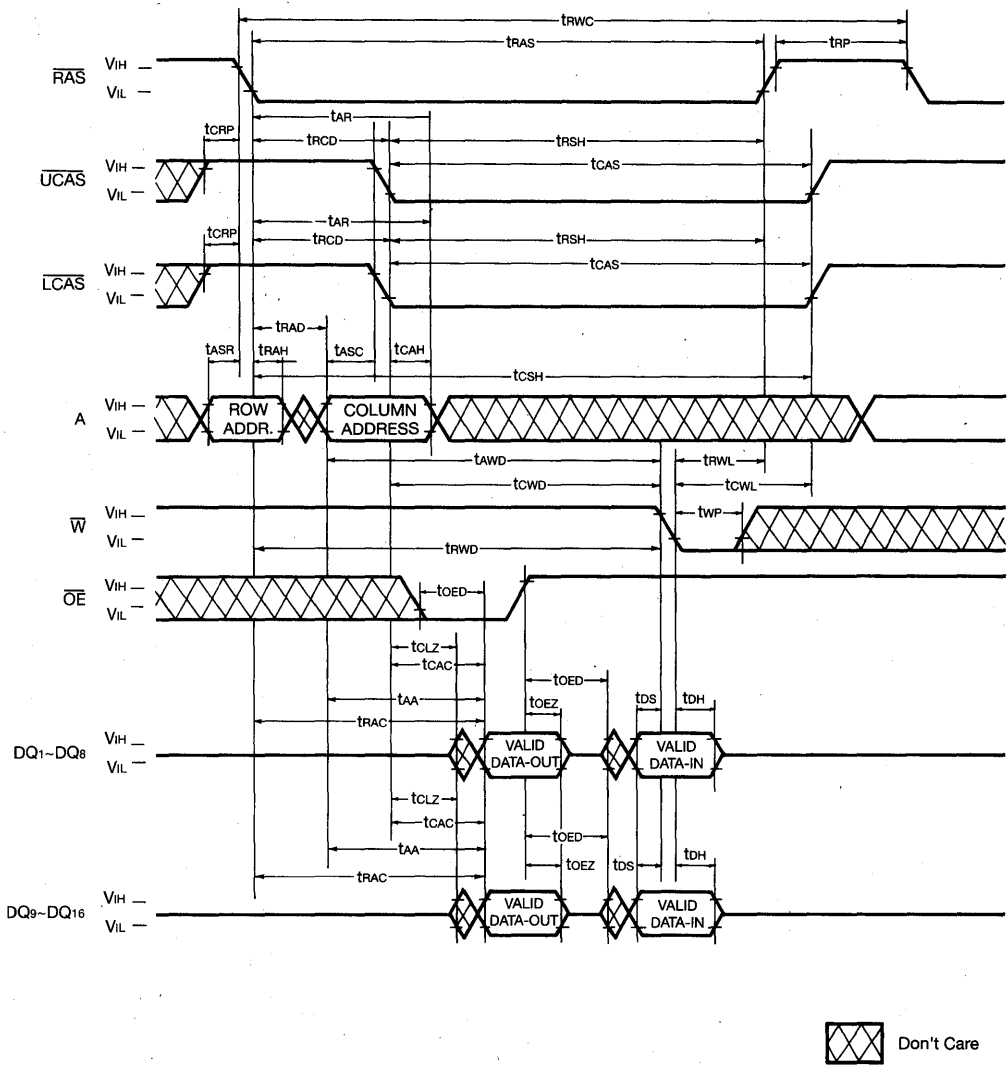
UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : Dout=OPEN

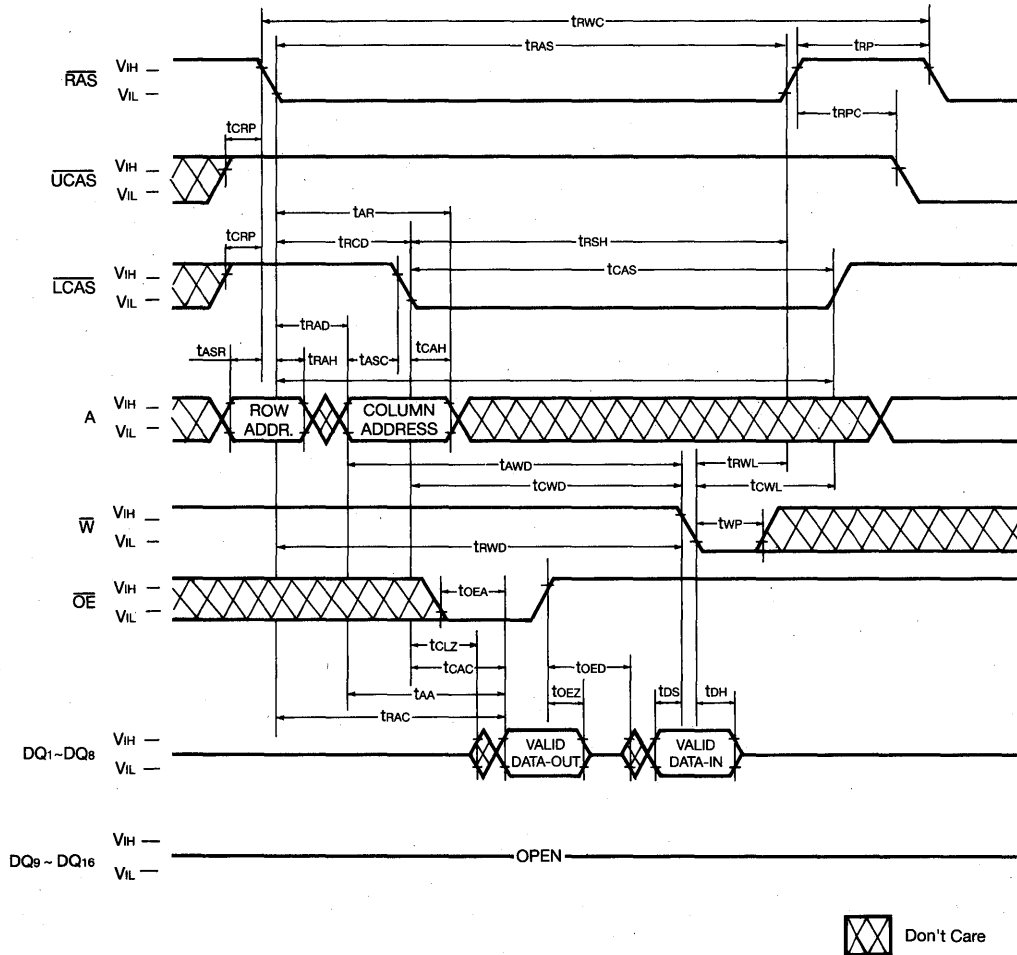


4

WORD READ-MODIFY-WRITE CYCLE

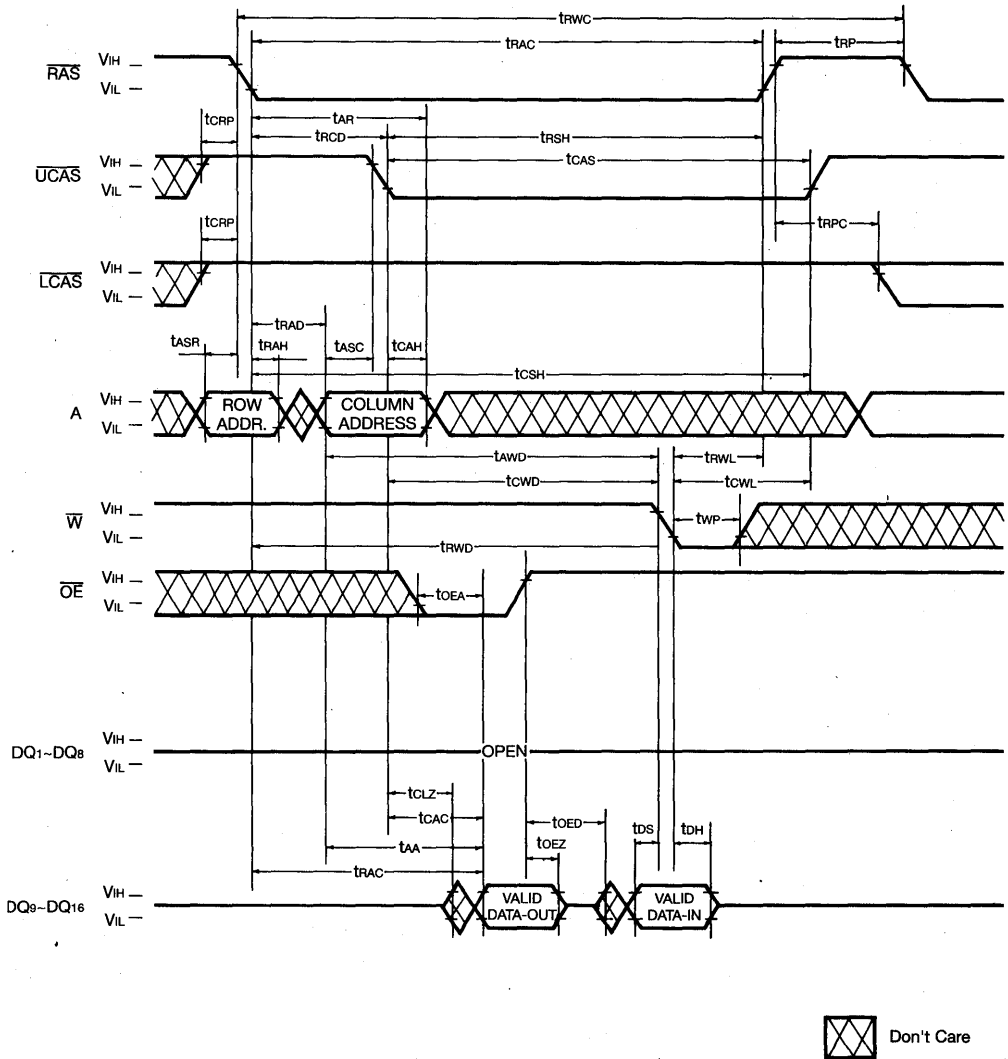


LOWER-BYTE READ-MODIFY-WRITE CYCLE

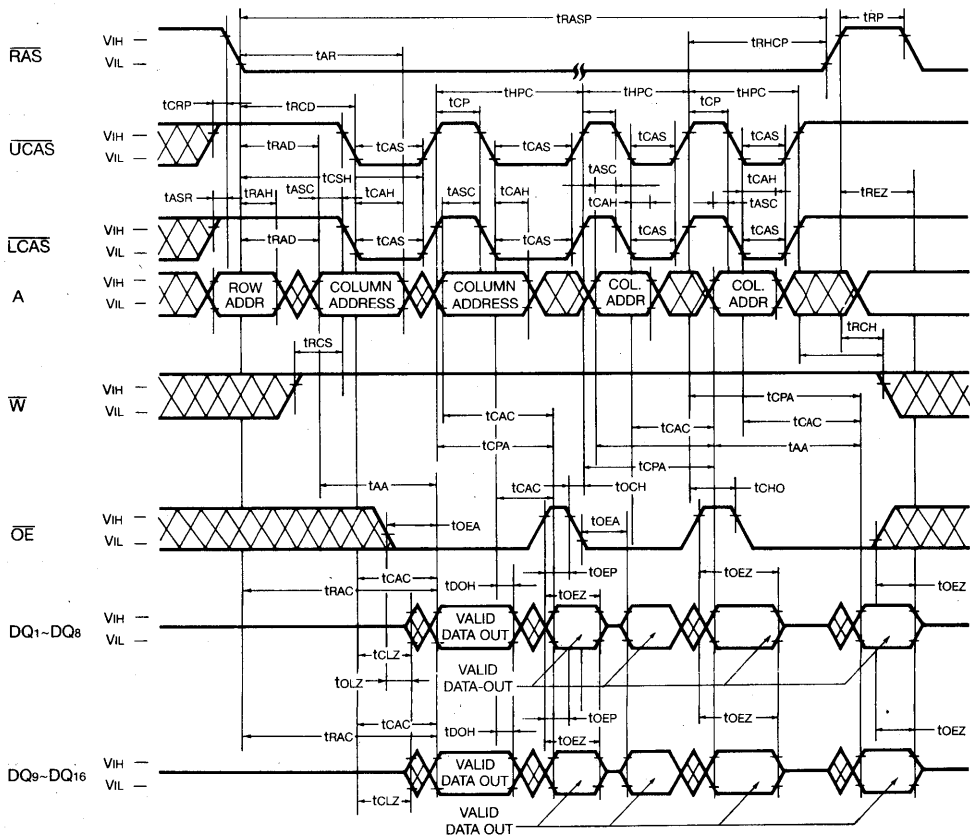


4

UPPER-BYTE READ-MODIFY-WRITE CYCLE

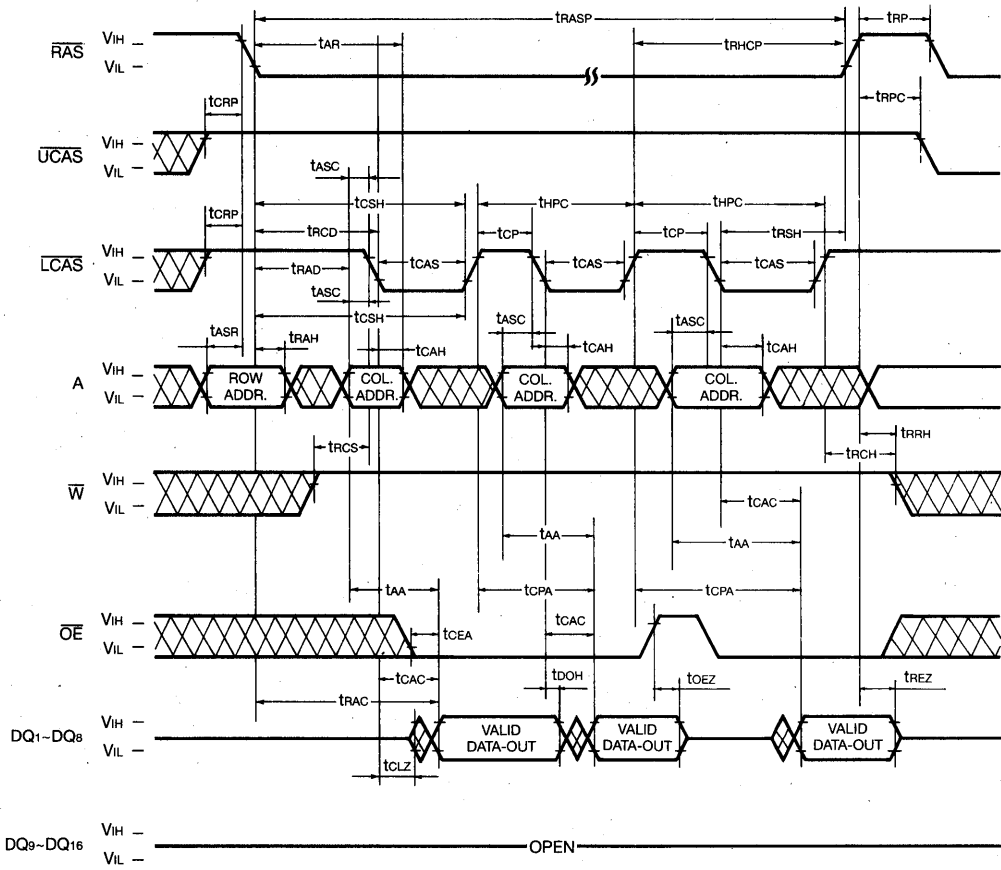


HYPER PAGE MODE WORD READ CYCLE



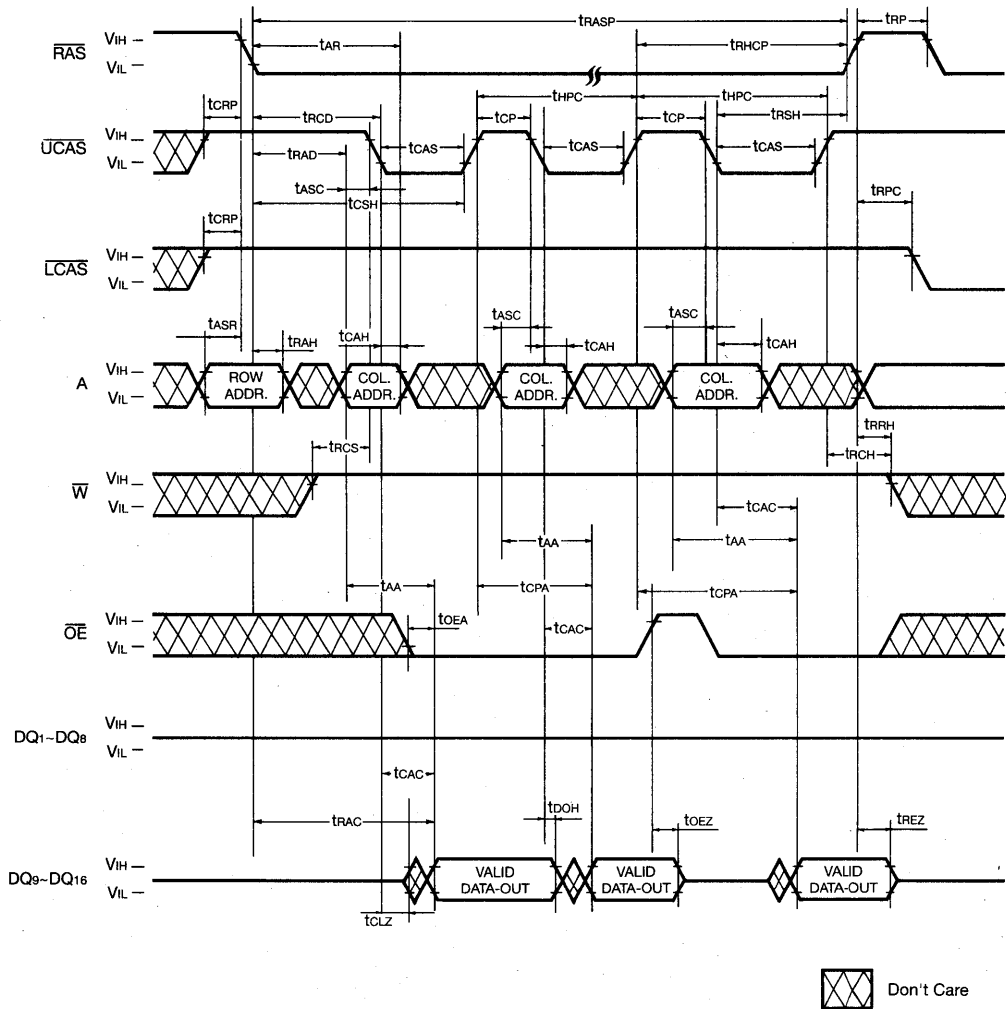
4

HYPER PAGE MODE LOWER BYTE READ CYCLE



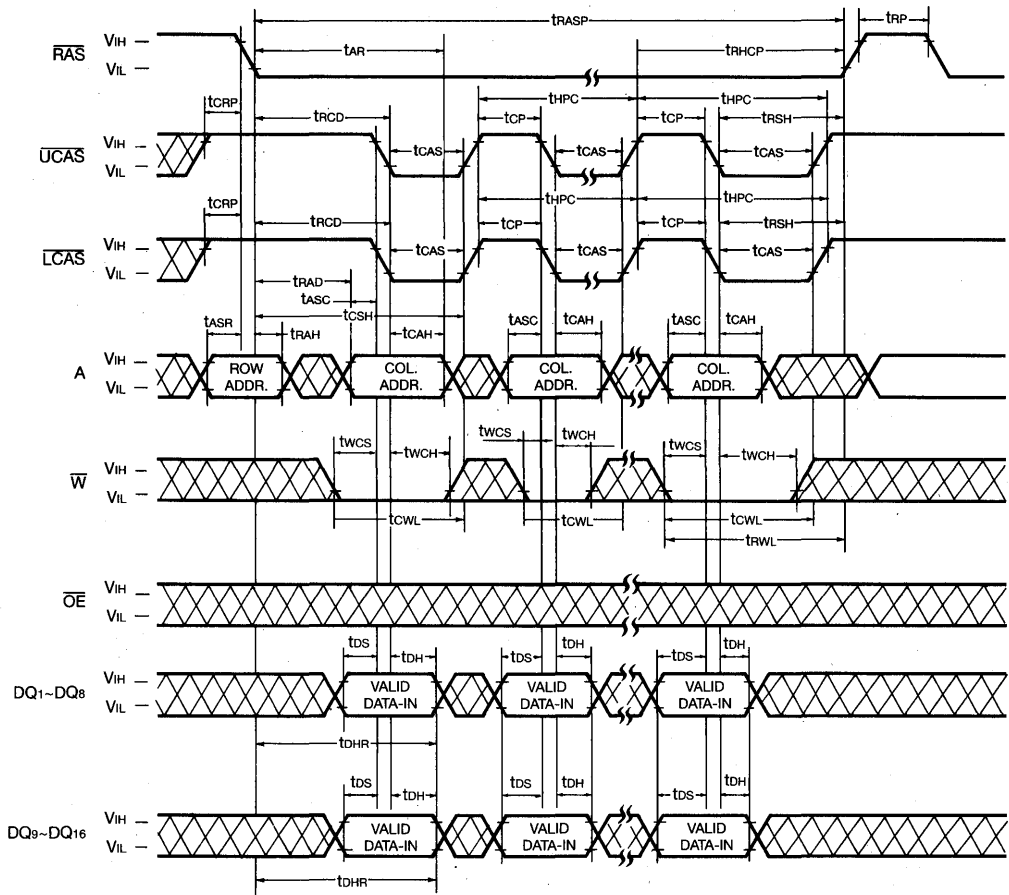
 Don't Care

HYPER PAGE MODE UPPER BYTE READ CYCLE



HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

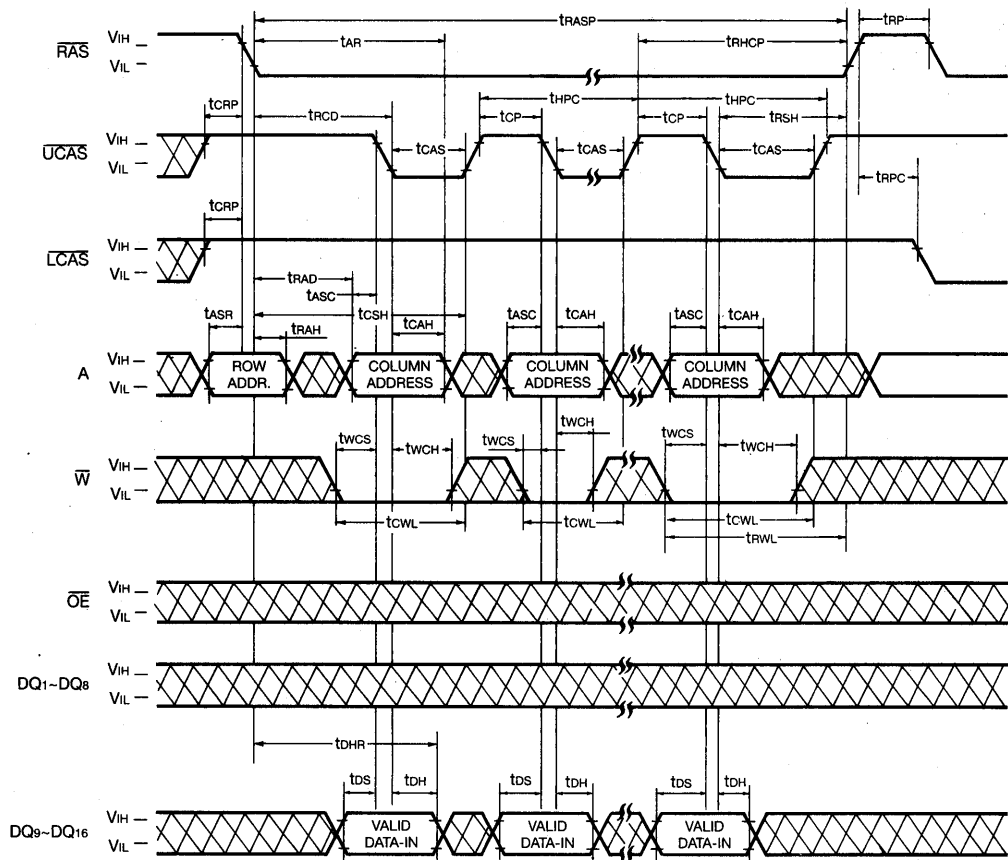
NOTE : DOUT=OPEN



 Don't Care

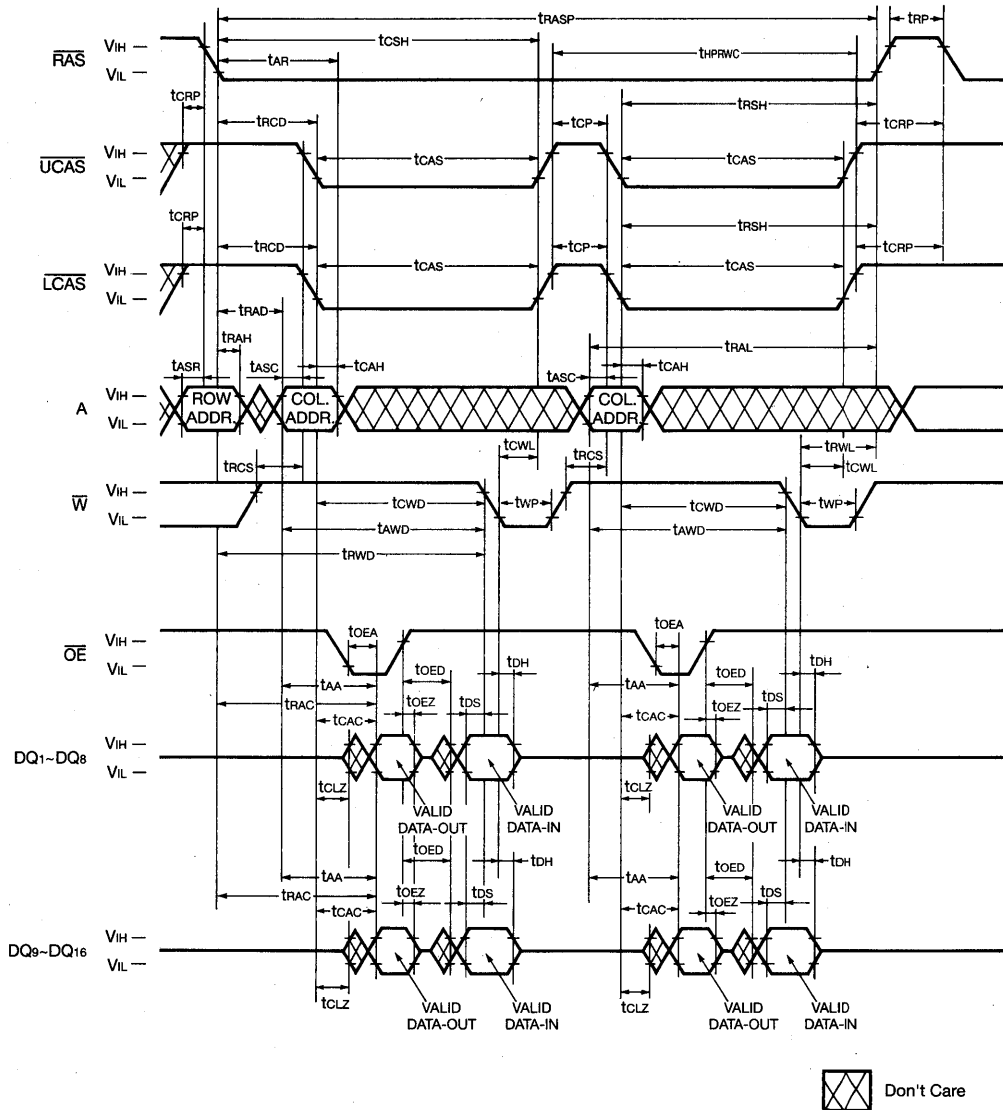
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT}=OPEN



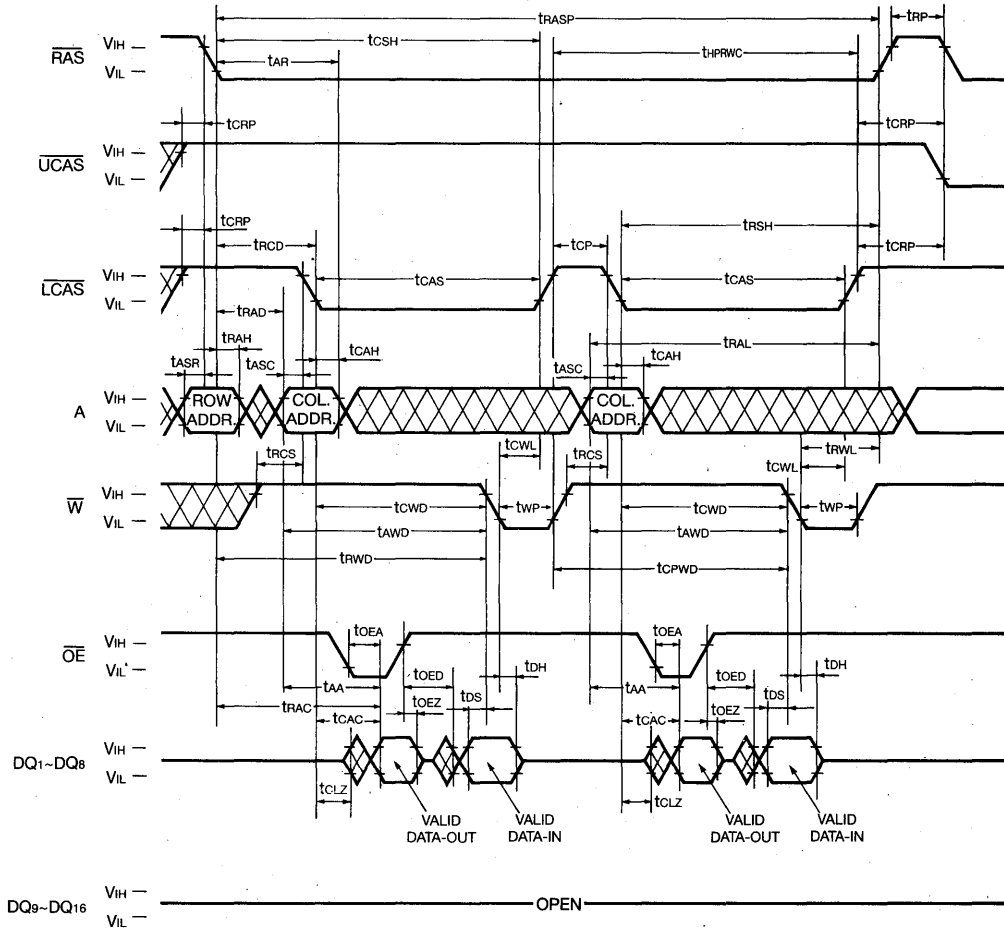
 Don't Care

HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



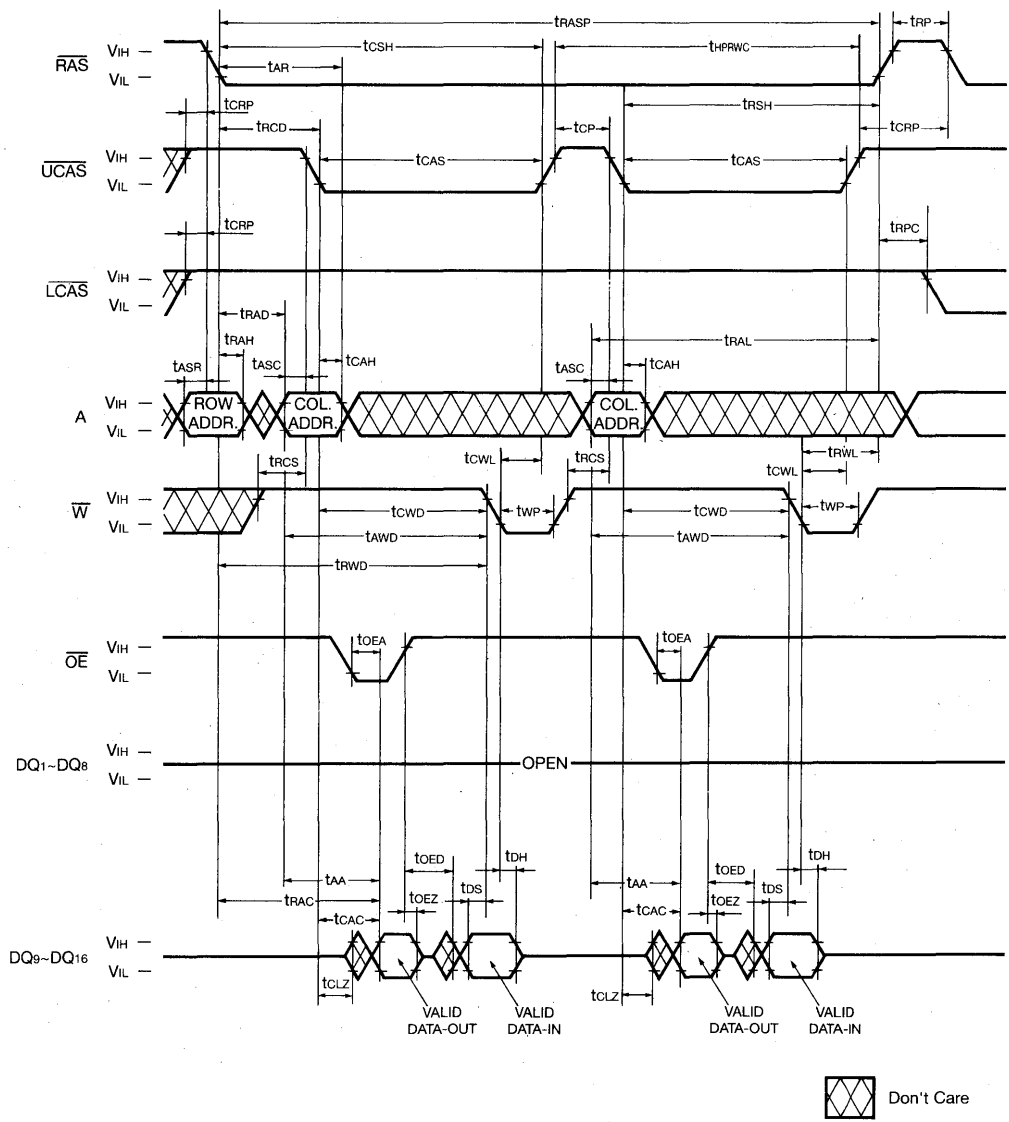
4

HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



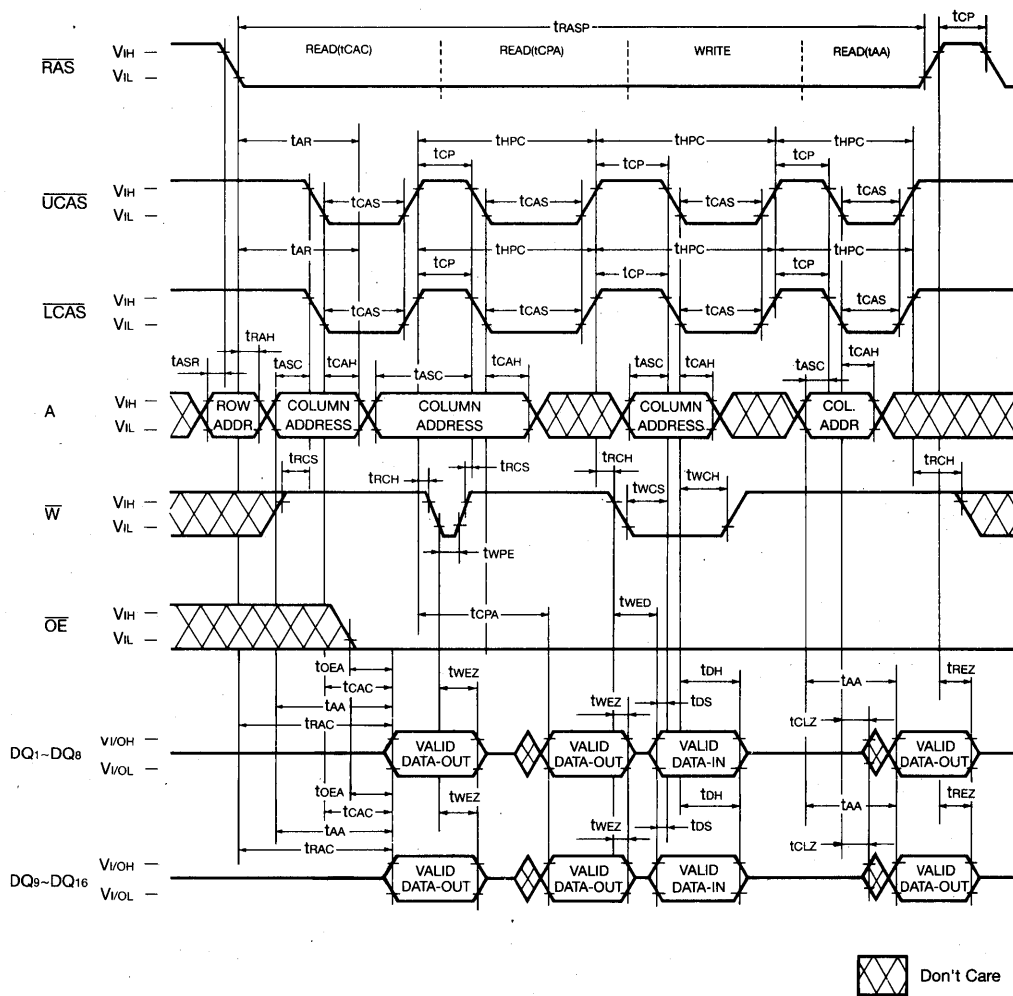
 Don't Care

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



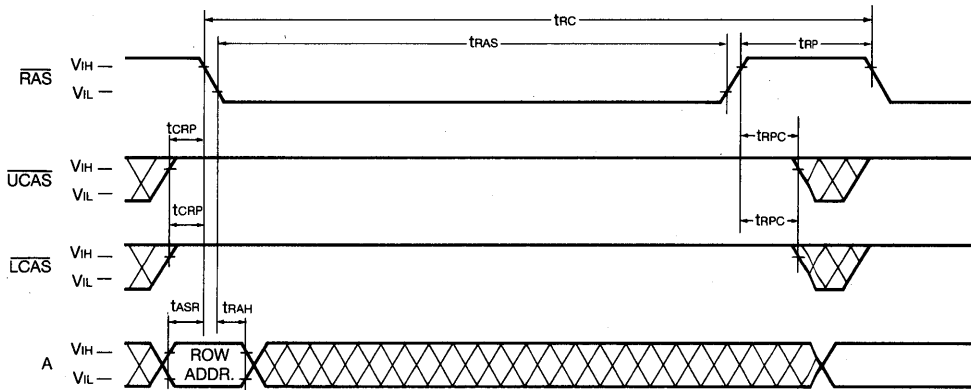
4

HYPER PAGE READ AND WRITE MIXED CYCLE



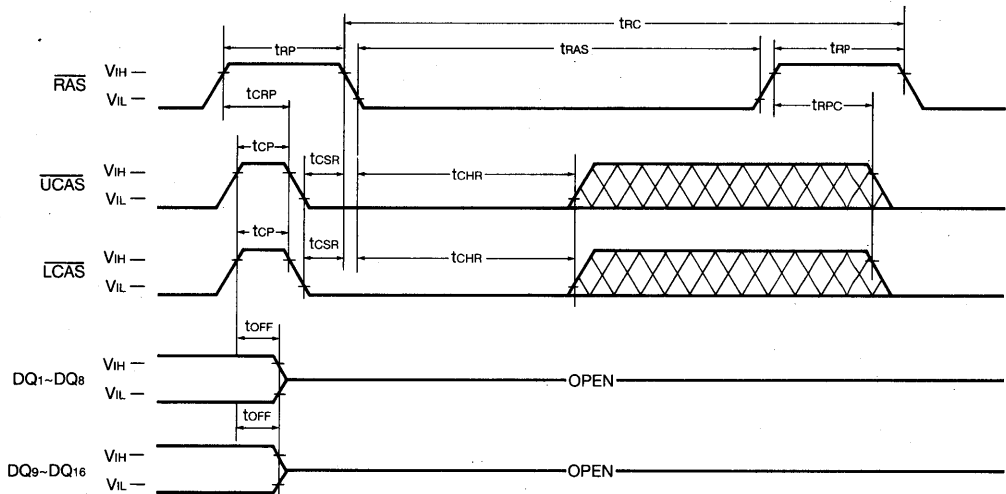
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} =Don't Care
 D_{OUT} =OPEN



CAS-BEFORE-RAS REFRESH CYCLE

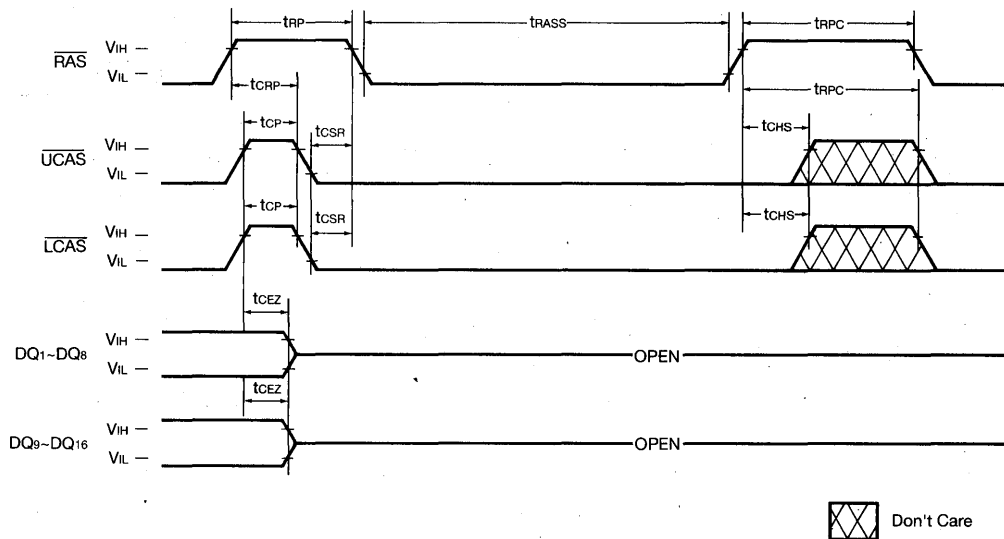
NOTE : \bar{W} , \bar{OE} , A=Don't Care



 Don't Care

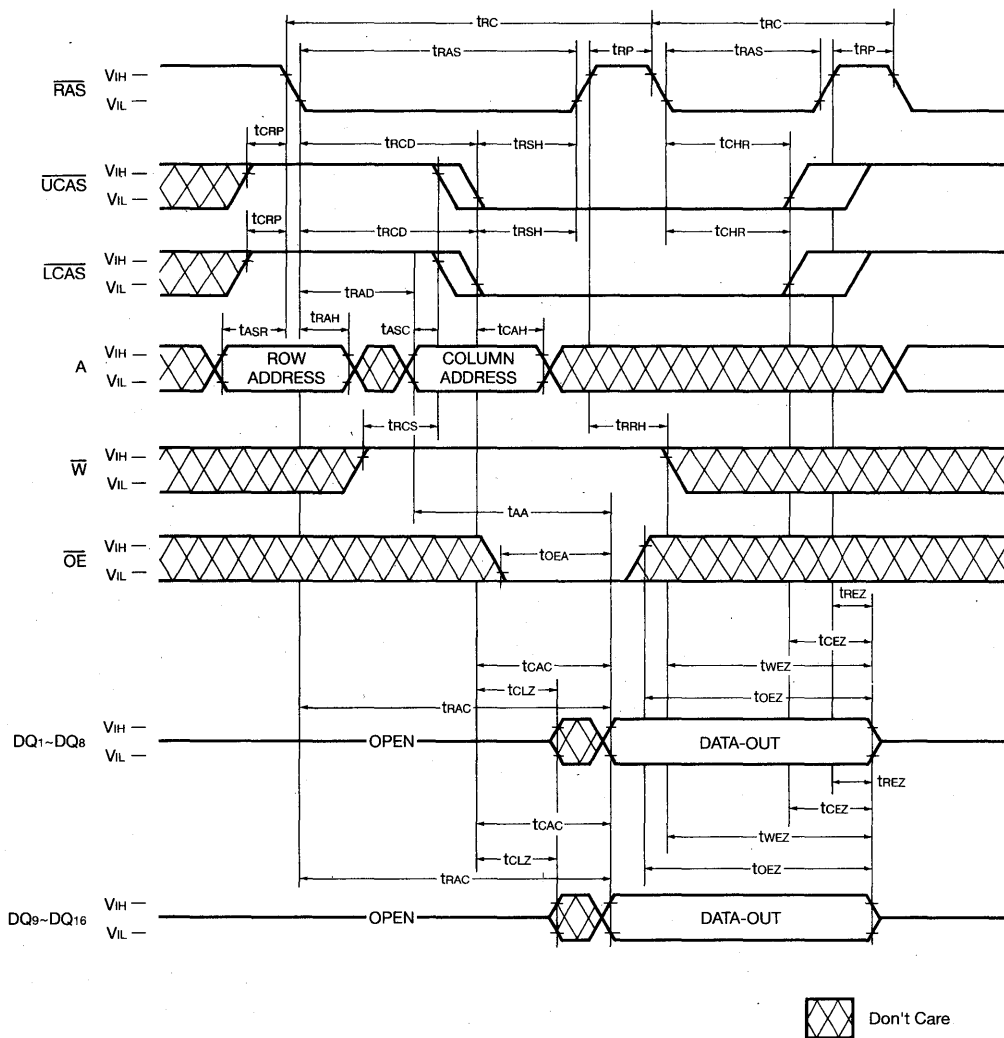
CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-Version)

NOTE : \bar{W} , \bar{OE} , A=Don't Care



 Don't Care

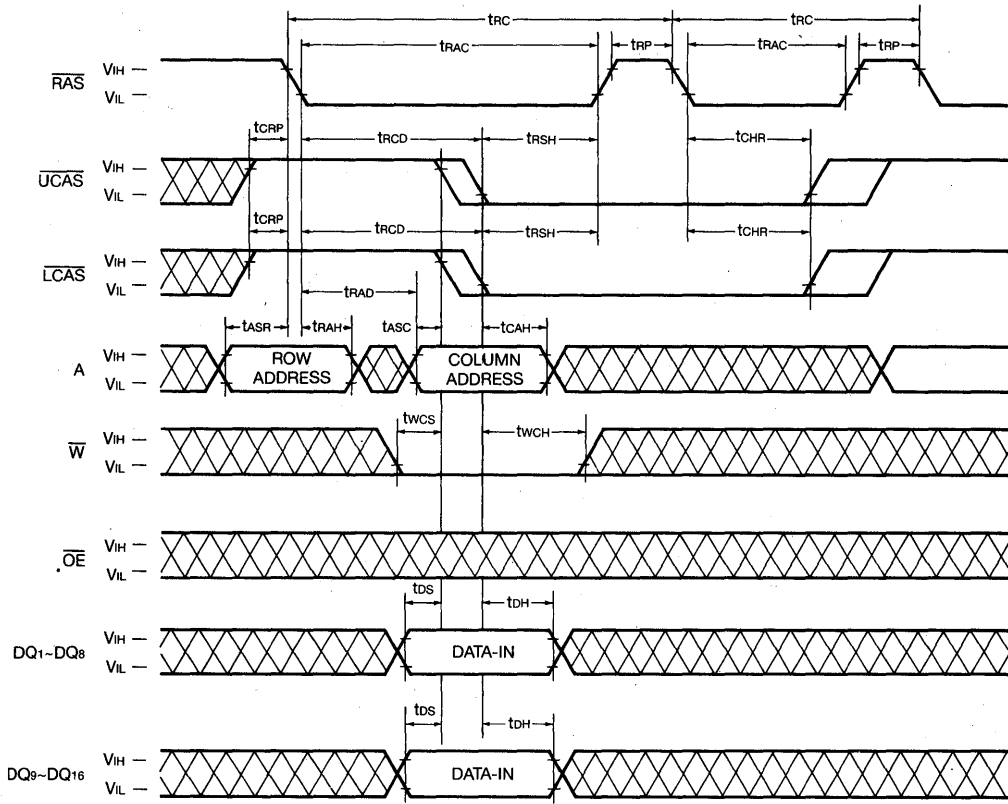
HIDDEN REFRESH CYCLE (READ)



4

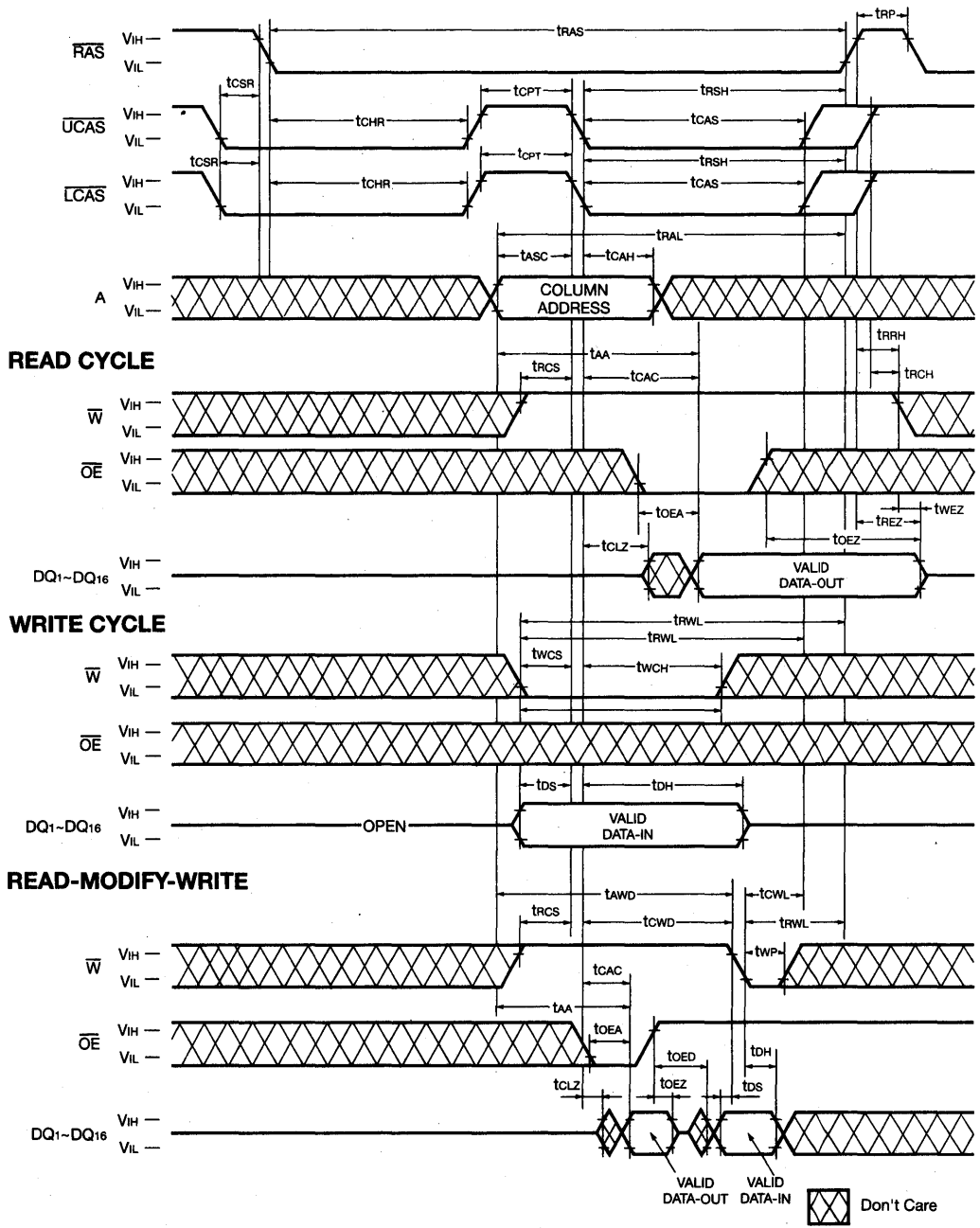
HIDDEN REFRESH CYCLE (WRITE)

NOTE : Dout=OPEN



 Don't Care

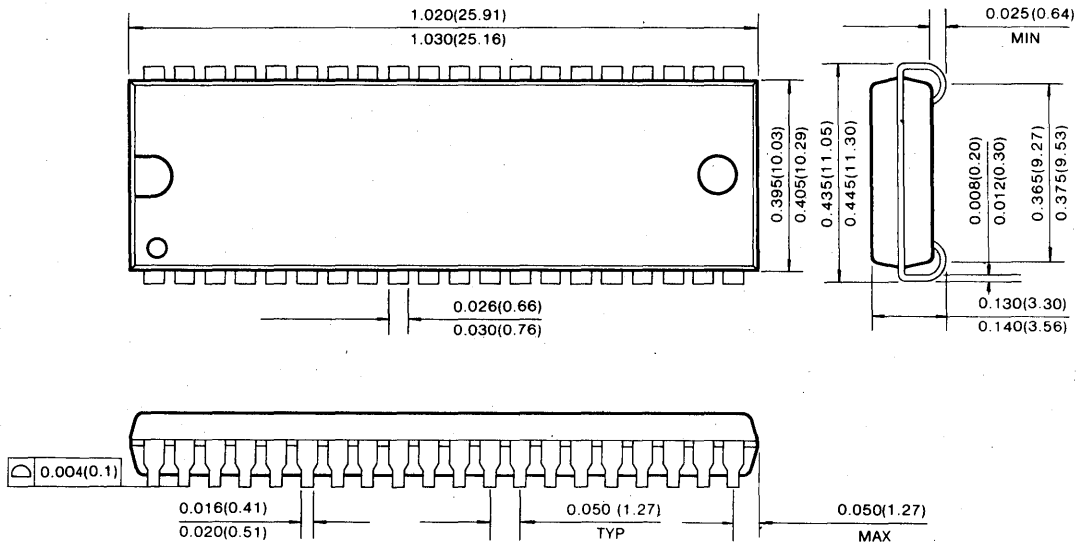
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



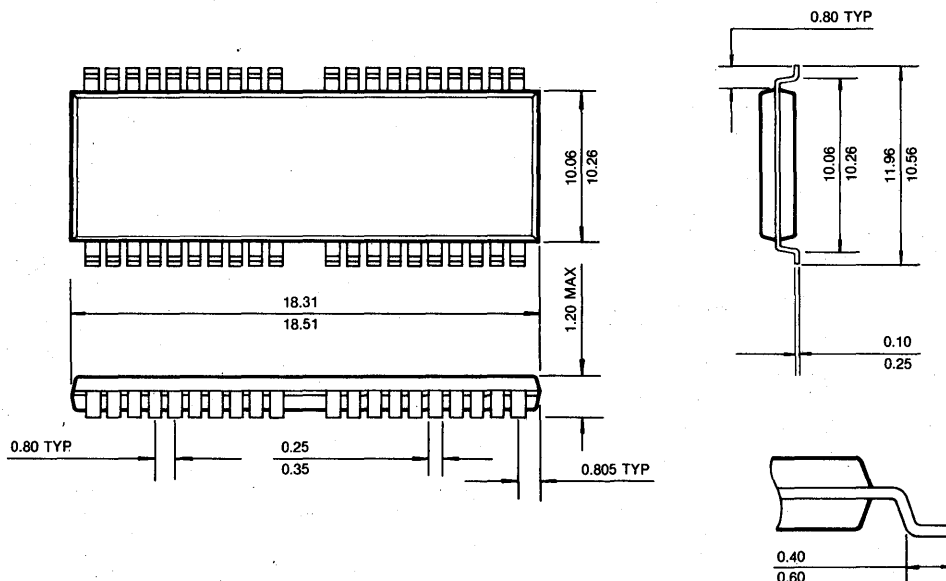
PACKAGE DIMENSION

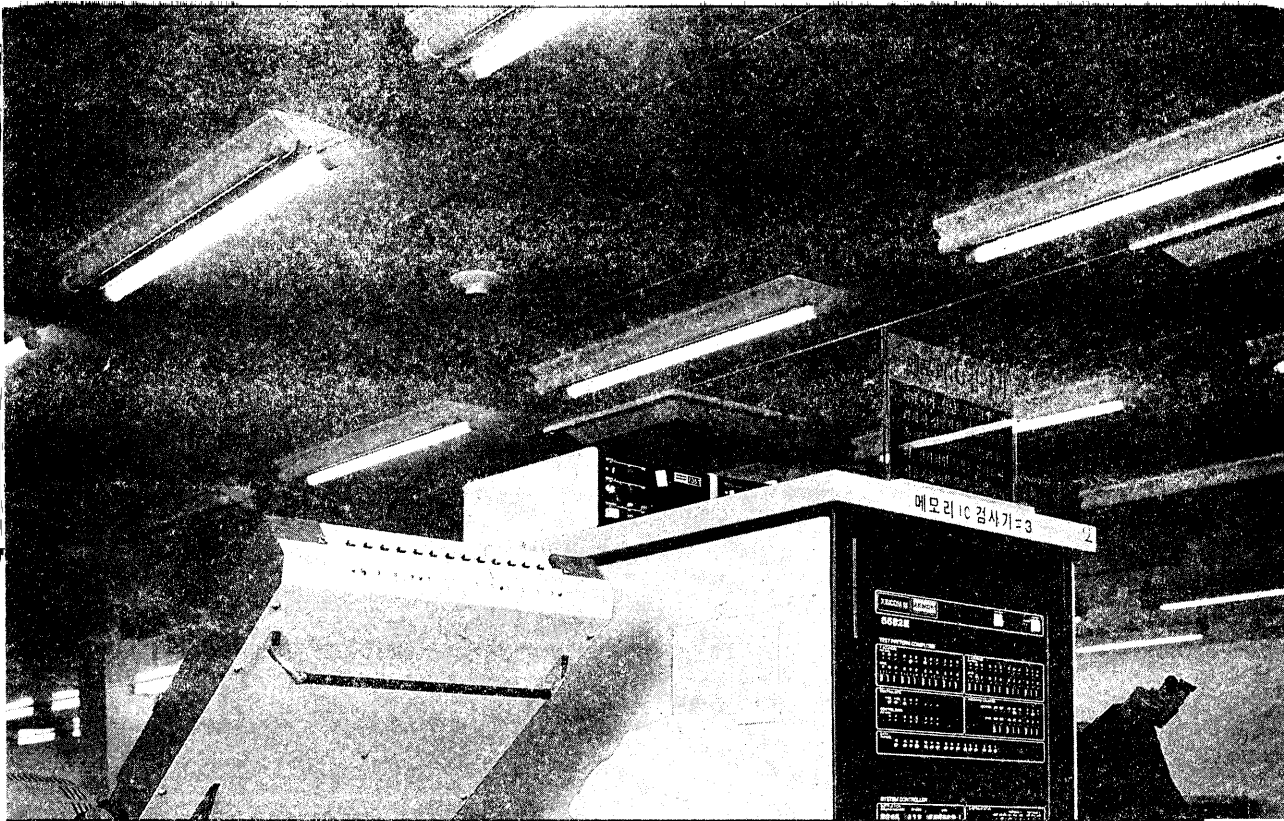
40-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)

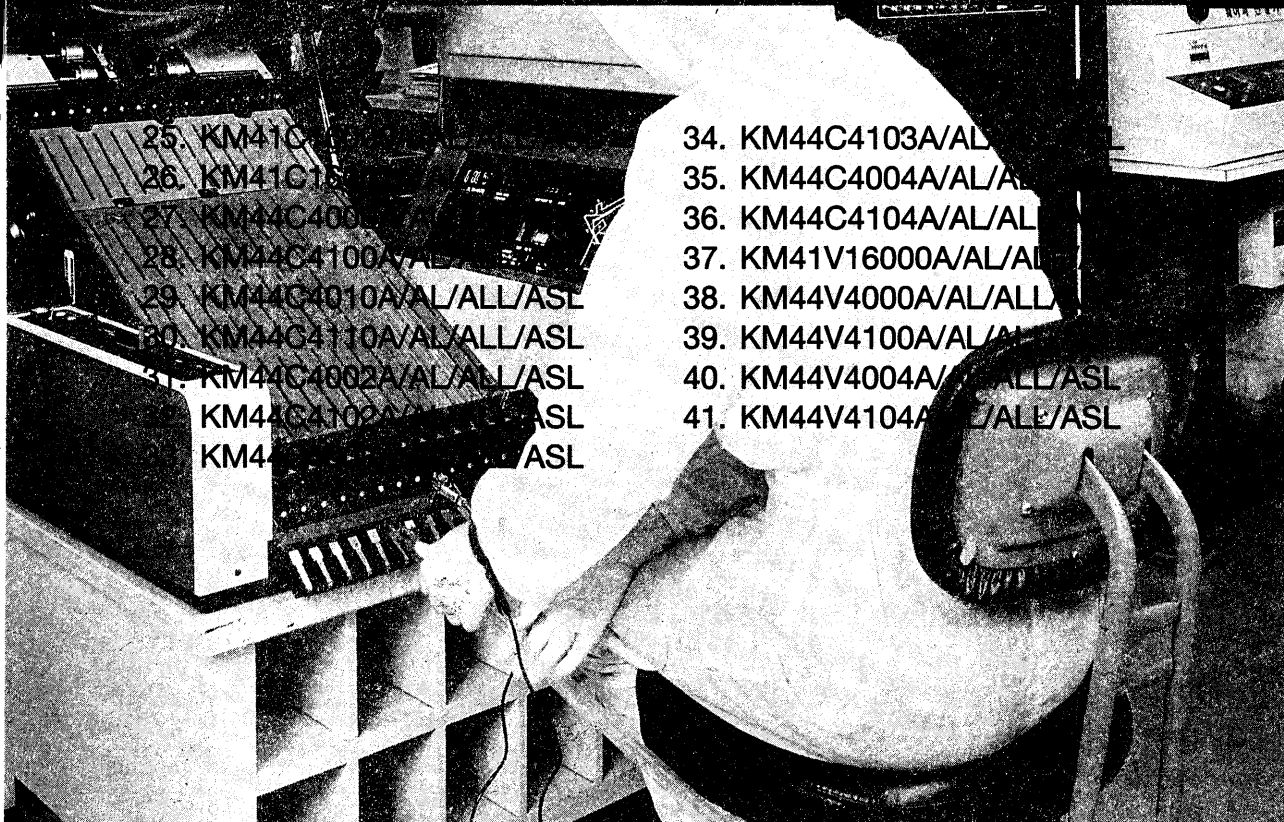


40 LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)
(Forward and Reverse Type)



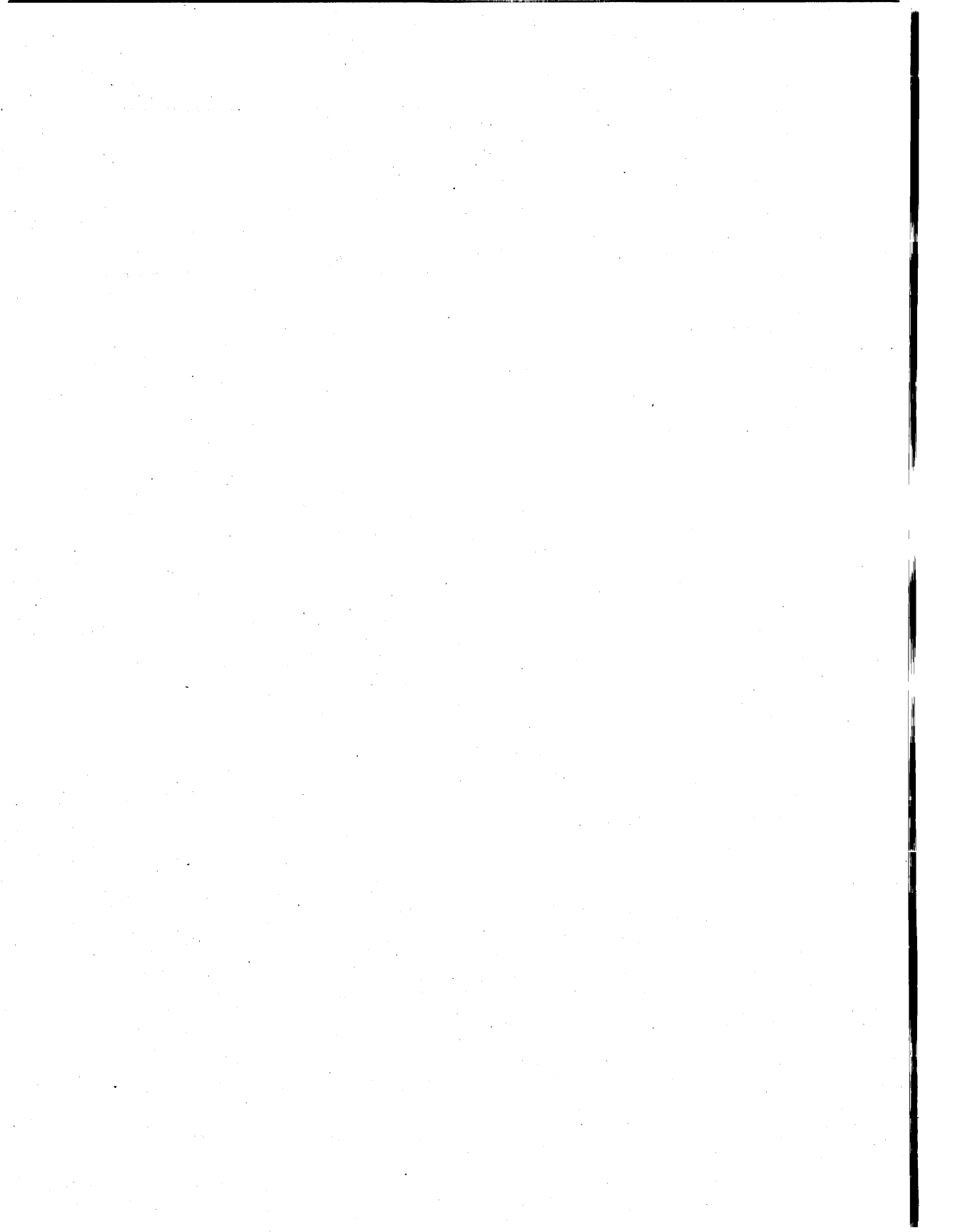


16M DRAM DATA SHEET 5



- 25. KM41C100A/AL/ASL
- 26. KM41C150A/AL/ASL
- 27. KM44C4000A/AL/ALL/ASL
- 28. KM44C4100A/AL/ALL/ASL
- 29. KM44C4010A/AL/ALL/ASL
- 30. KM44C4110A/AL/ALL/ASL
- 31. KM44C4002A/AL/ALL/ASL
- 32. KM44C4102A/AL/ALL/ASL
- 33. KM44C4103A/AL/ALL/ASL

- 34. KM44C4103A/AL/ALL/ASL
- 35. KM44C4004A/AL/ALL/ASL
- 36. KM44C4104A/AL/ALL/ASL
- 37. KM41V16000A/AL/ALL/ASL
- 38. KM44V4000A/AL/ALL/ASL
- 39. KM44V4100A/AL/ALL/ASL
- 40. KM44V4004A/AL/ALL/ASL
- 41. KM44V4104A/AL/ALL/ASL



16M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	trAC	tcAC	trC
KM41C16000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM41C16000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41C16000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41C16000A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Common I/O using Early Write
- Single+5.0V ± 10% power supply
- 4096 cycles/64ms refresh
- 4096 cycles/128ms (Low Power & Self Ref.)
- 4096 cycles/256ms (Super Low Power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

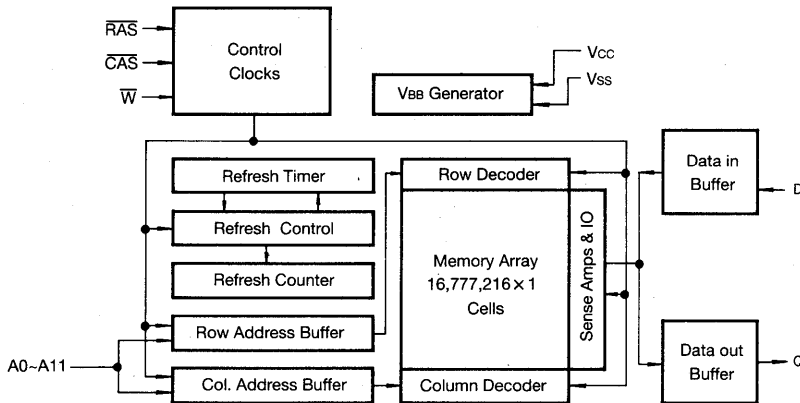
The Samsung KM41C16000A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM41C16000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and output are fully TTL compatible.

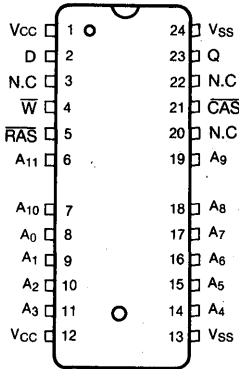
The KM41C16000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



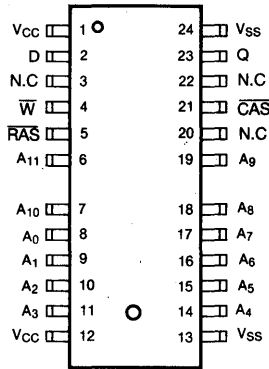
PIN CONFIGURATION (Top Views)

• KM41C16000 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



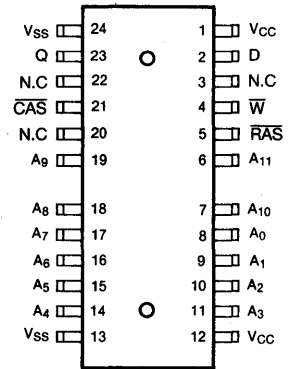
J : 400MIL
K : 300MIL

• KM41C16000 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM41C16000 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
Vcc	Power(+5.0V)
Vss	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @trc=min.)	KM41C16000A/AL/ALL/ASL-5	-	90	mA
	KM41C16000A/AL/ALL/ASL-6		80	mA
	KM41C16000A/AL/ALL/ASL-7		70	mA
	KM41C16000A/AL/ALL/ASL-8		60	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{IH}$)	KM41C16000A	-	2	mA
	KM41C16000AL		1	mA
	KM41C16000ALL		1	mA
	KM41C16000ASL		1	mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\text{CAS}=V_{IH}$, $\overline{\text{RAS}}$ Cycling @trc=min.)	KM41C16000A/AL/ALL/ASL-5	-	90	mA
	KM41C16000A/AL/ALL/ASL-6		80	mA
	KM41C16000A/AL/ALL/ASL-7		70	mA
	KM41C16000A/AL/ALL/ASL-8		60	mA
Fast Page Mode Current* ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{CAS}}$, Address Cycling @tpc=min.)	KM41C16000A/AL/ALL/ASL-5	-	80	mA
	KM41C16000A/AL/ALL/ASL-6		70	mA
	KM41C16000A/AL/ALL/ASL-7		60	mA
	KM41C16000A/AL/ALL/ASL-8		50	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{CC}-0.2V$)	KM41C16000A	-	1	mA
	KM41C16000AL		300	μA
	KM41C16000ALL		200	μA
	KM41C16000ASL		200	μA
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @trc=min.)	KM41C16000A/AL/ALL/ASL-5	-	90	mA
	KM41C16000A/AL/ALL/ASL-6		80	mA
	KM41C16000A/AL/ALL/ASL-7		70	mA
	KM41C16000A/AL/ALL/ASL-8		60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{\text{CAS}}=\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Cycling or 0.2V $\overline{\text{DIN}}=\overline{\text{Don't Care}}$ Trc=31.5μS(L-Ver.) 62.5μS(SL-Ver.), Tras ≤ min~300ns	KM41C16000AL	-	450	μA
	KM41C16000ASL		350	μA

5



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=A0-A11=Vcc-0.2V or 0.2V D,Q=Vcc-0.2V, 0.2V or Open	lccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)	Io(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: lcc1, lcc3, lcc4 and lcc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. lcc is specified as an average current. In lcc1 and lcc3, Address can be changed maximum two times while RAS=VIL. In lcc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	CIN1	-	7	pF
Input Capacitance (A0-A11)	CIN2	-	5	pF
Input Capacitance (RAS, CAS, W)	CIN3	-	7	pF
Input Capacitance (Q)	COUT	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 0.5V, See notes 1,2)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	tras	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trsh	13		15		20		20		ns	
CAS hold time	tCSH	50		60		70		80		ns	
CAS pulse width	tcas	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trcd	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trad	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	trcp	5		5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to \overline{RAS}	tAR	40		45		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to \overline{RAS}	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		20		20		ns	
Write command to \overline{CAS} lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to \overline{RAS}	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low Power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low Power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	tCWD	13		15		20		20		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	50		60		70		80		ns	8
Column address to \overline{W} delay time	tAWD	25		30		35		40		ns	8
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		15		15		ns	
\overline{RAS} to \overline{CAS} precharge time	tRPC	5		5		5		5		ns	
\overline{CAS} precharge time (\overline{C} - \overline{B} - \overline{R} counter test cycle)	tCPT	20		20		30		30		ns	
Access time from \overline{CAS} precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	53		60		70		75		ns	
\overline{CAS} precharge time (Fast Page mode)	tCP	10		10		10		10		ns	
\overline{RAS} pulse width (Fast Page mode)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	tRHCP	30		35		40		45		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
\bar{W} to \bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRP	10		10		10		10		ns	
\bar{W} to \bar{RAS} hold time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRH	10		10		10		10		ns	
\bar{RAS} pulse width (\bar{C} - \bar{B} - \bar{R} refresh)	tRASS	100		100		100		100		μ s	15
\bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	tRPS	90		110		130		150		ns	15
\bar{CAS} hold time (\bar{C} - \bar{B} - \bar{R} refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note 12)

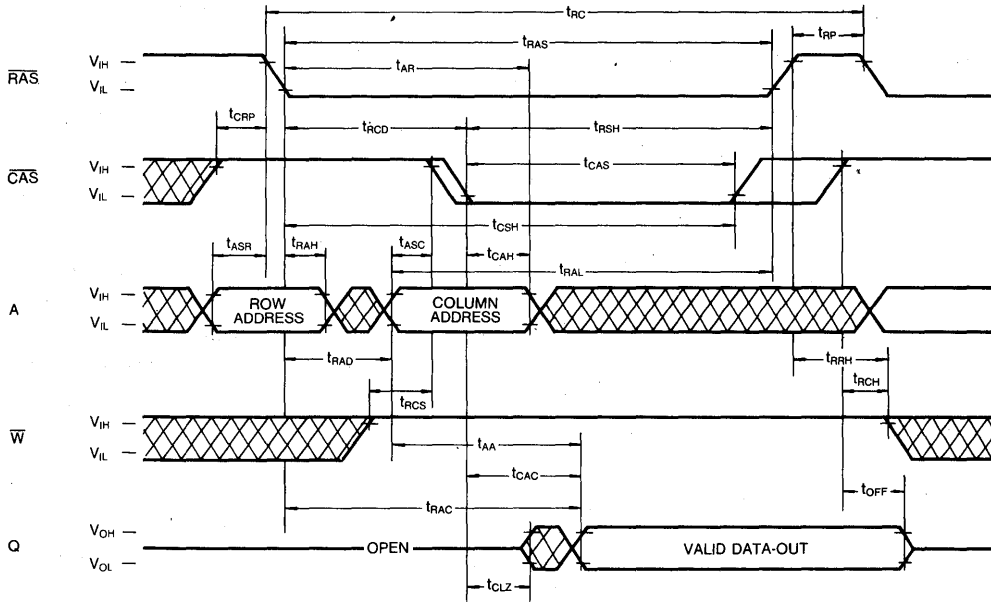
Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from \bar{RAS}	tRAC		55		65		75		85	ns	3,4,11
Access time from \bar{CAS}	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\bar{RAS} pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
\bar{RAS} hold time	tRSH	18		20		25		25		ns	
\bar{CAS} hold time	tCSH	55		65		75		85		ns	
Column address to \bar{RAS} lead time	tRAL	30		35		40		45		ns	
\bar{CAS} to \bar{W} delay time	tCWD	18		20		25		25		ns	8
\bar{RAS} to \bar{W} delay time	tRWD	55		65		75		85		ns	8
Column address to \bar{W} delay time	tAWD	30		35		40		45		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	58		65		75		80		ns	
\bar{RAS} pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	tCPA		35		40		45		50	ns	3

NOTES

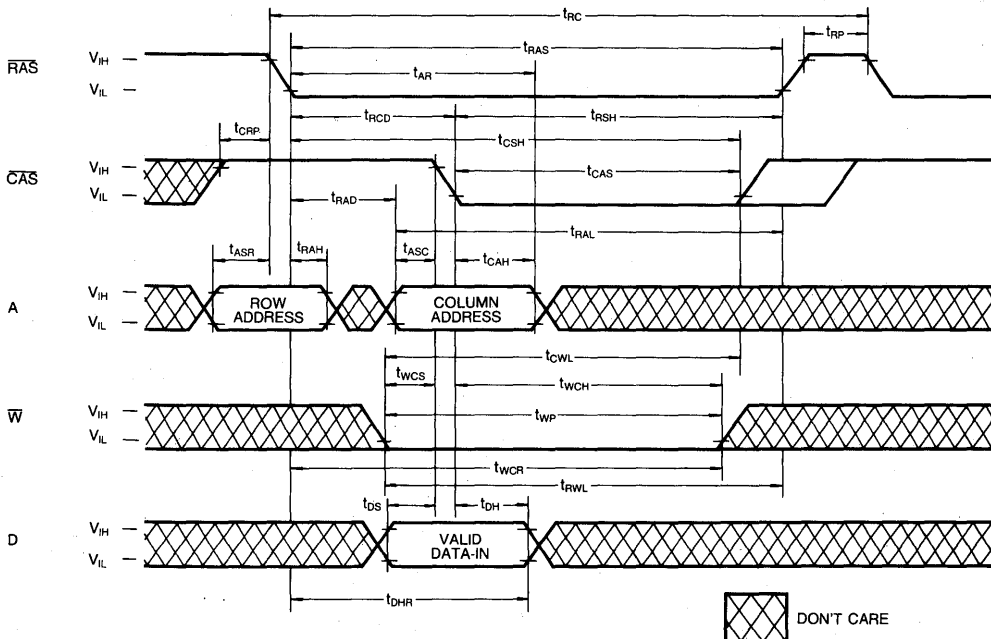
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RC}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RC}(\max)$ is specified as a reference point only. If t_{RC} is greater than the specified $t_{RC}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RC} \geq t_{RC}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE



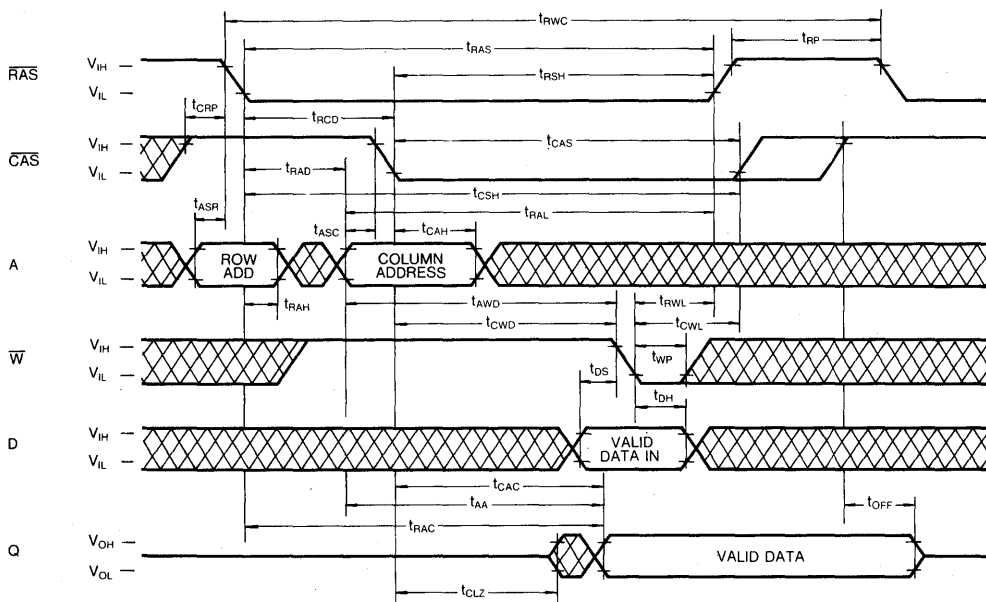
WRITE CYCLE (EARLY WRITE)



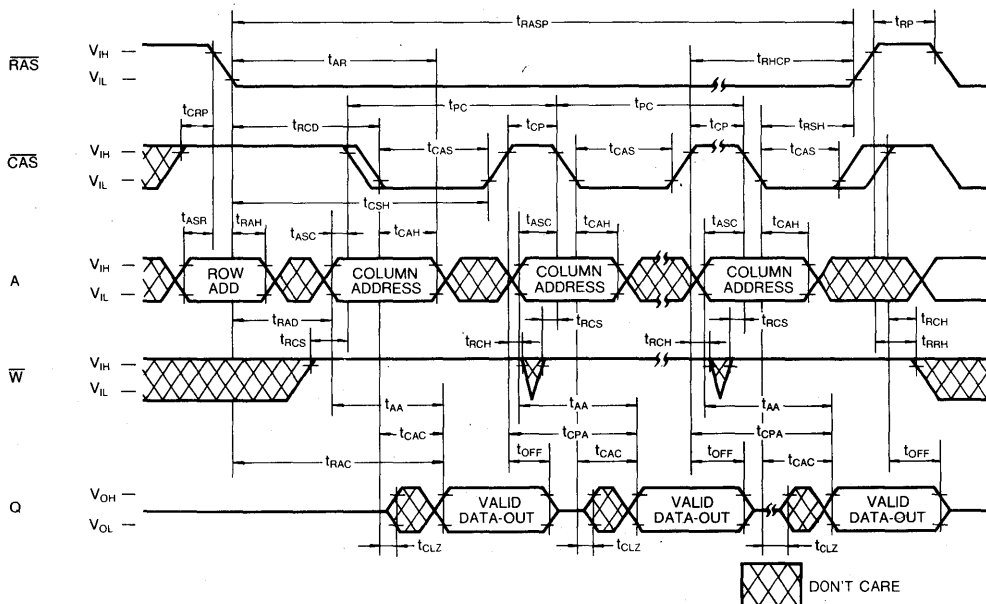
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE



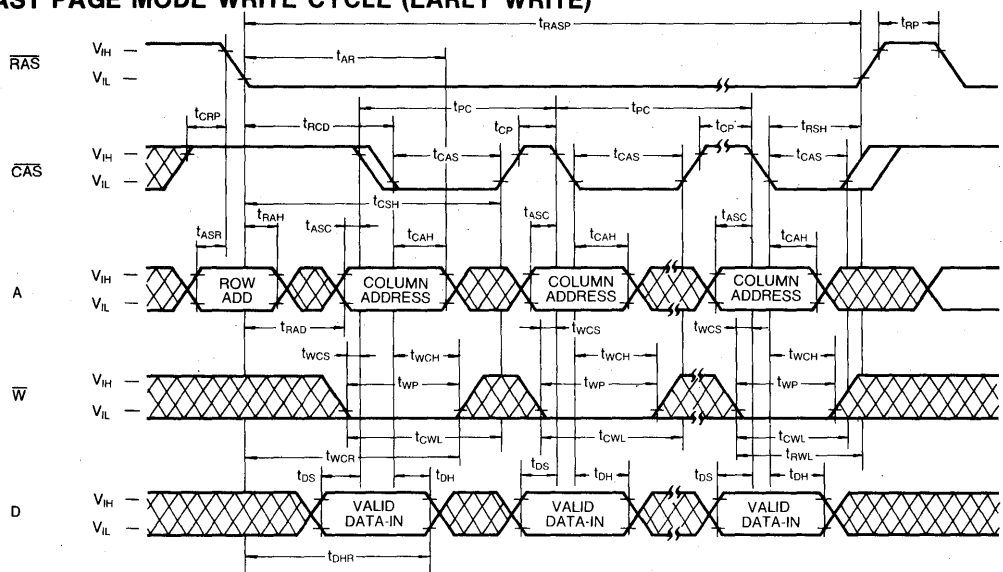
FAST PAGE MODE READ CYCLE



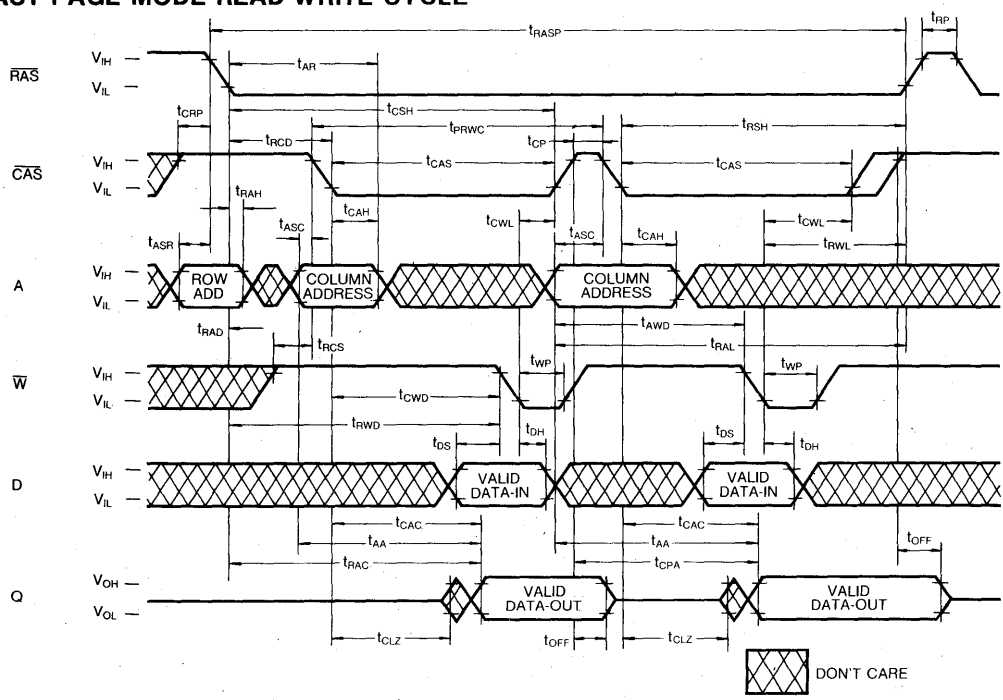
5

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



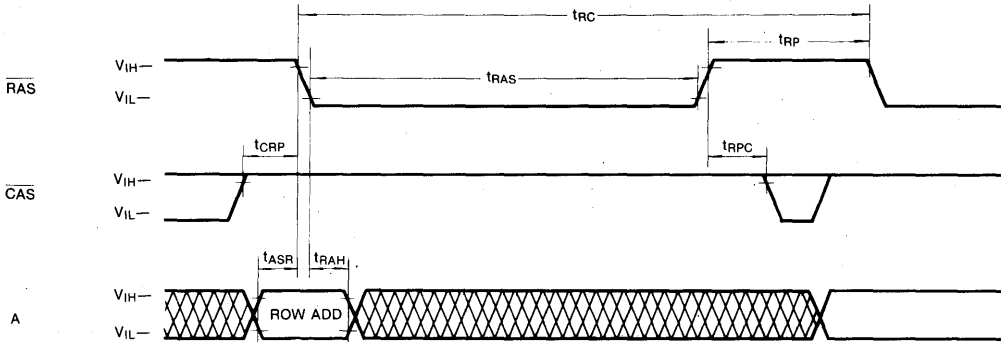
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

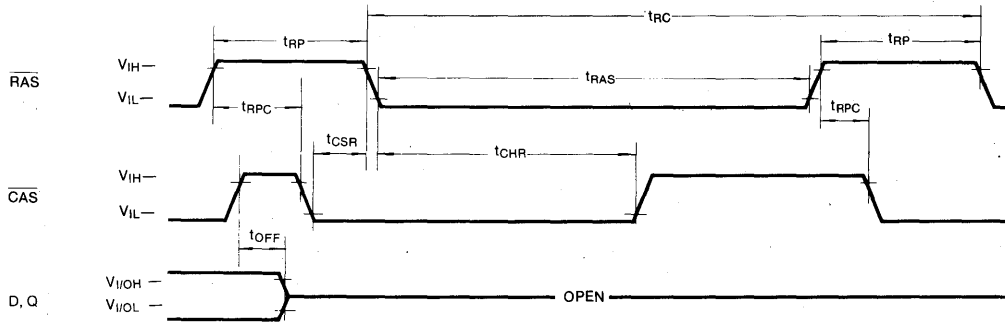
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , = Don't care



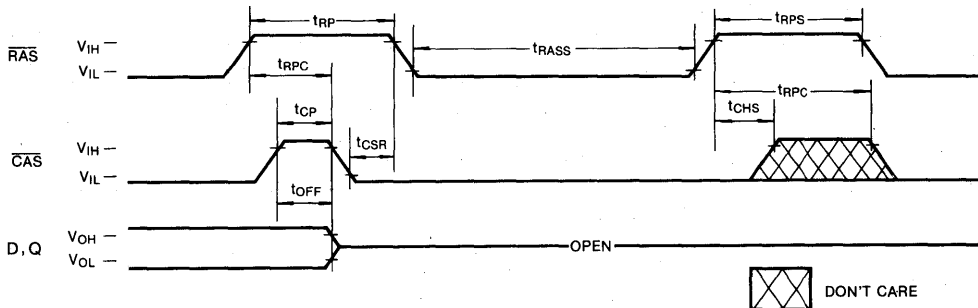
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\bar{W}=V_{IH}$, A=Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

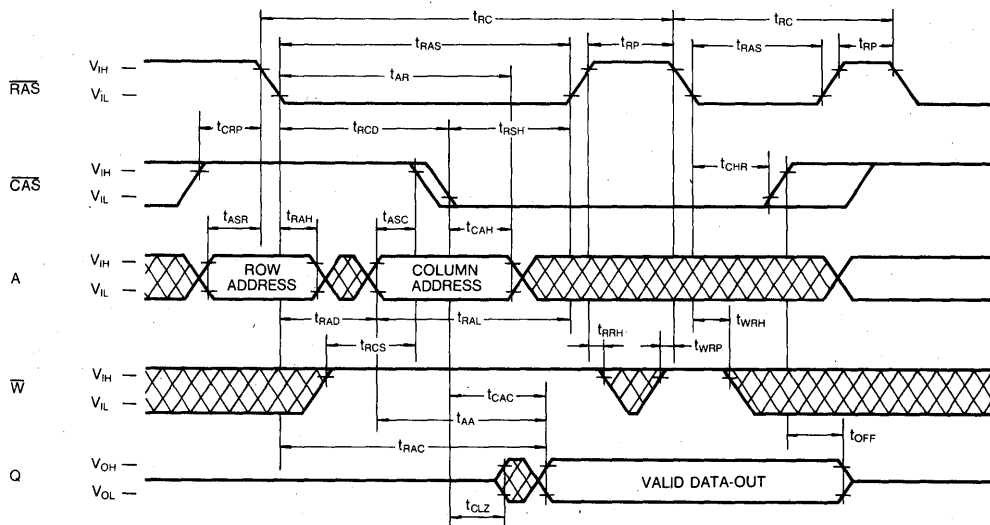
NOTE: \bar{W} , A=Don't Care



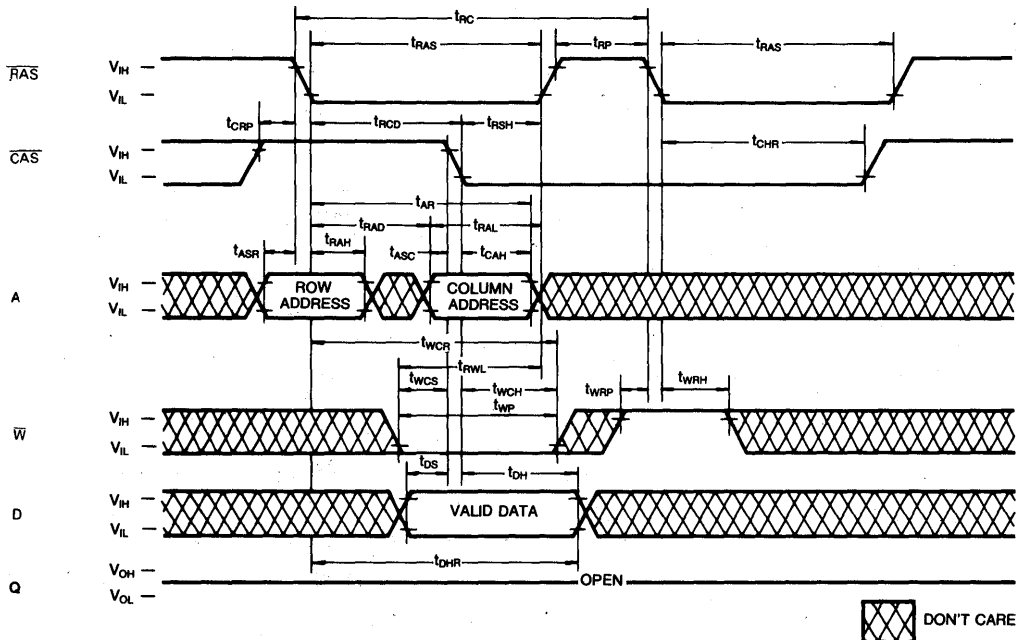
5

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



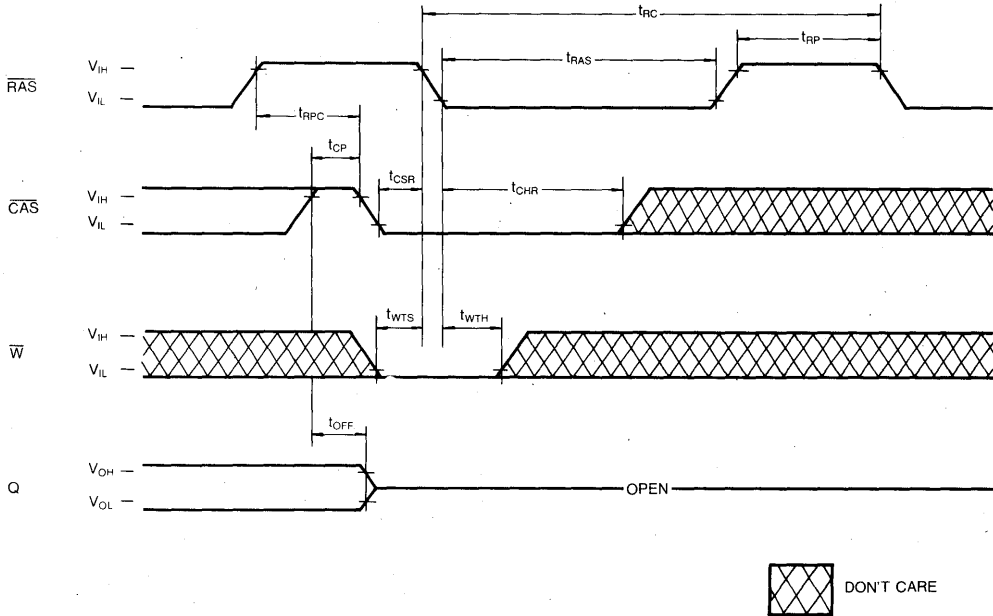
HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



TEST MODE DESCRIPTION

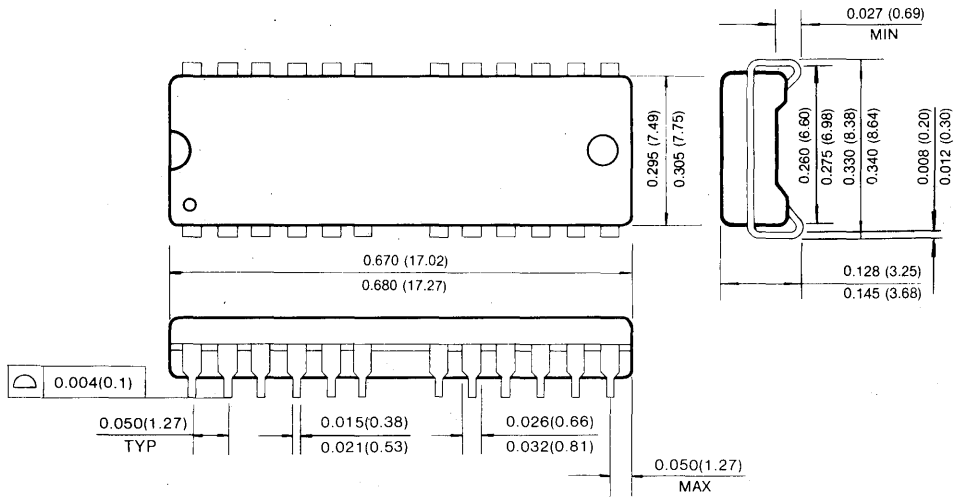
The KM41C16000A/AL/ALL/ASL is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A₀, A₁, A₁₀ and A₁₁ are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1". If they were not equal, the Q pin would indicate a "0". In

"Test Mode", the 16M DRAM can be tested as if it were a 1M × 1 DRAM. W, CAS-BEFORE-RAS Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "CAS-BEFORE-RAS REFRESH CYCLE" or "RAS-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

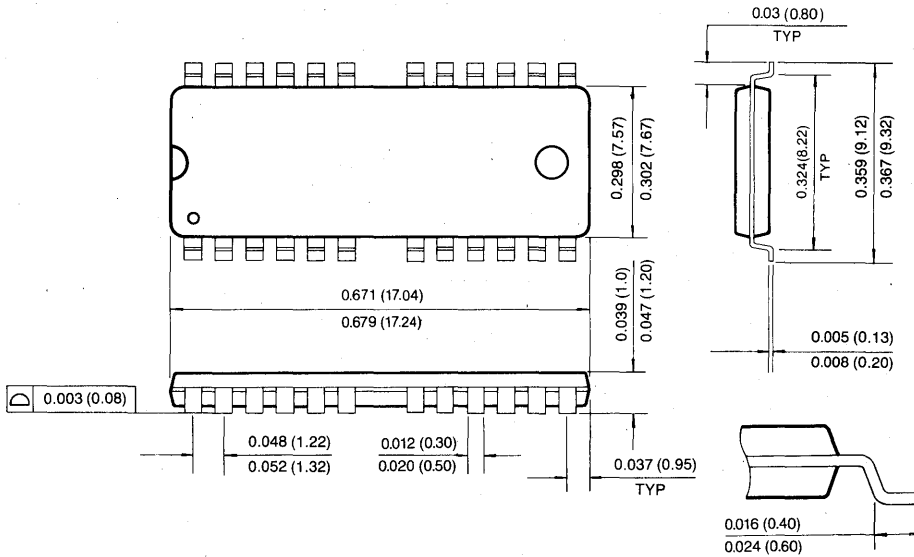
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

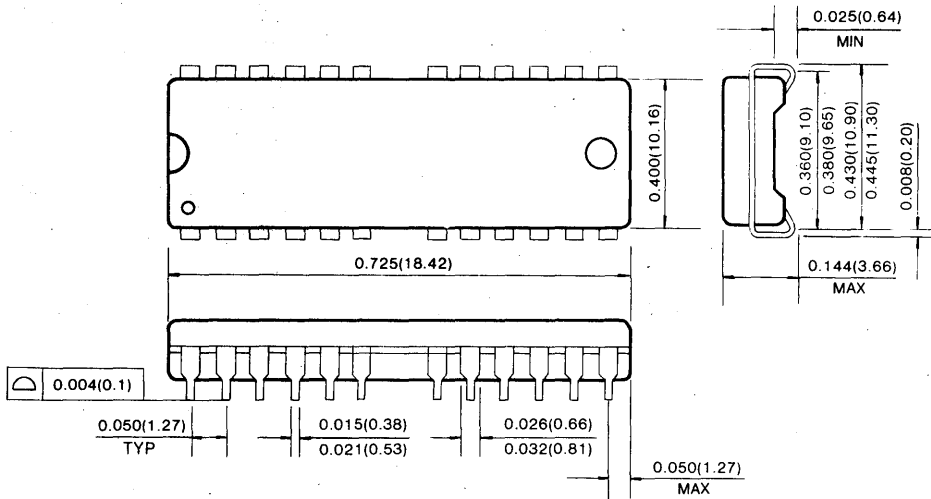


5

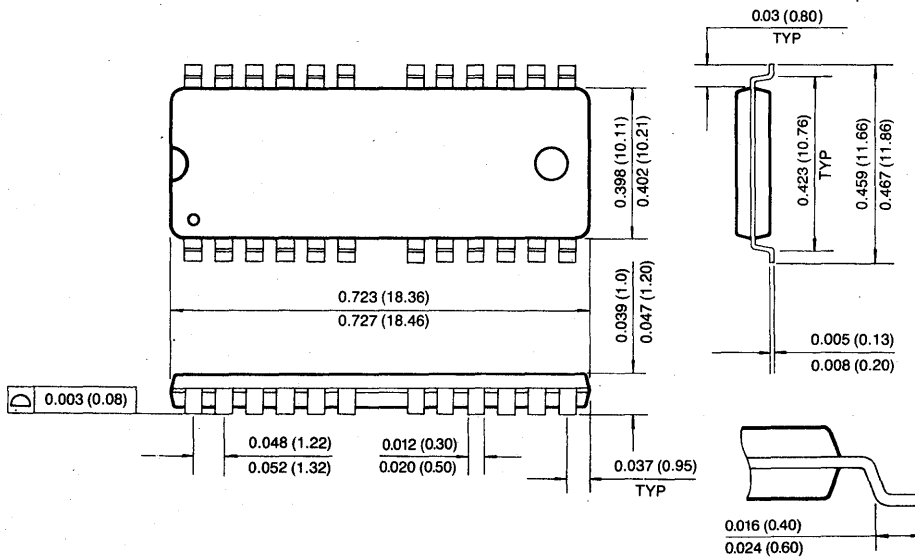
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



16M × 1 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM41C16002A/AL/ALL/ASL-5	50ns	13ns	90ns
KM41C16002A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41C16002A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41C16002A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Static Column Mode operation**
- **Self Refresh Operation (LL-ver, only)**
- **CS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V ± 10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

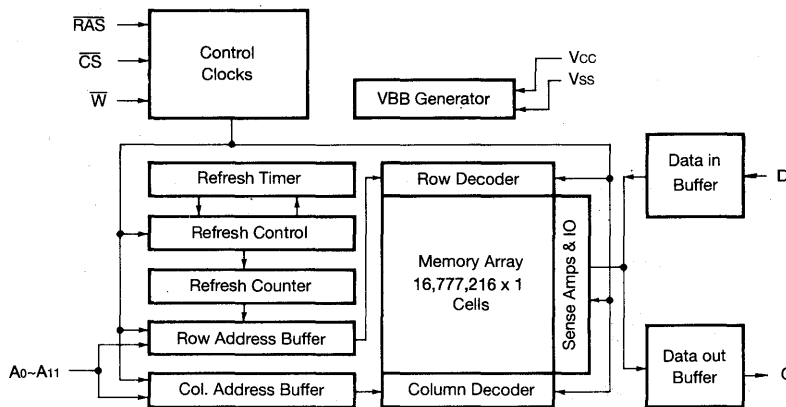
The Samsung KM41C16002A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM41C16002A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

CS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and output are fully TTL compatible.

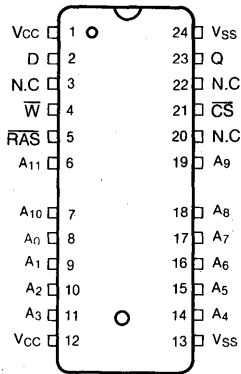
The KM41C16002A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



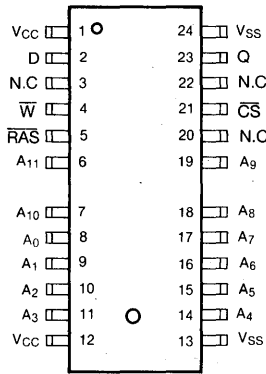
PIN CONFIGURATION (Top Views)

• KM41C16002 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



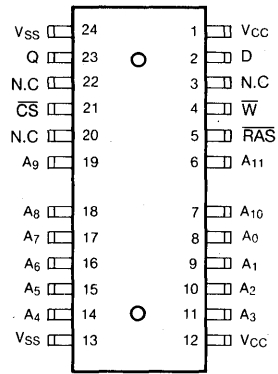
J : 400MIL
K : 300MIL

• KM41C16002 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM41C16002 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data out
RAS	Row Address Strobe
CS	Chip Select input
W	Read/Write Input
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CS Cycling @trc=min.)	KM41C16002A/AL/ALL/ASL-5	I _{CC1}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Standby Current (RAS=CS=W=V _{IH})	KM41C16002A	I _{CC2}	-	2	mA
	KM41C16002AL			1	mA
	KM41C16002ALL			1	mA
	KM41C16002ASL			1	mA
RAS-Only Refresh Current* (CS=V _{IH} , RAS Cycling @trc=min.)	KM41C16002A/AL/ALL/ASL-5	I _{CC3}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* (RAS=V _{IL} , CS, Address Cycling @tpc=min.)	KM41C16002A/AL/ALL/ASL-5	I _{CC4}	-	80	mA
	KM41C16002A/AL/ALL/ASL-6			70	mA
	KM41C16002A/AL/ALL/ASL-7			60	mA
	KM41C16002A/AL/ALL/ASL-8			50	mA
Standby Current (RAS=CS=W=V _{CC} -0.2V)	KM41C16002A	I _{CC5}	-	1	mA
	KM41C16002AL			300	μA
	KM41C16002ALL			200	μA
	KM41C16002ASL			200	μA
CS-Before-RAS Refresh Current* (RAS and CS Cycling @trc=min.)	KM41C16002A/AL/ALL/ASL-5	I _{CC6}	-	90	mA
	KM41C16002A/AL/ALL/ASL-6			80	mA
	KM41C16002A/AL/ALL/ASL-7			70	mA
	KM41C16002A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CS=CS-Before-RAS Cycling or 0.2V D=Don't Care trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), tRAS =tRAS min-300ns	KM41C16002AL	I _{CC7}	-	450	μA
	KM41C16002ASL			350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CS=0.2V W=A0-A11=Vcc-0.2V or 0.2V Vcc-0.2V, 0.2V or Open	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)	IoL	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IoL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one Static Column cycle.

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	CIN1	-	7	pF
Input Capacitance (A0~A11)	CIN2	-	5	pF
Input Capacitance (RAS, CS, W)	CIN3	-	7	pF
Input Capacitance (Q)	COU	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	115		135		155		175		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CS hold time	trSH	50		60		70		80		ns	
CS pulse width	trCS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CS to RAS precharge time	trCP	5		5		5		5		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CS}}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		50		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	tCWD	15		15		20		20		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	50		60		70		80		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	25		30		35		40		ns	8
$\overline{\text{CS}}$ set-up time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CS}}$ hold time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CS}}$ precharge time ($\overline{\text{C}}$ -B-R counter test cycle)	tCPT	20		20		30		30		ns	
Static column mode cycle time	tSC	30		35		40		45		ns	3
Static column mode read-write cycle time	tSRWC	50		60		70		80		ns	
Access time from last write	tALW		50		55		65		75	ns	3, 12
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{\text{W}}$	tOW		35		40		45		55	ns	
$\overline{\text{RAS}}$ pulse width (Static column mode)	tRASC	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{CS}}$ pulse width (Static column mode)	tCSC	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{\text{CS}}$ precharge time (Static column mode)	tCP	10		10		10		10		ns	
Column address hold time referenced to $\overline{\text{RAS}}$ rising	tAH	5		5		5		5		ns	
Last write to column address delay time	tLWAD	20	25	20	25	25	30	25	35	ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Last write to column address hold time	tAHLW	50		55		65		75		ns	
Write command inactive time	tWI	10		10		10		10		ns	
\overline{RAS} hold time referenced to \overline{OE}	tROH	13		15		20		20		ns	
Write address hold time referenced to \overline{RAS}	tAWR	40		45		55		60		ns	6
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	tWRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	tWRH	10		10		10		10		ns	
\overline{RAS} pulse width (\overline{C} - \overline{B} - \overline{R} self refresh)	tRASS	100		100		100		100		μ s	15
\overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} self refresh)	tRPS	90		110		130		150		ns	15
\overline{CS} hold time (\overline{C} - \overline{B} - \overline{R} self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

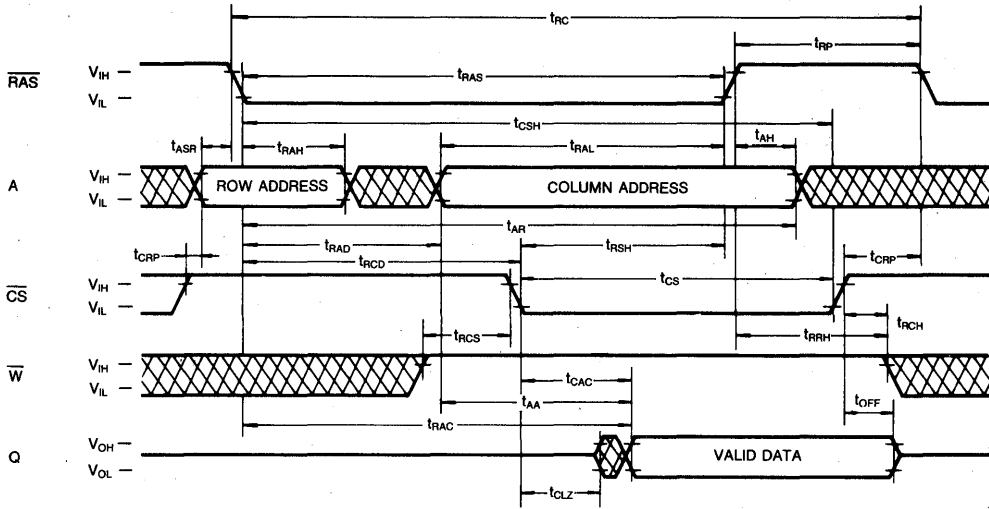
(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	140		160		190		210		ns	
Access time from \overline{RAS}	tRAC		55		65		75		85	ns	3,4,11
Access time from \overline{CS}	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\overline{RAS} pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\overline{CS} pulse width	tCS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
\overline{RAS} hold time	tRSH	20		20		25		25		ns	
\overline{CS} hold time	tCSH	55		65		75		85		ns	
Column address to \overline{RAS} lead time	tRAL	30		35		40		45		ns	
\overline{CS} to \overline{W} delay time	tCWD	45		45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	80		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	55		60		70		75		ns	8
Static column mode cycle time	tSC	35		40		45		50		ns	
Static column mode read-write cycle time	tSRWC	85		90		105		110		ns	
\overline{RAS} pulse width (Static column mode)	tRASC	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	tALW		50		60		70		80	ns	3,12

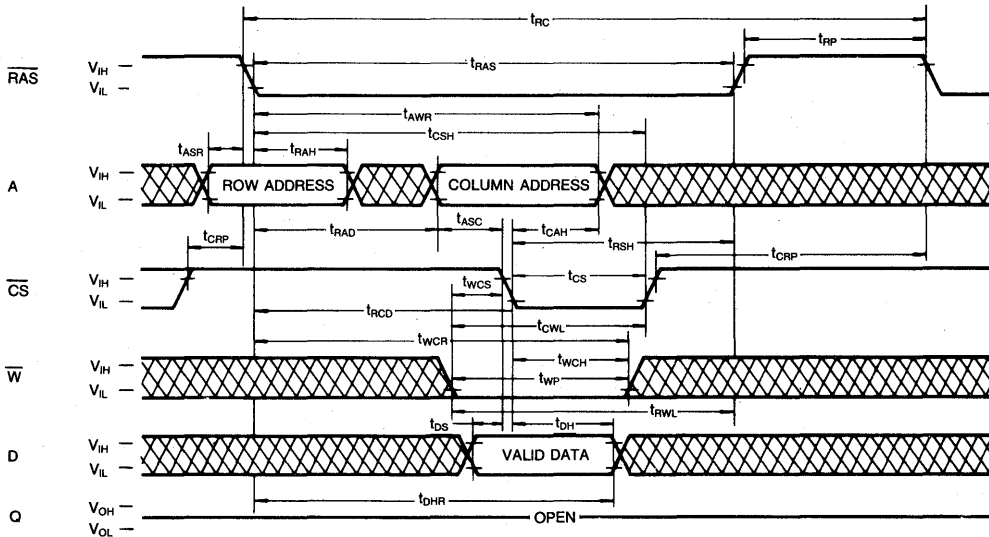
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

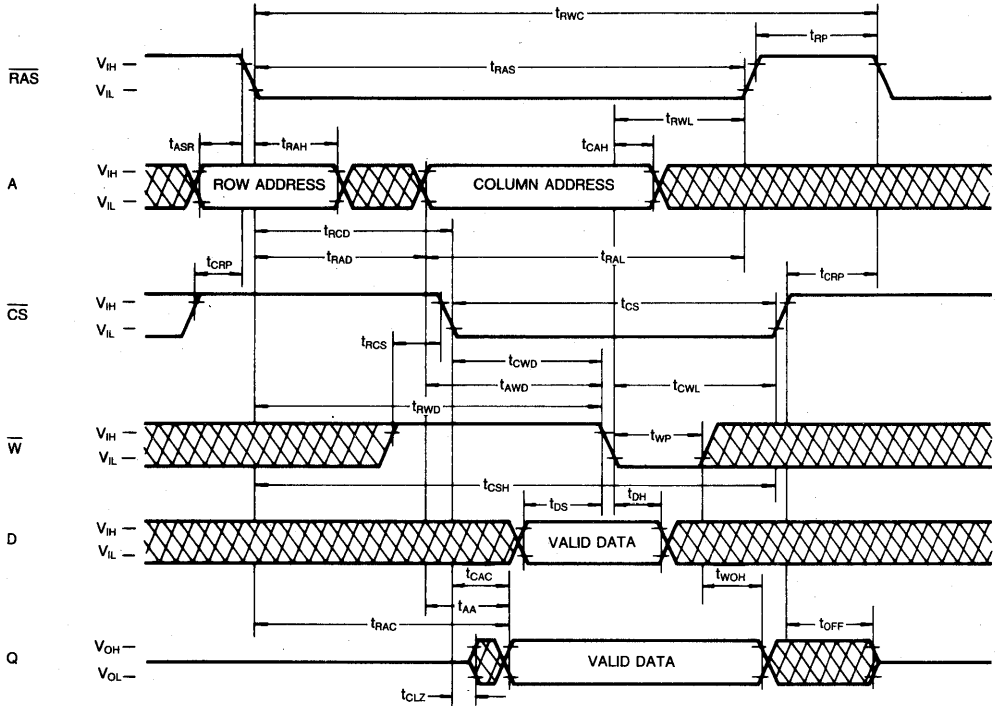
TIMING DIAGRAMS
READ CYCLE



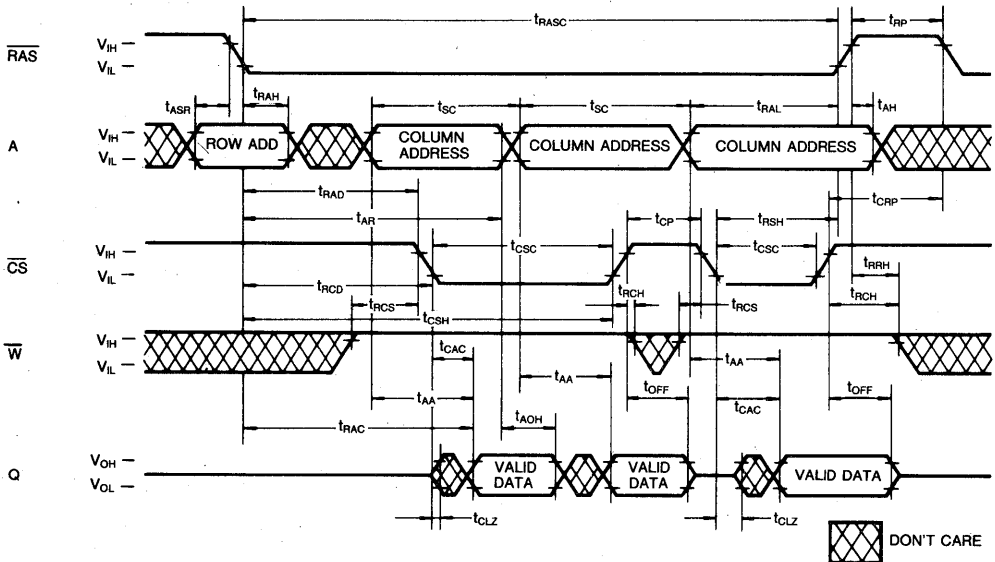
WRITE CYCLE (EARLY WRITE)



TIMING DIAGRAMS (Continued)
READ-WRITE/READ-MODIFY-WRITE CYCLE



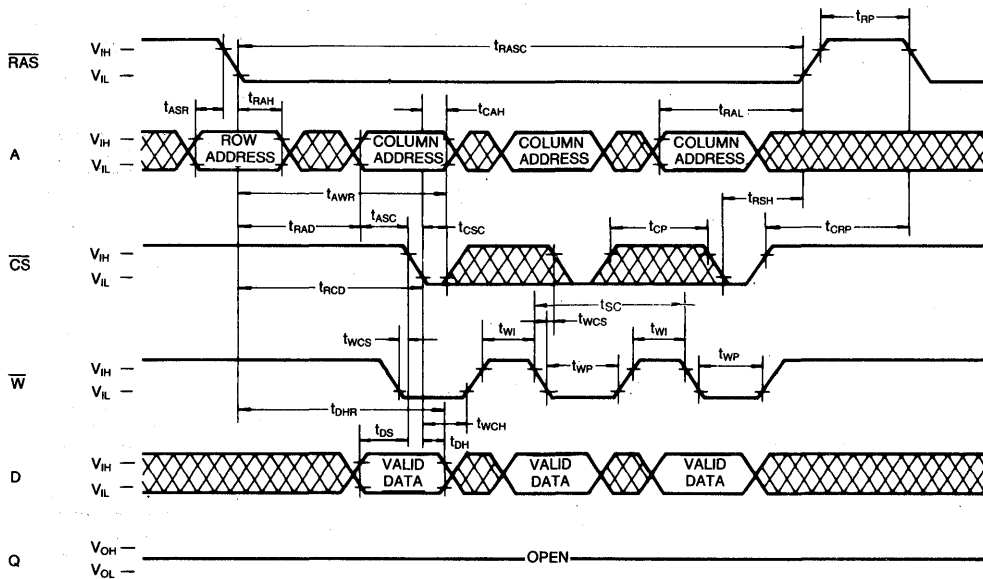
STATIC COLUMN MODE READ CYCLE



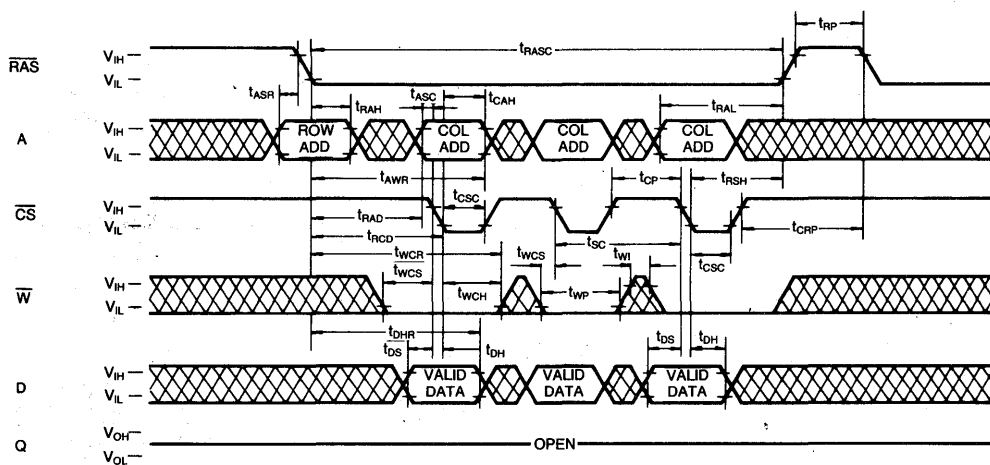
5

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE (\overline{W} CONTROLLED EARLY WRITE)



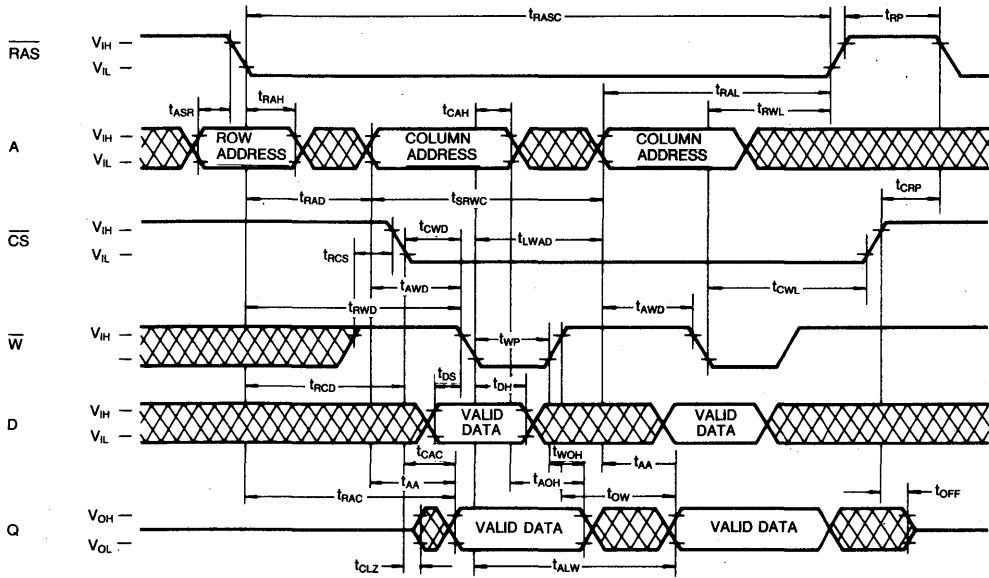
STATIC COLUMN MODE WRITE CYCLE (\overline{CS} CONTROLLED EARLY WRITE)



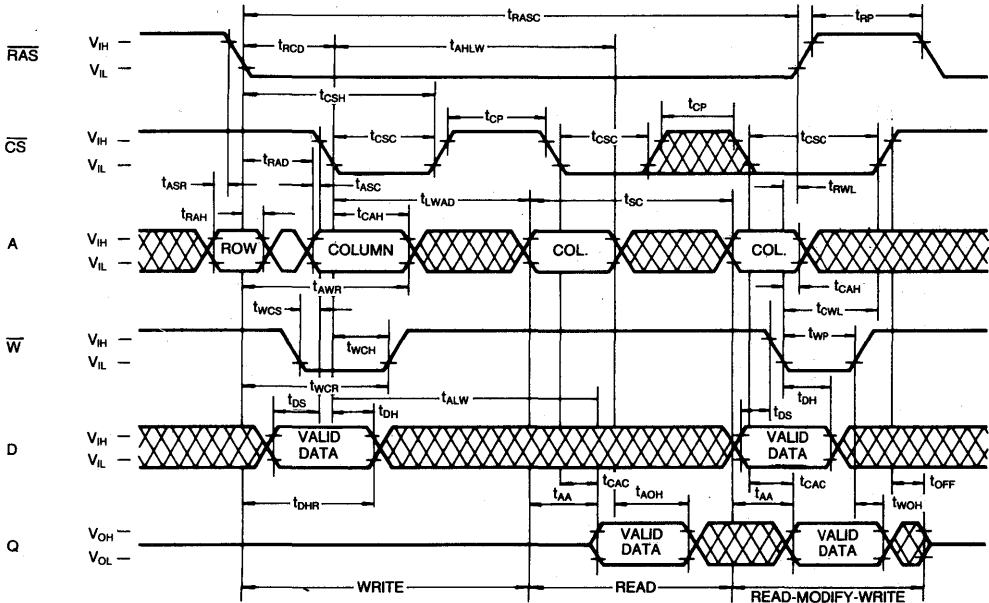
 DON'T CARE

TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-WRITE CYCLE



STATIC COLUMN MODE MIXED CYCLE

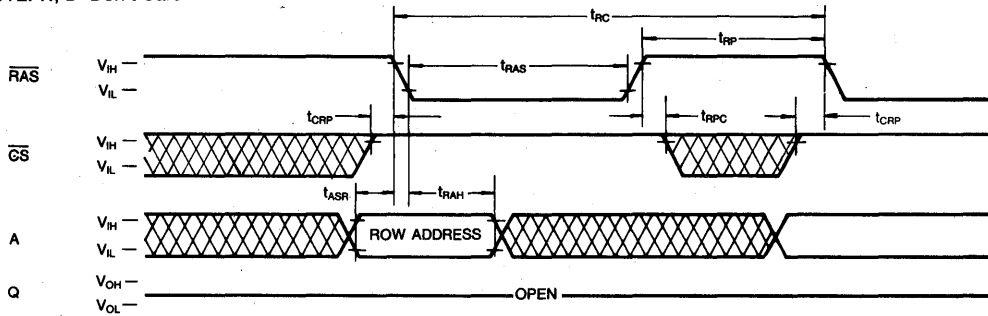


 DON'T CARE

TIMING DIAGRAMS (Continued)

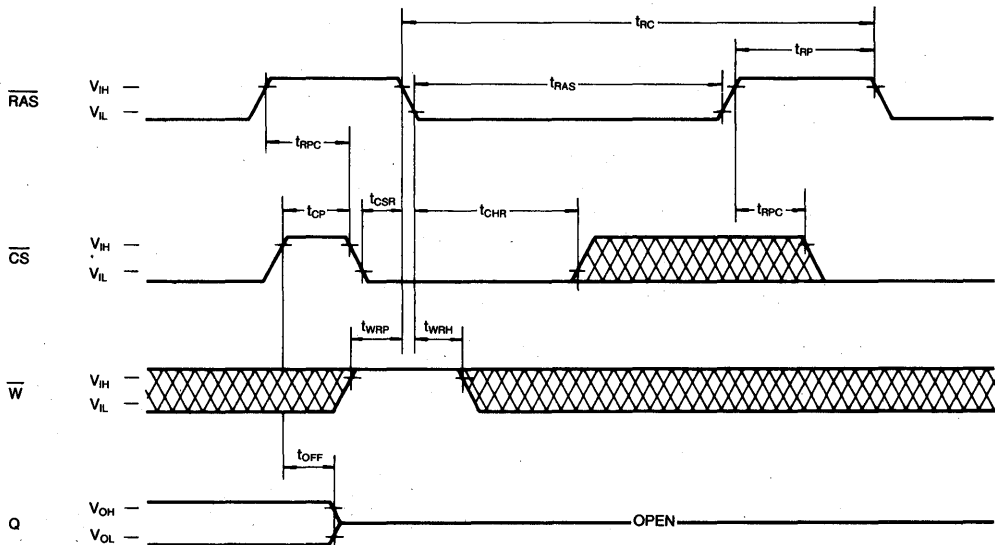
RAS-ONLY REFRESH CYCLE

NOTE: \bar{W} , D=Don't Care



\bar{CS} -BEFORE- \bar{RAS} REFRESH CYCLE

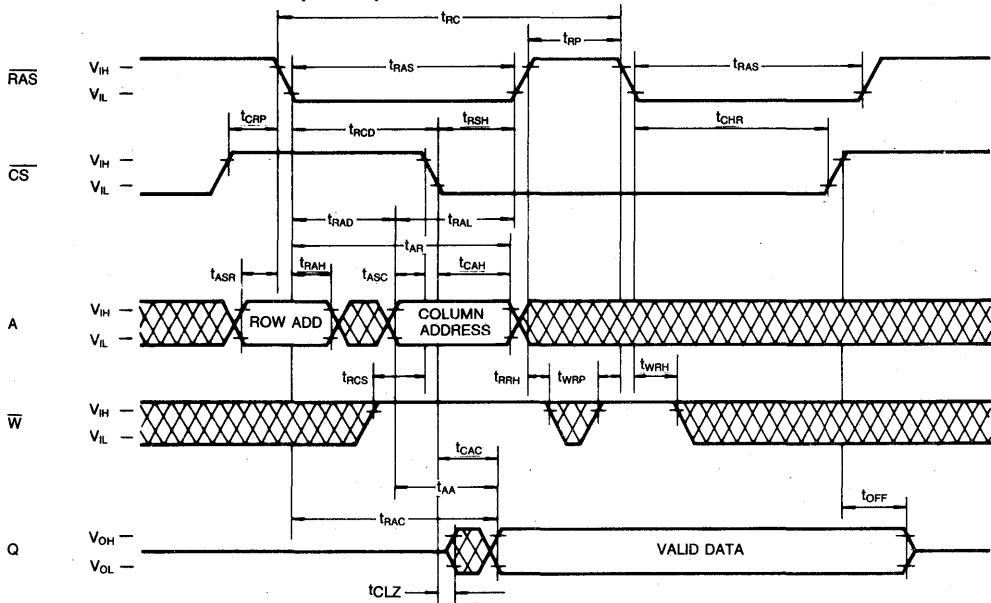
NOTE: Address=Don't Care



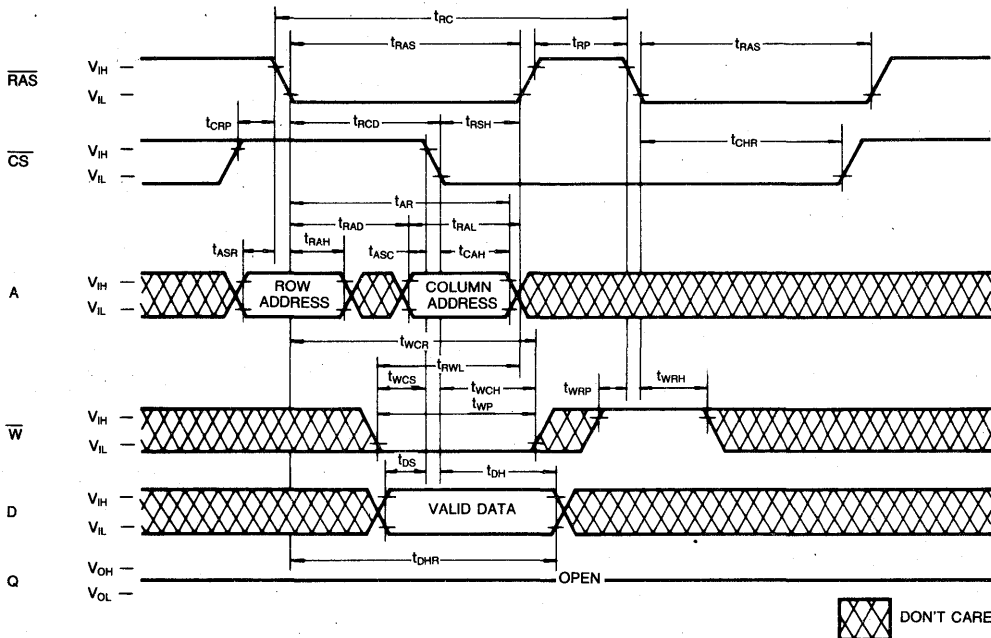
 DONT CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

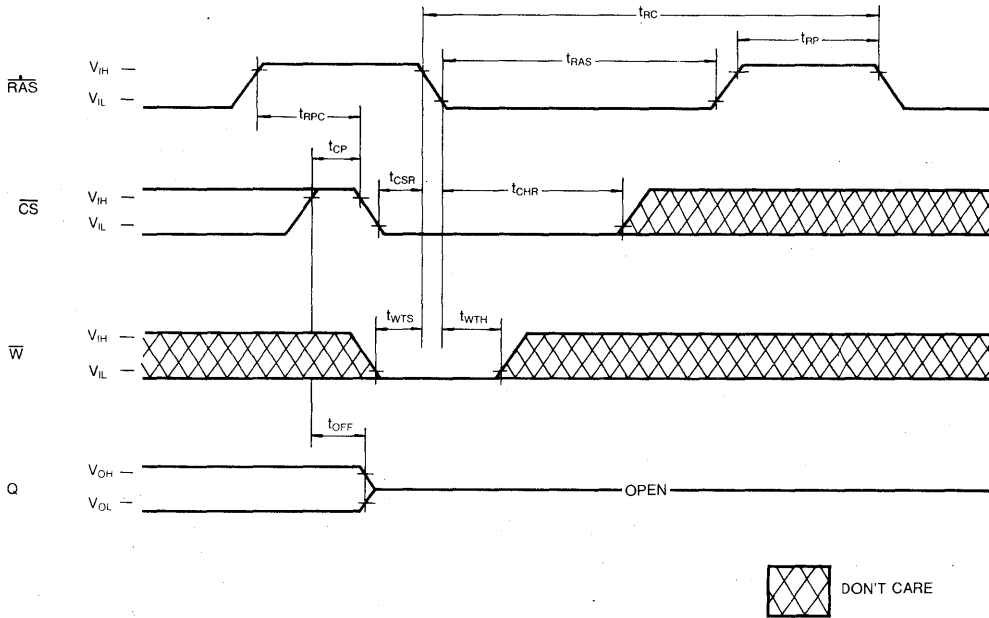


 DON'T CARE

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



5

TEST MODE DESCRIPTION

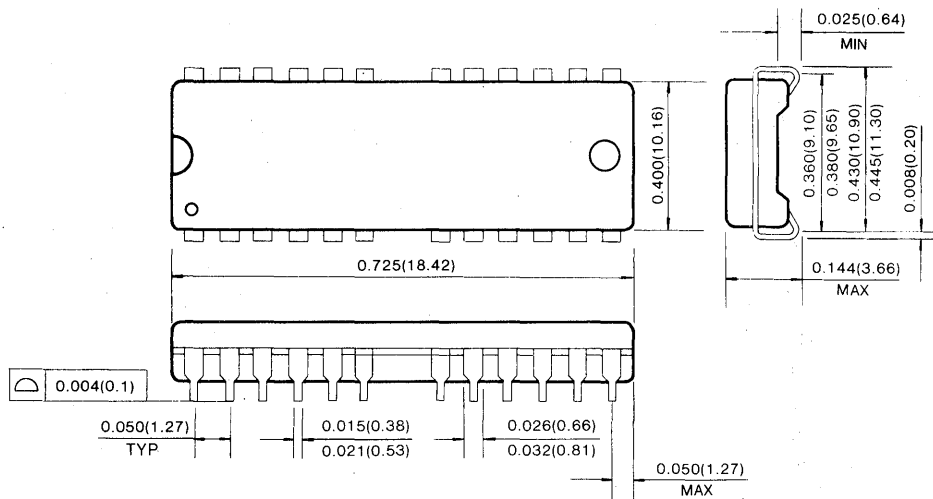
The KM41C16002 is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1,048,576 words by 16 bits. In "Test mode," data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 , A_1 , A_{10} and A_{11} are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1."

If they were not equal, the Q pin would indicate a "0." In "Test Mode," the 16M DRAM can be tested as if it were a 1M x 1 DRAM. \overline{W} , \overline{CS} -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode." And " \overline{CS} -BEFORE- \overline{RAS} REFRESH CYCLE" or " \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode." The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

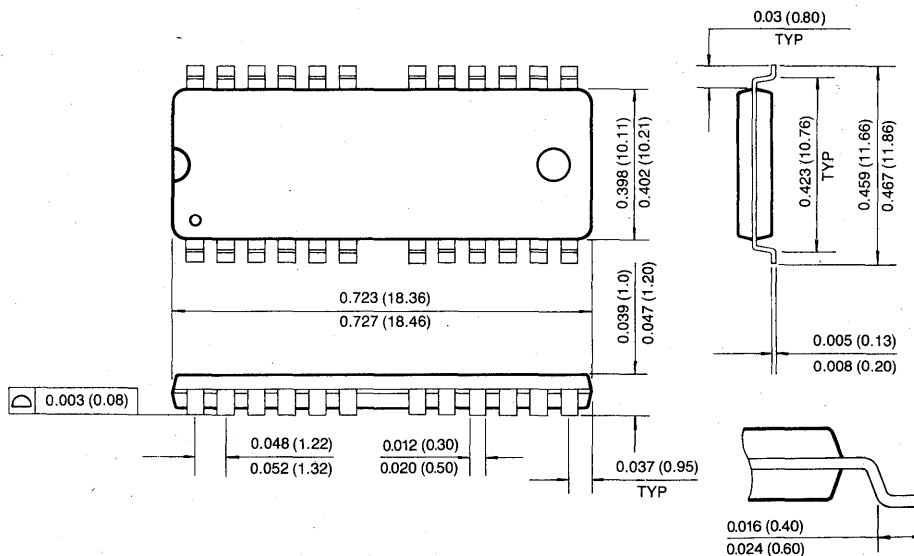
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE
(Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM44C4000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4000A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

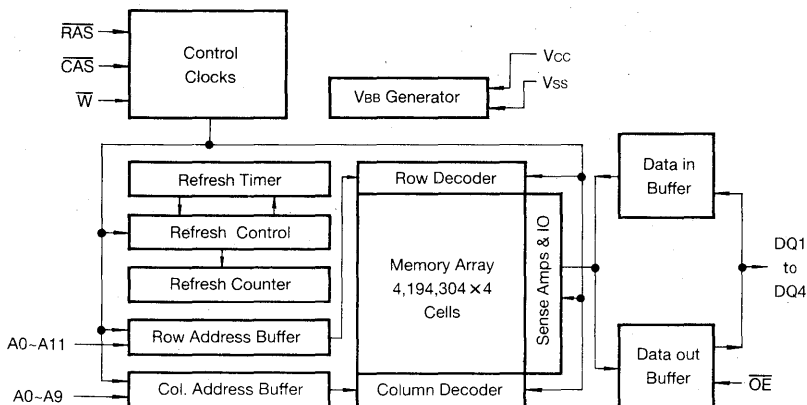
The Samsung KM44C4000A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

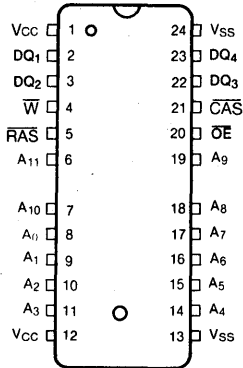
The KM44C4000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



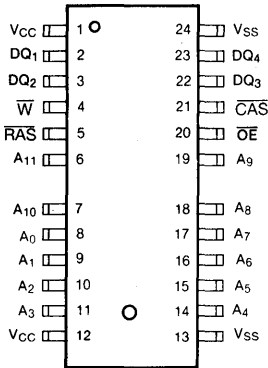
PIN CONFIGURATION (Top Views)

• KM44C4000 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



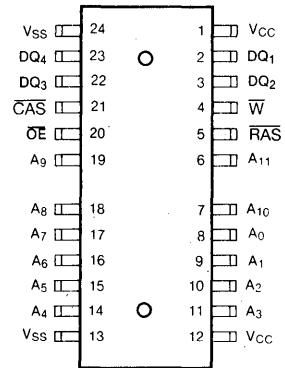
J : 400MIL
K : 300MIL

• KM44C4000 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4000 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44C4000A/AL/ALL/ASL-5 KM44C4000A/AL/ALL/ASL-6 KM44C4000A/AL/ALL/ASL-7 KM44C4000A/AL/ALL/ASL-8	I _{CC1}	90	mA
			80	mA
			70	mA
			60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	KM44C4000A KM44C4000AL KM44C4000ALL KM44C4000ASL	I _{CC2}	2	mA
			1	mA
			1	mA
			1	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} Cycling @trc=min.)	KM44C4000A/AL/ALL/ASL-5 KM44C4000A/AL/ALL/ASL-6 KM44C4000A/AL/ALL/ASL-7 KM44C4000A/AL/ALL/ASL-8	I _{CC3}	90	mA
			80	mA
			70	mA
			60	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @tpc=min.)	KM44C4000A/AL/ALL/ASL-5 KM44C4000A/AL/ALL/ASL-6 KM44C4000A/AL/ALL/ASL-7 KM44C4000A/AL/ALL/ASL-8	I _{CC4}	80	mA
			70	mA
			60	mA
			50	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)	KM44C4000A KM44C4000AL KM44C4000ALL KM44C4000ASL	I _{CC5}	1	mA
			300	μA
			200	μA
			200	μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44C4000A/AL/ALL/ASL-5 KM44C4000A/AL/ALL/ASL-6 KM44C4000A/AL/ALL/ASL-7 KM44C4000A/AL/ALL/ASL-8	I _{CC6}	90	mA
			80	mA
			70	mA
			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{CAS}=\overline{CAS}$ -Before- \overline{RAS} Cycling or 0.2V \overline{DIN} =Don't Care TRC=31.25μS(L-Ver.) 62.5μS(SL-Ver.), TRAS ≤ min~300ns	KM44C4000AL KM44C4000ASL	I _{CC7}	450	μA
			350	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	lccs	-	300	μA
Input Leakage Current (Any input 0 ≤ Vin ≤ Vcc+0.5V, all other pins not under test=0 volts.)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1-DQ4)	CDO	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 0.5V, See notes 1,2)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CAS hold time	tCSH	50		60		70		80		ns	
CAS pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	trCP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	TRAH	10		10		10		10		ns	
Column address set-up time	TASC	0		0		0		0		ns	
Column address hold time	TCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	TAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	TRAL	25		30		35		40		ns	
Read command set-up time	TRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	TRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	TRRH	0		0		0		0		ns	
Write command hold time	TWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	TWCR	40		45		55		60		ns	6
Write command pulse width	TWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	TRWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	TCWL	13		15		20		20		ns	
Data set-up time	tds	0		0		0		0		ns	10
Data hold time	tdh	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tdhr	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	twcs	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcwd	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trwd	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tawd	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tcsr	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tchr	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trpc	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tcpt	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcpa		30		35		40		45	ns	3
Fast Page mode cycle time	tpc	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tprwc	76		85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tcp	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	trasp	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trhcp	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	toea		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	toed	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	toez	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	toeh	13		15		20		20		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
W to RAS precharge time (\bar{C} -B- \bar{R} refresh)	tWRP	10		10		10		10		ns	
W to RAS hold time (\bar{C} -B- \bar{R} refresh)	tWRH	10		10		10		10		ns	
RAS pulse width (\bar{C} -B- \bar{R} self refresh)	tRASS	100		100		100		100		μ s	15
RAS precharge time (\bar{C} -B- \bar{R} self refresh)	tRPS	90		110		130		150		ns	15
CAS hold time (\bar{C} -B- \bar{R} self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

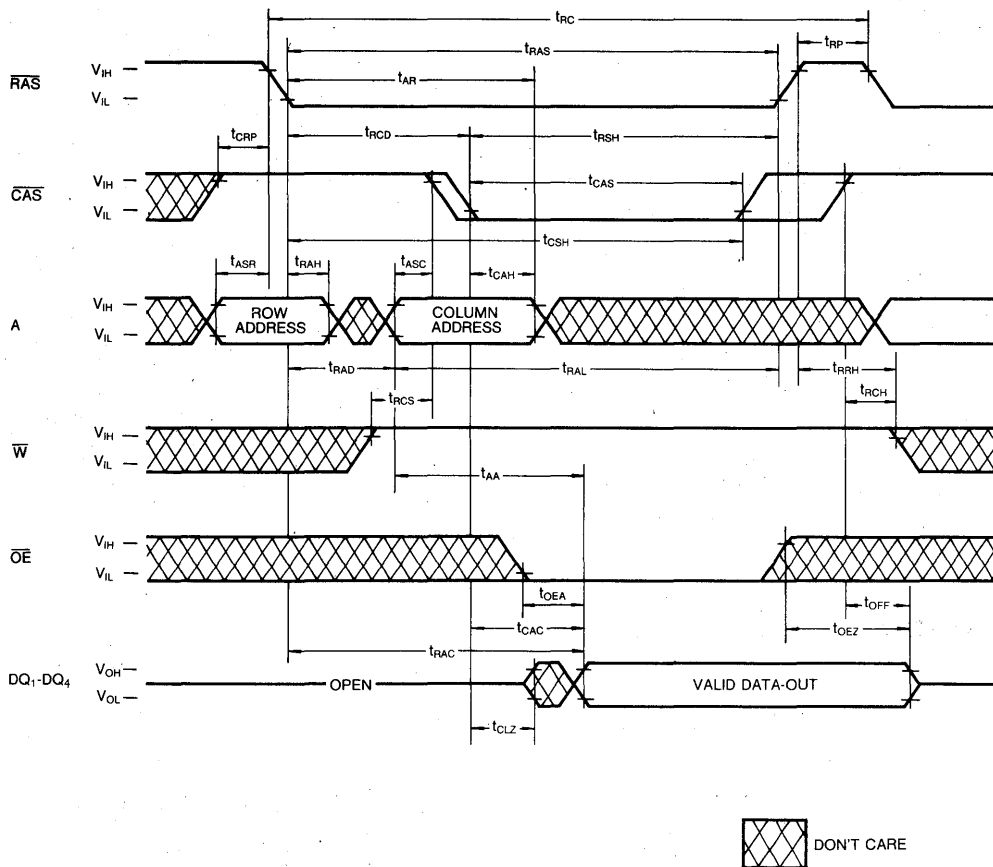
(Note.12)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWCM	138		160		190		210		ns	
Access time from RAS	tRAC		55		65		75		85	ns	3,4,11
Access time from CAS	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
RAS pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
CAS pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	tRSH	18		20		25		25		ns	
CAS hold time	tCSH	55		65		75		85		ns	
Column address to RAS lead time	tRAL	30		35		40		45		ns	
CAS to W delay time	tCWD	41		45		55		55		ns	8
RAS to W delay time	tRWD	78		90		105		115		ns	8
Column address to W delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
RAS pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tCPA		35		40		45		50	ns	3
OE access time	tOEA		18		20		25		25	ns	
OE to data delay	tOED	18		20		25		25		ns	
OE command hold time	tOEH	18		20		25		25		ns	

NOTES

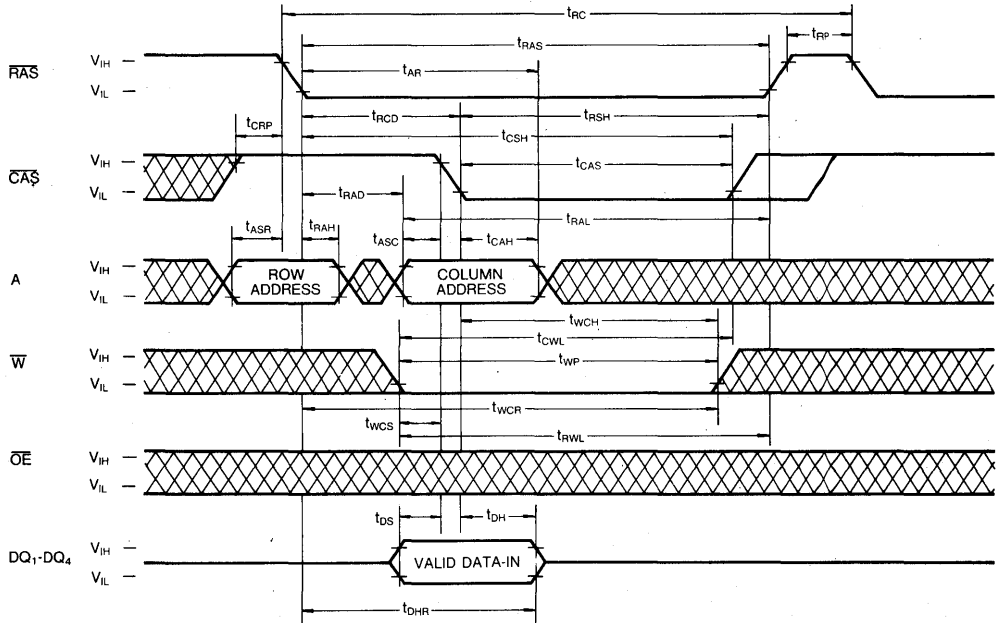
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS
READ CYCLE

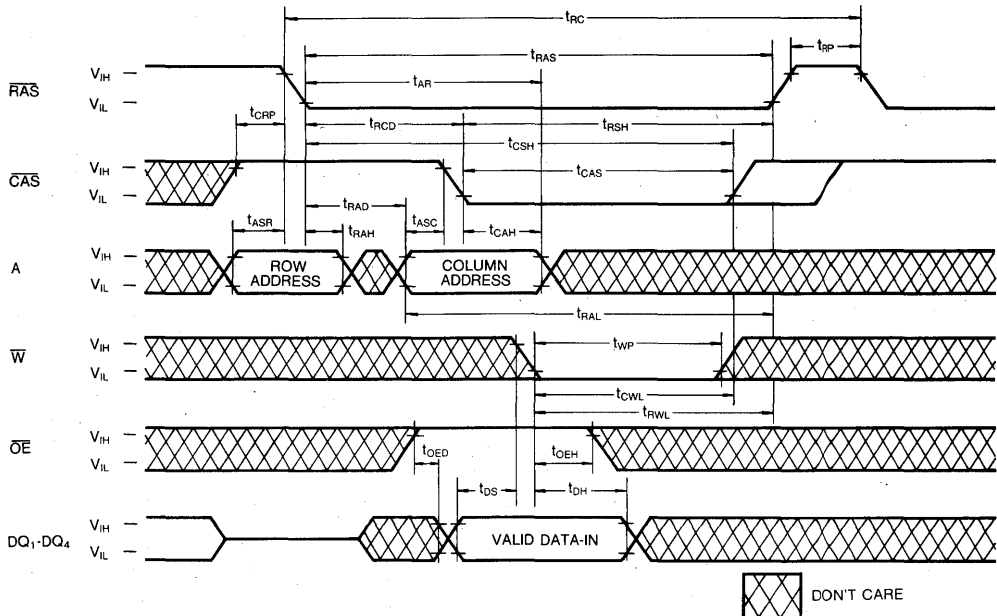


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

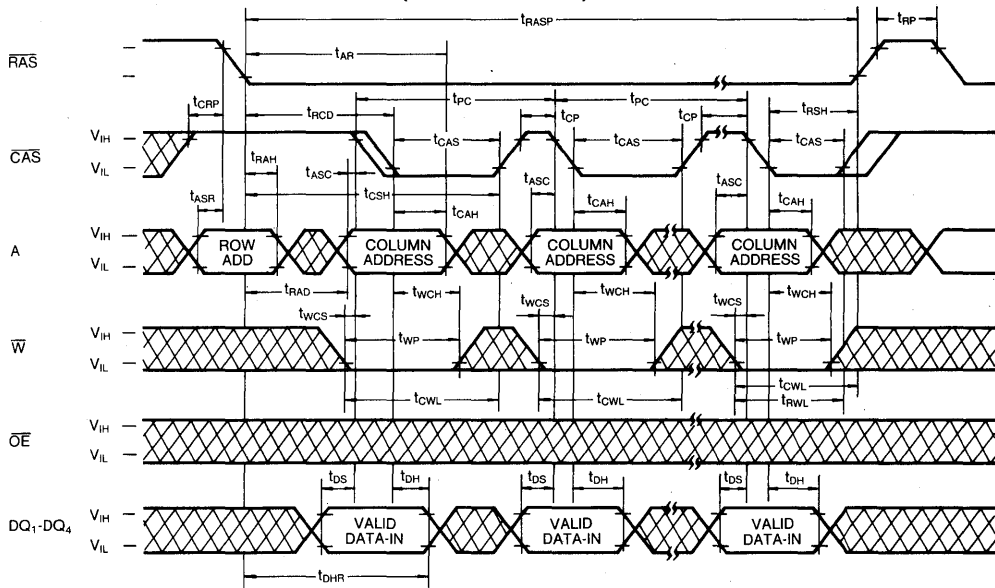


WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

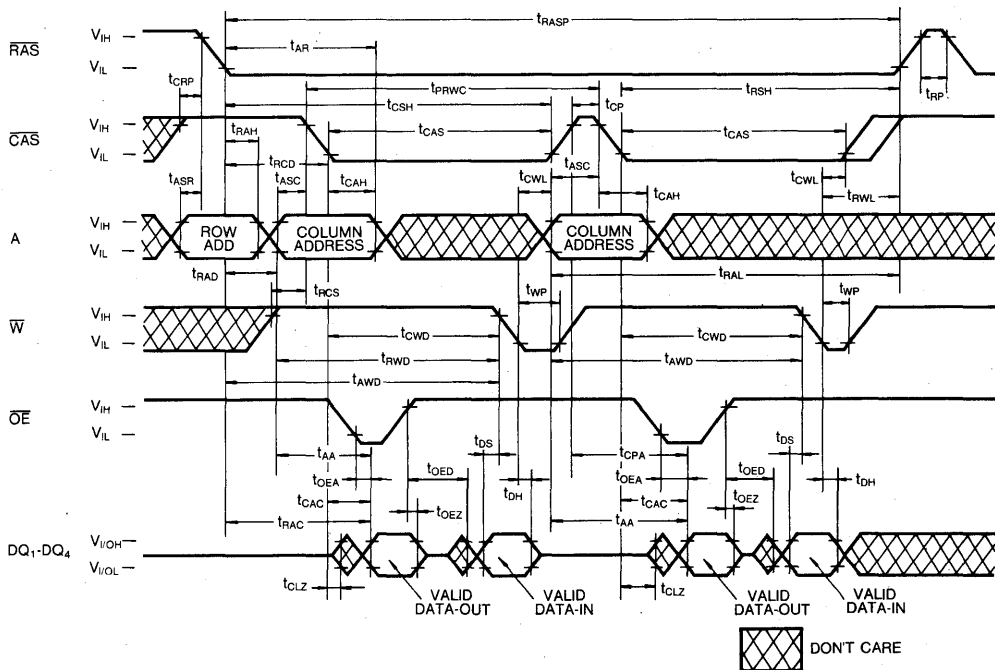


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

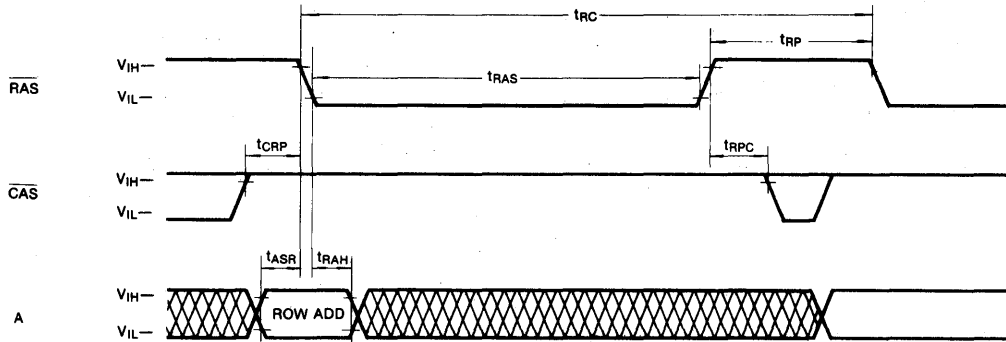


5

TIMING DIAGRAMS (Continued)

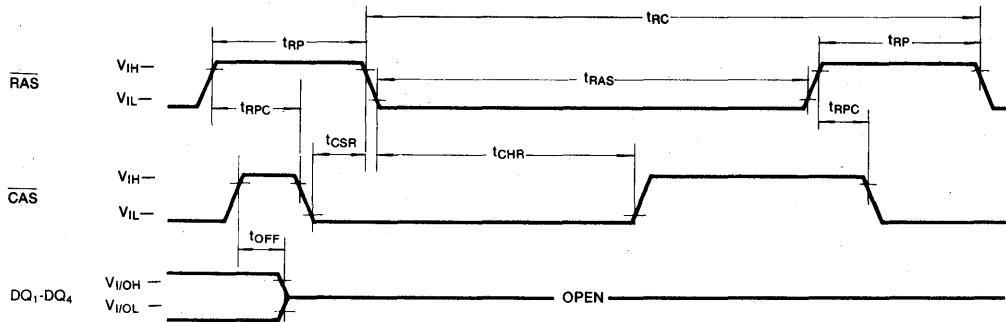
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



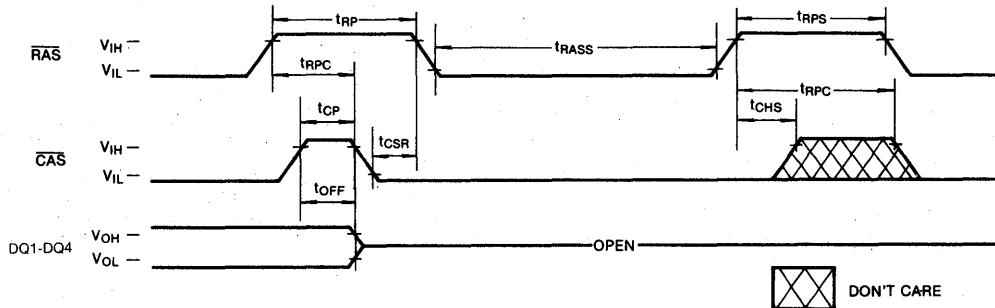
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\bar{W}=V_{IH}$, \bar{OE} , A=Don't Care



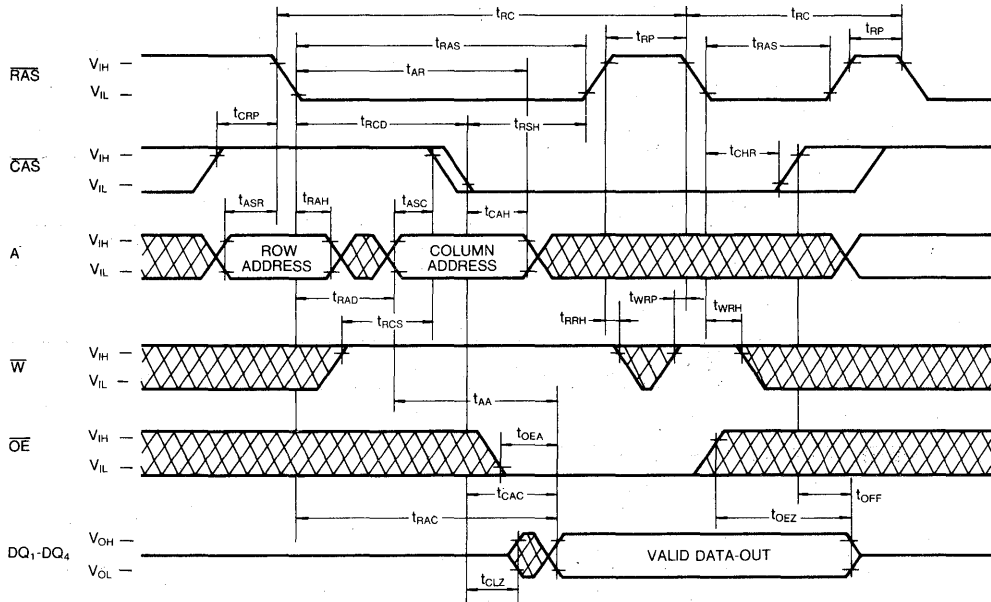
CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

NOTE: \bar{W} , \bar{OE} , A=Don't Care

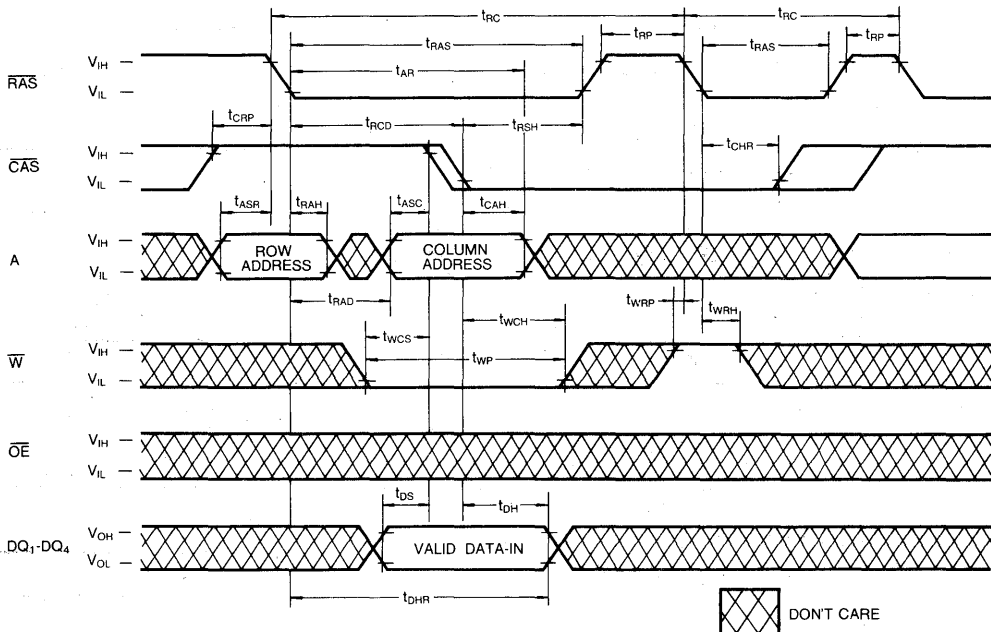


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



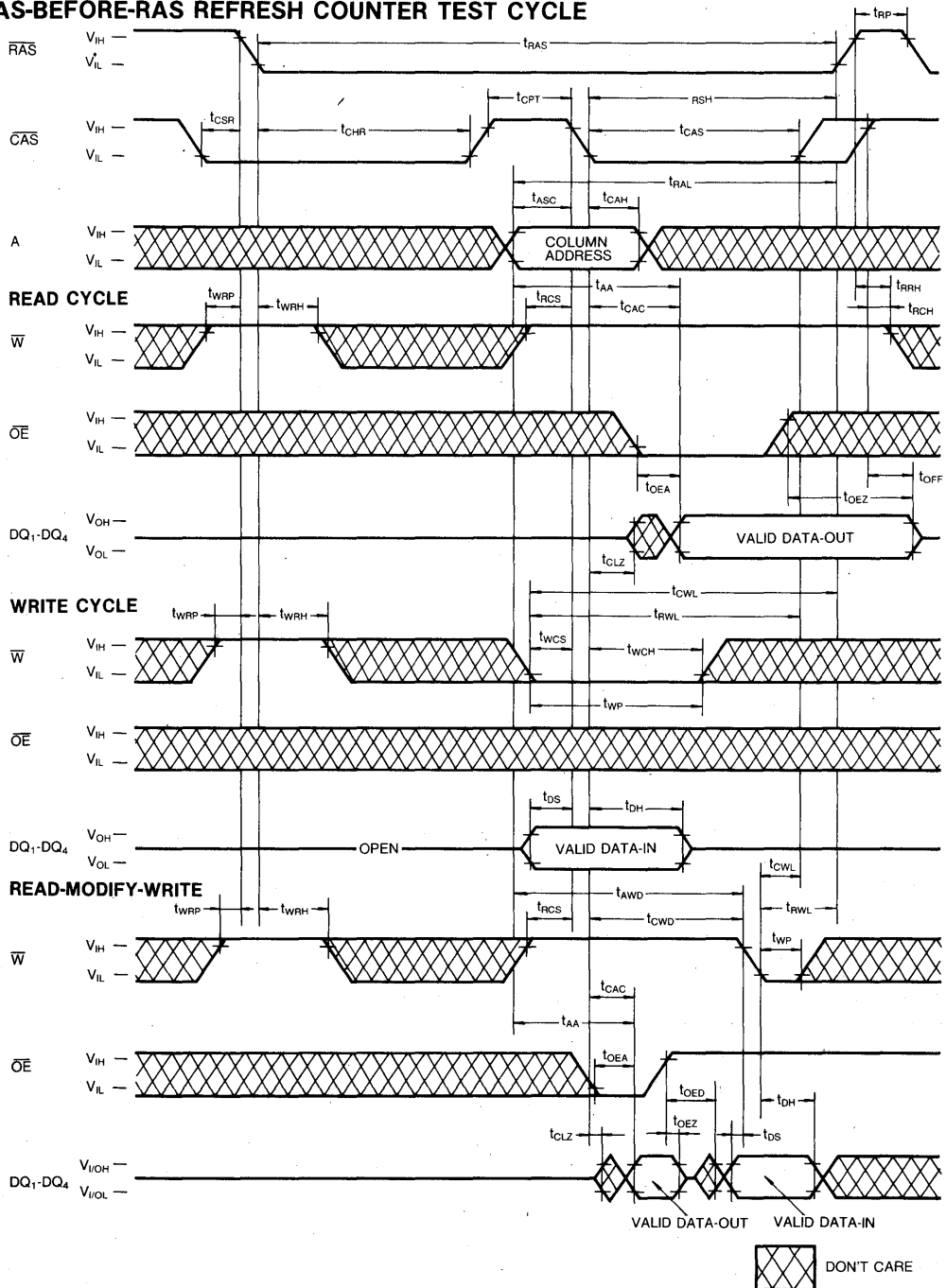
HIDDEN REFRESH CYCLE (WRITE)



5

TIMING DIAGRAMS (Continued)

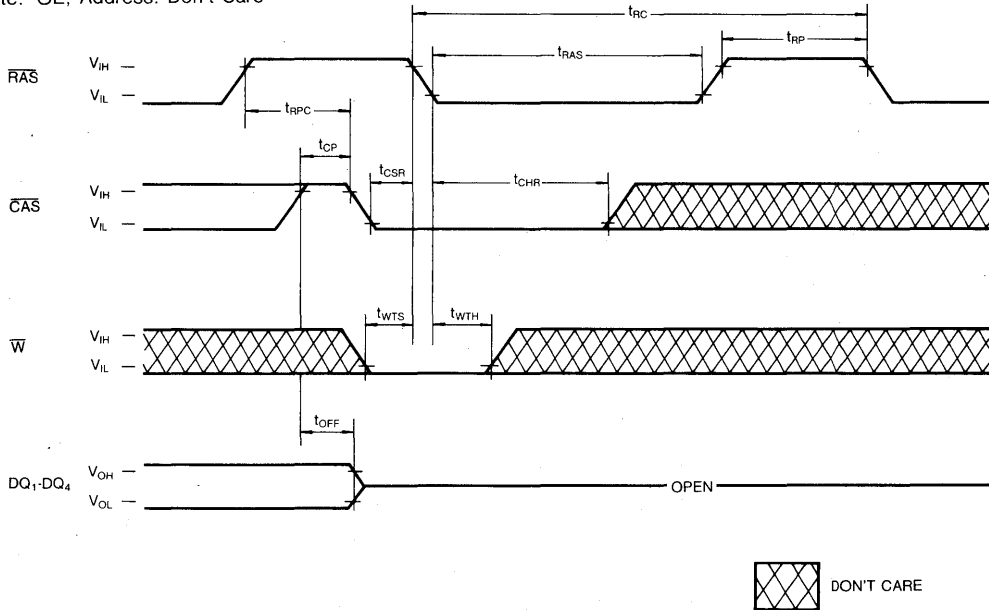
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: OE, Address: Don't Care



TEST MODE DESCRIPTION

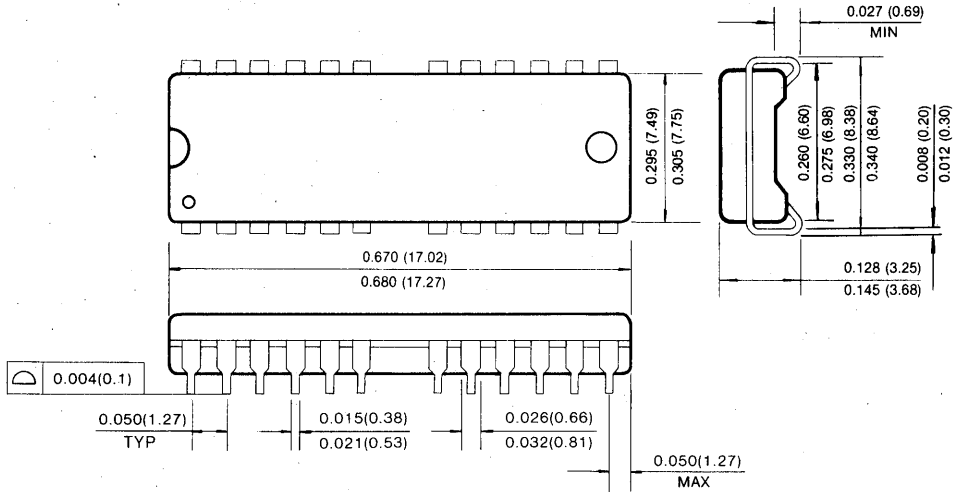
The KM44C4000A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A₀ and A₁ are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test

Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. \bar{W} , \bar{CAS} -BEFORE- \bar{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " \bar{CAS} -BEFORE- \bar{RAS} REFRESH CYCLE" or " \bar{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

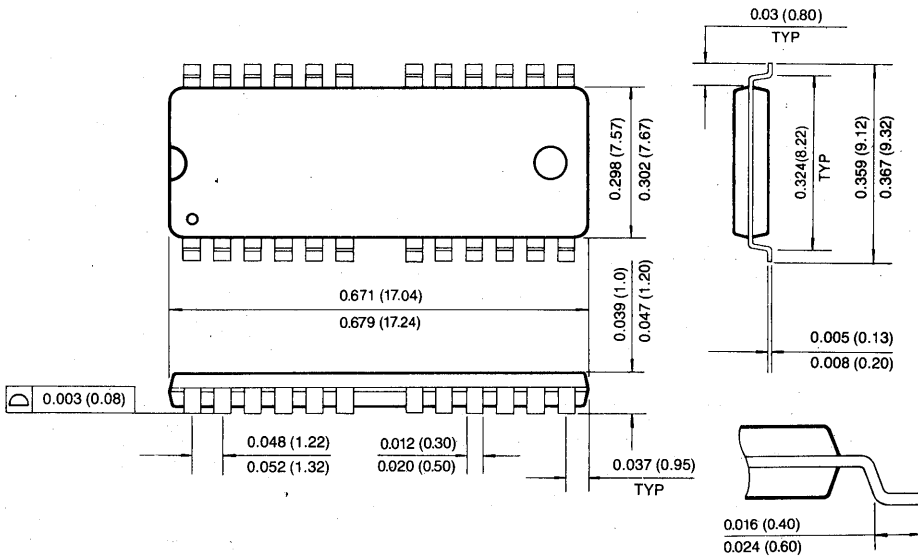
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



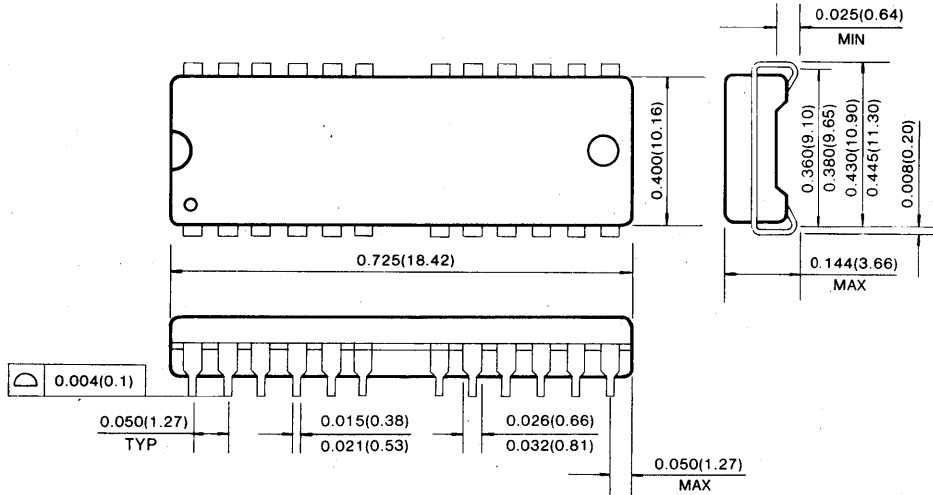
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



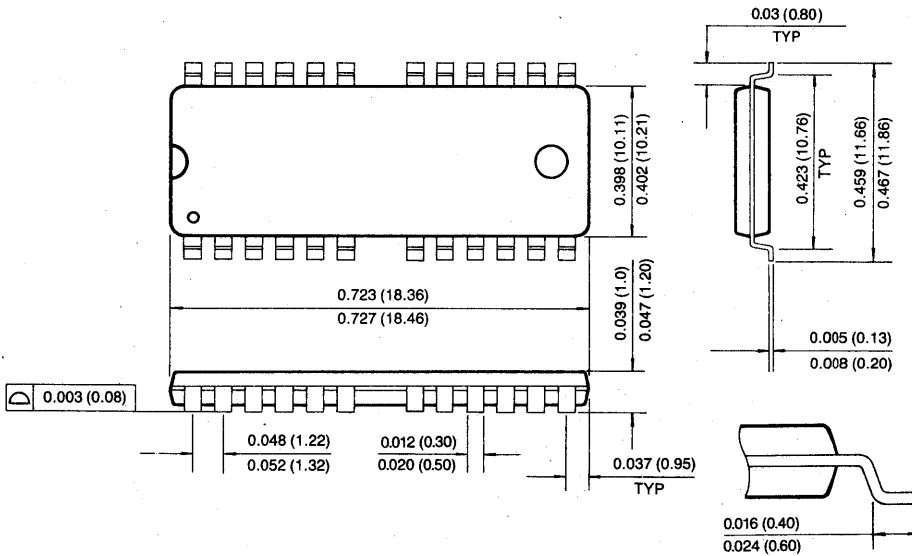
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{RC}
KM44C4100A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4100A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

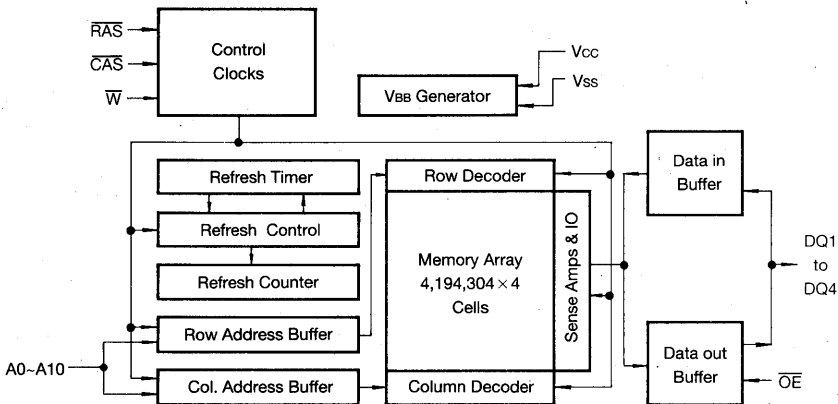
The Samsung KM44C4100A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

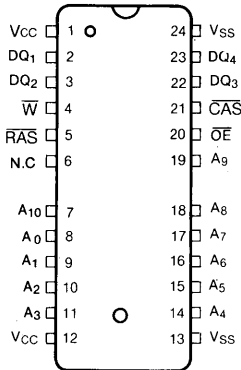
The KM44C4100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



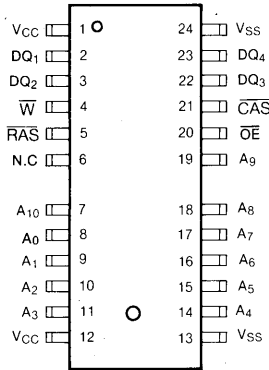
PIN CONFIGURATION (Top Views)

• KM44C4100 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



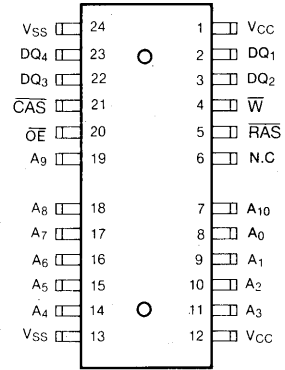
J : 400MIL
K : 300MIL

• KM44C4100 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4100 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~4	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{ss}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{cc} Supply Relative to V _{ss}	V _{cc}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{os}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{ss}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{cc}	4.5	5.0	5.5	V
Ground	V _{ss}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{cc} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (R _{AS} and C _{AS} Cycling @trc=min.)	KM44C4100A/AL/ALL/ASL-5	I _{cc1}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Standby Current (R _{AS} =C _{AS} =W=V _{IH})	KM44C4100A	I _{cc2}	-	2	mA
	KM44C4100AL			1	mA
	KM44C4100ALL			1	mA
	KM44C4100ASL			1	mA
R _{AS} -Only Refresh Current* (C _{AS} =V _{IH} , R _{AS} Cycling @trc=min.)	KM44C4100A/AL/ALL/ASL-5	I _{cc3}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* (R _{AS} =V _{IL} , C _{AS} , Address Cycling @tpc=min.)	KM44C4100A/AL/ALL/ASL-5	I _{cc4}	-	90	mA
	KM44C4100A/AL/ALL/ASL-6			80	mA
	KM44C4100A/AL/ALL/ASL-7			70	mA
	KM44C4100A/AL/ALL/ASL-8			60	mA
Standby Current (R _{AS} =C _{AS} =W=V _{cc} -0.2V)	KM44C4100A	I _{cc5}	-	1	mA
	KM44C4100AL			300	μA
	KM44C4100ALL			200	μA
	KM44C4100ASL			200	μA
C _{AS} -Before-R _{AS} Refresh Current* (R _{AS} and C _{AS} Cycling @trc=min.)	KM44C4100A/AL/ALL/ASL-5	I _{cc6}	-	110	mA
	KM44C4100A/AL/ALL/ASL-6			100	mA
	KM44C4100A/AL/ALL/ASL-7			90	mA
	KM44C4100A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{cc} -0.2V Input Low Voltage(V _{IL})=0.2V C _{AS} =C _{AS} -Before-R _{AS} Cycling or 0.2V DIN=Don't Care TRC=62.5μS(L-Ver.) 125μS(SL-Ver.), TRAS≤min-300ns	KM44C4100AL	I _{cc7}	-	400	μA
	KM44C4100ASL			300	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A10=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)	IOL	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25 C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A10)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CAS hold time	tcSH	50		60		70		80		ns	
CAS pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tcRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twts	10		10		10		10		ns	
Write command hold time (Test mode in)	twth	10		10		10		10		ns	
\bar{W} to \bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRP	10		10		10		10		ns	
\bar{W} to \bar{RAS} hold time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRH	10		10		10		10		ns	
\bar{RAS} pulse width (\bar{C} - \bar{B} - \bar{R} self refresh)	trASS	100		100		100		100		μ s	15
\bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} self refresh)	trPS	90		110		130		150		ns	15
\bar{CAS} hold time (\bar{C} - \bar{B} - \bar{R} self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

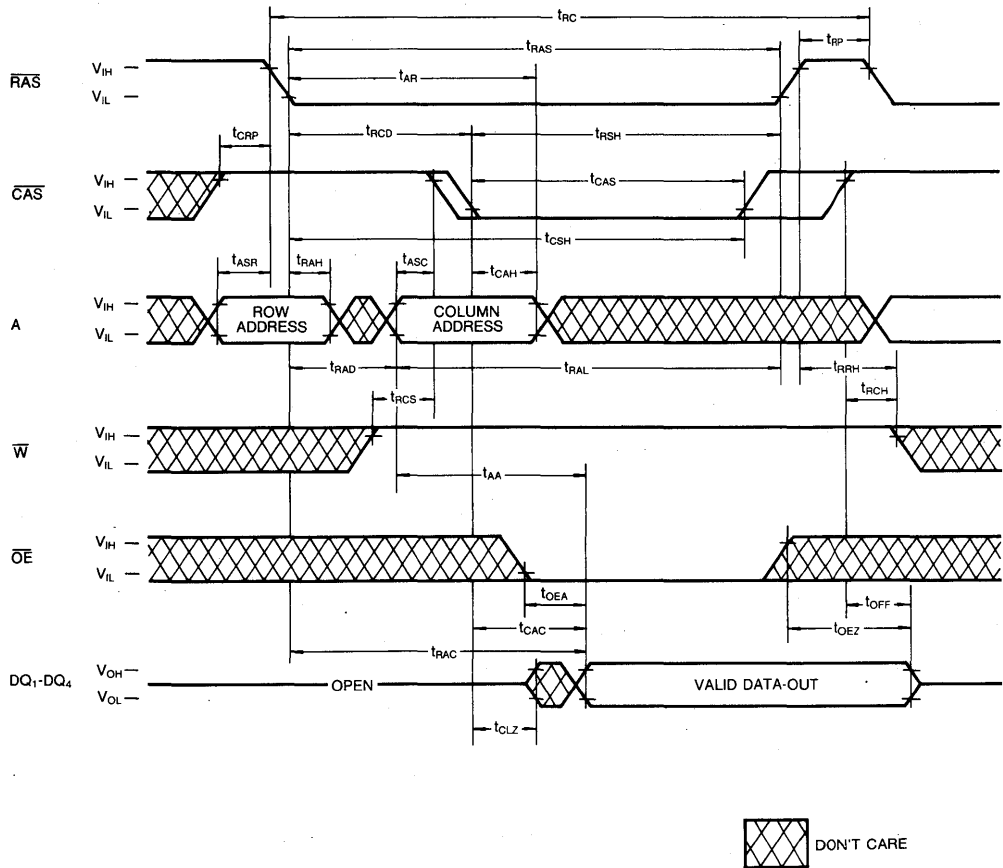
Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from \bar{RAS}	trAC		55		65		75		85	ns	3,4,11
Access time from \bar{CAS}	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\bar{RAS} pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
\bar{RAS} hold time	trSH	18		20		25		25		ns	
\bar{CAS} hold time	tCSH	55		65		75		85		ns	
Column address to \bar{RAS} lead time	trAL	30		35		40		45		ns	
\bar{CAS} to \bar{W} delay time	tCWD	41		45		55		55		ns	8
\bar{RAS} to \bar{W} delay time	trWD	78		90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tpc	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	trPWC	81		90		105		110		ns	
\bar{RAS} pulse width (Fast Page Mode)	trASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	tCPA		35		40		45		50	ns	3
\bar{OE} access time	toEA		18		20		25		25	ns	
\bar{OE} to data delay	toED	18		20		25		25		ns	
\bar{OE} command hold time	toEH	18		20		25		25		ns	

5

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

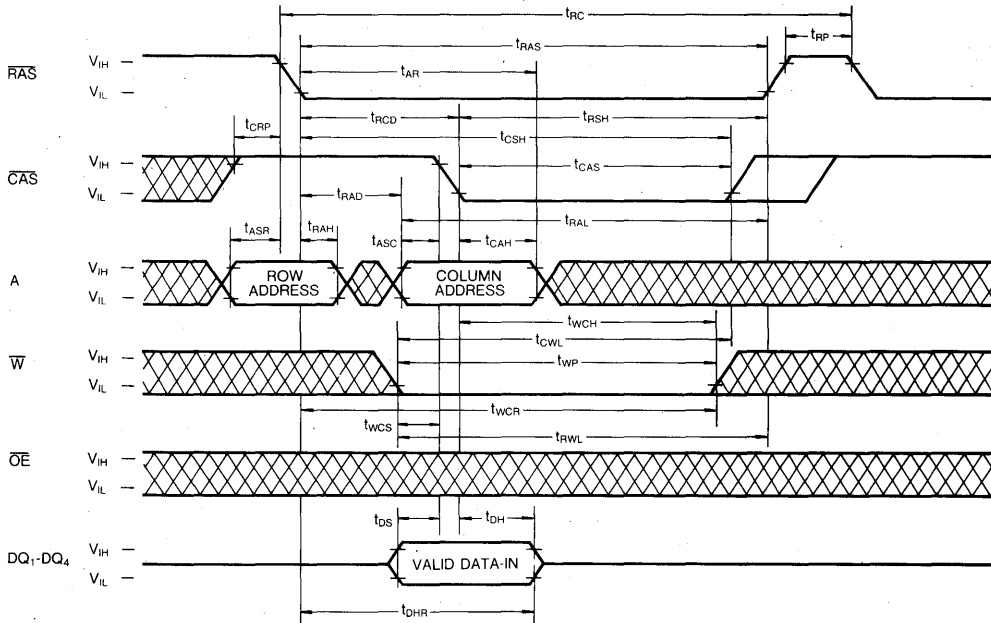
TIMING DIAGRAMS
READ CYCLE



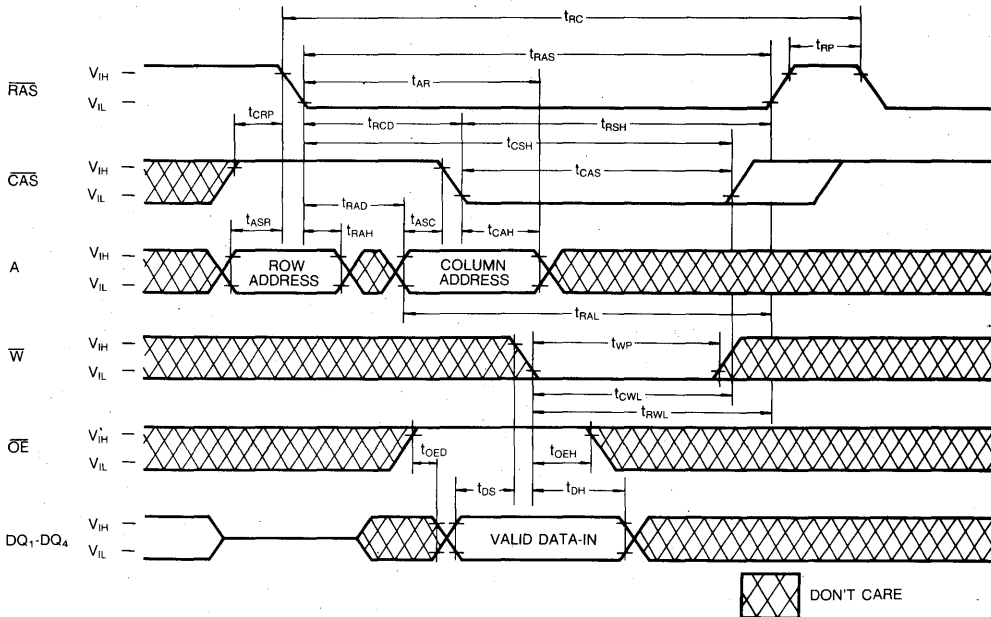
5

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

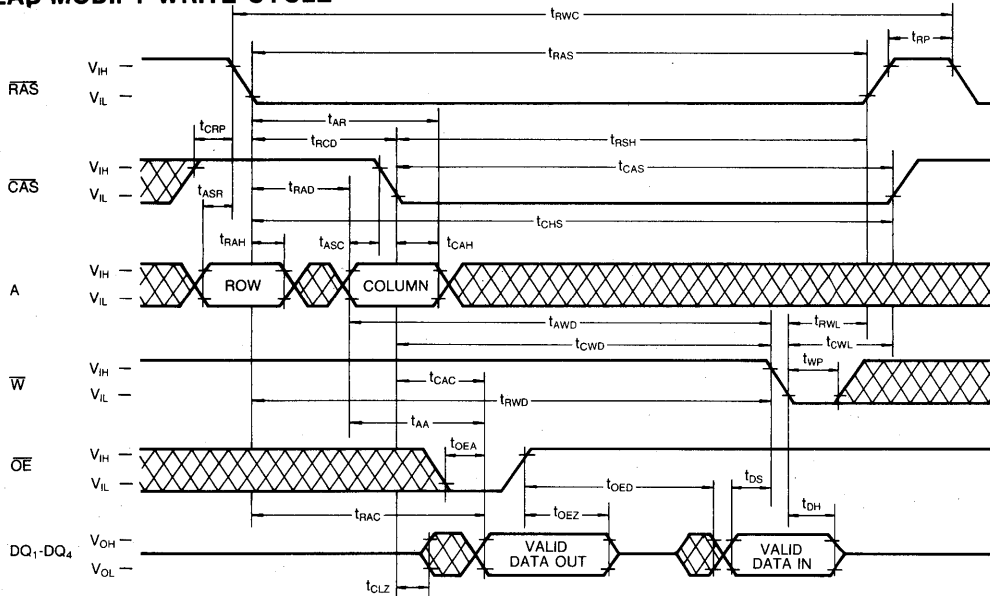


WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

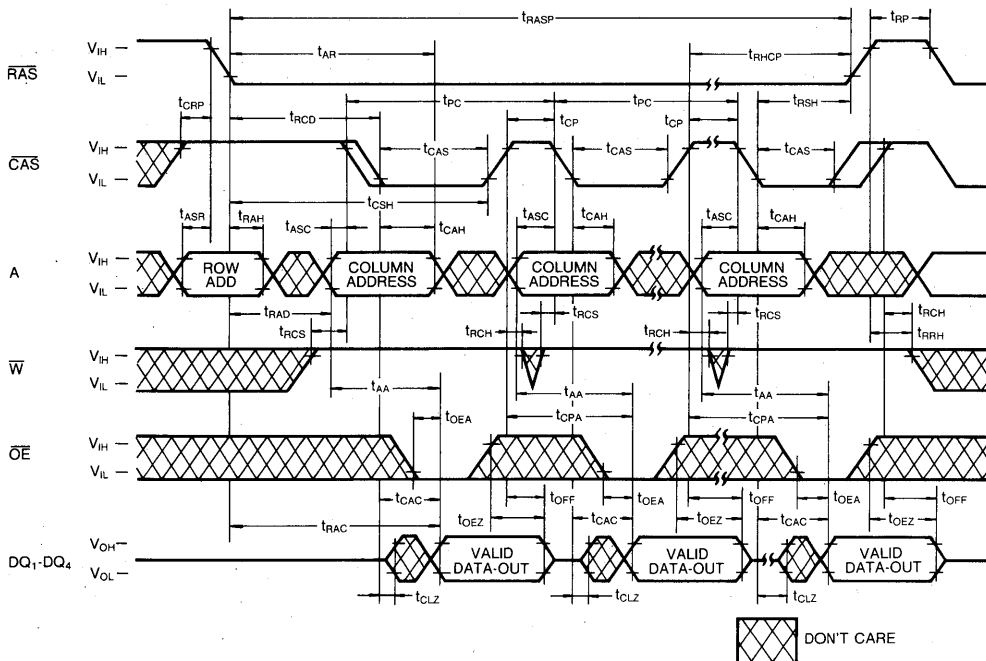


TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



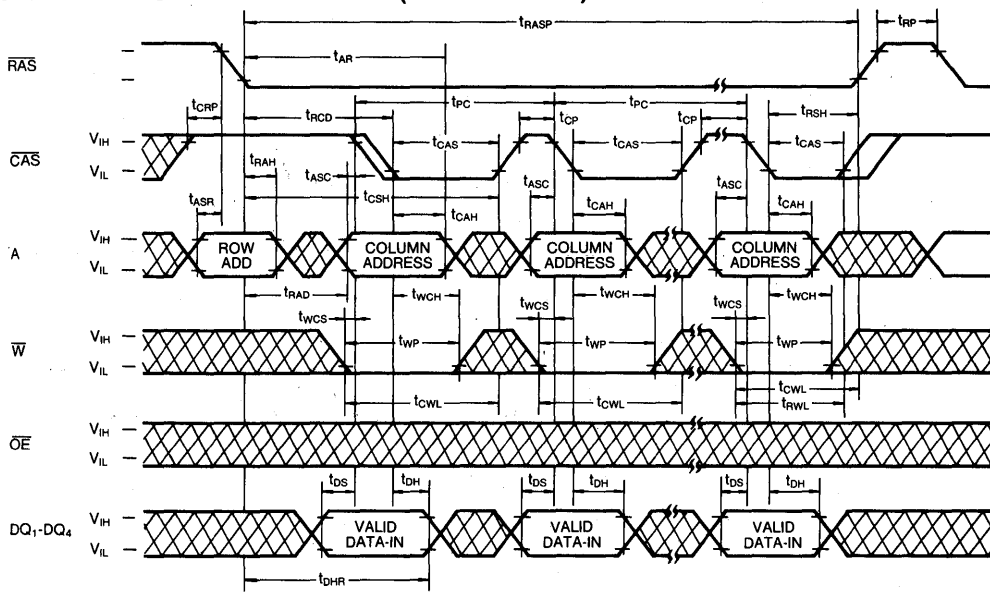
FAST PAGE MODE READ CYCLE



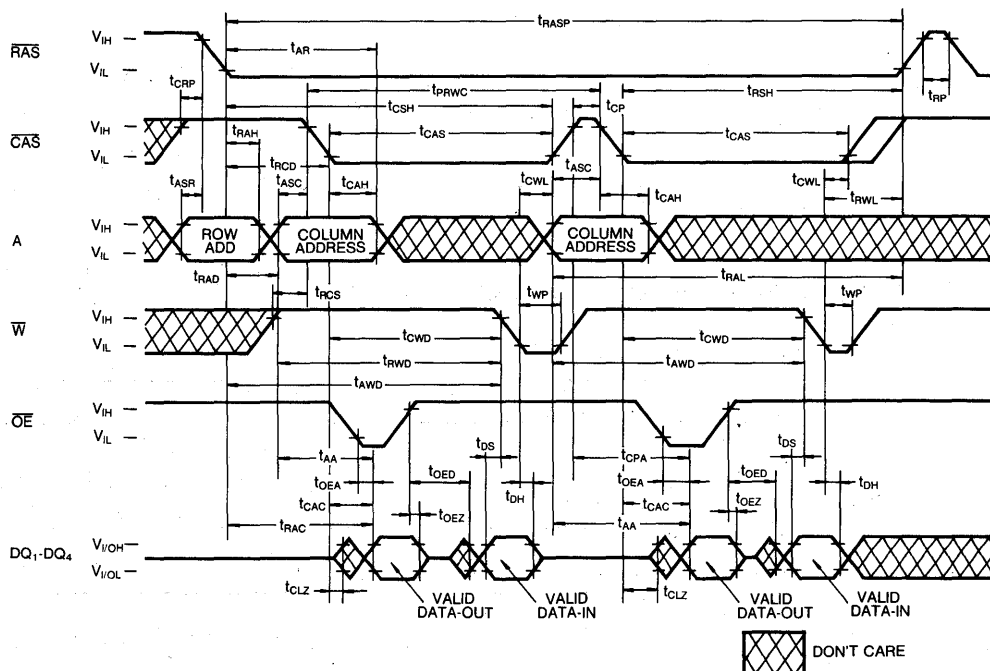
5

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



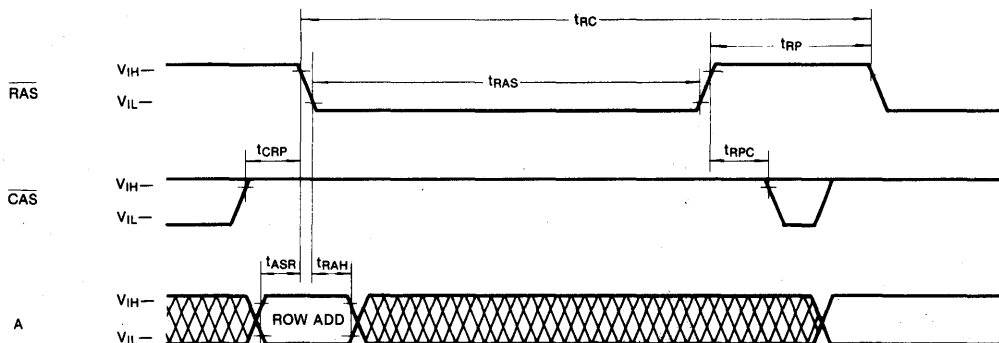
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

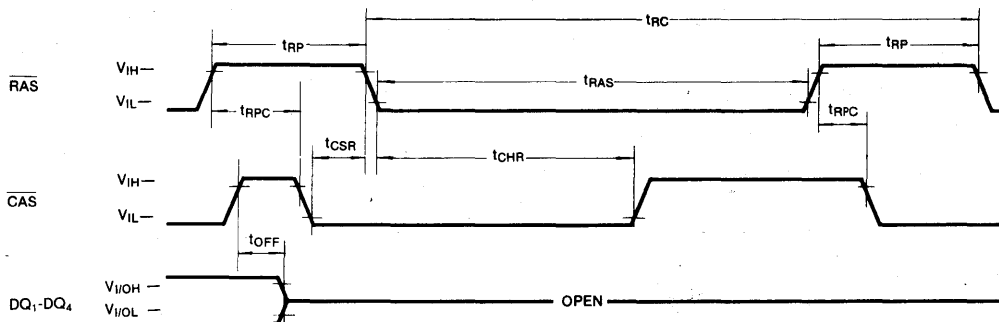
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} = Don't care



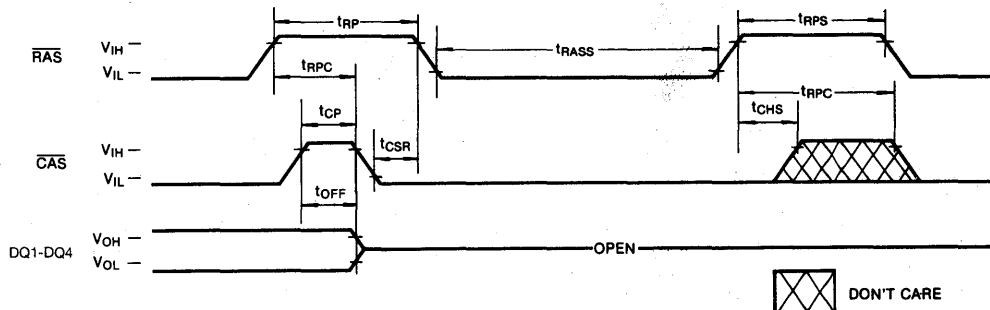
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \overline{W} = V_{IH} , \overline{OE} , A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

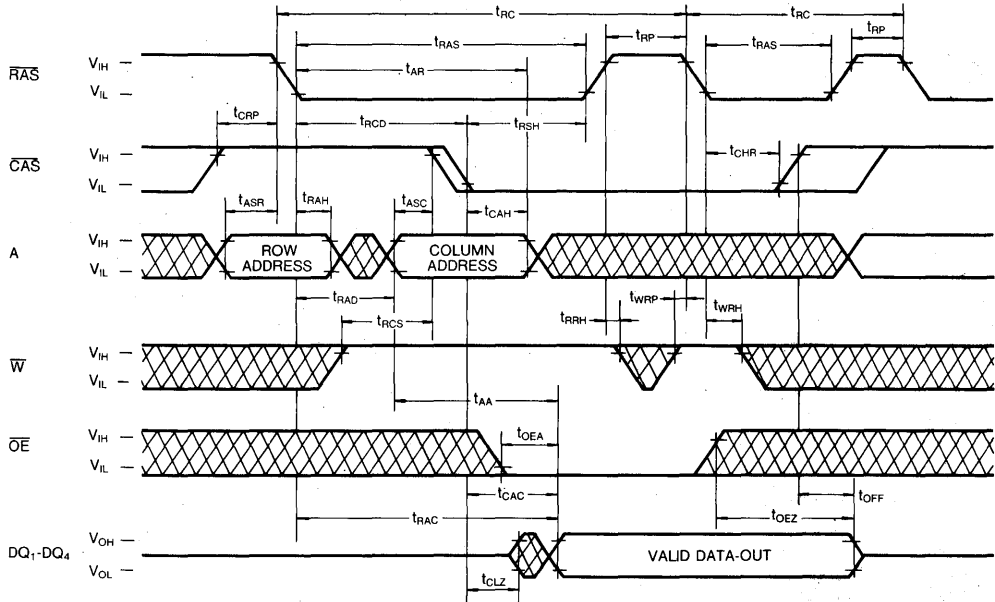
NOTE: \overline{W} , \overline{OE} , A = Don't Care



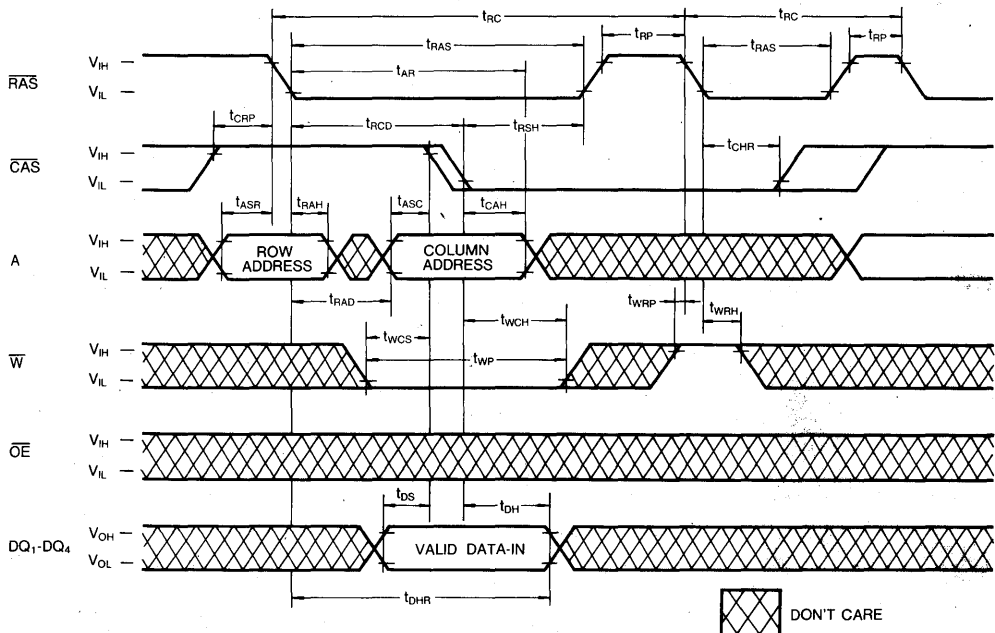
5

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

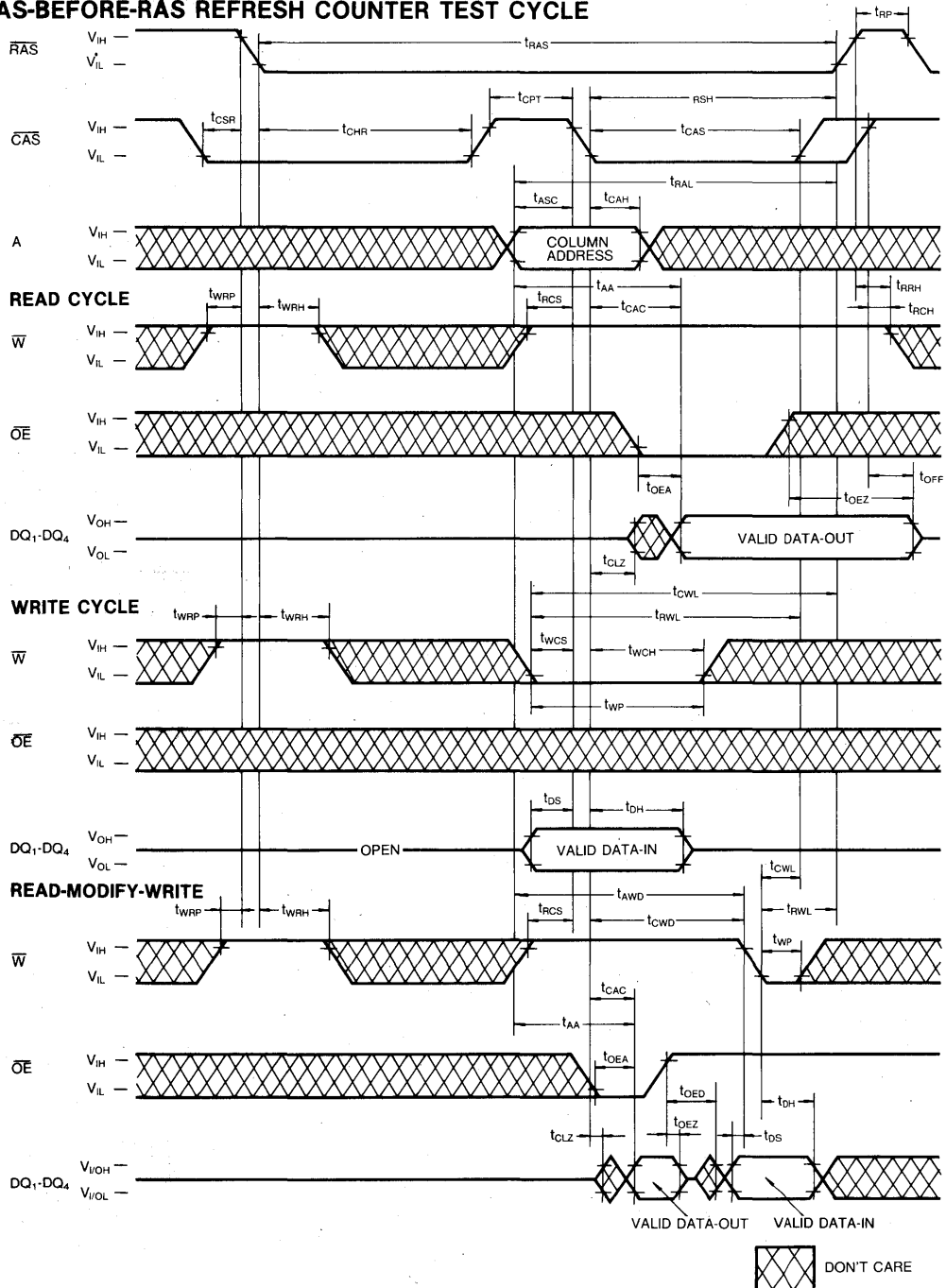


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

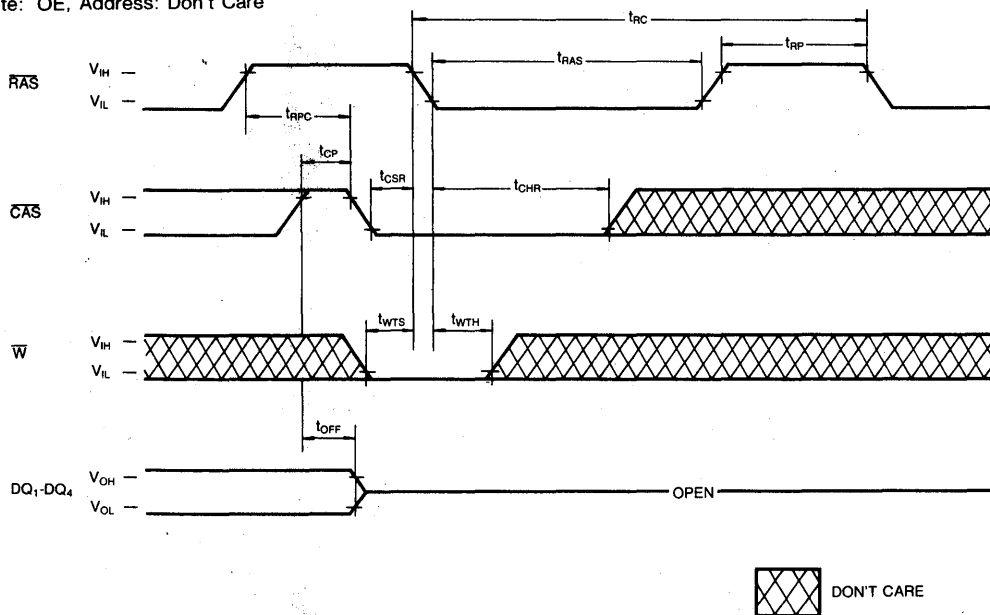


5

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: OE, Address: Don't Care



TEST MODE DESCRIPTION

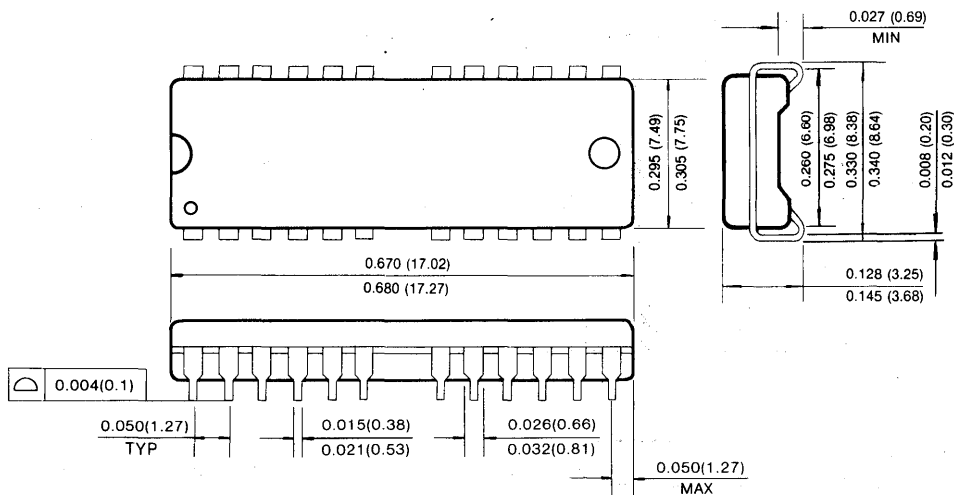
The KM44C4100A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A₀ and A₁ are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test

Mode", the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. W, CAS-BEFORE-RAS Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "CAS-BEFORE-RAS REFRESH CYCLE" or "RAS-only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

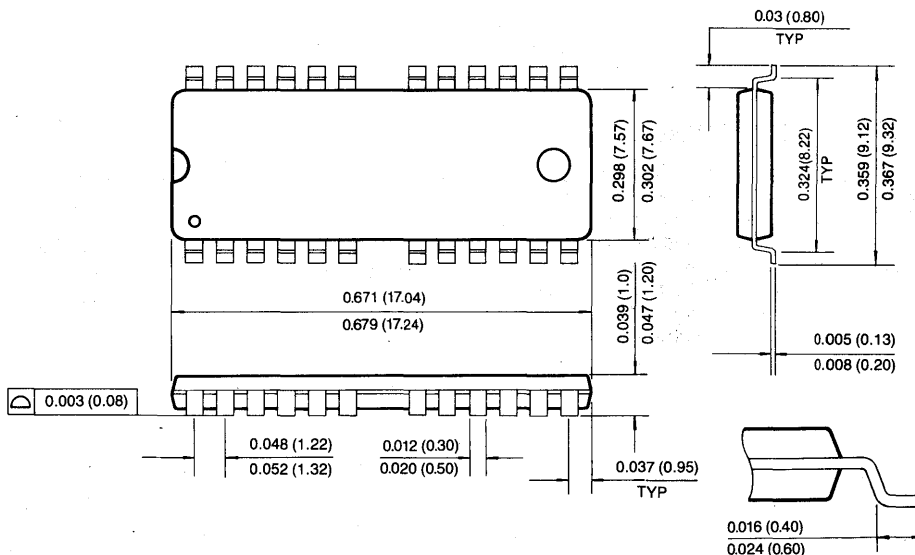
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

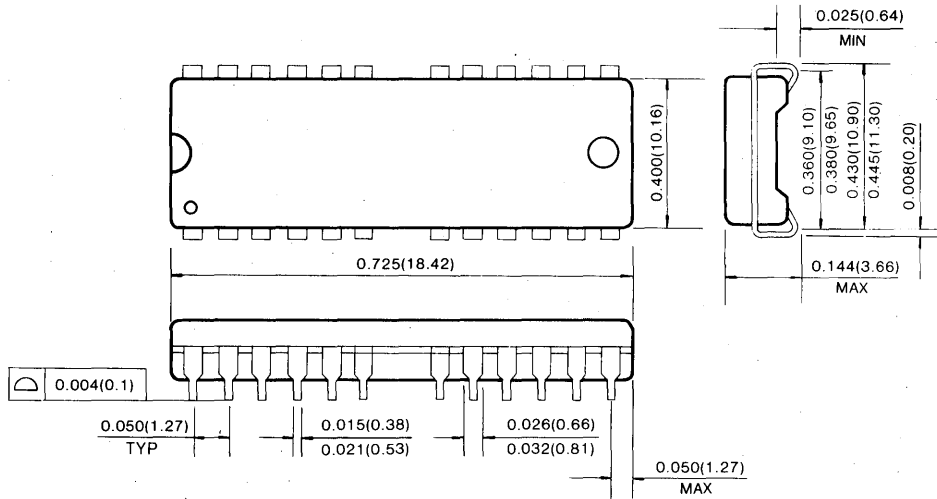


5

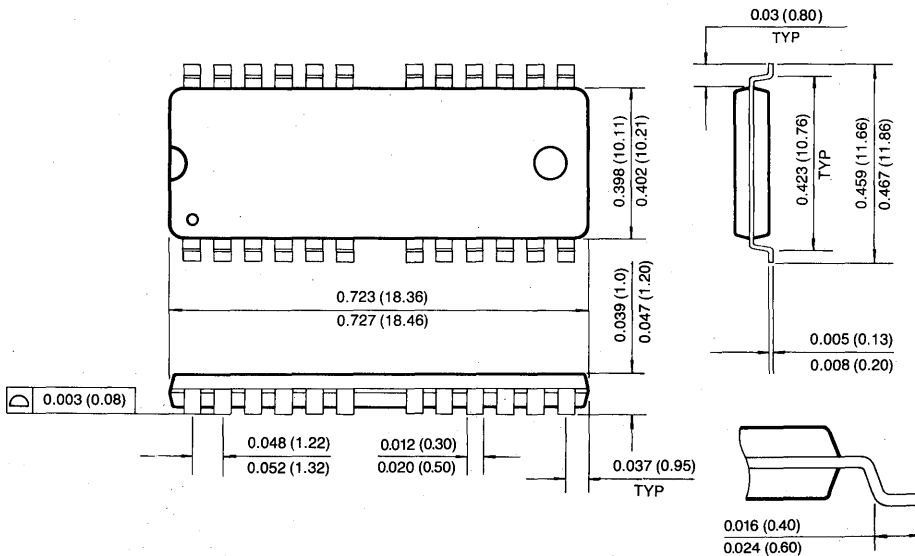
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE
(400MIL, Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

• **Performance range:**

	trAC	tcAC	trc
KM44C4010A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4010A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4010A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4010A/AL/ALL/ASL-8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **Self Refresh Operation (LL-ver. only)**
- **Write Per bit Mode capability**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V ± 10% power supply**
- **4096 cycles/64ms refresh (Normal)**
- **4096 cycles/128ms refresh (Low power & Self Ref.)**
- **4096 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

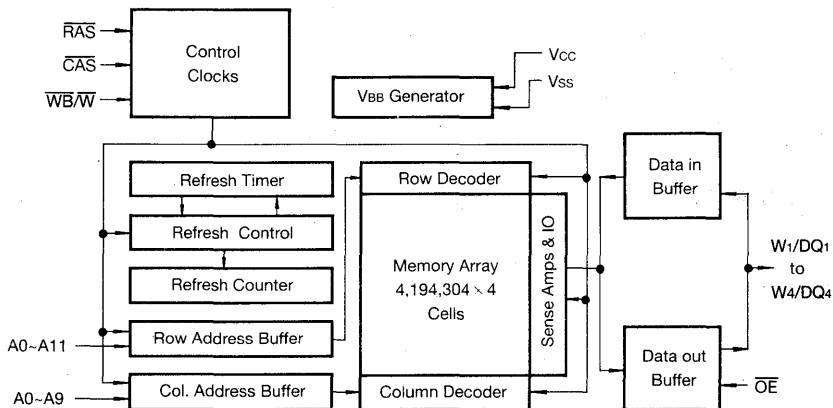
The Samsung KM44C4010A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4010A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

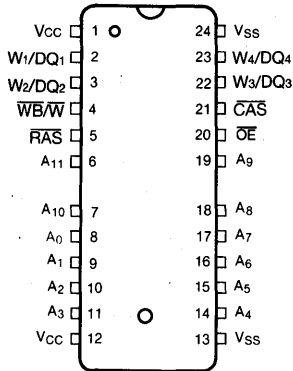
The KM44C4010A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



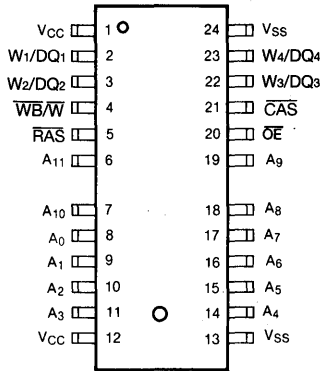
PIN CONFIGURATION (Top Views)

• KM44C4010 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



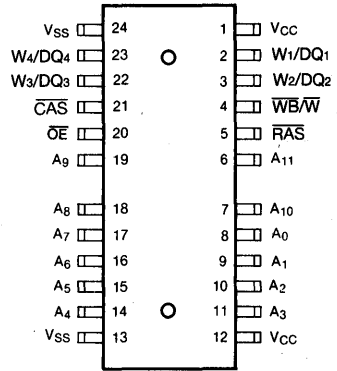
J : 400MIL
K : 300MIL

• KM44C4010 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4010 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
W1/DQ1-W4/DQ4	Write Select/Data in, out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WB/W}}$	Write Per Bit/Read/Write input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	Vcc + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44C4010A/AL/ALL/ASL-5		90	mA
	KM44C4010A/AL/ALL/ASL-6	I _{CC1}	80	mA
	KM44C4010A/AL/ALL/ASL-7		70	mA
	KM44C4010A/AL/ALL/ASL-8		60	mA
Standby Current (RAS=CAS=WB/W=V _{IH})	KM44C4010A	I _{CC2}	2	mA
	KM44C4010AL		1	mA
	KM44C4010ALL		1	mA
	KM44C4010ASL		1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM44C4010A/AL/ALL/ASL-5	I _{CC3}	90	mA
	KM44C4010A/AL/ALL/ASL-6		80	mA
	KM44C4010A/AL/ALL/ASL-7		70	mA
	KM44C4010A/AL/ALL/ASL-8		60	mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM44C4010A/AL/ALL/ASL-5	I _{CC4}	80	mA
	KM44C4010A/AL/ALL/ASL-6		70	mA
	KM44C4010A/AL/ALL/ASL-7		60	mA
	KM44C4010A/AL/ALL/ASL-8		50	mA
Standby Current (RAS=CAS=WB/W=Vcc-0.2V)	KM44C4010A	I _{CC5}	1	mA
	KM44C4010AL		300	µA
	KM44C4010ALL		200	µA
	KM44C4010ASL		200	µA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44C4010A/AL/ALL/ASL-5	I _{CC6}	90	mA
	KM44C4010A/AL/ALL/ASL-6		80	mA
	KM44C4010A/AL/ALL/ASL-7		70	mA
	KM44C4010A/AL/ALL/ASL-8		60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=Vcc-0.2V Input Low Voltage(V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V W ₁ /DQ ₁ -W ₄ /DQ ₄ =Don't Care trc=31.25µs(L-Ver) 62.5µs(SL-Ver), tRAS=tRAS min~300ns	KM44C4010AL	I _{CC7}	450	µA
	KM44C4010ASL		350	µA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V WB/W=OE=A0-A11=Vcc-0.2V or 0.2V W1/DQ1-W4/DQ4=Vcc-0.2V, 0.2V or Open	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ Vin ≤ Vcc+0.5V, all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)	IoL	-10	10	μA
Output High Voltage Level (IoH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IoL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, WB/W, OE)	CIN2	-	7	pF
Input Capacitance (W1/DQ1-W4/DQ4)	CdQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trWC	133		155		185		205		ns	
Access time from RAS	trAC		50		60		70		80	ns	3,4,11
Access time from CAS	tcAC		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toFF	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trP	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CAS hold time	tcSH	50		60		70		80		ns	
CAS pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tcRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	TRAH	10		10		10		10		ns	
Column address set-up time	TASC	0		0		0		0		ns	
Column address hold time	TCAH	10		10		15		15		ns	
Column address hold time referenced to \overline{RAS}	TAR	40		45		55		60		ns	6
Column address to \overline{RAS} lead time	TRAL	25		30		35		40		ns	
Read command set-up time	TRCS	0		0		0		0		ns	
Read command hold time referenced to \overline{CAS}	TRCH	0		0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	TRRH	0		0		0		0		ns	
Write command hold time	TWCH	10		10		15		15		ns	
Write command hold time referenced to \overline{RAS}	TWCR	40		45		55		60		ns	6
Write command pulse width	TWP	10		10		15		15		ns	
Write command to \overline{RAS} lead time	TRWL	15		15		20		20		ns	
Write command to \overline{CAS} lead time	TCWL	13		15		20		20		ns	
Data set-up time	TDS	0		0		0		0		ns	10
Data hold time	TDH	10		10		15		15		ns	10
Data hold time referenced to \overline{RAS}	TDHR	40		45		55		60		ns	6
Refresh period (Normal)	TREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	TREF		128		128		128		128	ms	
Refresh period (Super Low power)	TREF		256		256		256		256	ms	
Write command set-up time	TWCS	0		0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	TCWD	36		40		50		50		ns	8
\overline{RAS} to \overline{W} delay time	TRWD	73		85		100		110		ns	8
Column address to \overline{W} delay time	TAWD	48		55		65		70		ns	8
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	TCSR	10		10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	TCHR	10		10		15		15		ns	
\overline{RAS} to \overline{CAS} precharge time	TRPC	5		5		5		5		ns	
\overline{CAS} precharge time (\overline{C} - \overline{B} - \overline{R} counter test cycle)	TCPT	20		20		30		30		ns	
Access time from \overline{CAS} precharge	TCPA		30		35		40		45	ns	3
Fast Page mode cycle time	TPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	TPRWC	76		85		100		105		ns	
\overline{CAS} precharge time (Fast Page mode)	TCP	10		10		10		10		ns	
\overline{RAS} pulse width(Fast Page mode)	TRASP	50	200000	60	200000	70	200000	80	200000	ns	
\overline{RAS} hold time from \overline{CAS} precharge	TRHCP	30		35		40		45		ns	
\overline{OE} access time	TOEA		13		15		20		20	ns	
\overline{OE} to data delay	TOED	13		15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	TOEZ	0	13	0	15	0	20	0	20	ns	
\overline{OE} command hold time	TOEH	13		15		20		20		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	
W to RAS precharge time (C-B-R refresh)	twRP	10		10		10		10		ns	
W to RAS hold time (C-B-R refresh)	twRH	10		10		10		10		ns	
RAS pulse width (C-B-R self refresh)	trASS	100		100		100		100		μs	15
RAS precharge time (C-B-R self refresh)	trPS	90		110		130		150		ns	15
CAS hold time (C-B-R self refresh)	tcHS	-50		-50		-50		-50		ns	15
Write per bit set-up time	twBS	0		0		0		0		ns	
Write per bit hold time	twBH	10		10		10		10		ns	
Write selection set-up time	twDS	0		0		0		0		ns	
Write per bit selection hold time	twDH	10		10		10		10		ns	

TEST MODE CYCLE

(Note.12)

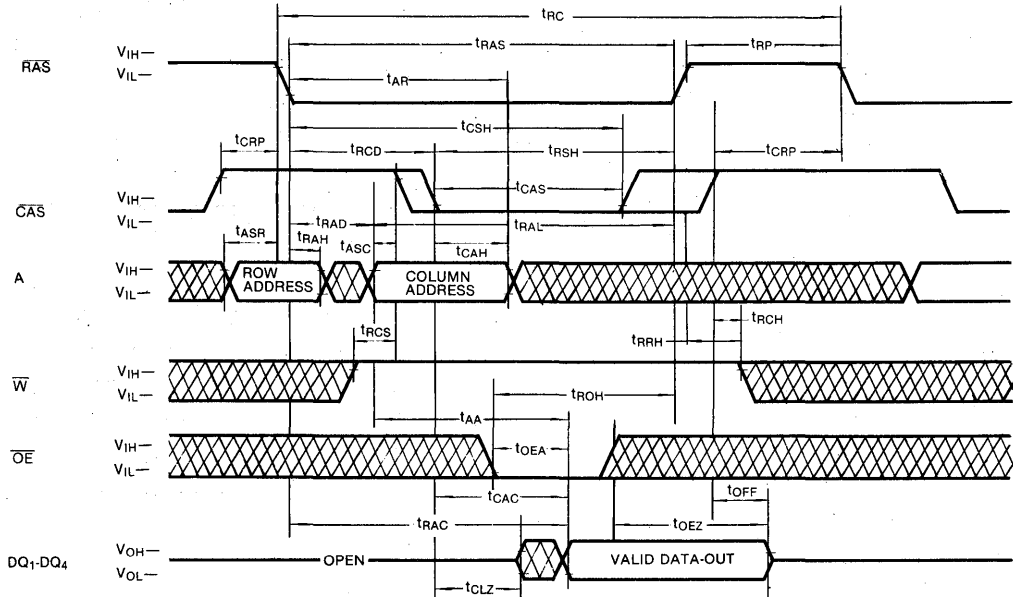
Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from RAS	trAC		55		65		75		85	ns	3,4,11
Access time from CAS	tcAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
RAS pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
CAS pulse width	tcAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	trSH	18		20		25		25		ns	
CAS hold time	tcSH	55		65		75		85		ns	
Column address to RAS lead time	trAL	30		35		40		45		ns	
CAS to W delay time	tcWD	41		45		55		55		ns	8
RAS to W delay time	trWD	78		90		105		115		ns	8
Column address to W delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tpC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tpRWC	81		90		105		110		ns	
RAS pulse width (Fast Page Mode)	trASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tcPA		35		40		45		50	ns	3
OE access time	toEA		18		20		25		25	ns	
OE to data delay	toED	18		20		25		25		ns	
OE command hold time	toEH	18		20		25		25		ns	

NOTES

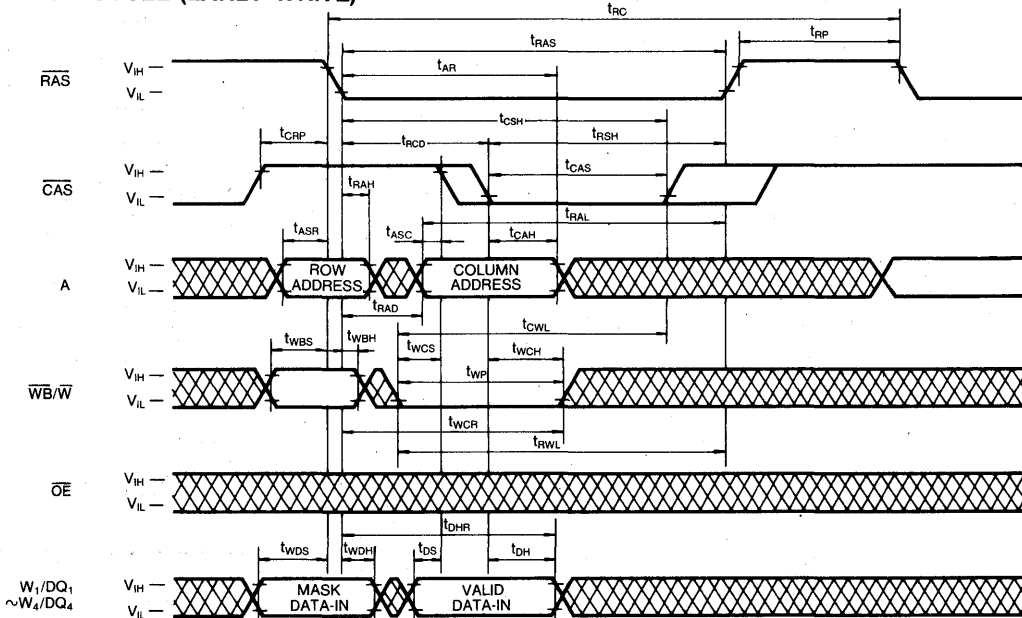
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE



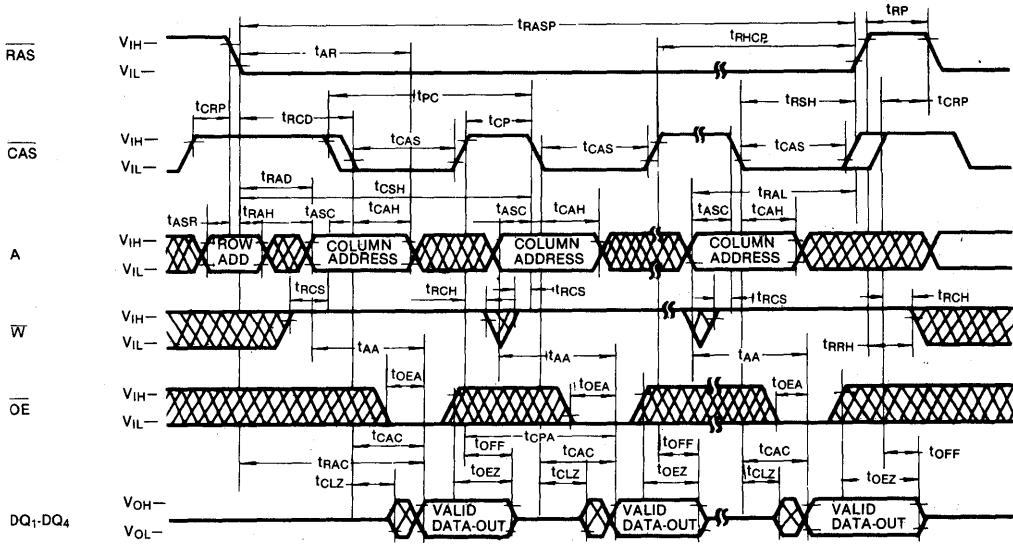
WRITE CYCLE (EARLY WRITE)



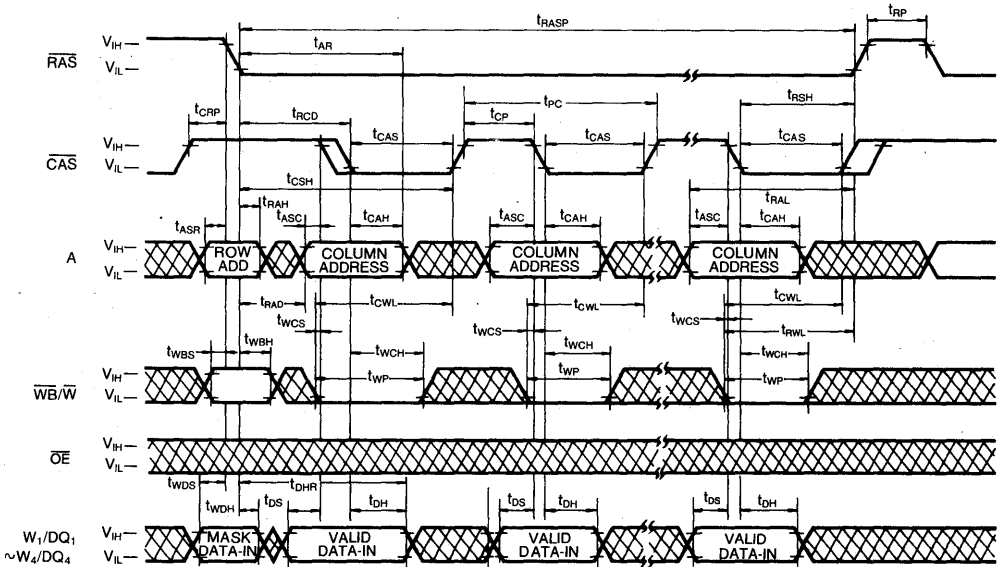
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

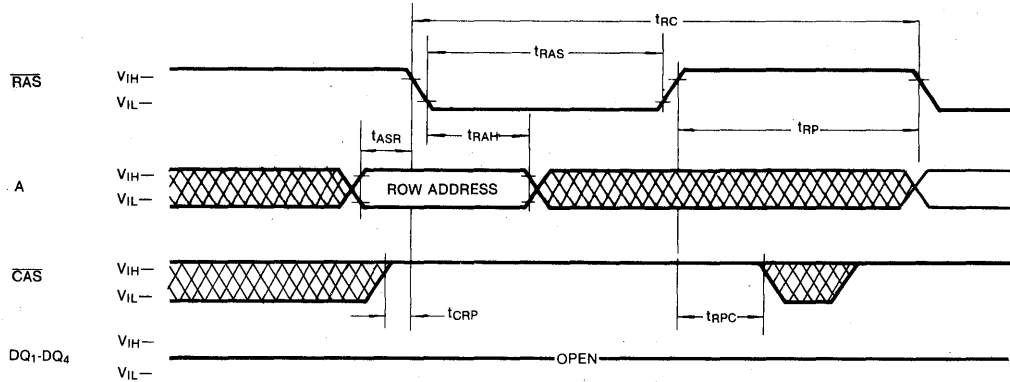


DON'T CARE

TIMING DIAGRAMS (Continued)

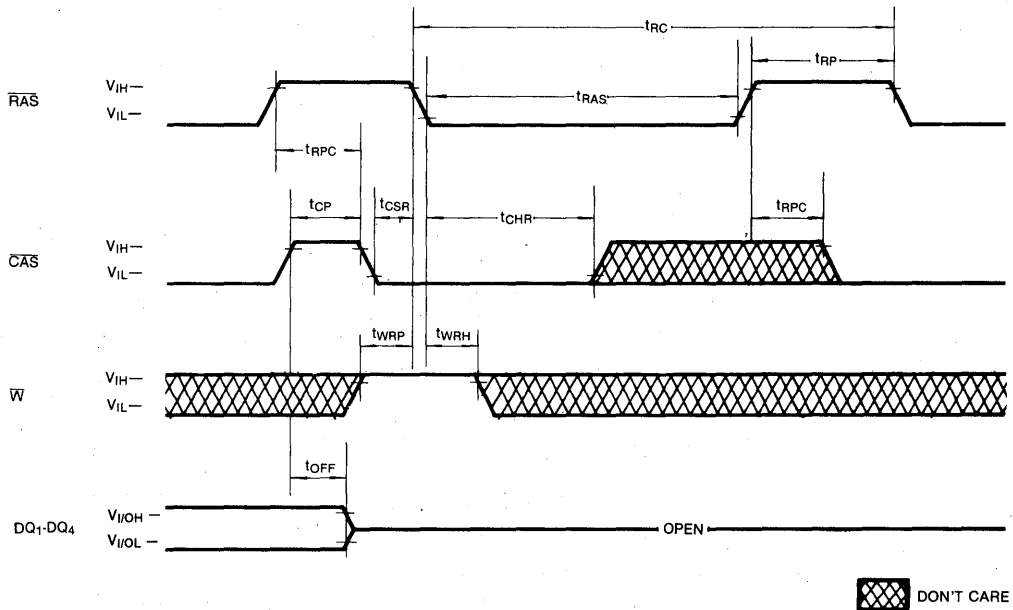
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't Care



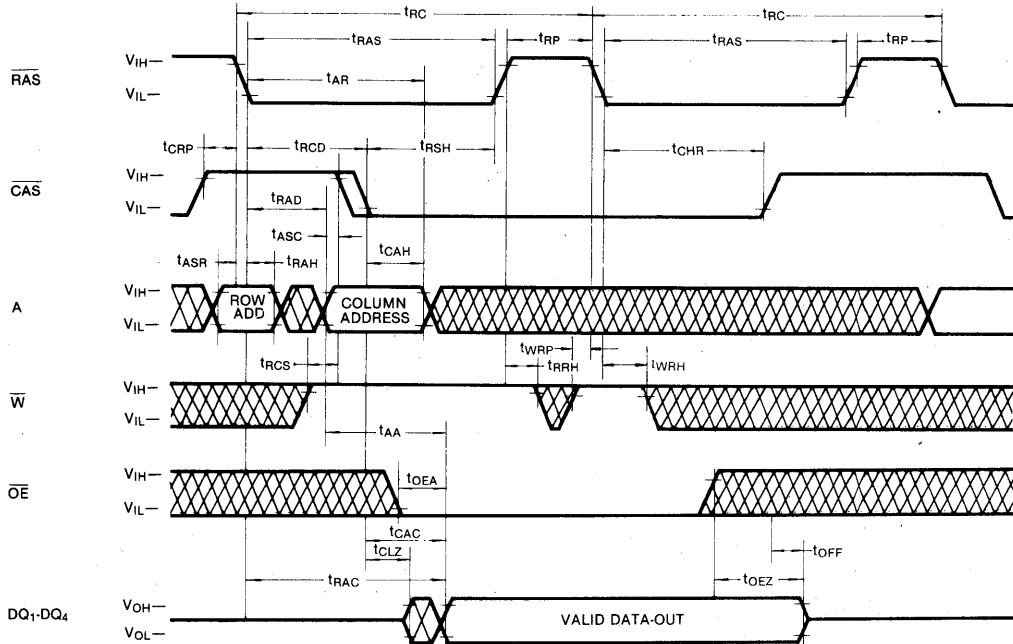
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \bar{OE} , Address = Don't Care

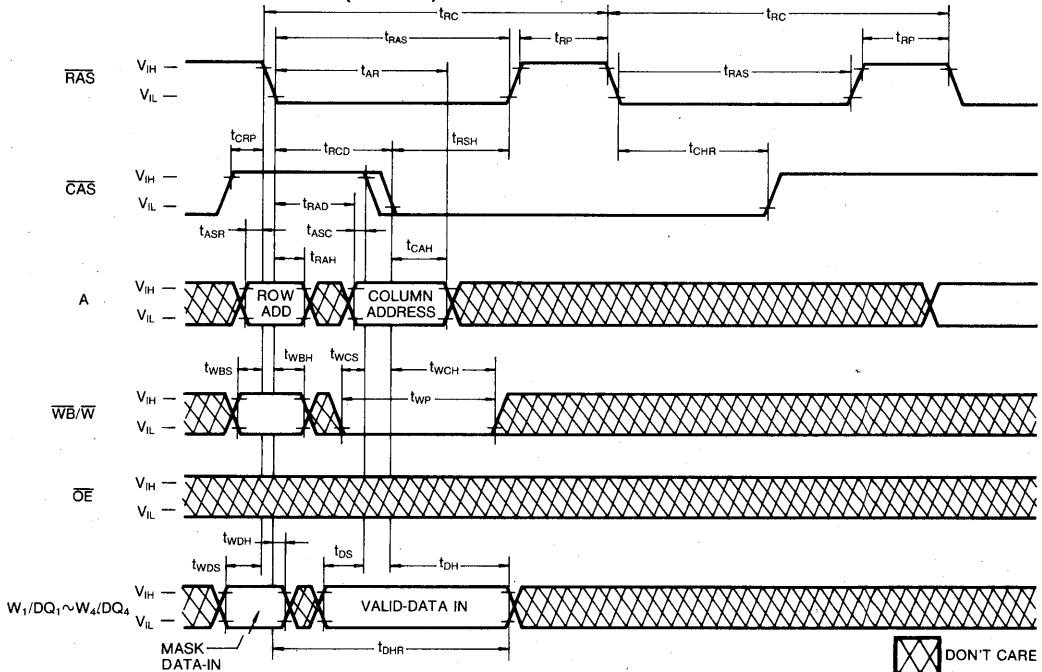


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



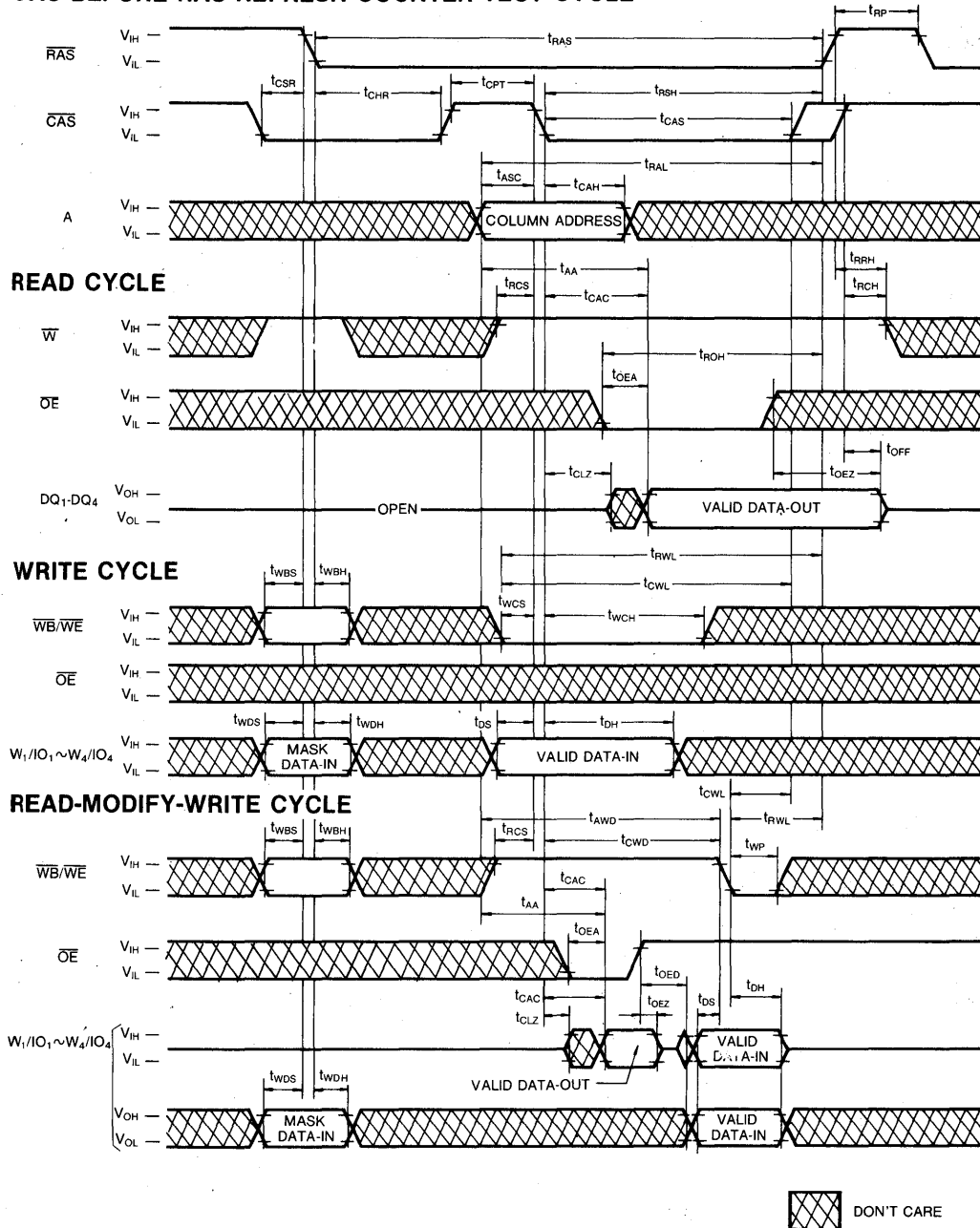
HIDDEN REFRESH CYCLE (WRITE)



5

TIMING DIAGRAMS (Continued)

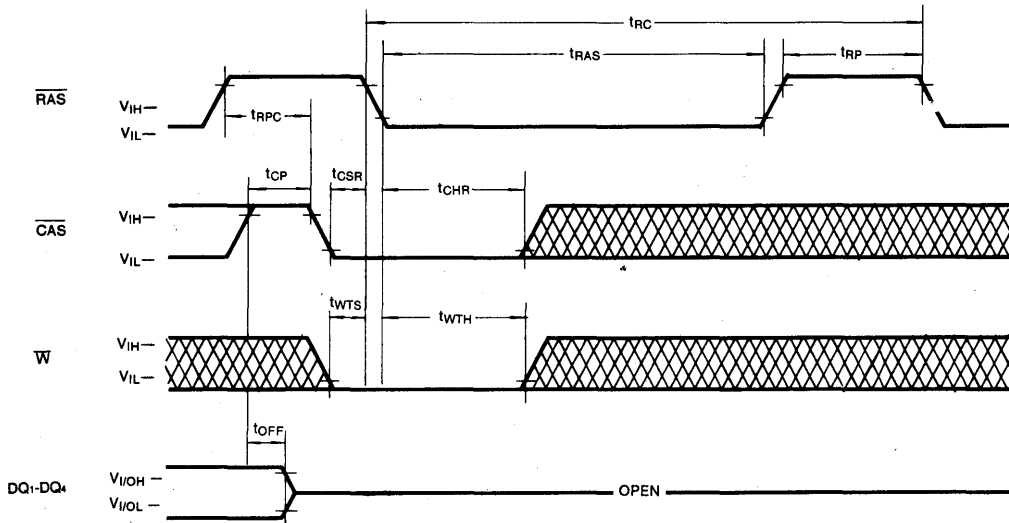
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: \overline{OE} , Address=Don't Care



5

DON'T CARE

TEST MODE DESCRIPTION

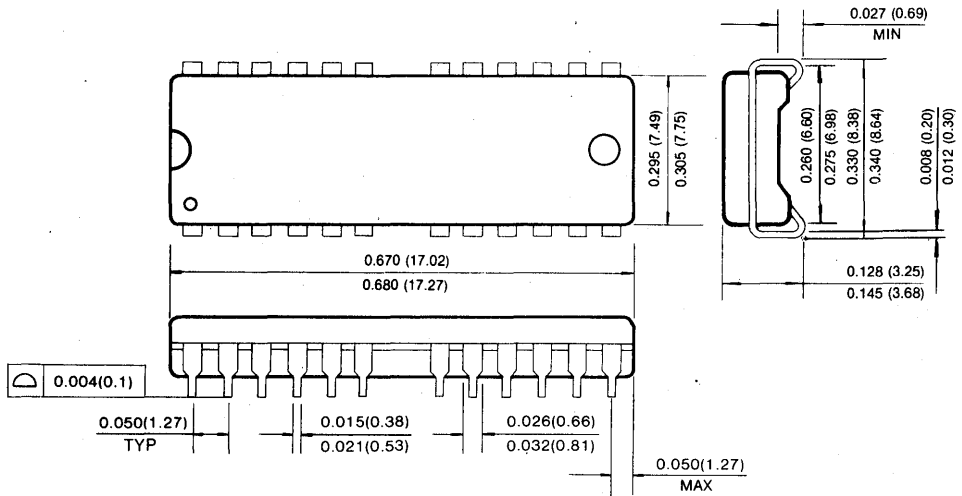
The KM44C4010 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin

would indicate a "0". In "Test Mode", the $4M \times 4$ DRAM can be tested as if it were a $1M \times 4$ DRAM. \overline{W} , \overline{CAS} -Before-Ras Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " \overline{CAS} -Before- \overline{RAS} Refresh Cycle" or " \overline{RAS} only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

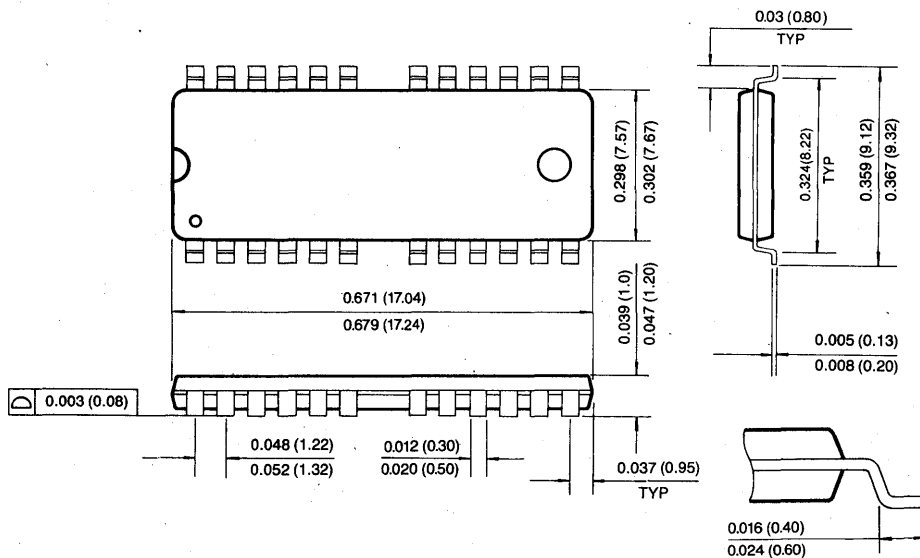
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



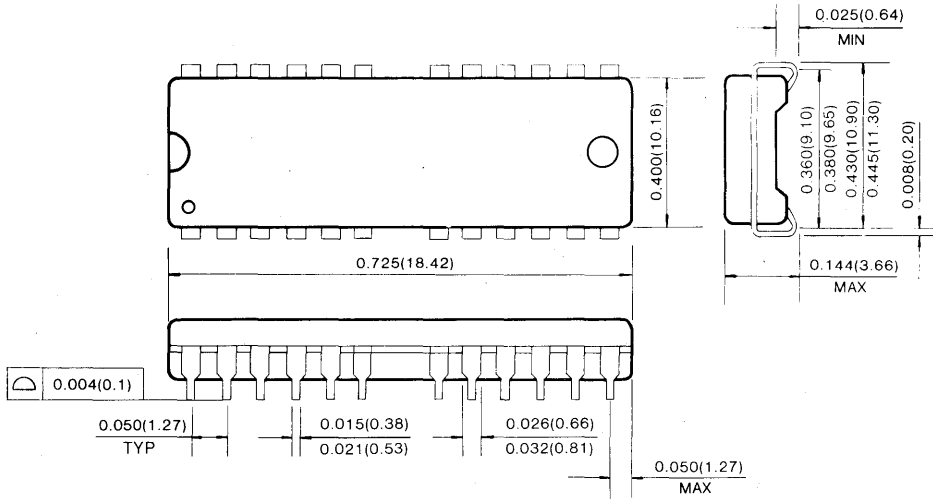
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



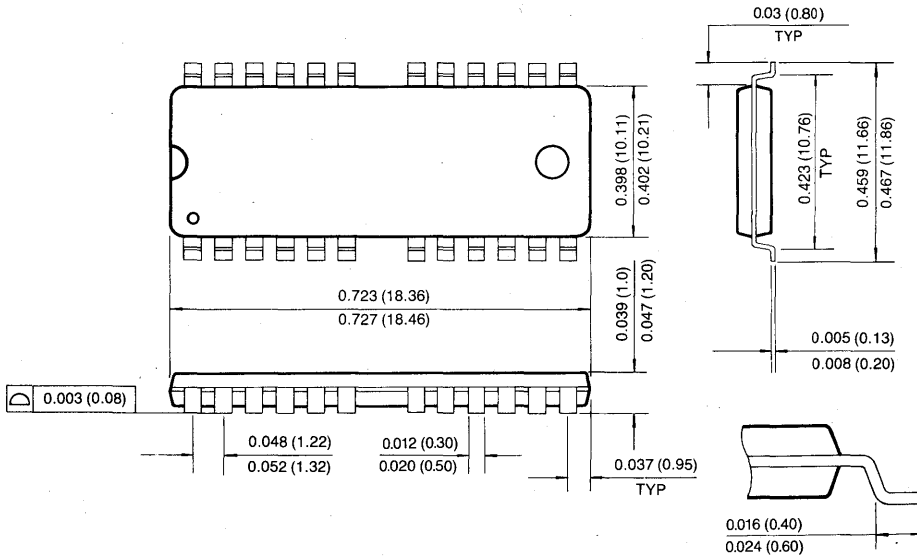
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



5

4M × 4 Bit CMOS Dynamic RAM with Fast Page Mode (Write Per Bit Mode)

FEATURES

• Performance range:

	t _{RAC}	t _{CAC}	t _{RC}
KM44C4110A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4110A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4110A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4110A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refrdsh Operation (LL-ver. only)
- Write Per Bit Mode capability
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

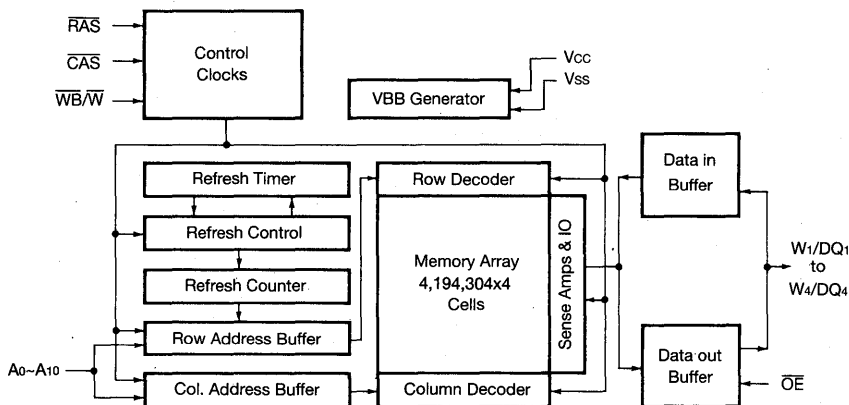
The Samsung KM44C4110A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4110A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

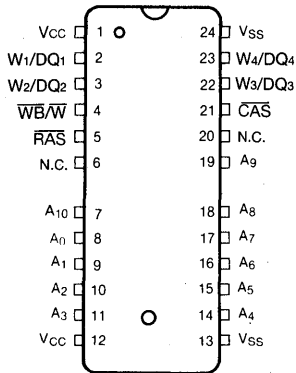
The KM44C4110A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



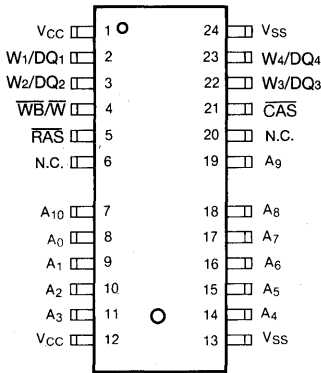
PIN CONFIGURATION (Top Views)

• KM44C4110 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



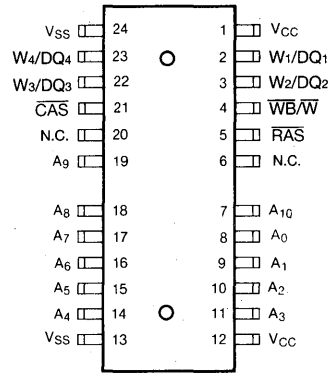
J : 400MIL
K : 300MIL

• KM44C4110 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4110 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
W1/DQ1-w4/DQ4	Write Select/Data in, out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
WB/W	Write Per Bit/Read, Write input
OE	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44C4110A/AL/ALL/ASL-5	I _{CC1}	-	110	mA
	KM44C4110A/AL/ALL/ASL-6			100	mA
	KM44C4110A/AL/ALL/ASL-7			90	mA
	KM44C4110A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{WB}/\overline{W}=V_{IH}$)	KM44C4110A	I _{CC2}	-	2	mA
	KM44C4110AL			1	mA
	KM44C4110ALL			1	mA
	KM44C4110ASL			1	mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} Cycling @trc=min.)	KM44C4110A/AL/ALL/ASL-5	I _{CC3}	-	110	mA
	KM44C4110A/AL/ALL/ASL-6			100	mA
	KM44C4110A/AL/ALL/ASL-7			90	mA
	KM44C4110A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @tpc=min.)	KM44C4110A/AL/ALL/ASL-5	I _{CC4}	-	90	mA
	KM44C4110A/AL/ALL/ASL-6			80	mA
	KM44C4110A/AL/ALL/ASL-7			70	mA
	KM44C4110A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{WB}/\overline{W}=V_{CC}-0.2V$)	KM44C4110A	I _{CC5}	-	1	mA
	KM44C4110AL			300	μA
	KM44C4110ALL			200	μA
	KM44C4110ASL			200	μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44C4110A/AL/ALL/ASL-5	I _{CC6}	-	110	mA
	KM44C4110A/AL/ALL/ASL-6			100	mA
	KM44C4110A/AL/ALL/ASL-7			90	mA
	KM44C4110A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{CAS}=\overline{CAS}$ -Before- \overline{RAS} Cycling or 0.2V DQ1-DQ4=Don't Care trc=62.5μs(L-Ver.) 125μs(SL-Ver.), t _{RAS} =t _{RAS} min-300ns	KM44C4110AL	I _{CC7}	-	400	μA
	KM44C4110ASL			300	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V WB/W=OE=A0-A10=Vcc-0.2V or 0.2V W1/DQ1-W4/DQ4=Vcc-0.2V, 0.2V or Open	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)	IOL	-10	10	μA
Output High Voltage Level (Ioh=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (Iol=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A10)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, WB/W, OE)	CIN2	-	7	pF
Input Capacitance (W1/DQ1~W4/DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CAS hold time	tCSH	50		60		70		80		ns	
CAS pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		50		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	
\bar{W} to \bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	twRP	10		10		10		10		ns	
\bar{W} to \bar{RAS} hold time (\bar{C} - \bar{B} - \bar{R} refresh)	twRH	10		10		10		10		ns	
\bar{RAS} pulse width (\bar{C} - \bar{B} - \bar{R} self refresh)	trASS	100		100		100		100		μ s	15
\bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} self refresh)	trPS	90		110		130		150		ns	15
\bar{CAS} hold time (\bar{C} - \bar{B} - \bar{R} self refresh)	tCHS	-50		-50		-50		-50		ns	15
Write per bit set-up time	twBS	0		0		0		0		ns	
Write per bit hold time	twBH	10		10		10		10		ns	
Write selection set-up time	twDS	0		0		0		0		ns	
Write per bit selection hold time	twDH	10		10		10		10		ns	

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from \bar{RAS}	trAC		55		65		75		85	ns	3,4,11
Access time from \bar{CAS}	trAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\bar{RAS} pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	trCS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
\bar{RAS} hold time	trSH	18		20		25		25		ns	
\bar{CAS} hold time	trSH	55		65		75		85		ns	
Column address to \bar{RAS} lead time	trAL	30		35		40		45		ns	
\bar{CAS} to \bar{W} delay time	trWD	41		45		55		55		ns	8
\bar{RAS} to \bar{W} delay time	trWD	78		90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	trPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	trPWC	81		90		105		110		ns	
\bar{RAS} pulse width (Fast Page Mode)	trASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	trCPA		35		40		45		50	ns	3
\bar{OE} access time	trOEA		18		20		25		25	ns	
\bar{OE} to data delay	trOED	18		20		25		25		ns	
\bar{OE} command hold time	trOEH	18		20		25		25		ns	

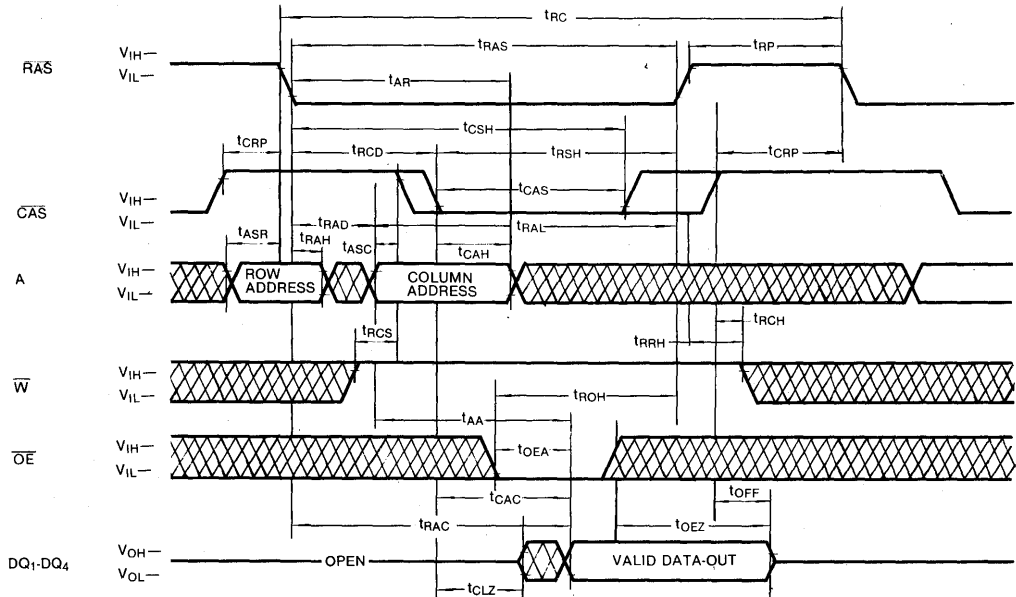
5

NOTES

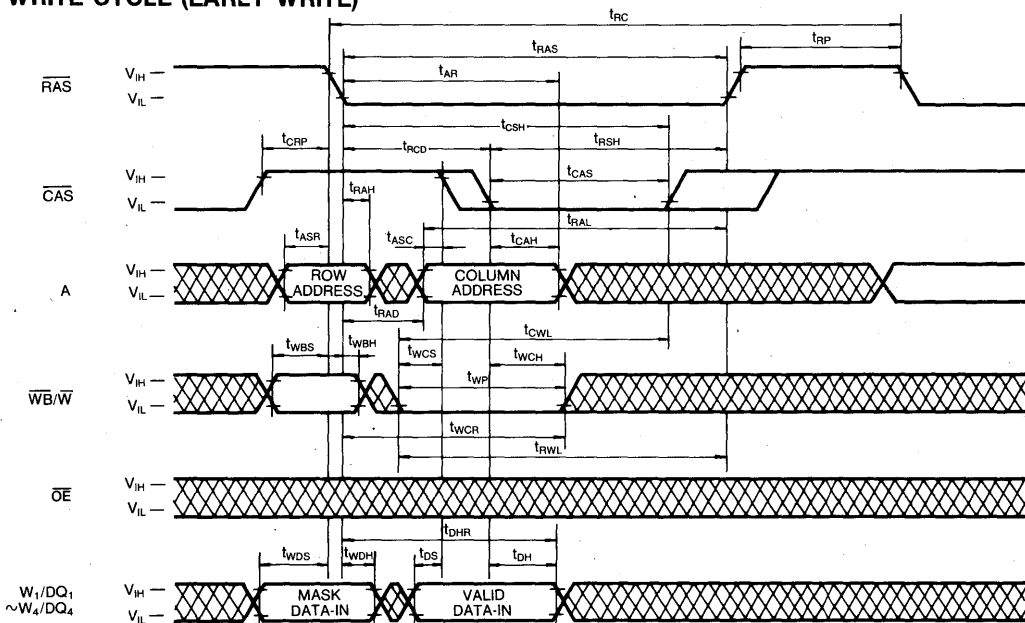
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)

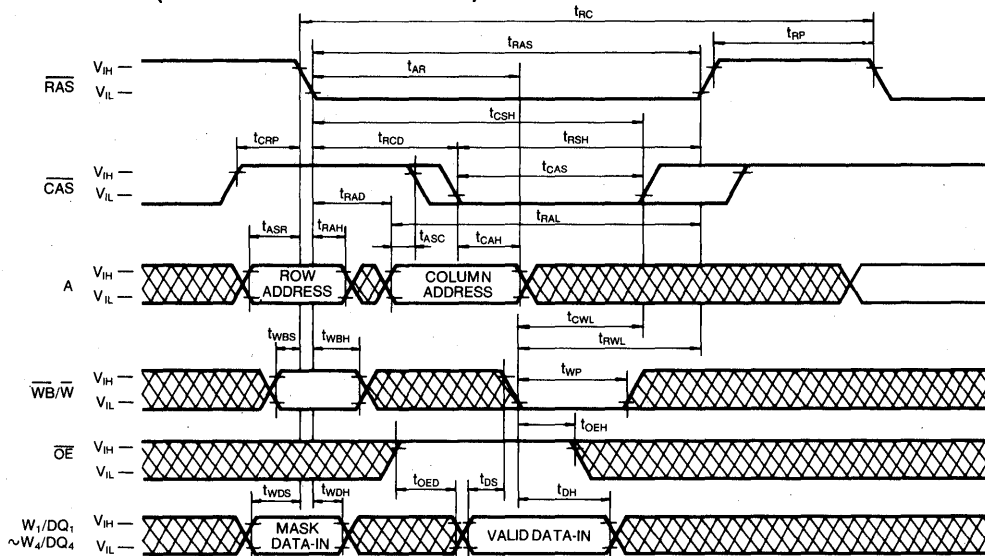


DON'T CARE

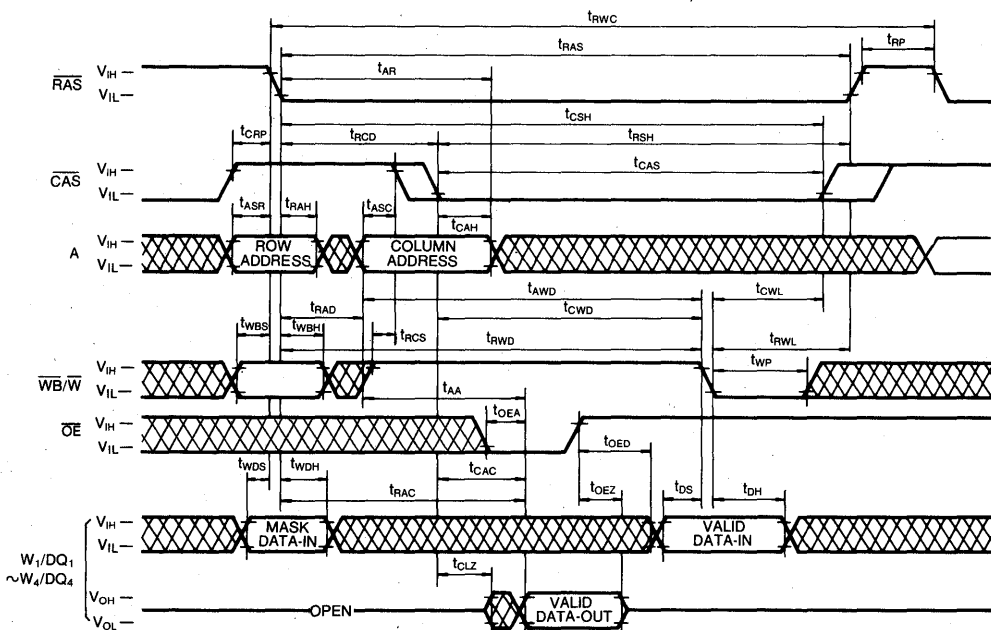
5

TIMING DIAGRAMS (Continued)

WRITE CYCLE (OE CONTROLLED WRITE)



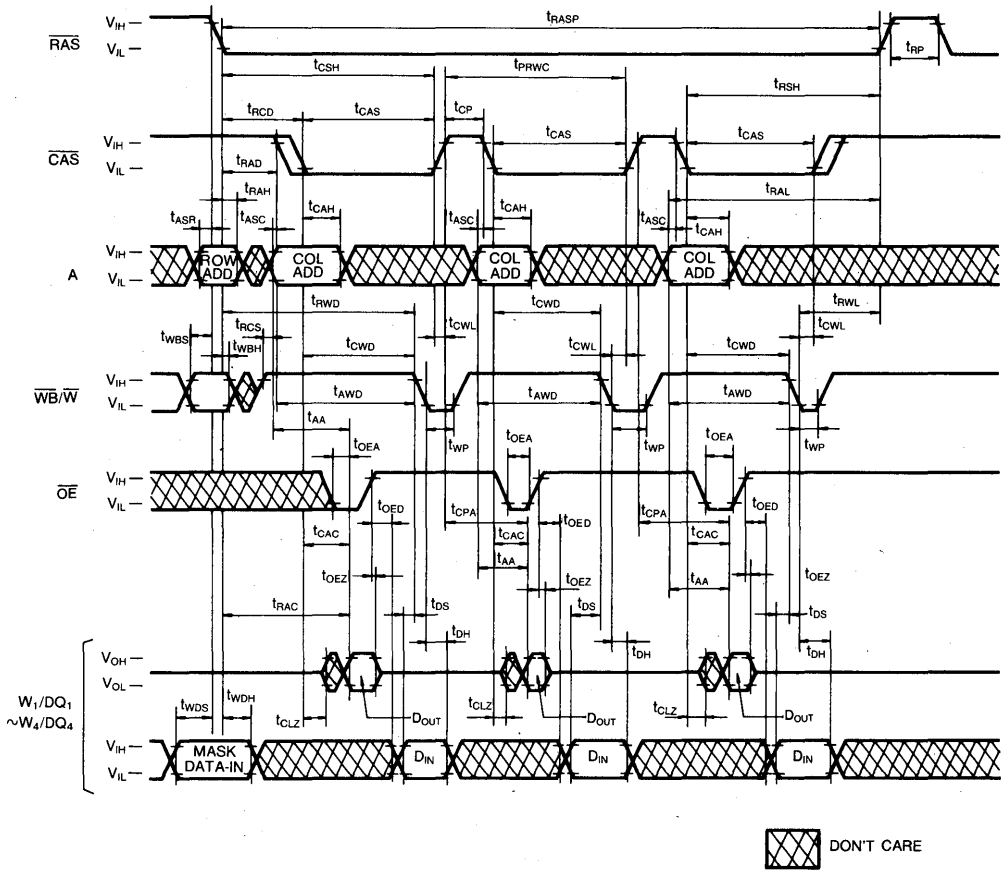
READ-MODIFY-WRITE CYCLE



 DON'T CARE

TIMING DIAGRAMS (Continued)

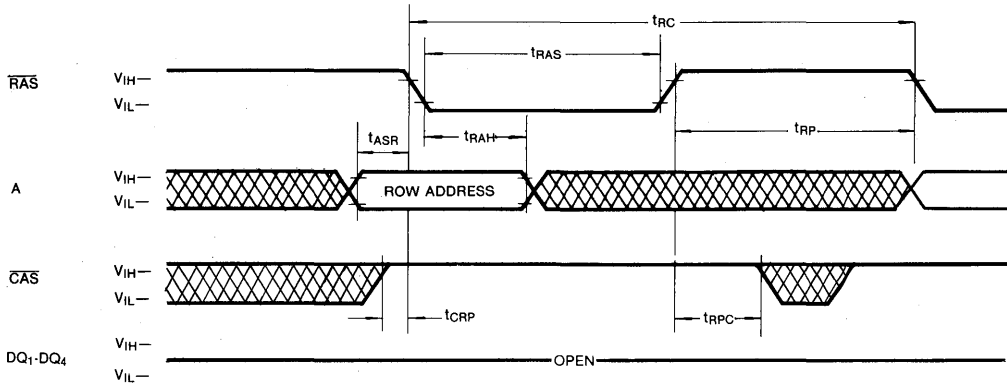
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

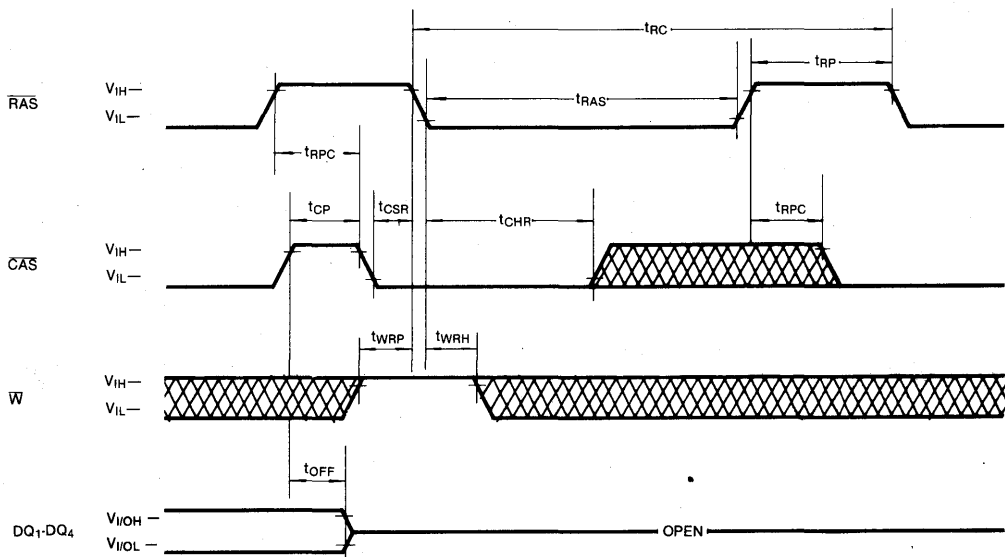
$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE

Note: $\overline{\text{W}}$, $\overline{\text{OE}}$ = Don't Care



$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH CYCLE

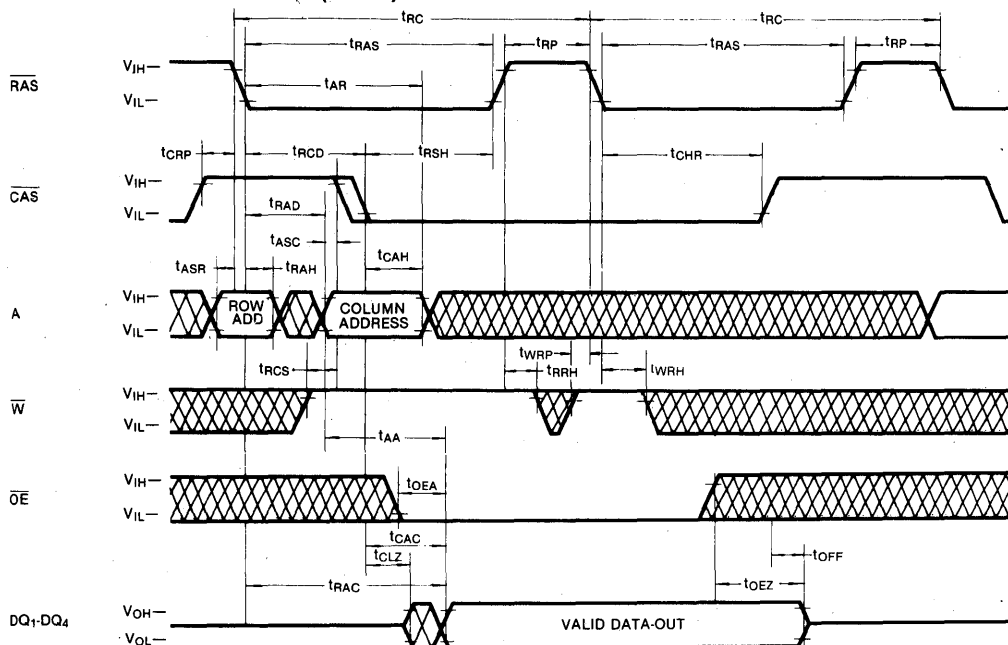
NOTE: $\overline{\text{OE}}$, Address = Don't Care



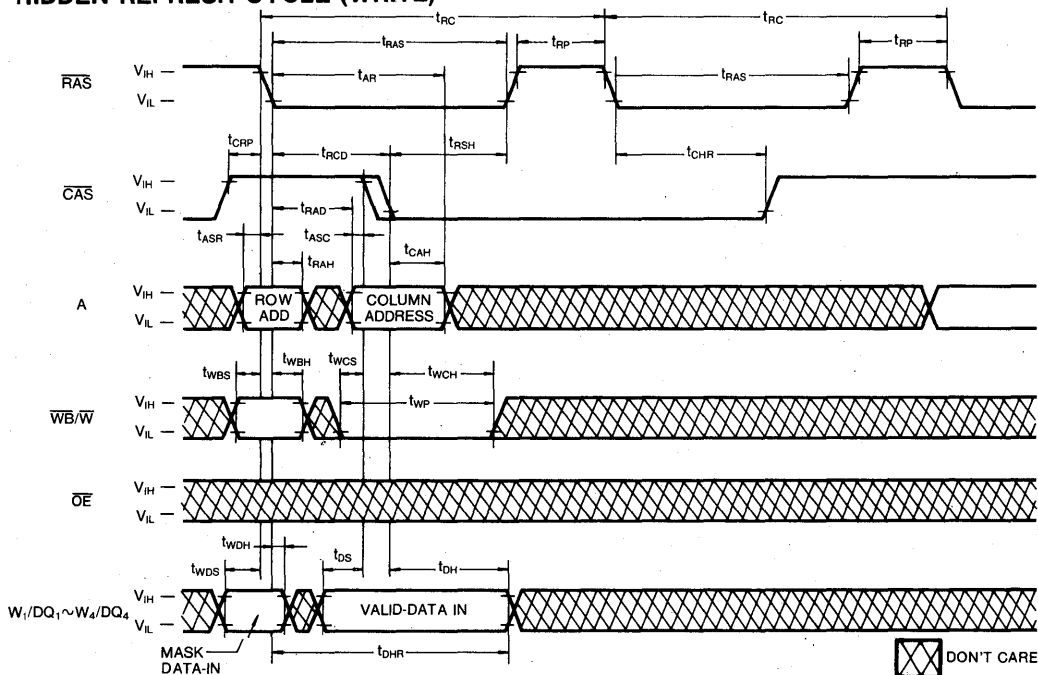
 DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

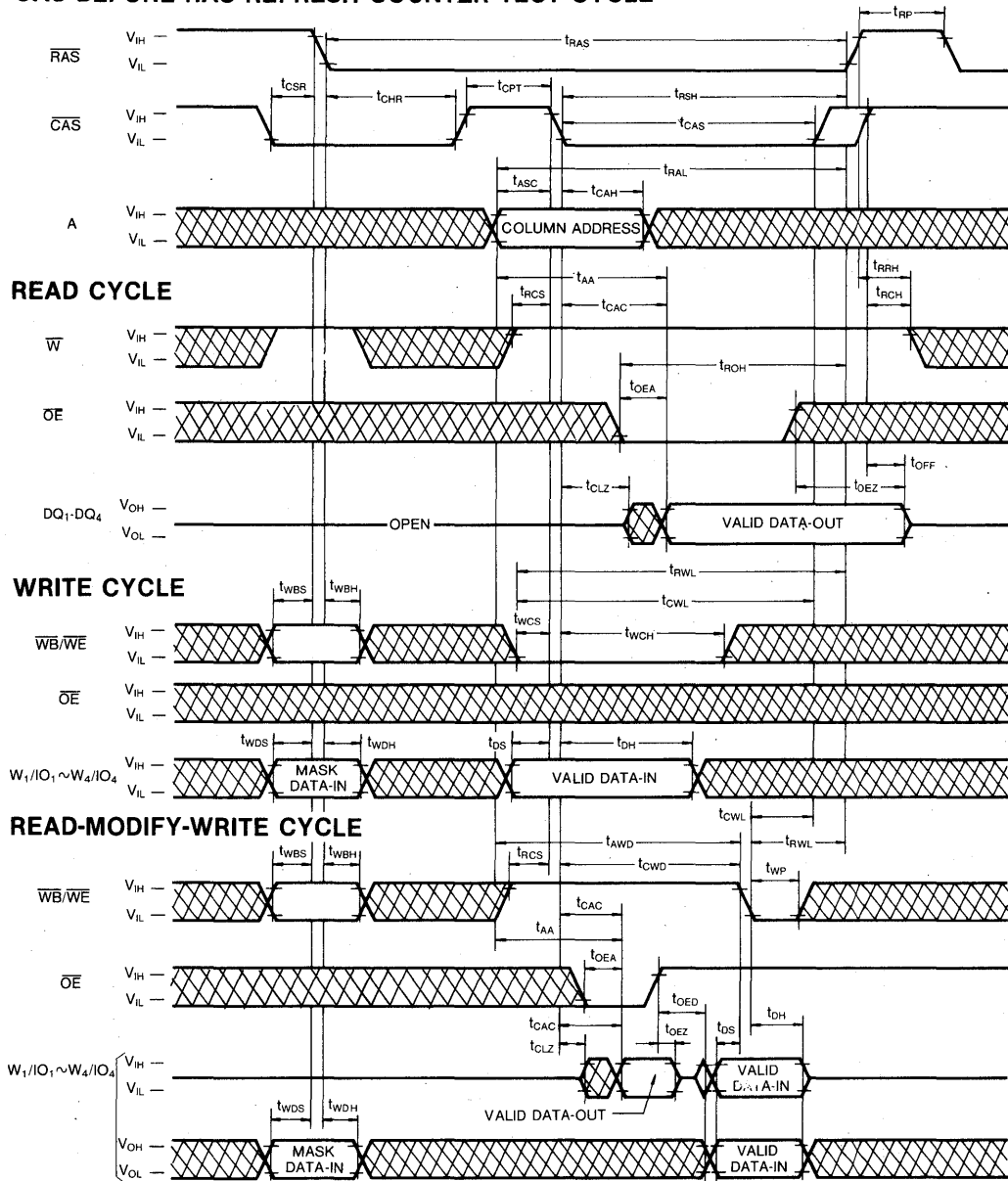


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

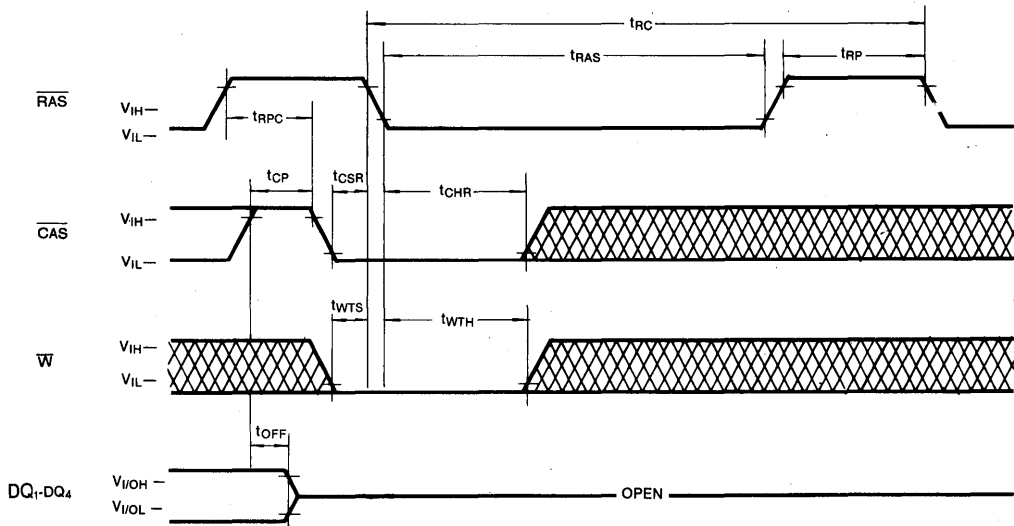


DON'T CARE

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

NOTE: \overline{OE} , Address=Don't Care



 DON'T CARE

TEST MODE DESCRIPTION

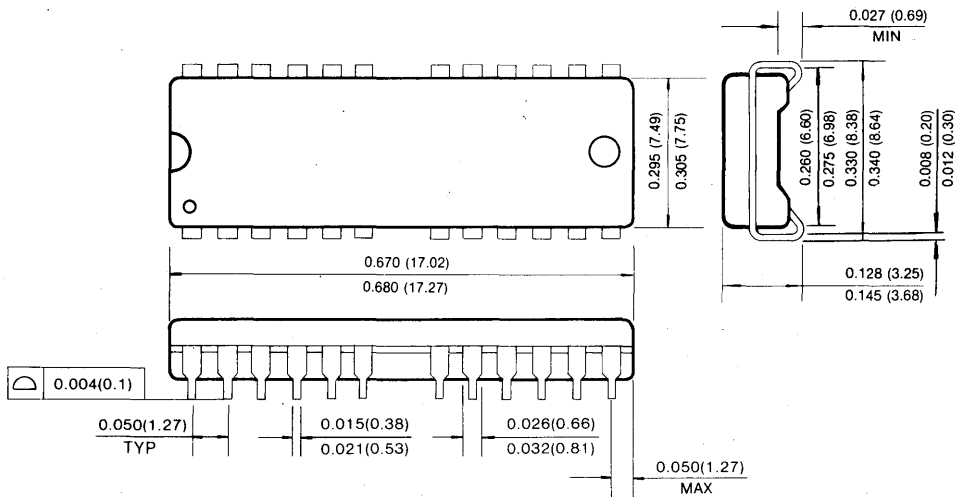
The KM44C4110 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 and A1 are not used. If, upon reading, four bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would

indicate a "0". In "Test Mode" the 4M×4 DRAM can be tested as if it were a 1M×4 DRAM. \overline{W} , \overline{CAS} -Before-RAS Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " \overline{CAS} -Before- \overline{RAS} Refresh Cycle" or "RAS only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

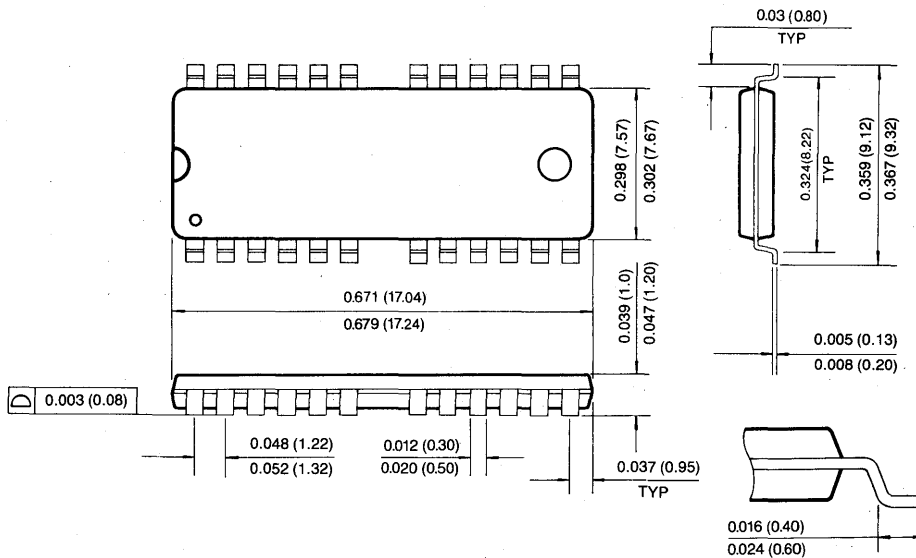
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

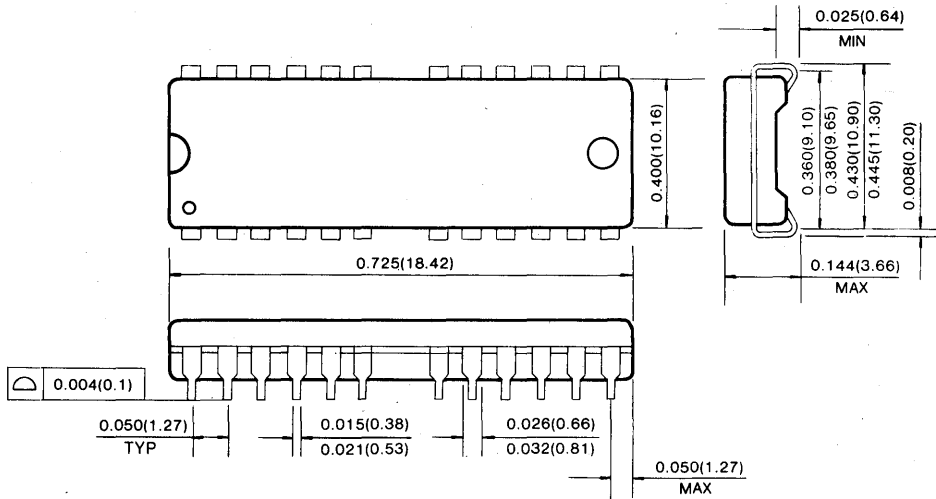


5

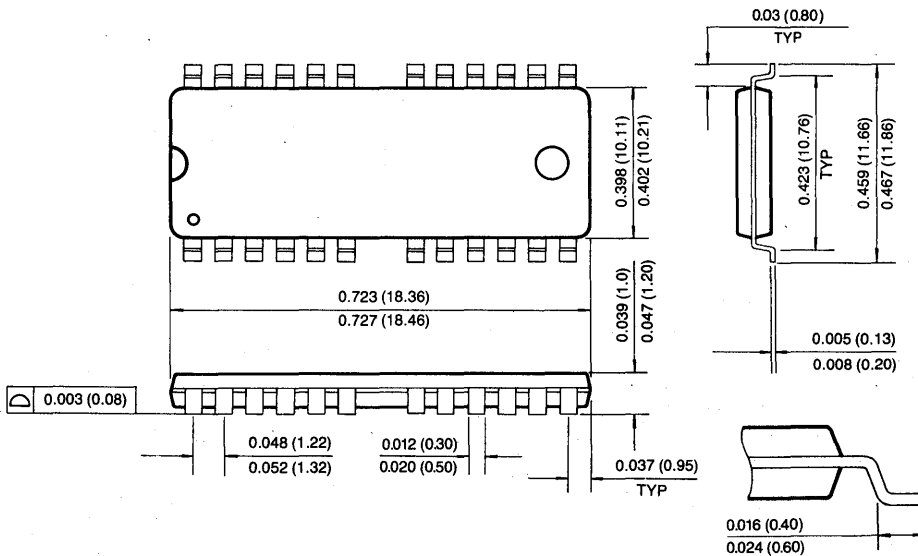
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM44C4002A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4002A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4002A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4002A/AL/ALL/ASL-8	80ns	20ns	150ns

- Static Column Mode operation
- Self Refresh Operation (LL-ver, only)
- CS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

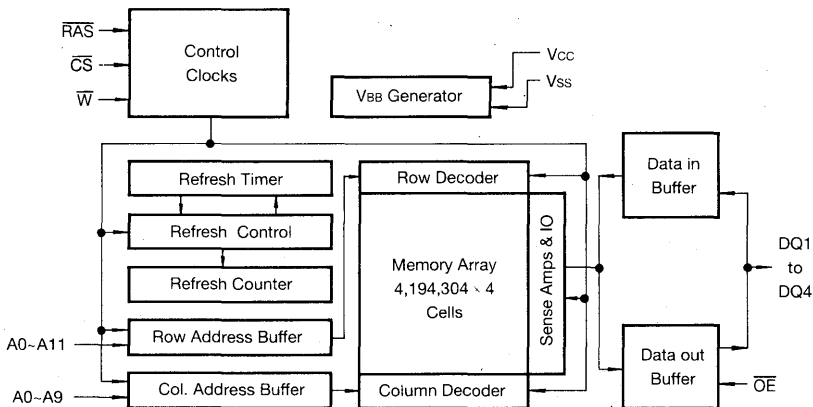
The Samsung KM44C4002A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4002A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

CS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

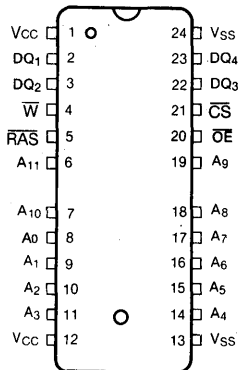
The KM44C4002A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



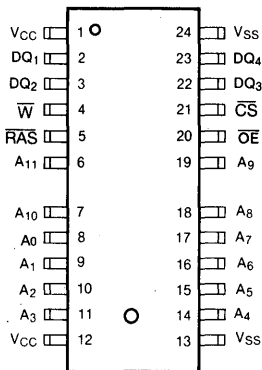
PIN CONFIGURATION (Top Views)

• KM44C4002 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



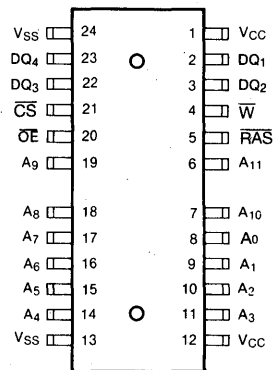
J : 400MIL
K : 300MIL

• KM44C4002 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4002 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CS	Chip Select input
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* (\overline{RAS} and \overline{CS} Cycling @ $t_{RC}=\text{min.}$)	KM44C4002A/AL/ALL/ASL-5	I _{CC1}	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{RAS}=\overline{CS}=\overline{W}=V_{IH}$)	KM44C4002A	I _{CC2}	-	2	mA
	KM44C4002AL			1	mA
	KM44C4002ALL			1	mA
	KM44C4002ASL			1	mA
\overline{RAS} -Only Refresh Current* ($\overline{CS}=V_{IH}$, \overline{RAS} Cycling @ $t_{RC}=\text{min.}$)	KM44C4002A/AL/ALL/ASL-5	I _{CC3}	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CS} , Address Cycling @ $t_{PC}=\text{min.}$)	KM44C4002A/AL/ALL/ASL-5	I _{CC4}	-	80	mA
	KM44C4002A/AL/ALL/ASL-6			70	mA
	KM44C4002A/AL/ALL/ASL-7			60	mA
	KM44C4002A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{RAS}=\overline{CS}=\overline{W}=V_{CC}-0.2V$)	KM44C4002A	I _{CC5}	-	1	mA
	KM44C4002AL			300	μA
	KM44C4002ALL			200	μA
	KM44C4002ASL			200	μA
\overline{CS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CS} Cycling @ $t_{RC}=\text{min.}$)	KM44C4002A/AL/ALL/ASL-5	I _{CC6}	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{CS}=\overline{CS}$ -Before- \overline{RAS} Cycling or 0.2V DQ1~DQ4=Don't Care $t_{RC}=31.25\mu s(L-Ver.)$ 62.5μs(SL-Ver), $t_{RAS}=\text{RAS min}\sim 300ns$	KM44C4002AL	I _{CC7}	-	450	μA
	KM44C4002ASL			350	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CS=0.2V W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)	IoL	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one Static Column cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A11)	CIN1	-	5	pF
Input Capacitance (RAS, CS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CS hold time	tCSH	50		60		70		80		ns	
CS pulse width	tCS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CS to RAS precharge time	trCP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CS}}$ lead time	tcWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		50		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	tcWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CS}}$ set-up time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CS}}$ hold time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CS}}$ precharge time ($\overline{\text{C}}$ -B-R counter test cycle)	tcPT	20		20		30		30		ns	
Static column mode cycle time	tSC	30		35		40		45		ns	3
Static column mode read-write cycle time	tSRWC	80		85		100		110		ns	
Access time from last write	tALW		50		55		65		75	ns	3, 12
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{\text{W}}$	tOW		35		40		45		55	ns	
$\overline{\text{RAS}}$ pulse width (Static column mode)	tRASC	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{CS}}$ pulse width (Static column mode)	tcSC	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{\text{CS}}$ precharge time (Static column mode)	tcP	10		10		10		10		ns	
Column address hold time referenced to $\overline{\text{RAS}}$ rising	tAH	5		5		5		5		ns	
Last write to column address delay time	tLWAD	20	25	20	25	25	30	25	35	ns	
Last write to column address hold time	tAHLW	50		55		65		75		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command inactive time	tWI	10		10		10		10		ns	
RAS hold time referenced to OE	tROH	13		15		20		20		ns	
Write address hold time referenced to RAS	tAWR	40		45		55		60		ns	6
OE access time	tOEA		13		15		20		20	ns	
OE to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from OE	tOEZ	0	13	0	15	0	20	0	20	ns	
OE command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
W to RAS precharge time (C-B-R refresh)	tWRP	10		10		10		10		ns	
W to RAS hold time (C-B-R refresh)	tWRH	10		10		10		10		ns	
RAS pulse width (C-B-R self refresh)	tRASS	100		100		100		100		μs	15
RAS precharge time (C-B-R self refresh)	tRPS	90		110		130		150		ns	15
CS hold time (C-B-R self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

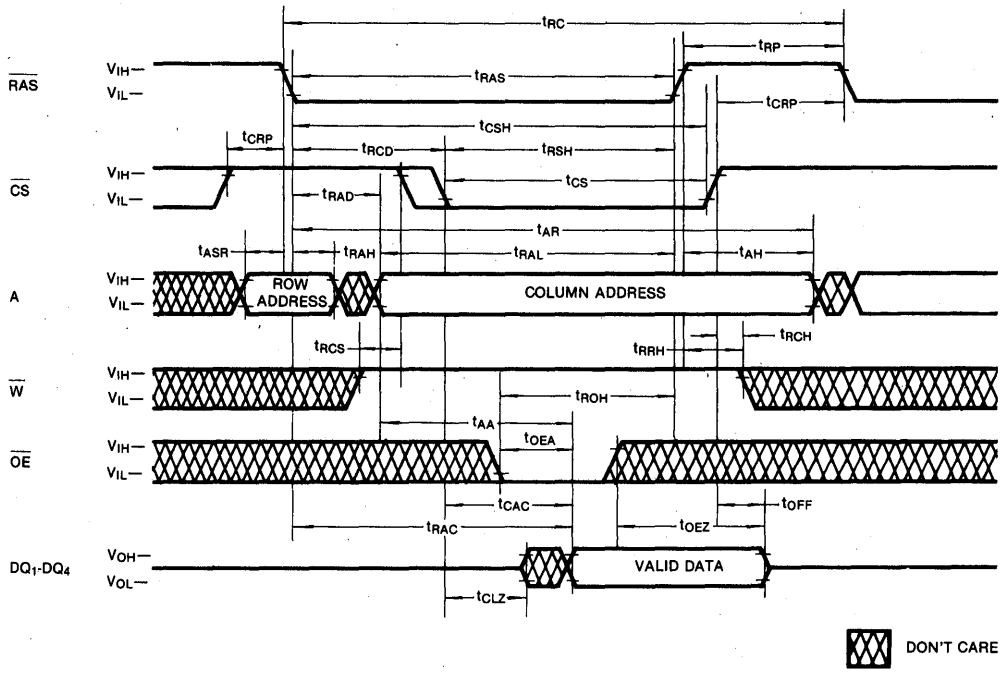
(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	140		160		190		210		ns	
Access time from RAS	tRAC		55		65		75		85	ns	3,4,11
Access time from CS	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
RAS pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
CS pulse width	tCS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	tRSH	20		20		25		25		ns	
CS hold time	tCSH	55		65		75		85		ns	
Column address to RAS lead time	tRAL	30		35		40		45		ns	
CS to W delay time	tCWD	45		45		55		55		ns	8
RAS to W delay time	tRWD	80		90		105		115		ns	8
Column address to W delay time	tAWD	55		60		70		75		ns	8
Static column mode cycle time	tSC	35		40		45		50		ns	
Static column mode read-write cycle time	tSRWC	85		90		105		110		ns	
RAS pulse width (Static column mode)	tRASC	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	tALW		55		60		70		80	ns	3,12
OE access time	tOEA		18		20		25		25	ns	
OE to data delay	tOED	18		20		25		25		ns	
OE command hold time	tOEH	18		20		25		25		ns	

NOTES

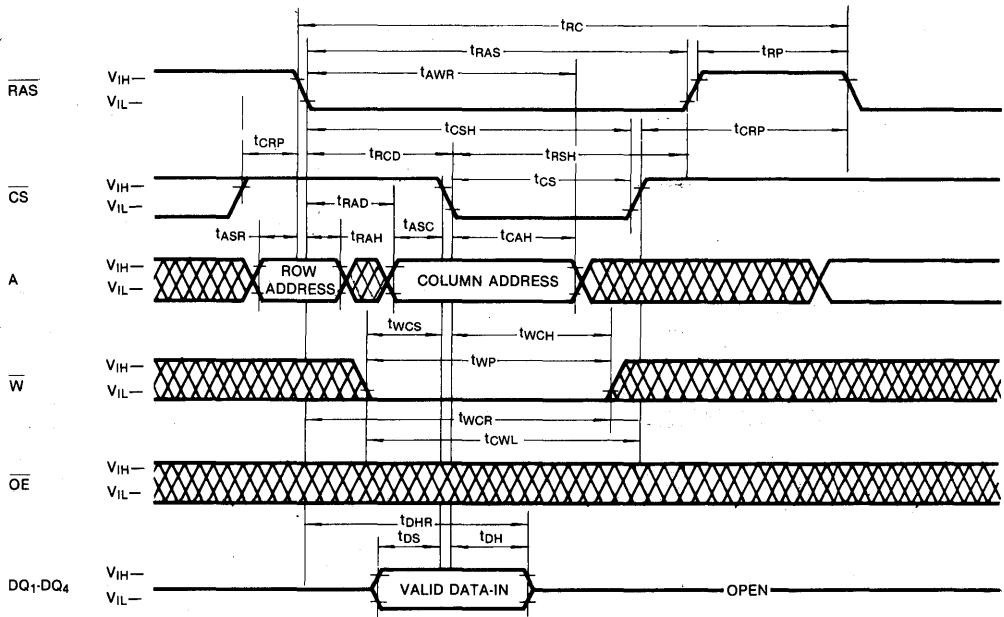
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS
READ CYCLE

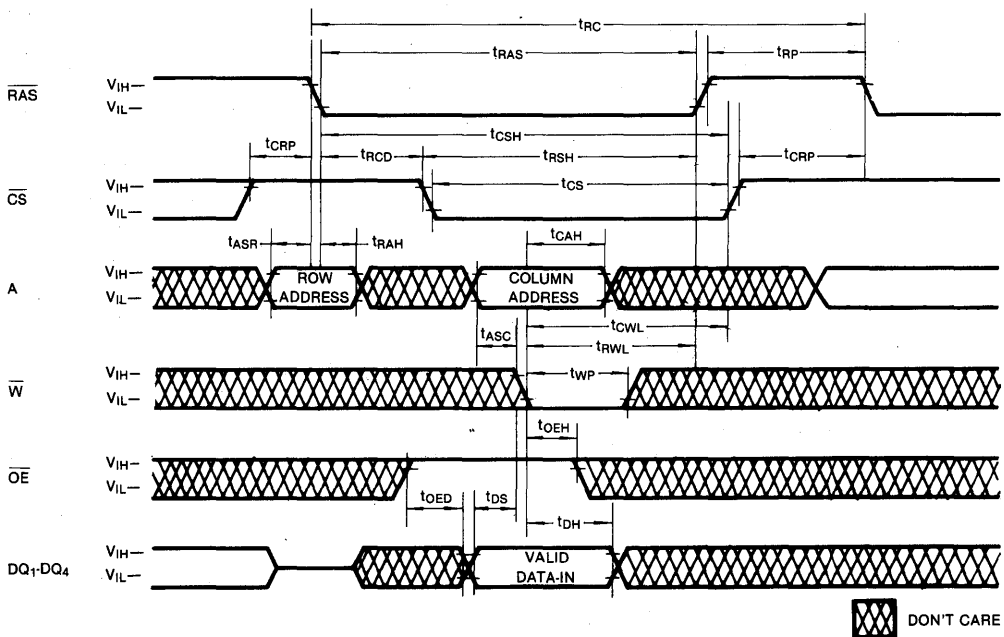


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



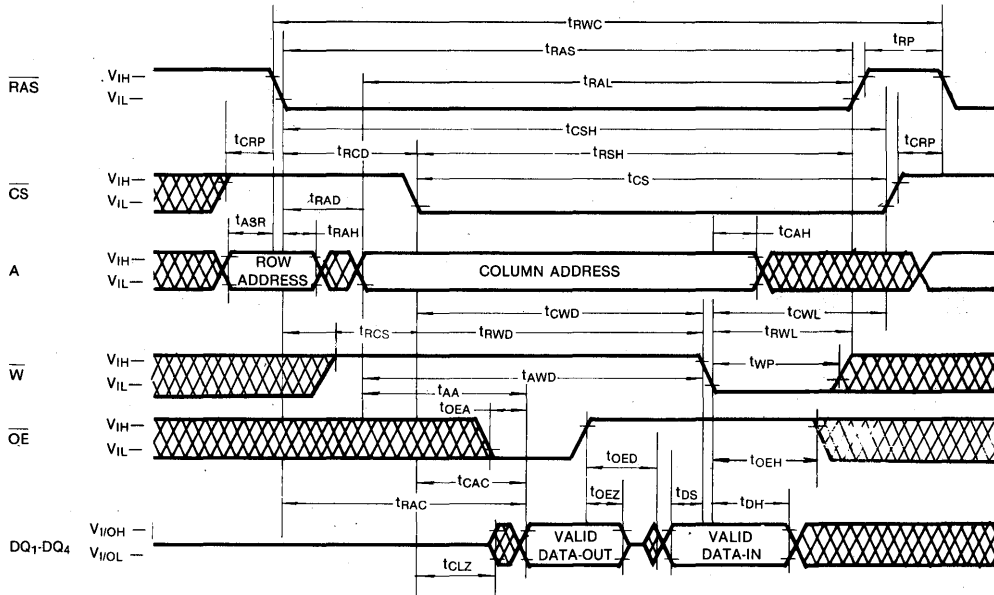
WRITE CYCLE (OE CONTROLLED WRITE)



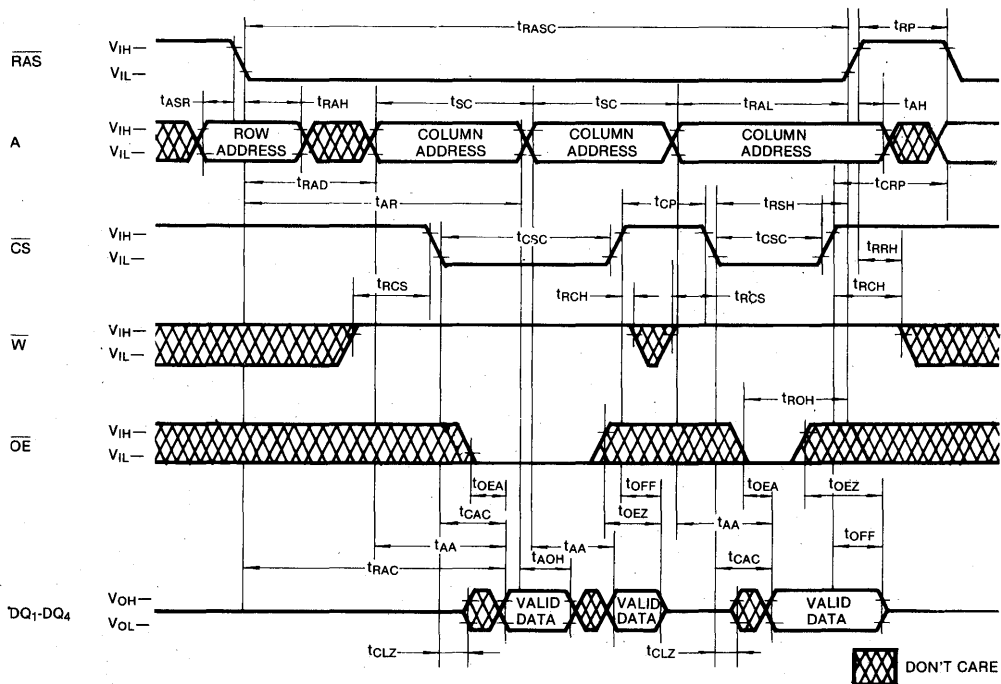
 DON'T CARE

5

TIMING DIAGRAMS (Continued)
READ-WRITE/READ-MODIFY-WRITE CYCLE

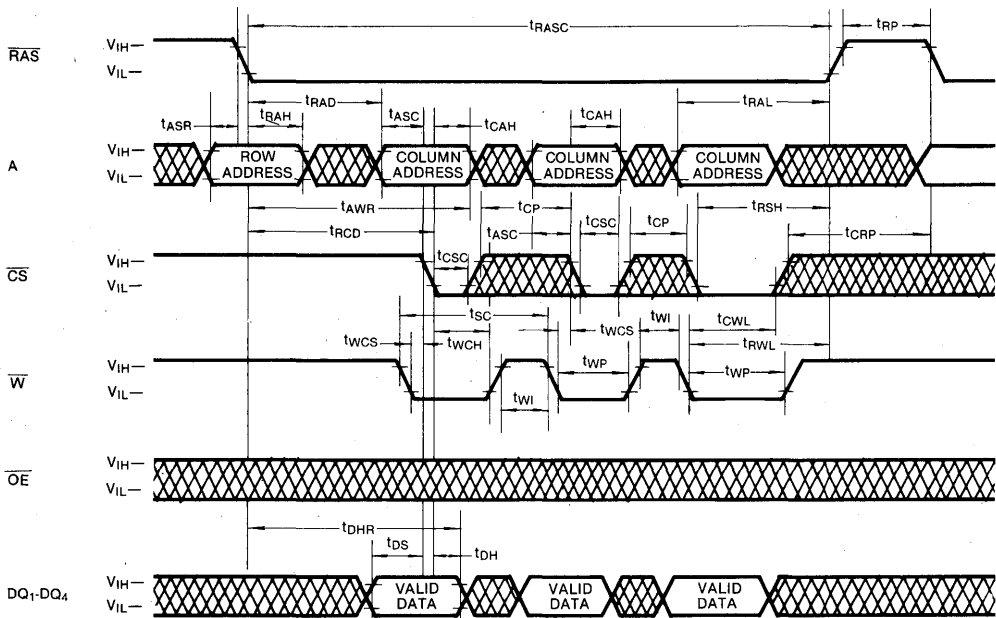


STATIC COLUMN MODE READ CYCLE

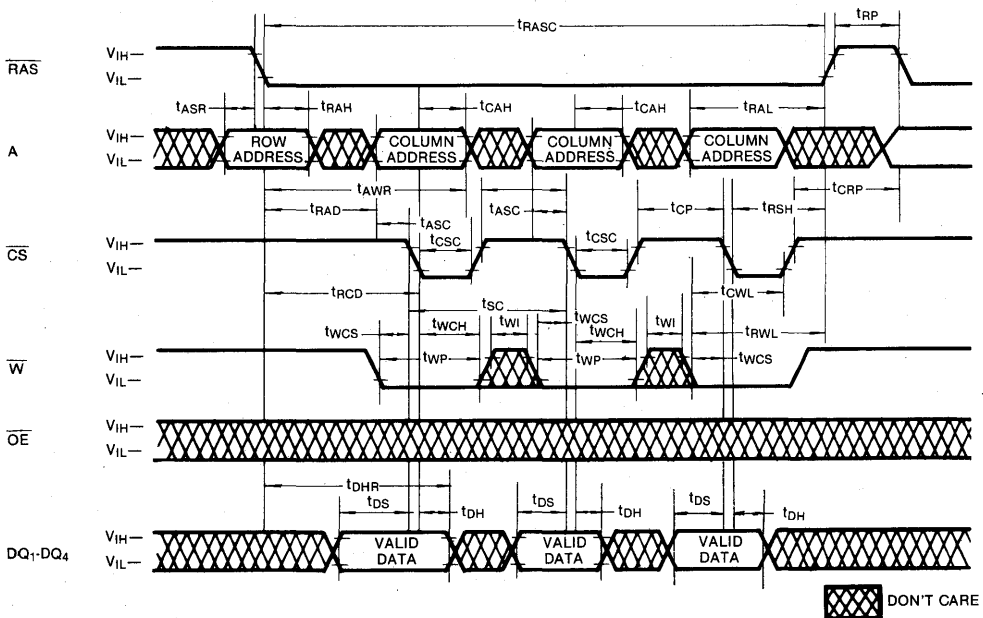


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE (\overline{W} controlled early write)



STATIC COLUMN MODE WRITE CYCLE (\overline{CS} controlled early write)

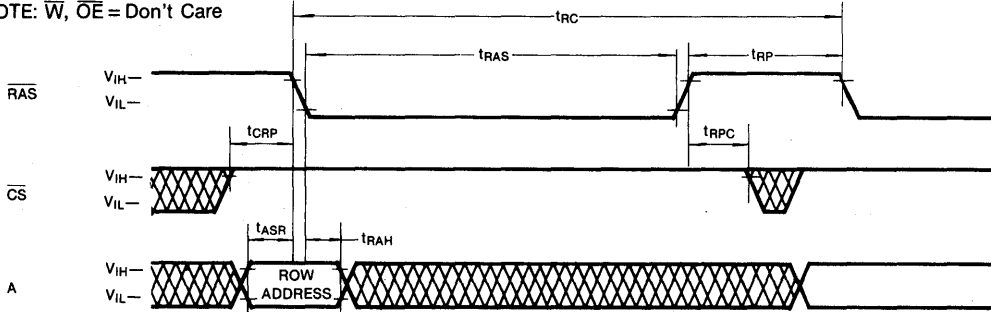


DON'T CARE

TIMING DIAGRAMS (Continued)

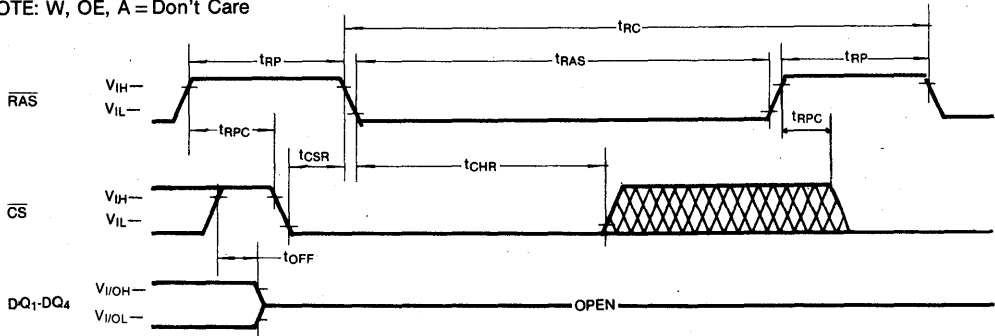
RAS-ONLY REFRESH CYCLE

NOTE: \overline{W} , \overline{OE} = Don't Care



CS-BEFORE-RAS REFRESH CYCLE

NOTE: \overline{W} , \overline{OE} , A = Don't Care

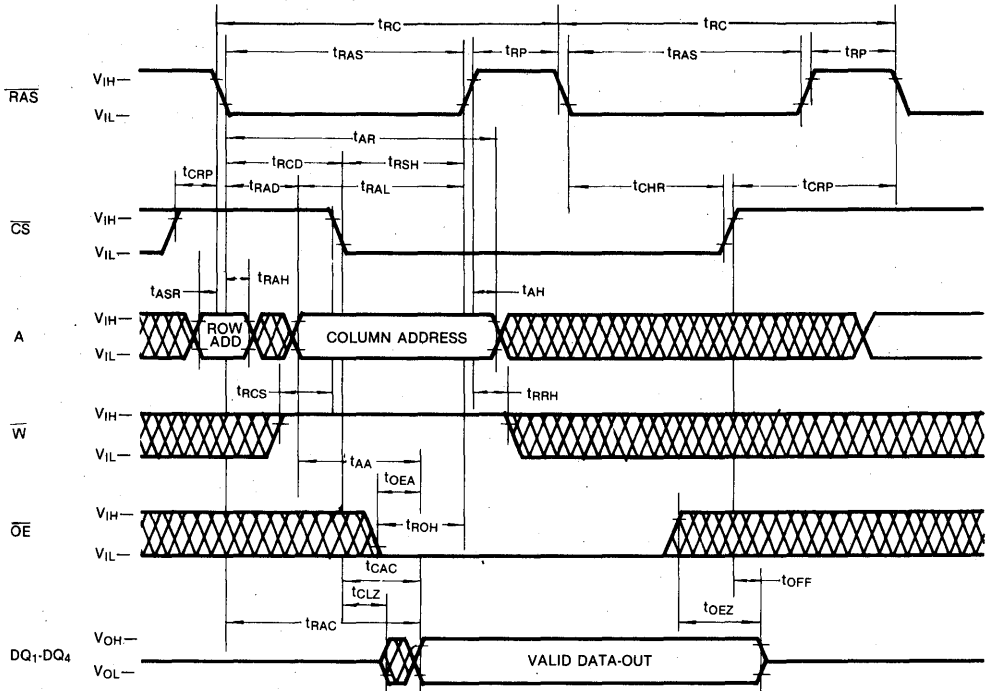


 DON'T CARE

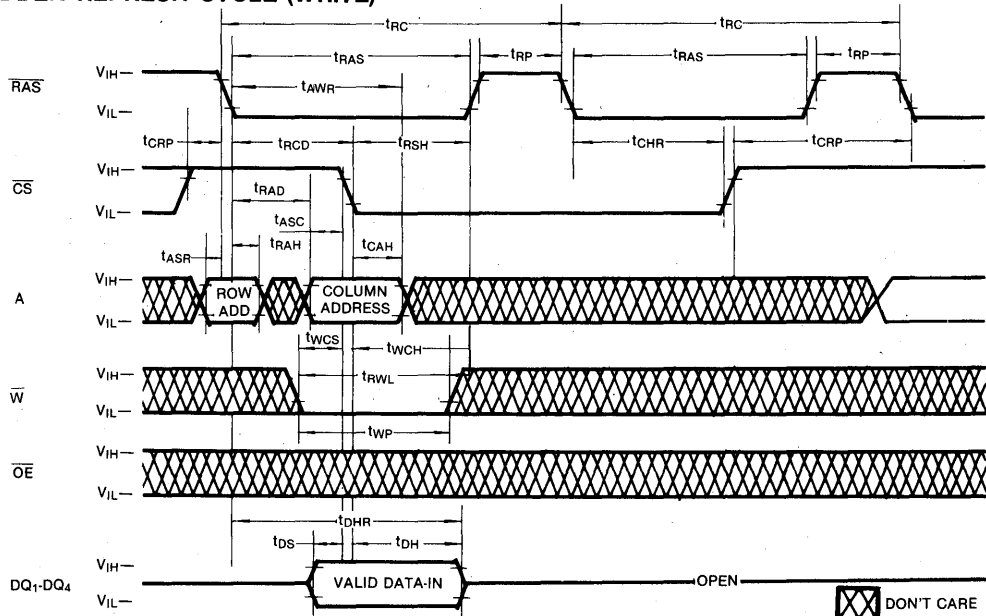
5

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



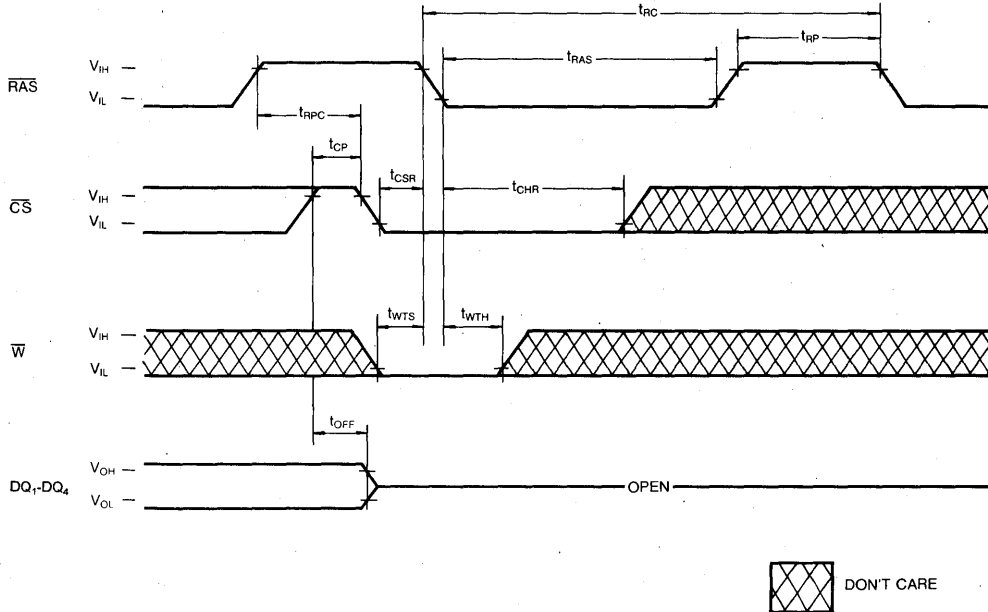
HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



TEST MODE DESCRIPTION

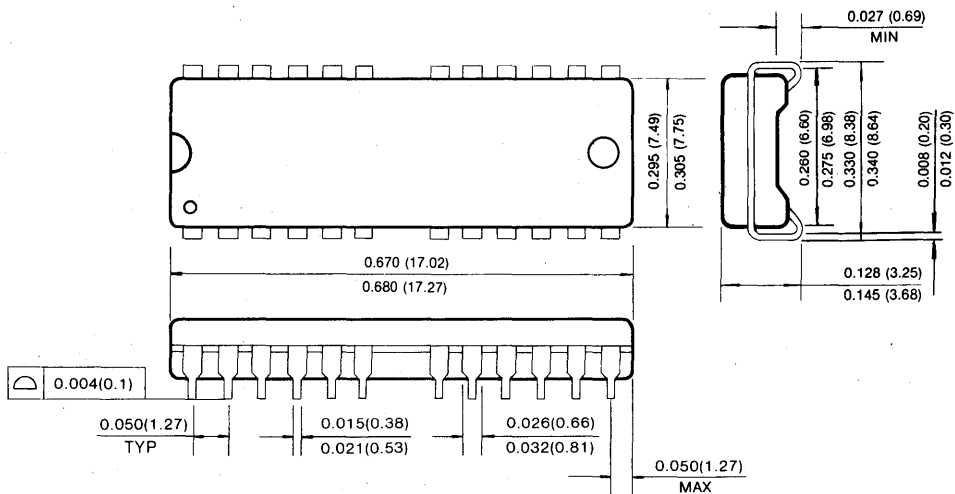
The KM44C4002 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1 , are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1". If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a $1M \times 4$ DRAM. $\overline{W}, \overline{CS}$ -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And \overline{CS} -BEFORE- \overline{RAS} REFRESH CYCLE "or" \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

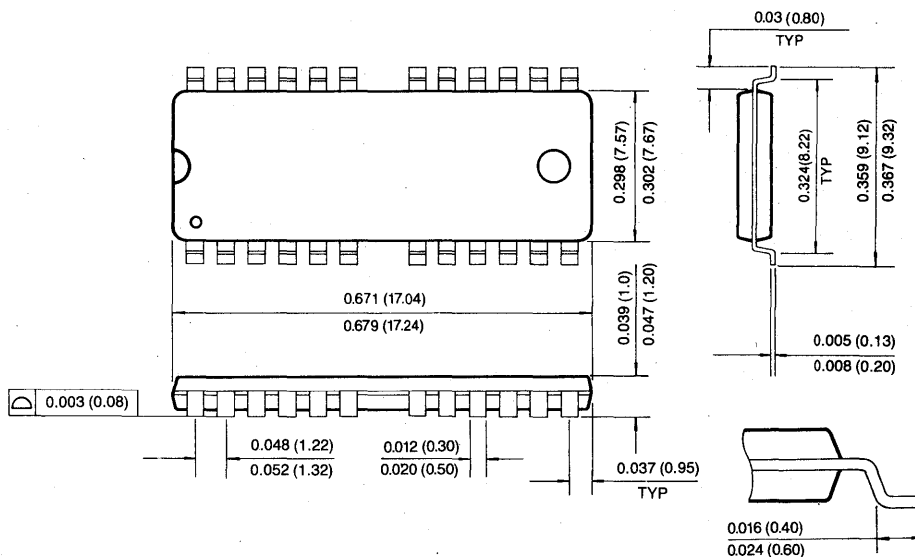
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



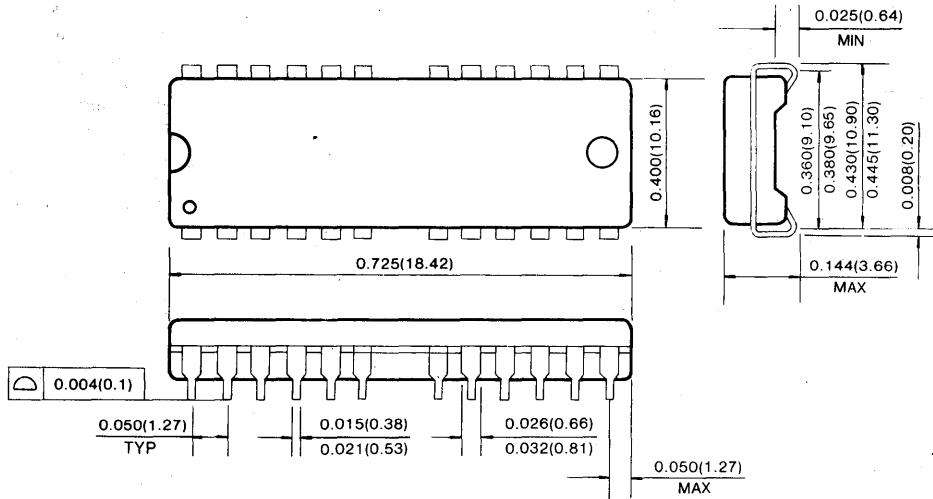
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



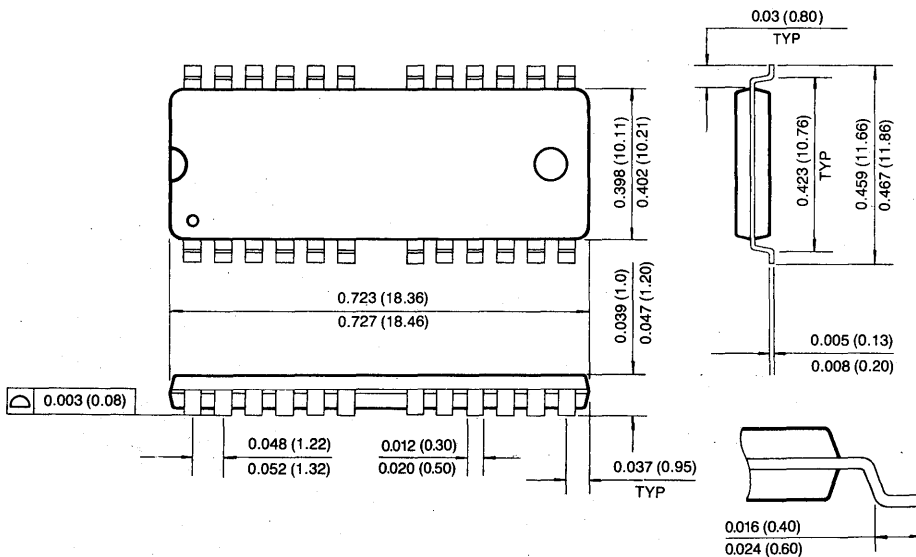
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M x 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• Performance range:

	t _{RAC}	t _{CAC}	t _{RC}
KM44C4102A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4102A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4102A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4102A/AL/ALL/ASL-8	80ns	20ns	150ns

- Self Refresh Operation (LL-ver. only)
- Static Column Mode operation
- CS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(III)

GENERAL DESCRIPTION

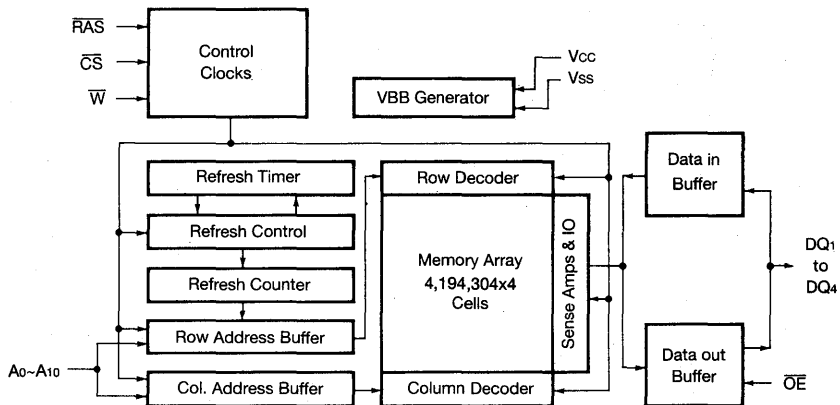
The Samsung KM44C4102A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4102A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

CS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

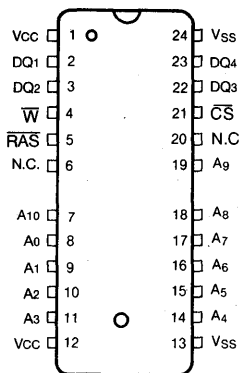
The KM44C4102A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



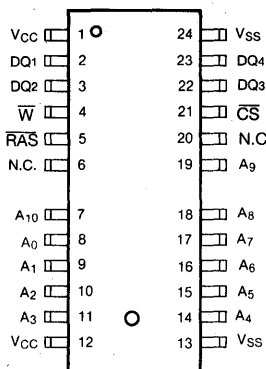
PIN CONFIGURATION (Top Views)

• KM44C4102 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



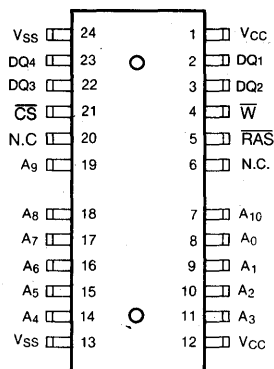
J : 400MIL
K : 300MIL

• KM44C4102 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4102 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CS}}$	Chip Select input
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CS Cycling @trc=min.)	KM44C4102A/AL/ALL/ASL-5	I _{CC1}	-	110	mA
	KM44C4102A/AL/ALL/ASL-6			100	mA
	KM44C4102A/AL/ALL/ASL-7			90	mA
	KM44C4102A/AL/ALL/ASL-8			80	mA
Standby Current (RAS=CS=W=V _{IH})	KM44C4102A	I _{CC2}	-	2	mA
	KM44C4102AL			1	mA
	KM44C4102ALL			1	mA
	KM44C4102ASL			1	mA
RAS-Only Refresh Current* (CS=V _{IH} , RAS Cycling @trc=min.)	KM44C4102A/AL/ALL/ASL-5	I _{CC3}	-	110	mA
	KM44C4102A/AL/ALL/ASL-6			100	mA
	KM44C4102A/AL/ALL/ASL-7			90	mA
	KM44C4102A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* (RAS=V _{IL} , CS, Address Cycling @tpc=min.)	KM44C4102A/AL/ALL/ASL-5	I _{CC4}	-	90	mA
	KM44C4102A/AL/ALL/ASL-6			80	mA
	KM44C4102A/AL/ALL/ASL-7			70	mA
	KM44C4102A/AL/ALL/ASL-8			60	mA
Standby Current (RAS=CS=W=V _{CC} -0.2V)	KM44C4102A	I _{CC5}	-	1	mA
	KM44C4102AL			300	μA
	KM44C4102ALL			200	μA
	KM44C4102ASL			200	μA
CS-Before-RAS Refresh Current* (RAS and CS Cycling @trc=min.)	KM44C4102A/AL/ALL/ASL-5	I _{CC6}	-	110	mA
	KM44C4102A/AL/ALL/ASL-6			100	mA
	KM44C4102A/AL/ALL/ASL-7			90	mA
	KM44C4102A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CS=CS-Before-RAS Cycling or 0.2V DQ1-DQ4=Don't Care trc=62.5μs(L-Ver.) 125μs(SL-Ver.), tRAS=tRAS min-300ns	KM44C4102AL KM44C4102ASL	I _{CC7}	-	400 300	μA μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CS=0.2V W=OE=A0-A10=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ Vin ≤ Vcc+0.5V, all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ 5.5V)	IOL	-10	10	μA
Output High Voltage Level (Ioh=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (Iol=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one Static Column cycle.

CAPACITANCE (TA=25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A10)	CIN1	-	5	pF
Input Capacitance (RAS, CS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tt	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CS hold time	tCSH	50		60		70		80		ns	
CS pulse width	tCS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CS}}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		50		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CS}}$ set-up time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CS}}$ hold time ($\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CS}}$ precharge time ($\overline{\text{C-B-F}}$ counter test cycle)	tCPT	20		20		30		30		ns	
Static column mode cycle time	tSC	30		35		40		45		ns	3
Static column mode read-write cycle time	tSRWC	80		85		100		110		ns	
Access time from last write	tALW		50		55		65		75	ns	3, 12
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{\text{W}}$	tOW		35		40		45		55	ns	
$\overline{\text{RAS}}$ pulse width (Static column mode)	tRASC	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{CS}}$ pulse width (Static column mode)	tCSC	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{\text{CS}}$ precharge time (Static column mode)	tCP	10		10		10		10		ns	
Column address hold time referenced to $\overline{\text{RAS}}$ rising	tAH	5		5		5		5		ns	
Last write to column address delay time	tLWAD	20	25	20	25	25	30	25	35	ns	
Last write to column address hold time	tAHLW	50		55		65		75		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command inactive time	twi	10		10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	tROH	13		15		20		20		ns	
Write address hold time referenced to $\overline{\text{RAS}}$	tAWR	40		45		55		60		ns	6
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRP	10		10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	tWRH	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRASS	100		100		100		100		μs	15
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tRPS	90		110		130		150		ns	15
$\overline{\text{CS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	140		160		190		210		ns	
Access time from $\overline{\text{RAS}}$	tRAC		55		65		75		85	ns	3,4,11
Access time from $\overline{\text{CS}}$	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
$\overline{\text{RAS}}$ pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{\text{CS}}$ pulse width	tCS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{\text{RAS}}$ hold time	tRSH	20		20		25		25		ns	
$\overline{\text{CS}}$ hold time	tCSH	55		65		75		85		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		45		ns	
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	tCWD	45		45		55		55		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	80		90		105		115		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		70		75		ns	8
Static column mode cycle time	tSC	35		40		45		50		ns	
Static column mode read-write cycle time	tSRWC	85		90		105		110		ns	
$\overline{\text{RAS}}$ pulse width (Static column mode)	tRASC	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	tALW		55		60		70		80	ns	3,12
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

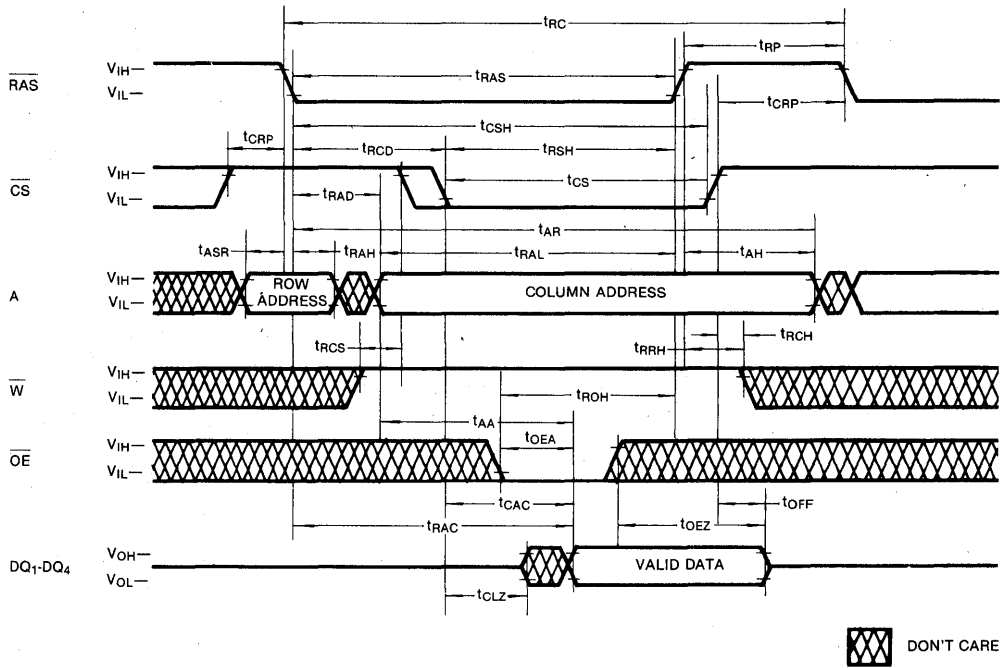


NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

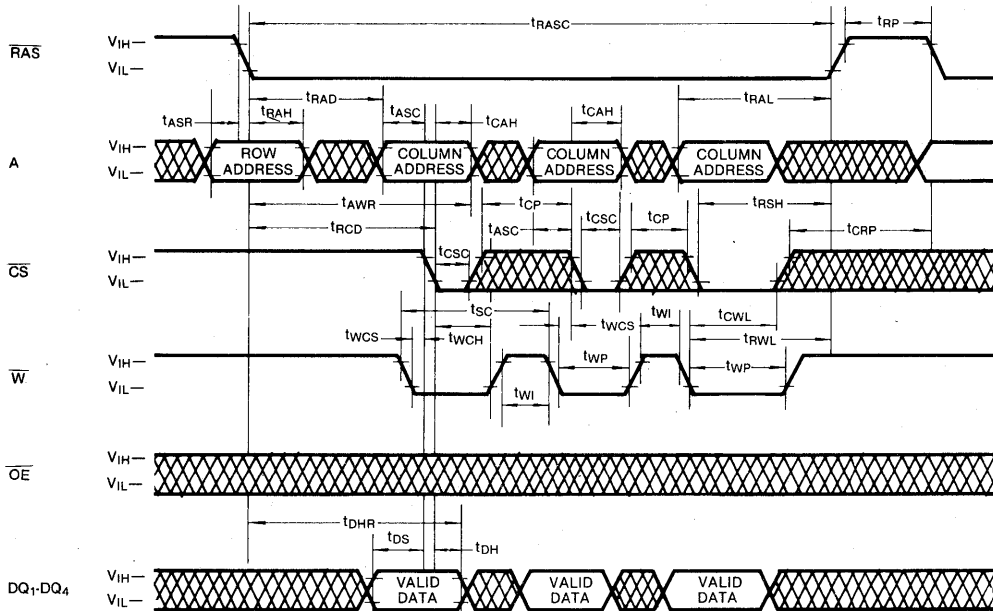
TIMING DIAGRAMS

READ CYCLE

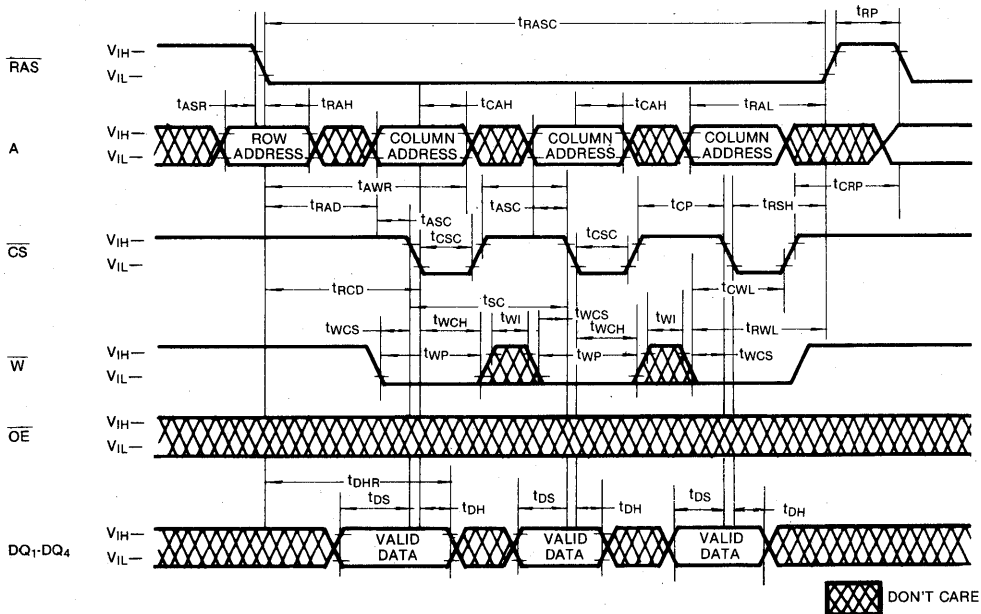


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE WRITE CYCLE (W controlled early write)



STATIC COLUMN MODE WRITE CYCLE (\overline{CS} controlled early write)

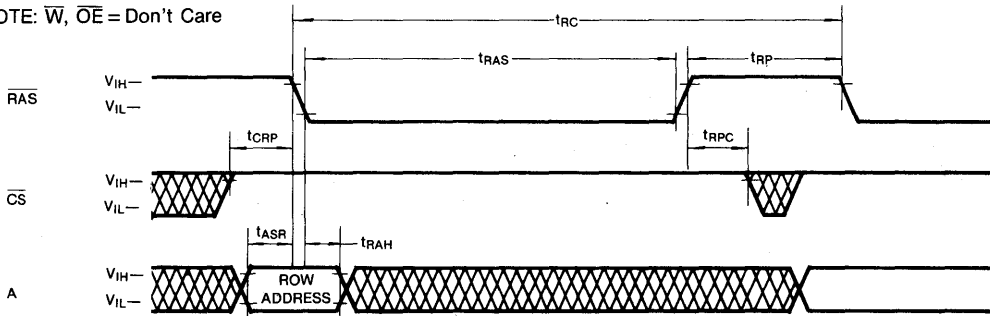


5

TIMING DIAGRAMS (Continued)

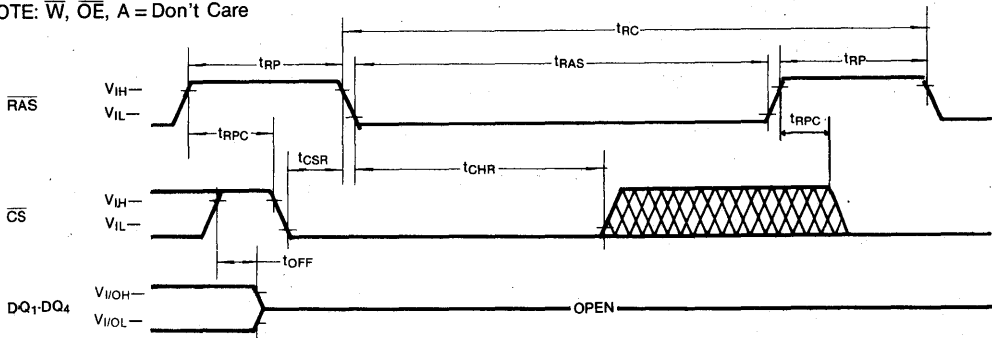
RAS-ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care



\bar{CS} -BEFORE- \bar{RAS} REFRESH CYCLE

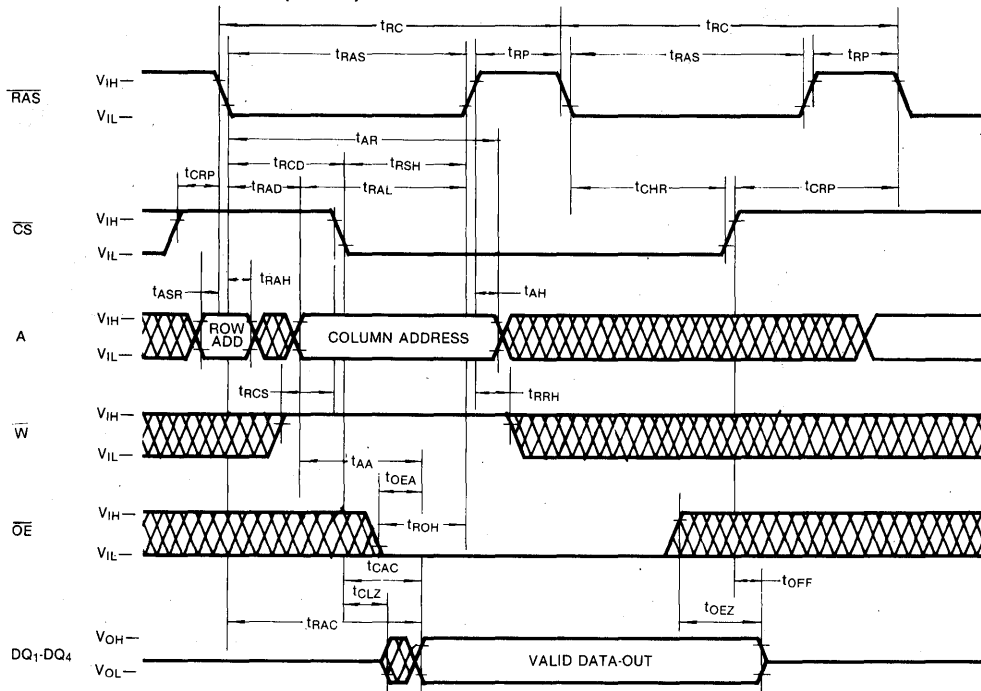
NOTE: \bar{W} , \bar{OE} , A = Don't Care



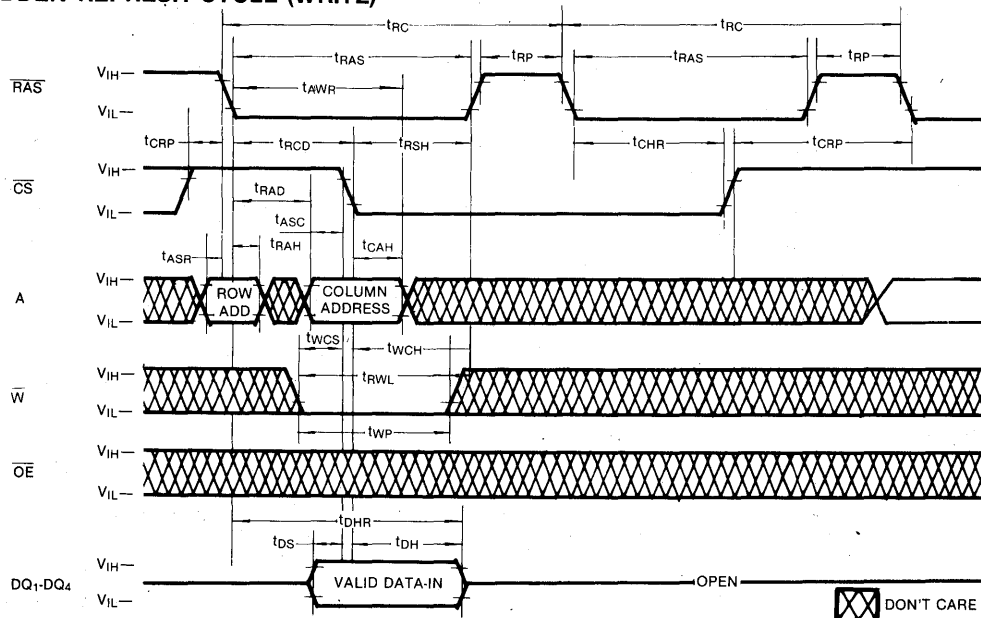
 DON'T CARE

5

TIMING DIAGRAMS (Continued)
HIDDEN REFRESH CYCLE (READ)

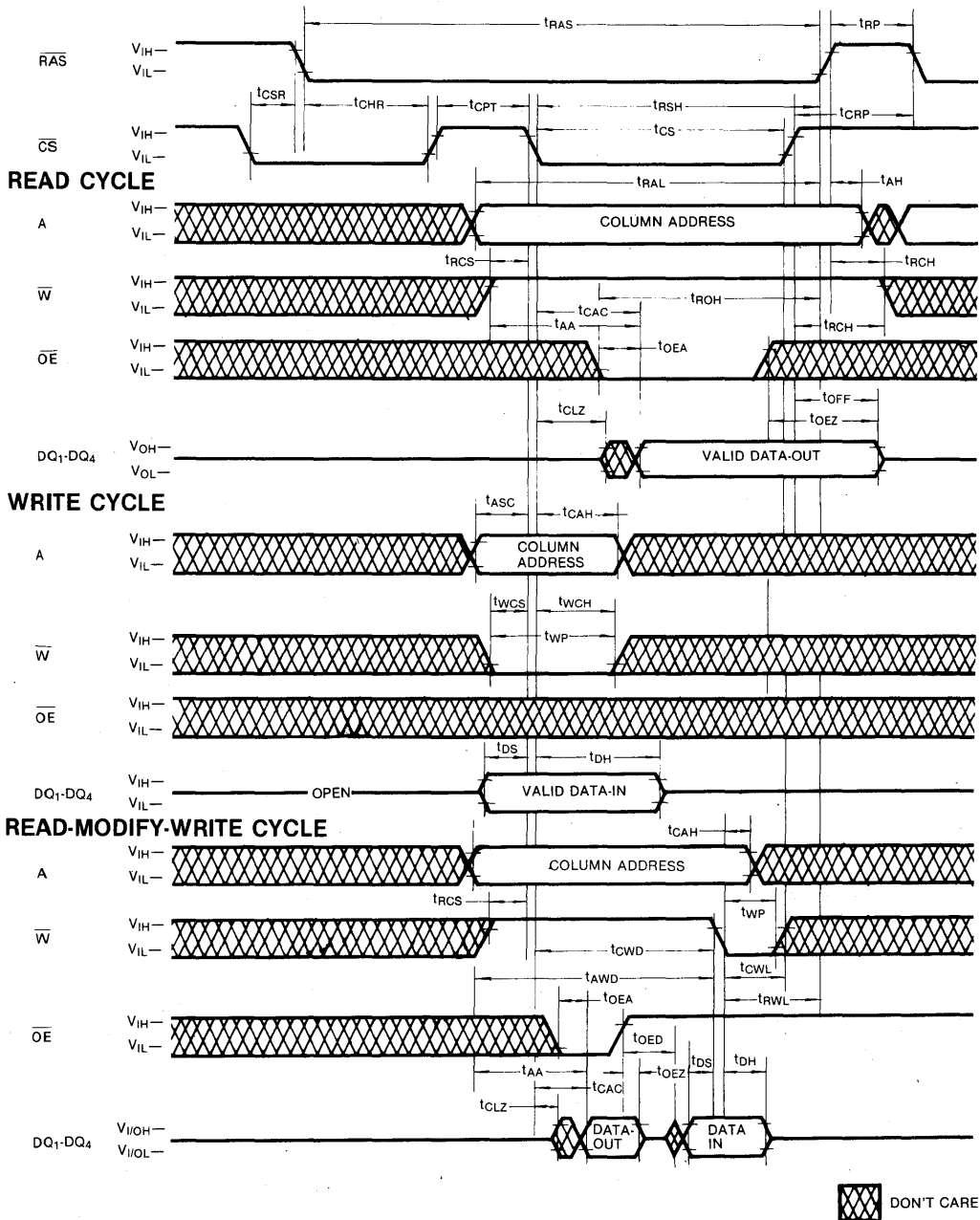


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

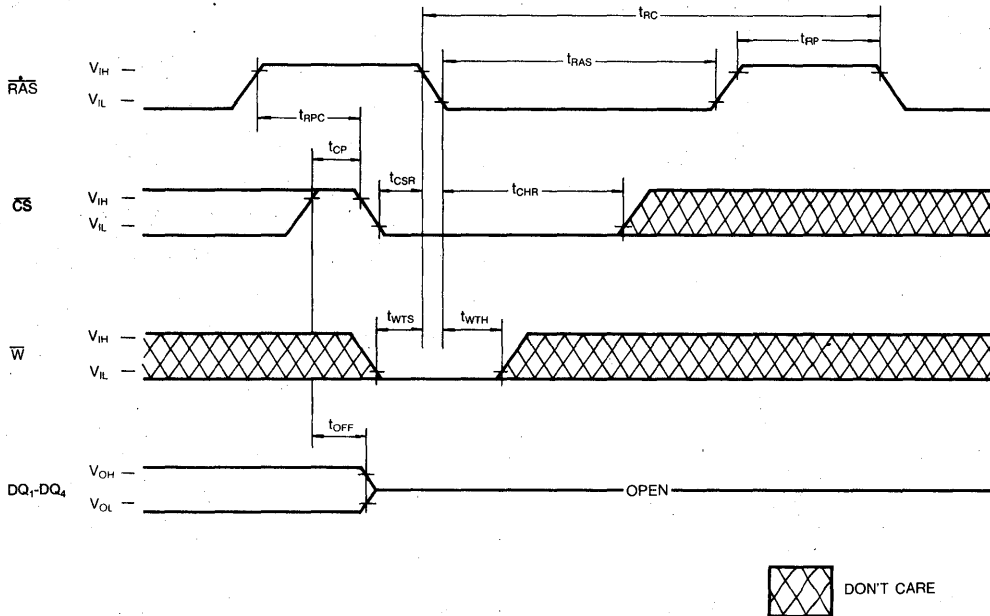


5

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



TEST MODE DESCRIPTION

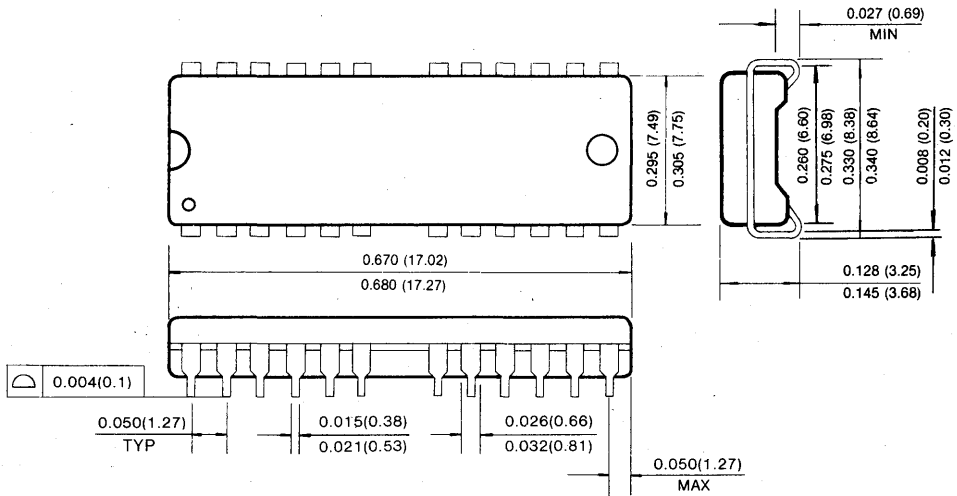
The KM44C4102 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0, A_1 , are not used. If, upon reading, 16 bits are equal (all "1" or "0's) the Q pin indicates a "1". If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a $1M \times 4$ DRAM. \overline{W} , \overline{CS} -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And \overline{CS} -BEFORE- \overline{RAS} REFRESH CYCLE "or" \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

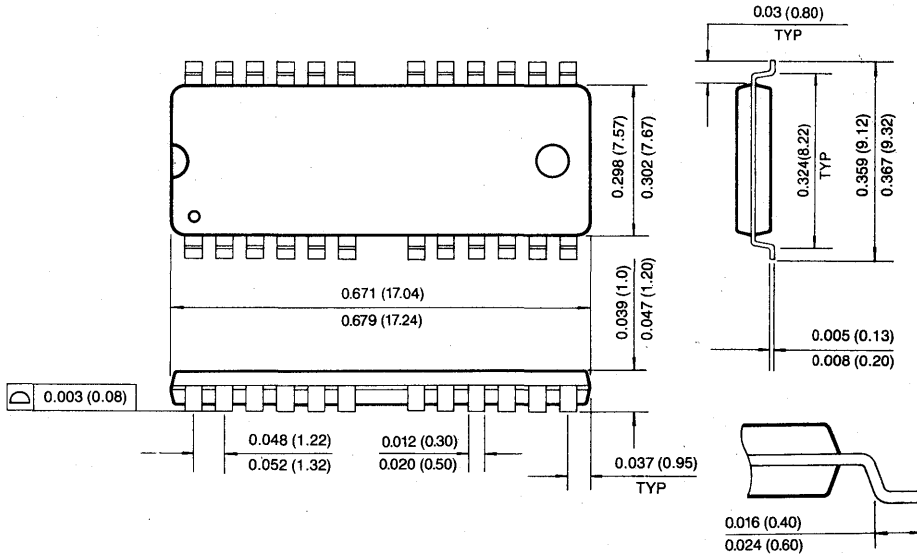
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



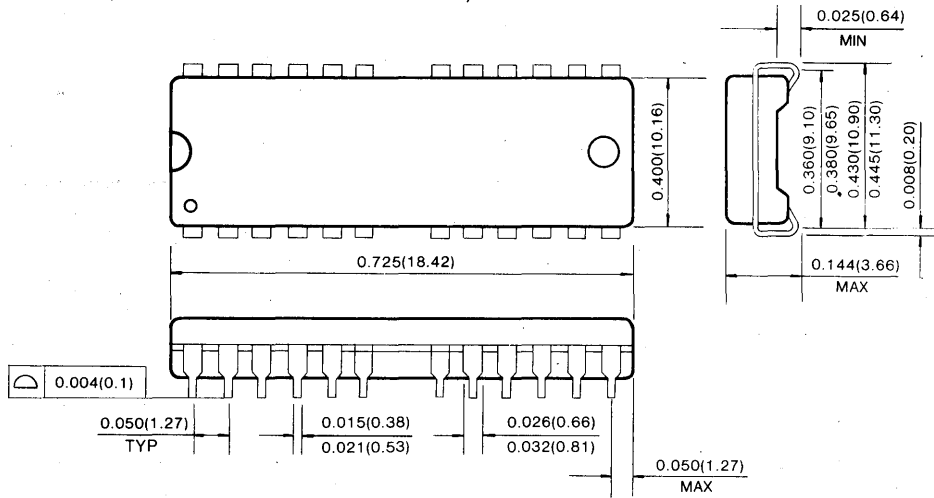
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



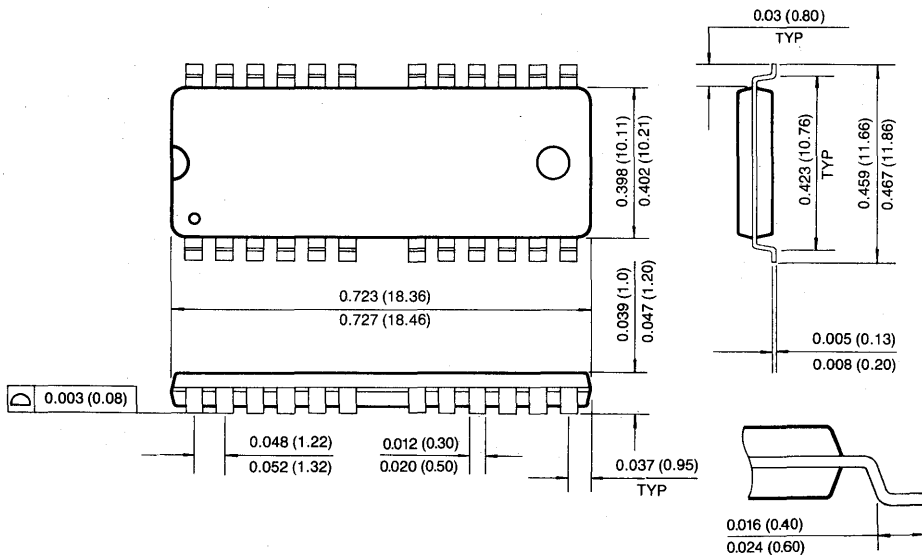
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE
(400MIL, Forward and Reverse Type)



4M × 4 Bit CMOS Quad CAS DRAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tCAC	trc
KM44C4003A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4003A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4003A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4003A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refresh Operation (LL-ver. only)
- Four separate CAS pins provide for separate I/O operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single +5.0V ± 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

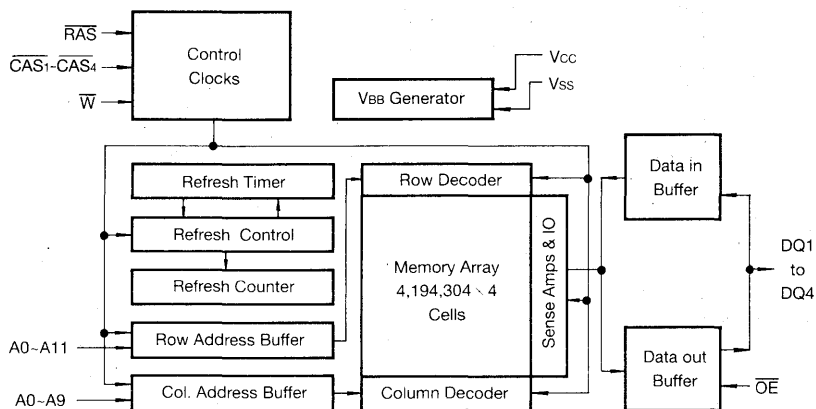
The Samsung KM44C4003A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4003A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible and four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation allowing this device to operate in parity mode.

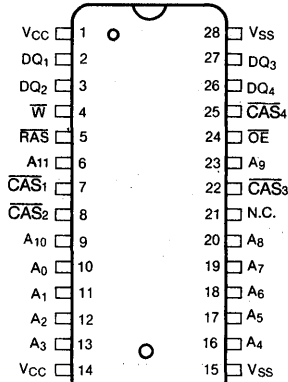
The KM44C4003A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



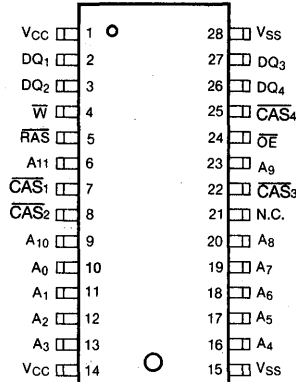
PIN CONFIGURATION (Top Views)

• KM44C4003 AJ/ALJ/ALLJ/ASLJ



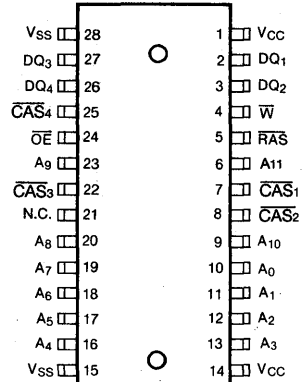
J : 400MIL

• KM44C4003 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM44C4003 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS1~CAS4	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5.0V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44C4003A/AL/ALL/ASL-5	I _{CC1}	-	90	mA
	KM44C4003A/AL/ALL/ASL-6			80	mA
	KM44C4003A/AL/ALL/ASL-7			70	mA
	KM44C4003A/AL/ALL/ASL-8			60	mA
Standby Current (RAS=CAS=W=V _{IH})	KM44C4003A	I _{CC2}	-	2	mA
	KM44C4003AL			1	mA
	KM44C4003ALL			1	mA
	KM44C4003ASL			1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM44C4003A/AL/ALL/ASL-5	I _{CC3}	-	90	mA
	KM44C4003A/AL/ALL/ASL-6			80	mA
	KM44C4003A/AL/ALL/ASL-7			70	mA
	KM44C4003A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM44C4003A/AL/ALL/ASL-5	I _{CC4}	-	80	mA
	KM44C4003A/AL/ALL/ASL-6			70	mA
	KM44C4003A/AL/ALL/ASL-7			60	mA
	KM44C4003A/AL/ALL/ASL-8			50	mA
Standby Current (RAS=CAS=W=V _{CC} -0.2V)	KM44C4003A	I _{CC5}	-	1	mA
	KM44C4003AL			300	μA
	KM44C4003ALL			200	μA
	KM44C4003ASL			200	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44C4003A/AL/ALL/ASL-5	I _{CC6}	-	90	mA
	KM44C4003A/AL/ALL/ASL-6			80	mA
	KM44C4003A/AL/ALL/ASL-7			70	mA
	KM44C4003A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DQ1-DQ4=Don't Care trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), trAS=trAS≤min-300ns	KM44C4003AL	I _{CC7}	-	450	μA
	KM44C4003ASL			350	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1-DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	TRC	90		110		130		150		ns	
Read-modify-write cycle time	TRWC	133		155		185		205		ns	
Access time from RAS	TRAC		50		60		70		80	ns	3,4,11
Access time from CAS	TCAC		13		15		20		20	ns	3,4,5,19
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3,19
Output buffer turn-off delay	toFF	0	15	0	15	0	20	0	20	ns	7,19
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trP	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	17
CAS hold time	tOSH	50		60		70		80		ns	18
CAS pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	24
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	4,17
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tcRP	5		5		5		5		ns	18
Row address set-up time	tASR	0		0		0		0		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	17
Column address hold time	tCAH	10		10		15		15		ns	17
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	17
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9,18
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	25
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		20		20		ns	18
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8,17
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	8,17
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	17
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	18
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time (C-B-R counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3,19
Fast Page mode cycle time	tPC	35		40		45		50		ns	20
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	20
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	21
$\overline{\text{RAS}}$ pulse width(Fast Page mode)	tRASP	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	22
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	23
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twts	10		10		10		10		ns	
Write command hold time (Test mode in)	twth	10		10		10		10		ns	
\bar{W} to $\bar{R}\bar{A}\bar{S}$ precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	twrp	10		10		10		10		ns	
\bar{W} to $\bar{R}\bar{A}\bar{S}$ hold time (\bar{C} - \bar{B} - \bar{R} refresh)	twrh	10		10		10		10		ns	
$\bar{R}\bar{A}\bar{S}$ pulse width (\bar{C} - \bar{B} - \bar{R} self refresh)	trass	100		100		100		100		μ s	15
$\bar{R}\bar{A}\bar{S}$ precharge time (\bar{C} - \bar{B} - \bar{R} self refresh)	trps	90		110		130		150		ns	15
$\bar{C}\bar{A}\bar{S}$ hold time (\bar{C} - \bar{B} - \bar{R} self refresh)	tchs	-50		-50		-50		-50		ns	15
Hold time $\bar{C}\bar{A}\bar{S}$ low to $\bar{C}\bar{A}\bar{S}$ high	tclch	5		5		5		5		ns	16

TEST MODE CYCLE

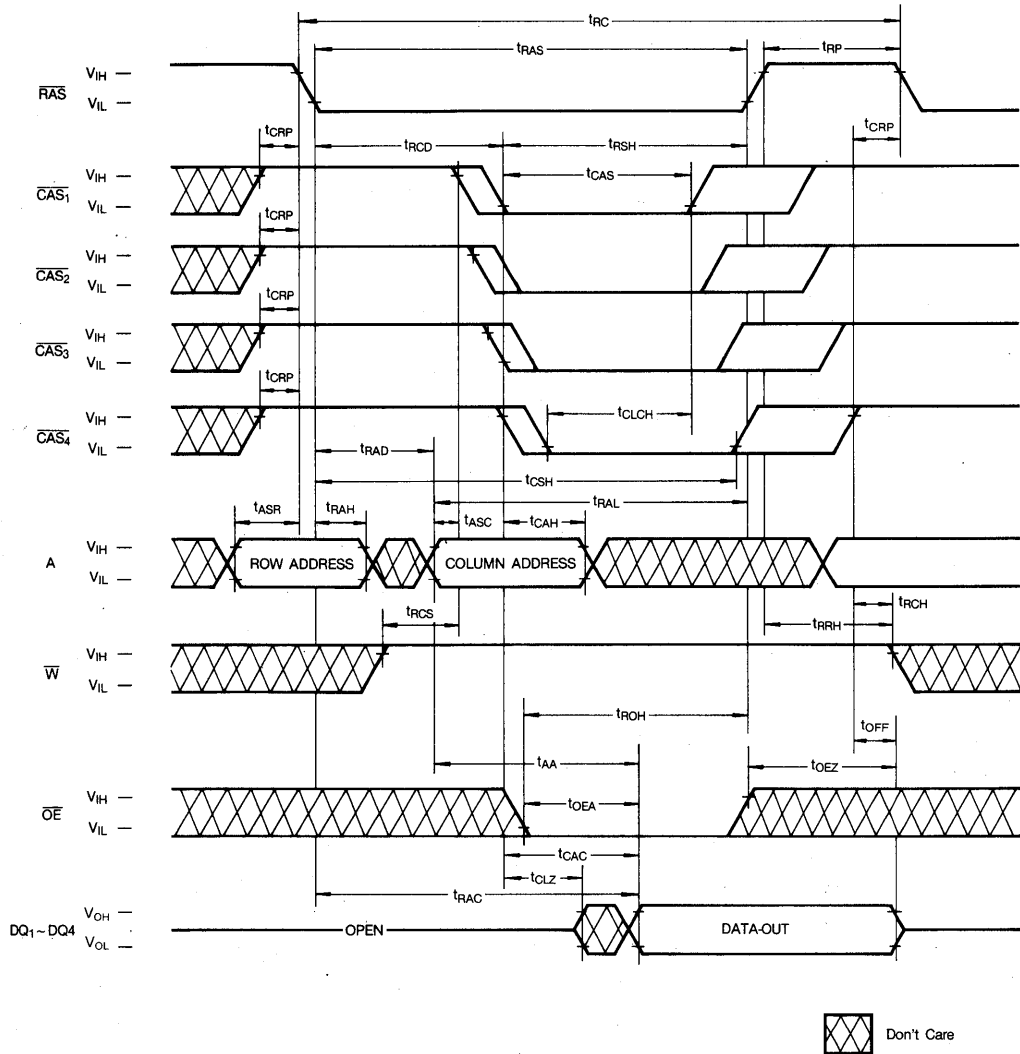
(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	95		115		135		155		ns	
Read-modify-write cycle time	trwc	138		160		190		210		ns	
Access time from $\bar{R}\bar{A}\bar{S}$	trac		55		65		75		85	ns	3,4,11,13
Access time from $\bar{C}\bar{A}\bar{S}$	tcac		18		20		25		25	ns	3,4,5,13
Access time from column address	taa		30		35		40		45	ns	3,11,13
$\bar{R}\bar{A}\bar{S}$ pulse width	tras	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\bar{C}\bar{A}\bar{S}$ pulse width	tcas	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\bar{R}\bar{A}\bar{S}$ hold time	trsh	18		20		25		25		ns	
$\bar{C}\bar{A}\bar{S}$ hold time	tcsH	55		65		75		85		ns	
Column address to $\bar{R}\bar{A}\bar{S}$ lead time	tral	30		35		40		45		ns	
$\bar{C}\bar{A}\bar{S}$ to \bar{W} delay time	tcwd	41		45		55		55		ns	8
$\bar{R}\bar{A}\bar{S}$ to \bar{W} delay time	trwd	78		90		105		115		ns	8
Column address to \bar{W} delay time	tawd	53		60		70		75		ns	8
Fast Page mode cycle time	tpc	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tprowc	81		90		105		110		ns	
$\bar{R}\bar{A}\bar{S}$ pulse width (Fast Page Mode)	trasp	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\bar{C}\bar{A}\bar{S}$ precharge	tcpa		35		40		45		50	ns	3
$\bar{O}\bar{E}$ access time	toea		18		20		25		25	ns	
$\bar{O}\bar{E}$ to data delay	toed	18		20		25		25		ns	
$\bar{O}\bar{E}$ command hold time	toeh	18		20		25		25		ns	

NOTES

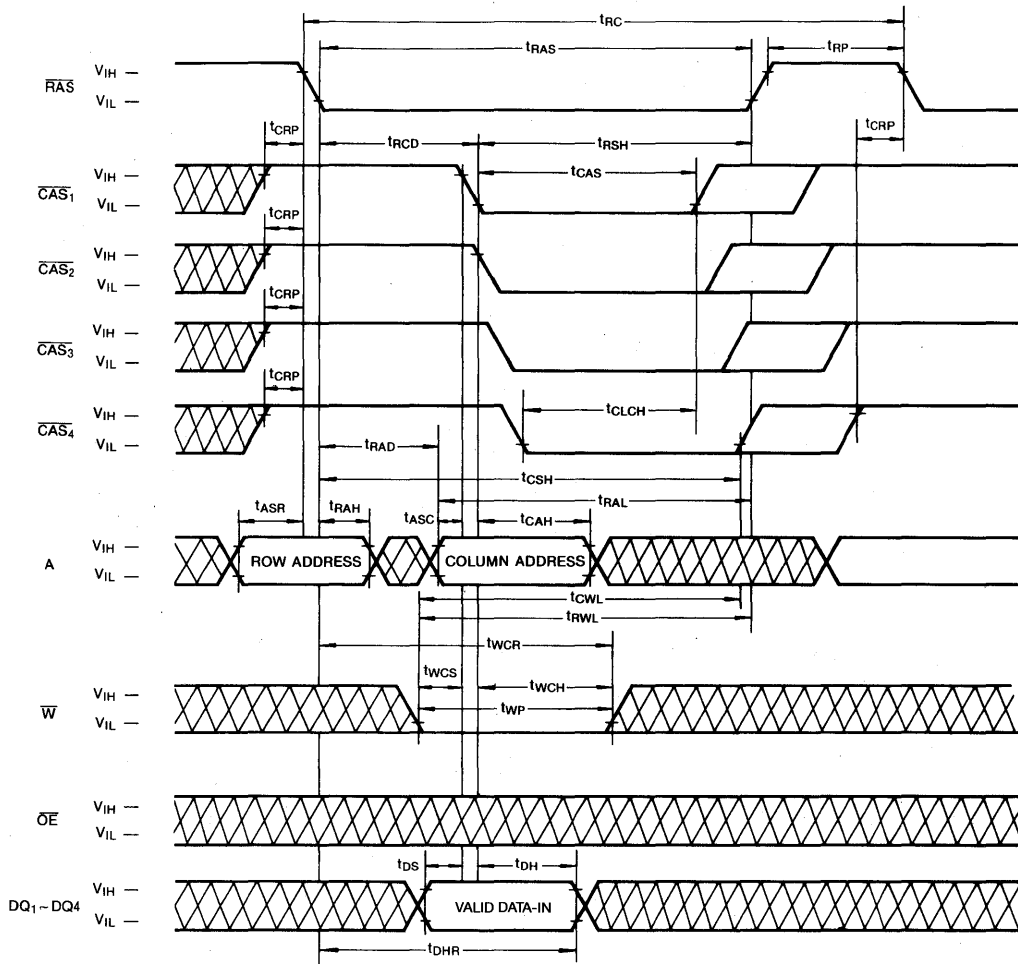
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RCD}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWd} , t_{cWd} and t_{AWd} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{cWd} \geq t_{cWd}(\min)$, $t_{RWd} \geq t_{RWd}(\min)$ and $t_{AWd} \geq t_{AWd}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RCD}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. In order to hold the address latched by the first \overline{CAS} going low, the parameter t_{CLCH} must be met.
17. The first \overline{CASx} edge to transition low.
18. The last \overline{CASx} edge to transition high.
19. Output parameter is referenced to corresponding \overline{CASx} input.
20. Last rising \overline{CASx} edge to next cycle's last rising \overline{CASx} edge.
21. Last rising \overline{CASx} edge to first falling \overline{CAS} edge.
22. First DQx controlled by the first \overline{CASx} to go low.
23. Last DQx controlled by the last \overline{CASx} to go high.
24. Each \overline{CASx} must meet minimum pulse width.
25. Last \overline{CASx} to go low.

TIMING DIAGRAM
READ CYCLE



TIMING DIAGRAM (Continued)

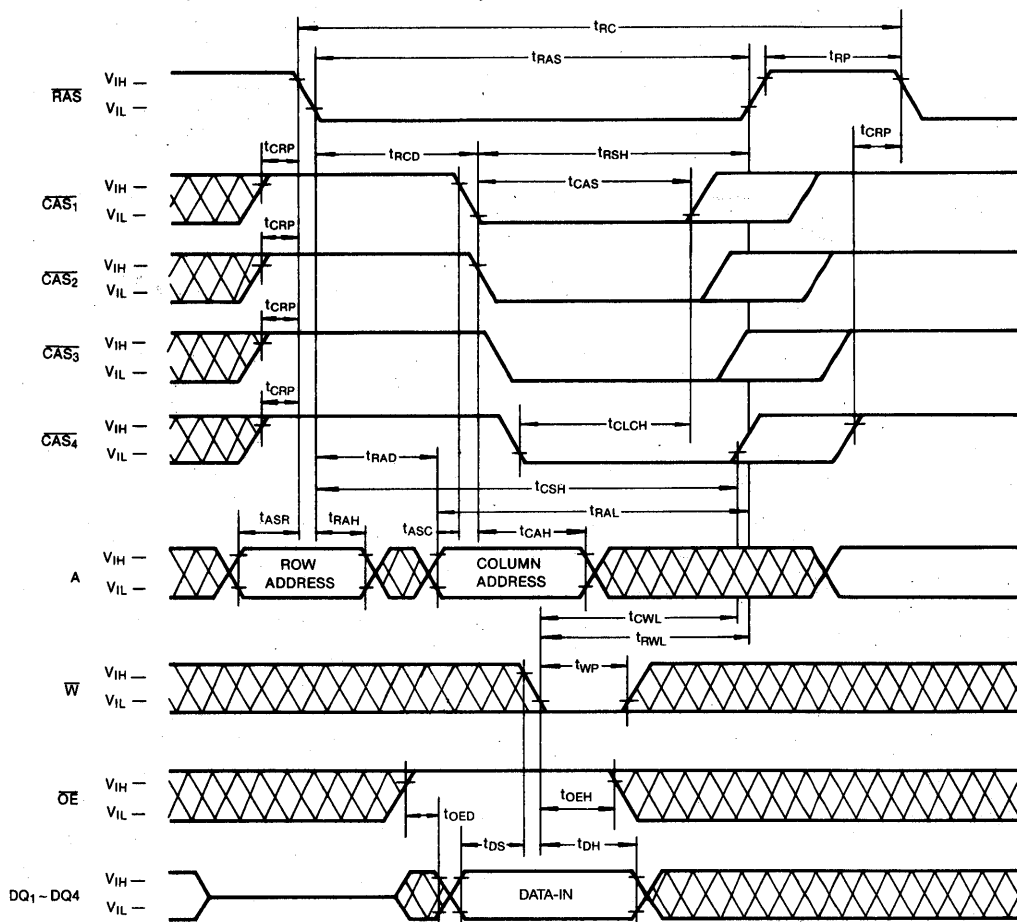
WRITE CYCLE (EARLY WRITE)



 Don't Care

TIMING DIAGRAM (Continued)

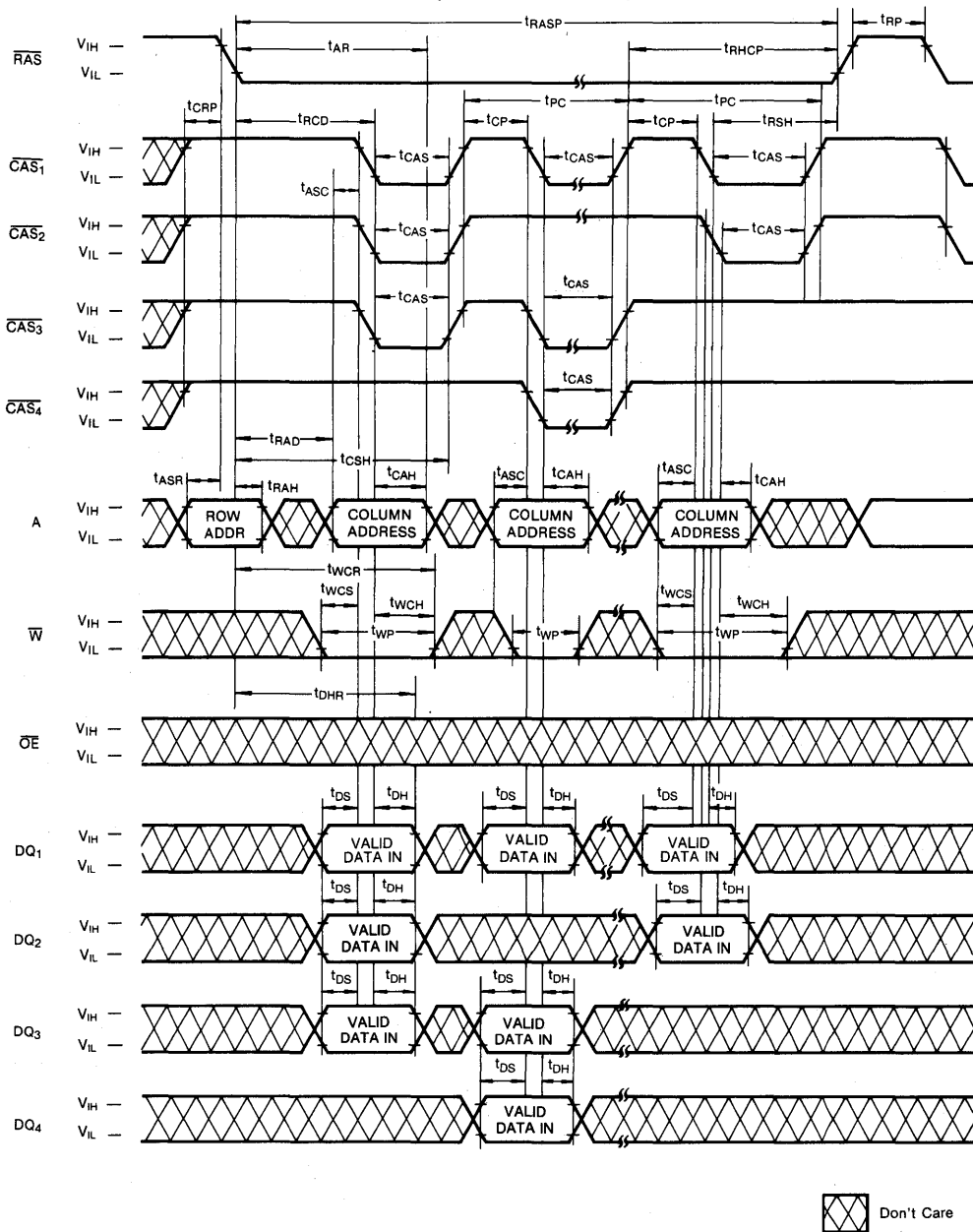
WRITE CYCLE (OE CONTROLLED WRITE)



 Don't Care

TIMING DIAGRAM (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

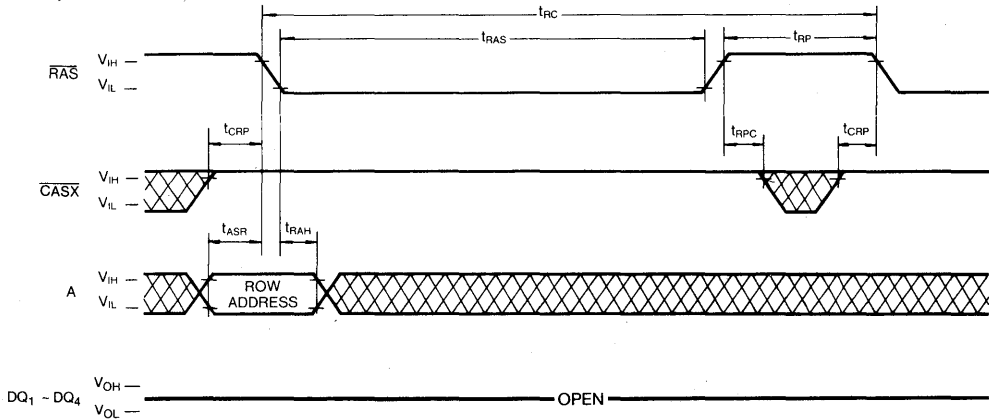


5

TIMING DIAGRAMS (Continued)

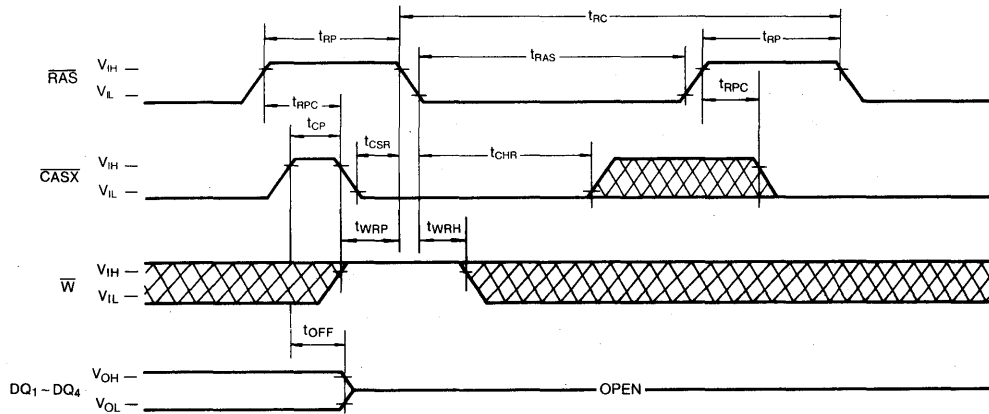
RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

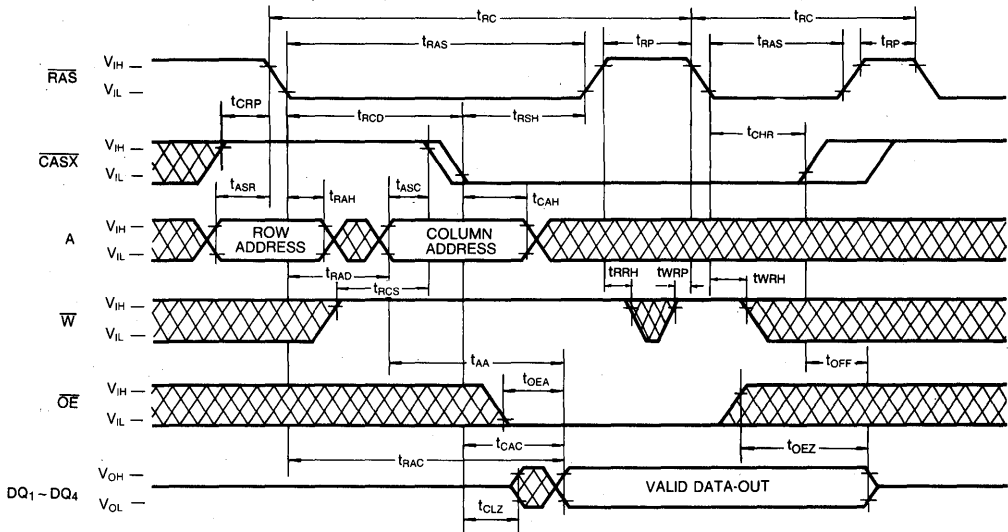
NOTE: \bar{W} , \bar{OE} , A = Don't Care



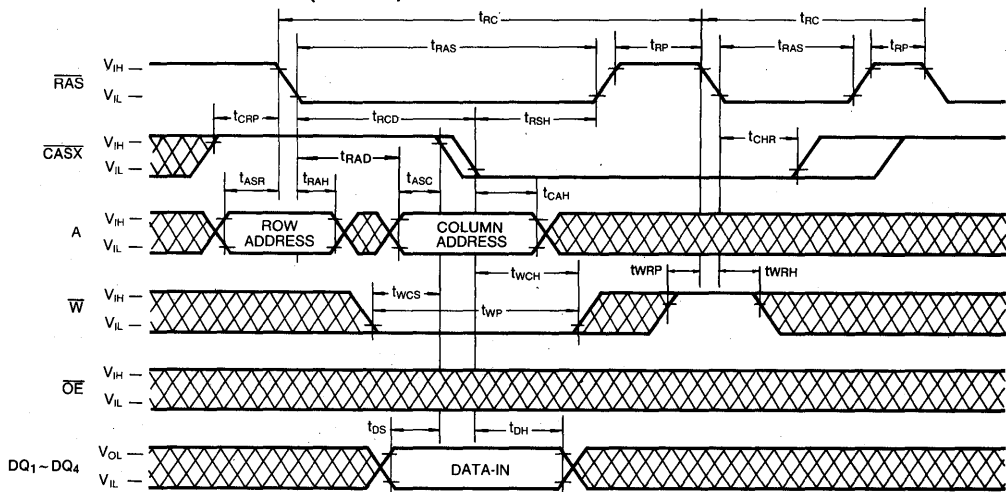
 DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

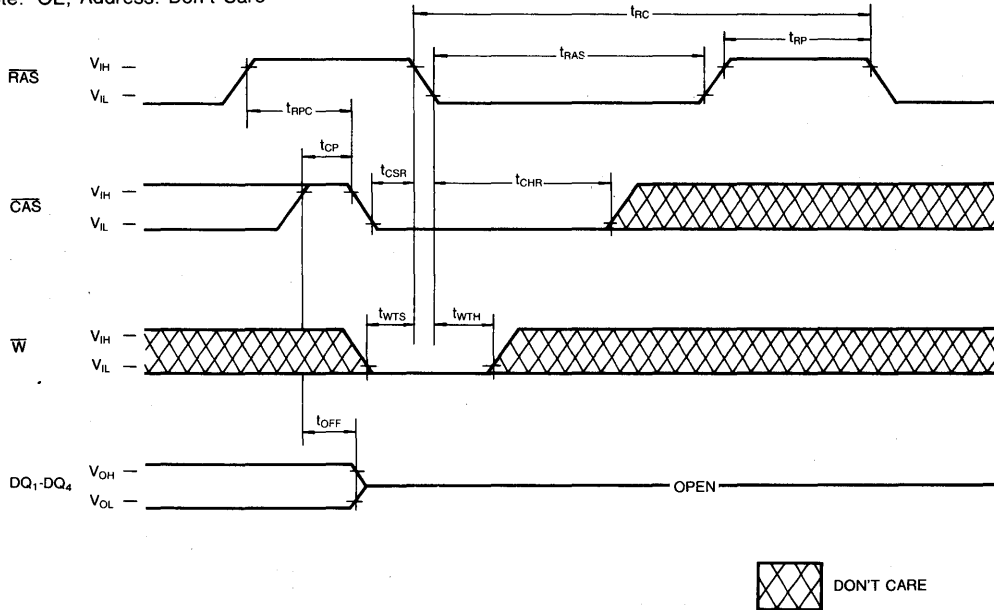


DON'T CARE

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

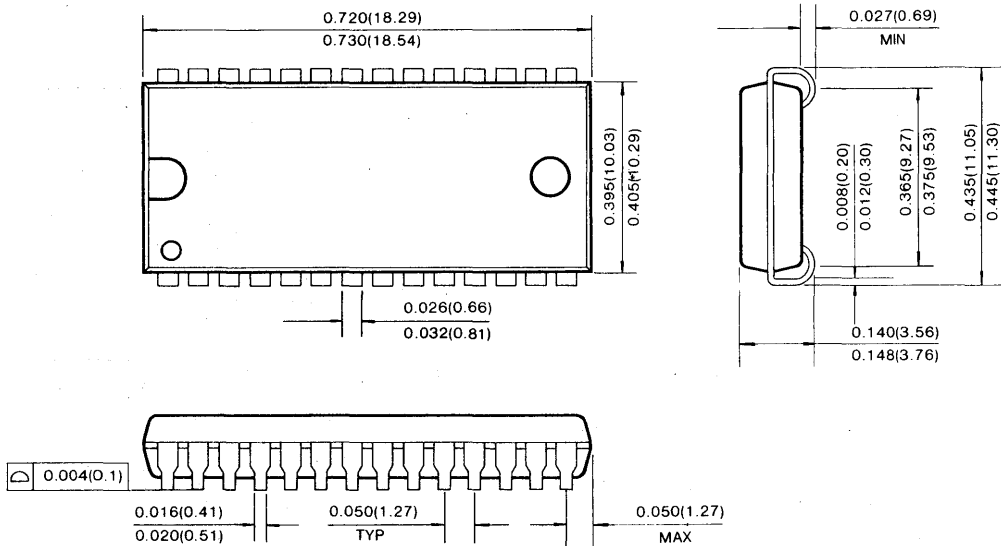
Note: OE, Address: Don't Care



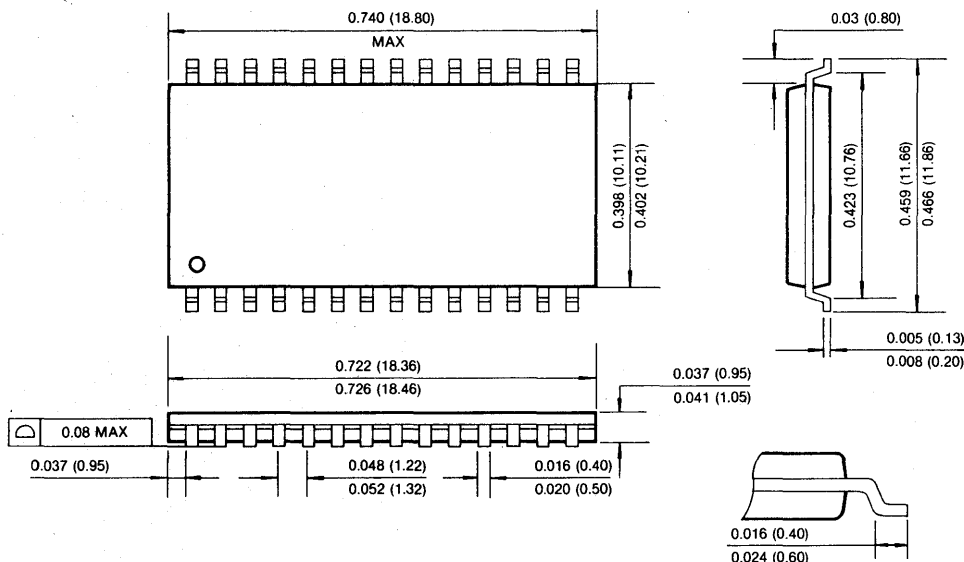
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



5

4M × 4 Bit CMOS Quad CAS DRAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM44C4103A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4103A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4103A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4103A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Self Refresh Operation (LL-ver, only)
- Four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single +5.0V ± 10% power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

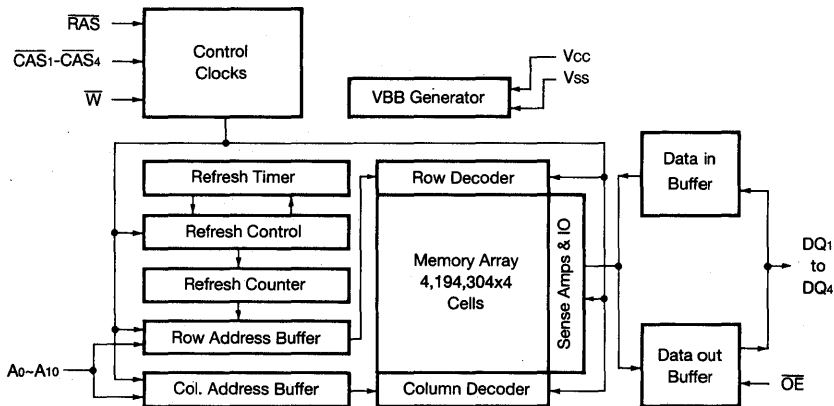
The Samsung KM44C4103A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4103A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible, and four separate $\overline{\text{CAS}}$ pins provide for separate I/O operation allowing this device to operate in parity mode.

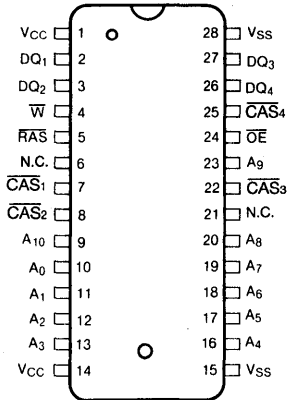
The KM44C4103A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



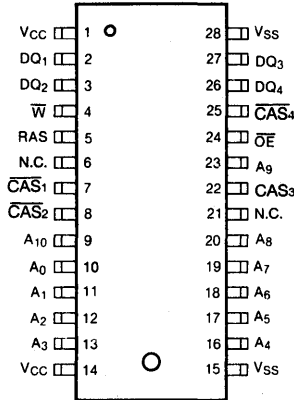
PIN CONFIGURATION (Top Views)

• KM44C4103 AJ/ALJ/ALLJ/ASLJ



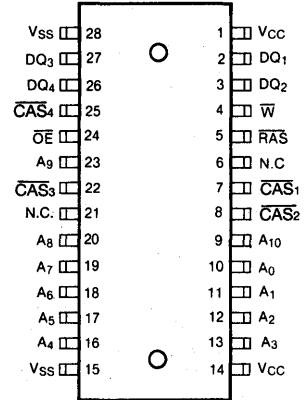
J : 400MIL

• KM44C4103 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM44C4103 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A ₀ -A ₁₀	Address Inputs
DQ ₁ -4	Data In/Out
Vss	Ground
\overline{RAS}	Row Address Strobe
\overline{CAS}_1 - \overline{CAS}_4	Column Address Strobe
\overline{W}	Read/Write Input
\overline{OE}	Data Output Enable
Vcc	Power(+5.0V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CAS Cycling @ t _{RC} =min.)	KM44C4103A/AL/ALL/ASL-5	I _{CC1}	-	110	mA
	KM44C4103A/AL/ALL/ASL-6			100	mA
	KM44C4103A/AL/ALL/ASL-7			90	mA
	KM44C4103A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{IH}$)	KM44C4103A	I _{CC2}	-	2	mA
	KM44C4103AL			1	mA
	KM44C4103ALL			1	mA
	KM44C4103ASL			1	mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\overline{\text{CAS}}=V_{IH}$, $\overline{\text{RAS}}$ Cycling @ t _{RC} =min.)	KM44C4103A/AL/ALL/ASL-5	I _{CC3}	-	110	mA
	KM44C4103A/AL/ALL/ASL-6			100	mA
	KM44C4103A/AL/ALL/ASL-7			90	mA
	KM44C4103A/AL/ALL/ASL-8			80	mA
Fast Page Mode Current* ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{CAS}}$, Address Cycling @ t _{FC} =min.)	KM44C4103A/AL/ALL/ASL-5	I _{CC4}	-	90	mA
	KM44C4103A/AL/ALL/ASL-6			80	mA
	KM44C4103A/AL/ALL/ASL-7			70	mA
	KM44C4103A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{CC}-0.2V$)	KM44C4103A	I _{CC5}	-	1	mA
	KM44C4103AL			300	μA
	KM44C4103ALL			200	μA
	KM44C4103ASL			200	μA
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ t _{RC} =min.)	KM44C4103A/AL/ALL/ASL-5	I _{CC6}	-	110	mA
	KM44C4103A/AL/ALL/ASL-6			100	mA
	KM44C4103A/AL/ALL/ASL-7			90	mA
	KM44C4103A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{\text{CAS}}=\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Cycling or 0.2V DQ1-DQ4=Don't Care t _{RC} =62.5μs(L-Ver.) 125μs(SL-Ver.), t _{TRAS} =t _{TRAS} ≤ min~300ns	KM44C4103AL	I _{CC7}	-	400	μA
	KM44C4103ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A10=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	I _{CCS}	-	300	μA
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{CC} +0.5V, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{CC})	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =4.2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (T_A=25°C, V_{CC}=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A10)	C _{IN1}	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	C _{IN2}	-	7	pF
Input Capacitance (DQ1-DQ4)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_a ≤ 70°C, V_{CC}=5.0V ± 0.5V, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	133		155		185		205		ns	
Access time from RAS	t _{RAC}		50		60		70		80	ns	3,4,11
Access time from CAS	t _{CAC}		13		15		20		20	ns	3,4,5,19
Access time from column address	t _{AA}		25		30		35		40	ns	3,11
CAS to output in Low-Z	t _{CLZ}	0		0		0		0		ns	3,19
Output buffer turn-off delay	t _{OFF}	0	15	0	15	0	20	0	20	ns	7,19
Transition time (rise and fall)	t _T	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	t _{RP}	30		40		50		60		ns	
RAS pulse width	t _{RS}	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	t _{RSH}	13		15		20		20		ns	17
CAS hold time	t _{CSH}	50		60		70		80		ns	18
CAS pulse width	t _{CAS}	13	10,000	15	10,000	20	10,000	20	10,000	ns	24
RAS to CAS delay time	t _{RCD}	20	37	20	45	20	50	20	60	ns	4,17
RAS to column address delay time	t _{RAD}	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	t _{CRP}	5		5		5		5		ns	18
Row address set-up time	t _{ASR}	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	17
Column address hold time	tCAH	10		10		15		15		ns	17
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	17
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9,18
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	25
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tRWL	13		15		20		20		ns	18
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8,17
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	8,17
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	17
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	18
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3,19
Fast Page mode cycle time	tPC	35		40		45		50		ns	20
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	20
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	21
$\overline{\text{RAS}}$ pulse width(Fast Page mode)	tRASP	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	22
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	23
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	
\bar{W} to \bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRP	10		10		10		10		ns	
\bar{W} to \bar{RAS} hold time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRH	10		10		10		10		ns	
\bar{RAS} pulse width (\bar{C} - \bar{B} - \bar{R} self refresh)	tRASS	100		100		100		100		μ s	15
\bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} self refresh)	tRPS	90		110		130		150		ns	15
\bar{CAS} hold time (\bar{C} - \bar{B} - \bar{R} self refresh)	tCHS	-50		-50		-50		-50		ns	15
Hold time \bar{CAS} low to \bar{CAS} high	tCLCH	5		5		5		5		ns	16

TEST MODE CYCLE

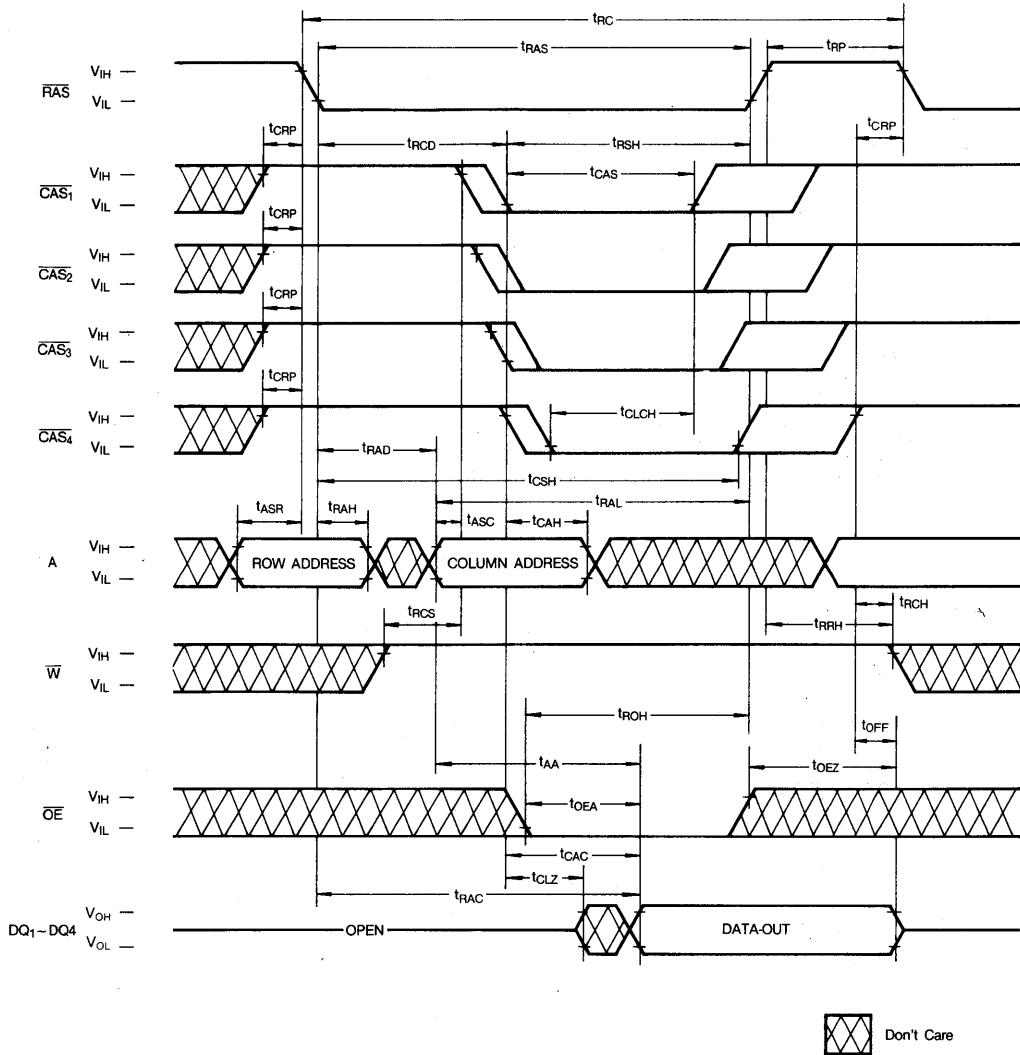
(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from \bar{RAS}	tRAC		55		65		75		85	ns	3,4,11,13
Access time from \bar{CAS}	tCAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
\bar{RAS} pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
\bar{RAS} hold time	tRSH	18		20		25		25		ns	
\bar{CAS} hold time	tCSH	55		65		75		85		ns	
Column address to \bar{RAS} lead time	tRAL	30		35		40		45		ns	
\bar{CAS} to \bar{W} delay time	tCWD	41		45		55		55		ns	8
\bar{RAS} to \bar{W} delay time	tRWD	78		90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
\bar{RAS} pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	tCPA		35		40		45		50	ns	3
\bar{OE} access time	tOEA		18		20		25		25	ns	
\bar{OE} to data delay	tOED	18		20		25		25		ns	
\bar{OE} command hold time	tOEH	18		20		25		25		ns	

NOTES

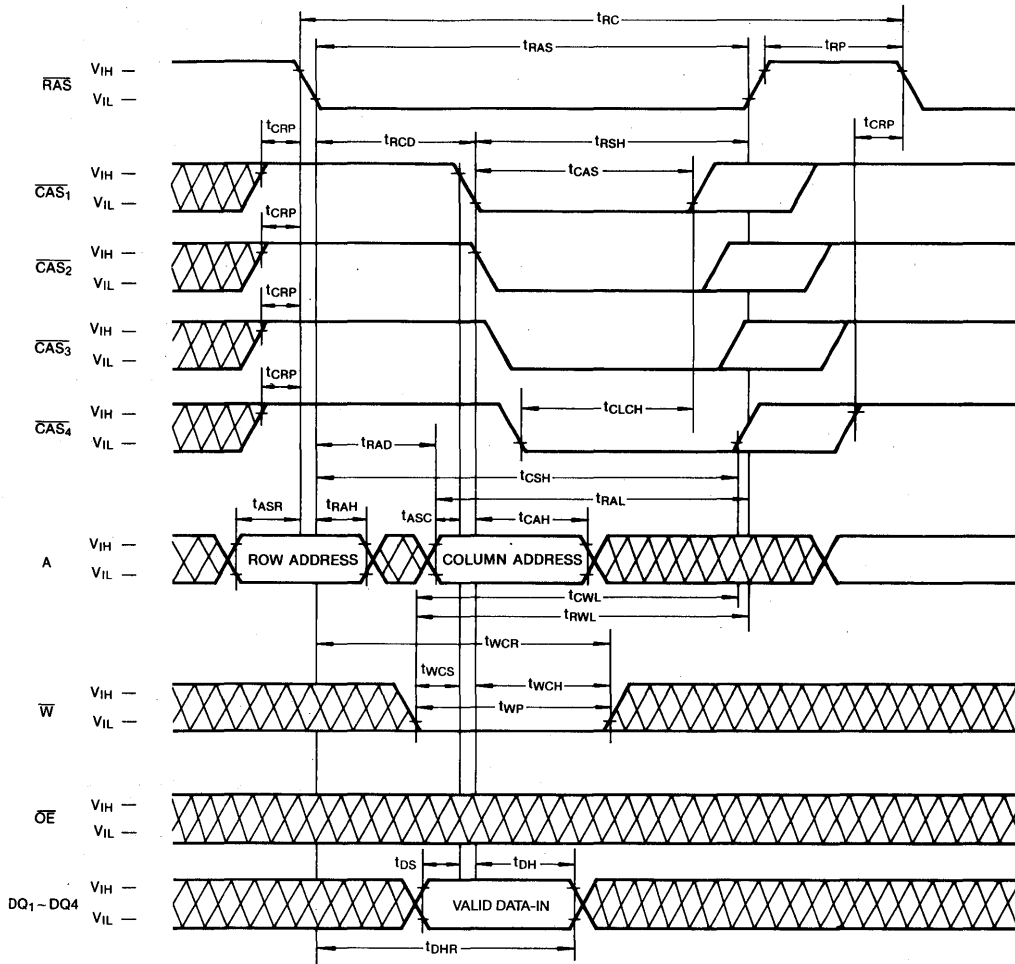
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 32ms before and after self refresh, in order to meet refresh specification.
16. In order to hold the address latched by the first \overline{CASx} going low. The parameter t_{CLCH} must be met.
17. The first \overline{CASx} edge to transition low.
18. The last \overline{CASx} edge to transition high.
19. Output parameter is referenced to corresponding \overline{CASx} input.
20. Last rising \overline{CASx} edge to next cycle's last rising \overline{CASx} edge.
21. Last rising \overline{CASx} edge to first falling \overline{CASx} edge.
22. First DQx controlled by the first \overline{CASx} to go low.
23. Last DQx controlled by the last \overline{CASx} to go high.
24. Each \overline{CASx} must meet minimum pulse width.
25. Last \overline{CASx} to go low.

TIMING DIAGRAM
READ CYCLE



5

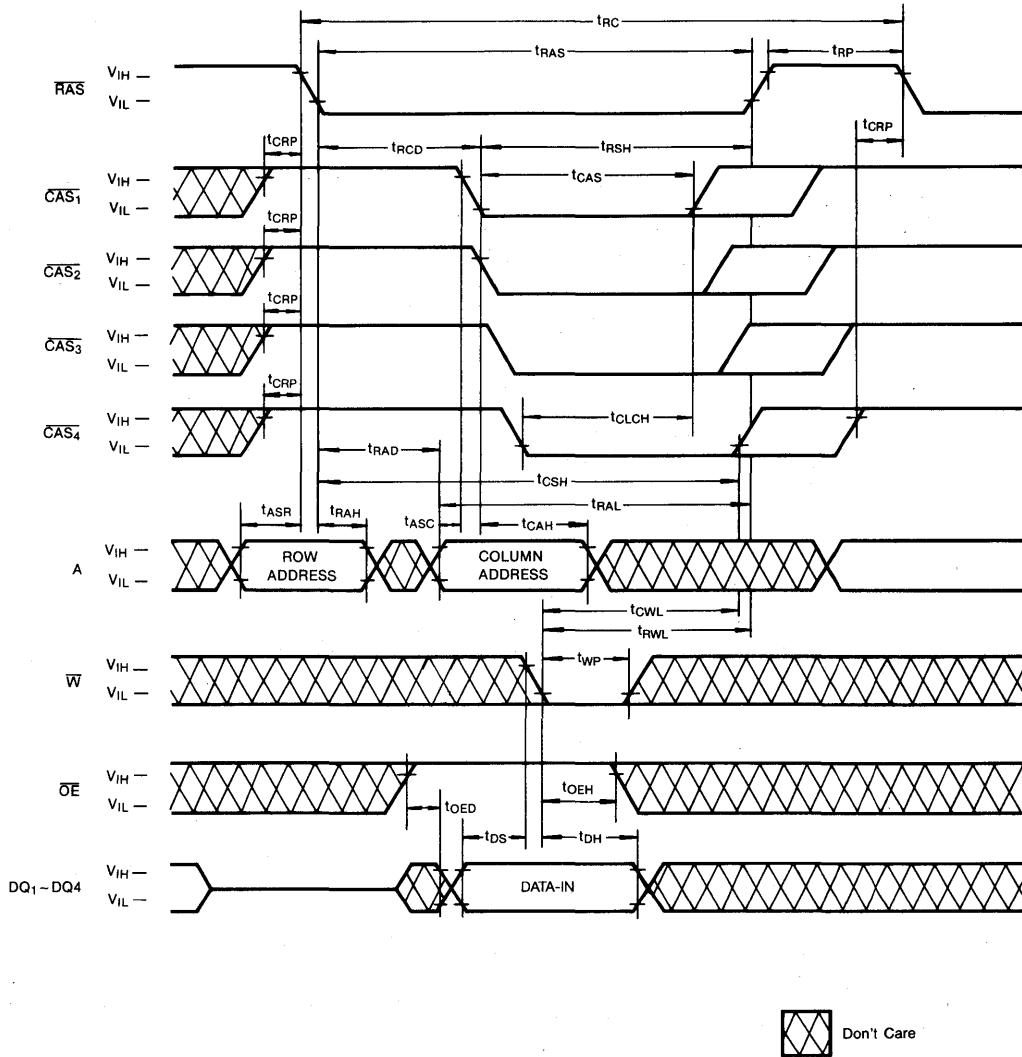
TIMING DIAGRAM (Continued)
WRITE CYCLE (EARLY WRITE)



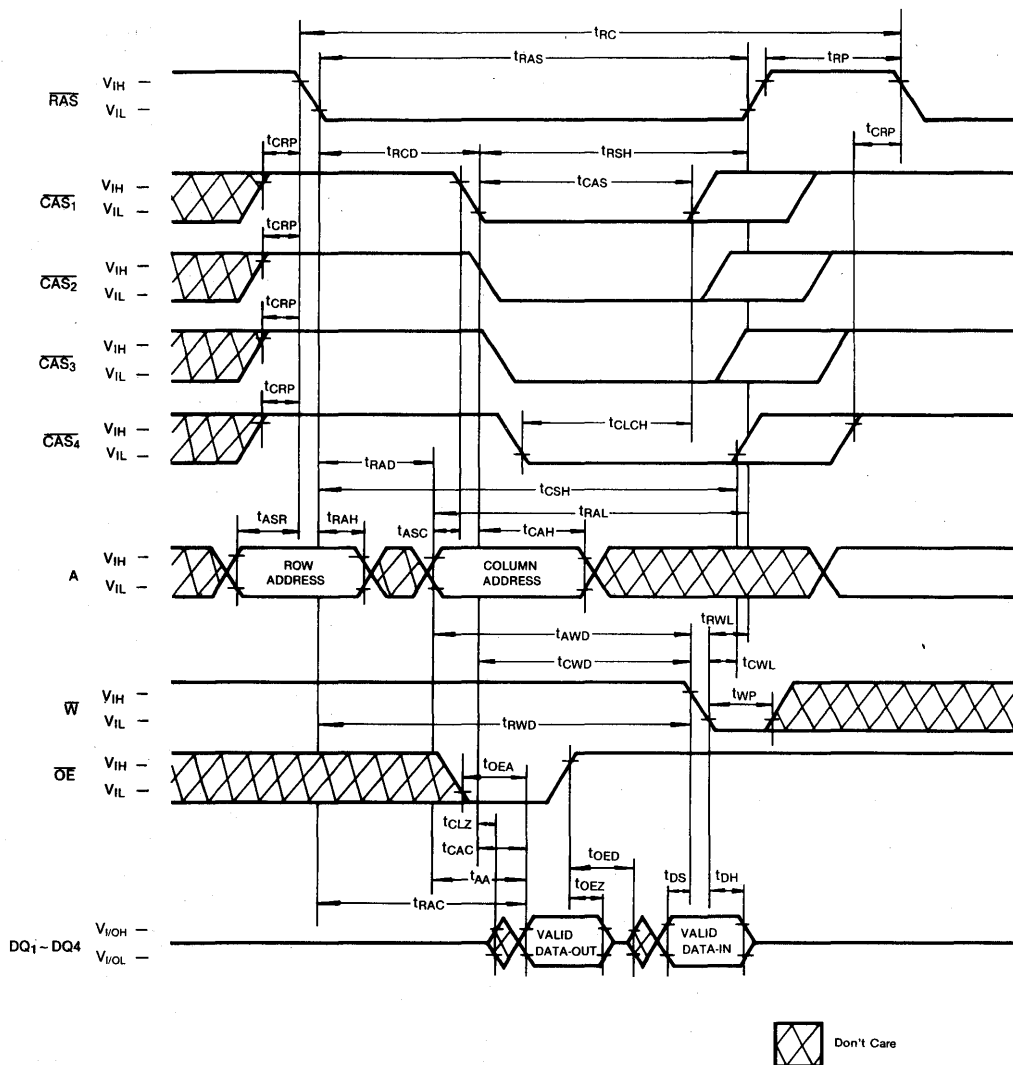
 Don't Care

TIMING DIAGRAM (Continued)

WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

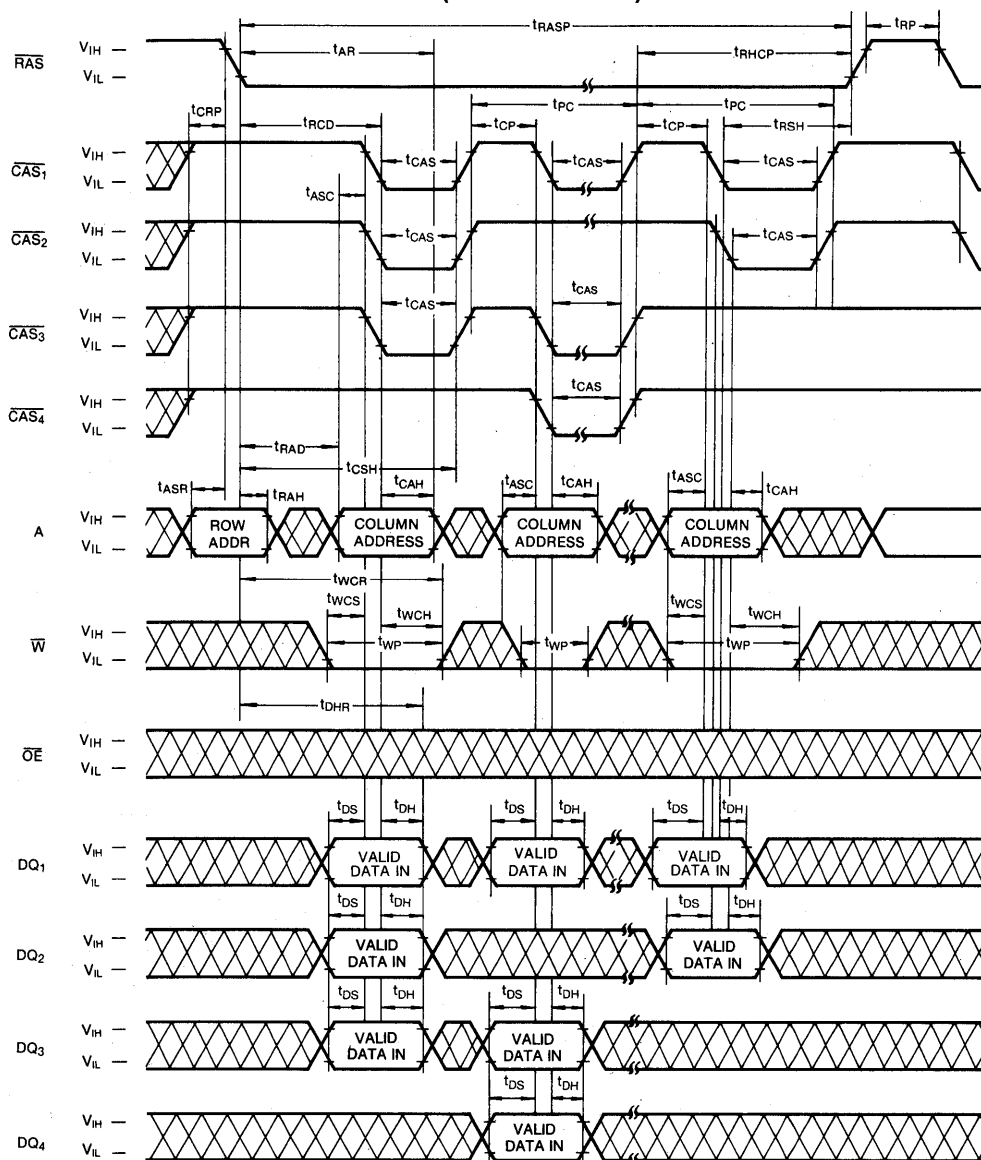


TIMING DIAGRAM (Continued)
READ-MODIFY-WRITE CYCLE



TIMING DIAGRAM (Continued)

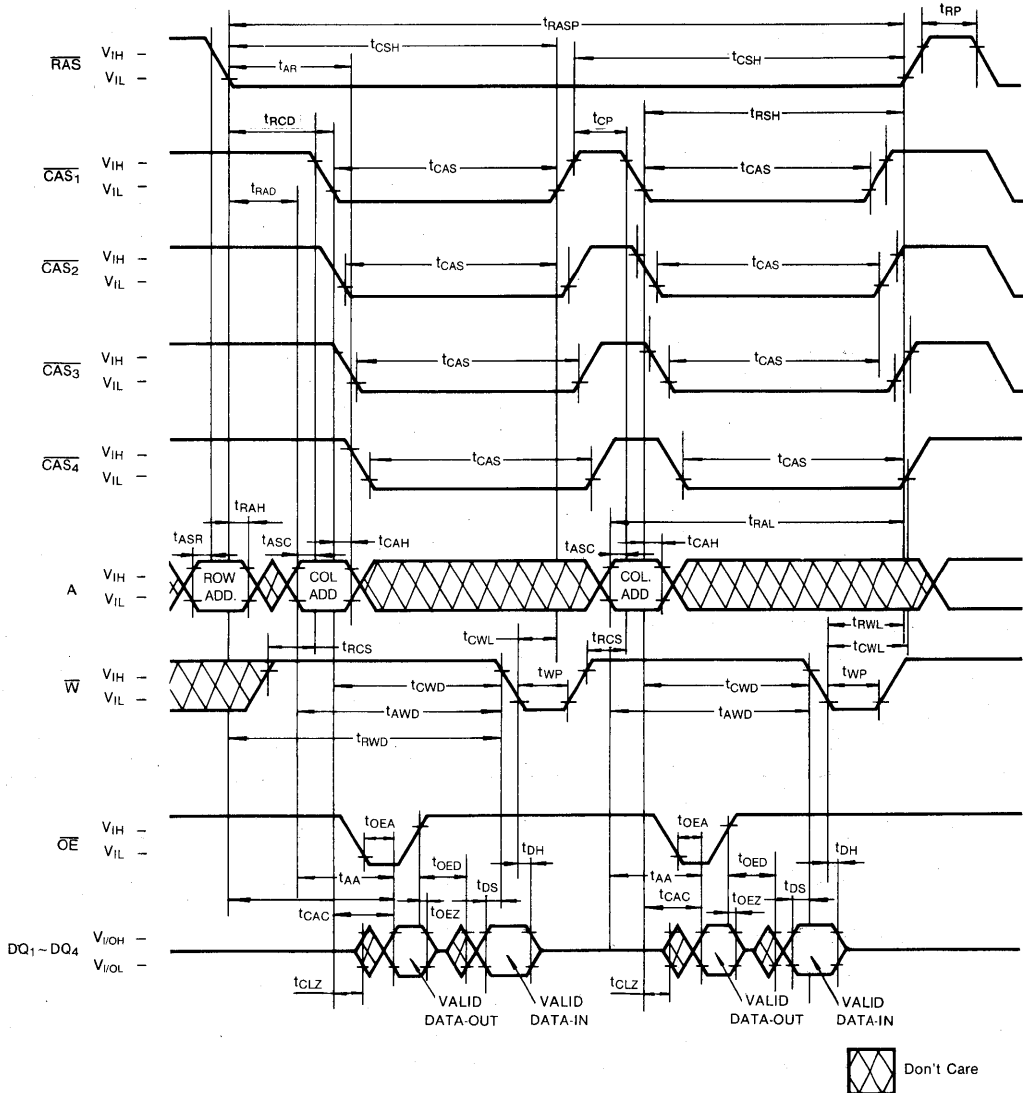
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



 Don't Care

TIMING DIAGRAM (Continued)

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

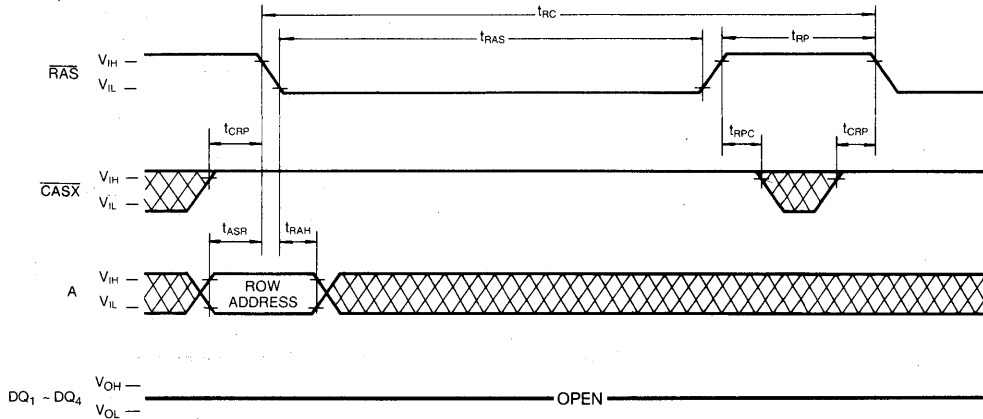


5

TIMING DIAGRAMS (Continued)

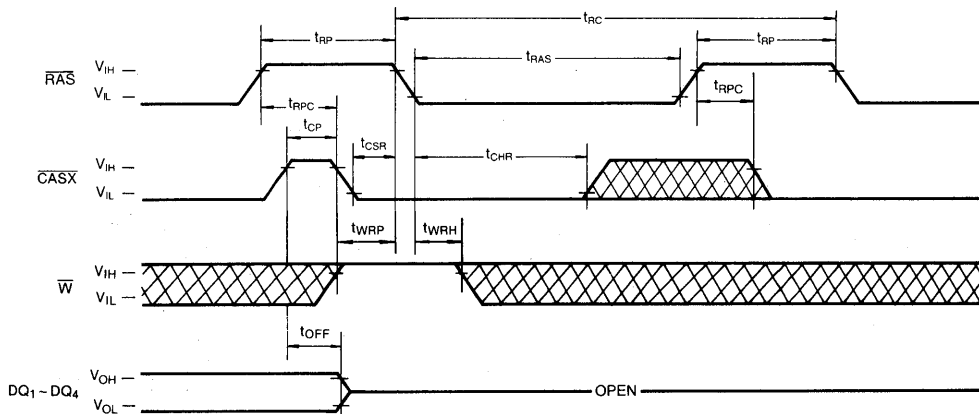
RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

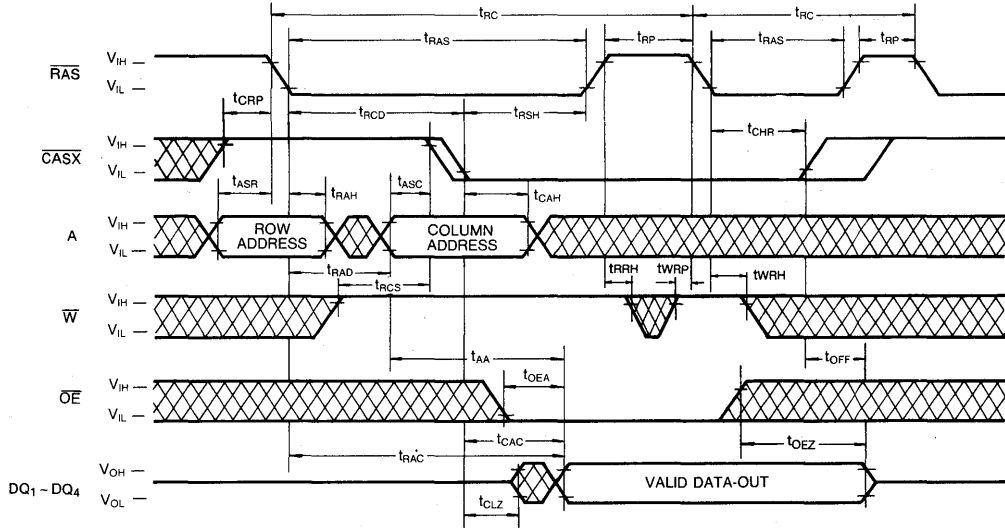
NOTE: \bar{W} , \bar{OE} , A = Don't Care



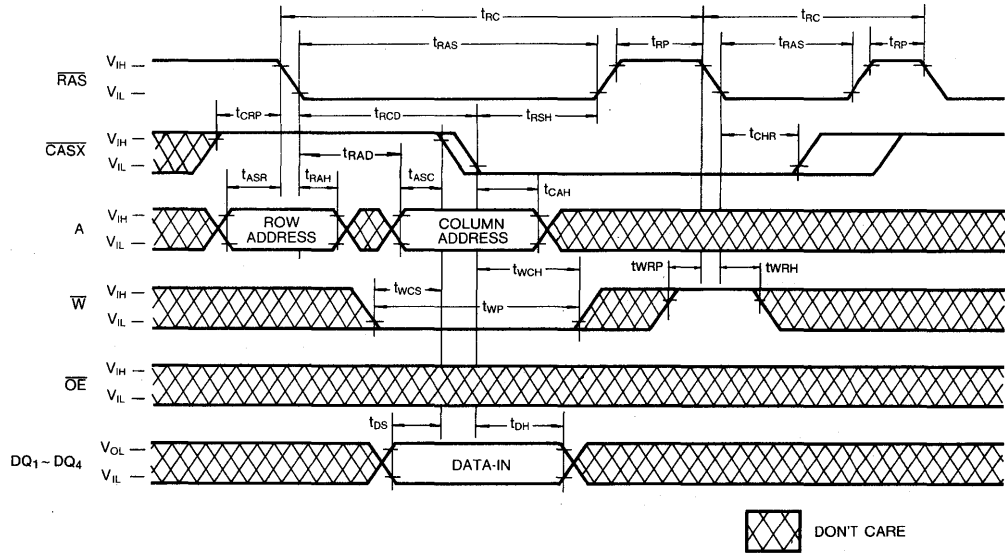
 DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

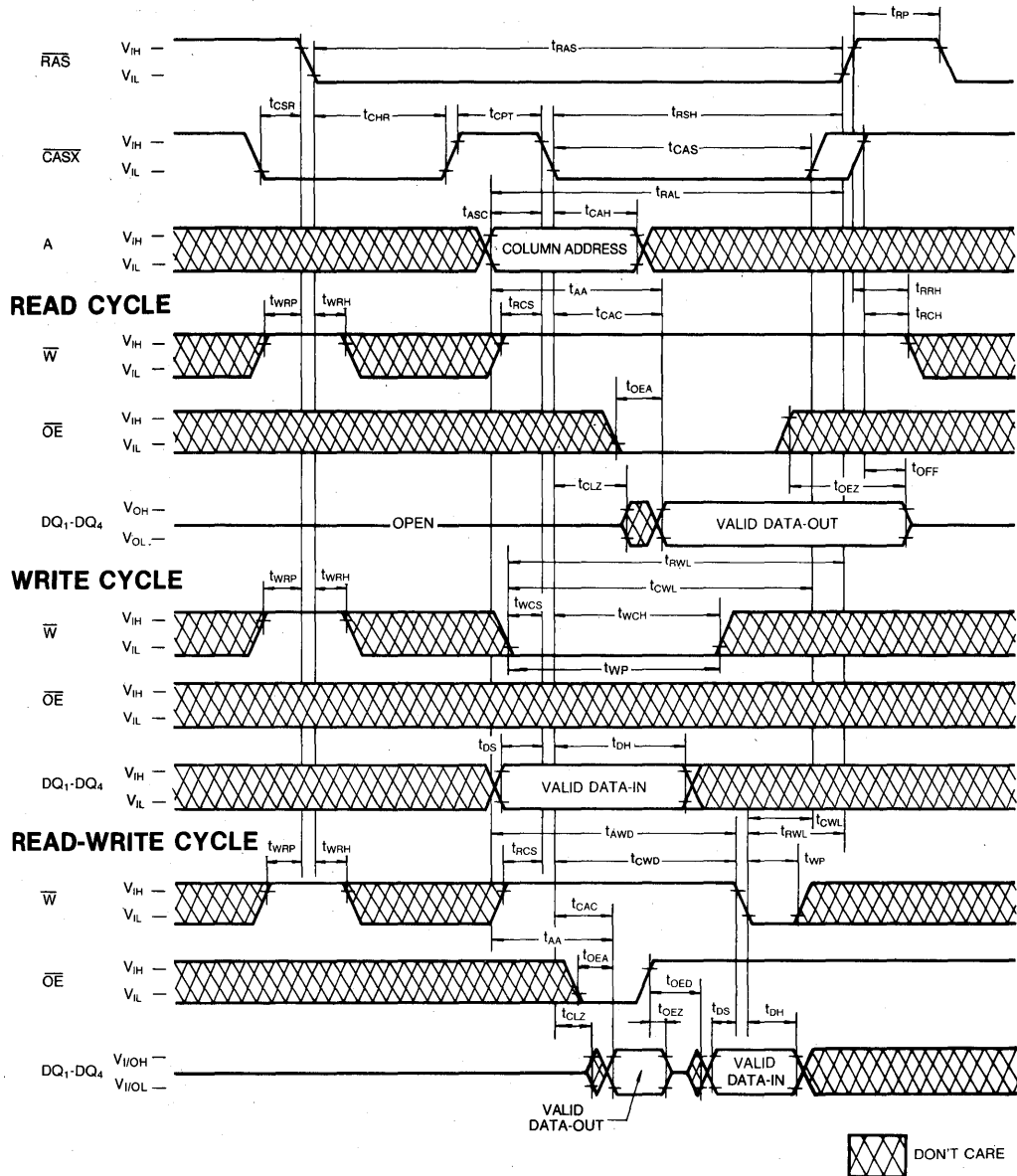


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

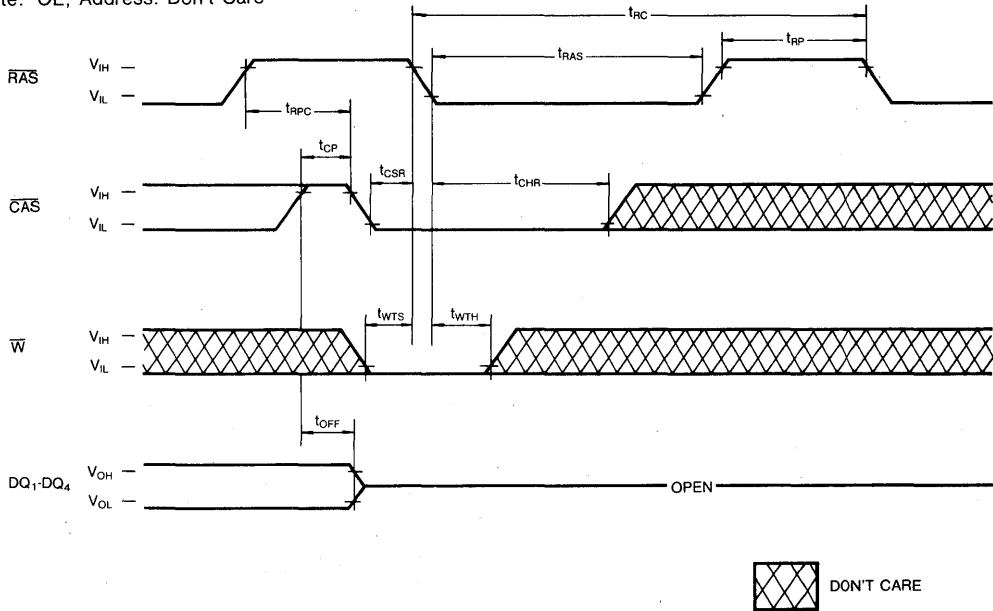
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

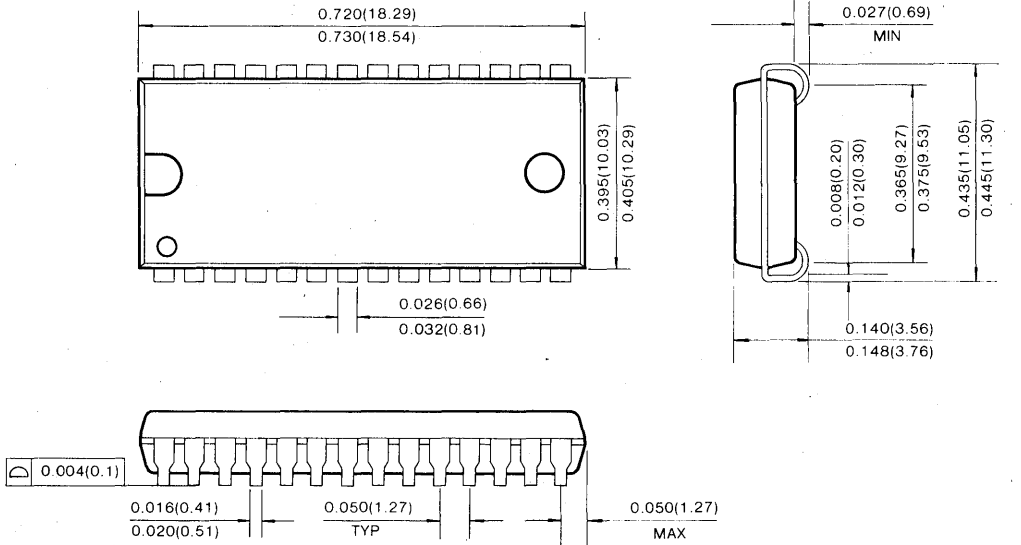
Note: \overline{OE} , Address: Don't Care



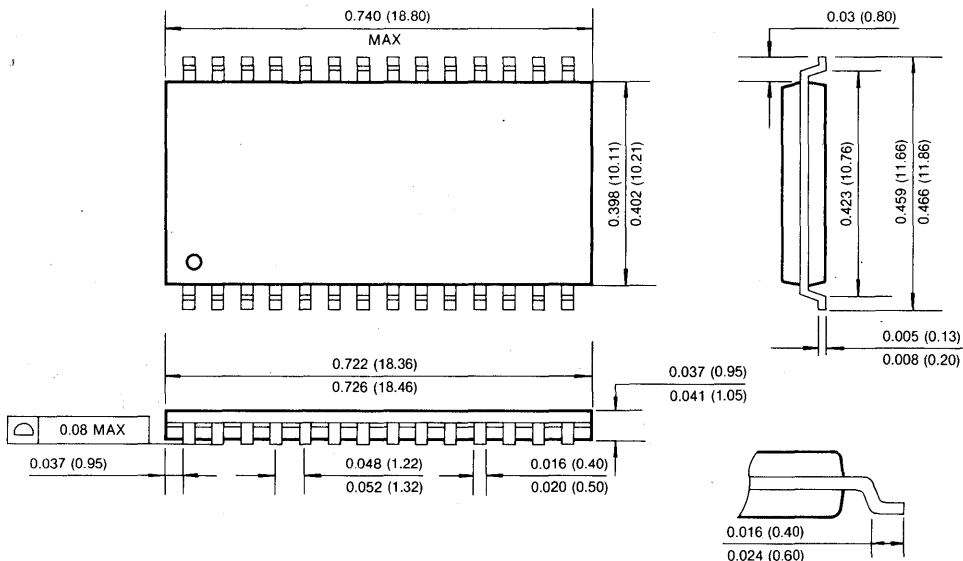
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- Performance range:

	tRAC	tCAC	tRC	tHPC
KM44C4004A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM44C4004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44C4004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44C4004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh operation (LL-ver. only)
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

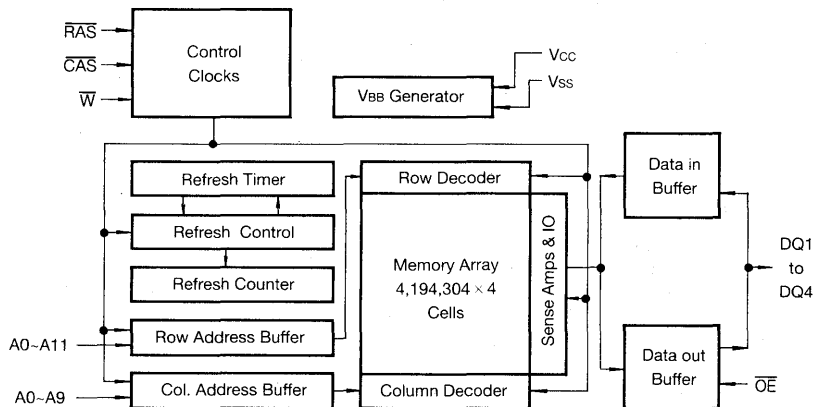
The Samsung KM44C4004A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

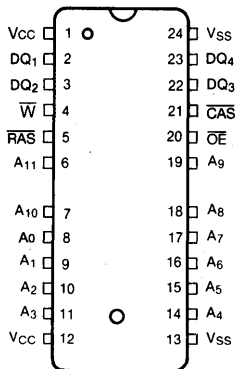
The KM44C4004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



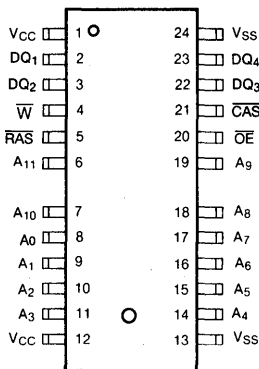
PIN CONFIGURATION (Top Views)

• KM44C4004 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



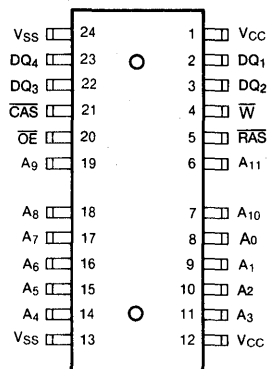
J : 400MIL
K : 300MIL

• KM44C4004 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4004 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC1}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Standby Current (RAS=CAS=W=V _{IH})	KM44C4004A	I _{CC2}	-	2	mA
	KM44C4004AL			1	mA
	KM44C4004ALL			1	mA
	KM44C4004ASL			1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC3}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Hyper Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC4}	-	100	mA
	KM44C4004A/AL/ALL/ASL-6			90	mA
	KM44C4004A/AL/ALL/ASL-7			80	mA
	KM44C4004A/AL/ALL/ASL-8			70	mA
Standby Current (RAS=CAS=W=V _{CC} -0.2V)	KM44C4004A	I _{CC5}	-	1	mA
	KM44C4004AL			300	μA
	KM44C4004ALL			200	μA
	KM44C4004ASL			200	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44C4004A/AL/ALL/ASL-5	I _{CC6}	-	90	mA
	KM44C4004A/AL/ALL/ASL-6			80	mA
	KM44C4004A/AL/ALL/ASL-7			70	mA
	KM44C4004A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DQ1~DQ4=Don't Care trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), tRAS=tRAS ≤ min~300ns	KM44C4004AL	I _{CC7}	-	450	μA
	KM44C4004ASL			350	μA

5



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	KM44C4004ALL	Iccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)		Ii(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)		Io(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)		VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)		VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while RAS=VIL. In Icc4, Address can be changed maximum once within one Hyper page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1-DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 0.5V, See notes 1,2)

Test condition: VIH/VIL=2.4V/0.8V, VOH/VOL=2.0V/0.8V, Output Loading CL=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	3		3		3		3		ns	3
OE to output in Low-Z	tOLZ	3		3		2		3		ns	3
Output buffer turn-off delay from CAS	tCEZ	3	13	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	tT	2	50	2	50	2	50	2	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10K	60	10K	70	10K	80	10K	ns	
RAS hold time	trSH	13		15		20		20		ns	
CAS hold time	tCSH	38		45		50		60		ns	16
CAS pulse width	tcAS	8	10K	10	10K	15	10K	20	10K	ns	4
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	11
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ oprecharge to $\overline{\text{W}}$ delay time	tCPWD	53		60		70		75		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
$\overline{\text{CAS}}$ precharge time (Hyper Page Cycle)	tCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page Cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	

5



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	toEZ	3	13	3	15	3	20	3	20	ns	7
\overline{OE} command hold time	toEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	12
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	twRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	twRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	treZ	3	13	3	15	3	20	3	20	ns	7,16
Output buffer turn off delay from \overline{W}	twEZ	3	13	3	15	3	20	3	20	ns	7
\overline{W} to data delay	twED	15		15		20		20		ns	
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		5		ns	
\overline{RAS} pulse width (LL-ver)	trASS	100		100		100		100		μ s	15
\overline{RAS} precharge time (LL-ver)	trPS	90		110		130		150		ns	15
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from \overline{RAS}	trAC		55		65		75		85	ns	3,4,11
Access time from \overline{CAS}	tcAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	tcAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	18		20		25		25		ns	
\overline{CAS} hold time	tCSH	43		20		55		65		ns	
Column address to \overline{RAS} lead time	trAL	30		35		40		45		ns	
\overline{CAS} to \overline{W} delay time	tcWD	41		45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	78		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	thPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	thPRWC	67		76		91		101		ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS pulse width (Hyper Page Cycle)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tCPA		35		40		45		50	ns	3
OE access time	tOEA		18		20		25		25	ns	
OE to data delay	tOED	18		20		25		25		ns	
OE command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM44C4004A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4

DRAM. \overline{W} and \overline{CAS} before \overline{RAS} Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and \overline{CAS} before \overline{RAS} Refresh Cycle" or \overline{RAS} Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, \overline{W} and \overline{CAS} before \overline{RAS} Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern)

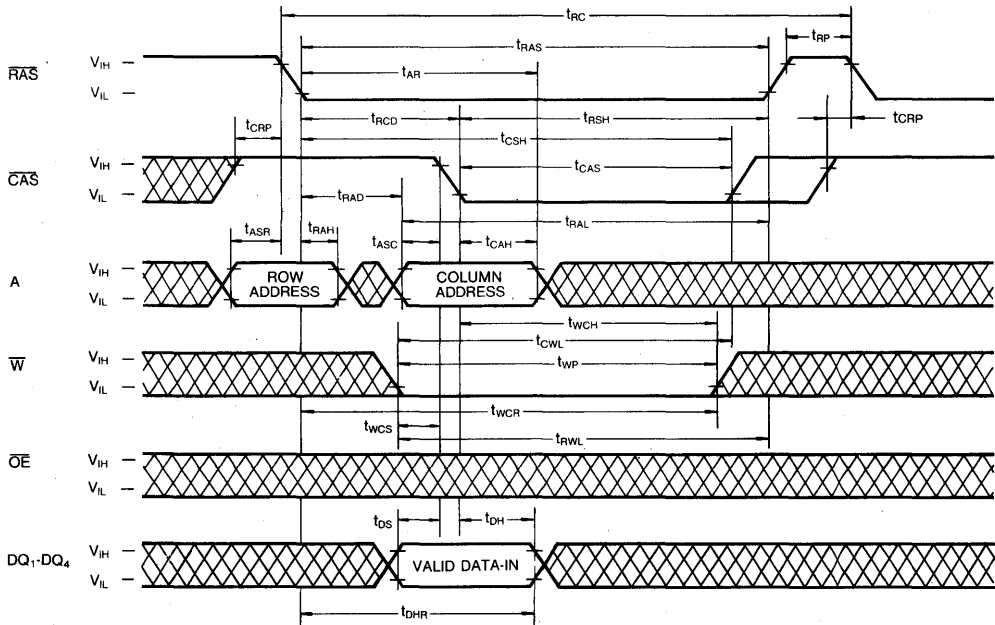
NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC} .
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\text{max})$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{RWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{REZ}(\text{max})$, $t_{CEZ}(\text{max})$, $t_{WEZ}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If \overline{RAS} goes high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going
17. $t_{ASC} \geq t_{CP}(\text{min})$, Assumn $t_T = 2.0\text{ns}$

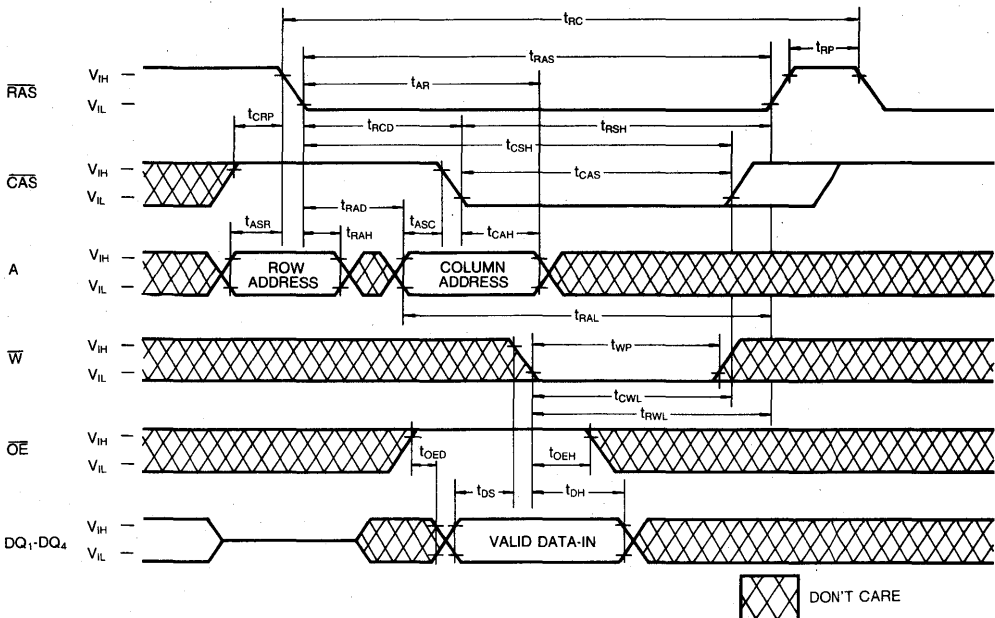


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



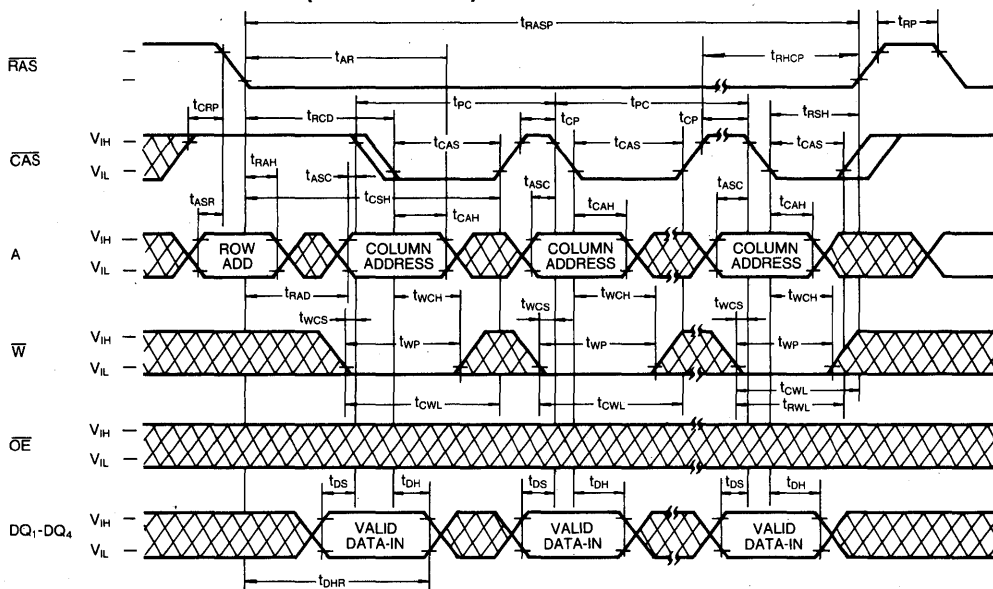
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



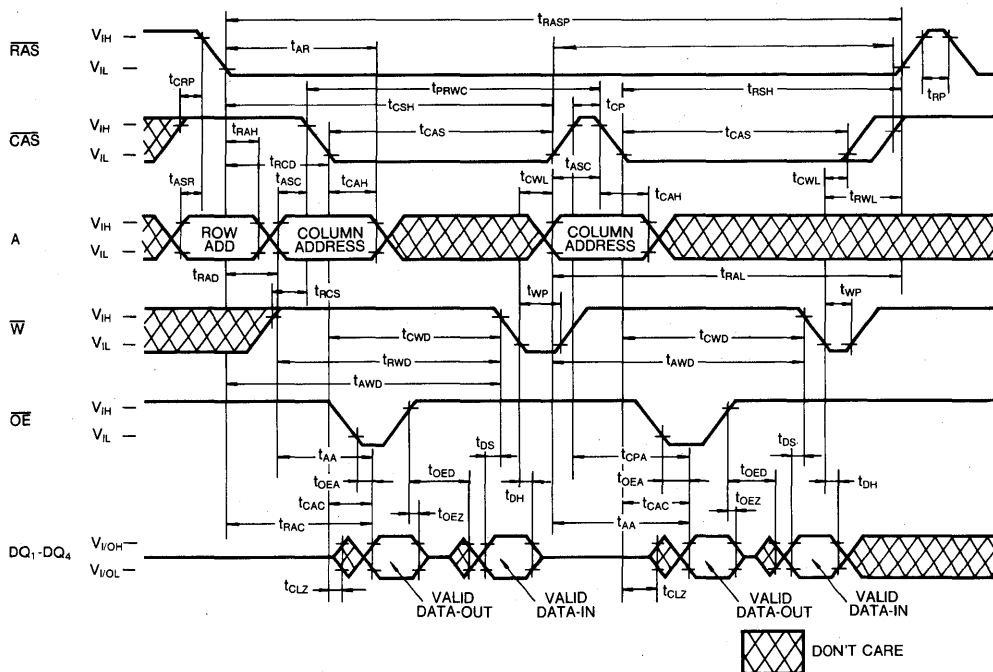
5

TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)

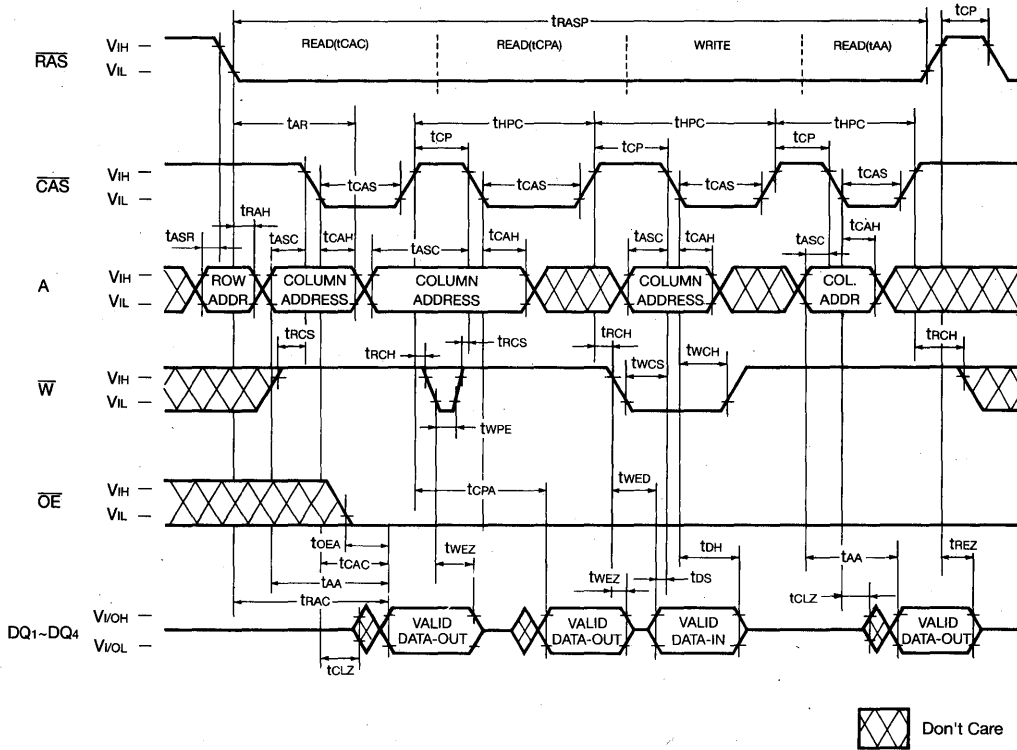


HYPER PAGE READ-MODIFY-WRITE CYCLE

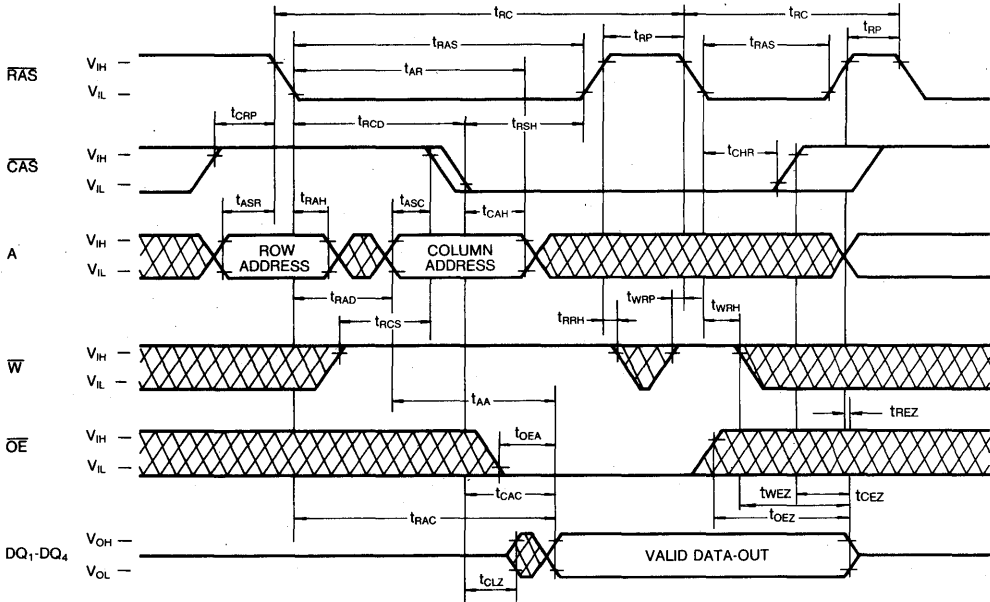


5

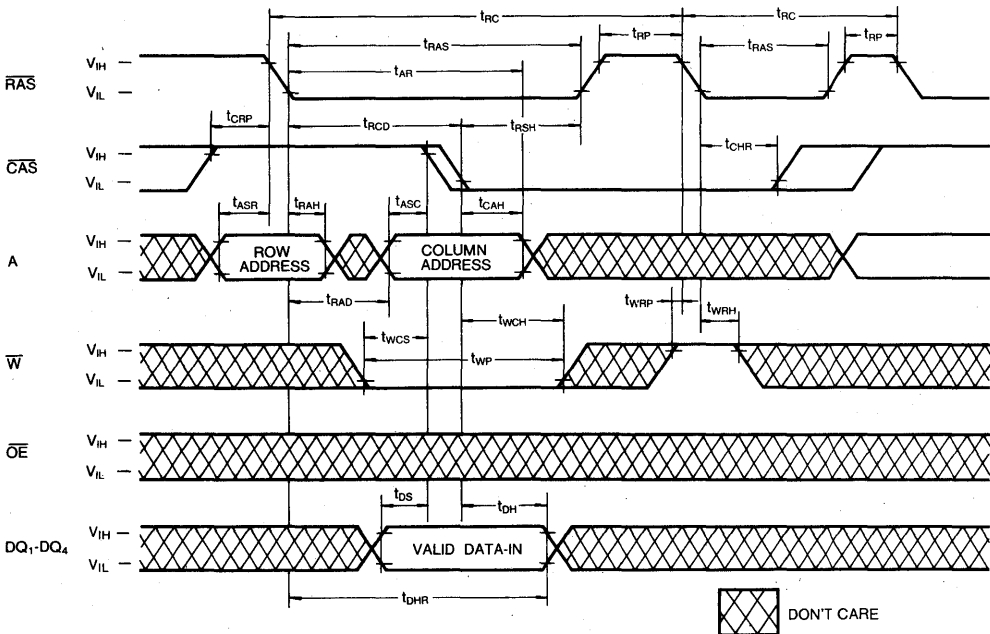
HYPER PAGE READ AND WRITE MIXED CYCLE



TIMING DIAGRAMS (Continued)
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

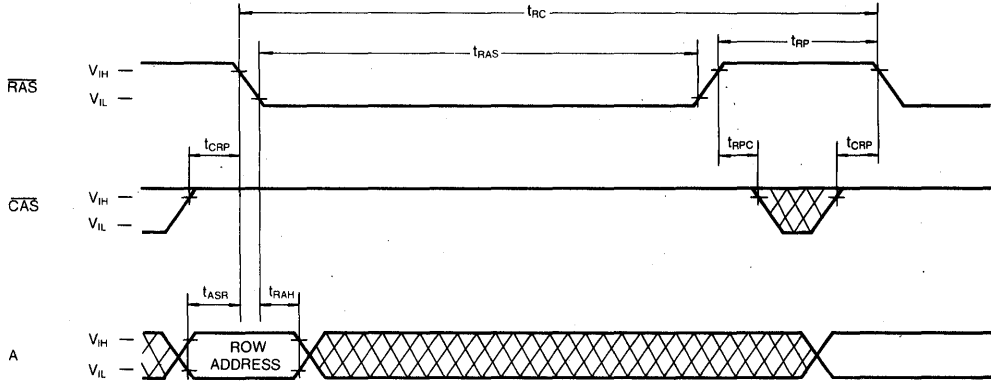


5

TIMING DIAGRAMS (Continued)

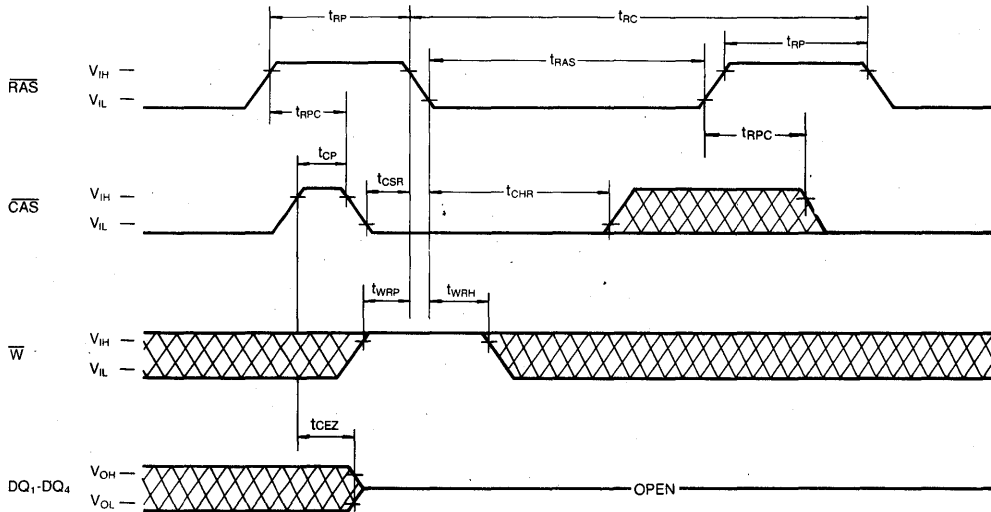
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} =Don't Care



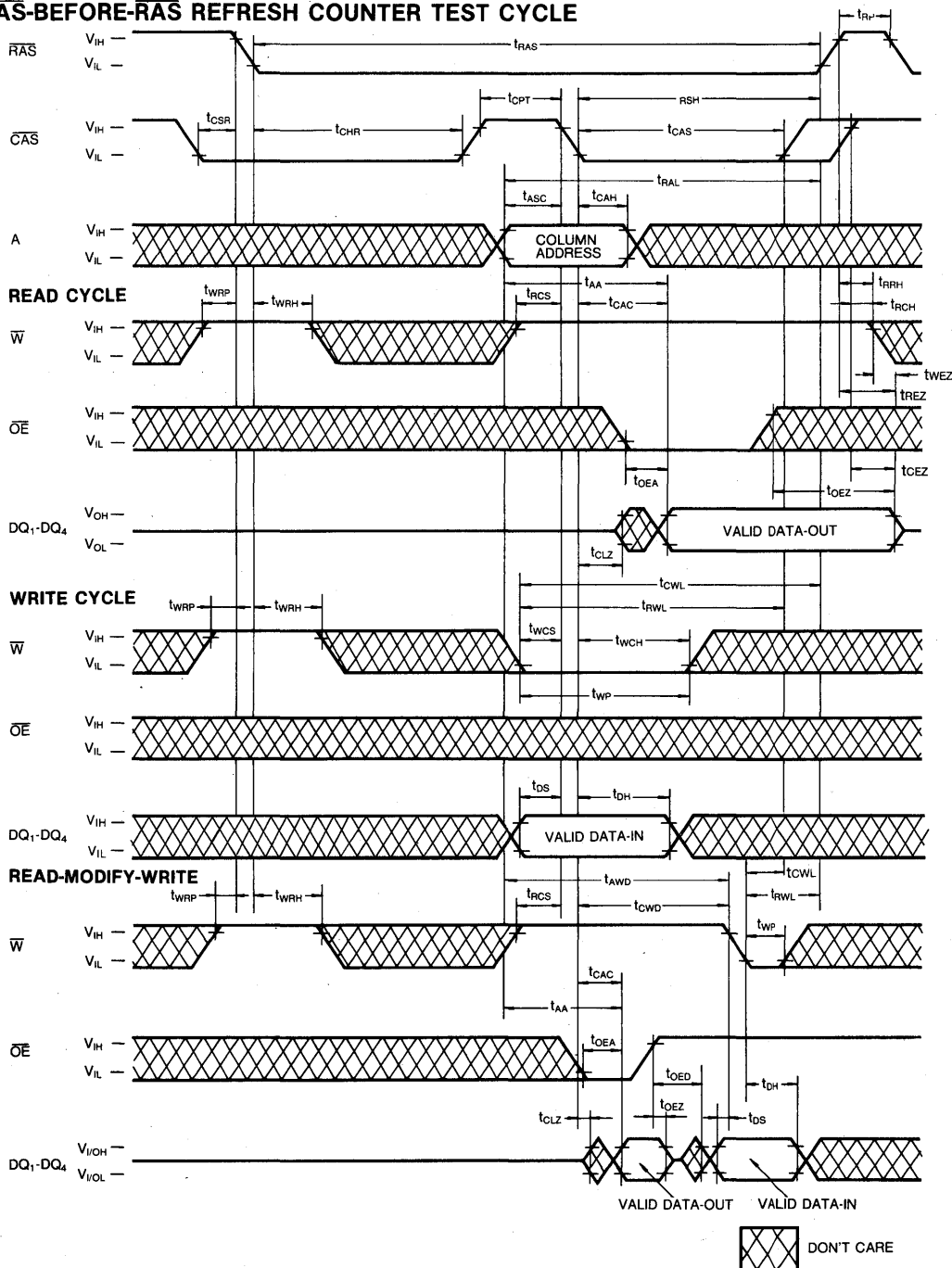
CAS-BEFORE-RAS REFRESH CYCLE

Note: \overline{OE} , Address=Don't Care



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

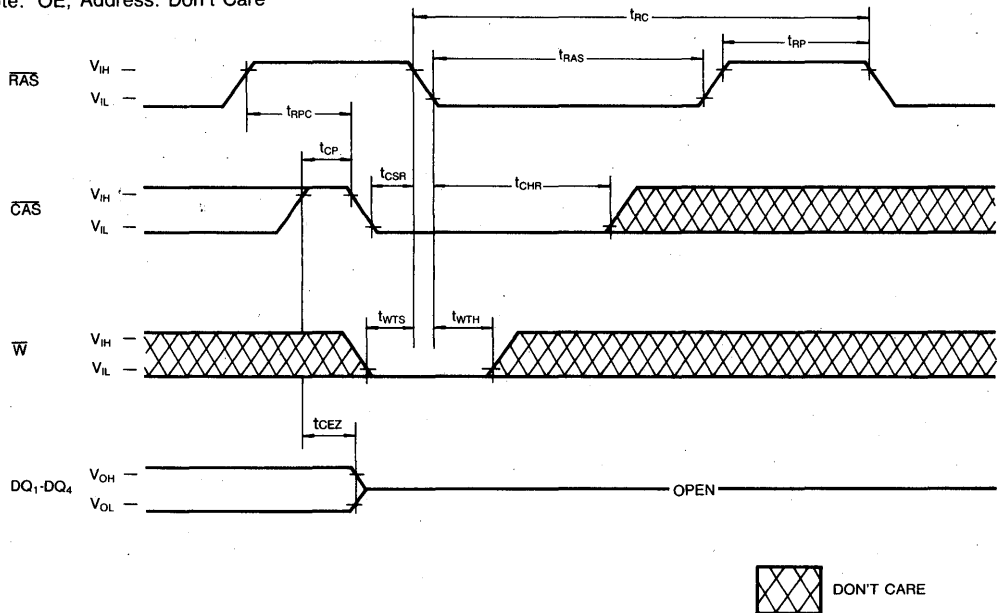


5

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

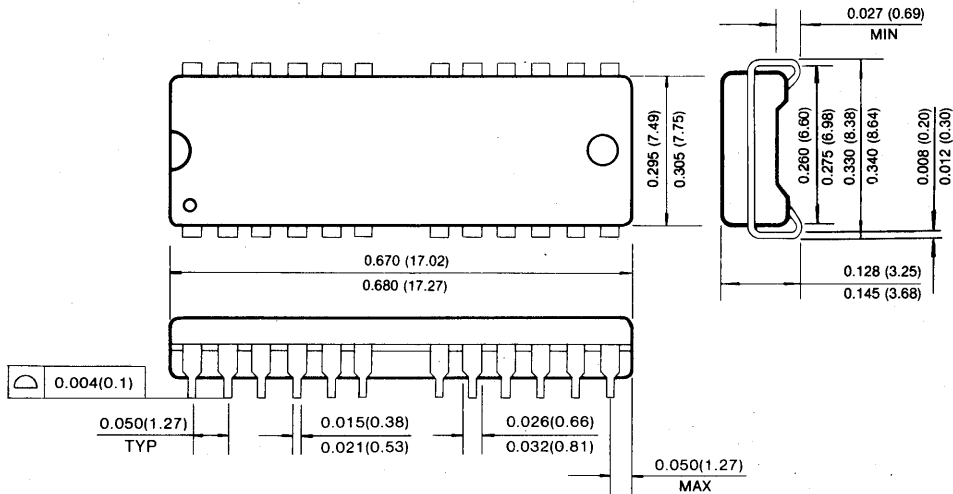
Note: \overline{OE} , Address: Don't Care



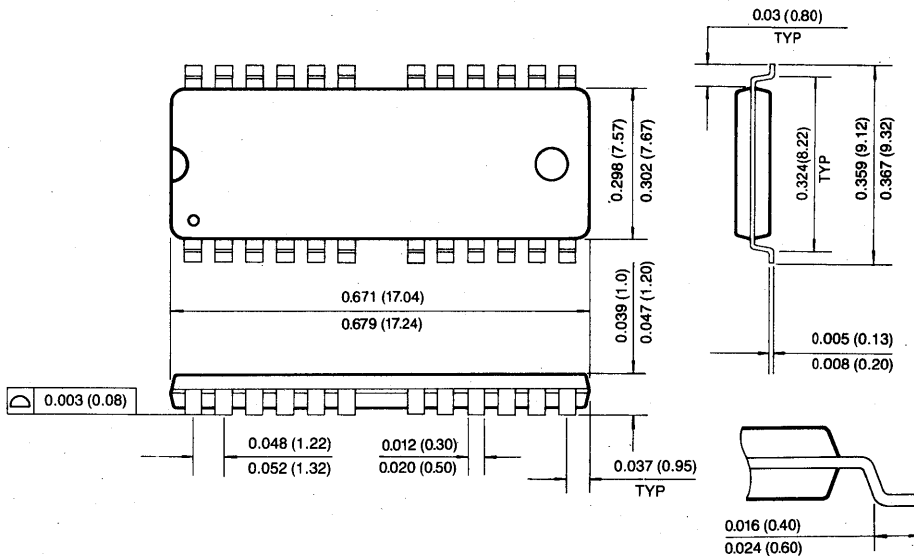
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

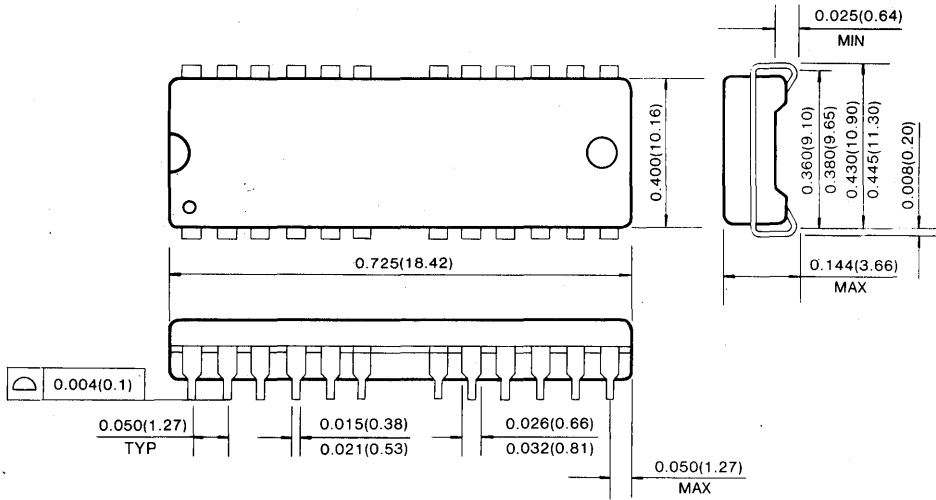


5

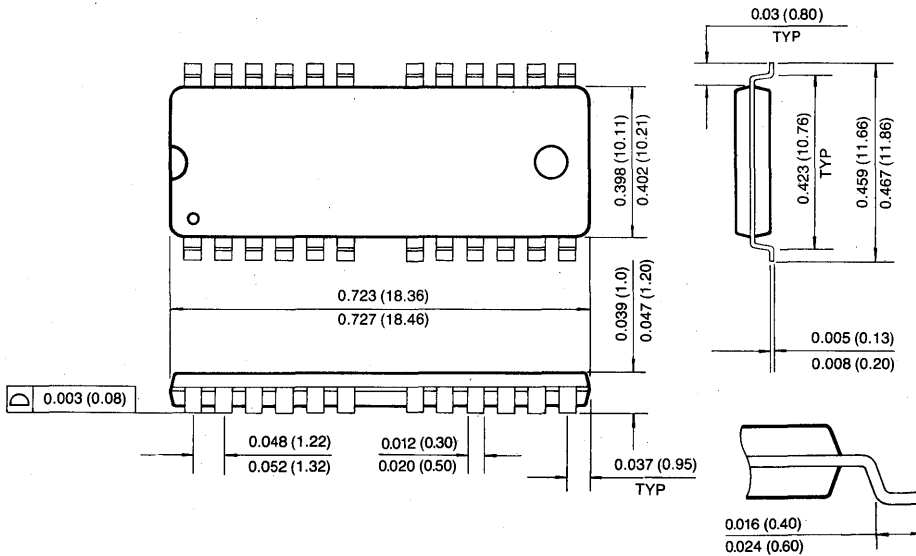
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
KM44C4104A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM44C4104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44C4104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44C4104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- **Fast Page Mode with Extended data out**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Fast parallel test mode Capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Single+5.0V ± 10% power supply**
- **2048 cycles/32ms refresh (Normal)**
- **2048 cycles/128ms refresh (Low power & Self Ref.)**
- **2048 cycles/256ms refresh (Super Low power)**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

GENERAL DESCRIPTION

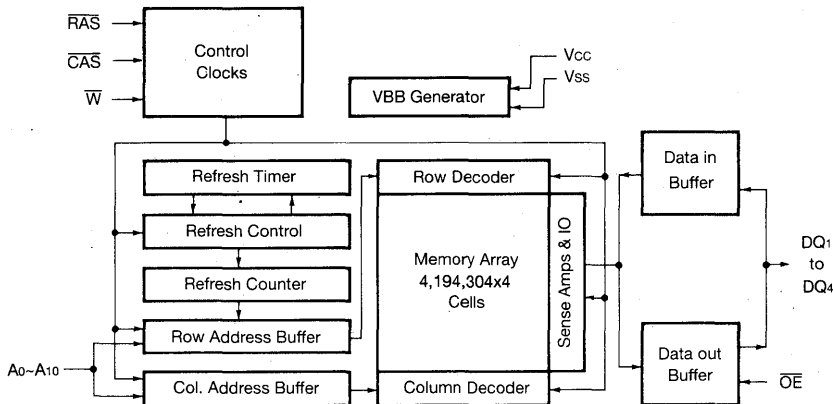
The Samsung KM44C4104A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

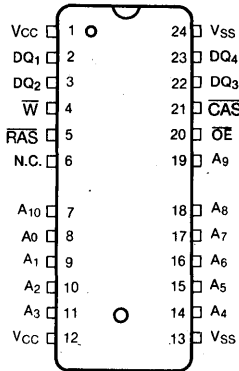
The KM44C4104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



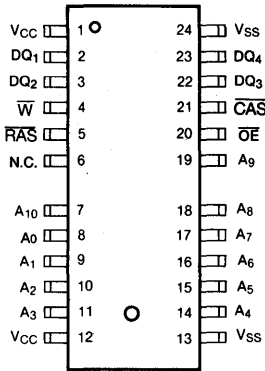
PIN CONFIGURATION (Top Views)

• KM44C4104 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



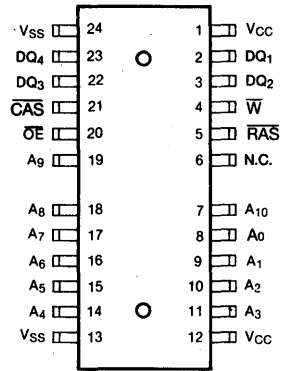
J : 400MIL
K : 300MIL

• KM44C4104 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44C4104 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ t _{RC} =min.)	KM44C4104A/AL/ALL/ASL-5	I _{CC1}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{IH}$)	KM44C4104A	I _{CC2}	-	2	mA
	KM44C4104AL			1	mA
	KM44C4104ALL			1	mA
	KM44C4104ASL			1	mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\overline{\text{CAS}}=V_{IH}$, $\overline{\text{RAS}}$ Cycling @ t _{RC} =min.)	KM44C4104A/AL/ALL/ASL-5	I _{CC3}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{CAS}}$, Address Cycling @ t _{RC} =min.)	KM44C4104A/AL/ALL/ASL-5	I _{CC4}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{CC}-0.2V$)	KM44C4104A	I _{CC5}	-	1	mA
	KM44C4104AL			300	μA
	KM44C4104ALL			200	μA
	KM44C4104ASL			200	μA
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ t _{RC} =min.)	KM44C4104A/AL/ALL/ASL-5	I _{CC6}	-	110	mA
	KM44C4104A/AL/ALL/ASL-6			100	mA
	KM44C4104A/AL/ALL/ASL-7			90	mA
	KM44C4104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V $\overline{\text{CAS}}=\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Cycling or 0.2V DQ1-DQ4=Don't Care t _{RC} =62.5μs(L-Ver.) 125μs(SL-Ver.), t _{TRAS} =t _{TRAS} ≤min-300ns	KM44C4104AL	I _{CC7}	-	400	μA
	KM44C4104ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A10=VCC-0.2V or 0.2V DQ1-DQ4=VCC-0.2V, 0.2V or Open	ICC5	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ VCC+0.5V, all other pins not under test=0 volts.)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ VCC)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, Address can be changed maximum two times while RAS=VIL. In ICC4, Address can be changed maximum once within one Hyper page cycle.

CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A10)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ4)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, VCC=5.0V ± 0.5V, See notes 1,2)

Test condition: VIH/VIL=2.4V/0.8V, VOH/VOL=2.0V/0.8V, Output Loading CL=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	TRC	90		110		130		150		ns	
Read-modify-write cycle time	TRWC	133		155		185		205		ns	
Access time from RAS	TRAC		50		60		70		80	ns	3,4,11
Access time from CAS	TCAC		13		15		20		20	ns	3,4,5
Access time from column address	TAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	TC LZ	3		3		3		3		ns	3
OE to output in Low-Z	TO LZ	3		3		2		3		ns	3
Output buffer turn-off delay from CAS	TCEZ	3	13	3	15	3	20	3	20	ns	7,15
Transition time (rise and fall)	tr	2	50	2	50	2	50	2	50	ns	2
RAS precharge time	TRP	30		40		50		60		ns	
RAS pulse width	TRAS	50	10K	60	10K	70	10K	80	10K	ns	
RAS hold time	TRSH	13		15		20		20		ns	
CAS hold time	TC SH	38		45		50		60		ns	16
CAS pulse width	TCAS	8	10K	10	10K	15	10K	20	10K	ns	4
RAS to CAS delay time	TRCD	20	37	20	45	20	50	20	60	ns	11
RAS to column address delay time	TRAD	15	25	15	30	15	35	15	40	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to RAS	tAR	40		45		55		60		ns	6
Column address to RAS lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to RAS	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to RAS lead time	tRWL	13		15		20		20		ns	
Write command to CAS lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to RAS	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
CAS to W delay time	tCWD	36		40		50		50		ns	8
RAS to W delay time	tRWD	73		85		100		110		ns	8
Column address to W delay time	tAWD	48		55		65		70		ns	8
CAS oprecharge to W delay time	tCPWD	53		60		70		75		ns	8
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		20		30		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
CAS precharge time (Hyper Page Cycle)	tCP	10		10		10		10		ns	
RAS pulse width (Hyper Page Cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	
OE to data delay	tOED	13		15		20		20		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	toEZ	3	13	3	15	3	20	3	20	ns	7
\overline{OE} command hold time	toEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	12
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	twRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	twRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	trEZ	3	13	3	15	3	20	3	20	ns	7,15
Output buffer turn off delay from \overline{W}	twEZ	3	13	3	15	3	20	3	20	ns	7
\overline{W} to data delay	twED	15		15		20		20		ns	
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		5		ns	
\overline{RAS} pulse width (LL-ver)	trASS	100		100		100		100		μ s	16
\overline{RAS} precharge time (LL-ver)	trPS	90		110		130		150		ns	16
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from \overline{RAS}	trAC		55		65		75		85	ns	3,4,11
Access time from \overline{CAS}	trAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	trAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	18		20		25		25		ns	
\overline{CAS} hold time	tCSH	43		20		55		65		ns	
Column address to \overline{RAS} lead time	trAL	30		35		40		45		ns	
\overline{CAS} to \overline{W} delay time	trWD	41		45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	78		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	trPC	25		29		34		39		ns	
Hyper Page read-modify-write cycle time	trPRWC	67		76		91		101		ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS pulse width (Hyper Page Cycle)	trASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tCPA		35		40		45		50	ns	3
OE access time	tOEA		18		20		25		25	ns	
OE to data delay	tOED	18		20		25		25		ns	
OE command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM44C4104A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4

DRAM. \overline{W} and \overline{CAS} before \overline{RAS} Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and " \overline{CAS} before \overline{RAS} Refresh Cycle" or " \overline{RAS} Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " \overline{W} and \overline{CAS} before \overline{RAS} Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time(1/4 in cases of N test pattern)

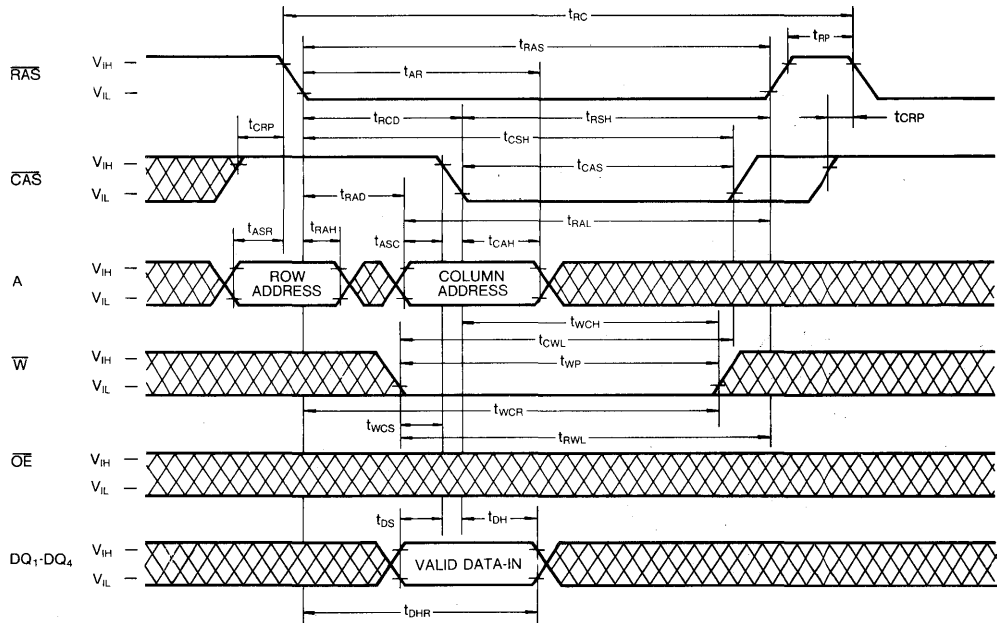
NOTES

- An initial pause of 200µs is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
- Measured with a load equivalent to 2 TTL loads and 100pF
- Operation within the t_{RC}D(max) limit insures that t_{TR}AC(max) can be met. t_{RC}D(max) is specified as a reference point only. If t_{RC}D is greater than the specified t_{RC}D(max) limit, then access time is controlled exclusively by t_{TR}AC.
- Assumes that t_{RC}D ≥ t_{RC}D (max).
- t_{AR}, t_WCR, t_DHR are referenced to t_{TR}AD(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_WCS, t_{TR}WD, t_{TR}CD and t_{TR}WD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If t_WCS ≥ t_WCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{TR}CD ≥ t_{TR}CD(min), t_{TR}WD ≥ t_{TR}WD(min) and t_{TR}WD ≥ t_{TR}WD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either t_{TR}CH or t_{TR}RH must be satisfied for a read cycle.
- These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
- Operation within the t_{TR}AD(max) limit insures that t_{TR}AC(max) can be met. t_{TR}AD(max) is specified as a reference point only. If t_{TR}AD is greater than the specified t_{TR}AD(max) limit, then access time is controlled by t_{AA}.
- These specifications are applied in the test mode.
- In test mode read cycle, the value of t_{TR}AC, t_{AA}, t_{TR}CD is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
- t_{TR}EZ(max), t_{TR}CEZ(max), t_{TR}WEZ(max) and t_{TR}OEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
- If \overline{RAS} goes high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going
- t_{TR}AS ≥ t_{TR}CP (min), Assumn t_{TR}=2.0ns

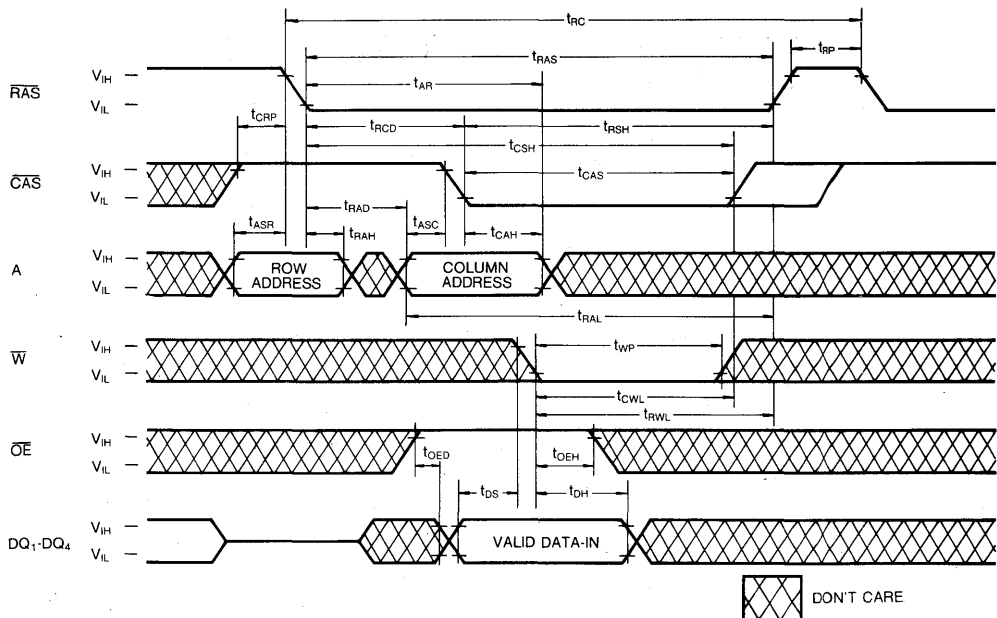


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



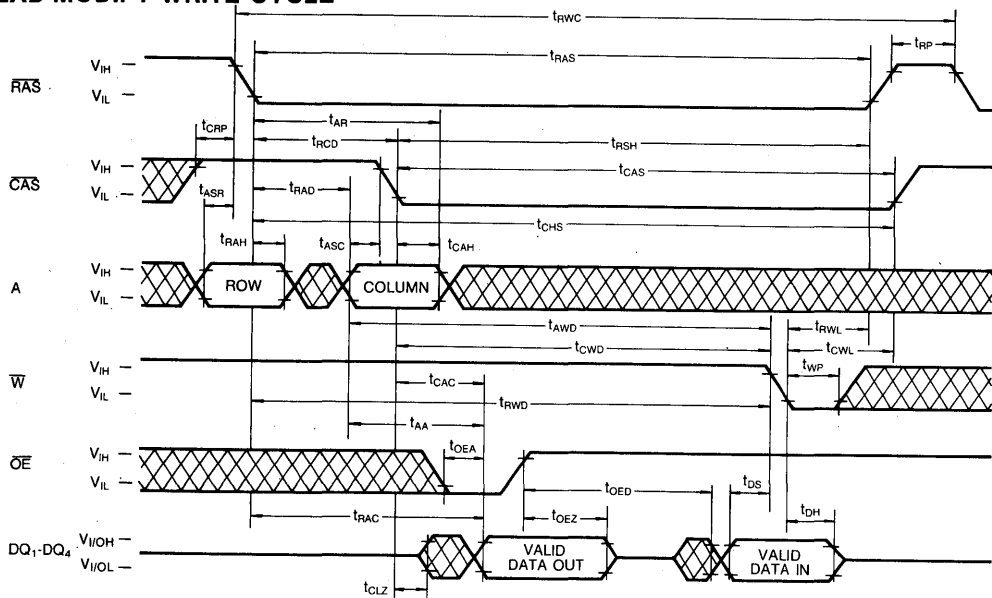
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



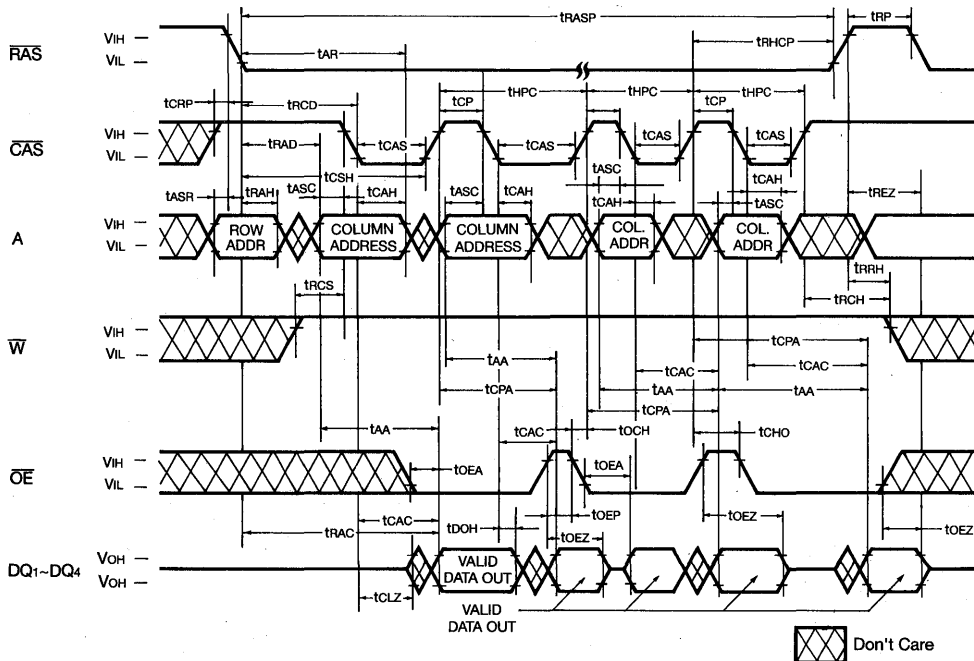
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE

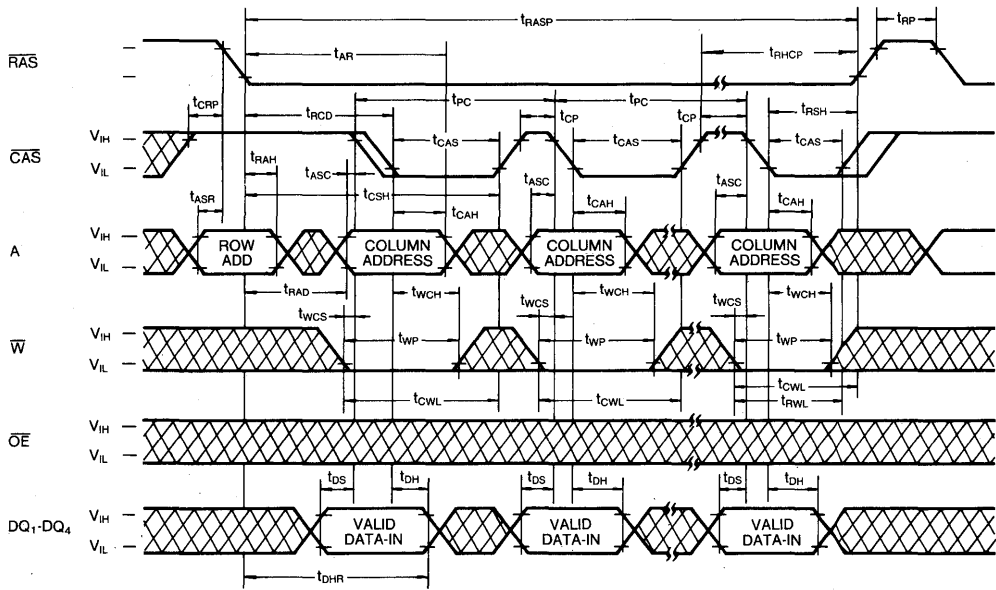


HYPER PAGE READ CYCLE

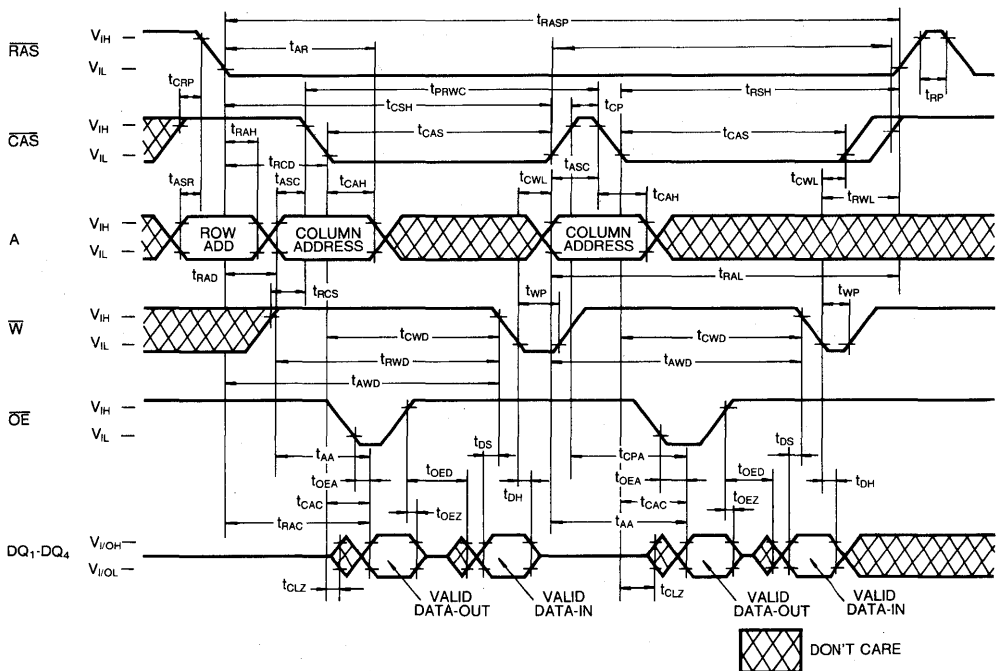


TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)



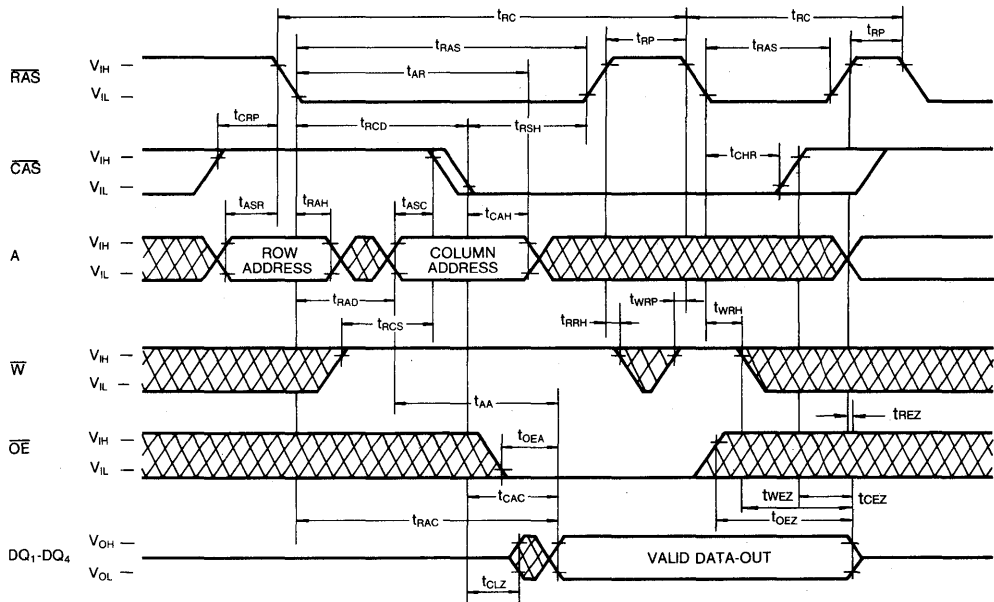
HYPER PAGE READ-MODIFY-WRITE CYCLE



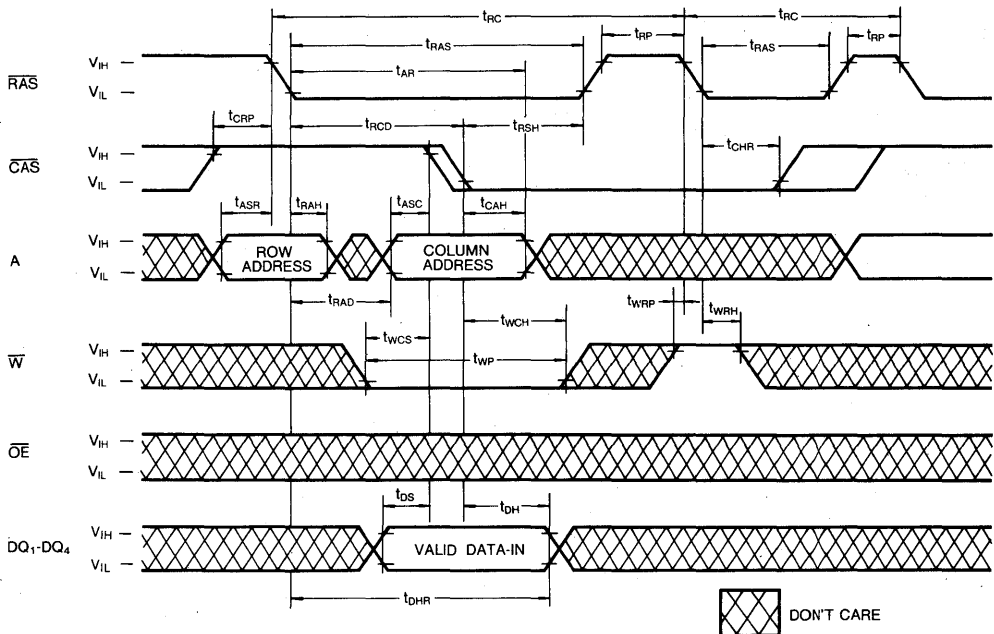
5

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

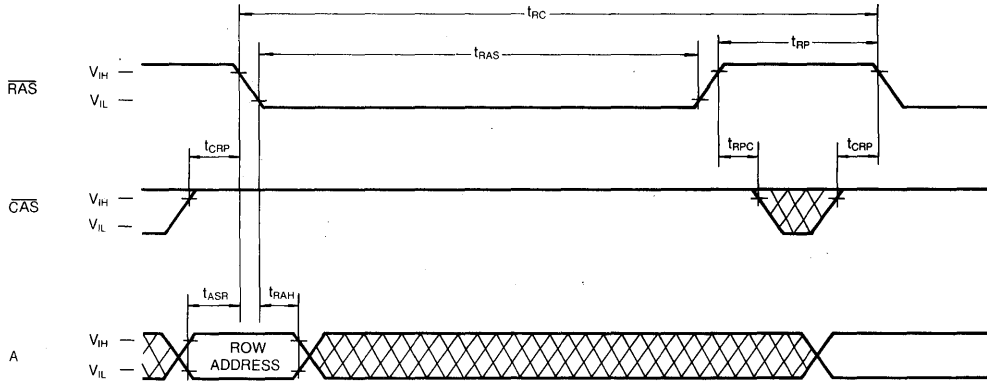


5

TIMING DIAGRAMS (Continued)

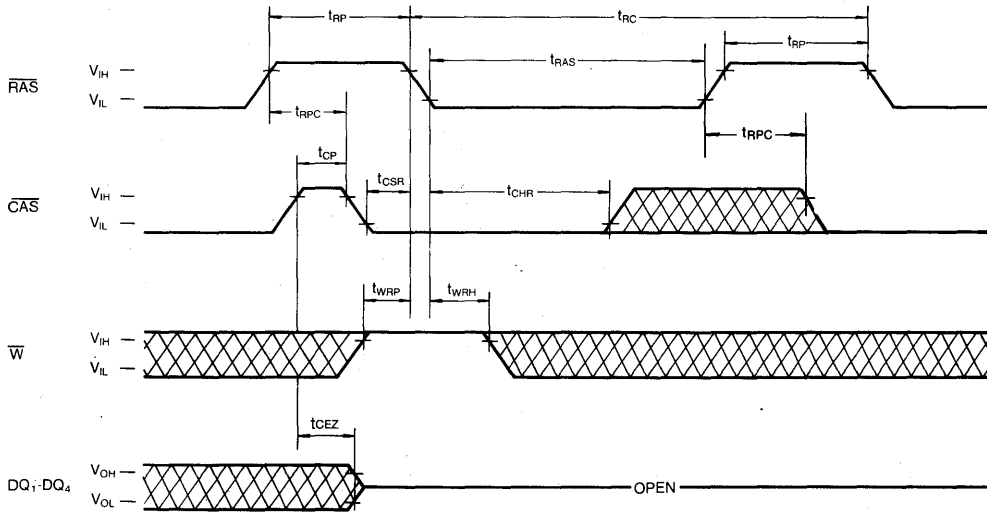
$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE

Note: $\overline{\text{W}}$, $\overline{\text{OE}}$ =Don't Care



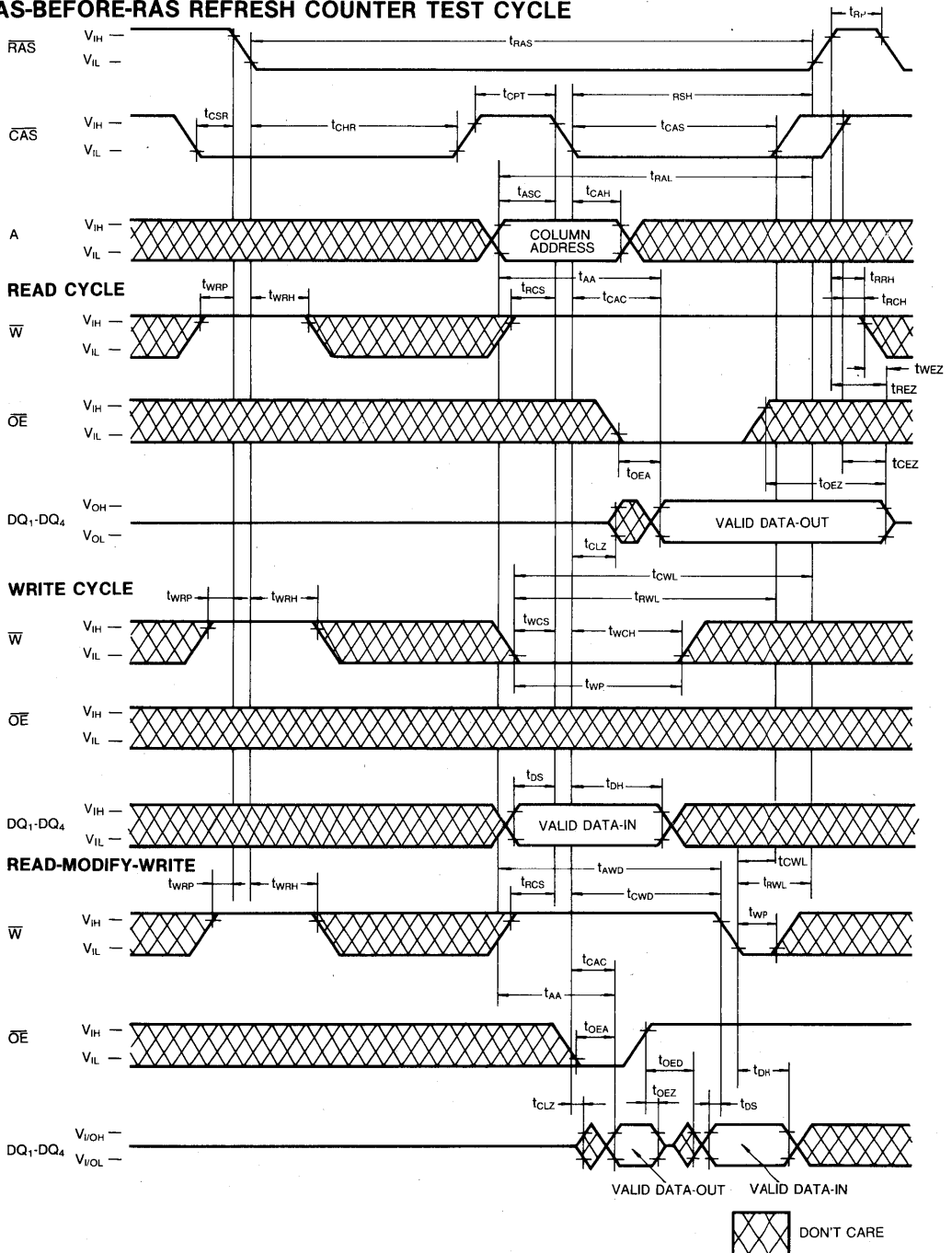
$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH CYCLE

Note: $\overline{\text{OE}}$, Address=Don't Care



TIMING DIAGRAMS (Continued)

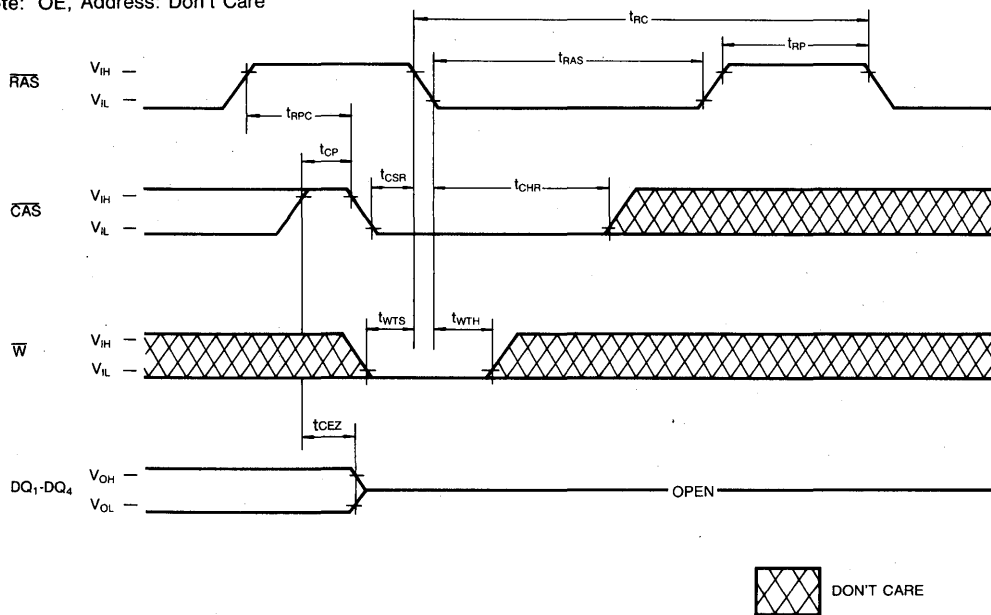
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

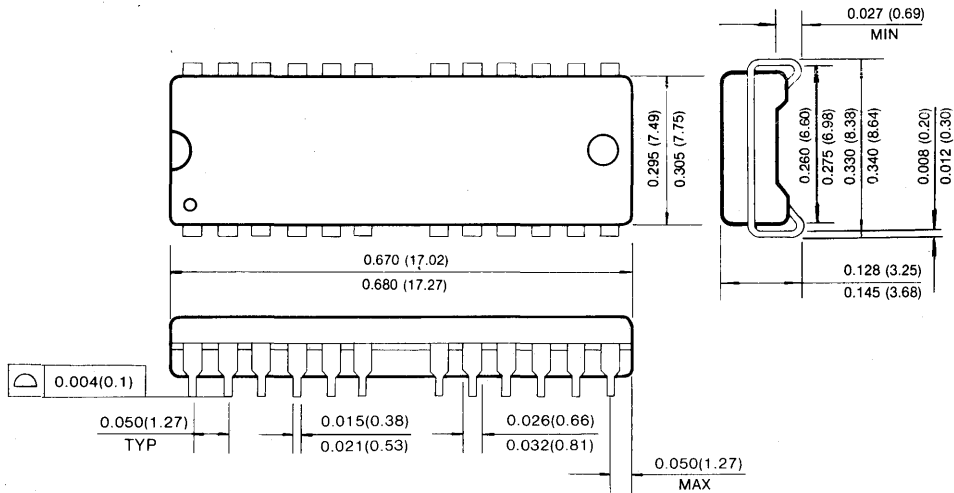
Note: \overline{OE} , Address: Don't Care



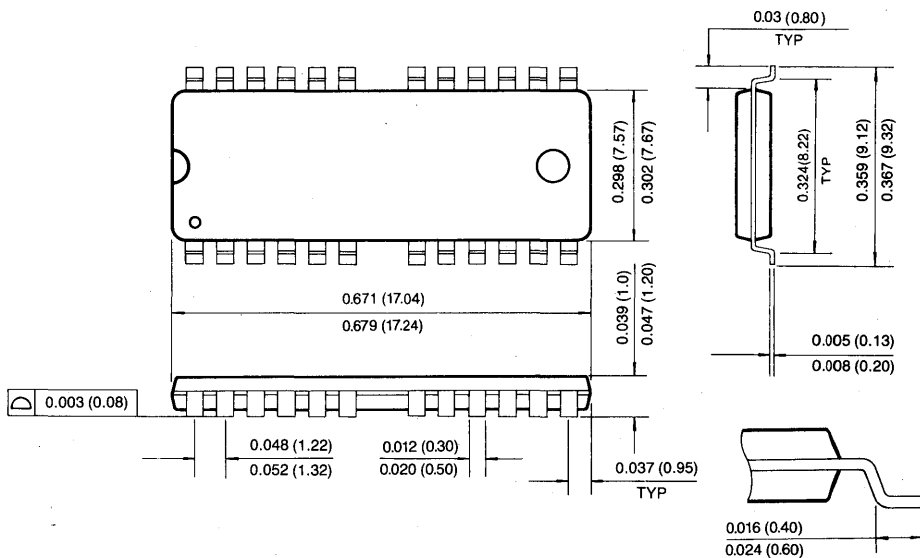
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

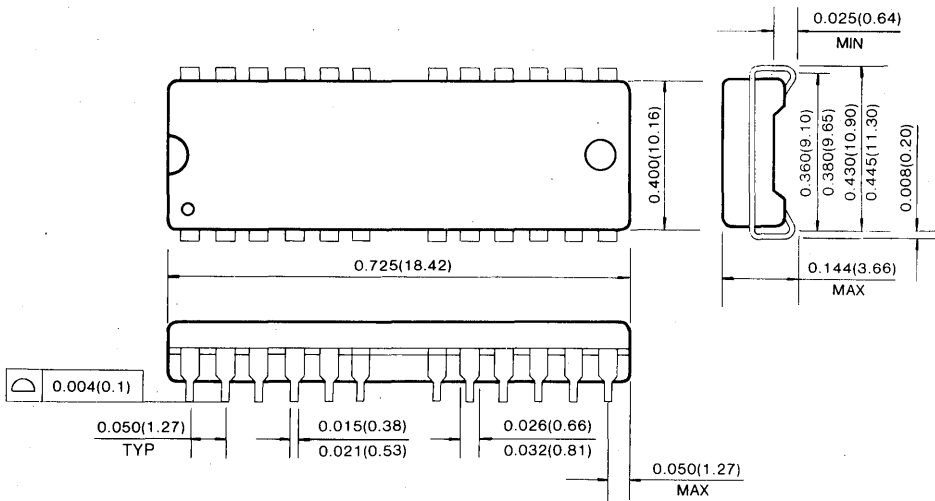


5

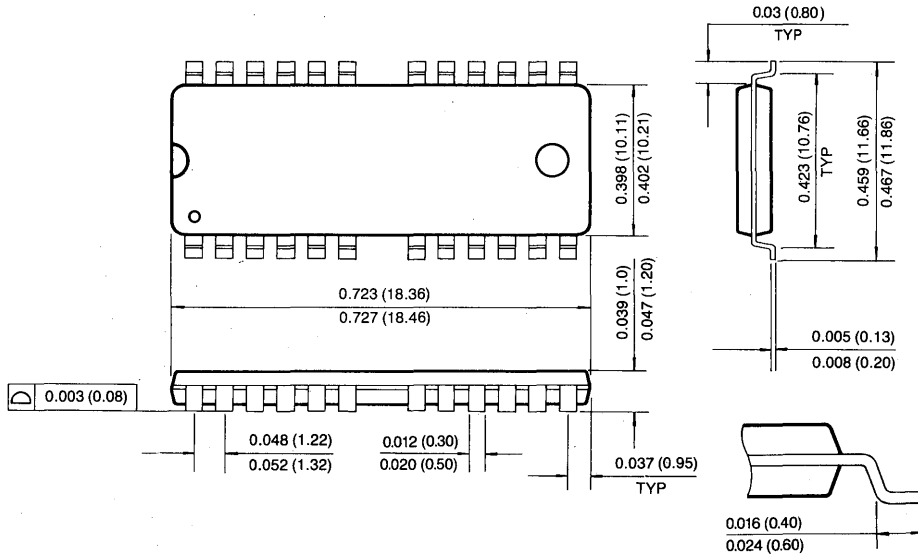
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE
(400MIL, Forward and Reverse Type)



16M × 1 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM41V16000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM41V16000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM41V16000A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Common I/O using Early Write
- Single+3.3V±0.3V power supply
- 4096 cycles/64ms refresh(Normal)
- 4096 cycles/128ms refresh(Low power & Self Ref.)
- 4096 cycles/256ms refresh(Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

GENERAL DESCRIPTION

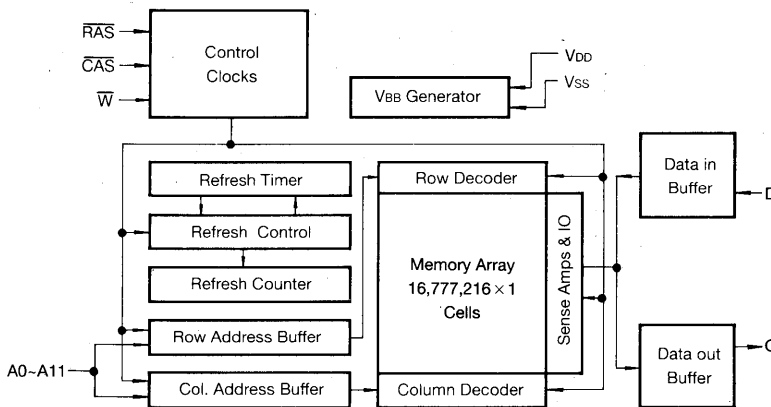
The Samsung KM41V16000A/AL/ALL/ASL is a high speed CMOS 16,777,216 bit × 1 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM41V16000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM41V16000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

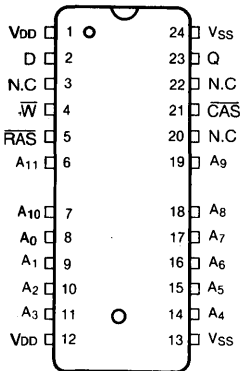


PIN CONFIGURATION (Top Views)

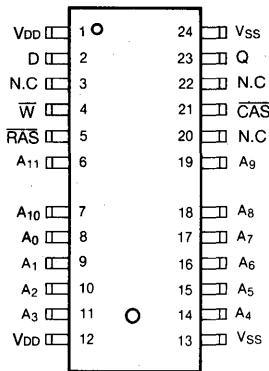
• KM41V16000 AJ/ALJ/ALLJ/ASLJ
/AK/ALK/ALLK/ASLK

• KM41V16000 AT/ALT/ALLT/ASLT
/AS/ALS/ALLS/ASLS

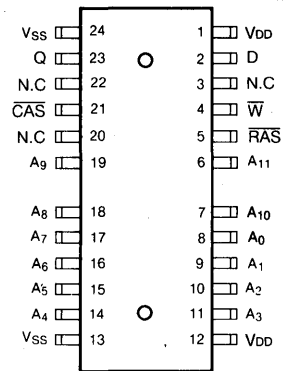
• KM41V16000 ATR/ALTR/ALLTR/ASLTR
/ASR/ALSR/ALLSR/ASLSR



J : 400MIL
K : 300MIL



T : 400MIL(Forward)
S : 300MIL(Forward)



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
D	Data In
Q	Data Out
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
Vcc	Power(+3.3V)
VDD	Ground
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 ~ 4.6	V
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.5 ~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM41V16000A/AL/ALL/ASL-6 KM41V16000A/AL/ALL/ASL-7 KM41V16000A/AL/ALL/ASL-8 I _{CC1}	-	80 70 60	mA mA mA
Standby Current (RAS=CAS=W=V _{IH})	KM41V16000A KM41V16000AL KM41V16000ALL KM41V16000ASL I _{CC2}	-	2 1 1 1	mA mA mA mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM41V16000A/AL/ALL/ASL-6 KM41V16000A/AL/ALL/ASL-7 KM41V16000A/AL/ALL/ASL-8 I _{CC3}	-	80 70 60	mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tPC=min.)	KM41V16000A/AL/ALL/ASL-6 KM41V16000A/AL/ALL/ASL-7 KM41V16000A/AL/ALL/ASL-8 I _{CC4}	-	70 60 50	mA mA mA
Standby Current (RAS=CAS=W=V _{DD} -0.2V)	KM41V16000A KM41V16000AL KM41V16000ALL KM41V16000ASL I _{CC5}	-	1 300 200 200	mA μA μA μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM41V16000A/AL/ALL/ASL-6 KM41V16000A/AL/ALL/ASL-7 KM41V16000A/AL/ALL/ASL-8 I _{CC6}	-	80 70 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V D _{IN} =Don't Care TRC=31.25μS(L-Ver.) 62.5μS(SL-Ver.), TRAS=TRAS min.~300ns	KM41V16000AL KM41V16000ASL I _{CC7}	-	450 350	μA μA
Self Refresh Current RAS=CAS=0.2V W= A ₀ -A ₁₁ =V _{DD} -0.2V or 0.2V D, Q=V _{DD} -0.2V, 0.2V or Open	KM41V16000ALL I _{CC8}	-	250	μA

5

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	$I_{(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{O(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , Address can be changed maximum two times while $RAS = V_{IL}$. In I_{CC4} , Address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	-	7	pF
Input Capacitance (A0-A11)	C_{IN2}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W})	C_{IN3}	-	7	pF
Input Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Test Condition : $V_{ih}/V_{il} = 2.0V/0.8V$, $V_{oh}/V_{ol} = 2.0V/0.8V$, Output Loading $C_L = 100pF$

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t _{AR}	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		40		ns	
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	9
Write command hold time	t _{WCH}	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	t _{WCR}	45		55		60		ns	6
Write command pulse width	t _{WP}	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	15		20		20		ns	
Data set-up time	t _{DS}	0		0		0		ns	10
Data hold time	t _{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	45		55		60		ns	6
Refresh period (Normal)	t _{REF}		64		64		64	ms	
Refresh period (Low power & self Ref.)	t _{REF}		128		128		128	ms	
Refresh period (Super Low power)	t _{REF}		256		256		256	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	15		20		20		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	60		70		80		ns	8
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	30		35		40		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	t _{CPT}	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40		45	ns	3
Fast Page mode cycle time	t _{PC}	40		45		50		ns	
Fast Page mode read-modify-write cycle time	t _{PRWC}	60		70		75		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	t _{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	35		40		45		ns	
Write command set-up time (Test mode in)	t _{WTS}	10		10		10		ns	
Write command hold time (Test mode in)	t _{WTH}	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	t _{WRP}	10		10		10		ns	
$\overline{\text{W}}$ to $\overline{\text{RAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	t _{WRH}	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	t _{RASS}	100		100		100		μs	15
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	t _{RPS}	110		130		150		ns	15
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ refresh)	t _{CHS}	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

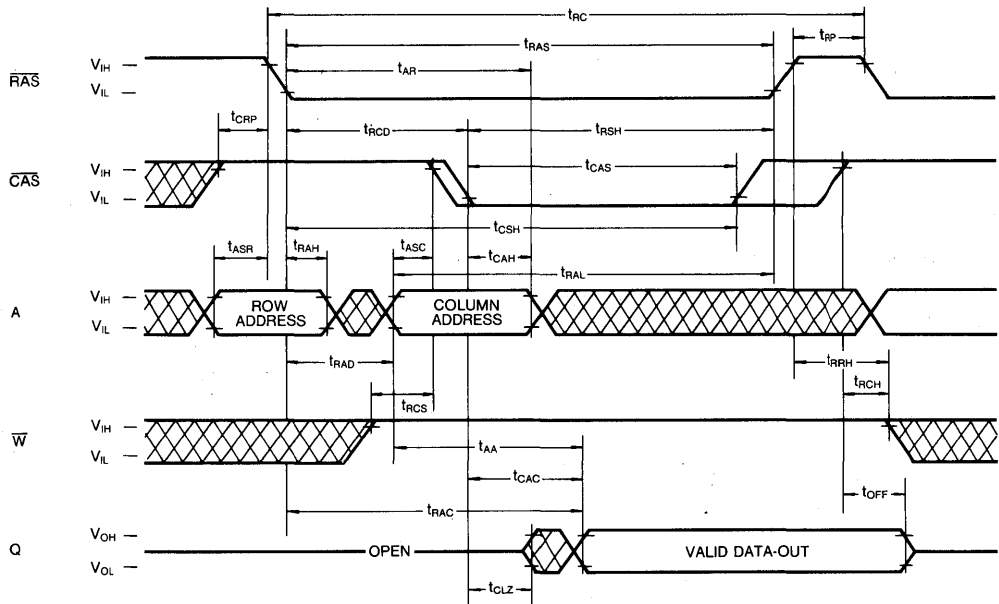
Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	115		135		155		ns	
Read-modify-write cycle time	trwc	160		190		210		ns	
Access time from RAS	trac		65		75		85	ns	3,4,11
Access time from CAS	tcac		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
RAS pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
CAS pulse width	tcAS	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	trSH	20		25		25		ns	
CAS hold time	tCSH	65		75		85		ns	
Column address to RAS lead time	trAL	35		40		45		ns	
CAS to \bar{W} delay time	tcWD	20		25		25		ns	8
RAS to \bar{W} delay time	trWD	65		75		85		ns	8
Column address to \bar{W} delay time	tAWD	35		40		45		ns	8
Fast Page mode cycle time	tpc	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tpRWC	65		75		80		ns	
RAS pulse width (Fast Page Mode)	trASP	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tCPA		40		45		50	ns	3

NOTES

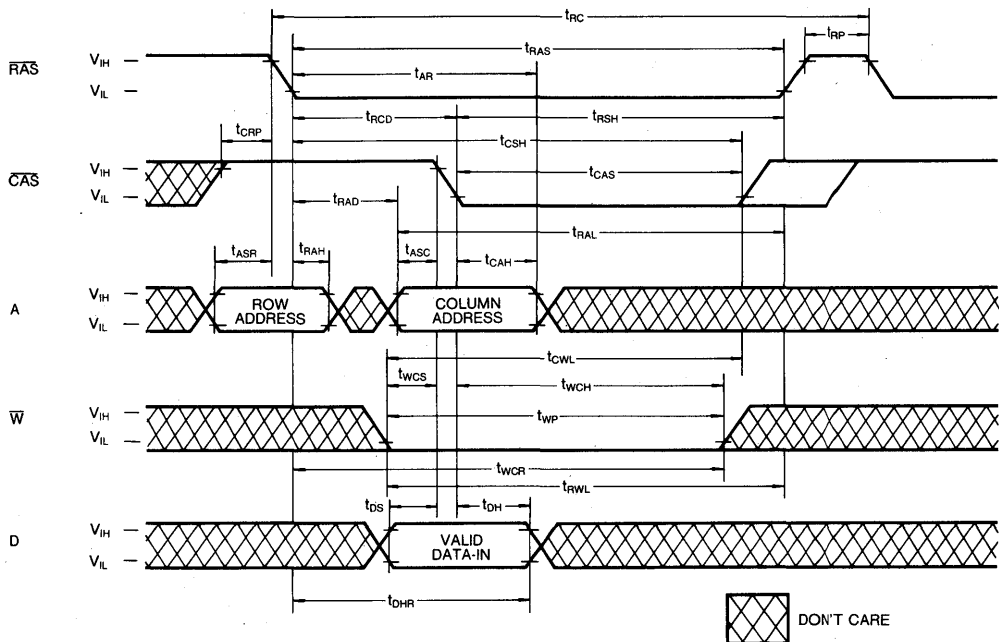
- An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{OUT}=2mA), V_{ol}=0.8V(I_{OUT}=2mA)
- Operation within the trCD(max) limit insures that trAC(max) can be met. trCD(max) is specified as a reference point only. If trCD is greater than the specified trCD(max) limit, then access time is controlled exclusively by tAC.
- Assumes that trCD \geq trCD (max).
- tAR, tWCR, tDHR are referenced to trAD(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- twCS, trWD, tcWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If twCS \geq twCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcWD \geq tcWD(min), trWD \geq trWD(min) and tAWD \geq tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either trCH or trRH must be satisfied for a read cycle.
- These parameters are referenced to the $\bar{C}AS$ leading edge in early write cycles and to the \bar{W} leading edge in read-write cycles.
- Operation within the trAD(max) limit insures that trAC(max) can be met. trAD(max) is specified as a reference point only. If trAD is greater than the specified trAD(max) limit, then access time is controlled by tAA.
- These specifications are applied in the test mode.
- In test mode read cycle, the value of trAC, tAA, tcAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
- tOFF(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

READ CYCLE



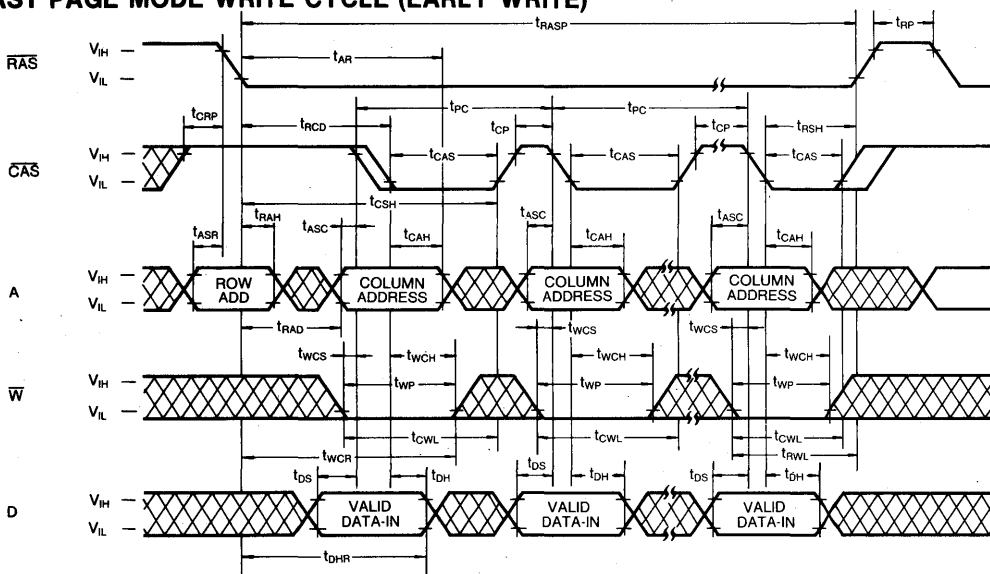
WRITE CYCLE (EARLY WRITE)



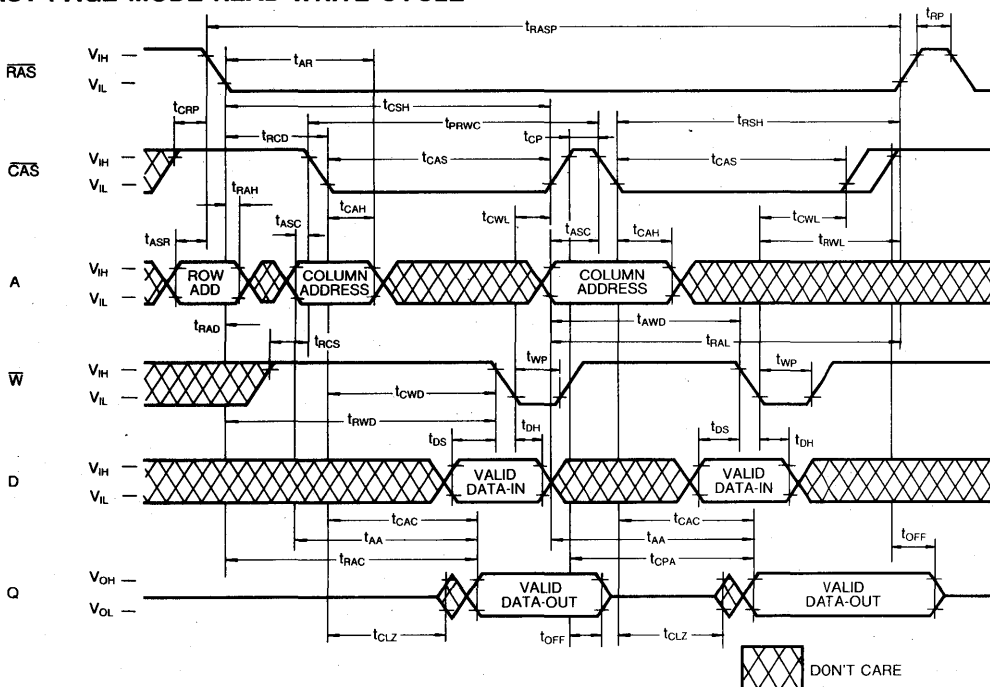
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



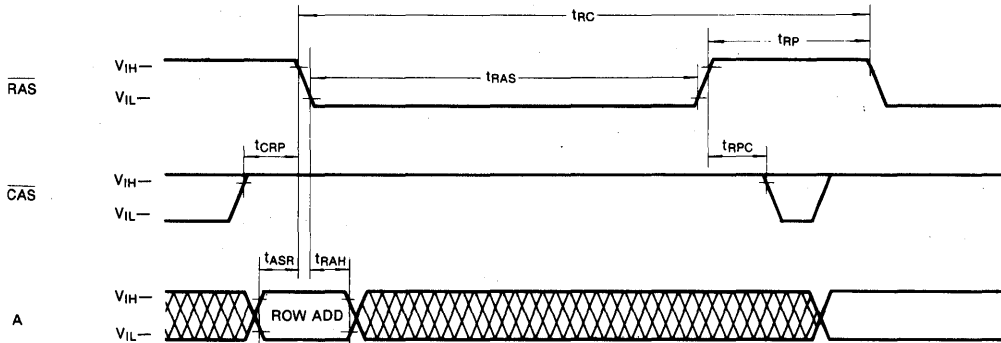
FAST PAGE MODE READ-WRITE CYCLE



TIMING DIAGRAMS (Continued)

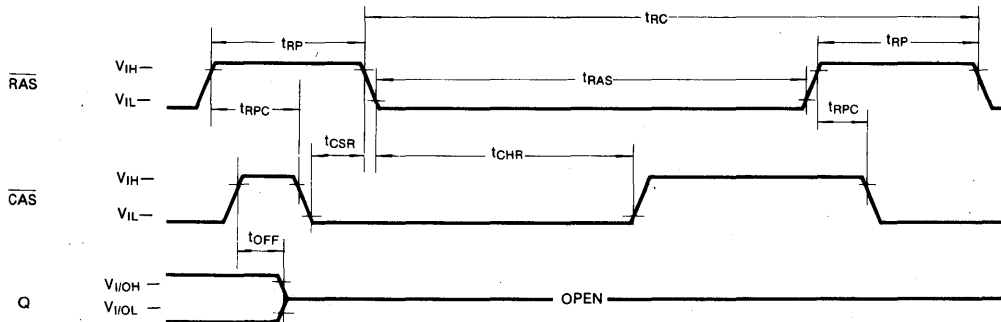
RAS-ONLY REFRESH CYCLE

Note: \bar{W} = Don't care



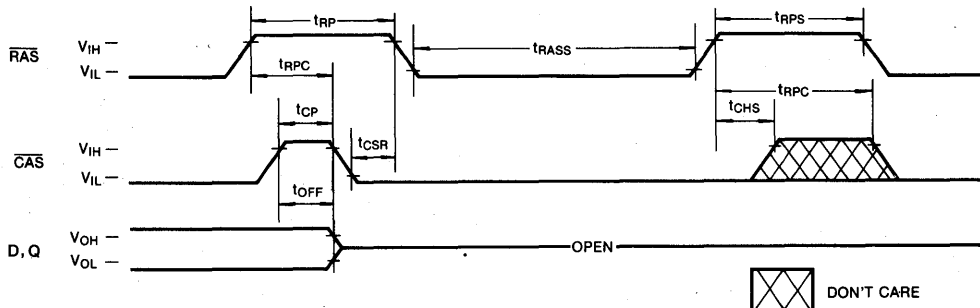
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\bar{W} = V_{IH}$, A = Don't Care



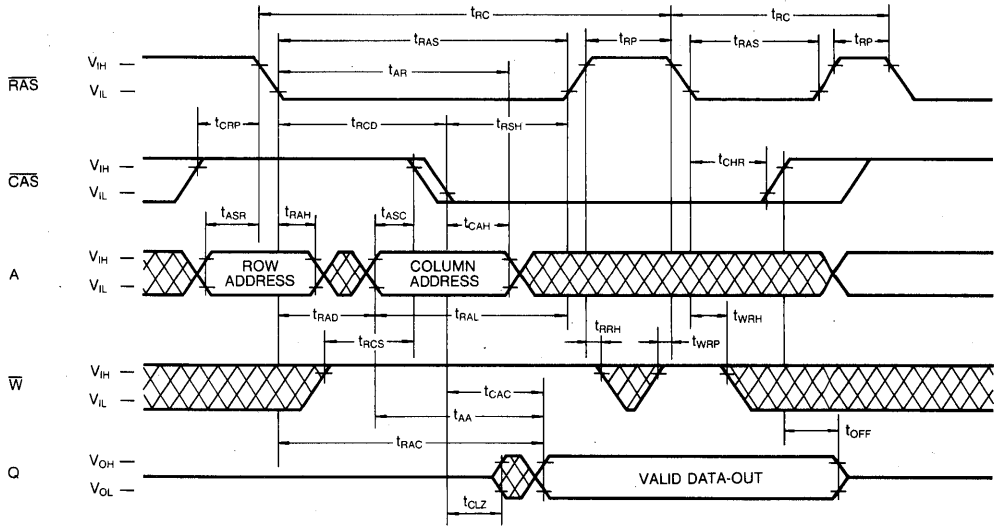
CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

NOTE: \bar{W} , A = Don't Care

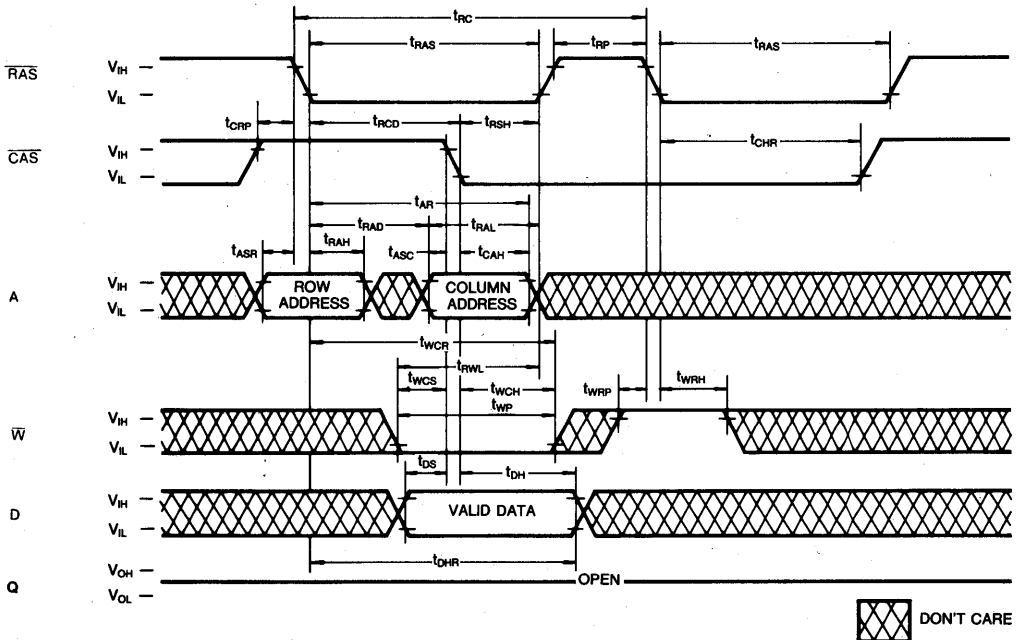


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



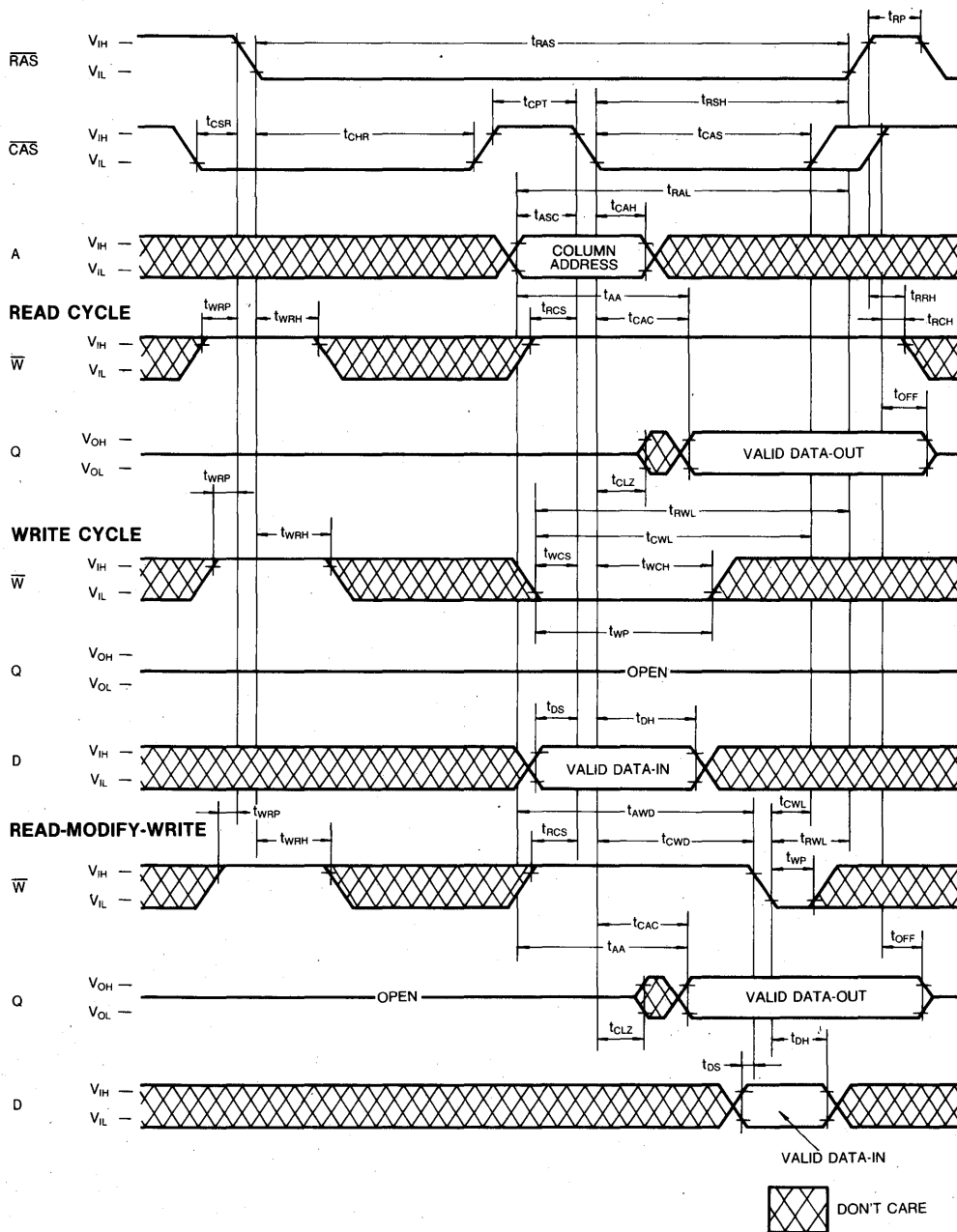
HIDDEN REFRESH CYCLE (WRITE)



5

TIMING DIAGRAMS (Continued)

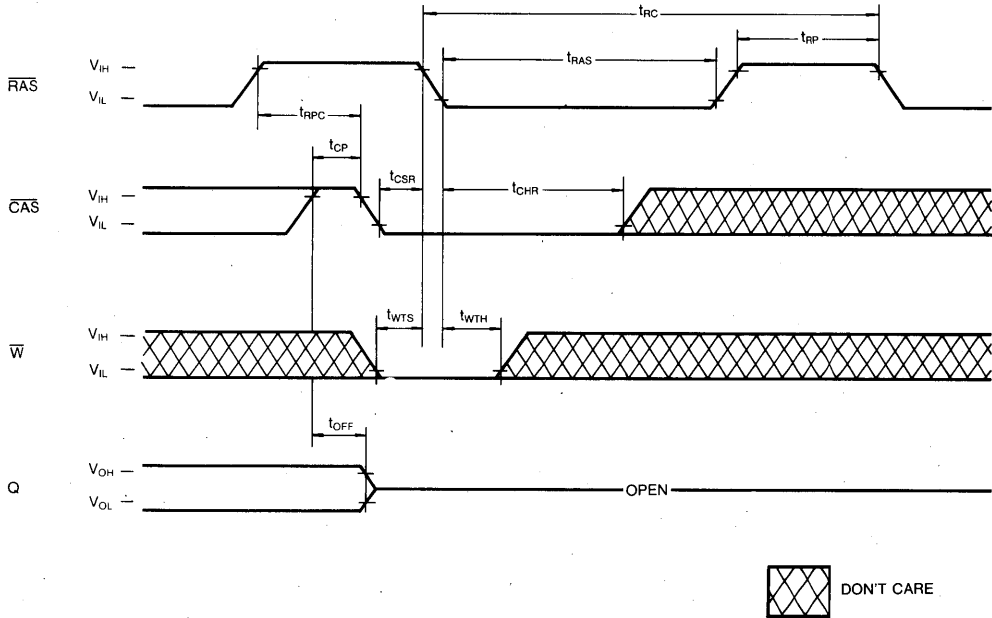
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: D, Address: Don't Care



5

TEST MODE DESCRIPTION

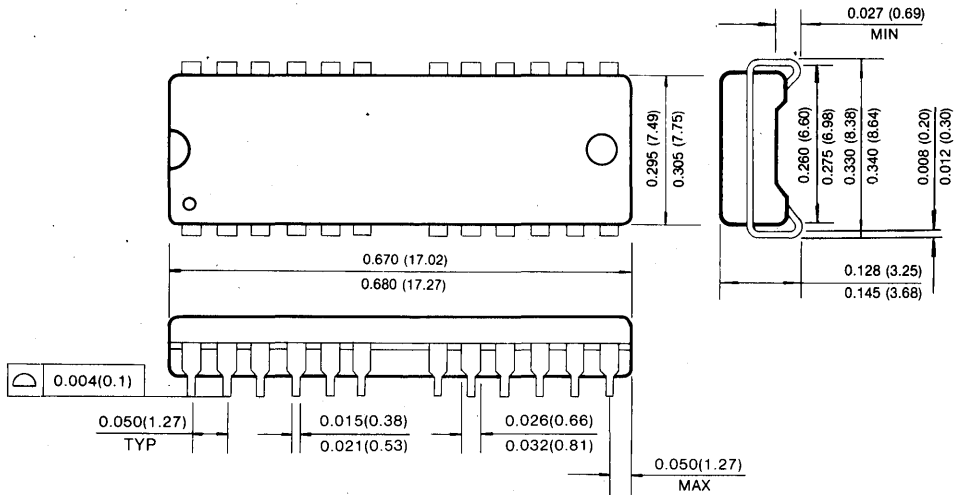
The KM41V16000A/AL/ALL/ASL is the RAM organized 16,777,216 words by 1 bit, it is internally organized 1, 048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0, A1, A10 and A11 are not used. If, upon reading, 16 bits are equal (all "1"s or "0"s) the Q pin indicates a "1". If they were not equal, the Q pin would indicate a "0". In

"Test Mode", the 16M DRAM can be tested as if it were a 1M x 1 DRAM. $\overline{\text{W}}$, $\overline{\text{CAS-BEFORE-RAS}}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " $\overline{\text{CAS-BEFORE-RAS}}$ REFRESH CYCLE" or " $\overline{\text{RAS}}$ -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/16 in cases of N test pattern).

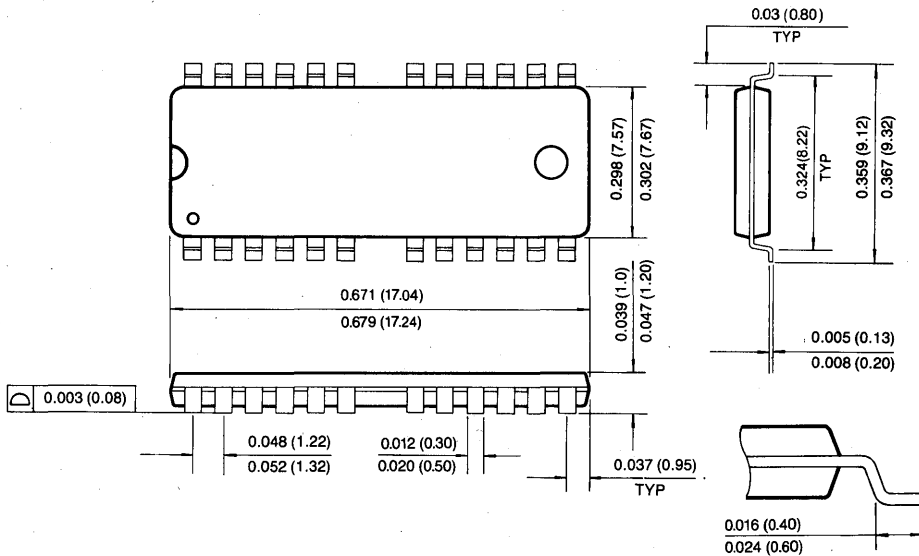
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



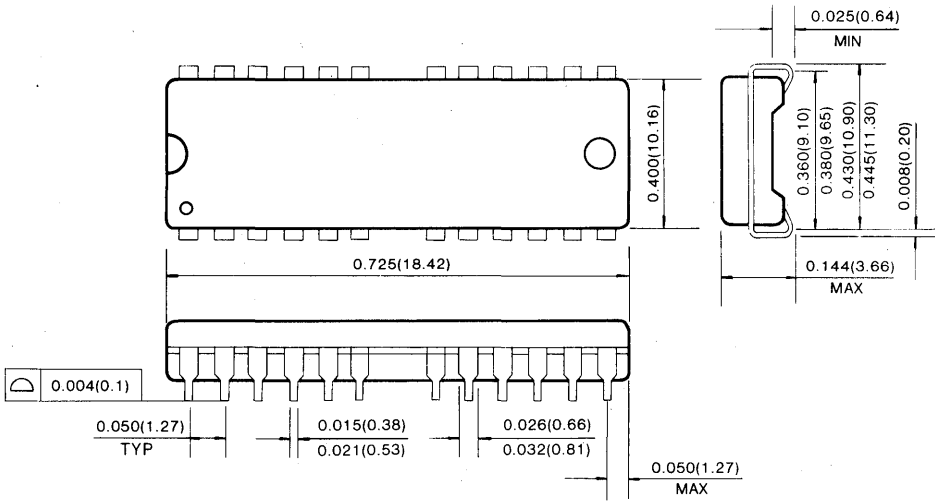
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



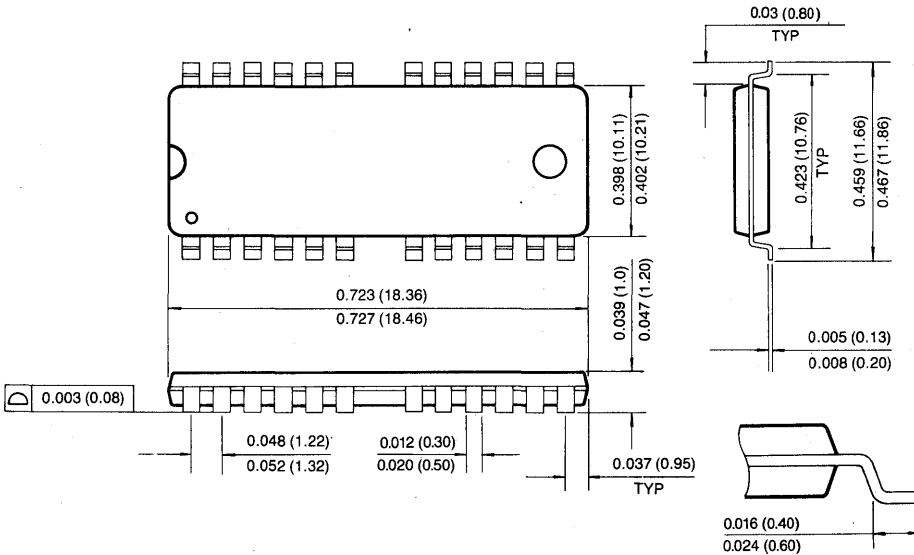
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



5

4M x 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{TRC}
KM44V4000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44V4000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44V4000A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single +3.3V ± 0.3V power supply
- 4096 cycles/64ms refresh (Normal DRAM)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

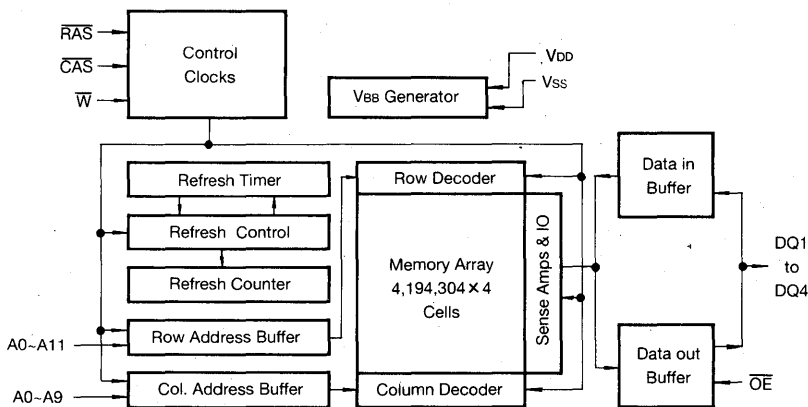
The Samsung KM44V4000A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

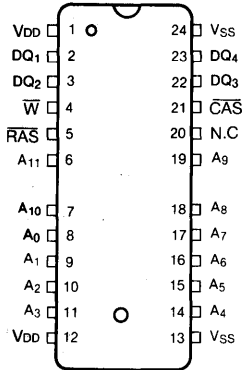
The KM44V4000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



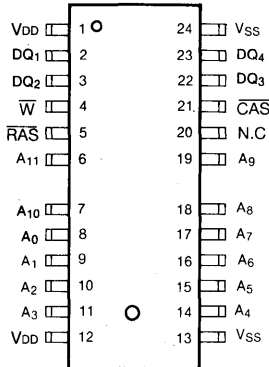
PIN CONFIGURATION (Top Views)

• KM44V4000 AJ/ALJ/ALLJ/ASLJ
/AK/ALK/ALLK/ASLK



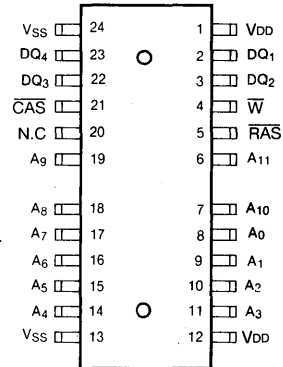
J : 400MIL
K : 300MIL

• KM44V4000 AT/ALT/ALLT/ASLT
/AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44V4000 ATR/ALTR/ALLTR/ASLTR
/ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-4	Data In/Out
VSS	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5 ~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ $\text{trc}=\text{min.}$)	KM44V4000A/AL/ALL/ASL-6	I _{CC1}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{IH}$)	KM44V4000A	I _{CC2}	-	2	mA
	KM44V4000AL			1	mA
	KM44V4000ALL			1	mA
	KM44V4000ASL			1	mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\overline{\text{CAS}}=V_{IH}$, $\overline{\text{RAS}}$ Cycling @ $\text{trc}=\text{min.}$)	KM44V4000A/AL/ALL/ASL-6	I _{CC3}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{CAS}}$, Address Cycling @ $\text{tPC}=\text{min.}$)	KM44V4000A/AL/ALL/ASL-6	I _{CC4}	-	70	mA
	KM44V4000A/AL/ALL/ASL-7			60	mA
	KM44V4000A/AL/ALL/ASL-8			50	mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{DD}-0.2V$)	KM44V4000A	I _{CC5}	-	1	mA
	KM44V4000AL			300	μA
	KM44V4000ALL			200	μA
	KM44V4000ASL			200	μA
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Cycling @ $\text{trc}=\text{min.}$)	KM44V4000A/AL/ALL/ASL-6	I _{CC6}	-	80	mA
	KM44V4000A/AL/ALL/ASL-7			70	mA
	KM44V4000A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V $\overline{\text{CAS}}=\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Cycling or 0.2V $\overline{\text{DIN}}$ =Don't Care $\text{TRC}=31.25\mu\text{S}(\text{L-Ver.})$ $62.5\mu\text{S}(\text{SL-Ver.})$, $\text{TRAS}=\text{TRAS min.} \sim 300\text{ns}$	KM44V4000AL	I _{CC7}	-	450	μA
	KM44V4000ASL			350	μA
Self Refresh Current $\overline{\text{RAS}}=\overline{\text{CAS}}=0.2V$ $\overline{\text{W}}=\overline{\text{OE}}=A_0-A_{11}=V_{DD}-0.2V$ or 0.2V $\overline{\text{DQ1}}-\overline{\text{DQ4}}=V_{DD}-0.2V$, 0.2V or Open	KM44V4000ALL	I _{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I_{OL}	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4} , Address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 \sim A_{11}$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Output Capacitance ($DQ_1 \sim DQ_4$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Test Condition : $V_{IH}/V_{IL} = 2.0V/0.8V$, $V_{OH}/V_{OL} = 2.0V/0.8V$, Output Loading $C_L = 100pF$

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from \overline{RAS}	trac		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tt	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	trp	40		50		60		ns	
\overline{RAS} pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	trSH	15		20		20		ns	
\overline{CAS} hold time	tCSH	60		70		80		ns	
\overline{CAS} pulse width	tcAS	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	trCD	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	trAD	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		20		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal DRAM only)	tREF		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\bar{W} to \bar{RAS} precharge time (\bar{C} -B- \bar{R} refresh)	tWRP	10		10		10		ns	
\bar{W} to \bar{RAS} hold time (\bar{C} -B- \bar{R} refresh)	tWRH	10		10		10		ns	
\bar{RAS} pulse width (\bar{C} -B- \bar{R} self refresh)	tRASS	100		100		100		μ s	15
\bar{RAS} precharge time (\bar{C} -B- \bar{R} self refresh)	tRPS	110		130		150		ns	15
\bar{CAS} hold time (\bar{C} -B- \bar{R} self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

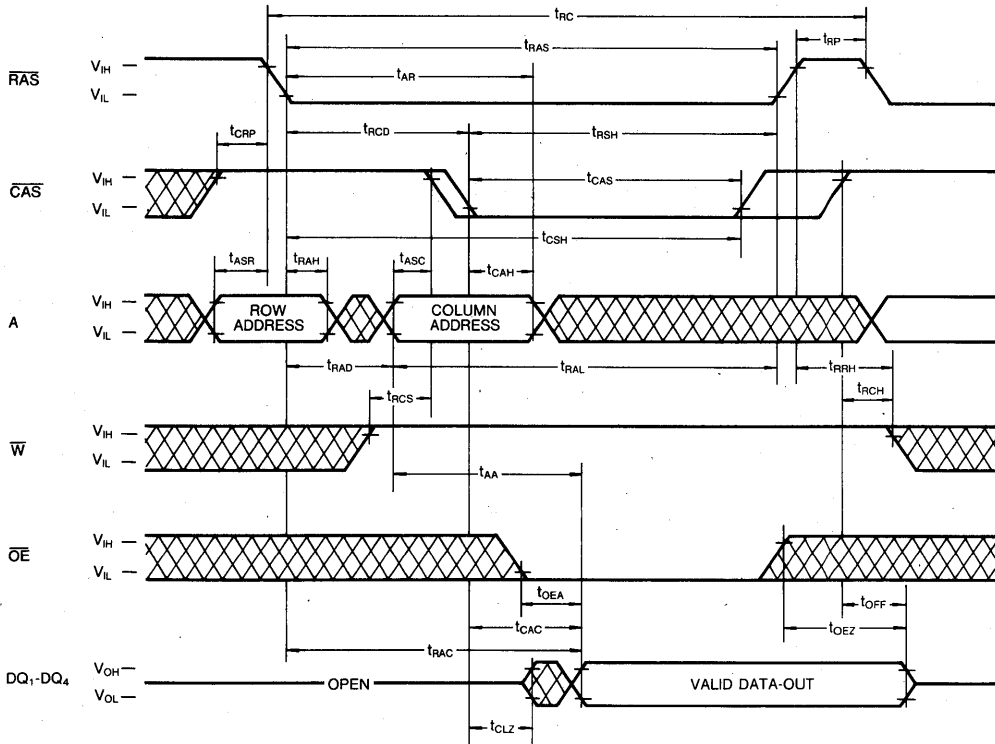
(Note.12)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	115		135		155		ns	
Read-modify-write cycle time	trWC	160		190		210		ns	
Access time from \bar{RAS}	trAC		65		75		85	ns	3,4,11
Access time from \bar{CAS}	tcAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\bar{RAS} pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	tcAS	20	10,000	25	10,000	25	10,000	ns	
\bar{RAS} hold time	trSH	20		25		25		ns	
\bar{CAS} hold time	tCSH	65		75		85		ns	
Column address to \bar{RAS} lead time	trAL	35		40		45		ns	
\bar{CAS} to \bar{W} delay time	tcWD	45		55		55		ns	8
\bar{RAS} to \bar{W} delay time	trWD	90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tpC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tpRWC	90		105		110		ns	
\bar{RAS} pulse width (Fast Page Mode)	trASP	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	tcPA		40		45		50	ns	3
\bar{OE} access time	toEA		20		25		25	ns	
\bar{OE} to data delay	toED	20		25		25		ns	
\bar{OE} command hold time	toEH	20		25		25		ns	

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and $V_{oh}=2.0V(I_{OUT}=2mA)$, $V_{ol}=0.8V(I_{OUT}=2mA)$
4. Operation within the $trCD(\text{max})$ limit insures that $trAC(\text{max})$ can be met. $trCD(\text{max})$ is specified as a reference point only. If $trCD$ is greater than the specified $trCD(\text{max})$ limit, then access time is controlled exclusively by $tcAC$.
5. Assumes that $trCD \geq trCD(\text{max})$.
6. tAR , $tWCR$, $tDHR$ are referenced to $trAD(\text{max})$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. $twCS$, $trWD$, $tcWD$ and $tAWD$ are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $twCS \geq twCS(\text{min})$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $tcWD \geq tcWD(\text{min})$, $trWD \geq trWD(\text{min})$ and $tAWD \geq tAWD(\text{min})$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either $trCH$ or $trRH$ must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $trAD(\text{max})$ limit insures that $trAC(\text{max})$ can be met. $trAD(\text{max})$ is specified as a reference point only. If $trAD$ is greater than the specified $trAD(\text{max})$ limit, then access time is controlled by tAA .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of $trAC$, tAA , $tcAC$ is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $toFF(\text{max})$ and $toEZ(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS
READ CYCLE



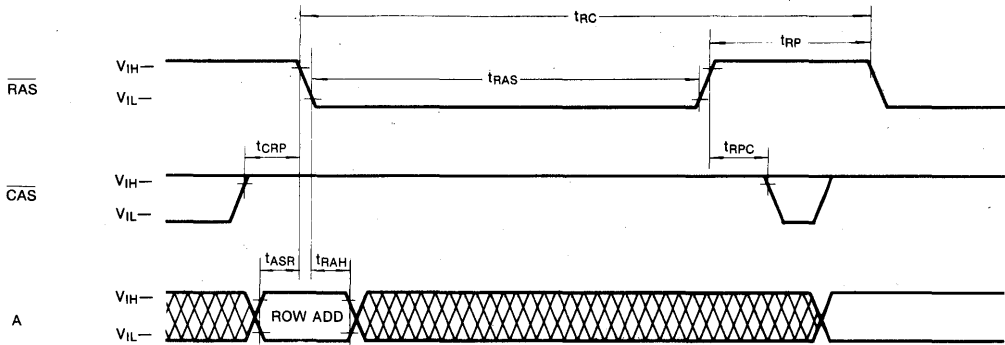
 DON'T CARE

5

TIMING DIAGRAMS (Continued)

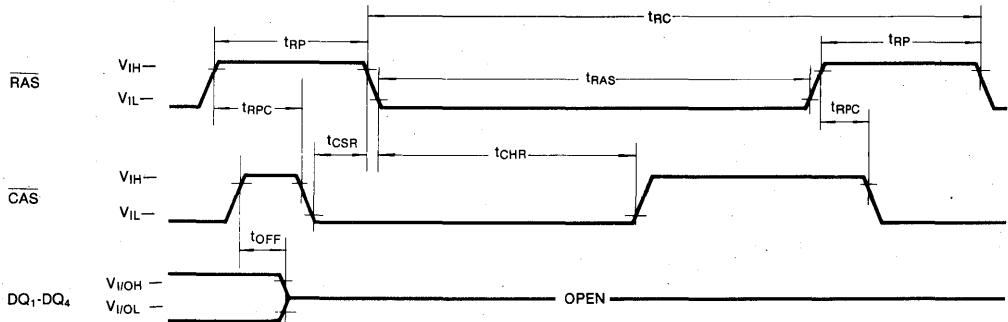
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



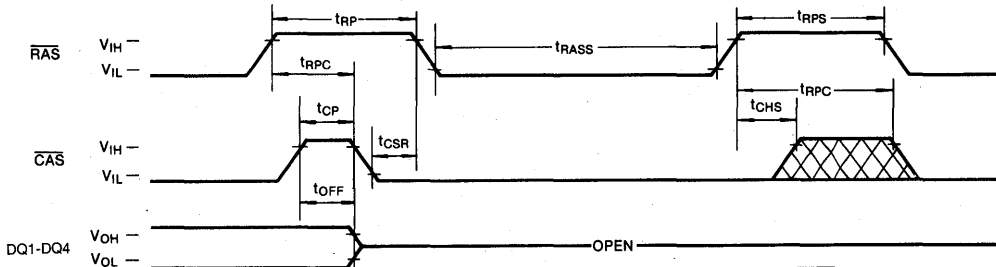
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \bar{W} = V_{IH} , \bar{OE} , A=Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

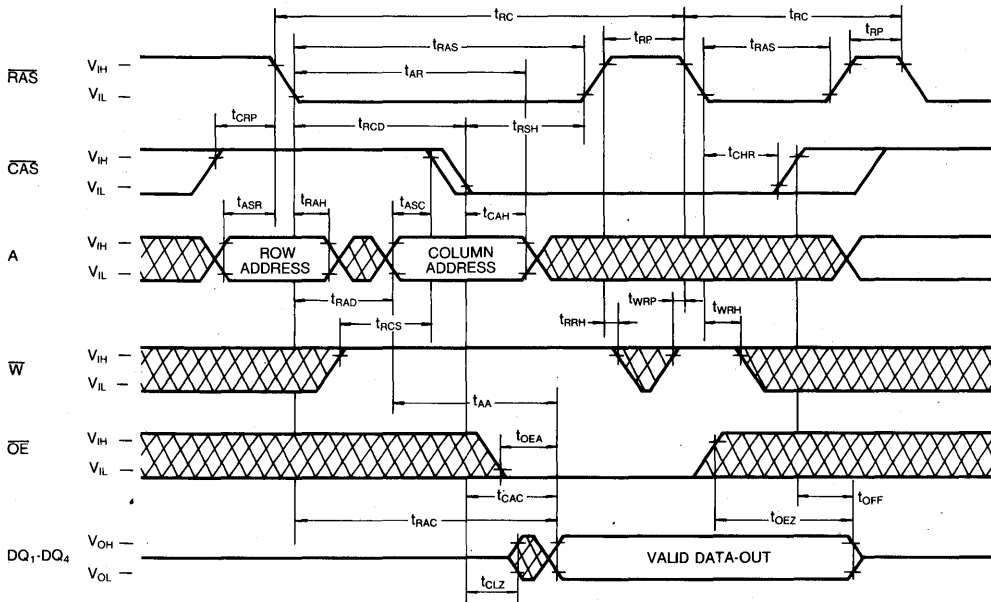
NOTE: \bar{W} , \bar{OE} , A=Don't Care



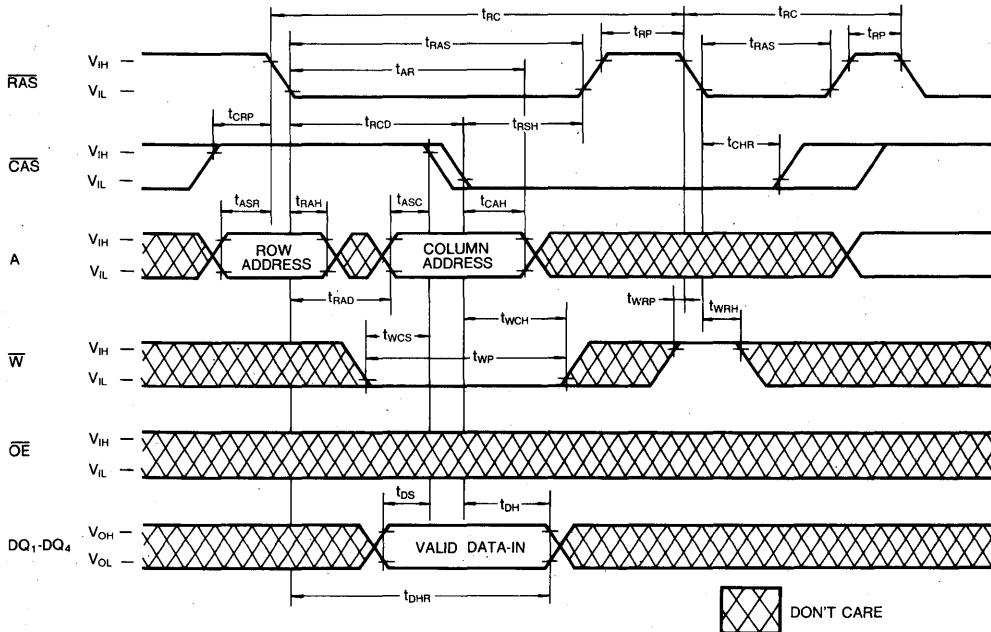
5

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

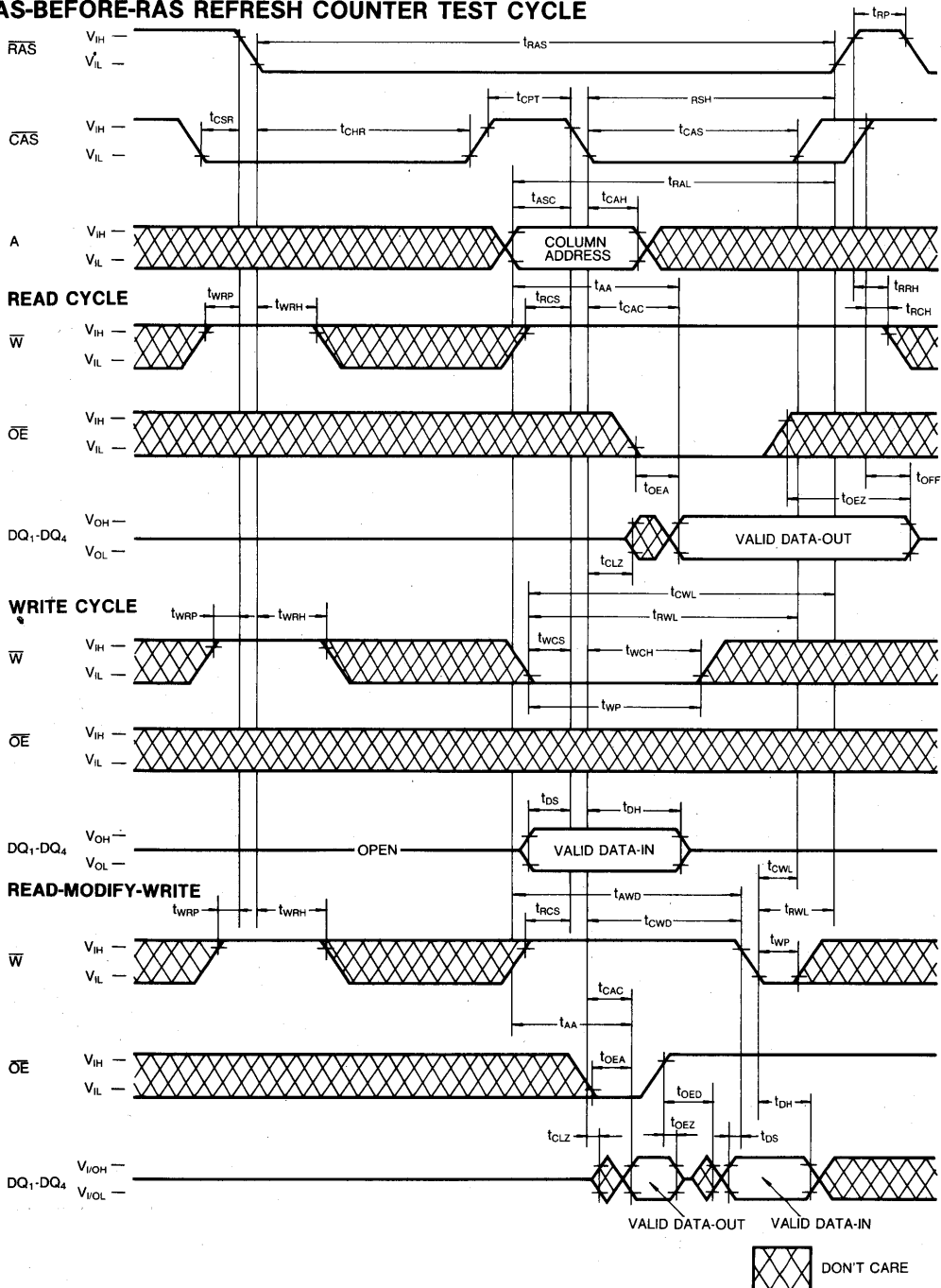


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

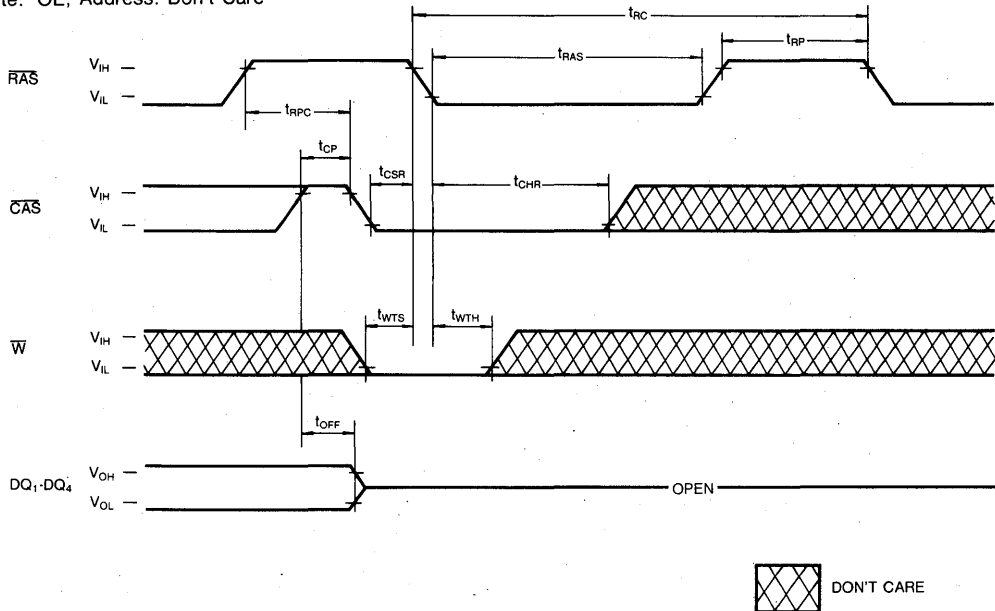


5

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



TEST MODE DESCRIPTION

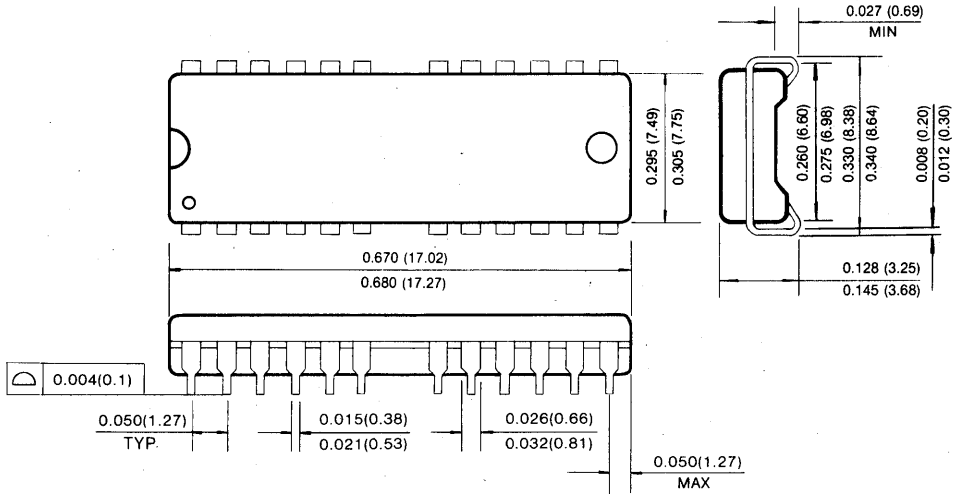
The KM44V4000A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A_0 and A_1 are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test

Mode", the $4M \times 4$ DRAM can be tested as if it were a $1M \times 4$ DRAM. \overline{W} , \overline{CAS} -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And " \overline{CAS} -BEFORE- \overline{RAS} REFRESH CYCLE" or " \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

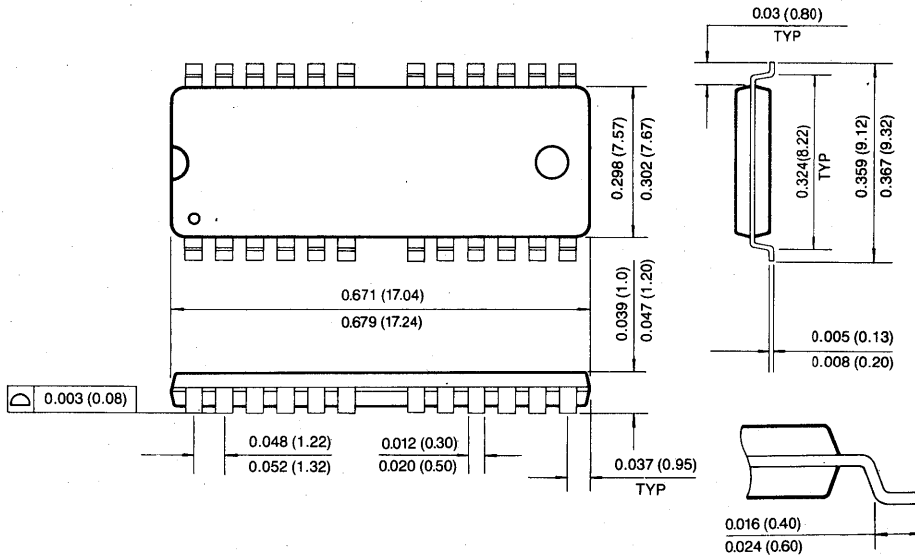
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



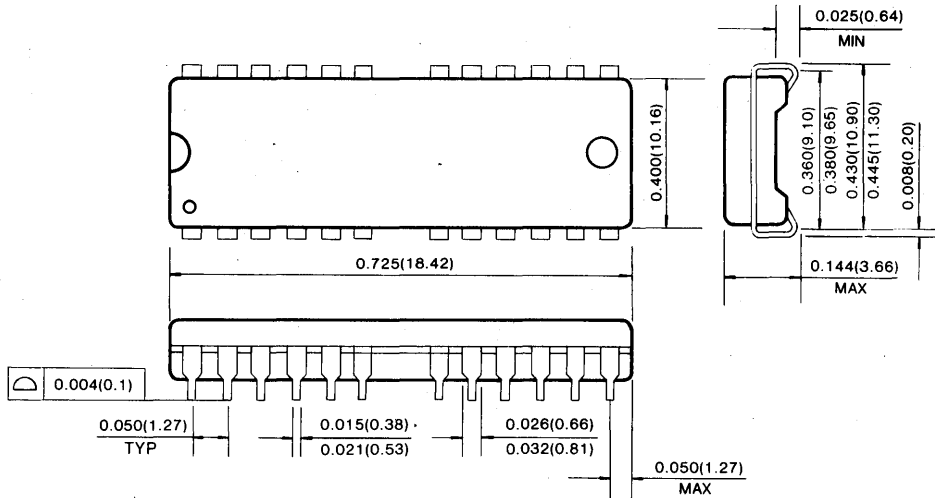
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



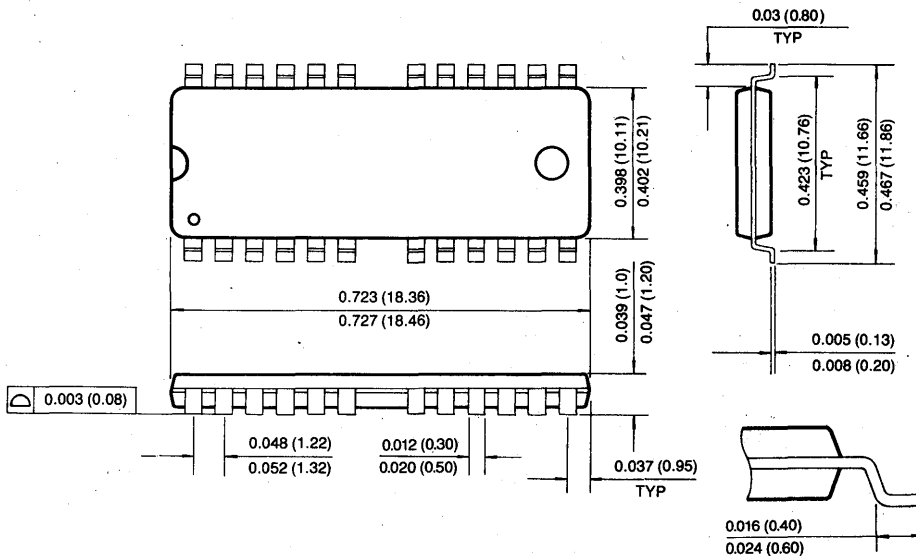
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{RC}
KM44V4100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44V4100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44V4100A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single+3.3V ± 0.3V power supply
- 2048 cycles/32ms refresh (Normal DRAM)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

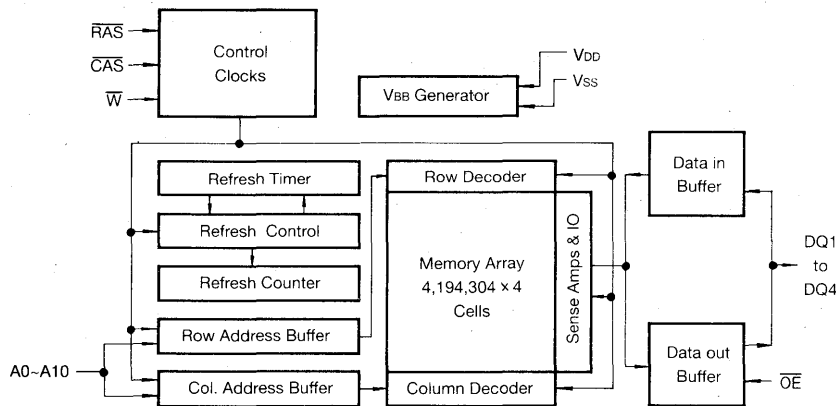
The Samsung KM44V4100A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

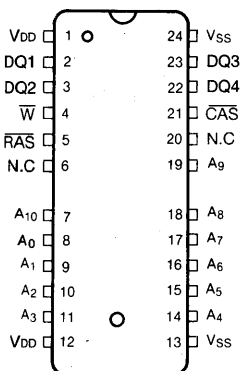
The KM44V4100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



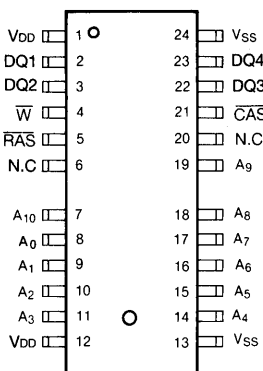
PIN CONFIGURATION (Top Views)

• KM44V4100 AJ/ALJ/ALLJ/ASLJ
/AK/ALK/ALLK/ASLK



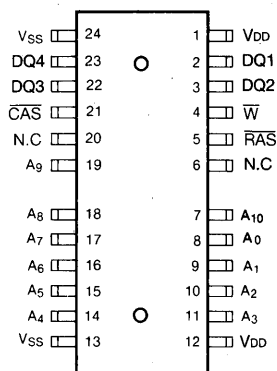
J : 400MIL
K : 300MIL

• KM44V4100 AT/ALT/ALLT/ASLT
/AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44V4100 ATR/ALTR/ALLTR/ASLTR
/ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-4	Data In/Out
VSS	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 4.6	V
Voltage on VDD Supply Relative to Vss	VDD	-0.5 ~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	VDD + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44V4100A/AL/ALL/ASL-6 KM44V4100A/AL/ALL/ASL-7 KM44V4100A/AL/ALL/ASL-8 Icc1	-	100 90 80	mA mA mA
Standby Current (RAS=CAS=W=V _{IH})	KM44V4100A KM44V4100AL KM44V4100ALL KM44V4100ASL Icc2	-	2 1 1 1	mA mA mA mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM44V4100A/AL/ALL/ASL-6 KM44V4100A/AL/ALL/ASL-7 KM44V4100A/AL/ALL/ASL-8 Icc3	-	100 90 80	mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tPC=min.)	KM44V4100A/AL/ALL/ASL-6 KM44V4100A/AL/ALL/ASL-7 KM44V4100A/AL/ALL/ASL-8 Icc4	-	80 70 60	mA mA mA
Standby Current (RAS=CAS=W=VDD-0.2V)	KM44V4100A KM44V4100AL KM44V4100ALL KM44V4100ASL Icc5	-	1 300 200 200	mA μA μA μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44V4100A/AL/ALL/ASL-6 KM44V4100A/AL/ALL/ASL-7 KM44V4100A/AL/ALL/ASL-8 Icc6	-	100 90 80	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=VDD-0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DIN=Don't Care TRC=62.5μS(L-Ver.) 125μS(SL-Ver.), TRAS=TRAS min.~300ns	KM44V4100AL KM44V4100ASL Icc7	-	400 300	μA μA
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A10=VDD-0.2V or 0.2V DQ1~DQ4=VDD-0.2V, 0.2V or Open	KM44V4100ALL Icc8	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test=0 volts.)	$I_{i(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{o(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , Address can be changed maximum two times while $RAS = V_{IL}$. In I_{CC4} , Address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 \sim A_{10}$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Input Capacitance ($DQ_1 \sim DQ_4$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Test Condition : $V_{ih}/V_{il} = 2.0V/0.8V$, $V_{oh}/V_{ol} = 2.0V/0.8V$, Output Loading $C_L = 100pF$

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	trAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	trAL	30		35		40		ns	
Read command set-up time	trCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command hold time	twCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	15		20		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal DRAM only)	tREF		32		32		32	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	twCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tcPT	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		35		40		45	ns	3
Fast Page mode cycle time	tpC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tpRWC	85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tcp	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	trASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	35		40		45		ns	
$\overline{\text{OE}}$ access time	toEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	toED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	toEZ	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ commend hold time	toEH	15		20		20		ns	

5

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\bar{W} to \bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRP	10		10		10		ns	
\bar{W} to \bar{RAS} hold time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRH	10		10		10		ns	
\bar{RAS} pulse width (\bar{C} - \bar{B} - \bar{R} self refresh)	tRASS	100		100		100		μ s	15
\bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} self refresh)	tRPS	110		130		150		ns	15
\bar{CAS} hold time (\bar{C} - \bar{B} - \bar{R} self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

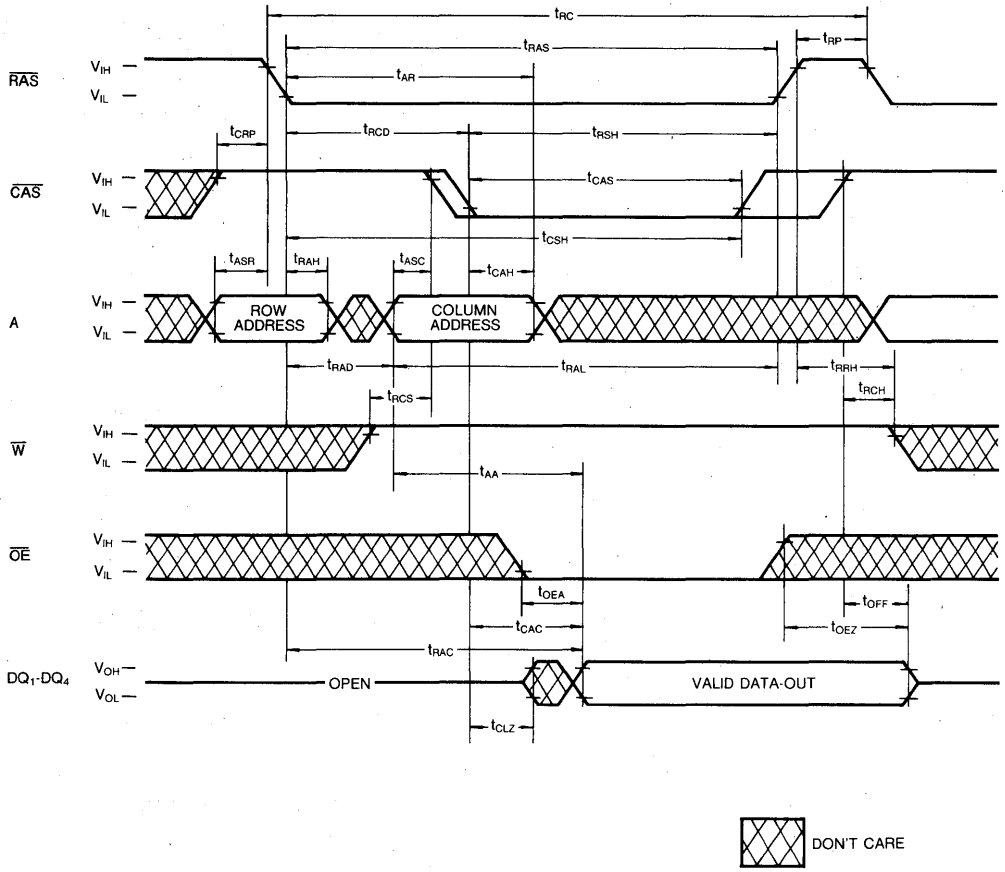
(Note.12)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from \bar{RAS}	tRAC		65		75		85	ns	3,4,11
Access time from \bar{CAS}	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\bar{RAS} pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
\bar{RAS} hold time	tRSH	20		25		25		ns	
\bar{CAS} hold time	tCSH	65		75		85		ns	
Column address to \bar{RAS} lead time	tRAL	35		40		45		ns	
\bar{CAS} to \bar{W} delay time	tCWD	45		55		55		ns	8
\bar{RAS} to \bar{W} delay time	tRWD	90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
\bar{RAS} pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	tCPA		40		45		50	ns	3
\bar{OE} access time	tOEA		20		25		25	ns	
\bar{OE} to data delay	tOED	20		25		25		ns	
\bar{OE} command hold time	tOEH	20		25		25		ns	

NOTES

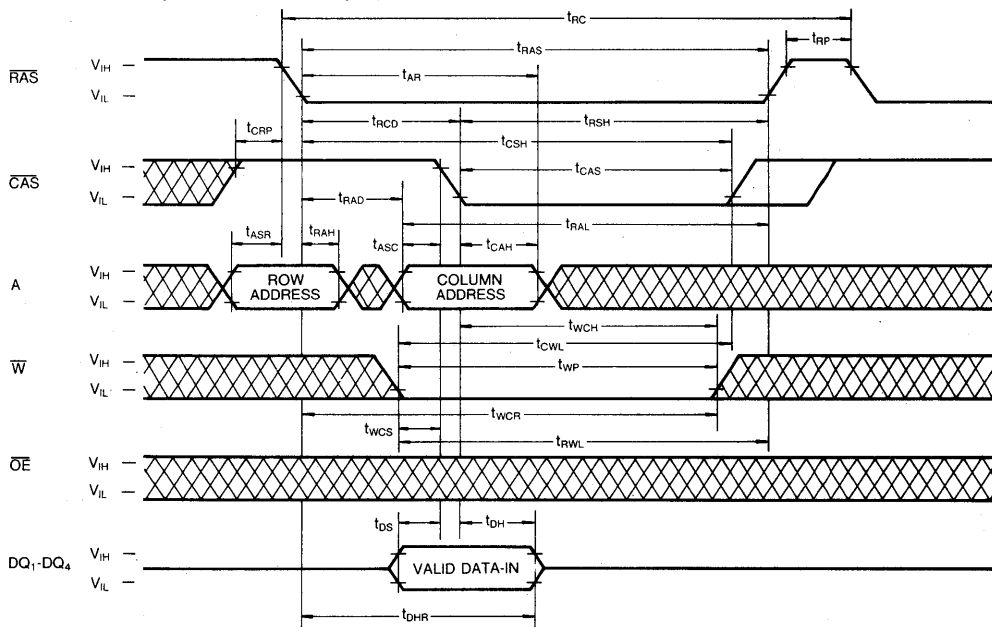
1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and $V_{OH}=2.0V(I_{OUT}=2mA)$, $V_{OL}=0.8V(I_{OUT}=2mA)$
4. Operation within the $t_{RCDB}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCDB}(\max)$ is specified as a reference point only. If t_{RCDB} is greater than the specified $t_{RCDB}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCDB} \geq t_{RCDB}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS
READ CYCLE

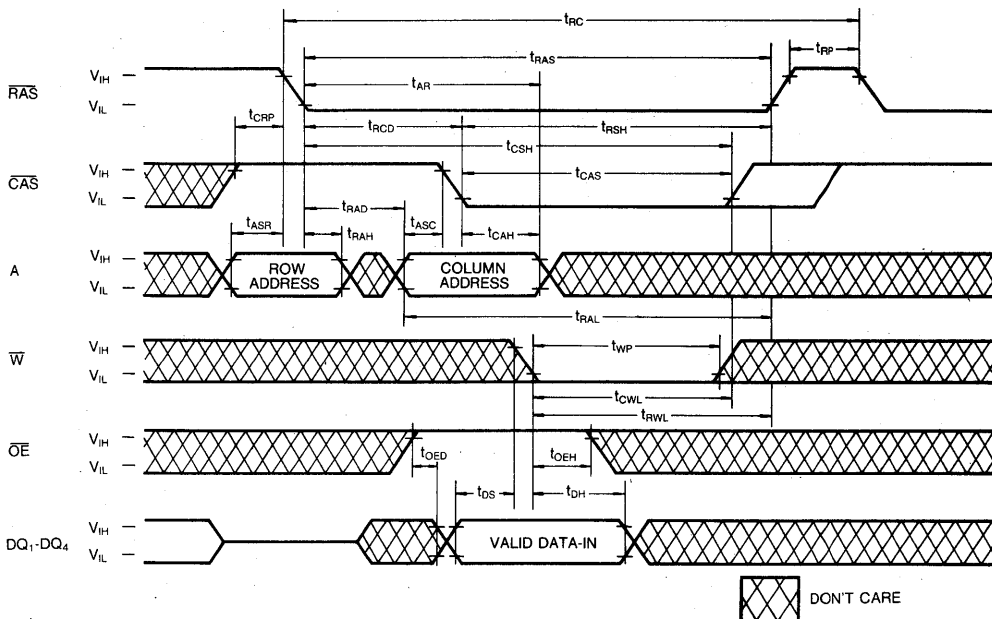


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

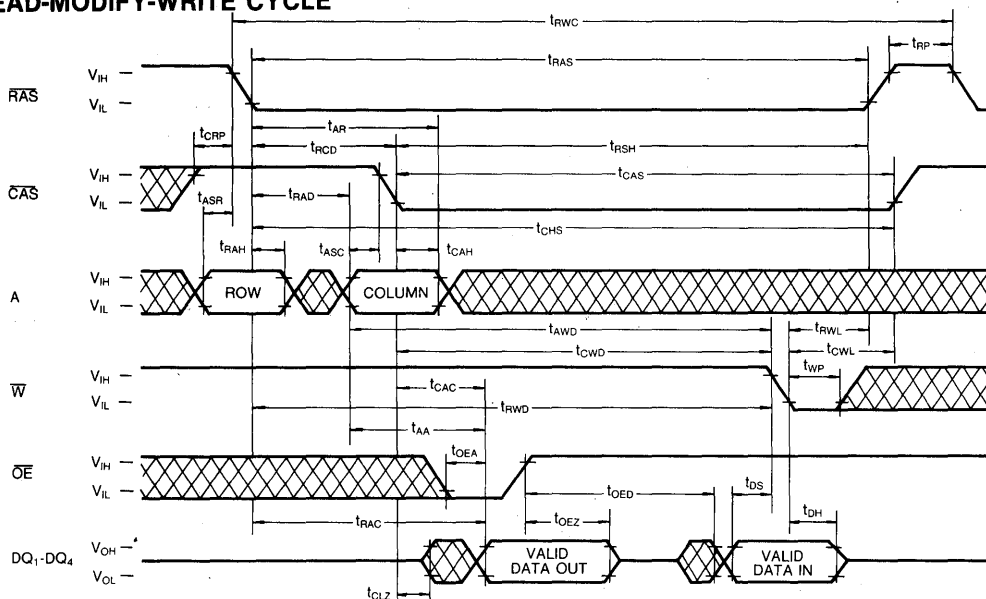


 DON'T CARE

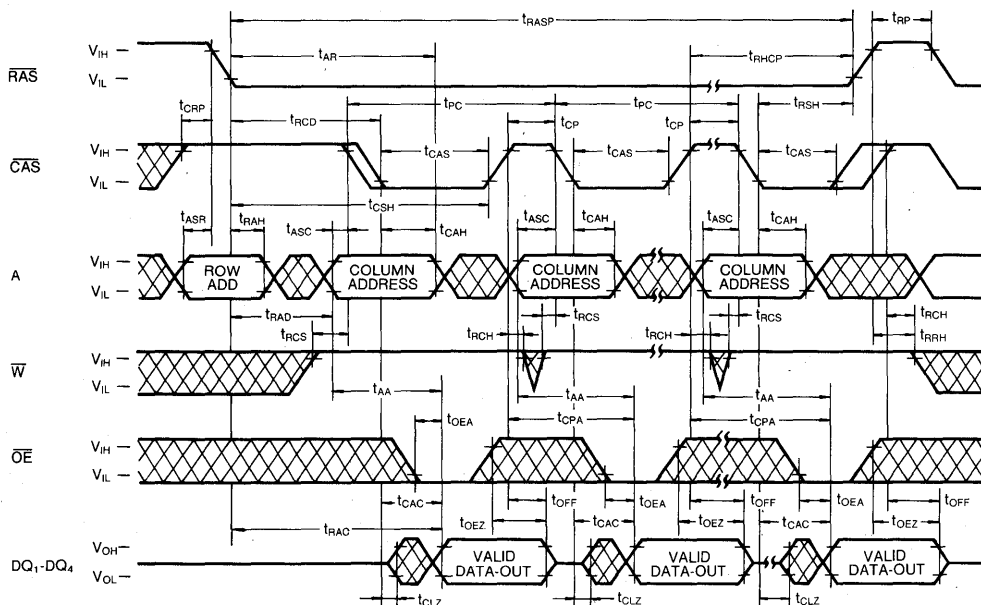
5

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



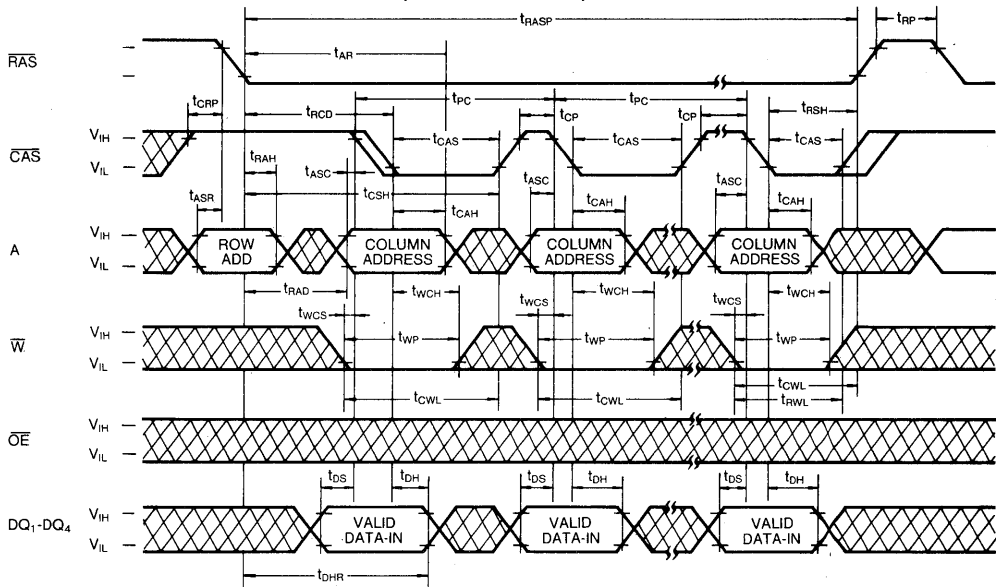
FAST PAGE MODE READ CYCLE



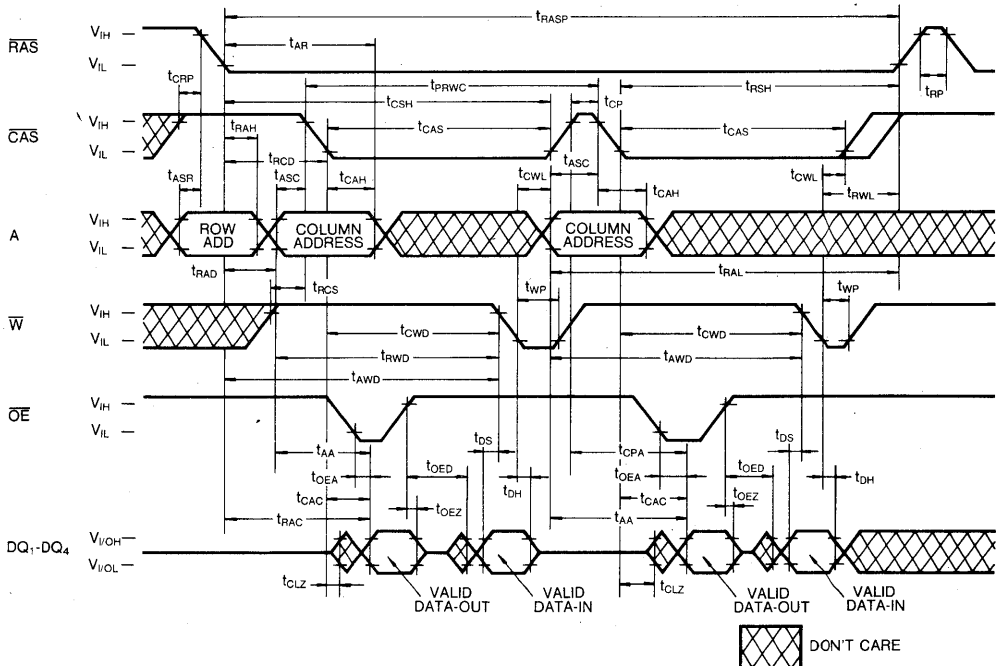
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

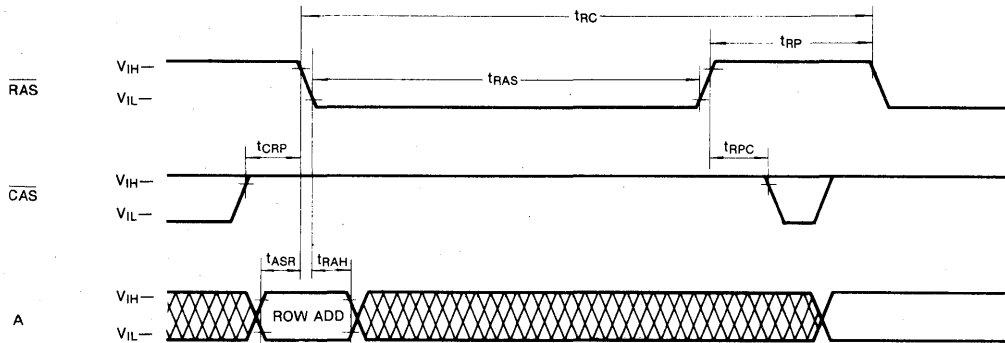


5

TIMING DIAGRAMS (Continued)

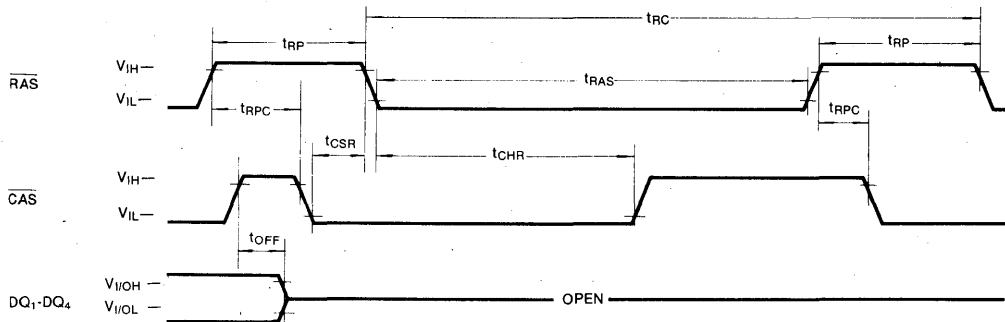
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



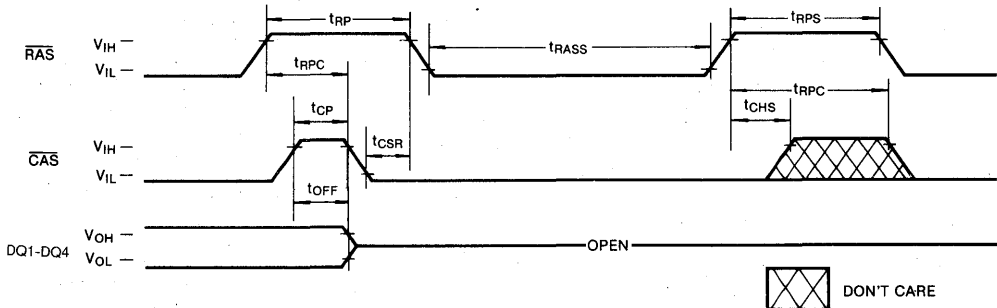
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\bar{W} = V_{IH}$, \bar{OE} , A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

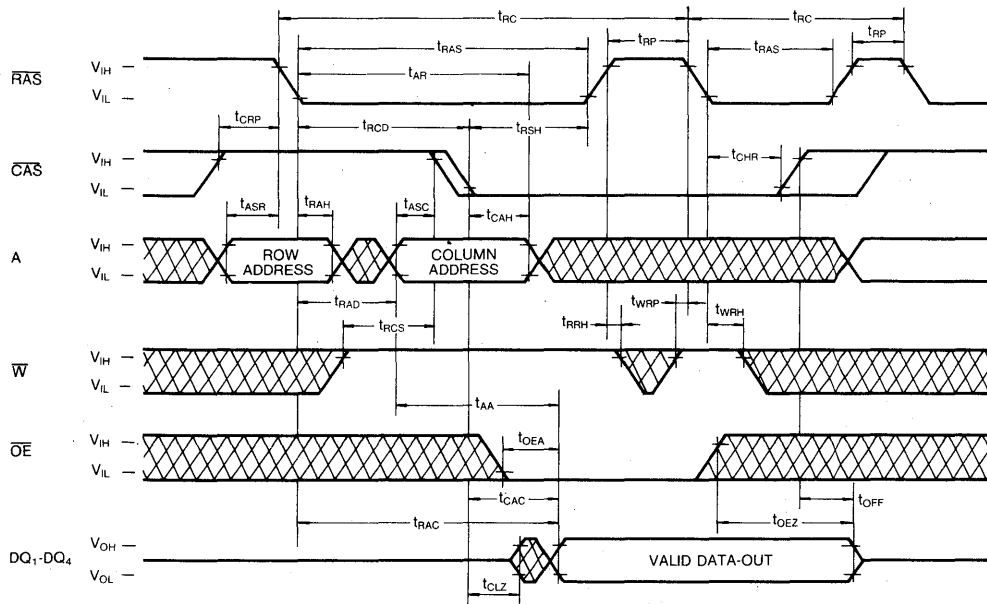
NOTE: \bar{W} , \bar{OE} , A = Don't Care



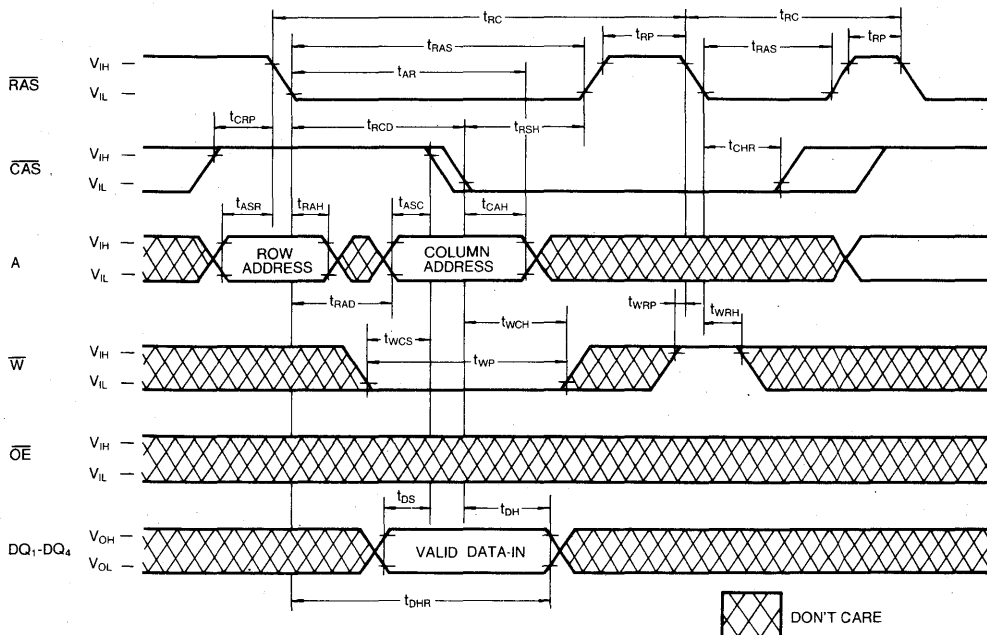
 DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

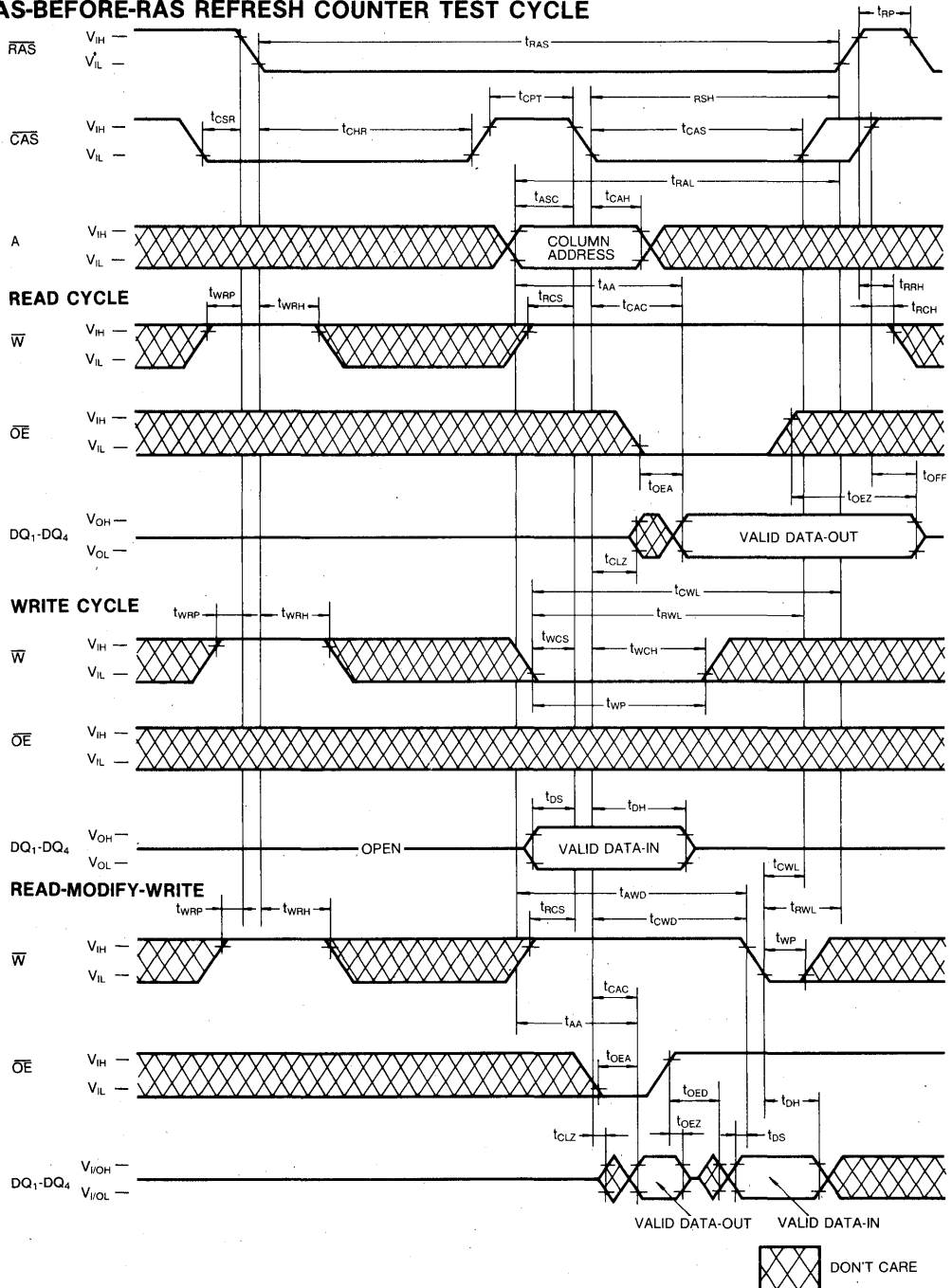


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

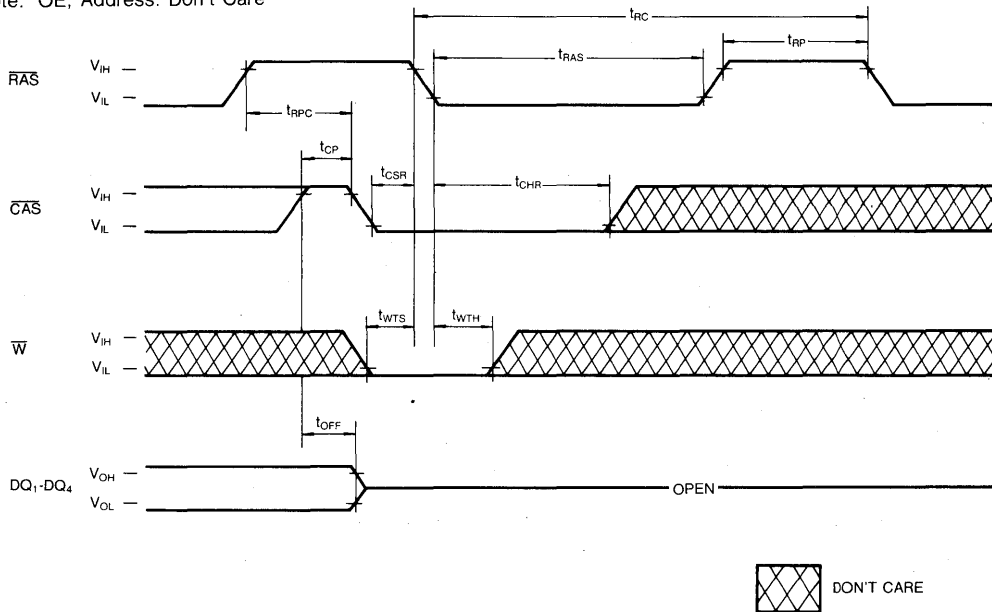
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care



TEST MODE DESCRIPTION

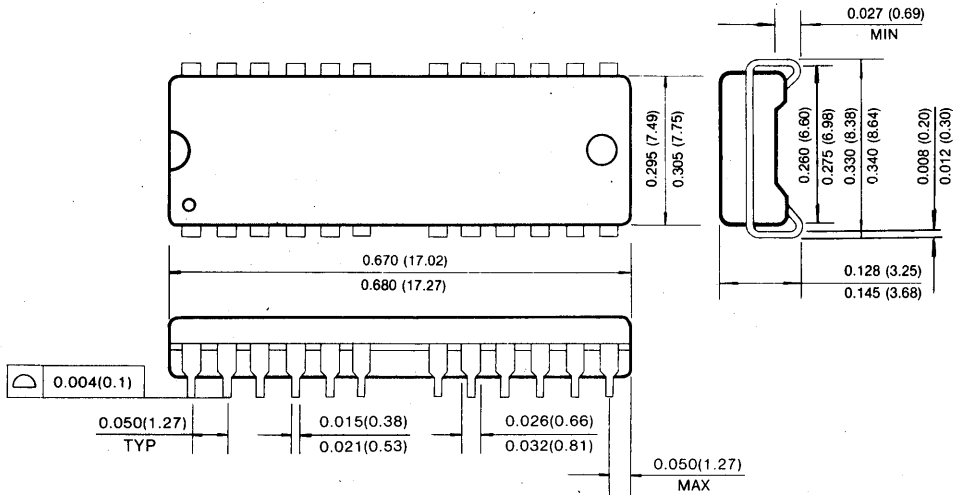
The KM44V4100A/AL/ALL/ASL is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A₀ and A₁ are not used. If, upon reading, four bits on one D/Q pin are equal (all "1"s or "0"s) the D/Q pin indicates a "1". If they were not equal, the D/Q pin would indicate a "0". In "Test

Mode", the 4M × 4 DRAM can be tested as if it were a 1M × 4 DRAM. \overline{W} , \overline{CAS} -BEFORE- \overline{RAS} Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "CAS-BEFORE- \overline{RAS} REFRESH CYCLE" or " \overline{RAS} -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

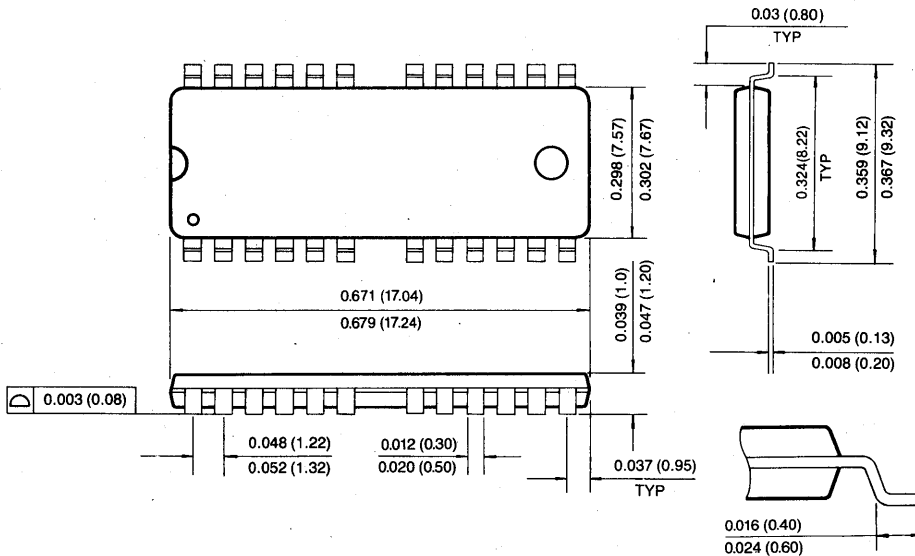
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



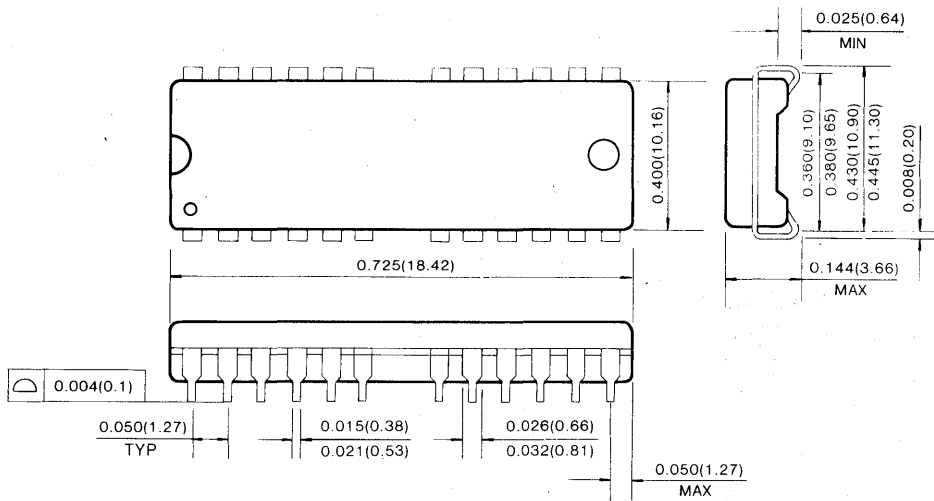
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



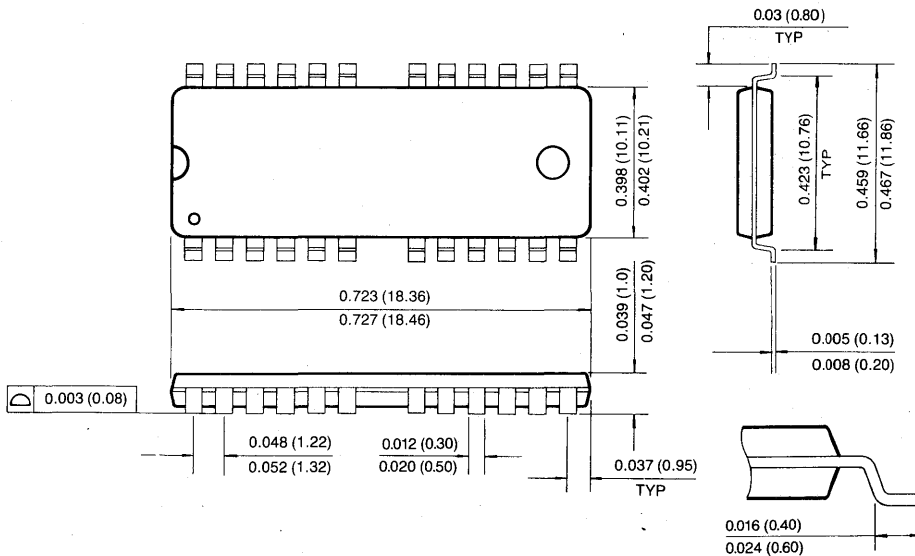
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



5

4M × 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
KM44V4004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44V4004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44V4004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh Operation (LL-ver. only)
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- LVTTTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+3.3V ± 0.3V power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

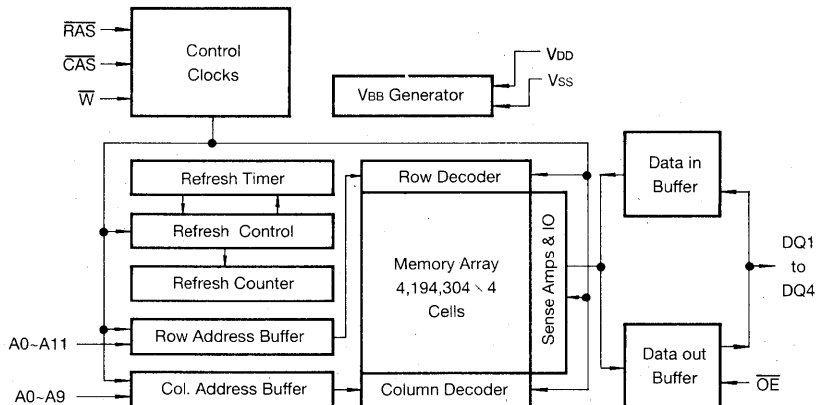
The Samsung KM44V4004A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

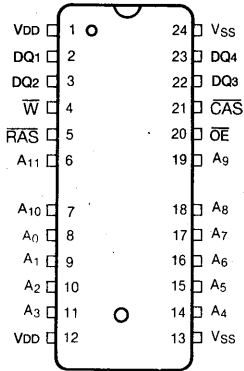
The KM44V4004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



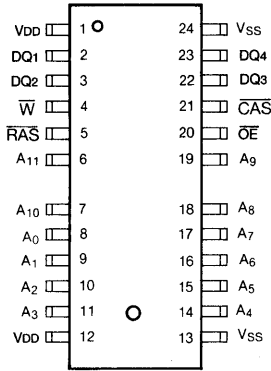
PIN CONFIGURATION (Top Views)

• KM44V4004 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



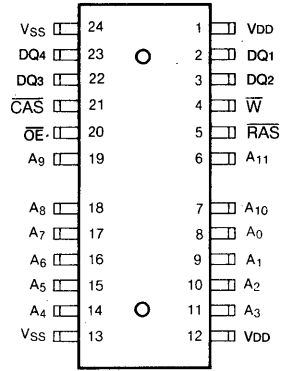
J : 400MIL
K : 300MIL

• KM44V4004 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44V4004 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-DQ4	Data In/Out
VSS	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5~ 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8	I _{CC1}	-	80 70 60 mA mA mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)	KM44V4004A KM44V4004AL KM44V4004ALL KM44V4004ASL	I _{CC2}	-	2 1 1 1 mA mA mA mA
\overline{RAS} -Only Refresh Current* ($\overline{CAS}=V_{IH}$, \overline{RAS} Cycling @trc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8	I _{CC3}	-	80 70 60 mA mA mA
Hyper Page Mode Current* ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address Cycling @tpc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8	I _{CC4}	-	90 80 70 mA mA mA
Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{DD}-0.2V$)	KM44V4004A KM44V4004AL KM44V4004ALL KM44V4004ASL	I _{CC5}	-	1 300 200 200 mA μA μA μA
\overline{CAS} -Before- \overline{RAS} Refresh Current* (\overline{RAS} and \overline{CAS} Cycling @trc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8	I _{CC6}	-	80 70 60 mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V $\overline{CAS}=\overline{CAS}$ -Before- \overline{RAS} Cycling or 0.2V DQ1~DQ4=Don't Care trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), t _{RAS} =t _{RAS} min. ~300ns	KM44V4004AL KM44V4004ASL	I _{CC7}	-	450 350 μA μA
Self Refresh Current $\overline{RAS}=\overline{CAS}=0.2V$ $\overline{W}=\overline{OE}=A_0-A_{11}=V_{DD}-0.2V$ or 0.2V DQ1~DQ4=V _{DD} -0.2V, 0.2V or Open	KM44V4004ALL	I _{CC8}	-	250 μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	I _{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I _{OL}	-10	10	μA
Output High Voltage Level (I _{OH} = -2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} = 2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while RAS=V_{IL}. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A = 25°C, V_{DD} = 3.3V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₁₁)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C _{IN2}	-	7	pF
Output Capacitance (DQ ₁ ~DQ ₄)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD} = 3.3V ± 0.3V. See notes 1,2)

Test condition: V_{ih}/V_{il} = 2.0V/0.8V, V_{oh}/V_{ol} = 2.0V/0.8V, Output Loading C_L = 100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	3		3		3		ns	3
\overline{OE} to output in Low-Z	t _{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	t _{CEZ}	3	15	3	20	3	20	ns	7,14,16
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	t _{RP}	40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	15		20		20		ns	
\overline{CAS} hold time	t _{CSH}	45		50		60		ns	
\overline{CAS} pulse width	t _{CAS}	10	10,000	15	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address hold time referenced to \overline{RAS}	tAR	45		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to \overline{RAS}	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to \overline{RAS} lead time	trWL	15		20		20		ns	
Write command to \overline{CAS} lead time	tcWL	10		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to \overline{RAS}	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	tcWD	40		50		50		ns	8
\overline{RAS} to \overline{W} delay time	trWD	85		100		110		ns	8
Column address to \overline{W} delay time	tAWD	55		65		70		ns	8
\overline{CAS} precharge to \overline{W} delay time	tcpWD	60		70		75		ns	8
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		15		15		ns	
\overline{RAS} to \overline{CAS} precharge time	trPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} -B- \overline{R} counter test cycle)	tcPT	20		30		30		ns	
Access time from \overline{CAS} precharge	tcPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	71		86		96		ns	17
\overline{CAS} precharge time (Hyper Page cycle)	tcp	10		10		10		ns	
\overline{RAS} pulse width (Hyper Page cycle)	trASP	60	200,000	70	200,000	80	200,000	ns	
\overline{RAS} hold time from \overline{CAS} precharge	trHCP	35		40		45		ns	
\overline{OE} access time	toEA		15		20		20	ns	
\overline{OE} to data delay	toED	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	toEZ	3	15	3	20	3	20	ns	7,14
\overline{OE} command hold time	toEH	15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{C} -B- \overline{R} refresh)	twRP	10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} -B- \overline{R} refresh)	twRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,16
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		ns	
\overline{W} pulse width(Hyper Page cycle)	twPE	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	treZ	3	15	3	20	3	20	ns	7,14,16
Output buffer turn off delay from \overline{W}	twEZ	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	twED	15		20		20		ns	
\overline{RAS} pulse width (LL-Ver)	trASS	100		100		100		μ s	15
\overline{RAS} precharge time (LL-Ver)	trPS	110		130		150		ns	15
\overline{CAS} hold time (LL-Ver)	tCHS	-50		-50		-50		ns	15

5

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	115		135		155		ns	
Read-modify-write cycle time	trWC	160		190		210		ns	
Access time from \overline{RAS}	trAC		65		75		85	ns	3,4,11
Access time from \overline{CAS}	trAC		20		20		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	trCS	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	20		25		25		ns	
\overline{CAS} hold time	trSH	20		55		65		ns	
Column address to \overline{RAS} lead time	trAL	35		40		45		ns	
\overline{CAS} to \overline{W} delay time	trWD	45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	60		70		75		ns	8
Hyper Page mode cycle time	trHPC	29		34		39		ns	
Hyper Page mode read-modify-write cycle time	trPRWC	76		91		101		ns	
\overline{RAS} pulse width (Hyper Page Mode)	trASP	65	200,000	75	200,000	85	200,000	ns	



TEST MODE CYCLE (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		40		45		50	ns	
$\overline{\text{OE}}$ access time	toEA		20		25		25	ns	3
$\overline{\text{OE}}$ to data delay	toED	20		25		25		ns	
$\overline{\text{OE}}$ command hold time	toEH	20		25		25		ns	

TEST MODE DESCRIPTION

The KM44V4004A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A₀ is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM.

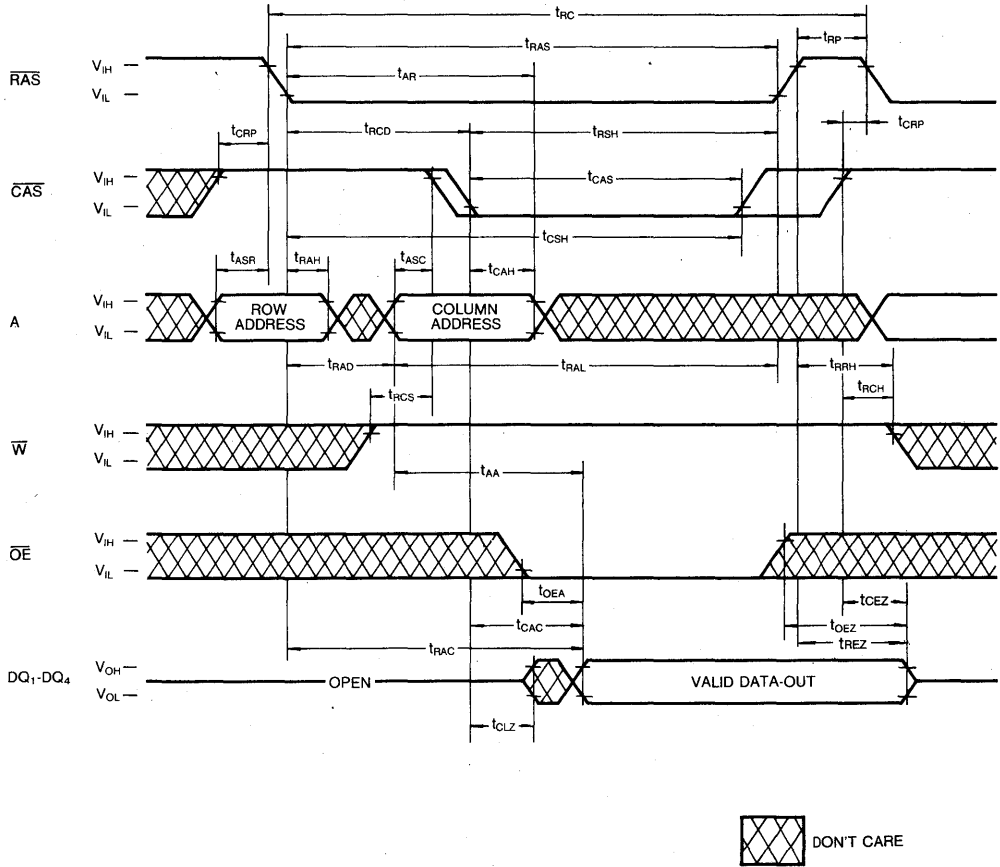
$\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And "CAS before $\overline{\text{RAS}}$ Refresh Cycle" or $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time (1/4 in cases of N test pattern)

NOTES

1. An initial pause of 200µs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPRWC}.
3. Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{out}=2mA), V_{ol}=0.8V(I_{out}=2mA)
4. Operation within the t_{RCd}(max) limit insures that t_{rac}(max) can be met. t_{RCd}(max) is specified as a reference point only. If t_{RCd} is greater than the specified t_{RCd}(max) limit, then access time is controlled exclusively by t_{CAc}.
5. Assumes that t_{RCd} ≥ t_{RCd}(max).
6. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD}(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
8. t_{WCS}, t_{TRWD}, t_{CDW} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If t_{WCS} ≥ t_{WCS}(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{CDW} ≥ t_{CDW}(min), t_{TRWD} ≥ t_{TRWD}(min) and t_{AWD} ≥ t_{AWD}(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the t_{RAD}(max) limit insures that t_{rac}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{rac}, t_{AA}, t_{CAc} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. t_{TRWZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going
17. t_{ASC} ≥ t_{CP}(min), Assumn t_r=2.0ns



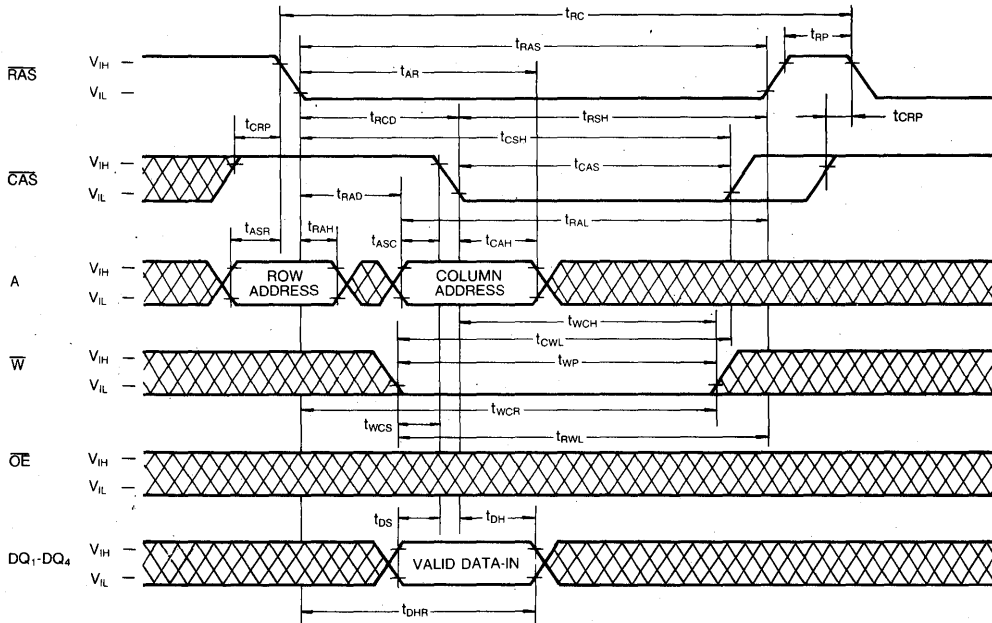
TIMING DIAGRAMS
READ CYCLE



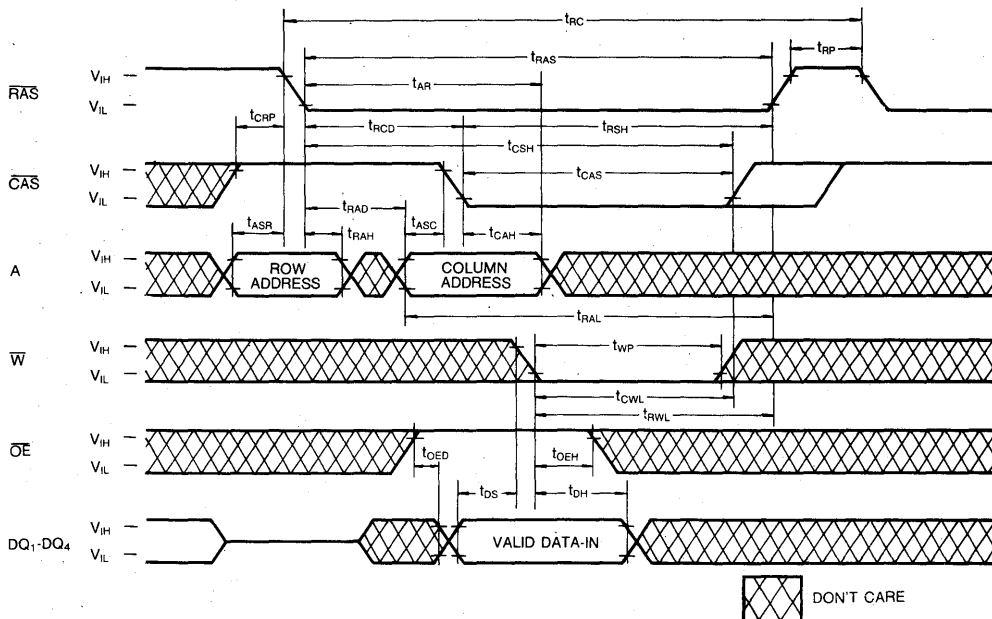
5

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)

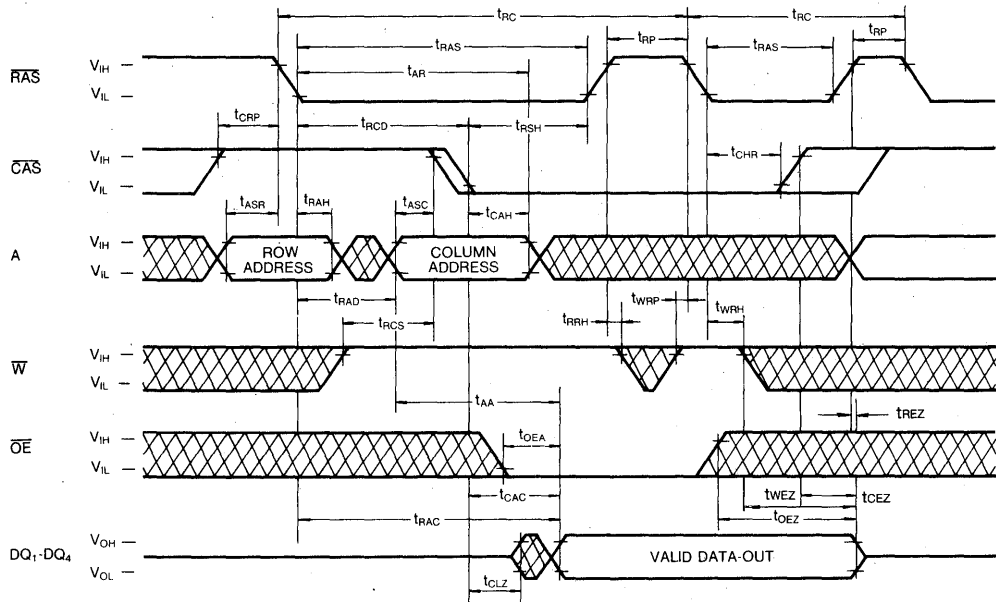


WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

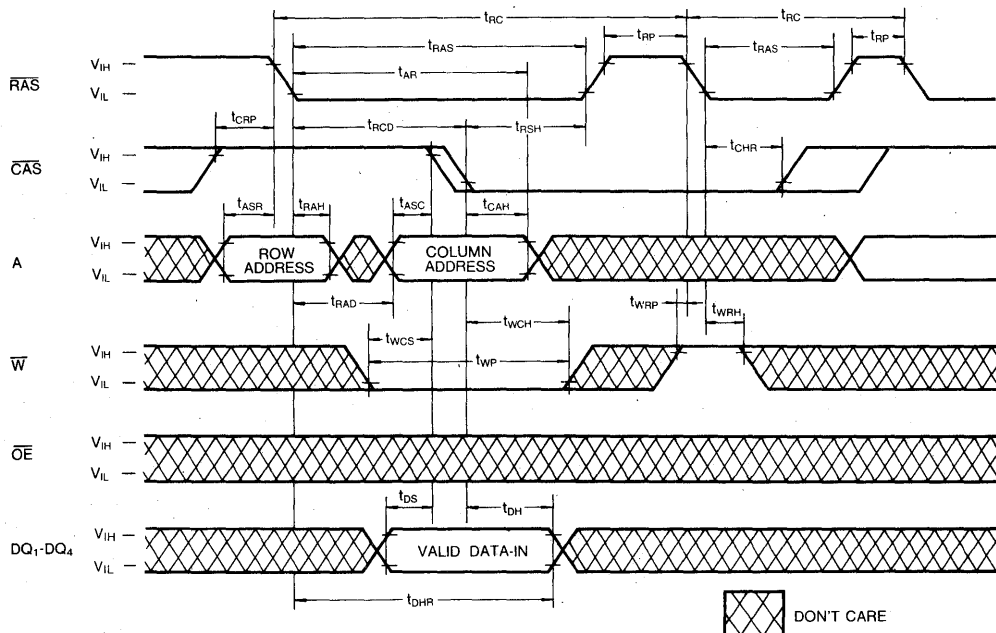


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



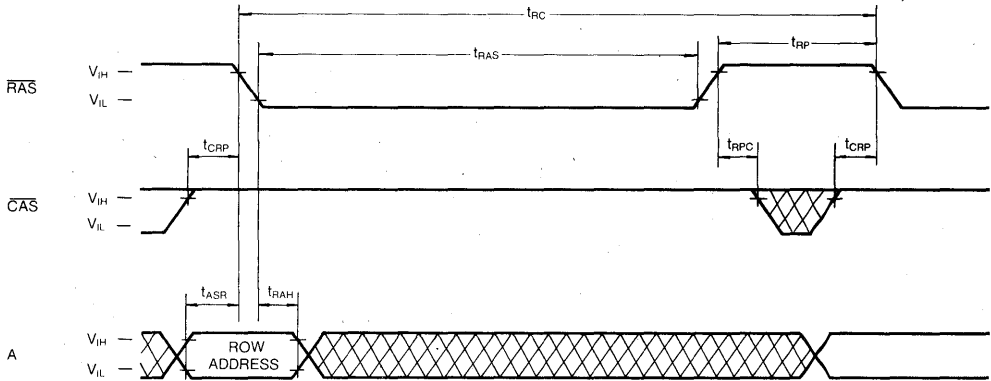
HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

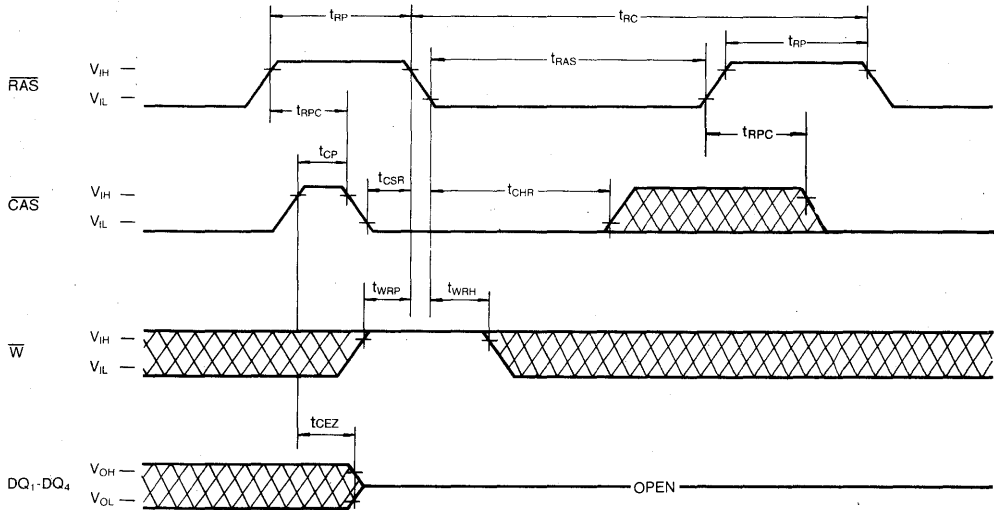
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} =Don't Care



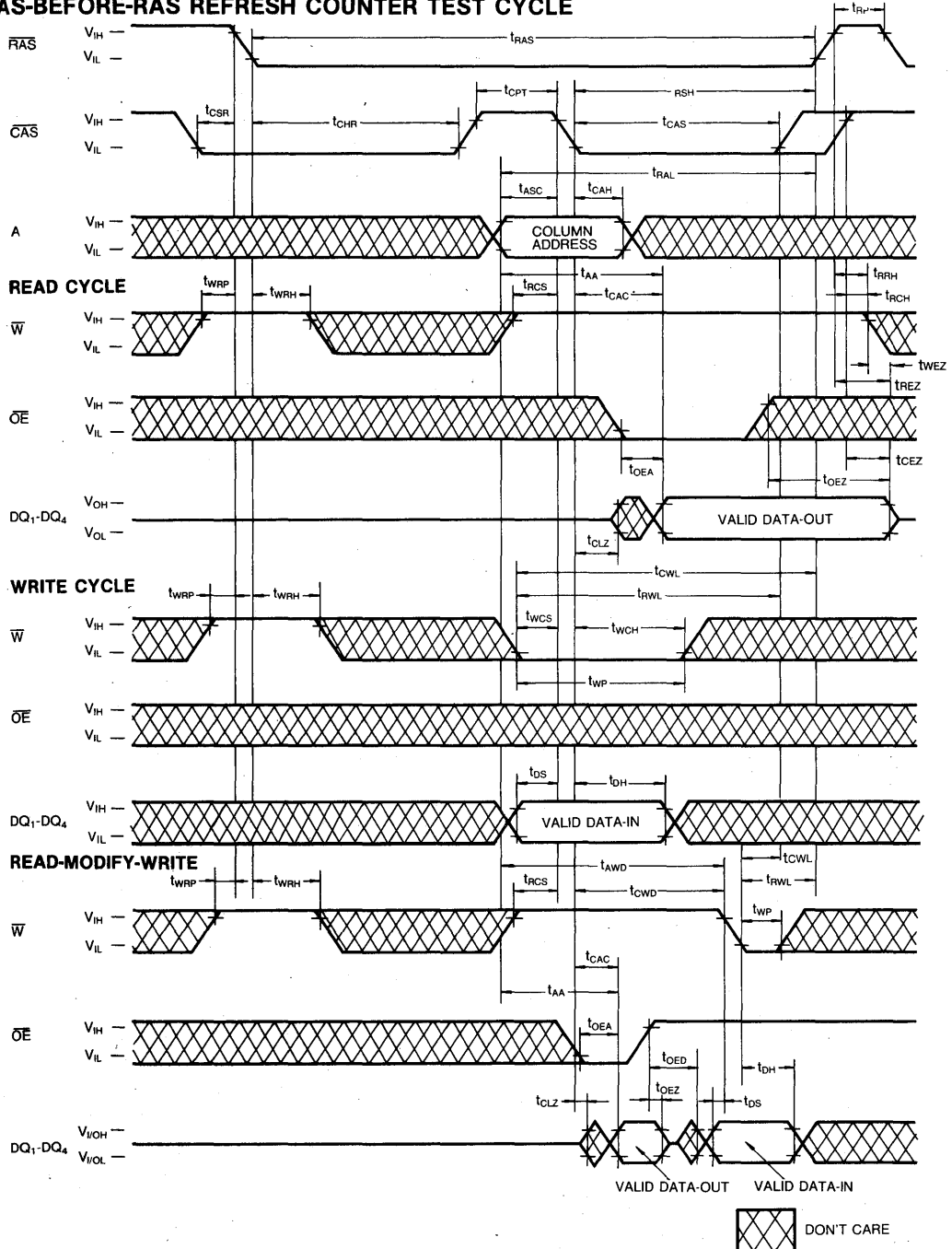
CAS-BEFORE-RAS REFRESH CYCLE

Note: \overline{OE} , Address=Don't Care



TIMING DIAGRAMS (Continued)

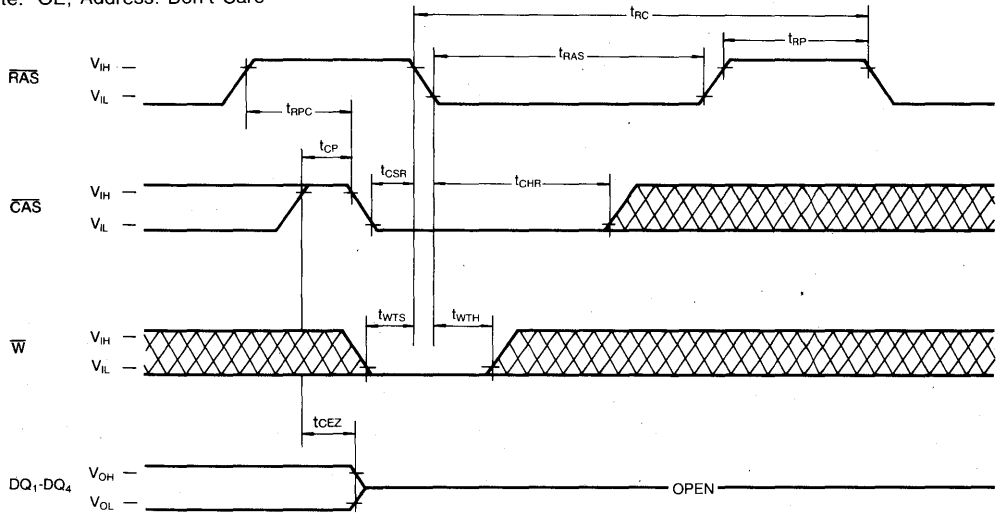
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

Note: \overline{OE} , Address: Don't Care

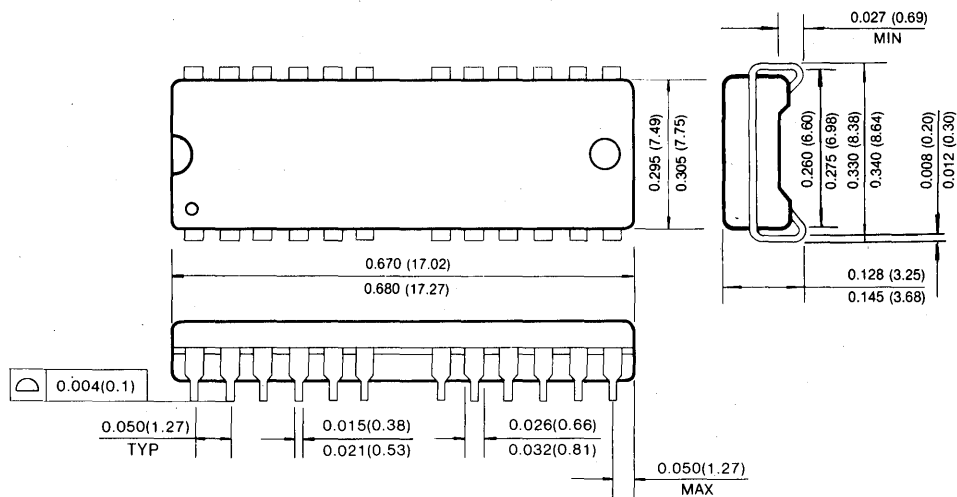


 DON'T CARE

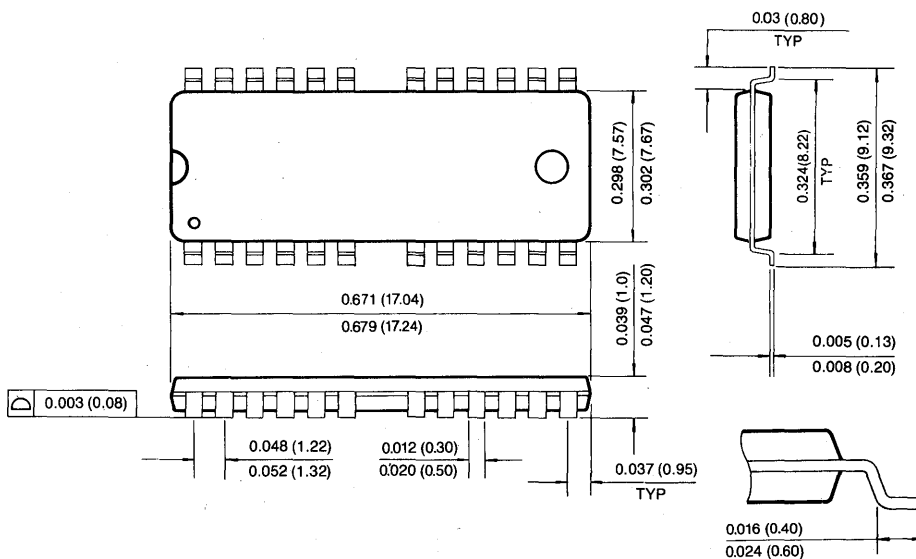
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



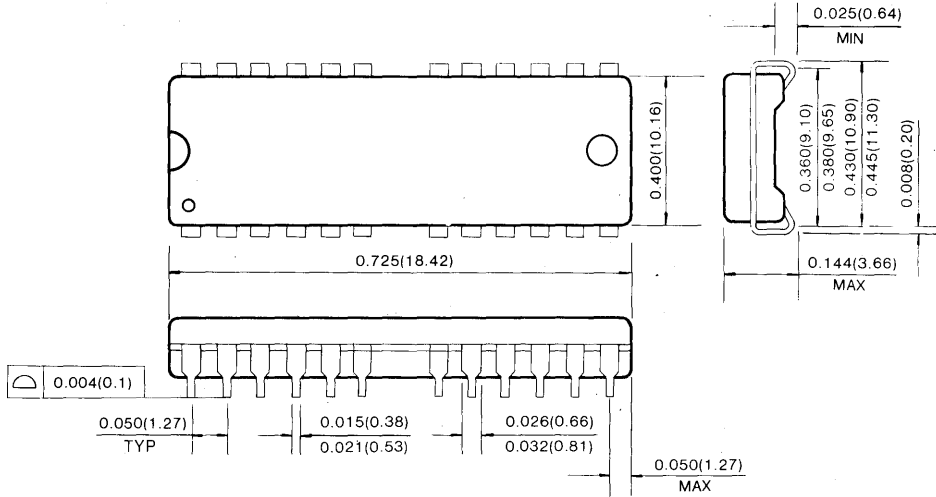
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



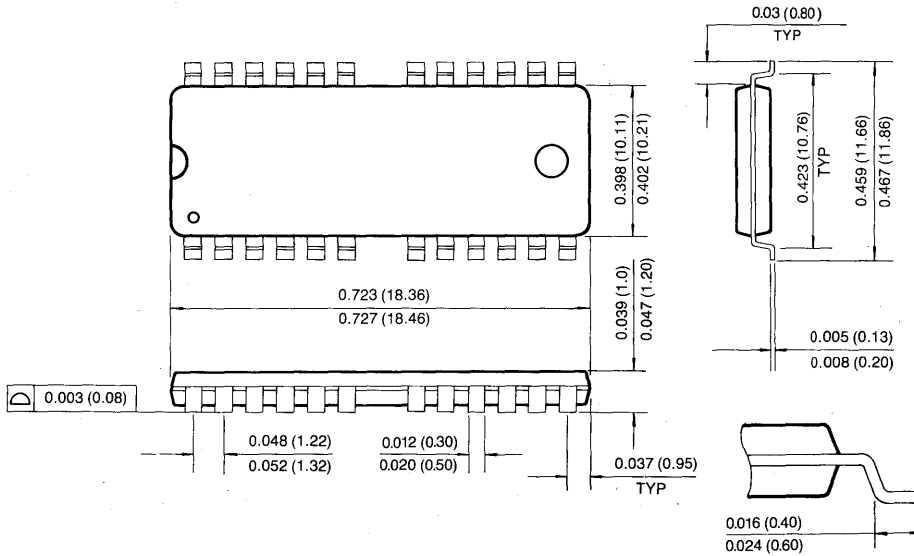
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)



4M × 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trC	tBPC
KM44V4104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44V4104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44V4104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh Operation (LL-ver. only)
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- LVTTTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+3.3V ± 0.3V power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

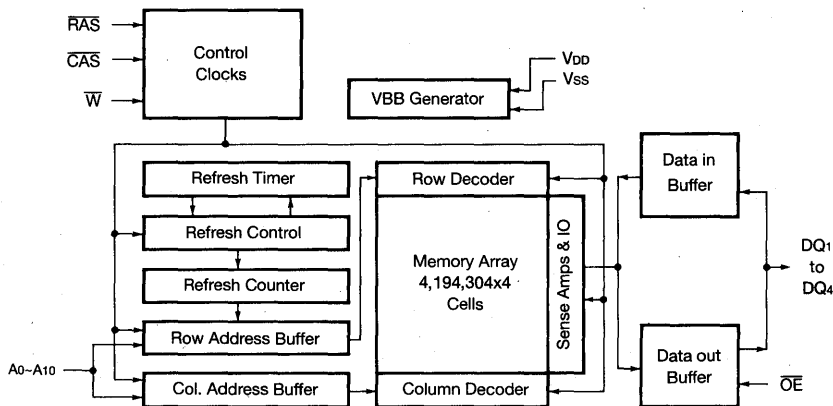
The Samsung KM44V4104A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

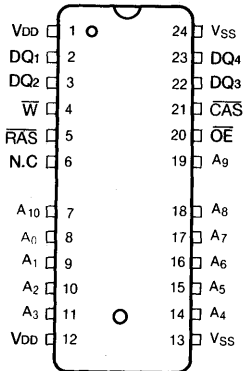
The KM44V4104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



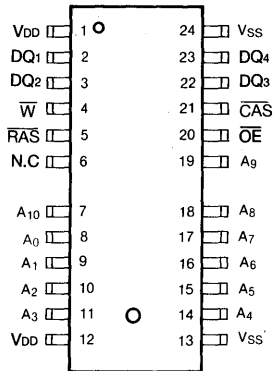
PIN CONFIGURATION (Top Views)

• KM44V4104 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



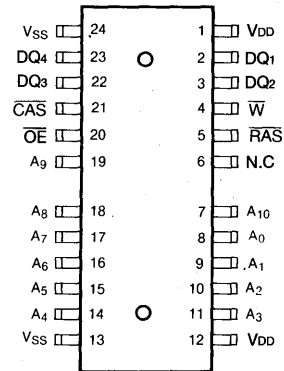
J : 400MIL
K : 300MIL

• KM44V4104 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44V4104 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5~ 4.6	V
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.5~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44V4104A/AL/ALL/ASL-6	I _{CC1}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Standby Current (RAS=CAS=W=V _{IH})	KM44V4104A	I _{CC2}	-	2	mA
	KM44V4104AL			1	mA
	KM44V4104ALL			1	mA
	KM44V4104ASL			1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM44V4104A/AL/ALL/ASL-6	I _{CC3}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM44V4104A/AL/ALL/ASL-6	I _{CC4}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Standby Current (RAS=CAS=W=V _{DD} -0.2V)	KM44V4104A	I _{CC5}	-	1	mA
	KM44V4104AL			300	μA
	KM44V4104ALL			200	μA
	KM44V4104ASL			200	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44V4104A/AL/ALL/ASL-6	I _{CC6}	-	100	mA
	KM44V4104A/AL/ALL/ASL-7			90	mA
	KM44V4104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V,DQ1~DQ4=Don't Care trc=62.5μs(L-Ver.) 125μs(SL-Ver.), tRAS=tRAS min.~300ns	KM44V4104AL	I _{CC7}	-	400	μA
	KM44V4104ASL			300	μA
Self Refresh Current RAS=CAS=2.0V W=OE=A0-A10=V _{DD} -0.2V or 0.2V DQ1~DQ4=V _{DD} -0.2V, 0.2V or Open	KM44V4104ALL	I _{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{in} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	IoL	-10	10	μA
Output High Voltage Level (I _{OH} =-2mA)	VOH	2.4	-	V
Output Low Voltage Level (I _{OL} =2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In Icc4, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₁₀)	CIN1	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	CIN2	-	7	pF
Output Capacitance (DQ ₁ ~DQ ₄)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD}=3.3V ± 0.3V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	3		3		3		ns	3
\overline{OE} to output in Low-Z	t _{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	t _{OFF}	3	15	3	50	3	20	ns	7,14,16
Transition time (rise and fall)	t _T	2	50	2	20	2	50	ns	2
\overline{RAS} precharge time	t _{RP}	40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	15		20		20		ns	
\overline{CAS} hold time	t _{CSH}	45		50		60		ns	
\overline{CAS} pulse width	t _{CAS}	10	10,000	15	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	trAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command hold time	twCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	10		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	twCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		65		70		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tcpWD	60		70		75		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tcPT	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcpA		35		40		45	ns	3
Hyper Page cycle time	thPC	24		29		34		ns	17
Hyper Page read-modify-write cycle time	thPRWC	71		86		96		ns	17
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tcp	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	trASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	35		40		45		ns	
$\overline{\text{OE}}$ access time	toEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	toED	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	toEZ	3	15	3	20	3	20	ns	7,14
\overline{OE} commend hold time	toEH	15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{C} -B- \overline{R} refresh)	twRP	10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} -B- \overline{R} refresh)	twRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,16
\overline{OE} to CAS hold time	toCH	5		5		5		ns	
CAS hold time to \overline{OE}	tCHO	5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		ns	
\overline{W} pulse width(Hyper Page cycle)	twPE	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	treZ	3	15	3	20	3	20	ns	7,14,16
Output buffer turn off delay from \overline{W}	twEZ	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	twED	15		20		20		ns	
RAS pulse width (LL-Ver)	trASS	100		100		100		μ s	15
RAS precharge time (LL-Ver)	trPS	110		130		150		ns	15
CAS hold time (LL-Ver)	tCHS	-50		-50		-50		ns	15

5

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	115		135		155		ns	
Read-modify-write cycle time	trWC	160		190		210		ns	
Access time from \overline{RAS}	trAC		65		75		85	ns	3,4,11
Access time from \overline{CAS}	trAC		20		20		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	trCAS	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	20		25		25		ns	
\overline{CAS} hold time	trSH	20		55		65		ns	
Column address to \overline{RAS} lead time	trAL	35		40		45		ns	
\overline{CAS} to \overline{W} delay time	trWD	45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	60		70		75		ns	8
Hyper Page mode cycle time	tHPC	29		34		39		ns	
Hyper Page mode read-modify-write cycle time	tHPRWC	76		91		101		ns	
\overline{RAS} pulse width (Hyper Page Mode)	trASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE(Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		40		45		50	ns	
$\overline{\text{OE}}$ access time	tOEA		20		25		25	ns	3
$\overline{\text{OE}}$ to data delay	tOED	20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTION

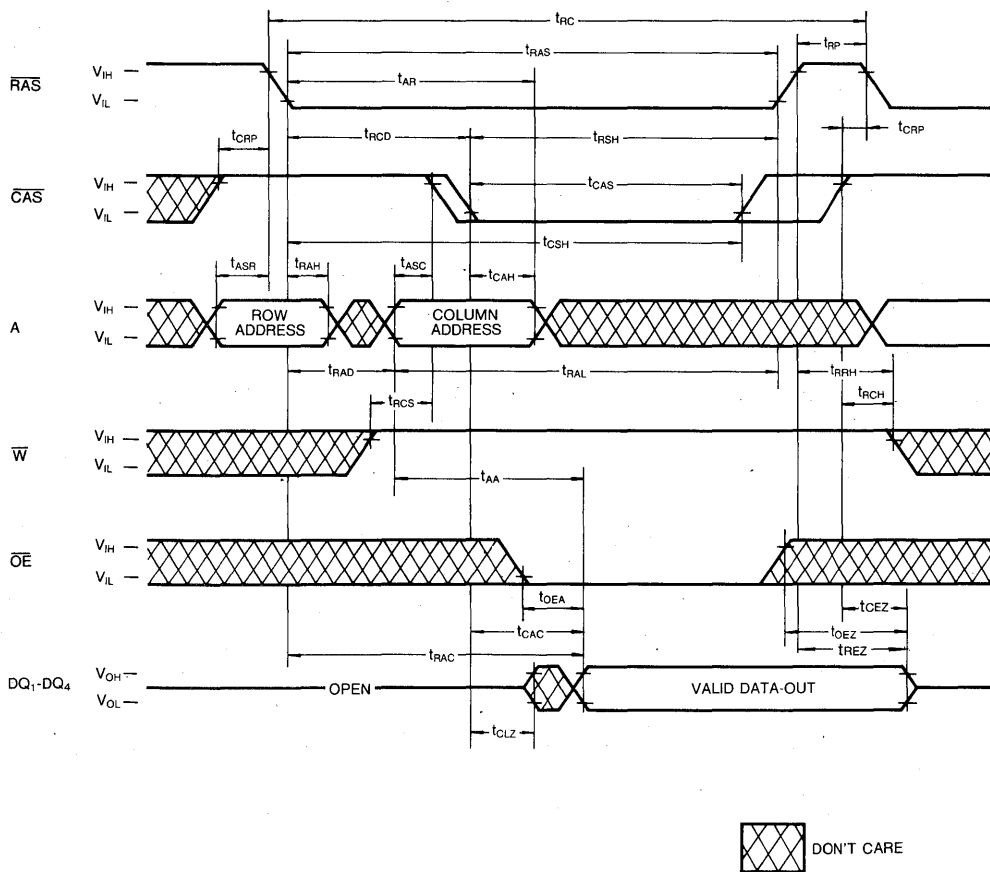
The KM44V4104A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A₀ is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM.

$\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And " $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" or " $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time (1/4 in cases of N test pattern)

NOTES

- An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
- Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{out}=2mA), V_{Ol}=0.8V(I_{out}=2mA)
- Operation within the t_{RCd}(max) limit insures that t_{TRAC}(max) can be met. t_{TRCD}(max) is specified as a reference point only. If t_{TRCD} is greater than the specified t_{TRCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{TRCD} ≥ t_{TRCD}(max).
- t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{TRAD}(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCs}, t_{TRWD}, t_{TCWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If t_{WCs} ≥ t_{WCs}(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{TCWD} ≥ t_{TCWD}(min), t_{TRWD} ≥ t_{TRWD}(min) and t_{AWD} ≥ t_{AWD}(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
- Operation within the t_{TRAD}(max) limit insures that t_{TRAC}(max) can be met. t_{TRAD}(max) is specified as a reference point only. If t_{TRAD} is greater than the specified t_{TRAD}(max) limit, then access time is controlled by t_{AA}.
- These specifications are applied in the test mode.
- In test mode read cycle, the value of t_{TRAC}, t_{AA}, t_{TCAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
- t_{TREZ}(max), t_{TCEZ}(max), t_{TWEZ}(max) and t_{TOEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
- If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going
- t_{ASC} ≥ t_{CP}(min), Assumn t_r=2.0ns

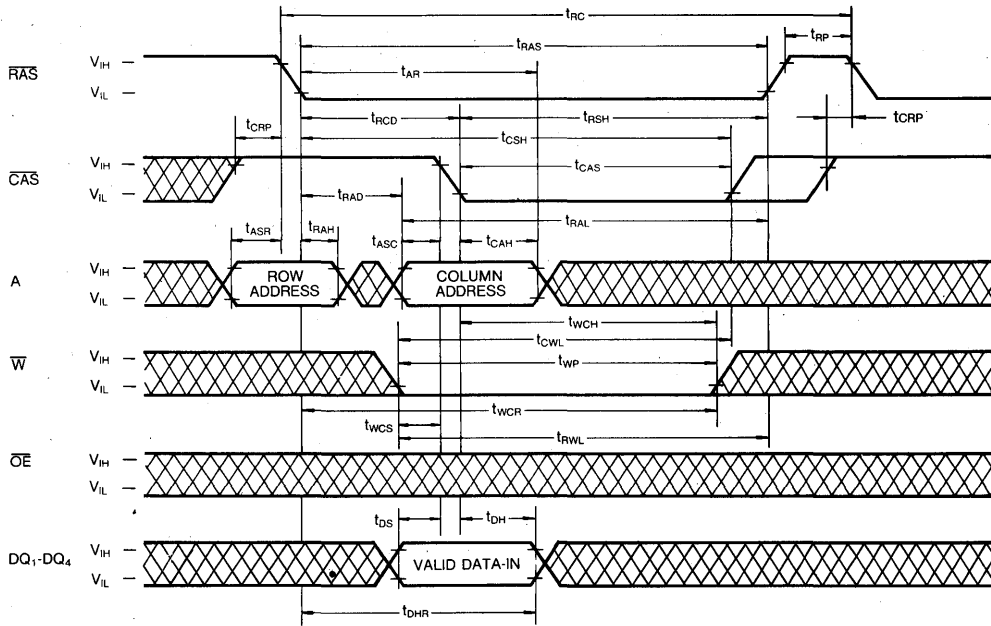
TIMING DIAGRAMS
READ CYCLE



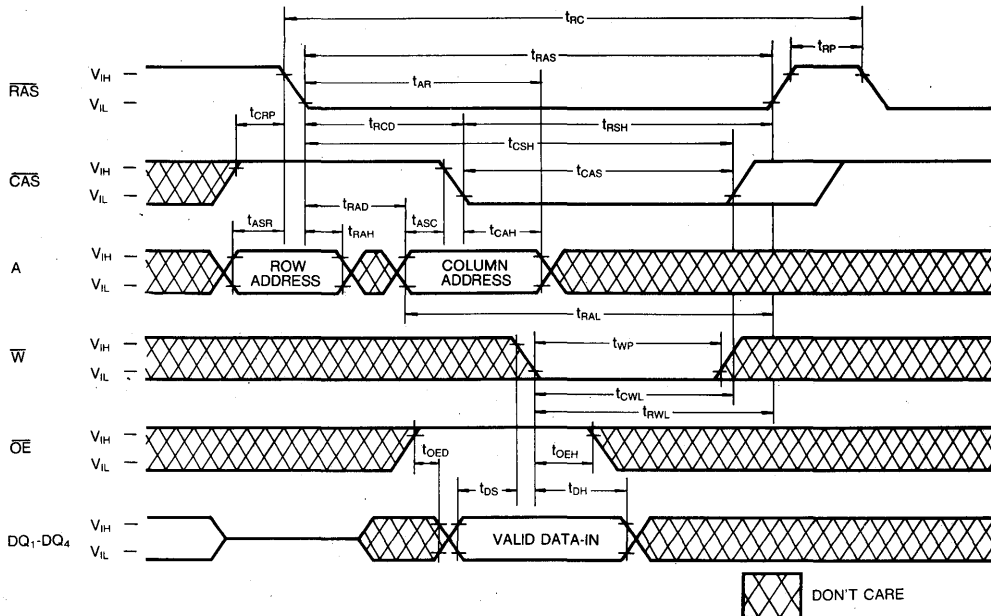
5

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



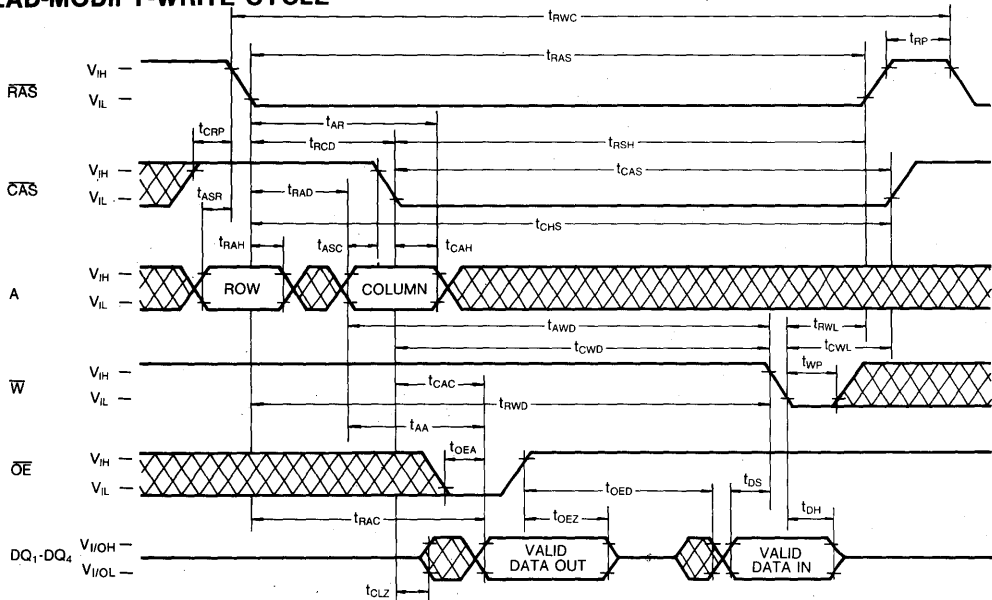
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



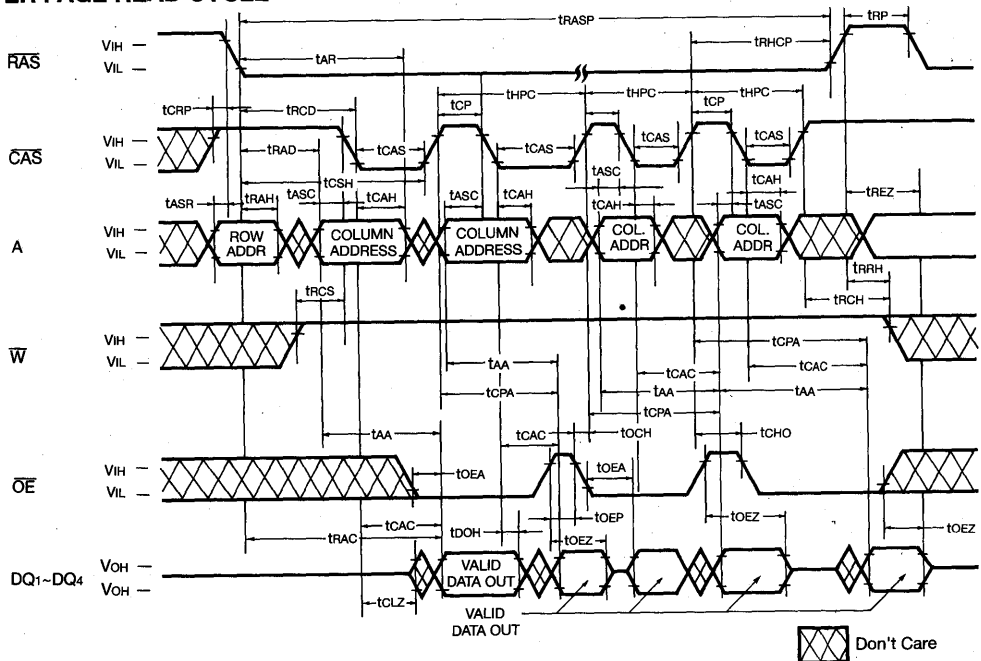
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



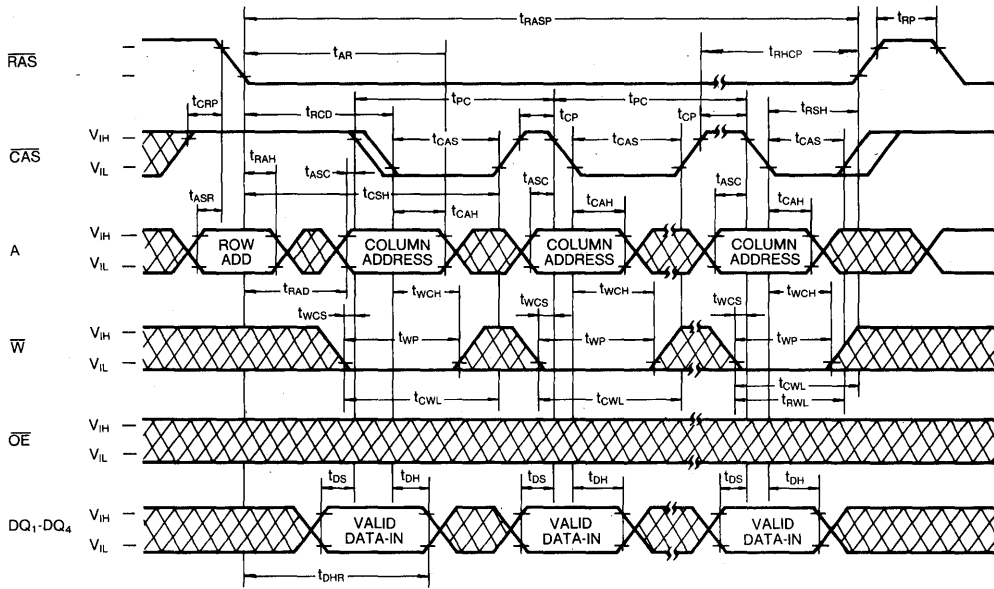
HYPER PAGE READ CYCLE



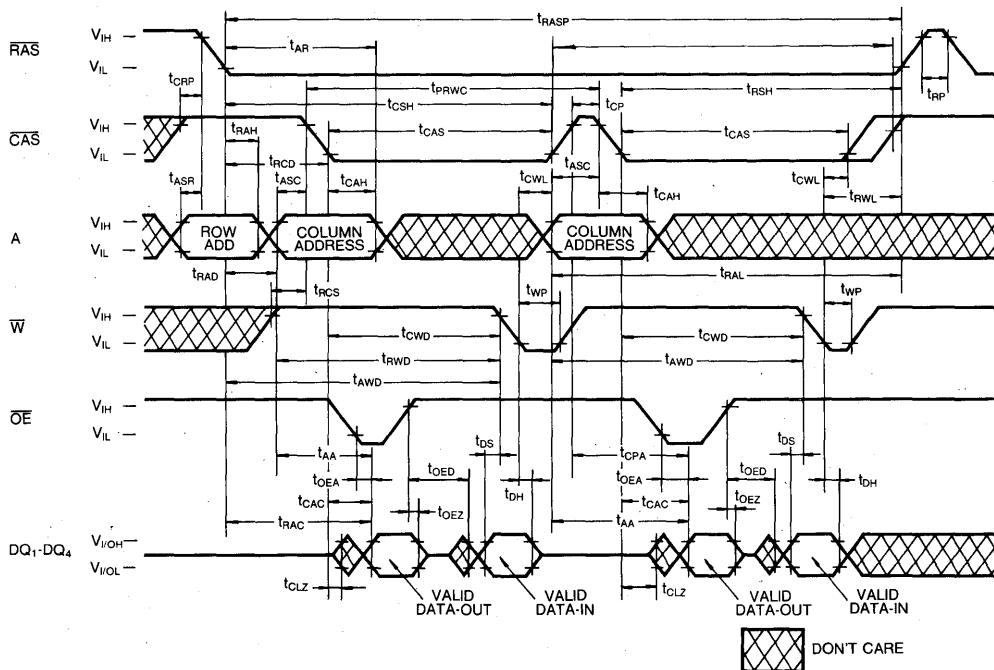
5

TIMING DIAGRAMS (Continued)

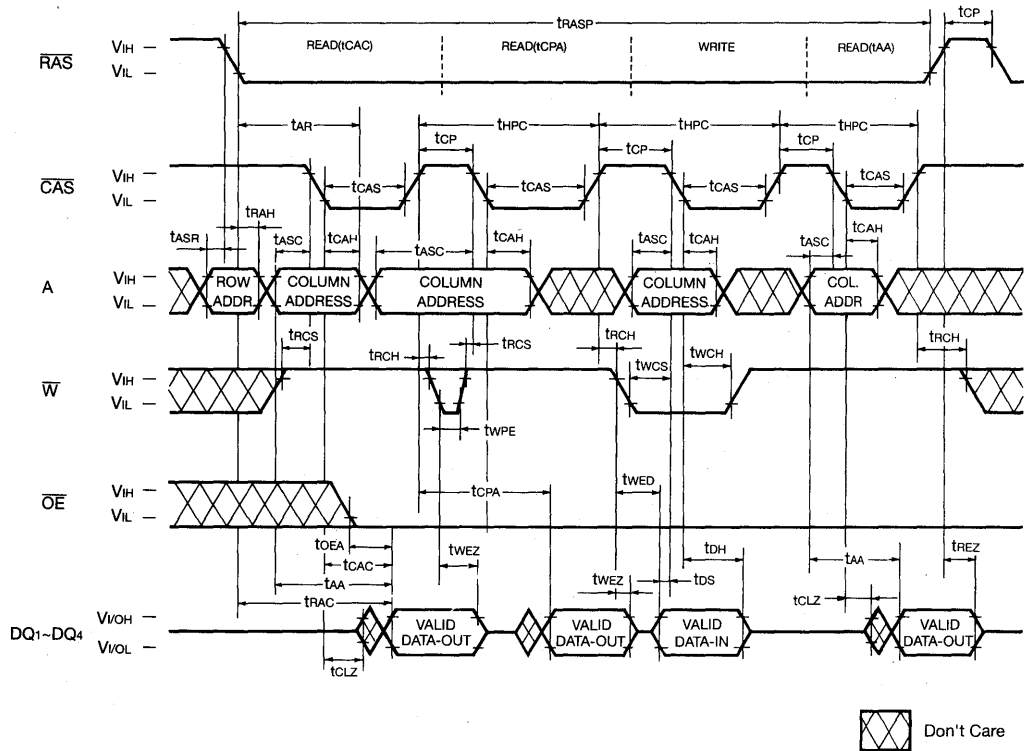
HYPER PAGE WRITE CYCLE (EARLY WRITE)



HYPER PAGE READ-MODIFY-WRITE CYCLE



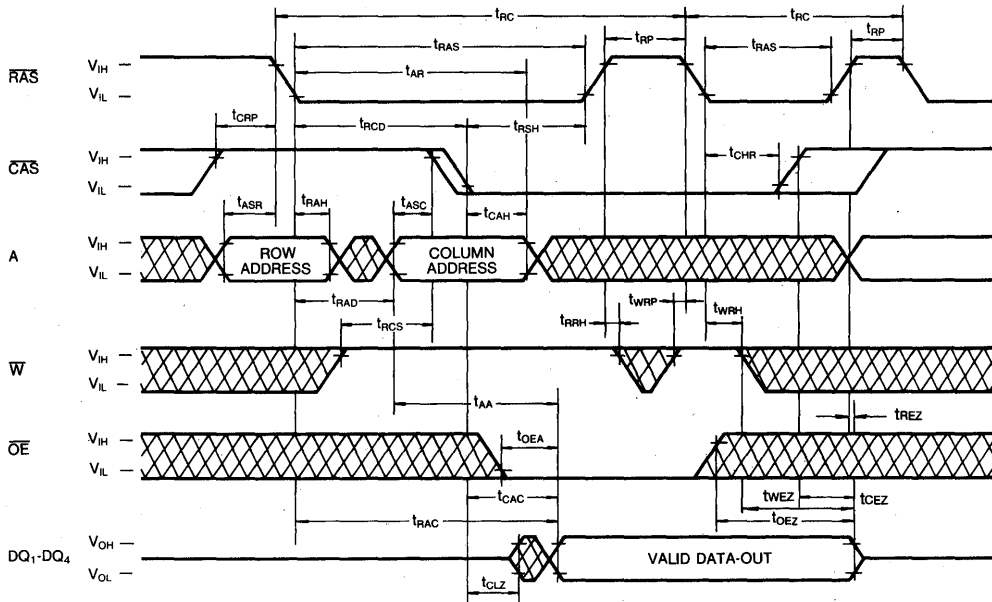
HYPER PAGE READ AND WRITE MIXED CYCLE



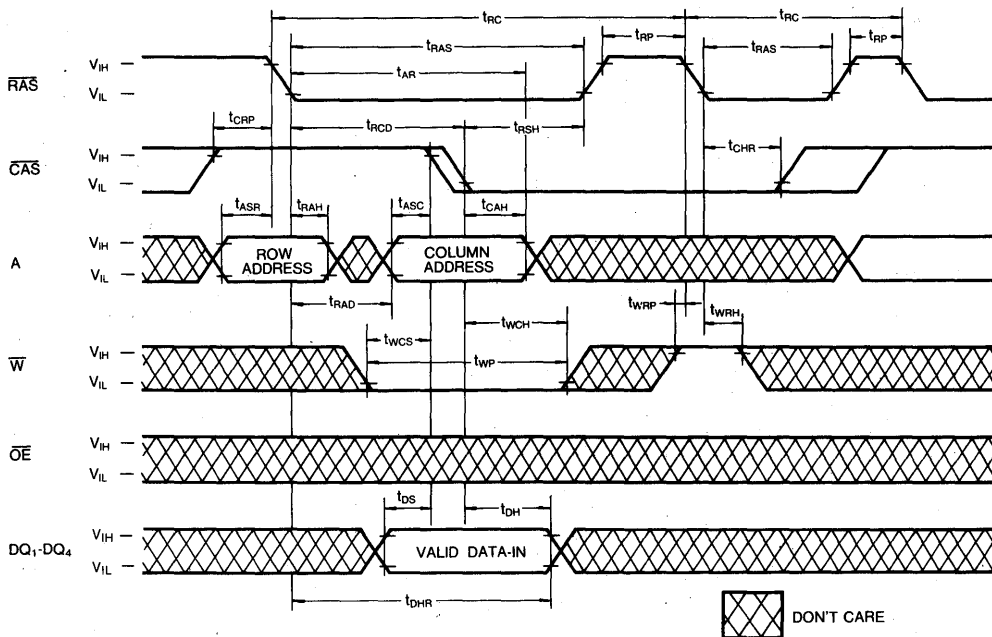
5

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



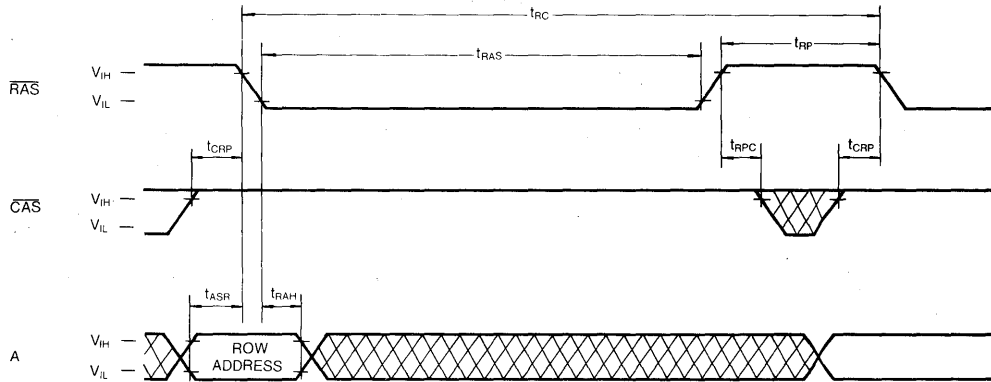
HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

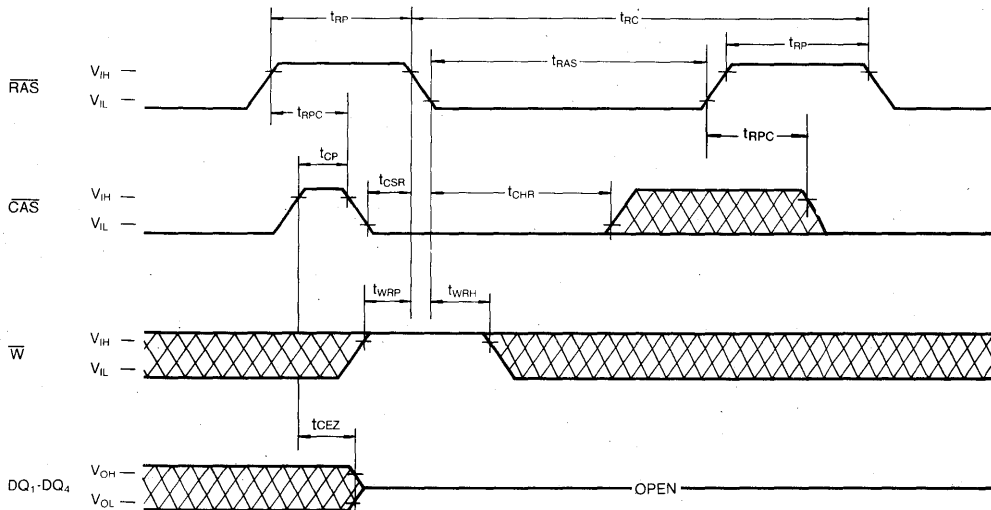
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

Note: \bar{OE} , Address=Don't Care

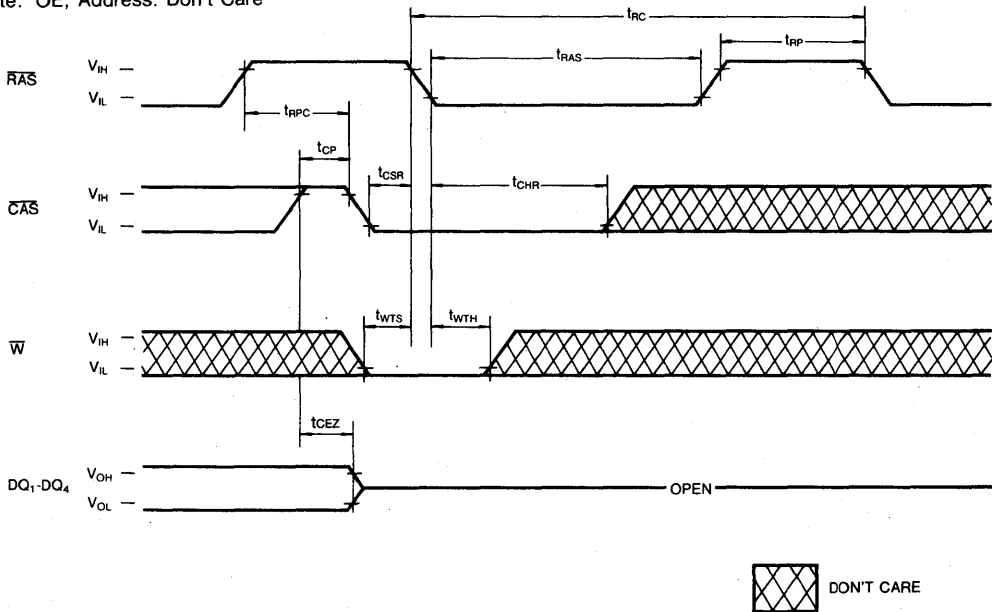


5

TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

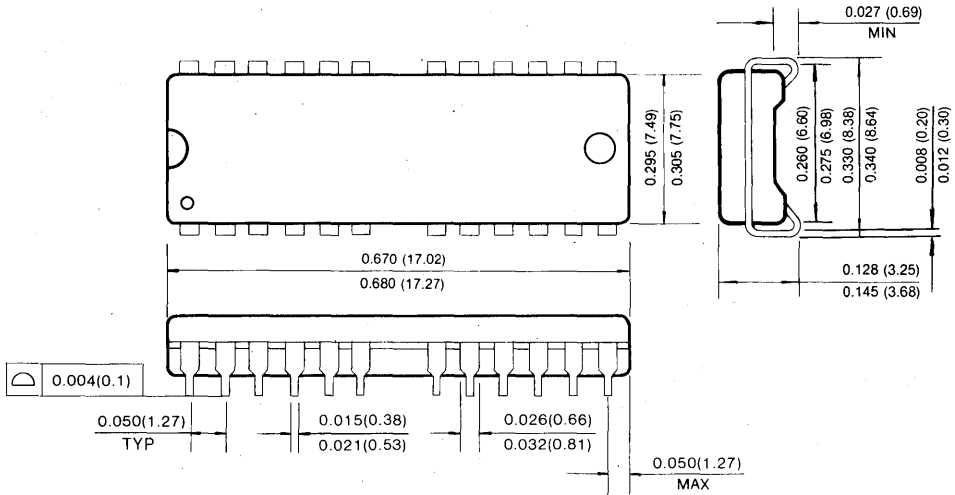
Note: $\bar{O}\bar{E}$, Address: Don't Care



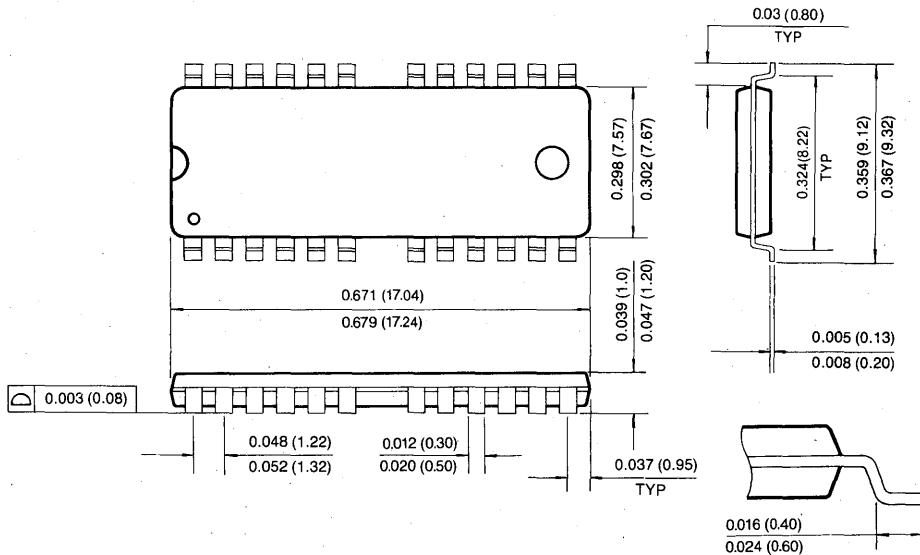
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



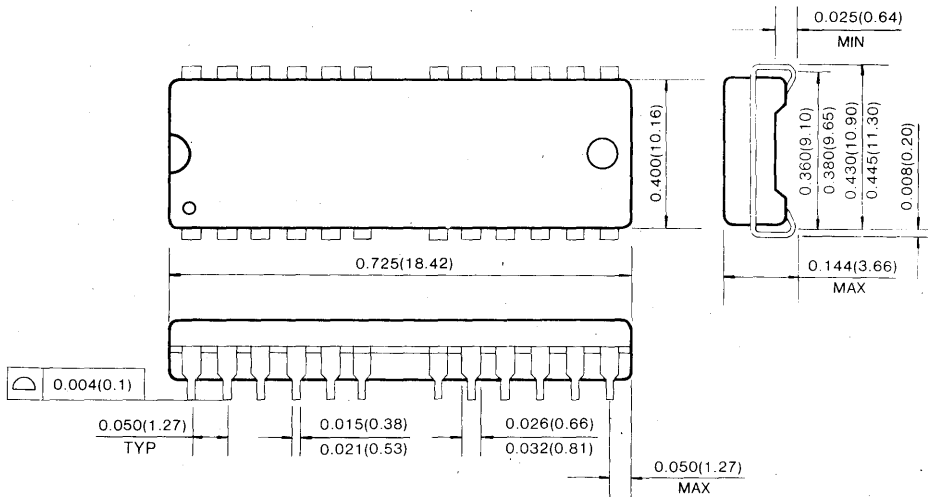
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



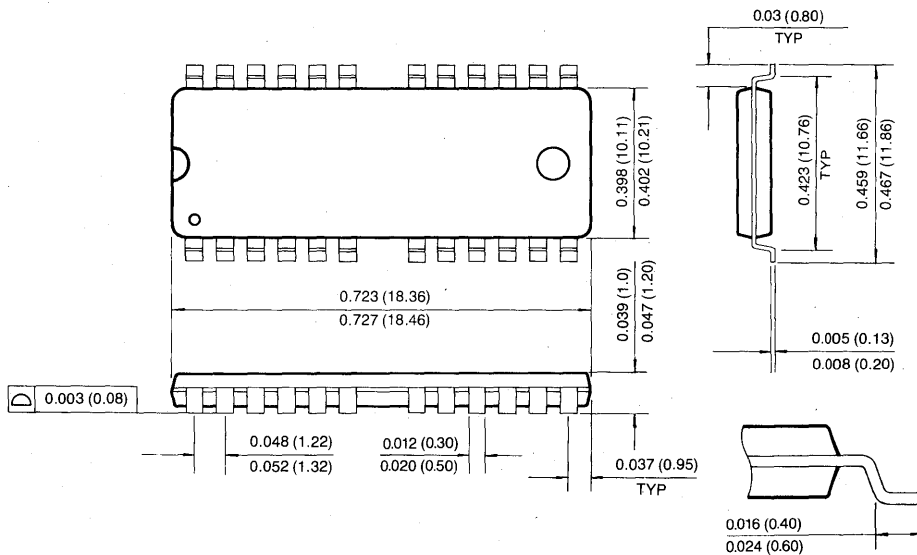
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)

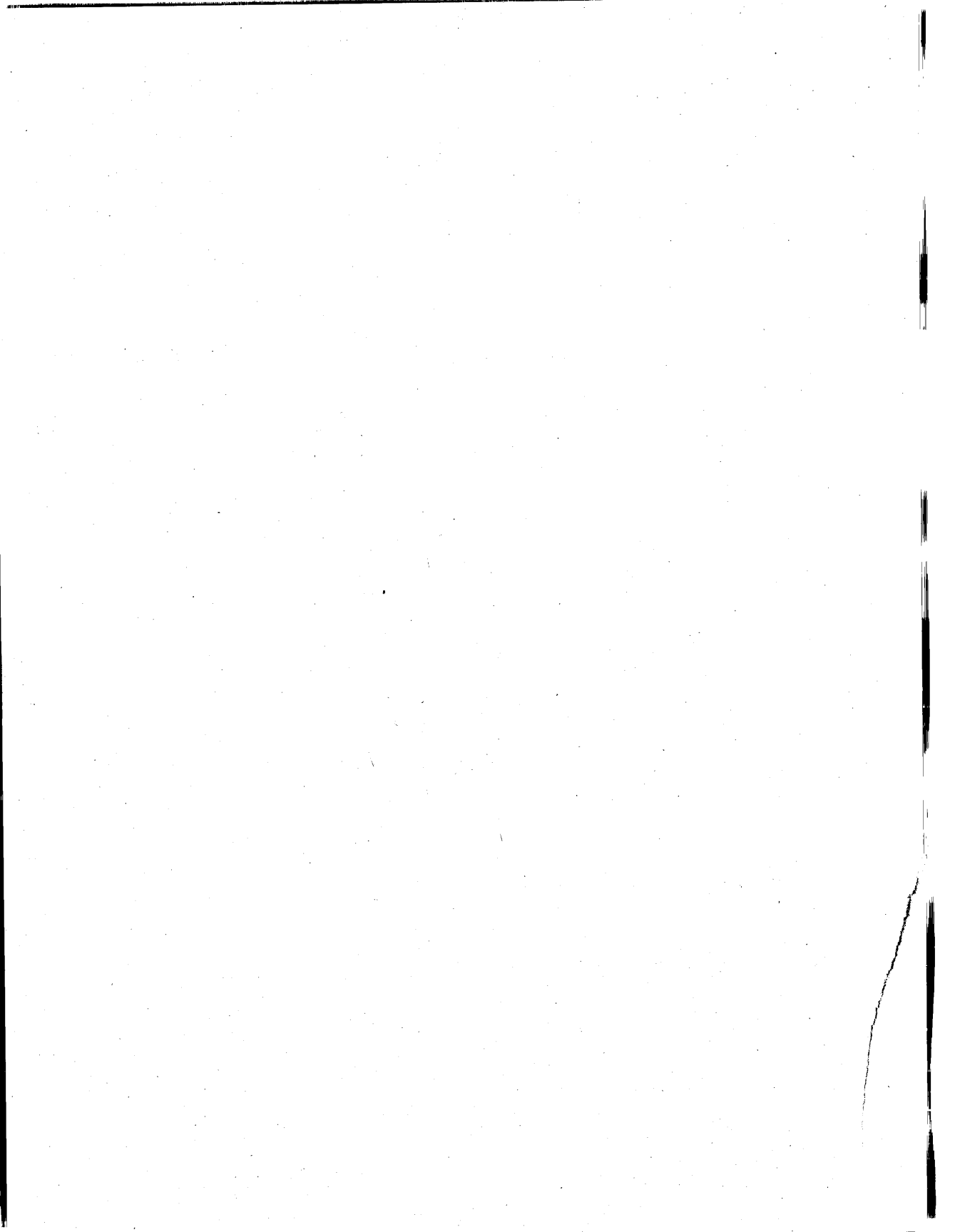


5



16M B/W DRAM DATA SHEET 6

- 42. KM48C
- 43. KM48
- 44. KM48
- 45. KM48
- 46. KM48
- 47. KM48
- 48. KM48
- 49. KM48
- 50. KM48
- 51. KM48
- 52. KM48
- 53. KM48
- 54. KM48
- 55. KM48
- 56. KM48
- 57. KM48
- 58. KM48
- 59. KM48
- 60. KM48



2M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM48C2000A/AL/ALL/ASL-5	50ns	13ns	90ns
KM48C2000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48C2000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48C2000A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

GENERAL DESCRIPTION

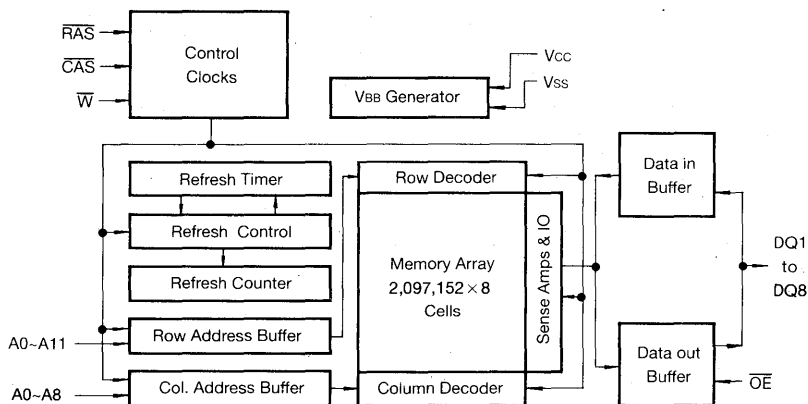
The Samsung KM48C2000A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

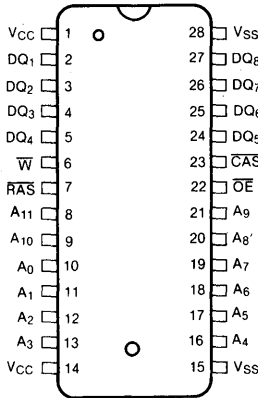
The KM48C2000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

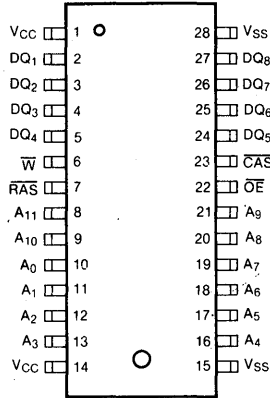


PIN CONFIGURATION (Top Views)

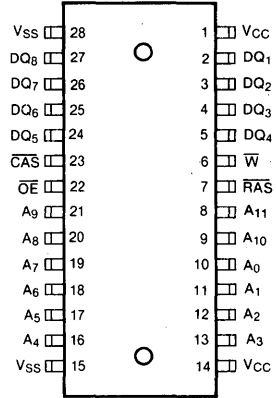
• KM48C2000 AJ/ALJ/ALLJ/ASLJ



• KM48C2000 AT/ALT/ALLT/ASLT



• KM48C2000 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-8	Data In/Out
Vss	Ground
RAS	Row Address Strobe
\bar{CAS}	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (R _{AS} and C _{AS} Cycling @ t _{RC} =min.)	KM48C2000A/AL/ALL/ASL-5 KM48C2000A/AL/ALL/ASL-6 KM48C2000A/AL/ALL/ASL-7 KM48C2000A/AL/ALL/ASL-8	I _{CC1}	-	90	mA
				80	mA
				70	mA
				60	mA
Standby Current (R _{AS} =C _{AS} =W=V _{IH})	KM48C2000A KM48C2000AL KM48C2000ALL KM48C2000ASL	I _{CC2}	-	2	mA
				1	mA
				1	mA
				1	mA
R _{AS} -Only Refresh Current* (C _{AS} =V _{IH} , R _{AS} Cycling @ t _{RC} =min.)	KM48C2000A/AL/ALL/ASL-5 KM48C2000A/AL/ALL/ASL-6 KM48C2000A/AL/ALL/ASL-7 KM48C2000A/AL/ALL/ASL-8	I _{CC3}	-	90	mA
				80	mA
				70	mA
				60	mA
Fast Page Mode Current* (R _{AS} =V _{IL} , C _{AS} , Address Cycling @ t _{PC} =min.)	KM48C2000A/AL/ALL/ASL-5 KM48C2000A/AL/ALL/ASL-6 KM48C2000A/AL/ALL/ASL-7 KM48C2000A/AL/ALL/ASL-8	I _{CC4}	-	80	mA
				70	mA
				60	mA
				50	mA
Standby Current (R _{AS} =C _{AS} =W=V _{CC} -0.2V)	KM48C2000A KM48C2000AL KM48C2000ALL KM48C2000ASL	I _{CC5}	-	1	mA
				300	μA
				200	μA
				200	μA
C _{AS} -Before-R _{AS} Refresh Current* (R _{AS} and C _{AS} Cycling @ t _{RC} =min.)	KM48C2000A/AL/ALL/ASL-5 KM48C2000A/AL/ALL/ASL-6 KM48C2000A/AL/ALL/ASL-7 KM48C2000A/AL/ALL/ASL-8	I _{CC6}	-	90	mA
				80	mA
				70	mA
				60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V C _{AS} =C _{AS} -Before-R _{AS} Cycling or 0.2V D _{IN} =Don't Care Trc=31.25μS(L-Ver.) 62.5μS(SL-Ver.), TRAS ≤ 300ns	KM48C2000AL KM48C2000ASL	I _{CC7}	-	450	μA
				350	μA

6

DC AND OPERATING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ8=Vcc-0.2V, 0.2V or Open	lccs	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: lcc1, lcc3, lcc4 and lcc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. lcc is specified as an average current. In lcc1 and lcc3, Address can be changed maximum two times while RAS=VIL. In lcc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1-DQ8)	CbQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, Vcc=5.0V ± 0.5V, See notes 1,2)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CAS hold time	tcSH	50		60		70		80		ns	
CAS pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tcRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	trAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	trAL	25		30		35		40		ns	
Read command set-up time	trCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		0		ns	
Write command hold time	twCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	twCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tcPT	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width(Fast Page mode)	trASP	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	

6



AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	
W to RAS precharge time (\overline{C} -B- \overline{R} refresh)	tWRP	10		10		10		10		ns	
W to RAS hold time (\overline{C} -B- \overline{R} refresh)	tWRH	10		10		10		10		ns	
RAS pulse width (\overline{C} -B- \overline{R} self refresh)	tRASS	100		100		100		100		μ s	15
RAS precharge time (\overline{C} -B- \overline{R} self refresh)	tRPS	90		110		130		150		ns	15
CAS hold time (\overline{C} -B- \overline{R} self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from RAS	tRAC		55		65		75		85	ns	3,4,11
Access time from CAS	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
RAS pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
CAS pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	tRSH	18		20		25		25		ns	
CAS hold time	tCSH	55		65		75		85		ns	
Column address to RAS lead time	tRAL	30		35		40		45		ns	
CAS to \overline{W} delay time	tCWD	41		45		55		55		ns	8
RAS to \overline{W} delay time	tRWD	78		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
RAS pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tCPA		35		40		45		50	ns	3
\overline{OE} access time	tOEA		18		20		25		25	ns	
\overline{OE} to data delay	tOED	18		20		25		25		ns	
\overline{OE} command hold time	tOEH	18		20		25		25		ns	

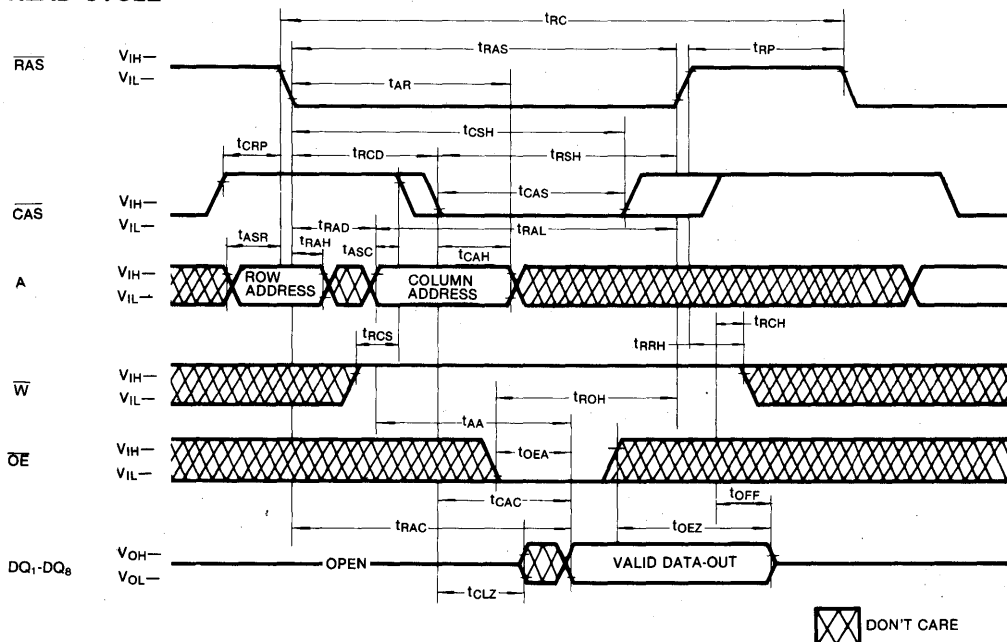
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a

- read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAMS

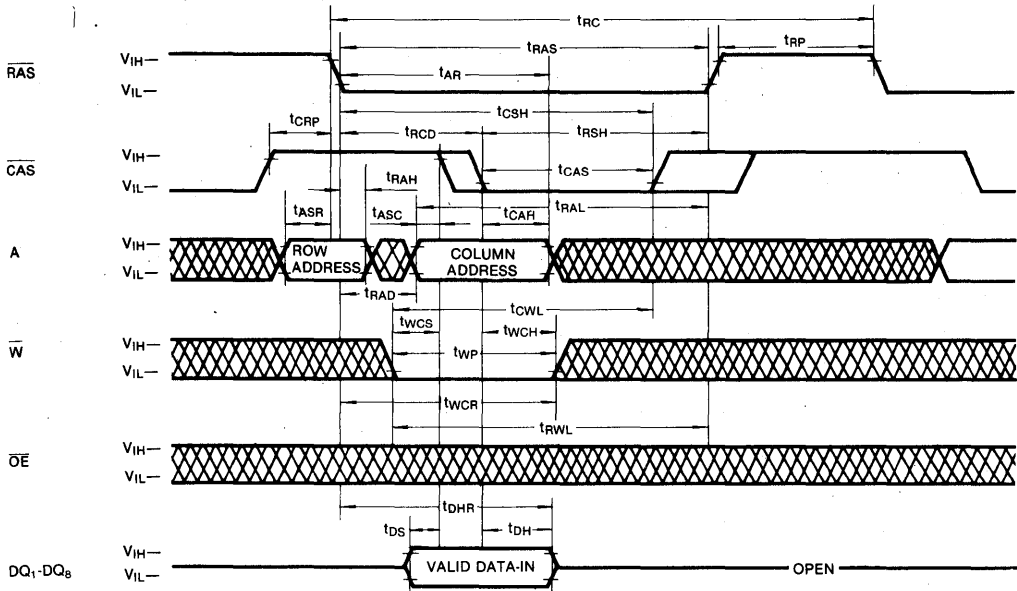
READ CYCLE



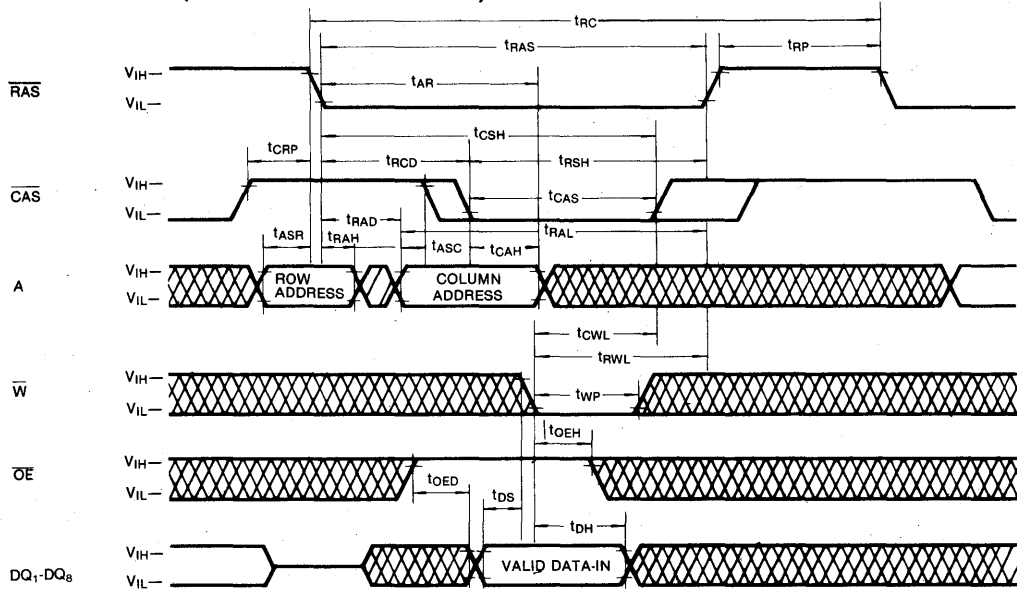
6

TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



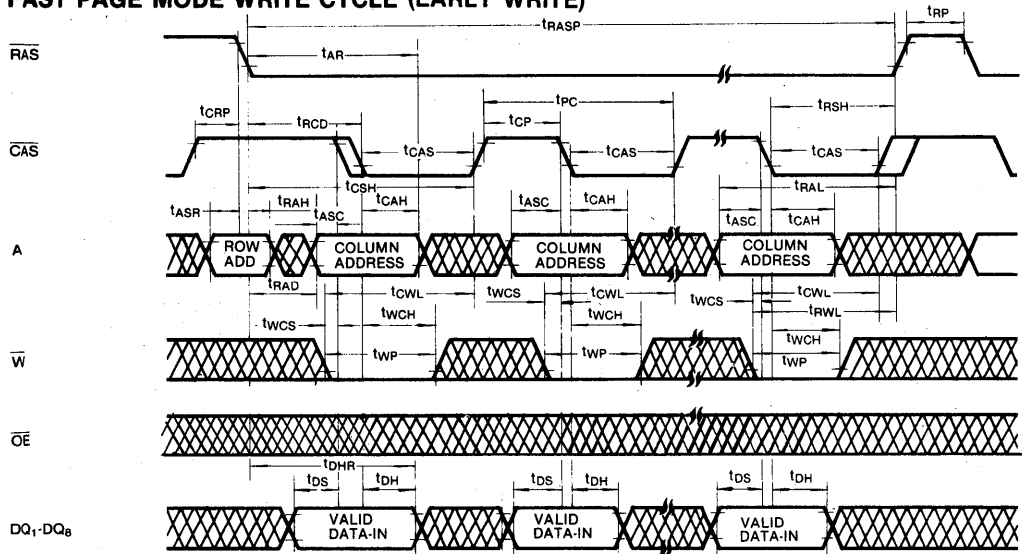
WRITE CYCLE (OE CONTROLLED WRITE)



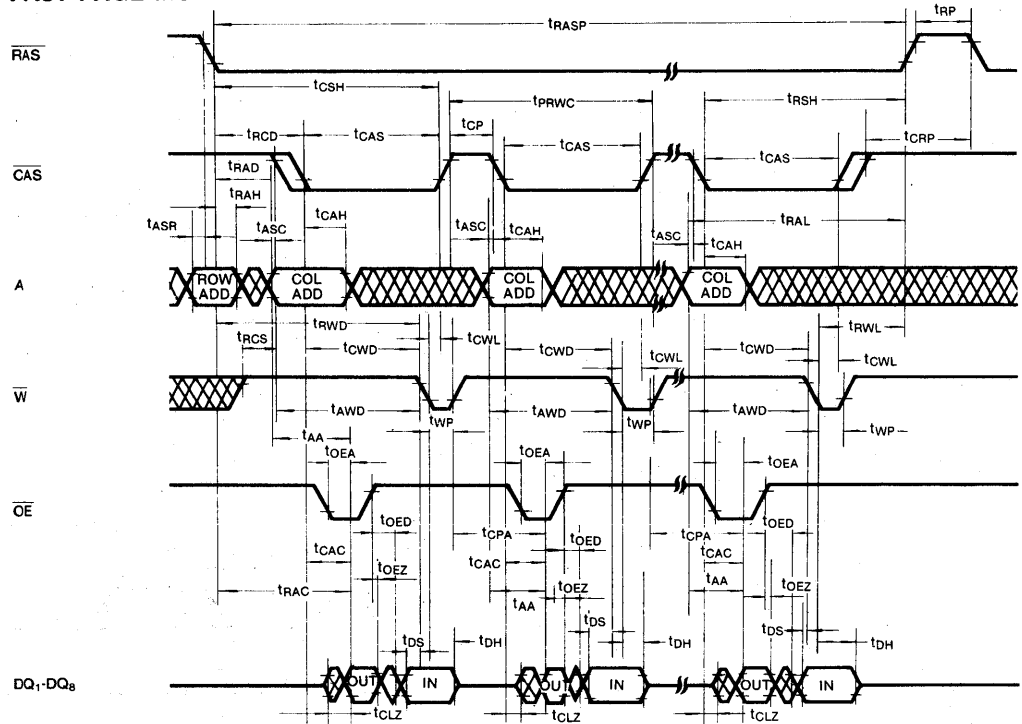
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

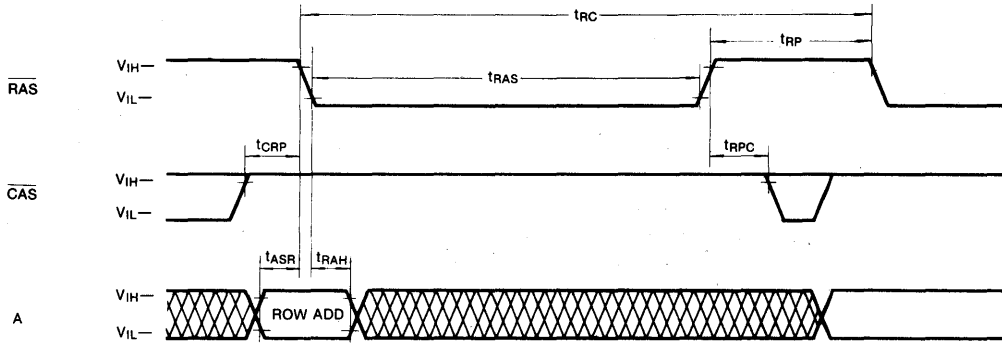


 DON'T CARE

TIMING DIAGRAMS (Continued)

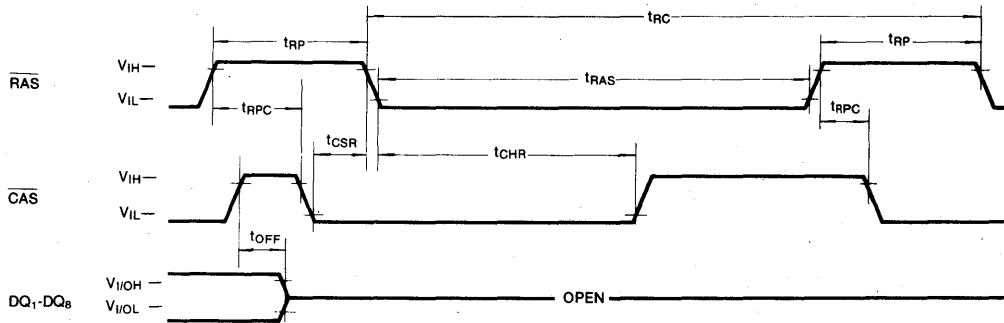
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



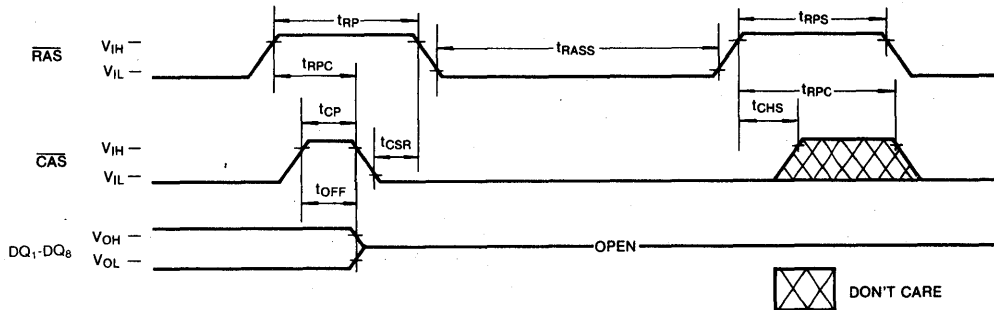
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \bar{W} =VIH, \bar{OE} , A=Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

NOTE: \bar{W} , \bar{OE} , A=Don't Care

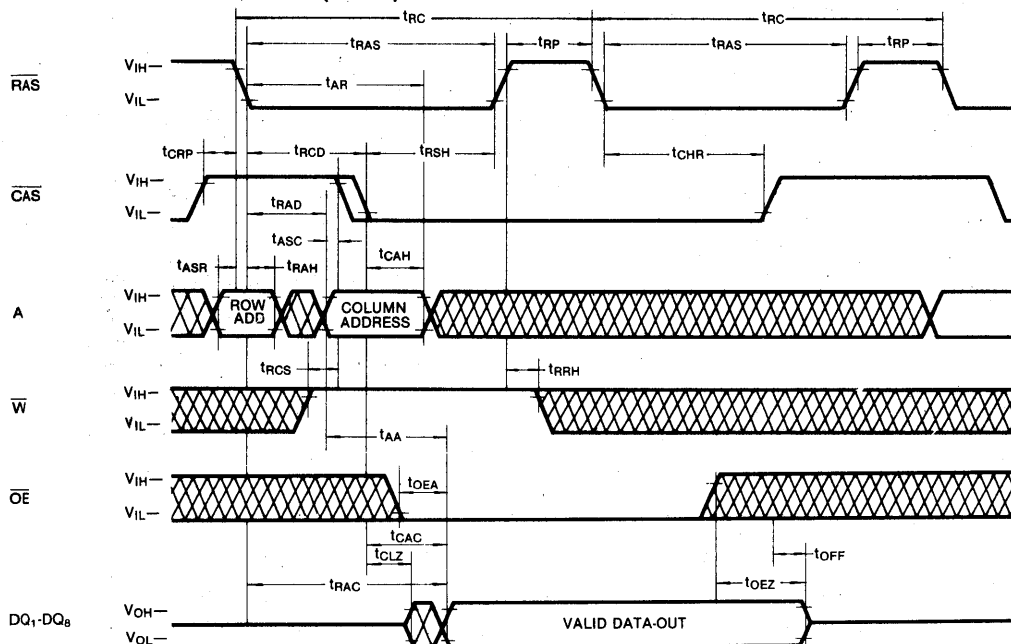


 DON'T CARE

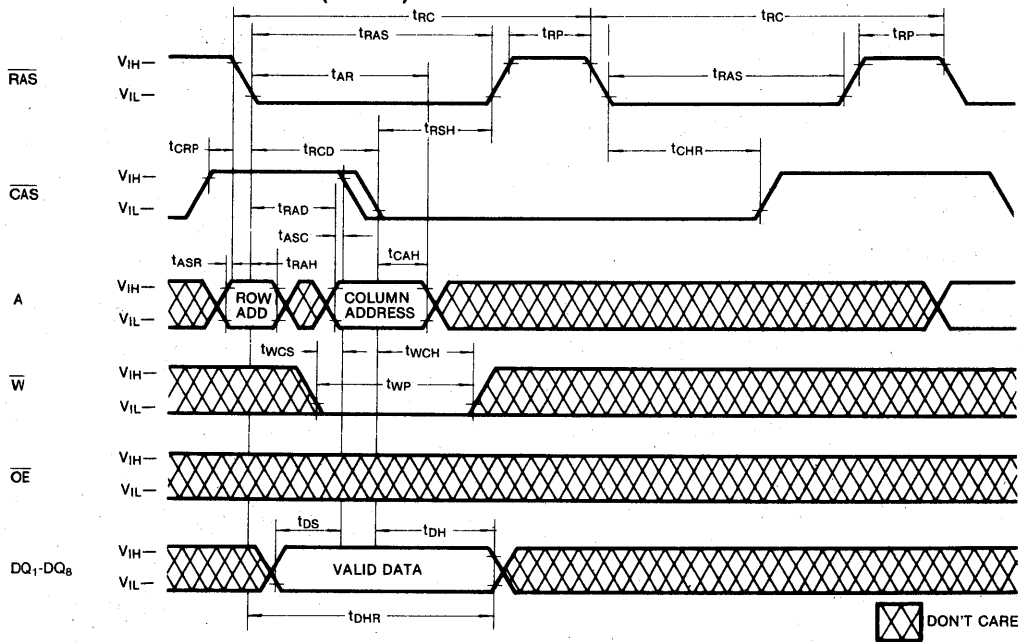
6

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

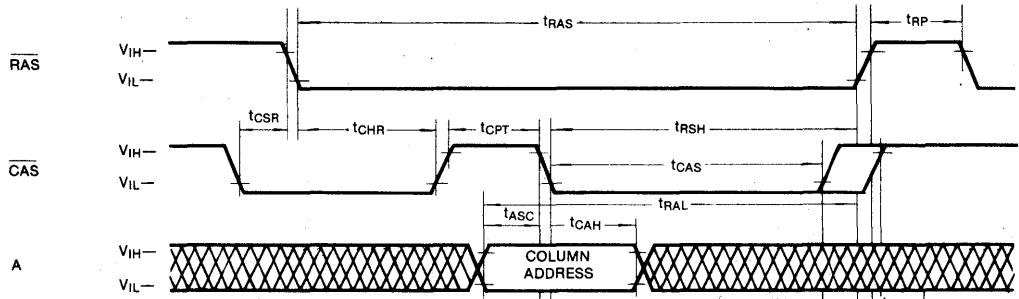


HIDDEN REFRESH CYCLE (WRITE)

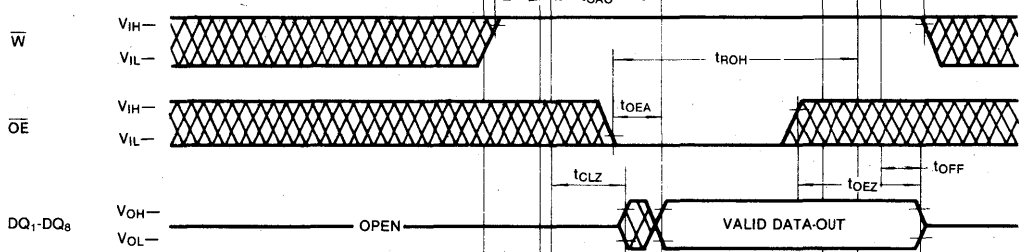


TIMING DIAGRAMS (Continued)

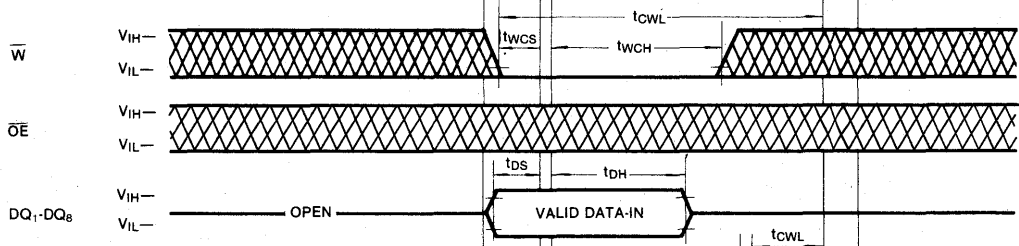
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



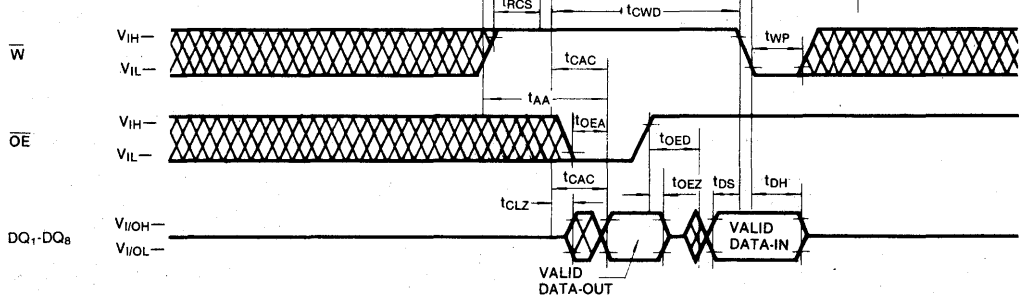
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



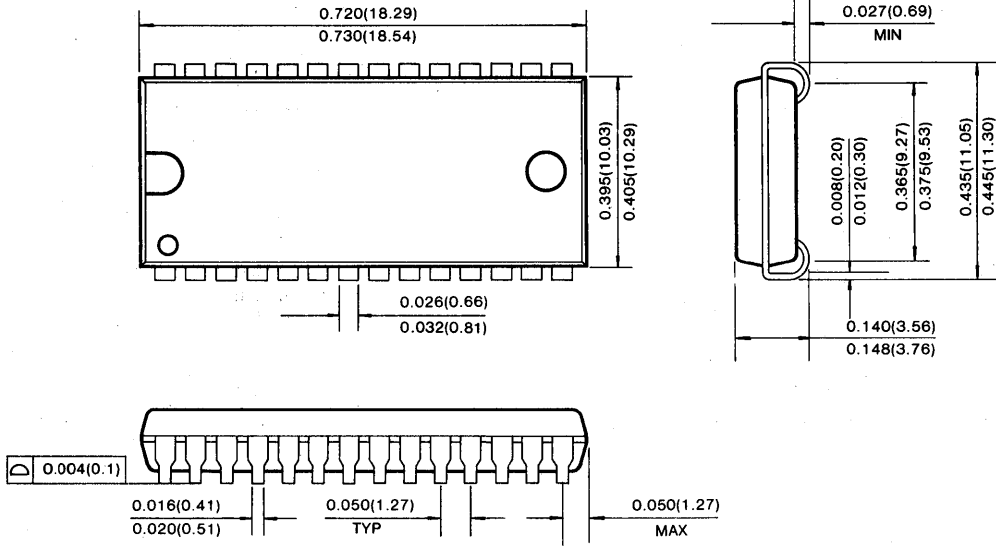
 DON'T CARE

6

PACKAGE DIMENSION

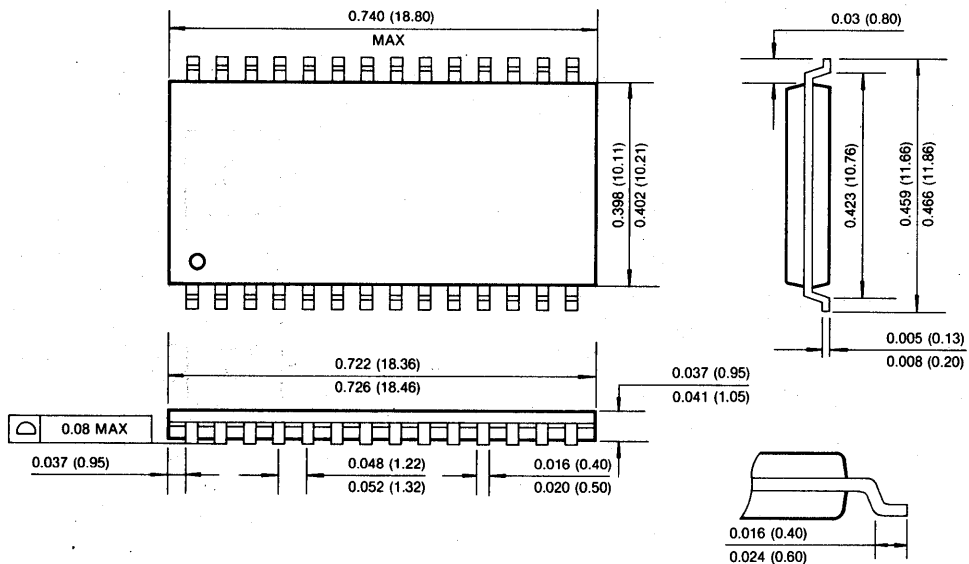
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M × 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM48C2100A/AL/ALL/ASL-5	50ns	13ns	90ns
KM48C2100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48C2100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48C2100A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

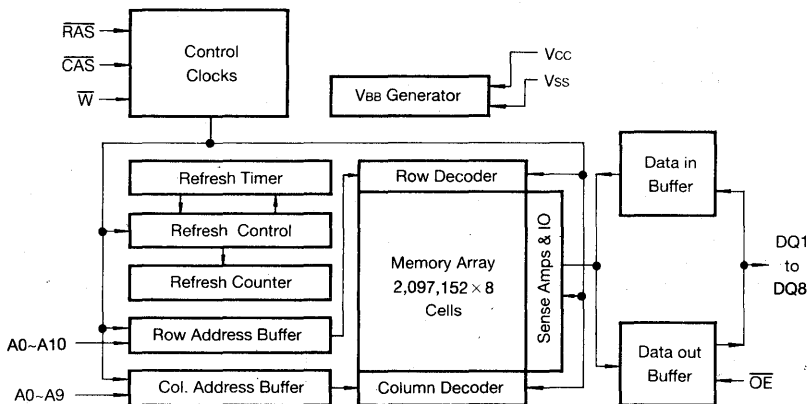
The Samsung KM48C2100A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

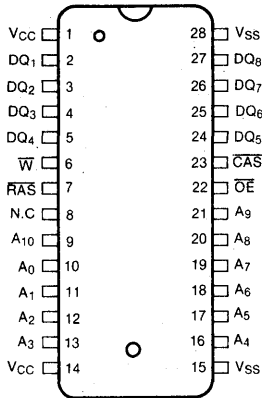
The KM48C2100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

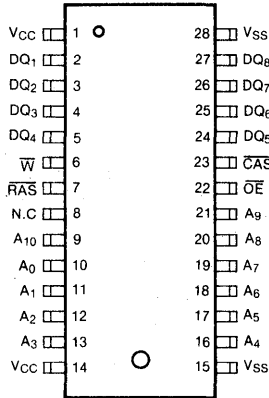


PIN CONFIGURATION (Top Views)

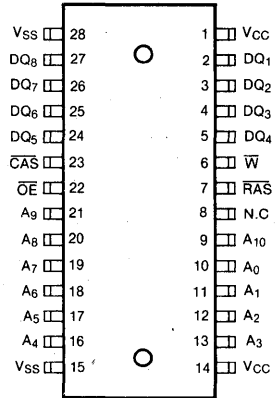
• KM48C2100 AJ/ALJ/ALLJ/ASLJ



• KM48C2100 AT/ALT/ALLT/ASLT



• KM48C2100 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0-A10	Address Inputs
DQ1~8	Data In/Out
Vss	Ground
\bar{RAS}	Row Address Strobe
\bar{CAS}	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
Vcc	Power(+5V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{os}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	Vcc + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM48C2100A/AL/ALL/ASL-5 KM48C2100A/AL/ALL/ASL-6 KM48C2100A/AL/ALL/ASL-7 KM48C2100A/AL/ALL/ASL-8	Icc1	110	mA
			100	mA
			90	mA
			80	mA
Standby Current (RAS=CAS=W=V _{IH})	KM48C2100A KM48C2100AL KM48C2100ALL KM48C2100ASL	Icc2	2	mA
			1	mA
			1	mA
			1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM48C2100A/AL/ALL/ASL-5 KM48C2100A/AL/ALL/ASL-6 KM48C2100A/AL/ALL/ASL-7 KM48C2100A/AL/ALL/ASL-8	Icc3	110	mA
			100	mA
			90	mA
			80	mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @trc=min.)	KM48C2100A/AL/ALL/ASL-5 KM48C2100A/AL/ALL/ASL-6 KM48C2100A/AL/ALL/ASL-7 KM48C2100A/AL/ALL/ASL-8	Icc4	90	mA
			80	mA
			70	mA
			60	mA
Standby Current (RAS=CAS=W=Vcc-0.2V)	KM48C2100A KM48C2100AL KM48C2100ALL KM48C2100ASL	Icc5	1	mA
			300	μA
			200	μA
			200	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM48C2100A/AL/ALL/ASL-5 KM48C2100A/AL/ALL/ASL-6 KM48C2100A/AL/ALL/ASL-7 KM48C2100A/AL/ALL/ASL-8	Icc6	110	mA
			100	mA
			90	mA
			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=Vcc-0.2V Input Low Voltage(V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DIN=Don't Care TRC=62.5μS(L-Ver.) 125μS(SL-Ver.), TRAS≤300ns	KM48C2100AL KM48C2100ASL	Icc7	400	μA
			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}=\overline{CAS}=0.2V$ $\overline{W}=\overline{OE}=A_0-A_{10}=V_{CC}-0.2V$ or $0.2V$ $DQ_1-DQ_8=V_{CC}-0.2V, 0.2V$ or Open	lccs	-	300	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 volts.)	li(L)	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	lo(L)	-10	10	μA
Output High Voltage Level ($I_{OH}=-5mA$)	VOH	2.4	-	V
Output Low Voltage Level ($I_{OL}=4.2mA$)	VOL	-	0.4	V

*NOTE: lcc1, lcc3, lcc4 and lcc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. lcc is specified as an average current. In lcc1 and lcc3, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. In lcc4, Address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A=25^\circ C, V_{CC}=5V, f=1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A_0-A_{10})	CIN1	-	5	pF
Input Capacitance ($\overline{RAS}, \overline{CAS}, \overline{W}, \overline{OE}$)	CIN2	-	7	pF
Input Capacitance (DQ_1-DQ_8)	CDQ	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_a \leq 70^\circ C, V_{CC}=5.0V \pm 10\%$, See notes 1,2)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from \overline{RAS}	trac		50		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	toff	0	13	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	trp	30		40		50		60		ns	
\overline{RAS} pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	trSH	13		15		20		20		ns	
\overline{CAS} hold time	tcSH	50		60		70		80		ns	
\overline{CAS} pulse width	tcAS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	trCD	20	37	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tcRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	



AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		0		ns	
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		30		35		40		45	ns	3
Fast Page mode cycle time	tPC	35		40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	76		85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	30		35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		13		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	13	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	13		15		20		20		ns	

6

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	
\bar{W} to \bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRP	10		10		10		10		ns	
\bar{W} to \bar{RAS} hold time (\bar{C} - \bar{B} - \bar{R} refresh)	tWRH	10		10		10		10		ns	
\bar{RAS} pulse width (\bar{C} - \bar{B} - \bar{R} self refresh)	tRASS	100		100		100		100		μ s	15
\bar{RAS} precharge time (\bar{C} - \bar{B} - \bar{R} self refresh)	tRPS	90		110		130		150		ns	15
\bar{CAS} hold time (\bar{C} - \bar{B} - \bar{R} self refresh)	tCHS	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note 12)

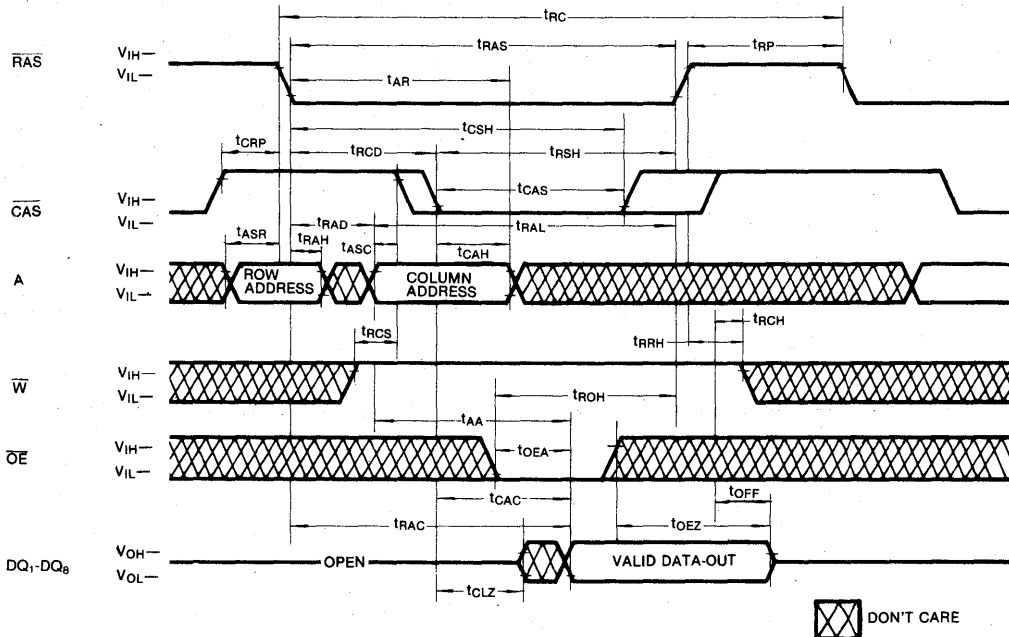
Parameter	Symbol	- 5		- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from \bar{RAS}	tRAC		55		65		75		85	ns	3,4,11
Access time from \bar{CAS}	tCAC		18		20		25		25	ns	3,4,5
Access time from column address	tAA		30		35		40		45	ns	3,11
\bar{RAS} pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	tCAS	18	10,000	20	10,000	25	10,000	25	10,000	ns	
\bar{RAS} hold time	tRSH	18		20		25		25		ns	
\bar{CAS} hold time	tCSH	55		65		75		85		ns	
Column address to \bar{RAS} lead time	tRAL	30		35		40		45		ns	
\bar{CAS} to \bar{W} delay time	tCWD	41		45		55		55		ns	8
\bar{RAS} to \bar{W} delay time	tRWD	78		90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	53		60		70		75		ns	8
Fast Page mode cycle time	tPC	40		45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	81		90		105		110		ns	
\bar{RAS} pulse width (Fast Page Mode)	tRASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	tCPA		35		40		45		50	ns	3
\bar{OE} access time	tOEA		18		20		25		25	ns	
\bar{OE} to data delay	tOED	18		20		25		25		ns	
\bar{OE} command hold time	tOEH	18		20		25		25		ns	

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF
4. Operation within the $t_{RC}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RC}(\max)$ is specified as a reference point only. If t_{RC} is greater than the specified $t_{RC}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RC} \geq t_{RC}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

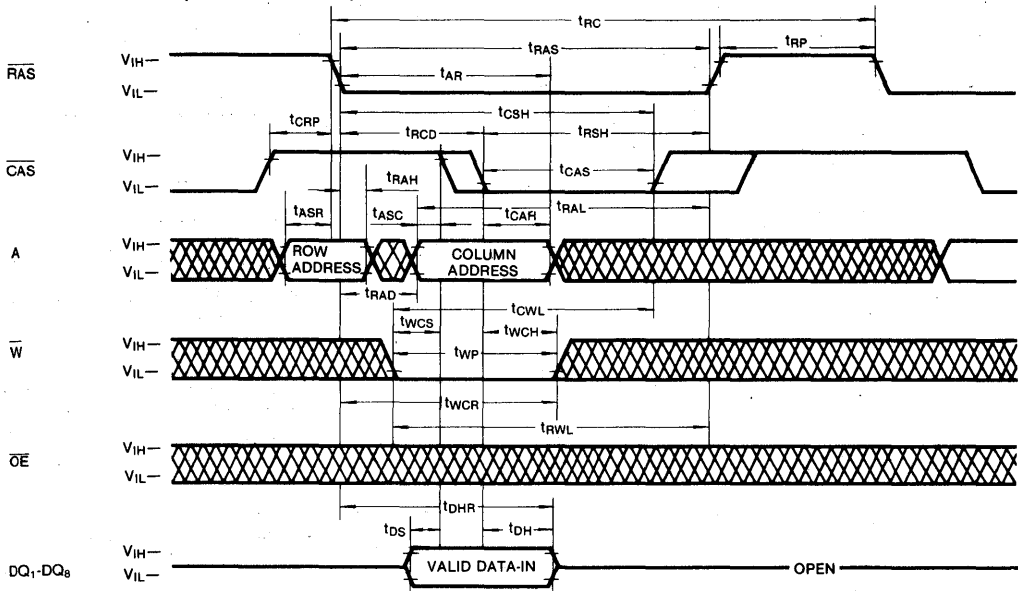
TIMING DIAGRAMS

READ CYCLE

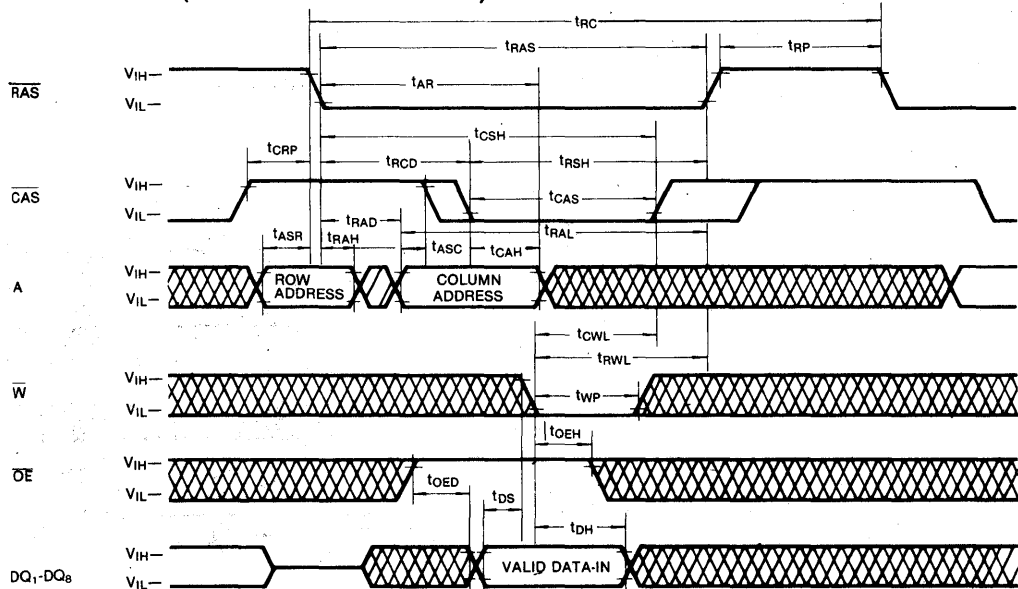


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



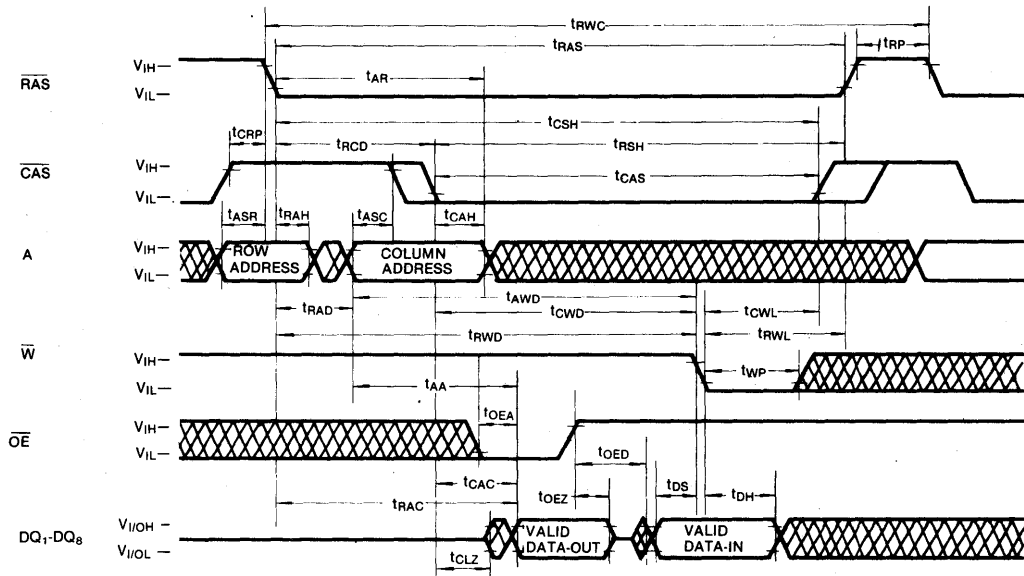
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)



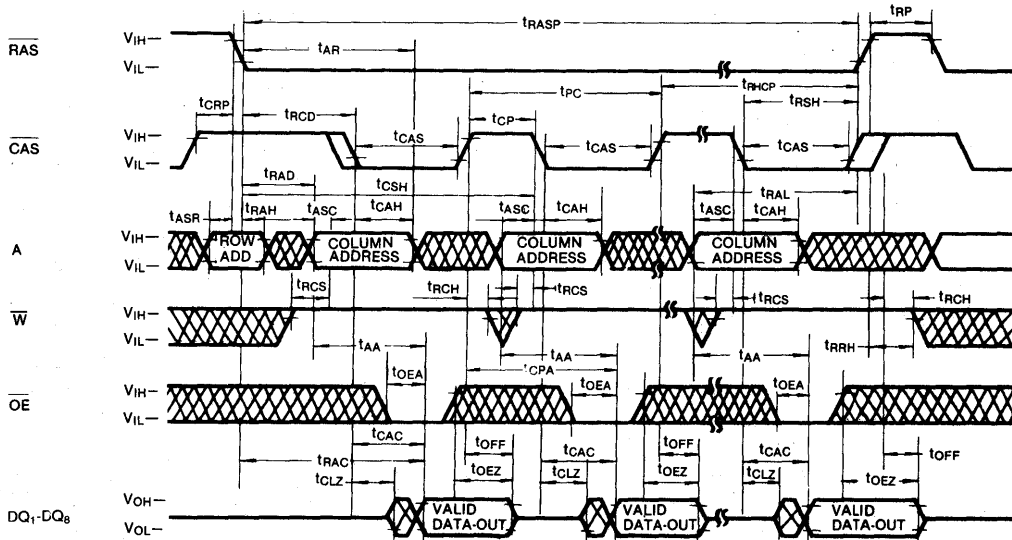
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



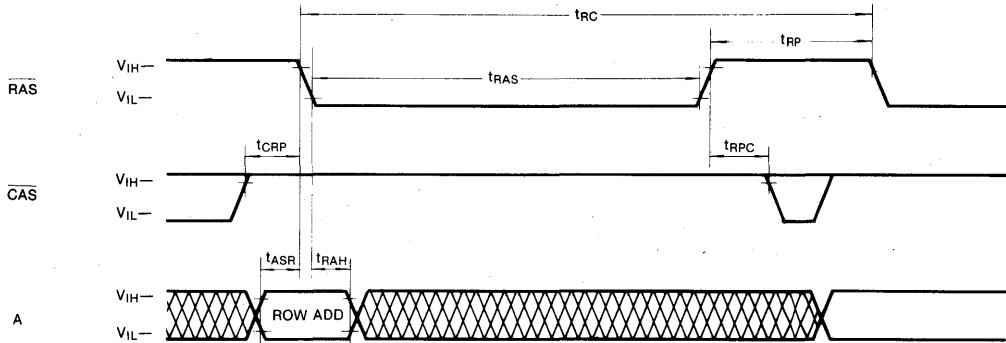
DON'T CARE

6

TIMING DIAGRAMS (Continued)

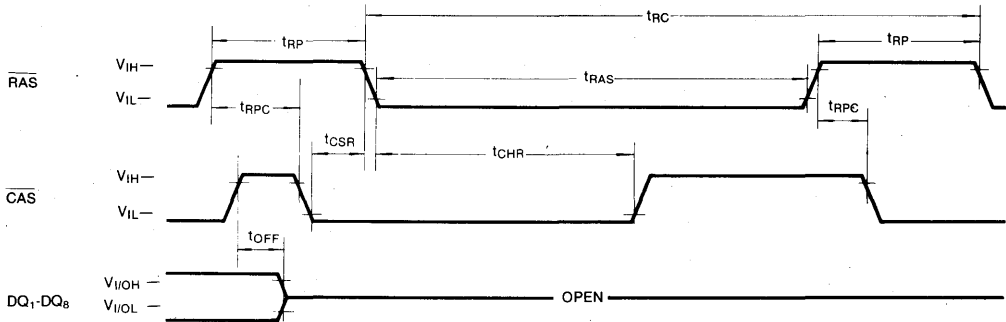
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} = Don't care



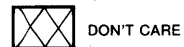
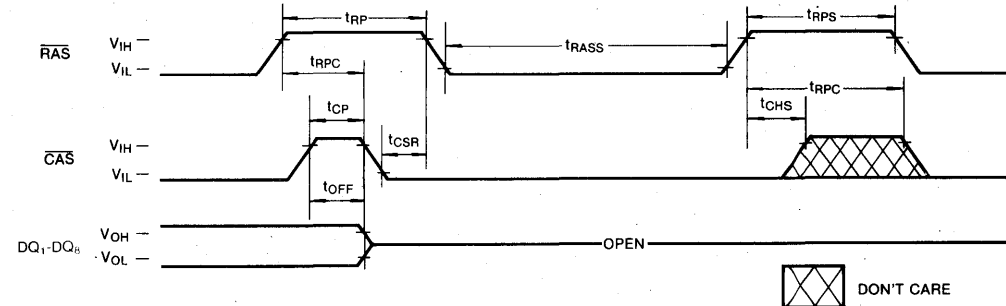
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\bar{W}=V_{IH}$, \bar{OE} , A=Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

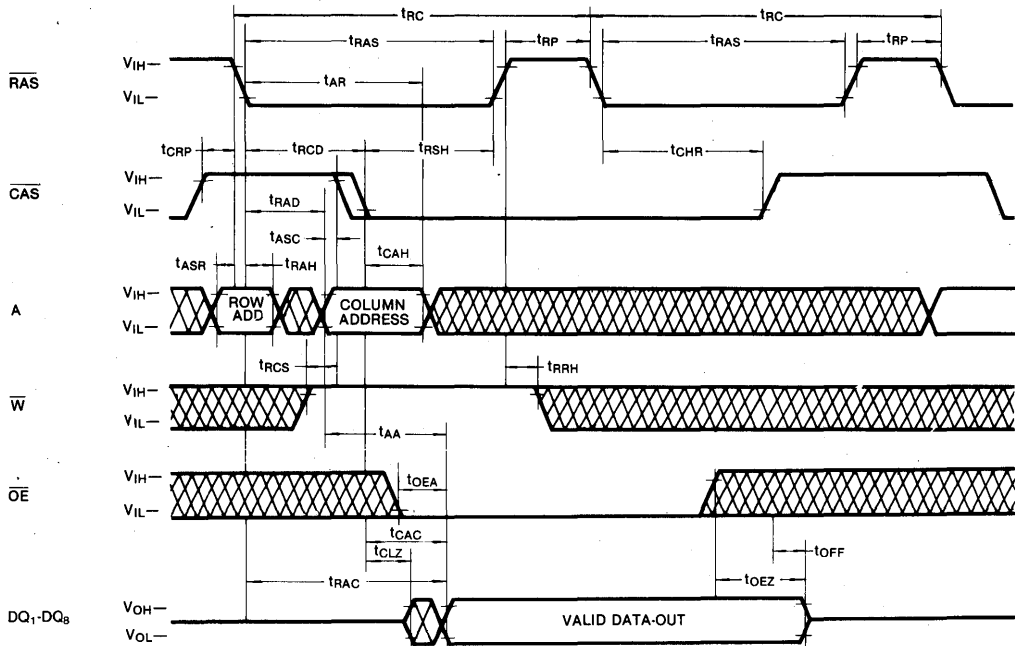
NOTE: \bar{W} , \bar{OE} , A=Don't Care



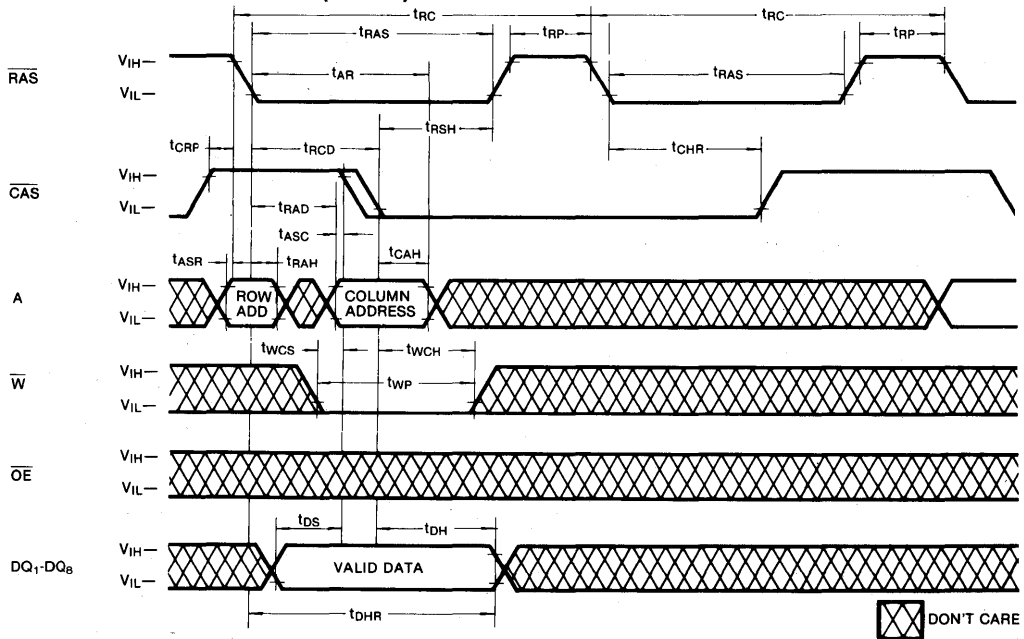
6

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



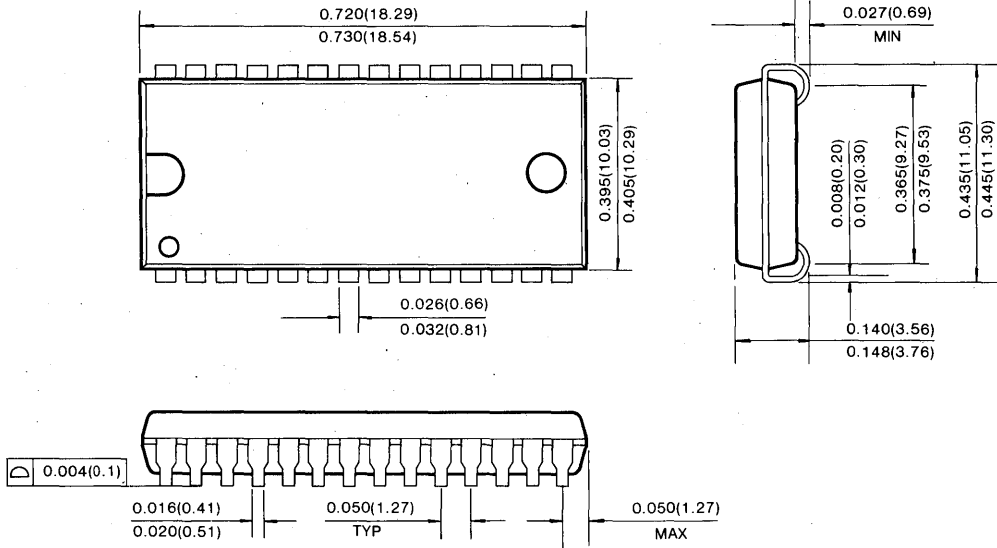
HIDDEN REFRESH CYCLE (WRITE)



PACKAGE DIMENSION

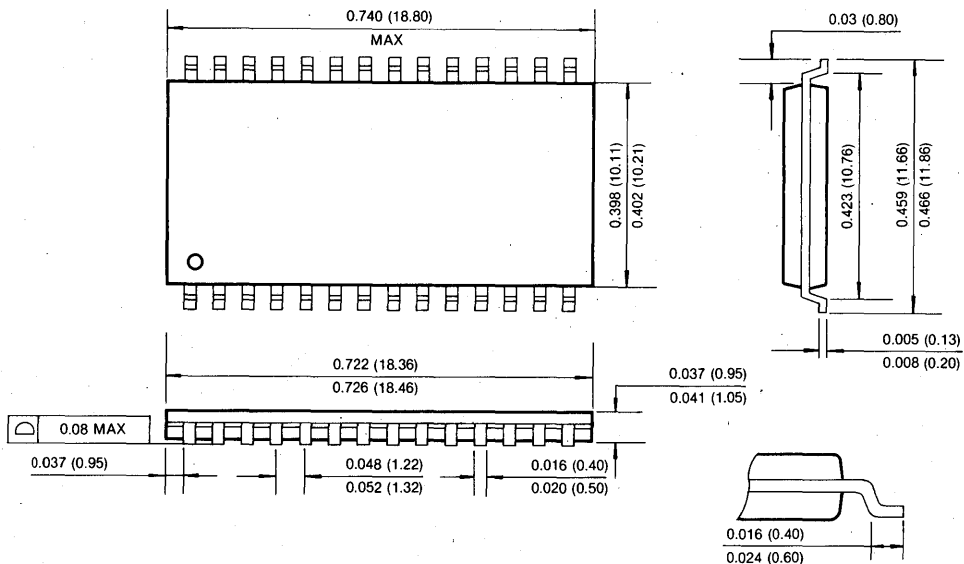
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M × 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
KM48C2004A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM48C2004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48C2004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48C2004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh Operation (LL-ver. only)
- Byte Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single +5.0V ± 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

GENERAL DESCRIPTION

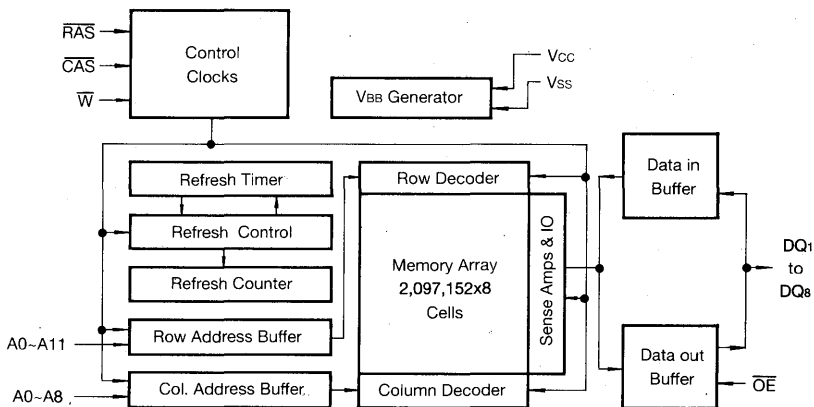
The Samsung KM48C2004A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

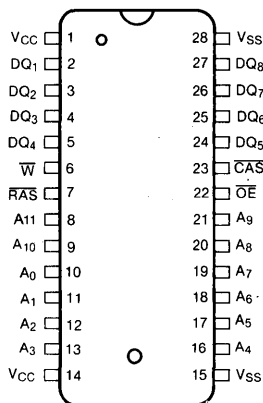
The KM48C2004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



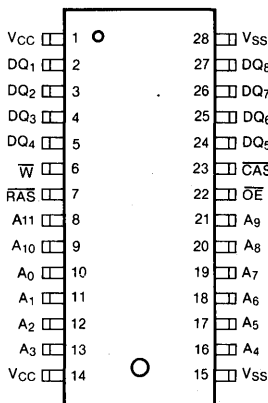
PIN CONFIGURATION (Top Views)

• KM48C2004 AJ/ALJ/ALLJ/ASLJ



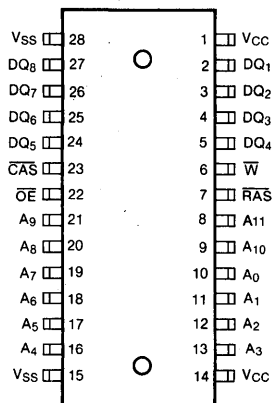
J : 400MIL

• KM48C2004 AT/ALT/ALLT/ASLT



T : 400MIL (Forward)

• KM48C2004 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL (Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-8	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5.0V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on Vcc Supply Relative to Vss	Vcc	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	Vcc + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM48C2004A/AL/ALL/ASL-5 KM48C2004A/AL/ALL/ASL-6 KM48C2004A/AL/ALL/ASL-7 KM48C2004A/AL/ALL/ASL-8 I _{CC1}	-	90 80 70 60	mA mA mA mA
Standby Current (RAS=CAS=W=V _{IH})	KM48C2004A KM48C2004AL KM48C2004ALL KM48C2004ASL I _{CC2}	-	2 1 1 1	mA mA mA mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM48C2004A/AL/ALL/ASL-5 KM48C2004A/AL/ALL/ASL-6 KM48C2004A/AL/ALL/ASL-7 KM48C2004A/AL/ALL/ASL-8 I _{CC3}	-	90 80 70 60	mA mA mA mA
Hyper Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM48C2004A/AL/ALL/ASL-5 KM48C2004A/AL/ALL/ASL-6 KM48C2004A/AL/ALL/ASL-7 KM48C2004A/AL/ALL/ASL-8 I _{CC4}	-	100 90 80 70	mA mA mA mA
Standby Current (RAS=CAS=W=Vcc-0.2V)	KM48C2004A KM48C2004AL KM48C2004ALL KM48C2004ASL I _{CC5}	-	1 300 200 200	mA μA μA μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM48C2004A/AL/ALL/ASL-5 KM48C2004A/AL/ALL/ASL-6 KM48C2004A/AL/ALL/ASL-7 KM48C2004A/AL/ALL/ASL-8 I _{CC6}	-	90 80 70 60	mA mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=Vcc-0.2V Input Low Voltage(V _{IL})=0.2V, CAS=CAS-Before-RAS Cycling or 0.2V, DQ1-DQ8=Don't Care, trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), tRAS=tRASmin~300ns	KM48C2004AL KM48C2004ASL I _{CC7}	-	450 350	μA μA

6

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ8=Vcc-0.2V, 0.2V or Open	ICC3	-	300	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 volts.)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ Vcc)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, Address can be changed maximum two times while RAS=VIL. In ICC4, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A11)	CIN1	-	5	pF
Input Capacitance (RAS, CAS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1~DQ8)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, Vcc=5.0V ± 0.5V, See notes 1,2)

Test condition: Vin/Vii=2.0V/0.8V, Voh/Voi=2.0V/0.8V, Output Loading CL=100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CAS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	3		3		3		3		ns	3
OE to output in Low-Z	tOLZ	3		3		3		3		ns	3
Output buffer turn-off delay from CAS	tCEZ	3	13	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	tr	2	50	2	50	2	50	2	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10K	60	10K	70	10K	80	10K	ns	
RAS hold time	trSH	13		15		20		20		ns	
CAS hold time	tCSH	38		45		50		60		ns	
CAS pulse width	tcAS	8	10K	10	10K	15	10K	20	10K	ns	16
RAS to CAS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to RAS	tAR	40		50		55		60		ns	6
Column address to RAS lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to RAS	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to RAS lead time	tRWL	13		15		20		20		ns	
Write command to CAS lead time	tCWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to RAS	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
CAS to W delay time	tCWD	36		40		50		50		ns	8
RAS to W delay time	tRWD	73		85		100		110		ns	8
Column address to W delay time	tAWD	48		55		65		70		ns	8
CAS address to W delay time	tCPWD	53		60		70		75		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		20		30		30		ns	
Access time from CAS precharge	tCPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
CAS precharge time (Hyper Page Cycle)	tCP	8		10		10		10		ns	
RAS pulse width(Hyper Page Cycle)	tRASPP	50	200K	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	

6

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
\overline{OE} to data delay	toED	13		15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	toEZ	3	13	3	15	3	20	3	20	ns	7,14
\overline{OE} command hold time	toEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	twTH	10		10		10		10		ns	12
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	twRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	twRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	treZ	3	13	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay from \overline{W}	tweZ	3	13	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	twED	15		15		20		20		ns	
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		5		ns	
\overline{RAS} pulse width (LL-ver)	trASS	100		100		100		100		μ s	16
\overline{RAS} precharge time (LL-ver)	trPS	90		110		130		150		ns	16
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	95		115		135		155		ns	
Read-modify-write cycle time	trWC	138		160		190		210		ns	
Access time from \overline{RAS}	trAC		55		65		75		85	ns	3,4,11,13
Access time from \overline{CAS}	tcAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
\overline{RAS} pulse width	trAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	tcAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	18		20		25		25		ns	
\overline{CAS} hold time	tcSH	43		50		55		65		ns	
Column address to \overline{RAS} lead time	trAL	30		35		40		45		ns	
\overline{CAS} to \overline{W} delay time	tcWD	41		45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	78		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	thPC	25		29		34		39		ns	17
Hyper Page read-modify-write cycle time	thPRWC	67		76		91		101		ns	17

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
RAS pulse width (Hyper Page Cycle)	trASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM48C2004A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx8 DRAM.

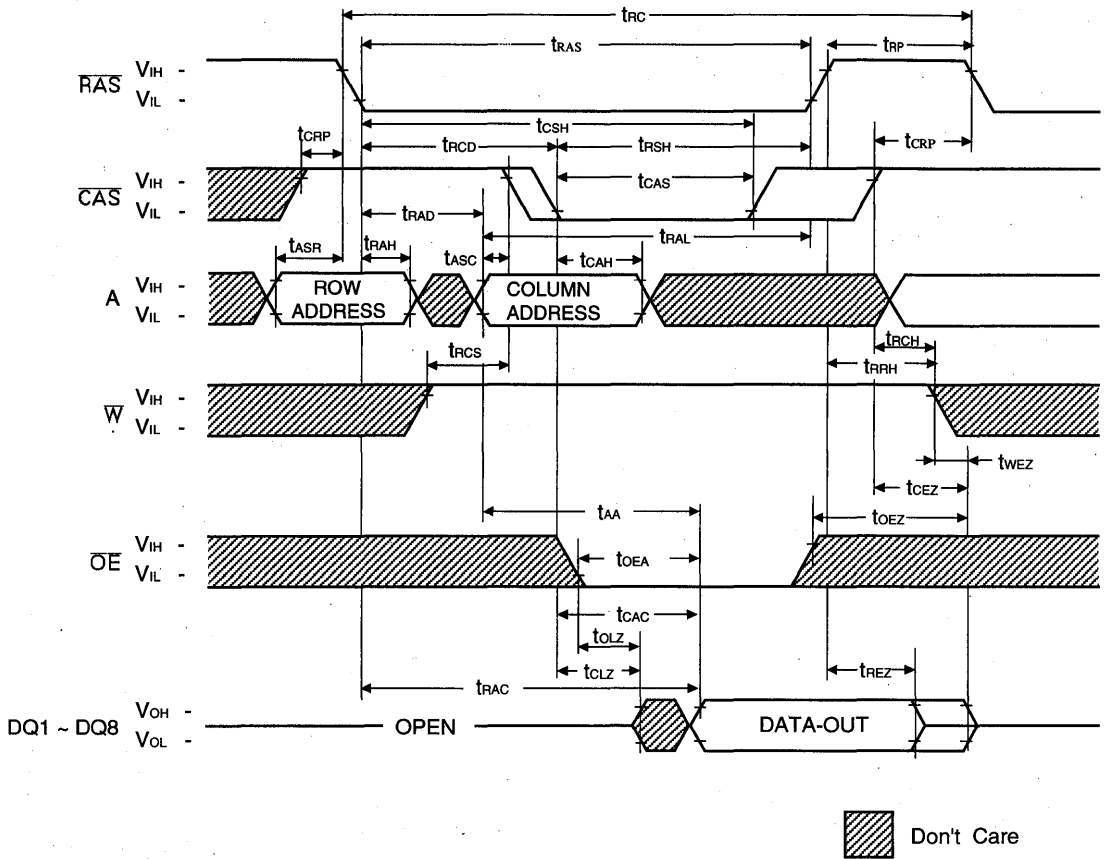
$\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh Cycle" or " $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "test Mode" function reduces test time (1/2 in cases of N test pattern).

NOTES

- An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, except tHPC and tHPRWC.
- Measured with a load equivalent to 2 TTL loads and 100pF
- Operation within the t_{RC}D(max) limit insures that t_{TR}AC(max) can be met. t_{RC}D(max) is specified as a reference point only. If t_{RC}D is greater than the specified t_{RC}D(max) limit, then access time is controlled exclusively by t_{CO}AC.
- Assumes that t_{RC}D \geq t_{RC}D (max).
- t_{AR}, t_WCR, t_DHR are referenced to t_{TR}AD(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- twcs, trwd, tcwd and tawd are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If twcs \geq twcs(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcwd \geq tcwd(min), trwd \geq trwd(min) and tawd \geq tawd(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either t_{TR}CH or t_{TR}RH must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
- Operation within the t_{TR}AD(max) limit insures that t_{TR}AC(max) can be met. t_{TR}AD(max) is specified as a reference point only. If t_{TR}AD is greater than the specified t_{TR}AD(max) limit, then access time is controlled by t_{AA}.
- These specifications are applied in the test mode.
- In test mode read cycle, the value of t_{TR}AC, t_{AA}, t_{CO}AC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
- t_{CE}Z(max), t_{OE}Z(max), t_{RE}Z(max) and t_{WE}Z(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
- If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going
- t_{ASC} \geq t_{CP}(min), Assumn t_r = 2.0ns

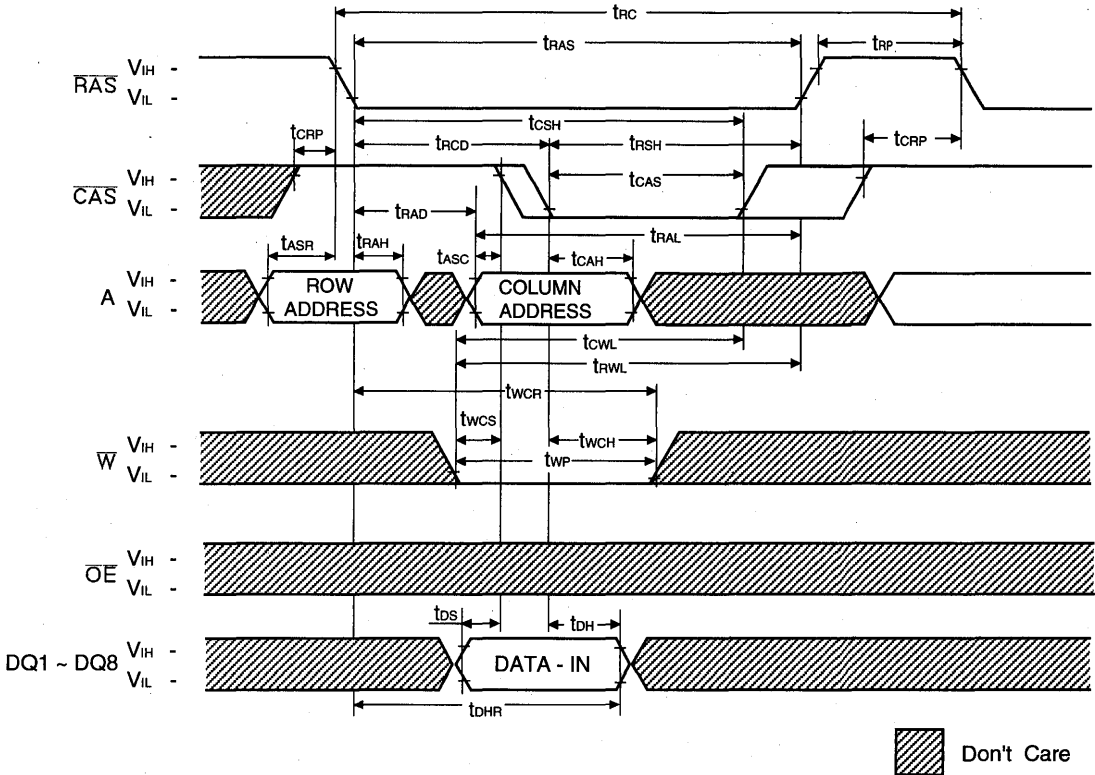
TIMING DIAGRAM

READ CYCLE



WRITE CYCLE (EARLY WRITE)

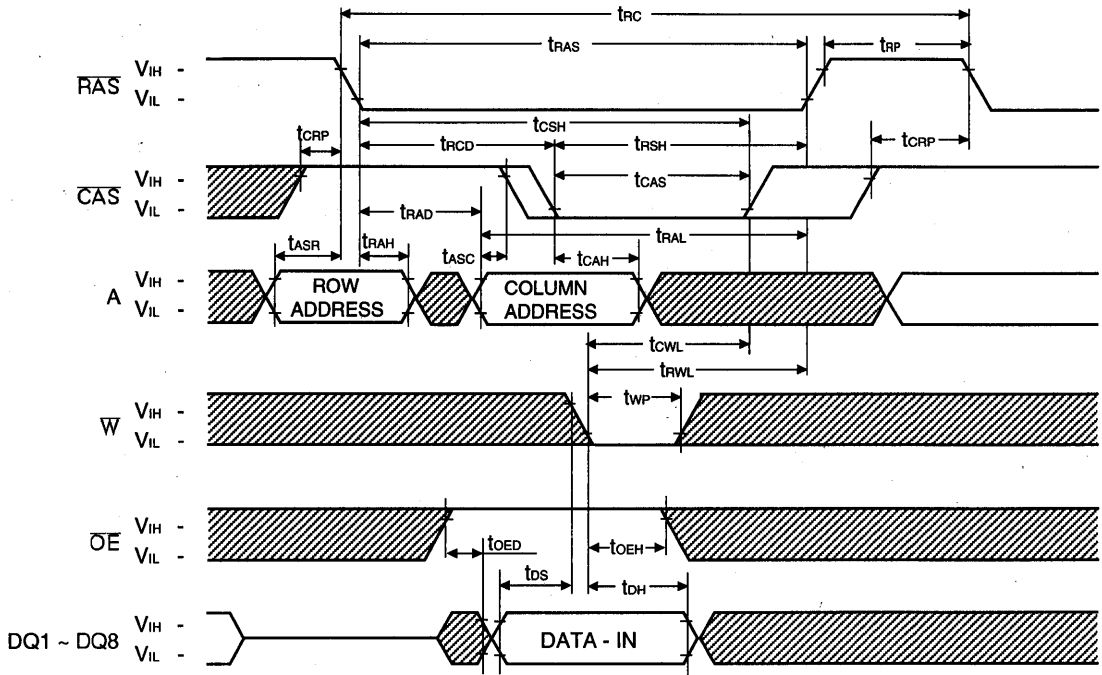
NOTE : D_{OUT} = OPEN



6

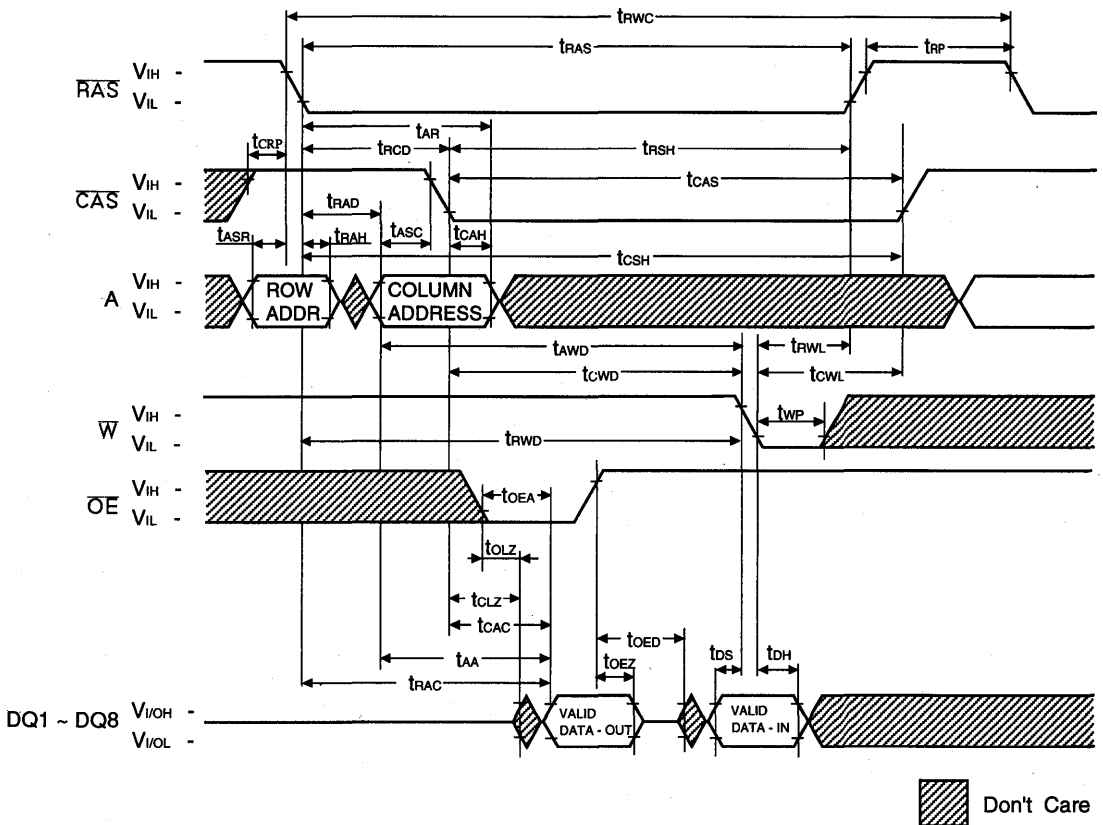
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



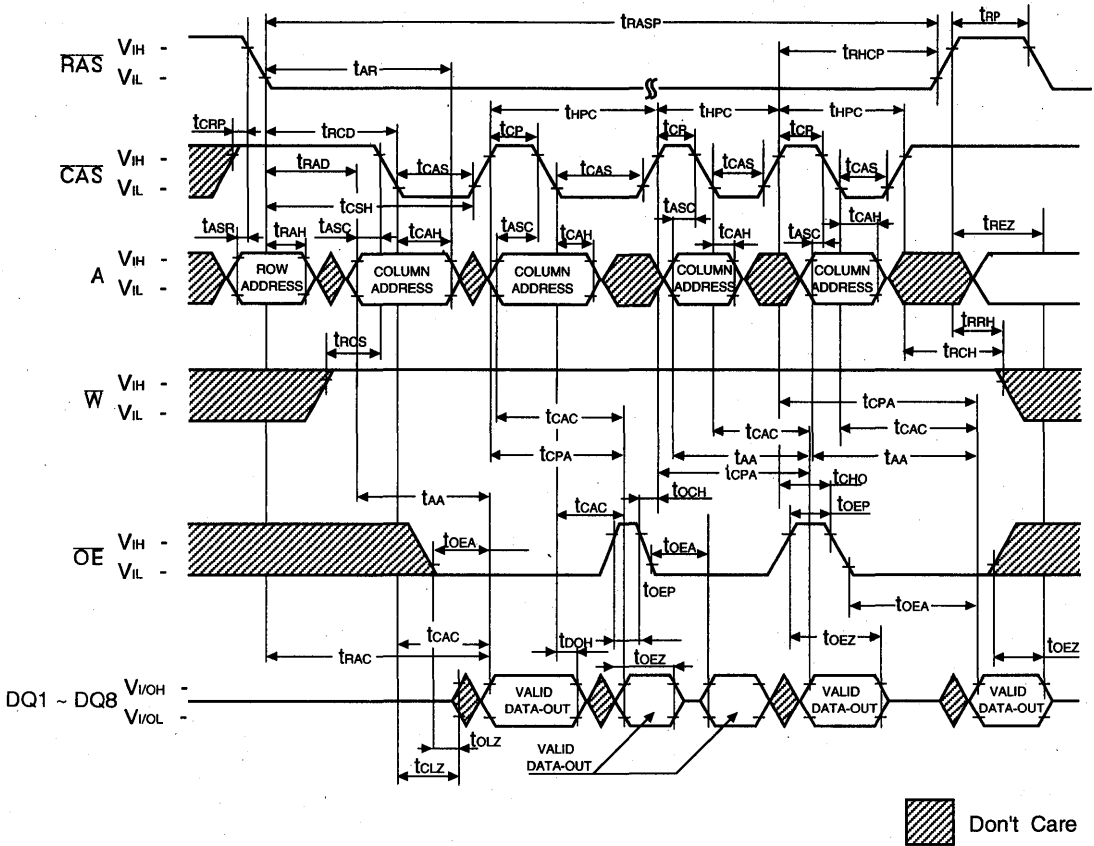
 Don't Care

READ - MODIFY - WRITE CYCLE



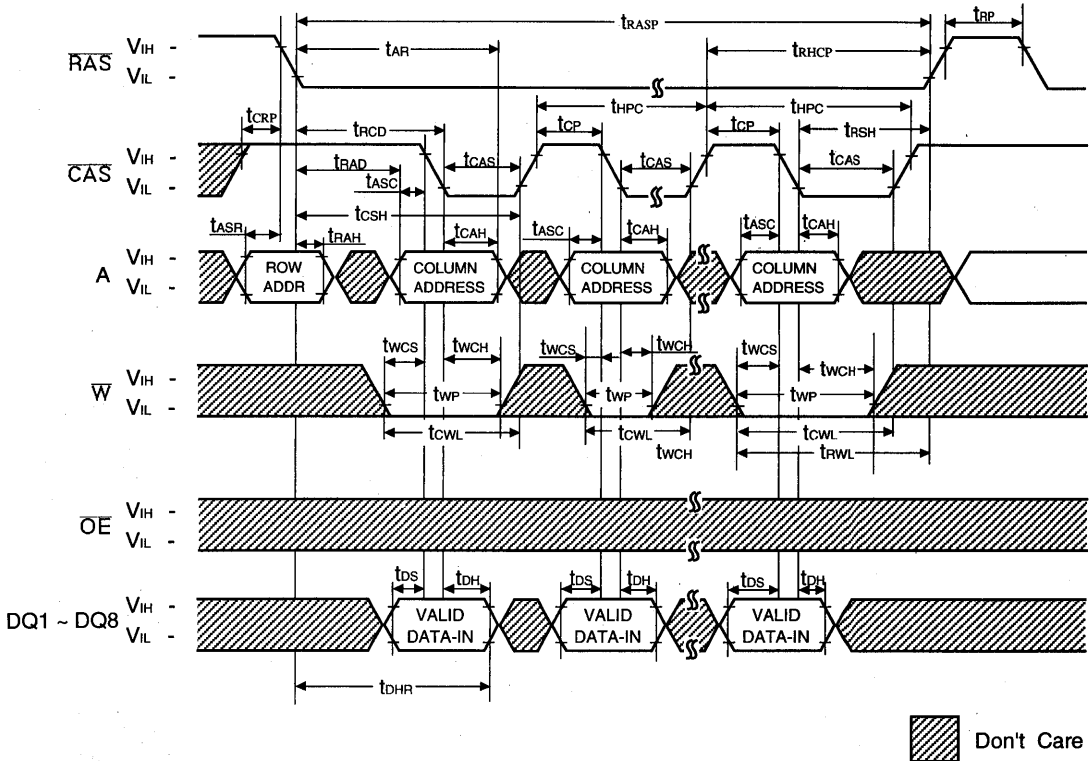
6

HYPER PAGE READ CYCLE



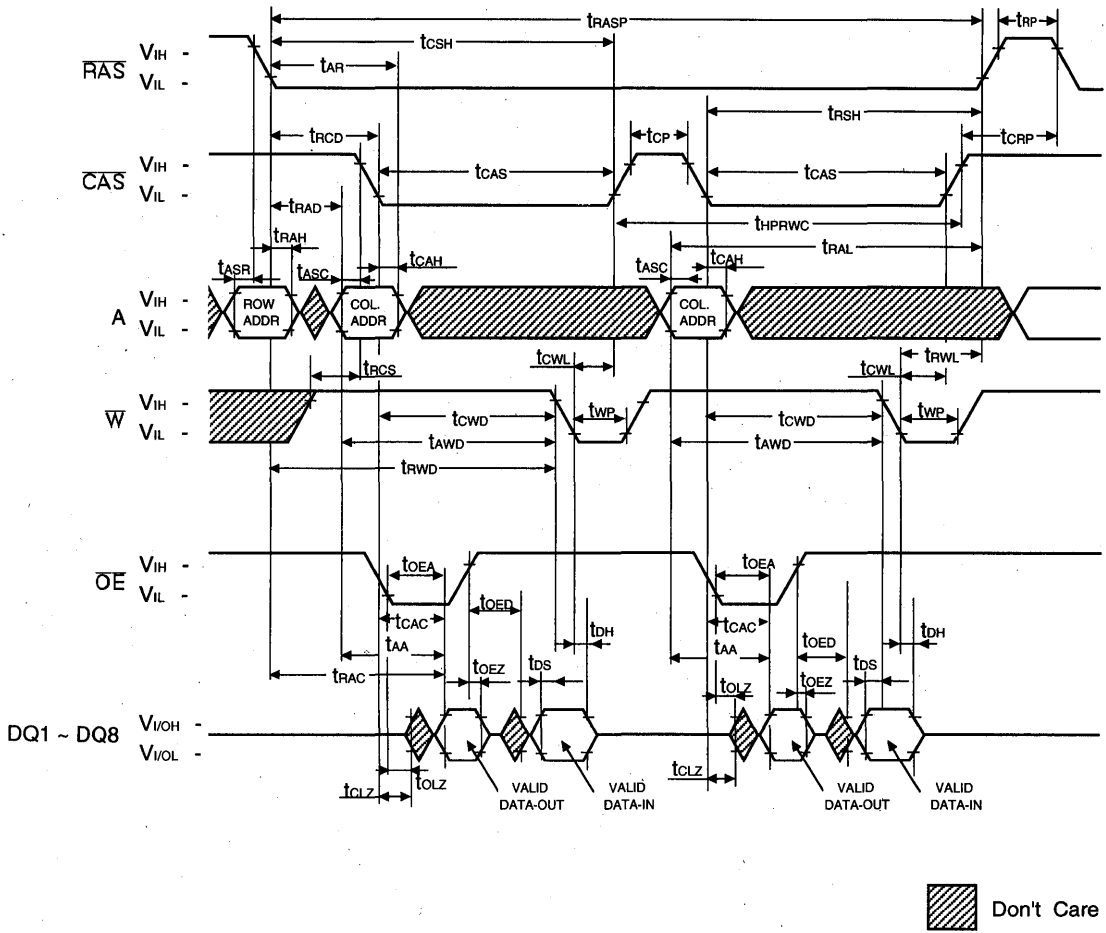
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open

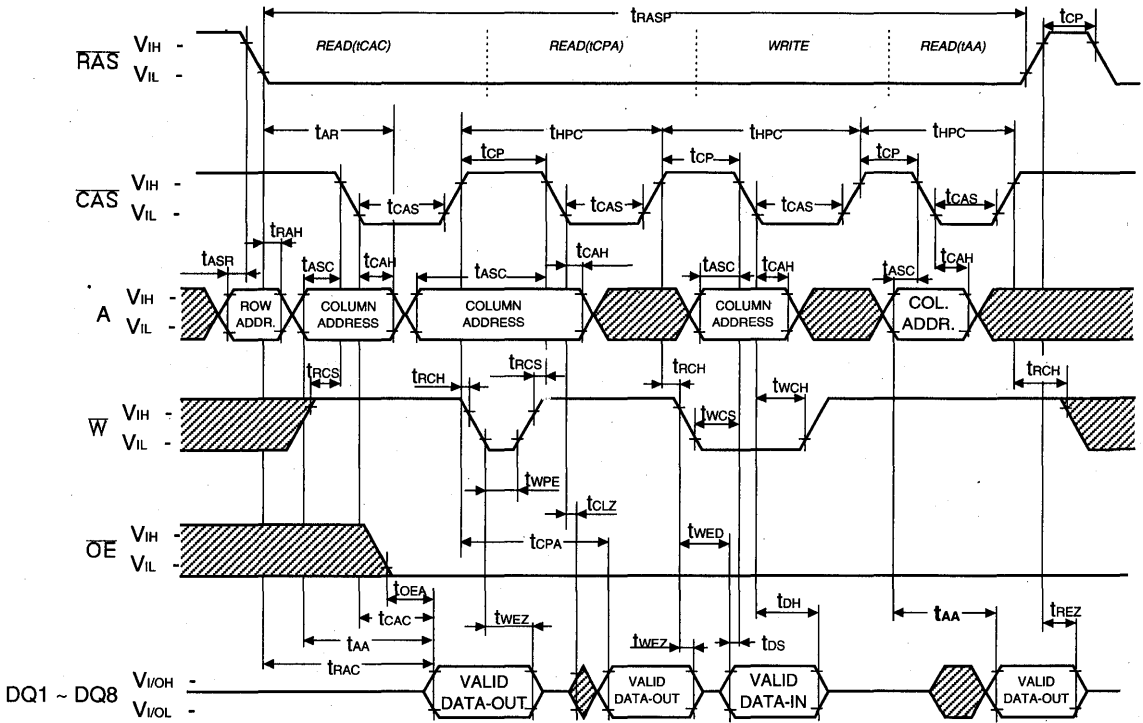


6

HYPER PAGE READ-MODIFY-WRITE CYCLE



HYPER PAGE READ AND WRITE MIXED CYCLE

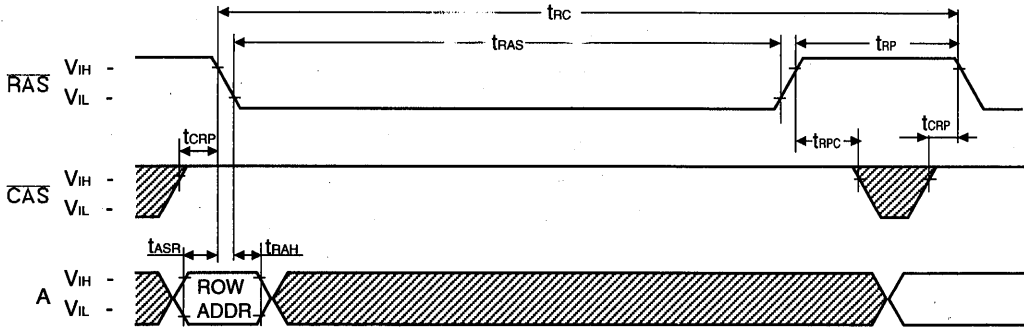


Don't Care

6

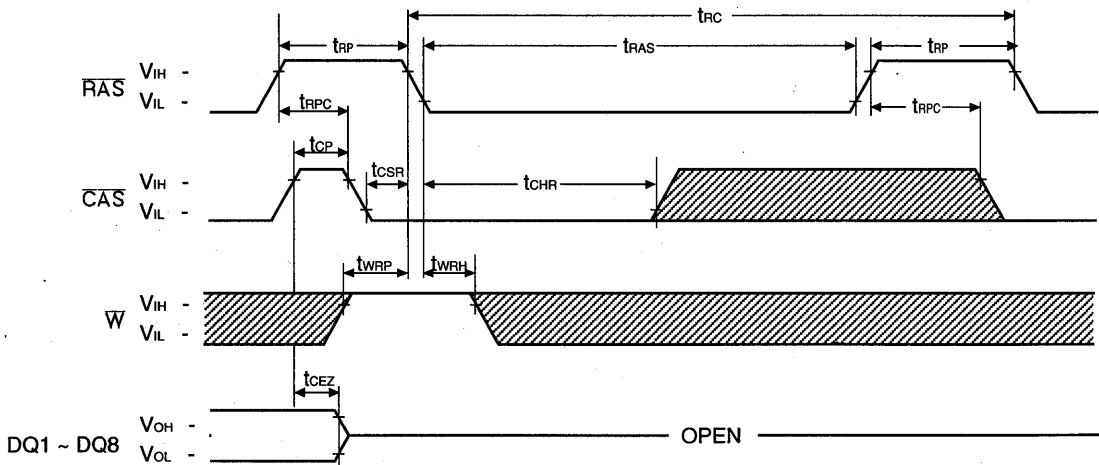
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



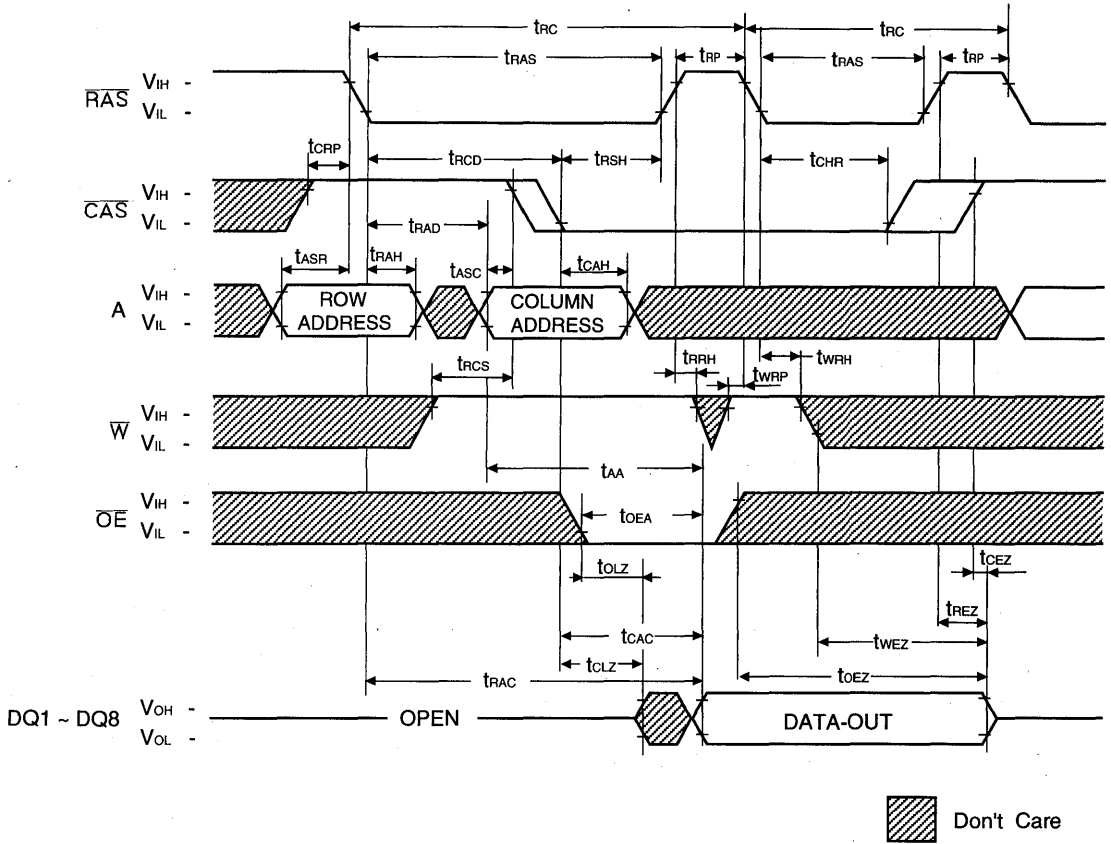
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care



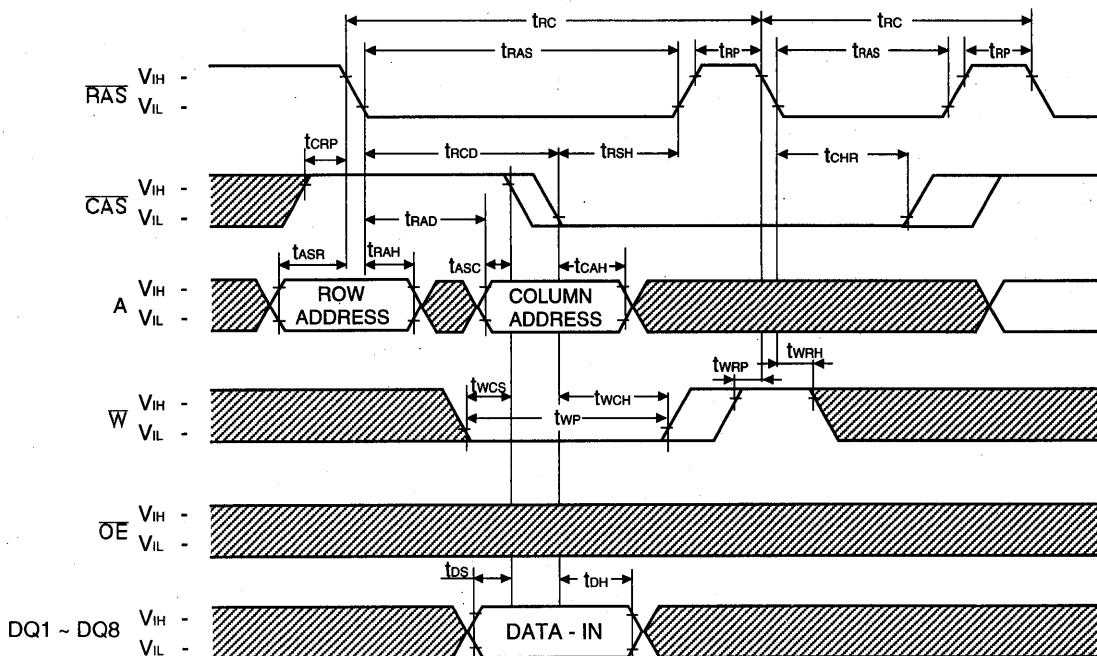
 Don't Care

HIDDEN REFRESH CYCLE (READ)



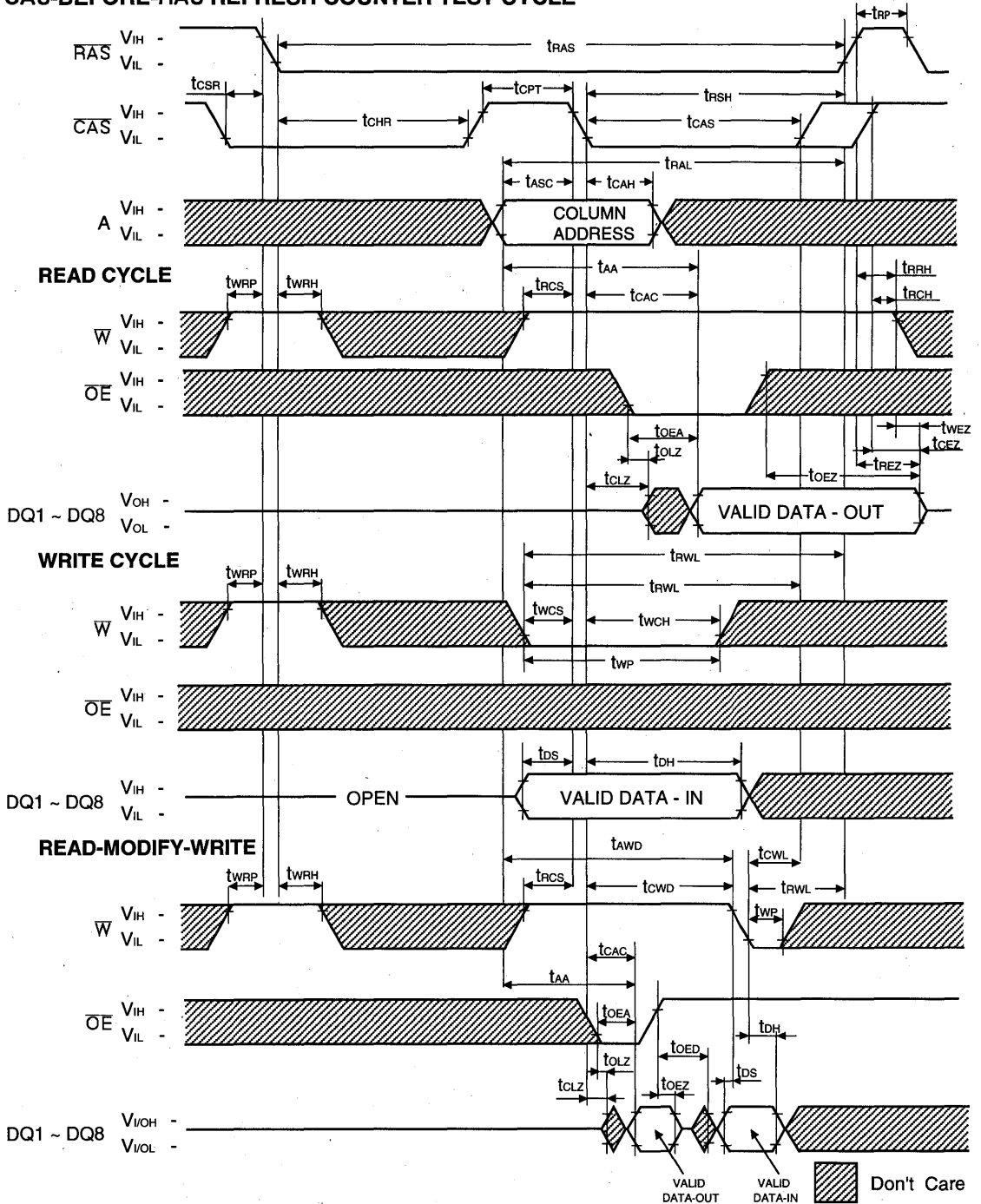
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



 Don't Care

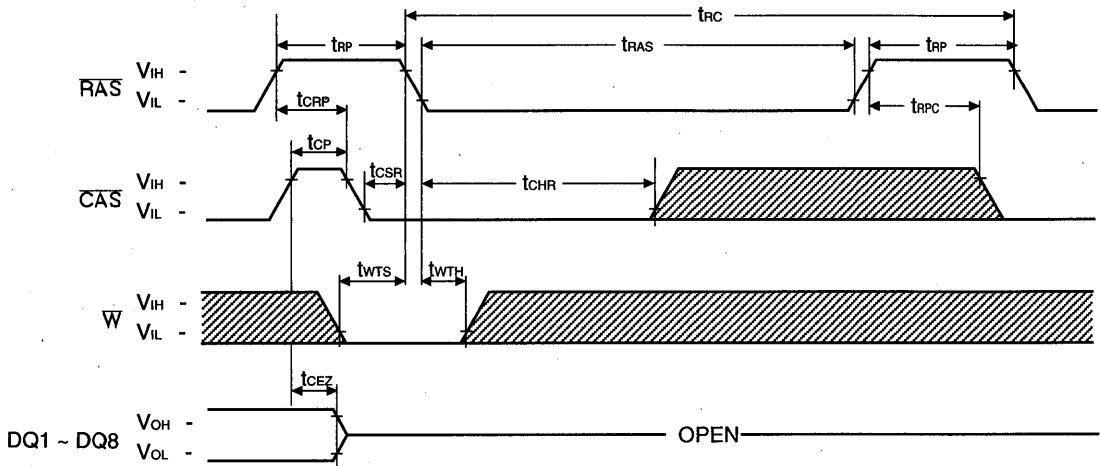
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE




6

TEST MODE IN CYCLE

NOTE : $\bar{O}E$, A = Don't Care

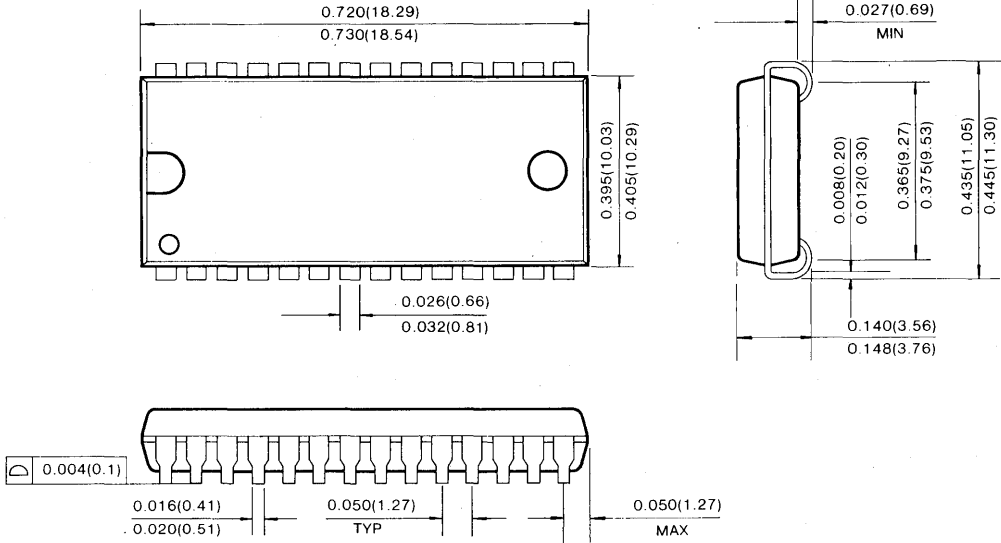


 Don't Care

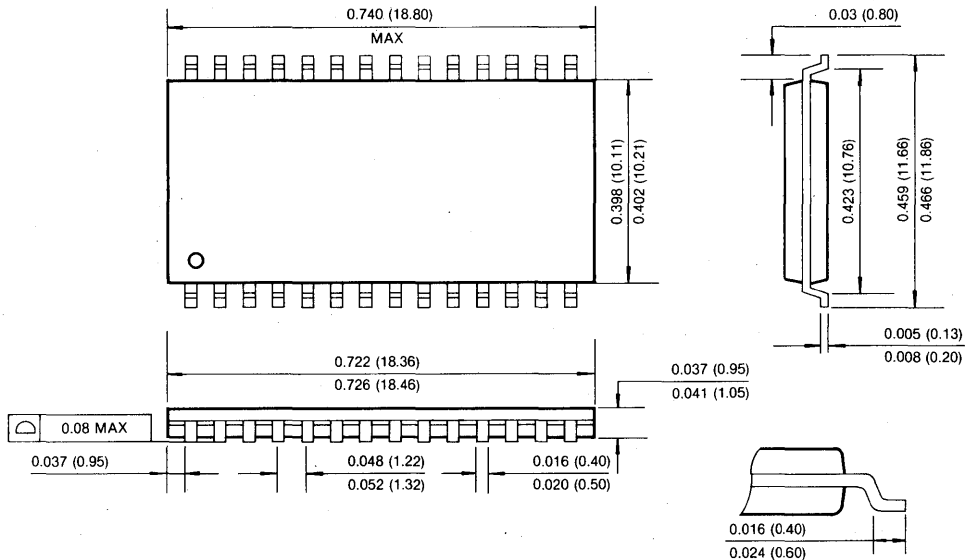
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



2M × 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trC	tHPC
KM48C2104A/AL/ALL/ASL-5	50ns	13ns	90ns	20ns
KM48C2104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48C2104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48C2104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh Operation (LL-ver. only)
- Byte Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single +5.0V ± 10% power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

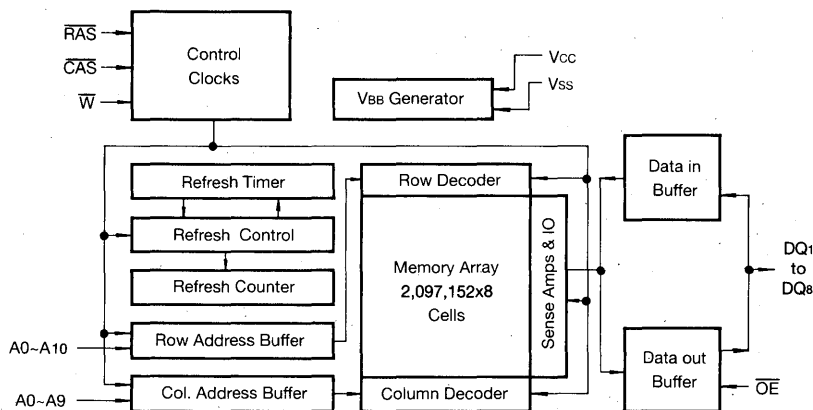
The Samsung KM48C2104A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48C2104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

The KM48C2104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

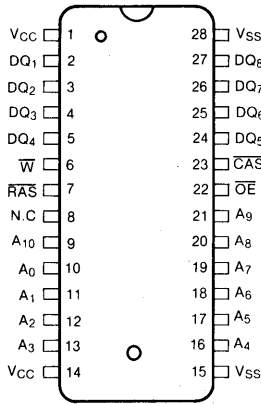


PIN CONFIGURATION (Top Views)

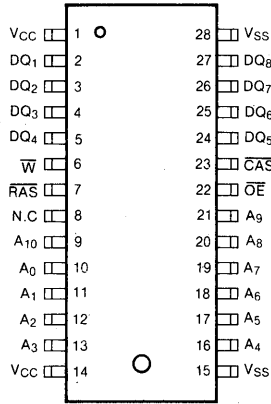
• KM48C2104 AJ/ALJ/ALLJ/ASLJ

• KM48C2104 AT/ALT/ALLT/ASLT

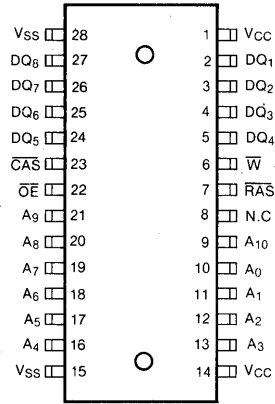
• KM48C2104 ATR/ALTR/ALLTR/ASLTR



J : 400MIL



T : 400MIL(Forward)



TR : 400MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-8	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
OE	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM48C2104A/AL/ALL/ASL-5	I _{CC1}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Standby Current (RAS=CAS=W=V _{IH})	KM48C2104A	I _{CC2}	-	2	mA
	KM48C2104AL			1	mA
	KM48C2104ALL			1	mA
	KM48C2104ASL			1	mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM48C2104A/AL/ALL/ASL-5	I _{CC3}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Hyper Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM48C2104A/AL/ALL/ASL-5	I _{CC4}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Standby Current (RAS=CAS=W=V _{CC} -0.2V)	KM48C2104A	I _{CC5}	-	1	mA
	KM48C2104AL			300	μA
	KM48C2104ALL			200	μA
	KM48C2104ASL			200	μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM48C2104A/AL/ALL/ASL-5	I _{CC6}	-	110	mA
	KM48C2104A/AL/ALL/ASL-6			100	mA
	KM48C2104A/AL/ALL/ASL-7			90	mA
	KM48C2104A/AL/ALL/ASL-8			80	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V Input Low Voltage(V _{IL})=0.2V, CAS=CAS-Before-RAS Cycling or 0.2V, DQ1-DQ8=Don't Care trc=62.5μs(L-Ver.) 125μs(SL-Ver.), tRAS=tRAS min~300ns	KM48C2104AL	I _{CC7}	-	400	μA
	KM48C2104ASL			300	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current R \overline{AS} =C \overline{AS} =0.2V W= \overline{OE} =A $_0$ -A $_{10}$ =V $_{CC}$ -0.2V or 0.2V DQ $_1$ -DQ $_8$ =V $_{CC}$ -0.2V, 0.2V or Open	l $_{CCS}$	-	300	μ A
Input Leakage Current (Any input 0 \leq V $_{in}$ \leq V $_{CC}$ +0.5V, all other pins not under test=0 volts.)	I $_{i(L)}$	-10	10	μ A
Output Leakage Current (Data out is disabled, 0V \leq V $_{OUT}$ \leq V $_{CC}$)	I $_{o(L)}$	-10	10	μ A
Output High Voltage Level (I $_{OH}$ =-5mA)	V $_{OH}$	2.4	-	V
Output Low Voltage Level (I $_{OL}$ =4.2mA)	V $_{OL}$	-	0.4	V

*NOTE: I $_{CC1}$, I $_{CC3}$, I $_{CC4}$ and I $_{CC6}$ are dependent on output loading and cycle rates. Specified values are obtained with the output open. I $_{CC}$ is specified as an average current. In I $_{CC1}$ and I $_{CC3}$, Address can be changed maximum two times while R \overline{AS} =V $_{IL}$. In I $_{CC4}$, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T $_A$ =25°C, V $_{CC}$ =5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A $_0$ -A $_{10}$)	C $_{IN1}$	-	5	pF
Input Capacitance (R \overline{AS} , C \overline{AS} , W, \overline{OE})	C $_{IN2}$	-	7	pF
Input Capacitance (DQ $_1$ -DQ $_8$)	C $_{DQ}$	-	7	pF

AC CHARACTERISTICS (0°C \leq T $_A$ \leq 70°C, V $_{CC}$ =5.0V \pm 0.5V, See notes 1,2)

Test condition: V $_{ih}$ /V $_{il}$ =2.4V/0.8V, V $_{oh}$ /V $_{ol}$ =2.0V/0.8V, Output Loading C $_L$ =100pF

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t $_{RC}$	90		110		130		150		ns	
Read-modify-write cycle time	t $_{RWC}$	133		155		185		205		ns	
Access time from R \overline{AS}	t $_{RAC}$		50		60		70		80	ns	3,4,11
Access time from C \overline{AS}	t $_{CAC}$		13		15		20		20	ns	3,4,5
Access time from column address	t $_{AA}$		25		30		35		40	ns	3,11
C \overline{AS} to output in Low-Z	t $_{CLZ}$	3		3		3		3		ns	3
\overline{OE} to output in Low-Z	t $_{OLZ}$	3		3		3		3		ns	3
Output buffer turn-off delay	t $_{CEZ}$	3	13	3	15	3	20	3	20	ns	7,14,15
Transition time (rise and fall)	t $_T$	2	50	2	50	2	50	2	50	ns	2
R \overline{AS} precharge time	t $_{RP}$	30		40		50		60		ns	
R \overline{AS} pulse width	t $_{RAS}$	50	10K	60	10K	70	10K	80	10K	ns	
R \overline{AS} hold time	t $_{RSH}$	13		15		20		20		ns	
C \overline{AS} hold time	t $_{CSH}$	38		45		50		60		ns	
C \overline{AS} pulse width	t $_{CAS}$	8	10K	10	10K	15	10K	20	10K	ns	16
R \overline{AS} to C \overline{AS} delay time	t $_{RCD}$	20	37	20	45	20	50	20	60	ns	4
R \overline{AS} to column address delay time	t $_{RAD}$	15	25	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
CAS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	
Row address hold time	tRAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	8		10		15		15		ns	
Column address hold time referenced to RAS	tAR	40		50		55		60		ns	6
Column address to RAS lead time	tRAL	25		30		35		40		ns	
Read command set-up time	tRCS	0		0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		0		ns	9
Write command hold time	tWCH	10		10		15		15		ns	
Write command hold time referenced to RAS	tWCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to RAS lead time	tRWL	13		15		20		20		ns	
Write command to CAS lead time	tcWL	8		10		15		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to RAS	tDHR	40		45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32		32	ms	
Refresh period (L-ver)	tREF		128		128		128		128	ms	
Refresh period (SL-ver)	tREF		256		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		0		ns	8
CAS to W delay time	tcWD	36		40		50		50		ns	8
RAS to W delay time	tRWD	73		85		100		110		ns	8
Column address to W delay time	tAWD	48		55		65		70		ns	8
CAS address to W delay time	tcPWD	53		60		70		75		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		10		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		15		15		ns	
RAS to CAS precharge time	tRPC	5		5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tcPT	20		20		30		30		ns	
Access time from CAS precharge	tcPA		30		35		40		45	ns	3
Hyper Page cycle time	tHPC	20		24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	62		71		86		96		ns	17
CAS precharge time (Hyper Page Cycle)	tcP	8		10		10		10		ns	
RAS pulse width(Hyper Page Cycle)	tRASP	50	200K	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		40		45		ns	
OE access time	tOEA		13		15		20		20	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
\overline{OE} to data delay	tOED	13		15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	3	13	3	15	3	20	3	20	ns	7,14
\overline{OE} command hold time	tOEH	13		15		20		20		ns	
Write command set-up time (Test mode in)	tWTS	10		10		10		10		ns	12
Write command hold time (Test mode in)	tWTH	10		10		10		10		ns	12
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	tWRP	10		10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	tWRH	10		10		10		10		ns	
Output data hold time	tDOH	5		5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	tREZ	3	13	3	15	3	20	3	20	ns	7,14,15
Output buffer turn off delay from \overline{W}	tWEZ	3	13	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	tWED	15		15		20		20		ns	
\overline{OE} to \overline{CAS} hold time	tOCH	5		5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		5		ns	
\overline{OE} precharge time	tOEP	5		5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	tWPE	5		5		5		5		ns	
\overline{RAS} pulse width (LL-ver)	tRASS	100		100		100		100		μ s	16
\overline{RAS} precharge time (LL-ver)	tRPS	90		110		130		150		ns	16
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	95		115		135		155		ns	
Read-modify-write cycle time	tRWC	138		160		190		210		ns	
Access time from \overline{RAS}	tRAC		55		65		75		85	ns	3,4,11,13
Access time from \overline{CAS}	tCAC		18		20		25		25	ns	3,4,5,13
Access time from column address	tAA		30		35		40		45	ns	3,11,13
\overline{RAS} pulse width	tRAS	55	10,000	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	tCAS	13	10,000	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	tRSH	18		20		25		25		ns	
\overline{CAS} hold time	tCSH	43		50		55		65		ns	
Column address to \overline{RAS} lead time	tRAL	30		35		40		45		ns	
\overline{CAS} to \overline{W} delay time	tCWD	41		45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	78		90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	53		60		70		75		ns	8
Hyper Page cycle time	tHPC	25		29		34		39		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	67		76		91		101		ns	17

TEST MODE CYCLE (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{\text{RAS}}$ pulse width (Hyper Page Cycle)	trASP	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		18		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	18		20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	18		20		25		25		ns	

TEST MODE DESCRIPTION

The KM48C2104A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 2Mx8 DRAM can be tested as if it were a 1Mx8 DRAM.

$\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" or " $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time (1/2 in cases of N test pattern).

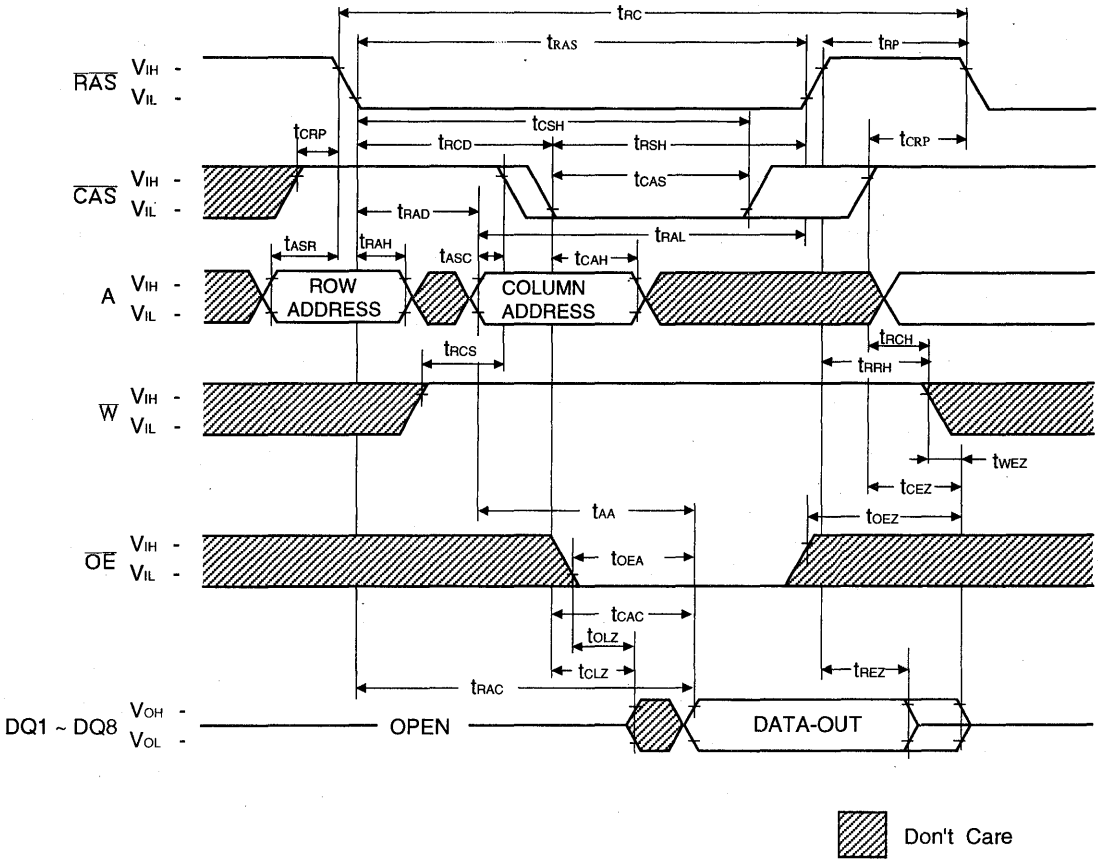
NOTES

- An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without t_{HPC} and t_{HPWC}.
- Measured with a load equivalent to 2TTL loads and 100pF.
- Operation within the t_{RC}(max) limit insures that t_{TRAC}(max) can be met. t_{RC}(max) is specified as a reference point only. If t_{RC} is greater than the specified t_{RC}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{RC} ≥ t_{RC}(max).
- t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{TRAD}(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCS}, t_{TRWD}, t_{ICWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If t_{WCS} ≥ t_{WCS}(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{ICWD} ≥ t_{ICWD}(min), t_{TRWD} ≥ t_{TRWD}(min) and t_{AWD} ≥ t_{AWD}(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
- Operation within the t_{TRAD}(max) limit insures that t_{TRAC}(max) can be met. t_{TRAD}(max) is specified as a reference point only. If t_{TRAD} is greater than the specified t_{TRAD}(max) limit, then access time is controlled by t_{AA}.
- These specifications are applied in the test mode.
- In test mode read cycle, the value of t_{TRAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
- t_{TREZ}(max), t_{TCEZ}(max), t_{TWEZ}(max) and t_{TOEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
- If RAS goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before RAS high going, the open circuit condition of the output is achieved by RAS high going
- t_{ASC} ≥ t_{CPmin}, Assumtn t_r=2.0ns



TIMING DIAGRAM

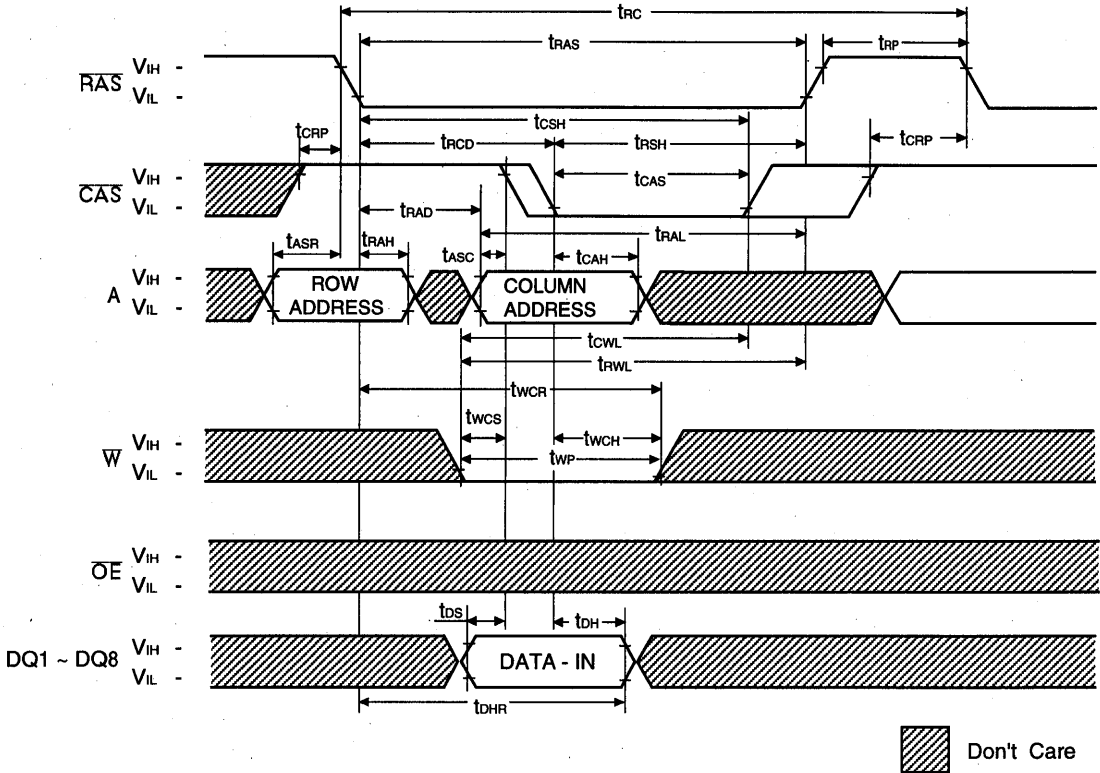
READ CYCLE



6

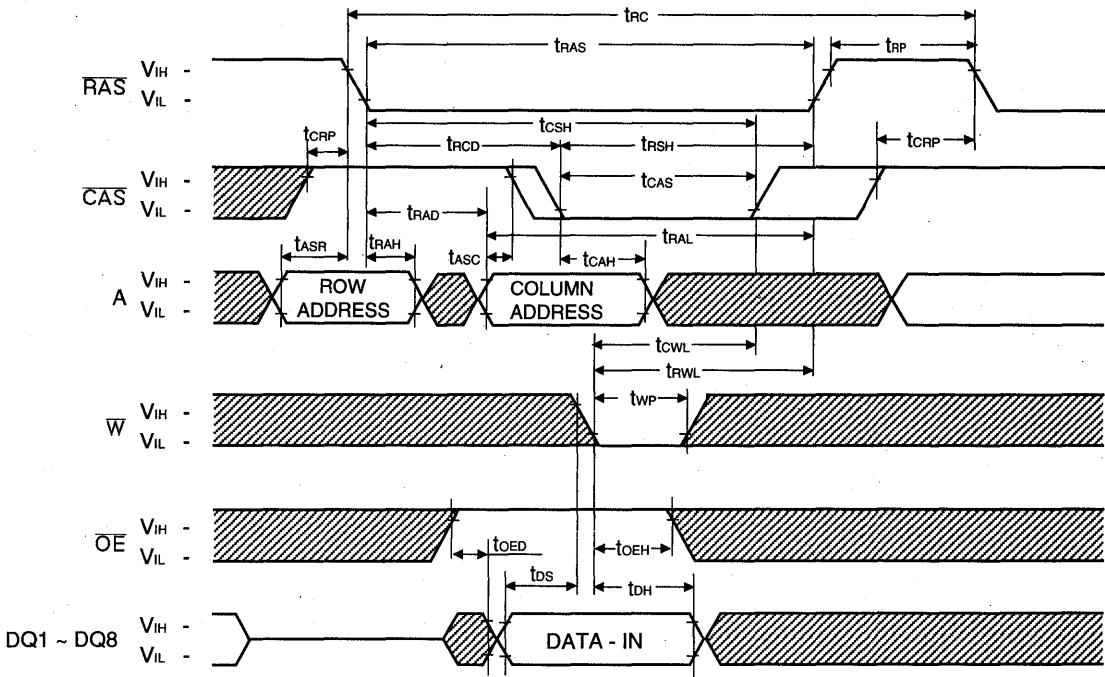
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



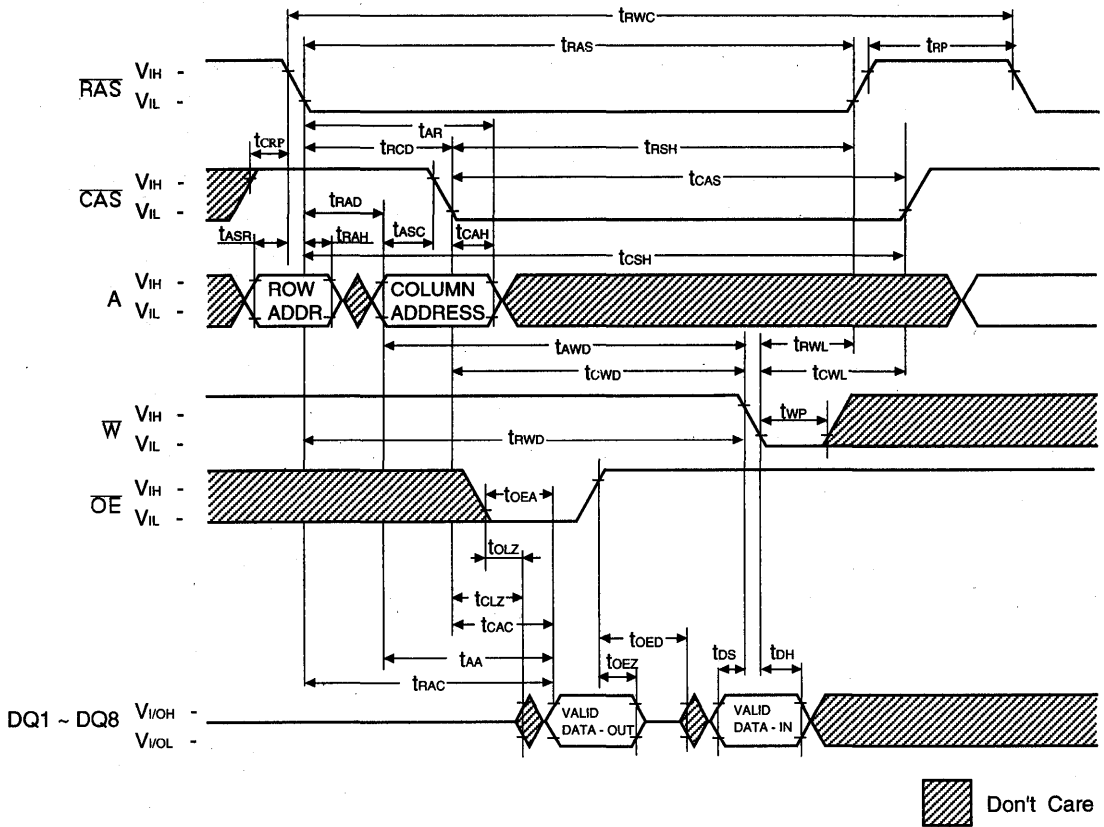
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



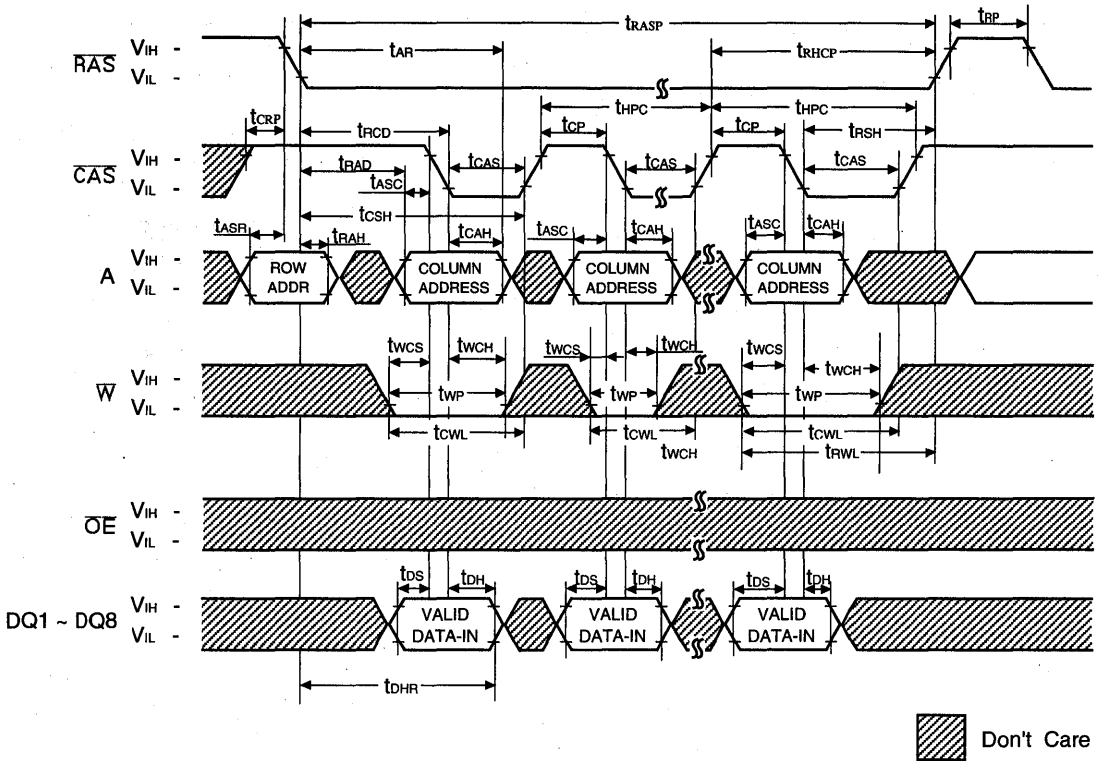
 Don't Care

READ - MODIFY - WRITE CYCLE



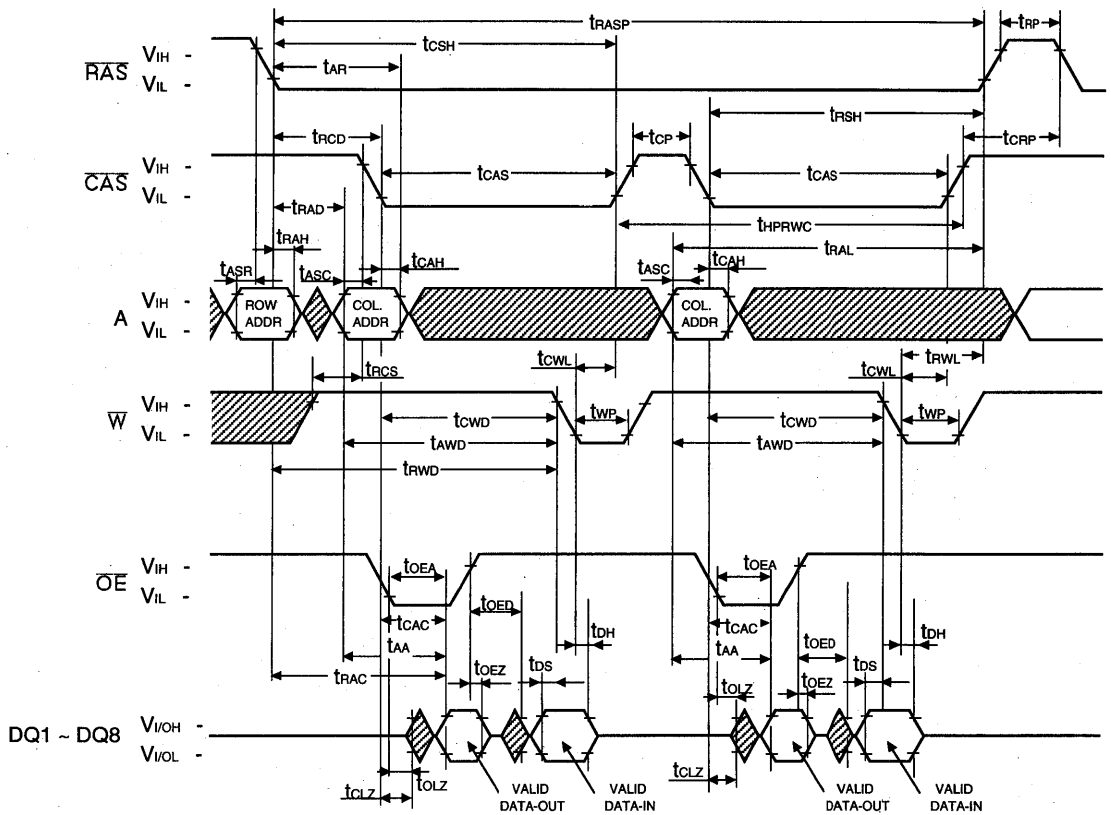
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



 Don't Care

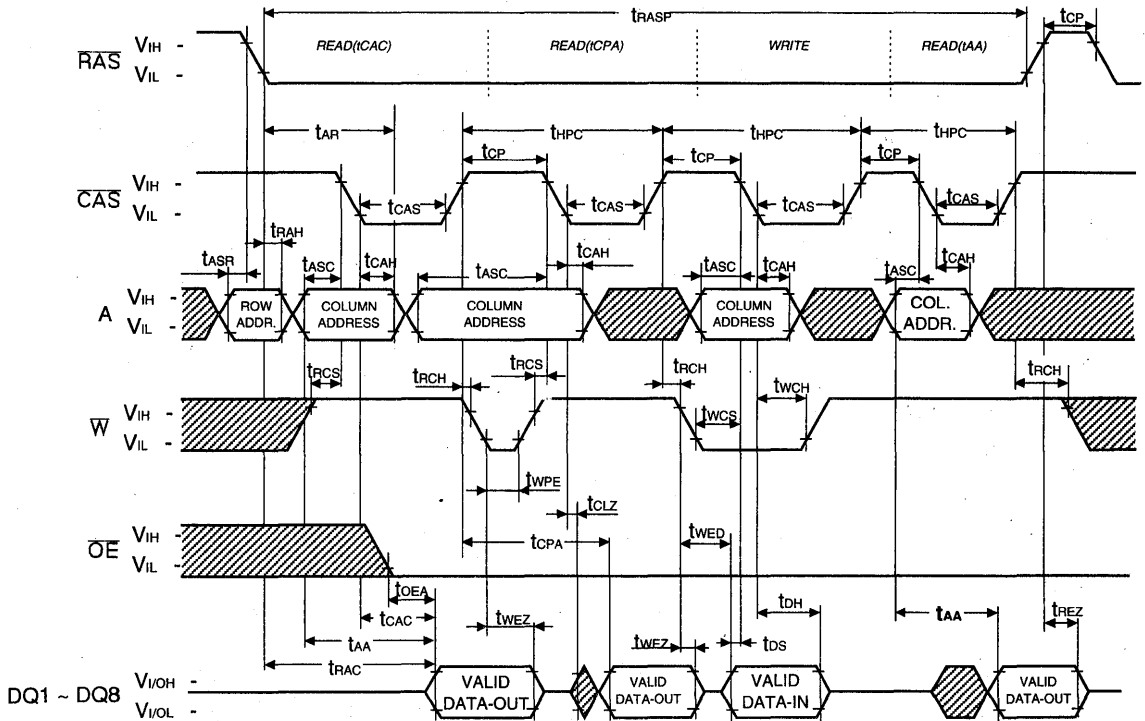
HYPER PAGE READ-MODIFY-WRITE CYCLE



 Don't Care

6

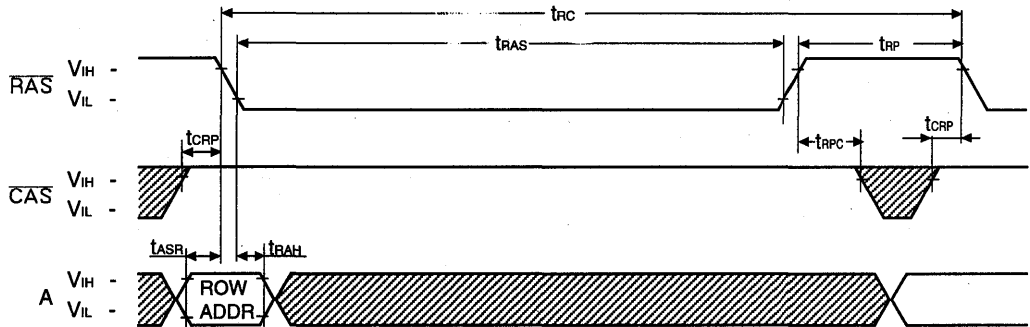
HYPER PAGE READ AND WRITE MIXED CYCLE



 Don't Care

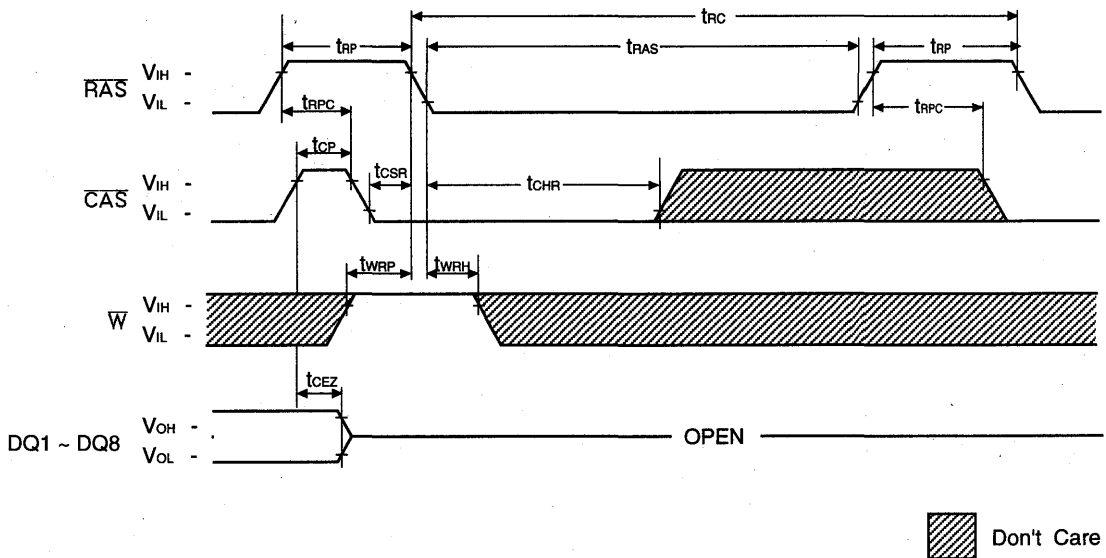
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



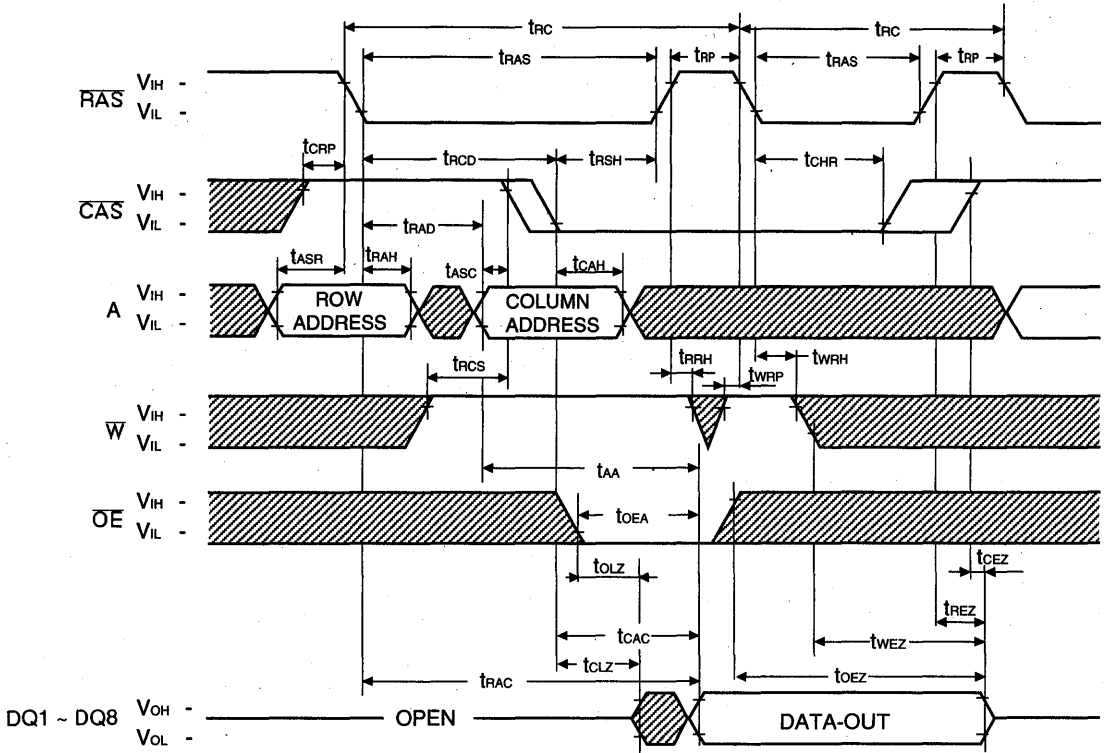
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care



Don't Care

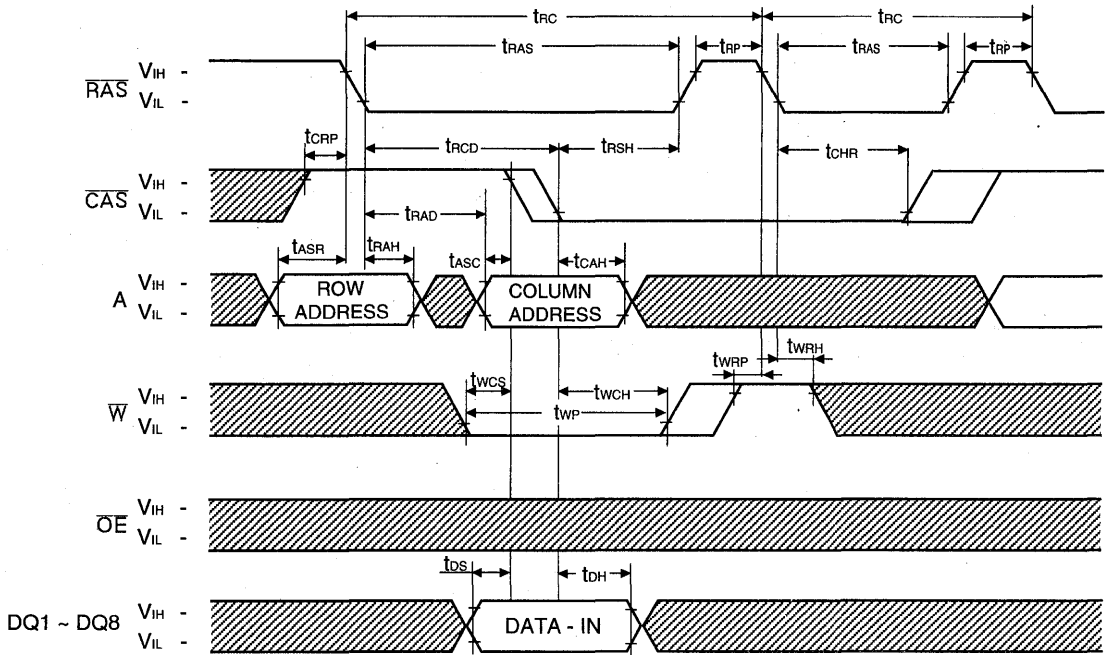
HIDDEN REFRESH CYCLE (READ)



 Don't Care

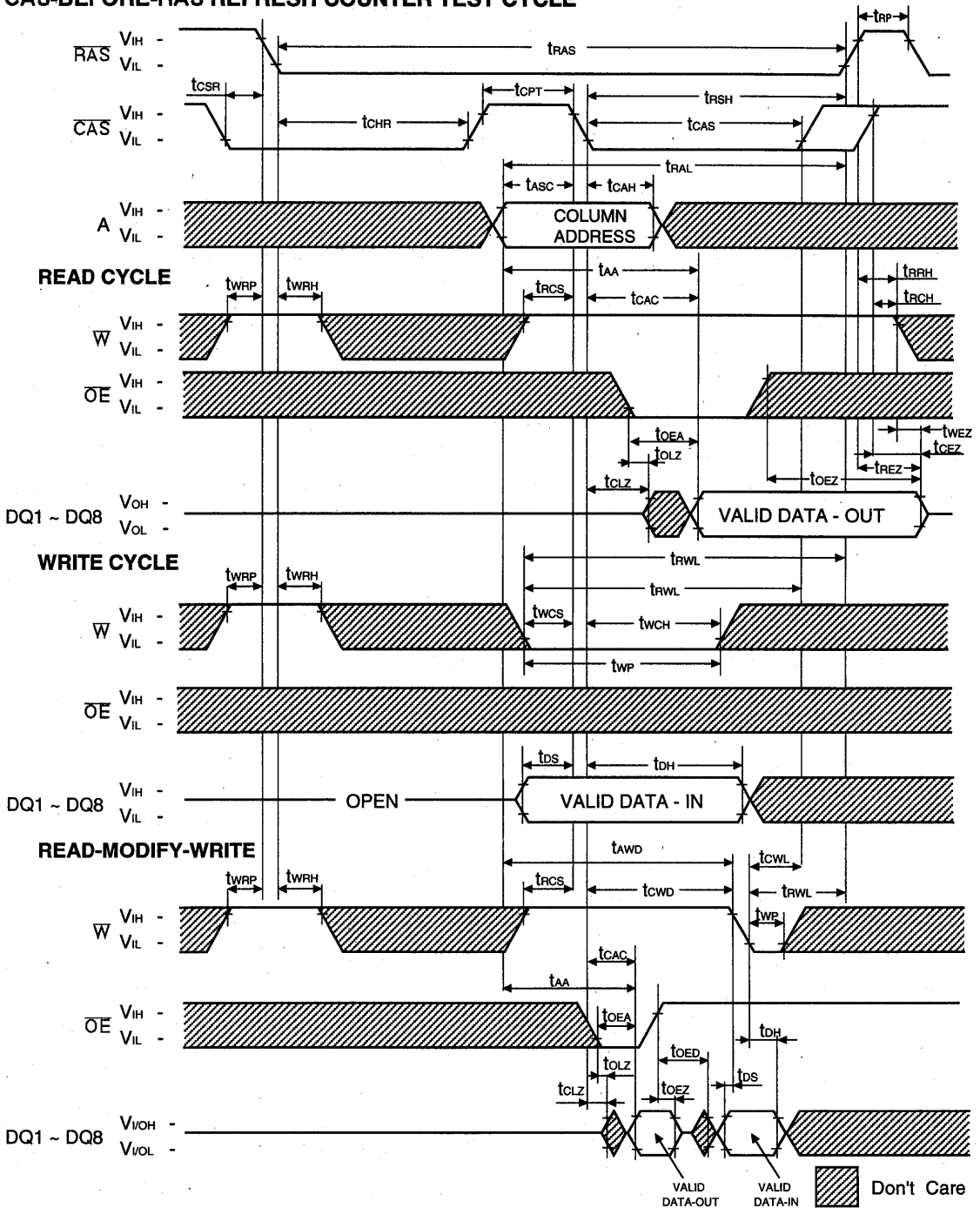
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



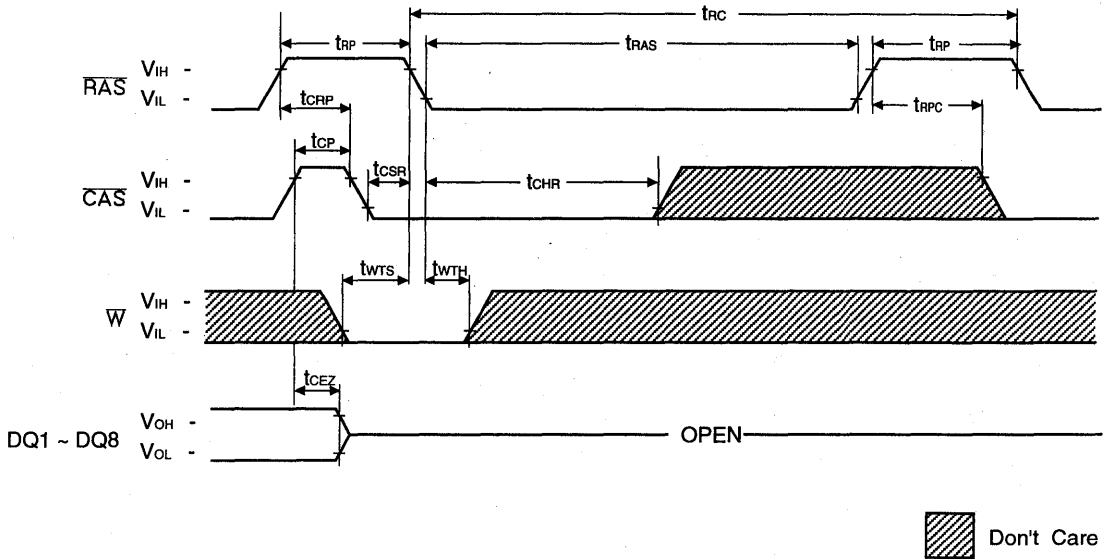
 Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE

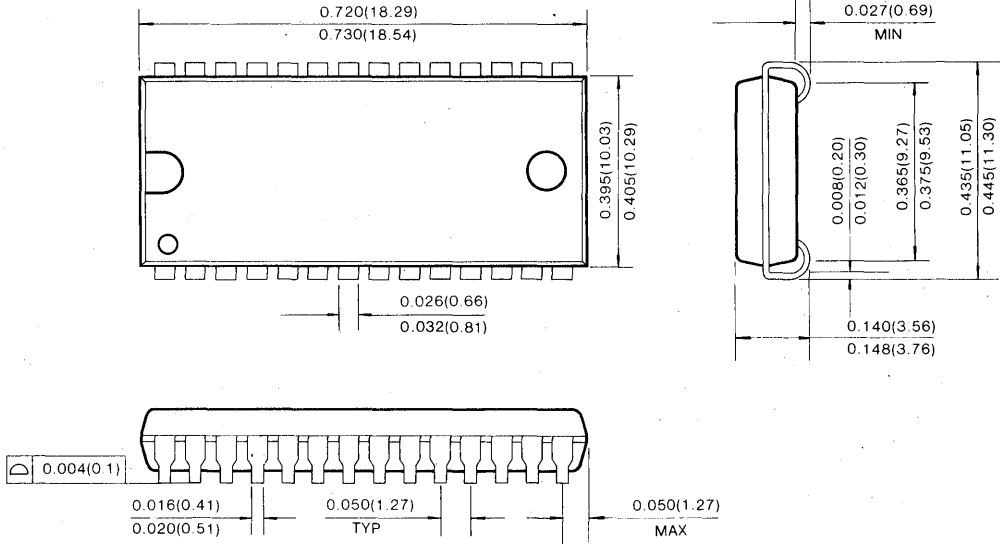
NOTE : $\bar{O}E$, A = Don't Care



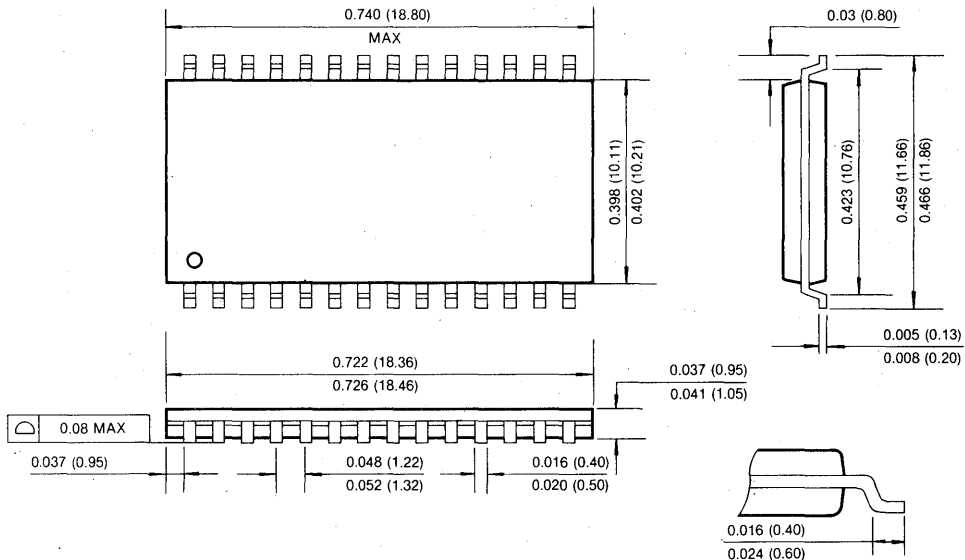
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



2M × 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM48V2000A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48V2000A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48V2000A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single+3.3V±0.3V power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

GENERAL DESCRIPTION

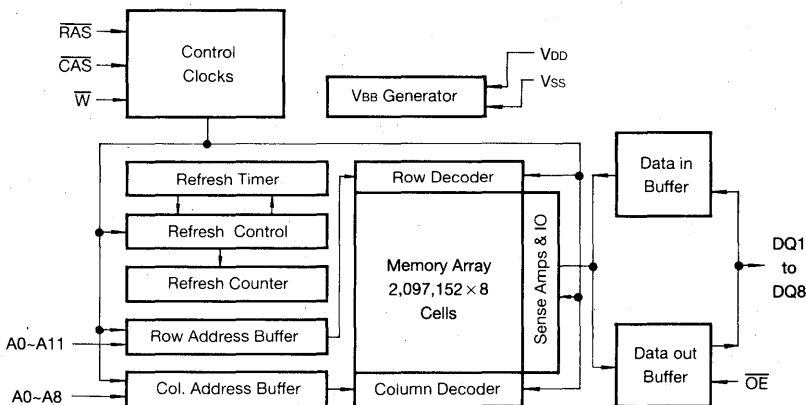
The Samsung KM48V2000A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2000A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

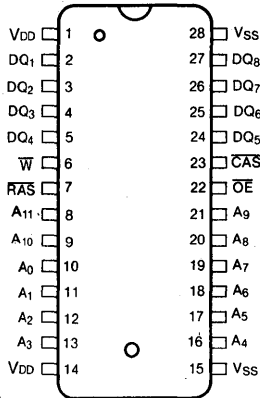
The KM48V2000A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

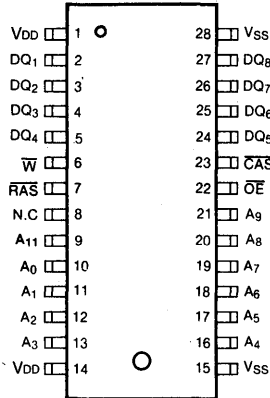


PIN CONFIGURATION (Top Views)

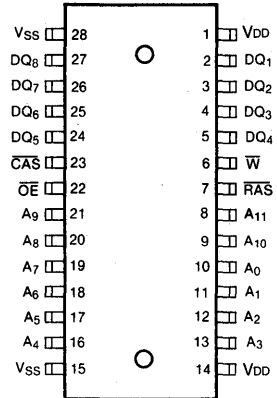
• KM48V2000 AJ/ALJ/ALLJ/ASLJ



• KM48V2000 AT/ALT/ALLT/ASLT



• KM48V2000 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A ₀ -A ₁₁	Address Inputs
DQ ₁ -8	Data In/Out
VSS	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 4.6	V
Voltage on VDD Supply Relative to Vss	VDD	-0.5 ~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	VDD + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8 Icc1	-	80 70 60	mA mA mA
Standby Current (RAS=CAS=W=V _{IH})	KM48V2000A KM48V2000AL KM48V2000ALL KM48V2000ASL Icc2	-	2 1 1 1	mA mA mA mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8 Icc3	-	80 70 60	mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8 Icc4	-	70 60 50	mA mA mA
Standby Current (RAS=CAS=W=VDD-0.2V)	KM48V2000A KM48V2000AL KM48V2000ALL KM48V2000ASL Icc5	-	1 300 200 200	mA μA μA μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM48V2000A/AL/ALL/ASL-6 KM48V2000A/AL/ALL/ASL-7 KM48V2000A/AL/ALL/ASL-8 Icc6	-	80 70 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=VDD-0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DIN=Don't Care TRC=31.25μS(L-Ver.) 62.5μS(SL-Ver.), TRAS=TRAS min. ~300ms	KM48V2000AL KM48V2000ASL Icc7	-	450 350	μA μA
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=VDD-0.2V or 0.2V DQ1-DQ8=VDD-0.2V, 0.2V or Open	KM48V2000ALL Icc8	-	250	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	$I_{i(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{o(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4} , Address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 \sim A_{11}$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Input Capacitance ($DQ_1 \sim DQ_8$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Test Condition : $V_{ih}/V_{il} = 2.0V/0.8V$, $V_{oh}/V_{ol} = 2.0V/0.8V$, Output Loading $C_L = 100pF$

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to \overline{RAS}	tAR	45		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to \overline{RAS}	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to \overline{RAS} lead time	tRWL	15		20		20		ns	
Write command to \overline{CAS} lead time	tCWL	15		20		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to \overline{RAS}	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	8
\overline{CAS} to \overline{W} delay time	tCWD	40		50		50		ns	8
\overline{RAS} to \overline{W} delay time	tRWD	85		100		110		ns	8
Column address to \overline{W} delay time	tAWD	55		65		70		ns	8
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		15		15		ns	
\overline{RAS} to \overline{CAS} precharge time	tRPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} -B-R counter test cycle)	tCPT	20		30		30		ns	
Access time from \overline{CAS} precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	85		100		105		ns	
\overline{CAS} precharge time (Fast Page mode)	tCP	10		10		10		ns	
\overline{RAS} pulse width (Fast Page mode)	tRASP	60	200,000	70	200,000	80	200,000	ns	
\overline{RAS} hold time from \overline{CAS} precharge	tRHCP	35		40		45		ns	
\overline{OE} access time	tOEA		15		20		20	ns	
\overline{OE} to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from \overline{OE}	tOEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	tOEH	15		20		20		ns	

6

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\bar{W} to \bar{RAS} precharge time (\bar{C} - B - \bar{R} refresh)	tWRP	10		10		10		ns	
W to RAS hold time (\bar{C} - B - \bar{R} refresh)	tWRH	10		10		10		ns	
RAS pulse width (\bar{C} - B - \bar{R} self refresh)	tRASS	100		100		100		us	15
RAS precharge time (\bar{C} - B - \bar{R} self refresh)	tRPS	110		130		150		ns	15
\bar{CAS} hold time (\bar{C} - B - \bar{R} self refresh)	tCHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

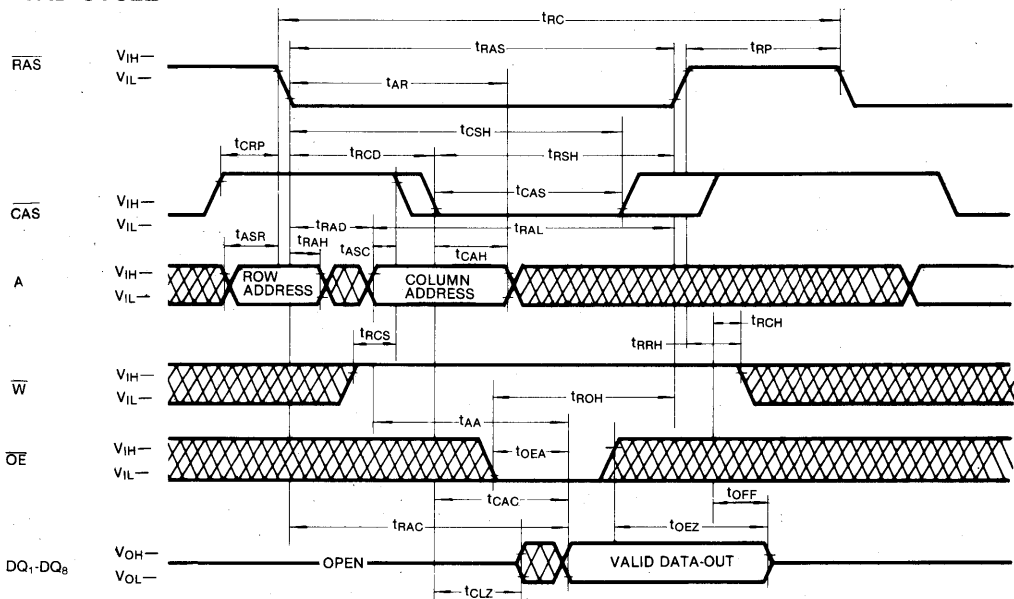
Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	115		135		155		ns	
Read-modify-write cycle time	tRWC	160		190		210		ns	
Access time from \bar{RAS}	tRAC		65		75		85	ns	3,4,11
Access time from \bar{CAS}	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
RAS pulse width	tRAS	65	10,000	75	10,000	85	10,000	ns	
\bar{CAS} pulse width	tCAS	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	tRSH	20		25		25		ns	
\bar{CAS} hold time	tCSH	65		75		85		ns	
Column address to \bar{RAS} lead time	tRAL	35		40		45		ns	
\bar{CAS} to \bar{W} delay time	tCWD	45		55		55		ns	8
RAS to \bar{W} delay time	tRWD	90		105		115		ns	8
Column address to \bar{W} delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tPC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tPRWC	90		105		110		ns	
RAS pulse width (Fast Page Mode)	tRASP	65	200,000	75	200,000	85	200,000	ns	
Access time from \bar{CAS} precharge	tCPA		40		45		50	ns	3
\bar{OE} access time	tOEA		20		25		25	ns	
\bar{OE} to data delay	tOED	20		25		25		ns	
\bar{OE} command hold time	tOEH	20		25		25		ns	

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and $V_{oh}=2.0V(I_{OUT}=2mA)$, $V_{ol}=0.8V(I_{OUT}=2mA)$
4. Operation within the $t_{RC}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

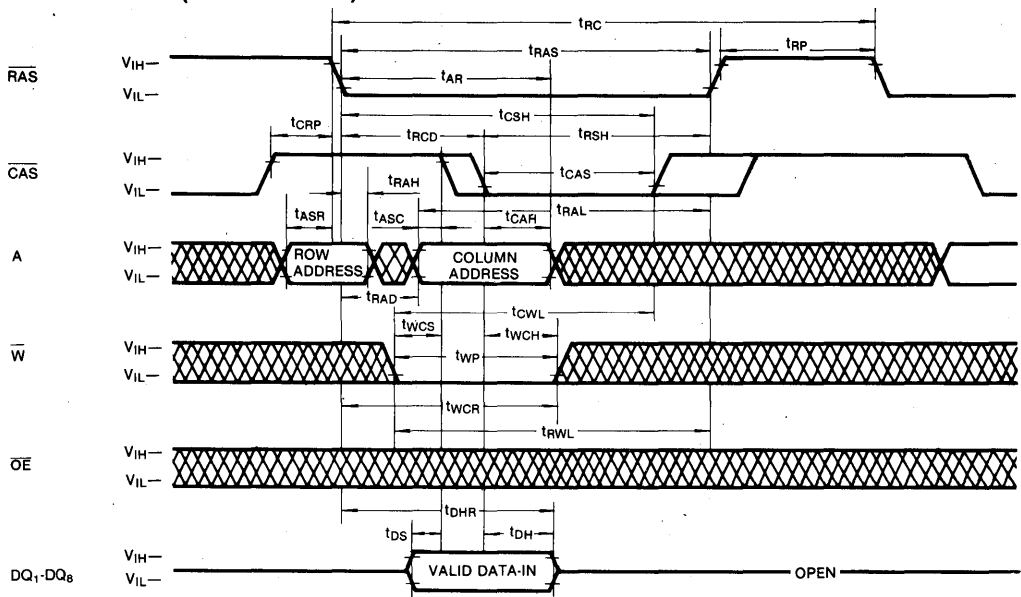
TIMING DIAGRAMS

READ CYCLE

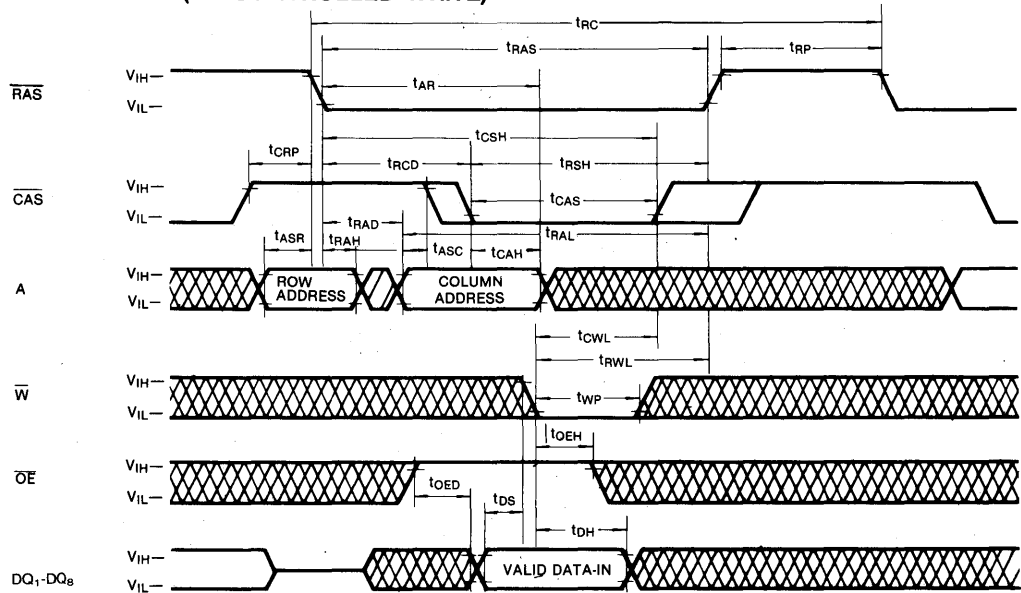


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



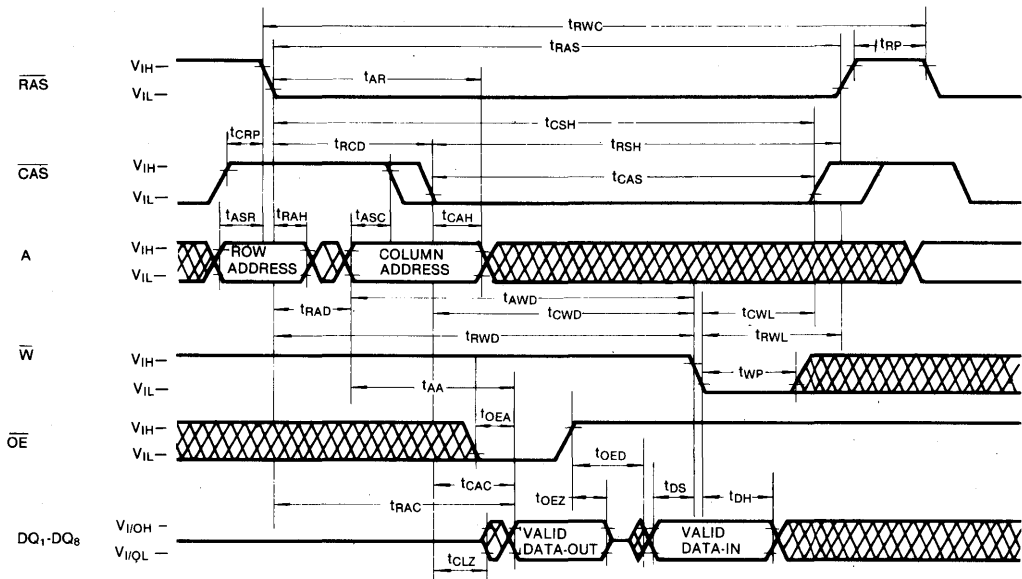
WRITE CYCLE (OE CONTROLLED WRITE)



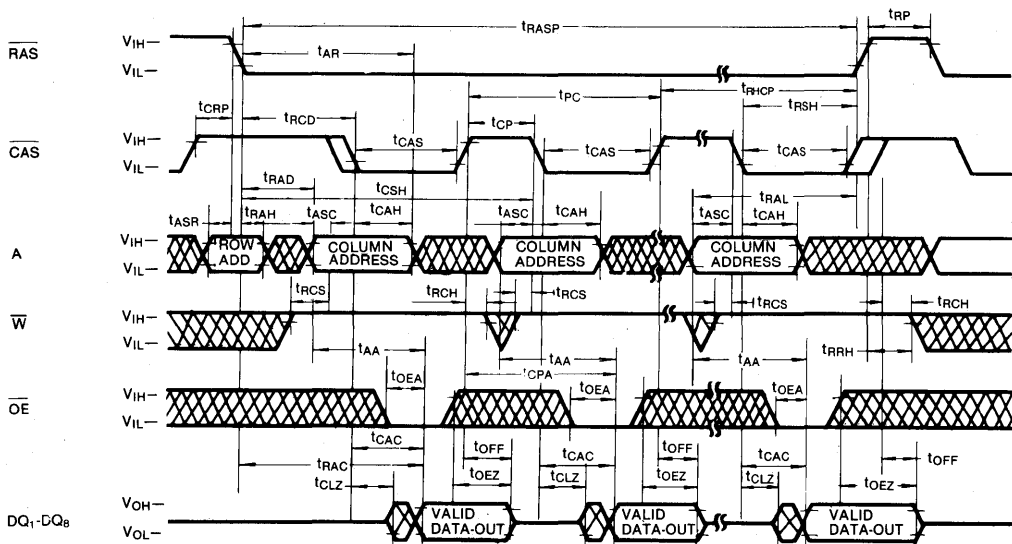
DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



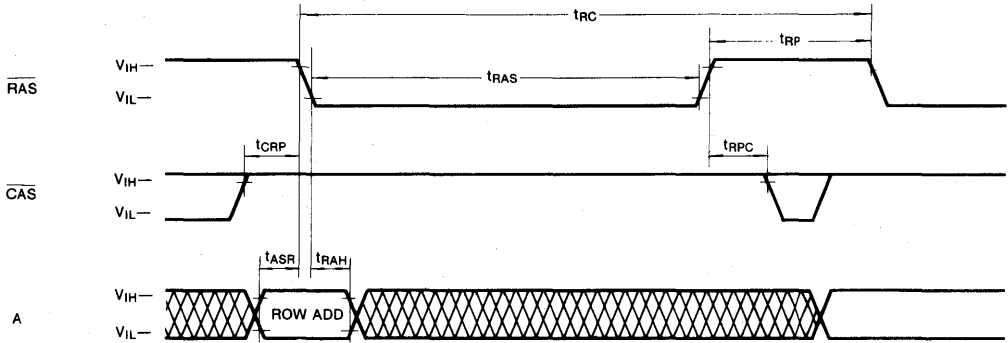
DON'T CARE

6

TIMING DIAGRAMS (Continued)

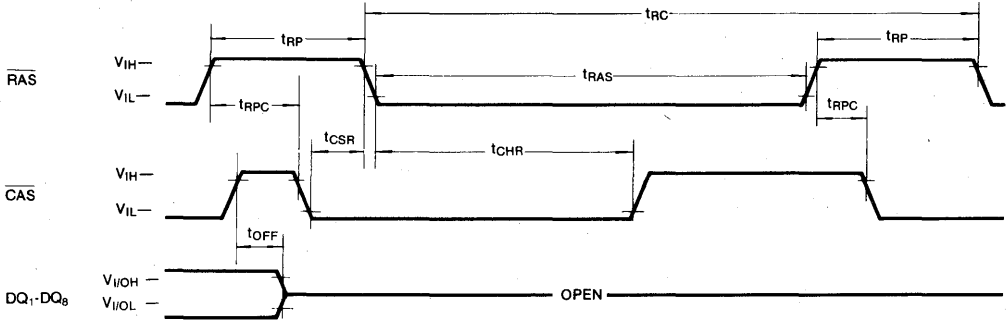
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} = Don't care



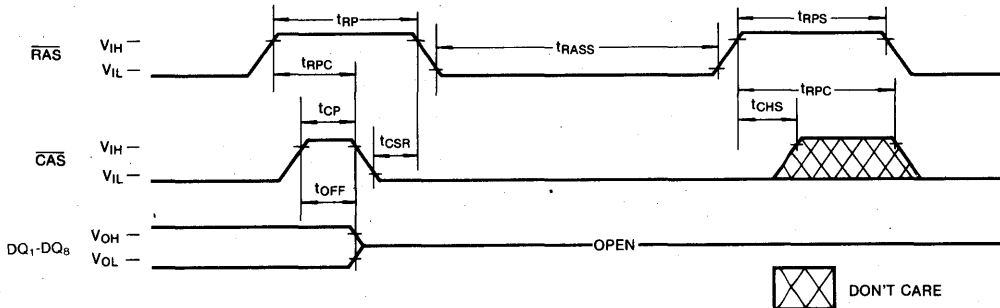
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\overline{W}=V_{IH}$, \overline{OE} , A=Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

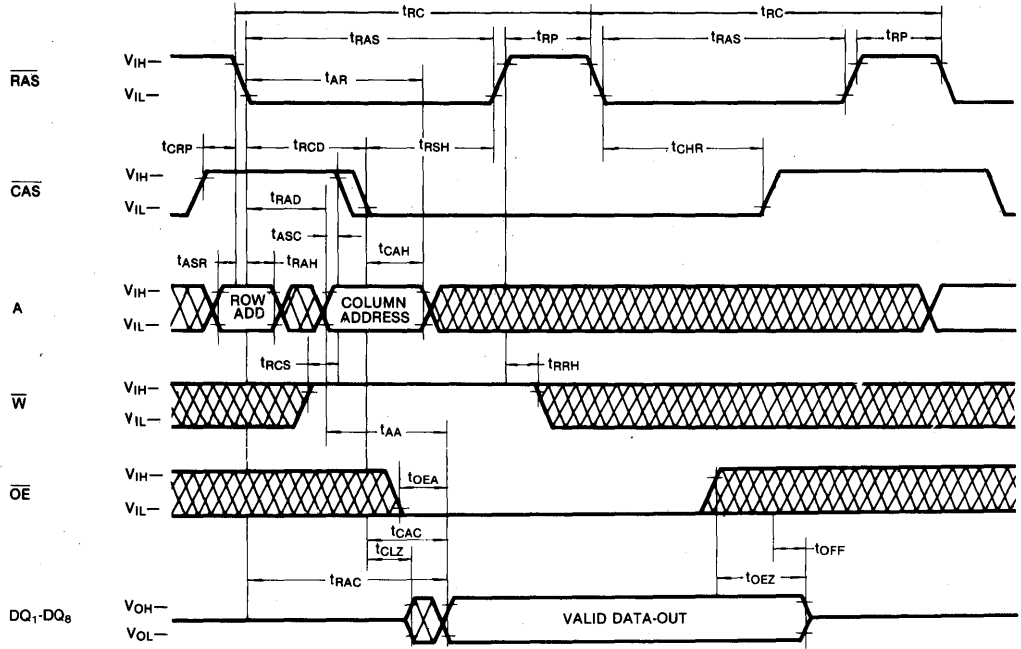
NOTE: \overline{W} , \overline{OE} , A=Don't Care



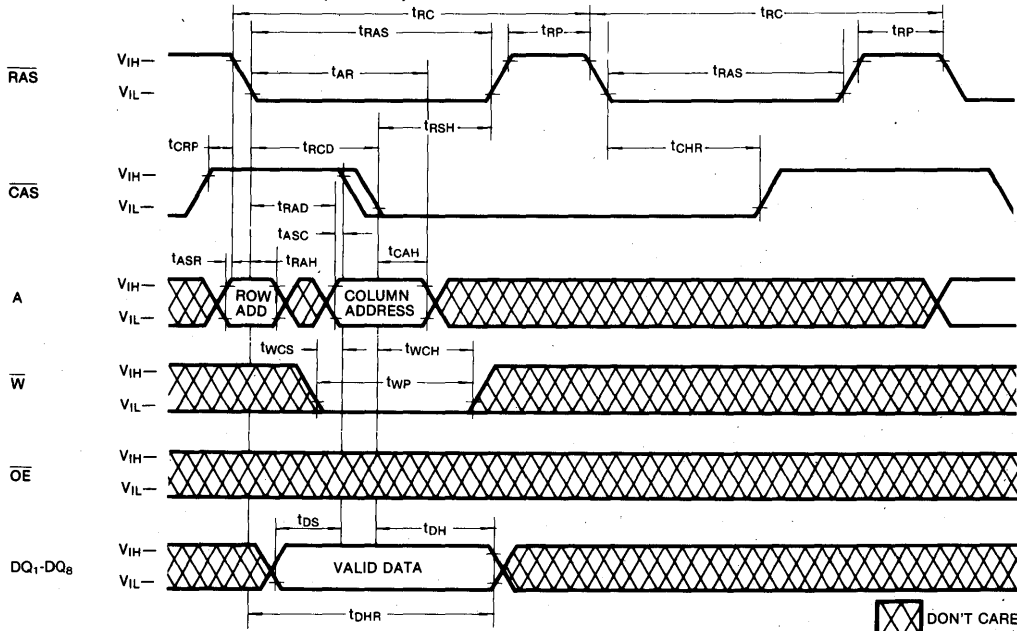
6

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



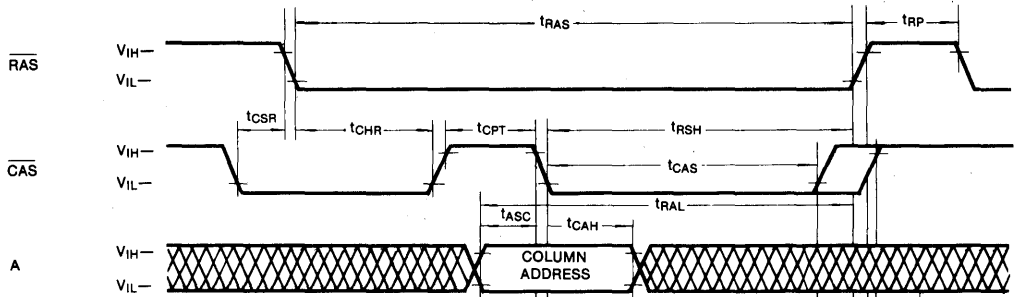
HIDDEN REFRESH CYCLE (WRITE)



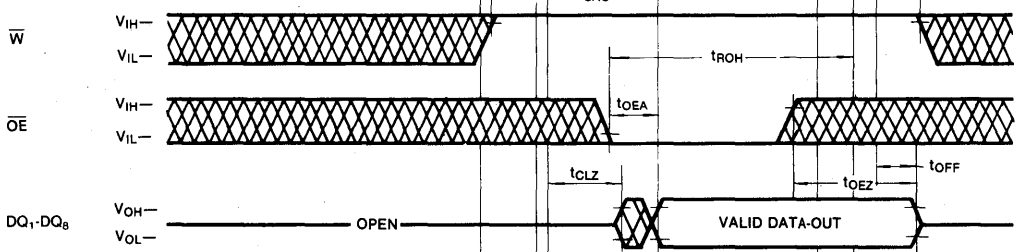
 DON'T CARE

TIMING DIAGRAMS (Continued)

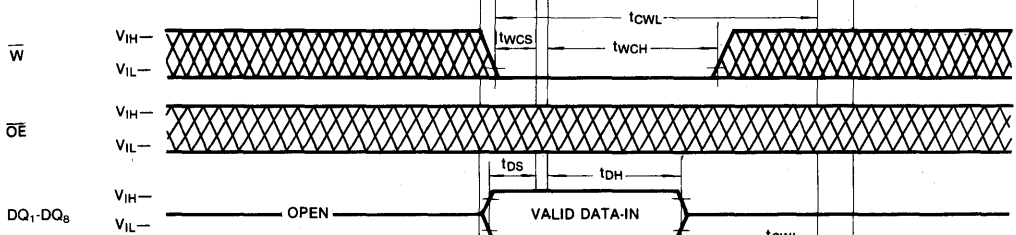
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



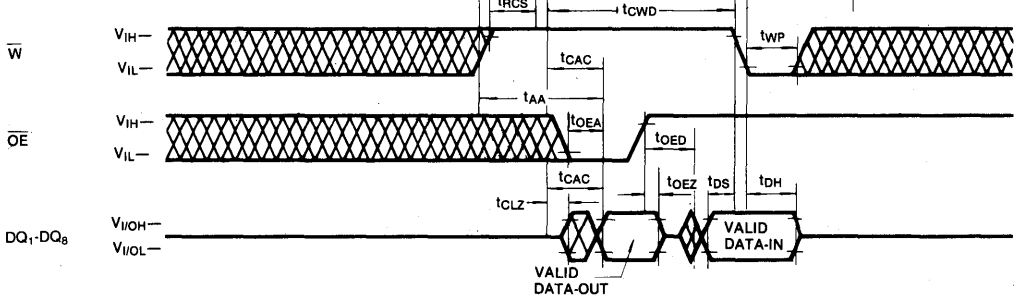
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



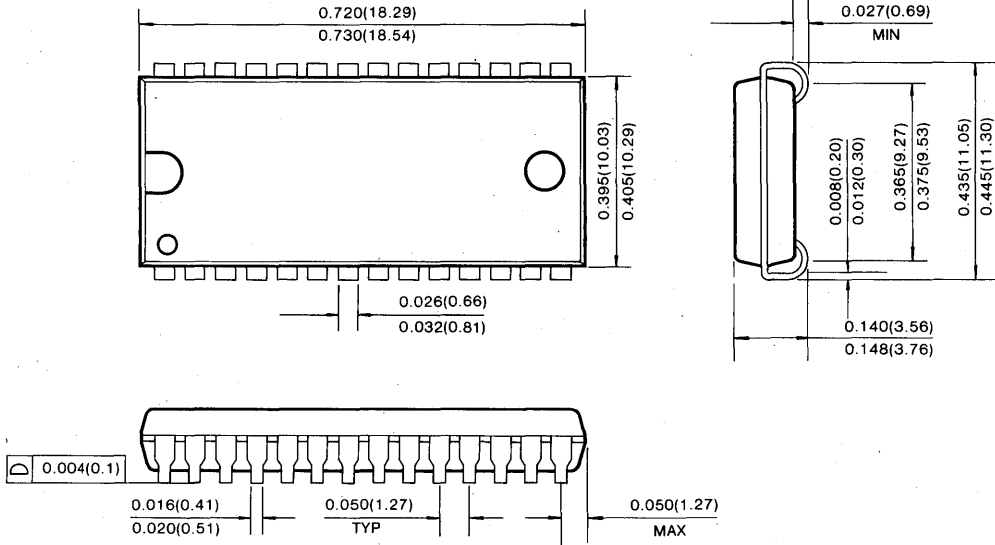
DON'T CARE

6

PACKAGE DIMENSION

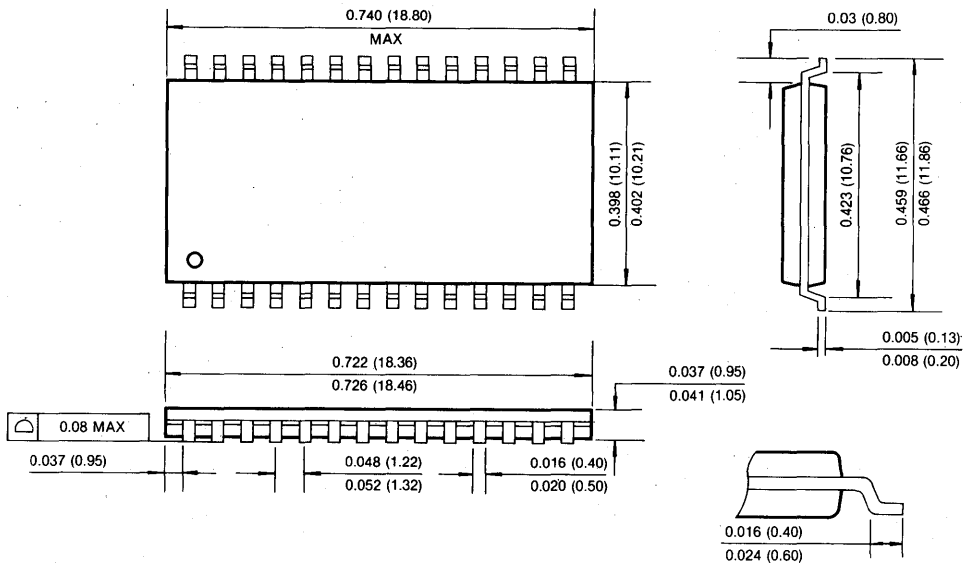
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M × 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{RAC}	t _{CAC}	t _{RC}
KM48V2100A/AL/ALL/ASL-6	60ns	15ns	110ns
KM48V2100A/AL/ALL/ASL-7	70ns	20ns	130ns
KM48V2100A/AL/ALL/ASL-8	80ns	20ns	150ns

- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- Single+3.3V±0.3V power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

GENERAL DESCRIPTION

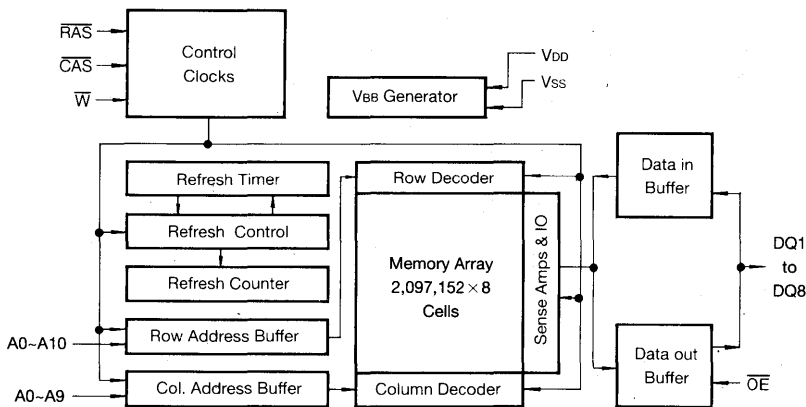
The Samsung KM48V2100A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2100A/AL/ALL/ASL features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM48V2100A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM

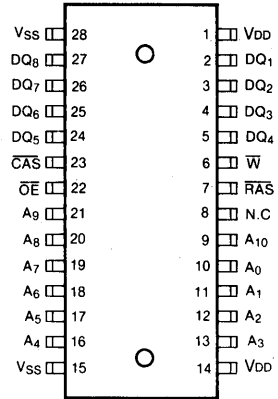
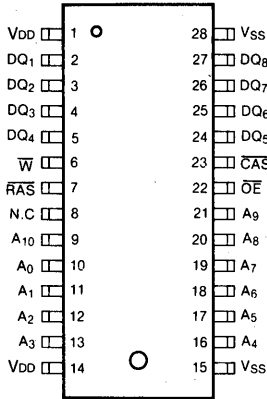
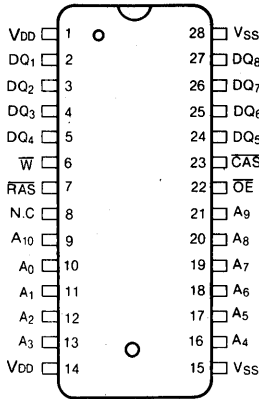


PIN CONFIGURATION (Top Views)

• KM48V2100 AJ/ALJ/ALLJ/ASLJ

• KM48V2100 AT/ALT/ALLT/ASLT

• KM48V2100 ATR/ALTR/ALLTR/ASLTR



Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-8	Data In/Out
VSS	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5 ~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (R _{AS} and C _{AS} Cycling @trc=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8 I _{CC1}	-	100 90 80	mA mA mA
Standby Current (R _{AS} =C _{AS} =W=V _{IH})	KM48V2100A KM48V2100AL KM48V2100ALL KM48V2100ASL I _{CC2}	-	2 1 1 1	mA mA mA mA
R _{AS} -Only Refresh Current* (C _{AS} =V _{IH} , R _{AS} Cycling @trc=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8 I _{CC3}	-	100 90 80	mA mA mA
Fast Page Mode Current* (R _{AS} =V _{IL} , C _{AS} , Address Cycling @tpc=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8 I _{CC4}	-	80 70 60	mA mA mA
Standby Current (R _{AS} =C _{AS} =W=V _{DD} -0.2V)	KM48V2100A KM48V2100AL KM48V2100ALL KM48V2100ASL I _{CC5}	-	1 300 200 200	mA μA μA μA
C _{AS} -Before-R _{AS} Refresh Current* (R _{AS} and C _{AS} Cycling @trc=min.)	KM48V2100A/AL/ALL/ASL-6 KM48V2100A/AL/ALL/ASL-7 KM48V2100A/AL/ALL/ASL-8 I _{CC6}	-	100 90 80	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V C _{AS} =C _{AS} -Before-R _{AS} Cycling or 0.2V D _{IN} =Don't Care Trc=62.5μS(L-Ver.) 125μS(SL-Ver.), TRAS=TRAS min.~300ns	KM48V2100AL KM48V2100ASL I _{CC7}	-	400 300	μA μA
Self Refresh Current R _{AS} =C _{AS} =0.2V W=OE=A0-A10=V _{DD} -0.2V or 0.2V DQ1~DQ8=V _{DD} -0.2V, 0.2V or Open	KM48V2100ALL I _{CC8}	-	250	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	$I_{i(L)}$	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	$I_{o(L)}$	-10	10	μA
Output High Voltage Level ($I_{OH} = -2mA$)	V_{OH}	2.4	-	V
Output Low Voltage Level ($I_{OL} = 2mA$)	V_{OL}	-	0.4	V

*NOTE: I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3} , Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4} , Address can be changed maximum once within one fast page cycle.

CAPACITANCE ($T_A = 25^\circ C$, $V_{DD} = 3.3V$, $f = 1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance ($A_0 \sim A_{11}$)	C_{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C_{IN2}	-	7	pF
Input Capacitance ($DQ_1 \sim DQ_8$)	C_{DQ}	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$, See notes 1,2)

Test Condition : $V_{in}/V_{il} = 2.0V/0.8V$, $V_{oh}/V_{ol} = 2.0V/0.8V$, Output Loading $C_L = 100pF$

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify-write cycle time	t_{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t_{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t_{CAC}		15		20		20	ns	3,4,5
Access time from column address	t_{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t_{CLZ}	0		0		0		ns	3
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
\overline{RAS} precharge time	t_{RP}	40		50		60		ns	
\overline{RAS} pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t_{RSH}	15		20		20		ns	
\overline{CAS} hold time	t_{CSH}	60		70		80		ns	
\overline{CAS} pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t_{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		20		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		32		32		32	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		65		70		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	85		100		105		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page mode)	tRASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	15		20		20		ns	
Out put buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	15	0	20	0	20	ns	
$\overline{\text{OE}}$ command hold time	tOEH	15		20		20		ns	

6



AC CHARACTERISTICS (Continued)

Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
W to RAS precharge time (C-B-R refresh)	twRP	10		10		10		ns	
W to RAS hold time (C-B-R refresh)	twRH	10		10		10		ns	
RAS pulse width (C-B-R self refresh)	trASS	100		100		100		μs	15
RAS precharge time (C-B-R self refresh)	trPS	110		130		150		ns	15
CAS hold time (C-B-R self refresh)	tcHS	-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

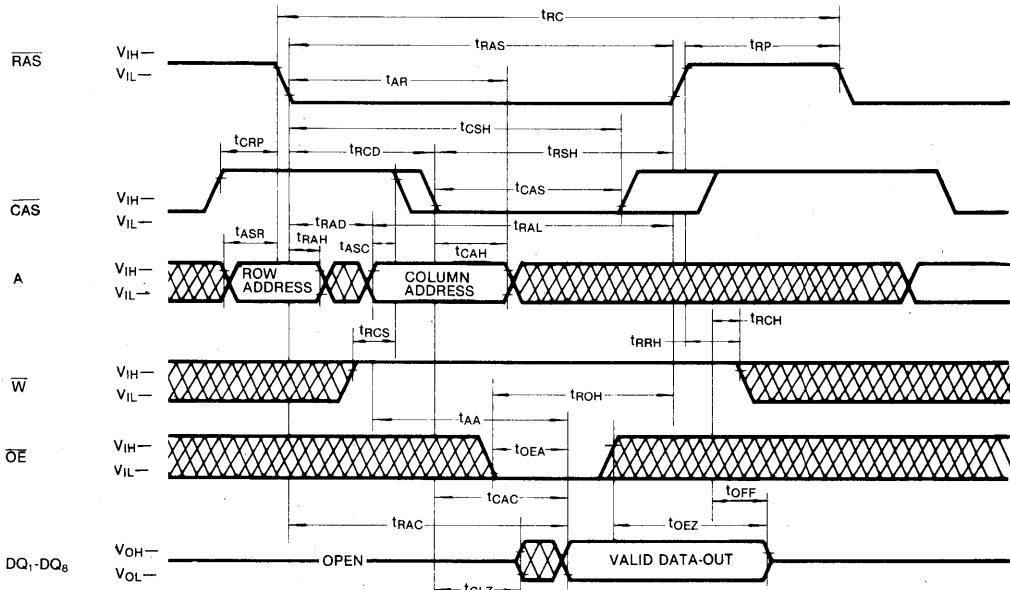
Parameter	Symbol	- 6		- 7		- 8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	115		135		155		ns	
Read-modify-write cycle time	trWC	160		190		210		ns	
Access time from RAS	trAC		65		75		85	ns	3,4,11
Access time from CAS	tcAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
RAS pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
CAS pulse width	tcAS	20	10,000	25	10,000	25	10,000	ns	
RAS hold time	trSH	20		25		25		ns	
CAS hold time	tcSH	65		75		85		ns	
Column address to RAS lead time	trAL	35		40		45		ns	
CAS to W delay time	tcWD	45		55		55		ns	8
RAS to W delay time	trWD	90		105		115		ns	8
Column address to W delay time	tAWD	60		70		75		ns	8
Fast Page mode cycle time	tpC	45		50		55		ns	
Fast Page mode read-modify-write cycle time	tpRWC	90		105		110		ns	
RAS pulse width (Fast Page Mode)	trASP	65	200,000	75	200,000	85	200,000	ns	
Access time from CAS precharge	tcPA		40		45		50	ns	3
OE access time	toEA		20		25		25	ns	
OE to data delay	toED	20		25		25		ns	
OE command hold time	toEH	20		25		25		ns	

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 100pF and $V_{oh}=2.0V(I_{OUT}=2mA)$, $V_{ol}=0.8V(I_{OUT}=2mA)$
4. Operation within the $t_{RC}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RC}(\max)$ is specified as a reference point only. If t_{RC} is greater than the specified $t_{RC}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RC} \geq t_{RC}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWd} , t_{cWd} and t_{AWd} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{cWd} \geq t_{cWd}(\min)$, $t_{RWd} \geq t_{RWd}(\min)$ and $t_{AWd} \geq t_{AWd}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. $t_{OFF}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

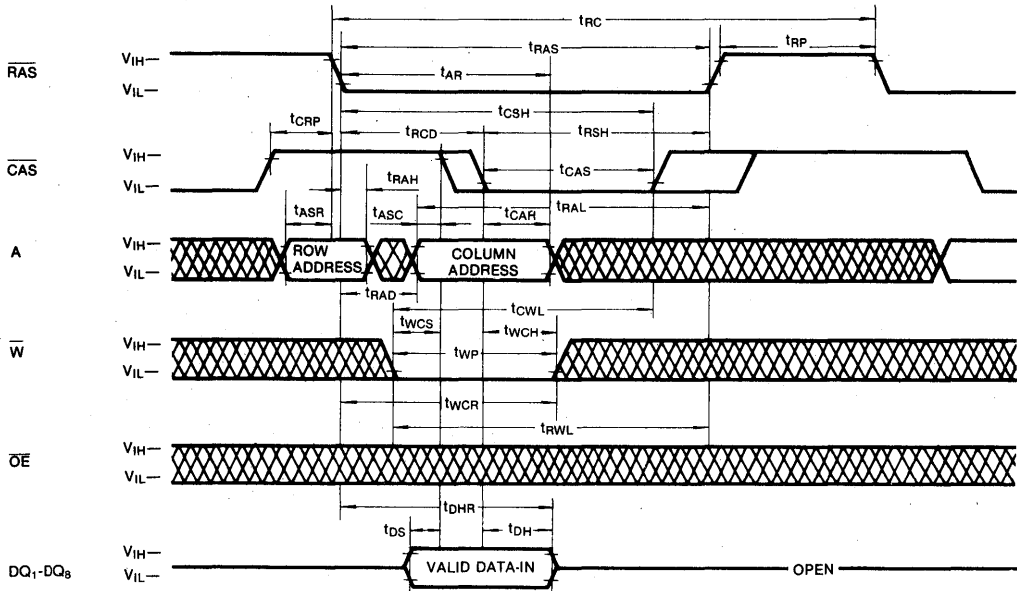
TIMING DIAGRAMS

READ CYCLE

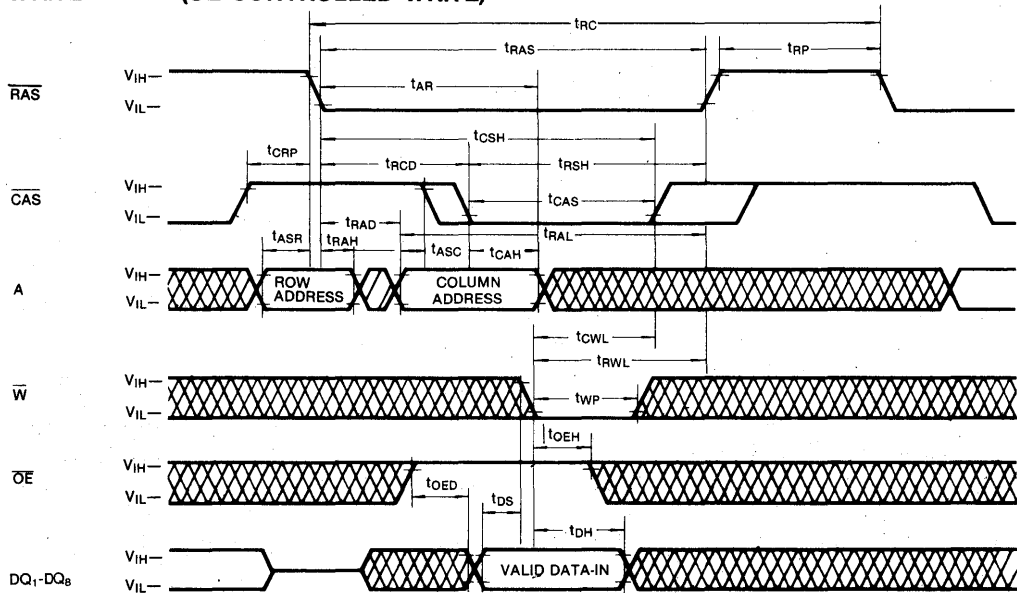


TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY WRITE)



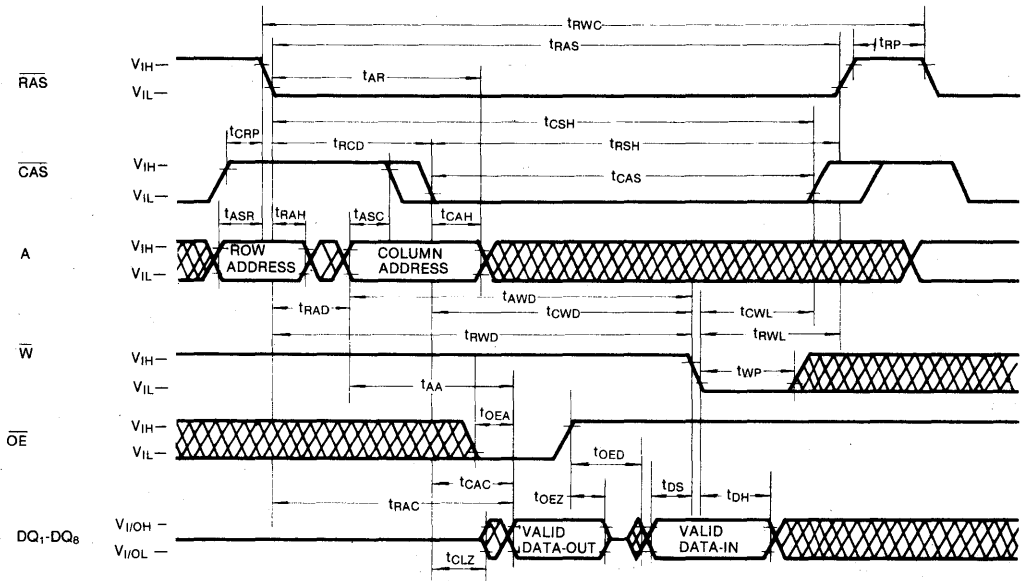
WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)



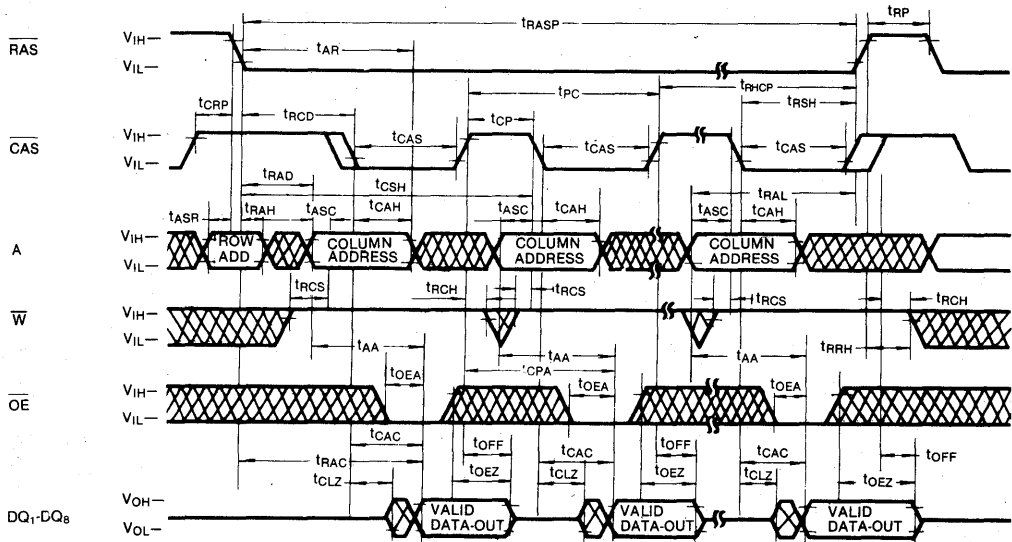
 DON'T CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

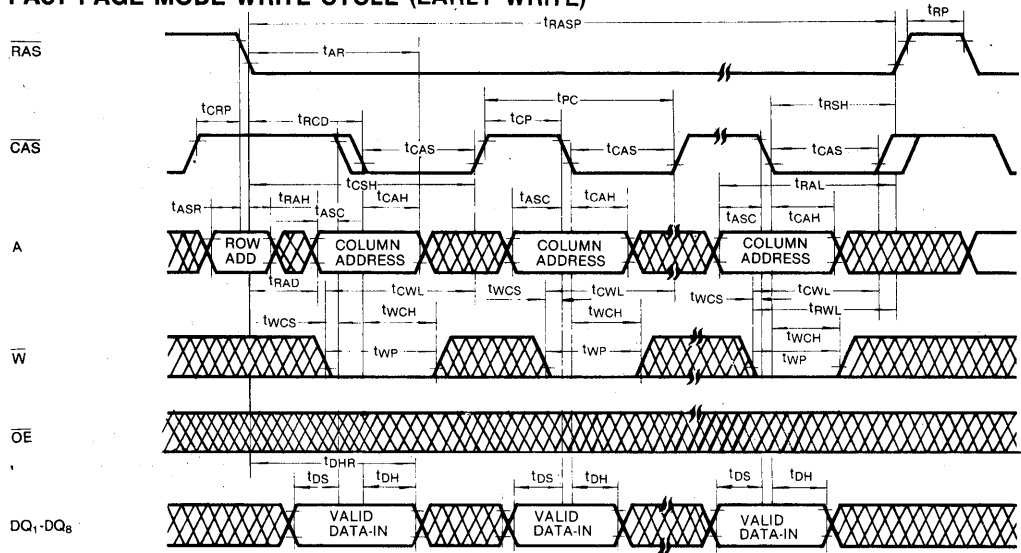


DON'T CARE

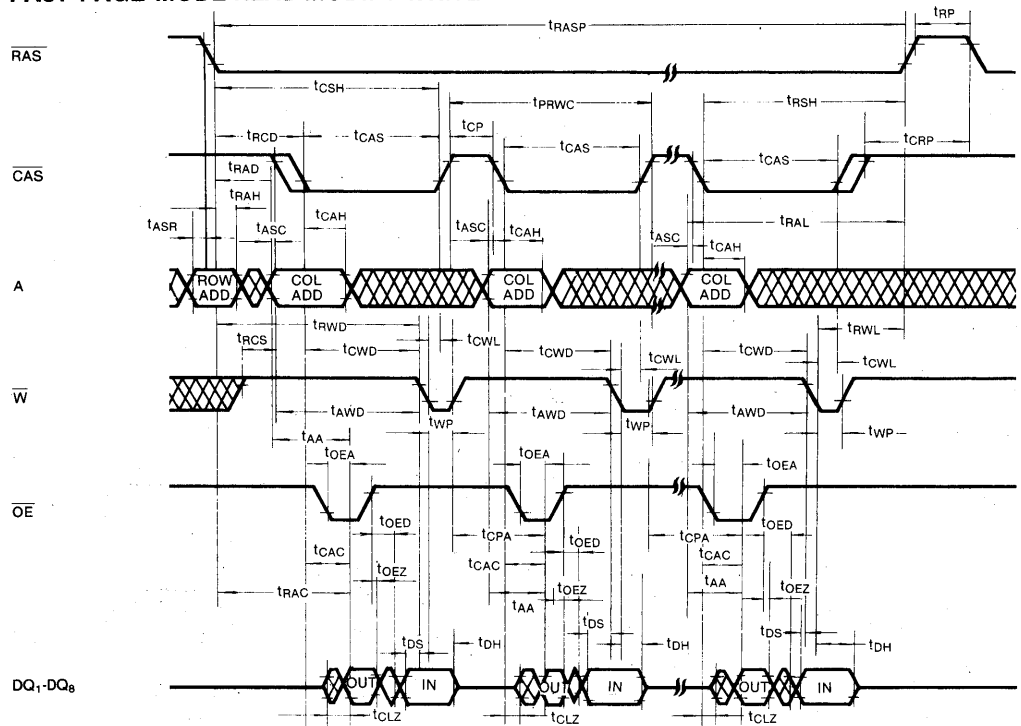
6

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

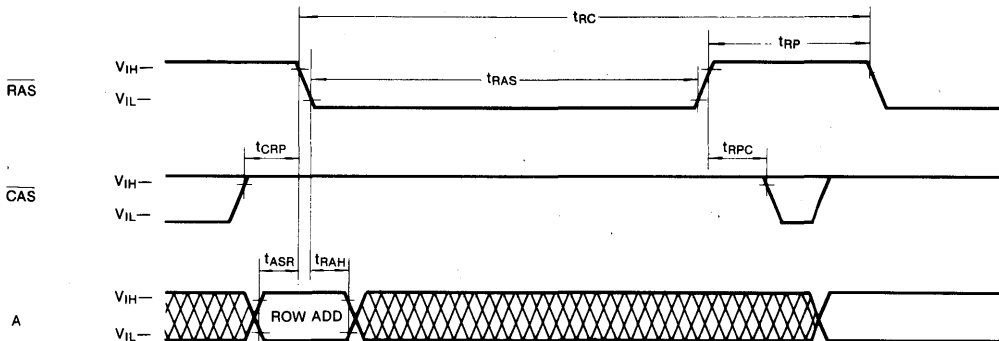


DON'T CARE

TIMING DIAGRAMS (Continued)

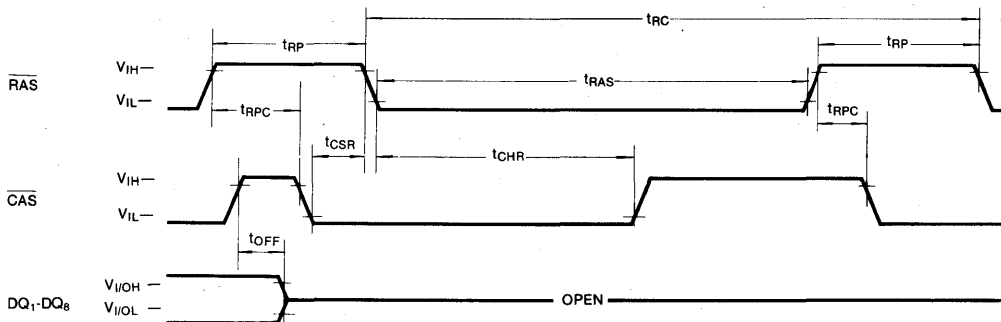
RAS-ONLY REFRESH CYCLE

Note: \overline{W} , \overline{OE} = Don't care



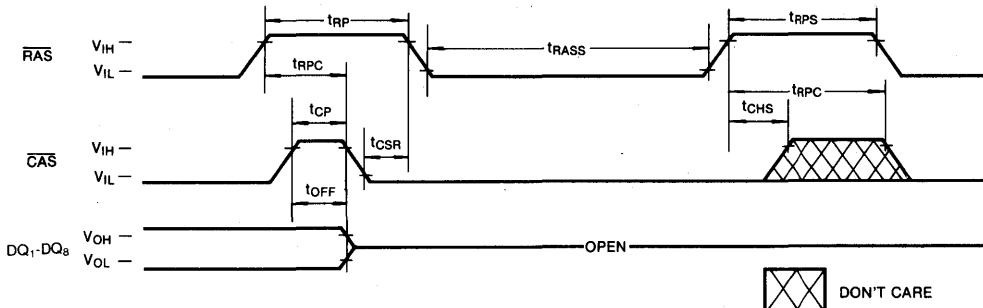
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \overline{W} = V_{IH} , \overline{OE} , A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (LL-version)

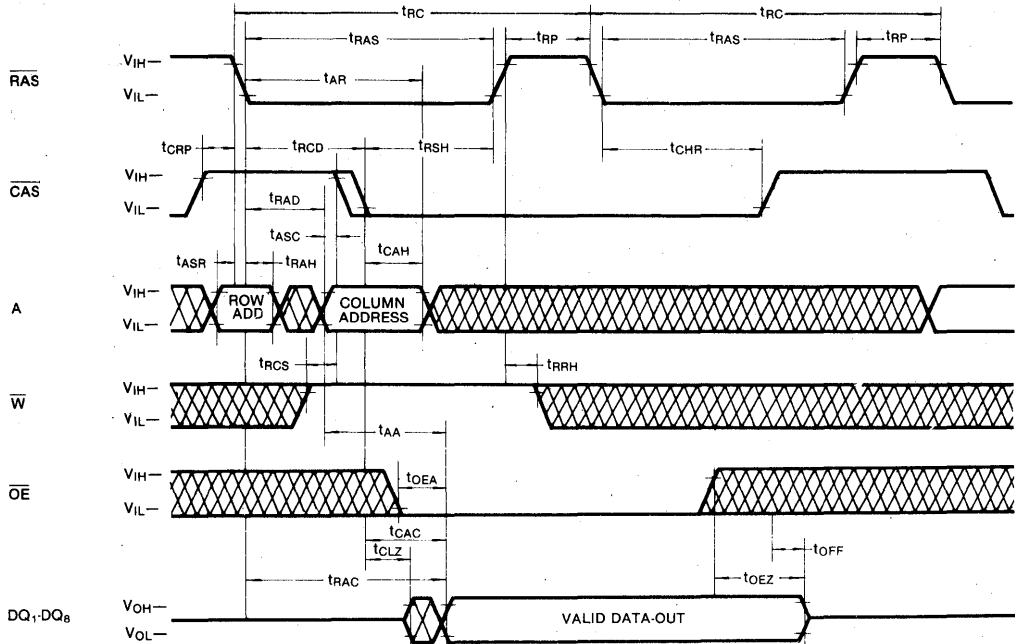
NOTE: \overline{W} , \overline{OE} , A = Don't Care



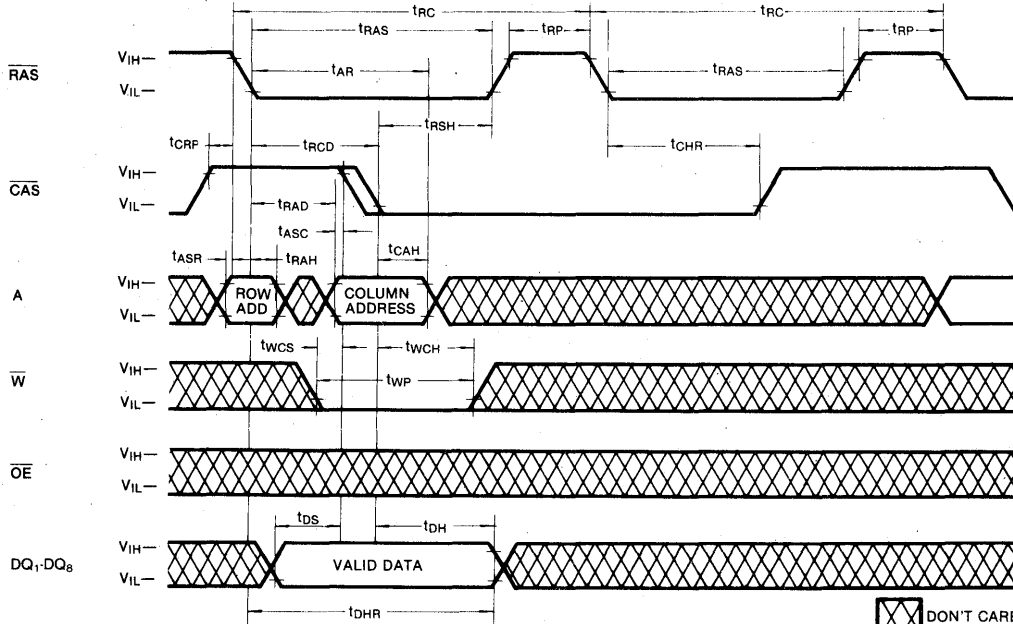
6

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



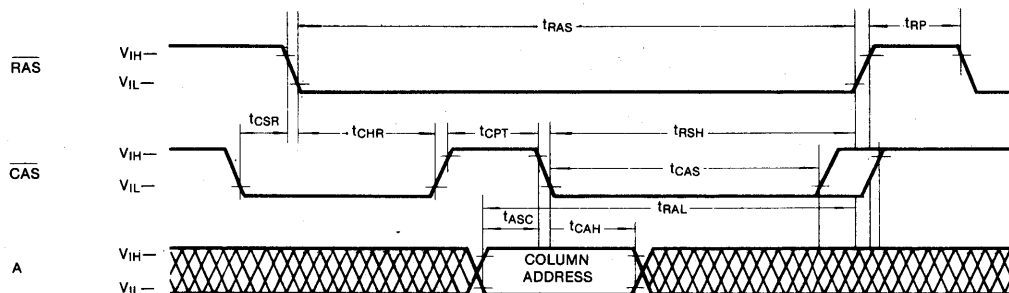
HIDDEN REFRESH CYCLE (WRITE)



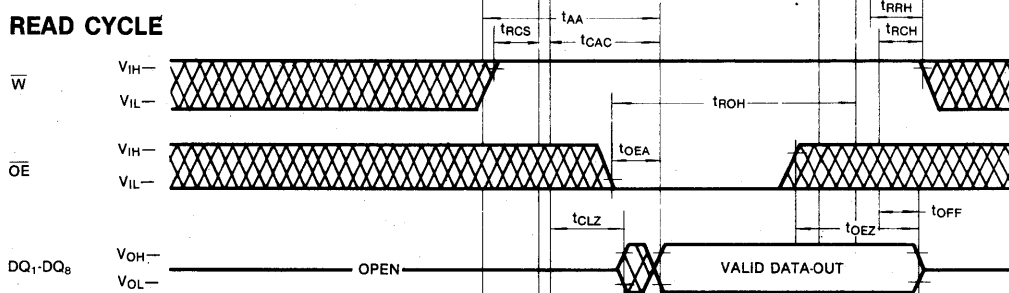
 DON'T CARE

TIMING DIAGRAMS (Continued)

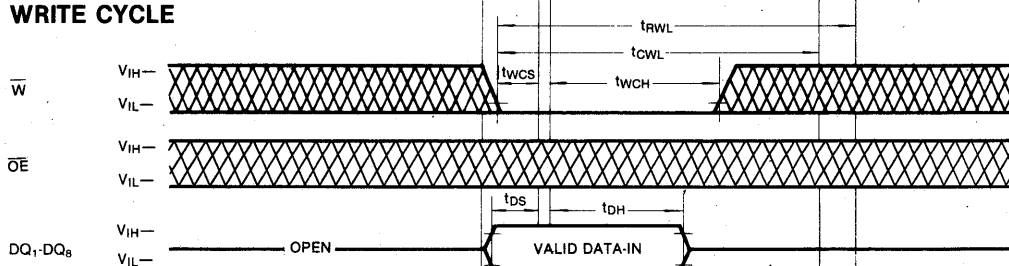
CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE



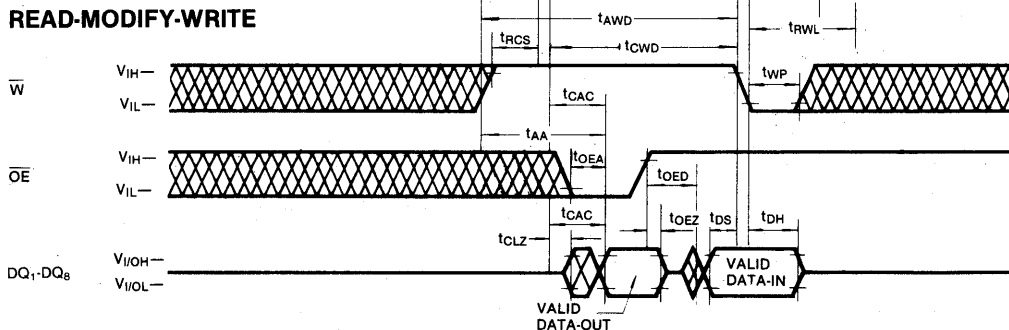
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



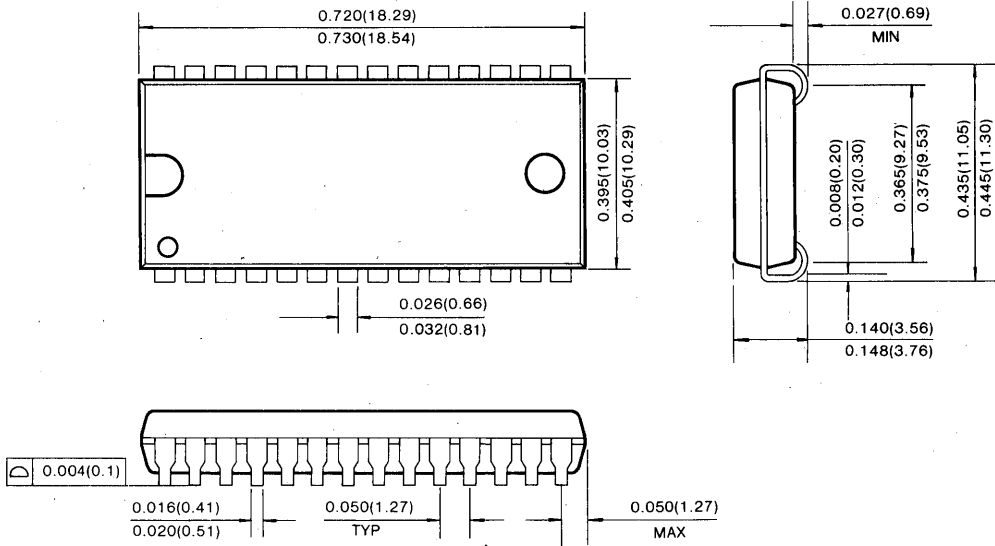
DON'T CARE

6

PACKAGE DIMENSION

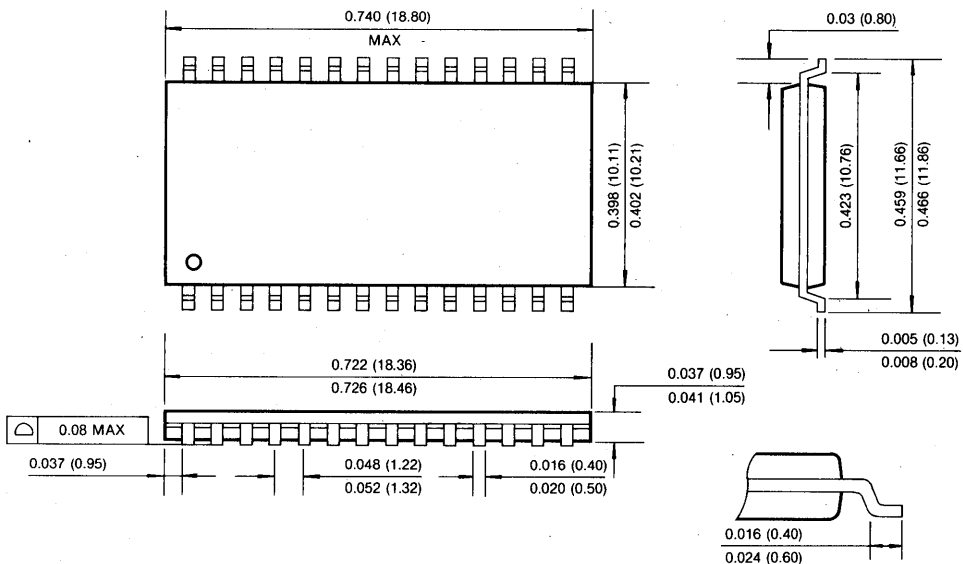
28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

Units: Inches (millimeters)



2M × 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- Performance range:

	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
KM48V2004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48V2004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48V2004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh Operation (LL-ver. only)
- Byte Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- LVTTTL compatible inputs and outputs
- Early write or output enable controlled write
- Single +3.3V ± 0.3V power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

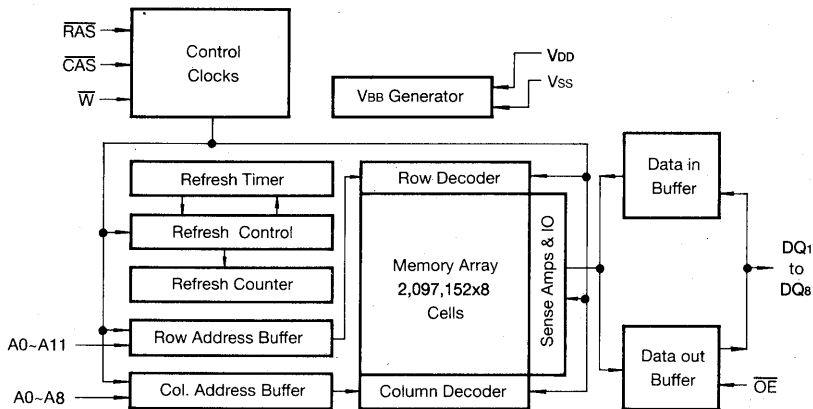
The Samsung KM48V2004A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

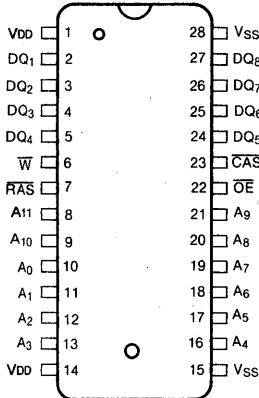
The KM48V2004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



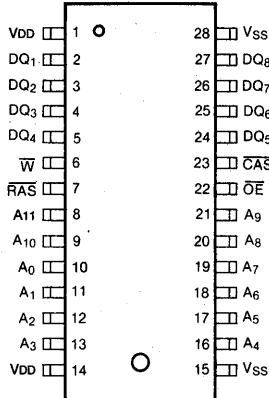
PIN CONFIGURATION (Top Views)

• KM48V2004 AJ/ALJ/ALLJ/ASLJ



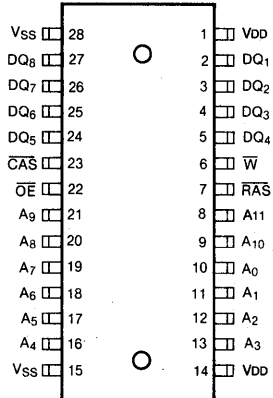
J : 400MIL

• KM48V2004 AT/ALT/ALLT/ASLT



T : 400MIL (Forward)

• KM48V2004 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL (Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-8	Data In/Out
Vss	Ground
\bar{RAS}	Row Address Strobe
\bar{CAS}	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
VDD	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5~ 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8 I _{CC1}	-	80 70 60	mA mA mA
Standby Current (RAS=CAS=W=V _{IH})	KM48V2004A KM48V2004AL KM48V2004ALL KM48V2004ASL I _{CC2}	-	2 1 1 1	mA mA mA mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8 I _{CC3}	-	80 70 60	mA mA mA
Hyper Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8 I _{CC4}	-	90 80 70	mA mA mA
Standby Current (RAS=CAS=W=V _{DD} -0.2V)	KM48V2004A KM48V2004AL KM48V2004ALL KM48V2004ASL I _{CC5}	-	1 300 200 200	mA μA μA μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM48V2004A/AL/ALL/ASL-6 KM48V2004A/AL/ALL/ASL-7 KM48V2004A/AL/ALL/ASL-8 I _{CC6}	-	80 70 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DQ1~DQ8=Don't Care trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), tRAS=tRAS min.~300ns	KM48V2004AL KM48V2004ASL I _{CC7}	-	450 350	μA μA
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=V _{DD} -0.2V or 0.2V DQ1~DQ8=V _{DD} -0.2V, 0.2V or Open	KM48V2004ALL I _{CC8}	-	250	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD}+0.3V$, all other pins not under test=0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS}=V_{IL}$. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ ~A ₁₁)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , W, \overline{OE})	C _{IN2}	-	7	pF
Output Capacitance (DQ ₁ ~DQ ₈)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD}=3.3V ± 0.3V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	3		3		3		ns	3
\overline{OE} to output in Low-Z	t _{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	t _{CEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	t _{RP}	40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	15		20		20		ns	
\overline{CAS} hold time	t _{CSH}	45		50		60		ns	
\overline{CAS} pulse width	t _{CAS}	10	10,000	15	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	45	20	50	20	60	ns	
\overline{RAS} to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	4
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	
Column address to $\overline{\text{RAS}}$ lead time	trAL	30		35		40		ns	6
Read command set-up time	trCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	trCH	0		0		0		ns	
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		ns	9
Write command hold time	twCH	10		15		15		ns	9
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	45		55		60		ns	
Write command pulse width	tWP	10		15		15		ns	6
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tcWL	10		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	twCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tcWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		65		70		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tcPWD	60		70		75		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	trPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tcPT	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tcPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	71		86		96		ns	17
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tcP	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	trASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	trHCP	35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	toED	15		20		20		ns	

6

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	tOEZ	3	15	3	20	3	20	ns	7,14
\overline{OE} command hold time	tOEH	15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	twRP	10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	twRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,15
\overline{OE} to \overline{CAS} hold time	tOCH	5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		ns	
\overline{OE} precharge time	tOEP	5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	trEZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from \overline{W}	twEZ	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	twED	15		20		20		ns	
\overline{RAS} pulse width (LL-ver)	trASS	100		100		100		μ s	16
\overline{RAS} precharge time (LL-ver)	trPS	110		130		150		ns	16
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	115		135		155		ns	
Read-modify-write cycle time	trWC	160		190		210		ns	
Access time from \overline{RAS}	trAC		65		75		85	ns	3,4,11
Access time from \overline{CAS}	tCAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	tCAS	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	20		25		25		ns	
\overline{CAS} hold time	tCSH	50		55		65		ns	
Column address to \overline{RAS} lead time	trAL	35		40		45		ns	
\overline{CAS} to \overline{W} delay time	tcWD	45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	thPC	29		34		39		ns	
Hyper Page read-modify-write cycle time	thPRWC	76		91		101		ns	
\overline{RAS} pulse width (Hyper Page Cycle)	trASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTION

The KM48V2004A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In Test Mode, the 2Mx8 DRAM can be tested as if it were a 1Mx8

DRAM. $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And " $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" or " $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. "Test Mode" function reduces test time (1/2 in cases of N test pattern).

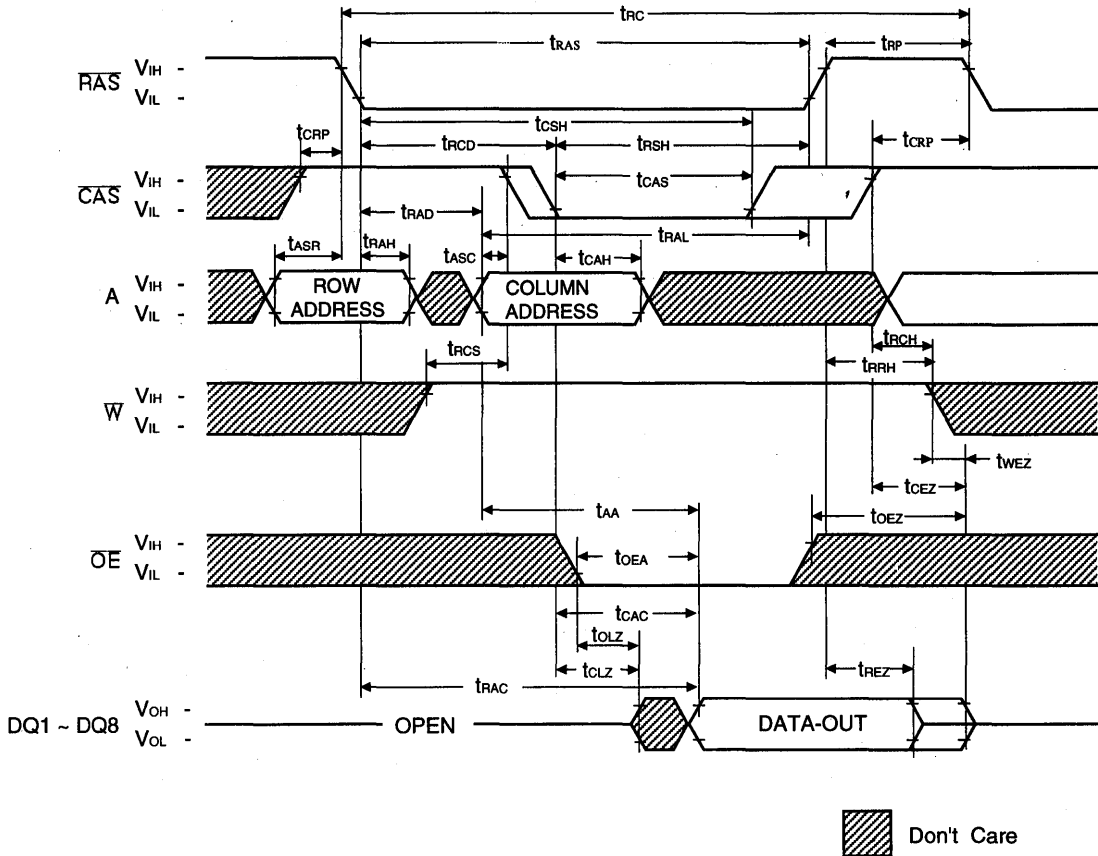
NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
3. Measured with a load equivalent to 1TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. twCS, trWD, tcWD and tAWD are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If twCS \geq twCS(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcWD \geq tcWD(min), trWD \geq trWD(min) and tAWD \geq tAWD(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either trCH or trRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tREZ(max), tCEZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going
17. tASC \geq tCP(min), Assumtn tr=2.0ns

6

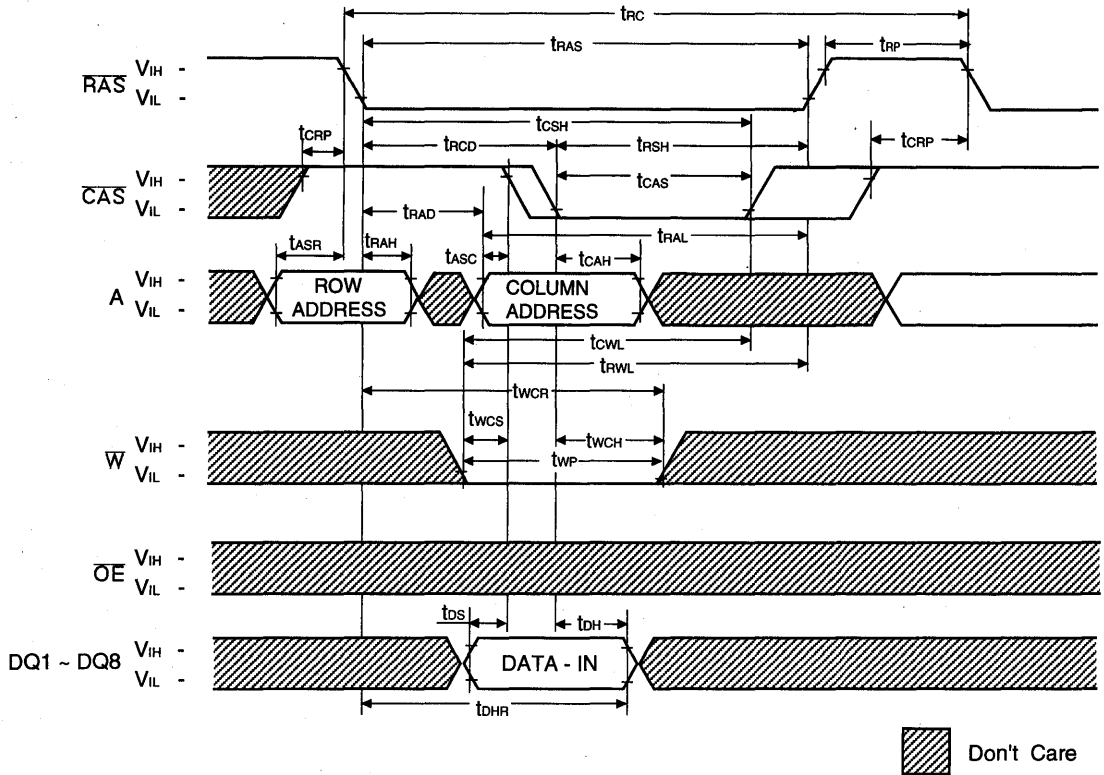
TIMING DIAGRAM

READ CYCLE



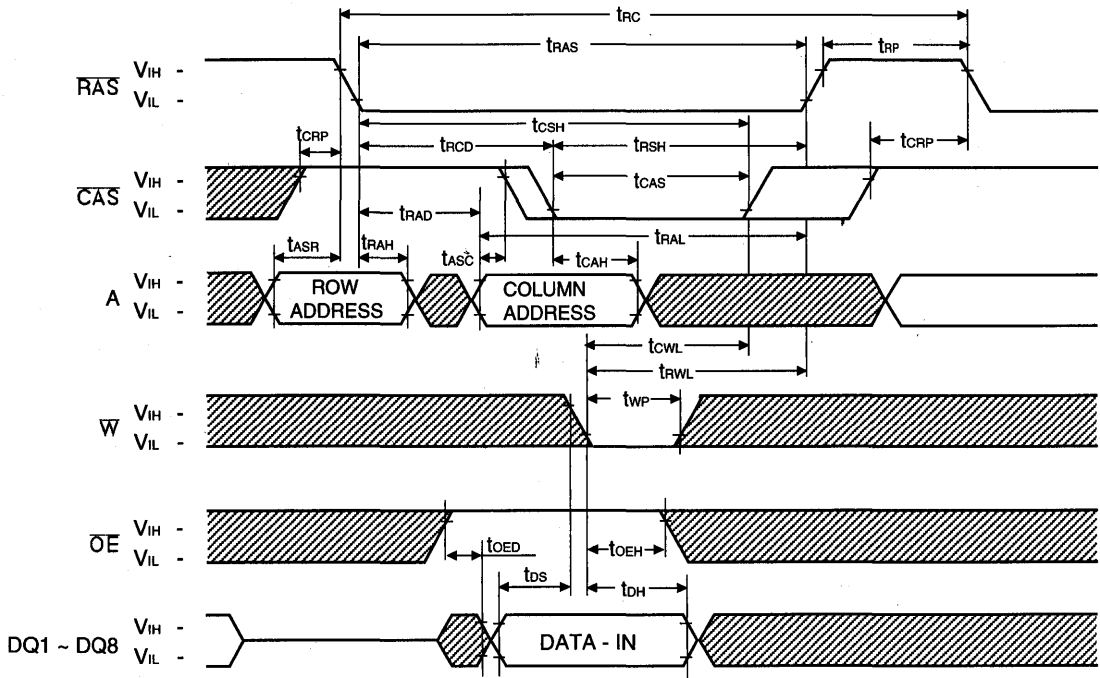
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



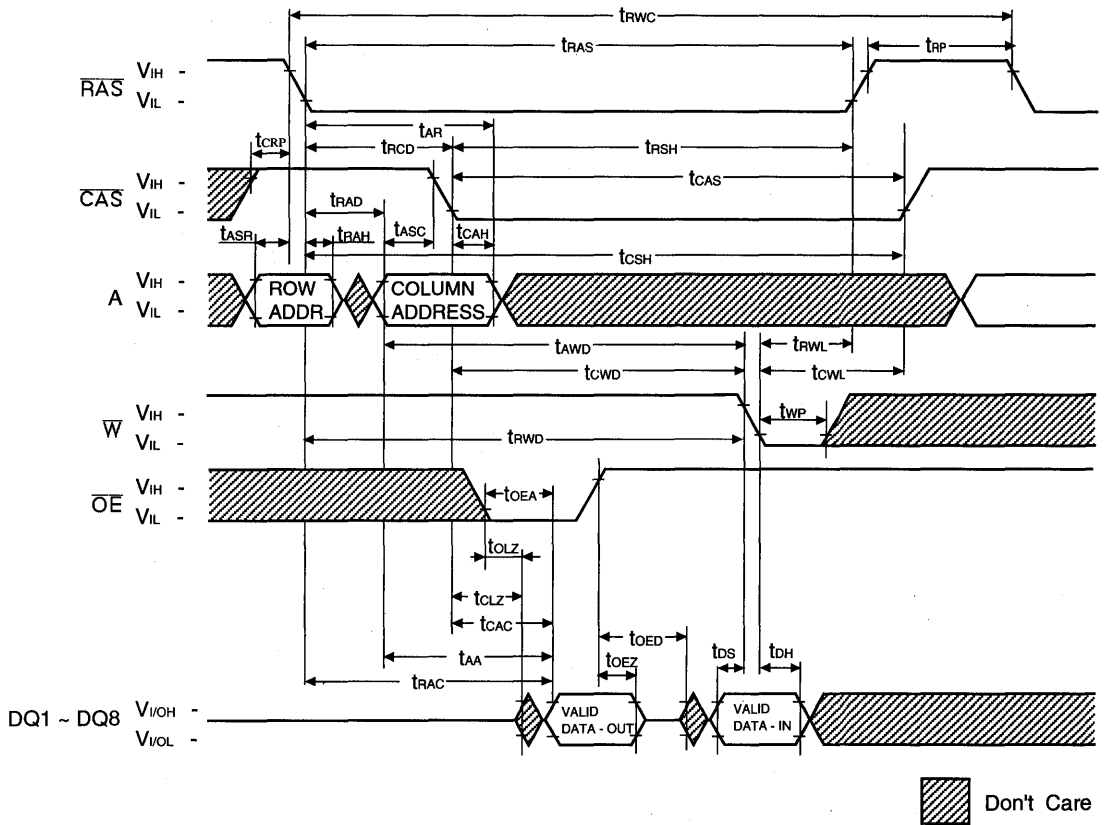
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : D_{out} = OPEN



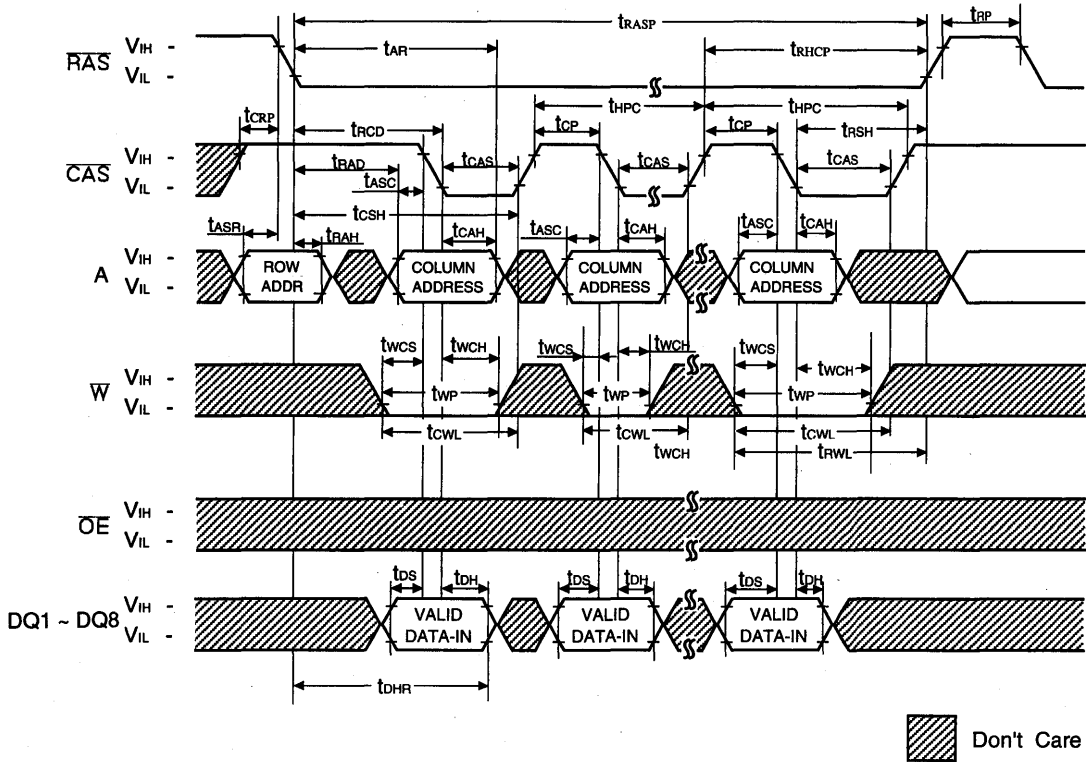
 Don't Care

READ - MODIFY - WRITE CYCLE

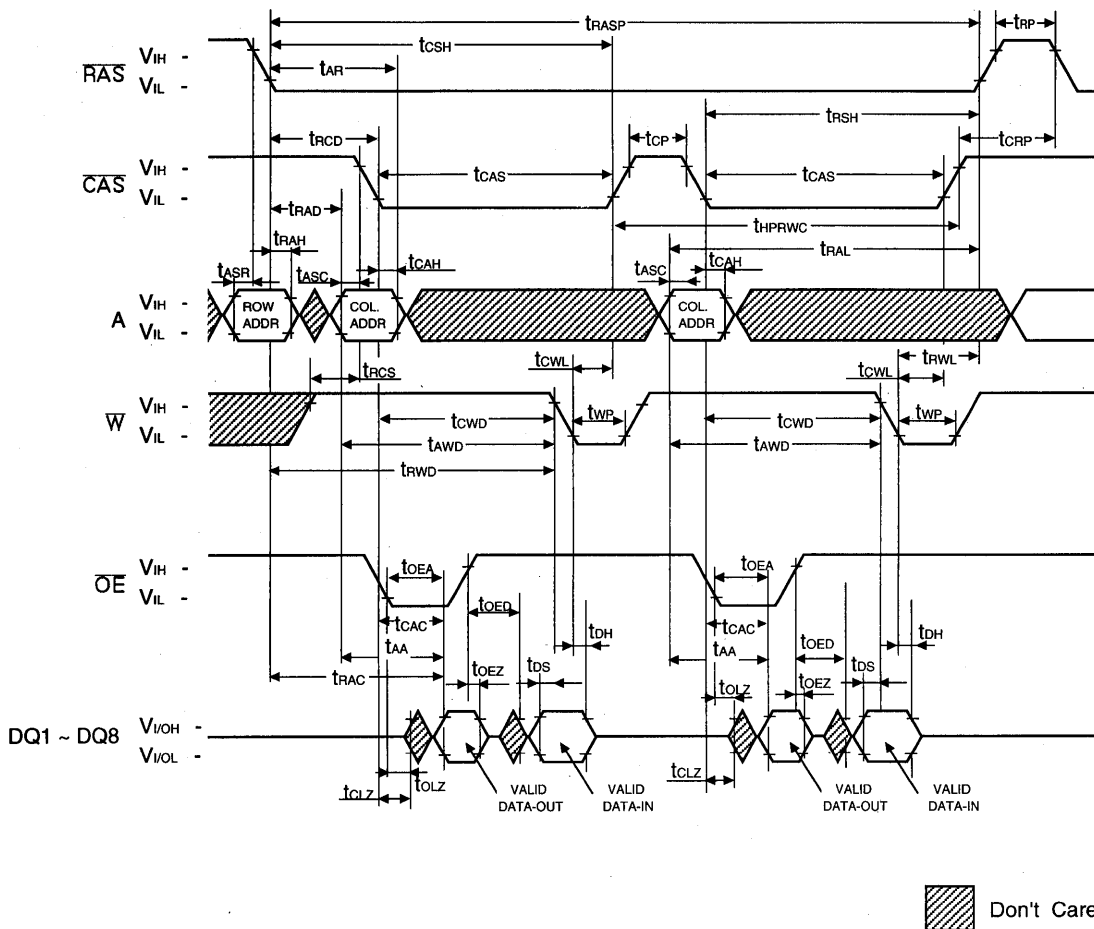


HYPER PAGE WRITE CYCLE (EARLY WRITE)

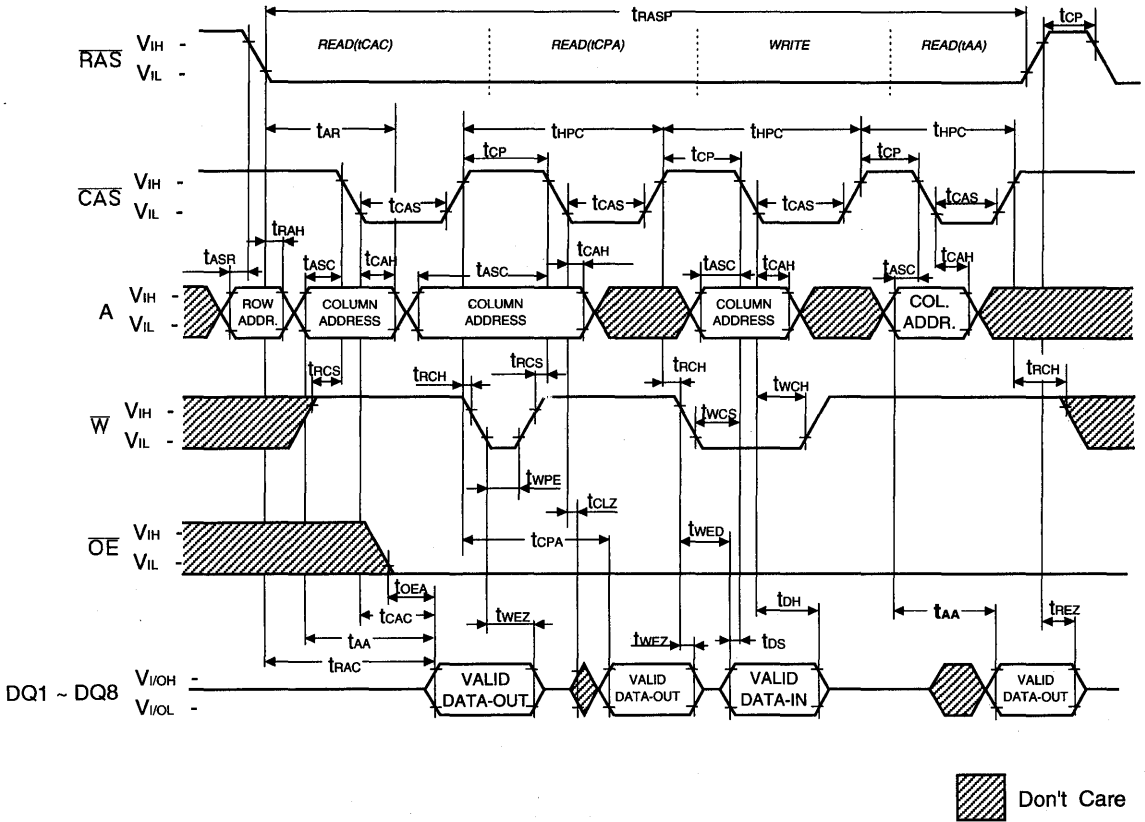
NOTE : Dout = Open



HYPER PAGE READ-MODIFY-WRITE CYCLE



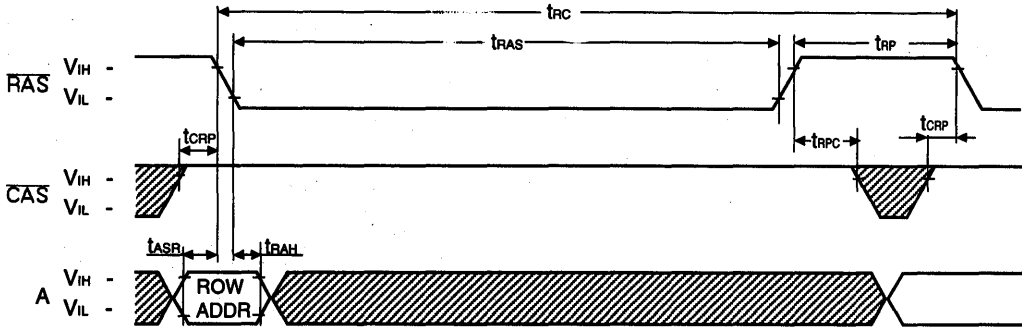
HYPER PAGE READ AND WRITE MIXED CYCLE



6

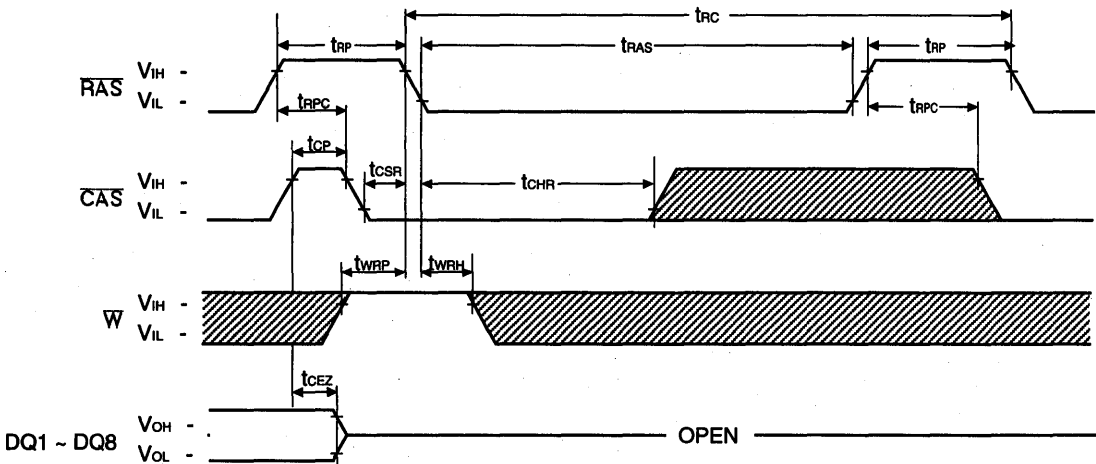
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{in} = Don't care
 D_{out} = Open



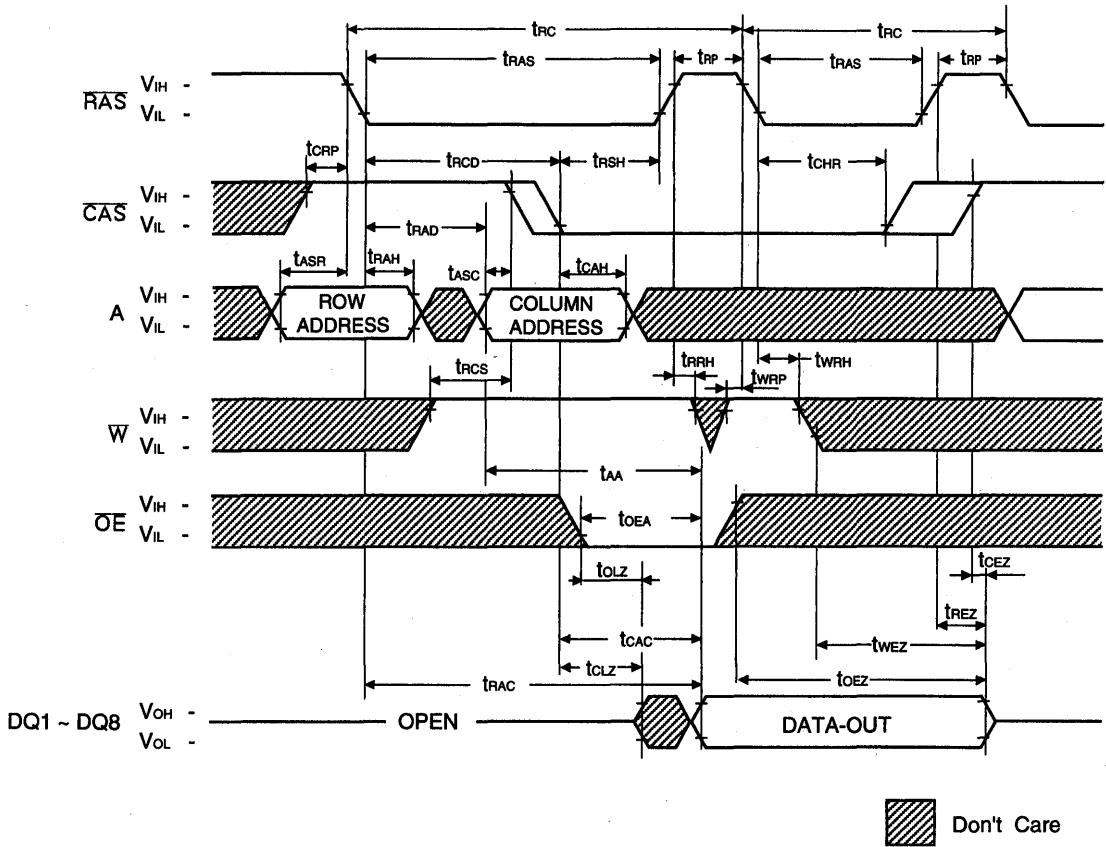
CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care



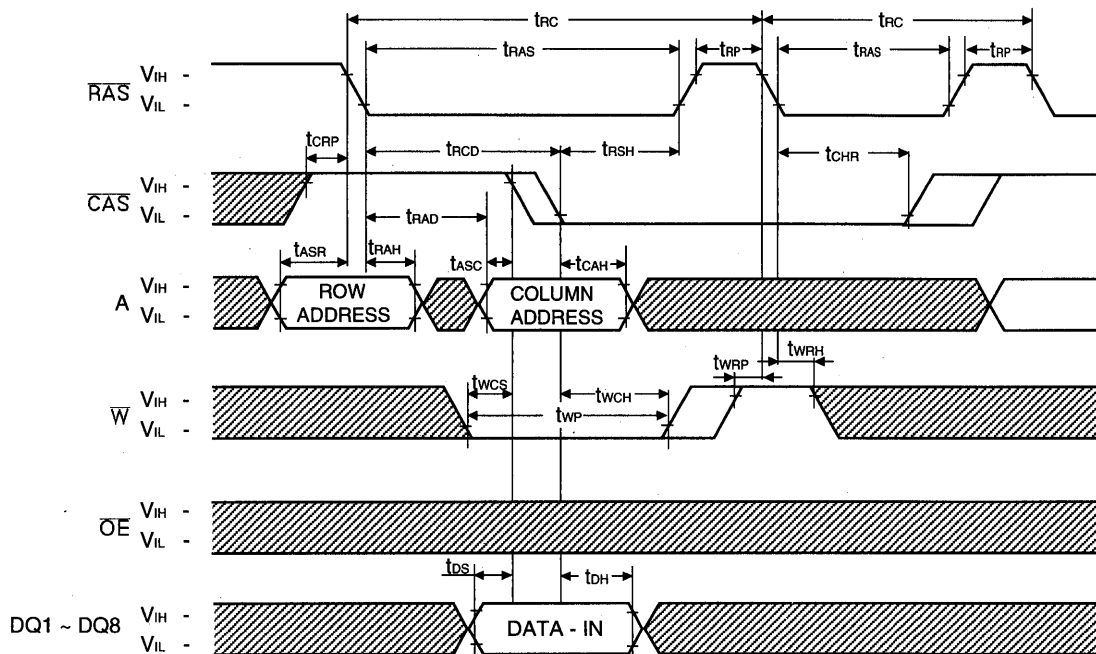
 Don't Care

HIDDEN REFRESH CYCLE (READ)



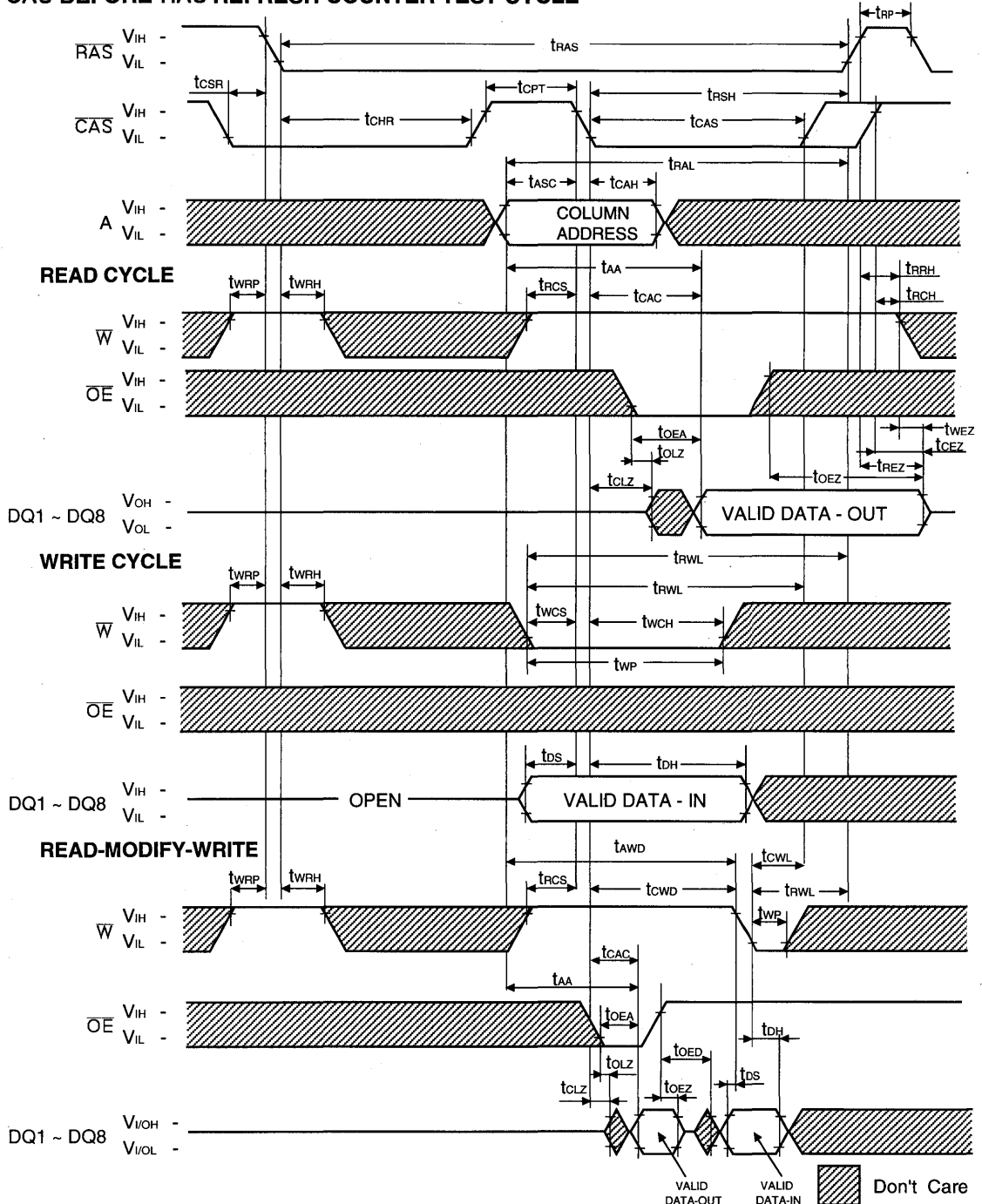
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



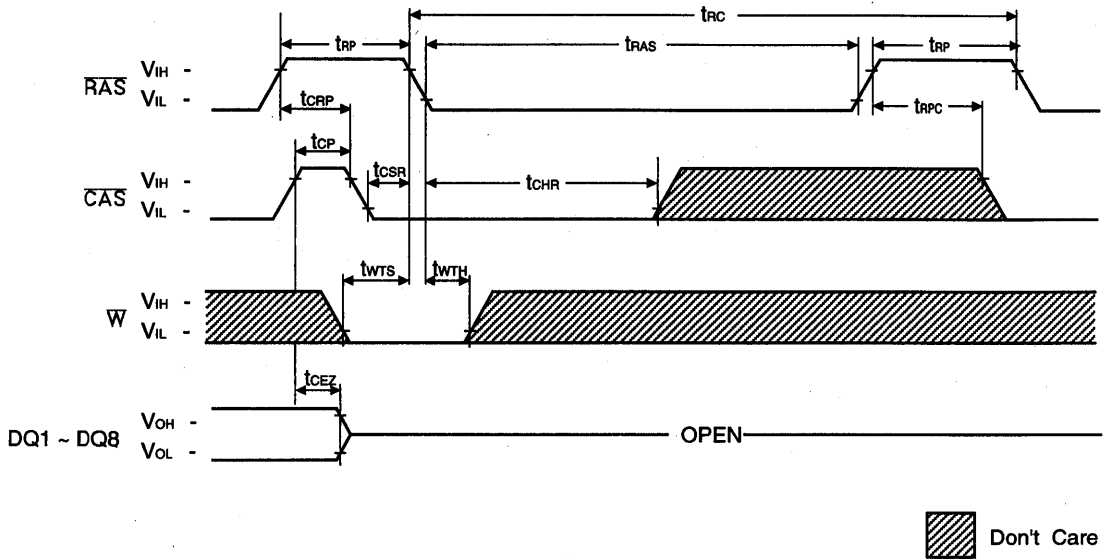
 Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE

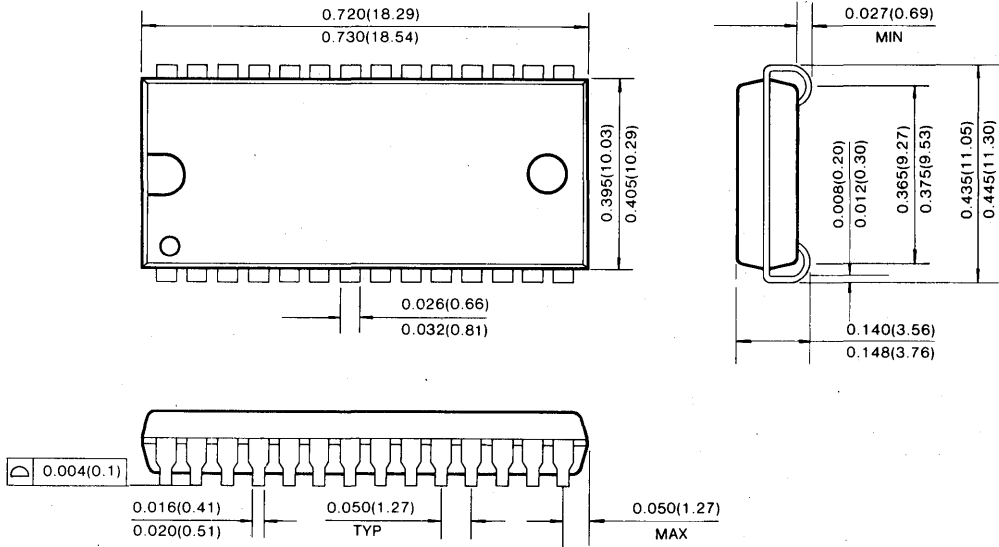
NOTE : $\bar{O}E$, A = Don't Care



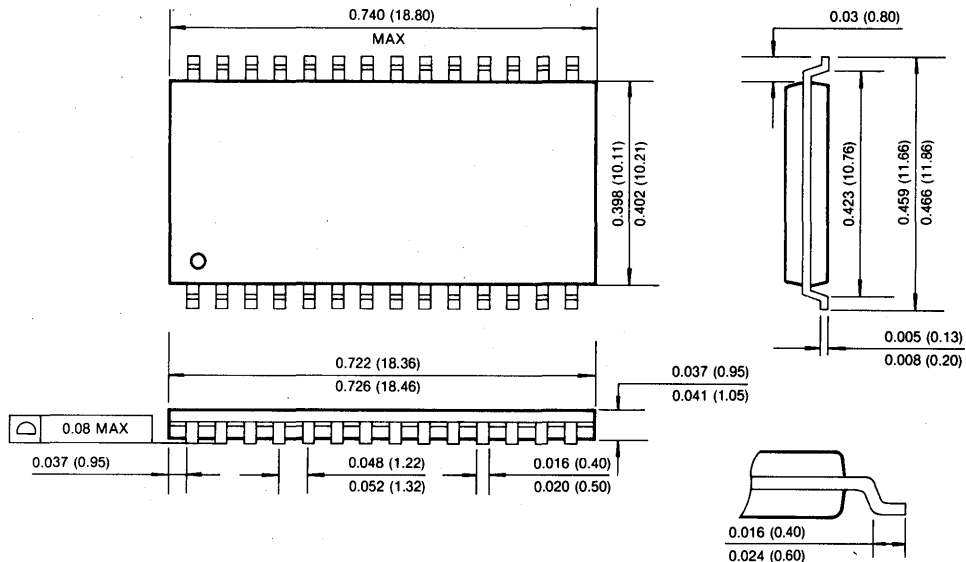
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



2M × 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

- Performance range:

	t _{TRAC}	t _{CAC}	t _{TRC}	t _{HPC}
KM48V2104A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM48V2104A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM48V2104A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh operation (LL-ver. only)
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- LVTTTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+3.3V ± 0.3V power supply
- 2048 cycles/32ms refresh (Normal)
- 2048 cycles/128ms refresh (Low power & Self Ref.)
- 2048 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

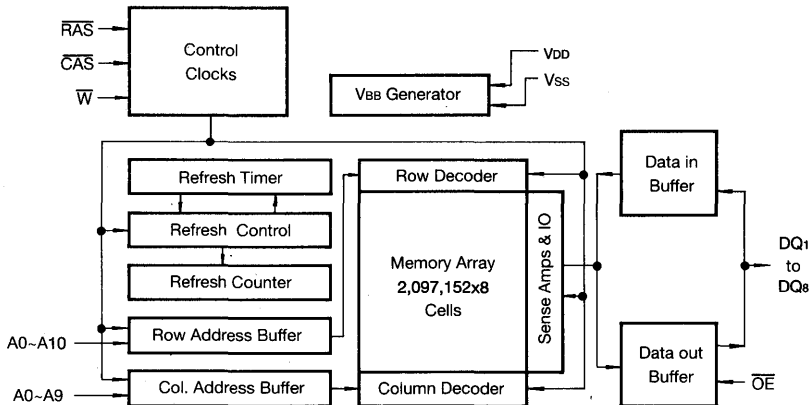
The Samsung KM48V2104A/AL/ALL/ASL is a high speed CMOS 2,097,152 bit × 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V2104A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

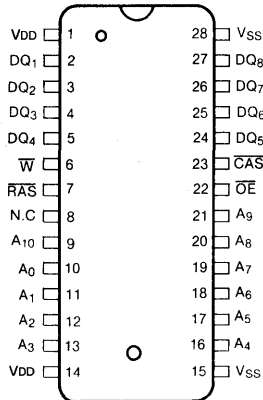
The KM48V2104A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



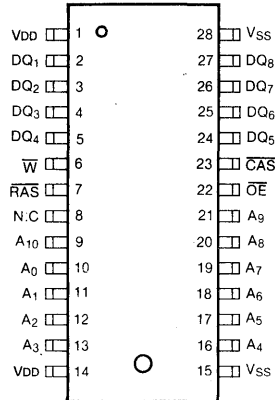
PIN CONFIGURATION (Top Views)

• KM48V2104 AJ/ALJ/ALLJ/ASLJ



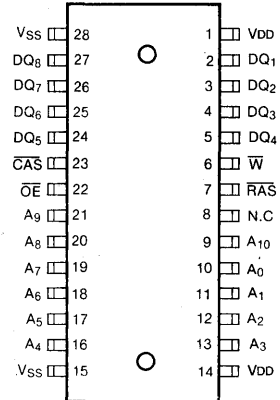
J : 400MIL

• KM48V2104 AT/ALT/ALLT/ASLT



T : 400MIL(Forward)

• KM48V2104 ATR/ALTR/ALLTR/ASLTR



TR : 400MIL(Reverse)

Pin Name	Pin Function
A0-A10	Address Inputs
DQ1-8	Data In/Out
Vss	Ground
\bar{RAS}	Row Address Strobe
\bar{CAS}	Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
VDD	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5~ 4.6	V
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.5~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (R _{AS} and C _{AS} Cycling @trc=min.)	KM48V2104A/AL/ALL/ASL-6 KM48V2104A/AL/ALL/ASL-7 KM48V2104A/AL/ALL/ASL-8 I _{CC1}	-	100 90 80	mA mA mA
Standby Current (R _{AS} =C _{AS} =W=V _{IH})	KM48V2104A KM48V2104AL KM48V2104ALL KM48V2104ASL I _{CC2}	-	2 1 1 1	mA mA mA mA
R _{AS} -Only Refresh Current* (C _{AS} =V _{IH} , R _{AS} Cycling @trc=min.)	KM48V2104A/AL/ALL/ASL-6 KM48V2104A/AL/ALL/ASL-7 KM48V2104A/AL/ALL/ASL-8 I _{CC3}	-	100 90 80	mA mA mA
Hyper Page Mode Current* (R _{AS} =V _{IL} , C _{AS} , Address Cycling @tPC=min.)	KM48V2104A/AL/ALL/ASL-6 KM48V2104A/AL/ALL/ASL-7 KM48V2104A/AL/ALL/ASL-8 I _{CC4}	-	100 90 80	mA mA mA
Standby Current (R _{AS} =C _{AS} =W=V _{DD} -0.2V)	KM48V2104A KM48V2104AL KM48V2104ALL KM48V2104ASL I _{CC5}	-	1 300 200 200	mA μA μA μA
C _{AS} -Before-R _{AS} Refresh Current* (R _{AS} and C _{AS} Cycling @trc=min.)	KM48V2104A/AL/ALL/ASL-6 KM48V2104A/AL/ALL/ASL-7 KM48V2104A/AL/ALL/ASL-8 I _{CC6}	-	100 90 80	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V, Input Low Voltage (V _{IL})=0.2V, C _{AS} =C _{AS} -Before-R _{AS} Cycling or 0.2V, DQ1~DQ8=Don't Care, trc=62.5μs(L-Ver.) 125μs(SL-Ver.), tRAS=tRAS min.~300ns	KM48V2104AL KM48V2104ASL I _{CC7}	-	400 300	μA μA
Self Refresh Current R _{AS} =C _{AS} =0.2V W=OE=A0-A10=V _{DD} -0.2V or 0.2V DQ1~DQ8=V _{DD} -0.2V, 0.2V or Open	KM48V2104ALL I _{CC8}	-	250	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test = 0 volts.)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} = -2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} = 2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A = 25°C, V_{DD} = 3.3V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A10)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , W, \overline{OE})	C _{IN2}	-	7	pF
Output Capacitance (DQ1-DQ8)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD} = 3.3V ± 0.3V, See notes 1,2)

Test Condition : V_{ih}/V_{il} = 2.0V/0.8V, V_{oh}/V_{ol} = 2.0V/0.8V, Output Loading C_L = 100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		15		20		20	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	3		3		3		ns	3
\overline{OE} to output in Low-Z	t _{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	t _{OEZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t _T	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	t _{RP}	40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	15		20		20		ns	
\overline{CAS} hold time	t _{CSH}	45		50		60		ns	
\overline{CAS} pulse width	t _{CAS}	10	10,000	15	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	45	20	50	20	60	ns	
\overline{RAS} to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	4
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	t _{ASR}	0		0		0		ns	
Row address hold time	t _{RAH}	10		10		10		ns	
Column address set-up time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	t _{AR}	45		55		60		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	30		35		40		ns	6
Read command set-up time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		0		ns	9
Write command hold time	t _{WCH}	10		15		15		ns	9
Write command hold time referenced to $\overline{\text{RAS}}$	t _{WCR}	45		55		60		ns	
Write command pulse width	t _{WP}	10		15		15		ns	6
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	10		15		20		ns	
Data set-up time	t _{DS}	0		0		0		ns	10
Data hold time	t _{DH}	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	t _{DHR}	45		55		60		ns	6
Refresh period (Normal)	t _{REF}		32		32		32	ms	
Refresh period (Low power & Self Ref.)	t _{REF}		128		128		128	ms	
Refresh period (Super Low power)	t _{REF}		256		256		256	ms	
Write command set-up time	t _{WCS}	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	t _{CWD}	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	t _{RWD}	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	t _{AWD}	55		65		70		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	t _{CPWD}	60		70		75		ns	8
$\overline{\text{CAS}}$ set-up time (CAS-before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	10		10		10		ns	
$\overline{\text{CAS}}$ hold time (CAS-before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	t _{CPT}	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}		35		40		45	ns	3
Hyper Page cycle time	t _{HPC}	24		29		34		ns	17
Hyper Page read-modify-write cycle time	t _{HPRWC}	71		86		96		ns	17
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	t _{CP}	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	t _{RASP}	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t _{RHCP}	35		40		45		ns	
$\overline{\text{OE}}$ access time	t _{OEA}		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	t _{OED}	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	toEZ	3	15	3	20	3	20	ns	7,14
\overline{OE} command hold time	toEH	15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{C} - \overline{B} - \overline{R} refresh)	twRP	10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} - \overline{B} - \overline{R} refresh)	twRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,15
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		ns	
\overline{W} pulse width (Hyper Page Cycle)	twPE	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	treZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from \overline{W}	tweZ	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	twED	15		20		20		ns	
\overline{RAS} pulse width (LL-ver)	trASS	100		100		100		μ s	16
\overline{RAS} precharge time (LL-ver)	trPS	110		130		150		ns	16
\overline{CAS} hold time (LL-ver)	tCHS	-50		-50		-50		ns	16

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	115		135		155		ns	
Read-modify-write cycle time	trWC	160		190		210		ns	
Access time from \overline{RAS}	trAC		65		75		85	ns	3,4,11
Access time from \overline{CAS}	trAC		20		25		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	trCAS	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	20		25		25		ns	
\overline{CAS} hold time	trSH	50		55		65		ns	
Column address to \overline{RAS} lead time	trAL	35		40		45		ns	
\overline{CAS} to \overline{W} delay time	trWD	45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	60		70		75		ns	8
Hyper Page cycle time	trHPC	29		34		39		ns	
Hyper Page read-modify-write cycle time	trPRWC	76		91		101		ns	
\overline{RAS} pulse width (Hyper Page Cycle)	trASP	65	200,000	75	200,000	85	200,000	ns	

TEST MODE CYCLE (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		40		45		50	ns	3
$\overline{\text{OE}}$ access time	tOEA		20		25		25	ns	
$\overline{\text{OE}}$ to data delay	tOED	20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTION

The KM48V2104A/AL/ALL/ASL is the CMOS DRAM organized 2,097,152 words by 8 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In Test Mode", the 2Mx8 DRAM can be tested, as if it were a 1Mx8

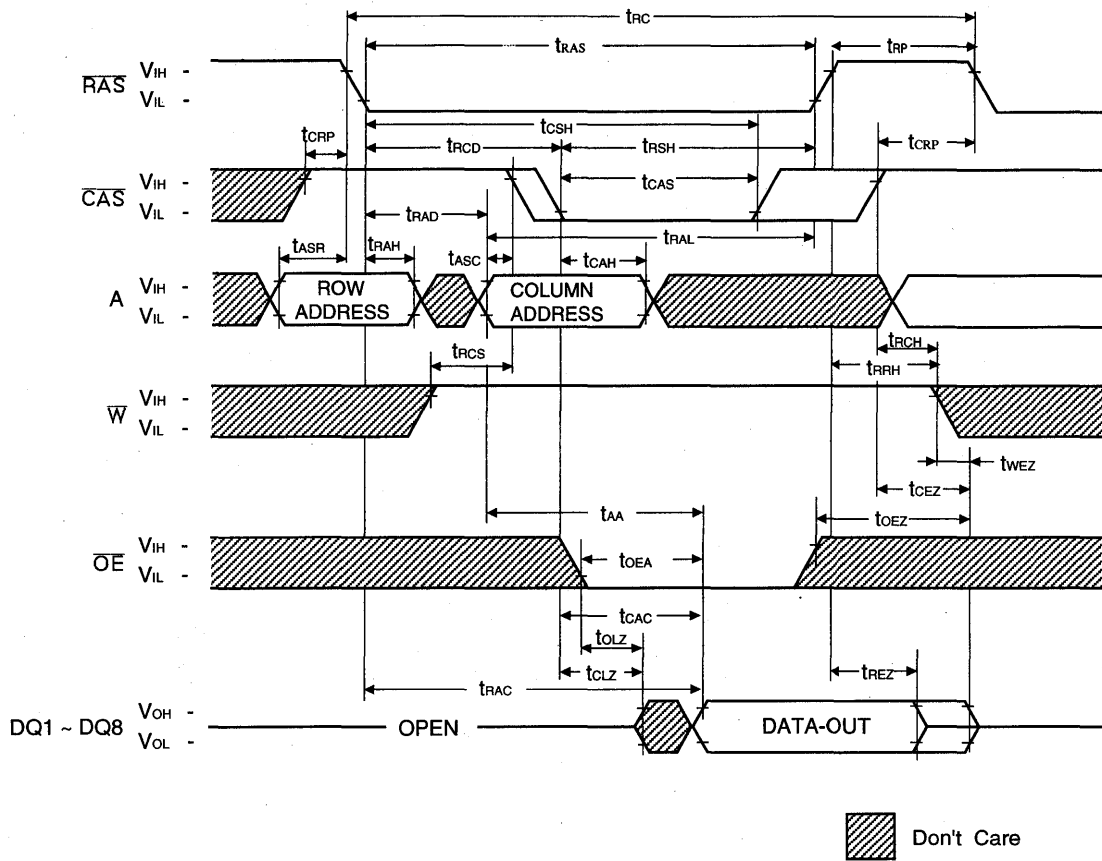
DRAM. $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And " $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" or "RAS Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. "Test Mode" function reduces test time (1/2 in cases of N test pattern).

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
3. Measured with a load equivalent to 1TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD \geq tRCD (max).
6. tAR, tWCR, tDHR are referenced to tRAD(max).
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to VOH or VOL.
8. twcs, trwd, tcwd and tawd are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If twcs \geq twcs(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If tcwd \geq tcwd(min), trwd \geq trwd(min) and tawd \geq tawd(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the tRAD(max) limit insures that tRAC(max) can be met. tRAD(max) is specified as a reference point only. If tRAD is greater than the specified tRAD(max) limit, then access time is controlled by tAA.
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of tRAC, tAA, tCAC is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14. tREZ(max), tCEZ(max), tWEZ(max) and tOEZ(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 2048 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
16. If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going
17. tASC \geq tOPmin, Assumnn tT=2.0ns

TIMING DIAGRAM

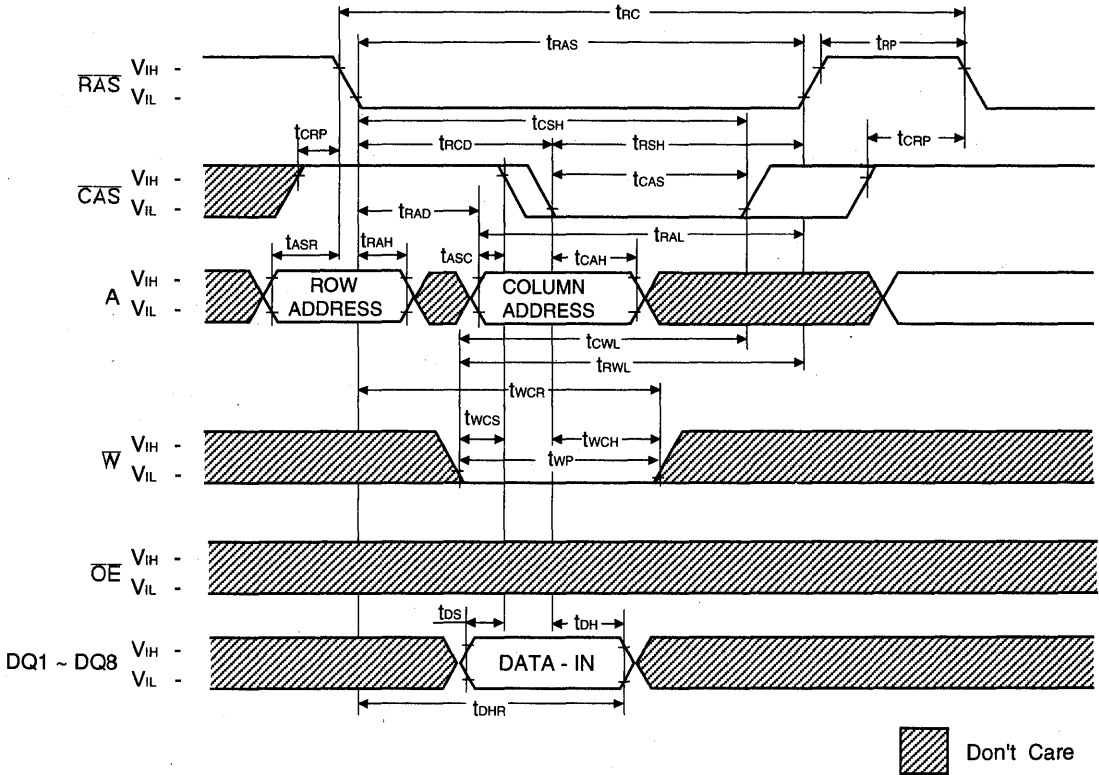
READ CYCLE



6

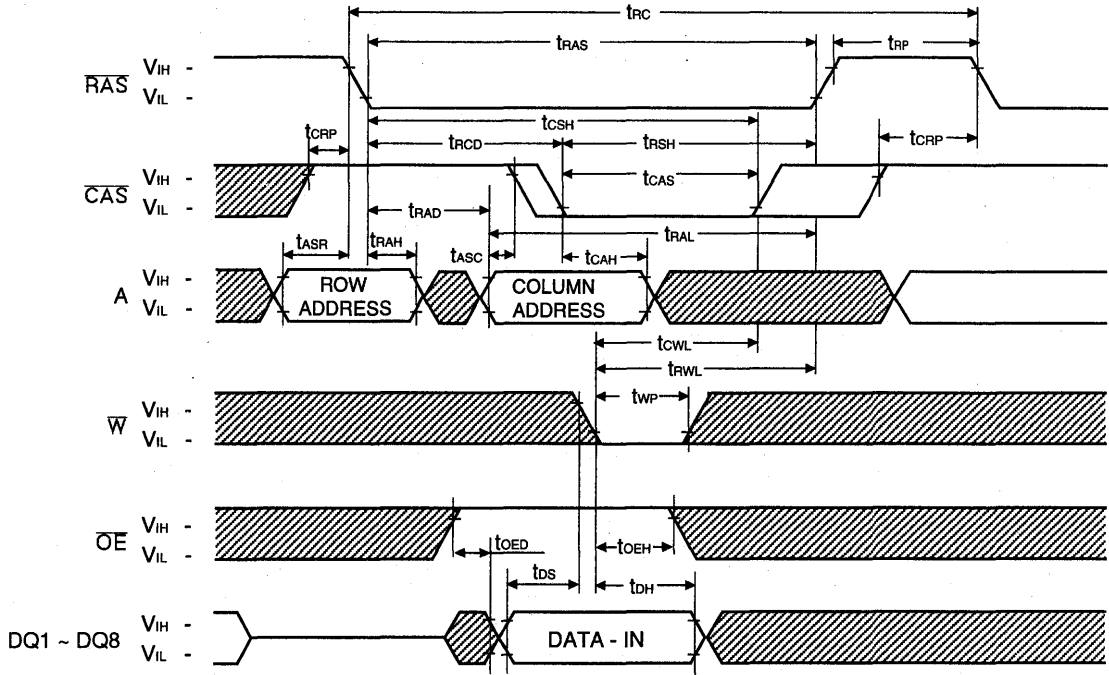
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



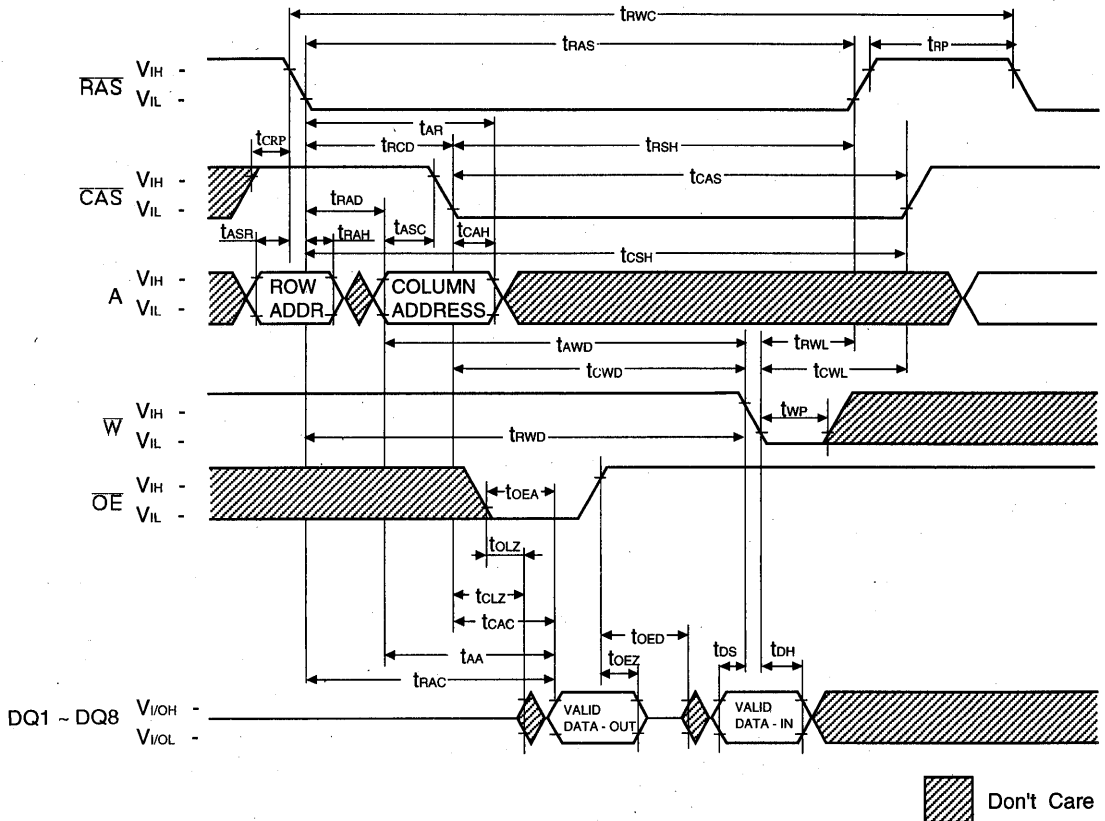
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

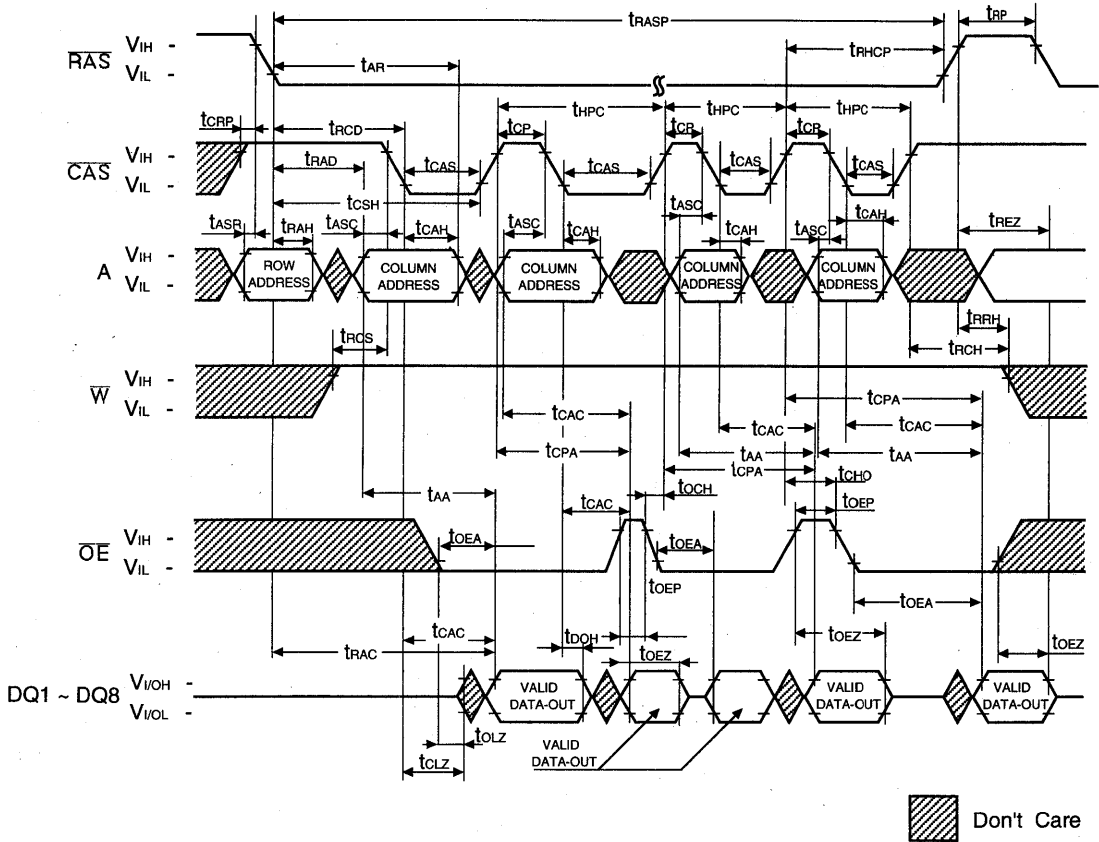


 Don't Care

READ - MODIFY - WRITE CYCLE



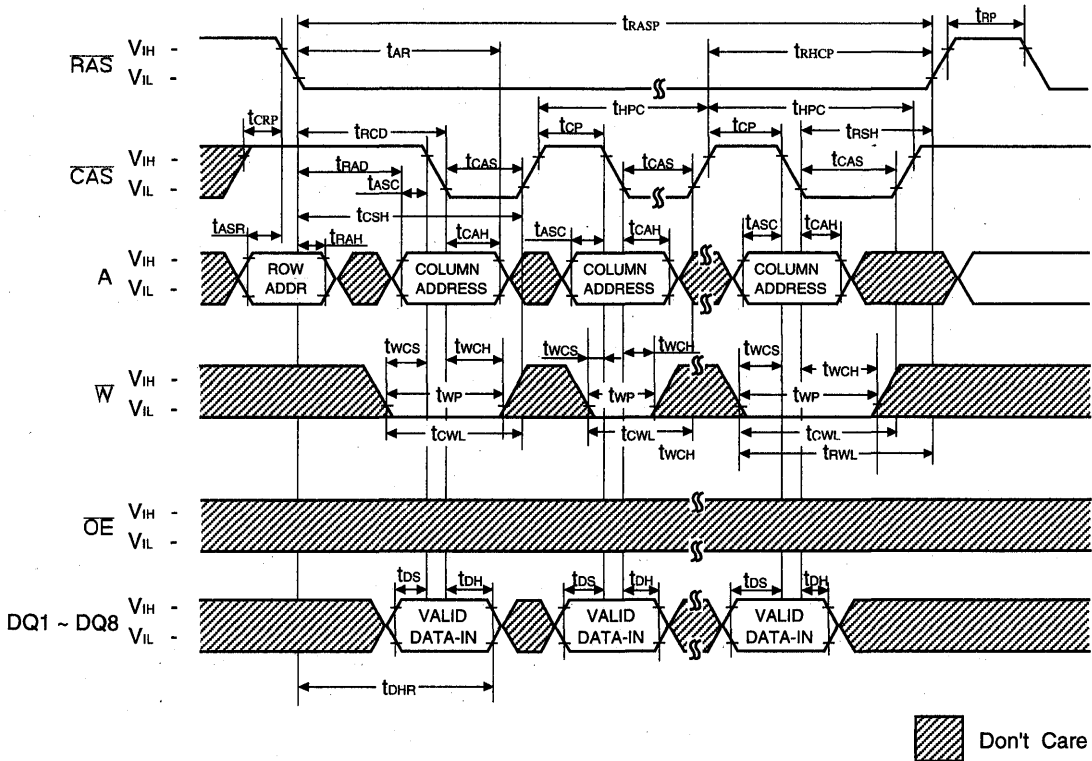
HYPER PAGE READ CYCLE



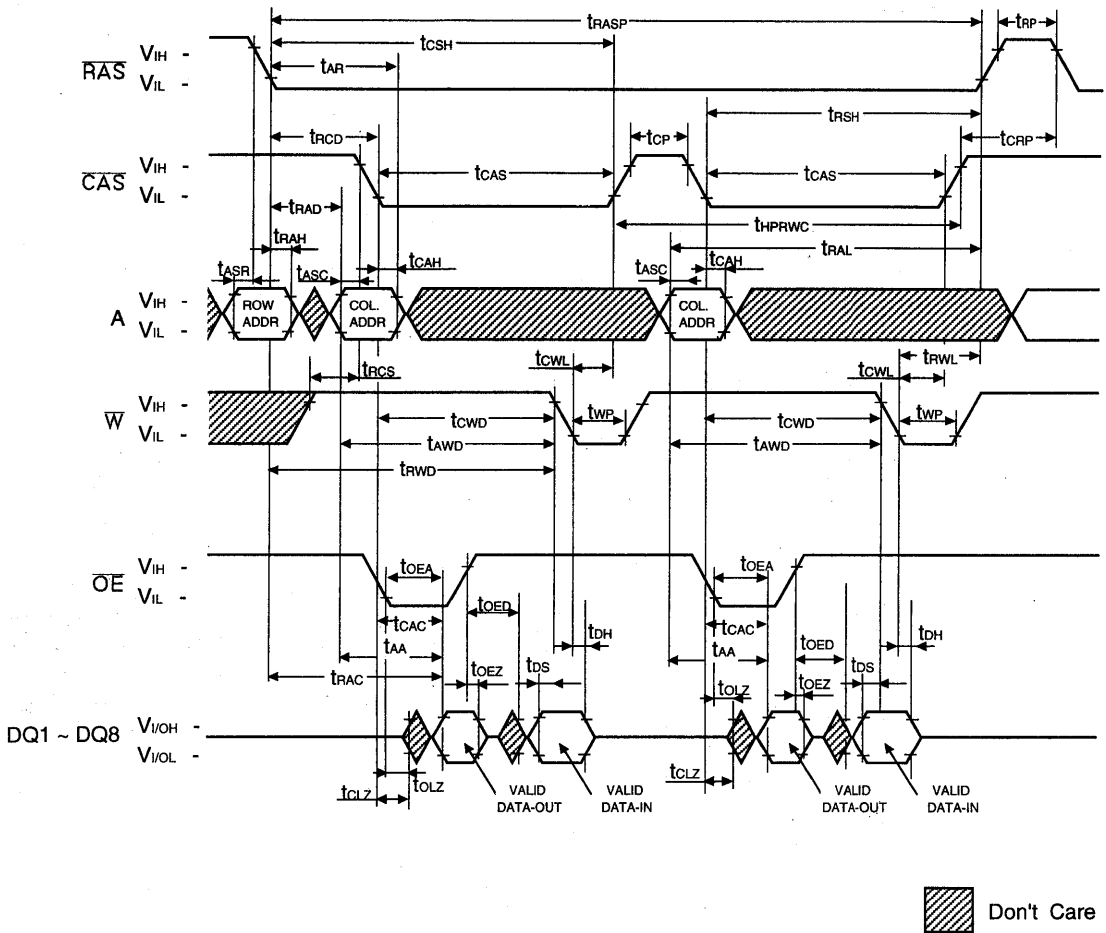
6

HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = Open

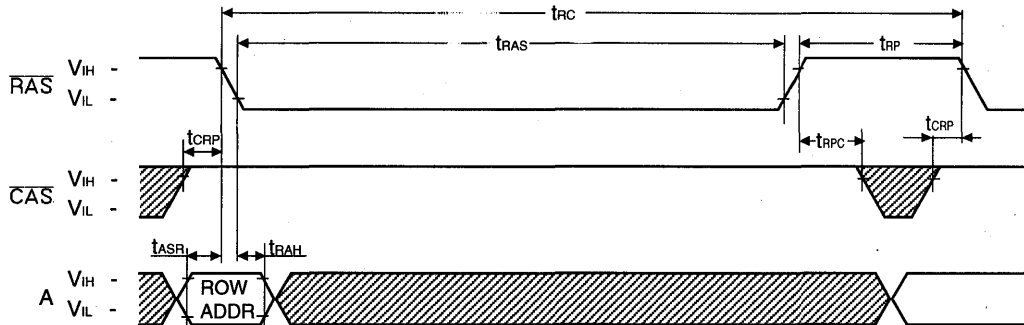


HYPER PAGE READ-MODIFY-WRITE CYCLE



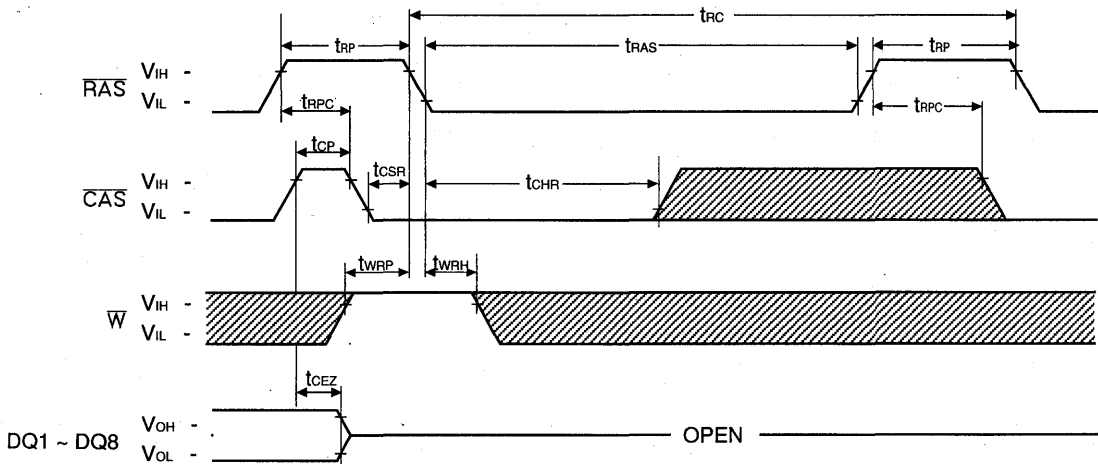
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



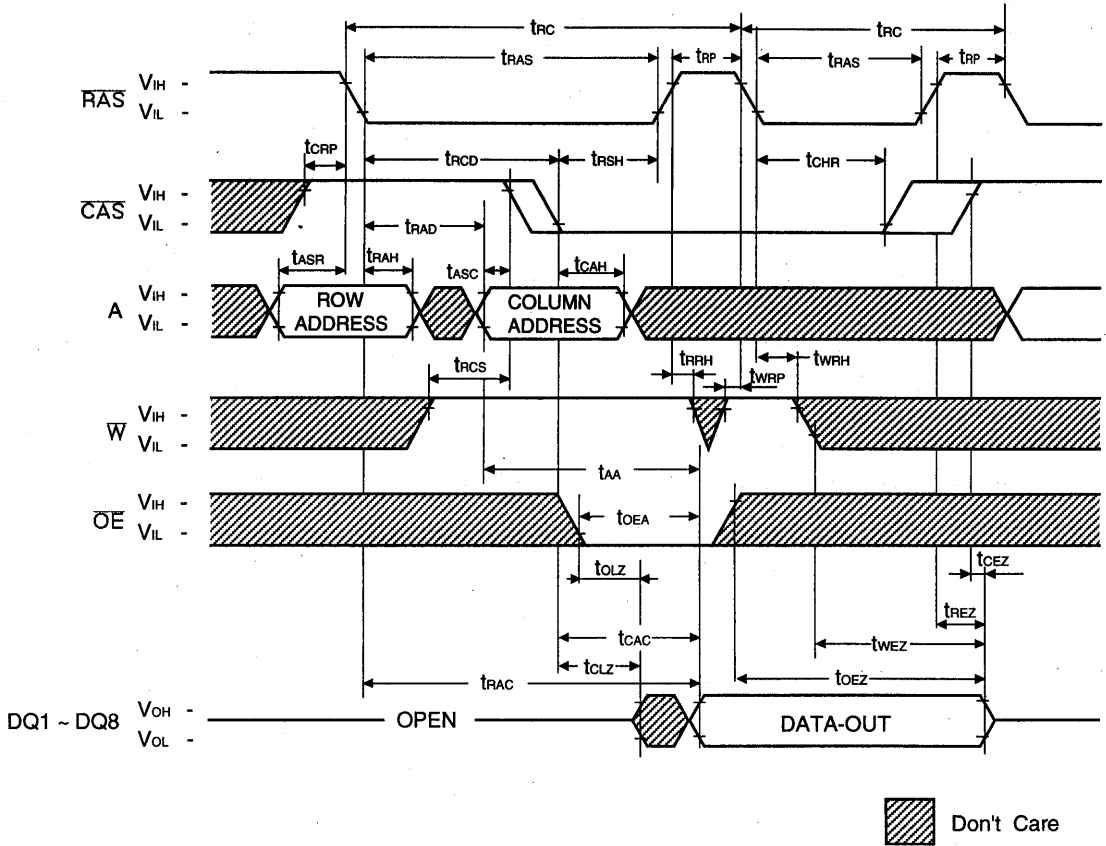
\bar{CAS} -BEFORE- \bar{RAS} REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care



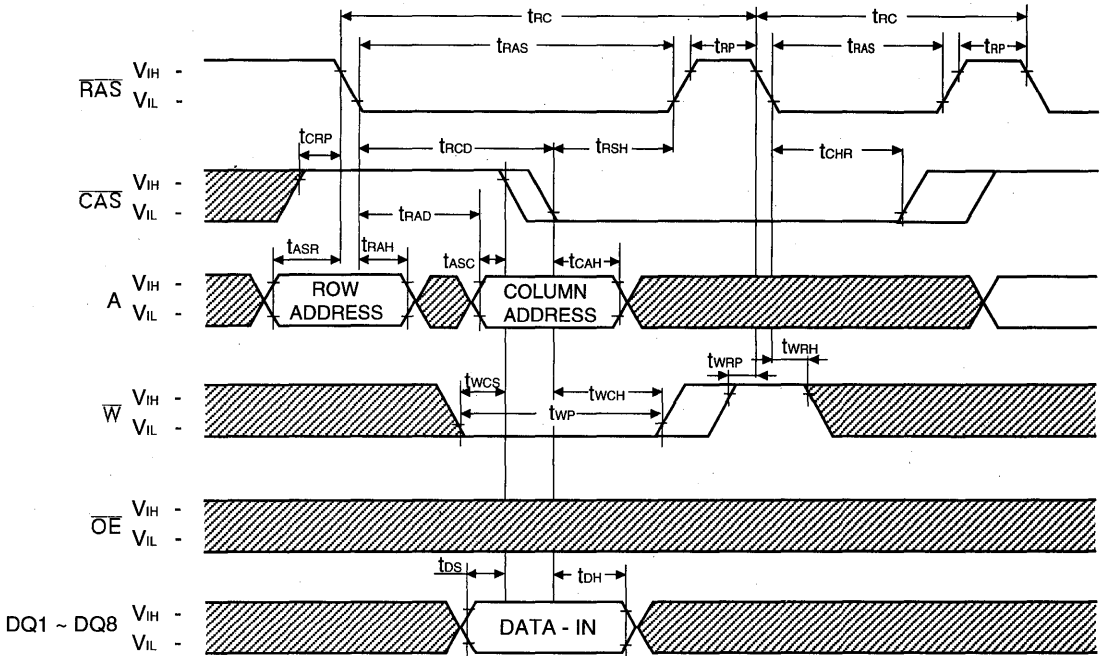
 Don't Care

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

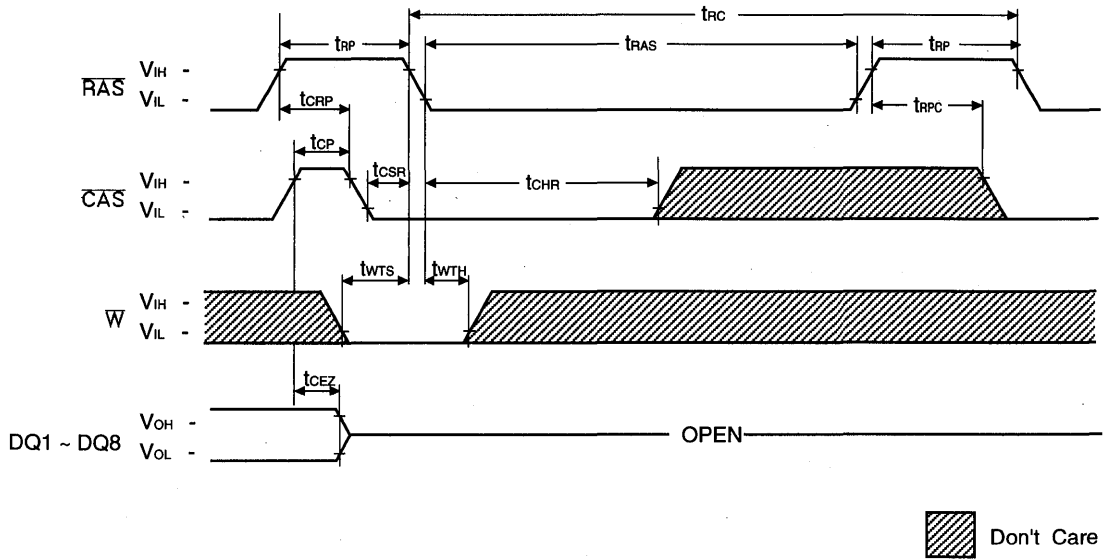
NOTE : D_{OUT} = OPEN



 Don't Care

TEST MODE IN CYCLE

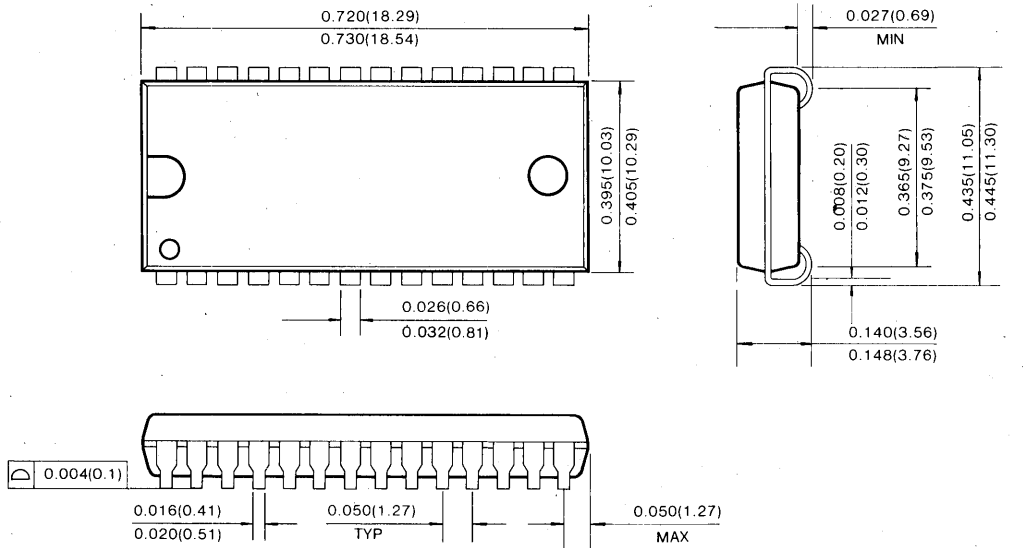
NOTE : \overline{OE} , A = Don't Care



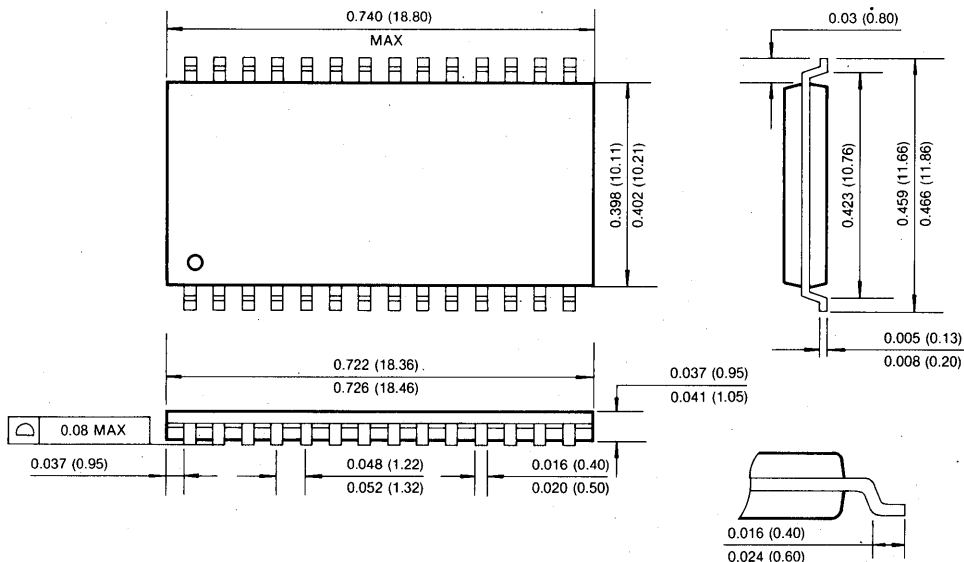
PACKAGE DIMENSION

28-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



28-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

- Performance range:

	trAC	tCAC	trC
KM416C1000A-6/A-L6/A-F6	60ns	15ns	110ns
KM416C1000A-7/A-L7/A-F7	70ns	20ns	130ns
KM416C1000A-8/A-L8/A-F8	80ns	20ns	150ns

- Fast Page Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +5V ± 10% power supply
- Refresh Cycle
 - 4096 cycle/64ms (Normal)
 - 4096 cycle/128ms (L-version)
 - 4096 cycle/128ms (F-version)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP II packages

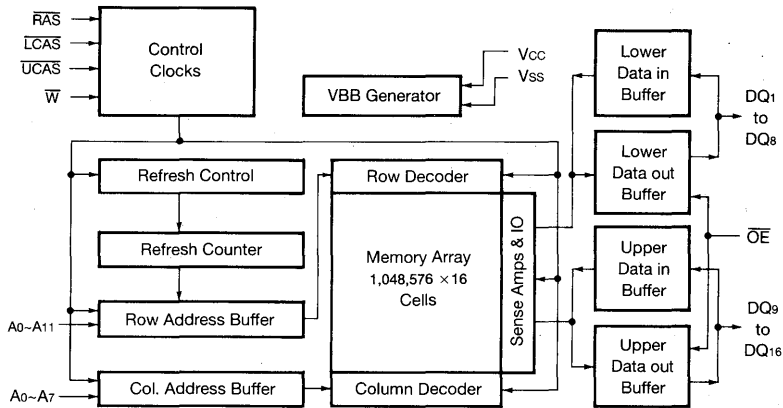
GENERAL DESCRIPTION

The Samsung KM416C1000A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416C1000A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

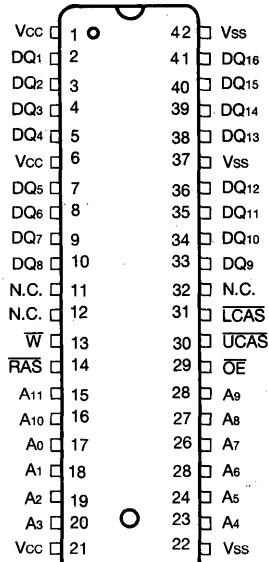
The KM416C1000A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



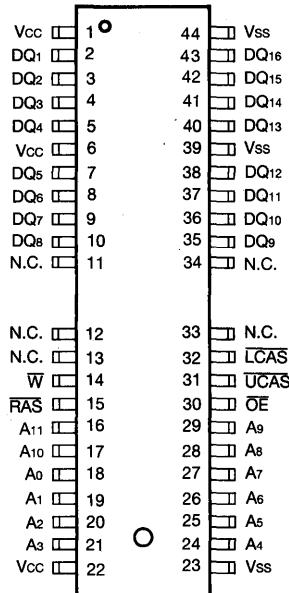
PIN CONFIGURATION (Top Views)

• KM416C1000AJ



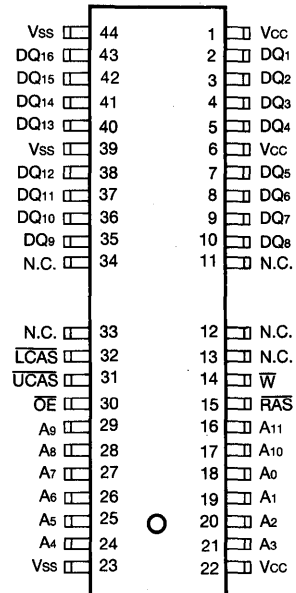
(SOJ)

• KM416C1000AT



(TSOP(II)-Forward)

• KM416C1000AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
\bar{RAS}	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
\bar{W}	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 ~ +7	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 ~ +7	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS, UCAS or LCAS, Address Cycling @trc=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I _{CC1}	-	100 90 80 mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{IH})	KM416C1000A KM416C1000A-L KM416C1000A-F	I _{CC2}	-	2 1 1 mA mA mA
RAS-Only Refresh Current* (UCAS=LCAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I _{CC3}	-	100 90 80 mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , UCAS or LCAS, Address Cycling @tpc=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I _{CC4}	-	100 90 80 mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{CC} -0.2V)	KM416C1000A KM416C1000A-L KM416C1000A-F	I _{CC5}	-	1 300 200 mA μA μA
CAS-Before-RAS Refresh Current* (RAS, UCAS or LCAS Cycling @trc=min.)	KM416C1000A-6/A-L6/A-F6 KM416C1000A-7/A-L7/A-F7 KM416C1000A-8/A-L8/A-F8	I _{CC6}	-	100 90 80 mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V, Input Low Voltage(V _{IL})=0.2V UCAS, LCAS=0.2V DN=Don't Care, trc=31.25μs (L-Version) TRAS=TRAS min~300ns	KM416C1000A-L	I _{CC7}	-	450 μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=VIL W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ16=Vcc-0.2V or 0.2V or Open	Iccs	-	250	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.5V$, all other pins not under test=0 V)	Ii(L)	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	Io(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=VIL. In Icc4, Address can be changed maximum once while page mode cycle time tpc.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-11)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1-DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

(Test condition : VIH/VIL=2.4V/0.8V, VOH/VOL=2.4V/0.4V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from RAS	tRAC		60		70		80	ns	3,4,11
Access time from CAS	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
RAS precharge time	tRP	40		50		60		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	tRSH	15		20		20		ns	
CAS hold time	tCSH	60		70		80		ns	
CAS pulse width	tCAS	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	4
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to RAS	tAR	45		55		60		ns	6
Column address to RAS lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to RAS	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		15		20		ns	
Write command to CAS lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to RAS	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
CAS to W delay time	tCWD	40		50		50		ns	8
RAS to W delay time	tRWD	85		95		105		ns	8
Column address to W delay time	tAWD	55		60		65		ns	8
CAS precharge to W delay time	tCPWD	60		65		70		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		ns	
RAS precharge to CAS hold time	tRPC	5		5		5		ns	
CAS precharge time (C-B-F counter test cycle)	tCPT	20		25		30		ns	
Access time from CAS precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
RAS pulse width (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
RAS hold time from CAS precharge	tRHCP	35		40		45		ns	
CAS precharge time (Fast page mode)	tCP	10		10		10		ns	
RAS hold time referenced to OE	tROH	15		20		20		ns	

6

AC CHARACTERISTICS (Continued)

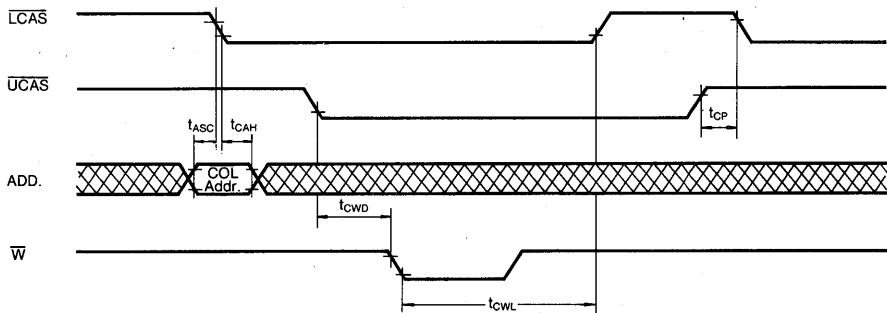
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} access time	tOEA		15		20		20	ns	
\overline{OE} to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	tOEH	15		20		20		ns	
\overline{RAS} pulse width (F-ver)	tRASS	100		100		100		μ s	19
\overline{RAS} precharge time (F-ver)	tRPS	110		130		150		ns	19
\overline{CAS} hold time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416C1000A/A-L/A-F Truth Table

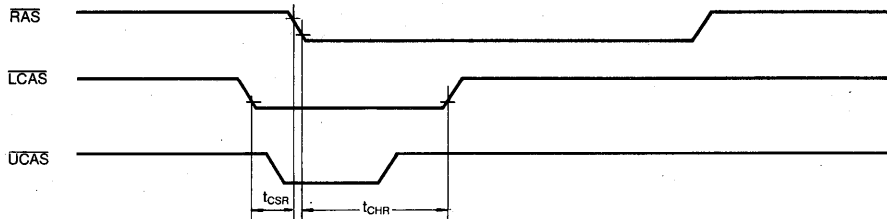
\overline{RAS}	\overline{LCAS}	\overline{UCAS}	\overline{W}	\overline{OE}	DQ ₁ -DQ ₈	DQ ₉ -DQ ₁₆	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

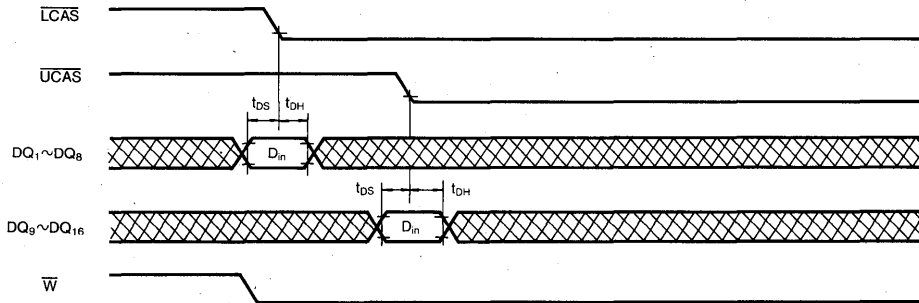
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(\min)}$ and $V_{IL(\max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(\min)}$ and $V_{IL(\max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RCD}(\max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}(\max)}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}(\max)}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}(\max)}$.
7. $t_{\text{OFF}(\max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}(\min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}(\min)}$, $t_{\text{RWD}} \geq t_{\text{RWD}(\min)}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RAD}(\max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}(\max)}$ limit, then access time is controlled by t_{AA} .
12. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
13. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.



16. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
17. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



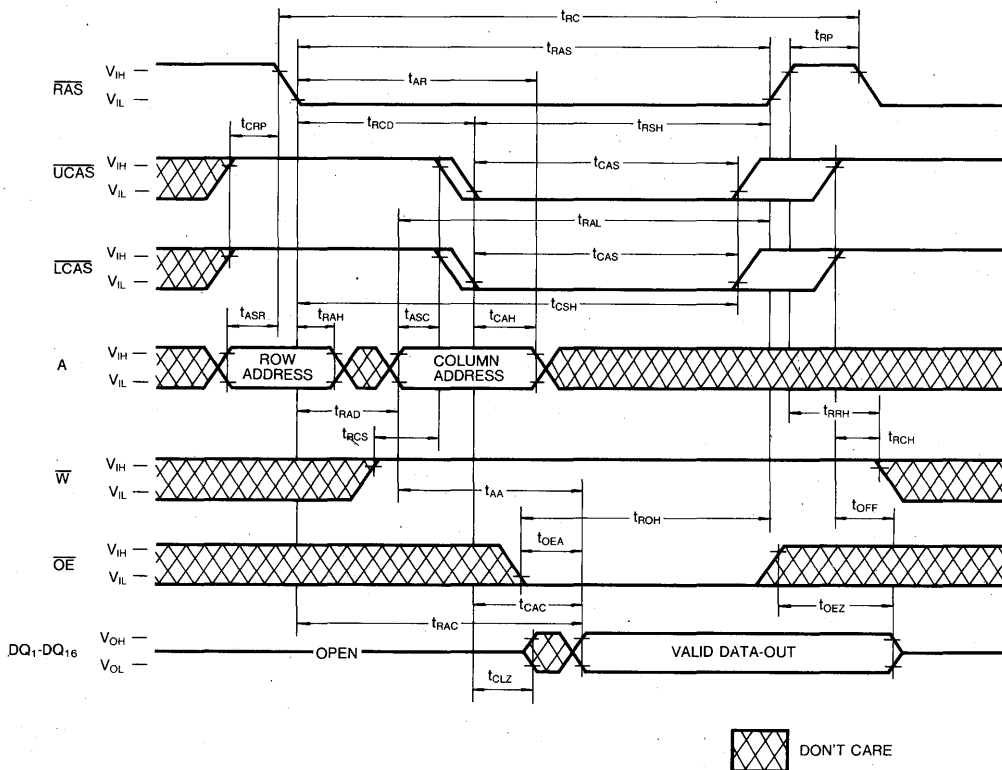
18. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1\sim8)}$, upper byte $D_{in(9\sim16)}$



19. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)

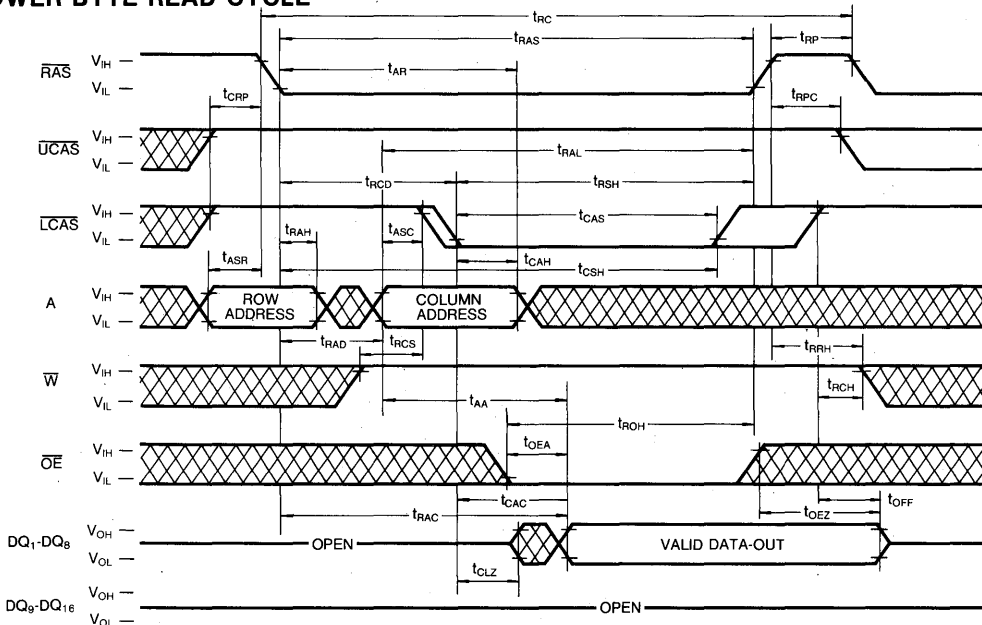
TIMING DIAGRAMS

WORD READ CYCLE

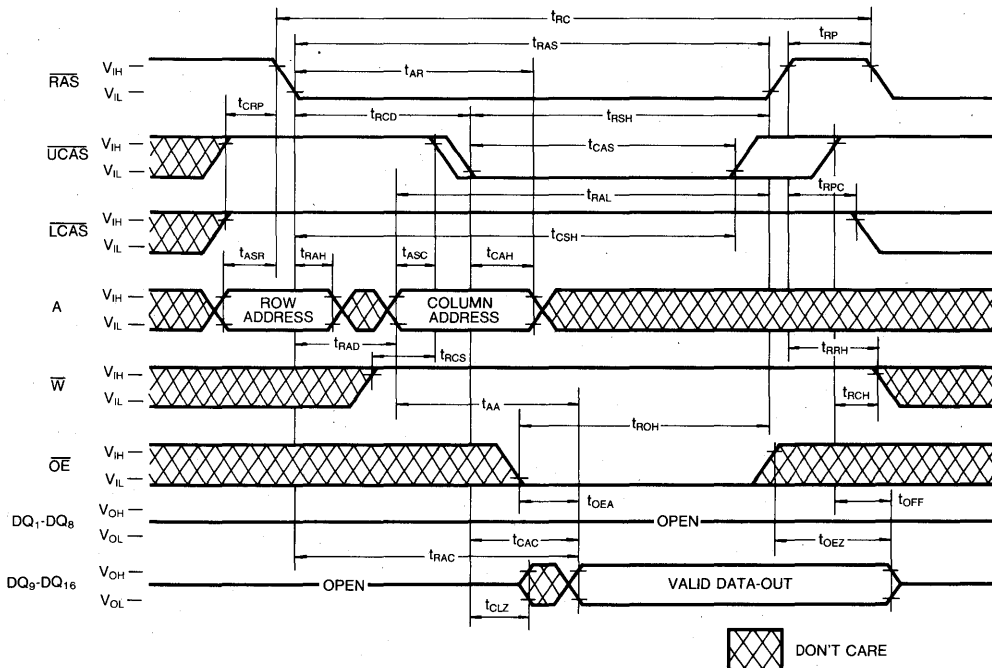


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

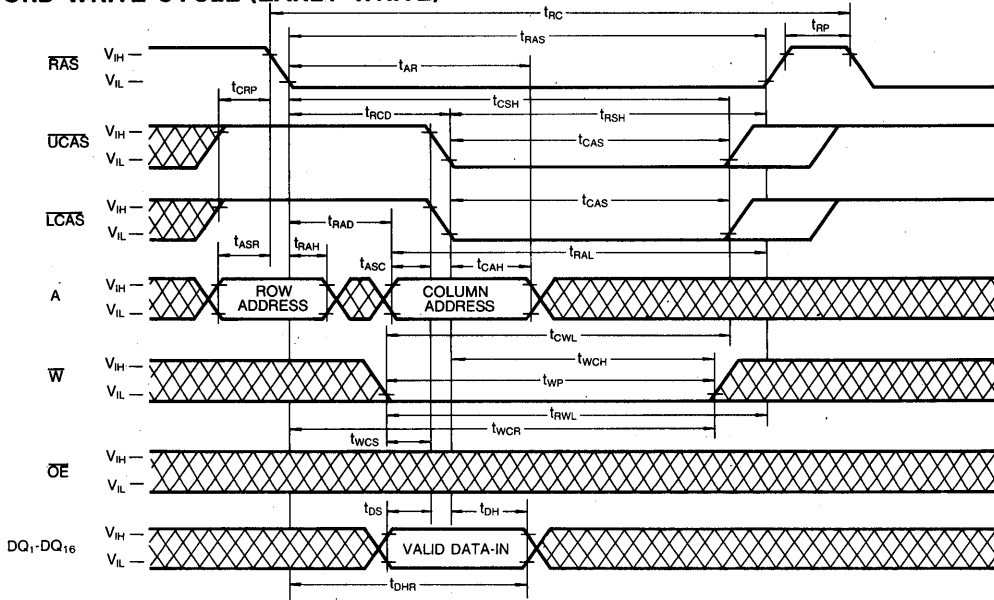


UPPER BYTE READ CYCLE

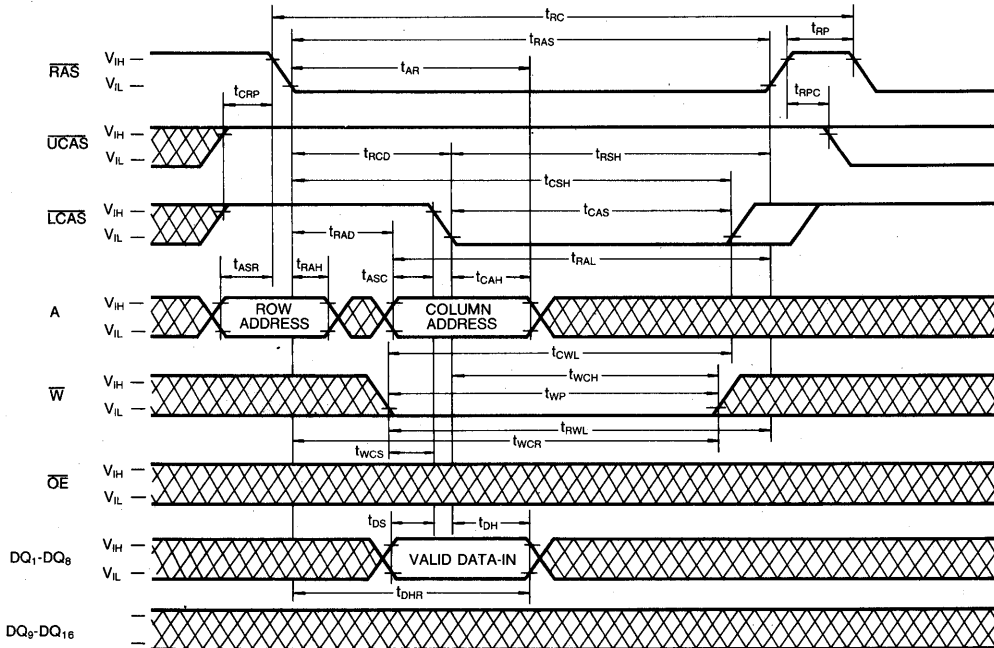


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



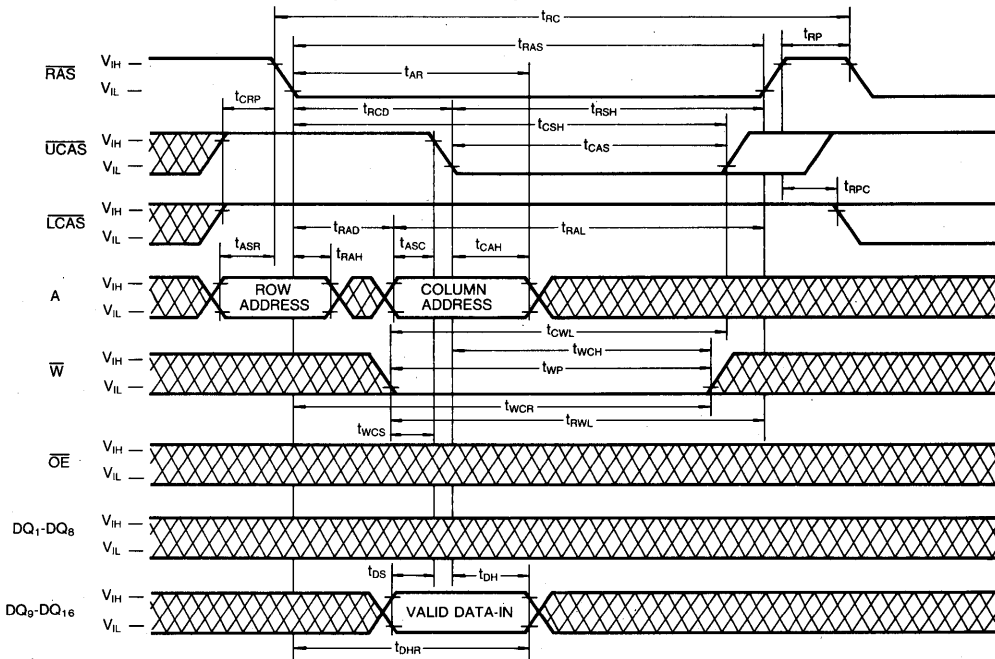
LOWER BYTE WRITE CYCLE (EARLY WRITE)



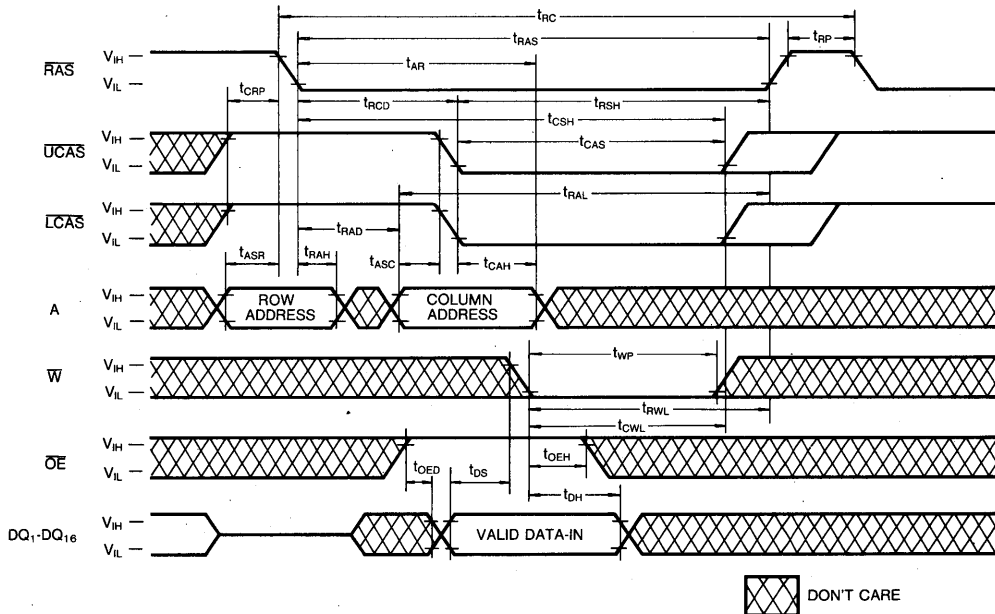
 DON'T CARE

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



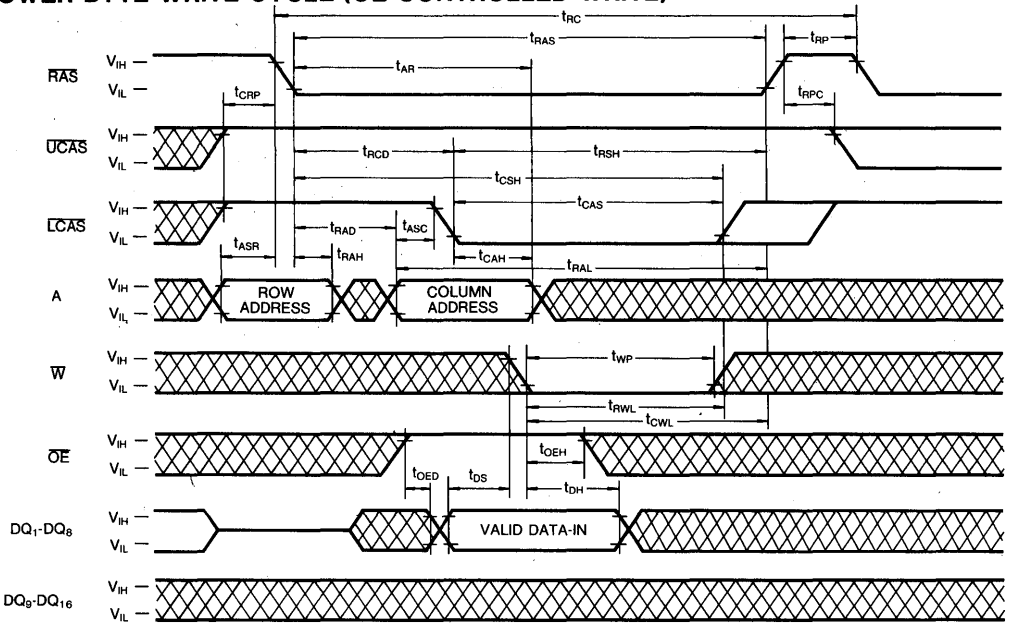
WORD WRITE CYCLE (OE CONTROLLED WRITE)



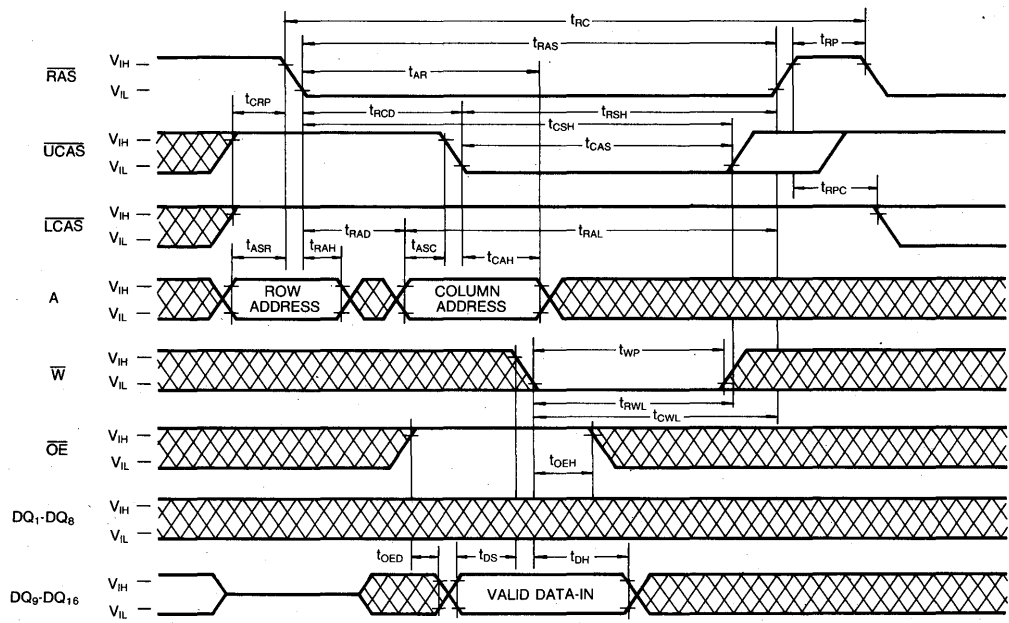
6

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



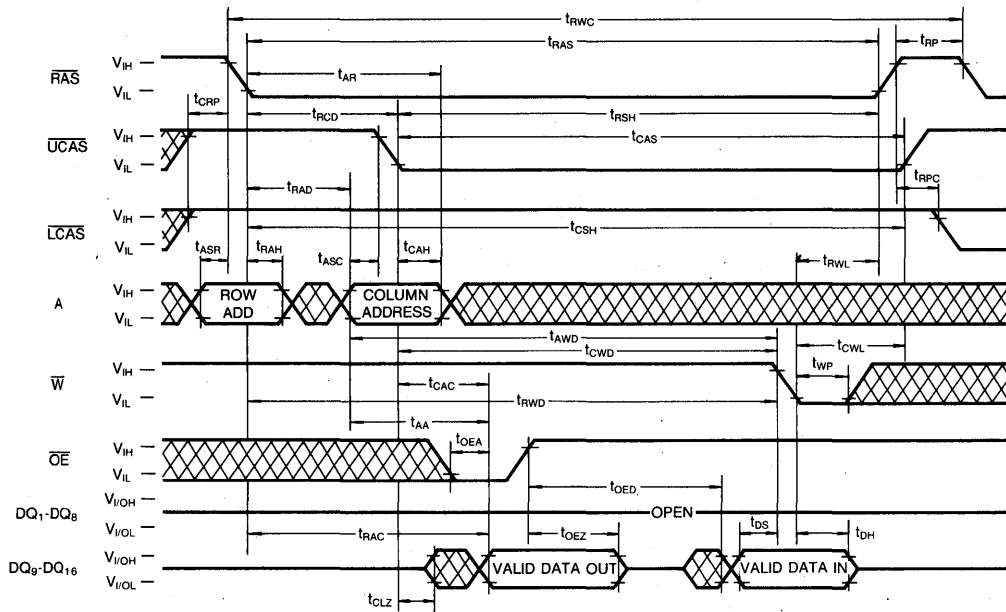
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



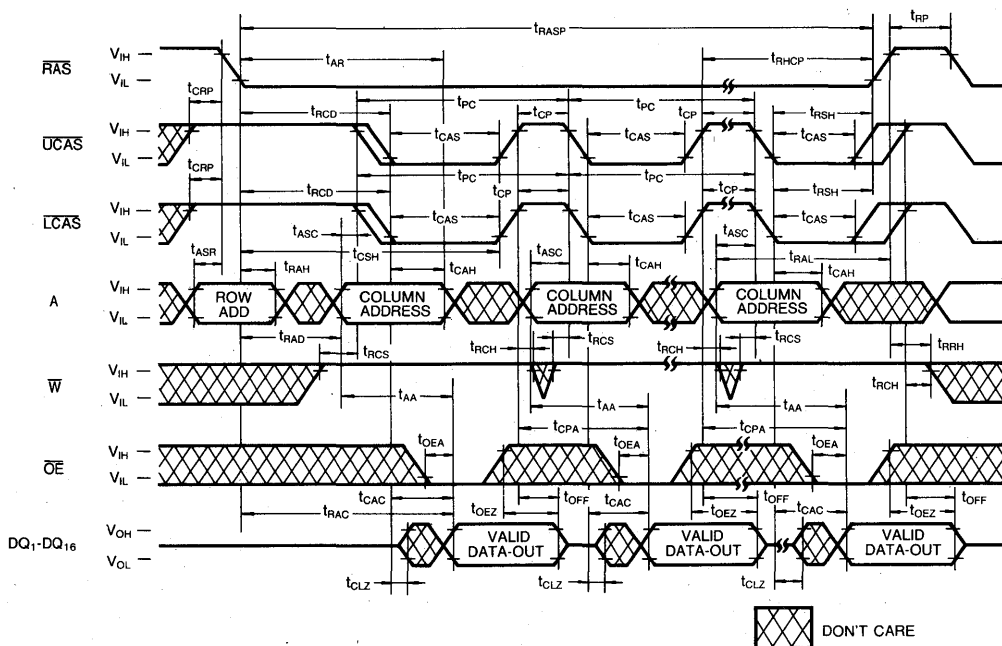
DONT CARE

TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE

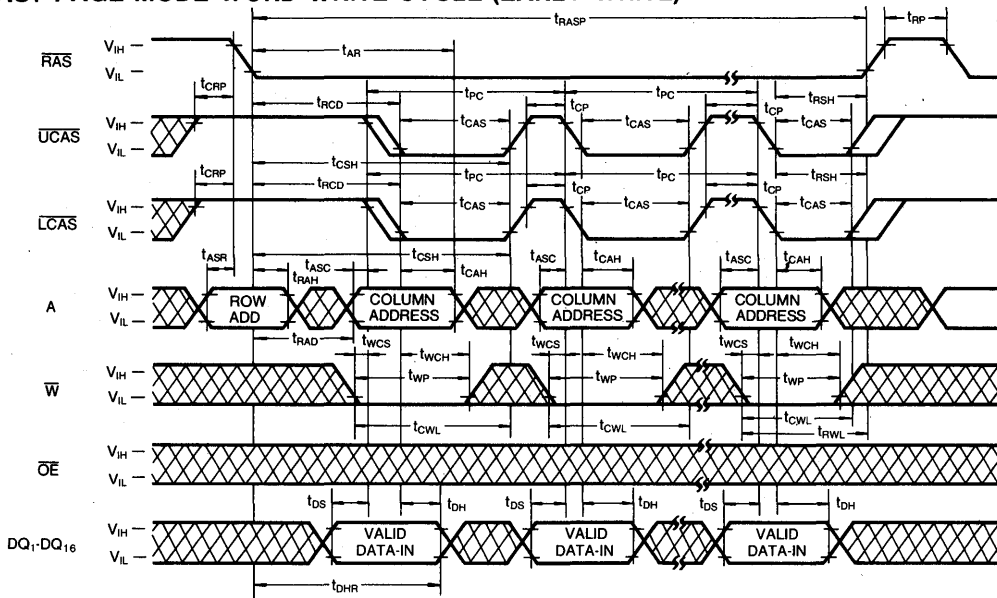


FAST PAGE MODE WORD READ CYCLE

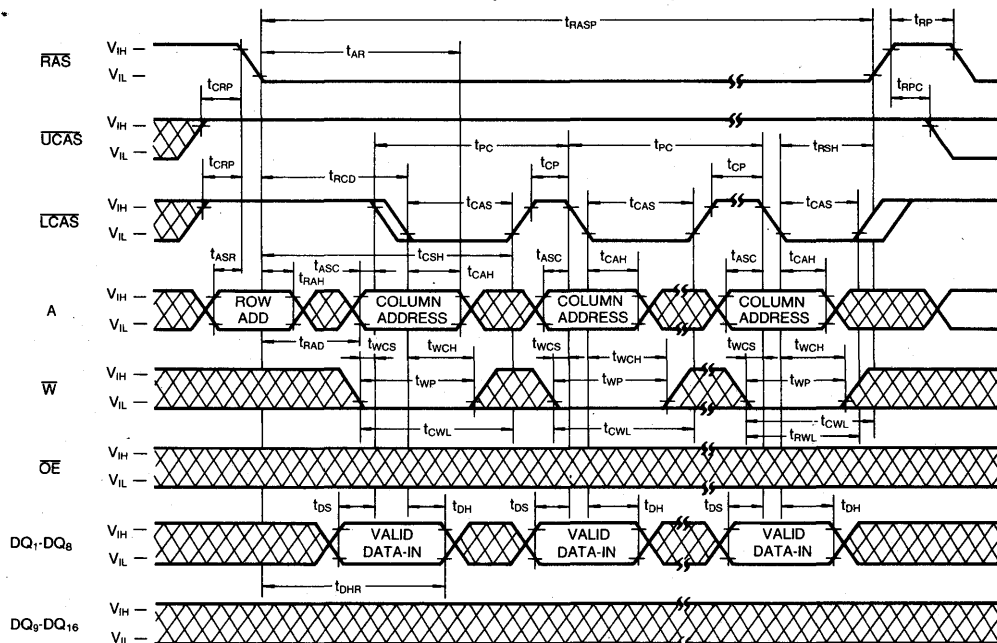


TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



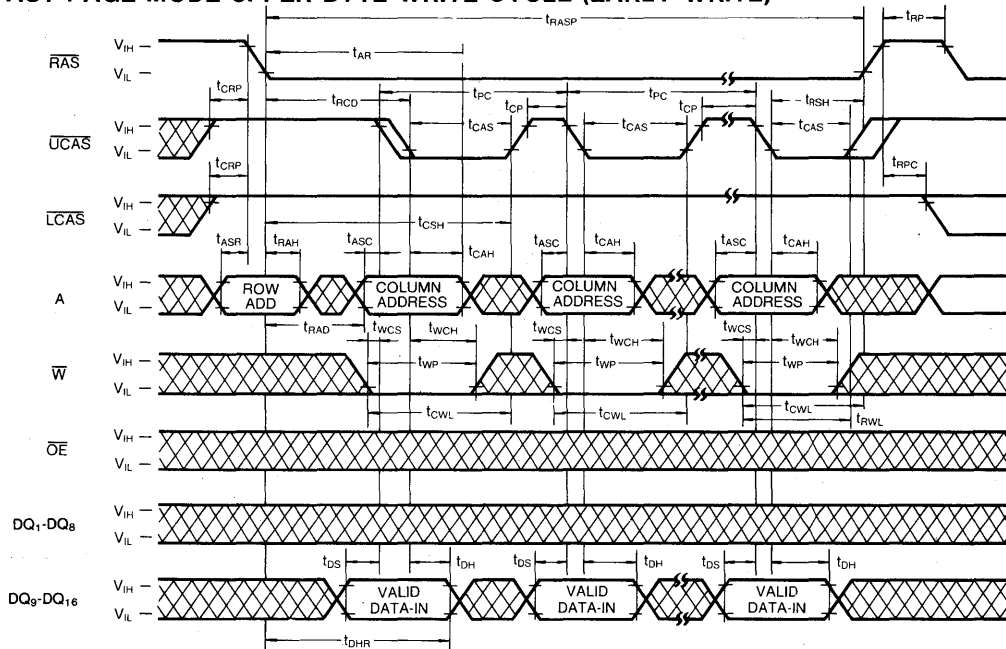
FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)



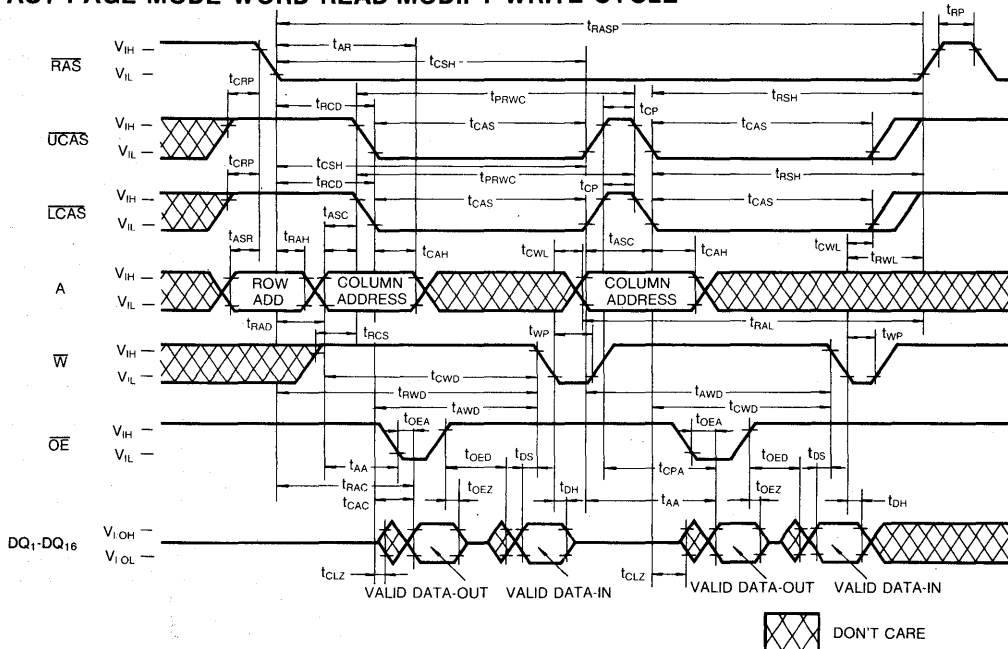
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

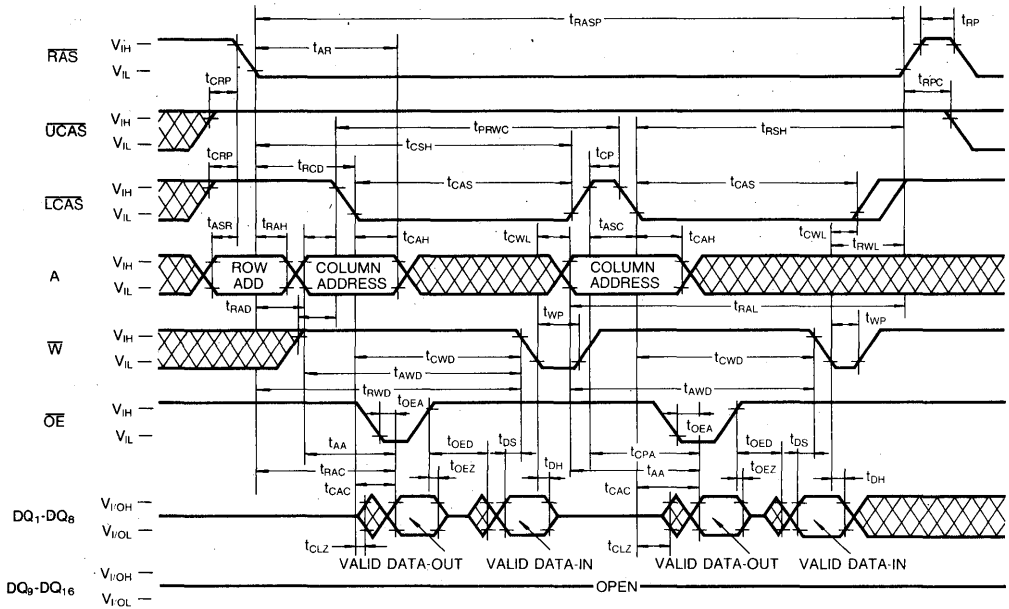


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE

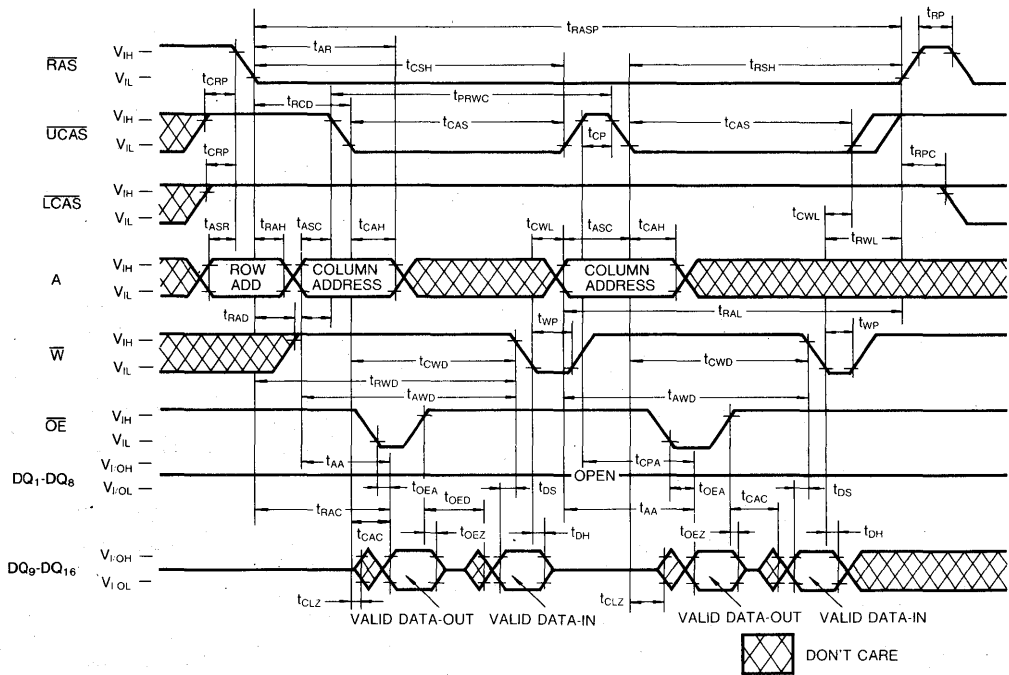


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



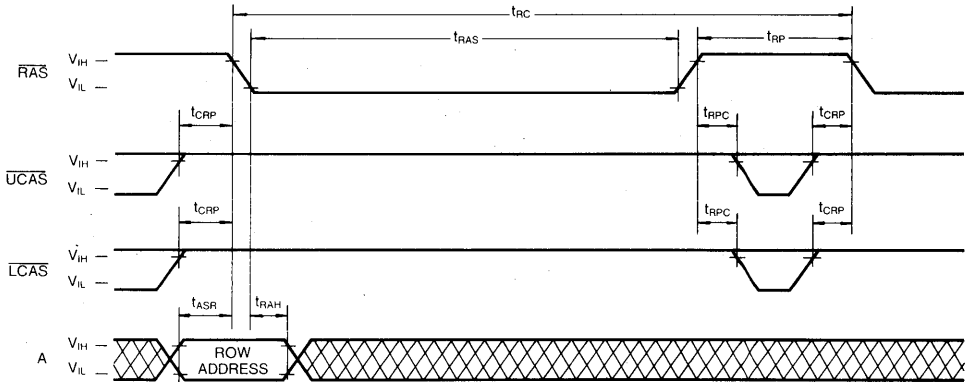
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

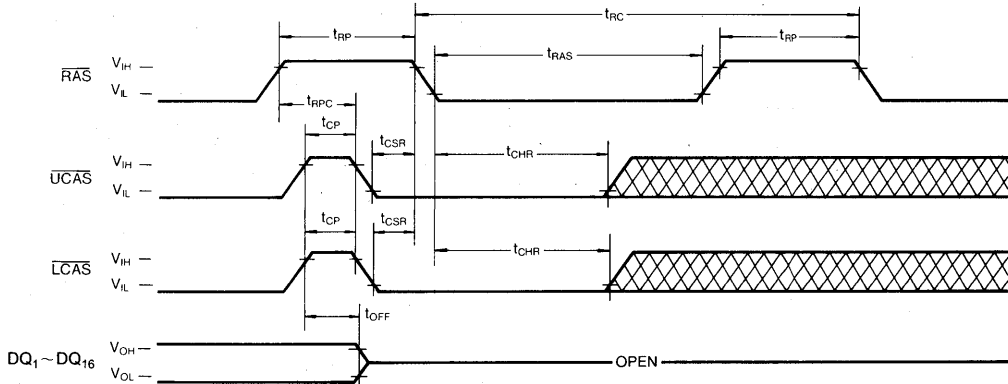
RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} = Don't Care



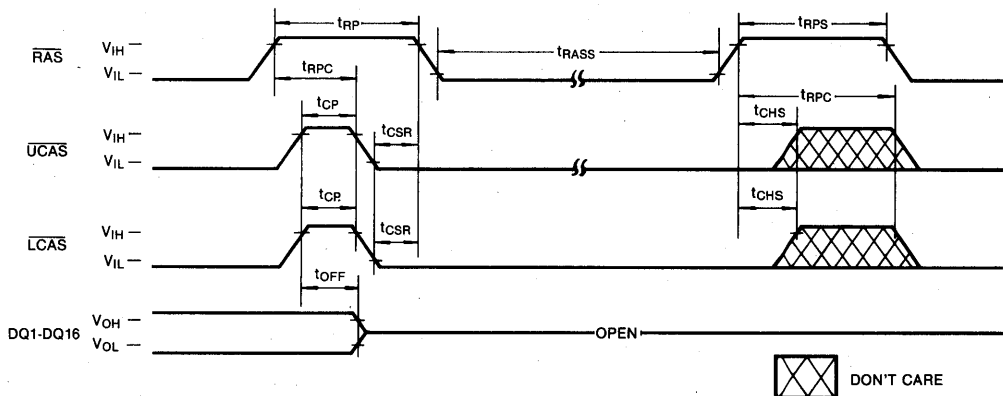
CAS-BEFORE-RAS REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} , A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE

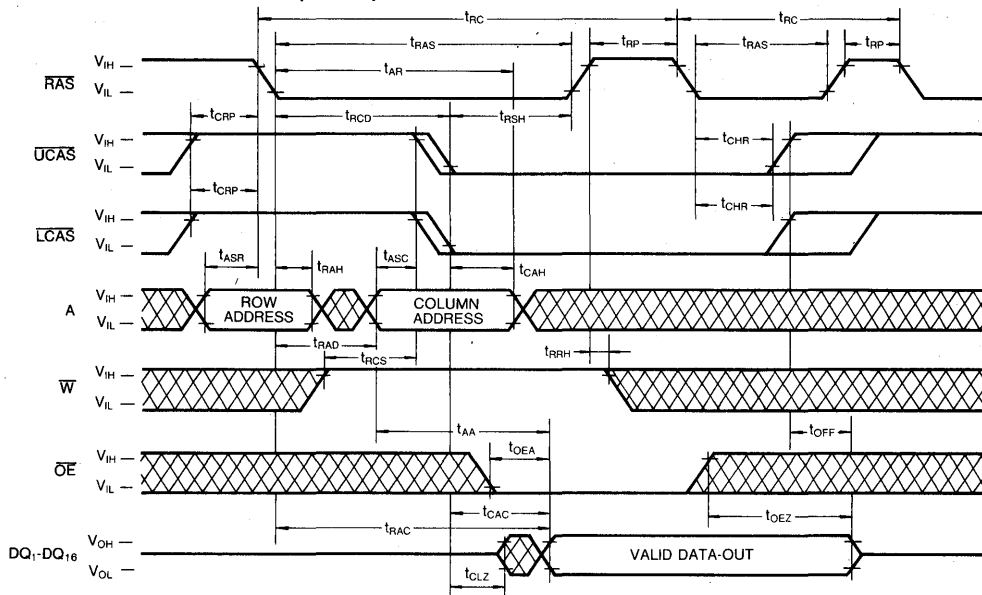
NOTE: \bar{W} , \bar{OE} , A = Don't Care



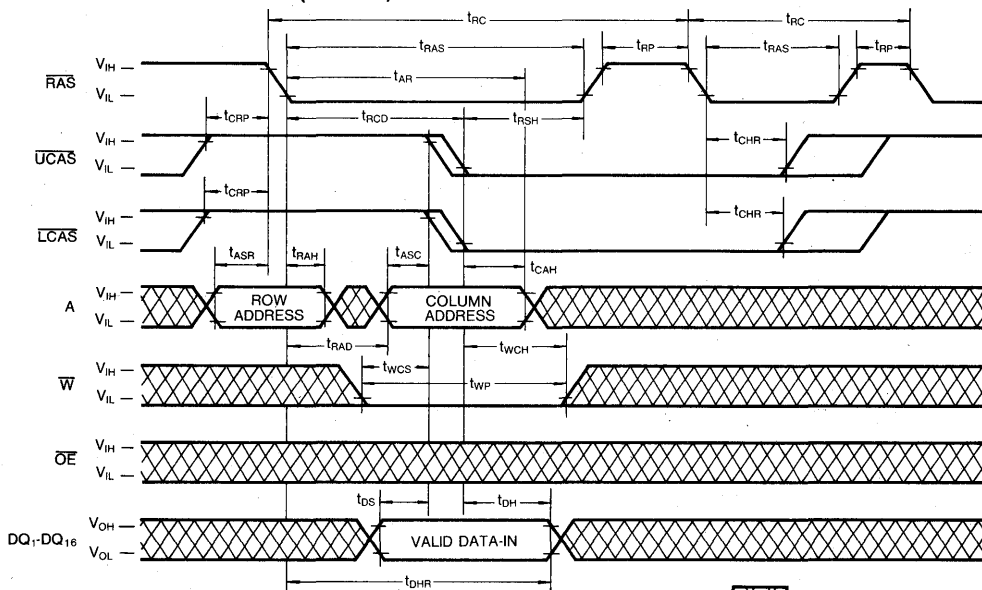
 DON'T CARE


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



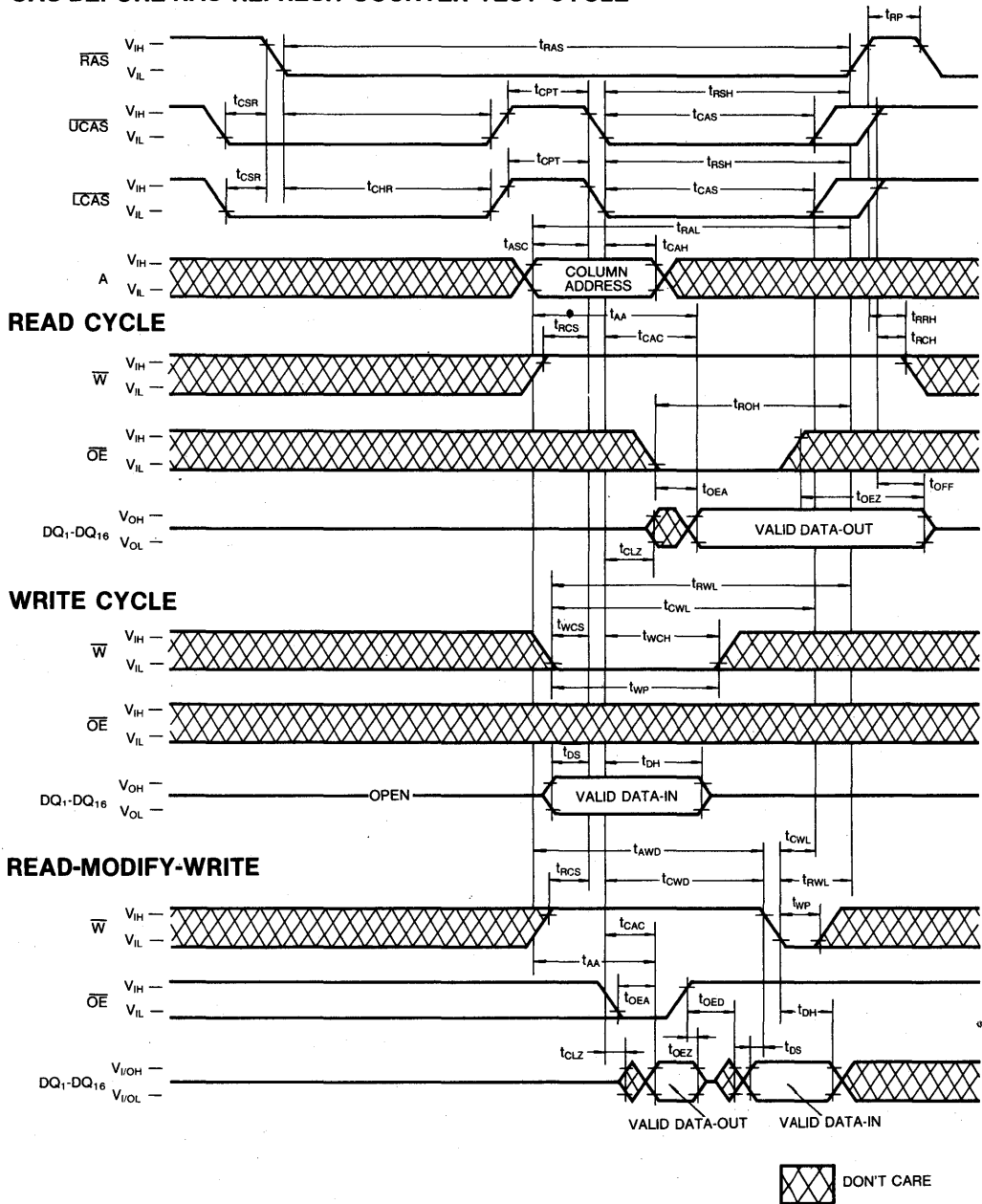
HIDDEN REFRESH CYCLE (WRITE)



 DON'T CARE

TIMING DIAGRAMS (Continued)

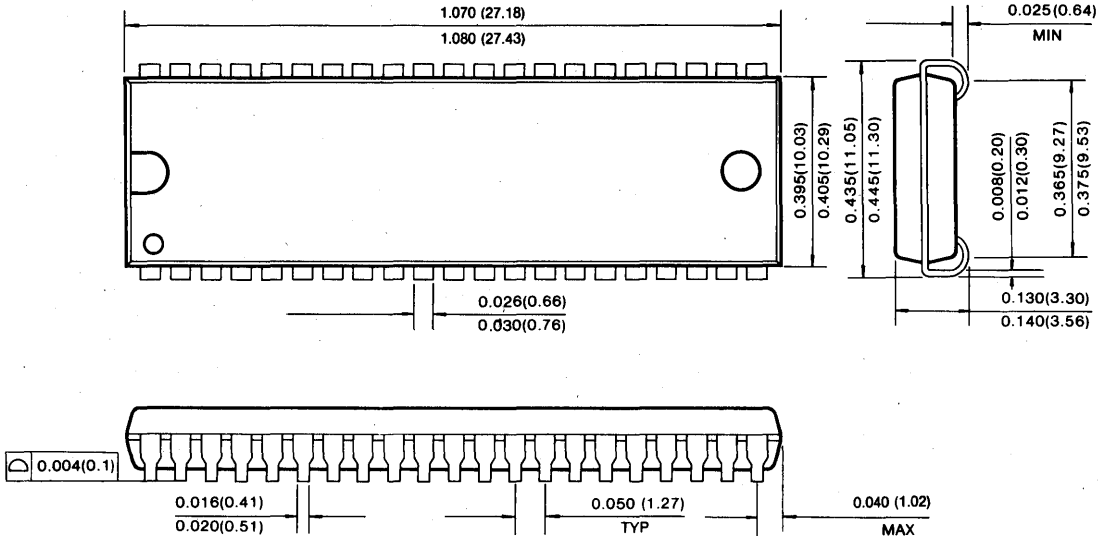
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



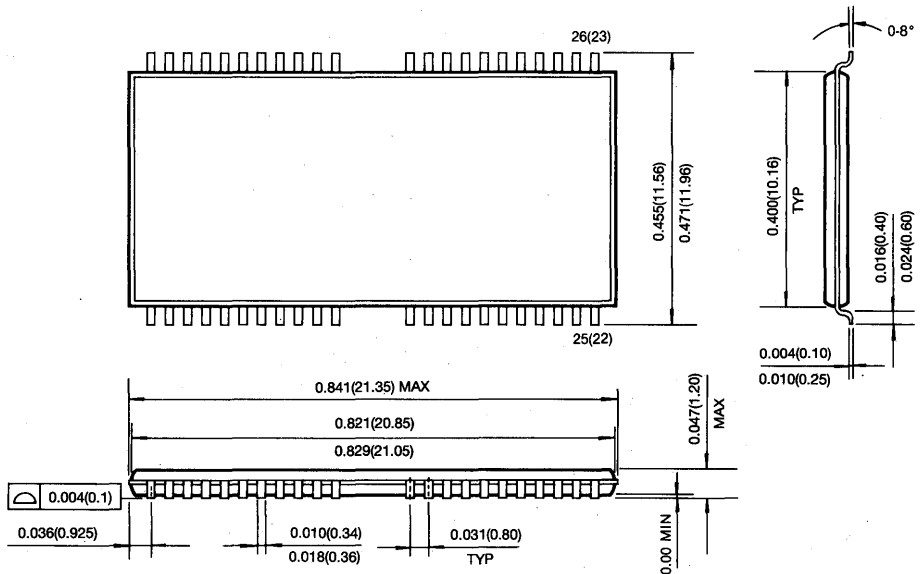
6

PACKAGE DIMENSION
42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	t_{TRAC}	t_{CAC}	t_{TRC}
KM416C1200A-6/A-L6/A-F6	60ns	15ns	110ns
KM416C1200A-7/A-L7/A-F7	70ns	20ns	130ns
KM416C1200A-8/A-L8/A-F8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 CAS Byte/Word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V ± 10% power supply**
- **Refresh Cycle**
 - 1024 cycles/16ms (Normal)
 - 1024 cycles/128ms (L-version)
 - 1024 cycles/128ms (F-version)
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

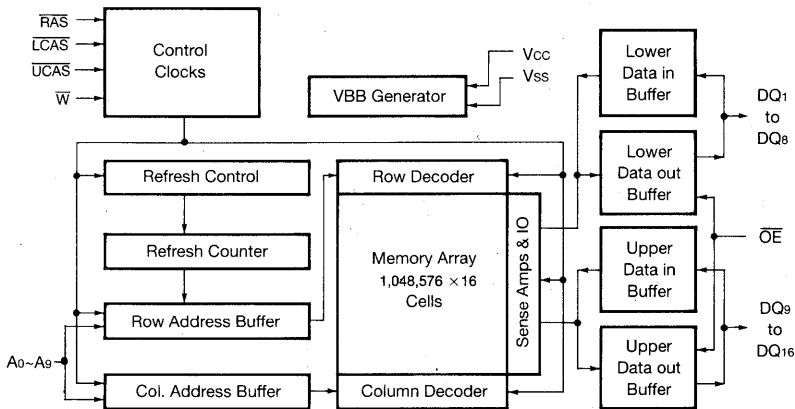
GENERAL DESCRIPTION

The Samsung KM416C1200A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

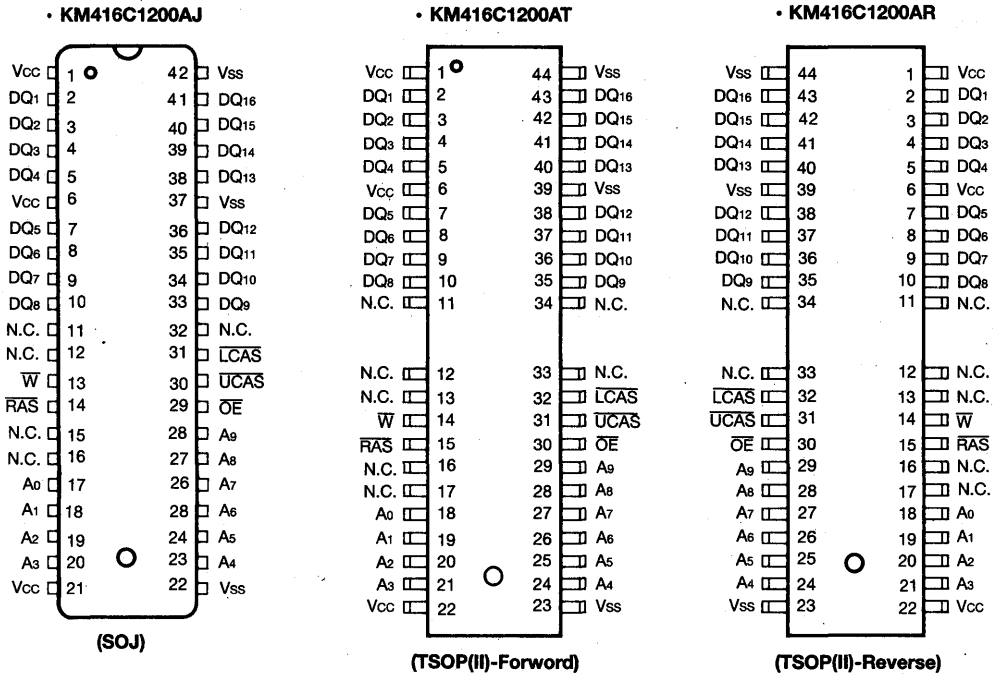
The KM416C1200A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1200A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5V)
N.C.	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1~ +7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1~ +7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} + 1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* (R _{AS} , UCAS or LCAS, Address Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I _{CC1}	-	160 150 140	mA mA mA
Standby Current (R _{AS} =UCAS=LCAS=W=V _{IH})	KM416C1200A KM416C1200A-L KM416C1200A-F	I _{CC2}	-	2 1 1	mA mA mA
R _{AS} -Only Refresh Current* (UCAS=LCAS=V _{IH} , R _{AS} , Address Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I _{CC3}	-	160 150 140	mA mA mA
Fast Page Mode Current* (R _{AS} =V _{IL} , UCAS or LCAS, Address Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I _{CC4}	-	110 100 90	mA mA mA
Standby Current (R _{AS} =UCAS=LCAS=W=V _{CC} -0.2V)	KM416C1200A KM416C1200A-L KM416C1200A-F	I _{CC5}	-	1 300 200	mA μA μA
C _{AS} -Before-R _{AS} Refresh Current* (R _{AS} , UCAS or LCAS Cycling @trc=min.)	KM416C1200A-6/A-L6/A-F6 KM416C1200A-7/A-L7/A-F7 KM416C1200A-8/A-L8/A-F8	I _{CC6}	-	160 150 140	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V, Input Low Voltage(V _{IL})=0.2V UCAS, LCAS= 0.2V DIN=Don't Care, trc=125μs (L-Version) tRAS=tRAS min~300ns	KM416C1200A-L	I _{CC7}	-	350	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A9=Vcc-0.2V or 0.2V DQ1-DQ16=Vcc-0.2V, 0.2V or Open	Iccs	-	250	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 V)	Ii(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)	Io(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=VIL. In Icc4, Address can be changed maximum once while page mode cycle time tpc.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A9)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1-DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, Vcc=5.0V ± 10%, See notes 1,2)

(Test condition : VIH/VIL=2.4V/0.8V, VOH/VOL=2.4V/0.4V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from RAS	trac		60		70		80	ns	3,4,11
Access time from CAS	tcac		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tr	3	50	3	50	3	50	ns	2
RAS precharge time	trp	40		50		60		ns	
RAS pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	15		20		20		ns	
CAS hold time	tcSH	60		70		80		ns	
CAS pulse width	tcAS	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ - $\overline{\text{B}}$ - $\overline{\text{R}}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	tROH	15		20		20		ns	

6

AC CHARACTERISTICS (Continued)

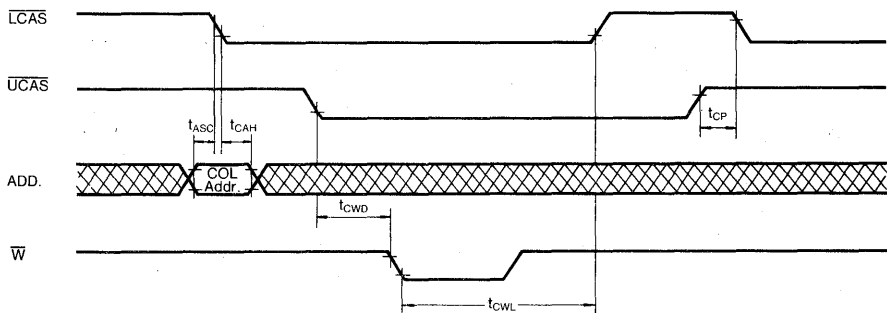
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} access time	toEA		15		20		20	ns	
\overline{OE} to data delay	toED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	toEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	toEH	15		20		20		ns	
\overline{RAS} pulse width (F-ver)	trASS	100		100		100		μ s	19
\overline{RAS} precharge time (F-ver)	trPS	110		130		150		ns	19
\overline{CAS} hold time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416C1200A/A-L/A-F Truth Table

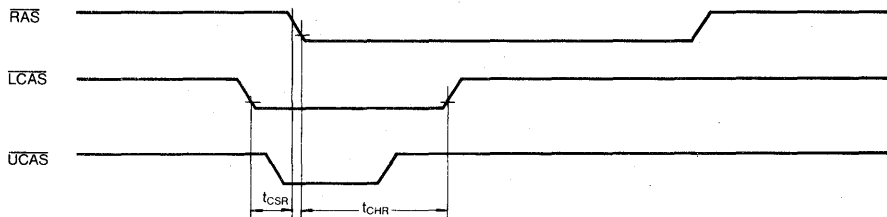
RAS	LCAS	UCAS	W	\overline{OE}	DQ ₁ -DQ ₈	DQ ₉ -DQ ₁₆	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

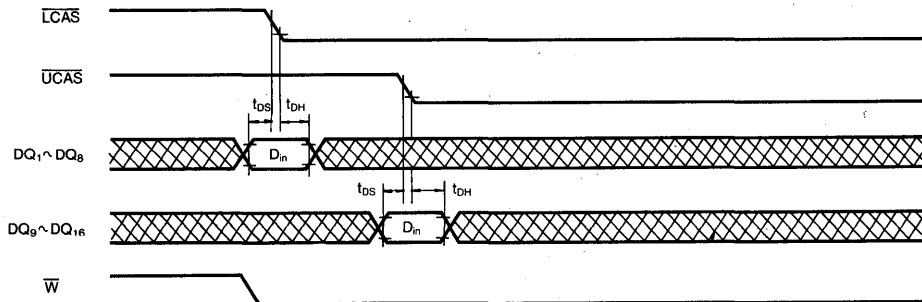
1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(\text{min})}$ and $V_{IL(\text{max})}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}(\text{max})}$ limit insures that $t_{\text{RAC}(\text{max})}$ can be met. $t_{\text{RCD}(\text{max})}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}(\text{max})}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}(\text{max})}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}(\text{max})}$.
7. $t_{\text{OFF}(\text{max})}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating aparameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}(\text{min})}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}(\text{min})}$, $t_{\text{RWD}} \geq t_{\text{RWD}(\text{min})}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\text{min})}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}(\text{max})}$ limit insures that $t_{\text{RAC}(\text{max})}$ can be met. $t_{\text{RAD}(\text{max})}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}(\text{max})}$ limit, then access time is controlled by t_{AA} .
12. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
13. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.



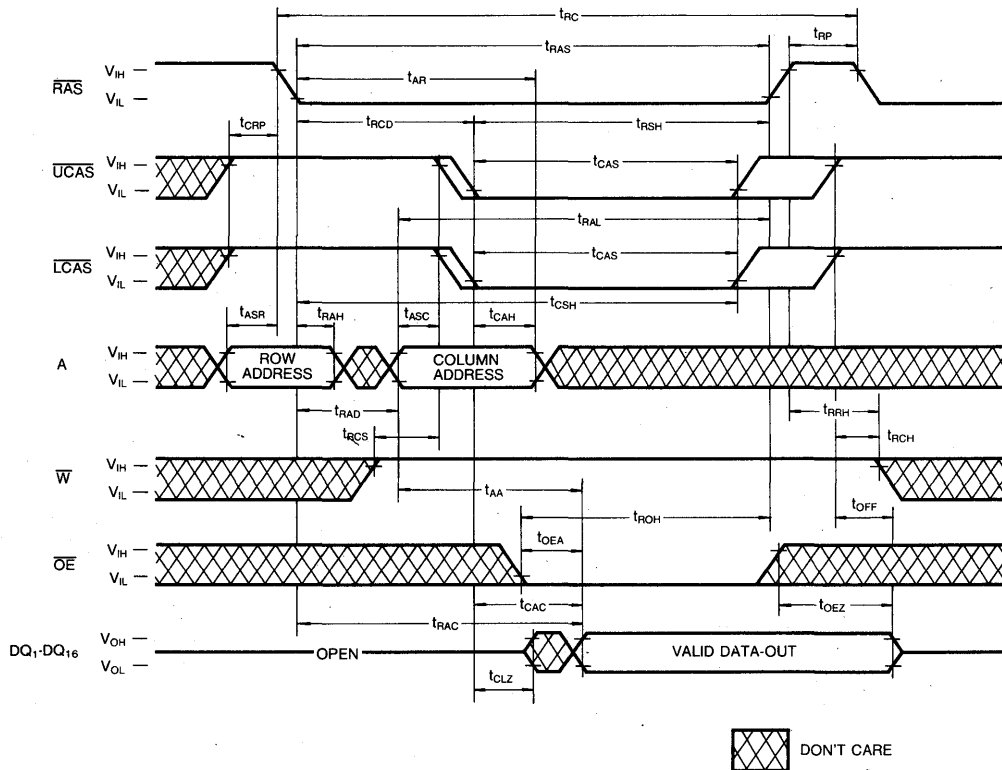
16. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
17. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.



18. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1\sim 8)}$, upper byte $D_{in(9\sim 16)}$

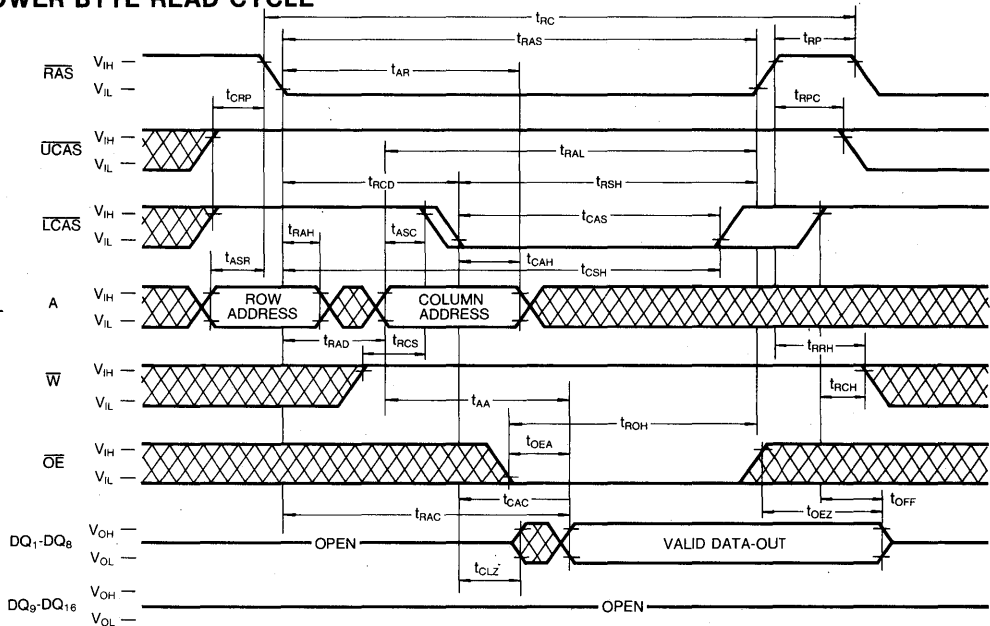


TIMING DIAGRAMS
WORD READ CYCLE

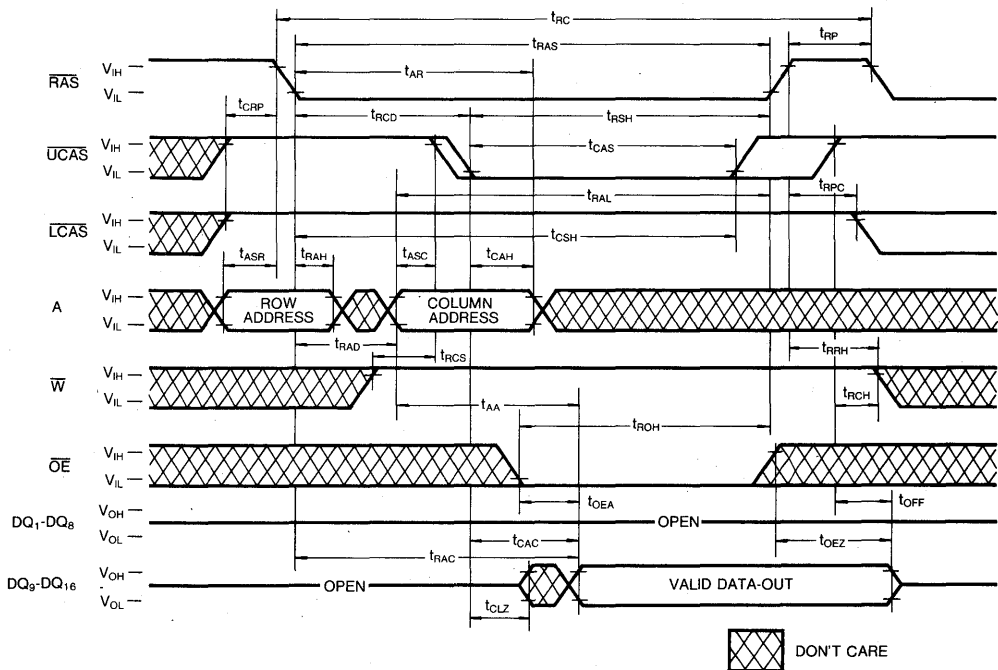


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

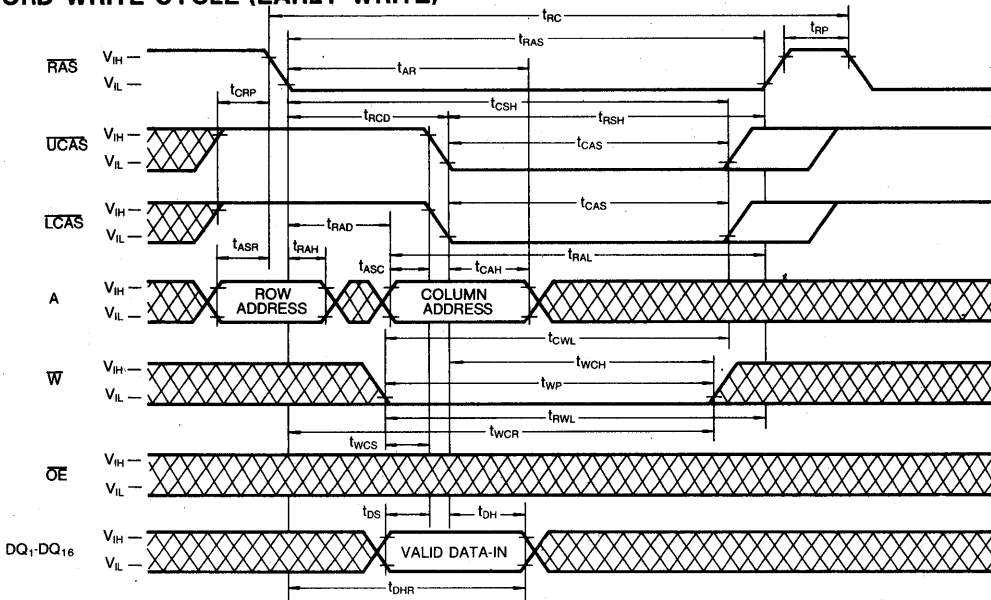


UPPER BYTE READ CYCLE

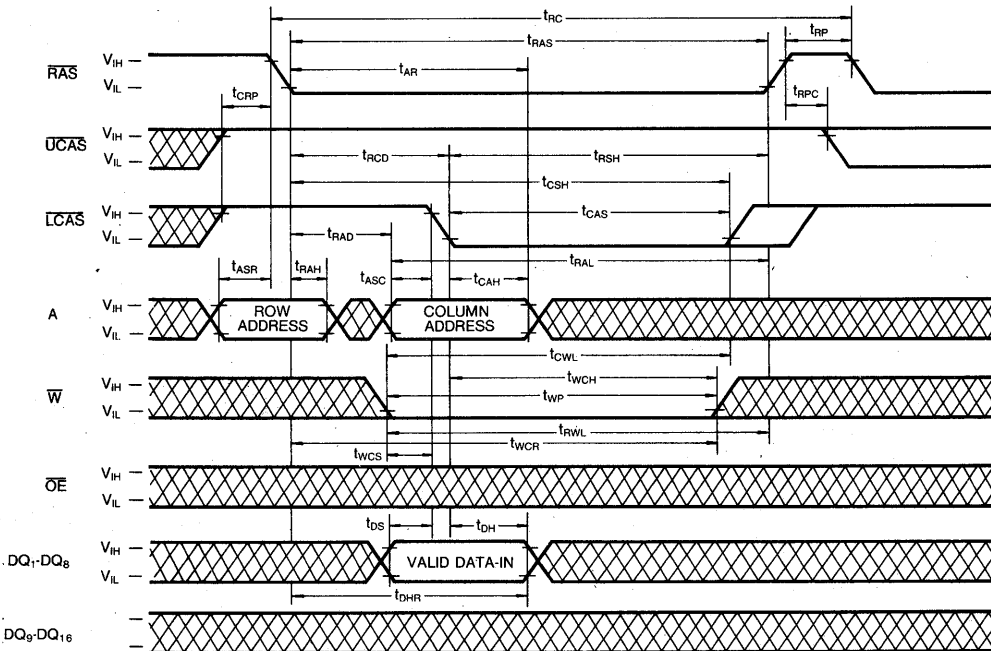


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



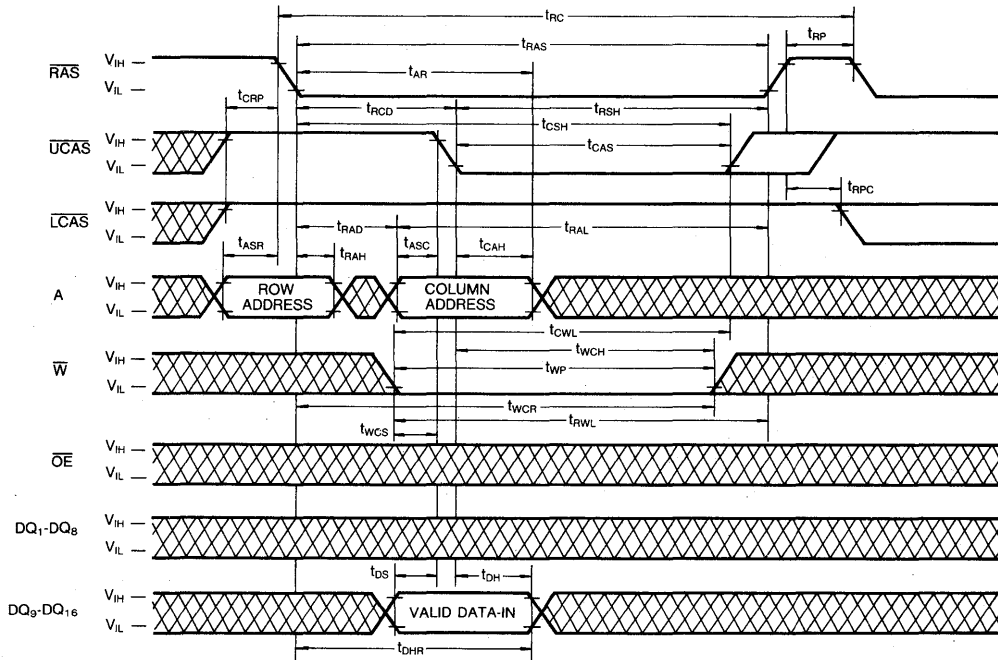
LOWER BYTE WRITE CYCLE (EARLY WRITE)



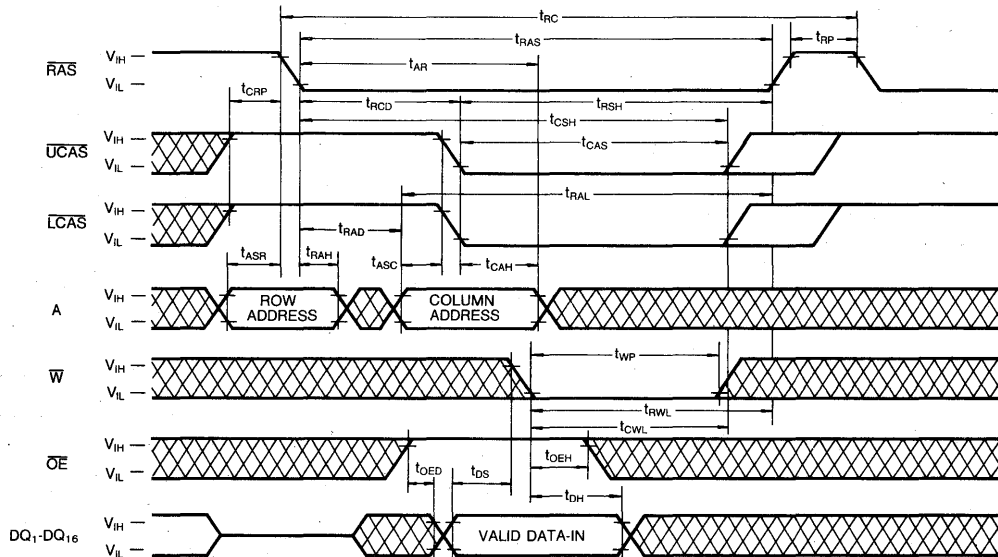
 DON'T CARE

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)



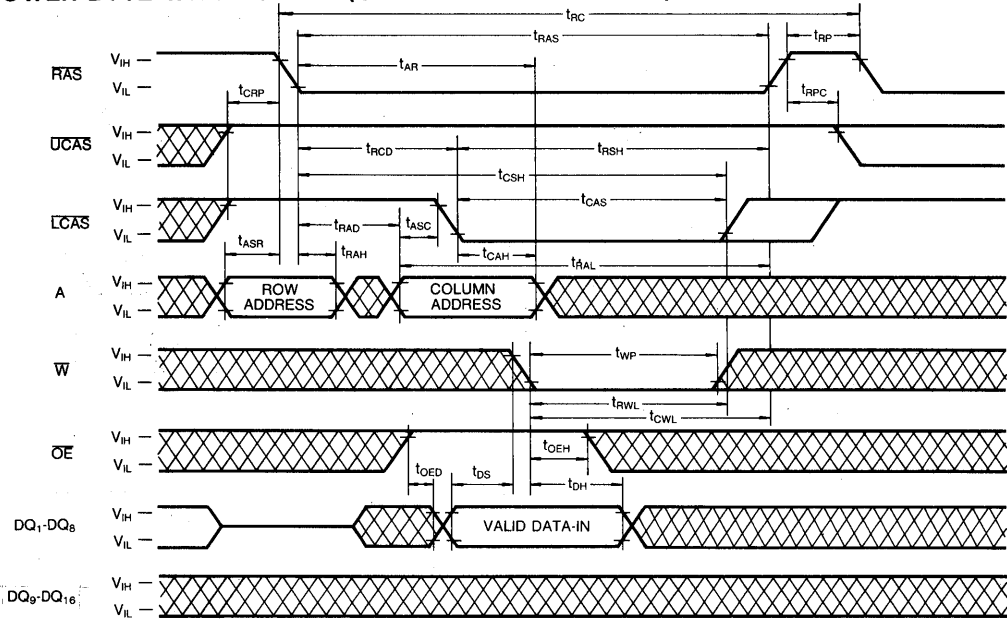
WORD WRITE CYCLE (OE CONTROLLED WRITE)



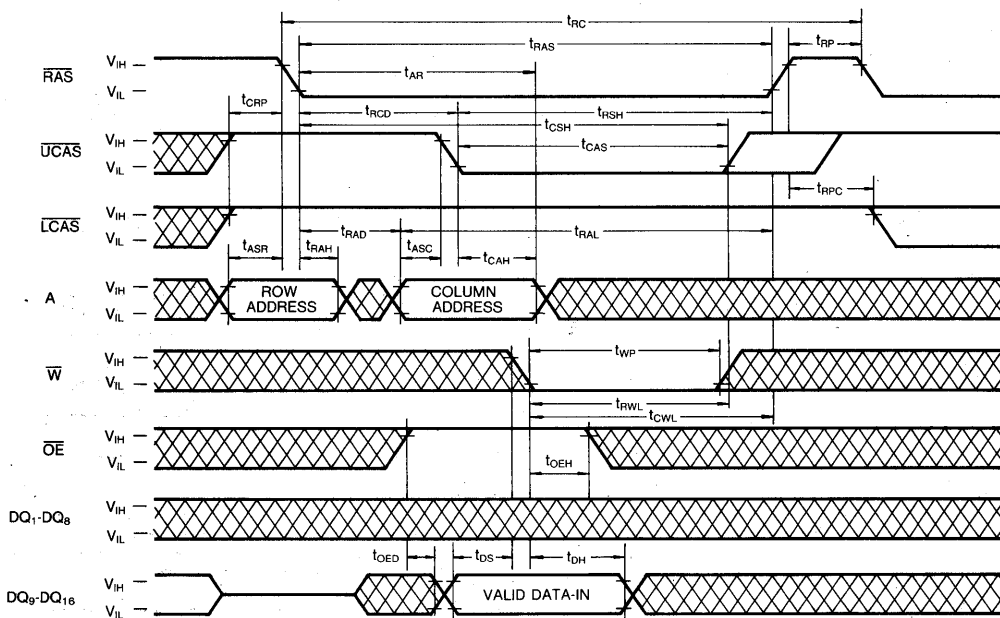
DON'T CARE

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



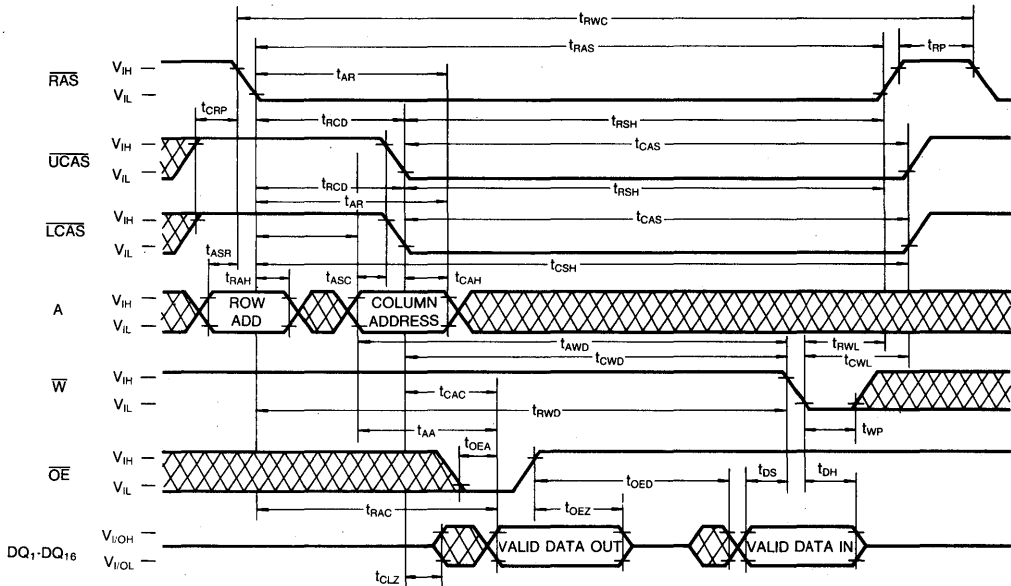
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



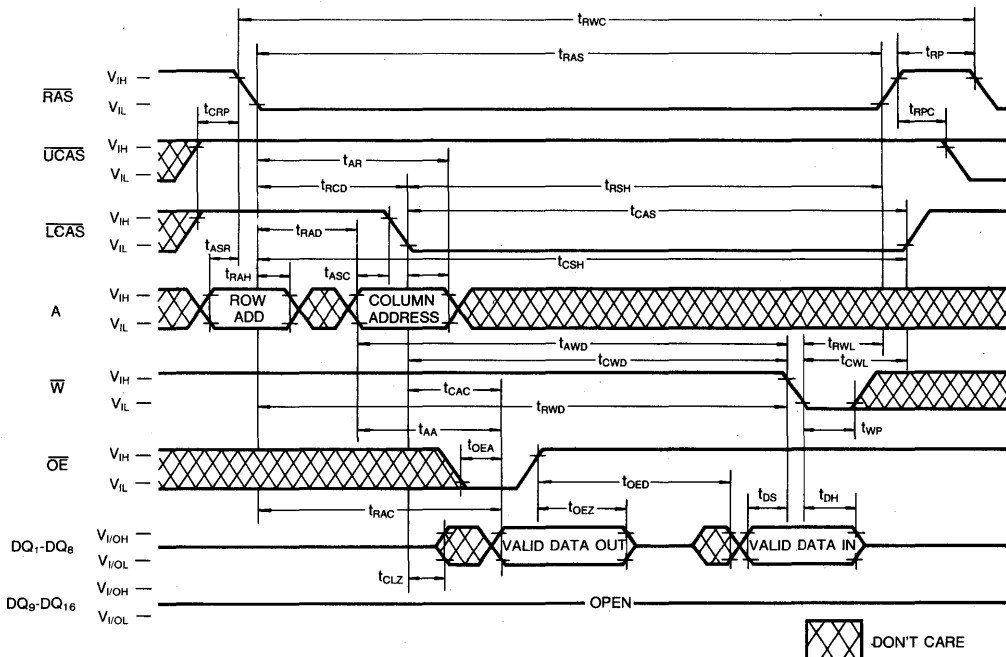
 DON'T CARE

TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

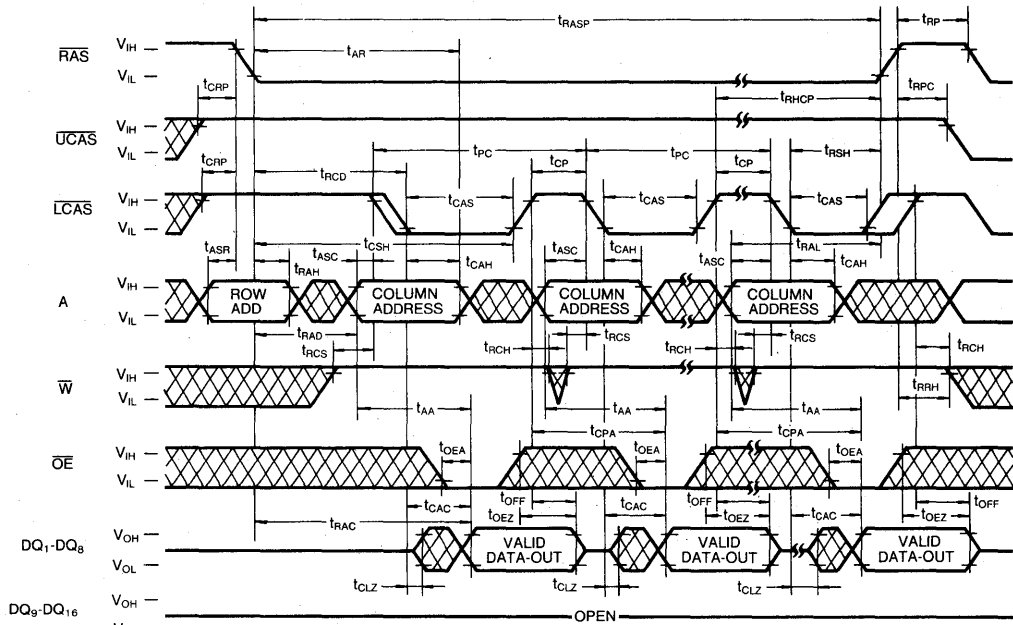


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

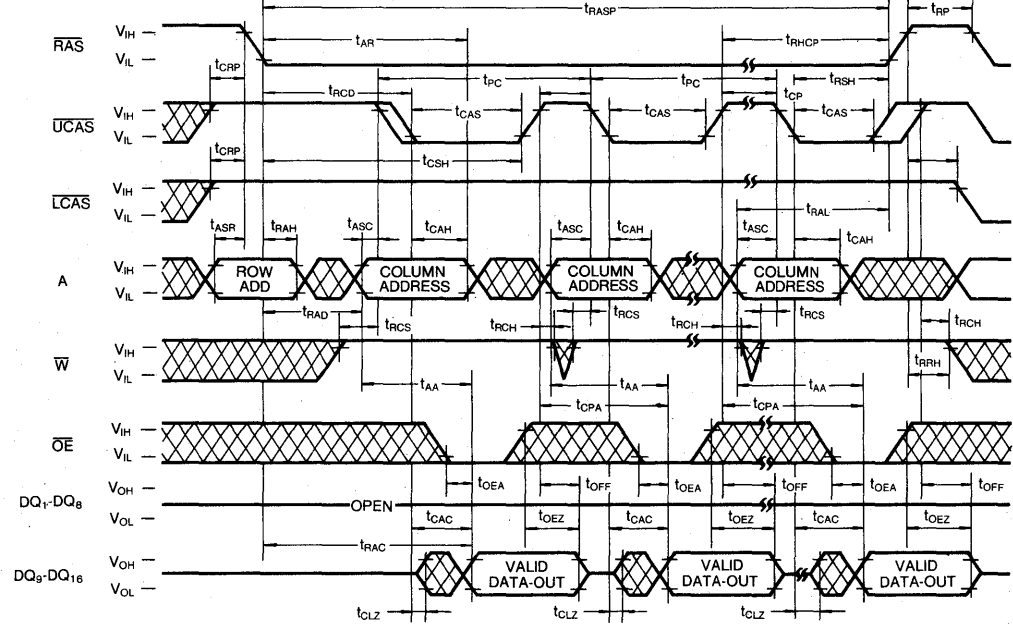


TIMING DIAGRAMS (Continued)

FAST PAGE MODE LOWER BYTE READ CYCLE



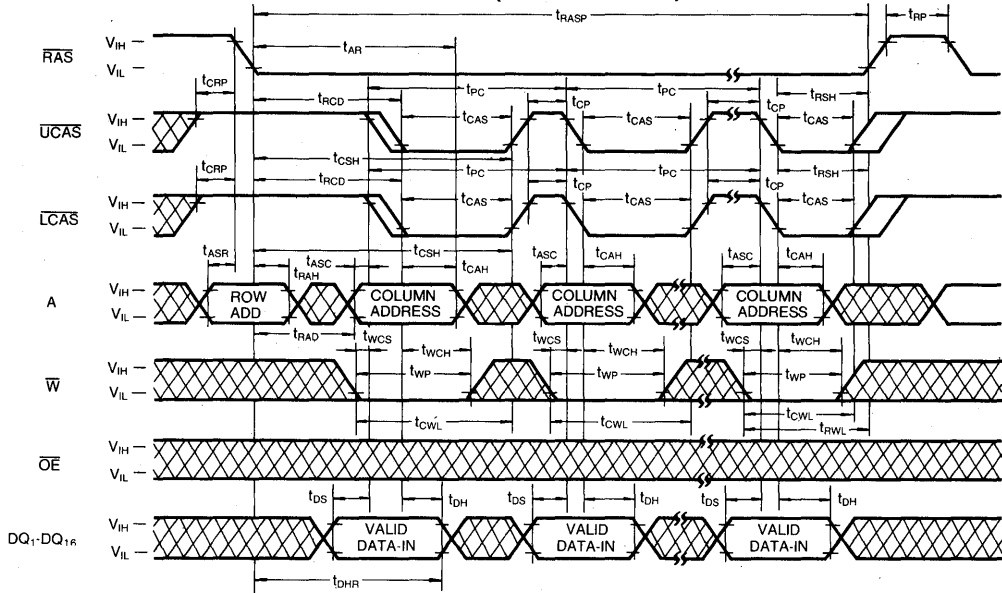
FAST PAGE MODE UPPER BYTE READ CYCLE



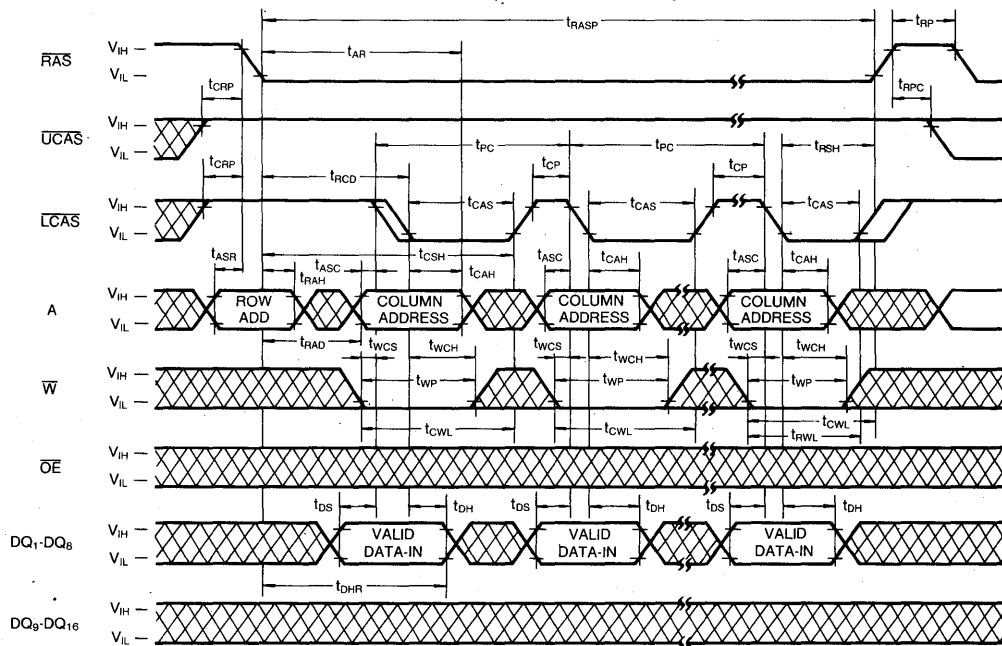
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



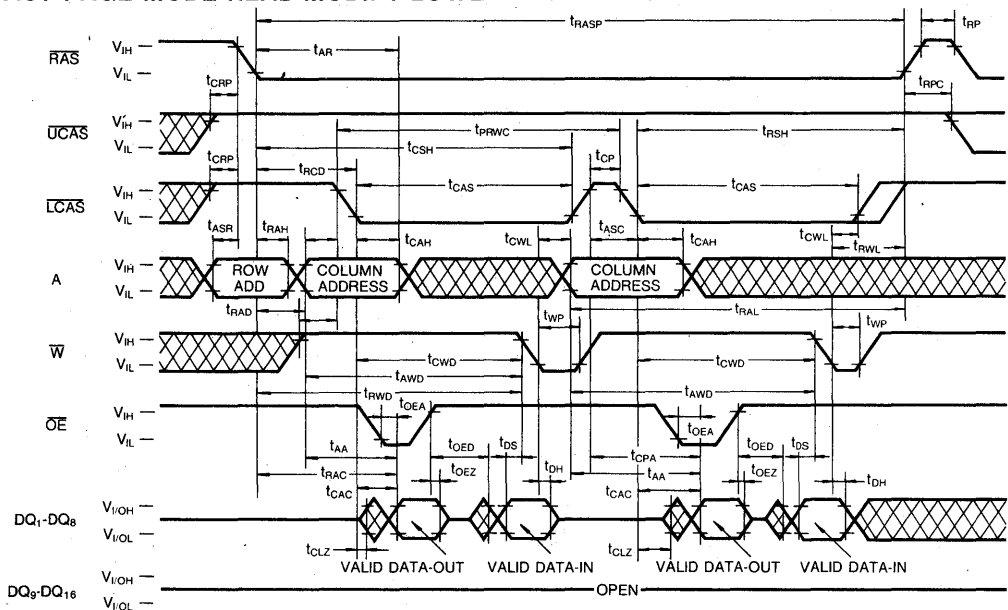
FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)



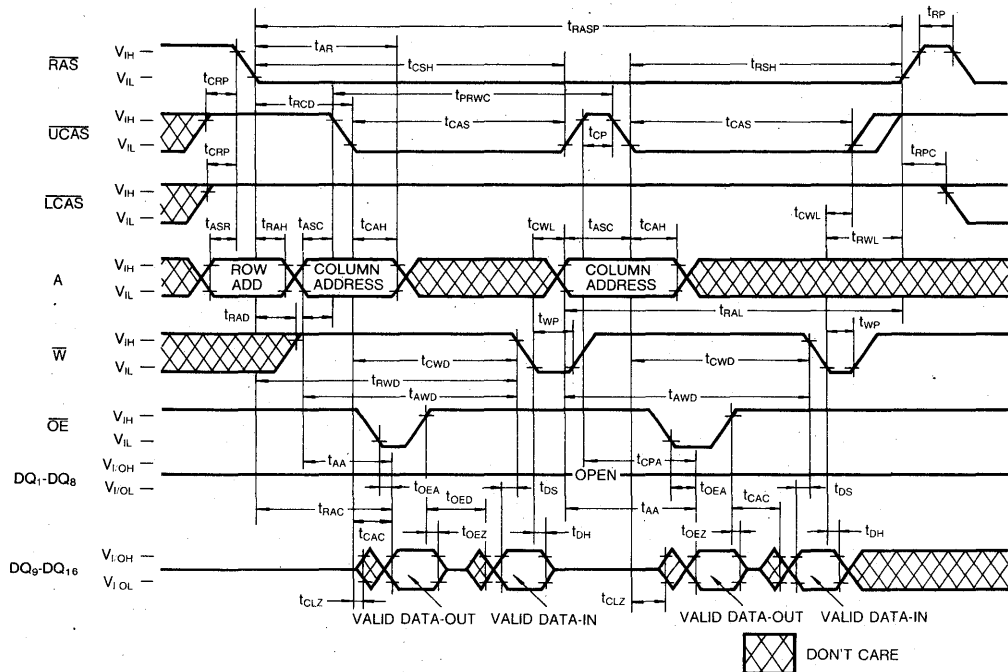
 DONT CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



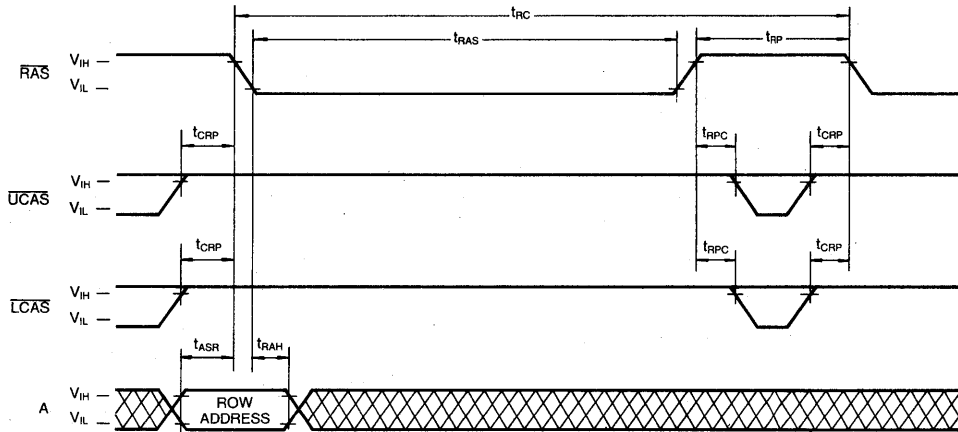
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



TIMING DIAGRAMS (Continued)

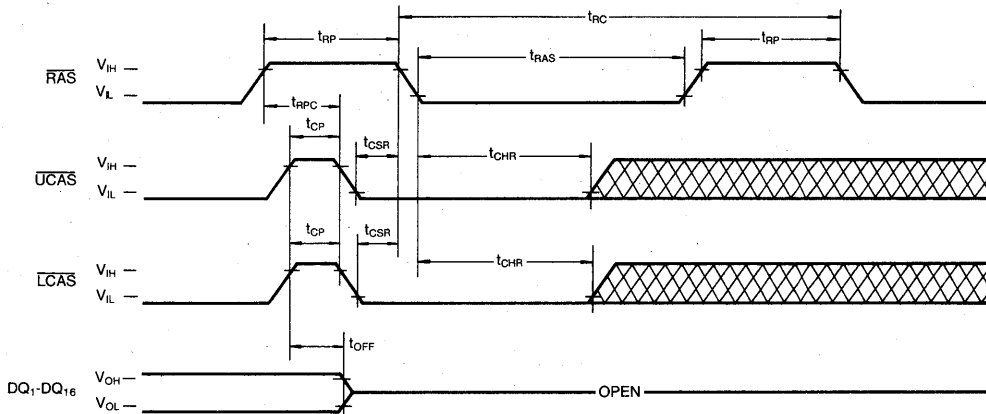
RAS ONLY REFRESH CYCLE


NOTE: \bar{W} , \bar{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

NOTE: $\bar{W}=V_{IH}$, \bar{OE} , A=Don't Care

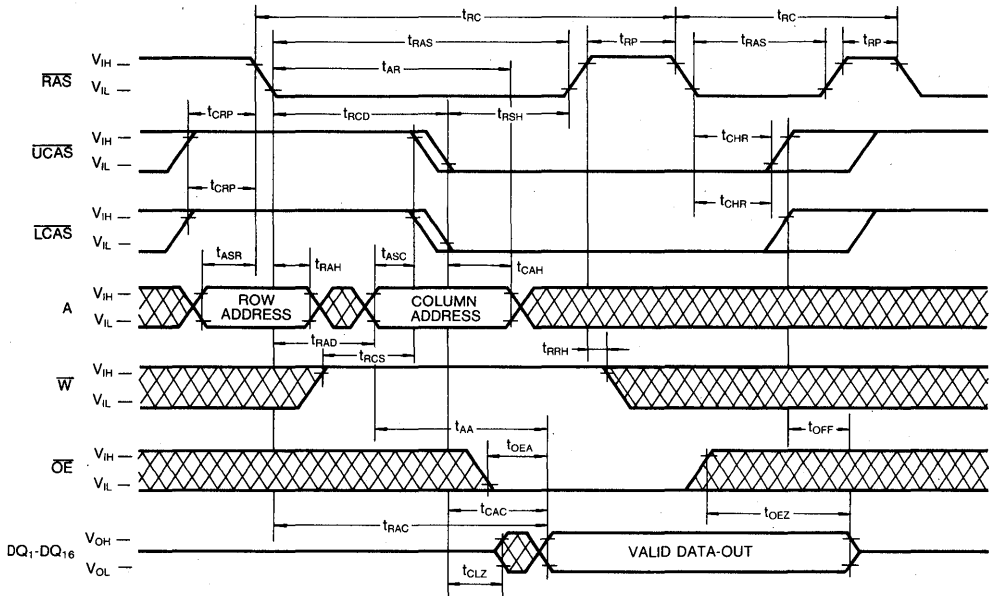


 DON'T CARE

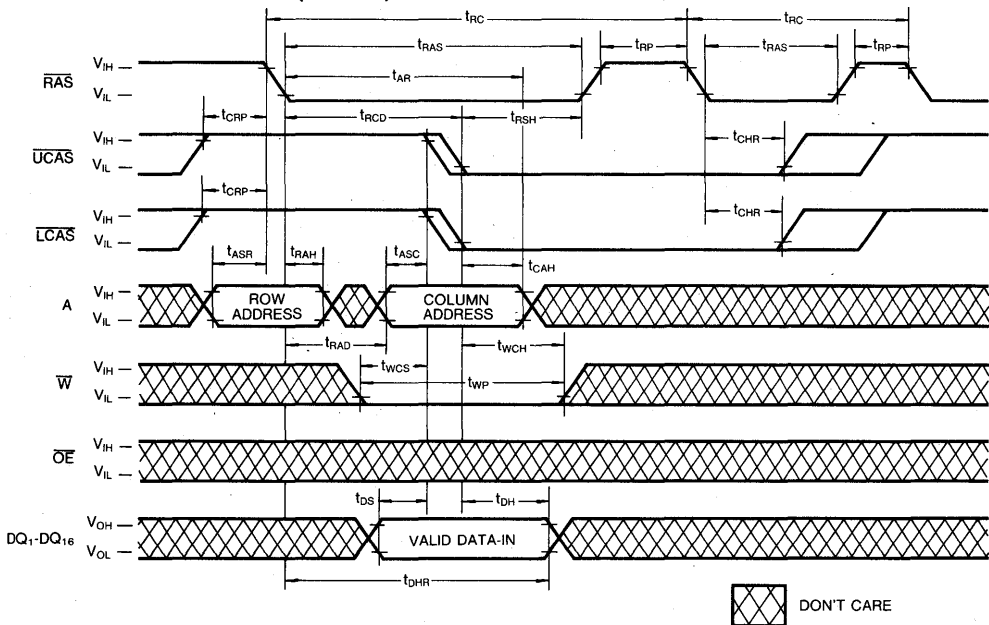
6

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

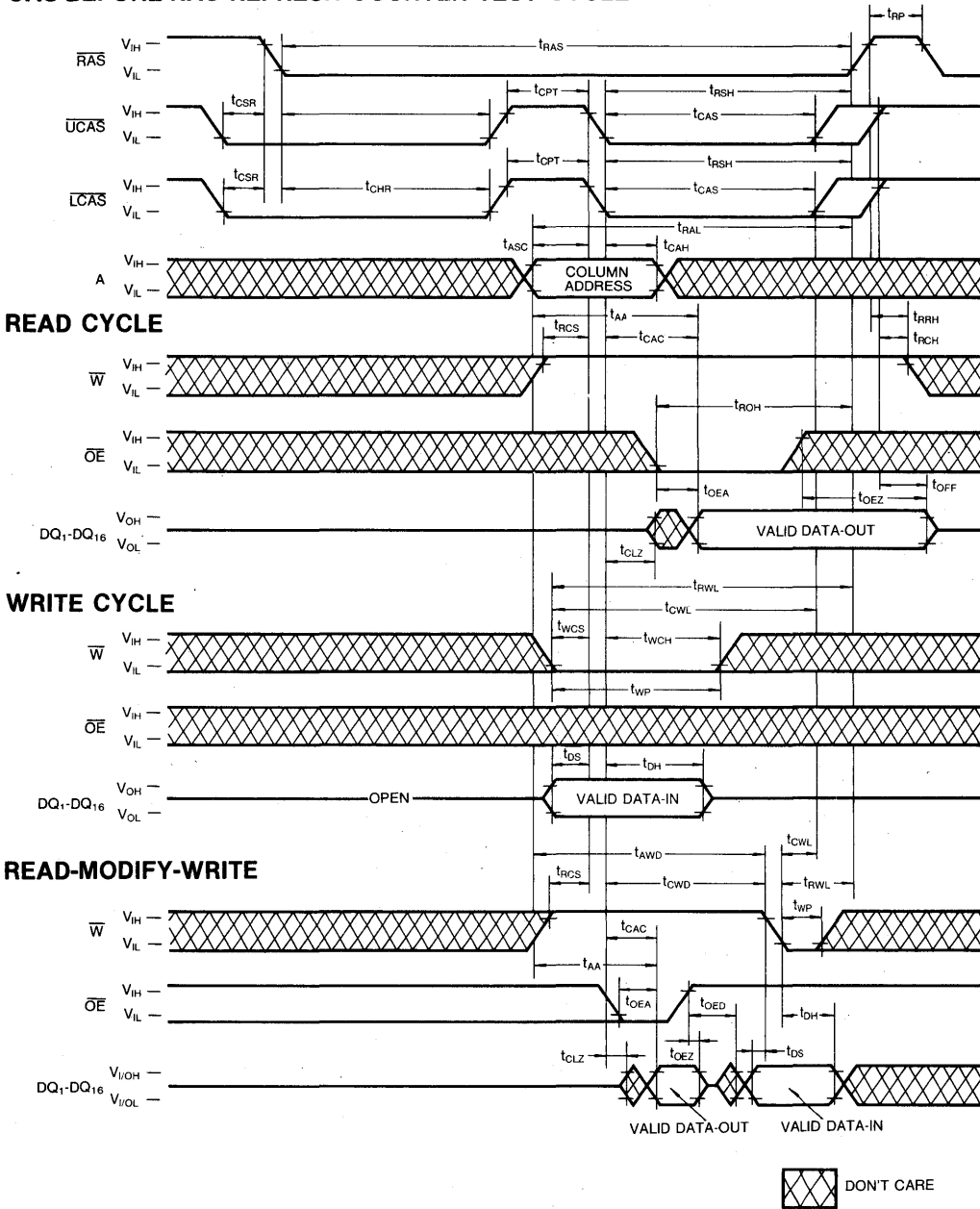


HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE

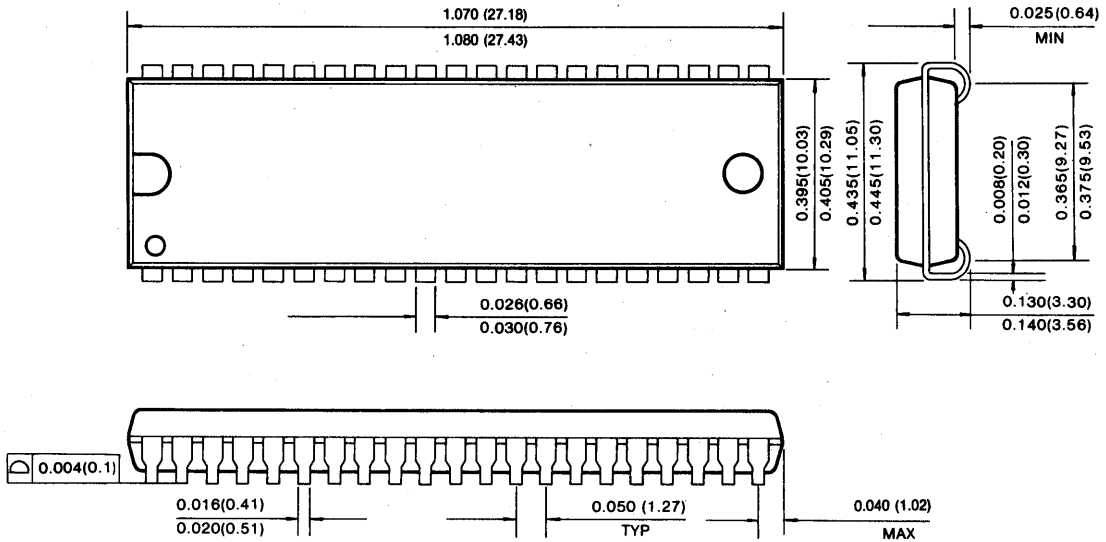


6

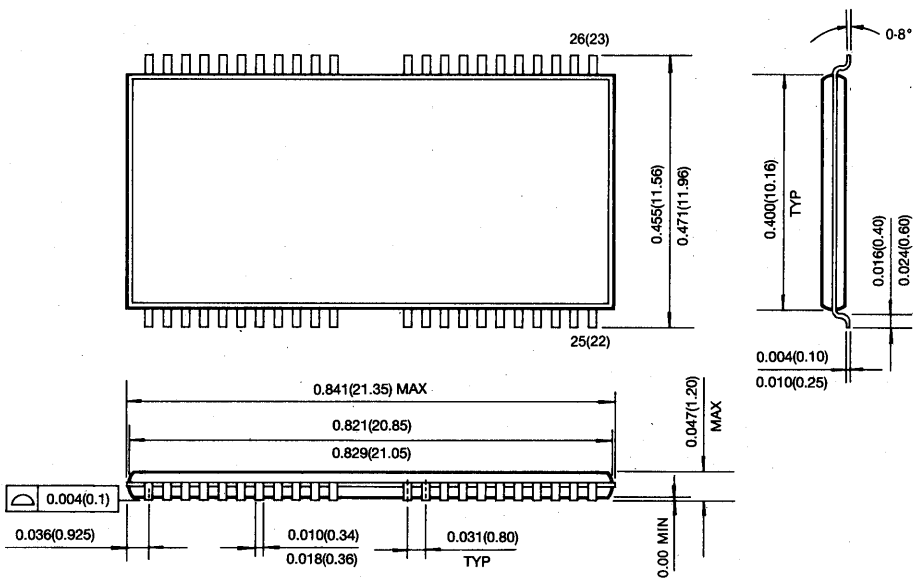
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{TRC}	t _{HPC}
KM416C1004A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416C1004A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416C1004A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- Extended Data Out Mode
(Fast Page Mode with Extended Data Out)
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +5V ± 10% power supply
- Refresh Cycle
 - 4096 cycle/64ms (Normal)
 - 4096 cycle/128ms (L-version)
 - 4096 cycle/128ms (F-version)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

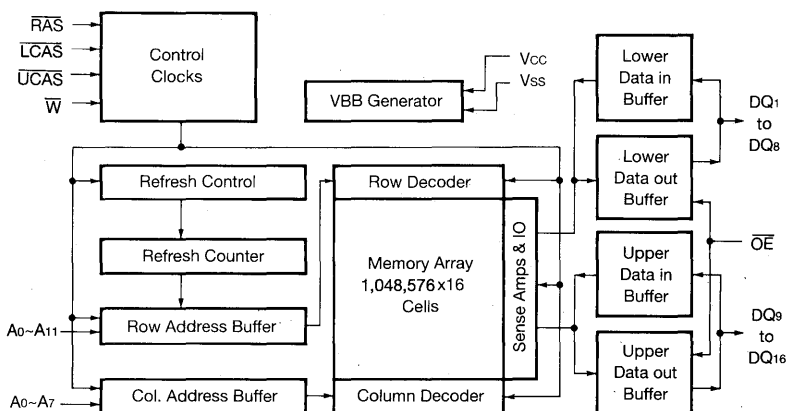
GENERAL DESCRIPTION

The Samsung KM416C1004A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

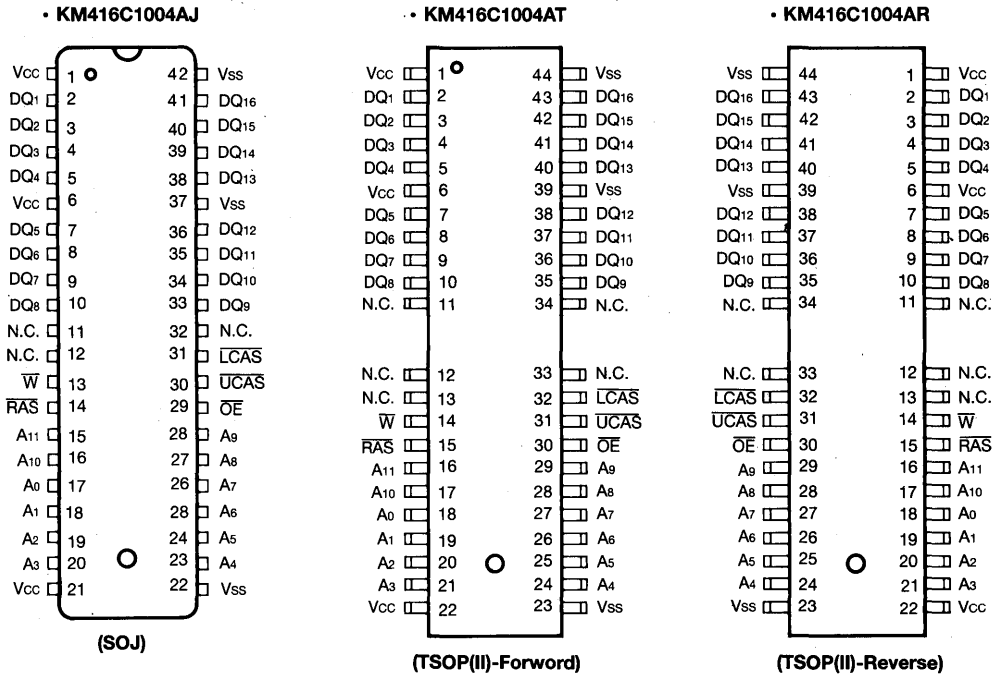
The KM416C1004A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1004A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
\bar{RAS}	Row Address Strobe
\bar{UCAS}	Upper Column Address Strobe
\bar{LCAS}	Lower Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
Vcc	Power(+5V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-1 to + 7.0	V
Voltage on V _{CC} Supply Relative to V _{SS}	V _{CC}	-1 to + 7.0	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @trc=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I _{CC1}	-	100 90 80	mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=V_{IH}$)	KM416C1004A KM416C1004A-L KM416C1004A-F	I _{CC2}	-	2 1 1	mA mA mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\overline{\text{UCAS}}=\overline{\text{LCAS}}=V_{IH}$, $\overline{\text{RAS}}$, Address Cycling @trc=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I _{CC3}	-	100 90 80	mA mA mA
EDO Mode Current* ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @tpc=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I _{CC4}	-	120 110 100	mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=V_{CC}-0.2V$)	KM416C1004A KM416C1004A-L KM416C1004A-F	I _{CC5}	-	1 300 200	mA μA μA
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ Cycling @trc=min.)	KM416C1004A-6/A-L6/A-F6 KM416C1004A-7/A-L7/A-F7 KM416C1004A-8/A-L8/A-F8	I _{CC6}	-	100 90 80	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V, Input Low Voltage(V _{IL})=0.2V $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}=0.2V$ D _{IN} =Don't Care, trc=31.25μs (L-Ver) tr _{AS} =tr _{AS} min~300ns	KM416C1004A-L	I _{CC7}	-	450	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current $\overline{RAS}=\overline{UCAS}=\overline{LCAS}=0.2V$ $W=\overline{OE}=A_0-A_{11}=V_{CC}-0.2V$ or $0.2V$ $DQ_1-DQ_{16}=V_{CC}-0.2V$ or $0.2V$ or Open	lccs	-	250	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 V)	li(L)	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{out} \leq V_{CC}$)	lo(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: lcc1, lcc3, lcc4 and lcc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. lcc is specified as an average current. In lcc1 and lcc3, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In lcc4, Address can be changed maximum once while one Hyper page mode cycle time tHPC.

CAPACITANCE ($T_A=25^\circ C$, $V_{CC}=5V$, $f=1MHz$)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (\overline{RAS} , \overline{LCAS} , \overline{UCAS} , W, \overline{OE})	CIN2	-	7	pF
Output Capacitance (DQ1-DQ16)	CDO	-	7	pF

AC CHARACTERISTICS ($0^\circ C \leq T_A \leq 70^\circ C$, $V_{CC}=5V \pm 10\%$, See notes 1,2)

(Test condition : $V_{IH}/V_{IL}=2.4V/0.8V$, $V_{OH}/V_{OL}=2.0V/0.8V$, Output Loading $C_L=100pF$)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from \overline{RAS}	trac		60		70		80	ns	3,4,11
Access time from \overline{CAS}	tcac		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	tCLZ	3		3		3		ns	3
\overline{OE} to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	tCEZ	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	tr	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	trp	40		50		60		ns	
\overline{RAS} pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	trSH	17		20		20		ns	
\overline{CAS} hold time	tCSH	50		60		70		ns	
\overline{CAS} pulse width	tcAS	10	10,000	15	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	trCD	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{RAS} to column address delay time	tRAD	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to \overline{RAS}	tAR	45		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to \overline{RAS}	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to \overline{RAS} lead time	tRWL	15		20		20		ns	
Write command to \overline{CAS} lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to \overline{RAS}	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
\overline{CAS} to \overline{W} delay time	tCWD	40		50		50		ns	8,17
\overline{RAS} to \overline{W} delay time	tRWD	85		95		105		ns	8
Column address to \overline{W} delay time	tAWD	55		60		65		ns	8
\overline{CAS} precharge to \overline{W} delay time	tCPWD	60		65		70		ns	
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	19
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		10		ns	20
\overline{RAS} precharge to \overline{CAS} hold time	tRPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} -B- \overline{R} counter test cycle)	tCPT	20		25		30		ns	
\overline{RAS} hold time referenced to \overline{OE}	tROH	15		20		20		ns	
\overline{OE} access time	tOEA		15		20		20	ns	
\overline{OE} to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	3	15	3	20	3	20	ns	7
\overline{OE} command hold time	tOEH	15		20		20		ns	
Access time from \overline{CAS} precharge	tCPA		35		40		45	ns	3

6



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
CAS orgcharge time (Hyper page mode)	tCP	10		10		10		ns	16
RAS pulse width (Hyper page mode)	tRASP	60	200.000	70	200.000	80	200.000	ns	
RAS hold time from CAS precharge	tRHCP	35		40		45		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from W	tWEZ	3	15	3	20	3	20	ns	7
W to data delay	tWED	15		20		20		ns	
OE to CAS hold time	tOCH	5		5		5		ns	
CAS hold time to OE	tCHO	5		5		5		ns	
OE precharge time	tOEP	5		5		5		ns	
W pulse width	tWPE	5		5		5		ns	
RAS pulse width (F-ver)	tRASS	100		100		100		μ s	13
RAS precharge time (F-ver)	tRPS	110		130		150		ns	13
CAS hold time (F-ver)	tCHS	-50		-50		-50		ns	13

KM416C1004A/A-L/A-F Truth Table

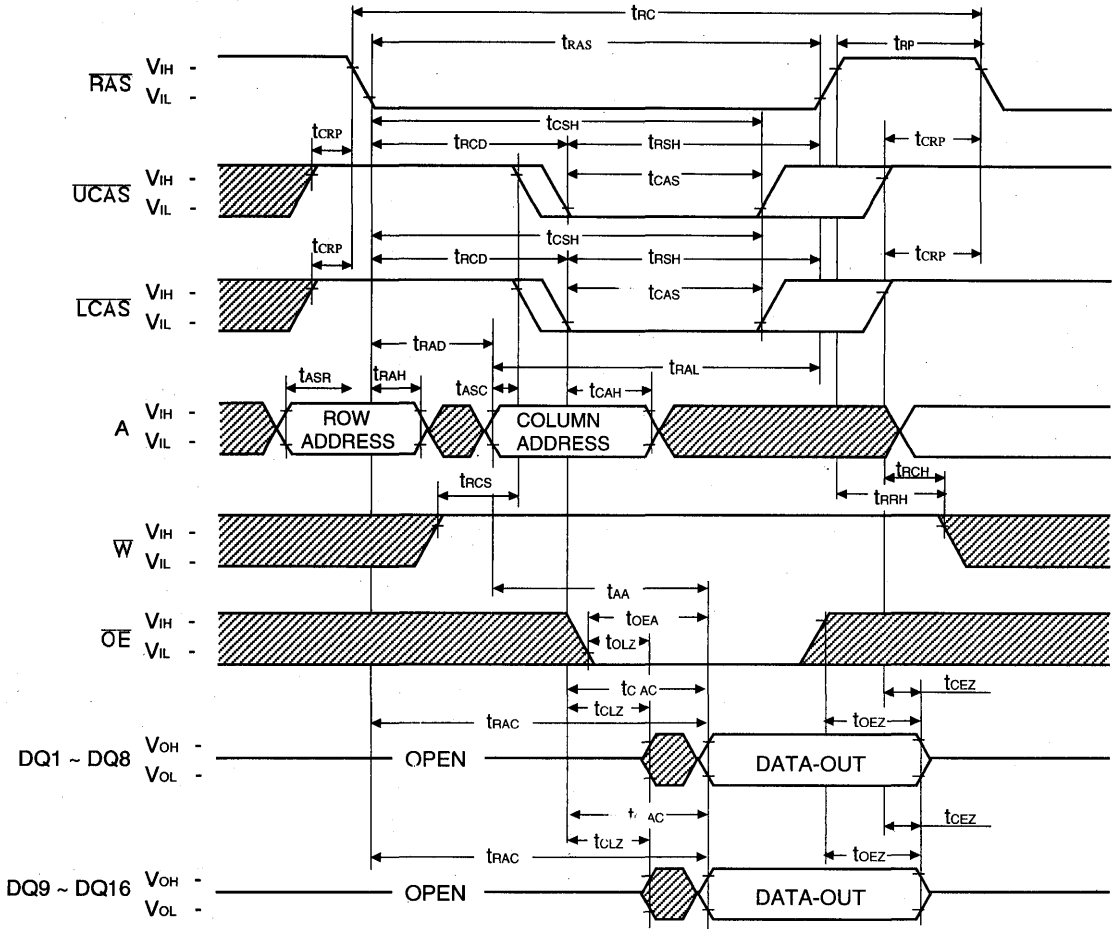
RAS	LCAS	UCAS	W	OE	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL Loads and 100pF
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWd} , t_{CWD} and t_{AWd} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWd} \geq t_{RWd}(\min)$ and $t_{AWd} \geq t_{AWd}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. $t_{ASC} \geq t_{CP} \min$, Assume $t_T = 2.0ns$.
13. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
15. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
16. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
17. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
19. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
20. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.
21. t_{DS} , t_{DH} is independetly specified for lower byte $D_{in}(1-8)$, upper byte $D_{in}(9-16)$.

TIMING DIAGRAM
WORD READ CYCLE

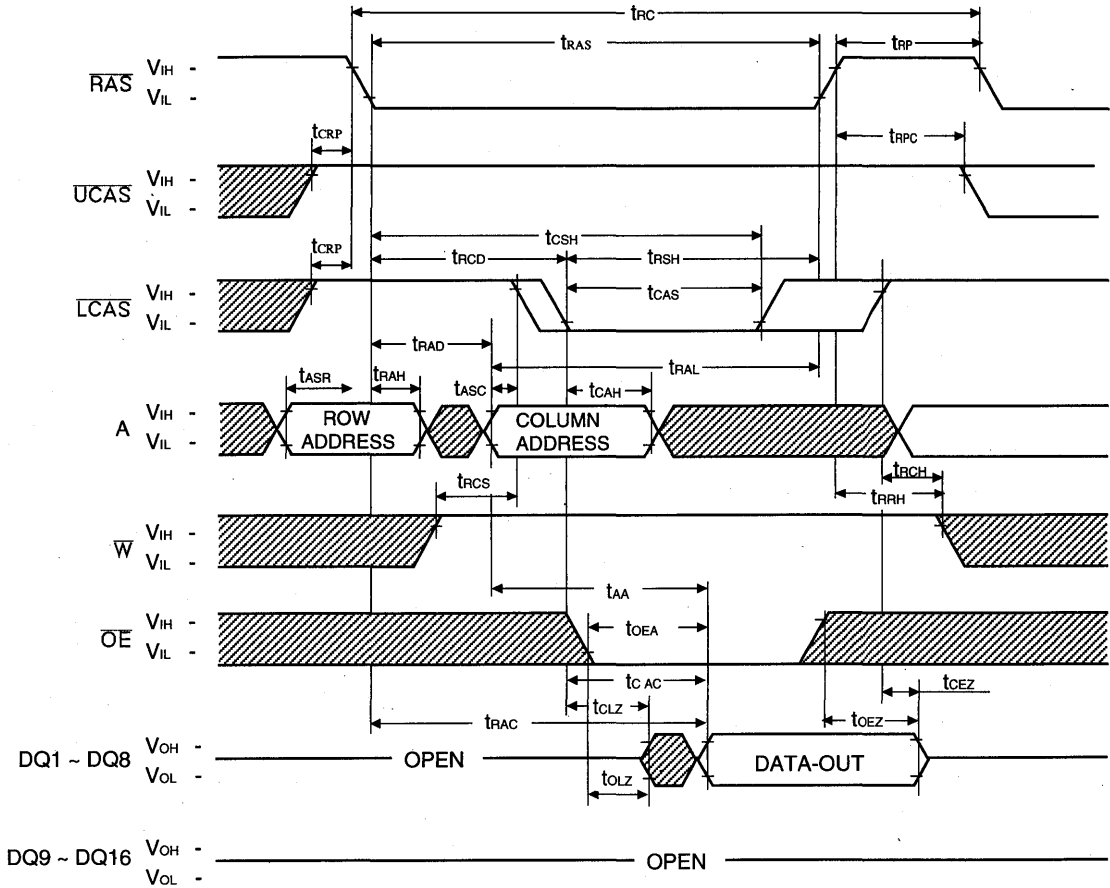
NOTE : D_{IN} = OPEN



 Don't Care

TIMING DIAGRAM
LOWER BYTE READ CYCLE

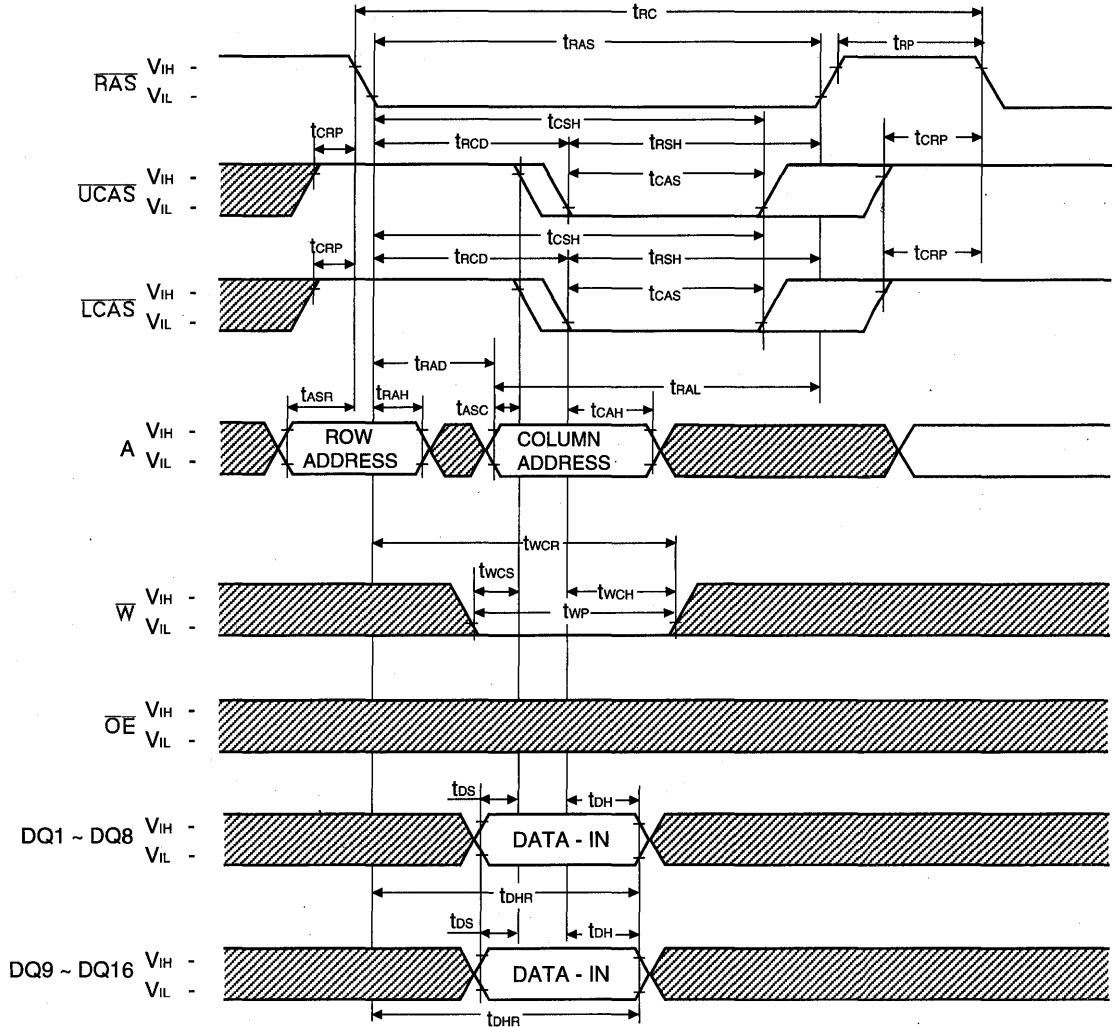
NOTE : D_{IN} = OPEN



 Don't Care

WORD WRITE CYCLE (EARLY WRITE)

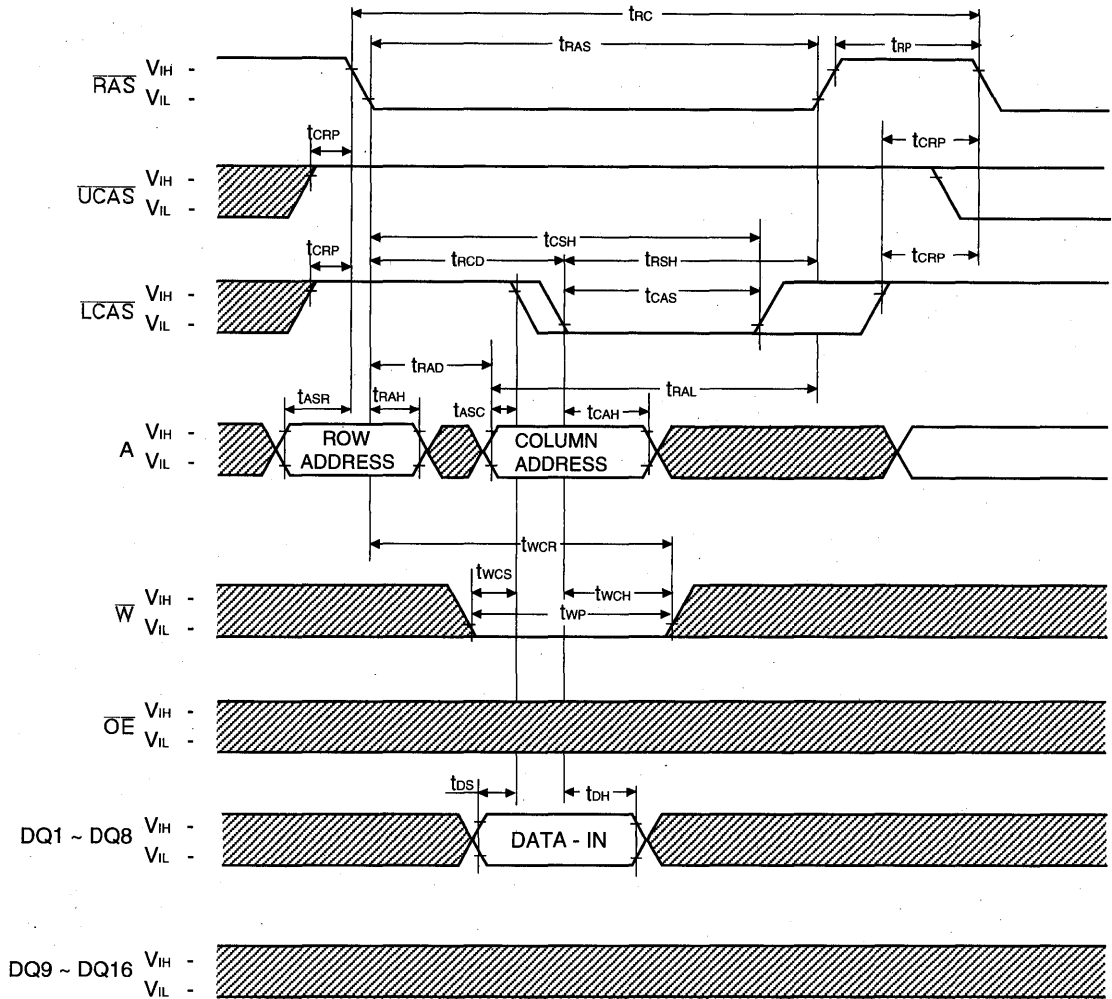
NOTE : DOUT = OPEN



 Don't Care

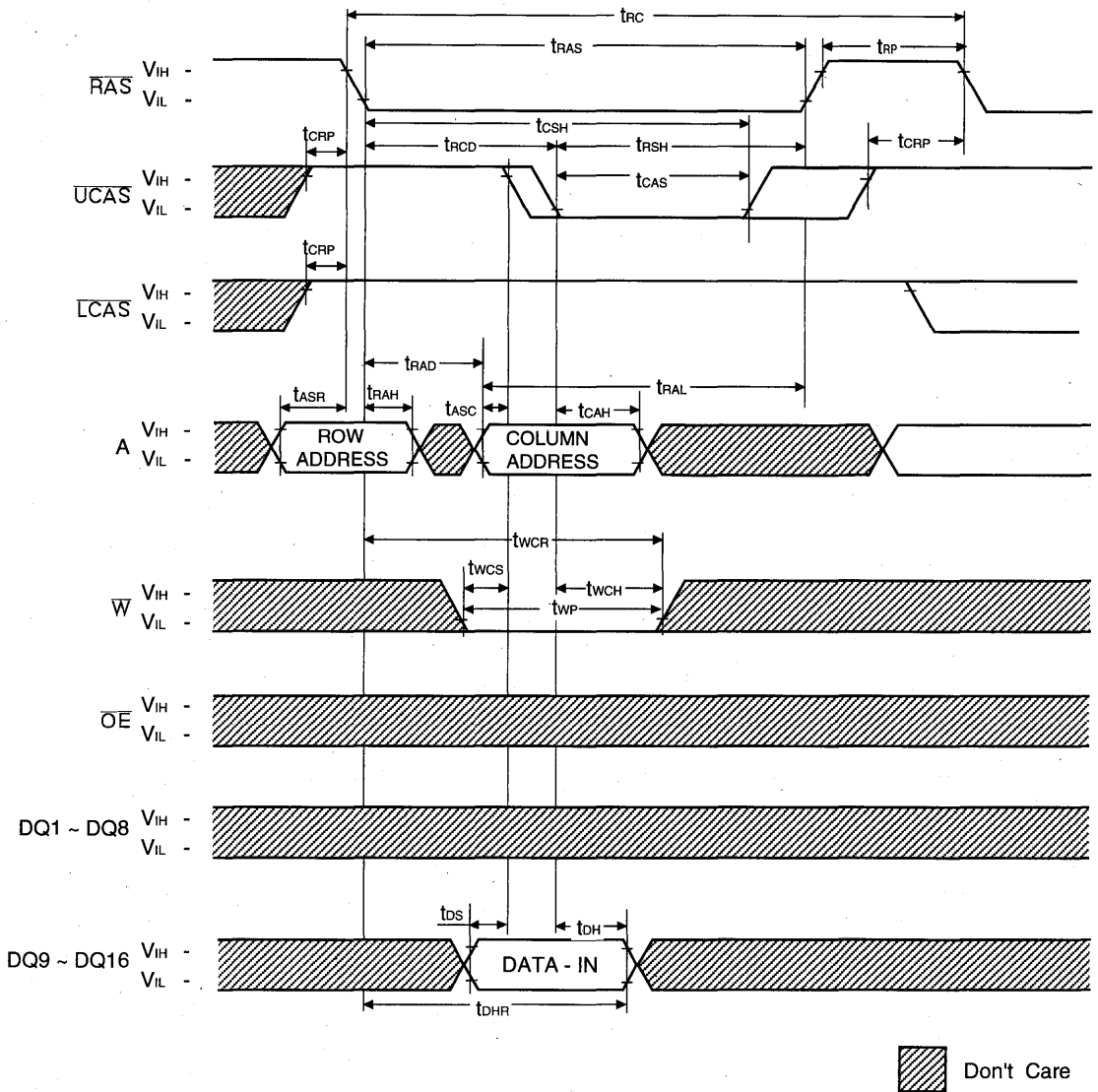
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



UPPER BYTE WRITE CYCLE (EARLY WRITE)

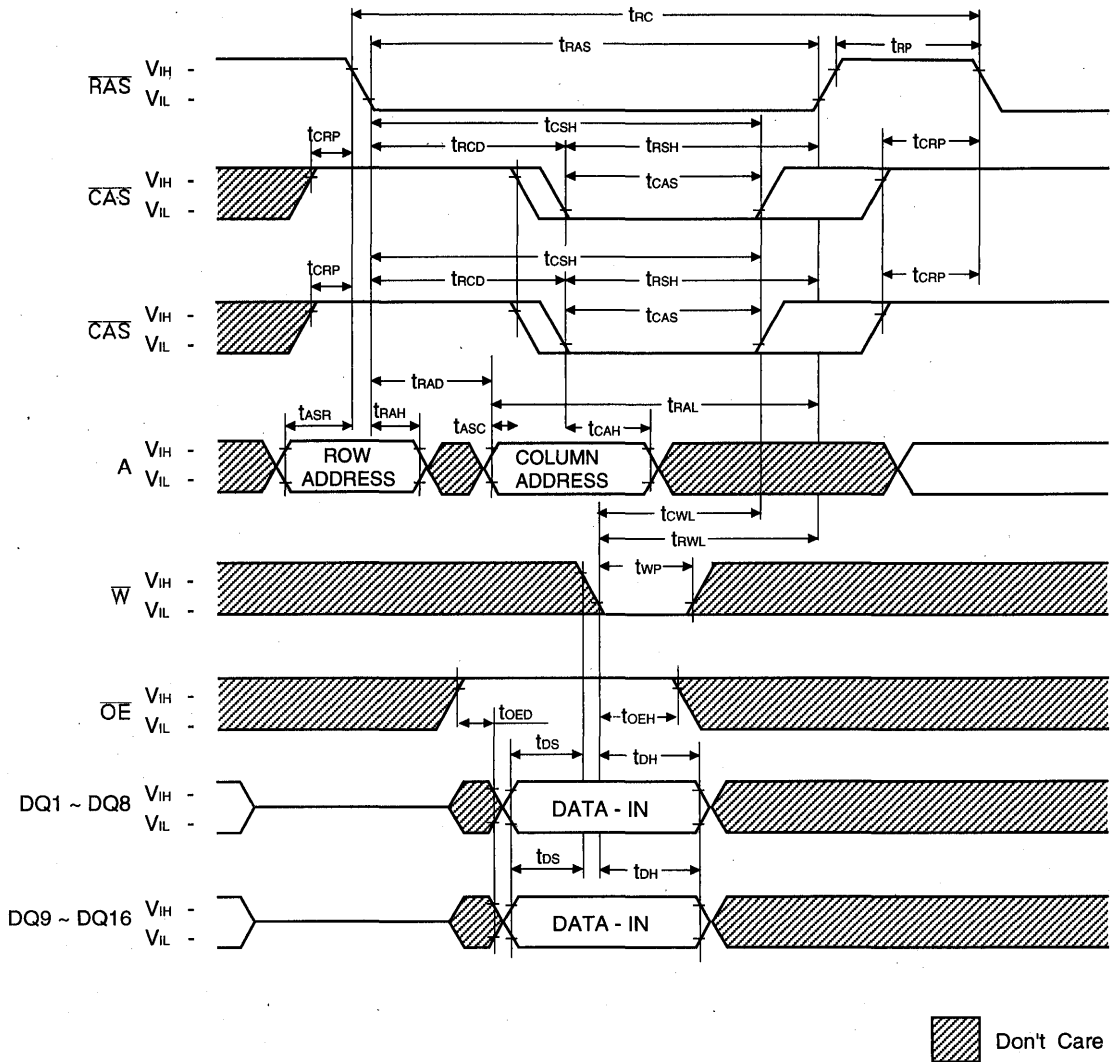
NOTE : D_{OUT} = OPEN



6

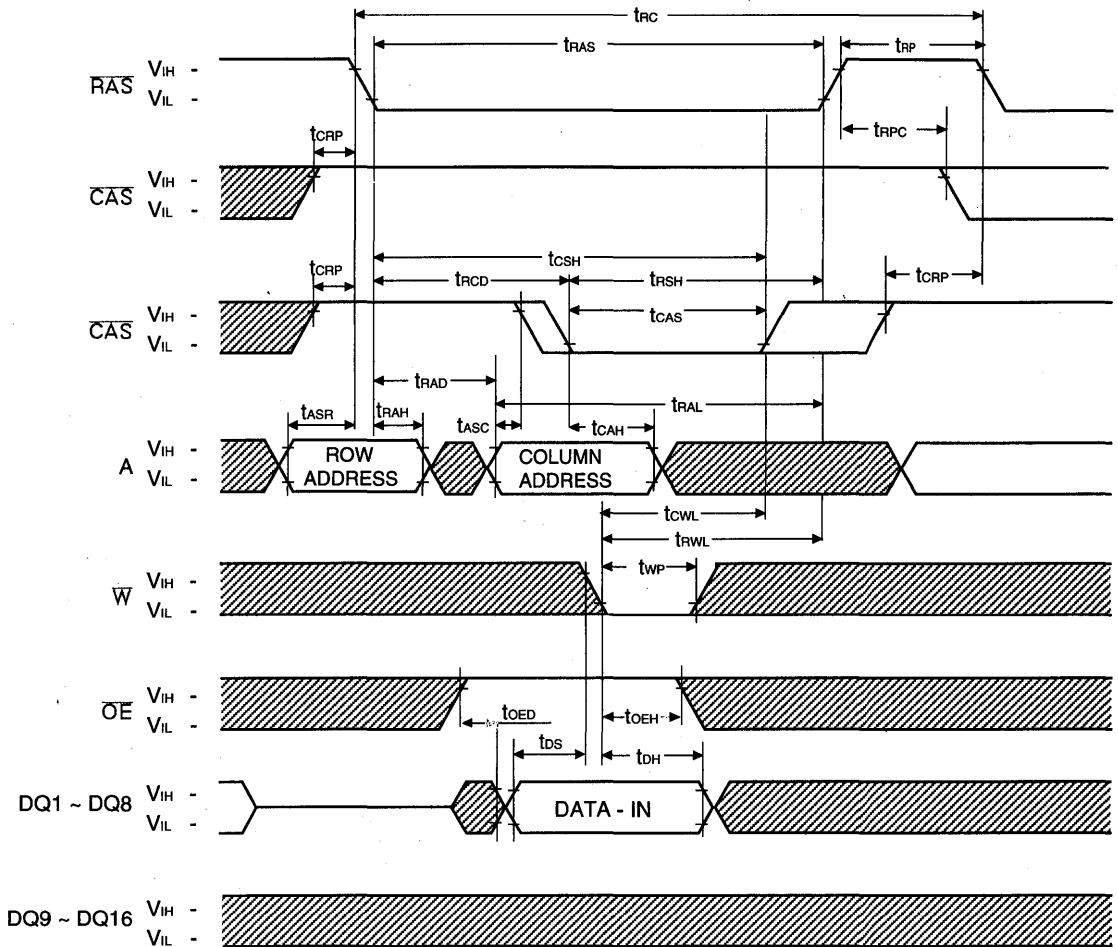
WORD WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : Dout = OPEN

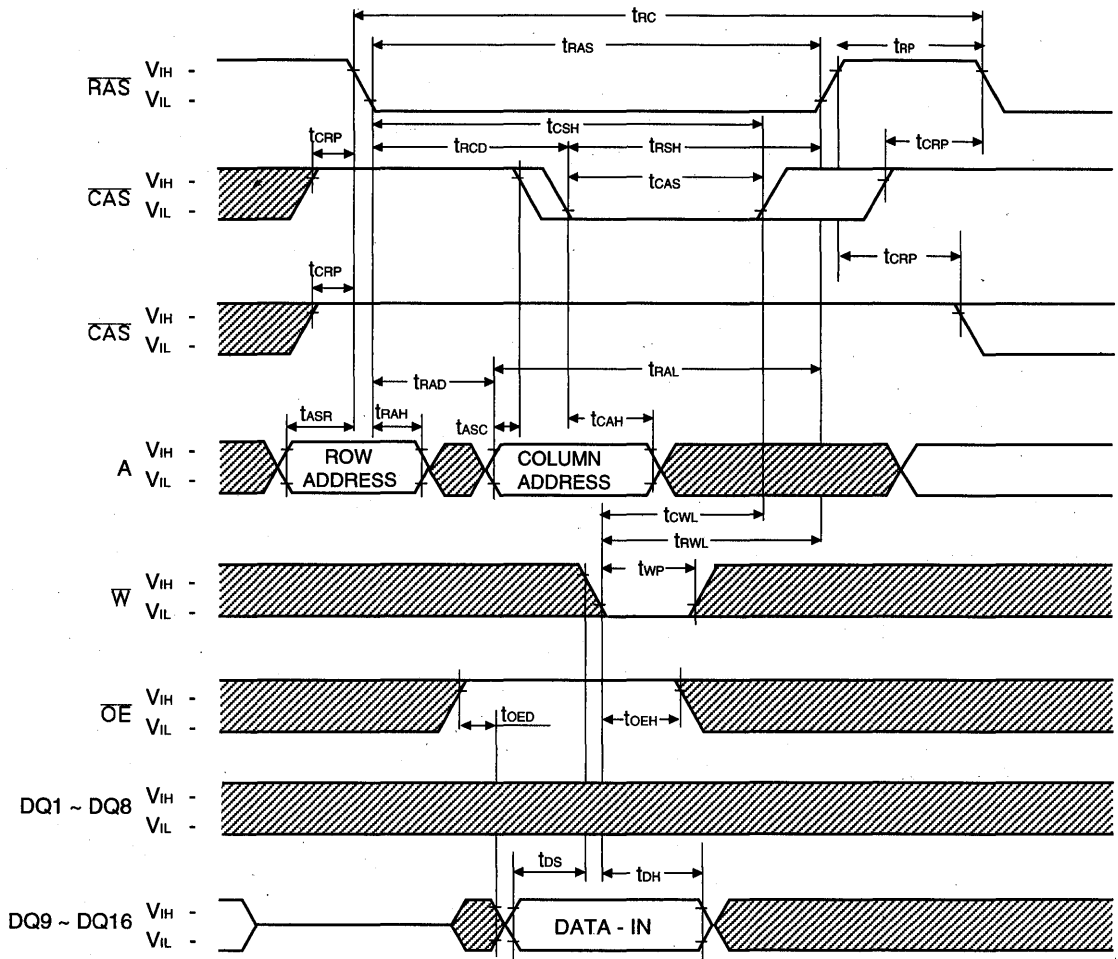


6

 Don't Care

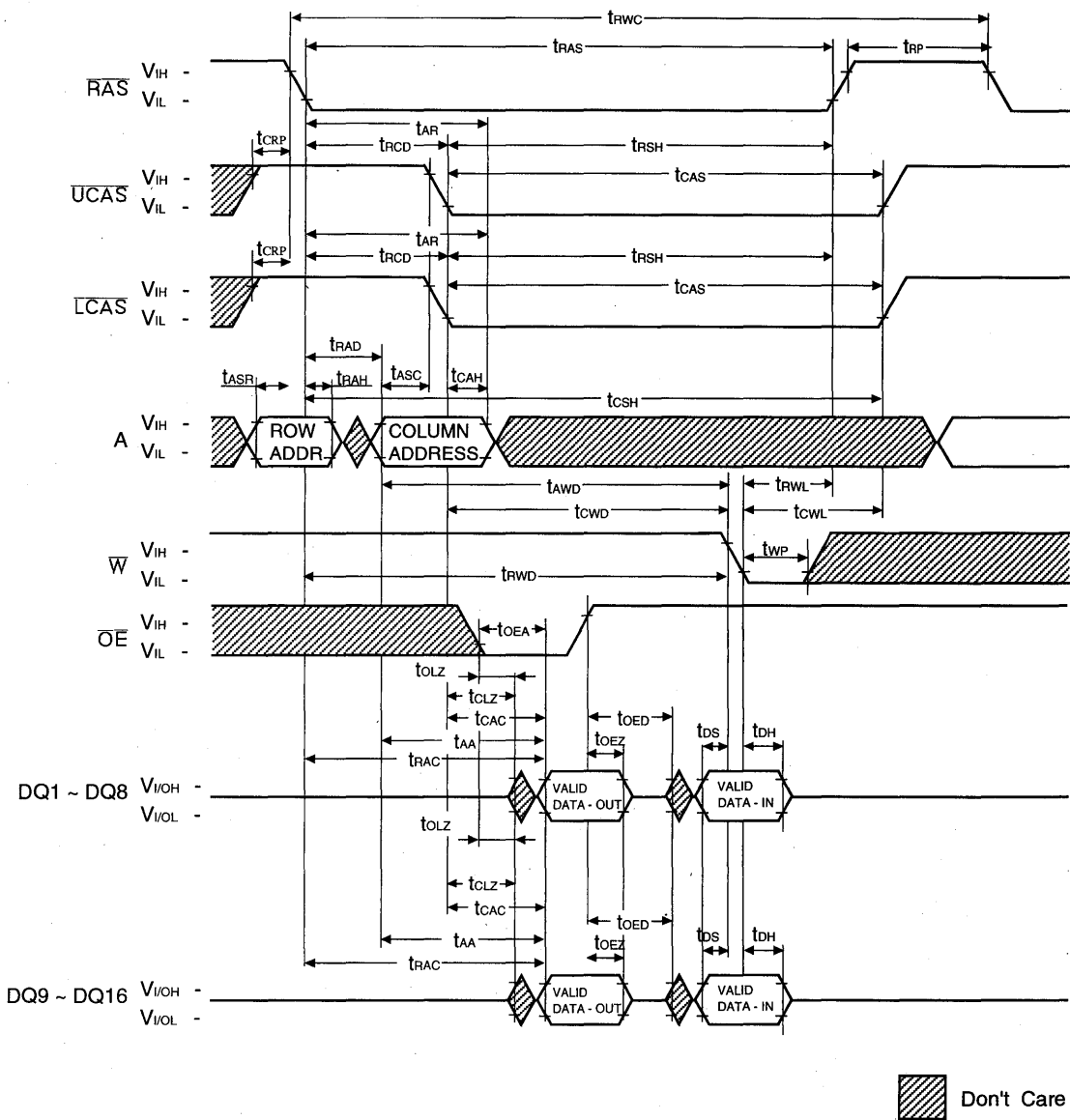
UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



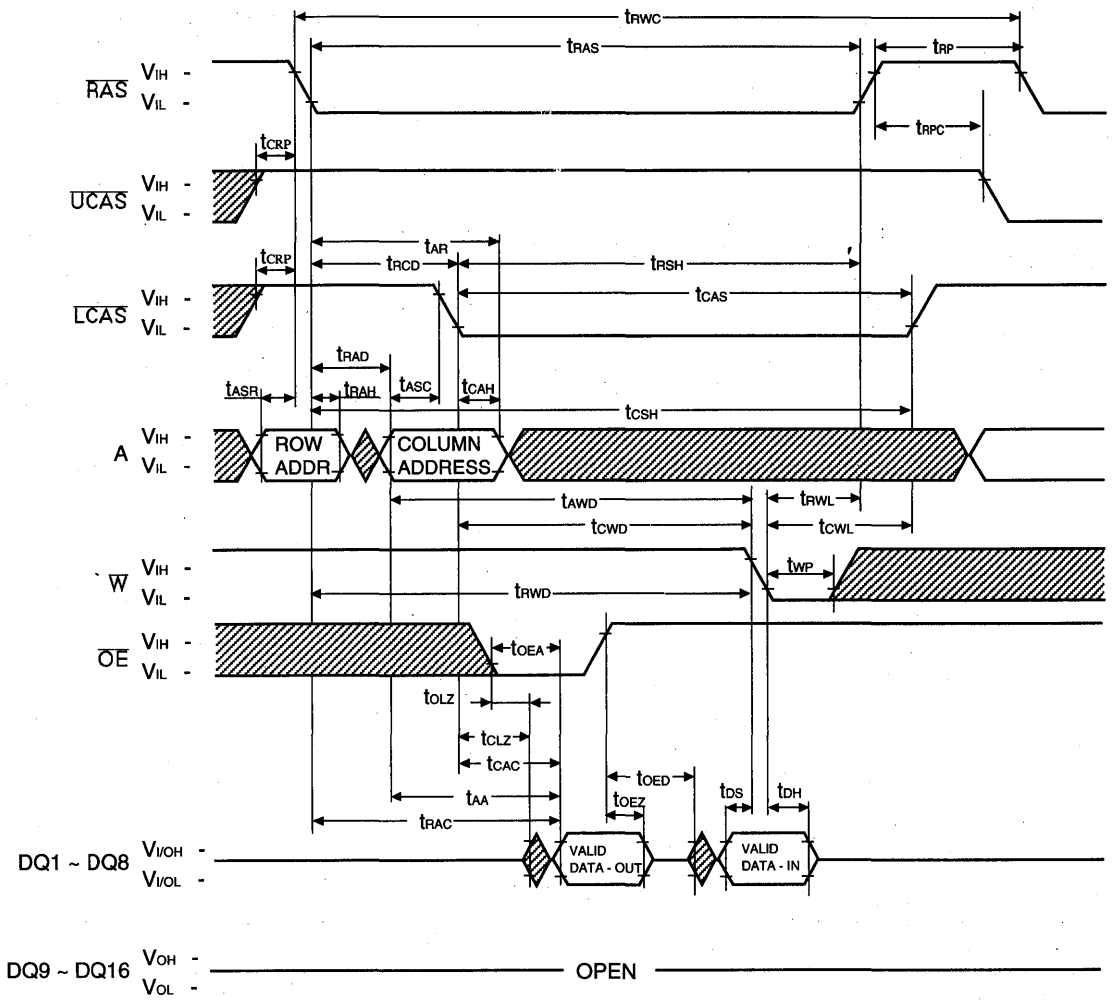
 Don't Care

WORD READ - MODIFY - WRITE CYCLE



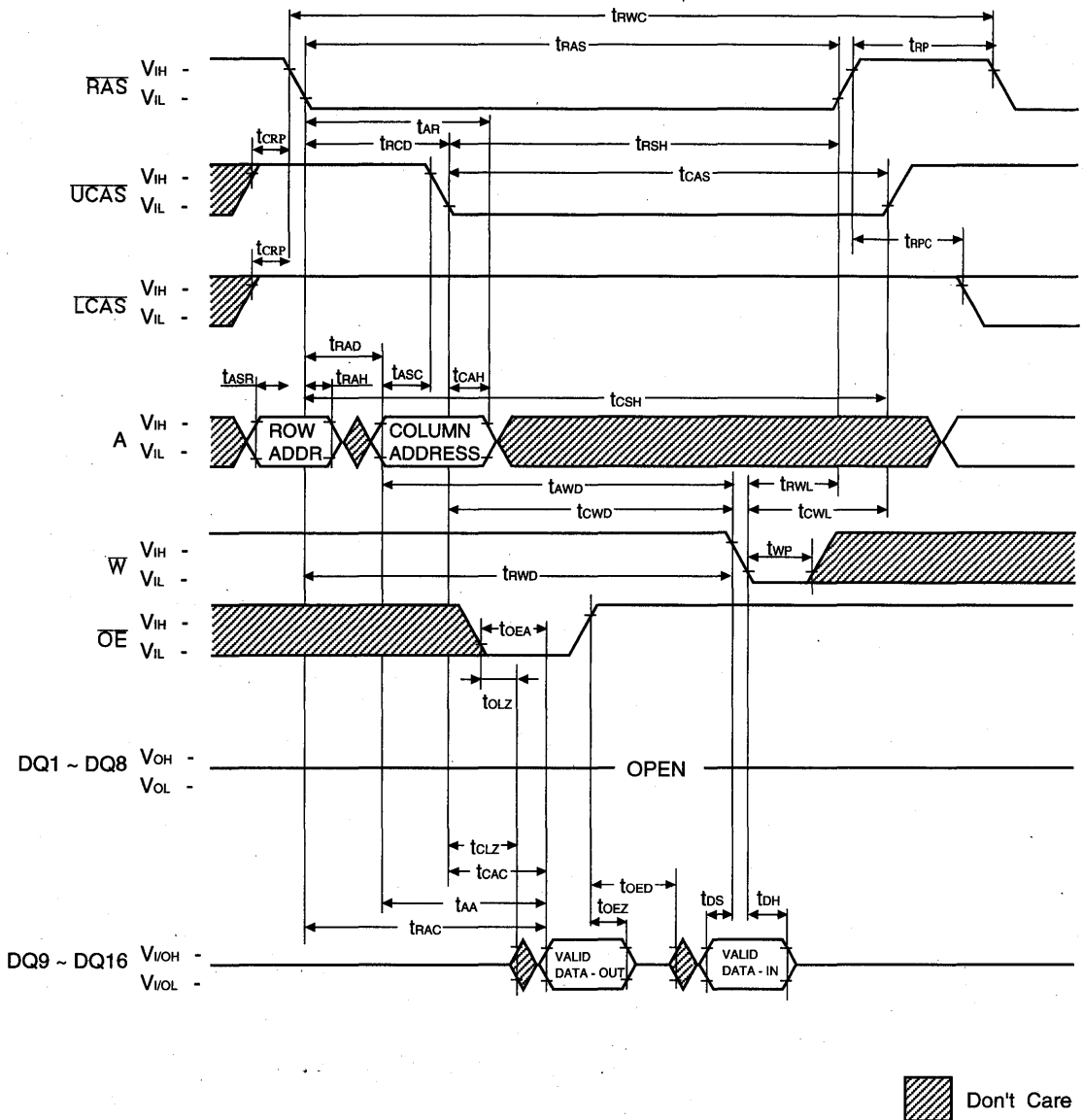
6

LOWER-BYTE READ - MODIFY - WRITE CYCLE

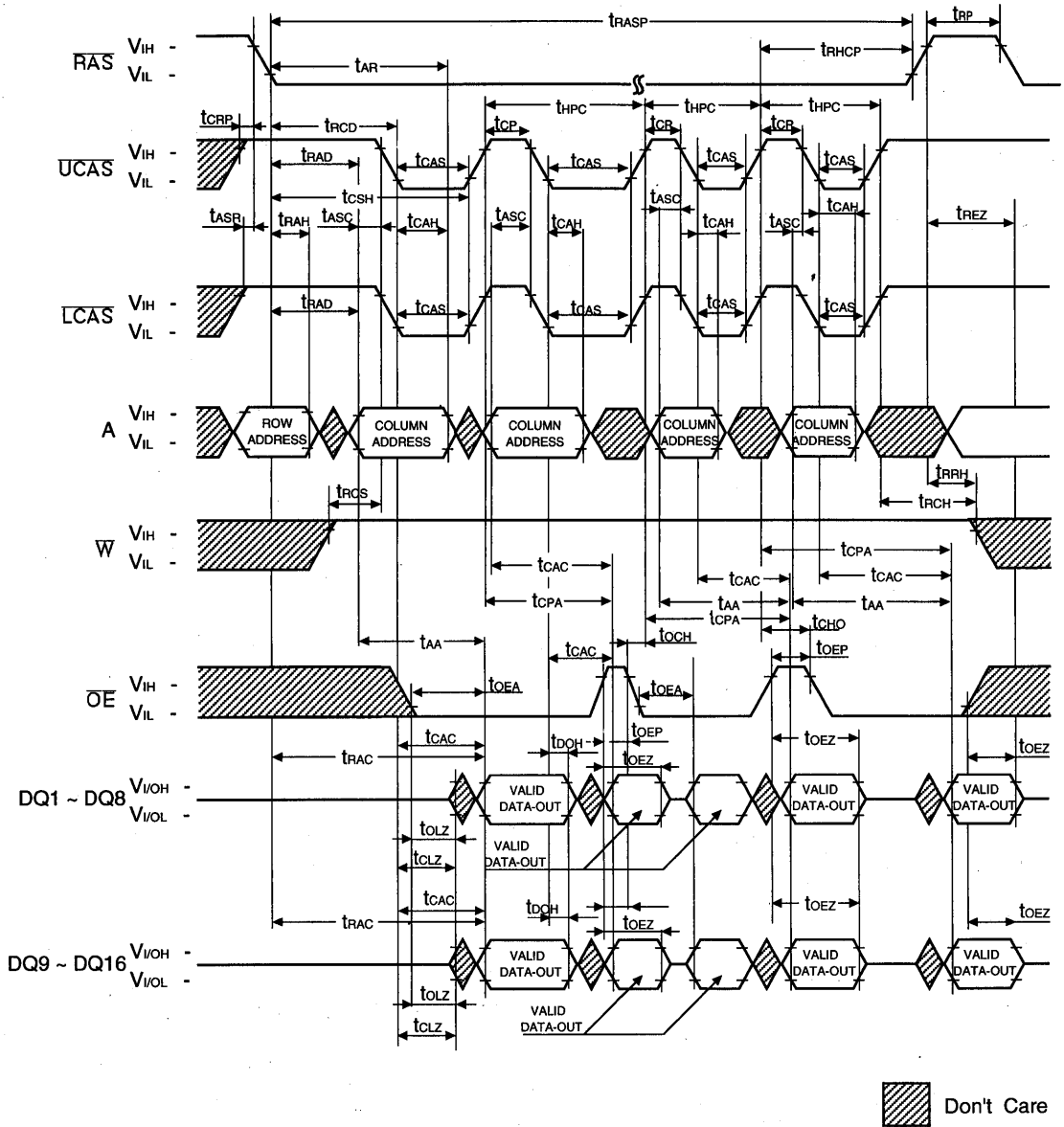


Don't Care

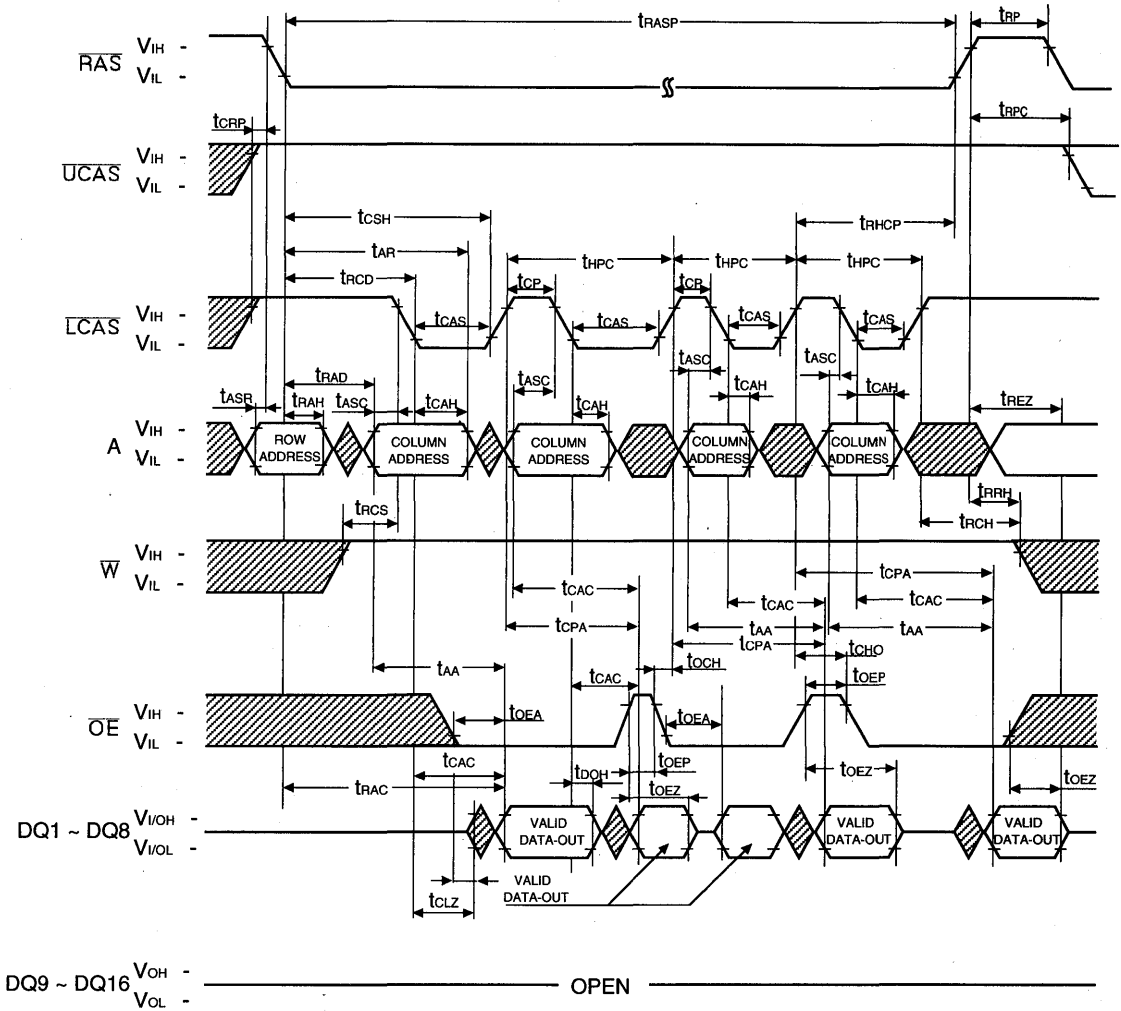
UPPER-BYTE READ - MODIFY - WRITE CYCLE



HYPER PAGE MODE WORD READ CYCLE



HYPER PAGE MODE LOWER BYTE READ CYCLE

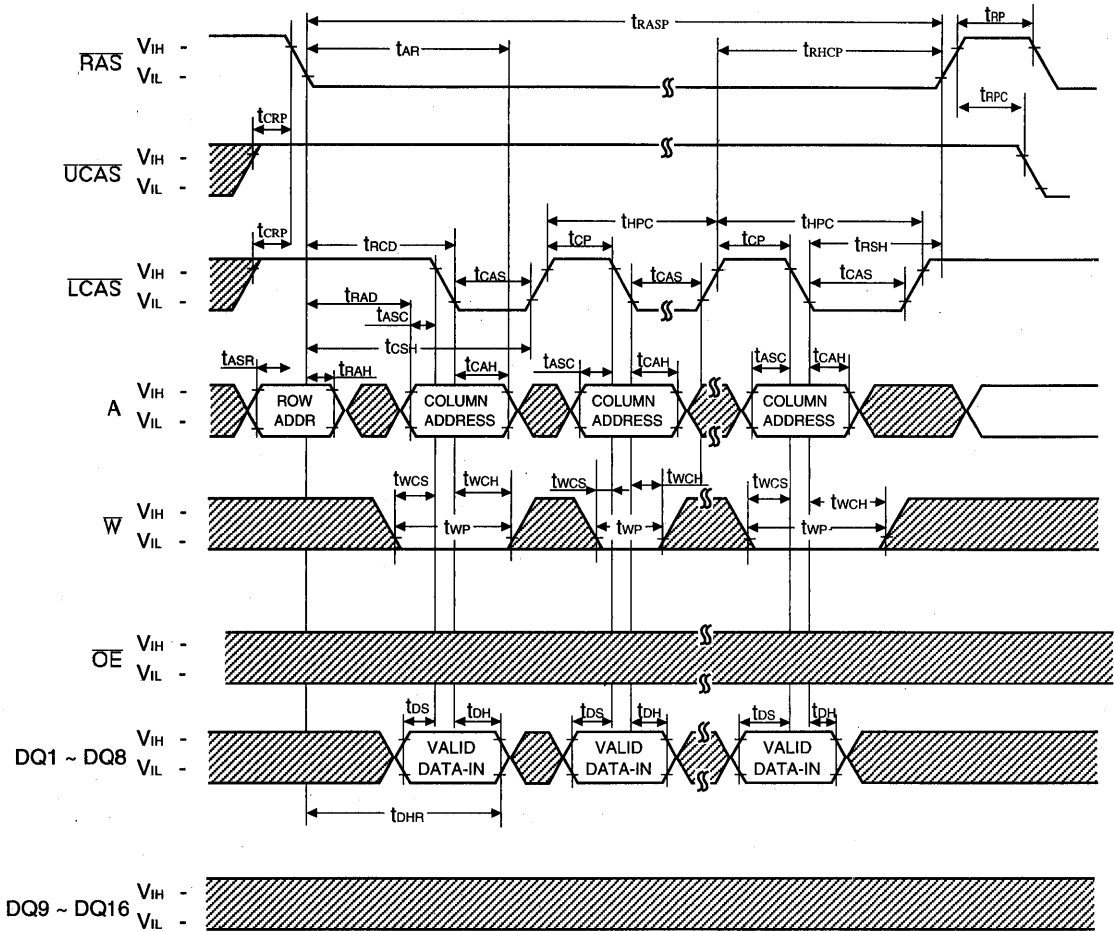


6

Don't Care

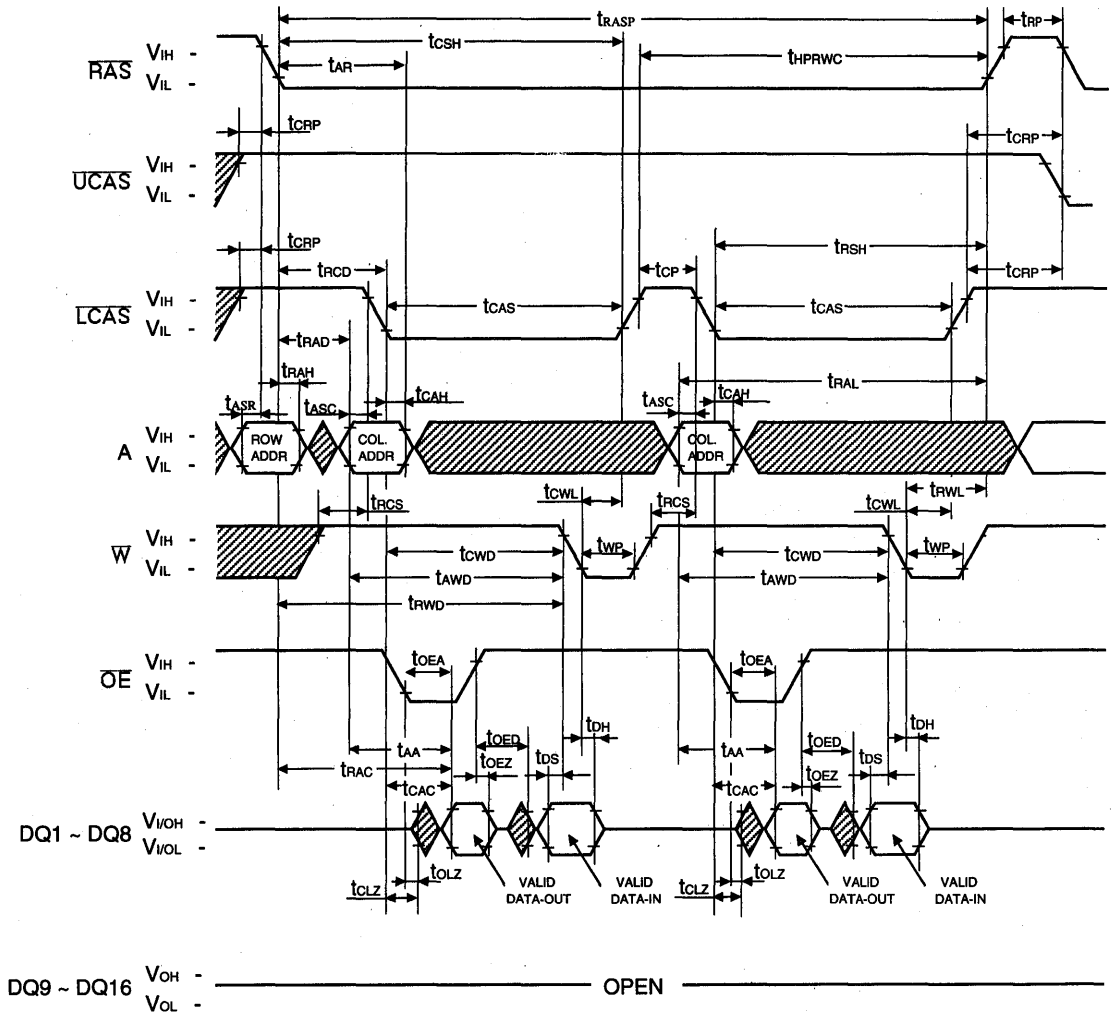
HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open




 Don't Care

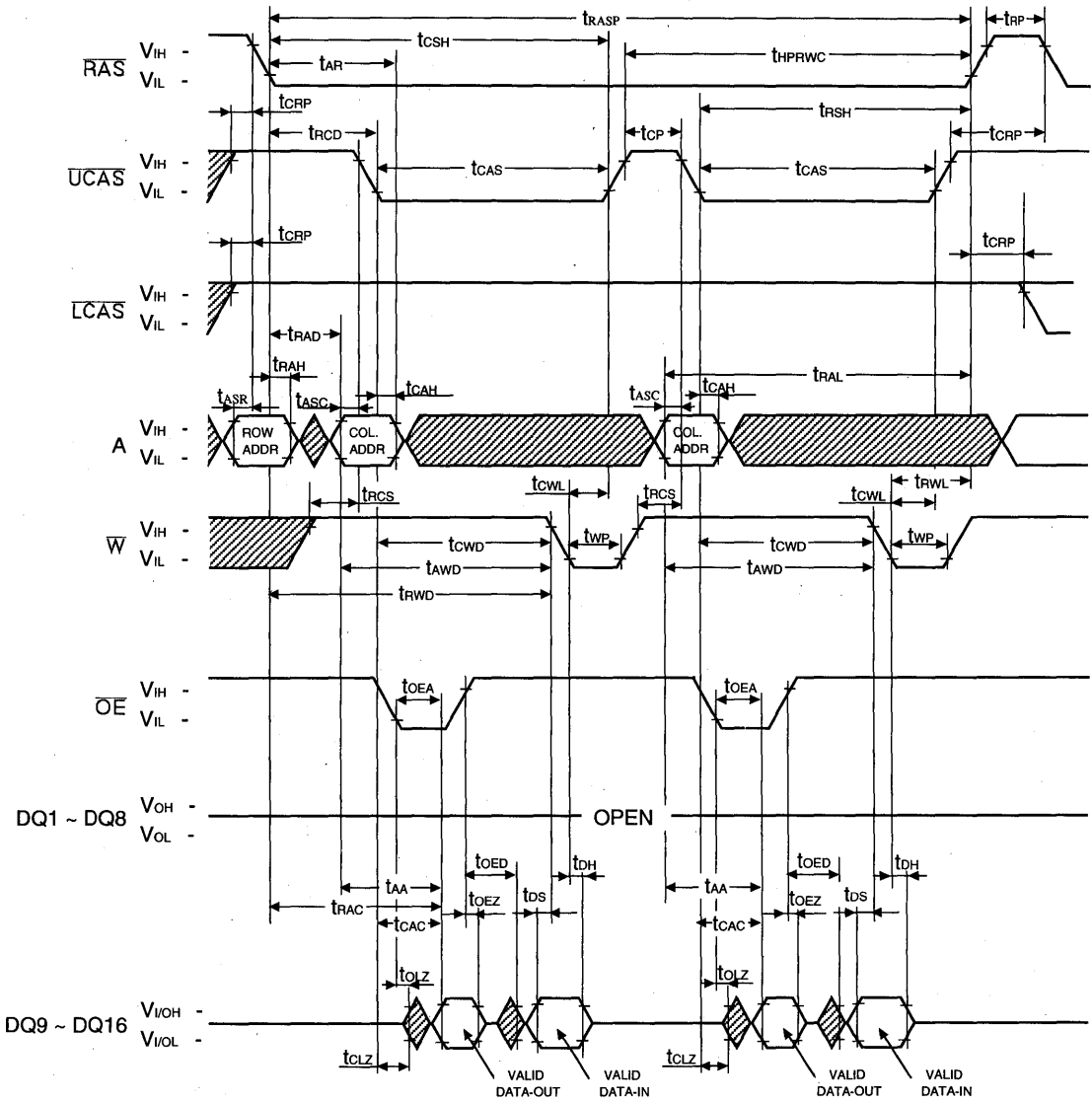
HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE




6

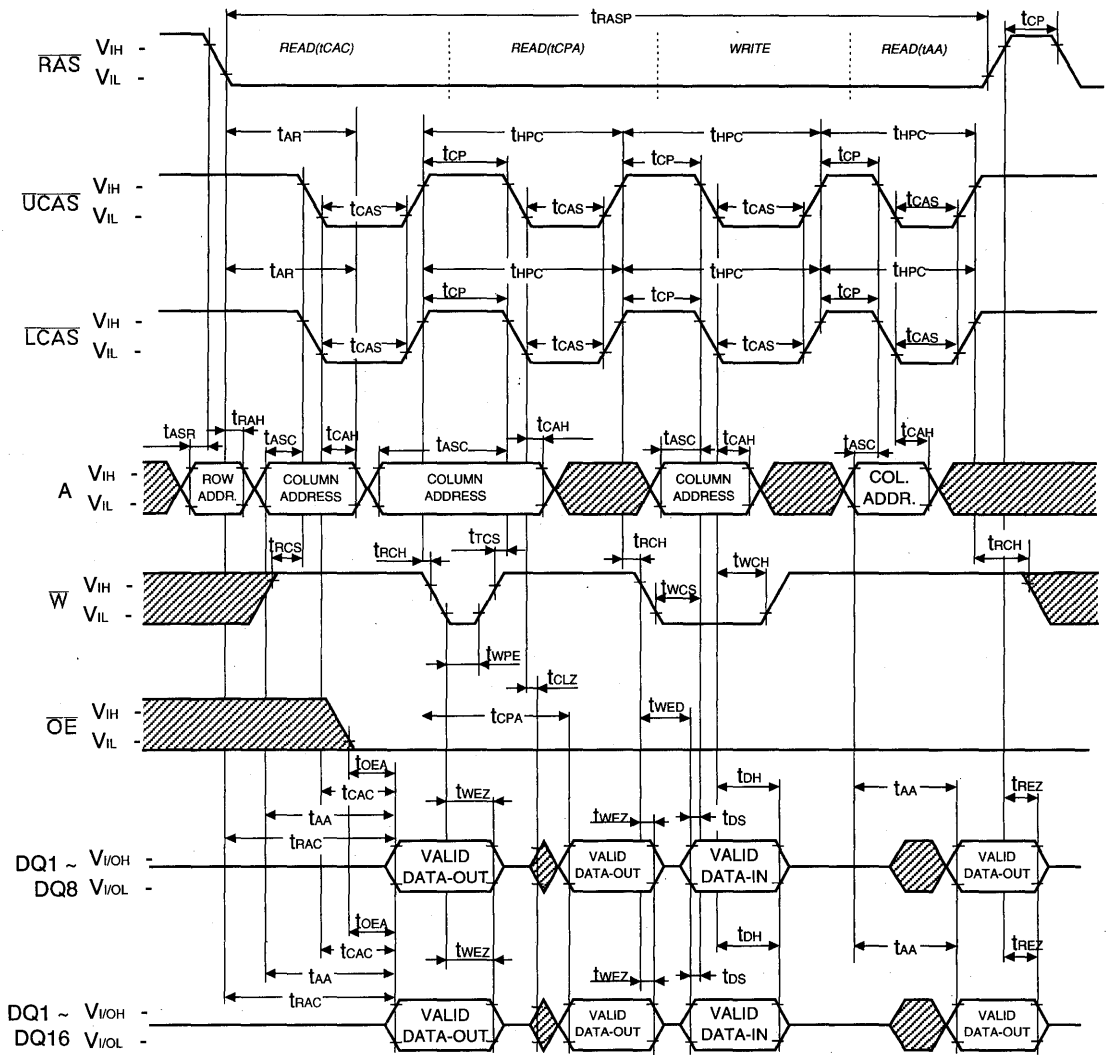
 Don't Care


HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



 Don't Care

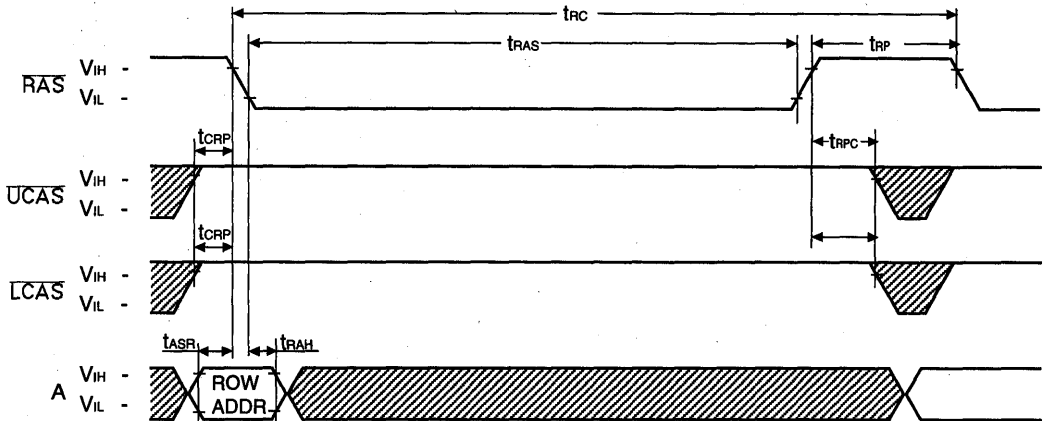
HYPER PAGE READ AND WRITE MIXED CYCLE



 Don't Care

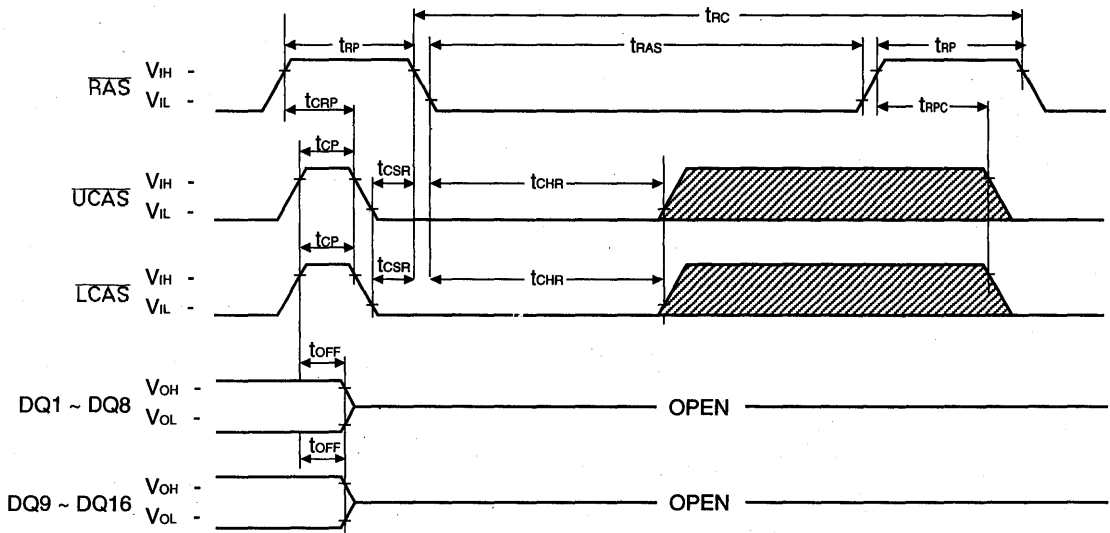
RAS-ONLY REFRESH CYCLE

NOTE : W, OE, DIN = Don't care
DOUT = Open



CAS-BEFORE-RAS REFRESH CYCLE

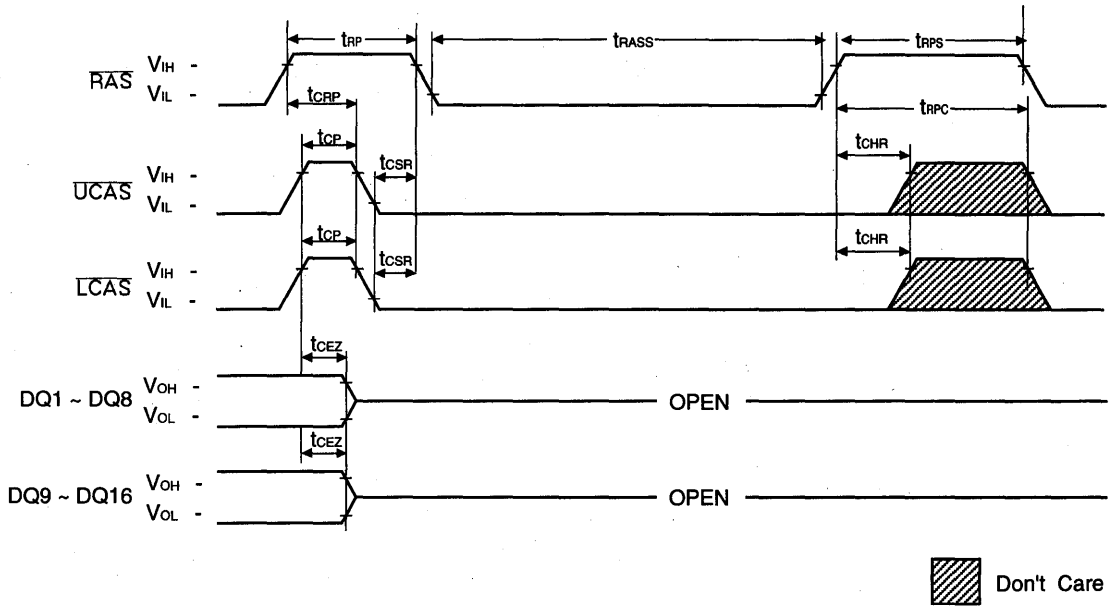
NOTE : W, OE, A = Don't Care



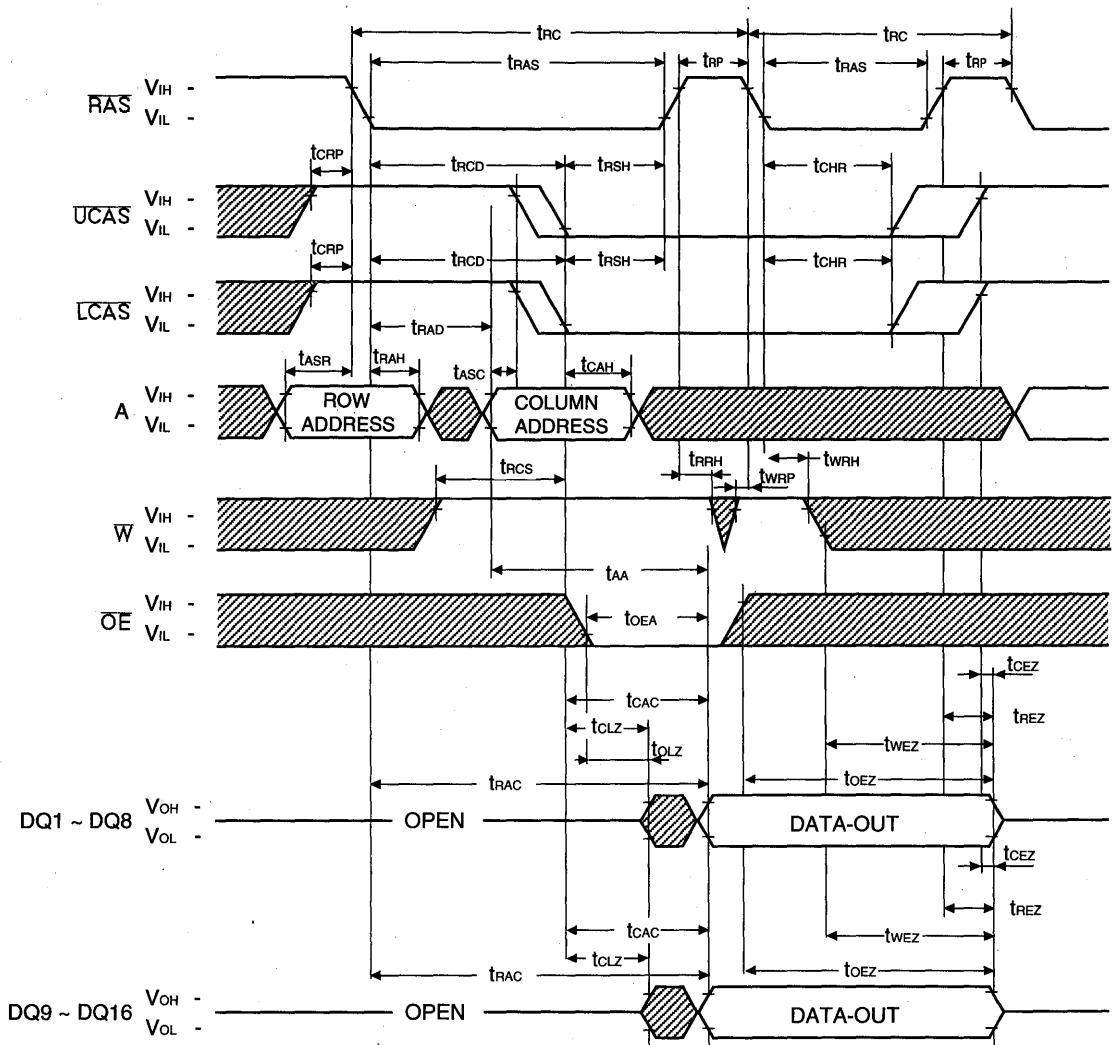
Don't Care

CAS-BEFORE-RAS SELF REFRESH CYCLE(LL-version)

NOTE : W, OE, A = Don't Care



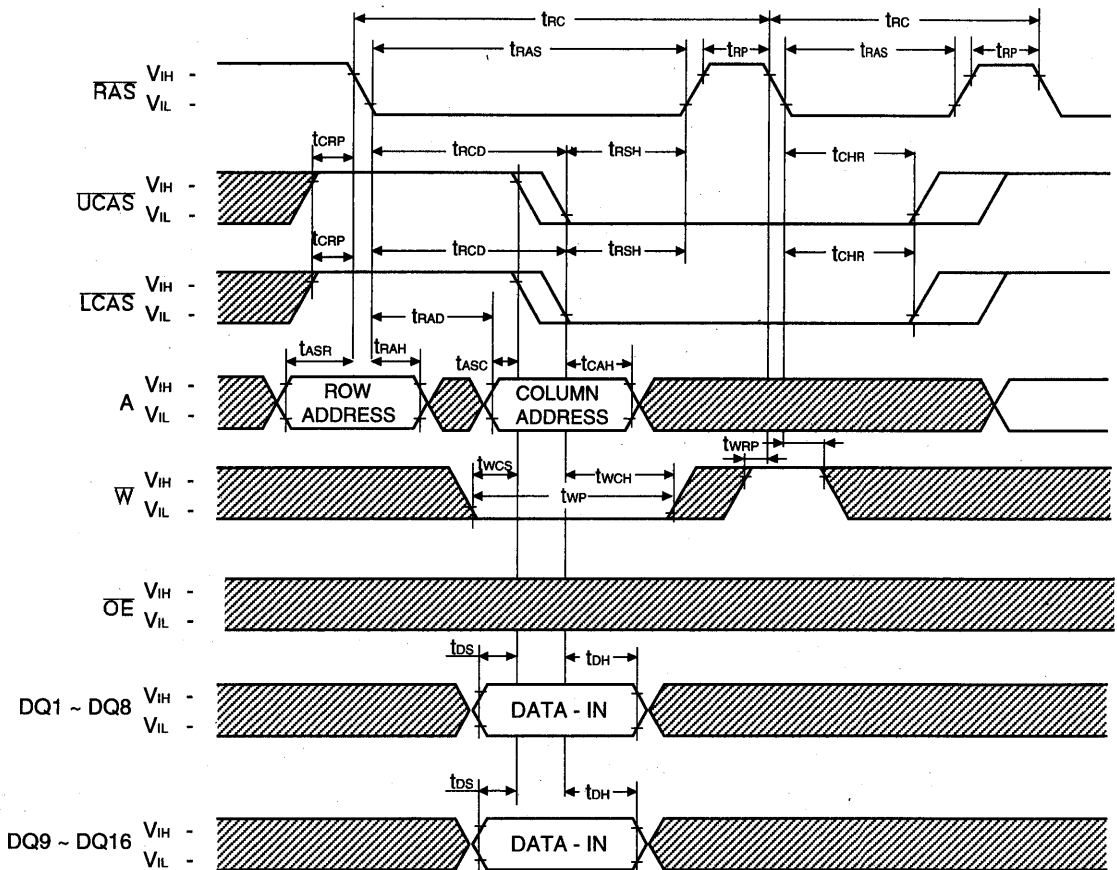
HIDDEN REFRESH CYCLE (READ)



 Don't Care

HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



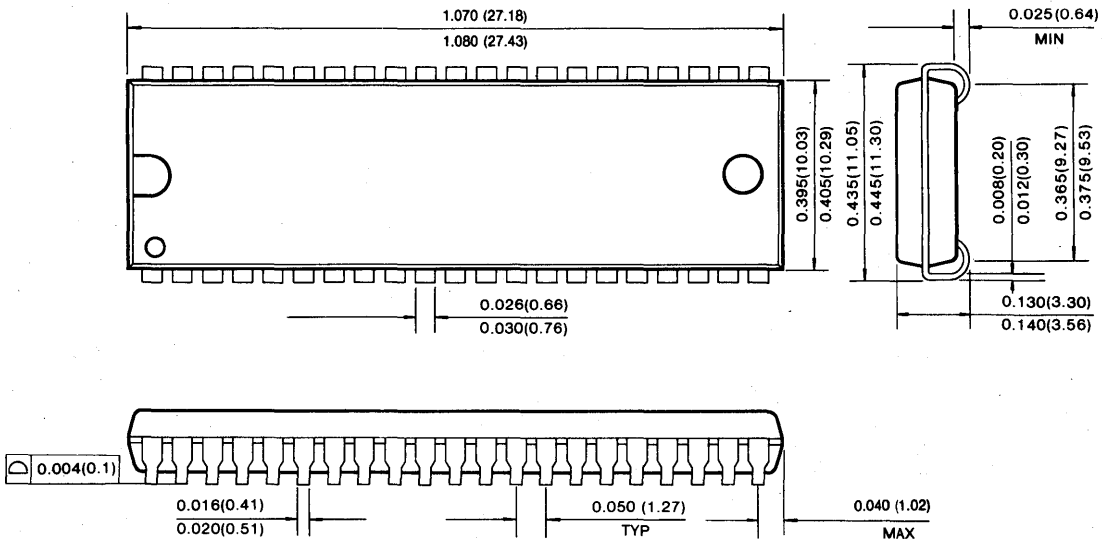
 Don't Care

6

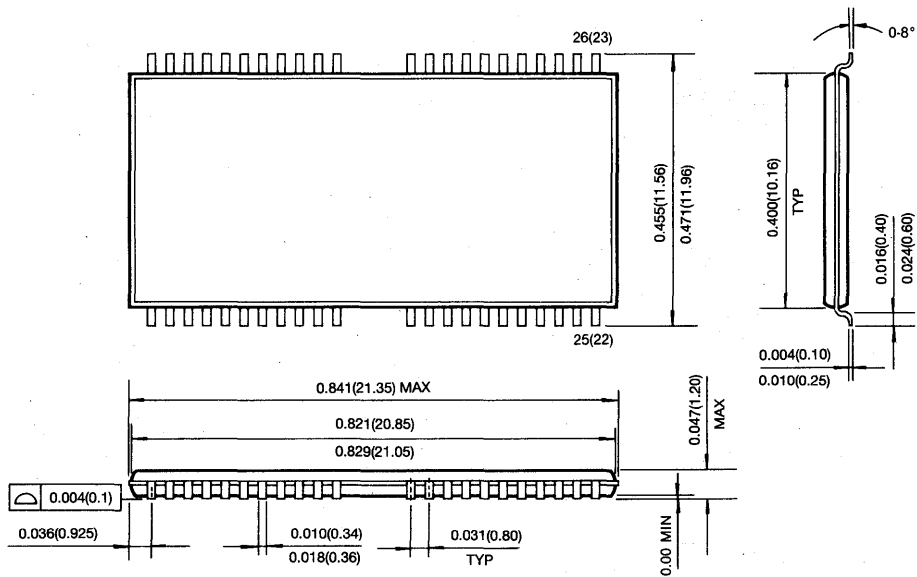
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	t _{TRAC}	t _{CAC}	t _{TRC}	t _{HPC}
KM416C1204A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416C1204A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416C1204A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- **Extended Data Out Mode**
(Fast Page Mode with Extended Data Out)
- **2 CAS Byte/Word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +5V ± 10% power supply**
- **Refresh Cycle**
-1024 cycle/16ms (Normal)
-1024 cycle/128ms (L-version)
-1024 cycle/128ms (F-version)
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II)**

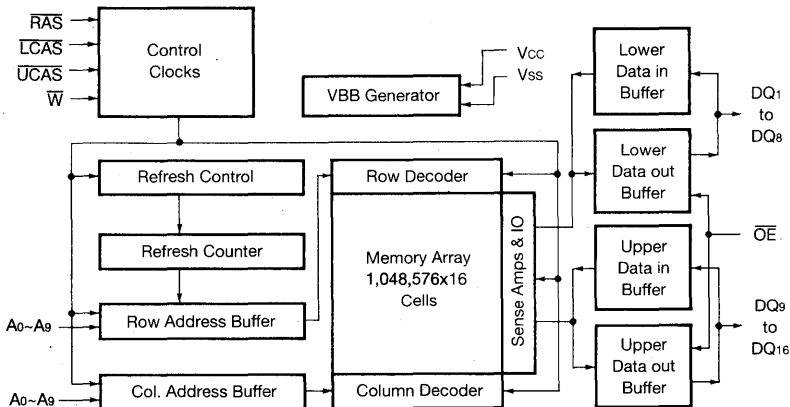
GENERAL DESCRIPTION

The Samsung KM416C1204A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

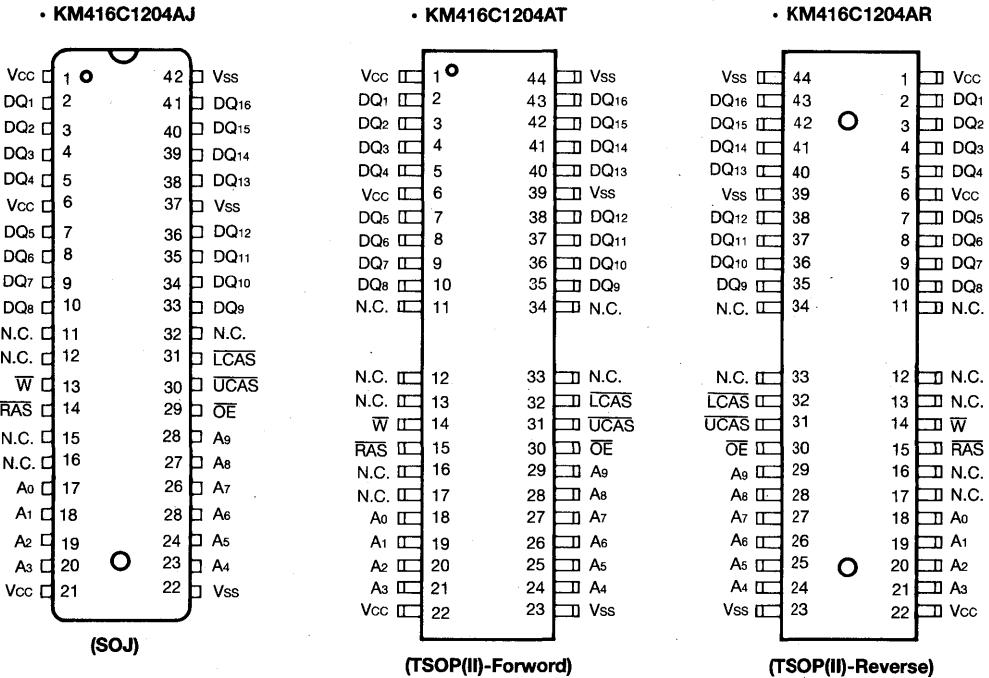
The KM416C1204A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

The KM416C1204A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
\bar{RAS}	Row Address Strobe
\bar{UCAS}	Upper Column Address Strobe
\bar{LCAS}	Lower Column Address Strobe
\bar{W}	Read/Write Input
\bar{OE}	Data Output Enable
Vcc	Power(+5V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc Supply Relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	—	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS, UCAS or LCAS, Address Cycling @trc=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8 I _{CC1}	-	160 150 140	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{IH})	KM416C1204A KM416C1204A-L KM416C1204A-F I _{CC2}	-	2 1 1	mA mA mA
RAS-Only Refresh Current* (UCAS=LCAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8 I _{CC3}	-	160 150 140	mA mA mA
EDO Mode Current* (RAS=V _{IL} , UCAS or LCAS, Address Cycling @tpc=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8 I _{CC4}	-	130 120 110	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{CC} -0.2V)	KM416C1204A KM416C1204A-L KM416C1204A-F I _{CC5}	-	1 300 200	mA μA μA
CAS-Before-RAS Refresh Current* (RAS, UCAS or LCAS Cycling @trc=min.)	KM416C1204A-6/A-L6/A-F6 KM416C1204A-7/A-L7/A-F7 KM416C1204A-8/A-L8/A-F8 I _{CC6}	-	160 150 140	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{CC} -0.2V, Input Low Voltage(V _{IL})=0.2V UCAS, LCAS=0.2V Din=Don't Care, trc=125μs (L-Ver) tRAS=tRAS min~300ns	KM416C1204A-L I _{CC7}	-	350	μA

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A9=Vcc-0.2V or 0.2V DQ1-DQ16=Vcc-0.2V or 0.2V or Open	lccs	-	250	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test=0 V)	Ii(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)	Io(L)	-10	10	μA
Output High Voltage Level (IOH=-5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

*NOTE: lcc1, lcc3, lcc4 and lcc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. lcc is specified as an average current. In lcc1 and lcc3, address can be changed maximum once while RAS=VIL. In lcc4, Address can be changed maximum once while one Hyper page mode cycle time THPC.

CAPACITANCE (TA=25°C, Vcc=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~A9)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1~DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, Vcc=5V ± 10%, See notes 1,2)

(Test condition : VIH/VIL=2.4V/0.8V, VOH/VOL=2.0V/0.8V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from RAS	trac		60		70		80	ns	3,4,11
Access time from CAS	tcac		17		20		20	ns	3,4,5
Access time from column address	taa		30		35		40	ns	3,11
CAS to output in Low-Z	tclz	3		3		3		ns	3
OE to output in Low-Z	tolz	3		3		3		ns	3
Output buffer turn-off delay from CAS	tcez	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	tt	2	50	2	50	2	50	ns	2
RAS precharge time	trp	40		50		60		ns	
RAS pulse width	trasp	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trsh	17		20		20		ns	
CAS hold time	tcs	50		60		70		ns	
CAS pulse width	tcasp	10	10,000	15	10,000	20	10,000	ns	
RAS to CAS delay time	trcd	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to RAS	tAR	45		55		60		ns	6
Column address to RAS lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to RAS	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		15		20		ns	
Write command to CAS lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to RAS	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
CAS to W delay time	tCWD	40		50		50		ns	8,17
RAS to W delay time	tRWD	85		95		105		ns	8
Column address to W delay time	tAWD	55		60		65		ns	8
CAS precharge to W delay time	tCPWD	60		65		70		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		ns	20
RAS precharge to CAS hold time	tRPC	5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		25		30		ns	
RAS hold time referenced to OE	tROH	15		20		20		ns	
OE access time	tOEA		15		20		20	ns	
OE to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from OE	tOEZ	3	15	3	20	3	20	ns	7
OE command hold time	tOEH	15		20		20		ns	
Access time from CAS precharge	tCPA		35		40		45	ns	3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
CAS orcharge time (Hyper page mode)	tCP	10		10		10		ns	16
RAS pulse width (Hyper page mode)	tRASP	60	200.000	70	200.000	80	200.000	ns	
RAS hold time from CAS precharge	tRHCP	35		40		45		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from W	tWEZ	3	15	3	20	3	20	ns	7
W to data delay	tWED	15		20		20		ns	
OE to CAS hold time	tOCH	5		5		5		ns	
CAS hold time to OE	tCHO	5		5		5		ns	
OE precharge time	tOEP	5		5		5		ns	
W pulse width	tWPE	5		5		5		ns	
RAS pulse width (F-ver)	tRASS	100		100		100		μ s	13
RAS precharge time (F-ver)	tRPS	110		130		150		ns	13
CAS hold time (F-ver)	tCHS	-50		-50		-50		ns	13

KM416C1204A/A-L/A-F Truth Table

RAS	LCAS	UCAS	W	OE	DQ1-DQ8	DQ9-DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	x	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

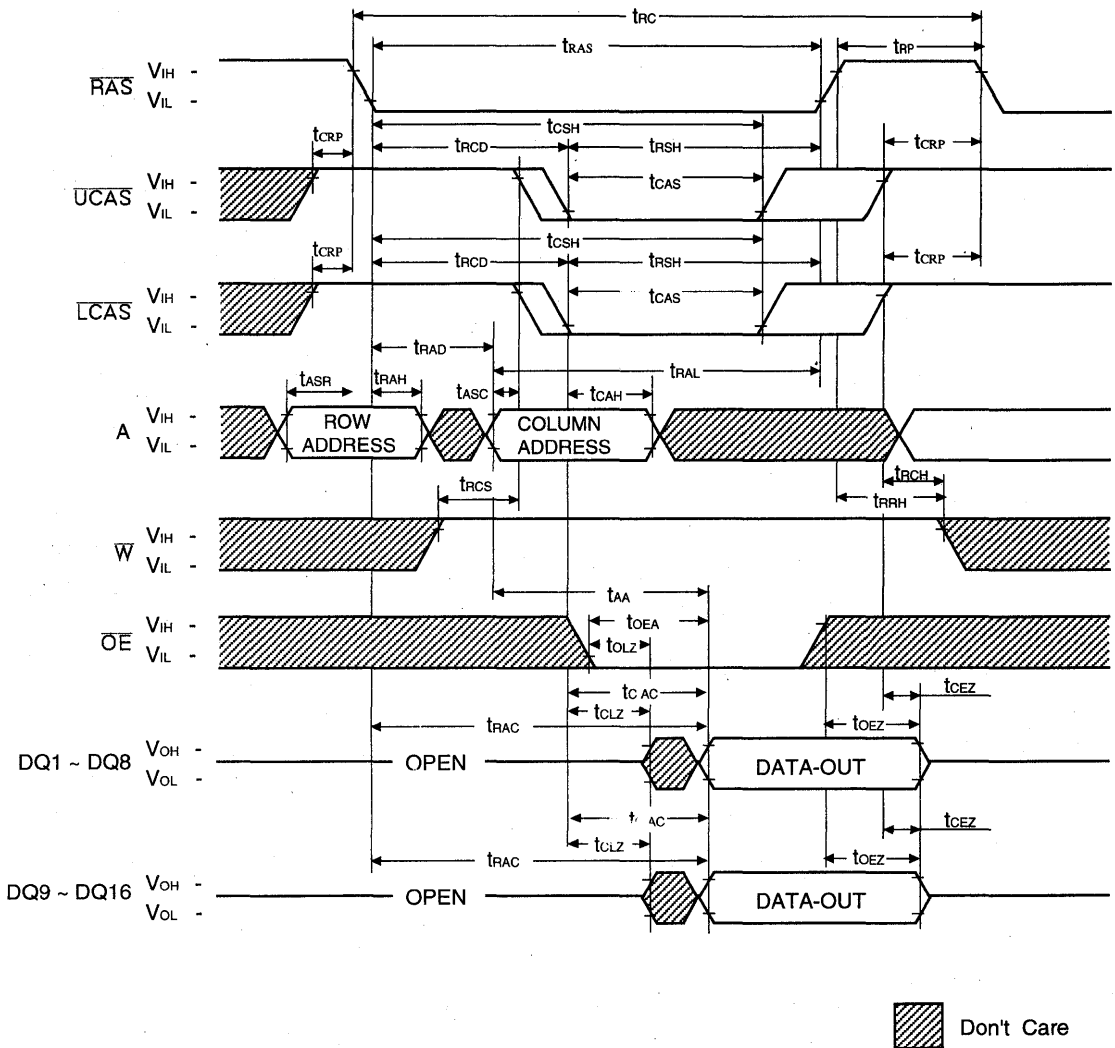
6

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL Loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. $t_{ASC} \geq t_{CP} \min$, Assume $t_T = 2.0ns$.
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
15. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
16. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
17. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
19. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
20. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.
21. t_{DS} , t_{DH} is independently specified for lower byte $D_{in(1-8)}$, upper byte $D_{in(9-16)}$

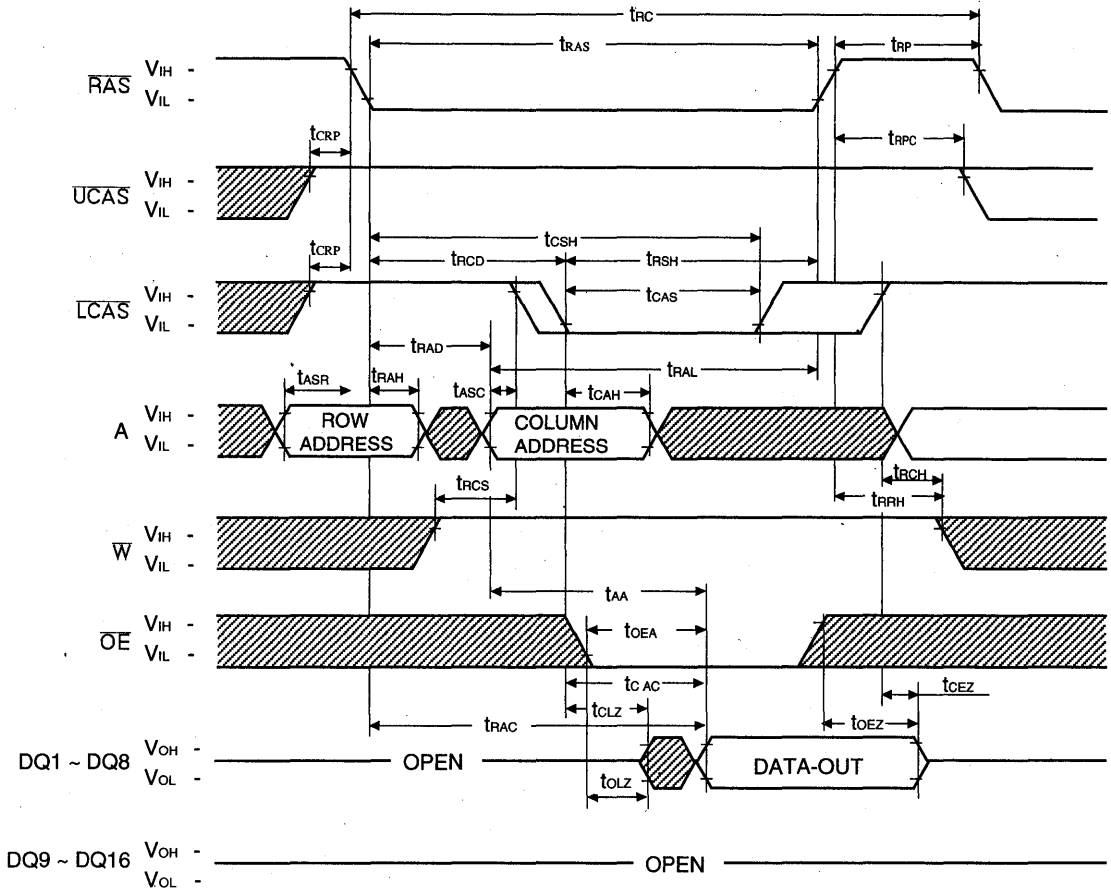
TIMING DIAGRAM
WORD READ CYCLE


NOTE : $D_{IN} = OPEN$



TIMING DIAGRAM
LOWER BYTE READ CYCLE

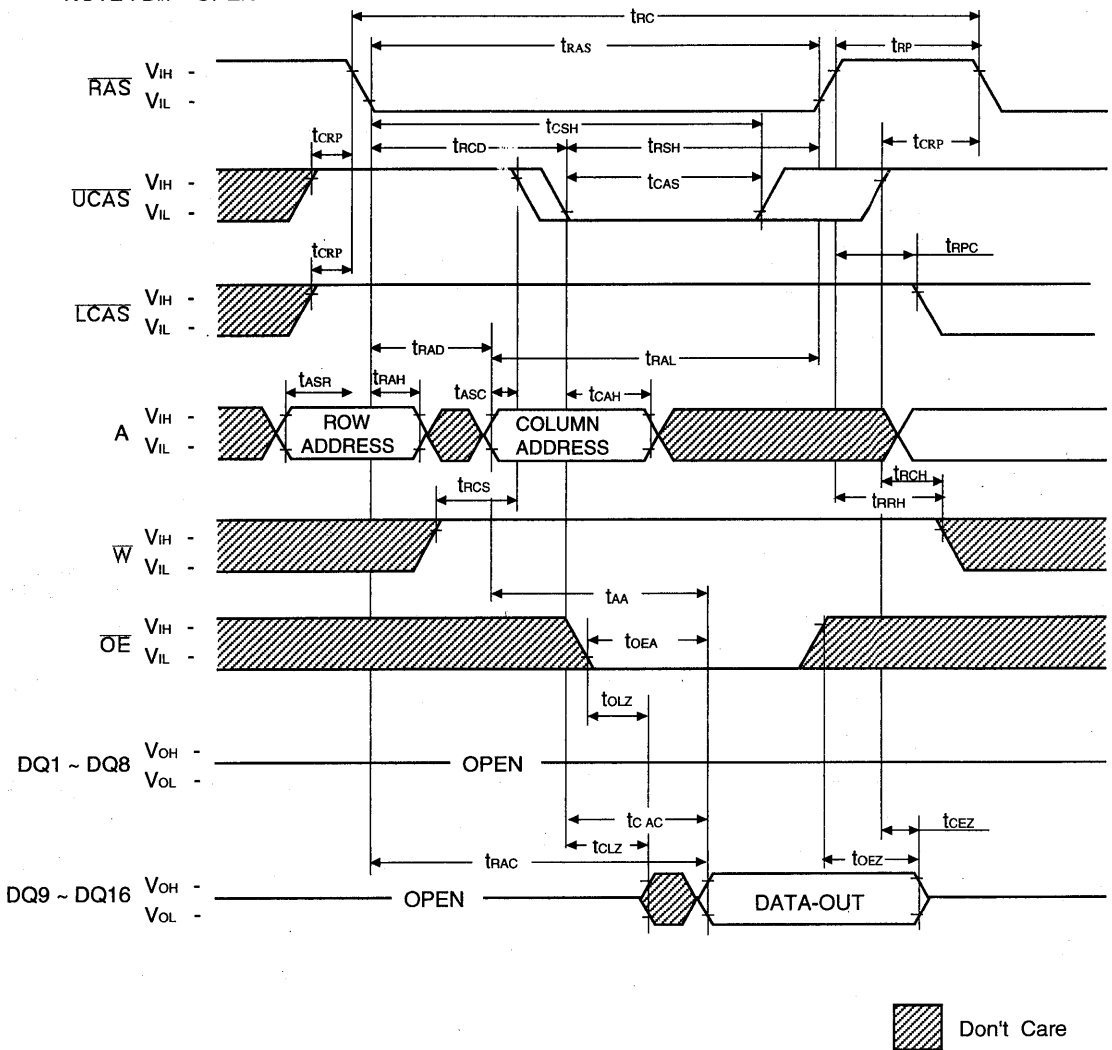
NOTE : D_{IN} = OPEN



 Don't Care

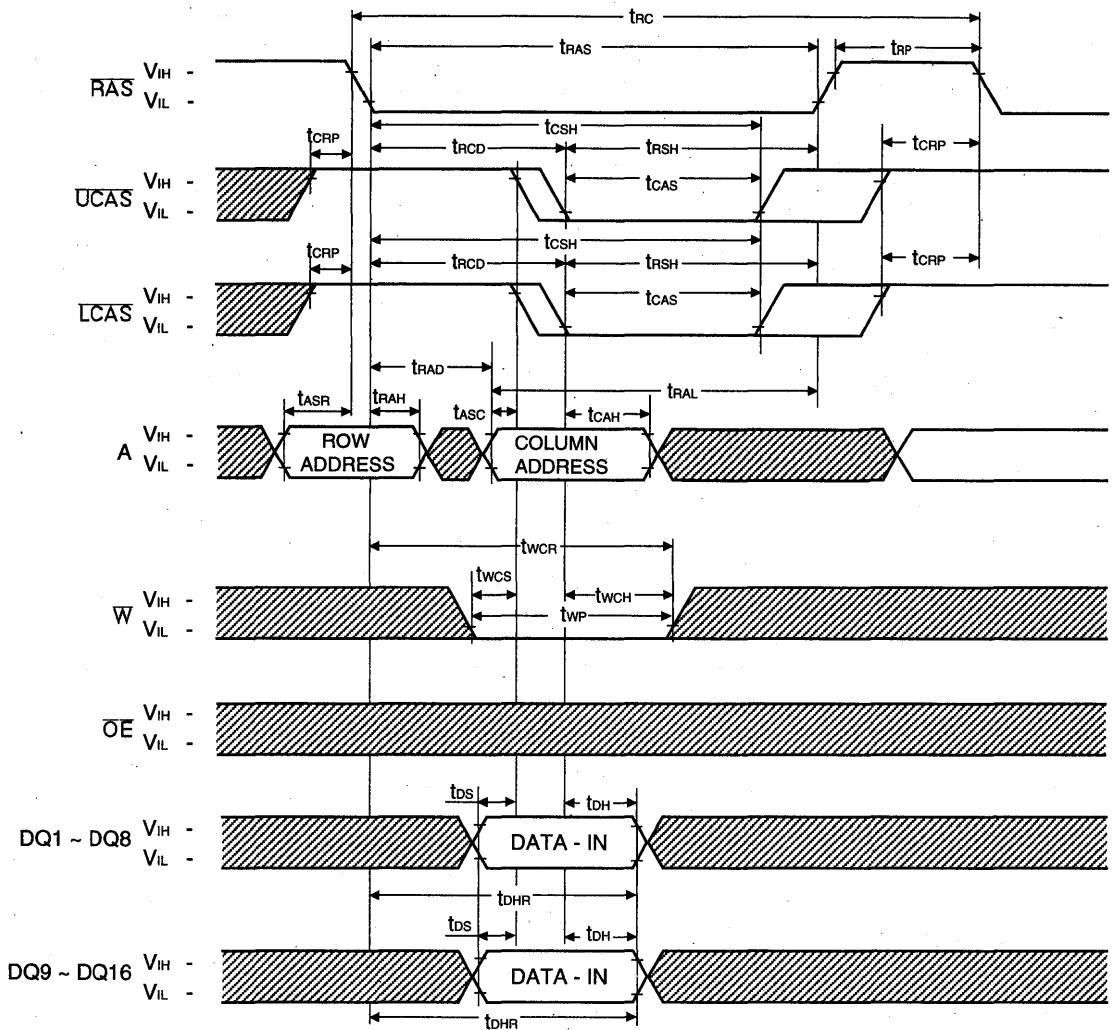
TIMING DIAGRAM
UPPER BYTE READ CYCLE


NOTE : $D_{IN} = OPEN$



WORD WRITE CYCLE (EARLY WRITE)

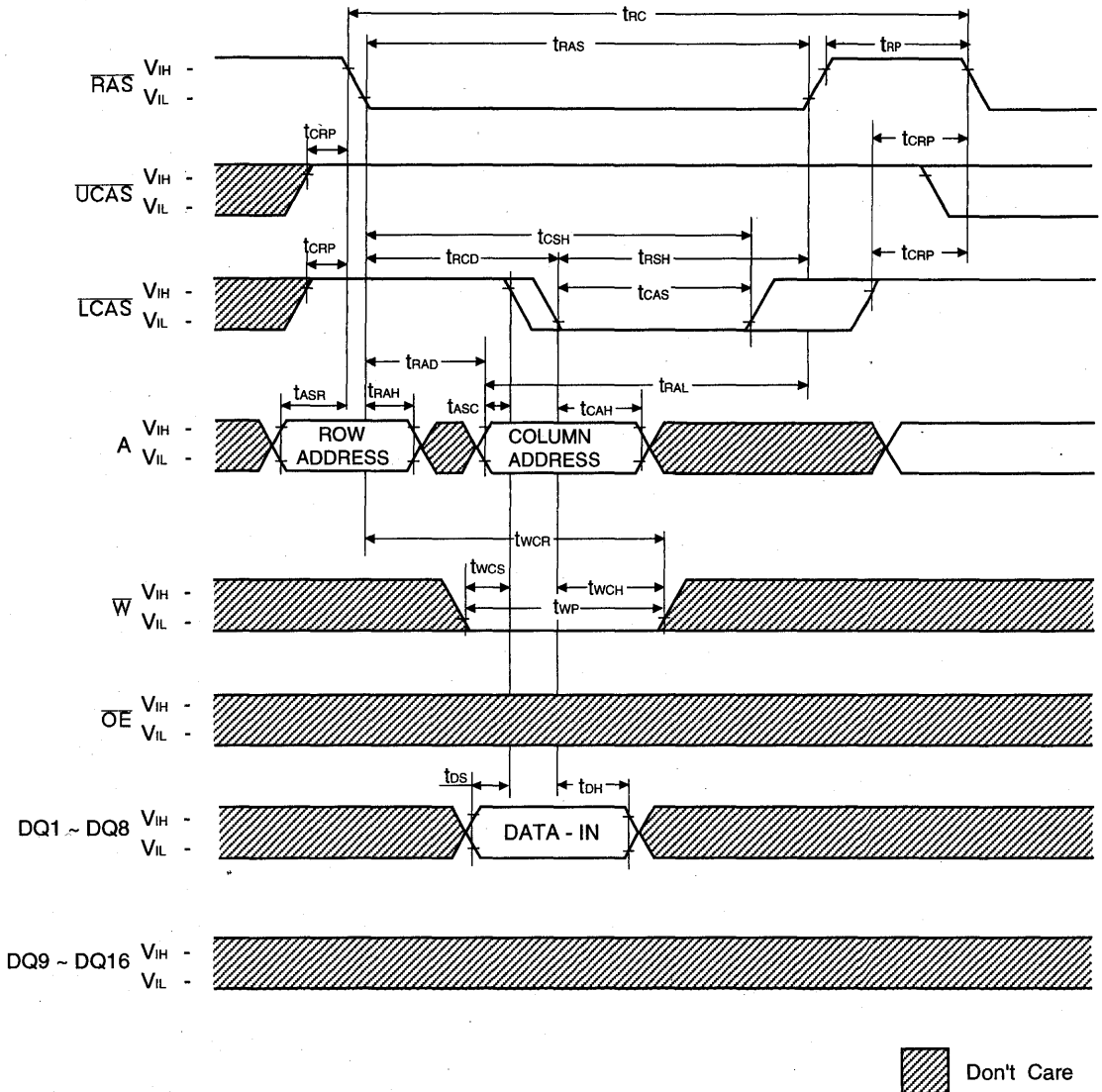
NOTE : DOUT = OPEN



 Don't Care

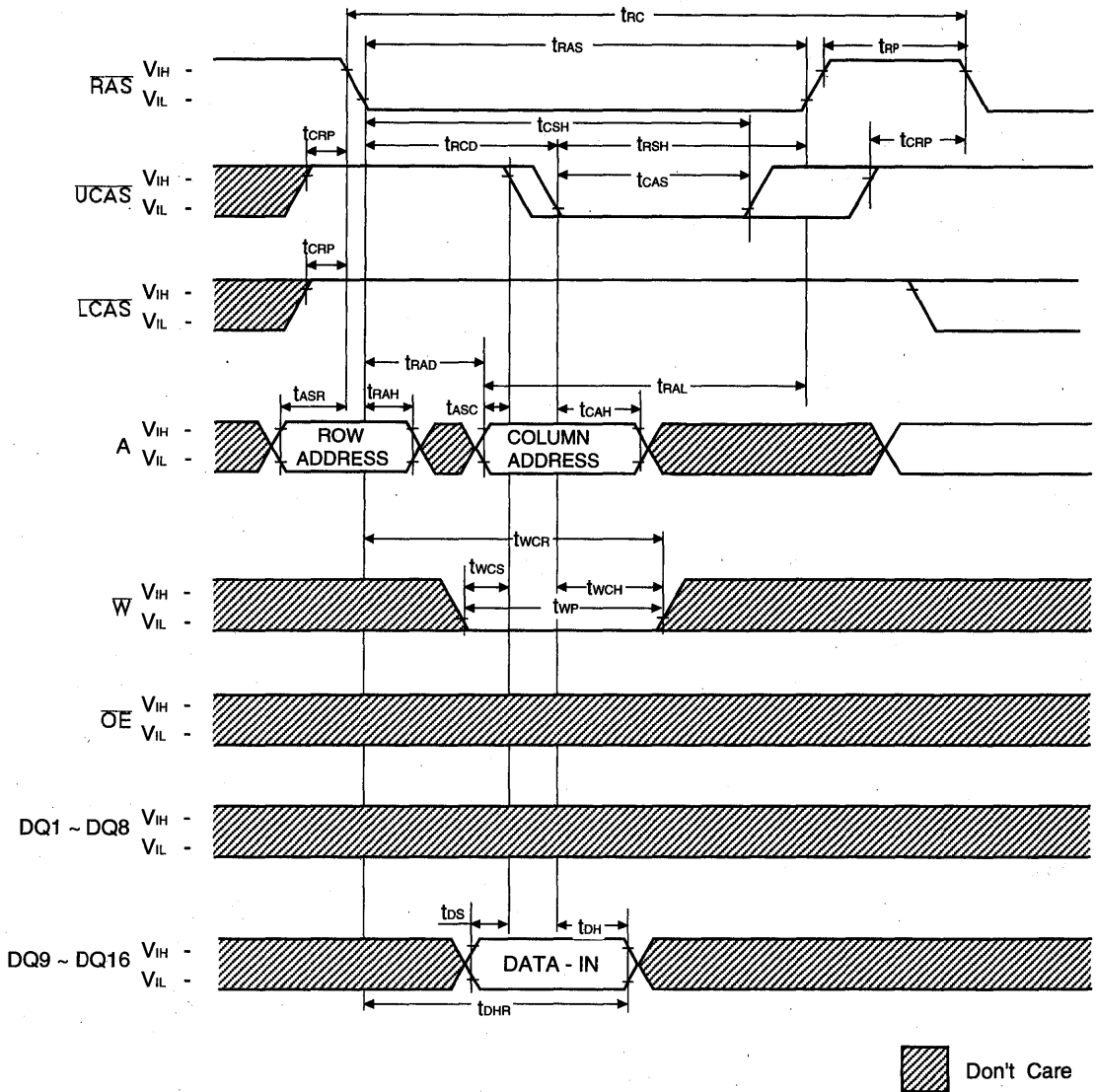
LOWER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



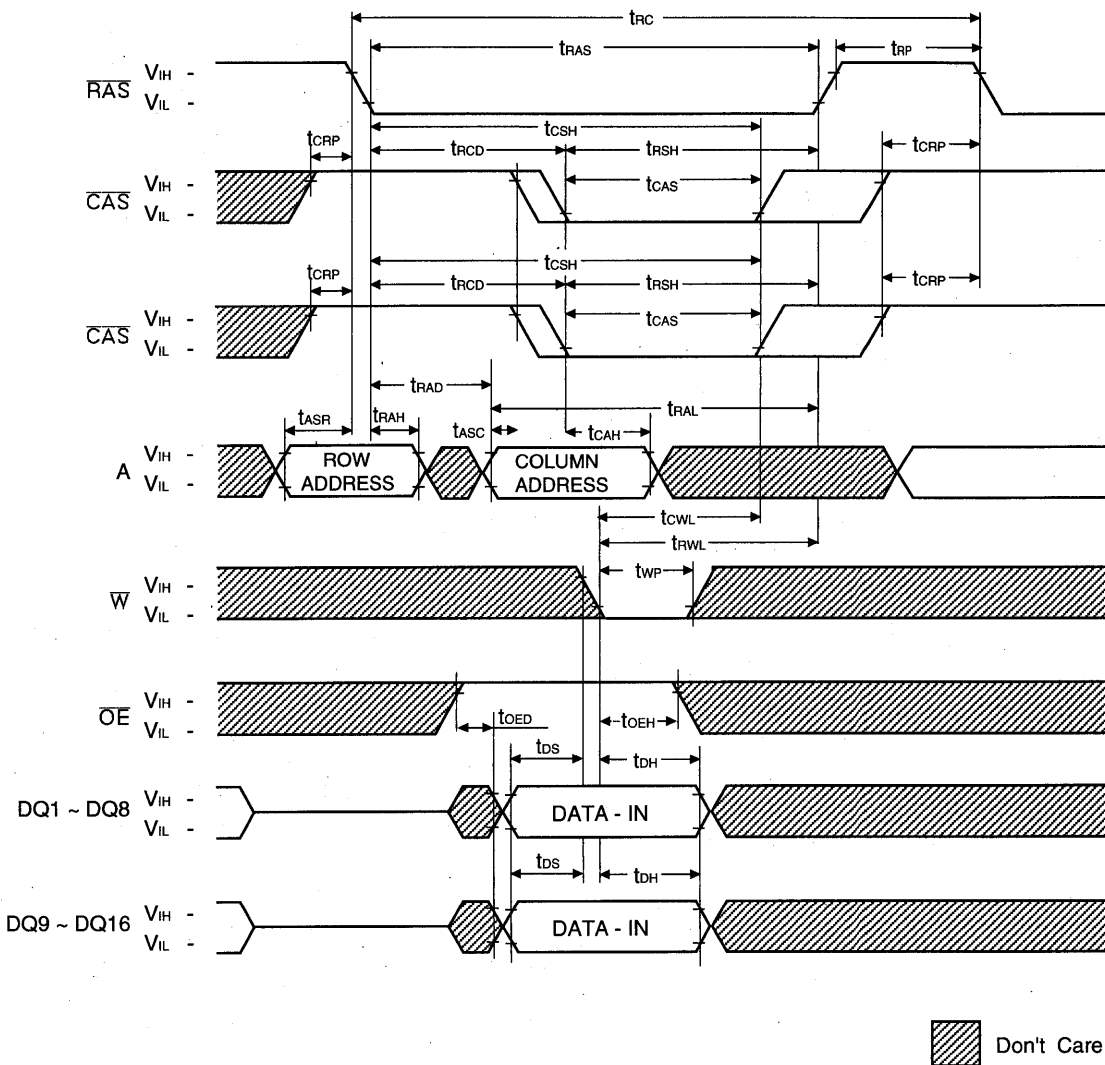
UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



WORD WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

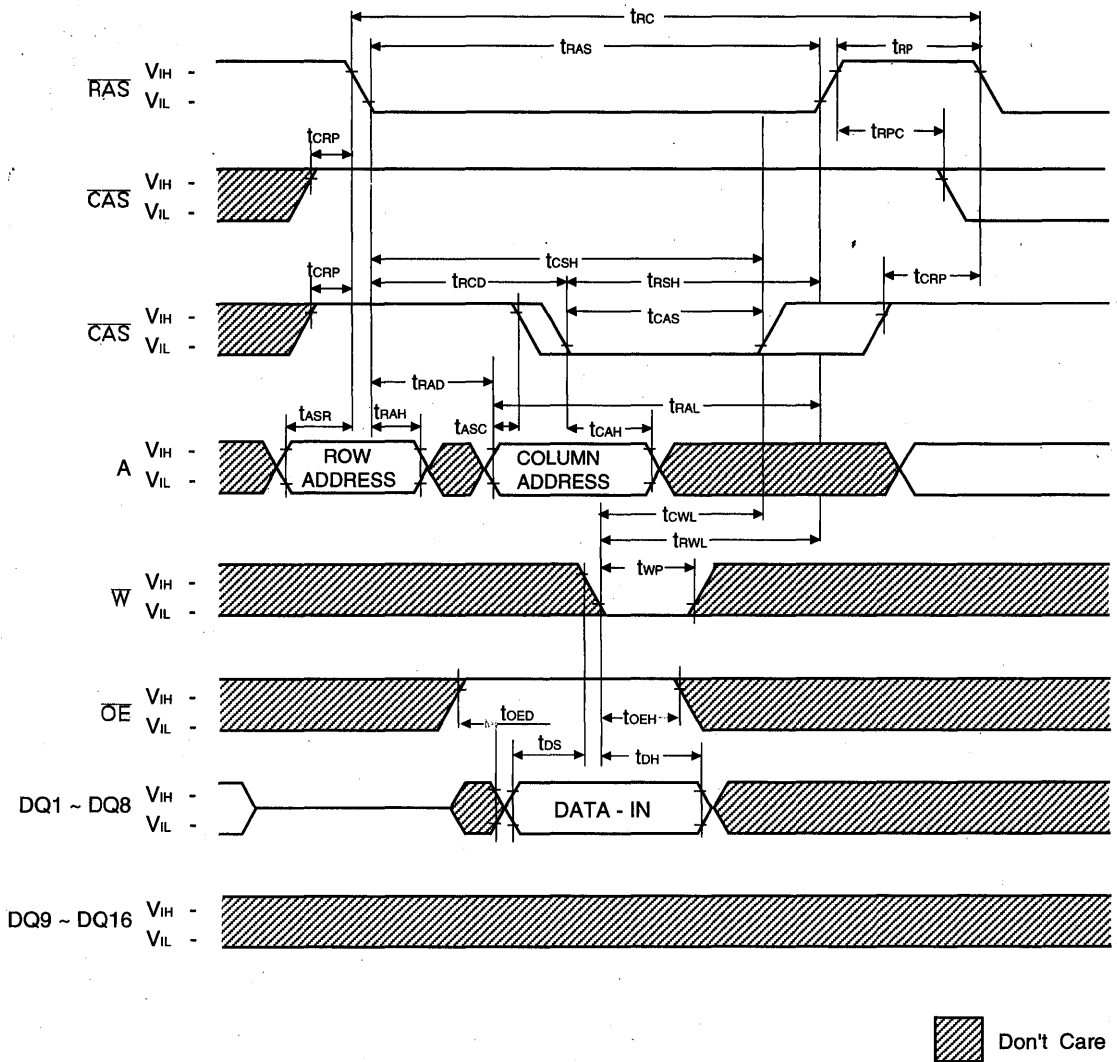
NOTE : $D_{OUT} = OPEN$



6

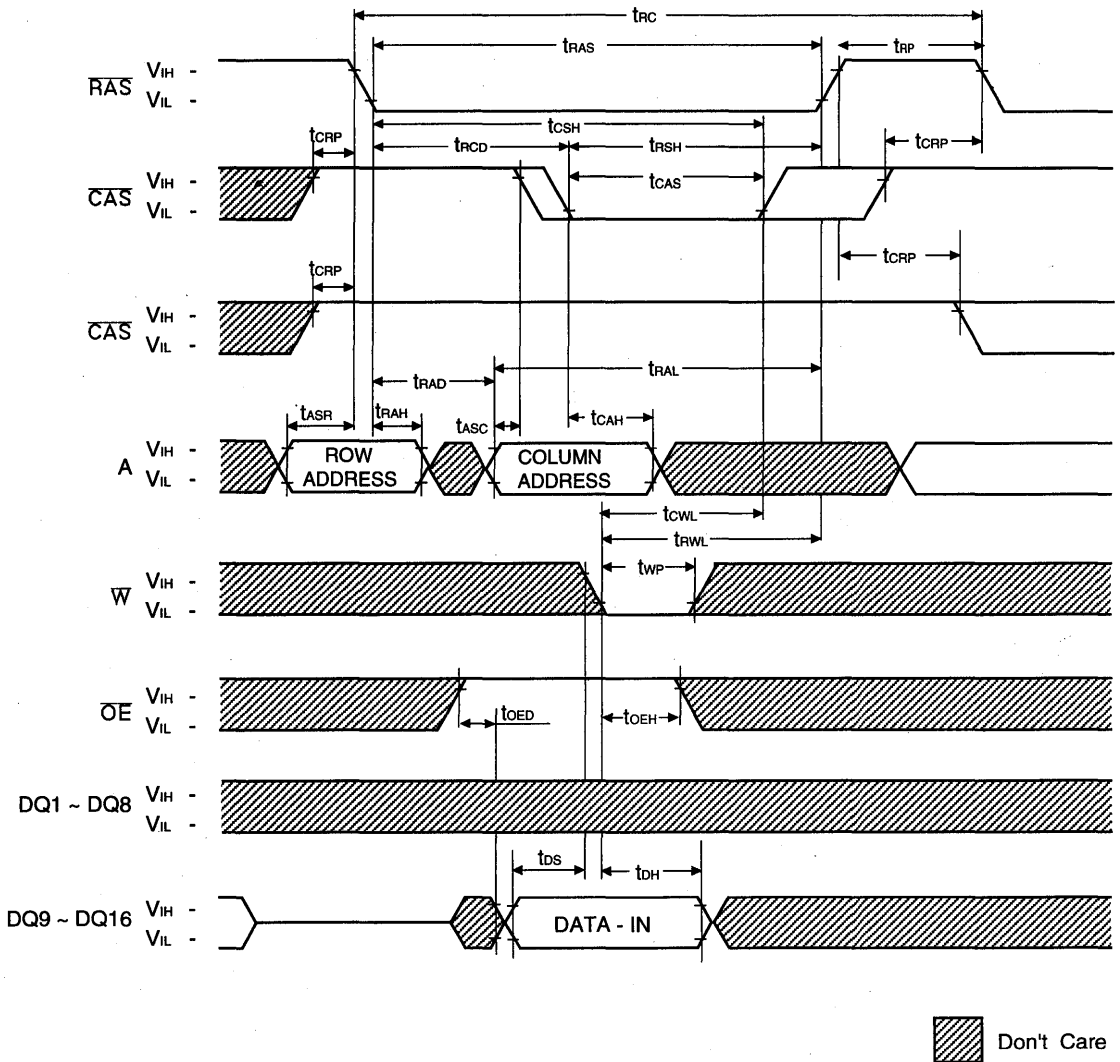
LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



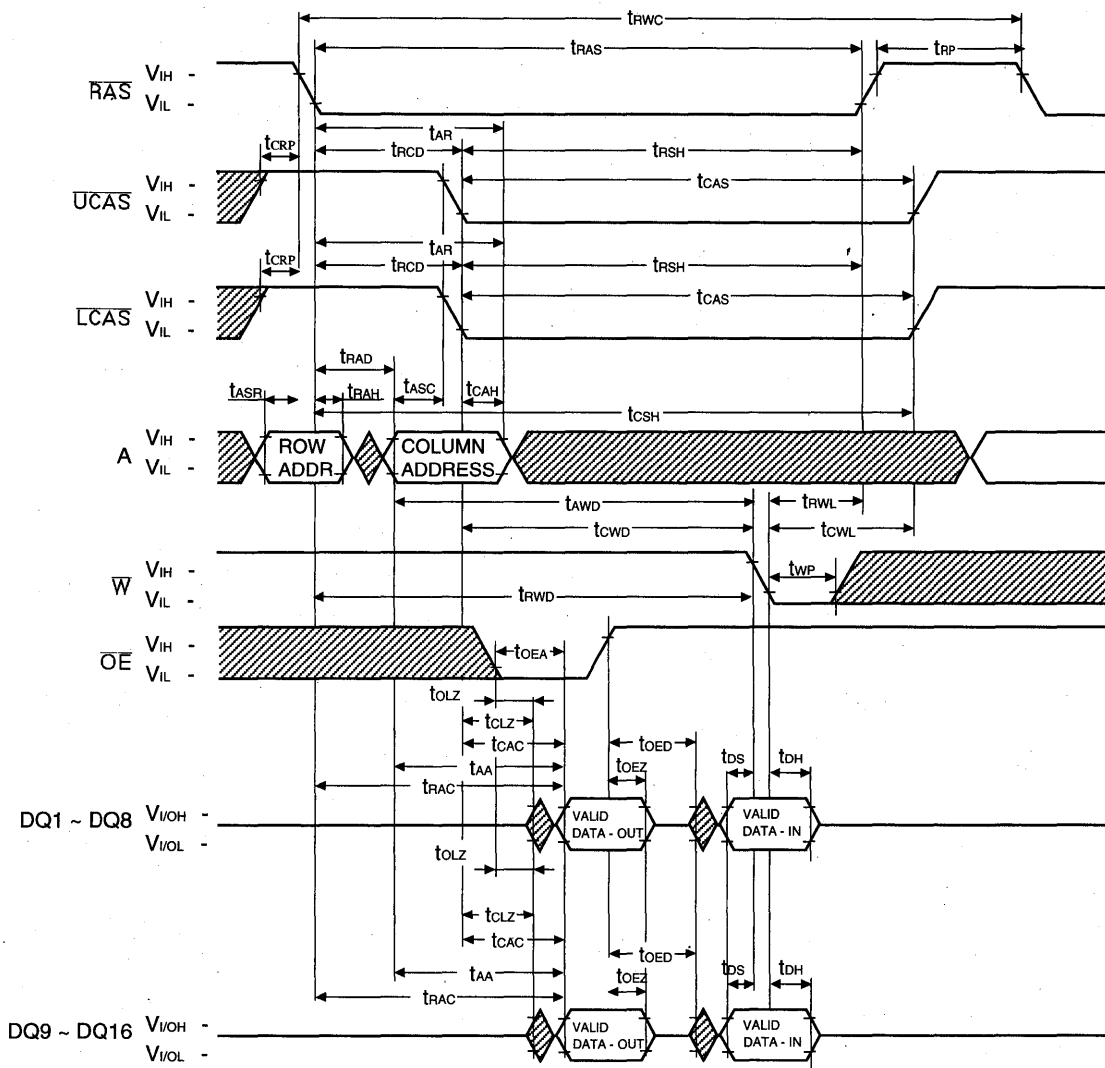
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



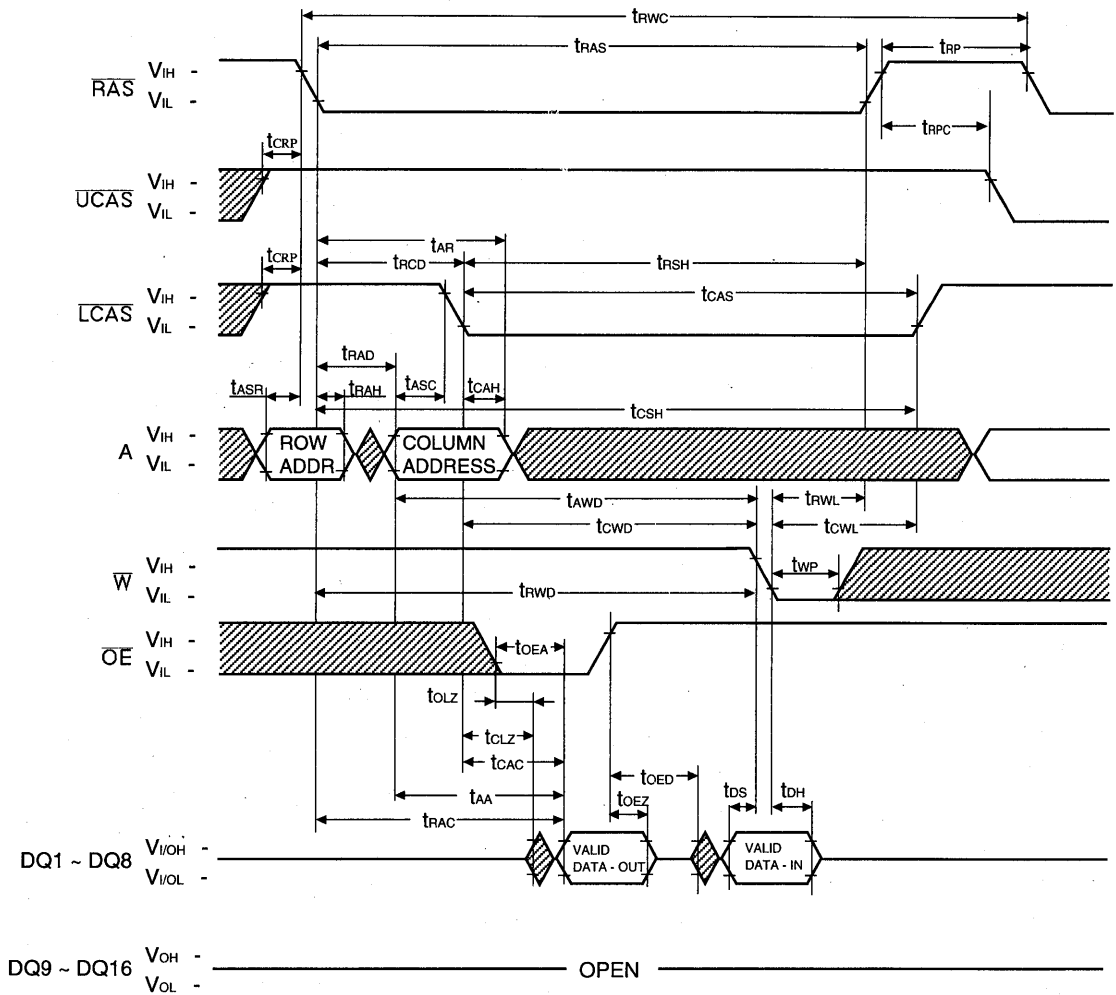
6

WORD READ - MODIFY - WRITE CYCLE



 Don't Care

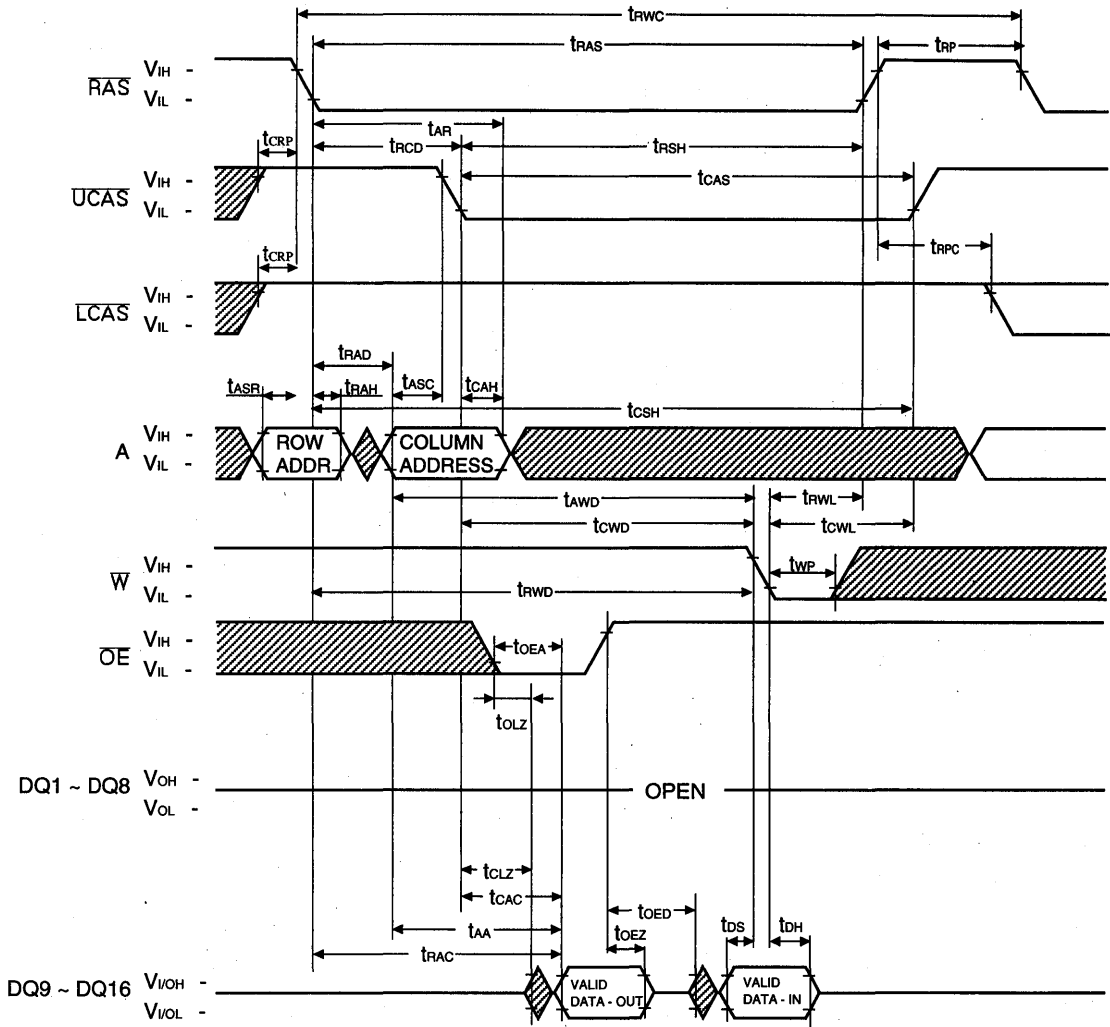
LOWER-BYTE READ - MODIFY - WRITE CYCLE



6

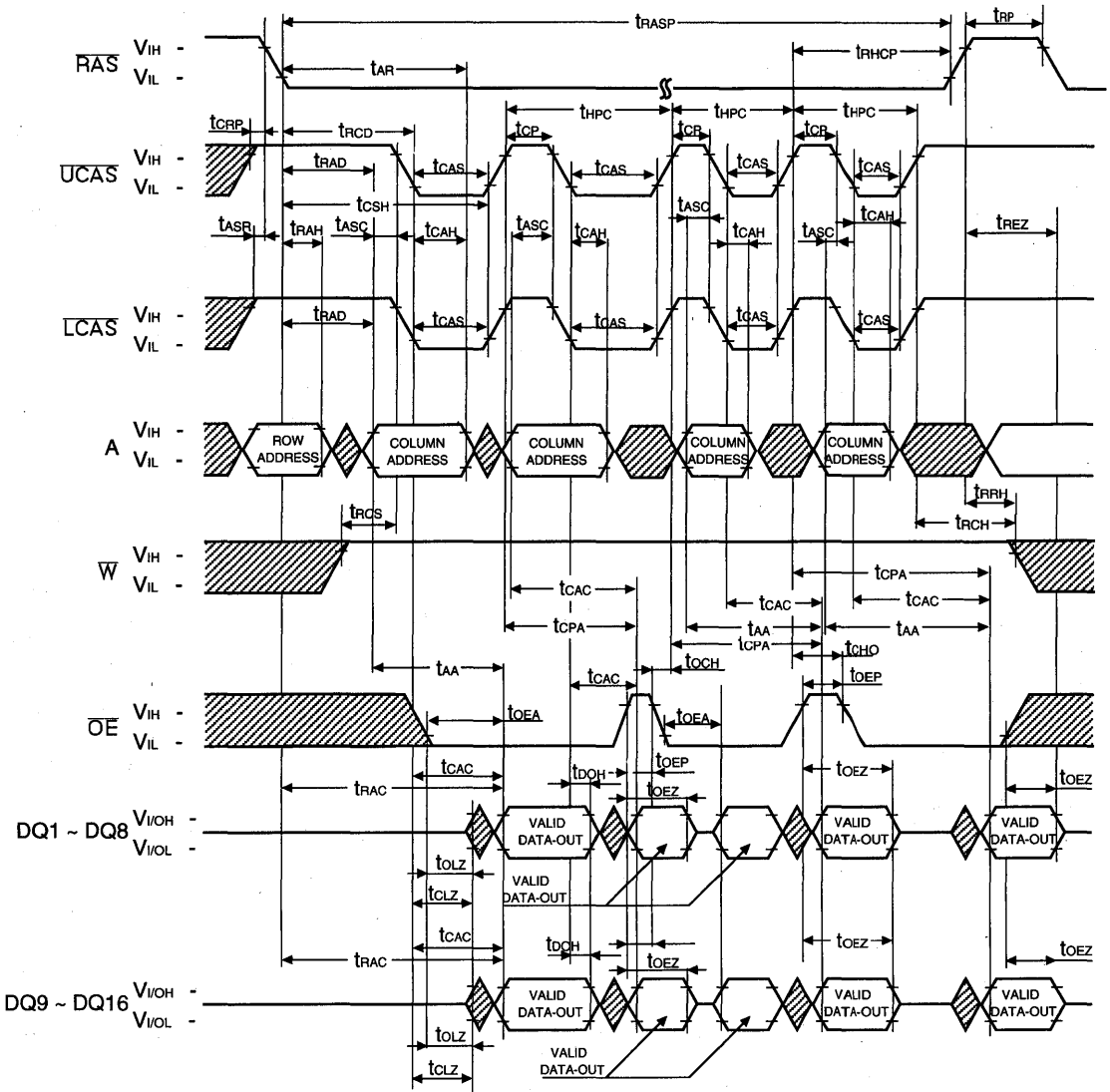
Don't Care

UPPER-BYTE READ - MODIFY - WRITE CYCLE



 Don't Care

HYPER PAGE MODE WORD READ CYCLE

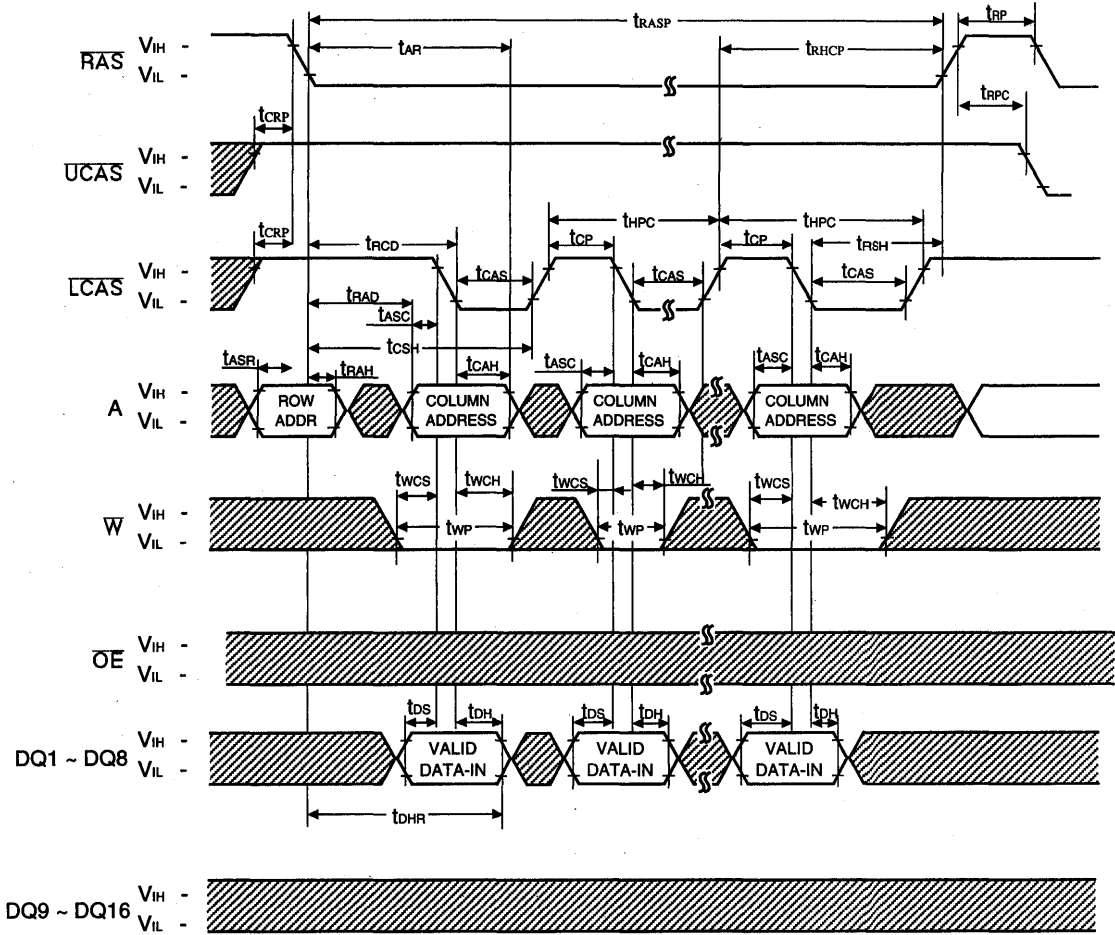


Don't Care

6

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

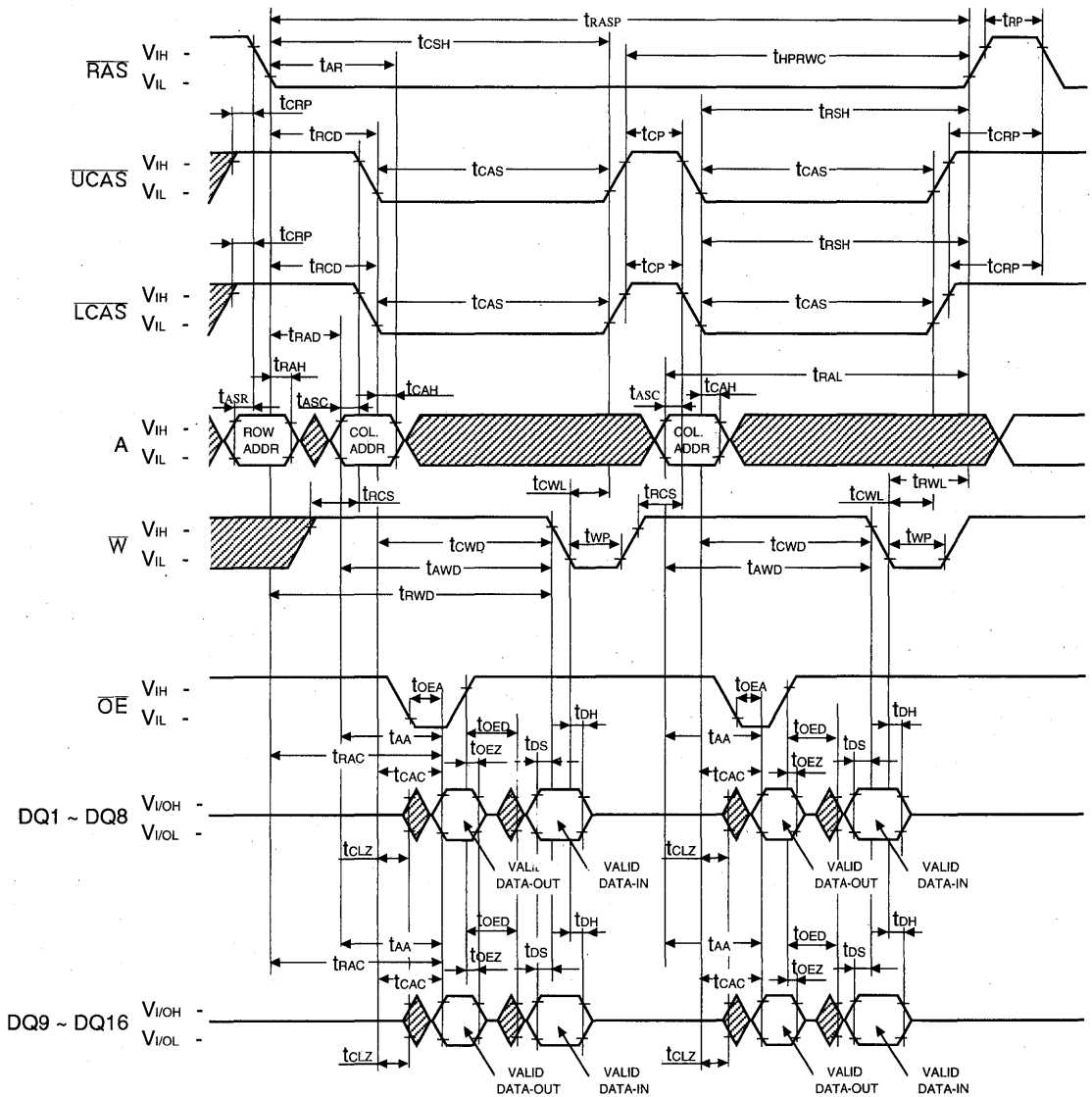
NOTE : Dout = Open



 Don't Care

6

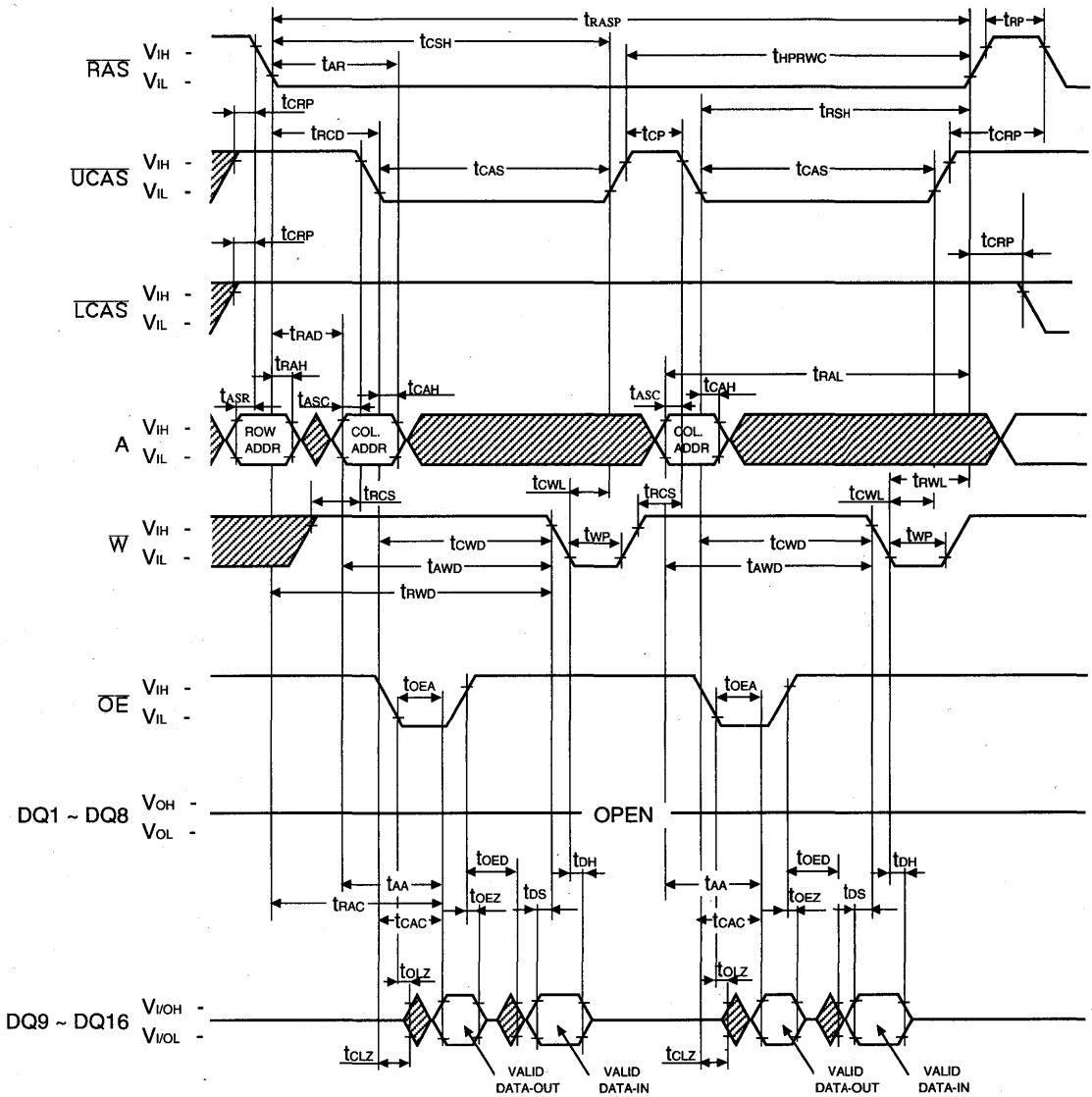
HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



6

 Don't Care

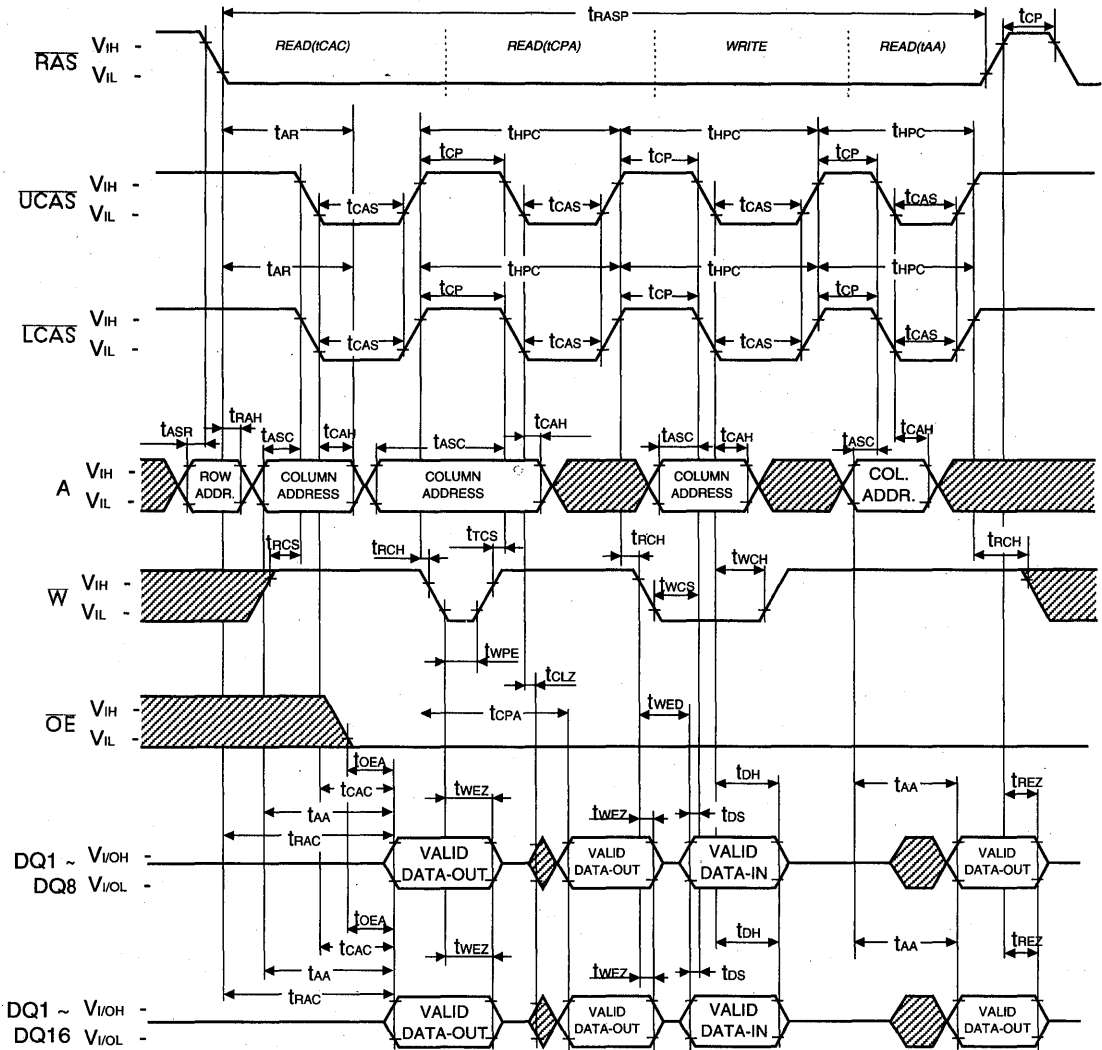
HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



6

 Don't Care

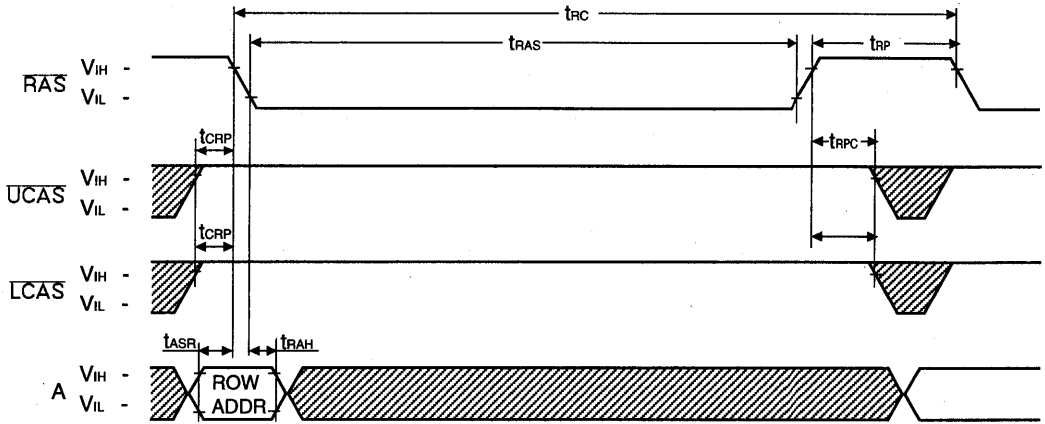
HYPER PAGE READ AND WRITE MIXED CYCLE



 Don't Care

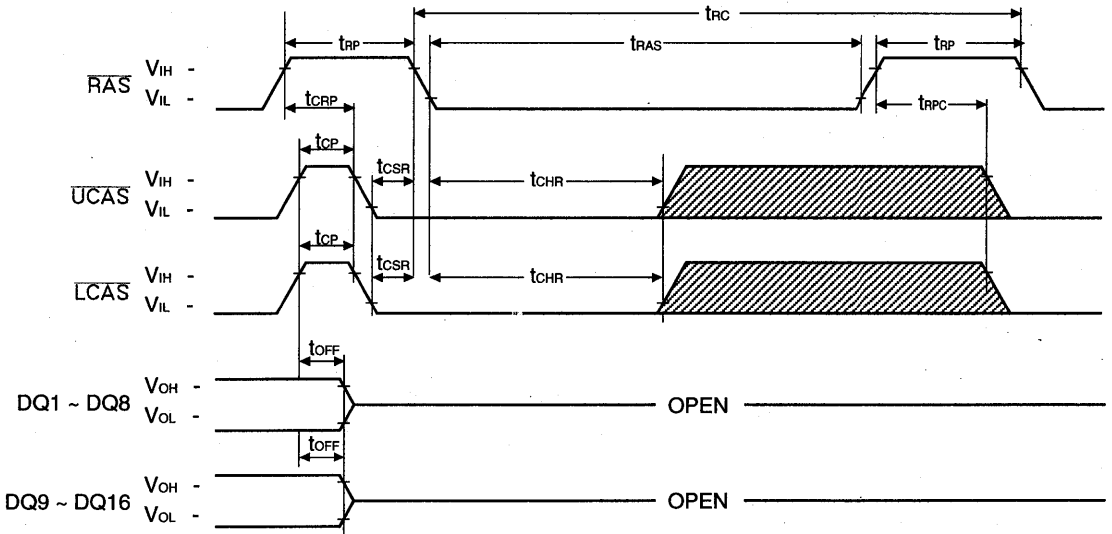
RAS-ONLY REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



CAS-BEFORE-RAS REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care

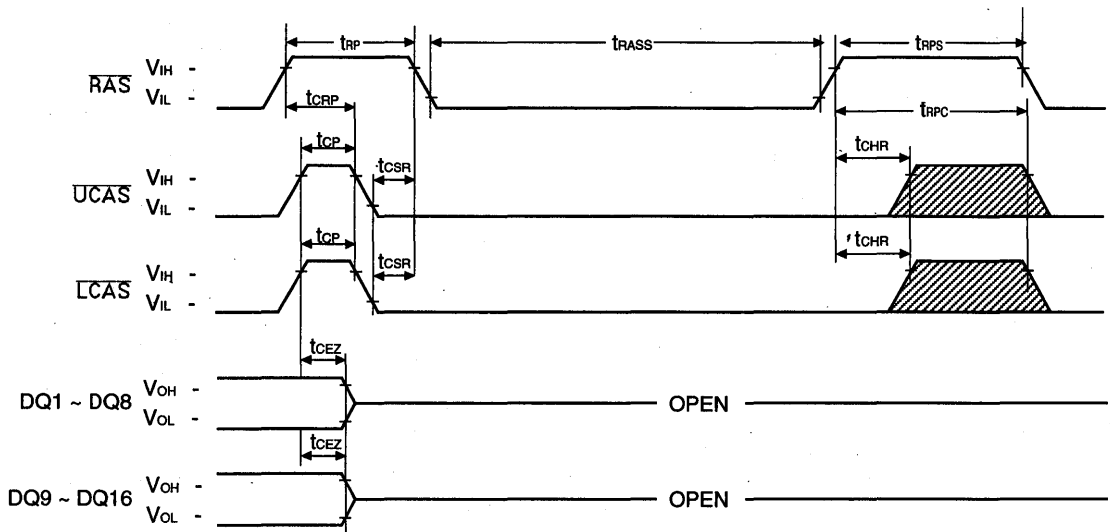


 Don't Care

6

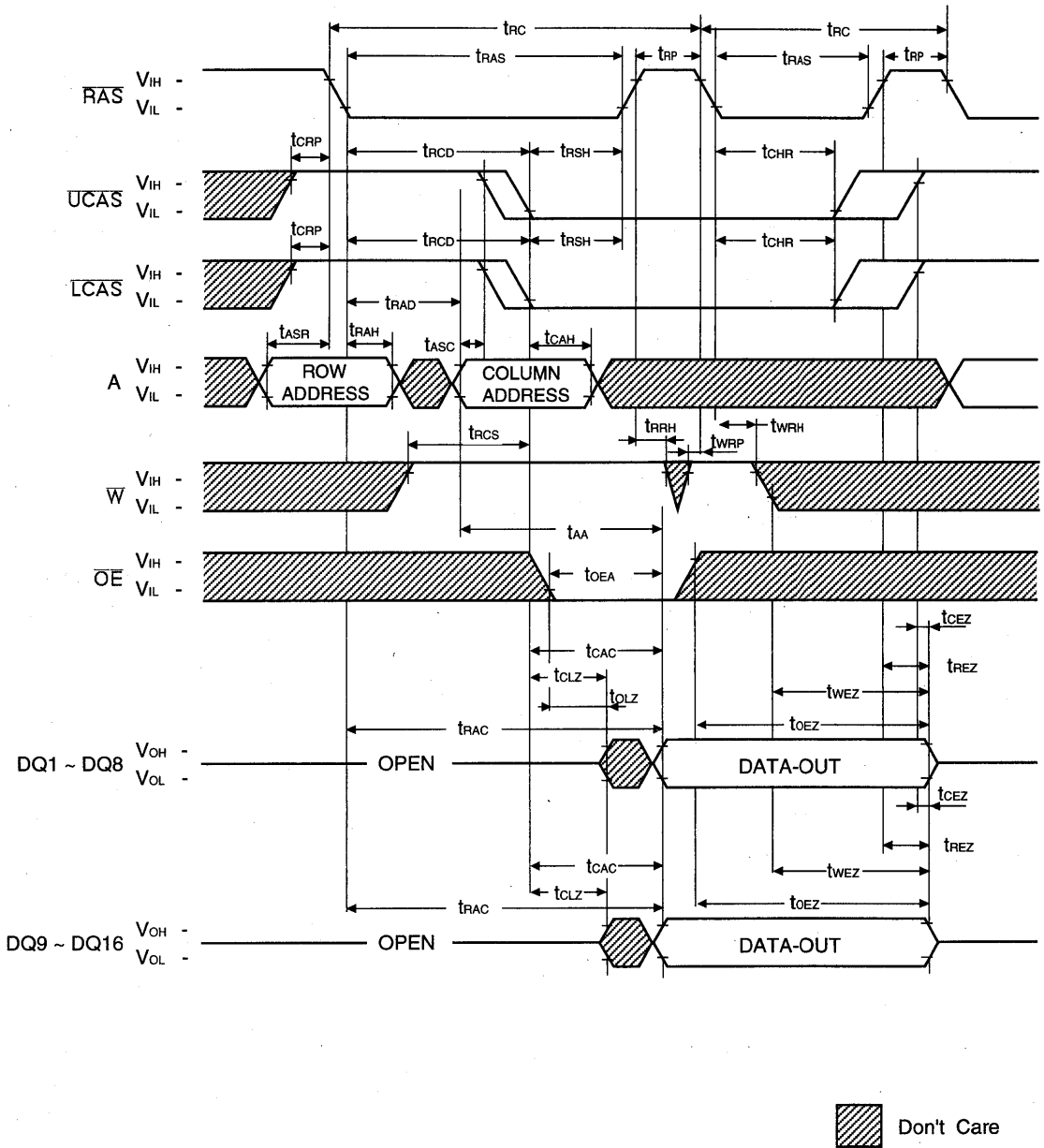
CAS-BEFORE-RAS SELF REFRESH CYCLE(LL-version)

NOTE : W, OE, A = Don't Care



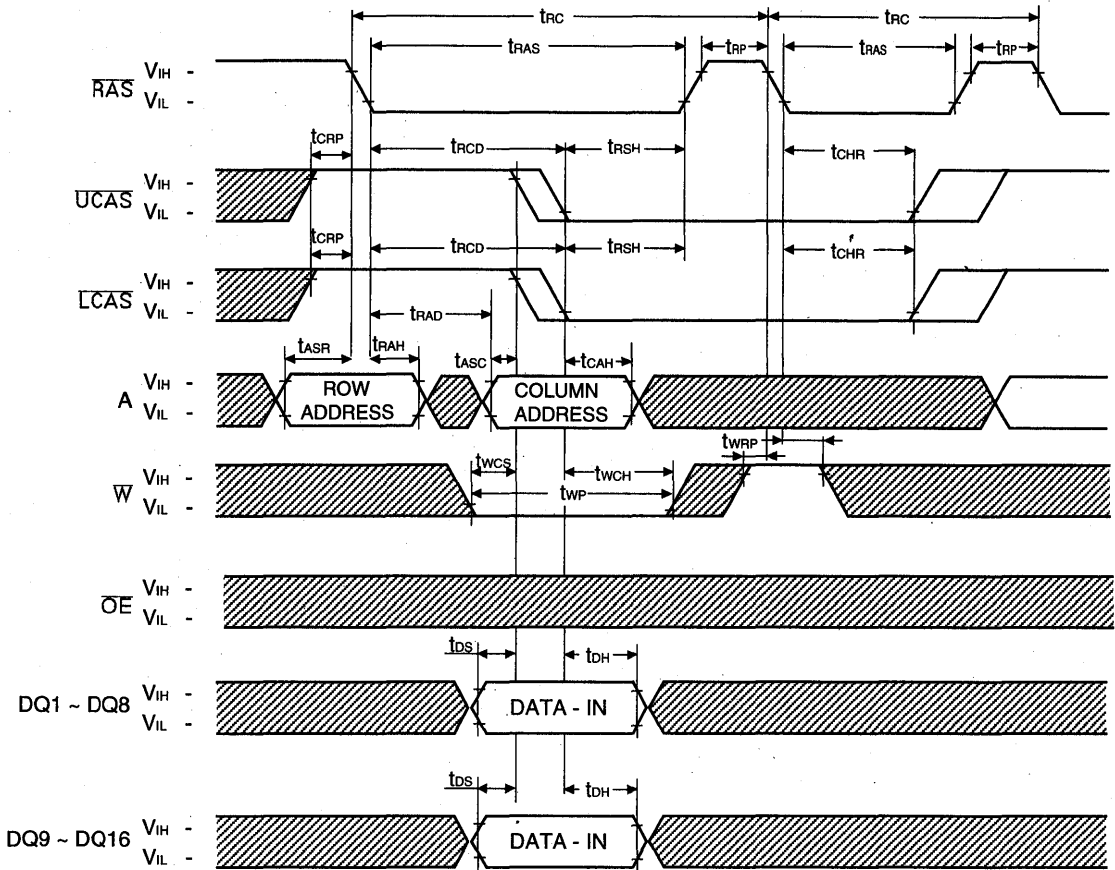
 Don't Care

HIDDEN REFRESH CYCLE (READ)



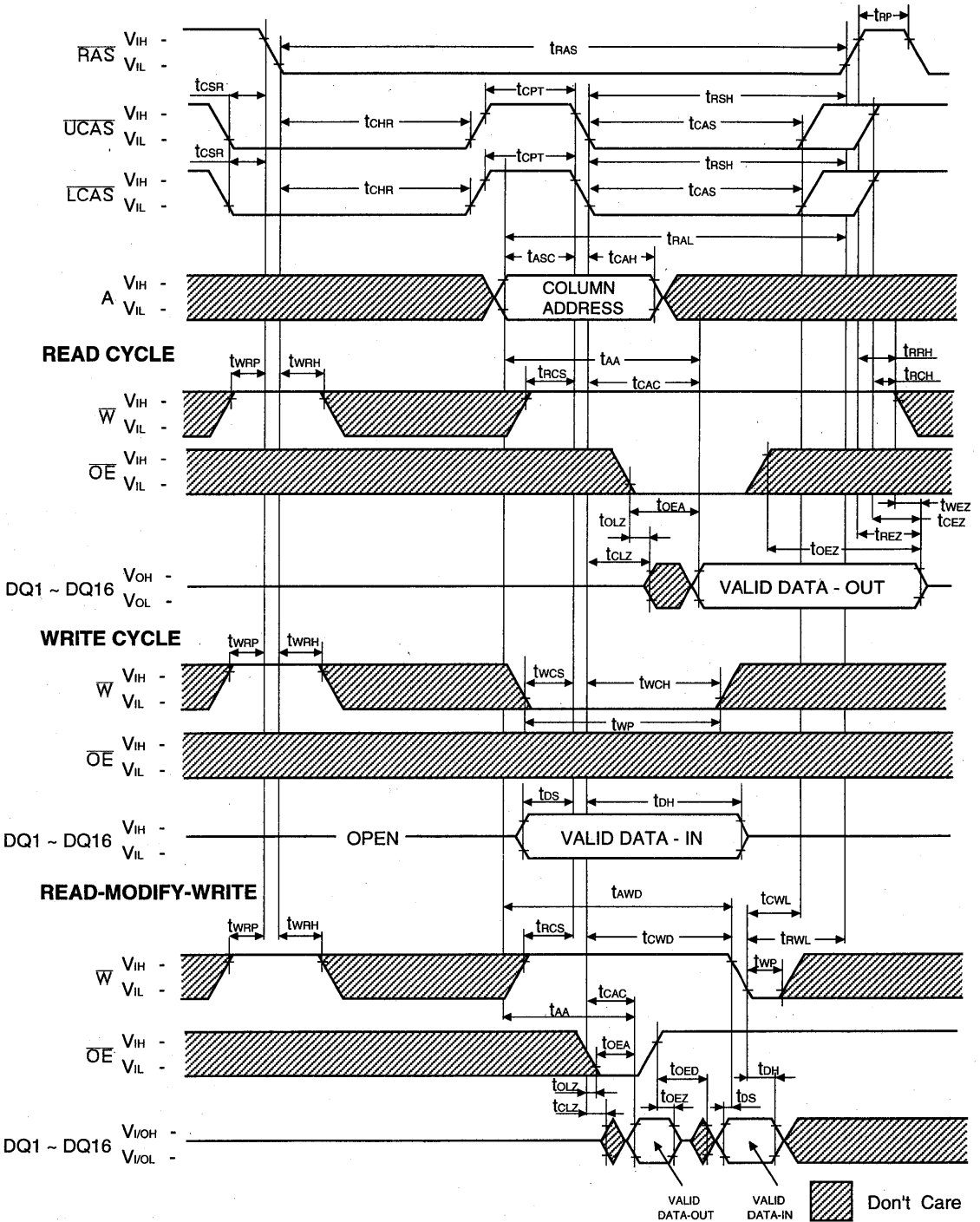
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



 Don't Care

CAS-BEFORE-RAS REFRESH CYCLE TEST CYCLE

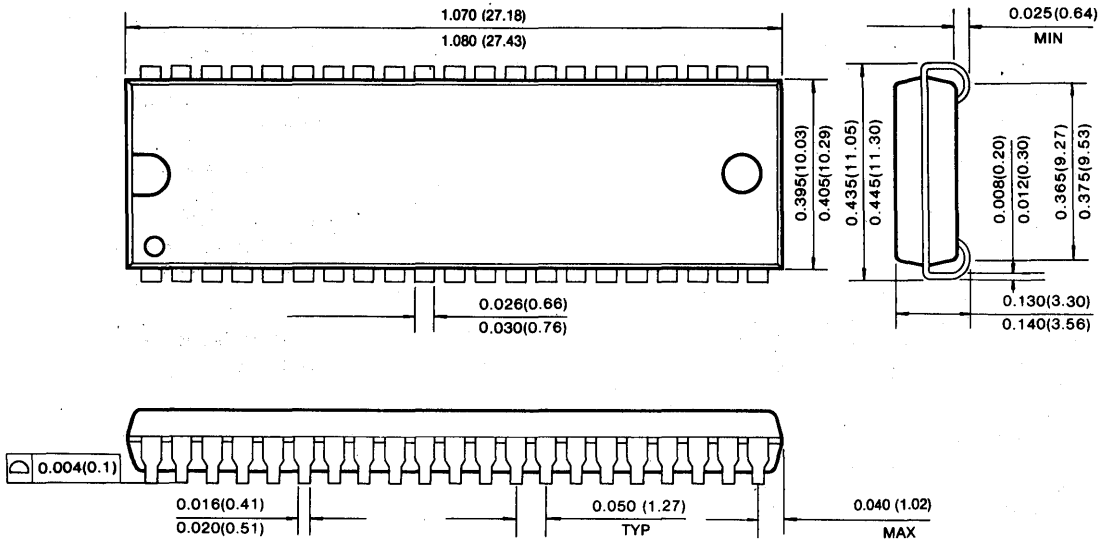


6

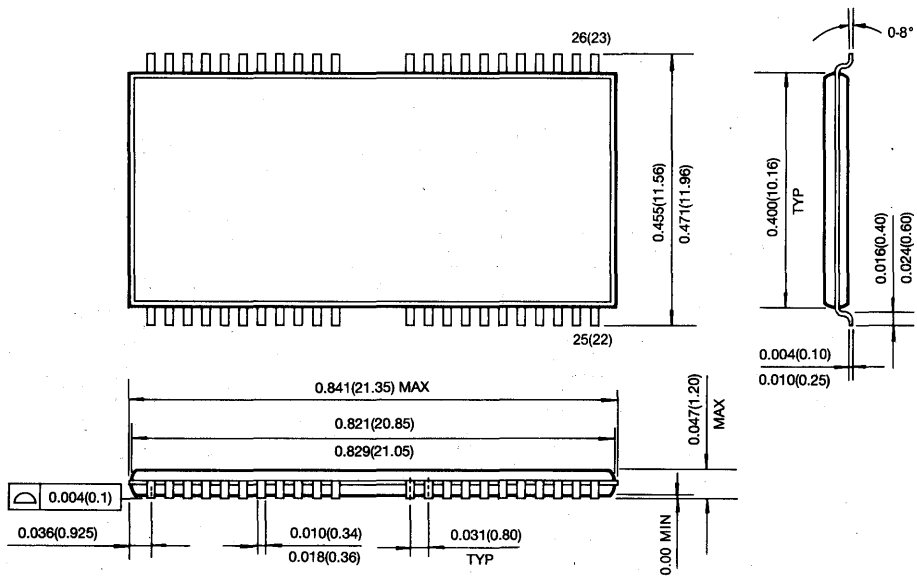
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM416V1000A-6/A-L6/A-F6	60ns	15ns	110ns
KM416V1000A-7/A-L7/A-F7	70ns	20ns	130ns
KM416V1000A-8/A-L8/A-F8	80ns	20ns	150ns

- Fast Page Mode operation
- 2 CAS Byte/Word Read/Write operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +3.3V±0.3V power supply
- Refresh Cycle
 - 4096 cycle/64ms (Normal)
 - 4096 cycle/128ms (L-version)
 - 4096 cycle/128ms (F-version)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

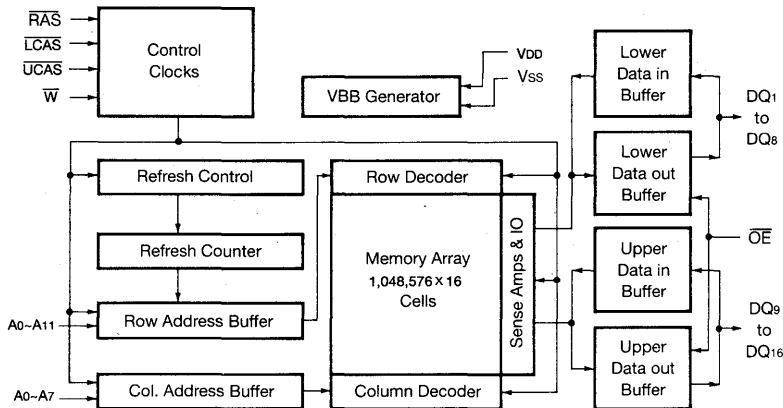
GENERAL DESCRIPTION

The Samsung KM416V1000A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

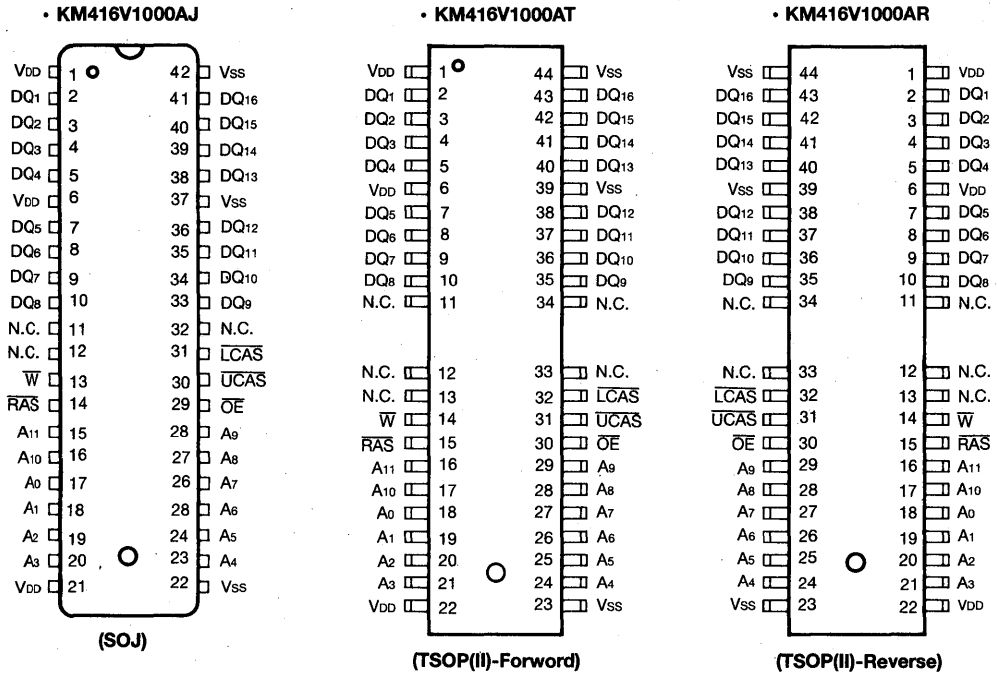
The KM416V1000A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1000A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
Vss	Ground
$\bar{R}AS$	Row Address Strobe
$\bar{U}CAS$	Upper Column Address Strobe
$\bar{L}CAS$	Lower Column Address Strobe
\bar{W}	Read/Write Input
$\bar{O}E$	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5 to 4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS, UCAS or LCAS, Address Cycling @trc=min.)	KM416V1000A-6/A-L6/A-F6 KM416V1000A-7/A-L7/A-F7 KM416V1000A-8/A-L8/A-F8 I _{CC1}	-	90 80 70	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{IH})	KM416V1000A KM416V1000A-L KM416V1000A-F I _{CC2}	-	2 1 1	mA mA mA
RAS-Only Refresh Current* (UCAS=LCAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM416V1000A-6/A-L6/A-F6 KM416V1000A-7/A-L7/A-F7 KM416V1000A-8/A-L8/A-F8 I _{CC3}	-	90 80 70	mA mA mA
Fast Page Mode Current* (RAS=V _{IL} , UCAS or LCAS, Address Cycling @trc=min.)	KM416V1000A-6/A-L6/A-F6 KM416V1000A-7/A-L7/A-F7 KM416V1000A-8/A-L8/A-F8 I _{CC4}	-	90 80 70	mA mA mA
Standby Current (RAS=UCAS=LCAS=W=V _{DD} -0.2V)	KM416V1000A KM416V1000A-L KM416V1000A-F I _{CC5}	-	1 300 200	mA μA μA
CAS-Before-RAS Refresh Current* (RAS, UCAS or LCAS Cycling @trc=min.)	KM416V1000A-6/A-L6/A-F6 KM416V1000A-7/A-L7/A-F7 KM416V1000A-8/A-L8/A-F8 I _{CC6}	-	90 80 70	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V, Input Low Voltage(V _{IL})=0.2V UCAS, LCAS= 0.2V DIN=Don't Care, trc=31.25μs (L-Version) trAS=trAS min-300ns	KM416V1000A-L I _{CC7}	-	450	μA

6



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=VIL W=OE=A0-A11=VDD-0.2V or 0.2V DQ1-DQ16=VDD-0.2V or 0.2V or Open	ICC3	-	250	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ VDD+0.3V, all other pins not under test=0 V)	II(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ VDD)	IO(L)	-10	10	μA
Output High Voltage Level (IOH=-2mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=2mA)	VOL	-	0.4	V

*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while RAS=VIL. In ICC4, Address can be changed maximum once while page mode cycle time tPC.

CAPACITANCE (TA=25°C, VDD=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1-DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VDD=3.3V ± 0.3V, See notes 1,2)

(Test condition : VIH/VIL=2.1V/0.8V, VOH/VOL=2.0V/0.8V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from RAS	tRAC		60		70		80	ns	3,4,11
Access time from CAS	tCAC		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
RAS precharge time	tRP	40		50		60		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	tRSH	15		20		20		ns	
CAS hold time	tCSH	60		70		80		ns	
CAS pulse width	tCAS	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	4
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	tROH	15		20		20		ns	

AC CHARACTERISTICS (Continued)

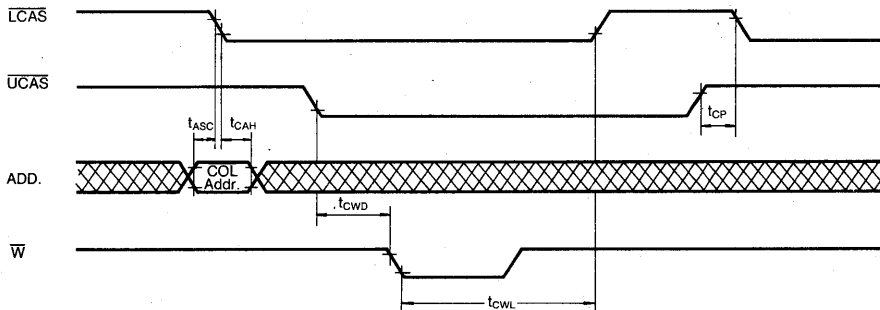
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} access time	toEA		15		20		20	ns	
\overline{OE} to data delay	toED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	toEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	toEH	15		20		20		ns	
\overline{RAS} pulse width (F-ver)	trASS	100		100		100		μ s	19
\overline{RAS} precharge time (F-ver)	trPS	110		130		150		ns	19
\overline{CAS} hold time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416V1000A/A-L/A-F Truth Table

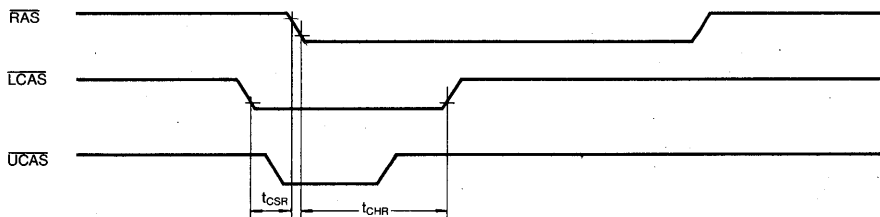
RAS	LCAS	UCAS	W	\overline{OE}	DQ ₁ -DQ ₈	DQ ₉ -DQ ₁₆	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL Loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWd} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWd} \geq t_{RWd}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
13. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
14. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.

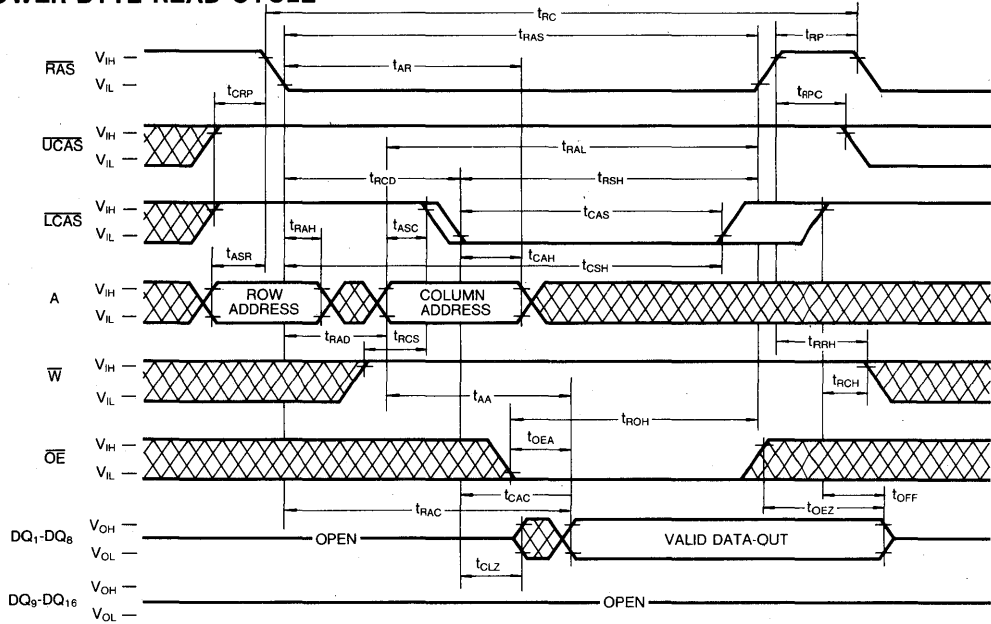


16. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
17. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.

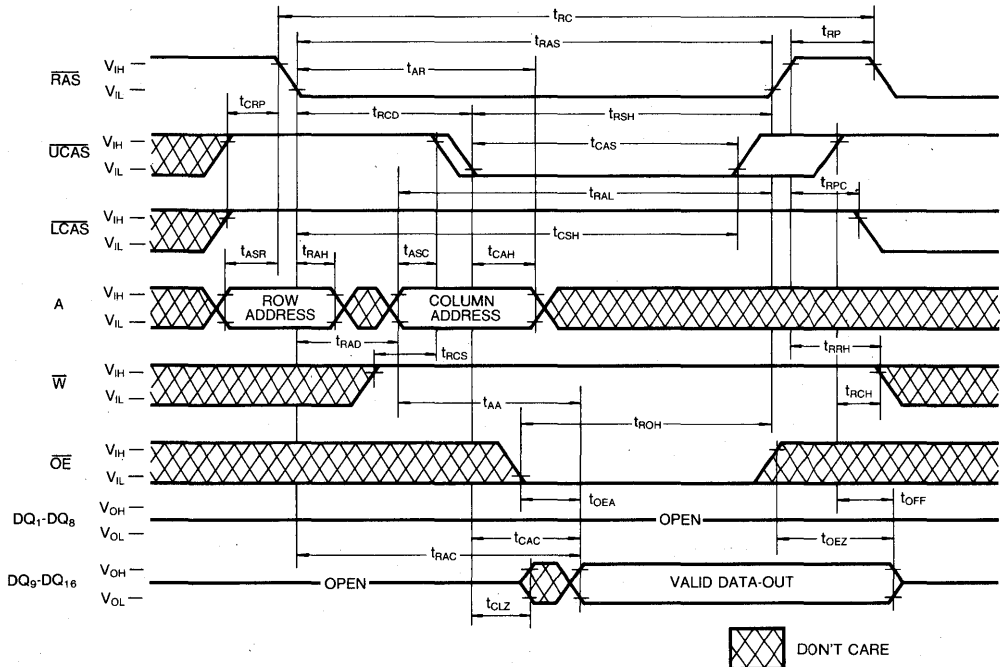


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE

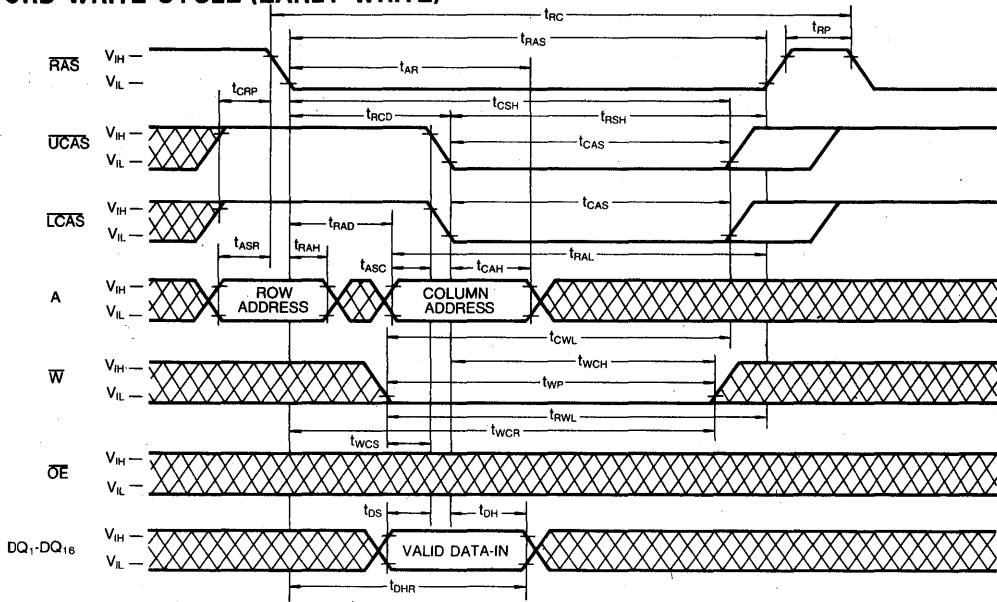


UPPER BYTE READ CYCLE

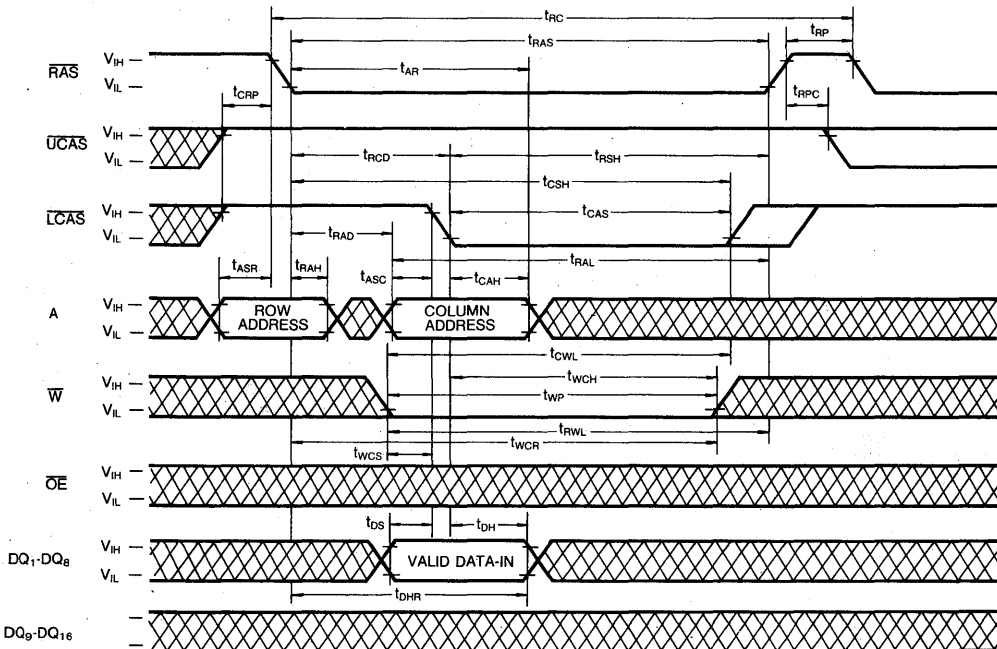


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



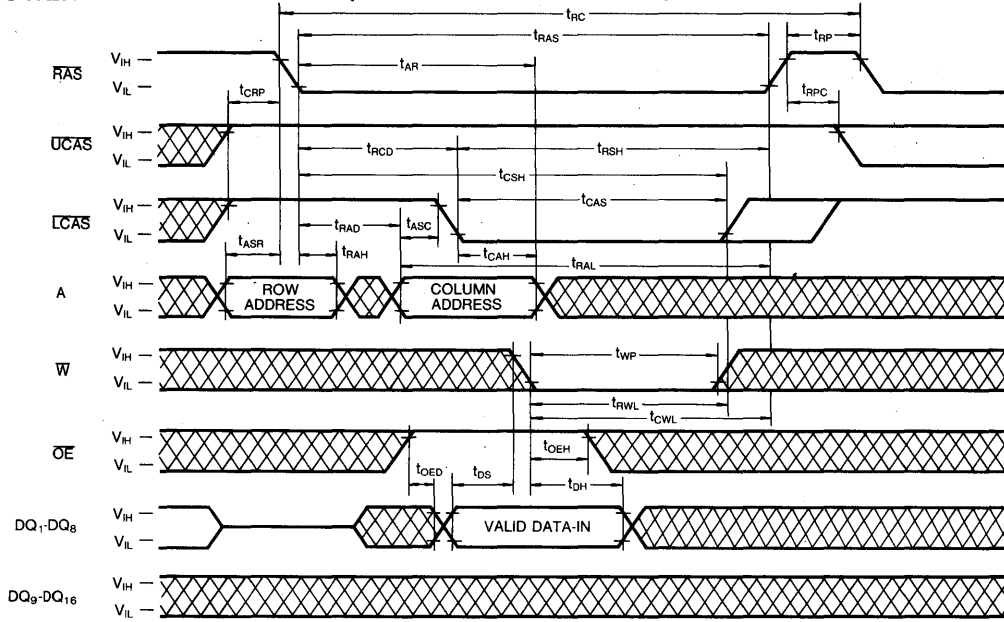
LOWER BYTE WRITE CYCLE (EARLY WRITE)



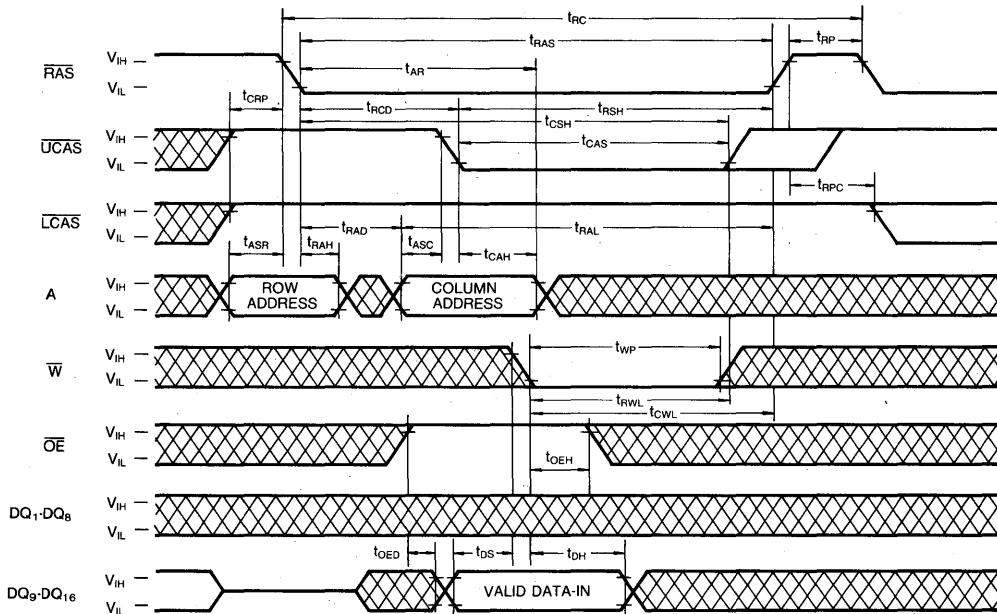
 DONT CARE

TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



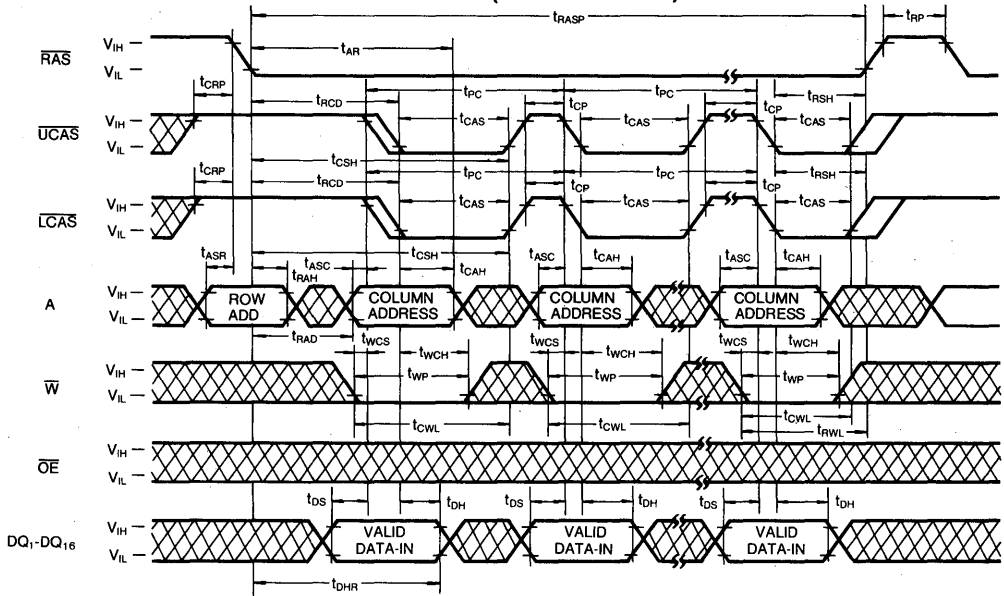
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



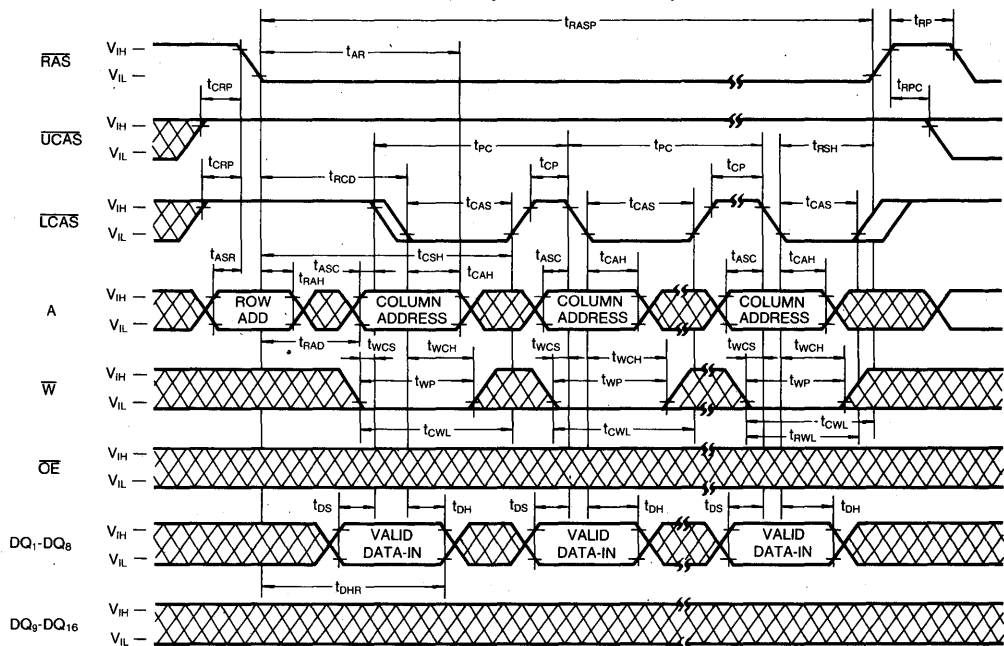
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



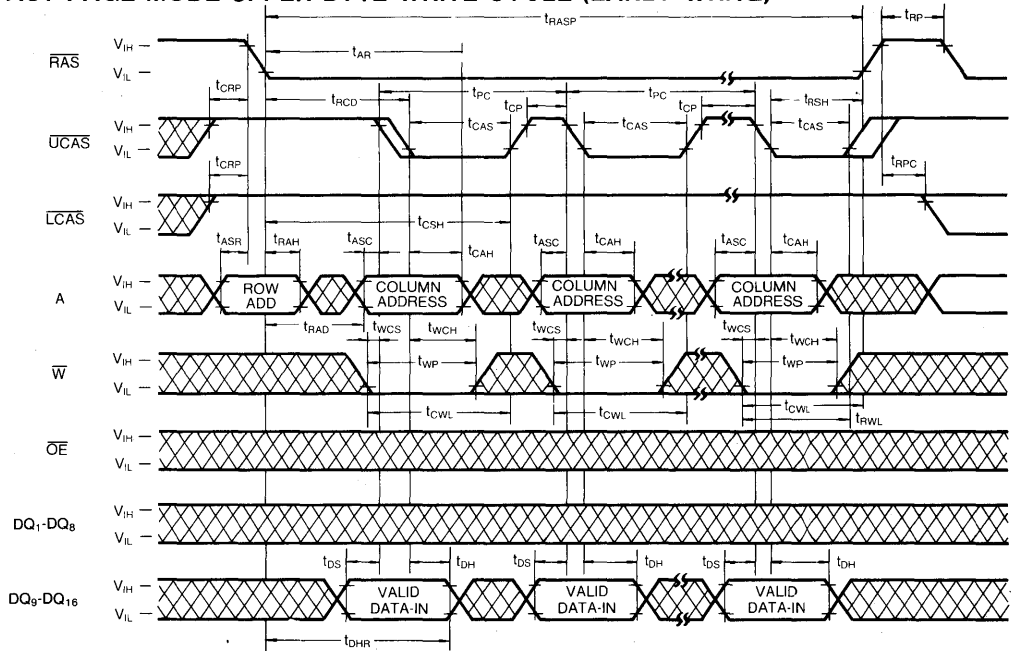
FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)



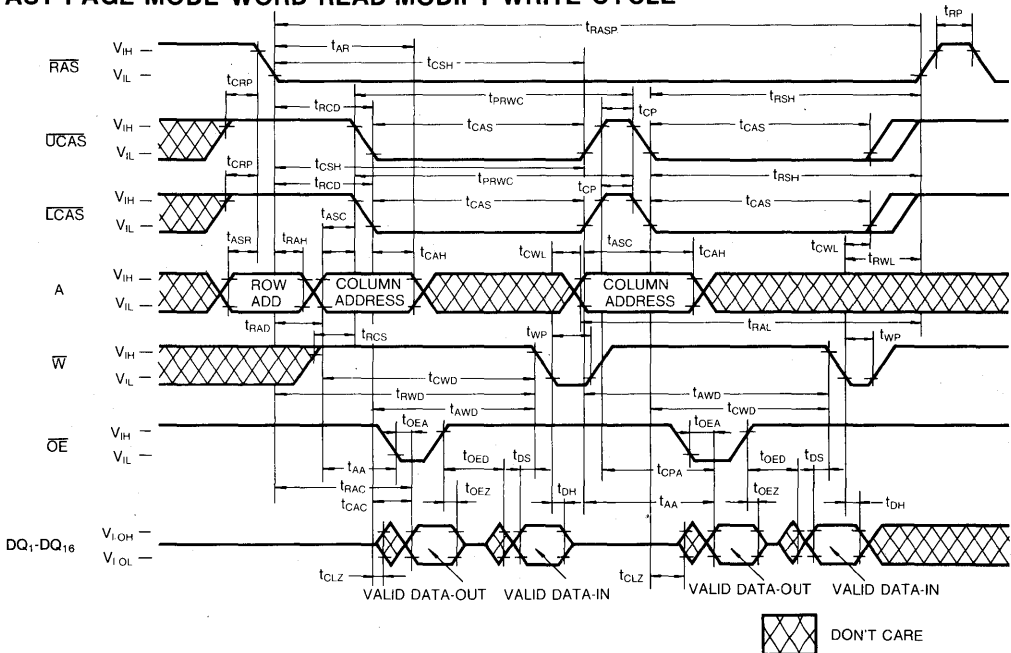
 **DONT CARE**

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



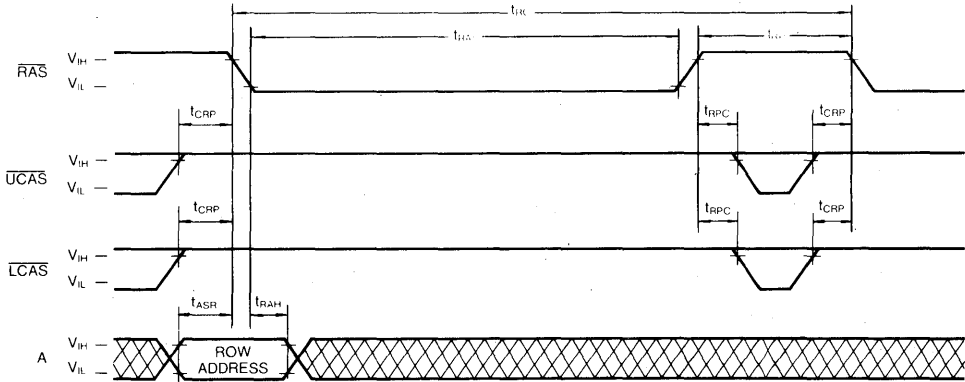
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



TIMING DIAGRAMS (Continued)

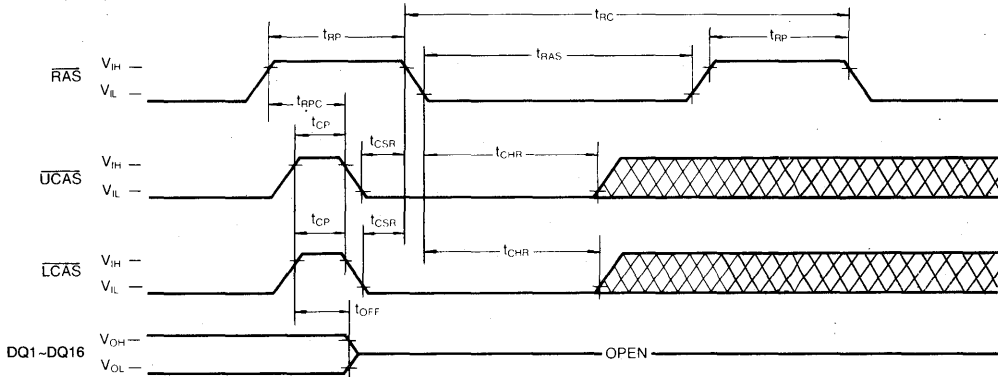
RAS ONLY REFRESH CYCLE

NOTE: \overline{W} , \overline{OE} = Don't Care



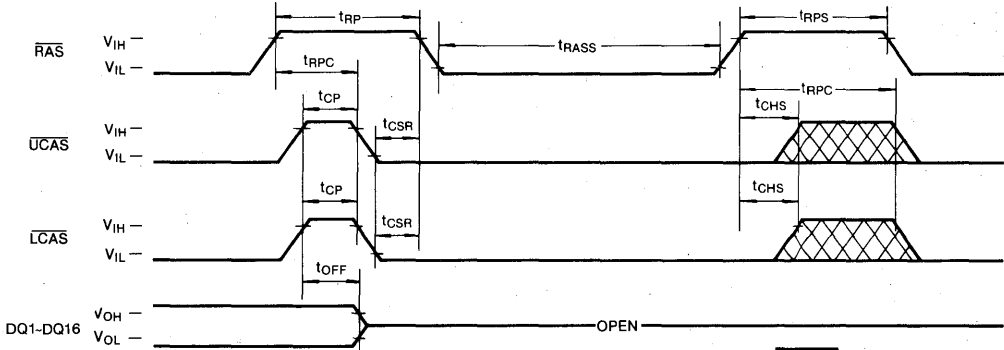
CAS-BEFORE-RAS REFRESH CYCLE


NOTE: \overline{W} , \overline{OE} , \overline{A} = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE (Self refresh only)

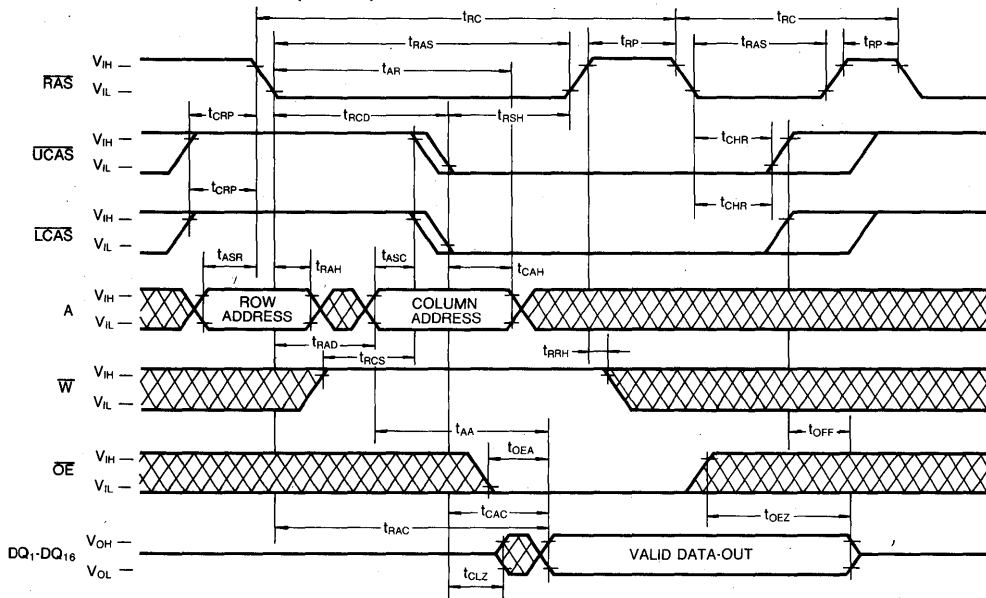
NOTE: \overline{W} , \overline{OE} , \overline{A} = Don't Care



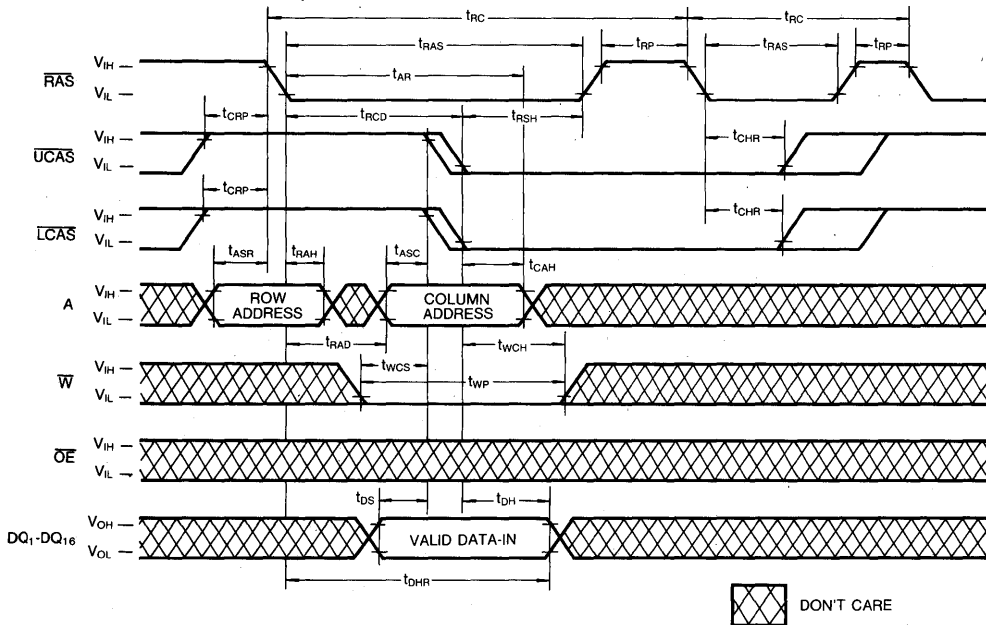
 DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



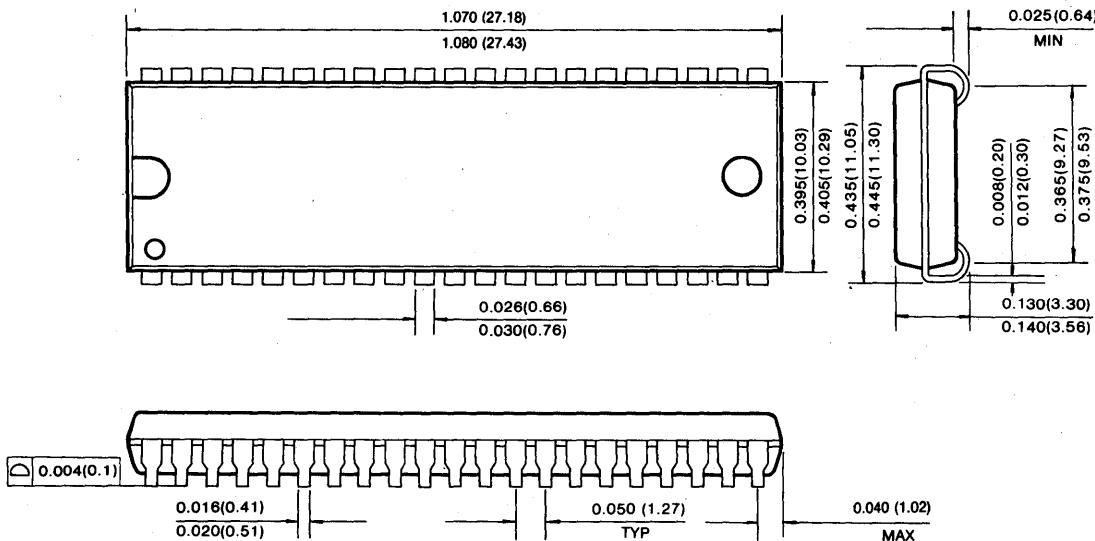
HIDDEN REFRESH CYCLE (WRITE)



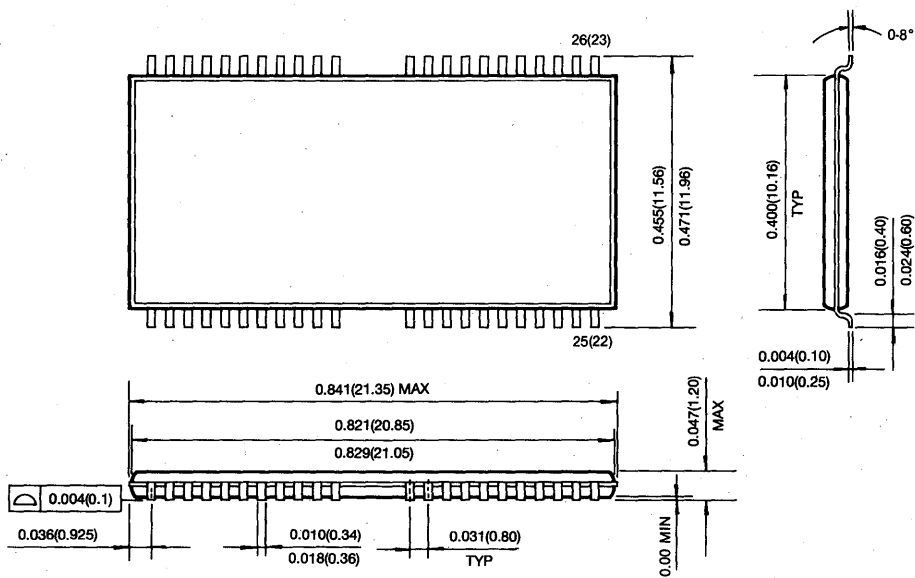
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• **Performance range:**

	trAC	tcAC	trC
KM416V1200A-6/A-L6/A-F6	60ns	15ns	110ns
KM416V1200A-7/A-L7/A-F7	70ns	20ns	130ns
KM416V1200A-8/A-L8/A-F8	80ns	20ns	150ns

- **Fast Page Mode operation**
- **2 CAS Byte/Word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V ± 0.3V power supply**
- **Refresh Cycle**
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/128ms (F-version)
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

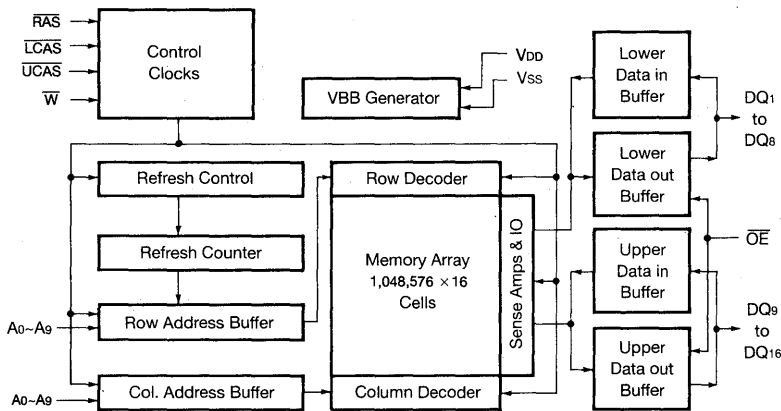
GENERAL DESCRIPTION

The Samsung KM416V1200A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

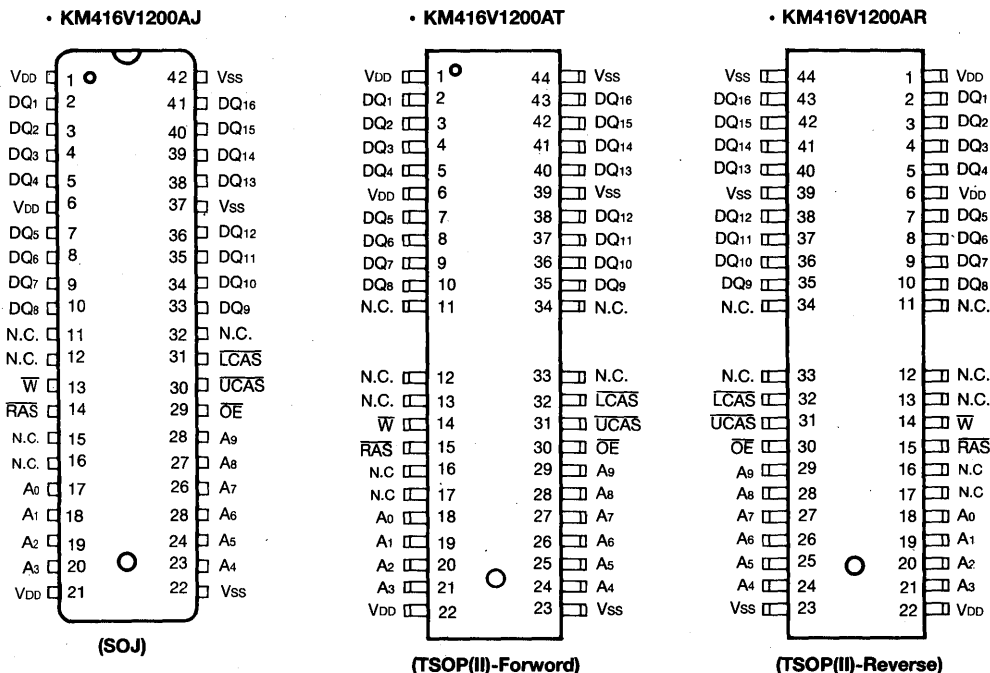
The KM416V1200A/A-L/A-F features Fast Page Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1200A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
\bar{W}	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5 to 4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS, UCAS or LCAS, Address Cycling @trc=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I _{CC1}	150	mA
			140	mA
			130	mA
Standby Current (RAS=UCAS=LCAS=̄W=V _{IH})	KM416V1200A KM416V1200A-L KM416V1200A-F	I _{CC2}	2	mA
			1	mA
			1	mA
RAS-Only Refresh Current* (UCAS=LCAS=V _{IH} , RAS, Address Cycling @trc=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I _{CC3}	150	mA
			140	mA
			130	mA
Fast Page Mode Current* (RAS=V _{IL} , UCAS or LCAS, Address Cycling @tpc=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I _{CC4}	100	mA
			90	mA
			80	mA
Standby Current (RAS=UCAS=LCAS=̄W=V _{DD} -0.2V)	KM416V1200A KM416V1200A-L KM416V1200A-F	I _{CC5}	1	mA
			300	μA
			200	μA
CAS-Before-RAS Refresh Current* (RAS, UCAS or LCAS Cycling @trc=min.)	KM416V1200A-6/A-L6/A-F6 KM416V1200A-7/A-L7/A-F7 KM416V1200A-8/A-L8/A-F8	I _{CC6}	150	mA
			140	mA
			130	mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V, Input Low Voltage(V _{IL})=0.2V UCAS, LCAS=0.2V DIN=Don't Care, trc=125μs (L-Version) trAS=trAS min-300ns	KM416V1200A-L	I _{CC7}	350	μA

6

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A9=VDD-0.2V or 0.2V DQ1-DQ16=VDD-0.2V or 0.2V or Open	Iccs	-	250	μA
Input Leakage Current (Any input 0 ≤ VIN ≤ VDD+0.3V, all other pins not under test=0 V)	Ii(L)	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ VOUT ≤ VDD)	Io(L)	-10	10	μA
Output High Voltage Level (IOH=-2mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=2mA)	VOL	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=VIL. In Icc4, Address can be changed maximum once while page mode cycle time tpc.

CAPACITANCE (TA=25°C, VDD=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A9)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1~DQ16)	CDQ	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VDD=3.3V ± 0.3V, See notes 1,2)

(Test condition : VIH/VIL=2.1V/0.8V, VOH/VOL=2.0V/0.8V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	110		130		150		ns	
Read-modify-write cycle time	trwc	155		185		205		ns	
Access time from RAS	trac		60		70		80	ns	3,4,11
Access time from CAS	tcac		15		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	toff	0	15	0	15	0	15	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
RAS precharge time	trp	40		50		60		ns	
RAS pulse width	trAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	15		20		20		ns	
CAS hold time	tCSH	60		70		80		ns	
CAS pulse width	tcAS	15	10,000	20	10,000	20	10,000	ns	
RAS to CAS delay time	trCD	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	30	15	35	15	40	ns	11

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		15		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	15		15		20		ns	
Data-in set-up time	tDS	0		0		0		ns	10
Data-in hold time	tDH	10		15		15		ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		95		105		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		60		65		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	60		65		70		ns	
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		10		ns	
$\overline{\text{RAS}}$ precharge to $\overline{\text{CAS}}$ hold time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20		25		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Fast Page mode cycle time	tPC	40		45		50		ns	
Fast Page mode read-modify-write cycle time	tPRWC	80		95		100		ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	tRASP	60	200K	70	200K	80	200K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{CAS}}$ precharge time (Fast page mode)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	tROH	15		20		20		ns	

6



AC CHARACTERISTICS (Continued)

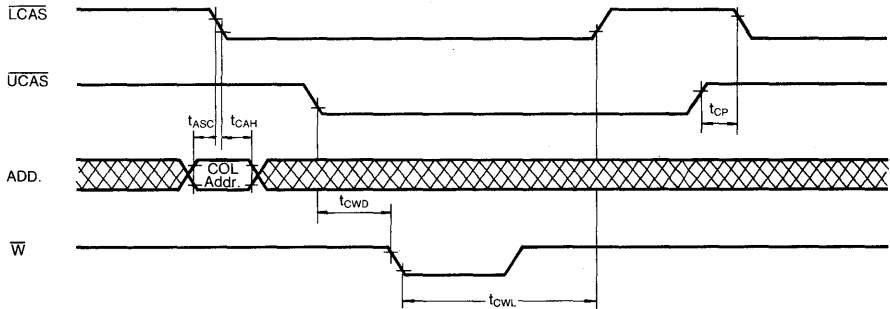
Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{OE} access time	tOEA		15		20		20	ns	
\overline{OE} to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	0	15	0	20	0	20	ns	
\overline{OE} command hold time	tOEH	15		20		20		ns	
\overline{RAS} pulse width (F-ver)	tRASS	100		100		100		μ s	19
\overline{RAS} precharge time (F-ver)	tRPS	110		130		150		ns	19
\overline{CAS} hold time (F-ver)	tCHS	-50		-50		-50		ns	19

KM416V1200A/A-L/A-F Truth Table

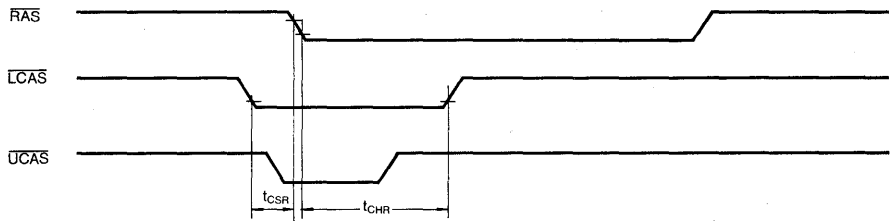
\overline{RAS}	\overline{LCAS}	\overline{UCAS}	\overline{W}	\overline{OE}	DQ1-DQ8	DQ9-DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 $\overline{\text{RAS}}$ -only or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH(\min)}$ and $V_{IL(\max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(\min)}$ and $V_{IL(\max)}$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the $t_{\text{RCD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RCD}(\max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}(\max)}$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}(\max)}$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}(\max)}$.
7. $t_{\text{OFF}(\max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating aparameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}(\min)}$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}(\min)}$, $t_{\text{RWD}} \geq t_{\text{RWD}(\min)}$, $t_{\text{AWD}} \geq t_{\text{AWD}(\min)}$ then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
11. Operation within the $t_{\text{RAD}(\max)}$ limit insures that $t_{\text{RAC}(\max)}$ can be met. $t_{\text{RAD}(\max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}(\max)}$ limit, then access time is controlled by t_{AA} .
12. t_{ASC} , t_{CAH} are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
13. t_{CP} is specified from the last $\overline{\text{CAS}}$ rising edge in the previous cycle to the first $\overline{\text{CAS}}$ falling edge in the next cycle.
14. t_{CWD} is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
15. t_{CWL} is specified from $\overline{\text{W}}$ falling edge to the earlier $\overline{\text{CAS}}$ rising edge.

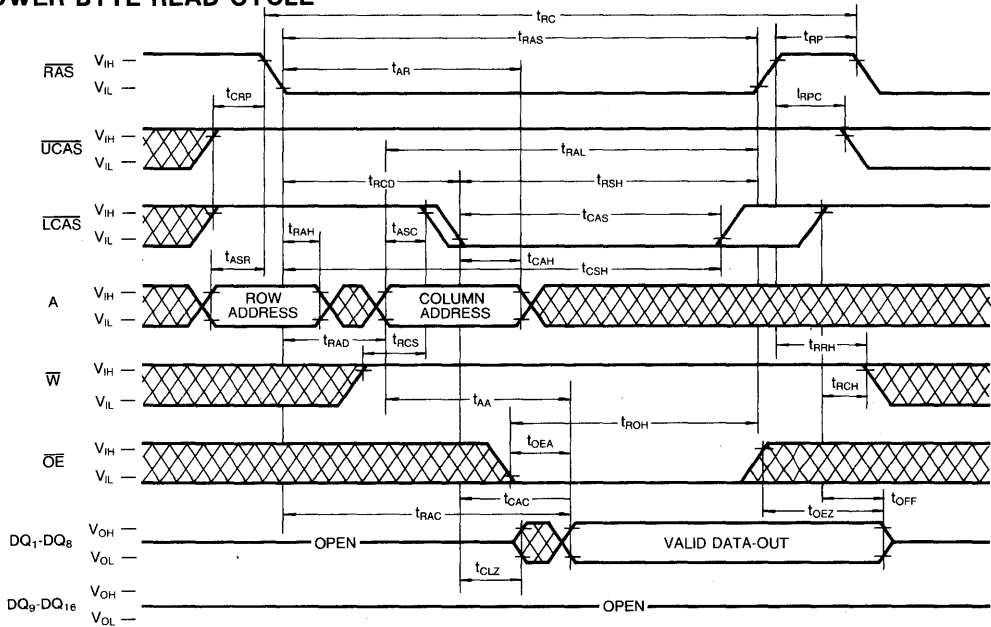


16. t_{CSR} is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
17. t_{CHR} is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.

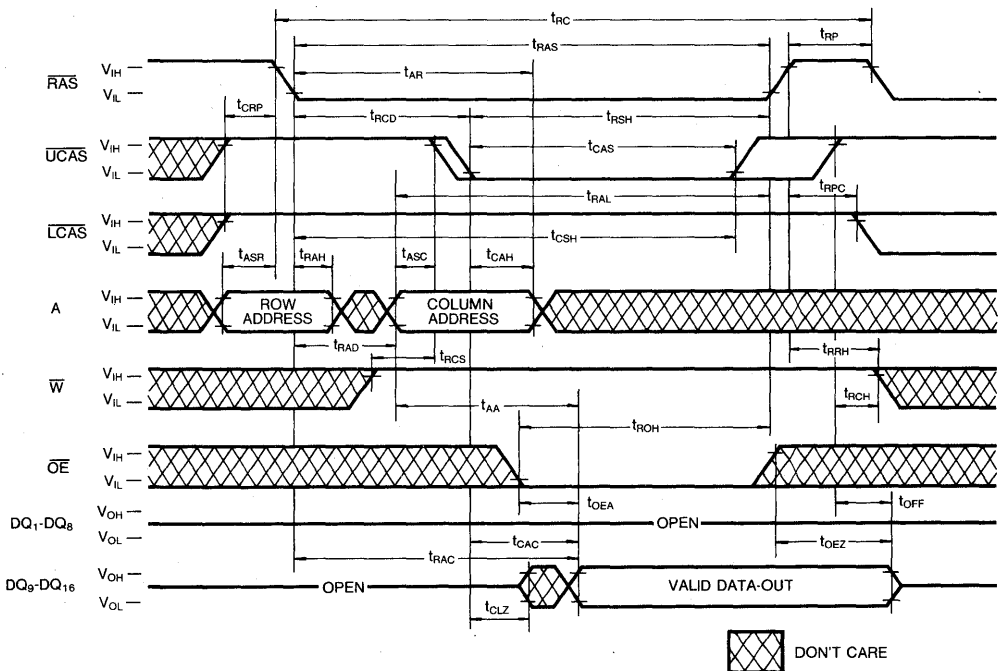


TIMING DIAGRAMS (Continued)

LOWER BYTE READ CYCLE



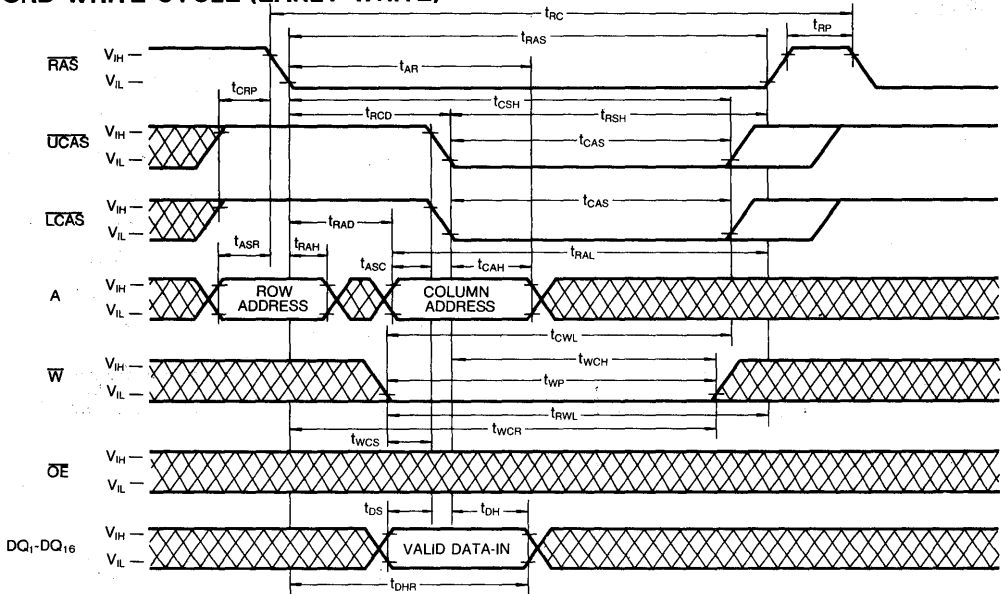
UPPER BYTE READ CYCLE



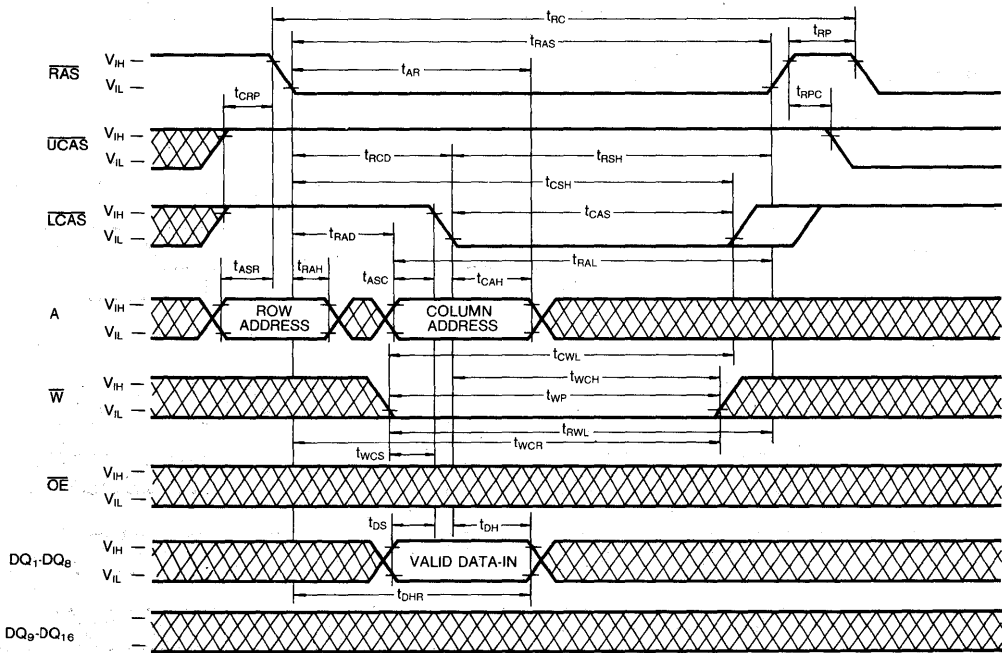
 DON'T CARE


TIMING DIAGRAMS (Continued)

WORD WRITE CYCLE (EARLY WRITE)



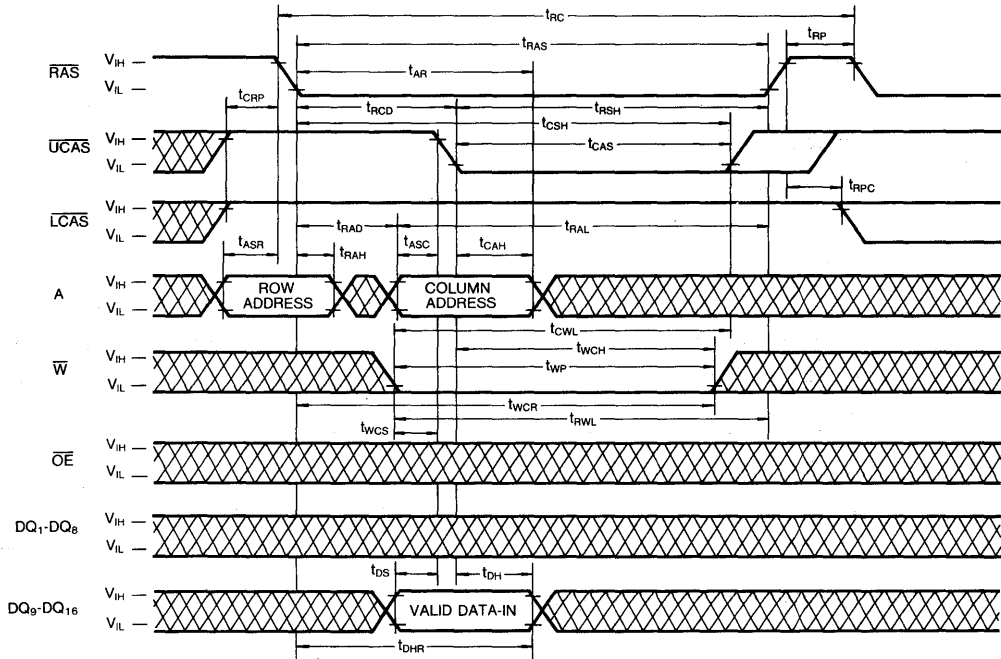
LOWER BYTE WRITE CYCLE (EARLY WRITE)



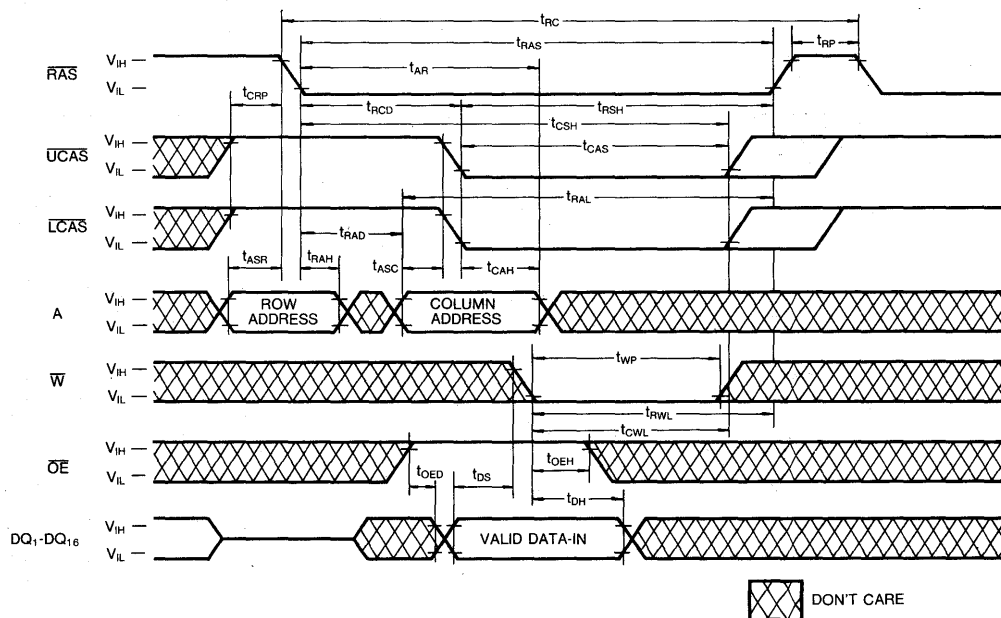
 DON'T CARE

TIMING DIAGRAMS (Continued)

UPPER BYTE WRITE CYCLE (EARLY WRITE)

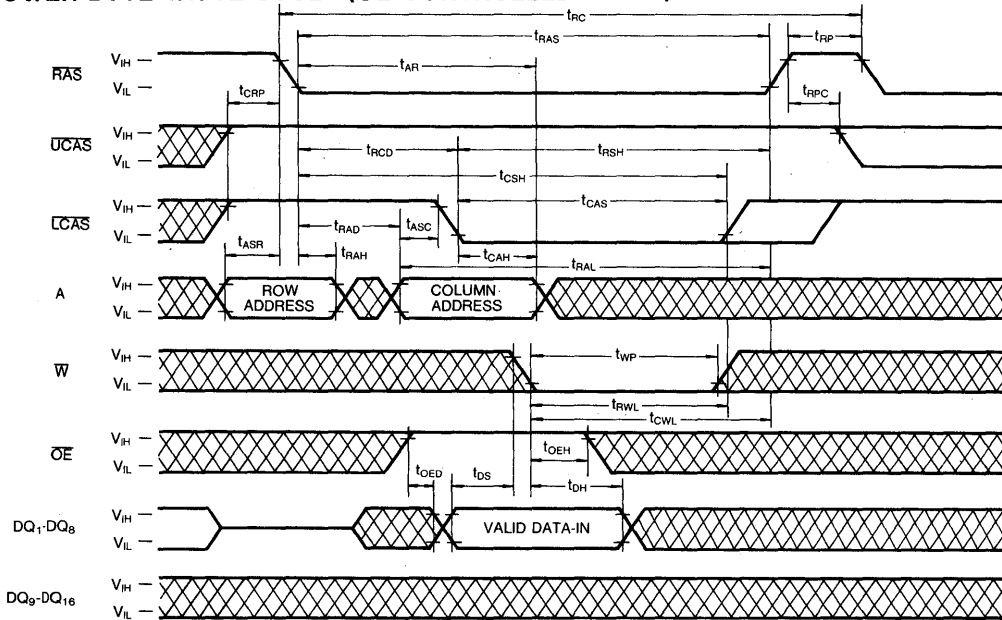


WORD WRITE CYCLE ($\overline{\text{OE}}$ CONTROLLED WRITE)

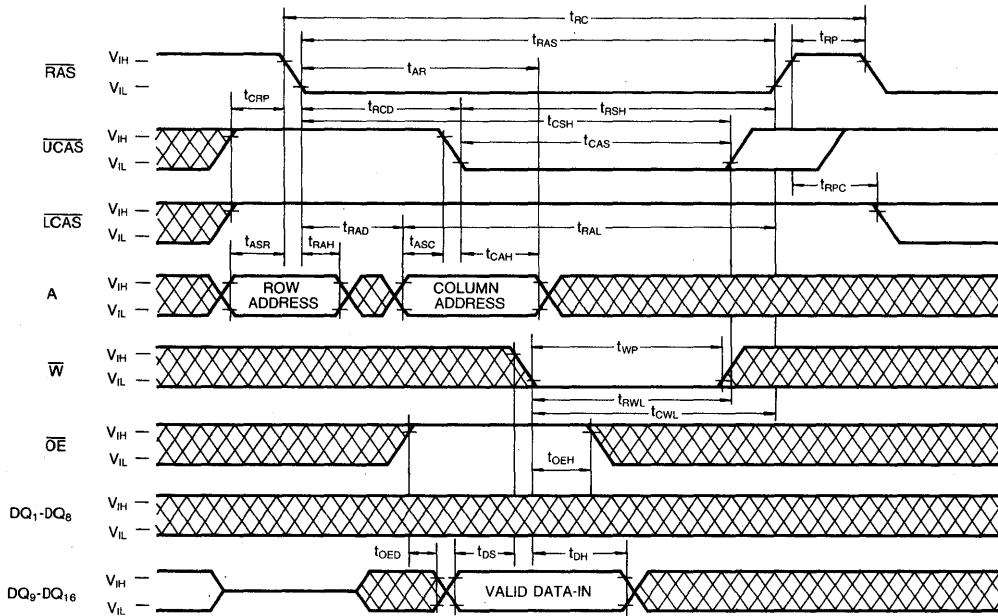


TIMING DIAGRAMS (Continued)

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



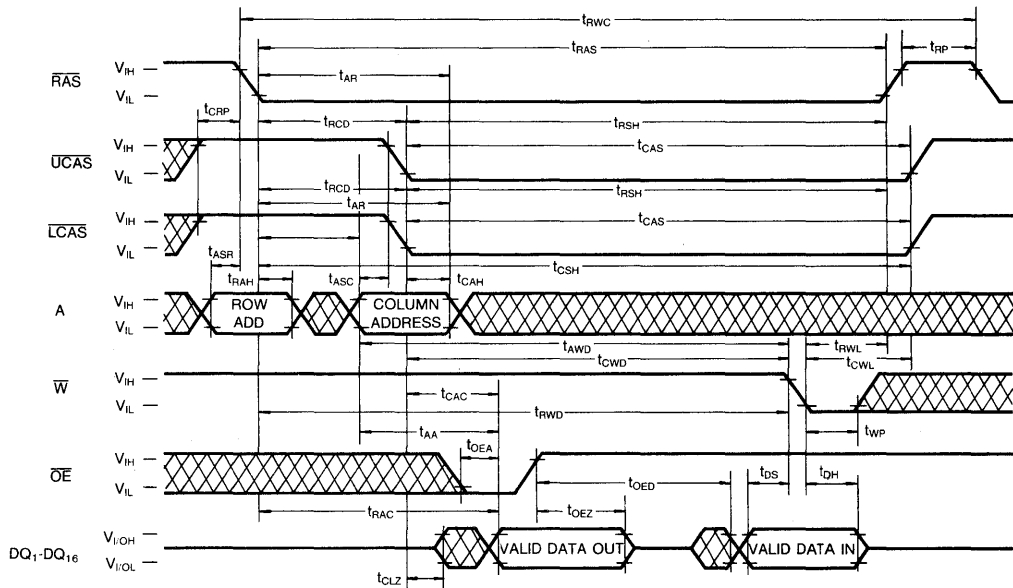
UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



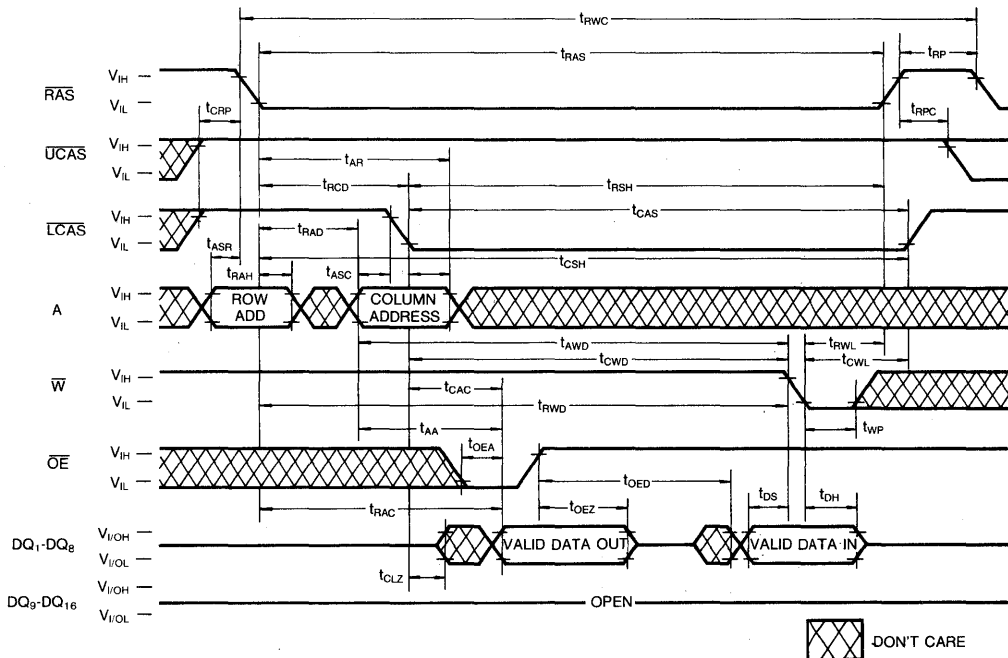
 DON'T CARE

TIMING DIAGRAMS (Continued)

WORD READ-MODIFY-WRITE CYCLE

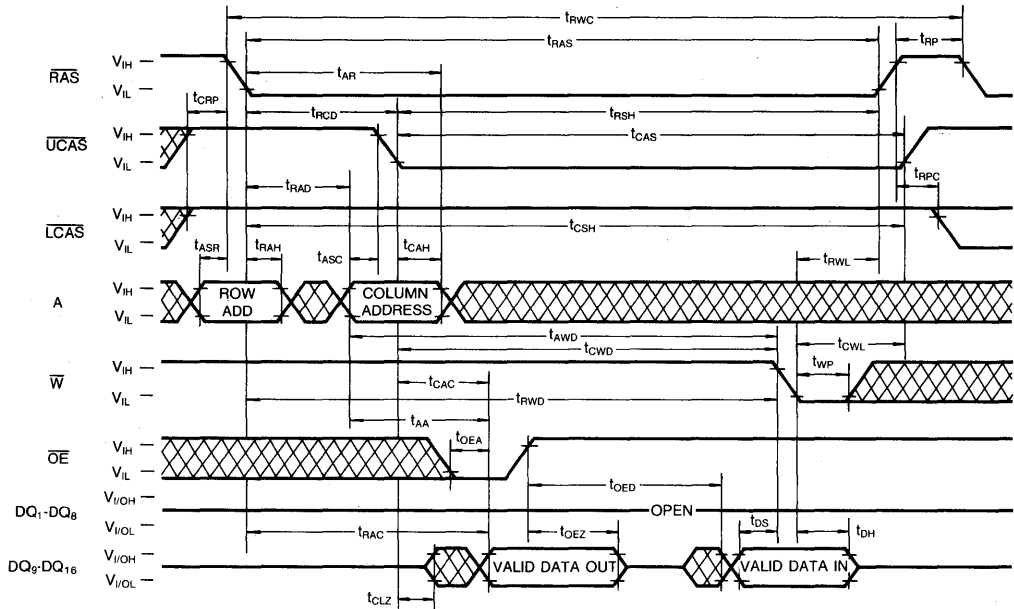


READ-MODIFY-LOWER-BYTE-WRITE CYCLE

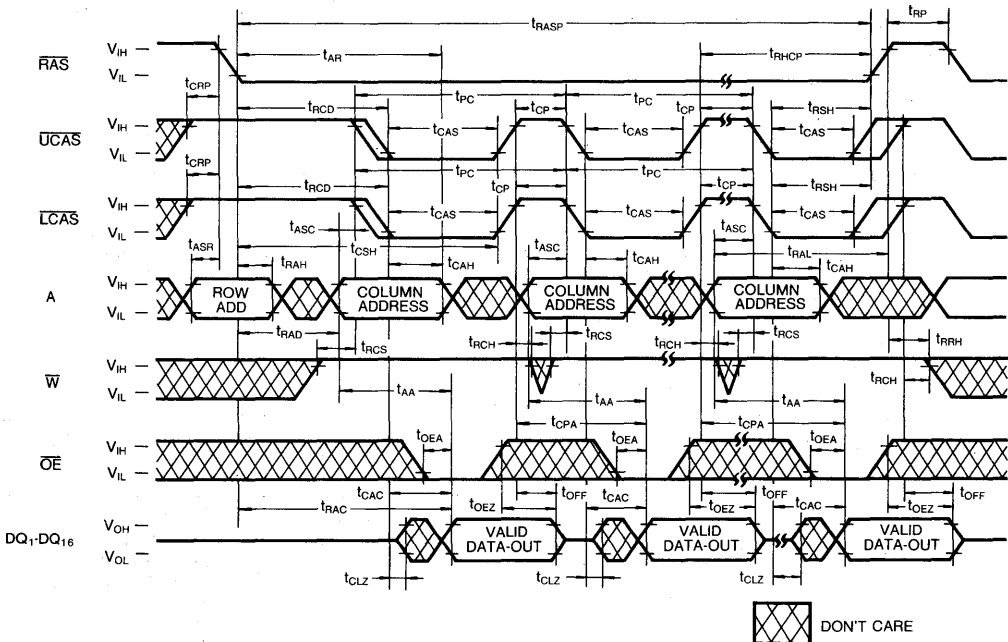


TIMING DIAGRAMS (Continued)

READ-MODIFY-UPPER-BYTE-WRITE CYCLE



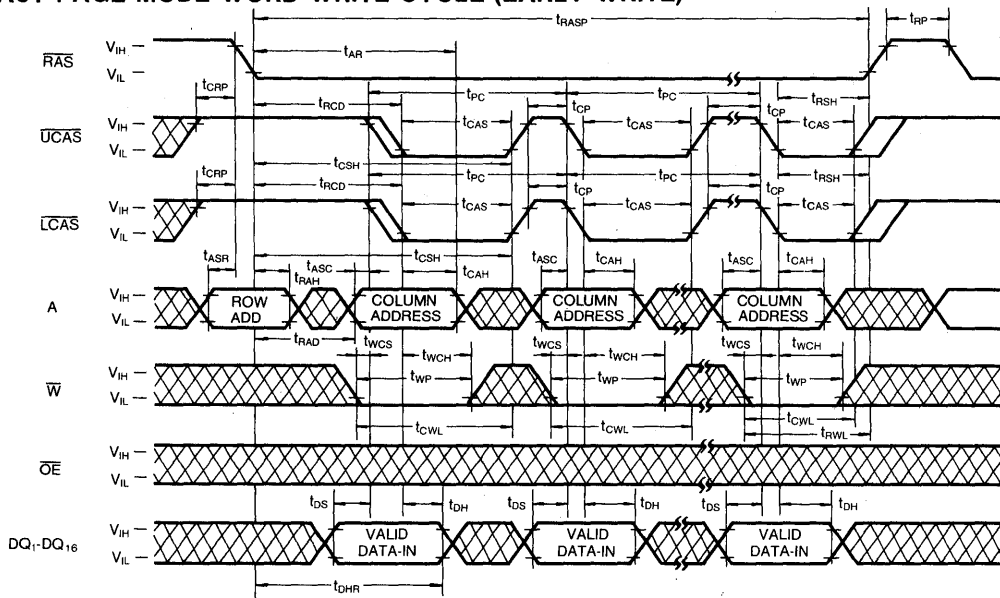
FAST PAGE MODE WORD READ CYCLE



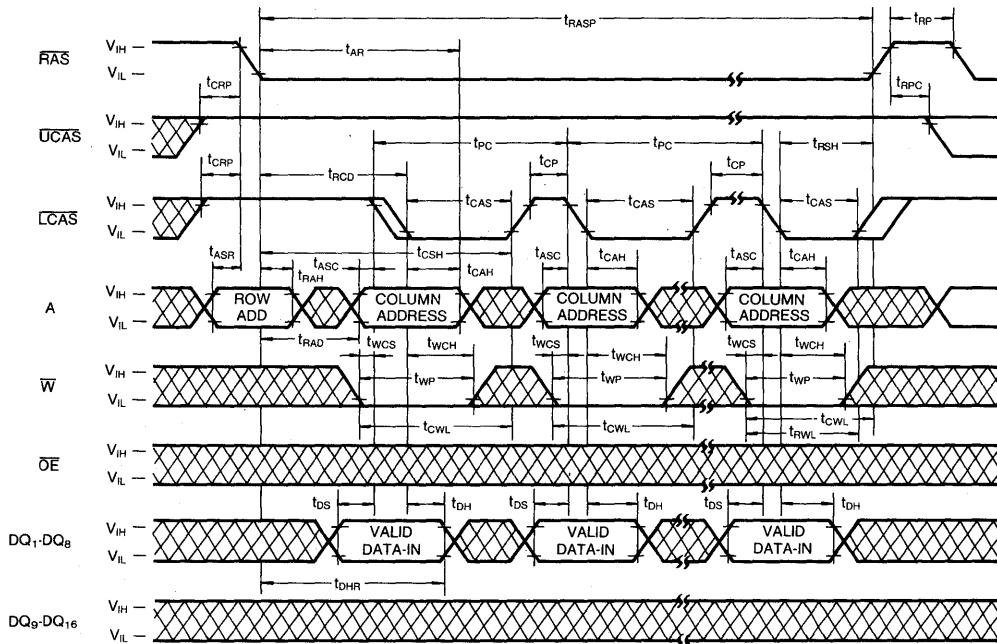
DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE WORD WRITE CYCLE (EARLY WRITE)



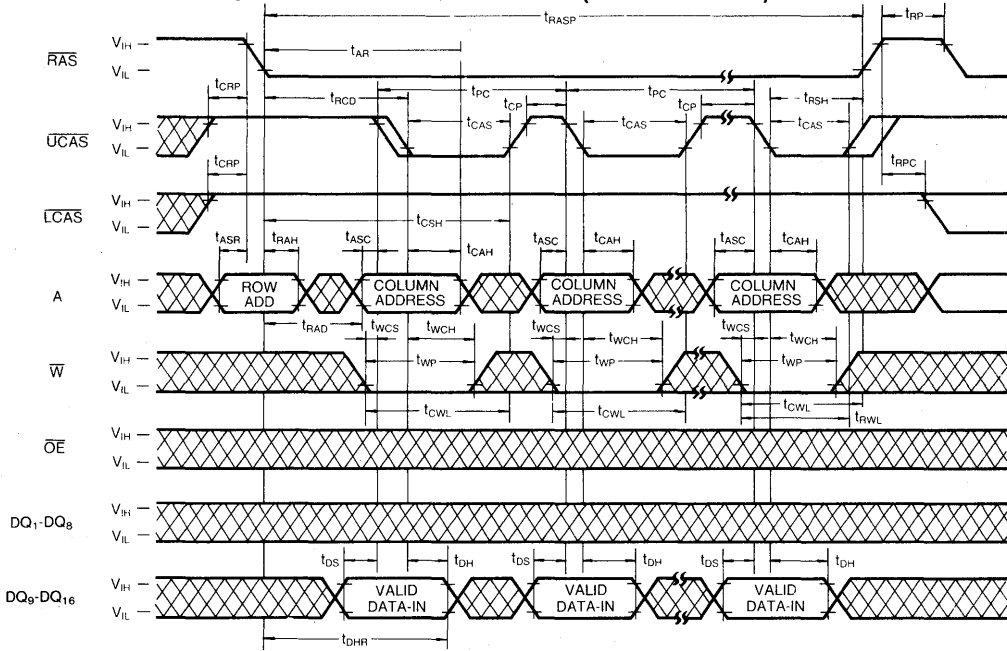
FAST PAGE MODE LOWER BYTE WRITE (EARLY WRITE)



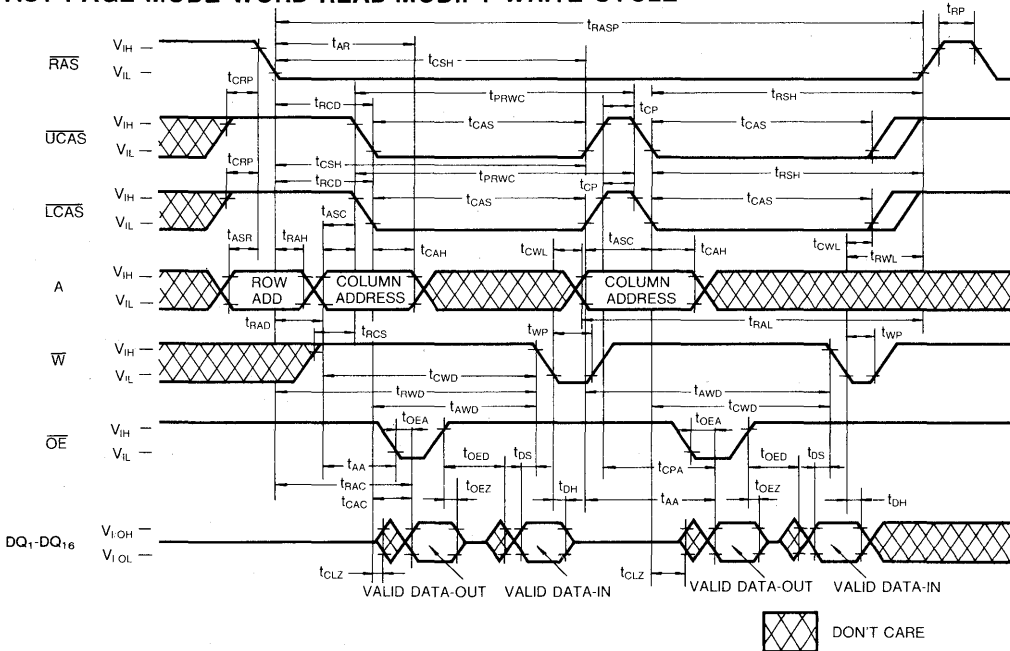
 DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



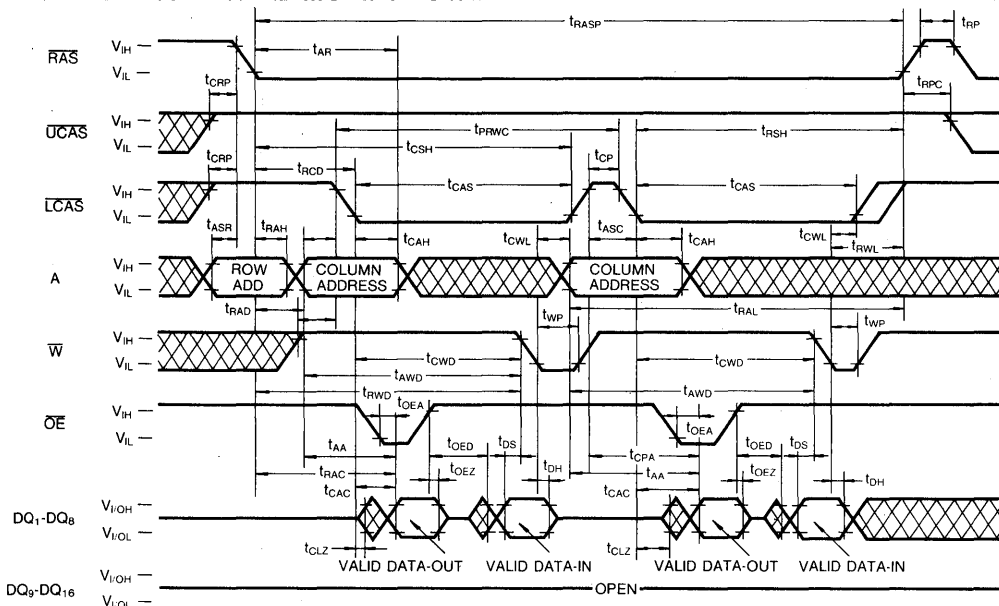
FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



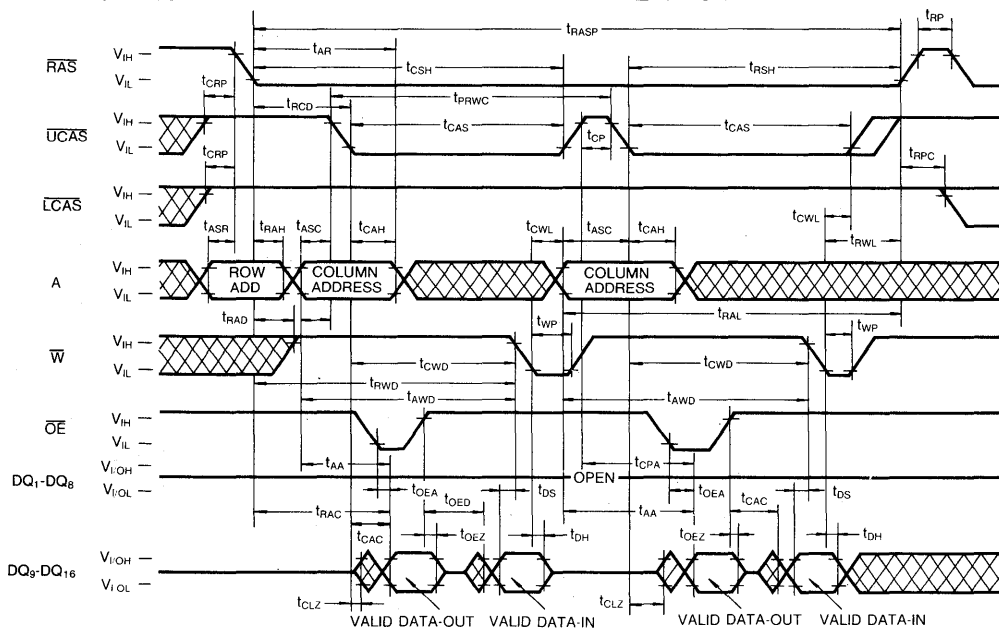
⊠ DON'T CARE

TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE

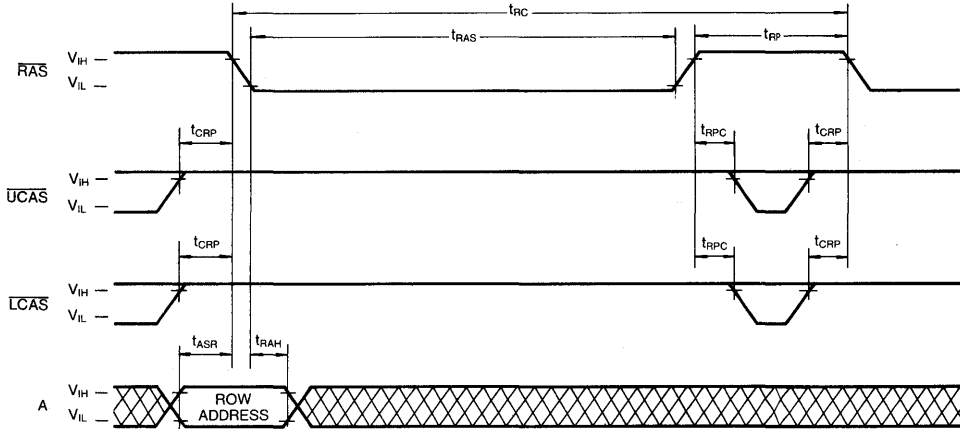


DON'T CARE

TIMING DIAGRAMS (Continued)

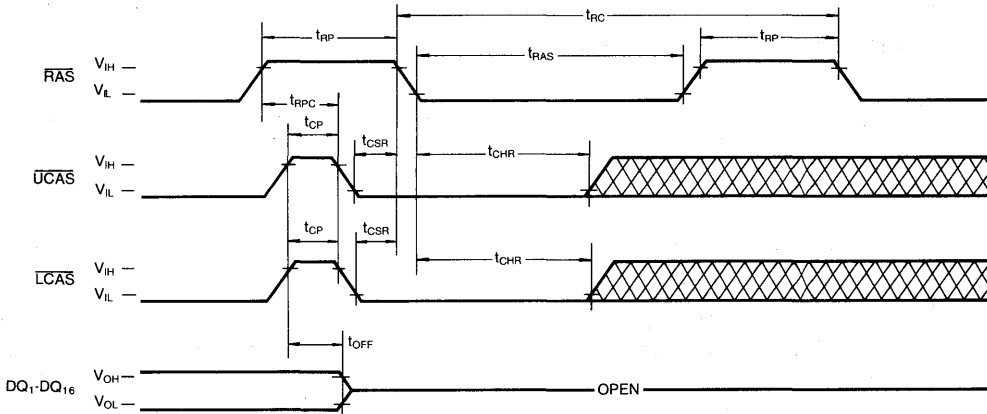
RAS ONLY REFRESH CYCLE

NOTE: \bar{W} , \bar{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

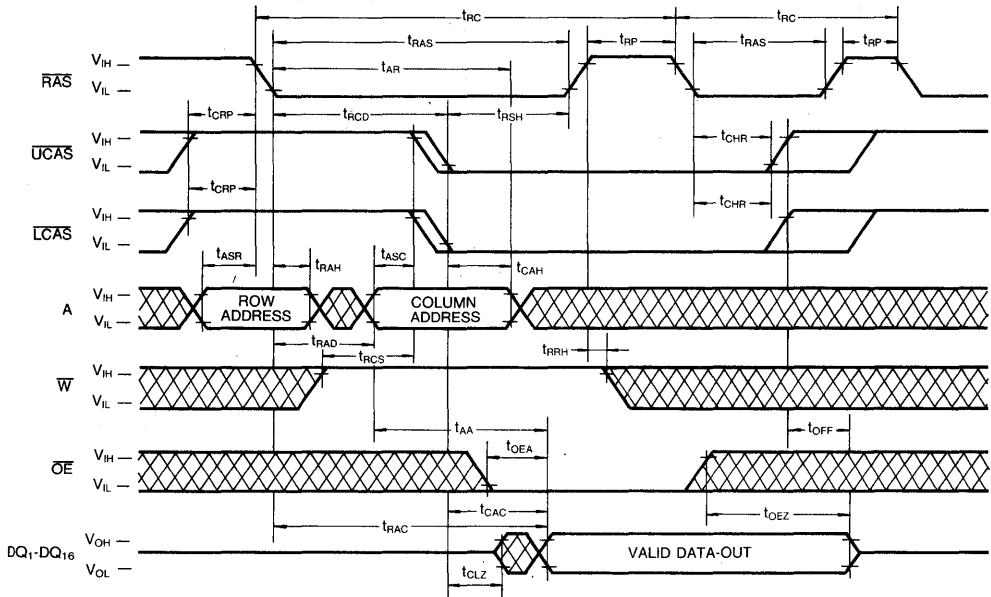
NOTE: $\bar{W}=V_{IH}$, \bar{OE} , A=Don't Care



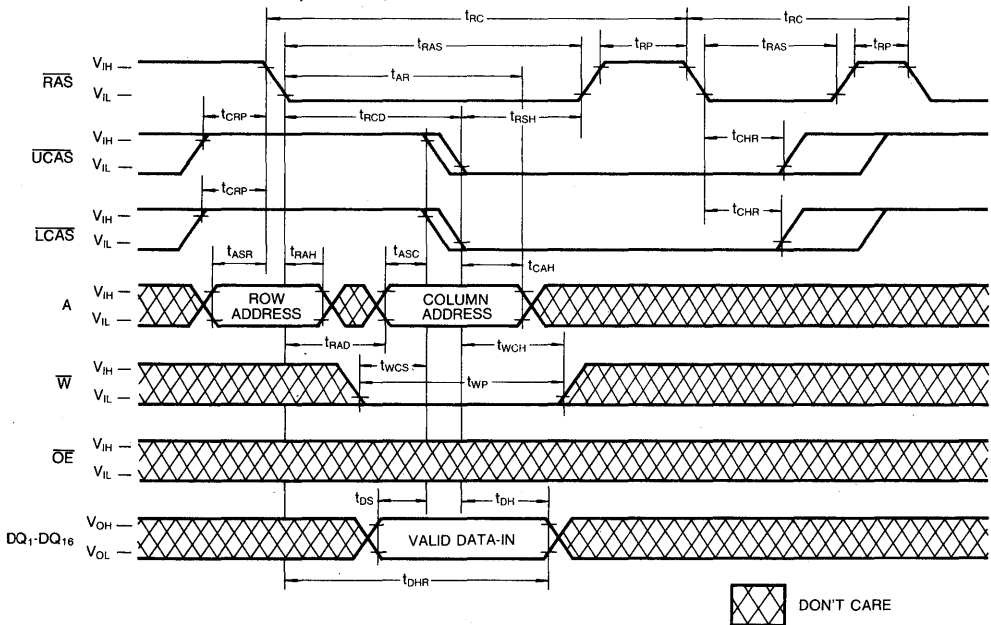
 DON'T CARE

TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)

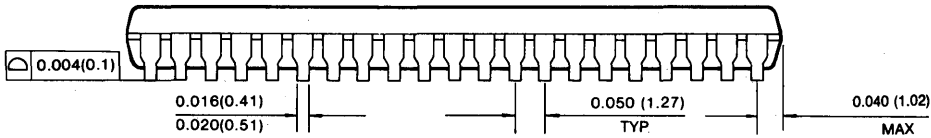
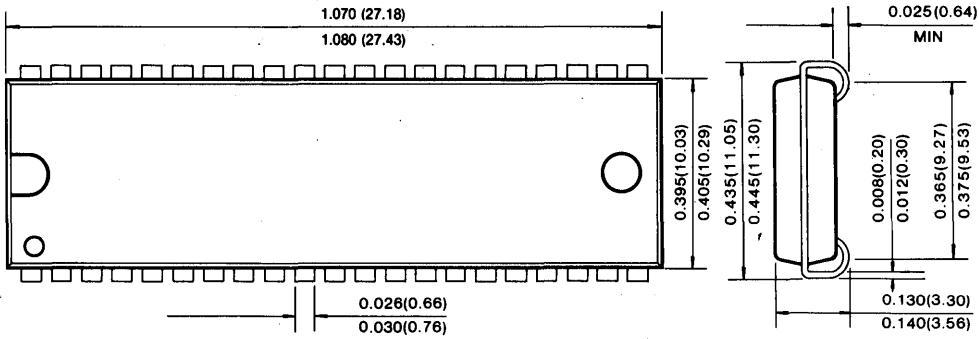


HIDDEN REFRESH CYCLE (WRITE)

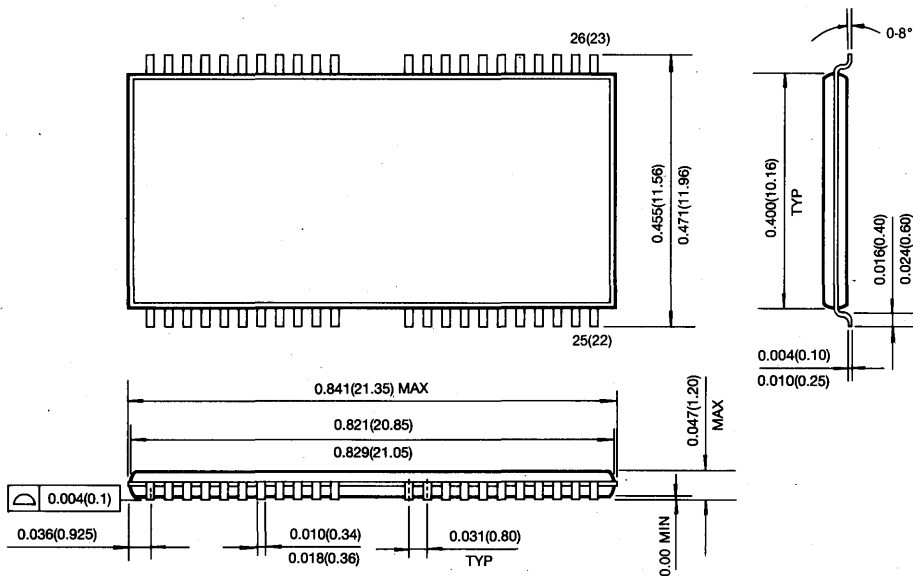


PACKAGE DIMENSION
42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trC	thPC
KM416V1004A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416V1004A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416V1004A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- Extended Data Out Mode (Fast Page Mode with Extended Data Out)
- 2 $\overline{\text{CAS}}$ Byte/Word Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Triple +3.3V \pm 0.3V power supply
- Refresh Cycle
 - 4096 cycle/64ms (Normal)
 - 4096 cycle/128ms (L-version)
 - 4096 cycle/128ms (F-version)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages

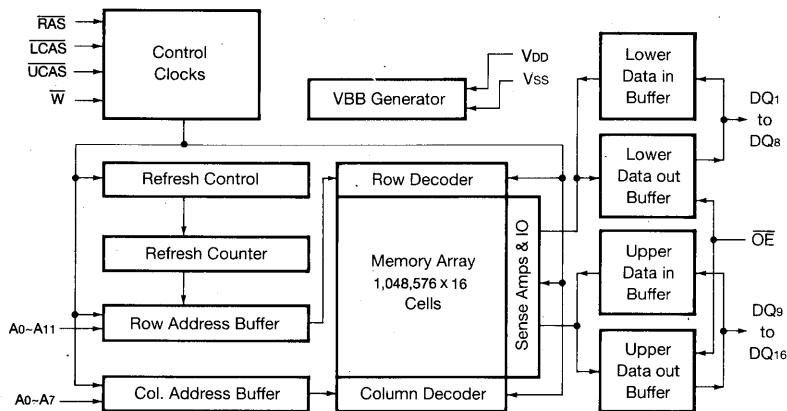
GENERAL DESCRIPTION

The Samsung KM416V1004A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

The KM416V1004A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

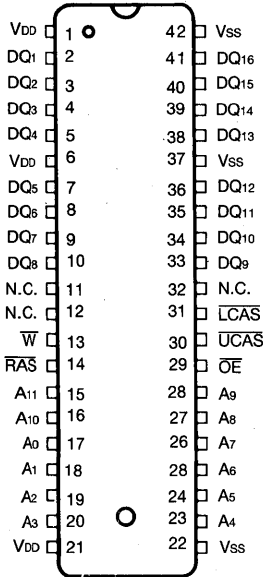
The KM416V1004A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



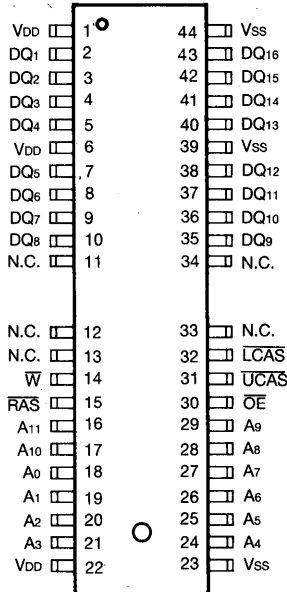
PIN CONFIGURATION (Top Views)

• KM416V1004AJ



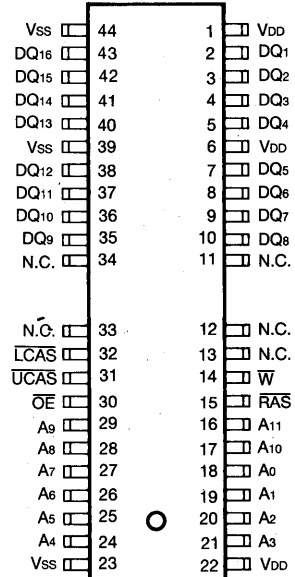
(SOJ)

• KM416V1004AT



(TSOP(II)-Forward)

• KM416V1004AR



(TSOP(II)-Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
RAS	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5 to 4.6	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC1}	-	90 80 70 mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=V_{IH}$)	KM416V1004A KM416V1004AL KM416V1004ALL	I _{CC2}	-	2 1 1 mA mA mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\overline{\text{UCAS}}=\overline{\text{LCAS}}=V_{IH}$, $\overline{\text{RAS}}$, Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC3}	-	90 80 70 mA mA mA
EDO Mode Current* ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC4}	-	110 100 90 mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=V_{DD}-0.2V$)	KM416V1004A KM416V1004AL KM416V1004ALL	I _{CC5}	-	1 300 200 mA μ A μ A
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ Cycling @trc=min.)	KM416V1004A-6/A-L6/A-F6 KM416V1004A-7/A-L7/A-F7 KM416V1004A-8/A-L8/A-F8	I _{CC6}	-	90 80 70 mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V, Input Low Voltage(V _{IL})=0.2V $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}=0.2V$ DIN=Don't Care, trc=31.25 μ s (L-Version) t _{RAS} =t _{TRAS} min~300ns	KM416V1004A-L	I _{CC7}	-	450 μ A

6

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A11=VDD-0.2V or 0.2V DQ1-DQ16=VDD-0.2V or 0.2V or Open	Iccs	-	250	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test=0 V)	I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =2mA)	V _{OL}	-	0.4	V

*NOTE: Icc1, Icc3, Icc4 and Icc6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current. In Icc1 and Icc3, address can be changed maximum once while RAS=VIL. In Icc4, Address can be changed maximum once while one Hyper page mode cycle time tHPC.

CAPACITANCE (TA=25°C, VDD=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-11)	CIN1	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	CIN2	-	7	pF
Output Capacitance (DQ1-DQ16)	CDO	-	7	pF

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, VDD=3.3V ± 0.3V, See notes 1,2)

(Test condition : VIH/VIL=2.1V/0.8V, VOH/VOL=2.0V/0.8V, Output Loading CL=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		150		ns	
Read-modify-write cycle time	tRWC	155		185		205		ns	
Access time from RAS	tRAC		60		70		80	ns	3,4,11
Access time from CAS	tCAC		17		20		20	ns	3,4,5
Access time from column address	tAA		30		35		40	ns	3,11
CAS to output in Low-Z	tCLZ	3		3		3		ns	3
OE to output in Low-Z	tOLZ	3		3		3		ns	3
Output buffer turn-off delay from CAS	tCEZ	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	tT	2	50	2	50	2	50	ns	2
RAS precharge time	tRP	40		50		60		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	tRSH	17		20		20		ns	
CAS hold time	tCSH	50		60		70		ns	
CAS pulse width	tCAS	10	10,000	15	10,000	20	10,000	ns	
RAS to CAS delay time	tRCD	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
\overline{RAS} to column address delay time	tRAD	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to \overline{RAS}	tAR	45		55		60		ns	6
Column address to \overline{RAS} lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		0		ns	9
Read command hold time referenced to \overline{RAS}	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to \overline{RAS}	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to \overline{RAS} lead time	tRWL	15		15		20		ns	
Write command to \overline{CAS} lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to \overline{RAS}	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
\overline{CAS} to \overline{W} delay time	tCWD	40		50		50		ns	8,17
\overline{RAS} to \overline{W} delay time	tRWD	85		95		105		ns	8
Column address to \overline{W} delay time	tAWD	55		60		65		ns	8
\overline{CAS} precharge to \overline{W} delay time	tCPWD	60		65		70		ns	
\overline{CAS} set-up time (\overline{CAS} -before- \overline{RAS} refresh)	tCSR	10		10		10		ns	19
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh)	tCHR	10		10		10		ns	20
\overline{RAS} precharge to \overline{CAS} hold time	tRPC	5		5		5		ns	
\overline{CAS} precharge time (\overline{C} -B- \overline{R} counter test cycle)	tCPT	20		25		30		ns	
\overline{RAS} hold time referenced to \overline{OE}	tROH	15		20		20		ns	
\overline{OE} access time	tOEA		15		20		20	ns	
\overline{OE} to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from \overline{OE}	tOEZ	3	15	3	20	3	20	ns	7
\overline{OE} command hold time	tOEH	15		20		20		ns	
Access time from \overline{CAS} precharge	tCPA		35		40		45	ns	3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
$\overline{\text{CAS}}$ precharge time (Hyper page mode)	tCP	10		10		10		ns	16
$\overline{\text{RAS}}$ pulse width (Hyper Page mode)	tRASP	60		70		80		ns	
$\overline{\text{RAS}}$ hold time from CAS precharge	tRHCP	35		40		45		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from $\overline{\text{RAS}}$	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from $\overline{\text{W}}$	tWEZ	3	15	3	20	3	20	ns	7
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	tOCH	5		5		5		ns	
$\overline{\text{CAS}}$ hold time to $\overline{\text{OE}}$	tCHO	5		5		5		ns	
$\overline{\text{OE}}$ precharge time	tOEP	5		5		5		ns	
$\overline{\text{W}}$ pulse width	tWPE	5		5		5		ns	
$\overline{\text{W}}$ to data delay	tWED	15		20		20		ns	
$\overline{\text{RAS}}$ pulse width (F-ver)	tRASS	100		100		100		μs	13
$\overline{\text{RAS}}$ precharge time (F-ver)	tRPS	110		130		150		ns	13
$\overline{\text{CAS}}$ hold time (F-ver)	tCHS	-50		-50		-50		ns	13

KM416V1004A/A-L/A-F Truth Table

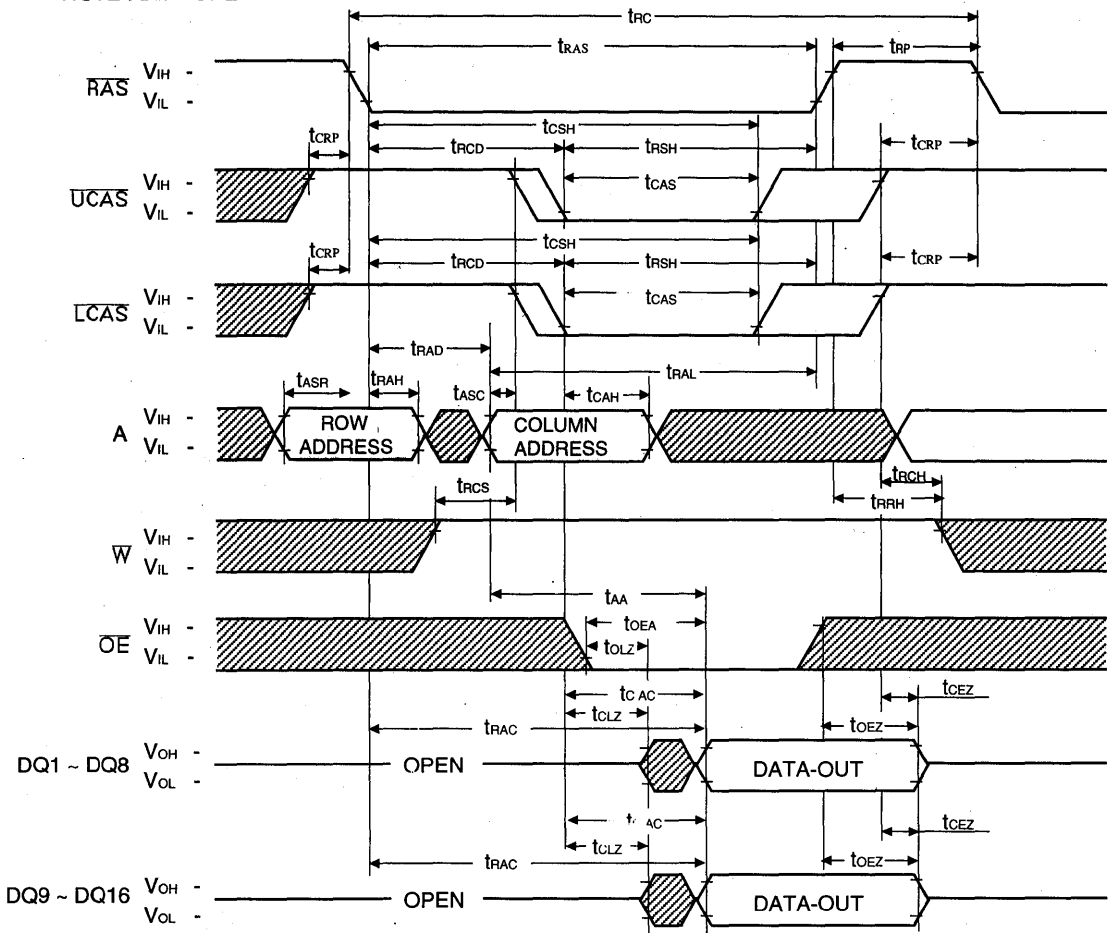
RAS	LCAS	UCAS	$\overline{\text{W}}$	$\overline{\text{OE}}$	DQ ₁ ~DQ ₈	DQ ₉ ~DQ ₁₆	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	X	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL Loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. $t_{ASC} \geq t_{CP} \min$, Assume $t_r=2.0ns$.
13. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
15. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
16. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
17. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
19. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
20. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.
21. t_{DS} , t_{DH} is independetly specified for lower byte $D_{in}(1-8)$, upper byte $D_{in}(9-16)$

TIMING DIAGRAM
WORD READ CYCLE

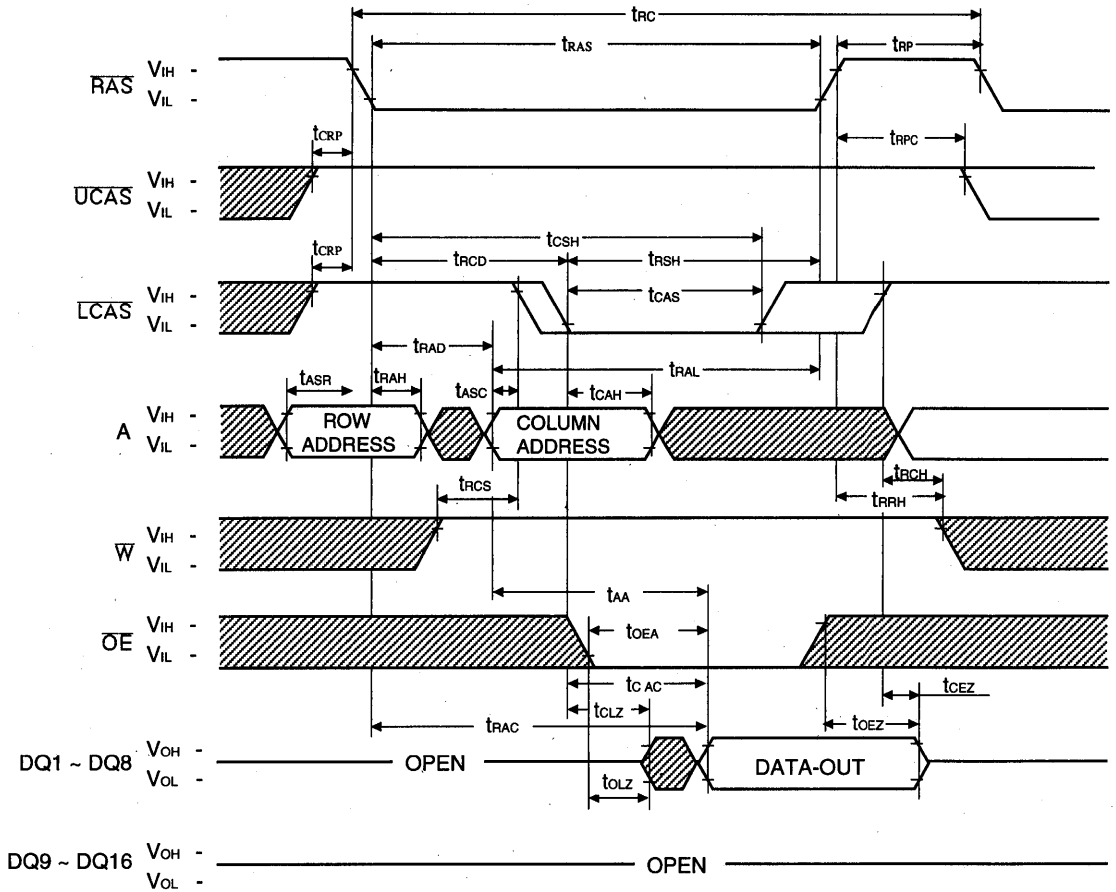
NOTE : $D_{IN} = OPEN$



 Don't Care

TIMING DIAGRAM
LOWER BYTE READ CYCLE

NOTE : $D_{IN} = OPEN$

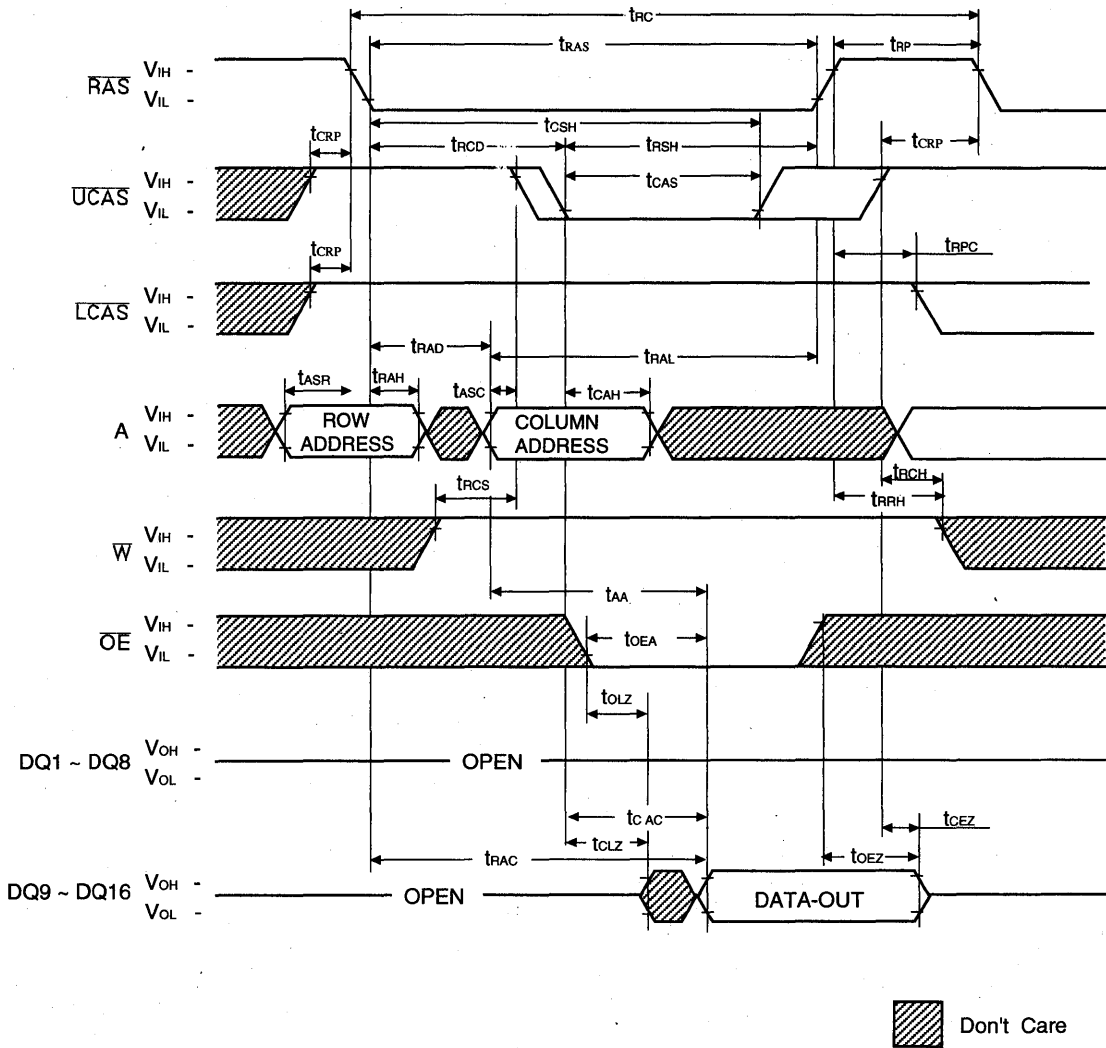


 Don't Care

6

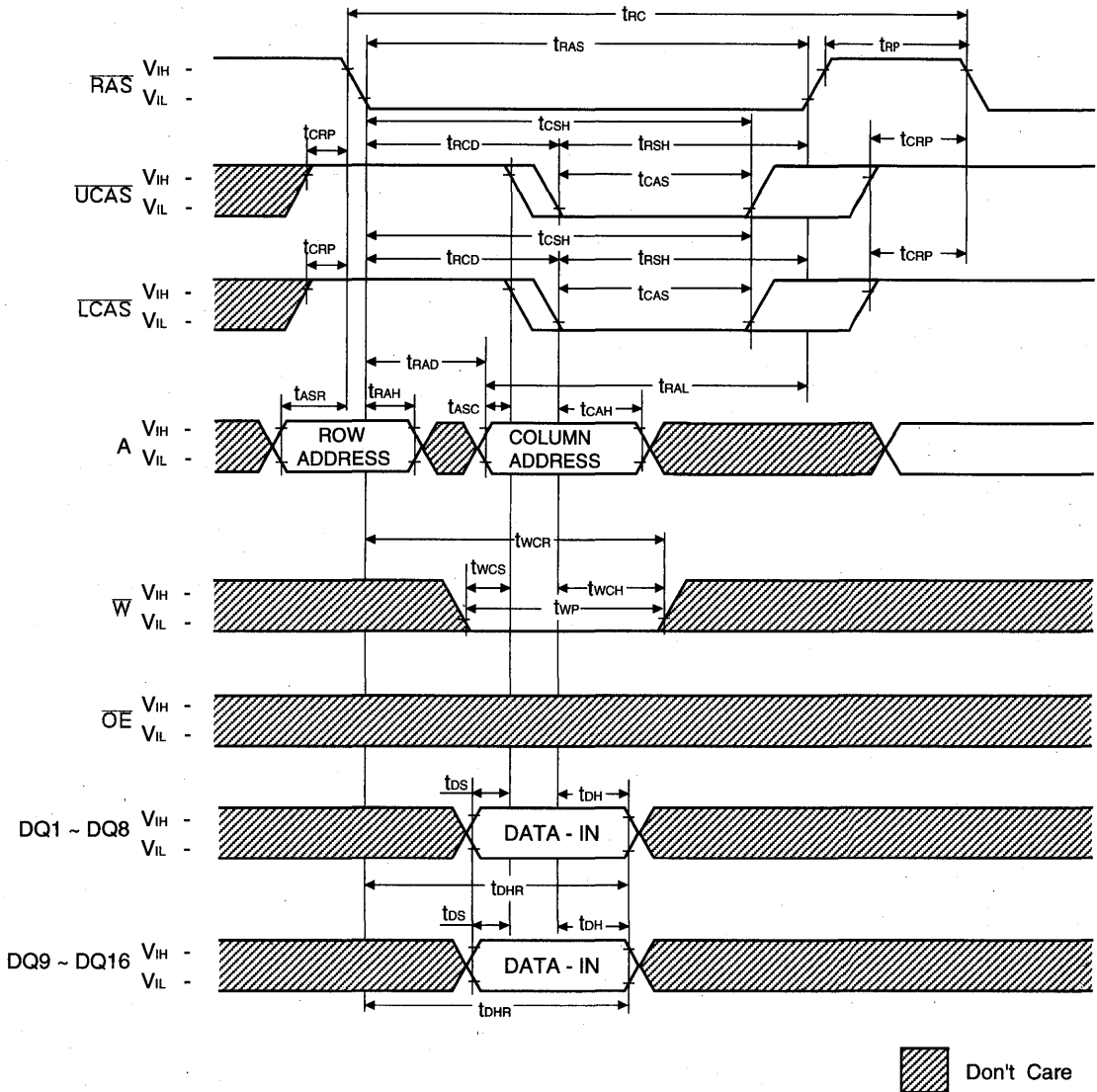
TIMING DIAGRAM
UPPER BYTE READ CYCLE

NOTE : D_{IN} = OPEN



WORD WRITE CYCLE (EARLY WRITE)

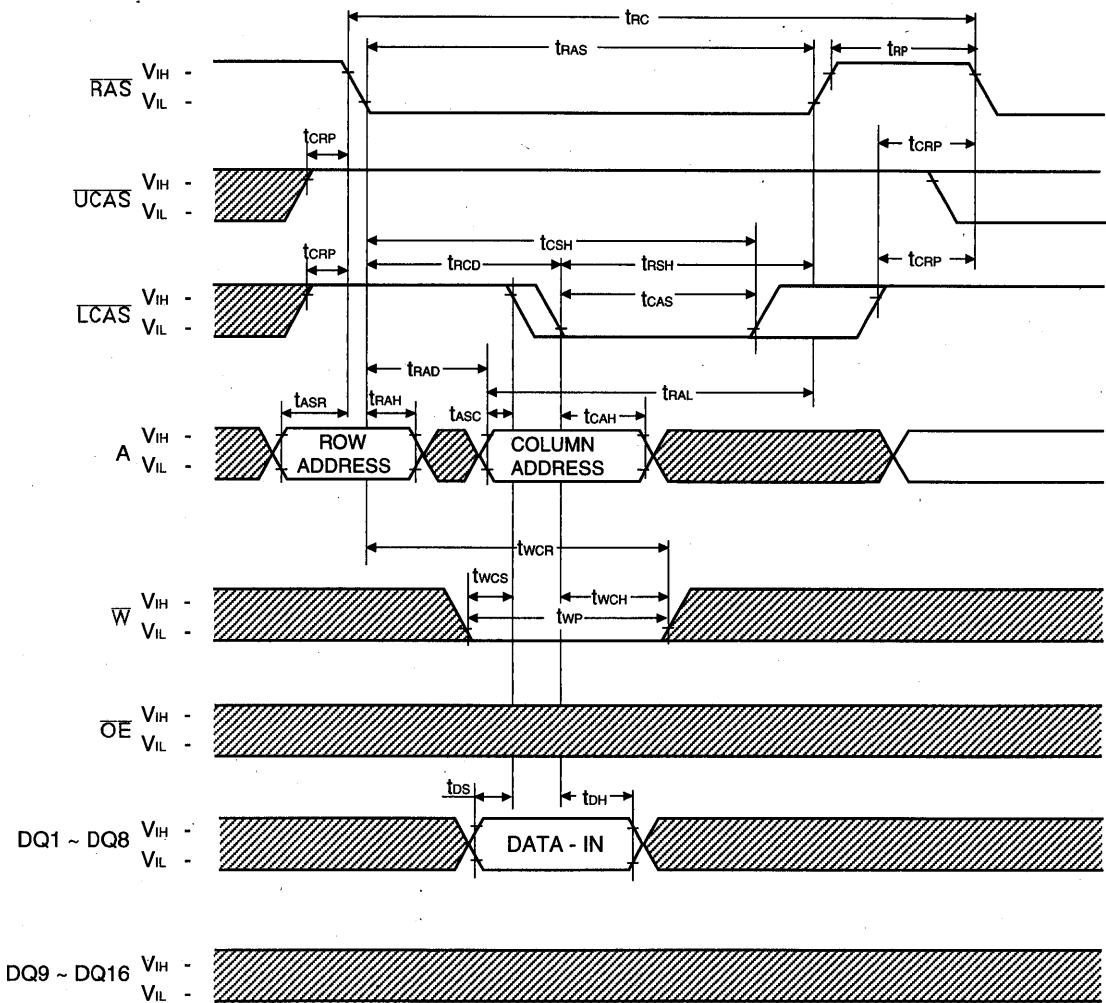
NOTE : D_{OUT} = OPEN



6

LOWER BYTE WRITE CYCLE (EARLY WRITE)

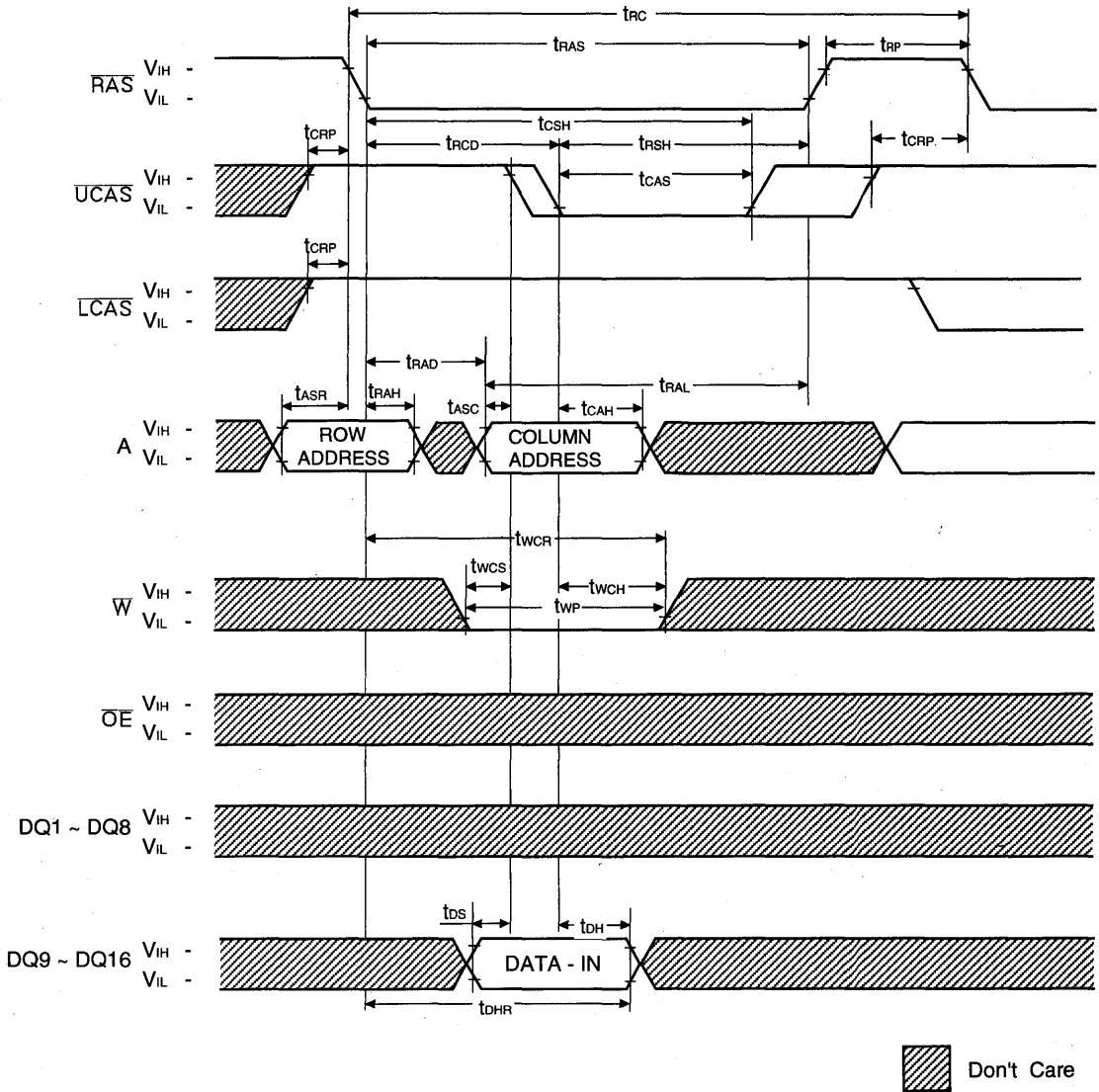
NOTE : D_{OUT} = OPEN



 Don't Care

UPPER BYTE WRITE CYCLE (EARLY WRITE)

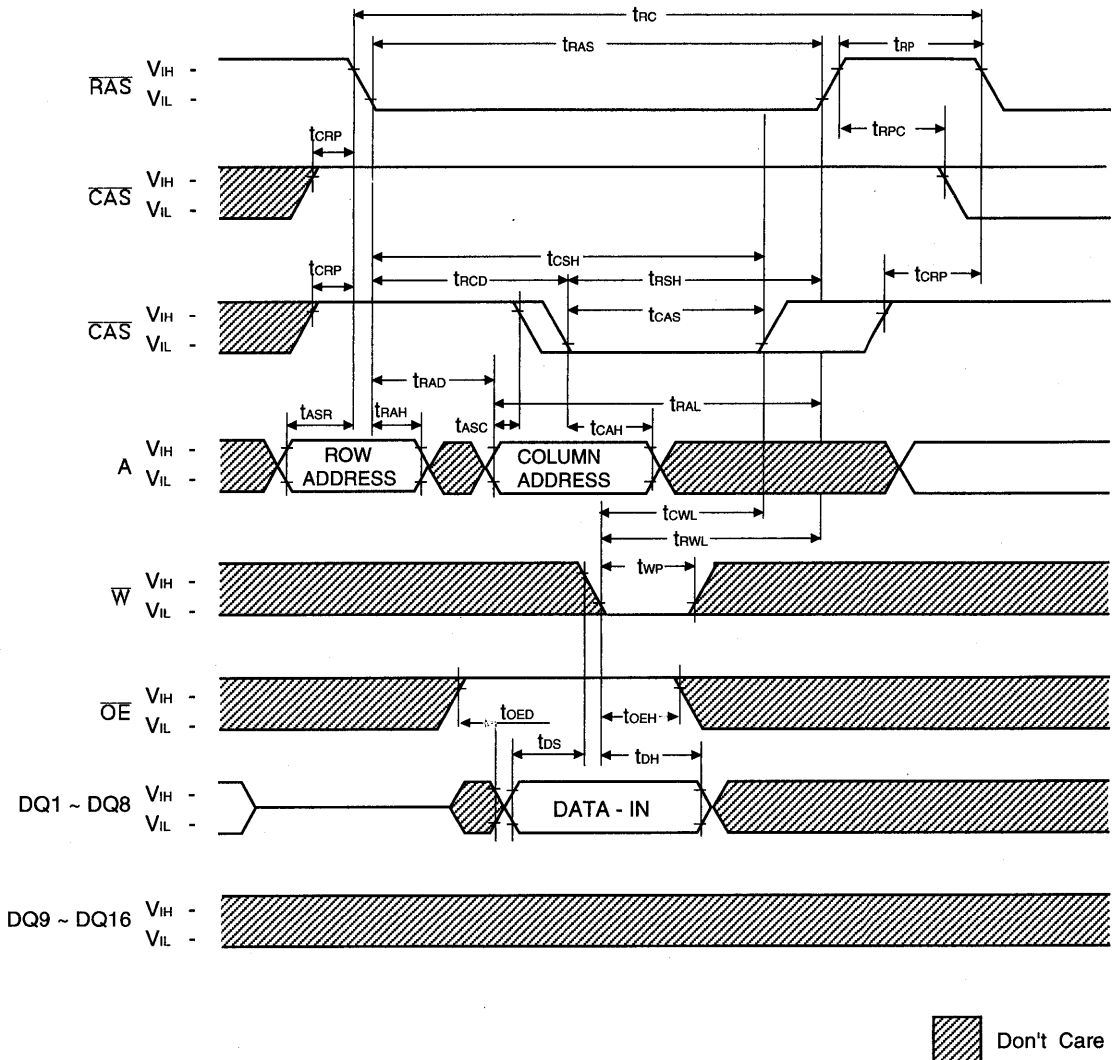
NOTE : DOUT = OPEN



6

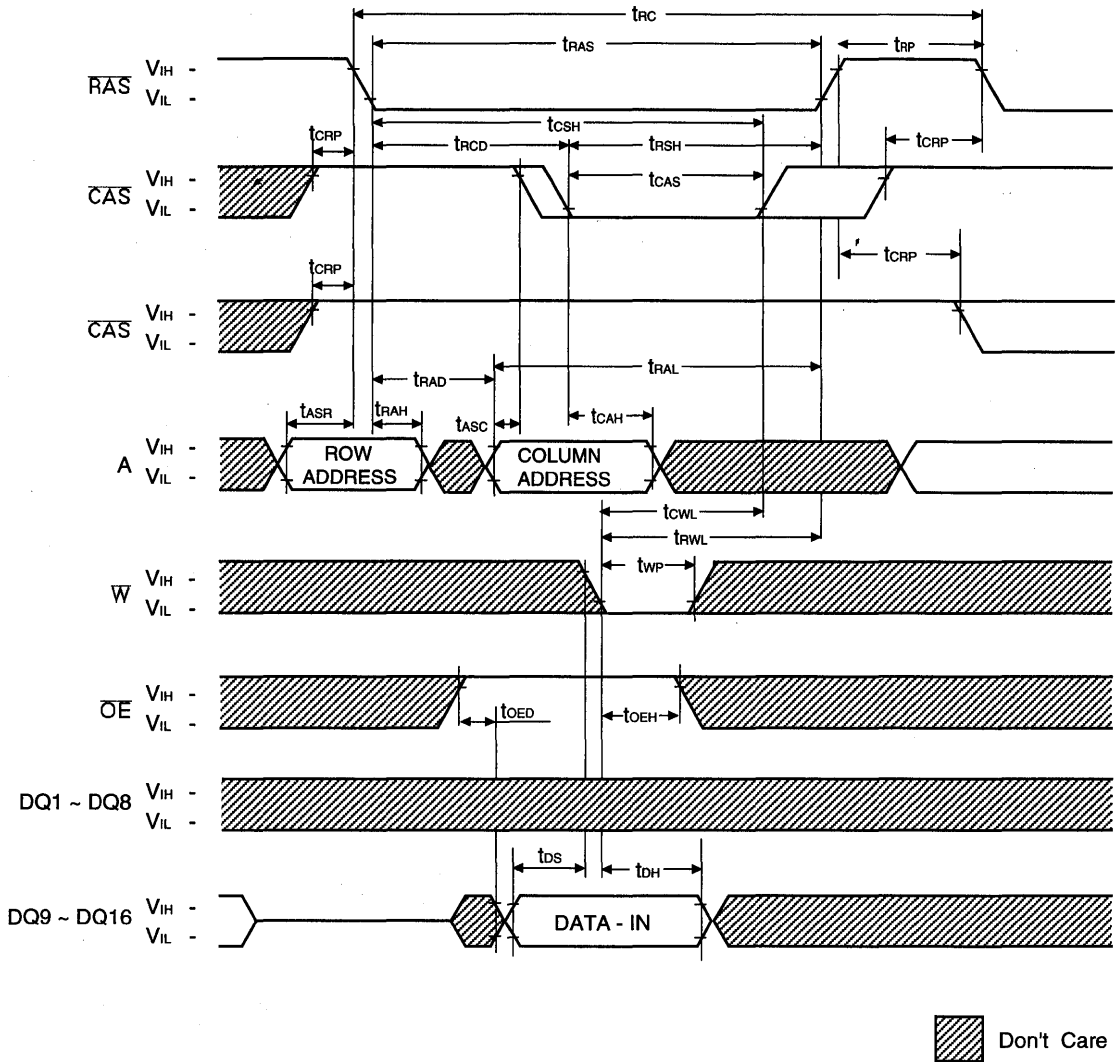
LOWER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : DOUT = OPEN

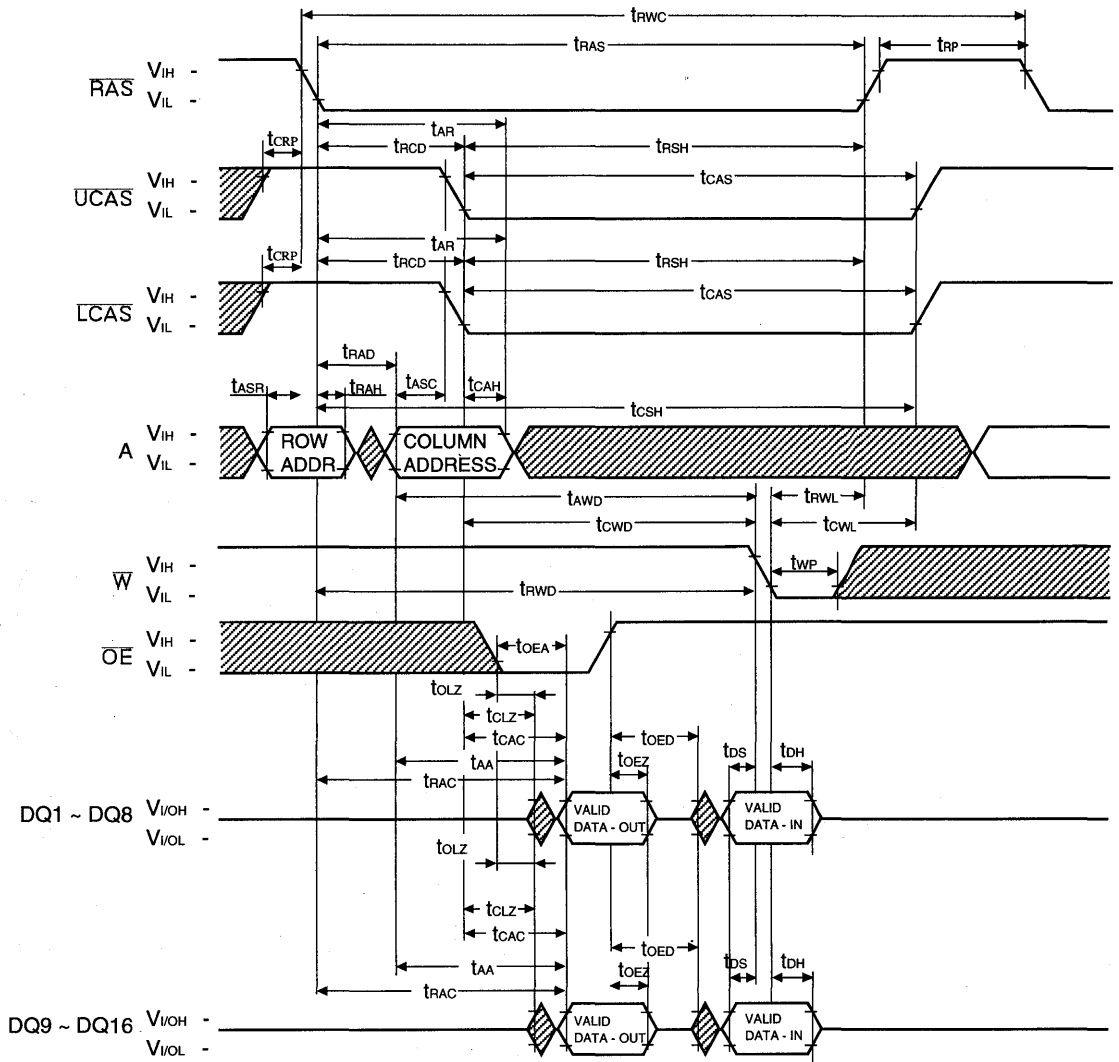


UPPER BYTE WRITE CYCLE (OE CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN



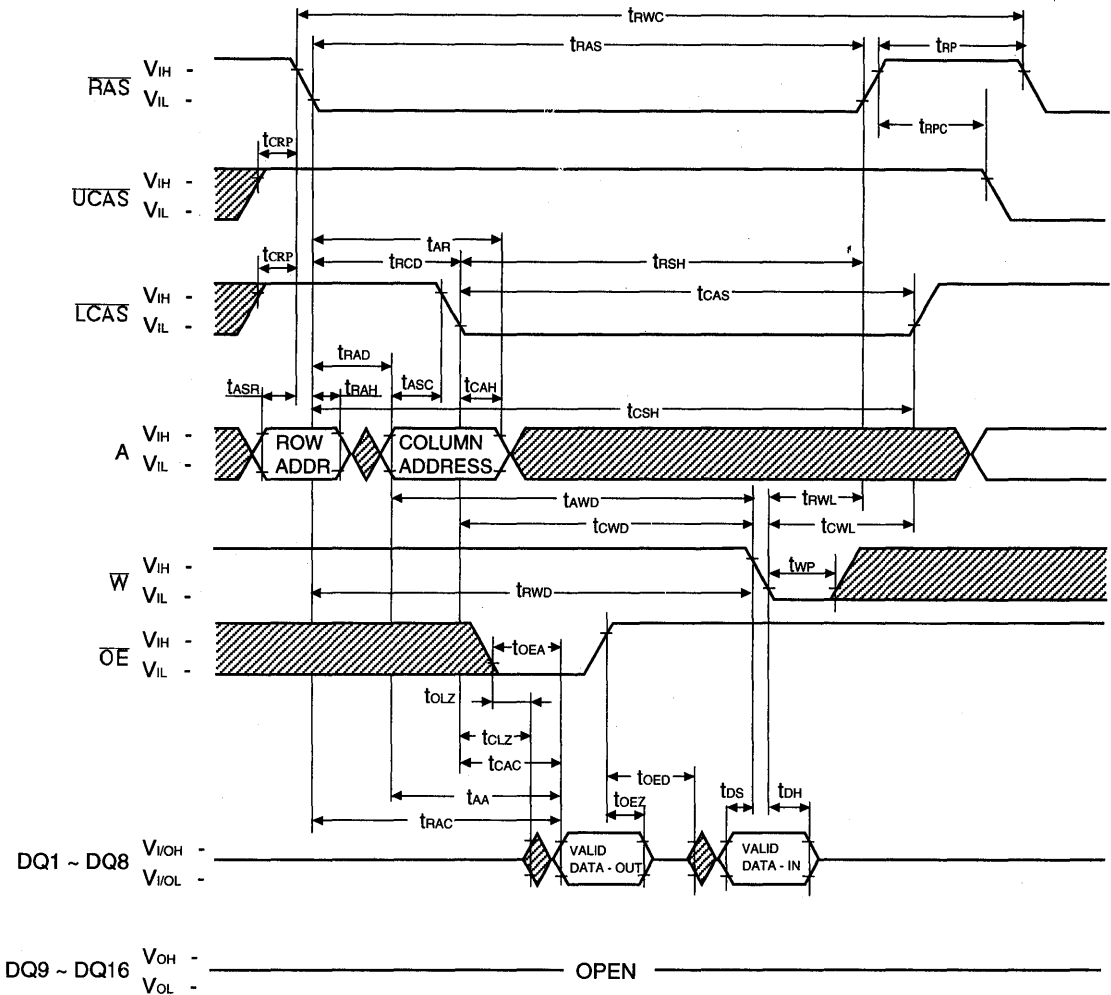
WORD READ - MODIFY - WRITE CYCLE



 Don't Care

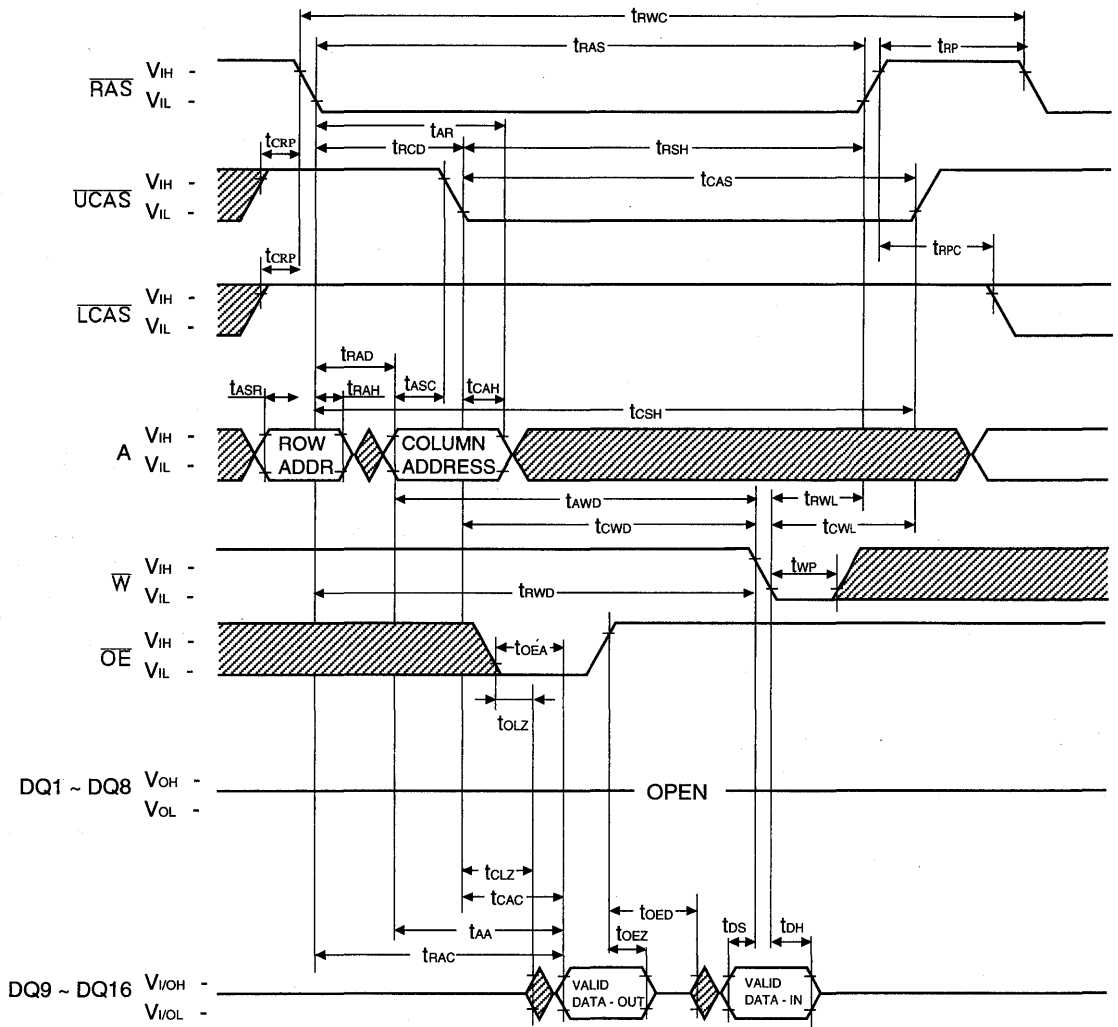
6

LOWER-BYTE READ - MODIFY - WRITE CYCLE



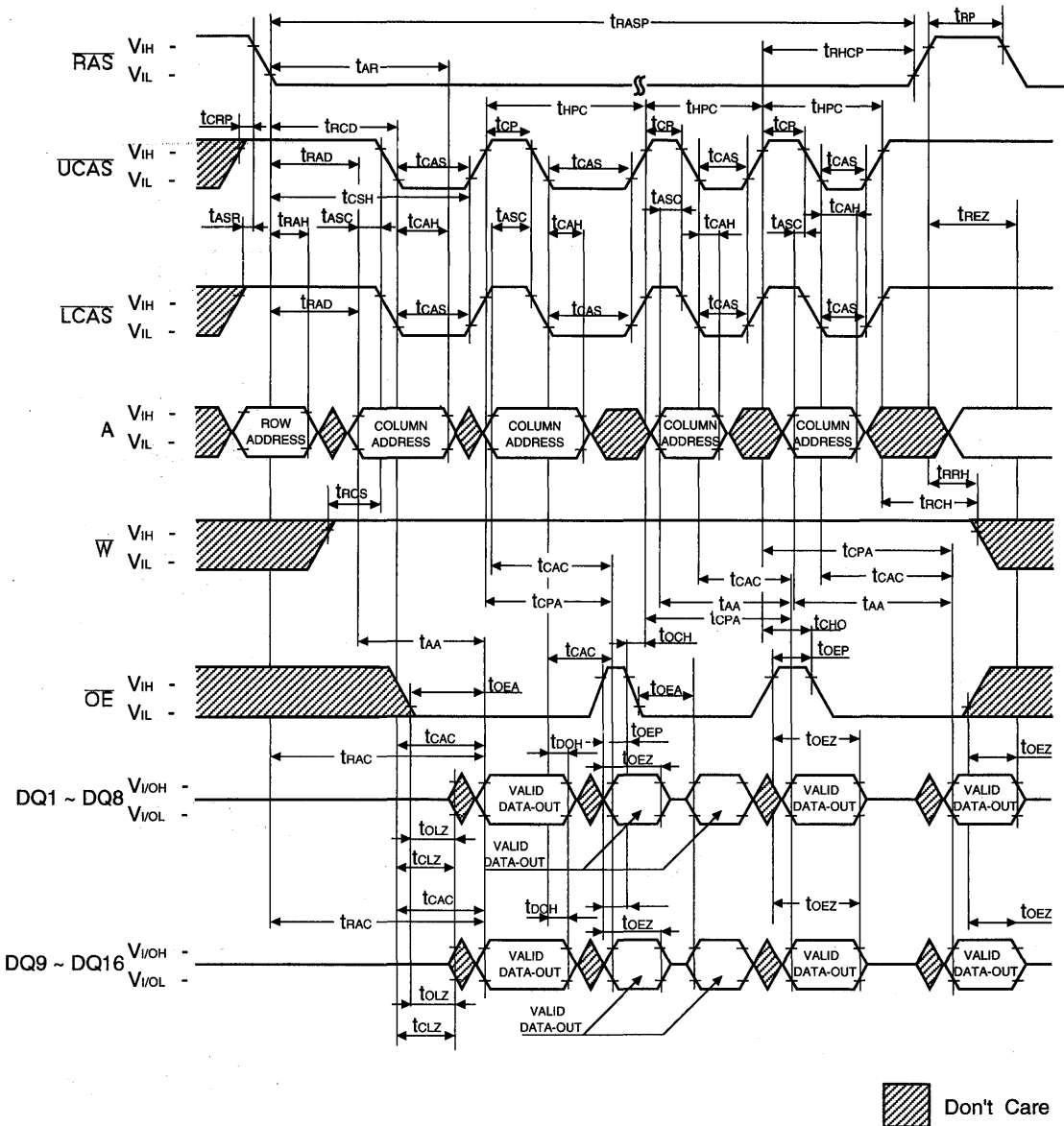
 Don't Care

UPPER-BYTE READ - MODIFY - WRITE CYCLE

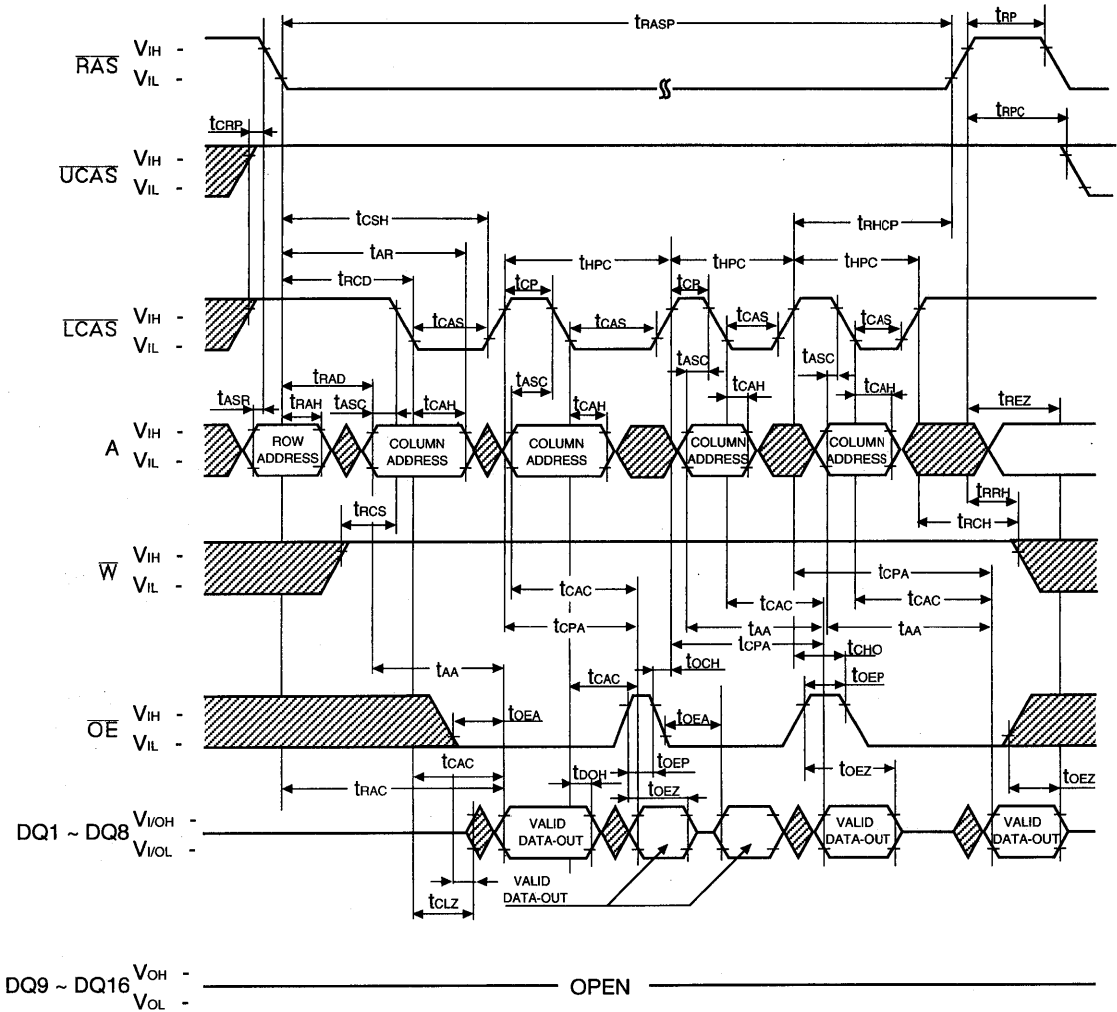


Don't Care

HYPER PAGE MODE WORD READ CYCLE

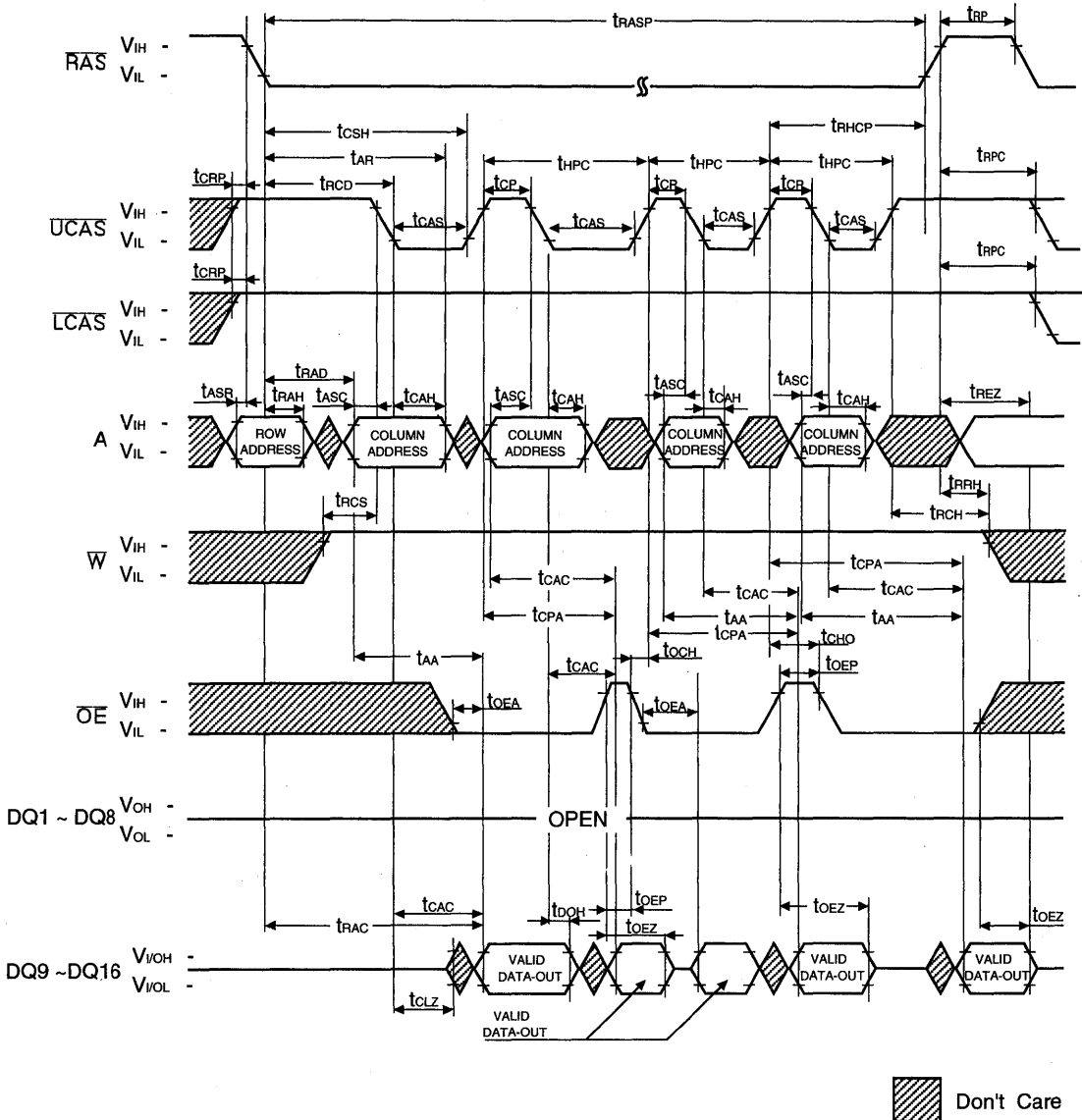


HYPER PAGE MODE LOWER BYTE READ CYCLE



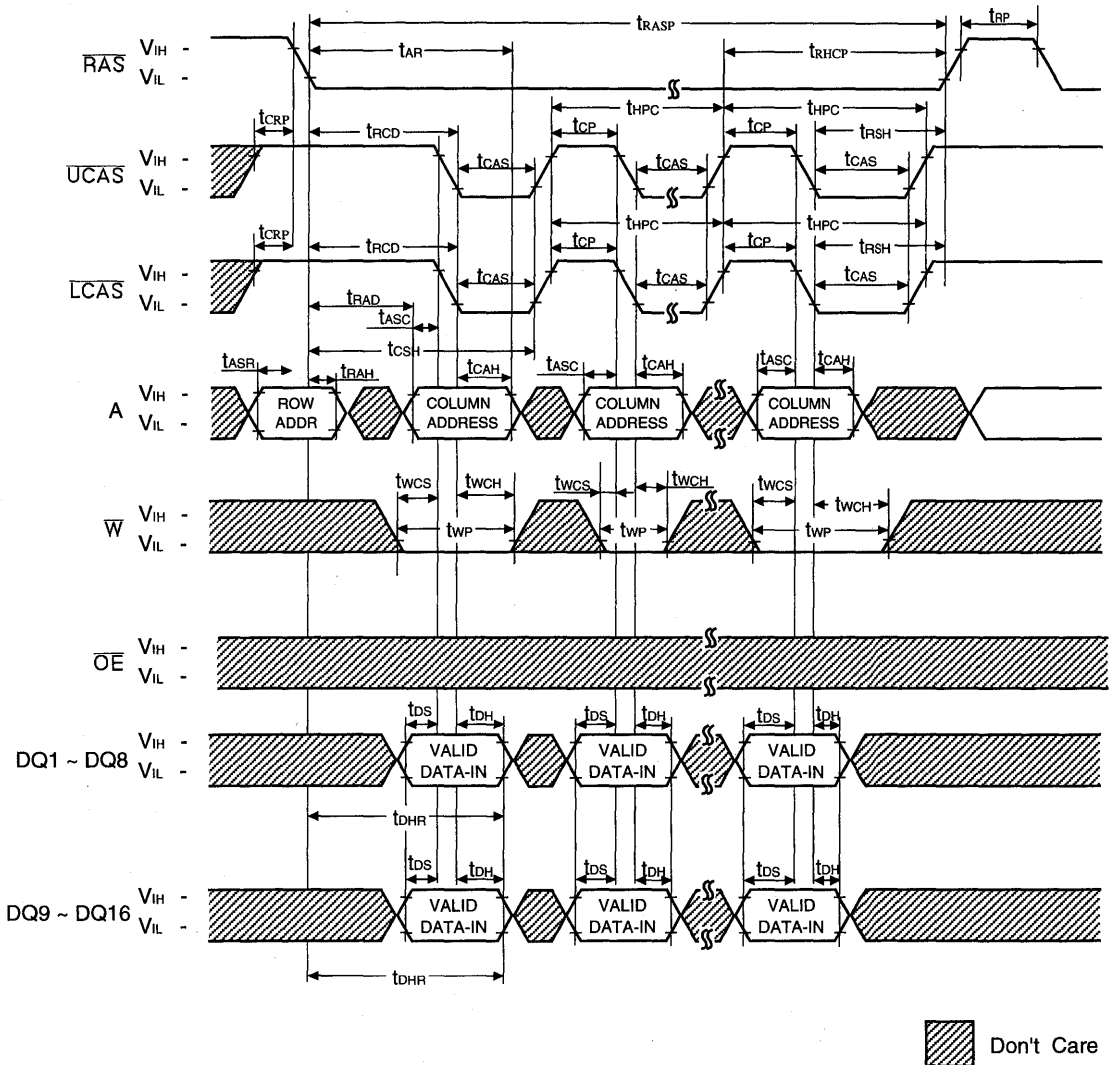
 Don't Care

HYPER PAGE MODE UPPER BYTE READ CYCLE



HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

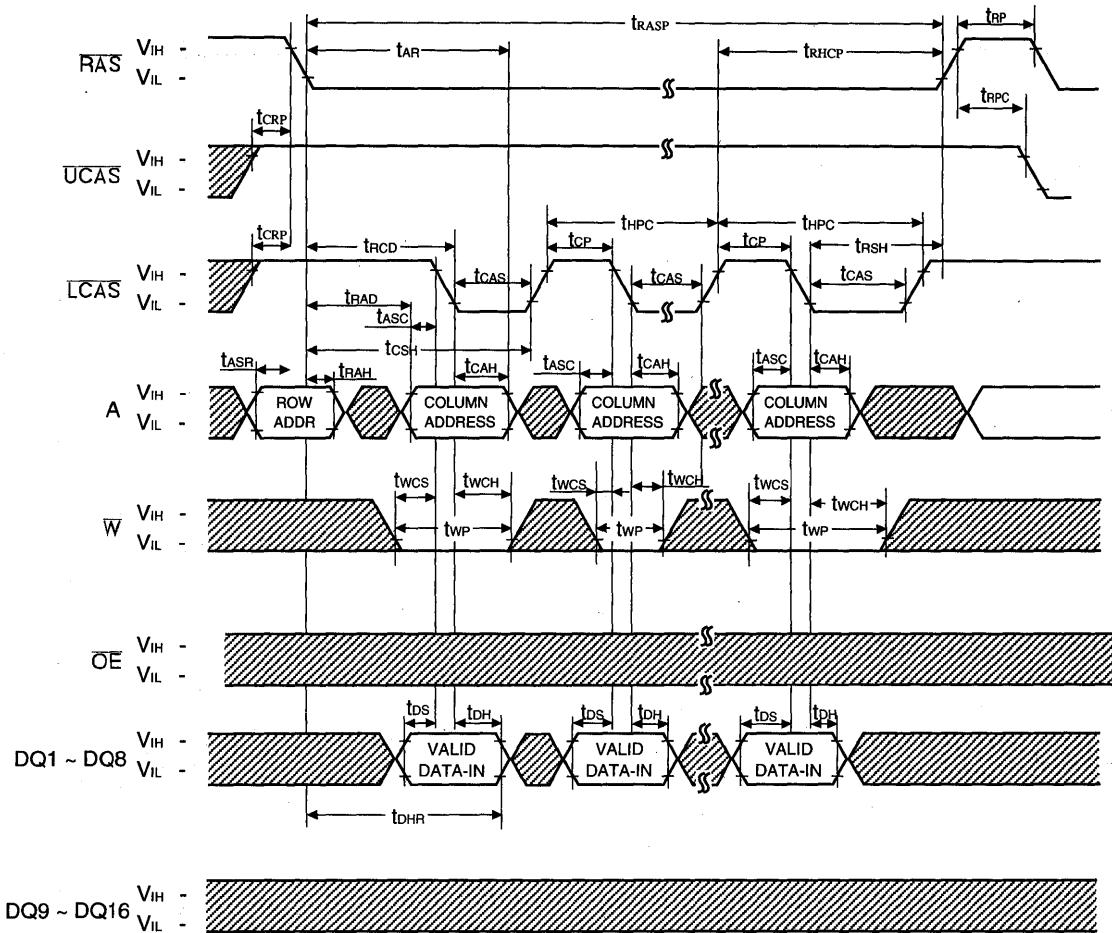
NOTE : DOUT = Open



6

HYPER PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)

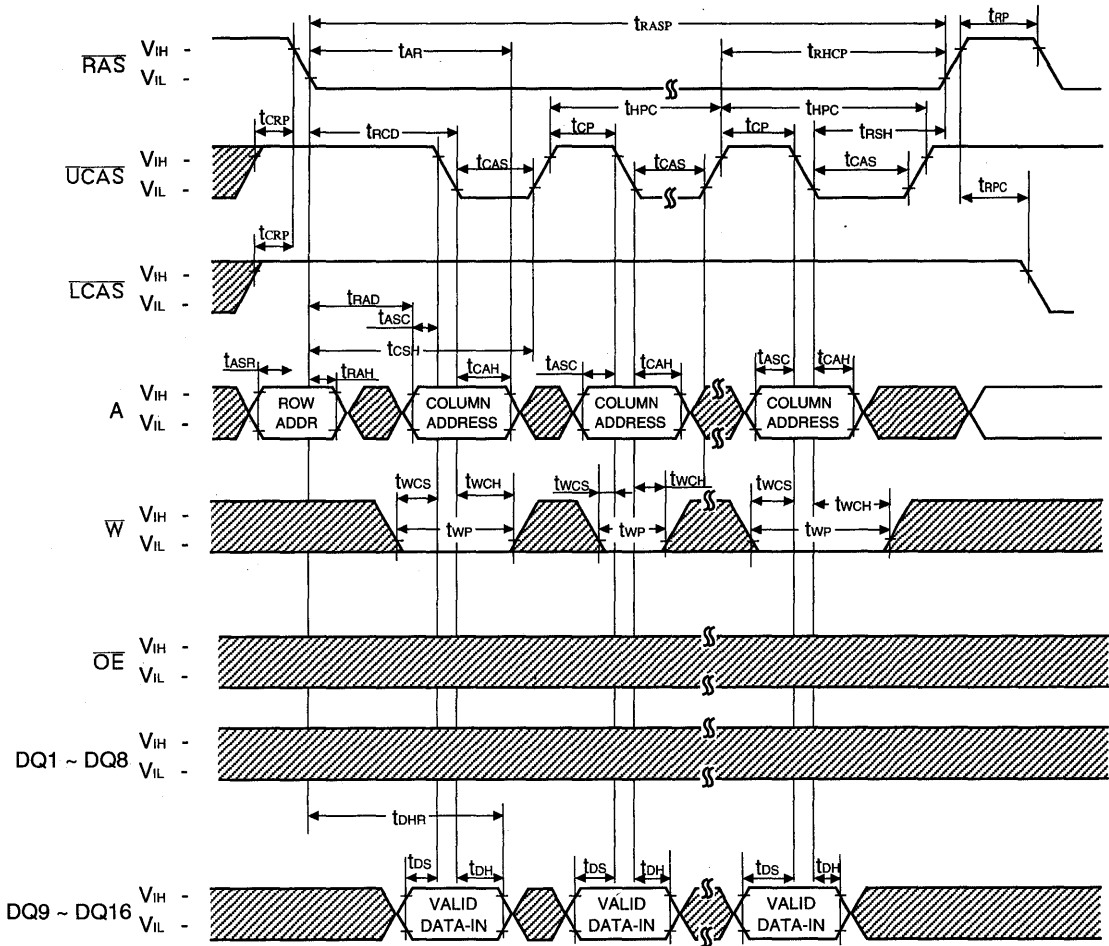
NOTE : D_{out} = Open



 Don't Care

HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

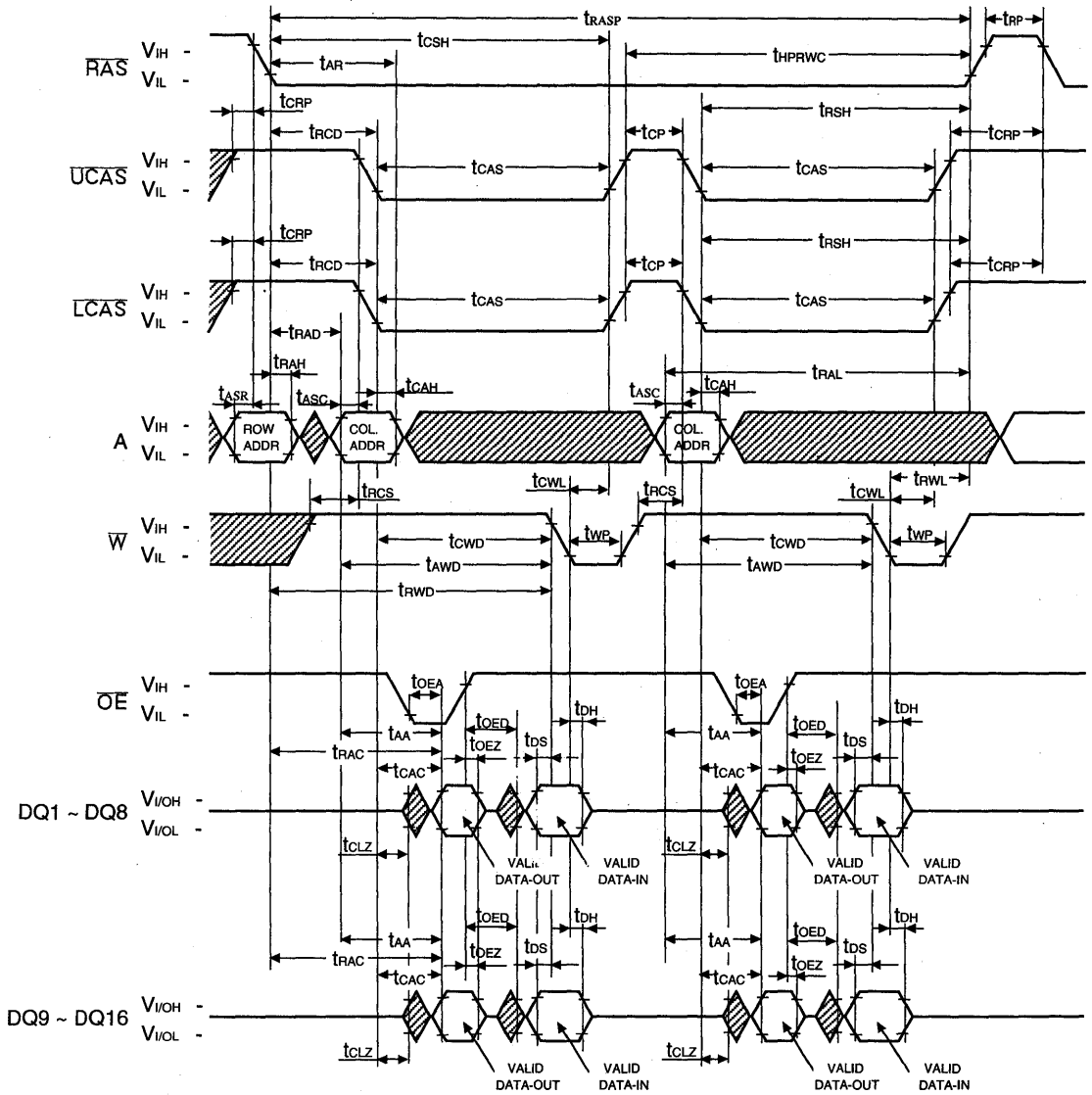
NOTE : DOUT = Open



 Don't Care

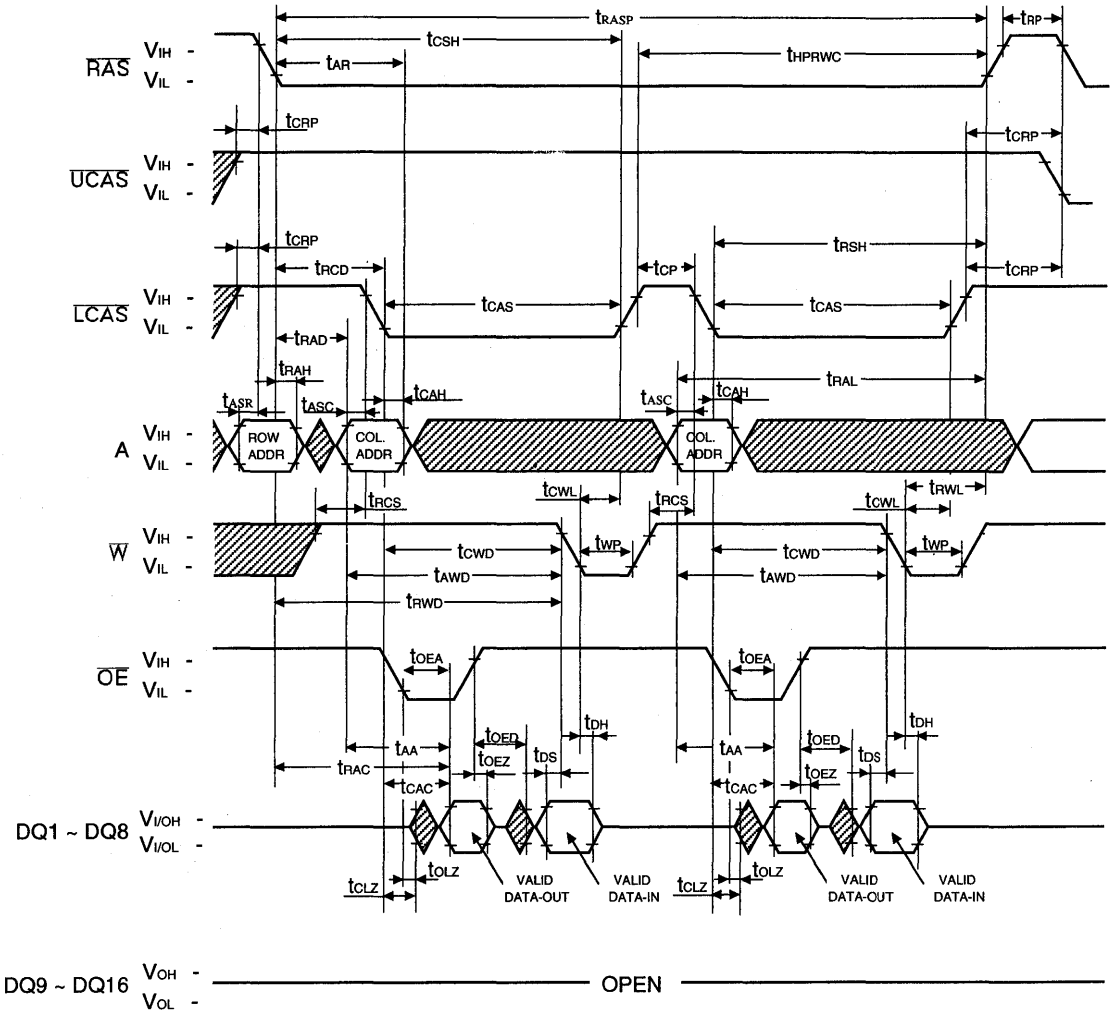
6

HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



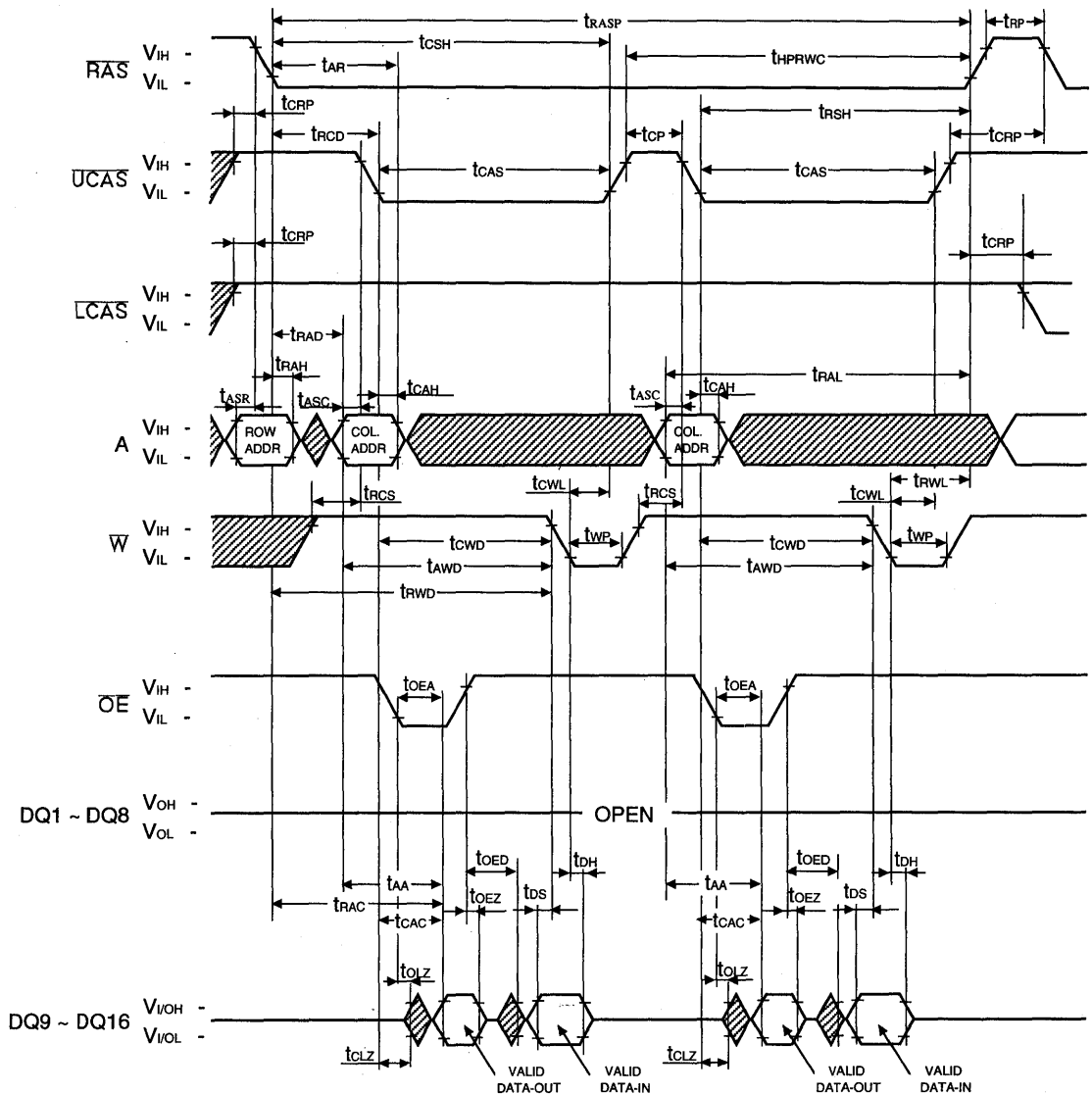
 Don't Care

HYPER PAGE MODE LOWER-BYTE-READ-MODIFY-WRITE CYCLE



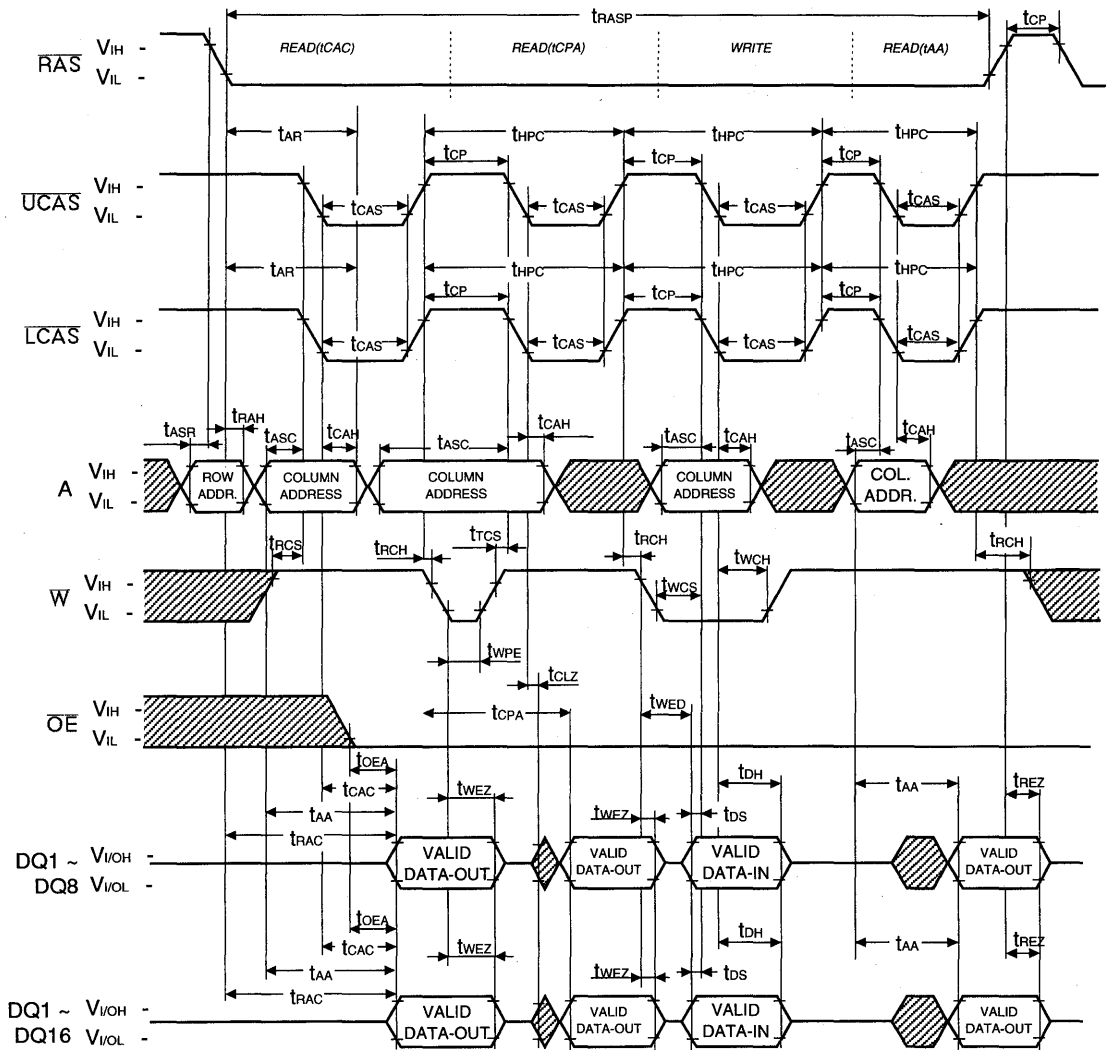
Don't Care

HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



 Don't Care

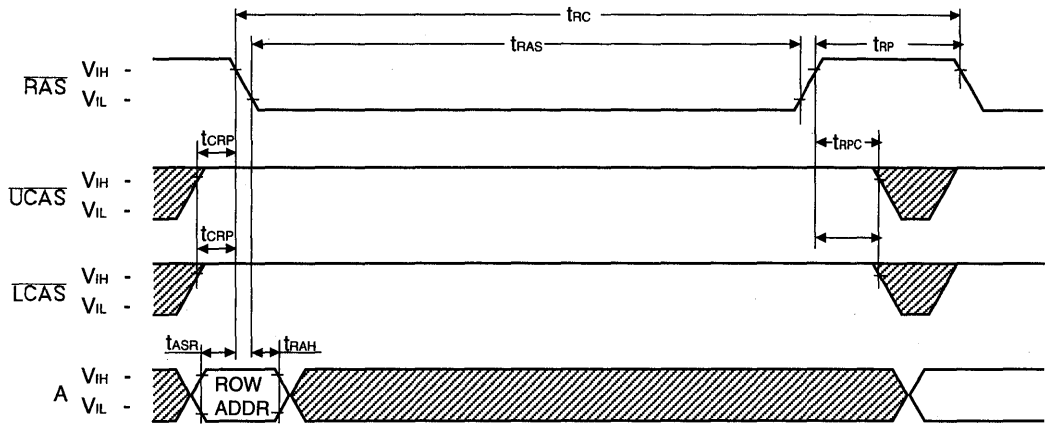
HYPER PAGE READ AND WRITE MIXED CYCLE



 Don't Care

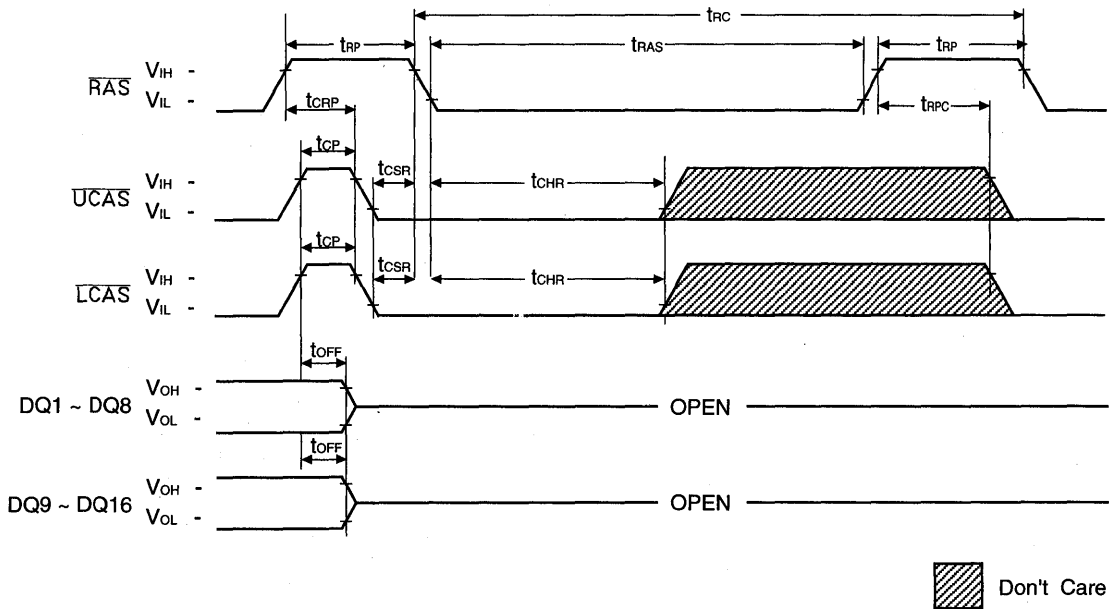
RAS-ONLY REFRESH CYCLE


NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



\bar{CAS} -BEFORE- \bar{RAS} REFRESH CYCLE

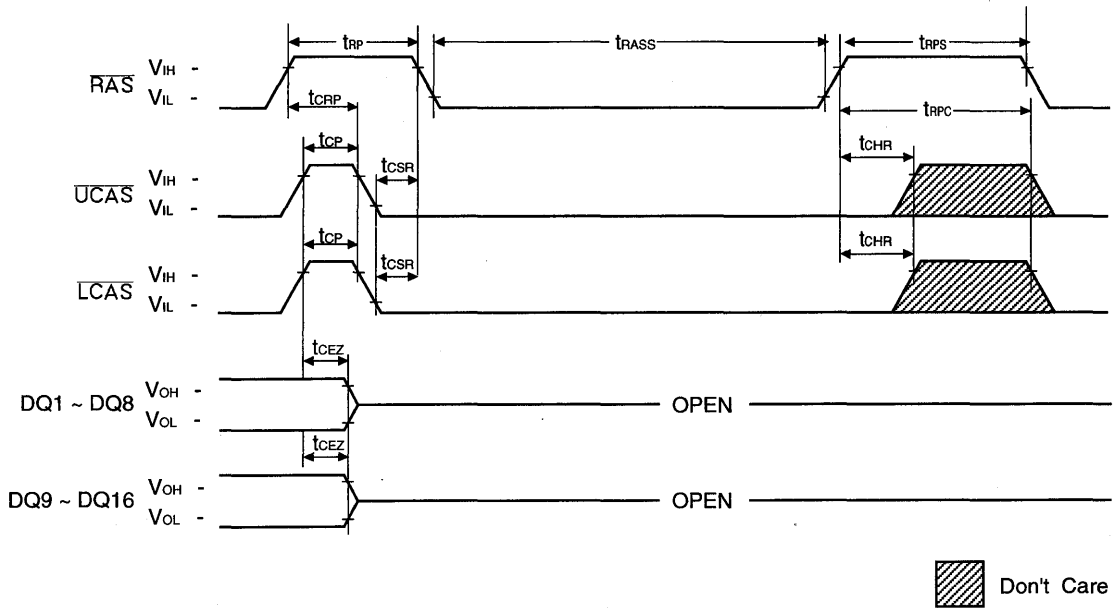
NOTE : \bar{W} , \bar{OE} , A = Don't Care



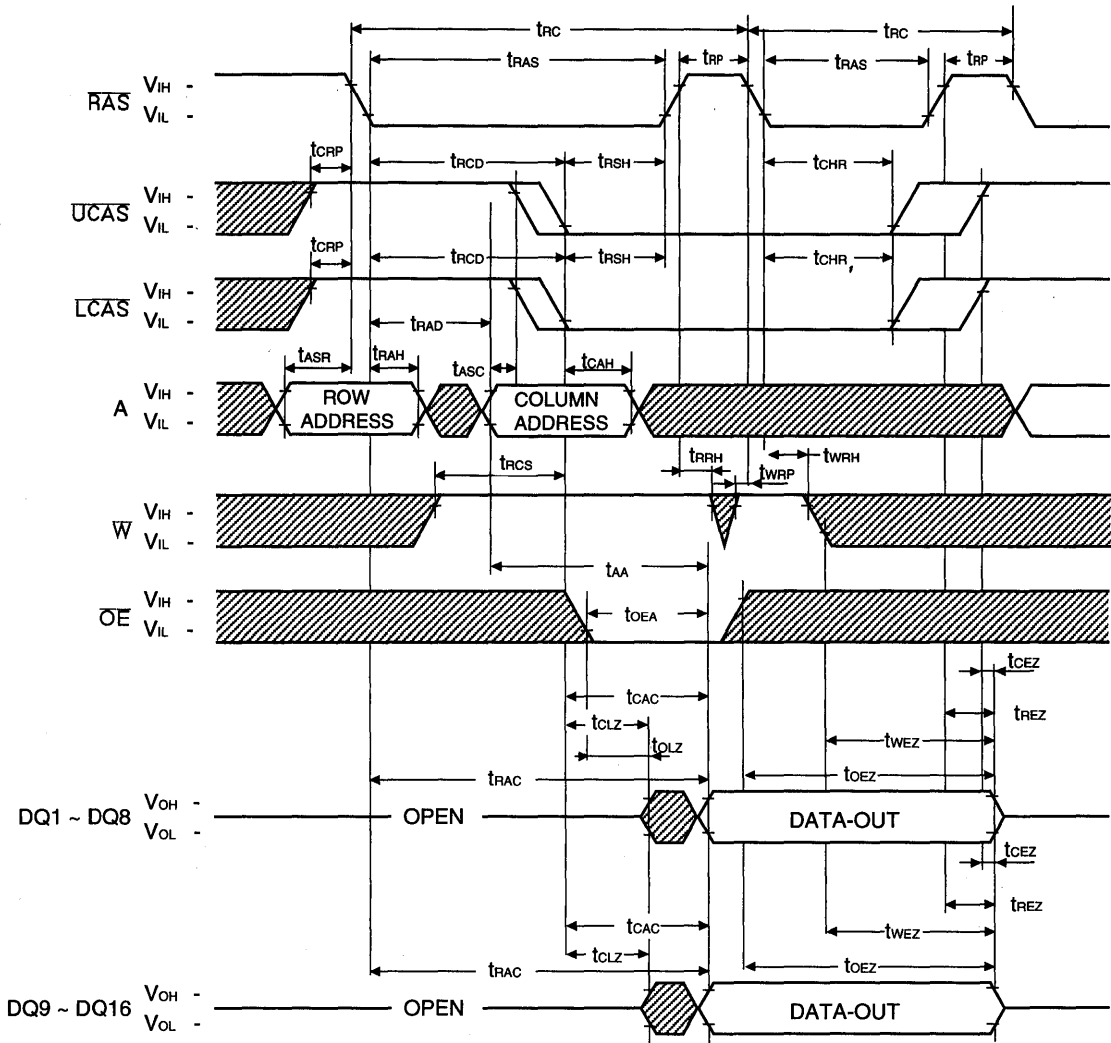
 Don't Care

$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ SELF REFRESH CYCLE(LL-version)

NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, A = Don't Care



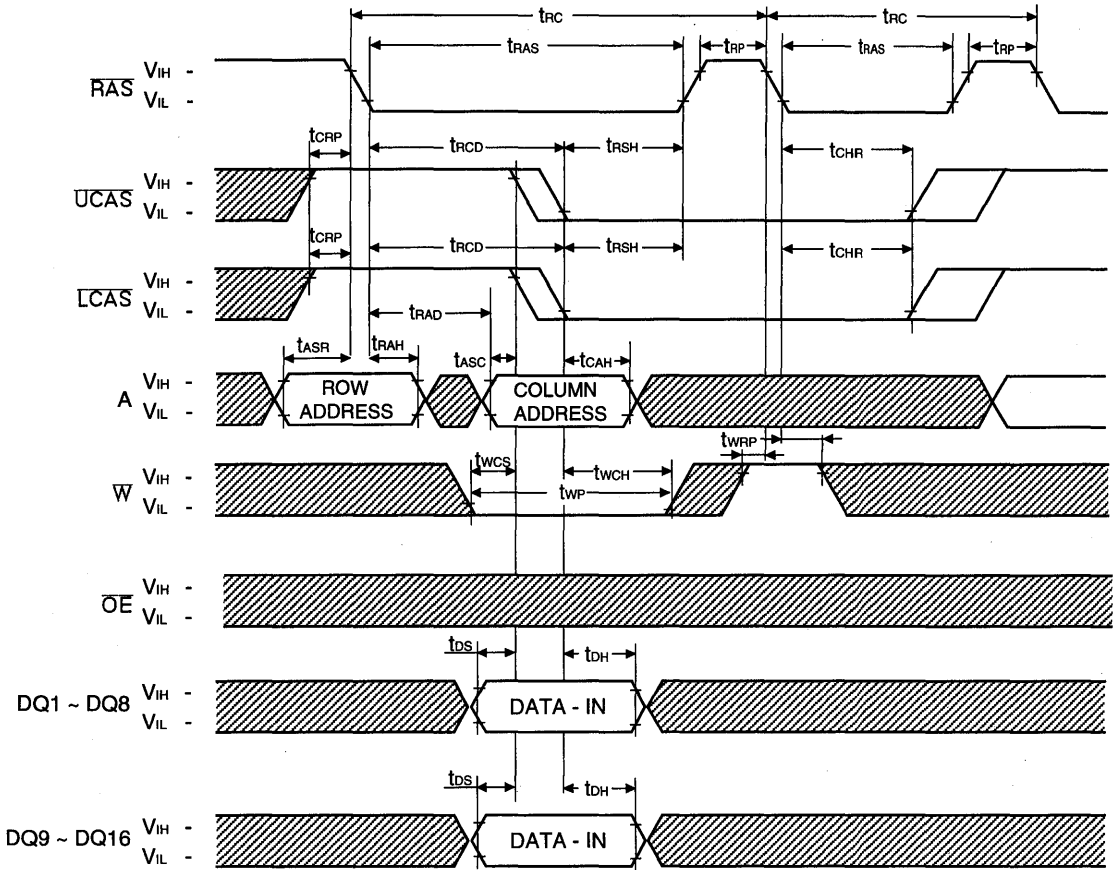
HIDDEN REFRESH CYCLE (READ)



 Don't Care

HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

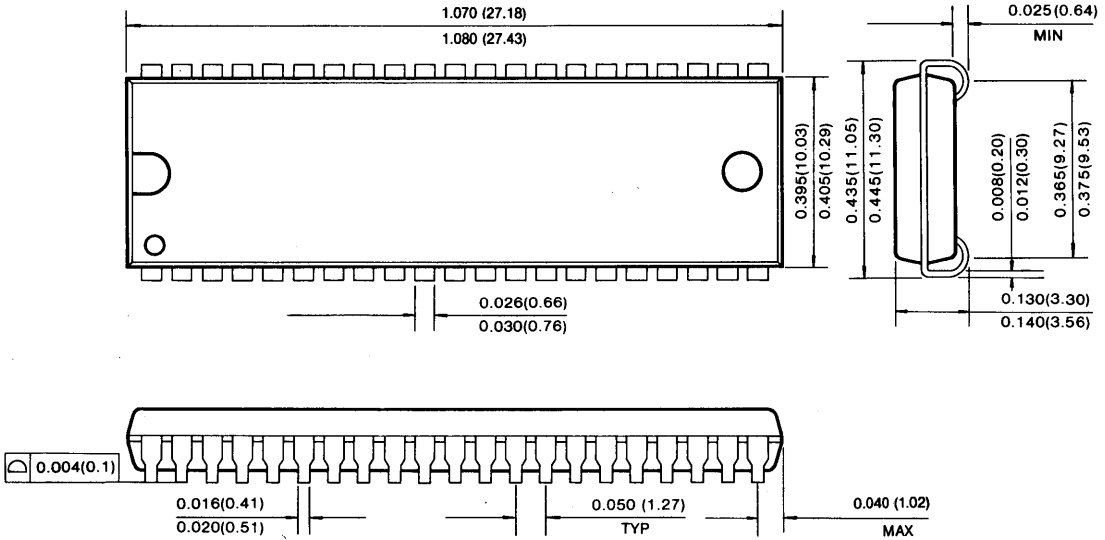


 Don't Care

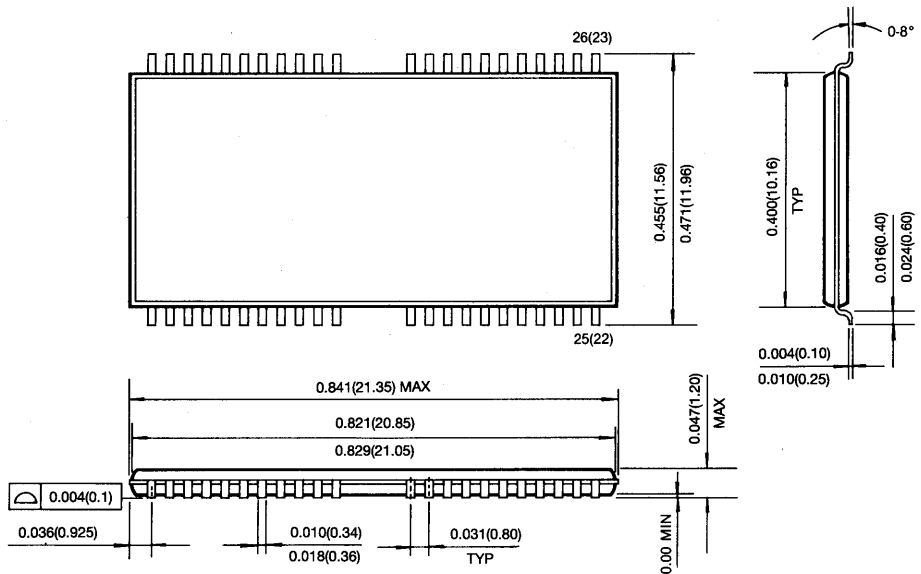
PACKAGE DIMENSION

42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)



1M x 16 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	trAC	tcAC	trc	tHPC
KM416V1204A-6/A-L6/A-F6	60ns	17ns	110ns	24ns
KM416V1204A-7/A-L7/A-F7	70ns	20ns	130ns	29ns
KM416V1204A-8/A-L8/A-F8	80ns	20ns	150ns	34ns

- **Extended Data Out Mode (Fast page Mode with Extended Data Out)**
- **2 CAS Byte/Word Read/Write operation**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **Triple +3.3V ± 0.3V power supply**
- **Refresh Cycle**
 - 1024 cycle/16ms (Normal)
 - 1024 cycle/128ms (L-version)
 - 1024 cycle/128ms (F-version)
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages**

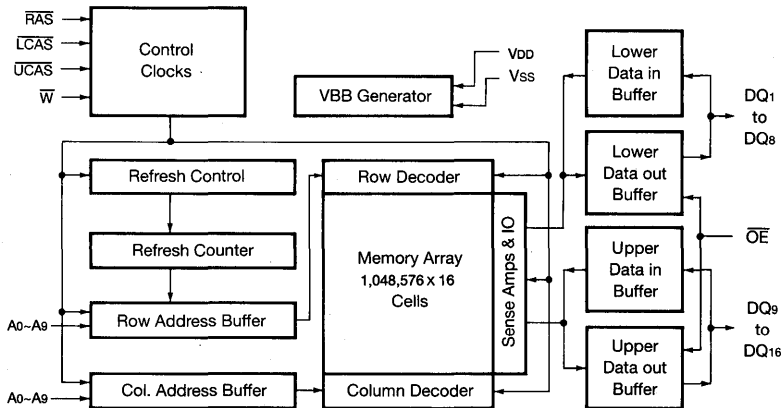
GENERAL DESCRIPTION

The Samsung KM416V1204A/A-L/A-F is a CMOS high speed 1,048,576 bit x 16 Dynamic Random Access Memory. Its design is optimized for high performance applications such as personal computer, and high performance portable computers.

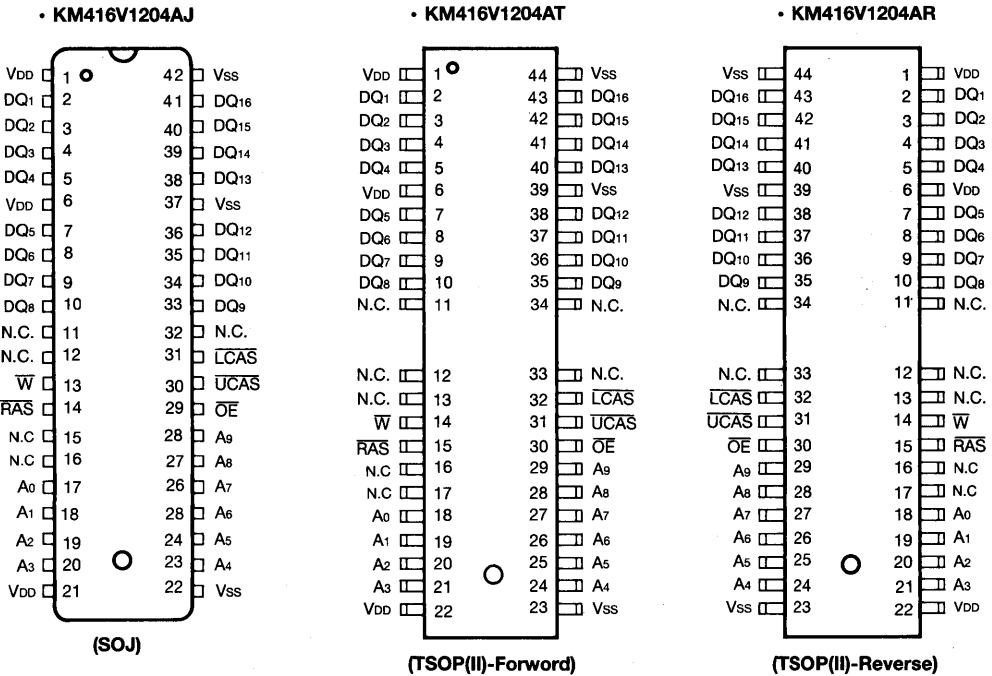
The KM416V1204A/A-L/A-F features EDO Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

The KM416V1204A/A-L/A-F is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A9	Address Inputs
DQ1-16	Data In/Out
VSS	Ground
\bar{RAS}	Row Address Strobe
UCAS	Upper Column Address Strobe
LCAS	Lower Column Address Strobe
\bar{W}	Read/Write Input
OE	Data Output Enable
VDD	Power(+3.3V)
N.C.	No connection

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 4.6	V
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.5 to 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.1	—	V _{DD} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units	
Operating Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @trc=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	icc1	-	150 140 130	mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=V_{IH}$)	KM416V1204A KM416V1204A-L KM416V1204A-F	icc2	-	2 1 1	mA mA mA
$\overline{\text{RAS}}$ -Only Refresh Current* ($\overline{\text{UCAS}}=\overline{\text{LCAS}}=V_{IH}$, $\overline{\text{RAS}}$, Address Cycling @trc=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	icc3	-	150 140 130	mA mA mA
EDO Mode Current* ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$, Address Cycling @tpc=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	icc4	-	120 110 100	mA mA mA
Standby Current ($\overline{\text{RAS}}=\overline{\text{UCAS}}=\overline{\text{LCAS}}=\overline{\text{W}}=V_{DD}-0.2V$)	KM416V1204A KM416V1204A-L KM416V1204A-F	icc5	-	1 300 200	mA μ A μ A
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current* ($\overline{\text{RAS}}$, $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ Cycling @trc=min.)	KM416V1204A-6/A-L6/A-F6 KM416V1204A-7/A-L7/A-F7 KM416V1204A-8/A-L8/A-F8	icc6	-	150 140 130	mA mA mA
Battery Back-Up Current, Average Power Supply Current, Battery Back-Up Mode, Input High Voltage(V _{IH})=V _{DD} -0.2V, Input Low Voltage(V _{IL})=0.2V $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}=0.2V$ DIN=Don't Care, trc=125 μ s (L-Ver) trAS=trAS min-300ns	KM416V1204A-L	icc7	-	350	μ A

DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Self Refresh Current RAS=UCAS=LCAS=0.2V W=OE=A0-A9=VDD-0.2V or 0.2V DQ1-DQ16=VDD-0.2V or 0.2V or Open	KM416V1204A-F	I _{CCS}	-	250	μA
Input Leakage Current (Any input 0 ≤ V _{IN} ≤ V _{DD} +0.3V, all other pins not under test=0V)		I _{I(L)}	-10	10	μA
Output Leakage Current (Data out is disabled, 0V ≤ V _{OUT} ≤ V _{DD})		I _{O(L)}	-10	10	μA
Output High Voltage Level (I _{OH} =-2mA)		V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =2mA)		V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while RAS=VIL. In I_{CC4}, Address can be changed maximum once while one Hyper page mode cycle time t_{HPC}.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0~9)	C _{IN1}	-	5	pF
Input Capacitance (RAS, LCAS, UCAS, W, OE)	C _{IN2}	-	7	pF
Output Capacitance (DQ1~DQ16)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD}=3.3V ± 0.3V, See notes 1,2)

(Test condition : V_{IH}/V_{IL}=2.1V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V, Output Loading C_L=100pF)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		185		205		ns	
Access time from RAS	t _{RAC}		60		70		80	ns	3,4,11
Access time from CAS	t _{CAC}		17		20		20	ns	3,4,5
Access time from column address	t _{AA}		30		35		40	ns	3,11
CAS to output in Low-Z	t _{CLZ}	3		3		3		ns	3
OE to output in Low-Z	t _{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from CAS	t _{CLZ}	3	15	3	20	3	20	ns	7,14
Transition time (rise and fall)	t _t	2	50	2	50	2	50	ns	2
RAS precharge time	t _{RP}	40		50		60		ns	
RAS pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	t _{RSH}	17		20		20		ns	
CAS hold time	t _{CSH}	50		60		70		ns	
CAS pulse width	t _{CAS}	10	10,000	15	10,000	20	10,000	ns	
RAS to CAS delay time	t _{RCD}	20	45	20	50	20	60	ns	4

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
RAS to column address delay time	tRAD	15	30	15	35	15	40	ns	11
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	15
Column address hold time	tCAH	10		15		15		ns	15
Column address hold time referenced to RAS	tAR	45		55		60		ns	6
Column address to RAS lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to CAS	tRCH	0		0		0		ns	9
Read command hold time referenced to RAS	tRRH	0		0		0		ns	9
Write command set-up time	tWCS	0		0		0		ns	8
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to RAS	tWCR	45		50		55		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	tRWL	15		15		20		ns	
Write command to CAS lead time	tCWL	10		15		20		ns	18
Data-in set-up time	tDS	0		0		0		ns	10,21
Data-in hold time	tDH	10		15		15		ns	10,21
Data-in hold time referenced to RAS	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		16		16		16	ms	
Refresh period (L-version)	tREF		128		128		128	ms	
Refresh period (F-version)	tREF		128		128		128	ms	
CAS to W delay time	tCWD	40		50		50		ns	8,17
RAS to W delay time	tRWD	85		95		105		ns	8
Column address to W delay time	tAWD	55		60		65		ns	8
CAS precharge to W delay time	tCPWD	60		65		70		ns	
CAS set-up time (CAS-before-RAS refresh)	tCSR	10		10		10		ns	19
CAS hold time (CAS-before-RAS refresh)	tCHR	10		10		10		ns	20
RAS precharge to CAS hold time	tRPC	5		5		5		ns	
CAS precharge time (C-B-R counter test cycle)	tCPT	20		25		30		ns	
RAS hold time referenced to OE	tROH	15		20		20		ns	
OE access time	tOEA		15		20		20	ns	
OE to data delay	tOED	15		20		20		ns	
Output buffer turn off delay time from OE	tOEZ	3	15	3	20	3	20	ns	7
OE command hold time	tOEH	15		20		20		ns	
Access time from CAS precharge	tCPA		35		40		45	ns	3

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Hyper Page mode cycle time	tHPC	24		29		34		ns	12
Hyper Page mode read-modify-write cycle time	tHPRWC	76		81		91		ns	12
CAS orcharge time (Hyper page mode)	tCP	10		10		10		ns	16
RAS pulse width (Hyper page mode)	tRASP	60	200.000	70	200.000	80	200.000	ns	
RAS hold time from CAS precharge	tRHCP	35		40		45		ns	
Output data hold time	tDOH	5		5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	15	3	20	3	20	ns	7,14
Output buffer turn off delay from W	tWEZ	3	15	3	20	3	20	ns	7
W to data delay	tWED	15		20		20		ns	
OE to CAS hold time	tOCH	5		5		5		ns	
CAS hold time to OE	tCHO	5		5		5		ns	
OE precharge time	tOEP	5		5		5		ns	
W pulse width	tWPE	5		5		5		ns	
RAS pulse width (F-ver)	tRASS	100		100		100		μs	13
RAS precharge time (F-ver)	tRPS	110		130		150		ns	13
CAS hold time (F-ver)	tCHS	-50		-50		-50		ns	13

KM416V1204A/A-L/A-F Truth Table

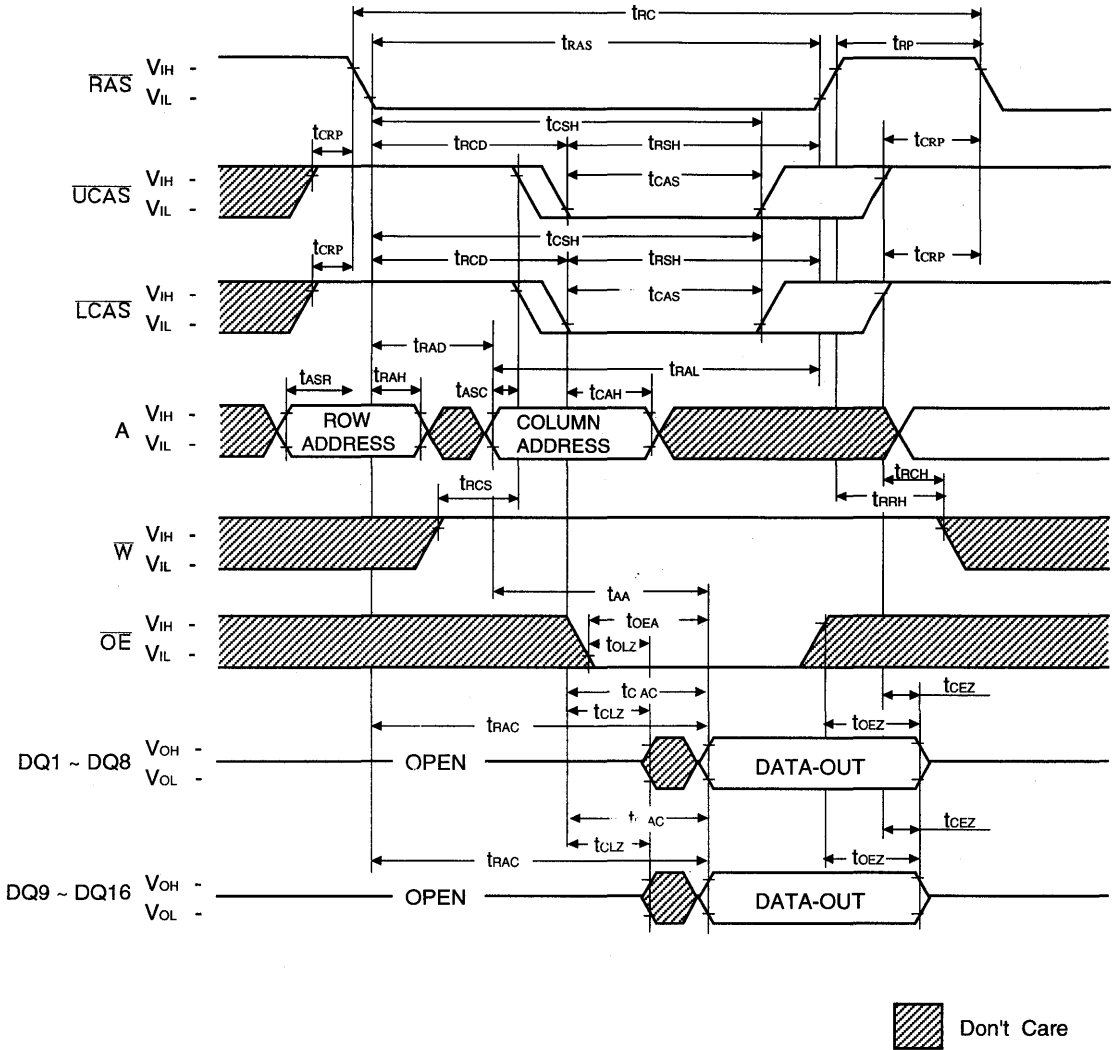
RAS	LCAS	UCAS	W	OE	DQ1~DQ8	DQ9~DQ16	STATE
H	X	X	X	X	HI-Z	HI-Z	Standby
L	H	H	X	x	HI-Z	HI-Z	Refresh
L	L	H	H	L	DQ-OUT	HI-Z	Lower Byte Read
L	H	L	H	L	HI-Z	DQ-OUT	Upper Byte Read
L	L	L	H	L	DQ-OUT	DQ-OUT	Word Read
L	L	H	L	H	DQ-IN	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	DQ-IN	Upper Byte Write
L	L	L	L	H	DQ-IN	DQ-IN	Word Write
L	L	L	H	H	HI-Z	HI-Z	-

NOTES

1. An initial pause of 200 μ s is required after power-up followed by any 8 ROR or CBR cycles before proper device operation is achieved.
2. $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL Loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{RAD}(\max)$.
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$ and $t_{AWD} \geq t_{AWD}(\min)$, then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
11. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
12. $t_{ASC} \geq t_{CP} \min$, Assume $t_r = 2.0ns$.
13. 1024 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification (F-version)
14. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
15. t_{ASC} , t_{CAH} are referenced to the earlier \overline{CAS} falling edge.
16. t_{CP} is specified from the last \overline{CAS} rising edge in the previous cycle to the first \overline{CAS} falling edge in the next cycle.
17. t_{CWD} is referenced to the later \overline{CAS} falling edge at word read-modify-write cycle.
18. t_{CWL} is specified from \overline{W} falling edge to the earlier \overline{CAS} rising edge.
19. t_{CSR} is referenced to earlier \overline{CAS} falling low before \overline{RAS} transition low.
20. t_{CHR} is referenced to the later \overline{CAS} rising high after \overline{RAS} transition low.
21. t_{DS} , t_{DH} is independetly specified for lower byte $D_{in(1-8)}$, upper byte $D_{in(9-16)}$

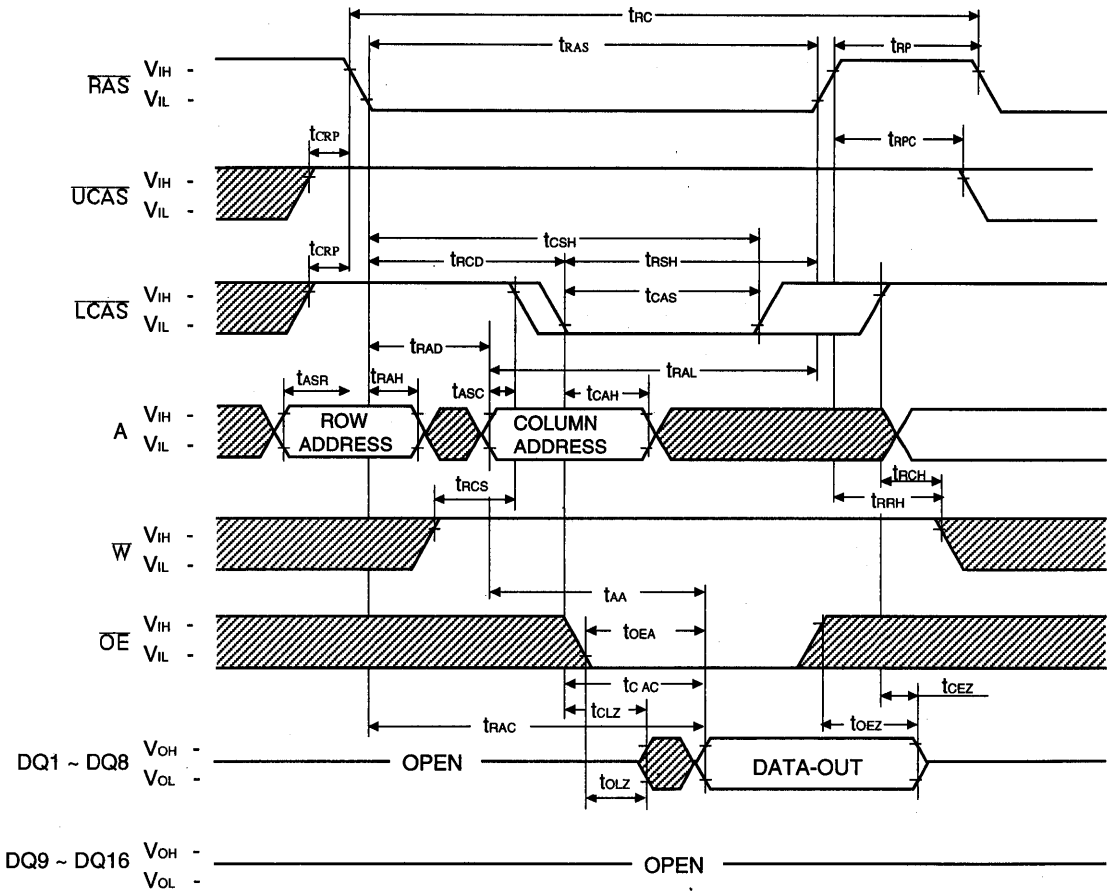
TIMING DIAGRAM
WORD READ CYCLE

NOTE : $D_{IN} = OPEN$



TIMING DIAGRAM
LOWER BYTE READ CYCLE

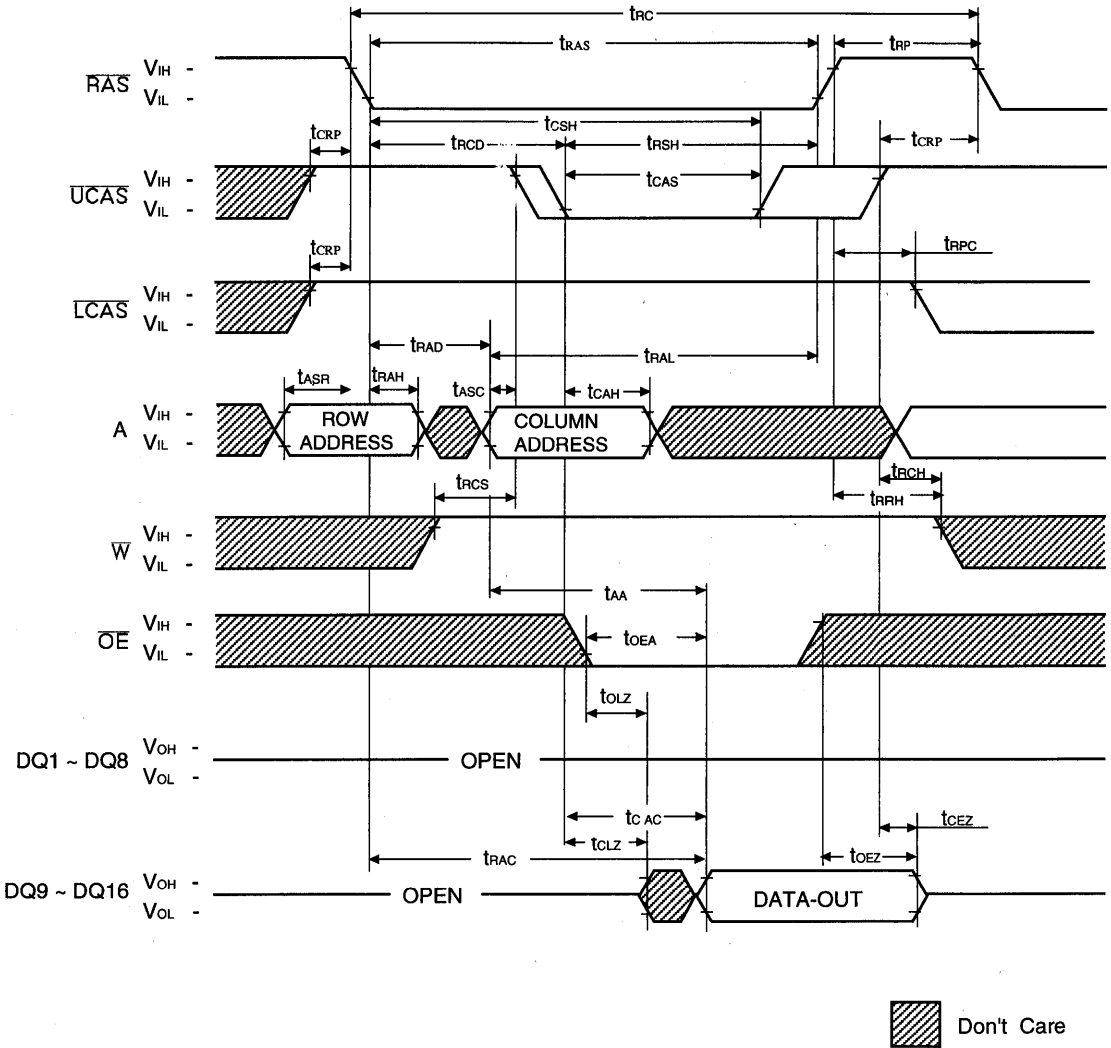
NOTE : D_{IN} = OPEN



 Don't Care

**TIMING DIAGRAM
UPPER BYTE READ CYCLE**

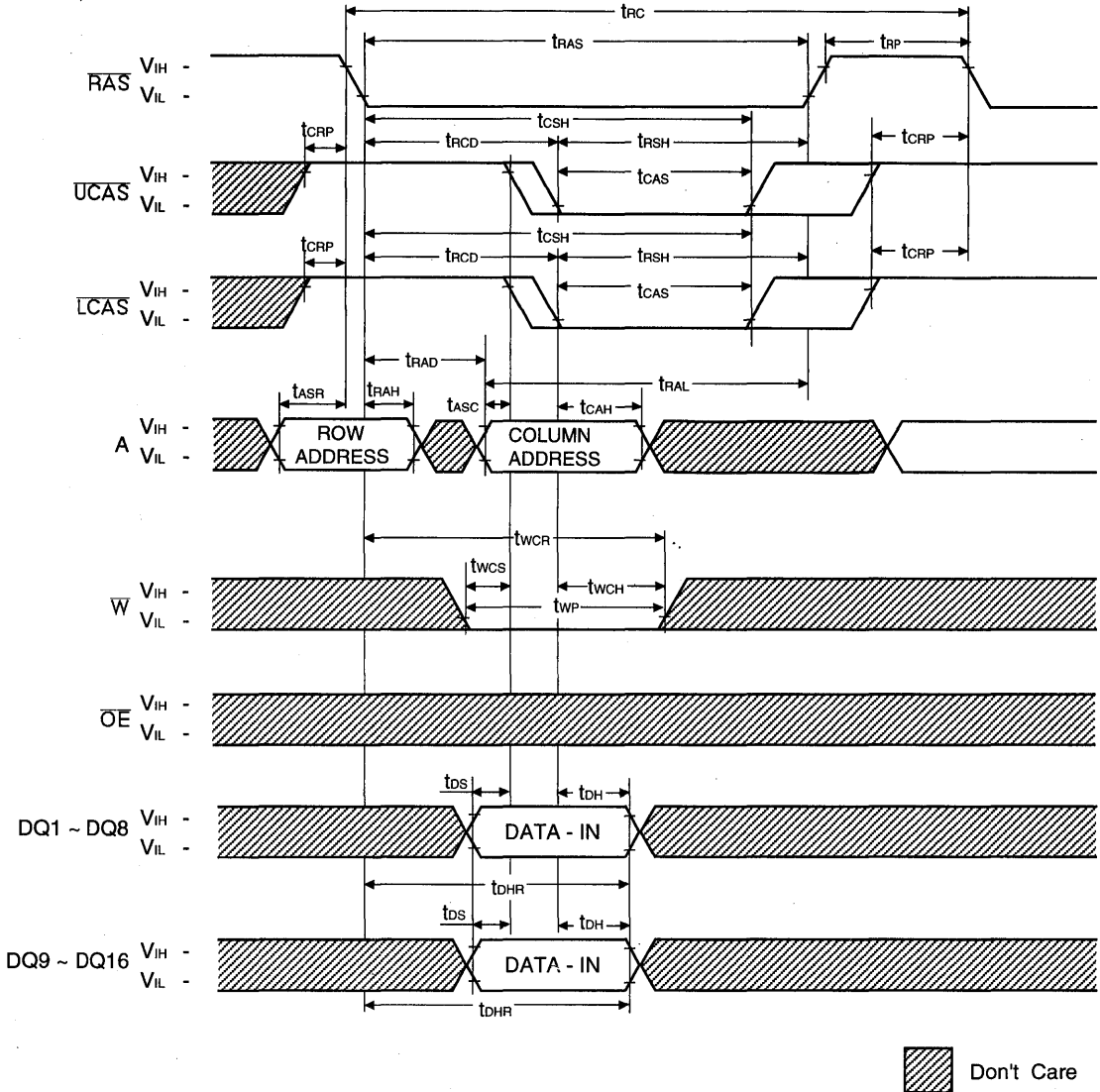
NOTE : D_{IN} = OPEN



6

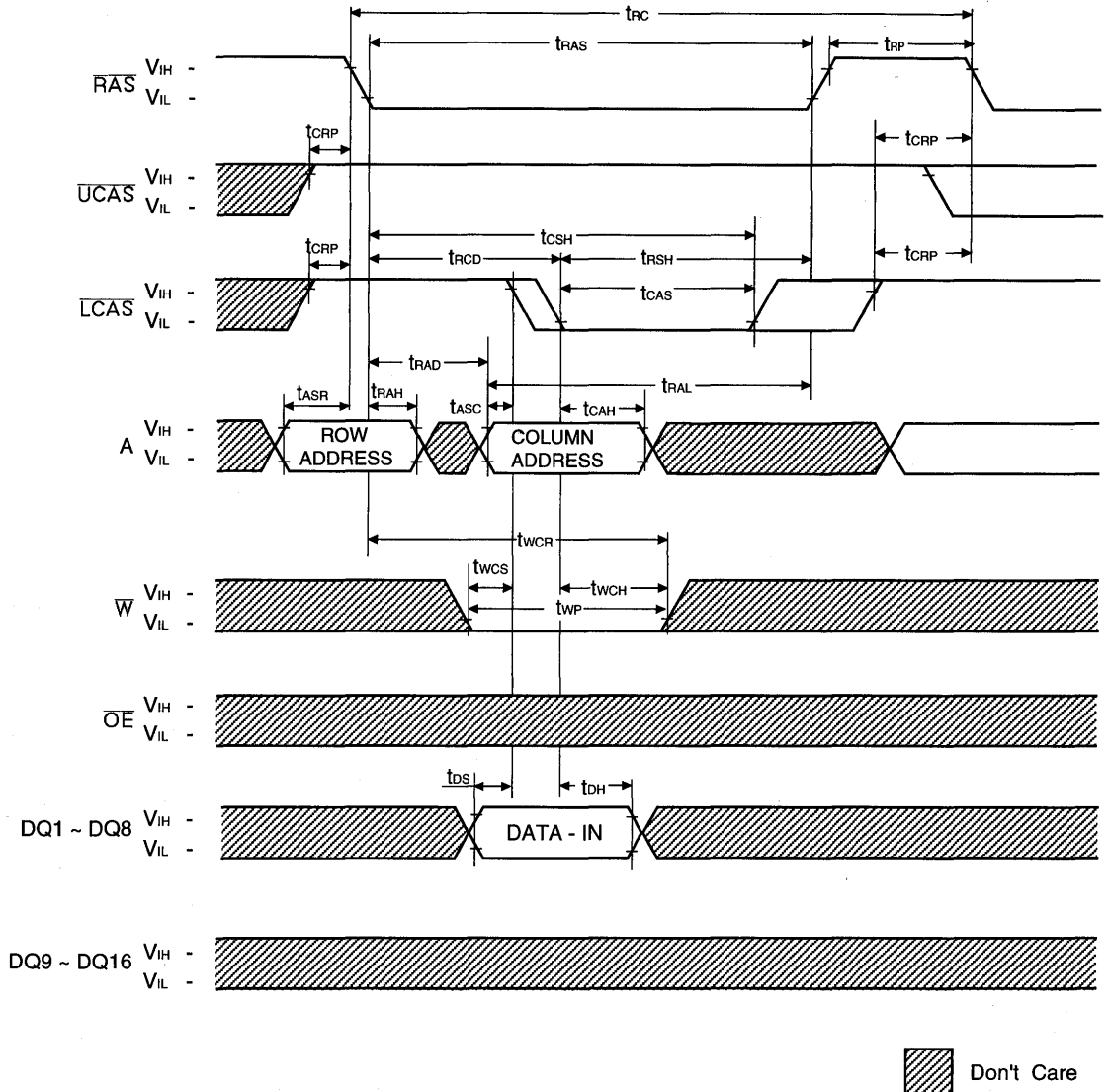
WORD WRITE CYCLE (EARLY WRITE)

NOTE : D_{out} = OPEN



LOWER BYTE WRITE CYCLE (EARLY WRITE)

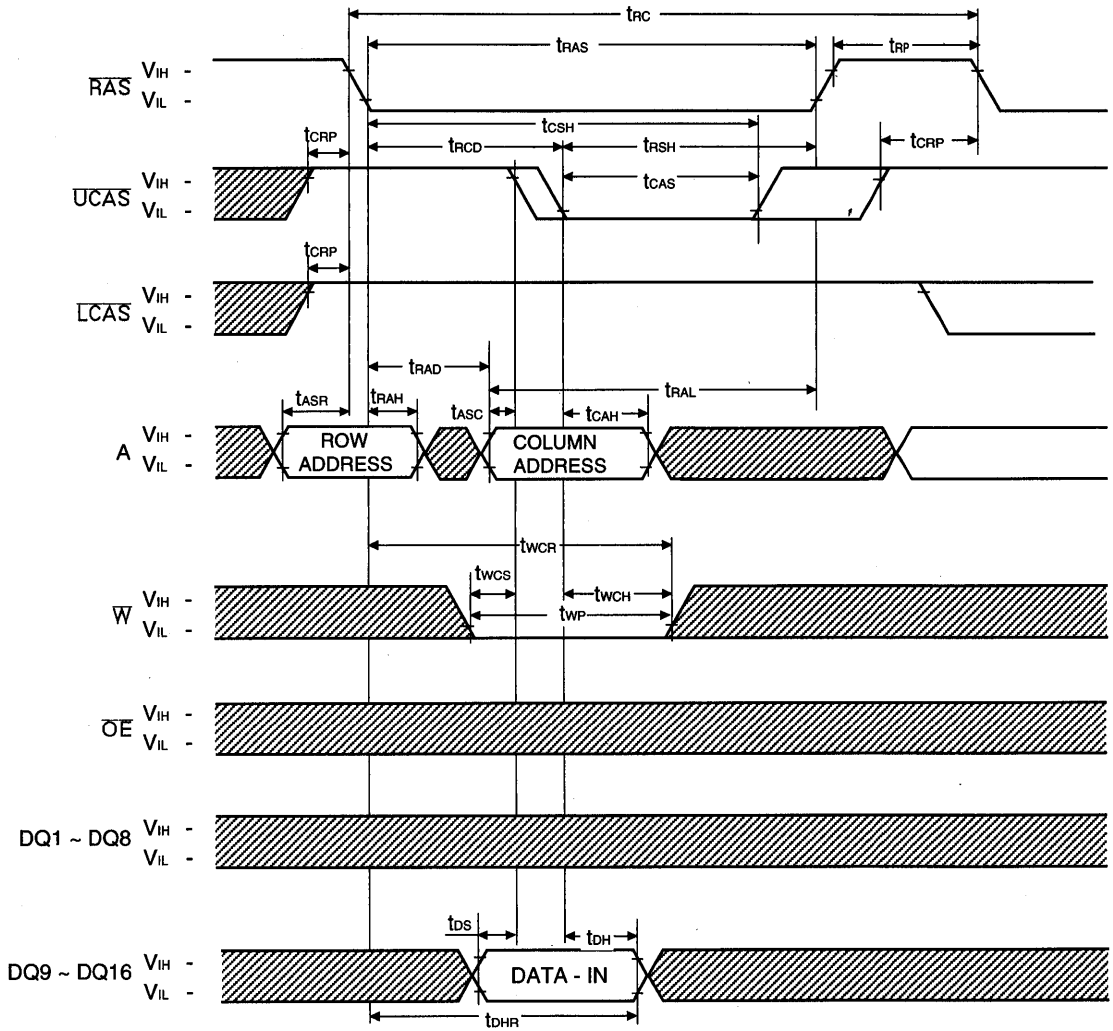
NOTE : Dout = OPEN



6

UPPER BYTE WRITE CYCLE (EARLY WRITE)

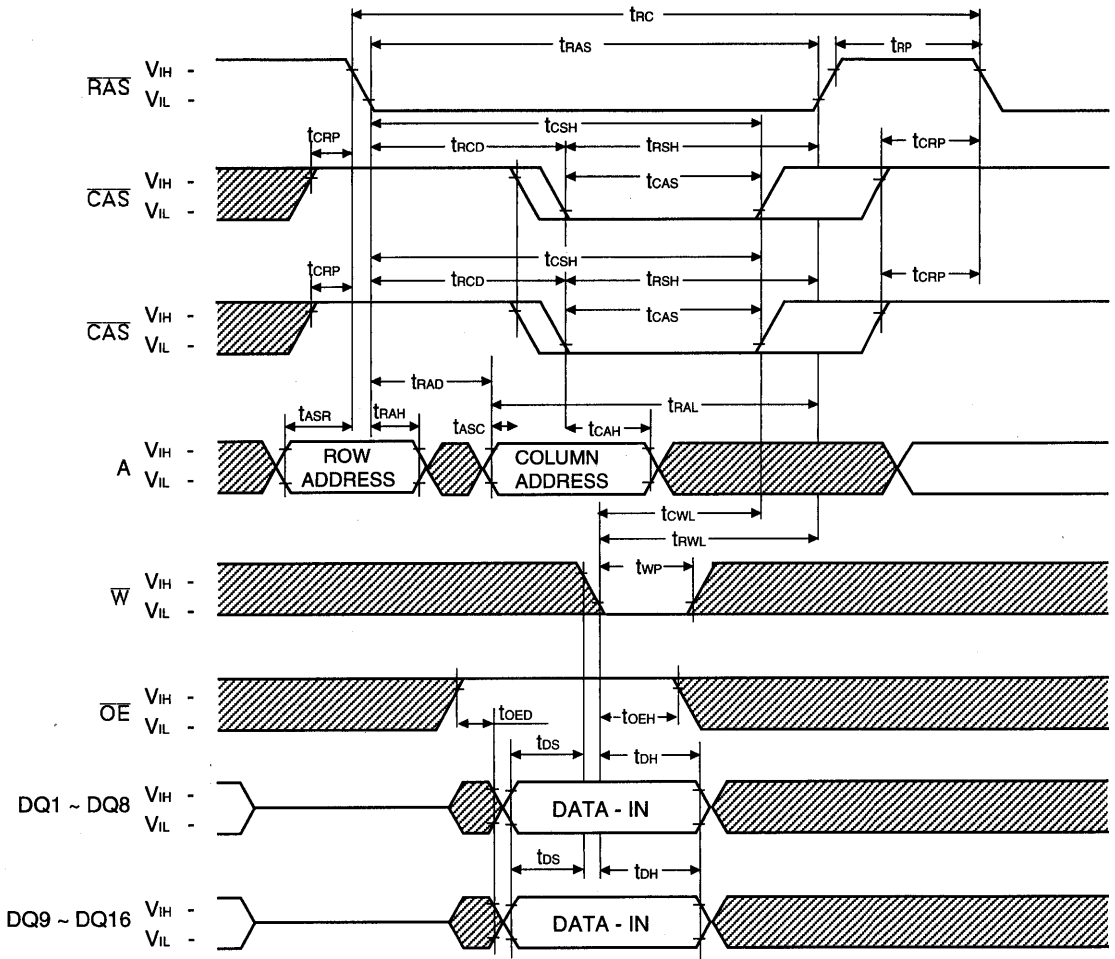
NOTE : D_{OUT} = OPEN



 Don't Care

WORD WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : D_{OUT} = OPEN

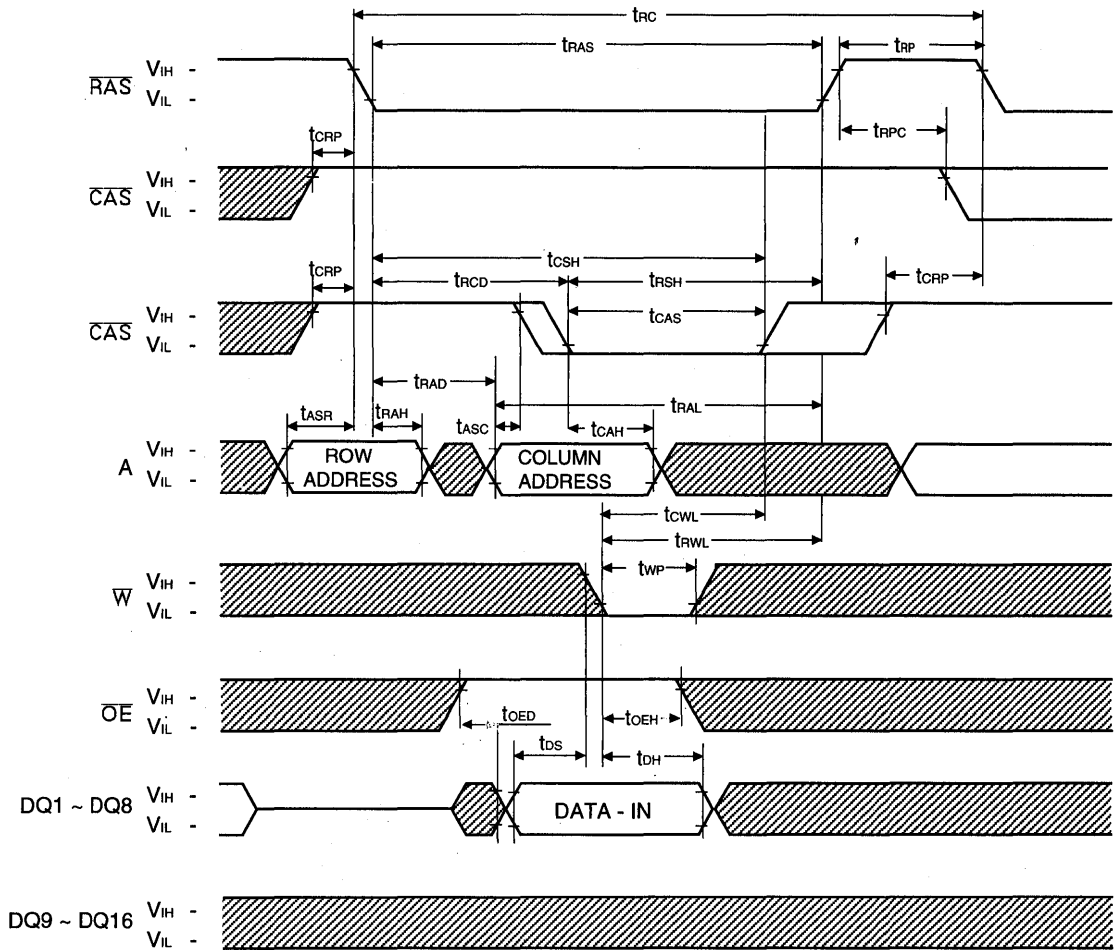


 Don't Care

6

LOWER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

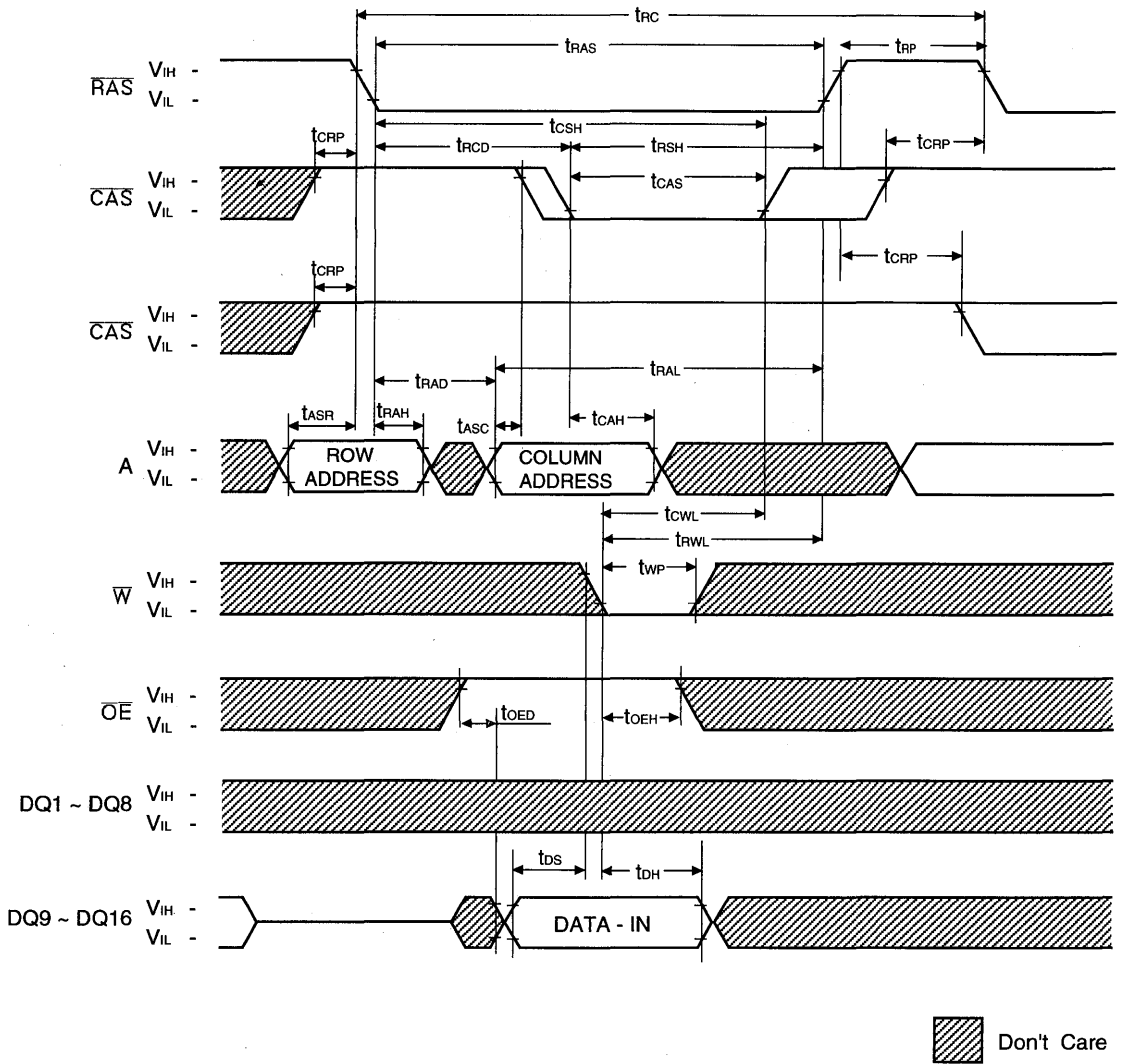
NOTE : DOUT = OPEN



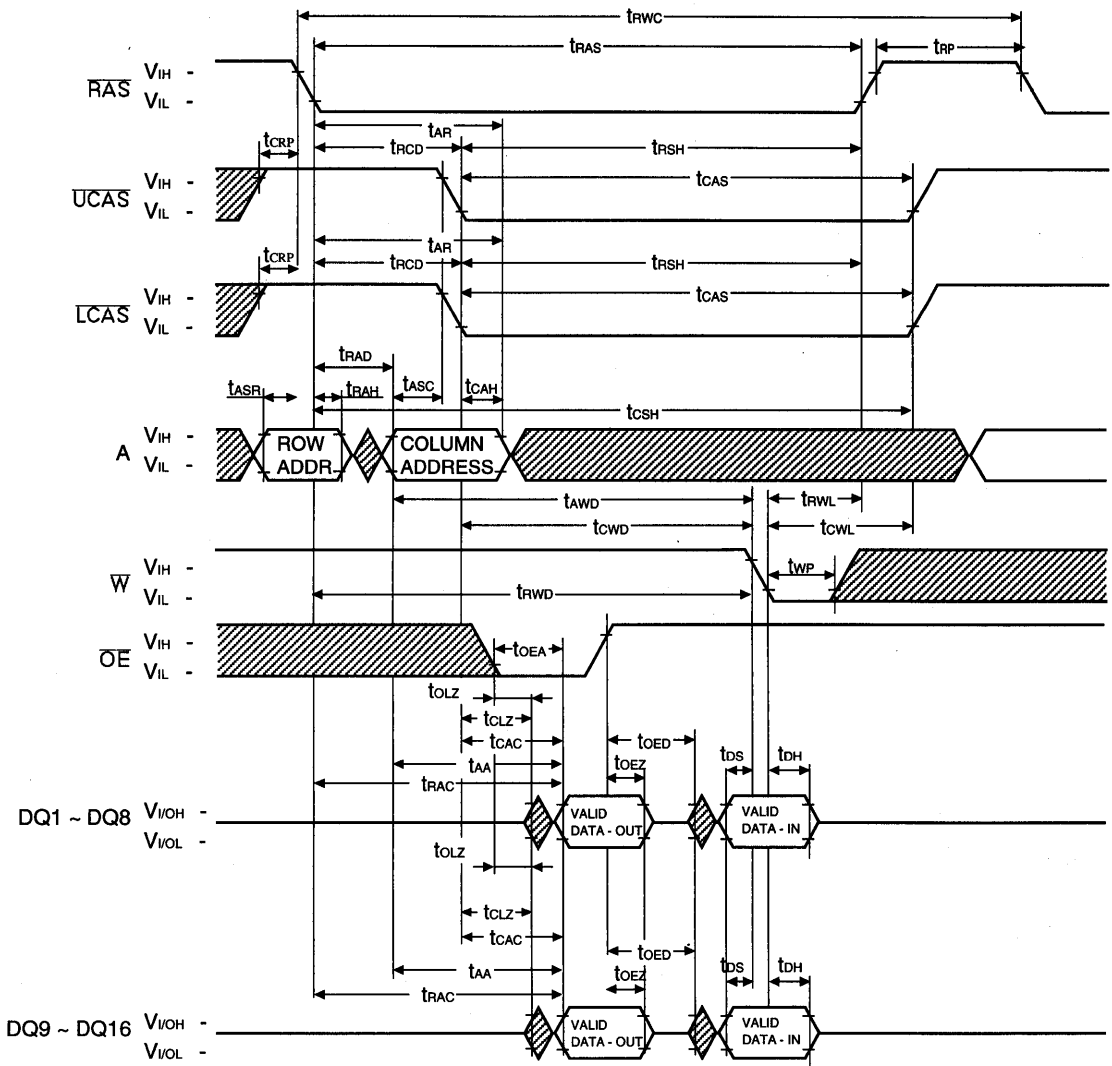
 Don't Care

UPPER BYTE WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : D_{out} = OPEN

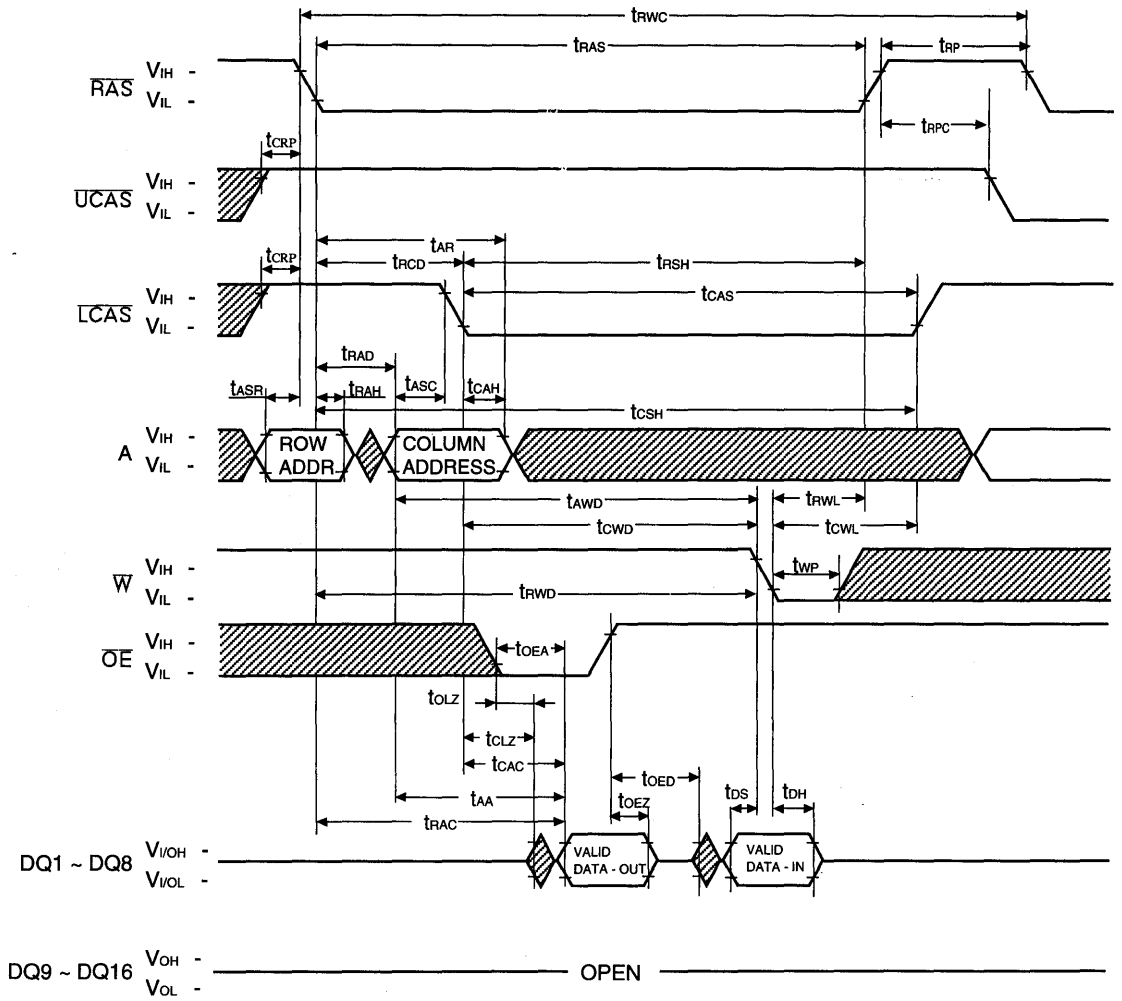


WORD READ - MODIFY - WRITE CYCLE



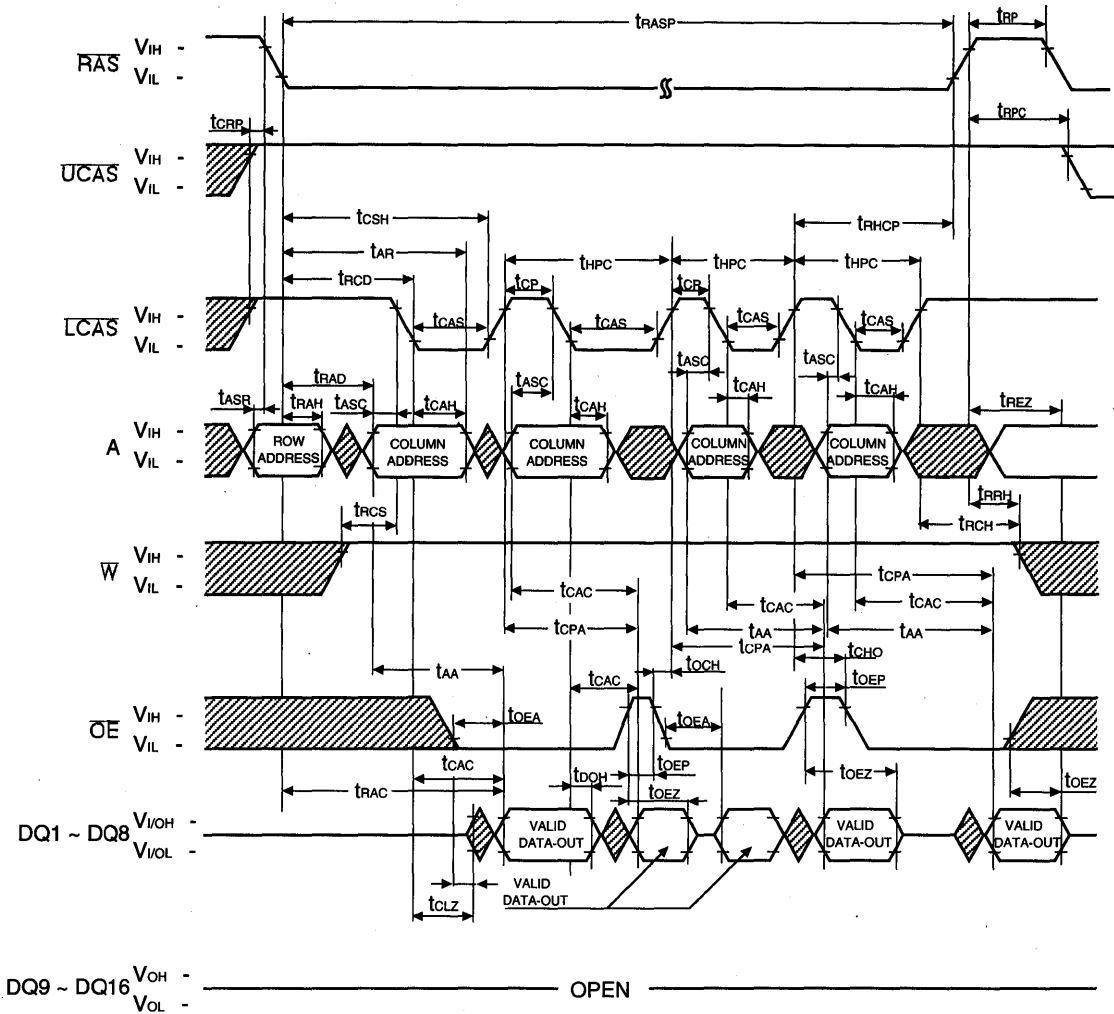
 Don't Care

LOWER-BYTE READ - MODIFY - WRITE CYCLE



6

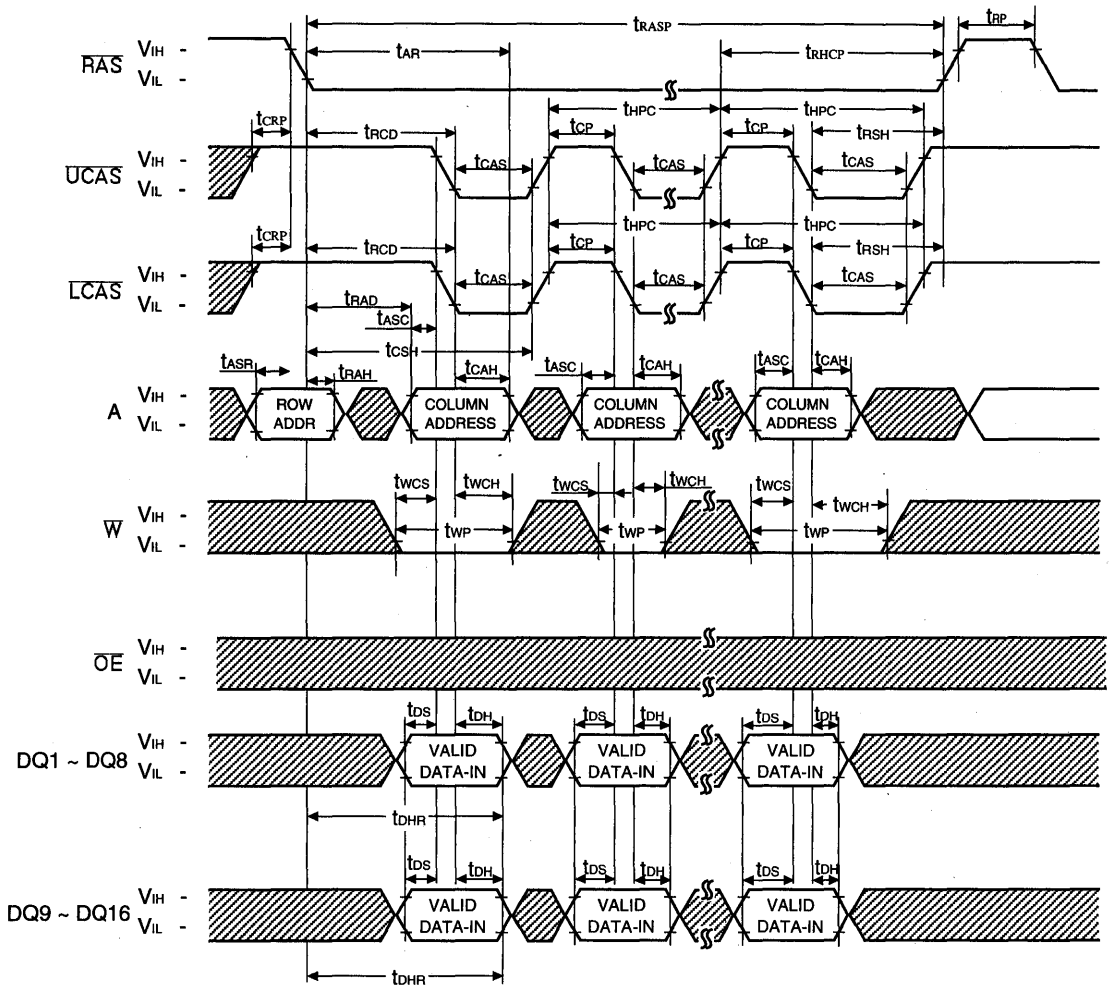
HYPER PAGE MODE LOWER BYTE READ CYCLE



 Don't Care

HYPER PAGE MODE WORD WRITE CYCLE (EARLY WRITE)

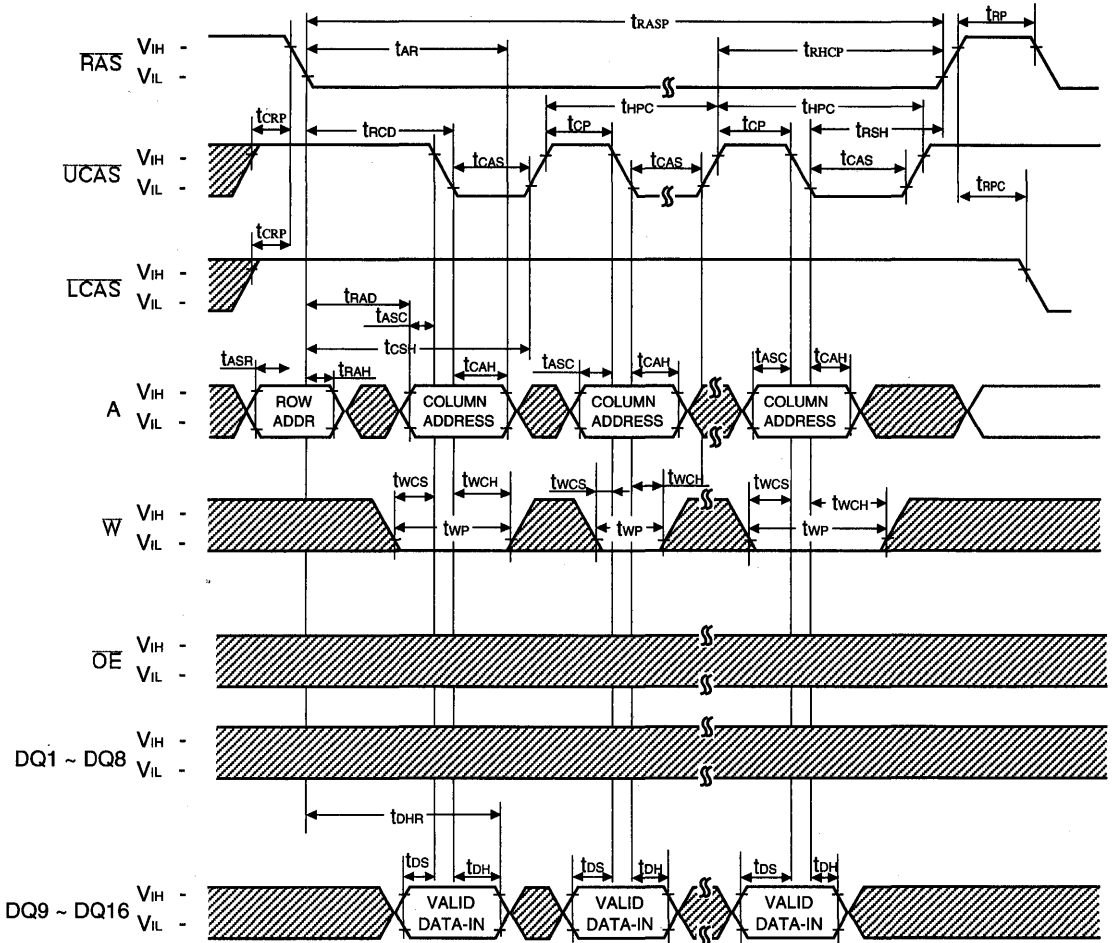
NOTE : Dout = Open



 Don't Care

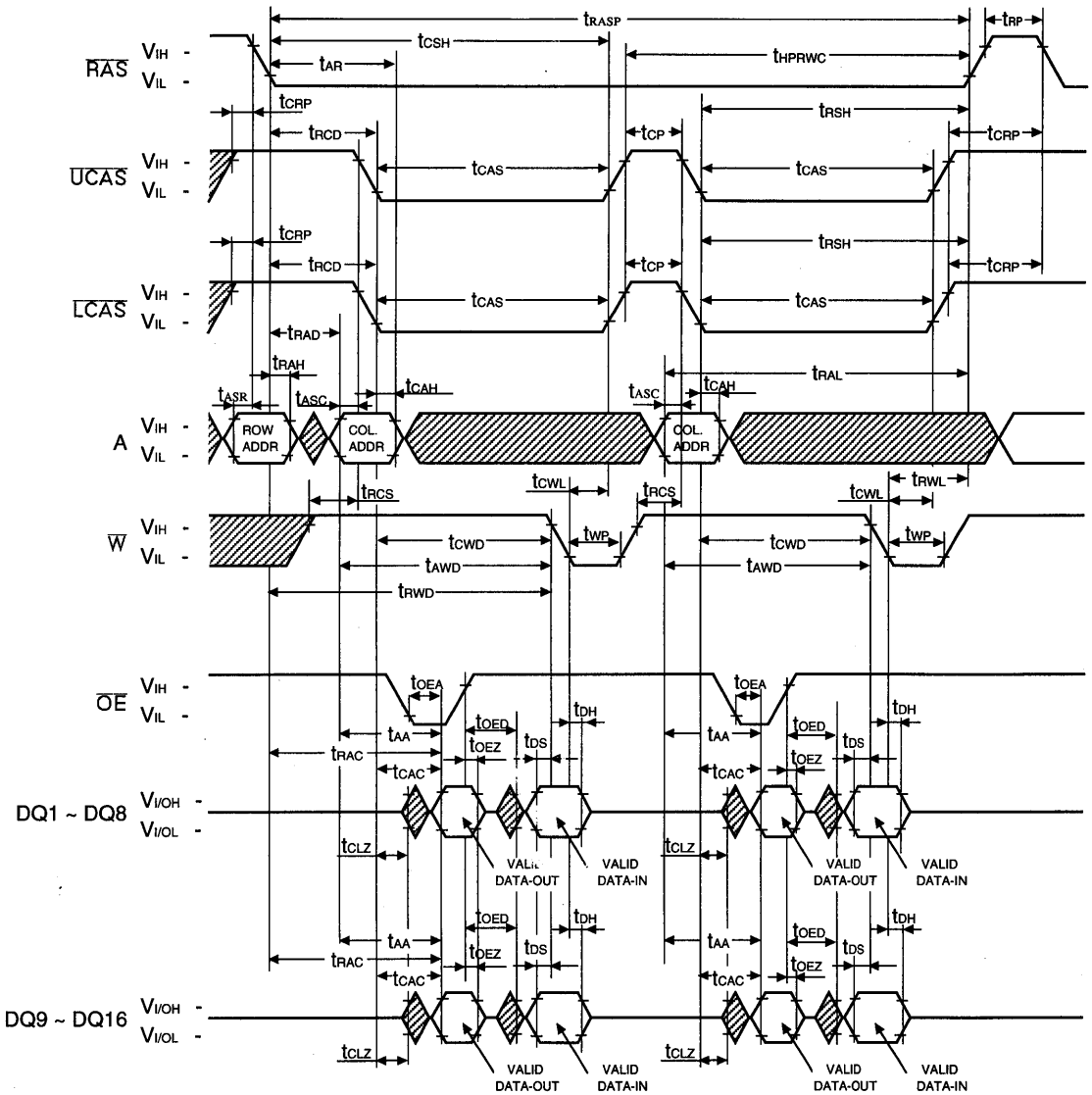
HYPER PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)

NOTE : Dout = Open



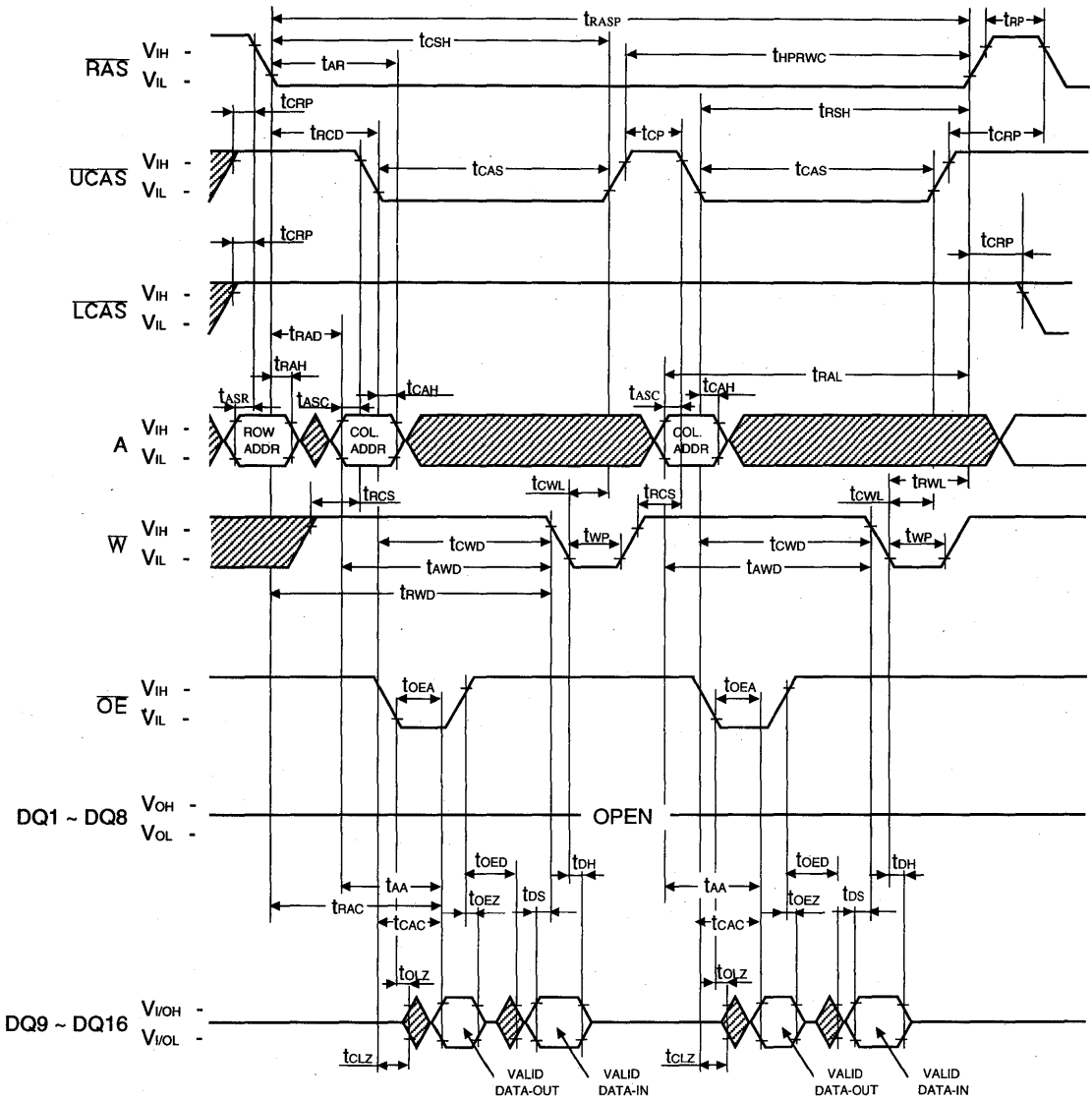
 Don't Care

HYPER PAGE MODE WORD READ-MODIFY-WRITE CYCLE



 Don't Care

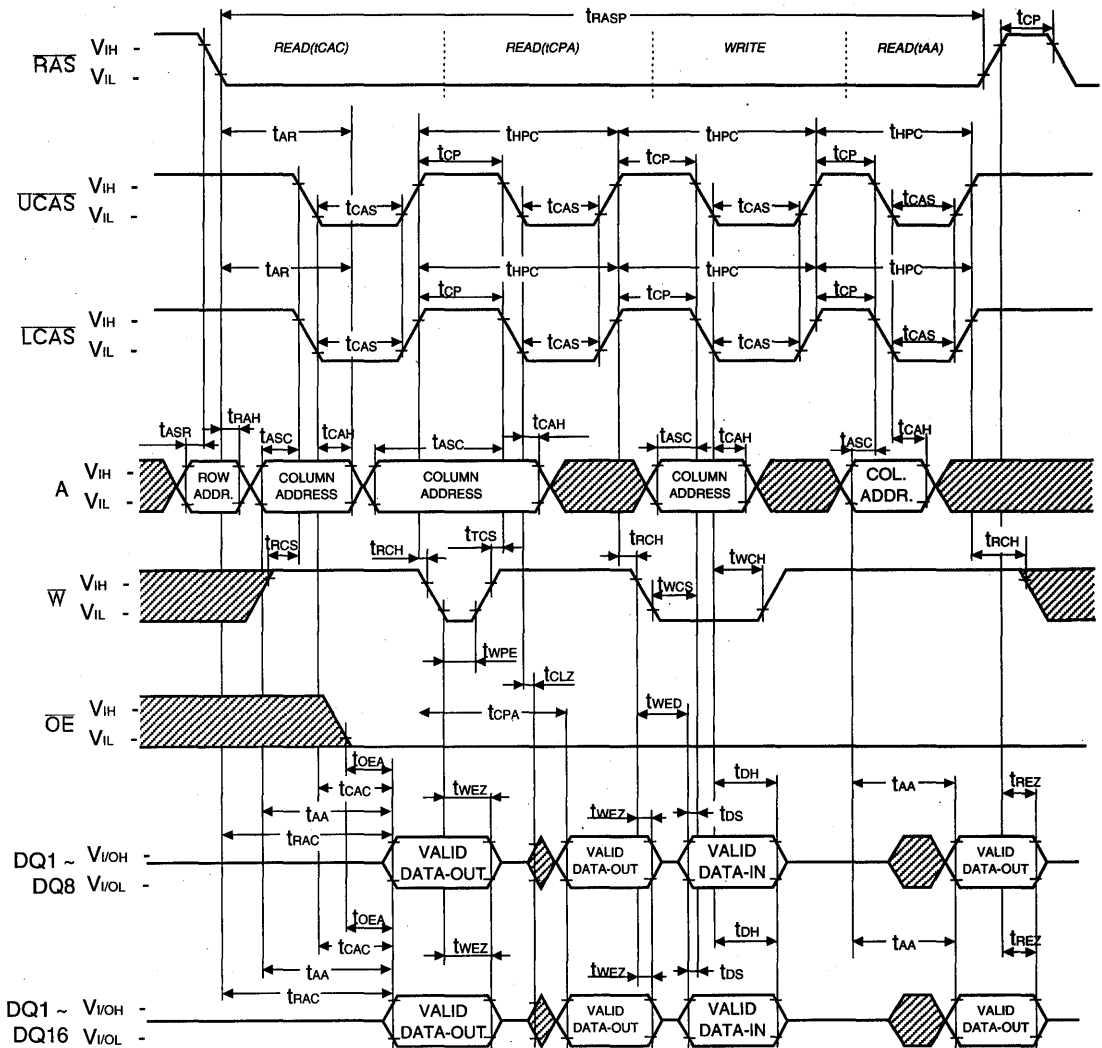
HYPER PAGE MODE UPPER-BYTE-READ-MODIFY-WRITE CYCLE



6

 Don't Care

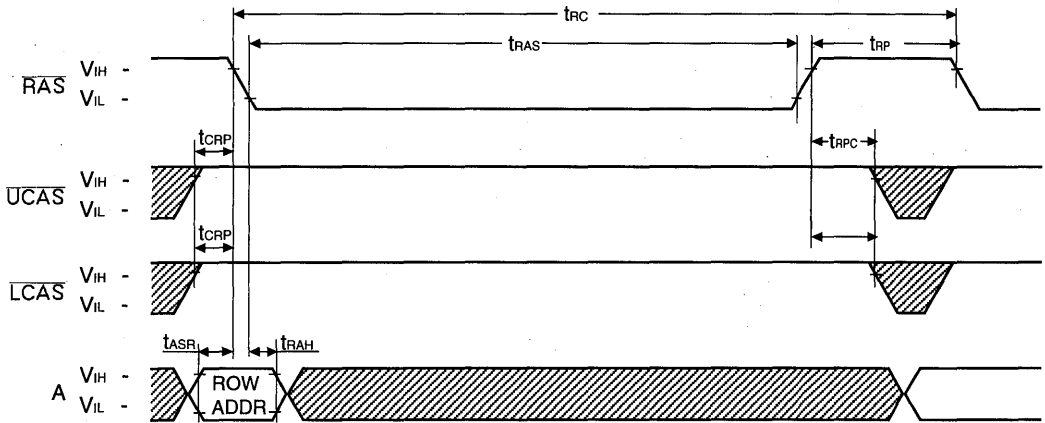
HYPER PAGE READ AND WRITE MIXED CYCLE



 Don't Care

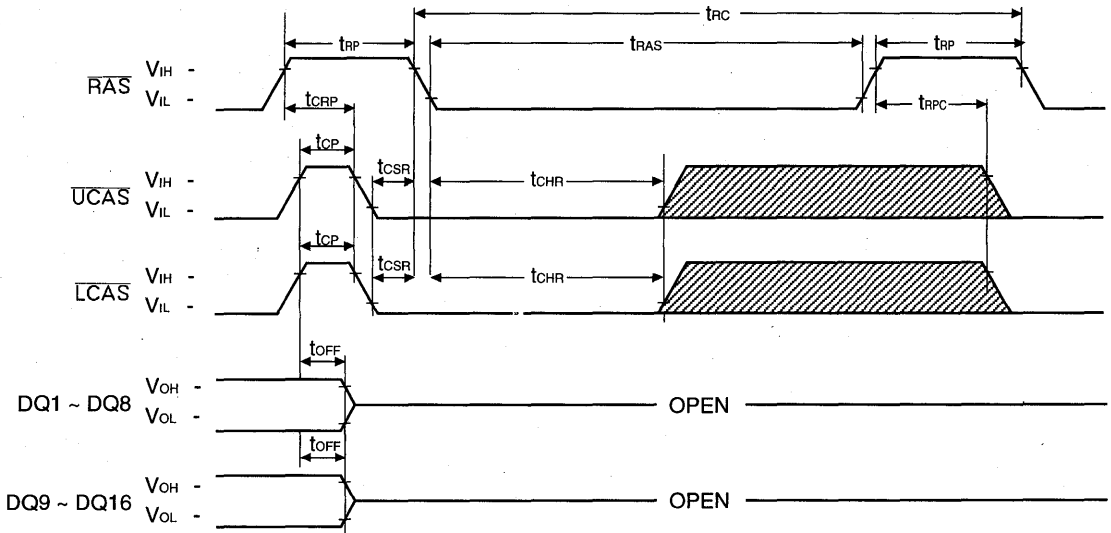
RAS-ONLY REFRESH CYCLE


NOTE : \bar{W} , \bar{OE} , D_{IN} = Don't care
 D_{OUT} = Open



$\bar{C}AS$ -BEFORE- $\bar{R}AS$ REFRESH CYCLE

NOTE : \bar{W} , \bar{OE} , A = Don't Care

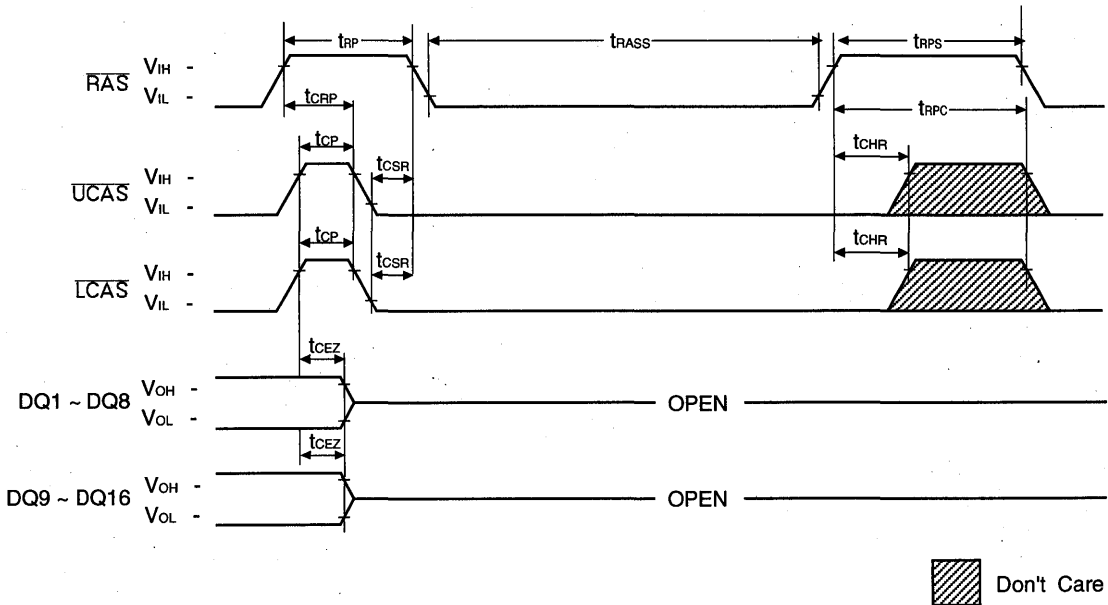


 Don't Care

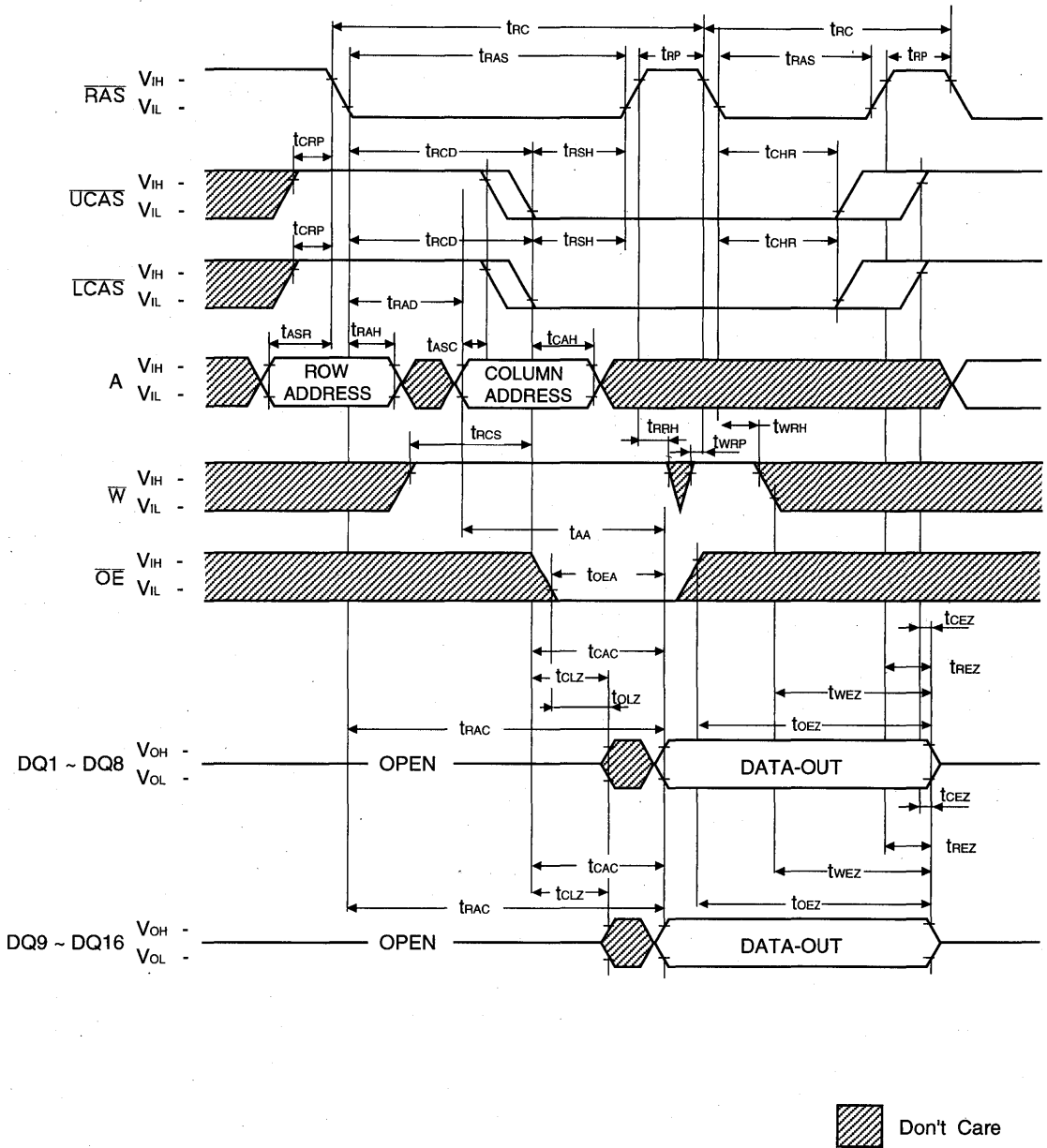
6

CAS-BEFORE-RAS SELF REFRESH CYCLE(LL-version)

NOTE : \bar{W} , \bar{OE} , A = Don't Care

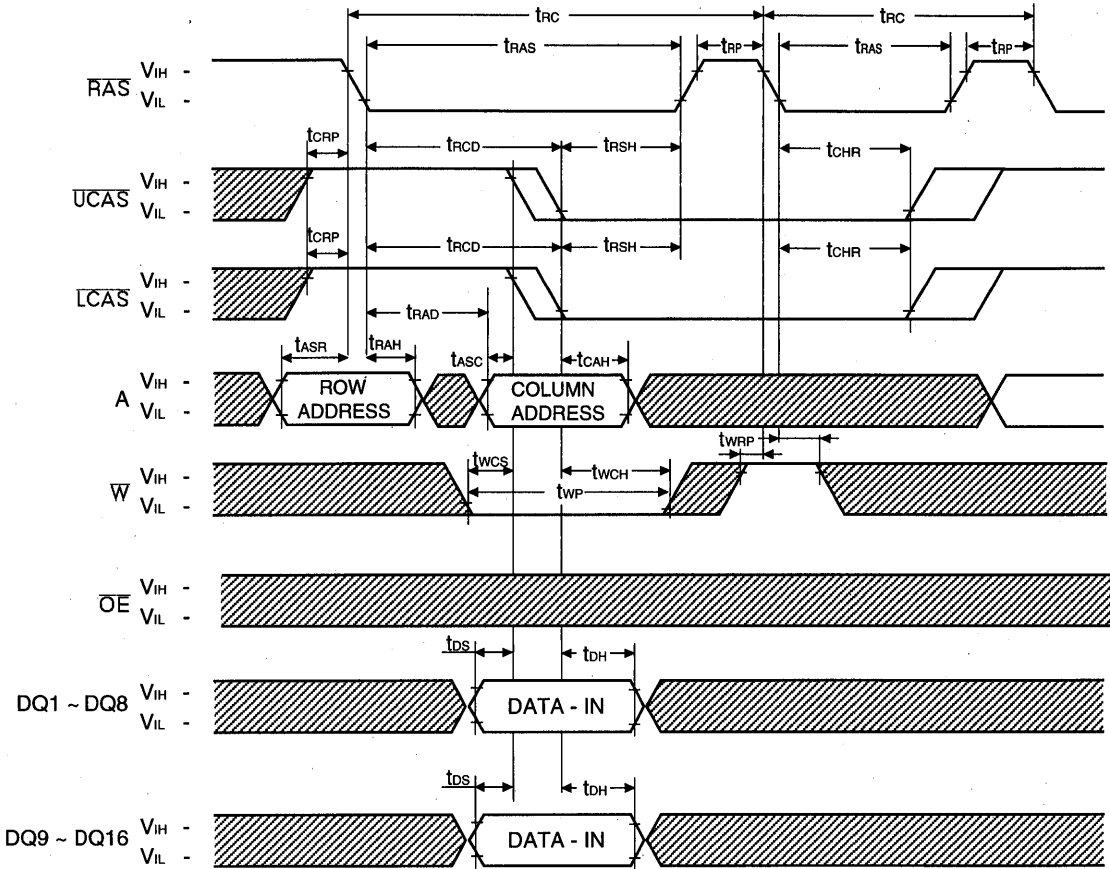


HIDDEN REFRESH CYCLE (READ)



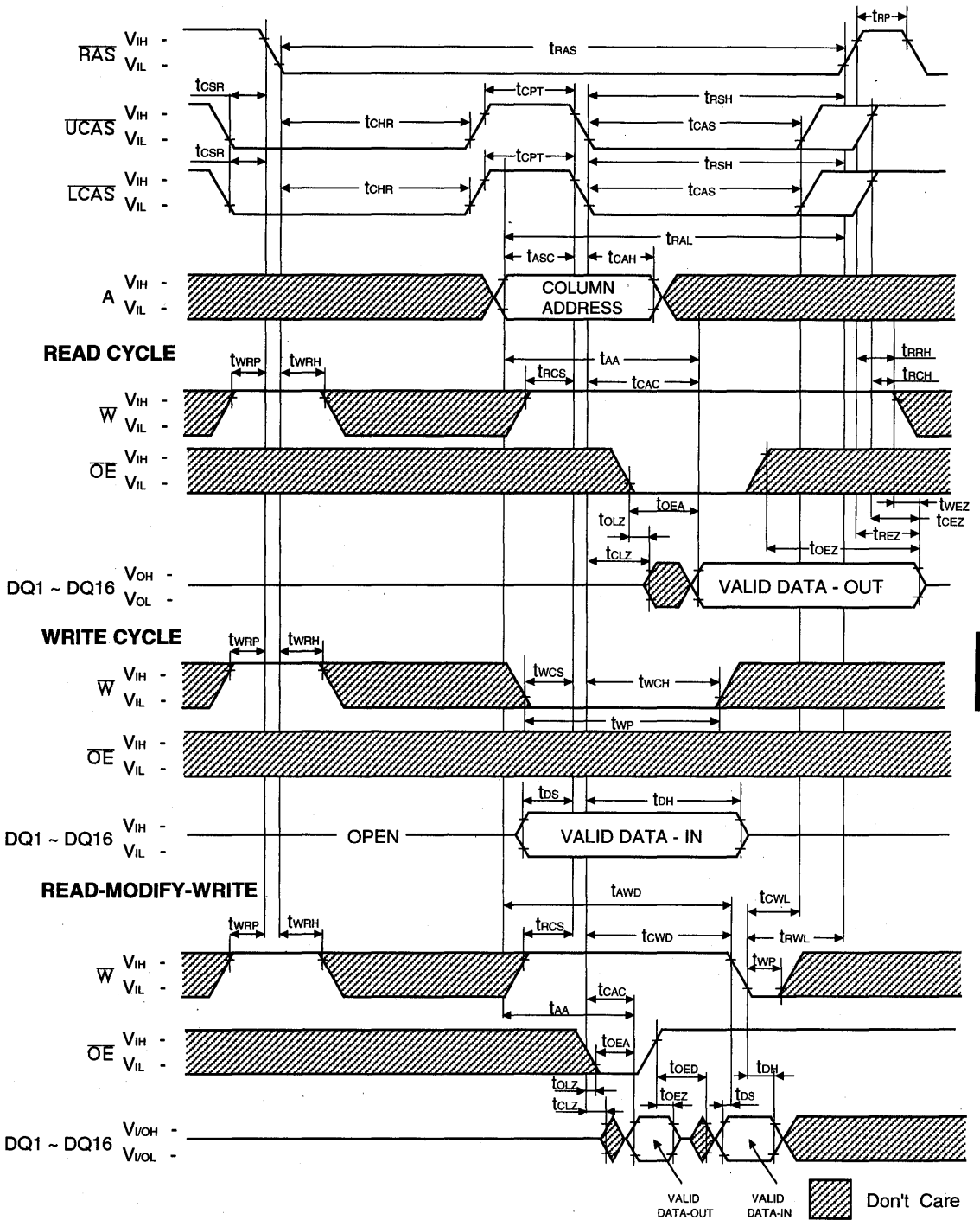
HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



 Don't Care

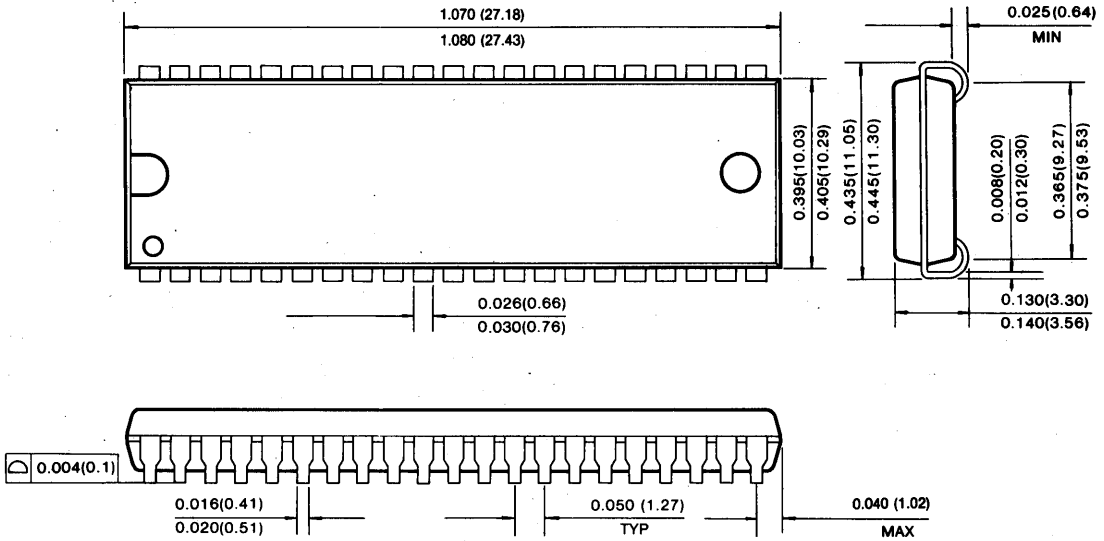
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



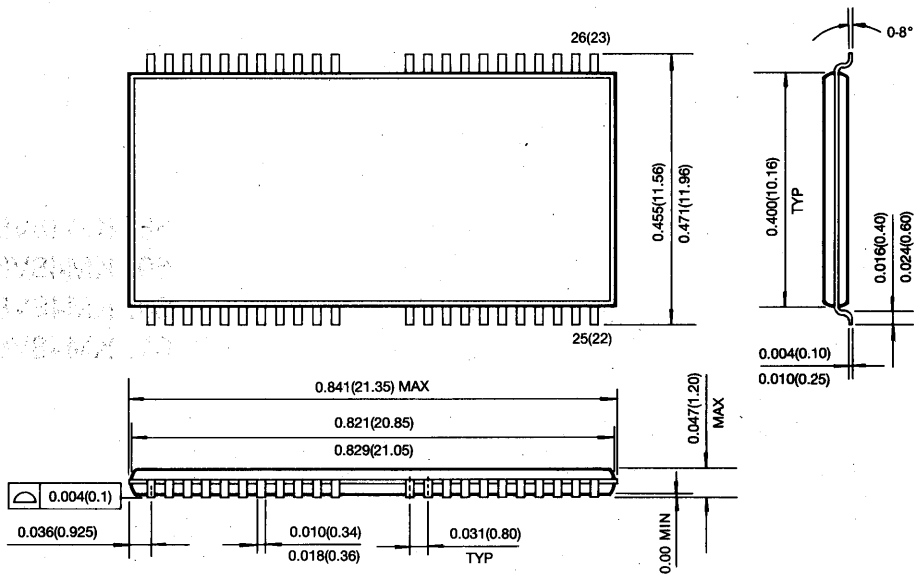
PACKAGE DIMENSION

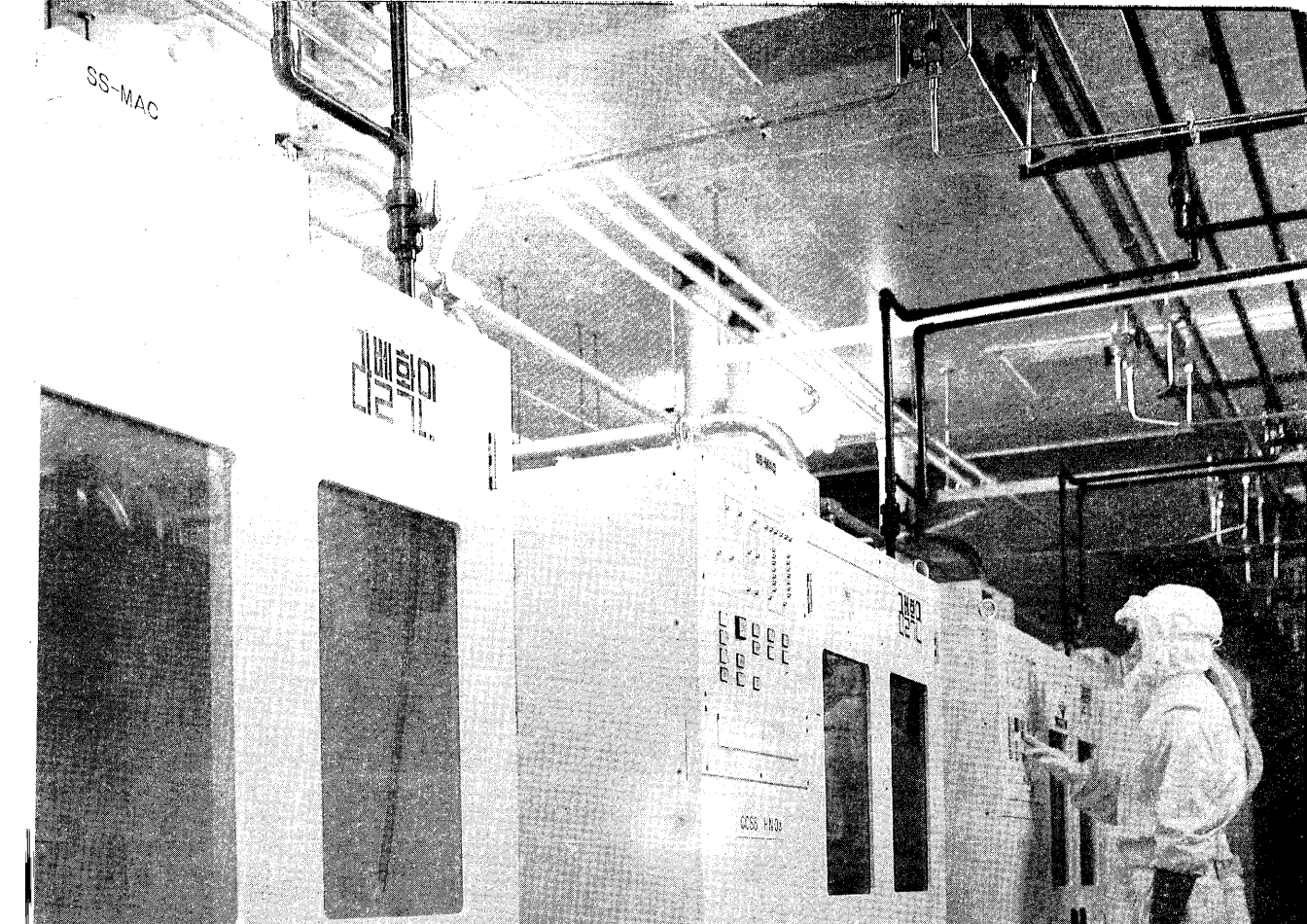
42-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



44-LEAD PLASTIC THIN SMALL OUT LINE PACKAGE (Forward and Reverse Type)

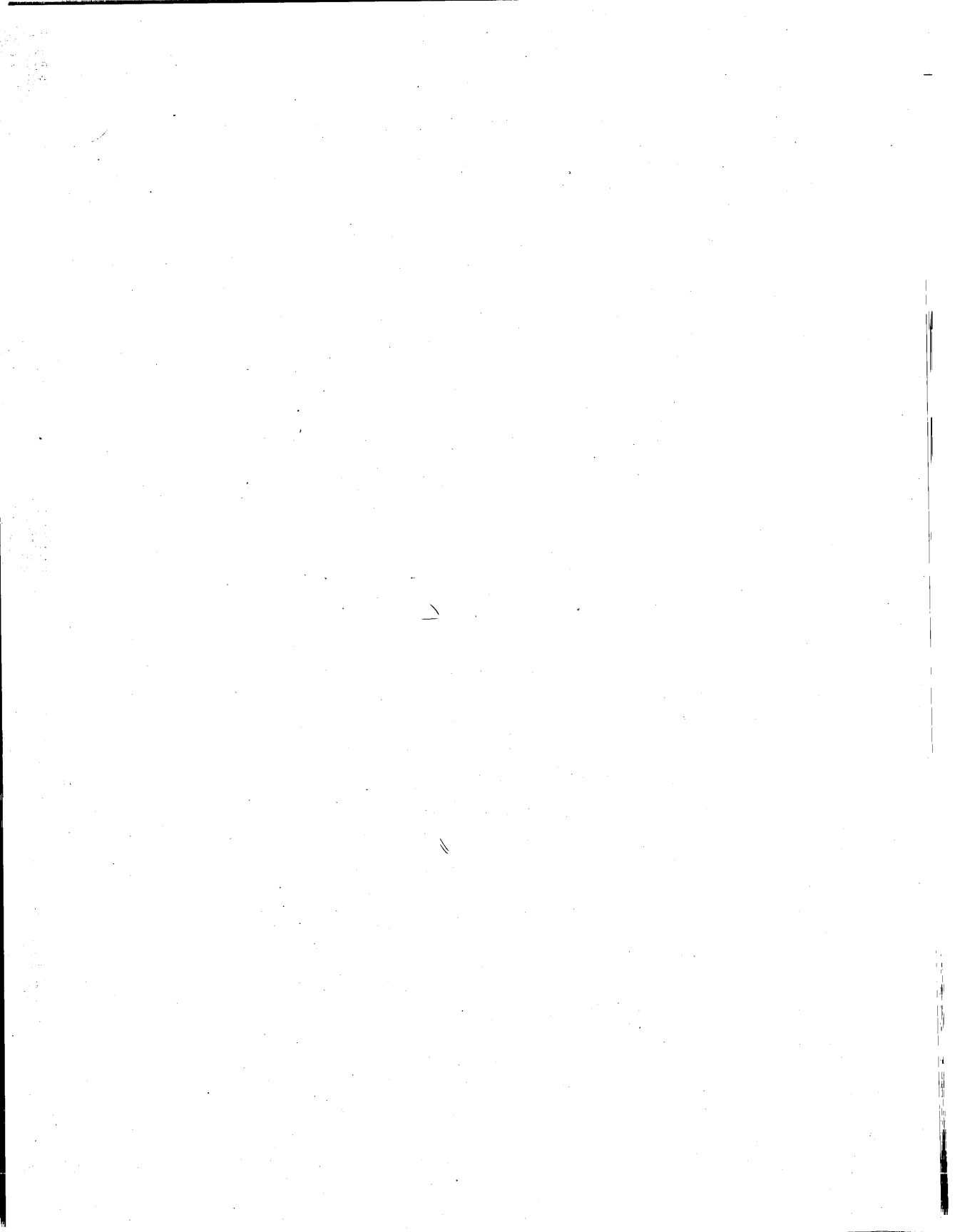




64M DRAM DATA SHEET 7

- 58. KM4090100
- 59. KM4090104
- 60. KM4090108
- 61. KM4090104

SIMTONG
The Best Memory Solution



8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	t _{RAC}	t _{CAC}	t _{RC}
KM48V8000-5	50ns	13ns	90ns
KM48V8000-6	60ns	15ns	110ns
KM48V8000-7	70ns	20ns	130ns

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- 3.3V ± 0.3V power supply
- 8192 cycles/128ms refresh
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages.

GENERAL DESCRIPTION

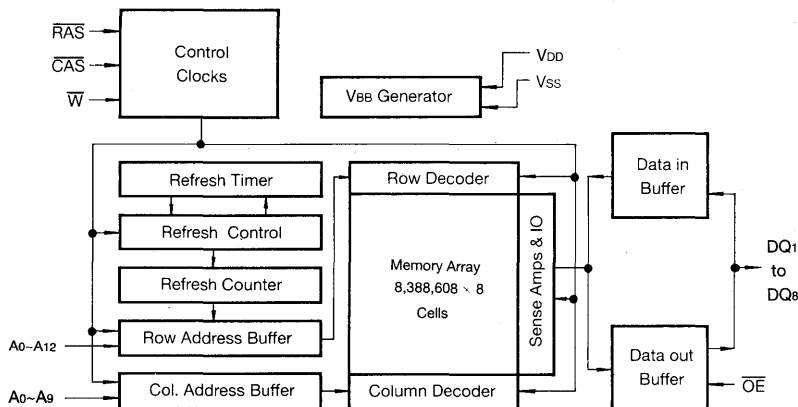
The Samsung KM48V8000 is a high speed CMOS 8, 388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM48V8000 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM48V8000 is fabricated using Samsung's advanced CMOS process

FUNCTIONAL BLOCK DIAGRAM



8M x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• **Performance range:**

	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
KM48V8004-5	50ns	13ns	90ns	20ns
KM48V8004-6	60ns	15ns	110ns	24ns
KM48V8004-7	70ns	20ns	130ns	29ns

- **Fast Page Mode operation with Extended data out**
- **CAS-before-RAS refresh capability**
- **RAS-only and Hidden Refresh capability**
- **Fast parallel test mode capability**
- **TTL compatible inputs and outputs**
- **Early write or output enable controlled write**
- **3.3V ± 0.3V power supply**
- **8192 cycles/128ms refresh**
- **JEDEC standard pinout**
- **Available in plastic SOJ and TSOP(II) packages.**

GENERAL DESCRIPTION

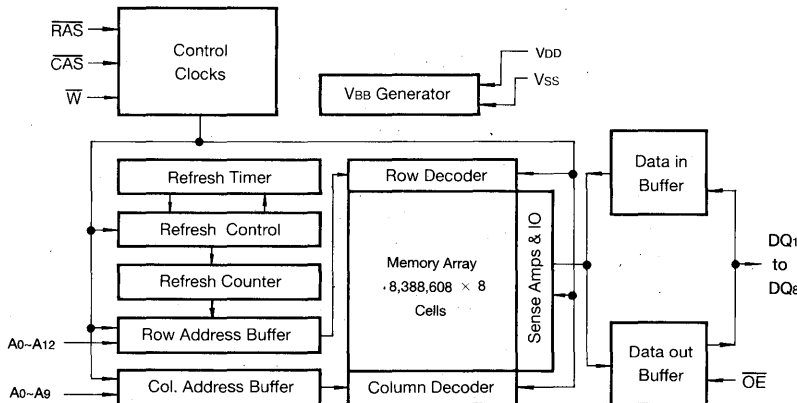
The Samsung KM48V8004 is a high speed CMOS 8, 388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, minicomputers, graphics and high performance portable computers.

The KM48V8004 features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM48V8004 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



8M x 8 Bit CMOS Dynamic RAM with Fast Page Mode

FEATURES

• Performance range:

	trAC	tcAC	trC
KM48V8100-5	50ns	13ns	90ns
KM48V8100-6	60ns	15ns	110ns
KM48V8100-7	70ns	20ns	130ns

- Fast Page Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden Refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- $3.3\text{V} \pm 0.3\text{V}$ power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages.

GENERAL DESCRIPTION

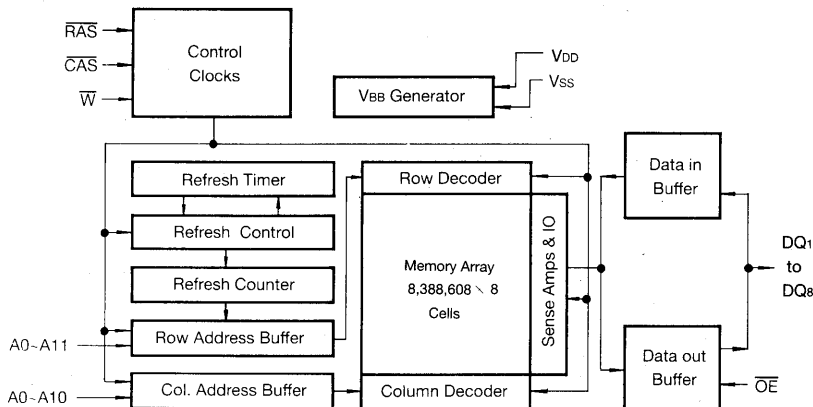
The Samsung KM48V8100 is a high speed CMOS 8, 388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, minicomputers, graphics and high performance portable computers.

The KM48V8100 features Fast Page Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

The KM48V8100 is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



8M x 8 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
KM48V8104-5	50ns	13ns	90ns	20ns
KM48V8104-6	60ns	15ns	110ns	24ns
KM48V8104-7	70ns	20ns	130ns	29ns

- Fast Page Mode operation with Extended data out
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ only and Hidden Refresh capability
- Fast parallel test mode capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- $3.3\text{V} \pm 0.3\text{V}$ power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II) packages.

GENERAL DESCRIPTION

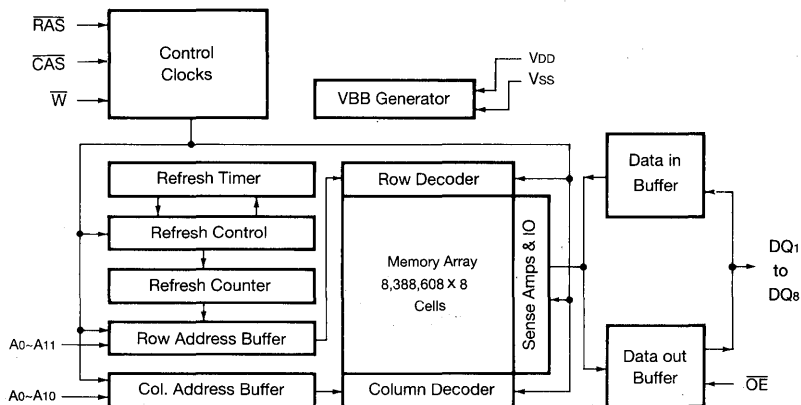
The Samsung KM48V8104 is a high speed CMOS 8, 388,608 bit x 8 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, minicomputers, graphics and high performance portable computers.

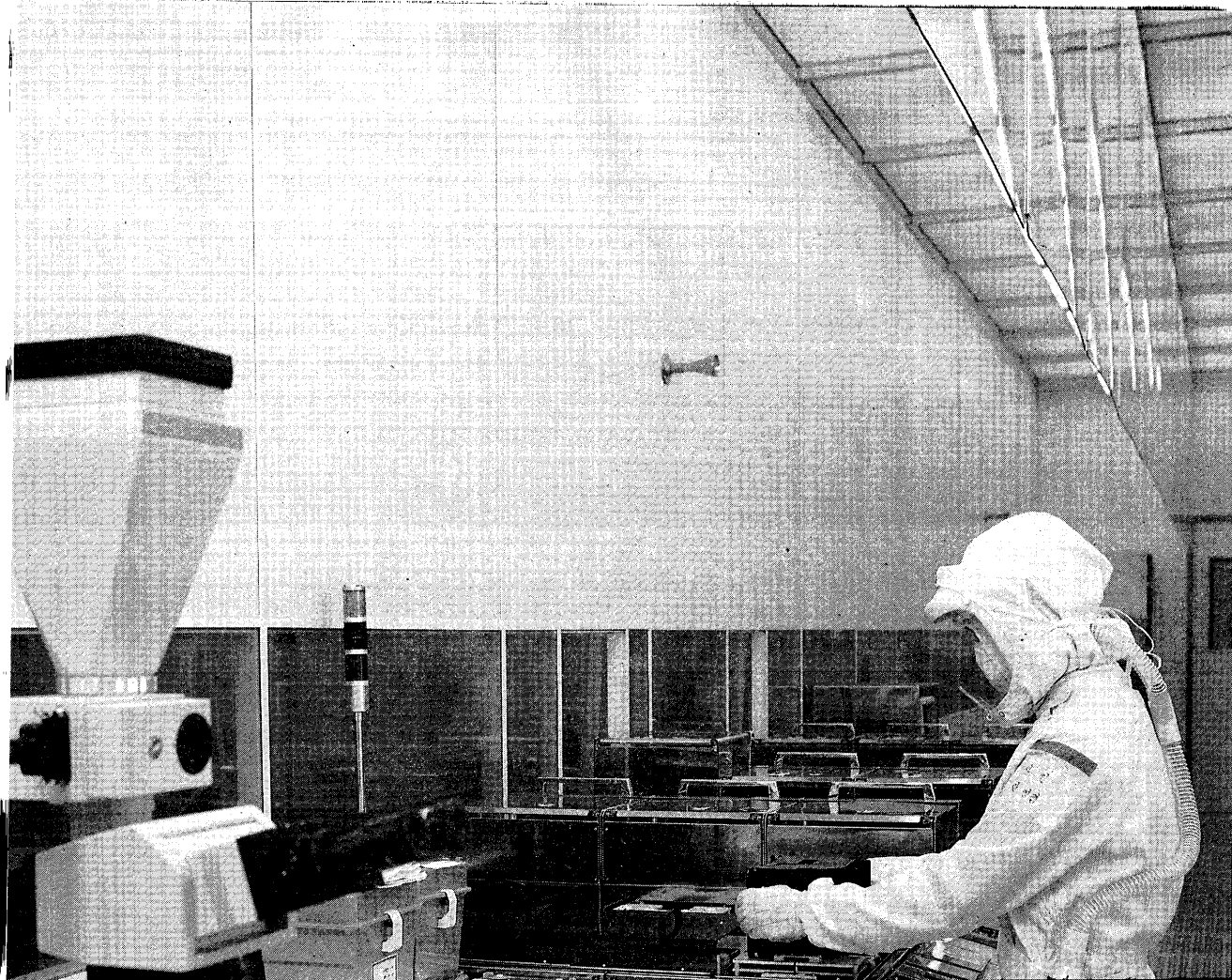
The KM48V8104 features EDO Mode operation which allows high speed random access of memory cells within the same row.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{\text{RAS}}$ -only refresh. All inputs and outputs are fully TTL compatible.

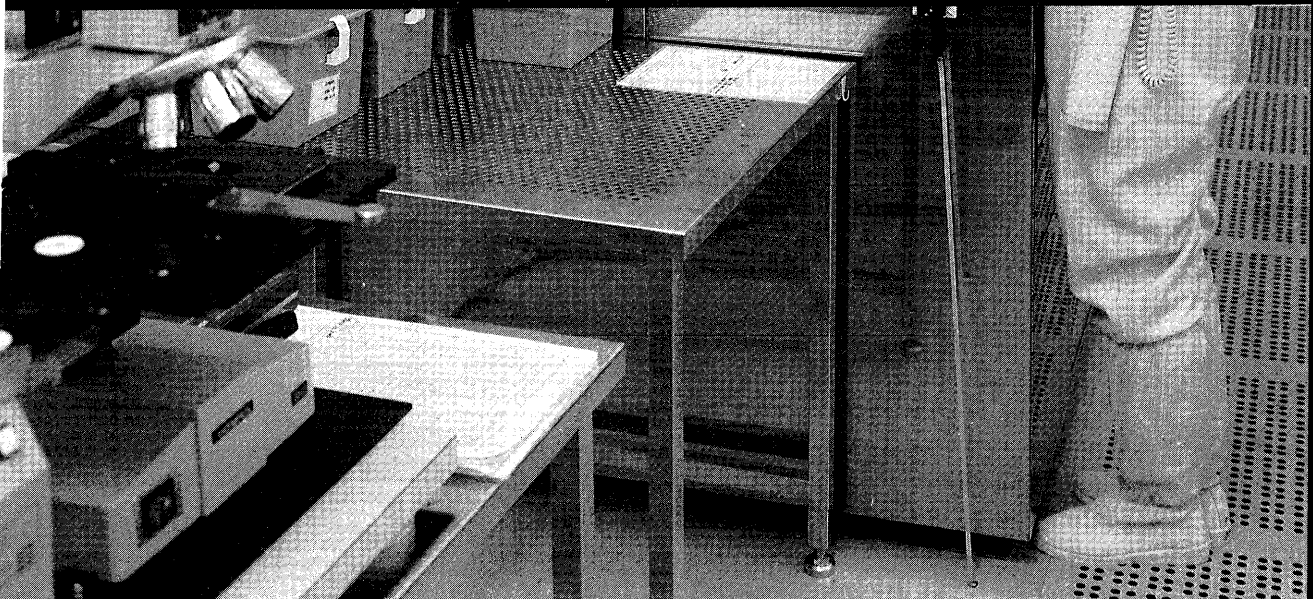
The KM48V8104 is fabricated using Samsung's advanced CMOS process.

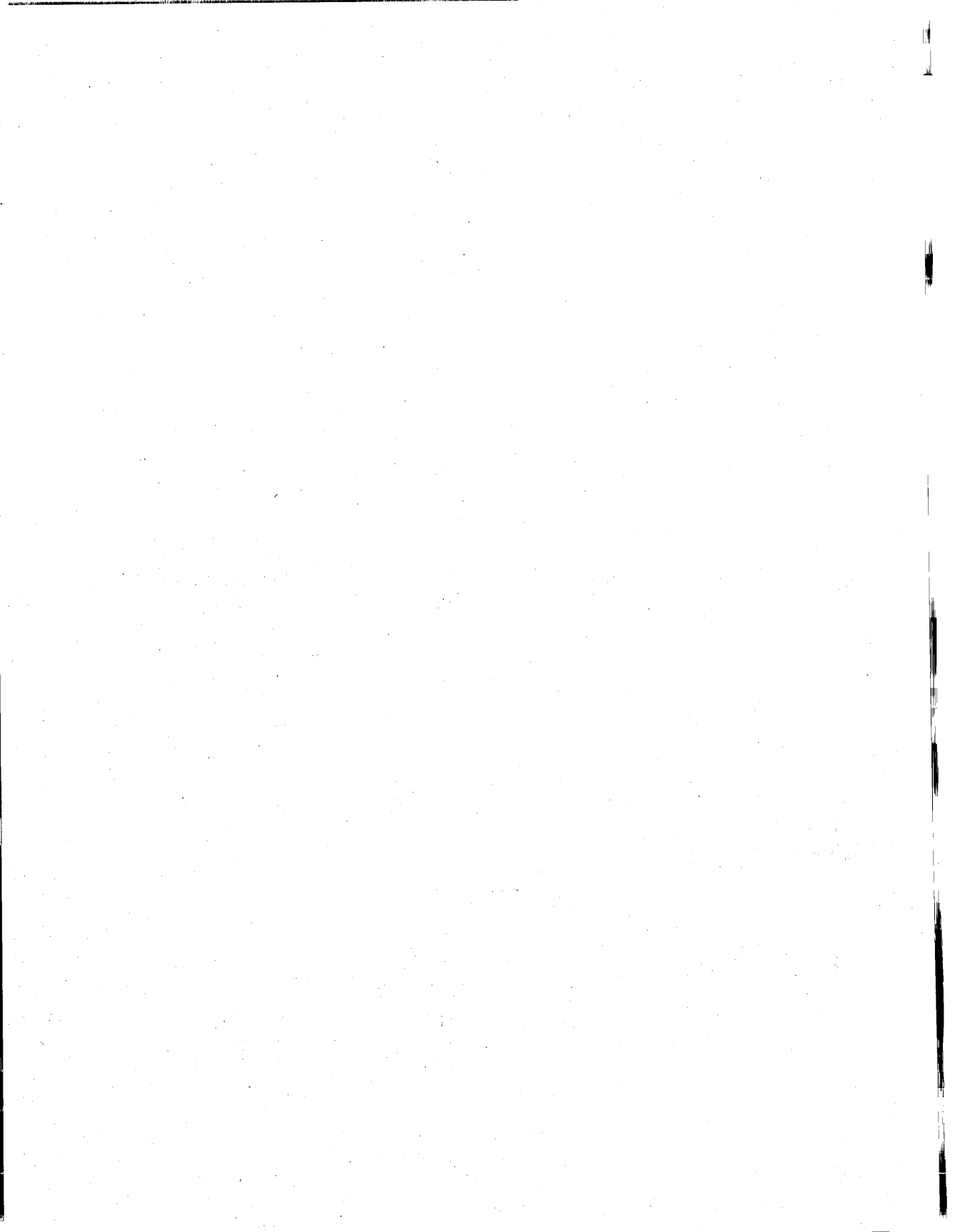
FUNCTIONAL BLOCK DIAGRAM





SALES OFFICES and MANUFACTURER'S REPRESENTATIVES 8





SAMSUNG SEMICONDUCTOR SALES OFFICES-U.S.A.

Northwest

3655 North First Street
San Jose, CA 95134
TEL: (408) 954-7000
FAX: (408) 954-7883

North Central

300 Park Boulevard
Suite 210
Itasca, IL 60143-2636
TEL: (708) 775-1050
FAX: (708) 775-1058

Northeast

119 Russell Street
Littleton, MA 01460
TEL: (508) 486-0700
FAX: (508) 486-8209

Southwest

16253 Laguna Canyon Road
Suite 100
Irvine, CA 92718
TEL: (714) 753-7530
FAX: (714) 753-7544

South Central

15851 Dallas Parkway
Suite 410
Dallas, TX 75248-3307
TEL: (214) 770-7970
FAX: (214) 770-7971

Southeast

802 Greenvalley Road
Suite 204
Greensboro, NC 27408
TEL: (919) 370-1600
FAX: (919) 370-1633

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

ALABAMA

SOUTHERN COMPONENT SALES

307 Clinton Ave. East TEL: (205) 533-6500
Suite 413 FAX: (205) 533-6578
Huntsville, AL 35801

ARIZONA

O'DONNELL ASSOCIATES TEL: (602) 944-9542
2432 W. Peoria Ave. FAX: (602) 861-2615
Suite 1026

Phoenix, AZ 85029
O'DONNELL ASSOCIATES TEL: (602) 797-2047
11449 N. Copper Springs Trail FAX: (602) 797-2047
Tucson, AZ 85737

CALIFORNIA

BESTRONICS TEL: (619) 693-1111
9683 Tierro Granda Street FAX: (619) 693-1963
Suite 102

San Diego, CA 92126
I-SQUARED TEL: (408) 988-3400
3355-1 Scott Blvd. FAX: (408) 988-2079
Suite 102

Santa Clara, CA 95054
WESTAR REP COMPANY TEL: (714) 453-7900
15265 Alton Parkway FAX: (714) 453-7930
Suite 400

Irvine, CA 92718
WESTAR REP COMPANY TEL: (818) 880-0594
26500 Agoura Rd. FAX: (818) 880-5013
Suite 204

Calabasas, CA 91302

CANADA

INTELTECH, INC. TEL: (613) 762-8014
275 Michael Copeland Drive FAX: (613) 253-1370
Kanata, Ontario K2M 2G2

INTELTECH, INC. TEL: (514) 343-4877
3700 Griffith Street FAX: (514) 343-4355
Suite 93

St. Laurent, Quebec H4T 1A7
INTELTECH, INC. TEL: (905) 629-0082
5525 Orbitor Drive FAX: (905) 629-1795
Suite 2

Mississauga, Ontario L4W4Y8

COLORADO

FRONT RANGE MARKETING TEL: (303) 443-4780
3100 Arapahoe Road FAX: (303) 447-0371
Suite 404
Boulder, CO 80303

FLORIDA

B/B TECH SALES TEL: (305) 477-0341
3900 N.W. 79th Avenue FAX: (305) 477-0343
Suite 636

Miami, FL 33166

DYNE-A-MARK TEL: (407) 660-1661
500 Winderley Place FAX: (407) 660-9407
Suite 110

Maitland, FL 32751

DYNE-A-MARK TEL: (305) 485-3500
3355 N.W. 55th Street FAX: (305) 485-6555
Fort Lauderdale, FL 33309

DYNE-A-MARK TEL: (407) 725-7470
742 Penguin Ave., NE FAX: (407) 984-2718
Palm Bay, FL 32905

DYNE-A-MARK TEL: (813) 345-9411
7884 Tent Avenue S FAX: (813) 345-3731
St. Petersburg, FL 33707

GEORGIA

SOUTH ATLANTIC COMPONENT SALES

3300 Holcomb Bridge Road TEL: (404) 447-6154
Suite 210 FAX: (404) 447-6714
Norcross, GA 30092

ILLINOIS

DAVIX INTERNATIONAL LTD. TEL: (708) 259-5300
1655 N. Arlington Heights Rd. FAX: (708) 259-5428
Suite 204East

Arlington Heights, IL 60004

INDIANA

GEN II MARKETING, INC. TEL: (317) 848-3083
31 E. Main Street FAX: (317) 848-1264
Carmel, IN 46032

GEN II MARKETING, INC TEL: (219) 436-4485
1415 Magnavox Way FAX: (219) 436-1977
Suite 130

Ft. Wayne, IN 46804

SAMSUNG

ELECTRONICS

IOWA

ASSOCIATED ELECTRONIC MARKETERS, INC.
4001 Shady Oak TEL: (319) 377-1129
Marion, IA 52302 FAX: (319) 377-1539

KANSAS

ASSOCIATED ELECTRONIC MARKETERS, INC.
8843 Long St. TEL: (913) 888-0022
Lenexa, KS 66215 FAX: (913) 888-4848

KENTUCKY

GEN II MARKETING, INC. TEL: (502) 894-9903
4012 Dupont Circle FAX: (502) 893-2435
Suite 414
Louisville, KY 40207

MASSACHUSETTS

NEW TECH SOLUTIONS, INC. TEL: (617) 229-8888
111 South Bedford Street FAX: (617) 229-1614
Suite 102
Burlington, MA 01803

MICHIGAN

MICROTECH SALES TEL: (313) 459-0200
9357 General Drive FAX: (313) 459-0232
Suite 116
Plymouth, MI 48170

MINNESOTA

GP SALES, INC. TEL: (612) 831-2362
7600 Parklawn FAX: (612) 831-2619
Suite 315
Edina, MN 55435

MISSOURI

ASSOCIATED ELECTRONIC MARKETERS, INC.
11520 St. Charles Rock Rd. TEL: (314) 298-9900
Suite 131 FAX: (314) 298-8660
Bridgeton, MO 63044

NEW YORK

NEPTUNE ELEC. TEL: (516) 349-1600
255 Executive Dr. FAX: (516) 349-1343
Suite 211
Plainview, NY 11803

T-SQUARED TEL: (315) 699-1559
6170 Wynmoor Drive FAX: (315) 699-1705
Cicero, NY 13039

T-SQUARED TEL: (716) 924-9101
7353 Victor-Pittsford Road FAX: (716) 924-4946
Victor, NY 14564

T-SQUARED TEL: (607) 625-3983
1790 Pennsylvania Avenue FAX: (607) 625-5294
Apalachin, NY 13732

NORTH CAROLINA

SOUTH ATLANTIC COMPONENT SALES
5200 Park Road TEL: (704) 525-0510
Suite 103 FAX: (704) 525-9714
Charlotte, NC 28209

SOUTH ATLANTIC COMPONENT SALES
4904 Waters Edge Drive TEL: (919) 859-9970
Suite 268 FAX: (919) 859-9974
Raleigh, NC 27606

OHIO

J.N. BAILEY & ASSOCIATES TEL: (513) 687-1325
129 W. Main Street FAX: (513) 687-2930
New Lebanon, OH 45345

J.N. BAILEY & ASSOCIATES TEL: (614) 262-7274
3591 Milton Avenue FAX: (614) 262-0384
Columbus, OH 43214

J.N. BAILEY & ASSOCIATES TEL: (216) 273-3798
1667 Devonshire Drive FAX: (216) 225-1461
Brunswick, OH 44212

OREGON

ATMI TEL: (503) 643-8307
4900 SW Griffith FAX: (503) 643-4364
Suite 155

Beaverton, OR 97005

PENNSYLVANIA

CMS SALES & MARKETING TEL: (215) 834-6840
527 Plymouth Road FAX: (215) 834-6848
Suite 420

Plymouth Meeting, PA 19462

PUERTO RICO

DIGIT-TECH
P.O. Box 1945 TEL: (809) 892-4260
Calle Cruz #2 FAX: (809) 892-3366

Bajos, San German
Puerto Rico 00753

TEXAS

O'DONNELL ASSOCIATES TEL: (915) 778-2581
5959 Gateway West FAX: (915) 778-6429
Suite 558

El Paso, TX 79925

VIELOCK ASSOCIATES TEL: (214) 881-1940
555 Republic Drive FAX: (214) 423-8556
Suite 105

Plano, TX 75074

VIELOCK ASSOCIATES TEL: (512) 345-8498
9430 Research Blvd. FAX: (512) 346-4037
Echelon Bldg. 2, Suite 330

Austin, TX 78759

VIELOCK ASSOCIATES TEL: (713) 974-3287
10700 Richmond Avenue FAX: (713) 974-3289
Suite 108

Houston, TX 77042

UTAH

FRONT RANGE MARKETING, INC.
488 E. 6400 South TEL: (801) 288-2500
Suite 280 FAX: (801) 288-2505

Murray, UT 84107

WASHINGTON

ATMI TEL: (206) 869-7636
8521 154th Ave., NE FAX: (206) 869-9841
Redmond, WA 98052

WISCONSIN

DAVIX INTERNATIONAL LTD. TEL: (414) 255-1600
N91 W17194 Appleton Avenue FAX: (414) 255-1863
Menomonee Falls, WI 53051

• • • • •

SAMSUNG SEMICONDUCTOR SALES OFFICES-EUROPE

SAMSUNG SEMICONDUCTOR EUROPE GmbH Am Unisyspark 1, 65843 Sulzbach (Germany) TEL: 0049-6196-582-06 FAX: 0049-6196-750-345	MUENCHEN OFFICE Cari-Zeiss-Ring 9 D-85737 Ismaning bei Muenchen TEL: 0049-89-964838 FAX: 0049-89-964873	MILANO OFFICE Viale G. Matteotti, 26 I-20095 Cusano Milanino TEL: 0039-2-66400181 FAX: 0039-2-6192279	LONDON Samsung House 225 Hook Rise South Surbiton Surrey KT6 7LD TEL: 0044-81-3914550 FAX: 0044-81-9742540	BIRMINGHAM OFFICE Florence House St. Mary's Road Hinckley, Leicestershire LE10 1EQ TEL: 0044-455-891111 FAX: 0044-455-612345
PARIS OFFICE Centre d'Affaires La Boursidiere RN 186, Bat. Bourgogne, BP 202 92357 Le Plessis-Robinson TEL: 0033-1-40940700 FAX: 0033-1-40940216	STOCKHOLM OFFICE Bergkaellavaegen 32 P.O. Box 319 S-19130 Sollentuna TEL: 0046-8-6269626 FAX: 0046-8-6268638	BARCELONA OFFICE C. Provenza, 5193-1 E-08025 Barcelona TEL: 0034-3-4-504876 FAX: 0034-3-4-331944	BELGIUM OFFICE Rue de Geneve 10, B3 B-1140 Brussels TEL: 0032-2-2456510 FAX: 0032-2-2456313	

SAMSUNG SEMICONDUCTOR-REPRESENTATIVES

EUROPE

BELGIUM

DANE-LEC BELGIUM

 91-93 Rue J.D. Navez
 B-1210 Bruxelles

 TEL: 0032-2-2167058
 FAX: 0032-2-2166871

DENMARK

EXATEC A/S

 Mileparken 20E
 DK-2740 Skovlunde

 TEL: 0045-44927000
 FAX: 0045-44926020

MIKO KOMPLEMENT AB

 Segersbyvaegen 3
 S-14502 Norsborg

 TEL: 0046-853189080
 FAX: 0046-853175340

FINLAND

TAHINIK OY

 P.O. Box 125
 SF-00241 Helsinki

 TEL: 00358-1482177
 FAX: 00358-1482189

OY FINTRONIC AB

 Pyyntitie 3
 SF-02230 Espoo

 TEL: 00358-0887331
 FAX: 00358-088733342

FRANCE

MEGACHIP

 7 avenue du Canada
 ZA de Courtaboeuf
 91966 LES ULIS Cedex
 FRANCE

 TEL: 0033-1-69290404
 FAX: 0033-1-69290039

SCAIB

 80 Rue d'Arcueil
 Silic 137
 94523 RUNGIS Cedex
 FRANCE

 TEL: 0033-1-46872313
 FAX: 0033-1-45605549

GERMANY

ASTRONIC GmbH

 Gruenwalder Weg 30
 D-82041 Deisenhofen

 TEL: 0049-89-6130303
 FAX: 0049-89-6131668

CANNING ELECTRONIC DISTRIBUTION CED GmbH

 Laatzener Str. 19
 D-30539 Hannover Deleete

 TEL: 0049-511-87640
 FAX: 0049-551-8764160

MSC VERTRIEBS GmbH

 Industrie Str. 16
 D-76297 Stutensee 3

 TEL: 0049-7249-9100
 FAX: 0047-7249-7993

MICRONETICS GmbH

 Dieselstrasse 12
 D-71272 Renningen

 TEL: 0049-7159-92583-0
 FAX: 0049-7159-9258355

SILCOM ELECTRONICS VERTRIEBS GmbH

 Hindenburg Str. 284
 D-41061 Moenchengladbach

 TEL: 0049-2161-15074
 FAX: 0049-2161-183313

ITALY

DEUTSCHE ITT INDUSTRIES GmbH

 Viale Milanofiori E/5
 I-20090 Assago Mi

 TEL: 0039-2-824701
 FAX: 0039-2-8242631/8242831

FANTON COMPONENTS BOLOGNA S.R.L.

 Via O. Simoni, 5
 I-40011 Anzola dell' Emilia

 TEL: 0039-51-735015
 FAX: 0039-51-735013

RAFI ELETTRONICA SPA

 Via Savona 134
 I-20144 Milano

 TEL: 0039-2-48300431
 FAX: 0039-2-428880


SAMSUNG SEMICONDUCTOR REPRESENTATIVES

THE NETHERLANDS

MALCHUS BV HANDELMIJ

Fokkerstraat 511-513
Postbus 48
NI-3125 BD Schiedam

TEL: 0031-10-4277777
FAX: 0031-10-4154867

SPAIN

SEMICONDUCTORS S.A.

Ronda General Mitre
240 Bjs
E-08006 Barcelona

TEL: 0034-3-2172340
FAX: 0034-3-2176598

SWEDEN

MIKO COMPONENTS

Segersbyvaegen 3
P.P. Box 2001
S-14502 Norsborg

TEL : 0046-853-189080
FAX : 0046-853-175340

SWITZERLAND

ELBATEX AG

Hard Str. 72
CH-5430 Wettingen Schweiz

TEL : 0041-56275511
FAX : 0041-56275532

UNITED KINGDOM

MAGNATEC

Coventry Road
Lutterworth
Leicestershire
LE17 4JB

TEL : 0044-455-554711
FAX : 0044-455-552612

ICE ELECTRONICS LTD.

31-32 Stephenson Road
Burrel Road Industrial Estate
St. Ives
Cambridgeshire
PE17 4WJ

TEL : 0044-480-496466
FAX : 0044-480-496621

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

ASIA

HONG KONG

AV. CONCEPT LTD.

Unit 11-15, 11/F1, Block A,
Focal Industrial Centre
21 Man Lok Street, Hungghom,
Kowloon, Hong Kong

TEL : 3347333
FAX : 7643108

PROTECH COMPONENTS LTD.

Unit 2,3/F, Wah Shing Centre,
11 Shing Yip Street,
Kwun Tong, Kowloon,
Hong Kong

TEL : 7930882
FAX : 7930811

WISEWORLD ELECTRONICS LTD.

Room 708, Tower A, 7/F1.,
Hungghom Commercial Centre,
37-39 Ma Tau Wai Road, Hungghom,
Kowloon, Hong Kong

TEL : 7658923
FAX : 3636203

IBDT HK LTD. (CHINA AREA)

Unit 2, 23rd floor,
Westlands Center,
No.20 Westlands Road,
Quarry Bay, Hong Kong

TEL : 565-5898
FAX : 564-5411

SOLARBRITE ELECTRONICS LTD. (CALCULATOR & WATCH)

Unit 1, 11/F, Tower 1, Harbour
Centre, 1, Hok cheung
St, Hungghom, Kowloon,
Hong Kong

TEL : 3633233
FAX : 3633900
TLX : 52543 SECL HX

ATLANTIC COMPONENTS LTD. (MEMORY & PC)

Unit 502, 5/F, Tower III,
Enterprise Square,
9 Sheung Yuet Road, Kowloon Bay,
Kowloon, Hong Kong

TEL : 7991996
FAX : 7559452

LISENG & CO. (4BIT/8BIT ONE CHIP SOFTWARE HOUSE)

Fiat B&C, 6/F, Four Seas
Communication Bank Bldg,
49-51 Bonham Strand
West, Hong Kong

TEL : 5431338
FAX : 5442602

SOLARI COMPUTER ENGINEERING LTD. (4 BIT/8BIT ONE CHIP SOFTWARE HOUSE)

Roon 2018-2025, Tower 1,
Metroplaza, Kwai Fong,
N.T., Hong Kong

TEL : 418-0988
FAX : 418-0887

DATAWORLD INTERNATIONAL LTD. (MIYUKI ELECTRONICS (HK) LTD.) (ASIC DESIGN HOUSE)

Fiat No. 3-4,5/F1.,
Yuen Shing Ind. Bldg.,
1033, Yee Kuk Street, West,
Kowloon, Hong Kong

TEL : 7862611
FAX : 7856213
TLX : 45876 MYK HX

SYNTHESIS SYSTEMS DESIGN, LTD. (ASIC DESIGN HOUSE)

Unit 4,12/F Chai Wan Ind. City,
Phase 2, No. 70, Wing Tai Road,
Chai Wan, Hong Kong

TEL : 557-1102
FAX : 889-2962

TAIWAN

YOSUN INDUSTRIAL CORP.

7F, No. 76, Sec. 1,
Cheng Kung Rd. Nan Kang,
Taipei, R.O.C.

TEL : (02)788-1991
FAX : (02)788-1996

SANT SONG CORP.

4F, No.12, Lane 94, Tsao
Ti Wei, Shen Keng Hsiang,
Taipei Hsien, Taiwan, R.O.C.

TEL : (02) 662-7829
FAX : (02) 662-0781

SUPREME ELECTRONICS CO., LTD.

18Fl., No.67, Section 2,
Tun hwa S. Road,
Taipei, Taiwan, R.O.C.

TEL : (02) 7023258/7023278
FAX : (02) 7063196

JAPAN

TOMEN ELECTRONICS CORP.

1-1 Uchisaiwa-Cho 2 Chome
Chiyoda-Ku Tokyo, 100 Japan

TEL : (03) 3506-3654
FAX : (03) 3506-3497

RIKEI

Nichimen Bldg.,
2-2 Nakanojima 2 Chome,
Kita-Ku, Osaka, 530 Japan

TEL : (06) 201-2081
FAX : (06) 222-1185

ISECO

26-3, Kitamagome 2 Chome,
Ota-Ku, Tokyo, 143, Japan

TEL : (03) 3777-3611
FAX : (03) 3777-3614

ADO

7F Sasage Bldg.,
4-6 Sotokanda 2 Chome
Chiyoda-Ku Tokyo, 101 Japan

TEL : (03) 3257-2600
FAX : (03) 3251-9705

MARUBUN

8-1 Nihombashi-Odenma-Cho
Chuo-Ku Tokyo, 103 Japan

TEL : (03) 3639-9897
FAX : (03) 3661-7433

SAMSUNG JAPAN

17F, Hamacho Center BLDG.
2-31-1, Nihonbashi-Hamacho
Chuo-ku, TOKYO 103 JAPAN

TEL : (03) 5641-9651
FAX : (03) 5641-9713

SAMSUNG SEMICONDUCTOR REPRESENTATIVES

SINGAPORE

ASTINA ELECTRONIC(S) PTE LTD.

203, Henderson Road TEL: 65-2769997
#12-08 Henderson Industrial Park, FAX: 65-2769996
Singapore 0315

BOSTEX ELECTRONICS PTE LTD.

No.221 Henderson Road TEL: 2765130
#04-06 Henderson Building FAX: 2765132
Singapore 0315

SAMSUNG (THAILAND) CO., LTD.

15th Fl. Sathorn Thani Bldg., TEL: 662-2367642-5
92/40-41 North Sathorn Road FAX: 662-2368049
Bankok 10500, Thailand

SOUTH-WEST ELECTRONICS PTE LTD.

30 Kallang Pudding Road, TEL: 7431813
#04-04 Valiant Industrial Bldg., FAX: 7471128
Singapore 1334

SYARIKAT SAMSUNG ELECTRONICS(S) PTE LTD.

Suite 9-2, Menara Penang TEL: 229-1670-1
Garden 42A, Jalan Suitoan FAX: 229-1678
Ahmad Shah 10050 Penang,
Malaysia

VUTIPONG ELECTRONIC CO., LTD.

51-53 Pahurat Rd, (Banmoh) TEL: 662-2266496-9
Bankok 10200, Thailand FAX: 662-2240861

YIC SINGAPORE PTE, LTD.

623, Aljunied Road, #06-08 TEL: 65-7490677
Aljunied Industrial Complex, FAX: 65-7477019
Singapore, 1438

SAMSUNG SINGAPORE PTE, LTD.

4, SHENTON WAY, #18-01/10 TEL: 65-5352808
Shingwan House, FAX: 65-2772792
Singapore 0106

WESTECH ELECTRONICS CO., LTD.

77/113, Ladprao SOI 3, TEL: 662-512-2751
Ladyao, Jatujak, Bangkok FAX: 662-512-5531
10900, Thailand

INDIA

COMPONENTS AND SYSTEMS MARKETING ASSOCIATES (INDIA) PVT. LTD.

100, Dadasaheb Phalke Road, TEL: 4114585
Dadar, Bombay 400 FAX: 4112546
014 TLX: 001-4605 PDT IN

TURKEY

ELEKTRO SAN. VE TIC. KOLL STI.

Hasanpasa, Ahmet Rasim TEL: 337-2245
Sok No. 16 Kadikoy Istanbul, FAX: 336-8814
Turkey TLX: 29569 elts tr

CHINA

IBDT(HK) LTD. (SHANGHAI LIAISON OFFICE)

Rm 501, TEL: (021) 4316170
750 Zhao Jia Bang Rang Road, FAX: (021) 4316170
Shanghai, China

KOREA

NAEWAE SEMICONDUCTOR CO., LTD.

Bangbae Center Bldg., TEL: (02)595-1010
875-5, Bangbae-4dong, FAX: (02)595-7888
Seocho-ku, Seoul, Korea

SAMSUNG LIGHT-ELECTRONICS CO., LTD.

4th Fl. Room 2-3, TEL: 718-0045
Electronics Main Bldg., 718-9531-5
16-9, Hankangro-3ka, FAX: 718-9536
Yongsan-ku, Seoul, Korea

NEWCASTLE SEMICONDUCTOR CO., LTD.

4th Fl. Room 410-411, TEL: 718-8531-4
Electronics Main Bldg., FAX: 718-8535
16-9, Hankangro-3ka,
Yongsan-ku, Seoul, Korea

HANKOOK SEMICONDUCTOR & TELECOMMUNICATION CO., LTD.

#302, Monami Bldg., 125-20, TEL: (02)542-4123
Chungdam-dong, Kangnam-ku, FAX: (02)542-2454
Seoul, Korea

SEGYUNG INTERISE CORP.

Dansan Bldg., 301, 7-44 TEL: (02)469-3511
Hwayang-dong, Sungdong-ku, FAX: (02)469-7966
Seoul, Korea

SEGYUNG ELECTRONICS

182-2, Jangsa-dong, TEL: (02)273-6781
Jongro-ku, Seoul, Korea FAX: (02)275-9448
TLX: K24950 SUKSEMT

SAMTEK

3/4 FL. Chungju Bldg., TEL: (02)538-4400
156-16, Samsung-dong, FAX: (02)538-4338-9
Kangnam-ku, Seoul, Korea

SUNIN TRADING CO., LTD.

Sunin Bldg., 7Fl., 16-8, TEL: (02)702-1257-8
Hankangro-2ka, Yongsan-ku, FAX: (02)704-0997
Seoul, Korea