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Technology, Incorporated

Data Book ....

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SEEQ Technology Product Selection Guide

4K EEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	F	
2804A	512 x 8	250	80	40	C,E,M	●	●				1-19
2804A	512 x 8	300	80	40	C,E,M	●	●				1-19
2804A	512 x 8	350	80	40	C,E,M	●	●				1-19

16K EEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	F	
52B13	2K x 8	200	80	30	C	●	●				1-3
52B13	2K x 8	250	80	30	C, E, M	●	●				1-3, 6-7
52B13	2K x 8	300	80	30	M	●	●				1-3, 6-7
52B13	2K x 8	350	80	30	C, E	●	●				1-3, 6-7
2816A	2K x 8	200	110	40	C	●	●				1-25
2816A	2K x 8	250	110	40	C, E, M	●	●				1-25, 6-21
2816A	2K x 8	300	110	40	C, E, M	●	●				1-25, 6-21
2816A	2K x 8	350	110	40	C	●	●				1-25
5516A	2K x 8	200	110	40	C		●				1-25
5516A	2K x 8	250	110	40	C		●				1-25
5516A	2K x 8	300	110	40	C		●				1-25
2817A	2K x 8	200	110	40	C	●	●				1-31
2817A	2K x 8	250	110	40	C, E, M	●	●				1-31, 6-27
2817A	2K x 8	300	110	40	C, E, M	●	●				1-31, 6-27
2817A	2K x 8	350	110	40	C	●	●				1-31
5517A	2K x 8	250	110	40	C		●				1-31
5517A	2K x 8	300	110	40	C		●				1-31

TEMPERATURE RANGE

C = Commercial 0°C to +70°C
E = Extended -40°C to +85°C
M = Military -55°C to +125°C

TBD = To Be Determined

*Commercial Temperature Range

PACKAGE

P = Plastic Dip
D = Ceramic Dip
N = Plastic Leaded Chip Carrier
L = Ceramic Leadless Chip Carrier
F = Flat Pack
M = Module

64K EEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*) ACTIVE	STANDBY	TEMP RANGE	PACKAGE P	D	N	L	F	DATA SHEET PAGE #
52B33	8K x 8	200	110	40	C	●	●				1-11
52B33	8K x 8	250	110	40	C, E, M	●	●		●		1-11, 6-15
52B33	8K x 8	300	110	40	C, E, M	●	●		●		1-11, 6-15
52B33	8K x 8	350	110	40	C	●	●				1-11
2864	8K x 8	250	110	40	C, E, M	●	●	●	●	●	1-37, 6-33
2864	8K x 8	300	110	40	C, E, M	●	●	●	●	●	1-37, 6-33
2864	8K x 8	350	110	40	C, E, M	●	●	●	●	●	1-37, 6-33
28C64	8K x 8	200	50	.150	C, E, M	●	●	●	●		1-43, 6-39
28C64	8K x 8	250	50	.150	C, E, M	●	●	●	●		1-43, 6-39
28C64	8K x 8	300	50	.150	C, E, M	●	●	●	●		1-43, 6-39
28C64	8K x 8	350	50	.150	C, E, M	●	●	●	●		1-43, 6-39
28C65	8K x 8	200	50	.150	C, E, M	●	●	●	●		1-51, 6-46
28C65	8K x 8	250	50	.150	C, E, M	●	●	●	●		1-51, 6-46
28C65	8K x 8	300	50	.150	C, E, M	●	●	●	●		1-51, 6-46
28C65	8K x 8	350	50	.150	C, E, M	●	●	●	●		1-51, 6-46

256K EEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*) ACTIVE	STANDBY	TEMP RANGE	PACKAGE P	D	N	L	F	DATA SHEET PAGE #
28C256	32K x 8	200	60	.150	C, E, M	●	●	●	●	●	1-59, 6-55
28C256	32K x 8	250	60	.150	C, E, M	●	●	●	●	●	1-59, 6-55
28C256	32K x 8	300	60	.150	C, E, M	●	●	●	●	●	1-59, 6-55
28C256	32K x 8	350	60	.150	C, E, M	●	●	●	●	●	1-59, 6-55

1024K EEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*) ACTIVE	STANDBY	TEMP RANGE	PACKAGE M	P	D	N	L	F	DATA SHEET PAGE #
M28C010	128K x 8	250	70	2	C, E, M	●						1-85, 6-75
M28C010	128K x 8	300	70	2	C, E, M	●						1-85, 6-75
M28C010	128K x 8	350	70	2	C, E, M	●						1-85, 6-75

TEMPERATURE RANGE

C = Commercial 0°C to +70°C
E = Extended −40°C to +85°C
M = Military −55°C to +125°C

TBD = To Be Determined

*Commercial Temperature Range

PACKAGE

P = Plastic Dip
D = Ceramic Dip
N = Plastic Leaded Chip Carrier
L = Ceramic Leadless Chip Carrier
F = Flat Pack
M = Module

FLASH™ EEPROMS

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	F	
48F512	64K x 8	200	60	.100	C	●	●	●			2-1
48F512	64K x 8	250	60	.100	C, E, M	●	●	●	●		2-1, 6-111
48F512	64K x 8	300	60	.100	C, E, M	●	●	●	●		2-1, 6-111
48F010	128K x 8	200	60	.100	C	●	●	●			2-13
48F010	128K x 8	250	60	.100	C, E, M	●	●	●	●		2-13, 6-123
48F010	128K x 8	300	60	.100	C, E, M	●	●	●	●		2-13, 6-123
27F010	128K x 8	200	60	.100	C	●	●	●			2-25
27F010	128K x 8	250	60	.100	C	●	●	●			2-25
27F010	128K x 8	300	60	.100	C	●	●	●			2-25
KT48	FLASH PROGRAMMING KIT										2-37

HIGH SPEED 16K EEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	F	
36C16	2K x 8	35	80	–	C	●	●				1-71
36C16	2K x 8	40	80	–	C	●	●				1-71
36C16	2K x 8	45	80	–	C, E, M	●	●		●		1-71, 6-63
36C16	2K x 8	55	80	–	C, E, M	●	●		●		1-71, 6-63
36C16	2K x 8	70	80	–	E, M		●		●		6-63
38C16	2K x 8	35	80	40	C	●	●	●			1-77
38C16	2K x 8	40	80	40	C	●	●	●			1-77
38C16	2K x 8	45	80	40	C, E, M	●	●	●	●		1-77, 6-69
38C16	2K x 8	55	80	40	C, E, M	●	●	●	●		1-77, 6-69
38C16	2K x 8	70	80	40	E, M		●		●		6-69

HIGH SPEED 32K EEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	F	
36C32	4K x 8	35	80	–	C	●	●				1-71
36C32	4K x 8	40	80	–	C	●	●				1-71
36C32	4K x 8	45	80	–	C, E, M	●	●		●		1-71, 6-63
36C32	4K x 8	55	80	–	C, E, M	●	●		●		1-71, 6-63
36C32	4K x 8	70	80	–	E, M		●		●		6-63
38C32	4K x 8	35	80	40	C	●	●	●			1-77
38C32	4K x 8	40	80	40	C	●	●	●			1-77
38C32	4K x 8	45	80	40	C, E, M	●	●	●	●		1-77, 6-69
38C32	4K x 8	55	80	40	C, E, M	●	●	●	●		1-77, 6-69
38C32	4K x 8	70	80	40	E, M	●	●	●	●		6-69

FLASH is a trademark of SEEQ Technology Inc.

64K/128K/256K UVEPROMs

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	F	
2764	8K x 8	160	100	30	C		●				3-1
2764	8K x 8	200	100	30	C, E, M		●				3-1, 6-83
2764	8K x 8	250	100	30	C, E, M		●				3-1, 6-83
2764	8K x 8	300	100	30	C		●				3-1
2764	8K x 8	350	100	30	E, M		●				6-83
2764	8K x 8	450	100	30	C, E, M		●				3-1, 6-83
27128	16K x 8	200	100	30	C, E, M		●		●		3-1, 6-83
27128	16K x 8	250	100	30	C, E, M		●		●		3-1, 6-83
27128	16K x 8	300	100	30	C		●				3-1
27128	16K x 8	350	100	30	E, M		●		●		6-83
27128	16K x 8	450	100	30	C, E, M		●		●		3-1, 6-83
27C256	32K x 8	200	50	.150	C, E, M		●		●		3-9, 6-91
27C256	32K x 8	250	50	.150	C, E, M		●		●		3-9, 6-91
27C256	32K x 8	300	50	.150	C, E, M		●		●		3-9, 6-91
27C256	32K x 8	450	50	.150	C		●				3-9

DESC-COMPLIANT UVEPROMS

PART NUMBER	ORGANIZATION	ACCESS TIME (ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	F	
82005	8K x 8	200	100	30	M		●				6-99
82005	8K x 8	250	100	30	M		●				6-99
82005	8K x 8	450	100	30	M		●				6-99
82025	16K x 8	200	100	30	M		●		●		6-103
82025	16K x 8	250	100	30	M		●		●		6-103
82025	16K x 8	300	100	30	M		●		●		6-103
82025	16K x 8	450	100	30	M		●		●		6-103
86063	32K x 8	200	50	.150	M		●		●		6-107
86063	32K x 8	250	50	.150	M		●		●		6-107
86063	32K x 8	300	50	.150	M		●		●		6-107

COMMUNICATION PRODUCTs

PART NUMBER	ICC MAX. ACTIVE (mA*)	TEMP RANGE	PACKAGE					FUNCTION	DATA SHEET PAGE #
			P	D	N	L	F		
8003	200	C	●	●				Ethernet Data Link Controller	4-1
8020	75	C	●	●	●			10 MHz Manchester Encoder/Decoder	4-13
8023A	75	C	●	●	●			10 MHz Manchester Encoder/Decoder	4-27
8005	350	C			●			Advanced Ethernet Data Link Controller	4-43

CMOS EEPLDs

PART NUMBER	DESCRIPTION	PINS	SPEED t_{PD} (ns)	ICC MAX. (mA*) ACTIVE	ICC MAX. (mA*) STANDBY	TEMP RANGE	PACKAGE P	PACKAGE D	PACKAGE N	PACKAGE L	PACKAGE F	DATA SHEET PAGE #
20RA10Z-35	Asynchronous	24	35	25**	.150	C***	●	●	●	●		5-1
20RA10Z-40	Asynchronous	24	40	25**	.150	C,*** E, M	●	●	●	●		5-1
20RA10Z-45	Asynchronous	24	45	25**	.150	C,*** E, M	●	●	●	●		5-1

TEMPERATURE RANGE

C = Commercial 0°C to +70°C
E = Extended −40°C to +85°C
M = Military −55°C to +125°C

TBD = To Be Determined

*Commercial Temperature Range
**f = 1 MHz; 5mA/Additional MHz
***Commercial 0°C to 75°C

PACKAGE

P = Plastic Dip
D = Ceramic Dip
N = Plastic Leaded Chip Carrier
L = Ceramic Leadless Chip Carrier
F = Flat Pack
M = Module

1 EEPROMS

(Electrically Erasable Programmable Read Only Memories)

SEEQ Technology
EEPROM Alternate Source

MFG.	Part No.	Description	SEEQ Part No.
A.M.D.	2817A	2K X 8 EEPROM	2817A
A.M.D.	9864	8K X 8 EEPROM	2864
A.M.D.	2864B	8K X 8 EEPROM	28C64
ATMEL	28C64	8K X 8 EEPROM	28C64
EXEL	2804A	512 X 8 EEPROM	2804A
EXEL	46C16-55	2K X 8 EEPROM	36C16-55
EXEL	2816A	2K X 8 EEPROM	2816A
EXEL	2864	8K X 8 EEPROM	28C64
EXEL	2865	8K X 8 EEPROM	28C65
FUJITSU	28C64	8K X 8 EEPROM	28C64
FUJITSU	28C65	8K X 8 EEPROM	28C65
G.I.	28C64	8K X 8 EEPROM	28C64
HITACHI	58064	8K X 8 EEPROM	52B33
INTEL	2816	2K X 8 EEPROM	52B13
INTEL	2816A	2K X 8 EEPROM	52B13
INTEL	2817A	2K X 8 EEPROM	2817A
NATIONAL	9816A	2K X 8 EEPROM	2816A
NATIONAL	9817A	2K X 8 EEPROM	2817A
SAMSUNG	2816A	2K X 8 EEPROM	2816A
SAMSUNG	2817A	2K X 8 EEPROM	2817A
XICOR	2616	2K X 8 EEPROM	36C16-45
XICOR	2816H	2K X 8 EEPROM	38C16-45
XICOR	2804A	512 X 8 EEPROM	2804A
XICOR	2816A	2K X 8 EEPROM	2816A
XICOR	2864A	8K X 8 EEPROM	28C64
XICOR	2864B	8K X 8 EEPROM	28C64
XICOR	28256	32K X 8 EEPROM	28C256

SEEQ Technology
PROM Replacement Chart

MFG.	Part No.	Description	SEEQ Part No.
A.M.D.	AM27PS291DC	2K X 8 PROM	36C16-45
A.M.D.	AM27PS291DM	2K X 8 PROM	36C16-55
A.M.D.	AM27PS291ADM	2K X 8 PROM	36C16-55
A.M.D.	AM27S291ADC	2K X 8 PROM	36C16-35
CYPRESS	CY7C291-35	2K X 8 PROM	36C16-35
CYPRESS	CY7C291-50	2K X 8 PROM	36C16-45
FUJITSU	MB7138Y-SKZ	2K X 8 PROM	36C16-35
FUJITSU	MB7138H-SKZ	2K X 8 PROM	36C16-45
FUJITSU	MB7138E-WZ	2K X 8 PROM	36C16-45
HARRIS	6-76161	2K X 8 PROM	36C16-45
M.M.I.	63S1681NS	2K X 8 PROM	36C16-45
M.M.I.	63S1681ANS	2K X 8 PROM	36C16-35
NATIONAL	DM77S291	2K X 8 PROM	36C16-55
NATIONAL	DM87S291	2K X 8 PROM	36C16-55
RAYTHEON	29681ASM	2K X 8 PROM	36C16-55
RAYTHEON	29681ASC	2K X 8 PROM	36C16-55
RAYTHEON	29681SC	2K X 8 PROM	36C16-55
RAYTHEON	29683ASC	2K X 8 PROM	36C16-45
RAYTHEON	29683ASM	2K X 8 PROM	36C16-55
SIGNETICS	82S291	2K X 8 PROM	36C16-45
T.I.	27C291-35	2K X 8 PROM	36C16-45
T.I.	27C291-50	2K X 8 PROM	36C16-45
T.I.	TBP28S166N	2K X 8 PROM	36C16-45
WAFRSCAL	57C291-40	2K X 8 PROM	36C16-35
WAFRSCAL	57C291-55	2K X 8 PROM	36C16-55
NATIONAL	DM87S421	4K X 8 PROM	36C32-55
NATIONAL	DM87S421A	4K X 8 PROM	36C32-45
NATIONAL	DM77S421	4K X 8 PROM	36C32-55
NATIONAL	DM77S421A	4K X 8 PROM	36C32-55
RAYTHEON	29671ASC	4K X 8 PROM	36C32-45
RAYTHEON	29671ASM	4K X 8 PROM	36C32-55
RAYTHEON	29673SC	4K X 8 PROM	36C32-55
RAYTHEON	29673SM	4K X 8 PROM	36C32-55

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52B13/52B13H

16K Electrically Erasable PROM

October 1988

Features

- **Input Latches**
- **TTL Byte Erase/Byte Write**
- **1 ms (52B13H) or 9 ms Byte Erase/Byte Write**
- **Power Up/Down Protection**
- **10,000 Erase/Write Cycles per Byte Minimum**
- **5V ± 10% Operation**
- **Fast Read Access Time — 200 ns**
- **Infinite Number of Read Cycles**
- **Chip Erase and Byte Erase**
- **DiTrace™**
- **JEDEC Approved Byte Wide Memory Pinout**
- **Military And Extended Temperature Range Available**
- **Direct Replacement For Intel 2816/2816A**

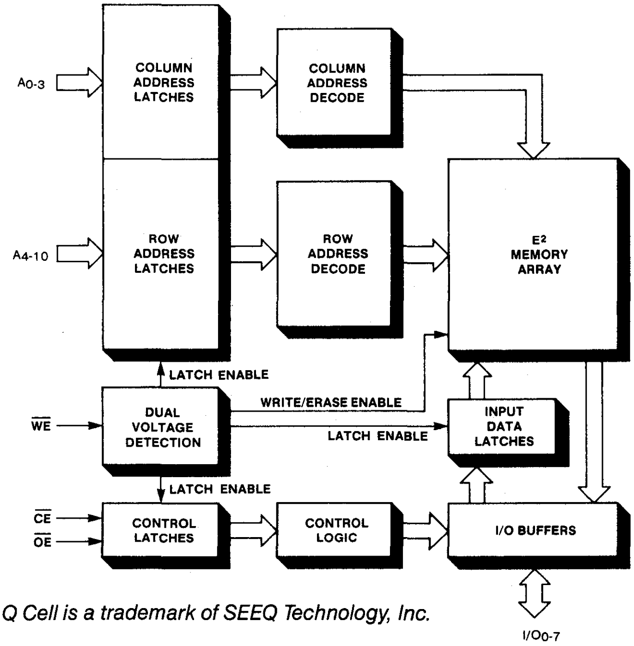
Description

SEEQ's 52B13 and 52B13H are 2048 x 8 bit, 5 volt electrically erasable programmable read only memories (EEPROM) with input latches on all address, data and control (chip and output enable) lines. Data is latched and electically written by either a TTL or a 21V pulse on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written a minimum of 10,000 times. They are direct pin-for-pin replacement for SEEQ's 5213 and Intel 2816/2816A.

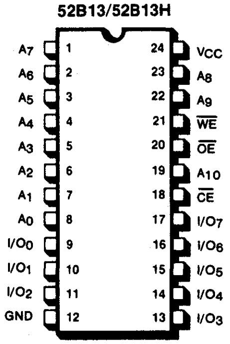
The 52B13 and 52B13H are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications for the 52B13 and 52B13H will be found in military avionics systems, programmable character generators, self-calibrating instruments/

(continued on next page)

Block Diagram



Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
$I/O_{0\text{-}7}$	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

machines, programmable industrial controllers, and an assortment of other systems. Designing the 52B13 and 52B13H into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance. Extended temperature and military grade versions are available.

Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is at TTL high, and TTL highs (logical 1s) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation EEPROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detection circuit which allows either a TTL low or 21V signal to be applied to $\overline{\text{WE}}$ to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of $\overline{\text{WE}}$.

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10 ms.

A characteristic of all EEPROMs is that the total number of write and erase cycle is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{\text{WE}}$, enabling the chip, and enabling the outputs. Data is available t_{CE} time after Chip Enable is applied or t_{AA} time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

DiTrace®

SEEQ's family of EEPROMs incorporate a DiTrace field. The DiTrace feature is a method for storing production flow information to wafer level in an extra column of EEPROM cells. As each major manufacturing operation is performed the DiTrace field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

DiTrace is a registered trademark of SEEQ Technology, Inc.

Table 1. Mode Selection ($V_{CC} = 5V \pm 10\%$)

Mode \ PIN	$\overline{\text{CE}}$ (18)	$\overline{\text{OE}}$ (20)	$\overline{\text{WE}}$ (21)	I/O (9-11, 13-17)
Read[1]	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby[1]	V_{IH}	Don't Care	V_{IH}	High Z
Byte Erase[2]	V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase[2]	V_{IL}	V_{OE}	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	High Z

NOTES:
1. $\overline{\text{WE}}$ may be from V_{IH} to 6V in the read and standby mode.
2. $\overline{\text{We}}$ may be at V_{IL} (TTL $\overline{\text{WE}}$ Mode) or from 15 to 21V (High Voltage $\overline{\text{WE}}$ Mode) in the byte erase, byte write, or chip erase mode of the 52B13/52B13H.

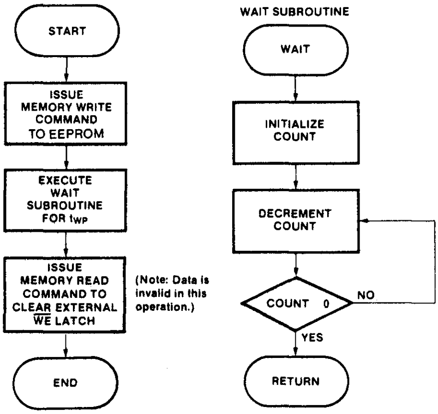
Power Up/Down Considerations

SEEQ's "52B" E^2 family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

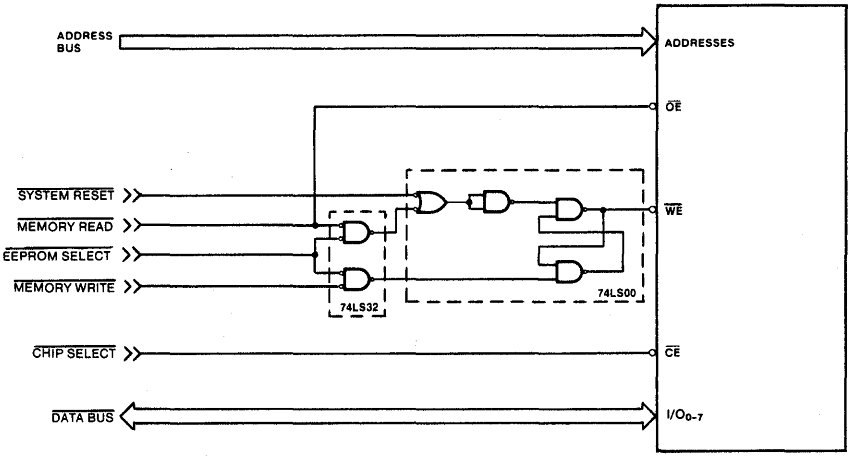
1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the mode selection table.

Typical EEPROM Write/Erase Routine



Microprocessor Interface Circuit Example for Byte Write/Erase



NOTE:

1. Characterized. Not tested.

Absolute Maximum Stress Ratings*

Temperature
Storage .... -65° C to +150° C
Under Bias .... -10° C to +80° C
All Inputs or Outputs with
Respect to Ground .... +6V to -0.3V
$\overline{WE}$ During Writing/Erasing
with Respect to Ground ...... +22.5V to -0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	52B13-200/-250/-350 52B13H-200/-250/-350
V_{CC} Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

D.C. Operating Characteristics During Read or Write/Erase (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Nom.[1]	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode			10	μA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	μA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode			1.5	mA	$\overline{WE}$ = 22V, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	μA	$\overline{WE} = V_{IL}$
	Chip Erase — High Voltage Mode			1.5	mA	$\overline{WE}$ = 22V
I_{CC1}	V_{CC} Standby Current		15	30	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{WE}	$\overline{WE}$ Read Voltage	2		V_{CC} + 1	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA
V_{OE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	I_{OE} = 10 μA

Notes:
1. Nominal values are for T_A = 25° C and V_{CC} = 5.0V

A.C. Operating Characteristics During Read (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	52B13 52B13H Min.	52B13 52B13H Max.	Unit	Test Conditions
t_{AA}	Address Access Time	–200 –250 –350		200 250 350	ns ns ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid	–200 –250 –350		200 250 350	ns ns ns	$\overline{OE} = V_{IL}$
t_{OE}[1]	Output Enable to Data Valid	–200 –250 –350		80 90 100	ns ns ns	$\overline{CE} = V_{IL}$
t_{DF}[2]	Output Enable to High Impedance	–200 –250 –350	0 0 0	60 70 80	ns ns ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold	All	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

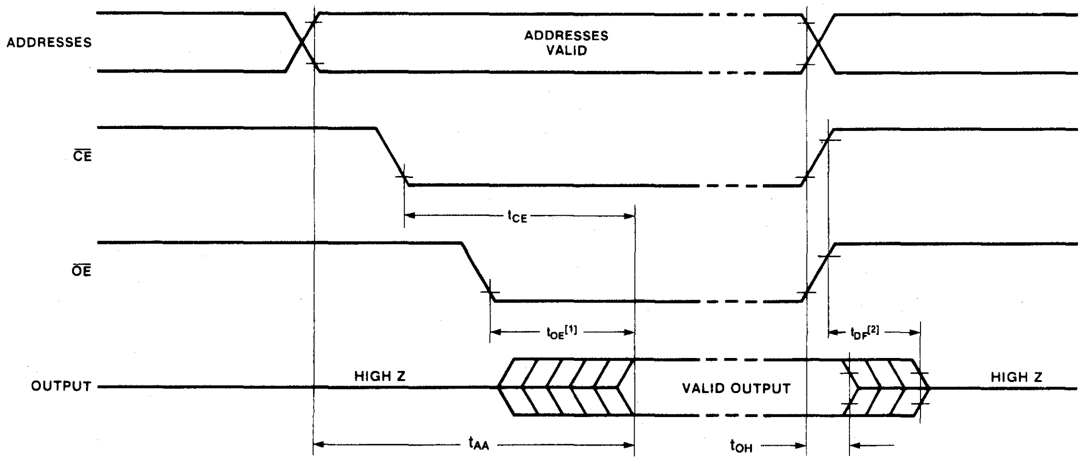
Capacitance[3] T_A=25°C, f=1 MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	10	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	10	pF	$V_{OUT} = 0V$
$C_{V_{CC}}$	V_{CC} Capacitance	500	pF	$\overline{OE} = \overline{CE} = V_{IH}$
$C_{V_{WE}}$	V_{WE} Capacitance	10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

Read Timing



NOTES:

1. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.

A.C. Operating Characteristics During Write/Erase (Over the operating V_{CC} and temperature range)

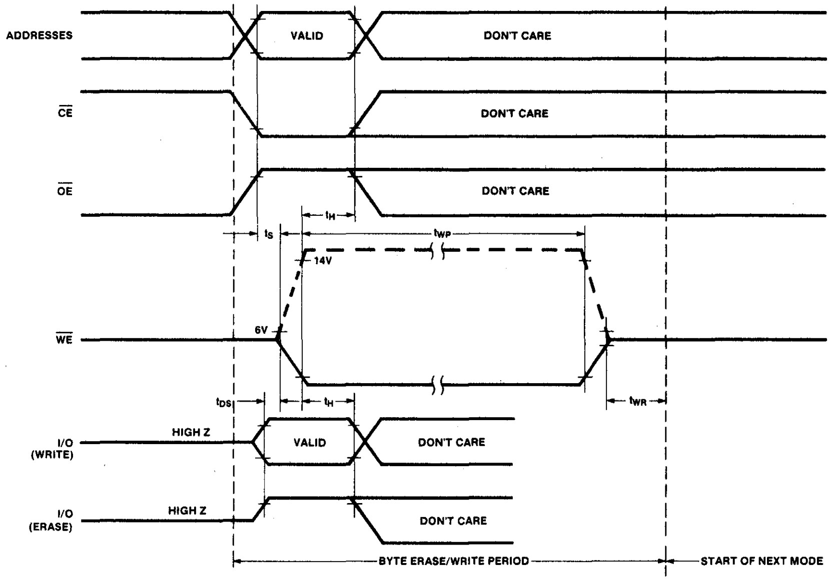
Symbol	Parameter		Min.	Max.	Units
t_S	$\overline{\text{CE}}$, $\overline{\text{OE}}$ or A_N Setup to $\overline{\text{WE}}$		50		ns
t_{DS}	Data Setup to $\overline{\text{WE}}$		15		ns
t_H[1]	$\overline{\text{WE}}$ to $\overline{\text{CE}}$, $\overline{\text{OE}}$, A_N or Data Change		50		ns
t_{WP}[1]	Write Enable, $\overline{\text{WE}}$,	52B13	9		ms
	Pulse Width	52B13H	1		ms
t_{WR}[2]	$\overline{\text{WE}}$ to Mode Change $\overline{\text{WE}}$ to next Byte Write/Erase Cycle		50		ns
	$\overline{\text{WE}}$ to start of a Read Cycle			2	µs

52B13/52B13H High Voltage Write Specifications

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications, including the TTL W/E mode.

		52B13		52B13H		
Symbol	Function/Parameter	Min.	Max.	Min.	Max.	Units
t_{WP}	Write Enable Pulse Width					
	Byte Write/Erase	9	20	1	10	ms
	Chip Erase	9	20	9	20	ms
V_{WE}	$\overline{\text{WE}}$ Write/Erase Voltage High Voltage Mode	14	22	14	22	V

Byte Erase or Byte Write Timing



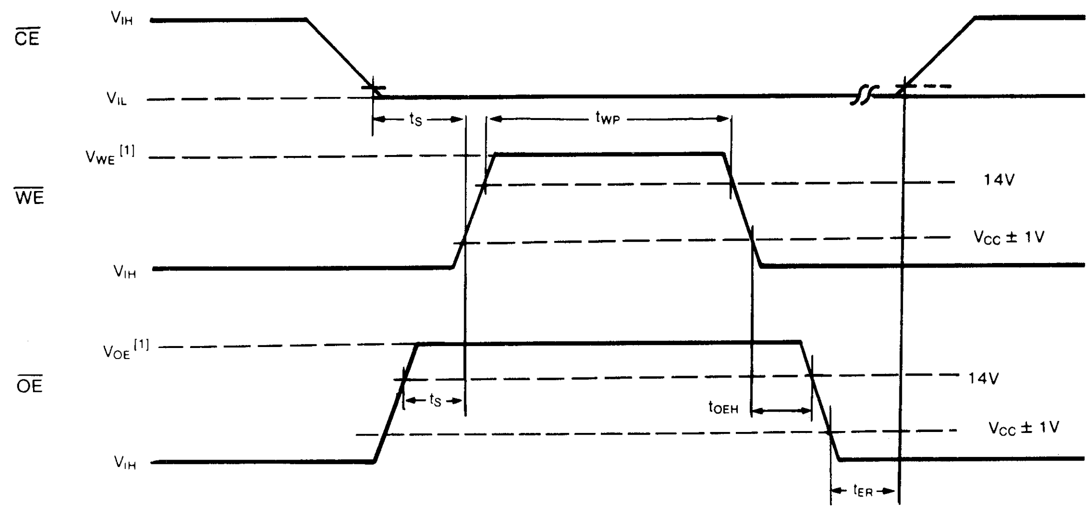
NOTES:

1. After t_H, hold time, from $\overline{\text{WE}}$, the inputs, $\overline{\text{CE}}$, $\overline{\text{OE}}$, address and Data are latched and are "Don't Cares" until t_{WR}, write recovery time, after the trailing edge of $\overline{\text{WE}}$.
2. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{\text{WE}}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

Chip Erase Specifications

Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ Setup to $\overline{WE}$	1		μs
t_{OEH}	$\overline{OE}$ Hold Time	1		μs
t_{WP}	$\overline{WE}$ Pulse Width	10		ms
t_{ER}	Erase Recovery Time		10	μs

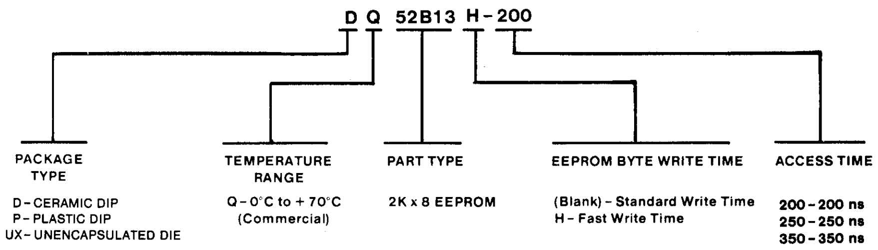
Chip Erase Timing



NOTES:

1. V_{WE} and V_{OE} can be from 15V to 21V in the high voltage mode for chip erase on 52B13.

Ordering Information



seeq

52B33/52B33H
64K Electrically Erasable PROM

October 1987

Features

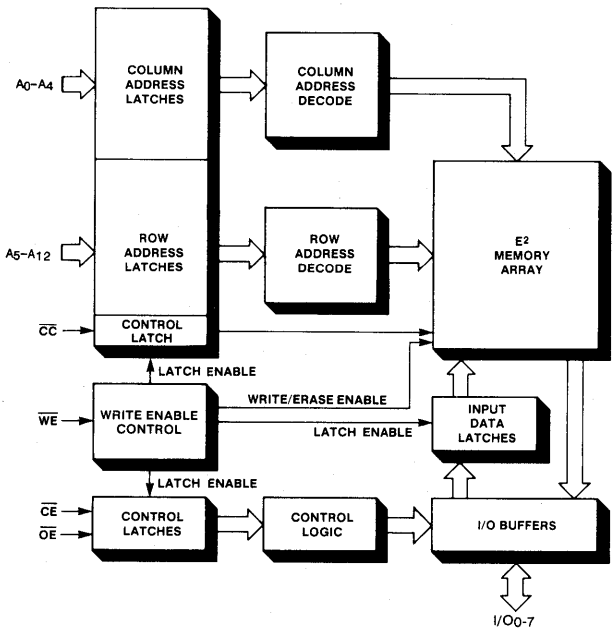
- ***High Write Endurance Over Temperature Range***
  - ***52B33/52B33H; 10,000 cycles/byte minimum***
- ***Input Latches***
- ***Fast TTL Byte Write Time***
  - ***1 ms for 52B33H***
  - ***9 ms for 52B33***
- ***5 V ± 10% V_{CC}***
- ***Power Up/Down Protection***
- ***200 ns Read Access Time***
- ***DiTrace®***
- ***Infinite Number of Read Cycles***
- ***JEDEC Approved Byte Wide Memory Pinout***
- ***Military And Extended Temperature Range Available***

Description

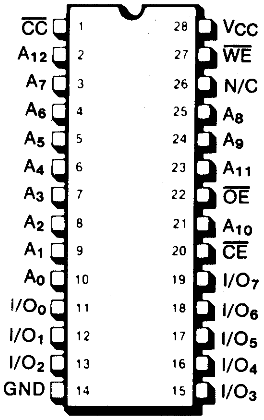
SEEQ's 52B33 is a 8192 x 8 bit, 5 volt electrically erasable programmable read only memory (EEPROM) which is specified over a 0°C to 70°C temperature range. Data retention is specified to be greater than 10 years. The device has input latches on all addresses, data, and control (chip and output) lines. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written there is no limit to the number of times data may be read. The erasure time is under 10 ms, and each byte may be erased and written a minimum of 10,000 times. For applications requiring a faster byte write or erase time, a 52B33H is available at 1 ms, giving a 10 times speed increase.

(continued on next page)

Block Diagram



Pin Configuration



Pin Names

A0-A4	ADDRESSES - COLUMN (LOWER ORDER BITS)
A5-A12	ADDRESSES - ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O0-7	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

The pin configuration is to the JEDEC approved byte wide memory pinout. EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the alteration of opening software in real-time) is made possible by EEPROMs. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other systems. Designing the EEPROMs into these systems is simplified because of the fast access time and input latches. The specified 200 ns access time eliminates or reduces the number of microprocessor wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ's 52B33 has six modes of operation (see Table 1) and requires only TTL inputs to operate these modes. The "H" members of the family operate in the same manner as the other devices except that a faster write enable pulse width of 1 ms is specified during byte erase or write.

Read

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is bought to a TTL low in order to enable the chip. The write enable ($\overline{WE}$) pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{OE}$) to a TTL low. During read, the address, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

Write

To write in to a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then brought to a TTL low level to latch all the inputs and I/O lines. All inputs can be released after the write enable hold time (t_H) and the next input conditions can be established while the byte is being erased. During this operation, the write enable must be held at a TTL low for 9 ms (t_{WP}). A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H performs the same as the 52B33 except that the byte erase/byte write time has been enhanced to 1 ms.

Chip Clear

Certain applications may require all bytes to be erased simultaneously. See A.C. Operating Characteristics for TTL chip erase timing specifications.

DiTrace®

SEEQ's family of EEPROMs incorporate a DiTrace field. The DiTrace feature is a method for storing production flow information in an extra row of EEPROM cells. As each major manufacturing operation is performed the DiTrace field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Power Up/Down Considerations

SEEQ's "52B" E^2 family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the mode selection table.

Mode Selection (Table 1)

Function (Pin) / Mode	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Clear	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL} or V_{IH}
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	Don't Care	High Z

DiTrace is a registered trademark of SEEQ Technology, Inc.

NOTE:

[1] Characterized. Not tested.

Absolute Maximum Stress Rating*

Temperature
Storage .... −65°C to +100°C
Under Bias .... −10°C to +80°C

All Inputs or Outputs with
Respect to Ground .... +6V to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	52B33, 52B33H
V_{CC} Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

D.C. Operating Characteristics During Read or Erase/Write (Over the operating V_{CC} and temperature range)

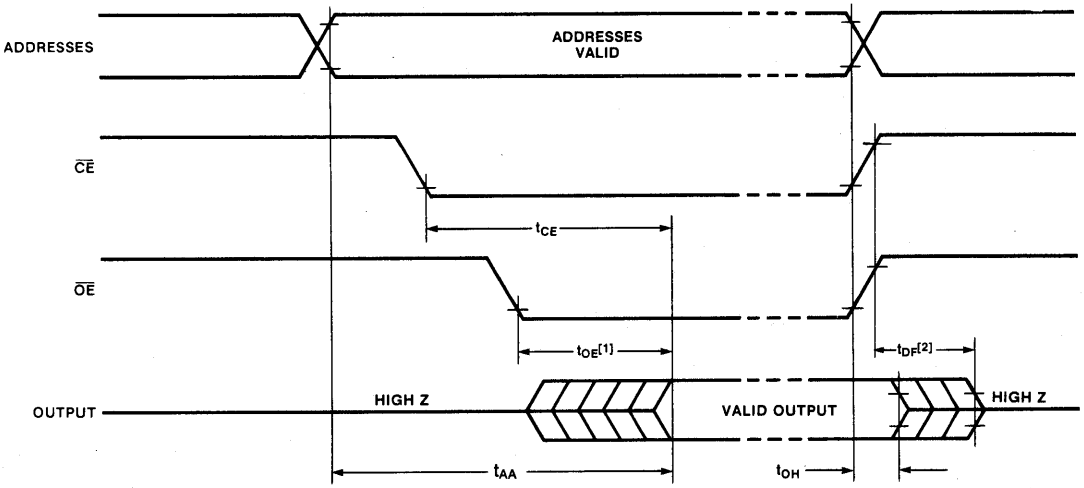
Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage			10	μA	$\overline{WE} = V_{IL}$
I_{CC1}	V_{CC} Standby Current		18	40	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		60	110	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

Notes:
1. Nominal values are for $T_A = 25°$ C and $V_{CC} = 5.0$ V

AC Operating Characteristics During Read (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	52B33 52B33H Min.	Max.	Unit	Test Conditions
t_{AA}	Address Access Time	−200		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		−250		250	ns	
		−350		350	ns	
t_{CE}	Chip Enable to Data Valid	−200		200	ns	$\overline{OE} = V_{IL}$
		−250		250	ns	
		−350		350	ns	
t_{OE}[1]	Output Enable to Data Valid	−200		80	ns	$\overline{CE} = V_{IL}$
		−250		90	ns	
		−350		100	ns	
t_{DF}[2]	Output Enable to High Impedance	−200	0	60	ns	$\overline{CE} = V_{IL}$
		−250	0	70	ns	
		−350	0	80	ns	
t_{OH}	Output Hold	All	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/ C_{OUT}[3]	Input and Output Capacitance	All		10	pF	$V_{IN} = 0$ V for C_{IN}, $V_{OUT} = 0$ V for C_{OUT}, $T_A = 25°C$

Read Cycle Timing



NOTES:

1. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
4. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
5. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

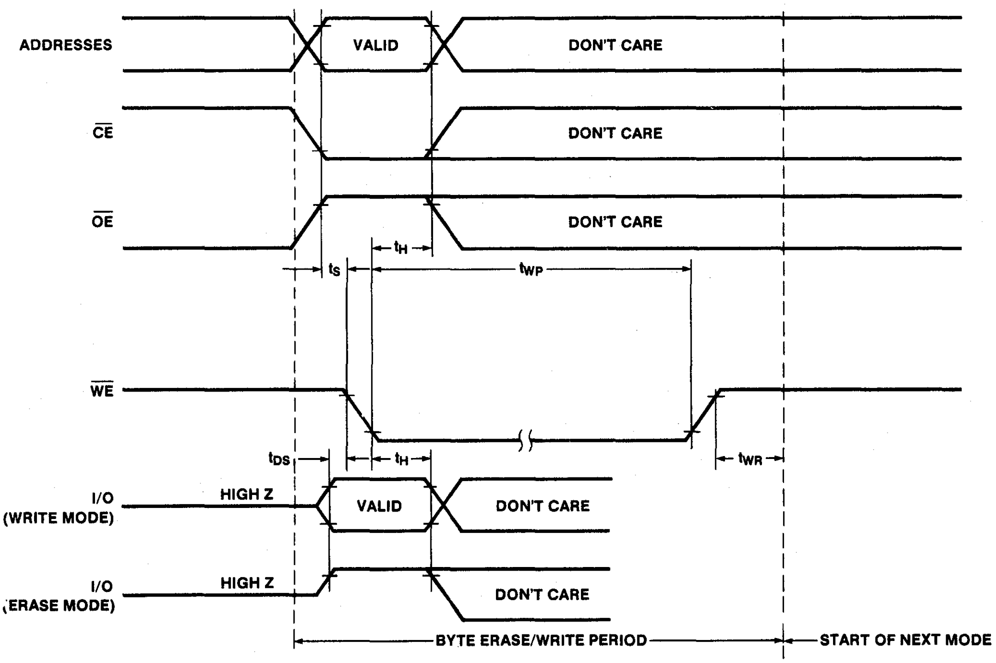
A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

A.C. Operating Characteristics During Write/Erase (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or Address Setup to $\overline{WE}$	50		ns
t_{DS}	Data Setup to $\overline{WE}$	15		ns
t_H[4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, Address or Data Change	50		ns
t_{WP}	Write Enable ($\overline{WE}$) Pulse Width Byte Modes — 52B33	9		ms
	Byte Modes — 52B33H	1		
t_{WR}[5]	$\overline{WE}$ to Mode change $\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle	1		µs

Byte Erase or Byte Write Cycle Timing

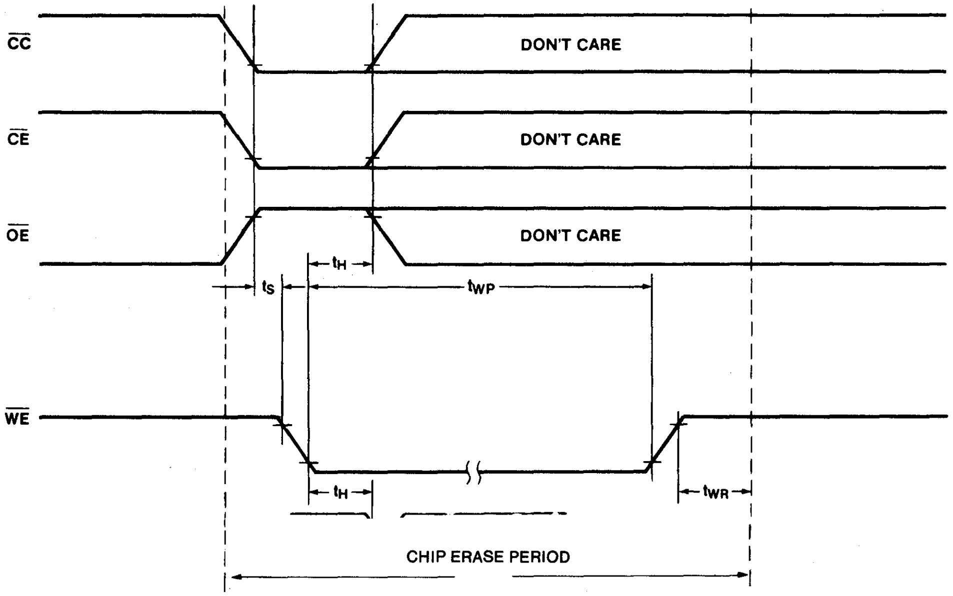


(Notes 4 and 5 are on previous page)

A.C. Operating Characteristics During Chip Erase (Over the operating V_{CC} and temperature range)

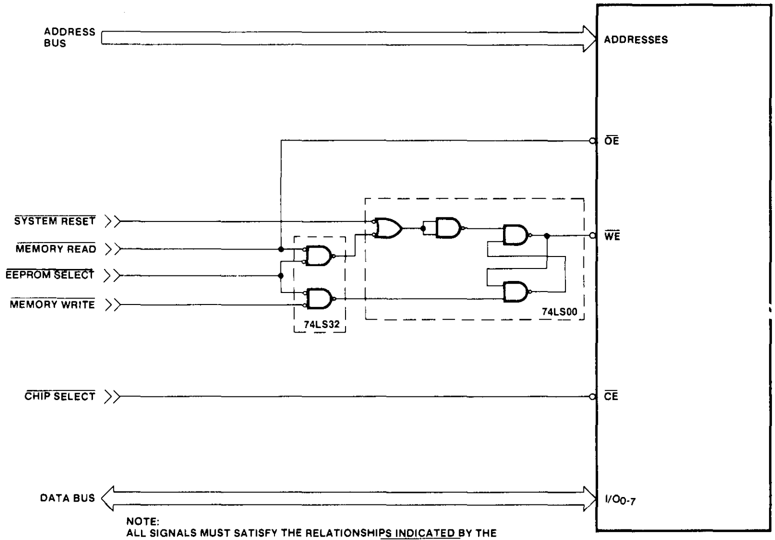
Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CC}$, $\overline{CE}$ $\overline{OE}$ Setup to $\overline{WE}$	50		ns
t_H[4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, $\overline{CC}$ change	50		ns
t_{WP}	Write Enable ($\overline{WE}$) Pulse Width Chip Erase — 52B33 Chip Erase — 52B33H	10		ms
t_{WR}[5]	$\overline{WE}$ to Mode change $\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle		1	μs

TTL Chip Erase Timing



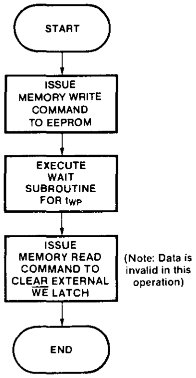
NOTE: Address, Data are don't care during Chip Erase.

Microprocessor Interface Circuit Example for Byte Write/Erase

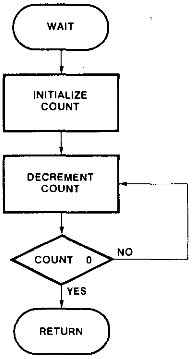


NOTE:
ALL SIGNALS MUST SATISFY THE RELATIONSHIPS INDICATED BY THE TIMING DIAGRAMS SHOWN ON PAGES 4 AND 5. EEPROM SELECT IS DERIVED FROM THE CHIP SELECT SIGNALS OF ALL DEVICES FOR WHICH THIS CIRCUIT GATES WE. THIS MAY ENTAIL A SIMPLE OR FUNCTION. IN CASE OF A SINGLE EEPROM, THE TWO SIGNALS WOULD BE COMMON.

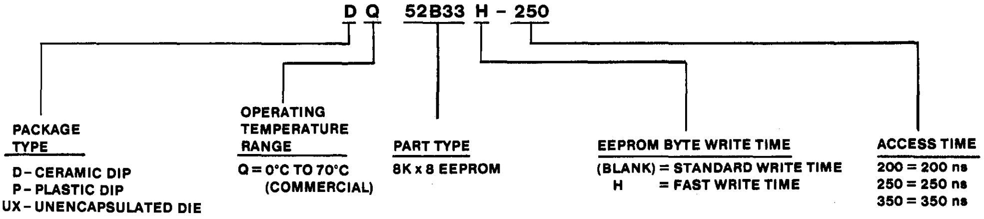
Typical EEPROM Write/Erase Routine



WAIT SUBROUTINE



Ordering Information



2804A
Timer E^2
4K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1988

Features

- **High Endurance**
  - **10,000 Cycles/Byte Minimum**
- **On-Chip Timer**
  - **Automatic Erase and Write Time Out**
- **All Inputs Latched by Write or Chip Enable**
- **Direct Replacement to 512 x 8 EEPROMS**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - **80 mA max. Active Current**
  - **40 mA max. Standby Current**
- **10 Year Data Retention**
- **JEDEC Standard Byte-Wide Pinout**

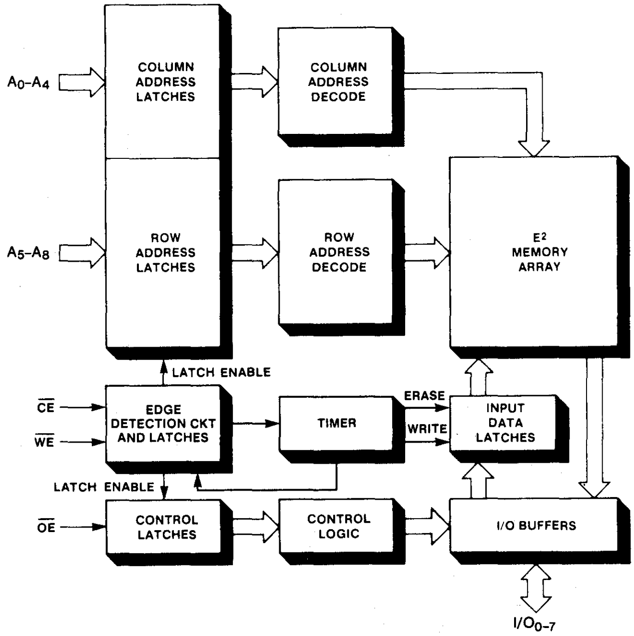
Description

SEEQ's 2804A is a 5 V only, 512 x 8 electrically erasable programmable read only memory (EEPROM). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times that a byte may be written, is 10 thousand cycles for the 2804A.

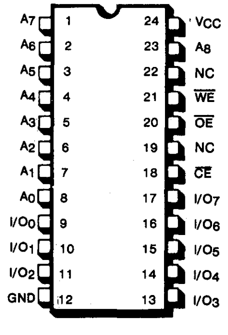
This device has an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable ($\overline{WE}$) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system for other tasks during the write time. The write time is 10 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

(Continued on page 2)

Block Diagram



Pin Configuration



Pin Names

A_0-A_4	COLUMN ADDRESSES
A_5-A_8	ROW ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE) DATA OUTPUT (READ)

Q Cell is a trademark of SEEQ Technology, Inc.

Device Operation

There are four operational modes (see Table 1) and only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$ and data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode. The 2804A ignores attempts to read or write while the internal write cycle is in progress.

Absolute Maximum Stress Ratings*

Temperature
Storage .... −65°C to +150°C
Under Bias .... −10°C to +80°C
All Inputs or Outputs with
Respect to Ground .... +6V to −0.3V

Recommended Operating Conditions

	2804A
Temperature Range	(Ambient) 0°C to 70°C
V_{CC} Supply Voltage	5 V ± 10%

Mode Selection (Table 1)

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X X	V_{IL} X	X V_{IH}	HI Z/D_{OUT} HI Z/D_{OUT}

X – Any TTL Level.

Power Up/Down Considerations

The 2804A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

DC Operating Characteristics T_A=0° to 70°C; V_{CC}=5 V ± 10%, unless otherwise noted.

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I_{CC}	Active V_{CC} Current		80	mA	$\overline{CE}$=$\overline{OE}$=V_{IL}; All I/O open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IL}; All I/O's Open; Other Inputs = 5.5 V
I_{IL}	Input Leakage Current		10	µA	V_{IN}=5.5 V
I_{OL}	Output Leakage Current		10	µA	V_{OUT}=5.5 V
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH}=-400 µA

NOTE:
1. Characterized. Not tested.

AC Characteristics

Read Operation T_A=0° to 70°C; V_{CC}=5 V ± 10%, unless otherwise noted.

Symbol	Parameter	Limits				Units
		2804A-250		2804A-300		
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		ns
t_{CE}	Chip Enable Access Time		250		300	ns
t_{AA}	Address Access Time		250		300	ns
t_{OE}	Output Enable Access Time		90		100	ns
t_{LZ}	$\overline{CE}$ to Output in Low Z	10		10		ns
t_{HZ}	$\overline{CE}$ to Output in HI Z		100		100	ns
t_{OLZ}	$\overline{OE}$ to Output in Low Z	50		50		ns
t_{OHZ}	$\overline{OE}$ to Output in HI Z		100		100	ns
t_{OH}[1]	Output Hold from Address Change	20		20		ns
t_{PU}[1]	$\overline{CE}$ to Power-up Time	0		0		ns
t_{PD}[1]	$\overline{CE}$ to Power Down Time		50		50	ns

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0$ V

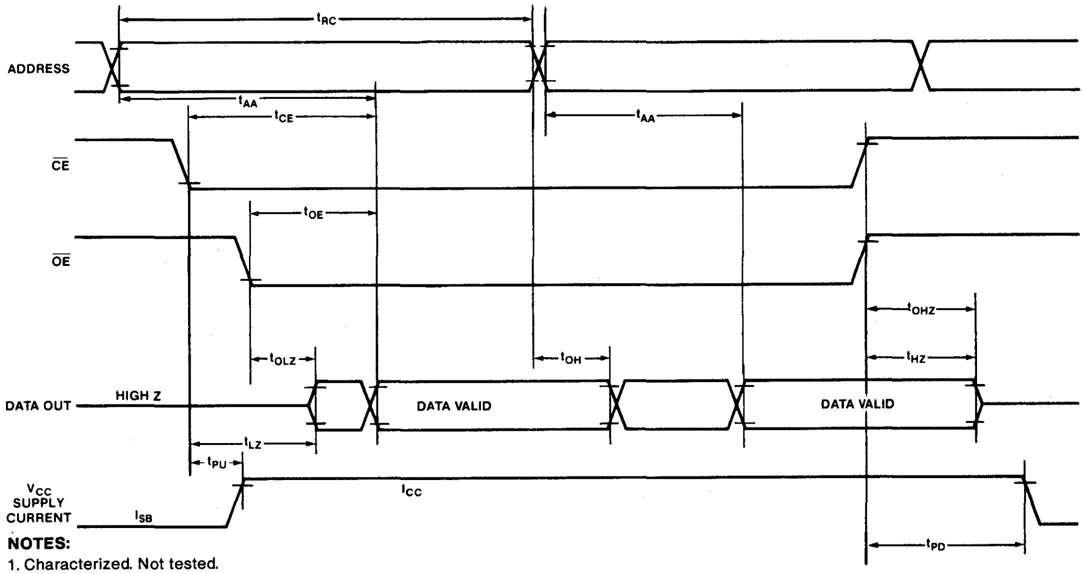
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[1]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Read Cycle Timing



NOTES:

1. Characterized. Not tested.
2. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

AC Characteristics

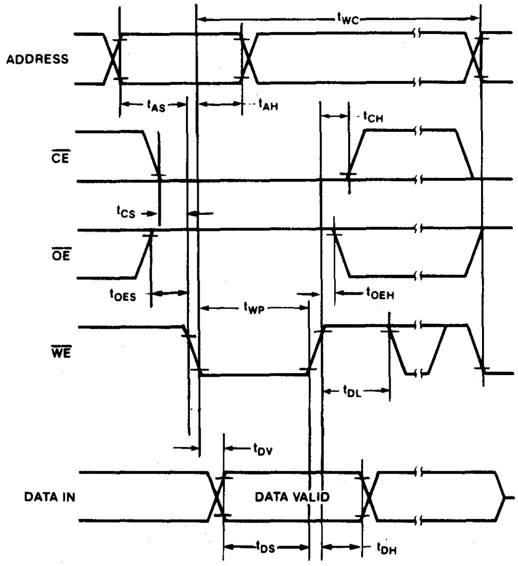
TTL WRITE CYCLE T_A=0° to 70°C; V_{CC}=5 V ± 10%, unless otherwise noted.

Symbol	Parameter	2804A-250 Min.	2804A-250 Max.	2804A-300 Min.	2804A-300 Max.	Units
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Set Up Time	10		10		ns
t_{AH}	Address Hold Time	50		70		ns
t_{CS}	Write Set Up Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{\text{CE}}$ to End of Write Input	150		150		ns
t_{OES}	$\overline{\text{OE}}$ Set Up Time	10		10		ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10		10		ns
t_{WP}[1]	$\overline{\text{WE}}$ Write Pulse Width	150		150		ns
t_{DL}	Data Latch Time	50		50		ns
t_{DV}[2]	Data Valid Time		1		1	μs
t_{DS}	Data Set Up Time	50		50		ns
t_{DH}	Data Hold Time	0		0		ns

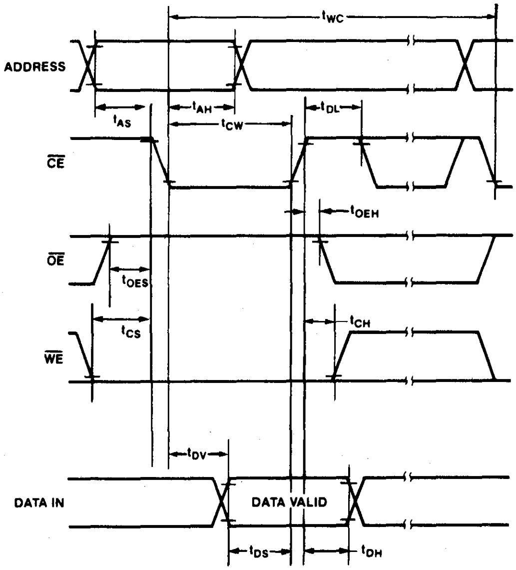
NOTES:
1. $\overline{\text{WE}}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle. Characterized, not tested.

TTL Byte Write Cycle

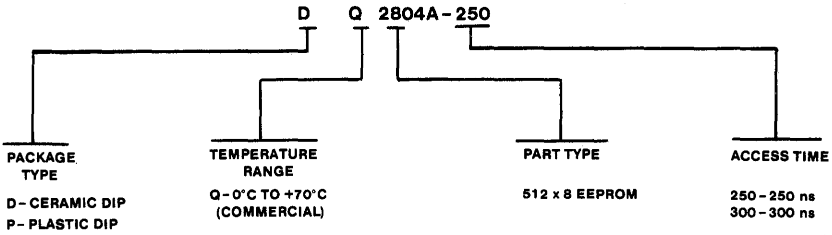
$\overline{\text{WE}}$ CONTROLLED WRITE CYCLE



$\overline{\text{CE}}$ CONTROLLED WRITE CYCLE



Ordering Information



seeq

2816A/5516A Timer E^2 16K Electrically Erasable PROMs

October 1988

Features

- **High Endurance Write Cycles**
  - **5516A: 1,000,000 Cycles/Byte Minimum**
  - **2816A: 10,000 Cycles/Byte Minimum**
- **On-Chip Timer**
  - **Automatic Erase and Write Time Out**
  - **2 ms Byte Write Time (2816AH)**
- **All Inputs Latched by Write or Chip Enable**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **200 ns max. Access Time**
- **Low Power Operation**
  - **110 mA max. Active Current**
  - **40 mA max. Standby Current**
- **JEDEC Approved Byte-Wide Pinout**
- **Military and Extended Temperature Range Available.**

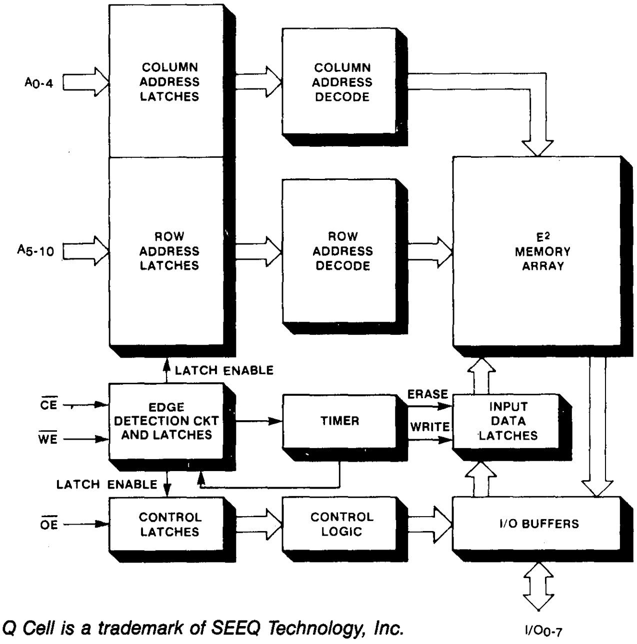
Description

SEEQ's 5516A and 2816A are 5 V only, 2Kx8 electrically erasable programmable read only memories (EEPROMs). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times that a byte may be written, is **1 million** for the 5516A and 10 thousand for the 2816A. The 5516A's extraordinary high endurance was accomplished using SEEQ's proprietary oxyntride EEPROM process and its innovative Q Cell™ design. The 5516A is ideal for systems that require frequent updates.

Both EEPROMs have an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable ($\overline{WE}$) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system for other tasks during the write time. The standard 2816A and 5516A's write time is 10 ms, while the 2816AH's write time

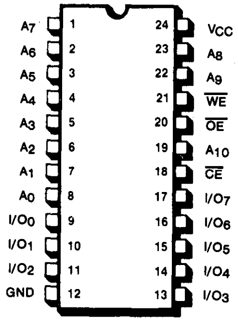
(continued on next page)

Block Diagram



Q Cell is a trademark of SEEQ Technology, Inc.

Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

is a fast 2 ms. Once a byte is written, it can be read in 200 ns. The inputs are TTL for both the byte write and read mode.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode[2], only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$ and data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

Mode Selection (Table 1)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X X	V_{IL} X	X V_{IH}	High Z/D_{OUT} High Z/D_{OUT}

X: any TTL level

Power Up/Down Considerations

The 2816A/5516A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.[3]*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage .... −65°C to +150°C
Under Bias .... −10°C to +80°C
All Inputs or Outputs with
Respect to Ground .... +6V to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	5516A/5516AH 2816A/2816AH
Temperature Range (Ambient)	0°C to 70°C
V_{CC} Supply Voltage	5 V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000 1,000,000 [1]	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

NOTES:
1. 5516A-1 million cycles/byte.
2. Chip Erase is an optional mode.
3. Characterized. Not tested.

DC Operating Characteristics T_A=0° to 70°C, V_{CC}=5 V ± 10% unless otherwise noted

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O's Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	μA	V_{IN} = 5.5 V
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = 5.5 V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400 μA

AC Characteristics

Read Operation T_A=0° to 70°C, V_{CC}=5 V ± 10%, unless otherwise noted

		Limits								
		5516A/5516AH-200 2816A/2816AH-200		5516A/5516AH-250 2816A/2816AH-250		5516A/5516AH-300 2816A/2816AH-300		2816A-350		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{RC}	Read Cycle Time	200		250		300		350		ns
t_{CE}	Chip Enable Access Time		200		250		300		350	ns
t_{AA}	Address Access Time		200		250		300		350	ns
t_{OE}	Output Enable Access Time		90		90		100		100	ns
t_{LZ}	$\overline{CE}$ to Output in Low Z	10		10		10		10		ns
t_{HZ}	$\overline{CE}$ to Output in High Z		100		100		100		100	ns
t_{OLZ}	$\overline{OE}$ to Output in Low Z	50		50		50		50		ns
t_{OHZ}	$\overline{OE}$ to Output in High Z		100		100		100		100	ns
t_{OH}[1]	Output Hold from Addr Change	20		20		20		20		ns
t_{PU}[1]	$\overline{CE}$ to Power-up Time	0		0		0		0		ns
t_{PD}[1]	$\overline{CE}$ to Power Down Time		50		50		50		50	ns

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O}$ = 0 V

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[1]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

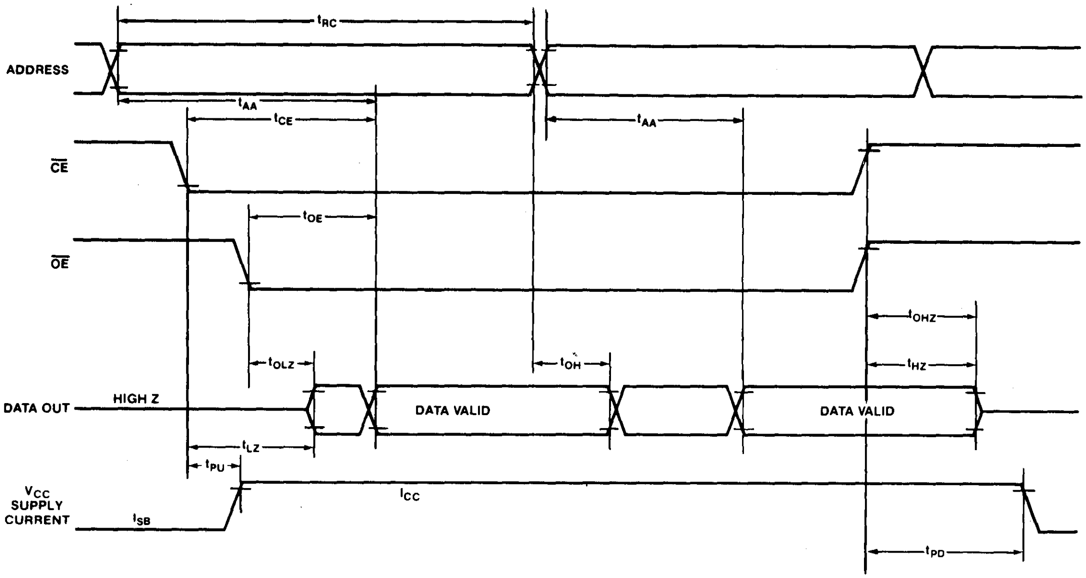
A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

NOTES:

1. Characterized. Not tested.
2. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

Read Cycle Timing



AC Characteristics

Write Operation T_A=0° to 70°C, V_{CC}=5 V ± 10% unless otherwise noted

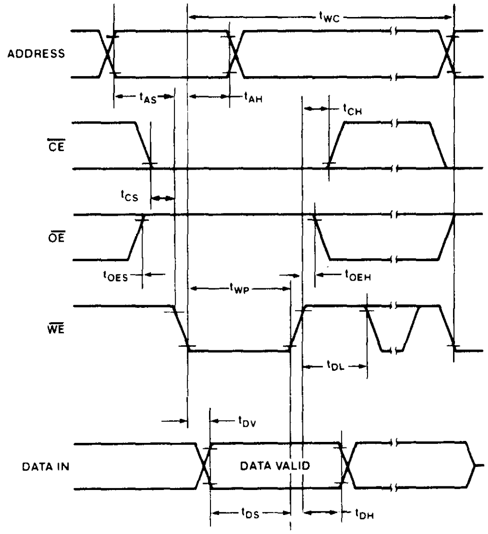
		Limits								
		5516A-200 2816A/2816AH-200		5516A-250 2816A/2816AH-250		5516A-300 2816A/2816AH-300		2816A-350		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WC}	Write Cycle Time 5516AH/2816AH		2		2		2	—	—	ms
	5516A/2816A		10		10		10		10	
t_{AS}	Address Set Up Time	10		10		10		10		ns
t_{AH}	Address Hold Time	50		50		70		70		ns
t_{CS}	Write Set Up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{\text{CE}}$ to End of Write Input	150		150		150		150		ns
t_{OES}	$\overline{\text{OE}}$ Set Up Time	10		10		10		10		ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10		10		10		10		ns
t_{WP}[1]	$\overline{\text{WE}}$ Write Pulse Width	150		150		150		150		ns
t_{DL}	Data Latch Time	50		50		50		50		ns
t_{DV}[2]	Data Valid Time		1		1		1		1	μs
t_{DS}	Data Set Up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns

Notes:

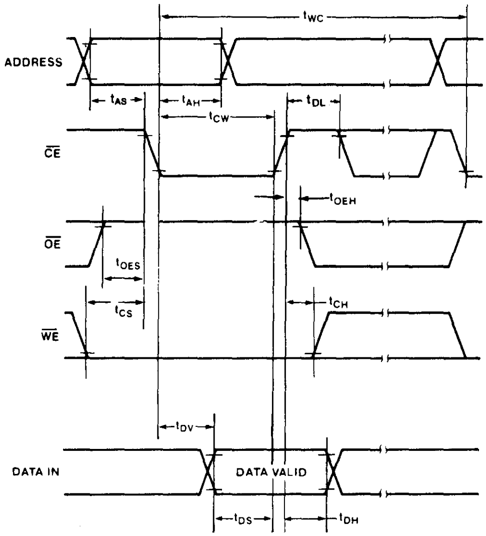
1. $\overline{\text{WE}}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

TTL Byte Write Cycle

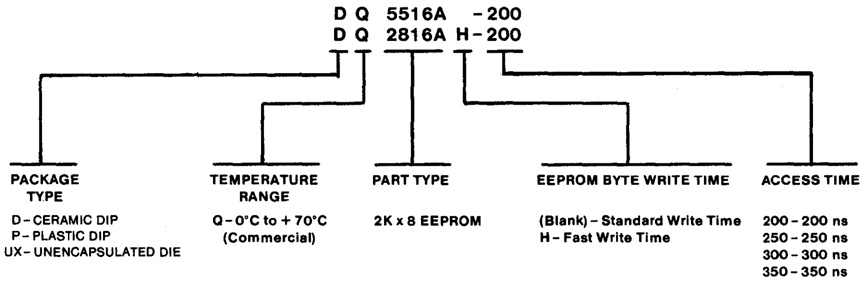
$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



Ordering Information



D Q 5516A -200
D Q 2816A H-200

PACKAGE TYPE
D- CERAMIC DIP
P- PLASTIC DIP
UX- UNENCAPSULATED DIE

TEMPERATURE RANGE
Q- 0°C to + 70°C (Commercial)

PART TYPE
2K x 8 EEPROM

EEPROM BYTE WRITE TIME
(Blank) - Standard Write Time
H- Fast Write Time

ACCESS TIME
200 - 200 ns
250 - 250 ns
300 - 300 ns
350 - 350 ns

seeq

2817A/5517A
Timer E^2
16K Electrically Erasable PROMs

October 1988

Features

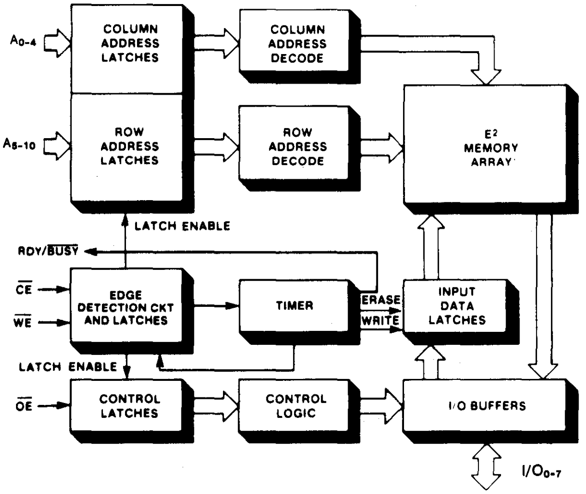
- **Ready/$\overline{\text{Busy}}$ Line for End-of-Write**
- **High Endurance Write Cycles**
  - **— 5517A: 1,000,000 Cycles/Byte Minimum**
  - **— 2817A: 10,000 Cycles/Byte Minimum**
- **On-Chip Timer**
  - **— Automatic Byte Erase Before Byte Write**
  - **— 2 ms Byte Write Time (2817AH)**
- **All Inputs Latched by Write or Chip Enable**
- **5 V ± 10% Power Supply**
- **Power Up/Down Supply**
- **200 ns max. Access Time**
- **10 Year Data Retention for Each Write**
- **JEDEC Approved Byte-Wide Pinout**
- **Military and Extended Temperature Range Available**

Description

SEEQ's 5517A and 2817A are 5 V only, 2Kx8 electrically erasable programmable read only memories (EEPROMs). They are packaged in a 28 pin package and have a ready/$\overline{\text{busy}}$ pin. These EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times which a byte may be written, is 1 million for the 5517A and 10 thousand for the 2817A. The 5517A's extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. The 5517A is ideal for systems that require frequent updates and/or high reliability. System reliability is enhanced greatly over lower specified endurance EEPROMs while still maintaining 10 year data retention.

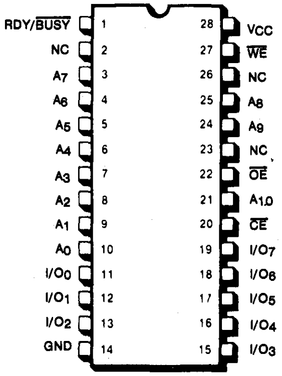
Both EEPROMs have an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The standard 5517A/2817A's write time is 10 ms, while the 2817AH's write time is a fast 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/$\overline{\text{busy}}$ pin signals the microprocessor that it is available for either a write or read mode. The inputs are TTL for both the byte write and read mode. Data retention is specified for 10 years.

Block Diagram



Q Cell is a trademark of SEEQ Technology, Inc.

Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)
RDY/$\overline{\text{BUSY}}$	DEVICE READY/$\overline{\text{BUSY}}$
NC	NO CONNECT

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode[2], only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occured first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied 2817A RDY/$\overline{BUSY}$ pins.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X	V_{IL}	X	High Z/D_{OUT}	High Z
	X	X	V_{IH}	High Z/D_{OUT}	High Z

X: Any TTL level

Power Up/Down Considerations

The 2817A/5517A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.[3]*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred with V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

*Absolute Maximum Stress Ratings**

Temperature
Storage .... −65°C to +150°C
Under Bias .... −10°C to +80°C
All Inputs or Outputs with
Respect to Ground .... +6V to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	5517A 2817A/2817AH
V_{CC} Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000 1,000,000 [1]	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

NOTES:
1. 5517A — 1 million cycles/byte.
2. Chip Erase is an optional mode.
3. Characterized. Not tested.

D.C. Operating Characteristics (Over the operating V_{CC} and temperature range)

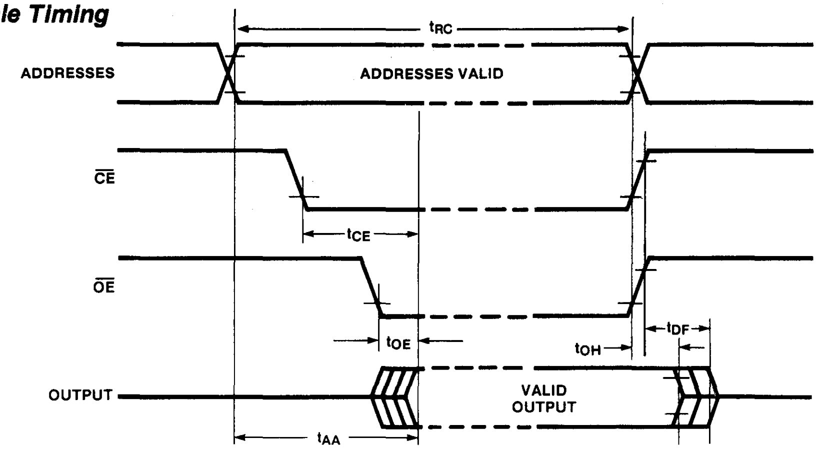
Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I_{CC}	Active V_{CC} Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = 5.5$ V
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = 5.5$ V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ µA

A.C. Characteristics

Read Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits								Units	Test Conditions
		2817AH-200 2817A-200		2817AH-250 5517A-250 2817A-250		2817AH-300 5517A-300 2817A-300		2817A-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		75		90		100		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven		60		60		60		80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first.	0		0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

Read Cycle Timing



Capacitance[1] T_A=25°C, f=1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O}$ = 0 V

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

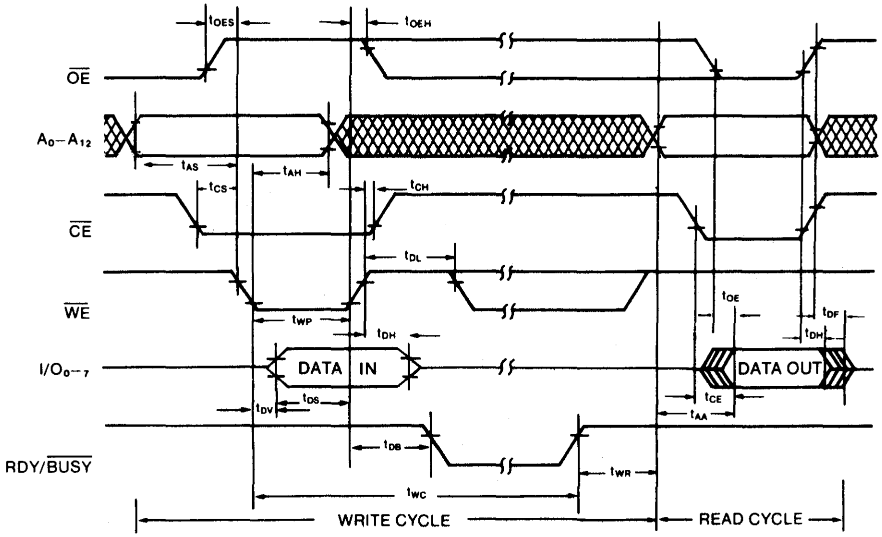
AC Characteristics

Write Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits								Units
		2817AH-200 2817A-200		2817AH-250 5517A-250 2817A-250		2817AH-300 5517A-300 2817A-300		2817A-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address to Write Set Up Time	10		10		10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	10		10		10		10		ns
t_{WP}[3]	$\overline{WE}$ Write Pulse Width	120		150		150		150		ns
t_{AH}	Address Hold Time	50		50		50		70		ns
t_{DS}	Data Set Up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		10		ns
t_{DL}	Data Latch Time	50		50		50		50		ns
t_{DV}[4]	Data Valid Time		1		1		1		1	μs
t_{DB}	Time to Device Busy		120		120		120		120	ns
t_{WR}	Write Recovery Time Before Read Cycle		10		10		10		10	μs
t_{WC}	Byte Write Cycle Time 2817A/5517A		10		10		10		10	ms
	2817AH		2		2		2			ms

NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.
3. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
4. Data must be valid within 1 ms maximum after the initiation of a write cycle.

Write Cycle Timing



Ordering Information

D Q 5517A -250
D Q 2817A -250
D Q 2817A -250

PACKAGE	TEMPERATURE RANGE	PART TYPE	EEPROM BYTE WRITE TIME	ACCESS TIME
D-CERAMIC DIP	Q-0°C to 70°C	2K x 8 EEPROM	(Blank) - Standard Write Time	200-200 ns
P-PLASTIC DIP			H - Fast Write Time	250-250 ns
UX-UNENCAPSULATED DIE				300-300 ns
				350-350 ns

seeq

2864/2864H
Timer E^2
64K Electrically Erasable PROM

October 1987

Features

- **Ready/$\overline{\text{Busy}}$ Pin**
- **High Endurance Write Cycles**
  - **10,000 Cycles/Byte Minimum**
- **On-Chip Timer**
  - **Automatic Byte Erase Before Byte Write**
  - **2 ms Byte Write (2864H)**
- **5 V±10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Military and Extended Temperature Range Available**

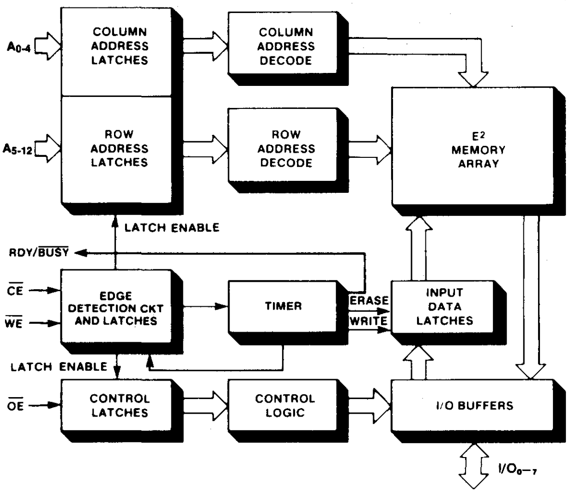
Description

SEEQ's 2864 is a 5 V only, 8K x 8 NMOS electrically erasable programmable read only memory (EEPROM). It is packaged in a 28 pin package and has a ready/$\overline{\text{busy}}$ pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is a minimum of 10 thousand cycles.

The EEPROM has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for tasks during the write time. The standard byte write cycle time is 10 ms. For systems requiring faster byte write, a 2864H is specified at 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/$\overline{\text{busy}}$ pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

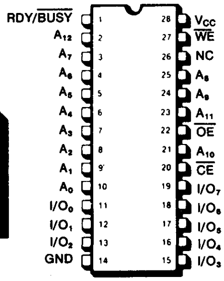
These two timer EEPROMs are ideal for systems with limited board area. For systems where cost is important, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

Block Diagram

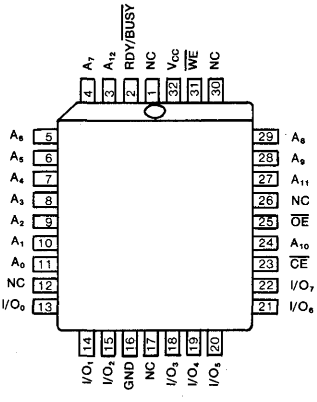


Pin Configuration

DUAL-IN-LINE TOP VIEW



PLASTIC LEADED CHIP CARRIER TOP VIEW



Pin Names

A_{0-4}	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_{5-12}	ADDRESSES — ROW
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/$\overline{\text{BUSY}}$	DEVICE READY/BUSY
N/C	NO CONNECT

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a 150 ns TTL pulse is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a 10 ms write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins. If RDY/$\overline{BUSY}$ is not used it can be left unconnected.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)	RDY/$\overline{BUSY}$ (1)*
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X	V_{IL}	X	High Z/D_{OUT}	High Z
	X	X	V_{IH}	High Z/D_{OUT}	High Z

*Pin 1 has an open drain output and requires an external 3K resistor to V_{CC} . The value of the resistor is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

Power Up/Down Considerations

The 2864 has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature

Storage	*-65° C to +150° C*
Under Bias	*-10° C to +80° C*
All Inputs or Outputs with Respect to Ground	*+6 V to −0.3 V*

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	2864H-250/H-300 2864-250/-300	2864-350
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C	0°C to 70°C

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

NOTE: 1 – Characterized. Not tested.

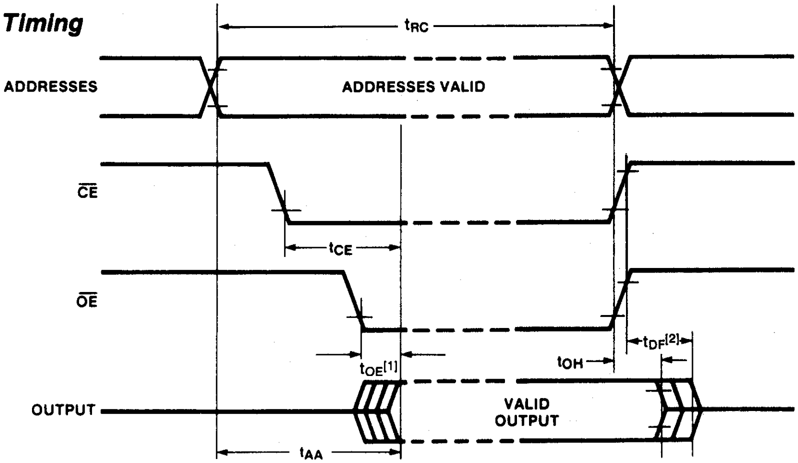
DC Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = V_{CC}$ Max.
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu$A

AC Characteristics Read Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	2864H-250 2864-250 Min.	2864H-250 2864-250 Max.	2864H-300 2864-300 Min.	2864H-300 2864-300 Max.	2864-350 Min.	2864-350 Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		90		100		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

Read Cycle Timing



NOTES:

1. $\overline{OE}$ MAY BE DELAYED TO $t_{AA} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{AA}.
2. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

Capacitance T_A[1] = 25°C; f = MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0$ V

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

E.S.D. Characteristics[4]

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

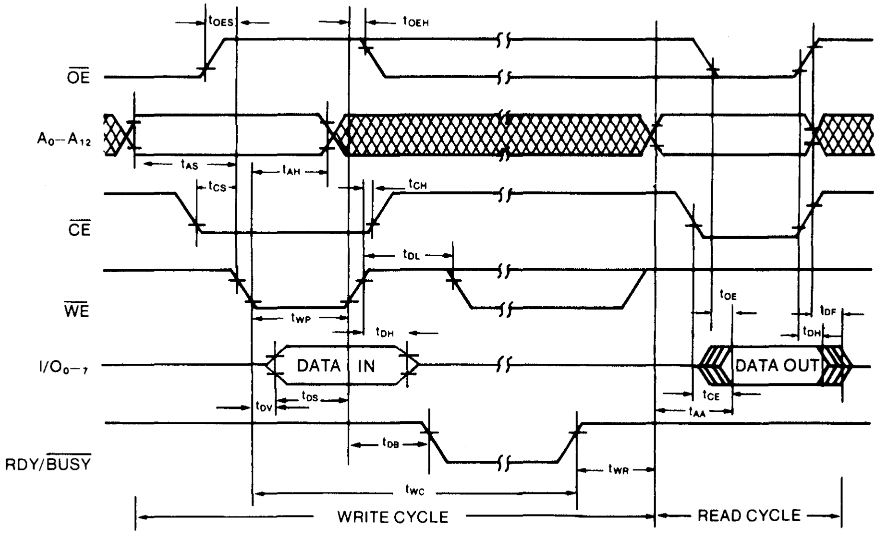
AC Characteristics

Write Operation (Over operating temperature and V_{CC} range)

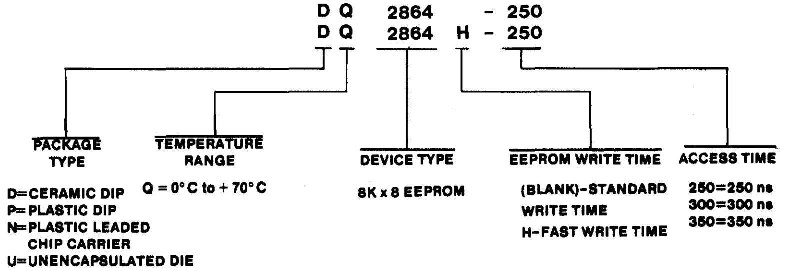
Symbol	Parameter	Limits						Units
		2864H-250 2864-250		2864H-300 2864-300		2864-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time/Byte Standard Family Only		10		10		10	ms
	“H” Family Only		2		2		—	ms
t_{AS}	Address to WE Set Up Time	10		10		10		ns
t_{CS}	$\overline{\text{CE}}$ to Write Set Up Time	0		0		0		ns
t_{WP}[2]	$\overline{\text{WE}}$ Write Pulse Width	150		150		150		ns
t_{AH}	Address Hold Time	50		50		70		ns
t_{DS}	Data Set Up Time	50		50		50		ns
t_{DH}	Data Hold Time	20		20		20		ns
t_{CH}	$\overline{\text{CE}}$ Hold Time	0		0		0		ns
t_{OES}	$\overline{\text{OE}}$ Set Up Time	10		10		10		ns
t_{OEH}	$\overline{\text{OE}}$ Hold Time	10		10		10		ns
t_{DL}	Data Latch Time	50		50		50		ns
t_{DV}[3]	Data Valid Time		1		1		1	μs
t_{DB}	Time to Device Busy		200		200		200	ns
t_{WR}	Write Recovery Time Before Read Cycle		10		10		10	μs

Notes:
1. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.
2. $\overline{\text{WE}}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within 1 μs maximum after the initiation of a write cycle.
4. Characterized. Not tested.

Write Cycle Timing



Ordering Information



D Q 2864 - 250
D Q 2864 H - 250

PACKAGE TYPE
D=CERAMIC DIP
P=PLASTIC DIP
N=PLASTIC LEADED CHIP CARRIER
U=UNENCAPSULATED DIE

TEMPERATURE RANGE
Q = 0°C to + 70°C

DEVICE TYPE
8K x 8 EEPROM

EEPROM WRITE TIME
(BLANK)-STANDARD WRITE TIME
H-FAST WRITE TIME

ACCESS TIME
250=250 ns
300=300 ns
350=350 ns

seeq

28C64
Timer E^2
64K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October, 1988

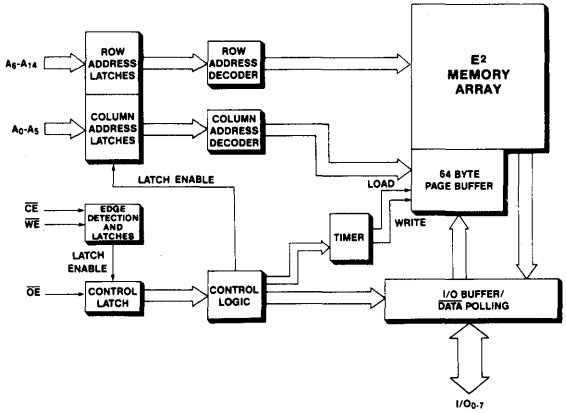
Features

- **CMOS Technology**
- **Low Power**
  - **50 mA Active**
  - **150 μA Standby**
- **Page Write Mode**
  - **64 Byte Page**
  - **160 us Average Byte Write Time**
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - **$\overline{\text{DATA}}$ Polling**
- **On Chip Timer**
  - **Automatic Erase Before Write**
- **High Endurance**
  - **10,000 Cycles/Byte**
  - **10 Year Data Retention**
- **Power Up/Down Protection Circuitry**
- **200 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**
- **Military and Extended Temperature Range Available**

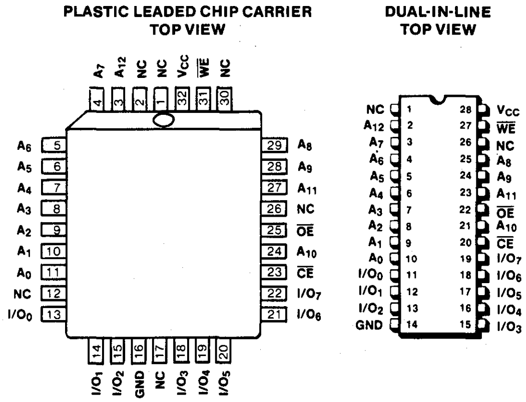
Description

SEEQ's 28C64 is a CMOS 5V only, 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Plastic Leaded Chip Carrier (PLCC). The 28C64 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. System reliability, in all applications, is higher because of the low failure rate of the Q Cell.

The 28C64 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the microprocessor



Pin Configuration


PLASTIC LEADED CHIP CARRIER TOP VIEW

DUAL-IN-LINE TOP VIEW

Pin Names

A_{0-5}	ADDRESSES—COLUMN
A_6-A_{12}	ADDRESSES—ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O$_{0-7}$	DATA INPUT (WRITE)/DATA OUTPUT (READ)
NC	NO CONNECTION

Q Cell is a trademark of SEEQ Technology, Inc.

for other tasks while the part is busy writing. The 28C64's write cycle time is 10 ms. An automatic erase is performed before a write. The $\overline{\text{DATA}}$ polling feature of the 28C64 can be used to determine the end of a write cycle. Once the write has been completed, data can be read in a maximum of 200 ns. Data retention is specified for 10 years.

Device Operation

Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

Mode Selection

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X X	V_{IL} X	X V_{IH}	HI Z/D_{OUT} HI Z/D_{OUT}
Chip Erase	V_{IL}	V_H	V_{IL}	X

X: Any TTL level
V_H: High Voltage

Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{\text{CE}}$ is brought to a TTL low in order to enable the chip. The $\overline{\text{WE}}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ($\overline{\text{OE}}$) to a TTL low. During read, the address, $\overline{\text{CE}}$, $\overline{\text{OE}}$, and I/O latches are transparent.

Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ($\overline{\text{WE}}$) pin of a selected ($\overline{\text{CE}}$ low) device. This combined with Output Enable ($\overline{\text{OE}}$) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurred last. Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurred first. An automatic erase is perfomed before data is written.

Write Cycle Control Pins

For system design simplification, the 28C64 is designed such that either the $\overline{\text{CE}}$ or $\overline{\text{WE}}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{\text{OE}}$ setup and hold are with respect to the later of $\overline{\text{CE}}$ or $\overline{\text{WE}}$; data setup and hold is with respect to the earlier of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

Write Mode

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the $\overline{\text{WE}}$ signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write initiated. These addresses and the $\overline{\text{OE}}$ state (high) are latched on the falling edge of $\overline{\text{WE}}$ signal. For proper write initiation and latching, the $\overline{\text{WE}}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{\text{WE}}$, allowing easy microprocessor interface.

Upon a low to high $\overline{\text{WE}}$ transition, the 28C64 latches data and starts the internal page load timer. The timer is reset on the falling edge of the $\overline{\text{WE}}$ signal if another write is initiated before the timer has timed out. The timer stays reset while the $\overline{\text{WE}}$ pin is kept low. If no additional write cycles have been initiated within t_{BLC} after the last $\overline{\text{WE}}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle ($\overline{\text{DATA}}$ polling).

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the 28C64 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining $\overline{\text{WE}}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{\text{CE}}$, $\overline{\text{OE}}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{\text{WE}}$, keeping this signal low will not start the page load timer. When $\overline{\text{WE}}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{\text{CE}}$ controlled write the same is true, with $\overline{\text{CE}}$ holding the timer reset instead of $\overline{\text{WE}}$.

$\overline{\text{DATA}}$ Polling

*The 28C64 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{\text{DATA}}$ polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C64 is **still writing,** the device will present the ones-complement of the last byte written. When the 28C64 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.*

A $\overline{\text{DATA}}$ polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. $\overline{\text{DATA}}$ polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a $\overline{\text{DATA}}$ polling read is the same as a normal read.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI}V*
2. *A high to low Write Enable ($\overline{\text{WE}}$) transition has not occurred when the V_{CC} supply is between V_{WI}V and V_{CC} with $\overline{\text{CE}}$ low and $\overline{\text{OE}}$ high.*

Writing will also be inhibited when $\overline{\text{WE}}$, $\overline{\text{CE}}$, or $\overline{\text{OE}}$ are in TTL logical states other than that specified for a write in the Mode Selection table.

*Absolute Maximum Stress Range**

Temperature
Storage .... −65°C to +150°C
Under Bias .... −10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs with respect to ground .... +6.0 V to −0.5 V
Undershoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground .... −1.0 V
Overshoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground .... +7.0 V

**COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	28C64
Temperature Range (Ambient)	0°C to 70°C
V_{CC} Power Supply	5 V ± 10%

Endurance and Data Retention

Symbol	**Parameter**	**Value**	**Units**	**Condition**
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

DC Characteristics (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	**Parameter**	**Limits**		**Units**	**Test Condition**
		Min.	**Max.**		
I_{CC}	Active V_{CC} Current		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.; Max read or write cycle time
I_{SB1}	Standby V_{CC} Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = ANY TTL LEVEL
I_{SB2}	Standby V_{CC} Current (CMOS Inputs)		150	μA	$\overline{CE} = V_{CC} - 0.3$ Other inputs = V_{IL} to V_{IH} All I/O Open
I_{IL}[2]	Input Leakage Current		1	μA	$V_{IN} = V_{CC}$ Max.
I_{OL}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu$A
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

Notes:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <10 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] $T_A = 25$ C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} =$ OV
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} =$ OV

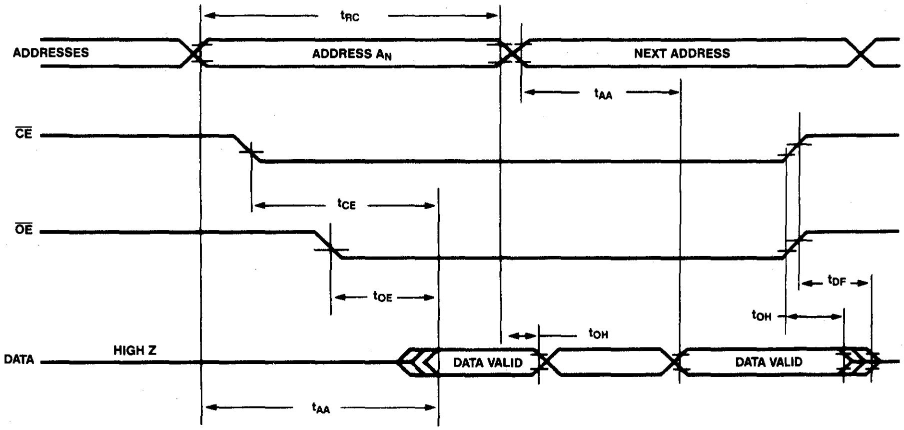
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

AC Characteristics Read Operation (Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	Parameter	Limits									Test Conditions
		28C64-200		28C64-250		28C64-300		28C64-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		80		90		90		90	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to output not being driven	0	60	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{\text{Data}}$ Polling Cycle Time



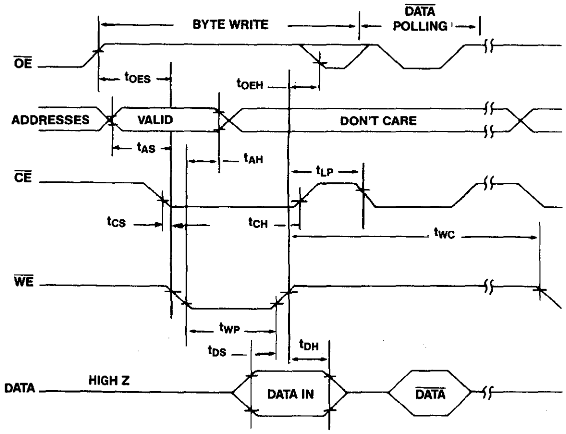
Notes:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

AC Characteristics Write Operation (Over the operating temperature and V_{CC} range, unless otherwise specified)

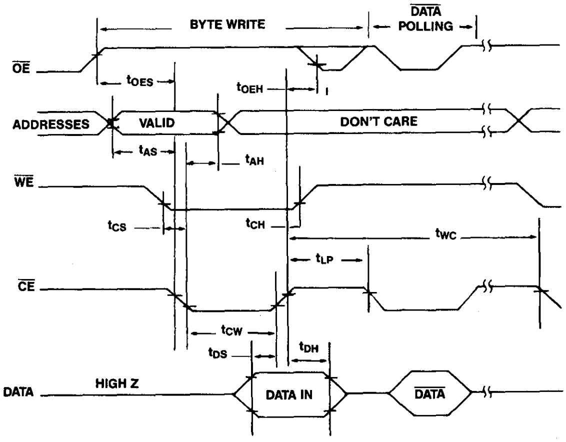
Symbol	Parameter	Limits								Units
		28C64-200		28C64-250		28C64-300		28C64-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Set-up Time	10		10		10		10		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	10		10		10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		10		10		10		ns
t_{WP}	$\overline{WE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (see note 3)	0.2	300	0.2	300	0.2	300	0.2	300	us
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		200		200		200		200	ns

Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



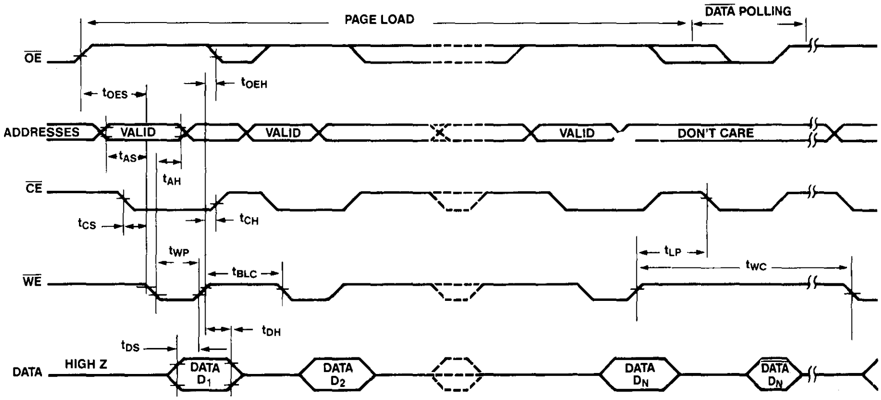
$\overline{CE}$ CONTROLLED WRITE CYCLE



Notes:

1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing



Ordering Information

D Q 28C64 - 250

PACKAGE
D = CERAMIC DIP
P = PLASTIC DIP
N = PLASTIC LEADED CHIP CARRIER
UX = UNENCAPSULATED DIE

TEMP. RANGE
Q–0°C to 70°C (COMMERCIAL)

PART TYPE
8K x 8 E²PROM

ACCESS TIME
200 = 200 ns
250 = 250 ns
300 = 300 ns
350 = 350 ns

seeq

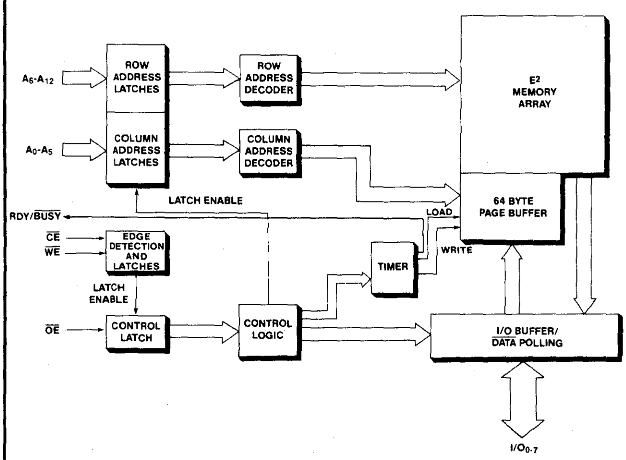
28C65
Timer E^2
64K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October, 1988

Features

- CMOS Technology
- Low Power
  - 50 mA Active
  - 150 μA Standby
- Page Write Mode
  - 64 Byte Page
  - 160 us Average Byte Write Time
- Byte Write Mode
- Write Cycle Completion Indication
  - $\overline{\text{DATA}}$ Polling
  - RDY/$\overline{\text{BUSY}}$ Pin
- On Chip Timer
  - Automatic Erase Before Write
- High Endurance
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- Power Up/Down Protection Circuitry
- 200 ns Maximum Access Time
- JEDEC Approved Byte Wide Pinout
- Military and Extended Temperature Range Available

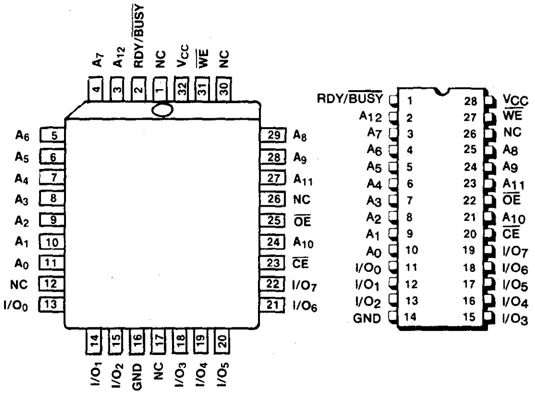


Description

SEEQ's 28C65 is a CMOS 5V only, 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Plastic Leaded Chip Carrier (PLCC). The 28C65 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. System reliability, in all applications, is higher because of the low failure rate of the Q Cell.

The 28C65 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the microprocessor

Pin Configuration



PLASTIC LEADED CHIP CARRIER TOP VIEW

DUAL-IN-LINE TOP VIEW

Pin Names

A_{0-5}	ADDRESSES — COLUMN
A_6-A_{12}	ADDRESSES ROW
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE) DATA OUTPUT (READ)
RDY/$\overline{\text{BUSY}}$	DEVICE READY/BUSY
NC	NO CONNECTION

Q Cell is a trademark of SEEQ Technology, Inc.

for other tasks while the part is busy writing. The 28C65's write cycle time is 10 ms. An automatic erase is performed before a write. The $\overline{DATA}$ polling feature of the 28C65 can be used to determine the end of a write cycle. Once the write has been completed, data can be read in a maximum of 200ns. Data retention is specified for 10 years.

Device Operation

Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

Mode Selection

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	RDY/$\overline{BUSY}$[1]
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	HI Z
Standby	V_{IH}	X	X	HI Z	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X	V_{IL}	X	HI Z/D_{OUT}	HI Z
	X	X	V_{IH}	HI Z/D_{OUT}	HI Z
Chip Erase	V_{IL}	V_H	V_{IL}	X	HI Z

X: Any TTL level
V_H: High Voltage

Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ($\overline{OE}$) to a TTL low. During read, the address, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This combined with Output Enable ($\overline{OE}$) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred last. Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ or CE, whichever occurred first. An automatic erase is perfomed before data is written.

Write Cycle Control Pins

For system design simplification, the 28C65 is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{OE}$ setup and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data setup and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC characteristics.

NOTES:

1. RDY/$\overline{BUSY}$ Pin 1 (Pin 2 on PLCC) has an open drain output and requires an external 3K resistor to V_{CC}. The value of the resistor is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Write Mode

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the WE signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write initiated. These addresses and the OE state (high) are latched on the falling edge of WE signal. For proper write initiation and latching, the WE pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of WE, allowing easy microprocessor interface.

Upon a low to high WE transition, the 28C65 latches data and starts the internal page load timer. The timer is reset on the falling edge of the WE signal if another write is initiated before the timer has timed out. The timer stays reset while the WE pin is kept low. If no additional write cycles have been initiated within t_{BLC} after the last WE low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle (DATA polling).

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the 28C65 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining WE low, assuming a write enable-controlled cycle, and leaving all other control inputs (CE, OE) in the proper page load cycle state. Since the page load timer is reset on the falling edge of WE, keeping this signal low will not start the page load timer. When WE returns high, the input data is latched and the page load cycle timer begins. In CE controlled write the same is true, with CE holding the timer reset instead of WE.

DATA Polling

The 28C65 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. DATA polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C65 is ***still writing,*** *the device will present the ones-complement of the last byte written. When the 28C65 has* ***completed*** *its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.*

A DATA polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. DATA polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a DATA polling read is the same as a normal read.

READY/BUSY Pin

28C65 provides write cycle status on this pin. RDY/BUSY output goes to a TTL low immediately after the falling edge of WE. RDY/BUSY will remain low during the byte load or page load cycle and continues to remain at a TTL low while the write cycle is in progress. An internal timer times out the required write cycle time and at the end of this time, the device signals RDY/BUSY pin to a TTL high. This pin can be polled for write cycle status or used to initate a rising edge triggered interrupt indicating write cycle completion. The RDY/BUSY pin is an open drain output and a typical 3 K pull-up resistor to V_{CC} is required. The pull-up value is dependent on the number of OR-tied RDY/BUSY pins. If RDY/BUSY is not used it can be left unconnected.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI}V*
2. *A high to low Write Enable (WE) transition has not occurred when the V_{CC} supply is between V_{WI}V and V_{CC} with CE low and OE high.*

Writing will also be inhibited when WE, CE, or OE are in TTL logical states other than that specified for a write in the Mode Selection table.

*Absolute Maximum Stress Range**

Temperature
Storage . . . . −65°C to +150°C
Under Bias . . . . −10°C to +80°C
D.C. Voltage applied to all Inputs or Outputs with respect to ground . . . . . . +6.0 V to −0.5 V
Undershoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground . . . . −1.0 V
Overshoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground . . . . +7.0 V

**COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	28C65
Temperature Range (Ambient)	0°C to 70°C
V_{CC} Power Supply	5 V ± 10%

Endurance and Data Retention

Symbol	**Parameter**	**Value**	**Units**	**Condition**
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

DC Characteristics (Over operating temperature and V_{CC} range, unless otherwise specified)

		Limits			
Symbol	**Parameter**	**Min.**	**Max.**	**Units**	**Test Condition**
I_{CC}	Active V_{CC} Current		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.; Max read or write cycle time
I_{SB1}	Standby V_{CC} Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = ANY TTL LEVEL
I_{SB2}	Standby V_{CC} Current (CMOS Inputs)		150	µA	$\overline{CE} = V_{CC} - 0.3$ Other inputs = V_{IL} to V_{IH} All I/O Open
I_{IL}[2]	Input Leakage Current		1	µA	$V_{IN} = V_{CC}$ Max.
I_{OL}	Output Leakage Current		10	µA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ µA
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

Notes:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.

AC Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <10 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] T_A = 25 C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	V_{IN} = OV
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O}$ = OV

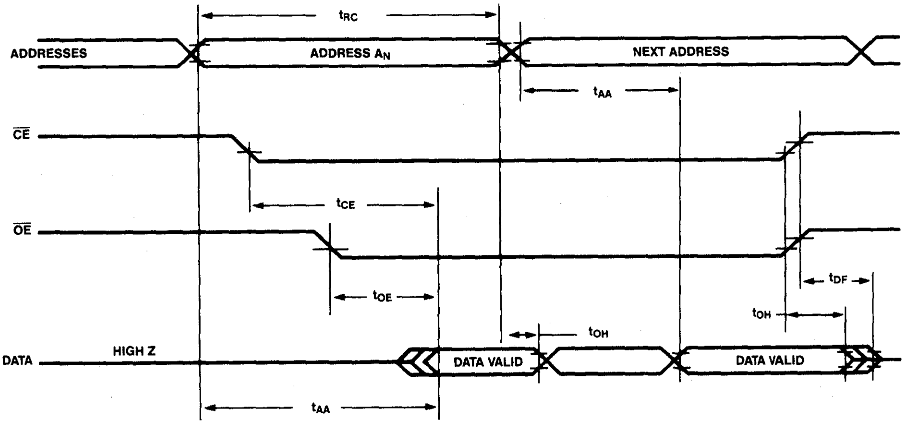
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

AC Characteristics *Read Operation* (Over operating temperature and V_{CC} Range, unless otherwise specified)

		Limits									
		28C65-200		28C65-250		28C65-300		28C65-350			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		80		90		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to output not being driven	0	60	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{\text{Data}}$ Polling Cycle Time



Notes:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

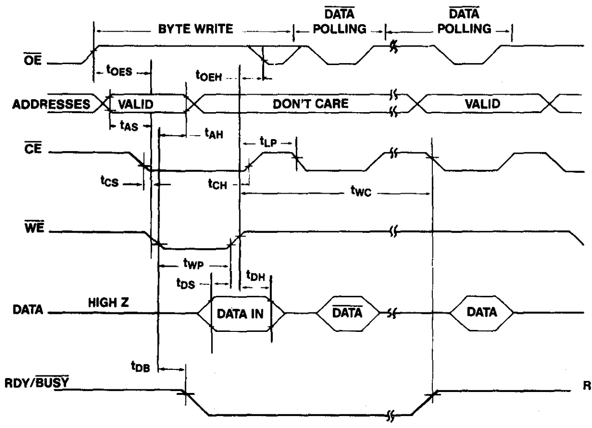
AC Characteristics

Write Operation (Over the operating V_{CC} and temperature range)

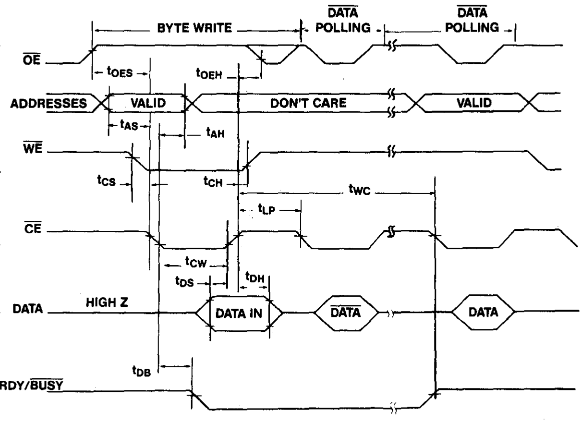
Symbol	Parameter	Limits								Units
		28C65-200		28C65-250		28C65-300		28C65-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Set-up Time	10		10		10		10		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	10		10		10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		10		10		10		ns
t_{WP}	$\overline{WE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	300	0.2	300	0.2	300	0.2	300	us
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		200		200		200		200	ns
t_{DB}	Time to Device Busy		100		100		100		100	ns

Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



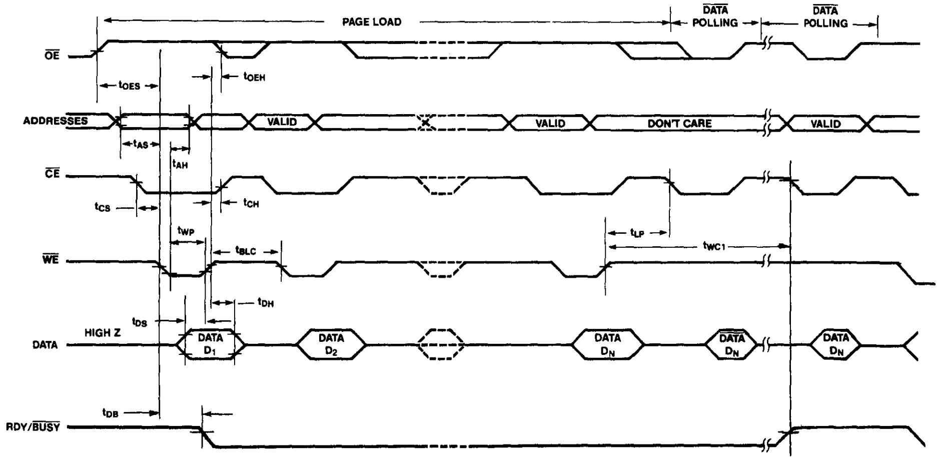
$\overline{CE}$ CONTROLLED WRITE CYCLE



NOTES:

1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating the internal write cycle.

Page Write Timing



Ordering Information

D Q 28C65 - 250

PACKAGE
D = CERAMIC DIP
P = PLASTIC DIP
N = PLASTIC LEADED CHIP CARRIER
UX = UNENCAPSULATED DIE

TEMP. RANGE
Q–0° to 70°C
(COMMERCIAL)

PART TYPE
8K x 8 E²PROM

ACCESS TIME
200 = 200 ns
250 = 250 ns
300 = 300 ns
350 = 350 ns

seeq

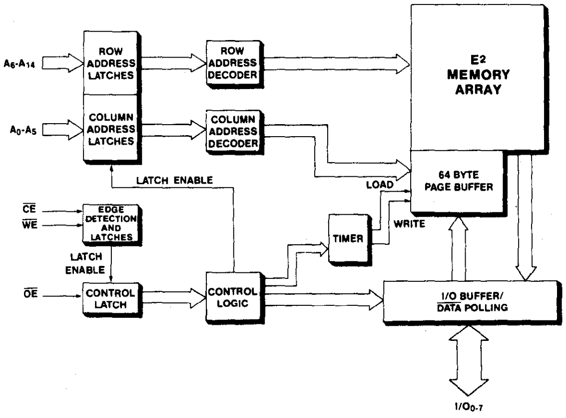
28C256
TimerE^2
256K Electrically Erasable PROM

PRELIMINARY DATA SHEET

November, 1988

Features

- **CMOS Technology**
- **Low Power**
  - 60 mA Active
  - 150 μA Standby
- **Page Write Mode**
  - 64 Byte Page
  - 160 us Average Byte Write Time
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - $\overline{\text{DATA}}$ Polling
- **On Chip Timer**
  - Automatic Erase Before Write
- **High Endurance**
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- **Power Up/Down Protection Circuitry**
- **200 ns Maximum Access Time**
- **Military and Extended Temperature Range Available.**



Q Cell is a trademark of SEEQ Technology, Inc.

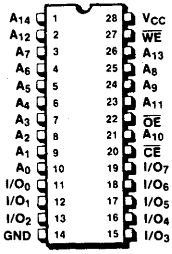
Description

SEEQ's 28C256 is a CMOS 5V only, 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Leadless Chip Carrier (LCC). The 28C256 is ideal for applications which require low power consumption, nonvolatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. System reliability, in all applications, is higher because of the low failure rate of the Q Cell.

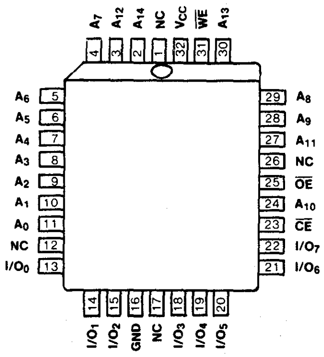
The 28C256 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the micro-

Pin Configuration

DUAL-IN-LINE
TOP VIEW



PLASTIC LEADED CHIP CARRIER
TOP VIEW



Pin Names

$A_{0\text{-}5}$	ADDRESSES — COLUMN
$A_{6\text{-}14}$	ADDRESSES — ROW
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
$I/O_{0\text{-}7}$	DATA INPUT (WRITE)/DATA OUTPUT (READ)

processor for other tasks while the part is busy writing. The 28C256's write cycle time is 10 ms maximum. An automatic erase is performed before a write. The $\overline{DATA}$ polling feature of the 28C256 can be used to determine the end of a write cycle. Once the write cycle has been completed, data can be read in a maximum of 200 ns. Data retention is greater than 10 years.

Device Operation

Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the a forementioned three input lines.

Table 1

Mode Selection

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X X	X V_{IL}	V_{IH} X	HI Z/D_{OUT} HI Z/D_{OUT}
Chip Erase	V_{IL}	V_{H}	V_{IL}	X

X: any TTL level
V_H: High Voltage

Reads

A read is typically accomplished by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ($\overline{OE}$) to a TTL low. During read, the addresses, $\overline{CE}$, $\overline{OE}$, and input data latches are transparent.

Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This combined with Output Enable ($\overline{OE}$) being high initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred last. Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred first. An automatic erase is performed before data is written.

The 28C256 can write both bytes and blocks of up to 64 bytes. The write mode is discussed below.

Write Cycle Control Pins

For system design simplification, the 28C256 is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{OE}$ set up and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data set up and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

Write Mode

One to 64 bytes of data can be randomly loaded into the device. The part latches row addresses, A6-A14, during the first byte write. These addresses are latched on the falling edge of the $\overline{WE}$ signal and are ignored after that until the end of t_{WC}. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write is initiated. These addresses and the $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the 28C256 latches data and starts the internal page load timer. The timer is reset on the falling edge of the $\overline{WE}$ signal if another write is initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no additional write cycles have been initiated in (t_{BLC}) after the last $\overline{WE}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can now be read to determine the end of write cycle ($\overline{DATA}$ Polling).

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the 28C256 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining $\overline{WE}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will inhibit the page load timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

$\overline{DATA}$ Polling

The 28C256 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C256 is ***still writing,*** *the device will present the ones-complement of the last byte written. When the 28C256 has* ***completed*** *its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. A $\overline{DATA}$ polling read should not be done until a minimum of t_{LP} microseconds after the last byte is written. Timing for a $\overline{DATA}$ polling read is the same as a normal read once the t_{LP} specification has been met.*

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI} V*
2. *A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.*

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

*Absolute Maximum Stress Range**

Temperature
Storage .... −65°C to +150°C
Under Bias .... −10°C to +80°C

D.C. Voltage applied to all Inputs or Outputs with respect to ground ...... +6.0 V to −0.5 V
Undershoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground .... −1.0 V
Overshoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground .... +7.0 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	28C256
Temperature Range	(Ambient) 0°C to 70°C
V_{CC} Supply Voltage	5 V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

DC Characteristics Read Operation *(Over operating temperature and V_{CC}Range, unless otherwise specified)*

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current		60	mA	$\overline{CE}=\overline{OE}=V_{IL}$; All I/O open; Other Inputs = V_{CC} Max. Min. read or write cycle time
I_{SB_1}	Standby V_{CC} Current (TTL Inputs)		2	mA	$\overline{CE}=V_{IH}$, $\overline{OE}=V_{IL}$; All I/O open; Other Inputs = V_{IL} to V_{IH}
I_{SB_2}	Standby V_{CC} Current (CMOS Inputs)		150	μA	$\overline{CE}=V_{CC}-0.3$ Other Inputs = V_{IL} to V_{IH} All I/O Open
I_{IL}[2]	Input Leakage Current		1	μA	$V_{IN}=V_{CC}$ Max.
I_{OL}[3]	Output Leakage Current		10	μA	$V_{OUT}=V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL}=2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH}=-400$ μA
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

NOTES:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.
3. For I/O only.

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <10 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

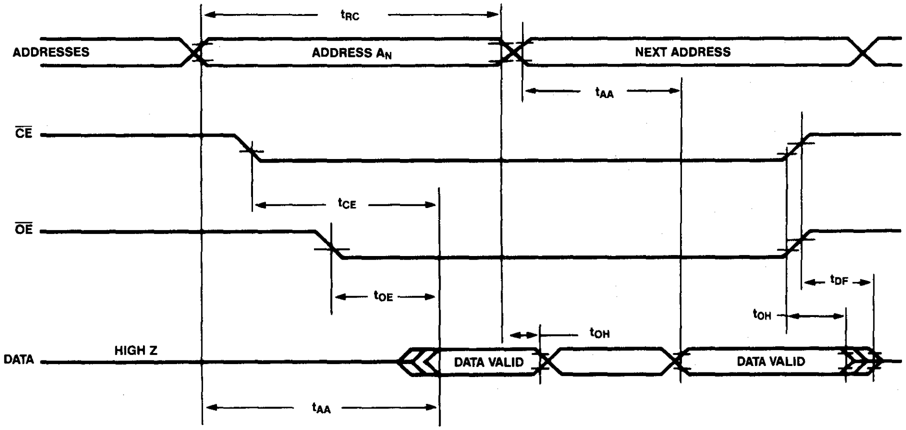
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	> 2000 V.	MIL-STD 883 Test Method 3015

AC Characteristics *Read Operation* (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits									Test Conditions
		28C256-200		28C256-250		28C256-300		28C256-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		80		90		90		90	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to output in Hi-Z	0	60	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{\text{DATA}}$ Polling Cycle

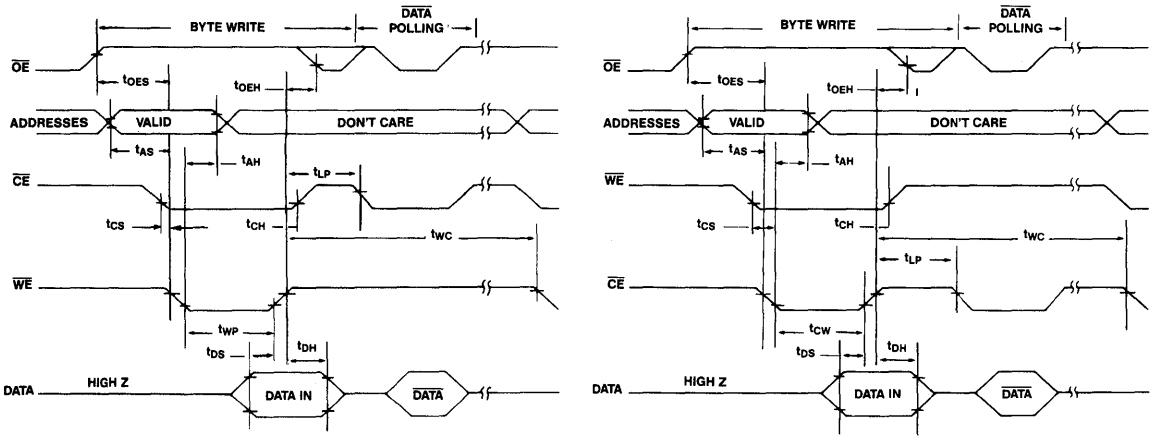


Notes:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

AC Characteristics Write Operation (Over the operating temperature and V_{CC} range, unless otherwise specified)

		Limits								
		28C256-200		28C256-250		28C256-300		28C256-350		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WC}	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Set-up Time	20		20		20		20		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	20		20		20		20		ns
t_{OEH}	$\overline{OE}$ High Hold Time	20		20		20		20		ns
t_{WP}	$\overline{WE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	300	0.2	300	0.2	300	0.2	300	us
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling Output		600		600		600		600	us

Write Timing



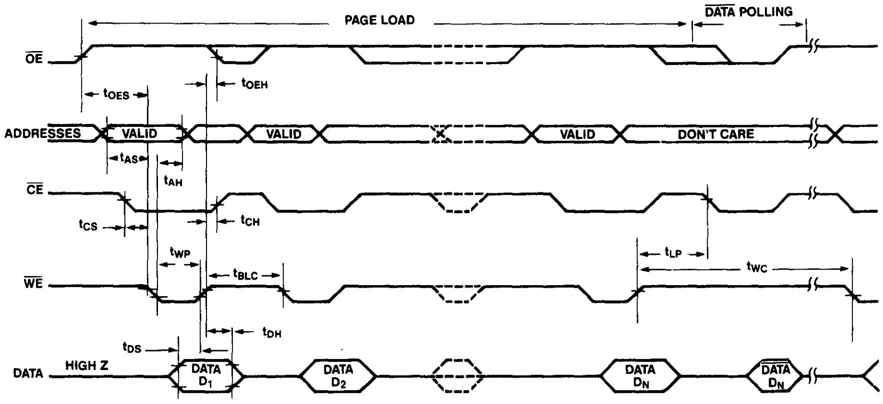
$\overline{WE}$ CONTROLLED WRITE CYCLE

$\overline{CE}$ CONTROLLED WRITE CYCLE

Notes:

1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing



Ordering Information

D Q 28C256 -250

PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME
P - PLASTIC DIP D - CERAMIC DIP N - PLASTIC LEADED CHIP CARRIER UX - UNENCAPSULATED DIE	Q - 0°C to +70°C (Commercial)	32K x 8 EEPROM	200 = 200 ns 250 = 250 ns 300 = 300 ns 350 = 350 ns

seeq

28C64A
High Speed CMOS 64K Electrically Erasable PROM

PRODUCT PREVIEW

October, 1988

Features

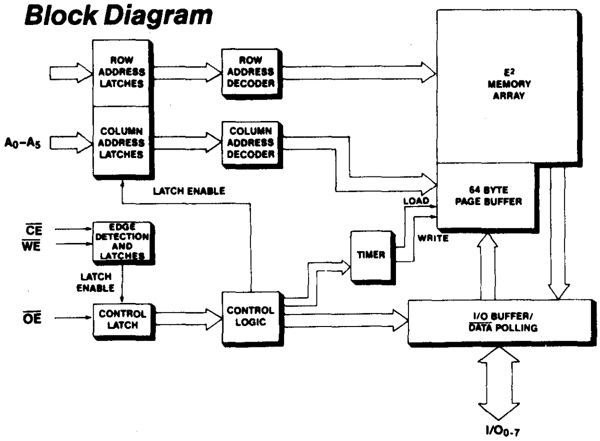
- ***High Speed: 90, 120, 150 ns Access Times***
- ***Commercial and Military Temperature Ranges***
- ***CMOS Technology***
- ***Low Power***
  - ***300 mW (Typical)***
  - ***Less than 1 mW Standby***
- ***Page Write Mode: 64 Byte Page***
- ***Fast Write: 5ms Byte/Page Write Time***
- ***Write Cycle Completion Indication***
  - ***$\overline{\text{DATA}}$ Polling of Data Bit 7***
- ***On Chip Timer***
  - ***Automatic Erase Before Write***
- ***High Endurance***
  - ***10,000 Cycles/Byte Minimum***
  - ***10 Year Data Retention***
- ***Power Up/Down Protection Circuitry***
- ***JEDEC Approved Byte-Wide Pinout***

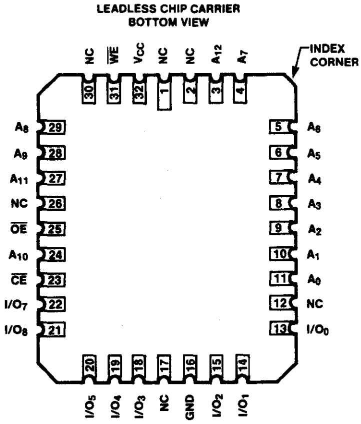
Description

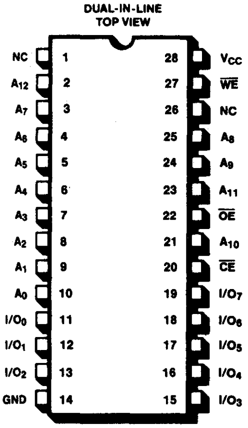
SEEQ's 28C64A is a high speed CMOS 5V only, 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS process and is available in 28 pin Cerdip, Plastic DIP packages and 32 pin LCC, PLCC. The 28C64A is ideal for high speed applications which require low power consumption, non-volatility and in-system reprogrammability. The endurance, the number of times which a byte may be written, is specified at 10,000 cycles per byte minimum.

The 90 ns, 120 ns, 150 ns access times meet the requirements of many of today's high performance microprocessors. The 28C64A has an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. The 28C64A's write cycle time is 5 msec typical. An automatic erase is performed before a write. The $\overline{\text{Data}}$ Polling feature of the 28C64A can be used to determine the end of a write cycle. All inputs are CMOS/TTL for both write and read modes. Data retention is specified to be greater than 10 years.

Block Diagram







Pin Names

A_0-A_5	ADDRESSES–COLUMN
A_6-A_{12}	ADDRESSES–ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/DATA OUTPUT (READ)
NC	NO CONNECT

seeq

28C256A
High Speed CMOS
256K Electrically Erasable PROM

PRODUCT PREVIEW

October, 1988

Features

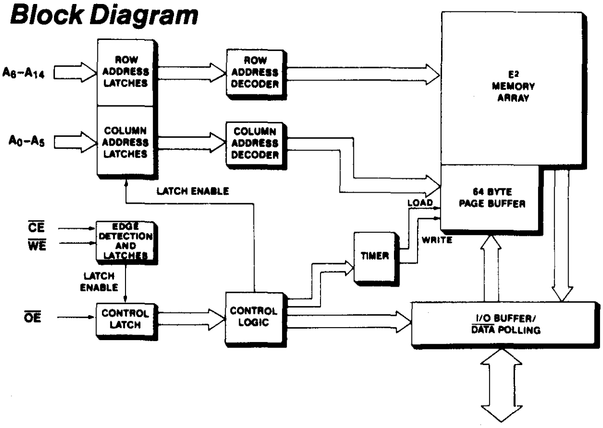
- **High Speed: 90, 120, 150 ns Access Times**
- **Commercial and Military Temperature Ranges**
- **CMOS Technology**
- **Low Power**
  - **300 mW (Typical)**
  - **Less than 1 mW Standby**
- **Page Write Mode: 64 Byte Page**
- **Fast Write: 5ms Byte/Page Write Time**
- **Write Cycle Completion Indication**
  - **$\overline{\text{DATA}}$ Polling of Data Bit 7**
- **On Chip Timer**
  - **Automatic Erase Before Write**
- **High Endurance**
  - **10,000 Cycles/Byte**
  - **10 Year Data Retention**
- **Power Up/Down Protection Circuitry**
- **JEDEC Approved Byte-Wide Pinout**

Description

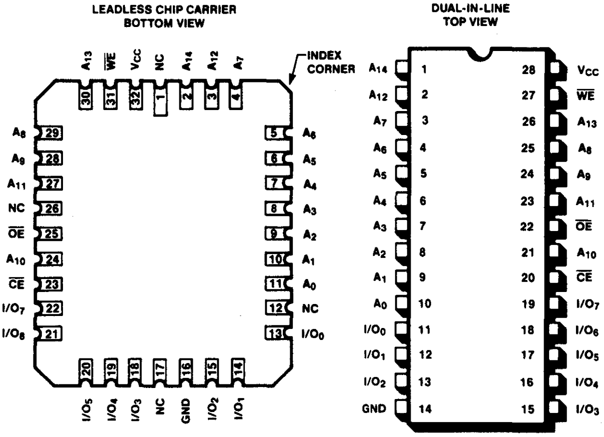
SEEQ's 28C256A is a high speed CMOS 5V only, 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS process and is available in 28 pin Cerdip, Plastic DIP packages and 32 pin LCC, PLCC. The 28C256A is ideal for high speed applications which require low power consumption, non-volatility and in-system reprogrammability. The endurance, the number of times which a byte may be written, is specified at 10,000 cycles per byte minimum.

The 90 ns, 120 ns, 150 ns maximum access times meet the requirements of many of today's high performance microprocessors. The 28C256A has an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. The 28C256A's write cycle time is 5 msec typical. An automatic erase is performed before a write. The $\overline{\text{DATA}}$ Polling feature of the 28C256A can be used to determine the end of a write cycle. All inputs are CMOS/TTL for both write and read modes. Data retention is specified to be greater than 10 years.

Block Diagram



Pin Configuration



Pin Names

A_0-A_5	ADDRESSES—COLUMN
A_6-A_{14}	ADDRESSES—ROW
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/DATA OUTPUT (READ)
NC	NO CONNECT

seeq

36C16
36C32

High Speed CMOS Electrically Erasable PROM

PRELIMINARY DATA SHEET *October, 1988*

Features

- ***High Speed:***
  - ***35 ns Maximum Access Time***
- ***CMOS Technology***
- ***Low Power:***
  - ***350 mW***
- ***10 Year Data Retention***
- ***High Output Drive***
  - ***Sink 16 mA at 0.45 V***
  - ***Source 4 mA at 2.4 V***
- ***5 V ± 10% Power Supply***
- ***Power Up/Down Protection Circuitry***
- ***Fast Byte Write***
  - ***5 ms/Byte***
- ***Automatic Byte Clear Before Write***
- ***JEDEC Approved PROM Pinout***
- ***Direct Replacement for Bipolar PROMs***
- ***Slim 300 mil Packaging Available***
- ***Military and Extended Temperature Range Available.***

Description

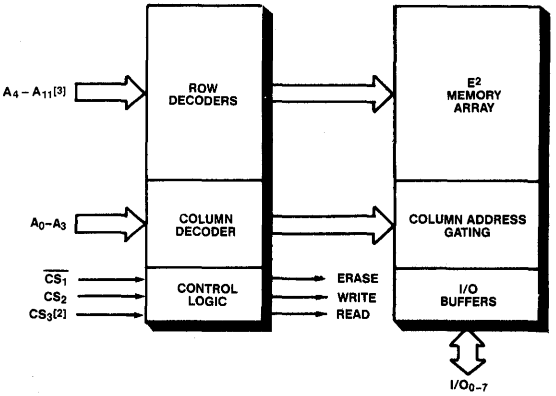
SEEQ's 36C16/32 are high speed 2K x 8/4K x 8 Electrically Erasable Programmable Read Only Memories, manufactured using SEEQ's advanced 1.25 micron CMOS Process.

The 36C16/32 are intended as bipolar PROM replacements in high speed applications. The 35ns maximum read access time meets the requirements of many of today's high performance processors. The endurance, the number of times the part can be erased/written, is specified to be greater than 100 cycles. The 36C16/32 are built using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design.

Data retention is specified to be greater than 10 years.

The 36C16/32 are available in 24 pin Slim 300 mil CERAMIC DIP and PLASTIC DIP. 24/28 pin full featured EEPROM versions are also available (38C16/32). All parts are available in commercial as well as military temperature ranges.

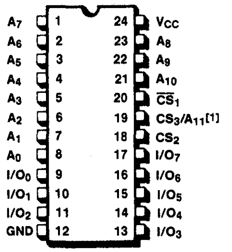
Block Diagram



Pin Configuration

DUAL-IN-LINE TOP VIEW

36C16/36C32
(24 pins)



NOTES: 1. Pin 19 is A_{11} on the 36C32.
2. CS_3 is on the 36C16 only.
3. A_4–A_{10} on 36C16

Pin Names

A_0-A_3	ADDRESSES — COLUMN
A_4-A_{11}[3]	ADDRESSES — ROW
$\overline{CS}_1$ CS_2 CS_3	CHIP SELECT INPUTS
I/O	DATA INPUT (WRITE) DATA OUTPUT (READ)

Q Cell is a trademark of SEEQ Technology, Inc.

Device Operation
Operational Modes

MODE PIN	$\overline{CS}_1$	CS_2	CS_3[2]	I/O
Read	V_{IL}	V_{IH}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
	X	V_{IL}	X	
	X	X	V_{IL}	
Write	V_H[1]	V_{IL}	X	D_{IN}

X: Any TTL level

Read

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable, the chip select inputs should be brought to the proper levels in order to enable the outputs (see Table above).

Write

To write into a particular location, addresses and data must be valid, CS_2 must be TTL low and a V_H[1] pulse has to be applied to $\overline{CS}_1$ for 5ms. An automatic internal byte clear is done prior to the byte write. The byte clear feature is transparent to the user.

NOTES:

1. V_H - High Voltage
2. CS_3 applies only to the 36C16. This pin becomes A_{11} in the 36C32.

Absolute Maximum Rating

Temperature	
Storage	*– 65°C to + 150°C*
Under Bias	*– 10°C to + 80°C*
All Inputs and Outputs with Respect to Ground	*– 3.V to + 7 V D.C.*
$\overline{CS}_1$ with Respect to Ground	*– 0.5 V to + 14 V D.C.*

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	36C16 **36C32**
V_{CC} Supply Voltage	5 V ± 10%
Temperature Range (Read Operation)	0°C to 70°C (Ambient)

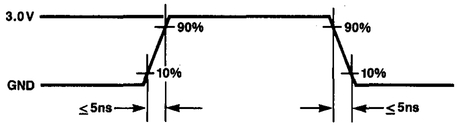
DC Operating Characteristics (Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	**Parameter**	**Limits**		**Unit**	**Test Condition**
		Min.	**Max.**		
I_{CC}	V_{CC} Active Current		80	mA	$CS_2 = CS_3 = V_{IH}$; $\overline{CS}_1 = V_{IL}$; Address Inputs = 20MHz I/O = 0mA
I_{IN}	Input Leakage Current		1	μA	0.1 V > = V_{IN} < = V_{CC} Max.
I_{OUT}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	– 0.5	0.8	V	
V_{IH}	Input High Voltage	2	6.5	V	V_{CC} Min.
V_H	Input High Voltage During Write	10.8	13.2	V	For $\overline{CS}_1$ Input Only
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 16$ mA, $V_{CC} = V_{CC}$ Min.
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -4$ mA, $V_{CC} = V_{CC}$ Min.
I_{OS}[1][2]	Output Short Circuit Current	– 20		mA	$V_{CC} = V_{CC}$ Max, $V_{OUT} = 0$
V_{CI}[2]	Input Undershoot Voltage	– 3		V	V_{IN} undershoot pulse width < 10ns

NOTE:
1. Only one pin at a time for less than one second.
2. Characterized. Not Tested.

AC Test Conditions

Output Load: 10 TTL gates and total $C_L = 30pF$
Input Rise and Fall Times: < 5ns
Input Pulse Levels: 0V to 3V
Timing Measurement Reference Level:
Inputs 1.5V
Outputs 1.5V



INPUT PULSES

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

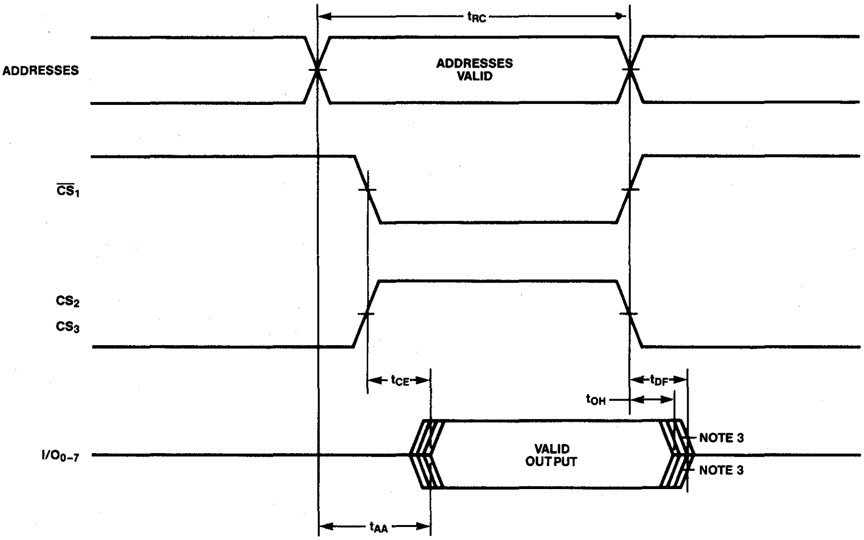
Capacitance[1] T_A=25°C, f=1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

AC Characteristics Read Operation (Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	Parameter	36C16-35 36C32-35 Min.	36C16-35 36C32-35 Max.	36C16-40 36C32-40 Min.	36C16-40 36C32-40 Max.	36C16-45 36C32-45 Min.	36C16-45 36C32-45 Max.	36C16-55 36C32-55 Min.	36C16-55 36C32-55 Max.	Units
t_{RC}	Read Cycle Time	35		40		45		55		ns
t_{CE}	Chip Select Access Time		25		25		30		35	ns
t_{AA}	Address Access Time		35		40		45		55	ns
t_{DF}	Output Enable to Output not being driven		25		25		25		30	ns
t_{OH}	Output Hold from Address Change or Chip Select whichever occurs first	0		0		0		0		ns

Read Cycle Timing



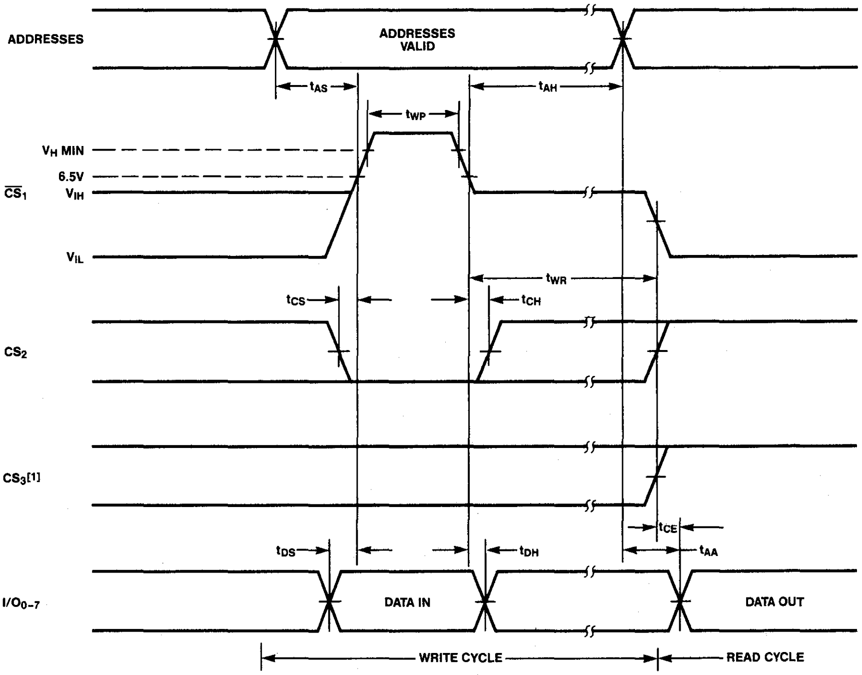
NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not Tested.
3. Transition is measured at steady state level −0.5V or steady state low level +0.5V on the output from the 1.5V level on the input.

AC Characteristics Write Operation (All Speeds)

(Over V_{CC} Range, $T_A = 25° \pm 5°C$ unless otherwise specified)

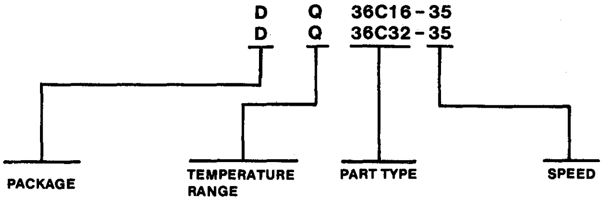
Symbol	Parameter	36C16 36C32 Min.	36C16 36C32 Max.	Units
t_{WP}	Write Pulse Width	5	50	ms
t_{AS}	Address Set-up Time	0		µs
t_{AH}	Address Hold Time	0.5		µs
t_{CS}	CS_2 Set-up Time	0		µs
t_{CH}	CS_2 Hold Time	0		µs
t_{DS}	Data Set-up Time	0		µs
t_{DH}	Data Hold Time	0		µs
t_{WR}	Write Recovery		10	µs

Write Cycle Timing



NOTE:
1. CS_3 is A_{11} on 36C32.

Ordering Information



PACKAGE	TEMPERATURE RANGE	PART TYPE	SPEED
D-SLIM CERAMIC DIP	Q-0°C to 70°C (COMMERCIAL)	36C16-2K x 8 EEPROM	35-35 ns
P-SLIM PLASTIC DIP		36C32-4K x 8 EEPROM	45-45 ns
			55-55 ns

SEEQ

38C16
38C32

High Speed CMOS Electrically Erasable PROM

PRELIMINARY DATA SHEET

October, 1988

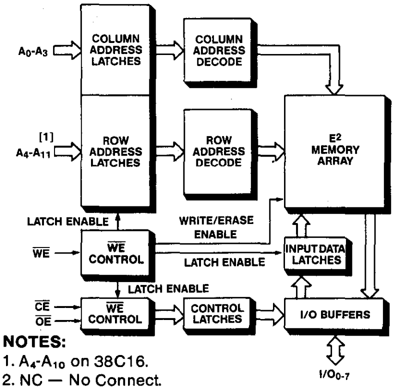
Features

- ***High Speed:***
  - ***35 ns Maximum Access Time***
- ***CMOS Technology***
- ***Low Power:***
  - ***350 mW***
- ***High Endurance:***
  - ***10,000 Cycles/Byte Minimum***
  - ***10 Year Data Retention***
- ***On-Chip Timer and Latches***
  - ***Automatic Byte Erase Before Write***
  - ***Fast Byte Write: 5 ms/Byte***
- ***High Speed Address/Data Latching***
- ***50 ms Chip Erase***
- ***5 V ± 10% Power Supply***
- ***Power Up/Down Protection Circuitry***
- ***$\overline{\text{DATA}}$ Polling of Data Bit 7***
- ***JEDEC Approved Byte Wide Pinout***
  - ***38C16: 2816A Pin Compatible***
  - ***38C32: 28C64 Pin Compatible***
- ***Military and Extended Temperature Range Available.***

Pin Names

A_0-A_3	ADDRESSES — COLUMN
A_4-A_{11}[1]	ROW ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
$I/O_{0\text{-}7}$	DATA INPUT (WRITE) DATA OUTPUT (READD)

Block Diagram



NOTES:

1. A_4-A_{10} on 38C16.
2. NC — No Connect.

Description

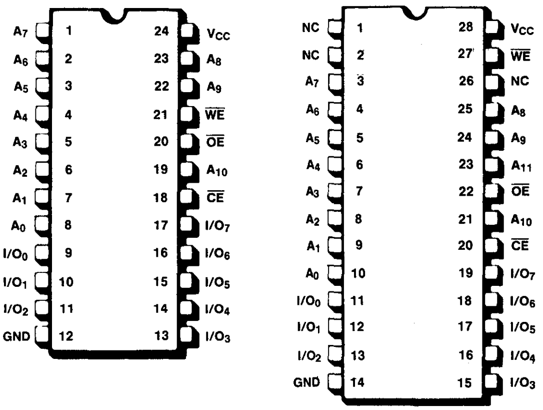
SEEQ's 38C16/32 are high speed 2K × 8/4K × 8 Electrically Erasable Programmable Read Only Memories (EEPROM), manufactured using SEEQ's advanced 1.25 micron CMOS process.

The 38C16/32 are ideal for high speed applications which require non-volatility and in-system reprogrammability. The endurance, the number of times a byte may be written, is specified at 10,000 cycles per byte minimum. The high endurance is accomplished using

Pin Configuration

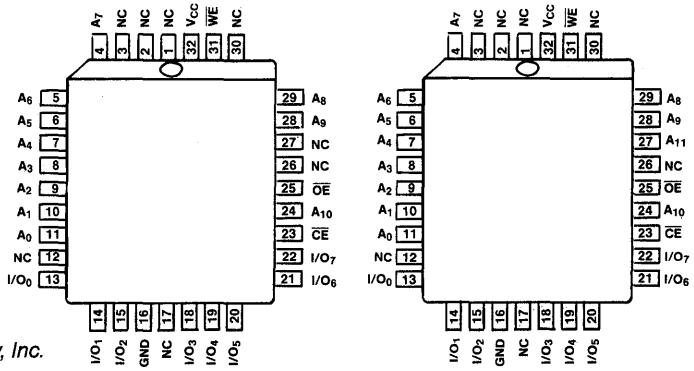
DUAL-IN-LINE TOP VIEW

38C16 (24 pins) **38C32** (28 pins)



PLASTIC LEADED CHIP CARRIER TOP VIEW

38C16 **38C32**



Q Cell is a trademark of SEEQ Technology, Inc.

SEEQ's proprietary oxynitride EEPROM process and its innovative "DQ cell" design. System reliability in applications where writes are frequent is increased because of the DQ-cell. The 35 ns maximum access time meets the requirements of many of today's high performance processors. The 38C16/32 have an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. $\overline{DATA}$ polling can be used to determine the end of a write cycle. All inputs are TTL compatible for both write and read modes.

Data retention is specified to be greater than 10 years.

The 38C16 and 38C32 are both available in CERAMIC DIP, PLASTIC DIP and PLCC packages. 24 pin versions of both 38C16 and 38C32 intended for bipolar PROM replacement are also available (36C16/36C32). All parts are available in commercial as well as military temperature ranges.

Device Operation
Operational Modes

MODE PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X V_{IH} X V_{IL}	X X V_{IL} V_{IL}	V_{IH} X V_{IH} V_{IL}	HI Z/D_{OUT} HI Z HI Z/D_{OUT} No Operation (HI Z)
Chip Erase[1]	V_{IH}	V_H[2]	V_{IH}	HI Z

X: Any TTL level

Read

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{OE}$) to a TTL low. During read, the address, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

Write

To write into a particular location, addresses must be valid and a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This initiates a write cycle. During a write cycle, all inputs except for data are latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$, whichever one occurred last). Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$, which ever one occurred first). An automatic byte erase is performed before data is written.

$\overline{DATA}$ Polling

The EEPROM has a specified t_{WC} write cycle time of 5ms. The typical device has a write cycle time faster than the t_{WC}. $\overline{DATA}$ polling is a method to indicate the completion of a timed write cycle. During the internal write cycle, the complement of the data bit 7 is presented at output 7 when a read is performed. Once the write cycle is finished, the true data is presented at the outputs. A software routine can be used to "poll", i.e. read the output, for true or complemented data bit 7. The polling cycle specifications are the same as for a read cycle. During data polling, the addresses are don't care.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

Protection against false write during V_{CC} power up/down is provided through on chip circuitry. Writing is prevented under any one of the following conditions:

1. *V_{CC} is less than V_{WI} V.*
1. *A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.*

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than those specified for a byte write in the Mode Selection table.

NOTES:

1. Chip erase is an optional mode.
2. V_H — High Voltage.

Absolute Maximum Rating

Temperature
Storage . . . . – 65°C to + 150°C
Under Bias . . . . – 10°C to + 80°C
All Inputs and Outputs
with Respect to Ground . . . . – 3. V to + 7 V D.C.

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	38C16 **38C32**
V_{CC} Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

Endurance and Data Retention

Symbol	**Parameter**	**Value**	**Units**	**Condition**
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

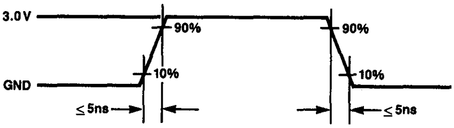
DC Operating Characteristics (Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	**Parameter**	**Limits**		**Unit**	**Test Condition**
		Min.	**Max.**		
I_{CC}	V_{CC} Active Current		80	mA	$\overline{CE} = \overline{OE} = V_{IL}$; Address Inputs = 20MHz I/O = 0mA
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$; All I/O open; All other inputs TTL don't care;
I_{IN}	Input Leakage Current		1	μA	$0.1V >= V_{IN} <= V_{CC}$ Max.
I_{OUT}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	– 0.5	0.8	V	
V_{IH}	Input High Voltage	2	6.5	V	V_{CC} Min.
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA, $V_{CC} = V_{CC}$ Min.
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA, V_{CC} Min.
V_{WI}[1]	Write Inhibit Voltage	3.8		V	
V_{CL}[1]	Input Undershoot Voltage	– 3		V	V_{IN} undershoot pulse width < 10ns

NOTES:
1. Characterized. Not tested.

AC Test Conditions

Output Load: 1 TTL gate and total $C_L = 30pF$
Input Rise and Fall Times: <5ns
Input Pulse Levels: 0V to 3V
Timing Measurement Reference Level:
Inputs 1.5V
Outputs 1.5V



INPUT PULSES

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000V	MIL-STD 883 Test Method 3015

Capacitance[1] $T_A = 25°C$, f=1 MHz

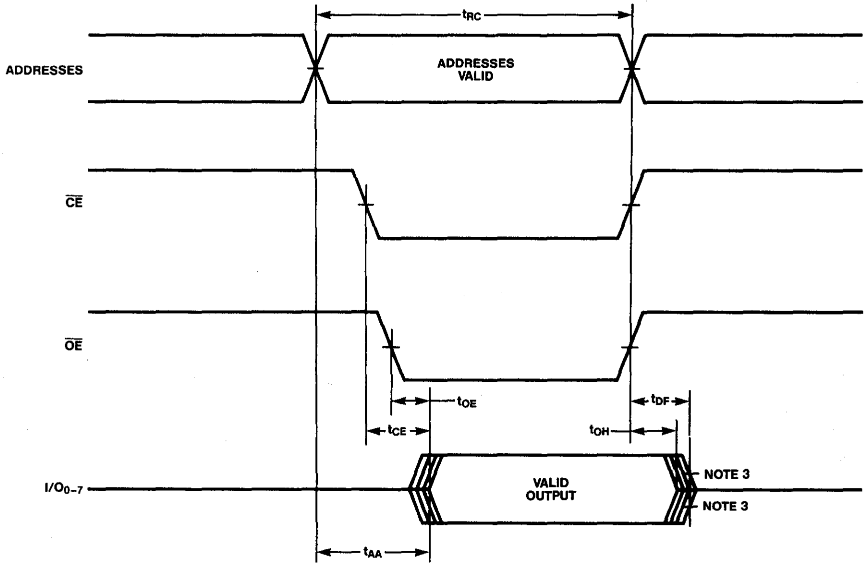
Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

AC Characteristics Read Operation

(Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	Parameter	Limits 38C16-35 38C32-35 Min.	Limits 38C16-35 38C32-35 Max.	38C16-40 38C32-40 Min.	38C16-40 38C32-40 Max.	38C16-45 38C32-45 Min.	38C16-45 38C32-45 Max.	38C16-55 38C32-55 Min.	38C16-55 38C32-55 Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	35		40		45		55		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		25		25		30		35	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		35		40		45		55	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		20		20		25		30	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable to Output Float not being Driven		15		15		25		30	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable or Output Enable whichever occurs first	0		0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

Read Cycle Timing



NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not Tested.
3. Transition is measured at steady state level −0.5V or steady state low level +0.5V on the output from the 1.5V level on the input.

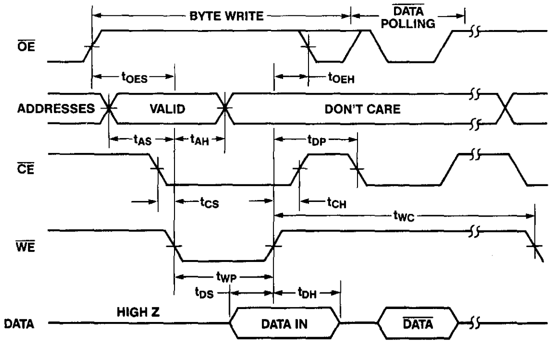
AC Characteristics Write Operation

(Over operating temperature and V_{CC} Range, unless otherwise specified)

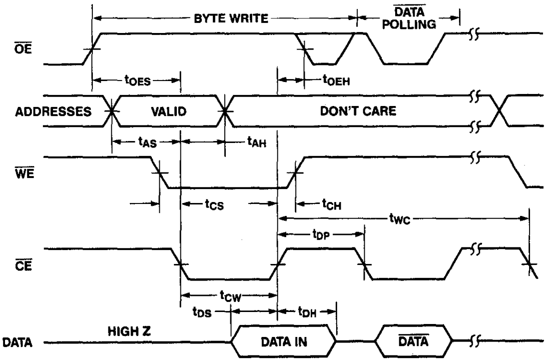
Symbol	Parameter	38C16-35 38C32-35		38C16-40 38C32-40		38C16-45 38C32-45		38C16-55 38C32-55		Units
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
t_{WC}	Write Cycle Time		5		5		5		5	ms
t_{AS}	Address Set-up Time	0		0		0		0		ns
t_{AH}	Address Hold Time	25		25		25		30		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width	20		20		25		30		ns
t_{OES}	$\overline{OE}$ High Set-up Time	5		5		5		5		ns
t_{OEH}	$\overline{OE}$ High Hold Time	0		0		0		0		ns
t_{WP}	$\overline{WE}$ Pulse Width	20		20		25		30		ns
t_{DS}	Data Set-up Time	20		20		25		30		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{DP}	Time to $\overline{DATA}$ Polling from Byte Latch		35		40		45		55	ns

Write Cycle Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



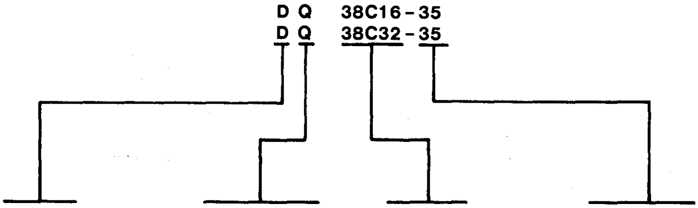
$\overline{CE}$ CONTROLLED WRITE CYCLE



NOTES:

1. Address hold time is with respect to the falling edge of the control signal WE or CE.

Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME
D - CERAMIC DIP	Q - 0°C to 70°C (COMMERCIAL)	38C16 - 2K x 8 EEPROM	35 - 35 ns
P - PLASTIC DIP		38C32 - 4K x 8 EEPROM	40 - 40 ns
N - PLCC			45 - 45 ns
			55 - 55 ns

seeq

28C010
CMOS Timer E^2
1024K Electrically Erasable PROM

PRODUCT PREVIEW

October, 1988

Features

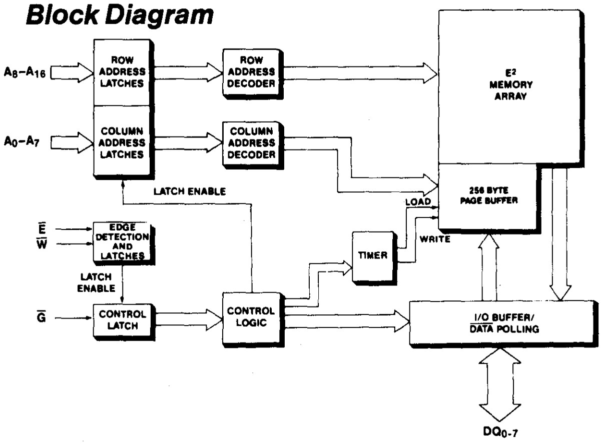
- ***Fast Access Times: 150, 200 ns***
- ***Commercial and Military Temperature Ranges***
- ***CMOS Technology***
- ***Low Power***
  - ***300 mW***
  - ***Less than 1 mW Standby***
- ***Page Write Mode: 256 Byte Page***
- ***Fast Write: 5ms Byte/Page Write Time***
- ***Write Cycle Completion Indication***
  - ***$\overline{\text{DATA}}$ Polling***
- ***On Chip Timer***
  - ***Automatic Erase Before Write***
- ***High Endurance***
  - ***10,000 Cycles/Byte***
  - ***10 Year Data Retention***
- ***Power Up/Down Protection Circuitry***
- ***JEDEC Approved Byte-Wide Pinout***

Description

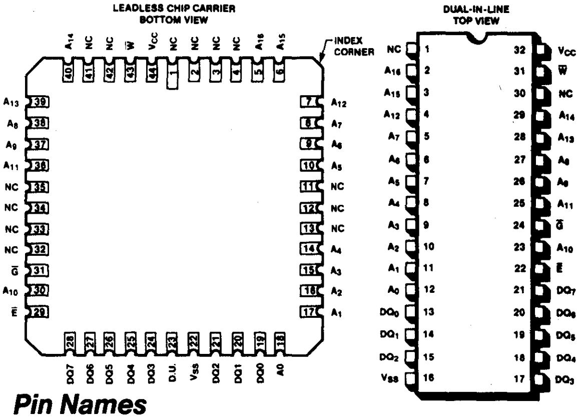
SEEQ's 28C010 is a CMOS 5V only, 128K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS process and is available in both a 32 pin Cerdip package as well as a 44-pin LCC. The 28C010 is ideal for applications which require low power consumption, non-volatility and in-system reprogrammability. The endurance, the number of times which a byte may be written, is specified at 10,000 cycles per byte minimum.

The 28C010 has an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. The 28C010's write cycle time is 5 msec typical. An automatic erase is performed before a write. The $\overline{\text{DATA}}$ Polling feature of the 28C010 can be used to determine the end of a write cycle. All inputs are CMOS/TTL for both write and read modes. Data retention is greater than 10 years.

Block Diagram



Pin Configuration



Pin Names

A_0-A_7	ADDRESSES—COLUMN
A_8-A_{16}	ADDRESSES—ROW
$\overline{E}$	CHIP ENABLE
$\overline{G}$	OUTPUT ENABLE
$\overline{W}$	WRITE ENABLE
D/Q_{0-7}	DATA INPUT (WRITE)/DATA OUTPUT (READ)
NC	NO CONNECT
DU	DON'T USE

seeq

MODULES Q/E28C010
Timer E^2
1024K *Electrically Erasable PROM*

PRELIMINARY DATA SHEET

October 1988

Features

- ***CMOS Technology***
- ***Military Temperature Range***
- ***Low Power Operation***
  - ***70 mA Active Current***
  - ***2 mA Standby Current***
- ***On-Chip Timer***
  - ***Automatic Erase Before Write***
- ***64 Byte Page Mode. . . Fast Effective Write Time***
  - ***80 μsec Average Byte Write Time***
- ***Write Cycle Completion Indication***
  - ***$\overline{\text{Data}}$ Polling***
- ***5V ± 10% Power Supply***
- ***Power Up/Power Down Protection Circuitry***
- ***JEDEC Approved Byte Wide Pinout***

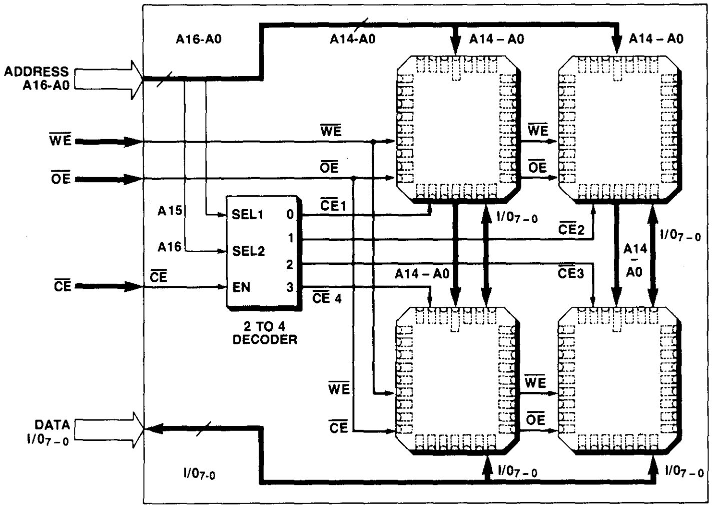
Description

SEEQ's MQ/ME28C010 is a CMOS 5V only, 128K × 8 Electrically Erasable Programmable Read Only Memory (EEPROM). The MQ/ME28C010 consists of 4 28C256 (32K × 8) CMOS EEPROMs and a 2 to 4 line decoder in LCC packages, mounted on and interconnected on a ceramic substrate. The MQ/ME28C010 is available in a 32 pin module package and is ideal for applications which require low power consumption, non-volatility and in-system reprogrammability.

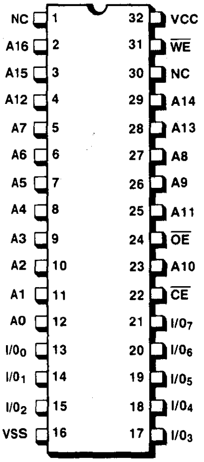
Pin Names

A16-A0	ADDRESSES
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O	DATA INPUT (WRITE)/DATA OUTPUT (READ)

Block Diagram



Pin Configuration



The MQ/ME28C010 has an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. The MQ/ME28C010's write cycle time is 10msec maximum. An automatic erase is performed before a write. The $\overline{\text{Data}}$ Polling feature of the MQ/ME28C010 can be used to determine the end of a write cycle. Data retention is greater than 10 years.

Device Operation

Operational Modes

There are four operational modes (see Table 1); only TTL inputs are required. Write can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the forementioned three input lines.

Table 1

Mode Selection

Mode Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
READ	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
STANDBY	V_{IH}	X	X	HI-Z
WRITE	V_{IL}	V_{IH}	V_{IL}	D_{IN}
WRITE INHIBIT	X V_{IH} X	X X V_{IL}	V_{IH} X X	HI-Z or D_{OUT} HI-Z HI-Z or D_{OUT}

X: any CMOS/TTL level

Reads

A read is typically accomplished by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{OE}$) to a TTL low. During read, the addresses, $\overline{CE}$, $\overline{OE}$, and input data latches are transparent.

Writes

To write into a particular location, addressess must be valid and a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This combined with the output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$, whichever one occurred last). Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$, whichever occurred first). An automatic erase is performed before data is written.

The MQ/ME28C010 can write both bytes and blocks of up to 64 bytes. The write mode is discussed below.

Write Cycle Control Pins

For system design simplification, the MQ/ME28C010 is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch the data. Address and $\overline{OE}$ set up and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data set up and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the control pin throughout the rest of this document. Timing diagrams of both write cycles are included in the AC characteristics.

Write Mode

One to 64 bytes of data can be loaded randomly into the MQ/ME28C010. Address lines A15 and A16 must be held valid during the entire page load cycle. The part latches row addresses, A6-A14 during the first byte write. These addresses are latched on the falling edge of $\overline{WE}$ signal (assuming $\overline{WE}$ control write cycle) and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5 which are used to write into different locations of the page, are latched every time a new write is initiated. These addresses along with $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the MQ/ME28C010 latches data and starts the internal page loader timer. The timer is reset on the falling edge of $\overline{WE}$ signal if a write is initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no more write cycles have been initiated in (t_{BLC}) after the last $\overline{WE}$ low to high transition, the part terminates page load cycle and starts the internal write. During this time, which takes a maximum of 10ms, the device ignores any additional load attempts. The part can be now read to determine the end of write cycle ($\overline{DATA}$ Polling). A 160µs maximum effective byte write time can be achieved if the page is fully utilized.

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the MQ/ME28C010 permits an extended page load cycle. To do this, the write cycle must be 'stretched' by maintaining $\overline{WE}$ low, assuming a write enable controlled cycle and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will inhibit the page load timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

Data Polling

The MQ/ME28C010 has a maximum write cycle time of 10ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual end point of a write cycle. If a read is performed to any address while the MQ/ME28C010 is still writing, the device will present the Ones-complement of the last data byte written. When the MQ/ME28C010 has completed its write cycle, a read from the last address written will result in valid data. Thus software can simply read from the part until the last data byte written is read correctly. A $\overline{DATA}$ polling read should not be done until a minimum of t_{LP} microseconds after the last byte is written. Timing for a $\overline{DATA}$ polling read is the same as a normal read once the t_{LP} specifications have been met.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI} V.*
2. *A high to low Write Enable (WE) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with CE low and OE high.*

Writing will also be inhibited when WE, CE, or OE are in TTL logical states other than that specified for a byte write in the Mode Selection table.

*Absolute Maximum Stress Range**

Temperature
Storage. . . . . −65°C to +150°C
Under Bias. . . . . −65°C to +135°C

All Input or Output Voltages
with Respect to V_{SS}. . . . . +6 V to −0.5 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	ME28C010	**MQ28C010**
Temperature Range (Ambient)	−55°C to 85°C	0°C to 70°C
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%

Endurance and Data Retention

Symbol	**Parameter**	**Value**	**Units**	**Condition**
N K	Minimum Endurance[4]	10,000 1,000	Cycles/Byte	MIL-STD 833 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 833 Test Method 1008

DC Charateristics

(Over operating temperature and V_{CC} Range, unless otherwise specified)

		Limits			
Symbol	**Parameter**	**Min.**	**Max.**	**Units**	**Test Condition**
I_{CC}	Active V_{CC} Current		70	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O = 0 ma; Addr = 5MHz
I_{SB_1}	Standby V_{CC} Current (TTL Inputs)		10	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O = 0 ma;
I_{SB_2}	Standby V_{CC} Current (CMOS Inputs)		2	mA	$\overline{CE} = V_{CC} - 0.2$; A15, A16 = $V_{CC} - 0.2$ Other Inputs = V_{IH} All I/O = 0 ma
I_{IL}[2]	Input Leakage Current		5	µA	$V_{IN} = V_{CC}$ Max.
I_{OL}[3]	Output Leakage Current		25	µA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ µA
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

NOTES:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.
3. For I/O only.
4. Endurance can be specified as an option to be 1000 or 10000 cycles/byte minimum for ME28C010 and is 1000 cycles/byte minimum for MQ28C010.

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: < 10 ns
Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] $T_A = 25°C$, t = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	30 pF	$V_{IN} = OV$
C_{OUT}	Data (I/0) Capacitance	40 pF	$V_{I/0} = OV$

E.S.D. Characteristics

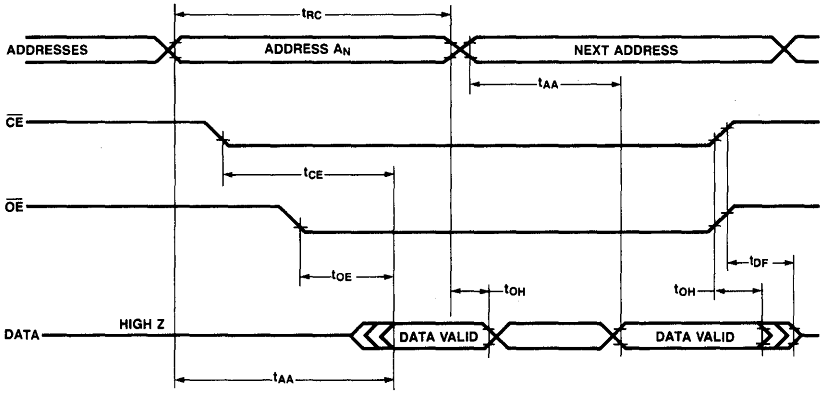
Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	> 1000 V	M_{IL} = STD 883 Test Method 3015

AC Characteristics Read Operation

(Over operating temperature and V_{CC} range, unless otherwise specified)

		Limits							
		MQ28C010-250 ME28C010-250		MQ28C010-300 ME28C010-300		MQ28C010-350 ME28C010-350			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
t_{RC}	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		150		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to Output in Hi-Z	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{\text{DATA}}$ Polling Cycle



NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

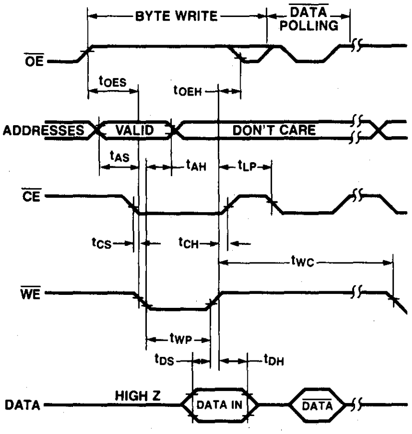
AC Characteristics Write Operation

(Over the operating temperature and V_{CC} range, unless otherwise specified)

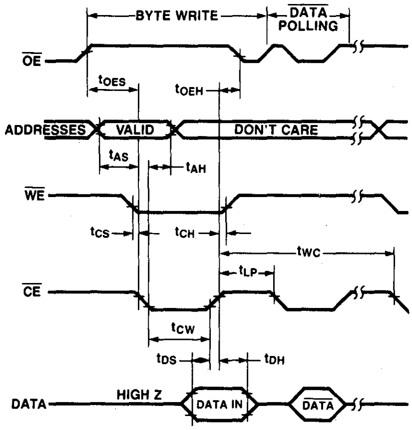
		Limits						
		MQ28C010-250 ME28C010-250		MQ28C010-300 ME28C010-300		MQ28C010-350 ME28C010-350		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Set-up Time	20		20		20		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (see note 2)	150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	20		20		20		ns
t_{OEH}	$\overline{OE}$ High Hold Time	20		20		20		ns
t_{WP}	$\overline{WE}$ Pulse Width (see note 2)	150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (see note 3)	0.2	200	0.2	200	0.2	200	µs
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		1		1		1	ms

Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



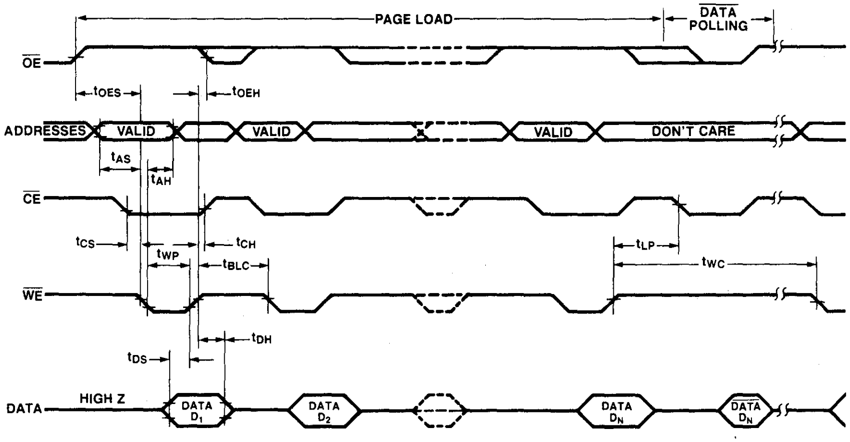
$\overline{CE}$ CONTROLLED WRITE CYCLE



NOTES:

1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing



Ordering Information

M Q 28C010 K -250

PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ENDURANCE	ACCESS TIME
M - MODULE	Q–0°C to 70°C (Commercial) E–55°C to 85°C (Extended)	128 K × 8 EEPROM	K = 1000 Cycles N = 10000 Cycles	250 = 250 ns 300 = 300 ns 350 = 350 ns

2 FLASH

seeq

48F512
512K FLASH™ EEPROM

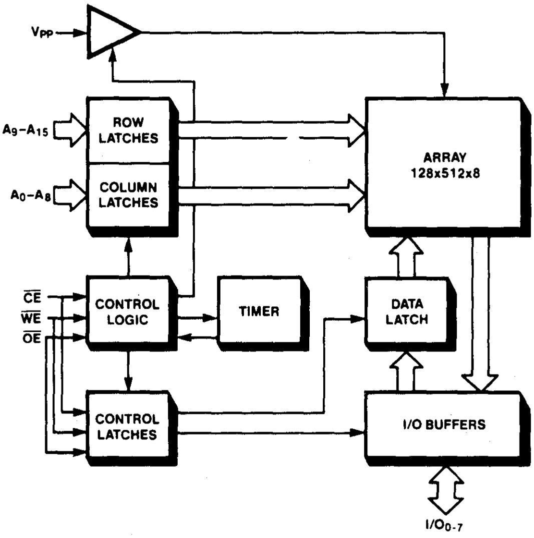
PRELIMINARY DATA SHEET

October 1988

Features

- 64K Byte FLASH Erasable Non-Volatile Memory
- Low Power CMOS Process
- Electrical Byte Write and Chip/Sector Erase
- Input Latches for Writing and Erasing
- Fast Read Access Time
- Single High Voltage for Writing and Erasing
- FLASH EEPROM Cell Technology
- Ideal for Low-Cost Program and Data Storage
  - Minimum 100 Cycle Endurance
  - Optional 1000 Cycle Endurance Screening
  - Minimum 10 Year Data Retention
- 5 V ± 10% V_{CC}, 0° C to +70° C Temperature Range
- Silicon Signature®
- JEDEC Standard Byte Wide Pinout
  - 32 Pin DIP
  - 32 Pin J-Bend Plastic Leaded Chip Carrier

Block Diagram



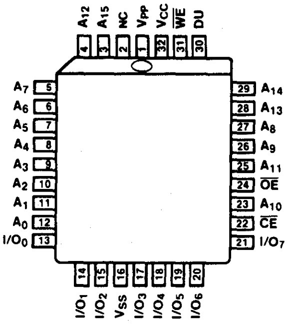
Pin Names

A_0-A_8	COLUMN ADDRESS INPUT
A_9-A_{15}	ROW ADDRESS INPUT
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

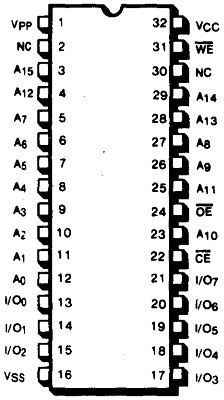
Silicon Signature is a registered trademark of SEEQ Technology.
FLASH is a trademark of SEEQ Technology.

Pin Configurations

PLASTIC LEADED CHIP CARRIER TOP VIEW



DUAL-IN-LINE TOP VIEW



Description

The 48F512 is a 512K bit CMOS FLASH EEPROM organized as 64K x 8 bits. SEEQ's 48F512 brings together the high density and cost effectiveness of UVEPROMs, with the electrical erase, in-circuit reprogrammability and package options of EEPROMs.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated. The memory array is divided into 128 sectors, with each sector containing 512 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

Endurance, the number of times each byte can be written, is specified at 100 cycles with an optional screen for 1000 cycles available. Electrical write/erase capability allows the 48F512 to accommodate a wide range of plastic, ceramic and surface mount packages.

Read

Reading is accomplished by presenting a valid address with chip enable and output enable at V_{IL}, write enable at V_{IH}, and V_{PP} at any level. See timing waveforms for A.C. parameters.

Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Sector Erase

Sector erase changes all bits in a sector of the array to a logical one. It requires that the V_{PP} pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs A_9 through A_{15}. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time t_{ABORT} to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the t_{ABORT} delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in figure 2. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Sector and Chip Erase Algorithm

To reduce the sector and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the sector erase and chip erase flow charts.

Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either sector erase or chip erase.

Data are organized in the 48F512 in a group of bytes called a sector. The memory array is divided into 128 sectors of 512 bytes each. Individual bytes are written as part of a sector write operation. The programming algorithm for either chip or sector write is detailed in figure 1.

*Sectors are written by applying a high voltage to the V_{PP} pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of t_{WC} ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired blocks have been written. After 10 loops, a read-verification is performed. For any bytes which do not verify, a fill-in programming loop is performed. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.
the number of loops required. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.*

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sector must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

Power Up/Down Protection

This device contains a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1 uf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the 48F512 which contains the device's Silicon Signature. Silicon Signature contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_9 to 12 ± 0.5 V. and bringing all other address inputs plus chip enable and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0. Silicon Signature is functional at room temperature only (25°C.)

Silicon Signature Bytes

	A_0	Data (Hex)
Seeq Code	V_{IL}	94
Product code 48F512	V_{IH}	1A

Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	A_{9-15}	A_{0-8}	D_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HI-Z
Byte write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip erase select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Sector erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

Absolute Maximum Stress Ratings

Temperature:	
Storage	*−65°C to +125°C*
Under bias	*−10°C to +85°C*
All Inputs except V_{PP} and outputs with Respect to V_{SS}	*+7 V to −0.5 V*
V_{PP} pin with respect to V_{SS}	*14 V*

E.S.D. Characteristics[1]

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note 1: Characterization data—not tested.

Recommended Operating Conditions

	48F512
V_{CC} supply voltage	5V ± 10%
Temperature range	0°C to 70°C (ambient temp.)

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	**Parameter**	**Value**	**Test Conditions**
C_{IN}	Input capacitance	6 pf.	V_{IN}= 0 V
C_{OUT}	Output capacitance	12 pf.	$V_{I/O}$= 0 V

Note 2: This parameter is only sampled and not 100% tested.

DC Operating Characteristics

Over the V_{CC} and temperature range

Symbol	**Parameter**	**Limits**			**Test Conditions**
		Min.	**Max.**	**Unit**	
I_{IH}	Input leakage high		1	μA	$V_{IN} = V_{CC}$
I_{IL}	Input leakage low		−1	μA	V_{IN} = 0.1 v
I_{OL}	Output leakage		10	μA	$V_{IN} = V_{CC}$
V_P	Program/erase voltage	11.75	13	V	
V_{PR}	V_{PP} Voltage during read	0	V_P	V	
I_{PP}	V_P current Standby mode Read mode Byte write Erase		 200 200 40 80	 μA μA mA mA	 $\overline{CE} = V_{IH}, V_{PP} = V_P$ $\overline{CE} = V_{IL}, V_{PP} = V_P$ $V_{PP}= V_P$ $V_{PP} = V_P$
I_{CC1}	Standby V_{CC} current		100	μA	$\overline{CE} = V_{CC} -0.3$ v
I_{CC2}	Standby V_{CC} current		5	mA	$\overline{CE}$ - V_{IH} min.
I_{CC3}	Active V_{CC} current		60	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input low voltage	−0.3	0.8	V	
V_{IH}	Input high voltage	2.0	7.0	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2.1 ma
V_{OH1}	Output level (TTL)	2.4		V	$I_{OH} = -400\mu A$
V_{OH2}	Output level (CMOS)	$V_{CC}-0.4$		V	$I_{OH} = -100\mu A$

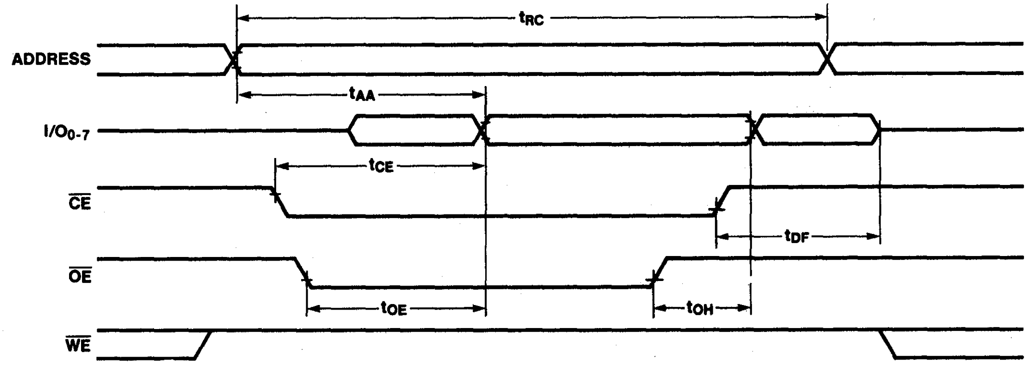
AC Characteristics

(over the V_{CC} and temperature range)

READ

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	200		250		300		ns
t_{AA}	Address to data		200		250		300	ns
t_{CE}	$\overline{CE}$ to data		200		250		300	ns
t_{OE}	$\overline{OE}$ to data		75		100		150	ns
t_{DF}	$\overline{OE}/\overline{CE}$ to data float		50		60		100	ns
t_{OH}	Output hold time	0		0		0		ns

Read Timing



AC Test Conditions

Output load: 1 TTL gate and C(load) 100 pf.
Input rise and fall times: < 20 ns.
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

AC Characteristics

(Over the V_{CC} and temperature range)

BYTE WRITE

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		μs
t_{VPH}	V_{PP} hold time	250		250		250		μs
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	10		10		10		ns
t_{OEH}	$\overline{OE}$ hold time	10		10		10		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{WC}	Write cycle time	100	150	100	150	100	150	μs
t_{WR}	Write recovery time		1.5		1.5		1.5	ms

Note: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g. access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Byte Write Timing

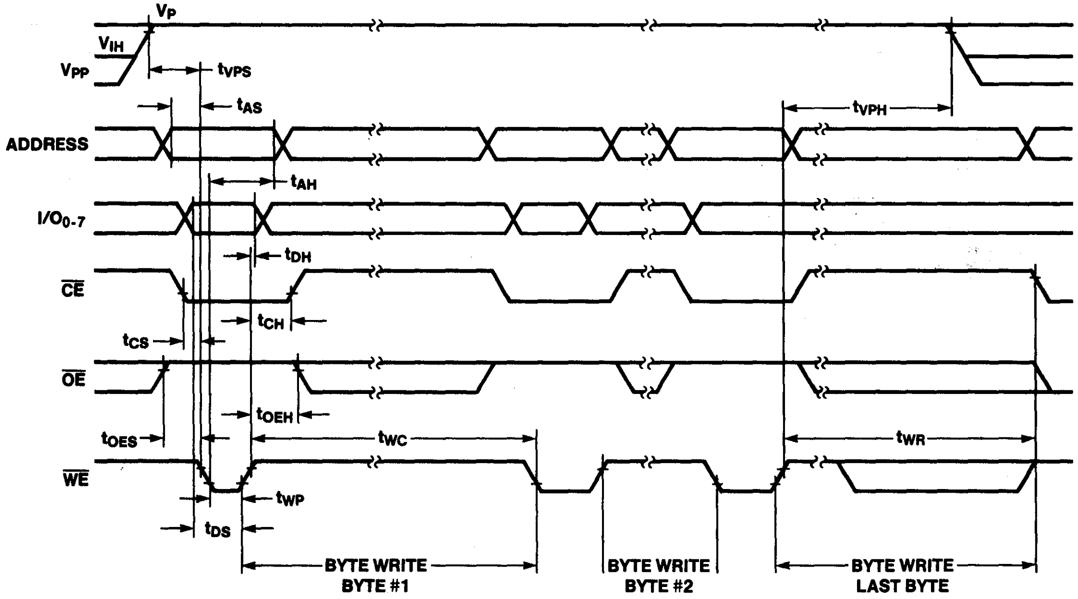
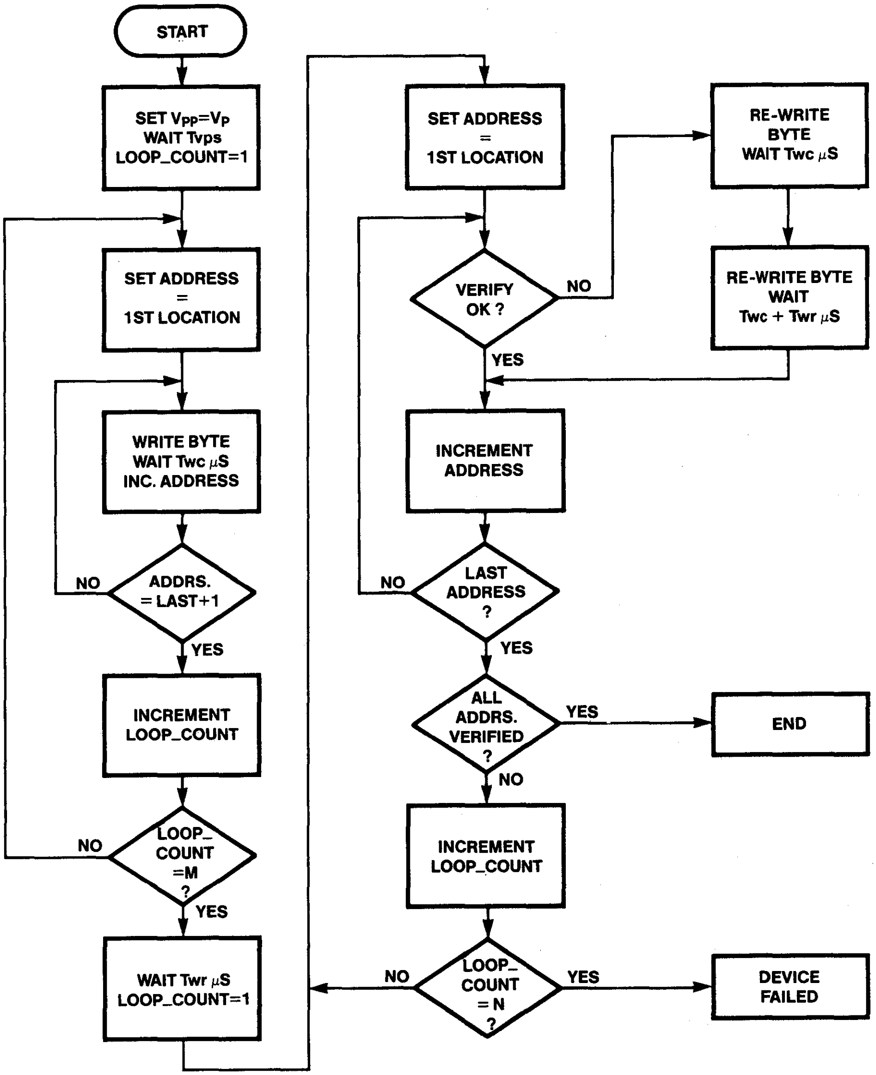


Figure 1
48F512 Write Algorithm



M=10
N=6

AC Characteristics *SECTOR ERASE*

(Over the V_{CC} and temperature range)

Symbol	Parameter	48F512 -200 Min.	48F512 -200 Max.	48F512 -250 Min.	48F512 -250 Max.	48F512 -300 Min.	48F512 -300 Max.	Unit
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Sector erase time		500		500		500	ms
t_{ABORT}	Sector erase delay		250		250		250	µs
t_{ER}	Erase recovery time		250		250		250	ms

Sector Erase Timing

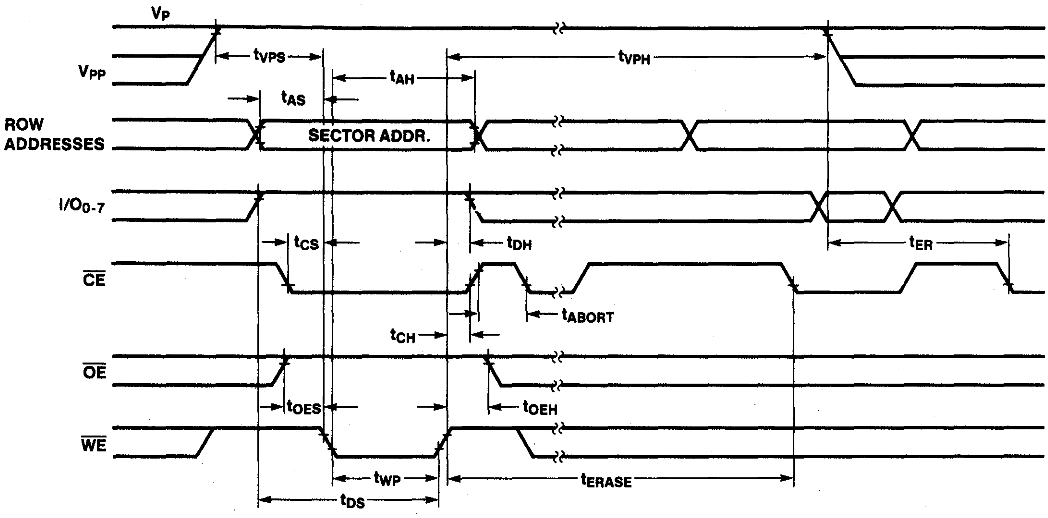
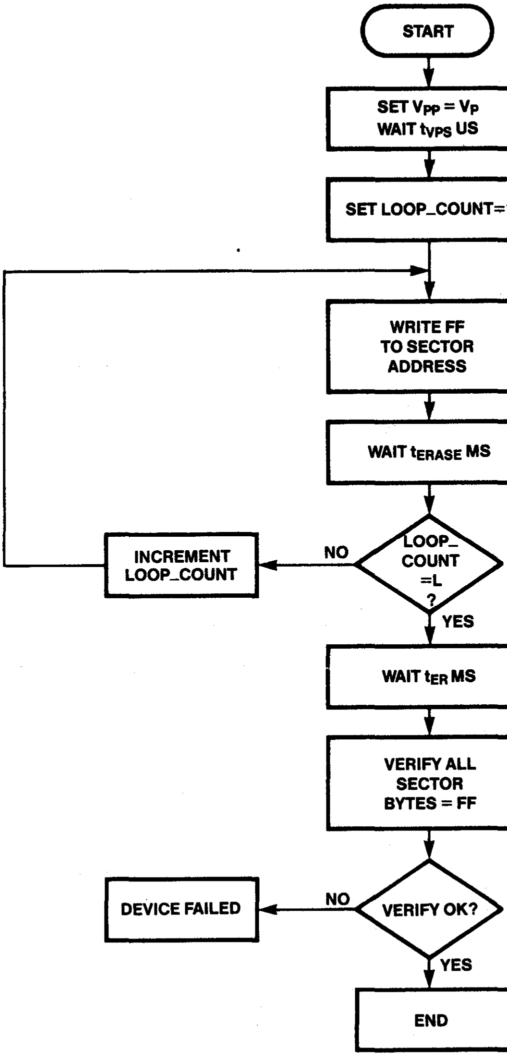


Figure 2
48F512 Sector Erase Algorithm



L=30

AC Characteristics

(Over the V_{CC} and temperature range)

CHIP ERASE

Symbol	Parameter	48F512 -200		48F512 -250		48F512 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Chip erase time		500		500		500	ms
t_{ER}	Erase recovery time		250		250		250	ms

Chip Erase Timing

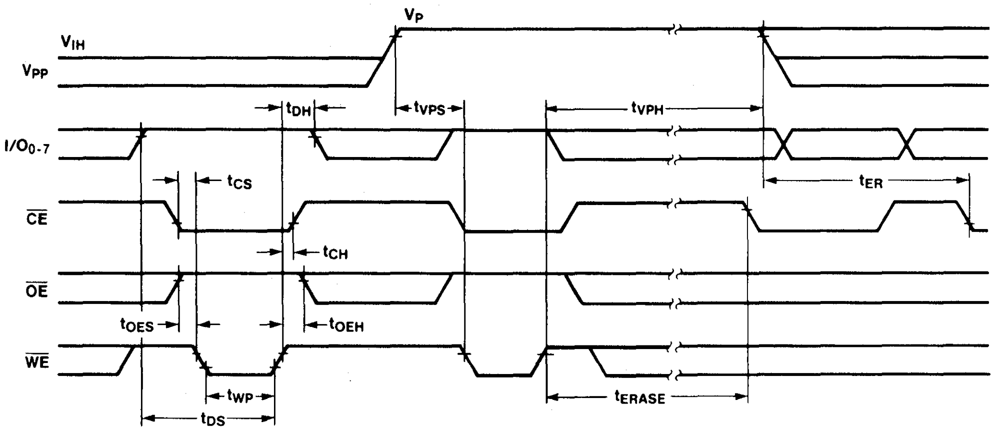
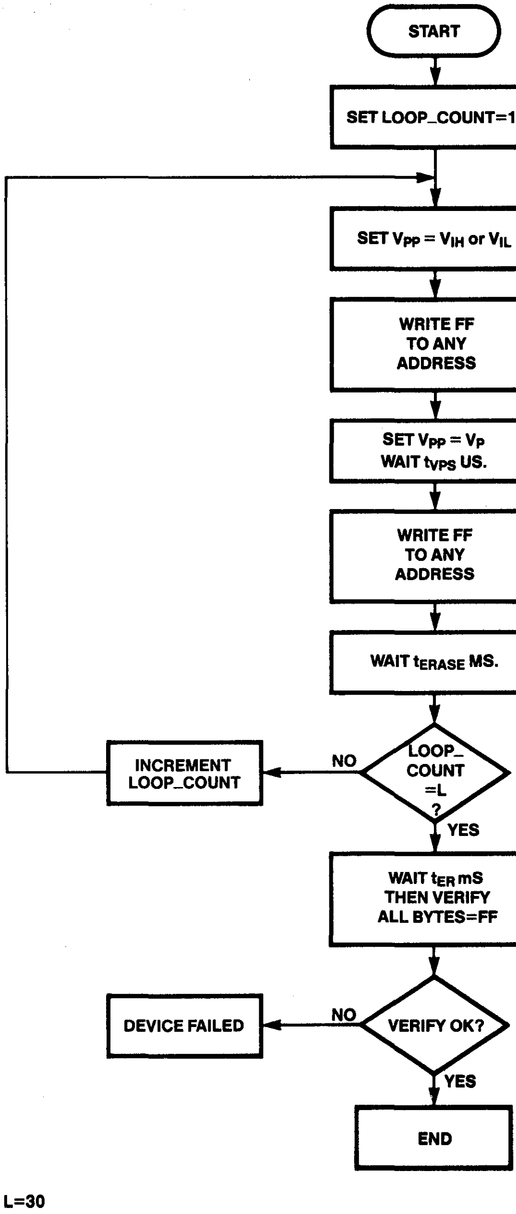


Figure 3
48F512 Chip Erase Algorithm



L=30

Ordering Information

D	Q	48F512	K	-200
Package Type	**Temperature Range**	**Device**	**Endurance**	**Access Time**
D = Ceramic Dip	Q = 0 to 70°C	64K x 8 FLASH EEPROM	Blank = 100	200 = 200ns
P = Plastic Dip			K = 1000	250 = 250ns
N = Plastic Leaded Chip Carrier				300 = 300ns

seeq

48F010
1024K FLASH™ EEPROM

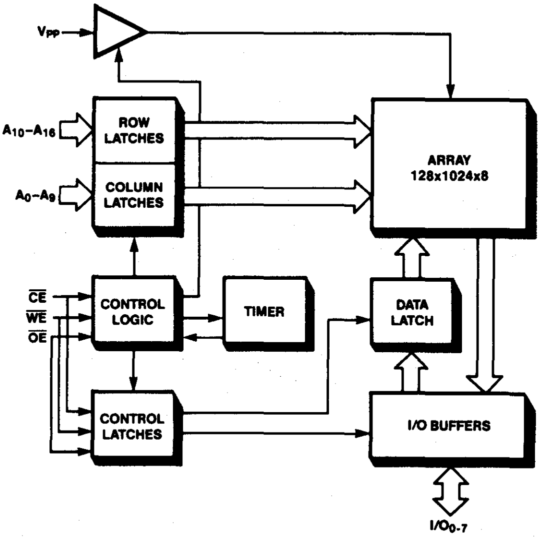
ADVANCE DATA SHEET

October 1988

Features

- ***128K Byte FLASH Erasable Non-Volatile Memory***
- ***Low Power CMOS Process***
- ***Electrical Byte Write and Chip/Sector Erase***
- ***Input Latches for Writing and Erasing***
- ***Fast Read Access Time***
- ***Single High Voltage for Writing and Erasing***
- ***FLASH EEPROM Cell Technology***
- ***Ideal for Low-Cost Program and Data Storage***
  - ***Minimum 100 Cycle Endurance***
  - ***Optional 1000 Cycle Endurance Screening***
  - ***Minimum 10 Year Data Retention***
- ***5 V ± 10% V_{CC}, 0° C to +70° C Temperature Range***
- ***Silicon Signature®***
- ***JEDEC Standard Byte Wide Pinout***
  - ***32 Pin DIP***
  - ***32 Pin J-Bend Plastic Leaded Chip Carrier***

Block Diagram

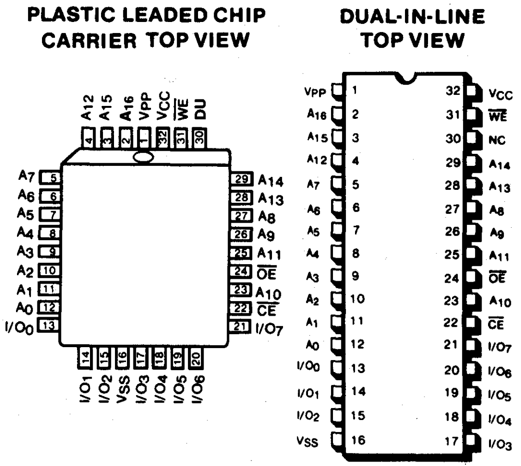


Pin Names

A_0-A_9	COLUMN ADDRESS INPUT
A_{10}-A_{16}	ROW ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

Silicon Signature is a registered trademark of SEEQ Technology.
FLASH is a trademark of SEEQ Technology.

Pin Configurations


PLASTIC LEADED CHIP CARRIER TOP VIEW

DUAL-IN-LINE TOP VIEW

Description

The 48F010 is a 1024K bit CMOS FLASH EEPROM organized as 128K x 8 bits. SEEQ's 48F010 brings together the high density and cost effectiveness of UVEPROMs, with the electrical erase, in-circuit reprogrammability and package options of EEPROMs.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated. The memory array is divided into 128 sectors, with each sector containing 1024 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

Endurance, the number of times each byte can be written, is specified at 100 cycles with an optional screen for 1000 cycles available. Electrical write/ erase capability allows the 48F010 to accommodate a wide range of plastic, ceramic and surface mount packages.

Read

Reading is accomplished by presenting a valid address with chip enable and output enable at V_{IL}, write enable at V_{IH}, and V_{PP} at any level. See timing waveforms for A.C. parameters.

Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Sector Erase

Sector erase changes all bits in a sector of the array to a logical one. It requires that the V_{PP} pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs A_{10} through A_{16}. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time t_{abort} to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the t_{ABORT} delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in figure 2. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Sector and Chip Erase Algorithm

To reduce the sector and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the sector erase and chip erase flow charts.

Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either sector erase or chip erase.

Data are organized in the 48F010 in a group of bytes called a sector. The memory array is divided into 128 sectors of 1024 bytes each. Individual bytes are written as part of a sector write operation. The programming algorithm for either chip or sector write is detailed in figure 1.

Sectors are written by applying a high voltage to the V_{PP} pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of t_{WC} ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired blocks have been written. After 10 loops, a read-verification is performed. For any bytes which do not verify, a fill-in programming loop is performed. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sector must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

Power Up/Down Protection

This device contains a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1 uf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the 48F010 which contains the device's Silicon Signature. Silicon Signature contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_9 to 12 ± 0.5 V. and bringing all other address inputs plus chip enable and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0. Silicon Signature is functional at room temperature only (25°C.)

Silicon Signature Bytes

	A_0	Data (Hex)
Seeq Code	V_{IL}	94
Product code 48F010	V_{IH}	1C

Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	A_{10-16}	A_{0-9}	D_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HI-Z
Byte write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip erase select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Sector erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

Absolute Maximum Stress Ratings

Temperature:	
Storage	*−65°C to +125°C*
Under bias	*−10°C to +85°C*
All Inputs except V_{PP} and outputs with Respect to V_{SS} . . .	*+7 V to −0.5 V*
V_{PP} pin with respect to V_{SS}	*14 V*

E.S.D. Characteristics[1]

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note 1: Characterization data—not tested.

Recommended Operating Conditions

	48F010
V_{CC} supply voltage	5V ± 10%
Temperature range	0°C to 70°C (ambient temp.)

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	Parameter	Value	Test Conditions
C_{IN}	Input capacitance	6 pf.	V_{IN}= 0 V
C_{OUT}	Output capacitance	12 pf.	$V_{I/O}$= 0 V

Note 2: This parameter is only sampled and not 100% tested.

DC Operating Characteristics

Over the V_{CC} and temperature range

		Limits			
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**	**Test Conditions**
I_{IH}	Input leakage high		1	μA	$V_{IN} = V_{CC}$
I_{IL}	Input leakage low		−1	μA	V_{IN} = 0.1 v
I_{OL}	Output leakage		10	μA	$V_{IN} = V_{CC}$
V_P	Program/erase voltage	11.75	13	V	
V_{PR}	V_{PP} Voltage during read	0	V_P	V	
I_{PP}	V_P current Standby mode Read mode Byte write Erase		 200 200 40 80	 μA μA mA mA	 $\overline{CE} = V_{IH}, V_{PP} = V_P$ $\overline{CE} = V_{IL}, V_{PP} = V_P$ $V_{PP}= V_P$ $V_{PP} = V_P$
I_{CC1}	Standby V_{CC} current		100	μA	$\overline{CE} = V_{CC} -0.3$ v
I_{CC2}	Standby V_{CC} current		5	mA	$\overline{CE}$ - V_{IH} min.
I_{CC3}	Active V_{CC} current		60	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input low voltage	−0.3	0.8	V	
V_{IH}	Input high voltage	2.0	7.0	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2.1 ma
V_{OH1}	Output level (TTL)	2.4		V	I_{OH} = −400μA
V_{OH2}	Output level (CMOS)	V_{CC}−0.4		V	I_{OH} = −100μA

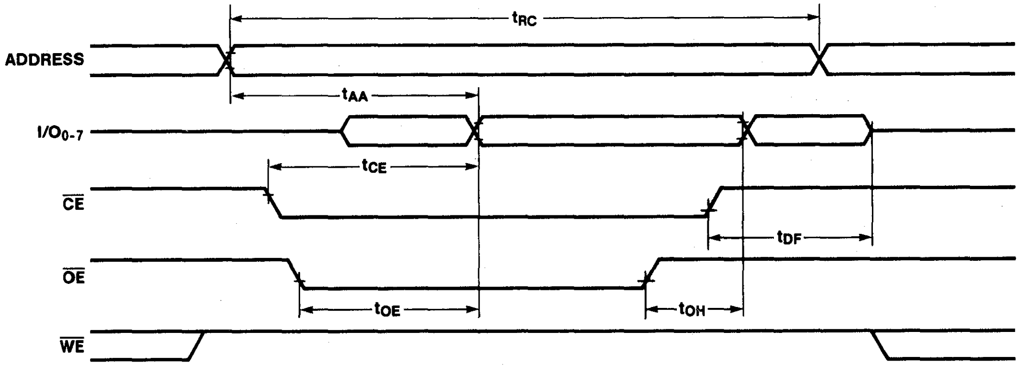
AC Characteristics

(over the V_{CC} and temperature range)

READ

Symbol	Parameter	48F010 -200		48F010 -250		48F010 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	200		250		300		ns
t_{AA}	Address to data		200		250		300	ns
t_{CE}	$\overline{CE}$ to data		200		250		300	ns
t_{OE}	$\overline{OE}$ to data		75		100		150	ns
t_{DF}	$\overline{OE}/\overline{CE}$ to data float		50		60		100	ns
t_{OH}	Output hold time	0		0		0		ns

Read Timing



AC Test Conditions

Output load: 1 TTL gate and C(load) 100 pf.
Input rise and fall times: < 20 ns.
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

AC Characteristics *BYTE WRITE*

(Over the V_{CC} and temperature range)

Symbol	Parameter	48F010 -200		48F010 -250		48F010 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		μs
t_{VPH}	V_{PP} hold time	250		250		250		μs
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	10		10		10		ns
t_{OEH}	$\overline{OE}$ hold time	10		10		10		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{WC}	Write cycle time	100	150	100	150	100	150	μs
t_{WR}	Write recovery time		1.5		1.5		1.5	ms

Note: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g. access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Advance Data Sheets contain target product specifications which are subject to change upon device characterization over the full specified temperature range. These specifications may be changed at any time, without notice.

Byte Write Timing

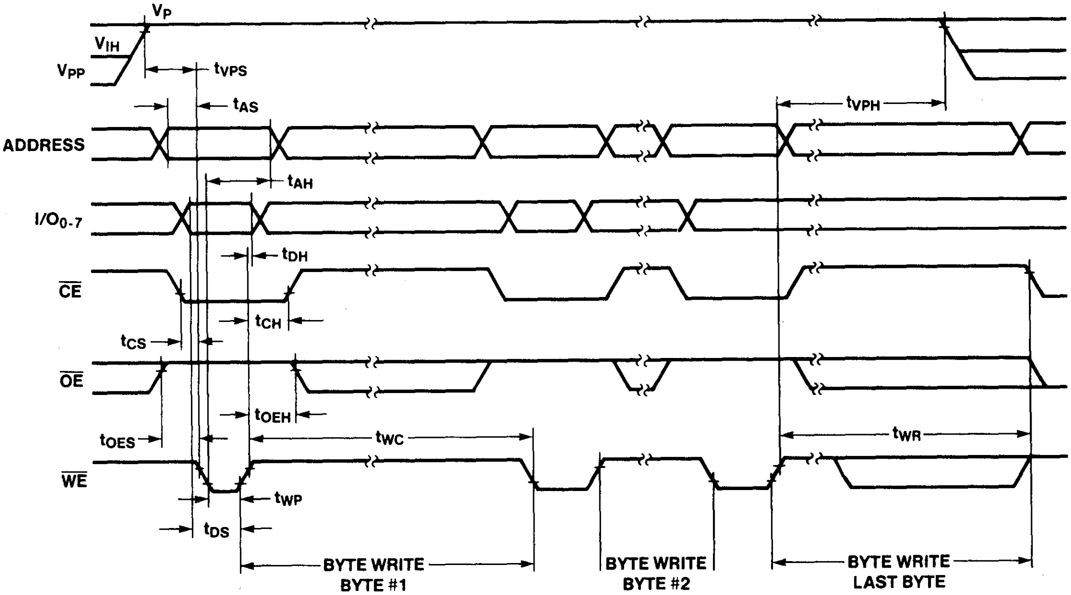
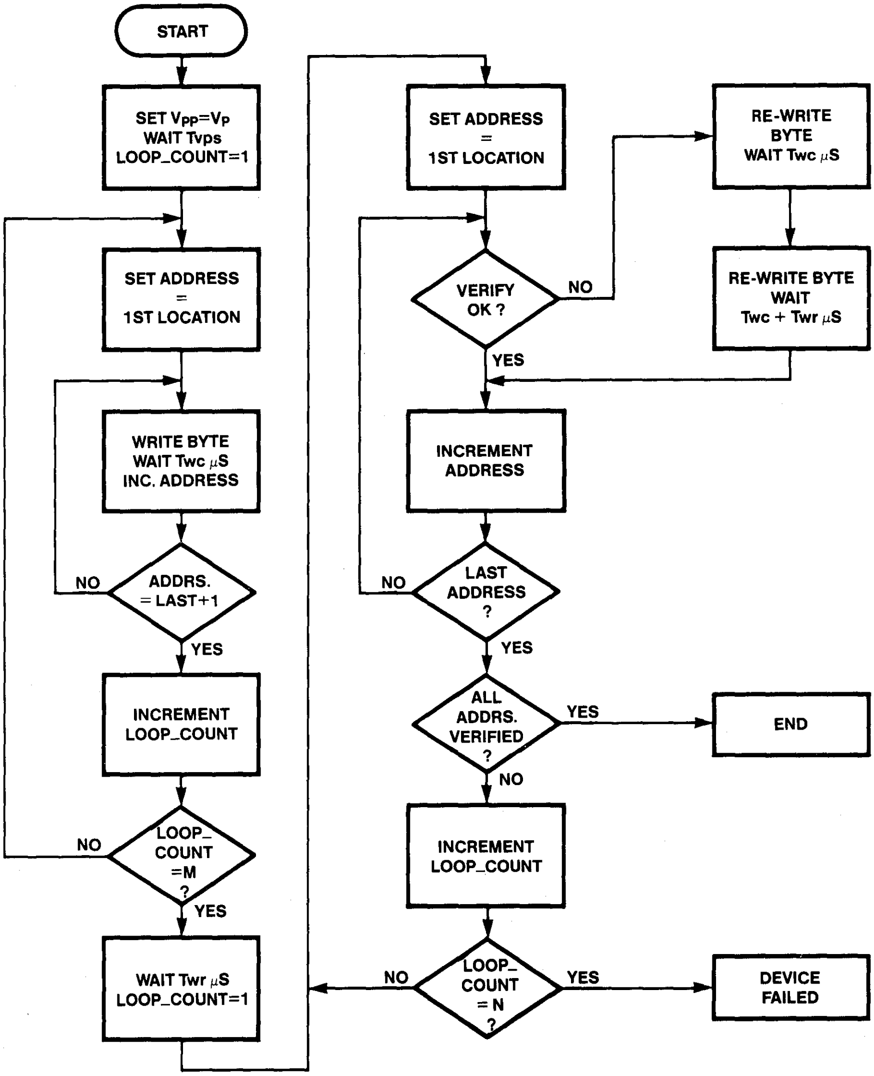


Figure 1
48F010 Write Algorithm



M=10
N=6

AC Characteristics

(Over the V_{CC} and temperature range)

SECTOR ERASE

Symbol	Parameter	48F010 -200 Min.	48F010 -200 Max.	48F010 -250 Min.	48F010 -250 Max.	48F010 -300 Min.	48F010 -300 Max.	Unit
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Sector erase time		500		500		500	ms
t_{ABORT}	Sector erase delay		250		250		250	µs
t_{ER}	Erase recovery time		250		250		250	ms

Sector Erase Timing

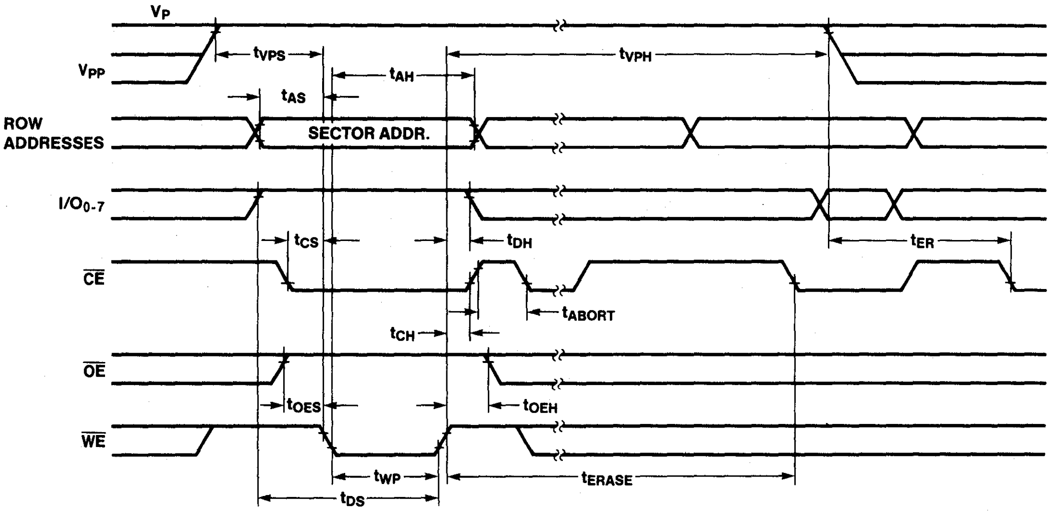
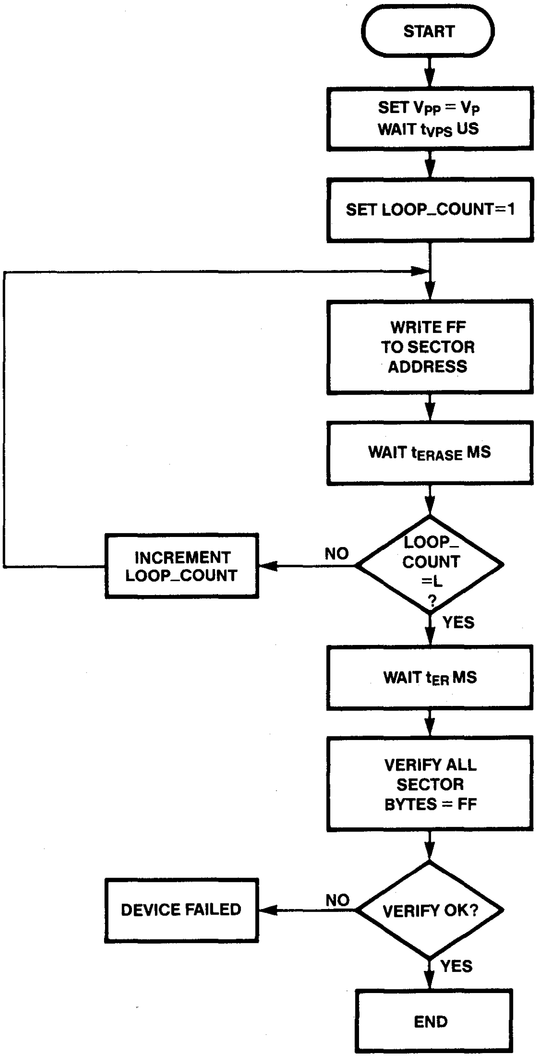


Figure 2
48F010 Sector Erase Algorithm



L=30

AC Characteristics

(Over the V_{CC} and temperature range)

CHIP ERASE

Symbol	Parameter	48F010 -200		48F010 -250		48F010 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Chip erase time		500		500		500	ms
t_{ER}	Erase recovery time		250		250		250	ms

Chip Erase Timing

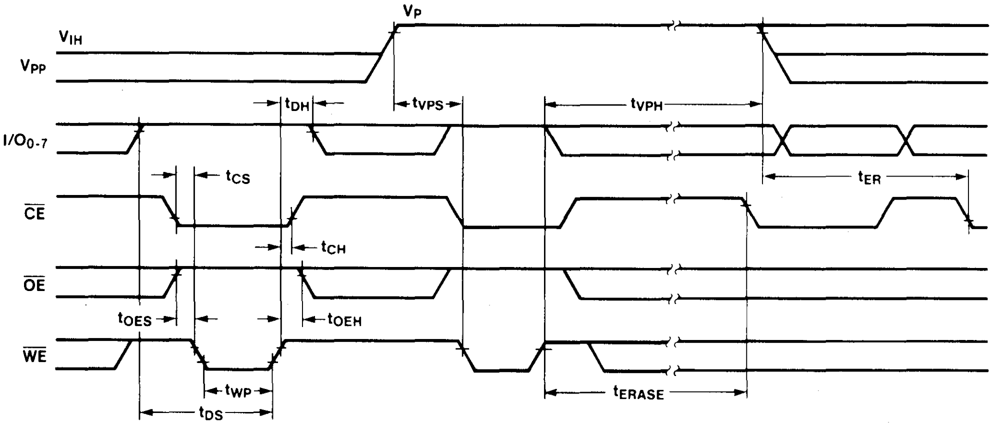
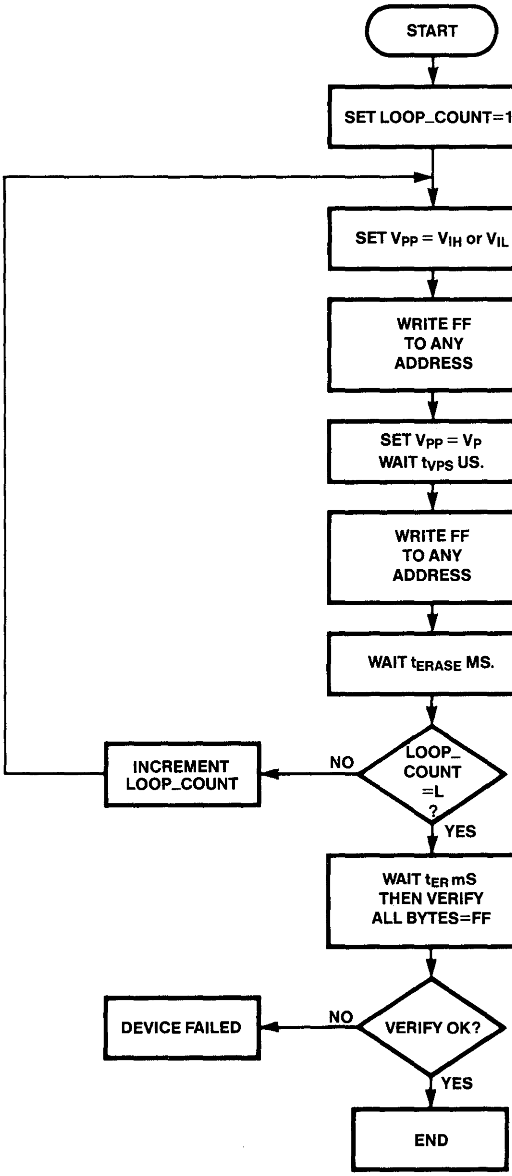


Figure 3
48F010 Chip Erase Algorithm



L=30

Ordering Information

D	Q	48F010	K	-200
Package Type	**Temperature Range**	**Device**	**Endurance**	**Access Time**
D = Ceramic Dip	Q = 0 to 70°C	128K x 8 FLASH EEPROM	Blank = 100	200 = 200ns
P = Plastic Dip			K = 1000	250 = 250ns
N = Plastic Leaded Chip Carrier				300 = 300ns

seeq

27F010
1024K FLASH™ EPROM

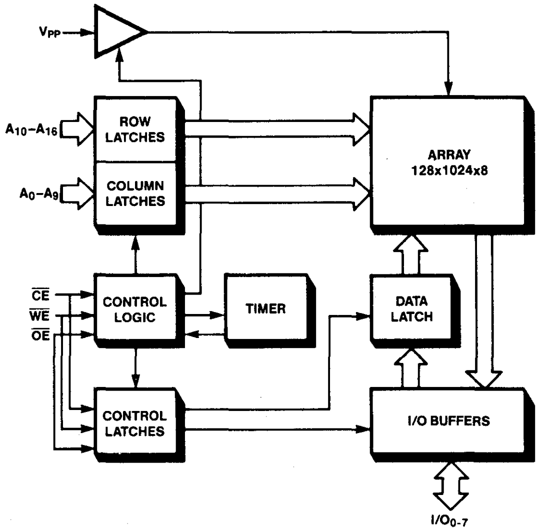
ADVANCE DATA SHEET

October 1988

Features

- *128K Byte FLASH Erasable Non-Volatile Memory*
- *Low Power CMOS Process*
- *Electrical Byte Write and Chip/Sector Erase*
- *Input Latches for Writing and Erasing*
- *Fast Read Access Time*
- *Single High Voltage for Writing and Erasing*
- *FLASH EPROM Cell Technology*
- *Ideal for Low-Cost Program and Data Storage*
  - *Minimum 10 Year Data Retention*
- *5 V ± 10% V_{CC}*
- *Silicon Signature®*
- *JEDEC Standard Byte Wide Pinout*
  - *32 Pin DIP*
  - *32 Pin J-Bend Plastic Leaded Chip Carrier*

Block Diagram



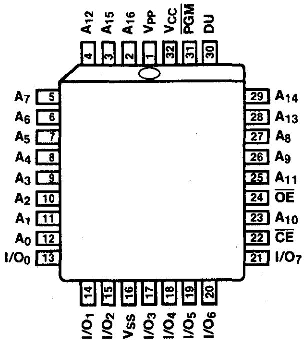
Pin Names

A_0-A_9	COLUMN ADDRESS INPUT
A_{10}-A_{16}	ROW ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{PGM}$	PROGRAM
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

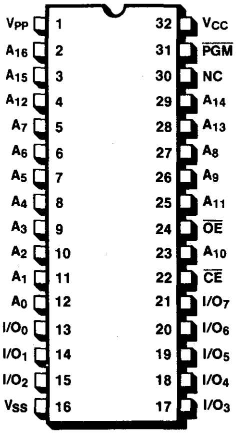
Silicon Signature is a registered trademark of SEEQ Technology.
FLASH is a trademark of SEEQ Technology.

Pin Configurations

PLASTIC LEADED CHIP CARRIER TOP VIEW



DUAL-IN-LINE TOP VIEW



Description

The 27F010 is a 1024K bit CMOS FLASH EPROM organized as 128K x 8 bits. SEEQ's 27F010 brings together the high density, cost effectiveness, and reprogrammability of UVEPROMs with the electrical erase and package options of EEPROMs.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated. The memory array is divided into 128 sectors, with each block containing 1024 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

Read

Reading is accomplished by presenting a valid address with chip enable and output enable at V_{IL}, $\overline{PGM}$ *at* V_{IH}, *and* V_{PP} *at any level. See timing waveforms for A.C. parameters.*

Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of $\overline{PGM}$ *or chip enable, whichever is later, while data inputs are latched on the rising edge of* $\overline{PGM}$ *or chip enable, whichever is earlier. The* $\overline{PGM}$ *input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and* $\overline{PGM}$ *must be in the proper state to initiate a write or erase. Timing diagrams depict* $\overline{PGM}$ *controlled writes; the timing also applies to chip enable controlled writes.*

Sector Erase

Sector erase changes all bits in a sector of the array to a logical one. It requires that the V_{PP} *pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs* A_{10} *through* A_{16}. *The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time* t_{abort} *to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the* t_{abort} *delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in figure 2.* V_{PP} *can be brought to any TTL level or left at high voltage after the erase.*

Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm. V_{PP} *can be brought to any TTL level or left at high voltage after the erase.*

Sector and Chip Erase Algorithm

To reduce the sector and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the sector erase and chip erase flow charts.

Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either sector erase or chip erase.

Data are organized in the 27F010 in a group of bytes called a sector. The memory array is divided into 128 sectors of 1024 bytes each. Individual bytes are written as part of a sector write operation. The programming algorithm for either chip or sector write is detailed in figure 1.

Sectors are written by applying a high voltage to the V_{PP} *pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of* t_{WC} *ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired sectors have been written. After 10 loops, a read-verification is performed. For any bytes which do not verify, a fill-in programming loop is performed. Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.*

Sectors need not be written separately; the entire device or any combination of sectors can be written using the write algorithm.

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sector must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

Power Up/Down Protection

The 27F010 contains a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input ($\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1 uf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the 27F010 which contains the device's Silicon Signature. Silicon Signature contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_9 to 12 ± 0.5 V. and bringing all other address inputs plus chip enable and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0. Silicon Signature is functional at room temperature only (25°C.)

Silicon Signature Bytes

	A_0	**Data (Hex)**
Seeq Code	V_{IL}	94
Product code 27F010	V_{IH}	1C

Mode Selection Table

MODE	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**V_{PP}**	**A_{10-16}**	**A_{0-9}**	**I/O_{0-7}**
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HI-Z
Byte write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip erase select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Sector erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

Absolute Maximum Stress Ratings

Temperature:	
Storage	*−65°C to +125°C*
Under bias	*−10°C to +85°C*
All Inputs except V_{PP} and outputs with Respect to V_{SS}	*+7 V to −0.5 V*
V_{PP} pin with respect to V_{SS}	*14 V*

E.S.D. Characteristics[1]

Symbol	**Parameter**	**Value**	**Test Conditions**
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note 1: Characterization data—not tested.

Recommended Operating Conditions

	27F010
V_{CC} supply voltage	5V ± 10%
Read Temperature range	0°C to 70°C (ambient temp.)
Write/Erase Temperature	25°C ± 5°C

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	Parameter	Value	Test Conditions
C_{IN}	Input capacitance	6 pf.	V_{IN}= 0 V
C_{OUT}	Output capacitance	12 pf.	$V_{I/O}$= 0 V

Note 2: This parameter is only sampled and not 100% tested.

DC Operating Characteristics

Over the V_{CC} and temperature range

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{IH}	Input leakage high		1	µA	$V_{IN} = V_{CC}$
I_{IL}	Input leakage low		−1	µA	V_{IN} = 0.1 v
I_{OL}	Output leakage		10	µA	$V_{IN} = V_{CC}$
V_P	Program/erase voltage	11.75	13	V	
V_{PR}	V_{PP} Voltage during read	0	V_P	V	
I_{PP}	V_P current Standby mode Read mode Byte write Erase		 200 200 40 80	 µA µA mA mA	 $\overline{CE} = V_{IH}, V_{PP} = V_P$ $\overline{CE} = V_{IL}, V_{PP} = V_P$ $V_{PP} = V_P$ $V_{PP} = V_P$
I_{CC1}	Standby V_{CC} current		100	µA	$\overline{CE} = V_{CC} - 0.3$ v
I_{CC2}	Standby V_{CC} current		5	mA	$\overline{CE}$ - V_{IH} min.
I_{CC3}	Active V_{CC} current		60	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input low voltage	−0.3	0.8	V	
V_{IH}	Input high voltage	2.0	7.0	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2.1 ma
V_{OH1}	Output high level (TTL)	2.4		V	$I_{OH} = -400\mu A$
V_{OH2}	Output high level (CMOS)	$V_{CC} - 0.4$		V	$I_{OH} = -100\mu A$

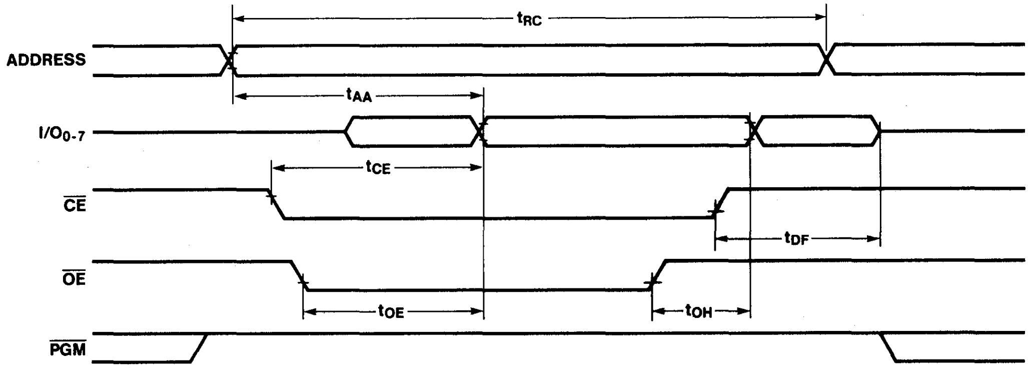
AC Characteristics

(over the V_{CC} and temperature range)

READ

Symbol	Parameter	27F010 -200		27F010 -250		27F010 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	200		250		300		ns
t_{AA}	Address to data		200		250		300	ns
t_{CE}	$\overline{CE}$ to data		200		250		300	ns
t_{OE}	$\overline{OE}$ to data		75		100		150	ns
t_{DF}	$\overline{OE}/\overline{CE}$ to data float		50		60		100	ns
t_{OH}	Output hold time	0		0		0		ns

Read Timing



AC Test Conditions

Output load: 1 TTL gate and C(load) 100 pf.
Input rise and fall times: < 20 ns.
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

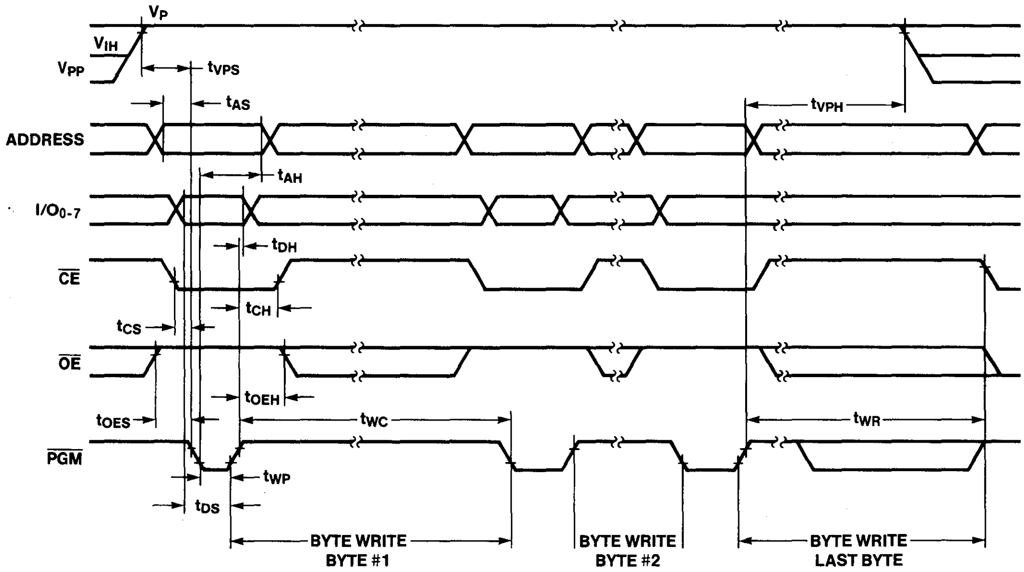
AC Characteristics

(Over the V_{CC} range)

BYTE WRITE

Symbol	Parameter	27F010 Min.	27F010 Max.	Unit
t_{VPS}	V_{PP} setup time	2		µs
t_{VPH}	V_{PP} hold time	250		µs
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OES}	$\overline{OE}$ setup time	10		ns
t_{OEH}	$\overline{OE}$ hold time	10		ns
t_{AS}	Address setup time	20		ns
t_{AH}	Address hold time	100		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	0		ns
t_{WP}	$\overline{PGM}$ pulse width	100		ns
t_{WC}	Write cycle time	100	150	µs
t_{WR}	Write recovery time		1.5	ms

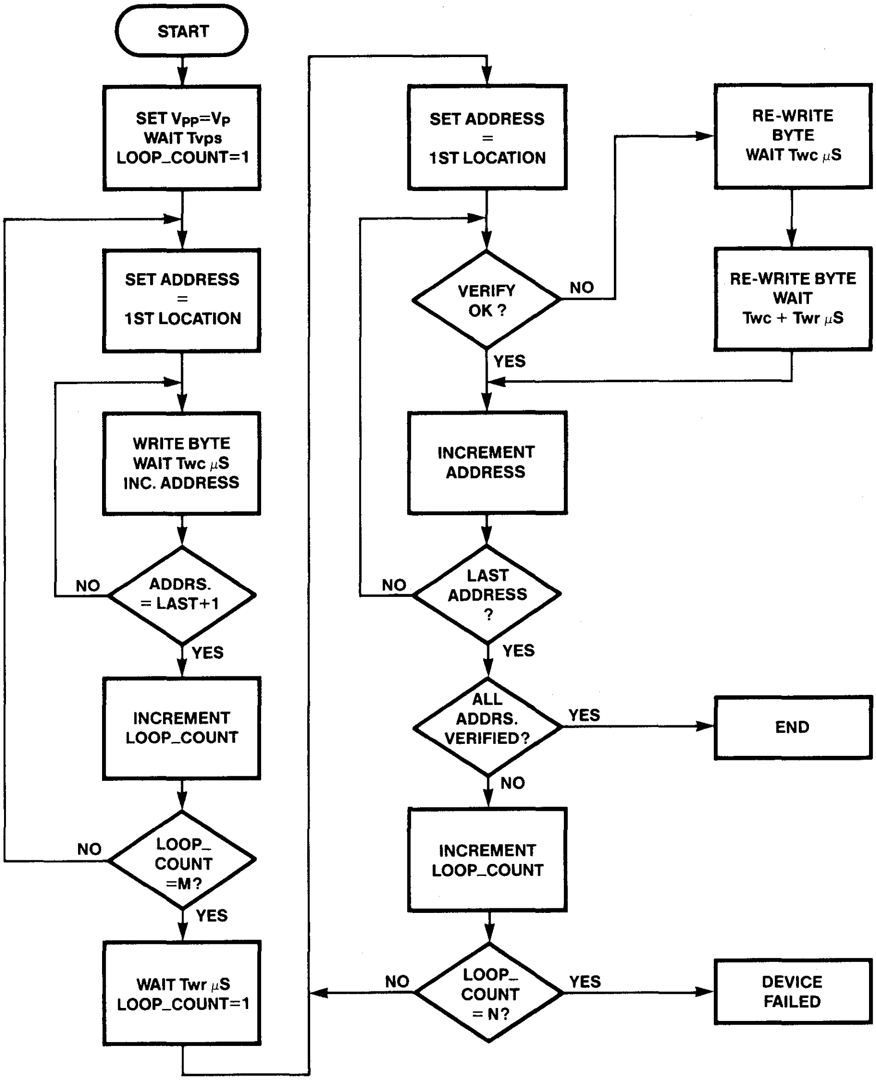
Byte Write Timing



Note: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g., access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Advance Data Sheets contain target product specifications which are subject to change upon device characterization over the full specified temperature range. These specifications may be changed at any time, without notice.

Figure 1
27F010 Write Algorithm



M=10
N=6

AC Characteristics

(Over the V_{CC} range)

SECTOR ERASE

Symbol	Parameter	27F010		Unit
		Min.	Max.	
t_{VPS}	V_{PP} setup time	2		μs
t_{VPH}	V_{PP} hold time	500		ms
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{OES}	$\overline{OE}$ setup time	0		ns
t_{AS}	Address setup time	20		ns
t_{AH}	Address hold time	100		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	0		ns
t_{WP}	$\overline{PGM}$ pulse width	100		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OEH}	$\overline{OE}$ hold time	0		ns
t_{ERASE}	Sector erase time		500	ms
t_{ABORT}	Sector erase delay		250	μs
t_{ER}	Erase recovery time		250	ms

Sector Erase Timing

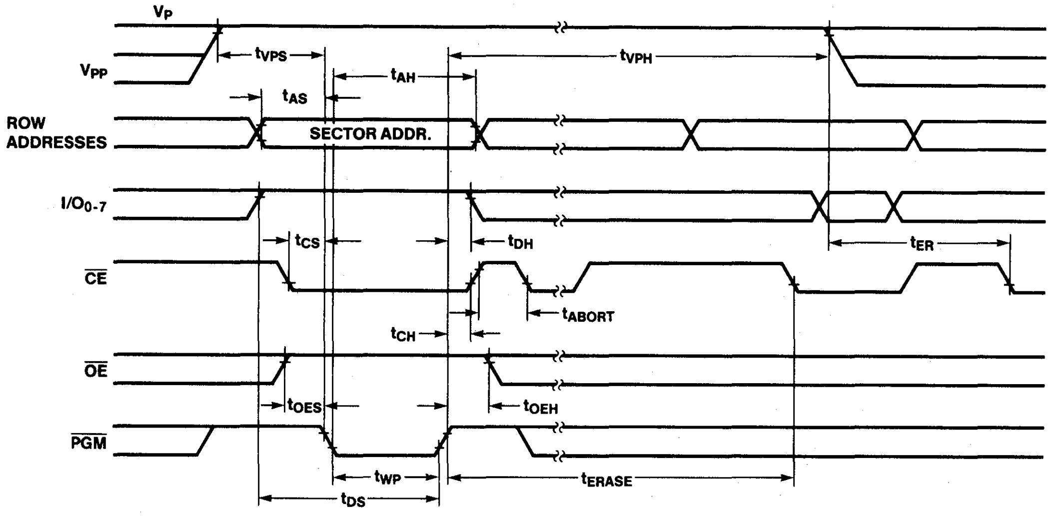
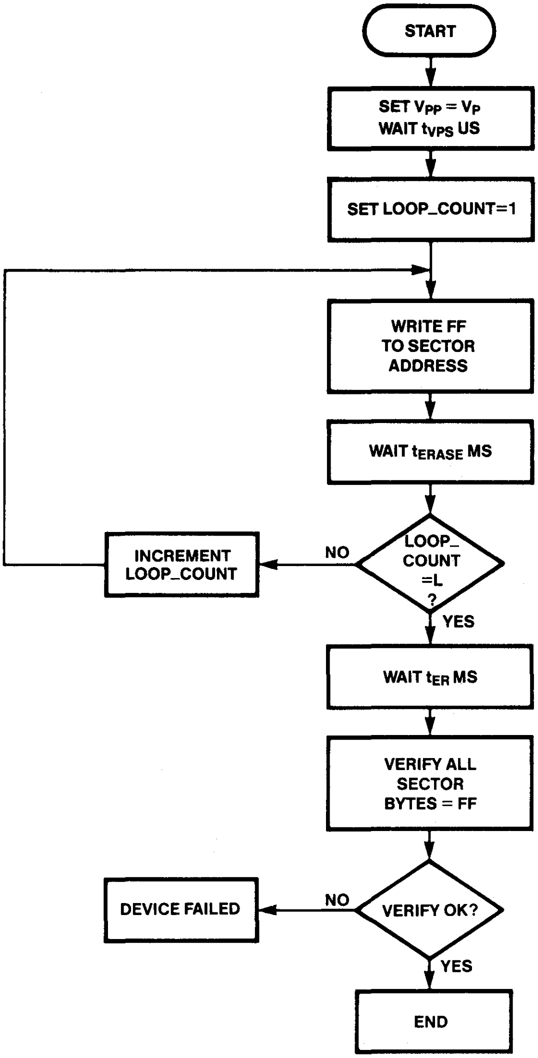


Figure 2
27F010 Sector Erase Algorithm



L=30

AC Characteristics

(Over the V_{CC} range)

CHIP ERASE

Symbol	Parameter	27F010		Unit
		Min.	Max.	
t_{VPS}	V_{PP} setup time	2		μs
t_{VPH}	V_{PP} hold time	500		ms
t_{CS}	$\overline{\text{CE}}$ setup time	0		ns
t_{OES}	$\overline{\text{OE}}$ setup time	0		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	0		ns
t_{WP}	$\overline{\text{PGM}}$ pulse width	100		ns
t_{CH}	$\overline{\text{CE}}$ hold time	0		ns
t_{OEH}	$\overline{\text{OE}}$ hold time	0		ns
t_{ERASE}	Chip erase time		500	ms
t_{ER}	Erase recovery time		250	ms

Chip Erase Timing

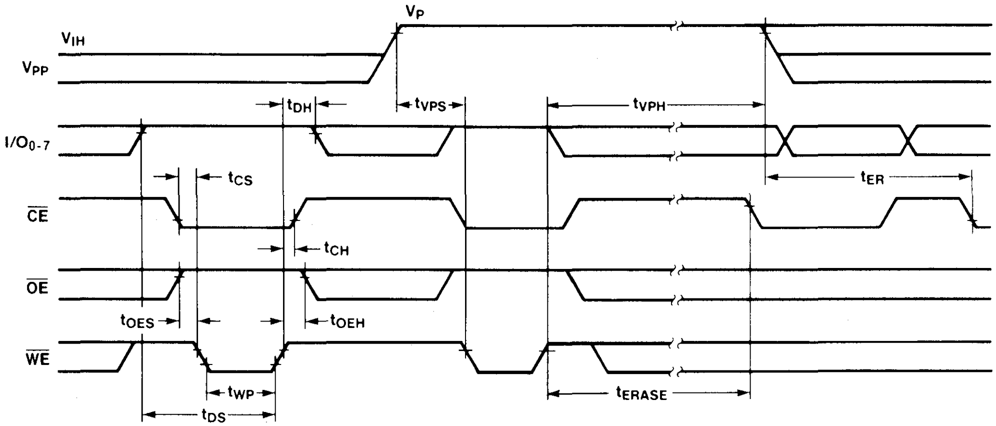
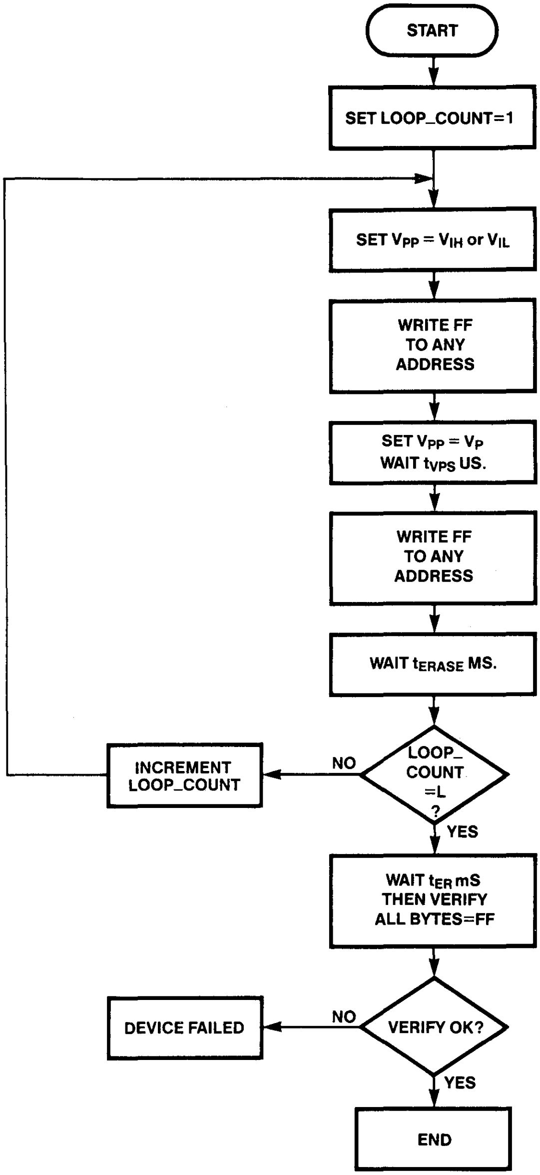


Figure 3
27F010 Chip Erase Algorithm



L=30

Ordering Information

D	**Q**	**27F010**	**–200**
Package Type	**Temperature Range**	**Device**	**Access Time**
D = Ceramic Dip	Q = 0 to 70°C	128K x 8 FLASH EPROM	200 = 200ns
P = Plastic Dip			250 = 250ns
N = Plastic Leaded Chip Carrier			300 = 300ns

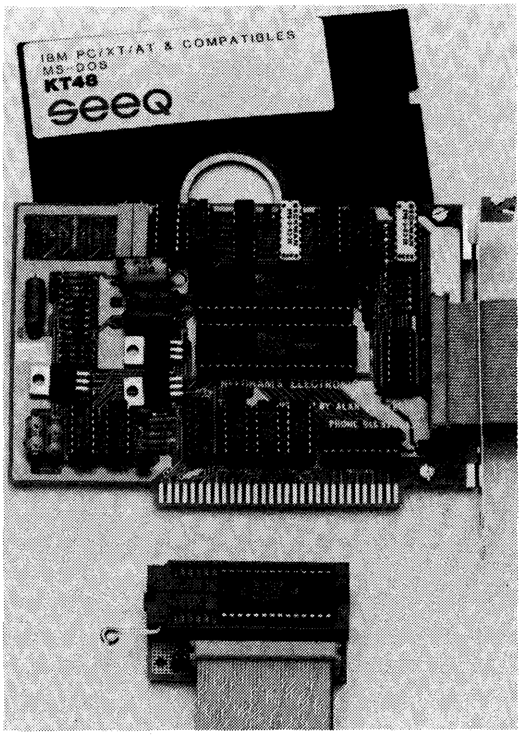
seeq

KT48
FLASH™ EEPROM PROGRAMMER

May 1988

Features

- **Programs SEEQ FLASH EEPROMs**
- **Half-card size programmer board fits into single expansion slot on IBM PC/XT/AT, with cable connector to a 40-pin ZIF DIP socket**
- **User-friendly menu driven software: Software resides on single floppy diskette**
- **Can load and save buffer: Reads/generates binary, Intel hex or Motorola S-record files**
- **Easy buffer editor with different entry modes including string and hex**
- **Split EEPROM feature allows splitting of 16- or 32-bit files**
- **Buffer allows stacking of code/data**



Description

KT48 is a FLASH EEPROM programmer from SEEQ Technology. The complete unit consists of a half-card size hardware board, a ribbon cable connected to a 40-pin ZIF DIP socket and MS/DOS compatible software. The programmer card fits into a single expansion slot on an IBM PC/XT/AT or IBM PC compatibles. The software is user friendly and menu driven. The programmer currently supports erasing/programming of SEEQ 128K-bit and 512K-bit density FLASH EEPROMs. Software updates will provide support for future members of SEEQ's FLASH product family.

KT48 enables an IBM PC to be turned into a local development station for program generation and product prototyping. By eliminating the need for separate downloading, the KT48 reduces the time needed for protyping/development work. The programmer erases/programs/verifies FLASH EEPROMs with one single socket insertion! Gone is the need for a UV-light eraser and 20 long minutes of waiting to erase a UV EPROM. These programmer features make program development easy, convenient, and cost effective.

Programmer Features:

All programmer commands are menu driven with user-selectable options. There is an online HELP system for programmer operation.

Erase Command: *This command erases the FLASH EEPROM and verifies erasure of the device. Errors, if any, are reported.*

Program Command: *This command programs the target device with data in the buffer memory and performs an automatic verification of programmed data. An automatic 'blank check' is also performed on the target device before programming. Errors, if any, are reported.*

Verify Erase Command: *This command is similar to a 'Blank Check.' Checks target device to see if it is erased. Errors, if any, are reported.*

Verify Data Command: *This command compares target device data to buffer data. Errors, if any, are reported.*

Read Command: *This command reads target device data into the buffer. Buffer size is automatically determined by the selection of the target device type.*

Configure System Command: *This command allows the user to specify port address selection for the programmer card, specify V_{CC} voltage levels during programming/erase and verify operations, select V_{PP} voltage during progamming/erase and Enable or Disable 'Beeper' sound prompts.*

Select Buffer Pointer Command: *This command is used to change the Buffer Pointer, normally 0. Using this command the user can divide or shuffle data/code for simplified partitioning into multiple FLASH EEPROM devices. For example, a 64K-byte large code can be split into four 16K-byte blocks—each small enough to be accommodated on a single 48128 device. Data can also be stacked into the buffer. For example, two 2764s (8K-bytes each) can be read into the buffer and re-programmed into a single 48128.*

Split FLASH EEPROM Command: *Using this command, 16- or 32-bit wide data can be split and programmed into standard 8-bit wide devices.*

Display/Modify Buffer Command: *This command displays buffer data. Using the buffer editor, data can be edited. The editor supports various entry modes including string and HEX.*

Read File Command: *This command reads a specified file from a disk into the buffer. Buffer size is determined by target device type selection. Binary, Intel HEX and Motorola S-record formats are supported. File Off-set option allows files to be off-set into the buffer as desired by the user.*

Save File Command: *This command allows buffer data to be saved to a disk under a specified file name. Binary, Intel HEX and Motorola S-record formats are supported. Buffer size i.e., length of the file is determined by the device type selected. Read and Save file commands allow 'Chip Master' copies to be maintained.*

Copy Buffer Command: *This command allows a user-defined block of buffer data to be copied into another block with a specified starting address.*

Print Buffer Command: *This command writes buffer data into a print file on the disk. The print file can be printed for a hard copy using MS/DOS print command or a word processing program.*

Fill Buffer Command: *This command fills the buffer with user specified data. User specifies starting address and ending address for the buffer fill command.*

Ordering Information

KT48-FLASH EEPROM Programmer

FLASH is a trademark of SEEQ Technology, Inc.

*IBM, XT, AT are trademarks of International Business Machines.

3

EPROMS

(Erasable Programmable Read Only Memories)

seeq

2764
64K EPROM
27128
128K EPROM

March 1987

Features

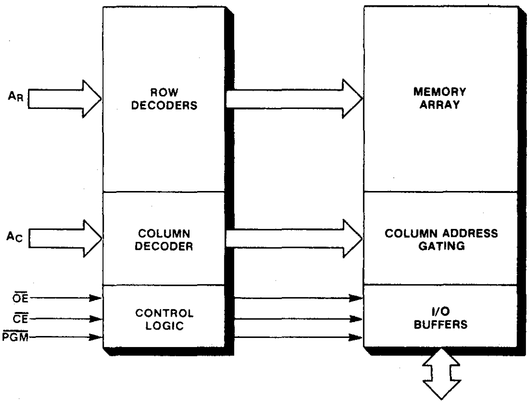
- **Fast Access Times at 0° to 70°C**
  - **— 2764 - 160 ns**
  - **— 27128 - 200 ns**
- **Programmed Using Intelligent Algorithm**
  - **— 21 V V_{PP}**
  - **— 2 Minutes for 27128**
  - **— 1 Minute for 2764**
- **JEDEC Approved Bytewide Pin Configuration**
  - **— 2764 8K x 8 Organization**
  - **— 27128 16K x 8 Organization**
- **Low Power Dissipation**
  - **— 100 mA Active Current**
  - **— 30 mA Standby Current**
- **Military And Extended Temperature Range Available**
- **Silicon Signature®**

Description

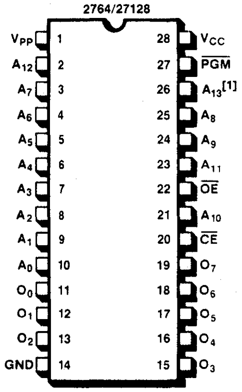
SEEQ's 2764 and 27128 are ultraviolet light erasable EPROMs which are organized 8Kx8 and 16Kx8 respectively. They are pin for pin compatible to JEDEC approved 64K and 128K EPROMs in all operational/programming modes. The devices have access times as fast as 160 ns over the 0° to 70°C temperature and V_{CC} tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 100 mA and 30 mA respectively. The fast access times allow higher system efficiency by eliminating the need for wait states in today's 8 - or 16-bit microprocessors.

Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to V_{pp} and a TTL "0" to pin 27 (program pin). The 2764 and 27128 may be programmed with an intelligent algorithm that is now

Block Diagram



Pin Configuration



NOTE 1: PIN 26 IS A NO CONNECT ON THE 2764.

Mode Selection

PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon Signature*	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}

* For Silicon Signature: A_O is toggled, A_9 = 12V, and all other addresses are at a TTL low.

Silicon Signature is a registered trademark of SEEQ Technology.

Pin Names

A_C	ADDRESSES — COLUMN (LSB)
A_R	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS
$\overline{PGM}$	PROGRAM

available on commercial programmers. The programming time is typically 5 ms/byte or 2 minutes for all 16K bytes of the 27128. The 2764 requires only half of this time, about a minute for 8K bytes. This faster time improves manufacturing throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, both EPROMs may be programmed using the conventional 50 ms programming specification of older generation EPROMs.

Incorporated on SEEQ's EPROMs is Silicon Signature. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, the product's fab location, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage .... -65° C to +150° C
Under Bias .... -10° C to +80° C
All Inputs or Outputs with
Respect to Ground .... +6V to –0.3V
V_{PP} During Programming with
Respect to Ground .... +22V to –0.3V
Voltage on A_9 with
Respect to Ground .... +15.5V to –0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	2764 27128
V_{CC} Supply Voltage[2]	5 V ± 10%
Temperature Range (Read Mode)	(Ambient) 0°C to 70°C
V_{PP} During Programming	21 ± 0.5 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter		Limits		Unit	Test Conditions
			Min.	Max.		
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{PP}[1]	V_{PP} Current	Read Mode		5	mA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode		30	mA	$V_{PP} = 21.5V$
I_{CC1}[1]	V_{CC} Standby Current			30	mA	$\overline{CE} = V_{IH}$
I_{CC2}[1]	V_{CC} Active Current			100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage		-0.1	0.8	V	
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4		V	$I_{OH} = -400$ μA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

AC Operating Characteristics During Read

Symbol	Parameter	Limits										Test Conditions
		2764-16		27XX-20		27XX-25		27XX-30		27XX-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address Access Time		160		200		250		300		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid		160		200		250		300		450	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Data Valid		75		75		100		120		150	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable to Output Float	0	60	0	60	0	60	0	105	0	130	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

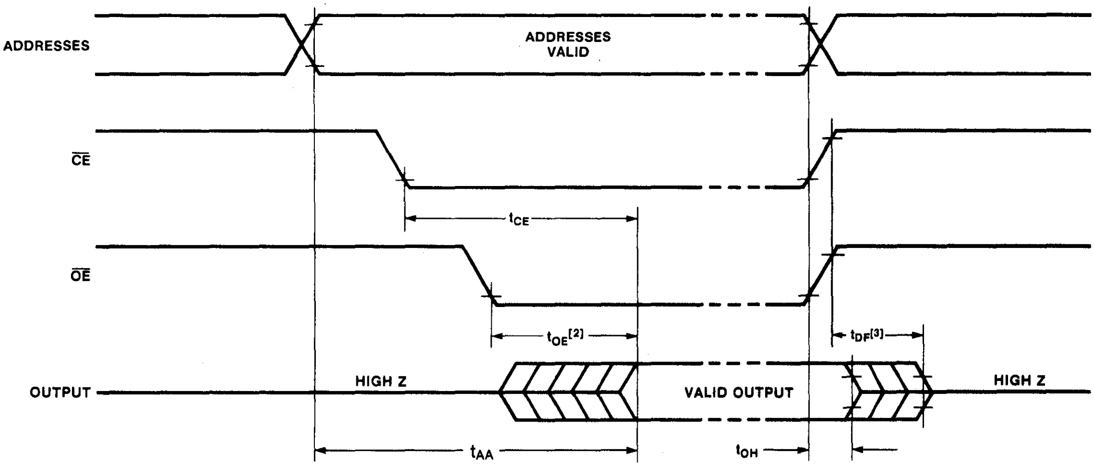
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:

1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{AA} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{AA}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

Erasure Characteristics

The 64K and 128K EPROMs are erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm^2. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer can proceed programming.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling (using TTL) the column address A_0. There are 2 bytes of data available (see Table 2). The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit. This mode is functional at 25 ± 5° C ambient temperature.

Table 2. Silicon Signature Bytes

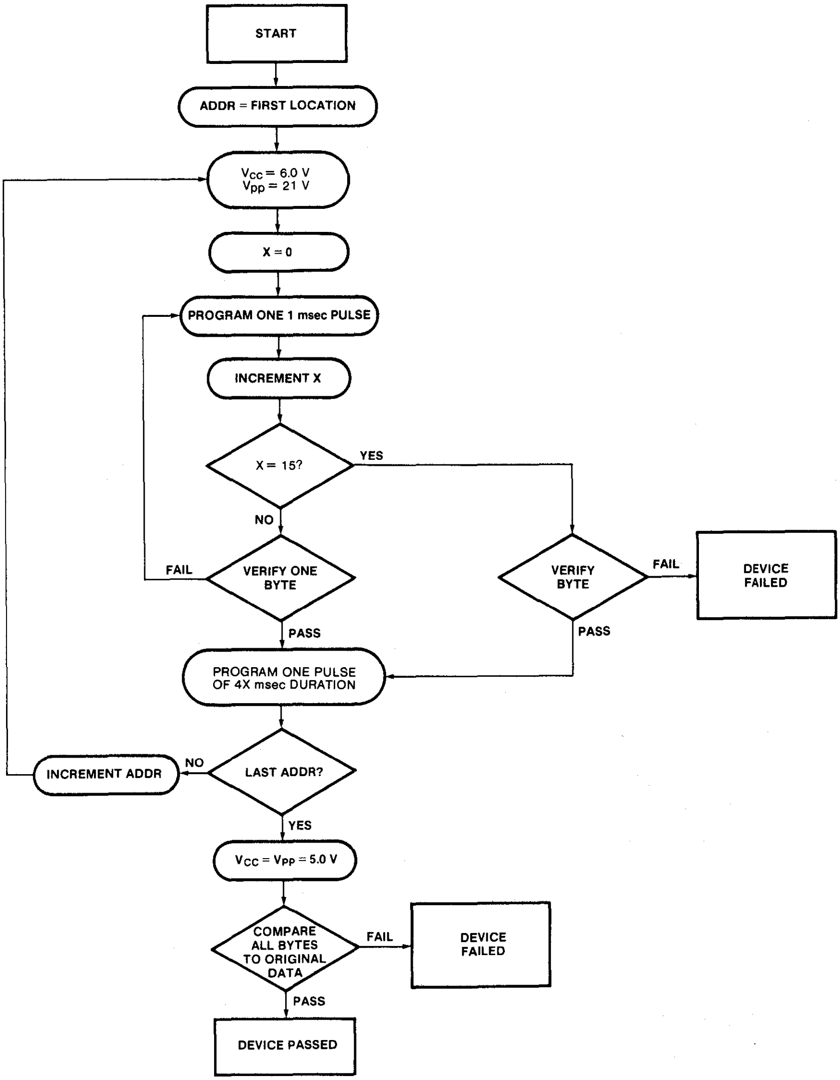
	A_0	Hex Data
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)		
2764	V_{IH}	40
27128	V_{IH}	C1

Programming

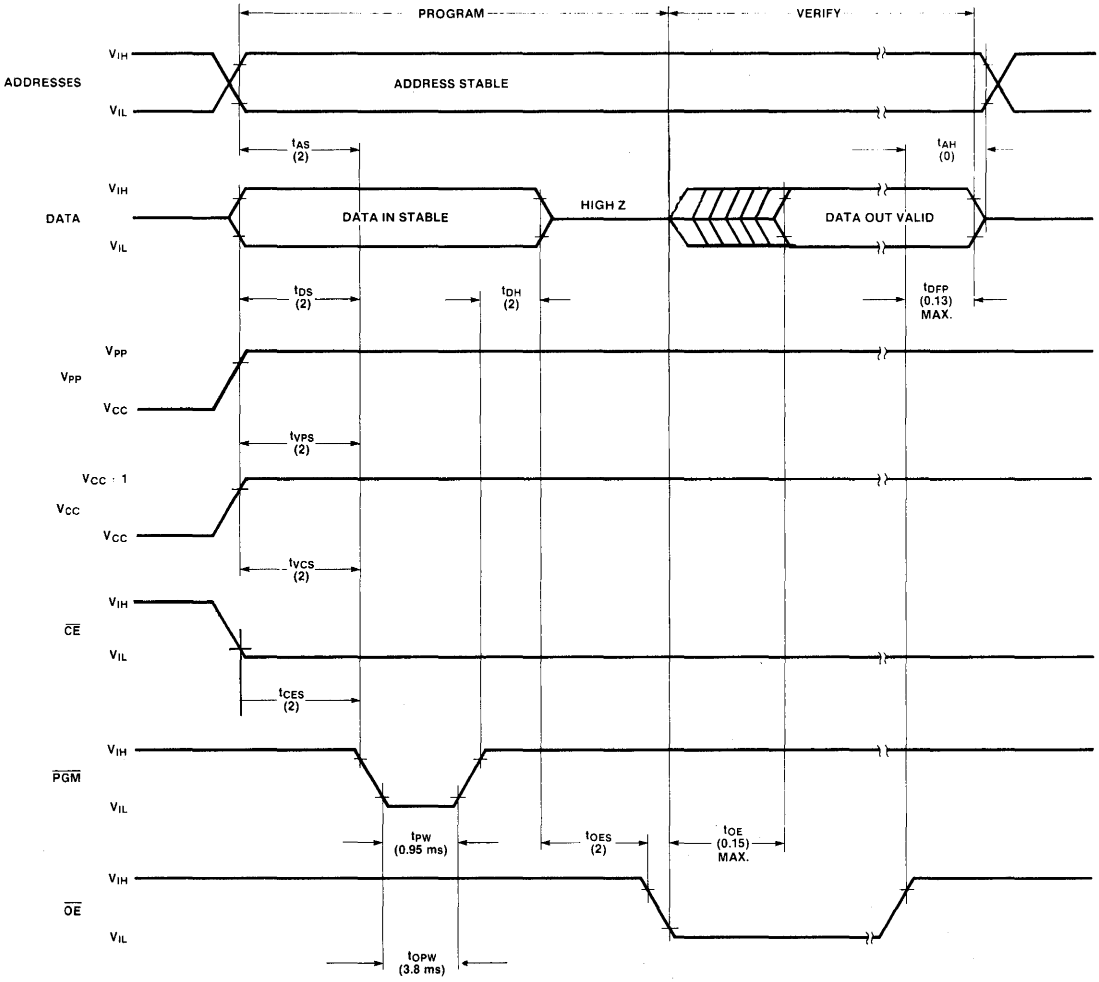
Both EPROMs may be programmed using an intelligent algorithm or with a conventional 50 msec programming pulse. The intelligent algorithm improves the total programming time by approximately 10 times over the conventional 50 msec algorithm. It typically requires only 1 and 2 minute programming time for all 64K and 128K bits respectively.

The intelligent algorithm requires V_{CC} = 6V and V_{PP} = 21V during byte programming. The initial program pulse width is one millisecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 4 times the number of one millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A maximum of 15 one millisecond pulses per byte should be applied to each address. When the intelligent algorithm cycle has been completed, all bytes must be read at V_{CC} = V_{PP} = 5V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A V_{IL} AND 2V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.

Intelligent Algorithm
AC Programming Characteristics[4] $T_A = 25° \pm 5° C$, V_{CC}[1] $= 6.0\ V \pm 0.25\ V$, $V_{PP} = 21\ V \pm 0.5\ V$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			μs
t_{OES}	$\overline{OE}$ Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}[2]	$\overline{PGM}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[3]	$\overline{PGM}$ Overprogram Pulse Width	3.8		63	ms
t_{CES}	$\overline{CE}$ Setup Time	2			μs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

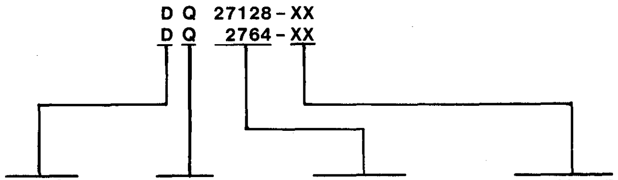
NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Initial Program Pulse width tolerance is 1 msec ± 5%.
3. The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
4. For 50 ms programming, $V_{CC} = 5\ V \pm 5\%$, $T_{PW} = 50$ ms ± 10%, and T_{OPW} is not applicable.

AC Test Conditions

Input Rise and Fall Times (10% to 90%) ...... 20 ns
Input Pulse Levels .... 0.45V to 2.4V
Input Timing Reference Level .... 0.8V and 2.0V
Output Timing Reference Level ...... 0.8V and 2.0V

Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME
			16-160 ns
			20-200 ns
D–CERDIP	Q-0°C to 70°C	2764-8K x 8 EPROM	25-250 ns
	(Commercial)	27128-16K x 8 EPROM	30-300 ns
			45-450 ns

seeq

27C256
256K CMOS EPROM

March 1987

Features

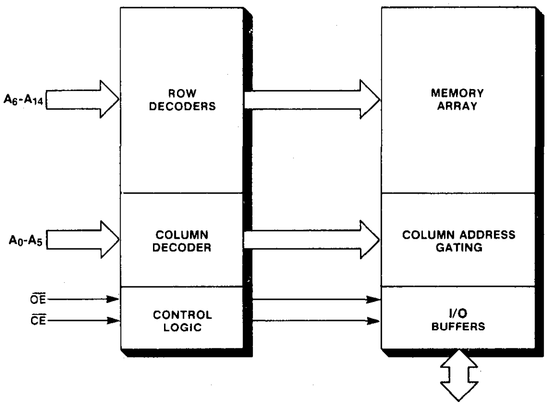
- **256K (32K x 8) CMOS EPROM**
- **Ultra Low Power**
  - **100 μA Max. V_{CC} Standby Current**
  - **40 mA Max. Active Current**
- **Programmed Using Intelligent Algorithm**
  - **12.5 V V_{pp}**
- **200 ns Access Times**
  - **5 V ±10% V_{CC}**
  - **0° to 70°C Temperature Range**
- **Minimum 10 Year Data Retention**
- **JEDEC Approved Bytewide Pin Configuration**
- **Silicon Signature®**
- **Military And Extended Temperature Range Available.**

Description

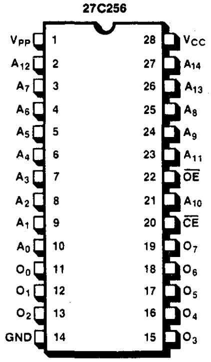
SEEQ's 27C256 is the industry's first 256K CMOS EPROM. It has a 32K x 8 organization and has very low power dissipation. Its 40 mA active current is less than one half the active power of n-channel EPROMs. In addition the 100 μA V_{CC} standby current is orders of magnitude lower than those same EPROMs. Consequently, system memory sizes can be substantially increased at a very small increase in power. Low active and standby power is important in applications which require portability, low cooling cost, high memory bit density, and long term reliability.

The 27C256 is specified over the 0° to 70°C temperature range and at 5 V ± 10% V_{CC}. The access time is specified at 200 ns, making the 27C256 compatible with most of today's microprocessors. Its inputs and outputs are completely TTL compatible.

Block Diagram



Pin Configuration



Mode Selection

PINS MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Silicon Signature™*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.

*For Silicon Signature: A_0 is toggled, A_9 = 12 V, and all other addresses are at a TTL low.

Silicon Signature is a registered trademark of SEEQ Technology.

Pin Names

A_0 - A_5	ADDRESSES — COLUMN (LSB)
A_6 - A_{14}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

Initially, and after erasure, all bits are in the "1" state. An intelligent algorithm is used to program the 27C256 typically in four minutes. Data is programmed using a 12.5 V V_{PP} and an initial chip enable pulse of 1.0 ms.

Incorporated on the 27C256 is Silicon Signature . Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage .... −65°C to +150°C
Under Bias .... −10°C to +80°C
All Inputs or Outputs with
Respect to Ground .... +6 V to −0.3 V
V_{PP} with Respect to Ground ...... +14.0 V to −0.3 V
Voltage on A_9 with
Respect to Ground .... +14.0 V to −0.3 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	27C256-20, 27C256-25, 27C256-30, 27C256-45,
V_{CC} Supply Voltage[1]	5 V ± 10%
Temperature Range (Read Mode)	(Ambient) 0°C to 70°C
V_{PP} During Read[2]	V_{CC}
V_{PP} During Programming[3]	12.5 ± 0.3 V

DC Operating Characteristics During Read or Programming

Symbol	**Parameter**	**Limits**		**Unit**	**Test Condition**
		Min.	**Max.**		
I_{IN}[4]	Input leakage		1	μA	$V_{IN}=V_{CC}$ Max.
I_O[5]	Output leakage		10	μA	$V_{OUT}=V_{CC}$ Max.
I_{PP}	V_{PP} current: Standby mode Read Mode Programming mode		 150 1 30	 μA mA mA	 $\overline{CE}=V_{CC}-1$ v. min. F=5 MHz., $\overline{CE}=V_{IL}$ $V_{PP}=12.5$ v.
I_{CC1}	V_{CC} standby current		100	μA	$\overline{CE}>=V_{CC}-1$ v.
I_{CC2}	V_{CC} standby current		1.5	mA	$\overline{CE}=V_{IH}$
I_{CC3}	V_{CC} active current		40	mA	$\overline{CE}=\overline{OE}=V_{IL}$, $O_{0-7}=0$, F=5 MHz.
V_{IL}	Input low voltage	−0.1	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC}+1$	V	
V_{OL}	Output low voltage		0.45	V	$I_{OL}=2.1$ ma.
V_{OH}	Output high voltage	2.4		V	$I_{OH}=-400$ μA.

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} cannot be left floating and should be connected to V_{CC} during read.
3. 0.1 μF ceramic capacitor on V_{PP} is required during programming only, to suppress voltage transients.
4. Inputs only. Does not include I/O.
5. For I/O only.

AC Characteristics Read Operation (Over Operating Temperature And V_{CC} Range, Unless Otherwise Specified)

Symbol	Parameter	Limits								Units	Test Conditions
		27C256-20		27C256-25		27C256-30		27C256-45			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{AA}	Address Access Time		200		250		300		450	ns	$\overline{CE}=\overline{OE}=V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		450	ns	$\overline{OE}=V_{IL}$
t_{OE}	Output Enable Access Time		75		100		120		150	ns	$\overline{CE}=V_{IL}$
t_{DF}	Output or Chip Enable off To Output Float[3]		60		60		105		130	ns	$\overline{CE}=V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE}=\overline{OE}=V_{IL}$

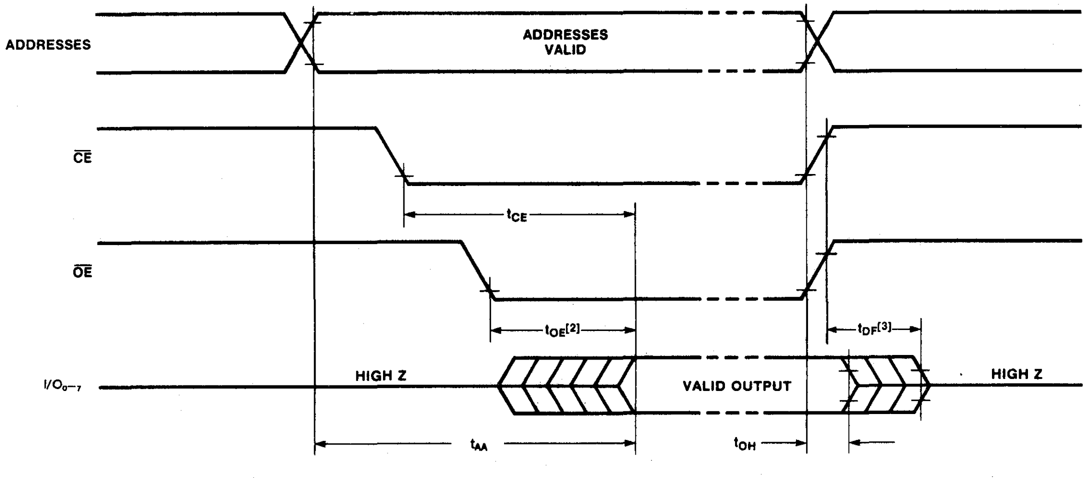
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{AA} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{AA}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

Erasure Characteristics

The 27C256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm^2. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling A_0. The data appears on outputs O_0 to O_6, with O_7 used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

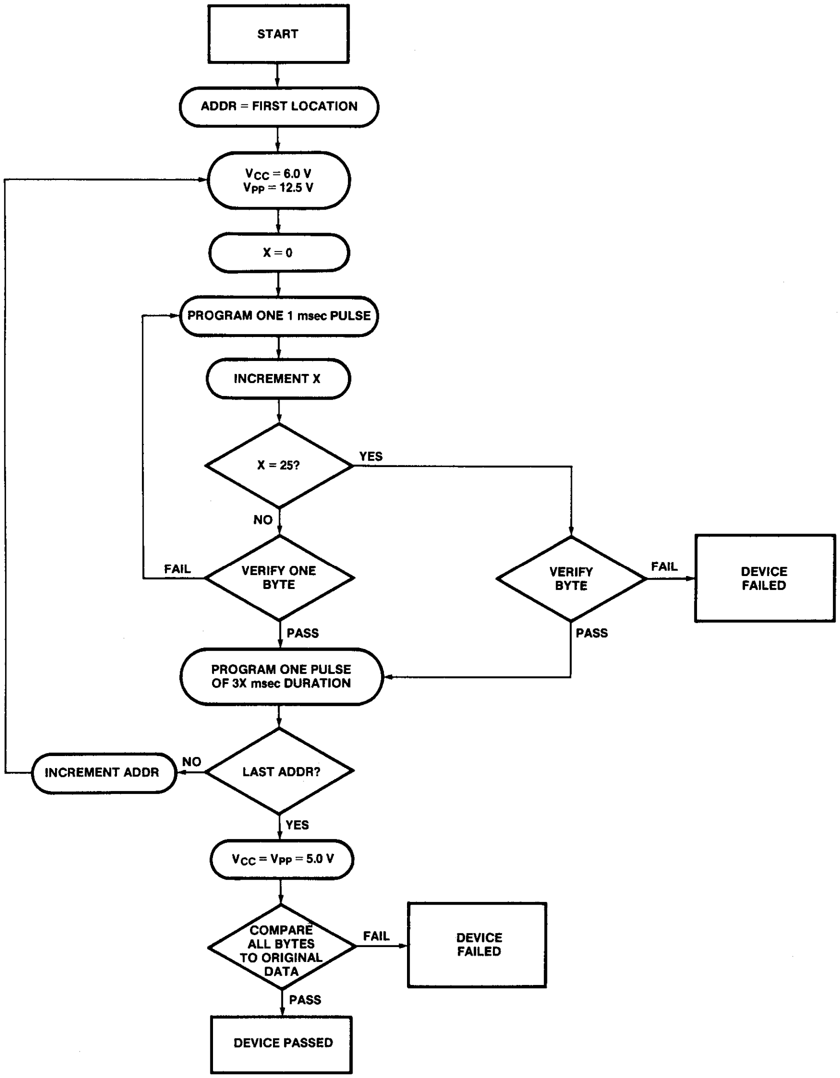
	A_0	Data (Hex)
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)	V_{IH}	C2

Programming

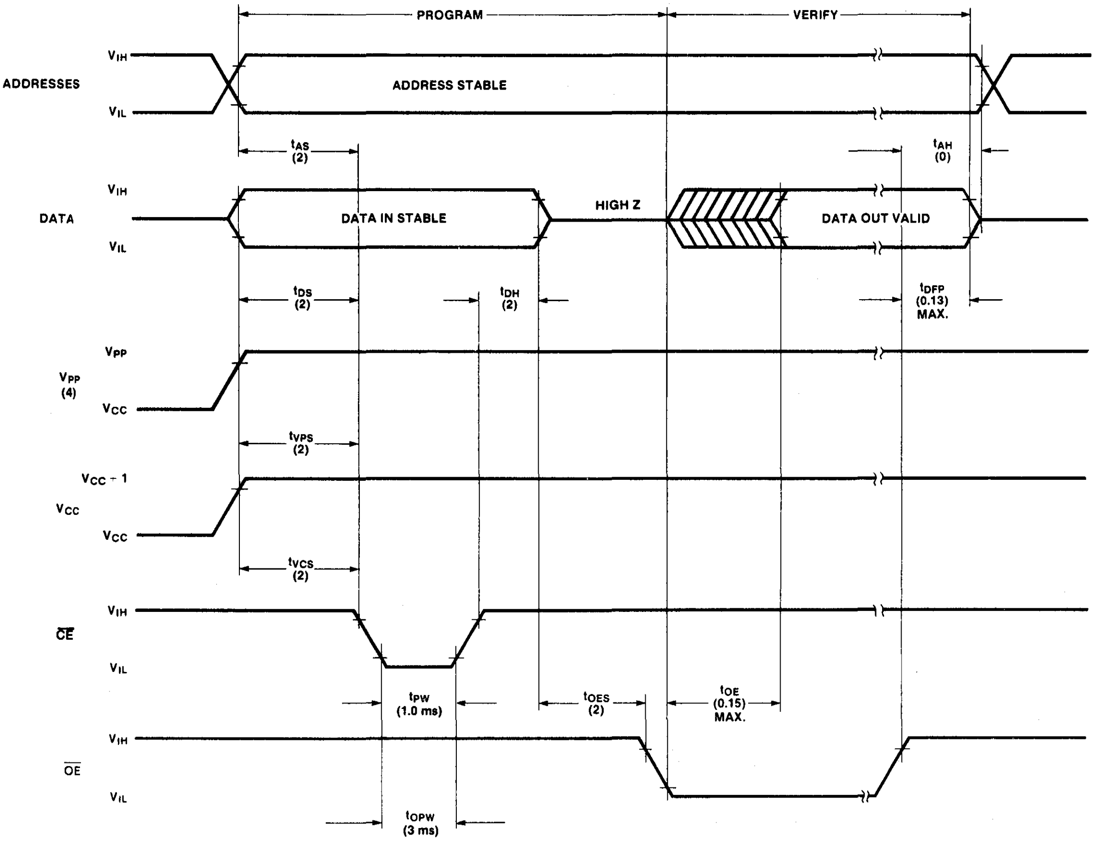
The 27C256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires $V_{CC} = 6$ V and $V_{PP} = 12.5$ V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X overpulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at $V_{CC} = V_{PP} = 5$ V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:

1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A V_{IL} AND 2 V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. 0.1 μF CERAMIC CAPACITOR ON V_{PP} IS REQUIRED DURING PROGRAMMING ONLY, TO SUPPRESS VOLTAGE TRANSIENTS.

Intelligent Algorithm

AC Programming Characteristics $T_A = 25° \pm 5°C$, V_{CC}[1] $= 6.0V \pm 0.25V$. $V_{PP} = 12.5V$

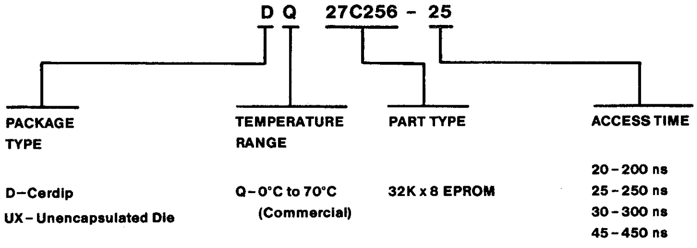
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			μs
t_{OES}	$\overline{OE}$ Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

AC Conditions of Test

Input Rise and Fall Times (10% to 90%) ...... 20 ns
Input Pulse Levels .... 0.45 V to 2.4 V
Input Timing Reference Level .... 0.8 V and 2.0 V
Output Timing Reference Level ..... 0.8 V and 2.0 V

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

Ordering Information



PACKAGE TYPE
D–Cerdip
UX–Unencapsulated Die

TEMPERATURE RANGE
Q–0°C to 70°C (Commercial)

PART TYPE
32K x 8 EPROM

ACCESS TIME
20–200 ns
25–250 ns
30–300 ns
45–450 ns

4 DATA COM

(Data Communications)

seeq

8003
EDLC® Ethernet Data Link Controller

October 1988

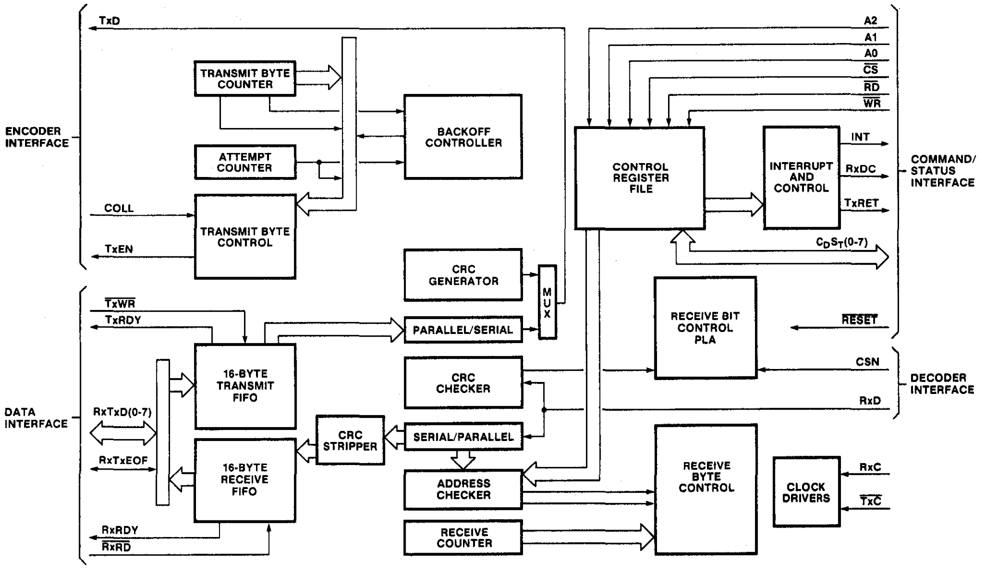
Features

- **Optimized for Burst Mode DMA Applications**
- **100% Ethernet/IEEE 802.3 (10BASE5) and IEEE802.3/CHEAPERNET (10BASE2)**
- **10 MHz Serial/Parallel Conversion**
- **Preamble Generation and Removal**
- **Automatic 32-Bit FCS (CRC) Generation and Checking**
- **Collision Handling, Transmission Deferral and Retransmission with Automatic Jam and Backoff Functions**
- **Error Interrupt and Status Generation**
- **40 Pin Package**
- **Single 5 V ±10% Power Supply**
- **Standard CPU and Peripheral Interface Control Signals**
- **Loopback Capability for Diagnostics**
- **Single Phase Clock**
- **Inputs and Outputs TTL Compatible**

Description

The SEEQ Ethernet Data Link Controller (EDLC) is designed to support the Data Link Layer (layer 2) of the Ethernet specification for Local Area Networks (LAN). The system interface is optimized for ease of connection to commonly available DMA Controllers and specifically for BURST MODE OPERATION. The 8003 interfaces directly to the 8023 Manchester Code Converter to complete the station resident Ethernet functions. The protocol used is Carrier Sense, Multiple Access with Collision Detection (CSMA/CD). The 8003 EDLC chip is a single 40 pin VLSI device which replaces approximately 60 MSI and SSI devices. It is designed to greatly simplify the development of Ethernet communication in computer based systems. The 8003 provides an economic solution for the construction of an Ethernet node, providing high speed data communication at 10 Megabits/second and sees applications in terminals, workstations, personal computers, small business systems, and large computer systems, in both the office and industrial environment. The 8003 EDLC chip has a universal system interface compatible with almost any microprocessor, microcomputer, or system bus, allowing the system designer to make the price/performance tradeoffs for each application. The transmit and receive sections of the EDLC chip are independent and can operate simultaneously to allow reception of a transmitted frame for use in loopback diagnostics modes.

Functional Block Diagram

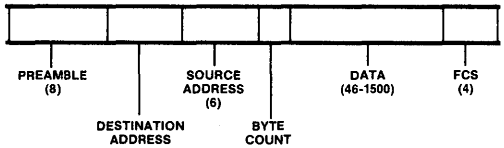


EDLC is a registered trademark of SEEQ Technology, Inc.

Functional Description

Frame Format

On an Ethernet communication network, information is transmitted and received in packets or frames. An Ethernet frame consists of a preamble, two address fields, a byte-count field, a data field, and a frame check sequence (FCS). Each field has a specific format which is described in detail below. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes exclusive of the preamble. The Ethernet frame format is shown below.



NOTE:
Field length in bytes in parentheses.

Preamble: *The preamble is a 64-bit field consisting of 62 alternating "1"s and "0"s followed by a "11" End-of-Preamble indicator.*

Destination Address: *The Destination Address is a 6-byte field containing either a specific Station Address, a Broadcast Address, or a Multicast Address to which this frame is directed.*

Source Address: *The Source Address is a 6-byte field containing the specific Station Address from which this frame originated.*

Byte-Count Field: *The Byte-Count Field consists of two bytes providing the number of valid data bytes in the Data Field, 46 to 1500. This field is uninterpreted at the Data Link Layer, and is passed through the EDLC chip to be handled at the Client Layer.*

Data Field: *The Data Field consists of 46 to 1500 bytes of information which are fully transparent in the sense that any arbitrary sequence of bytes may occur.*

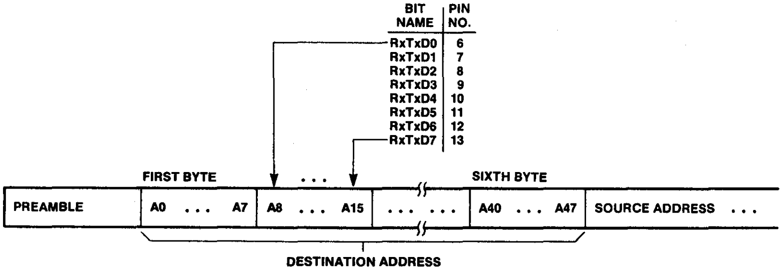
Frame Check Sequence: *The Frame Check Sequence (FCS) field is a 32-bit cyclic redundancy check (CRC) value computed as a function of the Destination Address Field, Source Address Field, Type Field, and Data Field. The FCS is appended to each transmitted frame, and used at reception to determine if the received frame is valid.*

Transmitting

The transmit data stream consists of the Preamble, four information fields, and the FCS which is computed in real time by the EDLC chip and automatically appended to the frame at the end of the serial data. The Preamble is also generated by the EDLC chip and transmitted immediately prior to the Destination Address. Destination Address, Source Address, Type Field and Data Field are prepared in the buffer memory prior to initiating transmission. The EDLC chip encapsulates these fields into an Ethernet frame by inserting a preamble prior to these information fields and appending a CRC after the information fields.

Transmission Initiation/Deferral

The Ethernet node initiates a transmission by storing the entire information content of the frame to be transmitted in an external buffer memory, and then transferring initial frame bytes to the EDLC Transmit FIFO. "Transmit-buffer to FIFO" transfers are coordinated via the $\overline{TxWR}$ and TxRDY handshake interface, i.e., bytes are written to the FIFO via $\overline{TxWR}$ only when TxRDY is HIGH. Actual transmission of the data onto the network will only occur if the network has not been busy for the minimum defer time (9.6 μs) and any Backoff time requirements have been satisfied. When transmission begins, the EDLC chip activates the transmit enable (TxEN) line concurrently with the transmission of the first bit of the Preamble and keeps it active for the duration of the transmission.



BITS WITHIN A BYTE ARE TRANSMITTED/RECEIVED BIT NO. "0" FIRST THROUGH BIT NO. "7" LAST.

Figure 1. Bit Serialization/Deserialization

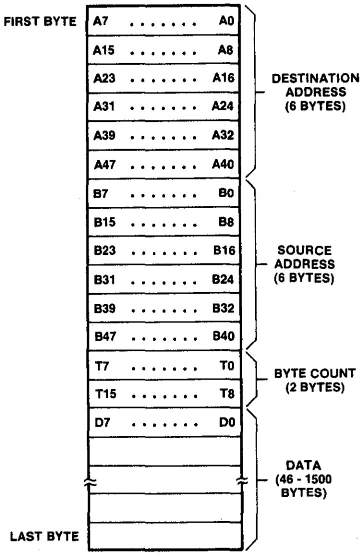


Figure 2. Typical Frame Buffer Format for Byte-Organized Memory

Collision

When concurrent transmissions from two or more Ethernet nodes occur (collision), the EDLC chip halts the transmission of the data bytes in the Transmit FIFO and transmits a Jam pattern consisting of 55555555 hex. At the end of the Jam transmission, the EDLC chip issues a TxRET signal to the CPU, and begins the Backoff wait period.

To reinitiate transmission, the initial bytes of the frame information fields must be reloaded into the EDLC Transmit FIFO. The TxRET is used to indicate to the buffer manager the need for frame reinitialization. The reloading of the Transmit FIFO may be done prior to the Backoff interval elapsing, so that no additional delay need be incurred to retransmission.

Scheduling of retransmission is determined by a controlled randomization process called Truncated Binary Exponential Backoff. The EDLC chip waits a random interval between 0 and 2^K slot times (51.2 µs per slot time) before attempting retransmission, where "K" is the current transmission attempt number (not to exceed 10).

When 16 consecutive attempts have been made at transmission and all have been terminated due to collision, the EDLC Transmit Control sets an error status bit and issues an interrupt to the CPU if enabled.

Terminating Transmission

Transmission terminates under the following conditions:

Normal: *The frame has been transmitted successfully without contention. Loading of the last data byte into the Transmit FIFO is signaled to the EDLC chip by activation of the RxTxEOF signal concurrently with the last byte of data loaded into the Transmit FIFO. This line acts as a ninth bit in the Transmit FIFO. When this last byte is serialized, the CRC is appended and transmitted concluding frame transmission. The Transmission Successful bit of the Transmit Status Register will be set by a normal termination.*

Collision: *Transmission attempted by two or more Ethernet nodes. The Jam sequence is transmitted, the Collision status bit is set, the TxRET signal is generated, and the Backoff interval begun.*

Underflow: *Transmit data is not ready when needed for transmission. Once transmission has begun, the EDLC chip on average requires one transmit byte every 800 ns in order to avoid Transmit FIFO underflow (starvation). If this condition occurs, the EDLC chip terminates the transmission, issues a TxRET signal, and sets the Transmit-Underflow status bit.*

16 Transmission Attempts: *If a Collision occurs for the sixteenth consecutive time, the 16-Transmission-Attempts status bit is set, the Collision status bit is set, the TxRET signal is generated, and the Backoff interval begun. The counter that keeps track of the number of collisions is modulo 16 and therefore rolls over on the 17th collision.*

At the completion of every transmission or retransmission, new status information is loaded into the Transmit Status Register. Dependent upon the bits enabled in the Transmit Command Register, an interrupt will be generated for the just completed transmission. In both collision and underflow the TxRET signal is activated.

Receiving

The EDLC chip is continuously monitoring the network. When activity is recognized via the Carrier Sense (CSN) line going active, the EDLC chip synchronizes itself to the incoming data stream during the Preamble, and then examines the destination address field of the frame. Depending on the Address Match Mode specified, the EDLC chip will either recognize the frame as being addressed to itself in a general or specific fashion or abort the frame reception.

Preamble Processing

The ELDC chip recognizes activity on the Ethernet via the Carrier Sense line. The Preamble is normally 64 *bits (8 bytes) long. The Preamble consists of a sequence of 62 alternating "1"s and "0"s followed by "11", with the frame information fields immediately following. In order for the decoder phase-lock to occur, the EDLC chip waits 16 bit times before looking for the "11" end of preamble indicator. If the EDLC chip receives a "00" before receiving the "11" in the Preamble, an error condition has occurred. The frame is not received, and the EDLC chip begins monitoring the network for a carrier again.*

Address Matching

Ethernet addresses consist of two 6-byte fields. The first bit of the address signifies whether it is a Station Address or a Multicast/Broadcast Address.

First Bit	*Address*
0	*Station Address (Physical)*
1	*Multicast/Broadcast Address (logical)*

Address matching occurs as follows:

Station Address: *All destination address bytes must match the corresponding bytes found in the Station Address Register.*

Multicast Address: *If the first bit of the incoming address is a 1 and the EDLC chip is programmed to accept Multicast Addresses, the frame is received.*

Broadcast Address: *The six incoming destination address bytes must all be FF hex. If the EDLC chip is programmed to accept Broadcast or Multicast Addresses the frame will be received.*

If the incoming frame is addressed to the EDLC chip specifically (Destination Address matches the contents of the Station Address Register), or is of general or group interest (Broadcast or Multicast Address), the EDLC chip will pass the frame exclusive of Preamble and FCS to the CPU buffer and indicate any error conditions at the end of the frame. If, however, the address does not match, as soon as the mismatch is recognized the EDLC chip will terminate reception and issue an RxDC.

The EDLC chip may be programmed via the Match Mode bits of the Receive Command Register to ignore all frames (Disable Receiver), accept all frames (Promiscuous mode), accept frames with the proper Station Address or the Broadcast Address (Station/Broadcast), or accept all frames with the proper Station Address, the Broadcast Address, or all Multicast Addresses (Station/Broadcast/Multicast).

Terminating Reception

Reception is terminated when either of the following conditions occur:

Carrier Sense Inactive: *Indicates that traffic is no longer present on the Ethernet cable.*

Overflow: *The host node for some reason is not able to empty the Receive FIFO as rapidly as it is filled, and an error occurs as frame data is lost. On average the Receive FIFO must be serviced every 800 ns to avoid this conditions.*

Frame Reception Conditions

Upon terminating reception, the EDLC chip will determine the status of the received frame and conditionally load it into the Receive Status Register. An interrupt will be issued if the appropriate conditions as specified in the Receive Command Register are present. The EDLC chip may report the following conditions at the end of frame reception:

Overflow: *The EDLC internal Receive FIFO overflows.*

Dribble Error: *Carrier Sense did not go inactive on a receive data byte boundary.*

CRC Error: *The 32-bit CRC transmitted with the frame does not match that calculated upon reception.*

Short Frame: *A frame containing less than 64 bytes of information was received (including FCS).*

Good Frame: *A frame is received that does not have a CRC error, Shortframe, or Overflow condition.*

System Interface

The EDLC chip system interface consists of two independent busses and respective control signals. Data is read and written over the Receive/Transmit Data Bus RxTxD (0-7). These transfers are controlled by the TxRDY and $\overline{\text{TxWR}}$ signals for transmitted data, and RxRDY and $\overline{\text{RxRD}}$ for received data. All Commands and Station Addresses are written, and all status read over a separate Command/Status Bus CdSt (0-7). These transfers are controlled by the $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and A0-A2 signals. The EDLC chip's command and status registers may be accessed at any time. However, it is recommended that writing to the command register be done only during interframe gaps.

With the exception of the two Match Mode bits in the Receive Command Register, all bits in both command registers are interrupt enable bits. Changing the interrupt enable bits during frame transmission does not affect the frame integrity. Asynchronous error events, however, e.g., overflow, underflow, etc., may cause chip operation to vary, if their corresponding enable bits are being altered at the same time.

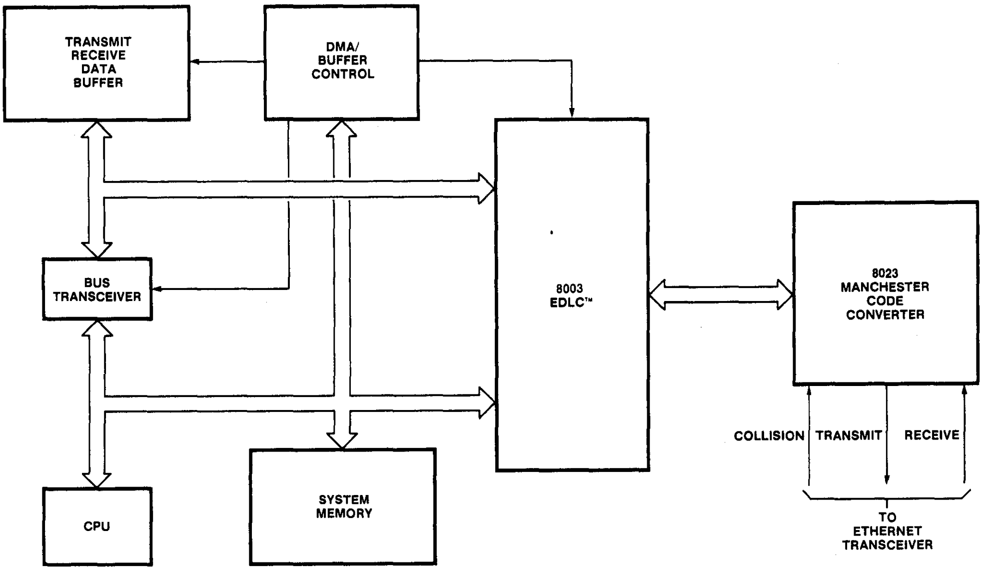


Figure 3. Typical Ethernet Node Configuration

Reading the status registers may also occur at any time during transmission or reception.

Internal Register Addressing

	Register Address			Register Description	
	A2	A1	A0	Read	Write
0	0	0	0	—	Station Addr 0
1	0	0	1	—	Station Addr 1
2	0	1	0	—	Station Addr 2
3	0	1	1	—	Station Addr 3
4	1	0	0	—	Station Addr 4
5	1	0	1	—	Station Addr 5
6	1	1	0	Rx Status	Rx Command
7	1	1	1	Tx Status	Tx Command

Status registers are read only registers. Command and Station Address registers are write only registers. Access to these registers is via the CPU interface: Control signals $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and the Command/Status Data Bus CdSt (0-7).

Station Address Register

The Station Address Register is 6 bytes in length. The contents may be written in any order, with bit "0" of byte "0" corresponding to the first bit received in the data stream, and indicating whether the address is physical or logical. Bit 7 of station address byte 5 is compared to the last bit of the received destination address. The Station Address should be programmed prior to enabling the receiver.

Transmit Command Register

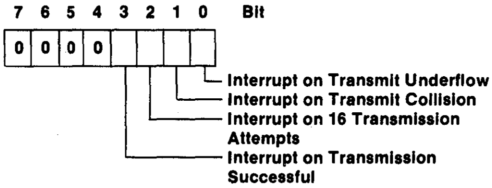
The Transmit Command Register is an interrupt mask register, which provides for control of the conditions allowed to generate transmit interrupts. Each of the four least significant bits of the register may be individually set or cleared. When set, the occurrence of the associated condition will cause an interrupt to be generated. The four specific conditions for which interrupts may be generated are:

- *Underflow*
- *Collision*
- *16 Collisions*
- *Transmission Successful*

The interrupt signal INT will be set when one or more of the specified transmission termination conditions occurs and the associated command bit has been set. The interrupt signal INT will be cleared when the Transmit Status Register is read.

All bits of the Transmit Command Register are cleared upon chip reset.

Transmit Command Register Format



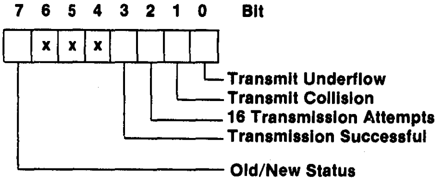
Transmission Successful is set only on the successful transmission or retransmission of a frame.

Transmit Status Register

The Transmit Status Register is loaded at the conclusion of each frame transmission or retransmission attempt. It provides for the reporting of both the normal and error termination conditions of each transmission.

The OLD/NEW status bit is set each time the Transmit Status Register is read, and reset each time new status is loaded into the Transmit Status Register. The OLD/NEW status bit is SET, and all other bits CLEARED upon chip reset.

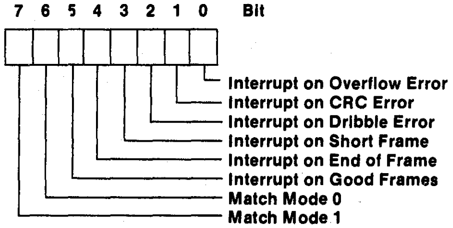
Transmit Status Register Format



Receive Command Register

The Receive Command Register has two primary functions, it specifies the Address Match Mode, and it specifies Frames-of-Interest. i.e. frames whose arrival must be communicated to the CPU via interrupts and status register updates. Frames-of-Interest are frames whose status must be saved for inspection, even at the expense of losing subsequent frames.

Receive Command Register Format



Bits 0-5 specify Interrupt and Frame-of-Interest when set. Bit 4, End of Frame, specifies any type of frame except overflow.

Match Mode Definition

	Match Mode 1	Match Mode 0	Function
0	0	0	Receiver Disable
1	0	1	Receive All Frames
2	1	0	Receive Station or Broadcast Frames
3	1	1	Receive Station, Broadcast/Multicast Frames

Changing the receive Match Mode bits during frame reception may change chip operation and give unpredictable results.

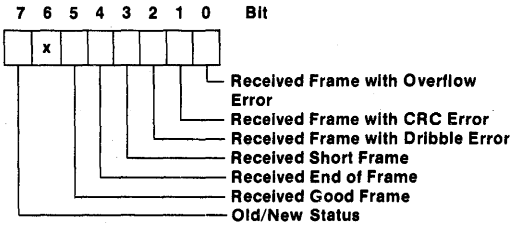
Interrupt Enable and Frames-of-Interest

Bits 0-5 when set specify interrupt generation on occurrence of the corresponding frame reception condition. They also specify the corresponding types of frames to be Frames-of-Interest for use by the Receive Status Register to control status loading.

Receive Status Register

The Receive Status Register is normally loaded with the status of each received frame when the frame has been received or frame reception has been terminated due to an error condition. In addition, this register contains the Old/New Status bit which is set when the Receive Status Register is read or the chip is reset, and cleared only when new status is loaded for a Frame-of-Interest (as defined by bits 0-5 of the Receive Command Register). All other bits are cleared upon chip reset.

Receive Status Register Format



The Old/New Status bit write-protects the Receive Status Register while it contains unread status for a Frame-of-Interest. When this bit is zero, the register is write-protected. The Old/New Status bit is cleared whenever the status of a new Frame-of-Interest is loaded into the Receive Status Register and is set after that status is read. When zero, it indicates "new status for a Frame-of-Interest".

Thus the status of any frame received following the reception of a Frame-of-Interest will not be loaded into the Receive Status Register unless the previous status has been read. If any following frame is received before the status of the previous Frame-of-Interest has been read, the new status will not be loaded, the Receive Discard (RxDC) signal will be issued and the Receive FIFO will be cleared.

With this one exception caused by a write-protect condition, the status of each frame is always loaded into the Receive Status Register on completion of reception.

Any frame received will cause an interrupt to be generated if the corresponding Interrupt Enable bit is set. This interrupt is reset upon reading the Receive Status Register.

These conditions ensure that a maximum number of good frames are received and retained.

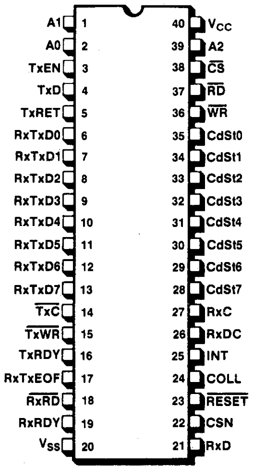


Figure 4. Pin Configuration

Pin Description

The EDLC chip has four groups of interface signals:

- *Power Supply*
- *Encoder/Decoder*
- *Data Buffer*
- *Command/Status*

Power Supply

V_{CC} .... *+5 V*

V_{SS} .... *Ground*

Encoder/Decoder Interface

$\overline{\text{TxC}}$ Transmit Clock (Input): *10 MHz, 50% duty cycle transmit clock used to synchronize the transmit data from the EDLC chip to the encoder. This clock runs continuously, and is asynchronous to RxC.*

TxD Transmit Data (Output): *Serial data output to the encoder. Active HIGH.*

TxEN Transmit Enable (Output): *This signal is used to activate the encoder. It becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. Active HIGH and cleared by Reset.*

RxC Receive Clock (Input): *10 MHz, 50% duty cycle nominal. The receive clock is used to synchronize incoming data to the EDLC chip from the decoder. This clock runs continuously, and is asynchronous to $\overline{\text{TxC}}$.*

RxD Receive Data (Input): *Serial input data to the EDLC chip from the decoder. Active HIGH.*

CSN Carrier Sense (Input): *Indicates traffic on the coaxial cable to the EDLC chip. Becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. Active HIGH.*

COLL Collision (Input): *Indicates transmission contention on the Ethernet cable. The Collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.*

Data Buffer Interface

RxTxD (0-7) Receive/Transmit Data Bus (I/O): *Carries Receive/Transmit data byte from/to the EDLC chip Receive/Transmit FIFOs.*

RxTxEOF Receive/Transmit End of Frame (I/O): *Indicates last byte of data on the Receive/Transmit Data Bus. Effectively a ninth bit in the FIFOs with identical timing to RxTxD (0-7). Active HIGH.*

RxRDY Receive Ready (Output): *Indicates that at least one byte of received data is available in the Receive FIFO. This signal will remain active high as long as one byte of data remains in the Receive FIFO. When this condition no longer exists, RxRDY will be deasserted with respect to the leading edge of the $\overline{\text{RxRD}}$ strobe that removes the last byte of data from the Receive FIFO. $\overline{\text{RxRD}}$ should not be activated if RxRDY is low. Active HIGH and cleared by Reset.*

$\overline{\text{RxRD}}$ Receive Read Strobe (Input): *Enables transfer of received data from the EDLC Receive FIFO to the RxTxD Bus. Data is valid from the EDLC Receive FIFO at the RxTxD pins on the rising edge of this signal. This signal should not be activated unless RxRDY is high. Active LOW.*

RxDC Receive Discard (Output): *Asserted when one of the following conditions occurs, and the associated Interrupt Enable bit in the Receive Command Register is reset. (1) Receive FIFO overflow. (2) CRC Error. (3) Short Frame Error. (4) Receive frame address non-match or (5) current frame status lost because previous status was not read. RxDC does not activate on errors when the associated Interrupt Enable bit is set. In this case, EOF will be generated instead when the Receive FIFO is read out. This allows reception of frames with errors. RxDC acts internally to clear the Receive FIFO.*

TxRDY Transmit Ready (Output): *Indicates that the Transmit FIFO has space available for at least one data byte. This signal will remain active high as long as one byte of space exists for transmitted data to be written into. When this condition no longer exists, TxRDY will be deasserted with respect to the leading edge of the $\overline{\text{TxWR}}$ strobe that fills the Transmit FIFO. TxRDY is forced inactive during Reset, and when TxRET is active. Active HIGH. Goes high after Reset.*

$\overline{\text{TxWR}}$ Transmit Write (Input): *Synchronizes data transfer from the RxTxD Bus to the Transmit FIFO. Data is written to the FIFO on the rising edge of this signal. This signal should not be active unless TxRDY is high. Active LOW.*

TxRET Transmit Retransmit (Output): *Asserted whenever either transmit underflow or transmit collision conditions occur. It is nominally 800 ns in width. Active HIGH. Asserted by Reset.*
TxRET clears the internal Transmit FIFO.

Command/Status Interface

CdSt (0-7) Command/Status Data Bus (I/O): *These lines carry commands and status as well as station address initialization information between the EDLC chip and CPU. These lines are nominally high impedance until activated by $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being simultaneously active.*

A0-A2 Address (0-2) (Input): *Address lines to select the proper EDLC internal registers for reading or writing.*

$\overline{\text{CS}}$ Chip Select (Input): *Chip Select input, must be active in conjunction with $\overline{\text{RD}}$ or $\overline{\text{WR}}$ to successfully access the EDLC internal registers. Active LOW.*

$\overline{\text{RD}}$ Read (Input): *Enables reading of the EDLC internal registers in conjunction with $\overline{\text{CS}}$. Data from the internal registers is enabled via the falling edge of $\overline{\text{RD}}$ and is valid on the rising edge of the signal. Active LOW.*

$\overline{\text{WR}}$ Write (Input): *Enables writing of the EDLC internal registers in conjunction with $\overline{\text{CS}}$. Write data on the CdSt (0-7) data lines must be set up relative to the rising edge of the signal. Active LOW.*

INT Interrupt (Output): *Enabled as outlined above by a variety of transmit and receive conditions. Remains active until the status register containing the reason for the interrupt is read. Active HIGH.*

$\overline{\text{RESET}}$ (Input): *Initializes control logic, clears command registers, clears the Transmit Status Register, clears bits 0-5 of the Receive Status Register, sets the Old/New Status bit (bit 7 of the Receive Status Register), asserts RxDC and TxRET and clears the Receive and Transmit FIFOs. In addition, TxRDY is forced low during a reset. TxRDY goes high when $\overline{\text{RESET}}$ goes high, indicating the EDLC chip is ready to transmit. $\overline{\text{RESET}}$ is active LOW.*

Absolute Maximum Ratings

Ambient Temperature
Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +150°C
All Input or Output Voltages
with Respect to Ground .... +6 V to −0.3 V
Package Maximum Power Dissipation ..... 1.5 Watts

DC Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 5\%$

Symbol	Paramater	Limits[1]			Units	Condition
		Min.	Typ.	Max.		
I_{IN}	Input Leakage Current			10	μA	V_{IN} = 0.45 V to 5.25 V
I_O	Output Leakage Current			10	μA	V_{OUT} = 0.45 V to 5.25 V
I_{CC}	V_{CC} Current		150	200	mA	
V_{CH}	Clock Input High Voltage	3.5		6	V	
V_{CL}	Clock Input Low Voltage			0.8	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH_1}	Input High Voltage	2.0		6	V	Except $\overline{\text{TxWR}}$ and $\overline{\text{RxRD}}$
V_{IH_2}	Input High Voltage	3.0		6	V	$\overline{\text{TxWR}}$ and $\overline{\text{RxRD}}$
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

NOTE:
1. Typical values are for T_A = 25° C and nominal supply voltages.

Operating Conditions

Ambient Temperature Range .... 0° C to 70° C
V_{CC} Power Supply .... 4.50 V to 5.50 V

Capacitance[6] $T_A = 25°C$, $F_C = 1$ MHz

Symbol	Parameter	Maximum	Condition
C_{IN}	Input Capacitance	15 pF	$V_{IN} = 0$ V
$C_{I/O}$	I/O Capacitance	15 pF	$V_{I/O} = 0$ V

AC Test Conditions

Output Load: 1 Schottky TTL Gate + CL = 100 pF
(All pins except TxEN, TxD)
TxEN, TxD Load: 1 Schottky TTL Gate + CL = 35 pF
Input Pulse Level: 0.4 V to 2.4 V
Timing Reference Level: 1.5 V

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5\ V \pm 5\%$

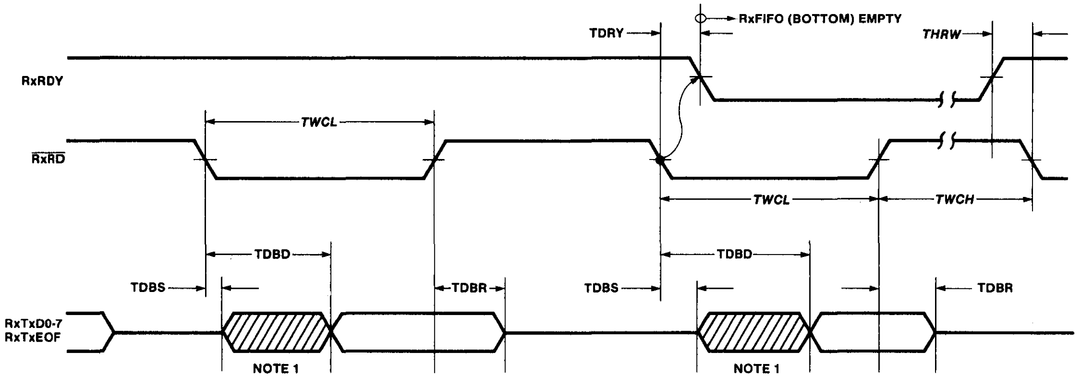
Symbol[5]	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units (ns)	Condition
DATA AND COMMAND/STATUS INTERFACE TIMING						
TDBD	RxTx/CdSt Bus Data Delay			150	ns	
TDBR	RxTx/CdSt Bus Release Delay	10			ns	
TDBS	RxTx/CdSt Bus Seizure Delay	10		150	ns	
TDRY	RxRDY/TxRDY Clear Delay			100	ns	
THAR	A_{0-2}/$\overline{\text{CS}}$ Hold	10			ns	
THDA	RxTx/CdSt Bus Hold	0			ns	
THRW	$\overline{\text{RxRD}}$/$\overline{\text{TxWR}}$ Hold	0			ns	
TSAR	A_{0-2}/$\overline{\text{CS}}$ Setup	0			ns	
TSCS	CdSt Bus Setup	90			ns	
TSRT	RxTx Bus Setup	90			ns	
TWCH	$\overline{\text{RxRD}}$/$\overline{\text{TxWR}}$/$\overline{\text{RD}}$//$\overline{\text{WR}}$ High Width	100			ns	
TWCL	$\overline{\text{RxRD}}$/$\overline{\text{TxWR}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ Low Width	200		10,000	ns	

Symbol[5]	Parameter	Limits Min.	Limits Typ.	Limits Max.	Units (ns)	Condition
SERIAL TRANSMIT AND RECEIVE INTERFACE TIMING						
TDDC	RxDC Set Delay	800			ns	Note 1
TDIC	INT Clear Delay			150	ns	
TDRE	TxRET Set Delay	2400		3400	ns	Note 3
TDRI	Receive INT Delay	1000			ns	Note 2
TDTD	TxD/TxEN Delay	20		60	ns	Cl = 35 pF
TDTI	Transmit INT Delay	1200			ns	Note 4
THRD	RxD Hold	20			ns	
TPCK	RxC/$\overline{\text{TxC}}$ Clock Period	95		1000	ns	
TSRD	RxD Setup	30			ns	
TWDC	RxDC High Width	600			ns	
TWRC	RxC High/Low Width	45			ns	
TWRE	TxRET High Width	600			ns	
TWRS	$\overline{\text{RESET}}$ Low Width	10,000			ns	
TWTC	$\overline{\text{TxC}}$ High/Low Width	45			ns	
TWCO	COLL Width	50			ns	

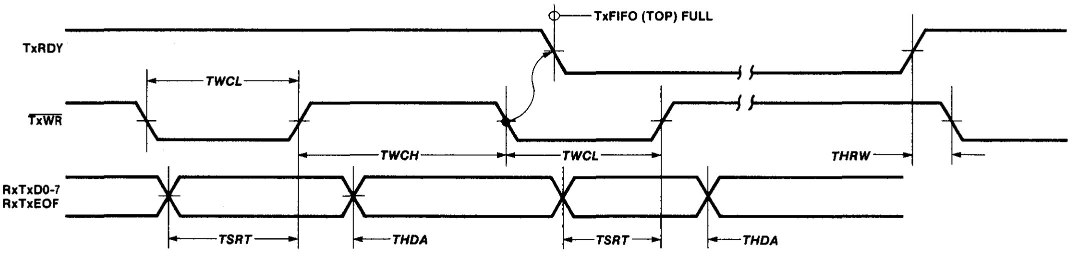
NOTES:

1. For frame reception with Shortframe or CRC Error. If frame reception is terminated due to Overflow, RxDC will be issued within 1.2 μs of Overflow. If frame reception is terminated due to non-match of address, RxDC will be issued within 2.4 μs of the receipt of the last address bit.
2. Normal frame reception without Overflow. If frame reception is terminated due to Overflow, INT will be issued within 1.2 μs of Overflow.
3. For TxRET caused by Collision or 16 Collision condition. If transmission is terminated due to Underflow TxRET will be issued within 1.2 μs of the Underflow.
4. For INT caused by Collision or 16 Collision condition. If caused by Underflow, INT will be issued within 1.2 μs. If caused by normal termination, INT will be issued within 200 ns of TxEN going LOW.
5. Italics indicate input requirement, non-italics indicate output timing.
6. Characterized. Not tested.

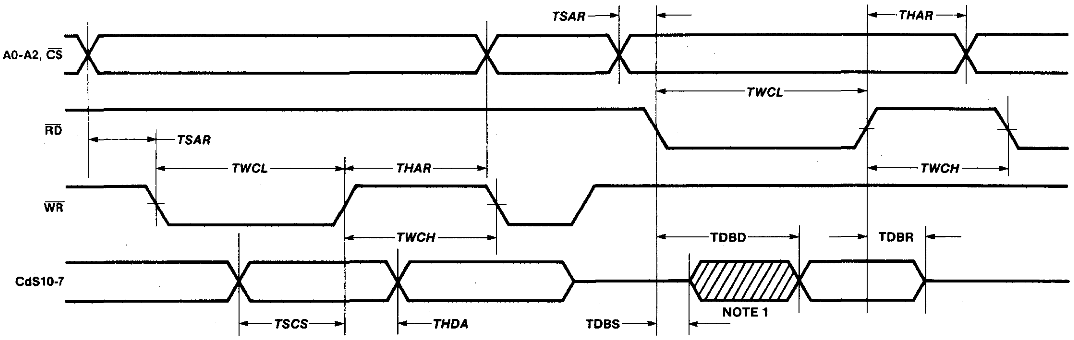
RECEIVE DATA INTERFACE TIMING



TRANSMIT DATA INTERFACE TIMING

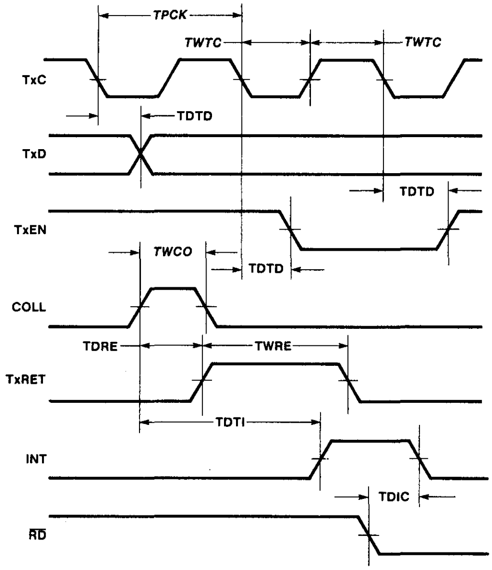


COMMAND/STATUS INTERFACE TIMING

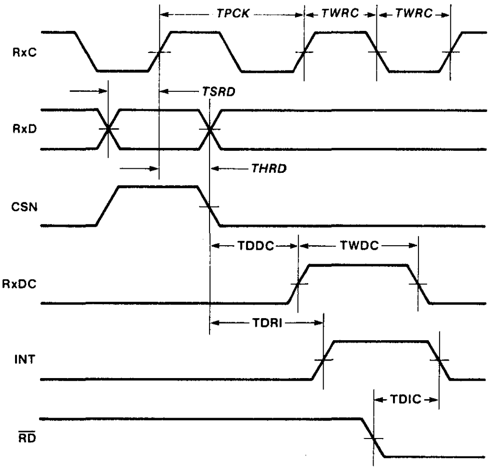


NOTE 1: BUS IS DRIVEN AT THIS TIME. HOWEVER, NO VALID INFORMATION PRESENT.

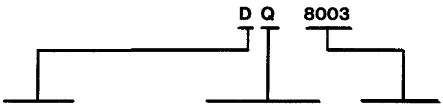
SERIAL TRANSMIT INTERFACE TIMING



SERIAL RECEIVE INTERFACE TIMING



Ordering Information



D Q 8003

PACKAGE TYPE
D = Ceramic DIP
P = Plastic DIP

TEMPERATURE RANGE
Q – 0°C to +70°C

PART TYPE
EDLC®

seeq

8020
MCC™ Manchester Code Converter

PRELIMINARY DATA SHEET

October 1988

Features

- ***Compatible with IEEE 802.3/Ethernet (10BASE5), IEEE802.3/Cheapernet (10BASE2) and Ethernet Rev. 1 Specifications***
- ***Compatible with the 8003 EDLC®, 8005 Advanced EDLC***
- ***Manchester Data Encoding/Decoding and Receiver Clock Recovery with Phase Locked Loop (PLL)***
- ***Receiver and Collision Squelch Circuit and Noise Rejection Filter***
- ***Differential TRANSMIT Cable Driver***
- ***Loopback Capability for Diagnostics and Isolation***
- ***Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission***
- ***20 MHz Crystal Oscillator***
- ***Transceiver Interface High Voltage (16 V) Short Circuit Protection***
- ***Low Power CMOS Technology with Single 5V Supply***
- ***20 pin DIP & PLCC Packages***

Functional Block Diagram

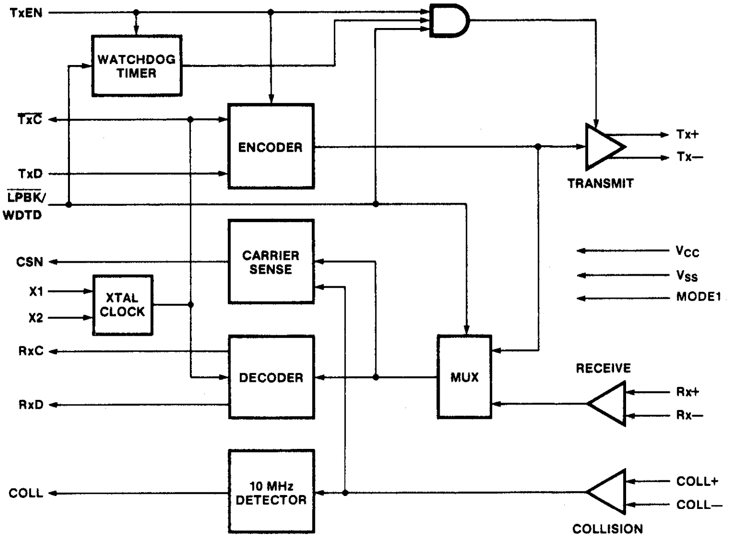


Figure 1. 8020 MCC® Manchester Code Converter Block Diagram.

Description

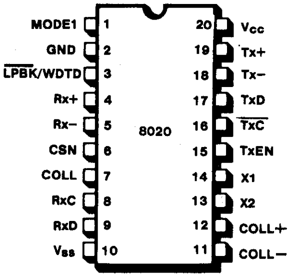
The SEEQ 8020 Manchester Code Converter chip provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the SEEQ 8003 and 8005 Controllers and any standard Ethernet transceiver as defined by IEEE 802.3 and Ethernet Revision 1.

The SEEQ 8020 MCC™ is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the 8020 includes a watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

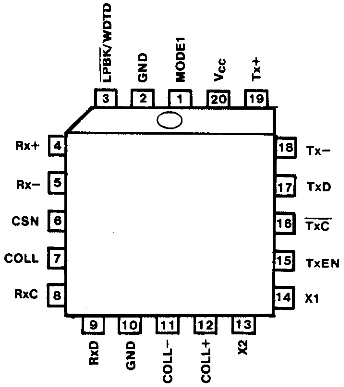
Together with the 8003 or 8005 and a transceiver, the 8020 Manchester Code Converter provides a high performance minimum cost interface for any system to Ethernet.

Pin Configuration

DUAL-IN LINE
TOP VIEW



PLASTIC LEADED CHIP CARRIER
TOP VIEW



EDLC is a registered trademark of SEEQ Technology, Inc.
MCC is a trademark of SEEQ Technology, Inc.

Functional Description

The 8020 Manchester Code Converter chip has two portions, transmitter and receiver. The transmitter uses Manchester encoding to combine the clock and data into a serial stream. It also differentially drives up to 50 meters of twisted pair transmission line. The receiver detects the presence of data and collisions. The 8020 MCC™ recovers the Manchester encoded data stream and decodes it into clock and data outputs. Manchester Encoding is the process of combining the clock and data stream so that they may be transmitted on a single twisted pair of wires, and the clock and data may be recovered accurately upon reception. Manchester encoding has the unique property of a transition at the center of each bit cell, a positive going transition for a "1," and a negative going transition for a "0" (See Figure 2). The encoding is accomplished by exlusive-ORing the clock and data prior to transmission, and the decoding by deriving the clock from the data with a phase locked loop.

Clock Generator

The internal oscillator is controlled by a 20 MHz parallel resonant crystal or by an external clock on X1. The 20 MHz clock is then divided by 2 to generate a 10 MHz ±0.01% transmitter clock. Both 10 MHz and 20 MHz clocks are used in Manchester data encoding.

Manchester Encoder and Differential Output Driver

The encoder combines clock and data information for the transceiver. In Manchester encoding, the first half of the bit cell contains the complement of the data and the second half contains the true data. Thus, a transition is always guaranteed in the middle of a bit cell.

Data encoding and transmission begin with TxEN going active; the first transition is always positive for Tx(-) and negative for Tx(+). In IEEE mode, at the termination of a transmission, TxEN goes inactive and transmit pair approach to zero differential. In Ethernet mode, at the end of the transmission, TxEN goes inactive and the transmit pair stay differentially high. The transmit termination can occur at bit cell center if the last bit is a one or at a bit boundary if the last bit is a zero. To eliminate DC current in the transformer during idle, Tx± is brought to 100 mV differential in 600 ns after the last transition (IEEE mode). The back swing voltage is guaranteed to be less than .1 V.

Watchdog Timer

A watchdog timer is built on chip. It can be enabled or disabled by the $\overline{\text{LPBK}}$/WDTD signal. The timer starts counting at the beginning of the transmission. If TxEN goes inactive before the timer expires, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted by disabling the differential transmitter. This is done by idling the differential output drivers (differential output voltage becomes zero) and deasserting CSN.

Differential Input Circuit (Rx+ and Rx−, COLL+ and COLL−).

As shown in Figure 3, the differential input for Rx+ and Rx- and COLL+ and COLL- are externally terminated by a pair of 39.2 Ω ± 1% resistors in series for proper impedance matching.

The center tap has a 0.01 µF capacitor, tied to ground, to provide the AC common mode impedance termination for the transceiver cable.

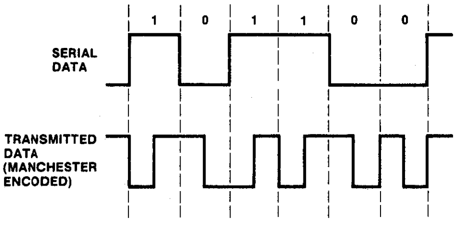


Figure 2. Manchester Coding

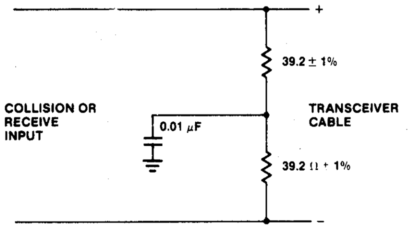


Figure 3. Differential Input Terminator

Both collision and receiver input circuits provide a static noise margin of -140 mV to -300 mV (peak value). Noise rejection filters are provided at both input pairs to prevent spurious signals. For the receiver pair, the range is 15 ns to 30 ns. For the collision pair, the range is 10 ns to 18 ns. The D.C. threshold and noise rejection filter assure that differential receiver data signals less than -140 mV in amplitude or narrower than 15 ns (10 ns for collision pair) are always rejected, signals greater than -300 mV and wider than 30 ns (18 ns for collision pair) are always accepted.

Manchester Decoder and Clock Recovery Circuit

The filtered data is processed by the data and clock recovery circuit using a phase-locked loop technique. The PLL is designed to lock onto the preamble of the incoming signal with a transition width asymmetry not greater than +8.25 ns to -8.25 ns within 12 bit cell times worst case and can sample the incoming data with a transition width asymmetry of up to +8.25 ns to -8.25 ns. The RxC high or low time will always be greater than 40 ns. RxC follows TxC for the first 1.2μs and then switches to the recovered clock. In addition, the Encoder/Decoder asserts the CSN signal while it is receiving data from the cable to indicate the receiver data and clock are valid and available. At the end of frame, after the node has finished transmitting, CSN is deasserted and will not be asserted again for a period of 4.5μs regardless of the state of the state of the receiver pair or collision pair. This is called the inhibit period. There is no inhibit period after packet reception. During clock switching, RxC may stay high for 200ns maximum.

Collision Circuit

A collision on the Ethernet cable is sensed by the transceiver. It generates a 10 MHz ±15% differential square wave to indicate the presence of the collision. During the collision period, CSN is asserted asynchronously with RxC. However, if a collision arrives during inhibit period 4.5 μs from the time CSN was deasserted, CSN will not be reasserted.

Loopback

In loopback mode, encoded data is switched to the PLL instead of Tx+/Tx- signals. The recovered data and clock are returned to the Ethernet Controller. All the transmit and receive circuits, including noise rejection filter, are tested except the differential output driver and the differential input receiver circuits which are disabled during loopback. At the end of frame transmission, the 8020 also generates a 650 ns long COLL signal 550 ns after CSN was deasserted to simulate the IEEE 802.3 SQE test. The watchdog timer remains enabled in this mode.

Pin Description

The MCC™ chip signals are grouped into four categories:

- Power Supply and Clock
- Controller Interface
- Transceiver Interface
- Miscellaneous

Power Supply

V_{CC}	+5V
V_{SS}	Ground

X1 and X2 Clock (Inputs): Clock Crystal: 20 MHz crystal oscillator input. Alternately, pin X1 may be used as a TTL level input for external timing by floating pin X2.

Controller Interface

RxC Receive Clock (Output): This signal is the recovered clock from the phase decoder circuit. It is switched to $\overline{\text{TxC}}$ when no incoming data is present from which a true receive clock is derived. 10 MHz nominal and TTL compatible.

RxD Receive Data (Output): The RxD signal is the recovered data from the phase decoder. During idle periods, the RxD pin is LOW under normal conditions. TTL and MOS level compatible. Active HIGH.

CSN Carrier Sense (Output): The Carrier Sense Signal indicates to the controller that there is activity on the coaxial cable. It is asserted when receive data is present or when a collision signal is present. It is deasserted at the end of frame or at the end of collision, whichever occurs later. It is asserted or deasserted synchronously with RxC. TTL compatible.

$\overline{\text{TxC}}$ Transmit Clock (Output): A 10 MHz signal derived from the internal oscillator. This clock is always active. TTL and MOS level compatible.

TxD Transmit Data (Input): TxD is the NRZ serial input data to be transmitted. The data is clocked into the MCC by $\overline{\text{TxC}}$. Active HIGH, TTL compatible.

TxEN Transmit Enable (Input): Transmit Enable, when asserted, enables data to be sent to the cable. It is asserted synchronously with $\overline{\text{TxC}}$. TxEN goes active with the first bit of transmission. TTL compatible.

COLL Collision (Output): *When asserted, indicates to the controller the simultaneous transmission of two or more stations on network cable. TTL Compatible.*

Transceiver Interface

Rx+ and Rx− Differential Receiver Input Pair (Input): *Differential receiver input pair which brings the encoded receive data to the 8020. The last transition is always positive-going to indicate the end of the frame.*

COLL+ and COLL− Differential Collision Input Pair (Input): *This is a 10 MHz ±15% differential signal from the transceiver indicating collision. The duty cycle should not be worse than 60%/40% — 40%/60%. The last transition is positive-going. This signal will respond to signals in the range of 5 MHz to 11.5 MHz. Collision signal may be asserted if 'MAU not available' signal is present.*

Tx+ and Tx− Differential Transmit Output Pair (Output): *Differential transmit pair which sends the encoded data to the transceiver. The cable driver buffers are source follower and require external 243 Ω resistors to ground as loading. These resistors must be rated at 1 watt to withstand the fault conditions specified by IEEE 802.3. If MODE1 = 1, after 200 ns following the last transition, the differential voltage is slowly reduced to zero volts in 8 μs to limit the back swing of the coupling transformer to less than 0.1 V.*

Miscellaneous

MODE1 (Input): *This pin is used to select between AC or DC coupling. When it is tied high or left floating, the output drivers provide differential zero signal during idle (IEEE 802.3 specification). When pin 1 is tied low, then the output is differentially high when idle (Ethernet Rev. 1 specification).*

$\overline{\text{LPBK}}$/WDTD $\overline{\text{Loopback}}$/Watchdog Timer Disable (Input):

Normal Operation: *For normal operation this pin should be HIGH or tied to V_{CC}. In normal operation the watchdog timer is enabled.*

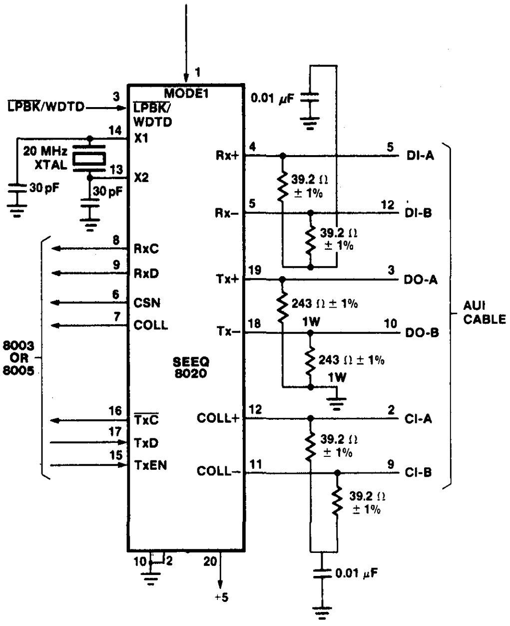


Figure 4. 8020 Interface

Loopback: *When this pin is brought low, the Manchester encoded transmit data from TxD and $\overline{\text{TxC}}$ is routed through the receiver circuit and sent back onto the RxD and RxC Pins. During loopback, Collision and Receive data inputs are ignored. The transmit pair is idled. At the end of transmission, the signal quality error test (SQET) will be simulated by asserting collision during the inhibit window. During loopback, the watchdog timer is enabled.*

Watchdog Timer Disable: *When this pin is between 10 V (Min.) and 16 V (Max.), the on chip 25 ms Watchdog Timer will be disabled. The watchdog timer is used to monitor the transmit enable pin. If TxEN is asserted for too long, then the watchdog timer (if enabled) will automatically deassert CSN and inhibit any further transmissions on the Tx+ and Tx− lines. The watchdog timer is automatically reset each time TxEN is deasserted.*

Interconnection to a Data Link Controller

Figure 5 shows the interconnections between the 8020 MCC™ and SEEQ's 8003 or 8005. There are three connections for each of the two transmission channels, transmit and receive, plus the Collision Signal line (COLL).

Transmitter connections are:

Transmit Data, TxD
Transmit Clock, $\overline{\text{TxC}}$
Transmit Enable, TxEN
Collision, COLL

Receiver connections are:

Receive Data, RxD
Receive Clock, RxC
Carrier Sense, CSN

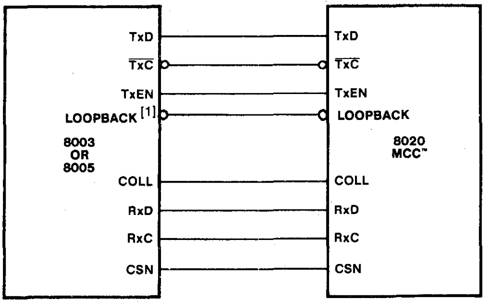


Figure 5. Interconnection of 8020 and 8003/8005

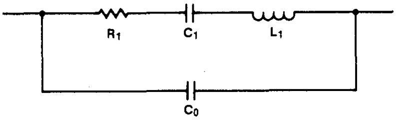
NOTE

1. Loopback output on 8005 only.

D.C. and A.C. Characteristics and Timing

Crystal Specification

Resonant Frequency (C_L = 20 pF)	*20 MHz ± 0.005% 0–70° C and ± 0.003% at 25° C*
Type	*Fundamental Mode*
Circuit	*Parallel Resonance*
Load Capacitance (C_L)	*20 pF*
Shunt Capacitance (C_O)	*7 pF Max.*
Equivalent Series Resistance (R1)	*25 Ω Max.*
Motional Capacitance (C1)	*0.02 pF Max.*
Drive Level	*2 mW*



EQUIVALENT CIRCUIT OF CRYSTAL

Figure 6.

*Absolute Maximum Ratings**

Storage Temperature	*−65° C to 150° C*
All Input and Output Voltage	*−0.3 to V_{CC}+0.3*
V_{CC}	*−0.3 to 7V*
(Rx±, Tx±, COLL±) High Voltage Short Circuit Immunity	*−0.3 to 16V*

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics T_A = 0°C to 70°C; V_{CC} = 5 V ± 5%

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{IL}	Input Leakage Current (except MODE1, Receive and Collision Pairs)		10	µA	$0 \le V_{IN} \le V_{CC}$
	MODE1 Input Leakage Current		200	µA	$0 \le V_{IN} \le V_{CC}$
	Receive and Collision Pairs (Rx±, COLL±) Input Leakage Current		2	mA	$V_{IN} = 0$
I_{CC}	V_{CC} Current		75	mA	All Inputs, Outputs Open
V_{IL}	TTL Input Low Voltage	−0.3	0.8	V	
V_{IH}	TTL Input High Voltage (except X1)	2.0	V_{CC}+0.3	V	
	X1 Input High Voltage	3.5	V_{CC}+0.3	V	
V_{OL}	TTL Output Low Voltage except TxC		0.4	V	I_{OL}=2.1 mA
	$\overline{\text{TxC}}$ Output Low Voltage		0.4	V	I_{OL}=4.2 mA
V_{OH}	TTL Output High Voltage (except RxC, $\overline{\text{TxC}}$, RxD)	2.4		V	t_{OH}=−400µA
	RxC, $\overline{\text{TxC}}$, RxD Output High Voltage	3.9		V	t_{OH}=−400µA
V_{ODF}	Differential Output Swing	±0.55	±1.2	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{OCM}	Common Mode Output Voltage	V_{CC} − 2.5	V_{CC} − 1	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{BKSV}	Tx± Backswing Voltage During Idle		0.1	V	Shunt inductive load≤27 µH
V_{IDF}	Input Differential Voltage (measured differentially)	±0.3	±1.2	V	
V_{ICM}	Input Commnon Mode Voltage	0	V_{CC}	V	
C_{IN}[1]	Input Capacitance		15	pF	
C_{OUT}[1]	Output Capacitance		15	pF	

NOTE:

1. Characterized. Not tested.

A.C. Test Conditions

Output Loading TTL Output:	*1 TTL gate and 20 pF capacitor*
Differential Output:	*243Ω resistor and 10 pF capacitor from each pin to V_{SS} and a termination 78Ω resistor load resistor in parallel with a 27 μH inductor between the two differential output pins*
Differential Signal Delay Time Reference Level:	*50% point of swing*
Differential Output Rise and Fall Time:	*20% to 80% points*
RxC, $\overline{\text{TxC}}$, X1 High and Low Time:	*High time measured at 3.0V* *Low time measured at 0.6V*
RxD, RxC, $\overline{\text{TxC}}$, X1 Rise and Fall Time:	*Measured between 0.6V and 3.0V points*
TTL Input Voltage (except X1):	*0.8V to 2.0V with 10 ns rise and fall time*
X1 Input Voltage:	*0.8V to 3.5V with 5 ns rise and fall time*
Differential Input Voltage:	*At least ± 300 mV with rise and fall time of 10 ns measured between −0.2V and +0.2V*

20 MHz TTL Clock Input Timing $T_A = 0°C$ to $70°C$; $V_{CC} = 5\ V \pm 5\%$

Symbol	Parameter	Min.	Max.	Units
t_1	X1 Cycle Time	49.995	50.005	ns
t_2	X1 High Time	15		ns
t_3	X1 Low Time	15		ns
t_4	X1 Rise Time		5	ns
t_5	X1 Fall Time		5	ns
t_{5A}	X1 to $\overline{\text{TxC}}$ Delay Time	10	45	ns

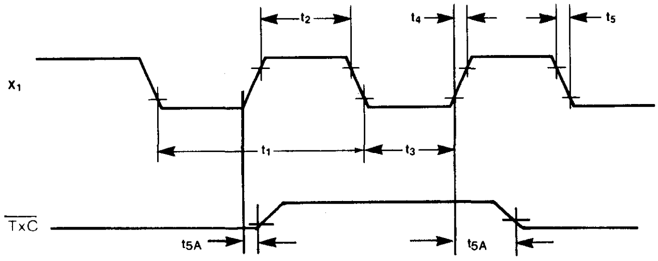


Figure 12. 20 MHz TTL Clock Timing

Transmit Timing $T_A = 0°C$ to $70°C$; $V_{CC} = 5\ V \pm 5\%$

Symbol	Parameter	Min.	Max.	Units
t_6[1]	$\overline{\text{TxC}}$ Cycle Time	99.99	100.01	ns
t_7	$\overline{\text{TxC}}$ High Time	40		ns
t_8	$\overline{\text{TxC}}$ Low Time	40		ns
t_9[1]	$\overline{\text{TxC}}$ Rise Time		5	ns
t_{10}[1]	$\overline{\text{TxC}}$ Fall Time		5	ns
t_{11}	TxEN Setup Time	40		ns
t_{12}	TxD Setup Time	40		ns
t_{13}[1]	Bit Center to Bit Center Time	99.5	100.5	ns
t_{14}[1]	Bit Center to Bit Boundary Time	49.5	50.5	ns
t_{15}[1]	Tx+ and Tx− Rise Time		5	ns
t_{16}[1]	Tx+ and Tx− Fall Time		5	ns
t_{17}	Transmit Active Time From The Last Positive Transition	200		ns
t_{17A}[1]	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 100 mV of 0 V	400	600	ns
t_{17B}[1]	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 40 mV of 0 V		7000	ns
t_{18}	Tx+ and Tx− Output Delay Time		70	ns
t_{19}	TxD Hold Time	15		ns
t_{20}	TxEN Hold Time	15		ns

NOTE:

1. Characterized. Not tested.

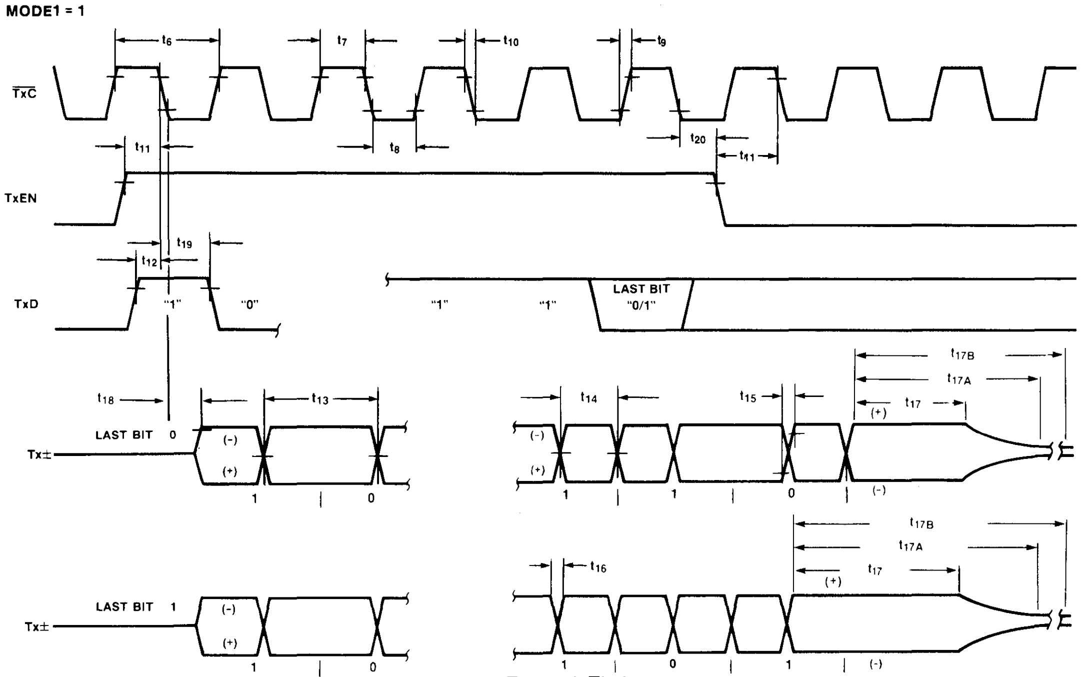


Figure 7. Transmit Timing

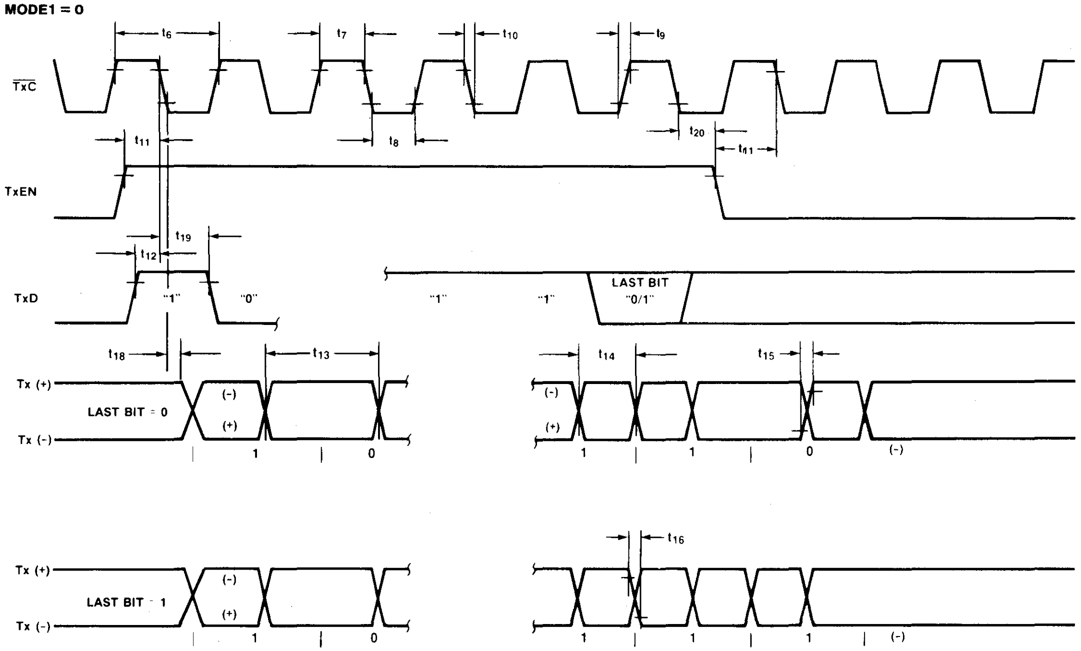


Figure 8. Transmit Timing

Receive Timing $T_A = 0°C$ to $70°C$; $V_{CC} = 5\ V \pm 5\%$

Symbol	Parameter	Min.	Max.	Units
t_{21}	CSN Assert Delay Time		240	ns
t_{22}	CSN Deasserts Delay Time (measured from Last Bit Boundary)		240	ns
t_{23A}	CSN Hold Time	30		ns
t_{23B}	CSN Set up Time	30		ns
t_{24}	RxD Hold Time	30		ns
t_{25}	RxD Set up Time	30		ns
t_{26}[1]	RxC Rise and Fall Time		5	ns
t_{27}[1]	During Clock Switch RxC Keeps High Time	40	200	ns
t_{28}	RxC High and Low Time	40		ns
t_{29}[1]	RxC Clock Cycle Time (during) data period)	95	105	ns
t_{30}	CSN Inhibit Time (on Transmission Node only)	4.3	4.6	µs
t_{31}	Rx+/Rx− Rise and Fall Time		10	ns
t_{32}[1]	Rx+/Rx− Begin Return to Zero from Last Positive-Going Transition	160		ns
t_{33}[1]	RxD Rise Time		10	ns
t_{34}[1]	RxD Fall Time		10	ns

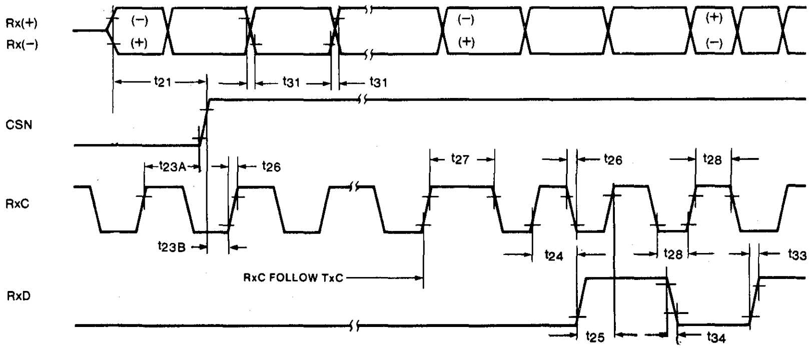


Figure 9. Receive Timing-Start of Packet

NOTE:
1. Characterized. Not tested.

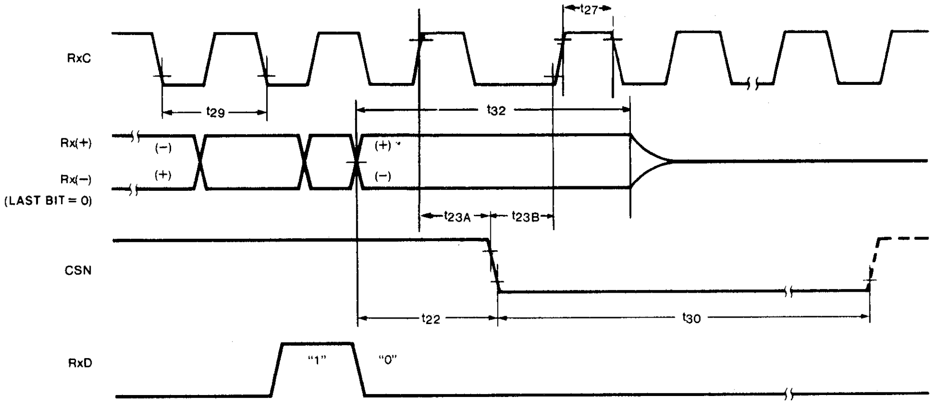


Figure 10. Receive Timing – End of Packet

Collision Timing $T_A = 0°C$ to $70°C$; $V_{CC} = 5\ V \pm 5\%$

Symbol	Parameter	Min.	Max.	Units
t_{51}	COLL+/COLL— Cycle Time	86	118	ns
t_{52}	COLL+/COLL— Rise and Fall Time		10	ns
t_{53}	COLL+/COLL— High and Low Time	35	70	ns
t_{54}	COLL+/COLL— Width (measured at −0.3V)	26		ns
t_{55}	COLL Asserts Delay Time		300	ns
t_{56}	COLL Deasserts Delay Time		500	ns
t_{57}	CSN Asserts Delay Time		400	ns
t_{58}	CSN Deasserts Delay Time		600	ns

Notes:

1. COLL+ and COLL- asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
2. If COLL+ and COLL- arrives within 4.5μs from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
3. When COLL+ and COLL- terminates, CSN will not be deasserted if Rx+ and Rx- are still active.
4. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for 4.5 μs.

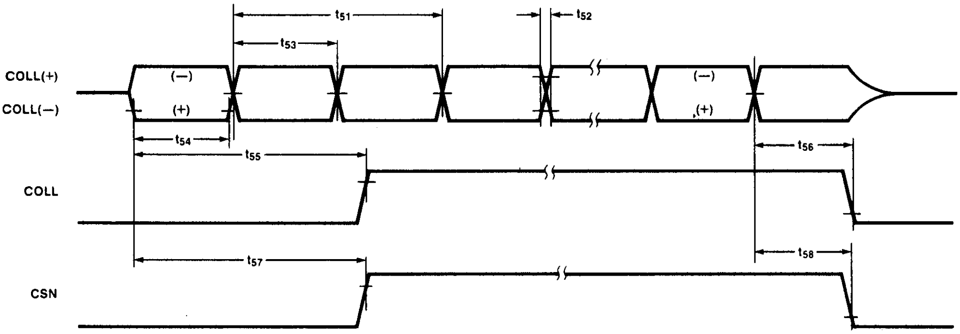


Figure 11. Collision Timing

Loopback Timing $T_A = 0°C$ to $70°C$; $V_{CC} = 5\ V \pm 5\%$

Symbol	Parameter	Min.	Max.	Units
t_{61}	LPBK Setup Time	500		ns
t_{62}	LPBK Hold Time	5		μs
t_{63}	In Collision Simulation, COLL Signal Delay Time	475	625	ns
t_{64}	COLL Duration Time	600	750	ns

Note:

1. PLL needs 12-bit cell times to acquire lock, RxD is invalid during this period.

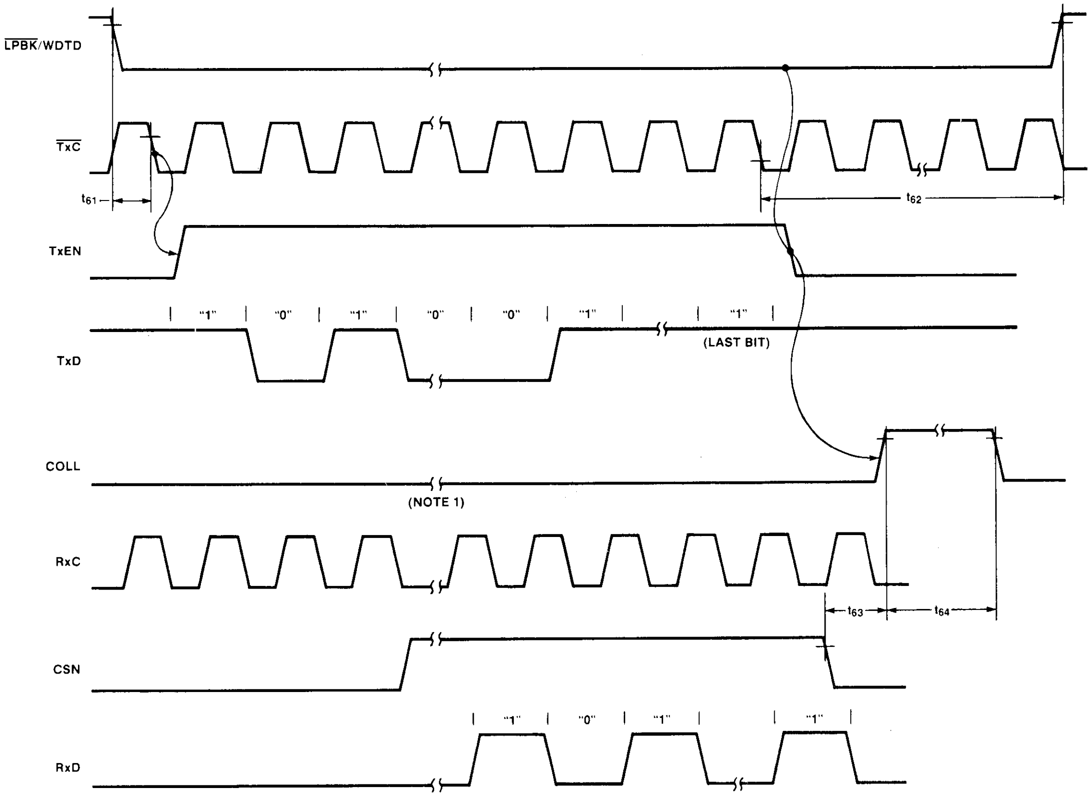
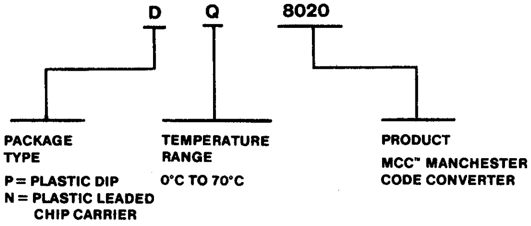


Figure 13. Loopback Timing

Ordering Information



seeq

8023A

MCC™ Manchester Code Converter

October 1988

Features

- **Compatible with IEEE 802.3/Ethernet (10BASE5), IEEE802.3/CHEAPERNET (10BASE2) and Ethernet Rev. 1 Specifications**
- **Compatible with the 8003 EDLC,® 8005 Advanced EDLC and Intel 82586 LAN Controller**
- **Manchester Data Encoding/Decoding and Receiver Clock Recovery with Phase Locked Loop (PLL)**
- **Receiver and Collision Squelch Circuit and Noise Rejection Filter**
- **Differential TRANSMIT Cable Driver**
- **Loopback Capability for Diagnostics and Isolation**
- **Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission**
- **20 MHz Crystal Oscillator**
- **Transceiver Interface High Voltage (16 V) Short Circuit Protection**
- **Low Power CMOS Technology with Single 5V Supply**
- **20 pin DIP & PLCC Packages**

Description

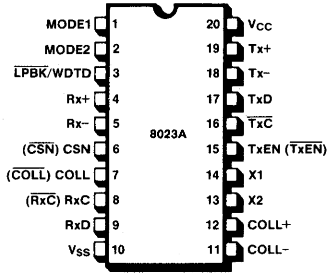
The SEEQ 8023A Manchester Code Converter chip provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the SEEQ 8003 and 8005 Ethernet Data Link Controllers or to the Intel 82586 LAN Controller and any standard Ethernet transceiver as defined by IEEE 802.3 and Ethernet Revision 1.

The SEEQ 8023A MCC is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the 8023A includes a 25 millisecond watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

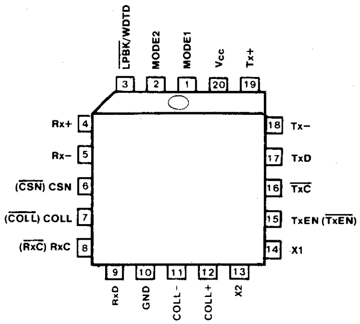
Together with the 8003 or 8005 and a transceiver, the 8023A Manchester Code Converter provides a high performance minimum cost interface for any system to Ethernet.

Pin Configuration

DUAL-IN-LINE
TOP VIEW



PLASTIC LEADED CHIP CARRIER
TOP VIEW



Functional Block Diagram

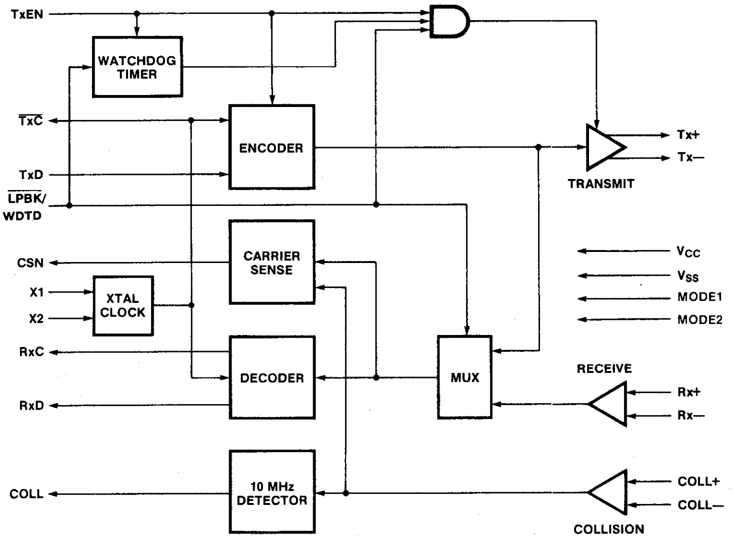


Figure 1. 8023A MCC Manchester Code Converter Block Diagram.

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MCC is a trademark of SEEQ Technology, Inc.

Functional Description

The 8023A Manchester Code Converter chip has two portions, transmitter and receiver. The transmitter uses Manchester encoding to combine the clock and data into a serial stream. It also differentially drives up to 50 meters of twisted pair transmission line. The receiver detects the presence of data and collisions. The 8023A MCC recovers the Manchester encoded data stream and decodes it into clock and data outputs. Manchester Encoding is the process of combining the clock and data stream so that they may be transmitted on a single twisted pair of wires, and the clock and data may be recovered accurately upon reception. Manchester encoding has the unique property of a transition at the center of each bit cell, a positive going transition for a "1", and a negative going transition for a "0" (See Figure 2). The encoding is accomplished by exlusive-ORing the clock and data prior to transmission, and the decoding by deriving the clock from the data with a phase locked loop.

Clock Generator

The internal oscillator is controlled by a 20 MHz parallel resonant crystal or by an external clock on X1. The 20 MHz clock is then divided by 2 to generate a 10 MHz ±0.01% transmitter clock. Both 10 MHz and 20 MHz clocks are used in Manchester data encoding.

Manchester Encoder and Differential Output Driver

The encoder combines clock and data information for the transceiver. In Manchester encoding, the first half of the bit cell contains the complement of the data and the second half contains the true data. Thus, a transition is always guaranteed in the middle of a bit cell.

Data encoding and transmission begin with TxEN going active; the first transition is always positive for Tx(-) and negative for Tx(+). In IEEE mode, at the termination of a transmission, TxEN goes inactive and the transmit pair approach to zero differential. In Ethernet mode, at the end of the transmission, TxEN goes inactive and the transmit pair stay differentially high. The transmit termination can occur at bit cell center if the last bit is a one or at a bit boundary if the last bit is a zero. To eliminate DC current in the transformer during idle, Tx ± is brought to 100 mV differential in 600 ns after the last transition (IEEE mode). The back swing voltage is guaranteed to be less than .1 V.

Watchdog Timer

A 25 ms watchdog timer is built on chip. It can be enabled or disabled by the $\overline{\text{LPBK}}$/WDTD signal. The timer starts counting at the beginning of the transmission. If TxEN goes inactive before the timer expires, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted by disabling the differential transmitter. This is done by idling the differential output drivers (differential output voltage becomes zero) and deasserting CSN.

Differential Input Circuit (Rx+ and Rx−, COLL+ and COLL−)

As shown in Figure 3, the differential input for Rx+ and Rx- and COLL+ and COLL- are externally terminated by a pair of 39.2 Ω ± 1% resistors in series for proper impedance matching.

The center tap has a 0.01 μF capacitor, tied to ground, to provide the AC common mode impedance termination for the transceiver cable.

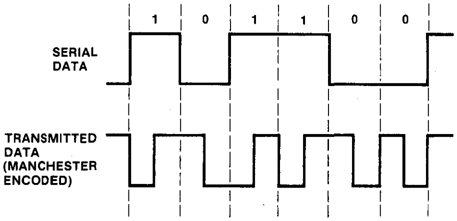


Figure 2. Manchester Coding

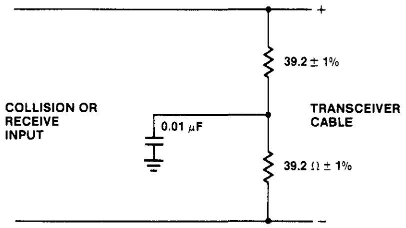


Figure 3. Differential Input Terminator

Both collision and receiver input circuits provide a static noise margin of -140 mV to -300 mV (peak value). Noise rejection filters are provided at both input pairs to prevent spurious signals. For the receiver pair, the range is 15 ns to 30 ns. For the collision pair, the range is 10 ns to 18 ns. The D.C. threshold and noise rejection filter assure that differential receiver data signals less than -140 mV in amplitude or narrower than 15 ns (10 ns for collision pair) are always rejected, signals greater than -300 mV and wider than 30 ns (18 ns for collision pair) are always accepted.

Manchester Decoder and Clock Recovery Circuit

The filtered data is processed by the data and clock recovery circuit using a phase-locked loop technique. The PLL is designed to lock onto the preamble of the incoming signal with a transition width asymmetry not greater than +8.25 ns to -8.25 ns within 12 bit cell times worst case and can sample the incoming data with a transition width asymmetry of up to +8.25 ns to -8.25 ns. The RxC high or low time will always be greater than 40 ns. If MODE 2 is high or floating, RxC will be held low for 1.2 us maximum while the PLL is acquiring lock. If MODE2 is low, RxC follows $\overline{\text{TxC}}$ for the first 1.2 µs and then switches to the recovered clock. In addition, the Encoder/Decoder asserts the CSN signal while it is receiving data from the cable to indicate the receiver data and clock are valid and available. At the end of frame, after the node has finished transmitting, CSN is deasserted and will not be asserted again for a period of 4.5 µs regardless of the state of the state of the receiver pair or collision pair. This is called the inhibit period. There is no inhibit period after packet reception. During clock switching, $\overline{\text{RxC}}$ may stay high for 200ns maximum.

Collision Circuit

A collision on the Ethernet cable is sensed by the transceiver. It generates a 10 MHz ±15% differential square wave to indicate the presence of the collision. During the collision period, CSN is asserted asynchronously with RxC. However, if a collision arrives during inhibit period 4.5 µs from the time CSN was deasserted, CSN will not be reasserted.

Loopback

In loopback mode, encoded data is switched to the PLL instead of Tx+/Tx- signals. The recovered data and clock are returned to the Ethernet Controller. All the transmit and receive circuits, including noise rejection filter, are tested except the differential output driver and the differential input receiver circuits which are disabled during loopback. At the end of frame transmission, the 8023A also generates a 650 ns long COLL signal 550 ns after CSN was deasserted to simulate the IEEE 802.3 SQE test. The watchdog timer remains enabled in this mode.

Pin Description

The MCC chip signals are grouped into four categories:

- Power Supply and Clock
- Controller Interface
- Transceiver Interface
- Miscellaneous

Power Supply

V_{CC}	+5V
V_{SS}	Ground

X1 and X2 Clock (Inputs): Clock Crystal: 20 MHz crystal oscillator input. Alternately, pin X1 may be used as a TTL level input for external timing by floating pin X2.

Controller Interface

RxC ($\overline{\text{RxC}}$) Receive Clock (Output): This signal is the recovered clock from the phase decoder circuit. It is switched to $\overline{\text{TxC}}$ when no incoming data is present from which a true receive clock is derived. 10 MHz nominal and TTL compatible. If the MODE2 signal is high, RxC is inverted ($\overline{\text{RxC}}$) and there is a 1.25 µsec discontinuity at the beginning of frame reception.

RxD Receive Data (Output): The RxD signal is the recovered data from the phase decoder. During idle periods, the RxD pin is LOW under normal conditions. However, if the MODE2 signal is HIGH, the RxD output will be HIGH during idle. TTL and MOS level compatible. Active HIGH.

CSN ($\overline{\text{CSN}}$) Carrier Sense (Output): The Carrier Sense Signal indicates to the controller that there is activity on the coaxial cable. It is asserted when receive data is present or when a collision signal is present. It is deasserted at the end of frame or at the end of collision, whichever occurs later. It is asserted or deasserted synchronously with RxC. TTL compatible. Normally active HIGH, unless MODE2 is HIGH, in which case $\overline{\text{CSN}}$ is active LOW.

$\overline{\text{TxC}}$ Transmit Clock (Output): A 10 MHz signal derived from the internal oscillator. This clock is always active. TTL and MOS level compatible.

TxD Transmit Data (Input): TxD is the NRZ serial input data to be transmitted. The data is clocked into the MCC by $\overline{\text{TxC}}$. Active HIGH, TTL compatible.

TxEN ($\overline{\text{TxEN}}$) Transmit Enable (Input): *Transmit Enable, when asserted, enables data to be sent to the cable. It is asserted synchronously with $\overline{\text{TxC}}$. TxEN goes active with the first bit of transmission. TTL compatible. If MODE2 is HIGH, TxEN is inverted.*

COLL ($\overline{\text{COLL}}$) Collision (Output): *When asserted, indicates to the controller the simultaneous transmission of two or more stations on network cable. TTL compatible. If MODE2 is HIGH, COLL is inverted.*

Transceiver Interface

Rx+ and Rx− Differential Receiver Input Pair (Input): *Differential receiver input pair which brings the encoded receive data to the 8023A. The last transition is always positive-going to indicate the end of the frame.*

COLL+ and COLL− Differential Collision Input Pair (Input): *This is a 10 MHz ±15% differential signal from the transceiver indicating collision. The duty cycle should not be worse than 60%/40% — 40%/60%. The last transition is positive-going. This signal will respond to signals in the range of 5 MHz to 11.5 MHz. Collision signal may be asserted if 'MAU not available' signal is present.*

Tx+ and Tx− Differential Transmit Output Pair (Output): *Differential transmit pair which sends the encoded data to the transceiver. The cable driver buffers are source follower and require external 243 Ω resistors to ground as loading. These resistors must be rated at 1 watt to withstand the fault conditions specified by IEEE 802.3. If MODE1=1, after 200 ns following the last transition, the differential voltage is slowly reduced to zero volts in 8 µs to limit the back swing of the coupling transformer to less than 0.1 V.*

Miscellaneous

MODE1 (Input): *This pin is used to select between AC or DC coupling. When it is tied high or left floating, the output drivers provide differential zero signal during idle (IEEE 802.3 specification). When pin 1 is tied low, the output is differentially high when idle (Ethernet Rev. 1 specification).*

MODE2 (Input): *The MODE2 Input signal is normally active LOW. In this configuration, the 8023A operates in a mode compatible with the SEEQ 8003. An alternate mode of operation may be achieved by configuring the MODE signal active HIGH, or by allowing it to float HIGH with its internal pullup. In this configuration, RxC, TxEN, CSN and COLL become active LOW. In addition, RxD is HIGH during idle, and RxC has a 1.2 µs discontinuity during signal acquisition.*

$\overline{\text{LPBK}}$/WDTD $\overline{\text{Loopback/}}$Watchdog Timer Disable (Input):

Normal Operation: *For normal operation this pin should be HIGH or tied to V_{CC}. In normal operation the watchdog timer is enabled.*

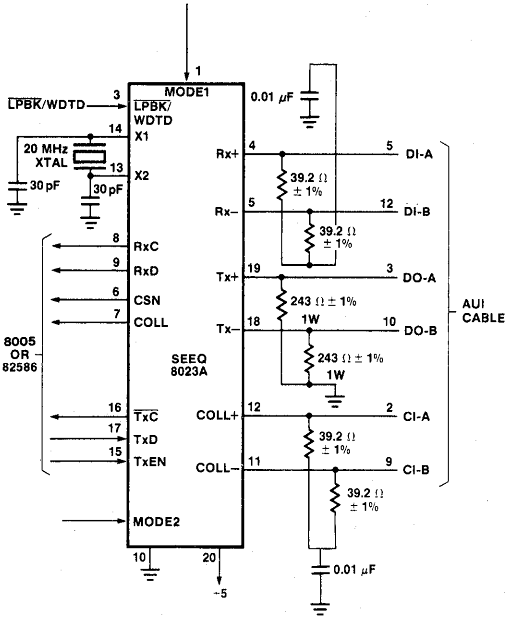


Figure 4. 8023A Interface

Loopback: When this pin is brought low, the Manchester encoded transmit data from TxD and $\overline{TxC}$ is routed through the receiver circuit and sent back onto the RxD and RxC Pins. During loopback, Collision and Receive data inputs are ignored. The transmit pair is idled. At the end of transmission, the signal quality error test (SQET) will be simulated by asserting collision during the inhibit window. During loopback, the watchdog timer is enabled.

Watchdog Timer Disable: When this pin is between 10 V (Min.) and 16 V (Max.), the on chip 25 ms Watchdog Timer will be disabled. The watchdog timer is used to monitor the transmit enable pin. If TxEN is asserted for longer than 25 ms, then the watchdog timer (if enabled) will automatically deassert CSN and inhibit any further transmissions on the Tx+ and Tx− lines. The watchdog timer is automatically reset each time TxEN is deasserted.

Interconnection to a Data Link Controller

Figure 5 shows the interconnections between the 8023A MCC and SEEQ's 8003 or 8005. There are three connections for each of the two transmission channels, transmit and receive, plus the Collision Signal line (COLL).

Transmitter connections are:

Transmit Data, TxD
Transmit Clock, $\overline{TxC}$
Transmit Enable, TxEN
Collision, COLL

Receiver connections are:

Receive Data, RxD
Receive Clock, RxC
Carrier Sense, CSN

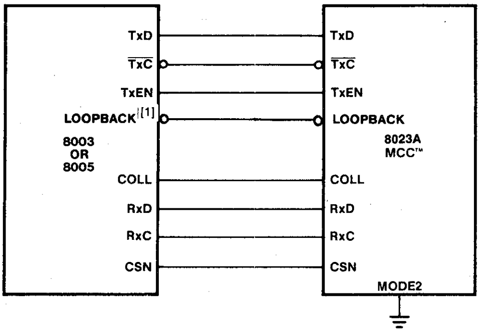


Figure 5. Interconnection of 8023A and 8003/8005

NOTE:
1. Loopback output on 8005 only.

Compatibility with Other LAN Controllers

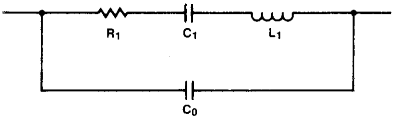
SEEQ's 8023A is compatible with other LAN Controllers, such as the 82586, when Pin 2 (MODE2) of the 8023A is floating or tied to V_{CC}. In this mode of operation, timing and polarity on the controller interface lines are compatible, with the 82586 specification dated March 1984.

Use of Time Domain Reflectometry in the 82586 is not recommended since the TDR transmission does not have a valid preamble.

D.C. and A.C. Characteristics and Timing

Crystal Specification

Resonant Frequency ($C_L = 20$ pF)	20 MHz ± 0.005% 0–70° C and ± 0.003% at 25° C
Type	Fundamental Mode
Circuit	Parallel Resonance
Load Capacitance (C_L)	20 pF
Shunt Capacitance (C_O)	7 pF Max.
Equivalent Series Resistance (R1)	25 Ω Max.
Motional Capacitance (C1)	0.02 pF Max.
Drive Level	2 mW



EQUIVALENT CIRCUIT OF CRYSTAL

Figure 6.

*Absolute Maximum Ratings**

Storage Temperature .... −65° C to 150° C
All Input and Output Voltage ..... −0.3 to V_{CC} +0.3
V_{CC} .... −0.3 to 7V
(Rx±, Tx±, COLL±) High Voltage
Short Circuit Immunity .... −0.3 to 16V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics T_A=0°C to 70°C; V_{CC}=5 V ± 10%

Symbol	Parameter	Min.	Max.	Unit	Conditions
I_{IL}	Input Leakage Current (except MODE1, MODE2 Receive and Collision Pairs)		10	µA	$0 \leq V_{IN} \leq V_{CC}$
	MODE1 Input Leakage Current		200	µA	$0 \leq V_{IN} \leq V_{CC}$
	Receive and Collision Pairs (Rx±, COLL±) Input Leakage Current		2	mA	$V_{IN} = 0$
I_{CC}	V_{CC} Current		75	mA	All Inputs, Outputs Open
V_{IL}	TTL Input Low Voltage	−0.3	0.8	V	
V_{IH}	TTL Input High Voltage (except X1)	2.0	V_{CC}+0.3	V	
	X1 Input High Voltage	3.5	V_{CC}+0.3	V	
V_{OL}	TTL Output Low Voltage except $\overline{\text{TxC}}$		0.4	V	I_{OL}=2.1 mA
	$\overline{\text{TxC}}$ Output Low Voltage		0.4	V	I_{OL}=4.2 mA
V_{OH}	TTL Output High Voltage (except RxC, $\overline{\text{TxC}}$, RxD)	2.4		V	t_{OH}=−400µA
	RxC, $\overline{\text{TxC}}$, RxD Output High Voltage	3.9		V	t_{OH}=−400µA
V_{ODF}	Differential Output Swing	±0.55	±1.2	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{OCM}	Common Mode Output Voltage	V_{CC} − 2.5	V_{CC} − 1	V	78Ω Termination Resistor and 243Ω Load Resistors
V_{BKSV}	Tx±Backswing Voltage During Idle		0.1	V	Shunt inductive load≤27 µH
V_{IDF}	Input Differential Voltage (measured differentially)	±0.3	±1.2	V	
V_{ICM}	Input Commnon Mode Voltage	0	V_{CC}	V	
C_{IN}[1]	Input Capacitance		15	pF	
C_{OUT}[1]	Output Capacitance		15	pF	

NOTE:
1. Characterized. Not tested.

A.C. Test Conditions

Output Loading TTL Output:	*1 TTL gate and 20 pF capacitor*
Differential Output:	*243Ω resistor and 10 pF capacitor from each pin to V_{SS} and a termination 78Ω resistor load resistor in parallel with a 27 µH inductor between the two differential output pins*
Differential Signal Delay Time Reference Level:	*50% point of swing*
Differential Output Rise and Fall Time:	*20% to 80% points*
RxC, $\overline{TxC}$, X1 High and Low Time:	*High time measured at 3.0V* *Low time measured at 0.6V*
RxD, RxC, $\overline{TxC}$, X1 Rise and Fall Time:	*Measured between 0.6V and 3.0V points*
TTL Input Voltage (except X1):	*0.8V to 2.0V with 10 ns rise and fall time*
X1 Input Voltage:	*0.8V to 3.5V with 5 ns rise and fall time*
Differential Input Voltage:	*At least ± 300 mV with rise and fall time of 10 ns measured between −0.2V and +0.2V*

20 MHz TTL Clock Input Timing T_A=0°C to 70°C; V_{CC}=5 V ± 10%

Symbol	Parameter	Min.	Max.	Units
t_1	X1 Cycle Time	49.995	50.005	ns
t_2	X1 High Time	15		ns
t_3	X1 Low Time	15		ns
t_4	X1 Rise Time		5	ns
t_5	X1 Fall Time		5	ns
t_{5A}	X1 to $\overline{TxC}$ Delay Time	10	45	ns

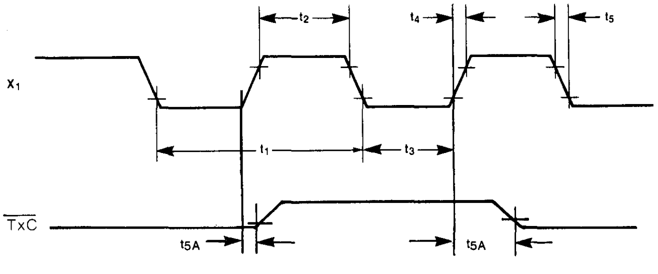


Figure 12.20 MHz TTL Clock Timing

Transmit Timing T_A=0°C to 70°C; V_{CC}=5 V ± 10%

Symbol	Parameter	Min.	Max.	Units
t_6[1]	$\overline{\text{TxC}}$ Cycle Time	99.99	100.01	ns
t_7	$\overline{\text{TxC}}$ High Time	40		ns
t_8	$\overline{\text{TxC}}$ Low Time	40		ns
t_9[1]	$\overline{\text{TxC}}$ Rise Time		5	ns
t_{10}[1]	$\overline{\text{TxC}}$ Fall Time		5	ns
t_{11}	TxEN Setup Time if Mode2=0 TxEN Setup Time if Mode2=1	40 55		ns ns
t_{12}	TxD Setup Time if Mode2=0 TxD Setup Time if Mode2=1	40 55		ns ns
t_{13}[1]	Bit Center to Bit Center Time	99.5	100.5	ns
t_{14}[1]	Bit Center to Bit Boundary Time	49.5	50.5	ns
t_{15}[1]	Tx+ and Tx− Rise Time		5	ns
t_{16}[1]	Tx+ and Tx− Fall Time		5	ns
t_{17}	Transmit Active Time From The Last Positive Transition	200		ns
t_{17A}[1]	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 100 mV of 0 V	400	600	ns
t_{17B}[1]	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 40 mV of 0 V		7000	ns
t_{18}	Tx+ and Tx− Output Delay Time		70	ns
t_{19}	TxD Hold Time if Mode2=0 TxD Hold Time if Mode2=1	15 0		ns ns
t_{20}	TxEN Hold Time if Mode2=0 TxEN Hold Time if Mode2=1	15 0		ns ns

NOTE:

1. Characterized. Not tested.

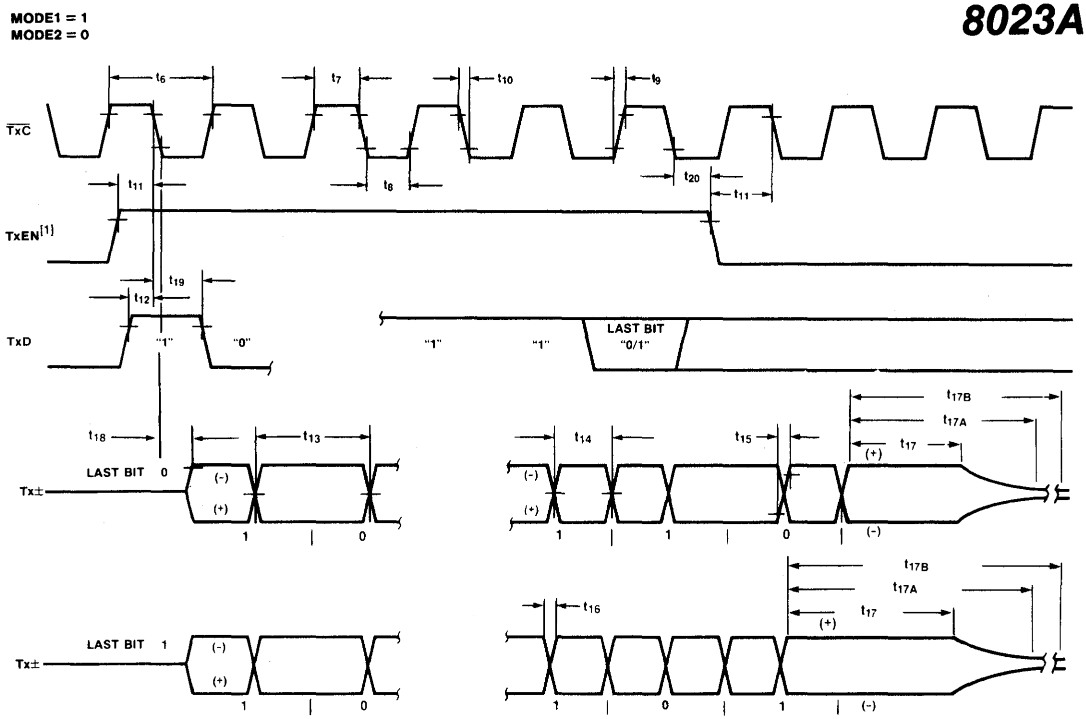


Figure 7. Transmit Timing

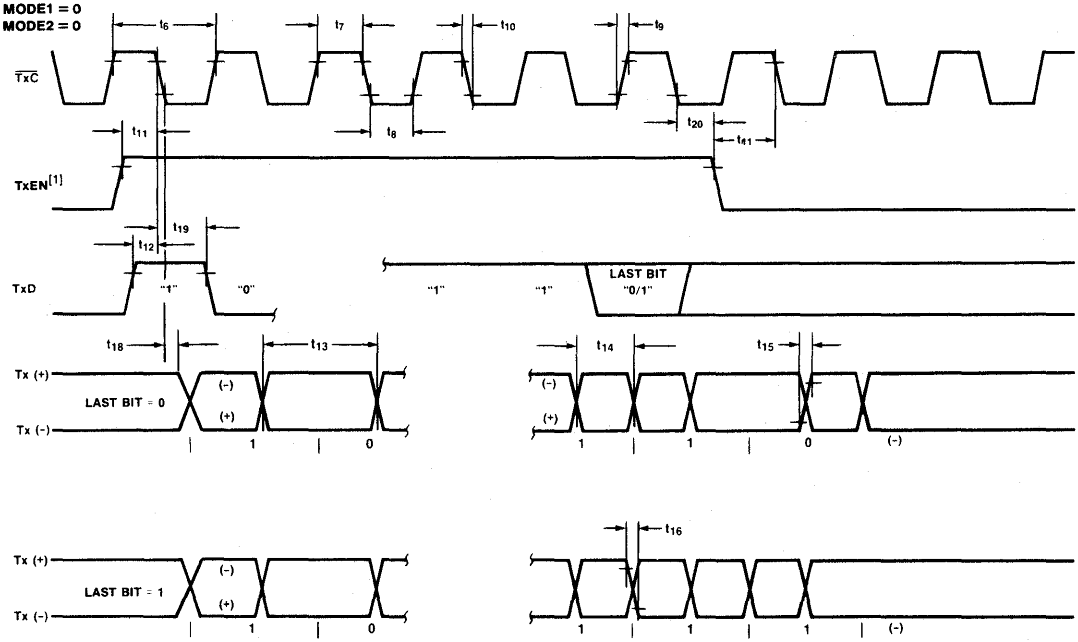
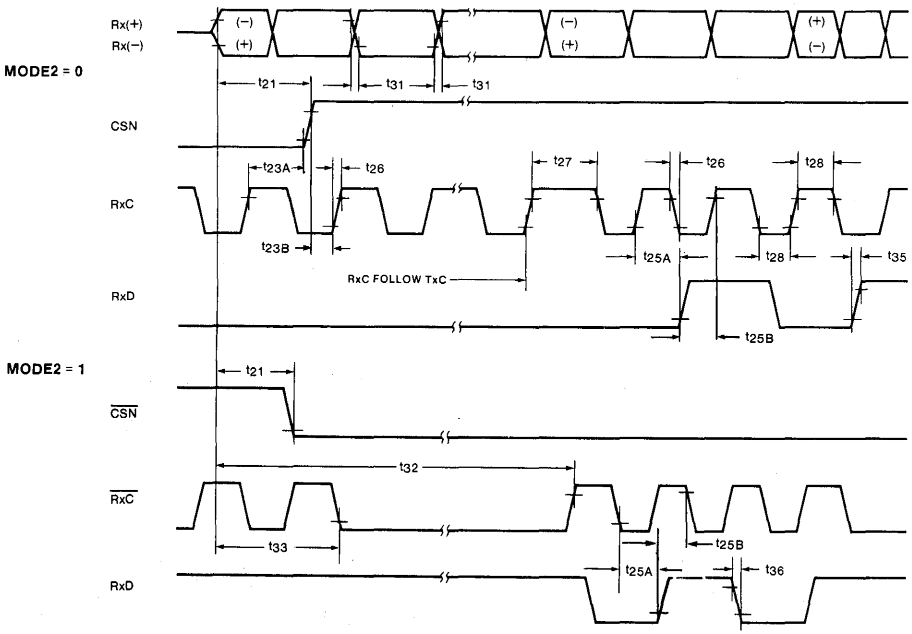


Figure 8. Transmit Timing

NOTE:
1. If MODE2= 1, TxEN becomes active low signal $\overline{\text{TxEN}}$.

Receive Timing T_A=0°C to 70°C; V_{CC}=5 V ± 10%

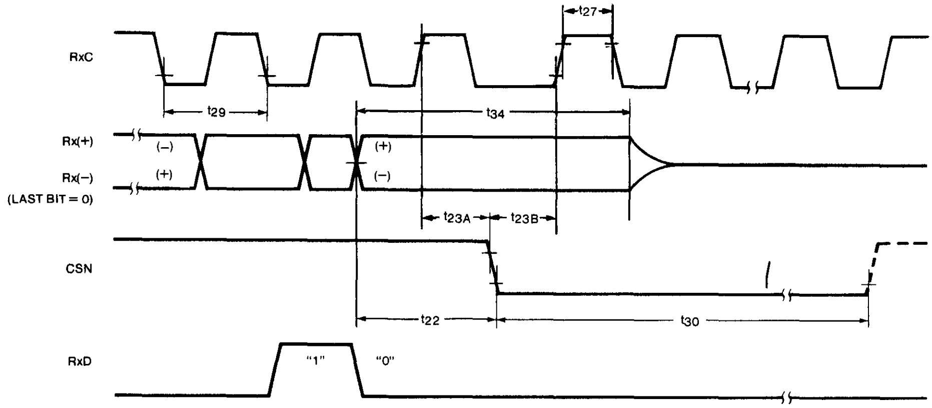
Symbol	Parameter	Min.	Max.	Units
t_{21}	$\overline{\text{CSN}}$ Assert Delay Time		240	ns
t_{22}	$\overline{\text{CSN}}$ Deasserts Delay Time (measured from Last Bit Boundary)		240	ns
t_{23A}	$\overline{\text{CSN}}$ Hold Time	30		ns
t_{23B}	$\overline{\text{CSN}}$ Set up Time	30		ns
t_{24}	$\overline{\text{CSN}}$ Deassertion Delay Time	10	35	ns
t_{25A}	RxD Hold Time	30		ns
t_{25B}	RxD Set up Time	30		ns
t_{26}[1]	RxC, $\overline{\text{RxC}}$ Rise and Fall Time		5	ns
t_{27}[1]	During Clock Switch RxC Keeps High, $\overline{\text{RxC}}$ Keeps Low Time	40	200	ns
t_{28}	RxC, $\overline{\text{RxC}}$ High and Low Time	40		ns
t_{29}[1]	RxC, $\overline{\text{RxC}}$ Clock Cycle Time (during) data period)	95	105	ns
t_{30}	CSN Inhibit Time (on Transmission Node only)	4.3	4.6	μs
t_{31}	Rx+/Rx− Rise and Fall Time		10	ns
t_{32}[1]	$\overline{\text{RxC}}$ Held Low Duration from First Valid Negative-Going Transition	1.15	1.35	μs
t_{33}	$\overline{\text{RxC}}$ Stops Delay Time from First Valid Negative-Going Transition		240	ns
t_{34}[1]	Rx+/Rx− Begin Return to Zero from Last Positive-Going Transition	160		ns
t_{35}[1]	RxD Rise Time		10	ns
t_{36}[1]	RxD Fall Time		10	ns



NOTE:
1. Characterized. Not tested.

Figure 9. Receive Timing–Start of Packet

MODE2 = 0



MODE2 = 1

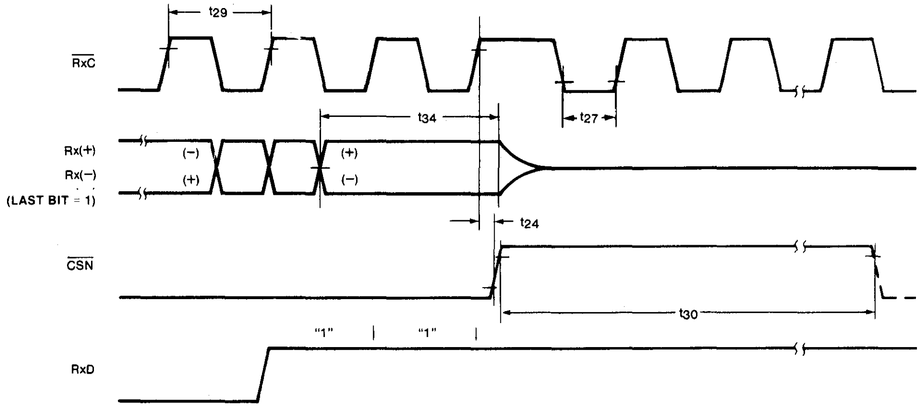


Figure 10. Receive Timing — End of Packet

Collision Timing T_A=0°C to 70°C; V_{CC}=5 V ± 10%

Symbol	Parameter	Min.	Max.	Units
t_{51}	COLL+/COLL— Cycle Time	86	118	ns
t_{52}	COLL+/COLL— Rise and Fall Time		10	ns
t_{53}	COLL+/COLL— High and Low Time	35	70	ns
t_{54}	COLL+/COLL— Width (measured at −0.3V)	26		ns
t_{55}	COLL Asserts Delay Time		300	ns
t_{56}	COLL Deasserts Delay Time		500	ns
t_{57}	CSN Asserts Delay Time		400	ns
t_{58}	CSN Deasserts Delay Time		600	ns

Notes:

1. COLL+ and COLL- asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
2. If COLL+ and COLL- arrives within 4.5μs from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
3. When COLL+ and COLL- terminates, CSN will not be deasserted if Rx+ and Rx- are still active.
4. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for 4.5 μs.
5. If MODE2 = 1, then COLL and CSN are inverted.

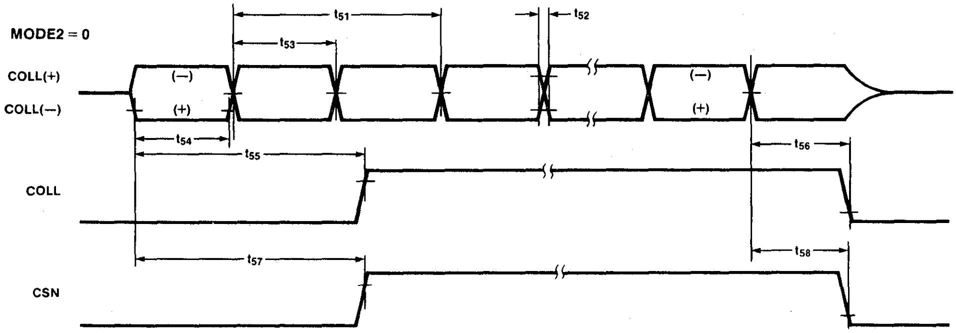


Figure 11. Collision Timing

Loopback Timing T_A=0°C to 70°C; V_{CC}=5 V ± 10%

Symbol	Parameter	Min.	Max.	Units
t_{61}	LPBK Setup Time	500		ns
t_{62}	LPBK Hold Time	5		μs
t_{63}	In Collision Simulation, COLL Signal Delay Time	475	625	ns
t_{64}	COLL Duration Time	600	750	ns

Note:

1. PLL needs 12-bit cell times to acquire lock, RxD is invalid during this period. RxC is low for 1.35 μs (max) if MODE2=1. RxD=0 if MODE2=0. RxD=1 if MODE2=1.

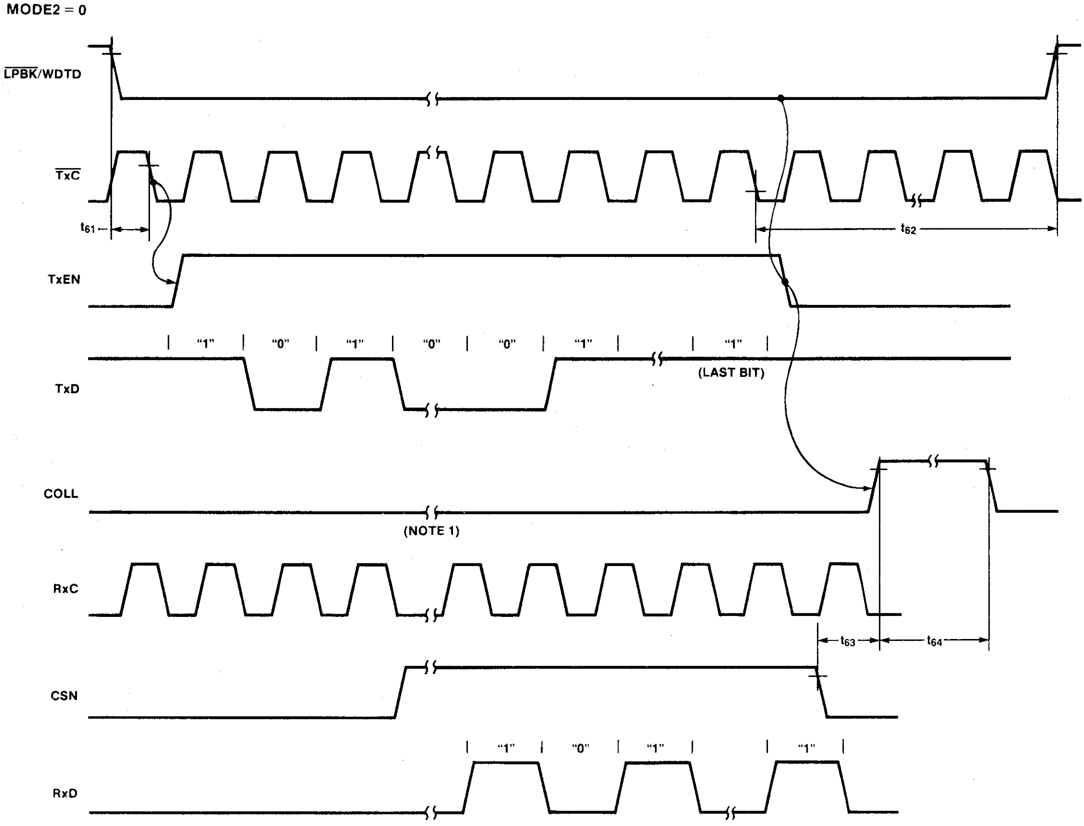


Figure 13. Loopback Timing

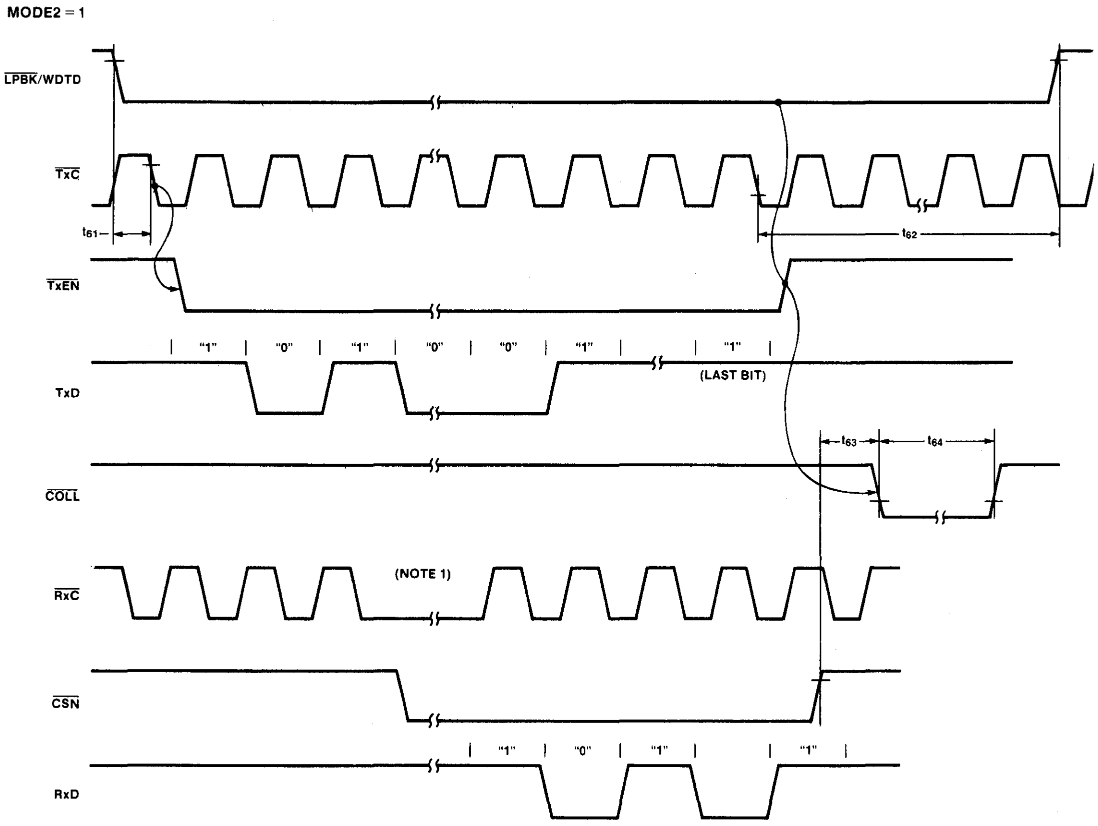
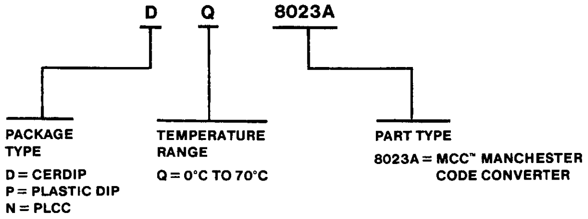


Figure 14. Loopback Timing — (Cont.)

Ordering Information



D Q 8023A

PACKAGE TYPE
D = CERDIP
P = PLASTIC DIP
N = PLCC

TEMPERATURE RANGE
Q = 0°C TO 70°C

PART TYPE
8023A = MCC™ MANCHESTER CODE CONVERTER

seeq

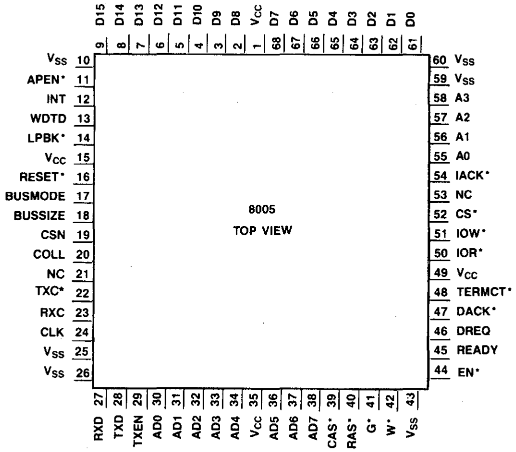
8005
Advanced Ethernet Data Link Controller

Preliminary

October 1988

Features

- ***Conforms to IEEE 802.3 Standard for Media Access Control (Ethernet and Cheapernet)***
- ***Recognizes One to Six Selectable Station Addresses***
- ***Software Selection of 2 Byte or 6 Byte Station Addresses***
- ***User Selectable Preamble and Frame Check Sequence Generation***
- ***Directly Supports 64K Bytes of Local Packet Buffer***
  - ***Connects to RAS/CAS/Data/Control of 64K x 4 Dynamic RAMS***
  - ***Automatic DRAM Refresh***
- ***Manages Local Receive/Transmit Packet Buffer by Buffer Chaining Technique***
  - ***Automatic Posting of Status in Buffer Header***
- ***Flexible System Bus Interface***
  - ***8 or 16 Bit Data Transfers with Byte Swap Capability***
  - ***Programmable DMA Burst Length***
  - ***Selectable for Intel or Motorola Compatible Bus Signals***
- ***Connects Directly to 8020 Manchester Code Converter***
- ***68 Pin Surface Mount Plastic Leaded Chip Carrier Package***



Pin Description

(An asterisk after a signal name signifies a low active signal)

D0-D15: *A 16 bit bidirectional system data bus. If BUSSIZE=0, the bus is configured as 8 bits and D8-D15 are not used for data transfer. D8-D15 are used to provide address information to the address PROM in both 8 and 16 bit modes. Byte order for local buffer data transfers on a 16 bit bus is software configured.*

EN*: *An output which can be used to control the tri-state control pin of external bi-directional drivers such as the 74LS245.*

APEN*: *Low active address PROM enable output.*

IOW*/R.W.*: *If busmode=1, this input defines the current bus cycle as a write. If busmode=0, this input defines the bus cycle as a read if a 1 or a write if a 0.*

IOR*: *If busmode=1, this input defines the current bus cycle as a read. If busmode=0, this input is not used.*

CS*: *The chip select input, used to access internal registers and the packet buffer.*

A0-A3: *Address select inputs used to select internal registers for reading or writing. A0 is not used in 16-bit mode.*

DACK*: *An input used to acknowledge granting of the system bus for external DMA transfers. When DREQ is active, DACK* functions as a chip select for reads and writes.*

DREQ/DREQ*: *An output to an external DMA controller used to signal that a DMA request is being made. This signal is high active when busmode=1, low active when busmode=0.*

TERMCT/TERMCT*: *An input which signals that the last byte or word of a DMA access is on the bus. When busmode=1, this input is high active; when busmode=0, it is low active.*

READY/DTACK*: *A tri-state output. When busmode=1, this output functions as a READY pin (Intel compatible); when busmode=0, this output is DTACK* (Motorola compatible).*

INT/INT*: *When busmode=1, this is a high active interrupt output; when busmode=0, this output is low active.*

IACK*: *Active low interrupt acknowledge input. When this input is active and INT is active the contents of the interrupt vector register are placed on D0-D7.*

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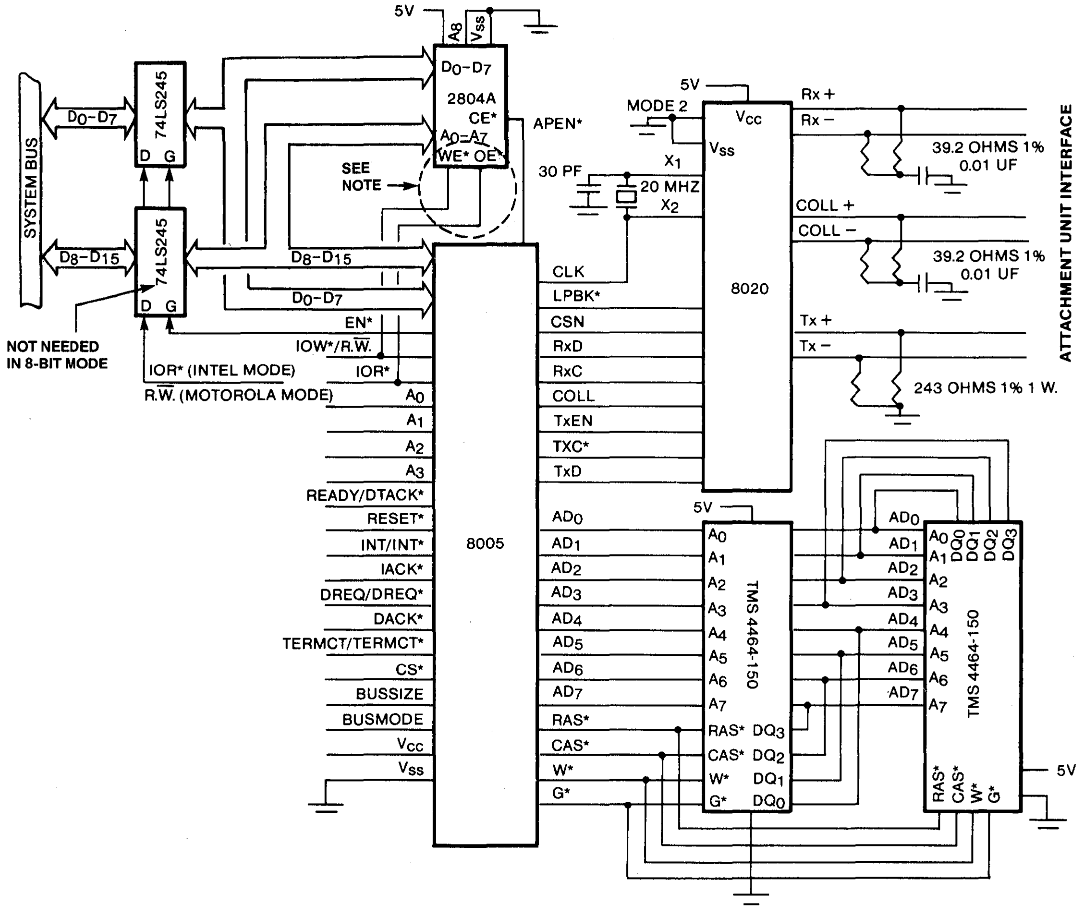
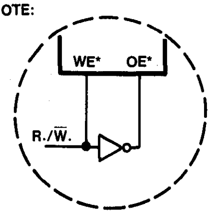


INTERCONNECT DIAGRAM

NOTE:



MOTOROLA MODE

RESET*: The low active reset input. Asserting RESET* clears all configuration and pointer registers to 00. Following reset, a wait of 4 µs is necessary before accessing the part.

BUSMODE: An input which selects Intel-compatible bus signals when high or Motorola-compatible bus signals when low.

BUSSIZE: An input which selects 8 bit system bus when low or 16 bit system bus when high.

AD0-AD7: A multiplexed address and data bus used to provide row and column addresses and read/write data to the packet buffer dynamic RAM.

RAS*: Row address strobe to the packet buffer memory.

CAS*: Column address strobe to the packet buffer memory. Page mode addressing is used when possible to speed access to the buffer.

W*: An output to the dynamic RAM buffer that indicates the current cycle is a write.

G*: An output to the dynamic RAM buffer that enables read data onto the AD bus.

TXEN: An output to the Manchester Code Converter that indicates a transmission is in progress.

TXC*: An input from the Manchester Code Converter that is used to synchronize transmitted data.

TXD: The transmit data output to the Manchester Code Converter.

RXC: An input from the Manchester Code Converter used to synchronize received data.

RXD: The receive data input from the Manchester Code Converter.

COLL: The collision input from the Manchester Code Converter.

CSN: The carrier sense input from the Manchester Code Converter.

WDTD: The watchdog timer disable output.

LPBK*: The loopback control output.

CLK: The master 20 MHz input clock.

Block Description

Three major blocks comprise the 8005: the EDLC® (Ethernet Data Link Controller), PBC (Packet Buffer Controller) and BIU (Bus Interface Unit).

The EDLC supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, frame check sequence generation/stripping, transmission deferral, collision handling and address recognition of up to 6 station addresses as well as multicast/broadcast addresses. It also supplies loopback and watchdog timer disable outputs which can be controlled by software to provide local diagnostic support. For non-IEEE 802.3 applications such as serial backplane buses, support is also provided for 2 byte address recognition, reduced slot time and reduced preamble length.

The PBC provides management for a 64K byte local packet buffer consisting of two 64K x 4 dynamic RAMS. This block provides arbitration and control for four different memory ports: the EDLC transmitter, for network transmit packets; the EDLC receiver, for received frames; the BIU, for system data and control; and an internal DRAM refresh generator. To minimize pin count, dynamic RAM addresses and data are time multiplexed on a single 8 bit bus. A control line and an 8 bit address is also provided to permit reading or writing to a locally attached EEPROM or PROM. This permits configuring a P.C. board with its station address(es) and configuration data independent of the network layer software used.

The BIU interfaces to the system bus and provides access to internal configuration/status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called the DMA FIFO. This permits high speed data transfers to occur even when the PBC is busy servicing the EDLC transmitter or receiver or refreshing the DRAM. Both 8 and 16 bit transfers are supported, and byte ordering on a 16 bit bus is under software control. The 8005 supports both Intel-compatible and Motorola-compatible buses.

Buffer Management

The PBC manages a 64K byte packet buffer into which packets that are received are temporarily stored until the system either reads or disposes of them and packets placed there by the system are held for transmission over the link. The buffer is logically divided into separate receive and transmit areas of selectable size. The transmit area always originates at address 0. Each packet in the buffer is prefixed by a header of 4 bytes that contains command and status information and a 16 bit pointer to the start of the next packet in the buffer.

To transmit frames, the system loads one or more packets of data, complete with header information, into the transmit area of the buffer and commands the 8005 to begin transmission starting from the address contained in the transmit pointer register. When transmission is complete, the 8005 updates the status byte in the header and interrupts the system if so programmed. The transmit pointer automatically wraps to location 0 when the transmit end area is reached.

The PBC manages the buffer area as a circular buffer with automatic wraparound. As data is received from the EDLC it is stored in the buffer beginning at the location specified by the receive pointer register. The receive pointer will wrap from FF,FF to Transmit End Area Address + 1,00. For example, if TEA = 80 the receive pointer wraps to 81,00. If the receive pointer reaches Receive End Area Address + 1,00 an overflow has occurred.

The receiver is then turned off and an interrupt is issued. Restarting the receiver is accomplished by freeing up buffer space and turning the receiver back on.

Transmit Packet Format

Each packet to be transmitted consists of a four byte header and up to 65,532 bytes of data which are placed into the local buffer via the BIU. The header contains the following information in the indicated order:

1. *Most significant byte of the address of the next packet header.*
2. *Least significant byte of the address of the next packet header.*
3. *A transmit command byte.*
4. *A transmit status byte which should be initialized to zero by the system and will contain status for this packet when transmission is complete.*

Bytes 1 and 2, called the next packet pointer, point to the location immediately following the last byte of the packet, which is the first byte of the next packet header, if it exists. When in 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used.

Byte 3 is the transmit command byte. It contains information to guide the controller in processing the packet associated with this block.

BIT 0: Xmit Babble Int. Enable. *The 8005 will transmit frames as large as the transmit buffer can hold but will flag long frames in the transmit status byte and interrupt if this bit is set to a one. This condition is caused by an attempt to transmit a packet larger than the allowed 1514 bytes, excluding preamble and CRC.*

Bit 1: Xmit Collision Interrupt Enable. *When set to a one, a transmit interrupt will be generated if a collision occurs during a transmit attempt.*

Bit 2: 16 Collisions Enable. *When set to a one, a transmit interrupt will be generated if 16 collisions occur during a transmit attempt.*

Bit 3: Xmit Success Interrupt Enable. *When set to a one, a transmit interrupt will be generated if the transmission is successful, that is, fewer than 16 collisions occurred.*

Bit 4: *Not used.*

Bit 5: Header Only. *If this bit is cleared to a zero, the transmitter will process this header as a pointer only, with no data associated with it.*

Bit 6: Chain Continue/End. *If set to a one, there are more headers in the chain to be processed. If this bit is a zero, this header is the last one in the chain.*

Bit 7: Xmit/Receive. *If this bit is a one, the current header is for a packet to be transmitted. If this bit is a zero, the frame header will be processed as a header only, like the header only bit (bit 5).*

Byte 4 is the transmit status byte, which is written by the PBC upon conclusion of each frame transmission or retransmission attempt. It provides for reporting of both normal and error termination conditions of each transmission.

BIT 0: Xmit Babble. *If set to a one, transmit babble occurred during the transmission attempt. This is caused by an attempt to transmit a packet larger than the allowed 1514 bytes, excluding preamble and CRC.*

Bit 1: Xmit Collision. *If set to a one, a collision occurred during the transmission attempt.*

Bit 2: 16 Collisions. *If set to a one, 16 collisions occurred during the transmission attempt.*

Bit 3, 4, 5 and 6: *Reserved.*

Bit 7: Done. *If set to a one, the controller has completed all processing of the packet associated with this header (either the packet has been sent successfully or 16 collisions occurred) and there is now valid status in the status byte. The user may now reuse the buffer area.*

Receive Packet Format

Each packet received is preceded by a four byte header and is placed into the local buffer via the PBC. The header contains the following information in the indicated order:

1. *Most significant byte of the address of the next packed header.*
2. *Least significant byte of the address of the next packet header.*
3. *Header status byte.*
4. *Frame status byte.*

Bytes 1 and 2, called the next packet pointer, point to the first byte of the next receive packet header. The next packet header starts immediately after the end of the current packet. The packet length is equal to the difference between the starting addresses of the two packet headers minus 4. If the value of the next packet pointer is less than the current one, the pointer has wrapped around from the end of the buffer to the Receive Start Area (the Receive Start Area equals the Transmit End Area address + 1) and then to the *value of the next pointer. When in 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used.*

The third byte of the header contains header information associated with this packet.

Bits 0 through 4: *Not used.*

Bit 5: Header Only. *If this bit is cleared to a zero, there is no packet associated with this header. This enables the controller to specify the end of a chain without touching the status of a packet already received. All 4 bytes in a header-only packet will be 00.*

Bit 6: Chain Continue/End. *If this bit is set to a one, there are more headers in this chain to be processed. If this bit is a zero, this header is the last one in the chain and this header space will be used for the next packet that is received.*

Bit 7: Xmit/Receive. *This bit is always set to 0 by the controller to indicate a receive packet header.*

The fourth byte of the header, called the packet status byte, contains status information resulting from processing the packet associated with this block.

Bit 0: Oversize Packet. *If this bit is a one, the packet was larger than 1514 bytes.*

Bit 1: CRC Error. *If this bit is a one, a CRC error (frame check sequence error) occurred in this frame. CRC status is captured on byte boundaries, so that 7 or less dribble bits will not cause a CRC error.*

Bit 2: Dribble Error. *Frames are integral multiples of octets (bytes). If this bit is a one, the received frame did not end on an octet (byte) boundary. This is normally not a fatal error unless the CRC error bit is also set.*

Bit 3: Short Frame. *If this bit is a one, the frame contained less than 64 bytes including CRC. Short frames are properly received as long as they are at least 6 bytes long; frames with less than 6 bytes will only be received if the match mode bits in configuration register #1 specify promiscuous mode, multicast/broadcast is selected and the first bit of the destination address is a 1, or the 2-byte address mode has been selected.*

BIT 4, 5 and 6: *Not used.*

Bit 7: Done. *If this bit is a one, the controller has completed all processing of this frame and there are now valid pointers and status in this header. The user may now move this packet out of the local buffer, if desired, and reuse this buffer space.*

Registers

There are nine directly accessible 16 bit registers in the 8005, one of which is used as a "window" into indirectly accessed registers as well as the local buffer memory. Access is controlled by chip select, I/O read, I/O write and four address inputs, A0-A3. The following description assumes a 16 bit wide system interface; as such, the low order address input, A0, is shown as "X," a don't care. In 8 bit mode, input pin A0 selects bits 0 through 7 of the register when a zero, and bits 8 through 15 when a one. Note that the byte swap bit does not affect the byte order of these registers.

Command Register, A3-0=000X$_2$ (Write only)

Bit 0: DMA Interrupt Enable. *When set to a 1, completion of a DMA operation, as signaled by Terminal Count, will generate an interrupt.*

Bit 1: Rx Interrupt Enable. *When set to a 1, this bit enables interrupts whenever a packet becomes available in the packet buffer.*

Bit 2: Tx Interrupt Enable. *When set to a 1, this bit enables interrupts for completion of transmit operations. See the transmit header command byte description for conditions that can cause an interrupt.*

Bit 3: Buffer Window Interrupt Enable. *Setting this bit to a one enables interrupts for buffer window register reads from the packet buffer.*

Bit 4: DMA Interrupt Acknowledge. *Setting this bit to a one causes a pending DMA interrupt to be cleared.*

Bit 5: Rx Interrupt Acknowledge. *Settling this bit to a one causes a pending receive interrupt to be cleared.*

Bit 6: Tx Interrupt Acknowledge. *Setting this bit to a one causes a pending transmit interrupt to be cleared.*

Bit 7: Buffer Window Interrupt Acknowledge. *Setting this bit to a one causes a pending buffer window interrupt to be cleared.*

Bit 8: Set DMA On. *Setting this bit to a one enables the DMA request logic. If the DMA FIFO is set to the read direction, a DMA request will be asserted when the DMA FIFO has enough bytes to satisfy the burst size. If the DMA FIFO is in the write direction the DMA request will be asserted immediately. Clearing this bit has no effect. Setting this bit with bit 11 set will force a DMA interrupt, provided the DMA interrupt enable bit is set, which permits testing the interrupt without actually performing DMA operations.*

Bit 9: Set Rx On. *Setting this bit to a one enables the EDLC receiver. Clearing this bit to a 0 has no effect. Setting this bit with bit 12 set will force an interrupt, provided the receive interrupt enable bit is set, which permits testing the interrupt without receiving packet data.*

Bit 10: Set Tx On. *Setting this bit to a 1 enables the EDLC transmitter. The PBC will read the header information pointed to by the transmit pointer and process the frame accordingly (see transmit packet header description). The conditions for interrupting upon completing packet processing are specified in the transmit header command byte, which is stored in the buffer memory. Setting this bit with bit 13 set will force a transmit interrupt for test purposes.*

Bit 11: Set DMA Off. *Setting this bit to a one disables the DMA request logic.*

Bit 12: Set Rx Off. *Setting this bit to a one disables the EDLC receive logic. If the EDLC is actively receiving a packet when bit 12 is set, the EDLC receiver will be disabled after completing reception of the packet.*

Bit 13: Set Tx Off. *Setting this bit to a one disables the EDLC transmitter. If a packet is being transmitted when this bit is set, the packet will be aborted.*

Bit 14: FIFO Read. *When set to a one, the DMA FIFO direction is set to read from the packet buffer. The FIFO direction should not be changed from a write to a read until it is empty (see FIFO status bits).*

Bit 15: FIFO Write. *When set to a one, the DMA FIFO direction is set to write to the packet buffer. Changing the DMA FIFO direction clears the DMA FIFO.*

Status Register, A3-0 = 000X$_2$ (Read only)

Bit 0: DMA Interrupt Enable. *When set, this bit indicates that interrupts are enabled for terminal count during a DMA operation.*

Bit 1: Rx Interrupt Enable. *When set, this bit indicates that interrupts are enabled for receive events.*

Bit 2: Tx Interrupt Enable. *When set, this bit indicates that interrupts are enabled for transmit events.*

Bit 3: Buffer Window Interrupt Enable. *When set, this bit indicates that interrupts are enabled for buffer window reads from the packet buffer.*

Bit 4: DMA Interrupt. *When set, this bit indicates that a DMA operation has been completed. If the associated interrupt enable bit is set, an interrupt will also be asserted.*

Bit 5: Rx Interrupt. *When set, this bit indicates that a receive packet chain is available. If the associated interrupt enable bit is set, an interrupt is also asserted.*

Bit 6: Tx Interrupt. *When set, this bit indicates that a transmit packet or packet chain has been completed. If the associated interrupt enable bit is set, an interrupt is also asserted.*

Bit 7: Buffer Window Interrupt. *When set, this bit indicates that data has been read from the local buffer into the DMA FIFO and is ready to be read via the BIU. If the associated interrupt enable bit has been set, an interrupt is asserted.*

Bit 8: DMA On. *When set, this bit indicates that the DMA logic is enabled. When terminal count is asserted, this bit will be reset to indicate that the DMA activity has been completed.*

Bit 9: Rx On. *When set, this bit indicates that the EDLC receiver is enabled.*

Bit 10: Tx On. *When set, this bit indicates that the EDLC transmitter is enabled.*

Bits 11 & 12: *Not used.*

Bit 13: DMA FIFO Full. *When set, this bit indicates that the DMA FIFO is full.*

Bit 14: DMA FIFO Empty. *When set, this bit indicates that the DMA FIFO is empty.*

Bit 15: FIFO Direction. *When set, this bit indicates that the DMA FIFO is in the read direction; when cleared, it indicates that the DMA FIFO is in the write direction. After hardware or software reset, this bit is cleared.*

Configuration Register 1, A3-0 = 001X$_2$

Bits 0-3: BufferCode. *These four bits are the buffer window code bits, which determine the source of buffer window register reads and the destination of buffer window register writes.*

Buffer Code Selection Table

BufferCode Bits				Buffer Window Reg. Contents
3	2	1	0	
0	0	0	0	Station addr. reg. 0
0	0	0	1	Station addr. reg. 1
0	0	1	0	Station addr. reg. 2
0	0	1	1	Station addr. reg. 3
0	1	0	0	Station addr. reg. 4
0	1	0	1	Station addr. reg. 5
0	1	1	0	Address PROM
0	1	1	1	Transmit end area
1	0	0	0	Local buffer memory
1	0	0	1	Interrupt vector
1	0	1	X	Reserved — do not use
1	1	X	X	Reserved — do not use

Bits 4-5: DmaBurstInterval. *These two bits specify the interval between DMA requests.*

5	4	Burst Interval
0	0	Continuous
0	1	800 nanoseconds
1	0	1600 nanoseconds
1	1	3200 nanoseconds

If configured for continuous mode, the DMA request will persist until TermCt is asserted.

Bits 6-7: DmaBurstSize. *These two bits specify the DMA burst transfer count. In 16 bit mode, the number of transfers is half that in byte mode.*

DMA Burst Size Selection

7	6	# of DMA Transfers/Burst
0	0	1
0	1	4
1	0	8
1	1	16 (Illegal in word mode)

Bits 8-13: *These six bits select which of the station address register sets (each register set contains 6 bytes) will be used to compare incoming destination addresses. Bit 8 corresponds to station address register set 0, bit 9 to register set 1, . . . bit 13 to register set 5. A 1 in any bit enables that station address register set for reception. These bits are both read and write.*

Bits 14-15: *These two bits define the match modes for the EDLC receiver logic.*

15	14	Matchmode Description
0	0	Specific addresses only
0	1	Specific + broadcast addresses
1	0	Above + multicast addresses
1	1	All frames (promiscuous mode)

Configuration Register 2, A0-A3 = 010X$_2$

Bit 0: ByteSwap. *The normal order for packing packet bytes into a 16 bit word is low byte first, i.e., the first byte of a packet is contained in bits 0 through 7, the second byte in bits 8 through 15. Setting this bit to a 1 causes the high and low order bytes to be swapped for data reads and writes to the buffer window when the 8005 is in 16 bit mode. Control registers are not affected. This bit has no effect when the 8005 is in 8 bit mode. It should not be changed when a DMA is in progress. Changing this bit will not affect the sequence of receive data bytes in the local buffer memory since the swap occurs on the system (BIU) side of the buffer memory. This bit is both read and write.*

Bit 1: AutoUpdREA. *If this bit is set to 1, the receive end area register will be updated with the most significant byte of the DMA pointer register after each DMA transfer. In this way, as buffer memory space is released by reading from it, free buffer space is automatically allocated to the receive logic.*

Bit 2: Not used.

Bit 3: CRC Error Enable. *When set, the receiver will accept packets with CRC errors, place them in the local buffer and indicate that a packet is available via the Rx Interrupt status bit.*

Bit 4: Dribble Error. *When set, the receiver will accept packets with a byte alignment error.*

Bit 5: Short Frame Enable. *When set, frames of less than 512 bits (64 bytes) exclusive of preamble and start frame delimiter bits will be received and placed in the local buffer. Frames shorter than 6 bytes (2 bytes if bit 8=1) will always be rejected unless the receiver is in promiscuous mode (all addresses match) or multicast/broadcast mode and the packet is a multicast/broadcast packet.*

Bit 6: SlotSelect. *This bit selects the slot time used to calculate backoff time following a collision. When a 0, which is the state after reset, the slot time is 512 bits and meets the IEEE 802.3 standard; when a 1, the slot time is 128 bits, the interframe spacing is 24 bits and the collision jam is 2 bytes long, which is useful for smaller networks such as serial backplane buses.*

Bit 7: PreamSelect. *When this bit is a 0, which is the state after reset, the 8005 automatically transmits an IEEE 802.3 compatible 64 bit preamble; when set to 1, the user must supply the preamble as part of the packet data. The preamble must still follow the 802.3 form in order to be recognized by other 8005's, but may have arbitrary length. Note that a minimum of 16 preamble bits are required by the 8005 on reception.*

Bit 8: AddrLength. *This bit selects the length of address to be used in address matching. When a 0, which is the state after reset, the length is 6 bytes, which conforms with the IEEE 802.3 standard; when set to 1 the length is 2 bytes, which is useful in limited networks such as serial backplane buses.*

Bit 9: RecCrc. *If set to a 1, received frames will include the CRC (Frame Check Sequence). If set to a 0, which is the state after reset, the 4 byte CRC will be stripped when received.*

Bit 10: XmitNoCrc. *If set to a 1, the transmitter will not append the 4 byte frame check sequence to each frame transmitted. This is useful in local loopback to perform diagnostic checks, since it allows the software to provide its own CRC as the last four bytes of a frame to check the EDLC receiver CRC logic. It is initialized to 0 after hardware or software reset.*

Bit 11: Loopback. *This bit controls the external loopback pin. When set to a 1, the loopback output pin is at Vol; after reset or when cleared to a 0, the loopback output pin is at Voh.*

Bit 12: WatchTimeDis. *This bit controls the external watchdog timer disable pin. When set to a 1, the watchdog timer disable pin is at Voh; when cleared to 0 or after reset, the watchdog timer disable pin is at Vol.*

Bits 13-14: *Not used.*

Bit 15: ChipRst. *Writing a 1 to this bit is the same as asserting the hardware reset input. Chip reset should be followed by a 4 μs wait before attempting another access. Reads as a 0.*

Receive End Area Register, A3-0 = $011X_2$

Bits 0-7: ReaPtr. The receive end area pointer contains the high order byte of the local buffer address at which the receive logic must stop to prevent writing over previously received packets. If the receive logic reaches this address it will stop; the receiver will be turned off and an interrupt will be issued. The receiver can be restarted by freeing up buffer space and turning the receiver back 'ON' again. This register can be updated automatically by setting bit 1 in configuration register #2, which causes ReaPtr to be updated after each DMA read. It is both read and write.

Buffer Window Register, A3-0 = $100X_2$

This register provides access to the area specified by the buffer code bits (bits 0-3) in configuration register #1. When the buffer code points to either the buffer memory (Bcode=1000_2) or the address PROM (Bcode=0110_2), the address of the data transferred through this register is determined by the DMA pointer register.

Receive Pointer Register, A3-0 = $101X_2$

The receive pointer register provides a 16 bit address that points to the next buffer memory location into which data or header information will be placed by the receive logic. The low order 8 bits contain the least significant byte of the address. Prior to enabling the receiver, this register should be set to point to the beginning of the receive area in the local buffer. This initial value should be remembered by system software since it will be the address of the first byte of the header block of the first packet received. While receiving, the receive pointer will be incremented for each byte stored into the local buffer. When the receive pointer increments past hex FFFF the most significant byte will be set equal to the value of the transmit end area + 1 and the least significant byte will be set to 00. Reading this register may be done at any time. It should be written only when the transmitter is idle.

Transmit Pointer Register, A3-0 = $110X_2$

The transmit pointer register points to the current location being accessed by the transmit logic. Before starting the transmitter, software loads this register with the address of the beginning of a transmit packet chain.

DMA Address Register, A3-0 = $111X_2$

The DMA address register provides 16 bits of address information to the local buffer memory and 8 bits of address to the address PROM, depending on the buffer code written into configuration register 1. Its normal use is to provide an auto-incremented address to the local buffer so that packet data can be moved via the BIU. **When the DMA address register is loaded, the DMA FIFO is cleared.** Therefore it is important to insure that the DMA FIFO is empty if it is in the write direction before loading the DMA register. When writing a packet to be transmitted, the DMA address register automatically wraps around to 0000 when the transmit end area (contained in an indirect register, buffer code 0111_2) has been reached. When reading receive packets, the DMA address register automatically wraps around to the receive start area (transmit end area + 1) when address $FFFF has been read.

Indirectly Accessed Registers

Infrequently used registers, e.g., those that are normally loaded only when initially configuring the 8005, are accessed indirectly by first loading the buffer code bits in configuration register #1 with a code that points to the desired register. Reads and writes occur through the buffer window register. All indirect registers (a total of 38) are 8 bits wide, thus only D0-D7 are used.

Station Address Registers

The 8005 contains six 48-bit station address registers, which permits one network connection to provide up to 6 different server functions. Each of these station address registers is comprised of six 8-bit registers which must be loaded through the buffer window register. Only those station address registers that will be enabled for address matching need to be loaded.

To load a station address register, first turn the receiver off. Select the desired station number (0-5) by writing the buffer code bits in configuration register #1. Next do 6 sequential **byte** writes to the buffer window register as follows: Write the least significant byte of the 6 byte station address; its low order bit, bit 0, will be the first bit received. Next write the remaining 5 bytes in ascending order. To read a station address register, select the desired station number by writing the buffer code bits in configuration register #1. Do 6 sequential reads to the buffer window; the first byte read will be the least significant byte. If the 8005 is configured to match 2 byte instead of 6 byte addresses, only the first 2 station address bytes are significant, although all 6 will read and write properly.

Transmit End Area Pointer

The 8 bit value in this register defines, with 256 location granularity, the end of the transmit packet buffer area by specifying the highest value permitted in the most significant byte of the transmit pointer register and, when loading a packet to be transmitted, the DMA address register. It also indirectly defines the receive start area *address, since the PBC automatically calculates the high order byte of this address by adding 1 to the transmit end area pointer. To read or write this value, load the buffer code bits of configuration register #1 with the code for the transmit end area, and do a read or write to the buffer window register.*

Interrupt Vector Register

This read/write register is accessed through the buffer window register when the buffer code in configuration register #1 is 9. It contains an 8 bit vector which is placed on data bits D0-D7 during an interrupt acknowledge cycle. If BUSMODE=0, an interrupt acknowledge cycle is defined by INT=0, IACK*=0 and READ/WRITE*=1. When BUSMODE=1, an interrupt acknowledge cycle is defined by INT=1, IACK*=0, and IOR*=0.*

Other Buffer Window Register Uses

Address PROM Access

The 8005 supports access to up to 256 bytes of configuration data contained in a PROM or EEPROM. This can be used for any purpose, such as storing station addresses, register configurations, network connection data, etc. The address to the PROM is supplied by the DMA register through data bus bits D8-D15; the data lines from the PROM are connected to D0-D7. Chip select for the PROM is provided by output APEN. Before accessing this PROM, insure that transmit, receive and DMA sections of the 8005 are disabled. Next load the PROM starting address which you wish to access into the low byte of the DMA register. Set the buffer code bits in configuration register #1 to point to the address PROM. Each access to the buffer window register will chip enable the PROM, permitting reads or writes. Successive accesses will increment the DMA register to point to the next byte in the PROM. If a 16 bit wide bus is used, the address supplied to the PROM will also be read on D8-D15.*

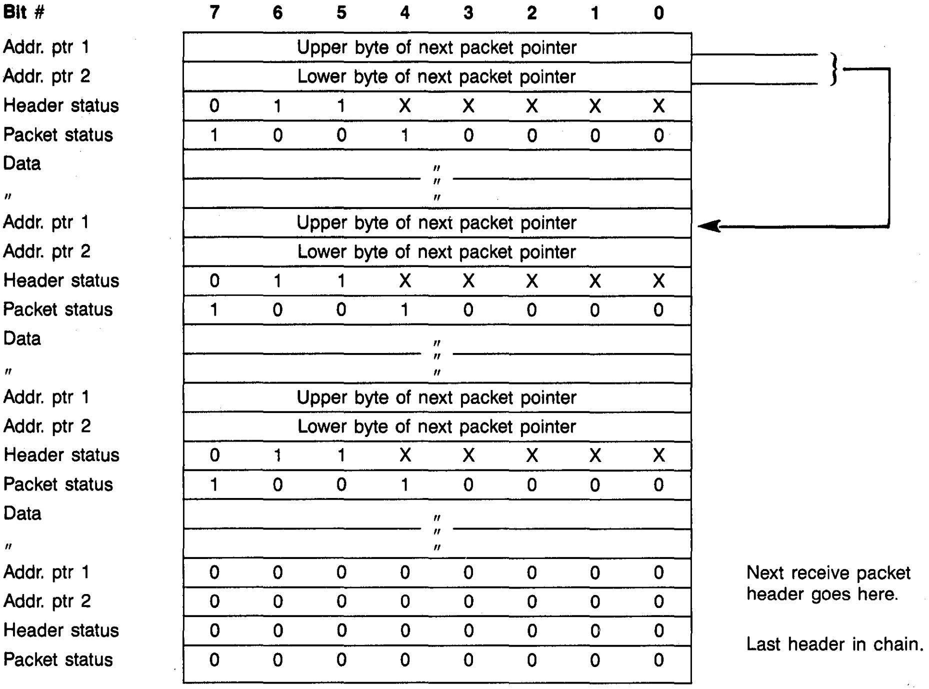
Buffer Memory Access

The normal state of the buffer code bits, once the 8005 has been initialized with station addresses and buffer areas have been allocated, is with buffer memory selected. Access to the local buffer memory is provided by the DMA register, which automatically increments after each byte or word transfer. To read from or write to the local buffer, set the buffer code to select the buffer memory, set the FIFO direction (Command Register bits 14 and 15), load a starting address into the DMA register and read from or write to the buffer window register. This is the simplest way to access the local buffer as it requires no system DMA activity. It also permits network layer software to read network control data at the beginning of a received packet to determine if it is necessary to move the packet into global memory for further processing or simply reuse the area occupied by the packet by updating the receive end area register. For fastest transfer speed, e.g., to move packet data, an external system DMA controller is supported via the DMA Request ouput, DMA Acknowledge input and Terminal Count input signals.

Asynchronous Bus Control

The 8005 supports asynchronous bus control via the READY/DTACK pin. By using READY/DTACK* the cycle time minimums listed in the tables A thru J need not be observed. READY/DTACK* takes care of these cycle times. This greatly simplifies the task of interfacing to the 8005 and also results in a higher overall data rate. To achieve the highest possible data rate, all data transfers should terminate within 50 ns of READY/DTACK* being asserted. This permits a sustained system bus transfer rate of 1.66 MWords/sec (3.33 Mbytes/sec) in 16 bit mode or 2.5 Mbytes/sec in 8 bit mode.*

Example of Chained Receive Frames



Bit #	7	6	5	4	3	2	1	0
Addr. ptr 1	Upper byte of next packet pointer							
Addr. ptr 2	Lower byte of next packet pointer							
Header status	0	1	1	X	X	X	X	X
Packet status	1	0	0	1	0	0	0	0
Data	″							
″	″							
Addr. ptr 1	Upper byte of next packet pointer							
Addr. ptr 2	Lower byte of next packet pointer							
Header status	0	1	1	X	X	X	X	X
Packet status	1	0	0	1	0	0	0	0
Data	″							
″	″							
Addr. ptr 1	Upper byte of next packet pointer							
Addr. ptr 2	Lower byte of next packet pointer							
Header status	0	1	1	X	X	X	X	X
Packet status	1	0	0	1	0	0	0	0
Data	″							
″	″							
Addr. ptr 1	0	0	0	0	0	0	0	0
Addr. ptr 2	0	0	0	0	0	0	0	0
Header status	0	0	0	0	0	0	0	0
Packet status	0	0	0	0	0	0	0	0

Next receive packet header goes here.

Last header in chain.

Packet Header Bytes

Transmit Header Command Byte
(Byte #3)

7	6	5	4	3	2	1	0
1	Chain Continue	Data Follows	Not Used	Xmit Sucess Enable	16 Coll. Enable	Coll. Int. Enable	Babble Int. Enable

Receive Header Status Byte
(Byte #3)

7	6	5	4	3	2	1	0
0	Chain Continue	Data Follows	Not Used	Not Used	Not Used	Not Used	Not Used

Transmit Packet Status Byte
(Byte #4)

7	6	5	4	3	2	1	0
Done	← Reserved →				16 Coll.	Collision	Babble

Receive Packet Status Byte
(Byte #4)

7	6	5	4	3	2	1	0
Done	Not Used	Not Used	Not Used	Short Frame	Drib. Error	CRC Error	Oversize

8005 Configuration and Pointer Registers

Command (write only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Write	FIFO Read	Set Tx Off	Set Rx Off	Set DMA Off	Set Tx On	Set Rx On	Set DMA On	Bufr Wndow Ack	Tx Int Ack	Rx Int Ack	DMA Int Ack	Bufr Wndow Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Status (read only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Dir	FIFO Empty	FIFO Full	Not Used	Not Used	Tx On	Rx On	DMA On	Bufr Wndow Int	Tx Int	Rx Int	DMA Int	Bufr Wndow Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Configuration Register #1 (A3-0 = 001X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addr Match Mode	Addr Match Mode	Sta. 5 Enable	Sta. 4 Enable	Sta. 3 Enable	Sta. 2 Enable	Sta. 1 Enable	Sta. 0 Enable	DMA Burst Lngth	DMA Burst Lngth	DMA Burst Intvl	DMA Burst Intvl	Buffr Code 3	Buffr Code 2	Buffr Code 1	Buffr Code 0

Configuration Register #2 (A3-0 = 010X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	Not Used	Not Used	Watch Time Dis.	Loop-Back	Xmit No CRC	Recv. CRC	Addr Leng.	Xmit No Pream	Slot Time Sel.	Short Frame Enable	Drib. Error Enable	CRC Error Enable	Not Used	Auto Update REA	Byte Swap

Receive End Area Register (A3-0 = 011X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	Receive End Area Pointer							

Receive Pointer Register (A3-0 = 101X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT RECEIVE BYTE															

Transmit Pointer Register (A3-0 = 110X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT TRANSMIT BYTE															

DMA Address Register (A3-0 = 111X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR SYSTEM READS OR WRITES															

Buffer Window Register (A3-0 = 100X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFFER CODE BITS DETERMINE SOURCE/DESTINATION FOR READS AND WRITES															

Station Address Register Format
2 of 6 Station Address Registers Shown

7 6 5 4 3 2 1	0
STATION ADDRESS REGISTER 0 BYTE 0 BUFFER CODE = 0000	M S B
STATION ADDRESS REGISTER 0 BYTE 1 BUFFER CODE = 0000	
STATION ADDRESS REGISTER 0 BYTE 2 BUFFER CODE = 0000	
STATION ADDRESS REGISTER 0 BYTE 3 BUFFER CODE = 0000	
STATION ADDRESS REGISTER 0 BYTE 4 BUFFER CODE = 0000	
STATION ADDRESS REGISTER 0 BYTE 5 BUFFER CODE = 0000	

7 6 5 4 3 2 1	0
STATION ADDRESS REGISTER 1 BYTE 0 BUFFER CODE = 0001	M S B
STATION ADDRESS REGISTER 1 BYTE 1 BUFFER CODE = 0001	
STATION ADDRESS REGISTER 1 BYTE 2 BUFFER CODE = 0001	
STATION ADDRESS REGISTER 1 BYTE 3 BUFFER CODE = 0001	
STATION ADDRESS REGISTER 1 BYTE 4 BUFFER CODE = 0001	
STATION ADDRESS REGISTER 1 BYTE 5 BUFFER CODE = 0001	

Absolute Maximum Stress Ratings

Temperature:

Storage	*−65°C to +150°C*
Under Bias	*−10°C to +80°C*
All Inputs and Outputs with Respect to V_{SS}	*+6 V to −0.3 V*

Recommended Operating Conditions

V_{CC} Supply Voltage	5V ± 10%
Ambient Temperature	0°C to 70°C

DC Operating Characteristics (Over the V_{CC} and Temperature Ranges)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I_{IL}	Input/Output Leakage		10 −10	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = 0.1V$
I_{CC}	Active V_{CC} Current		350	mA	CS* = V_{IL}, Outputs Open
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH1}	Input High Voltage (except TXC*, RXC, CLK)	2.0	$V_{CC} + 1$	V	
V_{IH2}	Input High Voltage (TXC*, RXC, CLK)	3.5	$V_{CC} + 1$	V	
V_{OL1}	Output Low Voltage (except AD_{0-7})		0.40	V	$I_{OL} = 2.1$ mA
V_{OL2}	Output Low Voltage (AD_{0-7})		0.40	V	$I_{OL} = 200\ \mu A$
V_{OH1}	Output High Voltage (except AD_{0-7})	2.4		V	$I_{OH} = -400\ \mu A$
V_{OH2}	Output High Voltage (AD_{0-7})	2.4		V	$I_{OH} = -200\ \mu A$

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Capacitance (Characterized — Not Tested)
Ambient Temperature = 25°C, F = 1 MHz

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
C_{IN}	Input Capacitance		15	pF	$V_{IN} = 0$
C_{OUT}	Output Capacitance		15	pF	$V_{OUT} = 0$

Electrostatic Discharge Characteristics (Characterized — Not Test)

Symbol	Parameter	Value	Test Condition
V_{ZAP}	E.S.D. Tolerance	> 2000 V	Mil-STD 883 Meth. 3015

A.C. Test Conditions

Output Load:
AD0-AD7, RAS, CAS*, W*, G*: I(load) = ± 200 μA, C(load) = 50 pF.*
All Other Outputs: 1 TTL Gate and C(load) = 100 pF.
Input Rise and Fall Times (except TXC, RXC, CLK): 10 ns. maximum.
Input Rise and Fall Times (TXC, RXC, CLK): 5 ns. maximum.
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs: 1 V and 2 V
Outputs: 0.8 V and 2 V

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table A. Bus Write Cycle – BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	50		ns
2	TRWVCSL	R/W* Setup Time	50		ns
3	TCSLCSH	CS* Pulse Width	100		ns
4	TDVCSL	Data Setup Time	70		ns
5	TCSHDX	Data Hold Time	0		ns
6	TCSLDTL	DTACK* Assertion Delay[4]		50	ns
7	TCSHDTH	DTACK* Deassertion Delay		50	ns
8	TCSHDTZ	DTACK* Hi-Z Delay		50	ns
9	TCSHAX	Address Hold Time	20		ns
10	TCSHRWX	R/W* Hold Time	20		ns
11	TCSHCSL	CS* High Time	200		ns
12	TCSLCSL	Write Cycle Time: a. FIFO Data Write[1] b. Configuration Regs.[1,2] c. Pointer Regs.[3]	 600 600 1600		ns ns ns ns
13	TCSLAPL	APEN* Assert Time		50	ns
14	TCSHAPH	APEN* Deassert Time		50	ns
15	TCSLENL	EN* Assert Delay		50	ns
16	TCSHENH	EN* Deassert Delay		50	ns
17	TCSLDTV	CS* Active to DTACK* Valid		50	ns

NOTES:
1. Cycle time is for 16 bit writes. If BUSSIZE = 0 (8 bit writes), the cycle time is 400 ns.
2. Configuration Registers are: Command/Status Register, Configuration Register #1, & 2, Interrupt Vector Register, and Station Address Registers.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA Register. If BUSSIZE = 0, the cycle time is 1000 ns.
4. DTACK* assertion will be delayed for all subsequent reads or writes until reference 12 cycle time has elapsed.

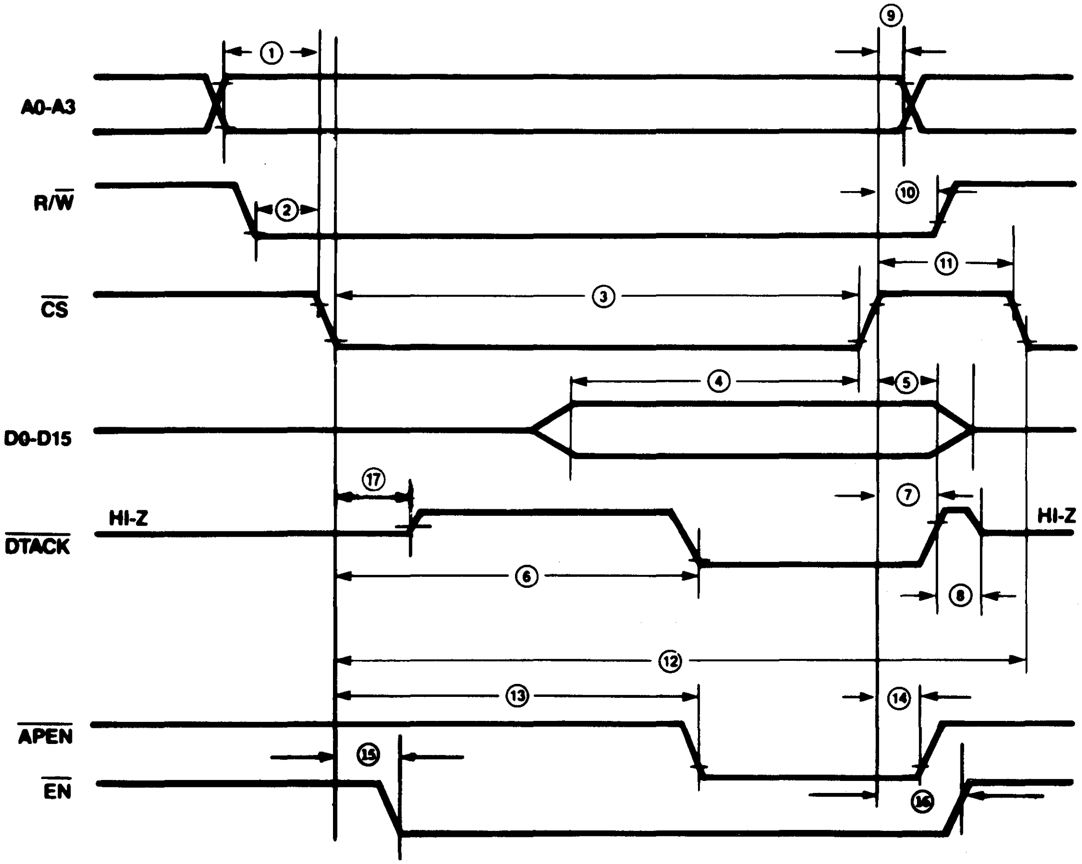


Figure A. Bus Write Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table B. Bus Read Cycle — BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	50		ns
2	TRWVCSL	R/W* Setup Time	50		ns
3	TCSLDV	Read Data Delay from CS*: a. FIFO Data b. Configuration Regs.[1] c. Other Pointer Regs.[2]		 100 700 1700	ns ns ns ns
4	TCSLDTL	DTACK* Assertion Delay	ref. 3 + 50		ns
5	TCSLCSH	CS* Pulse Width	100		ns
6	TCSHDTH	DTACK* Deassertion Delay		50	ns
7	TCSHDTZ	DTACK* Hi-Z Delay		50	ns
8	TCSHDZ	Data Hi-Z Delay		100	ns
9	TCSHDX	Data Hold Time	20		ns
10	TCSHRWX	R/W* Hold Time	20		ns
11	TCSHAX	Address Hold Time	20		ns
12	TCSHCSL	CS* High Time	200		ns
13	TCSLCSL	Read Cycle Time	300		ns
14	TCSLAPL	APEN* Assert Delay		50	ns
15	TCSHAPH	APEN* Deassert Delay		50	ns
16	TCSLENL	EN* Assert Delay		50	ns
17	TCSHENH	EN* Deassert Delay		50	ns
18	TCSLDTV	CS* Active to DTACK* Valid		50	ns

NOTES:
1. Configuration Registers are: Command/Status Register, Configuration Register #1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers. If BUSSIZE = 0 (8 bit writes), the read data delay is 500 ns.
2. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register. If BUSSIZE = 0, the read data delay is 1100 ns.

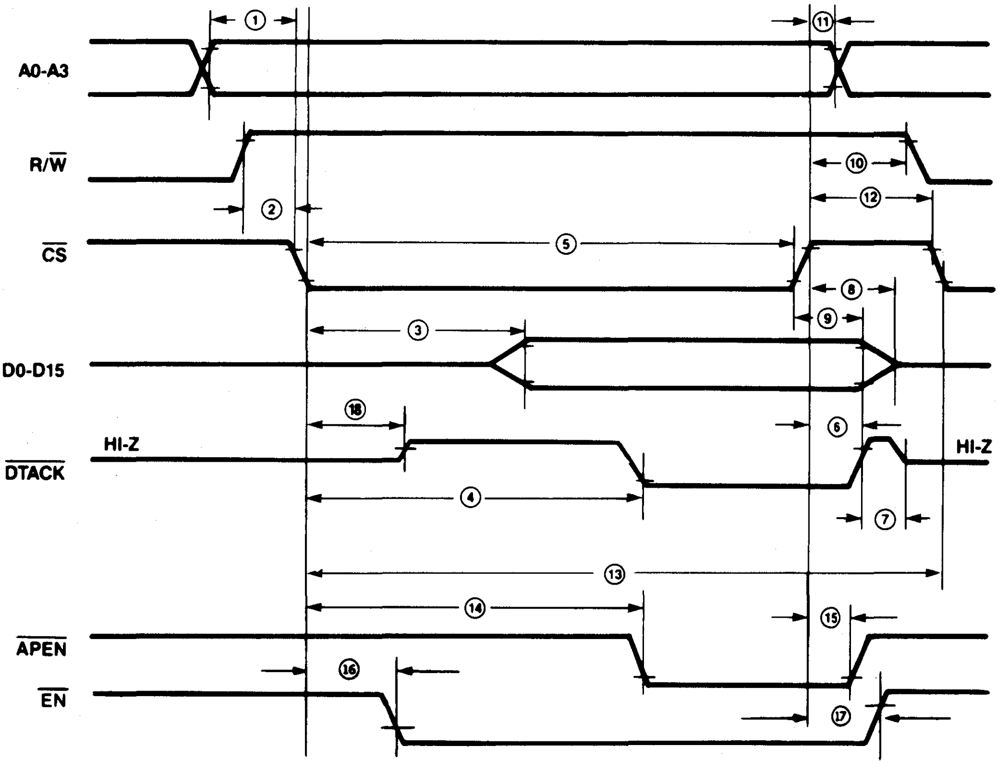


Figure B. Bus Read Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table C. Interrupt Cycle – BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TIAVQV	Data Delay from IACK*		500	ns
2	TIAVDTV	DTACK* Delay from IACK*		500	ns
3	TDTLIAH	IACK* Hold from DTACK*	0		ns
4	TIAHDX	Data Hold from IACK* Deassert	20		ns
5	TIAHDZ	Data Hi-Z from IACK* Deassert		100	ns
6	TIAHDTH	DTACK* Deassert from IACK*		50	ns
7	TIAHDTZ	DTACK* Hi-Z from IACK* Deassert		50	ns
8	TRHIAL	R/W* Setup Time	20		ns
9	TIAHRX	R/W* Hold Time from IACK*	0		ns
10	TIALENL	EN* Assert Delay		50	ns
11	TIAHENH	EN* Deassert Delay		50	ns
12	TIALDTV	IACK* Active to DTACK* Valid		50	ns

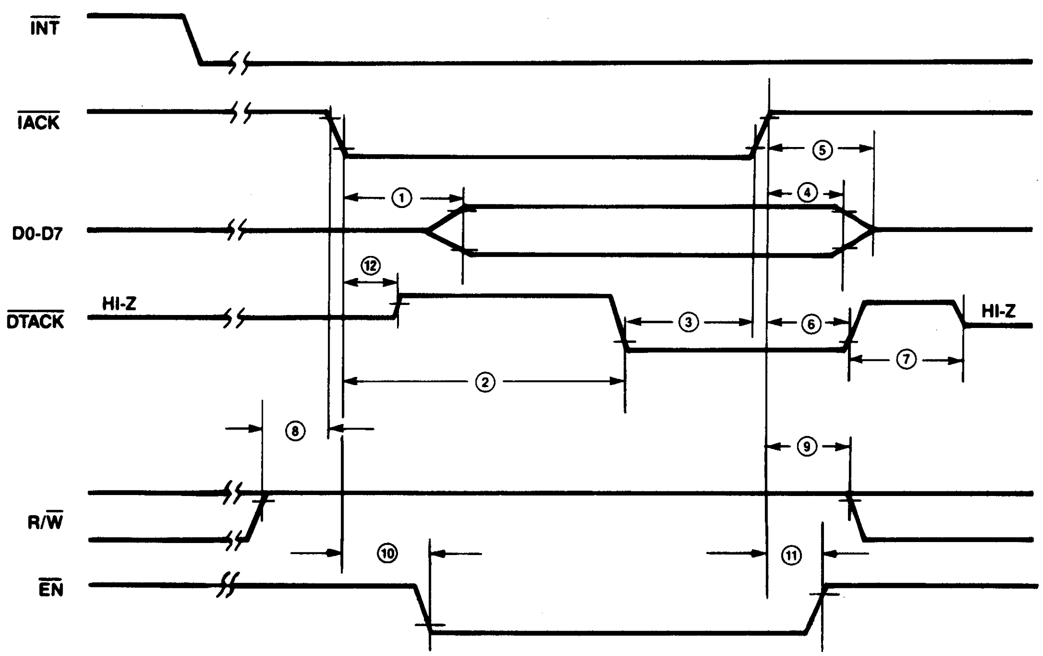


Figure C. Interrupt Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table D. DMA Read Cycle – BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRWHDAL	R/W* Setup Time	50		ns
2	TDALDAH	DACK* Pulse Width[1]	100		ns
3	TDALDV	Data Delay Time [2]		100	ns
4	TDAHDX	Data Hold Time		20	ns
5	TDAHDZ	Data Hi-Z Delay		100	ns
6	TDAHDAL	DACK* High Time	200		ns
7	TDALDAL	DMA Read Cycle Time	300		ns
8	TTCLDAL	TERMCT* Setup Time	0		ns
9	TDAHRWX	R/W* Hold Time	20		ns
10	TDAHTCX	TERMCT* Hold Time	100		ns
11	TDALDRH	DREQ* Delay		100	ns
12	TDALDTL1	DTACK* Assertion Delay [2]		50	ns
13	TDAHDTH	DTACK* Deassertion Delay		50	ns
14	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
15	TDRLDAL	DREQ* Setup to DACK*	0		ns
16	TDALENL	EN* Assert Delay		50	ns
17	TDAHENH	EN* Deassert Delay		50	ns
18	TDALDTV	DACK* Active to DTACK* Valid		50	ns
19	TDALDTL2	Read Recovery Time[3,4]	450	750	ns

NOTES:

1. DACK* must be asserted until DTACK* is asserted and for a minimum of 100 ns
2. This delay applies only if the 8005 is "ready" when DACK* is asserted, i.e., the first read of a burst, or a read that occurs after the Ref. #19 TDALDTL2 period has elapsed.
3. The BIU pre-fetches FIFO data. Thus, data is available immediately for the first read of any burst. Once the BIU detects a read operation, it begins fetching the next byte or word of data. This occurs during the Ref. #19 TDALDTL2 period. If a subsequent DACK* occurs within the Ref. #19 TDALDTL2 period, DTACK* will stay deasserted until the FIFO data has been fetched. If the subsequent DACK* does not occur until after the Ref. #19 TDALDTL2 period has elapsed, then the 8005 is "ready" and Ref. #12 TDALDTL1 applies.
4. Subtract 200 ns if BUSSIZE = 0 (8 bit mode).

All the timings in this table also apply when reading data with programmed I/O; CS* replaces DACK* and the DREQ* and TERMCT* signals do not apply. A0-A3 setup times are the same as R/W*.

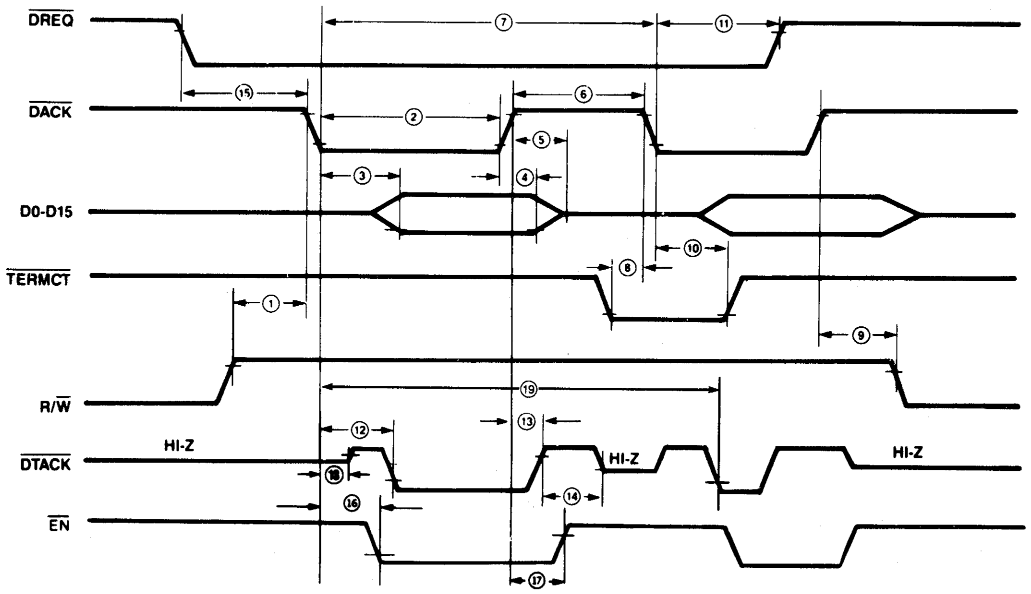


Figure D. DMA Read Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table E. DMA Write Cycle – BUSMODE = 0

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRWLDAL	R/W* Setup Time	50		ns
2	TDALDAH	DACK* Pulse Width[1]	100		ns
3	TDVDAH	Data Setup Time	70		ns
4	TDAHDX	Data Hold Time	0		ns
5	TTCLDAL	TERMCT* Setup Time	0		ns
6	TDAHDAL	DACK* High Time	200		ns
7	TDALDAL	DMA Write Cycle Time	300		ns
8	TDALTCH	TERMCT* Hold Time	100		ns
9	TDAHRWH	R/W* Hold Time	20		ns
10	TDALDRH	DREQ* Delay		100	ns
11	TDALDTL	DTACK* Assertion Delay[2]		50	ns
12	TDAHDTH	DTACK* Deassertion Delay		50	ns
13	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
14	TDRLDAL	DREQ* Setup to DACK*	0		ns
15	TDALENL	EN* Assert Delay		50	ns
16	TDAHENH	EN* Deassert Delay		50	ns
17	TDALDTV	DACK* Active to DTACK* Valid		50	ns
18	TDAHDTL	Write Recovery Time[3,4]	450	750	ns

NOTES:
1. DACK* must be asserted until DTACK* is asserted and for a minimum of 100 ns.
2. This delay applies only if the 8005 is "ready" when DACK* is asserted, i.e., the first write of a burst, or a write that occurs after Ref. #18 TDAHDTL period has elapsed.
3. The trailing edge of DACK* initiates an internal write sequence that lasts a minimum of 450 ns and a maximum of 750 ns in 16 bit mode. Should another DACK* occur during this period, DTACK* will remain deasserted until Ref. #18 TDAHDTL period has elapsed. If the subsequent DACK* does not occur until after the internal write sequence has ended, then the 8005 is "ready" and Ref. #11 TDALDTL applies.
4. Subtract 200 ns if BUSSIZE = 0 (8 bit mode).

All the timings in this table also apply when writing data with programmed I/O; CS* replaces DACK* and the DREQ*, TERMCT* signals do not apply. A0-A3 setup times are the same as R/W*.

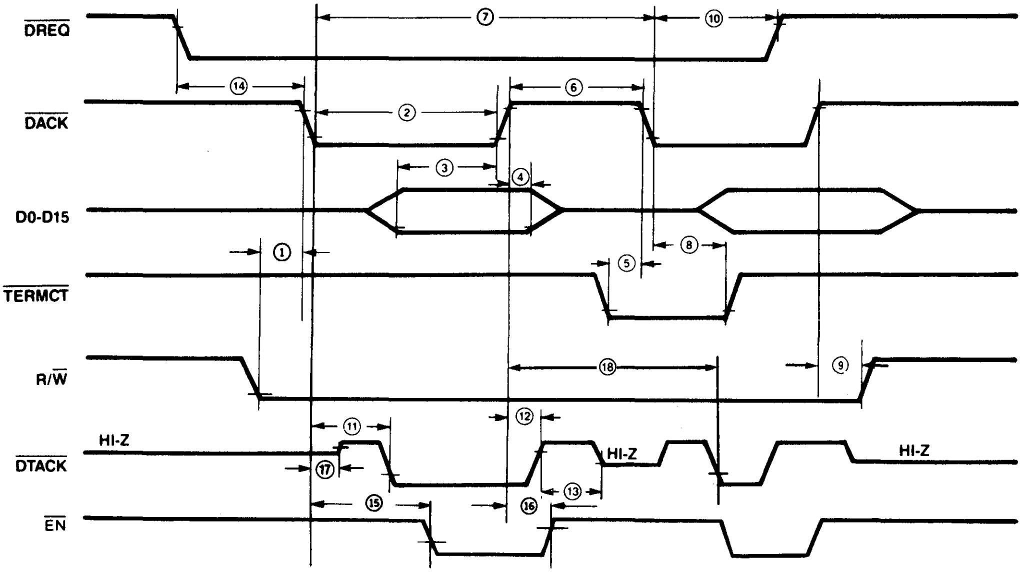


Figure E. DMA Write Cycle Timing Diagram — BUSMODE = 0

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table F. Bus Write Cycle – BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVWL	Address Setup Time	50		ns
2	TCSLWL	CS* Setup Time	50		ns
3	TWLWH	IOW* Pulse Width	100		ns
4	TDVWH	Data Setup Time	70		ns
5	TWHDX	Data Hold Time	0		ns
6	TWLRYL	READY Deassert Delay		35	ns
7	TCSLRYV	IOW* Active to READY Valid		50	ns
8	TCSHRYZ	READY Delay to Hi-Z		50	ns
9	TWHAX	Address Hold Time	20		ns
10	TWHCSH	CS* Hold Time	20		ns
11	TWHWL	Write Recovery Time	200		ns
12	TWLCSL	Write Cycle Time a. FIFO Data Write[1] b. Configuration Regs.[1,2] c. Pointer Registers[3]	 600 600 1600		ns ns ns ns
13	TWLAPL	APEN* Assert Delay		50	ns
14	TWHAPH	APEN* Deassert Delay		50	ns
15	TCSLENL	EN* Assert Delay		50	ns
16	TCSHENH	EN* Deassert Delay		50	ns

NOTES:
1. Cycle time is for 16 bit writes. If BUSSIZE = 0 (8 bit writes), the cycle time is 400 ns.
2. Configuration Registers are: Command/Status Register, Configuration Register #1, & 2, Interrupt Vector Register, and Station Address Registers.
3. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA Register. If BUSSIZE = 0, the cycle time is 1000 ns.
4. READY* assertion will be delayed for all subsequent reads or writes until reference 12 cycle time has elapsed.

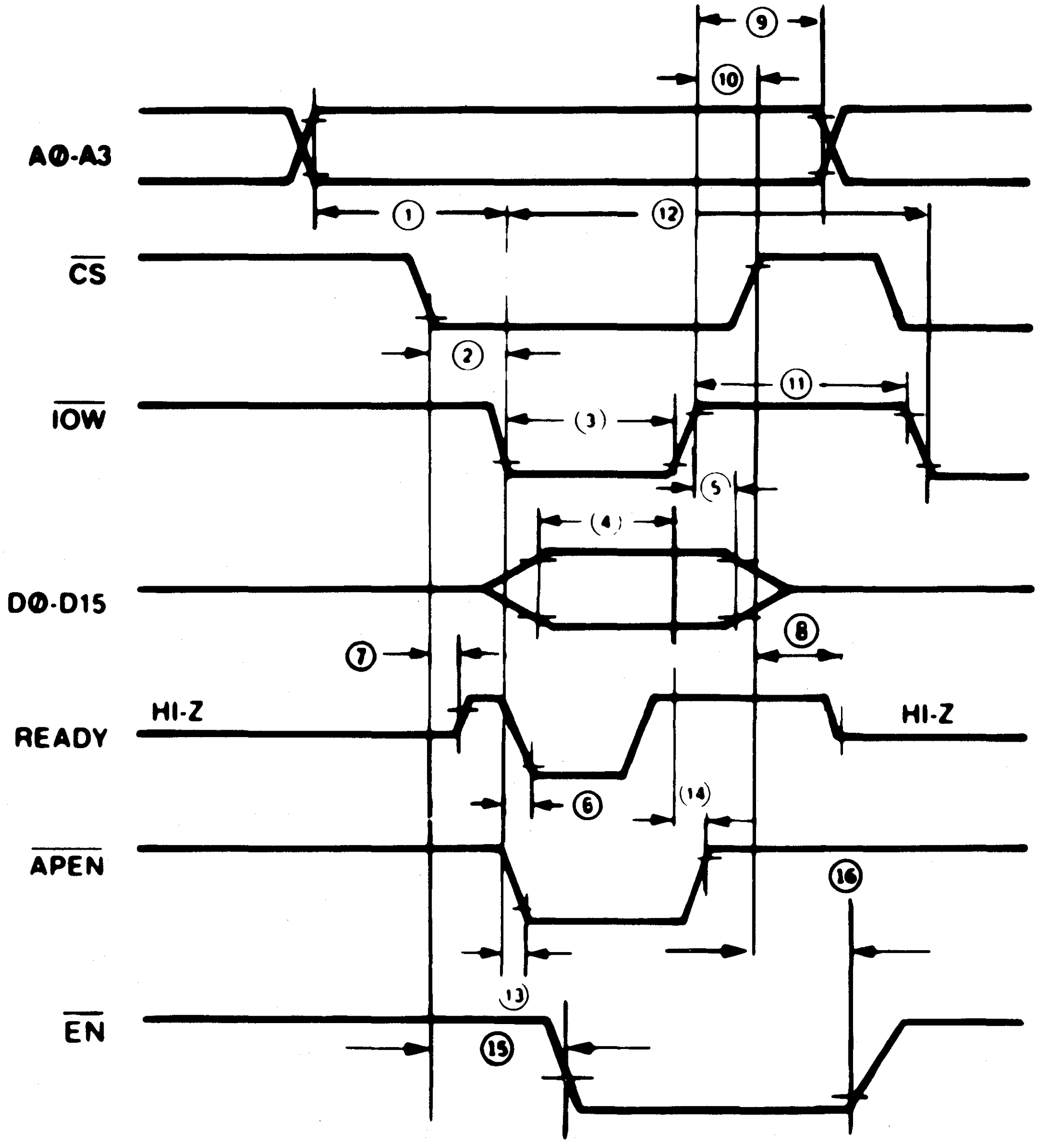


Figure F. Write Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table G. Bus Read Cycle – BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRL	Address Setup Time	50		ns
1a	TCSLRL	CS* Setup Time	50		ns
2	TRHRL	Read Recovery Time	200		ns
3	TRLRYH	READY Assert Delay			ns
		a. FIFO Data		100	ns
		b. Configuration Regs.[1]		700	ns
		c. Pointer Registers[2]		1700	ns
4	TRLRYL	READY Deassertion Delay		35	ns
5	TDVRYH	Data Setup to READY Assert	−50	0	ns
6	TCSHRYZ	READY Delay to Hi-Z		50	ns
7	TRHDX	Data Hold Time	20		ns
8	TRHDZ	Data Delay to Hi-Z		100	ns
9	TRHAX	Address Hold Time	20		ns
10	TRHCSH	CS* Hold Time	20		ns
11	TRLRH	IOR* Pulse Width	100		ns
12	TRLAPL	APEN* Assert Delay		50	ns
13	TRHAPH	APEN* Deassert Delay		50	ns
14	TCSLENL	EN* Assert Delay		50	ns
15	TCSHENH	EN* Deassert Delay		50	ns
16	TCSLRYV	CS* Active to READY Valid		50	ns

NOTES:

1. Configuration Registers are: Command/Status Register, Configuration Register #1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers. If BUSSIZE = 0 (8 bit writes), the read data delay is 500 ns.
2. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register. If BUSSIZE = 0, the read data delay is 1100 ns.

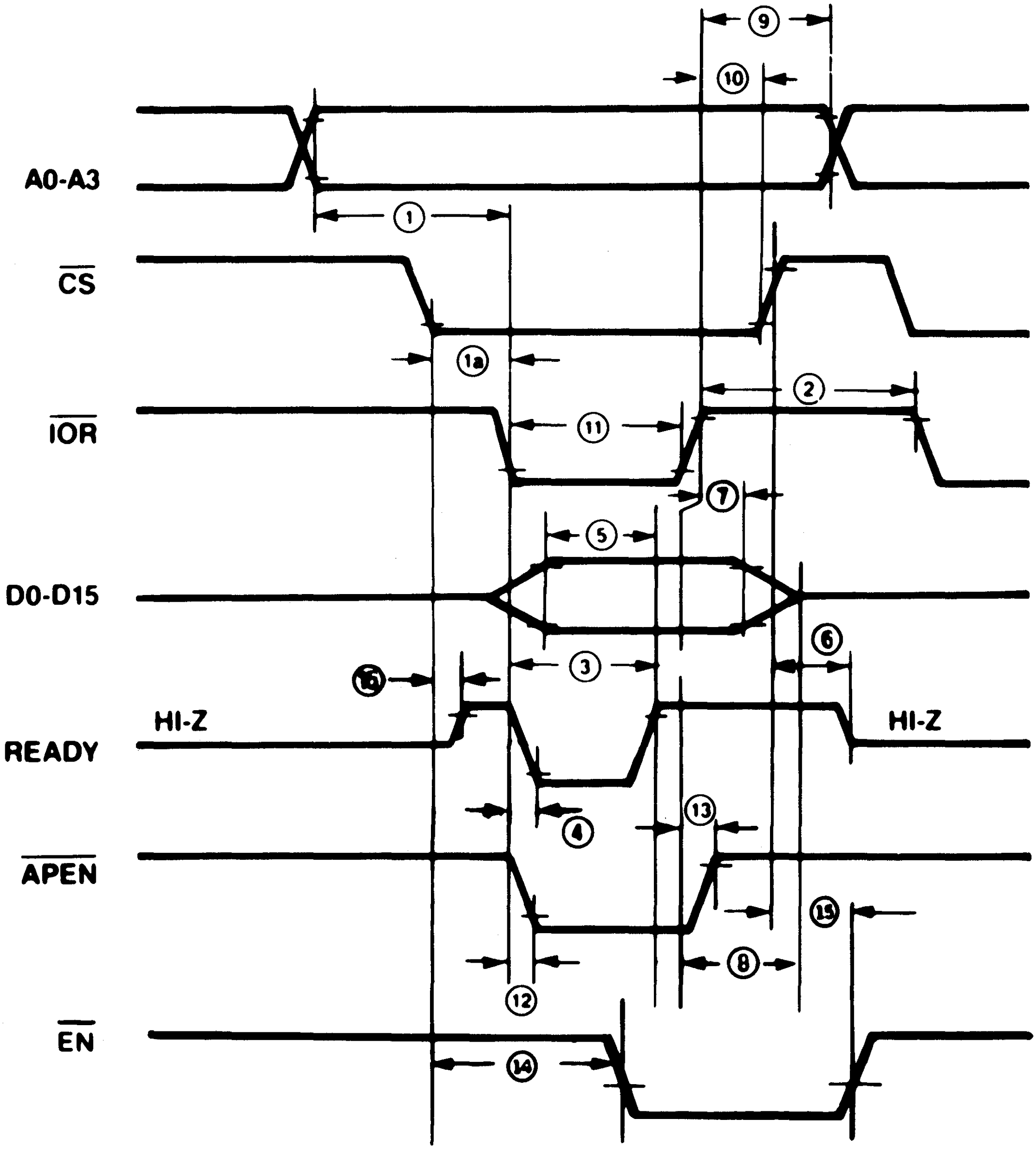


Figure G. Read Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock) ***Over the operating V_{CC} and Temperature Range***

Table H. Interrupt Cycle - BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRLDV	Data Delay from IOR*		500	ns
2	TRLRYL	READY Deassertion Delay		35	ns
3	TRLRYH	READY Assert Delay		500	ns
4	TIAHDZ	Data Delay to Hi-Z		100	ns
5	TIAHRYZ	READY Delay to Hi-Z		50	ns
6	TIAHDX	Data Hold from IOR*	20		ns
7	TELRL	IACK* Setup Time	50		ns
8	TIALENL	EN* Assert Delay		50	ns
9	TIAHENH	EN* Deassert Delay		50	ns
10	TIALRYV	IACK* Active to READY Valid		50	ns

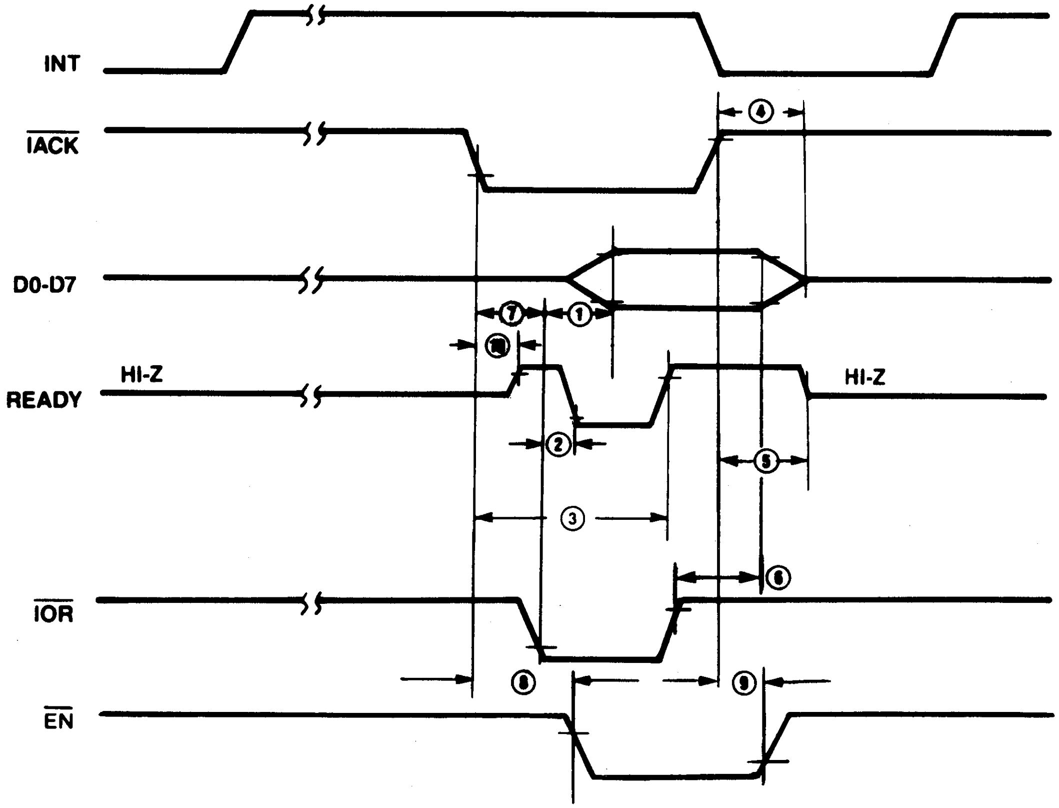


Figure H. Interrupt Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table I. DMA Write Cycle – BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TDALWL	DACK* Setup Time	50		ns
2	TWLWH	IOW* Pulse Width[1]	100		ns
3	TDVWH	Data Setup Time	70		ns
4	TWHDX	Data Hold Time	0		ns
5	TWHWL	IOW* High Time	200		ns
6	TWLWL	Write Cycle Time	300		ns
7	TTCHTCL	TERMCT Pulse Width	80		ns
8	TTCLDRL	DREQ Delay from TERMCT		100	ns
9	TWLDRL	DREQ Delay from IOW*		100	ns
10	TDRHDAL	DACK* Delay	0		ns
11	TWLTCH	TERMCT* Assert Delay	20		ns
12	TTCHWH	IOW* Hold Time	80		ns
13	TWHDAH	DACK* Hold Time	0		ns
14	TDALENL	EN* Assert Delay		50	ns
15	TDAHENH	EN* Deassert Delay		50	ns
16	TDALRYL	READY Deassert Delay		35	ns
17	TWHRYH	Write Recovery Time[2, 3]	450	750	ns
18	TDAHRYZ	READY Delay to Hi-Z		50	ns
19	TDALRYV	DACK* Active to READY Valid		50	ns

NOTES:
1. IOW* must be asserted until READY is asserted and for a minimum of 100 ns.
2. The trailing edge of IOW* initiates an internal write sequence that lasts a minimum of 450 ns and a maximum of 750 ns in 16 bit mode. Should another IOW* occur during this period, READY deasserts (Ref. #16 TDALRYL) and then asserts after the internal write sequence has finished (Ref. #17 TWHRYH). If the subsequent IOW* does not occur until after the internal write sequence has ended, then Ref. #17 TWHRYH has no meaning since READY does not deassert under this condition.
3. Subtract 200 ns when BUSSIZE = 0 (8 bit mode).

All the timings in this table also apply when writing data with programmed I/O; CS* replaces DACK* and the DREQ*, TERMCT signals do not apply. A0-A3 times are the same as CS*.

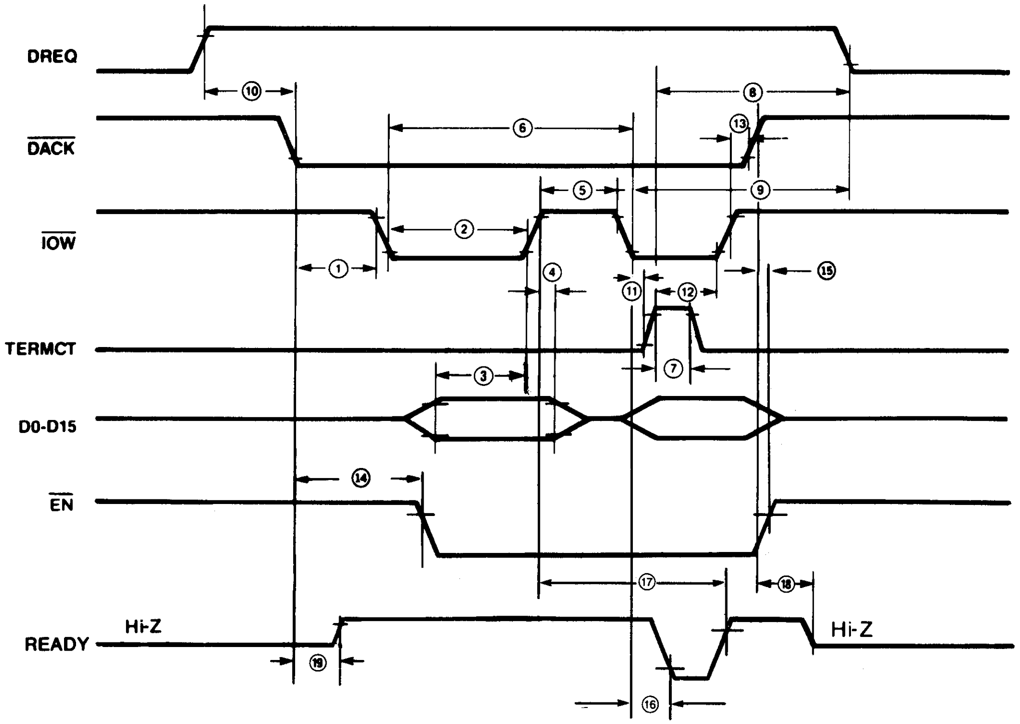


Figure I. DMA Write Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table J. DMA Read Cycle - BUSMODE = 1

Ref. #	Symbol	Description	Min.	Max.	Units
1	TDALRL	DACK* Setup Time	50		ns
2	TRLRH	IOR* Pulse Width[1]	100		ns
3	TRLDV	Data Delay Time[2]		100	ns
4	TRHDX	Data Hold Time	20		ns
5	TRHRL	IOR* High Time	200		ns
6	TRLRL	Read Cycle Time	300		ns
7	TTCHTCL	TERMCT Pulse Width	80		ns
8	TTCLDRL	DREQ Delay from TERMCT		100	ns
9	TDALDRL	DREQ Delay from IOR*		100	ns
10	TDRHDAL	DACK* Delay	0		ns
11	TRLTCH	TERMCT Assert Delay	20		ns
12	TTCLRH	IOR* Hold Time	80		ns
13	TRHDAH	DACK* Hold Time	0		ns
14	TRHDZ	Data Hi-Z Delay		50	ns
15	TDALENL	EN* Assert Delay		50	ns
16	TDALENL	EN* Deassert Delay		50	ns
17	TDALRYL	READY Deassert Delay		35	ns
18	TRLRYH	Read Recovery Time[3,4]	450	750	ns
19	TDAHRYZ	READY Delay to Hi-Z		50	ns
20	TDALRYV	DACK* Active to READY Valid		50	ns

NOTES:
1. IOR* must be asserted until READY is asserted and for a minimum of 100 ns.
2. This delay applies only if the 8005 is "ready" when IOR* is asserted, i.e., the first read of a burst or a read that occurs after the Ref. #18 TRLRYH has elapsed.
3. The BIU pre-fetches FIFO data. Thus, data is available immediately for the first read of any burst. Once the BIU detects a read operation, it begins fetching the next byte or word of data. This occurs during the Ref. #18 TRLRYH period. If a subsequent IOR* occurs within the Ref. #18 TRLRYH period, READY will deassert (Ref. #17 TDALRYL) and then assert after the FIFO data has been fetched (Ref. #18 TRLRYH). If the subsequent IOR* does not begin until Ref. #18 TRLRYH period has ended, then Ref. #18 has no meaning since READY does not deassert under this condition.
4. Subtract 200 ns if BUSSIZE = 0 (8 bit mode).

All the timings in this table also apply when reading data with programmed I/O: CS* replaces DACK* and the DREQ, TERMCT signals do not apply. A0-A3 times are the same as CS*.

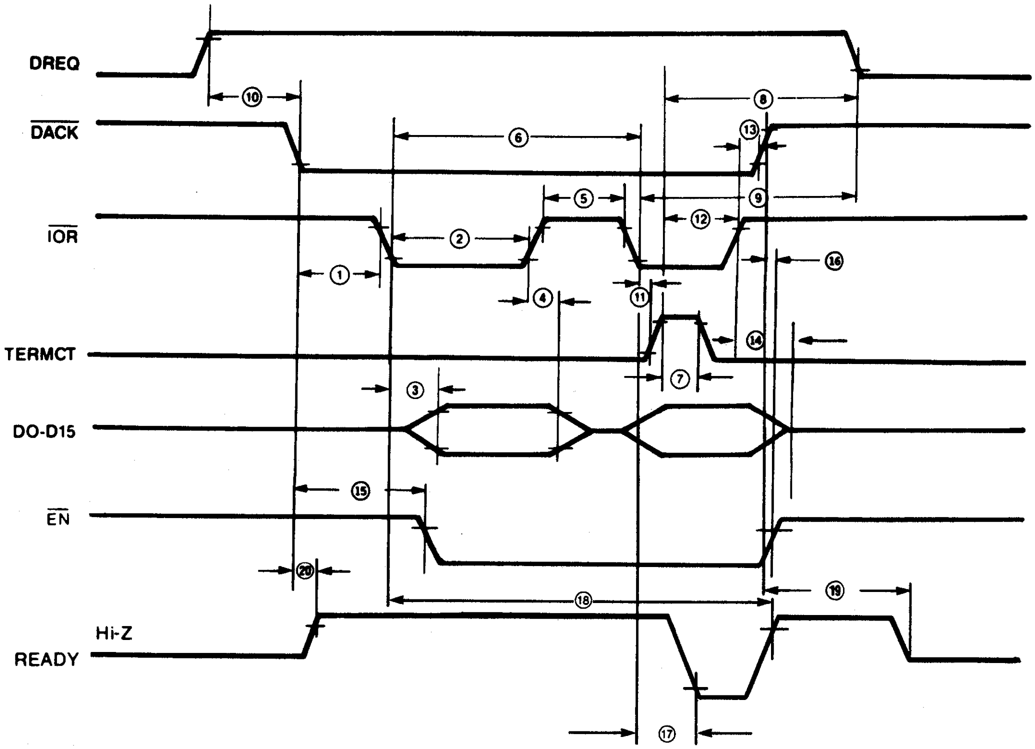


Figure J. DMA Read Cycle Timing Diagram — BUSMODE = 1

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table K. Local Buffer Read or Write Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRSLAX	Row Address Hold Time	150		ns
2	TAVRSL	Row Address Setup Time	5		ns
3	TRSHRSL	RAS* Pulse Width High	200		ns
4	TCSLAX	Column Address Hold Time	45		ns
5	TAVCSL	Column Address Setup Time	5		ns
6	TCSHCSL	CAS* Pulse Width – High	60		ns
7	TCSLCSH	CAS* Pulse Width – Low	110		ns
8	TAZGL	Address Hi-Z to G* Low Time	0		ns
9	TGLCH	G* Setup Time to G* Low	60		ns
10	TDVCSH	Data Setup to CAS*	15		ns
11	TCSHDX	Data Hold from CAS Deassert	0		ns
12	TCSHDZ	Data Hi-Z from CAS Deassert		40	ns
13	TAVAV	Read or Write Cycle Time a. Single Cycle b. Page Mode	 600 200		 ns ns
14	TDVWL	Data Setup Time	10		ns
15	TWLDX	Data Hold Time	60		ns
16	TWLWH	Write Pulse Width	60		ns
17	TCSLWL	CAS* Setup to W*	50		ns
18	TWLCSH	Write Setup Time	50		ns
19	TCSLWH	Write Hold Time	150		ns
20	TRSLRSL	RAS* Cycle Time	600		ns

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

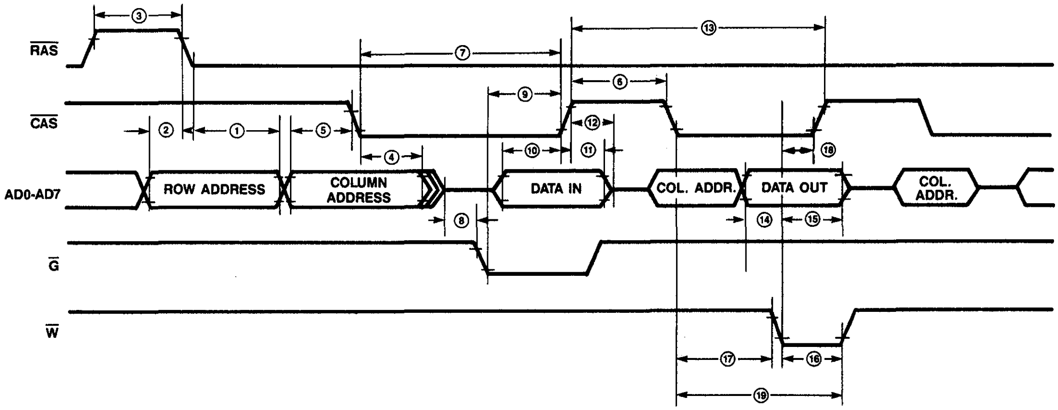


Figure K1. Local Dram Buffer Page-Mode Read and Write Cycle Timing Diagram

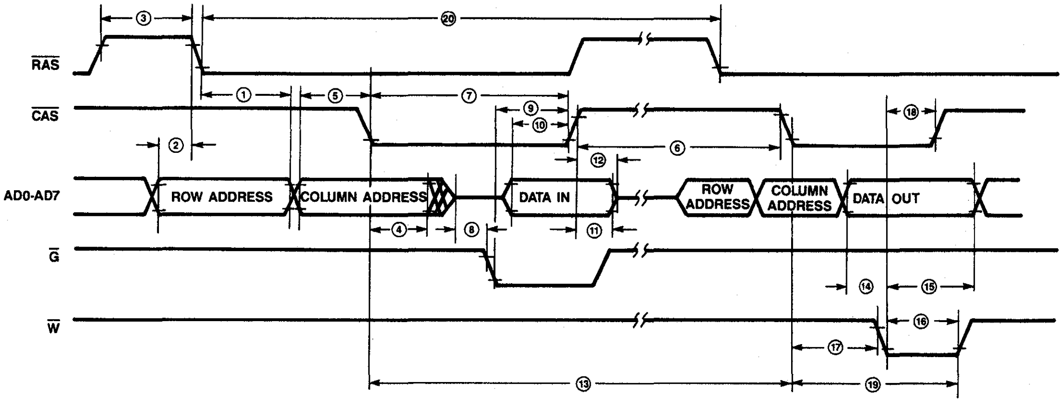


Figure K2. Local Dram Buffer Single Cycle Read and Write Cycle Timing Diagram

A.C. Characteristics (Assuming 20 MHz Input Master Clock) ***Over the operating V_{CC} and Temperature Range***

Table L. Local Buffer Refresh Cycle

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRSL	Address Setup Time to RAS*	5		ns
2	TRSLAX	Address Hold Time from RAS*	150		ns
3	TRSLRSH	RAS* Pulse Width	200		ns
4	TRSLRSL	RAS* Cycle Time	400		ns

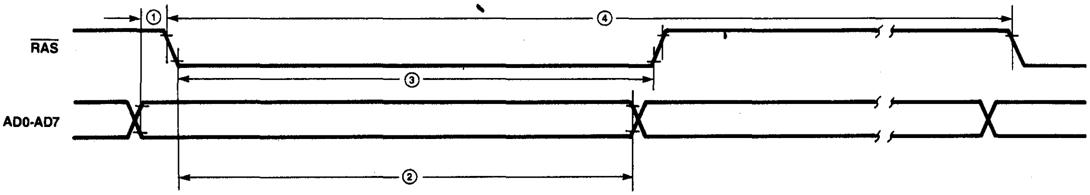


Figure L. Local Dram Buffer Refresh Cycle Timing Diagram

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table M. Serial Interface Timing

Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKH	T_{XC}/R_{XC} Cycle Time	95	1010	ns
2	TCKHCKL	T_{XC}/R_{XC} High Width	45		ns
3	TCKLCKH	T_{XC}/R_{XC} Low Width	45		ns
4	TCKLDV	T_{XD} Delay from T_{XC}		60	ns
5	TDVCKH	R_{XD} Setup to R_{XC}	30		ns
6	TCKHDX	R_{XD} Hold Time from R_{XC}	20		ns
7	TCKLTEH	T_{XEN} Delay from T_{XC}		60	ns
8	TCKLTEL	T_{XEN} Hold Time from T_{XC}	20		ns
9	TCSHCKH	CSN Setup to R_{XC}	20		ns
10	TCKHCSL	CSN Hold Time from R_{XC}	20		ns
11	TCHCL	COLL Pulse Width	Ref. 1+10		ns

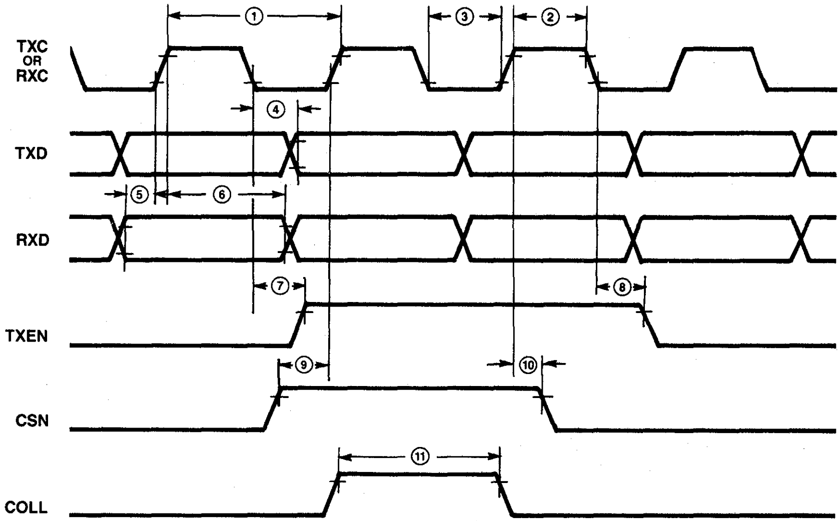


Figure M. Serial Transmit & Receive Interface Timing

A.C. Characteristics (Assuming 20 MHz Input Master Clock)
Over the operating V_{CC} and Temperature Range

Table N. Master Clock and Reset Timing

Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKL	CLK Pulse Width High	10	20	ns
2	TCKLCKH	CLK Pulse Width Low	20	30	ns
3	TCKHCKH	CLK Cycle Time	49.9	50.1	ns
4	TRSLRSH	Reset Pulse Width	10		µs

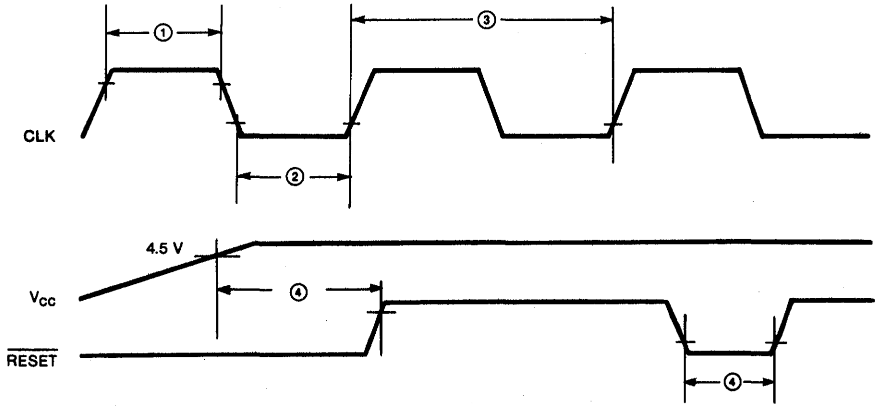


Figure N. Master Clock and Reset Timing

Ordering Information

PART NUMBER

N Q 8005

PRODUCT: 8005 ADVANCED EDLC
TEMPERATURE RANGE: Q = 0° TO 70°C
PACKAGE TYPE: N = 68 PIN PLCC

5

EEPLD

seeq

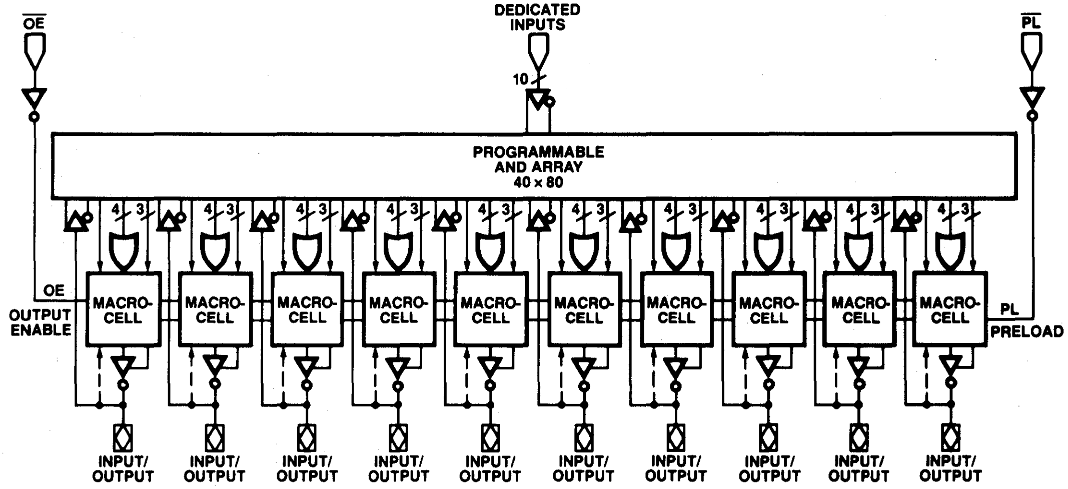
EEPLD
20RA10Z

October 1988

Features

- CMOS EEPLD with Zero Standby Power:
  - 10 μA Typical, 150 μA Maximum
- Operating Power Rises at Less Than 5 mA/MHz
- Propagation Delay: 35, 40 or 45 ns
- Asynchronous Architecture:
  - 10 Output Macro Cells with Individually Programmable Clocks, Preset and Reset Signals
- Individually Programmable and Global Output Enable
- Programmable Output Polarity
- Registers Can Be Bypassed Individually
- Preloadable Output Registers Facilitate Testing
- Quickly and Easily Reprogrammable in All Package Types
- 100 Reprogramming Cycles, Minimum
- Silicon Security Bit for Design Secrecy
- 100% Field Programming Yield
- 10 Years Data Retention Guaranteed
- Supported By: ABEL,* CUPL,* PALASM2,* PLDesigner*
- Programmed on Standard PAL* Device Programmers
- Space Saving 0.3" Wide 24-Pin Ceramic/Plastic DIP
- 28-Pin LCC and PLCC Packages in Development

Block Diagram



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*ABEL is a trademark of DATA I/O Corporation.

*PLDesigner is a trademark of Minc Inc.

*CUPL is a trademark of Logical Devices, Inc.

General Description

The 20RA10Z is functionally equivalent to the bipolar PAL20RA10. SEEQ's 20RA10Z consumes significantly less power than its bipolar equivalent: Standby power consumption is typically less than 10 µA; active power rises at less than 5 mA per MHz of operating frequency.

Bipolar devices can not be reprogrammed while UV erasable PLDs can be reprogrammed only in windowed, ceramic packages. Electrically erasable devices offer reprogrammability without constraints in all package types.

Reprogrammability reduces development costs and eliminates the risks involved in preprogramming production quantities. Systems can be updated quickly by reconfiguring the EEPLDs. Reprogrammability helps SEEQ to extensively test the entire device and offer 100% field programming yield.

The asynchronous 20RA10Z adds a new dimension to PAL device flexibility. Its unique architecture allows the designer to individually clock, set or reset each of the 10 output macro cells, and to enable/disable each output buffer individually.

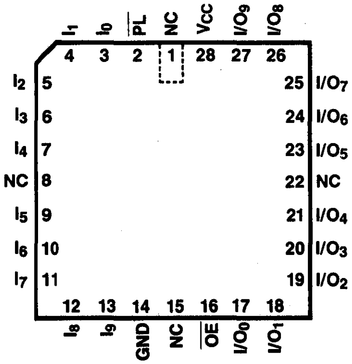
Functional Description

The 20RA10Z has ten dedicated input lines and 10 programmable I/O macrocells. The Registered Asynchronous (RA) macrocell is shown on page 3. Pin 1 of the EEPLD serves as global register preload, pin 13 (DIP) or pin 16 (LCC/PLCC) serves as global output enable. The exclusive-OR in every macro cell allows choosing between active high and active low output polarity, and ensures highest possible utilization of the AND-OR array.

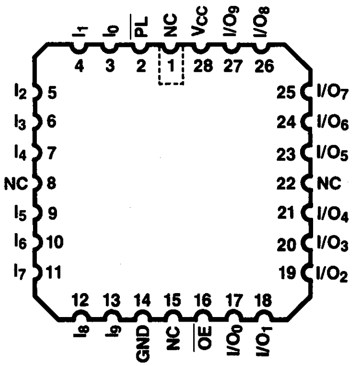
Third party software packages allow users to enter PLD designs on personal computers or engineering workstations. Common input formats are: Boolean Algebra, Truth-Tables, State Diagrams, Wave Forms or schematics. The software automatically converts such specifications into fuse patterns. These files, once downloaded to PAL programmers, configure PLDs according to the user's specifications.

Pin Configurations
(Top View)

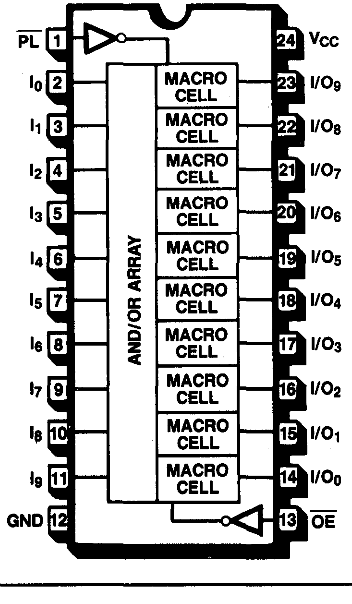
20RA10Z
PLCC PINOUT[1]



20RA10Z
LCC PINOUT[1]



20RA10Z
SLIM DIP PINOUT

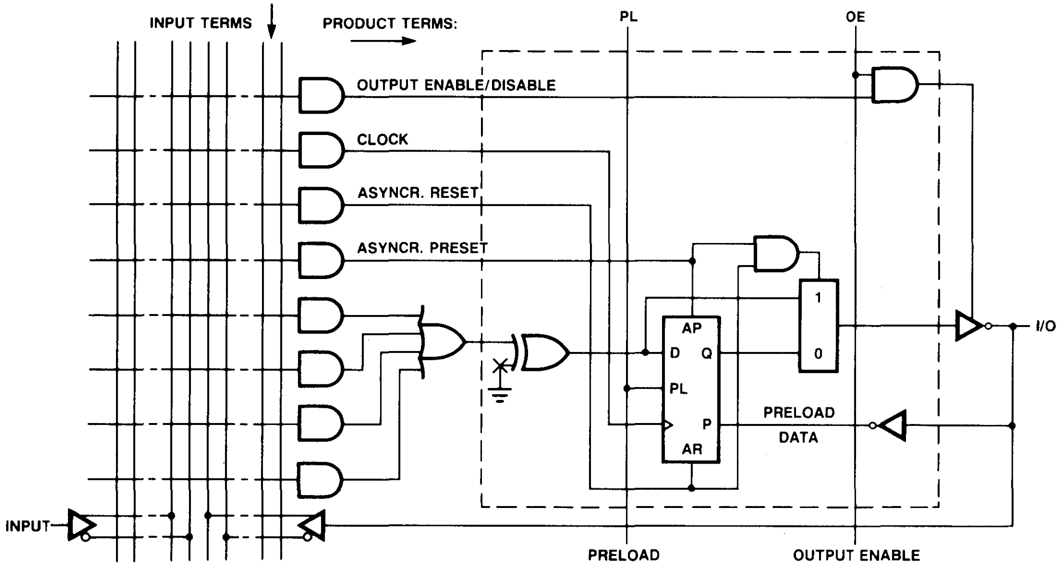


Pin Designations: I = Input
I/O = Input/Output
PL = Preload
OE = Output Enable
Vcc = Supply Voltage
GND = Ground
NC = No Connection

Note:

1. Surface Mount Packages pinout conform to JEDEC Standard.

RA Macrocell Configuration



Programmable Preset and Reset

In each macrocell, two product lines are dedicated to asynchronous preset and asynchronous reset. If the preset product term is HIGH, the Q output of the register becomes logic 1. If the reset product term is HIGH, the Q output of the register becomes a logic 0. The operation of the programmable preset and reset overrides the clock.

Programmable Clock

The clock input to each flip-flop comes from the programmable array, allowing any flip-flop to be clocked independently if desired.

Bypass Mode/Registered Mode

If both the preset and reset product terms are HIGH, the flip-flop is bypassed (Bypass Mode) and the output becomes combinatorial. Otherwise, the output is from the register (Registered Mode). Each output can be configured to be combinatorial or registered.

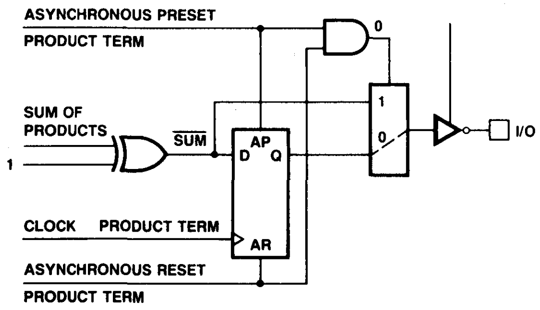
Programmable Polarity

The outputs can be programmed either active-LOW or active-HIGH. This is represented by the Exclusive-OR gate shown in the 20RA10Z logic diagram. When the output polarity bit is programmed, the lower input to the Exclusive-OR gate is HIGH, so the output is active-HIGH. Similarly when the output polarity bit is unprogrammed, the output is active-LOW. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

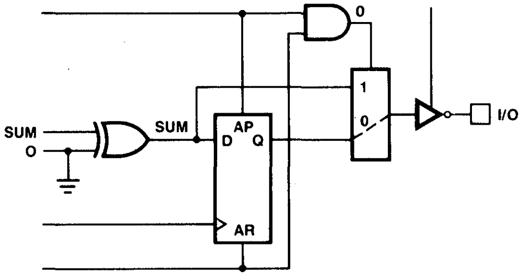
Remark: The output buffer inverts the sum of products signal.

Output Macrocell Configurations

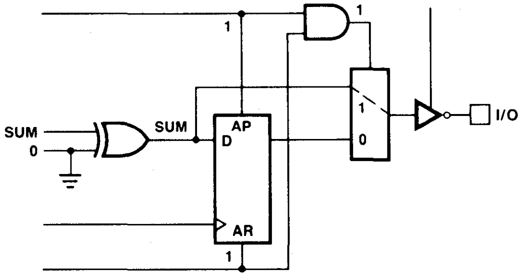
REGISTER OUTPUT/ACTIVE HIGH



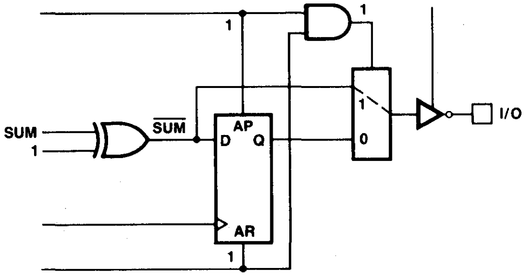
REGISTERED OUTPUT/ACTIVE LOW



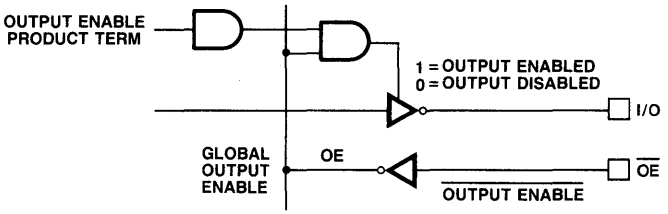
COMBINATORIAL OUTPUT/ACTIVE LOW
(REGISTER BYPASS MODE)



COMBINATORIAL OUTPUT/ACTIVE HIGH
(REGISTER BYPASS MODE)



Output Buffer with Individually Programmable and Global Output Enable



The device provides a product term dedicated to local output control. There is also a global output control pin. The output is enabled if both the global output control pin is LOW and the local output control product term is HIGH. If the global output control pin is HIGH, all outputs will be disabled. If the local output control product term is LOW, then that output will be disabled.

Register Preload

Register preload allows any arbitrary state to be loaded into the PAL device output registers. This allows complete logic verification, including states that are impossible or impractical to reach otherwise. To use the preload feature, first disable the outputs by bringing $\overline{OE}$ HIGH, and present the data at the output pins. A LOW level on the preload pin ($\overline{PL}$) will then load the data into the registers. (See Register Preload Waveform on page 10.)

OE Product Term	$\overline{OE}$ Pin	I/O
1	0	Indiv. output enabled
0	X	Indiv. output disabled*
X	1	All outputs disabled*

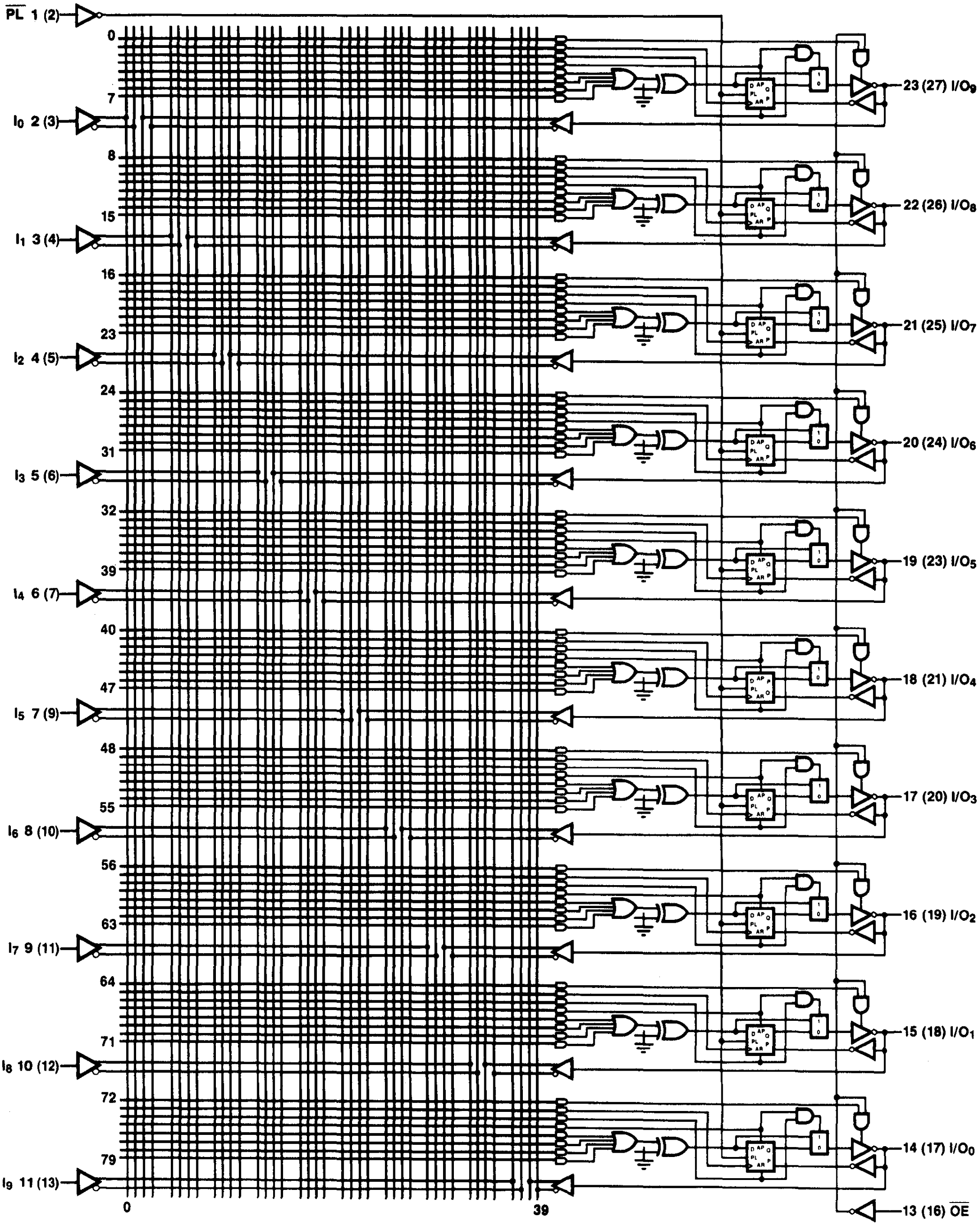
**Output pin(s) floating or used as input(s)*

Note: Floating outputs, as well as unused or floating inputs should be pulled HIGH or LOW. Otherwise noise, amplified through the feedback paths or input buffers, may constantly trigger the edge detection circuitry within the 20RA10Z and inhibit standby mode.

Security Bit

A security bit prevents copying of your proprietary design. When this bit is set, the verify data path in the PLD is disabled, making it impossible to copy your pattern. Since EEPLDs store patterns as electrical charges on floating polysilicon gates (and not in blown fuses, like other PLD technologies) it is not possible to determine the pattern by simply examining the die. A copy protected EEPLD can be reused after a block erase, which clears both the previously programmed pattern and the security bit at the same time.

EEPLD 20RA10Z Logic Diagram



PIN NUMBERS REFER TO DIP PINOUT (PLCC PINOUT)

Absolute Maximum Ratings

Supply voltage, V_{CC} . . . . −0.5 V to 7 V
DC input voltage, V_I . . . . −0.5 V to V_{CC} + 0.5 V
DC output voltage V_O . . . . −0.5 V to V_{CC} + 0.5 V
DC output source/sink
current per output pin, I_O . . . . ± 35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} . . . . ± 100 mA
Input diode current, I_{IK}:
$V_I < 0$ . . . . −20 mA
$V_I > V_{CC}$ . . . . + 20 mA
Output diode current, I_{OK}:
$V_O < 0$ . . . . −20 mA
$V_O > V_{CC}$ . . . . + 20 mA
Storage temperature . . . . −65°C to 150°C
Static discharge voltage . . . . > 2001 V
Latchup current . . . . > 100 mA
Ambient temperature
under bias . . . . −55°C to + 125°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (Q) Devices
Temperature (T_A)
Operating Free Air . . . . 0°C to + 75°C
Supply voltage, V_{CC} . . . . 4.75 V to 5.25 V
Industrial (E) Devices
Temperature (T_A)
Operating Free Air . . . . −40°C to + 85°C
Supply voltage, V_{CC} . . . . 4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics *over operating conditions unless otherwise specified.*

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{IL}	Low-level input voltage	Guaranteed Input Logical LOW Voltage for all Inputs[1]		0	0.8	V
V_{IH}	High-level input voltage	Guaranteed Input Logical HIGH Voltage for all Inputs[1]		2	V_{CC}	V
I_{IL}	Low-level input current	V_{CC} = Max.	V_I = GND	−1		μA
I_{IH}	High-level input current	V_{CC} = Max.	$V_I = V_{CC}$		1	μA
V_{OL}	Low-level output voltage	V_{CC} = Min.	I_{OL} = 8 mA		0.5	V
		V_{CC} = 5V	I_{OL} = 1 μA		0.05	
V_{OH}	High-level output voltage	V_{CC} = Min.	I_{OH} = −4.0 mA	3.80		V
		V_{CC} = 5V	I_{OH} = −1 μA	4.95		
I_{OZL}	Off-state output current	V_{CC} = Max.	V_O = GND[4]	−10		μA
I_{OZH}			$V_O = V_{CC}$[4]		10	μA
I_{CC}	Standby supply current[2]	I_O = 0 mA, V_I = GND or V_{CC}			150	μA
	Operating supply current[3]	f = 1 MHz, I_O = 0 mA, V_I = GND or V_{CC}			25	mA

Note: 1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Disabled output pins = V_{CC} or GND.
3. Frequency of any input. See graph page 11 for I_{CC} versus frequency.
4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OHZ}).

Capacitance

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input capacitance[1]	V_{IN} = 2.0V at f = 1.0 MHz V_{CC} = 5V T_A = 25°C	7	pF
C_{OUT}	Output capacitance[1]	V_{OUT} = 2.0V at f = 1.0 MHz V_{CC} = 5V T_A = 25°C	8	

Note: 1. Sampled but not 100% tested.

Switching Characteristics *over commercial operating range[1]*

Symbol	Parameter[2]		–35		–40[5]		–45[5]		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or feedback to output			35		40		45	ns
t_S	Setup time for input or feedback to clock		15		20		20		ns
t_H	Hold time		10		15		15		ns
t_{CO}	Clock to output or feedback[3]			35		40		45	ns
t_{WP}	Preload pulse width		25		30		30		ns
t_{SUP}	Preload setup time		20		25		25		ns
t_{HP}	Preload hold time		20		25		25		ns
t_{AP}	Asynchronous Preset to Registered Output[3]			40		45		45	ns
t_{APW}	Asynchronous Preset pulse width		25		25		30		ns
t_{APR}	Asyncronous Preset recovery time		15		15		15		ns
t_{AR}	Asynchronous Reset to Registered Output[3]			40		45		45	ns
t_{ARW}	Asynchronous Reset pulse width		25		25		30		ns
t_{ARR}	Asynchronous Reset recovery time		15		15		15		ns
t_{WL}	Width of clock	LOW	15		20		20		ns
t_{WH}		HIGH	15		20		20		ns
f_{MAX}	Maximum frequency	External feedback $1/(t_S + t_{CO})$	22.2		16.6		15.3		MHz
		No feedback $1/(t_{WL} + t_{WH})$	33.3		25		25		MHz
t_{PZX}	Common Enable to Output Buffer enabled			20		25		30	ns
t_{PXZ}	Common Enable to Output Buffer disabled			20		25		30	ns
t_{EA}	Input to Output Buffer enabled[4]			35		40		45	ns
t_{ER}	Input to Output Buffer disabled[4]			35		40		45	ns

Data Retention and Endurance

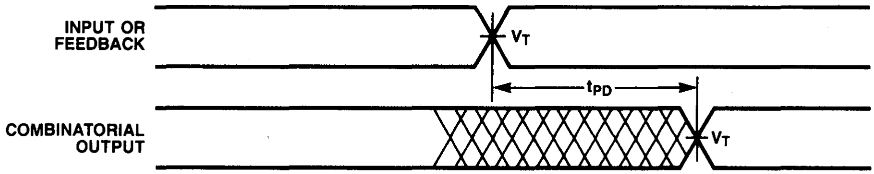
Symbol	Parameter	Value	Unit	Conditions
t_{DR}	Pattern data retention time	> 10	years	Max. storage temperature Mil-STD 883 Test Method 1008
N	Min. reprogramming cycles	100	cycles	Operating conditions

Notes:

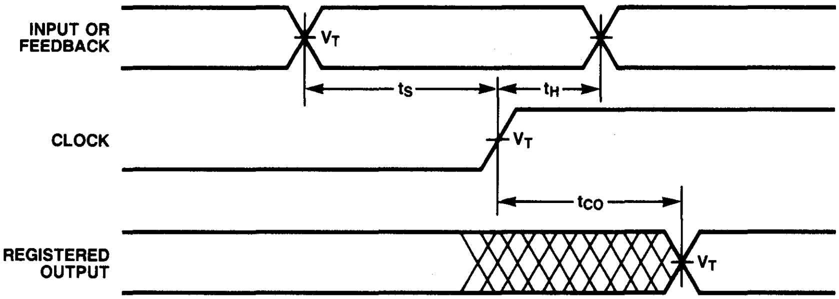
1. The 20RA10Z is designed for the full military operating range. Contact your nearest SEEQ representative for availability information and for specifications of military devices.
2. Test conditions are specified in table on page 11.
3. Minimum values of these parameters are guaranteed to be larger than the hold time t_H.
4. Equivalent functions to t_{PZX}/t_{PXZ} but using product term control.
5. The 20RA10Z-40, 20RA10Z-45 are available and specified for commercial and industrial operating conditions.

Remark: All specified input-to-output delays include the time it takes the input edge detection circuitry to activate the device (from standby mode into operating mode).

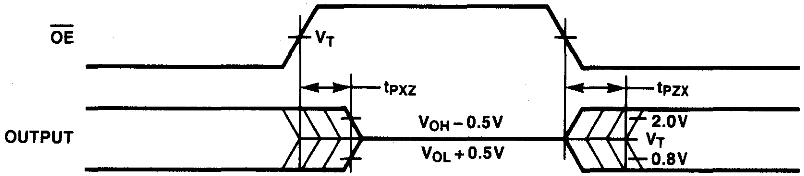
Switching Waveforms



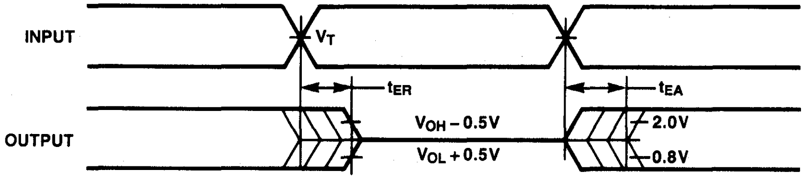
COMBINATORIAL OUTPUT (BYPASS MODE)



REGISTERED OUTPUT (REGISTERED MODE)

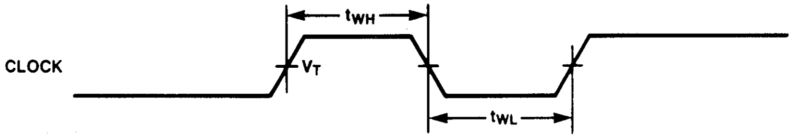


COMMON ENABLE ($\overline{OE}$) TO OUTPUT DISABLE/ENABLE

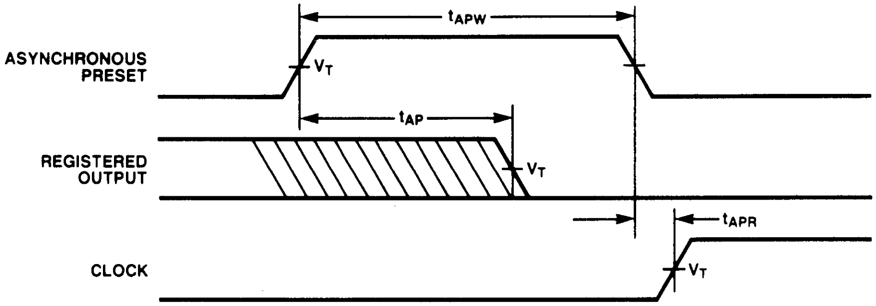


INPUT TO OUTPUT DISABLE/ENABLE

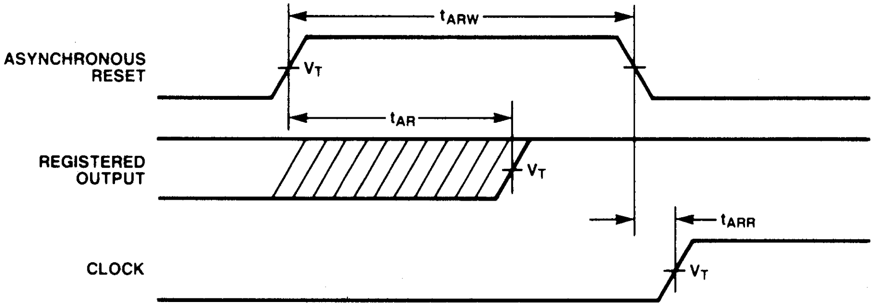
Switching Waveforms (continued)



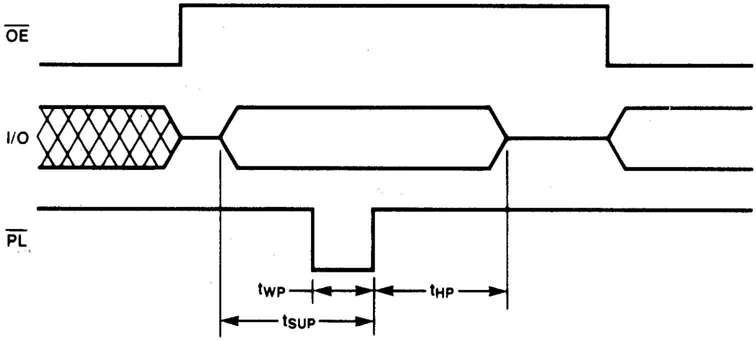
CLOCK WIDTH



ASYNCHRONOUS PRESET

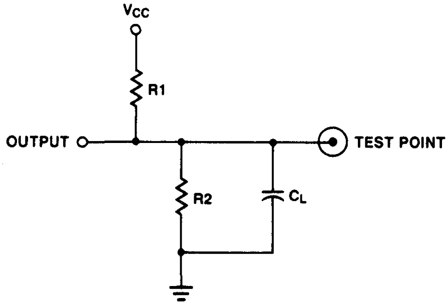


ASYNCHRONOUS RESET



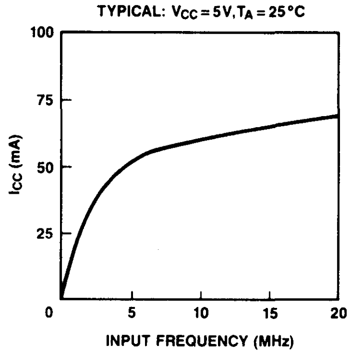
PRELOAD TIMING

Switching Test Load

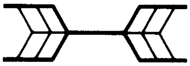
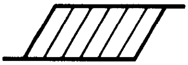


Specification	C_L	R_1	R_2	Measured Output Value
t_{IL}, t_{CO}	50pF	440Ω	190Ω	1.5V
t_{PZX}, t_{EA}	50pF	440Ω	190Ω	Z→H: 2.0V Z→L: 0.8V
t_{PXZ}, t_{ER}	5pF	440Ω	190Ω	H→Z: $V_{OH}-0.5V$ L→Z: $V_{OL}+0.5V$

I_{CC} Versus Frequency



Key to Timing Diagrams

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

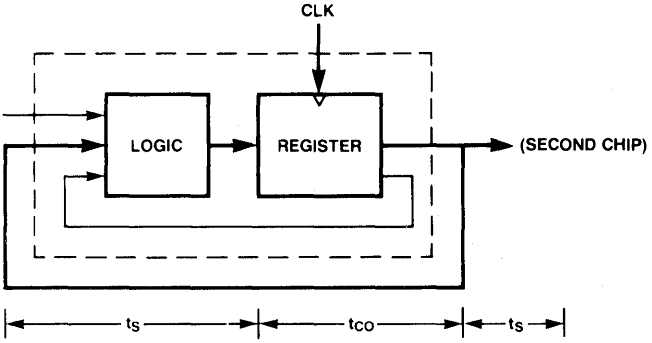
Notes:
1. $V_T=1.5V$
2. Input pulse amplitude 0V to 3.0V
3. Input rise and fall times 2 – 5ns typical

f_{MAX} Parameters

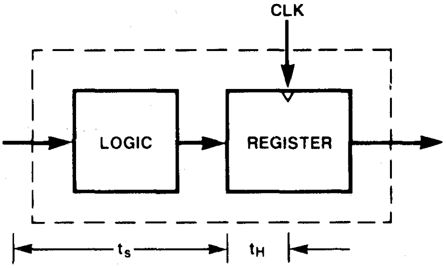
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified in this case for two types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "$f_{MAX,\ External\ Feedback}$."

The second type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the second f_{MAX}, designated "$f_{MAX,\ No\ feedback}$."



$f_{MAX,\ External\ Feedback}$; $1/(t_S + t_{CO})$



$f_{MAX,\ No\ Feedback}$; $1/(t_S + t_H)$ or $1/(t_{WH} + t_{WL})$

PLD Development

Development software assists the user in implementing a design in one or several PLDs. The software converts the users input into a device dependent fuse map in JEDEC format. The software packages listed below support the 20RA10Z EEPLD. For more information about PLD development software contact SEEQ Technology or the software vendor directly:

DATA I/O Corp.
10525 Willows Road, NE, P.O. Box 97046,
Redmont, WA 98073-9746
(800) 247-5700
Software offered: ABEL, PLD Test

Minc. Incorporated
1575 York Road, Colorado Springs, CO 80918
(719) 590-1155
Software offered: PLDesigner

Logical Devices, Inc.
1021 N.W. 65th Place, Fort Lauderdale, FL 33309
(305) 974-0967
Software offered: CUPL

PLD Programming

The 20RA10Z can be programmed on standard logic programmers. Previously programmed devices can be reprogrammed easily, using exactly the same procedure as required for blank EEPLDs. If the user wants to erase a 20RA10Z, but not program it to a new pattern, an empty JEDEC file should be loaded into the device programmer.

PLD Programmer Vendors

Adams MacDonald
800 Airport Road, Monterey, CA 93940
(408) 373-3607

DATA I/O Corp.
10525 Willows Road NE, P.O. Box 97046,
Redmont, WA 98073-9746
(800) 247-5700
PLD Programming equipment:
System 29A or 29B
Logic Pak™ 303A - V04
Adaptor 303-011A for 24 pin DIP
303-011B for 28 pin PLCC
Family Pinout Code for 20RA10Z: 9E/45

Digilec Inc.
22736 Vanowen, Canoga Park, CA 91307
(800) 367-8750; in CA: (818) 887-3755

Kontron Electronics Inc.
630 Clyde Ave., Mountain View, CA 94039
(415) 965-7020

Logical Devices Inc.
1201 N.W. 65th Place, Fort Lauderdale, FL 33309
(305) 974-0967

PROMAC
see Adams MacDonald

Stag Microsystems Inc.
1600 Wyatt Dr., Santa Clara, CA 95054
(408) 988-1118

Storey Systems
3201 N. Hwy 67, Suite E, Mesquite, TX 75150
(214) 270-4135

Structured Design
333 Cobalt Way, Suite 107, Sunnyvale, CA 94086
(408) 988-0725

Varix Corporation
1210 E. Campbell, Rd., Suite 100,
Richardson, TX 75081
(214) 437-0777

For more information about PLD programmers contact SEEQ Technology or the programmer vendor directly.

Logic Pak is a trademark of DATA I/O Corporation.

Ordering Information

P Q 20 RA 10 Z - 35

Package Type
- *P = Plastic DIP*
- *D = Ceramic DIP*
- *N = PLCC*
- *L = LCC*

Operating Range
- *Q = Commercial*
- *E = Industrial*
- *M = Military*

Number of Array Inputs

Output Type
- *R = Registered*
- *A = Asynchronous*

Number of Outputs

Zero Standby Power

Speed
- *$-35 = 35$ ns t_{PD}*
- *$-40 = 40$ ns t_{PD}*
- *$-45 = 45$ ns t_{PD}*

6 MILITARY

(Military and Industrial Temperature Range)

MIL-STD-883 Class B
Compliant Product Processing

SEEQ's Management emphasis is on Quality in products and performance, converting the results of the Technology evolution and innovations to the greatest benefit of our customers with an ever increased degree of system reliability, quality, and functionality.

SEEQ's comprehensive and interactive Quality program is designed to exceed military and customer expectations and requirements.

SEEQ's Quality program complies with MIL-STD-883 para 1.2.1 and military standards including MIL-Q-9858, MIL-I-45208, MIL-M-38510 Appendix A, MIL-STD-45662 and FED-STD-209. Fundamental building blocks of the Quality program are described below.

SEEQ's Military product flow (Chart 1) incorporates manufacturing processing, screening and controls. Controls as specified in Military procedures or customer specifications are an integral part of the processing flows in wafer fabrication, assembly product screening and test. (Table 1)

Quality Conformance Inspection

Quality conformance testing is performed per MIL-STD-883 para 1.2.1 and method 5005

Group A Tests

Group A—lot acceptance tests (see Table 2) are performed on each SEEQ inspection lot after completion of all screening per MIL-STD-883 method 5004 (see Table 1). Electrical test is per applicable SEEQ specification.

Group B—Tests (see Table 3)

Group B testing is performed by package type, lead finish and seal date code. The Group B covers all product manufactured using the same package type and lead finish assembled with the same week of seal per MIL-STD-883 method 5005 alternate Group B test.

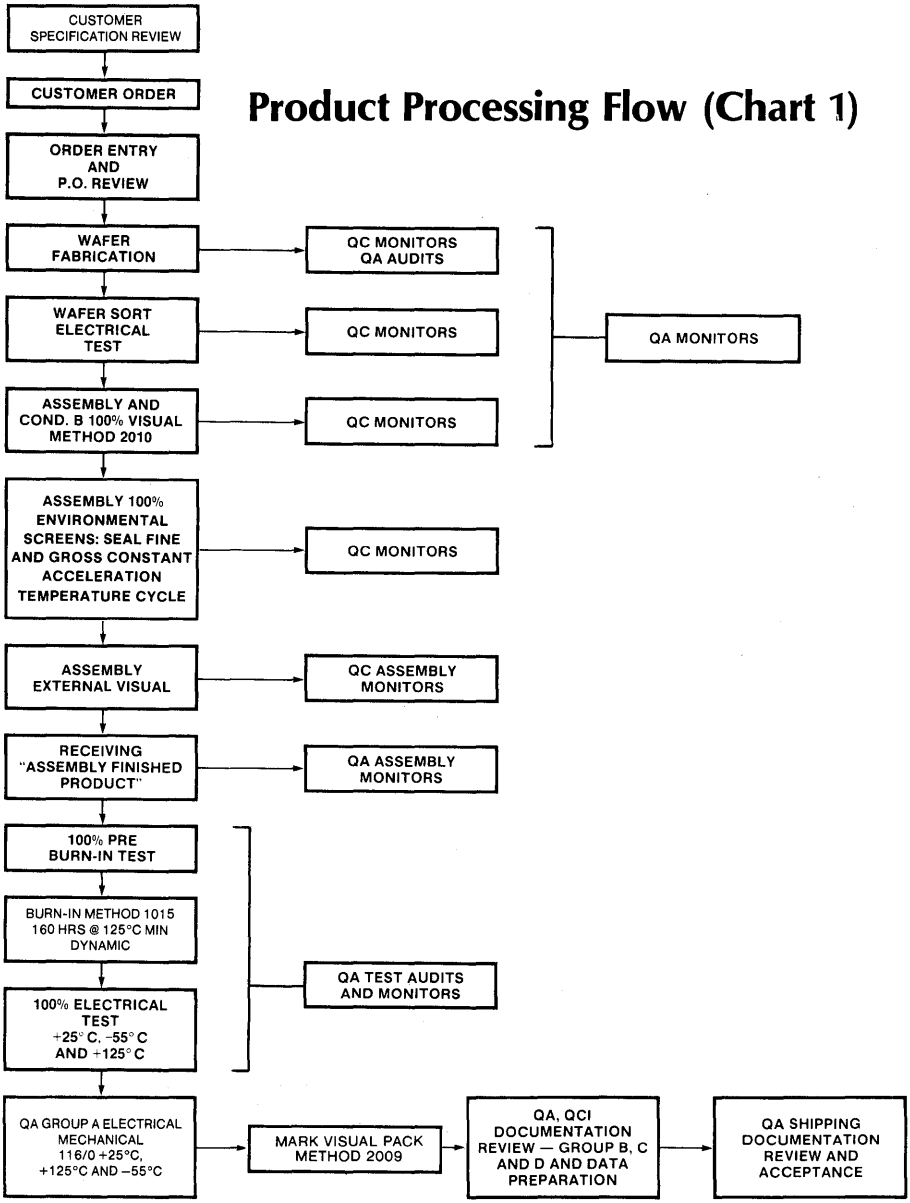
Group C Stresses — (see Table 4)

The product stressed, as part of Group C, is identical to that shipped or from the same process and product family. The seal date code of the product covered will be the same as or within the 51* consecutive weeks following the Group C seal date code. Electrical test is per applicable SEEQ specification.

Group D Stresses — (see Table 5)

Each package type and lead finish stressed, as part of Group D, is identical to that shipped. The seal date code of package lead finish covered will be the same as or within the 51* weeks following the Group D inspection lot code.

Product Processing Flow (Chart 1)



SEEQ Screens & Tests (Table 1)

Military Screen	MIL-STD Method	Reqmt.
Internal Visual	2010, Test Condition B	100%
Temperature Cycling	1010, Test Condition C	100%
Constant Acceleration	2001, Y_1 Orientation Only	100%
Seal (A) Fine (B) Gross	1014 Condition A Condition C	100%
Visual Inspection		100%
Initial (Pre-Burn-In-Test) Electrical Parameters	Per Applicable SEEQ Specification	100%
Burn-In Stress	1015, Dynamic @ 125°C MIN	100%
(Post-Burn-In—Test) Electrical Parameters Tested within 96 Hrs.	Per Applicable SEEQ Specification	100%
Percent Defective Allowable (PDA) Calculation	5%	100%
Final Electricals	Per Applicable SEEQ Specification	100%
Qualification or Quality Conformance Inspection Test Sample Selection		
External Visual	2009	100%

Group A Electrical Test per applicable SEEQ Specification (Table 2)

Subgroup	Description	Sample
1	Static Test @ 25°C	116/0
2	Static Test @ Max Rated Operating Temperature	116/0
3	Static Test @ Min Rated Operating Temperature	116/0
7	Functional Test @ 25°C	116/0
8A	Functional Test @ Max Rated Operating Temperature	116/0
8B	Functional Test @ Min Rated Operating Temperature	116/0
9	Switching Test @ 25°C	116/0
10	Switching Test @ Max Rated Operating Temperature	116/0
11	Switching Test @ Min Rated Operating Temperature	116/0
4	Dyanamic Test Capacitance Testing	Performed on initial qualification and design changes that may affect capacitance

Group B Tests (Table 3)

Test	Test Method	Test Conditions	Quality Level/ Accept Number
Subgroup 2 Resistance to Solvents	2015		4 Devices (no failures)
Subgroup 3 Solderability	2003	Soldering Temperature of +245°C Plus or Minus 5°C	LTPD 10 = 1
Subgroup 5 Bond Strength Ultrasonic or Wedge	2011	Test Condition C or D	LTPD 15 = 1

Subgroups 1, 4, 6, 7 and 8 have been deleted, the remaining Subgroups have not been renumbered, per MIL-STD-883, Method 5005.

Group C Stresses (Table 4)

Test	Test Method	Test Conditions	Quality Level/ Accept Number
Subgroup 1 Steady-State Life Test	1005	Condition D, Equivalent to 1000 hours @ 125°C	LTPD 5 = 1
End-Point Electrical		Per SEEQ Specification	

Group D Stresses (Table 5)

Test	MIL-STD Test Method	Test Conditions	Minimum Quality Level/ Accept Number
Subgroup 1			
Physical Dimensions	2016	Per SEEQ Outline Drawing	LTPD 15 = 1
Subgroup 2			
Lead Integrity	2004		LTPD 15 = 1
Hermeticity, Fine and Gross	1014		
Subgroup 3			
Thermal Shock	1011	−65°C Condition B, 15 Cycles Minimum	LTPD 15 = 1
Temperature Cycling	1010	−65°C Condition C, 100 Cycles Minimum	
Moisture Resistance	1004	90% Minimum Relative Humidity	
Hermeticity, Fine and Gross	1014		
Visual Examination	1004	Per SEEQ Specification	
End-Point Electrical Parameters	1010	Per SEEQ Specification	
Subgroup 4			
Mechanical Shock	2002	Condition B	LTPD 15 = 1
Vibration, Variable Frequency	2007	Condition A	
Constant Acceleration	2001	Y_1 Orientation	
Hermeticity			
Fine	1014	Condition A	
Gross	1014	Condition C	
Visual Examination	2009	Per SEEQ Specification	
End-Point Electrical Parameters		Per SEEQ Specification	
Subgroup 5			
Salt Atmosphere	1009	Condition A	LTPD 15 = 1
Hermeticity			
Fine	1014	Condition A	
Gross	1014	Condition C	
Visual Examination	1009	Per SEEQ Specification	
Subgroup 6			
Internal Wafer Vapor	1018	5,000 ppm Maximum Water Content at T = +100°C	3 Devices, 0 Failures or 5 Devices, 1 Failure
Subgroup 7			
Adhesion of Lead Finish	2025	Bend 90°, Inspect at 10x to 20x Magnification	LTPD 15 = 1
Subgroup 8			
Lid Torque	2024	As Applicable to Glass-Frit Packages	5 Devices, 0 Failures

M52B13/M52B13H
(Military Temperature Range)

E52B13/E52B13H
(Extended Temperature Range)

16K Electrically Erasable PROM

October, 1988

Features

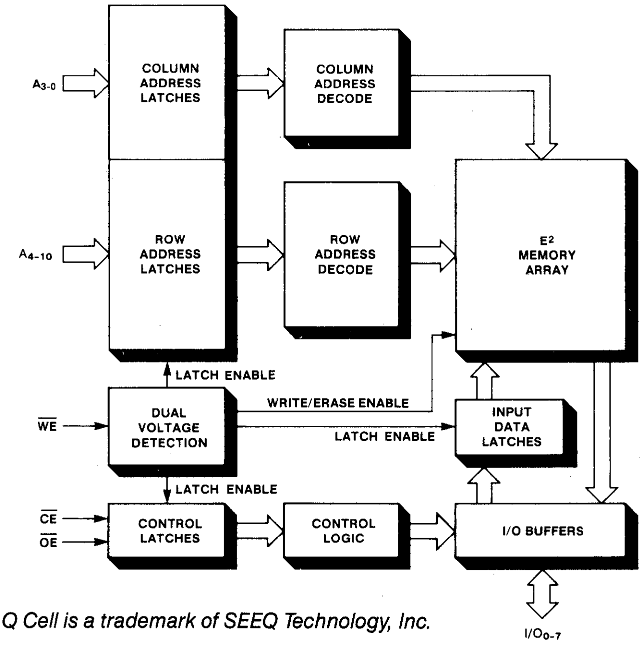
- **Military and Extended Temperature Range**
  - **M52B13/M52B13H: −55° to 110°C WRITE −55° to 125°C READ**
  - **E52B13/E52B13H: −40° to 85°C**
- **Input Latches**
- **5V ± 10% 2K X 8 EEPROM**
- **1 ms (52B13H) or 9 ms Byte TTL Erase/Byte Write**
- **10,000 Erase/Write Cycles per Byte Minimum**
- **Chip Erase and Byte Erase**
- **DiTrace™**
- **Fast Read Access Time — 250 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte Wide Memory Pinout**
- **Intel M2816/2816A E² Compatible**

Description

SEEQ's M52B13 and M52B13H are 2048 x 8 bit, 5 volt electrically erasable programmable read only memories (EEPROMs) which are specified over the military and extended temperature range respectively. They have input latches on all addresses, data, and control (chip and output) enable lines. In addition, for applications requiring fast byte write time (1 msec), an M52B13H and E52B13H are also available. Data is latched and electrically written by a TTL (or a 21V pulse) on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written a minimum of 10,000 times.

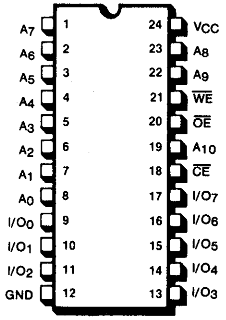
The M52B13 is compatible to the Intel M2816/2816A and SEEQ's M5213. For system upgrades of these older generation EEPROMs, the M52B13 is specified over the military temperature range and has an access time of 250 ns. The M52B13 is available in a 24 pin cerdip package.

Block Diagram



Pin Configuration

M52B13/E52B13



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O0-7	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

Q Cell is a trademark of SEEQ Technology, Inc.

These EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instruments/machines, programmable industrial controllers, and an assortment of other systems. Designing the EEPROMs into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is at TTL high, and TTL highs (logical 1's) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation EEPROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detection circuit which allows either a TTL low or 21V signal to be applied to $\overline{WE}$ to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of $\overline{WE}$.

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10 ms.

A characteristic of all EEPROMs is that the total number of write and erase cycles is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs. Data is available, t_{CE} time after Chip Enable is applied or t_{AA} time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

DiTrace®

SEEQ's family of EEPROMs incorporate a DiTrace field. The DiTrace feature is a method for storing production flow information to the wafer level in an extra column of EEPROM cells. As each major manufacturing operation is performed the DiTrace field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

DiTrace is a registered trademark of SEEQ Technology, Inc.

Table 1. Mode Selection ($V_{CC} = 5V \pm 10\%$)

PIN Mode	$\overline{CE}$ (18)	$\overline{OE}$ (20)	$\overline{WE}$ (21)	I/O (9-11, 13-17)
Read[1]	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby[1]	V_{IH}	Don't Care	V_{IH}	High Z
Byte Erase[2]	V_{IL}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase[2]	V_{IL}	V_{OE}	V_{IL}	$D_{IN} = V_{IH}$
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	High Z

NOTES:

1. $\overline{WE}$ may be from V_{IH} to 6V in the read and standby mode.
2. $\overline{We}$ may be at V_{IL} (TTL $\overline{WE}$ Mode) or from 15 to 21V (High Voltage $\overline{WE}$ Mode) in the byte erase, byte write, or chip erase mode of the 52B13/52B13H.

Power Up/Down Considerations

SEEQ's "52B" E^2 family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Under the above conditions, the outputs are in a high impedance state.

Absolute Maximum Stress Ratings*

Temperature
Storage .... −65°C to +150°C
Under Bias .... −65°C to +135°C
All inputs or Outputs with
Respect to Ground .... +6V to −0.3V
WE during Writing/Erasing
with Respect to Ground .... +22.5 to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability*

Recommended Operating Conditions

V_{CC} Supply Voltage	5 V ± 10%
Temperature Range: M52B13/M52B13H (Case)	WRITE −55° to +110°C READ −55° to +125°C
E52B13/E52B13H (Ambient)	−40° to +85°C

NOTE:
1. Characterized. Not tested.

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

D.C. Operating Characteristics During Read or Write/Erase (Over operating V_{CC} and temperature range.)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I_{IN}	Input Leakage Current			10	µA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	µA	$V_{OUT} = V_{CC}$ Max.
I_{WE}	Write Enable Leakage Read Mode			10	µA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	µA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode			1.5	mA	$\overline{WE} = 22V$, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode			1.5	mA	$\overline{WE} = 22V$, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	µA	$\overline{WE} = V_{IL}$
	Chip Erase—High Voltage Mode			1.5	mA	$\overline{WE} = 22V$
I_{CC1}	V_{CC} Standby Current		15	35	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	90	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2		$V_{CC} + 1$	V	
V_{WE}	$\overline{WE}$ Read Voltage	2		$V_{CC} + 1$	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA
V_{OE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	$I_{OE} = 10$ µA

NOTE:
1. Nominal values are for $T_A = 25°C$ and $V_{CC} = 5.0$ V.

A.C. Operating Characteristics During Read

Symbol	Parameter	Device Number Extension	M52B13/ M52B13H		E52B13/ E52B13H		Units	Test Conditions
			Min.	Max.	Min.	Max.		
t_{AA}	Address Access Time	–250		250		250	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		–300		300		—	ns	
		–350		—		350	ns	
t_{CE}	Chip Enable to Data Valid	–250		250		250	ns	$\overline{OE} = V_{IL}$
		–300		300		—	ns	
		–350		—		350	ns	
t_{OE}[1]	Output Enable to Data Valid	–250		90		90	ns	$\overline{CE} = V_{IL}$
		–300		90	—	—	ns	
		–350	—	—		110	ns	
t_{DF}[2]	Output Enable to High Impedance	–250	0	70	0	70	ns	$\overline{CE} = V_{IL}$
		–300	0	70	—	—	ns	
		–350	—	—	0	80	ns	
t_{OH}	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/C_{OUT}[3]	Input Capacitance	All		10		10	pF	$V_{IN} = 0$ V for C_{IN}, $V_{OUT} = 0$ V for C_{OUT}, $T_A = 25°C$
	Output Capacitance	All		10		10	pF	

Equivalent A.C. Test Conditions [6]

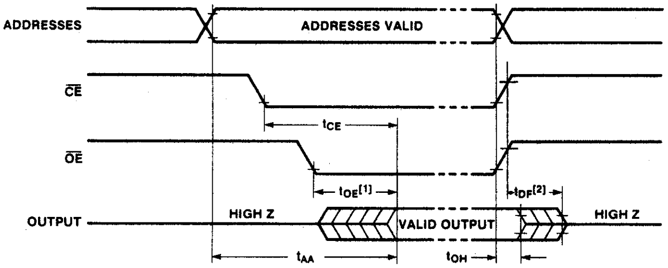
Output Load: 1 TTL gate and $C_L = 100$ pF

Input Rise and Fall Times: ≤ 20ns

Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

READ TIMING



NOTES:
1. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
2. t_{DF} is specified from $\overline{OE}$ oor $\overline{CE}$, whichever occurs first.
3. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
4. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
5. The Write Recovery Time, t_{wr}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.
6. These are equivalent test conditions and actual test conditions are dependent on the tester.

A.C. Operating Characteristics During Write/Erase (Over the operating V_{CC} and temperature range)

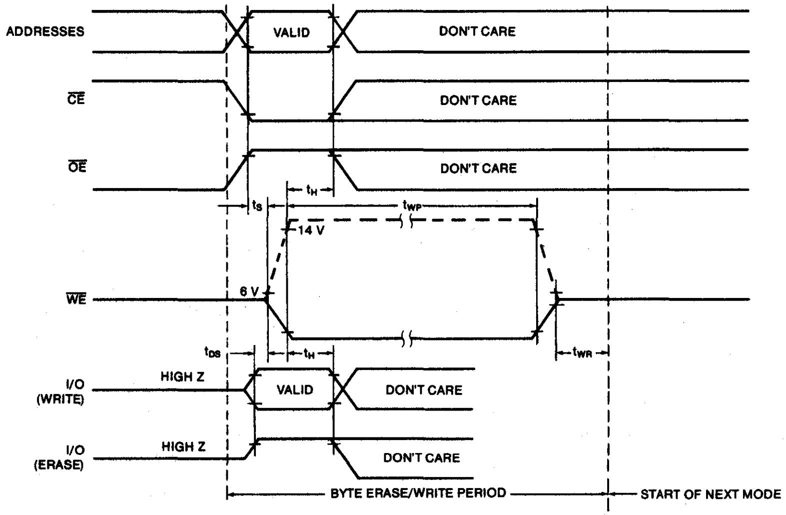
Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{\text{CE}}$, $\overline{\text{OE}}$ or Address Setup to $\overline{\text{WE}}$	50		ns
t_{DS}	Data Setup to $\overline{\text{WE}}$	15		ns
t_H[4]	$\overline{\text{WE}}$ to $\overline{\text{CE}}$, $\overline{\text{OE}}$, Address or Data Change	50		ns
t_{WP}	Write Enable ($\overline{\text{WE}}$) Pulse Width Byte Modes — M52B13/E52B13	9		ms
	Byte Modes — M52B13H /E52B13H	1		
t_{WR}[5]	$\overline{\text{WE}}$ to Mode change $\overline{\text{WE}}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{\text{WE}}$ to Start of Read Cycle		2	µs

52B13/52B13H High Voltage Write Specifications

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications, including the TTL W/E mode.

Symbol	Function/Parameter	M52B13 E52B13 Min.	M52B13 E52B13 Max.	M52B13H E52B13H Min.	M52B13H E52B13H Max.	Units
t_{WP}	Write Enable Pulse Width Byte Write/Erase	9	20	1	20	ms
	Chip Erase	9	20	9	20	ms
V_{WE}	$\overline{\text{WE}}$ Write/Erase Voltage High Voltage Mode	14	22	14	22	V

BYTE ERASE OR BYTE WRITE TIMING

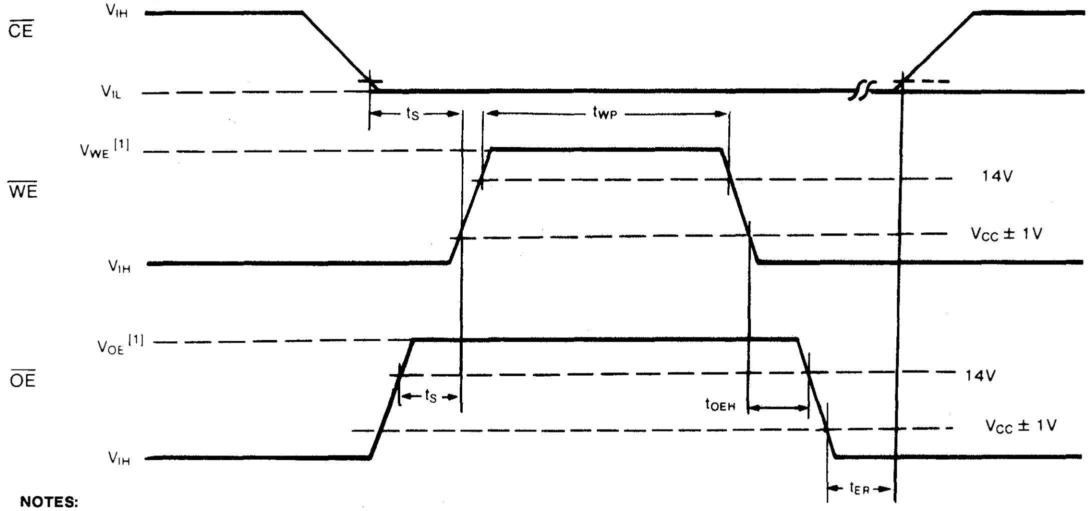


Notes: See AC notes

Chip Erase Specifications

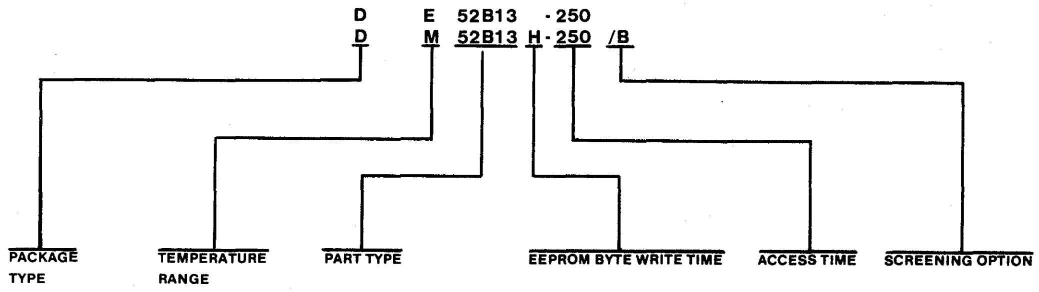
Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ Setup to $\overline{WE}$	1		µs
t_{OEH}	$\overline{OE}$ Hold Time	1		µs
t_{WP}	WE Pulse Width	10		ms
t_{ER}	Erase Recovery Time		10	µs

Chip Erase Timing



NOTES:
1. V_{WE} and V_{OE} can be from 15V to 21V in the high voltage mode for chip erase on 52B13.

Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	EEPROM BYTE WRITE TIME	ACCESS TIME	SCREENING OPTION
D - CERAMIC DIP L - LCC	M - Military E - Extended	2K x 8 EEPROM	(Blank) - Standard Write Time H - Fast Write Time	250 - 250 ns 300 - 300 ns 350 - 350 ns	/B - MIL 883 CLASS B Screened

M52B33/M52B33H
E52B33/E52B33H

64K Electrically Erasable PROM

October, 1988

Features

- **Full Military and Extended Temperature Range**
  - **M52B33/M52B33H: −55° to 125°C**
  - **E52B33/E52B33H: −40° to 85°C**
- **10,000 Write Cycles/Byte Over Temperature**
- **Input Latches**
- **5 V ±10% V_{CC}**
- **1 ms (52B33H) or 9 ms (52B33) TTL Byte Erase/Byte Write**
- **Power Up/Down Protection**
- **DiTrace®**
- **Fast Read Access Time—250 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte-Wide Memory Pinout**

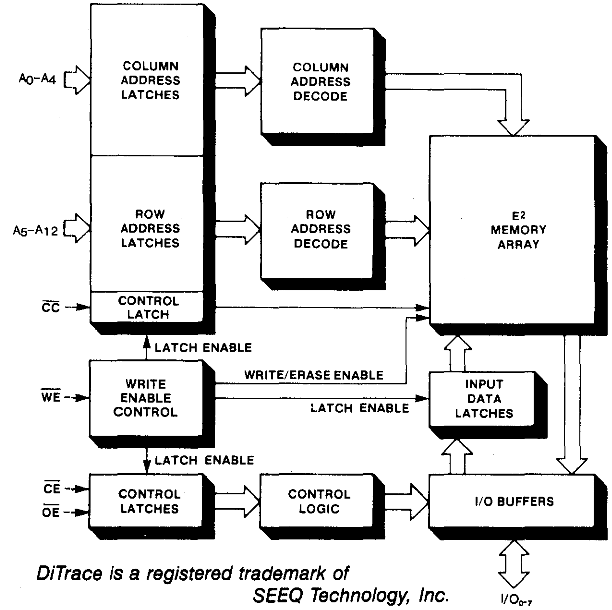
Description

SEEQ's M52B33 and E52B33 are 8192 x 8, 5V electrically erasable programmable read only memories (EEPROMs) which are specified over the military and extended temperature range respectively. They have input latches on all addresses, data, and control (chip and output) lines. In addition, for applications requiring fast byte write time (1 ms), an E52B33H and M52B33H are available. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written, there is no limit to the number of times data may be read. The erasure time is under 10 ms, and each byte may be erased and written a minimum of 10,000 times.

The E/M52B33 is available in a 28 pin cerdip or 32 pin leadless chip carrier. The pin configuration is to the JEDEC approved byte wide memory pinout for these two types of packages. These EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the alteration of opening software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other

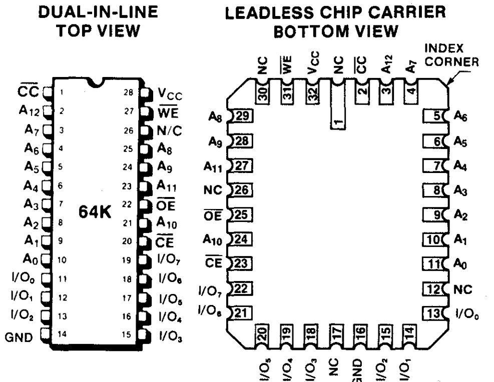
(continued on page 2)

Block Diagram



DiTrace is a registered trademark of SEEQ Technology, Inc.

Pin Configurations


DUAL-IN-LINE TOP VIEW

LEADLESS CHIP CARRIER BOTTOM VIEW

Pin Names

A_0–A_4	ADDRESSES - COLUMN (LOWER ORDER BITS)
A_5–A_{12}	ADDRESSES - ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
$\overline{CC}$	CHIP CLEAR
N/C	NO CONNECT

systems. Designing the EEPROMs into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

Device Operation

SEEQ E/M52B33 and E/M52B33H have six modes of operation (see Table 1) and require only TTL inputs to operate these modes.

To write into a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then brought to a TTL low level to latch all the inputs. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H performs the same as the E/M52B33 except that the byte erase/byte write time has been enhanced to 1 ms.

A characteristic of all EEPROMs is that the total number of write and erase cycles is not unlimited. The E/M52B33 is designed for applications requiring up to 10,000 write and erase cycles per byte over the temperature range. The write and erase cycling characteristics are completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs. Data is available, t_{CE} time after Chip Enable is applied or t_{AA} time from the addresses. System power may be reduced by placing the device into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

DiTrace®

SEEQ's family of EEPROMs incorporates a DiTrace field. The DiTrace feature is a method for storing production flow information in an extra row of EEPROM cells. As each major manufacturing operation is performed the DiTrace field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Chip Clear

Certain applications may require all bytes to be erased simultaneously. See A.C. Operating Characteristics for TTL chip erase timing specifications.

Power Up/Down Considerations

SEEQ's "52B" E^2 family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

Mode Selection (Table 1)

Mode \ Function (Pin)	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)
Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	Don't Care	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	$D_{IN} = V_{IH}$
Byte Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	D_{IN}
Chip Clear	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL} or V_{IH}
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	Don't Care	High Z

NOTE:
[1] Characterized. Not tested.

Absolute Maximum Stress Rating*

Temperature
Storage .... −65°C to +150°C
Under Bias .... −65°C to +135°C
All inputs or Outputs with
Respect to Ground .... +6V to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

Recommended Operating Conditions

V_{CC} Supply Voltage	5 V ± 10%
Temperature Range: M52B33/M52B33H (Case)	−55° to + 125°C
E52B33/E52B33H (Ambient)	−40° to + 85°C

DC Operating Characteristics During Read or Erase/Write

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Nom.[1]	Max.	Unit	Test Condition
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max
I_{WE}	Write Enable Leakage Read Mode W/E Mode			 10 10	 μA μA	 $\overline{WE} = V_{IH}$ $\overline{WE} = V_{IL}$
I_{CC1}	V_{CC} Standby Current		15	50	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage	−0.1		0.8	V	
V_{IH}	Input High Voltage	2		$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

NOTE: See next page for notes.

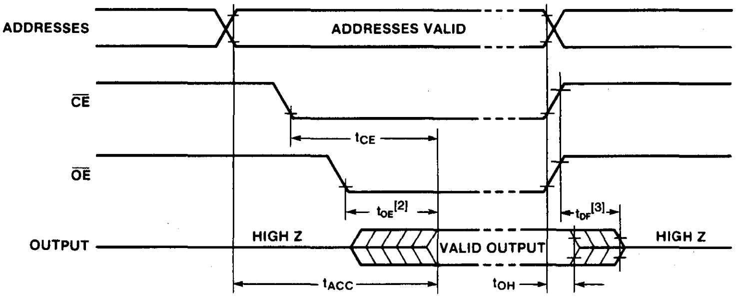
MILITARY

A.C. Operating Characteristics During Read

(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	M52B33 M52B33H Min.	M52B33 M52B33H Max.	E52833 E52833H Min.	E52833 E52833H Max.	Unit	Test Conditions
t_{AA}	Address Access Time	–250 –300		250 300		250 300	ns ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid	–250 –300		250 300		250 300	ns ns	$\overline{OE} = V_{IL}$
t_{OE}[2]	Output Enable to Data Valid	–250 –300		90 90		90 90	ns ns	$\overline{CE} = V_{IL}$
t_{DF}[3]	Output Enable to High Impedance	–250 –300	0 0	70 70	0 0	70 70	ns ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
C_{IN}/ C_{OUT}[4]	Input/Output Capacitance	All		10		10	pF	$V_{IN} = 0$ V for C_{IN}, $V_{OUT} = 0$ V for C_{OUT}, $T_A = 25°C$

Read Cycle Timing



NOTES:

1. Nominal values are for $T_A = 25°C$ and $V_{CC} = 5.0$ V.
3. $\overline{OE}$ may be delayed to $t_{AA} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{AA}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
5. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
5. After t_H, hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, $\overline{CC}$, Address and Data are latched and are "Don't Cares" until t_{WR}, Write Recovery Time, after the trailing edge of $\overline{WE}$.
6. The Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.
7. These are equivalent test conditions and actual test conditions are dependent on the tester.

A.C. Operating Characteristics During Write/Erase

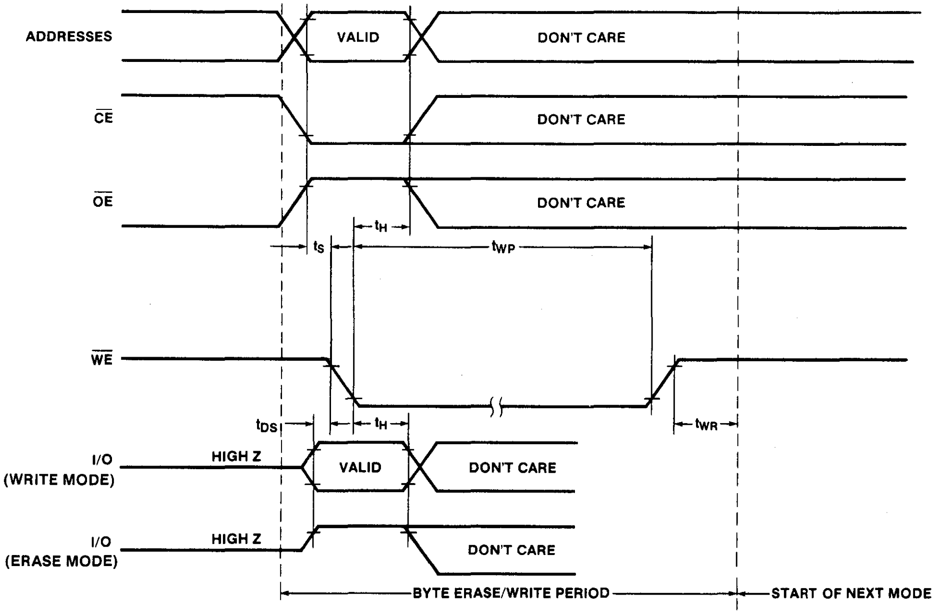
(Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits		Units
		Min.	Max.	
t_S	$\overline{CE}$, $\overline{OE}$ or Address Setup to $\overline{WE}$	50		ns
t_{DS}	Data Setup to $\overline{WE}$	15		ns
t_H[5]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, Address or Data Change	50		ns
t_{WP}	Write Enable, ($\overline{WE}$) Pulse Width			
	Byte Modes — M52B33/E52B33	9		ms
	Byte Modes — M52B33H	1		ms
t_{WR}[6]	$\overline{WE}$ to Mode Change			
	$\overline{WE}$ to Next Byte Write/Erase Cycle	50		ns
	$\overline{WE}$ to Start of a Read Cycle	1		μs

Equivalent A.C. Test Conditions[7]

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

Byte Erase or Byte Write Cycle Timing

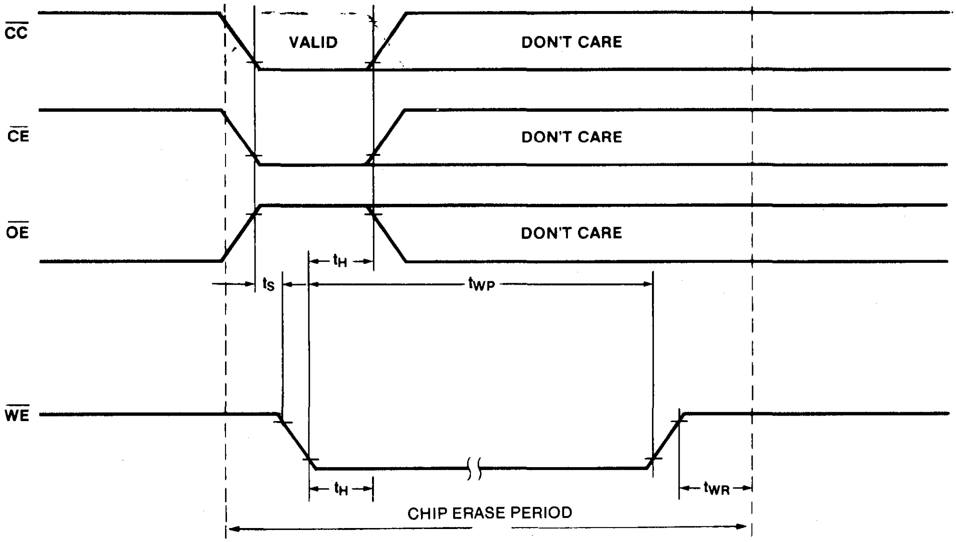


NOTES:
See previous page for notes.

A.C. Operating Characteristics During Chip/Erase (Over the operating V_{CC} and temperature range)

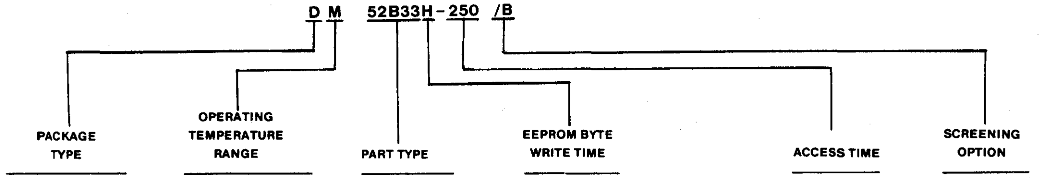
Symbol	Parameter	Min.	Max.	Units
t_S	$\overline{CC}$, $\overline{CE}$ $\overline{OE}$ Setup to $\overline{WE}$	50		ns
t_H[4]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, $\overline{CC}$ change	50		ns
t_{WP}	Write Enable ($\overline{WE}$) Pulse Width Chip Erase — M52B33/M52B33H Chip Erase — E52B33/E52B33H	10		ms
t_{WR}[5]	$\overline{WE}$ to Mode change $\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle		1	µs

TTL Chip Erase Timing



NOTE: Address, Data are don't care during Chip Erase.

Ordering Information



PACKAGE TYPE	OPERATING TEMPERATURE RANGE	PART TYPE	EEPROM BYTE WRITE TIME	ACCESS TIME	SCREENING OPTION
D = CERAMIC DIP L = LEADLESS CHIP CARRIER	E = −40°C TO + 85°C M = −55°C TO + 125°C	8K x 8 EEPROM	(BLANK) = STANDARD WRITE TIME H = FAST WRITE TIME	250 = 250 ns 300 = 300 ns	/B - MIL 883 CLASS B SCREENED

seeq

E/M2816A
Timer E^2
16K Electrically Erasable PROMs

October 1988

Features

- **High Endurance Write Cycles**
  - **2816A: 10,000 Cycles/Byte Minimum**
- **On-Chip Timer**
  - **Automatic Erase and Write Time Out**
- **All Inputs Latched by Write or Chip Enable**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - **110 mA max. Active Current**
  - **40 mA max. Standby Current**
- **JEDEC Approved Byte-Wide Pinout**
- **Military and Extended Temperature Range**
  - **−55°C to +125°C: M2816A (Military)**
  - **−40°C to +85°C: E2816A (Extended)**

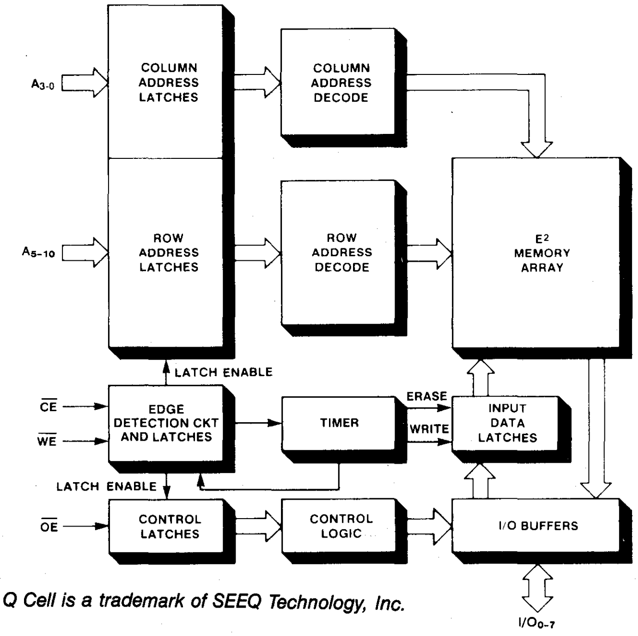
Description

SEEQ's E/M2816A are 5V only, 2K x 8 electrically erasable programmable read only memories (EEPROM). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times that a byte may be written, is 10 thousand for the E/M2816A. The E/M2816A's high endurance was accomplished using SEEQ's proprietary oxyntride EEPROM process and its innovative Q Cell™ design. The E/M2816A is ideal for systems that require frequent updates.

There is an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable (WE) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system

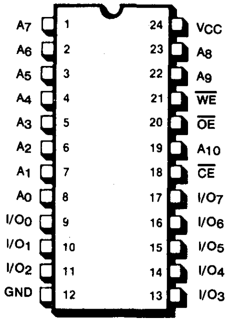
(continued on next page)

Block Diagram



Q Cell is a trademark of SEEQ Technology, Inc.

Pin Configuration



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

for other tasks during the write time. The E/M2816's write time is 10 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode[1], only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$ and data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

Mode Selection (Table 1)

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X	V_{IL}	X	High Z/D_{OUT}
	X	X	V_{IH}	High Z/D_{OUT}

X: Any TTL level.

Power Up/Down Considerations

The E/M2816A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.[2]*
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature

Storage	*−65°C to +150°C*
Under Bias	*−65°C to +135°C*
All Inputs or Outputs with Respect to Ground	*+6V to −0.3V*

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2816A	E2816A
Temperature Range	(Case) −55°C to 125°C	(Ambient) −40°C to 85°C
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%

Endurance and Data Retention

Condition	Symbol	Parameter	Value	Units
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

NOTES:
1. Chip Erase is an optional mode.
2. Characterized. Not tested.

DC Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current		125	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O's Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = 5.5$ V
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = 5.5$ V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ µA

AC Characteristics

Read Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits E/M2816A-250 Min.	Limits E/M2816A-250 Max.	Limits E/M2816A-350 Min.	Limits E/M2816A-350 Max.	Units
t_{RC}	Read Cycle Time	250		350		ns
t_{CE}	Chip Enable Access Time		250		350	ns
t_{AA}	Address Access Time		250		350	ns
t_{OE}	Output Enable Access Time		90		100	ns
t_{LZ}	$\overline{CE}$ to Output in Low Z	10		10		ns
t_{HZ}	$\overline{CE}$to Output in High Z		100		100	ns
t_{OLZ}	$\overline{OE}$ to Output in Low Z	50		50		ns
t_{OHZ}	$\overline{OE}$ to Output in High Z		100		100	ns
t_{OH}[1]	Output Hold from Address Change	20		20		ns
t_{PU}[1]	$\overline{CE}$ to Power-up Time	0		0		ns
t_{PD}[1]	$\overline{CE}$ to Power Down Time		50		50	ns

Capacitance[2] $T_A=25°C$, f=1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0$ V

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[1]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

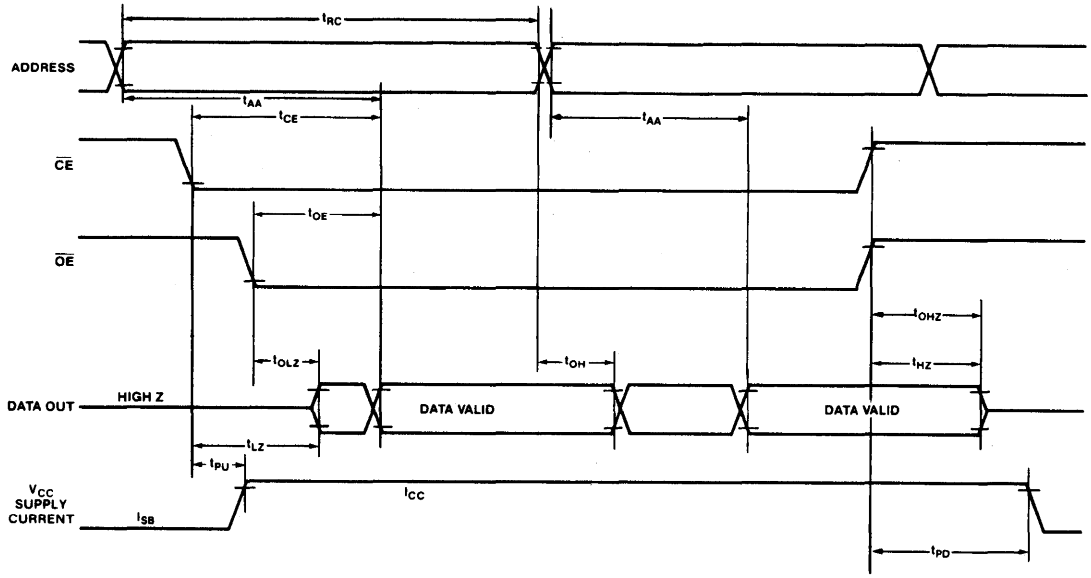
Equivalent A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

NOTES:

1. Characterized. Not tested.
2. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

Read Cycle Timing



AC Characteristics

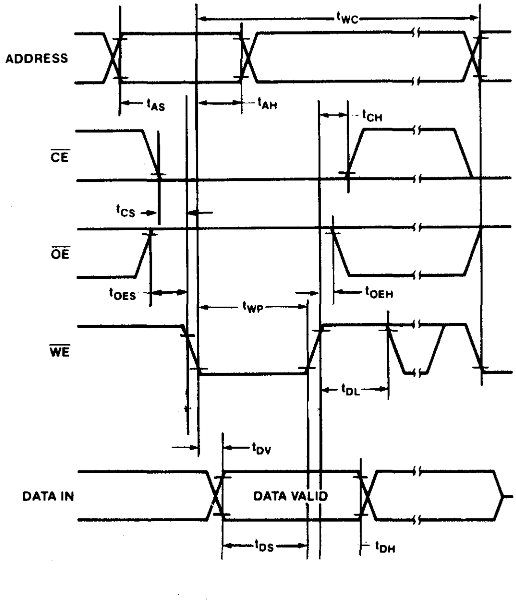
Write Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits				Units
		E/M2816A-250		E/M2816A-350		
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Set Up Time	10		10		ns
t_{AH}	Address Hold Time	50		70		ns
t_{CS}	Write Set Up Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ to End of Write Input	150		150		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		ns
t_{WP}[1]	$\overline{WE}$ Write Pulse Width	150		150		ns
t_{DL}	Data Latch Time	50		50		ns
t_{DV}[2]	Data Valid Time		1		1	μs
t_{DS}	Data Set Up Time	50		50		ns
t_{DH}	Data Hold Time	0		0		ns

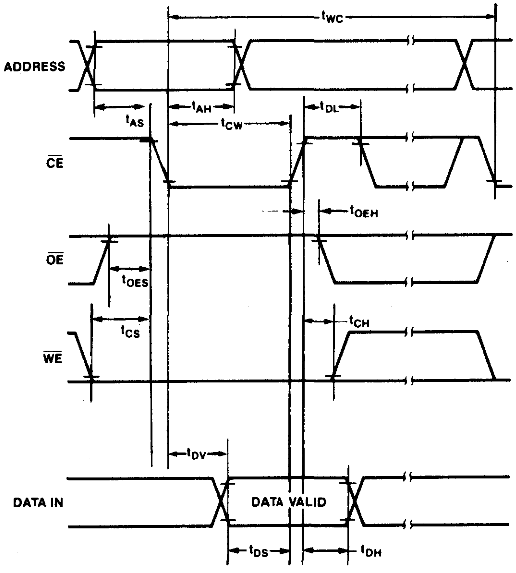
Notes:
1. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1 μs maximum after the initiation of a write cycle.

TTL Byte Write Cycle

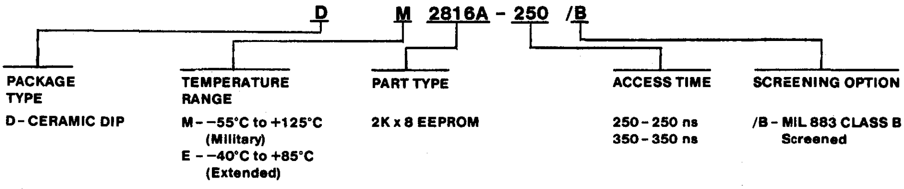
$\overline{\text{WE}}$ CONTROLLED WRITE CYCLE



$\overline{\text{CE}}$ CONTROLLED WRITE CYCLE



Ordering Information



D M 2816A - 250 /B

PACKAGE TYPE

D - CERAMIC DIP

TEMPERATURE RANGE

M - −55°C to +125°C (Military)
E - −40°C to +85°C (Extended)

PART TYPE

2K x 8 EEPROM

ACCESS TIME

250 - 250 ns
350 - 350 ns

SCREENING OPTION

/B - MIL 883 CLASS B Screened

seeq

E/M2817A
Timer E^2
16K Electrically Erasable PROMs

February 1987

Features

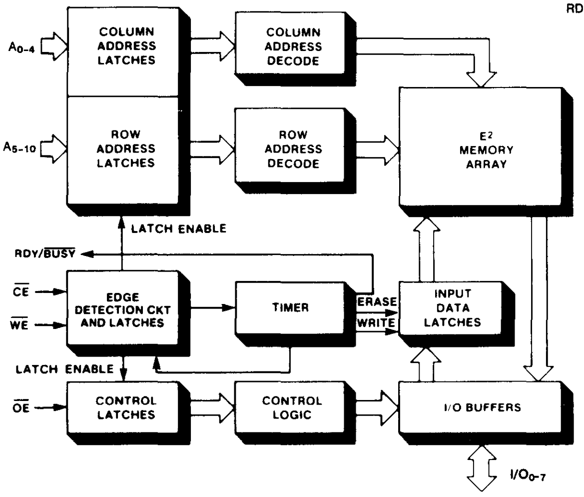
- **Military and Temperature Range**
  - **−55°C to +125°C: M2817A (Military)**
  - **−40°C to +85°C: E2817A (Extended)**
- **Read/$\overline{\text{Busy}}$ Pin**
- **High Endurance, 10,000 Byte Write Cycles Minimum**
- **On-Chip Timer**
  - **Automatic Byte Erase Before Byte Write**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - **110 mA Active Current**
  - **40 mA Standby Current**
- **JEDEC Approved Byte-Wide Pinout**

Description

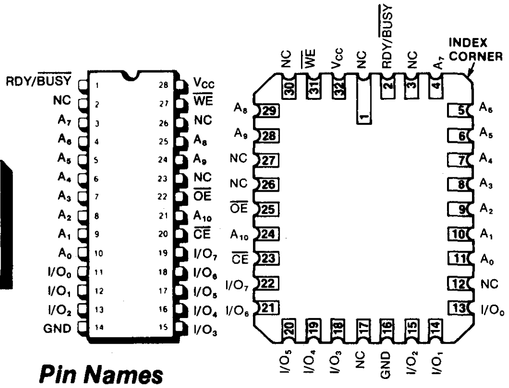
SEEQ's M2817A is a 5 V only, 2K x 8 electrically erasable programmable read only memory (EEPROM). It is packaged in a 28 pin package and has a ready/$\overline{\text{busy}}$ pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times which a byte may be written, is 10 thousand cycles.

The M2817A has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The 2817A's write cycle time is 10 ms over the military temperature

Block Diagram



Pin Configuration


DUAL-IN-LINE TOP VIEW

LEADLESS CHIP CARRIER BOTTOM VIEW

Pin Names

A_{0-4}	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_{5-10}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/$\overline{\text{BUSY}}$	DEVICE READY/$\overline{\text{BUSY}}$
N/C	NO CONNECT

range. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/$\overline{\text{busy}}$ pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode,[1] only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ($\overline{\text{WE}}$) pin of a selected ($\overline{\text{CE}}$ low) device. This, combined with output enable ($\overline{\text{OE}}$) being high, initiates a write cycle. During a byte write cyole, addresses are latched on either the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever one occurred last. Data is latched on the rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever one occured first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{\text{BUSY}}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{\text{BUSY}}$ pin to a TTL high. The RDY/$\overline{\text{BUSY}}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied 2817A RDY/$\overline{\text{BUSY}}$ pins.

Mode Selection (Table 1)

Mode/Pin	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O	RDY/$\overline{\text{BUSY}}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X X	V_{IL} X	X V_{IH}	High Z/D_{OUT} High Z/D_{OUT}	High Z High Z

X: Any TTL Level.

Power Up/Down Considerations

The M2817A has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.[2]*
2. *A negative Write Enable ($\overline{\text{WE}}$) transition has not occurred with V_{CC} is between 3 V and 5 V.*

   Writing will also be prevented if $\overline{\text{CE}}$ or $\overline{\text{OE}}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

Absolute Maximum Stress Ratings*

Temperature
Storage .... −65°C to +150°C
Under Bias .... −10°C to +135°C
All Inputs or Outputs with
Respect to Ground .... +6V to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2817A-300 M2817A-250	E 2817A-300 E 2817A-250
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%
Temperature Range	(Case) −55°C to +125°C	(Ambient) −40°C to +85°C

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

NOTES:
1. Chip Erase is an optional mode.
2. Characterized. Not tested.

D.C. Operating Characteristics (Over the operating V_{CC} and temperature range)

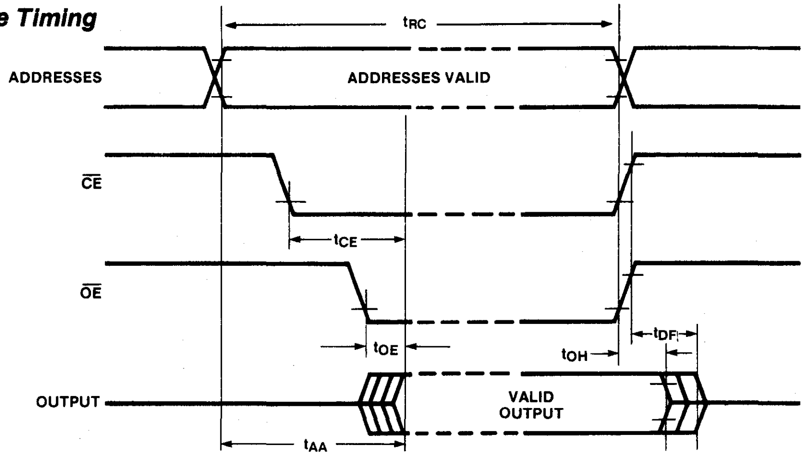
Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = 5.5 V
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = 5.5$ V
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = 5.5$ V
V_{IL}	Input Low Voltage	-0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA

A.C. Characteristics

Read Operation (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits E/M2817A-250 Min.	Limits E/M2817A-250 Max.	Limits E/M2817A-300 Min.	Limits E/M2817A-300 Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	250		300		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		90		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read Cycle Timing



Capacitance[1] T_A=25°C, f=1 MHz

Symbol	Parameter	Max	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0$ V

A.C. Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

AC Characteristics

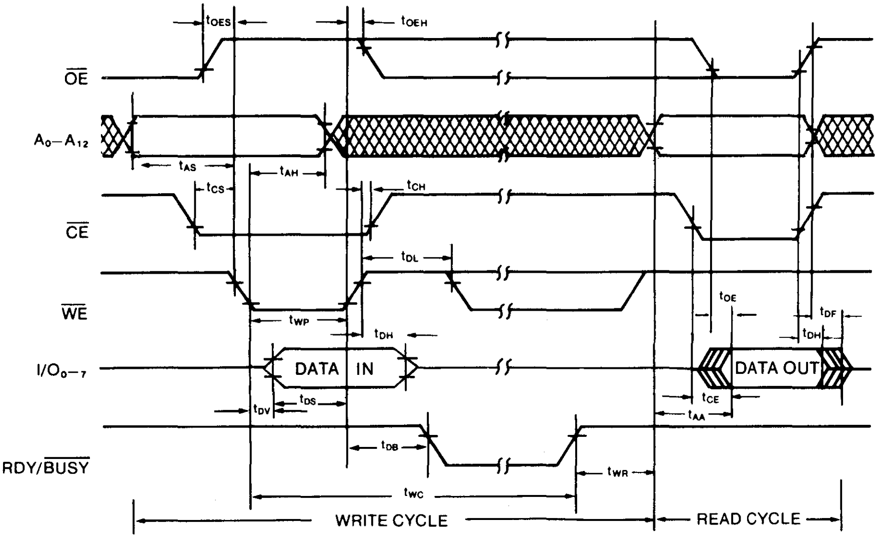
Write Operation (Over the operating $V_{CC}$and temperature range)

		Limits				
		E/M2817A-250		E/M2817A-300		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
t_{AS}	Address to Write Set Up Time	10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	10		10		ns
t_{WP}[3]	$\overline{WE}$ Write Pulse Width	150		150		ns
t_{AH}	Address Hold Time	50		50		ns
t_{DS}	Data Set Up Time	50		50		ns
t_{DH}	Data Hold Time	0		0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		ns
t_{DL}	Data Latch Time	50		50		ns
t_{DV}[4]	Data Valid Time		1		1	μs
t_{DB}	Time to Device Busy		200		200	ns
t_{WR}	Write Recovery Time Before Read Cycle		10		10	μs
t_{WC}	Byte Write Time		10		10	ms

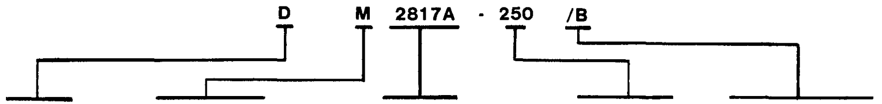
NOTES:

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.
3. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
4. Data must be valid within 1 ms maximum after the initiation of a write cycle.

Write Cycle Timing



Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D - Ceramic Dip L - LCC	M--55°C to +125°C (Military) E--40°C to +85°C (Extended)	2K x 8 EEPROM	250 - 250 ns 300 - 300 ns	/B - MIL 883 CLASS B Screened

seeq

M2864/M2864H
E2864/E2864H
Timer E^2
64K Electrically Erasable ROMs

October 1987

Features

- **64K EEPROM**
  - **— Military Temperature M2864**
  - **— Extended Temperature E2864**
- **Ready/Busy Pin**
- **High Endurance Write Cycles**
  - **— 10,000 Cycles/Byte Minimum**
- **On-Chip Timer**
  - **— Automatic Byte Erase Before Byte Write**
  - **— 2 ms Byte Write (M2864H)**
- **5 V±10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**

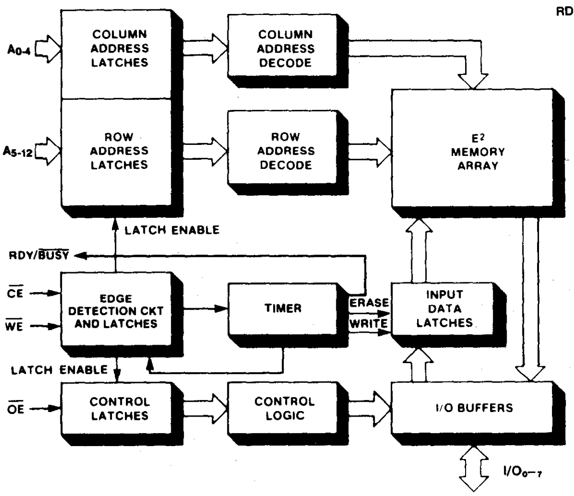
Description

SEEQ's M2864 is a 5 V only, 8K x 8 NMOS electrically erasable programmable read only memory (EEPROM). It is packaged in a 28 pin package and has a ready/$\overline{\text{busy}}$ pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is a minimum of 10 thousand cycles.

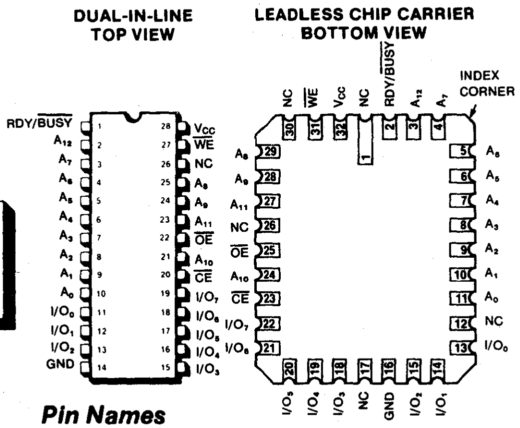
The EEPROM has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The standard byte write cycle time is 10 ms. For systems requiring faster byte write, an M2864H is specified at 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/$\overline{\text{busy}}$ pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

These two timer EEPROMs are ideal for systems with limited board area. For systems where cost is important, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

Block Diagram



Pin Configuration


DUAL-IN-LINE TOP VIEW

LEADLESS CHIP CARRIER BOTTOM VIEW

Pin Names

A_{0-4}	ADDRESSES — COLUMN (LOWER ORDER BITS)
A_{5-12}	ADDRESSES — ROW
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/$\overline{\text{BUSY}}$	DEVICE READY/BUSY
N/C	NO CONNECT

Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a 150 ns TTL pulse is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This, combined with output enable ($\overline{OE}$) being high, initiates a 10 ms write cycle. During a byte write cycle, addresses are latched on either the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred last. Data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3K Ω pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins. If RDY/$\overline{BUSY}$ is not used it can be left unconnected.

Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)	RDY/ $\overline{BUSY}$ (1)*
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z
Standby	V_{IH}	X	X	High Z	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X X	V_{IL} X	X V_{IH}	High Z/D_{OUT} High Z/D_{OUT}	High Z High Z

*Pin 1 has an open drain output and requires an external 3K resistor to V_{CC}. The resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

Power Up/Down Considerations

The M2864 has internal circuitry to minimize a false write during system V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions.

1. *V_{CC} is less than 3 V.*[1]
2. *A negative Write Enable ($\overline{WE}$) transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

*Absolute Maximum Stress Ratings**

Temperature
Storage .... -65° C to +150° C
Under Bias .... -65° C to +135° C

All Inputs or Outputs with
Respect to Ground .... +6 V to −0.3 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2864 M2864H	E2864 E2864H
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%
Temperature Range	(Case) −55°C to +125°C	(Ambient) −40°C to +85°C

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

NOTE: 1 – Characterized. Not tested.

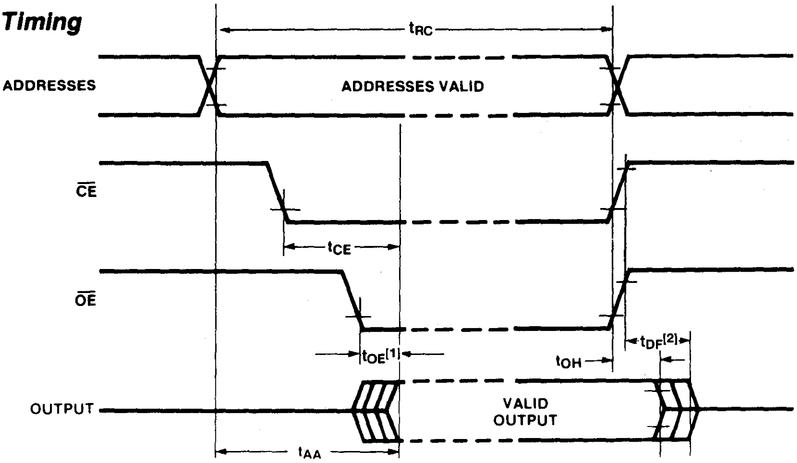
DC Operating Characteristics (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current (Includes Write Operation)		120	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{SB}	Standby V_{CC} Current		50	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = V_{CC}$ Max.
I_{LO}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.1	0.8	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA

AC Characteristics Read Operation (Over the operating V_{CC} and temperature range)

		Limits							
		E/M2864H-250 E/M2864-250		E/M2864H-300 E/M2864-300		M2864-350			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		90		100		100	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Not being Driven	0	60	0	60	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

Read Cycle Timing



NOTES:

1. $\overline{OE}$ MAY BE DELAYED TO $t_{AA} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{AA}.
2. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.

Capacitance T_A[1] = 25° C; f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0$ V
C_{OUT}	Data (I/O) Cap,	10 pF	$V_{I/O} = 0$ V

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

E.S.D. Characteristics[4]

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

AC Characteristics

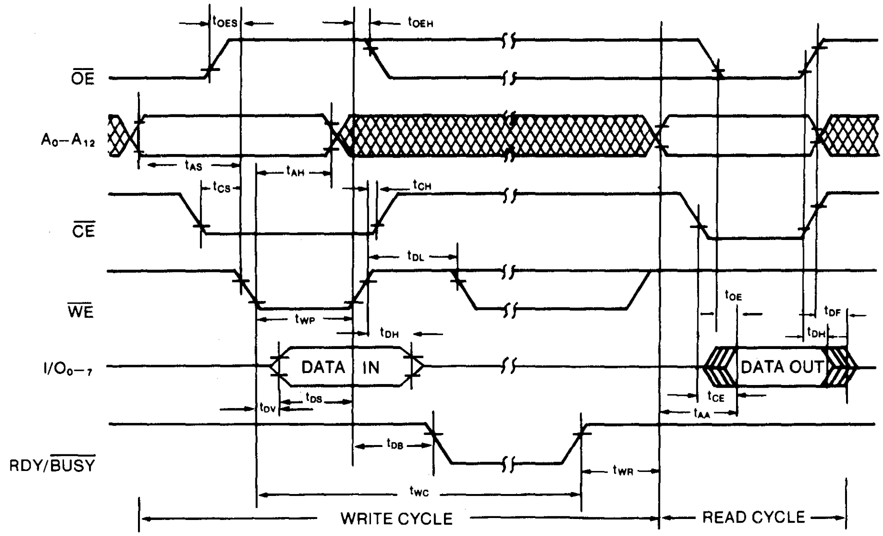
Write Operation (Over operating temperature and V_{CC} range)

		Limits						
		E/M2864H-250 E/M2864-250		E/M2864H-300 E/M2864-300		E/M2864H-350 E/M2864-350		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{WC}	Write Cycle Time/Byte Standard Family Only		10		10		10	ms
	"H" Family Only		2		2		—	ms
t_{AS}	Address to WE Set Up Time	10		10		10		ns
t_{CS}	$\overline{CE}$ to Write Set Up Time	0		0		0		ns
t_{WP}[2]	$\overline{WE}$ Write Pulse Width	150		150		150		ns
t_{AH}	Address Hold Time	50		50		70		ns
t_{DS}	Data Set Up Time	50		50		50		ns
t_{DH}	Data Hold Time	20		20		20		ns
t_{CH}	$\overline{CE}$ Hold Time	0		0		0		ns
t_{OES}	$\overline{OE}$ Set Up Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{DL}	Data Latch Time	50		50		50		ns
t_{DV}[3]	Data Valid Time		1		1		1	µs
t_{DB}	Time to Device Busy		200		200		200	ns
t_{WR}	Write Recovery Time Before Read Cycle		10		10		10	µs

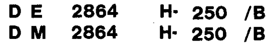
Notes:

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within 1 µs maximum after the initiation of a write cycle.
4. Characterized. Not tested.

Write Cycle Timing



Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	EEPROM BYTE WRITE TIME	ACCESS TIME	SCREENING OPTION
D=CERAMIC DIP L - LCC	M - −55°C to +125°C (Military) E - −40°C to +85°C (Extended)	8K x 8 EEPROM	(Blank) - Standard Write Time H - Fast Write Time	250 - 250 ns 300 - 300 ns 350 - 350 ns	/B - MIL 883 CLASS B SCREENED

seeq

E/M28C64
Timer E^2
64K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October, 1988

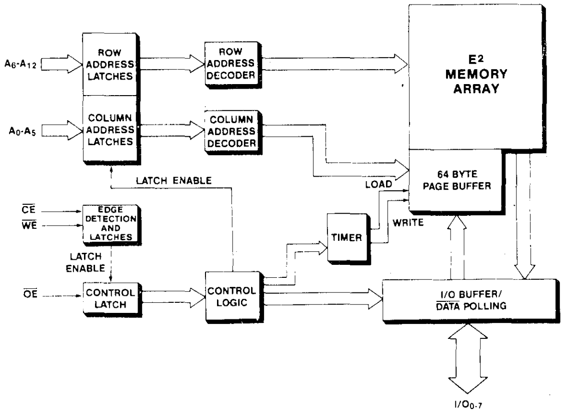
Features

- **Military and Extended Temperature Range**
  - **−55°C to +125°C Operation (Military)**
  - **−40°C to +85°C Operation (Extended)**
- **CMOS Technology**
- **Low Power**
  - **60 mA Active**
  - **250 μA Standby**
- **Page Write Mode**
  - **64 Byte Page**
  - **160 us Average Byte Write Time**
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - **$\overline{\text{DATA}}$ Polling**
- **On Chip Timer**
  - **Automatic Erase Before Write**
- **High Endurance**
  - **10,000 Cycles/Byte Minimum**
  - **10 Year Data Retention**
- **Power Up/Down Protection Circuitry**
- **200 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**

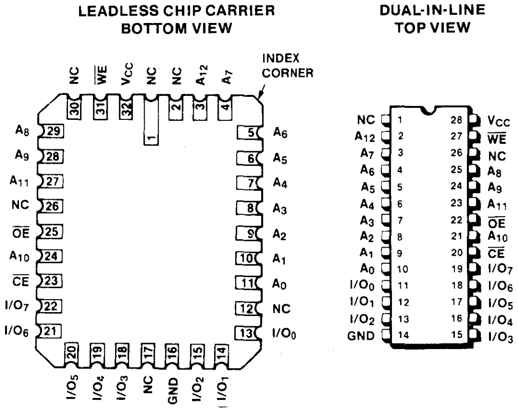
Description

SEEQ's E/M28C64 is a CMOS 5V only, 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Leadless Chip Carrier (LCC). The E/M28C64 is ideal for applications which require low power consumption, nonvolatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. System reliability, in all applications, is higher because of the low failure rate of the Q Cell.

The E/M28C64 has an internal timer which automatically times out the write time. the on-chip timer, along with input latches free the micro



Pin Configuration



Pin Names

A_{0-5}	ADDRESSES—COLUMN
A_6-A_{12}	ADDRESSES—ROW
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/DATA OUTPUT (READ)
NC	NO CONNECTION

Q Cell is a trademark of SEEQ Technology, Inc.

processor for other tasks while the part is busy writing. The E/M28C64's write cycle time is 10 ms. An automatic erase is performed before a write. The $\overline{\text{DATA}}$ polling feature of the E/M28C64 can be used to determine the end of a write cycle. Once the write cycle has been completed, data can be read in a maximum of 200 ns. Data retention is specified for 10 years.

Device Operation

Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

Mode Selection

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X X	V_{IL} X	X V_{IH}	HI Z/D_{OUT} HI Z/D_{OUT}
Chip Erase	V_{IL}	V_H	V_{IL}	X

X: Any TTL level
V_H: High Voltage

Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{\text{CE}}$ is brought to a TTL low in order to enable the chip. The $\overline{\text{WE}}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ($\overline{\text{OE}}$) to a TTL low. During read, the address, $\overline{\text{CE}}$, $\overline{\text{OE}}$, and I/O latches are transparent.

Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ($\overline{\text{WE}}$) pin of a selected ($\overline{\text{CE}}$ low) device. This combined with Output Enable ($\overline{\text{OE}}$) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurred last. Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurred first. An automatic erase is perfomed before data is written.

Write Cycle Control Pins

For system design simplification, the E/M28C64 is designed such that either the $\overline{\text{CE}}$ or $\overline{\text{WE}}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{\text{OE}}$ setup and hold are with respect to the later of $\overline{\text{CE}}$ or $\overline{\text{WE}}$; data setup and hold is with respect to the earlier of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

Write Mode

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the $\overline{WE}$ signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write initiated. These addresses and the $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the E/M28C64 latches data and starts the internal page load timer. The timer is reset on the falling edge of the $\overline{WE}$ signal if another write is initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no additional write cycles have been initiated within t_{BLC} after the last $\overline{WE}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle ($\overline{DATA}$ polling).

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the E/M28C64 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining $\overline{WE}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will not start the page load timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

$\overline{DATA}$ Polling

The E/M28C64 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the E/M28C64 is ***still writing,*** *the device will present the ones-complement of the last byte written. When the E/M28C64 has* ***completed*** *its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.*

A $\overline{DATA}$ polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. $\overline{DATA}$ polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a $\overline{DATA}$ polling read is the same as a normal read.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI}V*
2. *A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI}V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.*

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than that specified for a write in the Mode Selection table.

Absolute Maximum Stress Range*

Temperature
Storage.................... −65°C to +150°C
Under Bias .... −65°C to +135°C

D.C. Voltage applied to all Inputs or Outputs with respect to ground...... +6.0 V to −0.5 V

Undershoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground.............. −1.0 V

Overshoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs with respect to ground............. +7.0 V

**COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M28C64	E28C64
Temperature Range	(Case) −55°C to +125°C	(Ambient) −40°C to +85°C
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

DC Characteristics (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I_{CC}	Active V_{CC} Current		60	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.; Max read or write cycle time
I_{SB1}	Standby V_{CC} Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = ANY TTL LEVEL
I_{SB2}	Standby V_{CC} Current (CMOS Inputs)		250	μA	$\overline{CE} = V_{CC} - 0.3$ Other inputs = V_{IL} to V_{IH} All I/O Open
I_{IL}[2]	Input Leakage Current		1	μA	$V_{IN} = V_{CC}$ Max.
I_{OL}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

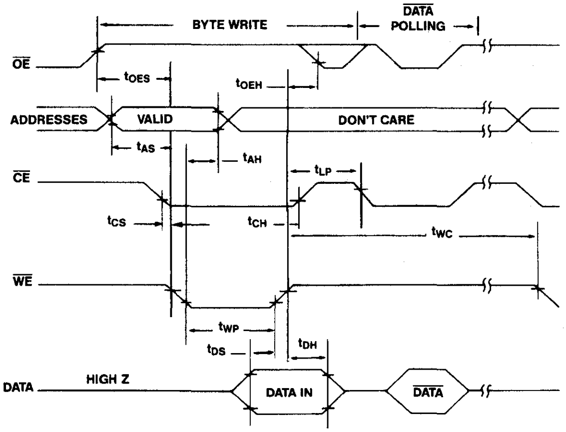
Notes:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.

AC Characteristics Write Operation (Over the operating temperature and V_{CC} range, unless otherwise specified)

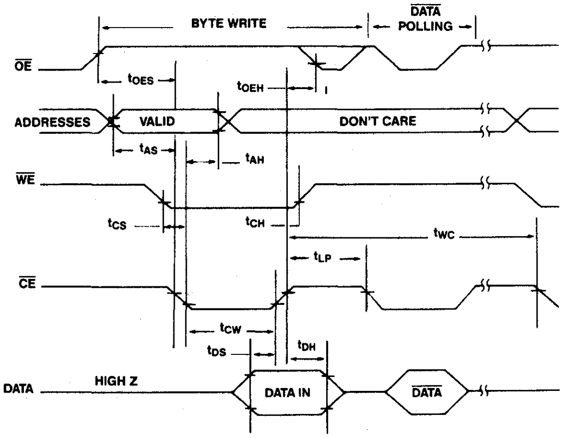
Symbol	Parameter	Limits								Units
		E/M28C64-200		E/M28C64-250		E/M28C64-300		E/M28C64-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Set-up Time	10		10		10		10		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	10		10		10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		10		10		10		ns
t_{WP}	$\overline{WE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (see note 3)	0.2	200	0.2	200	0.2	200	0.2	200	us
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		200		200		200		200	ns

Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



$\overline{CE}$ CONTROLLED WRITE CYCLE



Notes:
1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <10 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

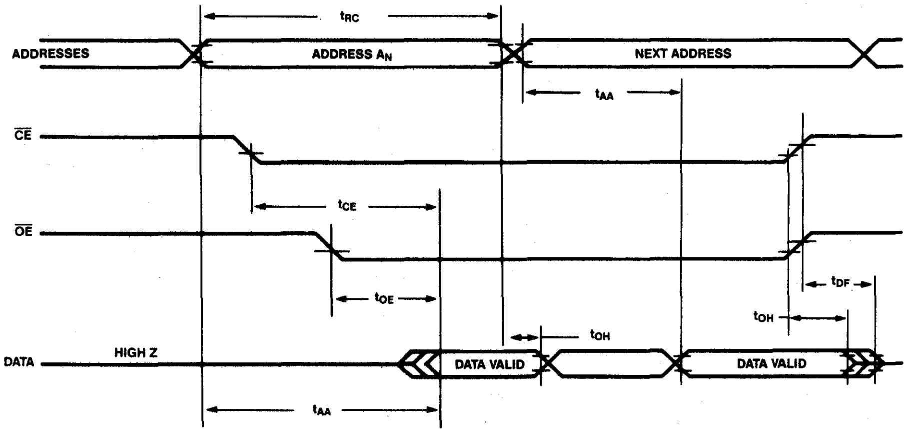
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

AC Characteristics **Read Operation** (Over operating temperature and V_{CC} range, unless otherwise specified)

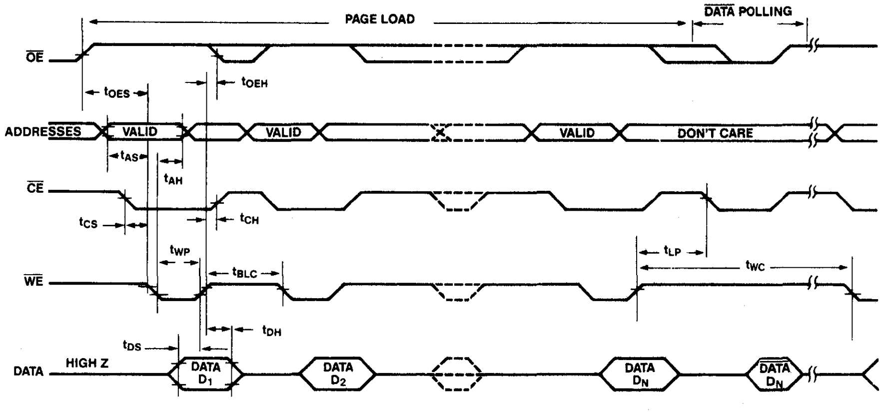
Symbol	Parameter	Limits									Test Conditions
		E/M28C64-200		E/M28C64-250		E/M28C64-300		E/M28C64-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		80		90		90		90	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to output not being driven	0	60	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{\text{Data}}$ Polling Cycle Time



Notes:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

Page Write Timing



Ordering Information

D M 28C64 -250/B

PACKAGE TYPE	TEMPERATURE RANGE	DEVICE	ACCESS TIME	MIL 883 CLASS B SCREENED
D=CERAMIC DIP L=LCC	M- −55° - +125°C (Military) E- −40° - +85°C (Extended)	8K x 8 E² PROM	200=200 ns 250=250 ns 300=300 ns 350=350 ns	

seeq

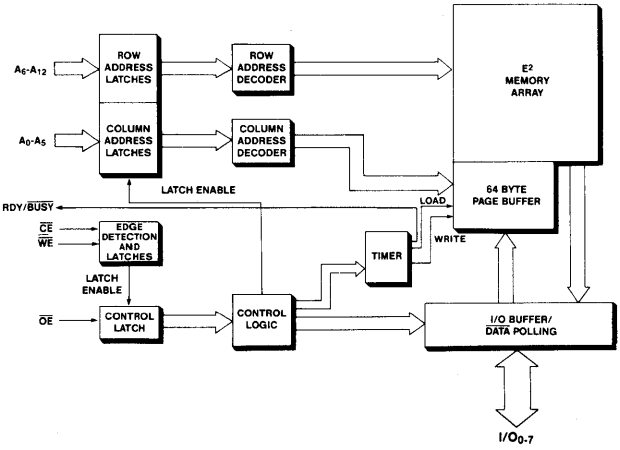
E/M28C65
Timer E^2
64K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October, 1988

Features

- **Military and Extended Temperature Range**
  - **−55°C to +125°C Operation (Military)**
  - **−40°C to +85°C Operation (Extended)**
- **CMOS Technology**
- **Low Power**
  - **60 mA Active**
  - **250 µA Standby**
- **Page Write Mode**
  - **64 Byte Page**
  - **160 us Average Byte Write Time**
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - **$\overline{\text{DATA}}$ Polling**
  - **RDY/$\overline{\text{BUSY}}$ Pin**
- **On Chip Timer**
  - **Automatic Erase Before Write**
- **High Endurance**
  - **10,000 Cycles/Byte Minimum**
  - **10 Year Data Retention**
- **Power Up/Down Protection Circuitry**
- **200 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**



Q Cell is a trademark of SEEQ Technology, Inc.

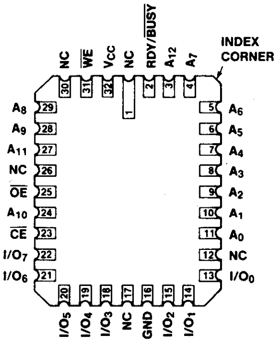
Description

SEEQ's E/M28C65 is a CMOS 5V only, 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Plastic Leadless Chip Carrier (LCC). The E/M28C65 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. System reliability, in all applications, is higher because of the low failure rate of the Q Cell.

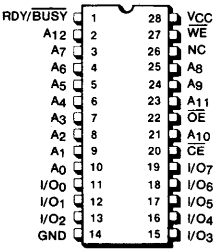
The E/M28C65 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the microprocessor

Pin Configuration

LEADLESS CHIP CARRIER
BOTTOM VIEW



DUAL-IN-LINE
TOP VIEW



Pin Names

A_{0-5}	ADDRESSES — COLUMN
A_{6-12}	ADDRESSES ROW
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE) DATA OUTPUT (READ)
RDY/$\overline{\text{BUSY}}$	DEVICE READY/BUSY
NC	NO CONNECTION

for other tasks while the part is busy writing. The E/M28C65's write cycle time is 10 ms. An automatic erase is performed before a write. The $\overline{DATA}$ polling feature of the E/M28C65 can be used to determine the end of a write cycle. Once the write has been completed, data can be read in a maximum of 200 ns. Data retention is specified for 10 years.

Device Operation

Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

Mode Selection

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	RDY/$\overline{BUSY}$[1]
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	HI Z
Standby	V_{IH}	X	X	HI Z	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}
Write Inhibit	X X	V_{IL} X	X V_{IH}	HI Z/D_{OUT} HI Z/D_{OUT}	HI Z HI Z
Chip Erase	V_{IL}	V_H	V_{IL}	X	HI Z

X: Any TTL level
V_H: High Voltage

Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ($\overline{OE}$) to a TTL low. During read, the address, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This combined with Output Enable ($\overline{OE}$) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred last. Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred first. An automatic erase is perfomed before data is written.

Write Cycle Control Pins

For system design simplification, the E/M28C65 is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{OE}$ setup and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data setup and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

NOTES:

1. RDY/$\overline{BUSY}$ Pin 1 (Pin 2 on LCC) has an open drain output and requires an external 3K resistor to V_{CC}. The value of the resistor is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins.

Write Mode

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the $\overline{WE}$ signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write initiated. These addresses and the $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the E/M28C65 latches data and starts the internal page load timer. The timer is reset on the falling edge of the $\overline{WE}$ signal if another write is initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no additional write cycles have been initiated within t_{BLC} after the last $\overline{WE}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle ($\overline{DATA}$ polling).

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the E/M28C65 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining $\overline{WE}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will not start the page load timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

$\overline{DATA}$ Polling

*The E/M28C65 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the E/M28C65 is **still writing,** the device will present the ones-complement of the last byte written. When the E/M28C65 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.*

A $\overline{DATA}$ polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. $\overline{DATA}$ polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a $\overline{DATA}$ polling read is the same as a normal read.

READY/$\overline{BUSY}$ Pin

E/M28C65 provides write cycle status on this pin. RDY/$\overline{BUSY}$ output goes to a TTL low immediately after the falling edge of $\overline{WE}$. RDY/$\overline{BUSY}$ will remain low during the byte load or page load cycle and continues to remain at a TTL low while the write cycle is in progress. An internal timer times out the required write cycle time and at the end of this time, the device signals RDY/$\overline{BUSY}$ pin to a TTL high. This pin can be polled for write cycle status or used to initate a rising edge triggered interrupt indicating write cycle completion. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3 K pull-up resistor to V_{CC} is required. The pull-up value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins. If RDY/$\overline{BUSY}$ is not used, it can be left unconnected.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI}V*
2. *A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI}V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.*

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than that specified for a write in the Mode Selection table.

Absolute Maximum Stress Range*

Temperature
Storage.................... −65°C to +150°C
Under Bias .... −65°C to +135°C
D.C. Voltage applied to all Inputs or Outputs
with respect to ground...... +6.0 V to −0.5 V
Undershoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs
with respect to ground.............. −1.0 V
Overshoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs
with respect to ground............. +7.0 V

**COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M28C64	**E28C64**
Temperature Range	(Case) −55°C to +125°C	(Ambient) −40°C to +85°C
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%

Endurance and Data Retention

Symbol	**Parameter**	**Value**	**Units**	**Condition**
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

DC Characteristics (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	**Parameter**	**Limits**		**Units**	**Test Condition**
		Min.	**Max.**		
I_{CC}	Active V_{CC} Current		60	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O Open; Other Inputs = V_{CC} Max.; Max read or write cycle time
I_{SB1}	Standby V_{CC} Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O Open; Other Inputs = ANY TTL LEVEL
I_{SB2}	Standby V_{CC} Current (CMOS Inputs)		250	μA	$\overline{CE} = V_{CC} - 0.3$ Other inputs = V_{IL} to V_{IH} All I/O Open
I_{IL}[2]	Input Leakage Current		1	μA	$V_{IN} = V_{CC}$ Max.
I_{OL}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

Notes:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <10 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] $T_A = 25$ C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

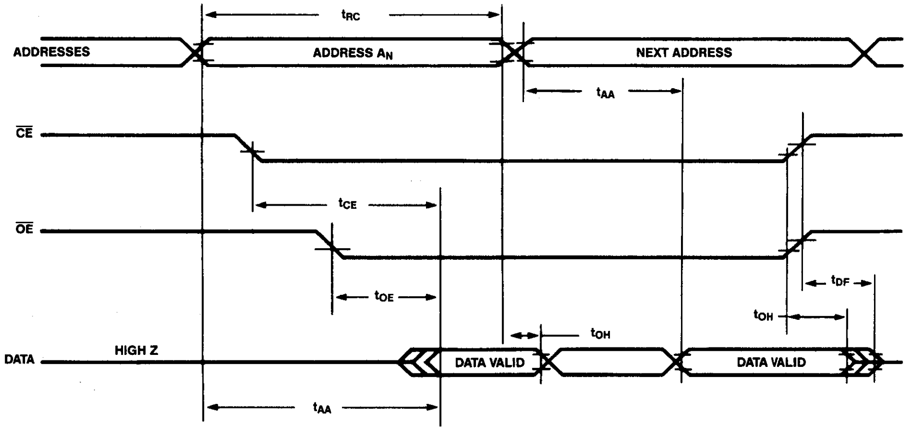
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

AC Characteristics *Read Operation* (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits									Test Conditions
		E/M28C65-200		E/M28C65-250		E/M28C65-300		E/M28C65-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		80		90		90		90	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to output not being driven	0	60	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{\text{Data}}$ Polling Cycle Time



Notes:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

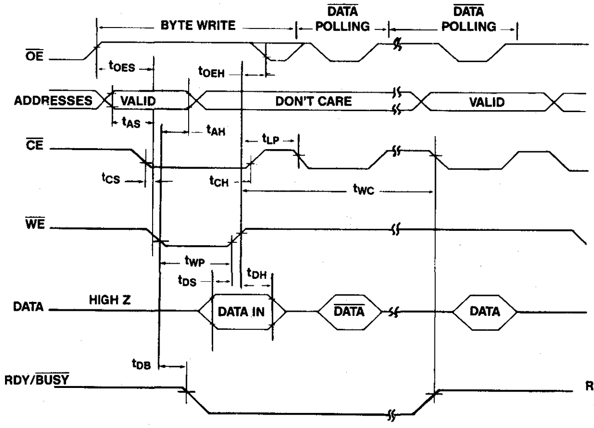
AC Characteristics

Write Operation (Over the operating V_{CC} and temperature range)

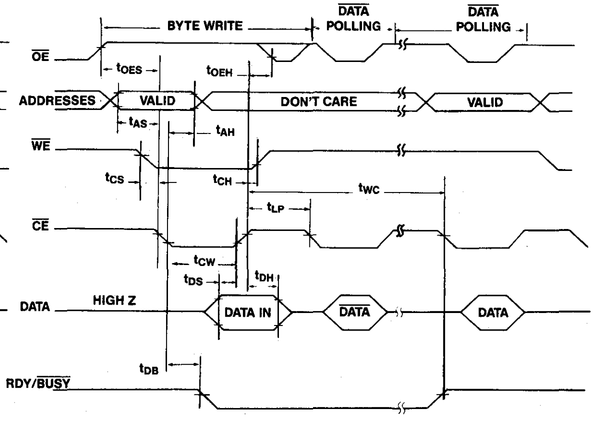
Symbol	Parameter	Limits								Units
		E/M28C65-200		E/M28C65-250		E/M28C65-300		E/M28C65-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Set-up Time	10		10		10		10		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{\text{CE}}$ Pulse Width (note 2)	150		150		150		150		ns
t_{OES}	$\overline{\text{OE}}$ High Set-up Time	10		10		10		10		ns
t_{OEH}	$\overline{\text{OE}}$ High Hold Time	10		10		10		10		ns
t_{WP}	$\overline{\text{WE}}$ Pulse Width (note 2)	150		150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	200	0.2	200	0.2	200	0.2	200	us
t_{LP}	Last Byte Loaded to $\overline{\text{DATA}}$ Polling		200		200		200		200	ns
t_{DB}	Time to Device Busy		100		100		100		100	ns

Write Timing

$\overline{\text{WE}}$ CONTROLLED WRITE CYCLE



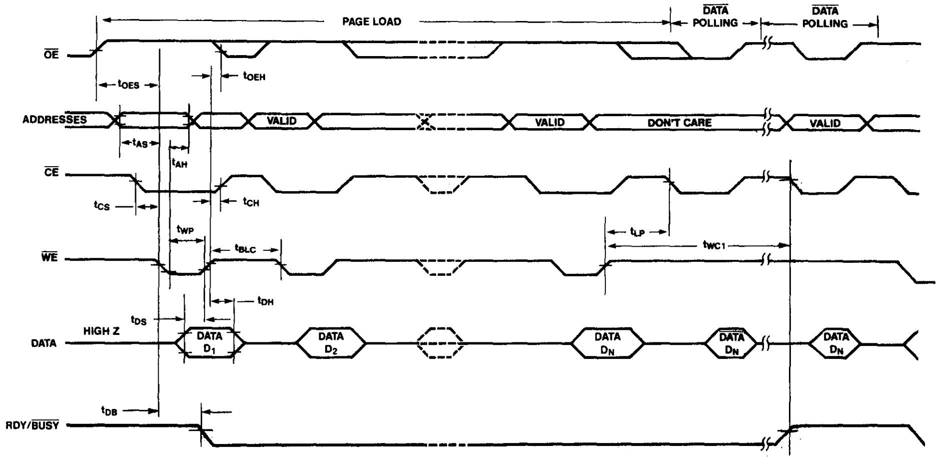
$\overline{\text{CE}}$ CONTROLLED WRITE CYCLE



NOTES:

1. Address hold time is with respect to the falling edge of the control signal $\overline{\text{WE}}$ or $\overline{\text{CE}}$.
2. $\overline{\text{WE}}$ and $\overline{\text{CE}}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating the internal write cycle.

Page Write Timing



Ordering Information

D M 28C65 -250/B

PACKAGE TYPE	TEMPERATURE RANGE	DEVICE	ACCESS TIME	MIL 883 CLASS B SCREENED
D=CERAMIC DIP L=LCC	M- −55° - +125°C (Military) E- −40° - +85°C (Extended)	8K x 8 E² PROM	200=200 ns 250=250 ns 300=300 ns 350=350 ns	

E/M28C256
Timer E^2
256K Electrically Erasable PROM

PRELIMINARY DATA SHEET *November, 1988*

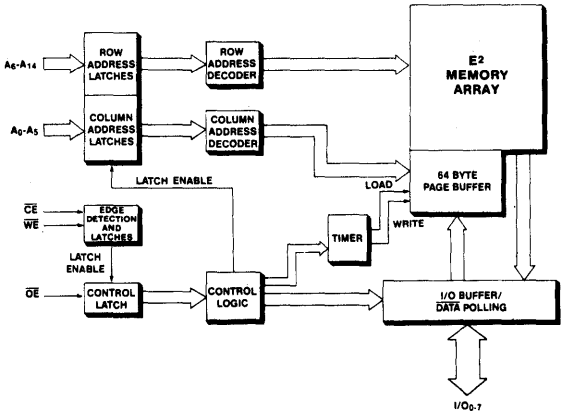
Features

- ***Military and Extended Temperature Range***
  - ***−55°C to +125°C Operation (Military)***
  - ***−40°C to +85°C Operation (Extended)***
- ***CMOS Technology***
- ***Low Power***
  - ***60 mA Active***
  - ***250 μA Standby***
- ***Page Write Mode***
  - ***64 Byte Page***
  - ***160 us Average Byte Write Time***
- ***Byte Write Mode***
- ***Write Cycle Completion Indication***
  - ***$\overline{\text{DATA}}$ Polling***
- ***On Chip Timer***
  - ***Automatic Erase Before Write***
- ***High Endurance***
  - ***10,000 Cycles/Byte***
  - ***10 Year Data Retention***
- ***Power Up/Down Protection Circuitry***
- ***200 ns Maximum Access Time***
- ***JEDEC Approved Byte Wide Pinout***

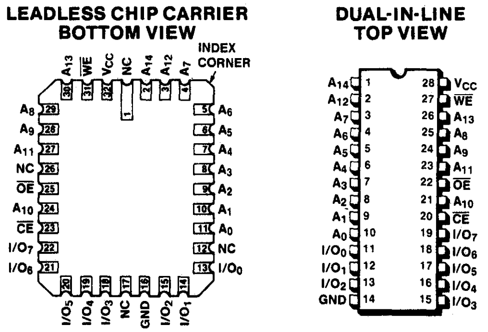
Description

SEEQ's 28C256 is a CMOS 5V only, 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Leadless Chip Carrier (LCC). The 28C256 is ideal for applications which require low power consumption, nonvolatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. System reliability, in all applications, is higher because of the low failure rate of the Q Cell.

The 28C256 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the micro-



Pin Configuration



Pin Names

A_{0-5}	ADDRESSES — COLUMN
A_{6-14}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE)/DATA OUTPUT (READ)

Q Cell is a trademark of SEEQ Technology, Inc.

processor for other tasks while the part is busy writing. The 28C256's write cycle time is 10 ms maximum. An automatic erase is performed before a write. The $\overline{DATA}$ polling feature of the 28C256 can be used to determine the end of a write cycle. Once the write cycle has been completed, data can be read in a maximum of 200 ns. Data retention is greater than 10 years.

Device Operation

Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the aforementioned three input lines.

Table 1

Mode Selection

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X X	X V_{IL}	V_{IH} X	HI Z/D_{OUT} HI Z/D_{OUT}
Chip Erase	V_{IL}	V_{H}	V_{IL}	X

X: any TTL level
V_H: High Voltage

Reads

A read is typically accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ($\overline{OE}$) to a TTL low. During read, the addresses, $\overline{CE}$, $\overline{OE}$, and input data latches are transparent.

Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This combined with Output Enable ($\overline{OE}$) being high initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred last. Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurred first. An automatic erase is performed before data is written.

The 28C256 can write both bytes and blocks of up to 64 bytes. The write mode is discussed below.

Write Cycle Control Pins

For system design simplification, the 28C256 is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch addresses and the earliest low-to-high transition to latch the data. Address and $\overline{OE}$ set up and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data set up and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

Write Mode

One to 64 bytes of data can be randomly loaded into the device. The part latches row addresses, A6-A14, during the first byte write. These addresses are latched on the falling edge of the $\overline{\text{WE}}$ signal and are ignored after that until the end of t_{WC}. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write is initiated. These addresses and the $\overline{\text{OE}}$ state (high) are latched on the falling edge of $\overline{\text{WE}}$ signal. For proper write initiation and latching, the $\overline{\text{WE}}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{\text{WE}}$, allowing easy microprocessor interface.

Upon a low to high $\overline{\text{WE}}$ transition, the 28C256 latches data and starts the internal page load timer. The timer is reset on the falling edge of the $\overline{\text{WE}}$ signal if another write is initiated before the timer has timed out. The timer stays reset while the $\overline{\text{WE}}$ pin is kept low. If no additional write cycles have been initiated in (t_{BLC}) after the last $\overline{\text{WE}}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can now be read to determine the end of write cycle ($\overline{\text{DATA}}$ Polling).

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the 28C256 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining $\overline{\text{WE}}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{\text{CE}}$, $\overline{\text{OE}}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{\text{WE}}$, keeping this signal low will inhibit the page load timer. When $\overline{\text{WE}}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{\text{CE}}$ controlled write the same is true, with CE holding the timer reset instead of $\overline{\text{WE}}$.

$\overline{\text{DATA}}$ Polling

*The 28C256 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{\text{DATA}}$ polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C256 is **still writing,** the device will present the ones-complement of the last byte written. When the 28C256 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. A $\overline{\text{DATA}}$ polling read should not be done until a minimum of t_{LP} microseconds after the last byte is written. Timing for a $\overline{\text{DATA}}$ polling read is the same as a normal read once the t_{LP} specification has been met.*

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI} V*
2. *A high to low Write Enable (WE) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with CE low and OE high.*

Writing will also be inhibited when $\overline{\text{WE}}$, $\overline{\text{CE}}$, or $\overline{\text{OE}}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

*Absolute Maximum Stress Range**

Temperature
Storage.................... −65°C to +150°C
Under Bias .... −65°C to +135°C

D.C. Voltage applied to all Inputs or Outputs
with respect to ground...... +6.0 V to −0.5 V
Undershoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs
with respect to ground.............. −1.0 V
Overshoot pulse of less than 10 ns (measured at 50% point) applied to all inputs or outputs
with respect to ground............. +7.0 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M28C256	E28C256
Temperature Range	(Case) −55°C to +125°C	(Ambient) −40°C to 85°C
V_{CC} Power Supply	5 V ± 10%	5 V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

DC Characteristics Read Operation *(Over operating temperature and V_{CC}Range, unless otherwise specified)*

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Condition
I_{CC}	Active V_{CC} Current		60	mA	$\overline{CE}$=$\overline{OE}$=V_{IL}; All I/O open; Other Inputs = V_{CC} Max. Min. read or write cycle time
I_{SB1}	Standby V_{CC} Current (TTL Inputs)		2	mA	$\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IL}; All I/O open; Other Inputs = V_{IL} to V_{IH}
I_{SB2}	Standby V_{CC} Current (CMOS Inputs)		250	μA	$\overline{CE}$=V_{CC}−0.3 Other Inputs = V_{IL} to V_{IH} All I/O Open
I_{IL}[2]	Input Leakage Current		1	μA	V_{IN}=V_{CC} Max.
I_{OL}[3]	Output Leakage Current		10	μA	V_{OUT}=V_{CC} Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL}=2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH}=−400 μA
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

NOTES:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.
3. For I/O only.

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: <10 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

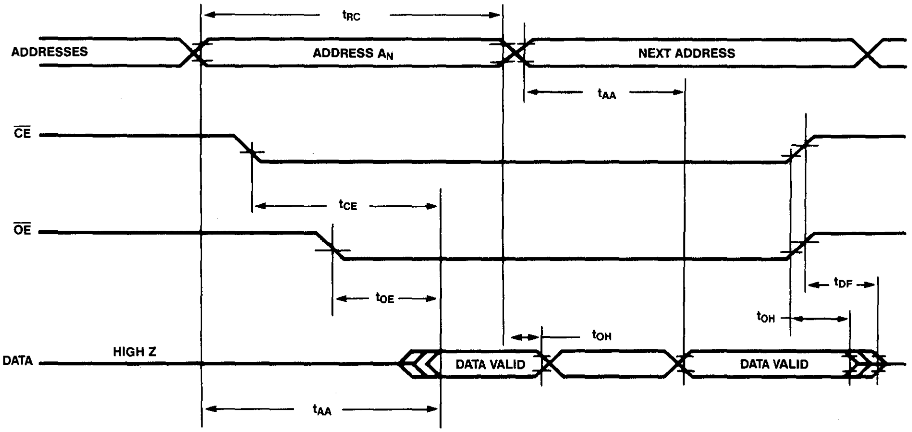
E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	> 2000 V.	MIL-STD 883 Test Method 3015

AC Characteristics Read Operation (Over operating temperature amd V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits									Test Conditions
		E/M28C256-200		E/M28C256-250		E/M28C256-300		E/M28C256-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Units	
t_{RC}	Read Cycle Time	200		250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		200		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		200		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		80		90		90		90	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to output in HI-Z	0	60	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Ouput Hold from Address Change, Chip Enable, or Ouput Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{DATA}$ Polling Cycle



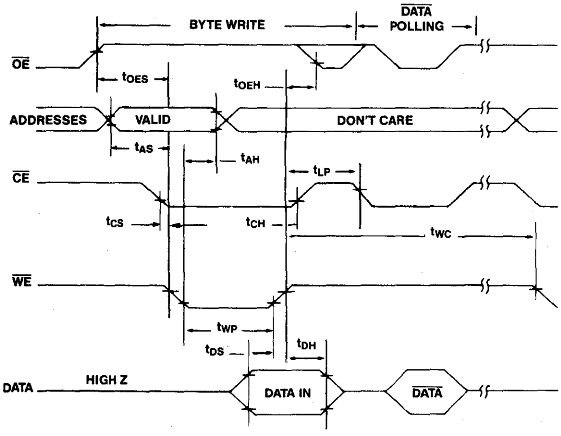
Notes:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

AC Characteristics Write Operation (Over the operating temperature and V_{CC} range, unless otherwise specified)

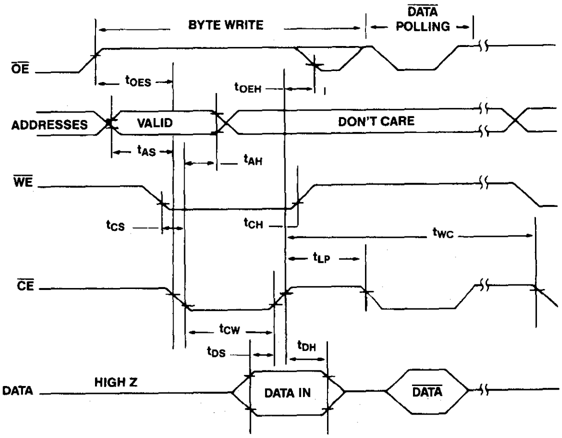
Symbol	Parameter	Limits								Units
		E/M28C256-200		E/M28C256-250		E/M28C256-300		E/M28C256-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10		10	ms
t_{AS}	Address Set-up Time	20		20		20		20		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	20		20		20		20		ns
t_{OEH}	$\overline{OE}$ High Hold Time	20		20		20		20		ns
t_{WP}	$\overline{WE}$ Pulse Width (note 2)	150		150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	200	0.2	200	0.2	200	0.2	200	µs
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		650		650		650		650	µs

Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE



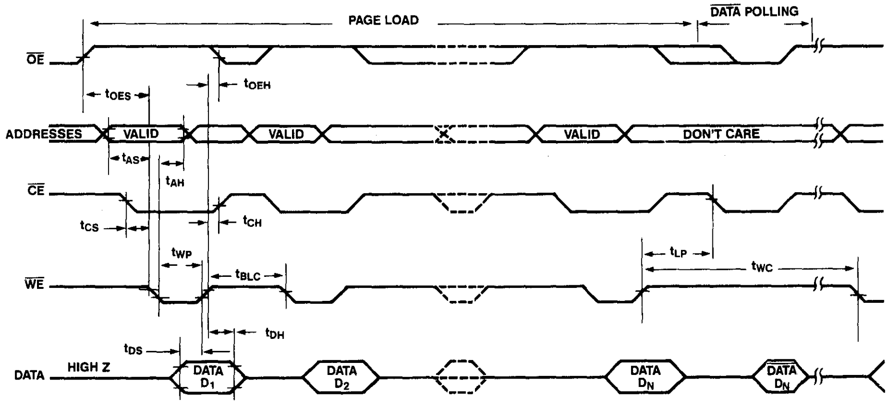
$\overline{CE}$ CONTROLLED WRITE CYCLE



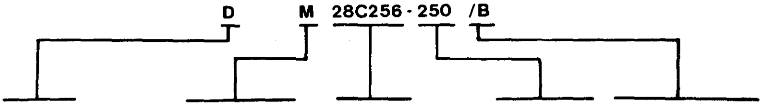
Notes:

1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing



Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D - Ceramic Dip L - LCC F-Flatpack	M - −55°C to +125°C (Military) E - −40°C to +85°C (Extended)	32K x 8 EEPROM	200 = 200 ns 250 = 250 ns 300 = 300 ns 350 = 350 ns	MIL 883 CLASS B SCREENED

seeq

E/M36C16
E/M36C32

High Speed CMOS Electrically Erasable PROM

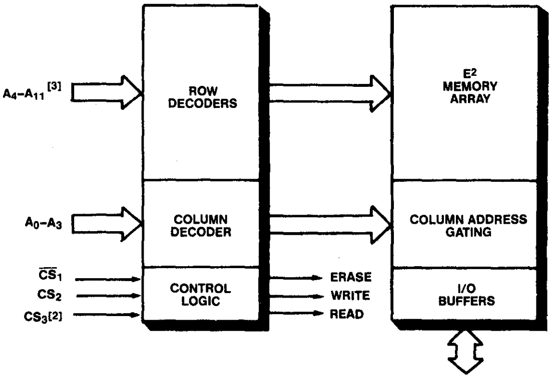
PRELIMINARY DATA SHEET

October 1988

Features

- **Military and Extended Temperature Range**
  - −55°C to +125°C Operation (Military)
  - −40°C to +85°C Operation (Extended)
- **High Speed:**
  - 45ns Maximum Access Time
- **CMOS Technology**
- **Low Power:**
  - 400mW
- **10 Year Data Retention**
- **High Output Drive**
  - Sink 16mA at 0.45V
  - Source 4mA at 2.4V
- **5V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **Fast Byte Write**
  - 5ms/Byte
- **Automatic Byte Clear Before Write**
- **JEDEC Approved PROM Pinout**
- **Direct Replacement for Bipolar PROMs**
- **Slim 300 mil Packaging Available**

Block Diagram



Pin Names

A_0-A_3	ADDRESSES — COLUMN
A_4-A_{11}[3]	ADDRESSES — ROW
$\overline{CS}_1$ CS_2 CS_3	CHIP SELECT INPUTS
I/O_{0-7}	DATA INPUT (WRITE) DATA OUTPUT (READ)

Q Cell is a trademark of SEEQ Technology, Inc.

Description

SEEQ's 36C16/32 are high speed 2K x 8/4K x 8 Electrically Erasable Programmable Read Only Memories, manufactured using SEEQ's advanced 1.25 micron CMOS Process.

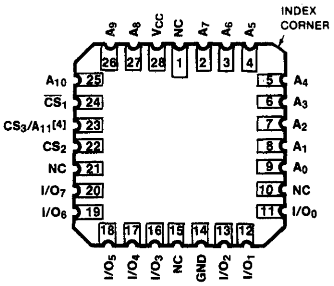
The 36C16/32 are intended as bipolar PROM replacements in high speed applications. The 45ns maximum read access time meets the requirements of many of today's high performance processors. The endurance, the number of times the part can be erased/written, is specified to be greater than 100 cycles. The 36C16/32 are built using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design.

Data retention is specified to be greater than 10 years.

The 36C16/32 are available in 24 pin Slim 300 mil CERAMIC DIP, and 28 pin LCC. Full featured EEPROM versions are also available (38C16/32) in 24/28 pin DIP and 32 pin surface mount packages.

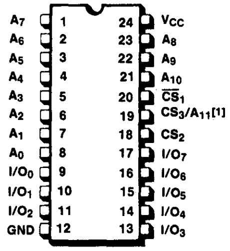
Pin Configuration

LEADLESS CHIP CARRIER
BOTTOM VIEW



DUAL-IN-LINE
TOP VIEW

36C16/36C32
(24 pins)



NOTES:
1. Pin 19 is A_{11} on the 36C32.
2. CS_3 is on the 36C16 only.
3. A_4–A_{10} on the 36C16.
4. Pin 23 is CS_3 on 36C16 and is A_{11} on 36C32.

Device Operation
Operational Modes

MODE PIN	$\overline{CS}_1$	CS_2	CS_3[2]	I/O
Read	V_{IL}	V_{IH}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
	X	V_{IL}	X	
	X	X	V_{IL}	
Write	V_H[1]	V_{IL}	X	D_{IN}

X: Any TTL level

Read

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable, the chip select inputs should be brought to the proper levels in order to enable the outputs (see Table above).

Write

To write into a particular location, addresses and data must be valid, CS_2 must be TTL low and a V_H[1] pulse has to be applied to CS_1 for 5ms. An automatic internal byte clear is done prior to the byte write. The byte clear feature is transparent to the user.

NOTES:
1. V_H – High Voltage.
2. CS_3 applies only to the 36C16. This pin becomes A_{11} in the 36C32.

Absolute Maximum Rating

Temperature	
Storage	*−65°C to +150°C*
Under Bias	*−65°C to +135°C*
All Inputs and Outputs with Respect to Ground	*−3.V to +7V D.C.*
$\overline{CS}_1$ with Respect to Ground	*−0.5V to +14V D.C.*

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	E36C16 E36C32	M36C16 M36C32
V_{CC} Supply Voltage	5V ± 10%	5V ± 10%
Temperature Range (Read Operation)	(Ambient) −40°C to +85°C	(Case) −55°C to 125°C

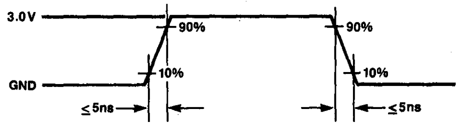
DC Operating Characteristics (Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I_{CC}	V_{CC} Active Current		80	mA	$CS_2 = CS_3 = V_{IH}$; $\overline{CS}_1 = V_{IL}$; Address inputs = 20 MHz I/O = 0mA
I_{IN}	Input Leakage Current		1	μA	$0.1V >= V_{IN} <= V_{CC}$ Max.
I_{OUT}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2	6.5	V	V_{CC} Min
V_H	Input High Voltage During Write/Chip Erase	10.8	13.2	V	For $\overline{CS}_1$ Input Only
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 16$ mA, $V_{CC} = V_{CC}$ Min.
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -4$ mA, $V_{CC} = V_{CC}$ Min.
I_{OS}[1][2]	Output Short Circuit Current	−20		mA	$V_{CC} = V_{CC}$ Max, $V_{OUT} = 0$
V_{CI}[2]	Input Undershoot Voltage	−3		V	V_{IN} undershoot pulse width < 10ns

NOTES:
1. Only one input at a time for less than one second.
2. Characterized. Not Tested.

AC Test Conditions

Output Load: 10 TTL gates and total $C_L = 30pF$
Input Rise and Fall Times: < 5ns
Input Pulse Levels: 0V to 3V
Timing Measurement Reference Level:
Inputs 1.5V
Outputs 1.5V



INPUT PULSES

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

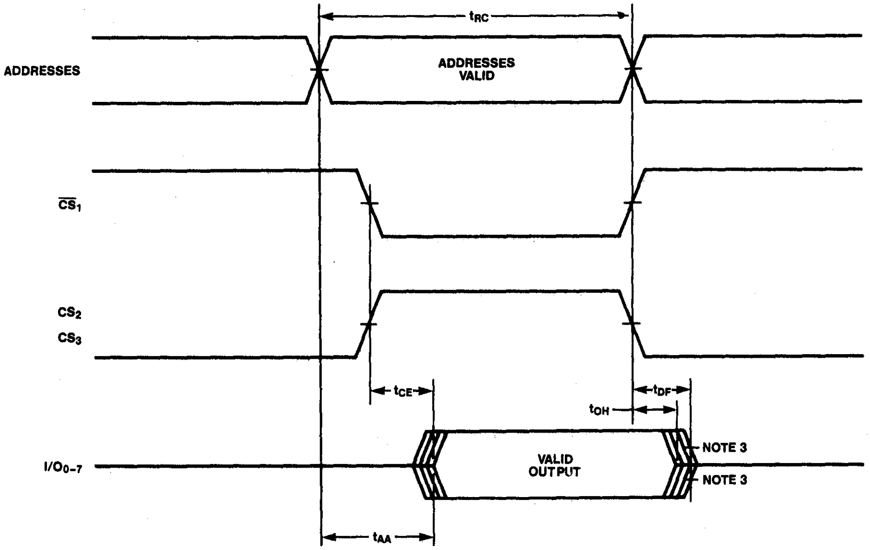
Capacitance[1] T_A=25°C, f=1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

AC Characteristics Read Operation (Over operating temperature and V_{CC} Range, unless otherwise specified)

		Limits						
		E/M36C16-45 E/M36C32-45		E/M36C16-55 E/M36C32-55		E/M36C16-70 E/M36C32-70		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
t_{RC}	Read Cycle Time	45		55		70		ns
t_{CE}	Chip Select Access Time		30		35		45	ns
t_{AA}	Address Access Time		45		55		70	ns
t_{DF}	Output Enable to Output not being Driven		25		30		35	ns
t_{OH}	Output Hold from Address Change or Chip Select whichever occurs first	0		0		0		ns

Read Cycle Timing



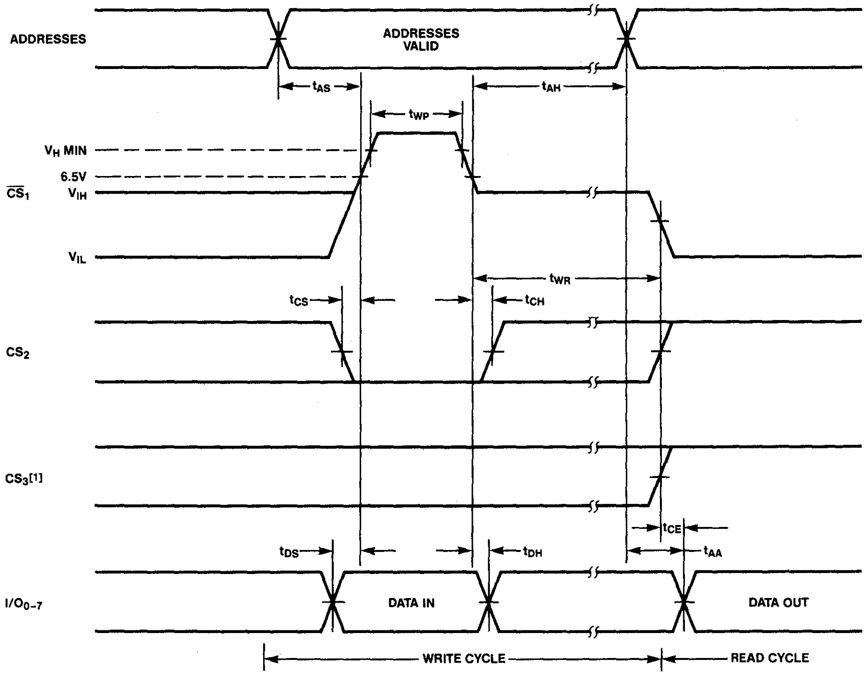
NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not Tested.
3. Transition is measured at steady state level −0.5V or steady state low level +0.5V on the output from the 1.5V level on the input.

AC Characteristics Write Operation (All Speeds)

(Over V_{CC} Range, $T_A = 25° \pm 5°C$, unless otherwise specified)

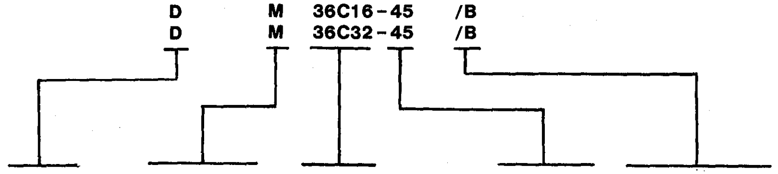
Symbol	Parameter	E/M36C16 E/M36C32 Min.	E/M36C16 E/M36C32 Max.	Units
t_{WP}	Write Pulse Width	5	50	ms
t_{AS}	Address Set-up Time	0		µs
t_{AH}	Address Hold Time	0.5		µs
t_{CS}	CS_2Set-up Time	0		µs
t_{CH}	CS_2Hold Time	0		µs
t_{DS}	Data Set-up Time	0		µs
t_{DH}	Data Hold Time	0		µs
t_{WR}	Write Recovery		10	µs

Write Cycle Timing



NOTE:
1. CS_3 is A_{11} on 36C32.

Ordering Information



PACKAGE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D-SLIM CERAMIC DIP	M--55°C to +125°C (MILITARY)	36C16-2K x 8 EEPROM	45-45 ns	/B-MIL 883 CLASS B SCREENED
L-LCC	E--40°C to +85°C (EXTENDED)	36C32-4K x 8 EEPROM	55-55 ns	
			70-70 ns	

The "Preliminary Data Sheet" designation on a SEEQ data sheet indicates that the product is not fully characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. SEEQ Technology or an authorized sales representative should be consulted for current information before using this product. No responsibility is assumed by SEEQ for its use, nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. SEEQ reserves the right to make changes in specifications at any time and without notice.

E/M38C16
E/M38C32

High Speed CMOS Electrically Erasable PROM

PRELIMINARY DATA SHEET

October, 1988

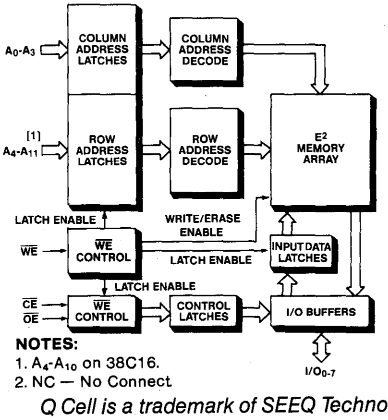
Features

- **Military and Extended Temperature Range**
  - −55°C to +125°C Operation (Military)
  - −40°C to +85°C Operation (Extended)
- **High Speed:**
  - 45 ns Maximum Access Time
- **CMOS Technology**
- **Low Power:**
  - 400 mW
- **High Endurance:**
  - 10,000 Cycles/Byte Minimum
  - 10 Year Data Retention
- **On-Chip Timer and Latches**
  - Automatic Byte Erase Before Write
  - Fast Byte Write: 5 ms/Byte
- **High Speed Address/Data Latching**
- **50 ms Chip Erase**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **$\overline{\text{DATA}}$ Polling of Data Bit 7**
- **JEDEC Approved PROM Pinout**
  - 38C16: 2816A Pin Compatible
  - 38C32: 28C64 Pin Compatible

Pin Names

A_0-A_3	ADDRESSES — COLUMN
A_4-A_{11}[1]	ROW ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE) DATA OUTPUT (READ)

Block Diagram



NOTES:
1. A_4-A_{10} on 38C16.
2. NC — No Connect.

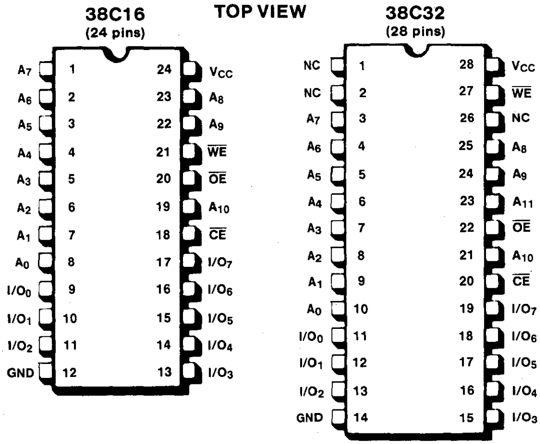
Description

SEEQ's 38C16/32 are high speed 2K x 8/4K x 8 Electrically Erasable Programmable Read Only Memories (EEPROM), manufactured using SEEQ's advanced 1.25 micron CMOS process.

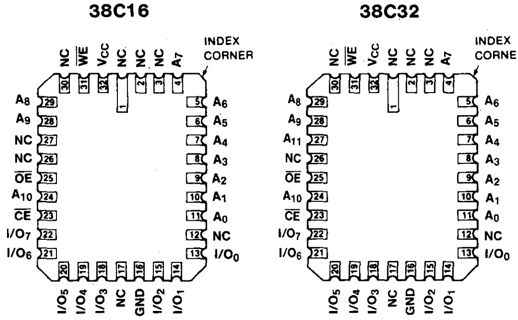
The 38C16/32 are ideal for high speed applications which require non-volatility and in-system reprogrammability. The endurance, the number of times a byte may be written, is specified to be greater than 10,000 cycles per byte minimum. The high endurance is accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative Q Cell™ design. System reliability in applications where writes are frequent is increased because of the low endurance-failure rate of the Q Cell. The 45ns maximum access time meets the requirements

Pin Configuration

DUAL-IN-LINE TOP VIEW



LEADLESS CHIP CARRIER BOTTOM VIEW



Q Cell is a trademark of SEEQ Technology, Inc.

of many of today's high performance processors. The 38C16/32 have an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. $\overline{DATA}$ Polling can be used to determine the end of a write cycle. All inputs are TTL compatible for both write and read modes.

Data retention is specified to be greater than 10 years.

The 38C16 is available in 24 pin CERAMIC DIP; the 38C32 in 28 pin CERAMIC DIP; 32 pin LCC packaged versions are also available. 24 pin versions of both 38C16 and 38C32 intended for bipolar PROM replacement are also available (36C16/36C32). All parts are available in commercial as well as military temperature ranges.

Device Operation
Operational Modes

MODE PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X V_{IH} X V_{IL}	X X V_{IL} V_{IL}	V_{IH} X V_{IH} V_{IL}	HI Z/D_{OUT} HI Z HI Z/D_{OUT} No Operation (HI Z)
Chip Erase[1]	V_{IH}	V_H[2]	V_{IH}	HI Z

X: Any TTL level

Read

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{OE}$) to a TTL low. During read, the address, $\overline{CE}$, $\overline{OE}$, and I/O latches are transparent.

NOTES:

1. Chip erase is an optional mode.
2. V_H — High Voltage.

Write

To write into a particular location, addresses must be valid and a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This initiates a write cycle. During a write cycle, all inputs except for data are latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$, whichever one occurred last). Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$, which ever one occurred first). An automatic byte erase is performed before data is written.

$\overline{DATA}$ Polling

The EEPROM has a specified t_{WC} write cycle time of 5ms. The typical device has a write cycle time faster than the t_{WC}. $\overline{DATA}$ polling is a method to indicate the completion of a timed write cycle. During the internal write cycle, the complement of the data bit 7 is presented at output 7 when a read is performed. Once the write cycle is finished, the true data is presented at the outputs. A software routine can be used to "poll", i.e. read the output, for true or complemented data bit 7. The polling cycle specifications are the same as for a read cycle. During data polling, the addresses are don't care.

Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

Power Up/Down Considerations

Protection against false write during V_{CC} power up/down is provided through on chip circuitry. Writing is prevented under any one of the following conditions:

1. *V_{CC} is less than V_{WI} V.*
1. *A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.*

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than those specified for a byte write in the Mode Selection table.

Absolute Maximum Rating

Temperature
Storage . . . . −65°C to + 150°C
Under Bias . . . . −65°C to + 135°C
All Inputs and Outputs
with Respect to Ground . . . . −3 V to + 7 V D.C.

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	M38C16 **M38C32**	**E38C16** **E38C32**
V_{CC} Supply Voltage	5 V ± 10%	5 V ± 10%
Temperature Range	(Ambient) −40°C to 85°C	(Case) −55°C to 125°C

Endurance and Data Retention

Symbol	**Parameter**	**Value**	**Units**	**Condition**
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

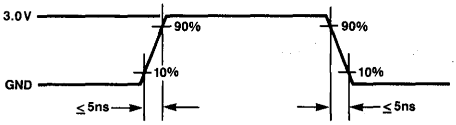
DC Operating Characteristics (Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	**Parameter**	**Limits**		**Unit**	**Test Condition**
		Min.	**Max.**		
I_{CC}	V_{CC} Active Current		80	mA	$\overline{CE} = \overline{OE} = V_{IL}$; Address Inputs = 20MHz I/O = 0mA
I_{SB}	Standby V_{CC} Current		40	mA	$\overline{CE} = V_{IH}$; All I/O open; All other inputs TTL don't care;
I_{IN}	Input Leakage Current		1	μA	0.1V > = V_{IN} < = V_{CC} Max.
I_{OUT}	Output Leakage Current		10	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2	6.5	V	V_{CC} Min.
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA, $V_{CC} = V_{CC}$ Min.
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA, V_{CC} Min.
V_{WI}[1]	Write Inhibit Voltage	3.8		V	
V_{CI}[1]	Input Undershoot Voltage	−3.0		V	V_{IN} undershoot pulse width < 10ns

NOTE:
1. Characterized. Not Tested.

AC Test Conditions

Output Load: 1 TTL gate and total $C_L = 30pF$
Input Rise and Fall Times: < 5ns
Input Pulse Levels: 0 V to 3 V
Timing Measurement Reference Level:
Inputs 1.5V
Outputs 1.5V



INPUT PULSES

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	>2000V	MIL-STD 883 Test Method 3015.3

Capacitance[1] T_A=25°C, f=1 MHz

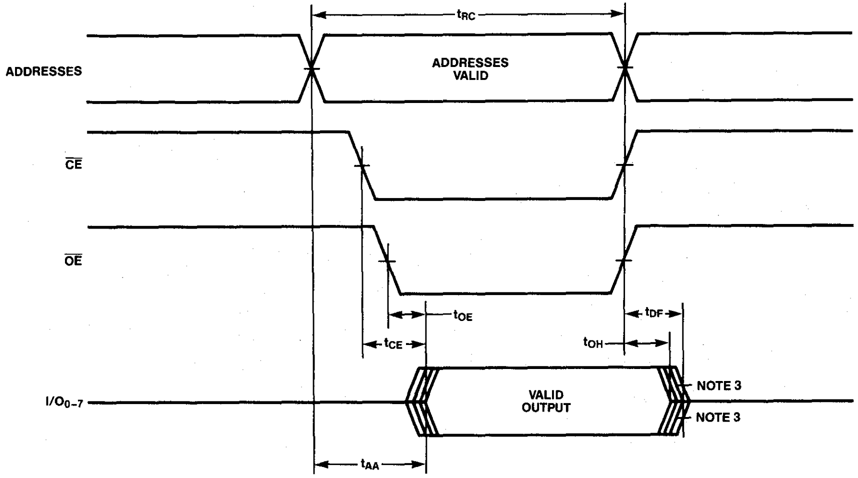
Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	6 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

AC Characteristics Read Operation

(Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	Parameter	Limits E/M38C16-45 E/M38C32-45 Min.	Limits E/M38C16-45 E/M38C32-45 Max.	Limits E/M38C16-55 E/M38C32-55 Min.	Limits E/M38C16-55 E/M38C32-55 Max.	Limits E/M38C16-70 E/M38C32-70 Min.	Limits E/M38C16-70 E/M38C32-70 Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	45		55		70		ns	$\overline{CE}=\overline{OE}=V_{IL}$
t_{CE}	Chip Enable Access Time		30		35		45	ns	$\overline{OE}=V_{IL}$
t_{AA}	Address Access Time		45		55		70	ns	$\overline{CE}=\overline{OE}=V_{IL}$
t_{OE}	Output Enable Access Time		25		30		40	ns	$\overline{CE}=V_{IL}$
t_{DF}	Output or Chip Enable to Output not being Driven		25		30		35	ns	$\overline{CE}=V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable Or Output Enable Which ever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE}=V_{IL}$

Read Cycle Timing



NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not Tested.
3. Transition is measured at steady state level −0.5V or steady state low level +0.5V on the output from the 1.5V level on the input.

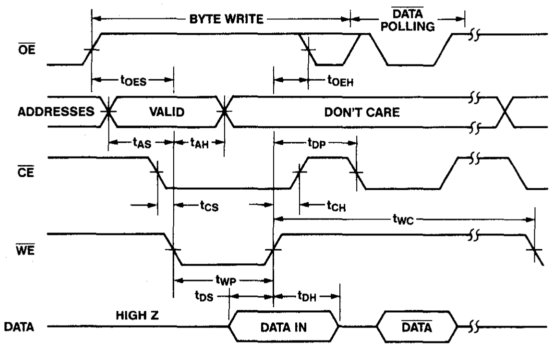
AC Characteristics Write Operation

(Over operating temperature and V_{CC} Range, unless otherwise specified)

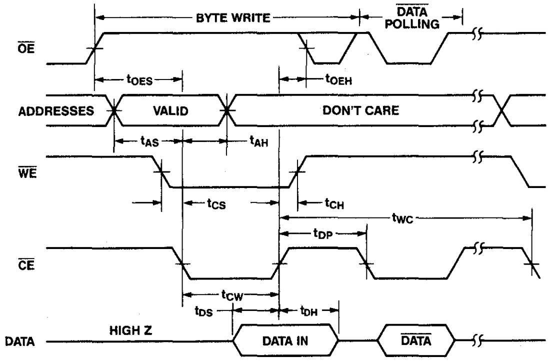
Symbol	Parameter	E/M38C16-45 E/M38C32-45 Min.	E/M38C16-45 E/M38C32-45 Max.	E/M38C16-55 E/M38C32-55 Min.	E/M38C16-55 E/M38C32-55 Max.	E/M38C16-70 E/M38C32-70 Min.	E/M38C16-70 E/M38C32-70 Max.	Units
t_{WC}	Write Cycle Time		5		5		5	ms
t_{AS}	Address Set-up Time	0		0		0		ns
t_{AH}	Address Hold Time	25		30		40		ns
t_{CS}	Write Set-up Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}	$\overline{\text{CE}}$ Pulse Width	25		30		40		ns
t_{OES}	$\overline{\text{OE}}$ High Set-up Time	5		5		5		ns
t_{OEH}	$\overline{\text{OE}}$ High Hold Time	0		0		0		ns
t_{WP}	$\overline{\text{WE}}$ Pulse Width	25		30		40		ns
t_{DS}	Data Set-up Time	25		30		40		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{DP}	Time to $\overline{\text{DATA}}$ Polling from Byte Latch		45		55		70	ns

Write Cycle Timing

$\overline{\text{WE}}$ CONTROLLED WRITE CYCLE

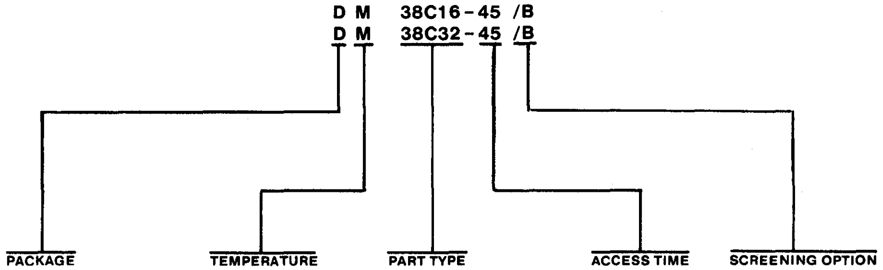


$\overline{\text{CE}}$ CONTROLLED WRITE CYCLE



NOTES:
1. Address hold time is with respect to the falling edge of the control signal $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D-CERAMIC DIP L-LCC	M--55°C to +125°C (MILITARY) E--40°C to +85°C (EXTENDED)	38C16-2K x 8 EEPROM 38C32-4K x 8 EEPROM	45-45 ns 55-55 ns 70-70 ns	/B-MIL 883 CLASS B SCREENED

seeq

MODULE M28C010
Timer E^2
1024K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1988

Features

- **CMOS Technology**
- **Military Temperature Range**
- **Low Power Operation**
  - 70 mA Active Current
  - 2 mA Standby Current
- **On-Chip Timer**
  - Automatic Erase Before Write
- **64 Byte Page Mode. . . Fast Effective Write Time**
  - 80 μsec Average Byte Write Time
- **Write Cycle Completion Indication**
  - $\overline{\text{Data}}$ Polling
- **5V± 10% Power Supply**
- **Power Up/Power Down Protection Circuitry**
- **JEDEC Approved Byte Wide Pinout**

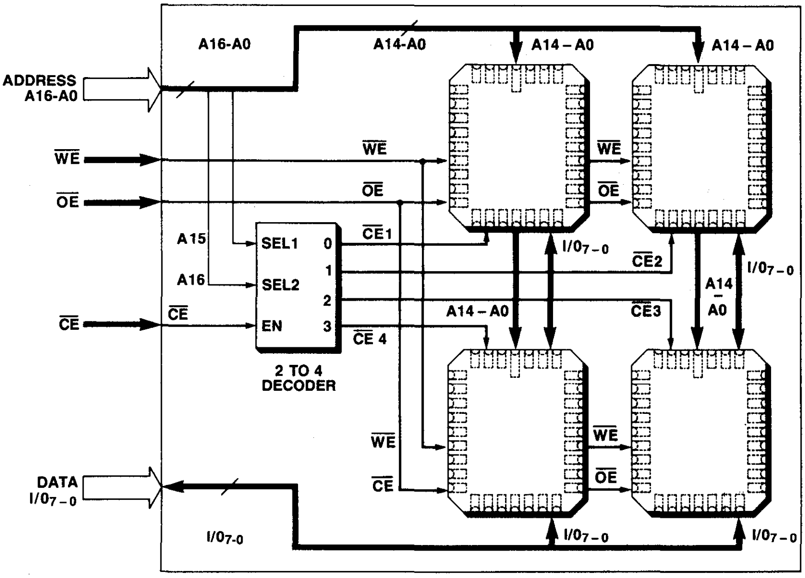
Description

SEEQ's MM28C010 is a CMOS 5V only, 128K × 8 Electrically Erasable Programmable Read Only Memory (EEPROM). The MM28C010 consists of 4 28C256 (32K × 8) CMOS EEPROMs and a 2 to 4 line decoder in LCC packages, mounted on and interconnected on a ceramic substrate. The MM28C010 is available in a 32 pin module package and is ideal for applications which require low power consumption, non-volatility and in-system reprogrammability.

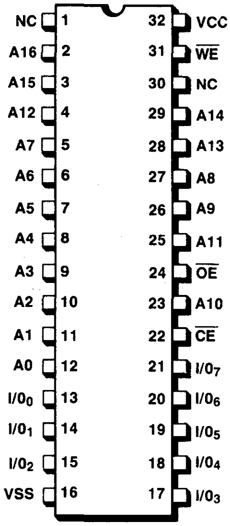
Pin Names

A16-A0	ADDRESSES
$\overline{\text{CE}}$	CHIP ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
$\overline{\text{WE}}$	WRITE ENABLE
I/O	DATA INPUT (WRITE)/DATA OUTPUT (READ)

Block Diagram



Pin Configuration



The MM28C010 has an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. The MM28C010's write cycle time is 10msec maximum. An automatic erase is performed before a write. The Data Polling feature of the MM28C010 can be used to determine the end of a write cycle. Data retention is greater than 10 years.

Device Operation

Operational Modes

There are four operational modes (see Table 1); only TTL inputs are required. Write can only be initiated under the conditions shown. Any other conditions for $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the forementioned three input lines.

Table 1

Mode Selection

Mode Pin	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
READ	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
STANDBY	V_{IH}	X	X	HI-Z
WRITE	V_{IL}	V_{IH}	V_{IL}	D_{IN}
WRITE INHIBIT	X	X	V_{IH}	HI-Z or D_{OUT}
	V_{IH}	X	X	HI-Z
	X	V_{IL}	X	HI-Z or D_{OUT}

X: any CMOS/TTL level

Reads

A read is typically accomplished by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{\text{CE}}$ is brought to a TTL low in order to enable the chip. The $\overline{\text{WE}}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{\text{OE}}$) to a TTL low. During read, the addresses, $\overline{\text{CE}}$, $\overline{\text{OE}}$, and input data latches are transparent.

Writes

To write into a particular location, addressess must be valid and a TTL low is applied to the write enable ($\overline{\text{WE}}$) pin of a selected ($\overline{\text{CE}}$ low) device. This combined with the output enable ($\overline{\text{OE}}$) being high, initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$, whichever one occurred last). Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{\text{WE}}$ (or $\overline{\text{CE}}$, whichever occurred first). An automatic erase is performed before data is written.

The MM28C010 can write both bytes and blocks of up to 64 bytes. The write mode is discussed below.

Write Cycle Control Pins

For system design simplification, the MM28C010 is designed such that either the $\overline{\text{CE}}$ or $\overline{\text{WE}}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{\text{CE}}$ or $\overline{\text{WE}}$ signal to latch the data. Address and $\overline{\text{OE}}$ set up and hold are with respect to the later of $\overline{\text{CE}}$ or $\overline{\text{WE}}$; data set up and hold is with respect to the earlier of $\overline{\text{WE}}$ or $\overline{\text{CE}}$.

To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the control pin throughout the rest of this document. Timing diagrams of both write cycles are included in the AC characteristics.

Write Mode

One to 64 bytes of data can be loaded randomly into the MM28C010. Address lines A15 and A16 must be held valid during the entire page load cycle. The part latches row addresses, A6-A14 during the first byte write. These addresses are latched on the falling edge of $\overline{\text{WE}}$ signal (assuming $\overline{\text{WE}}$ control write cycle) and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5 which are used to write into different locations of the page, are latched every time a new write is initiated. These addresses along with $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the MM28C010 latches data and starts the internal page loader timer. The timer is reset on the falling edge of $\overline{WE}$ signal if a write is initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no more write cycles have been initiated in (t_{BLC}) after the last $\overline{WE}$ low to high transition, the part terminates page load cycle and starts the internal write. During this time, which takes a maximum of 10ms, the device ignores any additional load attempts. The part can be now read to determine the end of write cycle ($\overline{DATA}$ Polling). A 160μs maximum effective byte write time can be achieved if the page is fully utilized.

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the MM28C010 permits an extended page load cycle. To do this, the write cycle must be 'stretched' by maintaining $\overline{WE}$ low, assuming a write enable controlled cycle and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will inhibit the page load timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

$\overline{\text{Data}}$ Polling

The MM28C010 has a maximum write cycle time of 10ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual end point of a write cycle. If a read is performed to any address while the MM28C010 is still writing, the device will present the Ones-complement of the last data byte written. When the MM28C010 has completed its write cycle, a read from the last address written will result in valid data. Thus software can simply read from the part until the last data byte written is read correctly. A $\overline{DATA}$ polling read should not be done until a minimum of t_{LP} microseconds after the last byte is written. Timing for a $\overline{DATA}$ polling read is the same as a normal read once the t_{LP} specifications have been met.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during V_{CC} power up or down. This circuitry prevents writing under any one of the following conditions:

1. *V_{CC} is less than V_{WI} V.*
2. *A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.*

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

*Absolute Maximum Stress Range**

Temperature
Storage. . . . . −65°C to +150°C
Under Bias. . . . . −65°C to +135°C
All Input or Output Voltages
with Respect to V_{SS}. . . . . +6 V to −0.5 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	MM28C010
Temperature Range	−55°C to +125°C (case temp.)
V_{CC} Power Supply	5 V ± 10%

Endurance and Data Retention

Symbol	**Parameter**	**Value**	**Units**	**Condition**
N K	Minimum Endurance[4]	10,000 1,000	Cycles/Byte	MIL-STD 833 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 833 Test Method 1008

DC Charateristics Read Operation

(Over operating temperature and V_{CC} Range, unless otherwise specified)

Symbol	**Parameter**	**Limits**		**Units**	**Test Condition**
		Min.	**Max.**		
I_{CC}	Active V_{CC} Current		70	mA	$\overline{CE} = \overline{OE} = V_{IL}$; All I/O = 0 ma; Addr = 5MHz
I_{SB_1}	Standby V_{CC} Current (TTL Inputs)		10	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$; All I/O = 0 ma;
I_{SB_2}	Standby V_{CC} Current (CMOS Inputs)		2	mA	$\overline{CE} = V_{CC} - 0.2$; A15, A16 = $V_{CC} - 0.2$ Other Inputs = V_{IH} All I/O = 0 ma
I_{IL}[2]	Input Leakage Current		5	μA	$V_{IN} = V_{CC}$ Max.
I_{OL}[3]	Output Leakage Current		25	μA	$V_{OUT} = V_{CC}$ Max.
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400$ μA
V_{WI}[1]	Write Inhibit Voltage	3.8		V	

NOTES:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.
3. For I/O only.
4. Endurance can be specified as an option to be 1000 or 10000 cycles/byte minimum.

AC Test Conditions

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: < 10 ns
Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

Capacitance[1] $T_A = 25°C$, t = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	30 pF	$V_{IN} = 0V$
C_{OUT}	Data (I/0) Capacitance	40 pF	$V_{I/0} = 0V$

E.S.D. Characteristics

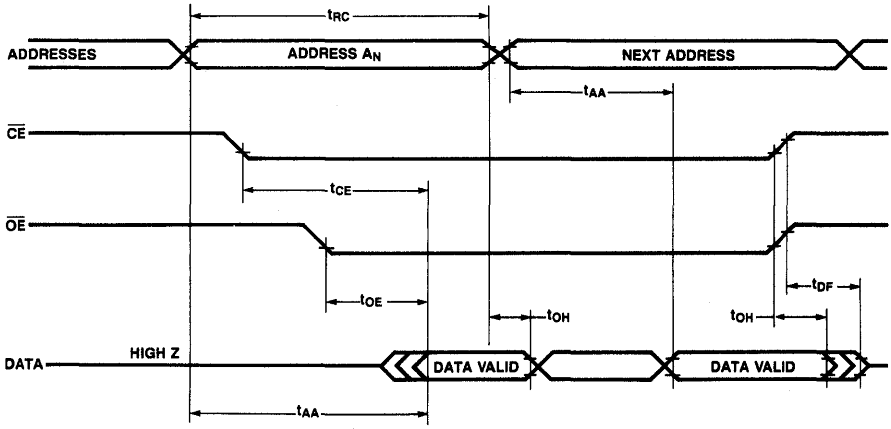
Symbol	Parameter	Value	Test Conditions
V_{ZAP}[2]	E.S.D. Tolerance	> 1000 V	M_{IL} = STD 883 Test Method 3015

AC Characteristics Read Operation

(Over operating temperature and V_{CC} range, unless otherwise specified)

		Limits							
		MM28C010-250		MM28C010-300		MM28C010-350			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units	Test Conditions
t_{RC}	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
t_{AA}	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t_{OE}	Output Enable Access Time		150		150		150	ns	$\overline{CE} = V_{IL}$
t_{DF}	Output or Chip Enable High to Output in Hi-Z	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

Read/$\overline{DATA}$ Polling Cycle



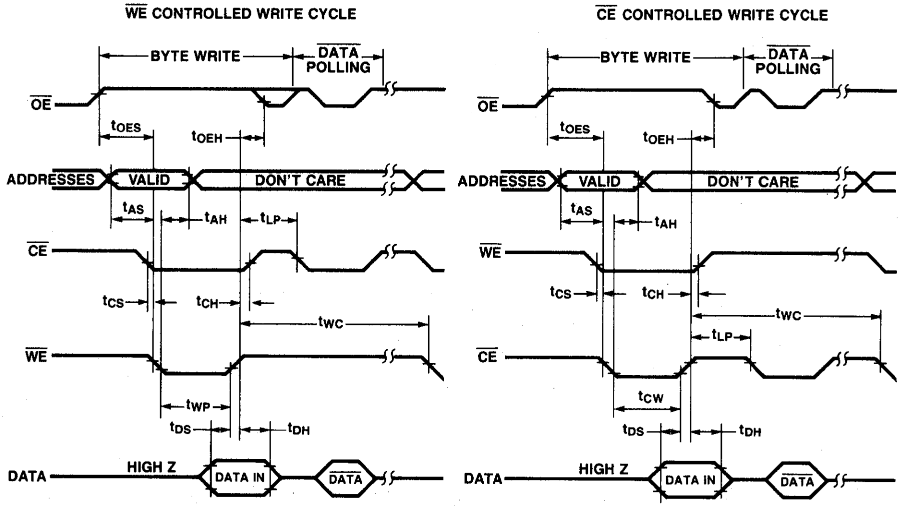
NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

AC Characteristics Write Operation

(Over the operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits						Units
		MM28C010-250		MM28C010-300		MM28C010-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Set-up Time	20		20		20		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (see note 2)	150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	20		20		20		ns
t_{OEH}	$\overline{OE}$ High Hold Time	20		20		20		ns
t_{WP}	$\overline{WE}$ Pulse Width (see note 2)	150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (see note 3)	0.2	200	0.2	200	0.2	200	μs
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		1		1		1	ms

Write Timing

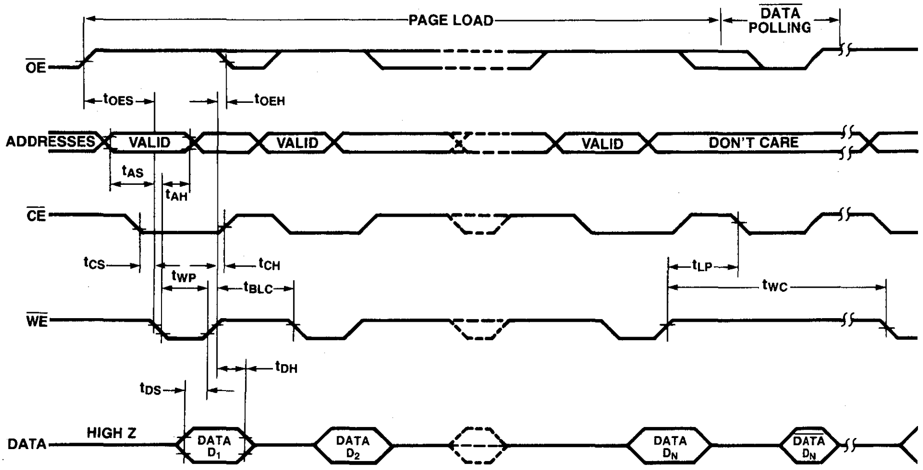


$\overline{WE}$ CONTROLLED WRITE CYCLE

$\overline{CE}$ CONTROLLED WRITE CYCLE

NOTES:
1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing



Ordering Information

M M 28C010 K -250 **MP**

PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ENDURANCE	ACCESS TIME	SCREENING OPTION
M – MODULE	M – 55°C to + 125°C (Military)	128K × 8 EEPROM	K = 1000 Cycles N = 10000 Cycles	250 = 250 ns 300 = 300 ns 350 = 350 ns	MILITARY PROCESSED MODULE COMPONENTS MIL 883 CLASS B SCREENED

M2764/M27128

(Military Temperature Range)

E2764/E27128

(Extended Temperature Range)

2764/27128 EPROM

March 1987

Features

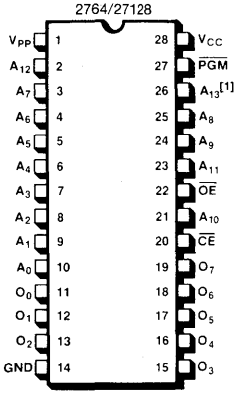
- **Military and Extended Temperature Range**
  - **−55° to +125°C: M2764**
  - **−55° to +125°C: M27128**
  - **−40° to +85°C: E2764/E27128**
- **200 ns Access Times at −55° to 125°C**
- **Programmed Using Intelligent Algorithm**
- **21 V V_{PP} Programming Voltage**
- **JEDEC Approved Bytewide Pin Configuration**
  - **2764 8K x 8 Organization**
  - **27128 16K x 8 Organization**
- **Low Power Dissipation**
  - **120 mA Active Current**
  - **40 mA Standby Current**
- **Silicon Signature®**

Description

SEEQ's 2764 and 27128 are ultraviolet light erasable EPROMs which are organized 8K x 8 and 16K x 8 respectively. They are specified over the military and extended temperature range and have access times as fast as 200 ns over the V_{CC} tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 120 mA and 40 mA respectively. The 200 ns allows higher system efficiency by eliminating the need for wait states in today's 8 - or 16-bit microprocessors.

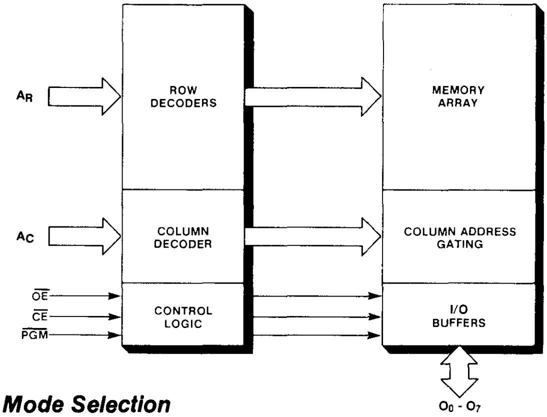
Pin Configurations

DUAL-IN-LINE
TOP VIEW



PIN 26 IS A NO CONNECT
ON THE DIP 2764

Block Diagram



Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon Signature™*	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}

* For Silicon Signature: A_0 is toggled, A_9 = 12V, and all other addresses are at TTL low.
Silicon Signature is a registered trademark of SEEQ Technology.

Pin Names

A_C	ADDRESSES — COLUMN (LSB)
A_R	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS
$\overline{PGM}$	PROGRAM

Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to V_{PP} and a TTL "0" to pin 27 (program pin). They may be programmed with an intelligent algorithm that is now available on commercial programmers. This faster time improves manufacturing throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, the 27128 and the 2764 may be programmed using the conventional 50 ms programming specification of older generation EPROMs.

Incorporated on the 27128 and 2764 is Silicon Signature . Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage .... -65° C to +150° C
Under Bias .... -65° C to +135° C
All Inputs or Outputs with
Respect to Ground .... +6V to −0.3V
V_{PP} During Programming with
Respect to Ground .... +22V to −0.3V
Voltage on A_9 with
Respect to Ground .... +15.5V to −0.3V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M2764 **M27128**	**E2764** **E27128**
V_{CC} Supply Voltage[1]	5 V ± 10%	5 V ± 10%
Temperature Range (Read Mode)	(Case) −55° to 125°C	(Ambient) −40° to 85°C
V_{PP} During Programming	21 ± 0.5 V	21 ± 0.5 V

DC Operating Characteristics During Read or Programming

Symbol	**Parameter**		**Limits**		**Unit**	**Test Conditions**
			Min.	**Max.**		
I_{IN}	Input Leakage Current			10	μA	$V_{IN} = V_{CC}$ Max.
I_O	Output Leakage Current			10	μA	$V_{OUT} = V_{CC}$ Max.
I_{PP}[2]	V_{PP} Current	Read Mode		5	mA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode (25° C)		30	mA	$V_{PP} = 21.5V$
I_{CC1}[2]	V_{CC} Standby Current			40	mA	$\overline{CE} = V_{IH}$
I_{CC2}[2]	V_{CC} Active Current			120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL}	Input Low Voltage		-0.1	0.8	V	
V_{IH}	Input High Voltage		2	$V_{CC} + 1$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage		2.4		V	$I_{OH} = -400$ μA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current is the sum of I_{CC} and I_{PP}.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)								Test Conditions
		E/M2764-20 E/M27128-20		E/M2764-25 E/M27128-25		E/M2764-35 E/M27128-35		M2764-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address Access Time		200		250		350		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid		200		250		350		450	$\overline{OE} = V_{IL}$
t_{OE}[2]	Output Enable to Data Valid		75		100		125		150	$\overline{CE} = V_{IL}$
t_{DF}[3]	Output Enable to Output Float	0	60	0	85	0	105	0	130	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable, whichever occurred first	0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

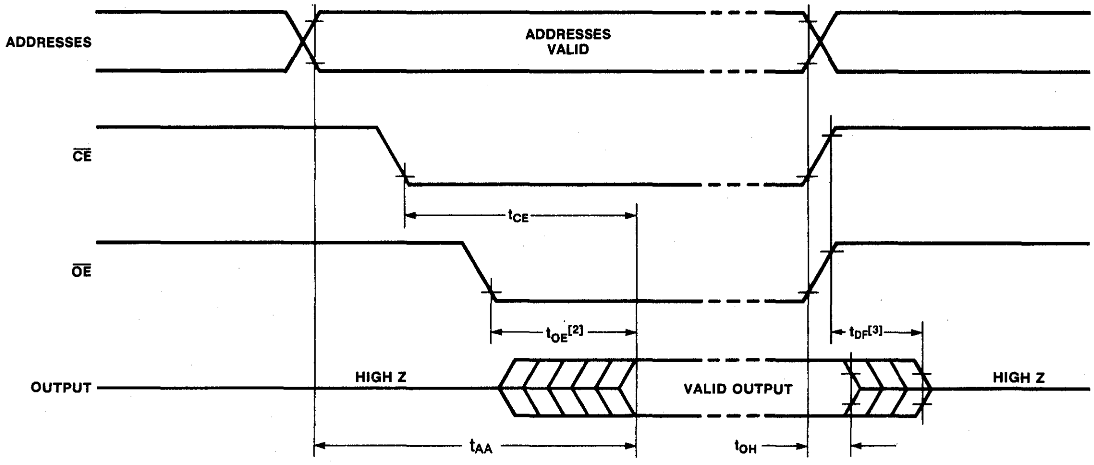
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Equivalent A.C. Test Conditions[4]

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{AA} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{AA}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

Erasure Characteristics

The 2764 and 27128 are erased using ultraviolet light which has a wavelenght of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm². The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm²)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. Silicon Signature allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds programming.

Silicon Signature is activated by raising address A_9 to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling (using TTL) the column address A_0. There are 2 bytes of data available. The data (see Table 2) appears on outputs O_0 to O_6, with O_7 used as an odd parity bit. This mode is functional at 25° ± 5°C ambient temperature.

Table 2. Silicon Signature Bytes

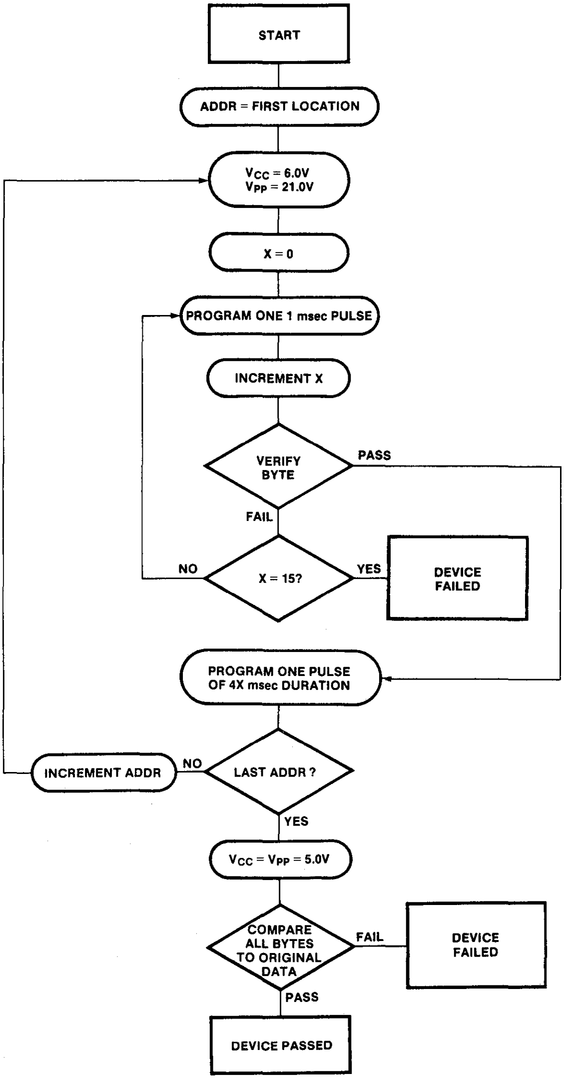
	A_0	Data (Hex)
SEEQ Code (Byte 0)	**V_{IL}**	**94**
Product Code (Byte 1)		
2764	V_{IH}	40
27128	V_{IH}	C1

Programming

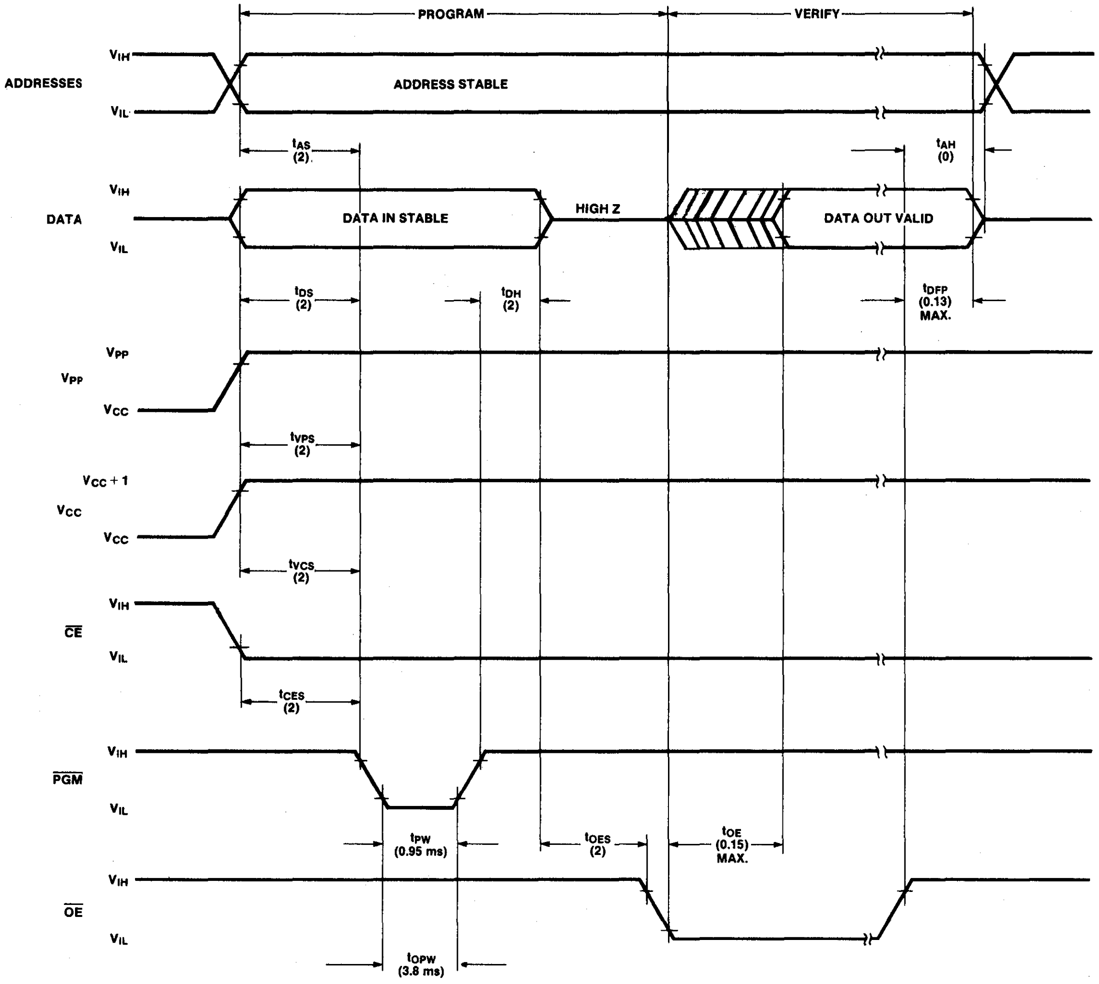
The EPROMs may be programmed using an intelligent algorithm or with a conventional 50 msec programming pulse. The intelligent algorithm improves the total programming time by approximately 10 times over the conventional 50 msec algorithm.

The intelligent algorithm requires V_{CC} = 6V and V_{PP} = 21V during byte programming. The initial program pulse width is one millisecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 4 times the number of one millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A maximum of 15 one millisecond pulses per byte should be applied to each address. When the intelligent algorithm cycle has been completed, all bytes must be read at V_{CC} = V_{PP} = 5V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A V_{IL} AND 2V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.

Intelligent Algorithm

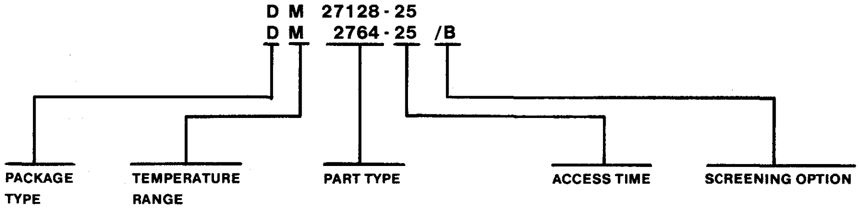
AC Programming Characteristics $T_A = 25° \pm 5°C$, V_{CC}[1,4] $= 6.0V \pm 0.25V$, $V_{PP} = 21V \pm 0.5V$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			μs
t_{OES}	OE Setup Time	2			μs
t_{DS}	Data Setup Time	2			μs
t_{AH}	Address Hold Time	0			μs
t_{DH}	Data Hold Time	2			μs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			μs
t_{VCS}	V_{CC} Setup Time	2			μs
t_{PW}[2]	$\overline{\text{PGM}}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[3, 4]	$\overline{\text{PGM}}$ Overprogram Pulse Width	3.8		63	ms
t_{CES}	$\overline{\text{CE}}$ Setup Time	2			μs
t_{OE}	Data Valid from $\overline{\text{OE}}$			150	ns

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Initial Program Pulse width tolerance is 1 msec ± 5%.
3. The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
4. For 50 ms programming, $V_{CC} = 5\ V \pm 5\%$, $T_{PW} = 50$ ms ± 10%, and T_{OPW} is not applicable.

Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D-Cerdip	M--55°C to +125°C (Military) E--40°C to +85°C (Extended)	2764-8K x 8 EPROM 27128-16K x 8 EPROM	20-200 ns 25-250 ns 35-350 ns 45-450 ns	MIL 883 CLASS B SCREENED

seeq

M27C256/E27C256
256K CMOS EPROM

September 1988

Features

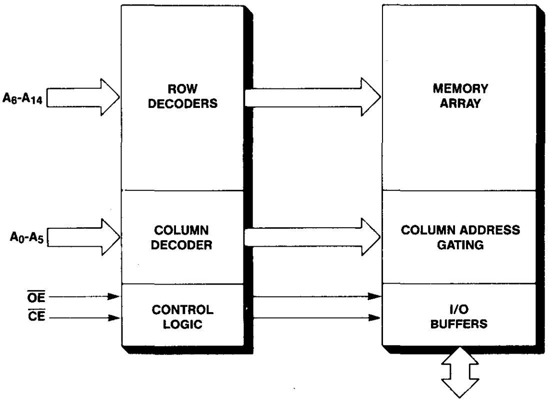
- **256K (32K x 8) CMOS EPROM**
- **Military and Extended Temperature Range**
  - −55° to +125°C: M27C256
  - −40° to +85°C: E27C256
- **Ultra Low Power**
  - 150 μA Max. V_{CC} Standby Current
  - 50 mA Max. Active Current
- **Programmed Using Intelligent Algorithm**
  - 12.5 V V_{PP}
- **200 ns Access Times**
- **5 V±10% V_{CC}**
- **JEDEC Approved Bytewide Pin Configuration**
- **Silicon Signature®**

Description

SEEQ's 27C256 is the industry's first 256K CMOS EPROM. It has a 32K x 8 organization and has very low power dissipation. Its active current is less than one half the active power of n-channel EPROMs. In addition the standby current is orders of magnitude lower than those same EPROMs. Consequently, system memory sizes can be substantially increased at a very small increase in power. Low active and standby power is important in applications which require portability, low cooling cost, high memory bit density, and long term reliability.

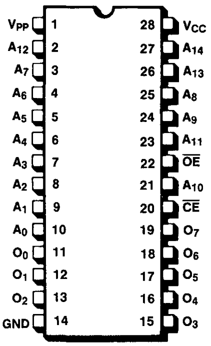
The 27C256 is specified over both the extended and military temperature ranges at 5 V±10% V_{CC}. The access time is specified at 200 ns, making the 27C256 compatible with most of today's microprocessors. Its inputs and outputs are completely TTL compatible.

Block Diagram

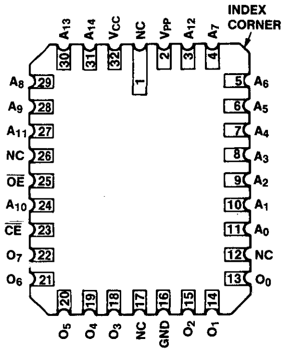


Pin Configuration

DUAL IN-LINE



LEADLESS CHIP CARRIER BOTTOM VIEW



Mode Selection

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	DOUT
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	V_{CC}	DIN
Program Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	DOUT
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z
Silicon Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}.

*For Silicon Signature: A_0 is toggled, A_9 = 12 V, and all other addresses are at a TTL low.

Silicon Signature is a registered trademark of SEEQ Technology.

Pin Names

A_0 - A_5	ADDRESSES — COLUMN (LSB)
A_6 - A_{14}	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS
NC	NO CONNECT

Initially, and after erasure, all bits are in the "1" state. An intelligent algorithm is used to program the 27C256 typically in four minutes. Data is programmed using a 12.5 V Vpp and an inital chip enable pulse of 1.0 ms.

Incorporated on the 27C256 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. This data is encoded in ROM to prevent erasure by ultraviolet light.

Absolute Maximum Ratings

Temperature
Storage .... −65°C to +150°C
M27C256 Under Bias .... −65°C to +135°C
E27C256 Under Bias .... −50°C to +95°C
All Inputs or Outputs with
Respect to Ground .... +6 V to −0.3 V
V_{PP} with Respect to Ground .... +14.0 V to −0.3 V
Voltage on A_9 with
Respect to Ground .... +14.0 V to −0.3 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	M27C256-20, M27C256-25, M27C256-30	E27C256-20, E27C256-25, E27C256-30
V_{CC} Supply Voltage[1]	5 V ± 10%	5 V ± 10%
Temperature Range (Read Mode)	(Case) −55°C to +125°C	(Ambient) −40°C to 85°C
V_{PP} During Read[2]	V_{CC}	V_{CC}
V_{PP} During Programming[3]	12.5 ± 0.3 V	12.5 ± 0.3 V

DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits Min.	Limits Max.	Unit	Test Condition
I_{IN}[4]	Input leakage		1	μA	$V_{IN}=V_{CC}$ Max.
I_O[5]	Output leakage		10	μA	$V_{OUT}=V_{CC}$ Max.
I_{PP}	V_{PP} current: Standby mode Read Mode Programming mode		 150 1 30	 μA mA mA	 $\overline{CE}=V_{CC}-1$ v. min. F=5 MHz., $\overline{CE}=V_{IL}$ $V_{PP}=12.5$ v.
I_{CC1}	V_{CC} standby current		150	μA	$\overline{CE}>=V_{CC}-1$ v.
I_{CC2}	V_{CC} standby current		2	mA	$\overline{CE}=V_{IH}$
I_{CC3}	V_{CC} active current		50	mA	$\overline{CE}=\overline{OE}=V_{IL}$, $O_{0-7}=0$, F=5 MHz.
V_{IL}	Input low voltage	−0.1	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC}+1$	V	
V_{OL}	Output low voltage		0.45	V	$I_{OL}=2.1$ ma.
V_{OH}	Output high voltage	2.4		V	$I_{OH}=-400$ μA.

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} cannot be left floating and should be connected to V_{CC} during read.
3. 0.1 μF ceramic capacitor on V_{PP} is required during programming only, to suppress voltage transients.
4. Inputs only. Does not include I/O.
5. For I/O only.

AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)						Test Conditions
		M27C256-20 E27C256-20		M27C256-25 E27C256-25		M27C256-30 E27C256-30		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address Access Time		200		250		300	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	Chip Enable to Data Valid		200		250		300	$\overline{OE} = V_{IL}$
$t_{OE}^{(2)}$	Output Enable to Data Valid		75		100		120	$\overline{CE} = V_{IL}$
$t_{DF}^{(3)}$	Output Enable or Chip Enable to Output Float		60		60		105	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

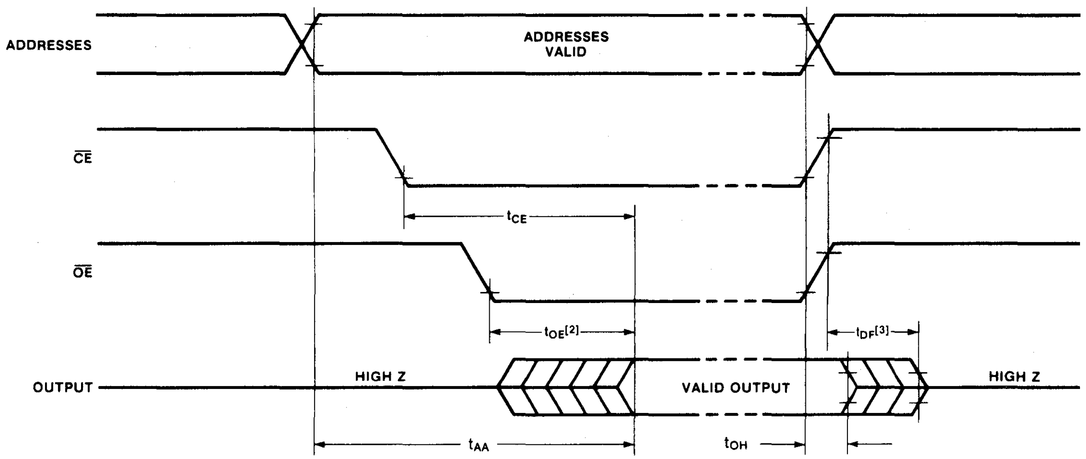
Capacitance[1]

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Equivalent A.C. Test Conditions[4]

Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A.C. Waveforms



NOTES:
1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2. $\overline{OE}$ MAY BE DELAYED TO $t_{AA} - t_{OE}$ AFTER THE FALLING EDGE OF $\overline{CE}$ WITHOUT IMPACT ON t_{AA}.
3. t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{CE}$, WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

Erasure Characteristics

The 27C256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm^2. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allow programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A_9 to 12V±0.5V, bringing chip enable and output enable to a TTL low, having V_{CC} at 5V, and having all addresses except A_0 at a TTL low. The Silicon Signature data is then accessed by toggling A_0. The data appears on outputs 0_0 to 0_6, with 0_7 used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

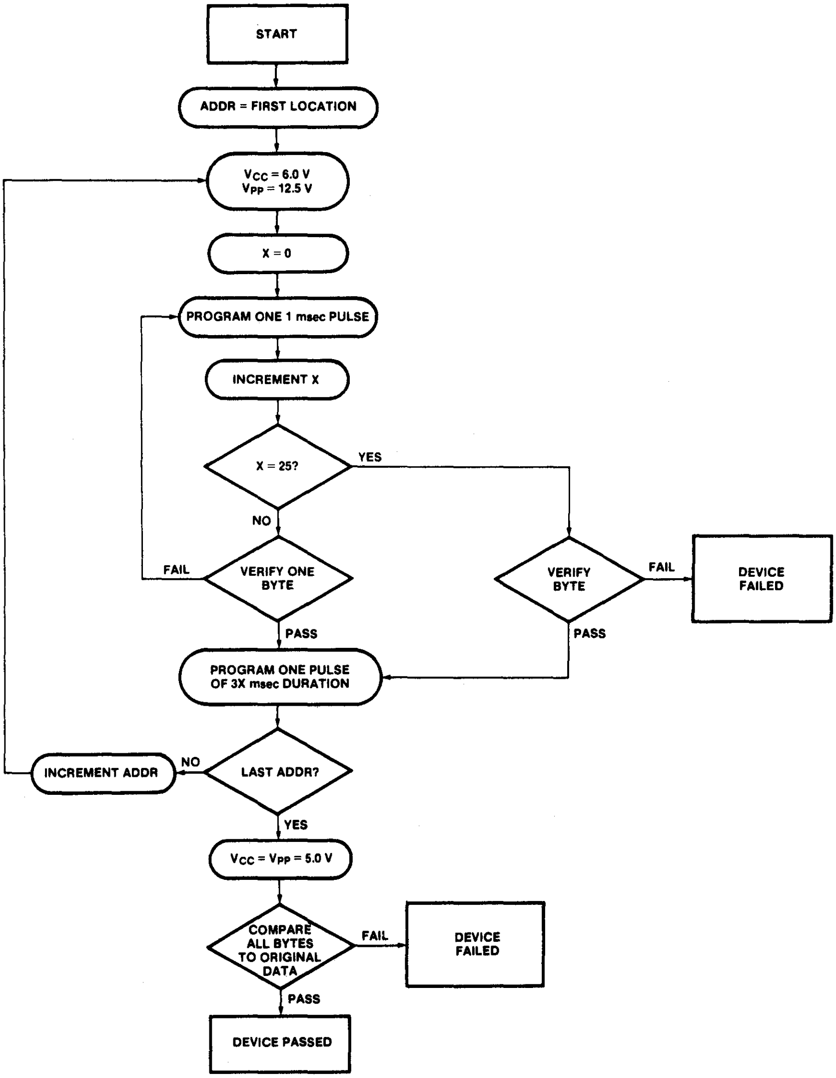
	A_0	Data (Hex)
SEEQ Code (Byte 0)	V_{IL}	94
Product Code (Byte 1)	V_{IH}	C2

Programming

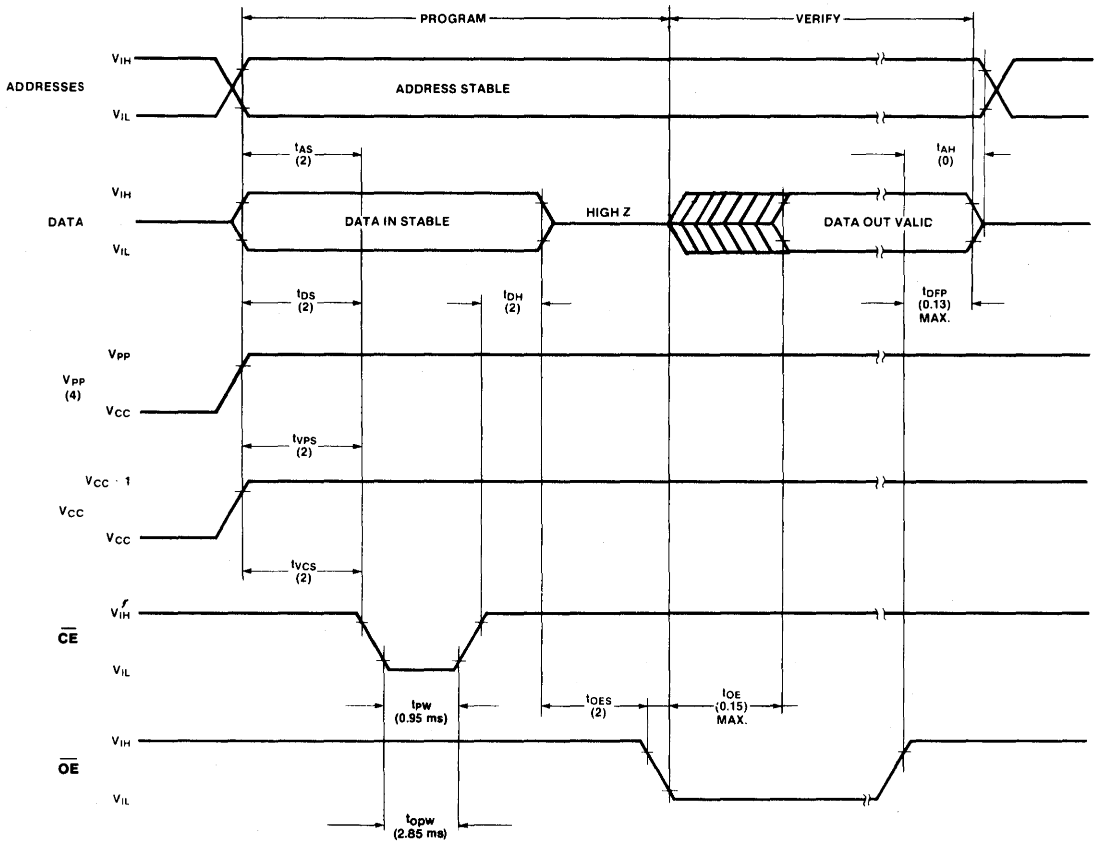
The 27C256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires V_{CC}=6 V and V_{PP}=12.5 V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X over-pulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at V_{CC}=V_{PP}=5 V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:
1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN μSEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A V_{IL} AND 2 V FOR A V_{IH}.
3. t_{OE} AND t_{DFP} ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. 0.1 μF CERAMIC CAPACITOR ON V_{PP} IS REQUIRED DURING PROGRAMMING ONLY, TO SUPPRESS VOLTAGE TRANSIENTS.

Intelligent Algorithm

AC Programming Characteristics $T_A = 25° \pm 5°C$, V_{CC}[1] $= 6.0V \pm 0.25V$. $V_{PP} = 12.5V$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AS}	Address Setup Time	2			µs
t_{OES}	$\overline{OE}$ Setup Time	2			µs
t_{DS}	Data Setup Time	2			µs
t_{AH}	Address Hold Time	0			µs
t_{DH}	Data Hold Time	2			µs
t_{DFP}	Output Enable to Output Float Delay	0		130	ns
t_{VPS}	V_{PP} Setup Time	2			µs
t_{VCS}	V_{CC} Setup Time	2			µs
t_{PW}	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
t_{OPW}[2]	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
t_{OE}	Data Valid from $\overline{OE}$			150	ns

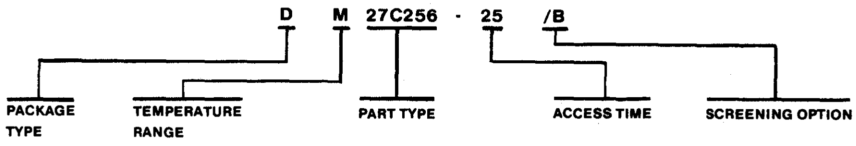
AC Conditions of Test

Input Rise and Fall Times (10% to 90%) .... 20 ns
Input Pulse Levels .... 0.45 V to 2.4 V
Input Timing Reference Level .... 0.8 V and 2.0 V
Output Timing Reference Level ... 0.8 V and 2.0 V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

Ordering Information



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D-Cerdip L-LCC	M--55°C to +125°C (Military) E--40°C to +85°C (Extended)	32K x 8 EPROM	20 - 200 ns 25 - 250 ns 30 - 300 ns	MIL 883 CLASS B SCREENED

82005
MILITARY DRAWING 64K UV EPROM

May 1988

Features

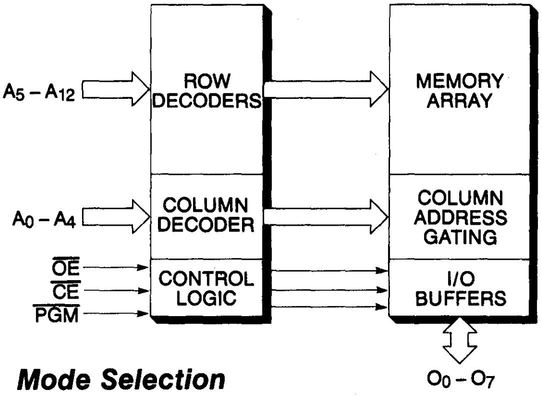
- **82005 Military Drawing Compliant**
- **Processing Per Method 5004/5005 MIL-STD-883**
- **21-Volt Programming**
- **JEDEC-Approved Bytewide Pin Configuration**
- **200 ns Access Time**
- **MIL-M-38510 Compliant Package Design**
- **Programmed Using Intelligent Algorithm**
- **Silicon Signature®**

Description

SEEQ's 82005 is a military drawing compliant, 21-volt programming, 65,532-bit (8192 × 8), ultraviolet erasable EPROM. The 64K EPROM is fabricated and tested in SEEQ Technology's DESC-approved manufacturing facility and has been processed per the requirements of Method 5004/5005 of MIL-STD-883. The 82005 EPROM provides continuing support for applications which utilize a 21-volt programming 64K EPROM in their design.

Using the 82005 will satisfy MIL-STD-454K which dictates the use of military drawing parts over 883C compliant parts if they are available. Furthermore, designing with standard military drawing devices eliminates the need for customer-generated source control drawings, while ensuring the highest level of device reliability.

Block Diagram



Mode Selection

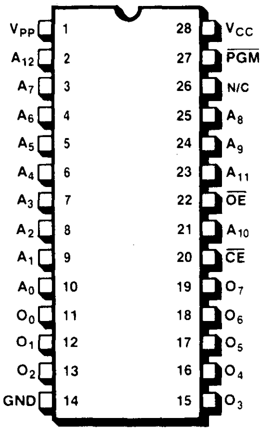
PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon Signature*	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}

*For Silicon Signature: A_0 is toggled, $A_9 = 12V$, and all other addresses are at a TTL low.

Silicon Signature is a registered trademark of SEEQ Technology.

Pin Configuration



Pin Names

A_0-A_4	ADDRESSES—COLUMN
A_5-A_{12}	ADDRESSES—ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM

Description (cont.)

The 82005 is manufactured using JEDEC approved bytewide pinouts and 28-pin package. Access times as fast as 200 ns eliminate the need for wait states in high-performance microprocessor systems. Programming can be accomplished using either the intelligent algorithm or the 50 ms/byte algorithm available on commercial programmers.

Quality-Assurance Provisions

Quality-assurance screening for the 82005 is performed on 100% of the devices in accordance with Method 5004 of MIL-STD-883. In addition, burn-in (Method 1015, 125°C min) and data retention bake are performed on each device after Method 5004 screening and prior to submitting for quality conformance inspection testing.

Quality-Conformance Inspection

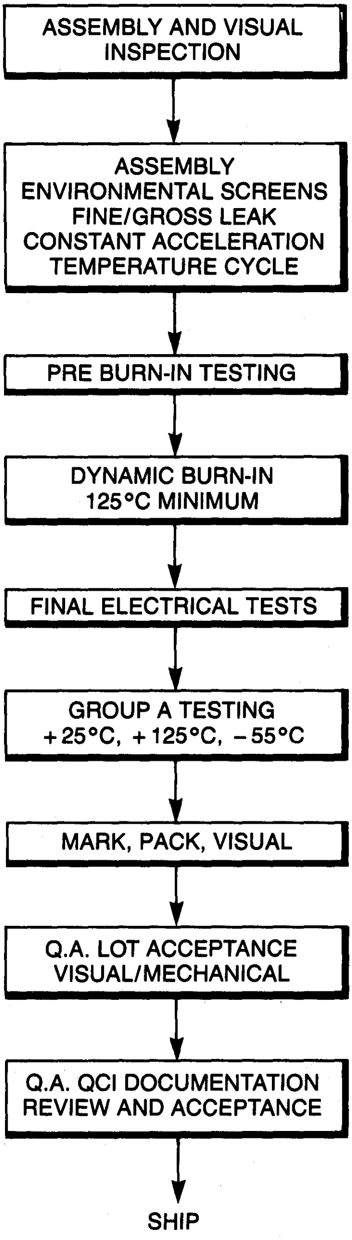
Quality-conformance inspection is performed in accordance with Method 5005 of MIL-STD-883. This includes Group A, Group B, Group C, and Group D inspections tests as defined in military drawing 82005. Generic QCI summary data will be provided upon request.

Electrical Performance Characteristics

The 82005 can be ordered from SEEQ Technology with device access times = 200 ns (82005-07), 250 ns (82005-02), and 450 ns (82005-01). Details on device specific electrical performance can be found in the complete DESC 82005 military drawing or SEEQ's data sheet for generic part type DM2764. SEEQ's testing meets or exceeds all electrical performance screening and test limits as specified on the 82005 military drawing.

82005 Assembly/Test Flow Chart

Screening per MIL-STD-883 Method 5004 and quality-conformance acceptance per Method 5005



Programming

The 82005 may be programmed using an interactive intelligent algorithm or with a conventional 50 ms/byte programming pulse. Use of the intelligent algorithm improves the total device programming time by approximately 10 times over the 50 ms/byte algorithm.

To program using the intelligent algorithm requires $V_{CC} = 6V$, $V_{PP} = 21V$, *and* $\overline{CE} = V_{IL}$. *The initial programming pulse applied to the* $\overline{PGM}$ *pin is one millisecond in duration, followed by a byte verification. Additional one millisecond program pulses are applied and checked until the byte passes verification. After verification, an overprogram pulse equal to 4X the number of one millisecond pulses required to initially program the byte is applied to the address. A maximum of 15 one millisecond pulses per byte is allowed. When the intelligent programming cycle has been completed, all bytes must be read with* $V_{CC} = V_{PP} = 5.0$ *volts to verify correct programming.*

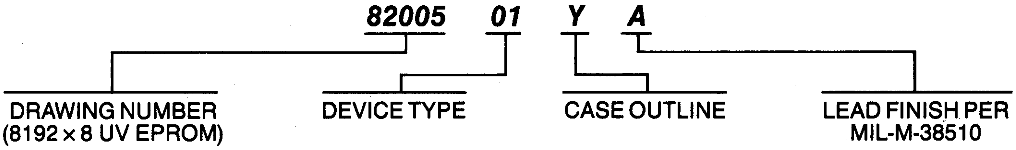
Erasure Characteristics

The 82005 is erased by exposure to high-intensity ultraviolet light with a wave length of 2537 angstroms. The minimum integrated dose for erasure (i.e. intensity × exposure time) is 15 watt-second/cm^2. *The device should be placed within one inch of the lamp tube during erasure. After erasure, all bits are in the high state.*

Silicon Signature

Incorporated in SEEQ's 82005 EPROM is a row of mask-programmed read-only memory (ROM) cells, located outside of the normal memory cell array. These ROM cells contain the EPROM's Silicon Signature. Silicon Signature identifies SEEQ as the manufacturer and gives the device's product code for programming. This allows the programmer to match the product to be programmed with the correct programming specification. Once the device code and programming specification have been verified, programming of the part can proceed.

Ordering Information



Device Type	Generic Number	Access Time
01	2764-45	450 ns
02	2764-25	250 ns
07	2764-20	200 ns

Case Outline
Y = D-10 (28 PIN, 1/2″ × 1-3/8″), DUAL-IN-LINE PACKAGE

Lead Finish
A = HOT SOLDER DIPPED

seeq

82025
MILITARY DRAWING 128K UV EPROM

May 1988

Features

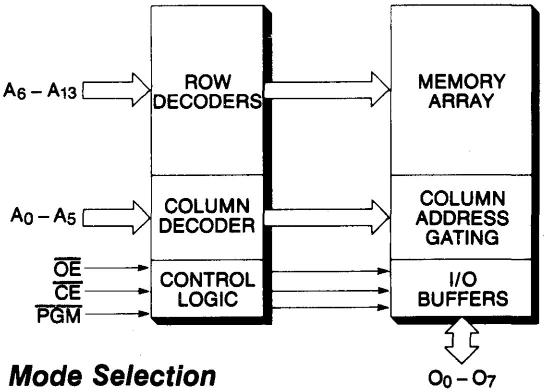
- ***82025 Military Drawing Compliant***
- ***Processing Per Method 5004/5005 MIL-STD-883***
- ***21-Volt Programming***
- ***JEDEC-Approved Bytewide Pin Configuration***
- ***200 ns Access Time***
- ***MIL-M-38510 Compliant Package Design***
- ***Programmed Using Intelligent Algorithm***
- ***Silicon Signature®***

Description

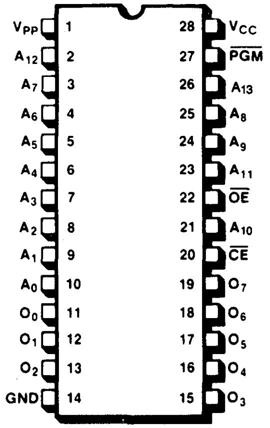
SEEQ's 82025 is a military drawing compliant, 21-volt programming, 131,064-bit (16,384 × 8), ultraviolet erasable EPROM. The 128K EPROM is fabricated and tested in SEEQ Technology's DESC-approved manufacturing facility and has been processed per the requirements of Method 5004/5005 of MIL-STD-883. The 82025 EPROM provides continuing support for applications which utilize a 21-volt programming 128K EPROM in their design.

Using the 82025 will satisfy MIL-STD-454K which dictates the use of military drawing parts over 883C compliant parts if they are available. Furthermore, designing with standard military drawing devices eliminates the need for customer-generated source control drawings, while ensuring the highest level of device reliability.

Block Diagram



Pin Configuration



Mode Selection

PINS / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	V_{CC}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	X	X	V_{PP}	V_{CC}	High Z
Silicon Signature*	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}

*For Silicon Signature: A_0 is toggled, $A_9 = 12V$, and all other addresses are at a TTL low.

Silicon Signature is a registered trademark of SEEQ Technology.

Pin Names

A_0-A_5	ADDRESSES—COLUMN
A_6-A_{13}	ADDRESSES—ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM

Description (cont.)

The 82025 is manufactured using JEDEC approved bytewide pinouts and 28-pin package. Access times as fast as 200 ns eliminate the need for wait states in high-performance microprocessor systems. Programming can be accomplished using either the intelligent algorithm or the 50 ms/byte algorithm available on commercial programmers.

Quality-Assurance Provisions

Quality-assurance screening for the 82025 is performed on 100% of the devices in accordance with Method 5004 of MIL-STD-883. In addition, burn-in (Method 1015, 125°C min) and data retention bake are performed on each device after Method 5004 screening and prior to submitting for quality conformance inspection testing.

Quality-Conformance Inspection

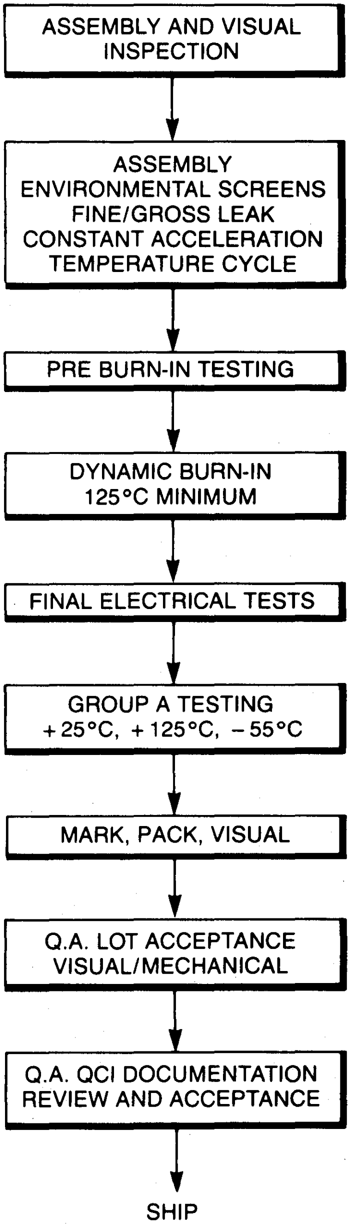
Quality-conformance inspection is performed in accordance with Method 5005 of MIL-STD-883. This includes Group A, Group B, Group C, and Group D inspections tests as defined in military drawing 82025. Generic QCI summary data will be provided upon request.

Electrical Performance Characteristics

The 82025 can be ordered from SEEQ Technology with device access times = 200 ns (82025-08), 250 ns (82025-02), 300 ns (82025-09), and 450 ns (82025-01). Details on device specific electrical performance can be found in the complete DESC 82025 military drawing or SEEQ's data sheet for generic part type DM27128. SEEQ's testing meets or exceeds all electrical performance screening and test limits as specified on the 82025 military drawing.

82025 Assembly/Test Flow Chart

Screening per MIL-STD-883 Method 5004 and quality-conformance acceptance per Method 5005



Programming

The 82025 may be programmed using an interactive intelligent algorithm or with a conventional 50 ms/byte programming pulse. Use of the intelligent algorithm improves the total device programming time by approximately 10 times over the 50 ms/byte algorithm.

To program using the intelligent algorithm requires $V_{CC}=6V$, $V_{PP}=21V$, and $\overline{CE}=V_{IL}$. The initial programming pulse applied to the $\overline{PGM}$ pin is one millisecond in duration, followed by a byte verification. Additional one millisecond program pulses are applied and checked until the byte passes verification. After verification, an overprogram pulse equal to 4X the number of one millisecond pulses required to initially program the byte is applied to the address. A maximum of 15 one millisecond pulses per byte is allowed. When the intelligent programming cycle has been completed, all bytes must be read with $V_{CC}=V_{PP}=5.0$ volts to verify correct programming.

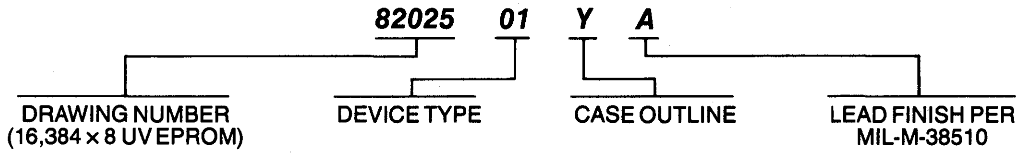
Erasure Characteristics

The 82025 is erased by exposure to high-intensity ultraviolet light with a wave length of 2537 angstroms. The minimum integrated dose for erasure (i.e. intensity × exposure time) is 15 watt-second/cm^2. The device should be placed within one inch of the lamp tube during erasure. After erasure, all bits are in the high state.

Silicon Signature

Incorporated in SEEQ's 82025 EPROM is a row of mask-programmed read-only memory (ROM) cells, located outside of the normal memory cell array. These ROM cells contain the EPROM's Silicon Signature. Silicon Signature identifies SEEQ as the manufacturer and gives the device's product code for programming. This allows the programmer to match the product to be programmed with the correct programming specification. Once the device code and programming specification have been verified, programming of the part can proceed.

Ordering Information



Device Type	Generic Number	Access Time
01	27128-45	450 ns
02	27128-25	250 ns
08	27128-20	200 ns
09	27128-30	300 ns

Case Outline
Y = D-10 (28 PIN, 1/2″ × 1-3/8″), DUAL-IN-LINE PACKAGE

Lead Finish
A = HOT SOLDER DIPPED

seeq

86063
MILITARY DRAWING
256K CMOS UV EPROM

May 1988

Features

- **86063 Military Drawing Compliant**
- **Processing Per Method 5004/5005 MIL-STD-883**
- **Low Power CMOS**
- **JEDEC-Approved Bytewide Pin Configuration**
- **200 ns Access Time**
- **MIL-M-38510 Compliant Package Design**
- **Programmed Using Intelligent Algorithm**
- **Silicon Signature®**

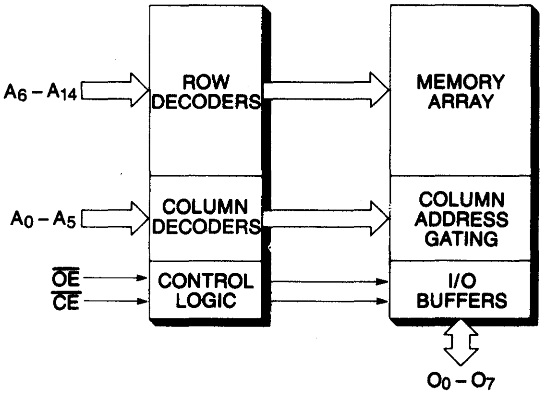
Description

SEEQ's 86063 is a military drawing compliant, 262,144-bit (32,768 × 8), ultra-violet erasable CMOS EPROM. The 256K EPROM is fabicated and tested in SEEQ Technology's DESC-approved manufacturing facility and has been processed per the requirements of Method 5004/5005 of MIL-STD-883. It's CMOS design draws less than one-half the active current and several orders of magnitude less standby current than the equivalent density N-channel EPROMS.

Pin Names

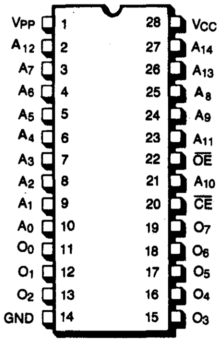
A_0-A_5	ADDRESSES—COLUMN
A_6-A_{14}	ADDRESSES—ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
NC	NO CONNECT

Block Diagram

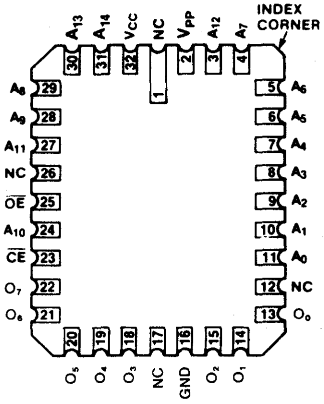


Pin Configuration

Dual-In-Line



Leadless Chip Carrier Bottom View



Silicon Signature is a registered trademark of SEEQ Technology.

Description (cont.)

The 86063 is manufactured using JEDEC approved bytewide pinouts for both the 28-pin dual-in-line and 32-pin leadless chip carrier packages. Access times as fast as 200 ns eliminate the need for wait states in high-performance microprocessor systems. Device programming is accomplished using the interactive intelligent algorithm available on commercial programmers.

Using the 86063 will satisfy MIL-STD-454K which dictates the use of military drawing parts over 883C compliant parts if they are available. Furthermore, designing with standard military drawing devices eliminates the need for customer-generated source control drawings, while ensuring the highest level of device reliability.

Quality-Assurance Provisions

Quality-assurance screening for the 86063 is performed on 100% of the devices in accordance with Method 5004 of MIL-STD-883. In addition, burn-in (Method 1015, 125°C min) and data retention bake are performed on each device after Method 5004 screening and prior to submitting for quality conformance inspection testing.

Quality-Conformance Inspection

Quality-conformance inspection is performed in accordance with Method 5005 of MIL-STD-883. This includes Group A, Group B, Group C, and Group D inspections tests as defined in military drawing 86063. Generic QCI summary data will be provided upon request.

Mode Selection

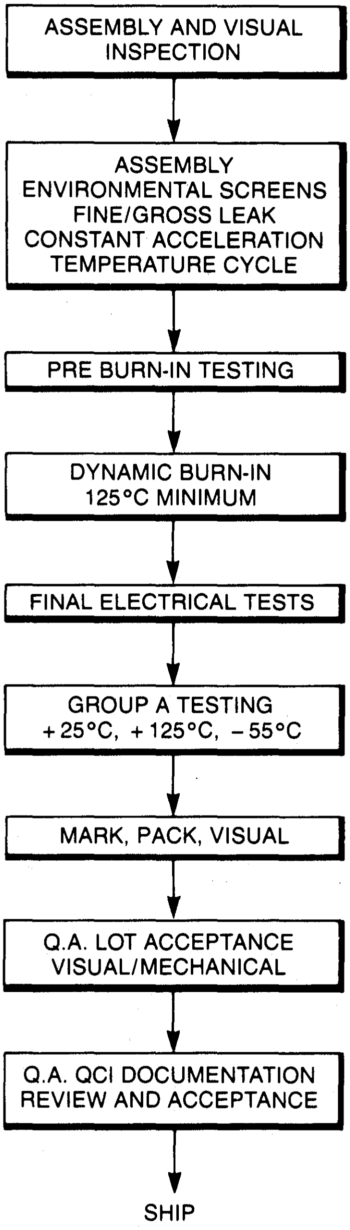
PINS MODE	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{PP}	6.0V	D_{IN}
Program Verify	V_{IH}	V_{IL}	V_{PP}	6.0V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	6.0V	High Z
Silicon Signature*	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Encoded Data

X can be either V_{IL} or V_{IH}

*For Silicon Signature: A_0 is toggled, $A_9 = 12V$, and all other addresses are at a TTL low.

86063 Assembly/Test Flow Chart

Screening per MIL-STD-883 Method 5004 and quality-conformance acceptance per Method 5005



Electrical Performance Characteristics

The 86063 can be ordered from SEEQ Technology with device access times = 200 ns (86063-01), 250 ns (86063-02), and 300 ns (86063-03). Details on device specific electrical performance can be found in the complete DESC 86063 military drawing or SEEQ's data sheet for generic part type DM27C256. SEEQ's testing meets or exceeds all electrical performance screening and test limits as specified on the 86063 military drawing.

Programming

To program the 86063 using the intelligent algorithm requires $V_{CC} = 6V$, $V_{PP} = 12.5V$, and $\overline{OE} = V_{IH}$. The initial programming pulse applied to the $\overline{CE}$ pin is one millisecond in duration, followed by a byte verification. Additional one millisecond program pulses are applied and checked until the byte passes verification. After verification, an overprogram pulse equal to 3X the number of one millisecond pulses required to initially program the byte is applied to the address. A maximum of 25 one millisecond pulses per byte is allowed. When the intelligent programming cycle has been completed, all bytes must be read with $V_{CC} = V_{PP} = 5.0$ volts to verify correct programming.

Erasure Characteristics

The 86063 is erased by exposure to high-intensity ultraviolet light with a wave length of 2537 angstroms. The minimum integrated dose for erasure (i.e. intensity × exposure time) is 15 watt-second/cm^2. The device should be placed within one inch of the lamp tube during erasure. After erasure, all bits are in the high state.

Silicon Signature

Incorporated in SEEQ's 86063 EPROM is a row of mask-programmed read-only memory (ROM) cells, located outside of the normal memory cell array. These ROM cells contain the EPROM's Silicon Signature. Silicon Signature identifies SEEQ as the manufacturer and gives the device's product code for programming. This allows the programmer to match the product to be programmed with the correct programming specification. Once the device code and programming specification have been verified, programming of the part can proceed.

Ordering Information

86063 01 X A

DRAWING NUMBER
(32,768 × 8 UV EPROM)

DEVICE TYPE

CASE OUTLINE

LEAD FINISH PER
MIL-M-38510

Device Type	Generic Number	Access Time
01	27C256-20	200 ns
02	27C256-25	250 ns
03	27C256-30	300 ns

Case Outline
X = D-10 (28 PIN, 1/2″ × 1-3/8″), DUAL-IN-LINE PACKAGE

Y = C-12 (32 TERMINAL, .450 × .550″), RECTANGULAR CHIP CARRIER PACKAGE

Lead Finish
A = HOT SOLDER DIPPED
C = GOLD PLATE

seeq

E/M 48F512
512K CMOS FLASH™ EEPROM

ADVANCE DATA SHEET *October 1988*

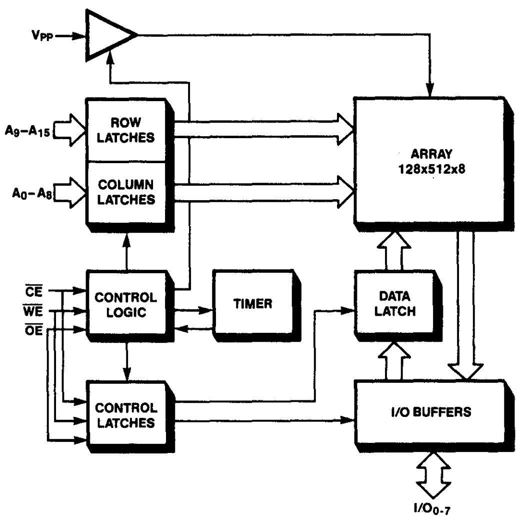
Features

- ***64K Byte FLASH Erasable Non-Volatile Memory***
- ***FLASH EEPROM Cell Technology***
- ***Electrical Chip and 512 Byte Sector Erase***
- ***Input Latches for Writing and Erasing***
- ***−55° C to +125° C Temp Read (M48F512)***
- ***−55° C to +85° C Temp Write/Erase (M48F512)***
- ***−40° C to +85° C Temp Read/Write/Erase (E48F512)***
- ***Ideal for Program and Data Storage Applications***
  - ***Minimum 100 Cycle Endurance***
  - ***Optional 1000 Cycle Endurance***
  - ***Minimum 10 Year Data Retention***
- ***Silicon Signature®***

Pin Names

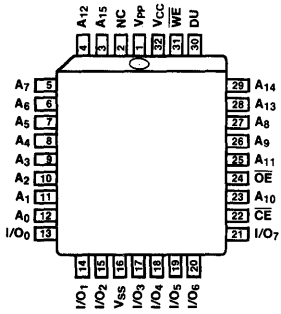
A_0-A_8	COLUMN ADDRESS INPUT
A_9-A_{15}	ROW ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

Block Diagram

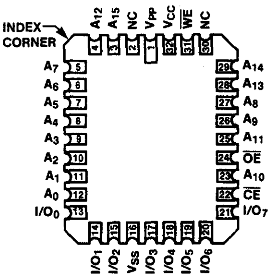


Pin Configurations

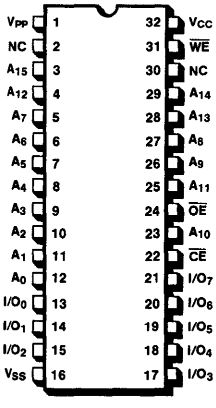
PLASTIC LEADED CHIP CARRIER TOP VIEW



LEADLESS CHIP CARRIER TOP VIEW



DUAL-IN-LINE TOP VIEW



Silicon Signature is a registered trademark of SEEQ Technology.
FLASH is a trademark of SEEQ Technology.

Description

The M48F512 is a 512K bit CMOS FLASH EEPROM organized as 64K x 8 bits. SEEQ's M48F512 brings together the high density and cost effectiveness of UVEPROMs, with the electrical erase, in-circuit reprogrammability and package options of EEPROMs.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated. The memory array is divided into 128 sectors, with each sector containing 512 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

Endurance, the number of times each byte can be written, is specified at 100 cycles with an optional screen for 1000 cycles available. Electrical write/erase capability allows the M48F512 to accommodate a wide range of plastic, ceramic and surface mount packages.

Read

Reading is accomplished by presenting a valid address with chip enable and output enable at V_{IL}, write enable at V_{IH}, and V_{PP} at any level. See timing waveforms for A.C. parameters.

Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Sector Erase

Sector erase changes all bits in a sector of the array to a logical one. It requires that the V_{PP} pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs A_9 through A_{15}. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time t_{abort} to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the t_{abort} delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in figure 2. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Sector and Chip Erase Algorithm

To reduce the sector and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the sector erase and chip erase flow charts.

Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either sector erase or chip erase.

Data are organized in the M48F512 in a group of bytes called a sector. The memory array is divided into 128 sectors of 512 bytes each. Individual bytes are written as part of a sector write operation. The programming algorithm for either chip or sector write is detailed in figure 1.

Sectors are written by applying a high voltage to the V_{PP} pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of t_{WC} ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired sectors have been written. After 15 loops, a read-verification is performed. For any bytes which do not verify, a fill-in programming loop is performed. Sectors need not be written separately; the entire device or any combination of blocks can be written using the write algorithm.

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sector must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

Power Up/Down Protection

These two devices contain a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1 uf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the M48F512 which contains the device's Silicon Signature. Silicon Signature contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_9 to 12 ± 0.5 V. and bringing all other address inputs plus chip enable and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0. Silicon Signature is functional at room temperature only (25°C.)

Silicon Signature Bytes

	A_0	Data (Hex)
Seeq Code	V_{IL}	94
Product code M48F512	V_{IH}	1A

Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	A_{9-15}	A_{0-8}	I/O_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HI-Z
Byte write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip erase select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Sector erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

Absolute Maximum Stress Ratings

Temperature:	
Storage	*−65°C to +150°C*
Under bias	*−65°C to +135°C*
All Inputs except V_{PP} and outputs with Respect to V_{SS}	*+7 V to −0.5 V*
V_{PP} pin with respect to V_{SS}	*14 V*

E.S.D. Characteristics[1]

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note 1: Characterization data—not tested.

Recommended Operating Conditions

	M48F512	E48F512
V_{CC} supply voltage	5V ± 10%	5V ± 10%
Temperature range (read mode)	−55°C to +125°C	−40°C to +85°C
Temperature range (write/erase mode)	−55°C to +85°C	−40°C to +85°C

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	Parameter	Value	Test Conditions
C_{IN}	Input capacitance	6 pf.	V_{IN}= 0 V
C_{OUT}	Output capacitance	12 pf.	$V_{I/O}$= 0 V

Note 2: Only performed for initial qualification and after any design or process change which could affect parameter limits.

DC Operating Characteristics

Over the V_{CC} and temperature range

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
I_{IH}	Input leakage high		1	μA	$V_{IN} = V_{CC}$
I_{IL}	Input leakage low		−1	μA	V_{IN} = 0.1 v
I_{OL}	Output leakage		10	μA	$V_{IN} = V_{CC}$
V_P	Program/erase voltage	11.75	13	V	
V_{PR}	V_{PP} Voltage during read	0	V_P	V	
I_{PP}	V_P current Standby mode Read mode Byte write Erase		 200 200 50 90	 μA μA mA mA	 $\overline{CE} = V_{IH}, V_{PP} = V_P$ $\overline{CE} = V_{IL}, V_{PP} = V_P$ $V_{PP} = V_P$ $V_{PP} = V_P$
I_{CC1}	Standby V_{CC} current		400	μA	$\overline{CE} = V_{CC} - 0.3$ v
I_{CC2}	Standby V_{CC} current		5	mA	$\overline{CE}$ - V_{IH} min.
I_{CC3}	Active V_{CC} current		100	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input low voltage	−0.3	0.8	V	
V_{IH}	Input high voltage	2.0	7.0	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2.1 ma
V_{OH1}	Output level (TTL)	2.4		V	$I_{OH} = -400\mu A$
V_{OH2}	Output level (CMOS)	V_{CC}−0.4		V	$I_{OH} = -100\mu A$

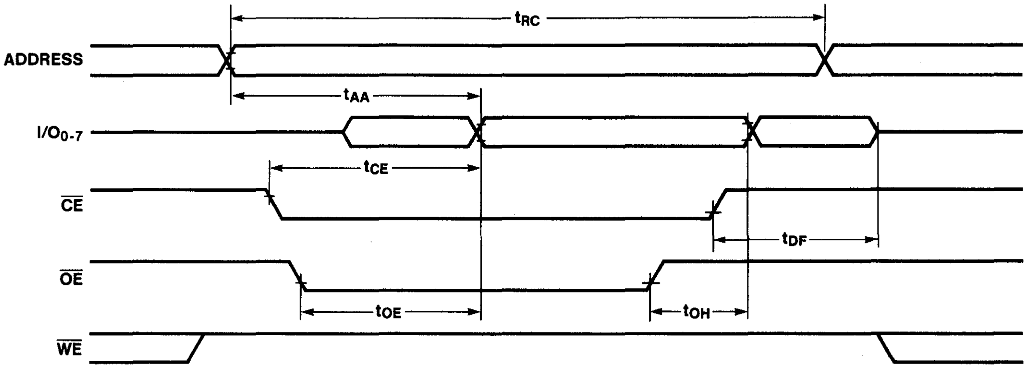
AC Characteristics

(over the V_{CC} and temperature range)

READ

Symbol	Parameter	E/M48F512 -250		E/M48F512 -300		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	250		300		ns
t_{AA}	Address to data		250		300	ns
t_{CE}	$\overline{CE}$ to data		250		300	ns
t_{OE}	$\overline{OE}$ to data		100		150	ns
t_{DF}	$\overline{OE}/\overline{CE}$ to data float		60		100	ns
t_{OH}	Output hold time	0		0		ns

Read Timing



AC Test Conditions

Output load: 1 TTL gate and C(load) 100 pf.
Input rise and fall times: < 20 ns.
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

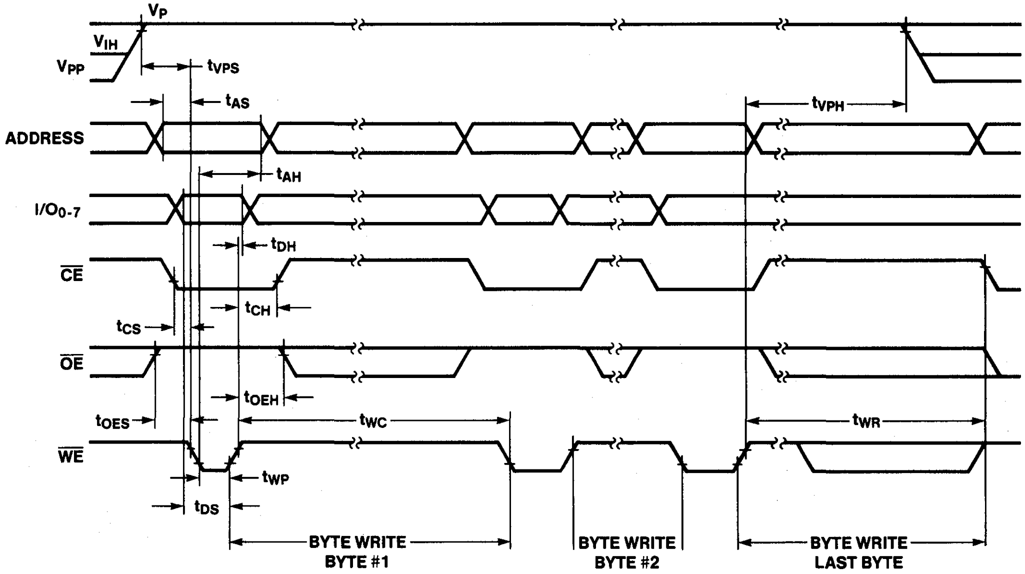
AC Characteristics

(Over the V_{CC} and temperature range)

BYTE WRITE

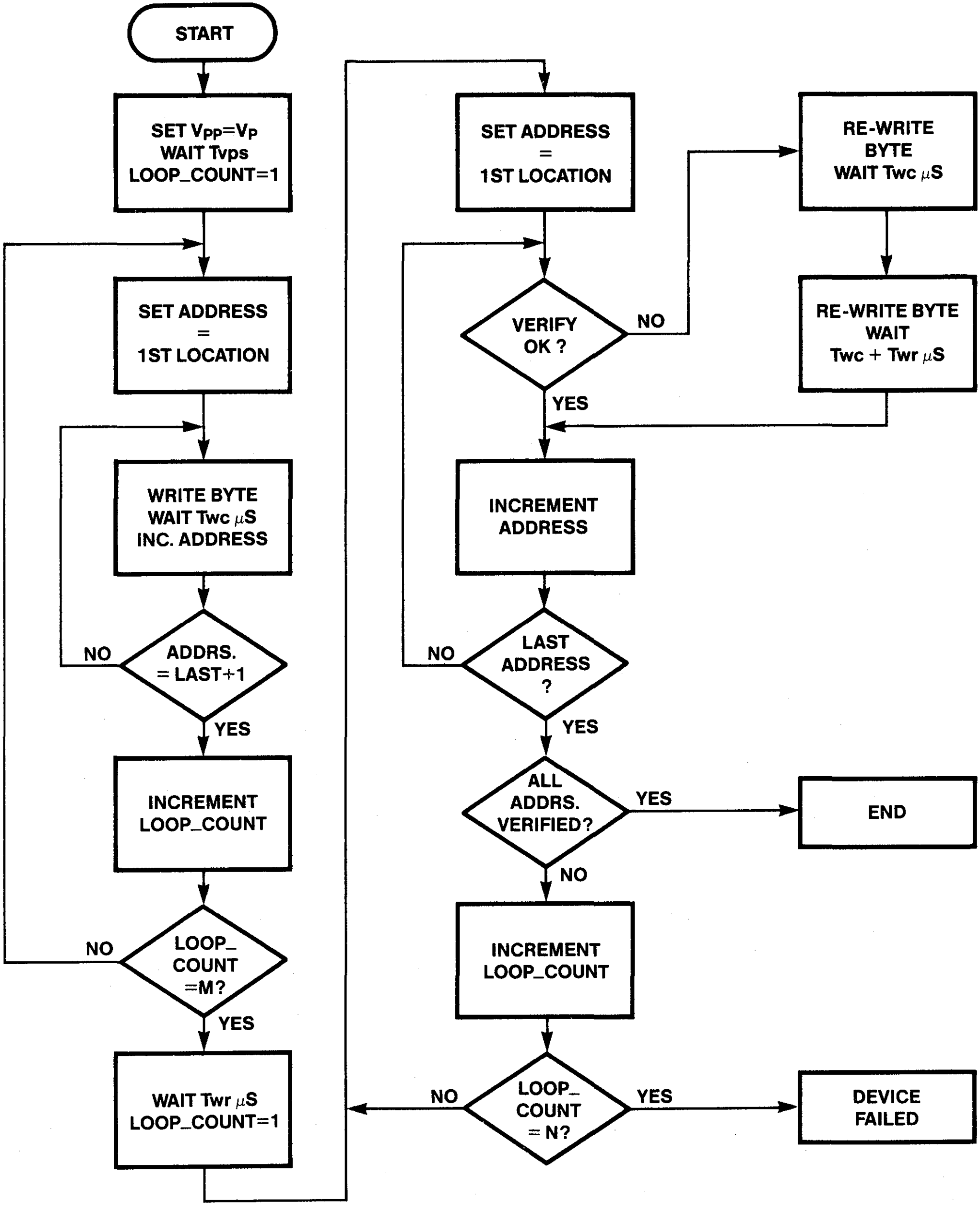
Symbol	Parameter	E/M48F512 Min.	E/M48F512 Max.	Unit
t_{VPS}	V_{PP} setup time	2		µs
t_{VPH}	V_{PP} hold time	250		µs
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OES}	$\overline{OE}$ setup time	10		ns
t_{OEH}	$\overline{OE}$ hold time	10		ns
t_{AS}	Address setup time	50		ns
t_{AH}	Address hold time	100		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	20		ns
t_{WP}	$\overline{WE}$ pulse width	150		ns
t_{WC}	Write cycle time	100	150	µs
t_{WR}	Write recovery time		2.0	ms

Byte Write Timing



Note: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g., access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Figure 1
E/M48F512 Write Algorithm



M=15
N=6

AC Characteristics

(Over the V_{CC} and temperature range)

SECTOR ERASE

Symbol	Parameter	E/M48F512 Min.	E/M48F512 Max.	Unit
t_{VPS}	V_{PP} setup time	2		µs
t_{VPH}	V_{PP} hold time	500		ms
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{OES}	$\overline{OE}$ setup time	0		ns
t_{AS}	Address setup time	50		ns
t_{AH}	Address hold time	100		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	20		ns
t_{WP}	$\overline{WE}$ pulse width	150		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OEH}	$\overline{OE}$ hold time	0		ns
t_{ERASE}	Sector erase time		500	ms
t_{ABORT}	Sector erase delay		250	µs
t_{ER}	Erase recovery time		500	ms

Sector Erase Timing

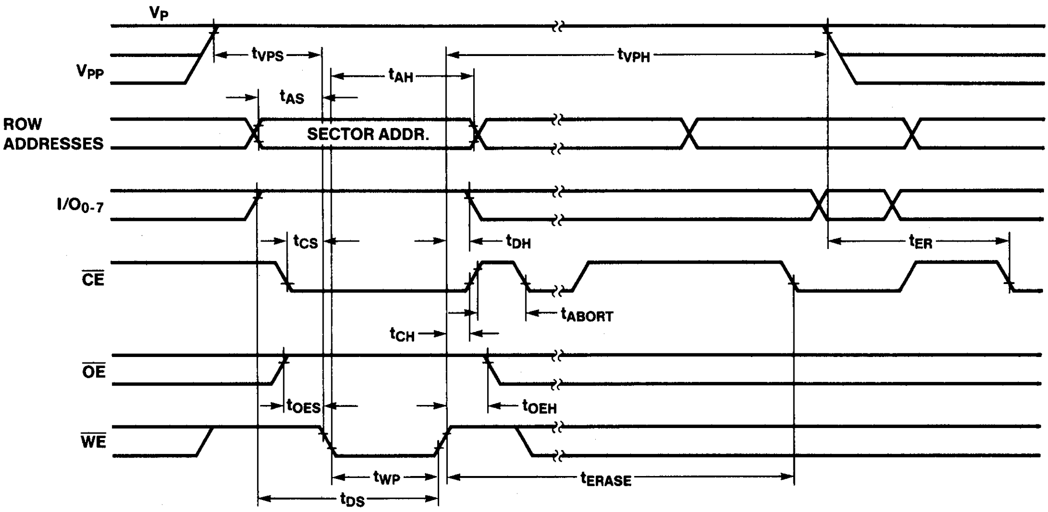
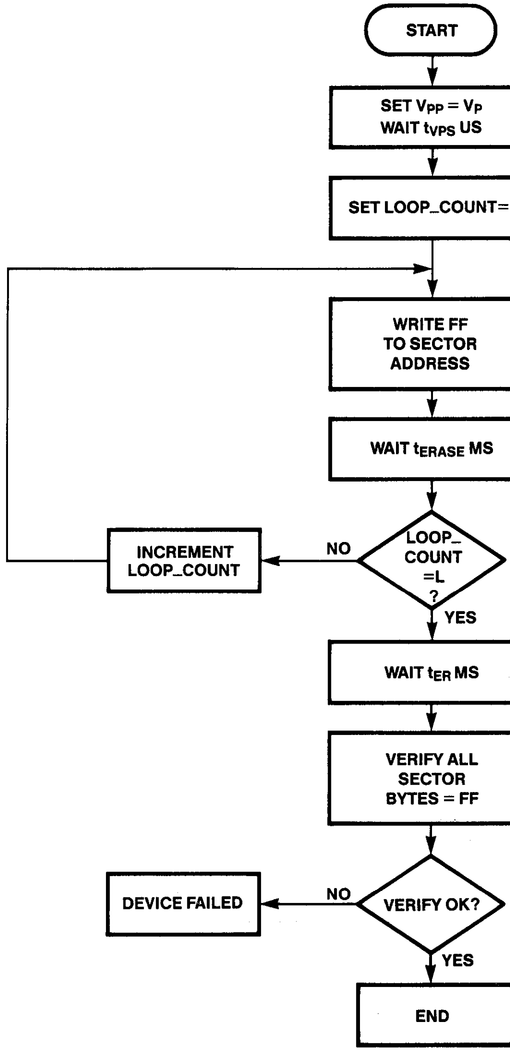


Figure 2
E/M48F512 Sector Erase Algorithm



L=60

AC Characteristics

(Over the V_{CC} and temperature range)

CHIP ERASE

Symbol	Parameter	E/M48F512		Unit
		Min.	**Max.**	
t_{VPS}	V_{PP} setup time	2		μs
t_{VPH}	V_{PP} hold time	500		ms
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{OES}	$\overline{OE}$ setup time	0		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	20		ns
t_{WP}	$\overline{WE}$ pulse width	150		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OEH}	$\overline{OE}$ hold time	0		ns
t_{ERASE}	Chip erase time		500	ms
t_{ER}	Erase recovery time		500	ms

Chip Erase Timing

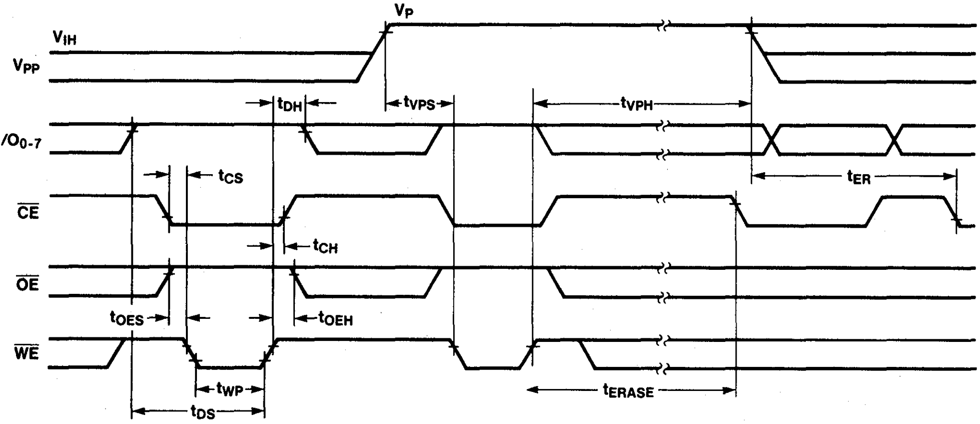
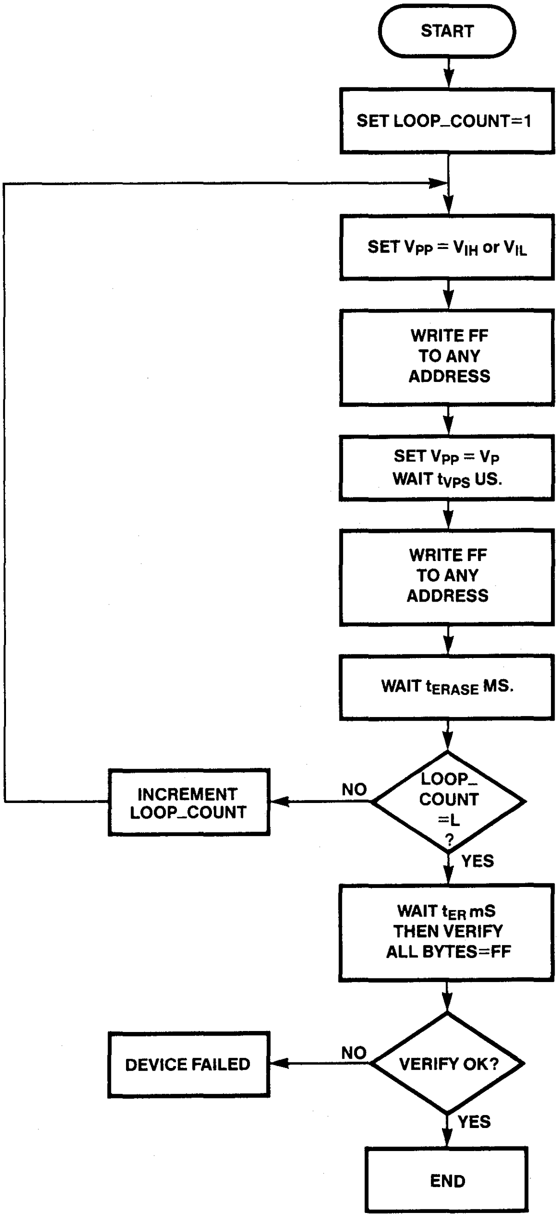


Figure 3
E/M48F512 Chip Erase Algorithm



L=60

Ordering Information

D	M	48F512	K	−250	/B
Package Type	**Temperature Range**	**Device**	**Endurance**	**Access Time**	**Screening**
D = Ceramic Dip	E = −40 to +85°C	64K x 8 FLASH EEPROM	Blank = 100	250 = 250ns	MIL 883 Class B Screened (Optional)
L = Ceramic Leadless Chip Carrier	M = −55 to +125°C (Read) −55 to +85°C (Write/Erase)		K = 1000	300 = 300ns	
N = Plastic Leaded Chip Carrier (−40 to +85°C Temp Range Only)					

seeq

E/M 48F010
1024K CMOS FLASH™ EEPROM

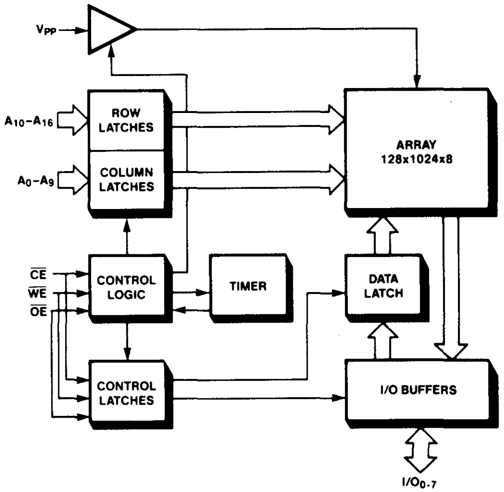
ADVANCE DATA SHEET

October 1988

Features

- ***128K Byte FLASH Erasable Non-Volatile Memory***
- ***FLASH EEPROM Cell Technology***
- ***Electrical Chip and 1024 Byte Sector Erase***
- ***Input Latches for Writing and Erasing***
- ***−55°C to +125°C Temp Read (M48F010)***
- ***−55°C to +85°C Temp Write/Erase (M48F010)***
- ***−40°C to +85°C Temp Read/Write/Erase (E48F010)***
- ***Ideal for Program and Data Storage Applications***
    - ***Minimum 100 Cycle Endurance***
    - ***Optional 1000 Cycle Endurance***
    - ***Minimum 10 Year Data Retention***
- ***Silicon Signature®***

Block Diagram

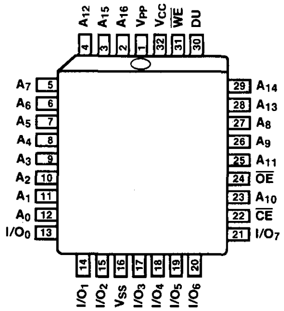


Pin Names

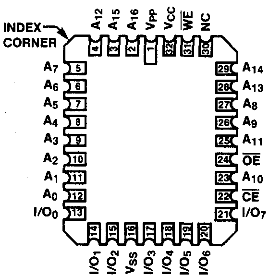
A_0-A_9	COLUMN ADDRESS INPUT
A_{10}-A_{16}	ROW ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

Pin Configurations

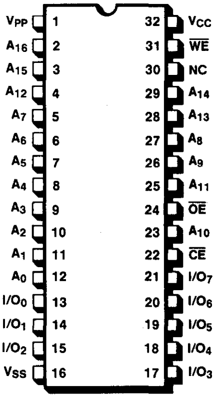
PLASTIC LEADED CHIP CARRIER TOP VIEW



LEADLESS CHIP CARRIER TOP VIEW



DUAL-IN-LINE TOP VIEW



Silicon Signature is a registered trademark of SEEQ Technology.
FLASH is a trademark of SEEQ Technology.

Description

The M48F010 is a 1024K bit CMOS FLASH EEPROM organized as 128K x 8 bits. SEEQ's M48F010 brings together the high density and cost effectiveness of UVEPROMs, with the electrical erase, in-circuit reprogrammability and package options of EEPROMs.

On-chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase/read cycles have been initiated. The memory array is divided into 128 sectors, with each sector containing 1024 bytes. Each sector can be individually erased, or the chip can be bulk erased before reprogramming.

Endurance, the number of times each byte can be written, is specified at 100 cycles with an optional screen for 1000 cycles available. Electrical write/erase capability allows the M48F010 to accommodate a wide range of plastic, ceramic and surface mount packages.

Read

Reading is accomplished by presenting a valid address with chip enable and output enable at V_{IL}, write enable at V_{IH}, and V_{PP} at any level. See timing waveforms for A.C. parameters.

Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Sector Erase

Sector erase changes all bits in a sector of the array to a logical one. It requires that the V_{PP} pin be brought to a high voltage and a write cycle performed. The sector to be erased is defined by address inputs A_{10} through A_{16}. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time t_{abort} to allow aborting the erase by writing again. This permits recovering from an unintentional sector erase if, for example, in loading a block of data a byte of 'FF' was written. After the t_{abort} delay, the sector erase will begin. The erase is accomplished by following the erase algorithm in figure 2. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Sector and Chip Erase Algorithm

To reduce the sector and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the sector erase and chip erase flow charts.

Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either sector erase or chip erase.

Data are organized in the M48F010 in a group of bytes called a sector. The memory array is divided into 128 sectors of 1024 bytes each. Individual bytes are written as part of a sector write operation. The programming algorithm for either chip or sector write is detailed in figure 1.

Sectors are written by applying a high voltage to the V_{PP} pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of t_{WC} ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired blocks have been written. After 15 loops, a read-verification is performed. For any bytes which do not verify, a fill-in programming loop is performed. Sectors need not be written separately; the entire device or any combination of blocks can be written using the write algorithm.

Because bytes can only be written as part of a sector write, if data is to be added to a partially written sector or one or more bytes in a sector must be changed, the contents of the sector must first be read into system RAM; the bytes can then be added to the block of data in RAM and the sector written using the sector write algorithm.

Power Up/Down Protection

These two devices contain a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1 uf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the M48F010 which contains the device's Silicon Signature. Silicon Signature contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_9 to 12 ± 0.5 V. and bringing all other address inputs plus chip enable and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0. Silicon Signature is functional at room temperature only (25°C.)

Silicon Signature Bytes

	A_0	Data (Hex)
Seeq Code	V_{IL}	94
Product code M48F010	V_{IH}	1C

Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	A_{10-16}	A_{0-9}	I/O_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HI-Z
Byte write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip erase select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Sector erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

Absolute Maximum Stress Ratings

Temperature:	
Storage	*−65°C to +150°C*
Under bias	*−65°C to +135°C*
All Inputs except V_{PP} and outputs with Respect to V_{SS}	*+7 V to −0.5 V*
V_{PP} pin with respect to V_{SS}	*14 V*

E.S.D. Characteristics[1]

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note 1: Characterization data—not tested.

Recommended Operating Conditions

	M48F010	E48F010
V_{CC} supply voltage	5V ± 10%	5V ± 10%
Temperature range (read mode)	−55°C to +125°C	−40°C to +85°C
Temperature range (write/erase mode)	−55°C to +85°C	−40°C to +85°C

Capacitance[2] T_A=25°C, f=1 MHz

Symbol	Parameter	Value	Test Conditions
C_{IN}	Input capacitance	6 pf.	V_{IN}= 0 V
C_{OUT}	Output capacitance	12 pf.	$V_{I/O}$= 0 V

Note 2: Only performed for initial qualification and after any design or process change which could affect parameter limits.

DC Operating Characteristics

Over the V_{CC} and temperature range

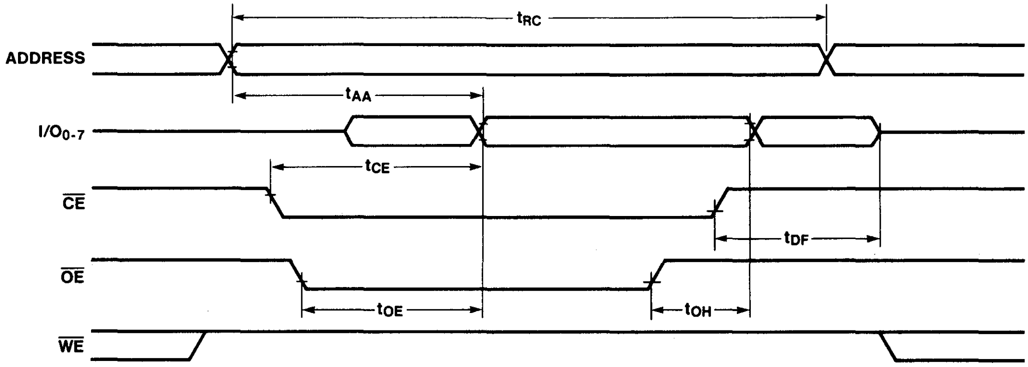
Symbol	Parameter	Limits Min.	Limits Max.	Limits Unit	Test Conditions
I_{IH}	Input leakage high		1	μA	$V_{IN} = V_{CC}$
I_{IL}	Input leakage low		−1	μA	V_{IN} = 0.1 v
I_{OL}	Output leakage		10	μA	$V_{IN} = V_{CC}$
V_P	Program/erase voltage	11.75	13	V	
V_{PR}	V_{PP} Voltage during read	0	V_P	V	
I_{PP}	V_P current Standby mode Read mode Byte write Erase		 200 200 50 90	 μA μA mA mA	 $\overline{CE} = V_{IH}, V_{PP} = V_P$ $\overline{CE} = V_{IL}, V_{PP} = V_P$ $V_{PP} = V_P$ $V_{PP} = V_P$
I_{CC1}	Standby V_{CC} current		400	μA	$\overline{CE} = V_{CC}$ −0.3 v
I_{CC2}	Standby V_{CC} current		5	mA	$\overline{CE}$ - V_{IH} min.
I_{CC3}	Active V_{CC} current		100	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input low voltage	−0.3	0.8	V	
V_{IH}	Input high voltage	2.0	7.0	V	
V_{OL}	Output low voltage		0.45	V	I_{OL} = 2.1 ma
V_{OH1}	Output level (TTL)	2.4		V	I_{OH} = −400μA
V_{OH2}	Output level (CMOS)	V_{CC}−0.4		V	I_{OH} = −100μA

AC Characteristics READ

(over the V_{CC} and temperature range)

Symbol	Parameter	E/M48F010 -250 Min.	E/M48F010 -250 Max.	E/M48F010 -300 Min.	E/M48F010 -300 Max.	Unit
t_{RC}	Read cycle time	250		300		ns
t_{AA}	Address to data		250		300	ns
t_{CE}	$\overline{CE}$ to data		250		300	ns
t_{OE}	$\overline{OE}$ to data		100		150	ns
t_{DF}	$\overline{OE}/\overline{CE}$ to data float		60		100	ns
t_{OH}	Output hold time	0		0		ns

Read Timing



AC Test Conditions

Output load: 1 TTL gate and C(load) 100 pf.
Input rise and fall times: < 20 ns.
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

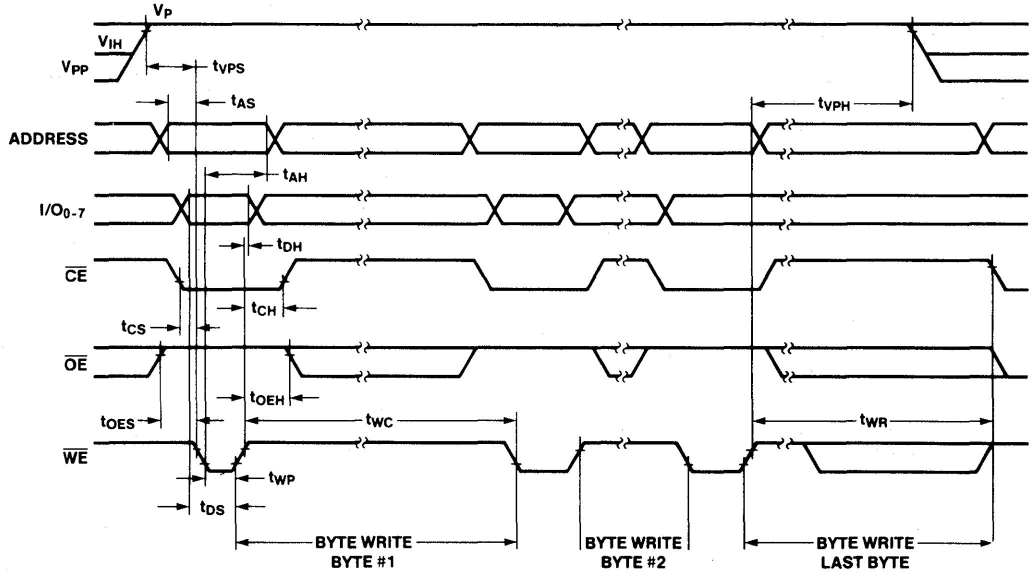
AC Characteristics

(Over the V_{CC} and temperature range)

BYTE WRITE

Symbol	Parameter	E/M48F010		Unit
		Min.	Max.	
t_{VPS}	V_{PP} setup time	2		µs
t_{VPH}	V_{PP} hold time	250		µs
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OES}	$\overline{OE}$ setup time	10		ns
t_{OEH}	$\overline{OE}$ hold time	10		ns
t_{AS}	Address setup time	50		ns
t_{AH}	Address hold time	100		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	20		ns
t_{WP}	$\overline{WE}$ pulse width	150		ns
t_{WC}	Write cycle time	100	150	µs
t_{WR}	Write recovery time		2.0	ms

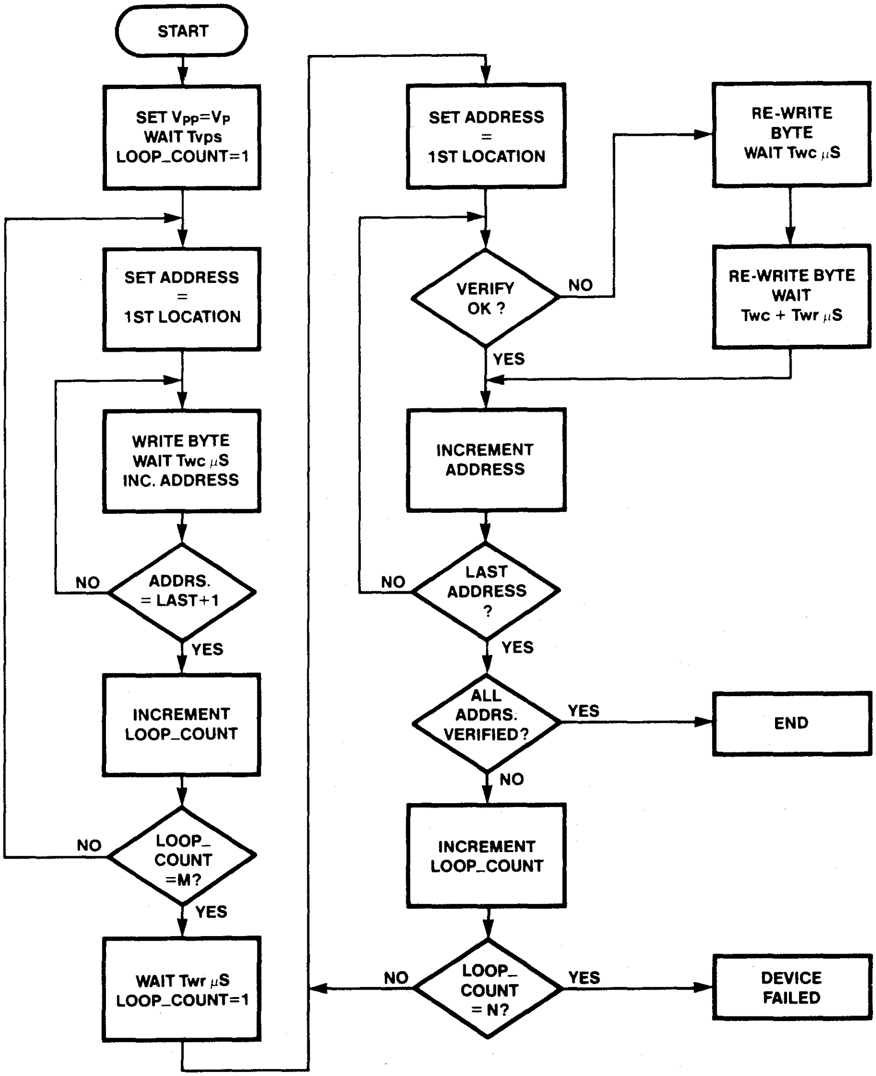
Byte Write Timing



Note: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g., access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Advance Data Sheets contain target product specifications which are subject to change upon device characterization over the full specified temperature range. These specifications may be changed at any time, without notice.

Figure 1
E/M48F010 Write Algorithm



M=15
N=6

AC Characteristics

(Over the V_{CC} and temperature range)

SECTOR ERASE

Symbol	Parameter	E/M48F010		Unit
		Min.	Max.	
t_{VPS}	V_{PP} setup time	2		µs
t_{VPH}	V_{PP} hold time	500		ms
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{OES}	$\overline{OE}$ setup time	0		ns
t_{AS}	Address setup time	50		ns
t_{AH}	Address hold time	100		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	20		ns
t_{WP}	$\overline{WE}$ pulse width	150		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OEH}	$\overline{OE}$ hold time	0		ns
t_{ERASE}	Sector erase time		500	ms
t_{ABORT}	Sector erase delay		250	µs
t_{ER}	Erase recovery time		500	ms

Sector Erase Timing

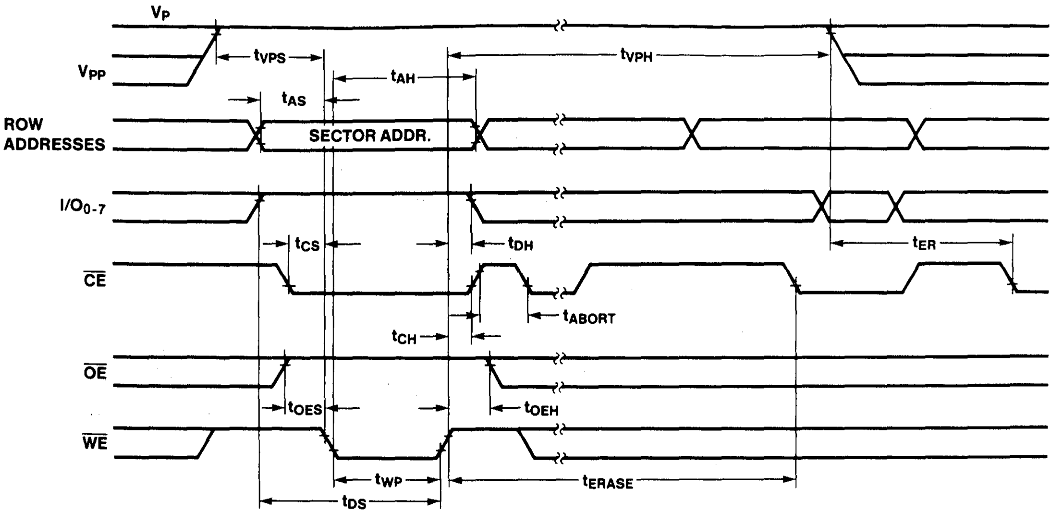
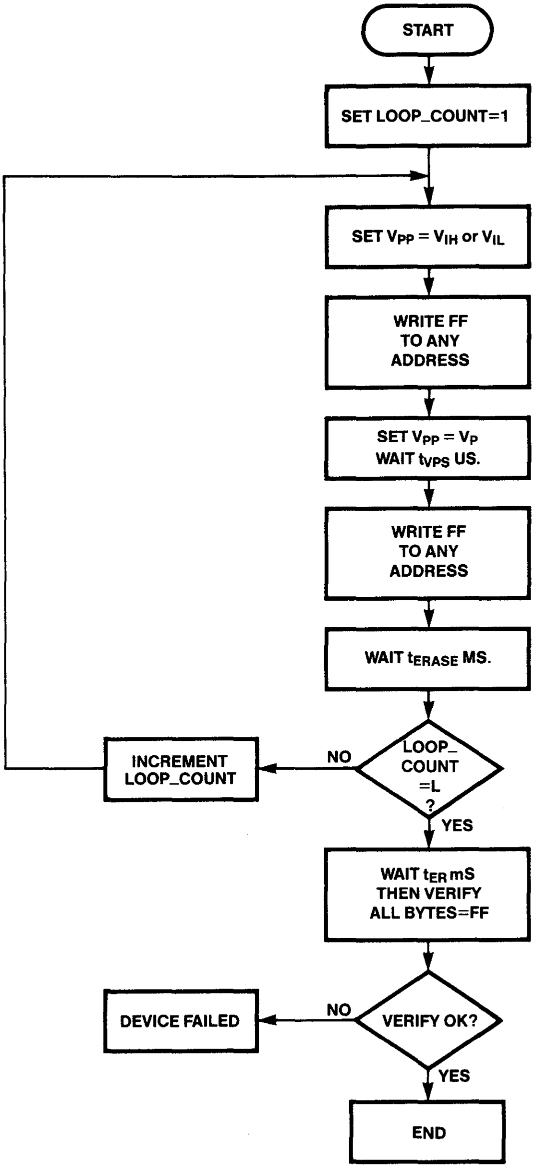


Figure 2
E/M48F010 Sector Erase Algorithm



L=60

AC Characteristics

(Over the V_{CC} and temperature range)

CHIP ERASE

Symbol	Parameter	E/M48F010		Unit
		Min.	Max.	
t_{VPS}	V_{PP} setup time	2		µs
t_{VPH}	V_{PP} hold time	500		ms
t_{CS}	$\overline{CE}$ setup time	0		ns
t_{OES}	$\overline{OE}$ setup time	0		ns
t_{DS}	Data setup time	50		ns
t_{DH}	Data hold time	20		ns
t_{WP}	$\overline{WE}$ pulse width	150		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{OEH}	$\overline{OE}$ hold time	0		ns
t_{ERASE}	Chip erase time		500	ms
t_{ER}	Erase recovery time		500	ms

Chip Erase Timing

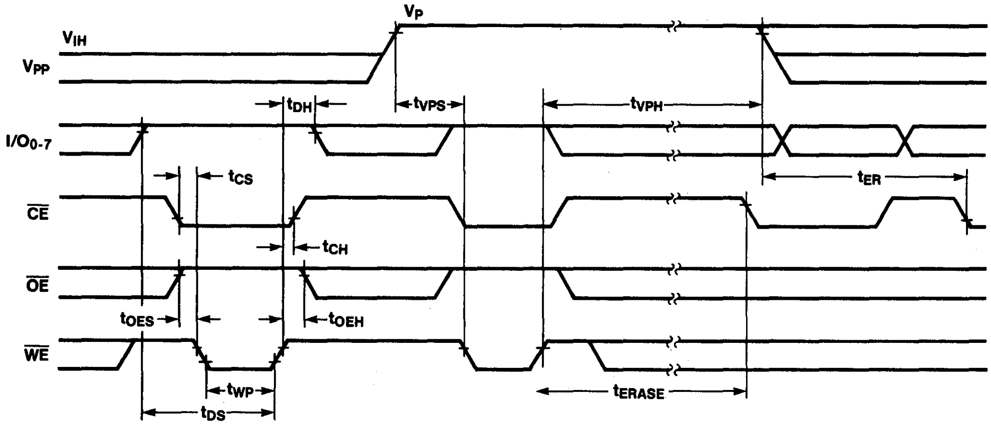
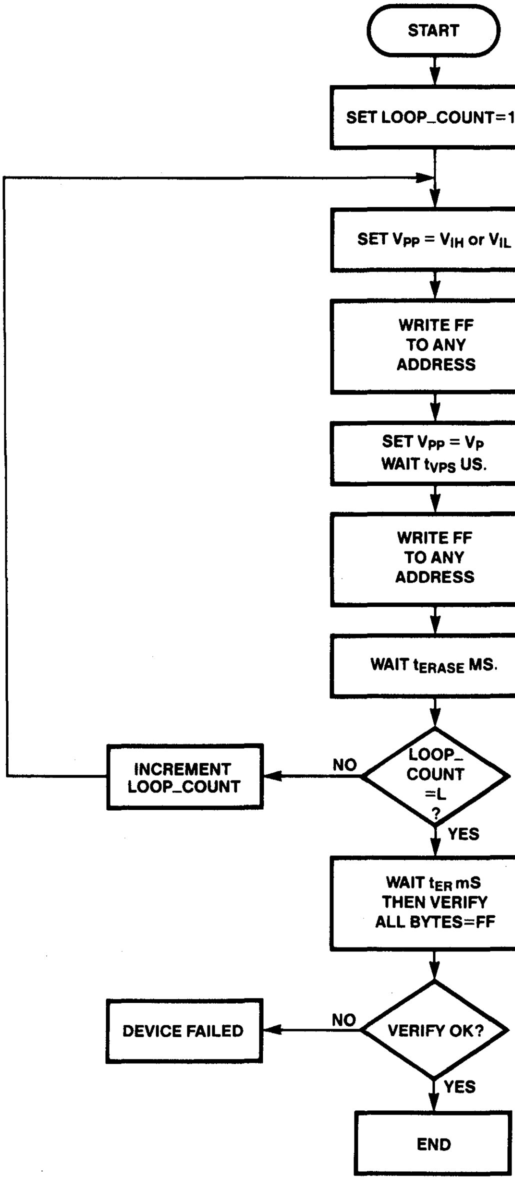


Figure 3
E/M48F010 Chip Erase Algorithm



L=60

Ordering Information

D	M	48F010	K	−250	/B
Package Type	**Temperature Range**	**Device**	**Endurance**	**Access Time**	**Screening**
D = Ceramic Dip	E = −40 to +85°C	128K x 8 FLASH EEPROM	Blank = 100	250 = 250ns	MIL 883 Class B Screened (Optional)
L = Ceramic Leadless Chip Carrier	M = −55 to +125°C (Read) −55 to +85°C (Write/Erase)		K = 1000	300 = 300ns	
N = Plastic Leaded Chip Carrier (−40 to +85°C Temp Range Only)					

For more information on SEEQ products, call our toll-free number:

1-800-3EEPROM

7 RELIABILITY

(Reliability Report)

SEEQ EEPROM Reliability Report

Introduction and Product Description

SEEQ offers a family of EEPROMs (Electrically Erasable Read Only Memories) which range in size from 4K to 256K bits in CMOS and NMOS technologies. They conform to the JEDEC configurations for byte wide memories. One family has internal input latches, a second family has internal input latches as well as a timer and a third with input latches, timer, and a page mode feature for fast write. New developments in process technology, circuit design techniques, and memory cell design combine to provide high performance from these EEPROMs that require only a single 5-volt power supply. SEEQ uses an innovative Q-Cell design on all its EEPROMs designed since 1983. The Q-Cell, combined with oxynitride in the tunnel dielectric, substantially improves the write/erase endurance of EEPROMs. This gives higher reliability to systems requiring infrequent writes (i.e., once a day for ten years) as well as to systems writing 5-10 times per day.

Programming the state of the memory cells (via the write and erase modes) is accomplished by charging and discharging a floating gate device via Fowler-Nordheim tunneling. This tunneling occurs through a proprietary oxynitride dielectric under the floating gate (see Figure 1). The use of oxynitride provides fast write/erase times at internal voltages that are 25% lower than those required for conventional oxide-only approaches due to a lower barrier height than thermal oxide. In addition, oxynitride provides lower charge trapping characteristics which gives improved write/erase endurance of each cell. The use of oxynitride in the dielectric area and SEEQ's proprietary Q-Cell design allows endurance to be specified up to 1,000,000 cycles/byte.

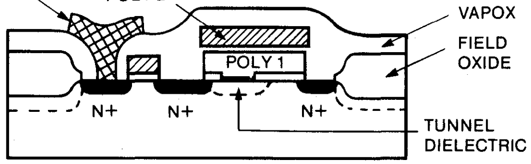


FIGURE 1. EEPROM N-MOS

Memory Cell Operation

The SEEQ EEPROM Memory Cell consists of a MOS Floating Gate Memory Transistor and a Select Transistor. See the Device Cross Section in Figure 1 and schematic representation in Figure 2. The Memory Cell defines the Logic state, either a "1" or a "0", by storing negative or positive charge on the Floating Poly Silicon Gate (Poly 1 in Figure 1). When the reference voltage is applied to the top Poly Silicon Gate (Poly 2 in Figure 1), the Memory Cell will or will not conduct a current. This cell current is detected by the sense amplifier and transmitted to the output buffers as the appropriate Logic state.

Charge is transferred on and off the Floating Gate through the thin Oxynitride Tunnel Dielectric by Fowler-Nordheim Tunneling; (A Quantum Mechanical transmission mechanism of an electron penetrating through the energy bandgap for the thin oxide MOS structure). Fowler-Nordheim Tunneling occurs when a high voltage, typically 17-20 Volts, is placed across the Tunnel Dielectric region of the Memory Cell. This high voltage is generated internal to the device, the user need only to apply an external 5 Volt level.

For a Logic "1", electrons are stored on the Floating Gate; using the conditions defined For "erase." For a Logic "0", holes are stored on the Floating Gate; using the conditions defined for "write." The Memory Cells Thresholds for a Logic "1" and "0" are shown in Figure 3.

	Program	Erase	Read
Column	17V	5V	5V
Row	20V	20V	5V
Sense	0	20V	0
Bit	17V	0	2V
Array V_{SS}	Floating	0	0
Floating Gate	$-V_P$	$+V_E$	
V_T	<-5V	>+2V	
I Cell	40μA	0μA	

The select transistors are used to isolate the Memory Transistor in order to prevent data disturb. Memory cells and Peripheral Logic are combined to form the Q-Cell, which is a Memory Error Correction technique transparent to the user.

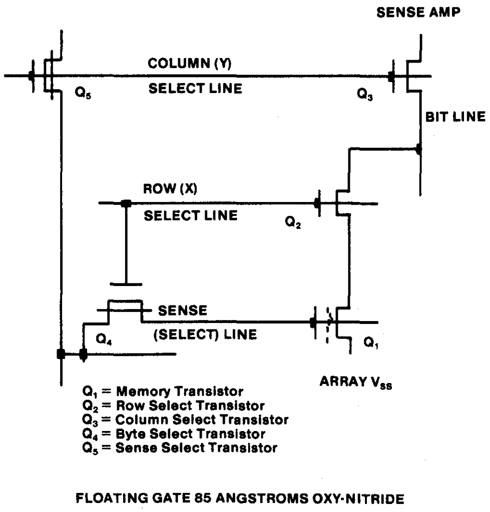


FIGURE 2. Generic EEPROM Memory Cell

Through the use of the proprietary Oxynitride process for the Tunnel Dielectric and use of the Q-Cell, SEEQ provides EEPROM's with typical data retention times of greater than 100 years, and Intrinsic Endurance Failure Rates of less than .03%/1000 cycles. Devices with a guaranteed Endurance of 1,000,000 cycles are possible.

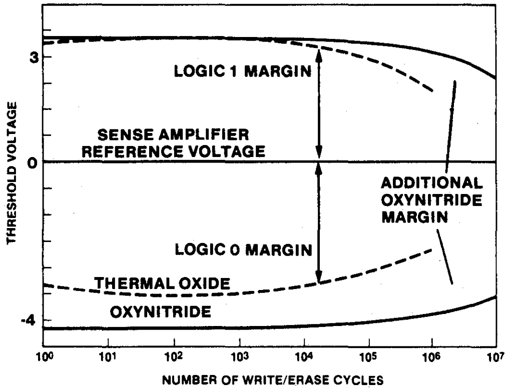


FIGURE 3. EEPROM Cell Margin Characteristics

Static Life

"Static" refers to the D.C. bias of the cell periphery. Failure modes for static life include threshold shifts and leakages. The typical failure mechanisms are mobile ion contamination or trapped charges.

The "static" stress mode may be used either for screening or determining the long term reliability of the product.

Operating Life

The operating life of an EEPROM is limited by its general reliability which includes integrity of the peripheral circuitry as well as the memory cells. The operating life is characterized using a dynamic high temperature life stress.

Dynamic high temperature life stress is a standard approach used to evaluate the failure rate distribution of a product under accelerated conditions. The failure rate is statistically derived from the experimental results obtained at elevated temperatures, then extrapolated to typical operating temperature conditions. This extrapolation is accomplished using the Arrhenius relationship and an apparent activation energy consistent with the failure mechanisms observed. This acceleration technique works well for common causes of failure such as oxide defects, interconnect voids, and defective bonding.

For ease of calculation, the instantaneous failure rate is assumed to be constant throughout the lifetime of the product (i.e., the probability density function of the time to failure is assumed to be exponential).

Units to be stressed were drawn from finished goods inventory and written with a data pattern selected to program both logic states of "1" and "0" into locations in each row and each column of the array. Initial, intermediate, and final electrical testing of units was conducted at room temperature using a test program that checks parametrics, functionality and timing parameters.

The dynamic high temperature stress was applied in accordance with the conditions prescribed in MIL-STD-883, Method 1015, Condition D. Oven ambient temperature was maintained at 125 degrees C. The schematics are available upon request.

Table 1. Static Life Stress Results

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 125° C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.6 eV)
52B13	324	324,000 hrs.	0	0.019%/1000 hrs.
2816	87	309,000 hrs.	0	0.020%/1000 hrs.

The results are summarized in Table 2. The predictions use an assumed activation energy of Ea = 0.4 ev for Ta = 55 degrees C. The predicted charge gain failure rate is less than one-half the intrinsic failure rate of NMOS, as would be expected. This implies the field usage failure rate would be accurately predicted by dynamic life test.

Data Retention Bake

Intrinsic data retention is defined as the ability to retain valid data over a prolonged period of time under storage conditions. At the cell level, data retention is a measure of the ability of the floating gate to retain charge in the absence of applied external gate bias. Data retention failures in a floating gate structure are commonly caused by dielectric defects and can be accelerated by high temperature bake stress. This characteristic provides a technique for both screening potentially defective product from the production flow as well as predicting expected retention lifetimes of outgoing product.

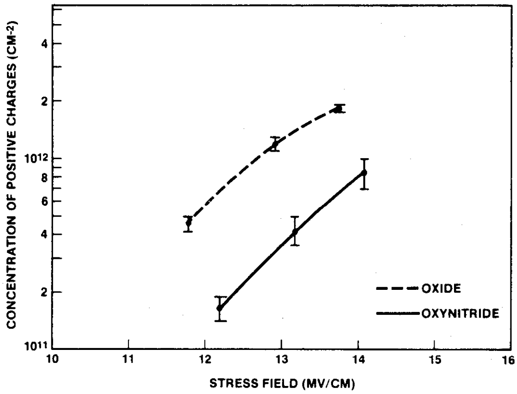


FIGURE 4. **Comparison of Positive Charge Trapping at Tunneling-Dielectric/Si Interface.**

In order to determine the data retention capability of SEEQ's products, unbiased devices are subjected to high temperature bake at 250 degrees C. The failure mode is a change in the state of the memory cell, and the typical failure mechanism is a dielectric defect resulting in "charge loss". Because dielectric defects can be induced by the electric fields generated during write/erase cycles, data retention and endurance are related topics. The effects of cycling on data retention are covered in the endurance section. In this section, the intrinsic data retention characteristics are evaluated and compared against the minimum data retention goal of ten years.

Units to be stressed are drawn from finished goods inventory and erased to an all 1's pattern (e.g., negative charge on floating gate). After erasing and initial testing, parts were temperature stressed at 250 degrees C. Voltage stress is not required for this evaluation; therefore, all leads are held at ground potential.

The results are summarized in Table 3. Using an activation energy of 0.6 ev, the data retention lifetime predicted by the data exceed 100 years at a 55 degrees C temperature. This period exceeds the industry 10 year standard for erasable memories.

Endurance

Endurance is defined as the ability of an EEPROM to operate to data sheet specifications after repeated write/erase cycles to each byte. SEEQ specifies an endurance option of either 10,000 or 1,000,000 cycles/byte. The extraordinary high endurance is accomplished using SEEQ's proprietary oxynitride process and its innovative Q-Cell design. Products which are specified with 1,000,000 cycle endurance are designated with "55" series part numbers.

Endurance failures are characteristically caused by dielectric breakdown occuring in the tunnel dielectric itself. This breakdown is associated with charge trapping

Table 2. High Temperature Dynamic Life Stress Results

Product	Total Devices Stressed	Total Devices Stress Hours	Stress Temperature	Number of Failures	Predicted Failure Rate @ 90% Confidence @ 55°C (Ea = 0.4 eV)
52B13	1089	1,009,000	125°C	1	0.034%/1000 hrs.
2816/2817	1307	1,782,000	125°C	3	0.033%/1000 hrs.
36C16	80	14,720	150°C	0	0.7118%/1000 hrs.
52B33	1086	1,142,000	125°C	2	0.0112%/1000 hrs.
2864	370	467,000	125°C	1	0.0411%/1000 hrs.
2864	77	38,500	150°C	1	0.459%/1000 hrs.
28C64	237	157,000	125°C	1	0.145%/1000 hrs.
28C64	157	53,536	150°C	0	0.196%/1000 hrs.
28C256	350	230,302	125°C	3	0.258%/1000 hrs.
28C256	77	38,500	150°C	1	0.459%/1000 hrs.

that occurs during repeated write/erase cycles. Because this behavior is central to the device physics of an EEPROM memory cell, endurance will be discussed in two parts; first, at the cell level, then, at the product level.

During each write/erase operation of a floating-gate EEPROM cell, a miniscule amount of charge is trapped in the dielectric through which the programming charge tunnels (Ref. 1). The cumulative effect of this charge trapping has a strong impact on the effective threshold voltage that the cell exhibits at each write/erase cycle. The envelope of the "written" threshold voltage and the "erased" threshold voltage plotted over a number of cycles is referred to as the cell threshold "window" and is a key figure of merit for any EEPROM cell. Referring to the representative threshold window shown in Figure 3 the net effect of charge trapping results in an initial widening of the window (due to positive trapped charge). Ultimately, negative charge trapping sets the upper limit on endurance when the window becomes too narrow to be useful.

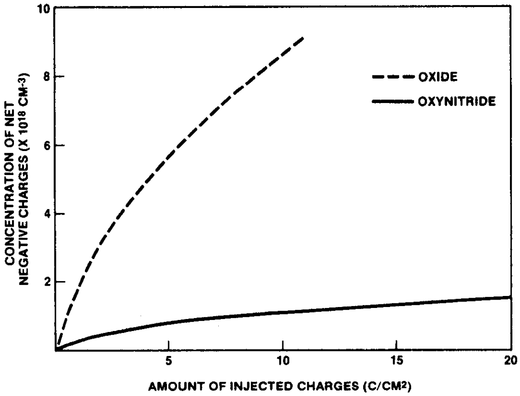


FIGURE 5. **Comparison of Negative Charge Trapping**

As seen from the endurance plot of Figure 3, the threshold window achieved using the SEEQ oxynitride dielectric represents an improvement over the traditional silicon dioxide case by at least a factor of ten. The oxynitride window demonstrates very little closing at 10^6 cycles, and provides a very useable window at 10^7 cycles.

The improved performance of oxynitride over oxide is directly related to the superior trapping characteristics of the oxynitride film, as shown in Figures 4 and 5. In Figure 4, the positive charge trapping characteristics of oxynitride and oxide are compared as a function of field strength (the principal independent variable). The positive charge trap density is consistently lower for oxynitride by approximately a factor of four. In Figure 5, the negative charge trapping characteristics of oxynitride and oxide are compared as a function of total injected charge (the principal independent variable in this case). Note the benefit of oxynitride in this case continues to increase with increasing charge, thus verifying the endurance improvement first observed in Figure 3.

Units were pulled from finished goods inventory and stressed by performing repeated write/erase cycles on every byte in the memory. Data retention, read/write functionality, AC performance, and parametrics were periodically tested against data sheet specs. Failures (typically caused by the selective failure of random bits) were analyzed and compiled for failure rate calculations.

A summary of the results is shown in Table 4. It shows that all of SEEQ's EEPROMs meet or exceed the intrinsic MOS failure rate of 0.05%/1000 hours if you write once per day. It should also be noted that the Q-Cell EEPROMs have higher endurance than the non Q-Cell 52B13. All of SEEQ's EEPROMs are Q-Cell except for the 52B13. For applications where writing occurs more frequently or where a failure rate of less than 0.03%/1000 hours is required, then a 1,000,000 cycle part such as the 16K 5516A should be considered.

Reference

(1) Ching S. Jeng et al, IEDM Technology Digest 1982, p. 811.

Table 3. High Temperature Bake Test Results

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 250° C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.6 eV)
52B13	82	118,000	2	0.0023%/1000 hrs.
2816	133	133,000	0	0.00087%/1000 hrs.
52B33	100	50,000	0	0.0014%/1000 hrs.
28C256	15	2,520	0	0.0461%/1000 hrs.

Table 4. Write/Erase Endurance Test Results

Product	Total Devices Stressed	Total Device Stress Cycles	Number of Failures	Predicted Failure Rate @ 90% Confidence (Ea = 0.125 eV)	Failure Rate with One Write Cycle per Day
52B13	189	4,400,000	5	0.305%/1000 cycles	0.013%/1000 hrs.
2816/2817	8917	3,355,820,000	190	0.009%/1000 cycles	0.0004%/1000 hrs.
5516	7481	7,798,000,000	88	0.0018%/1000 cycles	0.00008%/1000 hrs.
52B33	4013	1,787,810,000	68	0.006%/1000 cycles	0.0003%/1000 hrs.
2864	434	35,100,000	6	0.043%/1000 cycles	0.0018%/1000 hrs.
28C64	240	2,400,000	5	0.555%/1000 cycles	0.023%/1000 hrs.
28C256	450	45,000,000	11	0.0529%/1000 cycles	0.002%/1000 hrs.

Accelerated stress is updated quarterly and is available from SEEQ Technology.

seeq

Radiation and MOS Non-Volatile Memories

Introduction

The effect of radiation on non-volatile memories is of concern when the devices may be exposed to radiation and are expected to continue functioning. Such environments include space, non-hardened battlefield conditions or commercial radiation applications. SEEQ EEPROM's have demonstrated similar performance as other MOS memories and can be successfully used in the above listed environments, as well as other applications requiring functionality during and after radiation exposure. SEEQ EEPROM's have proven particularly resistant to single event upsets.

Concerns

A. Permanent damage is a function of:

1. Total dosage of ionizing radiation;
2. Neutron flux;
3. Gamma dose rate.

B. Transient errors (single event upset) are a function of:

1. Charged particles, e.g. Cosmic rays
2. Gamma dose rate.

Failure Mechanisms

A. Permanent Damage:

1. Build up of trapped charge in dielectrics, primarily gate oxides; caused by charge generated by the radiation flux congregating at defects in the oxide. This results in threshold shifts and subsequent non-functionality.
2. Build up of interface states caused by charge generated by the radiation flux accumulating at layer boundaries. This results in degradation in transconductance and threshold shifts and subsequent non-functionality.
3. Formation of interstitials and vacancies in the crystal lattice structure caused by neutron flux. This results in changes in the electrical characteristics of the bulk silicon and subsequent non-functionality.

B. Transient Errors:

1. Generation of false electrical signals from photocurrents in semi-conductor junctions caused by high energy particles or gamma rays. These result in data upset during read.

Models

A. Total dose ionizing radiation: Simulated by exposure to gamma rays, usually from a Co 60 source. Expect MOS devices to withstand 10^3 to 10^4 rad (Si) of total dose before permanent damage. Variables include:
1. Thinner gate oxides are less likely to trap charge.
2. Bias applied during irradiation aggravates charge trapping.

B. Dose rate: Simulated by exposure to gamma rays usually generated by a linear accelerator. Expect MOS parts to withstand 10^6 to 10^7 rad(Si)/sec before transient damage and 10^9 to 10^{10} rad(Si)/sec before permanent damage.

C. Neutron flux: Simulated by exposure to neutrons, usually generated by a nuclear reactor. Expect MOS parts to withstand greater than 10^{14} neutrons/cm^2.

D. Cosmic rays: Simulated by exposure to high energy, heavy ions, usually generated by a particle accelerator. Baseline standards are not well established for MOS parts.

Data for SEEQ MOS parts (see tables)

A. Total dose is as expected for a thin oxide, MOS part.

B. Dose rate for both transient and permanent damage is typical for MOS parts.

C. No data for neutron flux, but expect to be similar to other MOS parts, e.g. greater than 10^{14}/cm^2.

D. Data for single event upset (SEU) is using different ions to simulate worse case cosmic rays. The parts perform better than expected.

Definitions

A. Curie—A quantity of radioactive material undergoing 3.7 times 10^{10} disintegrations per second.

B. Rad—Radiation Absorbed Dose— The absorbtion of 100 ergs of radiation energy per gram of absorbing material.

C. Roentgen—The amount of gamma rays required to produce ions carrying 1 electro-static unit of charge in 1 cubic centimeter of dry air.

D. REM—Radiation Equivalent (in) Man—The measure of the biological effect of radiation exposure is obtained by multiplying the absorbed dose (in rads) by a "quality factor" for the particular radiation.

E. Radioactivity—The spontaneous emission of radiation, e.g. particles and/or electro-magnetic waves (photons), from the nuclei of an unstable isotope, which eventually decays to a stable non-radioactive isotope.

Radiation Test Results

			16K EEPROM (5516A/2816A, 5517A/2817A, 52B13)	64K EEPROM (52B33, 2864)
Stress	**Conditions**	**Failure Mode**	**Failure Range**	**Failure Range**
Unbaised total dose	Alternating data patterns, (e.g. 1st exposure all 0's, next exposure all 1's) Co 60 gamma ray source (10 RAD/SEC)	Device will read but some locations fail to write	9000 ± 2000 RAD (Si)	6500 ± 500 RAD (Si)
Biased total dose	Alternating data patterns, (e.g. 1st exposure all 0's, next exposure all 1's) Co 60 gamma ray source (10 RAD/SEC)	Device will read but some locations fail to write Read only	3000 ± 1500 RAD (Si)	3000 ± 500 RAD (Si) 11,000 (±) 2500 RAD (Si)
Biased dose rate upset	Erased (1's state), linear accelerator gamma ray source	Upset during read; not permanent	3 ± .75 X 10^7 RAD (Si)/SEC	1.6 ± .02 X 10^7 RAD (Si)/SEC
Biased dose rate survival	Erased (1's state), linear accelerator gamma ray source (200 RAD/20 ns PULSE)	Device will read, all locations fail to write	> 10^{10} RAD (Si)/SEC	~10^{10} RAD (Si)/SEC

			256K EPROM (27C256)	
Stress	**Conditions**	**Failure Mode**	**Failure Range**	
Biased total dose	Memory Programmed to all 0's, Exposed to Co60 source (1 to 35 RAD/SEC)	Device Fails to Read, Multiple bits read 1's	15,000 (±) 2,000 RAD (Si)	

Radiation Test Results

256K EEPROM
(28C256)

Stress	Conditions	Failure Mode	Failure Range
Biased Dose Rate upset	Byte Checkerboard Data Pattern; 54 ns to 1.5 us Pulse Widths; Linear Accelerator	Single Bits Change State	1.1×10^9 to 6.6×10^{10} RAD (Si)/SEC
Biased Dose Rate Lock-Up	Byte Checkerboard Data Pattern; 54 ns to 1.5 us Pulse Widths; linear Accelerator	Parts Fail to Read, Recover After Power Down	5×10^7 to 1×10^8 RAD (Si)/SEC
Biased total dose	Alternating data patterns (e.g. 1st exposure all 0's, next exposure all 1's Co 60 gamma ray source (10 RAD/SEC)	Device will read but some locations fail to write Read only	~10,000 RAD (Si) ~20,000 RAD (Si)

16K EEPROM
(36C16)

Stress	Conditions	Failure Mode	Failure Range
Biased total dose	Alternating data pattern (e.g. checkerboard) Co 60 gamma ray source (125–200 RAD/SEC)	Single Bits Fail to Write Read	10,000 ± 2000 RAD (Si) 20,000 ± 2000 RAD (Si)

Single Event Upset
64K EEPROM (52B33)

Samples were programmed and subjected to different levels of radiation to simulate a cosmic flux.

The devices are read after irradiating for upsets

RUN #	IONS	LET	FACILITY	ENERGY	RAD H20	TIME	UPSETS
1	Fe	8	BEVATRON		144	30 SEC	NONE
2	Fe	6	BEVATRON		144	30 SEC	NONE
3	Fe	4	BEVATRON		288	2 MIN	NONE
4	Fe	3.8	BEVATRON		288	2 MIN	NONE
5	Kr	41	CYCLOTRON	200 MeV			NONE
	Ar	15.4	CYCLOTRON	160 MeV			NONE
	Ne	5.7	CYCLOTRON	88 MeV			NONE
	O	1.8	CYCLOTRON	217 MeV			NONE
	N	2.9	CYCLOTRON	68 MeV			NONE
6	P	.004	CYCLOTRON	148 MeV			NONE
7	CF-252	42		105 MeV			NONE

256K EEPROM (28C256)

RUN #	IONS	LET	FACILITY	ENERGY	RAD H20	TIME	UPSETS
1	CF-252	42	–	105 MeV			NONE

Memory Products Reliability Note

1

CALCULATION OF EEPROM BOARD MTBF

November 1987

RELIABILITY

seeq

Technology, Incorporated

Calculation of EEPROM Board MTBF

The increasing use of EEPROMs for large arrays of non-volatile memory storage has raised interest in how to calculate the MTBF (mean time between failures) of the resulting assembly. This paper will demonstrate how to calculate the board MTBF as well as compare the results of using different EEPROM technologies and failure rates. Even though the microcircuit failure rate is among the least significant factors in board failures, the effects of other components will be ignored for the purpose of simplicity.

The MOS Floating Gate EEPROM has two reliability characteristics which require consideration beyond that of a normal MOS memory. Endurance, the number of times an EEPROM may be erased and re-programmed, is finite because of the effects of the Fowler-Nordheim tunneling current on the floating gate isolation dielectric(s). Data retention, the length of time the EEPROM will retain stored data, is finite because of the impossibility of permanently storing an electronic charge. The read or operating life reliability will be similar to other MOS memories of like density.

SEEQ builds EEPROMs with Q-Cell on-chip error correction in order to reduce the endurance failure rate. The cumulative reprogramming cycles in the operational life of the application must be less than the number of cycles before the onset of endurance wear-out; therefore, the average reprogramming frequency (cycles/hour) times the expected operational life of the application should be less than the typically specified 10,000 cycle endurance limit. During the operational life, the failure rate should be as low as possible in order to increase the system MTBF. The read and data retention failure rates of SEEQ EEPROMs appear similar to other vendors, although these rates should theoretically improve as a larger statistical data base is acquired.

Mil-Hdbk-217 is frequently used to calculate failure rates for microcircuits. Historically 217 has not made accurate predictions regarding LSI or VLSI devices such as MOS memories. This is exacerbated with EEPROMs that have the additional application-dependent considerations of data retention and endurance. In order to make accurate predictions of expected failure rates, manufacturers use data from accelerated stressing. This data is then de-accelerated to normal operating temperatures using the Arrhenius relationship and the apparent activation energy for the associated failure mechanism mortality function. Similar in methodology to operating life (read) calculations, failure rates for data retention in %/1000 hours and endurance in %/1000 cycles, may be calculated.

Most failure mechanisms are thermally accelerated, so with a lower operating temperature, the board MTBF will be longer. CMOS EEPROMs consume less current, both active and standby, than comparable NMOS EEPROMs. Therefore, the power requirements for CMOS-populated PCBs are less and the system will operate at a lower temperature.

In order to calculate the board MTBF, the number of EEPROMs, the read, endurance and data retention failure rates, the re-programming frequency, the rail temperature, the appropriate thermal resistances and the device power consumption must be known.

The calculation of the board MTBF is best illustrated through the use of an example. A comparison will be made between NMOS and SEEQ CMOS 256K bit EEPROMs to demonstrate the effects of power consumption, and the intrinsically lower endurance failure rate of SEEQ EEPROMs with Q-Cell on-chip error correction.

The following assumptions have been made:

1. Number of devices per board = 96; 3 active, 93 standby, during the operating life of the board.
2. The I_{CC} of each device at the operating temperature will be 50% of the maximum specified at −55 degrees C. and maximum operating frequency. Programming I_{CC} is slightly less than read I_{CC}; therefore, programming I_{CC} will be ignored. The devices are operated at a nominal 5 volts.
3. The average re-programming frequency is once every 8 operating hours.
4. The rail (heat sink) temperature is 71 degrees C. Uniform heat dissipation across the PCB.

5. Thermal resistances:
   a. board – rail, Θbr: 3° C/W
   b. case – board, Θcb: 2.5° C/W
   c. junction – case, Θjc: 20° C/W
6. Base failure rates are at 55 degrees C. and 90% Confidence Interval. Failure rates are accelerated according to the Arrhenius relationship, with following apparent activation energies (Ea):
   a. read: .4 ev.
   b. data retention: .6 ev.
   c. endurance: .12 ev.
7. The characteristics for the SEEQ 28C256 EEPROM are:
   a. I_{CC} active: 60 ma. max.
   b. I_{CC} standby: 250 μa. max.
   c. read failure rate: .02%/1000 hours
   d. data retention failure rate: .001%/1000 hours
   e. endurance failure rate: .05%/1000 cycles
8. The characteristics for the NMOS EEPROM are:
   a. I_{CC} active: 120 ma. max.
   b. I_{CC} standby: 60 ma. max.
   c. read failure rate: .02%/1000 hours
   d. data retention failure rate: .001%/1000 hours
   e. endurance failure rate: .2%/1000 cycles
9. The basic equations to be used are:
   a. junction temperature = (rail temperature + Θbr * PDboard) + (Θcb * PD part) + (Θjc * PDpart)); where Θxx is the appropriate thermal resistance and PDxx is the appropriate power dissipation.
   b. power dissipation/part = V_{CC} nominal * I_{CC} max * 50%.
   c. Power dissipation/board = (3 * PDactive) + (93 * PDstandby).
   d. Arrhenius acceleration factor $= e^{\frac{Ea}{K}\left(\frac{1}{Tn}-\frac{1}{Tj}\right)}$; where K = Boltzman's constant (8.62×10^{-5}) and Tn and Tj are the normalized and junction temperatures expressed in degrees Kelvin.
   e. MTBF = (1/(# parts * failure rate)) * 10^5 See note.
   f. Board MTBF = (1/(# parts * (failure rate read + failure rate retention + failure rate endurance)) * 10^5.

The results of the calculations are summarized in the following table:

TABLE 1

PARAMETER	CMOS	NMOS
Device power dissipation		
active	0.150 watts	0.300 watts
standby	.000625 watts	0.150 watts
Board power dissipation	0.5081 watts	14.85 watts
Rail temperature	71°C	71°C
Board temperature	72.52°C	115.55°C
Case temperature	72.89°C	116.3°C
Junction temperature	75.89°C	122.3°C
Failure rates at calculated T_J		
read	.0466 %/1000 hrs	.2223 %/1000 hrs
retention	.0035 %/1000 hrs	.0370 %/1000 hrs
endurance	.0080 %/1000 hrs	.0514 %/1000 hrs
MTBF of Devices:		
read	22,318 hours	4,684 hours
retention	292,191 hours	28,097 hours
endurance	129,252 hours	20,229 hours
MTBF of BOARD	17,868 hours	3,350 hours

NOTE:
Actual MTBF $= \frac{1}{(1-(1-\text{failure rate})^{\#\text{ parts}})}$ but equivalent to $\frac{1}{(\#\text{ parts} * \text{failure rate})}$ for very low failure rates.

The approximately 500% improvement in MTBF through use of the SEEQ CMOS EEPROMs compared with the NMOS EEPROMs may be attributed to two factors: the almost 50 degrees C. higher junction temperature caused by the higher power dissipation of the NMOS parts significantly accelerated the read and data retention failure rates; and the initial lower endurance failure rate of the SEEQ CMOS EEPROMs, which is not greatly affected by temperature.

Each application will have different initial conditions; however, through use of the above equations a board MTBF may be calculated. The board failure rate will always be reduced through the use of a CMOS EEPROM with lower power requirements and will always be reduced when using a SEEQ EEPROM with a lower endurance failure rate.

8

APPLICATIONS

(Application Notes)

Memory Products Application Note

2

MICROPROCESSOR INTERFACING WITH SEEQ's LATCHED EEPROM

March 1985

APP. NOTES

seeq
Technology, Incorporated

Microprocessor Interfacing with SEEQ's Latched EEPROM

Introduction

This application note describes the interfacing of SEEQ's "latched" Electrically Erasable Read Only Memory (E^{2}ROM or E^2) to a microprocessor bus. The latched E^{2}ROM family is comprised of a 16K 52B13 and 64K 52B33. On each of these devices there are internal latches on all inputs except write enable. A byte must first be erased before it can be written. In addition to the latched E^{2}ROM family, SEEQ has a timer E^{2}ROM family. This family is comprised of a 16K 2816A (24 pins), a 16K 2817A (ready/busy) and a 64K 2864 (ready/busy). The timer family has internal latches on all inputs and has an internal timer which automatically performs a byte erase before write. In this application note, the E^2 used is SEEQ's 52B13, a 2K x 8 memory. Since the timing of the higher-density members of the family is compatible, the circuits given can be extended to interface equally well with the 52B33 (8K x 8). Both bus timing and software timing are used to gate the control signals. The case presented here uses general control signals to permit adaptation to any system's bus structure. In addition, modifications are given for interfacing to specific processors.

Interface Signals

The solution presented here (see Figure 1) uses an $\overline{\text{S}}-\overline{\text{R}}$ flip-flop (74LS00) with TTL gates (74LS32) to latch $\overline{\text{WE}}$ for the 52B13. This flip-flop causes valid data to be latched correctly, satisfies device setup and hold times, and allows easy latch/unlatch of the $\overline{\text{WE}}$ signal.

The system-dependent direct bus interface components form the second part of the interface circuit. These components will generate $\overline{\text{CHIP SELECT}}$ and $\overline{\text{E}^2\text{ROM SELECT}}$ to enable this part of memory. $\overline{\text{CHIP SELECT}}$ is usually generated separately for each word-wide group of devices. In this way, it chooses the actual devices to be written. $\overline{\text{E}^2\text{ROM SELECT}}$ would be an "OR" function of the $\overline{\text{CHIP SELECT}}$ signals for all the devices for which this latch gates $\overline{\text{WE}}$. With $\overline{\text{WE}}$ wired in common, only one gated latch is required for the E^{2}ROM array. Of course, fanout must be considered, with a high-current driver used if necessary. In the example bus interfaces shown in this application note, gating for one device is assumed, and $\overline{\text{E}^2\text{ROM SELECT}}$ is tied directly to $\overline{\text{CHIP SELECT}}$.

The bus interface components perform other tasks common to a memory/bus interface. For a multiplexed data bus, the bus interface components must demultiplex the data and addresses. In addition, this bus interface circuitry may generate $\overline{\text{MEMORY READ}}$ and $\overline{\text{MEMORY WRITE}}$, if required. Details of this bus interface are given in the section "Considerations for Special Applications," beginning on page 5.

Details of Operation

Byte Write or Erase

The timing diagram in Figure 2 shows the details of a byte write or erase operation for SEEQ's latched E^{2}ROM family. The two modes are the same, except that hex "FF" is presented to the I/O lines for erasure. Due to this similarity, only the write mode will be discussed.

The first step is initiation of a write cycle. First, the processor issues addresses, and the system's decoding circuitry brings $\overline{\text{CHIP SELECT}}$ valid. Although the chip is enabled at this point, a write to the chip has not yet begun, because $\overline{\text{MEMORY WRITE}}$ has

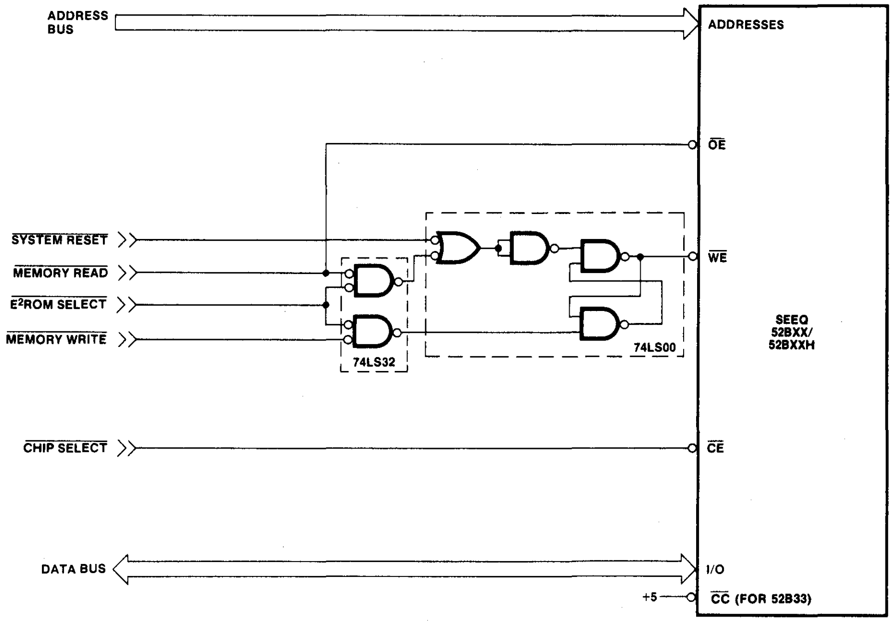


Figure 1. E²ROM Interface Circuit

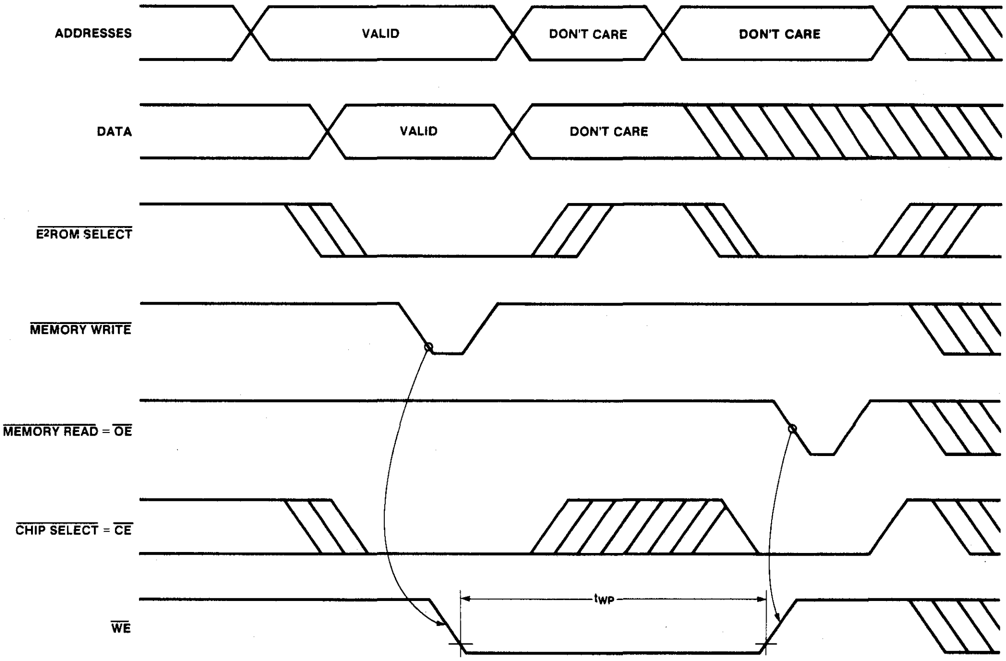


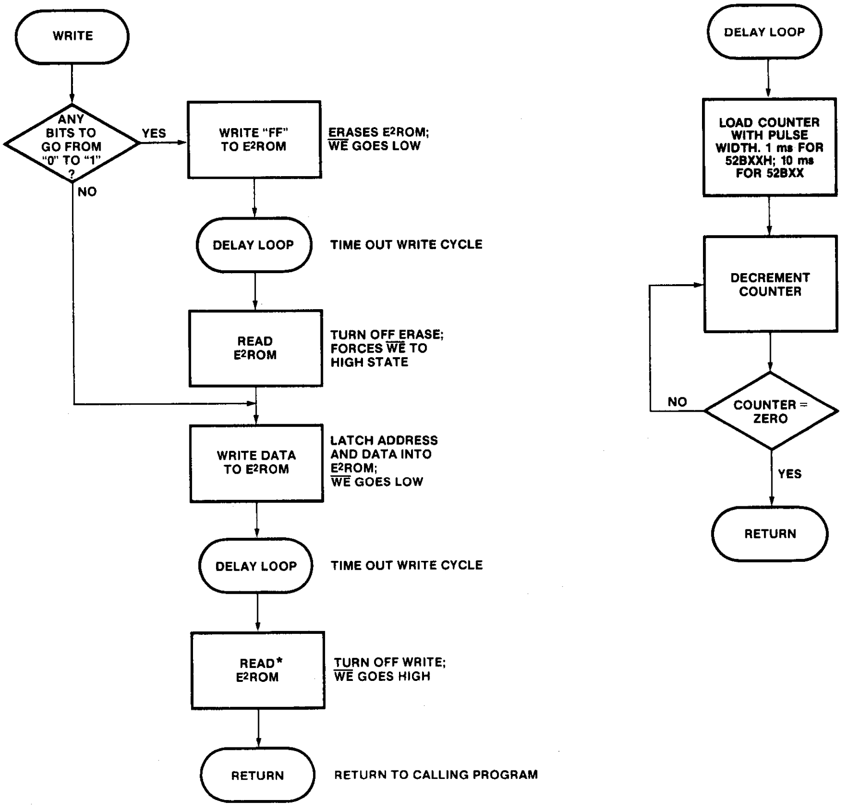
Figure 2. Write-Cycle Timing Diagram Latched E²ROM Interface Application

not yet been issued. This prevents inadvertently writing to an incorrect address as the address lines are allowed to settle out before a write is initiated. Following the timing events above, the active level of $\overline{\text{MEMORY WRITE}}$ sets the flip-flop, bringing $\overline{\text{WE}}$ low to the E^2. Data, Addresses, $\overline{\text{CE}}$, and $\overline{\text{OE}}$ are latched at this point.

In the second part of a write, $\overline{\text{WE}}$ continues to be active low for the entire write cycle. This requires a timeout, which can be effected in any of several ways. The designer can use a timing loop in software, or trigger a timer which interrupts the processor after the correct time. The software timeout may require less hardware on-board. The hardware timeout, on the other hand, allows the CPU to perform other tasks. Obviously, a good compromise is a software architecture with regular (perhaps one-millisecond) timing interrupts, for system real-time synchronization. Division of the task between hardware and software is best left to the individual systems engineer.

Regardless of the method used in the timeout, the write pulse is terminated by $\overline{\text{WE}}$ being brought high. This is effected by a read to any location in the device, which resets the flip-flop to bring $\overline{\text{WE}}$ high. A second read cycle is required for byte verify. System designers should allow extra time between the two reads to meet write recovery time (t_{WR}) requirement. This method of write-cycle termination provides another form of protection against inadvertent writing to the chip. Even if a statistically unlikely succession of glitches were to trigger both flip-flops, enable the gates, and bring $\overline{\text{WE}}$ low, a subsequent read to the device could terminate the write before data would be written.

For the case of a fully software-timed write, a flowchart is given for the sequence of operations (see Figure 3). This processor-independent flowchart handles all the erasure and writing for storing data in the E^{2}ROM, using the circuit from Figure 1. In addition, a segment of example code (written for the Z8) is shown (see Figure 4).



*Data is not valid during this cycle.

Figure 3. Flowchart for 52BXX Erase/Write — Software Timing

```
                   //-----------------------
                   // The following is a general routine for writing
                   // data contained in the working register
                   // DataReg to an EEROM in
                   // the location pointed to by the working register
                   // pair AdReg. This EEPROM is assumed to be in the
                   // external data memory of Z8.
                   // Write FF to erase byte.
P 0060 7C  FF      EEWR:   LD      OutReg, #%FF
P 0062 92  70              LDE     @AdReg,  OutReg
P 0064 D6  0071            CALL    WaitWP             // Wait for Twp
P 0067 82  80              LDE     NowReg, @AdReg   // Turn off WE
                   // Now, write the data to the part.
P 0069 92  90              LDE     @AdReg, DataReg
P 006B D6  0071            CALL    WaitWP             // Wait for Twp
P 006E 82  80              LDE     NowReg, @AdReg   // turn off WE

P 0070 AF          FinWr:  RET              //return from routine
                   // End of EEPROM Write Routine
                   //-----------------------------------------------

                   // Timing routines
P 0071 EC  0A      WaitWP: LD      RLoop2, #Twp  // # of ms to wait
                                            // 10-> wait 10 mS.
                                            // 1 -> Wait 1  mS.

P 0073 D6  007E    WPLoop: CALL    Wait1ms
P 0076 00  EE              DEC     RLoop2
P 0078 6D  007D            JP      Z, DunWP
P 007B 8B  F6              JR      WPLoop
P 007D AF          DunWP:  RET              // Done with Twp.

                   // Basic 1 msec timing routine-
                   // adjust for microprocessor crystal freq.
                   // The value of Hex58 (Dec88) works with
                   // a Z8 with a 6.144 MHz xtal.
                   // Use %6A for 7.3728 MHz xtal. Elimination
                   // of NOP, or xtal substitution, will
                   // require recalibration.
P 007E FC  6A      Wait1ms: LD     RLoop3, #%6A

P 0080 FF          Timlp:  NOP
P 0081 00  EF              DEC     RLoop3
P 0083 6D  0088            JP      Z, Dun1ms
P 0086 8B  F8              JR      Timlp

P 0088 AF          Dun1ms: RET              // Done with wait

                   //End of EEPROM Timing Routines
                   //---------------------------------
```

Figure 4. Sample Z8 Code for 52BXX Write

Read Operation

The timing for a read (see Figure 5) is simpler than for a write. In the read mode, the on-chip latches are transparent. The leading (falling) edge of $\overline{\text{CHIP SELECT}}$ brings $\overline{\text{CE}}$ low, and the falling edge of $\overline{\text{MEMORY READ}}$ brings $\overline{\text{OE}}$ low. Data is available from the 52BXX E²ROM after a delay of T_{OE} (from $\overline{\text{OE}}$) or T_{CE} (from $\overline{\text{CE}}$). Table 1 shows the T_{ACC} required for operation with sample microprocessors, using no wait states. Memory devices currently available from SEEQ feature T_{CE} as fast as 200 nanoseconds. For certain new microprocessors (for example, the 68000 or 8085A-1) which may require faster access, SEEQ is currently developing memories with access times of 150 nanoseconds or less.

To terminate the read, the rising edge of $\overline{\text{MEMORY READ}}$ brings $\overline{\text{OE}}$ high. $\overline{\text{CE}}$, however, is dependent only on $\overline{\text{CHIP SELECT}}$, and remains active low for the entire microprocessor cycle.

Table 1. Zero-Wait State Required Minimum T_{ACC} (Assuming zero delay for buffers and drivers)

Microprocessor	Clock Freq. (MHz)	Required T_{ACC} (nanoseconds)
72720	10	350
8085A/8085AH	3	460
8085A-2/8085AH-2	5	270
8085A-1/8085AH-1	6	175
8086/8088	5	402
8086-2/8088-2	8	267
8086-1	10	227
Z8	8	310
Z80	2	575
Z80A	2.5	325
Z80B	6	190
6800	1	605

Considerations for Special Applications

Use with Z8, Z8000 Systems

The implementation of the circuit shown in Figure 1 in a Z-Bus application allows simple generation of the control signals. First, the control signals $\overline{\text{MEMORY READ}}$ and $\overline{\text{MEMORY WRITE}}$ can be generated by one half of a 74LS139 decoder, as in Figure 6. In addition, for the Z8, the lower byte of addresses must be latched, due to the multiplexing of address and data. This can be easily accom-

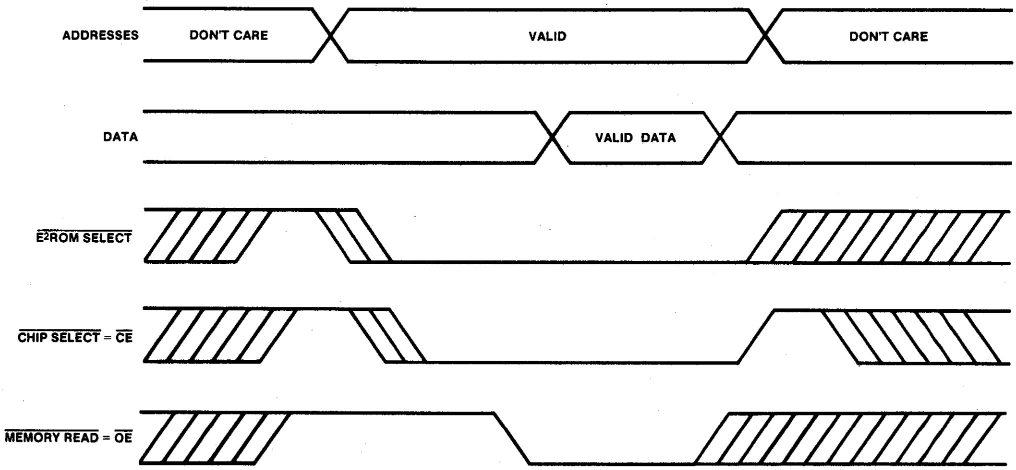


Figure 5. Read-Cycle Timing Diagram

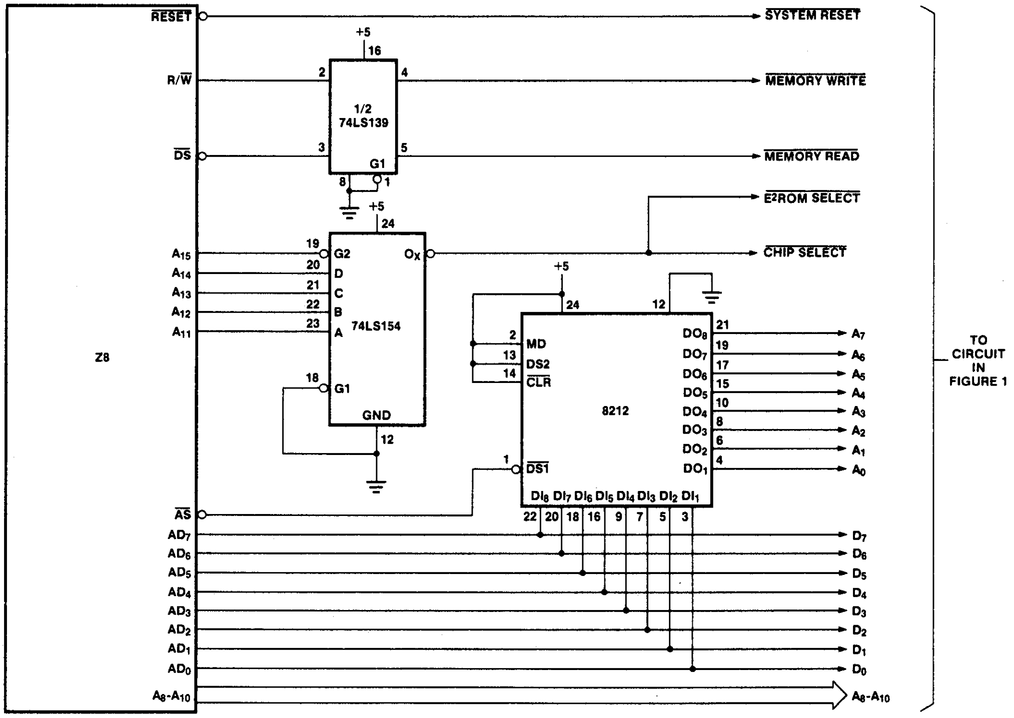


Figure 6. Interfacing to a Z8

plished with an 8212 octal latch, as in Figure 6. Interfacing to a Z8000 (or 16-bit Z-Bus) requires an additional 8212 latch, to demultiplex AD_8-AD_{15}. $\overline{AS}$, the Z-Bus address strobe, is active low, and must be connected to the active low input in order to clock these latches.

Use with Z80 Systems

The circuit shown in Figure 7 provides a bus interface to a Z80, Z80A, or Z80B processor. In Figure 7, $\overline{\text{MEMORY READ}}$ and $\overline{\text{MEMORY WRITE}}$ are generated from combining $\overline{\text{MREQ}}$ with the Z80 $\overline{\text{RD}}$ and $\overline{\text{WR}}$, respectively, Since address and data are issued by the Z80 processor on separate lines, the 8212 latch is not needed.

Use with 8085 Systems

The implementation of the E²ROM interface circuit in an 8085 system is extremely simple. Figure 8 shows the bus interfacing necessary. $\overline{\text{MEMORY READ}}$ and $\overline{\text{MEMORY WRITE}}$ are issued by the processor directly. However, $\overline{\text{MEMORY WRITE}}$ must be delayed, as shown in Figure 8, to ensure latching of valid data. $\overline{\text{CHIP SELECT}}$ is generated from the top 5 address bits and IO/$\overline{\text{M}}$, using a 74LS154 decoder. The $\overline{\text{RESET}}$ to the 8085 processor also supplies $\overline{\text{RESET}}$ for the E²ROM interface. Finally, the demultiplexing of address and data lines is accomplished by a 74LS373 latch triggered by ALE. Alternatively, an 8212 latch can be used but requires more board space.

Interfacing to 8088/8086 (Minimum Mode) Systems

The above considerations for implementation of this solution in an 8085 system also apply to an 8088/8086 system operation in minimum mode, with two additions. As above, the processor issues ALE, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and multiplexed address/data. However, an inverter is required in order to produce IO/$\overline{\text{M}}$ from $\overline{\text{M/IO}}$. In addition (for an 8086), another octal latch must be added, in order to demultiplex AD_8-AD_{15}.

The time delay indicated in Figure 8 depends on the type of processor used and its clock frequency. For a 5 MHz 8088/8086, this time delay should be 100 nanoseconds; for an 8088-2/8086-2 at 8 MHz, it should be 60 nanoseconds. For a 10 MHz 8086-1, the time delay should be 50 nanoseconds.

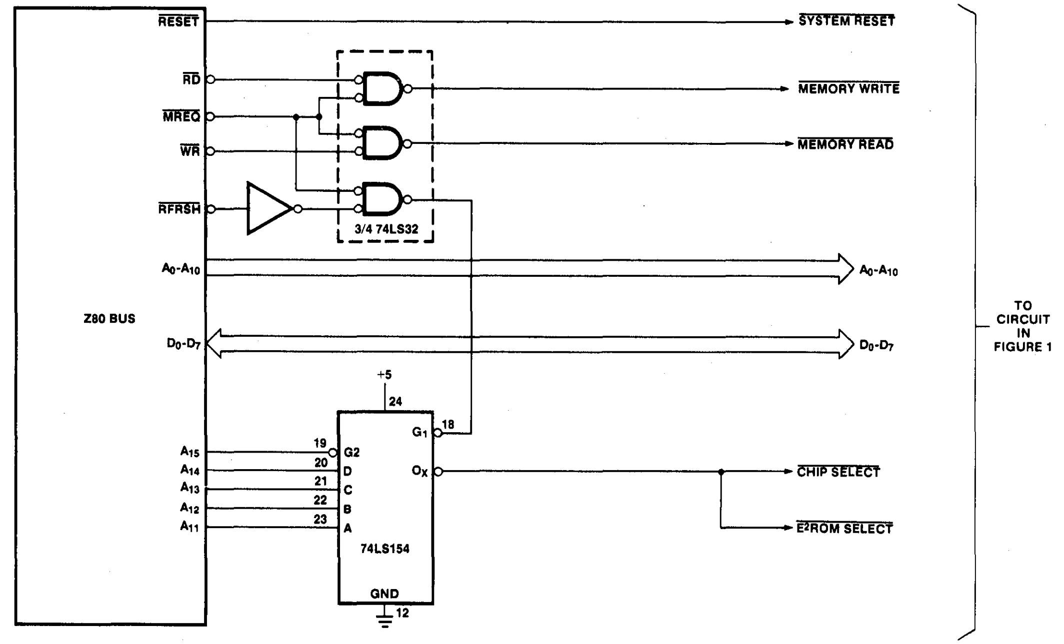


Figure 7. Bus Interface — Z80

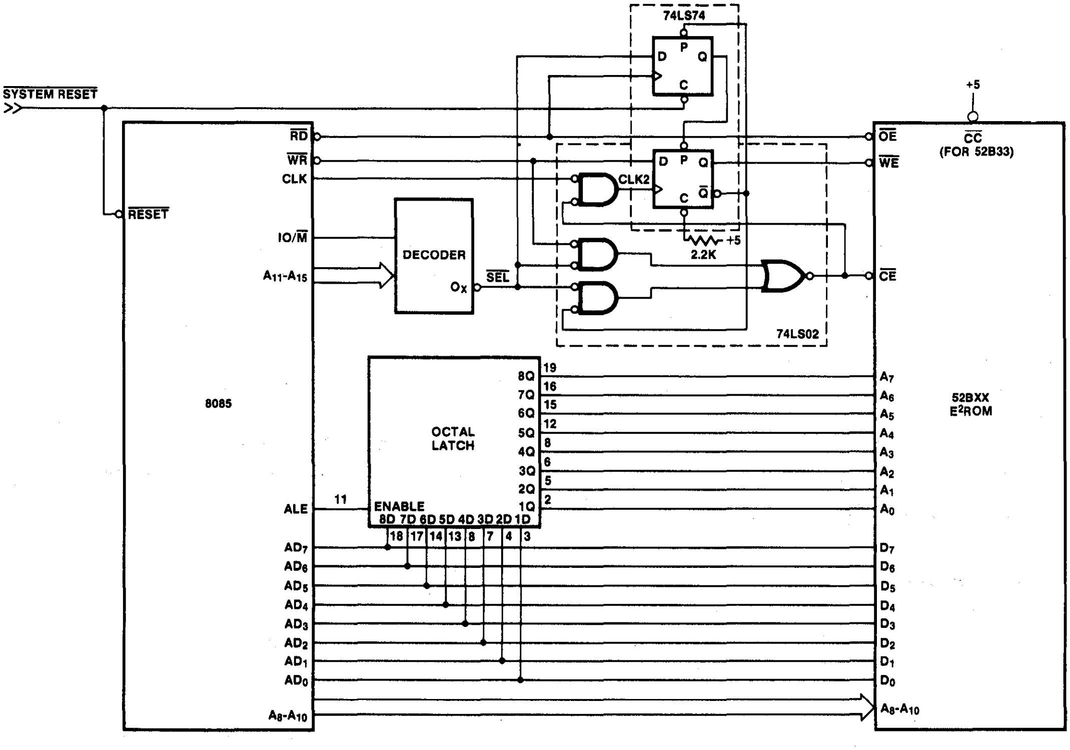


Figure 8. Bus Interface Circuitry — 8085 System

Interfacing with 72720 Systems

The 52BXX E^{2}ROM can be interfaced to SEEQ's new 72720 microcomputer (with 2K x 8 on-board E^{2}ROM) more easily than to any other processor. The 72720 PRG instruction operates off-board, to program an external E^{2}ROM. This instruction initiates latching and timing of $\overline{WE}$, as well as presentation of valid data. These tasks are handled automatically within the 72720. As a result, the write enable latch circuit of Figure 1 is not required. Total 52BXX interface hardware, shown in Figure 9, is very simple, even including a 74LS373 latch to demultiplex the lower eight bits of address. The software required for programming is shown in Figure 10. This example subroutine erases and writes one byte.

Interfacing with the 6800

One example of a complete interface between a 6800 processor and a 52BXX is shown in Figure 11. The DBE signal from the 6800 is delayed for a time between 250 and 350 nanoseconds, in order to provide a strobe for valid data. This data strobe clocks R/$\overline{W}$ into the flip-flop at the correct time, so that the falling edge of $\overline{WE}$ can satisfy timing requirements with respect to valid address, data, and control signals.

Conclusion

This application note has been prepared to assist the designer in implementing the technology of latched E^{2}ROMs in systems requiring adaptability. The designer is encouraged to create new designs based on these ideas. E^{2}ROM technology, while still in its infancy, holds the promise of being the memory breakthrough for the eighties. With a reliably nonvolatile approach to alterable program memory, systems for control of avionics, manufacturing, and data acquisition can be enhanced in usefulness. With the timing to use the advanced technology of E^{2}ROMs, the system designer can incorporate more features now, while allowing still more flexibility for the future.

Z-Bus, Z8, Z8000, Z80A, Z80, and Z80B are trademarks of Zilog.

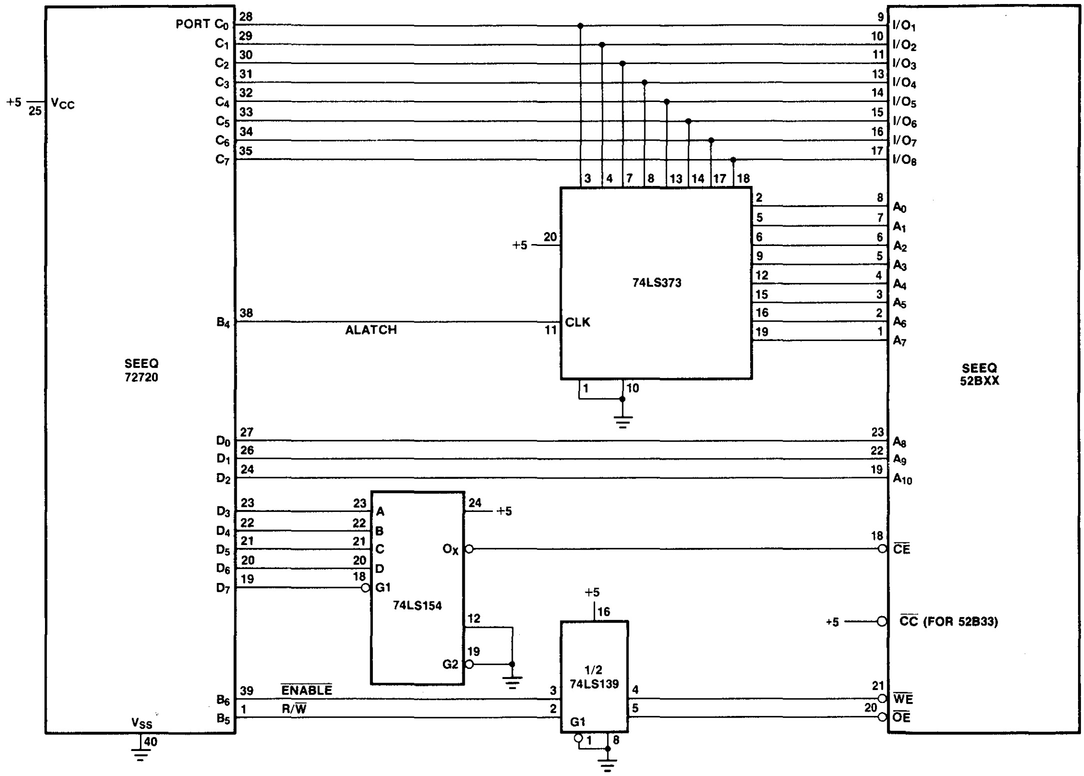
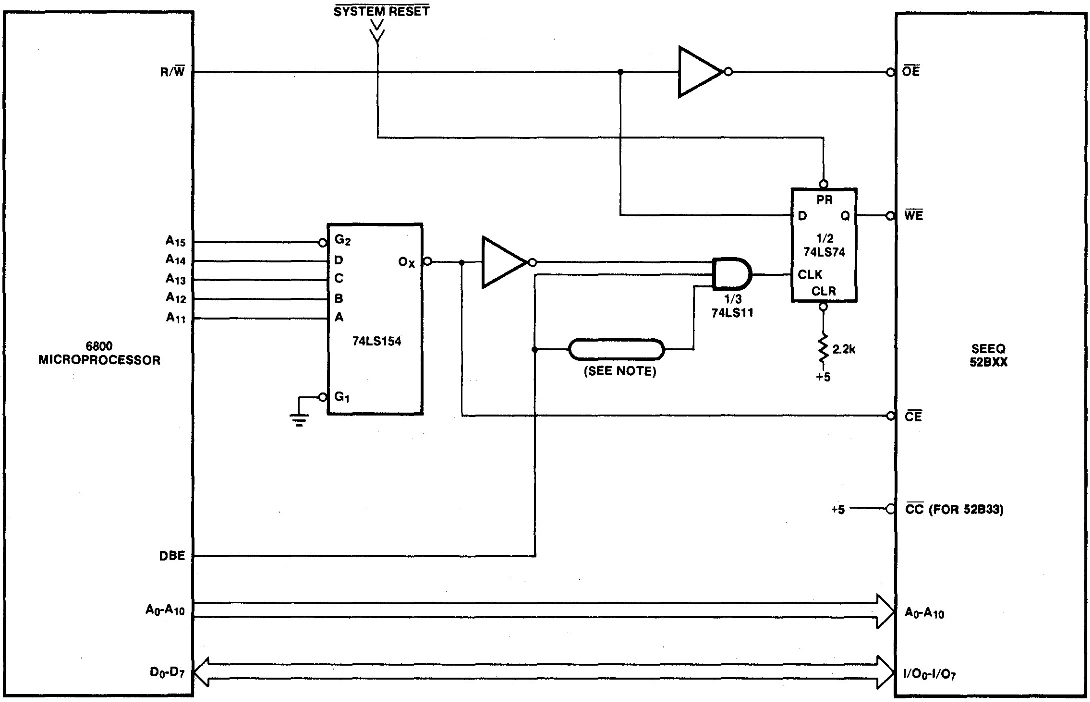


Figure 9. 72720 Interface

```
0 ERRORS
7000 ASSEMBLER  REV 1.3
>
0001  9000       ******************************************************
0002  9000       *                                                    *
0003  9000       *      EEROM  AUTO ERASE BEFORE WRITE ROUTINE        *
0004  9000       *                                                    *
0005  9000       *     DATA TO BE PROGRAMMED IN REGISTER 102          *
0006  9000       *   LOCATION TO BE PROGRAMMED IN REGISTERS 100/101   *
0007  9000       *                                                    *
0008  9000       ******************************************************
0010  9000       *
0020  9000 0066  EEDAT   EQU R102       DATA TO BE PROGRAMMED
0030  9000 0065  EEADR   EQU R101       POINTER TO LOCATION
0040  9000 B8    EEWR    PUSH A         SAVE ACCUMULATOR
0050  9001 22            MOV %>FF,A     IS LOCATION ALREADY ERASED?
      9002 FF
0060  9003 9D            CMPA *EEADR
      9004 65
0070  9005 E2            JEQ PROG
      9006 00
0080  9007 04            PRG *EEADR     IF NOT PROGRAM WITH FF HEX
      9008 65
0090  9009 12    PROG    MOV EEDAT,A    IF ERASED PROGRAM DATA
      900A 66
0100  900B 04            PRG *EEADR
      900C 65
0110  900D B9            POP A          RESTORE ACCUMULATOR
0120  900E 0A            RETS           RETURN
0130  900F               END
<
```

Figure 10. 72720 Code for Programming 52B13/33



NOTE: THIS ELEMENT OF THE CIRCUIT SHOULD DELAY A RISING EDGE (A TTL LOW-TO-HIGH TRANSITION) BY 250 (MIN) TO 350 (MAX) NANOSECONDS.

Figure 11. 6800/52BXX Interface

Communications Products Application Brief

5

INTERFACING THE 8003 EDLC® TO A 16-BIT BUS

March 1985

Technology, Incorporated

Interfacing the 8003 EDLC®
to a 16-Bit Bus

Introduction

The SEEQ 8003 Ethernet Data Link Controller (EDLC) chip together with the SEEQ 8023A Manchester Code Converter (MCC™) chip provide an economical two-chip solution for the Data Link Layer and Physical Layer of the Ethernet protocol. These chips are fully Ethernet compatible and suitable for use in terminals, personal computers, workstations, printers, disk drives and host computers.

The 8003 is a VLSI data link controller chip in a 40-pin package. It replaces approximately 60 MSI and SSI components in a typical Ethernet node configuration. The choice of which one to use is governed by the system interface requirements for the design. The 8003 provides protocol functions like frame formatting, link access control and error control. The part is optimized for Direct Memory Access techniques for frame storage.

The 8023A MCC Manchester Code Converter performs the signal encoding and decoding in Manchester Code at 10 million bits per second. It also monitors the channel for "carrier" and "collisions" (two nodes transmit simultaneously). Low-power CMOS technology is used in the 8023A, which is in the 0.3 inch 20-pin package.

Ethernet Node Configuration

A typical Ethernet node is shown in Figure 1. The System Interface on the left connects the host system bus to the network. This interface varies depending on processor and system requirements.

The station-resident hardware, consisting of the System Interface, the 8003 EDLC chip and the 8023A MCC chip, is connected to the Transceiver by the Access Unit Interface (AUI) cable. This cable consists of 78Ω balanced, shielded twisted-pair connections, DC biased at the station end and transformer-coupled at the Transceiver end.

Besides a passive tap to the Trunk Coax, the transceiver provides signal amplification, preconditioning on the receive path, impedance matching, DC isolation, collision detection and collision signaling generation. DC power for the Transceiver circuits is provided through the cable.

Host-Dependent System Interface

There are three basic methods for interfacing the CSMA/CD channel to the system bus. The first one employs First-In, First-Out (FIFO) buffer memory to temporarily hold the transmit and receive frames. On the system-bus side of the FIFOs, data is transferred serially a byte at a time by the processor. The second method uses Direct Memory Access to transfer data directly between the Ethernet Data Link Controller and the system memory. In the third method, Direct Memory Access is also used, this time with a temporary buffer memory intervening between the system memory and the EDLC chip. The intervening buffer relieves the system bus of some of the traffic and timing requirements associated with the channel. (For more information on DMA-type interfaces, see SEEQ's Application Brief 6).

MCC is a trademark of SEEQ Technology, Inc.

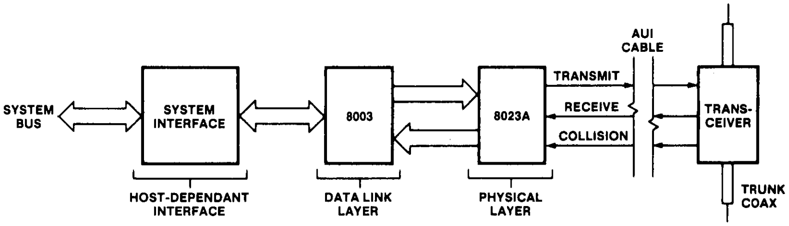


Figure 1. Ethernet Node Configuration

IEEE 802.3 CSMA/CD Standard Protocol for Local Area Networks (Alias Ethernet)

The first Ethernet local area network was implemented in Palo Alto, California in 1975 as a joint effort of Stanford University and Xerox Corporation. Since then, Ethernet has been expanding in use and accumulating history. Over the years, it has proven to be reliable and efficient in a wide variety of network applications. As a result, it has become the first industry-standard protocol for local area networks, supported internationally by computer manufacturers in the U.S. and Europe.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document and publish this protocol as an international industry standard. After three years of review and refinement, this specification is about to be published by IEEE Press under the title *IEEE 802.3 CSMA/CD Local Area Network Standard Protocol*, ("CSMA/CD" describes the medium access method, **C**arrier **S**ense, **M**ultiple **A**ccess with **C**ollision **D**etection). The IEEE 802.3 document supersedes all previously published Ethernet specifications.

CSMA/CD — Carrier Sense, Multiple Access with Collision Detection

CSMA/CD: This expression describes the medium access method used in Ethernet alias IEEE 802.3 CSMA/CD. **Carrier Sense** means all nodes on the network can detect all signals transmitted on the network from any source. **Multiple Access** means all nodes can have equal access to the network without need for centralized control. A node is permitted to transmit if the network is not already busy. If, however, two or more nodes start to transmit simultaneously, it is called a collision. **Collision Detection** means that all nodes can detect a collision by monitoring the medium. When a collision occurs, the transmitting nodes resolve which will retransmit first by differential backoff timing.

Data is transmitted in "packets" or "frames" which begin with a preamble for synchronization and end with a CRC field for error detection. In between, the frame has source and destination addresses, a byte-count field and an information field. Total frame length is 72 to 1526 bytes.

The physical signaling format used in Ethernet is baseband Manchester Code transmitted at a rate of 10 million bits per second. In Manchester Code, each bit is encoded by a transition. A "one" is encoded as a low-to-high transition and a "zero" as a high-to-low. In this way there is a continuous supply of bit-framing information for the receiver, since the transmitted signal is never stationary for more than one bit time.

Interface Techniques for 16-Bit Busses

Ethernet is a byte-oriented protocol. That is to say, the smallest unit of data which can be transmitted is a byte. Hence, the 8003 EDLC chip has byte-wide data bus. Whether the System Interface is the FIFO-buffer type or the DMA type, the data transfers to and from the 8003 are byte-wide. This application brief describes some techniques for interfacing this byte-wide communication channel to a 16-bit wide bus.

In designing an Ethernet node, trade-offs have to be made between processing speed and communication speed, cost and performance, flexibility and simplicity, etc. The right balance may be different for each piece of equipment designed, depending on its purpose and system requirements. In order to help you strike the right balance for your design, several interface techniques will be given in the following sections. They are covered in order of increasing cost/complexity/performance.

In an 8-bit system, the 8003 can be interfaced directly to the data bus as shown in Figure 2. The RxTxD0-7 bus is the bus for transferring frame data. It connects to the internal 16-byte transmit and receive FIFOs. The CdSt0-7 bus is a separate input/output port for control and status. It interfaces to the system bus so that the processor has direct access to all command and status bits. In a 16-bit system, CdSt0-7 would connect either to the upper or lower data byte.

Split-Word 16-Bit Data Interface

Refer to Figure 3 for a circuit diagram of this technique. The split-word method splits the 16-bit word into two halves, using one half for transmit data and the other for receive data. In Figure 3, the upper byte of the system data bus is used for the transmit memory buffer and the lower half for receive. Two 74LS244 tristate buffers isolate the system bus lines from the RxTxD0-7 bus of the 8003. The upper 74LS244 is enabled by $\overline{\text{TxACK}}$ from the DMA Controller. $\overline{\text{TxACK}}$ is the DMA Acknowledge signal for the transmit channel. When enabled, this buffer transfers a byte of data from the upper byte of system memory to the 8003's Transmit FIFO. Similarly, the lower 74LS244 transfers data from the 8003's Receive FIFO to the lower byte of system memory. Configured in this way, the transmit and receive buffers in system memory can occupy the same word-address space.

Full-Word 16-Bit Interface Using Byte-Wide Memory Transfers

Another type of 16-bit interface is one that assembles and disassembles words by transferring the upper byte and the lower byte separately. For example, suppose the convention is chosen that the upper byte is to be the first of the two bytes to be transmitted and the lower byte the second. Then the first byte of a frame and all odd-numbered bytes are always transferred to/from the upper byte of memory, and the second and all even-numbered bytes to/from the lower.

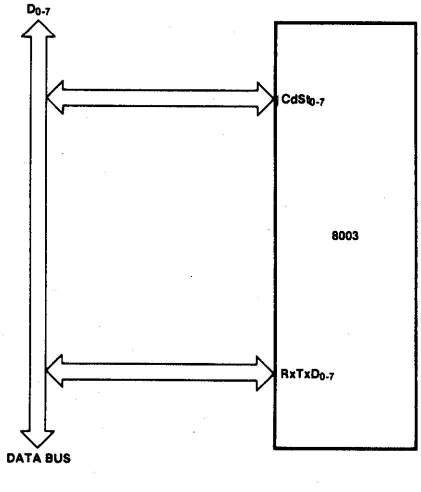


Figure 2. 8-Bit DMA Data Interface

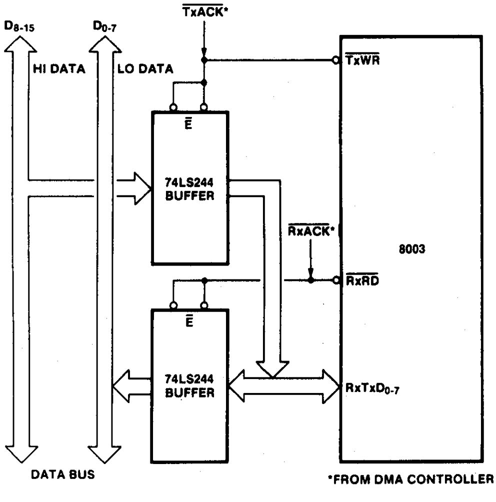


Figure 3. Split-Word 16-Bit DMA Data Interface

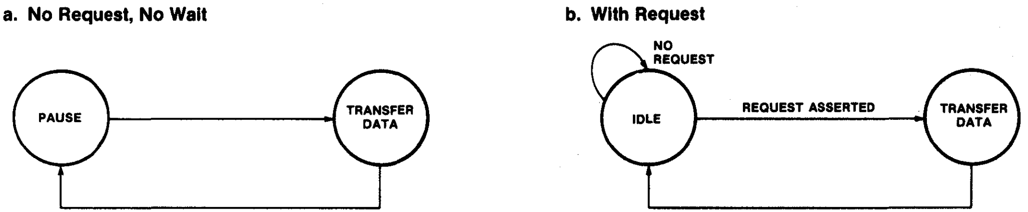
The data interface for this approach is a variation of the one shown in Figure 3. Two tristate buffers are replaced by two bi-directional transceivers. A0, the least-significant bit of the DMA Controller's address is decoded with $\overline{\text{TxACK}}$ and $\overline{\text{RxACK}}$ to enable the transceivers. The more significant address bits from the DMA Controller, A1 through A_N, are used as the memory address. Upper and lower memory strobes are also controlled by A0. Refer to Table 1 for the truth table.

This is the simpler and more economical of two "Full-Word" data interfaces described in this application brief. The other one, shown in Figure 5, assembles and disassembles words in registers, and transfers 16 bits at a time. The advantage of the latter approach is in saving bus bandwidth, since it uses half as many bus cycles to transfer the same amount of data; but there is some additional cost in hardware.

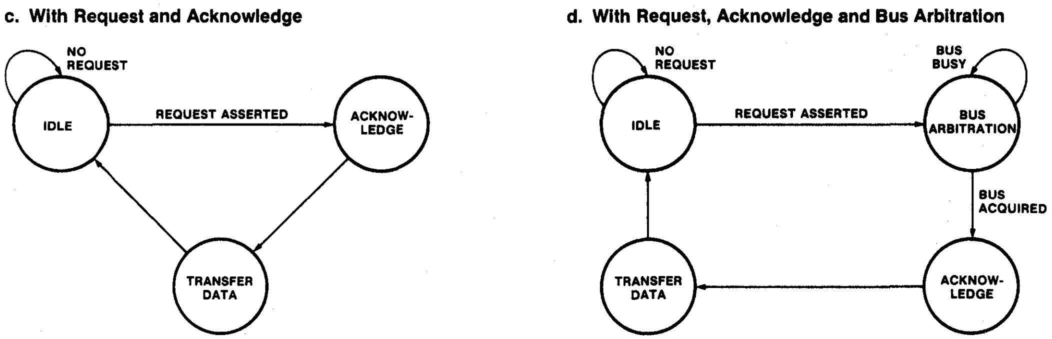
Table 1. A0 Address Decoding for Full-Word 16-Bit Interface Using Byte-wide Memory Transfers

DMA Controller Outputs			Transceiver Enabled Toward (Memory; I/O)		Memory Activity	
A0	$\overline{\text{TxACK}}$	$\overline{\text{RxACK}}$	Upper	Lower	Upper	Lower
—	1	1	—	—	—	—
0	0	1	I/O	—	Read	—
1	0	1	—	I/O	—	Read
0	1	0	Memory	—	Write	—
1	1	0	—	Memory	—	Write

Note: — indicates not active.


a. No Request, No Wait

b. With Request


c. With Request and Acknowledge

d. With Request, Acknowledge and Bus Arbitration

Figure 4. Data Transfer State Diagrams — Four Types

Four types of data transfers are shown in Figure 4. The first, labeled a, is an unconditional transfer sequence such as the type that would be used to refresh a CRT screen. This type has no use in an Ethernet interface since it is not controlled by availability of storage space or stored data.

The diagram in Figure 4 Part b, illustrates a transfer which is initiated "on demand". The transfer takes place only when a "request" is given. An example of this type is data moved by a processor on its own synchronous bus. Physically the request is generated by the processor, manifesting itself as a set of bus-controls, and an address.

Part c illustrates a transfer that is requested by one entity and acknowledged by another. The acknowledge signal is used to notify the requesting entity that the transfer is about to take place. This implementation provides the requesting entity verification that the transfer is taking place. The diagram represents the response of the acknowledging party to the request. The requesting party normally waits for the acknowledgement to occur. This allows the acknowledging party to delay, if necessary, for data access. This mechanism is used on asynchronous busses, like that of the 68000 microprocessor.

The diagram in Part d is that of a transfer with request, acknowledge, and bus arbitration. This implementation is one that is used to transfer information using a DMA controller on the main system bus. There are actually two request/acknowledgement sequences in this transfer, one for bus acquisition and one to transfer information on the acquired bus. Initially a request generated by one of the two "transferees" queues the DMA controller to exit its idle state, and arbitrate for the system bus by generating a "bus request" signal. When the bus master relinquishes the bus, a "bus grant" acknowledgement is received, notifying the DMA controller that it now owns the bus. The DMA controller then performs the transfer, or transfers, by generating a "DMA Acknowledge" to the original requesting device, and generating the appropriate addresses and read/write control signals. Finally the sequence is terminated with control of the bus returning to the main processor through another arbitration.

Diagrams like these can be used to design state machine programs for interfaces like the one in Figure 5, which employs a single-chip state machine.

Helpful Hints for State Machine Designers

As with writing a program, it is desirable to start with a "flow chart" or "state diagram". Examples of state diagrams can be seen in Figure 4. The following are the definitions used in the circle-and-arrow state diagrams used here.

1. Each circle represents a single physical machine state or an unconditional sequence of machine states such that there are no "hidden branches" omitted from the diagram.
2. All conditional branches, and wait states (which may be viewed as conditional branches) are indicated explicitly by arrows. Each arrow is labeled with the condition which determines the branch.

Following these or similar guidelines will help to avoid unforseen anomalies in the operating flow.

Care should be taken in defining the programs for state machines when inputs are asynchronous with respect to the state-register clock. Problems can result when making a conditional branch based on an asynchronous input. Such problems can cause intermittent branching failures with possibilities of perverse consequences. Intermittency makes this type of problem hard to diagnose, so it pays off to avoid them by following these design rules:

1. When a branch is conditional on an asynchronous input bit, assign next-state addresses such that only one state-register flip-flop is affected by the asynchronous bit.
2. For a 3 or more-way conditional branch based on more than one independent asynchronous bit, break it down into independent 2-way branches which conform to rule 1.
3. For inputs which are mutually-dependent combinations of 2 or more bits, it is best to synchronize them with an input register whose clock is synchronized to the state-register clock.

When you have finished the state diagram, you have defined the operating program design. The next step is to choose the hardware that can run your program most efficiently.

After choosing the hardware, you can translate the state diagram, verbatim into program code for the state machine.

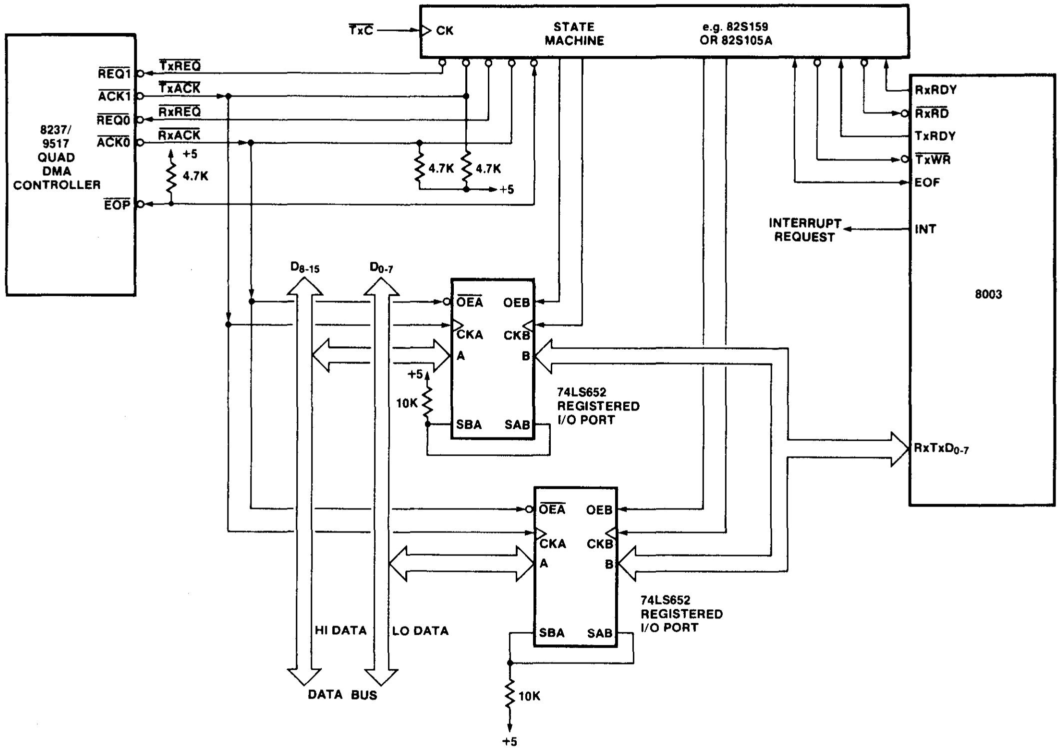


Figure 5. 16-Bit Full-Word DMA Data Interface with 8237/9517 Using Registered I/O Ports

Full-Word 16-Bit Interface Using Registered I/O Ports

This data interface method assembles/disassembles 16-bit words in a pair of 8-bit registered I/O ports. The data transfers between the memory and the I/O ports are 16 bits wide. Transfers between the ports and the 8003 EDLC chip are byte-wide.

Registered I/O ports are configured by taking two 8-bit D-type registers with tri-state outputs and connecting them front-to-back. The result is two 8-bit bus connections, each connected to the D inputs of one register and the tri-state outputs of the other. The port has two register clocks and two output-enable controls. An example of such a chip is the 74LS652. The more popular 8-bit registered I/O port chips on the market are in the 0.3 inch 24-pin package.

This interface technique can be used with some variation for any of the three basic types of system interface, i.e. 1. with FIFO frame buffers, 2. with DMA to off-line frame buffers or 3. with DMA to system memory.

A state machine is used to sequence the assembly and disassembly processes. Programmable single-chip state machines and logic blocks, available from multiple sources, are excellent for this type of design. Most are field-programmable one time by burning fuseable links. Normally, the state machine portion of the design can be done in one or two chips.

A circuit example with the 8237/9517 DMA Controller appears in Figure 5. A single-chip state machine, such as the Signetics 82S159 or 82S105A, coordinates the timing for all other components. Two 74LS652s are the two registered I/O ports. The bus lines on the right side of the ports are commoned to make an 8-bit connection to the RxTxD0-7 pins of the 8003. On the left, the 16 port lines connect to the data bus.

Most of the command signals associated with data transfer are sequenced by the state machine. DMA requests ($\overline{\text{REQ0}}$ and $\overline{\text{REQ1}}$), port output-enable line

OEB, register clock CKB, Transmit FIFO write ($\overline{TxWR}$) and Receive FIFO read ($\overline{RxRD}$) are all under state machine control. Output-enable $\overline{OEA}$ and register clock CKA are controlled by the DMA Acknowledge lines. All the status lines for data transfer connect to the state machine's inputs.

Figures 6 and 7 summarize the state-machine state diagrams for the application in Figure 5. Refer to Figure 6 for the word disassembly diagram. The disassembly process starts with a DMA request issued to the DMA's transmit channel. If the channel is not enabled, no acknowledge will be given and the state machine will remain in the DMA Request State. If the channel is enabled, the DMA Controller will request and acquire the system bus, then issue the DMA Acknowledge. A 16-bit word of data is then read from system memory into the two ports. The next state is Idle 1. Here the state machine waits for a TxRDY ready signal from the 8003 if not already present. When TxRDY is high, the machine goes to the Read First Byte State. This state moves the upper data byte from the upper port into the Transmit FIFO of the 8003. Another idle state occurs where TxRDY is checked for Transmit FIFO readiness. When ready, the lower data byte from the lower port is moved to the Transmit FIFO, ending the cycle.

Refer to Figure 7 for the word assembly state diagram. Word assembly starts in the Idle 1 State. Here, the state machine waits for a signal from the Receive FIFO (RxRDY pin) indicating data is present. When RxRDY is high, the machine advances to load the first byte of the word being assembled to the upper port. As the data is read out of the FIFO, the 8003's EOF line is tested to determine if it is the last byte of the frame. If it is, reading of the second byte is skipped. If not, the Idle 2 State is entered. When ready, the second byte will be loaded into the lower port. Then a DMA Request is given. The DMA Controller will then request the bus, acquire it and give the DMA Acknowledge. Then the state machine passes through the Transfer State, writing the 16-bit word to system memory. That ends the word assembly cycle.

Further References Available from SEEQ

8023A MCC Data Sheet

8003 EDLC Data Sheet

Application Note 3: Manchester Encoding and Decoding for Local Area Networks

Application Brief 6: DMA Interconnection to the 8003 EDLC™

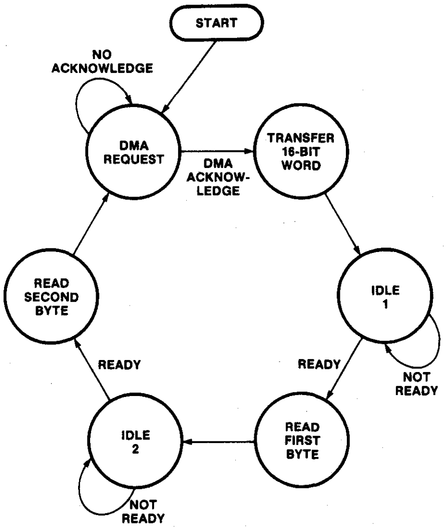


Figure 6. State Diagram for 16-Bit Word Disassembly

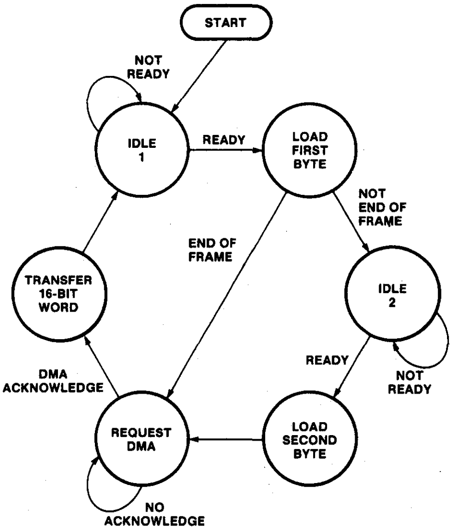


Figure 7. State Diagram for 16-Bit Word Assembly

Communications Products
Application Brief

6

DMA INTERCONNECTION TO THE 8003 EDLC®

March 1985

APP. NOTES

seeq
Technology, Incorporated

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DMA Interconnection to the 8003 EDLC

Introduction

SEEQ's 8003 Ethernet-compatible data link controller provides an economical communication interface for terminals, personal computers, workstations, printers, disk drives and host computers. The 8003 is a 40-pin VLSI device which can replace approximately 60 MSI and SSI components in a typical Ethernet node configuration.

This application brief is about design techniques for an Ethernet node when direct-memory access (DMA) is chosen as the means of transferring data between the system bus and the channel. The methods described herein can be applied to virtually any computer or system bus architecture.

Ethernet local area networks use the **broadcast** network topology. That is to say, a signal transmitted by any station reaches all other nodes on the network. This is in contrast to other types of networks, such as the "star" and the "ring", which use point-to-point interconnections. Transmitted messages in Ethernet are "broadcast" on a segment of 50Ω coaxial cable. Communication nodes are attached to this cable via passive taps, so that new nodes can be added at any time without interrupting the network service. Nodes on the network can be addressed individually, in "multicast" groups, or by the "broadcast mode" to all nodes simultaneously. The broadcast topology is a very efficient mode of communication, yet it is simple and inexpensive to implement.

Ethernet alias IEEE 802.3 CSMA/CD

The first Ethernet local area network was implemented in Palo Alto, California in 1975 as a joint effort of Stanford University and Xerox Corp. Since then, Ethernet has been expanding in use and accumulating history. Over the years, it has proven to be reliable and efficient in a wide variety of network applications. As a result, it has become the first industry-standard protocol for local area networks, supported internationally by computer manufacturers in the U.S. and Europe.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document and publish this protocol as an international industry-standard. After three years of review and refinement, this specification is about to be published by IEEE Press under the title *IEEE 802.3 CSMA/CD Local Area Network Standard Protocol.* ("CSMA/CD" describes the medium access method, **C**arrier **S**ense, **M**ultiple **A**ccess with **C**ollision **D**etection.) The IEEE 802.3 document supersedes all previously published Ethernet specifications.

CSMA/CD — Carrier Sense, Multiple Access with Collision Detection

CSMA/CD: This expression describes the medium access method used in Ethernet alias IEEE 802.3 CSMA/CD. **Carrier Sense** means all nodes on the network can detect all signals transmitted on the network from any source. **Multiple Access** means all nodes can have equal access to the network without need for centralized control. A node is permitted to transmit if the network is not already busy. If, however, two or more nodes start to transmit simultaneously, it is called a collision. **Collision Detection** means that all nodes can detect a collision by monitoring the medium. When a collision occurs, the transmitting nodes resolve which will retransmit first by differential backoff timing.

Data is transmitted in "packets" or "frames" which begin with a preamble for synchronization and end with a CRC field for error detection. In between, the frame has source and destination addresses, a byte-count field and an information field. Total frame length is 72 to 1526 bytes.

The physical signaling format used in Ethernet is baseband Manchester Code transmitted at a rate of 10 million bits per second. In Manchester Code, each bit is encoded by a transition. A "one" is encoded as a low-to-high transition and a "zero" as a high-to-low. In this way there is a continuous supply of bit-framing information for the receiver, since the transmitted signal is never stationary for more than one bit time.

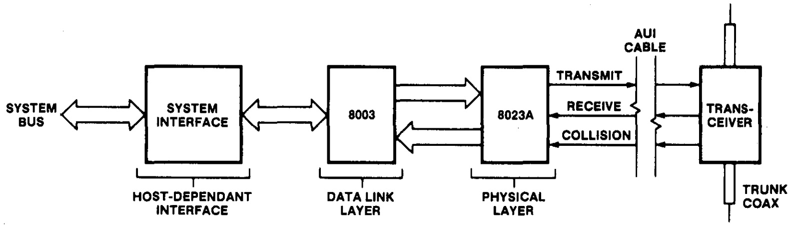

Figure 1. Ethernet Node Configuration

Figure 1 shows a typical CSMA/CD node configuration. The System Interface connects the host system bus to the network. This interface varies depending on processor and system requirements.

Data Link functions are performed by SEEQ's 8003 EDLC Ethernet Data Link Controller chip. This device performs medium access control, frame formatting and error detection.

The Physical Layer functions, carrier sense, collision signal detection, data signal encoding and decoding are performed by SEEQ's 8023A MCC™ Manchester Code Converter chip. Manchester Code is the physical signaling format used on the network. Data is transmitted on the network at a rate of 10 million bits per second.

The Data Terminal Equipment hardware, consisting of the System Interface, the 8003 EDLC chip and the 8023A MCC chip, is connected to the Transceiver by the Access Unit Interface (AUI) cable. This cable consists 78Ω balanced, shielded twisted-pair connections, DC biased at the Data Terminal end and transformer-coupled at the Transceiver end.

Besides the passive tap to the Trunk Coax, the Transceiver provides signal amplification, preconditioning on the receive path, impedance matching, DC isolation, collision detection and collision signaling generation. DC power for the Transceiver circuits is provided through the cable.

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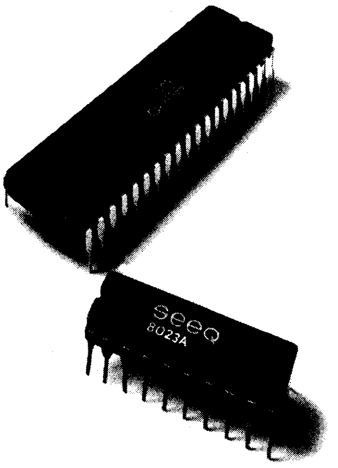

Figure 2. SEEQ's Ethernet Chip Family: 8003 EDLC Ethernet Data Link Controller, 8023A MCC Manchester Code Converter

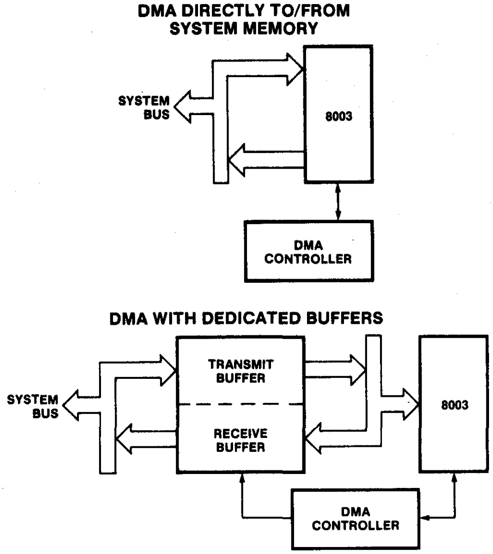

Figure 3. DMA System Interface Techniques

Direct Memory Access System Interface

There are two basic methods for interfacing the CSMA/CD channel to the system bus using DMA, illustrated in Figure 2. The first method uses DMA to transfer data directly between the Ethernet Data Link Controller and the system memory. In the second method, a temporary buffer memory intervenes between the system memory and the EDLC chip. The intervening buffer relieves the system bus of some of the traffic and timing requirements associated with the channel. These two methods will be the subject of the following sections.

DMA Design Considerations for Ethernet

In designing an Ethernet node, some trade-offs have to be made between processing speed and communication speed, cost and performance, flexibility and simplicity, etc. The right balance can be different for each piece of equipment designed, depending on its purpose and system requirements. In order to help you evaluate the trade-offs for your design, this section discusses some of the key parameters for you to consider at the outset.

Time is Data

Since the data transmission rate for Ethernet is 10 million bits per second, data transfers during active periods will have to keep up. That means data has to be moved at 1.25 million bytes per second to/from the communication channel. The DMA Controller must meet this speed requirement or frames will be lost. If the system is to support loopback diagnostics, both transmit and receive DMA channels will have to operate simultaneously, together transferring 2.5 million bytes per second. Not just any DMA Controller will do.

Bus Bandwidth

This is only a consideration for systems with heavy communications traffic and/or critical response timing. The transfer of data on the system bus can sometimes use up a considerable percentage of the bus time, at least for short bursts. If this is a problem, the method with dedication buffer memory can be used to offload the system bus (see Figure 2 bottom).

With or Without Dedicated Buffer Memory

If the system architecture does not support 1.25M Bytes/s DMA, the dedicated buffer approach can solve the timing problem. If the system architecture does support high-speed DMA, then bus bandwidth is the key factor which influences this decision. In this case it is clearly a cost-performance issue. The dedicated buffer can relieve system bus traffic, but it takes more hardware to implement.

Cycle-steal or Burst Mode DMA

Refer to Figures 3 and 4. In the Cycle-steal DMA Mode, the DMA Controller "steals" a bus cycle to transfer one and only one byte or word of data. In the Burst DMA Mode, each time the DMA Controller acquires the bus, it can transfer several bytes or all the data to fill or empty a buffer. Either of these two modes can work for Ethernet in principle if the transfer speed is adequate. The Burst Mode is usually preferred by reason of timing efficiency. In Burst Mode, bus arbitration and change-over delays are kept to a minimum. Also, Burst Mode allows the DMA Controller to fill or empty a buffer in one DMA cycle.

On Demand

Transfers between memory and the communication circuitry must be done *on demand*. Some DMA Controller chips will only transfer blocks of data in predetermined lengths. This will not work since the processor and DMA Controller cannot know in advance how many bytes of data can be transferred at a given time.

Maximum Bus Grant Latency

The time it takes to get the bus after a request is made is called bus grant latency. If the DMA method without buffer memory is used, each time a DMA transfer to/from the 8003 EDLC chip begins, the DMA Controller must arbitrate for and acquire the system bus. If the latency is too long, the transmitter may underflow or the receiver overflow. The 8003 has transmit and receive FIFOs which are 16 bytes deep, so it must transfer data at least once every 12.8 microseconds when active (16 x 800 nanoseconds). Maximum bus grant latency should be deterministic and always less than that required to prevent underflow and overflow.

8003/DMA Node Hardware

The 8003 has an 8-bit bi-directional data bus (RxTxD_{0-7}) for data transfers to and from its internal FIFOs. In Figure 6, the node hardware is configured to transfer data directly to/from system memory over this bus. (This is the technique referred to previously in Figure 3 at the top.) A two-channel DMA Controller is used, providing one channel for transmit data and one for receive data.

A transfer to the transmitter of the 8003 begins with a DMA Request given by the 8003 (its TxRDY pin goes high). The DMA Controller then issues a Bus Request to the processor. After completing the current cycle, the processor halts and gives a bus grant to the DMA Controller, which then transfers the data by issuing a DMA Acknowledge and all necessary address and control signals. Additional transfers would take place if Burst Mode is used until the Transmit FIFO is full, indicated by the TxRDY pin going low. Then the bus is released to the processor and the DMA cycle is over.

Data transfer from the Receive FIFO happens in the same way but with data flowing in the opposite direction. It starts with a DMA Request from the 8003 (its RxRDY pin goes high). If Burst Mode is used, the DMA will continue to transfer until the Receive FIFO is empty, indicated by a low on the RxRDY pin.

The Data Interface for a DMA node with buffer memory appears in Figure 6. In this case, a 4-channel DMA Controller is used. Two channels are needed as before to transfer data between the 8003 and memory. These two channels operate "off-line" and do not require bus arbitration. The other two transfer data between the buffer memory and the system bus. They do require the usual bus arbitration.

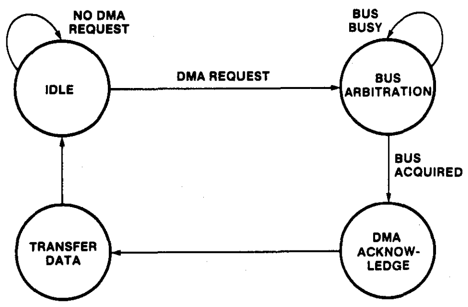

Figure 4. DMA Cycle-steal Mode State Diagram

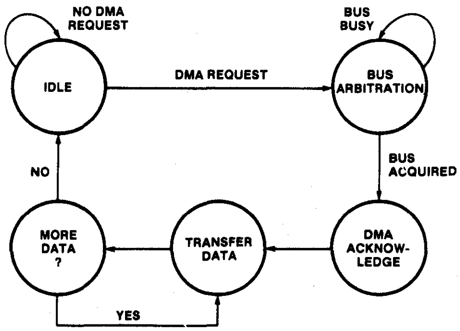

Figure 5. DMA Burst Mode State Diagram

For this design, the RxTxD$_{0-7}$ Receive/Transmit Data Bus of the 8003 connects to a separate bus which is isolated from the system bus by a transceiver. This bus gives the 8003 immediate access to the buffer memory without the need for arbitration.

The two channels for memory-to-memory transfer use the usual bus arbitration method to access the system bus. For these two channels, data being transferred passes through the transceiver shown in the top center of the figure. The tri-state buffer appearing at the bottom center passes the address from the DMA Controller to the System Memory during the transfer. The tri-state buffer and transceiver are enabled by the DMA Controller at the appropriate time in its cycle.

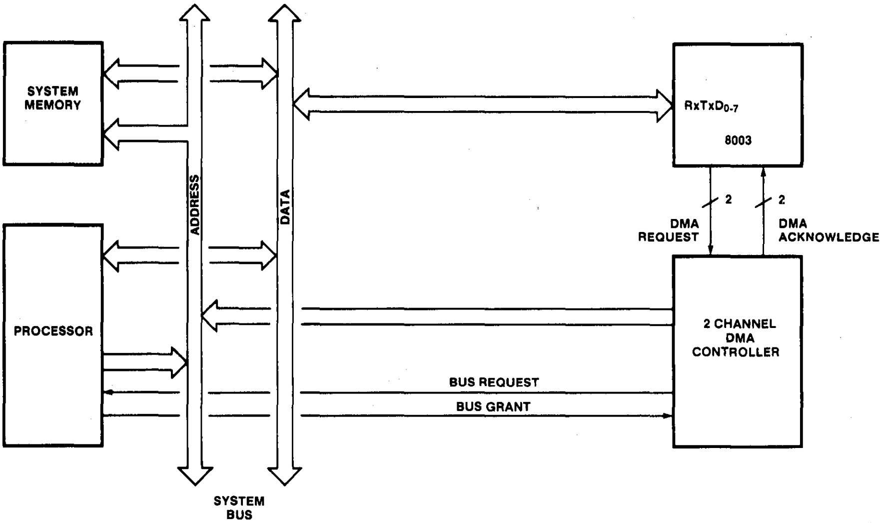

Figure 6. Data Interface for DMA Directly to/from System Memory

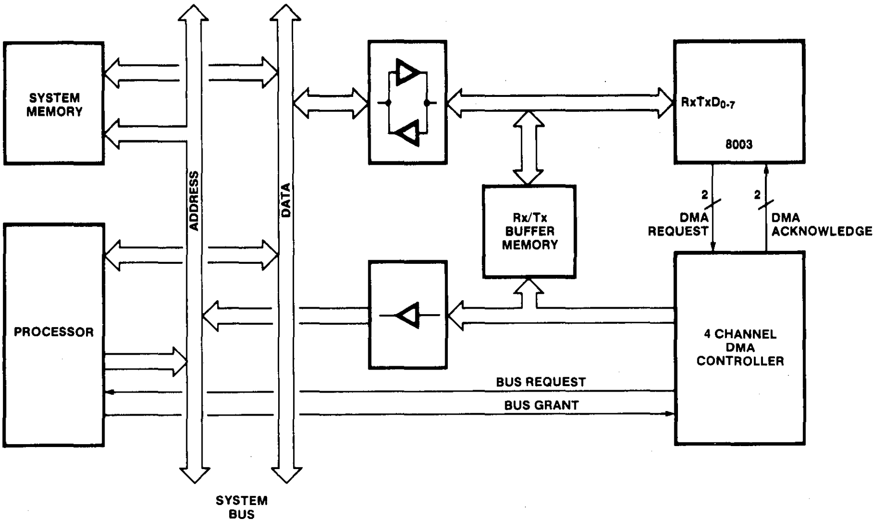

Figure 7. Data Interface for DMA with Buffer Memory

Command Status Interface

The Command/Status Interface for the 8003 is shown in Figure 8. The 8003 has a separate bidirectional 8-bit bus for accessing its internal command and status registers. This bus is labeled "CdSt0-7" in the figure. Three address lines, A_0, A_1 and A_2 select the register to be accessed. Refer to the 8003 data sheet for a full description of these registers and their addresses.

To write to a command register, the system bus decoder must provide a low level to both Chip Select ($\overline{\text{CS}}$) and Write ($\overline{\text{WR}}$) while data and the three address bits are valid. To read a status register, a low is applied to both Chip Select and Read ($\overline{\text{RD}}$) while the address is valid.

The Interrupt Request line (INT) goes high to request an interrupt when specific conditions occur. This line drives the interrupt input of the processor, either directly or through an interrupt-priority logic block. Conditions for generating an interrupt are selected by setting bits in the command registers. For details, see the data sheet. The Interrupt Request line is cleared automatically when the processor reads the status registers.

8237/9517 DMA Controller Interface

The interconnection of popular the 8237/9517 DMA Controller to the 8003 is illustrated in Figure 8. The TxRDY control line from the 8003, which indicates that the Transmit FIFO is not full, is used to generate the DMA request for Channel 1, the transmit channel. Similarly, RxRDY which indicates that the Receive FIFO is not empty generates a request for Channel 0, the receive channel. After a request for Channel 1, the DMA Controller will issue simultaneously a DMA acknowledge (on DACK1) and an input/output write ($\overline{\text{IOW}}$), which are used to assert the $\overline{\text{TxWR}}$ write line on the 8003. After a request for Channel 0, the DMA Controller will issue simultaneously a DMA acknowledge on DACK0 and an input/output read ($\overline{\text{IOR}}$). These are used to assert the $\overline{\text{RxRD}}$ read line on the 8003.

The $\overline{\text{EOP}}$ control line on the 8237/9517 indicates the "end of process" which has the same meaning as the 8003's "end of frame" line (EOF). These lines are used to terminate the transfer process after the last byte of a frame has been transferred. Both the $\overline{\text{EOP}}$ and EOF lines are bi-directional, the direction depending on the direction of data transfer. They are interfaced together by an inverting transceiver, whose direction of operation is controlled by the DACK0 and DACK1 acknowledge lines.

The active polarities of the DREQ and DACK lines on the 8237/9517 are programmable by setting internal control bits. For the interface shown, they should be programmed active high.

68440/68450 DMA Controller Interface

The 8003 interface to the 68440/68450 DMA Controllers from the popular 68000 microcomputer family is shown in Figure 9. The request lines on the 68440/68450 can be programmed to be level or edge sensitive. In this example, level sensitivity is selected by setting internal control bits. As in the previous example of Figure 9, the TxRDY output of the 8003 drives the request line for Channel 1 and the RxRDY requests Channel 0.

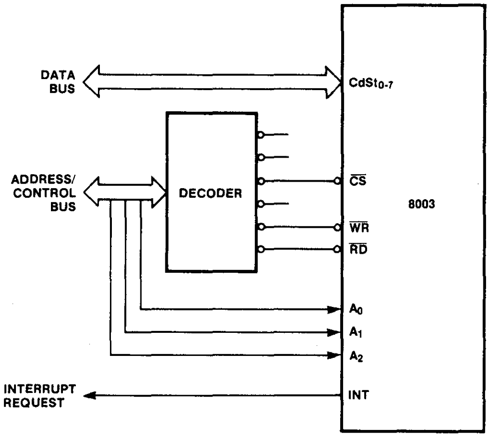

Figure 8. Control/Status Interface

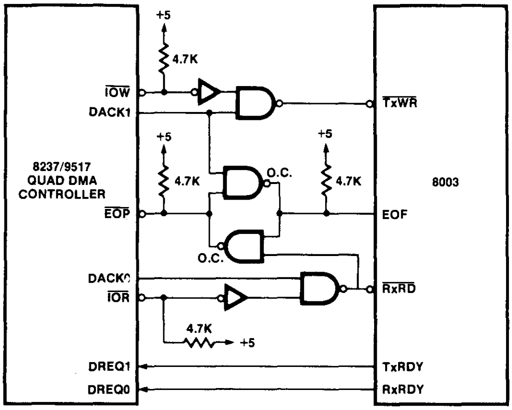

Figure 9. 8003 Interface to 8237/9517 DMA Controller

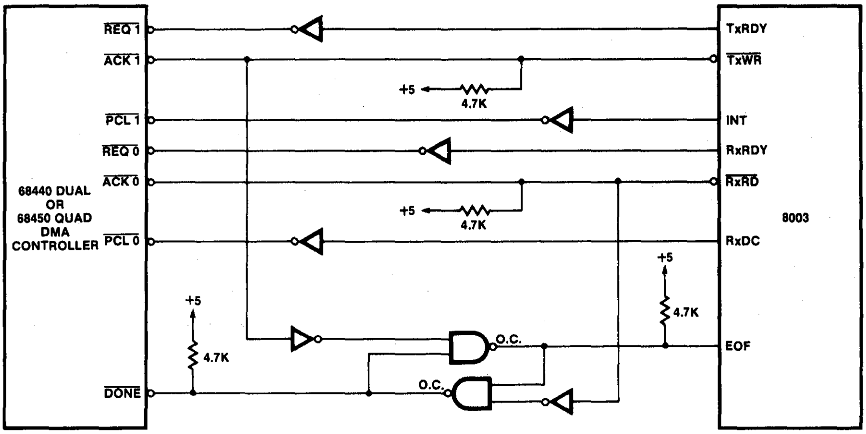

Figure 10. 8003 Interface to 68440/68450 DMA Controller

The acknowledge lines on the 68440/68450 can be connected directly to the TxWR and RxRD inputs of the 8003 as shown in Figure 9.

On the 68440/68450, the EOF function pin is called "done". The $\overline{\text{DONE}}$ pin interfaces to the 8003's EOF pin through an inverting bi-directional transceiver shown at bottom center of the drawing. As in the previous example, this signal terminates the channel activity at the end of the frame.

The $\overline{\text{PCL0}}$ and $\overline{\text{PCL1}}$ lines on the DMA Controller are put to good use in this application. They are programmable inputs associated with Channel 0 and Channel 1 respectively. By setting internal control bits, the $\overline{\text{PCL1}}$ line can be programmed to activate the on-chip interrupt request logic. The interrupt request output of the 8003 (INT) is used to drive it. A low on $\overline{\text{PCL1}}$ will interrupt the processor to read the status registers of the 8003. This is used for a variety of conditions which can occur on the network. For example, if 16 consecutive collisions occur, network diagnostics and/or an alarm are ordered by interrupting the processor. The status code which has generated the interrupt is read by the processor from the 8003's internal status registers.

The $\overline{\text{PCL0}}$ input can be programmed to be an input for restarting Channel 0, the receive channel. In this mode, a low on $\overline{\text{PCL0}}$ will re-initialize the channel automatically. It is driven by the 8003's RxDC receive discard line. RxDC goes high following reception of a bad frame or frame fragment. This will in effect discard the bad data and restart the receive channel, without the need for processor intervention in setting up the channel.

Communication Products Application Note

7

8005 ADVANCED EDLC® USER'S GUIDE

September 1987

APP. NOTES

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Technology, Incorporated

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8005
Advanced EDLC
User's Guide

Introduction

Ethernet was developed by the Palo Alto Research Center (PARC) of the Xerox Corporation. The first network was implemented in 1975, as a result of a joint effort by Stanford University and PARC. Over the years, it was proven to be reliable and efficient in a wide variety of network applications. As a result of that success, it became the first industry standard protocol for LANs, supported internationally by computer manufacturers in the United States and Europe.

The network allows equal access by all nodes, can support upwards of 1000 nodes, and can operate with a coaxial cable length in excess of 500 meters. Ethernet is easy to realize, due in large part to currently available LSI chips which implement it.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document, and publish this protocol as an international industry standard. After three years of review and refinement, this specification has been published by the IEEE press under the title, "ANSI/IEEE 802. 3-1985 CSMA/CD Local Area Network Standard Protocol". The medium access method is described by the abbreviation CSMA/CD, or Carrier Sense, Multiple Access with Collision Detection.

CSMA/CD: Carrier Sense, Multiple Access with Collision Detection

Carrier Sense

All nodes on the network can detect all signals transmitted from any source. A node is any connection to the coaxial cable via transceiver, shown in Figure 1. The transceiver makes a connection to the cable via connectors or has barbs to pierce the cable and establish an electrical connection when a screw or bolt is tightened. The transceiver provides collision detection, electrical isolation and voltage level translation between the system at the node and the cable carrying data.

Multiple Access

All nodes have equal access to the network. There is no priority assigned to any node. Also, there is no central control, nor is there any token passing. Any given node may transmit if the network is not already busy. If two or more nodes transmit at the same time, a collision occurs.

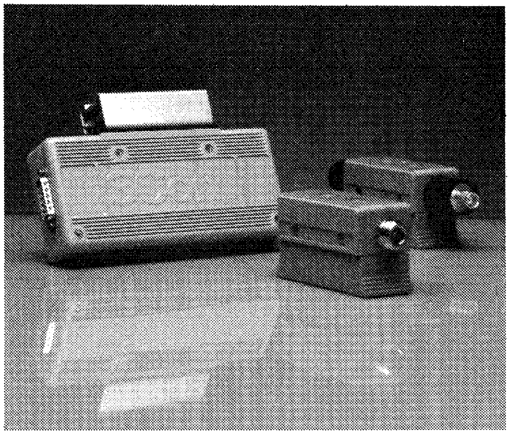


Figure 1.

Collision Detection

All nodes can detect a collision by monitoring the medium. When a collision occurs, the transmitting nodes jointly decide which node will retransmit first by a technique known as truncated binary exponential backoff, which provides for a random timeout at each node before each retransmit attempt.

Ethernet Data Format

Data is formatted and transmitted in "packets" or "frames", as shown in Figure 2. These frames begin with a preamble for synchronization, and end with a CRC field for error detection. In between, the frame has destination and source addresses, a byte count field, and a data field. This data field contains from 46 to 1500 bytes of information which is passed to a higher layer of software for processing. It is transparent to the media access layer of Ethernet, and may contain any arbitrary sequence of bytes.

Total frame length is 72 to 1526 bytes, including preamble (8 bytes), and frame check sequence (4 bytes).

The signaling method used in Ethernet is baseband Manchester code, transmitted at 10 Megabits per second. Manchester code is such that each bit is defined by a transition at its mid-bit point: a ONE is encoded as a high going signal and a ZERO is a low going signal. Thus, the data is said to be self clocked. This technique provides a continuous supply of bit framing information for the receiver, since the transmitted signal is never static for more than one bit time.

Addressing Scheme

An Ethernet address contains six bytes to define a station address. This allows for over 140 trillion unique addresses. The 48th bit in the address is reserved to indicate a broadcast or multicast address. Xerox Corporation controls issuing addresses for Ethernet. As a system manufacturer, you receive your block of addresses when you receive a license. It is necessary to assign a unique address for each product that communicates on Ethernet.

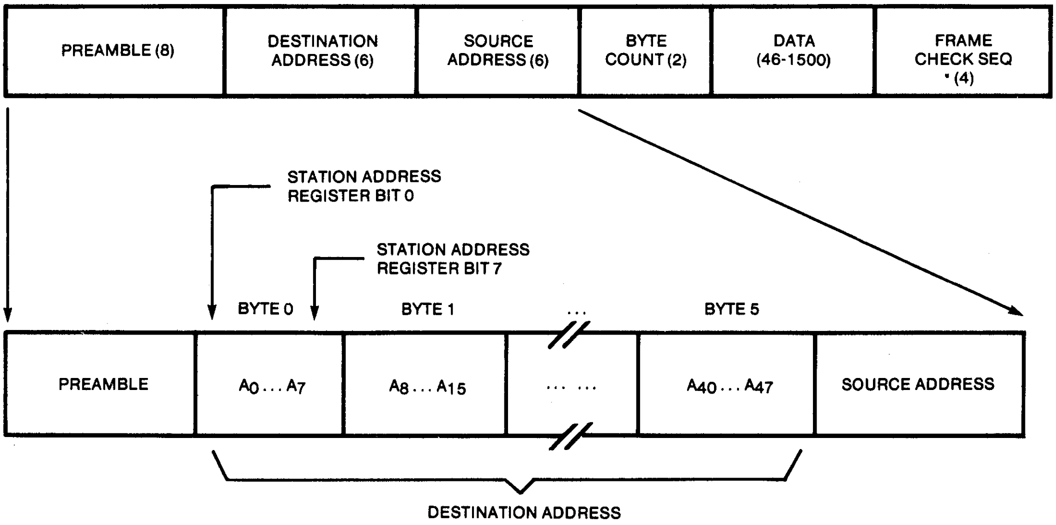


Figure 2. Ethernet frame format. Numbers in parentheses indicate the length of each field. Bits within a byte are transmitted and received LSB first and MSB last.

Direct Memory Access System Interface

There are two basic DMA techniques for interfacing the network to the system bus. The first, in Figure 3a, uses DMA to transfer data directly between the Ethernet controller and the system memory. In Figure 3b, a temporary buffer memory intervenes between the system memory and the controller chip. This buffer eliminates the need to service LAN traffic in real-time.

Why a Local Buffer?

Consider the first approach, where no local buffer is used at the node. Since the LAN data rate is 10 Megabits per second, the DMA controller must be capable of handling system data at a minimum of 1.25 Megabytes per second. If the controller cannot operate at this rate continuously, LAN data will be lost. Additionally, if the system is to support loopback diagnostics, both transmit and receive must operate simultaneously, together transferring 2.5 Megabytes per second. Clearly, a garden variety DMA controller will not get the job done. Particular attention must be paid to how long it takes the controller to acquire the system bus. If too long, Ethernet data will be lost.

Collision Effects

Collisions normally occur during transmission of the first 64 bytes of data. If packets are retrieved via DMA from system memory, when a collision occurs these 64 bytes must be retransmitted. This is an inefficient use of bus bandwidth.

An Ethernet Controller is a True Asynchronous Peripheral

Prudent system design calls for buffering any peripherals which are asynchronous in nature. Buffering makes the resource much more manageable at the system level.

Implementing a Local Buffer

Most currently available Ethernet controllers have a modest buffer built in, usually on the order of 16 bytes. This is sometimes adequate to handle system bus acquisition delay, but it does not make efficient use of bus bandwidth in three important areas:

1. Collisions during transmit. As network traffic increases, the probability of a collision increases. Each time a collision occurs the Ethernet controller must retransmit from the beginning of the packet. The time spent retransmitting due to collision uses bus bandwidth unnecessarily.

2. Frame check sequence (CRC) errors after receive. Since errors are not detected until after a packet has been received, bus bandwidth will be wasted when receiving packets with errors.

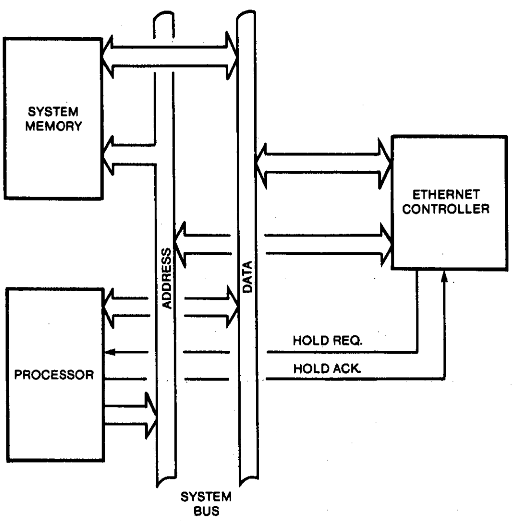


Figure 3a.

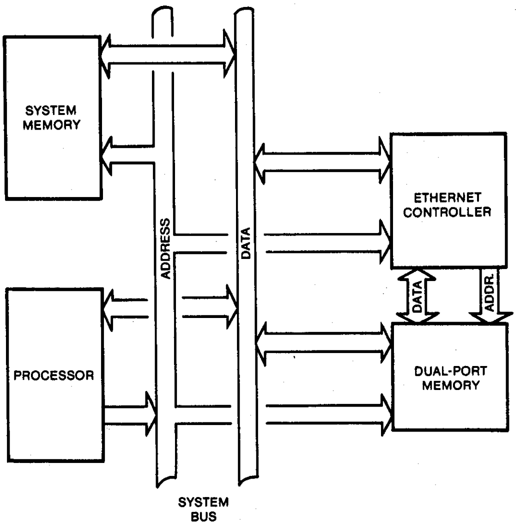


Figure 3b.

3. A significant number of receive packets are minimum size (64 bytes) yet contain much less than 64 bytes of information. For example, packet acknowledgments contain less than 20 bytes of information and are padded to the 64 byte minimum required. Transfer of these pad bytes over the system bus cannot be avoided without some large local buffer.

Supplementing the Controller Buffer

RAM can be added to the Ethernet board to add to the modest buffer already on the controller chip. Figures 4a and 4b show two possible ways.

The buffer should be at least 1514 bytes long. Static RAMs were chosen in Figure 4a to avoid having to include refresh control circuits in the dual port memory control logic.

The memory control must regulate access to the buffer by two buses: the system bus, and the data bus from the controller. The SRAMs are costly.

If DRAMs are used as in Figure 4b the cost is lower but they do require refresh circuitry in the memory controller.

Local Buffering with the 8005

The 8005 Advanced Ethernet Data Link Controller combines several unique approaches to the problem of implementing an Ethernet connection. Look at the design in Figure 5.

First consider the local buffer: the 8005 is designed to work with 64K x 4 DRAMs which are readily available, and inexpensive. It has on board refresh circuitry, and just two DRAM chips provide 64 Kbytes of local buffer storage.

The 8005 treats the DRAM in a unique fashion: it multiplexes both address and data over eight lines. This saves on circuit board traces: only 12 lines are required to interface with the DRAMs, compared with 26 lines if static RAMs are used.

The 8005 also directly supports an address (EE) PROM, which allows for storage of the 8005's Ethernet address and configuration data.

The 8005 supports six unique station addresses. Thus, one physical connection on the Ethernet suffices for six logical connections. You could make effective use of this feature by, for example, connecting six devices to one Ethernet node, and controlling access to each device.

Figure 6 illustrates a cluster controller which services three printers and three PCs or terminals, and provides access to the Ethernet for the devices.

The printer controller services the cluster of three printers, and a low cost, low speed LAN provides coverage for the PCs. This LAN coverage may represent a relatively small geographic area, like a single corporate department. Note, however, that each device has access to the Ethernet, and each has a specific Ethernet address.

Design Examples

In this section, we'll briefly examine the way in which the 8005 can put two popular microprocessor bus formats on Ethernet, by way of using the Intel and the Motorola bus modes built into the 8005. Then we'll look in detail at a intelligent Ethernet controller which could realistically reside on a PC board, and usurp a minimal amount of resources from the system in which it is installed.

The Intel Mode

Figure 7 shows an implementation of the 8005 in an environment using an Intel processor. Note that BUSMODE is pulled up, indicating that the 8005 will produce Intel-compatible output signals, and accept inputs from an Intel bus. Also, in this example, we have selected a 16 bit bus, since BUSSIZE is high.

The Motorola Mode

In Figure 8, the 8005 is configured for use with Motorola processors, and the interface fits that processor family. BUSMODE is a ZERO, and we have specified a 16 bit bus, as before with the Intel mode.

A Board Level Ethernet Controller

Figure 9 illustrates a design using the Intel 80186 as a co-processor with the 8005, on the same PC board, to implement Ethernet. The 80186 is a particularly good choice for this application, because it has an on-chip DMA controller.

The 80186 has multiplexed address and data lines, here shown being demultiplexed by the latch. The data bus is buffered by the 74LS245s, but these may not be required, depending on the fanout required by the specific application.

The important signals between the two chips are the following; refer also to Intel 80186 and SEEQ 8005 data sheets.

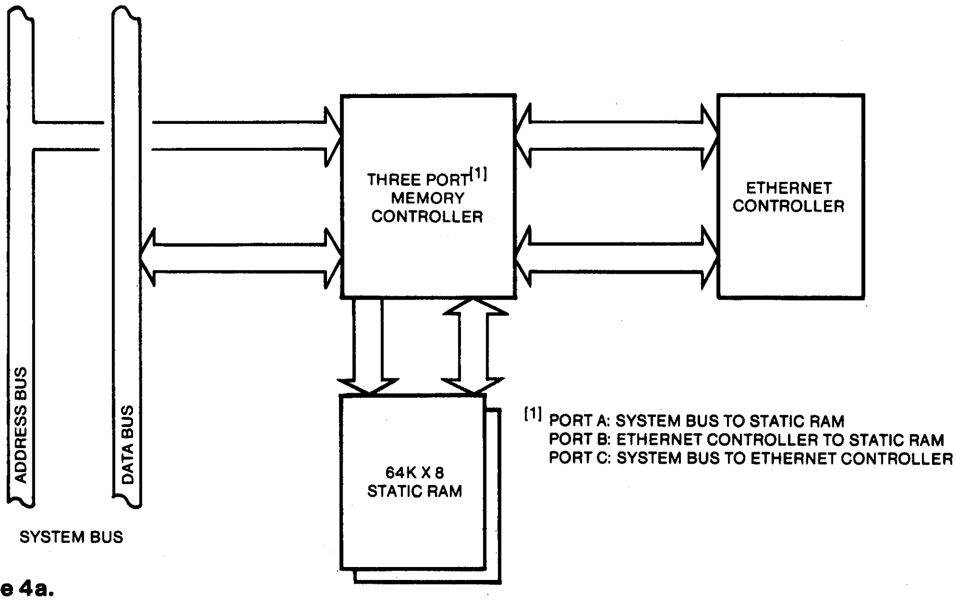


Figure 4a.

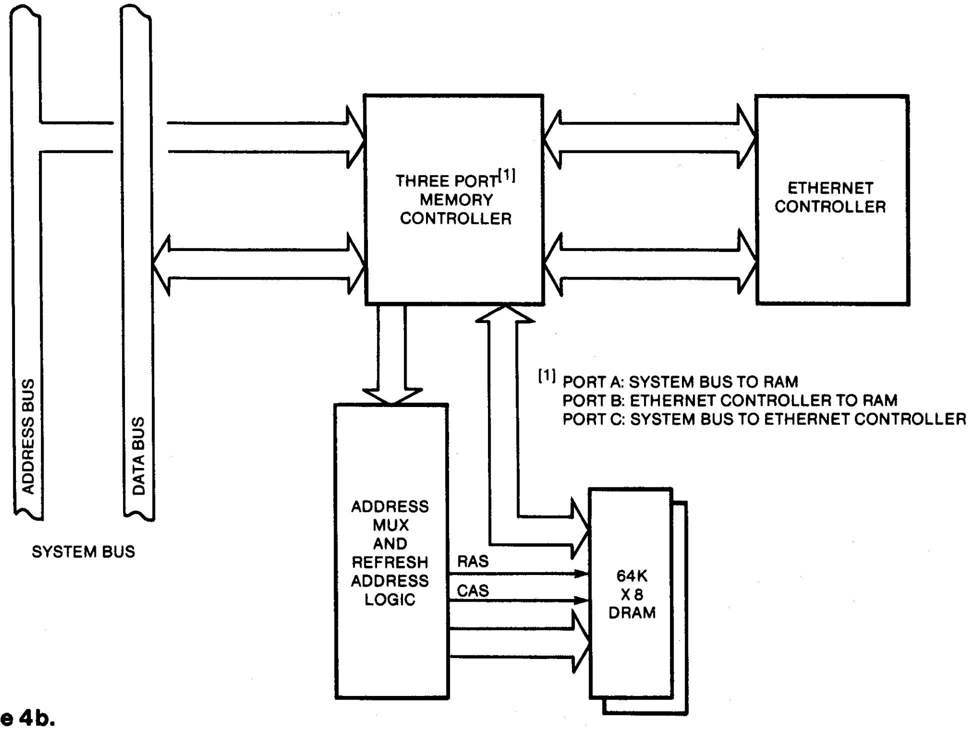
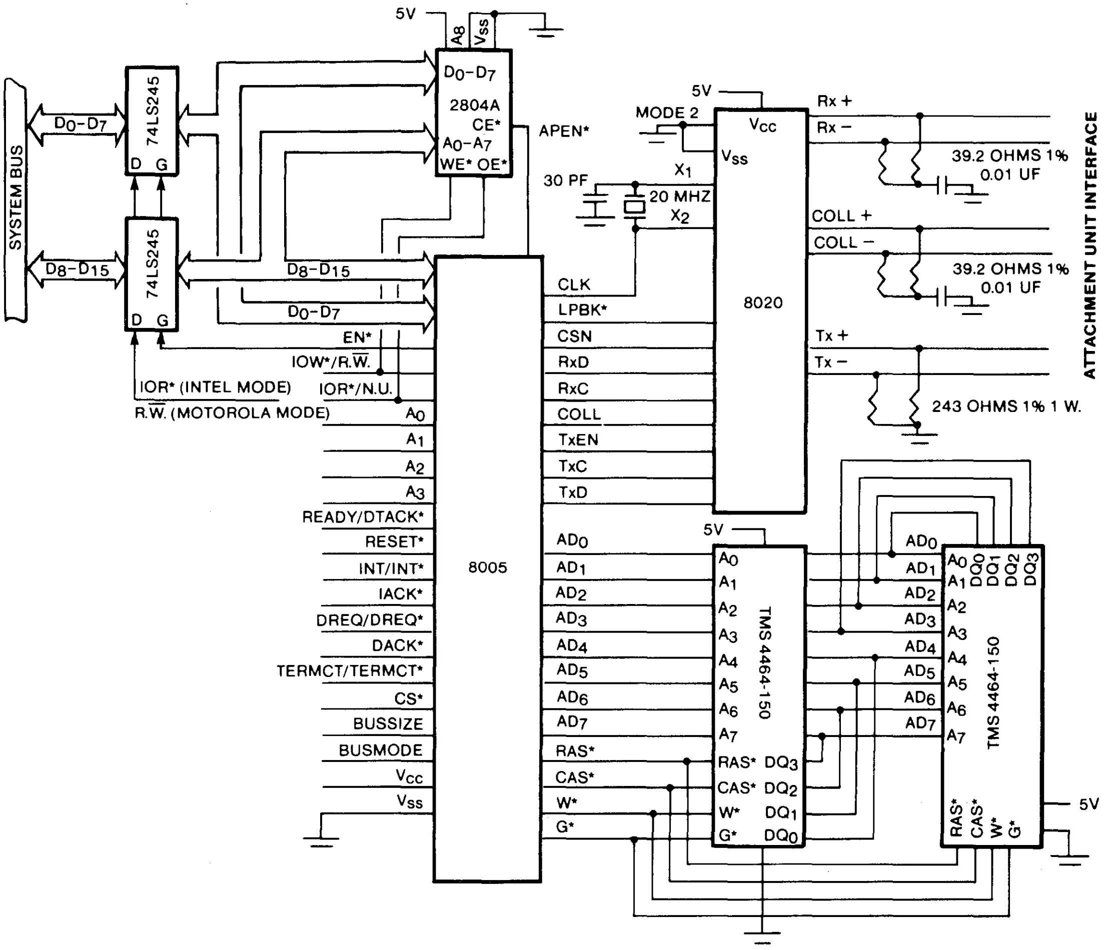


Figure 4b.

Figure 4. Implementing a local buffer for Ethernet traffic, using static RAM (a), and dynamic RAM (b). DRAMs are lower in cost, but require refresh circuitry.



INTERCONNECT DIAGRAM

Figure 5. The 8005 Advanced Ethernet Datalink Controller: it supports a local buffer via DRAM, keeps its Ethernet address and configuration data in its own on-board PROM, and provides a very flexible and sophisticated link between your system and Ethernet.

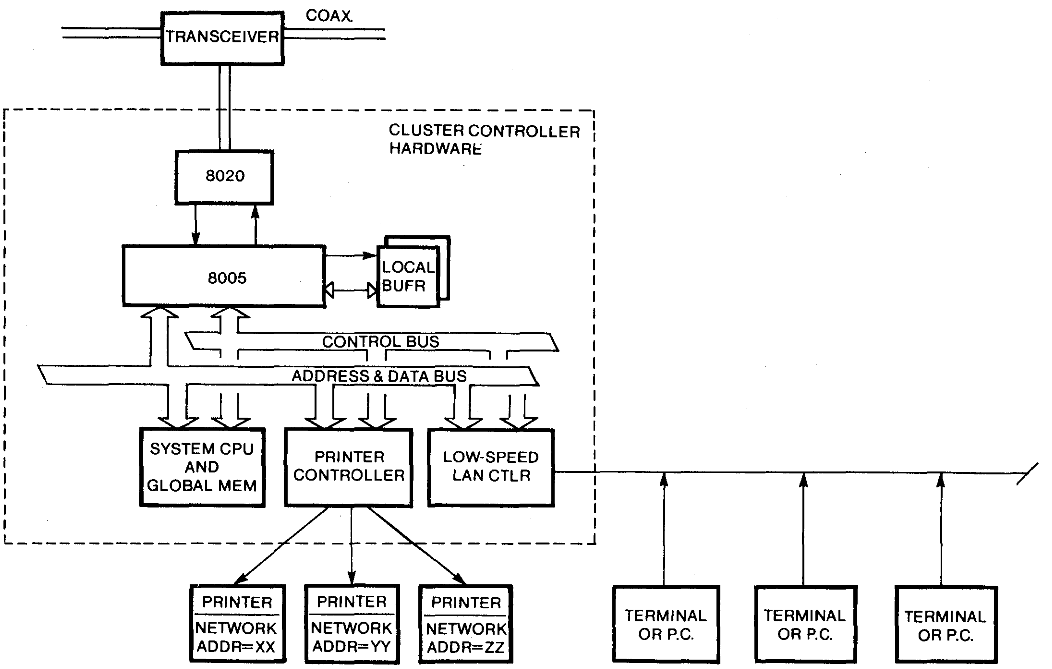


Figure 6. You can connect up to six devices to one Ethernet node using the capability of the 8005 to decode up to six station addresses. In this example, three printers and three PCs or terminals are connected to one Ethernet node. The 8005 and its system CPU controls Ethernet access to and from the devices.

Use DREQ from the 8005 into DRQ0 of the 80186. This is the highest priority DMA request on the 80186. Since the 80186 has no explicit DMA acknowledgment signal, you need to use the peripheral chip select signal: PCS1 is used as the DMA acknowledge, and PCS0 is the 8005 CS (chip select). The 8005 INTerrupt is connected to the 80186 INT0, and IACK of the 8005 is pulled up, since the 80186 does not provide for its use.

The RDY line of the 8005 is connected to the ARDY (asynchronous ready), since the two chips are each running off their own clocks. At the 80186, pull up SRDY (synchronous ready).

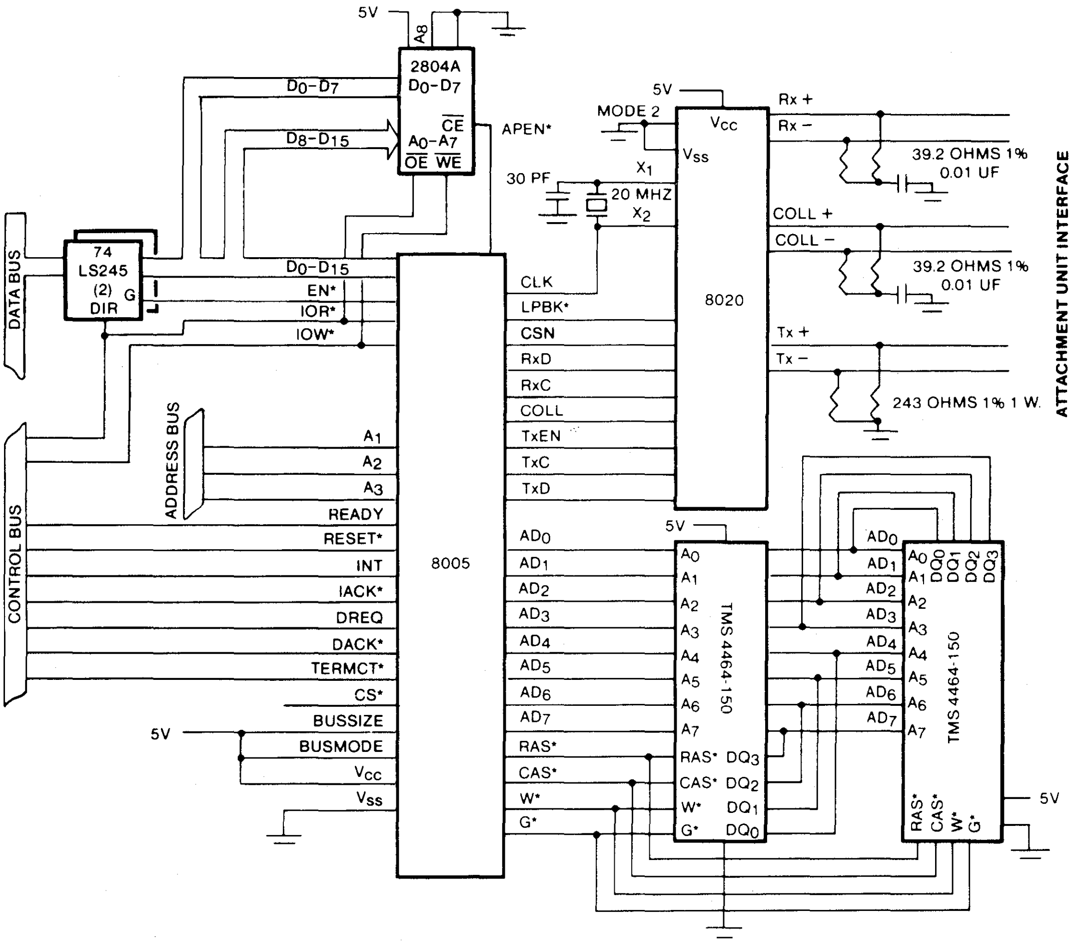
The 80186 does not provide a terminal count output, as do many other DMA controllers, to indicate to the 8005 to drop its DMA request. Therefore, when the 80186 Terminal Count Interrupt occurs, software must disable the DMA request in the 8005 by setting bit 11 in the command register.

Other Support Circuits

The 8005 supports a PROM, shown here as a 2804A E^{2}PROM. The PROM is used primarily to store its Ethernet address and configuration data, but other convenient data may be stored there too.

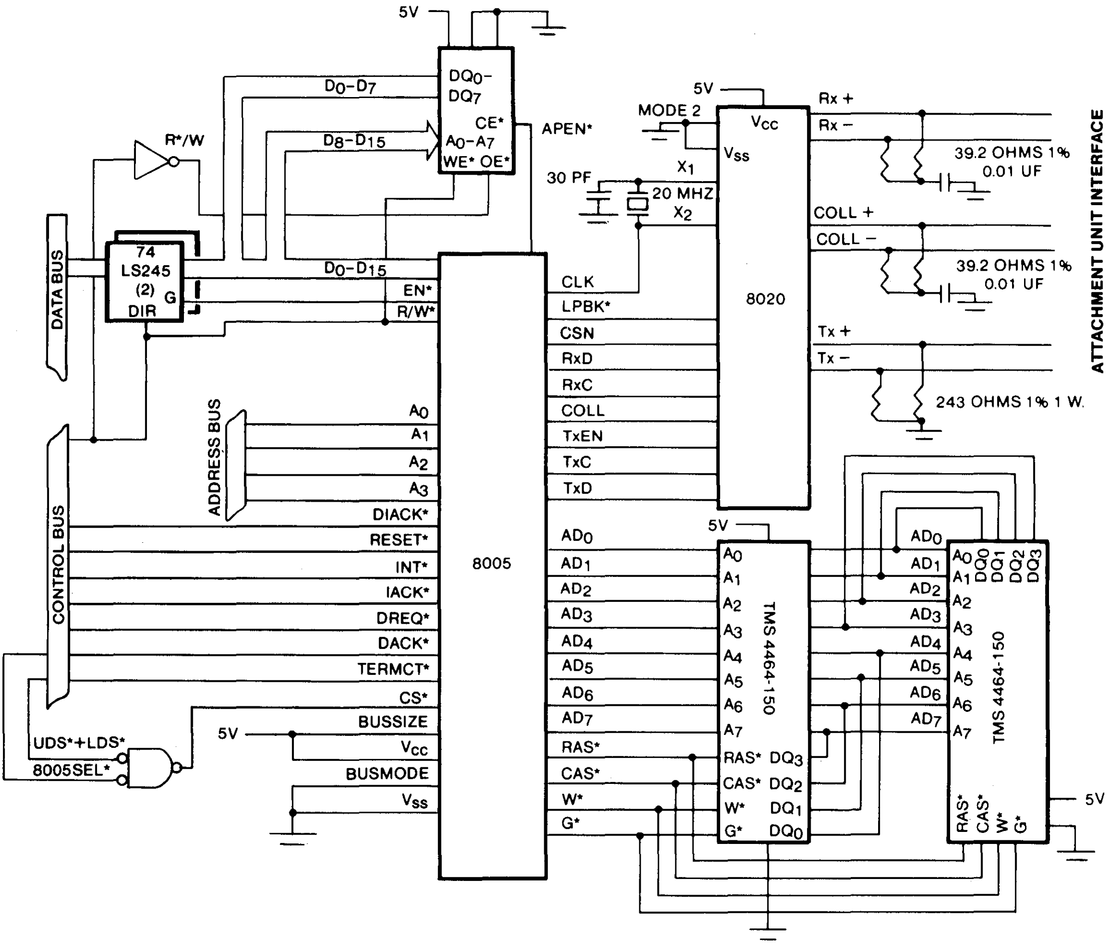
The 8005 supports the TI TMS 4464 DRAMs (or equivalent) with a minimum of PC board circuit traces by multiplexing both address and data lines to the DRAMs. Two DRAM chips provide an ample 64 Kbytes of Packet Buffer storage. The 8005 allows you to partition this buffer into receive and transmit areas of your own choice.

Finally, the diode RC network provides a power on reset pulse (minimum 10 microseconds wide) for both the 8005 and 80186.



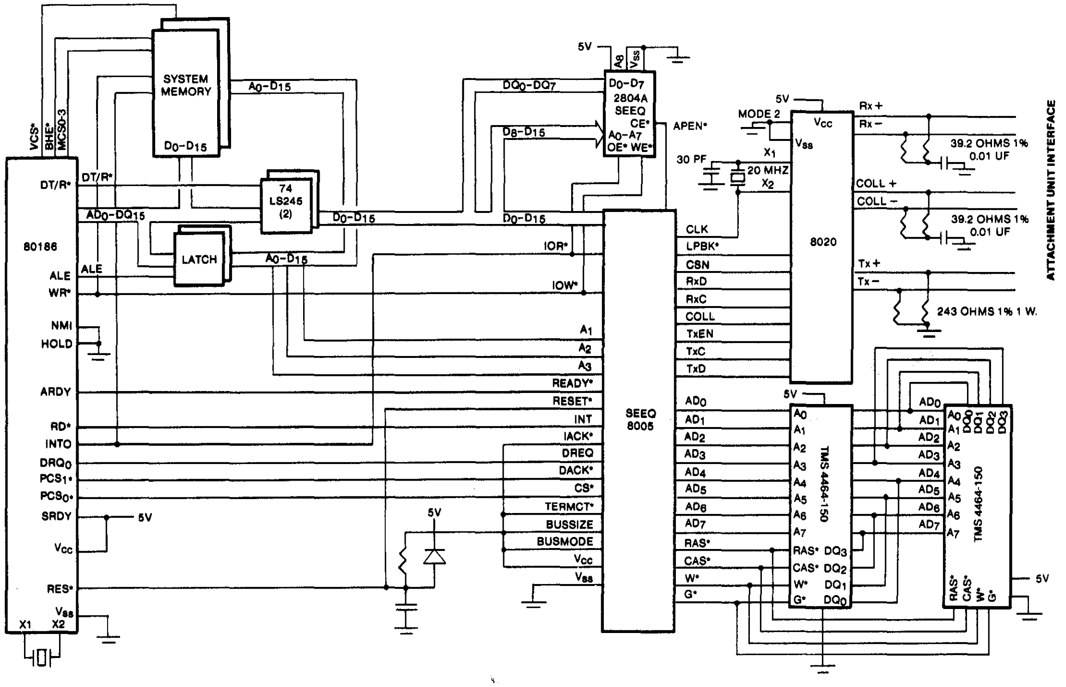
INTERCONNECT DIAGRAM
8005, 16 BIT BUS, INTEL MODE

Figure 7. The 8005 interfaced with an Intel processor. This example illustrates the use of a 16 bit bus, since BUSSIZE is a ONE.



INTERCONNECT DIAGRAM
8005, 16 BIT BUS, MOTOROLA MODE

Figure 8. The 8005 in a Motorola environment, and with a 16 bit bus size.



INTERCONNECT DIAGRAM
8005 AND INTEL 80186

Figure 9. The use of the 8005 and the Intel 80186 to implement a board level intelligent Ethernet data link. The 80186 is a good companion for the 8005, since it has an on-chip DMA controller. The 8005 supports an address PROM, and 64 Kbytes of DRAM to serve as a local Packet Buffer.

The 8005 in Non Ethernet Applications

The Ethernet, because of its simplicity and high speed, is often used in smaller physical configurations than those for which it was originally intended. Applications include communications between processors in a large parallel processing engine.

The 8005, because of its configurability, can be "trimmed down" for use in networks which need not strictly follow the Ethernet format.

The Ethernet address is six bytes long. The 8005 may be configured to accept just a 2 byte address, saving four bytes per address in a packet. Since there are two address fields per packet (destination and source), eight bytes are saved.

Ethernet specifies a minimum "slot time" of 51.2 microseconds. This represents the time required for one round trip of a packet on a maximum length cable, and is required for reliable collision detection. The 8005 may be configured for a slot time of 12 microseconds, which shortens waiting time after a collision. Additionally, when you select the shorter slot time, the 8005 automatically reduces the Collision Jam Pattern from 8 to two bytes, and reduces the interframe spacing from 9.6 to 2.4 microseconds.

Refer to the 8005 data sheet for more detail on selecting these optional parameters.

Configuring the 8005

This step is required following hardware reset or software reset. Note that a hardware reset must be provided following power on. Following reset, allow 10 microseconds after the reset before attempting access to the part.

Configuring includes loading the Ethernet station address(es), selecting transmit and receive packet buffer size and defining interrupt conditions and an optional interrupt vector.

All this information may be stored in a PROM on the same PC board as the 8005. This allows the assigned Ethernet station address(es) to travel with the board.

Register Architecture

The general approach to initializing the 8005 consists of reading information from the PROM into system RAM and writing it back into several registers inside the chip. See Figure 10, which depicts the Register Model of the 8005.

There are nine 16-bit registers which are directly accessable by using the signals Chip Select, I/O read, I/O write and A_1 through A_3. There are also four registers which are selected by the buffer window code bits and accessed indirectly through the buffer window register.

In the discussion below, note that the 8005 has been configured for a 16 bit bus. Input A_0 (pin 54) is ignored when in 16 bit mode, and is shown as a "Don't Care" (X). In 8 bit mode, A_0 selects the low order byte when a ZERO, and the high order byte when a ONE.

Reading the Address (EE) PROM

After reset, if you are using a local Address PROM, write that location to the DMA Address Register which points to the first configuration byte in the PROM. Select access to the Address PROM by writing 0006 to the Buffer Code Bits in Configuration Register #1. The 8005 will then drive the chip enable line of the PROM via APEN (pin 10) for each Read or Write to the Buffer Window Register. When all configuration and station address bytes have been moved into system RAM, the next step is to write them into the 8005.

Loading Indirect Registers

Indirect registers are selected by the buffer code in Configuration Register #1 and accessed through the buffer window register. All indirect registers are 8 bits wide and therefore only use data bits D_0–D_7.

Station Address Registers

To load the station address registers, select the desired station address register set by writing a value from 0000 to 0005 to Configuration Register #1. Then write the appropriate 6 byte address to the buffer window register, one byte at a time, with the most significant byte first, and the least significant byte last. Each write automatically increments an internal pointer register to the next byte of the station address. Repeat this process until you have loaded all desired station address registers.

Specify Transmit Buffer Size

Write a 0007 to Configuration Register #1 to select the Transmit End Area register. Write an 8 bit value to the Buffer Window register which specifies the most significant byte of the last address in the Transmit Buffer space.

For example, to define space for four packets, each 1514 bytes long:

$$\begin{array}{rl} 1514 \times 4 = & 6056 \text{ bytes for data} \\ 4 \times 4 = & \underline{16} \text{ bytes for header} \\ & 6072 \text{ bytes required;} \\ 6072/256 = & 23+, \text{ or hex } 0017 \end{array}$$

Thus, we would write hex 0017 to the transmit end area register. This also sets the receive buffer area, by default, to start at hex 1800, which leaves 58 Kbytes (hex FFFF minus hex 1800) for receive packets.

If interrupts will be enabled and an interrupt vector is required, write a 9 into Configuration Register #1 to select the Interrupt Vector Register, and then write the 8 bit interrupt vector into the Buffer Window Register.

Specify Receive Buffer Size

Write an 8 bit value into the least significant byte of the Receive End Area Register to specify the most significant byte of the last buffer address for receive packets. This would normally be hex FF if the rest of the local buffer is to be used for received frames.

Loading Direct Access Registers

Initialize Transmit Pointer Register

Write 0000 to this register.

Configuration Register #1

Loading this register defines receiver match modes, enables station address register sets and sets up DMA burst interval and size. Access this register by setting A_3–A_0 to 001X.

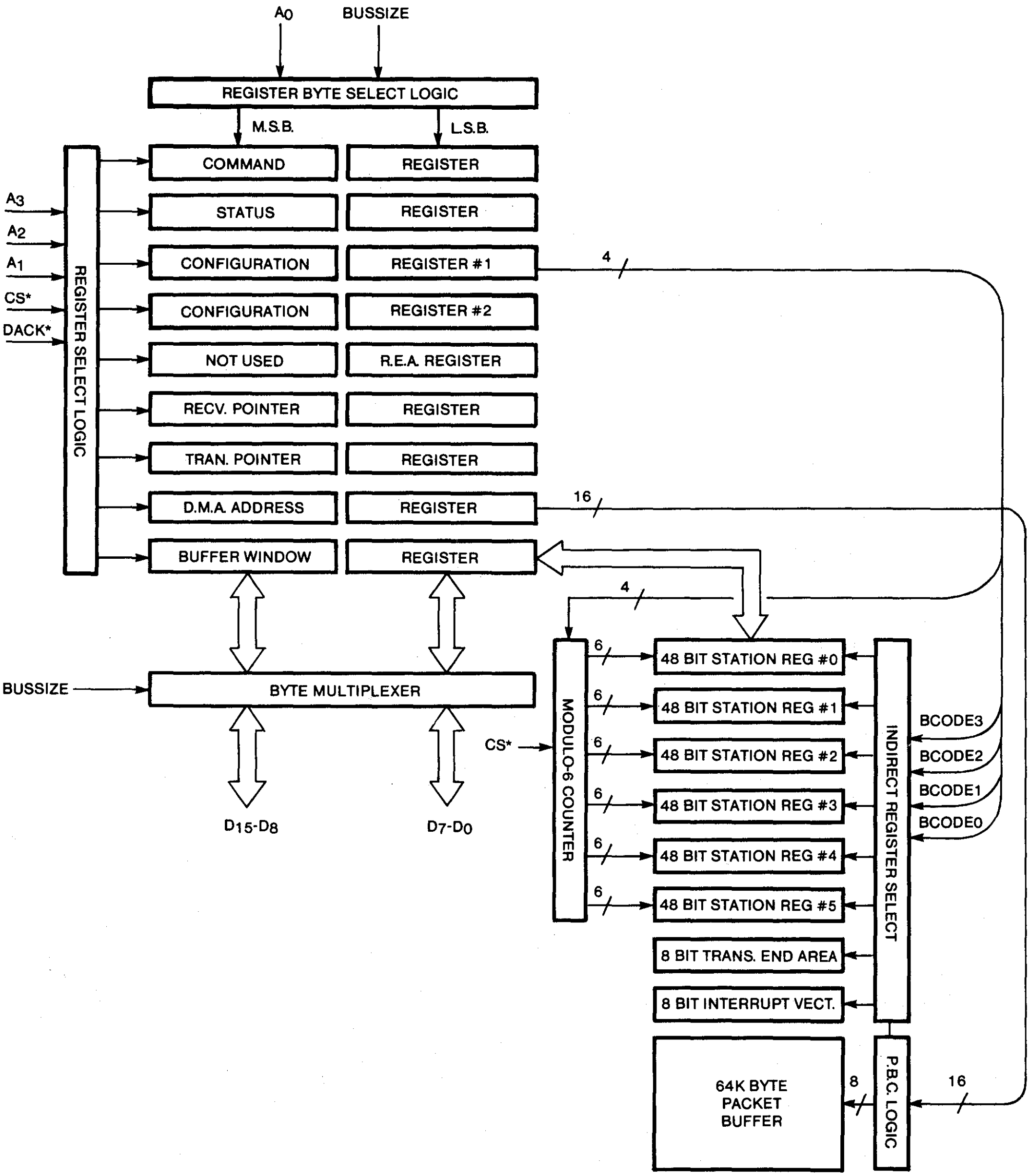


Figure 10. Register Model, which illustrates the register architecture inside the 8005. Using both directly and indirectly accessable registers lowers pin count. All access to indirect registers and the Packet Buffer is through the Buffer Window Register.

Configuration Register #2

Following reset, this register is configured for IEEE 802.3 compatible network interface. It contains bits to select non-IEEE 802.3 network operation, diagnostic modes (CRC enable/disable for both receive and transmit), enable receiving packets with errors (short frames, dribble errors, CRC errors, overflow errors), select byte order for 16 bit bus and enable automatic receive end area update.

Initialize Receive Pointer Register

Load this register with the same value as the Receive Start Area (16 bit Transmit End Area address plus hex 0100). Save this value, since it points to the first byte of the next packet header, and you will need it to find the next received packet.

In the example above, the Transmit End Area address was hex 17FF. Therefore, the Receive Pointer Register should be loaded with hex 1800.

Initialize DMA Address Register

If no packets are to be loaded into the transmit area, load this register with the contents of the Receive Pointer Register.

Command/Status Register

Set R_XO_N (bit 9), and, if desired, R_X I_{NT} Enabl (bit 1) to ONEs. If you are not using interrupts, you may poll R_X I_{NT} (bit 5) to see if a frame has been received.

Transmitting a Frame

This discussion assumes that the system is connected to an IEEE 802.3 compatible network. The contents of a Transmit frame have no meaning to the Packet Buffer Controller and the Ethernet Data Link Controller circuitry, and can be arbitrary in length and content. As discussed above, transmission of the Preamble and CRC (frame check sequence) can be suppressed under software control for specialized network requirements or diagnostic tests.

After you have gone through the configuring as outlined above, the 8005 is ready to receive or transmit frames. Refer to Figure 2 and recall that a frame consists of from 64 to 1514 bytes, which includes a 6 byte destination address, a 6 byte source address, and an area for data all of which is supplied by your system software. The entire frame has a prefix containing a 62 bit preamble

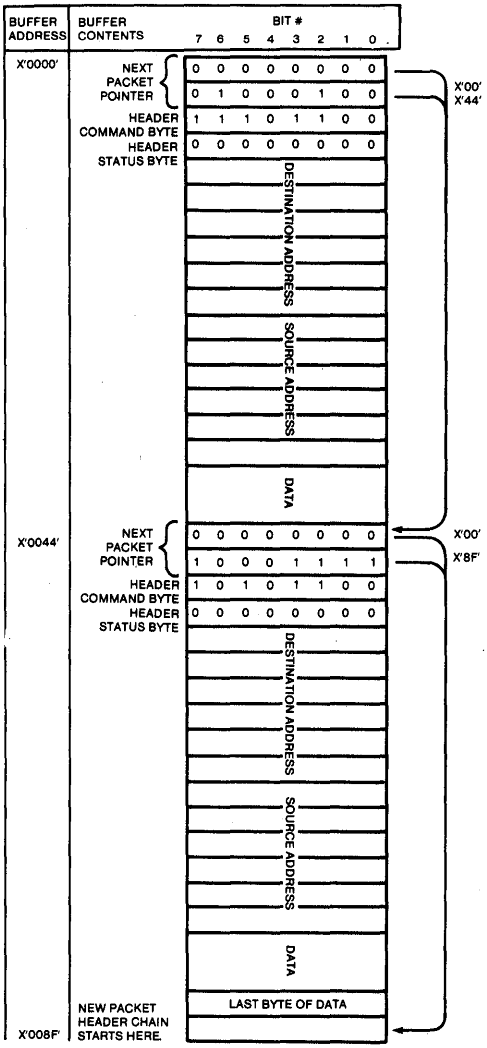


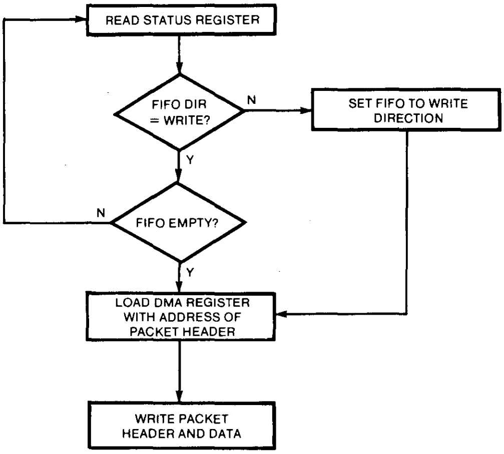
Figure 11. Transmit Packet Chain, residing in the Packet Buffer, and ready to be transmitted. Two packets are in this chain. Note that the Packet Buffer is nondestructively read, and the packets are still in the buffer after they have been transmitted. After transmission, the 8005 updates the Header Status Byte (byte 4). The first two bytes of the Packet Header point to the address of the first byte of the second Packet Header.

(which synchronizes the phase-locked-loop in the Manchester Code Converter with respect to the received packet), and a 2 bit start frame delimiter. Following the data field there is a 4 byte frame check sequence. All of the components of the prefix and the CRC are supplied by the 8005.

A packet is prepared for transmission by writing into the Transmit Buffer Area a 4 byte header, followed by the destination address, the source address, and finally the data field. Refer to Figure 11. You may choose to do this via programmed I/O, or via an external DMA controller. Frames may be chained together up to the capacity of the available Transmit Buffer Area by using the Next Packet Pointer (first two bytes) and the Chain Continue bit (bit 6) in the Transmit Header Command byte.

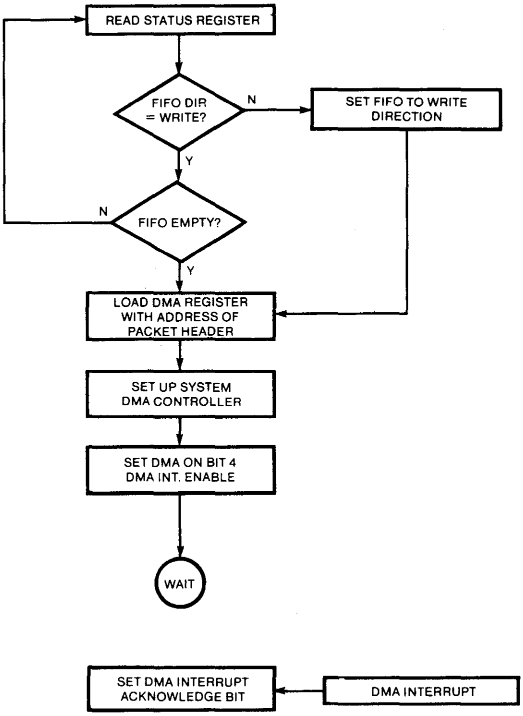
Refer to Figure 12. Read the Status Register to see if the DMA FIFO direction is set to write to the Packet Buffer (bit 15 cleared). If it is and the DMA register is not going to be loaded with a new value then data can be written immediately. If the DMA register is to be changed, then check to ensure that the FIFO is empty (Status Register bit 4 set). If the FIFO is not empty, continue testing bit 14 until the FIFO is empty. If you change the FIFO direction or write to the DMA Register, FIFO contents will be cleared.

If necessary, load the DMA Register with the address for the first byte of the Packet Header, and write Packet Header and data into the FIFO. The first Packet Header address is normally 0000.



LOADING TRANSMIT PACKETS INTO LOCAL BUFFER PROGRAMMED I/O

Figure 12. Loading Transmit Packets into the local Buffer, under Programmed I/O conditions. Note that, if you change the direction of the DMA FIFO, or load the DMA Pointer Register, you will lose any data stored in the FIFO.



LOADING TRANSMIT PACKETS INTO LOCAL BUFFER DMA TRANSFER WITH INTERRUPT

Figure 13. Loading Transmit Packets into the Local Buffer under DMA transfer, using Interrupt.

Figure 13 depicts the same operation, only under DMA control, After you set up the system DMA controller, set DMA ON (Command Register, bit 8), and DMA Interrupt Enable (Command Register, bit 0), if desired. The former enables the DMA request logic, and the latter causes an interrupt to be generated at the completion of a DMA operation i.e., when terminal count has been input.

After all of the packets in a given chain have been written into the Transmit Buffer Area, load the Transmit Pointer Register with the address of the first byte of the first transmit packet header, set T_XO_N (bit 10) and, optionally, T_XI_{NT}Enabl (bit 2) to ONEs in the Command/Status Register.

The 8005 will then read the first header, which is pointed to by the Transmit Pointer Register, and process that packet, and all additional packets in the packet chain in turn. Any retransmission of a packet due to a collision will be automatically handled by the 8005, thus relieving your system from having to transfer that packet of data more than once.

When a packet has been successfully transmitted (or 16 collisions occur), the Done bit (bit 7) in the transmit header status byte will be set to a ONE. The Transmit Buffer Area occupied by that packet is now available for another packet, and may be written to at the same time as subsequent packets are being transmitted. The 8005 will move to the next packet in the chain.

When all packets in a chain have been completed (transmitted successfully or collided 16 times), the 8005 resets T_XO_N (bit 10) in the status register to indicate that it is ready to transmit another packet chain. If 16 collisions occur on a packet, the 8005 stops transmission attempts for that packet only and moves to the next packet in the chain, if one exists. In the example in Figure 11, bits 2 and 3 are ON in the transmit header command byte which will cause the 8005 to set the transmit interrupt bit in the status register and, if enabled, interrupt the processor when 16 collisions occur or the transmission is successful.

The last packet in the chain is denoted by having the Chain Continue bit cleared to a ZERO. The Next Packet Pointer points to the address following the last byte of the last packet.

You may treat the transmit packet buffer in one of two ways:

1. As a circular buffer with wraparound, where you remember the address to load new packet headers and packet data. The DMA register automatically wraps around to address 0 when the transmit end area has been reached.

2. As a linear buffer, where you reset the transmit pointer to 0000 after each packet chain transmission.

Receiving Frames

Once the 8005 has been configured and the receiver enabled, frames which meet the match mode and station address requirements specified in Configuration Register #1 and the enable bits 2 - 5 in Configuration Register #2 will be moved into the Receive Buffer Area beginning at the address contained in the Receive Pointer Register.

When one or more packets are available in the receive area, the 8005 sets R_X Interrupt (bit 5) in the Command/Status Register to a ONE. If receive interrupts are enabled. (Command Register bit 1 set), then the external interrupt (pin 11) is asserted. Frame header and data can now be read by loading the DMA Register with the starting address of the Packet Header and executing successive reads. If Auto Updat REA (bit 1 of Configuration Register #2) is set, the Receive End Area Register will be updated with the upper byte of the DMA register each time a DMA read occurs. This releases buffer space as its contents are read, and allows for the receipt of more data at the same time as data is being read out.

The action taken on a receive packet depends on the status of the packet and its contents. If the packet status is bad, it may be skipped entirely without transferring any of its data to system memory by loading the Receive End Area Register with the most significant byte of the next packet pointer. This will release the buffer space of the previous packet for future packets. In like fashion, if the packet data shows it to be an "overhead" packet (such as a Packet Acknowledgement), this can be so noted in network software and the packet skipped. Thus, unnecessary transfer of the packet over the system bus can be avoided, and system bandwidth preserved. If the packet data must be processed, just the information portion of a packet (exclusive of any bytes used to pad the packet to a minimum size) can be read to system memory by programmed I/O or by an external DMA controller.

Receive Packet Chaining

The 8005 automatically chains together receive packets using a circular FIFO buffer structure. Each packet is prefaced by a 4 byte header whose first two bytes form a 16 bit address that points to the next header. A chain of packets always ends with a header-only packet whose 4 bytes equal 00. The address of this header-only packet should be saved, since it will contain the header of the next packet received. It is a simple matter to follow the packet chain from header to header until the chain Continue/End bit is read as a ZERO, calculate the length of the chain and set up the DMA Register and an external DMA controller to transfer the entire chain of packets to system memory if desired. This is advisable in applications where high average receive data rates are expected and data must be moved quickly from the local buffer to the system memory at the expense of bus bandwidth. To minimize system bus utilization, packets can be moved one at a time; this permits moving only the information content of a packet.

Calculating Packet Chain Length

In order to perform a DMA transfer, you need to give the DMA controller the "count"; i.e., how many bytes (or words, in a 16 bit system) will be transferred. To do that, you need to calculate how many bytes are available in the Packet Buffer as a result of receive activity.

Refer to Figure 17. This flow chart illustrates the steps required to calculate the length of the packet chain.

The first step requires that you know the Packet Buffer address of the last packet header read in the most previous receipt of Ethernet data. If the 8005 has just been initialized, the address is the beginning of the Receive Packet Buffer which was determined earlier in this note (hex 1800). If packets have been previously been read this address will be the location of the header last read that had the chain continue/end bit reset.

The next step, referring to Figure 17, is to turn off the Auto Updat REA (Configuration Register #2, bit 1). This insures that the 8005 will not use the area occupied by this packet chain for new receive data.

Read each Packet Pointer in turn, and then read the Header Status byte immediately after the Pointer, which is Byte #3. Bit 6 of Byte #3 is the Chain Continue bit. Continue reading this bit in each packet header until this bit goes to ZERO. This signals the end of the chain. Save the local buffer address of the first byte of this last header as this is the address of the header for the next packet received. Subtract the address of the first header in the chain from this address. If the result is a positive number, you have the chain length directly.

If the result is negative it denotes that the Receive Pointer Register has wrapped around past the beginning address of the receive area. The chain length will be equal to the sum of the receive buffer size plus the value (including sign) of this result. You already know the buffer size, since you defined it during configuration of the 8005: hex FFFF minus the receive start address (defined during configuration) plus 1. For the previous example, the buffer length is hex E800 (FFFF - 1800 + 1). Load the chain length into the DMA controller, and set Auto Updat REA. You are now ready to read data out of the receive buffer and into system memory.

There are two ways to read Packets out of the Local Buffer:

1. Via programmed I/O.
2. Via DMA transfer.

The front end portion of each procedure is the same: first, check to see if the FIFO is empty; then set it to Read. If the FIFO is not empty, check to see if it is in the Write direction. If not, load the DMA Register with the address of the next Packet Header. If this is the first Packet to be read, this address will be that which was derived when you defined the Transmit Buffer size during configuration of the 8005.

Reading Packets Using Programmed I/O

The data path between the local buffer and the host bus is buffered by a 16 byte FIFO called the DMA FIFO. It serves as a rate buffer between the host and the local buffer, especially for 16-bit data transfers. Because the local buffer is a shared resource (there are 4 ports including the DRAM refresh port), the initial read from the buffer window which follows loading the DMA register may take eight microseconds worst case. The 8005 signals this delay by deasserting Ready (if Busmode=1) or delaying D_{TACK} (if Busmode=0). If this initial read wait state is unacceptable, then the buffer window interrupt feature can be used.

The buffer window interrupt is asserted for programmed I/O reads (not DMA reads) when the DMA FIFO has data available.

Under Programmed I/O control (see Figure 14), after you load the DMA Register, read Status Register bit 7, Buffer Window Interrupt or wait for a hardware Buffer Window Interrupt if it is enabled. When the interrupt is asserted, read Packet Header and data out of the receive FIFO, via the Buffer Window, until all bytes have been transferred.

Reading Packets Using DMA

The second approach is by DMA transfer. See Figure 15. After loading the DMA Register, load the system DMA controller with the destination address in system memory, and the previously calculated packet chain length. Then set DMA ON (bit 8 in the Command Register). This enables the DMA Request logic inside the 8005. Optionally, set DMA Interrupt Enable, which will cause an Interrupt to be generated when the DMA controller has asserted Terminal Count. The DMA Request output signal will be asserted when there are a sufficient number of bytes in the DMA FIFO to satisfy the DMA Burst Size (2, 4, 8, or 16 bytes) which you selected earlier when configuring the 8005.

Interrupts

There are several interrupt sources in the 8005. This section describes these interrupts and how to service them. For this discussion, refer to Figure 18.

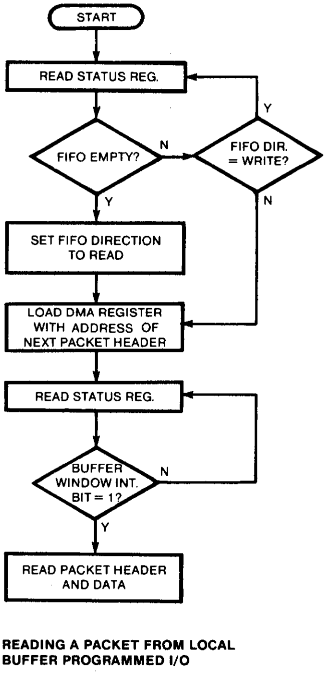


Figure 14. Reading Packets out of the FIFO using the Programmed I/O procedure.

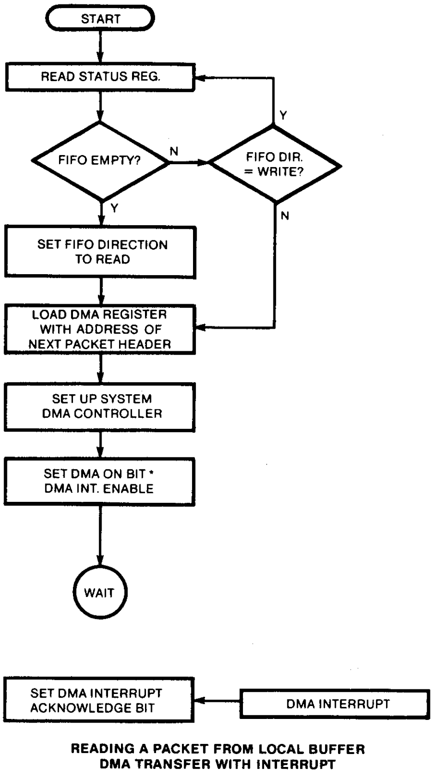


Figure 15. Reading the Local Buffer under DMA control.

Transmit Interrupts

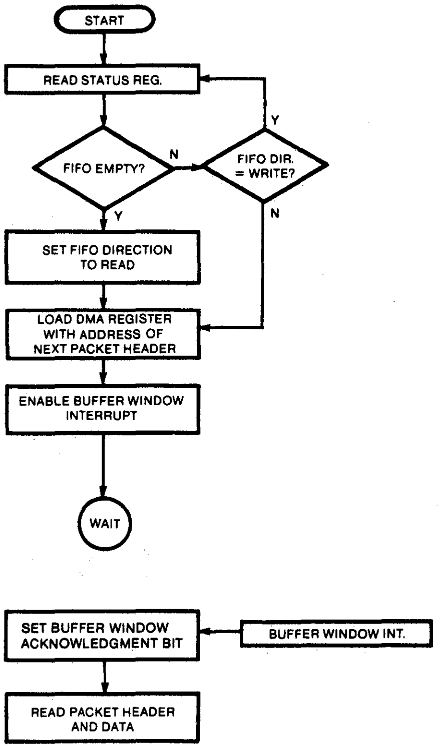
There are four transmit interrupt sources in the 8005; Babble, Collision, 16 Collisions, and Transmit Success. Each of these can set the transmit interrupt bit in the status register if so programmed in the transmit header command byte. If T_X Interrupt Enable (Command Register bit 2) is set, the 8005 will also assert an interrupt on pin 11. The transmit interrupt is cleared by setting $T_X I_{NT} A_{CK}$ (bit 6) in the command register.

Babble Interrupt

The 8005 will transmit packets as large as will fit in the transmit buffer. The IEEE 802.3 standard specifies a maximum packet size of 1514 bytes. The babble interrupt indicates that a packet larger than 1514 bytes was transmitted.

Collision Interrupt

When a packet collision occurs, the 8005 packet buffer controller automatically restores its transmit pointer to the beginning of the packet and schedules retransmission following the back-off time. In some applications it may be desirable to record the number of collisions that occur. This bit enables setting the $T_X I_{NT}$ bit in the status register for each collision.



READING A PACKET FROM LOCAL BUFFER USING BUFFER WINDOW INTERRUPT

Figure 16. Reading a Packet from the local Packet Buffer using the Buffer Window Interrupt approach.

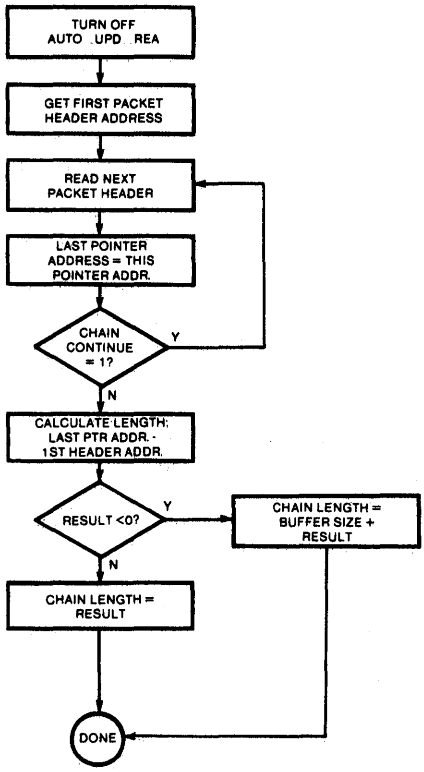


Figure 17. The steps necessary to calculate the length of a Packet Chain. You need to save the address of the last header in the last packet read, in order to perform the calculation.

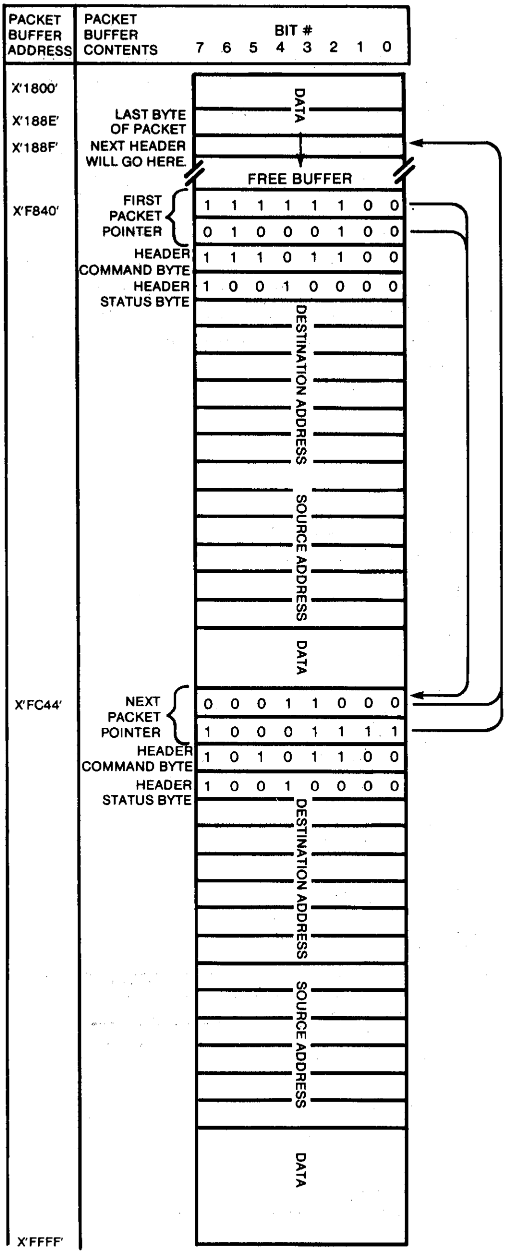


Figure 17a. Example of two receive packets in a packet chain with wraparound.

16 Collisions Interrupt

The 8005 counts the number of collisions that occur on each packet. If a packet has collided 16 times, the usual cause is a network fault such as an unterminated coaxial cable or an open in the cable. This interrupt notifies the host that a packet has collided 16 times, and the packet buffer controller will now abandon transmit attempts for that packet and move on to the next packet in the chain if one exists.

Transmit Successful Interrupt

This interrupt indicates that a packet was successfully transmitted with less than 16 collisions.

Receive Interrupts

The 8005 sets the receive interrupt bit (status register bit 5) whenever a packet that meets the criteria in bits 2 - 5 of Configuration Register #2 has been placed in the local buffer. It will remain set and, if the receive interrupt enable bit is also set, the external interrupt will remain asserted until the receive interrupt acknowledge bit is set. If a separate interrupt for each packet is desired, the receive interrupt should be acknowledged within 70 microseconds, which is the minimum time for receipt of a subsequent 64 byte packet. If more than 70 microseconds elapses before acknowledging a receive interrupt, it is possible for additional packets to be added to the packet chain.

The 8005 protects the receive interrupt condition such that if a new interrupt is being generated while the host is setting the receive interrupt acknowledge, the receive interrupt will persist. If, however, a new frame is received after the interrupt acknowledge and before the calculation of the packet chain length, the packet chain which is read will include the new packet associated with the new interrupt. The new interrupt, when serviced, will now be associated with an empty packet since it was part of the previous chain.

DMA Interrupts

The DMA interrupt bit in the status register is set following receipt of terminal count from the external DMA controller. If the DMA interrupt enable bit (command register bit #0) is also set, an external interrupt will be asserted. The interrupt is cleared by writing a 1 to the DMA interrupt acknowledge bit.

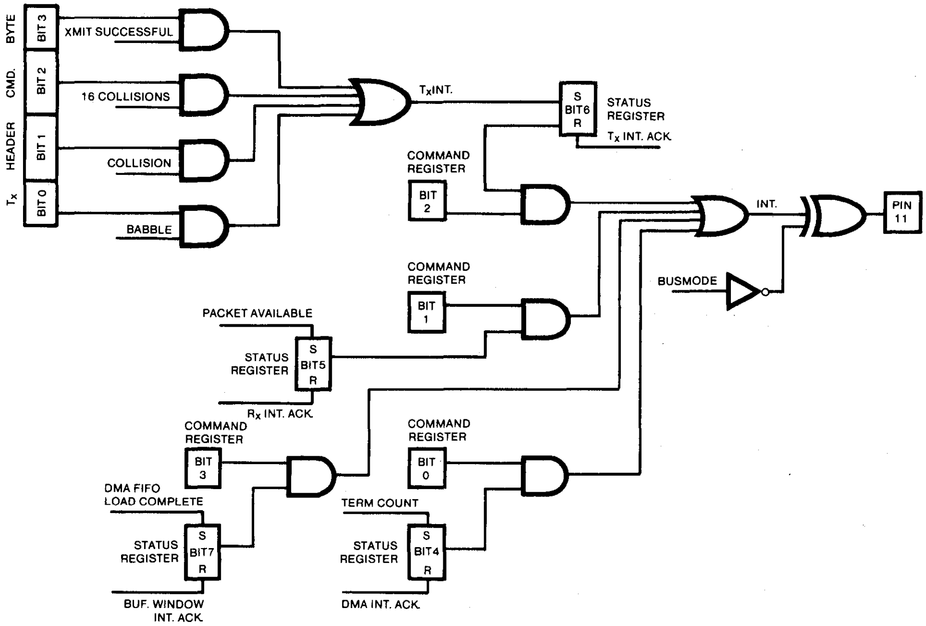


Figure 18. Functional diagram of interrupt logic.

Self-Test and Network Diagnostics

The 8005 contains a number of special features for self-test and network diagnostic support.

Loopback

Two forms of loopback are possible with the 8005. Local loopback is accomplished when the 8005 is connected to an 8020 Manchester Code Converter. When bit 11 of Configuration Register #2 is set, the loopback pin of the 8020 will be brought low. This causes transmitted data to be looped back to the receiver of the 8020. If the packet transmitted meets the match mode and is addressed to one of the 8005's enabled station addresses, it will be received and placed in the local buffer. Using diagnostic control bits 9 and 10 in Configuration Register #2, it is possible to transmit packets with CRC errors to check the receive CRC logic, and to include the CRC in a receive packet to check the transmit CRC logic. Loopback can also be accomplished by connecting the 8020 to an Ethernet transceiver. Because the network is half-duplex, any data transmitted will also be received. Thus the same loopback test as above can be performed while the network is active by simply sending a packet to oneself.

Interrupts

The 8005 has separate control bits for turning on an off the receive logic, transmit logic and DMA logic. The interrupts for these functions can be tested without actually performing the function by setting both the on and off control bits simultaneously. For example, if the receive interrupt logic is to be tested set both R_XO_N and R_XO_{FF} bits in the command register. This will cause the receive interrupt bit in the status register to be set and, if the receive interrupt enable bit is also set, will cause an external interrupt. This mode has no effect on any logic other than the interrupt logic and associated status register bit, i.e., packets can be transmitted and received while this diagnostic mode is set.

Detecting Network Cable Faults

It is possible to make a gross determination of cable faults by taking advantage of the full-duplex nature of the 8005: although it will not transmit while receiving (that would violate the Ethernet specification), it does receive while transmitting, as long as the packet destination address fits the receiver match mode.

Cable Opens/Missing Terminator

An open coaxial cable or a missing cable terminator results in the transmission line being terminated in an infinite impedance. Thus, any data transmitted will be reflected back from the impedance mismatch some time delay after it is transmitted. This time delay depends on the physical distance to the impedance mismatch, so the length of the packet must be large enough to insure that data are still being transmitted after one round trip propagation delay to the mismatch. A 256 byte packet should be an adequate size. The reflected signal will partially cancel the transmitted signal and cause a collision to be detected by the transceiver. Thus an open is indicated by repeated collisions when transmitting a packet or, if the network is known to be quiet (no other nodes active), a single collision when transmitting. It is also possible to make a rough determination of where the fault is by enabling receipt of packets with errors (Configuration Register #2 bits 3 - 5) and then counting the number of bytes correctly received. Note that if the cable open is very close to the transmitting node, the collision may occur during the preamble and the 8005 would unconditionally reject the receive packet.

Cable Shorts

A shorted coaxial cable causes premature loss of carrier sense to the receiver of the 8005 while it is transmitting. It is therefore possible to send a packet of at least 256 bytes to oneself with the receiver enabled to accept frames with errors. A cable short results in a truncated receive packet; the size of the receive packet indicates the rough distance to the cable short.

EEPROM INTERFACING

April 1987

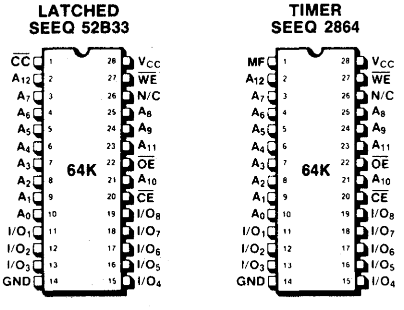
seeq
Technology, Incorporated

EEPROM Interfacing

Introduction

The continuing rapid evolution in semiconductor E^{2}ROM memory device technology offers the system designer an ever-increasing choice of function and capability. With these increasing choices for E^{2}ROM devices, however, comes the problem of standardization (or lack thereof) concerning such specifications as endurance, timing characteristics, interface requirements, ad infinitum. Today, there are two popular types of commercially available E^{2}ROM devices.

Both of these types of devices have the JEDEC-approved pinout shown in Figure 1, including the multi-functional pin 1, but differ in the timing of the control interface. The first E^{2}ROM type, the latched type device, such as SEEQ's 52B33 latches the addresses, control, and data inputs on the falling edge of $\overline{\text{WRITE ENABLE}}$ ($\overline{\text{WE}}$). For this type device, the $\overline{\text{WE}}$ input must remain active low for the duration of the write cycle. The second type of E^{2}ROM, the timer-type device, latches addresses, data, and control signals on the rising edge of $\overline{\text{WRITE ENABLE}}$ or the rising edge of $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$). For the timer device, such as SEEQ's 2864 the $\overline{\text{WE}}$ input need not be held low for the entire write cycle. The primary difference between the latched and timer devices is the control timing required to interface to the microprocessor. Each of these types of devices has advantages depending on system performance and configuration requirements.


LATCHED SEEQ 52B33

TIMER SEEQ 2864

Figure 1. JEDEC Pinout — 64K E^{2}ROMs

When the designer attempts to use the advantages of both in the same system, a problem is encountered.

One of the most frustrating problems facing a system designer is the design of an E^{2}ROM/microprocessor interface that will allow compatible operation of timer and latched type E^{2}ROM devices in the microprocessor-based system. The purpose of this application note is to give examples of cost-effective designs of E^{2}ROM/microprocessor interfaces, which allow the use of both timer and latched E^{2}ROM devices in the system with no changes required to either the controlling software or the hardware. With the interfaces shown in this application note, it is possible to operate with BOTH latched and timer devices simultaneously in the system if the device access times are compatible.

The microprocessor interfaces described in this application note are for the 8085, 8086, 8088, Z80,* and 71840. Software examples are provided for the Z80 and 71840 processors. By extension, the Z80 code is easily transportable to 808X processors. In most cases, the hardware required for compatibility consists of only two additional standard (14-pin) TTL packages.

It is hoped that these example interfaces will assist the system designer in implementing E^{2}ROMs in his system. By no means are these special cases presented to limit the system designer, but to provide a starting point for his design. The interface circuits presented are for the family of E^{2}ROM devices (16K, 32K, and 64K). Other extensions of the ideas presented may permit lower power, lower cost, or optimization of other parameters deemed more important.

The body of this application note consists of two sections. First, the Basic Operation section gives the theory of operation of all of the interfaces and should be read to familiarize oneself with those factors common to all of the microprocessor interfaces. Second, the Microprocessor Interface section details the design of the TTL interface required for the given microprocessor.

Basic Operation

Each of the E^2ROM microprocessor interfaces described in the next section integrates hardware and software to achieve compatibility between latched and timer E^2ROM devices. Naturally, both hardware and software are processor-dependent. However, the write cycle used is basically the same for all the examples shown.

For compatibility between the latched and timer E^2ROM devices, the interface provides control waveforms that have timing compatible with both, since the major difference between latched and timer E^2ROM devices is the timing of the write control interface to the microprocessor (see Introduction). The basic waveforms for latched and timer E^2ROMs are shown in Figures 2a and 2b, respectively. The latched type E^2ROM device acquires data on the leading edge of $\overline{\text{WRITE ENABLE}}$

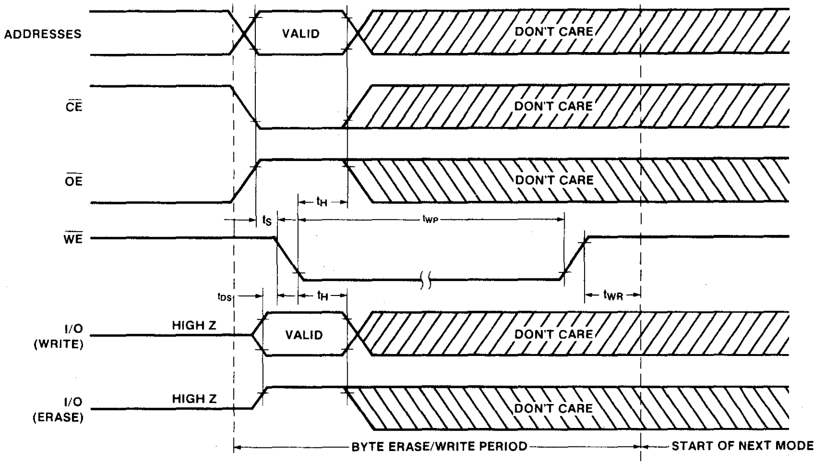


Figure 2a. Latched E^2ROM Write Cycle

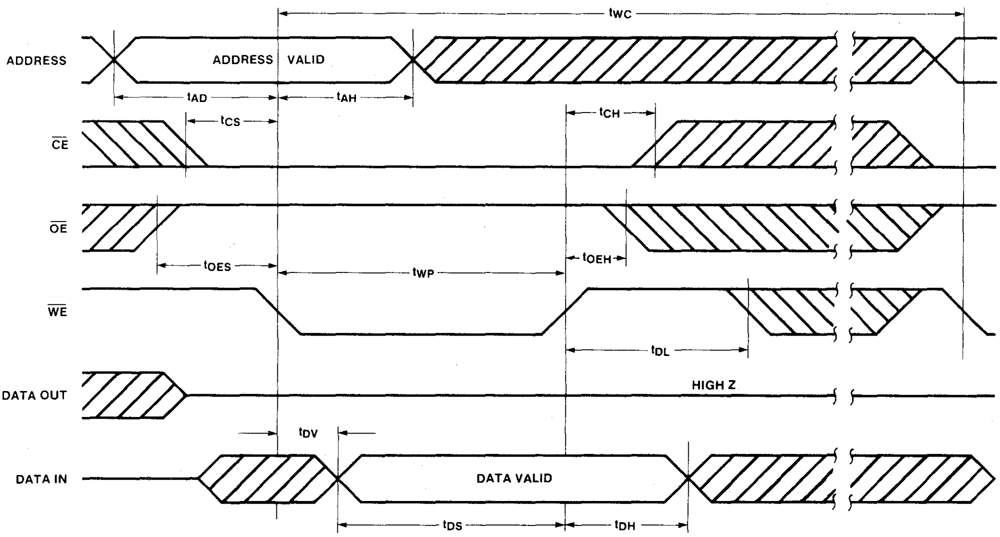


Figure 2b. Timer E^2ROM Write Cycle

($\overline{\text{WE}}$). The timer type device acquires data on either the trailing edge of $\overline{\text{WE}}$ or the trailing edge of $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$). Interface compatibility is achieved between the latched and timer devices by strobing the data, control, and addresses on the leading edge of the Write Enable pulse for the latched device and then by strobing the data on the trailing edge of $\overline{\text{CHIP ENABLE}}$ for the timer device (see Figure 3). By using this technique, the hardware interface is greatly simplified.

The software part of an E^{2}ROM interface is very simple, but very important. A read operation for both latched and timer E^{2}ROM devices is accomplished by a straightforward issuance of a microprocessor Read command at a particular address (see Figure 4). A write operation, however, involves a more complex process.

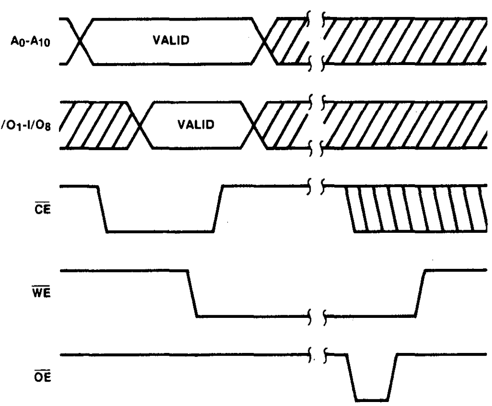
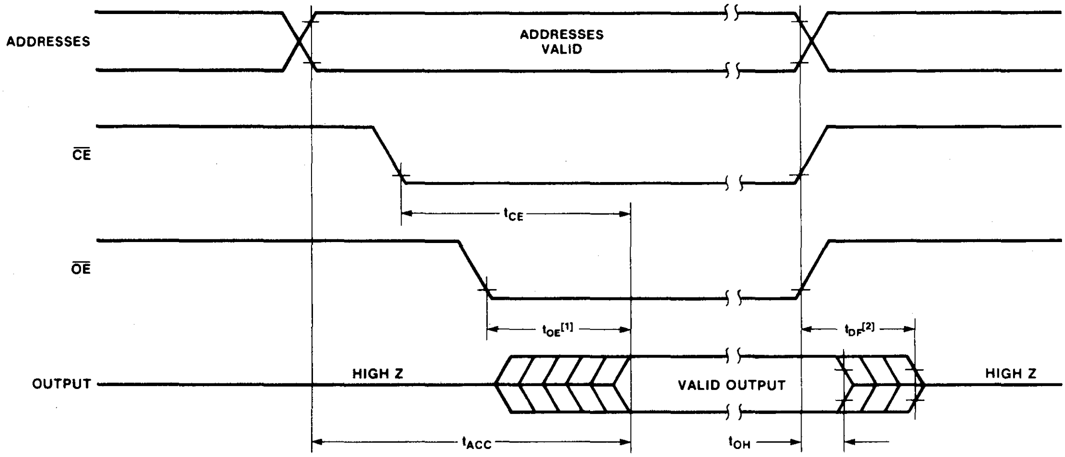


Figure 3. Latched/Timer Compatible E^{2}ROM Write Cycle

The flow chart for writing to the E^{2}ROM is the same for all microprocessors and is shown in Figure 5. After a Write command is issued, time is required to allow proper writing to the storage cell of the E^{2}ROM device. A Read command is then issued to terminate the write operation. Note that this Read command is not to be used to actually read the E^{2}ROM device, but is inserted to reset the logic circuits used to drive the $\overline{\text{WE}}$ input of the E^{2}ROM device.

Between initiation and termination of a write cycle, the interface uses some timing mechanism to assure proper write conditions to the E^{2}ROM and to know when the E^{2}ROM is available for another read/write cycle. The duration of the timeout (t_{WP}) depends upon the type of E^{2}ROM used. For all types, t_{WP} should fall between the minimum and maximum specifications of all E^{2}ROMs for which the application is designed. The latched type of device requires less write time than does the timer type device.

The implementation of this timing can be accomplished in either hardware or software. In hardware timing, a timer can interrupt the processor at regular intervals, or at the end of the desired write time (t_{WP}). In software timing, the processor simply counts down, waiting for the desired t_{WP}. For ease of general implementation, the given examples utilize software timing (see Figure 5). The tradeoffs, however, between software and hardware timing comprise an involved topic. The system designer must make this decision, considering such factors as processor throughput, board space, and expense.



Notes: 1. $\overline{\text{OE}}$ may be delayed up to t_{ACC} — t_{OE} after the falling edge of $\overline{\text{CE}}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{\text{OE}}$ or $\overline{\text{CE}}$, whichever occurs first.
3. This parameter is periodically sampled.

Figure 4. E^{2}ROM Read Cycle

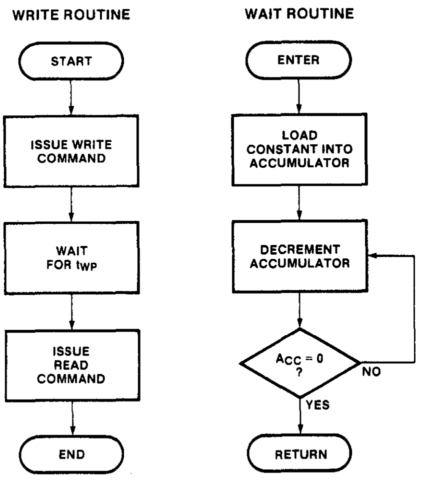


Figure 5. Software Flowchart — E^{2}ROM Write Cycle

After the cycle described by Figure 5 is complete, the E^{2}ROM device is available to be accessed for another Read or Write command. Often, another read will be performed in order to verify the written data. With the solution proposed, this subsequent read cycle will have normal timing, and all required write recovery parameters will be satisfied.

The general description provided above applies to most of the processors shown in the specific examples below. For more detailed information, the reader should refer to the schematic, waveforms, and software that apply to a specific processor.

Microprocessor Interfaces

8085 Interface

The schematic for the 8085 interface to a timer or latched E^{2}ROM device is shown in Figure 6. This interface consists of one each of a 74LS02 and 74LS74 type package and allows the system designer to use the $\overline{WR}$ signal from the 8085 to initiate the write cycle to the E^{2}ROM device. The design permits use of either a timer

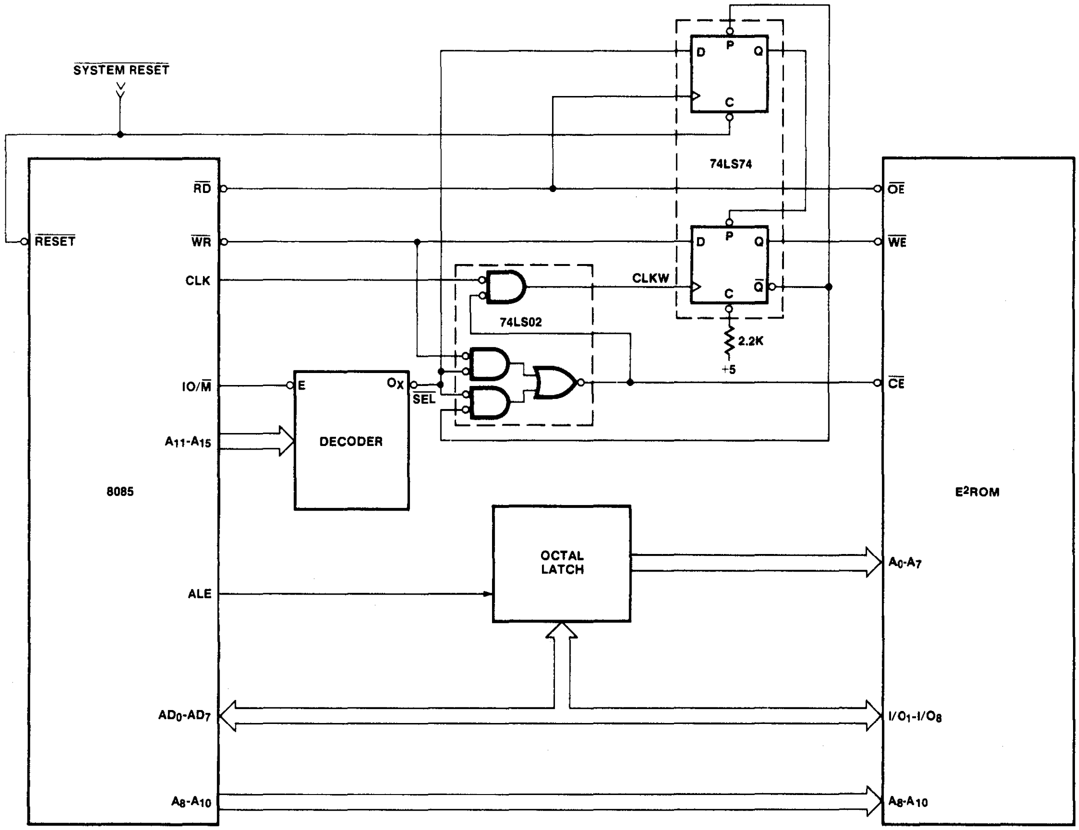


Figure 6. 8085/E^{2}ROM Interface

OR a latched E^{2}ROM device with no change required to the controlling software or hardware. The following discussion of the operation of the 8085 interface relies on the 8085 timing diagram summary for read and write cycles shown in Figures 7a and 7b respectively.

Initiating a write cycle requires the software control routine as charted in Figure 5. Should the reader desire a specific example, the Z80 code (see Figure 12) is transportable to the 8085.

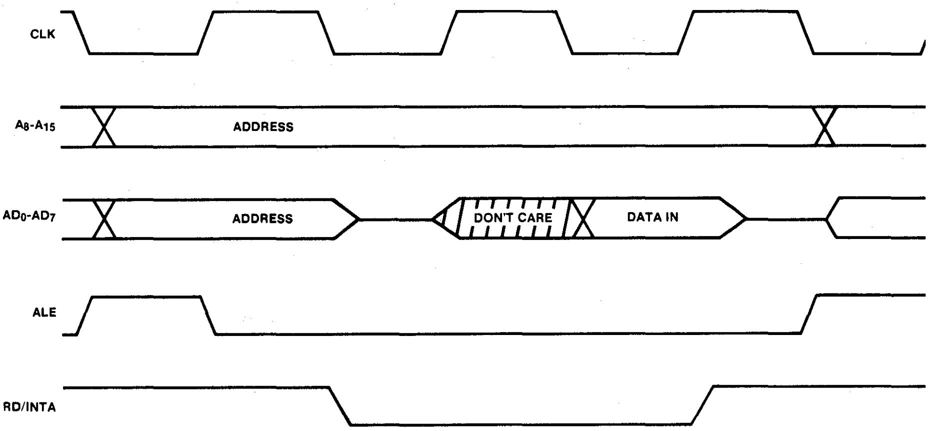


Figure 7a. 8085 Read Timing Summary

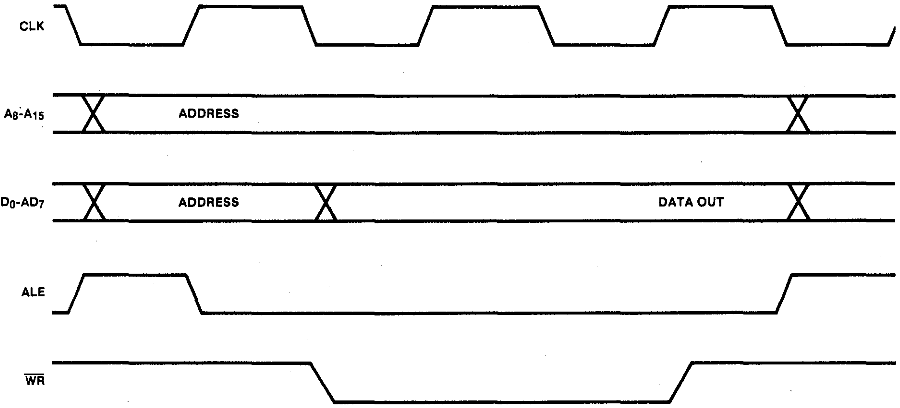
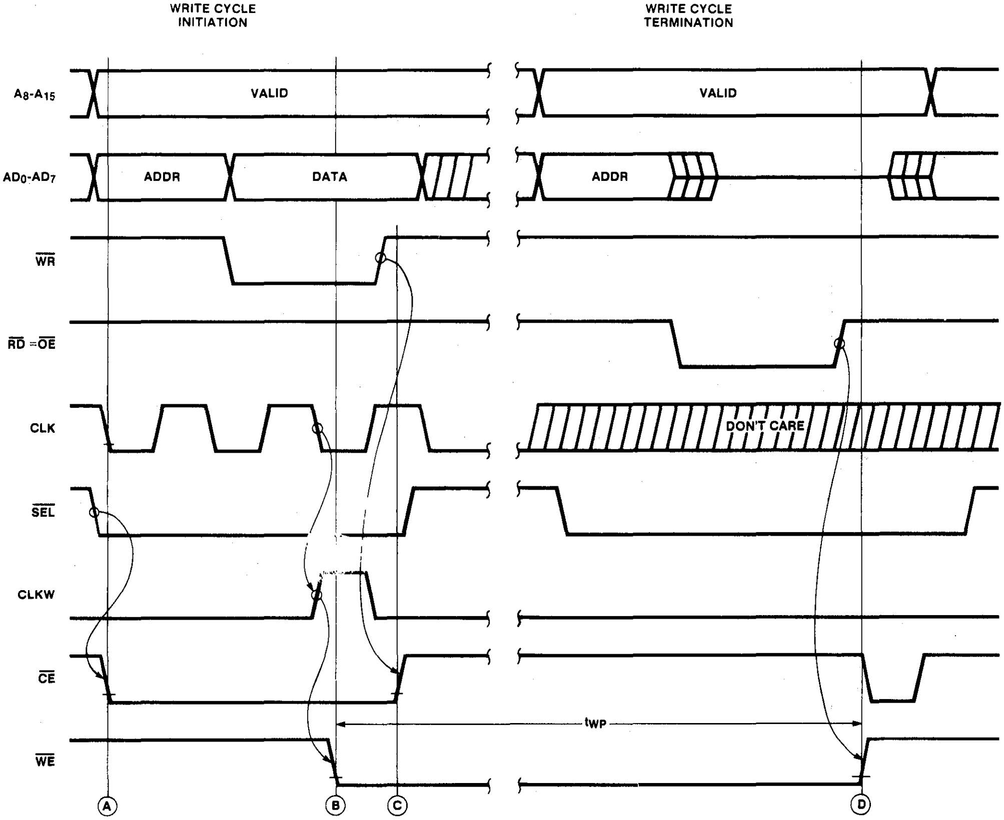


Figure 7b. 8085 Write Timing Summary

The basic write operation waveforms for this interface are shown in Figure 8. The write cycle begins with the addresses becoming valid and being decoded to drive SELECT active low, in order to drive the CHIP ENABLE (CE) active low at the E^{2}ROM device pin (selecting the desired device) (see Ⓐ in Figure 6). An active low level on WR from the 8085 (indicating a write cycle initiation) allows the WRITE ENABLE latch of the interface to be clocked by the next falling edge of the 8085 clock output (CLK) (see Ⓑ). Addresses, data, and control inputs to the latched type E^{2}ROM are latched in at the falling edge of WRITE ENABLE (WE) — shown as Ⓑ in Figure 8. For the timer type E^{2}ROM device, however, data is latched on the rising edge of CHIP ENABLE (CE) — shown as Ⓒ in Figure 8. Note that CE is held active low for a relatively short period of time, while WRITE ENABLE (WE) is held low for the entire write time of the E^{2}ROM device. In this manner, the waveforms shown in Figure 3 are produced, providing signals compatible with both the latched and timer type devices.

To end the write cycle, the 8085 issues a Read command to the E^{2}ROM device. This read cycle enables the Write Reset latch which in turn presets the WRITE ENABLE latch (shown in Figure 6). The preset to the WE latch brings WE to V_{IH} (see Ⓓ in Figure 8). As indicated in Figure 8, this read cycle does not produce valid data from the E^{2}ROM. This read cycle is used merely to terminate the write cycle.

The latched and timer devices respond identically in a read cycle. The 8085 read cycle, shown in Figure 7a, produces the read cycle waveforms shown in Figure 4.



*A_0-A_7: ADDRRESS SIGNALS MULTIPLEXED WITH DATA SIGNALS MUST BE DEMULTIPLEXED USING OCTAL LATCHES.

Figure 8. Timing Diagram — 8085/E^{2}ROM Interface

Z80 Interface

A sample interface is shown for a Z80 processor (see Figure 9). The timing diagram for write cycle waveforms at this interface is also shown (see Figure 10). The basic circuit is very similar to the 8085 interface, with the differences based on the fact that the Z80 has data valid at both edges of $\overline{WR}$ (see Figure 11). This simplified timing allows a more simple interface. The CLK output from the processor is not necessary, and $\overline{WR}$ alone provides timing for the write cycle initiation.

The operation of the circuit is otherwise very similar to the 8085 interface. After addresses are brought valid on the address bus, they are decoded to drive $\overline{SEL}$ active low, which drives $\overline{CE}$ active low at the E²ROM device pin (see Figure 9, and Ⓐ in Figure 10). At the falling edge of $\overline{WR}$ (when this device is selected), the $\overline{WE}$ latch is clocked, bringing $\overline{WE}$ active low (see Ⓑ in Figure 10). At this time, the latched type device latches address, data, and control signals, while the timer type device latches address and control signals. At the falling edge of $\overline{WR}$, the gating circuitry brings $\overline{CE}$ high , latching data for the timer type part (see Ⓒ in Figure 10). Within a normal processor cycle, a write cycle has been initiated with timing in accordance with the general approach of Figure 3. Even with additional buffers which may be common in a bus oriented system, this interface can be used with a Z80, Z80A, or Z80B operating with no wait states at up to 6 MHz clock frequency. The individual system designer, of course, must check his own application to ensure satisfaction of applicable setup and hold requirements in the specific system for which the application is intended.

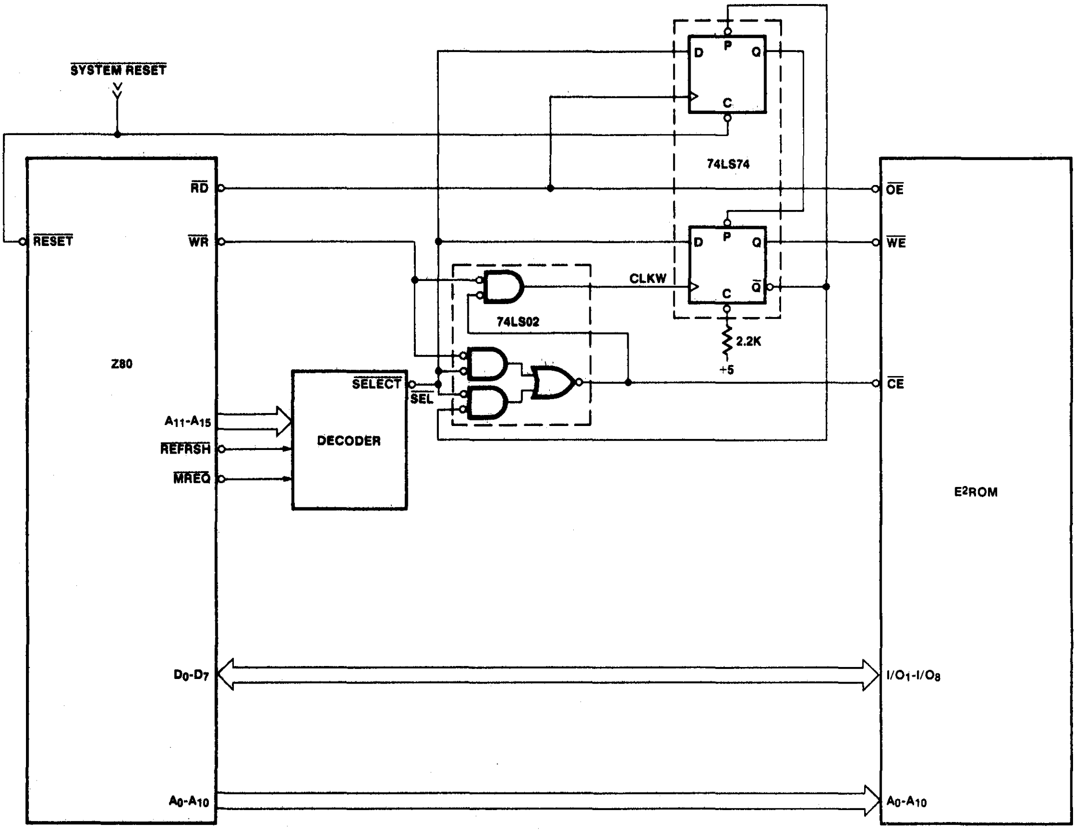


Figure 9. Z80/E²ROM Interface

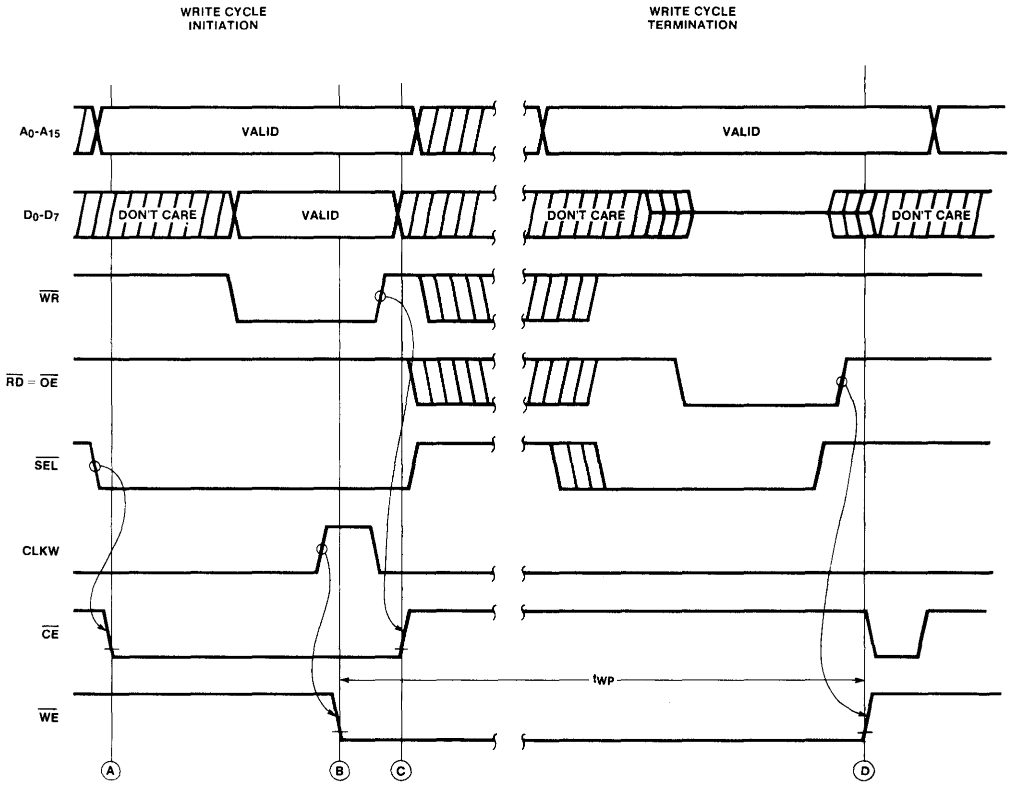


Figure 10. Timing Diagram — E^2ROM Interface (Write Cycle)

The termination of a write cycle is very straightforward. As shown in the Basic Operation section (see Figure 5), a read operation to the E^2ROM terminates the write cycle, but does not provide valid data. For the interface operation in write cycle termination, the reader should refer to Figure 10. The addresses are brought valid on the address bus, and are decoded to drive $\overline{\text{SEL}}$ active low (see Ⓐ in Figure 10). The gating circuitry, however, inhibits $\overline{\text{CE}}$, and $\overline{\text{CE}}$ remains at V_{IH}. At the rising edge of $\overline{\text{RD}}$, the flip-flop receives a positive edge trigger, and clocks in the $\overline{\text{SEL}}$ signal to preset the $\overline{\text{WE}}$ latch. At this point, $\overline{\text{WE}}$ is brought high (see Ⓓ in Figure 10), terminating the write cycle. For the remainder of this processor bus cycle, $\overline{\text{CE}}$ becomes valid for a short while. However, $\overline{\text{RD}}$ is no longer active low, and no valid data is read in this bus cycle. There is no problem with t_{WR} since the write recovery time occurs during the remaining part of this bus cycle.

Frequently, one may wish to read again from the device, in order to verify data written. This read will be a normal read, following the general waveforms of Figure 4. In a read operation, the interface drives $\overline{\text{CE}}$ active low to select the device, and $\overline{\text{RD}}$ enables the output from the E^2ROM device.

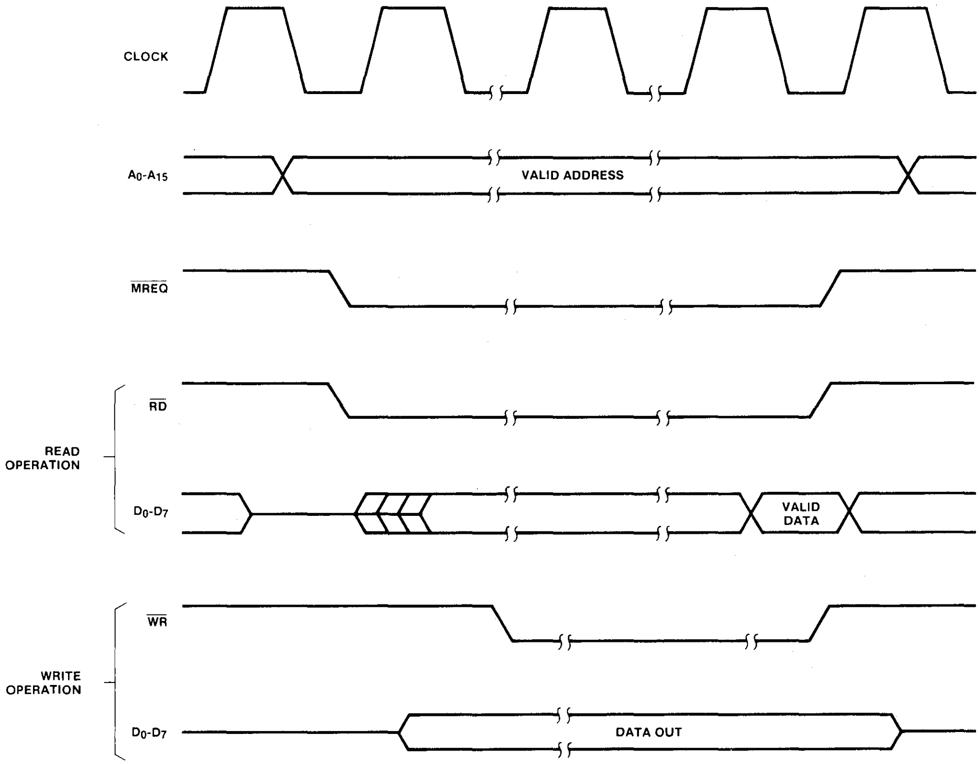


Figure 11. Z80 Read and Write Cycle

```
                            EEWRZ80.1
LOC    OBJ CODE M STMT SOURCE STATEMENT                         ASM 5.9

                    175
                    176  ;-------------------------------------
                    177  ; Z80 EEROM Write routine.
                    178  ; Incorporates auto-erase and timing
                    179  ; in software.
                    180  ; Accepts: address to be written: Reg DE
                    181  ;          Data    to be written: Reg B
                    182  ; Uses: A, B, D, E Destroys: A
                    183  ;-------------------------------------
                    184
009B   3EFF         185  EEWR:   LD      A,0FFH   ; FF for erasure.
009D   12           186          LD      (DE), A ; BEGIN ERASE
009E   CDAE00       187          CALL    WaitTwp
00A1   1A           188          LD      A, (DE) ; END ERASE
                    189
00A2   78           190          LD      A,B      ; Data to be written
00A3   12           191          LD      (DE), A  ; BEGIN WRITE
00A4   CDAE00       192          CALL    WaitTwp
00A7   1A           193          LD      A, (DE) ; Read to end Write
00A8   1A           194          LD      A, (DE) ; Read to Verify
00A9   B8           195          CP      B       ; Check Verification
00AA   C2C800       196          JP      NZ, ERR1
00AD   C9           197          RET
                    198
                    199
                    200  ;----------------------------
                    201  ; Wait routine for EEROM Byte/ Erase
                    202  ; Uses: Registers A, B,C
                    203  ; Destroys: A,C
                    204  ;----------------------------
00AE   78           205  WaitTwp:LD      A,B
                    206  ; Store B reg in TMP1
00AF   3202C0       207          LD      (TMP1),A
                    208
                    209  ; Set timing constant for Twp.
                    210  ; This 16-bit constant is loaded
                    211  ; into Registers BC, and depends
                    212  ; on the speed of the CPU clock.
00B2   3E07         213          LD      A, 07
00B4   47           214          LD      B,A
00B5   3E06         215          LD      A, 06
00B7   4F           216          LD      C,A
                    217
                    218  ; The following loop performs the wait,
                    219  ; by decrementing BC until the 16-bit
                    220  ; number contained in BC equals zero.
                    221
00B8   3E00         222          LD      A, 00H
00BA   0B           223  More:   DEC     BC
00BB   B8           224          CP      B
00BC   C2BA00       225          JP      NZ, More
00BF   B9           226          CP      C
00C0   C2BA00       227          JP      NZ, More
00C3   3A02C0       228  DUN:    LD      A, (TMP1) ; Restore B Reg
00C6   47           229          LD      B,A
00C7   C9           230          RET
```

Figure 12. Z80 E²ROM Erase/Write Routine

APP. NOTES

8088 Interface

An example interface is shown between an 8088 (operating in minimum mode) and a 16K E^{2}ROM (see Figure 14). The reader may note that this is almost identical to the 8085 E^{2}ROM interface (see Figure 6), with only minor differences. First, the NOR gates used cannot be a standard TTL or LSTTL device, but must be a CMOS or other high impedance input, so that the CLK signal is not loaded. The CLK signal, as output by the 8284, is used as the clock input to the 8088. The V_{OH} level on this signal can fall below specification as a result of a TTL load. A CMOS NOR package, such as a 74C02 or similar device, eliminates this problem. Since the 74LS74 operates from bussed control and data lines, its requirements are not so stringent, and a 74LS74 will work fine in most applications.

The operation of this circuit is almost identical to the operation of the 8085 interface, as a comparison of the timing diagrams will show (see Figures 7b and 15) Because these processors share similar bus timing, the signals differ only in magnitudes of setup and hold times. All required setup and hold times should be confirmed to the satisfaction of the system designer.

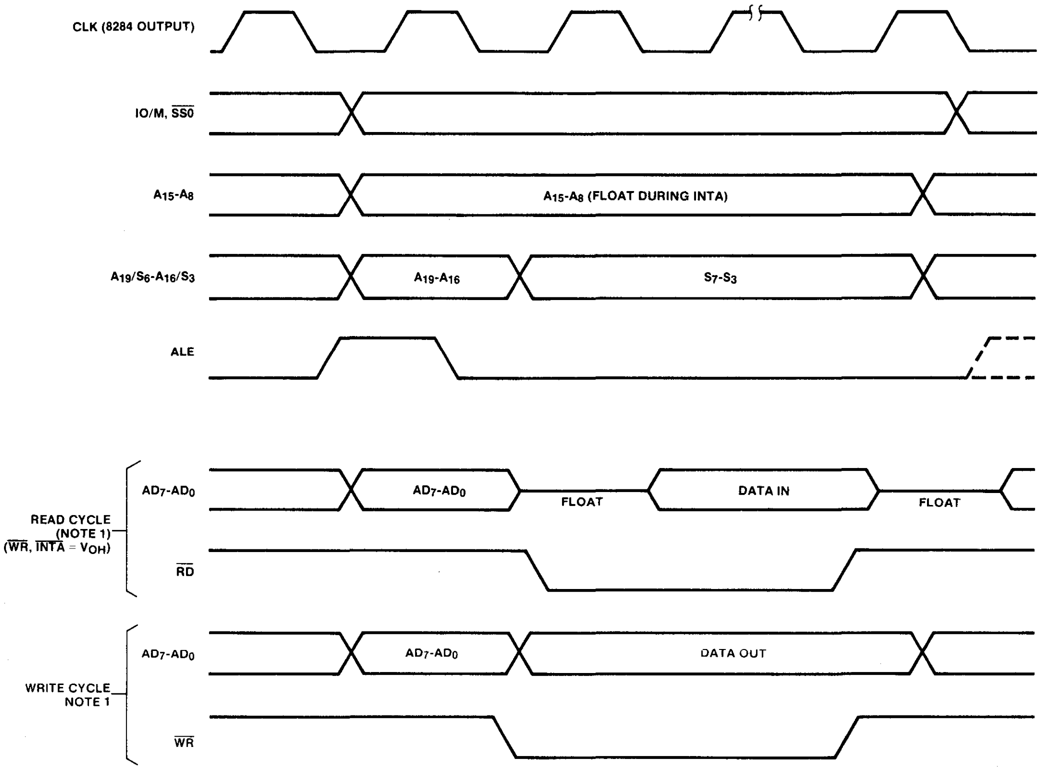


Figure 13. 8088/8086 Bus Timing — Minimum Mode

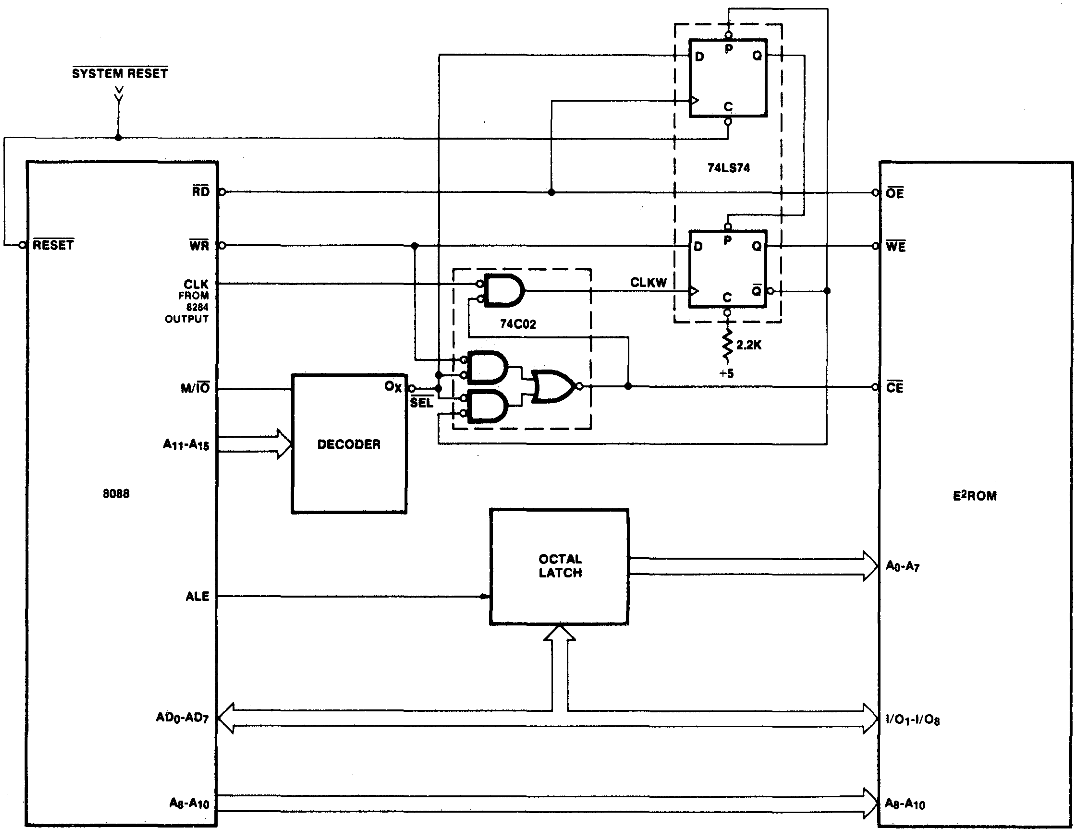
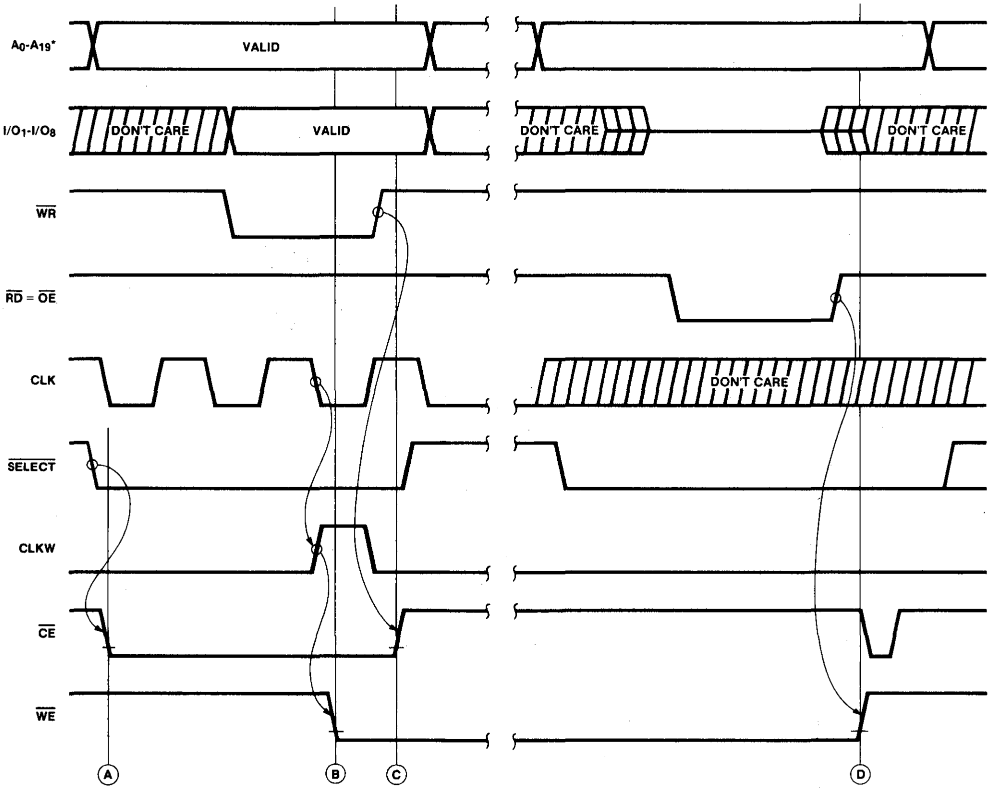


Figure 14. E^{2}ROM Interface — 8088 (Minimum Mode)



*A0-A19: ADDRRESS SIGNALS MULTIPLEXED WITH STATUS AND DATA SIGNALS MUST BE DEMULTIPLEXED USING OCTAL LATCHES.

Figure 15. Timing Diagram — 8088/8086 E^{2}ROM Interface

8086 Interface

A sample E^{2}ROM interface shown for the 8086 (see Figure 16) compares very closely in layout and operation to that for the 8088 (see Figure 14). The 8086 interface accounts for the 16-bit 8086 data bus by latching both bytes of address and implementing a pair of devices to read and write an entire word at a time. E^{2}ROM interface control signals are identical to those for the 8088 interface (see Figure 15).

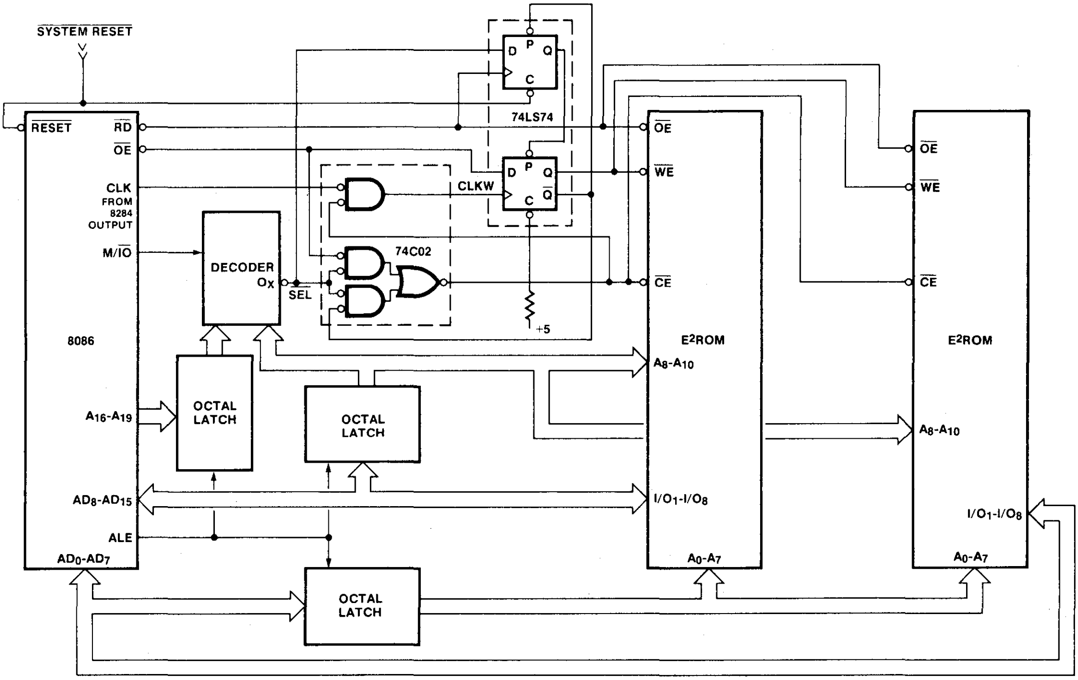


Figure 16. E^2ROM Interface — 8086 (Minimum Mode)

Conclusion

The development in E^2ROM memory is continuing at an ever increasing pace. Recent strides in E^2ROM cost reduction, access time, and availability have made non-volatile memory suitable for more applications than ever before. It is the purpose of this application note to contribute to this evolution in semiconductor memory by assisting the system designer in the task of E^2ROM implementation. Armed with basic hardware and software examples of working E^2ROM applications, the designer can more easily complete a feasible E^2ROM design, using the flexible, cost-effective devices currently offered.

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Memory Products
Application Note

9

SOFTWARE DOWNLINE LOAD USING SEEQ'S CMOS EEPROMS

June 1987

seeq
Technology, Incorporated

Software Downline Load Using SEEQ's CMOS EEPROMS

Introduction

Non-volatile semiconductor memories have been commercially available for some time but these early devices required multiple power supplies, high voltages and were slow in programming. The RAM-like nature of the new Electrically Erasable Read Only Memory (EEPROM) greatly simplifies their use in all areas of microprocessor based design. The elimination of complex timing and voltage requirements makes it attractive to the designer to incorporate in a design an EEPROM such as SEEQ's 28C64 or 28C256. These EEPROMs are self-supporting and as simple to use as a static random access memory. In addition, because of internal control over the write cycle, they can plug into the standard socket of the 8K by 8 bit and 32K by 8 bit static RAM.

These EEPROMs are true non-volatile memories. Non-volatility is provided in the same way as EPROM. Unlike EPROM they can be written to without prior ultra violet light erasure. The byte-write requirements are identical to that of static RAM except that the EEPROM write cycle, once initiated by normal static RAM timing takes as long as 10ms. Once a write operation begins, the EEPROM is self supporting freeing the processor and all external circuitry for other tasks. This is accomplished through latches, as internal self-timing circuit and wave shaping circuitry. It also generates all necessary high-voltage programming pulses. These features fit well in a RAM environment where 5 volts is the only voltage level available. The read timing cycle of the EEPROM is identical to that of a standard EPROM, RAM or ROM.

The early EEPROMs had small storage capability. For this reason, they were not seriously considered as main program storage medium. Therefore, most of the initial EEPROM applications used the EEPROM for limited data storage, such as calibration parameters and system configuration. The use of the EEPROM for main program storage was obviously reserved for those who could afford the cost and the board space required. The availability of the 28C256 EEPROM along with the reduction in cost of lower density devices has created new interest among design engineers. The EEPROM is now considered a cost effective approach to non-volatile main program storage, either by itself or in combination with ROMs and EPROMs. It will operate with the signals normally applied to a RAM, with the only restriction being the worst-case delay of 10ms after starting a write cycle before accessing data.

Device Operation

The internal circuitry of the 28C64 and 28C256 EEPROM does not write entered data bytes immediately to the array of memory cells. The bytes first accumulate in a 64 byte page buffer and subsequently transfer to a specific "page" of the array in an independently timed manner. As a result, up to 64 bytes can be written within one 10 ms write cycle to the EEPROM array.

Each byte can be written to any location within the address space boundary of the currently active page. Because the device ignores the row address input after the first byte write, an attempt to load data bytes beyond this boundary will not affect data elsewhere in the EEPROM array, but will cause the data to be written to the page buffer at a location determined by the lower 6 bits of the address bytes. The procedure to transfer a data byte from the bus to the EEPROM array consists of three steps: the load cycle, the write cycle and the optional data polling.

The load cycle

The load cycle is basically a byte-load window (t_{BLC}) during which a data byte can be entered into a 64 byte page buffer before the write cycle starts. If an additional data byte is entered within the byte-load window the initial window timer is retriggered and the internal write cycle is prevented from commencing. Taking in consideration the t_{WP} min and t_{BLC} min specifications, it will require only 22.4 us to enter a string of 64 bytes into the page buffer. The latest high to low transition of either the Chip Enable signal ($\overline{CE}$) or Write Enable signal ($\overline{WE}$) latches the address bits into the address latches. It also resets the internal page load timer. In order to ensure proper latching and write cycle initiation the $\overline{WE}$ and the $\overline{CE}$ signals must meet t_{WP} min. Upon the earliest low to high transition of either $\overline{CE}$ or $\overline{WE}$ the EEPROM latches the data byte, places it in the page buffer and starts the internal page load timer t_{BLC}.

The write cycle

If no data byte has been loaded within the byte-load window the EEPROM terminates its load cycle and initiates its write cycle. During this write cycle, which takes maximum 10 ms, additional load attempts are ignored. The EEPROM, during these 10 ms, is not on the bus and requires no processor service.

The timing diagram on the 28C64 and 28C256 data sheet shows that it can complete a byte load cycle within 170 ns.

i.e. $(t_{AS}+t_{WP}+t_{DH}) = 20+150+0 = 170$ ns.

The remaining 9.99983 ms of the 10 ms write cycle can be used to execute other system tasks. The write cycle is illustrated in Figure 1.

DATA polling

During the write cycle, the data bus of the EEPROM exhibits high impedance. The write cycle ends when the internal operations are completed, at which time the EEPROM is immediately available for access. A read command will then present true data at the output port. The maximum write cycle time is 10 ms, but typically it takes less time. The 28C64 and 28C256 have a built-in software feature to take advantage of this shorter write cycle.

When the EEPROM, while still in its write cycle, is read anywhere in its address space, the software feature will present at the EEPROM data bus the ones-complement of the data byte at the last address loaded. For example, data byte 10001101 is read as 01110010. With this feature the end of the write cycle can be detected and data loading can immediately be resumed. As a result the processor waiting time is reduced. This polling procedure is illustrated in Figure 2.

Design Considerations

The page mode feature can reduce the overall write-time by a factor equal to the page size. Unfortunately, page sizes as well as timing specifications for EEPROMs vary significantly among manufacturers and may not always match the timing requirements of a particular processor. For instance, a tight byte-load window specification, i.e. t_{BLC} min to t_{BLC} max, might not take full advantage of the page load feature. Consequently, the maximum possible data transfer rate is not obtained. To illustrate this, the specifcations of the most significant EEPROM parameters, as given by different manufacturers, are shown in Figure 3. The byte-load window specification of the SEEQ 28C64 and 28C256 EEPROMs accomodates a large number of processors.

Software examples

Processors with MOVE STRING or LOOP/REPEAT instructions might be able to load a

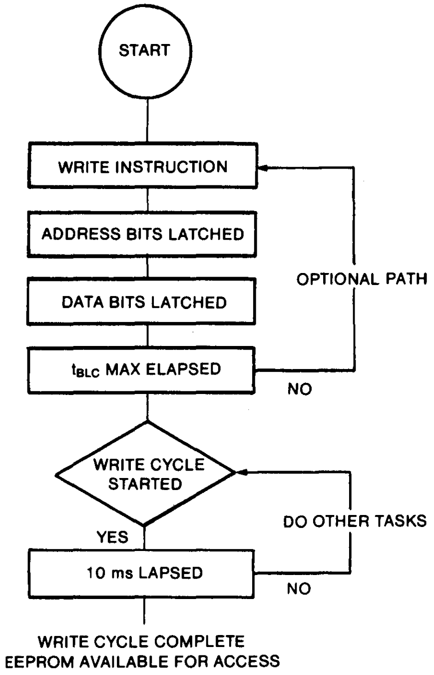


Figure 1. Page Mode EEPROM Write Cycle.

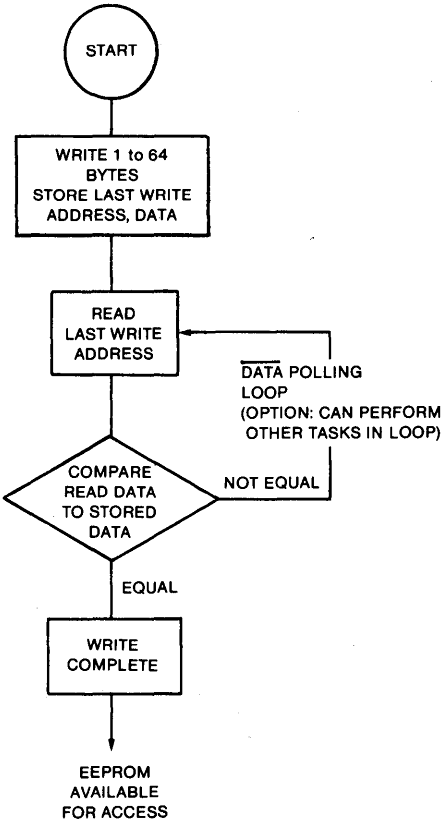


Figure 2. Page Mode Write $\overline{\text{DATA}}$ Polling

Specification Comparison Table for 64K EEPROM

MANUFACTURER	t_{BLC} MIN.	t_{BLC} MAX.	t_{PLW} MIN.	PAGE SIZE
SEEQ*	200 ns	200us	infinite	64 bytes
#1	3 us	20 us	150 us max.	16 bytes
#2	3 us	100 us	infinite	32 bytes
#3	30 us	100 us	infinite	32 bytes
#4	100 us	500 us	infinite	32 bytes

Specification Comparison Table for 256K EEPROM

MANUFACTURER	t_{BLC} MIN.	t_{BLC} MAX.	t_{PLW} MIN.	PAGE SIZE
SEEQ*	200 ns	200us	infinite	64 bytes
#1	2 us	100 us	infinite	64 bytes

*Times are shown for military temperature range devices.

Figure 3.

group of data bytes faster than the EEPROM allows. In that case the data transfer rate of the processor is in conflict with the minimum byte-load-time specification of that EEPROM. The solution to this problem is to emulate the MOVE STRING instruction in assembly code. This approach might cause conflict with the maximum byte-load-time specification.

Example 1, the t_{BLC} min specification

The MOVE BLOCK instruction of the 8086 processor moves data bytes so rapidly that it conflicts with the t_{BLC} min of the EEPROM specification from several manufacturers. The following code instructions illustrate this.

```
DESTADD EQU                       ES:BYTE PTR [DI]
SRADD    EQU                      DS:BYTE PTR [SI]

— — — — — — — — — — — — — —  code instructions to
— — — — — — — — — — — — — —  cause registers to point
— — — — — — — — — — — — — —  to EEPROM address and
— — — — — — — — — — — — — —  data source address.

MOV CX, NDLOAD               ;  load page size
REP  MOVS DESTADD, SRSADD    ;  do page load till CX=0
●
●
●
RET
```

The REP MOVS DESTADD, SRSADD instruction requires 9 clock periods to initiate the byte-move process and 17 clock periods to move each consecutive byte. Consequently, the 8086 driven by a 6 MHz clock can move a byte in 2.83 us. This is in conflict with the minimum value for the t_{BLC} specification of the 64K EEPROM made by manufacturers #1,#2, #3 and #4.

Any solution to this problem would reduce the data transfer rate. SEEQ EEPROMs are much faster and, as the table below illustrates, accommodate these data rates easily.

PROCESSOR	CLOCK RATE	DATA RATE
80186	8 MHz	1.0 us/byte
80286	8 MHz	0.5 us/byte

Figure 4.

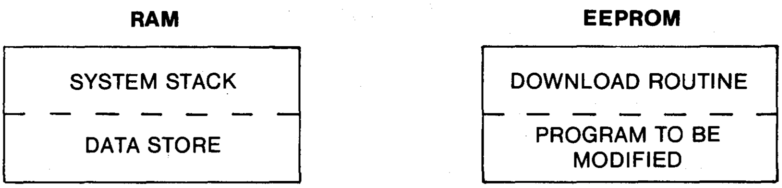


Figure 5.

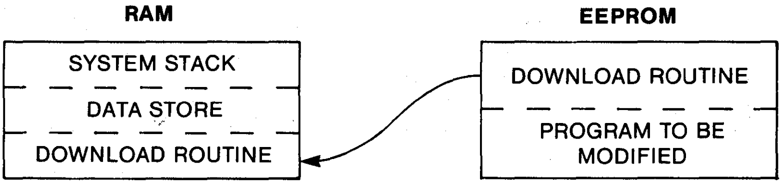


Figure 6.

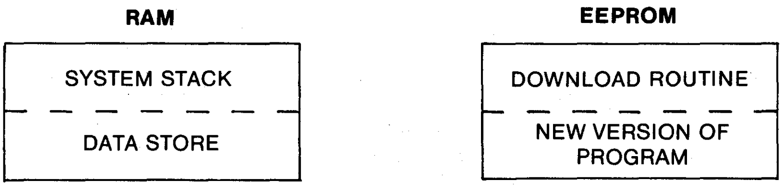


Figure 7.

Example 2, the t_{BLC} max specification

Since the 8051 processor does not have BLOCK MOVE instructions it must emulate a BLOCK MOVE with 13 instructions, each requiring 24 clock periods.

At a clock cycle rate of 12 MHz the data rate is 26 μs per byte. This conflicts with the t_{BLC} max specification of manufacturer #1. Other examples, which violate the specification of manufacturer #1 are shown in the table below.

PROCESSOR	CLOCK RATE	DATA RATE
6805	4 MHz	20 us/byte
6801	4 MHz	36 us/byte

Example 3, the t_{PLW} max specification

EEPROMS from some manufacturers require that all bytes be loaded into the page within a specified maximum time (t_{PLW}). For example, if a processor has a data load rate of 10 μs per byte then this value complies with the t_{BLC} specifications of an EEPROM from manufacturer #1. The t_{PLW} specification of the same EEPROM is 150 μs and therefore, the processor can only load 150/10=15 bytes before the write cycle starts. As a result, the page buffer capacity is not fully utilized, and it takes longer to program the EEPROM.

SEEQ does not specify a limit for t_{PLW}. The total page-load window time is infinitely long assuming the time between byte loads meets t_{BLC} max.

EEPROM Download

The cost of updating software contained in ROM or EPROM in the field is very high. EEPROMs allow the system software to be changed remotely, either through a terminal or a modem link to a main computer. Therefore, the key advantage of the EEPROM is reduced service cost for it allows update of software contained in non-volatile memory, without removing the memory device from the system. These remote software updates are very attractive for updating system software, self-calibration or changing the system configuration or capabilities. Data load rates in excess of 50,000 bits/sec are possible using the page mode feature of SEEQ's 28C256 and 28C64.

EEPROM and resident PROM configuration

In the case of an EEPROM and processor resident bootstrap PROM combination, the actual download routine resides in the PROM as shown in Figure 4. The processor can now fetch instructions from the PROM during the EEPROM write cycle.

All EEPROM configuration

If only EEPROM is used for the program storage and the code to be modified is on a different EEPROM than the one from which the processor is executing then a situation similar to figure 4 exists. A more general approach which allows any EEPROM in the system to be written is the EEPROM and RAM configuration.

EEPROM and RAM configuration

In the case of the EEPROM and RAM configuration, the following approach is required. The procedure starts with the memory contents as shown in Figure 5.

In the first step both the download routine and the system program are stored in EEPROM. Once the system is instructed that the new version of the program is to be downloaded, the system copies the download routine from EEPROM to the RAM. At this point, the memory contents are as shown in Figure 6.

The processor then jumps to the RAM and executes the download routine and loads the new main program in the EEPROM. Next, the processor jumps to the new main program in EEPROM to continue its normal task, leaving the RAM available for other services. Figure 7 shows the final contents of the memory devices.

Applications

EEPROM is the preferred memory device when variable data storage is required. There are three important characteristics associated with EEPROM

1. Data contained within the EEPROM is retained when power is removed.
2. The EEPROM can store sufficient data to accommodate large lookup tables or computer programs.
3. Data in the EEPROM is easily alterable, remotely or locally.

The list below illustrates that EEPROM applications are as various as they are numerous.

- Data lookup tables.
- Smart cards
- Electronic toys
- Terminal configuration (baud rate, data format, parity)
- Measurement instruments
- Digital positioning machinery
- Boot-up storage
- Calibration data
- Traffic control equipment
- Telemetry
- Navigational reference system
- Music synthesizers
- Signal synthesizers
- Radio and TV program control
- Disc Drive Servo
- Robotics
- Data encryption
- Self-modifying code.

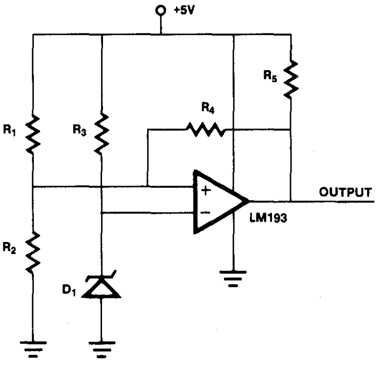
Power-Up/Down with SEEQ's EEPROM

Introduction

Electrically Erasable programmable Read-Only Memories (E^2ROMs) are semiconductor devices offering high-density non-volatile random-access data storage. A read operation with E^2 devices is similar to that for an EPROM or static RAM. The write operation, however, requires a millisecond or longer. Previous generations of E^2ROMs required high-voltage wave-shaped pulses during a write operation. With such strict requirements for the write control signal, the typical E^2 system designer was careful to ensure the correct level of this signal under all conditions, including power-related situations when the system is turned off or on. Only recently has the convenience of E^2ROM been available in devices which can be written with simple TTL-compatible signals. SEEQ offers such devices in several densities.

With the advent of five-volt E^2ROMs, non-volatile memory has shown far greater flexibility and ease of implementation. The ease of use allowed by TTL interfaces cannot release the designer from the normal constraint of ensuring reliable operation during power on/off situations. What signals should the interface devices provide when the system is turned off or on (or otherwise loses power)? Under conditions of extreme or repeated brownouts? During times such as these, when V_{CC} may be outside of specified limits for correct operation of support logic, this support logic can supply signals to the E^2ROM which initiate an undesired write cycle. This causes an inadvertent write to a location in the E^2ROM. In order to ensure system reliability in such situations, it is very important to ensure that inputs (during power up/down conditions) from support devices do not cause inadvertent writes to an E^2ROM device. A certain amount of the required protection is included on-board the E^2ROMs, and is described below. At the system designer's option, system reliability may be enhanced by absolute prevention of false writes.

The purpose of this application note is to provide the system designer with a simple method by which to prevent false writes during power-up and power-down situations. A simple circuit is shown (see Figure 1), its operation is explained, and some useful design considerations are outlined.



R_1 = 63.4 KΩ (1% Metal Film)
R_2 = 71.5 KΩ (1% Metal Film)
R_3 = 51 KΩ
R_4 = 1.5 MΩ (1% Metal Film)
R_5 = 10 KΩ
D_1 = LT1004 - 2.5

Figure 1. E^2ROM Write-Protection Circuit

The ideas and designs presented in this note are meant to serve as a starting point for the designer, to assist him in accomplishing his goal. The solution given, however, is not the only approach. There are many ways to ensure desired signals to the E²ROM during power up/down conditions. The designer is encouraged to tailor his solution to the specific requirements of his application.

Using E²ROM's Built-in Protection

In SEEQ's E²ROMs, protection against false writes has been simplified by 3 built-in protection mechanisms on the chip. This protection logic (transparent to the user) does not make writing any less convenient. Table 1 shows the conditions which are required in order to guarantee initiation of a write cycle V_{CC} must be within specified limits, $\overline{CE}$ must be active low, and $\overline{OE}$ must be V_{IH}, T_{CS} (50 ns) before the falling edge of $\overline{WE}$. Due to E²ROM's protection logic, under certain other conditions, there are modes in which writing is inhibited (see Table 2). First, if V_{CC} is less than 3.0 V, writing is prevented, regardless of the other input signals. Second, $\overline{OUTPUT\ ENABLE}$ ($\overline{OE}$) at V_{IL} (satisfying T_{CS}) inhibits writing. Third, in order to inhibit a write cycle, $\overline{WE}$ or $\overline{CE}$ can be held at V_{IH}.

Several failure modes are prevented by the protection logic described above. For example, if V_{CC} comes up with $\overline{WE}$ already low, this will be interpreted as a continuous low on $\overline{WE}$ and will not initiate a write cycle, because a falling edge on $\overline{WE}$ is required AFTER V_{CC} rises. Inadvertent writes are prevented when V_{CC} is less than 3.0 V (see Table 2); all that is left to external circuitry is write-protection for V_{CC} between the levels of 3.0 V (the lowest V_{CC} level at which the device can write) and the V_{CC} level at which the support logic issues valid signals.

Table 1. Conditions Required to Guarantee Write-Cycle Initiation in E²ROMs

$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{CC}	All Other Pins
	V_{IL}	V_{IH}	4.5 -5.5 V	X

Notes:
1. Active levels shown in above table require T_S set-up time of 50 ns (see E²ROM's data sheet)
2. X = TTL Don't Care.

External Write-Protection Circuitry

With the protection logic on board the E²ROMs, the part can be protected against inadvertent writes in any of several ways. The system designer can ensure that $\overline{CE}$ is high during power-up and power-down. Alternatively, one can ensure that $\overline{WE}$ never has a falling edge during power-up or power-down. For example, one could ensure that $\overline{WE}$ stays at V_{IL} on power-up until a latch is reset, releasing a pull-down. This would ensure write prevention.

Another manner of write protection has been to bring $\overline{OE}$ low during power-up and power-down. This inhibits writing (see Table 2), often allows the simplest realization, and is the general path chosen in this application note. Yet the timing and levels of signals provided must be scrutinized here, as well.

Merely inserting a pull-up on $\overline{OE}$ will tend to pull $\overline{OE}$ down when V_{CC} is low, but may not force a valid V_{IL} level. Inserting a low forward voltage drop diode between the system-wide $\overline{RESET}$ signal and the E²ROM's $\overline{OE}$ signal may work, but depends on the timing of V_{CC} and $\overline{RESET}$.

The specific form of protection against inadvertent write cycles chosen for this application note, one with more certainty of protecting against inadvertent writes, is to force either $\overline{OE}$ low (V_{IL}) or $\overline{CE}$ High (V_{IH}) during power-up and power-down. Figure 1 shows a circuit that can be used to fulfill this requirement.

Table 2. Conditions Required to Inhibit Write-Cycle Initiation in E²ROMs

	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	V_{CC}	All Other Pins
Inhibition Mode 1	V_{IH}	X	X	X	X
Inhibition Mode 2	X	V_{IH}	X	X	X
Inhibition Mode 3	X	X	V_{IL}	X	X
Inhibition Mode 4	X	X	X	Under 3.0 V	X

Notes:
1. Active levels shown in above table require T_S set-up time of 50 ns (see E²ROM's data sheet)
2. X = TTL Don't Care.

The circuit shown in Figure 1 provides a proper output signal (comparator's output) to prevent false write. During power-up, as is shown in Figure 2A, the output of the comparator is kept low from the time that V_{CC} is 2.5 V until it reaches 4.8 volts. The output switches to V_{IH} when V_{CC} goes above 4.8 volts. During power-down, however, as is shown in Figure 2B, the comparator's output is forced low as soon as V_{CC} falls below 4.6 V and is kept low until V_{CC} goes below 2.5 volts. Circuit functionality is not guaranteed below this point.

To prevent inadvertent writes, either $\overline{OE}$ or $\overline{CE}$ pin can be used. The first method is by forcing and keeping $\overline{OE}$ low (V_{IL}) when V_{CC} is below 4.5 volts. This can be done, as is shown in Figure 3A, by connecting comparator's output directly to E^{2}ROM's $\overline{OE}$ pin. As soon as V_{CC} falls below 4.6 V, the $\overline{OE}$ is forced low preventing any internal write initiation. This pin is kept low (valid) until V_{CC} goes below 2.5 volts. Internal protection circuitry protects the part beyond this point (activated when V_{CC} falls below 3.0 V).

The second method of protecting the part against inadvertent write is by forcing and keeping $\overline{CE}$ high when V_{CC} is below 4.5 and above 2.5 volts. This can be done, as is shown in Figure 3B, by NAND gating (74HCT00) the comparator's output with a CS signal. The output of the NAND gate, which is connected to E^{2}ROM's $\overline{CE}$ pin, is controlled by the CS input when V_{CC} is above 4.6 volts. The other input controls NAND gate's output when V_{CC} is below 4.6 V (above 2.5 V). Keep in mind that the CS line must be a high true signal and the NAND gate should be a high speed CMOS device.

Either method described above can be used for protection against inadvertent writes. System designers have to determine their need first and based upon that, select one of the above circuits or one of their own.

Circuit Operation

The circuit shown in Figure 1 is designed to provide a high (V_{IH}) output (comparator's output) when V_{CC} is above 4.8 volts and a low (V_{IL}) output when V_{CC} falls below 4.6 V (above 2.5 V). This is done by using a comparator (LM193 available from National Semiconductor), a temperature compensated voltage reference device (LT1004MH-2.5 available from Linear Technology) and a few resistors. The circuit has been designed to operate over military temperature range.

As it can be seen in Figure 1, the negative input of the comparator is connected to ground through a temperature compensated voltage reference device (D_1) and to V_{CC} through a resistor (R_3). As long as

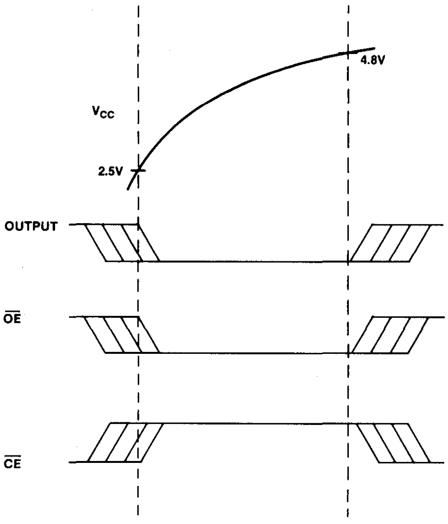


Figure 2A. Timing Diagram—Power-Up Using Either $\overline{CE}$ or $\overline{OE}$ Protection

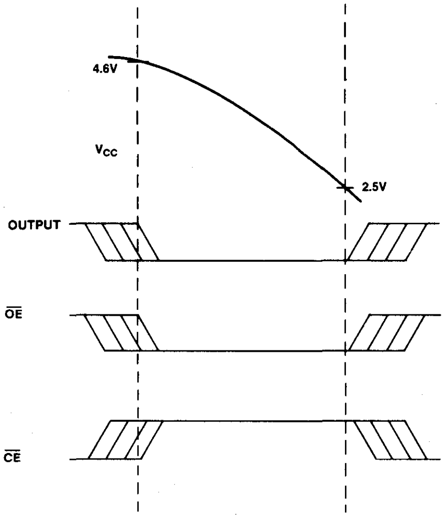


Figure 2B. Timing Diagram—Power-Down Using Either $\overline{CE}$ or $\overline{OE}$ Protection

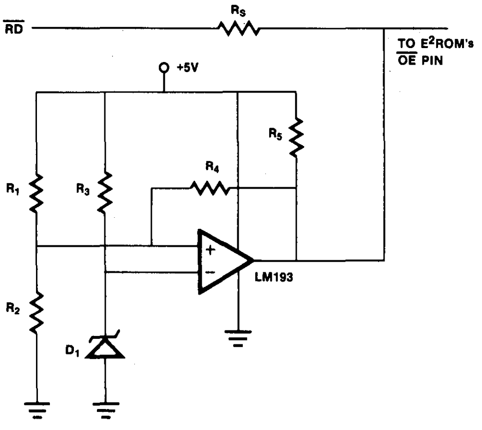


Figure 3A. $\overline{\text{OE}}$ Protection Circuit

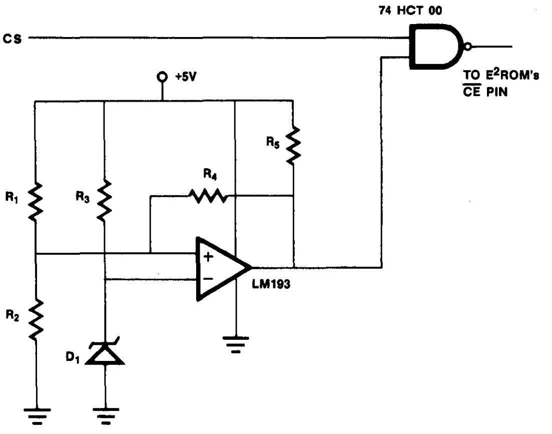


Figure 3B. $\overline{\text{CE}}$ Protection Circuit

V_{CC} is below 2.5 V, D_1 is not conducting (no current flow through it). However, as soon as V_{CC} goes above 2.5 V and stays there, D_1 conducts providing a 2.5 V reference voltage at the negative input (no current flow into negative input). The resistor (R_3) is used to limit the amount of current through D_1.

The positive input on the other hand, is connected to a voltage divider (R_1 & R_2) as well as the output (through R_4). The voltage at this input forces the output to go either high (V_{IH}) or low (V_{IL}). When V_{CC} is below 4.6 V, the voltage divider causes this input to be below reference voltage with respect to ground forcing the output low. On the other hand, when V_{CC} goes above 4.8 V, the positive input voltage goes above reference voltage forcing the output high. The output stays high as long as V_{CC} is above 4.8 volts. The feedback resistor (R_4) is used to enforce output voltage on the positive input while R_5 is used as a pull-up resistor. Proper device selection, as is recommended in this Application Note, can insure correct operation of the circuit over military temperature range.

System Consideration

As was mentioned above, correct circuit operation requires proper device selection. The comparator and temperature compensated voltage reference device (D_1) selections are critical. You have to be sure that D_1 provides 2.5 V drop across allowing half a volt safety margin between external protection circuit and the internal one (3.0 V internal power protection). It is suggested to use devices recommended in this Application Note. Other circuit elements that can influence circuit operation are the resistors. For correct operation over temperature, it is recommended to use 1% metal film resistor for R_1, R_2 and R_4. The other two can be carbon film resistors.

If $\overline{\text{CE}}$ pin is used for protection, the comparator's output must be NAND gated with a CS signal. Proper gate output is guaranteed if a high speed CMOS gate is used. Also, designers have to make sure that the CS input is a high true signal. However, no NAND gate is needed if $\overline{\text{OE}}$ pin is used to protect the part against false write. Comparator's output can be connected to $\overline{\text{OE}}$ (through R_S). A choice of values for R_S Resistor depends on $\overline{\text{OE}}$ driver (RD line). The R_S resistor is used to insure a low $\overline{\text{OE}}$ input when V_{CC} is below 4.6 V (comparator's output is low). If open collector driver is used, the pull-up resistor can replace R_S.

Conclusion

It has always been important for a system designer to ensure reliability as his system is turned off and on. Currently, the importance of this area of design is increasing. As the usage of five-volt E²ROMs increases, applications are expanding into environments where V_{CC} may be undependable, power glitches may exist, and in general a system must be more fault-tolerant. With the circuit contained in this application note, the designer can more easily ensure that his system meets applicable specifications and is able to utilize the convenience of E²ROMs.

Memory Products
Application Note

11

POWER FAIL PROTECTION WITH SEEQ'S CMOS EEPROMS

October 1987

Power Fail Protection With Seeq's CMOS EEPROMS

Since 1982, SEEQ Technology Inc. has been producing EEPROMs that can be programmed in-circuit using only a 5 volt supply. All of the high voltages necessary for programming are generated by an on-chip charge pump. Therefore, the external signals required to initiate a write need only be at TTL levels. Unfortunately, these external signals can do unpredictable things during power-up or power-down. If during these power transitions (or during a brown-out), the signals needed to initiate a write to the EEPROM are generated, the system's non-volatile memory may be corrupted.

Several methods of insuring the integrity of a system's data have been proposed, and these methods are often referred to as "write protection". The two major classifications of write-protection are "software write-protection" and "hardware write-protection".

SOFTWARE WRITE-PROTECTION

Software write-protection involves the use of decoders and latches which need to be written to by the system processor in a specific manner. This "unlock code" sequence must be executed before the EEPROM's control signals can become valid, allowing a write into the EEPROM. These latches and decoders can be on the EEPROM die itself or part of the external circuitry.

The idea is that during power-ups and power-downs the chances of the proper sequence of signals needed to program the EE being generated randomly are very slim. While this is true, there are some limitations to this technique which need to be discussed:

1. Since the unlock code used must be resident somewhere in the system's software, a "run-away" processor could easily execute the unlock sequence, causing false writes. The only way to prevent this from happening during power-up or power-down is by generating a system reset signal via a low voltage detector. How to prevent this during "normal" processor operations is beyond the scope of this article.
2. What happens if power fails after the system has executed a legitimate unlock sequence to perform a desired write? In this case, the EEPROM is vulnerable to false writes on power down unless some form of low voltage detector disables the EEPROM.
3. If power fails during the EEPROM's internal programming cycle (while new data is actually being written into the memory array), data may be corrupted.

Obviously, software write-protection has some limitations which can only be overcome through the use of external hardware.

HARDWARE WRITE-PROTECTION

Hardware write-protection is just that; the use of hardware to eliminate false writes. Much of this circuitry is contained onboard the EEPROM itself. Absolute protection against false writes is thus accomplished with the addition of some external hardware (which we have seen is needed even if software write-protection is used). An additional benefit of hardware write-protect is that it is totally transparent to the system's software designer.

For these reasons, the remainder of this article will address the various aspects of hardware protection.

SEEQ'S ON-CHIP WRITE-PROTECT CIRCUITRY

A. Bandgap Reference Voltage

Internal to all of SEEQ's CMOS EEPROMS is a bandgap voltage level detector. This detector disables the EEPROM whenever V_{CC} is below the WRITE INHIBIT VOLTAGE, V_{Wi}. Characterization data (see figure 1) has shown V_{Wi} to be between 3.85 volts and 4.25 volts over the entire military temperature range. When V_{CC} is below V_{Wi}, two things will be true:

1. The internal charge pump is disabled, preventing the high voltages which are necessary for programming the EEPROM from being generated. It is impossible for any data to be altered when the charge pump is disabled.
2. The EEPROM's internal oscillator is disabled, forcing the device into a low-power standby mode. This feature results in an orderly shutdown of the device when the system's power fails or is turned off. Also, this feature will save power in an all CMOS system where a low V_{CC} standby mode is used.

Since SEEQ's EEPROMs are guaranteed to be disabled when V_{CC} is below 3.85 volts, but TTL signals are only valid when V_{CC} is above 4.5 volts, some external circuitry must disable the EEPROM (and probably hold the system in reset) while V_{CC} is between 3.85 volts and 4.5 volts. In a CMOS system, logic signals are valid with V_{CC} as low as 3.0 volts, which is well below the V_{Wi} threshold of the EEPROM. It would seem then that an external voltage detector might not be needed in a CMOS system. We will see that this assumption may not be valid.

On power-up, this assumption would be valid because the EEPROM would be idle and disabled until well after the system's bus had settled down into valid logic levels. Unfortunately, if power is lost while the EEPROM is in the midst of an internal programming cycle, the data being programmed may be stored incorrectly.

Of course, with the orderly shutdown feature of SEEQ's EEPROMs, and because the page address is latched into the device upon the first falling edge of WE, only those locations being changed when power was lost might be corrupted. All other locations will remain unchanged. Also, if the system processor was doing a page load on SEEQ's EEPROMs and V_{CC} was to drop below 3.85 volts before the T_{blc} Timer timed out (see data sheet), then that programming cycle would never start and no locations would be changed.

Fortunately, there is a way to eliminate the possibility of having the EEPROM in an internal programming cycle, while allowing one final data store, when V_{CC} fails. This is accomplished by detecting a drop in the raw DC or AC voltage used to power the system (see Figure 2). As long as C_f is large enough, which is load

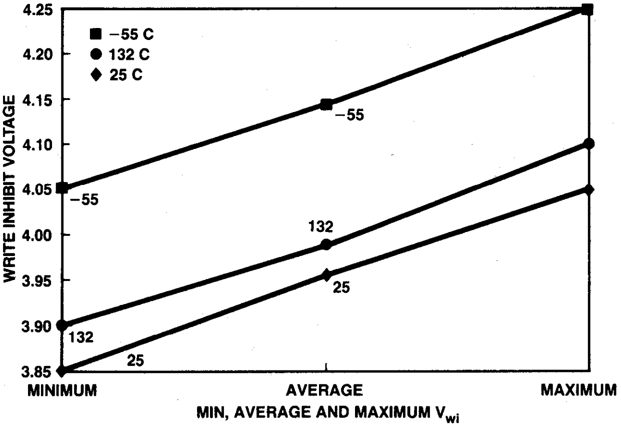


Figure 1. WRITE INHIBIT VOLTAGE—28C256 AND 28C64

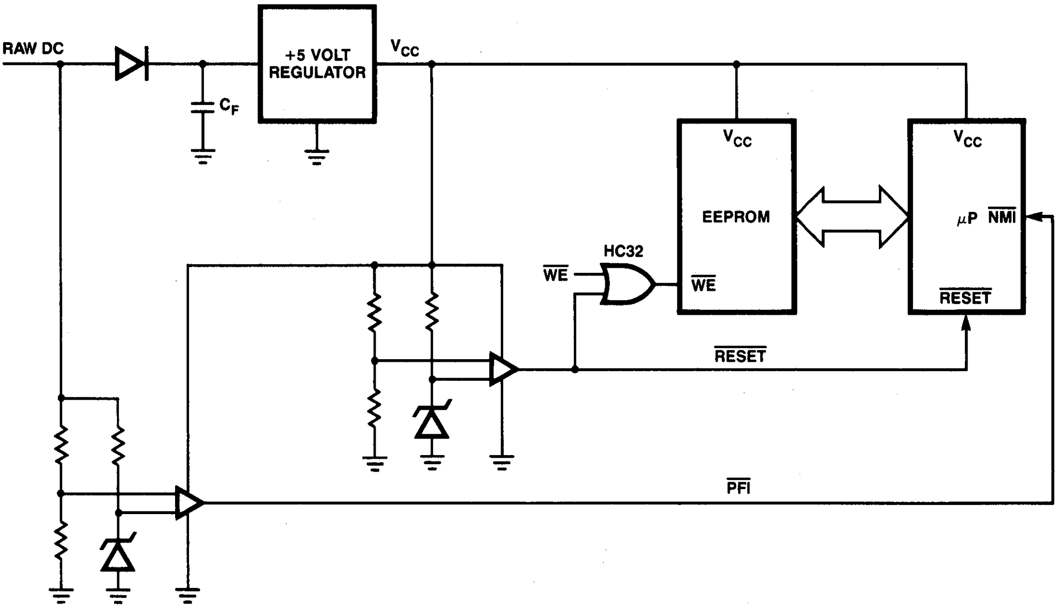


Figure 2.

dependent, a POWER FAILURE IMMINENT (PFI) signal can be generated at least 10 ms before V_{CC} fails.

This PFI signal can then be used to warn the system processor that there is time for only one more programming cycle before shut-down. Up to 64 bytes of data can be stored in one 10 ms programming cycle and return to its standby mode before V_{CC} fails. The final store is accomplished, and all data is intact.

Now we must turn our attention to disabling the EEPROM when V_{CC} is between 3.8 volts and 4.5 volts.

B. Multiple Control Pins

There are three control signals on SEEQ's EEPROMs, and each signal must be at the proper logic level for a write cycle to begin. Therefore, writes can be inhibited if any of the following input conditions are met:

CE	WE	OE	V_{CC}	WRITE MODE
V_{IH}	X	X	X	INHIBITED
X	V_{IH}	X	X	INHIBITED
X	X	V_{IL}	X	INHIBITED
X	X	X	BELOW V_{WI}	INHIBITED

1. $3.8 < V_{wi} < 4.25$
2. X – Don't Care
3. All other inputs are don't care
4. Set-up and hold times on transition are in the specific data sheets for each part.

By using an HCMOS logic gate and a RESET signal (see figure 2) we can force any one of the control lines to a known state to disable the EEPROM when V_{CC} is below 4.5 volts. We could also use the RESET signal to remove power from the device, which will accomplish the same thing. An HCMOS gate should be used since it will drive the control line to either power rail even with V_{CC} as low as 3.0 volts.

Why must we have a separate RESET line? Why not use the PFI line to disable the EEPROM? Well, that would allow the EEPROM time to finish an internal programming cycle before V_{CC} fails, but there are several problems with this approach.

First, during power-up, the unregulated voltage could be above threshold (enabling the EEPROM) some time before V_{CC} has reached 4.5 volts. This could lead to false writes. Second, if the EEPROM is disabled as soon as an imminent power failure is detected, the system would be unable to initiate any final programming cycles prior to shut-down. This could lead to the loss of valuable data.

From this, we can see that the EEPROM disable signal must be generated from a low voltage detector on the V_{CC} line. This disable signal would be the system's normal RESET line (see figure 2).

EXTERNAL WRITE-PROTECT CIRCUITRY (SEE FIGURE 2)

In this circuit, the RESET signal will disable the EEPROM and hold the µP in RESET any time V_{CC} is below 4.5 volts (or whatever other threshold is chosen). This will prevent any false writes from occuring during power-up. However, the RESET line will only prevent false writes during power-down if the EEPROM was not already in an internal programming cycle. If this does happen, only those bytes which were being reprogrammed could possibly be corrupted.

The PFI signal will prevent this from happening, as well as allowing the system enough time to save any vital data prior to power failure. By

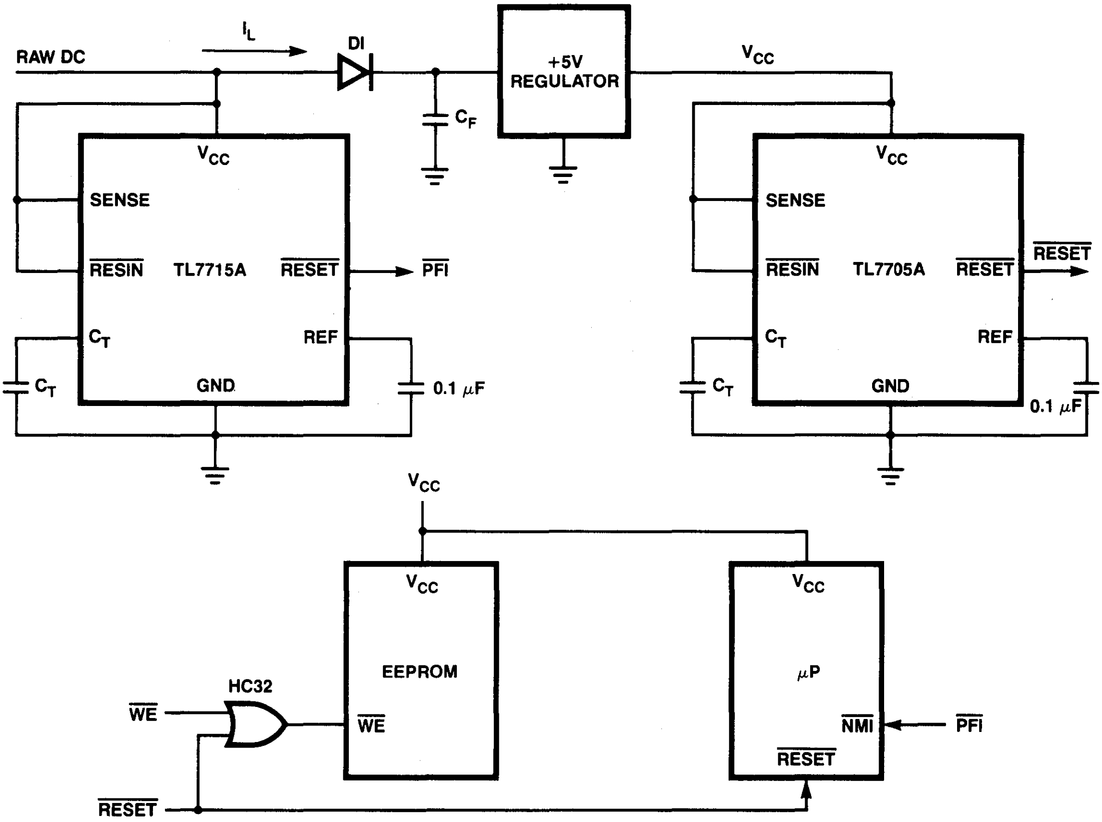


Figure 3.

making C_f large enough (which is load dependent), PFI will warn the μP 10 ms before V_{CC} fails. After being warned, the μP can initiate one more programming cycle. The EEPROM will then have enough time to complete its internal programming cycle before it is disabled.

In conclusion, the possibility of false writes can be totally eliminated if the system makes use of a RESET signal and a PFI signal in combination with SEEQ's on-board write-protection circuitry.

A MONOLITHIC SOLUTION (SEE FIGURE 3)

An alternative to using op-amps and discrete components to produce the PFI and RESET signals can be seen in Figure 3. This circuit makes use of a monolithic supply voltage supervisor family from TEXAS INSTRUMENTS. These devices are useful to detect power-up, power-down, and brown-outs. In addition, C_t can be chosen to determine how long the RESET signals will remain active after V_{CC} is above threshold, which guarantees proper system initialization on power-up. The reader should refer to T.I.'s data sheet for details.

In this example, a TL7715 is used to produce PFI while a TL7705 is used to generate the RESET signal. This arrangement ensures that the EEPROM is disabled anytime V_{CC} is below 4.5 volts, and the PFI warning is issued anytime the raw DC powering the system falls below 13.2 volts. (See TL7705 and TL7715 data sheets for details).

Lets assume that:

a. power is lost abruptly

b. V_f of D1 is 0.7 volts

c. The drop-out voltage of the regulator is 2.0 volts

Then we can see that the voltage across C_f must take at least 10 ms to drop from 12.5 volts to 7.0 volts at the given load, I_l. ($13.2 - 0.7 = 12.5$ and $5.0 + 2.0 = 7.0$). Since $I_l = C_f\ dv/dt$ and $dv = 5.5$ volts, $dt = 10$ms, we have this relationship: $I_l = 550\ C_f$.

In other words, if I_l is 550 mA, then C_f must be 1000 μF for proper operation of the PFI protection.

CONCLUSION

Designers must be careful to avoid false writes to a system's EEPROM during power-up, power-down, and brown-outs. This is especially true in CMOS systems where "brown-outs" are often entered purposely to achieve low V_{CC}/low power standby states.

We have seen that to completely eliminate the possibility of false writes, the system must monitor the voltages on both sides of the V_{CC} regulator. This is true whether software or hardware write-protection is used.

SEEQ Technology has incorporated all of the on-chip hardware write-protection needed to design a trouble-free system using EEPROMS. In addition, this form of write-protection is completely transparent to the system, making the software interface more convenient.

Memory Products Application Note

24

EEPROM AS A SUBSTITUTE FOR BUBBLE MEMORY

October 1987

APP. NOTES

seeq
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As more systems designers are dropping bubbles, EEPROM—based designs are rapidly increasing. In the early to mid 80's, we were told bubbles would take over mass storage designs. Surely bubbles were the design of the future for core memories and even to replace disc memories. As many of these dreams fade, let us consider some of the pro's and con's of each technology.

Common design considerations include density, power consumption, weight, access time, data rate, and environmental susceptability.

Density is certainly one issue that gets a lot of discussion. Commonly available 4 megabit bubble packs are approximately 1.25 cubic inches for the basic block. SEEQ Technology's 256K PLCC package has a volume of approximately .0125 cubic inches or 1% of the volume of the bubble pack. Therefore, an equivalent 4 megabit EE memory using 16 256Kbit devices has less than 20% of the volume of the bubble memory. Mounting of either device was not taken into consideration; neither was the volume of the required support chips. The EEPROMs would take more area mounted than was implied strictly with a volume specification. Spacing between packages could increase total volume, although the ratio between EE and bubble would still be substantial. Additionally, the high profile of a bubble memory device would greatly increase overall board volume as boards cannot be spaced closer together than the tallest component height. Decoding of a 4 megabit EEPROM array can be done with a simple one-of-sixteen decoder such as the 74LS154. In comparison, that 1.25 cubic inch bubble pack required a series of controllers, coil drivers, current drivers, etc. In the final analysis, semiconductor EEPROM memory will occupy a fraction of the space of bubble memories.

Access time is the time from the issuance of the valid address or name of a file, datablock, word or byte until the first full size segment of data is available. A full size segment would be the first bit of a serial data stream or the first full byte or word in a parallel data bank. Common 4 megabit bubble memories today have average random access times on the order of 50 to 90 milliseconds. Some of the new small size modules have average access times less than 10ms, but specify maximums above 500ms. SEEQ Technology's 28C256 has a maximum access time of 250 nanoseconds. Comparing the two technologies, bubble memory's average access time is 200,000 times longer than the EEPROMs worst case; the EEPROMs could deliver 200,000 bytes of data while the bubble memory is accessing the first bit.

FIGURE 1
COMPARISON CHART
BUBBLES TO EEPROMs

	BUBBLE	EEPROM	RATIO	REMARKS
Power Consumption	5	.5	10/1	Considerable current would be drawn by bubble memory support circuitry
Access Time in microseconds	50,000	.25	200,000/1	
Average Data Rate (Read) K Bits/Second	125	32,000	1/256	
Data Rate (Write) K Bits/Second	125	800	1/6.5	4 Megabit bubble and sixteen 256K EEPROMs/ shown in fig. 3
Weight (Grams)	75	5	15/1	
1 Megabit Volume (Unit only) Cubic Inches	1.25	.2	6/1	Does not include bubble support chips

Weight is one area that seldom becomes an issue in most designs but does come up on occasion. Once again, the comparison is not straight forward. Basic bubble memory devices commonly have weights in the vicinity of 75 grams per 1 megabit device. This, of course, does not take the weight of support circuitry into consideration. The equivalent EEPROM bank of four 256K devices would have an approximate weight of 5 grams. With the bubble memory support devices also taken into consideration, the ratio would significantly surpass this 15 to 1 ratio.

Power consumption almost always warrants some consideration. Four megabit bubbles have power supply requirements around 4 watts typical and greater than 5 watts maximum. Sixteen (16) of the 256K type EEPROMs and a one-of-sixteen decoder under worst case conditions would draw less than 100 ma at 5 volts. This would be one-half watt or about 10 percent of the power of a bubble memory. While the sixteen 256K's only require a single decoding chip for support, the bubble requires numerous support chips. This support draws power too. To get a realistic feel for bubble power consumption, it becomes necessary to examine then at the board level where the host of necessary support devices are installed.

The boards considered for comparison were not expandable, that is to say they were fully stuffed, 4 megabit boards. Power consumption on these boards runs between 10 and 20 watts. Additionally, there were multiple power supplies required, not the single 5 volt supply required by the EEPROMs.

Data rate is the speed at which the data can be continuously delivered to the addressing device. In this area the bubble is specified at maximum (burst) and average. Burst data rates can be fast as 200,000 bits per second. Average data rates can be on the order of 125,000 bits per second. Making the EE comparison, data rates are the same as access times, and therefore 250 nanoseconds per byte (8 bits). Putting this in perspective, after the bubble has taken 88 milliseconds to get started (initial access time), while the bubble is fetching 256 bytes the EEPROM could deliver 65,536 bytes.

Data rate does not imply direction. This is to say that data rate does not apply only to reads of data but also to data writes. For a bubble memory, read and write data rates are equal, but the rates differ when EEPROMs are used. Read data rates were discussed above. Write data rates in EEPROMs are a bit more complex. In high density EEPROMs, byte write times and page write times are the same. A "page" is 64 consecutive bytes of data. This page of data can be loaded as fast as 350 nanoseconds per byte, thus a page load would take 22.4 microseconds. After this time, a maximum of 10 milliseconds is required for the write cycle to complete.

The microprocessor's write data process must halt during this 10 milliseconds until the device is again ready to load another page and begin the 10 millisecond write sequence again. This would imply a write data rate of 350 nanoseconds per byte "burst-mode" with a maximum of 64 bytes or an over all rate of 6400 bytes per second. This 6400 bytes per second rate is comprised of one hundred 10 millisecond write sequences of 64 bytes. While 6400 bytes per second (this would be 51.2K bits per second) is about half the speed of the bubble's write data rate it can be improved many fold for systems using multiple EE Devices.

In the case of medium to large arrays, which would be the case in mass storage applications, the common approach is to decode chip selects from the high-order address inputs (see figures 2 and 3). But positioning the chip select decoder in the address space immediately above the page address inputs would allow each consecutive device to store the next logical page.

Applying this approach to a 4 megabit array, system addresses A_0 to A_5 would go directly to A_0 to A_5 inputs of the EEPROMs. For an array of 16 E^2 devices, requiring 4 address inputs to select the 16 devices, system addresses $A_6 - A_9$ would go to a 4 to 16 decoder network, providing the 16 chip selects required. System address A_{10} would go to address A_6, system address A_{11} to address A_7, continuining thru system address A_{18} to address A_{14}. The 10 msec write cycle would continue independently in each device while the system was continuing to write logically consecutive pages in the other devices. This makes the page size 1024 bytes, thus the system should stop writing and wait for the write cycle to complete after 1024 sequential bytes had been written.

For a 4 megabit array (sixteen 256K EEPROMs), this design approach would produce a data rate in write mode of greater than 100,000 bytes per second or 6½ times the bubble's write data rate.

Temperature sensitivity is often a major design consideration. This is very true for military, industrial and space applications. These designs often require operation or at least storage down to −55 degree C and as high as 125 degree C. Bubble memories have problems at temperature extremes and often specify their minimum temperature for operation a few degrees above 0 C. This does not comply with standard commercial grade temperature ranges and falls far short of either military or industrial grade temperature ranges. Similar problems exist at high temperature. We commonly see maximum temperature for operation between +30 degree C and +50 degree C. Even the +50 degree C falls for short of the commercial temperature specification of +70 degree C. Needless to say both military and industrial temperature ranges are completely missed. EEPROMs operate over the entire commercial, industrial and military temperature ranges.

Clearly, EEPROMs share the intrinsic nonvolatility of bubble memories without the disadvantages in speed, power consumption and temperature range. Figure 1 compares the important attributes of the two technologies. Complete technical information is contained in Seeq's 28C256 datasheet.

NORMAL CHIP SELECT DECODE

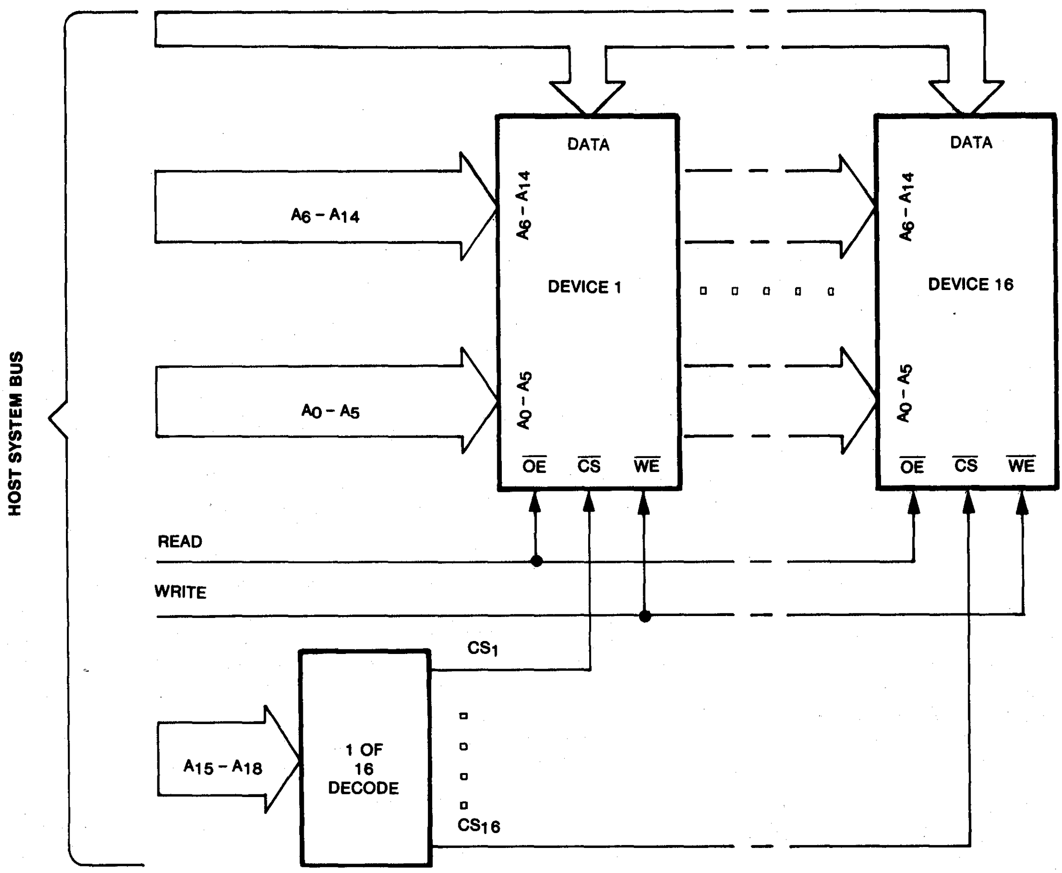


Figure 2.

DECODING METHOD TO ENHANCE WRITE CYCLE DATA RATE

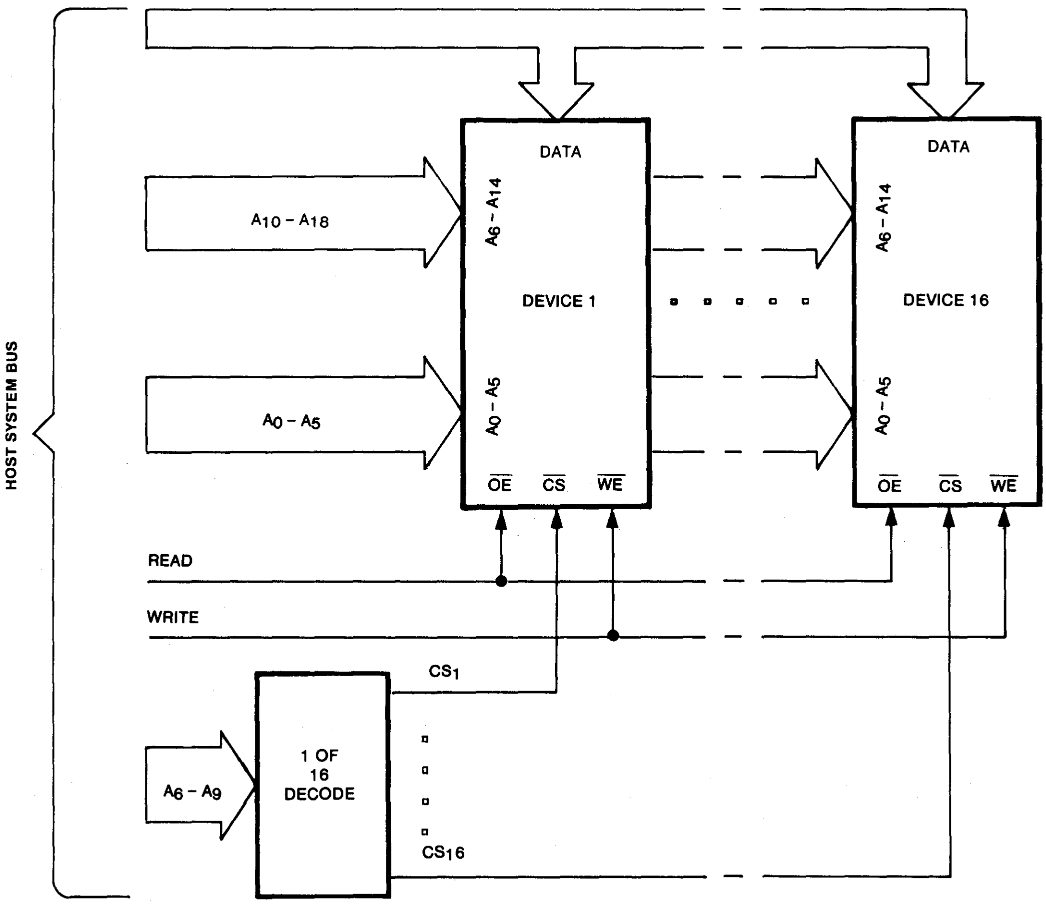


Figure 3.

27

USING HIGH SPEED CMOS EEPROMS WITH HIGH PERFORMANCE MICROPROCESSORS.

October 1987

seeq
Technology, Incorporated

Using High Speed CMOS EEPROMs with High Performance Microprocessors.

Satisfying ever increasing demands on microprocessor throughout can be achieved in several ways, the simplest of which is to increase system clock frequency. However, this technique yields higher performance only if the remainder of the system is capable of operating at the higher rate. Memory devices on the system must be able to respond to the accelerated transfer rate to avoid insertion of wait states. Speeding up clock rates without decreasing access times will generally cause the microprocessor to wait faster. The 38C16 and 38C32 high speed CMOS EEPROMs from SEEQ technology are designed to satisfy the performance requirements of high performance microprocessors.

The 38C16 and 38C32 are 2K x 8 and 4K x 8 bit CMOS EEPROMs manufactured using SEEQ's advanced 1.25 micron CMOS process. Seeq's proprietary oxynitride process and patented differential Q cell™ design give the parts fast access times and high endurance. The 38C16/32 are ideal for high speed applications requiring nonvolatility and in-system reprogrammability. Both commercial and military temperature range products are available.

Device Features:

Read Operation:

38C16 and 38C32 are available in access times ranging from 35 ns to 70 ns. The operational mode table is shown in Table 1. Read operation for the devices is similar to any standard memory device. Chip enable access times are faster than address access times (see data sheet) which can be a significant advantage in high speed microprocessor designs.

38C16/32 OPERATIONAL MODES

MODE PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	HI Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X V_{IH} X V_{IL}	X X V_{IL} V_{IL}	V_{IH} X V_{IH} V_{IL}	HI Z/D_{OUT} HI Z HI Z/D_{OUT} No Operation (HI Z)

X: Any TTL level

Table 1.

Q Cell is a trademark of SEEQ Technology, Inc.

Write Operation:

The write operation is similar to static RAM. Because of the fast address and data latches, the write data latch cycle is as fast as a read cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever occurs last and data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever occurs first. After the data is latched the built-in timer completes the non-volatile write cycle within a maximum time of 5 ms. A typical device has a write cycle time faster than the maximum specified 5 ms. The 38C16/32 feature $\overline{\text{DATA}}$ polling to enable the user to optimize write time. During the internal write cycle, the complement of bit 7 of the data byte written is presented at the output I/O_7 when a read is performed. Once the write cycle is completed, true data is presented at the outputs. A software 'polling' routine (see fig. 1) can be used to determine write cycle completion. The data bit 7 polling cycle specifications are the same as a read operation. During data polling, the addresses are a don't care.

Write data protection:

38C16 and 38C32 provide protection against false write during powerup/down using on chip circuitry. Writing is prevented under any one of the following conditions:

1. When V_{CC} is below write inhibit voltage V_{WI}.
2. A high to low write enable transition has not occured when V_{CC} is between V_{WI} and V_{CC} min.
3. $\overline{WE}$, $\overline{CE}$ or $\overline{OE}$ are in TTL logical states other than those specified for byte write in the mode table (Table 1).

38C16 and 38C32 feature an on-board bandgap voltage level detector. The detector disables the EEPROM write circuitry whenever V_{CC} falls below write inhibit voltage V_{WI}. The internal charge pump (voltage multiplier) is disabled, preventing the high voltages which are necessary for the programming cycle from being generated. It is impossible for data corruption to occur when the charge pump is disabled. Seeq's EEPROMs are guaranteed to be write disabled when V_{CC} falls below write inhibit voltage V_{WI}. V_{WI} is between 3.8 to 4.25 V over the military temperature range.

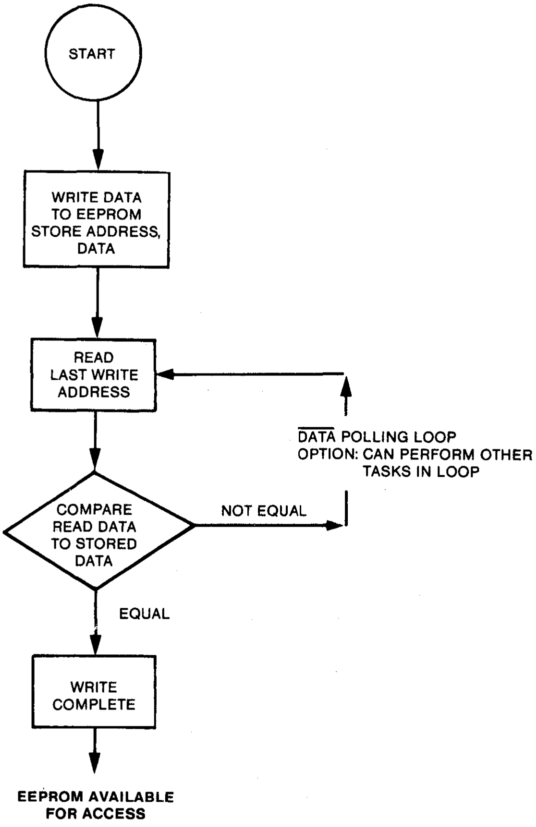


Figure 1. BYTE WRITE WITH $\overline{\text{DATA}}$ POLLING.

Since present day systems employ a mixmatch of both TTL and CMOS components, it is recommended that external hardware write protection circuitry be used in addition to the on-board protection circuitry just described. This is needed to eliminates false writes when V_{CC} is between 3.8 to 4.5 V (see Application Note 11). Absolute protection from false writes can be thus achieved while having the added benefit of being totally transparent to the system software.

System Interface examples:

MIL-STD-1750A is the U.S. Air Force's instruction set for 16-bit microprocessors embedded in avionic weapon systems. This standard is also used by the Navy, Army and NATO. Typical 1750A applications involve real-time avionic applications in systems incorporated into aircraft, missiles and even ships or ground vehicles. The standard specifies the microprocessor architecture and instruction set. Also defined are two memory addressing modes, a standard mode of

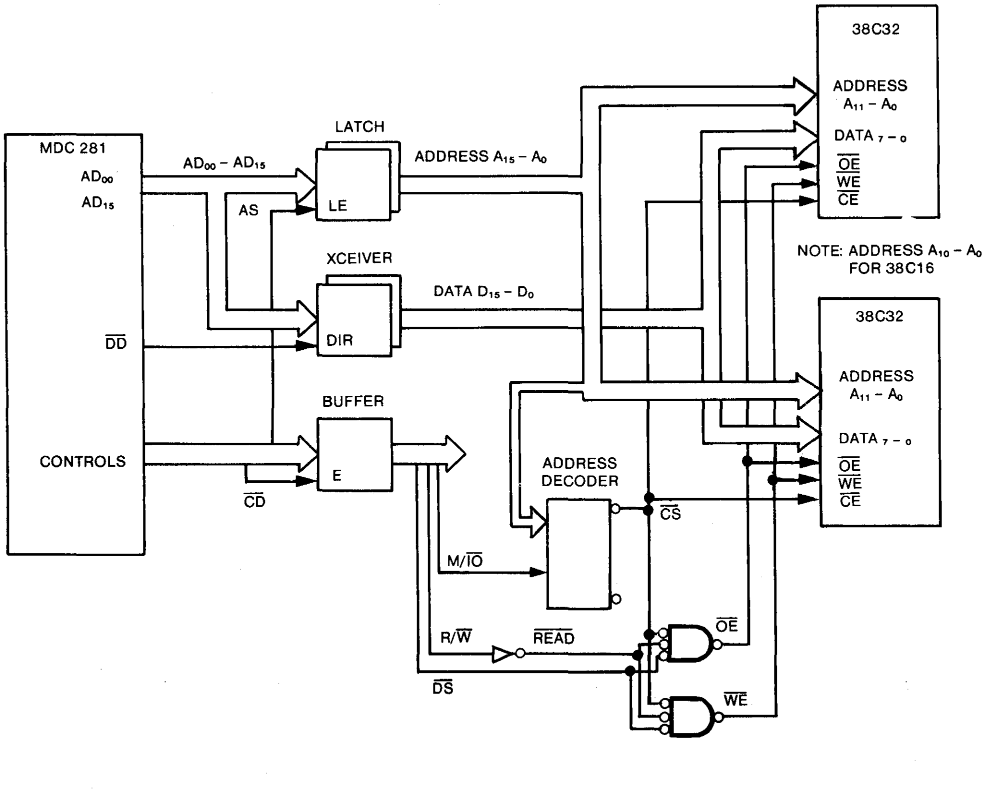


Figure 2. MDC281 INTERFACE TO 38C16/32

64K-word direct addressing and an optional expansion mode of 1-Mword direct addressing. The latter mode is segmented into 256 blocks of 4K-words each. The 38C16 and 38C32 offer an excellent fit for 1750A processors and give system designers/programmers a wider array of choices to come up with the next generation of flexible and more powerful adaptive systems.

MDC281 MIL-STD-1750A CPU Module:

The McDonnell Douglas MDC281 is a certified MIL-STD-1750A (Notice 1) 16-bit CPU consisting of three custom CMOS/SOS LSI chips MDC17501 (Execution unit), MDC 17502 (Control unit) and MDC 17503 (Interrupt unit) mounted on and interconnected within a ceramic substrate. The MDC281 CPU is designed for military avionics applications like sensor data processing, operation and control of weapons systems. The CPU is particularly suitable for embedded applications requiring less than 64K-words of memory.

38C16/32 Interface:

A typical MDC281 interface to 38C16/32 memory is shown in fig 2. 38C16-70 or 38C32-70 with a maximum address access time of 70 ns can be used without wait states in the memory subsystem for a 20 MHZ MDC281. For a complete description of pin assignments and signal functions refer to the MDC281 data sheet. Each machine cycle consists of a minimum of 5 OSC periods. The synchronization clock ($\overline{SYNC}$) output high to low transition signals the start of a new machine cycle and is used as the timing reference. $\overline{SYNC}$ low indicates that address is on the AD bus. The AD bus is a bidirectional multiplexed Address and Data bus (AD_{00} – AD_{15}). This bus is shared between the external system and the internal module resources and hence to avoid bus contention, the AD bus must be isolated from the external system using a bidirectional transceiver. Data Direction signal $\overline{DD}$ is used for transceiver direction control. $\overline{DD}$ low indicates read transfer, while high indicates a write transfer. High to Low transition of the address strobe AS is used to latch Address into a transparent latch during AD bus de-multiplexing.

All transfers between the module and the memory are referenced to the AS and $\overline{DS}$ bus control signals and are characterized by IN/$\overline{OP}$ low and M/$\overline{IO}$, $\overline{CD}$ high. Control Direction signal $\overline{CD}$ is used to control direction of the control signal transceiver. This signal goes high to indicate that the module is driving the AS, $\overline{DS}$, M/$\overline{IO}$, RD/$\overline{WR}$ and IN/$\overline{OP}$ signals.

Read Operation:

Read transfers begin with address being placed on the AD bus immediately following $\overline{SYNC}$ high to low transition. This address is assured to be valid for the cycle by latching it in a transparent latch on the high to low transition of AS. The $\overline{DD}$ signal is high during this portion of the transfer. RD/$\overline{W}$ indicates direction of transfer. During read (fig. 3) the AD bus drivers are placed in a high impedance state at the low to high transition of $\overline{SYNC}$ to give the memory access to the bus. Next $\overline{DS}$ signal goes low and is used by the memory system to generate output enable ($\overline{OE}$). $\overline{DD}$ also goes low shortly after $\overline{DS}$ goes low and this signal reverses the direction of the AD bus transceivers. The memory then pulls $\overline{RDY}$ low to conclude the transfer. Read data from the 38C16/32 is latched into the module on the $\overline{SYNC}$ high to low transition.

Write Operation:

Write is indicated by RD/$\overline{W}$ going low (fig. 4). The address is replaced by data when $\overline{SYNC}$ transitions from low to high. Next, the $\overline{DS}$ signal goes low and is used by the memory system to generate $\overline{WE}$. Data is valid at the low to high transition of $\overline{DS}$ and is latched into the 38C16/32. $\overline{DD}$ stays high for the duration of a write transfer. The memory system pulls $\overline{RDY}$ low to conclude the transfer.

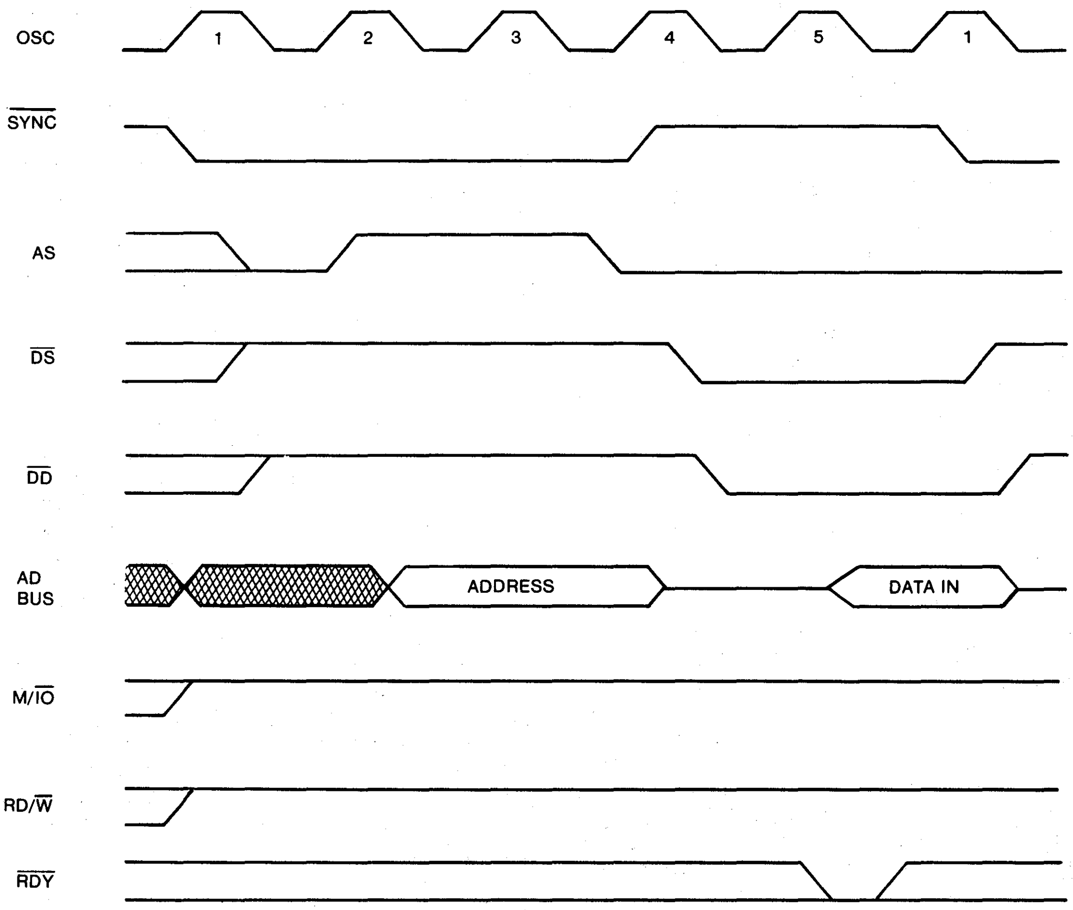


Figure 3. MDC281 READ CYCLE

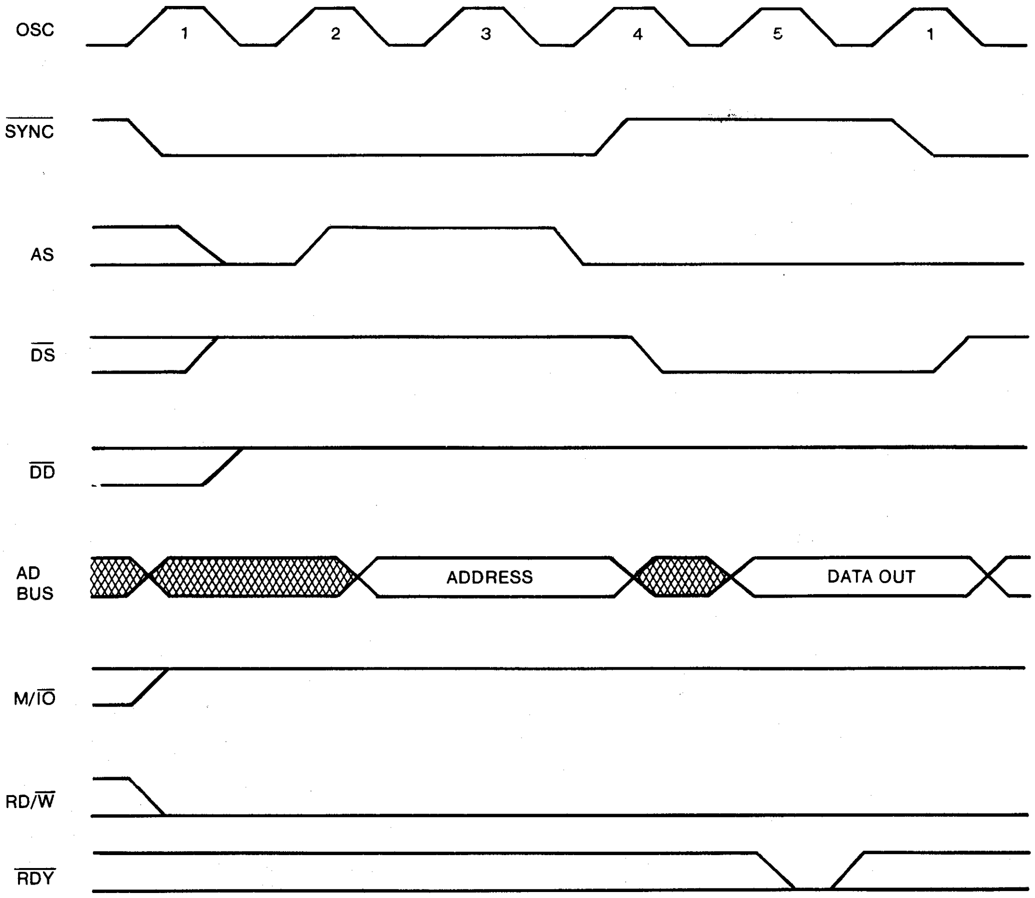


Figure 4. MDC281 WRITE CYCLE

Fairchild 9450:

Fairchild 9450 is single chip solution implementing the complete MIL-STD 1750A instruction set architecture (ISA) and its floating point standard. It allows addressing of up to 2M words of memory and with the addition of the F9451 Memory management unit (MMU), up to 16M words of memory.

38C16/32 Interface:

A typical minimal configuration 38C16/32 memory subsystem interface is shown in fig. 5. The 20 MHz F9450 provides for a 90 ns memory access time without wait states. Hence, 38C16-70 or 38C32-70 with a maximum address access time of 70 ns can be used in the memory subsystem. Bus cycles are a minimum of 4 or 5 states long. Memory and $\overline{\text{I/O}}$ cycles are identical and the status of the M/$\overline{\text{IO}}$ line distinguishes the two cycles. State S_0 is used for bus acquisition. This state is followed by S_1 state. After the start of S_1 state, the CPU outputs the address after a delay. At the end of S_1, RDYA input is sampled. If RDYA is low the CPU stays in S_1, extending the address phase of the bus cycle. Otherwise, it proceeds to states S_2 followed by S_3.

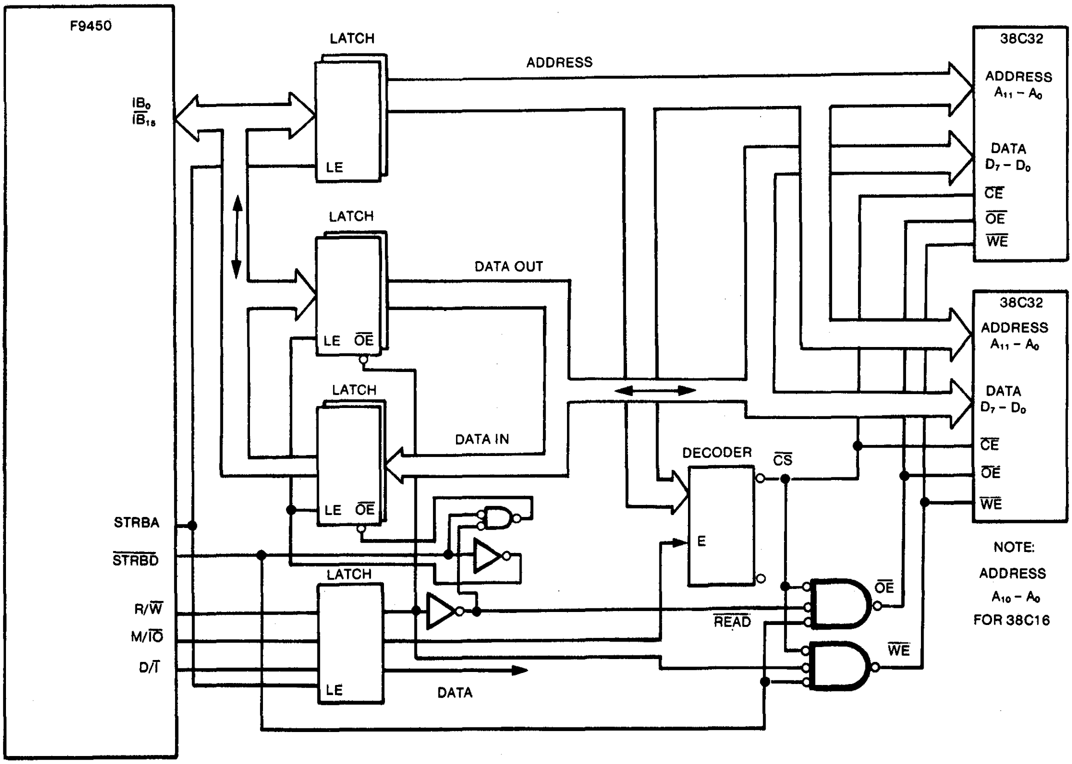


Figure 5. F9450 MEMORY INTERFACE

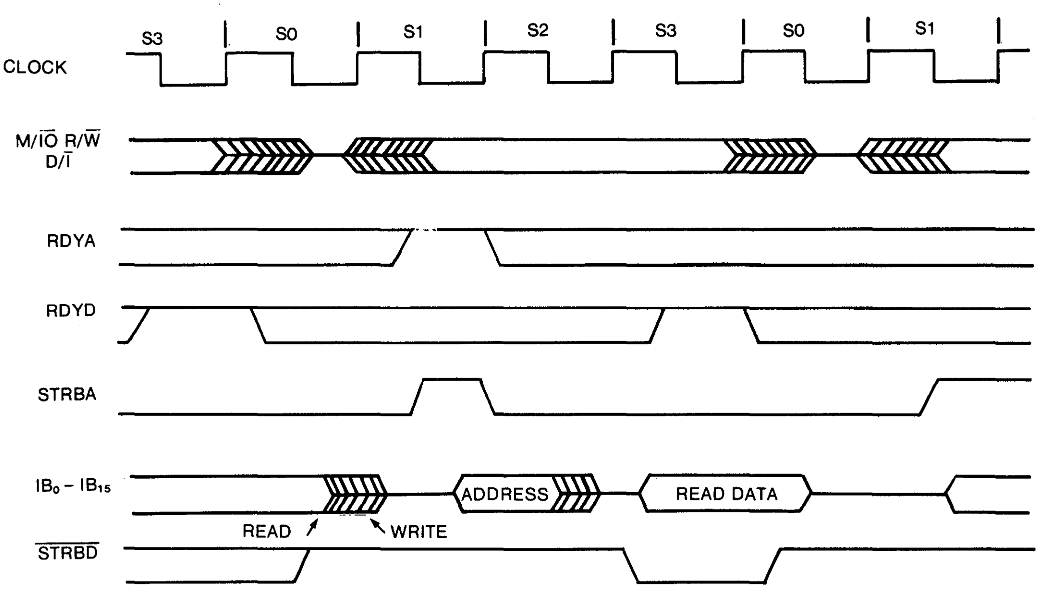


Figure 6. F9450 READ CYCLE

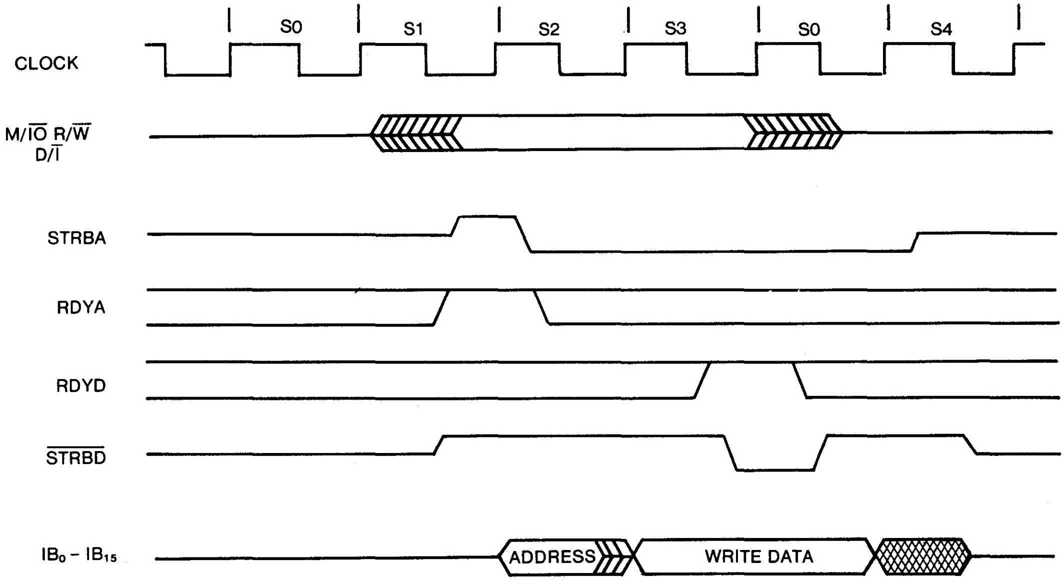


Figure 7. F9450 WRITE CYCLE

Read Operation:

STRBA signal is pulled low in state S_2 (fig. 6). The high to low transition of this signal is used to latch the memory address. The CPU the pulls $\overline{\text{STRBD}}$ output low and prepares to receive read data from 38C16/32 by turning the address/data bus around. $\overline{\text{STRBD}}$ is used to enable data from the memory.

Write Operation:

During write cycles the CPU starts driving the bus with the write data immediately after the address (fig. 7). $\overline{\text{STRBD}}$ signal is activated during S_3, allowing enough write data setup time to $\overline{\text{STRBD}}$ falling edge and hold time for the rising edge of $\overline{\text{STRBD}}$ to write data. At the end of S_3 RDYD is sampled, and if low, state S_3 is continued extending the data phase. If the signal is sampled high the write cycle is terminated.

Software Considerations:

Examples of hardware interface of MIL-STD-1750A microprocessors to 38C16/32 have been shown. 38C16/32 have a built-in timer to control the internal non-volatile write cycle The parts feature an automatic erase before write. The write cycle takes a maximum of 5ms/byte. System software has to take into account this byte write time of the EEPROM. The system writes to the EEPROM and then follows the write with a polling routine as shown in fig. 1 to determine the end of the EEPROM internal write cycle. If the system application demands that the 5ms write time be utilized usefully, the technique shown in fig. 8 can be used. The on-board timers A or B can be used. These timers can be used to timeout the 5ms write time of the EEPROM and programmed to interrupt the CPU. The CPU can thus carry out other tasks while the internal write cycle of the EEPROM is in progress.

DSP Applications:

Present day DSP processors are finding a wide range of applications like Encryption/Decryption, voice-band, precision servo control, pattern recognition, adaptive control and intelligent filtering. Most of today's applications use ROM or EPROM based memories to store algorithms and as a result use is restricted to applications that utilize fixed algorithms and co-efficients. Adaptive algorithms must use RAM, thus forcing the processor to repeat its adaption sequence each time power is turned on. Seeq's high speed CMOS EEPROMs 38C16 and 38C32 present an excellent fit for many of today's DSP processors and open the door for system designers and programmers.

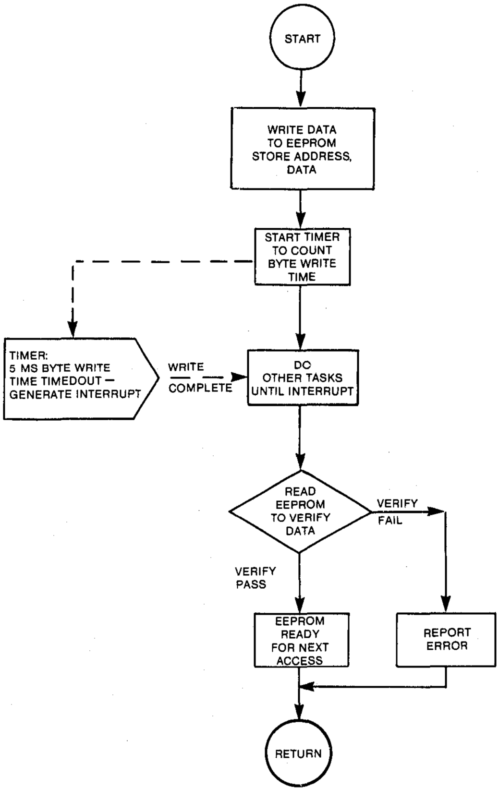


Figure 8. EEPROM BYTE WRITE SEQUENCE USING SOFTWARE CONTROLLED TIMER

TMS320C25:

The TMS320C25 is a high performance digital signal processor featuring a single accumulator and a Harvard type architecture in which program and data are implemented in separate address spaces. The processor features on-chip data RAM of 544 words, on-chip program ROM of 4K words and supports direct addressing of up to 64K words of external program memory and 64K words of external data memory. An on-chip serial port provides direct communication capabilities with serial devices.

For protyping, system expansion, external memories may be required. The 38C16/32 can be used as program memory and offer the ability to implement adaptive algorithms because of their reprogrammability.

38C16/32 Memory Interface:

The TMS320C25 distinguishes between program memory and data memory spaces using $\overline{PS}$ and $\overline{DS}$ signals. For a detailed description of pin assignments and their functions refer to the 320C25 data sheet. The crystal or external clock source is divided internally by the 320C25 to produce a four phase clock. All bus activity is referenced to the four-phase clock. The interface discussed here is for a TMS320C25 running at 40 MHz. Fig. 9 shows 38C32-35 used as program memory. The 35ns maximum address time of the 38C32 satisfies the memory performance requirements of the 320C25.

External Read Cycle:

During the beginning of machine cycle (fig. 10) clock quarter-phase1, the 320C25 begins driving the address bus and one of the memory space select signals $\overline{PS}$ or $\overline{DS}$. R/$\overline{W}$ is driven high to indicate a read cycle. At the beginning of quarter phase2, $\overline{STRB}$ goes low to indicate valid address. $\overline{STRB}$ is used with R/$\overline{W}$ to state memory read enable signal. After decoding the address, the memory system must set up READY during quarter-phase2. READY is sampled by the 320C25 at the beginning of quarter-phase3. If READY is sampled high, read data from the memory is clocked in at the end of quarter-phase3. Ready can be pulled high permanently, if the system components used do not require wait states. At the beginning of quarter-phase4 $\overline{STRB}$ is deasserted. The read cycle is terminated with the de-activation of the address bus and $\overline{PS}$, $\overline{DS}$. Care must be taken to avoid bus conflicts when a read cycle is followed by a write cycle. The 38C32 has a 15ns max disable time and hence will not cause bus conflict.

External Write Cycle:

The external write cycle is similar to the read cycle described above, with the following differences: R/$\overline{W}$ is driven low indicate an external memory write. $\overline{STRB}$ is used with R/$\overline{W}$ to gate write enable signal. Write data is placed on the bus at the start of quarter-phase2. $\overline{STRB}$ is deasserted at the beginning of quarter-phase4 and the write cycle ends with the de-activation of address bus and $\overline{PS}$, $\overline{DS}$. As before, care must be taken to avoid bus conflict when a write cycle is followed by a read cycle. Since $\overline{STRB}$ is used to enable the 38C32, potential bus conflict is avoided.

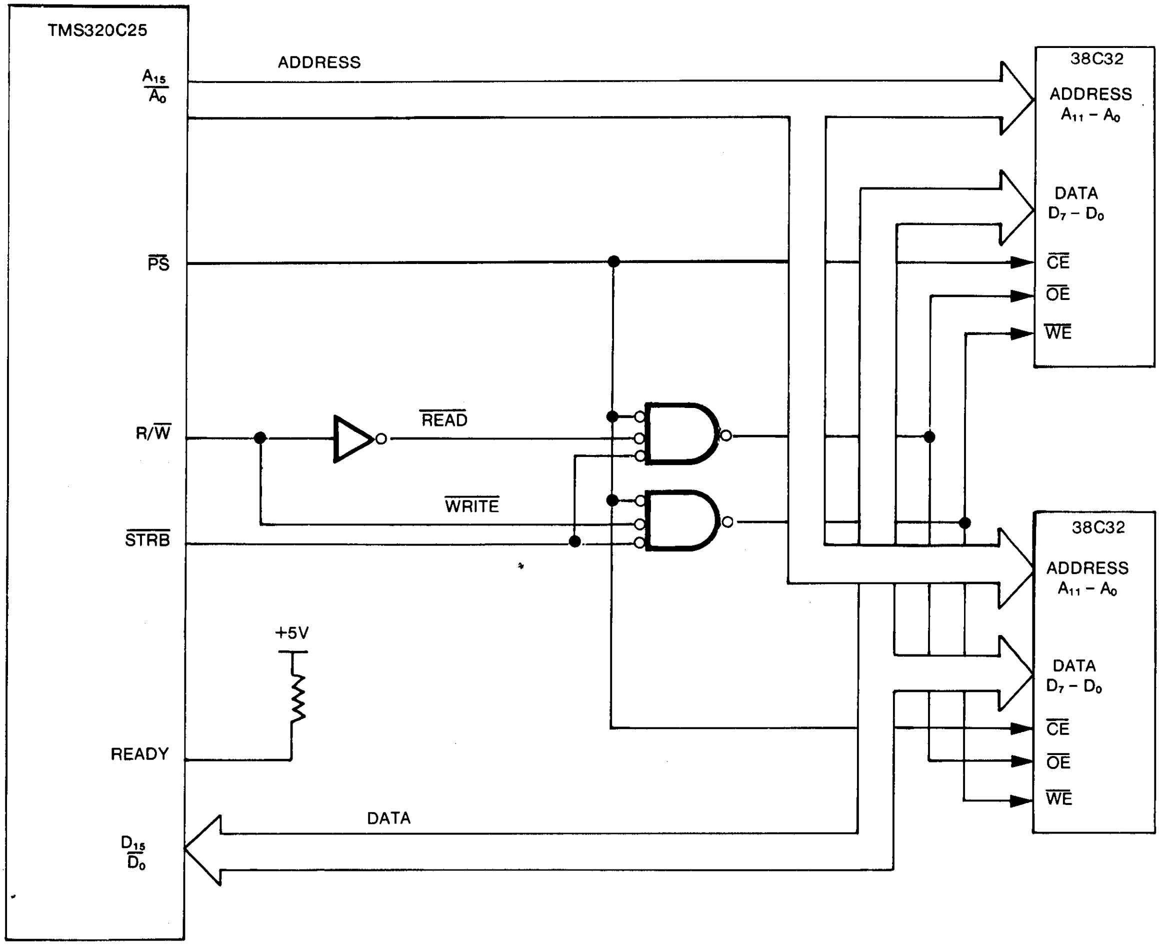


Figure 9. TMS320C25 MINIMAL EXTERNAL MEMORY INTERFACE

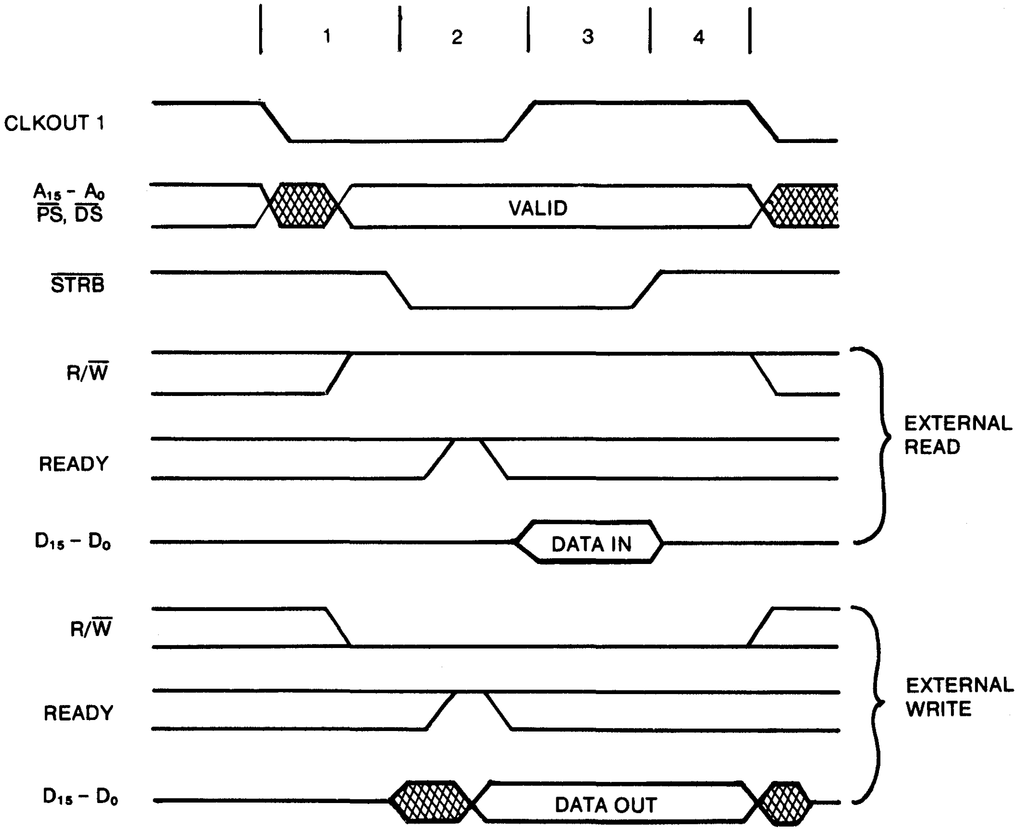


Figure 10. TMS320C25 READ AND WRITE CYCLES

Software Considerations:

When 38C16 or 38C32 are used as program memory, the system can take advantage of the easy reprogrammability of these devices. Code or Program coefficients can be easily altered to implement adaptive systems. The 38C16/32 byte write time of 5ms max should be accommodated by the system software (fig. 11). The on-chip timer can be utilized to timeout the byte write time. A timer interrupt is generated every time the timer decrements to zero. The period register (PRD) can be used if necessary, so that interrupts can be programmed to occur at regular intervals.

Using the 38C16/32, remote down-load capabilities can be provided to the system using the on-chip serial port. Object code can be downloaded into RAM at high speed and then written into the EEPROMs from the RAM. Typical DSP algorithm implementations need up to 4K words of program space. Using the 38C16 or 38C32 only two packages are required thus minimizing package count.

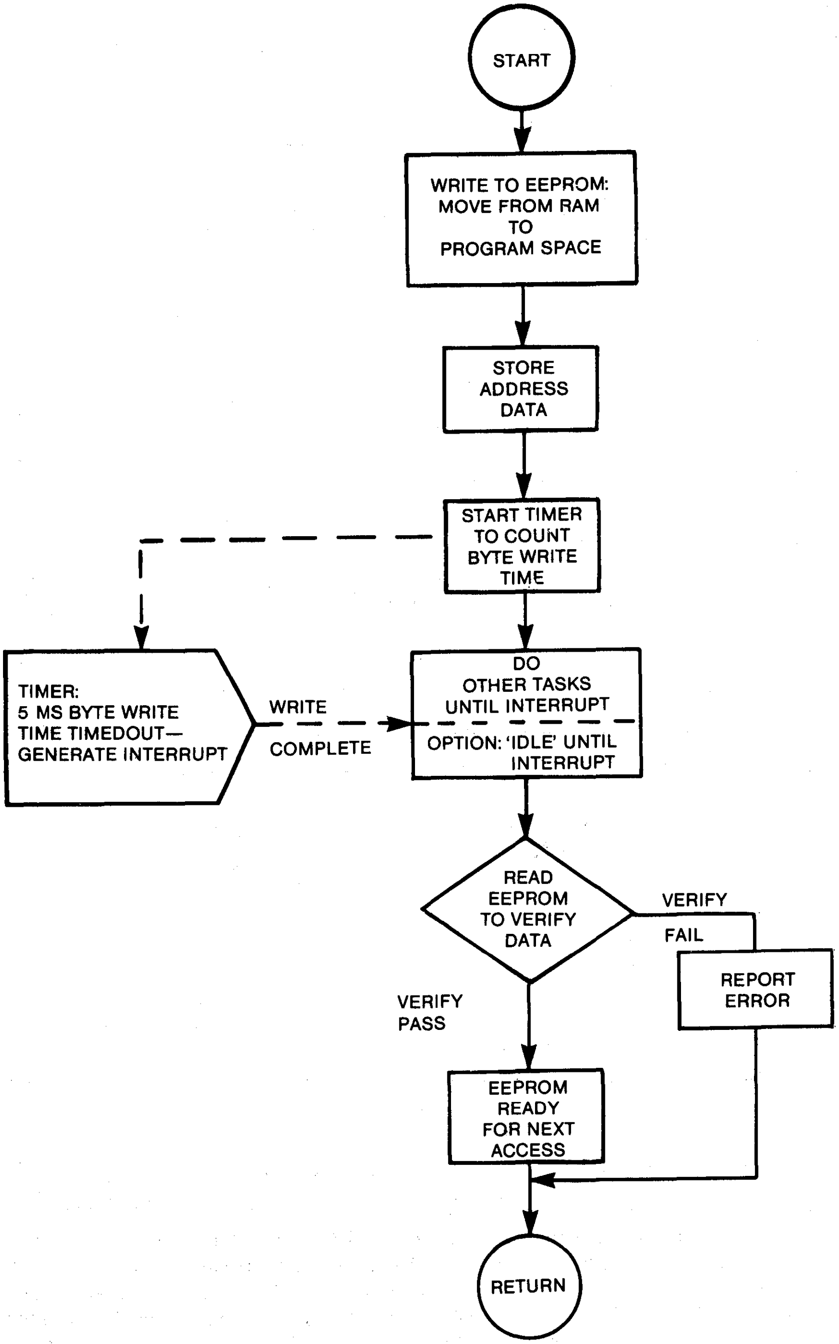


Figure 11. TMS320C25 WRITE SEQUENCE FOR 38C16/32 EEPROM WRITE.

Communications Products Application Brief

28

EEPLD's INTERFACE IBM PC BUS WITH THE EDLC® 8003

August 1988

APP. NOTES

seeq
Technology, Incorporated

Ethernet/Cheapernet Controller Design

PC/AT personal computers can be networked together via 10 Megabit per second Ethernet/Cheapernet IEEE 802.3 CSMA/CD protocol using the SEEQ 8003 Ethernet Datalink Controller (EDLC®) and the SEEQ 8020 Manchester Code Converter (MCC™). As the PC Bus data rate is typically one byte per microsecond and interrupt latency may be hundreds of microseconds, a FIFO buffer memory is required to capture Ethernet data frames which can come at any time. In this application brief, the FIFO buffer consists of an economical industry standard 8K byte static RAM together with SEEQ EEPLD20RA10Z electrically erasable programmable array logic devices. The EEPLD devices provide handshake/arbitration control logic between the FIFO, EDLC and PC Bus. Additionally, the EEPLD devices provide the memory address decode logic from the PC Bus. A system block diagram for the Ethernet Controller is shown in Figure 1.

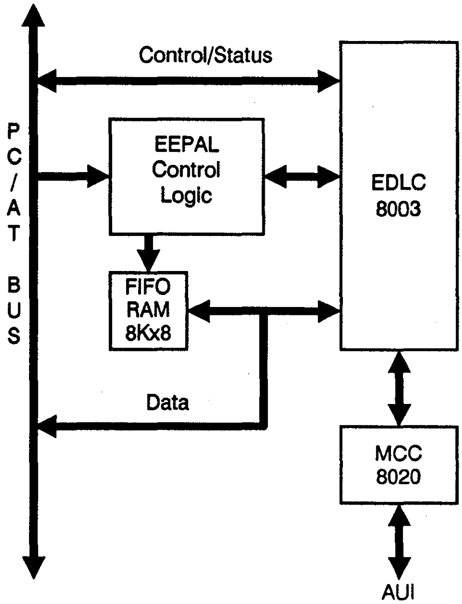


Figure 1. Ethernet Controller System

FIFO RAM Buffer

The FIFO RAM buffer is divided into four 2K byte sections as shown in Figure 2. Incoming Ethernet data frames range from 60 to 1514 bytes which are loaded into the RAM at locations 0, 2048, 4096, and then back around to 0. The PC must unload these frames before the fourth frame overwrites the first frame. More frames could, of course, be buffered by increasing the RAM size to, say, 32K bytes. The PC is aware of the location of the frames by keeping count of the EDLC Receive End of Frame interrupts or by closely watching the status of incoming frames in the EDLC Receive Status Register.

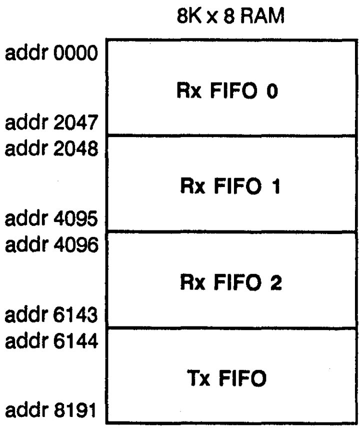


Figure 2. FIFO RAM Partitioning

Rx Counter

The FIFO RAM address is supplied by the RX Counter (EEPLD) during EDLC receive data transfers. This counter is reset to 0 on PC IO Write Command "ResetRxCounter". It is incremented on EDLC RxRD unless RxTxEOF in which case it is advanced to the next 2K boundary (0 if address greater than 4K) .

Tx Counter

The FIFO RAM address is supplied by the Tx Counter (EEPLD) during EDLC transmit data transfers. This counter is loaded by the PC with

EDLC is a registered trademark of SEEQ Technology, Inc.
MCC is a trademark of SEEQ Technology, Inc.

address 8191 minus the frame byte count. It is incremented on EDLC TxWR. On arriving at the terminal count, 8191, an RxTxEOF signal is supplied to the EDLC, signaling the end of the frame.

The Tx Counter is used by the PC to read out Receive frames. Simultaneously, the Rx counter may be receiving a new frame while the current frame is being transferred to the PC. Care must be taken in the software design to assure that a transmit frame is completed before using the Tx counter for an Rx read out. The Tx Counter is incremented automatically when the PC IOR read signal executes a read byte.

PC Bus Decode

EEPLD devices decode the PC Bus Address, IO Read, and IO Write signals to provide PC access to the EDLC 8003, FIFO RAM, Rx Counter, Tx Counter, and miscellaneous controls such as reset, TxMode and LoopBack.

Bus Transceivers

Data bytes are transferred to and from the PC, FIFO RAM, and EDLC 8003 on the Data D0..D7 bus via Transceiver 74LS245 and are controlled by EEPLD signals DIR1 and G1. Control/Status bytes are transferred to and from the PC and EDLC 8003 on the CMMD D0..D7 bus via Transceiver 74LS245 and are controlled by EEPLD signals DIR2 and G2.

Attachment Unit Interface, AUI

The Ethernet Controller Design provides a physical data link between the PC and the AUI interface. The six AUI signals Rx+, Rx-, COLL+, COLL-, Tx+, and Tx- will drive up to 50 meters twisted pair transmission line to another Controller as demonstrated by this application brief or to a Media Attachment Unit (MAU) for communication over single wire coax Standard Ethernet cable. The addition of a transceiver chip and electrical isolation makes possible support of Cheapernet.

PC Implementation on Half Card

The Ethernet Controller has been implemented on an IBM PC expansion board using less area than that required for a half card. The schematic diagram for the design is shown in Figure 9.

Designing with SEEQ EEPLD's

The EEPAL20RA10Z devices provide the glue to hook the EDLC, MCC, and FIFO RAM to the PC bus. The design methodology utilizes PC based assemblers such as PALASM® ABEL™ CUPL™ or MINC™ to transform equations and simulations into JEDEC link maps and test vectors. In this application brief, PALASM2 is chosen. The design specifications are shown in Figure 5.

Testing the Design

Four software programs demonstrate the operation of the Ethernet Controller design. The source language chosen is Turbo PASCAL 4.0™ (Borland International). PC bus operations are implemented using the PORT instructions:

```
PC IO Write :  Port[Address] := Data;PC IO
Read :         Data := Port[Address];
```

The software programs are illustrated in Figure 11.

RAM Test

The basic PC operations of memory address decode, load/increment Tx Counter, Read and Write RAM are exercised by this test. The 8192 RAM locations are loaded with numbers 0 thru 4095 in pairs of bytes, then read back for comparison check.

LoopBack Test

The EDLC 8003 is tested by transmitting a frame to itself in LoopBack Mode. The frame received is compared with the frame that was transmitted.

Continuous Transmit/Receive Test

Using two Ethernet Controllers in two PC's, random frames are continuously transmitted from one controller to the other and echoed back, while error status is checked and errors are counted.

Hello Hello PC to PC Terminal Emulation

Two PCs are configured as terminals as shown in Figure 3., allowing simultaneous frames to be passed back and forth at each operators discretion.

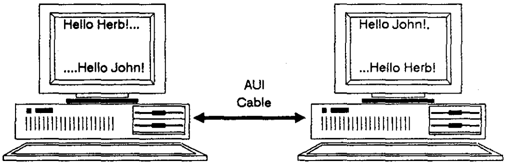


Figure3. PC to PC Terminal Emulation

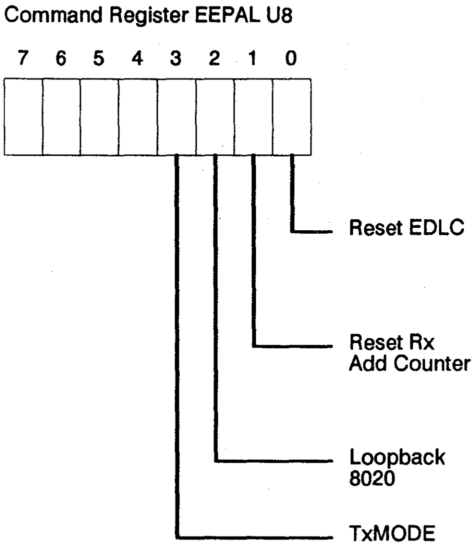


Figure 4. Command Register Bit Map

Address Map

Hex Add A0..A9	**Read** (IOR)	**Write** (IOW)	
300		Station Add 0	EDLC 8003
301		Station Add 1	
302		Station Add 2	
303		Station Add 3	
304		Station Add 4	
305		Station Add 5	
306	Rx Status	Rx Command	
307	Tx Status	Tx Command	
308		Command Reg	EEPAL U3 U4
309		LD Tx A0..A7	EEPAL U9
30A		LD Tx A8..A12	EEPAL U9 U10
30B			Unused
30C	RAM Read	RAM Write	RAM 8kX8

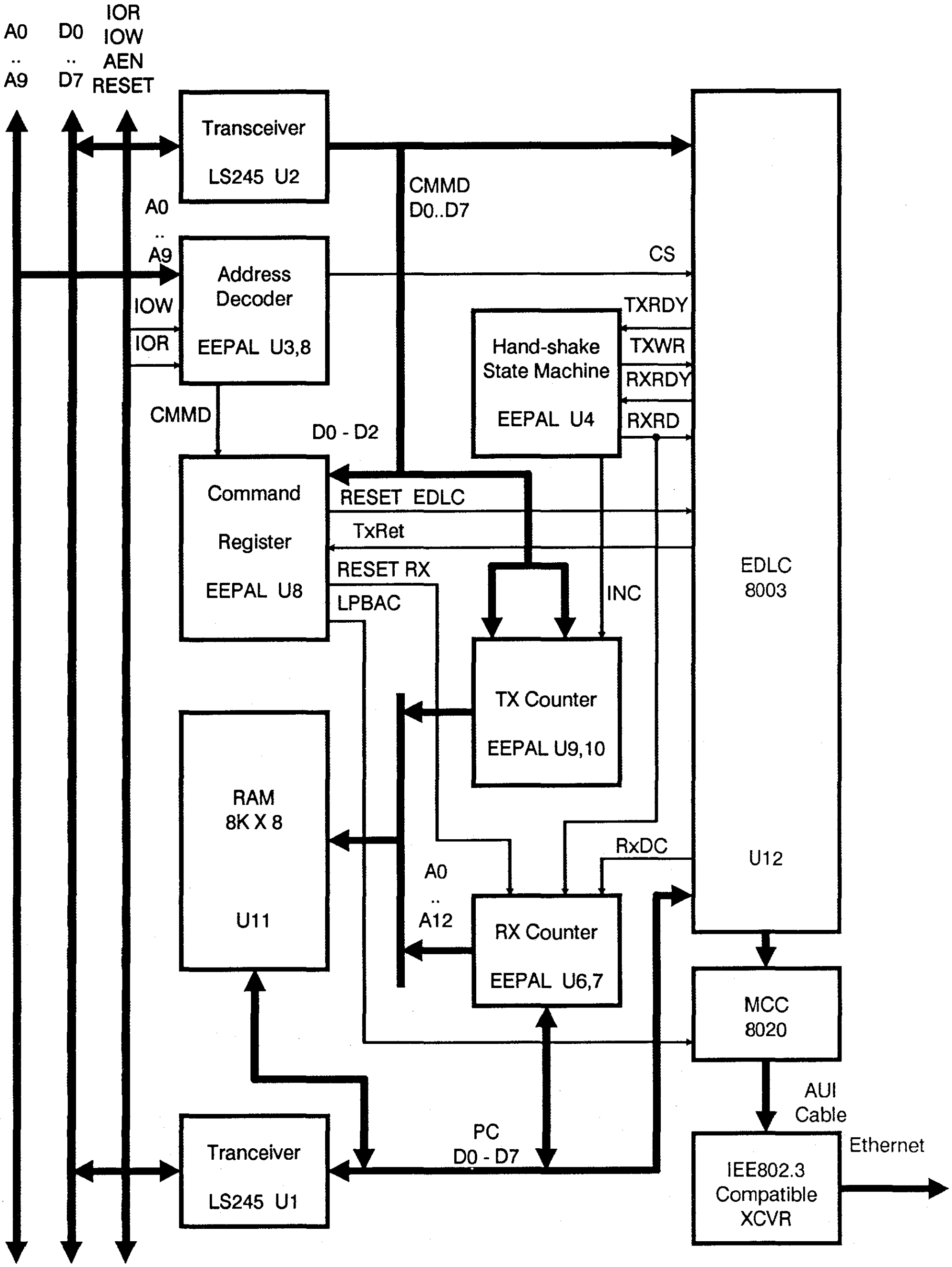
Figure 5. Address Map

Build Your Own Ethernet/Cheapernet Controller

Using the SEEQ EDLC, MCC, and EEPLDs, you can build your own Ethernet/Cheapernet Controller. Contact you local SEEQ representative for a PC/XT/AT floppy disk containing the EEPLD Design Specifications and the EDLC Demonstration software as described below:

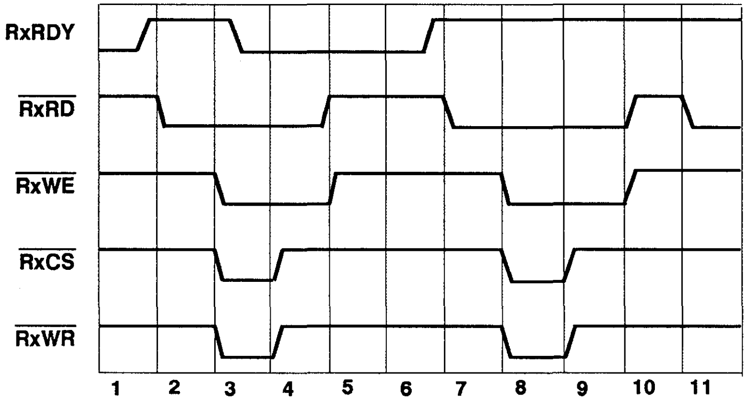
EDLC.EXE
EDLC.PAS
EEPALU3.PDS
EEPALU3.JED
EEPALU4.PDS
EEPALU4.JED
EEPALU6.PDS
EEPALU6.JED
EEPALU7.PDS
EEPALU7.JED
EEPALU8.PDS
EEPALU8.JED
EEPALU9.PDS
EEPALU9.JED
EEPALU10.PDS
EEPAL103.JED
MAKE.BAT

Figure 6. Ethernet/CheaperNet Controller Block Diagram



APP. NOTES

Figure 7. RxRDY/$\overline{\text{RxRD}}$ Handshake Waveforms and Truth Table.



1.RxRDY INACTIVE NO RECEIVED DATA EXISTS IN THE EDLC CHIP. $\overline{\text{RxRD}}$, $\overline{\text{RxWE}}$, $\overline{\text{RxCS}}$ AND $\overline{\text{RxWR}}$ ARE IN AN INACTIVE STATE.

2.THE PLD20RA10Z SAMPLES AN ACTIVE HIGH RXRDY,AT LEAST ONE RECEIVED DATA BYTE EXISTS IN THE EDLC FIFO BUFFER. $\overline{\text{RxRD}}$ GOES ACTIVE LOW.

3.THE STATE MACHINE OUTPUTS $\overline{\text{RxWE}}$, $\overline{\text{RxCS}}$ AND $\overline{\text{RxWR}}$ GO LOW. $\overline{\text{RxCS}}$ AND $\overline{\text{RxWR}}$ CONTROL THE RAM INPUTS TO ENABLE AN ACTIVE WRITE CYCLE.

4.$\overline{\text{RxCS}}$ AND $\overline{\text{RxWR}}$ GO INACTIVE TO END THE RAM WRITE CYCLE.

5.$\overline{\text{RxRD}}$ AND $\overline{\text{RxWE}}$ GO INACTIVE HIGH TO COMPLETE THE HANDSHAKE CYCLE.

6.RxRDY STAYS INACTIVE LOW. ALL OUTPUTS $\overline{\text{RxRD}}$, $\overline{\text{RxWE}}$, $\overline{\text{RxCS}}$ AND $\overline{\text{RxWR}}$ HOLD IN AN INACTIVE STATE.

7 -11.IF RxRDY GOES HIGH THEN THE STATE MACHINE WILL REPEAT THE HANDSHAKE CYCLES WRITING TO THE RAM UNTIL RxRDY GOES INACTIVE AGAIN.

TRUTH TABLE:

RXRDY	$\overline{\text{RxRD}}$	$\overline{\text{RxWE}}$	$\overline{\text{RxCS}}$	
L	H	H	H	;IDLE STATE NO HANDSHAKE ACTIVITY.
H	L	H	H	;$\overline{\text{RxRD}}$ ACKNOWLEDGES ACTIVE RXRDY.
X	L	L	L	;$\overline{\text{RxWE}}$ GOES LOW WITH $\overline{\text{RxCS.}}$
X	L	L	L	;$\overline{\text{RxCS}}$ GOES INACTIVE AFTER WRITE.
L	H	H	H	;ONE HANDSHAKE CYCLE IS COMPLETE.

Figure 8. Design of the RxRDY/$\overline{\mathrm{RxRD}}$ Handshake Logic:

EQUATIONS:

$\overline{\mathrm{RxRD}} := \overline{\mathrm{RxRD}} * \overline{\mathrm{RxWE}} * \overline{\mathrm{RxCS}} * \overline{\mathrm{RxRDY}}$;HOLDS $\overline{\mathrm{RxRD}}$ HIGH WHEN RxRDY
IS INACTIVE.

$+ \mathrm{RxRD} * \mathrm{RxWE} * \overline{\mathrm{RxCS}}$;TOGGLES $\overline{\mathrm{RxRD}}$ INACTIVE AFTER
ACTIVE CYCLE.

$+ \overline{\mathrm{RxRD}} * \mathrm{Rx}\overline{\mathrm{WE}} * \mathrm{RxCS}$;HOLDS $\overline{\mathrm{RxRD}}$ HIGH WHEN THE PC IS
ACCESSING MEMORY.

$\overline{\mathrm{RxWE}} := \mathrm{RxWE}*\mathrm{RxRD}*\overline{\mathrm{RxCS}}$;TOGGLES $\overline{\mathrm{RxWE}}$ INACTIVE AFTER
ACTIVE CYCLE.

$+ \overline{\mathrm{RxWE}}*\overline{\mathrm{RxRD}}*\overline{\mathrm{RxCS}}$;HOLD $\overline{\mathrm{RxWE}}$ INACTIVE WHILE NO

$\overline{\mathrm{RxRD}}$ \ $\overline{\mathrm{RxCS}}$ $\overline{\mathrm{RxWE}}$	01	11	10	00
1	0	1	0	0
0	0	0	1	0

$\overline{\mathrm{RxRD}}$ \ $\overline{\mathrm{RxCS}}$ $\overline{\mathrm{RxWE}}$	01	11	10	00
1	1	1	0	0
0	0	0	1	0

$\mathrm{RxCS} := \mathrm{RxCS}*\overline{\mathrm{RxWE}}*\overline{\mathrm{RxRD}}$;TOGGLES AFTER STATE 2 IN THE
WAVEFORM DIAGRAM. PROGRAMMABLE
POLARITY IS USED ON THIS OUTPUT.

$+ \mathrm{G2}*\mathrm{DIR2}$ GOES LOW FOR PC READ CYCLES.

$\mathrm{RxWR} := \mathrm{RxRD}*\overline{\mathrm{RxWE}}*\overline{\mathrm{RxRD}}$;$\overline{\mathrm{RxWR}}$ GOES LOW AFTER STATE 2 IN
WAVEFORM DIAGRAM. PROGRAMMABLE
POLARITY USED ON THIS OUTPUT.

Figure 9(a). Schematic Diagram, PC Bus and Address Decode

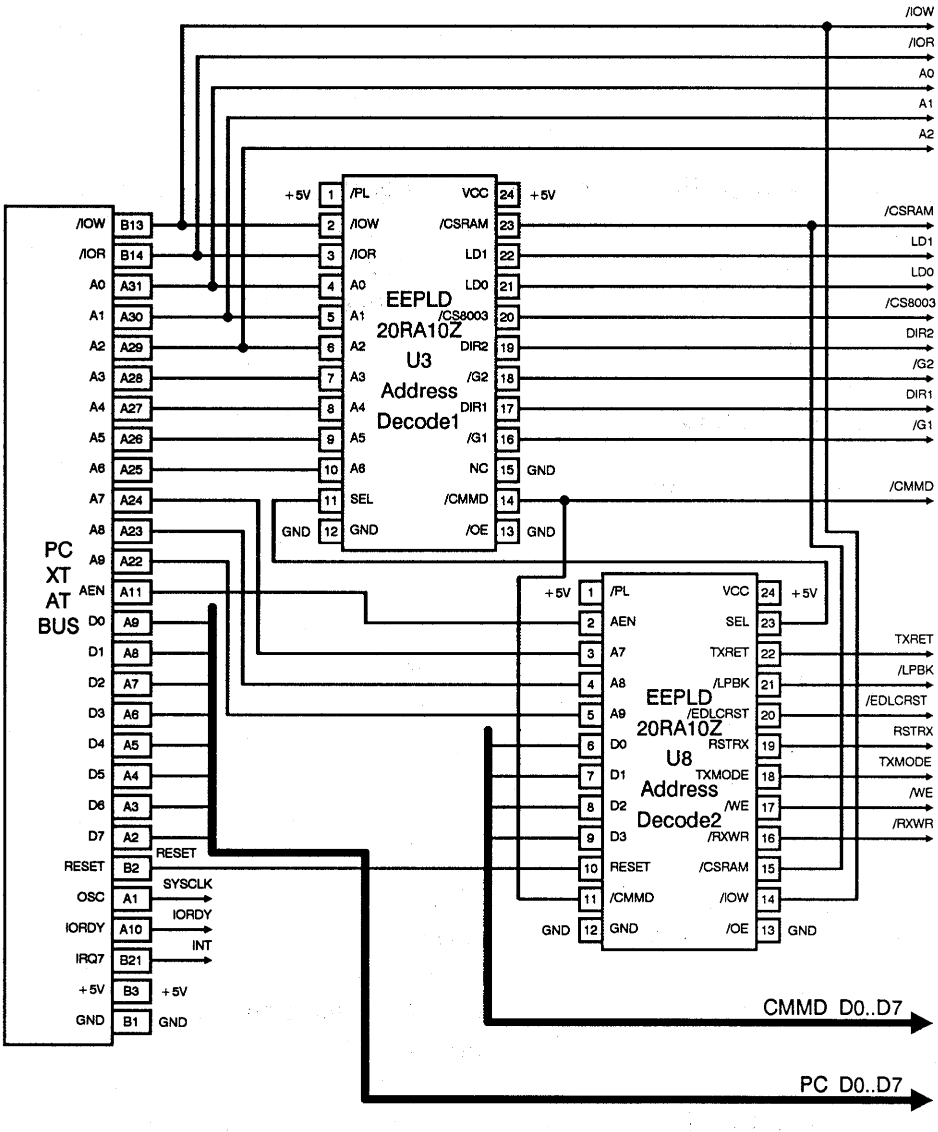


Figure 9(b). Schematic Diagram, Tranceiver and RAM

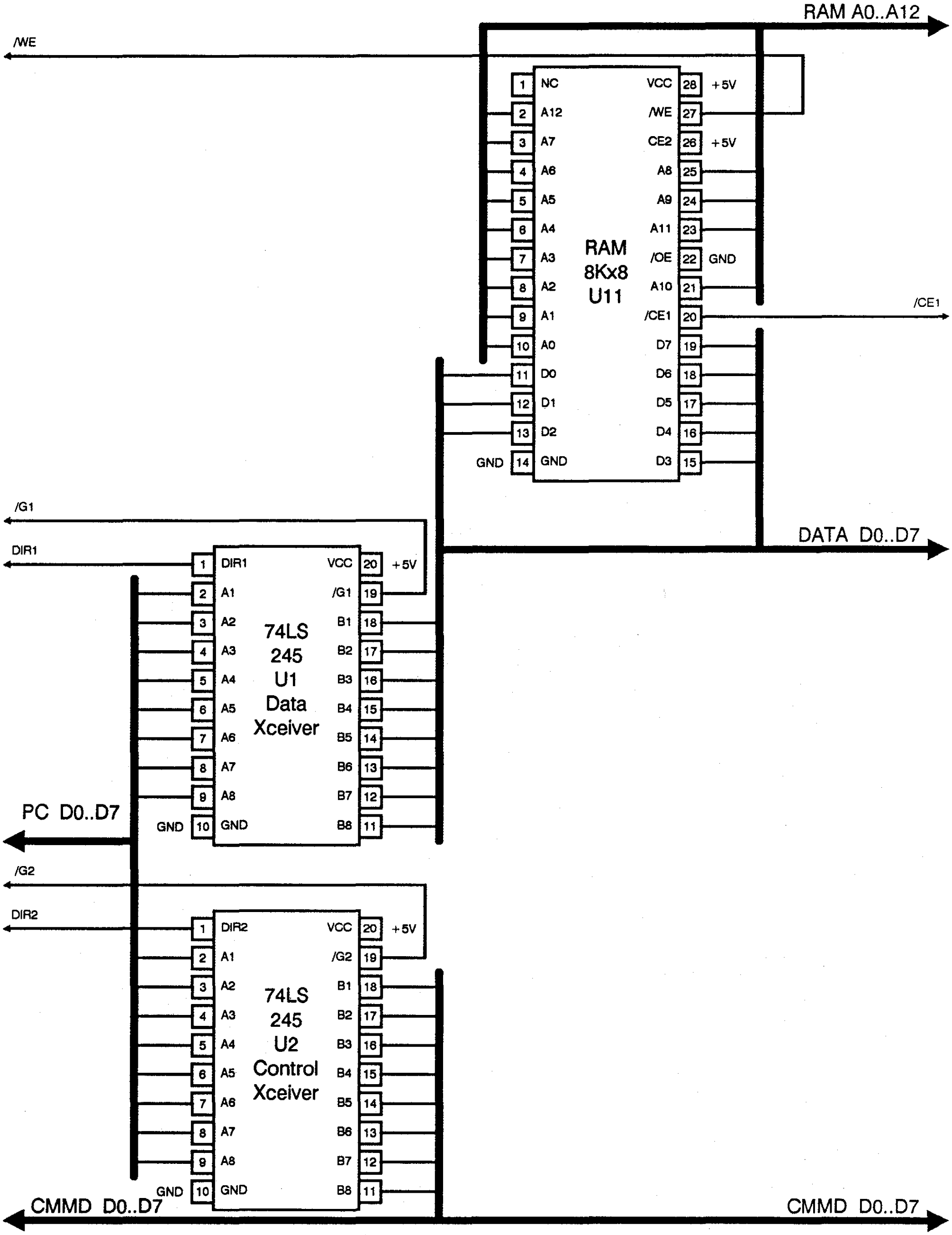


Figure 9(c). Schematic Diagram, Tx and Rx Address Counters

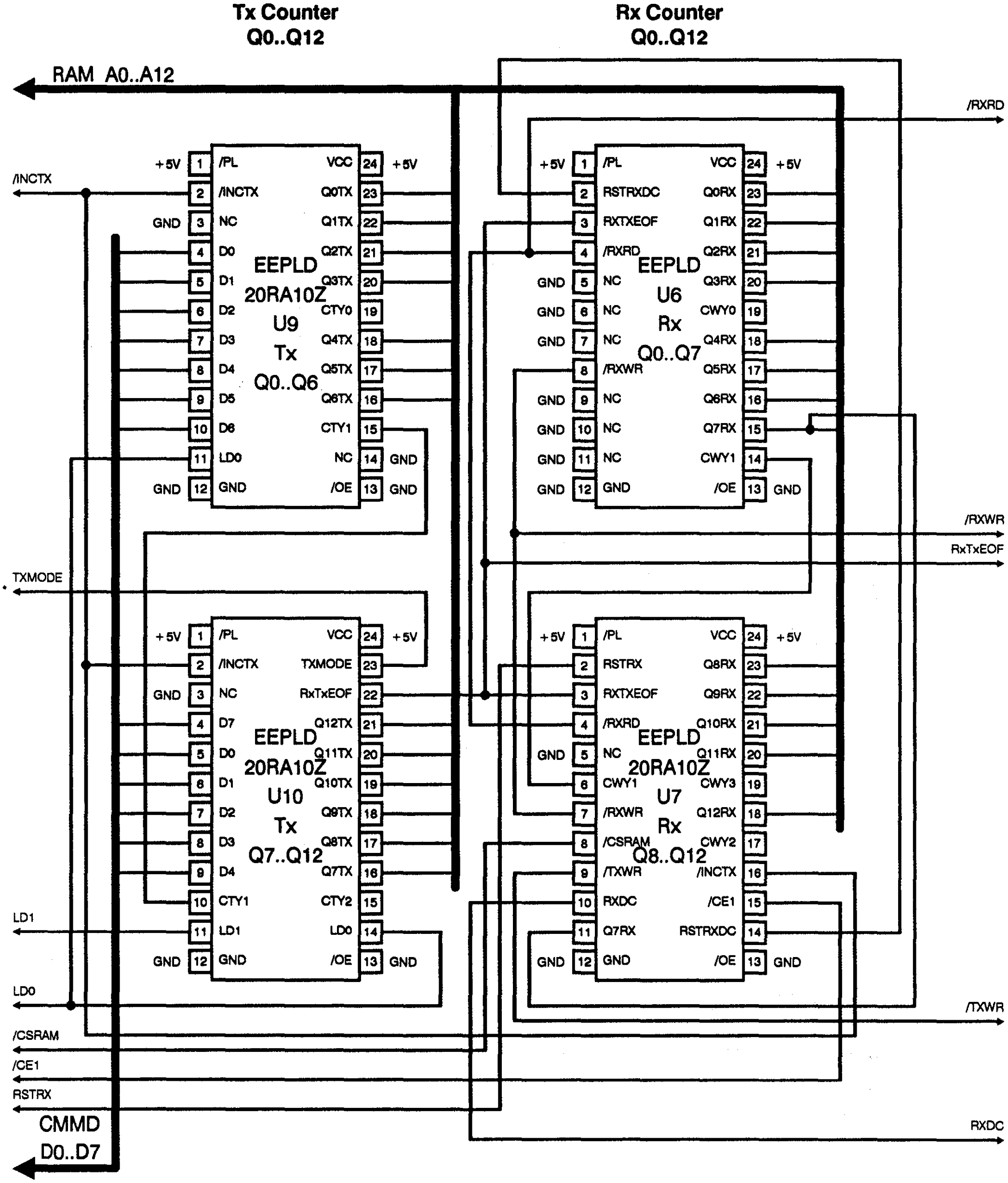
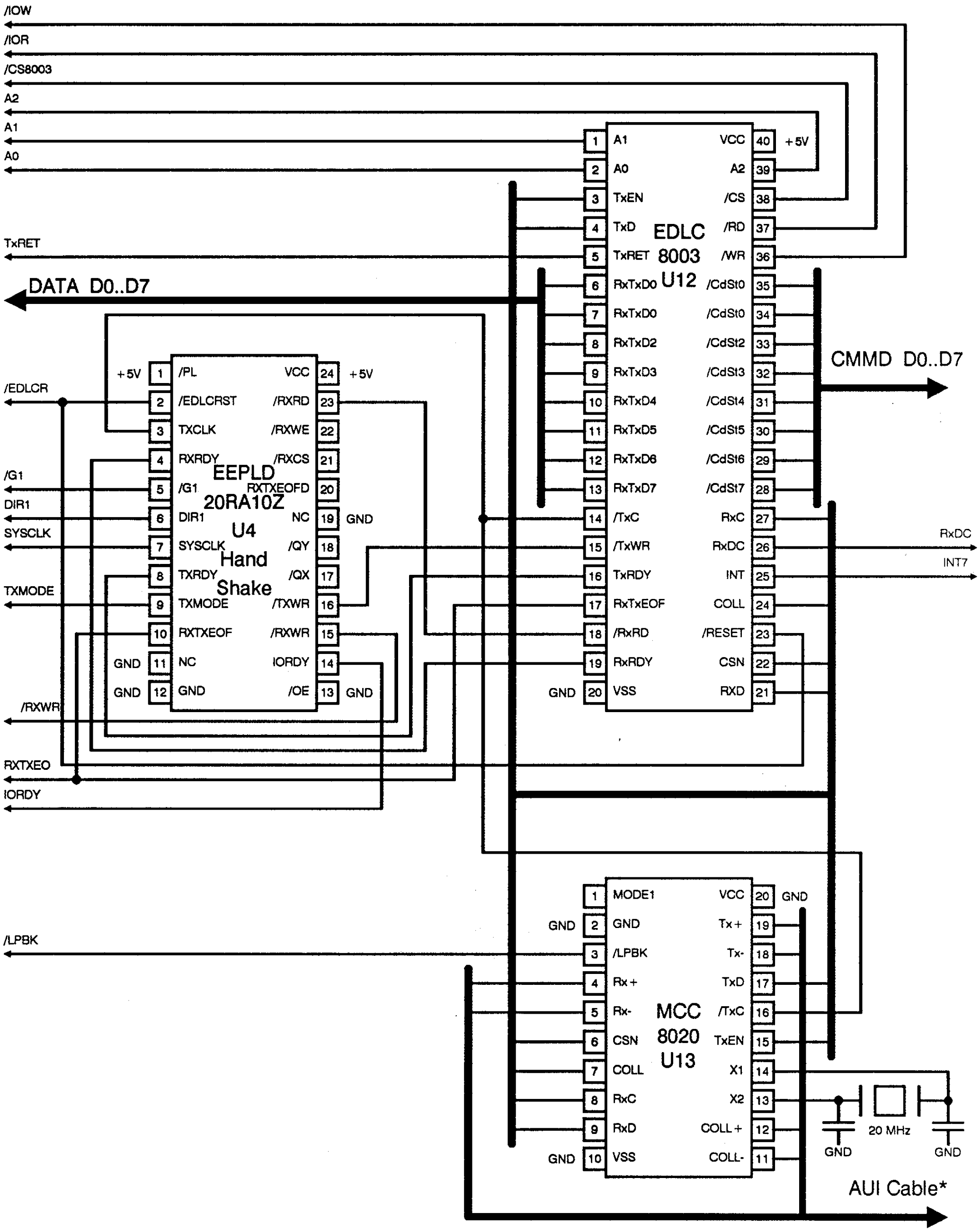


Figure 9(d). Schematic Diagram, EDLC and MCC

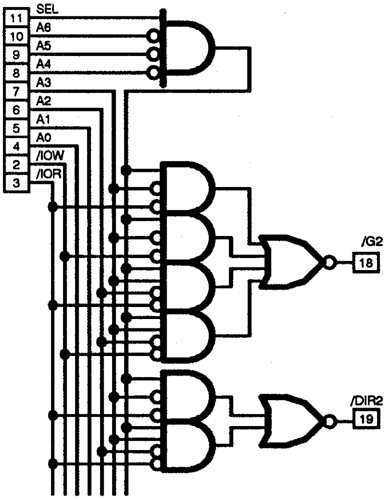


*Note resistor termination as shown in 8020 data sheet

Figure 10. EEPLD Design Specification

Address Decode 1

Logic Gates Example of selected Boolean Equations:



```
TITLE           DECODE_1
PATTERN         U3
REVISION        01
AUTHOR          PEER RESEARCH.
COMPANY         PEER RESEARCH.
DATE            30TH APRIL 1988.
;
CHIP DECODE PAL20RA10
;
;PINS   1       2       3       4       5       6
        /PL     /IOW    /IOR    A0      A1      A2

;PINS   7       8       9       10      11      12
        A3      A4      A5      A6      SEL     GND

;PINS   13      14      15      16      17      18
        /OE     /CMMD   NC      /G1     DIR1    /G2

;PINS   19      20      21      22      23      24
        DIR2    /CS8003 LD0     LD1     /CSRAM  VCC
;
;       Address decode PAL20RA10 U3 is designed generate
;       the enable inputs and direction control of
;       two 74LS245 bi-directional buffer circuits.
;       Also, to create an I/O mapped control load input
;       to the transmit counters, i n addition to giving
;       select inputs to the RAM buffer and 8003 EDLC
;       device.
;       The enable signal G2 selcts a data path to and
;       from the 8003 EDLC device. Data read and write
;       is controlled by the DIR2 signal. The 8003
;       internal registers are selected in the I/O
;       mapping scheme address 0300 to 0307. The second
;       74LS245 is selected in the memory map 0308 to 030F
;       and enables a bi-directional path to the 8k
;       byte RAM buffer store and the RXTXD0-D7 I/O
;       path to and from the 8003 device.
;
EQUATIONS

G2      = SEL*/A6*/A5*/A4*/A3*IOR           ;ADDRESS
        + SEL*/A6*/A5*/A4*/A3*IOW           ;SELECT
        + SEL*/A6*/A5*/A4*A3*/A2*IOR        ;300 TO
        + SEL*/A6*/A5*/A4*A3*/A2*IOW        ;30B
                                            ;
/DIR2   = SEL*/A6*/A5*/A4*/A3*IOR           ;READ ONLY
        + SEL*/A6*/A5*/A4*A3*/A2*IOR        ;300 - 30B
                                            ;(30B UNSUED)
G1      = SEL*/A6*/A5*/A4*A3*A2*IOR         ;ADDRESS
        + SEL*/A6*/A5*/A4*A3*A2*IOW         ;SELECT
                                            ;30C TO
/DIR1   = SEL*/A6*/A5*/A4*A3*A2*IOR         ;30F DIR
                                            ;READ ONLY
CS8003  = SEL*/A6*/A5*/A4*/A3*IOR           ;SELECT
        + SEL*/A6*/A5*/A4*/A3*IOW           ;8003 300
                                            ;TO 307
CMMD    = SEL*/A6*/A5*/A4*A3*/A2*/A1        ;RESET EDLC
        */A0*IOW                            ;ADDRESS 308
                                            ;
CSRAM   = SEL*/A6*/A5*/A4*A3*A2*/A1         ;RAM SELECT
        */A0*IOR                            ;30C
        + SEL*/A6*/A5*/A4*A3*A2*/A1         ;ENABLES WRITE
        */A0*IOW                            ;FROM PC
                                            ;
LD0     = SEL*/A6*/A5*/A4*A3*/A2*/A1        ;LOAD D0-D6
        *A0*IOW                             ;ADDRESS 309
                                            ;
LD1     = SEL*/A6*/A5*/A4*A3*/A2            ;LOAD D7, D0
        *A1*/A0*IOW                         ;TO D4
                                            ;ADDRESS 30A
                                            ;
```

```
SIMULATION                                ;
TRACE_ON       /IOR /IOW                  ;TRACE ALL
               CS8003 LD0 LD1             ;SIGNALS
               G1 DIR1 G2 DIR2            ;
               CMMD A0 A1 A2 A3           ;
               A4 A5 A6 SEL               ;
SETF           OE /PL /IOR /IOW           ;ENABLE OUTPUT
               /A0 /A1 /A2 /A3 /A4        ;DISABLE PRE-
               /A5 /A6 SEL                ;LOAD. SET IOW
FOR L := 0 TO 1 DO                        ;IOR INACTIVE
BEGIN                                     ;ADDRESS INPUT
IF L = 1 THEN                             ;TO ZERO SEL
BEGIN SETF A3 /A2 /A1 /A0                 ;ACTIVE. ADDRESS
END                                       ;A0 - A3 IS
FOR K := 0 TO 1 DO                        ;INCREMENTED
BEGIN                                     ;FROM 0 TO F HEX
IF K = 1 THEN                             ;IN LOOPS L,
BEGIN SETF A2 /A1 /A0                     ;K, J. IN LOOP
END                                       ;I THE IOW AND
FOR J := 0 TO 3 DO                        ;IOR ARE TURNED
BEGIN                                     ;ON AND OFF IN
IF J = 0 THEN                             ;ANTIPHASE.
BEGIN SETF /A0 /A1                        ;
END                                       ;
IF J = 1 THEN                             ;
BEGIN SETF A0                             ;
END                                       ;
IF J = 2 THEN                             ;
BEGIN SETF /A0 A1                         ;
END                                       ;
IF J = 3 THEN                             ;
BEGIN SETF A0                             ;
END                                       ;
FOR I := 1 TO 2 DO                        ;
BEGIN                                     ;
SETF      IOR /IOW                        ;
SETF      /IOR IOW                        ;
END                                       ;
END                                       ;
END                                       ;
END                                       ;
TRACE_OFF                                 ;
```

Figure 10. EEPLD Design Specification

Address Decode 2

```
TITLE           DECODE_2
PATTERN         U8
REVISION        01
AUTHOR          PEER RESEARCH.
COMPANY         PEER RESEARCH.
DATE            30TH APRIL 1988.
;
;
CHIP DECODE PAL20RA10
;
;PINS   1       2       3       4       5       6
        /PL     /AEN    A7      A8      A9      D0

;PINS   7       8       9       10      11      12
        D1      D2      D3      RESET   /CMMD   GND

;PINS   13      14      15      16      17      18
        /OE     /IOW    /CSRAM  /RXWR   /WE     TXMODE

;PINS   19      20      21      22      23      24
        RSTRX   /EDLCRST /LPBK  TXRET   SEL     VCC
;
;       /AEN, address enable and A9, A8, A7, address
;       inputs from the PC bus are gated to form SEL
;       a chip select input to the lower order address
;       decoder logic PAL20RA10 PATTERN U3. /CMMD input
;       is a decoded signal from U3 at address location
;       308 which enable the data inputs D0, D1, D2
;       and D3. When D0 and CMMD are valid the 8003
;       EDLC chip is reset. D1 and CMMD reset the RX
;       counters U6 and U7. A loop back test in the
;       EDLC chip is enabled when D2 and CMMD are valid
;       local testing of the interface is possible
;       when this mode is selected. D3 and CMMD enable
;       the EDLC device to mode 1 operation and D3 with
;       a valid CMMD input enable the EDLC 8003 device
;       to perform transimission over the interface.
;       A composite RAM WE signal is generated from
;       CSRAM and IOW or RXWR, for PC and RXCounter
;       access respectively.
;
EQUATIONS
                                                ;ACTIVE HIGH
SEL             = A9*A8*/A7*AEN                 ;ADDRESS

EDLCRST         := D0                           ;RESET EDLC.
EDLCRST.CLKF    = /CMMD                         ;8003 LOGIC
EDLCRST.SETF    = RESET                         ;PC RESET
                                                ;
RSTRX           := D1                           ;RESET RECIEVE
RSTRX.CLKF      = /CMMD                         ;COUNTER.
RSTRX.RSTF      = RESET                         ;PC RESET.
                                                ;
LPBK            := D2                           ;ENABLE
LPBK.CLKF       = /CMMD                         ;LOOPBACK
LPBK.SETF       = RESET                         ;PC RESET.
                                                ;
TXMODE          := D3                           ;ENABLE EDLC
TXMODE.CLKF     = /CMMD                         ;FOR TRANS-
TXMODE.SETF     = TXRET                         ;PC RESET.
                                                ;
WE              = IOW*CSRAM                     ;COMPOSITE
                + RXWR                          ;WRITE ENABLE
                                                ;TO RAM.
```

```
SIMULATION                                    ;
TRACE_ON       /AEN A9 A8 A7 CMMD             ;TRACE ALL
               D0 D1 D2 D3 SEL                ;INPUT/OUTPUT
               EDLCRST RSTRX LPBK             ;SIGNALS
               TXMODE /WE                     ;
               IOW CSRAM RXWR                 ;
               RESET TXRET                    ;
SETF           /AEN /CMMD A7 A8 A9            ;
               /D0 /D1 /D2 /D3                ;
               /IOW /CSRAM /RXWR              ;
               /RESET /TXRET                  ;
               OE /PL                         ;
SETF           AEN                            ;TEST SEL OUTPUT
SETF           /A7                            ;
SETF           A7 /A8                         ;
SETF           A8 /A9                         ;
SETF           /AEN                           ;
SETF           CMMD                           ;TEST EDLC RESET
SETF           D0                             ;TEST RXRST
SETF           /D0 D1                         ;OUTPUT
SETF           /D1 D2                         ;TEST LOOPBACK
SETF           /D2 D3                         ;SELECT
SETF           /D3                            ;SELECT, TXMODE
SETF           /CMMD                          ;
SETF           CSRAM IOW                      ;TEST WRITE MODE
SETF           /IOW                           ;SELECTION FOR
SETF           /CSRAM                         ;THE RAM BUFFER.
SETF           RXWR                           ;
SETF           /RXWR                          ;
TRACE_OFF                                     ;
```

Figure 10. EEPLD Design Specification

Handshake Logic

```
TITLE           HANDSHAKE_LOGIC
PATTERN         U4
REVISION        04.
AUTHOR          PEER RESEARCH.
COMPANY         PEER RESEARCH.
DATE            30TH MAY 1988.
;
;
CHIP HSHAKE1 PAL20RA10
;
;PINS    1       2       3       4       5       6
         /PL     /EDLCRST TXCLK  RXRDY   /G1     DIR1

;PINS    7       8       9       10      11      12
         SYSCLK  TXRDY   TXMODE RXTXEOFNC        GND

;PINS    13      14      15      16      17      18
         /OE     IORDY   /RXWR   /TXWR   /QX     /QY

;PINS    19      20      21      22      23      24
         NC      RXTXEOFD /RXCS  /RXWE   /RXRD   VCC
;
;        Pins RXRDY and /RXRD perform the handshake operation
;        between the 8003 ethernet interface and the PAL20RA10
;        the RXRDY high output from the 8003 chip tells the
;        PAL20RA10 that there exists, at least one, data byte
;        in the internal 16 byte FIFO. when this signal goes
;        high it is sampled by the rising edge of TXCLK which
;        is the transmitter clock output of the 8020 Manchester
;        encoder device. the internal state machine output of
;        /RXRD performs the handshake response, while /RXWE and
;        /RXCS cycles through a write operation. The /RXWE
;        signal is not used for RAM write operations it
;        is used here as an additional register to enable
;        the correct sequence in the /RXRD RXRDY handshake
;        state machine. it is /RXCS going active LOW that
;        creates the RAM write operation.
;        The TXRDY and /TXWR are the transmitter handshake
;        signals. The EDLC 8003 sends a valid TXRDY signal
;        when its internal 16 byte FIFO is empty. If the
;        handshake operation is enabled by TXMODE then the
;        process of reading data from the buffer RAM and
;        writing to the 8003's fifo continues until an end
;        of file (RXTXEOF) is generated by PAL20RA10 U10.
;        Control of the buffer RAM is handled by RXCS and
;        RXWE. RXCS is the RAM chip select signal that is
;        active during write operations. It is gated with
;        two other signals in PAL20RA10 U5 to select the
;        RAM during both read and write operations. TXMODE
;        is enabled or disabled by software in the PC.
;
EQUATIONS
                                                 ;
/RXRD           := RXRD*RXWE*/RXCS               ;TOGGLE RXRD.
                 + TXWR                          ;WAIT TXWR.
                 + /RXRD*/RXWE*RXCS              ;HOLD RXRD ACTIVE.
                 + /RXWE*/RXCS*/RXRD             ;HOLD RXRD IF
                  */RXRDY                        ;RXRDY NOT TRUE.
/RXRD.CLKF       = TXCLK                         ;CLOCK RXRD.
/RXRD.RSTF       = EDLCRST                       ;RESET RXRD.
                                                 ;
/RXWE           := /RXRD*/RXWE*/RXCS             ;HOLD RXWE.
                 + RXRD*RXWE*/RXCS               ;TOGGLE RXWE.
                 + /RXRD*/RXWE*RXCS              ;HOLD RXWE.
/RXWE.CLKF       = TXCLK                         ;
/RXWE.RSTF       = EDLCRST                       ;
                                                 ;
RXCS            := RXRD*/RXWE*/RXCS              ;ENABLE RAM
                 + G1*DIR1                       ;ENABLE U2.
/RXCS.CLKF       = TXCLK                         ;
/RXCS.RSTF       = EDLCRST                       ;
                                                 ;
RXWR             = RXRD*RXWE*RXCS                ;WRITE TO RAM
                                                 ;WHEN RXRD,RXWE
IORDY           := G1*/RXRD                      ;RXCS ACTIVE
IORDY.CLKF       = SYSCLK                        ;ENABLE AND
IORDY.SETF       = EDLCRST                       ;CONTROL U2
IORDY.TRST       = GND                           ;DIRECTION.
```

```
                                       ;
TXWR            := /TXWR*TXRDY*TXMODE  ;TXWR ACTIVE
                */RXTXEOFD*/RXRDY*/RXRD;IF TXRDY AND
                 +  TXWR*QX            ;TXMODE SET.
                 +  TXWR*QY            ;QX AND QY
TXWR.CLKF        = TXCLK               ;HOLD TXWR
TXWR.RSTF        = EDLCRST             ;ACTIVE FOR
                                       ;THREE CLOCK
QX              := /TXWR*TXRDY*TXMODE  ;CYCLES. TO
                */RXTXEOFD*/RXRDY*/RXRD;SATISFY RAM
QX.CLKF          = TXCLK               ;WRITE CYCLE
QX.RSTF          = /TXMODE             ;TIME.
                                       ;
QY              := QX                  ;REGISTERS QX
QY.CLKF          = TXCLK               ;AND QY STRETCH
QY.RSTF          = /TXMODE             ;TXWR.
                                       ;
RXTXEOFD        := RXTXEOF             ;
RXTXEOFD.CLKF    = /TXWR               ;
RXTXEOFD.SETF    = /TXMODE             ;
                                       ;
SIMULATION                             ;
TRACE_ON        TXCLK EDLCRST TXRDY    ;TRACE ON ALL
                /TXWR /QX /QY RXRDY /RXRD ;SIGNALS.
                /RXWE /RXCS /RXWR /SYSCLK ;
                IORDY /G1 DIR1         ;
                                       ;
SETF            /TXCLK /SYSCLK EDLCRST ;SET IDLE MODE,
                /RXRDY OE /PL /G1      ;NO INCOMING DATA
                DIR1 /TXRDY TXMODE     ;FROM ETHERNET.
SETF            /EDLCRST               ;NO PC ACCESS.
FOR I := 1 TO 8 DO                     ;
BEGIN                                  ;CLOCK FOR EIGHT
SETF            TXCLK /SYSCLK          ;PERIODS TO TEST
SETF            /TXCLK SYSCLK          ;HOLD CONDITION.
END
SETF            RXRDY                  ;SET RECIEVER READY
FOR J := 1 TO 2 DO                     ;8003 FIFO HAS DATA
BEGIN                                  ;FROM ETHERNET.
FOR I := 1 TO 8 DO                     ;SET A LOOP FOR
BEGIN                                  ;SIXTEEN CLOCK
SETF            RXRDY                  ;CYCLES. FOUR HAND-
IF I = 2 THEN BEGIN                    ;SHAKE CYCLES TAKE
SETF            /RXRDY                 ;PLACE. RXRDY TURNS
END                                    ;OFF THEN ON AFTER
SETF            TXCLK /SYSCLK          ;FIRST AND THIRD
SETF            /TXCLK   SYSCLK        ;HANDSHAKE.
END                                    ;
END                                    ;
SETF            /RXRDY G1              ;TURN OF RXRDY
FOR J := 1 TO 4 DO                     ;SELECTION OF G1
BEGIN                                  ;BY DECODING ADD-
SETF            G1                     ;RESS FROM PC TO
FOR I := 1 TO 4 DO                     ;TEST I/O READY
BEGIN                                  ;SIGNAL.
SETF            /TXCLK SYSCLK          ;
SETF            TXCLK /SYSCLK          ;
END                                    ;
SETF            /G1                    ;TURN OF PC SELEC-
SETF            /TXCLK SYSCLK          ;TION.
SETF            TXCLK /SYSCLK          ;
END                                    ;TURN OF END OFF
SETF     TXRDY TXMODE /RXTXEOF         ;FILE TURN ON TXRDY
FOR I := 1 TO 16 DO                    ;AND TXMODE TO TEST
BEGIN                                  ;THE TXRDY AND TXWR
SETF /TXCLK SYSCLK                     ;HANDSHAKE FOR
SETF TXCLK /SYSCLK                     ;SIXTEEN CYCLES.
END                                    ;
TRACE_OFF                              ;
```

Figure 10. EEPLD Design Specification

Rx Counter Q0..Q7

```
TITLE           RXCOUNTER_Q0-Q7
PATTERN         U6
REVISION        04.
AUTHOR          PEER RESEARCH.
COMPANY         PEER RESEARCH.
DATE            30TH MAY 1988.
;
;
CHIP COUNTER PAL20RA10
;
;
;PINS   1       2       3        4       5       6
        /PL     RSTRXDC RXTXEOF /RXRD    NC      NC

;PINS   7       8       9       10      11      12
        NC      /RXWR   NC      NC      NC      GND

;PINS   13      14      15      16      17      18
        /OE     CWY1    Q7RX    Q6RX    Q5RX    Q4RX

;PINS   19      20      21      22      23      24
        CWY0    Q3RX    Q2RX    Q1RX    Q0RX    VCC
;
;       The receive counter has been designed to give
;       a binary count output to the 8K RAM. Registers
;       Q0RX - Q7RX are contained in PAL20RA10 U6 and
;       registers Q8RX - Q12RX in U7. The carry outputs
;       from U6 are connected to U7 to provide the
;       link necessary for a synchronous count. The
;       receive counter, RXCOUNTER is clocked by the
;       /RXWR input. After a valid RXRD (receiver
;       ready) /RXWR from U4 goes LOW to perform a
;       write cycle in the RAM. When /RXWR goes HIGH
;       the rising edge of this signal increments the
;       counter to point to the next location in the
;       RAM. The 3 - State control of U6's  output
;       buffers are controlled by the RXRD so when
;       RXRD is active the registered outputs drive
;       the RAM address inputs. Unlike the transmit
;       counter the receive counter cannot be loaded
;       with a starting address, but it can be reset
;       from the PC by a decoded I/O address from the
;       bus. When RSTRXDC is active the contents of
;       the counter is asynchronously set to zero.
;       The RXTXEOF signal is an output from the
;       EDLC 8003 device during data reception, and
;       this signal is used to reset the counter
;       after a complete data frame has been received
;
EQUATIONS

Q0RX            : = /Q0RX*/RXTXEOF          ;TOGGLE Q0RX WHEN
Q0RX.CLKF        = /RXWR                    ;RXTXEOF INACTIVE
Q0RX.SETF        = RSTRXDC                  ;CLEAR OUTPUT
Q0RX.TRST        = RXRD                     ;HIGH - Z WHEN
                                            ;RXRD NOT ACTIVE.
Q1RX            : = /Q1RX*Q0RX*/RXTXEOF     ;TOGGLE Q1RX
                 + Q1RX*/Q0RX*/RXTXEOF      ;HOLD Q1RX
Q1RX.CLKF        = /RXWR                    ;CLOCK Q1RX
Q1RX.SETF        = RSTRXDC                  ;CLEAR OUTPUT
Q1RX.TRST        = RXRD                     ;HIGH - Z WHEN
                                            ;RXRD NOT ACTIVE.
Q2RX            : = /Q2RX*Q0RX*Q1RX         ;TOGGLE Q2RX
                */RXTXEOF                   ;
                 + Q2RX*/Q1RX*/RXTXEOF      ;HOLD Q2RX
                 + Q2RX*/Q0RX*/RXTXEOF      ;HOLD Q2RX
Q2RX.CLKF        = /RXWR                    ;CLOCK Q2RX
Q2RX.SETF        = RSTRXDC                  ;CLEAR OUTPUT
Q2RX.TRST        = RXRD                     ;HIGH - Z WHEN
                                            ;RXRD NOT ACTIVE.
Q3RX            : = /Q3RX*Q2RX*Q0RX         ;TOGGLE Q3RX
                *Q1RX*/RXTXEOF              ;
                 + Q3RX*/Q2RX*/RXTXEOF      ;HOLD Q3RX
                 + Q3RX*/Q1RX*/RXTXEOF      ;HOLD Q3RX
                 + Q3RX*/Q0RX*/RXTXEOF      ;HOLD Q3RX
Q3RX.CLKF        = /RXWR                    ;CLOCK Q3RX
Q3RX.SETF        = RSTRXDC                  ;CLEAR OUTPUT
Q3RX.TRST        = RXRD                     ;HIGH - Z WHEN
```

```
                                        ;RXRD NOT ACTIVE.
CWY0            = Q0RX*Q1RX*Q2RX*Q3RX;CARRY PROPAGATE.
                                        ;
Q4RX            := /Q4RX*CWY0*/RXTXEOF  ;TOGGLE Q4RX
                 + Q4RX*/CWY0*/RXTXEOF  ;
Q4RX.CLKF        = /RXWR                ;CLOCK Q4RX
Q4RX.SETF        = RSTRXDC              ;CLEAR OUTPUT
Q4RX.TRST        = RXRD                 ;HIGH - Z WHEN
                                        ;RXRD NOT ACTIVE.
Q5RX            := /Q5RX*Q4RX*CWY0      ;TOGGLE Q5RX
                 */RXTXEOF              ;
                 + Q5RX*/Q4RX*/RXTXEOF  ;HOLD Q5RX
                 + Q5RX*/CWY0*/RXTXEOF  ;HOLD Q5RX
Q5RX.CLKF        = /RXWR                ;CLOCK Q5RX
Q5RX.SETF        = RSTRXDC              ;CLEAR OUTPUT
Q5RX.TRST        = RXRD                 ;HIGH - Z WHEN
                                        ;RXRD NOT ACTIVE.
Q6RX            := /Q6RX*Q5RX*Q4RX      ;TOGGLE Q6RX
                 *CWY0*/RXTXEOF         ;
                 + Q6RX*/Q5RX*/RXTXEOF  ;HOLD Q6RX
                 + Q6RX*/Q4RX*/RXTXEOF  ;HOLD Q6RX
                 + Q6RX*/CWY0*/RXTXEOF  ;HOLD Q6RX
Q6RX.CLKF        = /RXWR                ;CLOCK Q6RX
Q6RX.SETF        = RSTRXDC              ;CLEAR OUTPUT
Q6RX.TRST        = RXRD                 ;HIGH - Z WHEN
                                        ;NOT ACTIVE.
CWY1             = Q6RX*Q5RX*Q4RX       ;CARRY PROPAGATE.
                 * Q3RX*Q2RX*Q1RX*Q0RX  ;
                                        ;
Q7RX            := /Q7RX*CWY1*/RXTXEOF  ;Q7RX TOGGLE
                 + Q7RX*/CWY1*/RXTXEOF  ;
Q7RX.CLKF        = /RXWR                ;CLOCK Q7RX
Q7RX.SETF        = RSTRXDC              ;CLEAR OUTPUT
Q7RX.TRST        = RXRD                 ;HIGH - Z WHEN
                                        ;NOT ACTIVE.
SIMULATION                              ;
TRACE_ON        /RXWR /RXRD RSTRXDC     ;TRACE ALL SIGNALS.
                RXTXEOF Q0RX Q1RX Q2RX  ;
                Q3RX CWY0 Q4RX Q5RX     ;
                Q6RX CWY1 Q7RX          ;

SETF            RXWR RXRD RSTRXDC /PL   ;ENABLE OUTPUTS AND
                OE /RXTXEOF             ;COUNTER, DISABLE
SETF            /RSTRXDC                         ;PRELOAD.
FOR I := 1 TO 64 DO                     ;FOR 64 CLOCKS
BEGIN                                   ;COUNT A BINARY
SETF     /RXWR                          ;ADDRESS SEQUENCE.
SETF     RXWR                           ;
END                                     ;
TRACE_OFF                               ;
```

Figure 10. EEPLD Design Specification

Rx Counter Q8..Q12

```
TITLE           RXCOUNTER_Q8-Q12
PATTERN         U7
REVISION        04.
AUTHOR          PEER RESEARCH.
COMPANY         PEER RESEARCH.
DATE            30TH MAY 1988.
;
;
CHIP COUNTER PAL20RA10
;
;
;PINS   1       2       3       4       5       6
        /PL     RSTRX   RXTXEOF/RXRD    NC      CWY1

;PINS   7       8       9       10      11      12
        /RXWR   /CSRAM  /TXWR   RXDC    Q7RX    GND

;PINS   13      14      15      16      17      18
        /OE     RSTRXDC/CE1     /INCTX  CWY2    Q12RX

;PINS   19      20      21      22      23      24
        CWY3    Q11RX   Q10RX   Q9RX    Q8RX    VCC
;
;       PAL20RA10 U7 is used in conjunction with U6
;       as an counter to address the 8K RAM as a
;       receive buffer. When the EDLC 8003 device is
;       receiving data the RXRDY and /RXRD handshake
;       control the flow of data from the EDLC's
;       FIFO. As with U6 RXWR and RXRD control the
;       incrementing and 3 - State disable of the
;       output buffers from each counter register.
;       Q7RX - Q10RX perform the conventional binary
;       count, but Q11RX and Q12RX point to the page
;       boundaries at 0 - 2K, 2K - 4K and 4K - 6K.
;       The RXCOUNTER does not encroach into the
;       RAM space allocated for transmition of data,
;       6K - 8K. The count sequence of Q11RX and
;       Q12RX is of the sequence 0 to 1 to 2 then
;       back to 0.
;       Additional logic has been incorporated in
;       this device, /INCTX and /CE1. The /INCTX
;       output is a combinational sum of CSRAM and
;       /TXWR and is responsible for incrementing
;       the transmitter counter U9 and U10 after
;       a PC or EDLC access. The /CE1 is a sum of
;       CSRAM, /TXWR and /RXRD to enable RAM access
;       from the PC, EDLC in transmit mode or EDLC
;       in receive mode.
;
EQUATIONS
                                                ;CARRY THROUGH
CWY2            = CWY1*Q7RX                     ;FROM U6.
                                                ;
Q8RX            := /Q8RX*CWY2*/RXTXEOF          ;TOGGLE Q8RX
                 + Q8RX*/CWY2*/RXTXEOF          ;HOLD Q8RX
Q8RX.CLKF        = /RXWR                        ;CLOCK Q8RX
Q8RX.SETF        = RSTRXDC                      ;CLEAR OUTPUT
Q8RX.TRST        = RXRD                         ;HIGH - Z WHEN
                                                ;NOT ACTIVE.
Q9RX            := /Q9RX*Q8RX*CWY2              ;TOGGLE Q9RX
                 */RXTXEOF                      ;
                 + Q9RX*/Q8RX*/RXTXEOF          ;HOLD Q9RX
                 + Q9RX*/CWY2*/RXTXEOF          ;HOLD Q9RX
Q9RX.CLKF        = /RXWR                        ;CLOCK Q9RX
Q9RX.SETF        = RSTRXDC                      ;CLEAR OUTPUT
Q9RX.TRST        = RXRD                         ;HIGH - Z WHEN
                                                ;NOT ACTIVE.
Q10RX           := /Q10RX*Q9RX*Q8RX             ;TOGGLE Q10RX
                 *CWY2*/RXTXEOF                 ;
                 + Q10RX*/Q8RX*/RXTXEOF         ;HOLD Q10RX
                 + Q10RX*/Q9RX*/RXTXEOF         ;HOLD Q10RX
                 + Q10RX*/CWY2*/RXTXEOF         ;HOLD Q10RX
Q10RX.CLKF       = /RXWR                        ;CLOCK Q10RX
Q10RX.SETF       = RSTRXDC                      ;CLEAR OUTPUT
Q10RX.TRST       = RXRD                         ;HIGH - Z WHEN
                                                ;NOT ACTIVE.
CWY3             = CWY2*Q8RX*Q9RX*Q10RX ;CARRY PROPAGATE.
```

```
Q11RX           := /Q11RX*/Q12RX          ;Q11RX TOGGLES IF
                 *RXTXEOF                 ;Q12RX IS LOW.
                 + Q11RX*/RXTXEOF         ;AND NOT RXTXEOF
Q11RX.CLKF       = /RXWR                  ;ELSE HOLD.
Q11RX.SETF       = RSTRX                  ;CLEAR OUTPUT
Q11RX.TRST       = RXRD                   ;HIGH - Z WHEN
                                          ;NOT ACTIVE.
Q12RX           := /Q12RX*Q11RX*RXTXEOF   ;Q12RX TOGGLES IF
                 + Q12RX*/RXTXEOF         ;Q11RX HIGH AND
Q12RX.CLKF       = /RXWR                  ;NOT RXTXEOF ELSE
Q12RX.SETF       = RSTRX                  ;HOLD. CLEAR
Q12RX.TRST       = RXRD                   ;OUTPUT HIGH - Z
                                          ;WHEN NOT ACTIVE.
RSTRXDC          = RSTRX + RXDC;RESET OR RXDC
                                          ;
INCTX            = CSRAM                  ;CSRAM OR TXWR
                 + TXWR                   ;INCREMENTS TX
                                          ;COUNTER.
CE1              = CSRAM                  ;RAM IS SELECTED
                 + TXWR                   ;FOR PC, TX OR
                 + RXRD                   ;RX ACCESS.
                                          ;
SIMULATION                                ;
TRACE_ON        /RXWR /RXRD RSTRX         ;TRACE ALL SIGNALS.
                RXTXEOF Q8RX Q9RX         ;
                Q10RX CWY3 Q11RX          ;
                Q12RX                     ;
SETF            RXWR RXRD RSTRX /PL       ;ENABLE OUTPUTS
                OE Q7RX CWY1      ;DISABLE PRELOAD.
                /RXTXEOF                  ;WHEN RXTXEOF NOT
SETF            /RSTRX                    ;ACTIVE CLOCK
FOR I := 1 TO 64 DO                       ;COUNTER 64 TIMES.
BEGIN                                     ;
SETF     /RXWR                            ;
SETF     RXWR                             ;
END                                       ;
TRACE_OFF                                 ;
```

Figure 10. EEPLD Design Specification

Tx Counter Q0..Q6

```
TITLE           TXCOUNTER_Q0-Q6
PATTERN         U9
REVISION        04.
AUTHOR          PEER RESEARCH.
COMPANY         PEER RESEARCH.
DATE            30TH MAY 1988.
;
;
CHIP COUNTER PAL20RA10
;
;
;PINS    1        2        3        4        5        6
         /PL      /INCTX   NC       D0       D1       D2

;PINS    7        8        9        10       11       12
         D3       D4       D5       D6       LD0      GND

;PINS    13       14       15       16       17       18
         /OE      NC       CTY1     Q6T      Q5T      Q4T

;PINS    19       20       21       22       23       24
         CTY0     Q3T      Q2T      Q1T      Q0T      VCC
;
;        The transmit RAM buffer counter is a loadable
;        binary counter from the PC bus. When LD0 is
;        active data on D0 - D6 is loaded into registers
;        Q0 - Q6. LD0 is a signal decoded from the PC
;        at the I/O location 309. The /INCTX input
;        performs two functions, it controls the enable
;        output of the counter during a transmission
;        access to the RAM buffer and then increments
;        the counter on the rising edge. When HIGH the
;        counter outputs are in a 3 - State condition.
;        In a 3 - State the recieve counter can be
;        enabled onto the address inputs of the buffer
;        RAM. /INCTX comes from the RAM SELECT PAL20RA10
;        U5. The binary counter Q0 - Q6 is synchronous
;        with carry enable signals CTY1 and CTY0 linking
;        the registers in the counter.
;
;
;

EQUATIONS
                                                    ;
Q0T             : = /Q0T                            ;Q0T LSB OF COUNT
Q0T.CLKF          = /INCTX                          ;INCREMENT
Q0T.SETF          = /D0*LD0                         ;LOAD LOW
Q0T.RSTF          = D0*LD0                          ;LOAD HIGH
Q0T.TRST          = INCTX                           ;HIGH - Z
                                                    ;
Q1T             : = /Q1T*Q0T                        ;TOGGLE Q1T
                  + Q1T*/Q0T                        ;HOLD Q1T
Q1T.CLKF          = /INCTX                          ;INCREMENT
Q1T.SETF          = /D1*LD0                         ;LOAD LOW
Q1T.RSTF          = D1*LD0                          ;LOAD HIGH
Q1T.TRST          = INCTX                           ;HIGH - Z
                                                    ;
Q2T             : = /Q2T*Q0T*Q1T                    ;TOGGLE Q2T
                  + Q2T*/Q1T                        ;HOLD Q2T
                  + Q2T*/Q0T                        ;HOLD Q2T
Q2T.CLKF          = /INCTX                          ;INCREMENT
Q2T.SETF          = /D2*LD0                         ;LOAD LOW
Q2T.RSTF          = D2*LD0                          ;LOAD HIGH
Q2T.TRST          = INCTX                           ;HIGH - Z
                                                    ;
Q3T             : = /Q3T*Q2T*Q0T*Q1T                ;TOGGLE Q3T
                  + Q3T*/Q2T                        ;HOLD Q3T
                  + Q3T*/Q1T                        ;HOLD Q3T
                  + Q3T*/Q0T                        ;HOLD Q3T
Q3T.CLKF          = /INCTX                          ;INCREMENT
Q3T.SETF          = /D3*LD0                         ;LOAD LOW
Q3T.RSTF          = D3*LD0                          ;LOAD HIGH
Q3T.TRST          = INCTX                           ;HIGH - Z
                                                    ;
CTY0              = Q0T*Q1T*Q2T*Q3T                 ;CARRY TO
                                                    ;Q4T, Q5T Q6T
```

```
Q4T             := /Q4T*CTY0               ;TOGGLE Q4T
                 + Q4T*/CTY0               ;HOLD Q4T
Q4T.CLKF         = /INCTX                  ;INCREMENT
Q4T.SETF         = /D4*LD0                 ;LOAD LOW
Q4T.RSTF         = D4*LD0                  ;LOAD HIGH
Q4T.TRST         = INCTX                   ;HIGH - Z
                                           ;
Q5T             := /Q5T*Q4T*CTY0           ;TOGGLE QT5
                 + Q5T*/Q4T                ;HOLD QT5
                 + Q5T*/CTY0               ;HOLD QT5
Q5T.CLKF         = /INCTX                  ;INCREMENT
Q5T.SETF         = /D5*LD0                 ;LOAD LOW
Q5T.RSTF         = D5*LD0                  ;LOAD HIGH
Q5T.TRST         = INCTX                   ;HIGH - Z
                                           ;
Q6T             := /Q6T*Q5T*Q4T*CTY0       ;TOGGLE QT6
                 + Q6T*/Q5T                ;HOLD QT6
                 + Q6T*/Q4T                ;HOLD QT6
                 + Q6T*/CTY0               ;HOLD QT6
Q6T.CLKF         = /INCTX                  ;INCREMENT
Q6T.SETF         = /D6*LD0                 ;LOAD LOW
Q6T.RSTF         = D6*LD0                  ;LOAD HIGH
Q6T.TRST         = INCTX                   ;HIGH - Z
                                           ;
CTY1             = Q6T*Q5T*Q4T*Q3T*Q2T     ;CARRY FOR
                   *Q1T*Q0T                ;NEXT STAGE
                                           ;
SIMULATION                                 ;
TRACE_ON        /INCTX LD0                 ;TRACE ALL
                Q0T Q1T Q2T Q3T CTY0       ;SIGNALS.
                Q4T Q5T Q6T CTY1 OE /PL    ;
SETF            /LD0 D0 D1 D2 D3 D4        ;TEST LOAD
                D5 D6                      ;FUNCTION
                OE /PL INCTX               ;FOR ALL HIGH
SETF            LD0                        ;THEN ALL LOW.
SETF            /LD0 /D0 /D1 /D2 /D3       ;
                /D4 /D5 /D6                ;
SETF            LD0                        ;
SETF            /LD0                       ;DISABLE LOAD
FOR I := 1 TO 128 DO                       ;ENABLE COUNT
BEGIN                                      ;FOR 128 TEST
SETF      INCTX                            ;VECTORS.
SETF      /INCTX                           ;
END                                        ;
TRACE_OFF                                  ;
```

Figure 10. EEPLD Design Specification

Tx Counter Q7..Q12

```
TITLE           TXCOUNTER_Q7-Q12
PATTERN         U10
REVISION        04.
AUTHOR          PEER RESEARCH.
COMPANY         PEER RESEARCH.
DATE            30TH MAY 1988.
;
;
CHIP COUNTER PAL20RA10

;PINS   1       2       3       4       5       6
        /PL     /INCTX  NC      D7      D0      D1

;PINS   7       8       9       10      11      12
        D2      D3      D4      CTY1    LD1     GND

;PINS   13      14      15      16      17      18
        /OE     LD0     CTY2    Q7T     Q8T     Q9T

;PINS   19      20      21      22      23      24
        Q10T    Q11T    Q12T    RXTXEOFTXMODE   VCC

;       The transmit buffer counter outputs Q7T - Q12T
;       are the higher order address bits to Q0T - Q6T
;       registers from PAL20RA10 U9. Q7T is loaded from
;       the PC bus I/O location 309 and Q10T - Q12T is
;       loaded from D0 - D4 at I/O location 30A. The
;       outputs when enabled to count access locations
;       in the buffer RAM and are incremented by the
;       rising edge of /INCTX, when HIGH this signal
;       puts the output buffers into 3 - State.
;       The RXTXEOF goes active at the final count of the
;       counter, that is when registers Q0 - Q12
;       contain all logic HIGHs. The start location
;       of the data tranfer to RAM is loaded from the
;       PC bus. The RXTXEOF signal, when active informs
;       the EDLC device that a block of data has been
;       read from the buffer RAM and tranmitted by the
;       8003 EDLC device The 3 - State condition of RXTXEOF
;       is qualified by TXMODE (and input) and /INCTX.
;       This is because the EDLC RXTXEOF signal also serves
;       as an RXTXEOF output during receive activity. The
;       RXTXEOF line is connected to the RXTXEOF pin of the
;       8003 EDLC chip.
;
EQUATIONS
                                                  ;
Q7T             := /Q7T*CTY1                      ;TOGGLE Q7T
                 + Q7T*/CTY1                      ;HOLD Q7T
Q7T.CLKF         = /INCTX                         ;INCREMENT
Q7T.SETF         = /D7*LD0                        ;LOAD LOW
Q7T.RSTF         = D7*LD0                         ;LOAD HIGH
Q7T.TRST         = INCTX                          ;HIGH - Z
                                                  ;
Q8T             := /Q8T*Q7T*CTY1                  ;TOGGLE Q8T
                 + Q8T*/Q7T                       ;HOLD Q8T
                 + Q8T*/CTY1                      ;HOLD Q8T
Q8T.CLKF         = /INCTX                         ;INCREMENT
Q8T.SETF         = /D0*LD1                        ;LOAD LOW
Q8T.RSTF         = D0*LD1                         ;LOAD HIGH
Q8T.TRST         = INCTX                          ;HIGH - Z
                                                  ;
Q9T             := /Q9T*Q8T*Q7T*CTY1              ;TOGGLE Q9T
                 + Q9T*/Q8T                       ;HOLD Q9T
                 + Q9T*/Q7T                       ;HOLD Q9T
                 + Q9T*/CTY1                      ;HOLD Q9T
Q9T.CLKF         = /INCTX                         ;INCREMENT
Q9T.SETF         = /D1*LD1                        ;LOAD LOW
Q9T.RSTF         = D1*LD1                         ;LOAD HIGH
Q9T.TRST         = INCTX                          ;HIGH - Z
                                                  ;
CTY2             = Q9T*Q8T*Q7T*CTY1               ;CARRY TO
                                                  ;NEXT STAGE
```

```
Q10T             := /Q10T*CTY2             ;TOGGLE Q10T
                  + Q10T*/CTY2             ;HOLD Q10T
Q10T.CLKF         = /INCTX                 ;INCREMENT
Q10T.SETF         = /D2*LD1                ;LOAD LOW
Q10T.RSTF         = D2*LD1                 ;LOAD HIGH
Q10T.TRST         = INCTX                  ;HIGH - Z
                                           ;
Q11T             := /Q11T*Q10T*CTY2        ;TOGGLE Q11T
                  + Q11T*/Q10T             ;HOLD Q11T
                  + Q11T*/CTY2             ;HOLD Q11T
Q11T.CLKF         = /INCTX                 ;INCREMENT
Q11T.SETF         = /D3*LD1                ;LOAD LOW
Q11T.RSTF         = D3*LD1                 ;LOAD HIGH
Q11T.TRST         = INCTX                  ;HIGH - Z
                                           ;
Q12T             := /Q12T*Q11T*Q10T*CTY2   ;TOGGLE Q12T
                  + Q12T*/Q11T             ;HOLD Q12T
                  + Q12T*/Q10T             ;HOLD Q12T
                  + Q12T*/CTY2             ;HOLD Q12T
Q12T.CLKF         = /INCTX                 ;INCREMENT
Q12T.SETF         = /D4*LD1                ;LOAD LOW
Q12T.RSTF         = D4*LD1                 ;LOAD HIGH
Q12T.TRST         = INCTX                  ;HIGH - Z
                                           ;
RXTXEOF           = Q12T*Q11T*Q10T*Q9T     ;END OF FILE
                   *Q8T*Q7T*CTY1           ;ACTIVE HIGH
RXTXEOF.TRST      = TXMODE*INCTX           ;
                                           ;
SIMULATION                                 ;
TRACE_ON         INCTX LD1 LD0 Q7T         ;TRACE ALL
                 Q8T Q9T Q10T CTY2         ;SIGNALS
                 Q11T Q12T RXTXEOF         ;
                 TXMODE OE /PL             ;
SETF             /LD1 /LD0 INCTX           ;TEST FOR
                 D7 D0 D1 D2 D3 D4         ;LOADING OF
                 CTY1 TXMODE OE /PL        ;REGISTERS
SETF             LD1 LD0                   ;Q7T - Q12T
SETF             /LD1 /LD0 /D7 /D0         ;ENABLE LOAD
                 /D1 /D2 /D3 /D4           ;ALL HIGH
SETF             LD1 LD0                   ;THEN ALL LOW
SETF             /LD1 /LD0 /INCTX          ;DISABLE LOAD
FOR I := 1 TO 64 DO                        ;ENABLE COUNT
BEGIN                                      ;FOR 64 CLOCK
SETF      INCTX                            ;PULSES.
SETF      /INCTX                           ;
END                                        ;
TRACE_OFF                                  ;
```

Figure 11. PASCAL Software Source

```
program EDLC;     {  EDLC Hello Test  }
{ Turbo Pascal Source Listing for PC/XT/AT 5/1/88 }
uses crt;
type
 Str2 = string[2]; Str4 = string[4];
 Frame = record
  DestinationAddress, SourceAddress : array[1..6] of byte;
  ByteCount : array[1..2] of byte;
  Data : array[1..46] of byte;
 end;
```

Variable Declaration

```
var TransmitFrameBuffer, ReceiveFrameBuffer : Frame;
 ReadByte, Rx2kBank, TestData, TestData1 : byte;
 InKey, OutChar, Select : char;
 TxCount, TxFail, RxCount, RxFail : word; i : integer;
 Address, LastAddress, ReadWord : word;
 Fail, InhibitMessage : boolean;
```

Constants

```
const
 EDLCStationAddress          = $300;
 EDLCReceive                 = $306;
 EDLCTransmit                = $307;
 Command                     = $308;
 LoadTransmitCounter0        = $309;
 LoadTransmitCounter1        = $30A;
 FifoData                    = $30C;

 ResetEDLC                   = $01;
 ResetRxCounter              = $02;
 SetEDLClpbk                 = $04;
 SetTxMode                   = $08;
 ResetTxMode                 = $00;
 ResetAllCommands            = $00;
 NoCommand                   = $00;

 StartTransmitCommand        = $08;
 TransmissionSuccess         = $08;
 StartReceiveCommand         = $E0;
 ReceivedGoodFrame           = $20;
 OldTransmitStatus           = $80;
 OldReceiveStatus            = $80;
 ResetStatus                 = $80;

 TestStationAddress : array[1..6] of byte = (00,11,22,33,44,55);
 TestFrame : Frame =
  (DestinationAddress : (00,11,22,33,44,55);
   SourceAddress :    (00,11,22,33,44,55);
   ByteCount :        (46,00);
   Data :
   (00,01,02,03,04,05,06,07,08,09,10,11,12,13,14,15,
    16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,
    32,33,34,35,36,37,38,39,40,41,42,43,44,45) );

 ESC = #27; CR = #13; BKSP = #08;
```

Misc. Functions

```
function UpCase(inchar : char): char;
begin
if inchar in ['a'..'z'] then Upcase := chr( ord(inchar) and $DF)
else UpCase := inchar;
end;

function h(number : integer) : char; begin
   case number of 0:h:='0';1:h:='1';2:h:='2';3:h:='3';4:h:='4';5:h:='5';
   6:h:='6';7:h:='7';8:h:='8';9:h:='9';10:h:='A';11:h:='B';12:h:='C';
   13:h:='D';14:h:='E';15:h:='F';end; end;

function HexByte(Number : byte) : str2;
 begin  HexByte :=  h((Number shr 4) and 15)+h((Number) and 15) ; end;

function HexWord(Number : byte) : str4;
 begin HexWord :=  h((Number shr 12) and 15)+h((Number shr  8) and 15)
  +h((Number shr  4) and 15)+h((Number) and 15); end;
```

Screen Functions

```
procedure ClearScreen(Color : Word);
begin
 TextBackGround(Color);
 clrscr;
end;
```

Figure 11. PASCAL Software Source

PC/XT/AT
I/O Port
Bus Instructions

RAM
Test
Procedures

```
function Match(Mask, Arg : byte) : boolean;
begin  Match := not ((Mask and Arg) = 0 ); end;

procedure WritePCBus(Address : word; Data : byte);
begin port[Address] := Data; end;

function ReadPCBus(Address  : word) : byte;
begin ReadPCBus := port[Address]; end;

procedure ClearRAM;
var i,j : integer;
begin
 WritePCBus(LoadTransmitCounter0, 0);
 WritePCBus(LoadTransmitCounter1, 0);
 for j := 1 to 8192 do WritePCBus(FifoData, 0 );
end;

procedure DumpRAM;
var i,j,k : integer;
begin
 WritePCBus(LoadTransmitCounter0, 0);
 WritePCBus(LoadTransmitCounter1, 0);
 k := 0;
 while (not(k = 16)) and not(InKey = ESC) do
  begin
  for j := 0 to 15 do
  begin
   write((k*512+j*32):4, ' ');
   for i := 0 to 31 do Write(HexByte(ReadPCBus(FifoData))); writeln('');
  end;
  writeln(''); k := k + 1; InKey := ReadKey;
 end;
end;

procedure WriteInRAM(Address : word);  var i : integer;
begin
 WritePCBus(LoadTransmitCounter0, Lo(Address));
 WritePCBus(LoadTransmitCounter1, Hi(Address));
 write('   ', Address:5, ' ');
 for i := 0 to 31 do Write(HexByte(ReadPCBus(FifoData)));
 writeln('');
end;

procedure DumpRAMPackets;  var i : integer;
begin
writeln (''); WriteInRAM(0000); WriteInRAM(0032);
writeln (''); WriteInRAM(2048); WriteInRAM(2080);
writeln (''); WriteInRAM(4096); WriteInRAM(4128);
writeln (''); WriteInRAM(8128); WriteInRAM(8160);
end;

procedure LoadStationAddress; var i : integer;
begin
 for i := 1 to 6 do
  WritePCBus(EDLCStationAddress + i-1, TestStationAddress[i]);
end;

Function ReceiveEqualTransmit : boolean;
type Fb=array[1..60] of byte; var TfPtr, RfPtr : ^Fb; i : integer;
begin
 ReceiveEqualTransmit := true; RfPtr: =addr(ReceiveFrameBuffer);
 TfPtr: =addr(TransmitFrameBuffer);
 for i := 1 to 60 do if not(RfPtr^[i] = TfPtr^[i]) then
ReceiveEqualTransmit := false;
end;

procedure InitialTransmitFrameBuffer; var i : integer;
begin
for i := 1 to 46 do if TestData=$11 then
TransmitFrameBuffer.Data[i]: =random(255)
  else TransmitFrameBuffer.Data[i] := Testdata;
end;

procedure InitializeEDLC;
begin
 WritePCBus(Command, ResetEDLC + ResetRxCounter);
 WritePCBus(Command, ResetAllCommands);
 ClearRAM;
```

Figure 11. PASCAL Software Source

```
 Rx2kBank := 0;
 LoadStationAddress;
 WritePCBus(EDLCReceive, StartReceiveCommand);
 WritePCBus(EDLCTransmit, StartTransmitCommand);
end;
```

RAM Tests Continued

```
procedure Initialize;
begin
 TxCount := 1; RxCount := 0;
 TxFail := 0; RxFail := 0;
 Randomize;
 Inkey := ' ';
 TransmitFrameBuffer := TestFrame;
 InitialTransmitFrameBuffer;
 InitializeEDLC;
 gotoxy(20, 2); write('SEEQ 8003 EDLC Demonstration V1.0');
end;

procedure RAMTest;
begin
 InKey := '?'; Fail := false;  LastAddress := 4095;
 Initialize;
 gotoxy(1, 3);
 while not (InKey = ESC )do
  begin
  WritePCBus(Command, ResetEDLC);
  WritePCBus(Command, ResetAllCommands);
  WritePCBus(LoadTransmitCounter0, 0);
  WritePCBus(LoadTransmitCounter1, 0);
  for Address := 0 to LastAddress do
   begin
   WritePCBus(FifoData, Hi(Address)); { write(H( Lo(Address)), '  ');}
   WritePCBus(FifoData, Lo(Address)); { write(H( Hi(Address)), '  ');}
   end;
  WritePCBus(LoadTransmitCounter0, 0);
  WritePCBus(LoadTransmitCounter1, 0);
  Address := 0;
  while  not (Address = LastAddress + 1) and
      not (InKey = ESC ) do
   begin
   ReadWord := ReadPCBus(FifoData);
   ReadByte := ReadPCBus(FifoData);
   ReadWord := swap(ReadWord) + ReadByte;;
   if not(ReadWord = Address) then
    begin
    writeln('Address = ', HexWord(Address),
        ' Read DATA = ', HexWord(ReadWord) );
    InKey := readkey; Fail := true;
    end;
   Address := Address + 1;
   end;
  if keypressed then InKey := readkey;
  if Fail then writeln('Fail RAM Test')
  else      writeln('Pass RAM Test');
  end;
end;
```

Receive Frame

```
procedure ReceiveFrame;
var i : integer;
begin
 WritePCBus(LoadTransmitCounter0, 0);
 WritePCBus(LoadTransmitCounter1, Rx2kBank*8);
 with ReceiveFrameBuffer do
 begin
 for i:=1 to 6 do  DestinationAddress[i]:=ReadPCBus(FifoData);
 for i:=1 to 6 do  SourceAddress[i]  :=ReadPCBus(FifoData);
 for i:=1 to 2 do  ByteCount[i] :=ReadPCBus(FifoData);
 for i:=1 to 46 do  Data[i]  :=ReadPCBus(FifoData);
 end;
 if Rx2kBank = 2 then Rx2kBank := 0
 else Rx2kBank := Rx2kBank + 1;
end;
```

Transmit Frame

```
procedure TransmitFrame(CurrentMode : byte);
var i : integer;
begin
 WritePCBus(LoadTransmitCounter0, $C4);
 WritePCBus(LoadTransmitCounter1, $FF);
```

Figure 11. PASCAL Software Source

```
 with TransmitFrameBuffer do
 begin
 for i: = 1 to 6  do  WritePCBus(FifoData,DestinationAddress[i] );
 for i: = 1 to 6  do  WritePCBus(FifoData, SourceAddress[i] );
 for i: = 1 to 2  do  WritePCBus(FifoData, ByteCount[i] );
 for i: = 1 to 46 do  WritePCBus(FifoData, Data[i] );
 end;
 WritePCBus(LoadTransmitCounter0, $C4);
 WritePCBus(LoadTransmitCounter1, $FF);
 WritePCBus(Command, SetTxMode + CurrentMode);
end;
```

Read Character

```
procedure ReadCharacter;
var SaveX,SaveY : byte;
begin
 while not keypressed do
 begin
 ReadByte : = ReadPCBus(EDLCReceive);
 if not Match( OldReceiveStatus, ReadByte) then
  begin
   SaveX : = whereX;  SaveY : = whereY;
   gotoxy(3,10);
   write('Receive  Status  = ', HexByte(Readbyte), '  ');
   ReceiveFrame;
   gotoxy(3,6);
   write('Receive  Message ');
   i : =  1;
   repeat
    if i  =  1 then clreol;
    OutChar : =  (chr(ReceiveFrameBuffer.Data[i]));
    if OutChar in ['0'..'9', 'a'..'z', 'A'..'Z','.',',',' '] then write(OutChar);
    i : = i  + 1;
   until (i  =  47)  or (OutChar  =  CR) or  (OutChar  =  ESC);
   gotoxy(1,13);  DumpRAMPackets;
   gotoxy(SaveX,SaveY);
  end;
 end;
 InKey : =  readkey;
end;
```

Hello Hello

```
procedure HelloHello;
var i : integer;
begin
 Initialize; InKey : =  '?';
 while not (InKey  =  ESC) do
begin
 gotoxy(3,4);   clreol;
 write('Transmit Message ');
 i : =  1;
 repeat
  ReadCharacter;
  if InKey in ['0'..'9', 'a'..'z', 'A'..'Z','.',',',' '] then
  begin
   write(InKey);
   TransmitFrameBuffer.Data[i] : =  ord(InKey);
   i : = i  +  1;
  end;
  if (InKey  =  BKSP) and not (i  =  1) then
  begin
   write(BKSP); write(' '); write(BKSP);
   i : =  i - 1;
   TransmitFrameBuffer.Data[i] : =  ord(' ');
  end;
 until (i  =  47) or (InKey  =  CR) or (InKey  =  ESC);
 while not (i  =  47) do
 begin
  TransmitFrameBuffer.Data[i] : =  0;
  i : = i  +  1;
 end;
 TransmitFrame(NoCommand);
 ReadByte : =  OldTransmitStatus;
 i : =  1;
 while Match(OldTransmitStatus , ReadByte) and not (i  =  1000)  do
 begin
  ReadByte : =  ReadPCBus(EDLCTransmit); i : =  i  +  1;
 end;
 WritePCBus(Command, ResetTxMode);
 gotoxy(3,8);
```

Figure 11. PASCAL Software Source

```
 write('Transmit Status = ', HexByte(Readbyte), '  ');
 TxFail := TxFail + 1;
 gotoxy(1,13);
 DumpRAMPackets;
end;
end;
```

Display Frame

```
Procedure WriteFrame(Buffer : Frame);
type Fb=array[1..60] of byte; var RfPtr : ^Fb; i : integer;
begin RfPtr:=addr(Buffer); for i := 1 to 14 do
  write(HexByte(RfPtr^[i]), ' '); writeln('');
 for i := 15 to 37 do
  write(HexByte(RfPtr^[i]), ' '); writeln('');
 for i := 38 to 60 do
  write(HexByte(RfPtr^[i]), ' '); writeln('');
end;
```

Wait for Status

```
procedure WaitWhile(Device : word; Status : byte);
var i : integer;
begin
 ReadByte := Status;
 i := 1;
 while Match(Status , ReadByte) and not (i = 10000) do
 begin
  ReadByte := ReadPCBus(Device); i := i + 1;
 end;
 write (HexByte(Readbyte), ':');
end;
```

Echo Frame

```
procedure EchoFrames;
var i : integer;
begin
 Initialize;
 while not(InKey = ESC) do
 begin
  gotoxy(1,13);
  ReadByte := OldReceiveStatus;
  while Match(OldReceiveStatus , ReadByte) and not keypressed do
   ReadByte := ReadPCBus(EDLCReceive);
  write (HexByte(Readbyte), ':');
  if Match( ReceivedGoodFrame, ReadByte ) then
   writeln('Receive Good Frame') else
   begin
    writeln('Receive Fail       '); RxFail := RxFail + 1;
   end;
  ReceiveFrame; TransmitFrameBuffer := ReceiveFrameBuffer;
  if not InhibitMessage then WriteFrame(TransmitFrameBuffer);
  writeln('');
  TransmitFrame(NoCommand);
  WaitWhile(EDLCTransmit, OldTransmitStatus);
  WritePCBus(Command, ResetTxMode);
  if Match( TransmissionSuccess, ReadByte )
   then writeln('Transmit Successful') else
   begin
    writeln('Transmit Fail'); RxFail := RxFail + 1;
   end;
  writeln('');
  Write('Count = ', TxCount, '  RxFail = ', RxFail,'          ');
  TxCount := TxCount + 1;
  if keypressed then InKey := readkey;
 end;
end;
```

LoopBack Test

```
procedure LoopBackTest(CurrentMode : byte); var i : integer;
begin
 Initialize;
 WritePCBus(Command, CurrentMode);
 while not(InKey = ESC) do
 begin
  gotoxy(1,13);
  TransmitFrame(CurrentMode);
  WaitWhile(EDLCTransmit, OldTransmitStatus);
  WritePCBus(Command, ResetTxMode + CurrentMode); clreol;
  if Match( TransmissionSuccess, ReadByte )
    then writeln('Transmission Successful')
  else writeln('Transmission Fail');
  if not InhibitMessage then WriteFrame(TransmitFrameBuffer);
  writeln(''); WaitWhile(EDLCReceive, OldReceiveStatus);
```

Figure 11. PASCAL Software Source

LoopBack Test Continued

```
  if Match( ReceivedGoodFrame, ReadByte ) then
  begin
   ReceiveFrame;  writeln('Receive Good Frame');
   if not InhibitMessage then WriteFrame(ReceiveFrameBuffer);
   if ReceiveEqualTransmit  then
   begin  if CurrentMode = SetEDLCLpbk then
        write('EDLC Loopback Test Pass')
    else write('EDLC Transmit Test Pass');
   end
   else
   begin
   if CurrentMode = SetEDLCLpbk then write('EDLC Loopback Test Fail')
   else write('EDLC Transmit Test Fail');
   RxFail := RxFail + 1; InitializeEDLC;
   end;
 end
  else
  begin writeln('Receive Fail     '); writeln('');
   if not InhibitMessage then begin Writeln(''); Writeln(''); Writeln(''); end;
  end;
  writeln('');
  clreol; Write('  TxCount = ', TxCount, '   RxFail = ', RxFail, '  ');
  TxCount := TxCount + 1;  InitialTransmitFrameBuffer;
  if keypressed or (InKey = ' ') then InKey := readkey;
 end;
end;
```

Main Program

```
begin {main program}
 Initialize;
 TextColor(Yellow);  InhibitMessage := false; TestData := $11; Select := '?';
 while not (Select = ESC) do
 begin
```

Menu Display

```
  ClearScreen(Blue); InKey := '?';
  gotoxy(20, 2);  write('SEEQ 8003 EDLC Demonstration V1.0');
  gotoxy(25, 5);  write('H - Hello Hello');
  gotoxy(25, 6);  write('L - Loop Back Test');
  gotoxy(25, 7);  write('T - Transmit Data Frames');
  gotoxy(25, 8);  write('E - Echo Frames');
  gotoxy(25, 9);  write('R - RAM Test');
  gotoxy(25,10);  write('D - Dump RAM');
  gotoxy(25,11);  write('B - Dump RAM Brief');
  gotoxy(25,12);  if not InhibitMessage then
                  write('I - Messages = ON') else  write('I - Messages = OFF');
  gotoxy(25,13);  case TestData of
       $11: write('C - Data = Random');   $00: write('C - Data = hex00');
       $55: write('C - Data = hex55');      $AA: write('C - Data = hexAA');
       $FF: write('C - Data = hexFF'); end;
  gotoxy(25,14);  write('Esc - Quit to DOS');
  gotoxy(25,16);  if Select = '#' then
          begin sound(400); delay(10);
          write('ERROR!, enter new selection');  nosound;
          end
          else
          write('enter selection');
  Select := UpCase(readkey);
  ClearScreen(red);
```

Menu Calls

```
  case Select of
  'H': HelloHello;
  'L': LoopBackTest(SetEDLCLpbk);
  'T': LoopBackTest(NoCommand);
  'E': EchoFrames;
  'R': RAMTest;
  'D': DumpRAM;
  'B': begin gotoxy(1,13); DumpRAMPackets; InKey := readkey; end;
  'I': InhibitMessage := not InhibitMessage;
  'C': begin case TestData of $11: TestData1 := $00;
      $00: TestData1 := $55;$55: TestData1 := $AA;
      $AA: TestData1 := $FF;
      $FF: TestData1 := $11;
      end;
     TestData := TestData1
     end;
  ESC: write('Quit');
  else Select := '#'
  end; {case}
 end;
 ClearScreen(Black);
end.
```

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ABEL is a trademark of DATA I/O Corporation.

CUPL is a trademark of Logical Devices Inc.

MINC is a trademark of MINC.

Turbo PASCAL 4.0 is a trademark of Borland International Inc.

9

GENERAL INFORMATION

Thermal Resistance of SEEQ Products

March 1987

LEAD COUNT	PACKAGE TYPE	$\emptyset_{JA}$ (C/WATTS)	Θ_{JC} (C/WATTS)
20	CERDIP (300 MILS)	60	22
	PLCC	60	UE
24	CERDIP (600 MILS)	58	21
	PLASTIC DIP (600 MILS)	49	UE
28	CERDIP (600 MILS)	45 — 55	21
	PLASTIC DIP (600 MILS)	40 — 50	UE
32	LCC	50 — 65	18
	PLCC	58	UE
40	CERDIP (600 MILS)	42	18

NOTES: 1. Actual Thermal Resistance of a given device may vary from the value on the table, this table contains the representative values for the package types specified.

2. All plastic package data refers to CU leadframe material.

3. All values are for socketed units.

4. UE = Under evaluation
LCC = Leadless Chip Carrier
DIP = Dual-In Line Package
PLCC = Plastic Leaded Chip Carrier

Packaging Information

SEEQ Plastic Packages Incorporate:

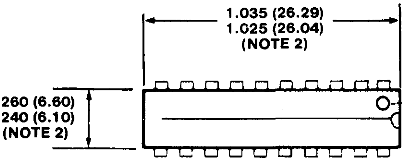
- High thermal conductivity copper leadframe.
- Silver-filled epoxy die attach material.
- Gold bond wires.
- Low stress, moisture-resistant molding compound.

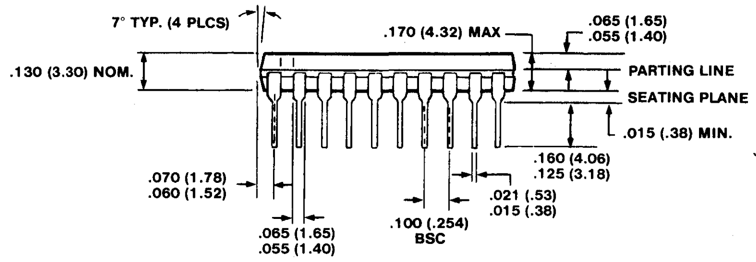
SEEQ Cerdip Packages Incorporate:

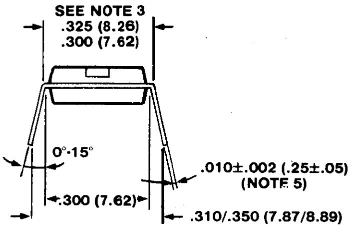
- Thermal conductivity Alumina substrates.
- Gold Silicon Eutectic die attach.
- Alloy 42 leadframe.
- Aluminum bond wires.

PLASTIC DUAL-IN-LINE PACKAGES

20 LEAD PLASTIC PACKAGE TYPE P



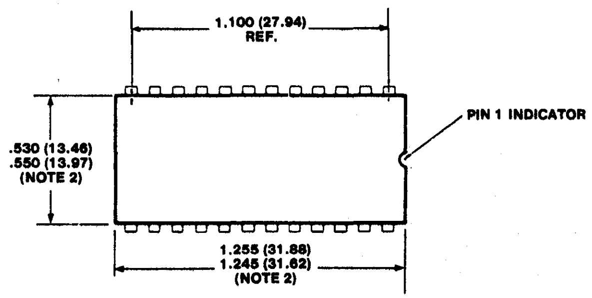


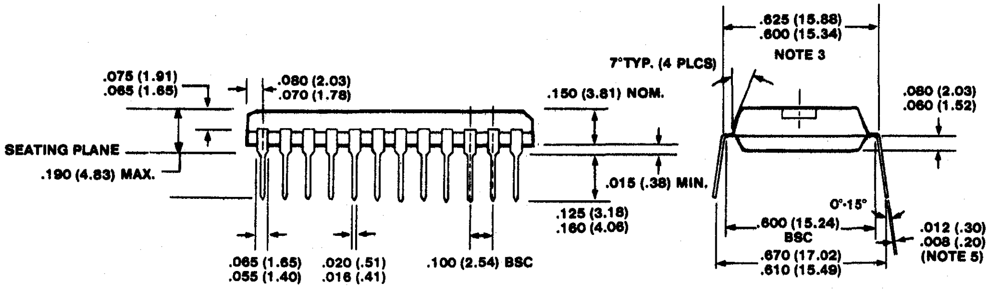


NOTES
1. **All dimensions are in inches and (millimeters).**
2. **Dimensions do not include mold flash. Max. allowable mold flash is .010 (.25).**
3. **Dimension is measured from shoulder to shoulder**
4. **Tolerances are ± .010 (.25) unless otherwise specified.**
5. **For solder dipped leads, thickness will be .020 (.51) max.**

PLASTIC DUAL-IN-LINE PACKAGES

24 LEAD PLASTIC PACKAGE TYPE P

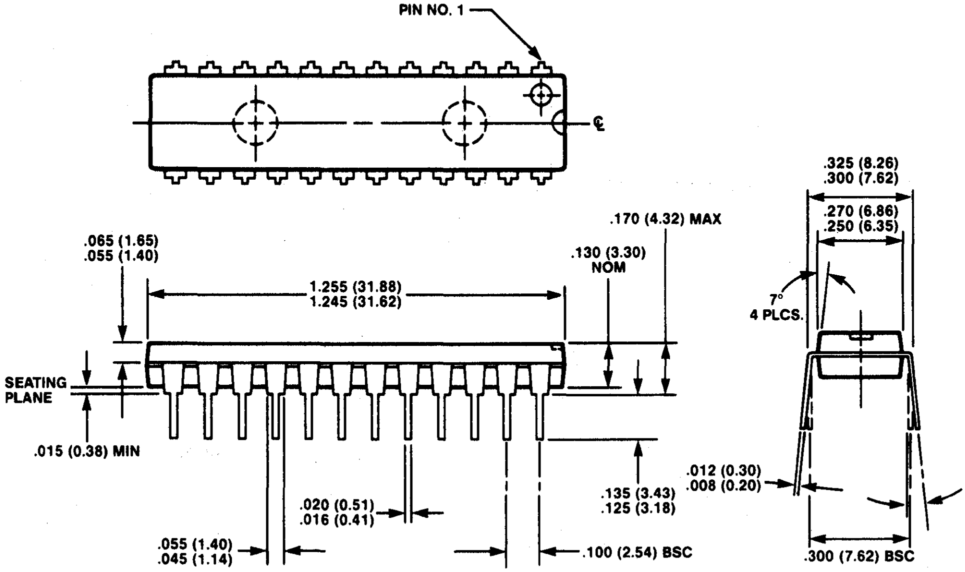




NOTES
1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Max. allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder
4. Tolerances are ± .010 (.25) unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

PLASTIC DUAL-IN-LINE PACKAGES

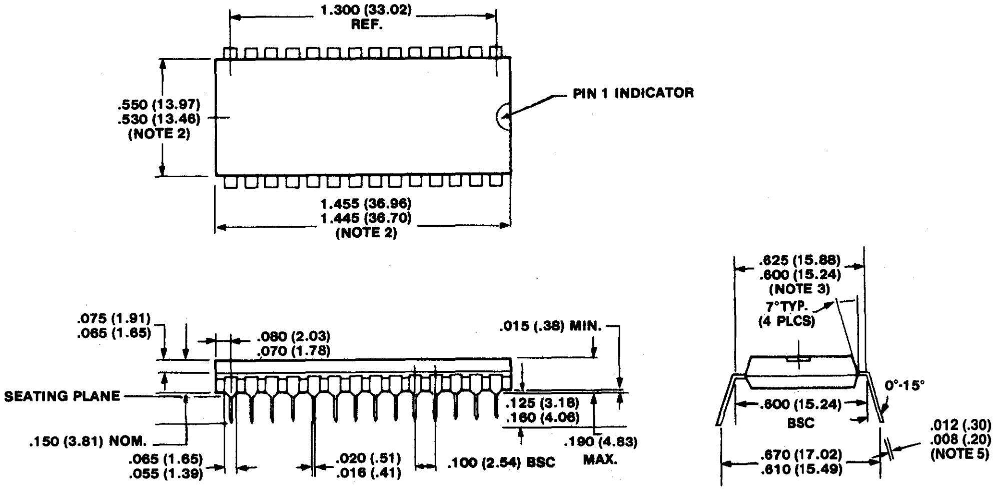
24-LEAD SLIM PLASTIC PACKAGE TYPE P



NOTES:
1. All dimensions in inches and (millimeters).
2. Dimensions do not include mold flash. Maximum allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder.
4. Tolerances are ± .010 (.25) unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

PLASTIC DUAL-IN-LINE PACKAGES

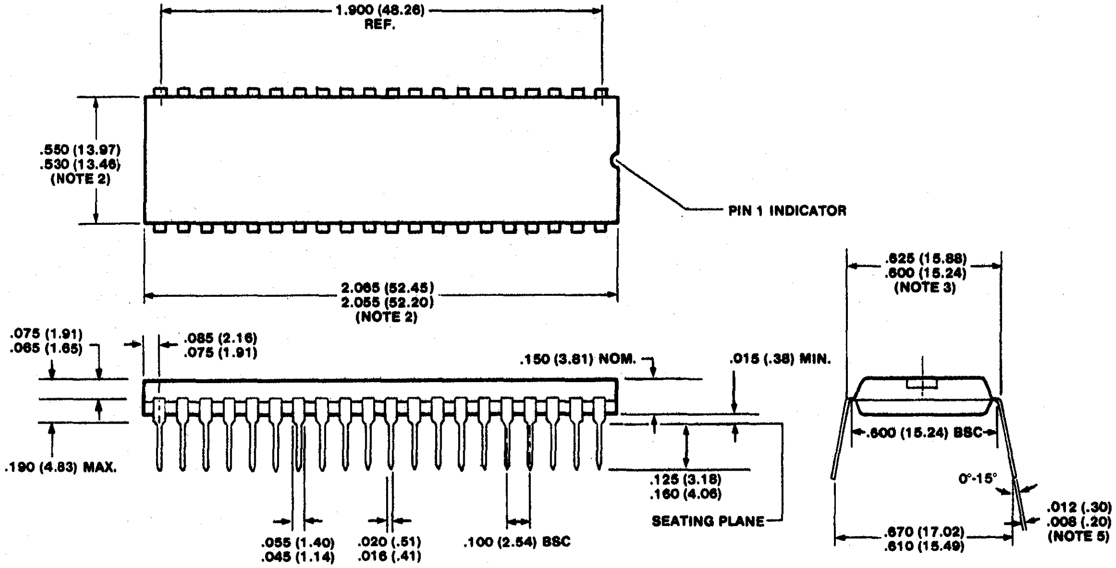
28 LEAD PLASTIC PACKAGE TYPE P



NOTES
1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Max. allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder.
4. Tolerances are ± .010 (.25) unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

PLASTIC DUAL-IN-LINE PACKAGES

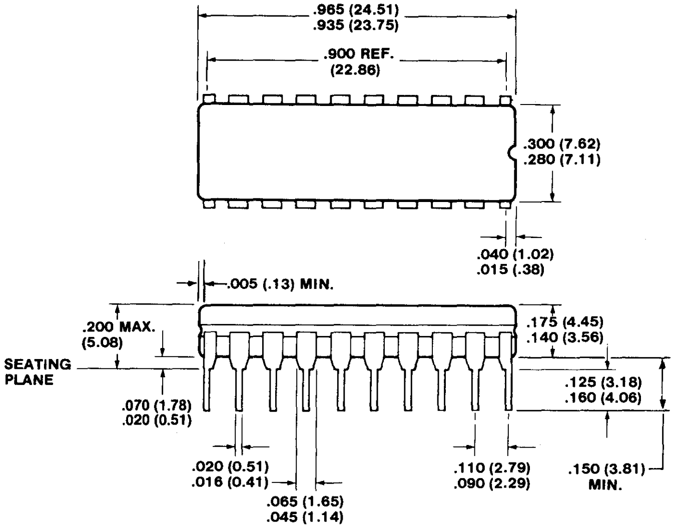
40 LEAD PLASTIC PACKAGE TYPE P

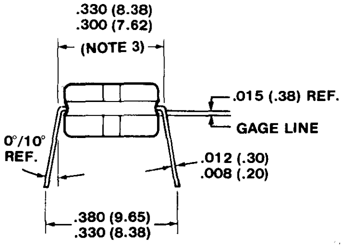


NOTES
1. All dimensions in inches and millimeters).
2. Dimensions do not include mold flash. Allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder.
4. Tolerances are ± .010 (.25) unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

CERAMIC DUAL-IN-LINE PACKAGES

20 LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D



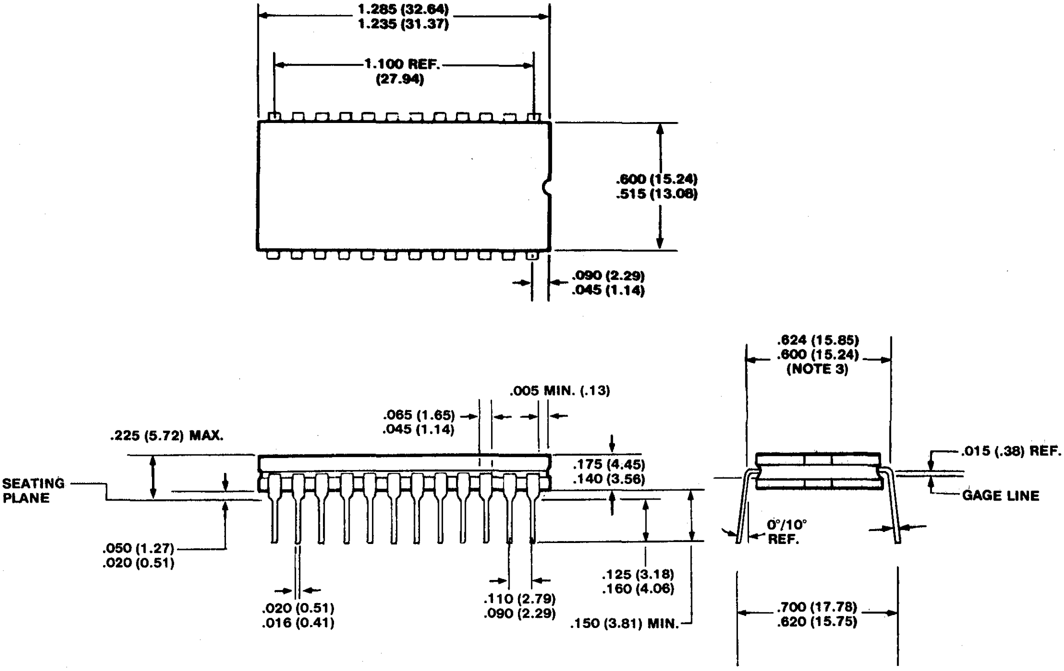


NOTES

1. For solder dipped leads, thickness will be .020 max.
2. All dimensions in inches and (millimeters).
3. Dimension is measured from outside shoulder to shoulder. This complies with Mil-M-38510, Appendix C, Dimension E_2 on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .290 (7.37) max. .320 (8.13).

CERAMIC DUAL-IN-LINE PACKAGES

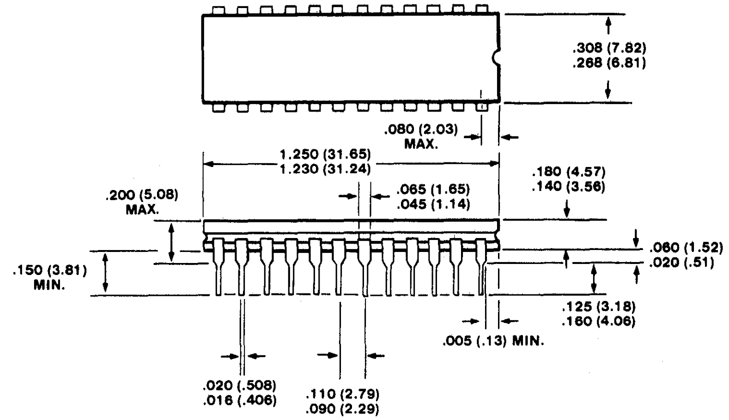
24 LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D

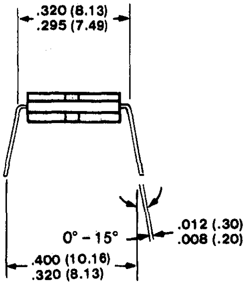


NOTES
1. All dimensions in inches and (millimeters).
2. For solder dipped leads, thickness will be .020 (.51) max.
3. Dimension is measured from outside shoulder-to-shoulder. This complies with Mil-M-38510, Appendix C, Dimension E_2 on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .590 (14.99) max. .620 (15.75).

CERAMIC DUAL-IN-LINE PACKAGES

24-LEAD HERMATIC SLIM CERAMIC PACKEGE TYPE D

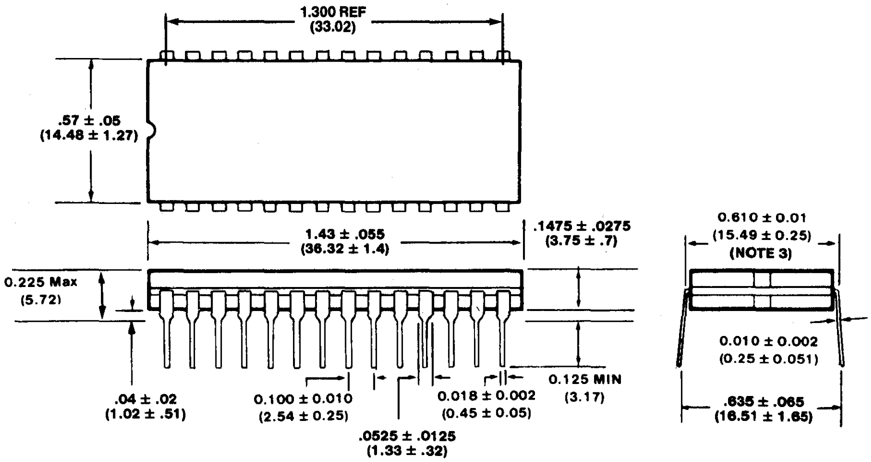




NOTES
1. For solder dipped leads, thickness will be .020 max.
2. All dimensions in inches and (millimeters).
3. Dimension is measured from outside shoulder-to-shoulder. This complies with Mil-M-38510, Appendix C, Dimension E_2 on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .290 (7.37) max. .320 (8.13).

CERAMIC DUAL-IN-LINE PACKAGES

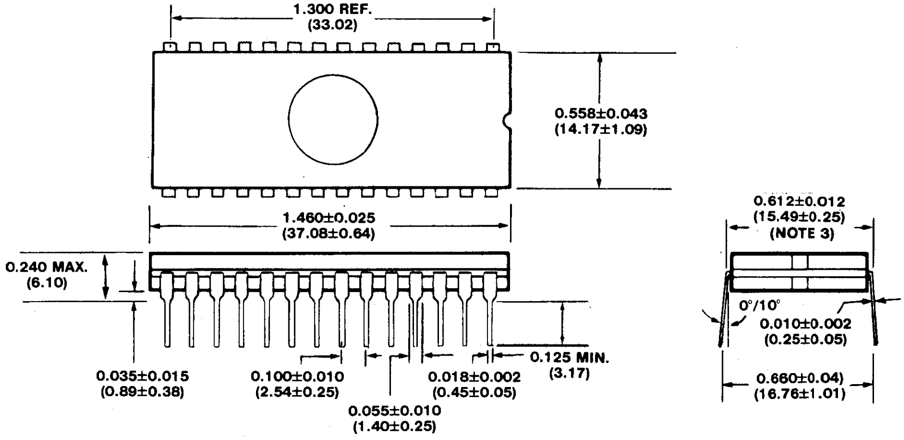
28-LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D



NOTES
1. All dimensions in inches and (millimeters).
2. For solder dipped leads, thickness will be .020 (.51) max.
3. Dimension is measured from outside shoulder-to-shoulder. This complies with Mil-M-38510, Appendix C, Dimension E_2 on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .590 (14.99) max. .620 (15.75).

CERAMIC DUAL-IN-LINE PACKAGES

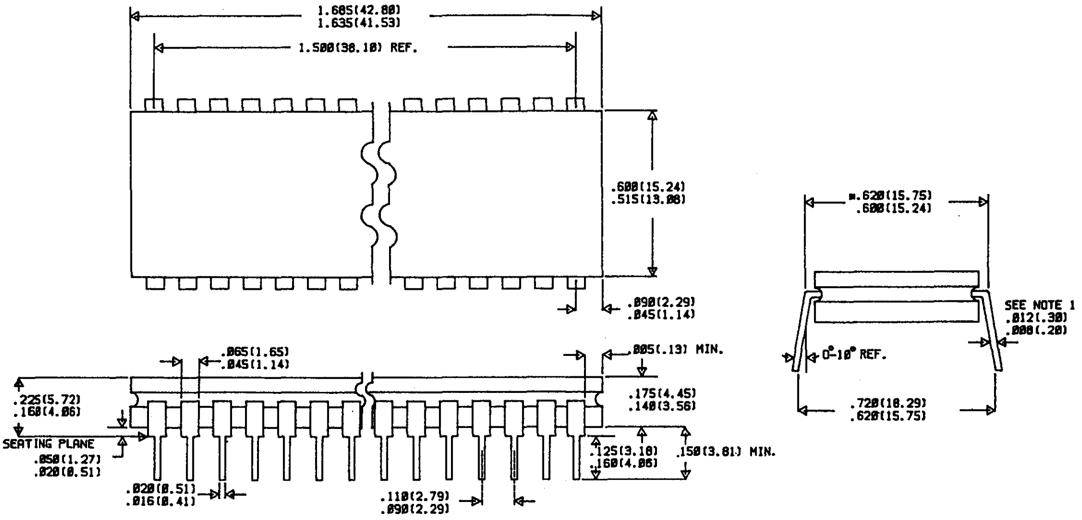
28 LEAD HERMETIC WINDOWED CERAMIC DIP PACKAGE TYPE D



NOTES
1. All dimensions in inches and (millimeters).
2. For solder dipped leads, thickness will be .020 (.51) max.
3. Dimension is measured from outside shoulder-to-shoulder. This complies with Mil-M-38510, Appendix C, Dimension E_2 on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .590 (14.99) max. .620 (15.75).

CERAMIC DUAL-IN-LINE PACKAGES

32-LEAD HERMATIC CERAMIC DIP PACKAGE TYPE D

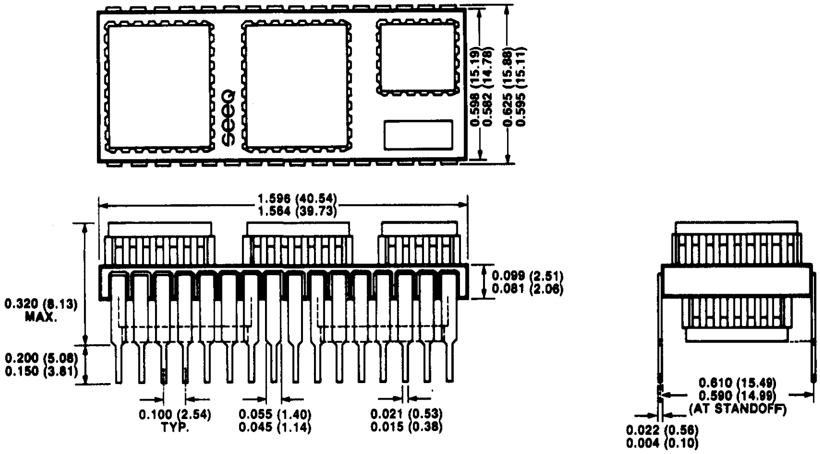


NOTES:

1. FOR SOLDER DIPPED LEADS, THICKNESS WILL BE .020 MAX.
2. ALL DIMENSIONS IN INCHES AND (MILLIMETERS).
3. * DIMENSION IS MEASURED FROM OUTSIDE SHOULDER TO SHOULDER.

CERAMIC DUAL-IN-LINE PACKAGES

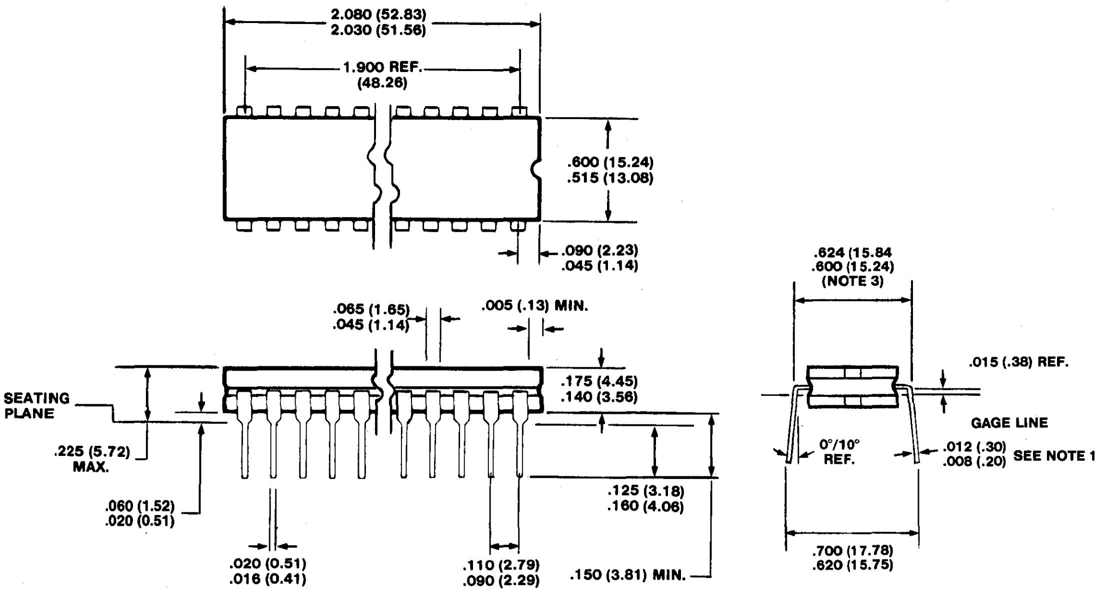
32-PIN CERAMIC SUBSTRATE MODULE TYPE M



NOTE: All dimensions in inches (millimeters).

CERAMIC DUAL-IN-LINE PACKAGES

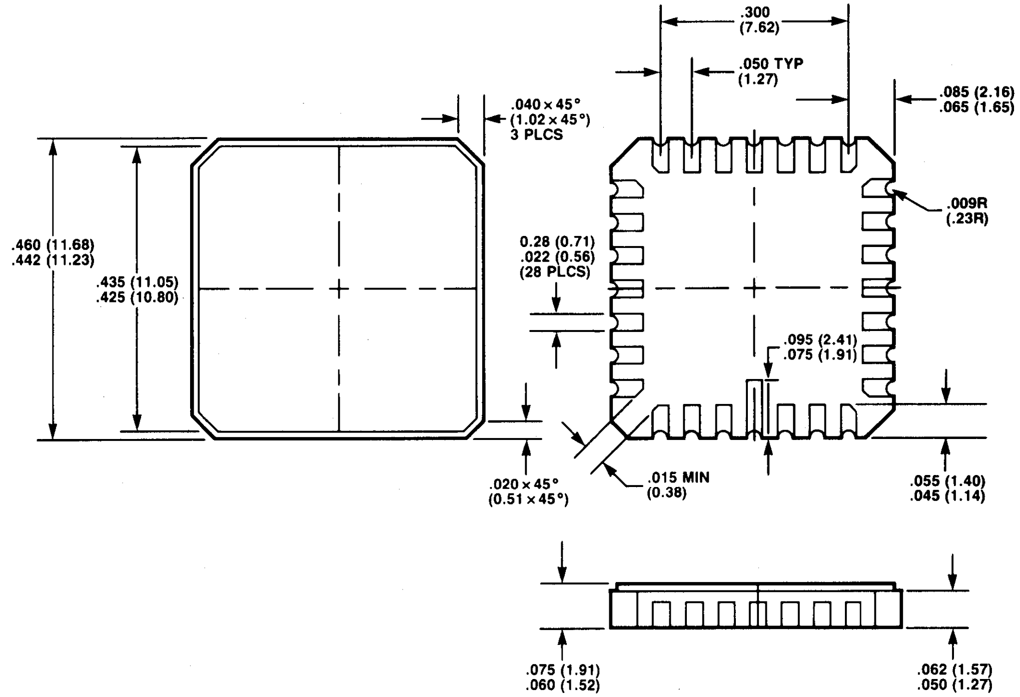
40 LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D



NOTES
1. For solder dipped leads, thickness will be .020 max.
2. All dimensions in inches and (millimeters).
3. Dimension is measured from outside shoulder to shoulder. This complies with Mil-M-38510, Appendix C, Dimension E_2 on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .590 (14.99) max. .620 (15.75).

SURFACE MOUNT PACKAGES

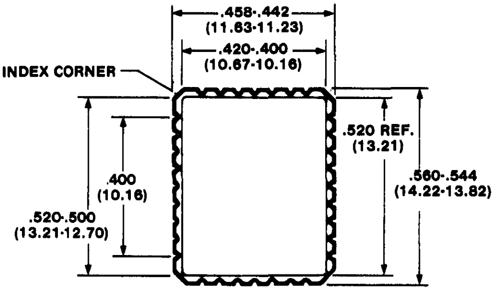
28-PIN CERAMIC LEADLESS CHIP CARRIER TYPE L

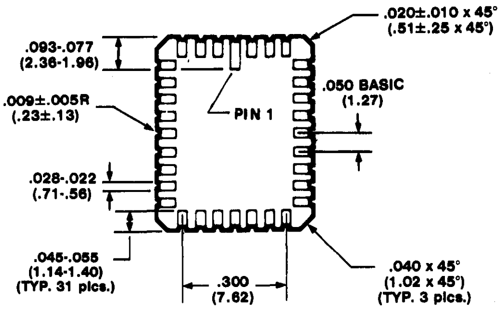


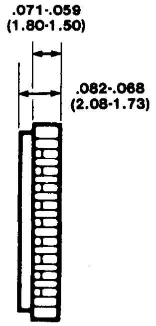
Notes:
1. All dimensions in inches and (millimeters).
2. All tolerences shall be ±0.010 (0.25) unless otherwise specified.

SURFACE MOUNT PACKAGES

32 PIN CERAMIC LEADLESS CHIP CARRIER TYPE L



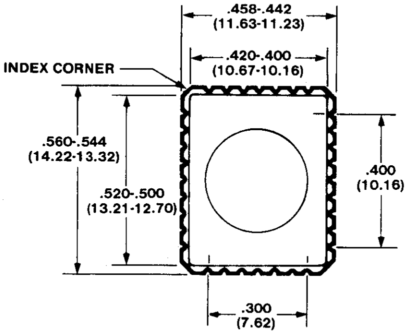


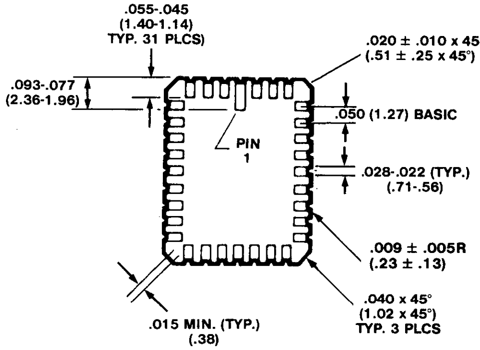


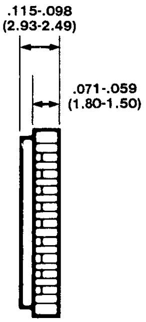
NOTES
1. All dimensions in inches and (millimeters).
2. All tolerances shall be ± .010 (.25) unless otherwise specified.

SURFACE MOUNT PACKAGES

32 PIN WINDOWED CERAMIC LEADLESS CHIP CARRIER TYPE L



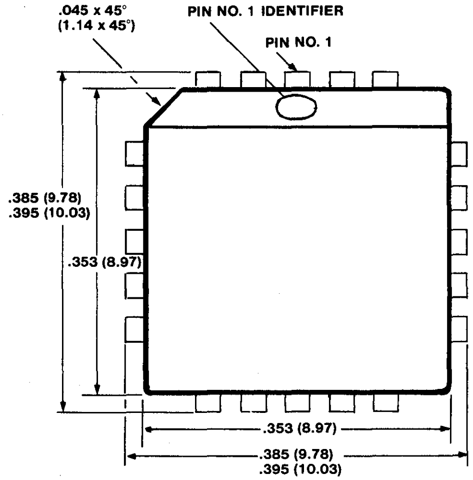


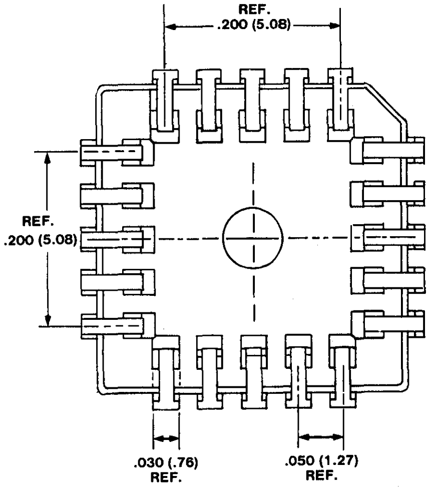


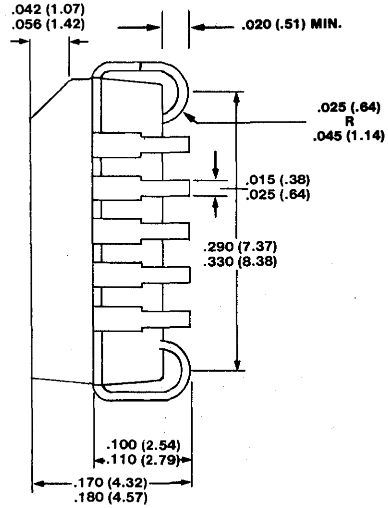
NOTES
1. All tolerances shall be ± .010 (.25) unless otherwise specified.
2. All dimensions are in inches and (millimeters).
3. Drawing 295003 forms a part of this drawing.

SURFACE MOUNT PACKAGES

20 PIN PLASTIC LEADED CHIP CARRIER TYPE N



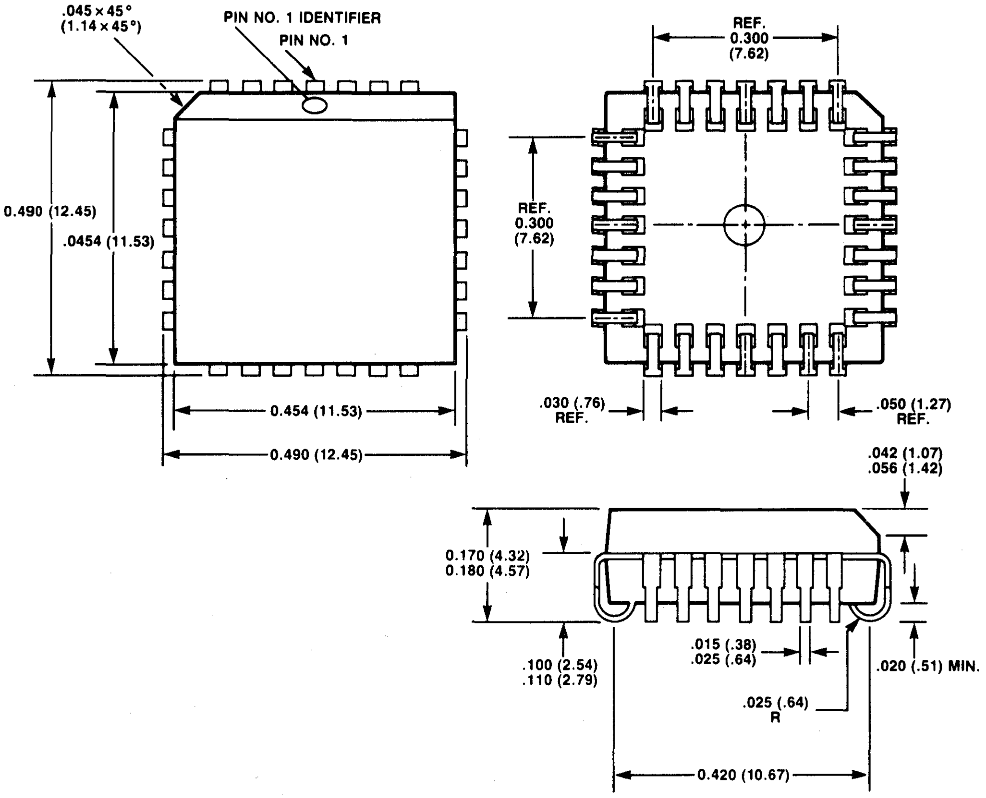




NOTES
1. All dimensions in inches and (millimeters).
2. All tolerances shall be ± .003 (.08) unless otherwise specified.
3. Dimensions do not include mold flash. Max allowable flash is .008 (.20).

SURFACE MOUNT PACKAGES

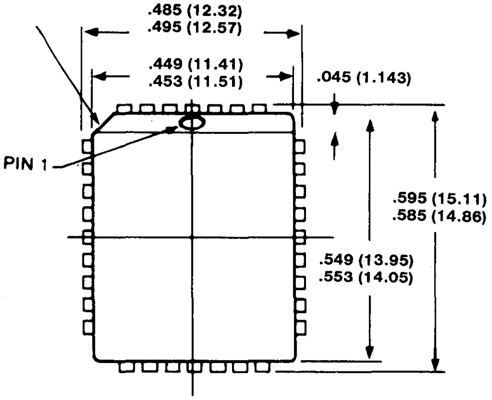
28-PIN PLASTIC LEADED CHIP CARRIER TYPE N

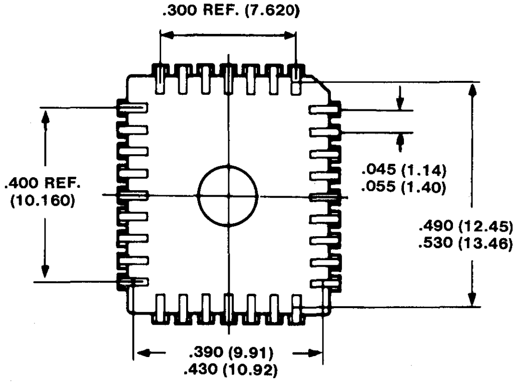


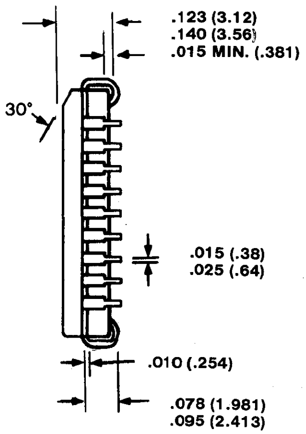
Notes:
1. All dimensions in inches and (millimeters).
2. All tolerences shall be ± .003 (.08) unless otherwise specified.
3. Dimensions do not include mold flash. Maximum allowable flash is .008 (.20)

SURFACE MOUNT PACKAGES

32 PIN PLASTIC LEADED CHIP CARRIER TYPE N



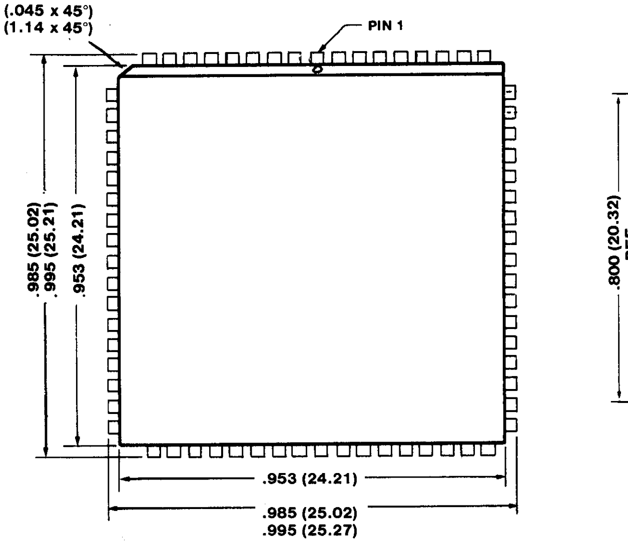


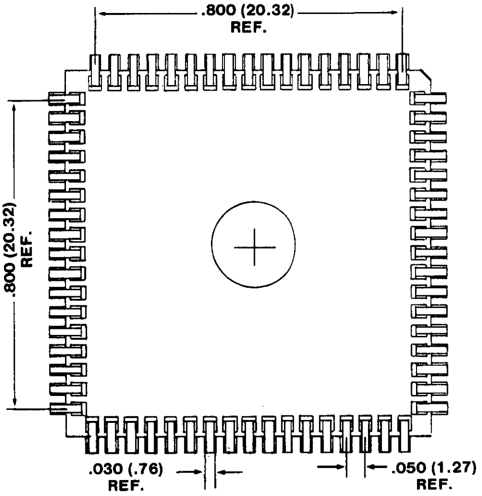


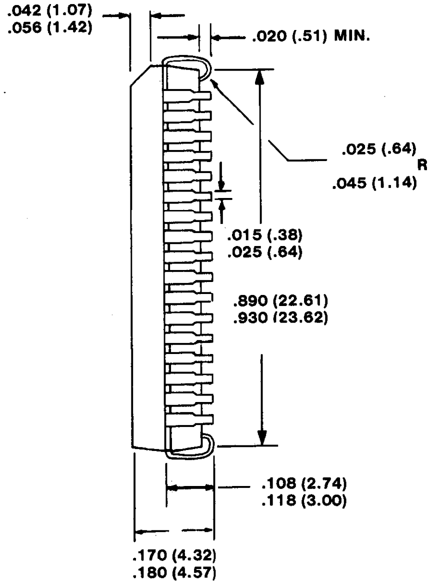
NOTES
1. All dimensions in inches and (millimeters).
2. All tolerances shall be ± .003 (.076)
   unless otherwise specified.
3. Dimensions do not include mold flash.
   Max allowable flash is .008 (.20).

SURFACE MOUNT PACKAGES

68 PIN PLASTIC LEADED CHIP CARRIER TYPE N



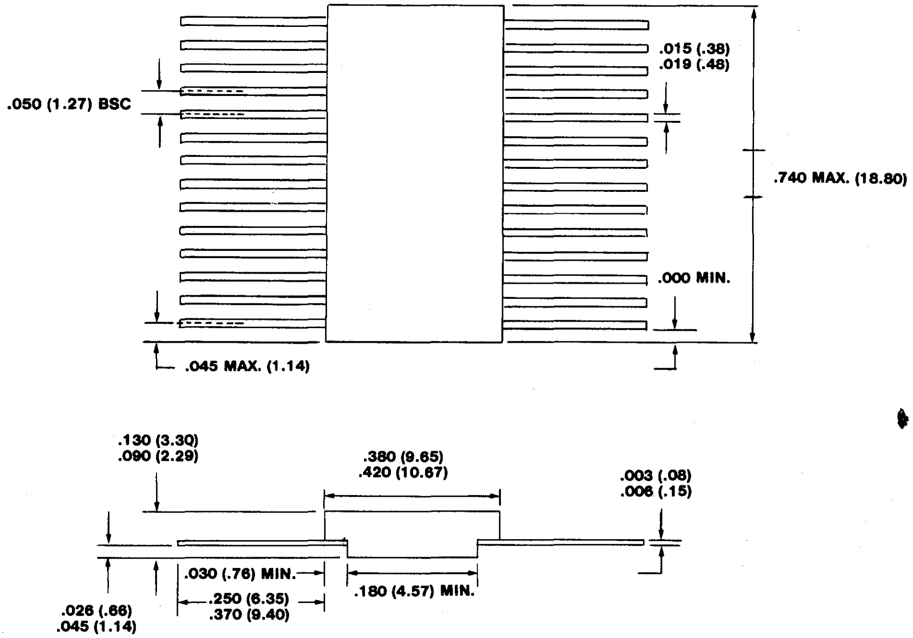




NOTES
1. All dimensions are in inches and (millimeters).
2. Tolerances are ± .003 (.08) unless otherwise specified.
3. Dimensions do not include mold flash. Max. allowable flash is .008 (.20).

SURFACE MOUNT PACKAGES

28-LEAD HERMETIC CERAMIC FLATPACK TYPE F



NOTES
1. All dimensions are in inches and (millimeters).
2. Tolerances are ± .003 (.076) unless otherwise specified.

SEEQ Die Sales

Many of the SEEQ Technology Products contained in this Data Book are available in unencapsulated die form. Products sold in die form have been specifically screened to a special die sales test flow and are ideally suited for hybrid and memory card applications. After screening, all die are optically inspected per method 2010 condition B of MIL-STD 883C. Die are then placed in waffle packs and enclosed in anti-static vacuum sealed bags prior to shipment.

For your reference, the following pages detail product specific bond pad locations and die dimensions for the SEEQ products available in die form. Contact the factory or your local SEEQ representative for additional information.


20
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18
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22
23
24
1
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14
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6
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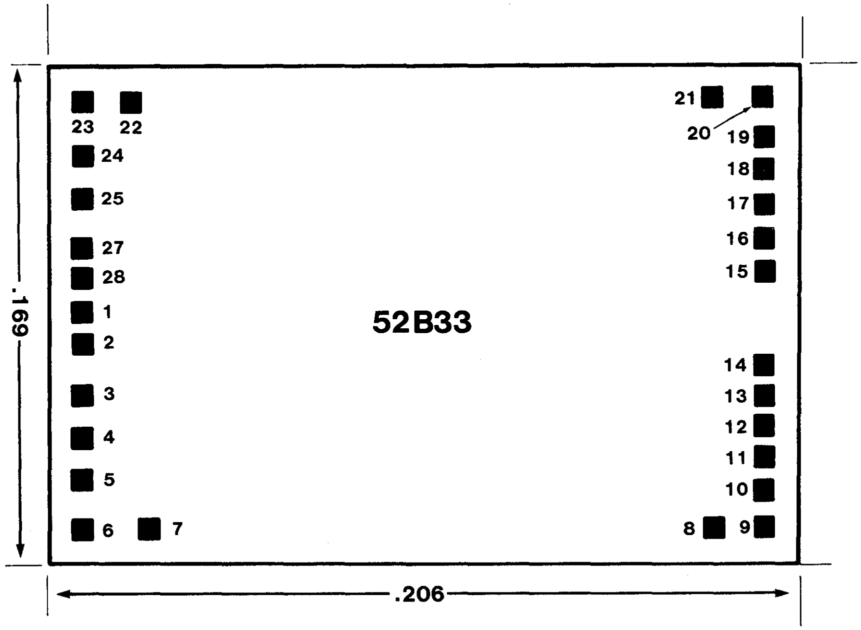
8
52B13
.113
.161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28
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52B33
14
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12
11
10
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4
5
6
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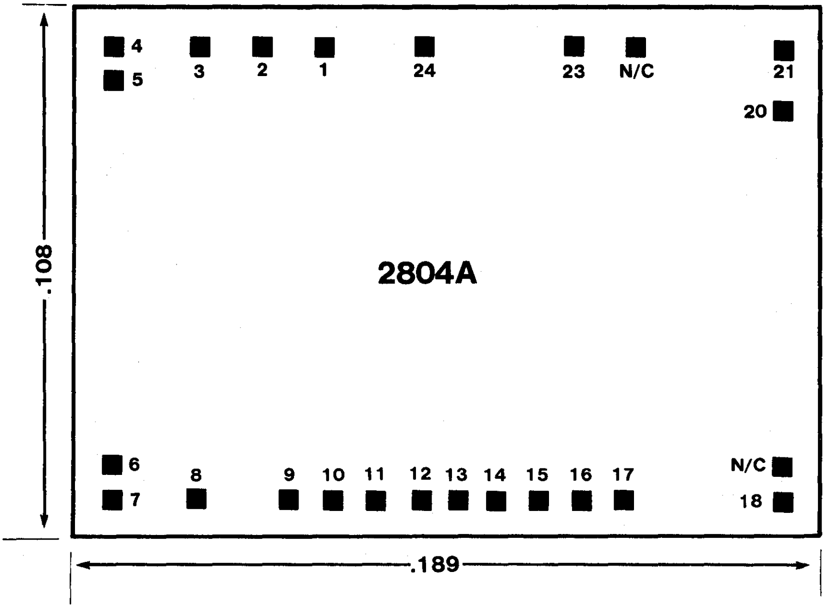
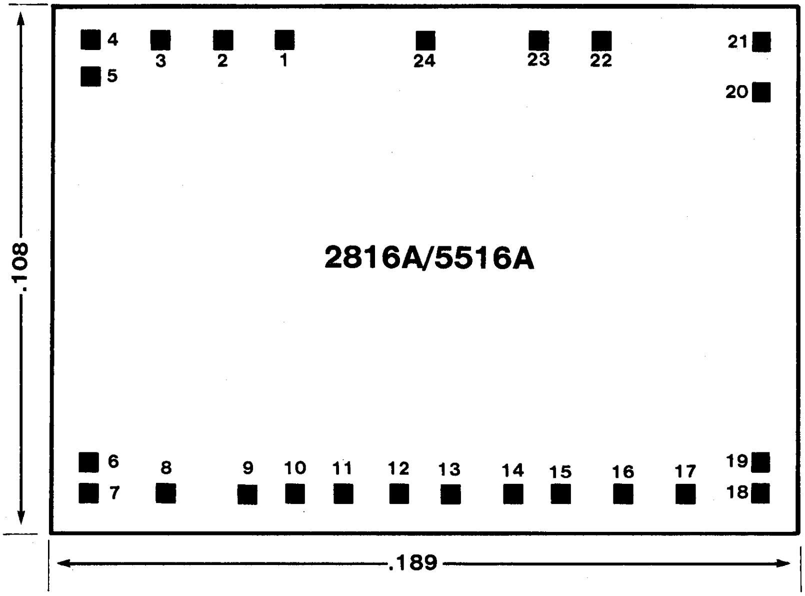
.169
.206


4
5
3
2
1
24
23
N/C
21
20
.108
2804A
6
7
8
9
10
11
12
13
14
15
16
17
N/C
18
.189



.108
.189
2816A/5516A
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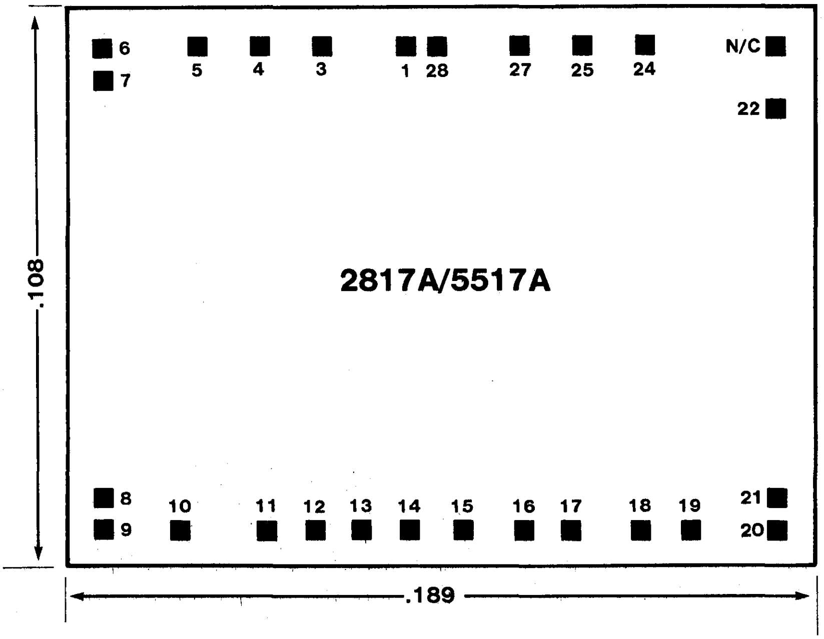
6
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2817A/5517A
.108
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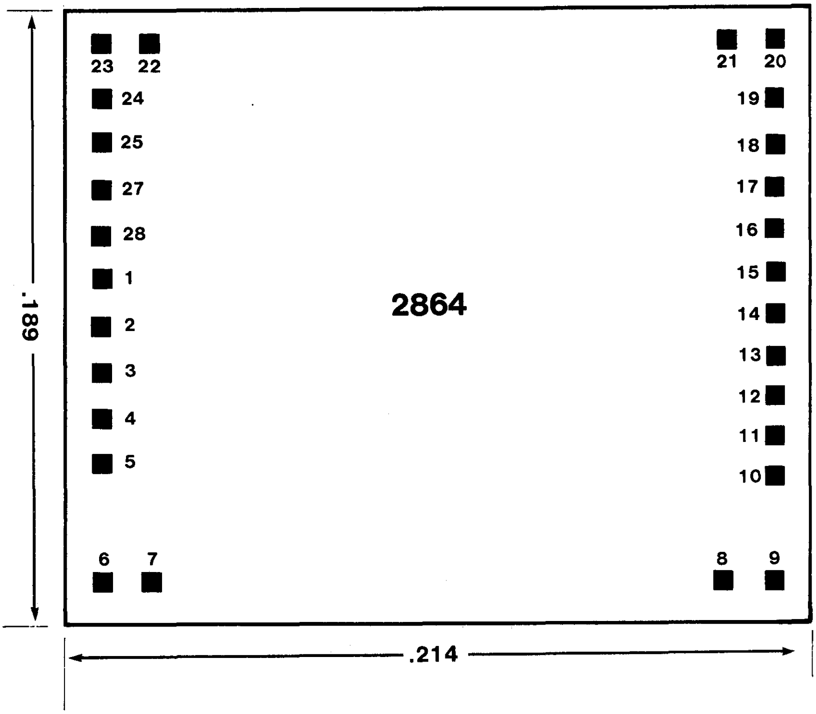
19
21
9
20
.189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2864
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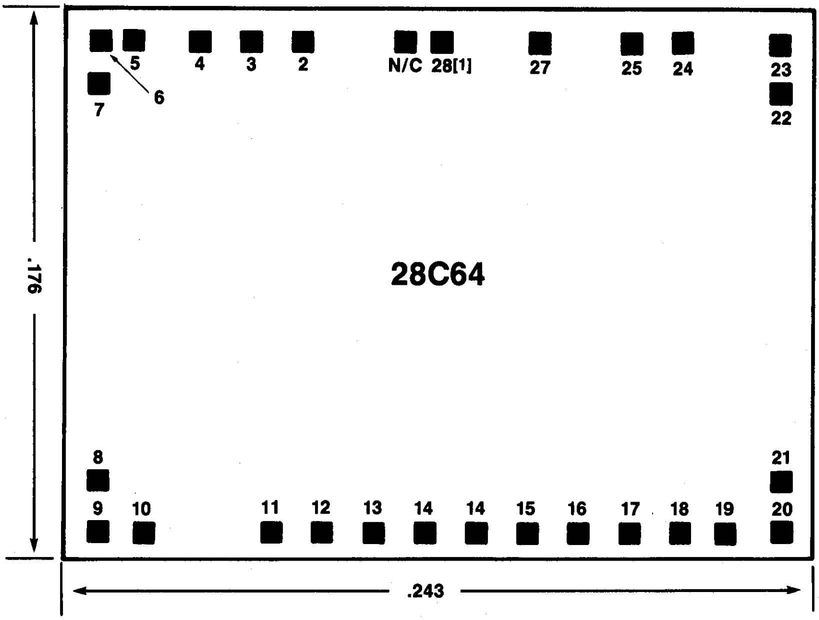
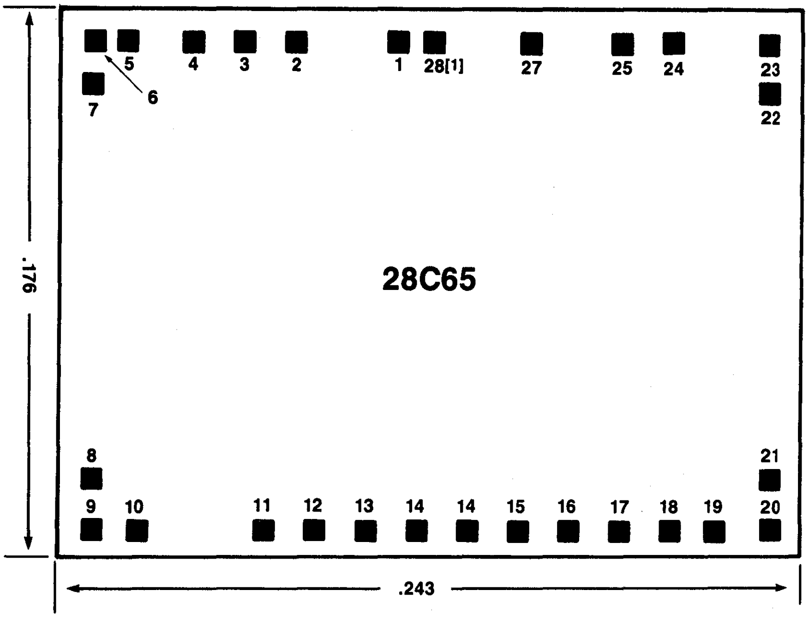
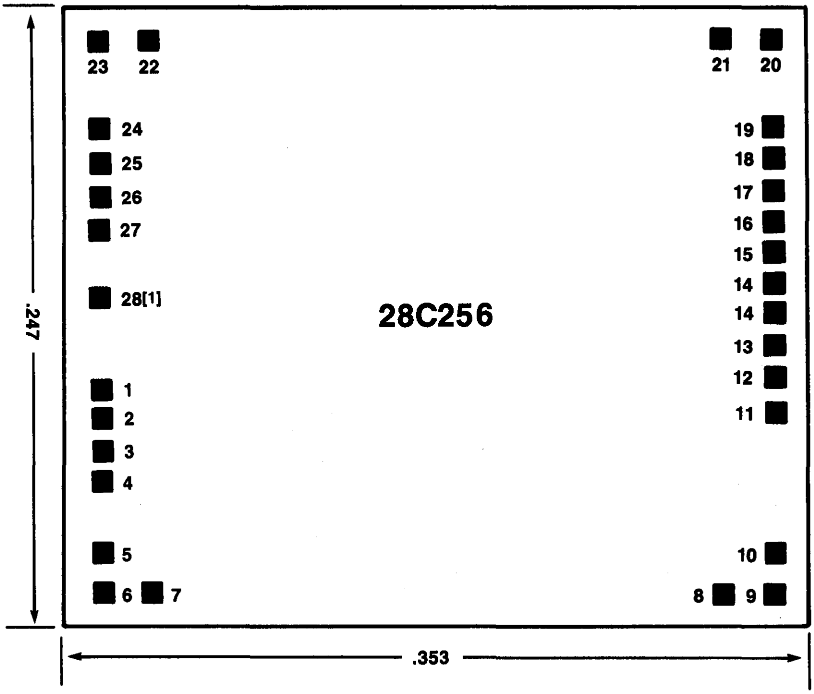
.189
.214



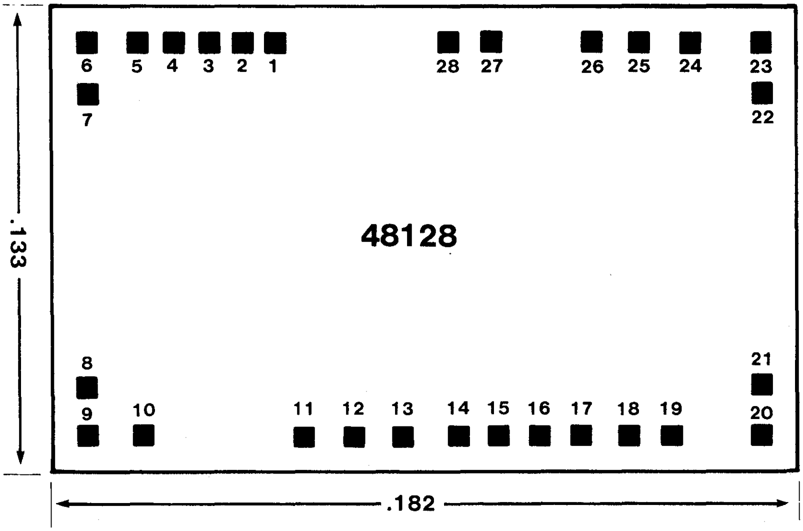
NOTE:
1. Should be double bonded.



NOTE:
1. Should be double bonded.



NOTE:
1. Should be double bonded.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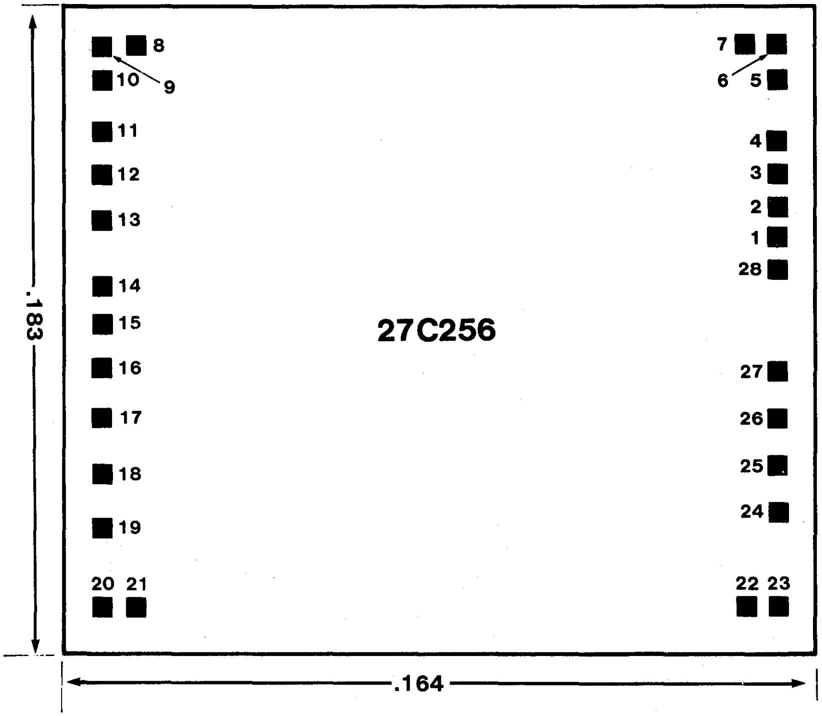
.133
.182



27C256
.183
.164
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Farsoe
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Stuttgart
Tel: 49(711)76 40 33

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Reptronic
Paris
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Bangalore
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Moxel
Milano
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Corporation (JMC)
Kawasaki-City
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Osaka City
Tel: (0/6) 325 0880

Korea
Hanaro
Seoul
Tel: (02) 783-7141

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Electronics Manudax
Heeswijk-Dinther
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Arcobel
OSS
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